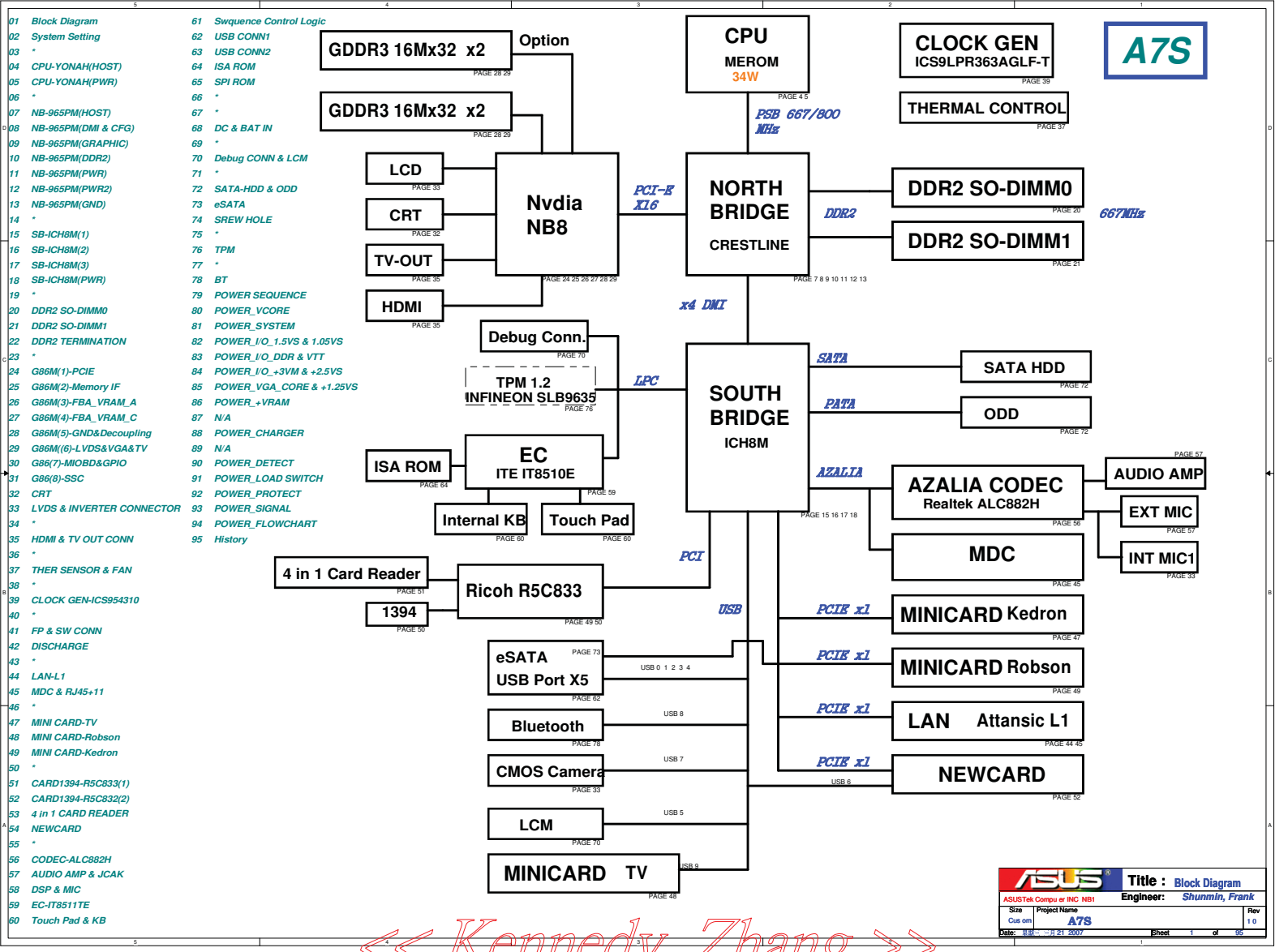


ASUSTek Computer INC NB1

Title : Block Diagram

Engineer: Shunmin, Frank

Size	Project Name	Rev
Custom	A7S	1.0

Date: 星期二, 二月 21, 2007 Sheet 1 of 95

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	/	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	I/0
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
165	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	GAIN_AMP#_K	O
87	ADC4/GPE0	COLOREN#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7	/	
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANTON#	I
113	FA16/GPG0	FA16\	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	CPUPWR_GD#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_ON	O
75	GPH5	SUSB_ON	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BTLED_ON	I/O
AC18	GPIO07	WLA LED_EN	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	WLAN_ON#	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13		
R4	GPIO14		
E22	GPIO15	CB_SD#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	TP_LEDON	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	CPU_Select	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24		
D20	GPIO25		
A21	GPIO26/EL_RSVD		
B21	GPIO27/EL_STATE0	PD_DET#	I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC#5	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC#7	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O
U2	GPIO34/AZ_DOCK_RST#		
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP		
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	A
1394	AD17	0	B

PCIE Device	Bus
L1	PE(T/R)(p/n)1
MINI_CARD Kedron	PE(T/R)(p/n)2
NEWCARD	PE(T/R)(p/n)3
MINI_CARD Robson	PE(T/R)(p/n)4
eSATA	PE(T/R)(p/n)5
MINI_CARD TV	PE(T/R)(p/n)6

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(MAX6657)	0100110x (4C)
VGA Thermal Sensor(MAX6649)	0100110x (4C)

Pins	Pin Name	Devices
3	PCICLK3	TPM
4	PCICLK4	CardBus R5C832
5	SELPCIEX0_LCD#/PCICLK5	EC IT8510E
8	ITP_EN/PCICLK_F0	ICH7
9	SELLCD_27#/PCICLK_F1	x
12	FSLA/USB_48MHz	ICH7
14	DOTT_96MHz	x
15	DOTC_96MHz	x
17	27FIX/LCD_SSCGT/PCIEX0T	G72/G73
18	27SS/LCD_SSCGC/PCIEX0C	G72/G73
19	PCIEXT1	x
20	PCIEXC1	x
22	PCIEXT2	ICH7
23	PCIEXC2	ICH7
24	PCIEXT3	MCH
25	PCIEXC3	MCH
26	SATACLKT	ICH7
27	SATACLKC	ICH7
30	PCIEXT4	LAN
31	PCIEXC4	LAN
35	PCIEXT5	G72/G73
36	PCIEXC5	G72/G73
38	PCIEXT6	MINICARD
39	PCIEXC6	MINICARD
40	PERBQ2#/PCIEXC7	NEWCARD
41	PERBQ1#/PCIEXT7	MINICARD
43	CPUCLKC2_ITP/PCIEXC8	NEWCARD
44	CPUCLKT2_ITP/PCIEXT8	NEWCARD
48	CPUCLKC1	MCH
49	CPUCLKT1	MCH
51	CPUCLKC0	CPU
52	CPUCLKT0	CPU
57	X2	14.318
58	X1	14.318
60	REF0	ICH7
61	REF1/FSLC/TEST_SEL	x

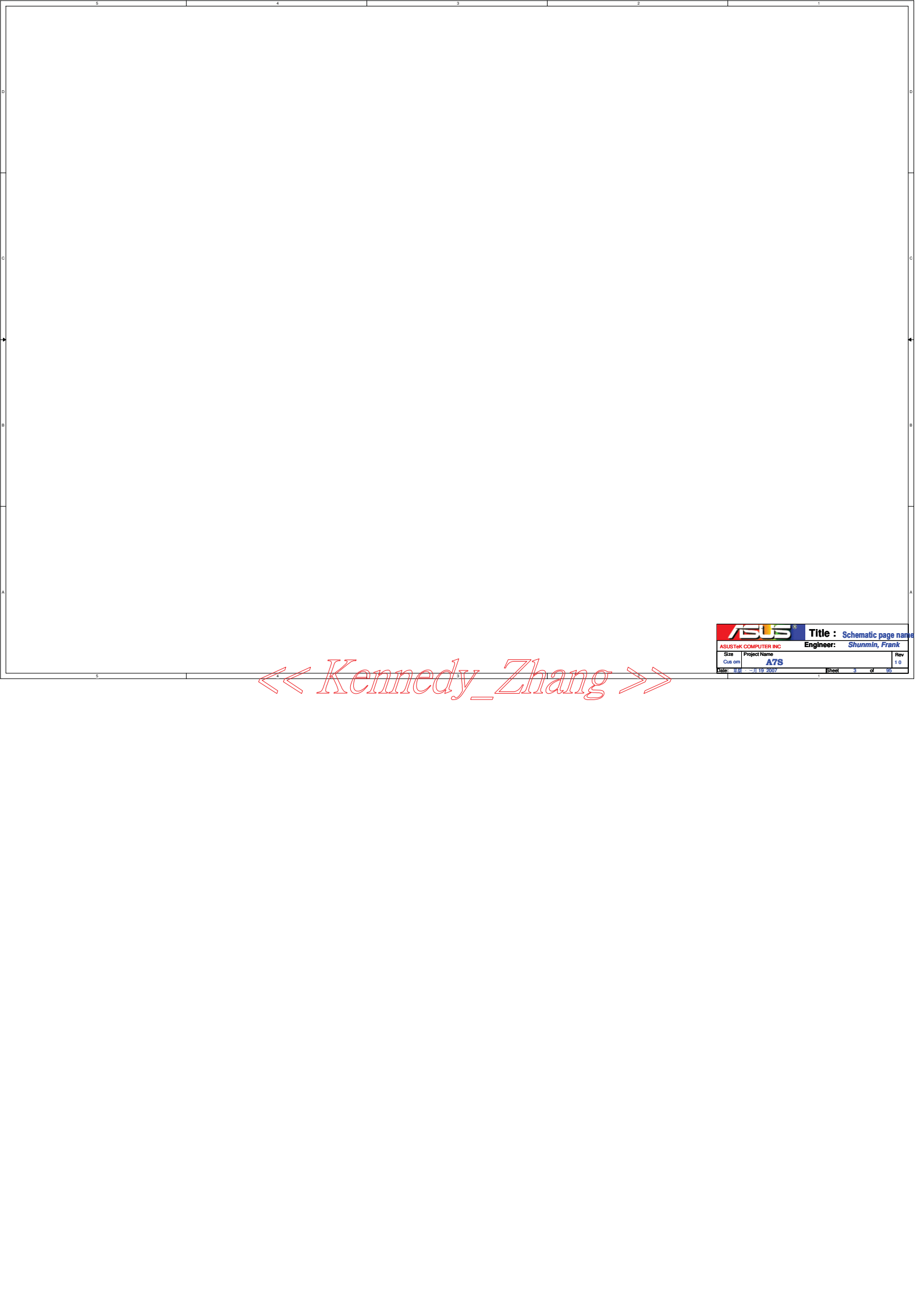
ASUSTek Computer INC NB1

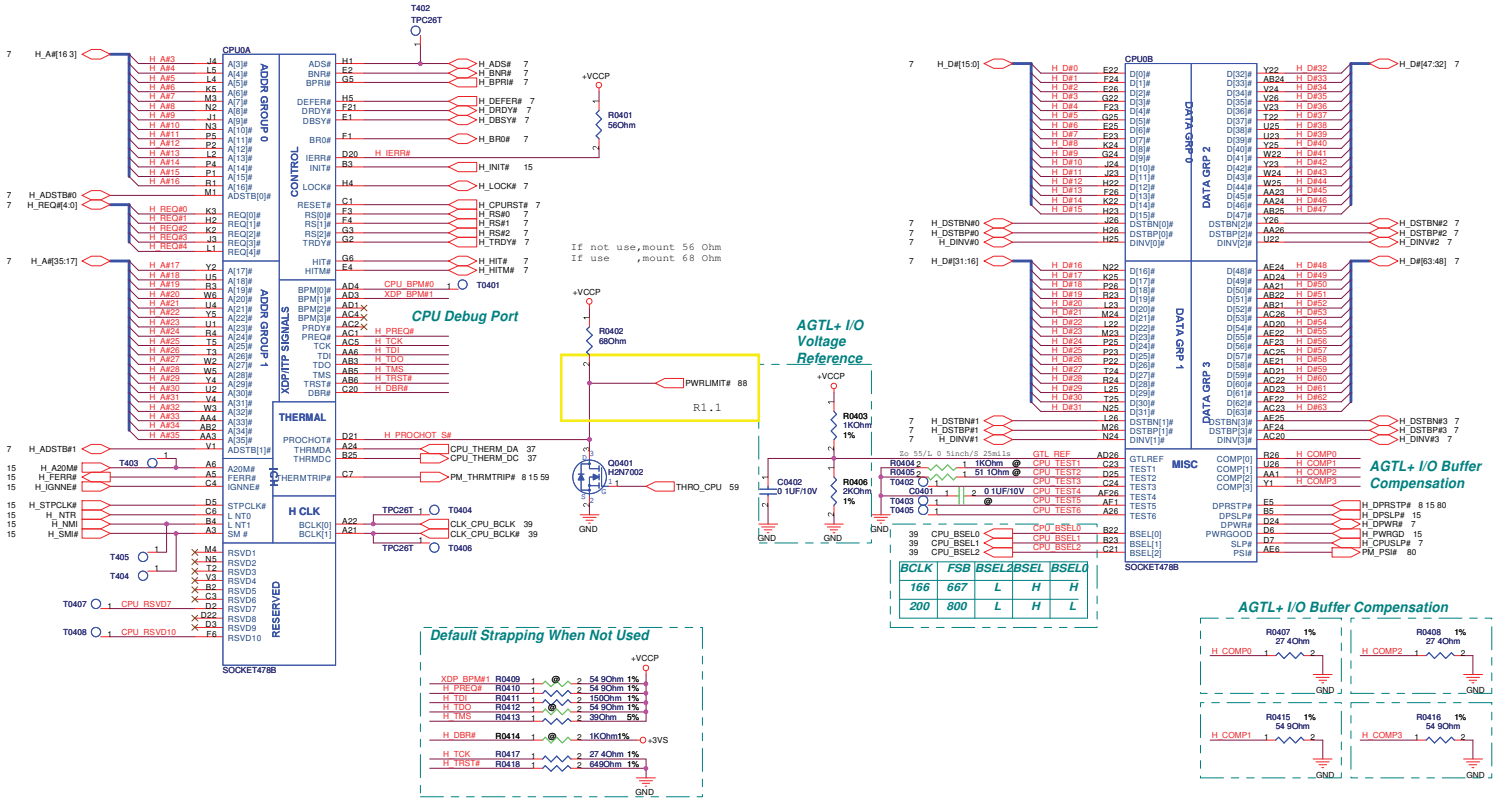
Title : <Title>

Engineer: Shunmin, Frank

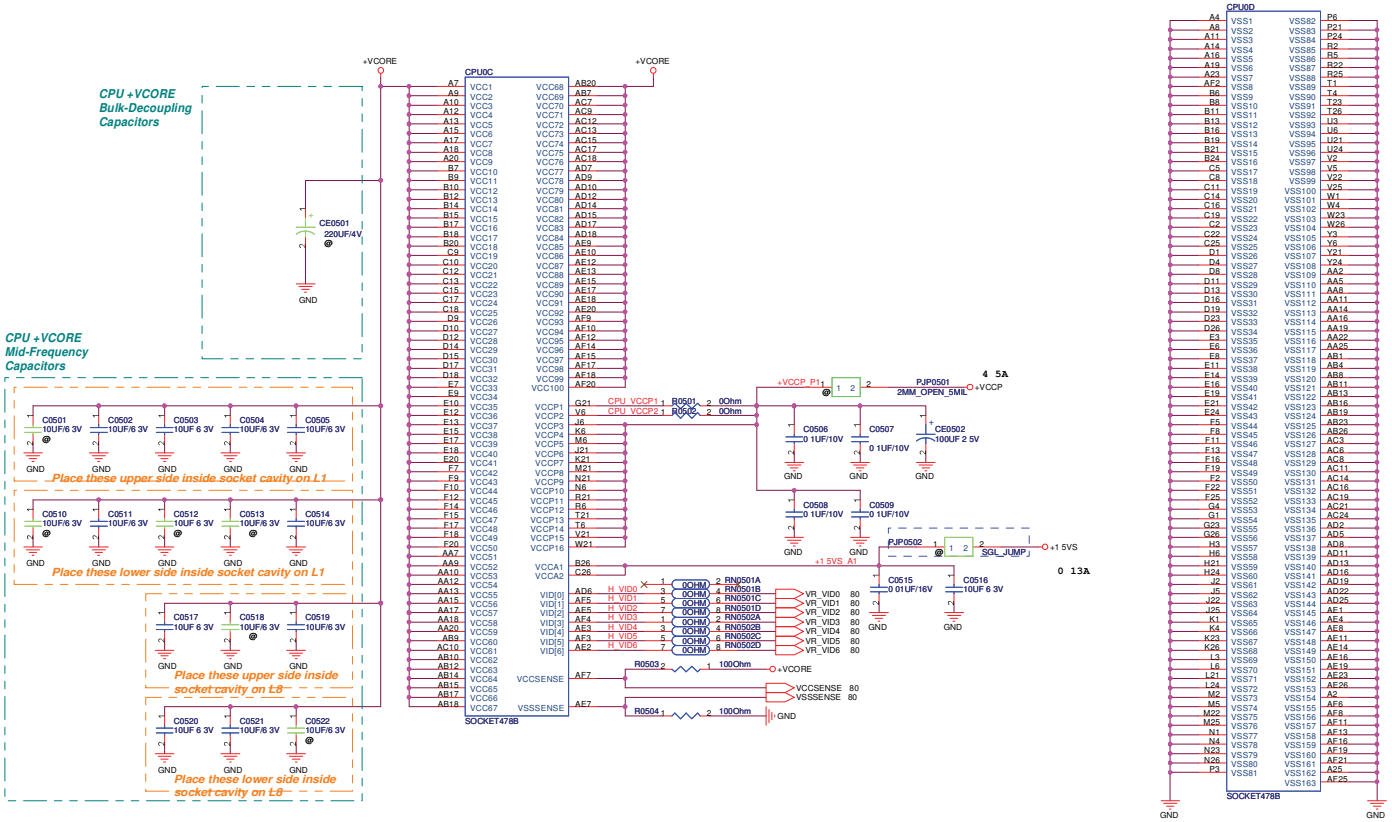
Size: Custom | Project Name: A7S | Rev: 1.0

Date: 星期 一 一月 19 2007 | Sheet 2 of 95





Title :	CPU-Merom(HOST)	
ASUSTeK COMPUTER INC NB1	Engineer:	Shunmin, Frank
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 二月 19 2007	Sheet 4 of 95	



+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
F3S: 10UF *16
A7S: 10UF *10 ....11/17
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
F3S: 100UF *1, 0.1UF *4

ASUSTeK COMPUTER INC NB1	Title : CPU_Merom(PWR)	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 月 19 2007	Sheet 5 of 95	

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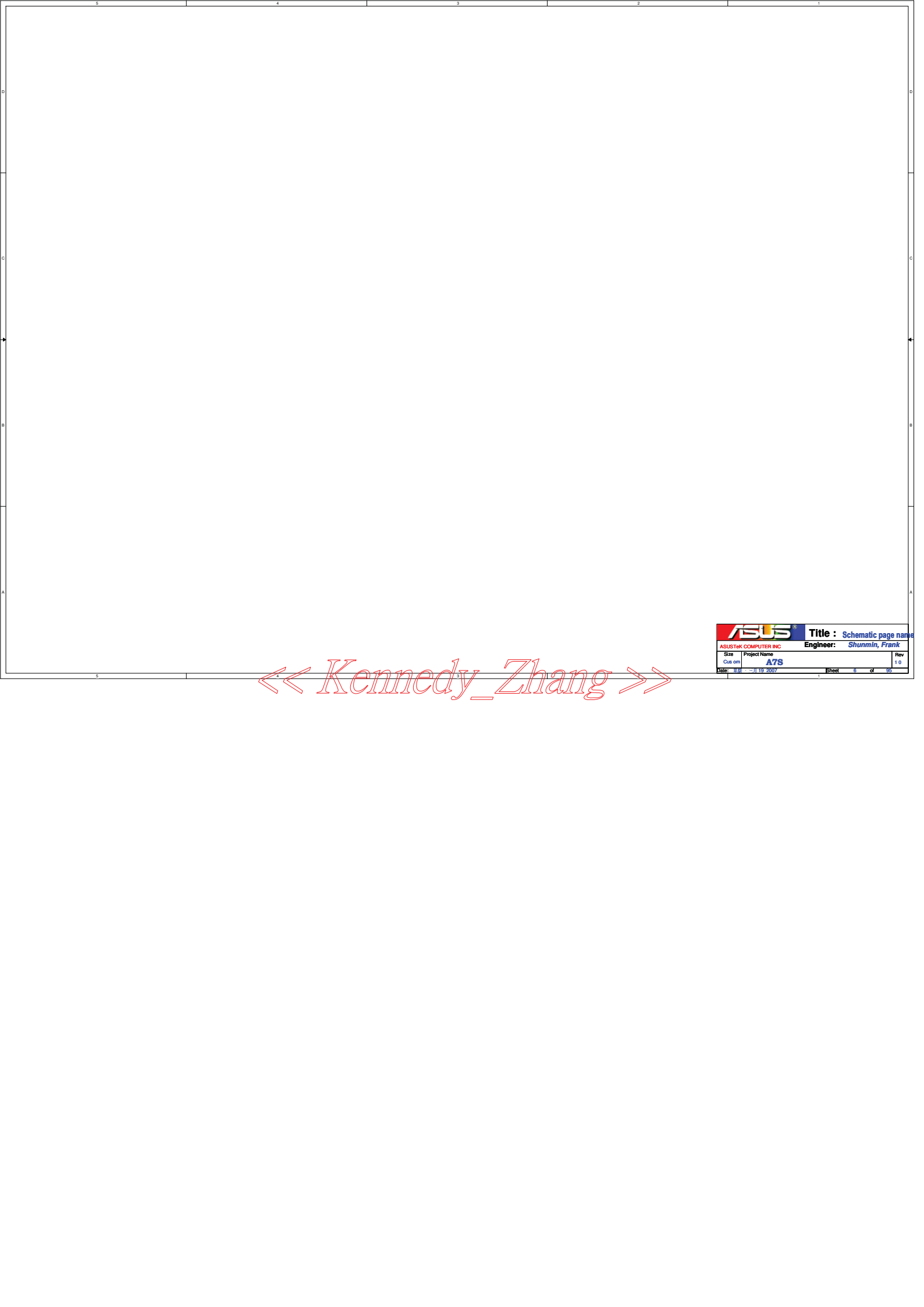
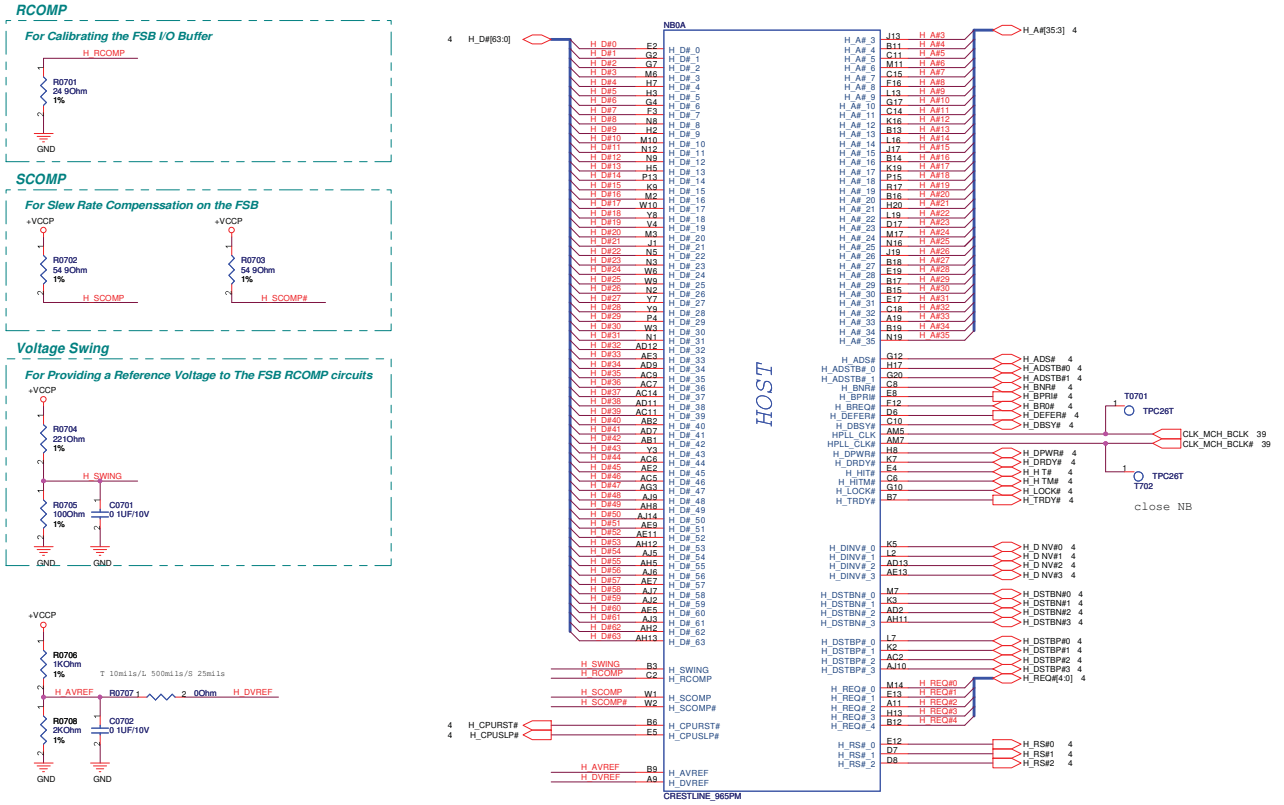




ASUSTeK COMPUTER INC NB1

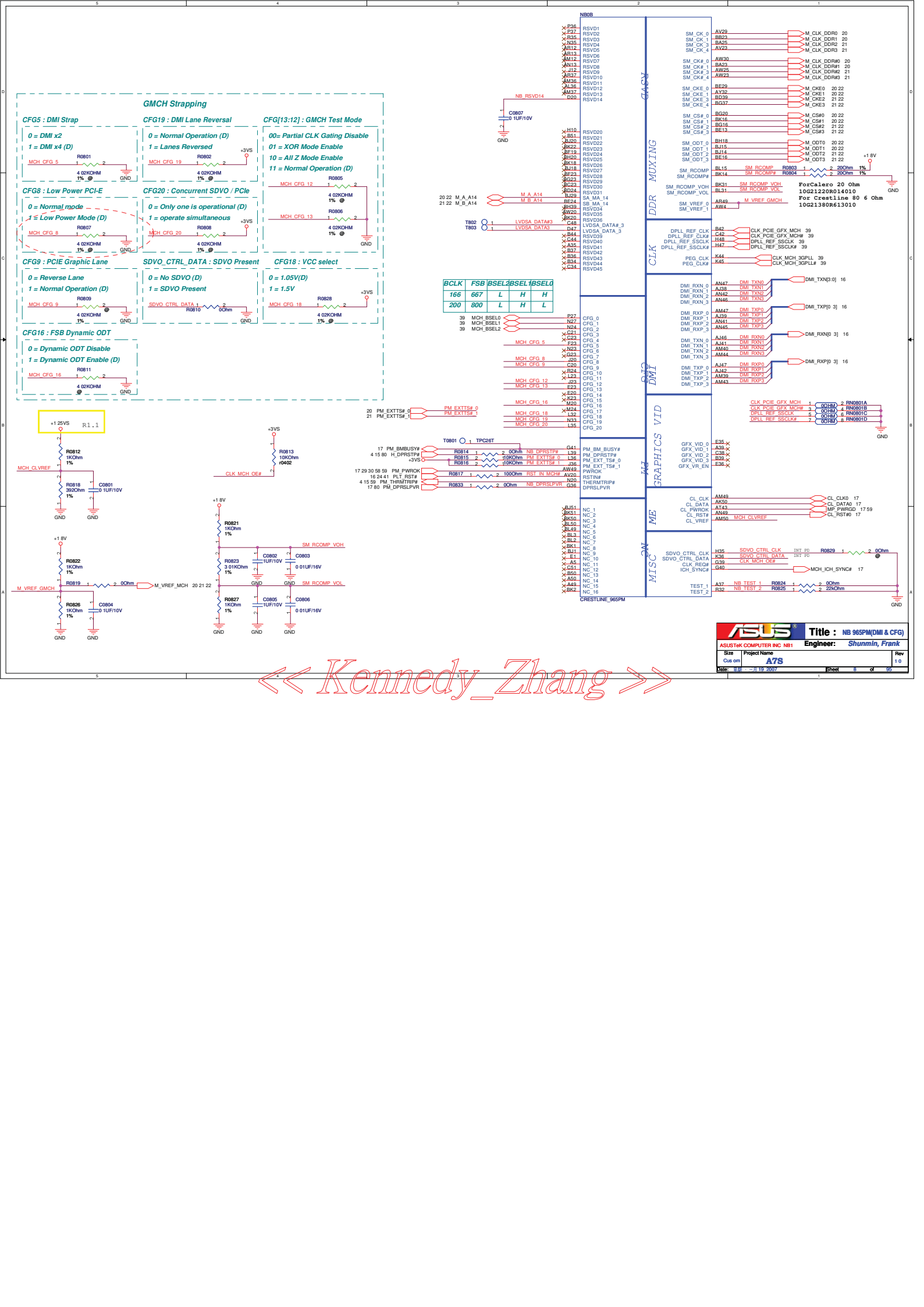
Title : NB-965PM(HOST)

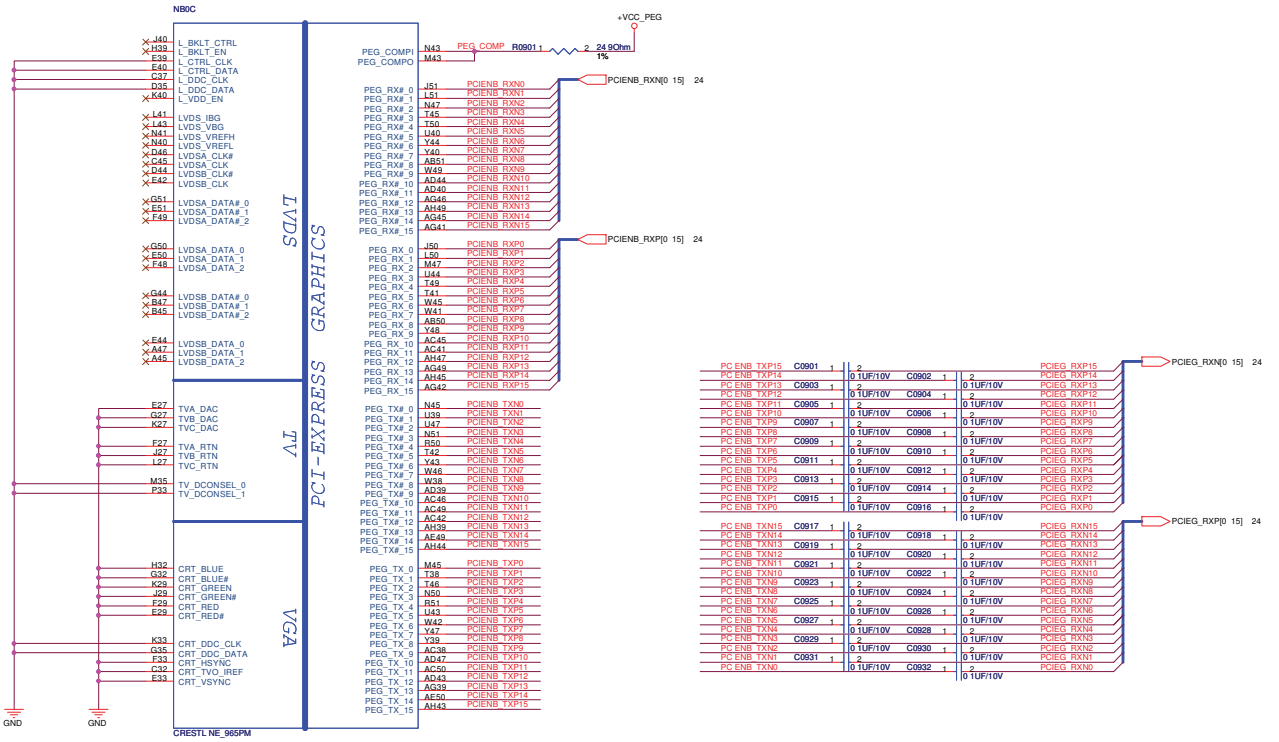
Engineer: Shunmin, Frank

Size	Project Name	Rev
Cus om	A7S	1 0

Date: 星期 二 一月 20 2007 Sheet 7 of 95

<< Kennedy_Zhang >>

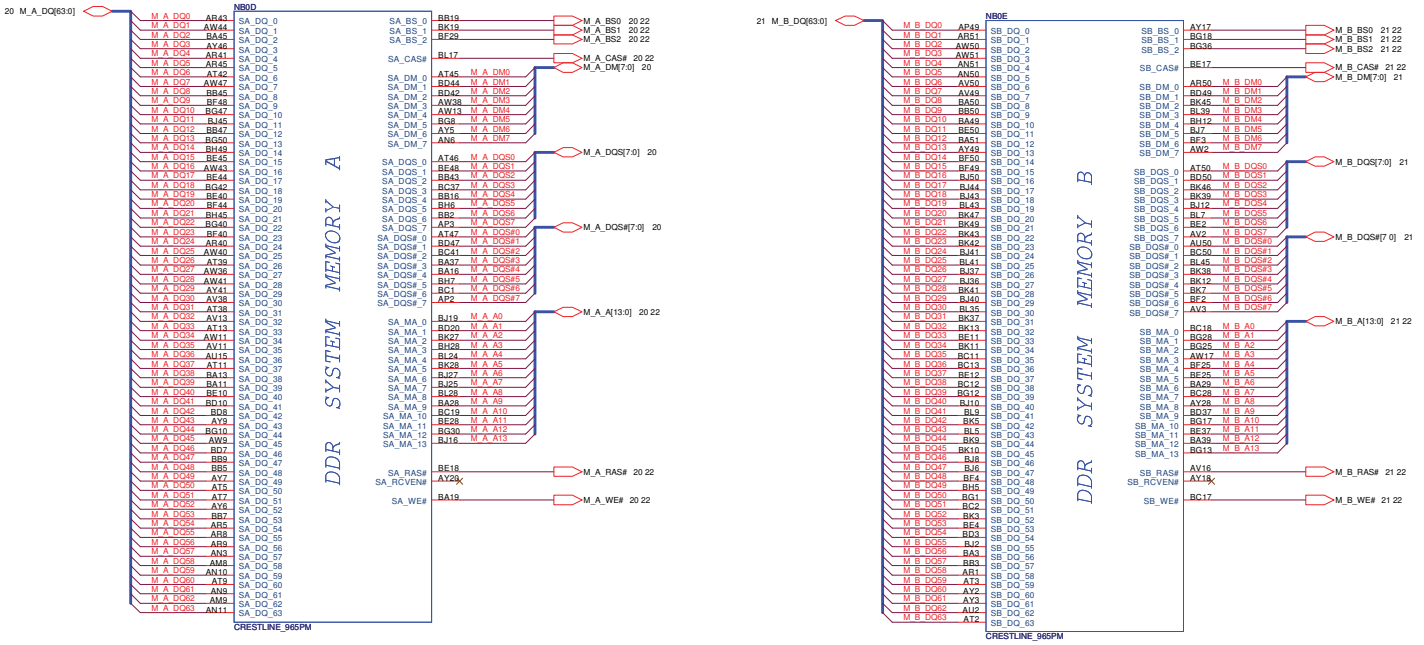

GMCH Strapping
CFG5 : DMI Strap
0 = DMI x2
1 = DMI x4 (D)
CFG19 : DMI Lane Reversal
0 = Normal Operation (D)
1 = Lanes Reversed
CFG[13:12] : GMCH Test Mode
00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)
CFG8 : Low Power PCI-E
0 = Normal mode
1 = Low Power Mode (D)
CFG20 : Concurrent SDVO / PCIe
0 = Only one is operational (D)
1 = operate simultaneous
CFG9 : PCIE Graphic Lane
0 = Reverse Lane
1 = Normal Operation (D)
SDVO_CTRL_DATA : SDVO Present
0 = No SDVO (D)
1 = SDVO Present
CFG18 : VCC select
0 = 1.05V(D)
1 = 1.5V
CFG16 : FSB Dynamic ODT
0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)
NB0B
CRESTLINE_965PM
GMCH
DDR MUXING
CLK
DMI
VID
GRAPHICS
ME
MISC
Title : NB 965PM(DMI & CFG)
ASUSTeK COMPUTER INC NB1
Engineer: Shunmin, Frank
Project Name A7S
Rev 1.0
Sheet 8 of 95
<< Kennedy_Zhang >>



R1.1 Remove all 965GM components

Title :	NB_965PM(GRAPHIC)
ASUSTeK COMPUTER INC NB1	Engineer: Shunmin, Frank
Size: Cus om	Project Name: A7S
Rev: 1 0	
Date: 星期 一月 19 2007	Sheet 9 of 95

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC NB1

Title : NB-965PM(DDR2)

Engineer: Shunmin, Frank

Size	Project Name	Rev
Cus om	A7S	1 0

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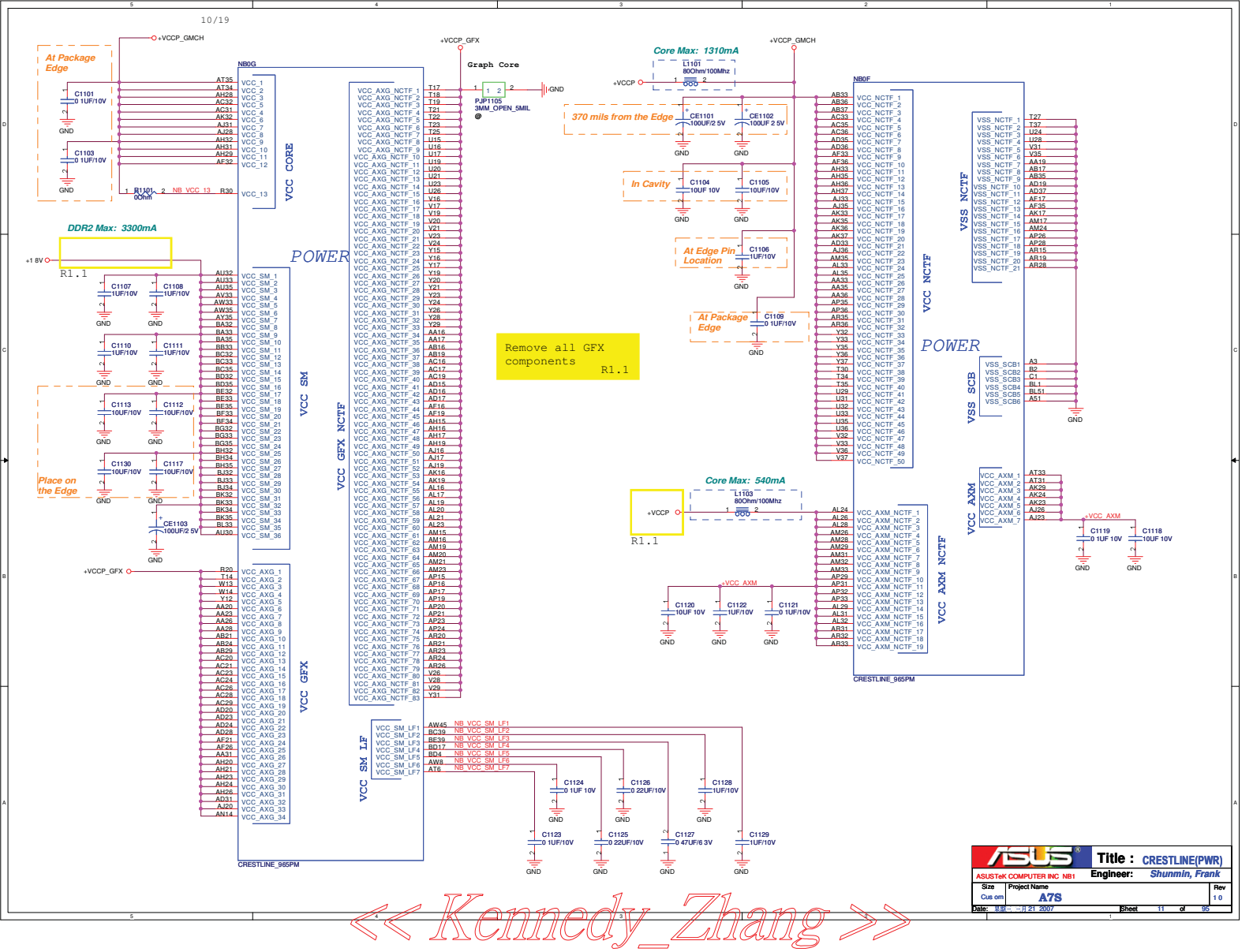
10/19
+VCCP_GMCH
At Package Edge
C1101 0 1UF/10V
C1103 0 1UF/10V
GND
R1101 0ohm
NB_VCC_13
R30
NB0G
VCC_CORE
VCC_13
DDR2 Max: 3300mA
+1.8V
R1.1
C1107 1UF/10V
C1108 1UF/10V
C1110 1UF/10V
C1111 1UF/10V
C1113 10UF/10V
C1112 10UF/10V
C1130 10UF/10V
C1117 10UF/10V
Place on the Edge
CE1103 100UF/2.5V
POWER
VCC_SM
VCC_GFX_NCTF
+VCCP_GFX
VCC_GFX
VCC_SM_LF
CRESTLINE_965PM
Graph Core
PJP1105 3MM_OPEN_5MIL
@
+VCCP_GFX
Core Max: 1310mA
L1101 80Ohm/100Mhz
+VCCP
370 mils from the Edge
CE1101 100UF/2.5V
CE1102 100UF 2.5V
In Cavity
C1104 10UF 10V
C1105 10UF/10V
At Edge Pin Location
C1106 1UF/10V
At Package Edge
C1109 0 1UF/10V
Remove all GFX components
R1.1
Core Max: 540mA
L1103 80Ohm/100Mhz
+VCCP
R1.1
+VCC_AXM
C1120 10UF 10V
C1122 1UF/10V
C1121 0 1UF/10V
C1124 0 1UF 10V
C1126 0 22UF/10V
C1128 1UF/10V
C1123 0 1UF/10V
C1125 0 22UF/10V
C1127 0 47UF/6.3V
C1129 1UF/10V
NB0F
VCC_NCTF
VSS_NCTF
VCC_AXM_NCTF
VSS_SCB
VCC_AXM
C1119 0 1UF 10V
C1118 10UF 10V
CRESTLINE_965PM
ASUSTeK COMPUTER INC NB1
Title : CRESTLINE(PWR)
Engineer: Shunmin, Frank
Size: Cus om
Project Name: A7S
Rev: 1.0
Date: 星期二, 二月 21, 2007
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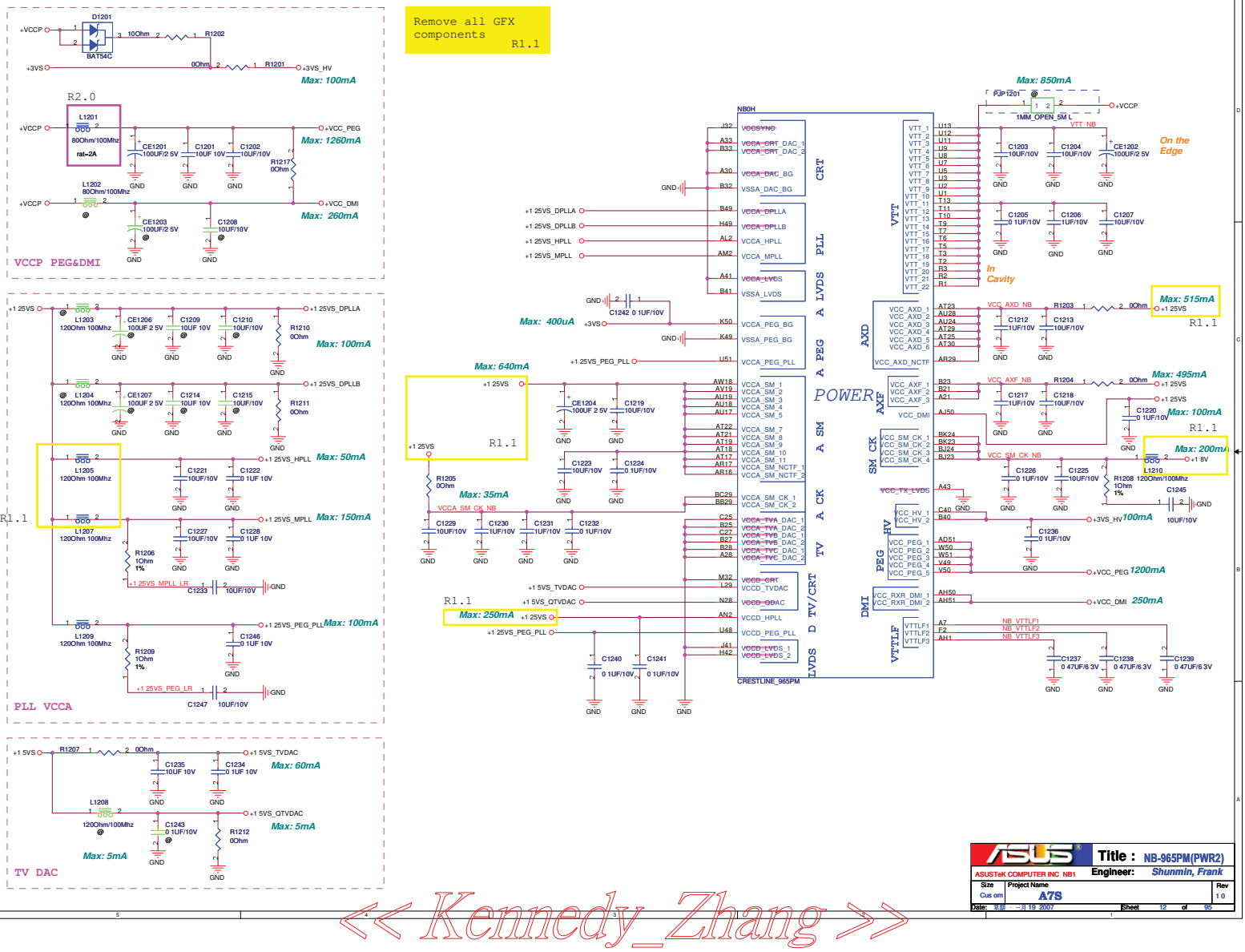
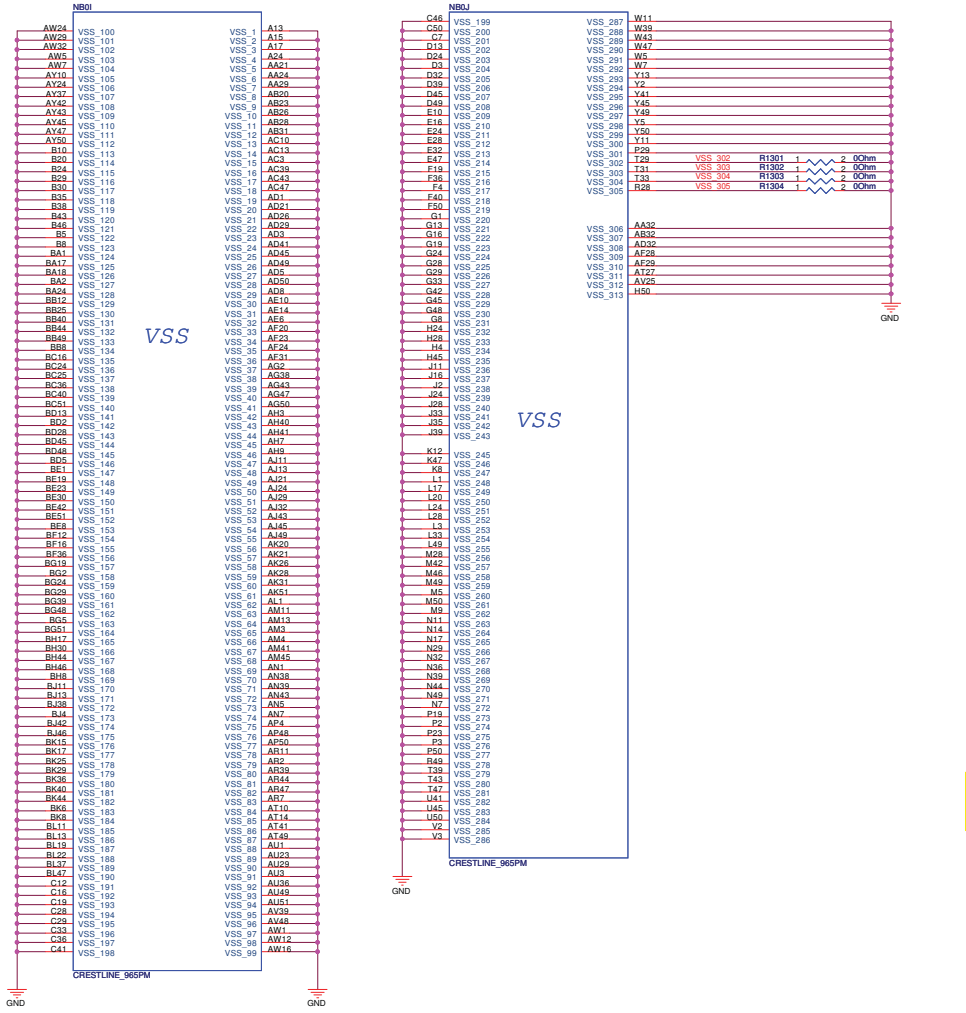
<< Kennedy_Zhang >>

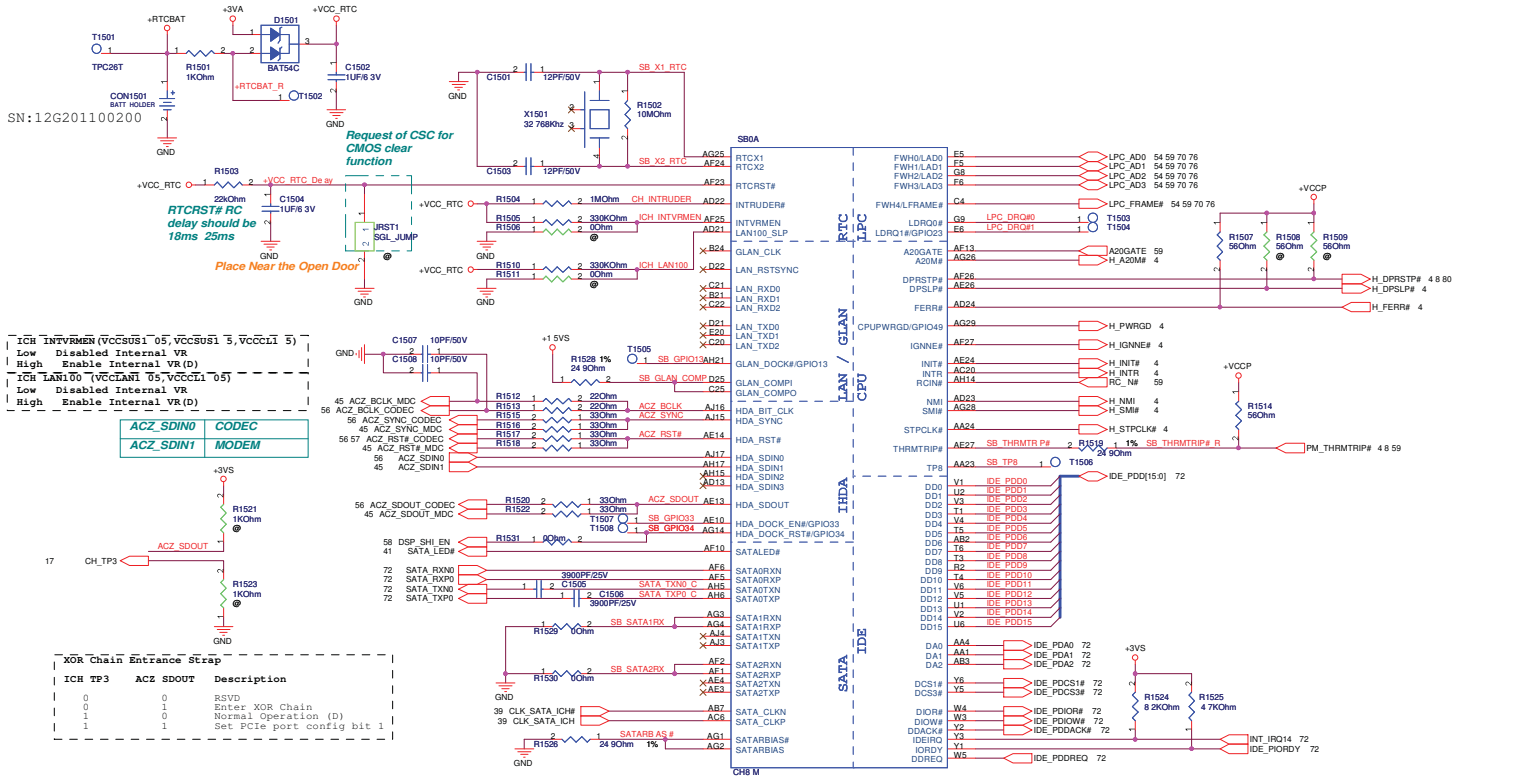

Remove all GFX components
R1.1
VCCP PEG&DMI
PLL VCCA
TV DAC
POWER
NB0H
CRESTLINE_965PM
Max: 850mA
Max: 515mA
Max: 495mA
Max: 100mA
Max: 200mA
Max: 640mA
Max: 400uA
Max: 35mA
Max: 250mA
Max: 1200mA
Max: 250mA
On the Edge
In Cavity
Title : NB-965PM(PWR2)
ASUSTeK COMPUTER INC NB1
Engineer: Shunmin, Frank
Project Name A7S
Rev 1.0
Date: 星期 一 一月 19 2007
Sheet 12 of 95
<< Kennedy_Zhang >>



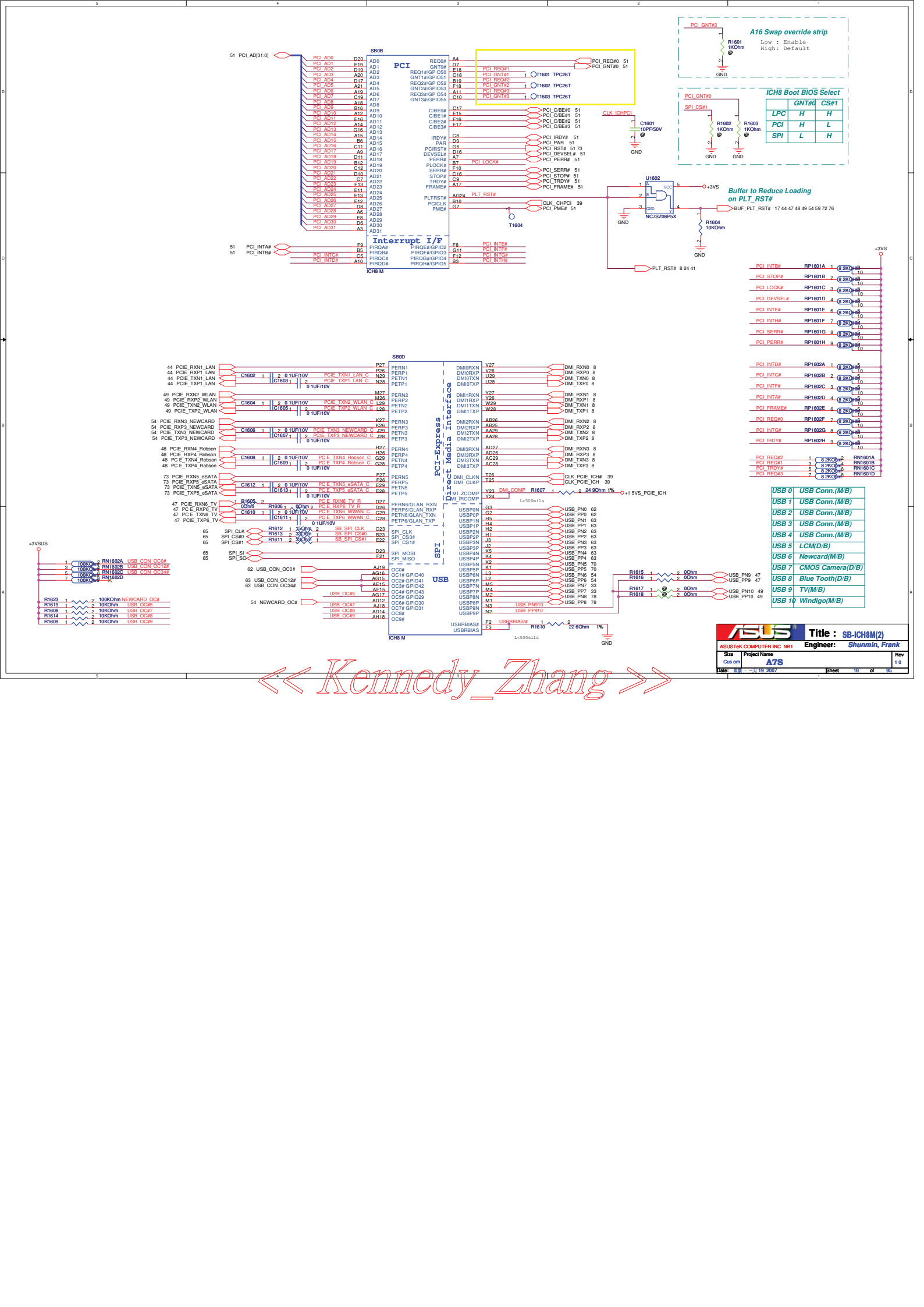
Remove all GFX components R1.1

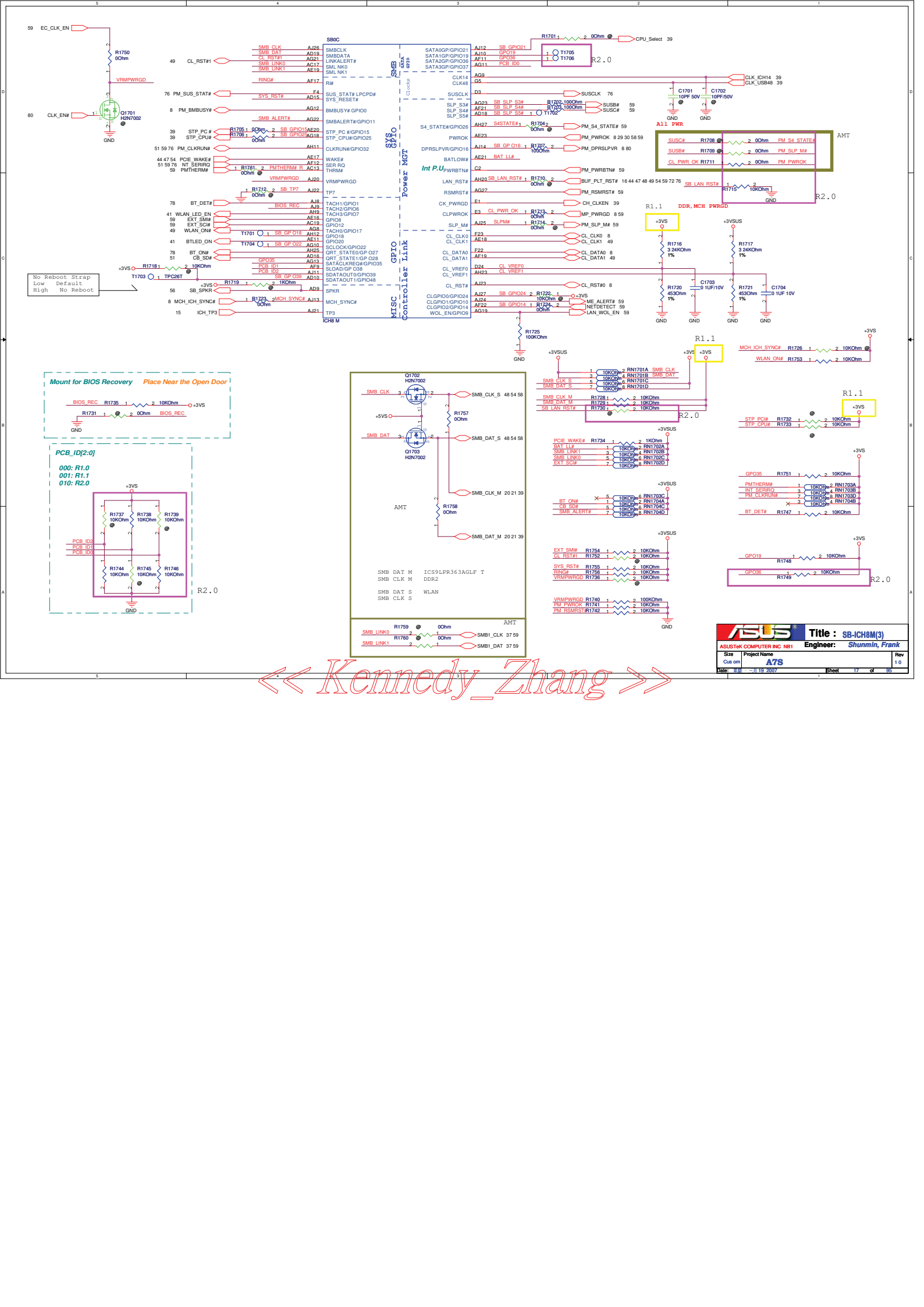
ASUSTeK COMPUTER INC NB1	Title : CRESTLINE(GND)		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 13 of 95		

<< Kennedy_Zhang >>



Title : SB-ICH8M(1)			
ASUSTeK COMPUTER INC NB1	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 二 月 20 2007	Sheet 15 of 95		




SB0C
ICH8 M
SMB
GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
Int P.U
Clocks
No Reboot Strap
Low Default
High No Reboot
Mount for BIOS Recovery
Place Near the Open Door
PCB_ID[2:0]
000: R1.0
001: R1.1
010: R2.0
R2.0
R1.1
AMT
All PWR
DDR_MCH_PWRGD
SMB_DAT_M ICS9LPR363AGLF T
SMB_CLK_M DDR2
SMB_DAT_S WLAN
SMB_CLK_S WLAN
Title : SB-ICH8M(3)
ASUSTeK COMPUTER INC NB1
Engineer: Shunmin, Frank
Size Cus om
Project Name A7S
Rev 1 0
Date: 星期 一 一月 19 2007
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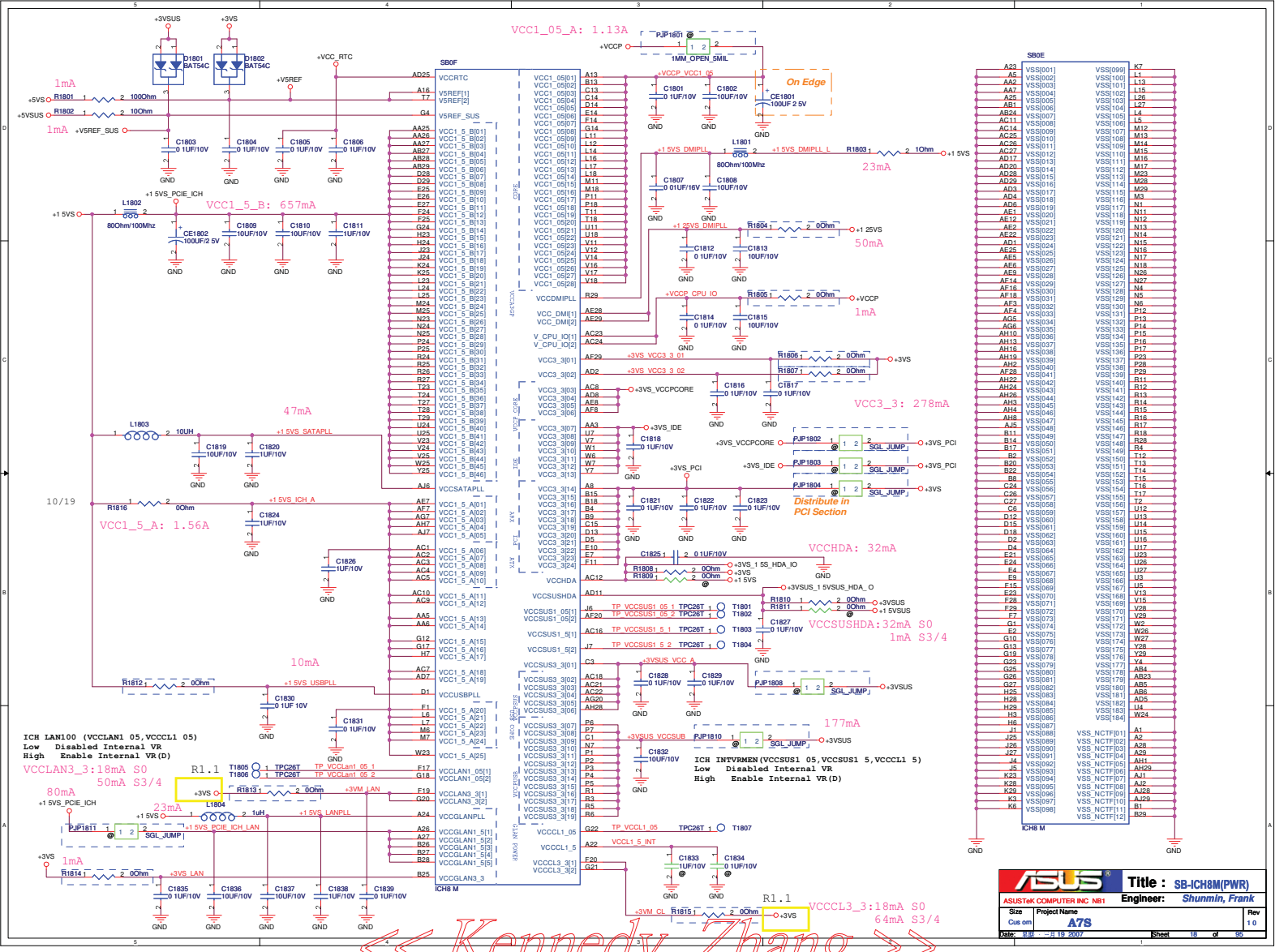
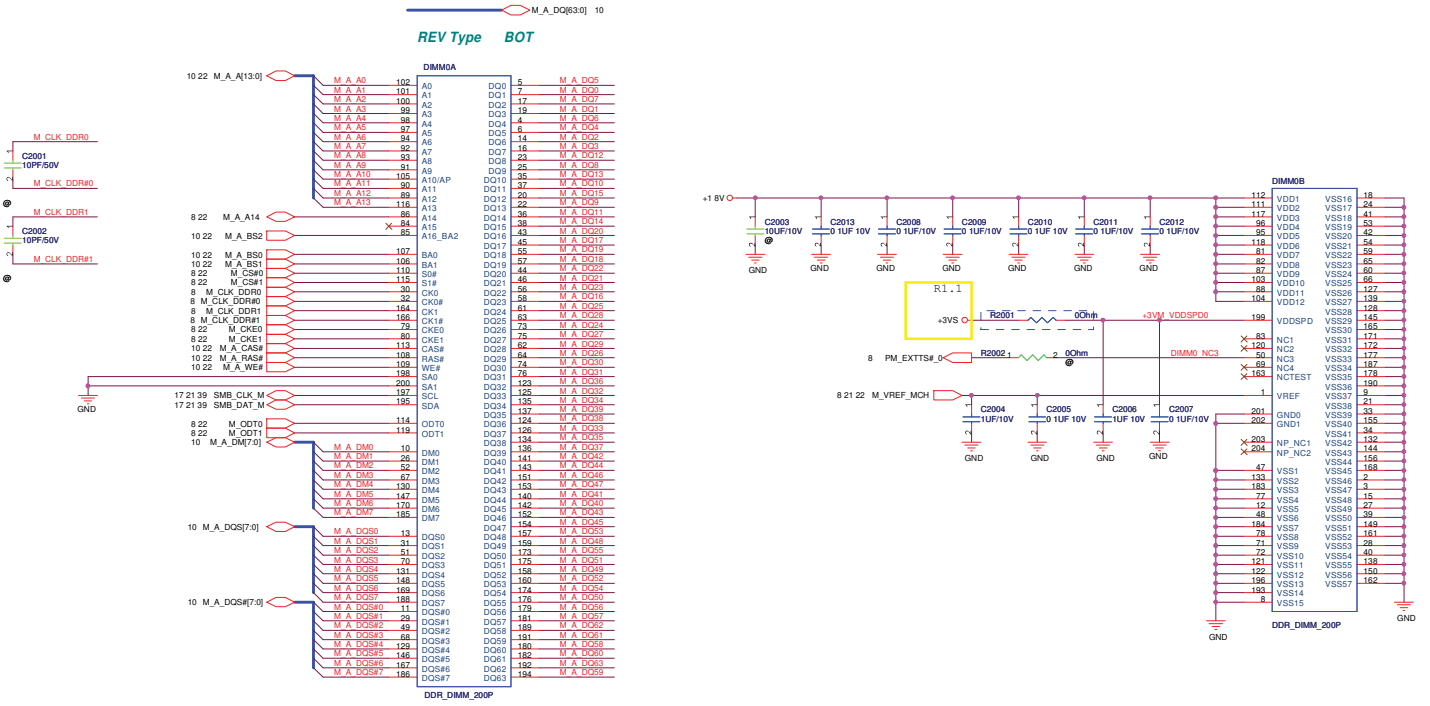
<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC NB1	Title : SB-ICH8M(PWR)		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 月 19 2007	Sheet 18 of 95		

ASUSTeK COMPUTER INC			Title :	Schematic page name
			Engineer:	Shunmin, Frank
Size	Project Name			Rev
Cus om	A7S			1 0
Date: 星期 一 一月 19 2007			Sheet 19 of 95	

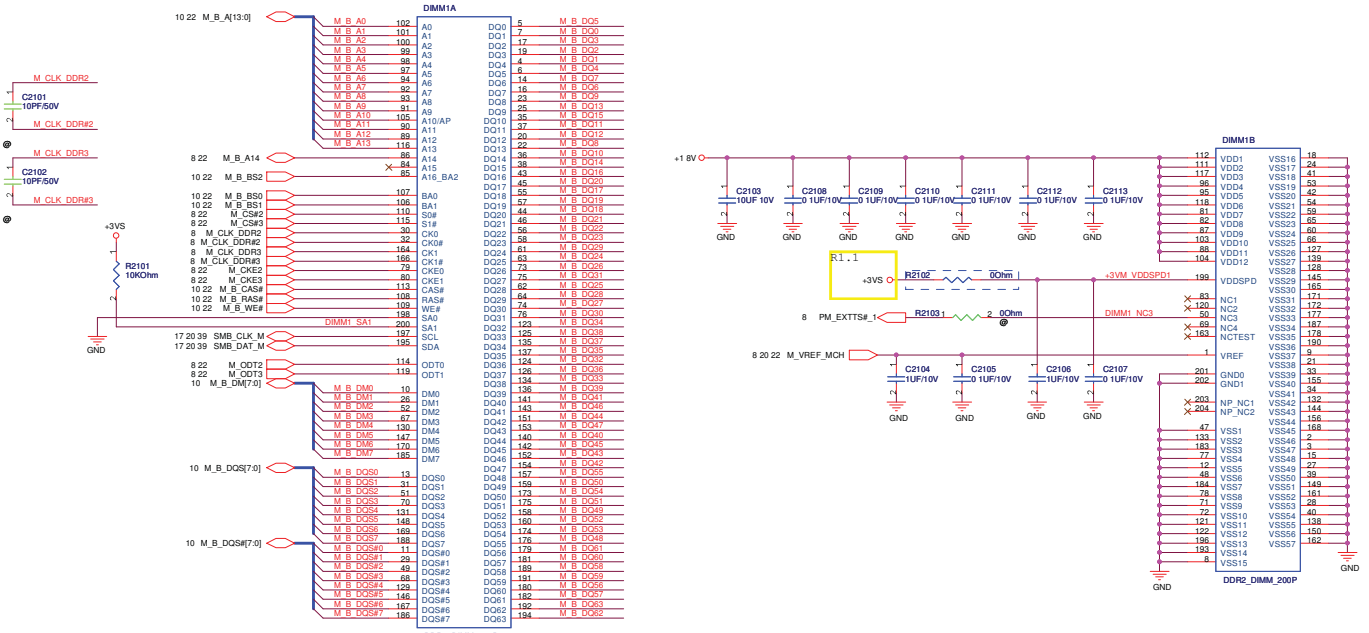


12G025122006

ASUSTeK COMPUTER INC NB1	Title : DDR2 SO-DIMM0		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 20 of 95		

M_B_DQ[63 0] 10

STD Type TOP



SN:12G02502200E

ASUSTeK COMPUTER INC NB1	Title : DDR2 SO-DIMM1		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 二月 19 2007	Sheet 21 of 95		

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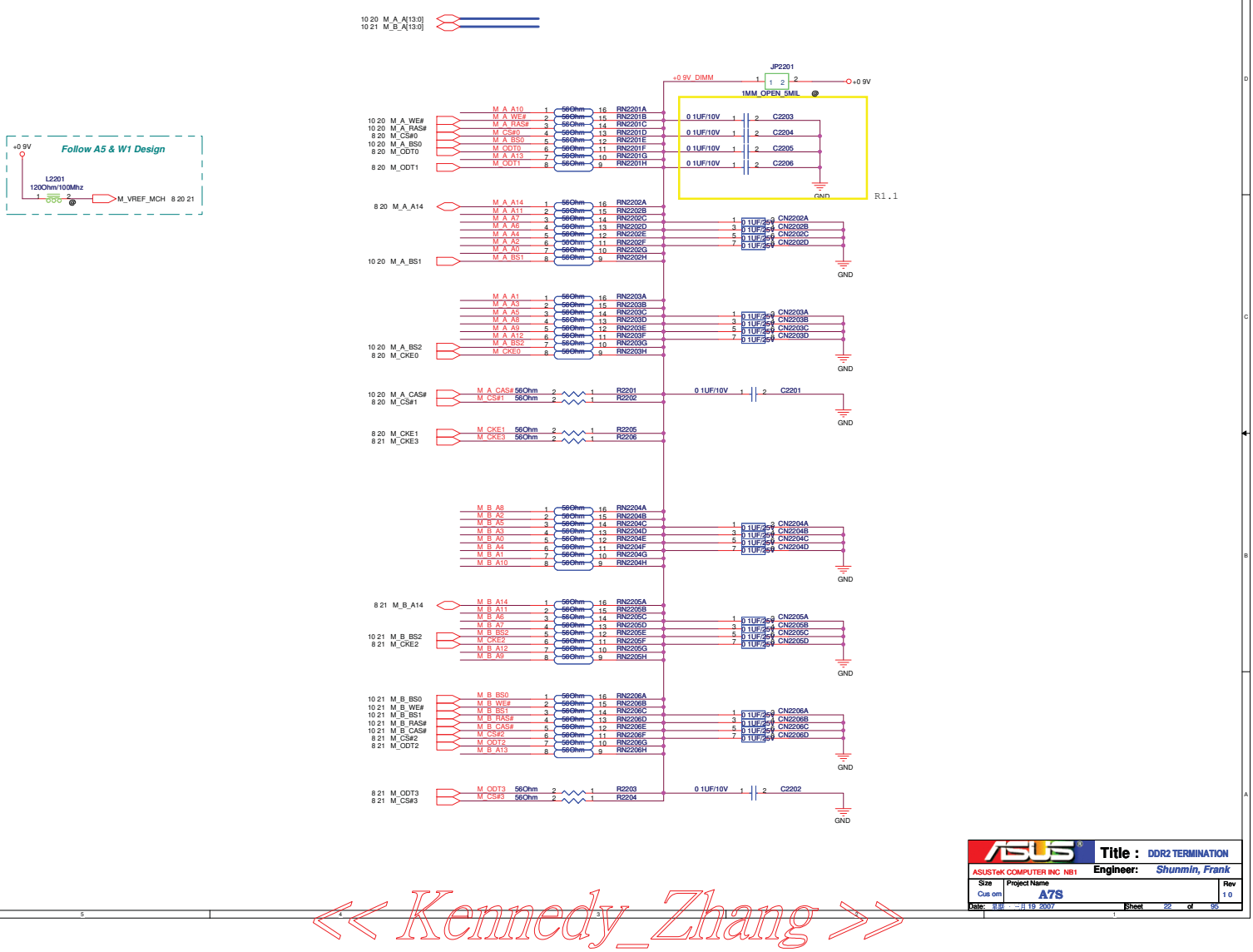


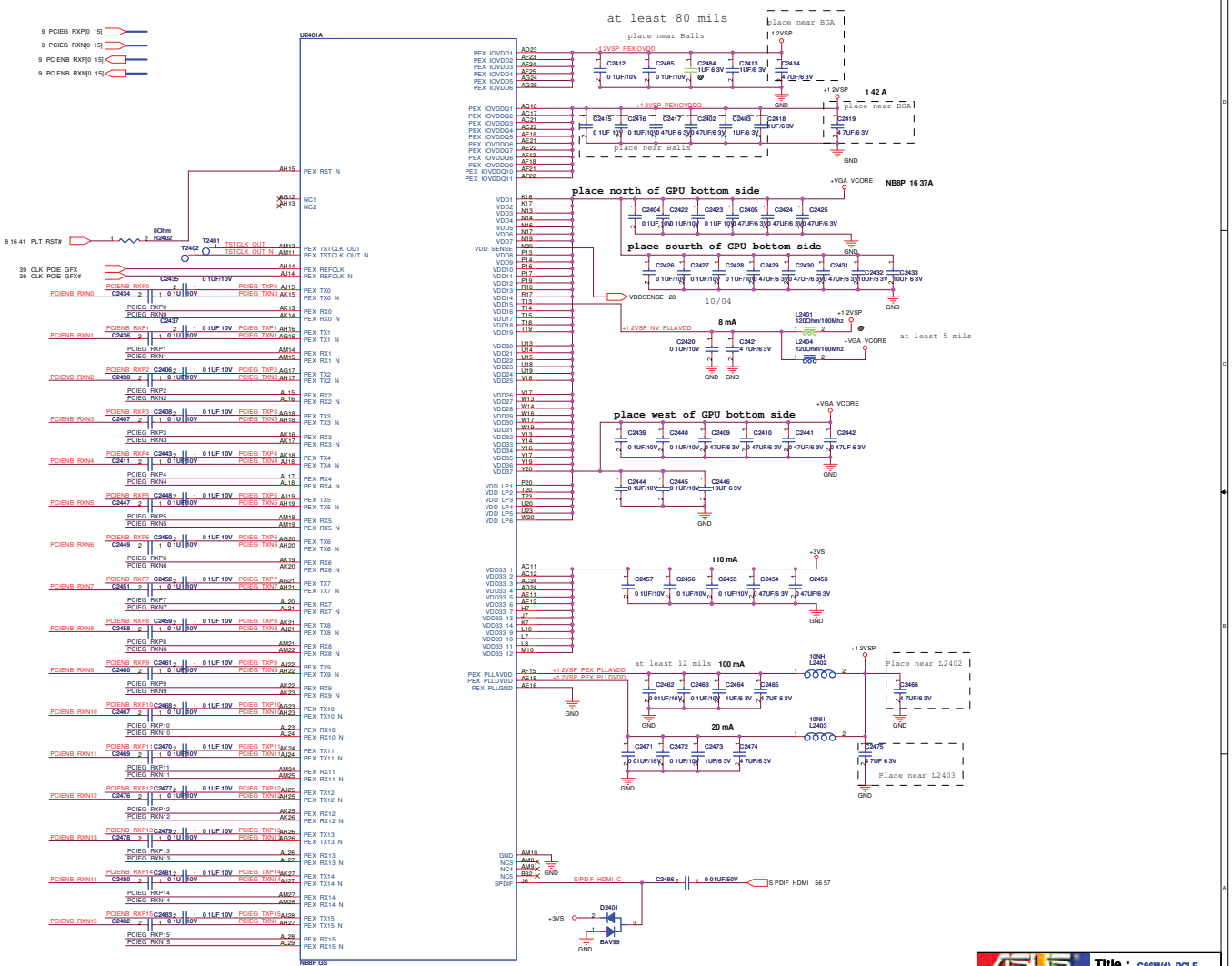
ASUSTeK COMPUTER INC

Title : Schematic page name

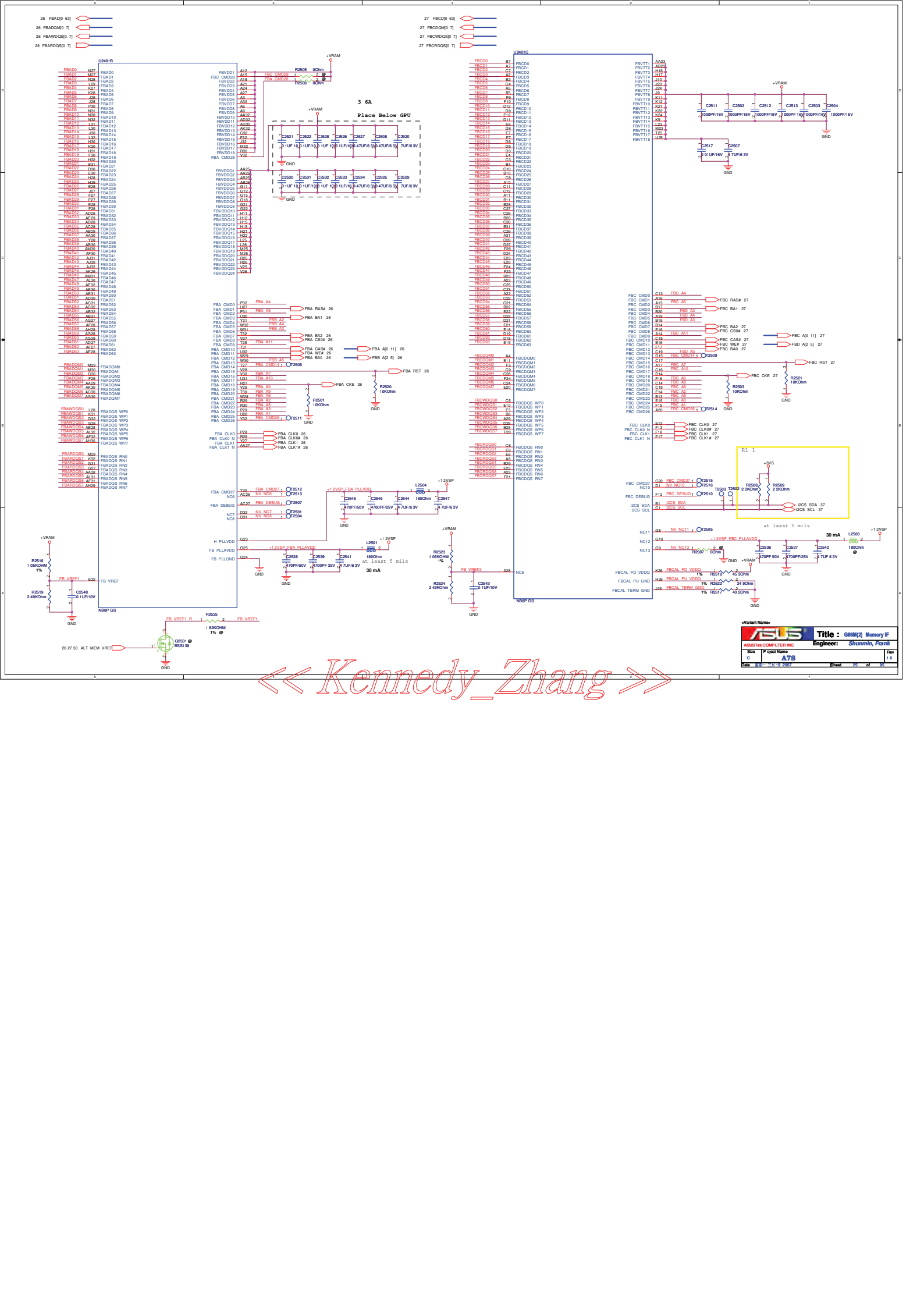
Engineer: Shunmin, Frank

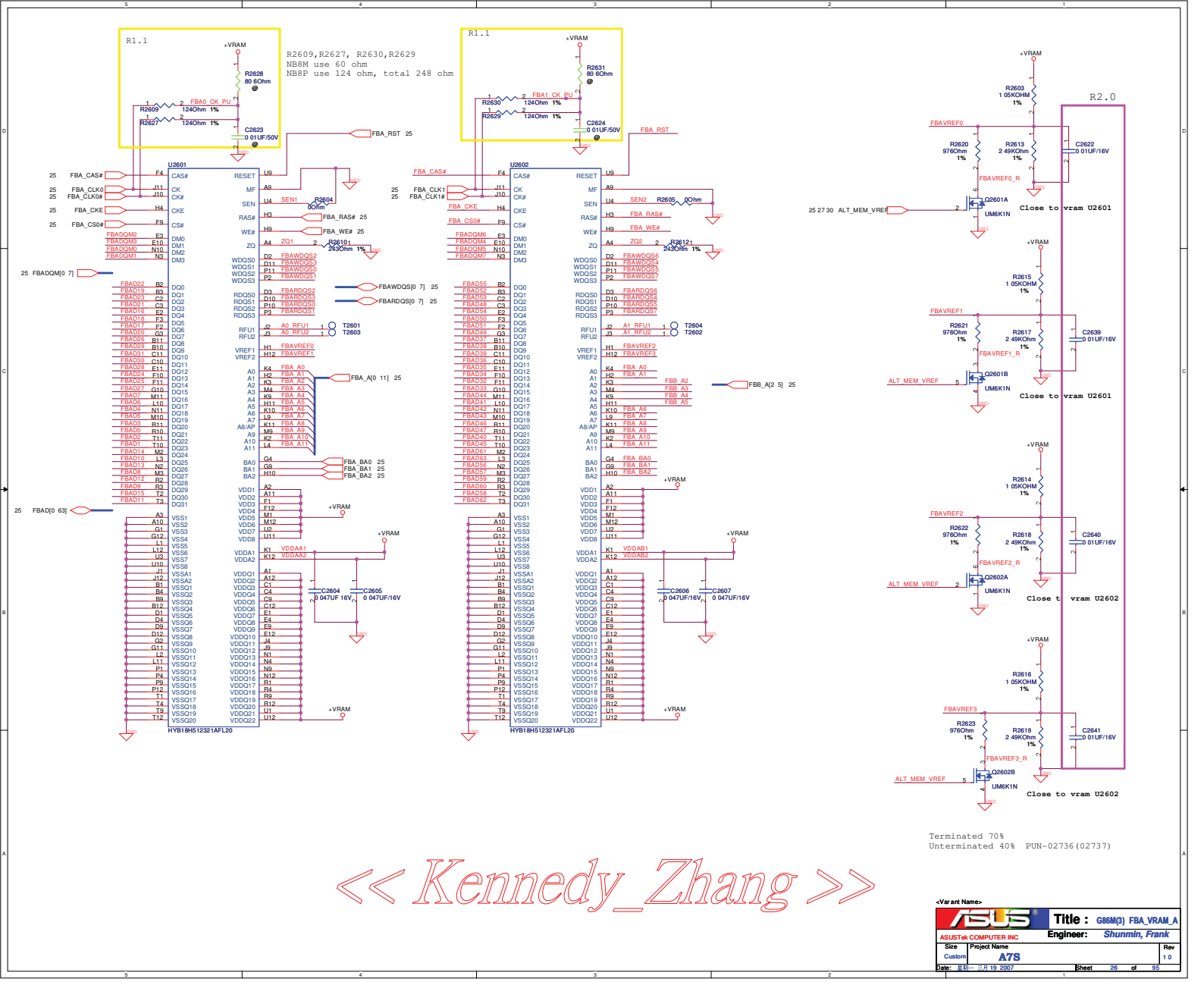
Size	Project Name	Rev
C	A7S	1.0

Date: 星期一 三月 19 2007 Sheet 23 of 95



ASUSTeK COMPUTER INC	Title : G86M(1)_PCI E		
	Engineer: Shunmin, Frank		
Size: C	Project Name: A7S		Rev: 1.0
Date: Wednesday, July 18, 2007	Sheet 24 of 55		

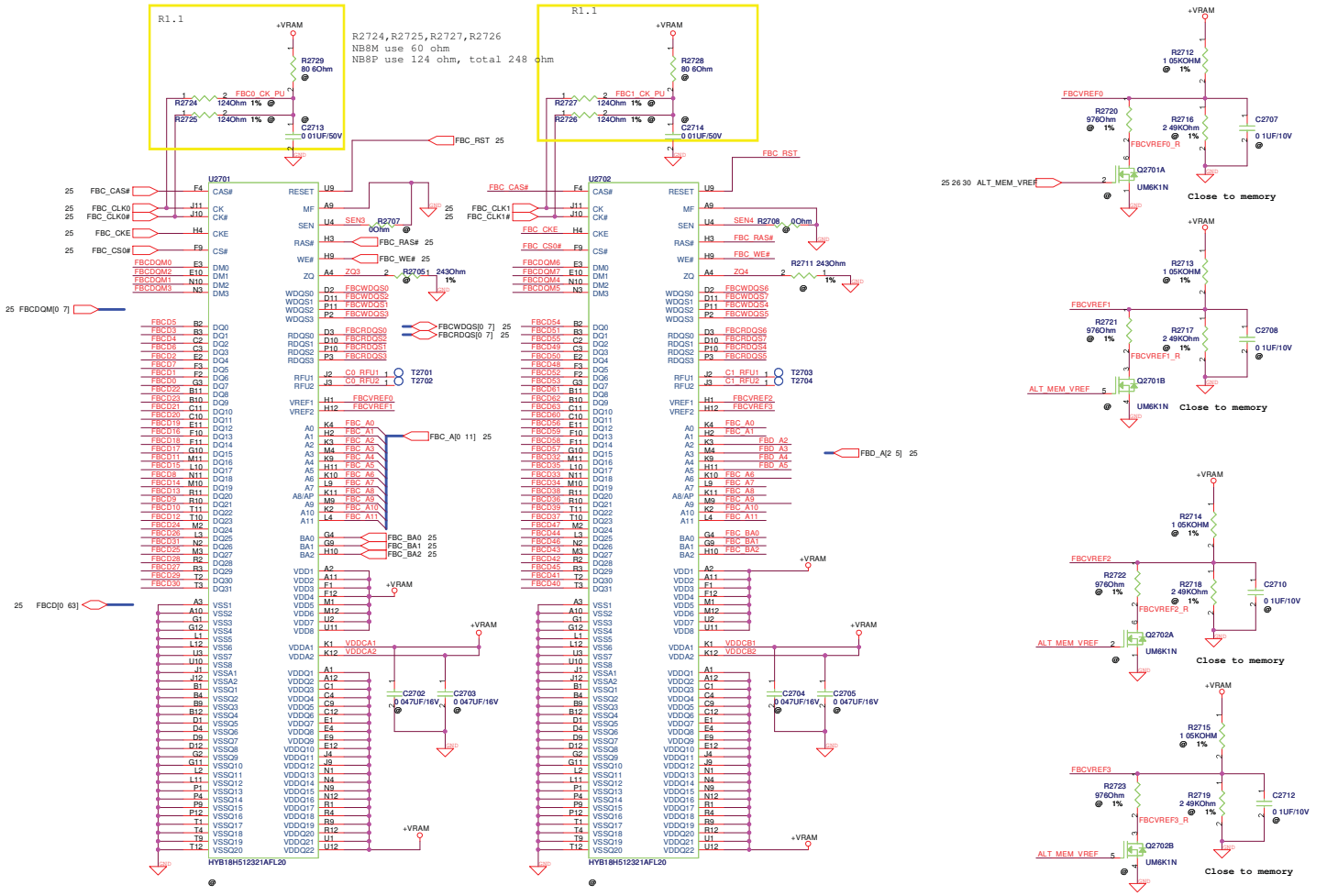




<< Kennedy_Zhang >>

<Variant Name>

ASUSTeK COMPUTER INC	Title : G86M(3) FBA_VRAM_A	
	Engineer: Shunmin, Frank	
Size: Custom	Project Name: A7S	Rev: 1 0
Date: 星期一 三月 19 2007	Sheet 26 of 95	



Terminated 70%
Unterminated 40% PUN-02736(02737)

<< Kennedy_Zhang >>

<Variant Name>

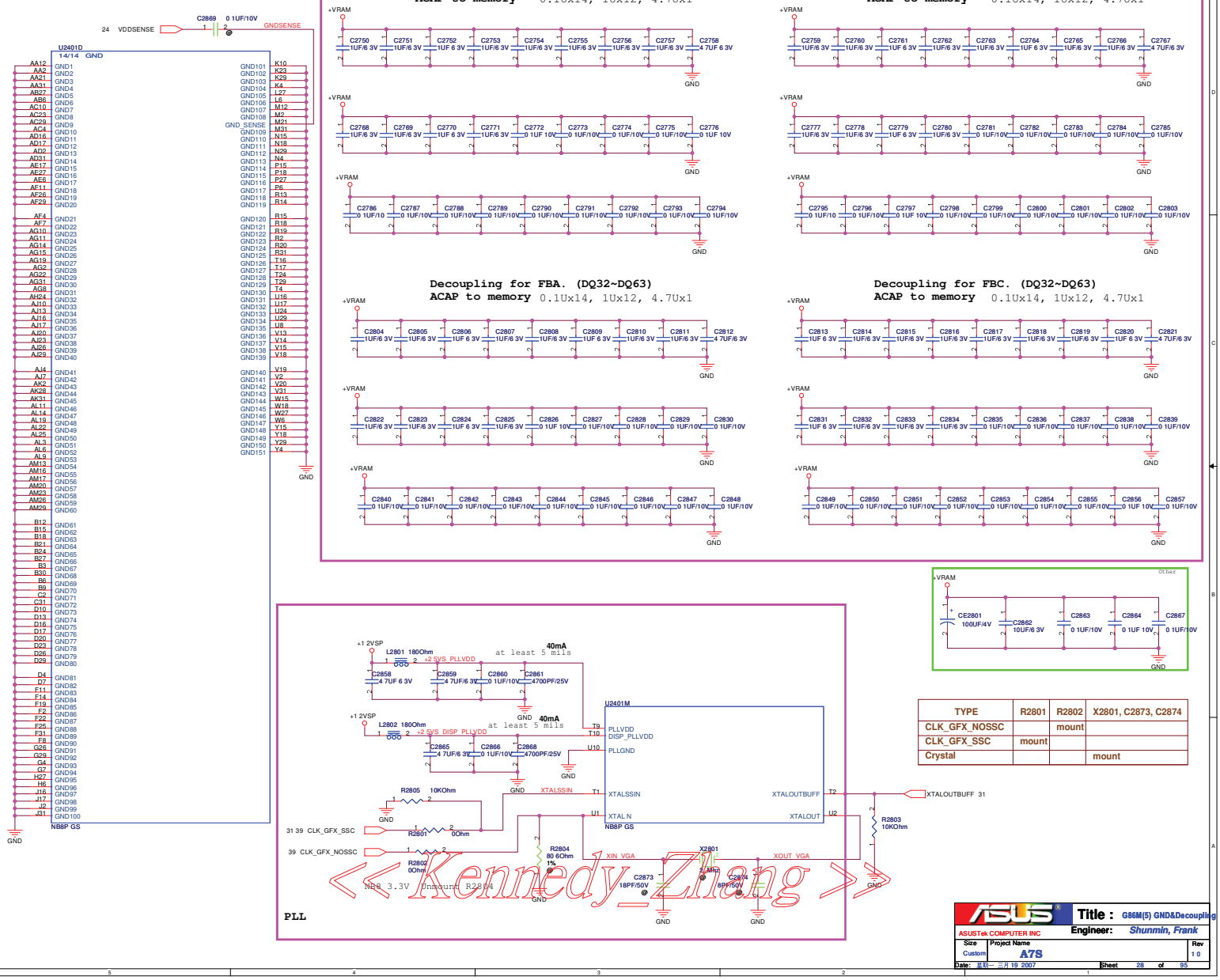
ASUSTek COMPUTER INC

Title : G86M(4) FBC_VRAM_C

Engineer: Shunmin, Frank

Size	Project Name	Rev
Custom	A7S	1 0

Date: 星期一 三月 19 2007 Sheet 27 of 95



TYPE	R2801	R2802	X2801, C2873, C2874
CLK_GFX_NOSSC		mount	
CLK_GFX_SSC	mount		
Crystal			mount

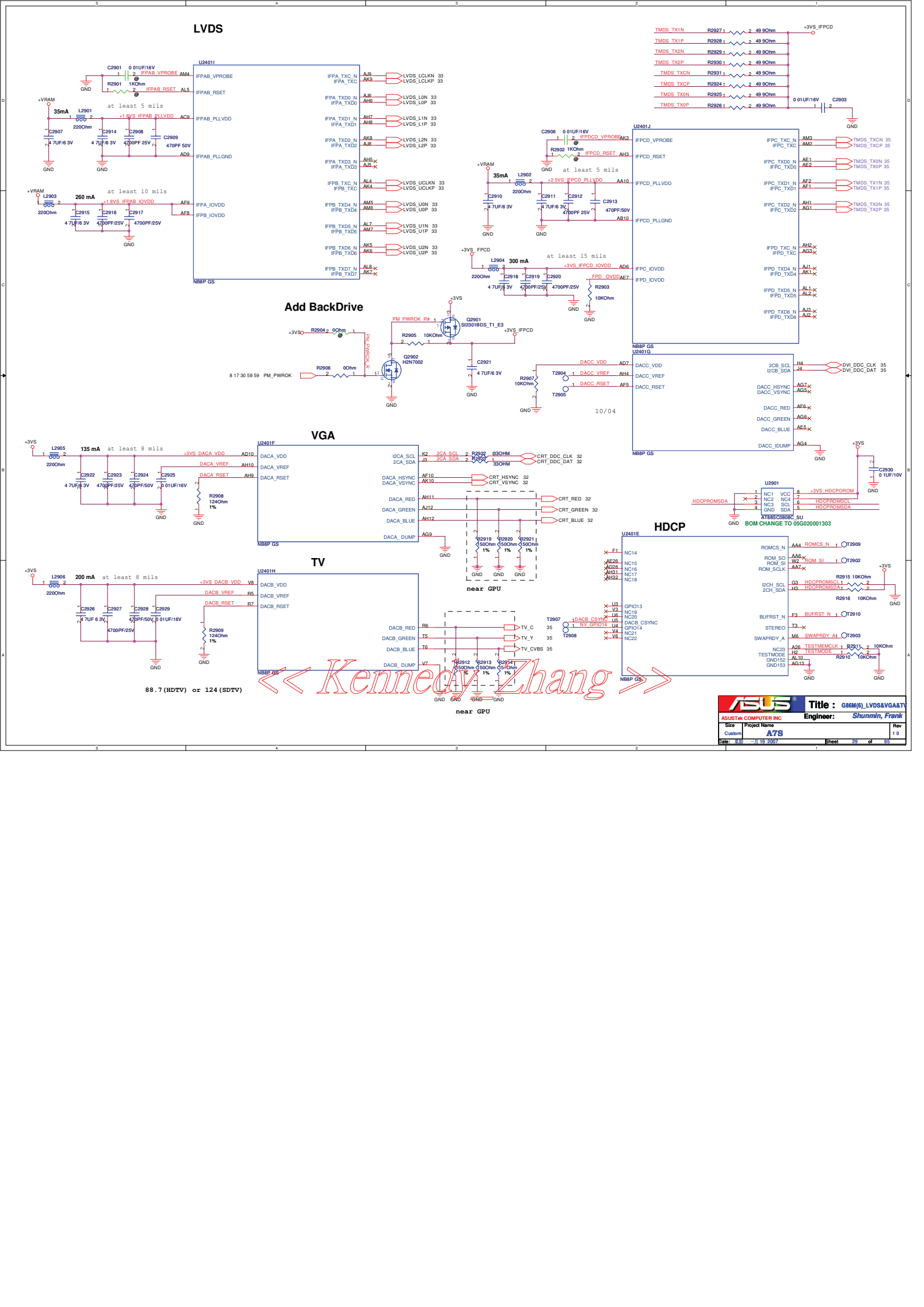
ASUSTek COMPUTER INC

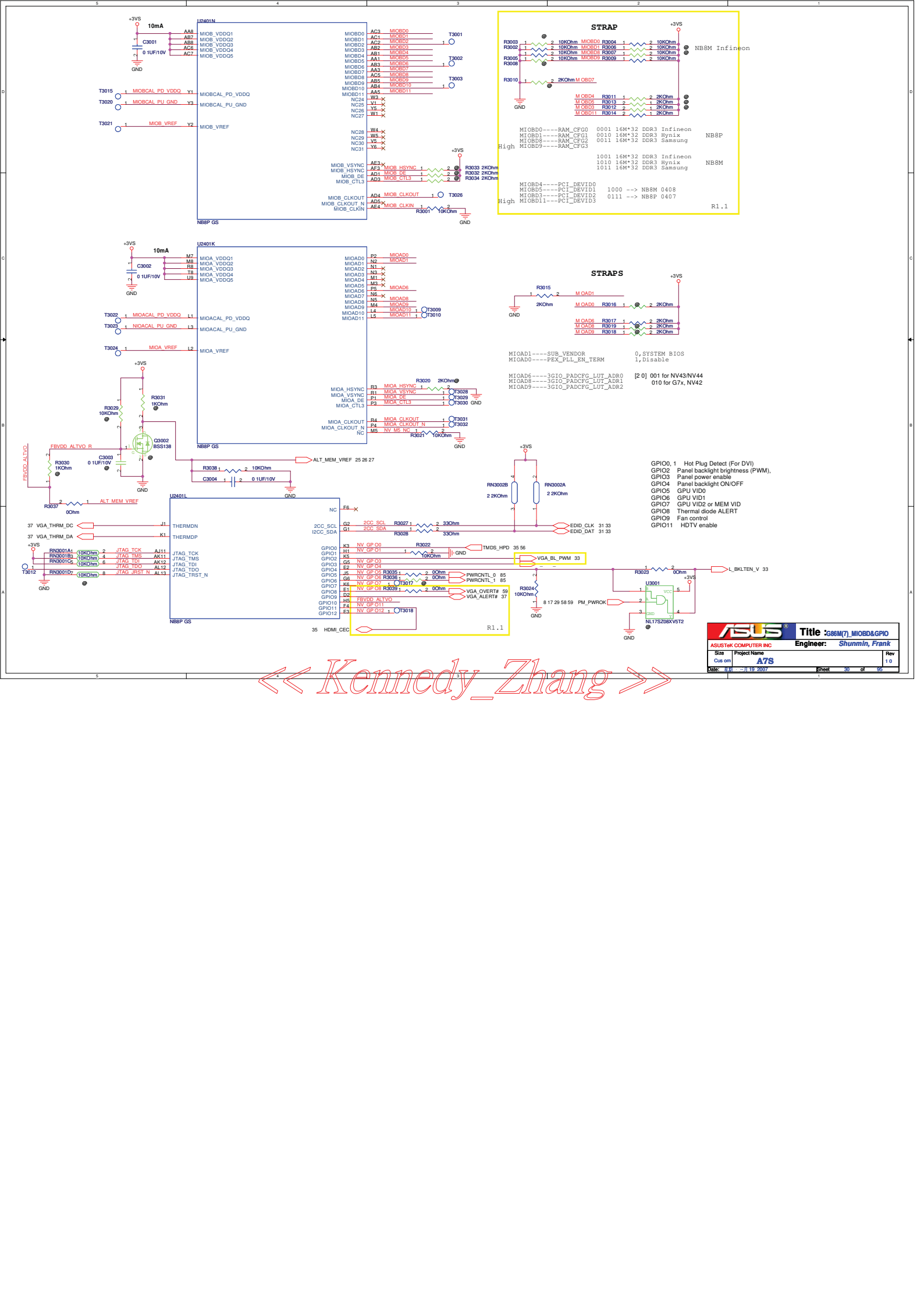
Title : G86M(5) GND&Decoupling

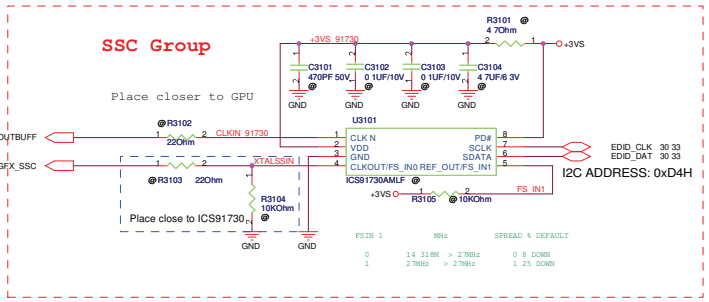
Engineer: Shunmin, Frank

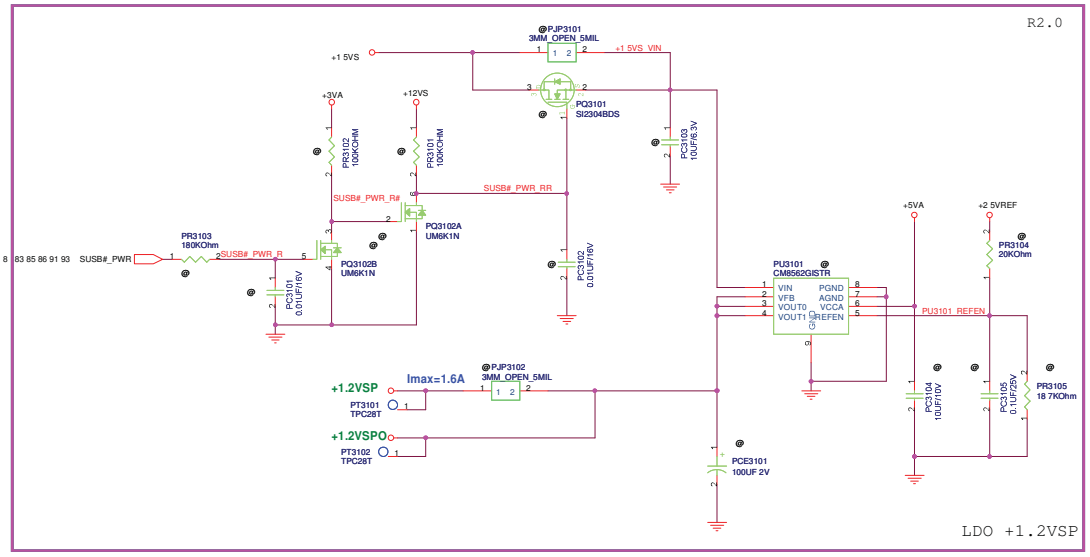
Size	Project Name	Rev
Custom	A7S	1.0

Date: 星期一 三月 19 2007 Sheet 28 of 95


LVDS
Add BackDrive
VGA
TV
HDCP
near GPU
near GPU
88.7(HDTV) or 124(SDTV)
BOM CHANGE TO 05G020001303
<< KennedyZhang >>
Title : G86M(6)_LVDS&VGA&TV
ASUSTeK COMPUTER INC
Engineer: Shunmin, Frank
Project Name A7S
Size Custom
Rev 1.0
Sheet 29 of 95


STRAP
NB8M Infineon
MIOBD0-----RAM_CFG0 0001 16M*32 DDR3 Infineon
MIOBD1-----RAM_CFG1 0010 16M*32 DDR3 Hynix NB8P
MIOBD8-----RAM_CFG2 0011 16M*32 DDR3 Samsung
High MIOBD9-----RAM_CFG3
1001 16M*32 DDR3 Infineon
1010 16M*32 DDR3 Hynix NB8M
1011 16M*32 DDR3 Samsung
MIOBD4-----PCI_DEVID0
MIOBD5-----PCI_DEVID1 1000 --> NB8M 0408
MIOBD3-----PCI_DEVID2 0111 --> NB8P 0407
High MIOBD11----PCI_DEVID3
R1.1
STRAPS
MIOAD1----SUB_VENDOR 0,SYSTEM BIOS
MIOAD0-----PEX_PLL_EN_TERM 1,Disable
MIOAD6-----3GIO_PADCFG_LUT_ADR0 [2 0] 001 for NV43/NV44
MIOAD8-----3GIO_PADCFG_LUT_ADR1 010 for G7x, NV42
MIOAD9-----3GIO_PADCFG_LUT_ADR2
GPIO0, 1 Hot Plug Detect (For DVI)
GPIO2 Panel backlight brightness (PWM),
GPIO3 Panel power enable
GPIO4 Panel backlight ON/OFF
GPIO5 GPU VID0
GPIO6 GPU VID1
GPIO7 GPU VID2 or MEM VID
GPIO8 Thermal diode ALERT
GPIO9 Fan control
GPIO11 HDTV enable
Title :G86M(7)_MIOBD&GPIO
ASUSTeK COMPUTER INC
Engineer: Shunmin, Frank
Size Project Name Rev
Cus om A7S 1 0
Date: 星期 一月 19 2007 Sheet 30 of 95
<< Kennedy_Zhang >>

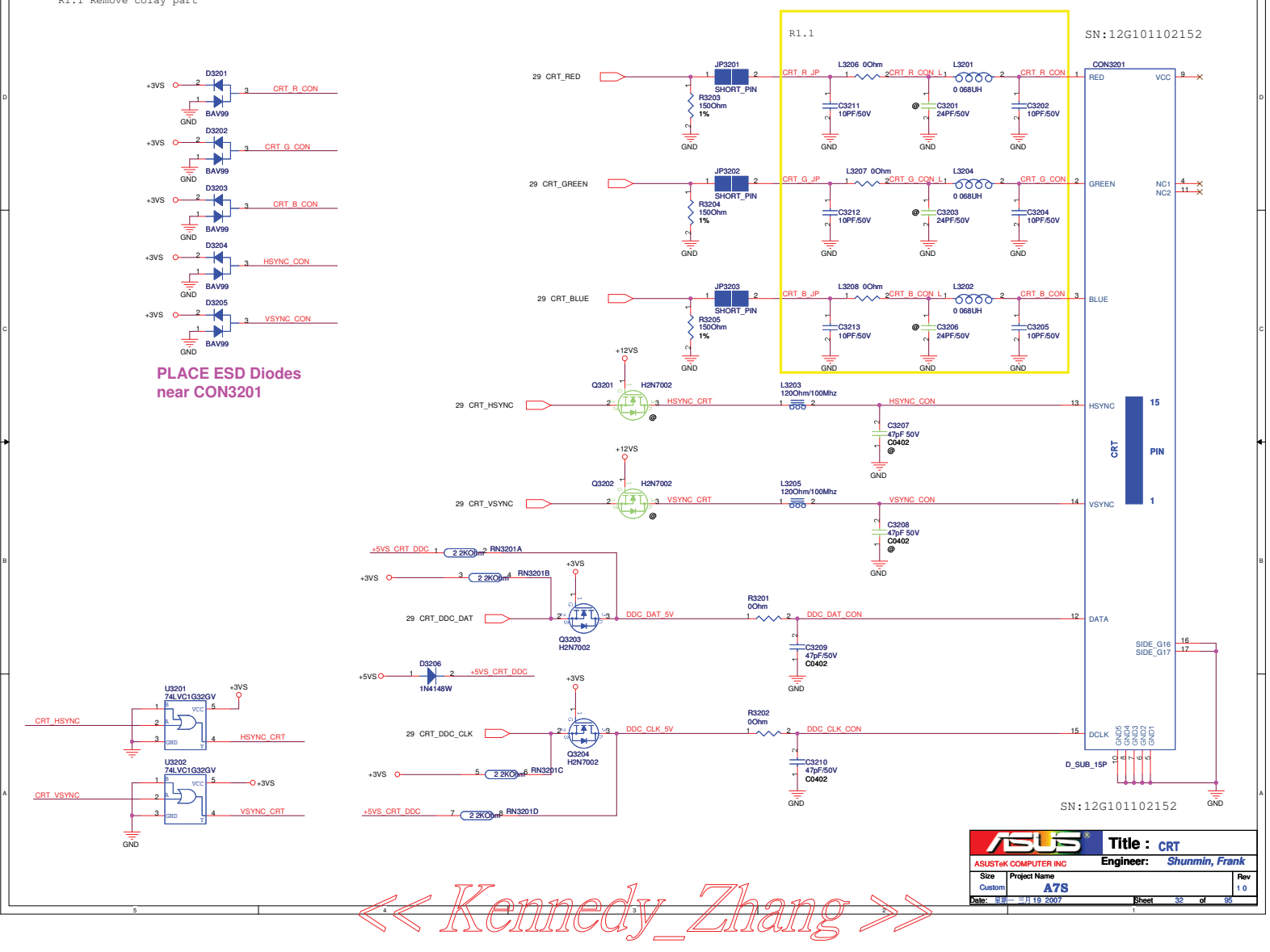




ASUSTeK COMPUTER INC	Title : G86M(8)-SSC		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 31 of 95		

<< Kennedy_Zhang >>

R1.1 Remove colay part



ASUSTeK COMPUTER INC

Title : CRT

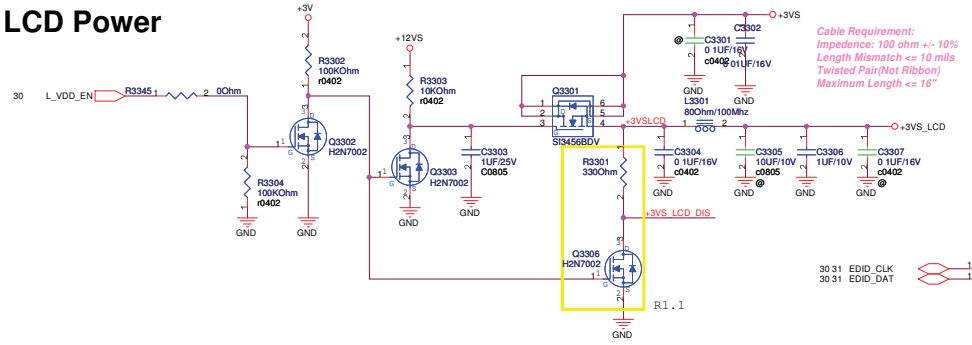
Engineer: Shunmin, Frank

Size	Project Name	Rev
Custom	A7S	1.0

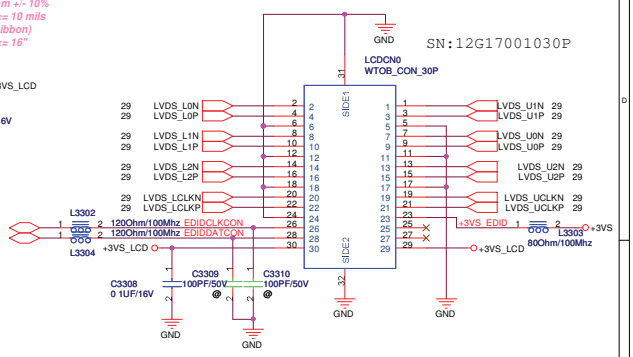
Date: 星期一 三月 19 2007 Sheet 32 of 95

<< Kennedy_Zhang >>

LCD Power



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

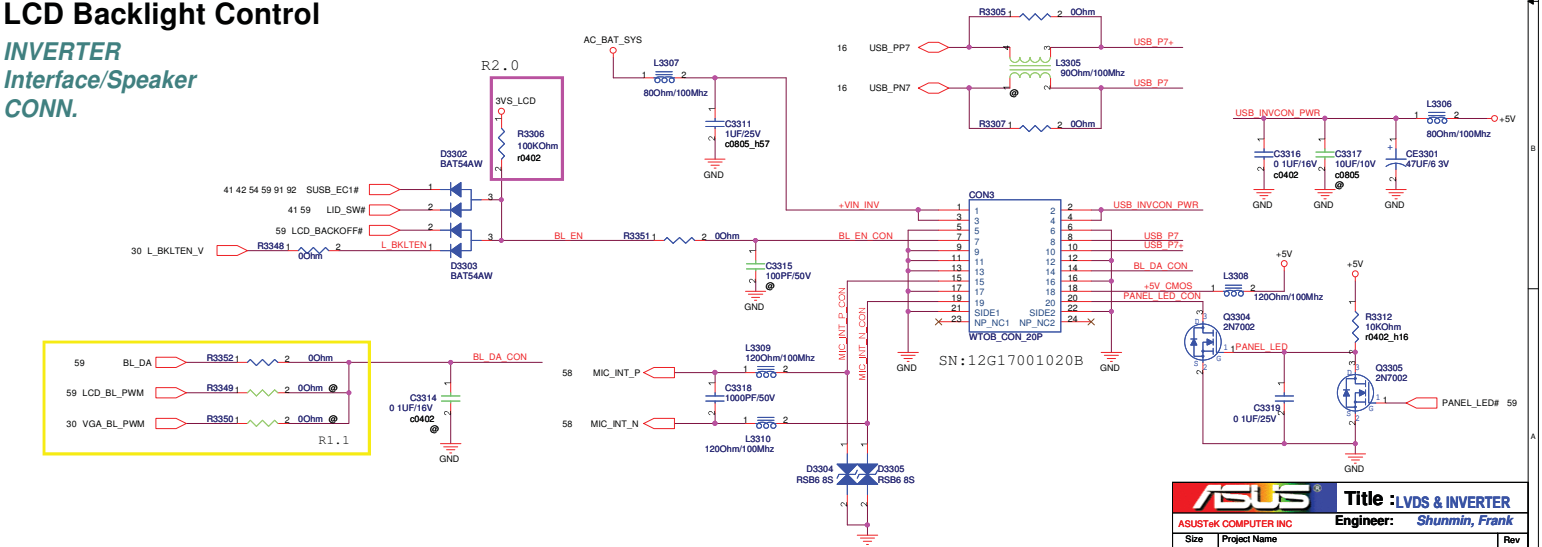


LCD LVDS Interface

R1.1 Remove colay part

LCD Backlight Control

INVERTER Interface/Speaker CONN.



ASUSTeK COMPUTER INC

Title : LVDS & INVERTER

Engineer: Shunmin, Frank

Size	Project Name	Rev
Custom	A7S	1.0

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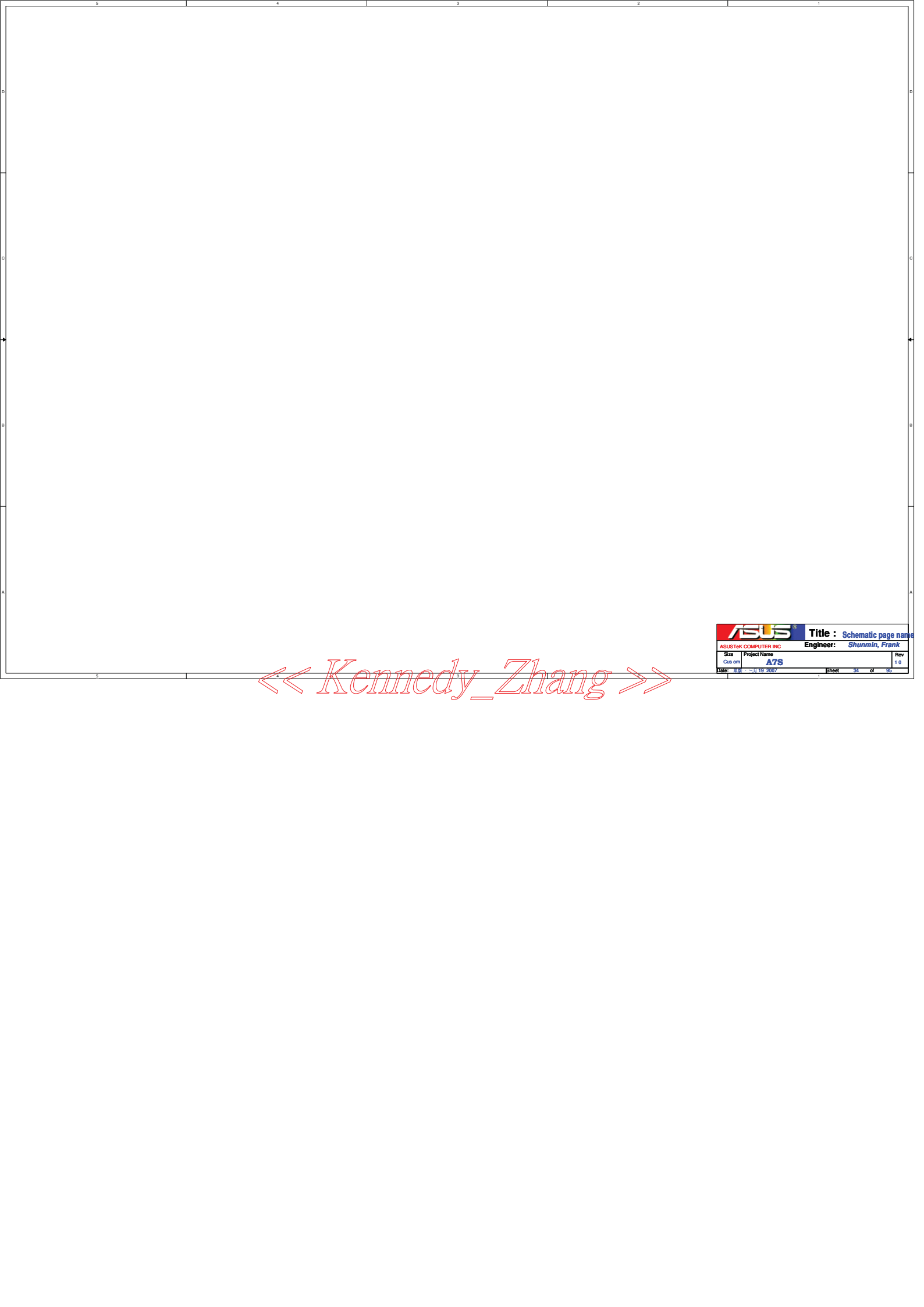
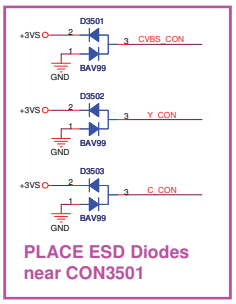
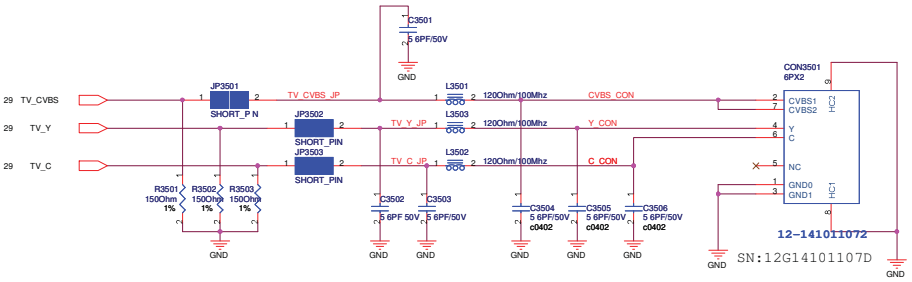
<< Kennedy_Zhang >>



TV OUT

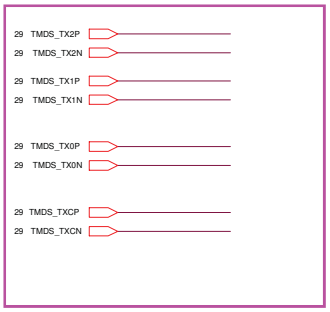
R1.1 Remove colay part

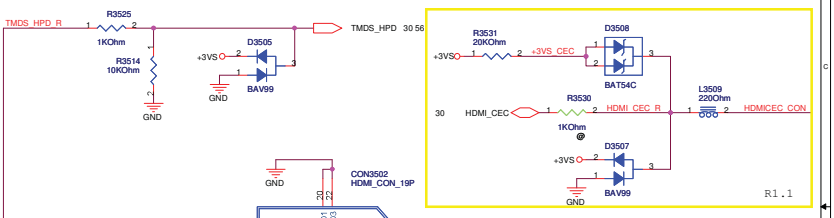


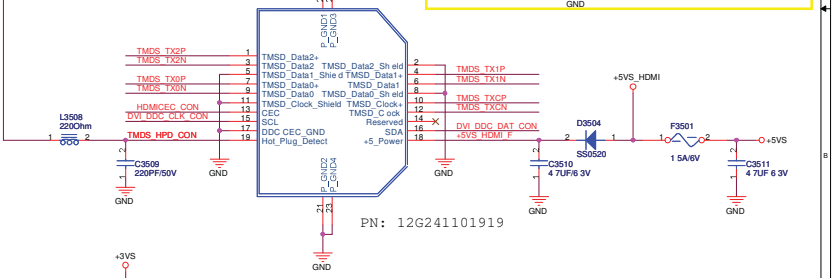


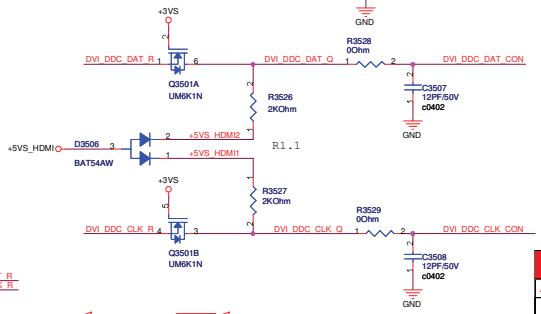
HDMI

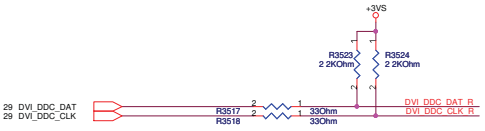
R2.0

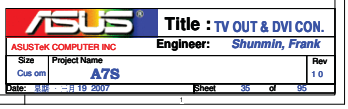












ASUSTeK COMPUTER INC

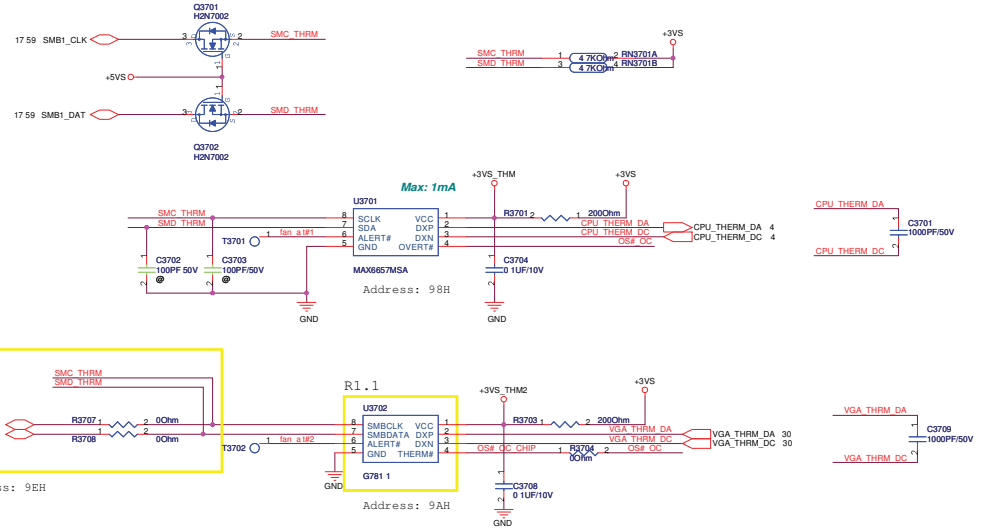
Title : Schematic page name

Engineer: Shunmin, Frank

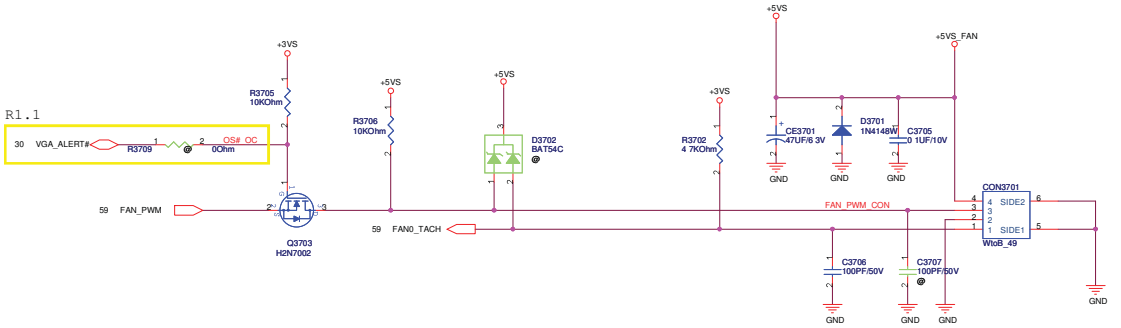
Size	Project Name	Rev
Cus om	A7S	1 0

Date: 星期 一 一月 19 2007 Sheet 38 of 95

Thermal Sensor



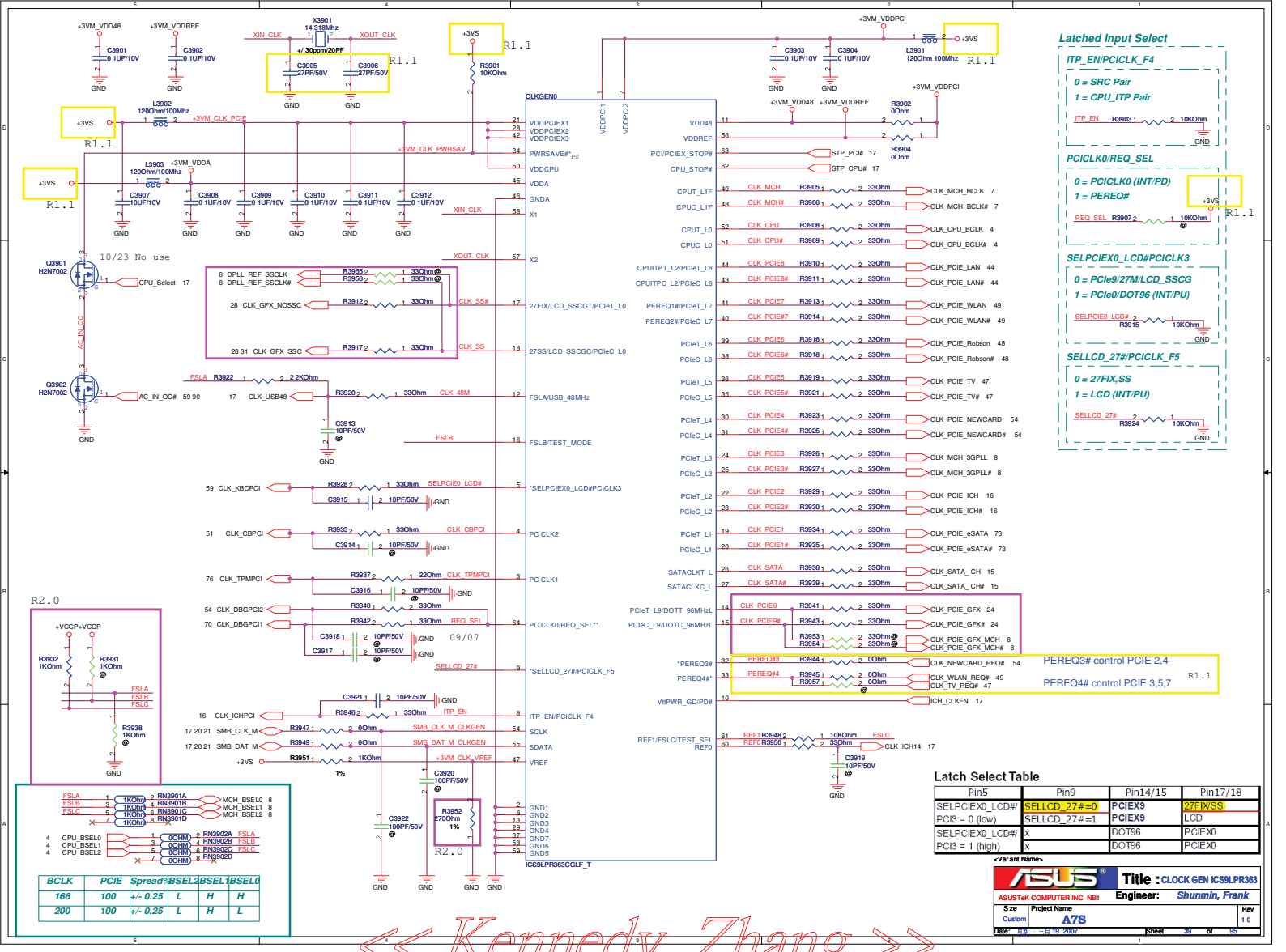
DC FAN Control



ASUSTeK COMPUTER INC NB1	Title : THER SENSOR & FAN	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1.0
Date: 星期 一, 十月 19, 2007	Sheet 37 of 95	

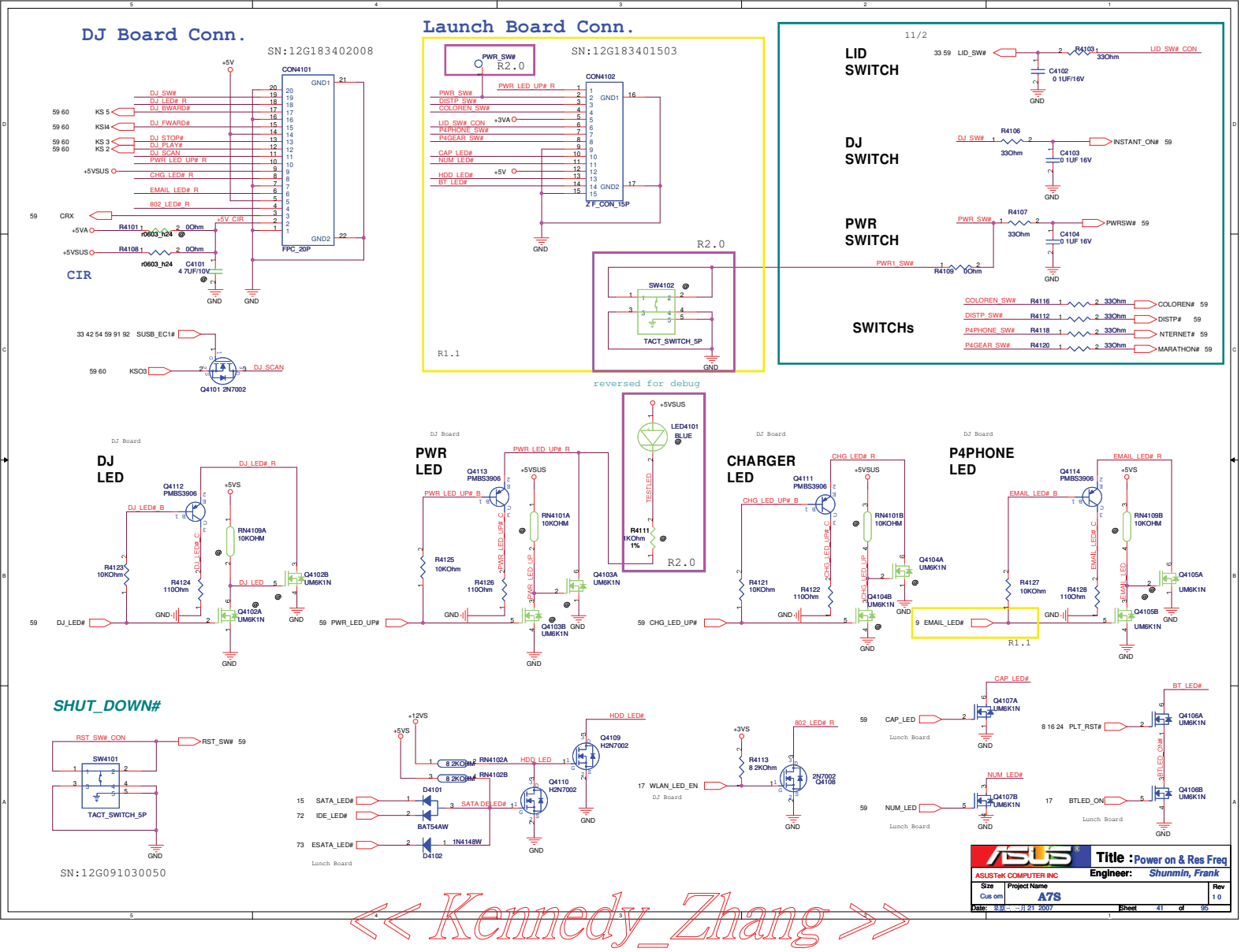
<< Kennedy_Zhang >>

ASUSTeK COMPUTER INC	Title :	Schematic page name	
	Engineer:	Shunmin, Frank	
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 38 of 95		

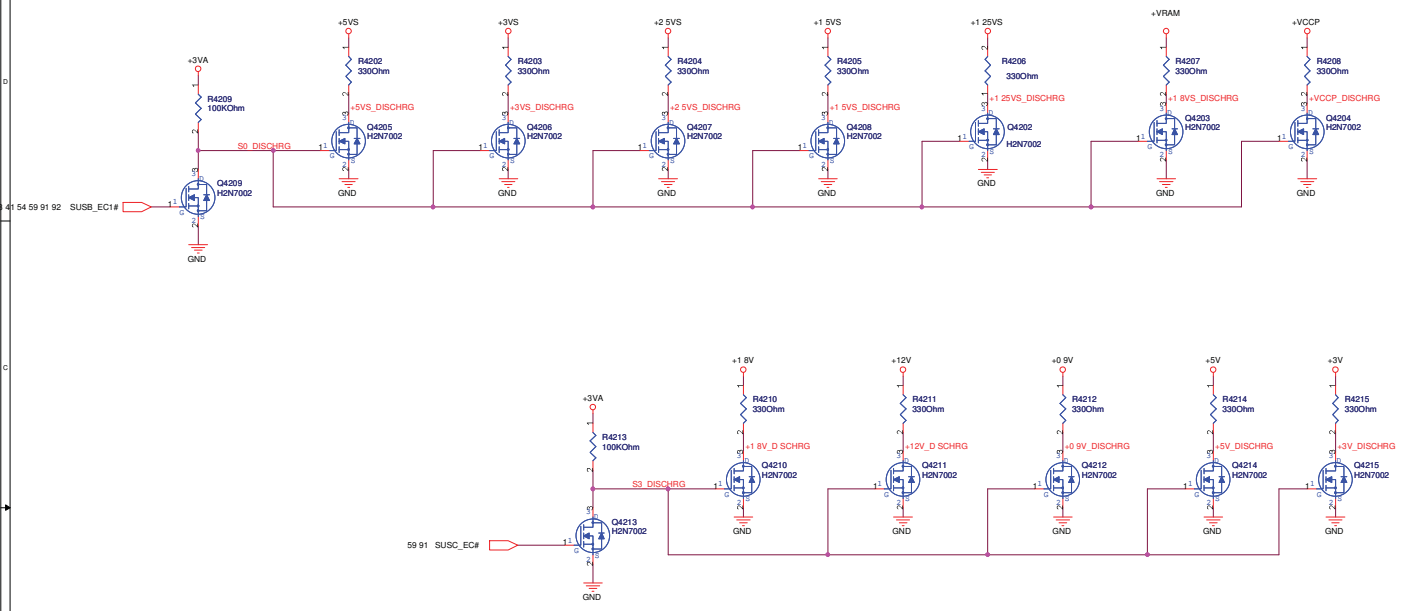


R1.1 Del LED

ASUSTeK COMPUTER INC	Title :	Schematic page name	
	Engineer:	Shunmin, Frank	
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 40 of 95		



<< Kennedy_Zhang >>

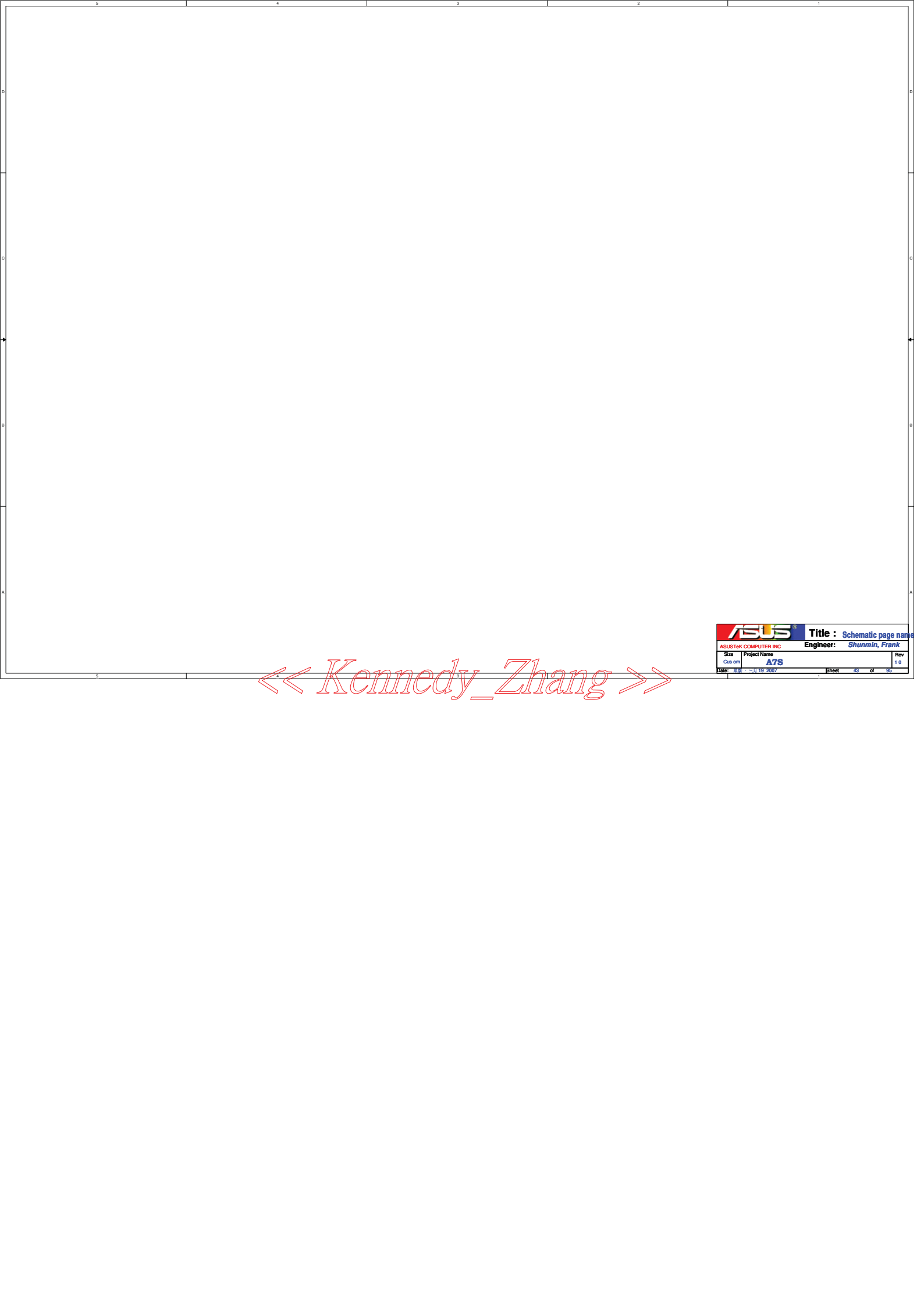


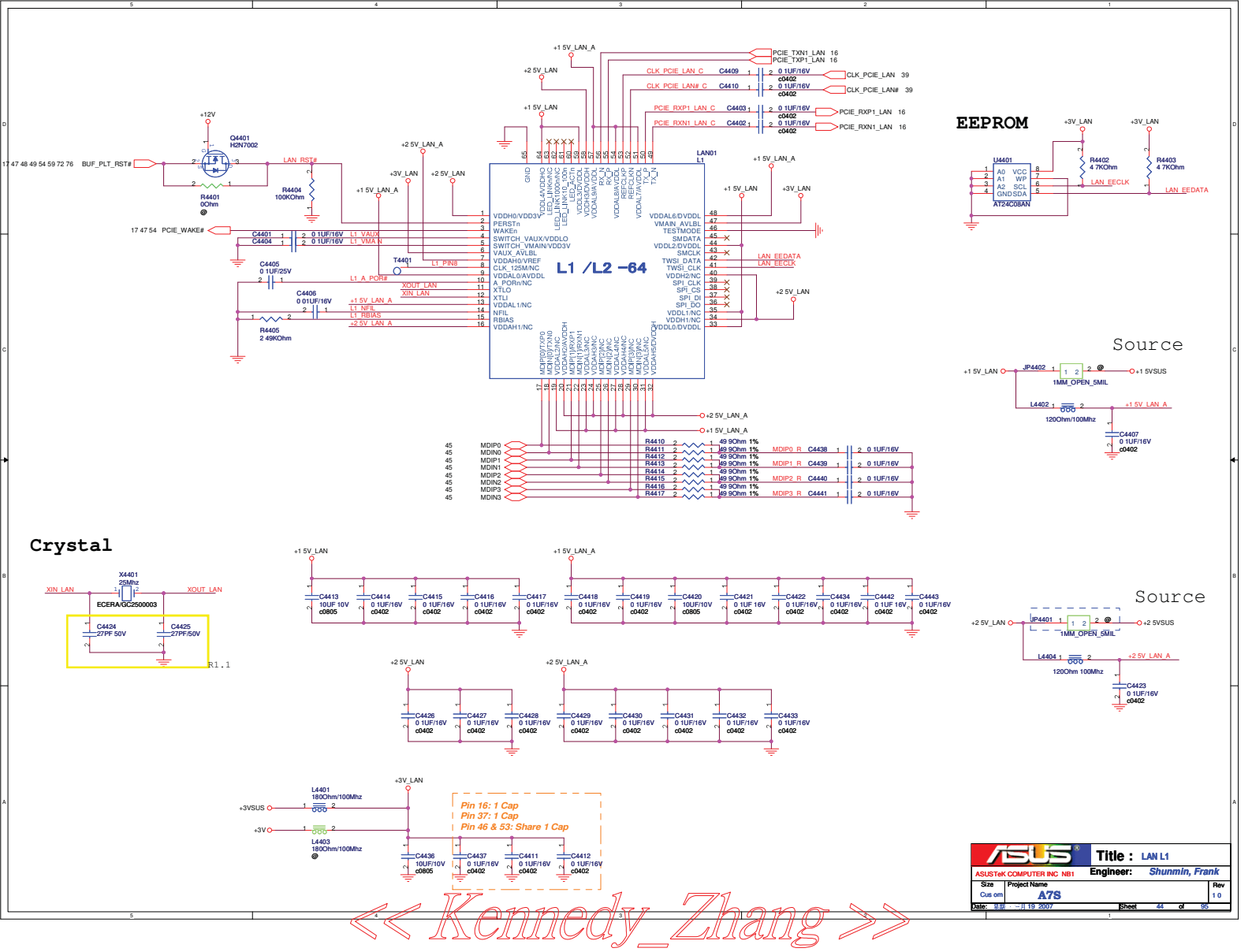
Remove VM discharge

R1.1

ASUSTeK COMPUTER INC NB1	Title : DISCHARGE & EMI CAP	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 月 19 2007	Sheet 42 of 95	

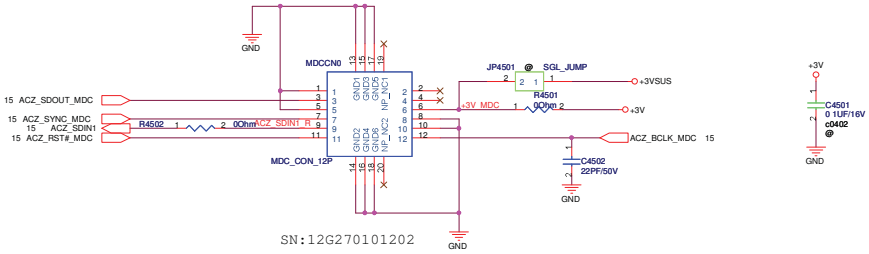
<< Kennedy_Zhang >>





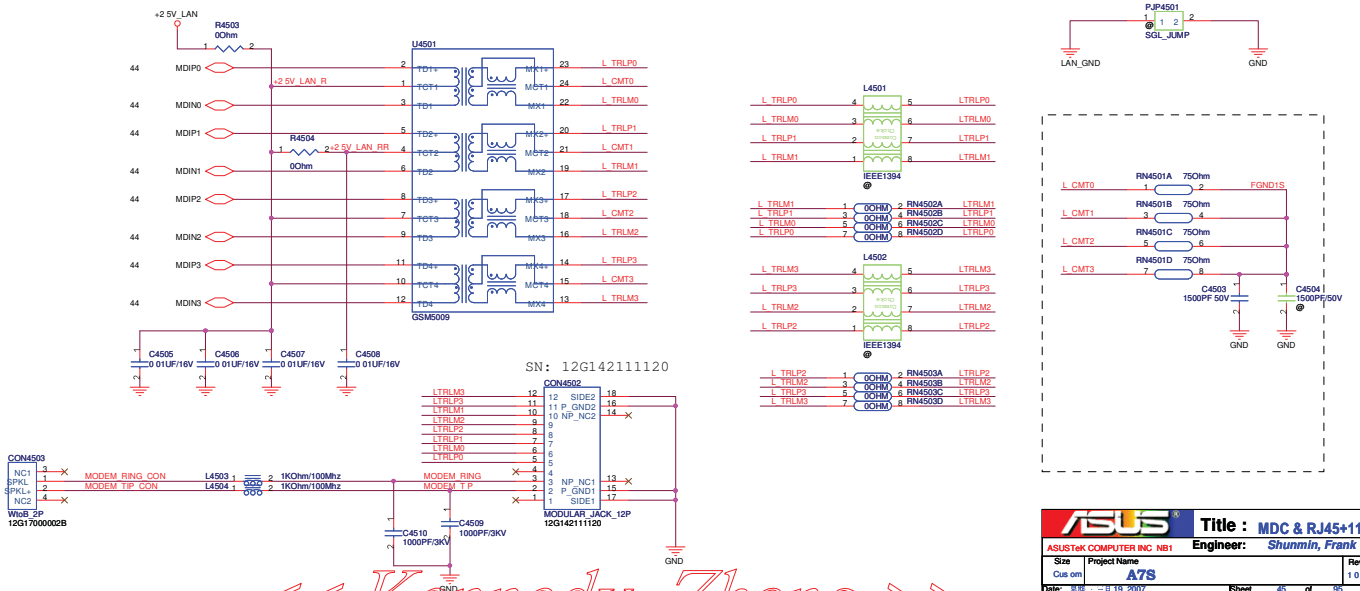
Change to
13GN7510M270

MDC CONN.



EMI need
short 03/01

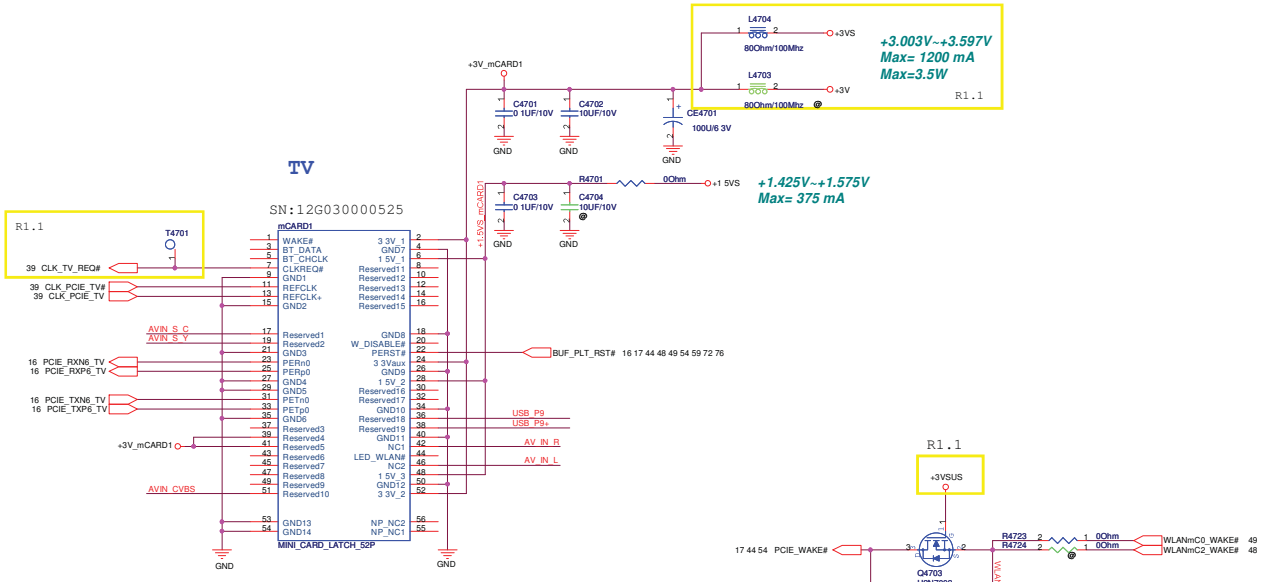
LAN CONN.



SN: 12G142111120

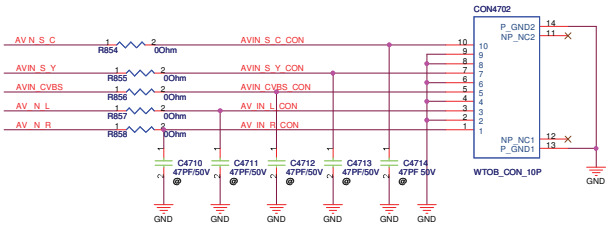
ASUSTeK COMPUTER INC NB1	Title : MDC & RJ45+11	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1.0
Date: 星期 一月 19 2007	Sheet 45 of 95	

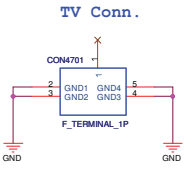
ASUSTeK COMPUTER INC			Title :	Schematic page name
			Engineer:	Shunmin, Frank
Size	Project Name			Rev
Cus om	A7S			1 0
Date: 星期 一 一月 19 2007			Sheet 46 of 95	



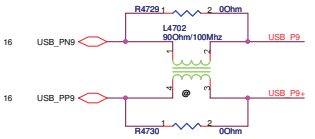
Put it the middle the board

BOM ---> 12G171030104

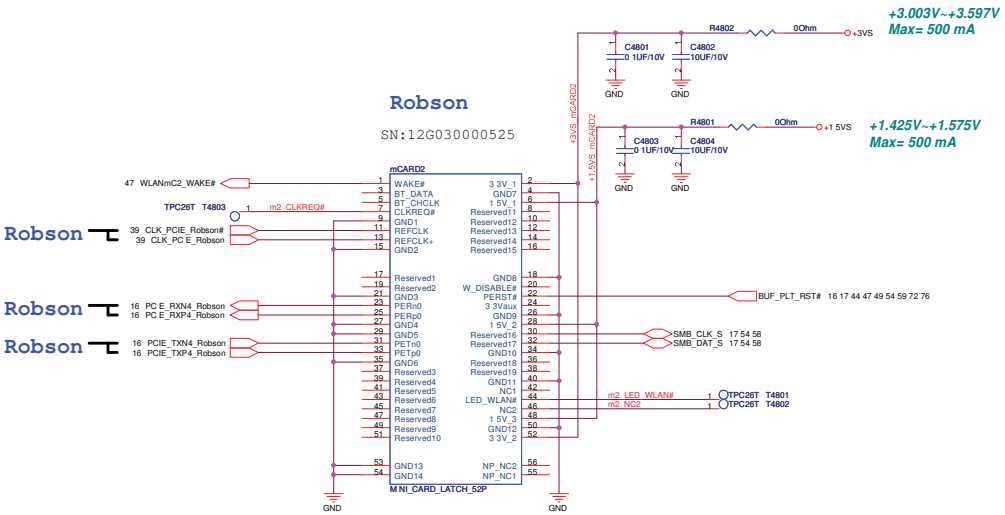




SN:14G152075001 NO part



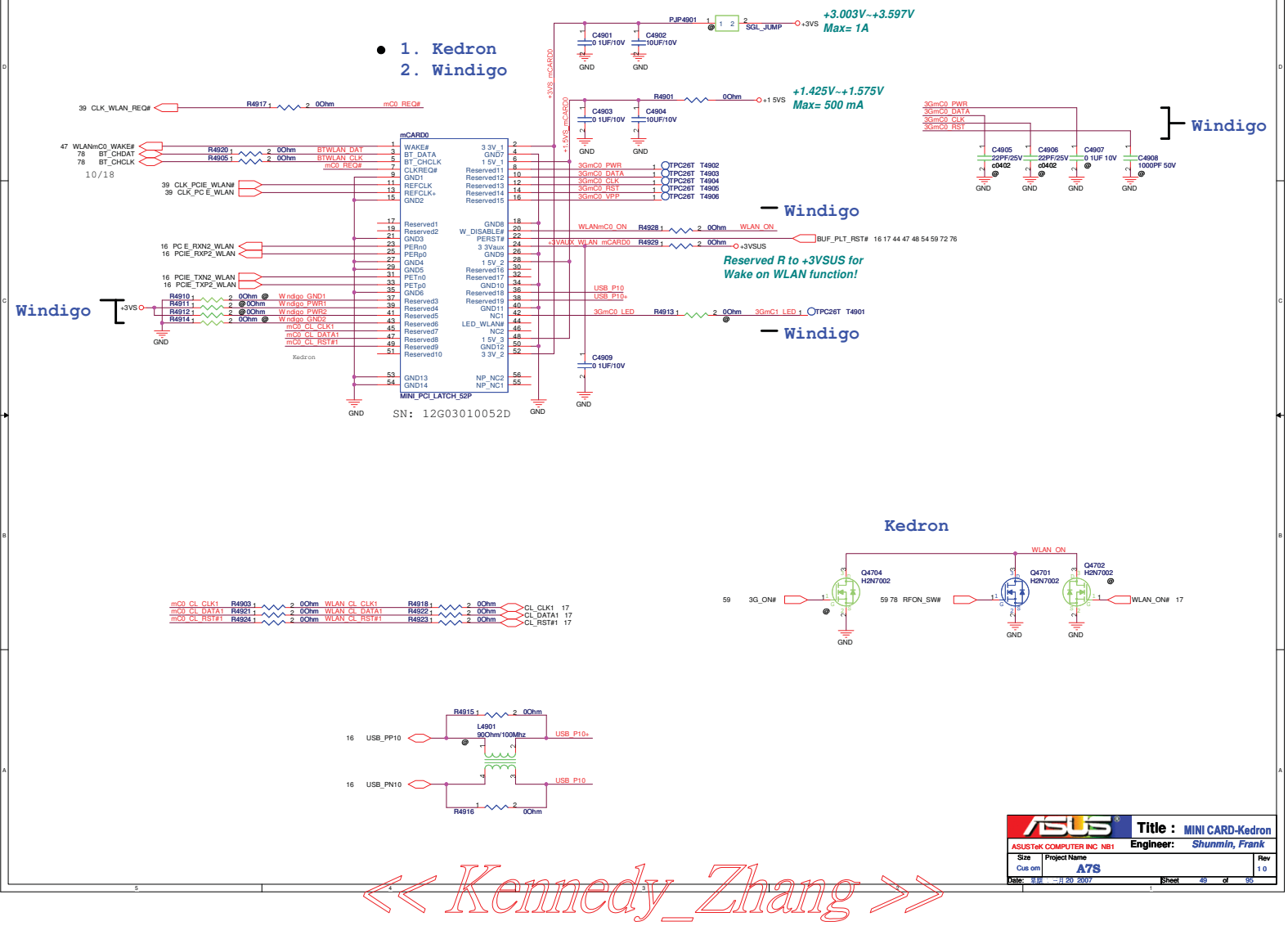
<< Kennedy_Zhang >>



Put it down on the board

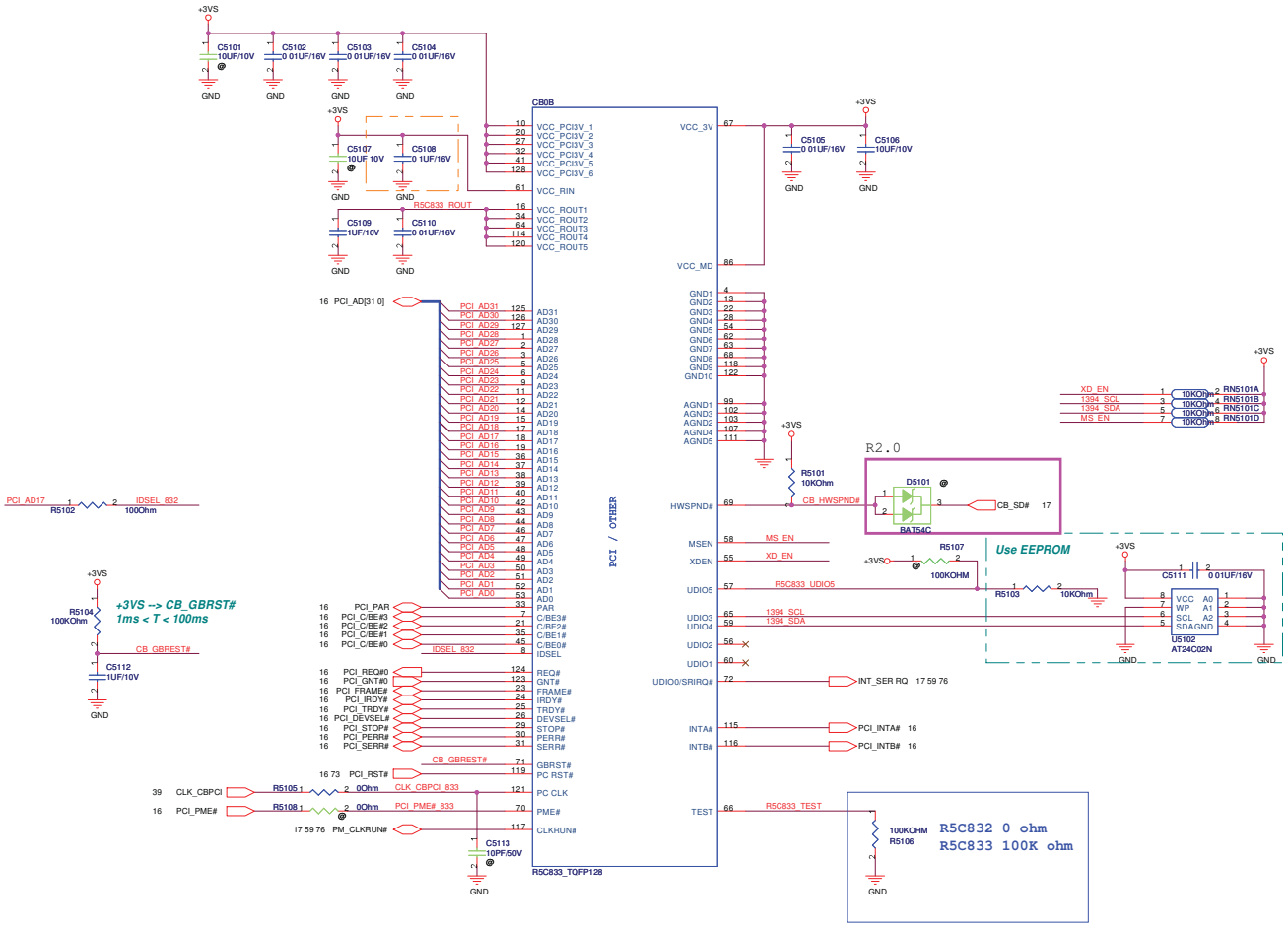
ASUSTeK COMPUTER INC NB1	Title : MINI CARD-Robson		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 二 一月 20 2007	Sheet 48 of 95		

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC NB1	Title : MINI CARD-Kedron		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 二 月 20 2007	Sheet 49 of 95		

ASUSTeK COMPUTER INC			Title :	Schematic page name
			Engineer:	Shunmin, Frank
Size	Project Name			Rev
Cus om	A7S			1 0
Date: 星期 一 一月 19 2007			Sheet 50 of 95	



ASUSTeK COMPUTER INC NB1

Title : CARD1394-R5C833(1)

Engineer: Shunmin, Frank

Size	Project Name	Rev
Cus om	A7S	1 0

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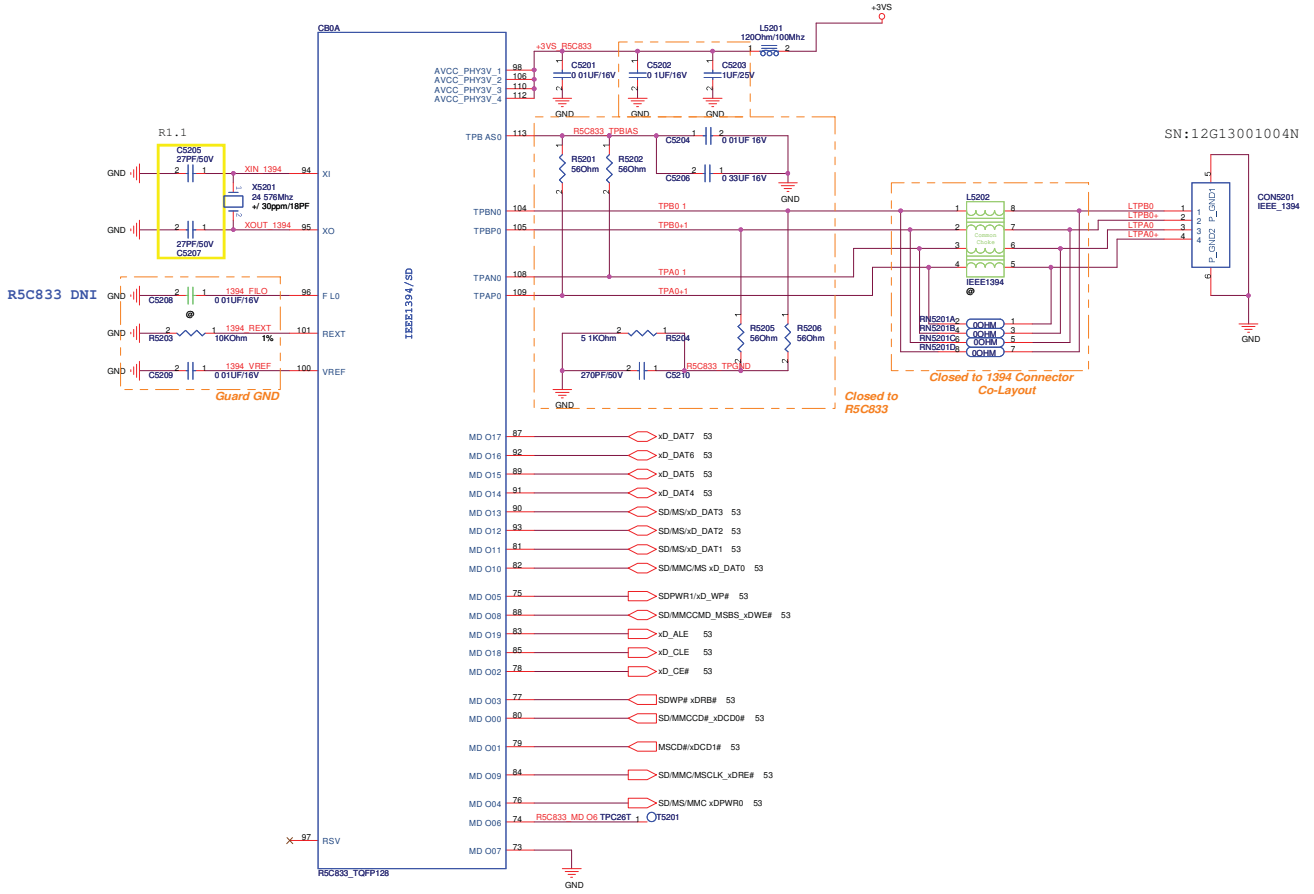
<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC NB1

Title : CARD1394 R5C833(2)

Engineer: Shunmin, Frank

Size	Project Name	Rev
Cus om	A7S	1 0

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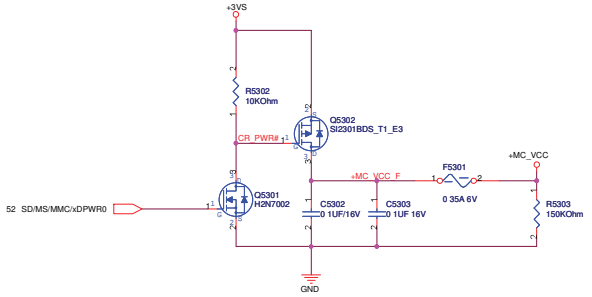
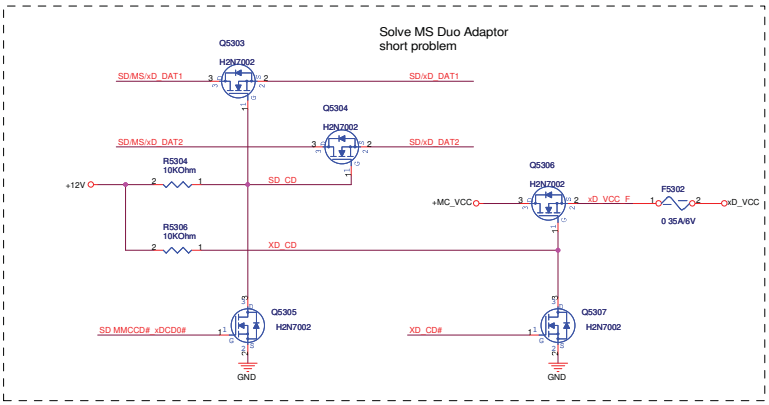
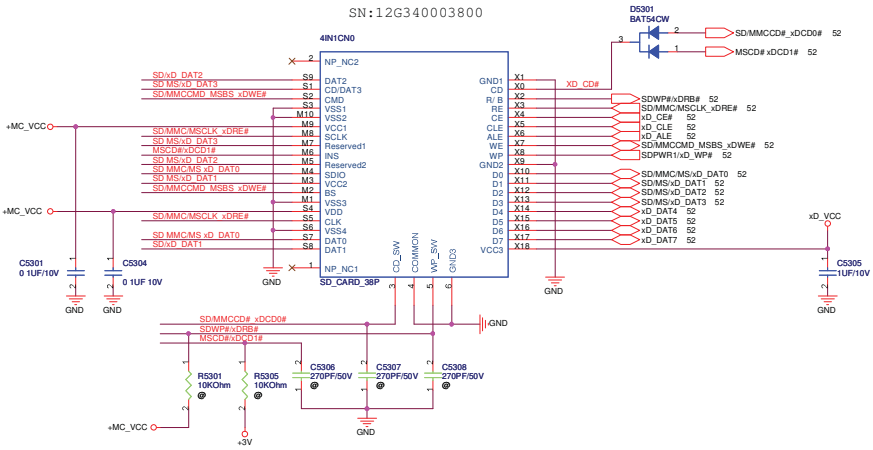
<< Kennedy_Zhang >>







ASUSTeK COMPUTER INC

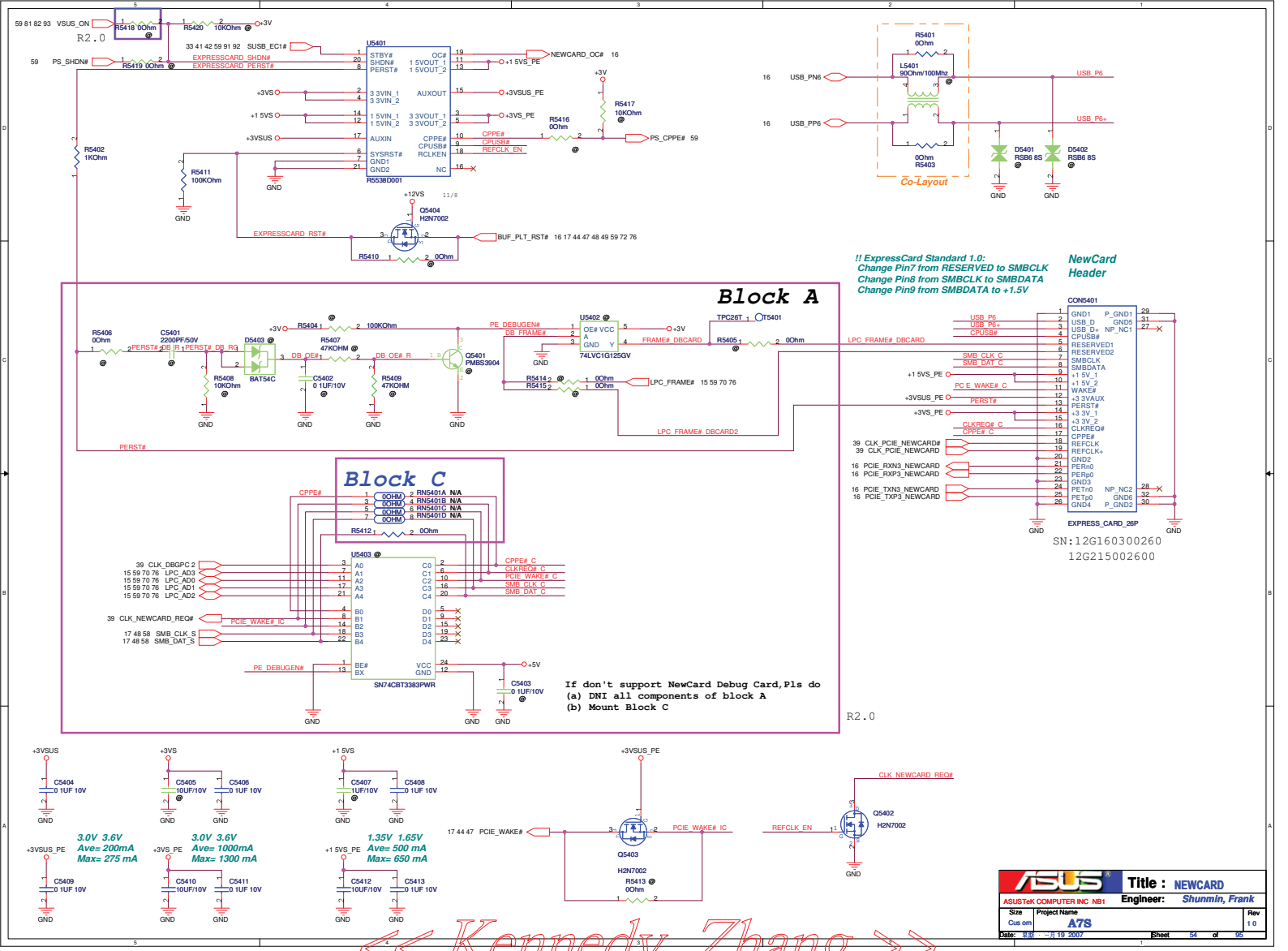
Title : 4 in 1 CARD READER

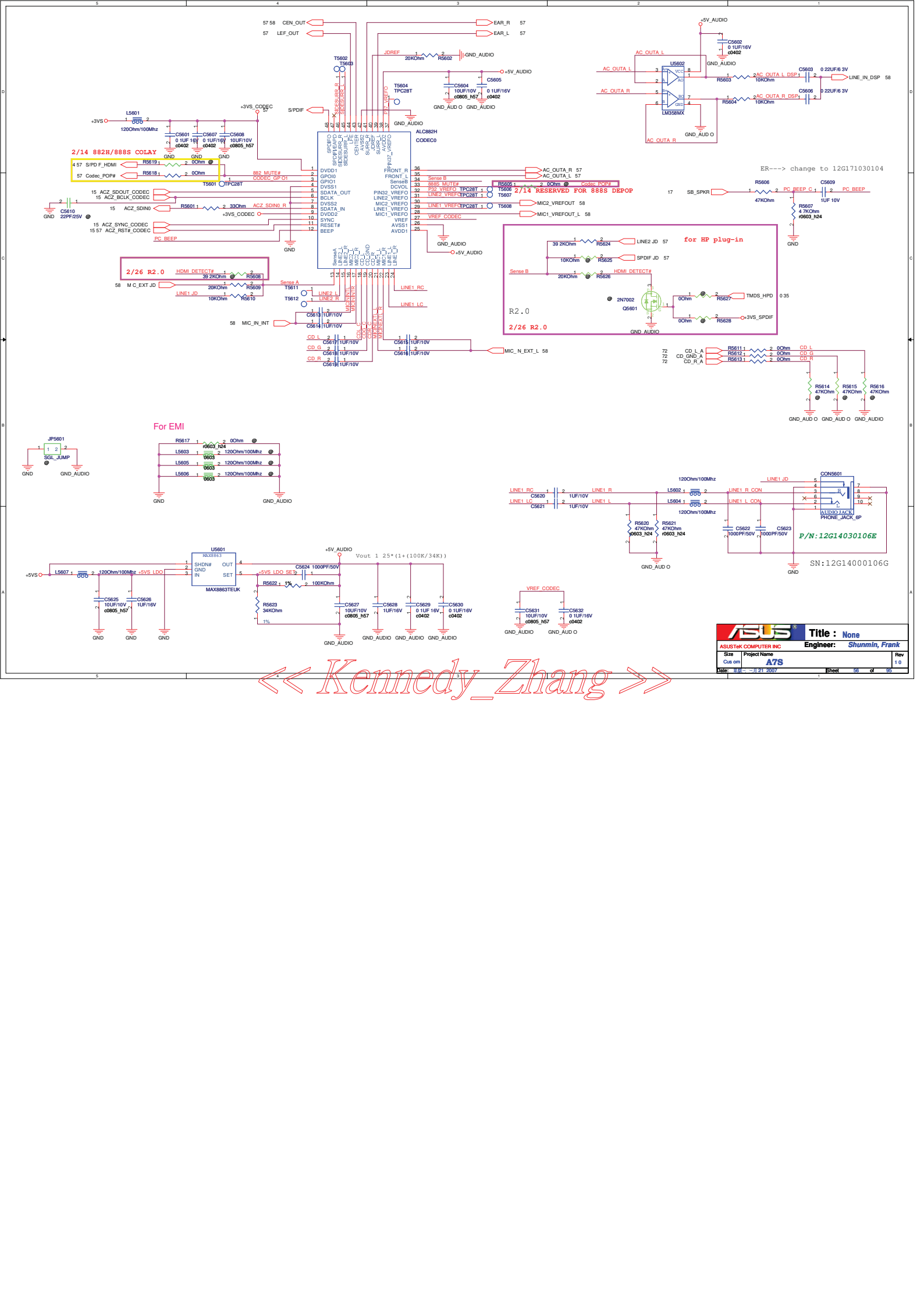
Engineer: Shunmin, Frank

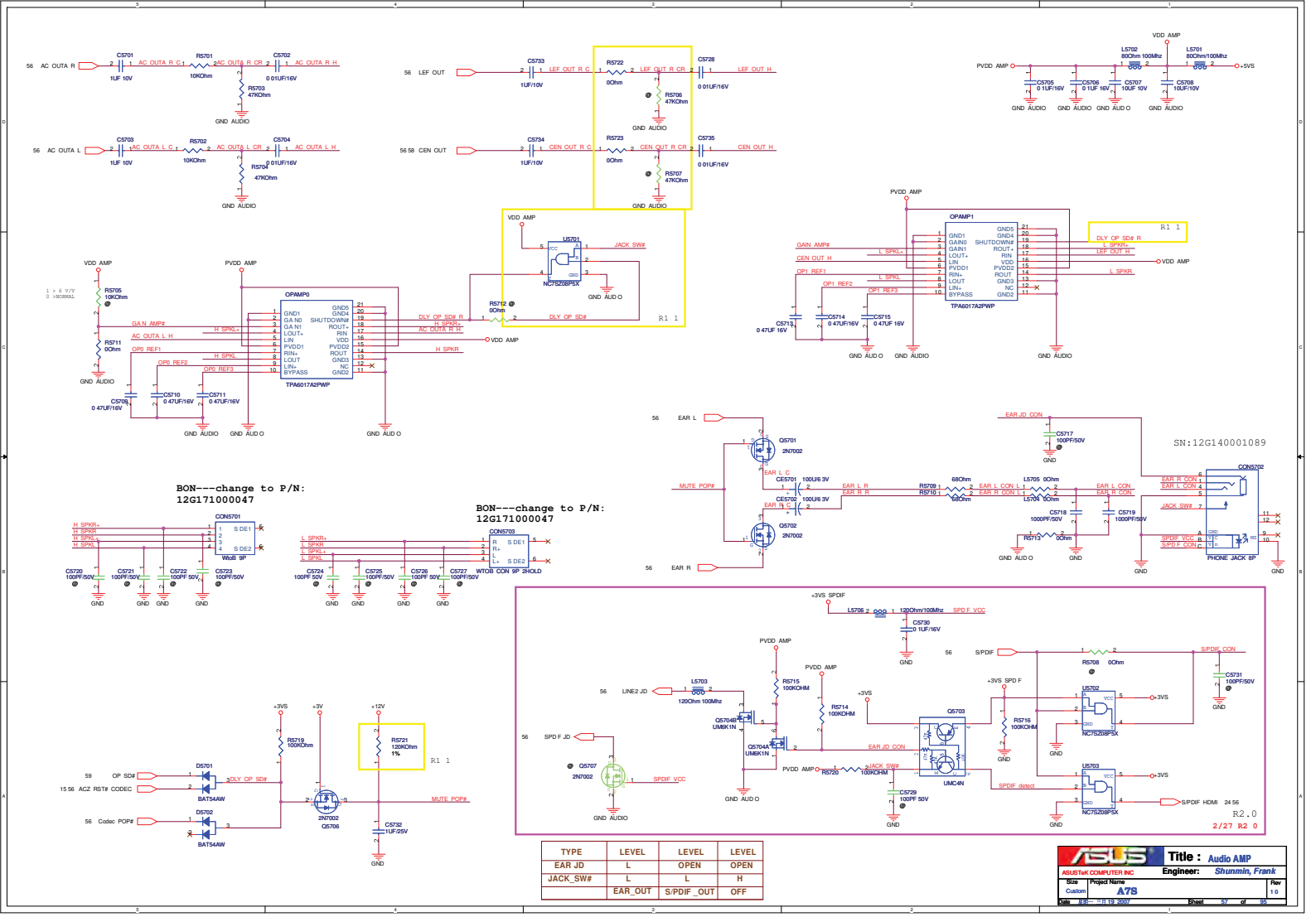
Size	Project Name	Rev
Cus om	A7S	1 0

Date: 星期 一 一月 19 2007 Sheet 53 of 95

<< Kennedy_Zhang >>



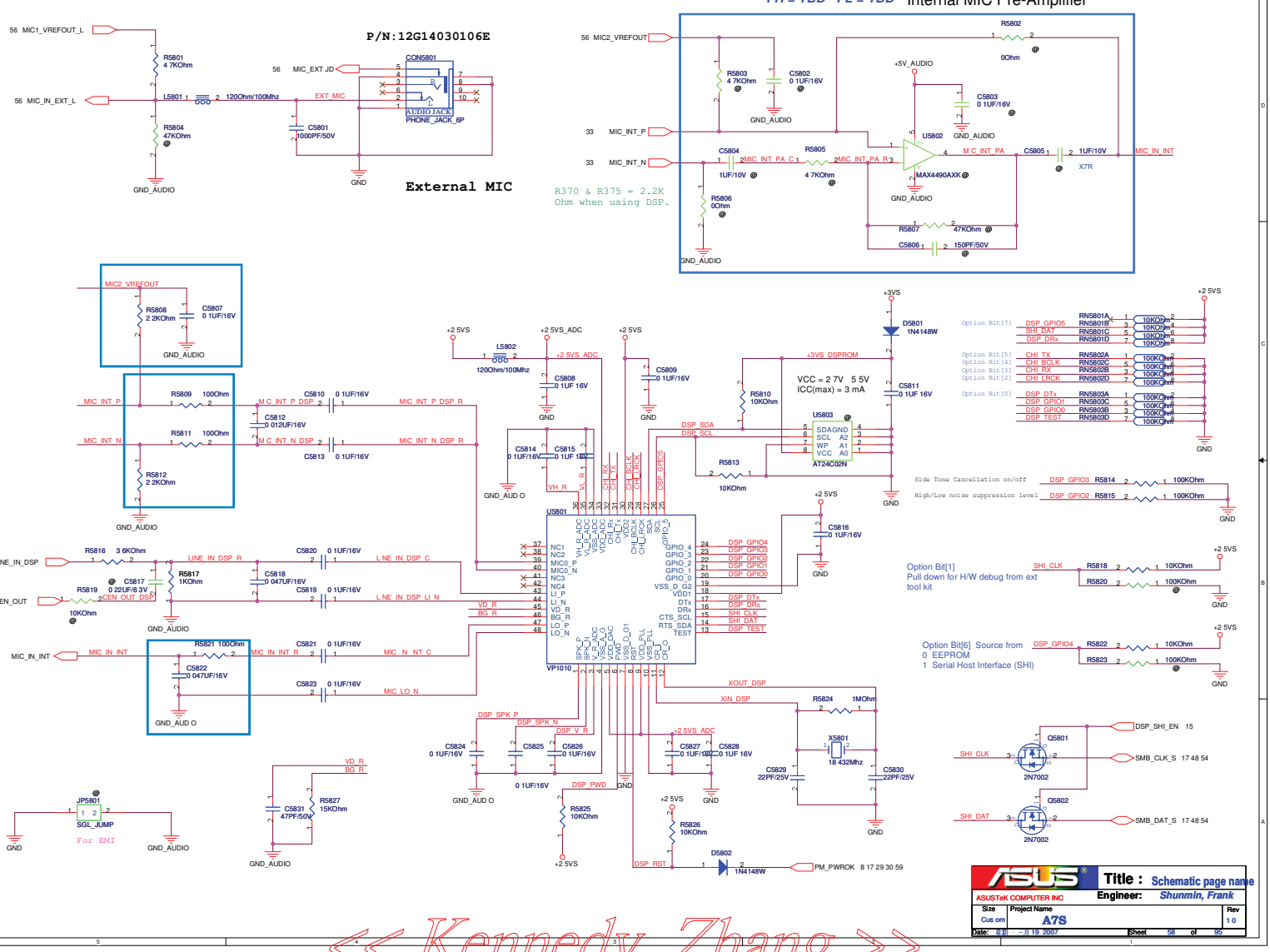

2/14 882H/888S COLAY
2/14 RESERVED FOR 888S DEPOP
ER---> change to 12G171030104
for HP plug-in
2/26 R2.0
R2.0
For EMI
ALC882H
CODEC0
MAX8863TEUK
P/N:12G14030106E
SN:12G14000106G
Title : None
ASUSTeK COMPUTER INC
Engineer: Shunmin, Frank
Project Name A7S
Date: 星期二, 二月 21, 2007
Sheet 56 of 95
<< Kennedy_Zhang >>

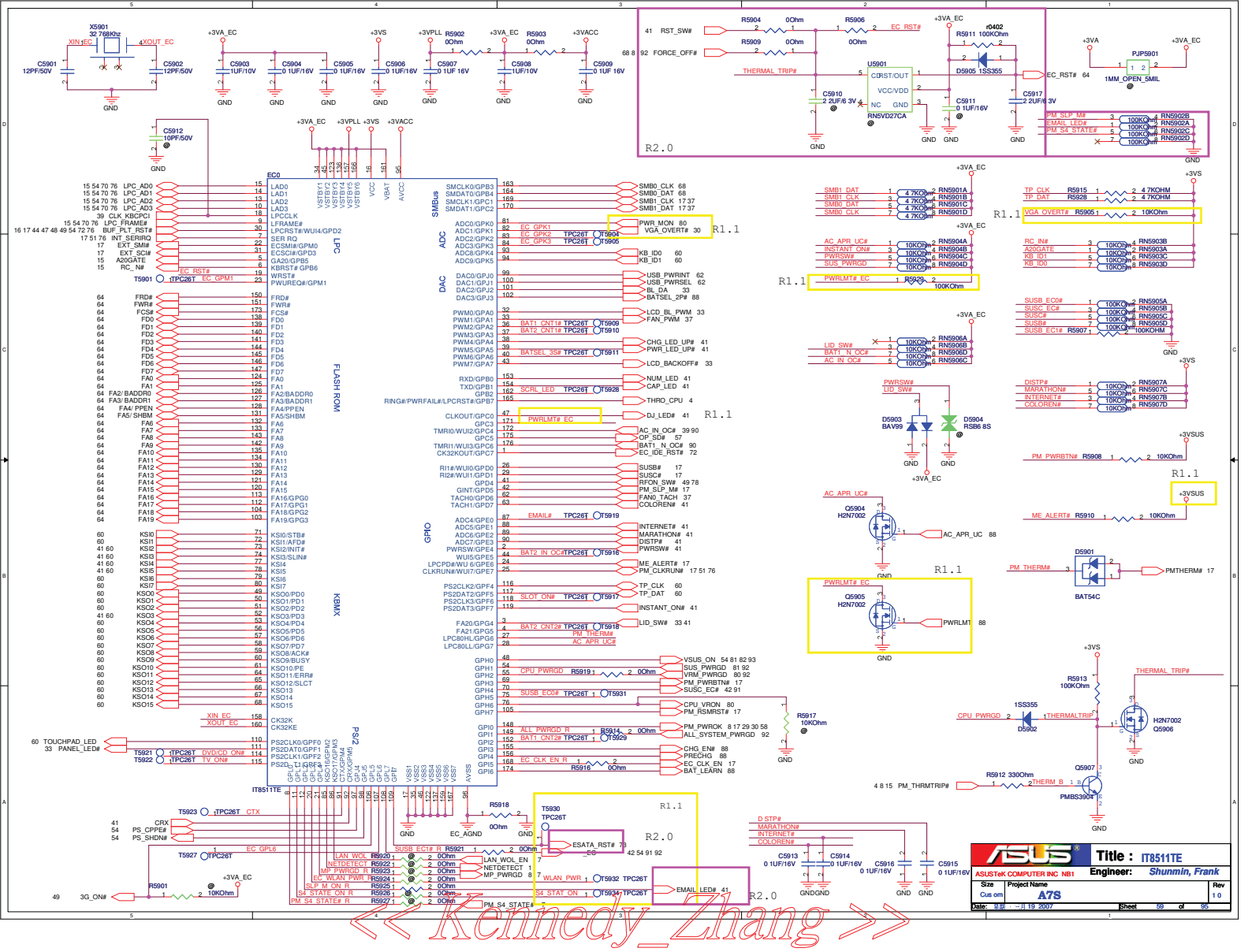


TYPE	LEVEL	LEVEL	LEVEL
EAR JD	L	OPEN	OPEN
JACK_SW#	L	L	H
	EAR_OUT	S/PDIF_OUT	OFF

ASUS	Title : Audio AMP		
ASUSTeK COMPUTER INC	Engineer: Shunmin, Frank		
Size: Custom	Project Name: A7S		Rev: 1.0
Date: 三月 19, 2007	Sheet 57 of 95		

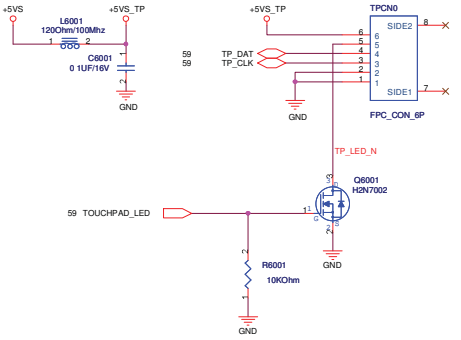
<< Kennedy_Zhang >>


FH = TBD FL = TBD Internal MIC Pre-Amplifier
P/N:12G14030106E
External MIC
R370 & R375 = 2.2K Ohm when using DSP.
MIC_INT_P_DSP_R
MIC_INT_N_DSP_R
LINE_IN_DSP_R
LINE_IN_DSP_L
MIC_IN_INT_R
MIC_LO_N
VD_R
BG_R
XOUT_DSP
XIN_DSP
DSP_SPK_P
DSP_SPK_N
DSP_V_R
DSP_PWD
DSP_RST
DSP_SDA
DSP_SCL
VCC = 2.7V 5.5V
ICC(max) = 3 mA
Option Bit[1]
Pull down for H/W debug from ext tool kit
Option Bit[6] Source from
0 EEPROM
1 Serial Host Interface (SHI)
Side Tone Cancellation on/off
High/Low noise suppression level
For EMI
ASUSTeK COMPUTER INC
Title : Schematic page name
Engineer: Shunmin, Frank
Project Name A7S
Rev 1.0
Sheet 58 of 95
<< Kennedy_Zhang >>


EC0
IT8511TE
Title : IT8511TE
ASUSTeK COMPUTER INC NB1
Engineer: Shunmin, Frank
A7S
Kennedy_Zhang

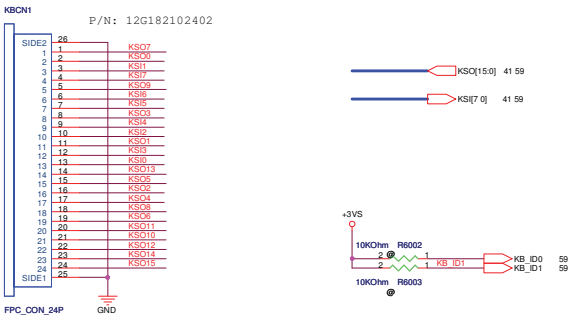
For Touch-Pad

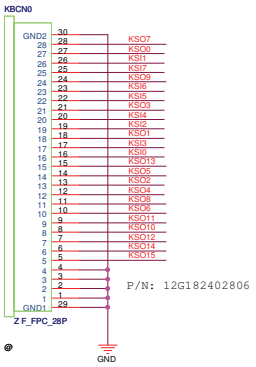
SN:12G182400604



For Keyboard

Big Keyboard for A7S





Small Keboard for G2S

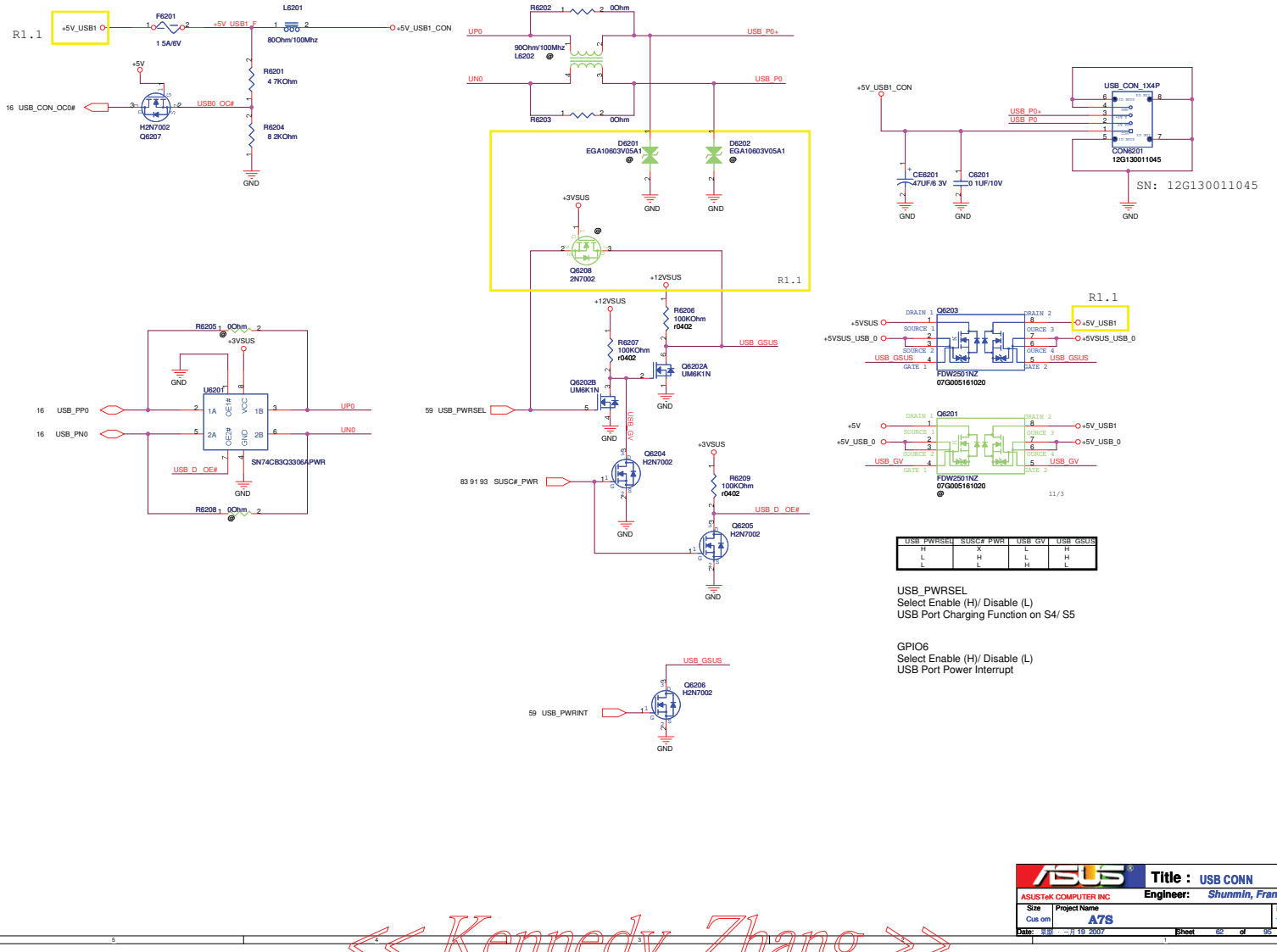
ASUSTeK COMPUTER INC NB1	Title : Touch Pad & KB	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 60 of 95	

<< Kennedy_Zhang >>

Remove IAMT control logic

R1.1

ASUSTeK COMPUTER INC NB1	Title: Sequence Control Logic		
	Engineer: Shunmin, Frank		
Size: Custom	Project Name: A7S		Rev: 1.0
Date: 星期 一 一月 19 2007		Sheet 61 of 95	



USB_PWRSEL	SUSC# PWR	USB_GV	USB_GSUS
H	X	L	H
L	H	L	L
L	L	H	L

USB_PWRSEL
Select Enable (H)/ Disable (L)
USB Port Charging Function on S4/ S5

GPIO6
Select Enable (H)/ Disable (L)
USB Port Power Interrupt

ASUSTeK COMPUTER INC

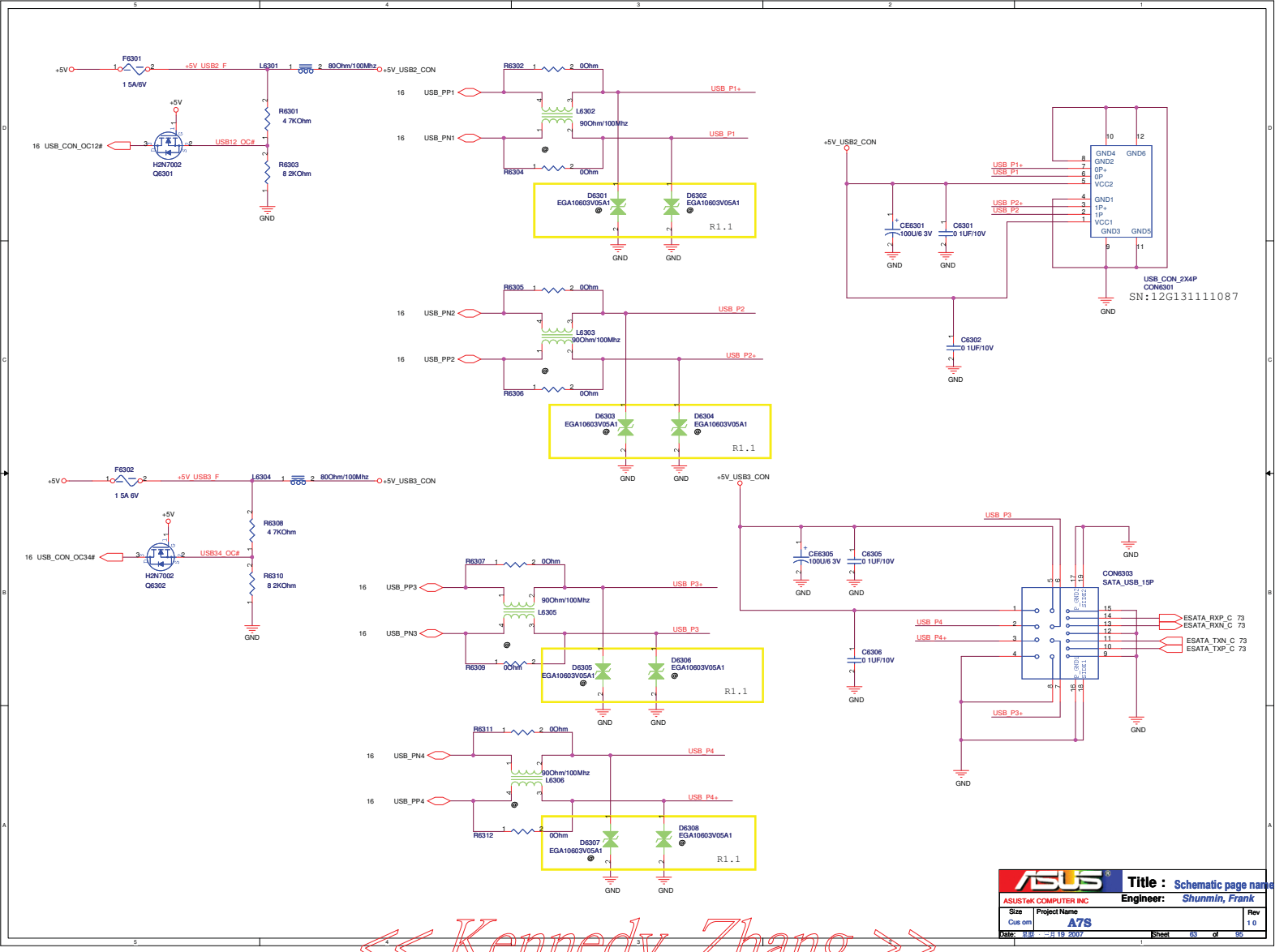
Title : USB CONN

Engineer: Shunmin, Frank

Size	Project Name	Rev
Cus om	A7S	1 0

Date: 星期 一 一月 19 2007 Sheet 62 of 95

<< Kennedy_Zhang >>



ASUSTeK COMPUTER INC

Title : Schematic page name

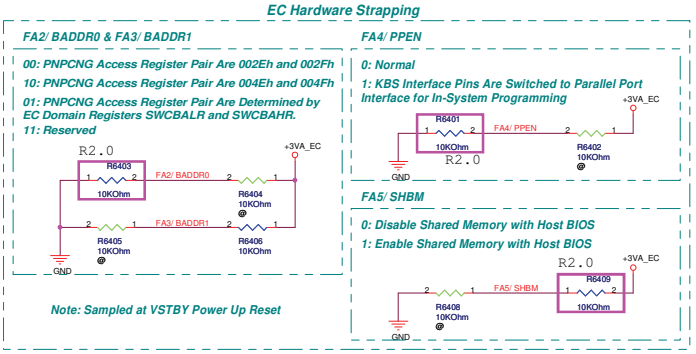
Engineer: Shunmin, Frank

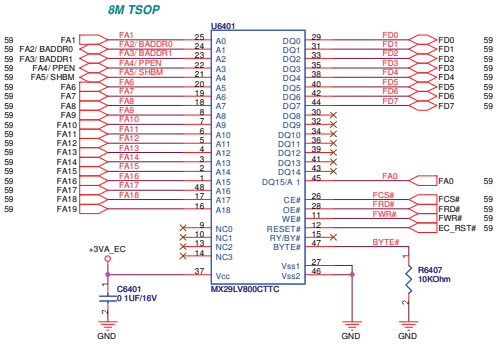
Size	Project Name	Rev
Cus om	A7S	1 0

Date: 星期 一月 19 2007 Sheet 63 of 95

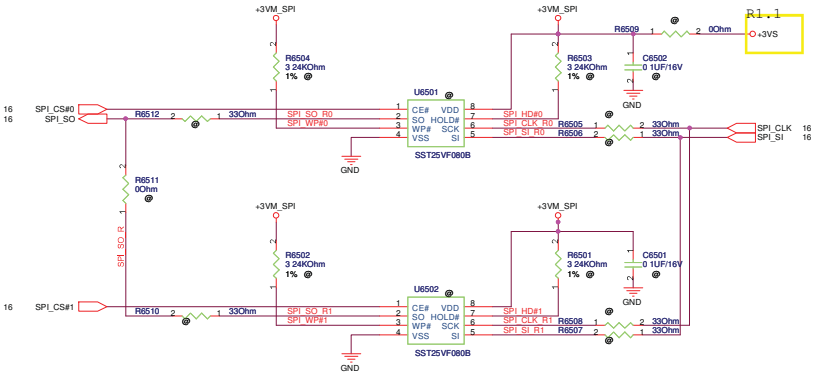
<< Kennedy_Zhang >>

ISA ROM



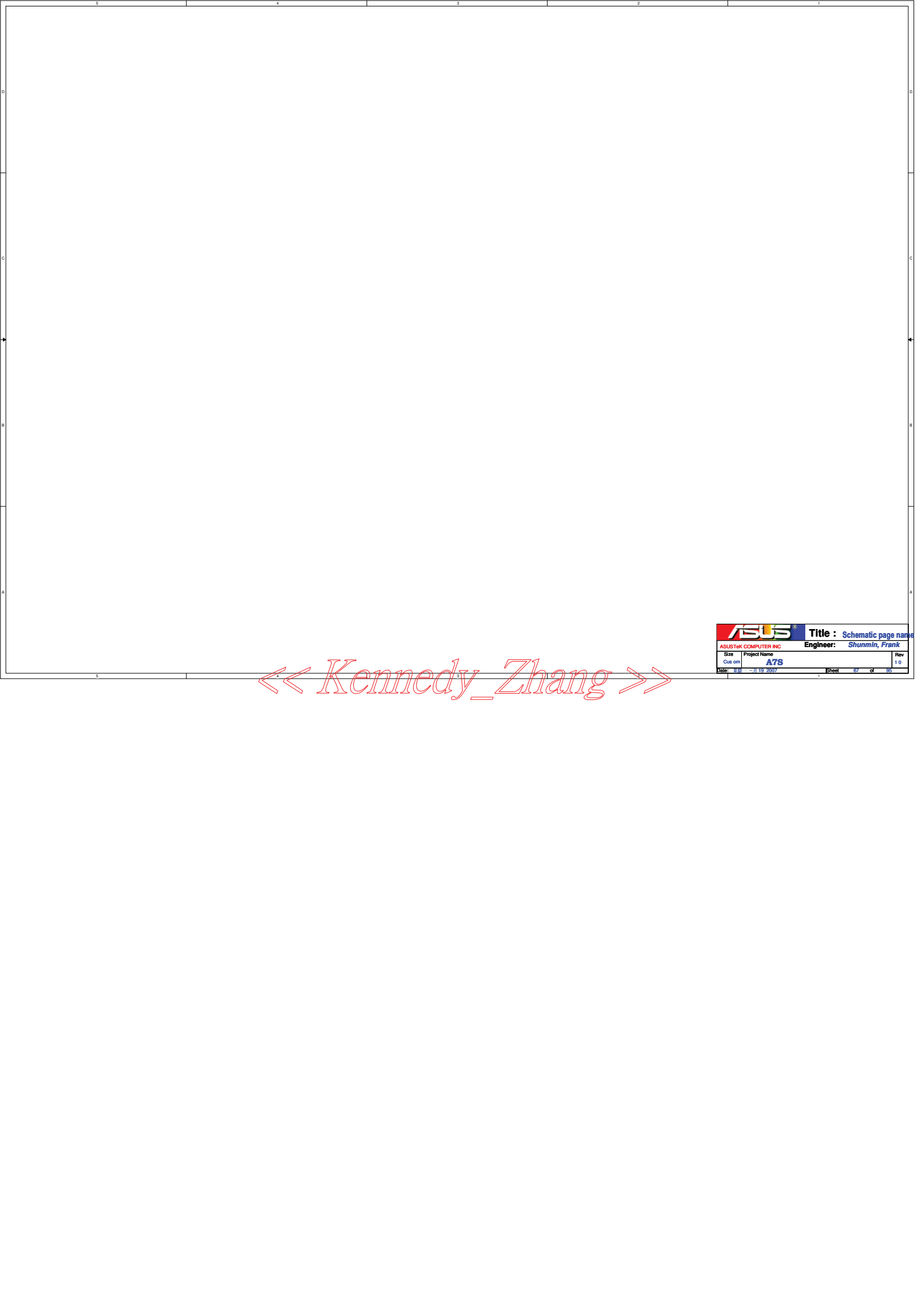


ASUSTeK COMPUTER INC NB1	Title : ISA ROM	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 二月 19 2007	Sheet 64 of 95	

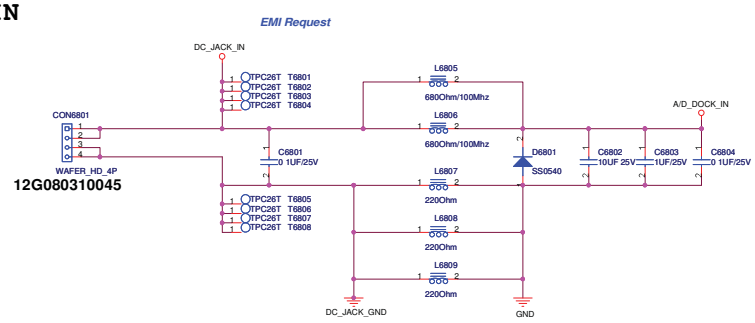


ASUSTeK COMPUTER INC NB1	Title : SPI ROM		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1.0
Date: 星期 一 一月 19 2007	Sheet 65 of 95		

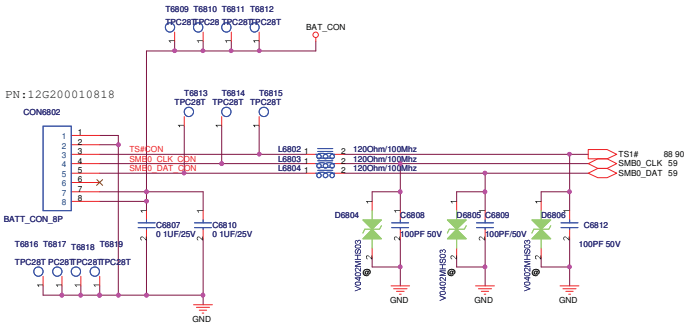
ASUSTeK COMPUTER INC	Title : LED		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 66 of 95		



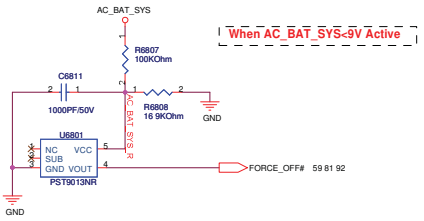
DC-IN



Battery Connector



Without Battery & Pull out Adapter

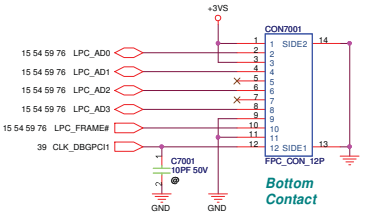


ASUSTeK COMPUTER INC NB1	Title : DC & BAT IN	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 二月 19 2007	Sheet 68 of 95	

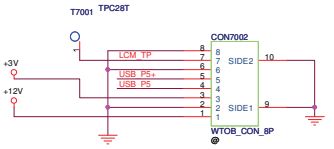
ASUSTeK COMPUTER INC			Title :	Schematic page name
			Engineer:	Shunmin, Frank
Size	Project Name			Rev
Cus om	A7S			1 0
Date: 星期 一 一月 19 2007			Sheet 69 of 95	

For Debug

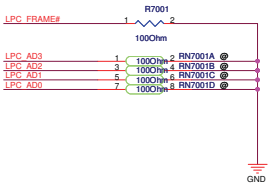
If support NewCard Debug Card,
Pls don't mount all components.

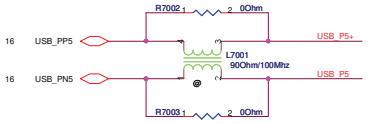


Bottom Contact



For G2S





ASUSTeK COMPUTER INC	Title : Debug CONN.		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1 0
Date: 星期二, 一月 21, 2007	Sheet 70 of 95		

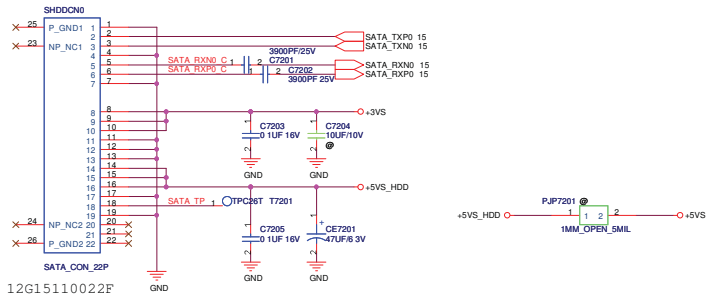
ASUSTeK COMPUTER INC

Title : Schematic page name

Engineer: Shunmin, Frank

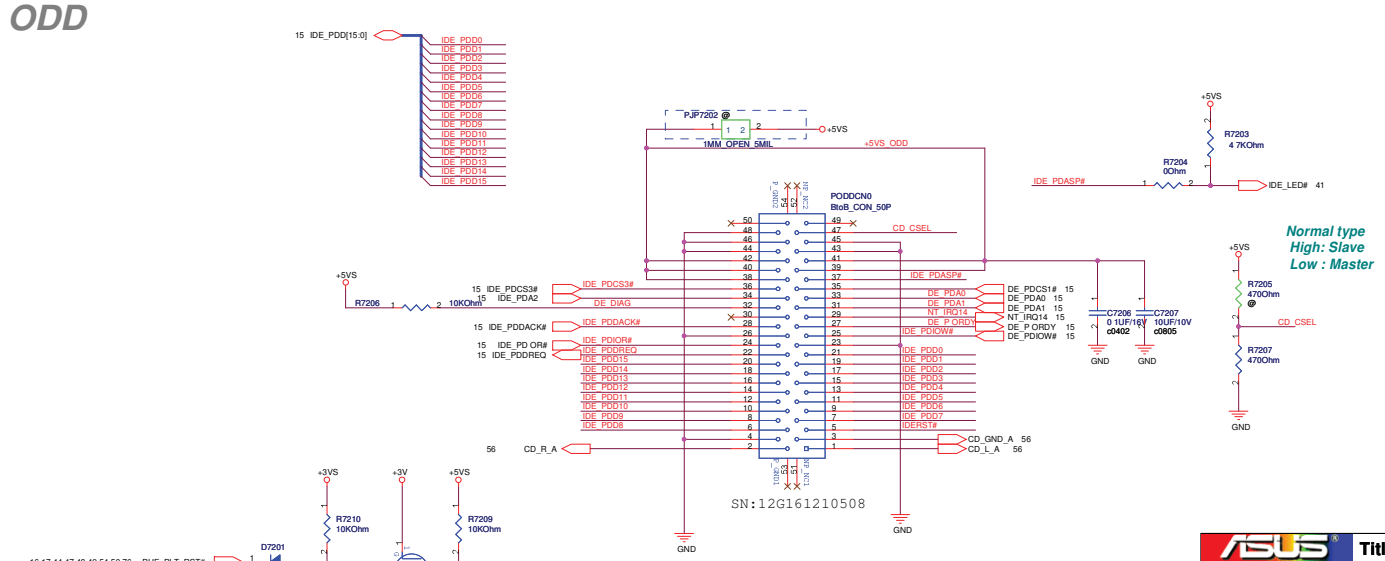
Size	Project Name	Rev
Cus om	A7S	1 0

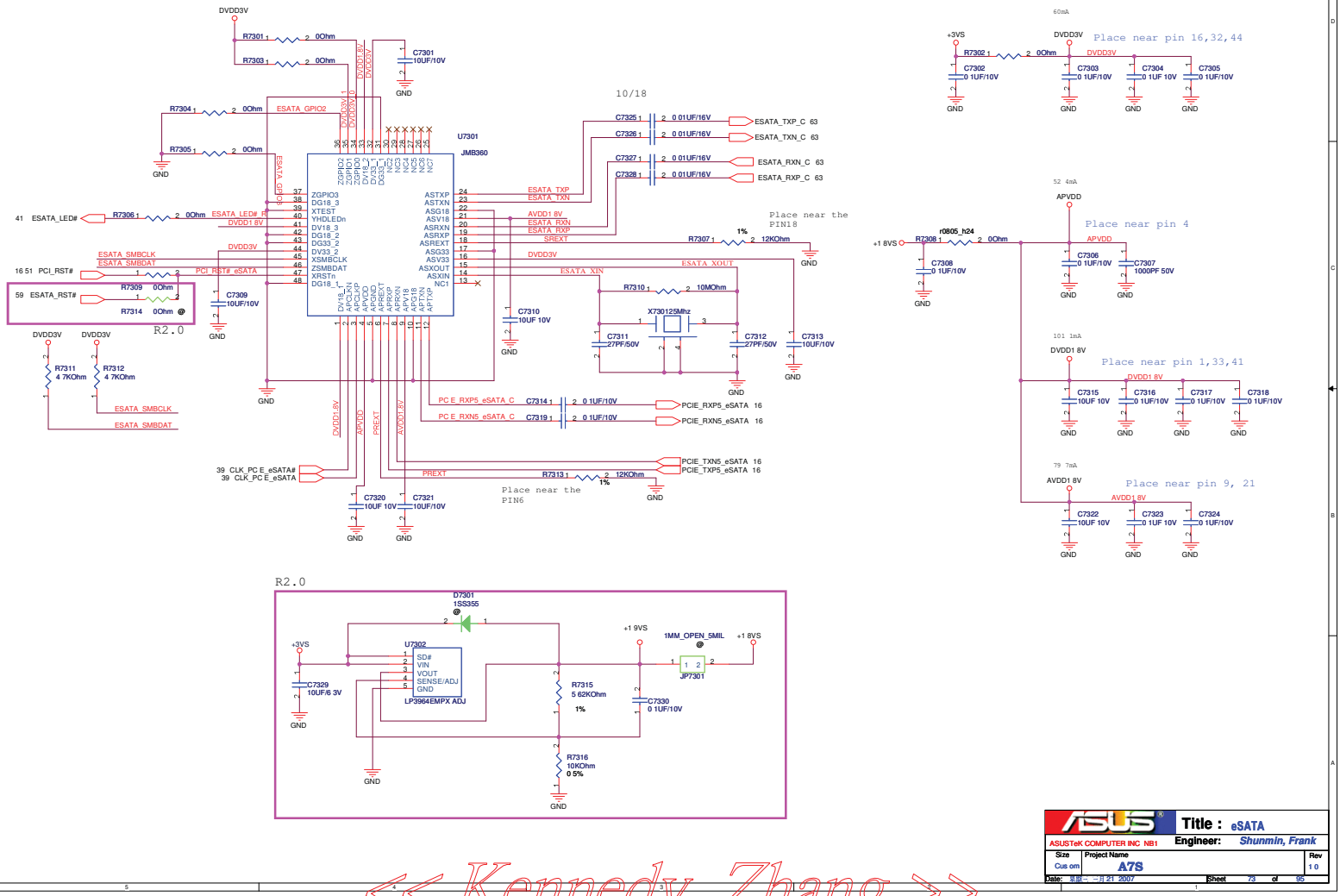
Date: 星期 一 一月 19 2007 Sheet 71 of 95



SATA HDD

ODD



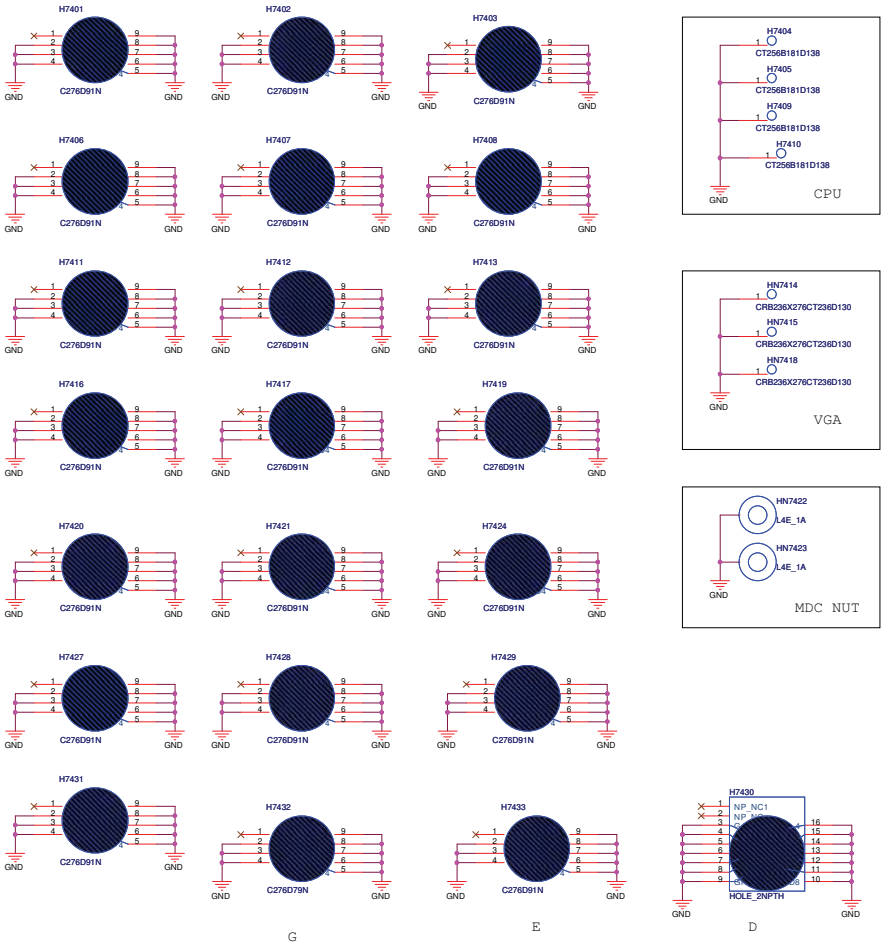


R2.0

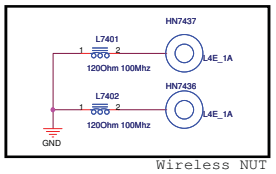
ASUSTeK COMPUTER INC NB1	Title : eSATA		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1.0
Date: 星期二, 一月 21, 2007	Sheet 73 of 95		

<< Kennedy_Zhang >>

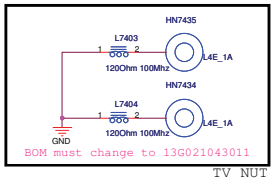
remember MDC 2 NUT
MINI CARD 6 NUT



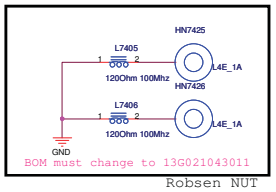
G E D



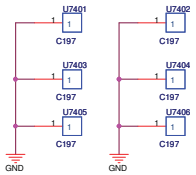
Wireless NUT



TV NUT



Robsen NUT

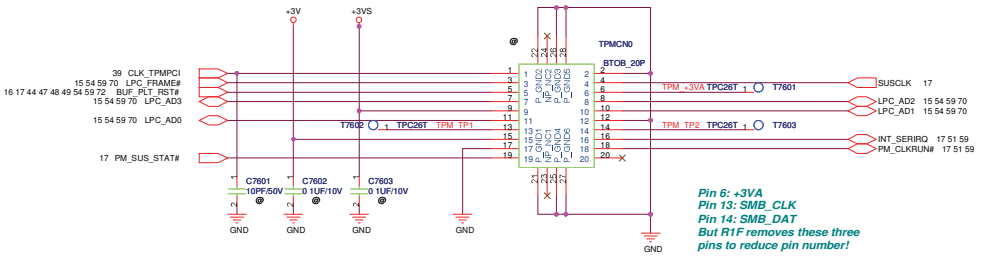


ASUSTeK COMPUTER INC	Title : SREW HOLE	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期二 三月 20 2007	Sheet 74 of 95	

<< Kennedy_Zhang >>

ASUSTeK COMPUTER INC			Title :	Schematic page name
			Engineer:	Shunmin, Frank
Size	Project Name			Rev
Cus om	A7S			1 0
Date: 星期 一 一月 19 2007			Sheet 75 of 95	

For TPM Module

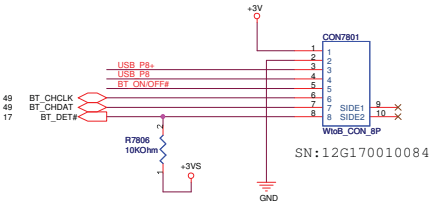


Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

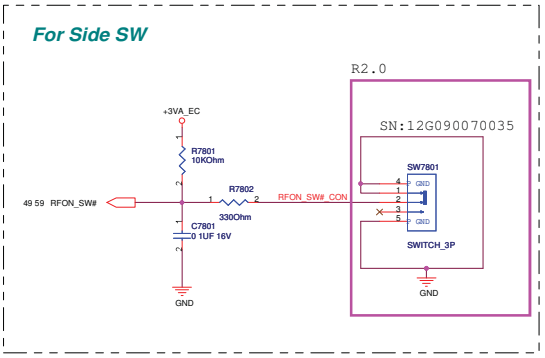
ASUSTeK COMPUTER INC	Title : TPM		
	Engineer: Shunmin, Frank		
Size: Cus om	Project Name: A7S		Rev: 1.0
Date: 星期 一 一月 19 2007	Sheet 76 of 95		

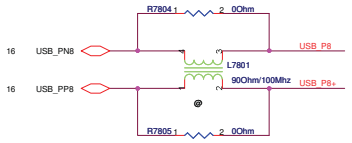
ASUSTeK COMPUTER INC			Title: Schematic page name	
			Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S			Rev: 1 0
Date: 星期 一 一月 19 2007		Sheet 77 of 95		

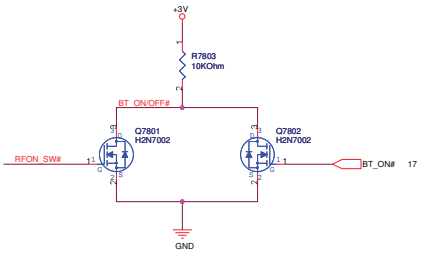
For Bluetooth



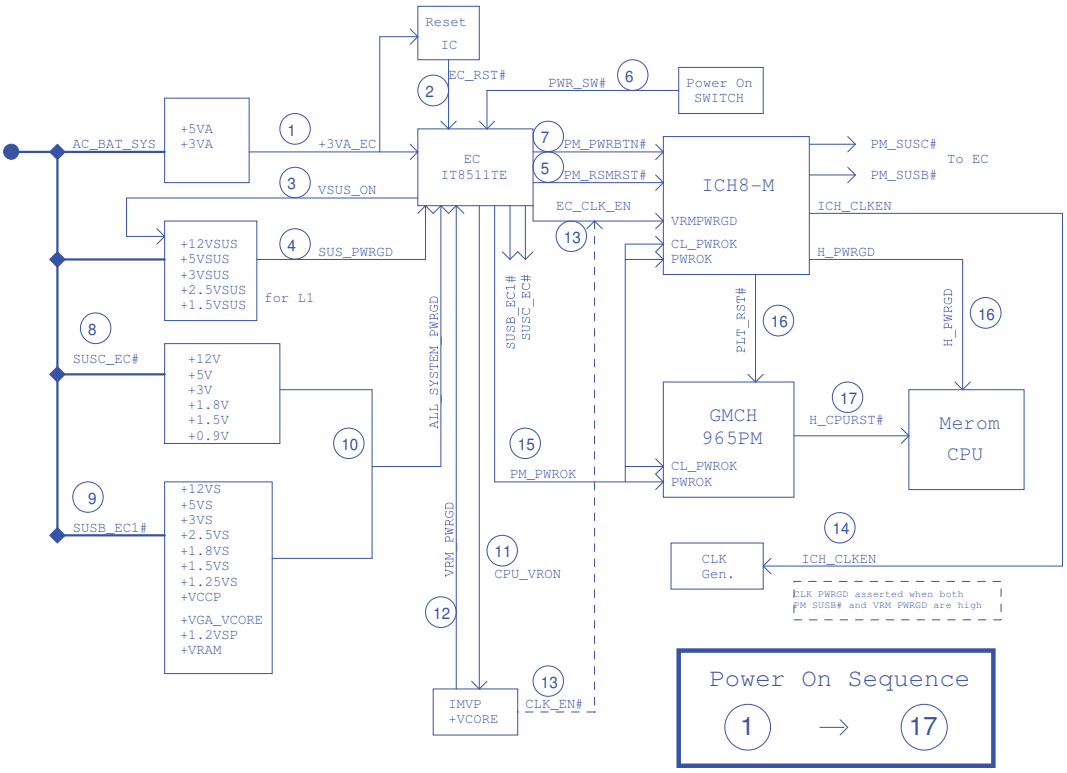
For Side SW







ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: Shunmin, Frank	
Size: Cus om	Project Name: A7S	Rev: 1 0
Date: 星期 一 一月 19 2007	Sheet 78 of 95	



ASUSTeK COMPUTER INC

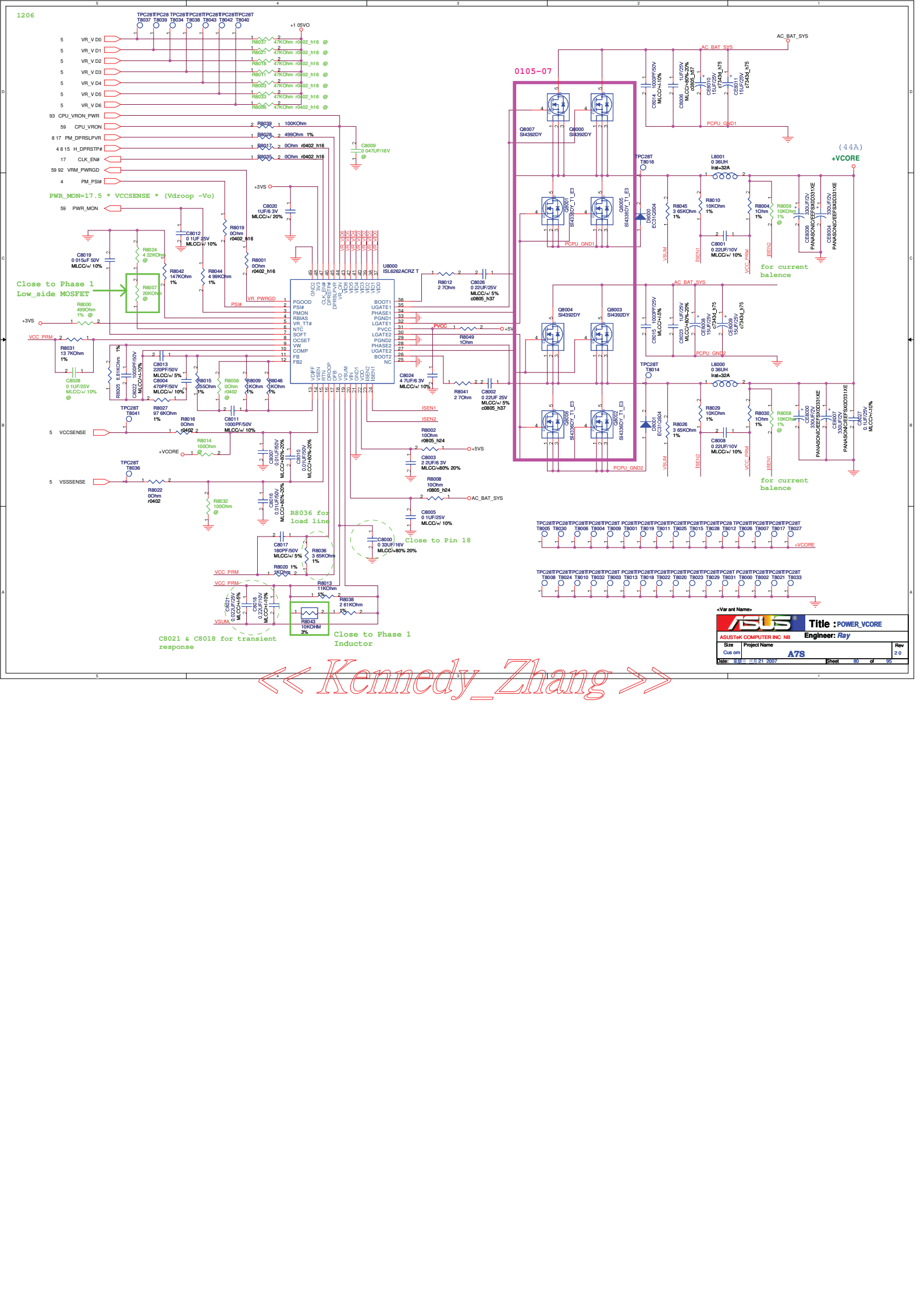
Title : POWER SEQUENCE

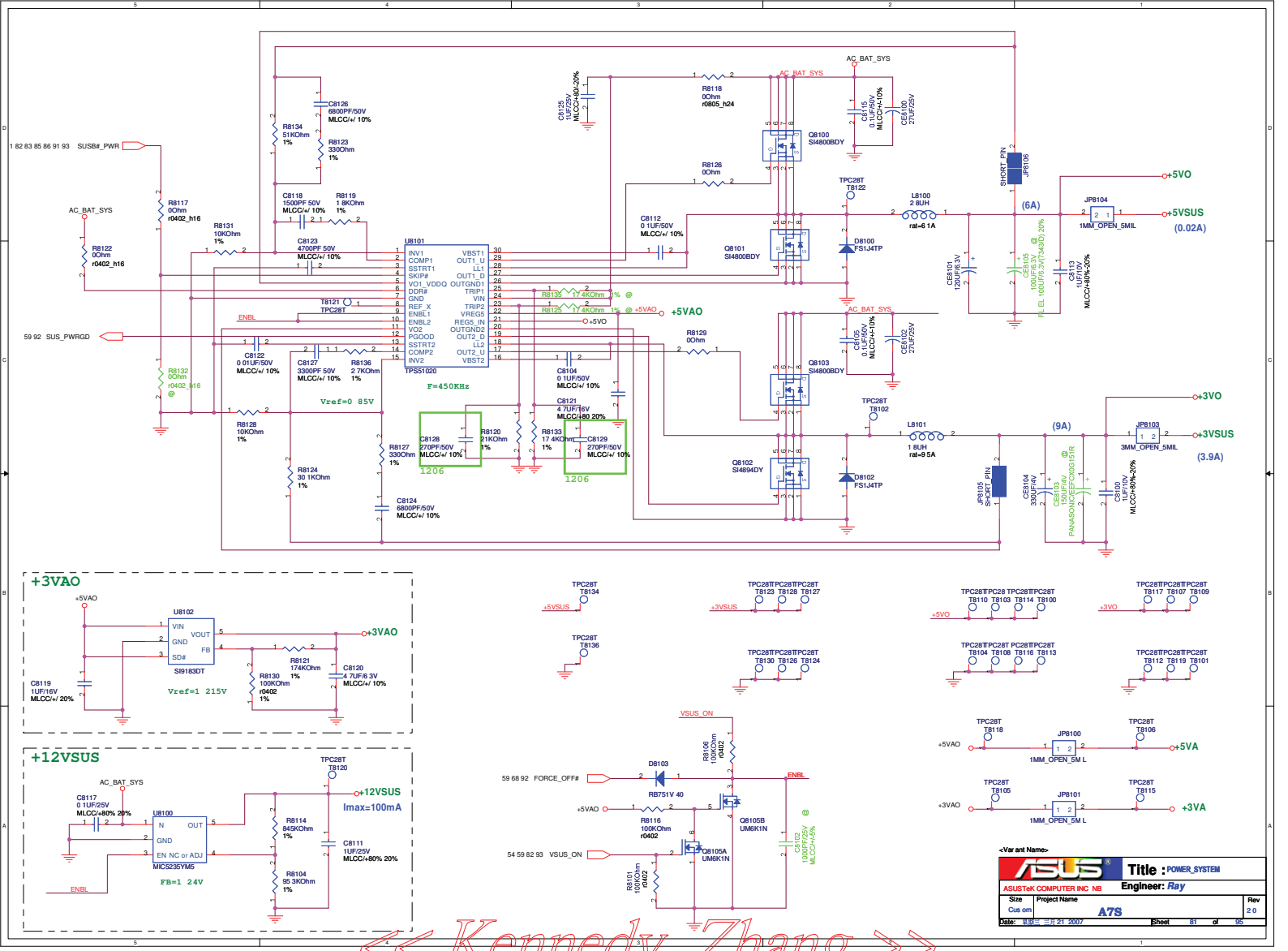
Engineer: Shunmin, Frank

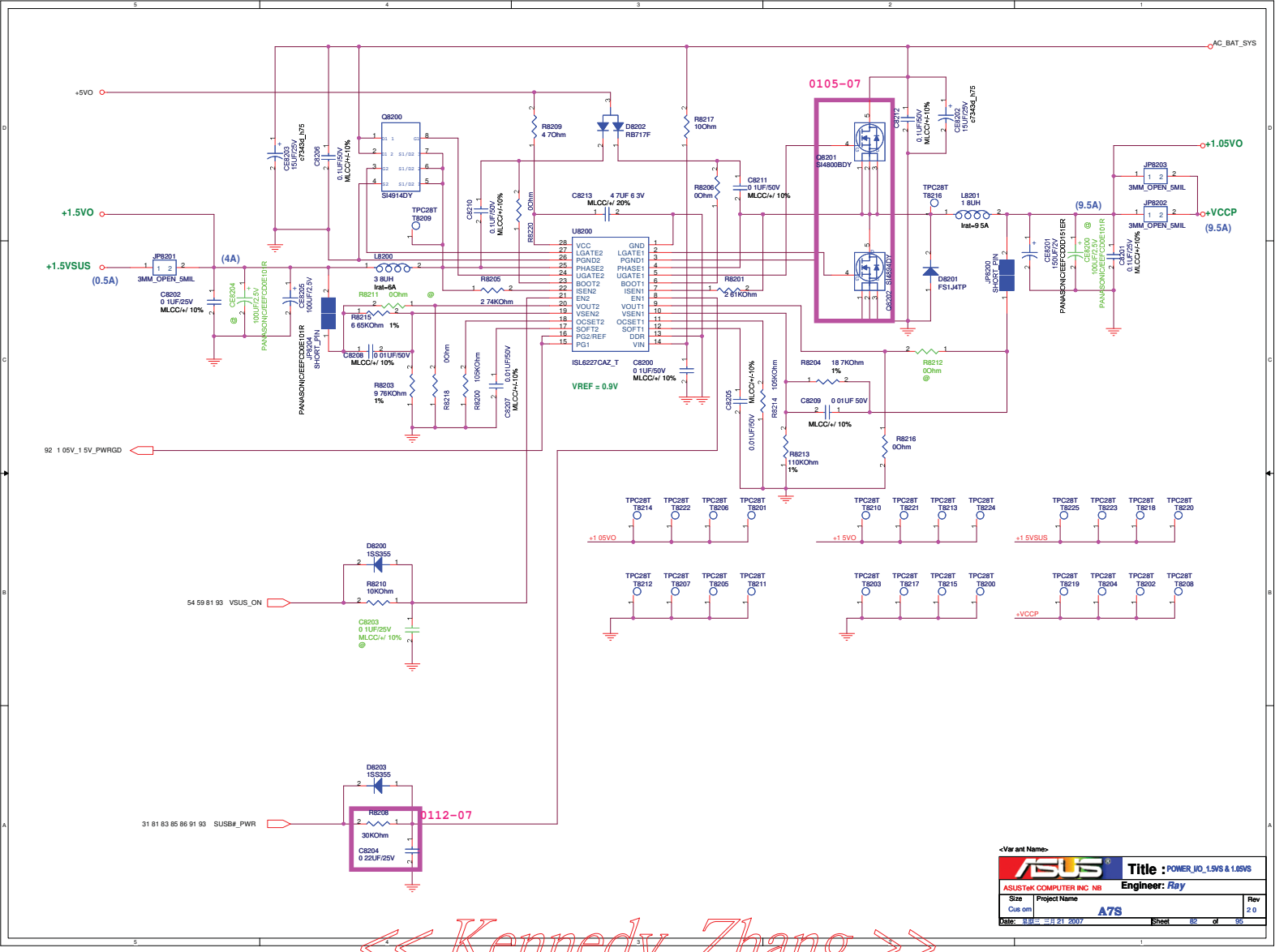
Size: C | Project Name: A7S | Rev: 1.0

Date: Wed, Jul 25 2007 | Sheet 79 of 95

<< Kennedy_Zhang >>


1206
0105-07
(44A)
+VCORE
PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
Close to Phase 1
Low_side MOSFET
for current
balence
R8036 for
load line
Close to Pin 18
C8021 & C8018 for transient
response
Close to Phase 1
Inductor
Title : POWER_VCORE
ASUSTeK COMPUTER INC NB
Engineer: Ray
A7S
<< Kennedy_Zhang >>

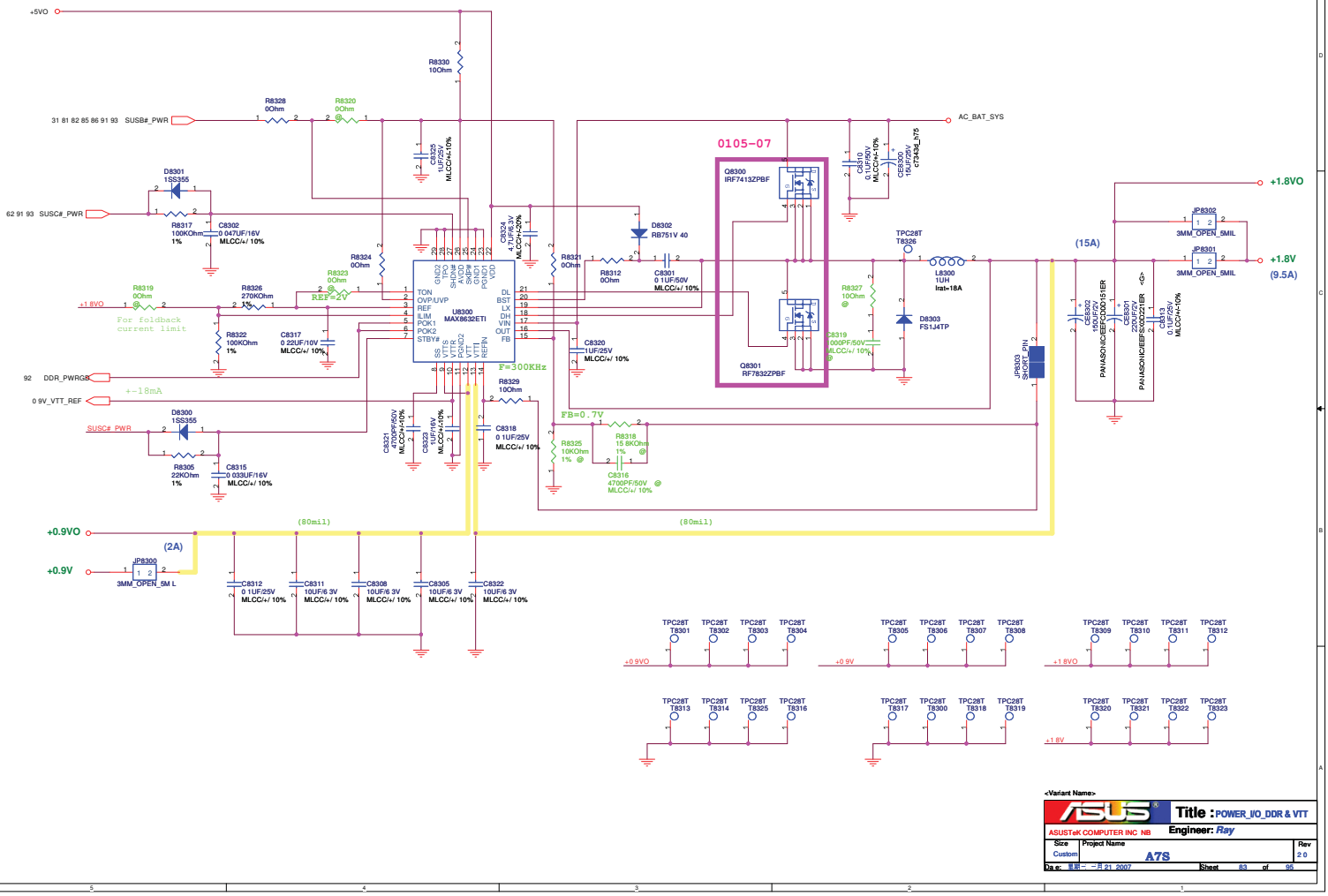




<Var ant Name>

ASUSTeK COMPUTER INC NB	Title : POWER_I/O_1.5VS & 1.05VS	
	Engineer: Ray	
Size: Cus om	Project Name: A7S	Rev: 2 0
Date: 星期三 三月 21 2007	Sheet 82 of 95	

<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC NB

Title : POWER_I/O_DDR & VTT

Engineer: Ray

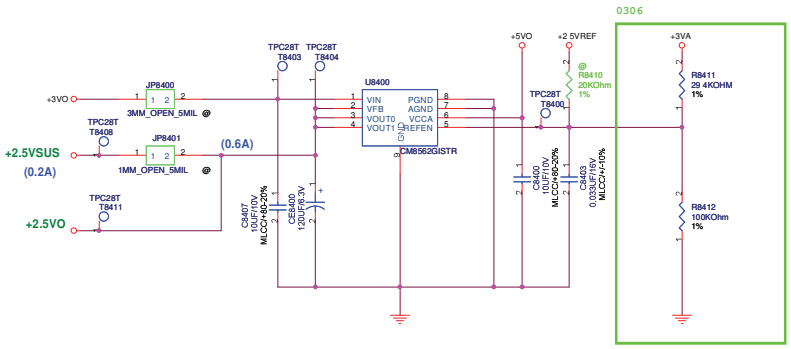
Size	Project Name	Rev
Custom	A7S	2.0

Date: 星期二 一月 21 2007 Sheet 83 of 95

<< Kennedy_Zhang >>

+2.5VS & +2.5VSUS

0704



<Variant Name>

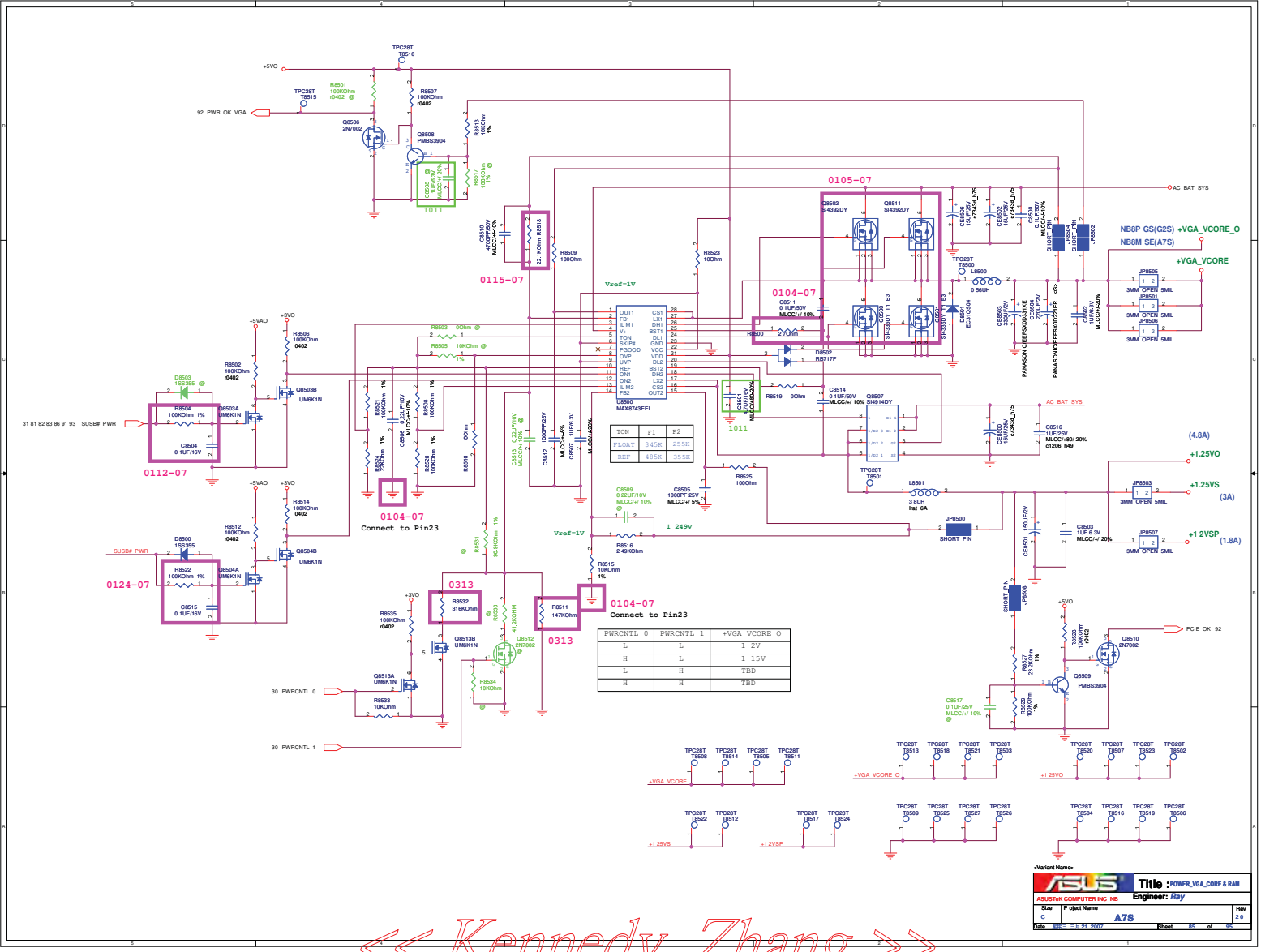
ASUSTeK COMPUTER INC NB

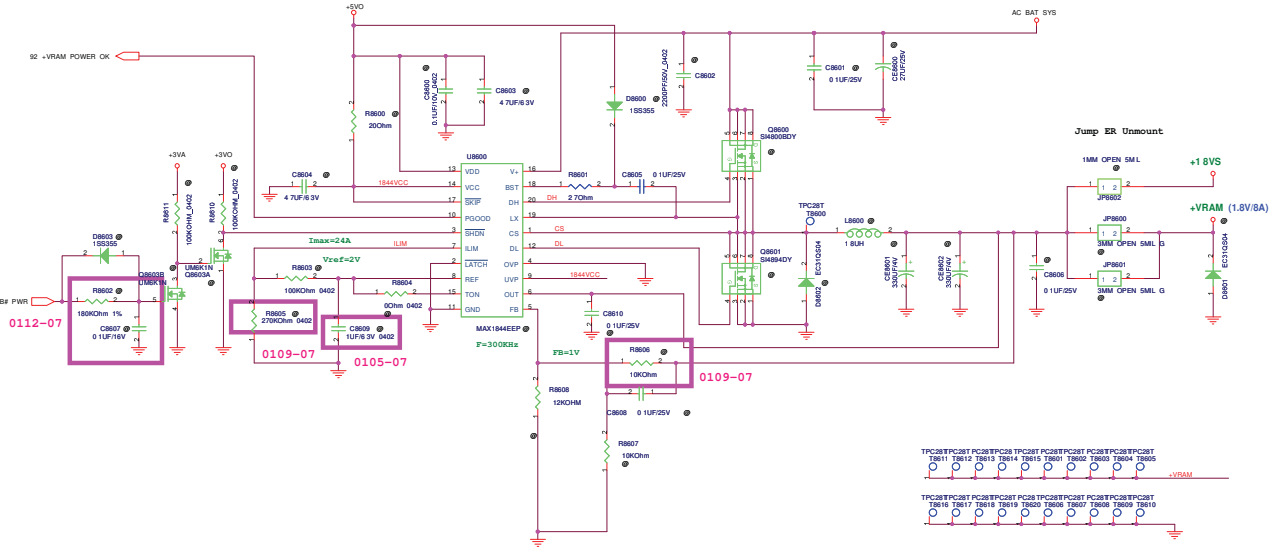
Title : POWER_I/O_ +2.5VS

Engineer: Ray

Size	Project Name	Rev
Cus om	A7S	2.0

Date: 星期三 三月 21 2007 Sheet 84 of 95





<Variant Name>

ASUSTeK COMPUTER INC NB	Title : +VRAM	
	Engineer: Ray	
Size: C	P oject Name: A7S	Rev: 2.0
Date: Fri Jan 26 2007	Sheet 55 of 55	

<Variant Name>

Title : POWER_SHUTDOWN#

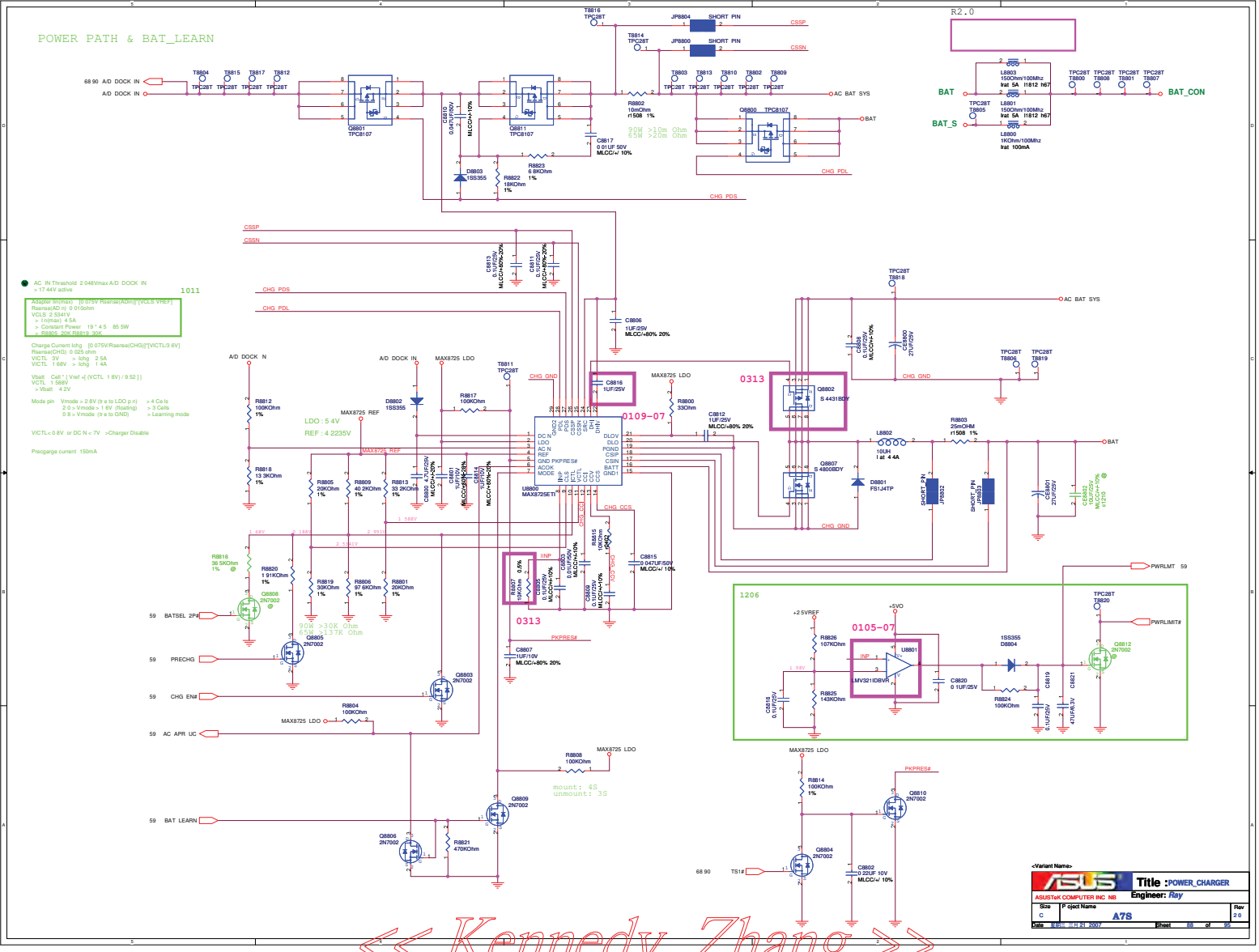
ASUSTeK COMPUTER INC NB

Engineer: Ray

Size	Project Name	Rev
Cus om	A7S	2 0

Date: 星期二, 一月 21, 2007 Sheet 87 of 95

<< Kennedy_Zhang >>


POWER PATH & BAT_LEARN
R2.0
A/D DOCK IN
AC BAT SYS
BAT
BAT_CON
BAT_S
CSSP
CSSN
CHG_PDS
CHG_PDL
CHG_GND
MAX8725 LDO
MAX8725 REF
LDO : 5.4V
REF : 4.2235V
0109-07
0313
0105-07
1206
1011
PKPRES#
PWRLMT 59
PWRLIMIT#
BATSEL 2P#
PRECHG
CHG EN#
AC APR UC
BAT LEARN
TS1#
mount: 4S
unmount: 3S
90W >10K Ohm
65W >137K Ohm
<Variant Name>
Title : POWER_CHARGER
ASUSTeK COMPUTER INC NB
Engineer: Ray
A7S
Kennedy_Zhang

<Var ant Name>

Title : N/A

ASUSTeK COMPUTER INC NB

Engineer: Ray

Size	Project Name	Rev
Cus om	A7S	2 0

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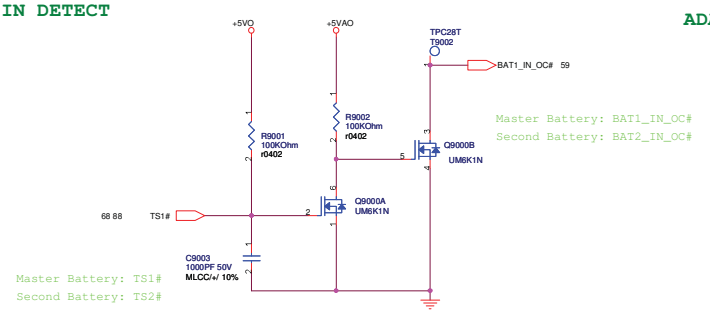
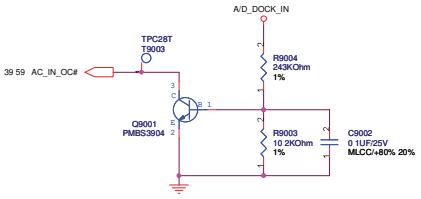
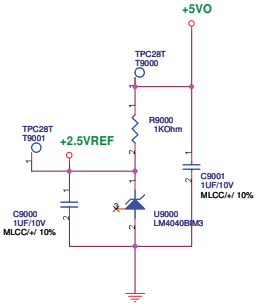
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



<Var ant Name>

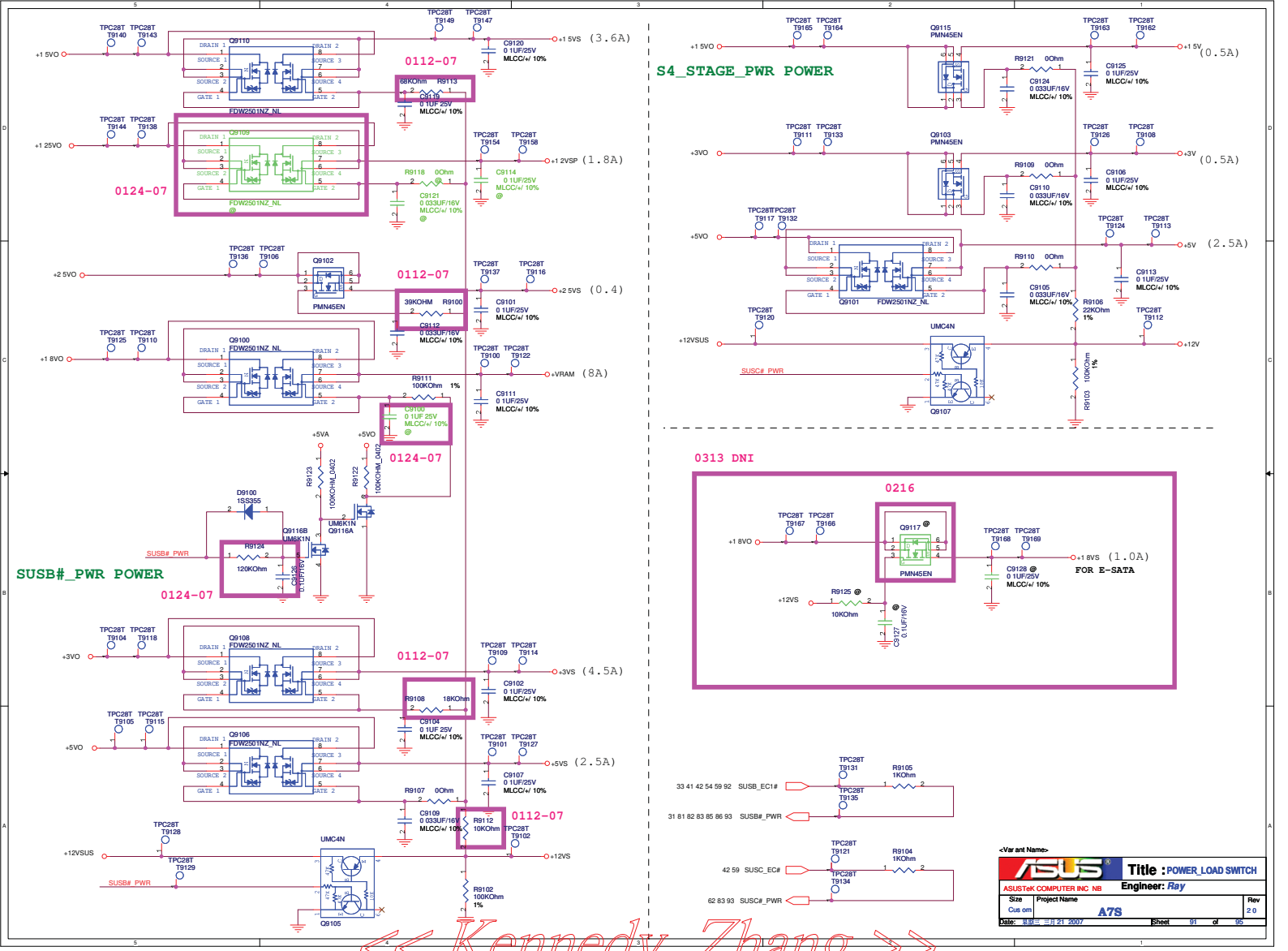
ASUSTeK COMPUTER INC NB

Title : POWER_DETECT

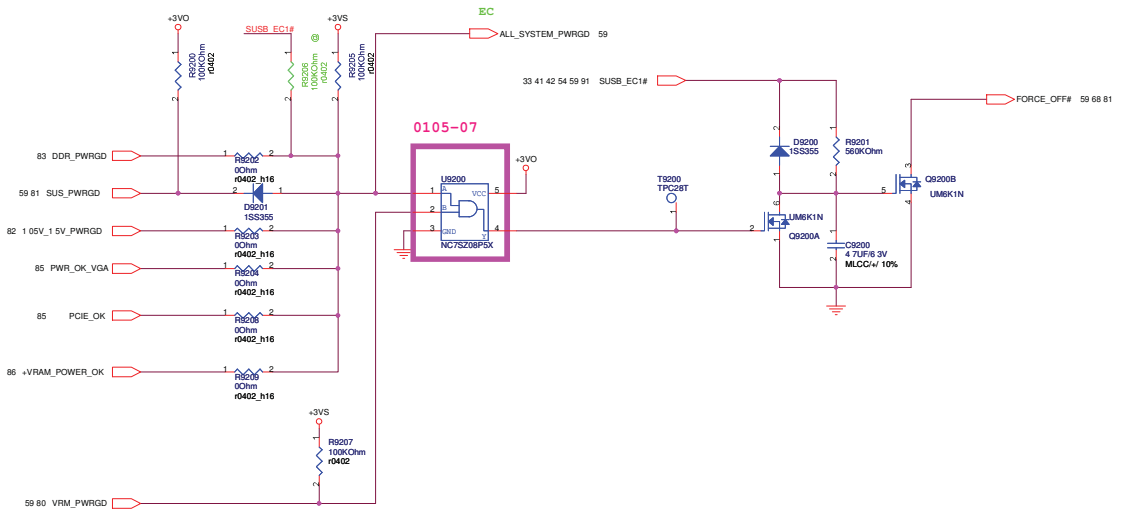
Engineer: Ray

Size	Project Name	Rev
Cus om	A7S	1 1

Date: 星期三 三月 21 2007 Sheet 90 of 95



POWER GOOD DETECTER



<Var ant Name>

ASUSTeK COMPUTER INC NB	Title : POWER_PROTECT
	Engineer: Ray
Size: Cus om	Project Name: A7S
Rev: 2 0	
Date: 星期三 三月 21 2007	Sheet 92 of 95

AC_BAT_SYS — AC_BAT_SYS 33 68 80 81 82 83 85 86 88
BAT — BAT 88
BAT_CON — BAT_CON 68 88

+2 5VREF — +2 5VREF 31 84 88 90

+3VA — +3VA 15 31 41 42 59 81 86
+5VAO — +5VAO 81 85 90
+5VO — +5VO 81 82 83 84 85 86 88 90 91
+5VSUS — +5VSUS 18 41 62 81
+5V — +5V 33 41 42 54 62 63 91
+5VS — +5VS 17 18 32 35 37 41 42 56 57 60 72 80 91
+3VO — +3VO 81 84 85 86 91 92
+3VSUS — +3VSUS 16 17 18 44 45 47 49 54 59 62 81
+3V — +3V 33 42 44 45 47 53 54 57 70 72 76 78 91
+3VS — +3VS 4 8 12 15 16 17 18 20 21 24 25 29 30 31 32 33 35 37 39 41 42 47 48 49 51 52 53 54 56 57 58 59 60 65 70 72 73 76 78 80 91 92
+3VSG — +3VSG

+12VSUS — +12VSUS 62 81 91
+12V — +12V 42 44 53 57 70 91
+12VS — +12VS 31 32 33 41 54 91

+1 8VO — +1 8VO 83 91
+1 8V — +1 8V 8 11 12 20 21 42 83
+1 8VS — +1 8VS 73 86 91
+0 9VS — +0 9VS
+0 9VO — +0 9VO 83

+1 05VO — +1 05VO 80 82
+VCCP — +VCCP 4 5 7 11 12 15 18 39 42 82
+1 5VO — +1 5VO 82 91
+1 5VS — +1 5VS 5 12 15 18 31 42 47 48 49 54 91

+2 5VO — +2 5VO 84 91
+2 5VS — +2 5VS 42 58 91

+VCORE — +VCORE 5 80

+VGA_VCORE — +VGA_VCORE 24 85

+VRAM — +VRAM 25 26 27 28 29 42 86 91
+1 2VSP — +1 2VSP 24 25 28 31 85 91
+1 25VS — +1 25VS 8 12 18 42 85

+3VM — +3VM
+3VM_CLK — +3VM_CLK
+1 25VM — +1 25VM
+1 05VM — +1 05VM
+1 5V — +1 5V 91
+0 9V — +0 9V 22 42 83

IAMT Only
Please delete if Non-IAMT

+1 5VSUS — +1 5VSUS 18 44 82
+2 5VSUS — +2 5VSUS 44 84

FOR POWER TEST

+3VA — JP9300 (SGL_JUMP) — CPU_VRON_PWR 80
+3VA — JP9301 (SGL_JUMP) — SUSB#_PWR — SUSB#_PWR 31 81 82 83 85 86 91
+3VA — JP9302 (SGL_JUMP) — SUSC#_PWR — SUSC#_PWR 62 83 91
+3VA — JP9303 (SGL_JUMP) — VSUS_ON — VSUS_ON 54 59 81 82

<Var ant Name>

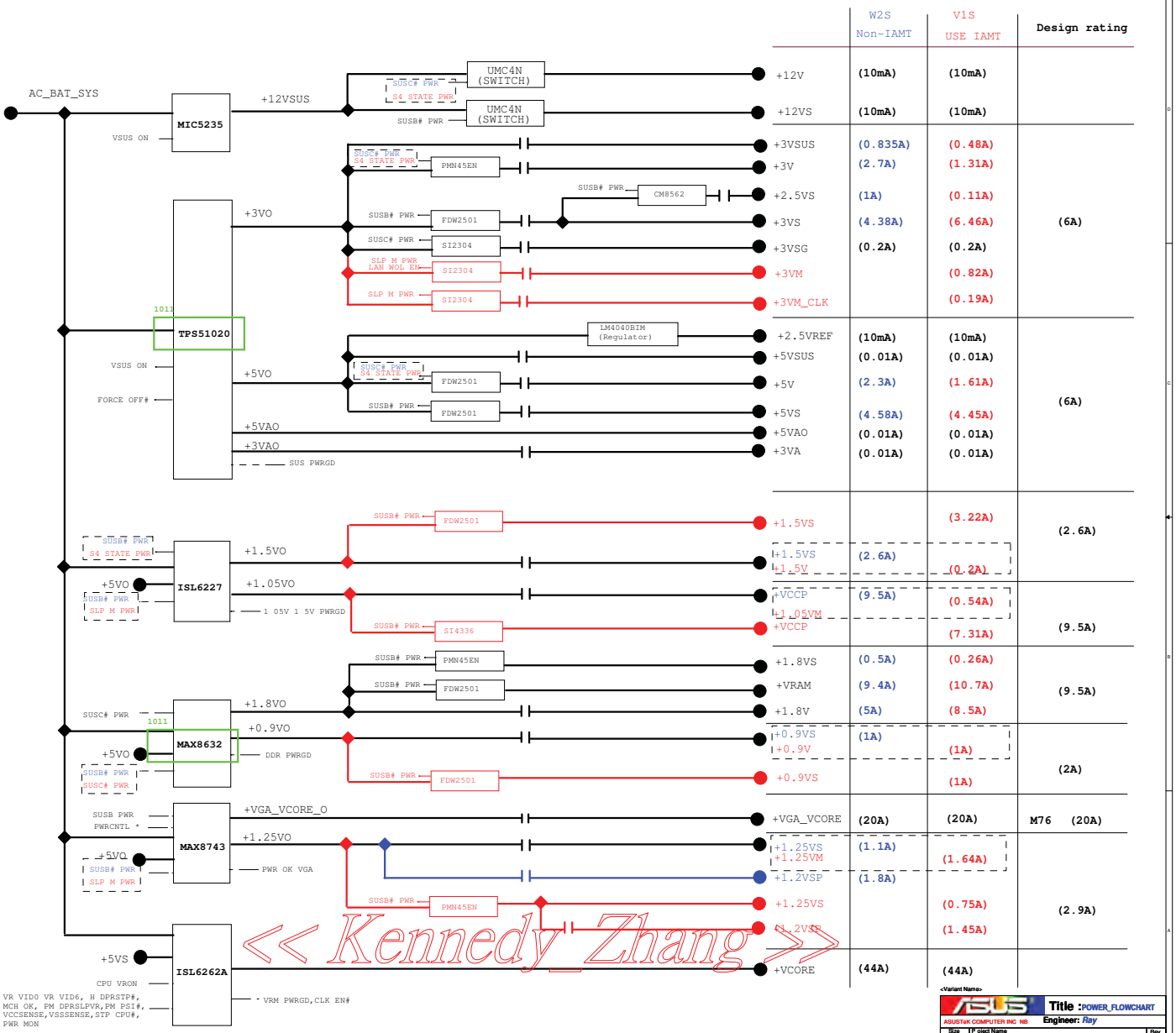
ASUSTeK COMPUTER INC NB

Title : POWER_SIGNAL
Engineer: Ray

Size	Project Name	Rev
Cus om	A7S	2 0

Date: 星期三 三月 21 2007 Sheet 93 of 95

<< Kennedy_Zhang >>



	W2S Non-IAMT	V1S USE IAMT	Design rating
+12V	(10mA)	(10mA)	
+12VS	(10mA)	(10mA)	
+3VSUS	(0.835A)	(0.48A)	
+3V	(2.7A)	(1.31A)	
+2.5VS	(1A)	(0.11A)	
+3VS	(4.38A)	(6.46A)	(6A)
+3VSG	(0.2A)	(0.2A)	
+3VM		(0.82A)	
+3VM_CLK		(0.19A)	
+2.5VREF	(10mA)	(10mA)	
+5VSUS	(0.01A)	(0.01A)	
+5V	(2.3A)	(1.61A)	
+5VS	(4.58A)	(4.45A)	(6A)
+5VAO	(0.01A)	(0.01A)	
+3VA	(0.01A)	(0.01A)	
+1.5VS		(3.22A)	(2.6A)
+1.5VS	(2.6A)		
+1.5V		(0.2A)	
+VCCP	(9.5A)	(0.54A)	
+1.05VM			(9.5A)
+VCCP		(7.31A)	
+1.8VS	(0.5A)	(0.26A)	
+VRAM	(9.4A)	(10.7A)	(9.5A)
+1.8V	(5A)	(8.5A)	
+0.9VS	(1A)		
+0.9V		(1A)	(2A)
+0.9VS		(1A)	
+VGA_VCORE	(20A)	(20A)	M76 (20A)
+1.25VS	(1.1A)		
+1.25VM		(1.64A)	
+1.2VSP	(1.8A)		
+1.25VS		(0.75A)	(2.9A)
+1.2VSP		(1.45A)	
+VCORE	(44A)	(44A)	

<Variant Name>

ASUSTeK COMPUTER INC NB

Title : POWER_FLOWCHART

Engineer: Ray

Size: Custom | Project Name: A7S | Rev: 2.0

Date: 月 日, 一 21 2007 | Sheet 94 of 95

Rev	Date	Description
1.0	10/04/05	1. Initial release.
1.1	12/26/05	1. Remove CardReader PME schemaic for R5C832 CardReader.[16,49] 2. Change X6 32.768MHz source.[59] 3. Remove FAN control schematic of the 3PIN.[37] 4. Remove EC control pin for Fan control schmatic.[59] 5. Delete VGA Thermal OTEMP# 0 ohm resistor .[37] 6. Unmount USB 47uF for dual USB connector .[62] 7. Delete REAR_R & REAR_L 1uF and 220 ohm.[56] 8. Add 4 pcs 10uF (0805) for +VRAM.[28] 9. Change TPLED_ON GPIO pin from GPIO19 to GPIO14 and 10K ohm pull low.[17,66] 10. Change LAN, CRT, DVI,USB, SVIDEO, SATA, PATA, DC, BAT, NewCard, MIC connector. [45,32,35,62,35,72,72,68,68,52,57] 11. USB Schematic modify.[62] 12. Delete U38 BIOS Socket.[64] 13. PCB_ID from 000 change to 001.[17] 14. Reverse RN28 pin definition.[70] 15. CLK_TPMPCI termination resistor from 33 Ohm to 22 Ohm.[39] 16. Add Pre-Amplifier MIC circuit.[56,57] 17. Add H3,H4 NUT for FAN and modify screw hole H17, H20.[37,74] 18. Modify ACZ__BCLK_CODEC R407 & ACZ_BCLK_MOD R351 termination resistor.change to 22 OHM and mount 22pF capacitor C482 & C575[15,45,56] 19. Modify SDWP net name.[50,51] 20. Add SD/MSCLK C641 10pF/50V.[51] 21. Ear output from FRONT R/L OUT change to SURR_OUT_R/L.[56,57] 22. Unmount C608 U32 Amplifier PC-BEEP capacitor.[57] 23. Add C885 LAN_GND capacitor for EMI request.[45] 24. Modify C676 & C677 1000pF/3KV capacitor for EMI request.[45] 25. Modify L121~L124 220 Ohm bead for EMI request.[57] 26. Modify RN55 0 Ohm for inverter signal.[33] 27. Modify CPU & VGA screw hole H39,H40,H43,H44,H47,H48,H51.[74]

Rev	Date	Description

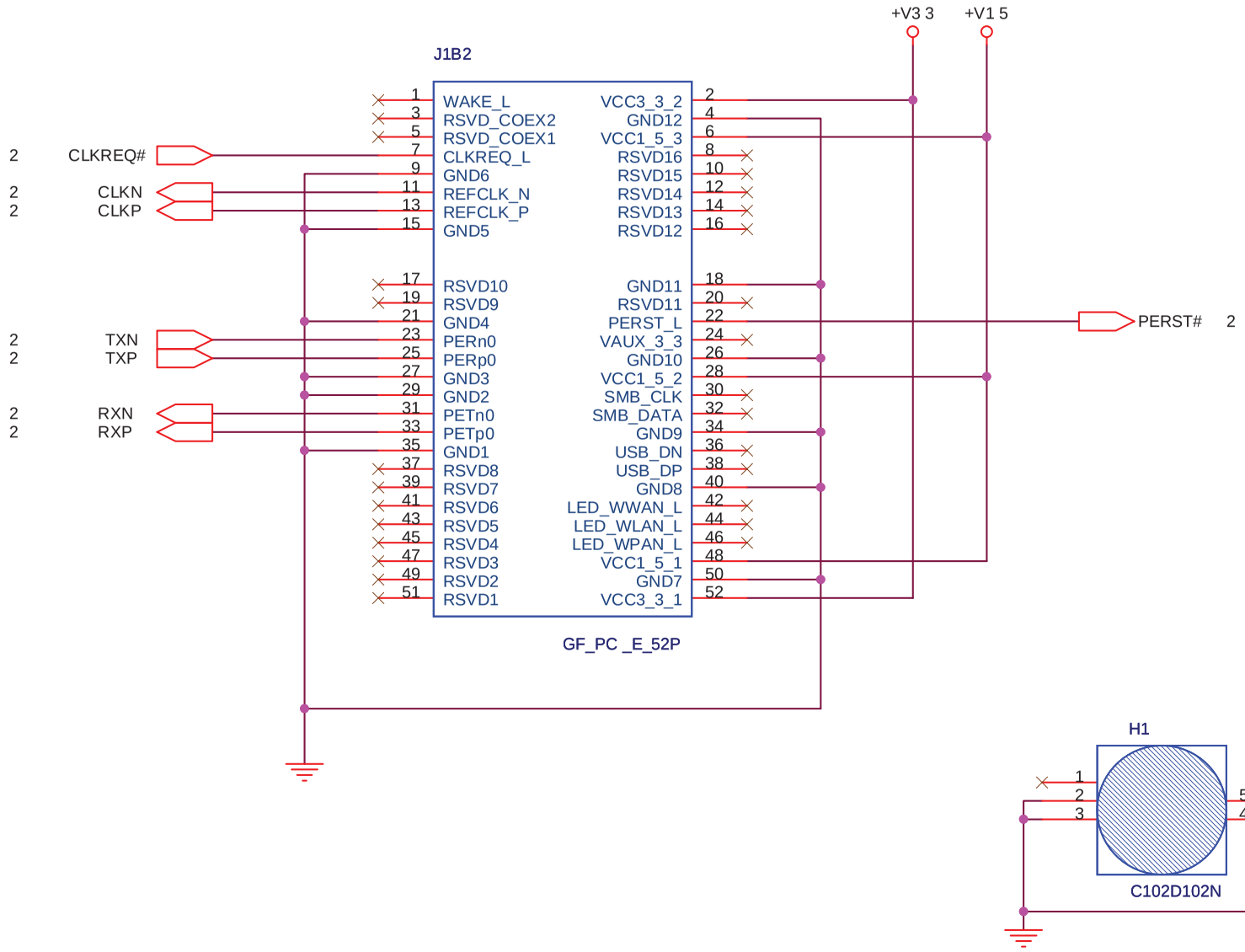
ASUSTek COMPUTER INC

Title : History

Engineer: Ray

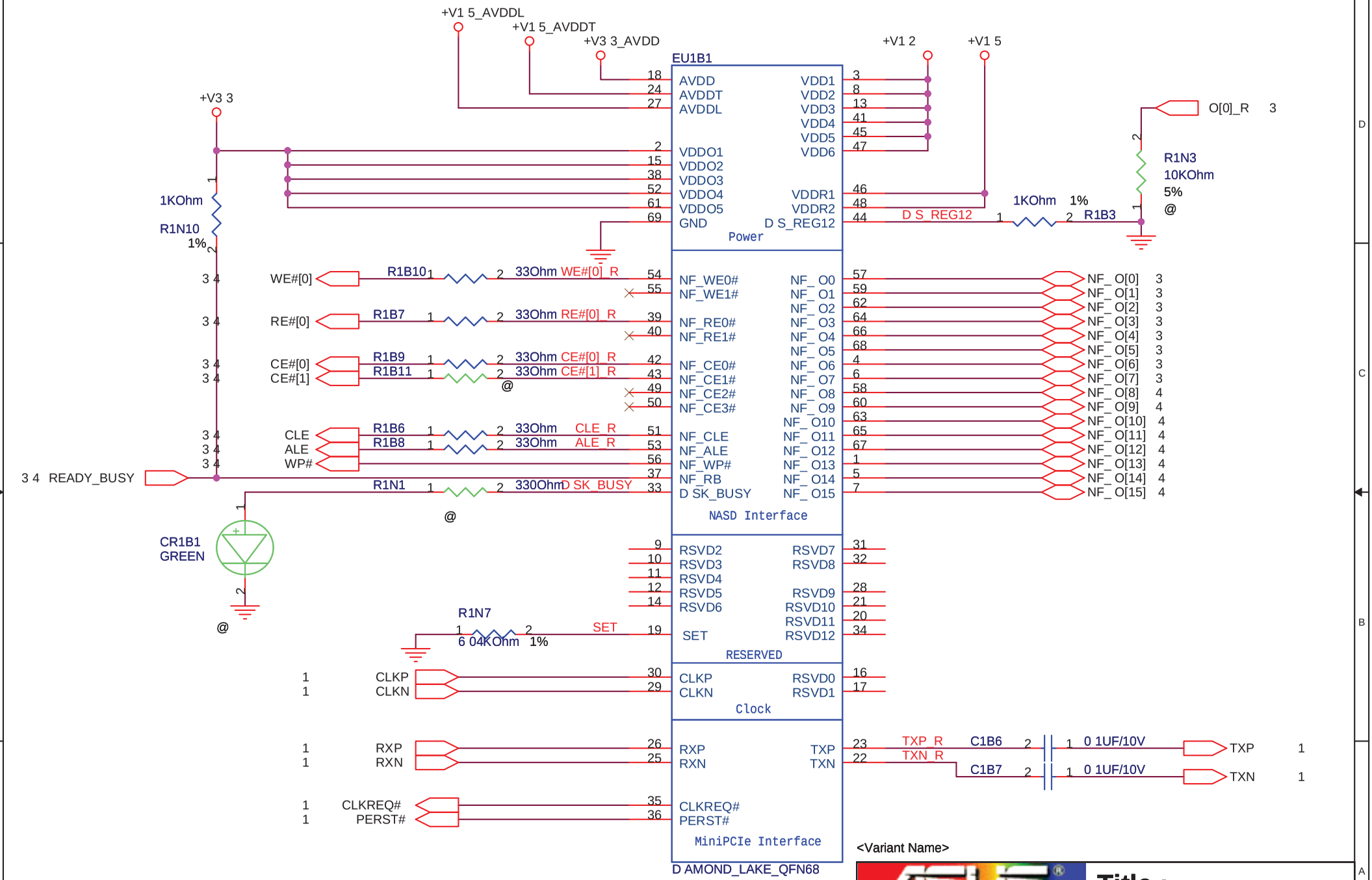
Size	Project Name	Rev
Cus om	A7S	1 1

Date: 星期二, 一月 21, 2007 Sheet 95 of 95



<Variant Name>

ASUSTeK COMPUTER NC NB1	Title : MINI CARD GF	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 1 0
Date: Thursday May 17 2007	Sheet 1 of 5	


+V1 5_AVDDL
+V1 5_AVDDT
+V3 3_AVDD
+V3 3
+V1 2
+V1 5
EU1B1
AVDD
AVDDT
AVDDL
VDDO1
VDDO2
VDDO3
VDDO4
VDDO5
GND
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDDR1
VDDR2
D S_REG12
Power
1KOhm
R1N10
1%
D S_REG12
1KOhm 1%
R1B3
R1N3
10KOhm
5%
@
O[0]_R 3
WE#[0]
R1B10 33Ohm WE#[0]_R
RE#[0]
R1B7 33Ohm RE#[0]_R
CE#[0]
CE#[1]
R1B9 33Ohm CE#[0]_R
R1B11 33Ohm CE#[1]_R
CLE
ALE
WP#
R1B6 33Ohm CLE_R
R1B8 33Ohm ALE_R
3 4 READY_BUSY
R1N1 330Ohm D SK_BUSY
NF_WE0#
NF_WE1#
NF_RE0#
NF_RE1#
NF_CE0#
NF_CE1#
NF_CE2#
NF_CE3#
NF_CLE
NF_ALE
NF_WP#
NF_RB
D SK_BUSY
NF_ O0
NF_ O1
NF_ O2
NF_ O3
NF_ O4
NF_ O5
NF_ O6
NF_ O7
NF_ O8
NF_ O9
NF_ O10
NF_ O11
NF_ O12
NF_ O13
NF_ O14
NF_ O15
NF_ O[0] 3
NF_ O[1] 3
NF_ O[2] 3
NF_ O[3] 3
NF_ O[4] 3
NF_ O[5] 3
NF_ O[6] 3
NF_ O[7] 3
NF_ O[8] 4
NF_ O[9] 4
NF_ O[10] 4
NF_ O[11] 4
NF_ O[12] 4
NF_ O[13] 4
NF_ O[14] 4
NF_ O[15] 4
NASD Interface
CR1B1
GREEN
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
SET
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
R1N7
6 04KOhm 1%
SET
RESERVED
CLKP
CLKN
RSVD0
RSVD1
Clock
RXP
RXN
TXP
TXN
TXP_R
TXN_R
C1B6 0 1UF/10V
C1B7 0 1UF/10V
TXP 1
TXN 1
CLKREQ#
PERST#
MiniPCIe Interface
D AMOND_LAKE_QFN68
<Variant Name>
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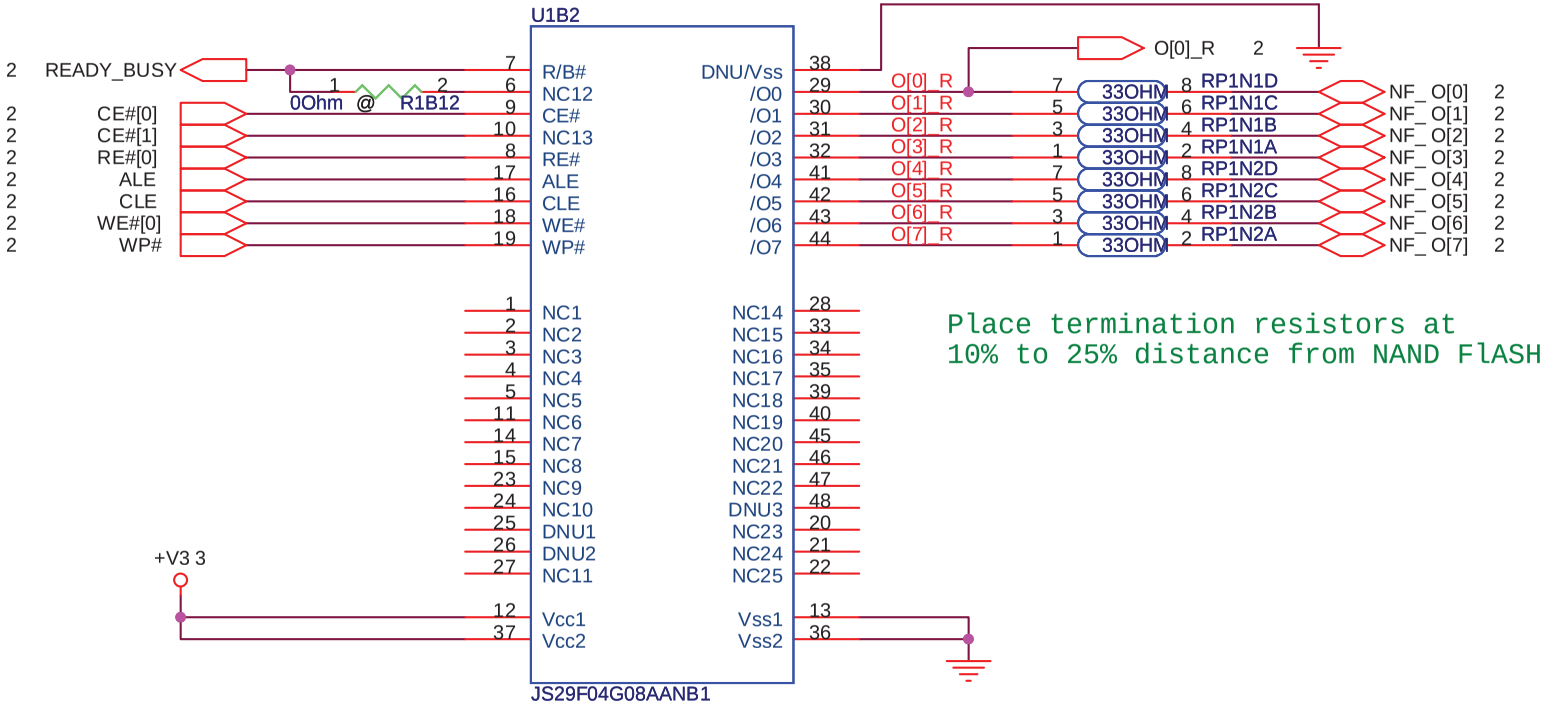
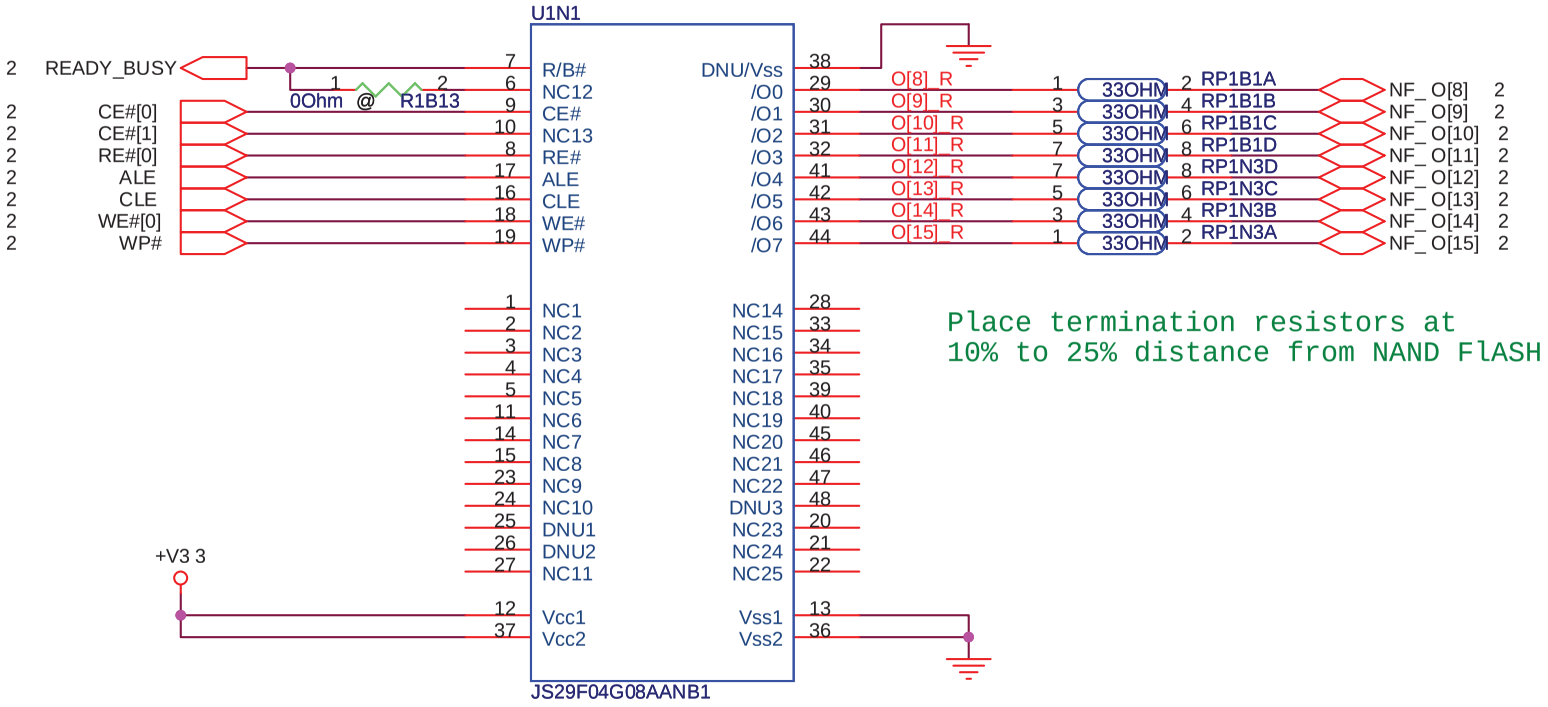
ASUSTeK COMPUTER NC NB1
Engineer: Mark_Lin
Size A
Project Name Robson
Rev 1 0
Date Friday May 18 2007
Sheet 2 of 5



<Variant Name>

ASUSTeK COMPUTER NC NB1	Title : NAND FLASH #1	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 1 0
Date: Thursday May 17 2007	Sheet 3 of 5	

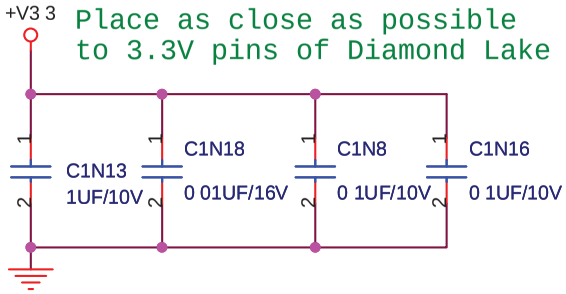


Place termination resistors at
10% to 25% distance from NAND FlASH

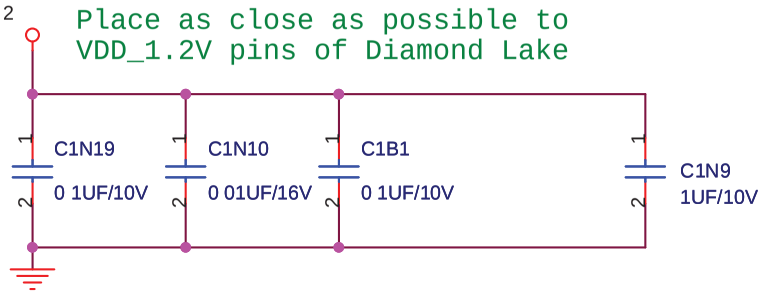
<Variant Name>

ASUSTeK COMPUTER NC NB1	Title : NAND FLASH #2	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 1 0
Date: Thursday May 17 2007	Sheet 4 of 5	

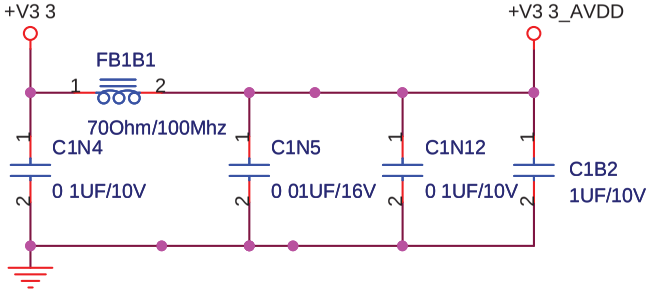
Place as close as possible to 3.3V pins of Diamond Lake



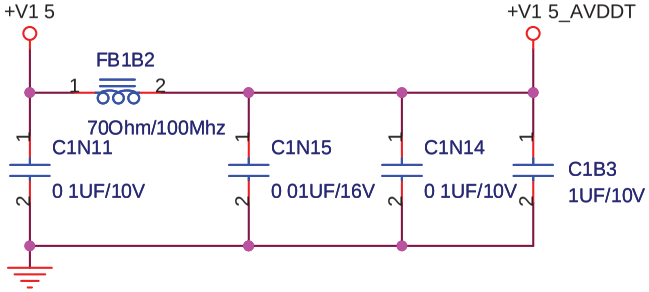
Place as close as possible to VDD_1.2V pins of Diamond Lake



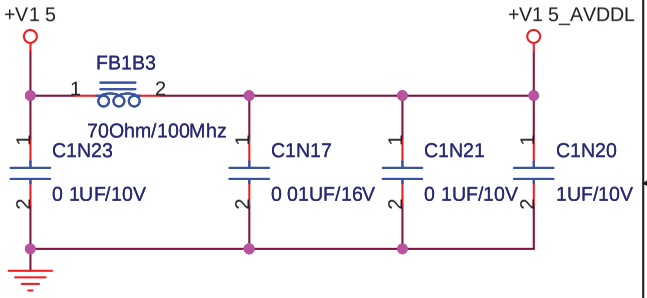
Place as close as possible to AVDD pins of Diamond Lake

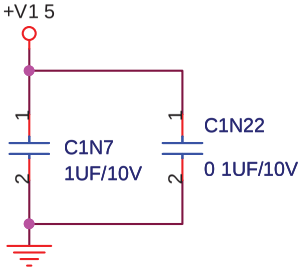


Place as close as possible to AVDDT pins of Diamond Lake

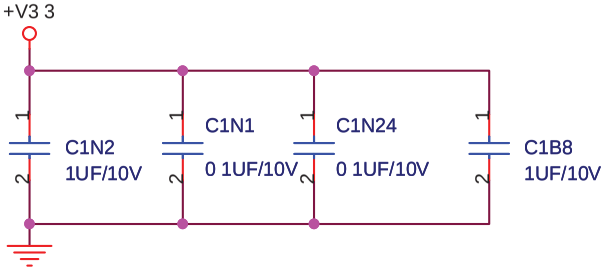


Place as close as possible to AVDDL pins of Diamond Lake





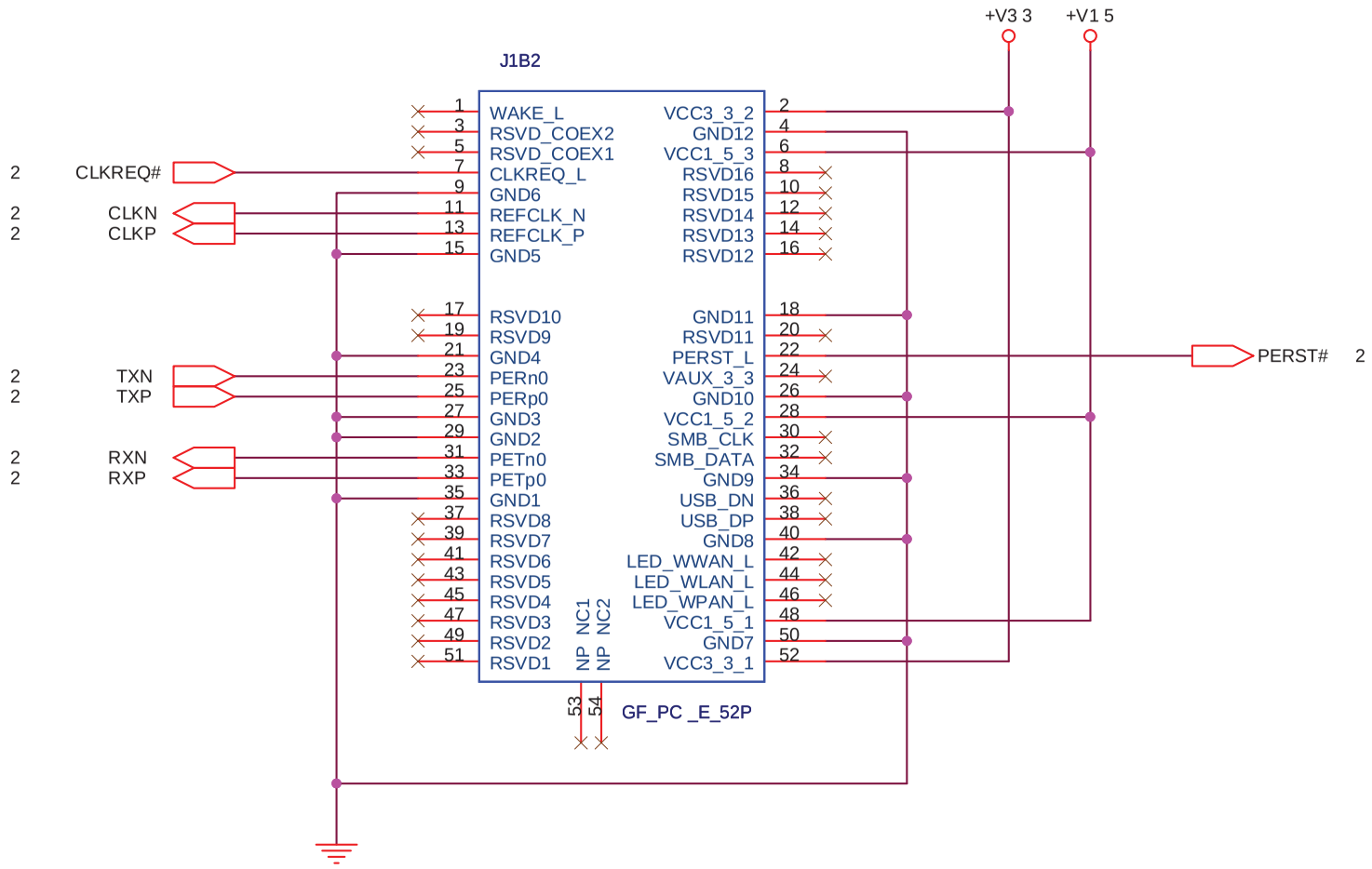
Place as close as possible to VDDR1 and VDDR2 pins of Diamond Lake



Place as close as possible to 3.3V pins of Nand Flash

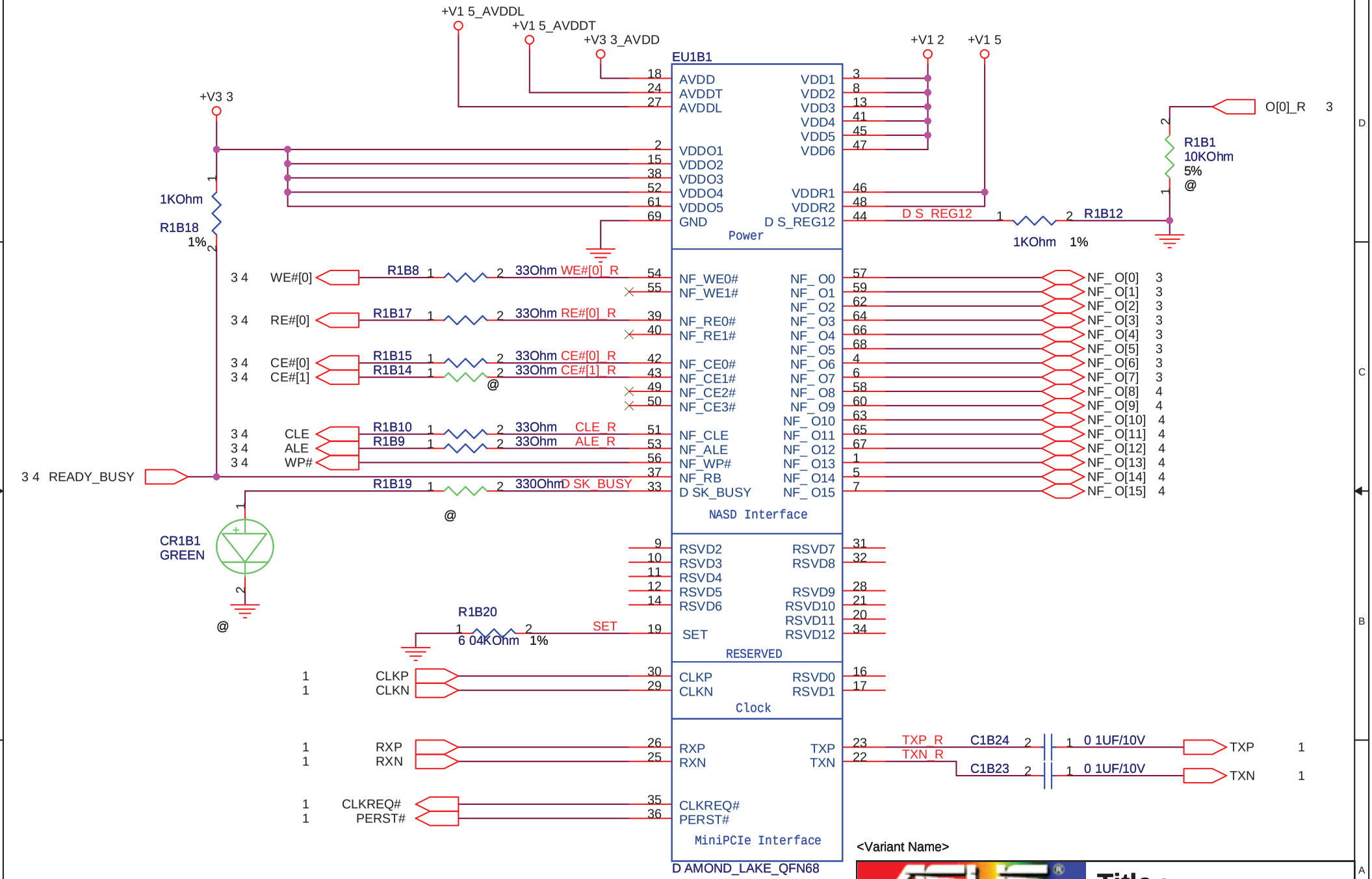
<Variant Name>

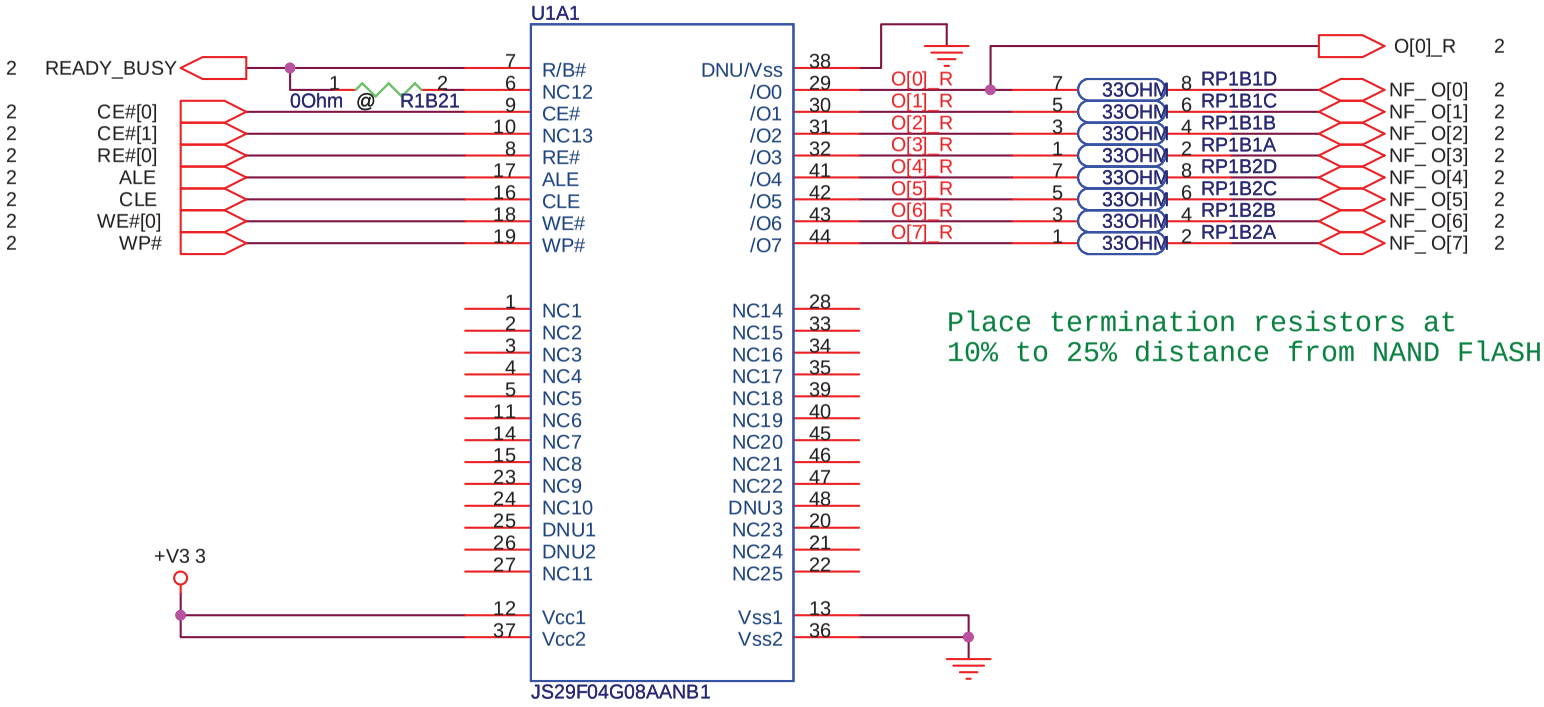
ASUSTeK COMPUTER NC NB1	Title : POWER AND DECOUPLING	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 1 0
Date: Thursday May 17 2007	Sheet 5 of 5	



<Variant Name>

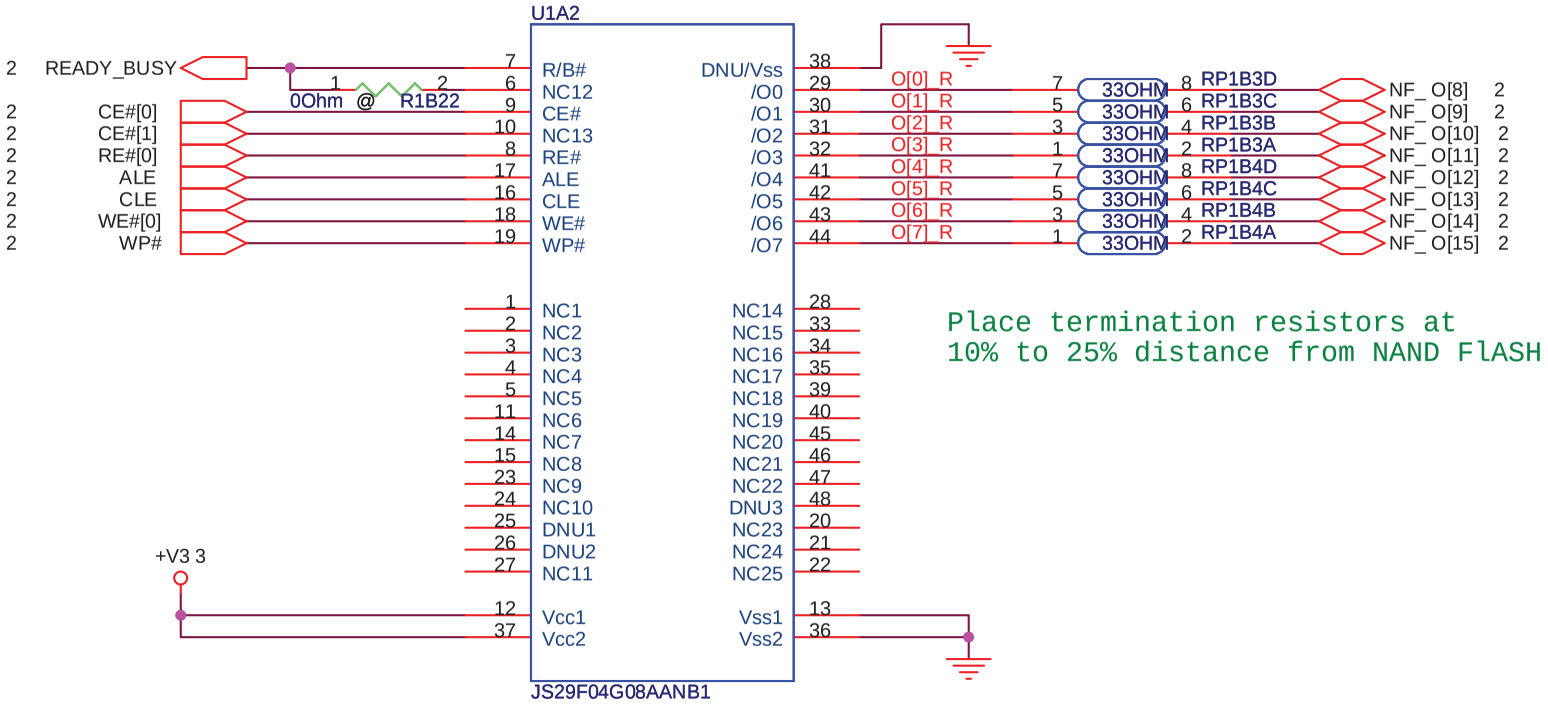
ASUSTeK COMPUTER NC NB1	Title : MINI CARD GF	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 2 0
Date: Thursday May 17 2007	Sheet 1 of 5	


+V1 5_AVDDL
+V1 5_AVDDT
+V3 3_AVDD
+V3 3
+V1 2
+V1 5
EU1B1
AVDD
AVDDT
AVDDL
VDDO1
VDDO2
VDDO3
VDDO4
VDDO5
GND
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDDR1
VDDR2
D S_REG12
Power
1KOhm
R1B18
1%
D S_REG12
R1B12
1KOhm 1%
R1B1
10KOhm
5%
O[0]_R
WE#[0]
RE#[0]
CE#[0]
CE#[1]
CLE
ALE
WP#
READY_BUSY
R1B8 33Ohm WE#[0]_R
R1B17 33Ohm RE#[0]_R
R1B15 33Ohm CE#[0]_R
R1B14 33Ohm CE#[1]_R
R1B10 33Ohm CLE_R
R1B9 33Ohm ALE_R
R1B19 330Ohm D SK_BUSY
NF_WE0#
NF_WE1#
NF_RE0#
NF_RE1#
NF_CE0#
NF_CE1#
NF_CE2#
NF_CE3#
NF_CLE
NF_ALE
NF_WP#
NF_RB
D SK_BUSY
NF_ O0
NF_ O1
NF_ O2
NF_ O3
NF_ O4
NF_ O5
NF_ O6
NF_ O7
NF_ O8
NF_ O9
NF_ O10
NF_ O11
NF_ O12
NF_ O13
NF_ O14
NF_ O15
NF_ O[0]
NF_ O[1]
NF_ O[2]
NF_ O[3]
NF_ O[4]
NF_ O[5]
NF_ O[6]
NF_ O[7]
NF_ O[8]
NF_ O[9]
NF_ O[10]
NF_ O[11]
NF_ O[12]
NF_ O[13]
NF_ O[14]
NF_ O[15]
NASD Interface
CR1B1
GREEN
R1B20
6 04KOhm 1%
SET
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
SET
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD0
RSVD1
RESERVED
CLKP
CLKN
Clock
RXP
RXN
TXP
TXN
TXP_R
TXN_R
C1B24 0 1UF/10V
C1B23 0 1UF/10V
CLKREQ#
PERST#
MiniPCIe Interface
D AMOND_LAKE_QFN68
<Variant Name>
Title : DIAMOND LAKE
ASUSTeK COMPUTER NC NB1
Engineer: Mark_Lin
Size A
Project Name Robson
Rev 2 0
Date Friday May 18 2007
Sheet 2 of 5



<Variant Name>

ASUSTeK COMPUTER NC NB1	Title : NAND FLASH #1	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 2 0
Date: Thursday May 17 2007	Sheet 3 of 5	

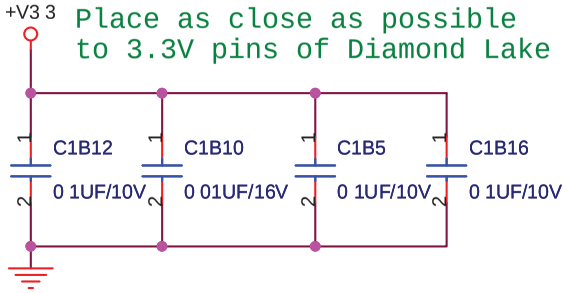


Place termination resistors at
10% to 25% distance from NAND FlASH

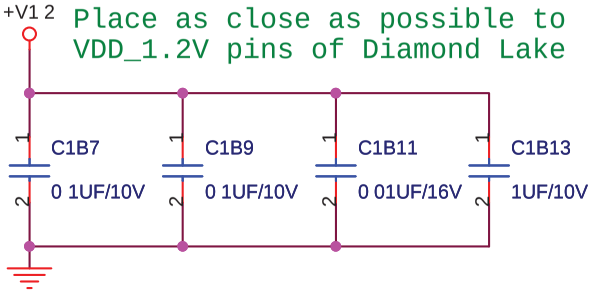
<Variant Name>

ASUSTeK COMPUTER NC NB1	Title : NAND FLASH #2	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 2 0
Date: Thursday May 17 2007	Sheet 4 of 5	

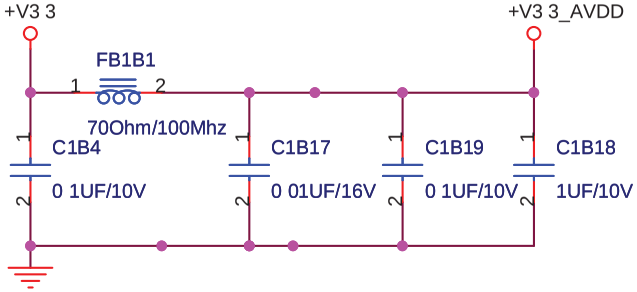
Place as close as possible to 3.3V pins of Diamond Lake



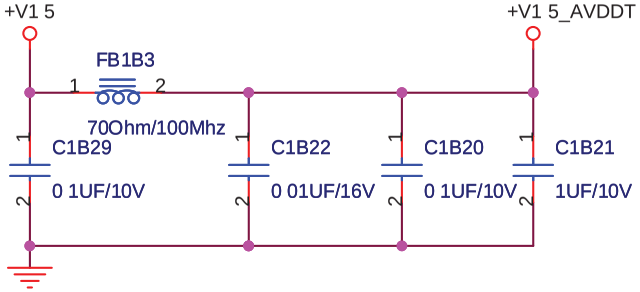
Place as close as possible to VDD_1.2V pins of Diamond Lake



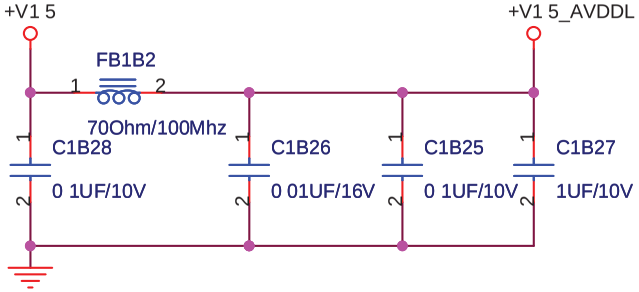
Place as close as possible to AVDD pins of Diamond Lake

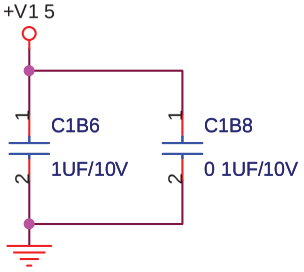


Place as close as possible to AVDDT pins of Diamond Lake

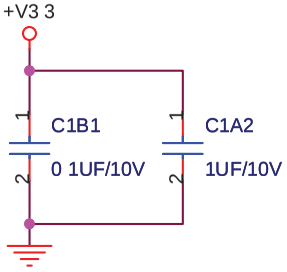


Place as close as possible to AVDDL pins of Diamond Lake

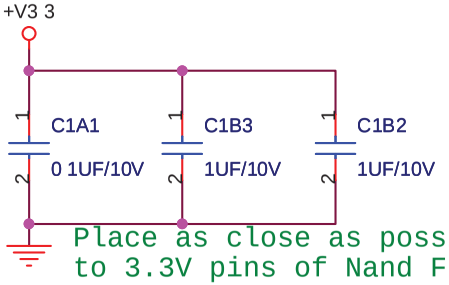




Place as close as possible to VDDR1 and VDDR2 pins of Diamond Lake



Place as close as possible to 3.3V pins of Nand Flash1



Place as close as possible to 3.3V pins of Nand Flash2

<Variant Name>

ASUSTeK COMPUTER NC NB1	Title : POWER AND DECOUPLING	
	Engineer: Mark_Lin	
Size: A	Project Name: Robson	Rev: 2 0
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