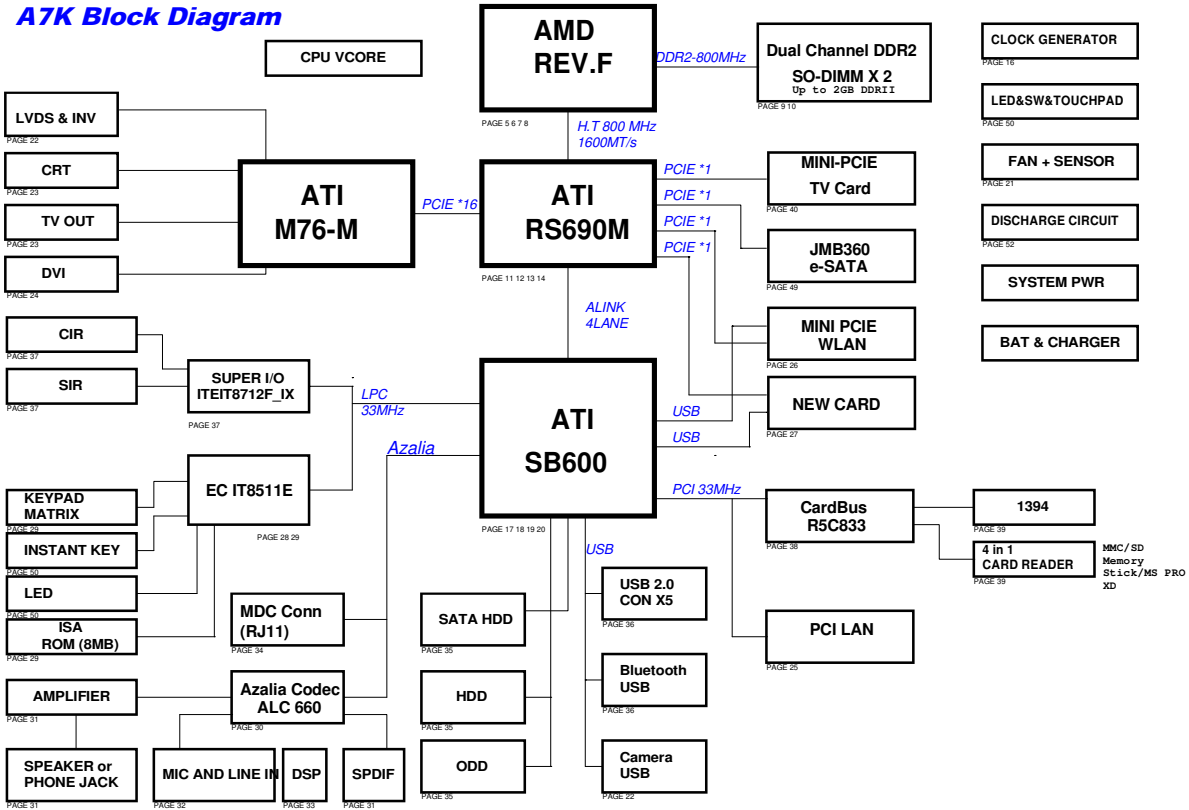
A7K Block Diagram



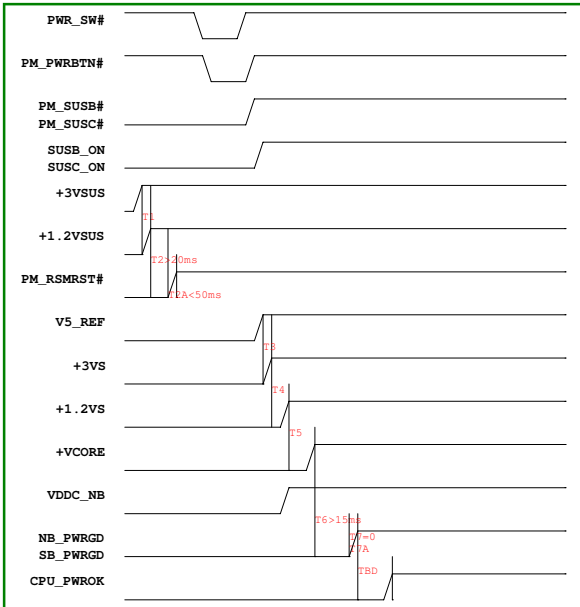
ASUSTECH CO LTD		Title :	A7K
		Engineer:	Endy Zhang
Size: Custom	Project Name: Block Diagram		Rev: 2.0
Date: 星期四 六月 14 2007		Sheet 1 of 69	

PCI DEVICES IRQ TABLE

DEVICE	IDSEL#	REQ/GNT#	PCI INT	CLOCK
NB VGA	N/A	N/A	A	
SB	AD31(INT)	N/A	N/A	
ATA100	AD31	N/A	A	INT
AC97/AZALIA	AD31	N/A	B	INT
USB	AD30	N/A	D	INT
CARD BUS	AD17	0	F,G	PCI_CLK0
PCI LAN	AD18	1	E	PCI_CLK1

SMBUS TABLE

SOURCE	SIGNAL NAME	LINKED DEVICES
NB	DAC_SCL/DAC_SDAT	CRT/LVDS
	I2C_CLK/I2C_DATA	LVDS
	I2C_CLK/DDC_DATA	DVI
SB	SCLK0/SDATA0	SO-DIMMs/CLK_GEN/DSP
	SCLK1/SDATA1	MINI-PCIE(WLAN)/NEW CARD/MINI-PCIE(TV)
EC	SMCLK0/SMDAT0	BATTERY
	SMCLK1/SMDAT1	THERMAL(CPU:98H GPU:4CH)



GPIO

NB	STRP_DATA	SEL_VCC_NB	TUNE NB VOLTAGE	OUTPUT
SB	RI#EXTEVNT0#	KB_SCI#	KEYBOARD SCI	INPUT
	LPC_PME#/GEVENT3#	LPC_PME#	PME FROM SIO	INPUT
	LPC_SMI#/EXTEVNT1#	LPC_SMI#	SMI FROM EC	INPUT
	WAKE#/GEVENT8#	SB_WAKE#	PCI E WAKE	INPUT
	GPIO10	BT_DET#	BLUETOOTH DETECT	INPUT
	GPIO6	BT_LED_EN#	BLUETOOTH LED	OUTPUT
	GPO4	802_LED_EN#	WIRELESS LAN LED	OUTPUT
	GPIO5	CB_HWSUSPEND	CARDBUS SUPEND	OUTPUT
	GPIO8	BT_ON#	BLUETOOTH ENABLE(OPTION)	OUTPUT
	GPIO0	WLAN_ON#	WIRELESS LAN ENABLE	OUTPUT
	LLB#/GPIO66	BAT_LL#	BATTERY LOW(OPTION)	INPUT
	TEMPIN0	CPU_THRM	CPU TEMPERATURE(OPTION)	
	TEMPIN1	NB_THERM	NB TEMPERATURE	
	GPIO11	SB_THRO_CPU	CPU OVER TEMP AND SHUT	OUTPUT
	GPIO12	TV_ON#	TV ENABLE	OUTPUT
	GPIO64	PM_THERM#	THERM ALERT FROM EC	INPUT
EC	ECSMI#/GPM0	EXSMI#	SMI TO SB	OUTPUT
	ECSCI#/GPD3	EXT_SCI#	SCI TO SB	OUTPUT
	SM0	SM_BAT	SMBUS TO BATTERY	
	SM1	SMB1	SMBUS TO THERMAL	
	ADC0/GPK0	BATO_AD	BATTERY VOLTAGE	INPUT
	ADC2/GPK2	AC_AD	AC ADAPTER VOLTAGE	INPUT
	GPK4	KID0	KEYBOARD ID0	INPUT
	GPK5	KID1	KEYBOARD ID1	INPUT
	DAC0/GPJ0	FAN_DA	FAN CONTROL(OPTION)	OUTPUT
	DAC2/GPJ2	BRIGHT_PWM	LCD BRIGHT CONTROL	OUTPUT
	GPJ3	BATSEL_2P#	2P BATTERY	INPUT
	PWM1/GPA1	FAN_PWM	FAN CONTROL	OUTPUT
	GPA4	CHG_LED_UP#	CHARGE LED	OUTPUT
	GPA5	PWR_LED_UP#	POWER LED	OUTPUT
	GPA6	BATSEL_3S#	3S BATTERY	INPUT
	GPA7	BACK_OFF#	LCD BACK OFF	OUTPUT
	GPB0	NUM_LED	NUM LOCK LED	OUTPUT
	GPB1	CAP_LED	CAP LOCK LED	OUTPUT
	GPB7	THRO_CPU	CPU OVER TEMP AND SHUT	OUTPUT
	GPC0	DJ_LED#	AUDIO DJ LED	OUTPUT
	GPC3	EMAIL_LED#	EMAIL LED	OUTPUT
	GPC4	ACIN_OC#	ADAPTER IN	INPUT
	GPC5	OP_SD#	AUDIO SHUTDOWN	OUTPUT
	GPC6	BAT_IN_OC#	BATTERY IN	INPUT
	GPC7	EC_IDE_RST#	EC CONTROL IDE RST	OUTPUT
	RI1#/WUI0/GPD0	PM_SUSB#	SB SUSB# IN	INPUT
	RI2#/WUI1/GPD1	PM_SUSC#	SB SUSC# IN	INPUT
	GPD4	RF_OFF_SW#	RF SWITCH OFF	INPUT
	GPD6	FAN2_TACH	FAN TACH	INPUT
	GPE0	EMAIL_SW#	EMAIL SWITCH	INPUT
	GPE1	NTERNET#	INTERNET SWITCH	INPUT
	GPE2	MARATHON#	POWER GEAR	INPUT
	GPE3	DISTP_SW#	DISABLE TOUCHPAD	INPUT
	PWRSE/GPE4	PWRSW#_EC	POWER SWITCH	INPUT
	GPE6	LID_EC#	LID STATUS IN	INPUT
	GPE7	BT_ON#	BLUETOOTH ENABLE	OUTPUT
	PS2CLK2/GPF4	TPAD_CLK	TOUCHPAD CLK	
	PS2DAT2/GPF5	TPAD_DAT	TOUCHPAD DATA	
	GPF6	PWRLMT#	POWER LIMIT	OUTPUT
	GPF7	DJSW#	DJ SWITCH	INPUT
	GPG4	THRM_CPU	ALERT FROM THERMAL IC	INPUT
	GPG6	PMTHERM#	THERM ALERT TO SB	OUTPUT
	GPG7	AC_APR_UC#	ADAPTER POWER OK	INPUT
	GPH0	VSUS_ON	ENABLE VSUS POWER	OUTPUT
	GPH1	VSUS_GD_EC#	VSUS OK	INPUT
	GPH2	MVPOK#	CPU POWER OK	INPUT
	GPH3	PM_PWRBTN#	PWRBTN TO SB	OUTPUT
	GPH4	SUSC_ON	SUSC ON	OUTPUT
	GPH5	SUSB_ON	SUSB_ON	OUTPUT
	GPH6	CPU_VRON	ENABLE VCORE	OUTPUT
	GPH7	PM_RSMRST#	SB RSUMRESET	OUTPUT
	GPI1	WATCH_DOG#	WATCH_DOG CONTROL FAN	OUTPUT
	GPI3	CHG_EN#	ENABLE CHARGE	OUTPUT
	GPI4	PRECHG	BATTERY PRECHARGE	OUTPUT
	GPI5	BAT_LL#	BATTERY LOW	OUTPUT
	GPI6	BAT_LEARN	BATTERY LEARN	OUTPUT
SIO	PME#	LCP_PME#	PME TO SB	OUTPUT

ASUSTECH CO LTD

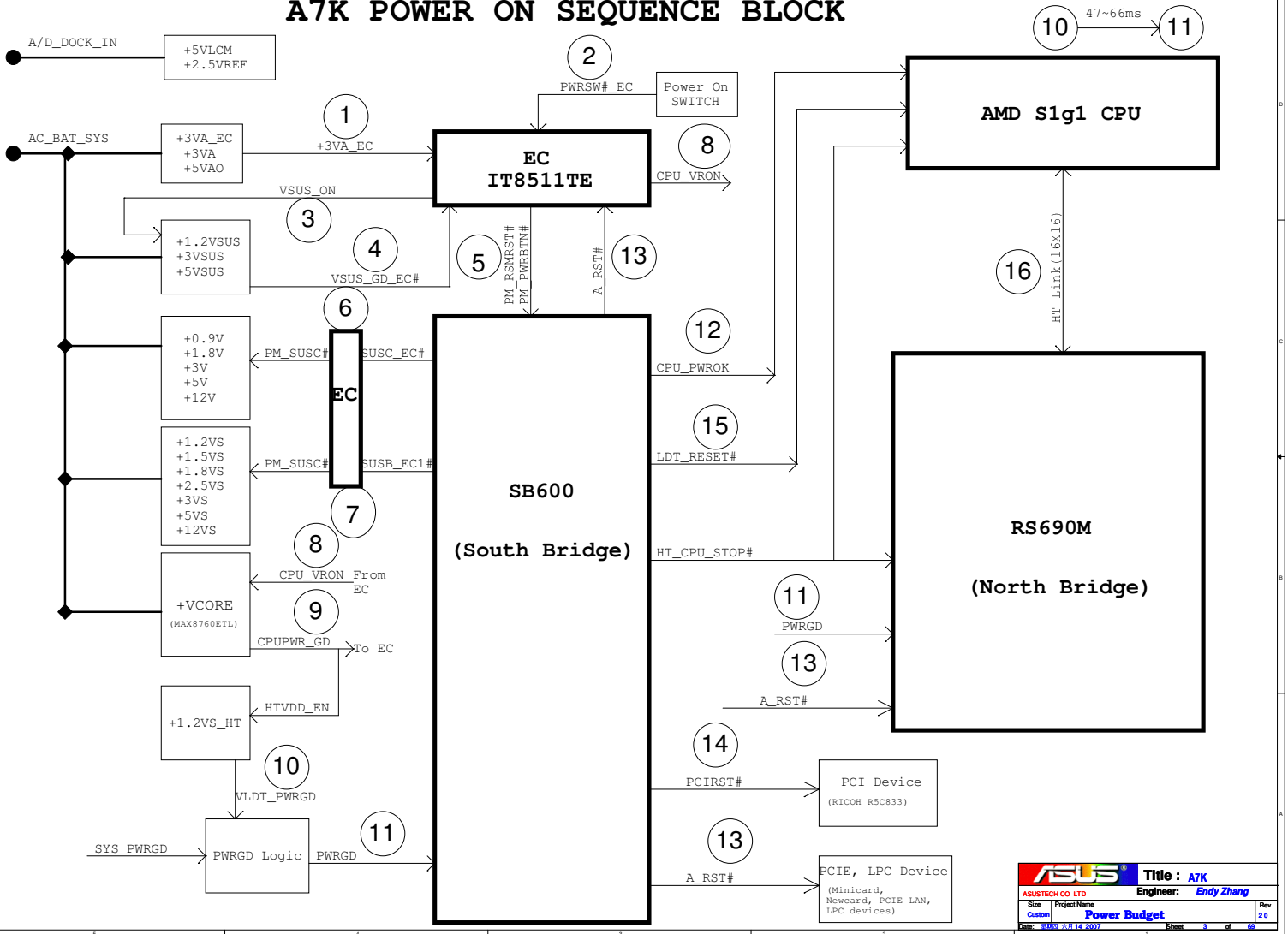
Title : A7K

Engineer: Endy Zhang

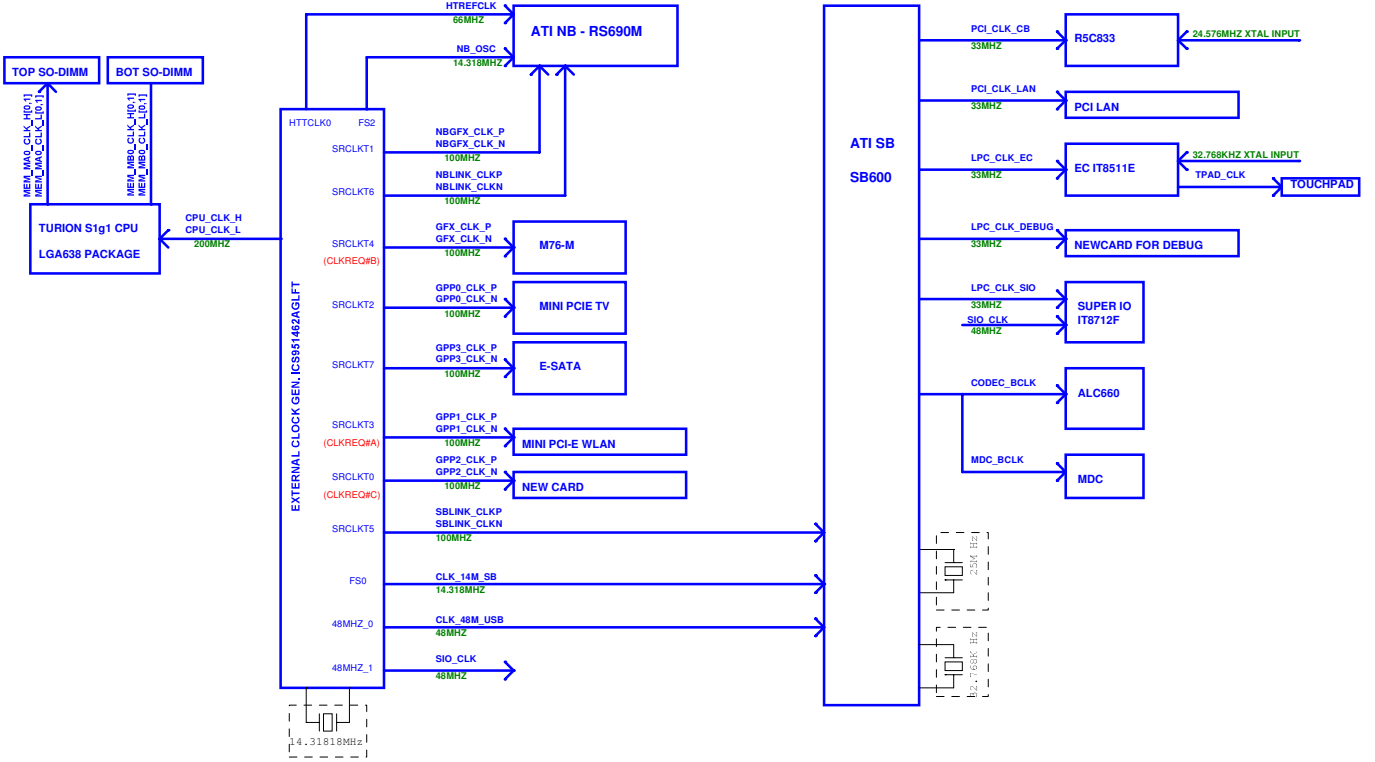
Size: Custom | Project Name: Table of Contents | Rev: 2.0

Date: 星期一 六月 11, 2007 | Sheet 2 of 69

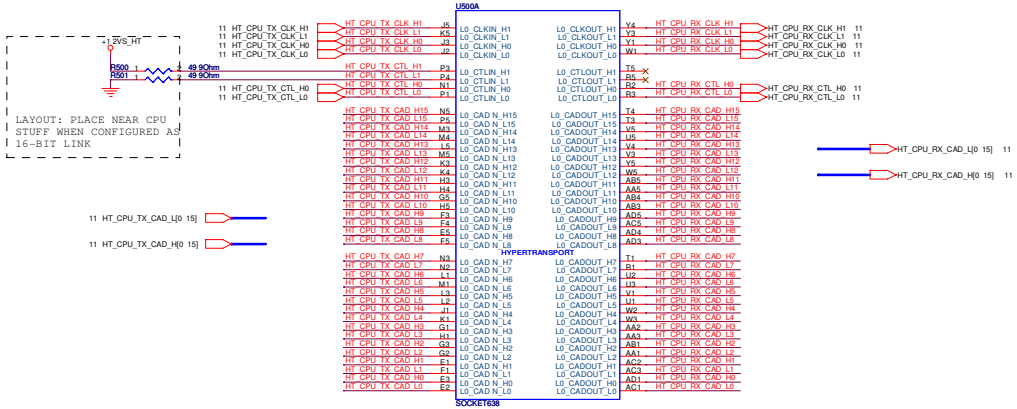
A7K POWER ON SEQUENCE BLOCK



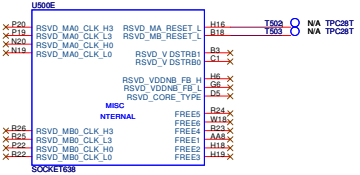
ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: Power Budget		Rev: 2.0
Date: 星期四 六月 14 2007		Sheet 3 of 69	

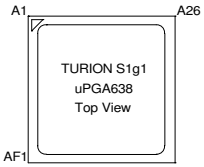


ASUSTECH CO LTD	Title : A7K	
	Engineer: Endy Zhang	
Size: Custom	Project Name: Clock Distribution	Rev: 2.0
Date: 星期四 十月 11, 2007	Sheet 4 of 69	

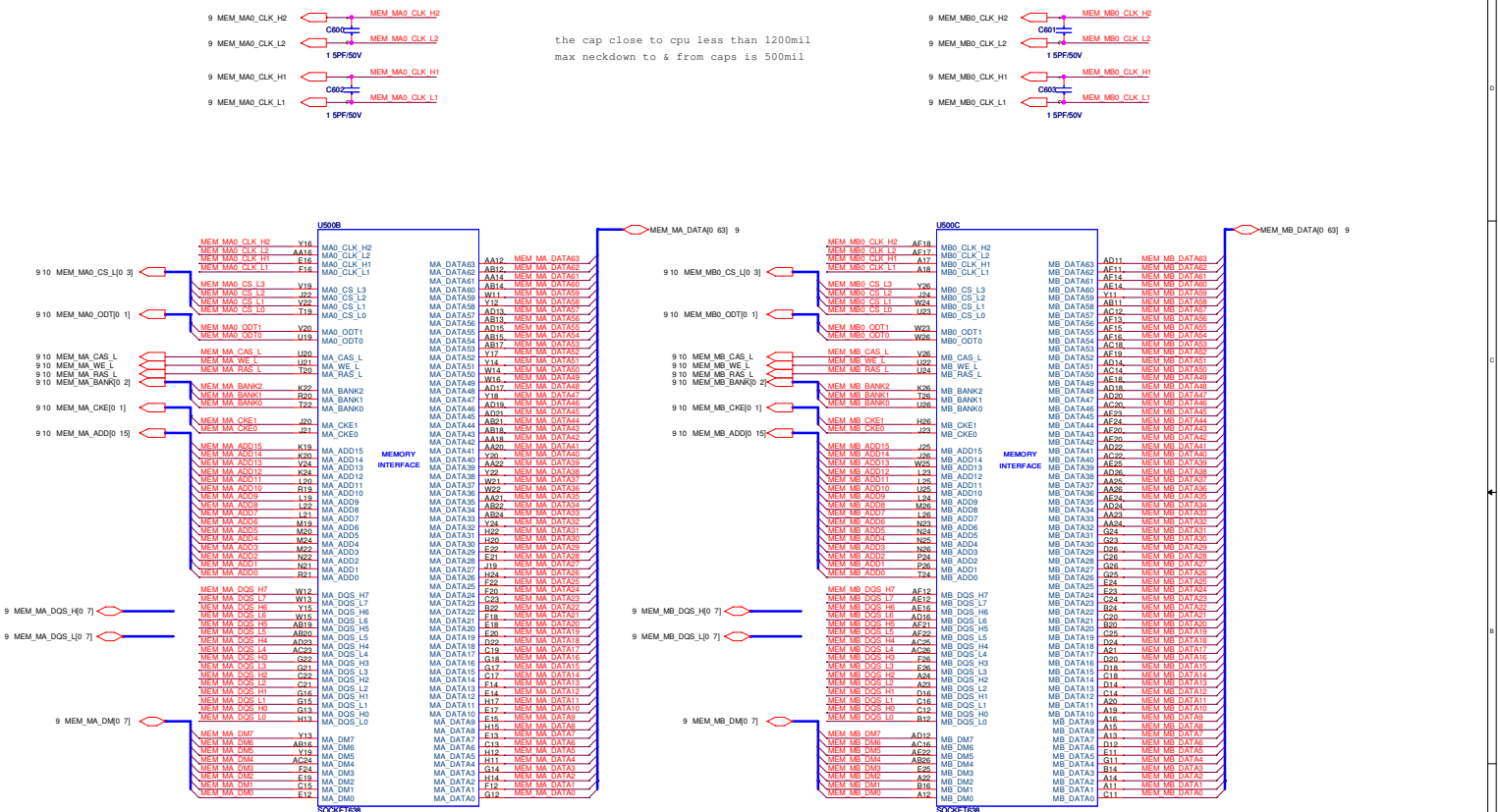


Do not cross plane.



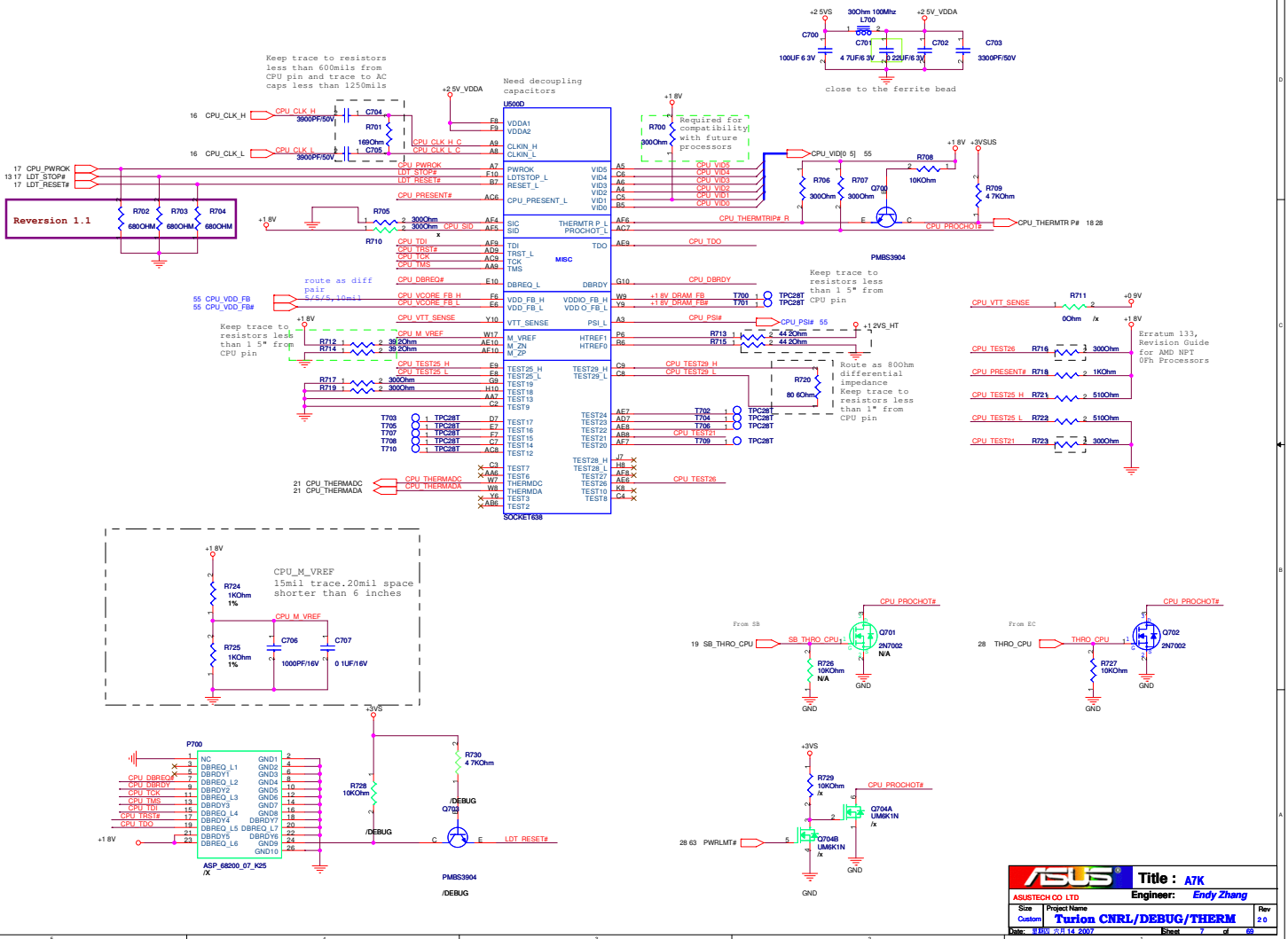


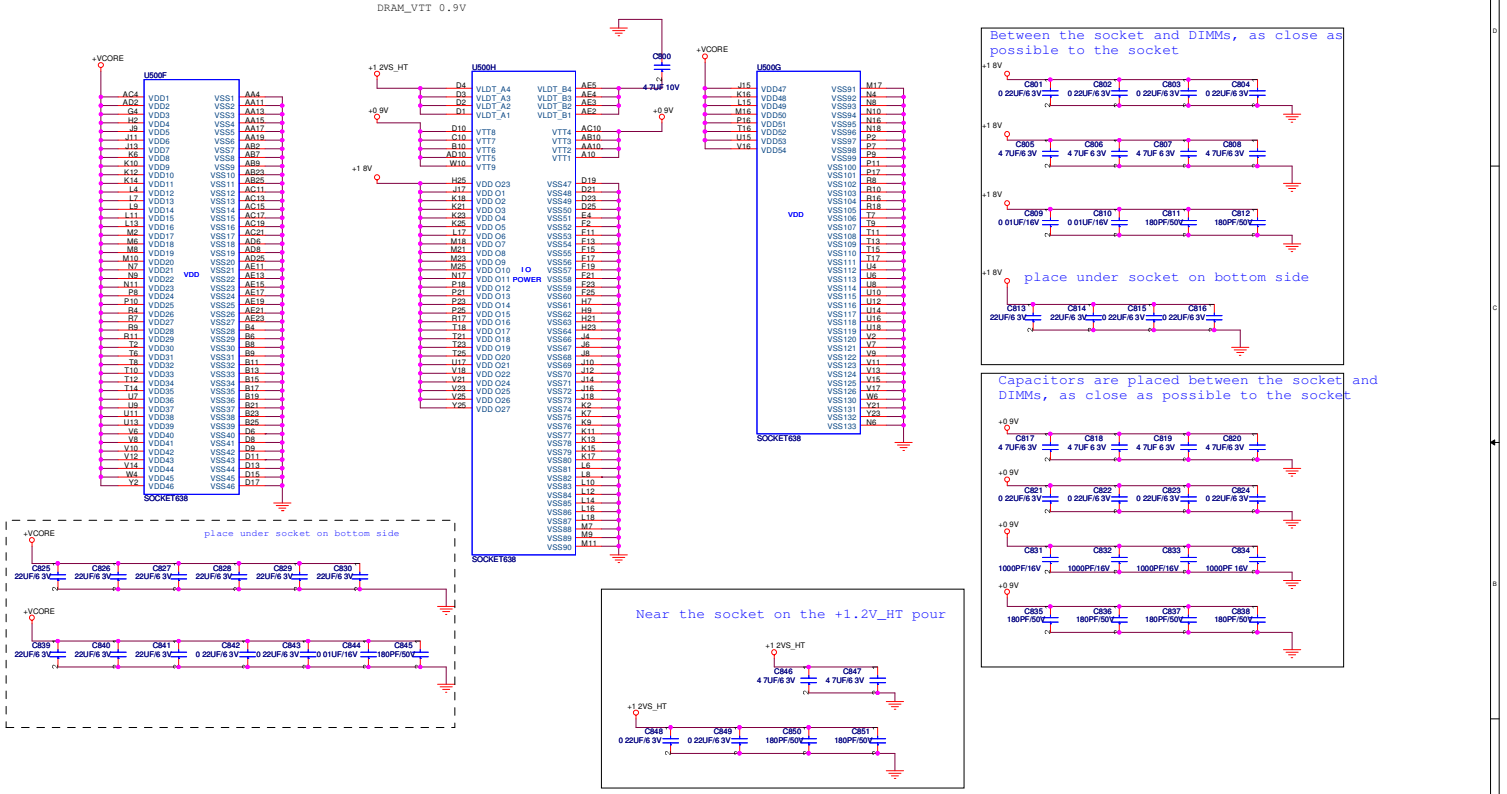
ASUS	Title : A7K		
ASUSTECH CO LTD	Engineer: Endy Zhang		
Size: Custom	Project Name: Turion HT I/F		Rev: 2.0
Date: 星期四 六月 14 2007	Sheet 5 of 69		



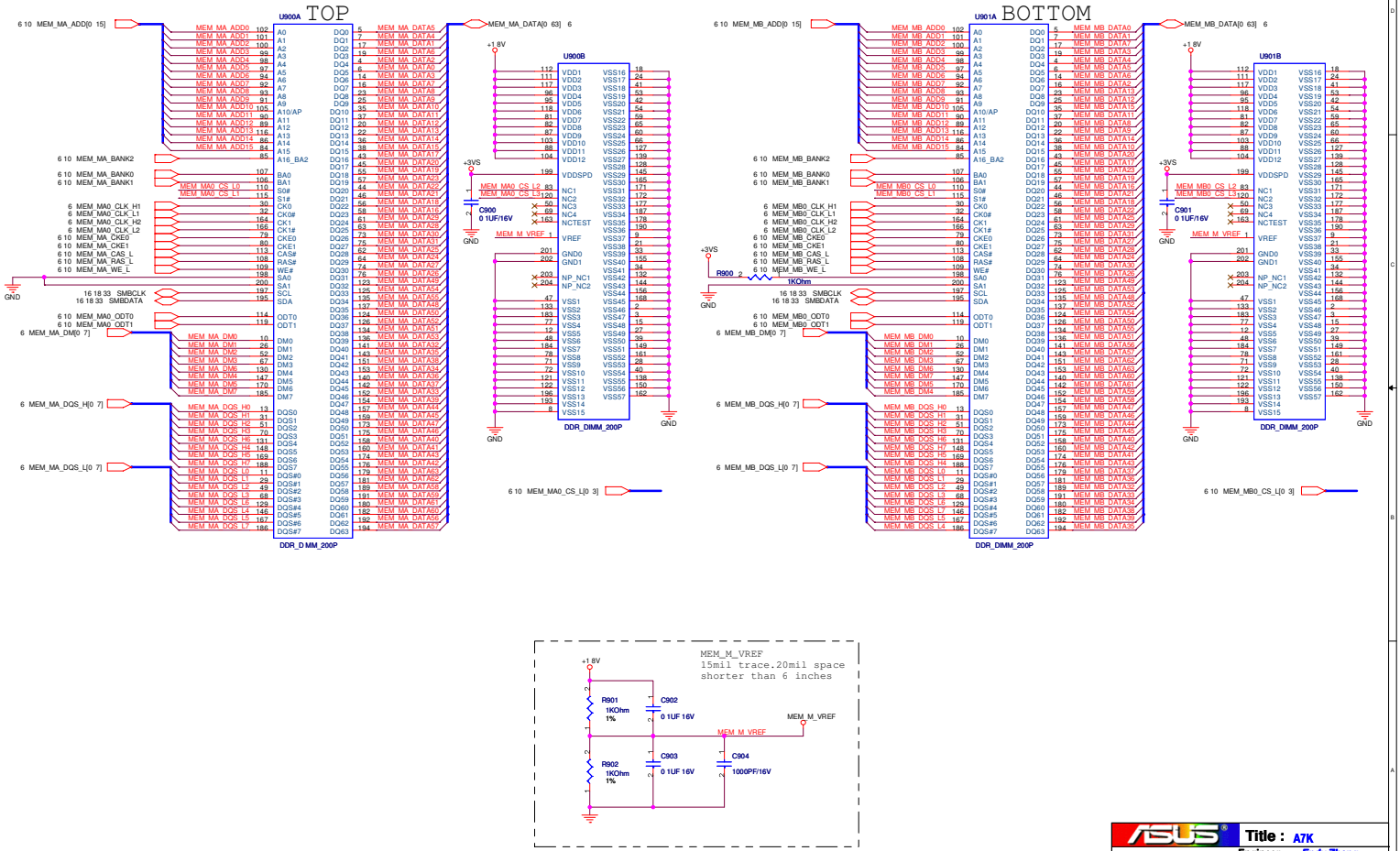
ASUSTECH CO LTD		Engineer:	Endy Zhang
Size: Custom	Project Name: Turion DDR2 Memory I/F		Rev: 2.0
Date: 星期四 六月 14, 2007		Sheet 6 of 69	

Title : A7K


Reversion 1.1
Keep trace to resistors less than 600mils from CPU pin and trace to AC caps less than 1250mils
Need decoupling capacitors
SOCKET638
Required for compatibility with future processors
PMBS3904
route as diff pair 5/5/5/10mil
Keep trace to resistors less than 1 5" from CPU pin
Keep trace to resistors less than 1" from CPU pin
Route as 800hm differential impedance
close to the ferrite bead
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
CPU_M_VREF
15mil trace.20mil space shorter than 6 inches
ASP_68200_07_K25
/X
/DEBUG
Title : A7K
ASUSTECH CO LTD
Engineer: Endy Zhang
Project Name
Turion CNRL/DEBUG/THERM
Rev
2.0
Sheet 7 of 69

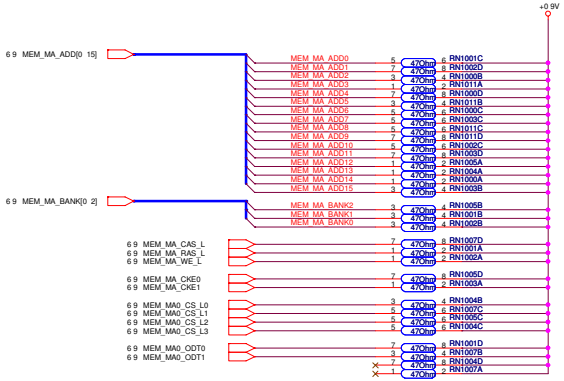


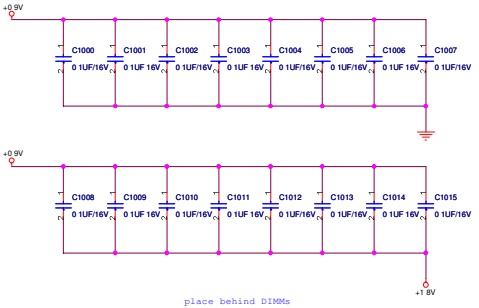
ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: Turion Power		Rev: 2.0
Date: 星期一 六月 11, 2007	Sheet 8 of 69		

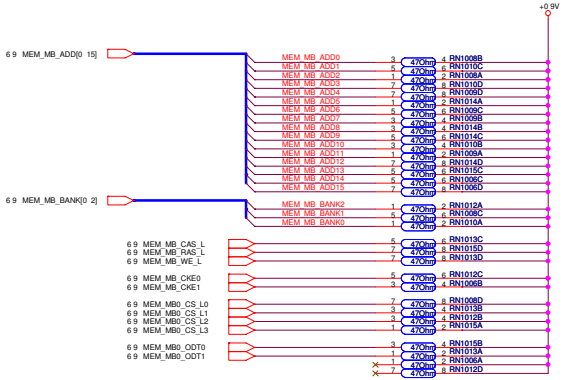


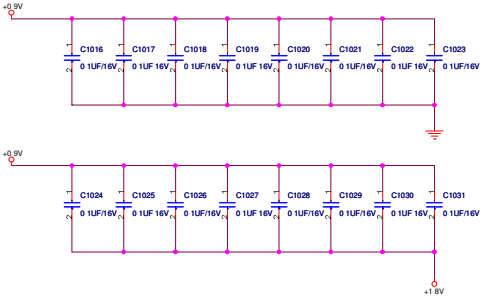
ASUSTECH CO LTD		Engineer:	Endy Zhang
Size: Custom	Project Name: DDR2 SODIMM		Rev: 2.0
Date: 星期四 六月 14 2007		Sheet 9 of 69	

Title : A7K


+0.9V
6 9 MEM_MA_ADD[0 15]
MEM_MA_ADD0
MEM_MA_ADD1
MEM_MA_ADD2
MEM_MA_ADD3
MEM_MA_ADD4
MEM_MA_ADD5
MEM_MA_ADD6
MEM_MA_ADD7
MEM_MA_ADD8
MEM_MA_ADD9
MEM_MA_ADD10
MEM_MA_ADD11
MEM_MA_ADD12
MEM_MA_ADD13
MEM_MA_ADD14
MEM_MA_ADD15
RN1001C
RN1002D
RN1000B
RN1011A
RN1000D
RN1011B
RN1000C
RN1003C
RN1011C
RN1011D
RN1002C
RN1003D
RN1005A
RN1004A
RN1000A
RN1003B
6 9 MEM_MA_BANK[0 2]
MEM_MA_BANK2
MEM_MA_BANK1
MEM_MA_BANK0
RN1005B
RN1001B
RN1002B
6 9 MEM_MA_CAS_L
6 9 MEM_MA_RAS_L
6 9 MEM_MA_WE_L
RN1007D
RN1001A
RN1002A
6 9 MEM_MA_CKE0
6 9 MEM_MA_CKE1
RN1005D
RN1003A
6 9 MEM_MA0_CS_L0
6 9 MEM_MA0_CS_L1
6 9 MEM_MA0_CS_L2
6 9 MEM_MA0_CS_L3
RN1004B
RN1007C
RN1005C
RN1004C
6 9 MEM_MA0_ODT0
6 9 MEM_MA0_ODT1
RN1001D
RN1007B
RN1004D
RN1007A
47Ohm

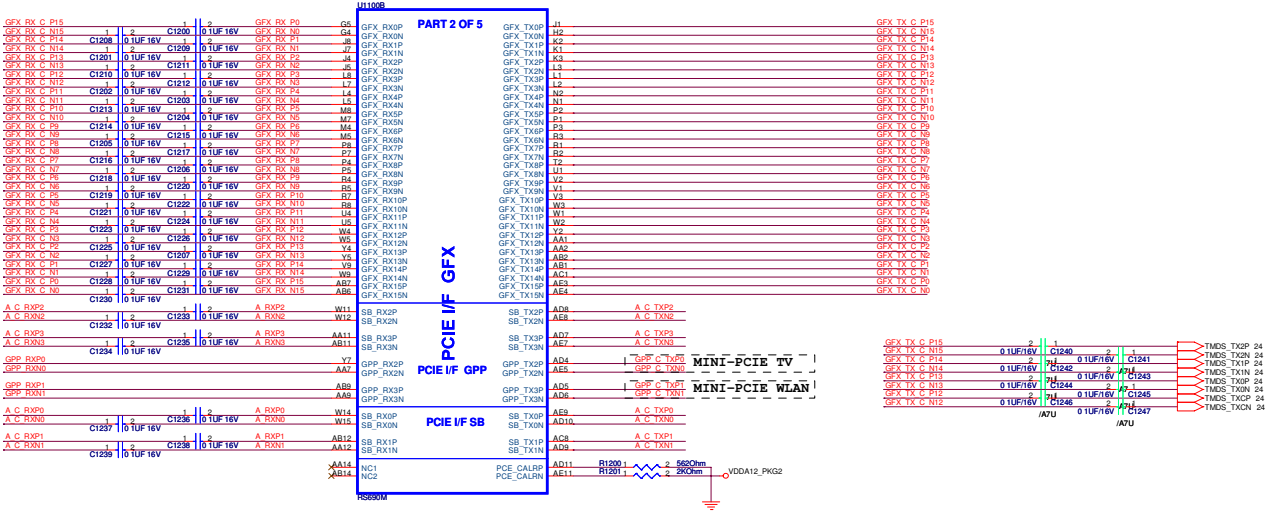

+0.9V
C1000
C1001
C1002
C1003
C1004
C1005
C1006
C1007
C1008
C1009
C1010
C1011
C1012
C1013
C1014
C1015
0 1UF/16V
+1.8V
place behind DIMMs


+0.9V
6 9 MEM_MB_ADD[0 15]
MEM_MB_ADD0
MEM_MB_ADD1
MEM_MB_ADD2
MEM_MB_ADD3
MEM_MB_ADD4
MEM_MB_ADD5
MEM_MB_ADD6
MEM_MB_ADD7
MEM_MB_ADD8
MEM_MB_ADD9
MEM_MB_ADD10
MEM_MB_ADD11
MEM_MB_ADD12
MEM_MB_ADD13
MEM_MB_ADD14
MEM_MB_ADD15
RN1008B
RN1010C
RN1008A
RN1010D
RN1009D
RN1014A
RN1009C
RN1009B
RN1014B
RN1014C
RN1010B
RN1009A
RN1014D
RN1015C
RN1006C
RN1008D
6 9 MEM_MB_BANK[0 2]
MEM_MB_BANK2
MEM_MB_BANK1
MEM_MB_BANK0
RN1012A
RN1008C
RN1010A
6 9 MEM_MB_CAS_L
6 9 MEM_MB_RAS_L
6 9 MEM_MB_WE_L
RN1013C
RN1015D
RN1013D
6 9 MEM_MB_CKE0
6 9 MEM_MB_CKE1
RN1012C
RN1006B
6 9 MEM_MB0_CS_L0
6 9 MEM_MB0_CS_L1
6 9 MEM_MB0_CS_L2
6 9 MEM_MB0_CS_L3
RN1008D
RN1013B
RN1012B
RN1015A
6 9 MEM_MB0_ODT0
6 9 MEM_MB0_ODT1
RN1015B
RN1013A
RN1006A
RN1012D
47Ohm

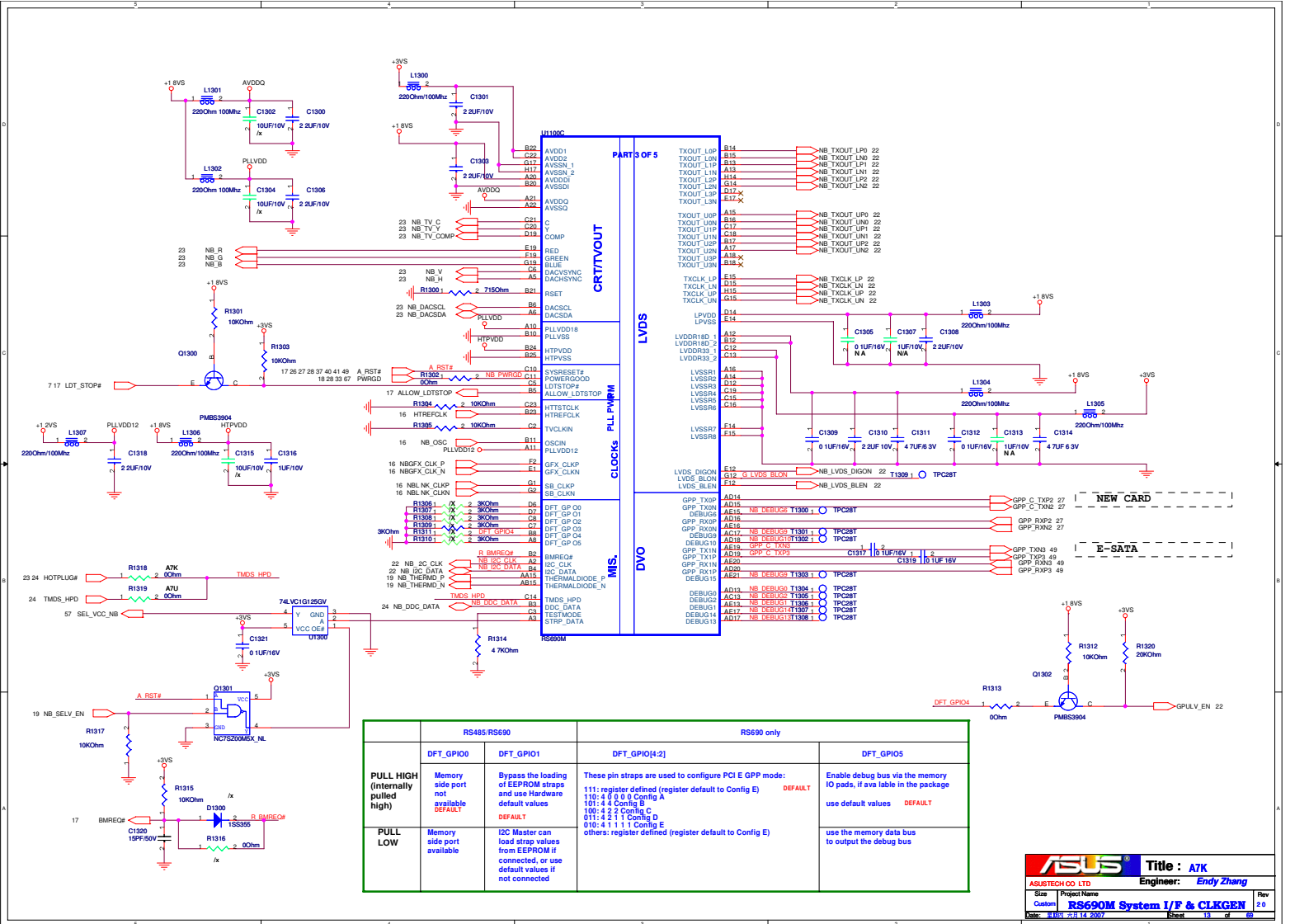

+0.9V
C1016
C1017
C1018
C1019
C1020
C1021
C1022
C1023
C1024
C1025
C1026
C1027
C1028
C1029
C1030
C1031
0 1UF/16V
+1.8V
place behind DIMMs

ASUSTECH CO LTD		Engineer: Endy Zhang	
Size: Custom	Project Name: RS690M HT Link0 I/F		Rev: 2.0
Date: 星期四 六月 14 2007		Sheet 11 of 69	

Title : A7K

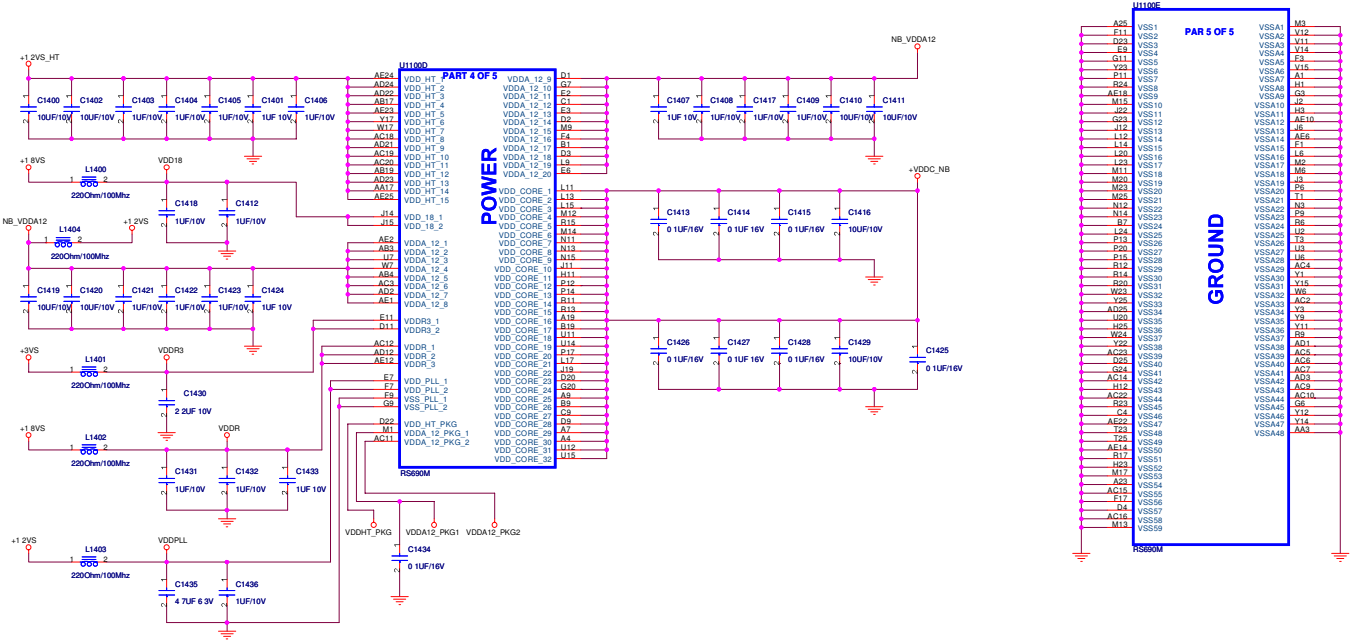


Title :	A7K
ASUSTECH CO LTD	Engineer: Endy Zhang
Size: Custom	Project Name: RS690M PCIE Link I/F
Rev: 2.0	
Date: 星期四 六月 14 2007	Sheet 12 of 69



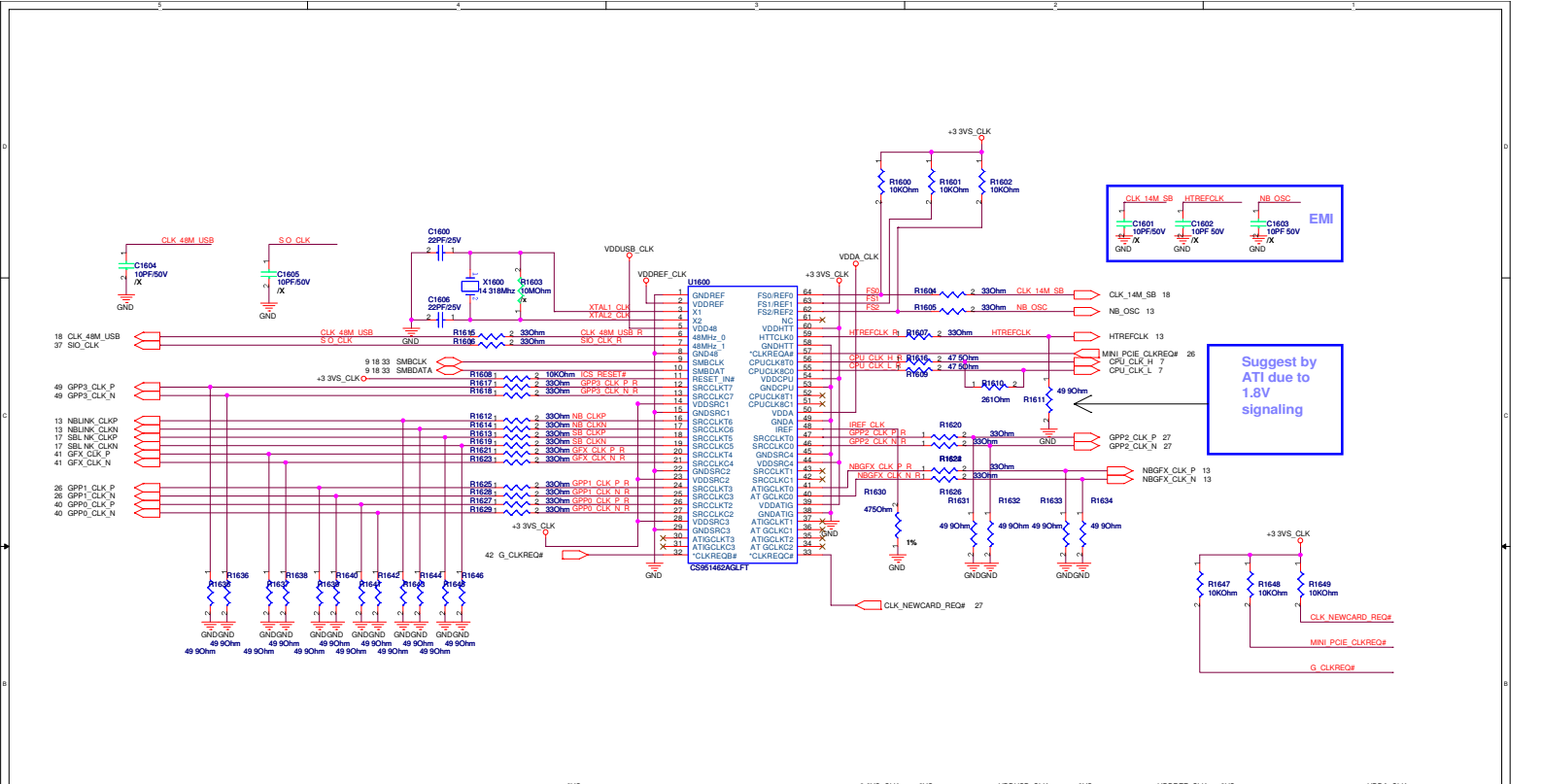
	RS485/RS690		RS690 only	
	DFT_GPIO0	DFT_GPIO1	DFT_GPIO[4:2]	DFT_GPIO5
PULL HIGH (internally pulled high)	Memory side port not available DEFAULT	Bypass the loading of EEPROM straps and use Hardware default values DEFAULT	These pin straps are used to configure PCI E GPP mode: 111: register defined (register default to Config E) DEFAULT 110: 4 0 0 0 0 Config A 101: 4 4 Config B 100: 4 2 2 Config C 011: 4 2 1 1 Config D 010: 4 1 1 1 1 Config E others: register defined (register default to Config E)	Enable debug bus via the memory IO pads, if ava lable in the package use default values DEFAULT
PULL LOW	Memory side port available	I2C Master can load strap values from EEPROM if connected, or use default values if not connected		use the memory data bus to output the debug bus

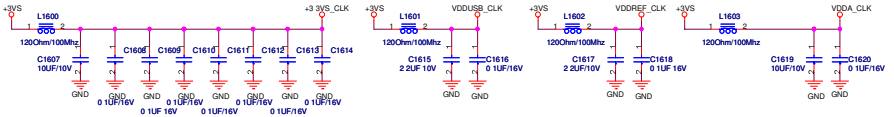
ASUSTECH CO LTD	Title : A7K	
	Engineer: Endy Zhang	
Size: Custom	Project Name: RS690M System I/F & CLKGEN	Rev: 2.0
Date: Wed, 14, 2007	Sheet 13 of 69	



ASUSTEK CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: RS690M Power		Rev: 2.0
Date: 星期四 六月 14 2007	Sheet 14 of 69		

ASUSTECH CO LTD		Title : A7KM	
		Engineer: Endy Zhang	
Size: Custom	Project Name: <Doc>		Rev: 2.0
Date: 星期四 六月 14 2007		Sheet 15 of 69	





EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

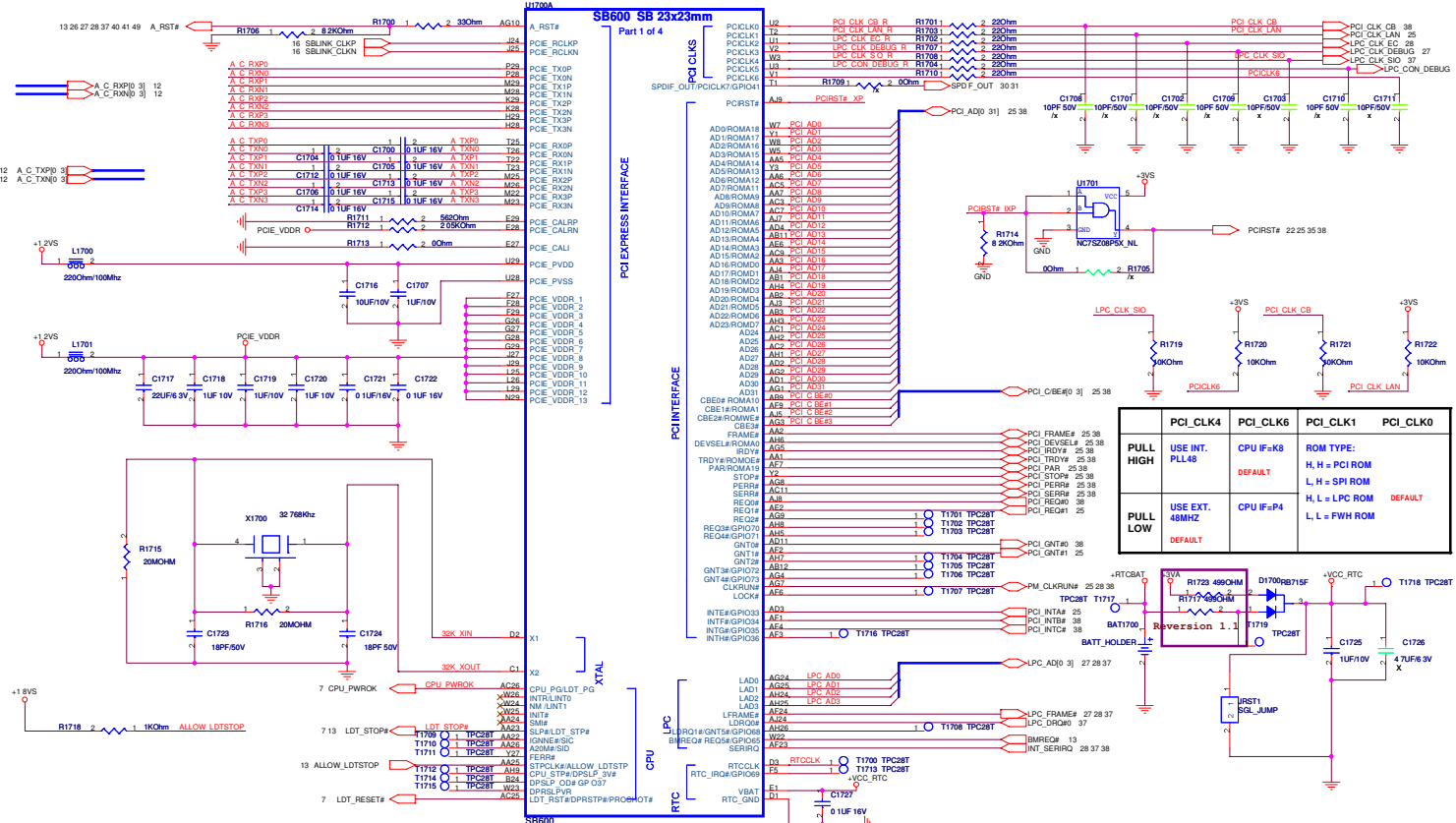
ASUSTECH CO LTD

Title : A7K

Engineer: Endy Zhang

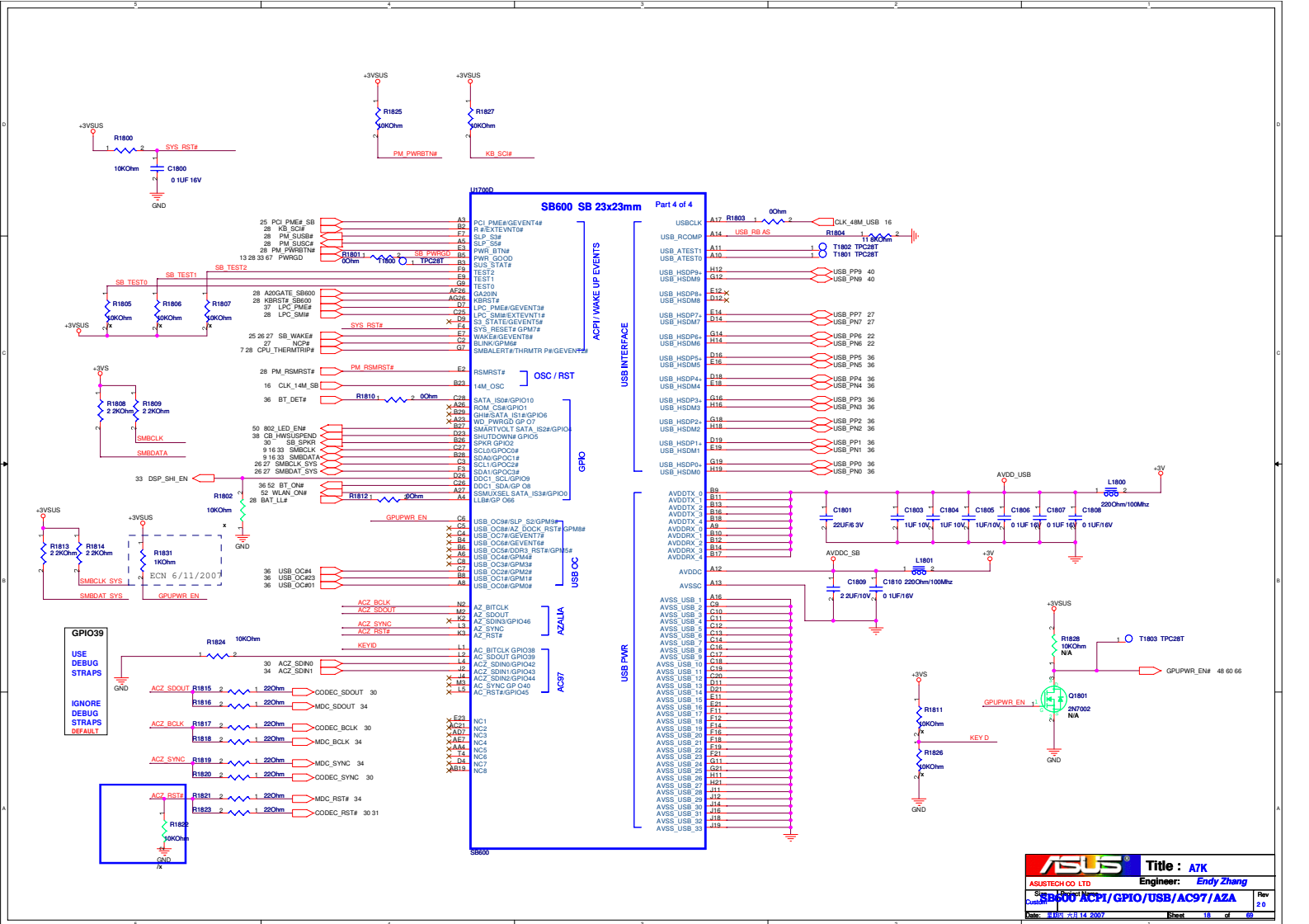
Size: Custom | Project Name: External Clock Generator | Rev: 2.0

Date: 星期六 十月 14, 2007 | Sheet 16 of 69

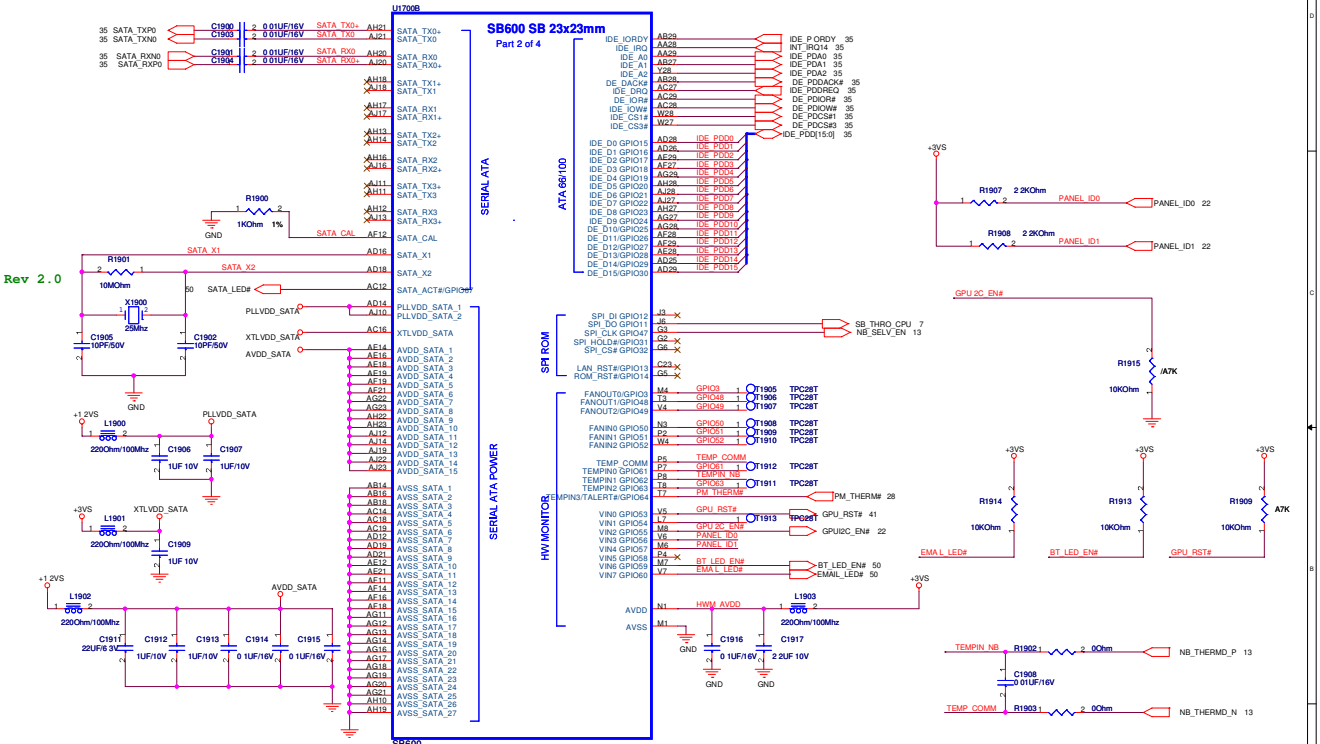


	PCI_CLK4	PCI_CLK6	PCI_CLK1	PCI_CLK0
PULL HIGH	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM L, H = SPI ROM H, L = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

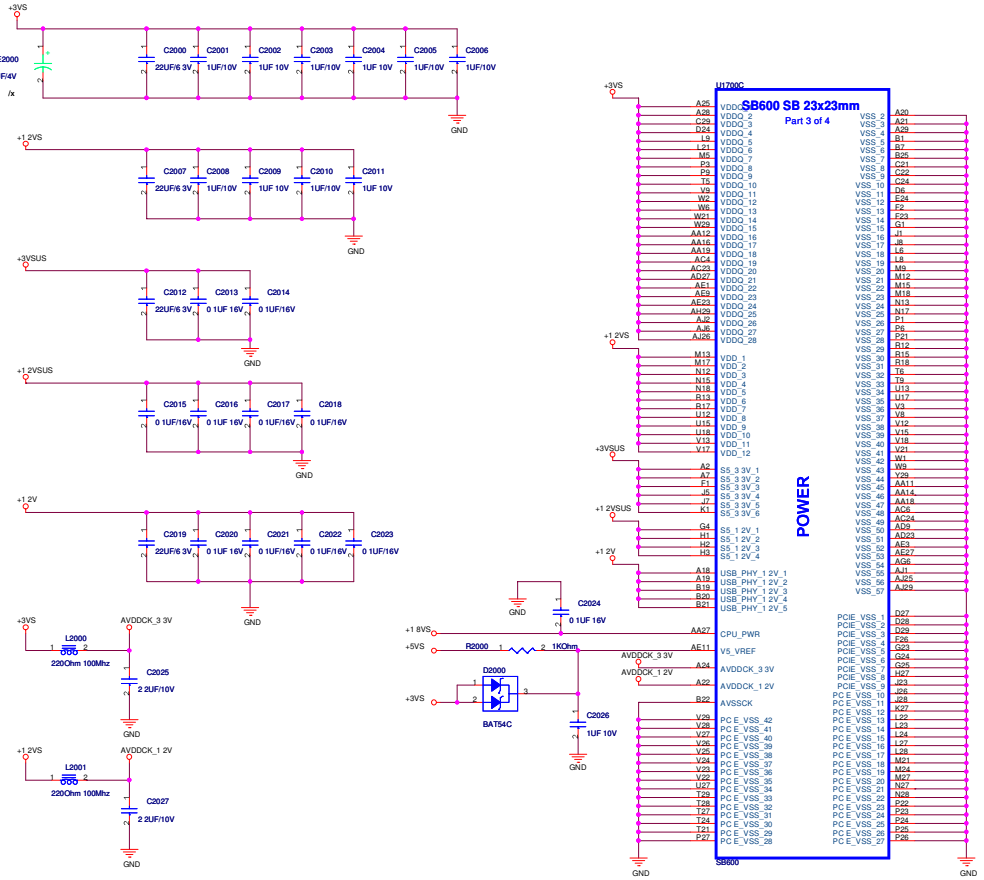
ASUSTEK CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: SB600 PCIE/PCI/CPU/LPC		Rev: 2.0
Date: 星期日, 六月 17, 2007	Sheet 17 of 69		



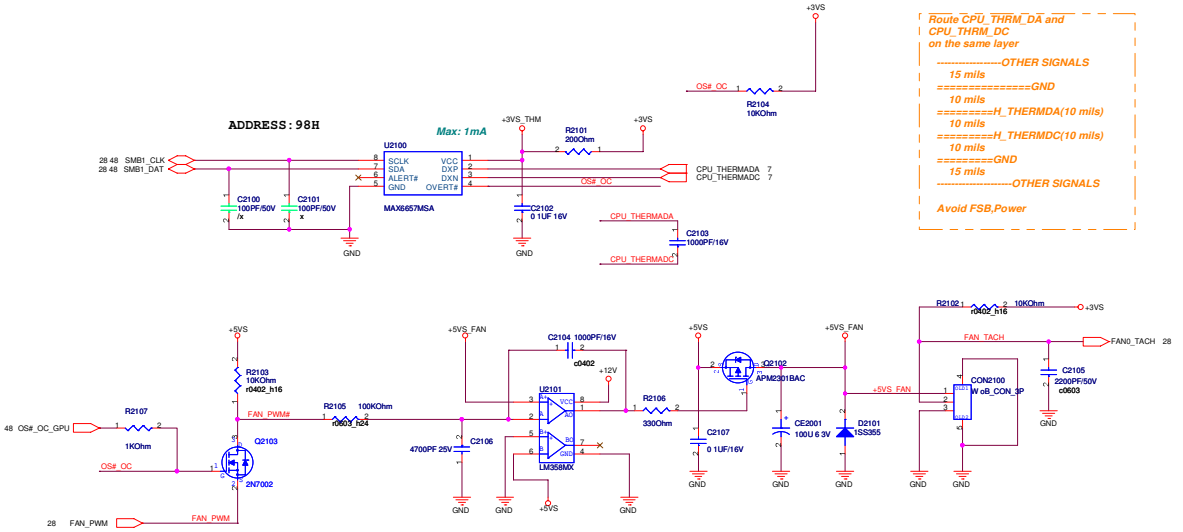
Title :	A7K
ASUSTECH CO LTD	Engineer: Endy Zhang
Size: Custom	Document Number: SB600 ACPI / GPIO / USB / AC97 / AZA
Date: 星期一 六月 11, 2007	Sheet 18 of 69



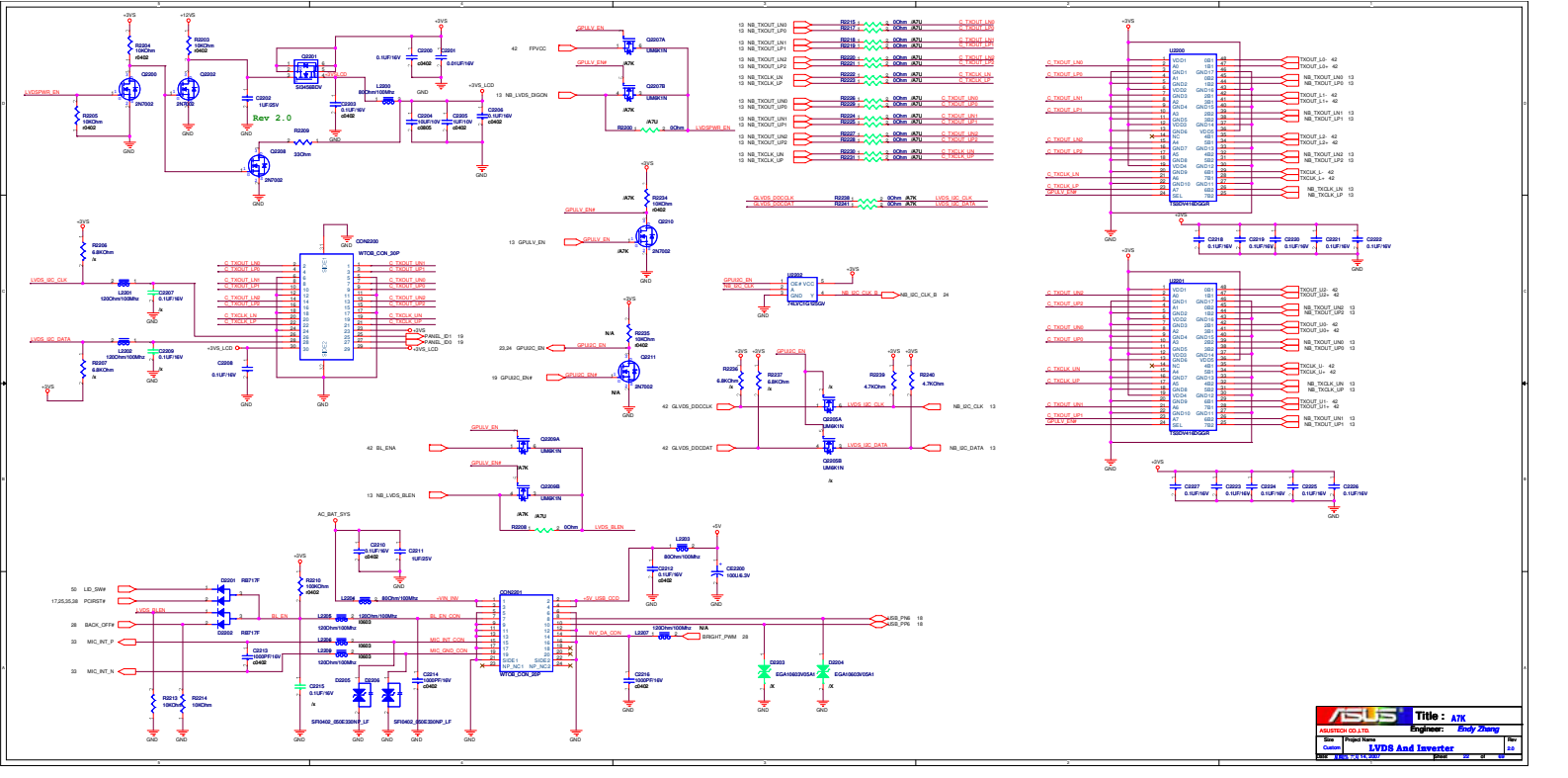
ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: SB60 SATA/IDE/HWM/SPI		Rev: 2.0
Date: 星期六 十月 14, 2007		Sheet 19 of 69	



Title :	A7K
ASUSTECH CO LTD	Engineer: Endy Zhang
Size: Custom	Project Name: SB600 Power & Decoupling
Rev: 2.0	
Date: 星期四 六月 14 2007	Sheet 20 of 69



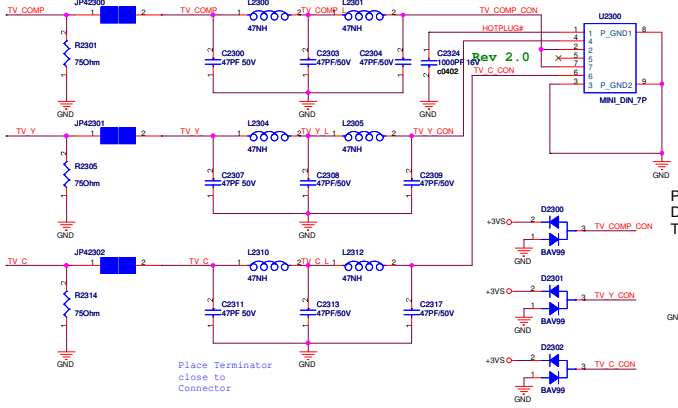
ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: Thermal Fan Control		Rev: 2.0
Date: 星期日 六月 17, 2007		Sheet 21 of 69	


Rev 2.0
WTOB_CON_30P
CON2200
CON2201
WTOB_CON_30P
U2200
U2201
TSSOP48DGGR
Title : A7K
ASUSTeK CO.,LTD.
Engineer: Andy Zhang
Project Name
LVDS And Inverter
Rev
2.0
Date: Mon, Jul 14, 2007
Sheet 22 of 56

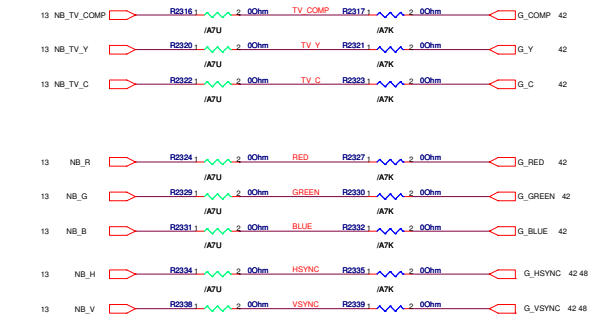
L change to 09G0234720001!!!

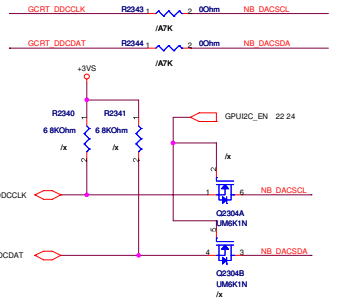
TV OUT

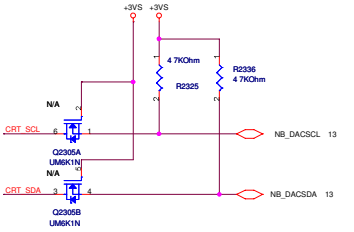
CRT OUT

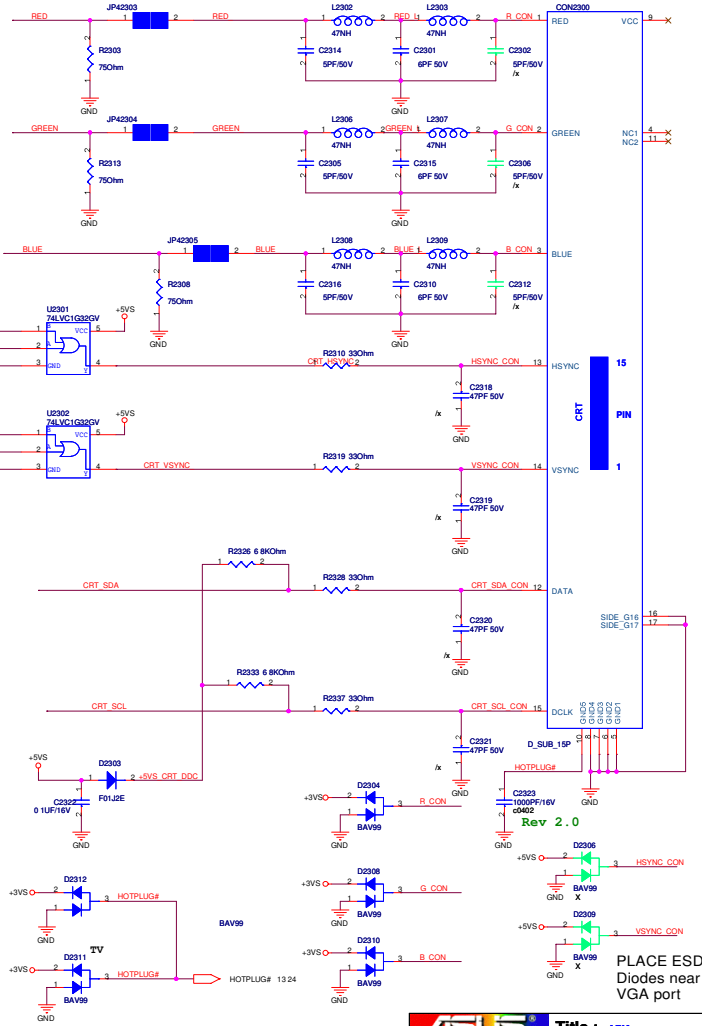


PLACE ESD
Diodes near
TV port



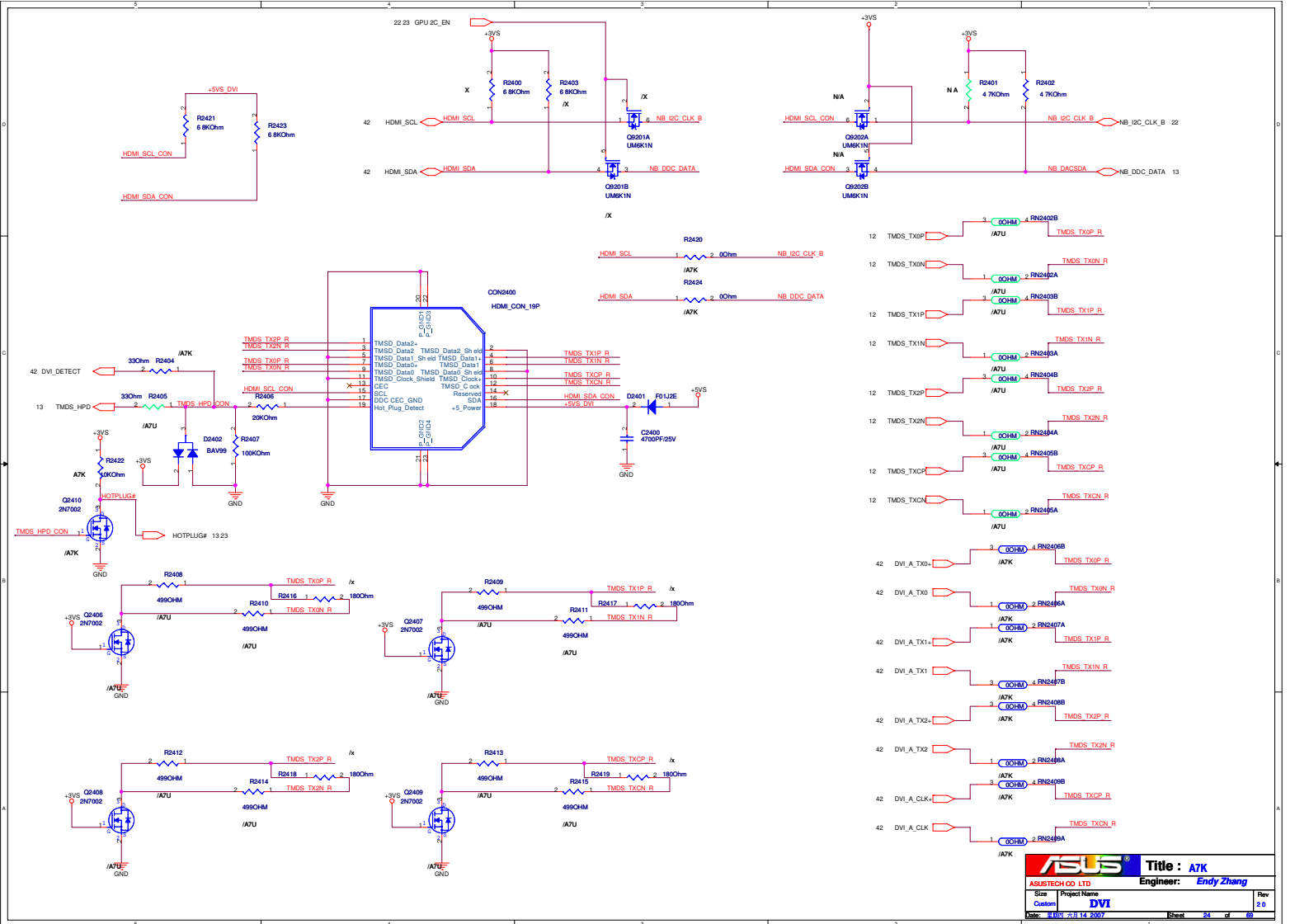


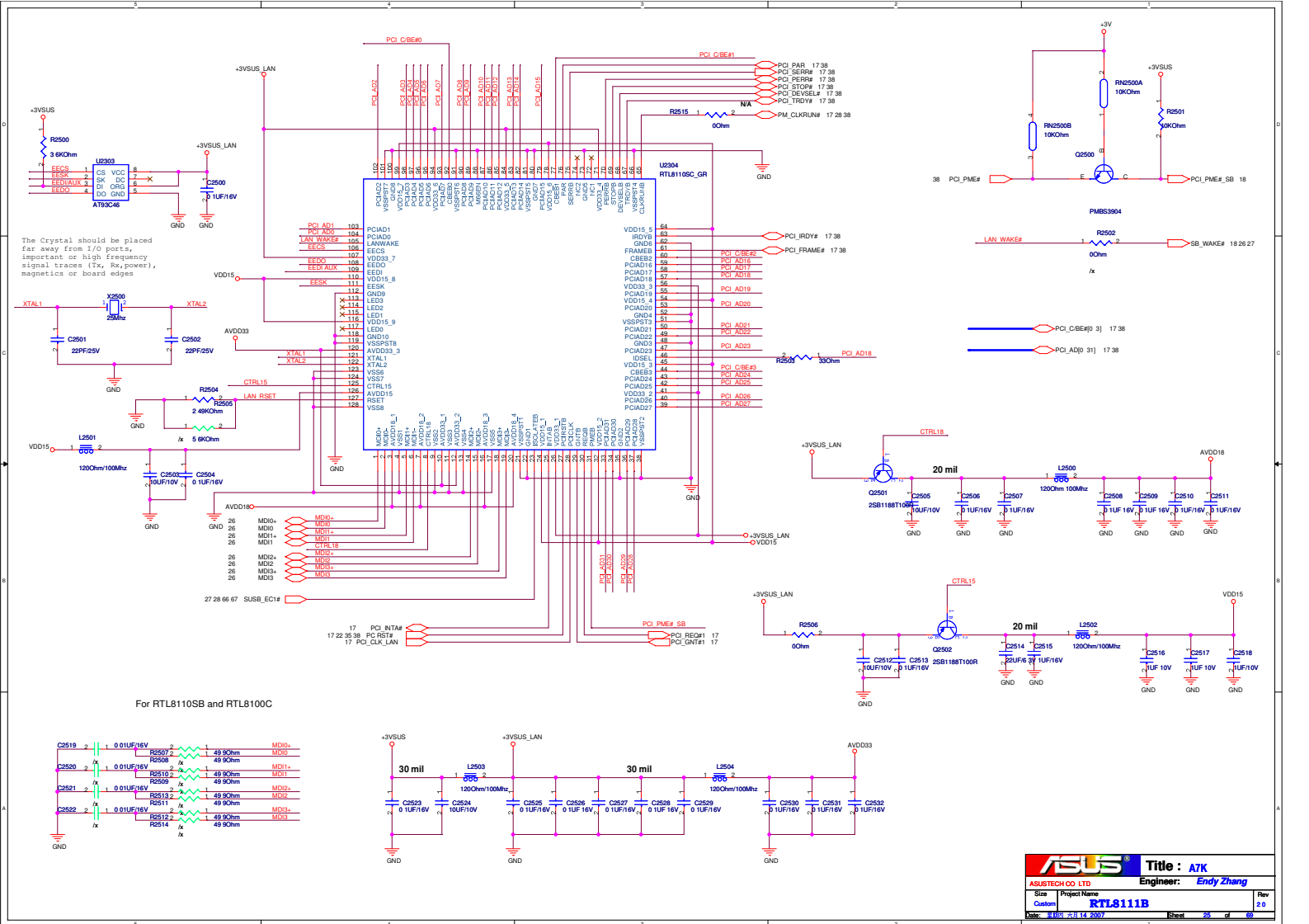


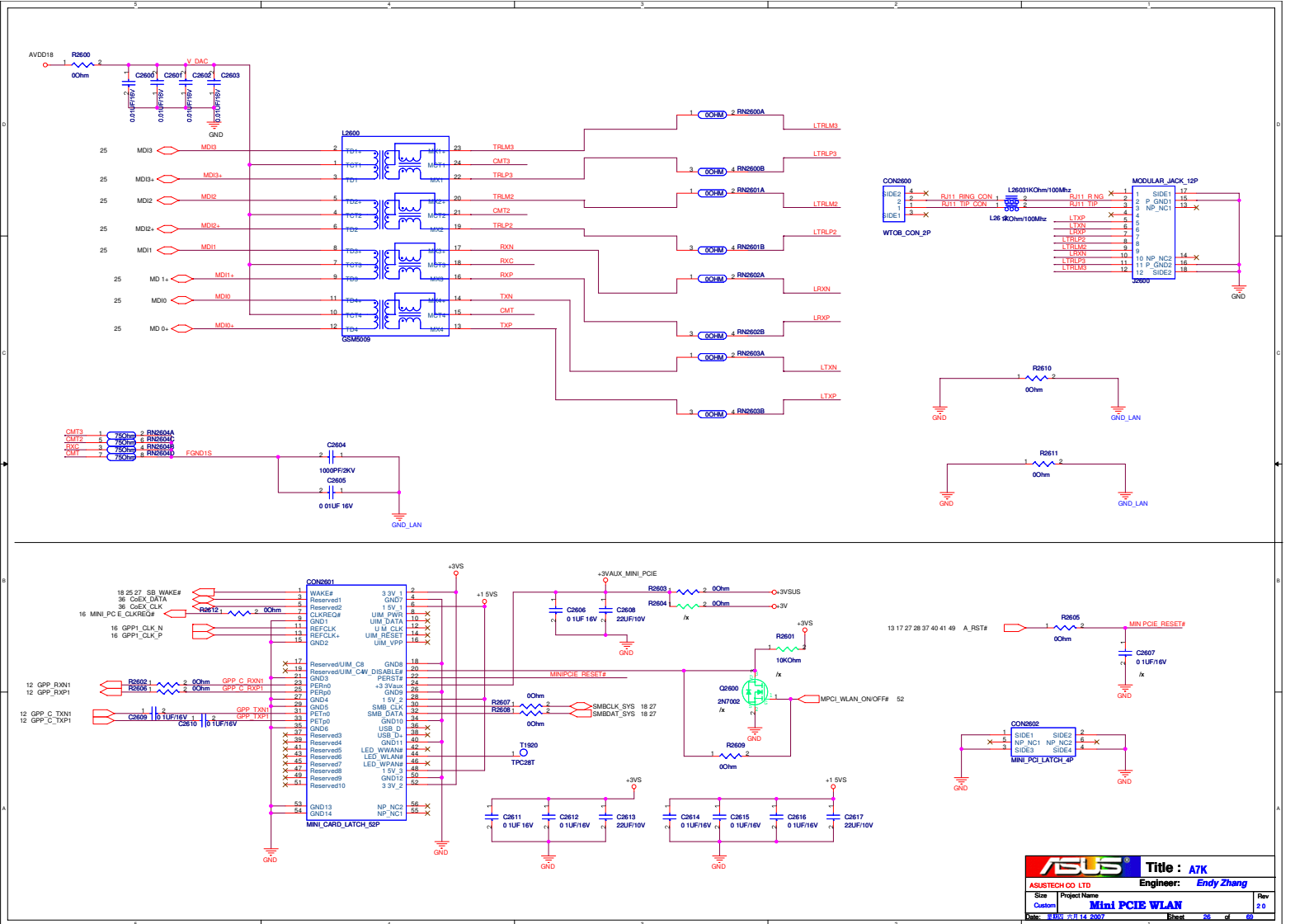


PLACE ESD
Diodes near
VGA port

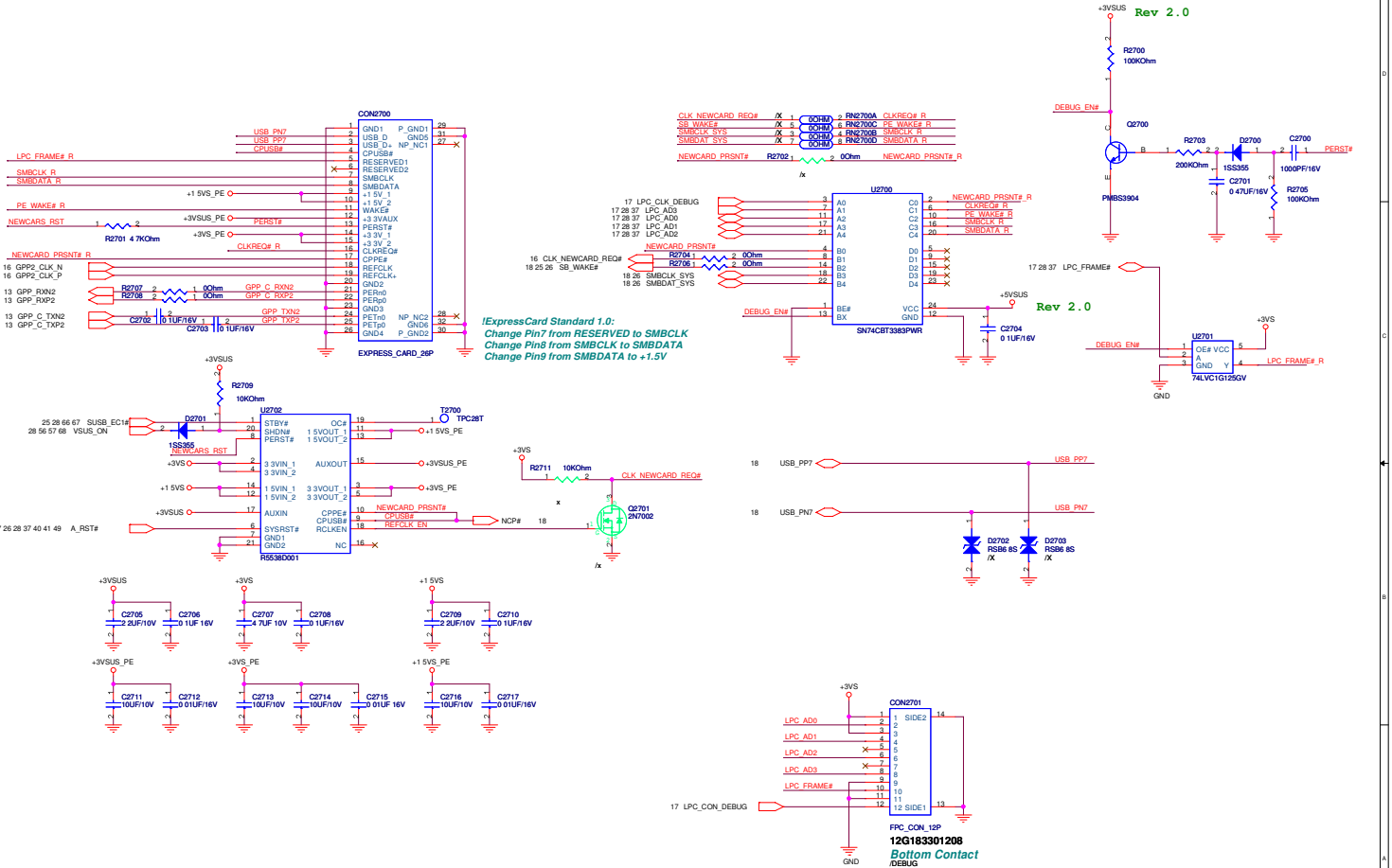
ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: CRT And TV Connector		Rev: 2.0
Date: 星期四 8月 16, 2007	Sheet 23 of 69		


+5VS_DVI
R2421 6 8KOhm
R2423 6 8KOhm
HDMI_SCL_CON
HDMI_SDA_CON
22 23 GPU 2C_EN
+3VS
R2400 6 8KOhm
R2403 6 8KOhm
X
/X
42 HDMI_SCL
HDMI_SCL
NB_I2C_CLK_B
Q9201A UM6K1N
42 HDMI_SDA
HDMI_SDA
NB_DDC_DATA
Q9201B UM6K1N
+3VS
R2401 4 7KOhm
R2402 4 7KOhm
N/A
HDMI_SCL_CON
NB_I2C_CLK_B
NB_I2C_CLK_B 22
Q9202A UM6K1N
HDMI_SDA_CON
NB_DACSDA
NB_DDC_DATA 13
Q9202B UM6K1N
R2420
HDMI_SCL
0Ohm
NB_I2C_CLK_B
/A7K
R2424
HDMI_SDA
0Ohm
NB_DDC_DATA
/A7K
CON2400
HDMI_CON_19P
42 DVI_DETECT
13 TMDS_HPD
33Ohm R2404
33Ohm R2405
/A7K
/A7U
TMDS_HPD_CON
R2406 20KOhm
D2402 BAV99
R2407 100KOhm
R2422 10KOhm
+3VS
A7K
Q2410 2N7002
HOTPLUG#
HOTPLUG# 13 23
TMDS_HPD_CON
GND
TMDS_TX2P_R
TMDS_TX2N_R
TMDS_TX0P_R
TMDS_TX0N_R
HDMI_SCL_CON
HDMI_SDA_CON
TMDS_TX1P_R
TMDS_TX1N_R
TMDS_TXCP_R
TMDS_TXCN_R
+5VS_DVI
TMSD_Data2+
TMSD_Data2
TMSD_Data2_Sh eld
TMSD_Data1_Sh eld
TMSD_Data1+
TMSD_Data1-
TMSD_Data1
TMSD_Data0
TMSD_Data0_Sh eld
TMSD_Clock_Shield
TMSD_Clock+
CEC
TMSD_C ock
SCL
Reserved
DDC CEC_GND
SDA
Hot_Plug_Detect
+5_Power
P_GND1
P_GND3
P_GND2
P_GND4
D2401 F01J2E
C2400 4700PF/25V
R2408 499OHM
R2410 499OHM
R2416 180Ohm
Q2406 2N7002
R2409 499OHM
R2411 499OHM
R2417 180Ohm
Q2407 2N7002
R2412 499OHM
R2414 499OHM
R2418 180Ohm
Q2408 2N7002
R2413 499OHM
R2415 499OHM
R2419 180Ohm
Q2409 2N7002
12 TMDS_TX0P
12 TMDS_TX0N
12 TMDS_TX1P
12 TMDS_TX1N
12 TMDS_TX2P
12 TMDS_TX2N
12 TMDS_TXCP
12 TMDS_TXCN
RN2402B 0OHM
RN2402A 0OHM
RN2403B 0OHM
RN2403A 0OHM
RN2404B 0OHM
RN2404A 0OHM
RN2405B 0OHM
RN2405A 0OHM
TMDS_TX0P_R
TMDS_TX0N_R
TMDS_TX1P_R
TMDS_TX1N_R
TMDS_TX2P_R
TMDS_TX2N_R
TMDS_TXCP_R
TMDS_TXCN_R
42 DVI_A_TX0+
42 DVI_A_TX0
42 DVI_A_TX1+
42 DVI_A_TX1
42 DVI_A_TX2+
42 DVI_A_TX2
42 DVI_A_CLK+
42 DVI_A_CLK
RN2406B 0OHM
RN2406A 0OHM
RN2407A 0OHM
RN2407B 0OHM
RN2408B 0OHM
RN2408A 0OHM
RN2409B 0OHM
RN2409A 0OHM
/A7K
/A7U
ASUSTECH CO LTD
Title : A7K
Engineer: Endy Zhang
Size Custom
Project Name DVI
Rev 2.0
Date: 七月 14, 2007
Sheet 24 of 69

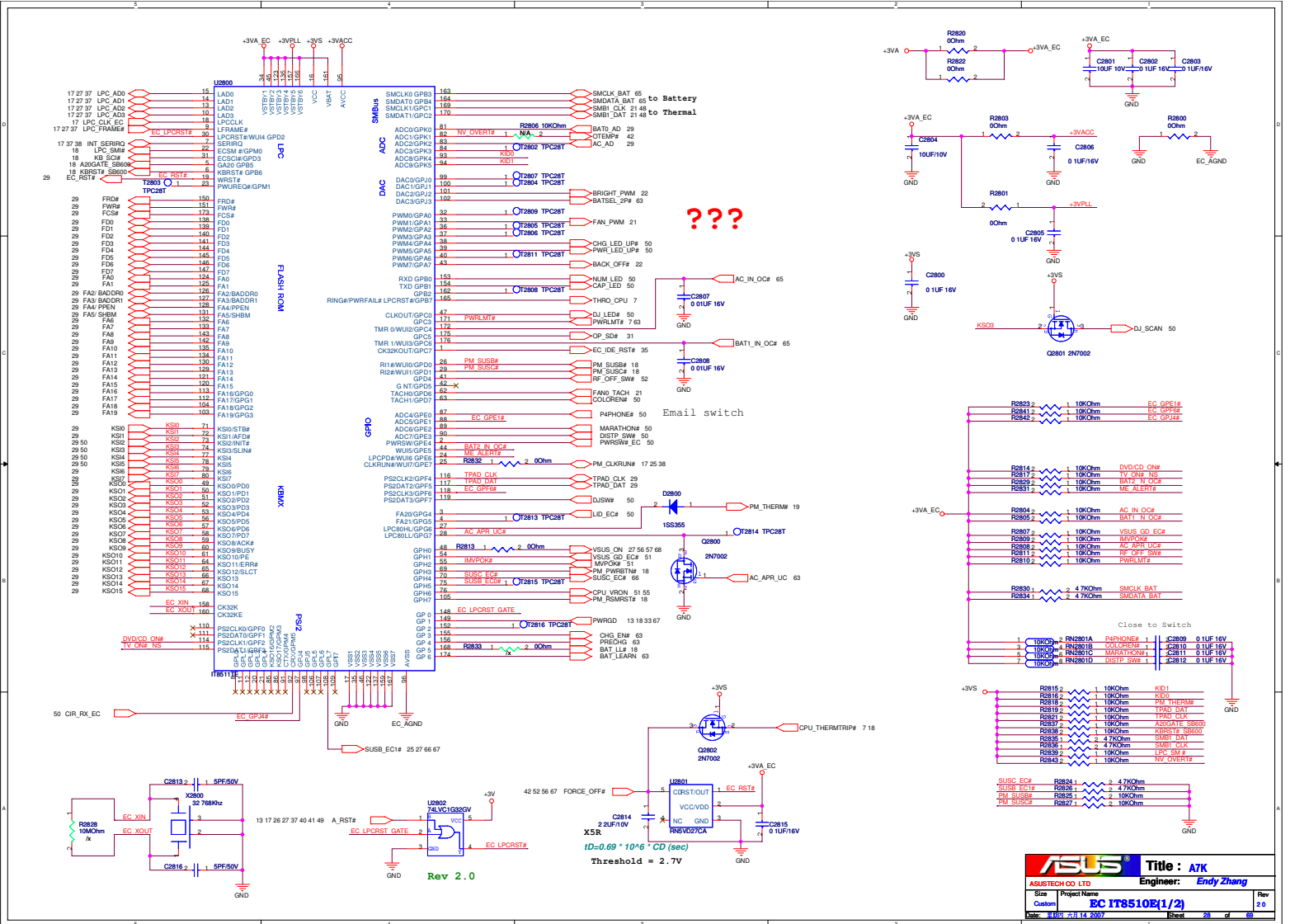

U2304
RTL8110SC_GR
U2303
AT93C46
X2500
25Mhz
Q2500
PMBS3904
Q2501
2SB1188T100R
Q2502
2SB1188T100R
The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx,power), magnetics or board edges
For RTL8110SB and RTL8100C
+3VSUS
+3VSUS_LAN
+3V
VDD15
AVDD33
AVDD18
CTRL18
CTRL15
LAN_RSET
XTAL1
XTAL2
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#[0 3] 17 38
PCI_AD[0 31] 17 38
PCI_PAR 17 38
PCI_SERR# 17 38
PCI_PERR# 17 38
PCI_STOP# 17 38
PCI_DEVSEL# 17 38
PCI_TRDY# 17 38
PCI_IRDY# 17 38
PCI_FRAME# 17 38
PM_CLKRUN# 17 28 38
PCI_PME# 38
PCI_PME#_SB 18
LAN_WAKE#
SB_WAKE# 18 26 27
PCI_INTA# 17
PCI_RST# 17 22 35 38
PCI_CLK_LAN 17
PCI_REQ#1 17
PCI_GNT#1 17
SUSB_EC1# 27 28 66 67
MDI0+ 26
MDI0- 26
MDI1+ 26
MDI1- 26
MDI2+ 26
MDI2- 26
MDI3+ 26
MDI3- 26
20 mil
30 mil
L2500 120Ohm 100Mhz
L2501 120Ohm/100Mhz
L2502 120Ohm/100Mhz
L2503 120Ohm/100Mhz
L2504 120Ohm/100Mhz
ASUSTECH CO LTD
Title : A7K
Engineer: Endy Zhang
Project Name RTL8111B
Rev 2.0
Sheet 25 of 69

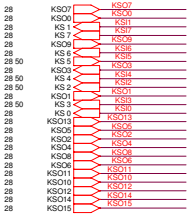


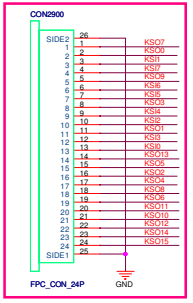
ASUSTECH CO LTD		Title : A7K		
		Engineer: Endy Zhang		
Size	Project Name			Rev
Custom	Mini PCIE WLAN			2.0
Date: 星期四 六月 14, 2007		Sheet 26 of 69		



ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: New Card		Rev: 2.0
Date: 星期四 六月 14, 2007		Sheet 27 of 69	


U2800
IT8511E
SMBus
LPC
ADC
DAC
FLASH ROM
KBMX
GPIO
PSIF
to Battery
to Thermal
???
Email switch
Close to Switch
Rev 2.0
ASUSTECH CO LTD
Title : A7K
Engineer: Endy Zhang
Project Name
EC IT8510E(1/2)
Rev 2.0
Sheet 28 of 69



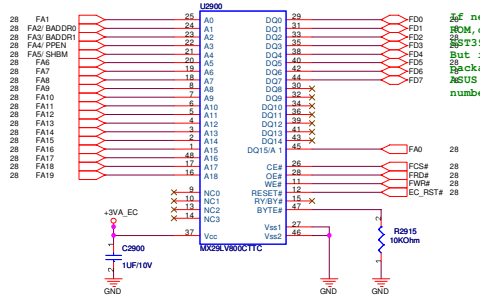


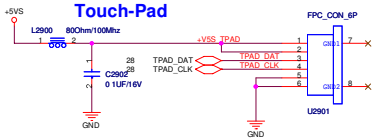
ISA ROM

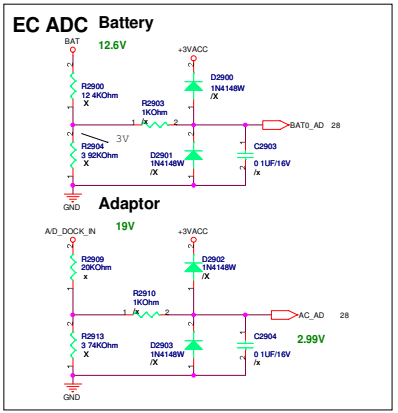
(8Mbits)

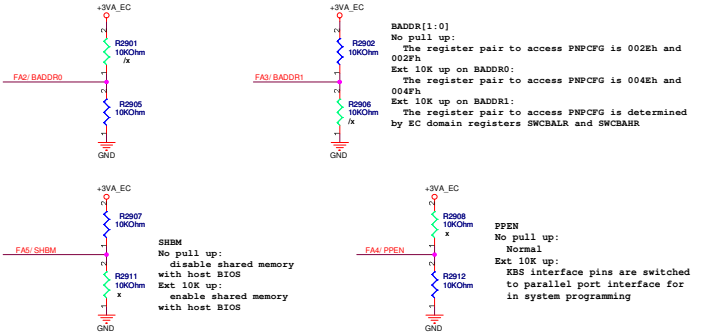
SST-PLCC32 4Mbits Flash ROM
PN:05G001014110
(FLASH SST SST39VF040-70-4C-NHE
4M-70 PLCC-32)

If need to use 8Mbits ISA ROM,could choose SST39LF080.
But it does not have PLCC32 Package.
ASUS does not have part number yet.





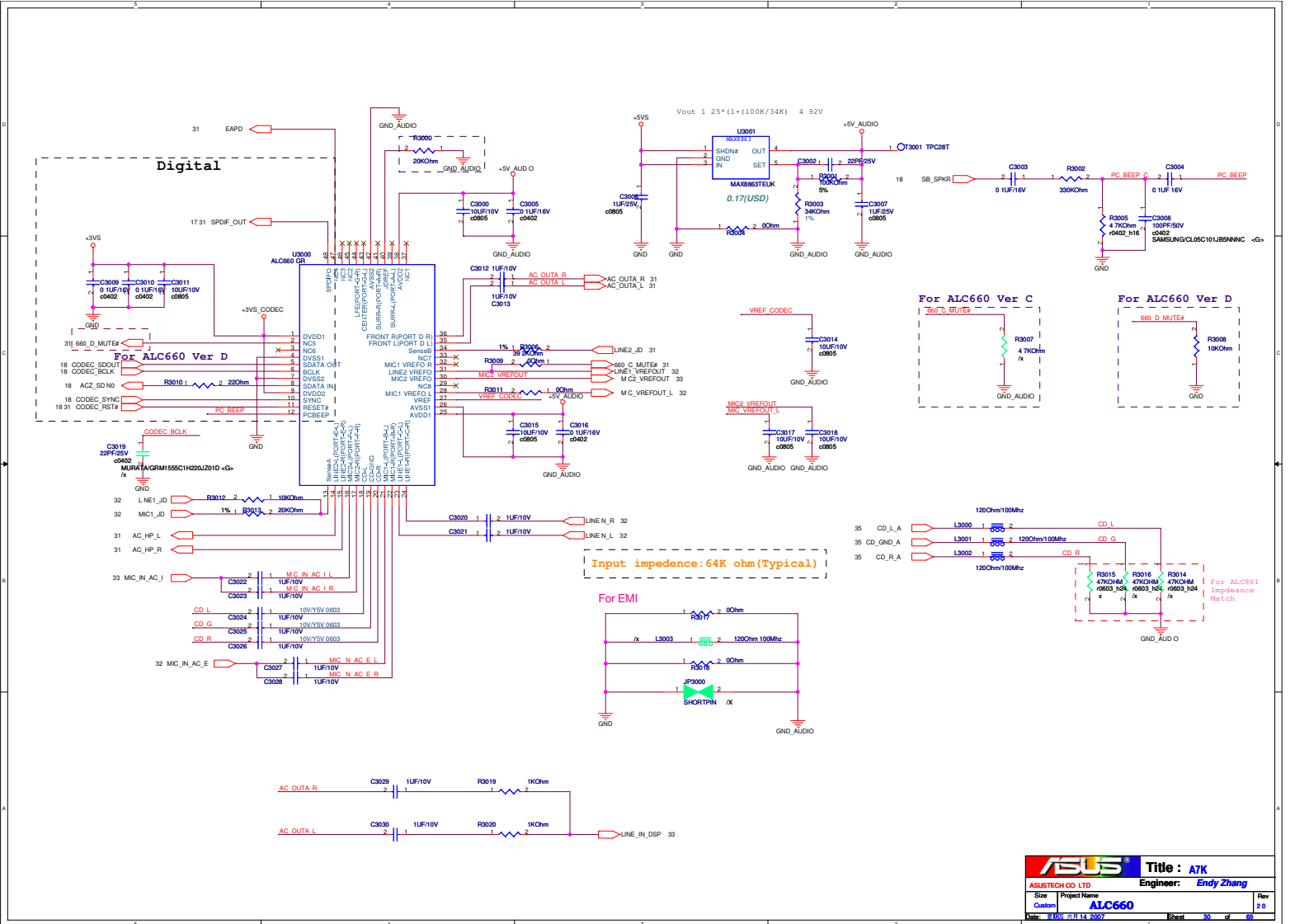


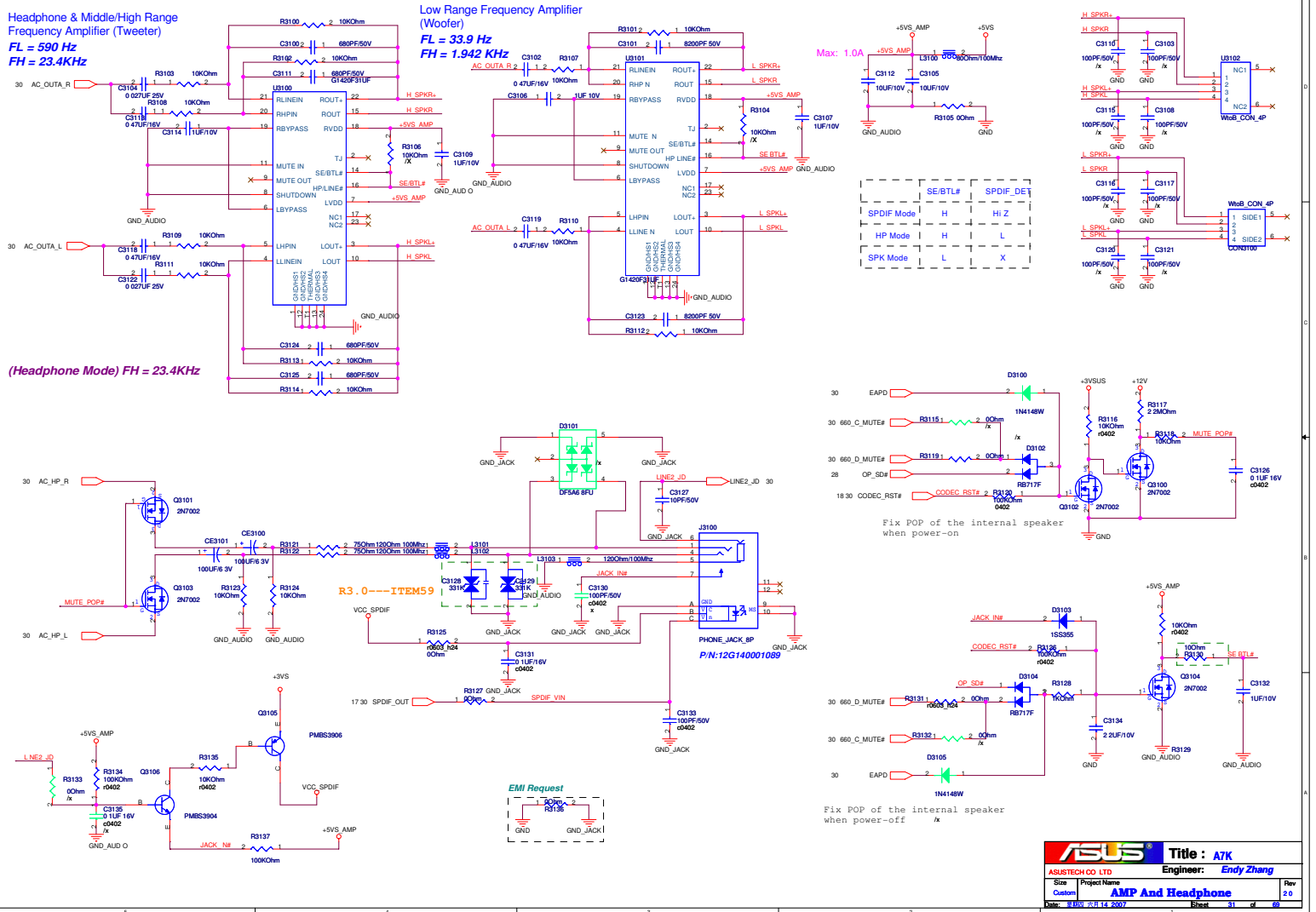


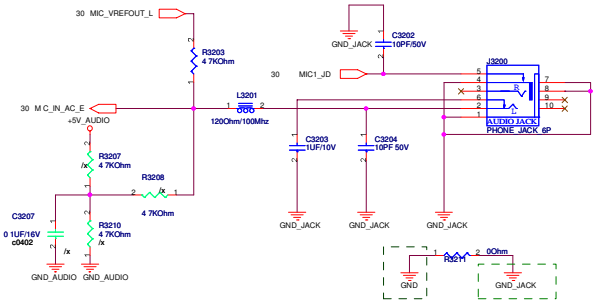
EC Hardware Strap

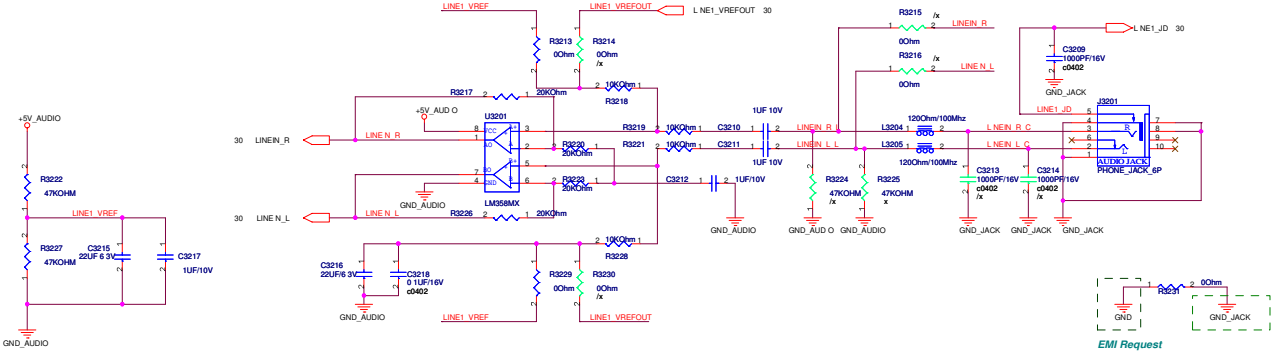
strap value sampled after VSTBY power up reset

ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: EC IT8510E(2/2)		Rev: 2.0
Date: 星期一 六月 11, 2007	Sheet 29 of 69		


Digital
U3000
ALC660 GR
For ALC660 Ver D
For ALC660 Ver C
For ALC660 Ver D
U3001
MAX8863EUK
0.17(USD)
Input impedence:64K ohm(Typical)
For EMI
For ALC861 Impdeance Match
Title : A7K
ASUSTECH CO LTD
Engineer: Endy Zhang
Project Name
ALC660
Rev
2.0
Sheet 30 of 69

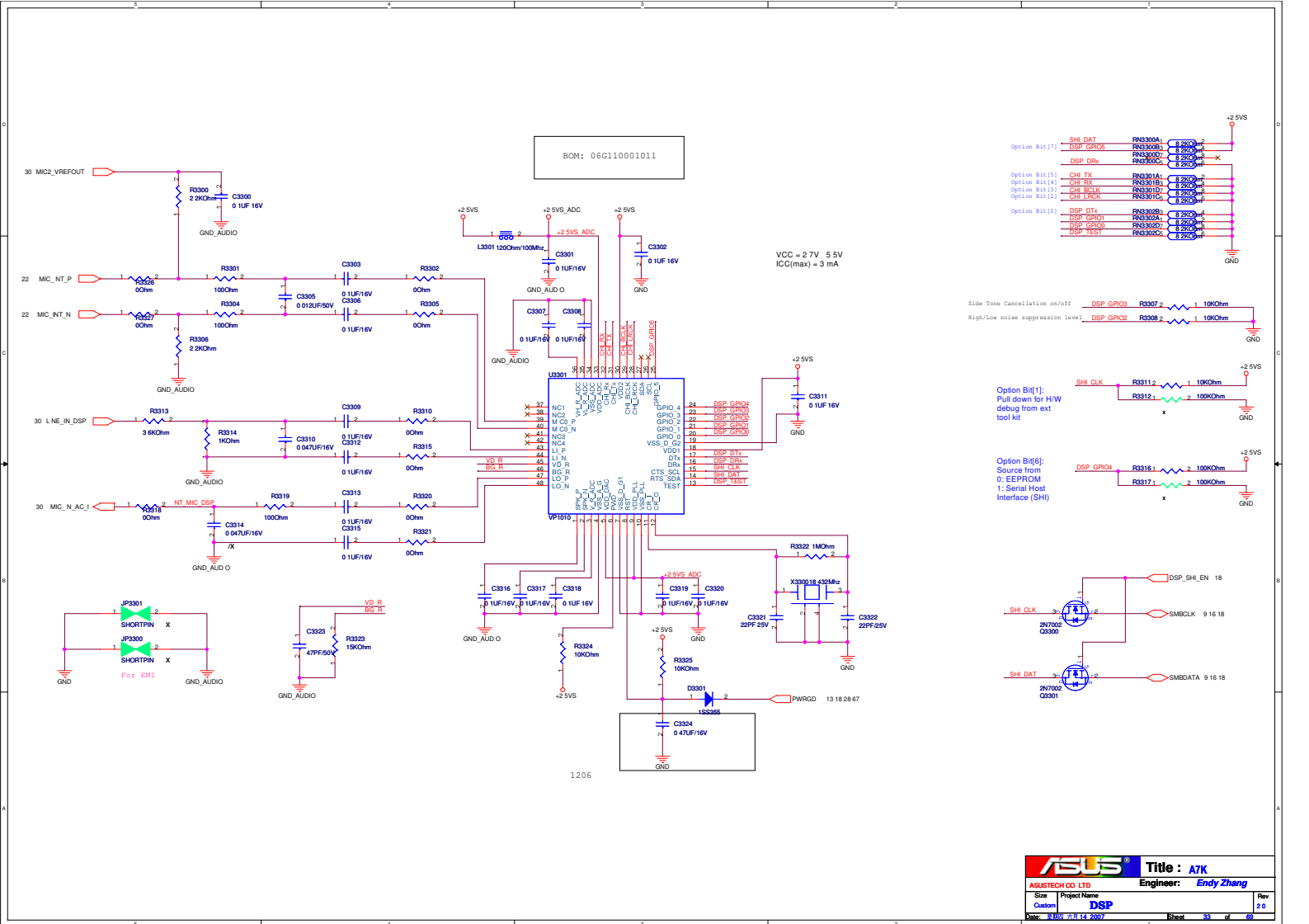

Headphone & Middle/High Range Frequency Amplifier (Tweeter)
FL = 590 Hz
FH = 23.4KHz
Low Range Frequency Amplifier (Woofer)
FL = 33.9 Hz
FH = 1.942 KHz
(Headphone Mode) FH = 23.4KHz
Max: 1.0A
SPDIF Mode
HP Mode
SPK Mode
SE/BTL#
SPDIF_DET
Fix POP of the internal speaker when power-on
Fix POP of the internal speaker when power-off
R3.0---ITEM59
P/N:12G140001089
EMI Request
ASUSTECH CO LTD
Engineer: Endy Zhang
Title : A7K
AMP And Headphone
Rev 2.0
Sheet 31 of 69





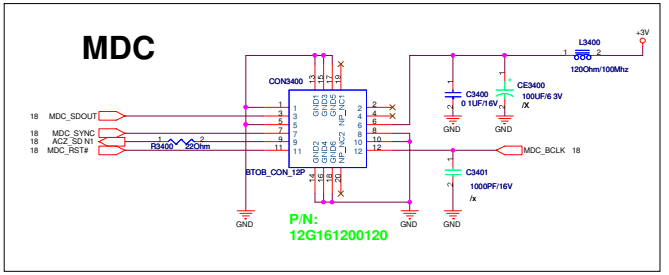
ASUSTECH CO LTD		Engineer:	Endy Zhang
Size: Custom	Project Name: MIC And Line in		Rev: 2.0
Date: 星期四 六月 14 2007		Sheet 32 of 69	

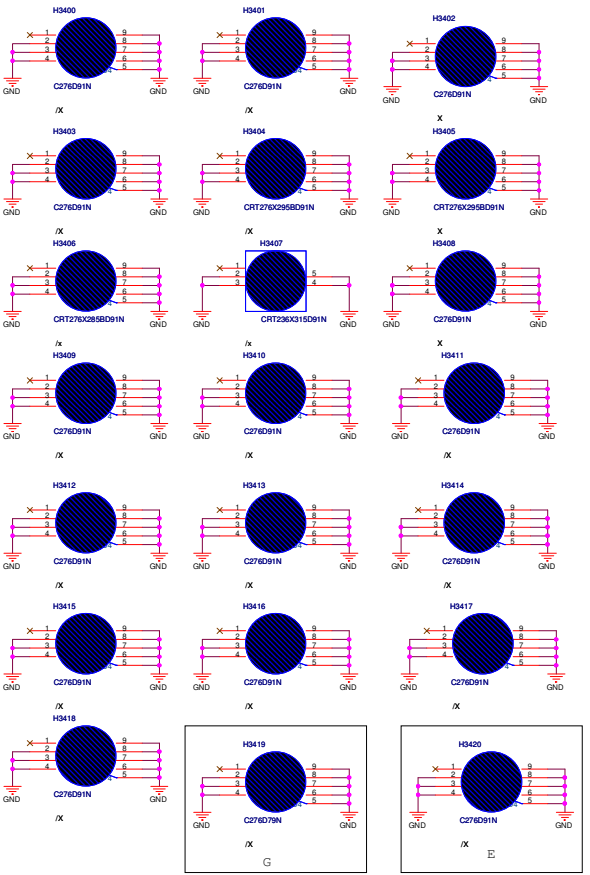
Title : A7K

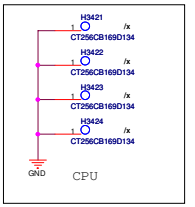


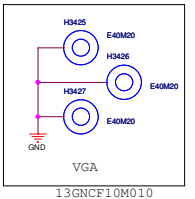
1206

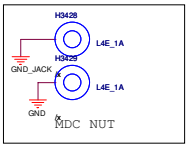
ASUSTEK CO LTD	Title : A7K	
	Engineer: Endy Zhang	
Size: Custom	Project Name: DSP	Rev: 2 0
Date: 星期四 六月 14 2007	Sheet 33 of 69	

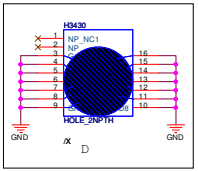




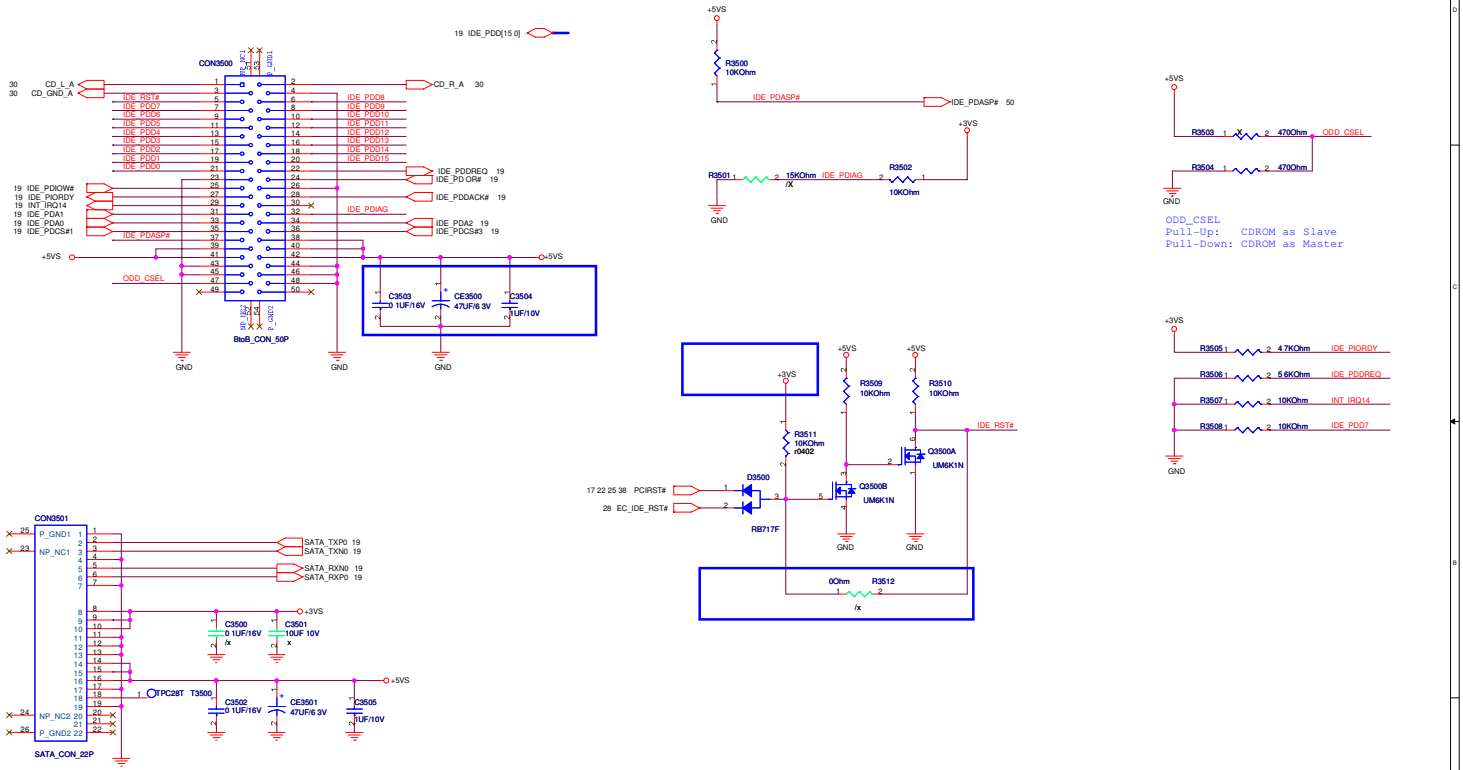




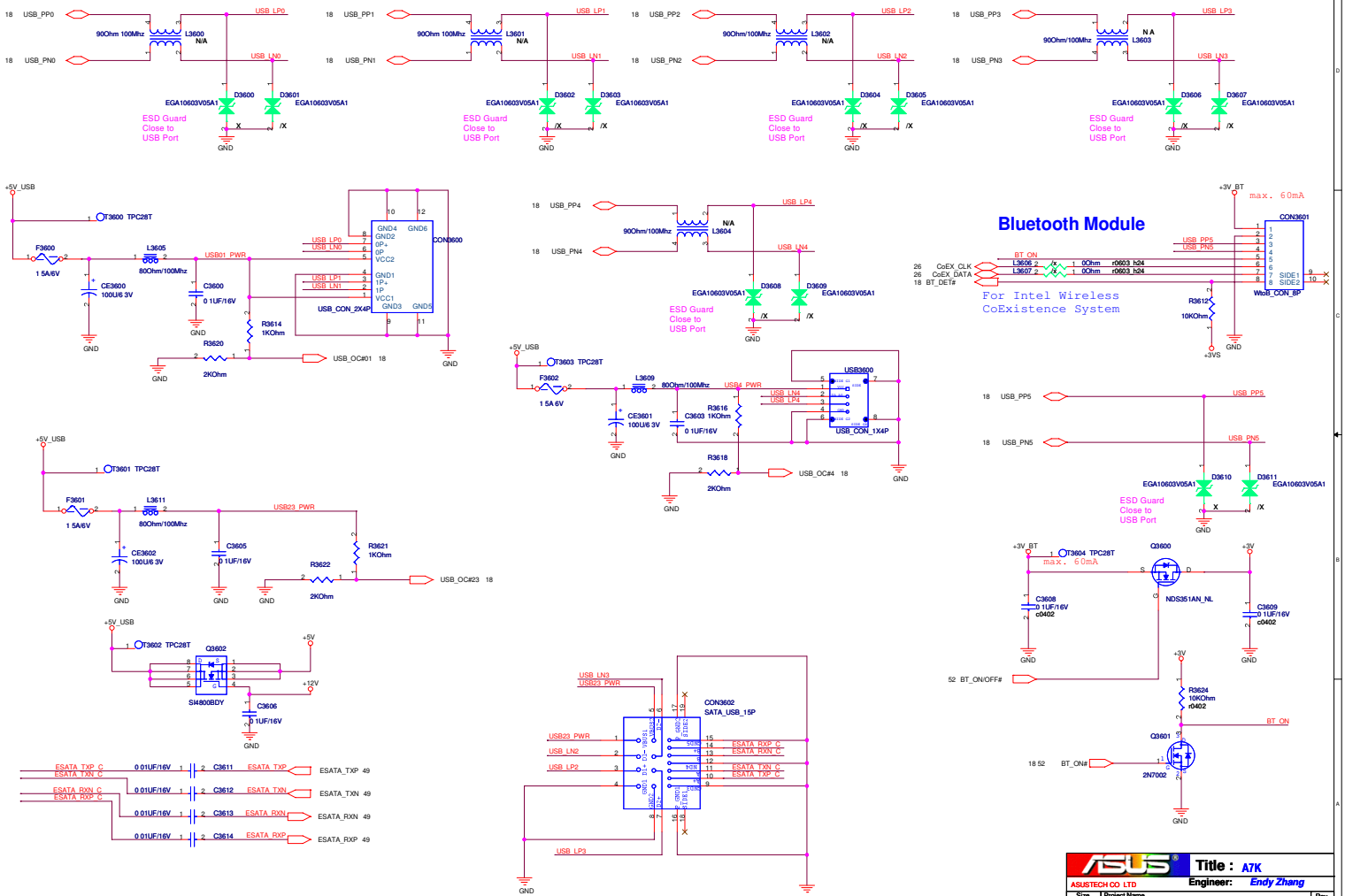


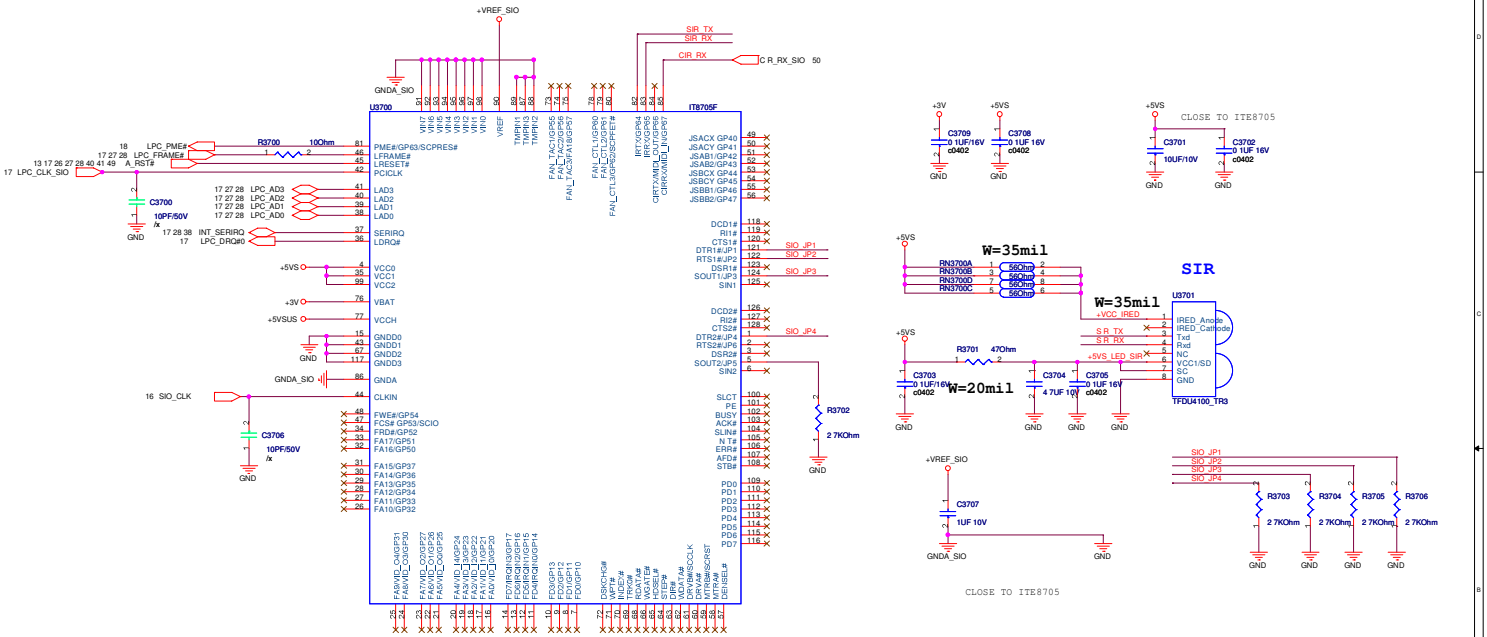


ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: MDC		Rev: 2.0
Date: 星期四 十月 14, 2007		Sheet 34 of 69	

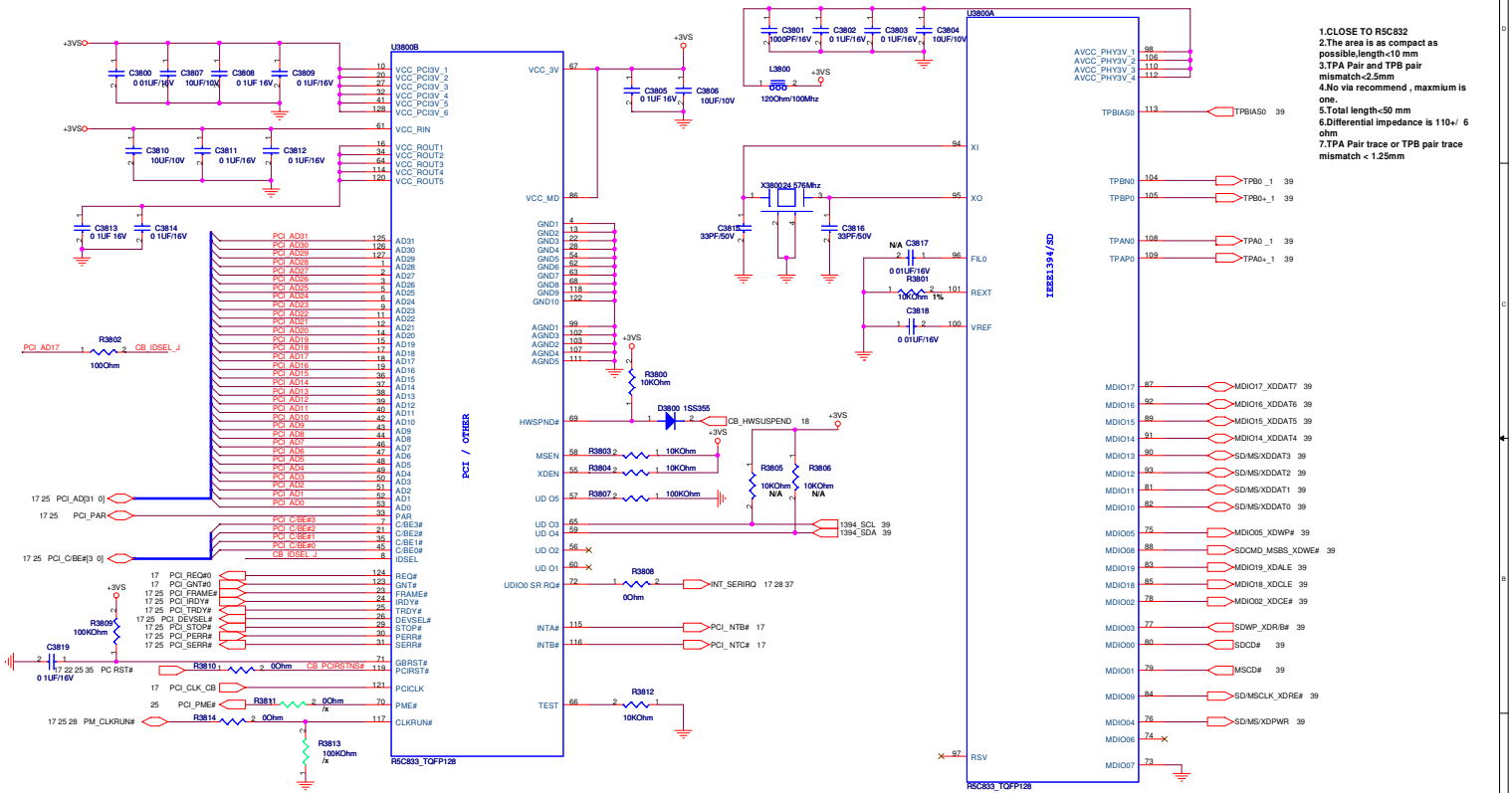


ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: HDD And ODD		Rev: 2.0
Date: 星期四 六月 14 2007	Sheet 35 of 69		


18 USB_PP0
18 USB_PN0
90Ohm 100Mhz
L3600
N/A
USB_LP0
USB_LN0
D3600
D3601
EGA10603V05A1
ESD Guard Close to USB Port
GND
18 USB_PP1
18 USB_PN1
L3601
USB_LP1
USB_LN1
D3602
D3603
18 USB_PP2
18 USB_PN2
90Ohm/100Mhz
L3602
USB_LP2
USB_LN2
D3604
D3605
18 USB_PP3
18 USB_PN3
L3603
USB_LP3
USB_LN3
D3606
D3607
+5V_USB
T3600 TPC28T
F3600
1 5A/6V
L3605
80Ohm/100Mhz
USB01_PWR
CE3600
100U/6 3V
C3600
0 1UF/16V
R3614
1KOhm
R3620
2KOhm
USB_OC#01 18
USB_CON_2X4P
CON3600
GND4
GND2
0P+
0P
VCC2
GND1
1P+
1P
VCC1
GND3
GND5
GND6
T3603 TPC28T
F3602
1 5A 6V
L3609
80Ohm/100Mhz
USB4_PWR
CE3601
100U/6 3V
C3603
0 1UF/16V
R3616
1KOhm
R3618
2KOhm
USB_OC#4 18
USB3600
USB_CON_1X4P
T3601 TPC28T
F3601
1 5A/6V
L3611
80Ohm/100Mhz
USB23_PWR
CE3602
100U/6 3V
C3605
0 1UF/16V
R3622
2KOhm
R3621
1KOhm
USB_OC#23 18
T3602 TPC28T
Q3602
SI4800BDY
+5V
+12V
C3606
0 1UF/16V
ESATA_TXP_C
ESATA_TXN_C
ESATA_RXP_C
ESATA_RXN_C
0.01UF/16V
C3611
C3612
C3613
C3614
ESATA_TXP
ESATA_TXN
ESATA_RXN
ESATA_RXP
ESATA_TXP 49
ESATA_TXN 49
ESATA_RXN 49
ESATA_RXP 49
18 USB_PP4
18 USB_PN4
L3604
USB_LP4
USB_LN4
D3608
D3609
USB_LN3
USB23_PWR
USB_LN2
USB_LP2
USB_LP3
CON3602
SATA_USB_15P
Bluetooth Module
+3V_BT
max. 60mA
T3604 TPC28T
CON3601
BT_ON
26 CoEX_CLK
26 CoEX_DATA
18 BT_DET#
L3606
L3607
0Ohm r0603_h24
USB_PP5
USB_PN5
R3612
10KOhm
+3VS
Wis8_CON_BP
For Intel Wireless CoExistence System
Q3600
NDS351AN_NL
C3608
0 1UF/16V
c0402
C3609
0 1UF/16V
c0402
52 BT_ON/OFF#
R3624
10KOhm
r0402
BT_ON
Q3601
2N7002
18 52 BT_ON#
D3610
D3611
ASUSTEK CO LTD
Title : A7K
Engineer: Endy Zhang
Size: Custom
Project Name: USB Connector and BT
Rev: 2.0
Date: 星期三 六月 13, 2007
Sheet 36 of 69

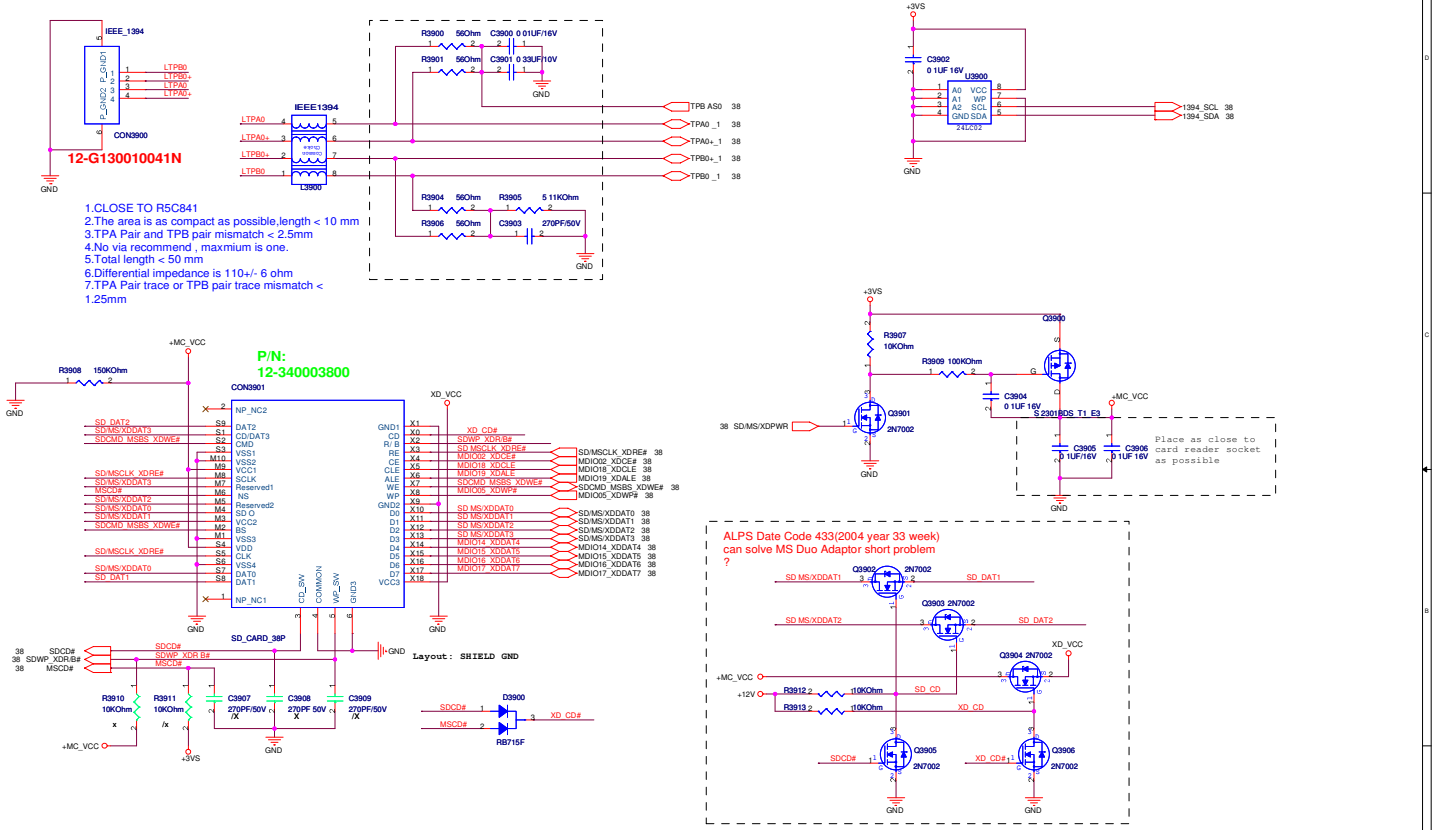


ASUS	Title : A7K		
ASUSTECH CO LTD	Engineer: Endy Zhang		
Size: Custom	Project Name: SIO and SIR		Rev: 2.0
Date: 星期二 六月 19, 2007	Sheet 37 of 69		

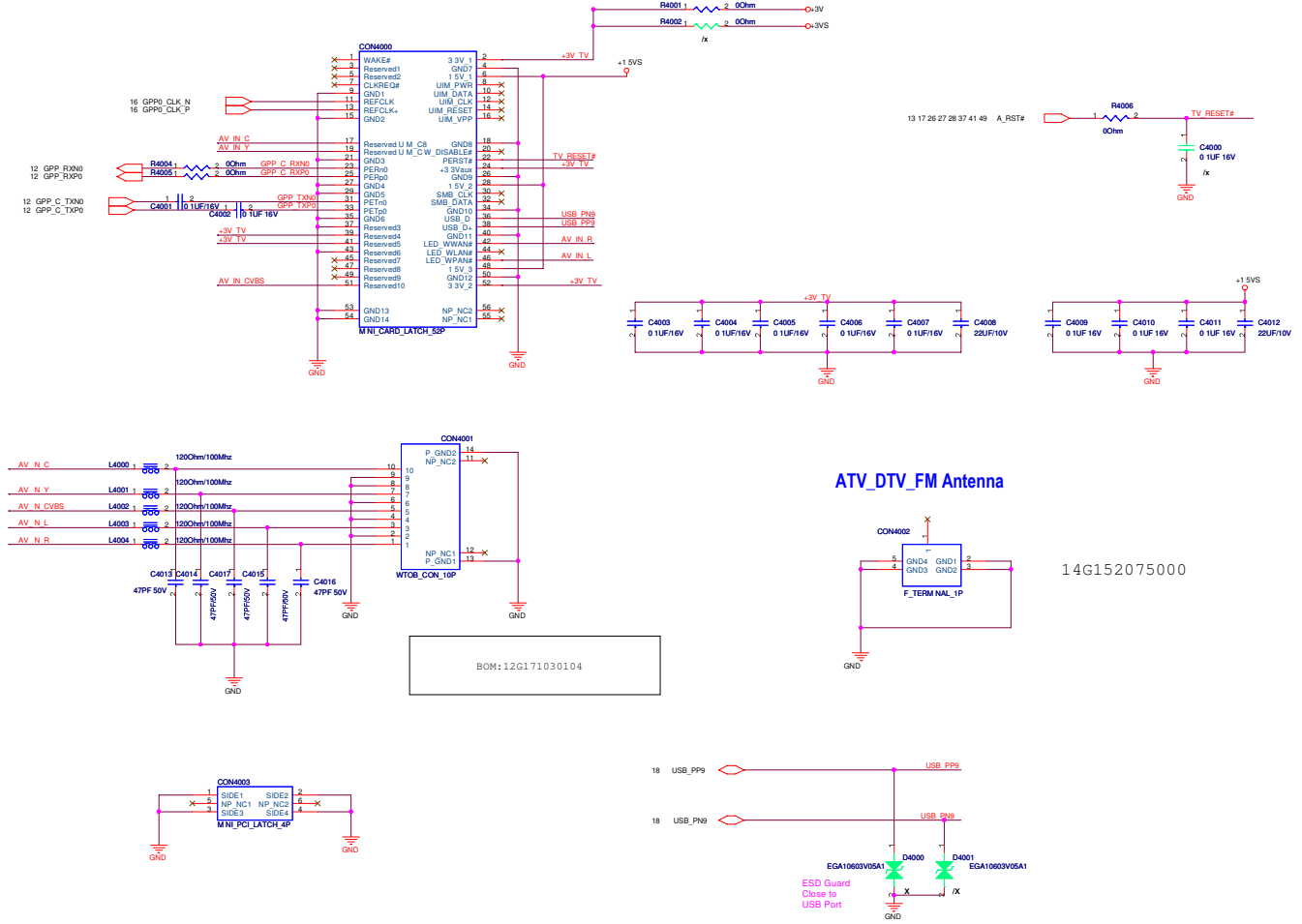


1.CLOSE TO R5C832
2.The area is as compact as possible,length<10 mm
3.TPA Pair and TPB pair mismatch<2.5mm
4.No via recommend , maxmium is one.
5.Total length<50 mm
6.Differential impedance is 110+/ 6 ohm
7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

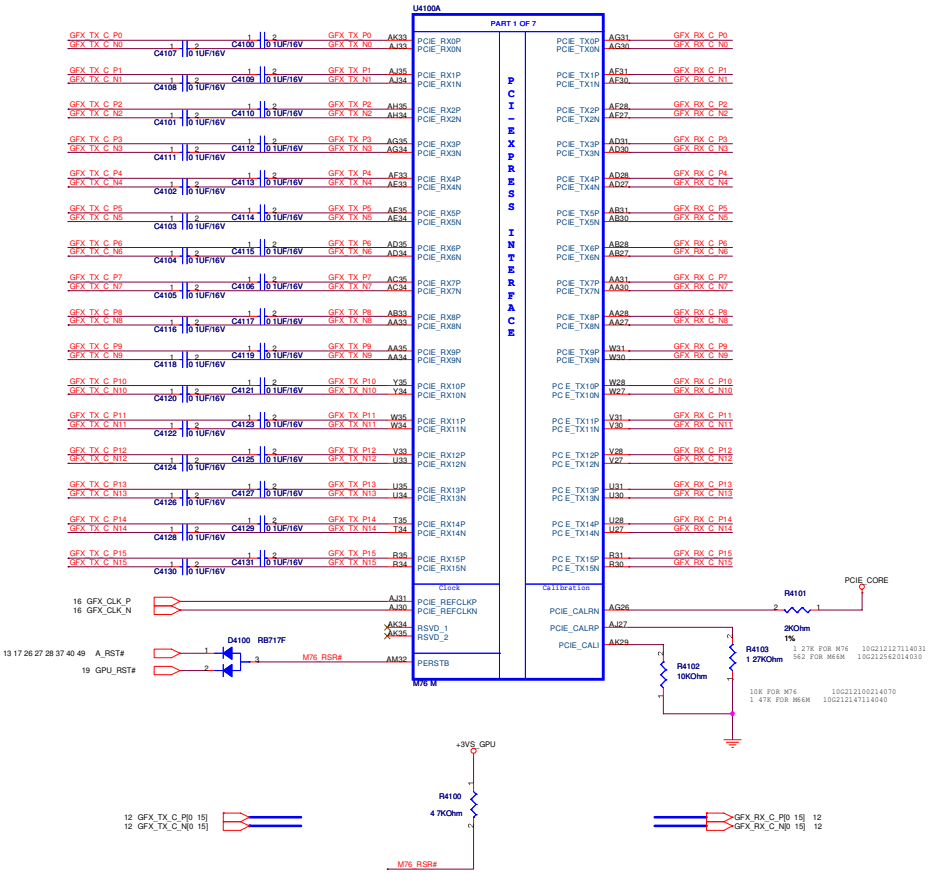
ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: Card Bus R5C832		Rev: 2.0
Date: 星期四 六月 14, 2007	Sheet 38 of 69		



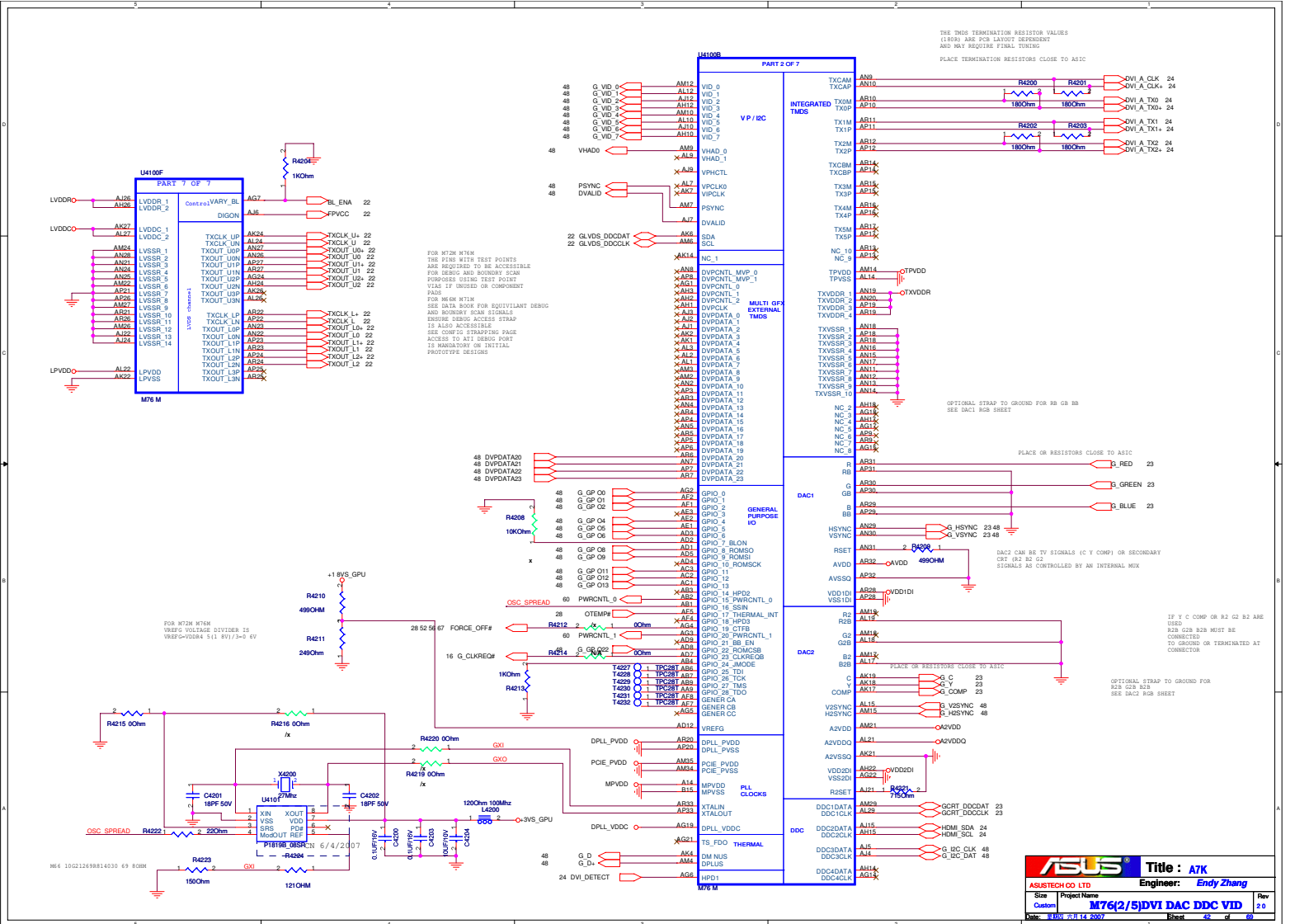
ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: 1394 And Card Reader		Rev: 2 0
Date: 星期四 六月 14 2007	Sheet 39 of 69		

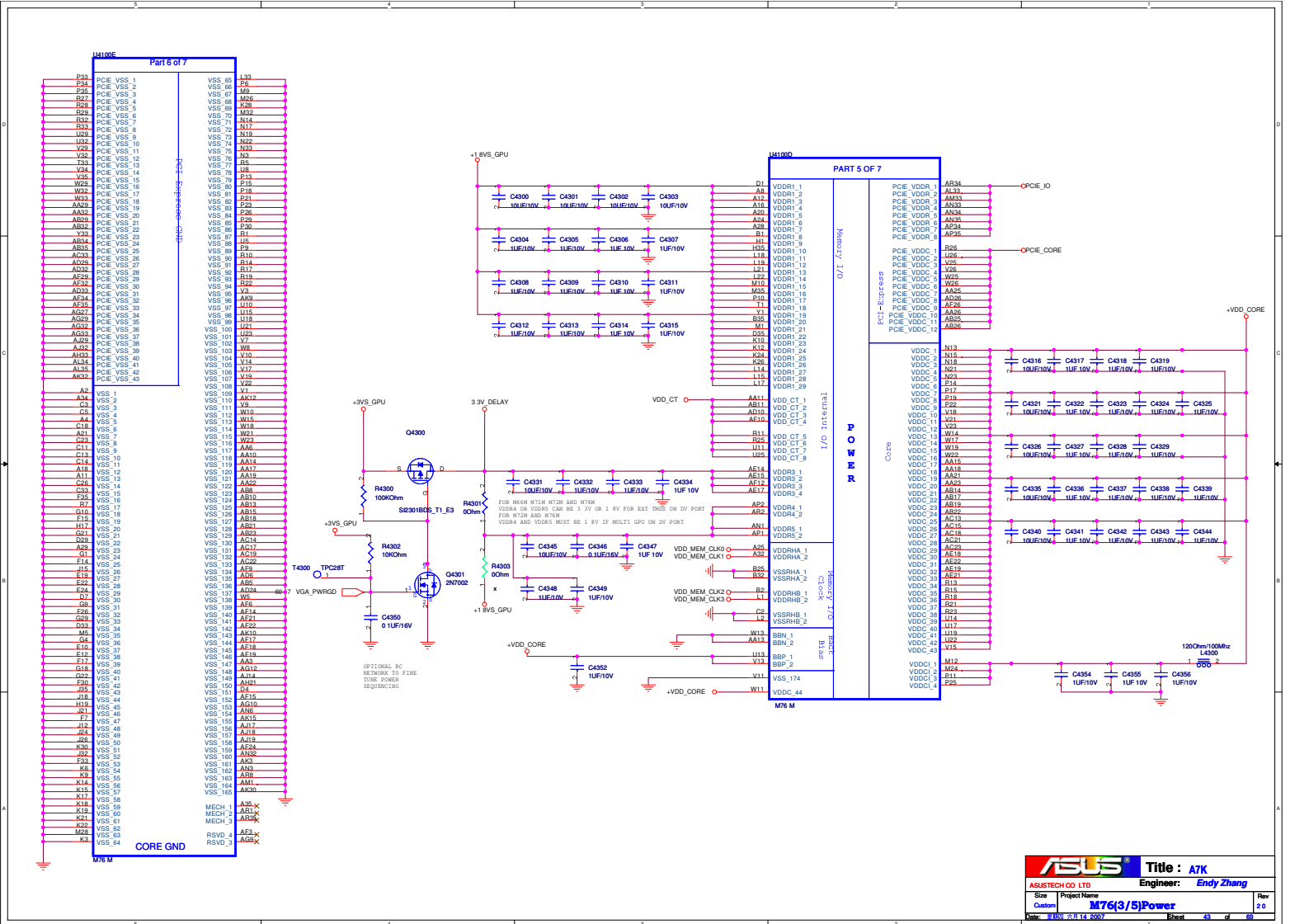


ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: Mini PCIE(TV)		Rev: 2.0
Date: 星期四 六月 14, 2007		Sheet 40 of 69	



ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: M76(1/5)PCIE I/F		Rev: 2.0
Date: 星期四 六月 14 2007	Sheet 41 of 69		

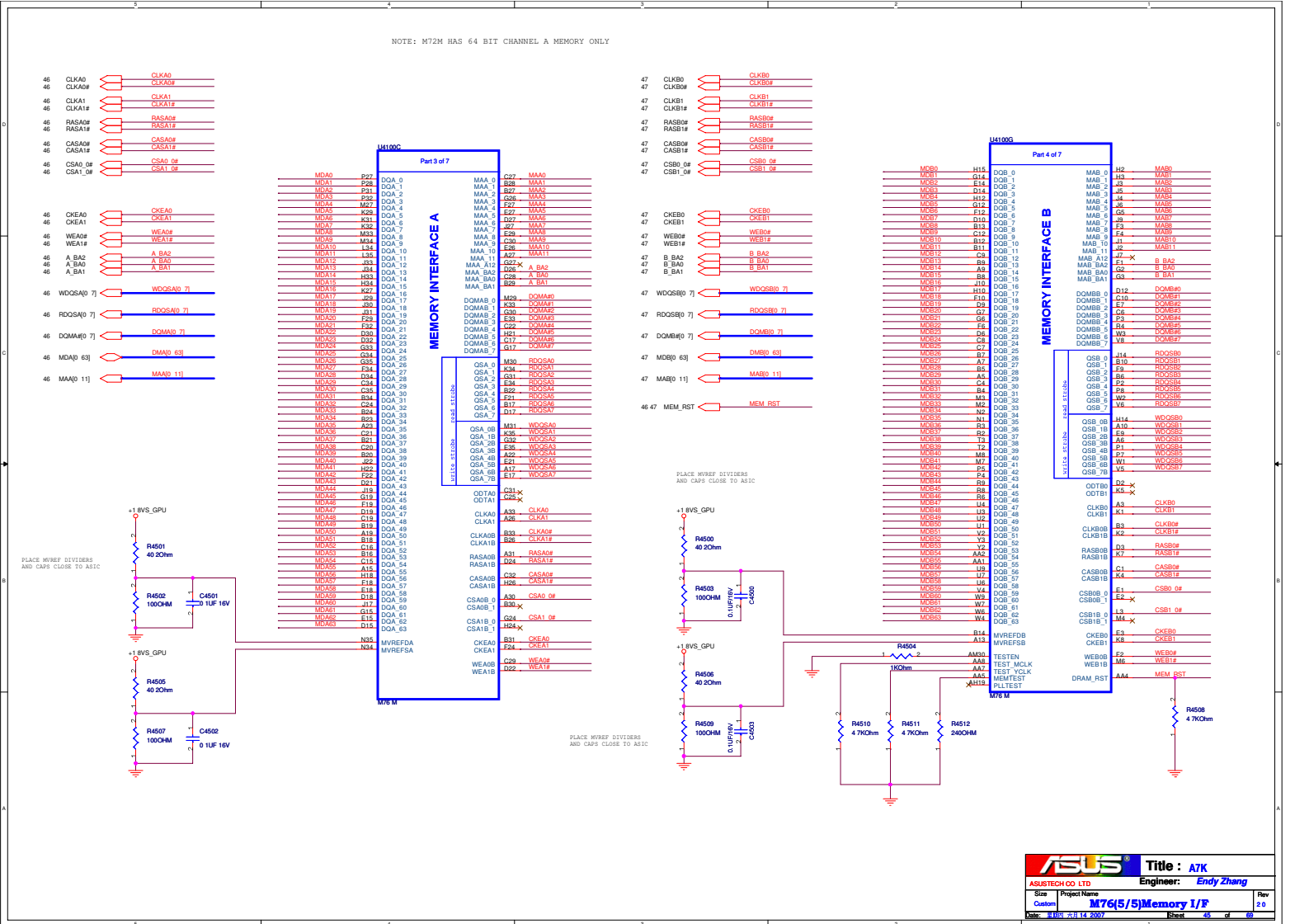

THE TMDS TERMINATION RESISTOR VALUES (180R) ARE PCB LAYOUT DEPENDENT AND MAY REQUIRE FINAL TUNING
PLACE TERMINATION RESISTORS CLOSE TO ASIC
U4100B
PART 2 OF 7
V P / I2C
INTEGRATED TMDS
MULTI GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
PLL CLOCKS
THERMAL
DDC
DAC1
DAC2
U4100F
PART 7 OF 7
M76 M
FOR M72M M76M THE PINS WITH TEST POINTS ARE REQUIRED TO BE ACCESSIBLE FOR DEBUG AND BOUNDRY SCAN PURPOSES USING TEST POINT VIAS IF UNUSED OR COMPONENT PADS FOR M56M M71M SEE DATA BOOK FOR EQUIVILANT DEBUG AND BOUNDRY SCAN SIGNALS ENSURE DEBUG ACCESS STRAP IS ALSO ACCESSIBLE SEE CONFIG STRAPPING PAGE ACCESS TO ATI DEBUG PORT IS MANDATORY ON INITIAL PROTOTYPE DESIGNS
OPTIONAL STRAP TO GROUND FOR RB GB BB SEE DAC1 RGB SHEET
PLACE OR RESISTORS CLOSE TO ASIC
DAC2 CAN BE TV SIGNALS (C Y COMP) OR SECONDARY CRT (R2 B2 G2 SIGNALS AS CONTROLLED BY AN INTERNAL MUX
IF Y C COMP OR R2 G2 B2 ARE USED R2B G2B B2B MUST BE CONNECTED TO GROUND OR TERMINATED AT CONNECTOR
OPTIONAL STRAP TO GROUND FOR R2B G2B B2B SEE DAC2 RGB SHEET
FOR M72M_M76M VREFG VOLTAGE DIVIDER IS VREFG=VDDR4 5(1 8V)/3=0 6V
+1 8VS_GPU
X4200 27MHz
U4100
P1819B_08SR
ASUSTECH CO LTD
Title : A7K
Engineer: Endy Zhang
Size: Custom
Project Name: M76(2/5)DVI DAC DDC VID
Rev: 2 0
Date: 星期四 六月 14 2007
Sheet 42 of 69



ASUS	Title : A7K		
ASUSTECH CO LTD	Engineer: Endy Zhang		
Size: Custom	Project Name: M76(3/5)Power		Rev: 2.0
Date: 星期四 六月 14 2007	Sheet 43 of 69		

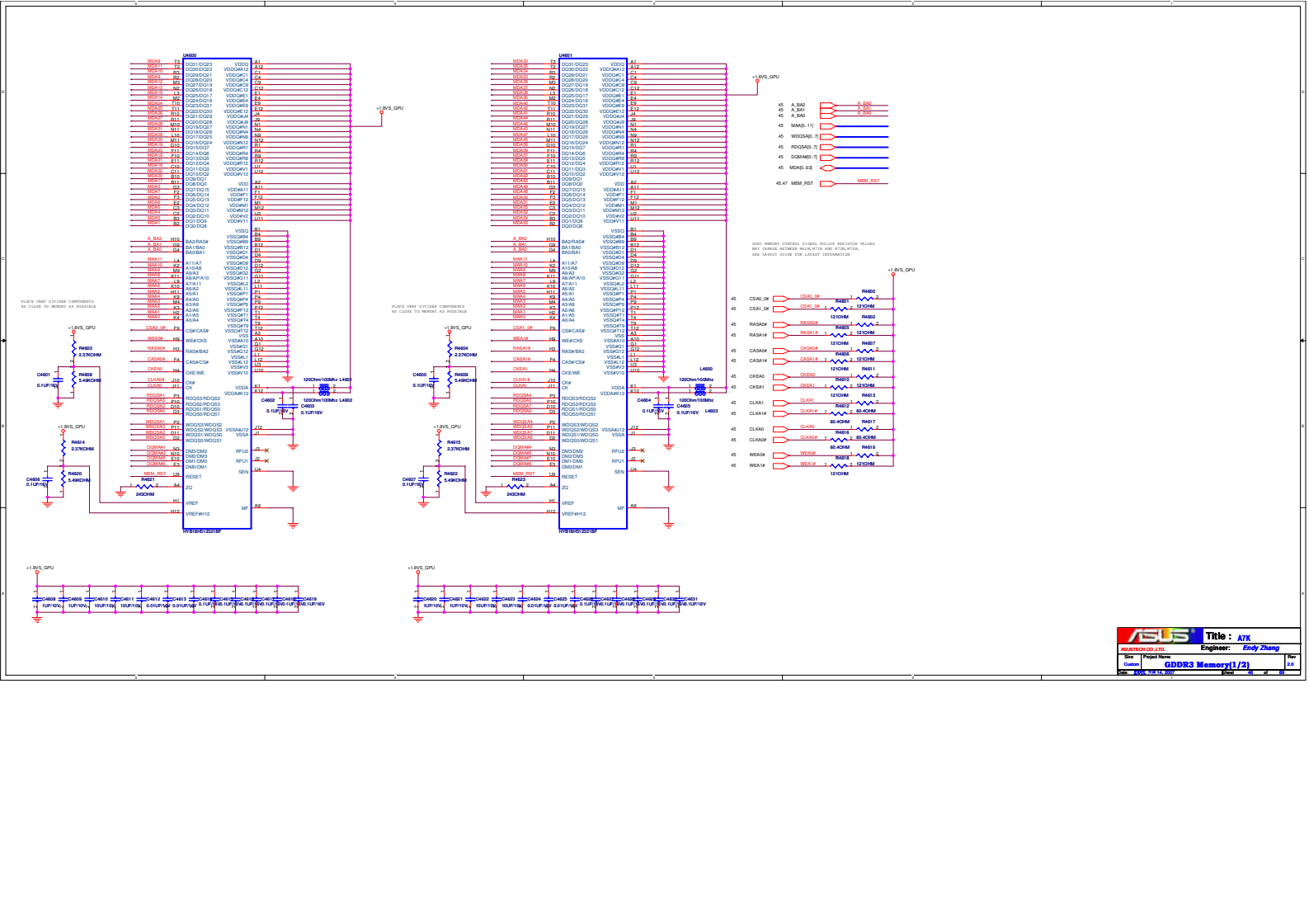
ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: <Doc>		Rev: 2.0
Date: 星期日 六月 14 2007		Sheet 44 of 69	

NOTE: M72M HAS 64 BIT CHANNEL A MEMORY ONLY



ASUSTECH CO LTD	Engineer: Endy Zhang
Size: Custom	Project Name: M76(5/5)Memory I/F
Rev: 2.0	
Date: 星期一 六月 14, 2007	Sheet 45 of 69

Title : A7K

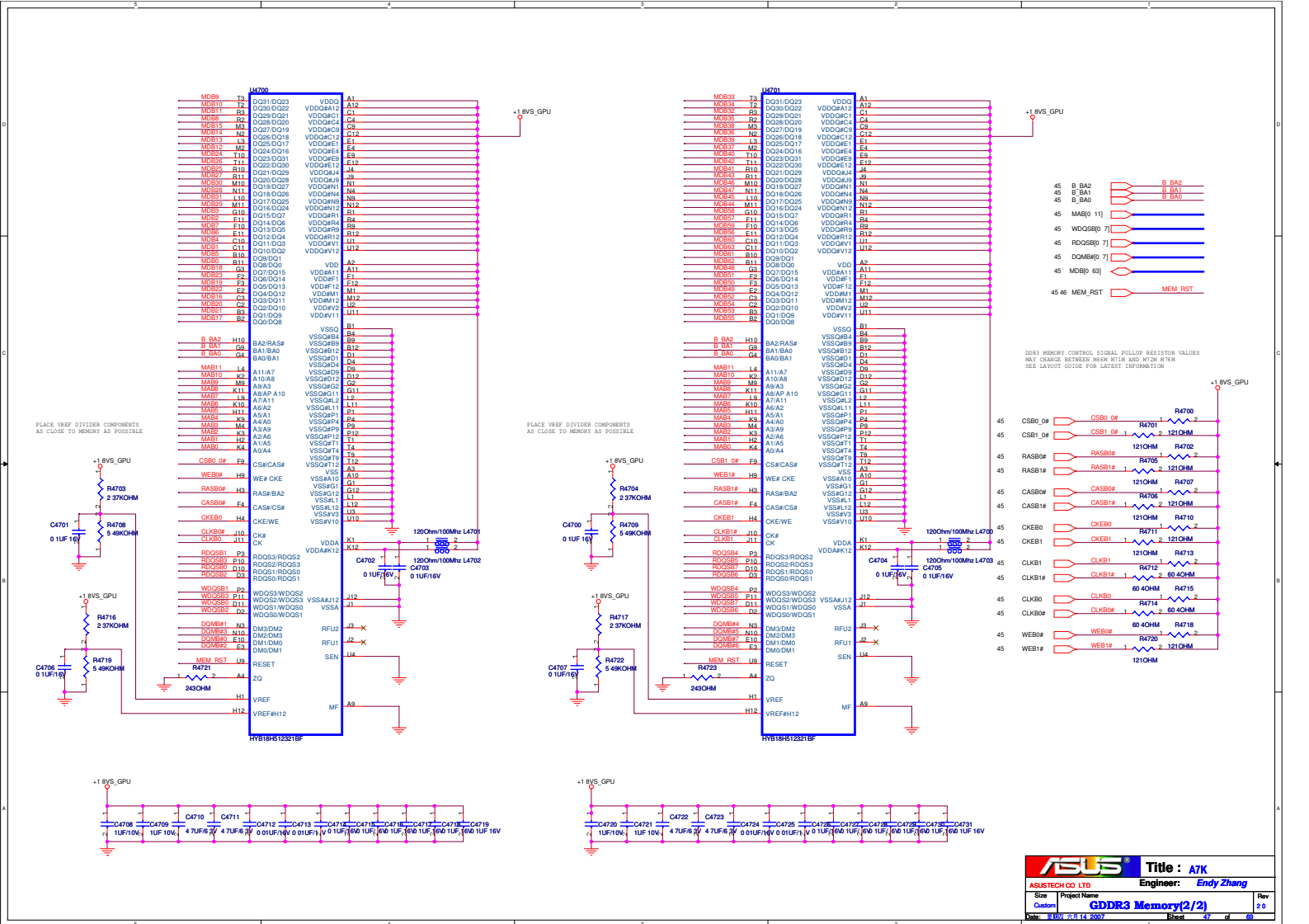


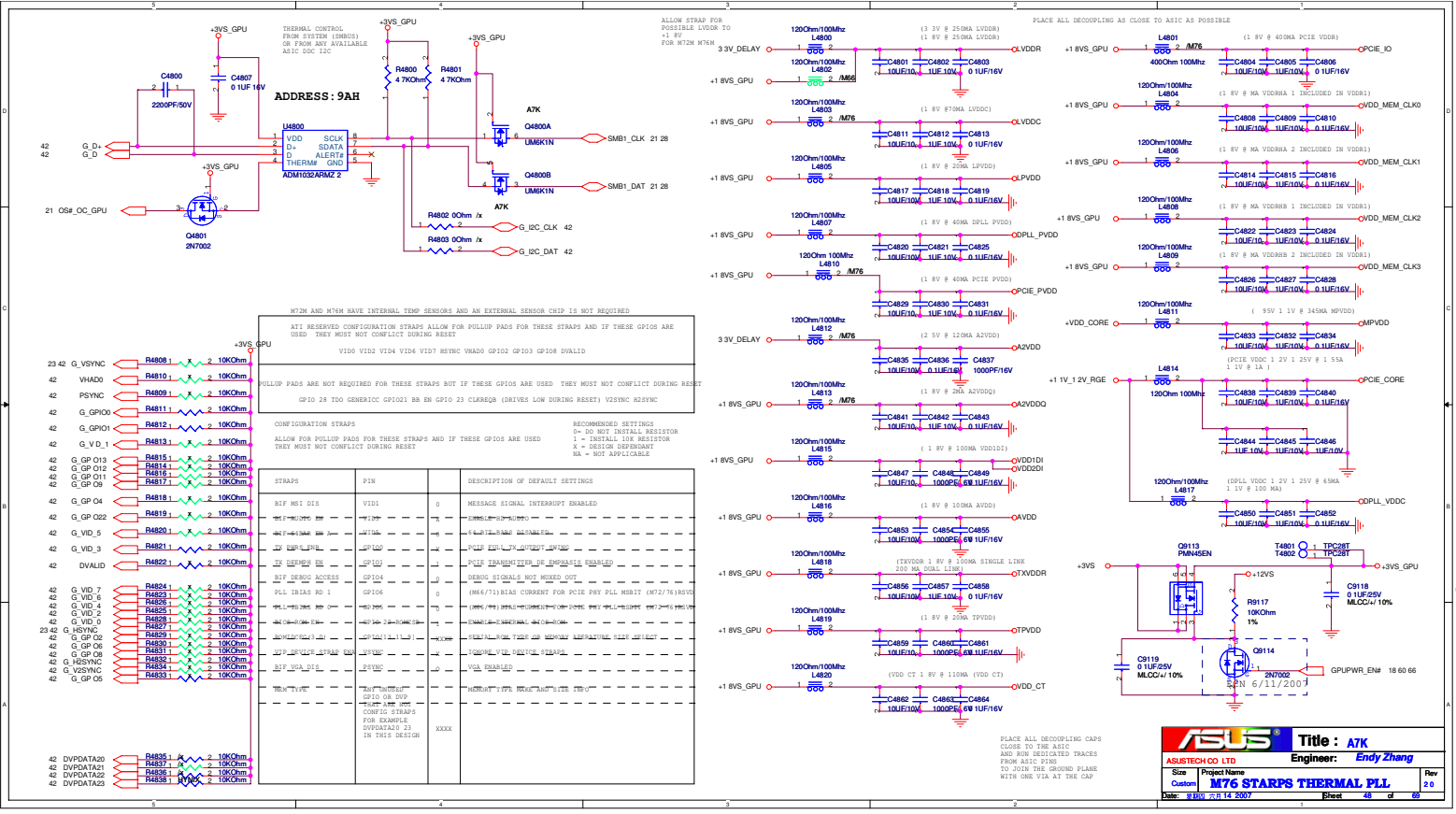
Size	Project Name		Rev
Custom	GDDR3 Memory(1/2)		2.0
Date:	Sheet	of	

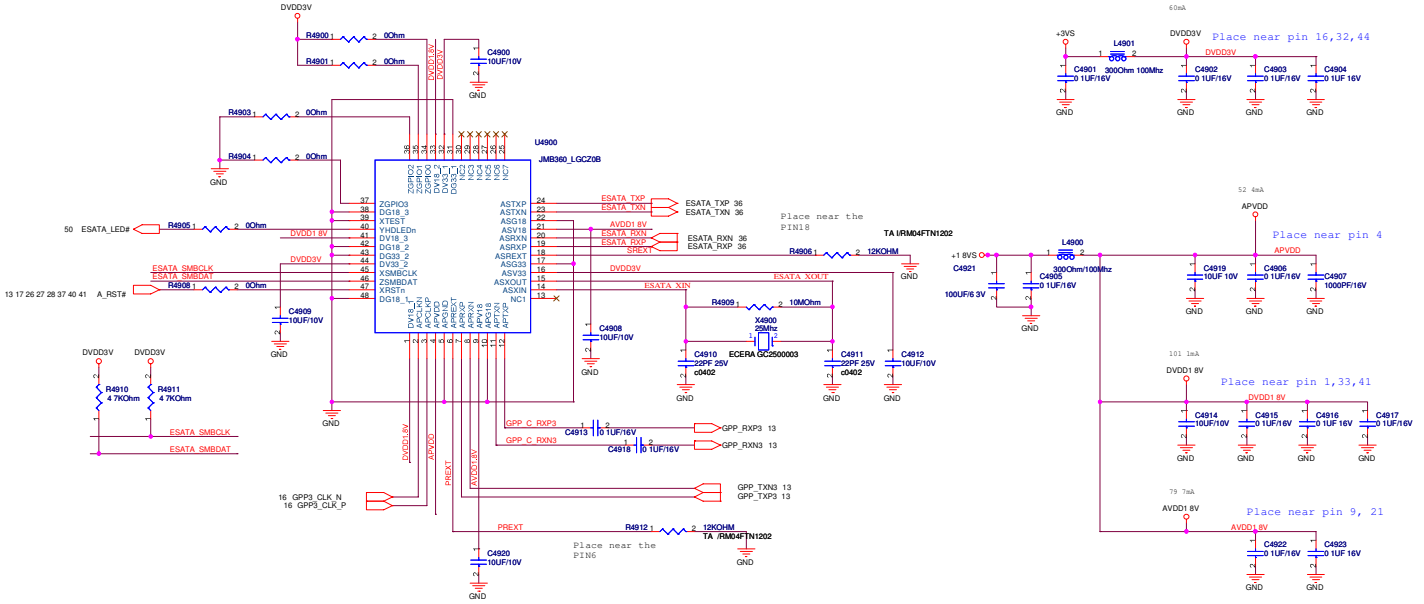
ASUSTeK COMPUTER INC.

Title : A7K

Engineer: Endy Zhang


U4700
U4701
HY5PS1G831FP-Y5
+1.8VS_GPU
PLACE VREF DIVIDER COMPONENTS AS CLOSE TO MEMORY AS POSSIBLE
DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES MAY CHANGE BETWEEN M66M M71M AND M72M M76M SEE LAYOUT GUIDE FOR LATEST INFORMATION
B_BA2
B_BA1
B_BA0
MAB[0 11]
WDQSB[0 7]
RDQSB[0 7]
DQMB[0 7]
MDB[0 63]
MEM_RST
CSB0_0#
CSB1_0#
RASB0#
RASB1#
CASB0#
CASB1#
CKEB0
CKEB1
CLKB1
CLKB1#
CLKB0
CLKB0#
WEB0#
WEB1#
120Ohm/100Mhz L4700
120Ohm/100Mhz L4701
120Ohm/100Mhz L4702
120Ohm/100Mhz L4703
120Ohm/100Mhz L4704
120Ohm/100Mhz L4705
R4700 121OHM
R4701 121OHM
R4702 121OHM
R4705 121OHM
R4707 121OHM
R4706 121OHM
R4710 121OHM
R4711 121OHM
R4713 121OHM
R4712 60.4OHM
R4715 60.4OHM
R4714 60.4OHM
R4718 60.4OHM
R4720 121OHM
R4703 2.37KOHM
R4704 2.37KOHM
R4716 2.37KOHM
R4717 2.37KOHM
R4708 5.49KOHM
R4709 5.49KOHM
R4719 5.49KOHM
R4722 5.49KOHM
R4721 243OHM
R4723 243OHM
C4700 0 1UF/16V
C4701 0 1UF/16V
C4702 0 1UF/16V
C4703 0 1UF/16V
C4704 0 1UF/16V
C4705 0 1UF/16V
C4706 0 1UF/16V
C4707 0 1UF/16V
C4706 1UF/10V
C4709 1UF 10V
C4710 4.7UF/6.3V
C4711 4.7UF/6.3V
C4712 0.01UF/16V
C4713 0.01UF/16V
C4714 0.1UF/16V
C4715 1UF/6.3V
C4716 1UF/6.3V
C4717 1UF/6.3V
C4719 1UF/6.3V
C4720 1UF/10V
C4721 1UF 10V
C4722 4.7UF/6.3V
C4723 4.7UF/6.3V
C4724 0.01UF/16V
C4725 0.01UF/16V
C4726 0.1UF/16V
C4727 1UF/6.3V
C4728 1UF/6.3V
C4729 1UF/6.3V
C4730 1UF/6.3V
C4731 1UF/6.3V
Title : A7K
ASUSTECH CO LTD
Engineer: Endy Zhang
Size: Custom
Project Name: GDDR3 Memory(2/2)
Rev: 2.0
Date: 星期四 六月 14, 2007
Sheet 47 of 69


THERMAL CONTROL FROM SYSTEM (SMBUS) OR FROM ANY AVAILABLE ASIC DDC I2C
ADDRESS : 9AH
U4800
ADM1032ARMZ 2
Q4800A
Q4800B
UM6K1N
A7K
SMB1_CLK 21 28
SMB1_DAT 21 28
G_I2C_CLK 42
G_I2C_DAT 42
Q4801
2N7002
21 OS#_OC_GPU
M72M AND M76M HAVE INTERNAL TEMP SENSORS AND AN EXTERNAL SENSOR CHIP IS NOT REQUIRED
ATI RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED THEY MUST NOT CONFLICT DURING RESET
VID0 VID2 VID4 VID6 VID7 H5YNC VHAD0 GPIO2 GPIO3 GPIO8 DVALID
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED THEY MUST NOT CONFLICT DURING RESET
GPIO 28 TDO GENERICC GPIO21 BB EN GPIO 23 CLKREQB (DRIVES LOW DURING RESET) V2SYNC H2SYNC
CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED THEY MUST NOT CONFLICT DURING RESET
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
STRAPS
PIN
DESCRIPTION OF DEFAULT SETTINGS
BIF MSI DIS
VID1
MESSAGE SIGNAL INTERRUPT ENABLED
PLL IBIAS RD 1
GPIO6
(M66/71)BIAS CURRENT FOR PCIE PHY PLL MSBIT (M72/76)RSVD
BIF VGA DIS
H5YNC
VGA ENABLED
IGNORE VID DEVICE STRAPS
CONFIG STRAPS FOR EXAMPLE DVPDATA20 23 IN THIS DESIGN
XXXX
ALLOW STRAP FOR POSSIBLE LVDDR TO +1 8V FOR M72M M76M
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE
PLACE ALL DECOUPLING CAPS CLOSE TO THE ASIC AND RUN DEDICATED TRACES FROM ASIC PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT THE CAP
Title : A7K
ASUSTECH CO LTD
Engineer: Endy Zhang
Size: Custom
Project Name: M76 STARPS THERMAL PLL
Rev: 2 0
Date: 星期 六月 14, 2007
Sheet 46 of 69



ASUSTECH CO LTD	Title : A7K		
	Engineer: Endy Zhang		
Size: Custom	Project Name: E-SATA		Rev: 2.0
Date: 星期四 六月 14 2007	Sheet 49 of 69		

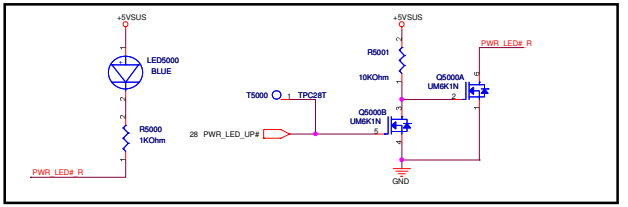
A7K TOP VIEW

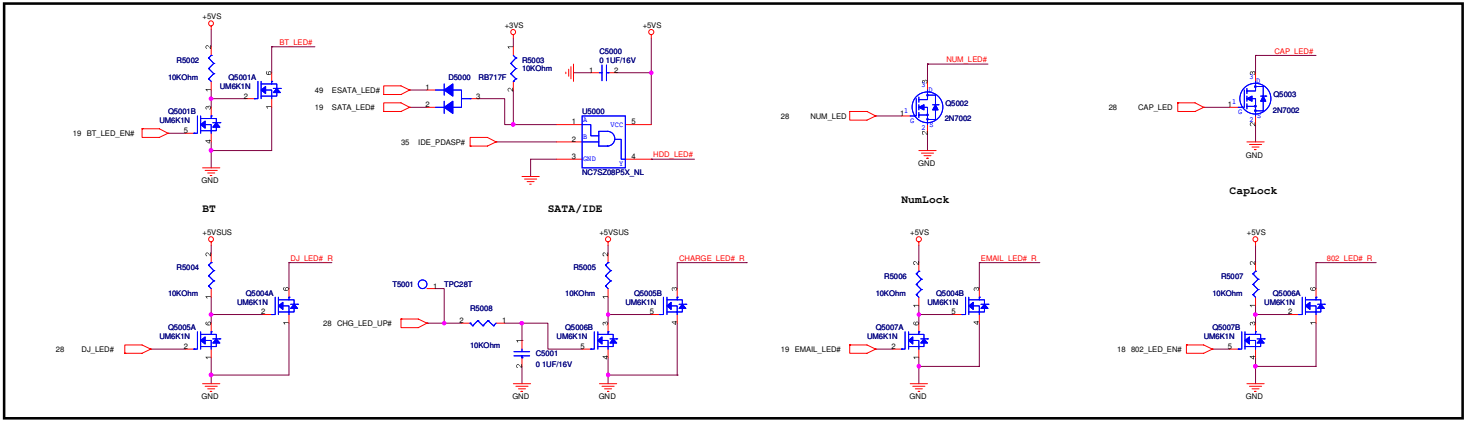
LED	LED	LED	LED	SW	SW	SW	SW
BT	SATA/IDE	NumLock	CapLock	MARATHON	P4PHONE	CLOREN	DISTP

SW	LED	SW	SW	SW	SW	LED	LED	LED	LED
DJ	DJ	BWARD	FWARD	STOP	PLAY	POWER	CHARGE	EMAIL	WLAN

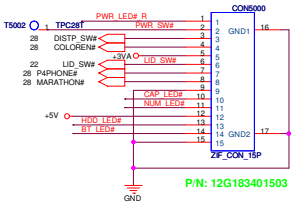
PWR_SW

POWER



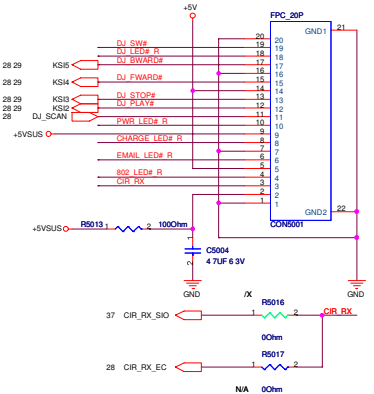


Launch Board Conn.

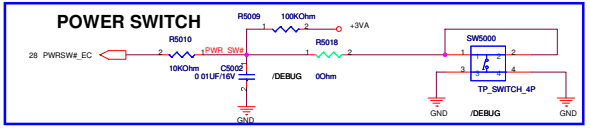


P/N: 12G183401503

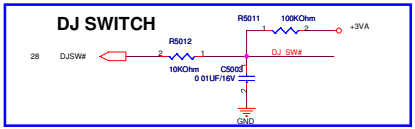
DJ Board Conn.



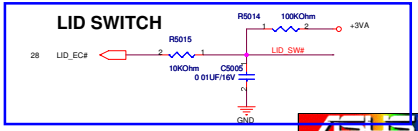
POWER SWITCH



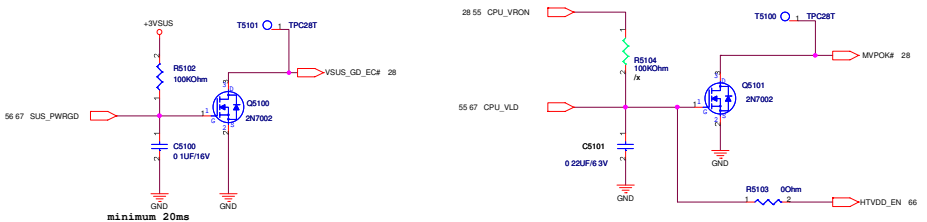
DJ SWITCH



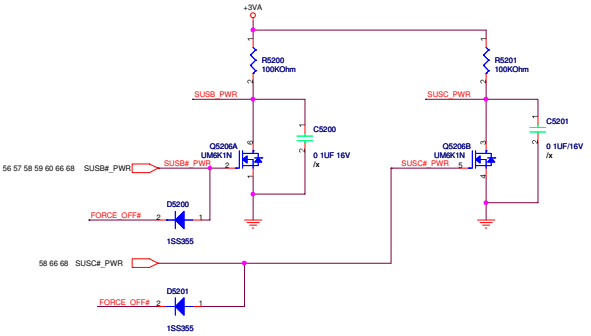
LID SWITCH

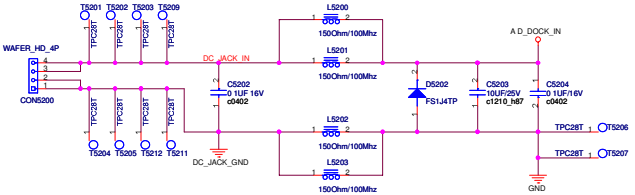


ASUSTECH CO LTD	Title : A7K	
	Engineer: Endy Zhang	
Size: Custom	Project Name: Function Key	Rev: 2.0
Date: 星期一 六月 11, 2007	Sheet 50 of 69	

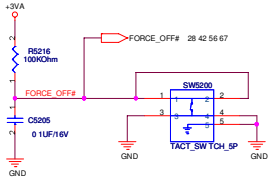


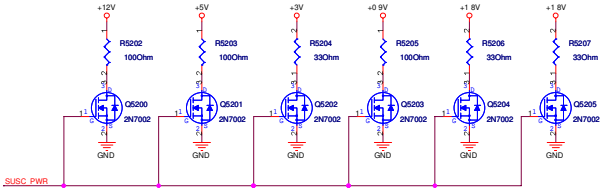
ASUSTECH CO LTD	Title : A7K	
	Engineer: Endy Zhang	
Size: Custom	Project Name: Power Sequence	Rev: 2 0
Date: 星期六 8月 14 2007	Sheet 51 of 69	

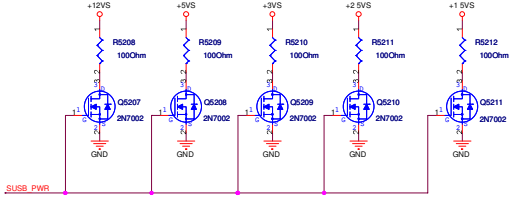


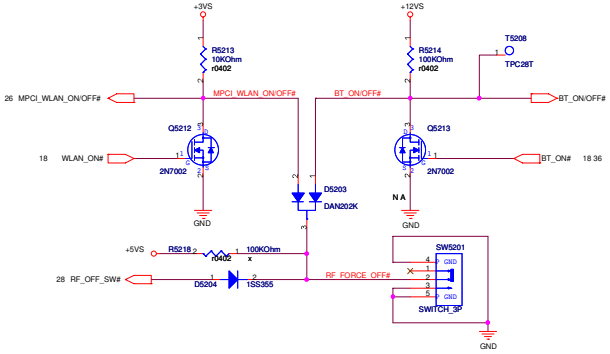


DC_IN Conn.









ASUSTECH CO LTD		Title : A7K	
		Engineer: Endy Zhang	
Size: Custom	Project Name: Discharge		Rev: 2 0
Date: 星期 六 8 14, 2007		Sheet 52 of 69	

ASUSTECH CO LTD

Title : A7K

Engineer: Endy Zhang

Size	Project Name	Rev
Custom	BLANK	2.0

Date: 星期六 十月 14, 2007 Sheet 53 of 69

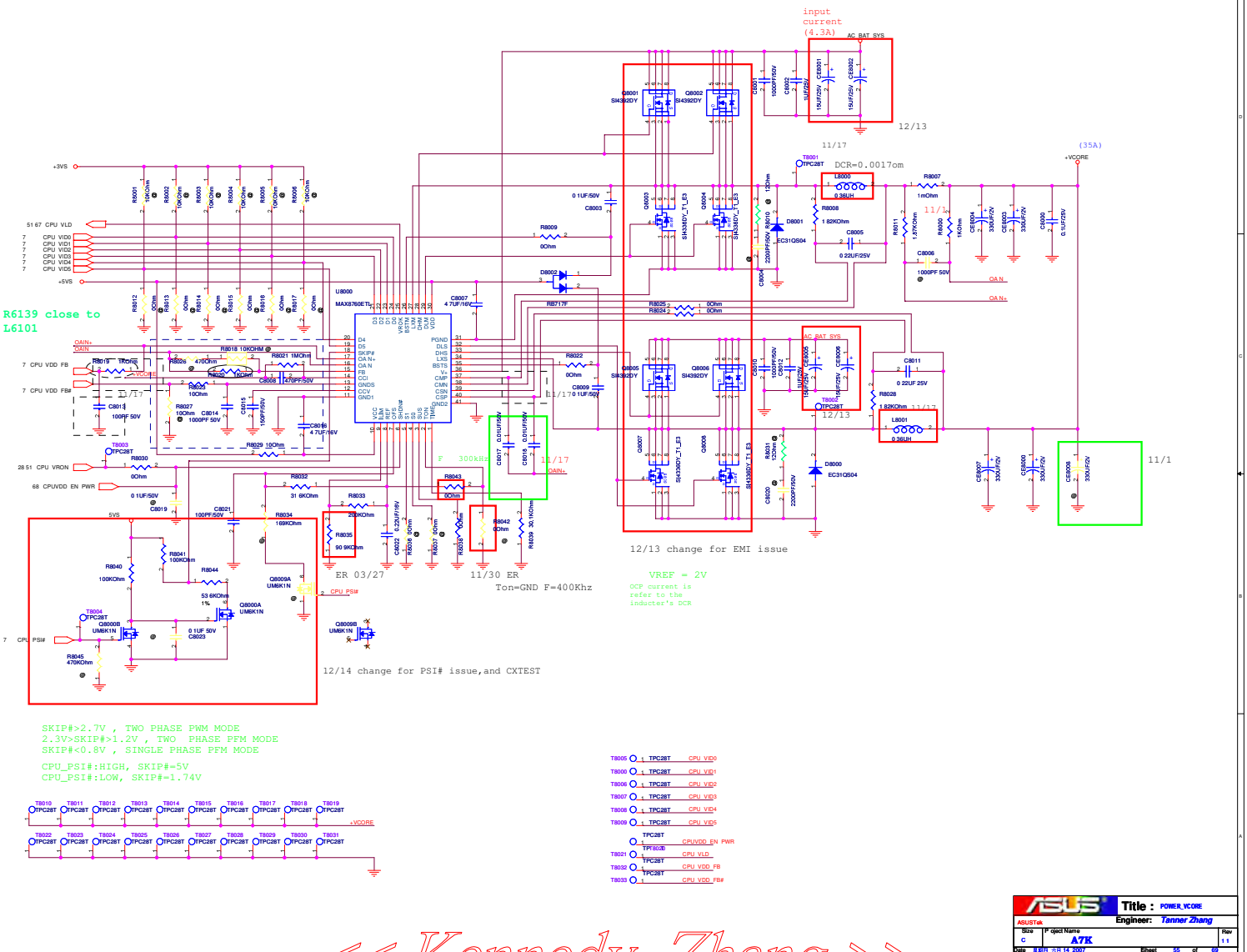
ASUSTECH CO LTD

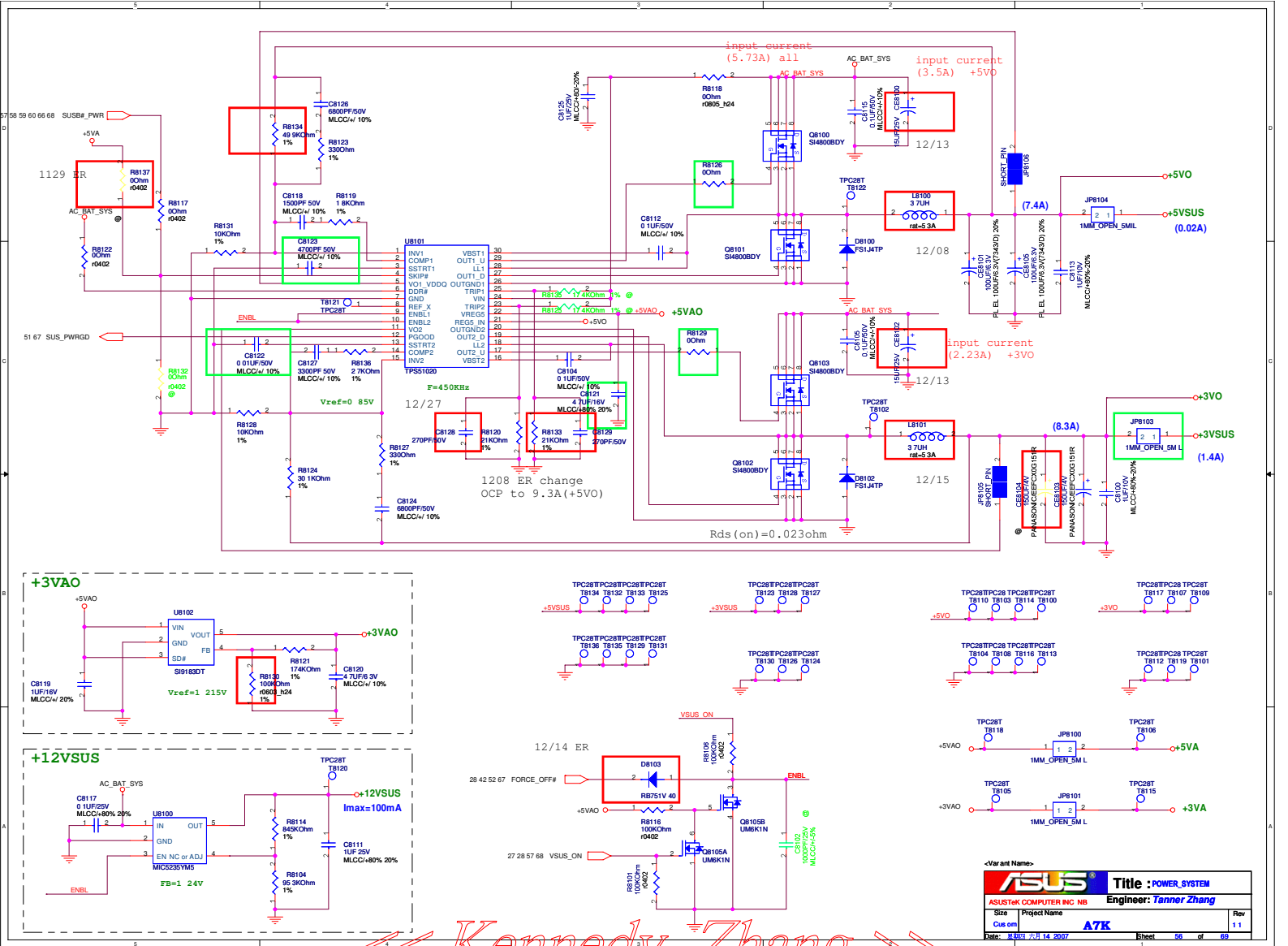
Title : A7K

Engineer: Endy Zhang

Size	Project Name	Rev
Custom	BLANK	2.0

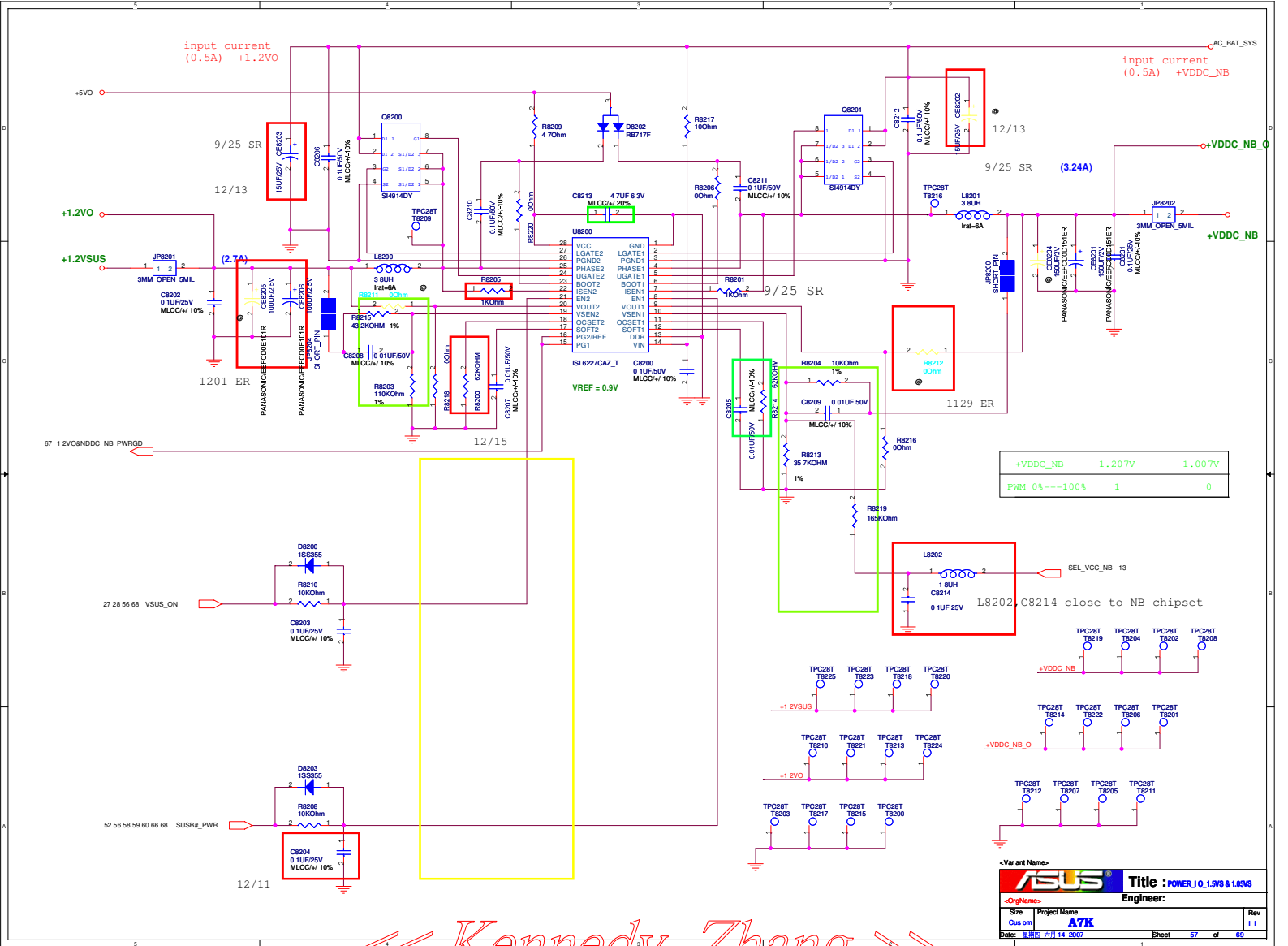
Date: 星期六 十月 14, 2007 Sheet 54 of 69


input current (4.3A)
AC_BAT_SYS
12/13
11/17
(35A)
+VCORE
DCR=0.0017om
R6139 close to L6101
MAX8760ETL
F 300kHz
11/17
12/13 change for EMI issue
VREF = 2V
OCP current is refer to the inducter's DCR
ER 03/27
11/30 ER
Ton=GND F=400Khz
12/14 change for PSI# issue,and CXTEST
SKIP#>2.7V , TWO PHASE PWM MODE
2.3V>SKIP#>1.2V , TWO PHASE PFM MODE
SKIP#<0.8V , SINGLE PHASE PFM MODE
CPU_PSI#:HIGH, SKIP#=5V
CPU_PSI#:LOW, SKIP#=1.74V
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
CPUVDD_EN_PWR
CPU_VLD
CPU_VDD_FB
CPU_VDD_FB#
Title : POWER_VCORE
Engineer: Tanner Zhang
ASUSTek
Size C
Project Name A7K
Rev 1.1
Date JAN 14, 2007
Sheet 55 of 89



<Varant Name>

Title :	POWER_SYSTEM
ASUSTeK COMPUTER INC NB	Engineer: Tanner Zhang
Size: Cus om	Project Name: A7K
Rev	1 1
Date: 星期日 六月 14 2007	Sheet 56 of 69


input current
(0.5A) +1.2VO
input current
(0.5A) +VDDC_NB
AC_BAT_SYS
+5VO
+1.2VO
+1.2VSUS
+VDDC_NB_O
+VDDC_NB
9/25 SR
12/13
(2.7A)
(3.24A)
1201 ER
1129 ER
12/15
12/11
L8200
3 8UH
Irat=6A
L8202
1 8UH
C8214
0 1UF 25V
L8202,C8214 close to NB chipset
U8200
ISL6227CAZ_T
VREF = 0.9V
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
Q8200
SI4914DY
Q8201
SI4914DY
D8202
RB717F
D8200
1SS355
D8203
1SS355
R8209 4 7Ohm
R8217 10Ohm
R8206 0Ohm
C8211 0 1UF/50V MLCC/+/ 10%
C8213 4 7UF 6 3V MLCC/+/ 20%
C8210 0 1UF/50V MLCC/+/-10%
R8220 0Ohm
R8205 1KOhm
R8201 1KOhm
R8211 0Ohm
R8215 43 2KOHM 1%
C8208 0 01UF/50V MLCC/+/ 10%
R8203 110KOhm 1%
R8218 0Ohm
R8203 62KOHM
C8207 0 01UF/50V MLCC/+-10%
C8202 0 1UF/25V MLCC/+/ 10%
C8205 10UF/25V
C8206 100UF/25V
JP8201 3MM_OPEN_5MIL
JP8200 SHORT_PIN
JP8202 3MM_OPEN_5MIL
JP8201 SHORT_PIN
C8203 15UF/25V
C8306 0 1UF/50V MLCC/+/-10%
C8212 0 1UF/50V MLCC/+/-10%
C8202 15UF/25V
TPC28T T8216
TPC28T T8209
L8201 3 8UH Irat=6A
CE8204 100UF/25V
CE8201 100UF/25V
C8201 0 1UF/25V MLCC/+/-10%
PANASONIC/EEFCD0D151ER
R8204 10KOhm 1%
C8209 0 01UF 50V MLCC/+/ 10%
R8214 82KOHM
C8205 0 01UF/50V
R8213 35 7KOHM 1%
R8216 0Ohm
R8219 165KOhm
R8212 0Ohm
R8210 10KOhm
C8203 0 1UF/25V MLCC/+/ 10%
R8208 10KOhm
C8204 0 1UF/25V MLCC/+/ 10%
67 1 2VO&NDDC_NB_PWRGD
27 28 56 68 VSUS_ON
52 56 58 59 60 66 68 SUSB#_PWR
SEL_VCC_NB 13
+VDDC_NB 1.207V 1.007V
PWM 0%---100% 1 0
TPC28T T8219
TPC28T T8204
TPC28T T8202
TPC28T T8208
+VDDC_NB
TPC28T T8225
TPC28T T8223
TPC28T T8218
TPC28T T8220
+1 2VSUS
TPC28T T8214
TPC28T T8222
TPC28T T8206
TPC28T T8201
+VDDC_NB_O
TPC28T T8210
TPC28T T8221
TPC28T T8213
TPC28T T8224
+1 2VO
TPC28T T8212
TPC28T T8207
TPC28T T8205
TPC28T T8211
TPC28T T8203
TPC28T T8217
TPC28T T8215
TPC28T T8200
<Var ant Name:>
Title : POWER_I O_1 5VS & 1 05VS
Engineer:
<OrgName>
Size Cus om
Project Name A7K
Rev 1 1
Date: 星期四 六月 14 2007
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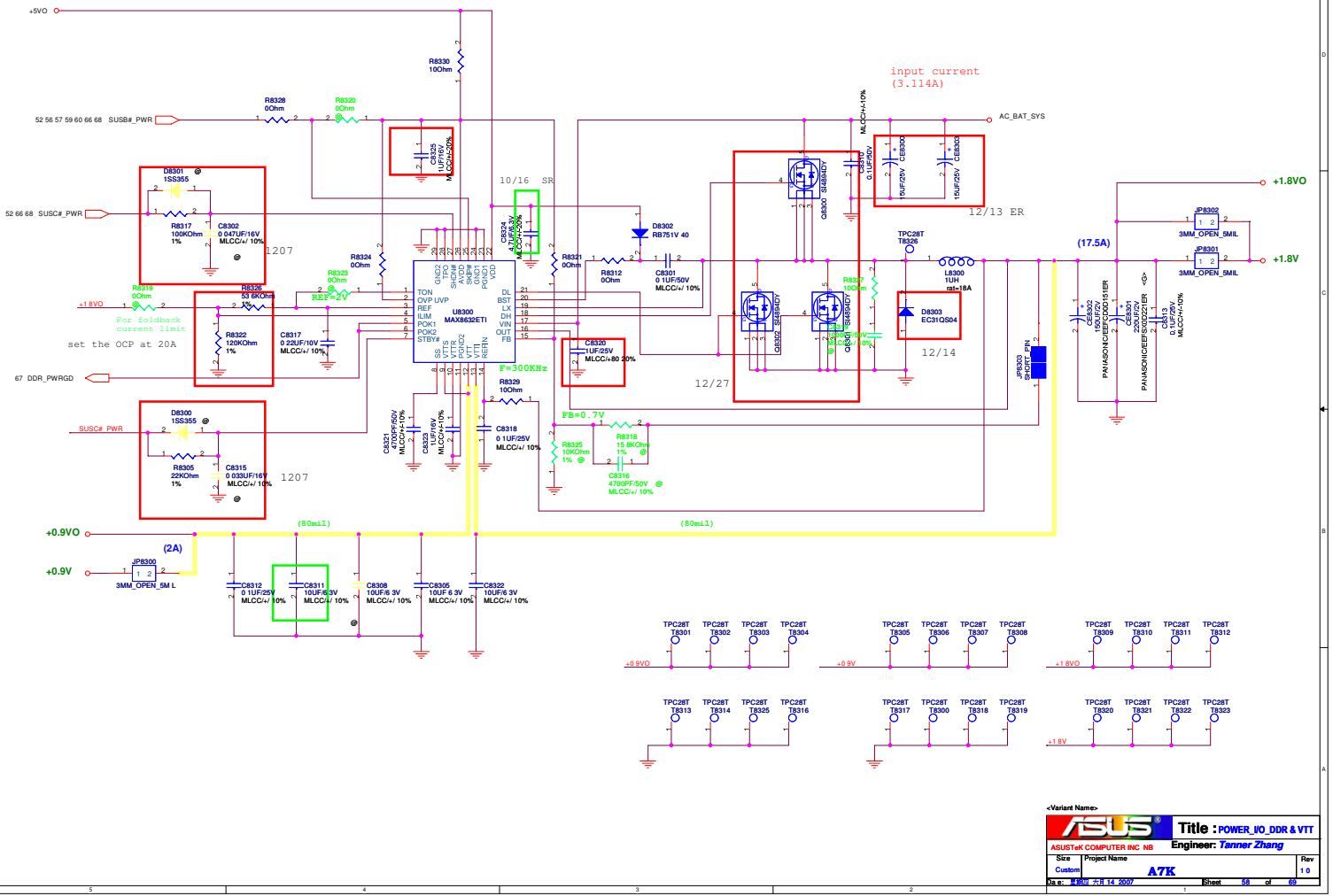


<Variant Name>

ASUSTeK COMPUTER INC NB

Title : POWER_I/O_DDR & VTT

Engineer: Tanner Zhang

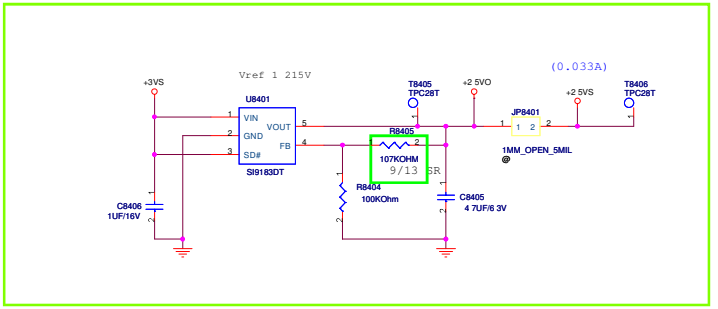
Size	Project Name	Rev
Custom	A7K	1.0

Date: 星期四 六月 14, 2007 Sheet 58 of 69

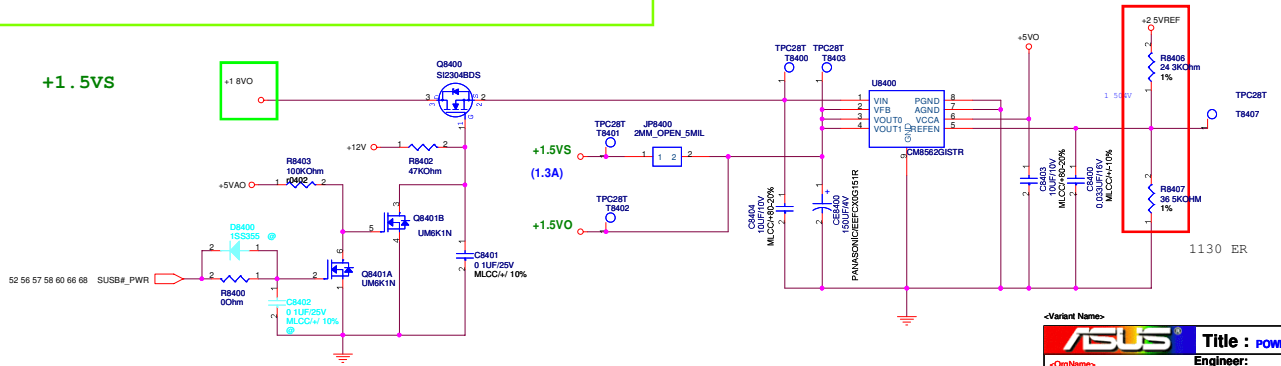
Kennedy Zhang

2.5V_REG FOR ATI M66(remove) 12/14

+2.5VS



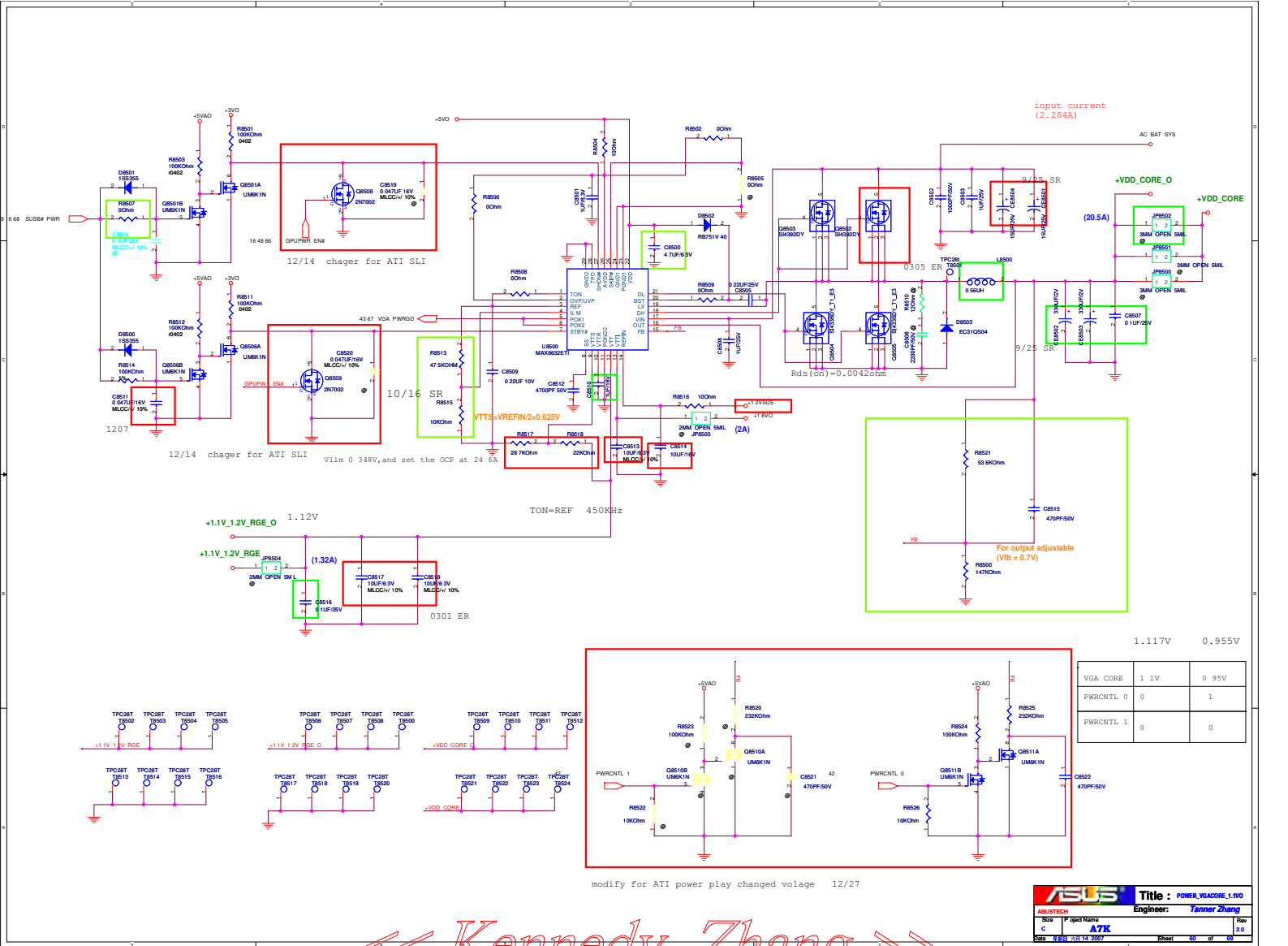
+1.5VS



<Variant Name>

<OrgName>	Title : POWER_I/O_+3VA & +2.5V	
	Engineer:	
Size: Custom	Project Name: A7K	Rev: 1.1
Date: 星期四 六月 14 2007	Sheet 59 of 69	

Kennedy Zhang



VGA CORE	1 1V	0 95V
PWRCNTL 0	0	1
PWRCNTL 1	0	0

ASUSTECH	Title :	POWER_VGACORE_1.1VD	
	Engineer:	Tanner Zhang	
Size C	Project Name A7K		Rev 2.0
Date: MON, FEB 19, 2007		Sheet 60 of 89	

Kennedy Zhang

<Variant Name>

Title : N/A

<OrgName>

Engineer:

Size	Project Name	Rev
B	A7K	1.1

Date: 星期四, 六月 14, 2007 Sheet 61 of 69

<Var ant Name>

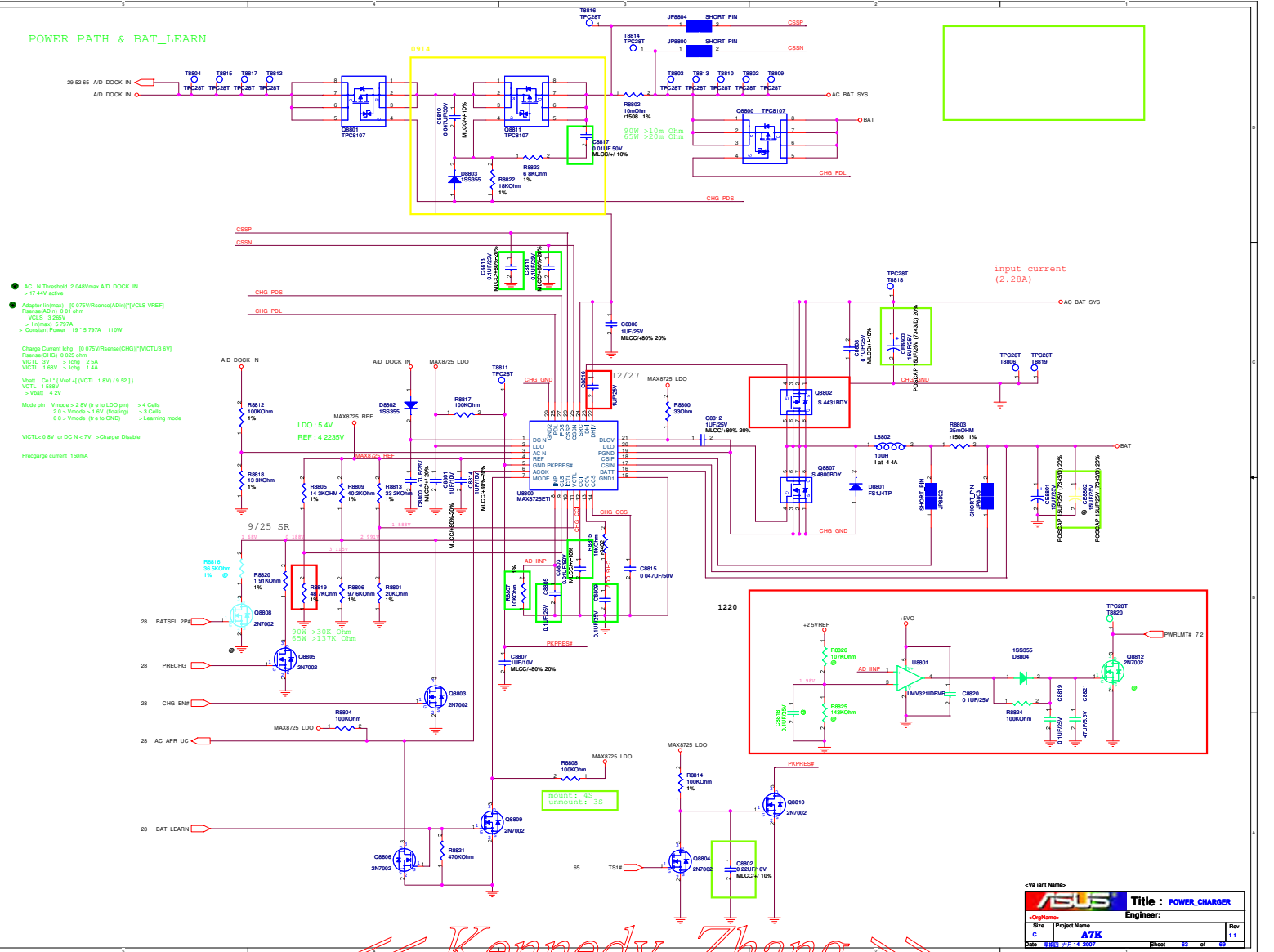
Title : POWER_SHUTDOWN#

<OrgName>

Engineer:

Size	Project Name	Rev
Cus om	A7K	1 1

Date: 星期四 六月 14 2007 Sheet 62 of 69


POWER PATH & BAT_LEARN
0914
A/D DOCK IN
AC BAT SYS
BAT
CHG PDL
CHG PDS
CSSP
CSSN
MAX8725 LDO
MAX8725 REF
LDO : 5.4V
REF : 4.2235V
input current
(2.28A)
12/27
9/25 SR
1220
AD DOCK N
A/D DOCK IN
CHG GND
CHG CCS
AD IINP
PKPRES#
BATSEL 2P#
PRECHG
CHG EN#
AC APR UC
BAT LEARN
TS1#
PWRLMT# 7 2
mount: 4S
unmount: 3S
90W >30K Ohm
65W >137K Ohm
AC Adapter In(max) [0.075V/Rsense(ADin)]*[VCLS VREF]
Rsense(AD in) 0.01 ohm
VCLS 3.285V
> In(max) 5.797A
> Constant Power 19 * 5.797A 110W
Charge Current Ichg [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG) 0.025 ohm
VICTL 3V > Ichg 2.5A
VICTL 1.68V > Ichg 1.4A
Vbatt Ce * [Vref +[(VCTL 1.8V) / 9.52]]
VCTL 1.588V
> Vbatt 4.2V
Mode pin Vmode > 2.8V (tr e to LDO p n) > 4 Cells
2.0 > Vmode > 1.6V (floating) > 3 Cells
0.8 > Vmode (tr e to GND) > Learning mode
VICTL< 0.8V or DC N < 7V >Charger Disable
Precgarge current 150mA
Title : POWER_CHARGER
Engineer:
Size C
Project Name A7K
Rev 1.1
Date 8 8/24 /Fri 14 2007
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<Var ant Name>

Title : NA

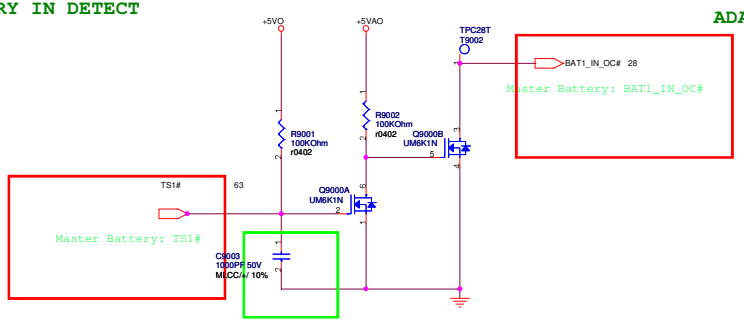
<OrgName>

Engineer:

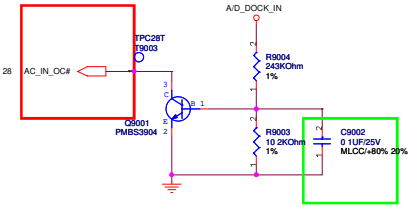
Size	Project Name	Rev
Cus om	A7K	1 1

Date: 星期四 六月 14 2007 Sheet 64 of 69

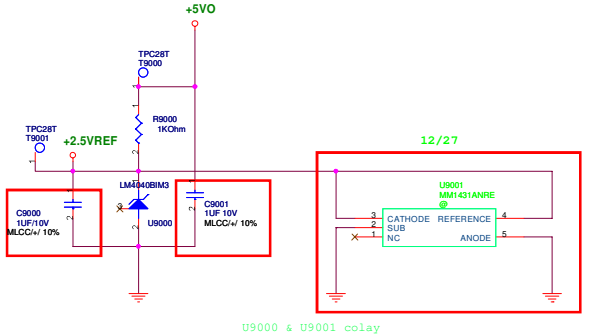
BATTERY IN DETECT



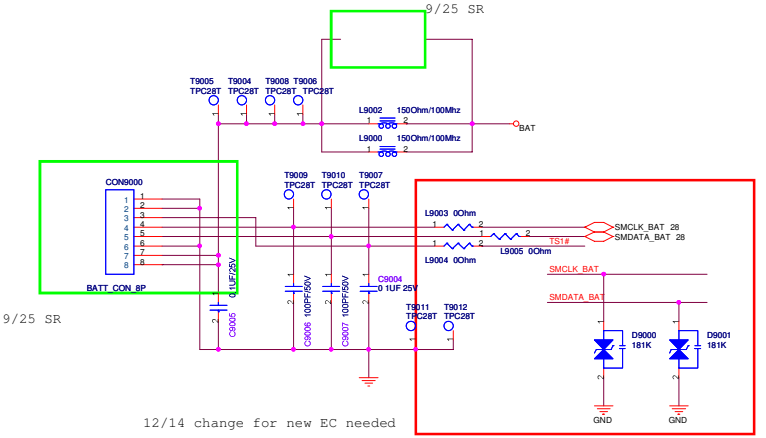
ADAPTER IN DETECT



+2.5VREF



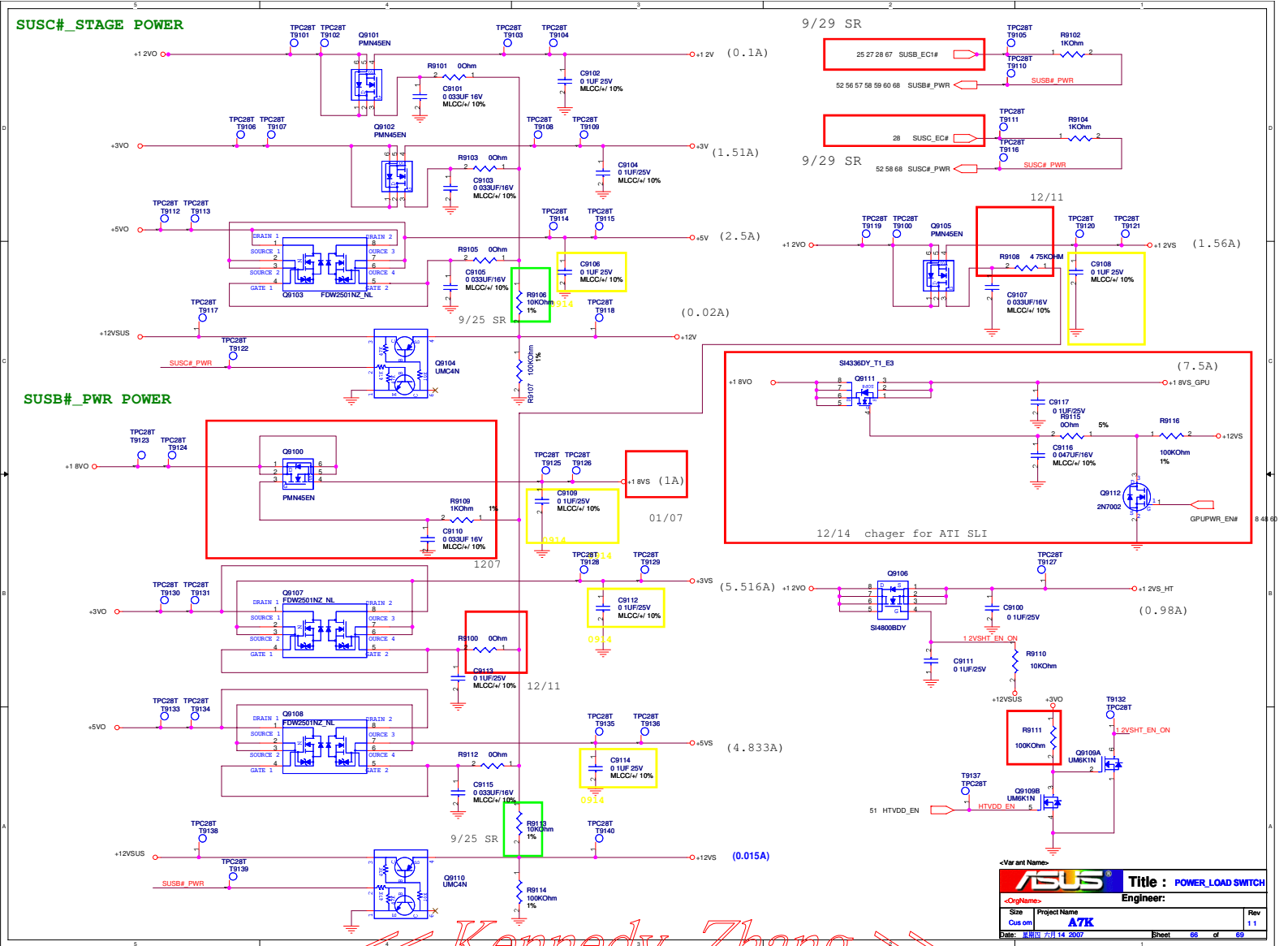
BATCON



<Var ant Name>

ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Tanner Zhang	
Size: Cus om	Project Name: A7K	Rev: 1 1
Date: 星期四 六月 14 2007	Sheet 65 of 69	

Kennedy Zhang


SUSC#_STAGE POWER
+1 2VO
TPC28T T9101
TPC28T T9102
Q9101 PMN45EN
TPC28T T9103
TPC28T T9104
+1 2V (0.1A)
R9101 0Ohm
C9101 0 033UF 16V MLCC/+/ 10%
C9102 0 1UF 25V MLCC/+/ 10%
+3VO
TPC28T T9106
TPC28T T9107
Q9102 PMN45EN
TPC28T T9108
TPC28T T9109
+3V (1.51A)
R9103 0Ohm
C9103 0 033UF/16V MLCC/+/ 10%
C9104 0 1UF/25V MLCC/+/ 10%
+5VO
TPC28T T9112
TPC28T T9113
Q9103 FDW2501NZ_NL
TPC28T T9114
TPC28T T9115
+5V (2.5A)
R9105 0Ohm
C9105 0 033UF/16V MLCC/+/ 10%
C9106 0 1UF 25V MLCC/+/ 10%
R9106 10KOhm 1%
9/25 SR
+12VSUS
TPC28T T9117
TPC28T T9122
SUSC#_PWR
Q9104 UMC4N
TPC28T T9118
+12V (0.02A)
R9107 100KOhm 1%
9/29 SR
25 27 28 67 SUSB_EC1#
52 56 57 58 59 60 68 SUSB#_PWR
TPC28T T9105
TPC28T T9110
R9102 1KOhm
SUSB#_PWR
28 SUSC_EC#
TPC28T T9111
TPC28T T9116
R9104 1KOhm
52 58 68 SUSC#_PWR
SUSC#_PWR
12/11
+1 2VO
TPC28T T9119
TPC28T T9100
Q9105 PMN45EN
TPC28T T9120
TPC28T T9121
+1 2VS (1.56A)
R9108 4 75KOHM
C9107 0 033UF/16V MLCC/+/ 10%
C9108 0 1UF 25V MLCC/+/ 10%
SUSB#_PWR POWER
+1 8VO
TPC28T T9123
TPC28T T9124
Q9100 PMN45EN
TPC28T T9125
TPC28T T9126
+1 8VS (1A)
R9109 1KOhm 1%
C9109 0 1UF/25V MLCC/+/ 10%
C9110 0 033UF 16V MLCC/+/ 10%
01/07
1207
SI4336DY_T1_E3
Q9111
+1 8VS_GPU (7.5A)
C9117 0 1UF/25V
R9115 0Ohm 5%
R9116
+12VS
C9116 0 047UF/16V MLCC/+/ 10%
100KOhm 1%
Q9112 2N7002
GPUPWR_EN#
12/14 chager for ATI SLI
+3VO
TPC28T T9130
TPC28T T9131
Q9107 FDW2501NZ_NL
TPC28T T9128
TPC28T T9129
+3VS (5.516A)
C9112 0 1UF/25V MLCC/+/ 10%
R9100 0Ohm
C9113 0 1UF/25V MLCC/+/ 10%
12/11
+1 2VO
Q9106 SI4800BDY
TPC28T T9127
+1 2VS_HT (0.98A)
C9100 0 1UF/25V
1 2VSHT_EN_ON
C9111 0 1UF/25V
R9110 10KOhm
+5VO
TPC28T T9133
TPC28T T9134
Q9108 FDW2501NZ_NL
TPC28T T9135
TPC28T T9136
+5VS (4.833A)
R9112 0Ohm
C9115 0 033UF/16V MLCC/+/ 10%
C9114 0 1UF 25V MLCC/+/ 10%
R9113 10KOhm 1%
9/25 SR
+12VSUS
TPC28T T9138
TPC28T T9139
SUSB#_PWR
Q9110 UMC4N
TPC28T T9140
+12VS (0.015A)
R9114 100KOhm 1%
+12VSUS
+3VO
T9132 TPC28T
R9111 100KOhm
1 2VSHT_EN_ON
Q9109A UM6K1N
T9137 TPC28T
Q9109B UM6K1N
51 HTVDD_EN
HTVDD_EN
<Var ant Name>
Title : POWER_LOAD SWITCH
<OrgName>
Engineer:
Size Cus om
Project Name A7K
Rev 1 1
Date: 星期四 六月 14 2007
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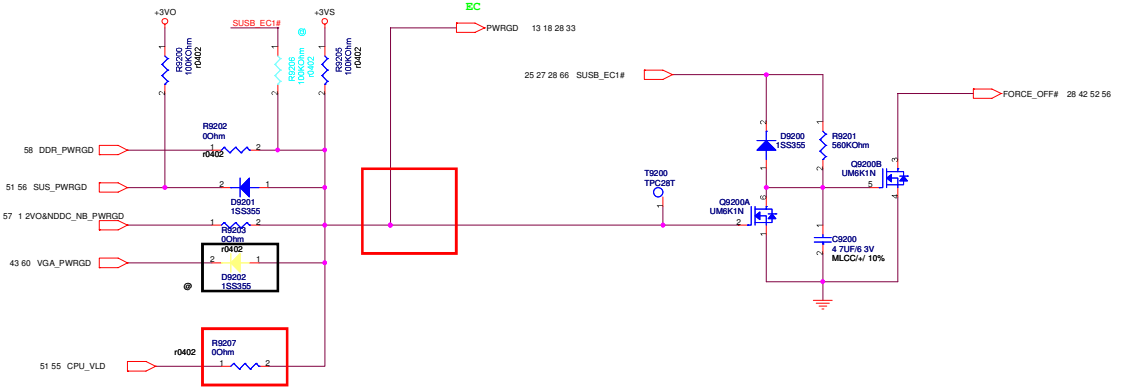
POWER GOOD DETECTER



1207

<Variant Name>

<OrgName>	Title : POWER_PROTECT	
	Engineer:	
Size: Cus om	Project Name: A7K	Rev: 1 1
Date: 星期四 六月 14 2007	Sheet 67 of 69	

AC_BAT_SYS — AC_BAT_SYS 22 55 56 57 58 60 63
+3VA — +3VA 17 28 50 52 56
+5VA — +5VA 56
+5VO — +5VO 56 57 58 59 60 63 65 66
+3VO — +3VO 56 60 66 67
+3VSUS — +3VSUS 7 18 20 25 26 27 31 51 56
+5VSUS — +5VSUS 27 37 50 56
+3V — +3V 18 25 26 28 34 36 37 40 52 66
+3VS — +3VS 7 9 13 14 16 17 18 19 20 21 22 23 24 26 27 28 30 31 33 35 36 38 39 40 48 49 50 52 55 59 66 67

+12VSUS — +12VSUS 56 66
+12V — +12V 21 31 36 39 52 59 66
+12VS — +12VS 22 48 52 66

+5V — +5V 22 36 50 52 66
+5VS — +5VS 20 21 23 24 29 30 31 35 37 50 52 55 66

+2 5VO — +2 5VO 59
+2 5VS — +2 5VS 7 33 52 59
+1 8VO — +1 8VO 58 59 60 66
+1 8V — +1 8V 7 8 9 10 52 58
+1 8VS — +1 8VS 13 14 17 20 49 66
+VDDC_NB_O — +VDDC_NB_O 57
+VDDC_NB — +VDDC_NB 14 57

+0 9V — +0 9V 7 8 10 52 58
BAT — BAT 29 63 65
+1 5VO — +1 5VO 59
+1 5VS — +1 5VS 26 27 40 52 59
+2 5VREF — +2 5VREF 59 63 65
+VCORE — +VCORE 8 55

+VDD_CORE_O — +VDD_CORE_O 60
+1 1V_1 2V_RGE_O — +1 1V_1 2V_RGE_O 60
+VDD_CORE — +VDD_CORE 43 48 60
+1 1V_1 2V_RGE — +1 1V_1 2V_RGE 48 60
+1 2VO — +1 2VO 57 66
+1 2VSUS — +1 2VSUS 20 57 60

+1 2V — +1 2V 20 66
+1 2VS — +1 2VS 13 14 17 19 20 66

+1 2VS_HT — +1 2VS_HT 5 7 8 14 66

FOR POWER TEST

+3VA

JP9300 (SGL_JUMP): 1 — 1 2 — 2 — CPUVDD_EN_PWR 57

JP9301 (SGL_JUMP): 1 — 1 2 — 2 — SUSB#_PWR — SUSB#_PWR 52 56 57 58 59 60 66

JP9302 (SGL_JUMP): 1 — 1 2 — 2 — SUSC#_PWR — SUSC#_PWR 52 58 66

JP9303 (SGL_JUMP): 1 — 1 2 — 2 — VSUS_ON — VSUS_ON 27 28 56 57

<Variant Name>

Title : POWER_SIGNAL

<OrgName> Engineer:

Size	Project Name	Rev
Cus om	A7K	1 1

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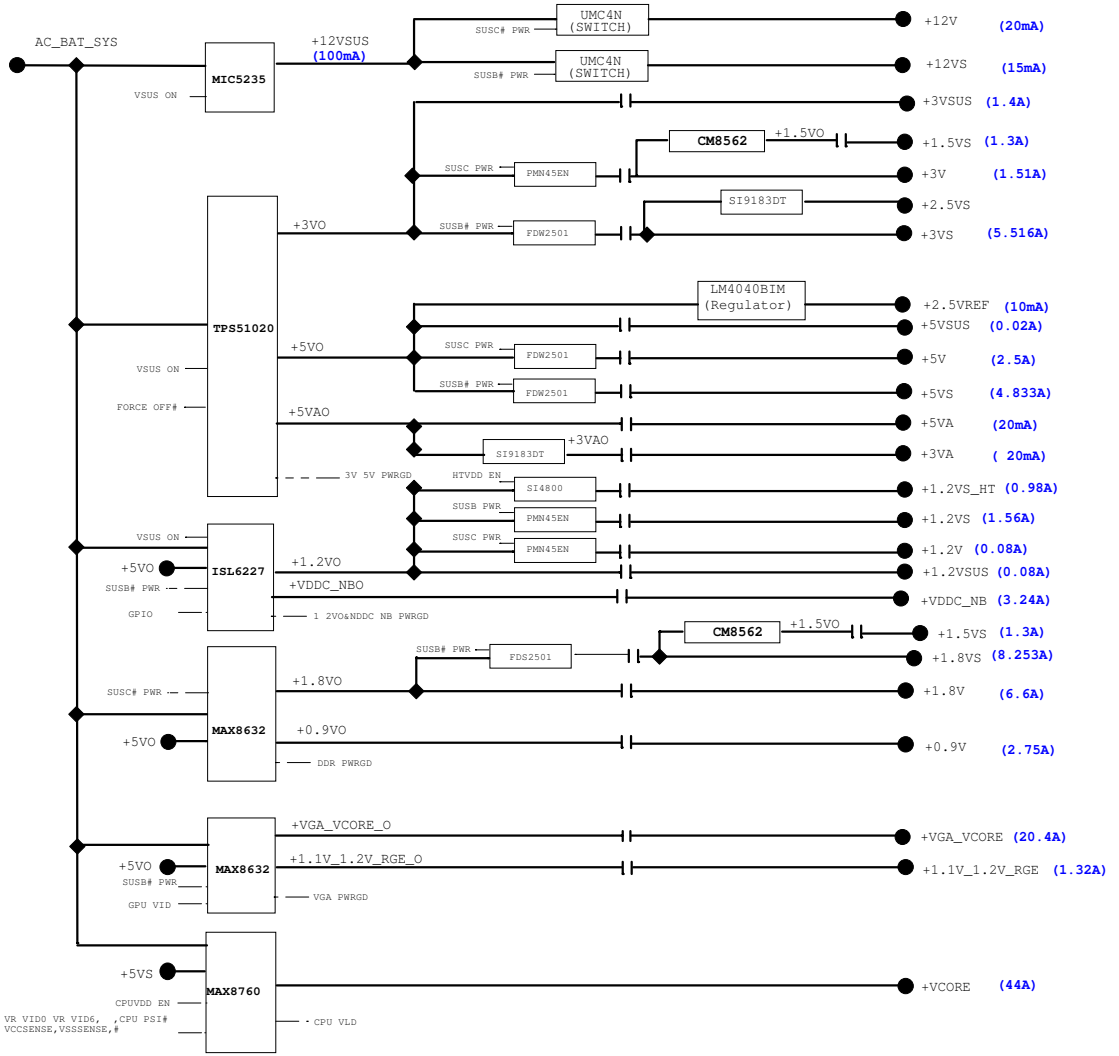
Kennedy Zhang



Kennedy Zhang