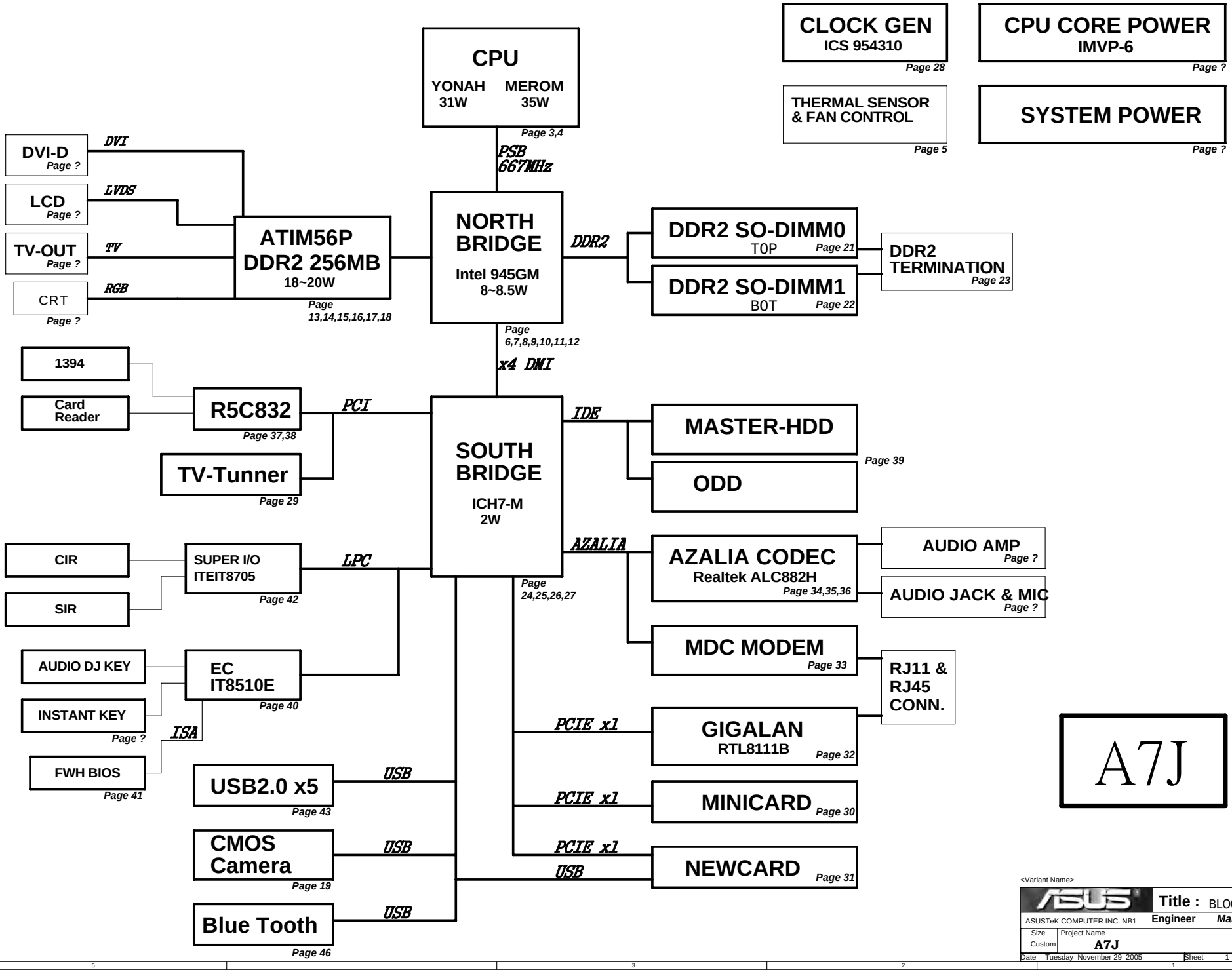


<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : BLOCK DIAGRAM

Engineer Mark , Frank

Size	Project Name	Rev
Custom	A7J	2.0

Date Tuesday November 29 2005 Sheet 1 of 52

REVISION LIST

R1.0 2005/08/01

R1.1 2005/10/20

R2.0 2005/11/17

R2.1 2005/11/25

POWER INTERFACE

SIGNALS	TYPE	POWER
PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT1_IN#_OC	I	+3.3V
BAT2_IN#_OC	I	+3.3V
CHG_EN_OC	I	+3.3V
CHG_LED	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SMCLK_BAT2	IO	+3.3V
SMDATA_BAT2	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 V	6.0A
+0.9VS	0.9V	1.0A
+1.5VS	1.5V	3A
+1.8V	1.8V	5.5A
+1.8VS	1.8V	3.3A
+2.5VS	2.5V	0.3 A
+3V	3.3V	1.5A
+3VS	3.3V	2.0A
+3VSUS	3.3V	0.72A
+5V	5V	4.8A
+5VS	5V	3.3A
+5VSUS	5V	0.01A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM	WIDTH
TOP/BOT	18 mils

37.5 OHM	WIDTH
TOP/BOT	11 mils
IN1/IN2/IN3	11 mils

42 OHM	WIDTH
TOP/BOT	9 mils
IN1/IN2/IN3	9 mils

50 OHM	WIDTH
TOP/BOT	6.5 mils
IN1/IN2/IN3	6.5 mils

55 OHM	WIDTH
TOP/BOT	5 mils
IN1/IN2/IN3	5 mils

75 OHM	WIDTH
TOP/BOT	4 mils
IN1/IN2/IN3	4 mils

Differential

70 OHM	WIDTH/SPACE
TOP/BOT	9 mils/ 4 mils
IN1/IN2/IN3	9 mils/ 4 mils

85 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 4 mils
IN1/IN2/IN3	5 mils/ 4 mils

90 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 4.5 mils
IN1/IN2/IN3	5 mils/ 4.5 mils

100 OHM	WIDTH/SPACE
TOP/BOT	5 mils/ 7 mils
IN1/IN2/IN3	5 mils/ 7 mils

110 OHM	WIDTH/SPACE
TOP/BOT	4 mils/ 8 mils
IN1/IN2/IN3	4 mils/ 8 mils

PCI INTERFACE

PCI_REQ#

MINIPCI(TV)	PCI_REQ#0
CB&1394	PCI_REQ#1

IDSEL

MINIPCI(TV)	PCI_AD16
CB&1394	PCI_AD17

PCB STACK-UP

PCB THICKNESS: 1.6 mm

L1	TOP
L2	GND
L3	IN1
L4	VCC
L5	IN2
L6	IN3
L7	GND
L6	BOT

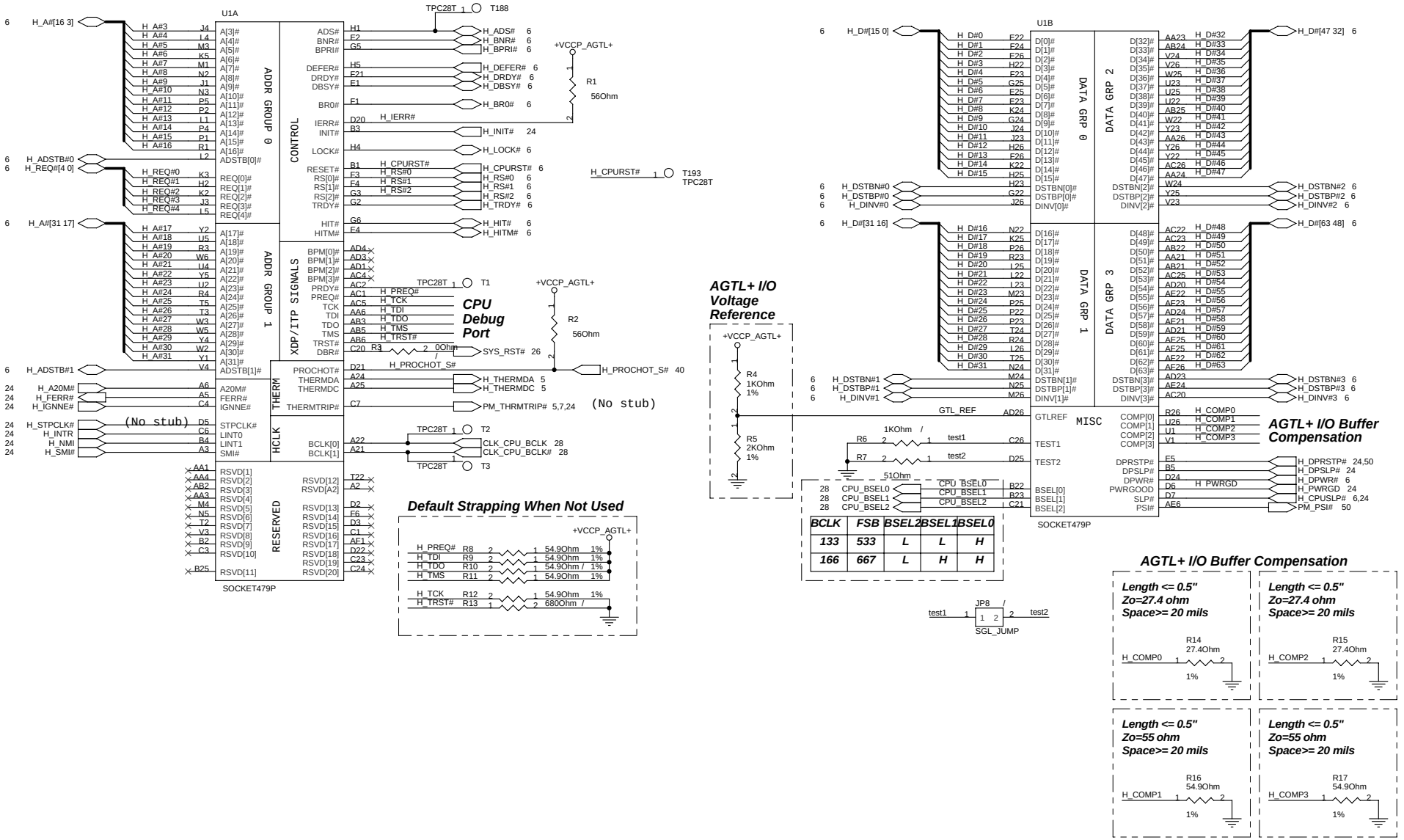
<Variant Name>

Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC. NB1 Engineer *Mark , Frank*

Size	Project Name	Rev
Custom	A7J	2.0

Date: Tuesday, November 29, 2005 Sheet 2 of 52



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

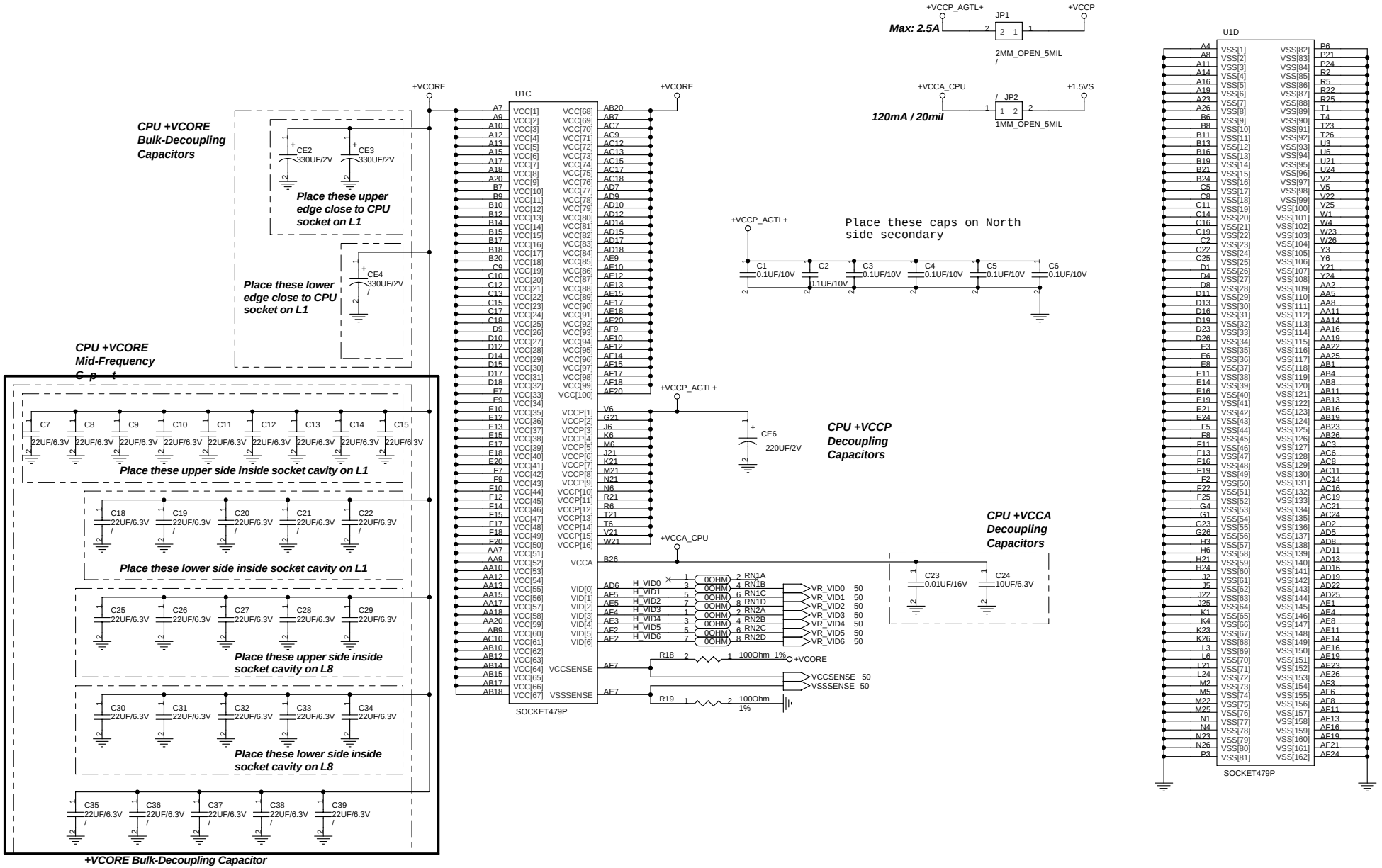
<Variant Name>

Title : CPU-YONAH(HOST)

ASUSTeK COMPUTER INC. NB1 Engineer Mark , Frank

Size	Project Name	Rev
Custom	A7J	2.0

Date Tuesday November 29 2005 Sheet 3 of 52



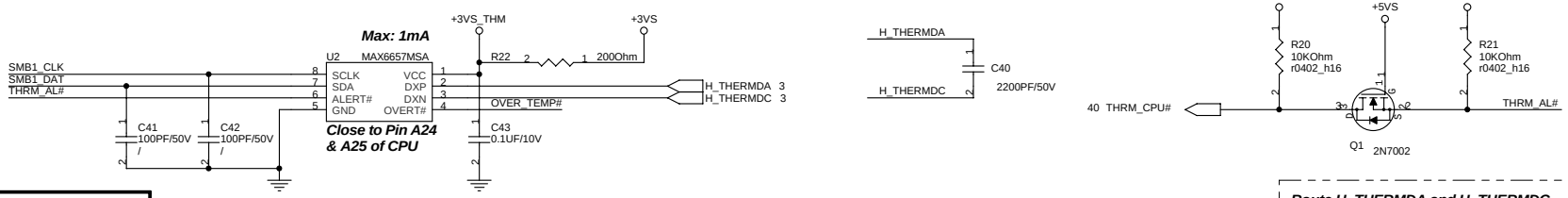
+VCORE Bulk-Decoupling Capacitor
Intel: 330UF *6
R1F: 330UF *4
A7J: 330UF *5
+VCORE Mid-Frequency Capacitor
Intel: 22UF *32
R1F: 22UF *16
A7J:22UF*29 use 19
+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4
A7J: 220UF *1, 0,1UF *6

<Variant Name>

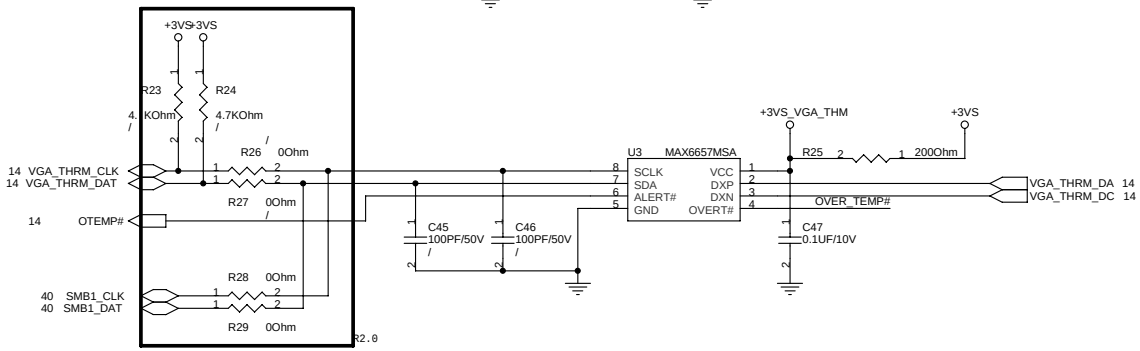
ASUSTeK COMPUTER INC. NB1	Title : CPU_YONAH(PWR)	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 4 of 52	

Thermal Sensor

CPU



VGA

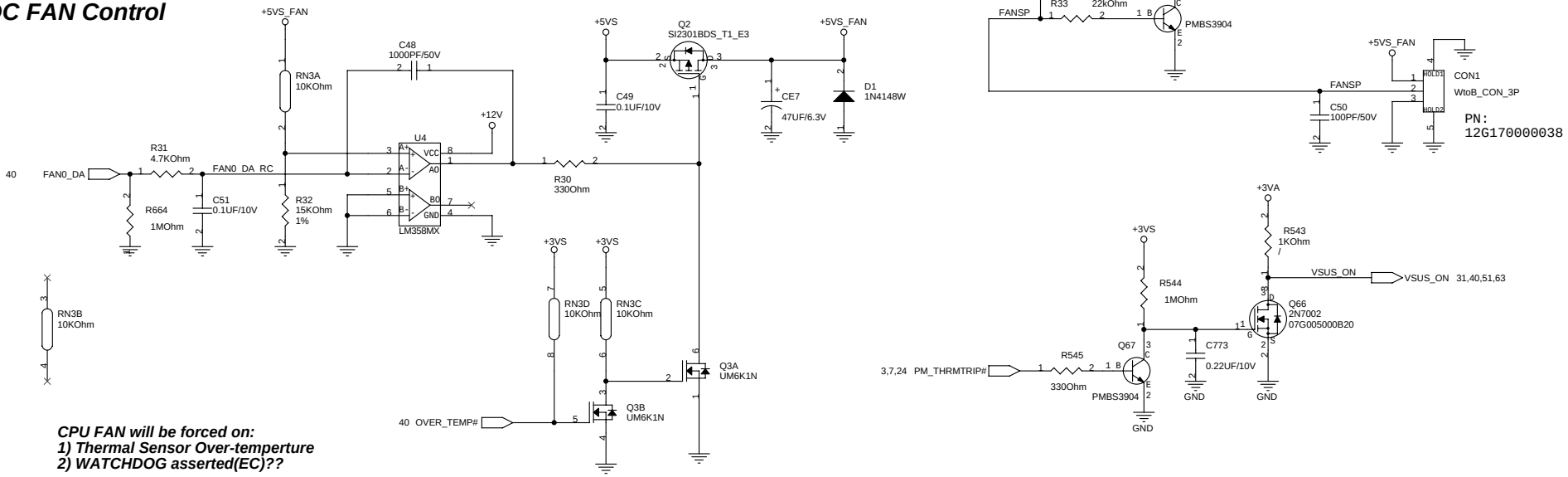


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



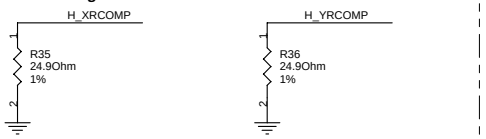
CPU FAN will be forced on:
1) Thermal Sensor Over-temperture
2) WATCHDOG asserted(EC)??

<Variant Name>

ASUSTeK COMPUTER INC. NB1	**Title :** THER SENSOR & FAN	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 5 of 52	

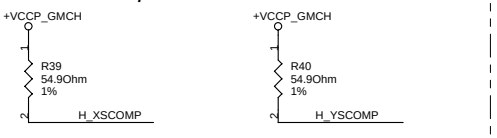
RCOMP

For Calibrating the FSB I/O Buffer



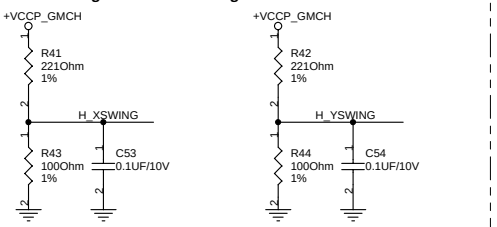
SCOMP

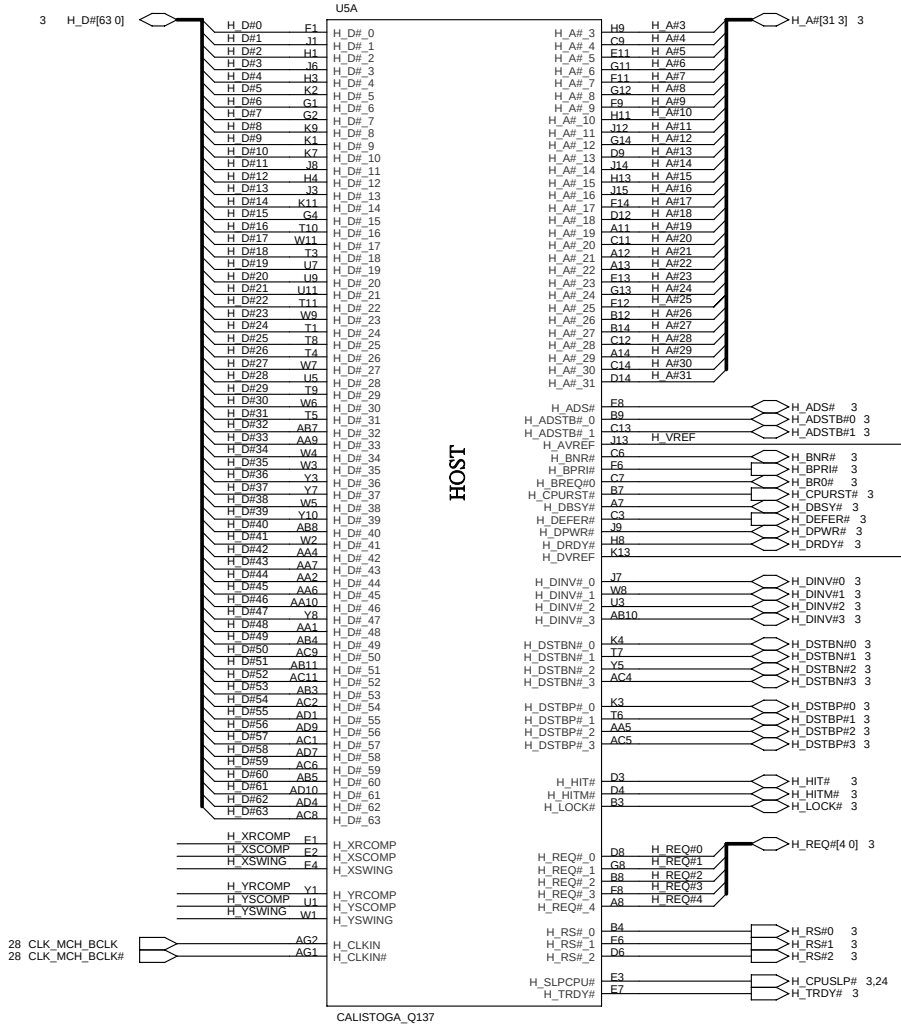
For Slew Rate Compenssation on the FSB



Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits





<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(HOST)	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 6 of 52	

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

MCH_CFG_5 — R45 1 2 1KOhm /

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R46 1 2 1KOhm /

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

MCH_CFG_13 — R50 1 2 1KOhm /

MCH_CFG_12 — R51 1 2 1KOhm /

CFG7 : CPU Strap

0 = DT/Transpotable CPU

1 = Mobile CPU (D)

MCH_CFG_7 — R47 1 2 1KOhm /

CFG18 : VCC Select

0 = 1.05V (D)

1 = 1.5V

+3VS

MCH_CFG_18 — R58 1 2 1KOhm /

CFG9 : PCIE Graphic Lane

0 = Reverse Lane

1 = Normal Operation (D)

MCH_CFG_9 — R54 1 2 1KOhm /

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)

1 = Lanes Reversed

+3VS

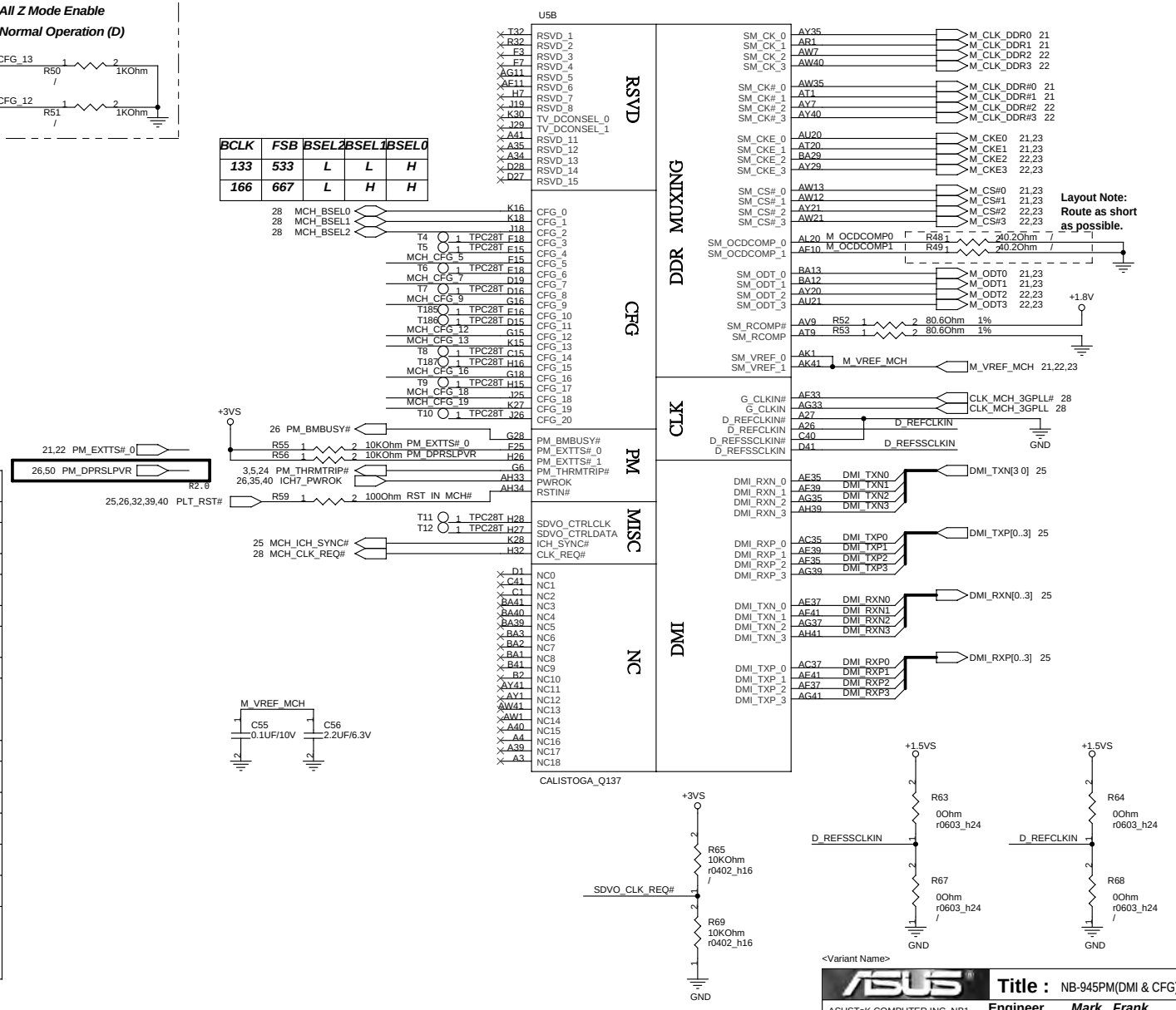
MCH_CFG_19 — R61 1 2 1KOhm /

Note: CFG[17:3] have internal pull-ups while CFG[20:18] have internal pull-downs.

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	*533*	*L*	*L*	*H*
166	*667*	*L*	*H*	*H*

CFG — All are sampled with respect to the leading edge of the GMCH PWROK

2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4
6		(Default)
7	CPU Strap	0 = Reserved 1 = Mobile
8		CPU (Default)
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal
11:10		(Default)
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled
17		(Default)
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



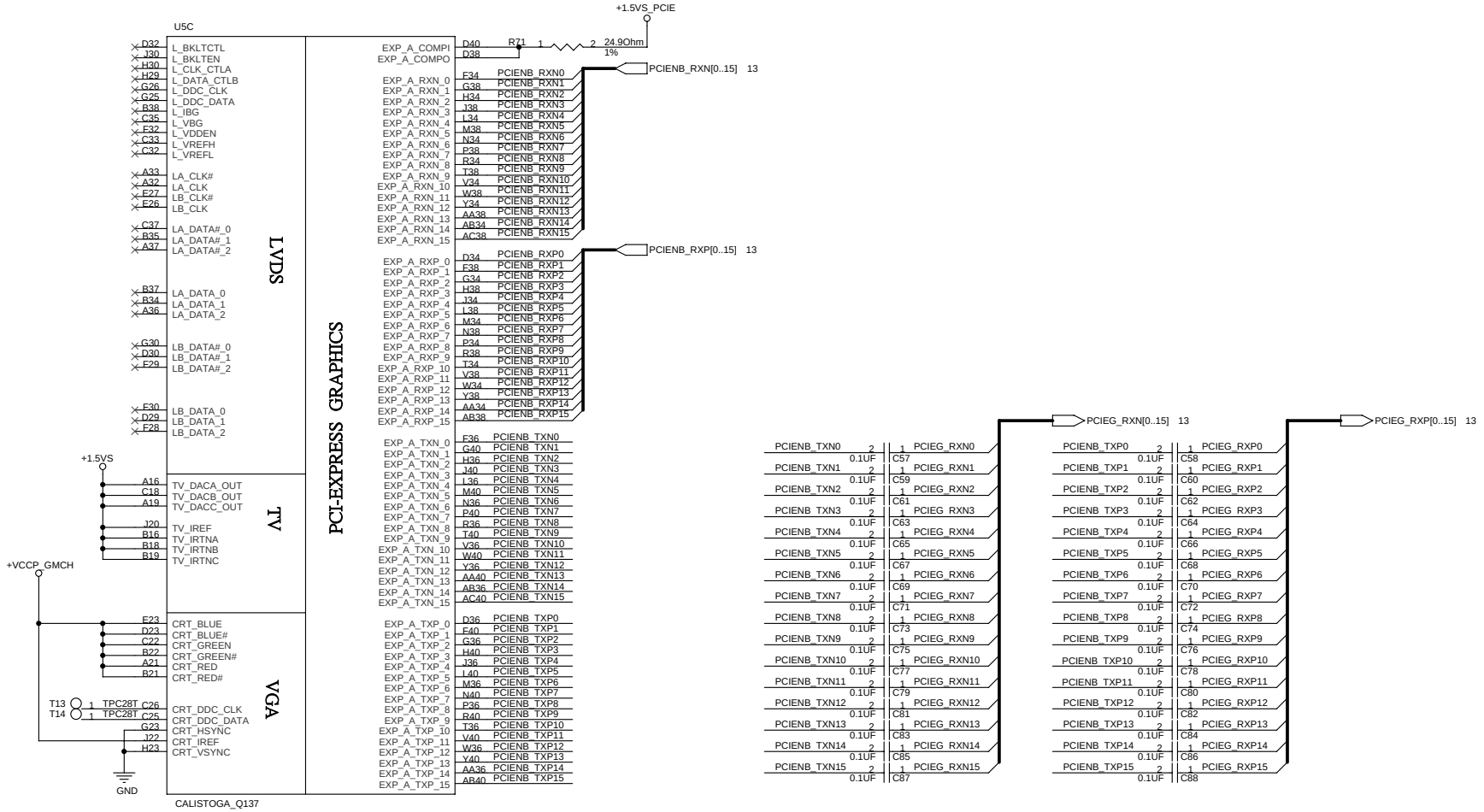
<Variant Name>

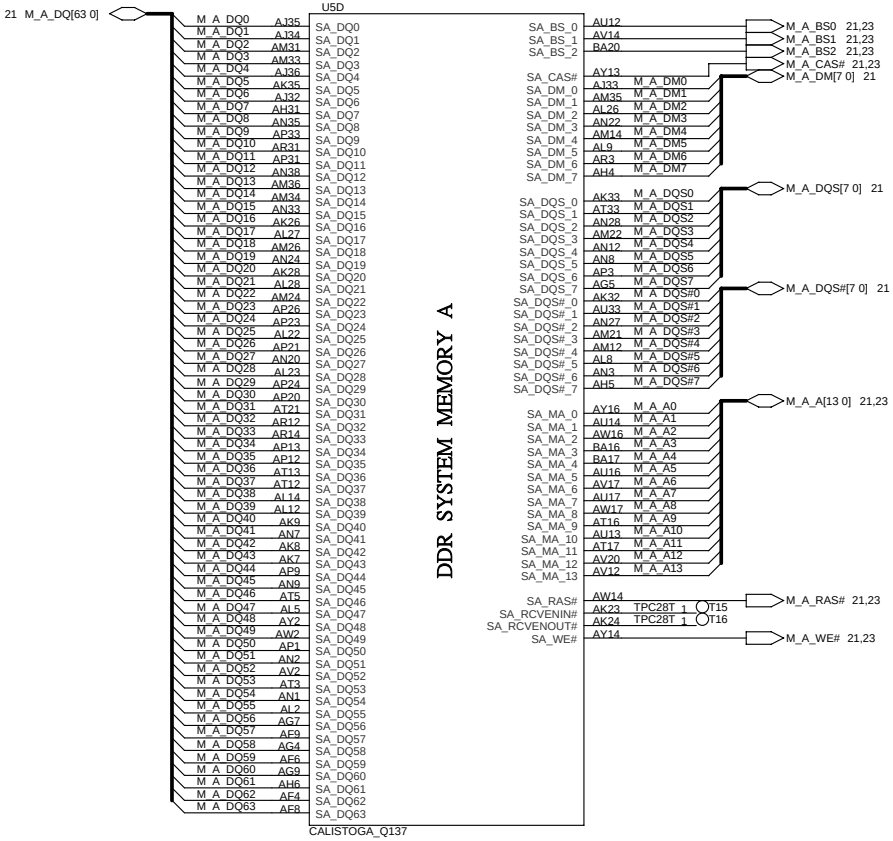
Title : NB-945PM(DMI & CFG)

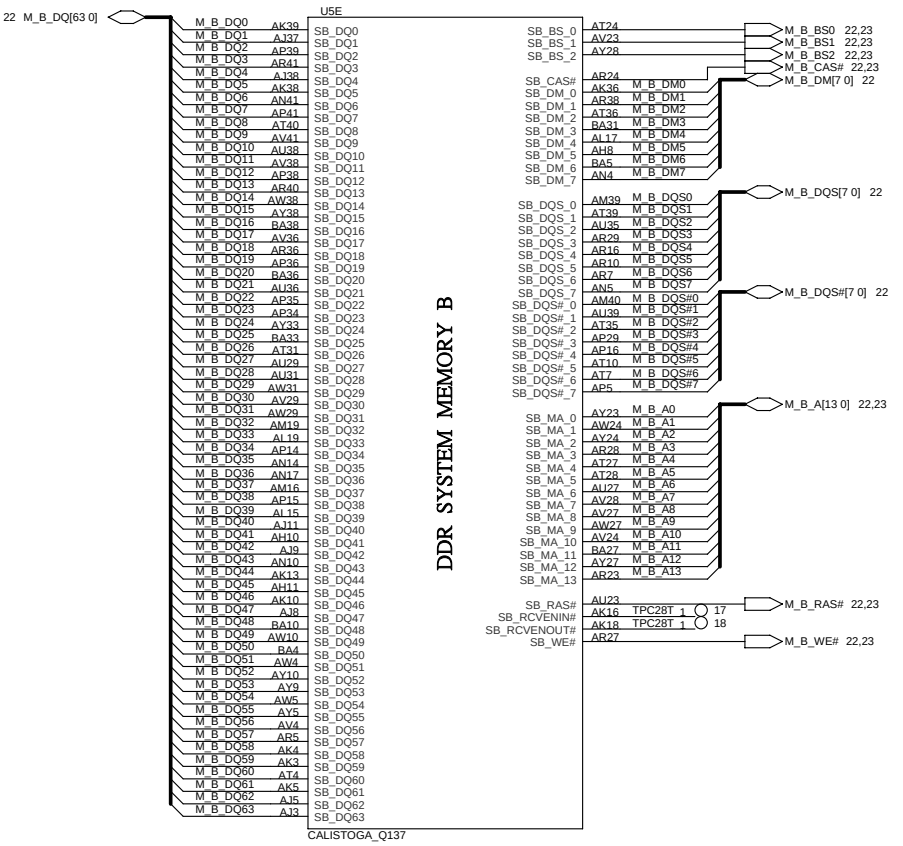
ASUSTeK COMPUTER INC. NB1 — **Engineer** *Mark , Frank*

Size	Project Name	Rev
Custom	**A7J**	2.0

Date Tuesday November 29 2005 — Sheet 7 of 52

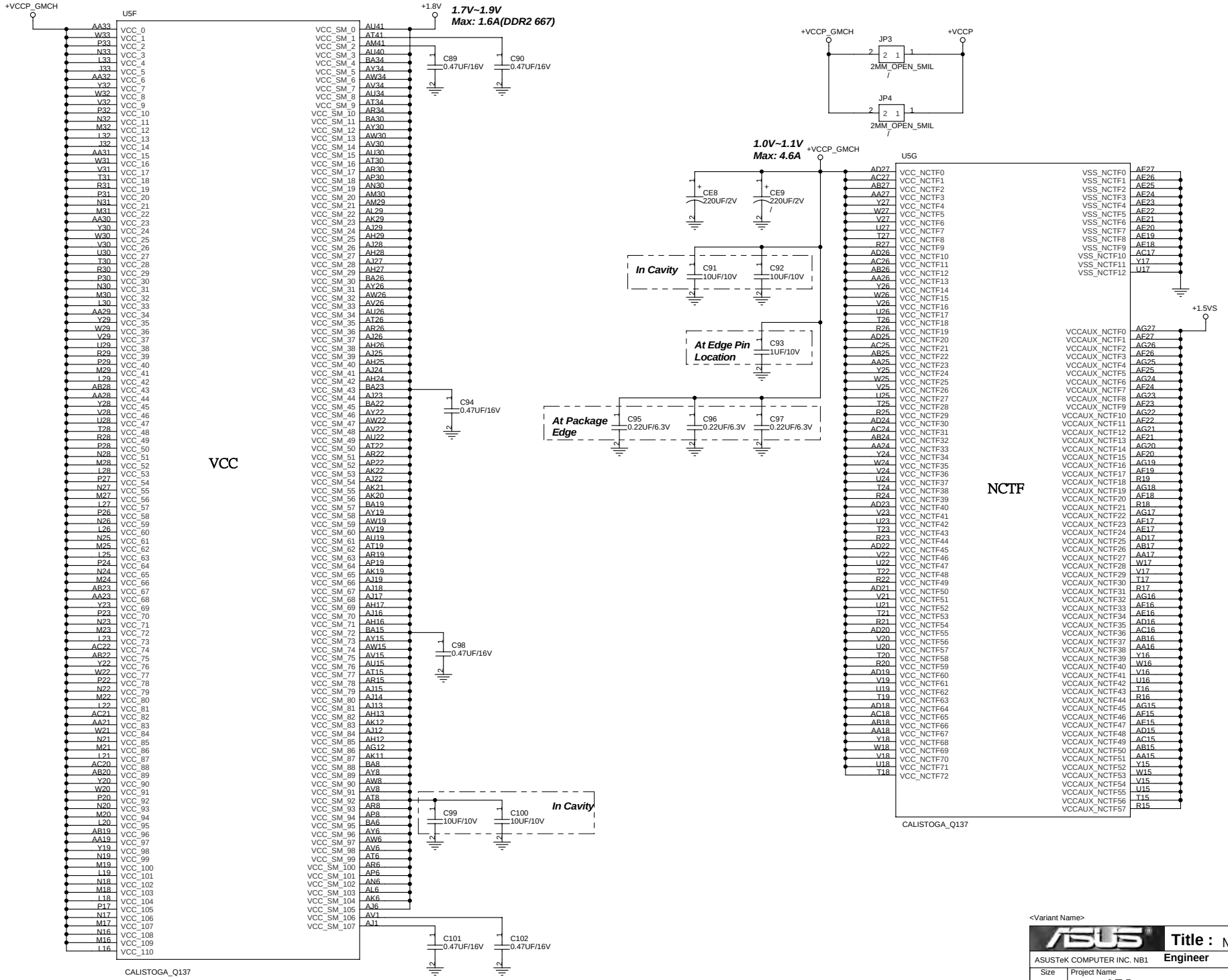

U5C
+1.5VS_PCIE
R71 1 2 24.9Ohm 1%
PCIENB_RXN[0..15] 13
PCIENB_RXP[0..15] 13
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
+1.5VS
+VCCP_GMCH
GND
T13 TPC28T C26
T14 TPC28T C25
CALISTOGA_Q137
PCIEG_RXN[0..15] 13
PCIEG_RXP[0..15] 13





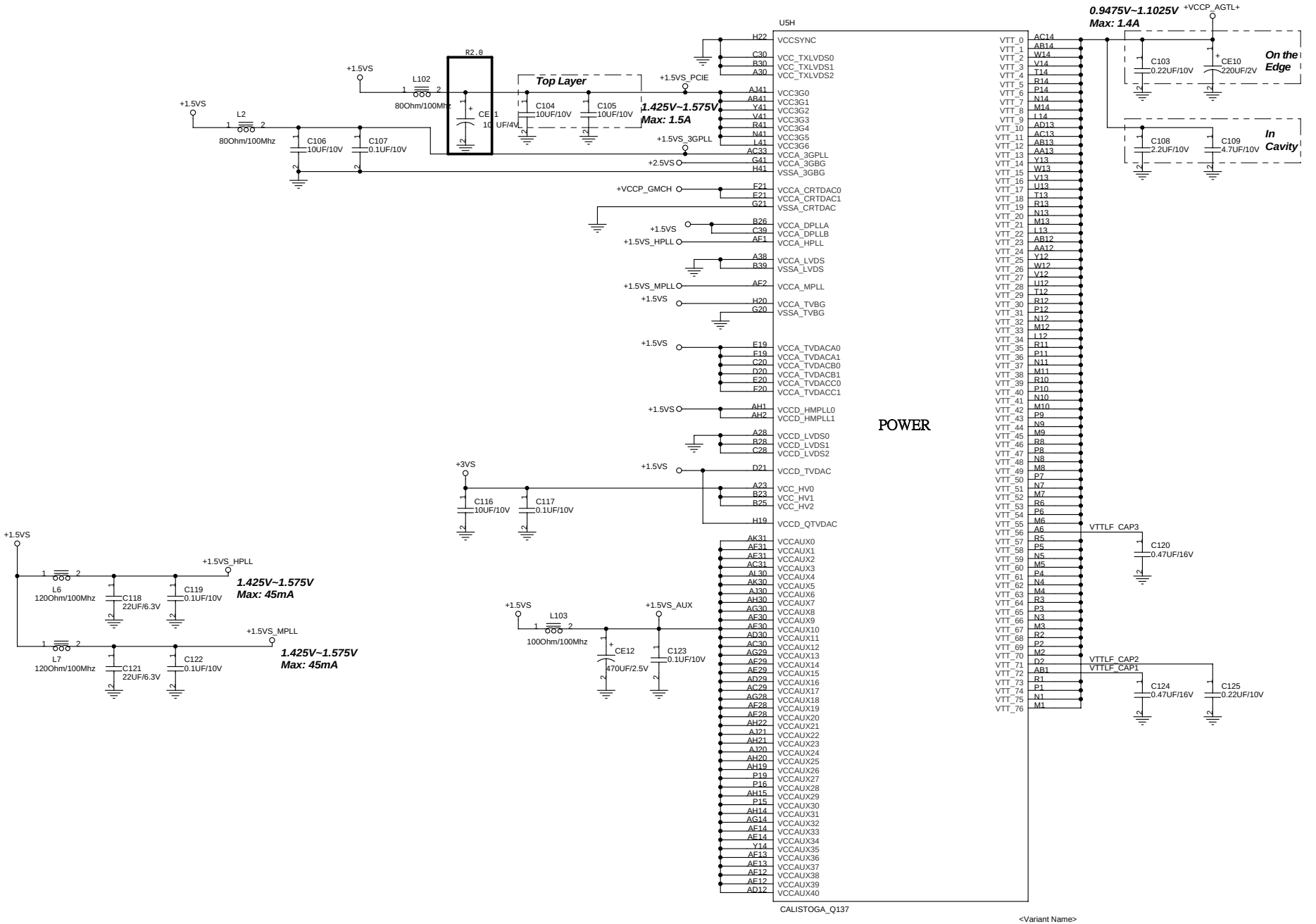
<Variant Name>

ASUSTeK COMPUTER INC. NB1	**Title :** NB-945PM(DDR2)	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 9 of 52	



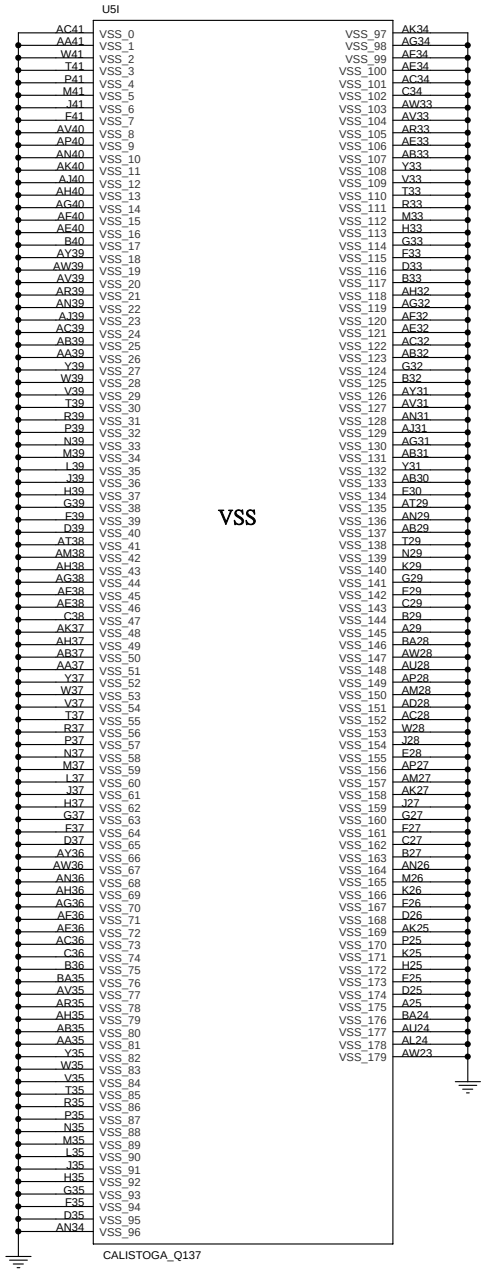
<variant_name>

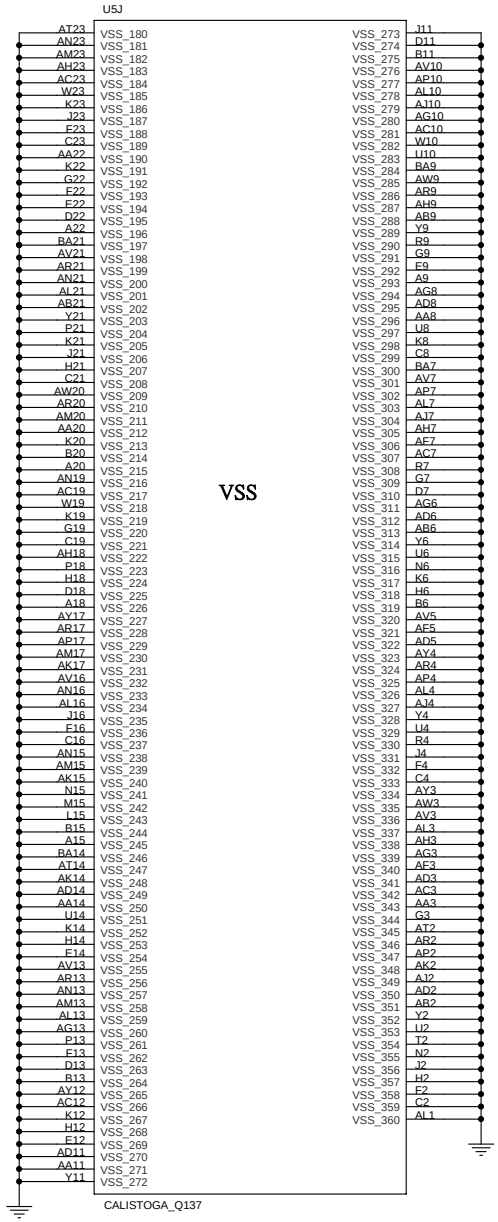
ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(PWR)	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 10 of 52	



<Variant Name>

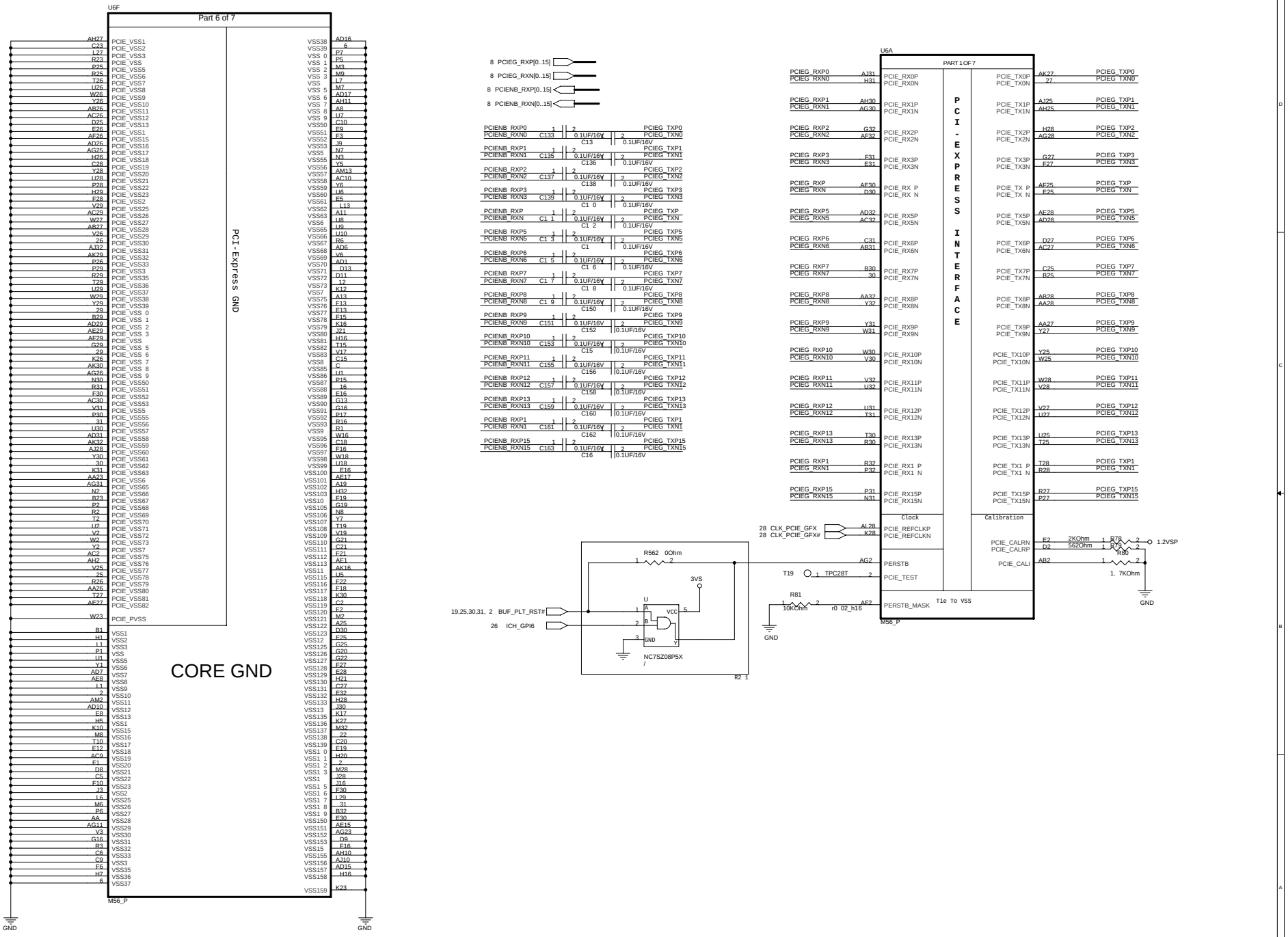
ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(PWR2)	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 11 of 52	





<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(GND)	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 12 of 52	



<Var ant Name>

ASUSTek COMPUTER INC

Engineer: <Enginner Name>

Title : ATI_M56P_PCI-E(1)

Size	Project Name	Rev
C	A7J	2.0

Date: Tuesday, November 29, 2005 Sheet 13 of 52

+AVDD<78 mA VDD1DI+VDD2DI<48 mA

MEM_ID[1:0]: MEM_Type
00: Infineon HYB18T256161AFL-25_16Mx16
01: xxx
10: Hynix HY5PS561621AFP-25_16Mx16
11: xxx

GPIO[0]: Tx Power Savings Enable
0: 50% Tx output swing
1: full Tx output swing (recommended)
(default 0, internal pull-down)

GPIO[1]: Tx De-emphasis Enable
0: Tx de-emphasis disbale
1: Tx de-emphasis enable
(default 0, internal pull-down)

R1.0 0802

R1.1

1.65V VREF Divider close to M56

+PVDD = 36 mA (max)

+MPVDD = 12 mA (max)

+TPVDD< 24 mA

+TXVDDR < 180 mA

+A2VDD < 156 mA

U6B PART 2 OF 7

VIDEO & MULTIMEDIA

Expand GPIO

VIP Host/External TMDS

General Purpose I/O

Thermal Diode

PLL & XTAL

Test

ROM

LVDS PLL and I/O GND

External SSC

Integrated TMDS

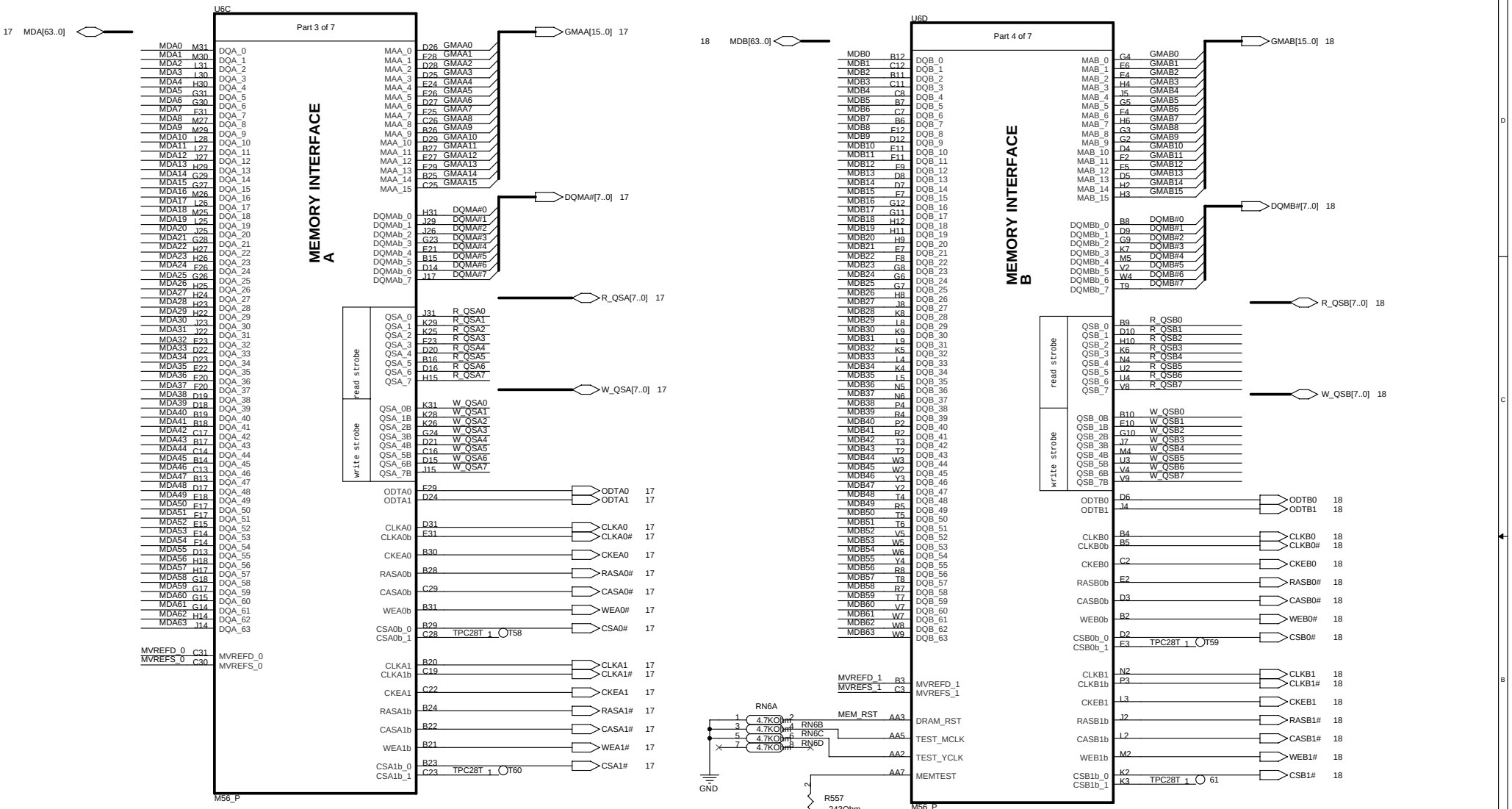
DAC / CRT

DAC2 (TV/CRT2)

Monitor Interface

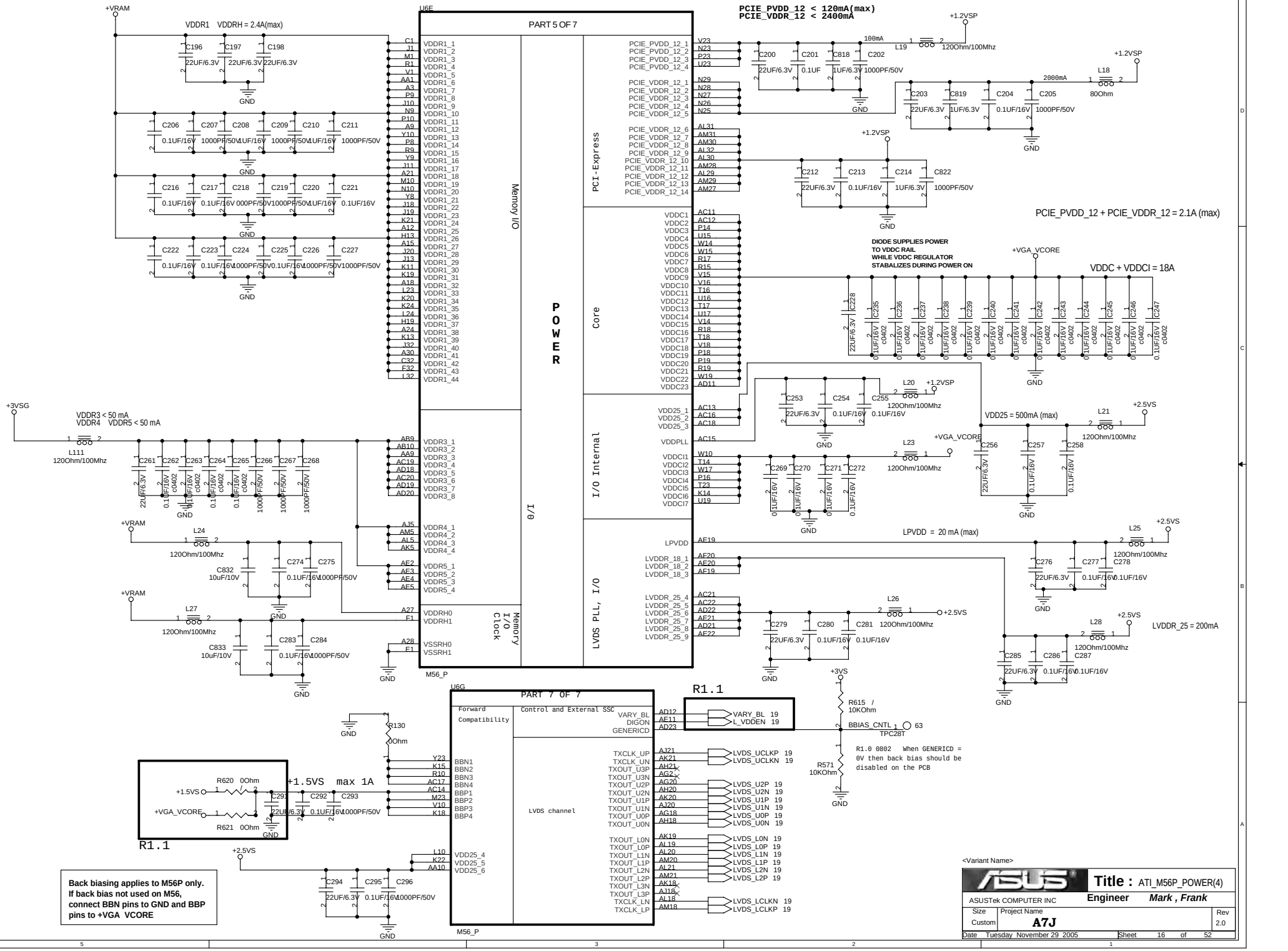
M56_P

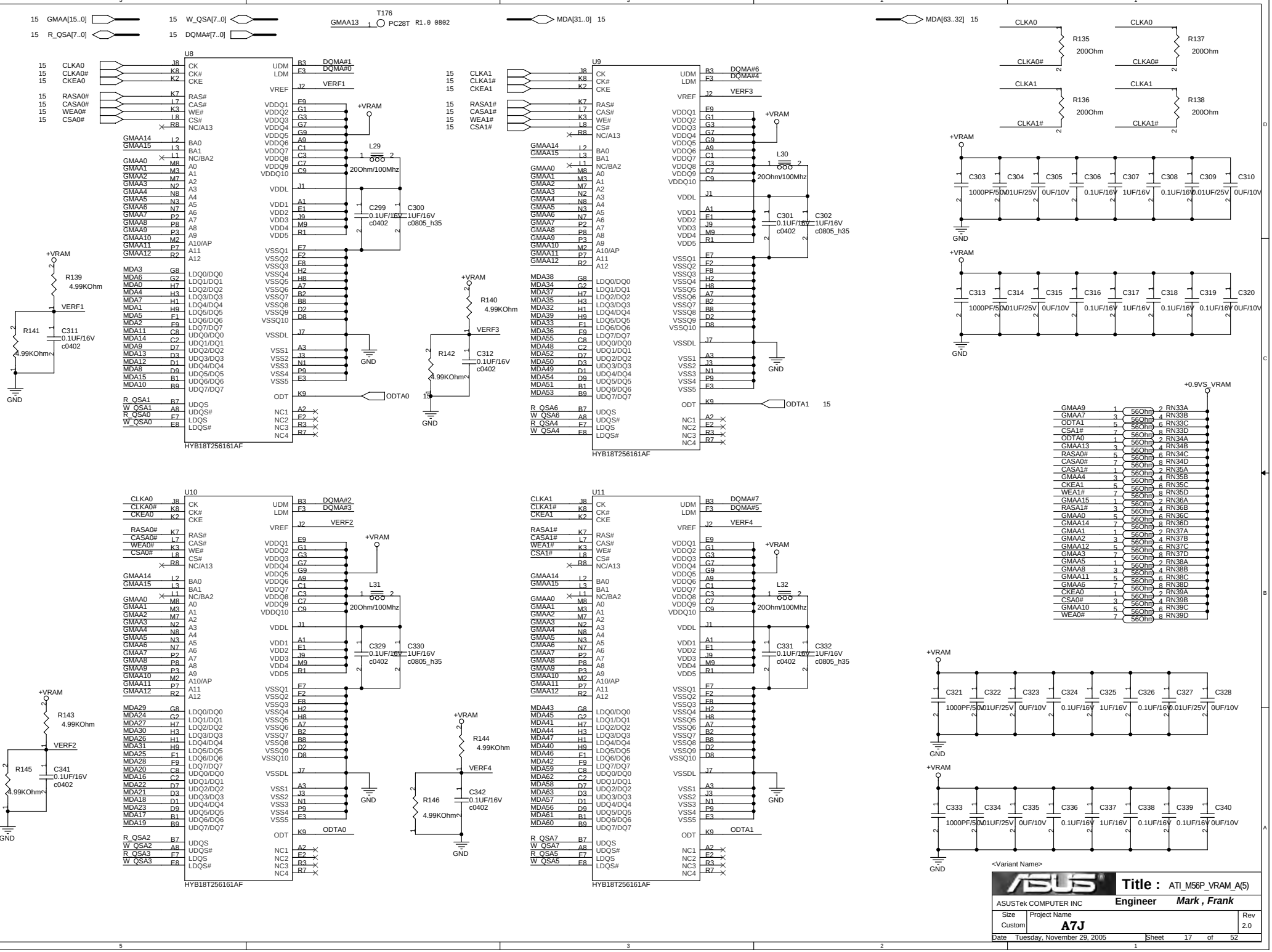
Title :	ATI_M56P_MAIN(2)		
ASUSTek COMPUTER INC	Engineer	Mark , Frank	
Size: Custom	Project Name: A7J		Rev: 2.0
Date: Tuesday November 29 2005	Sheet 14 of 52		



<Variant Name>

ASUSTek COMPUTER INC	Title : ATI_M56P_Memory(3)	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday, November 29, 2005	Sheet 15 of 52	


PCIE_PVDD_12 < 120mA(max)
PCIE_VDDR_12 < 2400mA
PCIE_PVDD_12 + PCIE_VDDR_12 = 2.1A (max)
VDDC + VDDCI = 18A
VDDR1 VDDRH = 2.4A(max)
VDDR3 < 50 mA
VDDR4 VDDR5 < 50 mA
DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON
VDD25 = 500mA (max)
LPVDD = 20 mA (max)
LVDDR_25 = 200mA
+1.5VS max 1A
R1.1
R1.1
R1.0 0802 When GENERICD = 0V then back bias should be disabled on the PCB
Back biasing applies to M56P only. If back bias not used on M56, connect BBN pins to GND and BBP pins to +VGA VCORE
PART 5 OF 7
PART 7 OF 7
POWER
Memory I/O
I/O
Core
I/O Internal
LVDS PLL, I/O
PCI-Express
Memory I/O Clock
M56_P
U6E
U6G
<Variant Name>
Title : ATI_M56P_POWER(4)
ASUSTek COMPUTER INC
Engineer Mark , Frank
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday November 29 2005
Sheet 16 of 52


15 GMAA[15..0]
15 R_QSA[7..0]
15 W_QSA[7..0]
15 DQMA#[7..0]
T176
GMAA13 1 PC28T R1.0 0802
MDA[31..0] 15
MDA[63..32] 15
U8
U9
U10
U11
HYB18T256161AF
+VRAM
+0.9VS_VRAM
GND
VERF1
VERF2
VERF3
VERF4
ODTA0
ODTA1
L29
L30
L31
L32
20Ohm/100Mhz
R135 200Ohm
R136 200Ohm
R137 200Ohm
R138 200Ohm
R139 4.99KOhm
R140 4.99KOhm
R141 4.99KOhm
R142 4.99KOhm
R143 4.99KOhm
R144 4.99KOhm
R145 4.99KOhm
R146 4.99KOhm
C299 C300 C301 C302 C303 C304 C305 C306 C307 C308 C309 C310
C311 C312 C313 C314 C315 C316 C317 C318 C319 C320
C329 C330 C331 C332 C321 C322 C323 C324 C325 C326 C327 C328
C341 C342 C333 C334 C335 C336 C337 C338 C339 C340
0.1UF/16V c0402
1UF/16V c0805_h35
1000PF/50V 0.01UF/25V 0UF/10V 0.1UF/16V 1UF/16V
RN33A RN33B RN33C RN33D RN34A RN34B RN34C RN34D RN35A RN35B RN35C RN35D RN36A RN36B RN36C RN36D RN37A RN37B RN37C RN37D RN38A RN38B RN38C RN38D RN39A RN39B RN39C RN39D
56Ohm
<Variant Name>
Title : ATI_M56P_VRAM_A(5)
ASUSTek COMPUTER INC
Engineer Mark , Frank
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday, November 29, 2005
Sheet 17 of 52

15 GMAB[15..0]
15 R_QSB[7..0]
15 W_QSB[7..0]
15 DQMB#[7..0]

GMAB13 — T177 TPC28T

MDB[31..0] 15

MDB[63..32] 15

U12

15 CLKB0
15 CLKB0#
15 CKEB0
15 RASB0#
15 CASB0#
15 WEB0#
15 CSB0#

J8 CK, K8 CK#, K2 CKE, K7 RAS#, L7 CAS#, K3 WE#, L8 CS#, R8 NC/A13

GMAB14 L2, GMAB15 L3, L1 NC/BA2, GMAB0 M8, GMAB1 M3, GMAB2 M7, GMAB3 N2, GMAB4 N8, GMAB5 N3, GMAB6 N7, GMAB7 P2, GMAB8 P8, GMAB9 P3, GMAB10 M2, GMAB11 P7, GMAB12 R2

BA0, BA1, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12

MDB10 G8, MDB13 G2, MDB11 H7, MDB12 H3, MDB15 H1, MDB9 H9, MDB14 F1, MDB8 F9, MDB5 C8, MDB0 C2, MDB4 D7, MDB3 D3, MDB2 D1, MDB6 D9, MDB1 B1, MDB7 B9

LDQ0/DQ0, LDQ1/DQ1, LDQ2/DQ2, LDQ3/DQ3, LDQ4/DQ4, LDQ5/DQ5, LDQ6/DQ6, LDQ7/DQ7, UDQ0/DQ0, UDQ1/DQ1, UDQ2/DQ2, UDQ3/DQ3, UDQ4/DQ4, UDQ5/DQ5, UDQ6/DQ6, UDQ7/DQ7

R_QSB0 B7, W_QSB0 A8, R_QSB1 F7, W_QSB1 F8

UDQS, UDQS#, LDQS, LDQS#

UDM B3, LDM F3, DQMB#0, DQMB#1, VREF J2, VERF5

VDDQ1 E9, VDDQ2 G1, VDDQ3 G3, VDDQ4 G7, VDDQ5 G9, VDDQ6 A9, VDDQ7 C1, VDDQ8 C3, VDDQ9 C7, VDDQ10 C9

VDDL J1

VDD1 A1, VDD2 E1, VDD3 J9, VDD4 M9, VDD5 R1

VSSQ1 E7, VSSQ2 F2, VSSQ3 F8, VSSQ4 H2, VSSQ5 H8, VSSQ6 A7, VSSQ7 B2, VSSQ8 B8, VSSQ9 D2, VSSQ10 D8

VSSDL J7

VSS1 A3, VSS2 J3, VSS3 N1, VSS4 P9, VSS5 F3

ODT K9 — ODTB0 15

NC1 A2, NC2 E2, NC3 R3, NC4 R7

HYB18T256161AF

+VRAM

R152 4.99KOhm — VERF5

R154 4.99KOhm — C358 0.1UF/16V c0402

GND

L33 20Ohm/100Mhz

C345 0.1UF/16V c0402

C346 1UF/16V c0805_h35

U13

15 CLKB1
15 CLKB1#
15 CKEB1
15 RASB1#
15 CASB1#
15 WEB1#
15 CSB1#

J8 CK, K8 CK#, K2 CKE, K7 RAS#, L7 CAS#, K3 WE#, L8 CS#, R8 NC/A13

GMAB14 L2, GMAB15 L3, L1 NC/BA2, GMAB0 M8, GMAB1 M3, GMAB2 M7, GMAB3 N2, GMAB4 N8, GMAB5 N3, GMAB6 N7, GMAB7 P2, GMAB8 P8, GMAB9 P3, GMAB10 M2, GMAB11 P7, GMAB12 R2

BA0, BA1, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12

MDB33 G8, MDB36 G2, MDB32 H7, MDB38 H3, MDB39 H1, MDB34 H9, MDB37 F1, MDB35 F9, MDB41 C8, MDB45 C2, MDB42 D7, MDB44 D3, MDB46 D1, MDB43 D9, MDB47 B1, MDB40 B9

LDQ0/DQ0, LDQ1/DQ1, LDQ2/DQ2, LDQ3/DQ3, LDQ4/DQ4, LDQ5/DQ5, LDQ6/DQ6, LDQ7/DQ7, UDQ0/DQ0, UDQ1/DQ1, UDQ2/DQ2, UDQ3/DQ3, UDQ4/DQ4, UDQ5/DQ5, UDQ6/DQ6, UDQ7/DQ7

R_QSB5 B7, W_QSB5 A8, R_QSB4 F7, W_QSB4 F8

UDQS, UDQS#, LDQS, LDQS#

UDM B3, LDM F3, DQMB#5, DQMB#4, VREF J2, VERF7

VDDQ1 E9, VDDQ2 G1, VDDQ3 G3, VDDQ4 G7, VDDQ5 G9, VDDQ6 A9, VDDQ7 C1, VDDQ8 C3, VDDQ9 C7, VDDQ10 C9

VDDL J1

VDD1 A1, VDD2 E1, VDD3 J9, VDD4 M9, VDD5 R1

VSSQ1 E7, VSSQ2 F2, VSSQ3 F8, VSSQ4 H2, VSSQ5 H8, VSSQ6 A7, VSSQ7 B2, VSSQ8 B8, VSSQ9 D2, VSSQ10 D8

VSSDL J7

VSS1 A3, VSS2 J3, VSS3 N1, VSS4 P9, VSS5 F3

ODT K9 — ODTB1 15

NC1 A2, NC2 E2, NC3 R3, NC4 R7

HYB18T256161AF

+VRAM

R151 4.99KOhm — VERF7

R153 4.99KOhm — C357 0.1UF/16V c0402

GND

L34 20Ohm/100Mhz

C347 0.1UF/16V c0402

C348 1UF/16V c0805_h35

CLKB0 — R147 200Ohm — R149 200Ohm — CLKB0#

CLKB1 — R148 200Ohm — R150 200Ohm — CLKB1#

+VRAM

C349 1000PF/50V, C350 0.01UF/25V, C351 10UF/10V, C352 0.1UF/16V, C353 1UF/16V, C354 0.1UF/16V, C355 0.01UF/25V, C356 10UF/10V

GND

+VRAM

C359 1000PF/50V, C360 0.01UF/25V, C361 10UF/10V, C362 0.1UF/16V, C363 1UF/16V, C364 0.1UF/16V, C365 0.1UF/16V, C366 10UF/10V

GND

U14

CLKB0
CLKB0#
CKEB0
RASB0#
CASB0#
WEB0#
CSB0#

J8 CK, K8 CK#, K2 CKE, K7 RAS#, L7 CAS#, K3 WE#, L8 CS#, R8 NC/A13

GMAB14 L2, GMAB15 L3, L1 NC/BA2, GMAB0 M8, GMAB1 M3, GMAB2 M7, GMAB3 N2, GMAB4 N8, GMAB5 N3, GMAB6 N7, GMAB7 P2, GMAB8 P8, GMAB9 P3, GMAB10 M2, GMAB11 P7, GMAB12 R2

BA0, BA1, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12

MDB21 G8, MDB19 G2, MDB22 H7, MDB23 H3, MDB18 H1, MDB16 H9, MDB20 F1, MDB17 F9, MDB24 C8, MDB28 C2, MDB27 D7, MDB30 D3, MDB29 D1, MDB25 D9, MDB31 B1, MDB26 B9

LDQ0/DQ0, LDQ1/DQ1, LDQ2/DQ2, LDQ3/DQ3, LDQ4/DQ4, LDQ5/DQ5, LDQ6/DQ6, LDQ7/DQ7, UDQ0/DQ0, UDQ1/DQ1, UDQ2/DQ2, UDQ3/DQ3, UDQ4/DQ4, UDQ5/DQ5, UDQ6/DQ6, UDQ7/DQ7

R_QSB3 B7, W_QSB3 A8, R_QSB2 F7, W_QSB2 F8

UDQS, UDQS#, LDQS, LDQS#

UDM B3, LDM F3, DQMB#3, DQMB#2, VREF J2, VERF6

VDDQ1 E9, VDDQ2 G1, VDDQ3 G3, VDDQ4 G7, VDDQ5 G9, VDDQ6 A9, VDDQ7 C1, VDDQ8 C3, VDDQ9 C7, VDDQ10 C9

VDDL J1

VDD1 A1, VDD2 E1, VDD3 J9, VDD4 M9, VDD5 R1

VSSQ1 E7, VSSQ2 F2, VSSQ3 F8, VSSQ4 H2, VSSQ5 H8, VSSQ6 A7, VSSQ7 B2, VSSQ8 B8, VSSQ9 D2, VSSQ10 D8

VSSDL J7

VSS1 A3, VSS2 J3, VSS3 N1, VSS4 P9, VSS5 F3

ODT K9 — ODTB0

NC1 A2, NC2 E2, NC3 R3, NC4 R7

HYB18T256161AF

+VRAM

R156 4.99KOhm — VERF6

R158 4.99KOhm — C388 0.1UF/16V c0402

GND

L35 20Ohm/100Mhz

C375 0.1UF/16V c0402

C376 1UF/16V c0805_h35

U15

CLKB1
CLKB1#
CKEB1
RASB1#
CASB1#
WEB1#
CSB1#

J8 CK, K8 CK#, K2 CKE, K7 RAS#, L7 CAS#, K3 WE#, L8 CS#, R8 NC/A13

GMAB14 L2, GMAB15 L3, L1 NC/BA2, GMAB0 M8, GMAB1 M3, GMAB2 M7, GMAB3 N2, GMAB4 N8, GMAB5 N3, GMAB6 N7, GMAB7 P2, GMAB8 P8, GMAB9 P3, GMAB10 M2, GMAB11 P7, GMAB12 R2

BA0, BA1, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12

MDB51 G8, MDB52 G2, MDB50 H7, MDB55 H3, MDB54 H1, MDB49 H9, MDB53 F1, MDB48 F9, MDB60 C8, MDB62 C2, MDB61 D7, MDB63 D3, MDB56 D1, MDB57 D9, MDB58 B1, MDB59 B9

LDQ0/DQ0, LDQ1/DQ1, LDQ2/DQ2, LDQ3/DQ3, LDQ4/DQ4, LDQ5/DQ5, LDQ6/DQ6, LDQ7/DQ7, UDQ0/DQ0, UDQ1/DQ1, UDQ2/DQ2, UDQ3/DQ3, UDQ4/DQ4, UDQ5/DQ5, UDQ6/DQ6, UDQ7/DQ7

R_QSB7 B7, W_QSB7 A8, R_QSB6 F7, W_QSB6 F8

UDQS, UDQS#, LDQS, LDQS#

UDM B3, LDM F3, DQMB#7, DQMB#6, VREF J2, VERF8

VDDQ1 E9, VDDQ2 G1, VDDQ3 G3, VDDQ4 G7, VDDQ5 G9, VDDQ6 A9, VDDQ7 C1, VDDQ8 C3, VDDQ9 C7, VDDQ10 C9

VDDL J1

VDD1 A1, VDD2 E1, VDD3 J9, VDD4 M9, VDD5 R1

VSSQ1 E7, VSSQ2 F2, VSSQ3 F8, VSSQ4 H2, VSSQ5 H8, VSSQ6 A7, VSSQ7 B2, VSSQ8 B8, VSSQ9 D2, VSSQ10 D8

VSSDL J7

VSS1 A3, VSS2 J3, VSS3 N1, VSS4 P9, VSS5 F3

ODT K9 — ODTB1

NC1 A2, NC2 E2, NC3 R3, NC4 R7

HYB18T256161AF

+VRAM

R155 4.99KOhm — VERF8

R157 4.99KOhm — C387 0.1UF/16V c0402

GND

L36 20Ohm/100Mhz

C377 0.1UF/16V c0402

C378 1UF/16V c0805_h35

+0.9VS_VRAM

GMAB5 1 — 56Ohm — 2 RN40A
GMAB7 3 — 56Ohm — 4 RN40B
GMAB1 5 — 56Ohm — 6 RN40C
GMAB6 7 — 56Ohm — 8 RN40D
GMAB15 1 — 56Ohm — 2 RN41A
GMAB0 3 — 56Ohm — 4 RN41B
GMAB4 5 — 56Ohm — 6 RN41C
GMAB3 7 — 56Ohm — 8 RN41D
GMAB8 1 — 56Ohm — 2 RN42A
GMAB11 3 — 56Ohm — 4 RN42B
GMAB10 5 — 56Ohm — 6 RN42C
GMAB13 7 — 56Ohm — 8 RN42D
WEB1# 1 — 56Ohm — 2 RN44A
CASB1# 3 — 56Ohm — 4 RN44B
CSB1# 5 — 56Ohm — 6 RN44C
ODTB1 7 — 56Ohm — 8 RN44D
GMAB12 1 — 56Ohm — 2 RN45A
GMAB9 3 — 56Ohm — 4 RN45B
GMAB2 5 — 56Ohm — 6 RN45C
GMAB14 7 — 56Ohm — 8 RN45D
CKEB0 1 — 56Ohm — 2 RN46A
RASB0# 3 — 56Ohm — 4 RN46B
CASB0# 5 — 56Ohm — 6 RN46C
CSB0# 7 — 56Ohm — 8 RN46D

WEB0# 1 — R616 56Ohm — 2
ODTB0 1 — R617 56Ohm — 2
CKEB1 1 — R618 56Ohm — 2
RASB1# 1 — R619 56Ohm — 2

+VRAM

C367 1000PF/50V, C368 0.01UF/25V, C369 10UF/10V, C370 0.1UF/16V, C371 1UF/16V, C372 0.1UF/16V, C373 0.01UF/25V, C374 10UF/10V

GND

+VRAM

C379 1000PF/50V, C380 0.01UF/25V, C381 10UF/10V, C382 0.1UF/16V, C383 1UF/16V, C384 0.1UF/16V, C385 0.1UF/16V, C386 10UF/10V

GND

<Variant Name>

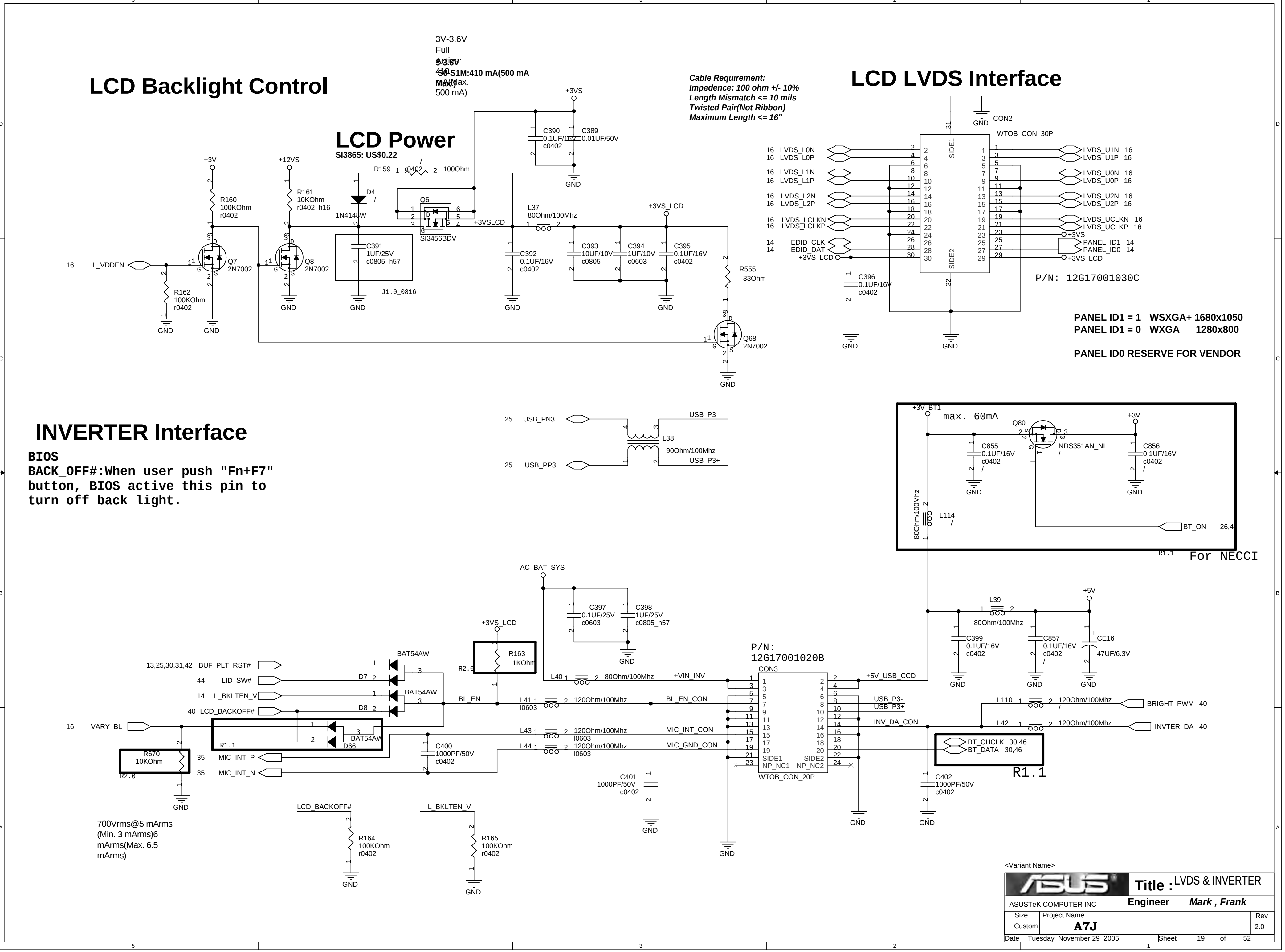
ASUSTek COMPUTER INC

Title : ATI_M56P_VRAM_B(6)

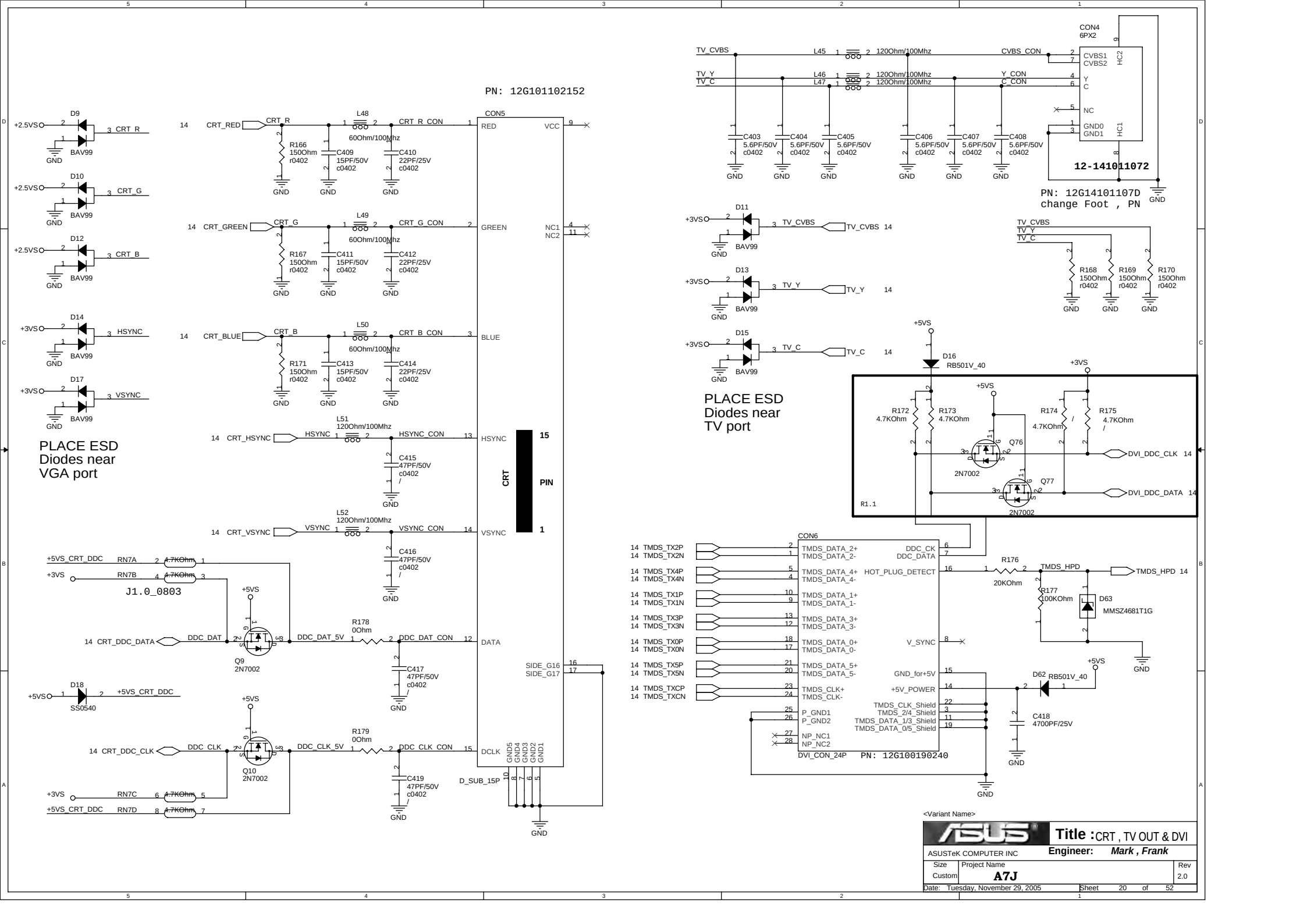
Engineer Mark , Frank

Size	Project Name	Rev
Custom	A7J	2.0

Date Tuesday November 29 2005 Sheet 18 of 52



LCD Backlight Control
LCD Power
SI3865: US$0.22
3V-3.6V
Full Active:
S0-S1M:410 mA(500 mA Max)
+3V
+12VS
+3VS
+3VS_LCD
+3VSLCD
L_VDDEN
R160 100KOhm r0402
R161 10KOhm r0402_h16
R162 100KOhm r0402
Q7 2N7002
Q8 2N7002
Q6 SI3456BDV
D4 1N4148W
R159 r0402 100Ohm
C391 1UF/25V c0805_h57
J1.0_0816
C390 0.1UF/16V c0402
C389 0.01UF/50V
L37 80Ohm/100Mhz
C392 0.1UF/16V c0402
C393 10UF/10V c0805
C394 1UF/10V c0603
C395 0.1UF/16V c0402
R555 33Ohm
Q68 2N7002
GND
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"
LCD LVDS Interface
CON2
WTOB_CON_30P
LVDS_L0N
LVDS_L0P
LVDS_L1N
LVDS_L1P
LVDS_L2N
LVDS_L2P
LVDS_LCLKN
LVDS_LCLKP
EDID_CLK
EDID_DAT
LVDS_U1N
LVDS_U1P
LVDS_U0N
LVDS_U0P
LVDS_U2N
LVDS_U2P
LVDS_UCLKN
LVDS_UCLKP
PANEL_ID1
PANEL_ID0
C396 0.1UF/16V c0402
P/N: 12G17001030C
PANEL ID1 = 1 WSXGA+ 1680x1050
PANEL ID1 = 0 WXGA 1280x800
PANEL ID0 RESERVE FOR VENDOR
INVERTER Interface
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.
USB_PN3
USB_PP3
USB_P3-
USB_P3+
L38 90Ohm/100Mhz
+3V_BT1
max. 60mA
Q80 NDS351AN_NL
C855 0.1UF/16V c0402
C856 0.1UF/16V c0402
L114 80Ohm/100Mhz
BT_ON 26,4
R1.1
For NECCI
AC_BAT_SYS
C397 0.1UF/25V c0603
C398 1UF/25V c0805_h57
+5V
L39 80Ohm/100Mhz
C399 0.1UF/16V c0402
C857 0.1UF/16V c0402
CE16 47UF/6.3V
BUF_PLT_RST#
LID_SW#
L_BKLTEN_V
LCD_BACKOFF#
VARY_BL
BAT54AW
D7
D8
D66
R163 1KOhm
R2.0
BL_EN
L40 80Ohm/100Mhz
L41 120Ohm/100Mhz I0603
L43 120Ohm/100Mhz I0603
L44 120Ohm/100Mhz I0603
+VIN_INV
BL_EN_CON
MIC_INT_CON
MIC_GND_CON
P/N: 12G17001020B
CON3
WTOB_CON_20P
+5V_USB_CCD
INV_DA_CON
L110 120Ohm/100Mhz
L42 120Ohm/100Mhz
BRIGHT_PWM 40
INVTER_DA 40
BT_CHCLK 30,46
BT_DATA 30,46
R670 10KOhm
MIC_INT_P
MIC_INT_N
C400 1000PF/50V c0402
C401 1000PF/50V c0402
C402 1000PF/50V c0402
R164 100KOhm r0402
R165 100KOhm r0402
700Vrms@5 mArms (Min. 3 mArms)6 mArms(Max. 6.5 mArms)
<Variant Name>
Title : LVDS & INVERTER
ASUSTeK COMPUTER INC
Engineer Mark , Frank
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday November 29 2005
Sheet 19 of 52



<Variant Name>

Title : CRT , TV OUT & DVI

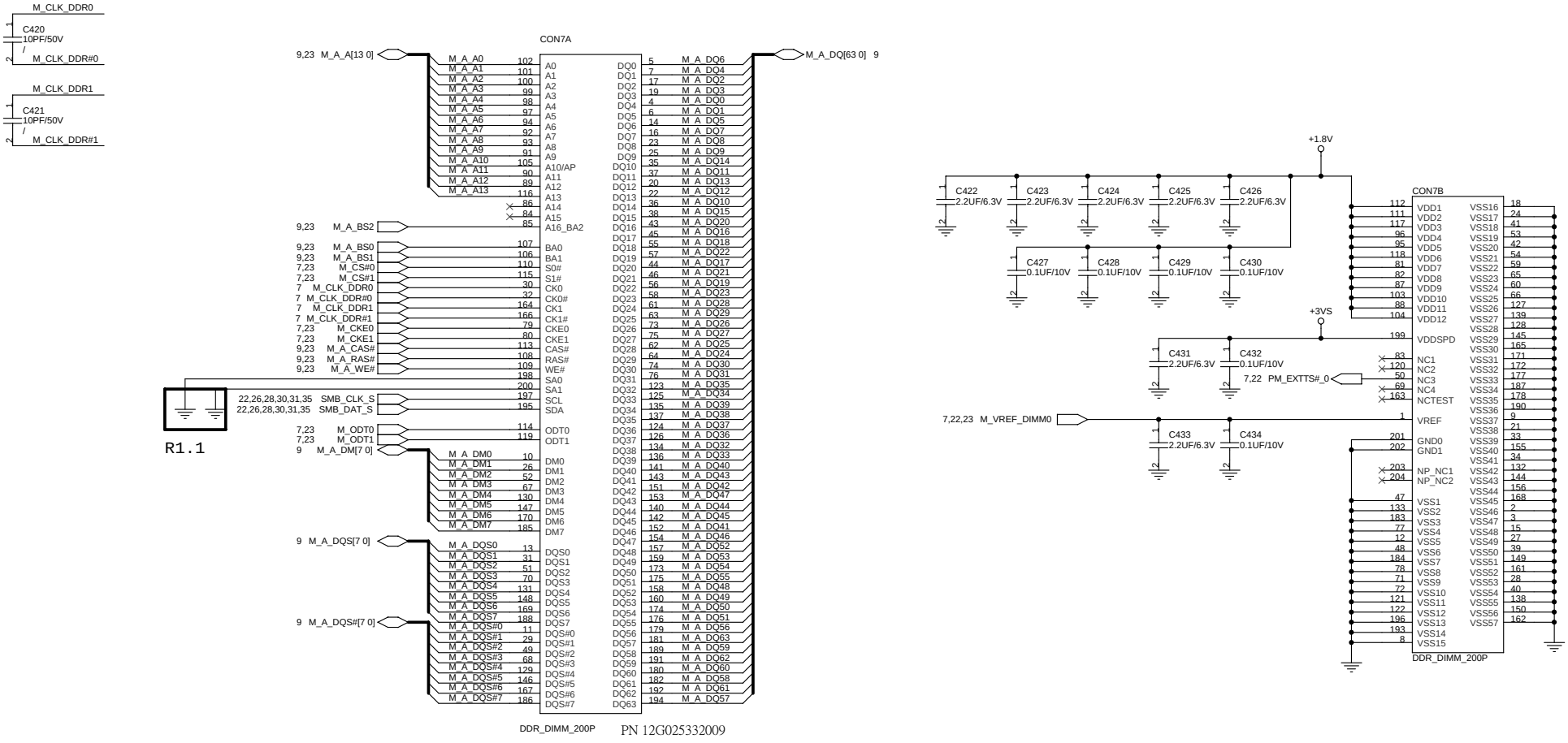
ASUSTeK COMPUTER INC

Engineer: *Mark , Frank*

Size	Project Name	Rev
Custom	**A7J**	2.0

Date: Tuesday, November 29, 2005 Sheet 20 of 52

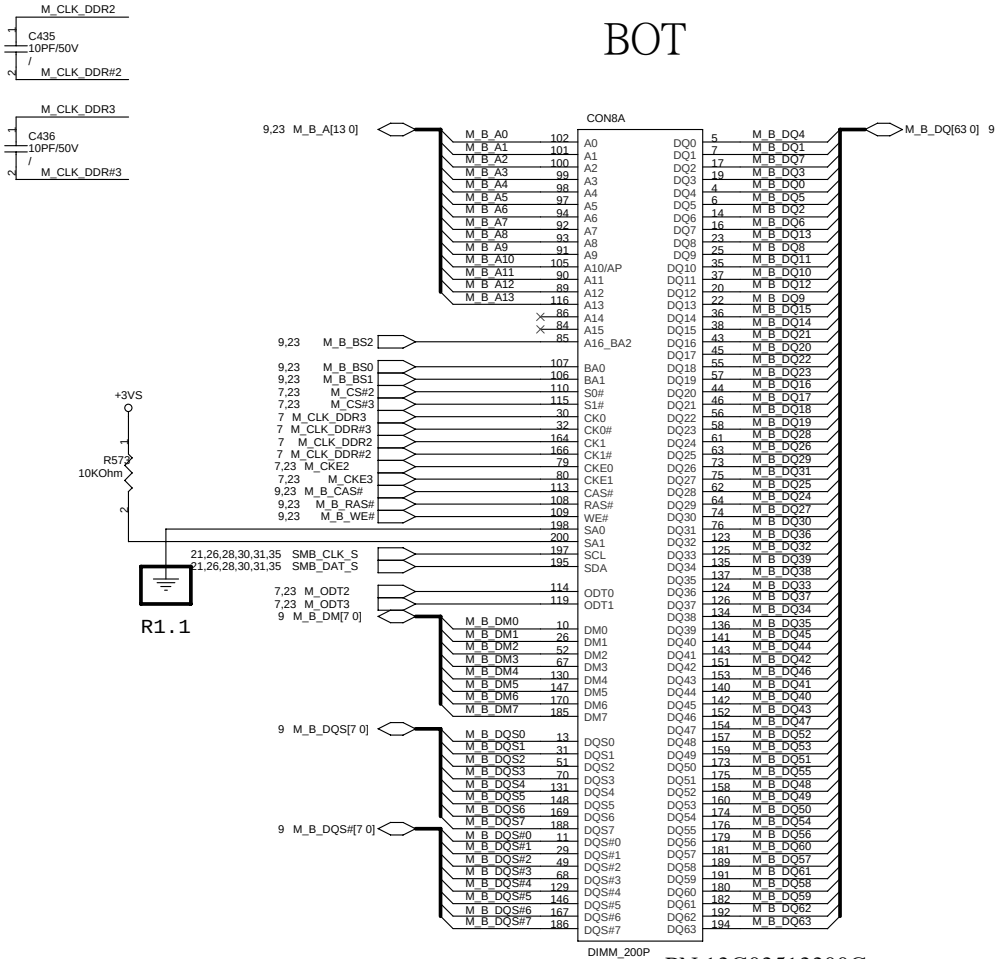
TOP



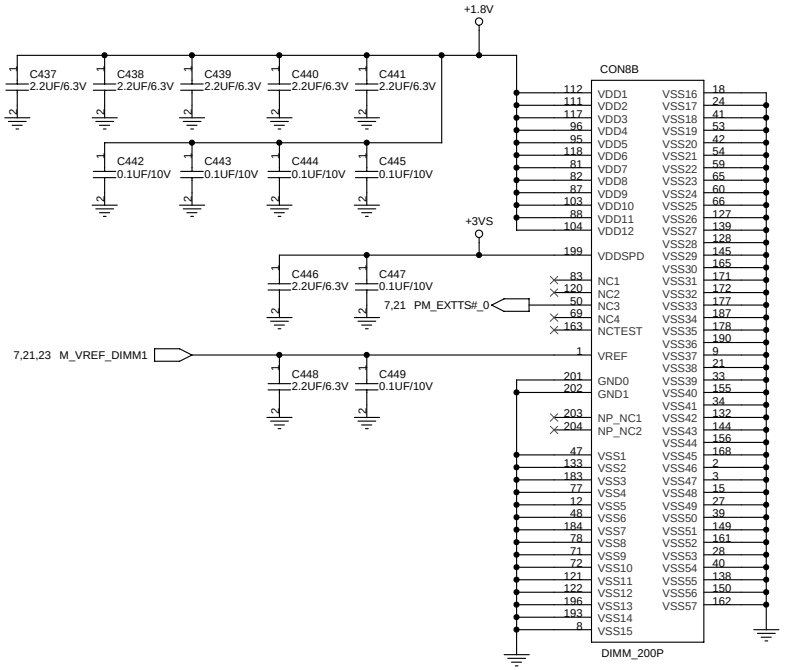
<Variant Name>

ASUSTeK COMPUTER INC. NB1	**Title :** DDR2 SO-DIMM1	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 21 of 52	

BOT



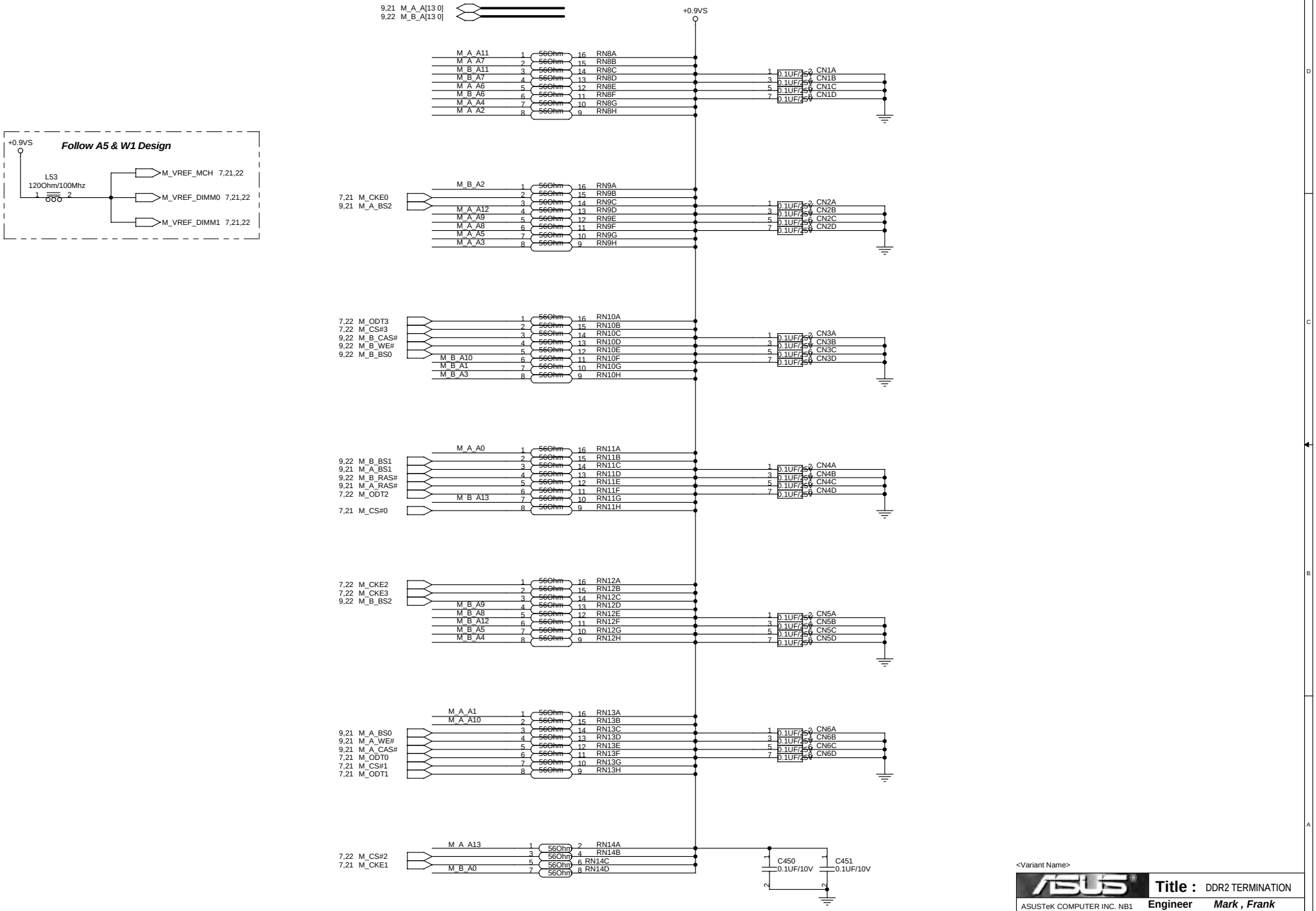
PN:12G02512200G



PN:12G02512200G

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 22 of 52	



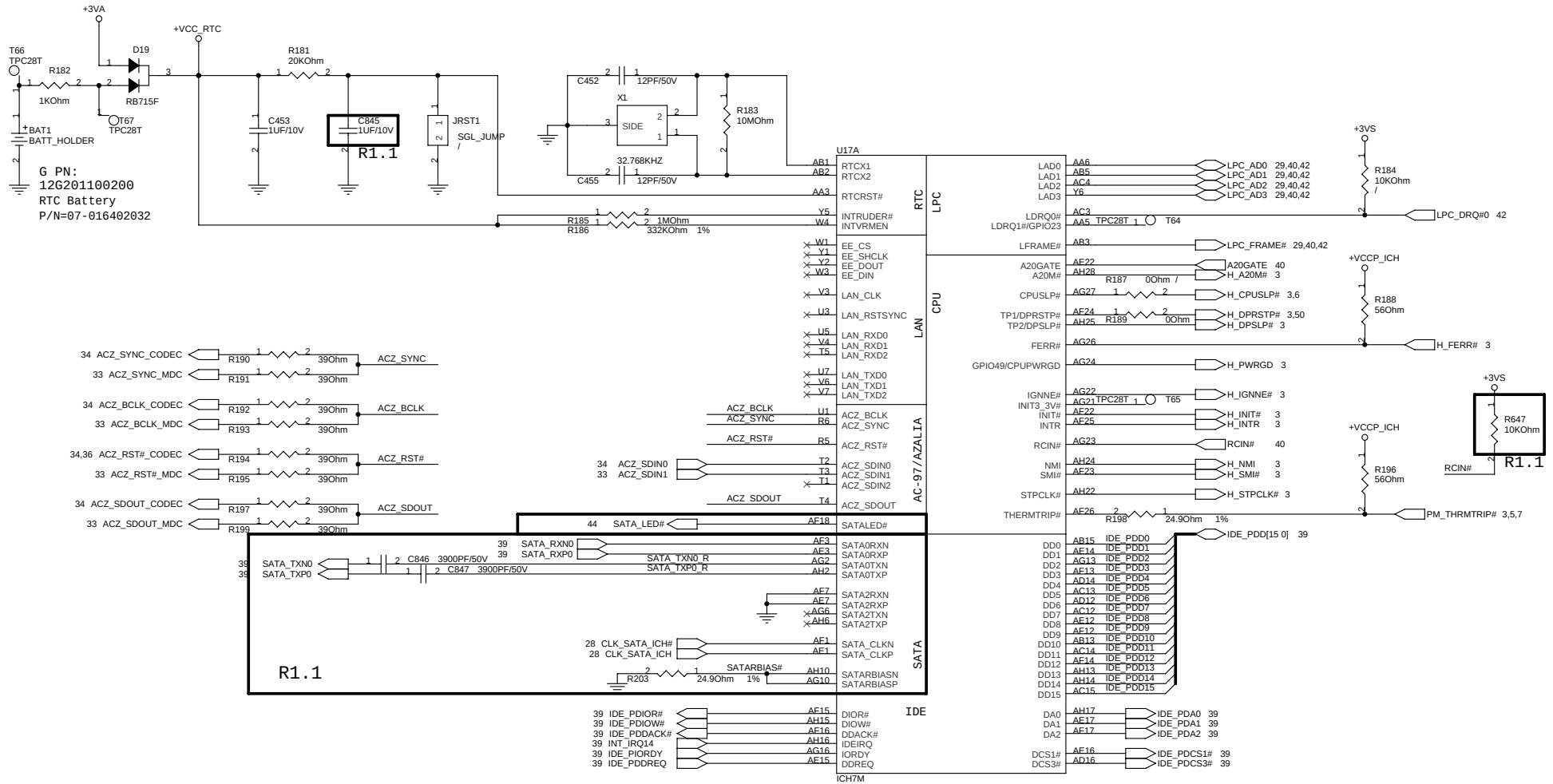
<Variant Name>

Title : DDR2 TERMINATION

ASUSTeK COMPUTER INC. NB1 **Engineer** ***Mark , Frank***

Size	Project Name	Rev
Custom	**A7J**	2.0

Date Tuesday November 29 2005 Sheet 23 of 52



<Variant Name>

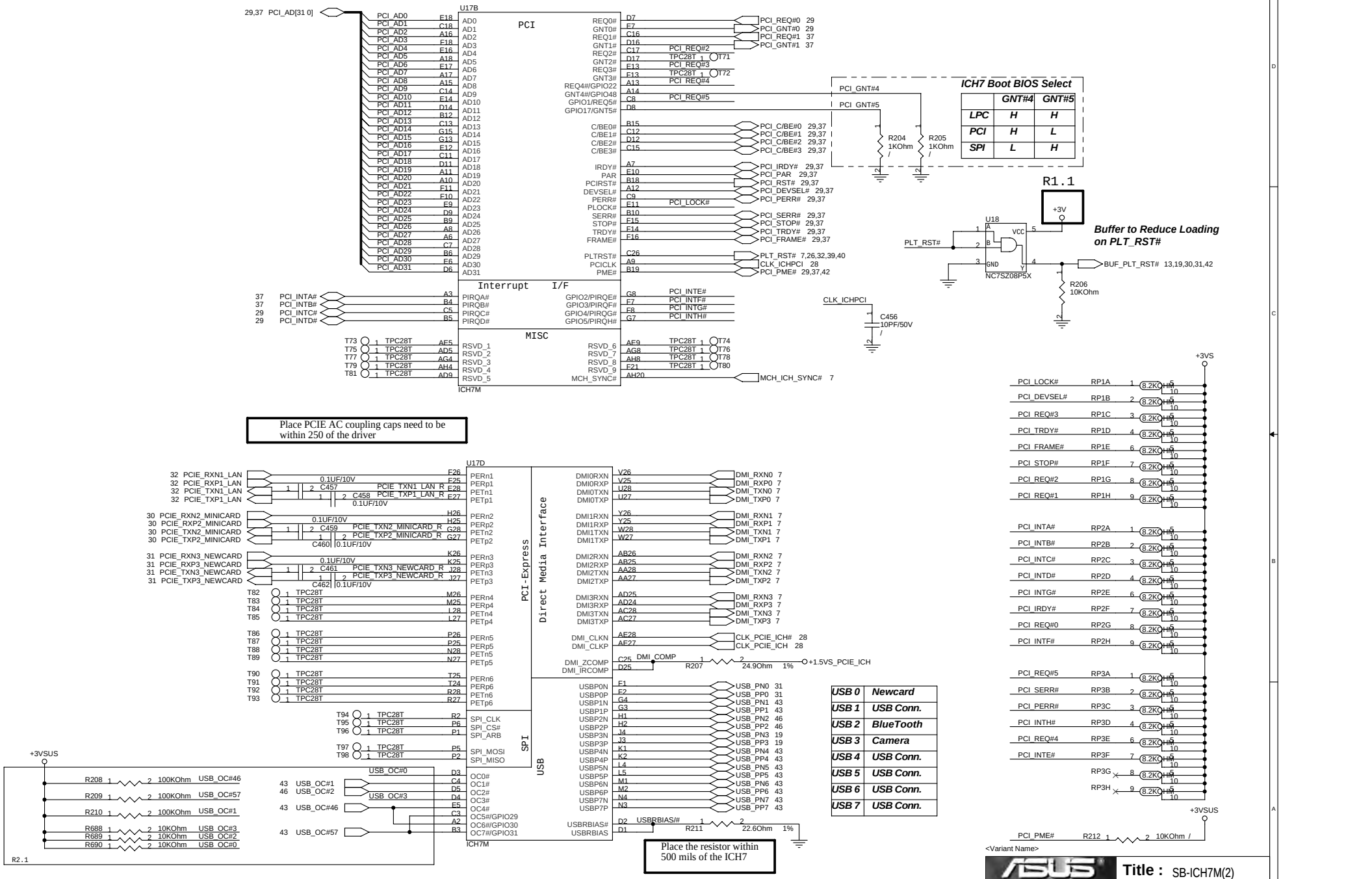
ASUSTeK COMPUTER INC. NB1

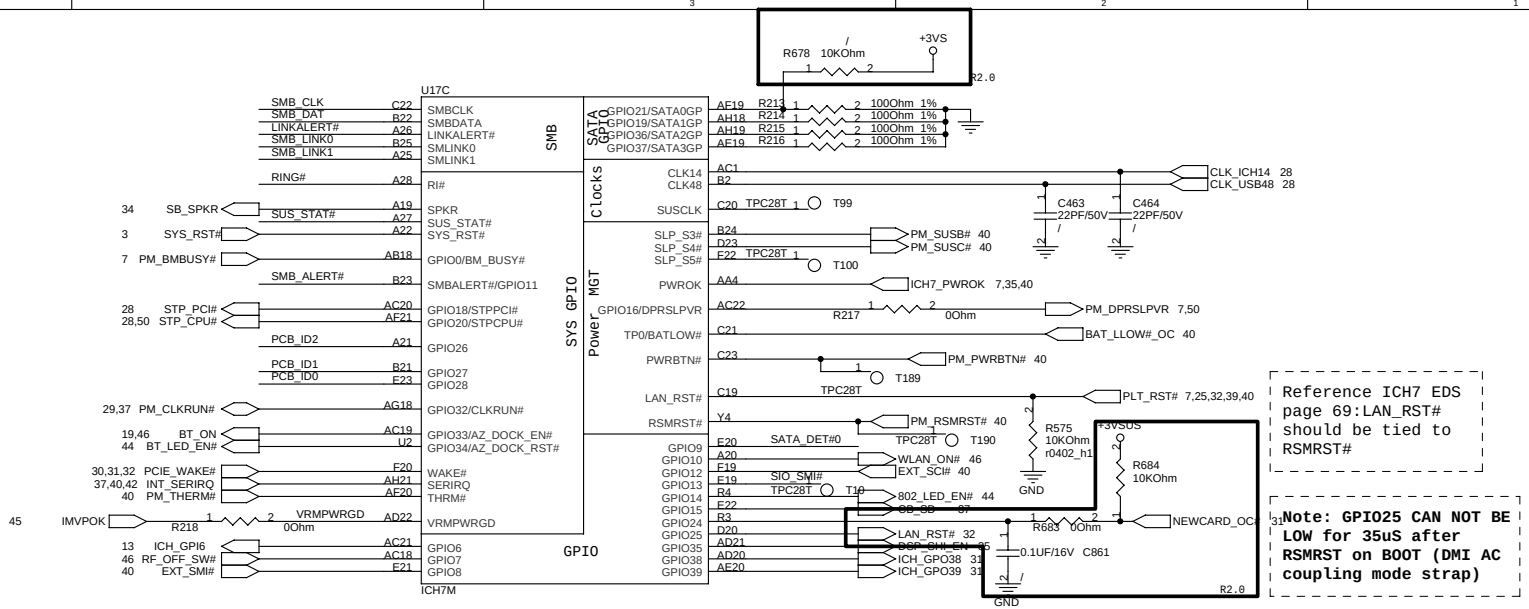
Title : SB-ICH7-M(1)

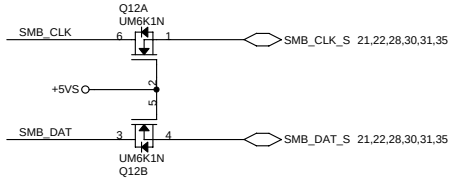
Engineer *Mark , Frank*

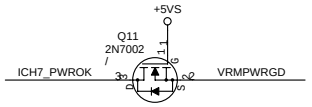
Size	Project Name	Rev
Custom	**A7J**	2.0

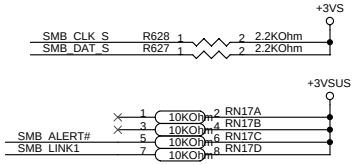
Date Tuesday November 29 2005 Sheet 24 of 52

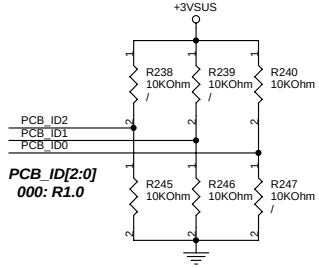

U17B
PCI
Interrupt I/F
MISC
ICH7M
ICH7 Boot BIOS Select
GNT#4 GNT#5
LPC H H
PCI H L
SPI L H
R1.1
Buffer to Reduce Loading on PLT_RST#
NC7SZ08P5X
Place PCIE AC coupling caps need to be within 250 of the driver
U17D
PCI-Express
Direct Media Interface
USB
SPI
USB_OC#46
USB_OC#57
R2.1
Place the resistor within 500 mils of the ICH7
USB 0 Newcard
USB 1 USB Conn.
USB 2 BlueTooth
USB 3 Camera
USB 4 USB Conn.
USB 5 USB Conn.
USB 6 USB Conn.
USB 7 USB Conn.
Title : SB-ICH7M(2)
ASUSTeK COMPUTER INC. NB1
Engineer Mark , Frank
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday November 29 2005
Sheet 25 of 52

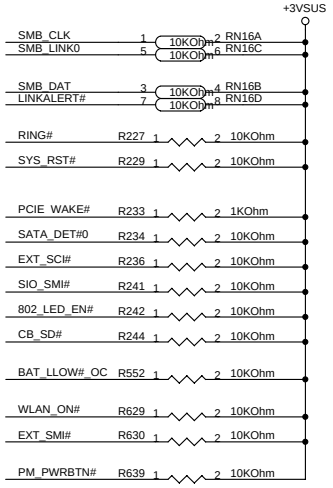


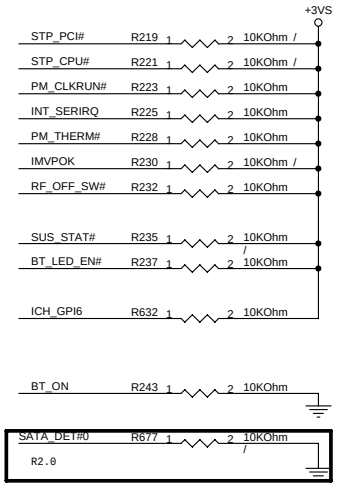


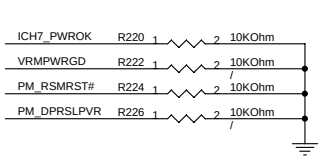






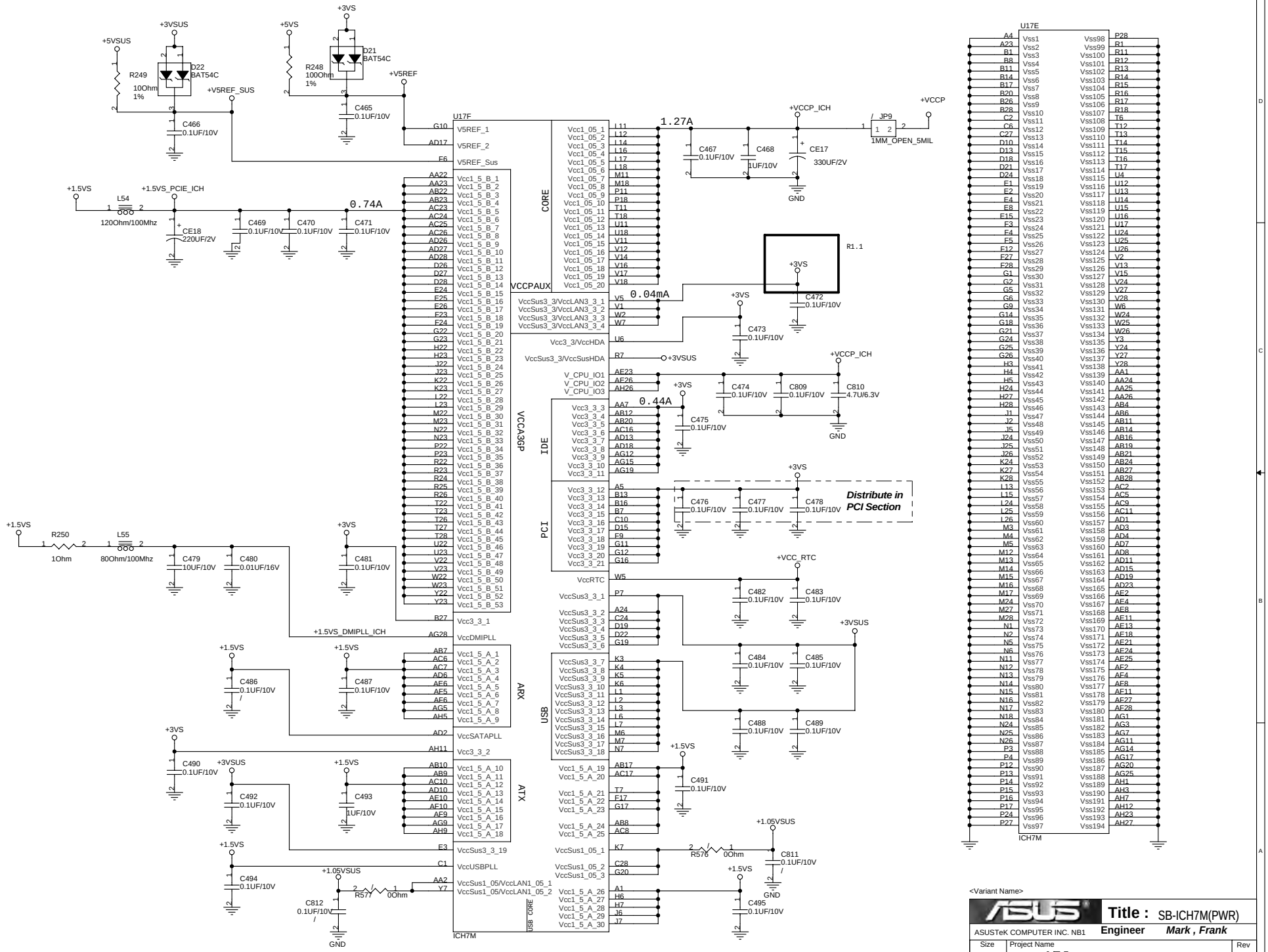






<variant_name>

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(3)	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 26 of 52	


+3VSUS
+5VSUS
+5VS
+3VS
+V5REF
+V5REF_SUS
R249
10Ohm
1%
D22
BAT54C
R248
100Ohm
1%
D21
BAT54C
C465
0.1UF/10V
C466
0.1UF/10V
U17F
V5REF_1
V5REF_2
V5REF_Sus
+1.5VS
+1.5VS_PCIE_ICH
L54
120Ohm/100Mhz
0.74A
CE18
220UF/2V
C469
0.1UF/10V
C470
0.1UF/10V
C471
0.1UF/10V
Vcc1_5_B_1
Vcc1_5_B_2
Vcc1_5_B_3
Vcc1_5_B_4
Vcc1_5_B_5
Vcc1_5_B_6
Vcc1_5_B_7
Vcc1_5_B_8
Vcc1_5_B_9
Vcc1_5_B_10
Vcc1_5_B_11
Vcc1_5_B_12
Vcc1_5_B_13
Vcc1_5_B_14
Vcc1_5_B_15
Vcc1_5_B_16
Vcc1_5_B_17
Vcc1_5_B_18
Vcc1_5_B_19
Vcc1_5_B_20
Vcc1_5_B_21
Vcc1_5_B_22
Vcc1_5_B_23
Vcc1_5_B_24
Vcc1_5_B_25
Vcc1_5_B_26
Vcc1_5_B_27
Vcc1_5_B_28
Vcc1_5_B_29
Vcc1_5_B_30
Vcc1_5_B_31
Vcc1_5_B_32
Vcc1_5_B_33
Vcc1_5_B_34
Vcc1_5_B_35
Vcc1_5_B_36
Vcc1_5_B_37
Vcc1_5_B_38
Vcc1_5_B_39
Vcc1_5_B_40
Vcc1_5_B_41
Vcc1_5_B_42
Vcc1_5_B_43
Vcc1_5_B_44
Vcc1_5_B_45
Vcc1_5_B_46
Vcc1_5_B_47
Vcc1_5_B_48
Vcc1_5_B_49
Vcc1_5_B_50
Vcc1_5_B_51
Vcc1_5_B_52
Vcc1_5_B_53
Vcc3_3_1
+1.5VS_DMIPLL_ICH
VccDMIPLL
Vcc1_5_A_1
Vcc1_5_A_2
Vcc1_5_A_3
Vcc1_5_A_4
Vcc1_5_A_5
Vcc1_5_A_6
Vcc1_5_A_7
Vcc1_5_A_8
Vcc1_5_A_9
VccSATAPLL
Vcc3_3_2
Vcc1_5_A_10
Vcc1_5_A_11
Vcc1_5_A_12
Vcc1_5_A_13
Vcc1_5_A_14
Vcc1_5_A_15
Vcc1_5_A_16
Vcc1_5_A_17
Vcc1_5_A_18
VccSus3_3_19
VccUSBPLL
VccSus1_05/VccLAN1_05_1
VccSus1_05/VccLAN1_05_2
ICH7M
CORE
VCCAUXP
IDE
PCI
ARX
ATX
USB
USB CORE
Vcc1_05_1
Vcc1_05_2
Vcc1_05_3
Vcc1_05_4
Vcc1_05_5
Vcc1_05_6
Vcc1_05_7
Vcc1_05_8
Vcc1_05_9
Vcc1_05_10
Vcc1_05_11
Vcc1_05_12
Vcc1_05_13
Vcc1_05_14
Vcc1_05_15
Vcc1_05_16
Vcc1_05_17
Vcc1_05_18
Vcc1_05_19
Vcc1_05_20
1.27A
+VCCP_ICH
+VCCP
JP9
1MM_OPEN_5MIL
C467
0.1UF/10V
C468
1UF/10V
CE17
330UF/2V
GND
R1.1
C472
0.1UF/10V
VccSus3_3/VccLAN3_3_1
VccSus3_3/VccLAN3_3_2
VccSus3_3/VccLAN3_3_3
VccSus3_3/VccLAN3_3_4
0.04mA
C473
0.1UF/10V
Vcc3_3/VccHDA
VccSus3_3/VccSusHDA
+3VSUS
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
0.44A
C474
0.1UF/10V
C809
0.1UF/10V
C810
4.7U/6.3V
C475
0.1UF/10V
Vcc3_3_3
Vcc3_3_4
Vcc3_3_5
Vcc3_3_6
Vcc3_3_7
Vcc3_3_8
Vcc3_3_9
Vcc3_3_10
Vcc3_3_11
Vcc3_3_12
Vcc3_3_13
Vcc3_3_14
Vcc3_3_15
Vcc3_3_16
Vcc3_3_17
Vcc3_3_18
Vcc3_3_19
Vcc3_3_20
Vcc3_3_21
Distribute in
PCI Section
C476
0.1UF/10V
C477
0.1UF/10V
C478
0.1UF/10V
VccRTC
+VCC_RTC
C482
0.1UF/10V
C483
0.1UF/10V
VccSus3_3_1
VccSus3_3_2
VccSus3_3_3
VccSus3_3_4
VccSus3_3_5
VccSus3_3_6
C484
0.1UF/10V
C485
0.1UF/10V
VccSus3_3_7
VccSus3_3_8
VccSus3_3_9
VccSus3_3_10
VccSus3_3_11
VccSus3_3_12
VccSus3_3_13
VccSus3_3_14
VccSus3_3_15
VccSus3_3_16
VccSus3_3_17
VccSus3_3_18
C488
0.1UF/10V
C489
0.1UF/10V
Vcc1_5_A_19
Vcc1_5_A_20
Vcc1_5_A_21
Vcc1_5_A_22
Vcc1_5_A_23
Vcc1_5_A_24
Vcc1_5_A_25
C491
0.1UF/10V
VccSus1_05_1
VccSus1_05_2
VccSus1_05_3
R576
0Ohm
+1.05VSUS
C811
0.1UF/10V
Vcc1_5_A_26
Vcc1_5_A_27
Vcc1_5_A_28
Vcc1_5_A_29
Vcc1_5_A_30
C495
0.1UF/10V
R577
0Ohm
C812
0.1UF/10V
R250
1Ohm
L55
80Ohm/100Mhz
C479
10UF/10V
C480
0.01UF/16V
C481
0.1UF/10V
C486
0.1UF/10V
C487
0.1UF/10V
C490
0.1UF/10V
C492
0.1UF/10V
C493
1UF/10V
C494
0.1UF/10V
U17E
Vss1
Vss2
Vss3
Vss4
Vss5
Vss6
Vss7
Vss8
Vss9
Vss10
Vss11
Vss12
Vss13
Vss14
Vss15
Vss16
Vss17
Vss18
Vss19
Vss20
Vss21
Vss22
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Vss28
Vss29
Vss30
Vss31
Vss32
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Vss63
Vss64
Vss65
Vss66
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Vss69
Vss70
Vss71
Vss72
Vss73
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Vss78
Vss79
Vss80
Vss81
Vss82
Vss83
Vss84
Vss85
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Vss87
Vss88
Vss89
Vss90
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Vss94
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Vss98
Vss99
Vss100
Vss101
Vss102
Vss103
Vss104
Vss105
Vss106
Vss107
Vss108
Vss109
Vss110
Vss111
Vss112
Vss113
Vss114
Vss115
Vss116
Vss117
Vss118
Vss119
Vss120
Vss121
Vss122
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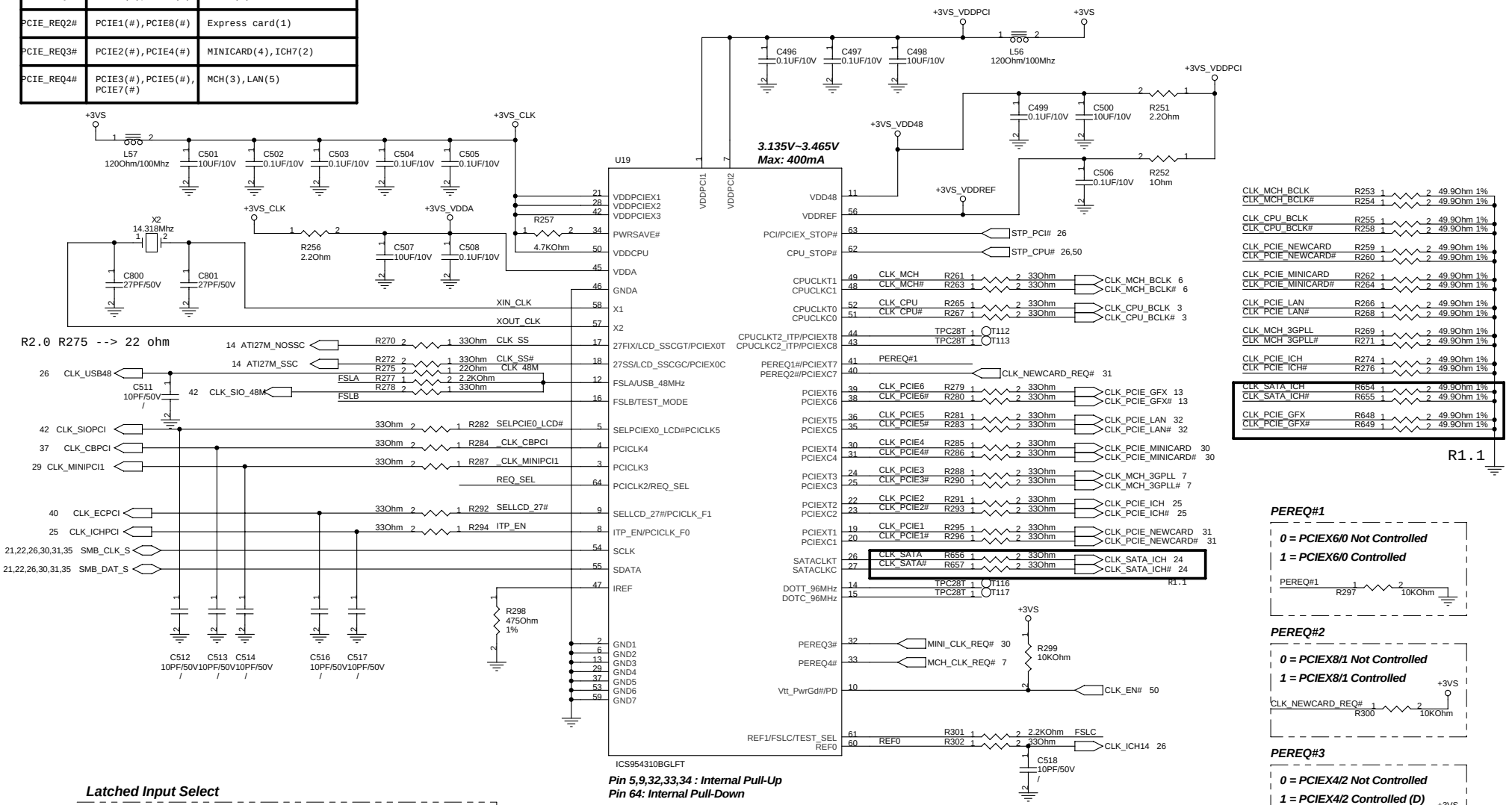
Vss127
Vss128
Vss129
Vss130
Vss131
Vss132
Vss133
Vss134
Vss135
Vss136
Vss137
Vss138
Vss139
Vss140
Vss141
Vss142
Vss143
Vss144
Vss145
Vss146
Vss147
Vss148
Vss149
Vss150
Vss151
Vss152
Vss153
Vss154
Vss155
Vss156
Vss157
Vss158
Vss159
Vss160
Vss161
Vss162
Vss163
Vss164
Vss165
Vss166
Vss167
Vss168
Vss169
Vss170
Vss171
Vss172
Vss173
Vss174
Vss175
Vss176
Vss177
Vss178
Vss179
Vss180
Vss181
Vss182
Vss183
Vss184
Vss185
Vss186
Vss187
Vss188
Vss189
Vss190
Vss191
Vss192
Vss193
Vss194
ICH7M
<Variant Name>
Title : SB-ICH7M(PWR)
ASUSTeK COMPUTER INC. NB1
Engineer Mark , Frank
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday November 29 2005
Sheet 27 of 52

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	M56(6)
PCIE_REQ2#	PCIE1(#),PCIE8(#)	Express card(1)
PCIE_REQ3#	PCIE2(#),PCIE4(#)	MINICARD(4),ICH7(2)
PCIE_REQ4#	PCIE3(#),PCIE5(#),PCIE7(#)	MCH(3),LAN(5)



Latched Input Select

ITP_EN/PCICLK_F0
- 0 = SRC Pair
- 1 = CPU_ITP Pair

SELPCIE0_LCD#/PCI_CLK5
- 0 = LCD Clock (96MHz)
- 1 = PCI Express (100MHz) (D)

PCI_CLK2/REQ_SEL
- 0 = PCICLK(D)
- 1 = PEREQ#

SELLCD_27#/PCICLK_F1
- 0 = 27MHzSS/27MHzSS# Pair
- 1 = LCD_CLK Pair (D)

Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down

Reserved for Debug & Expriment

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

PEREQ#1
- 0 = PCIEX6/0 Not Controlled
- 1 = PCIEX6/0 Controlled

PEREQ#2
- 0 = PCIEX8/1 Not Controlled
- 1 = PCIEX8/1 Controlled

PEREQ#3
- 0 = PCIEX4/2 Not Controlled
- 1 = PCIEX4/2 Controlled (D)

PEREQ#4
- 0 = PCIEX7/5/3 Not Controlled
- 1 = PCIEX7/5/3 Controlled (D)

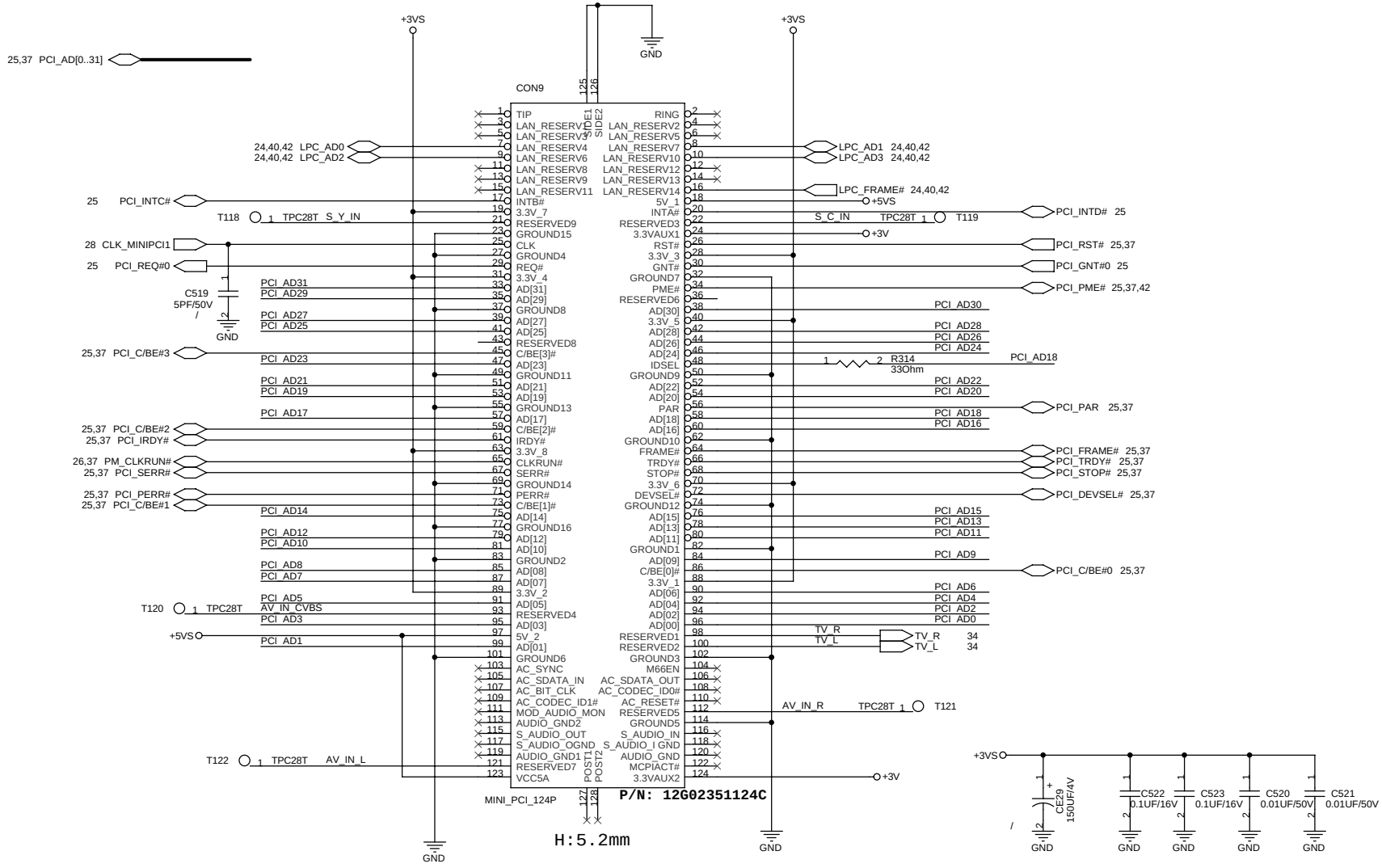
<Variant Name>

ASUSTeK COMPUTER INC. NB1 — Engineer: Mark , Frank

Title : CLOCK GEN-ICS954310

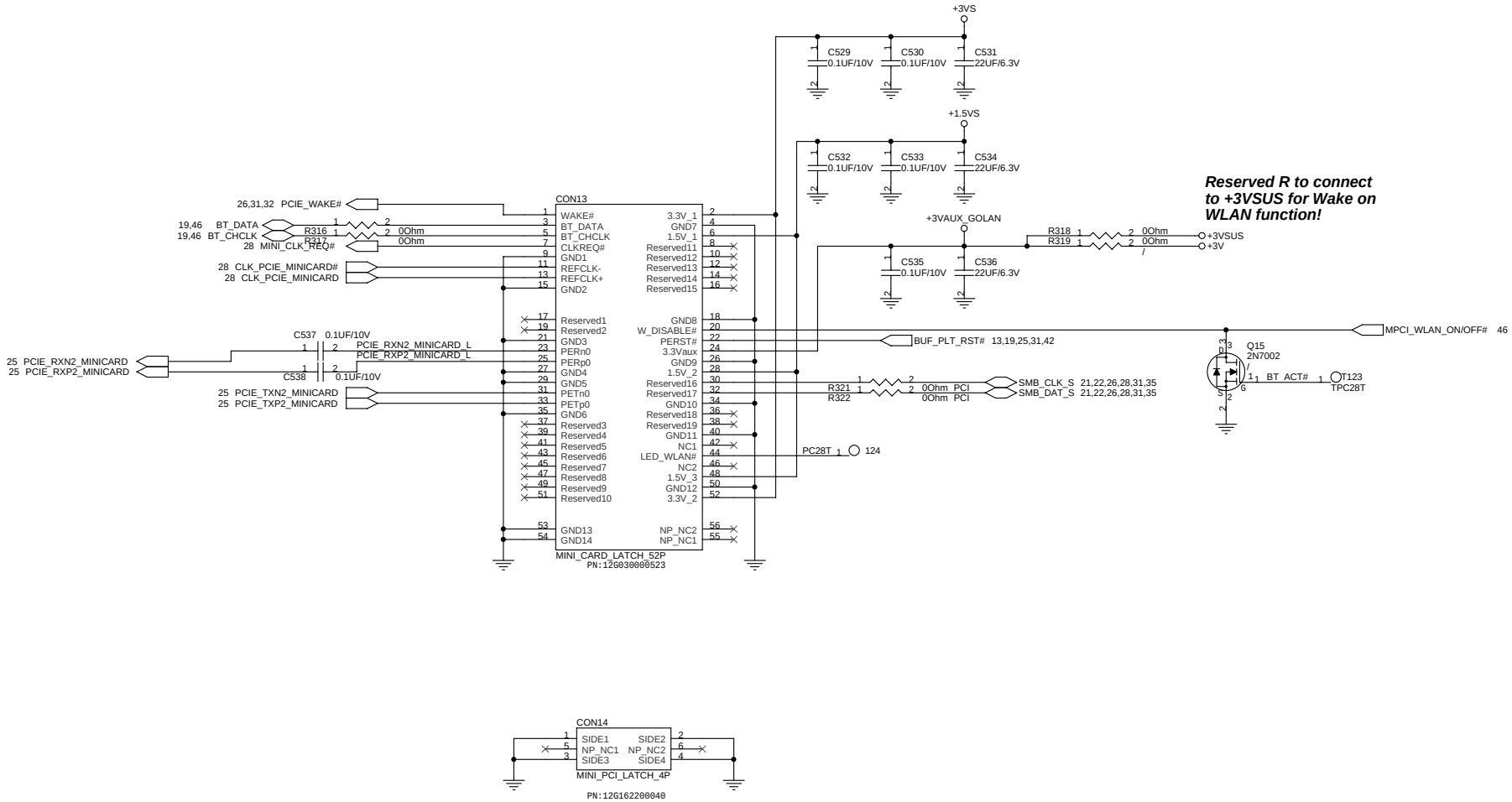
Size	Project Name	Rev
Custom	A7J	2.0

Date: Tuesday November 29 2005 — Sheet 28 of 52



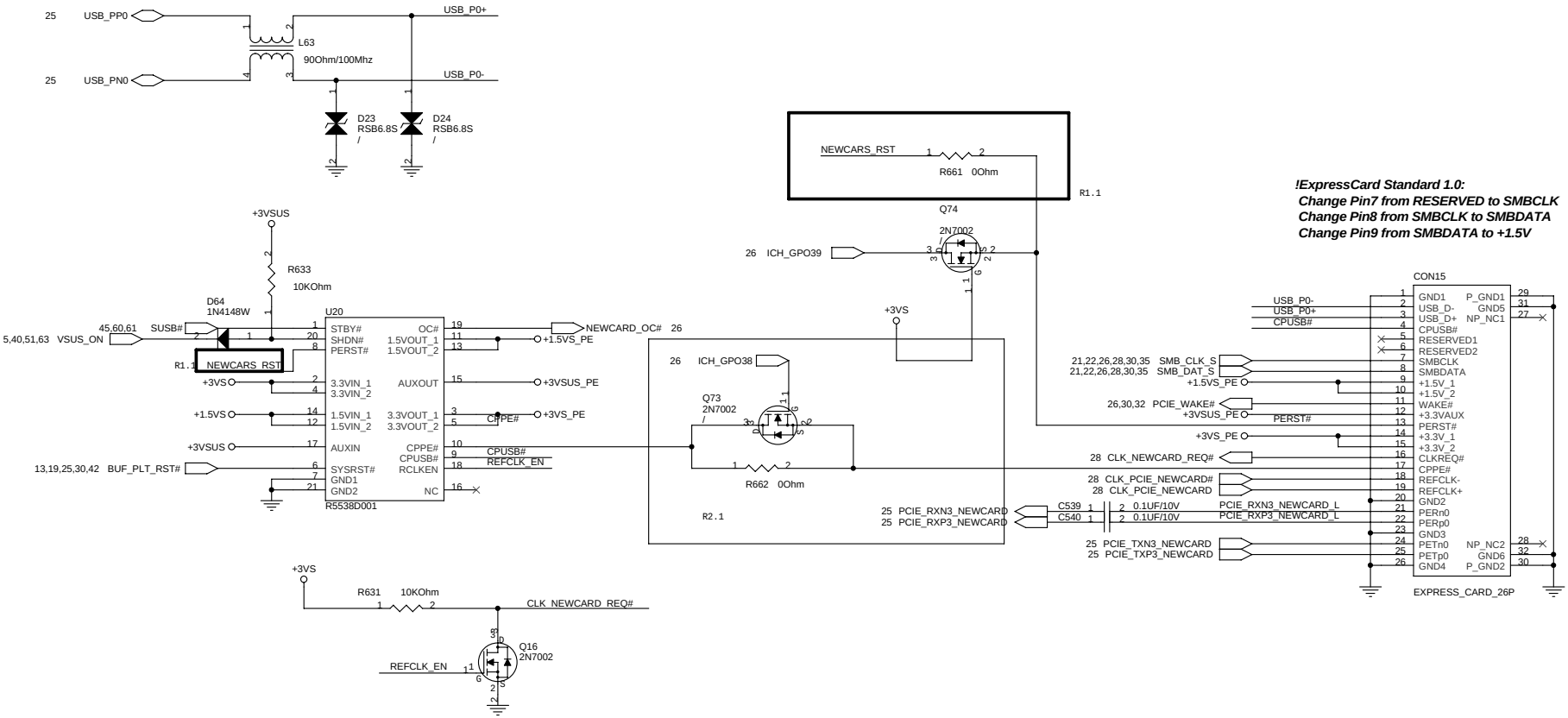
<Variant Name>

ASUSTeK COMPUTER INC	Title : MINIPCI-TV	
	Engineer: *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday, November 29, 2005	Sheet 29 of 52	

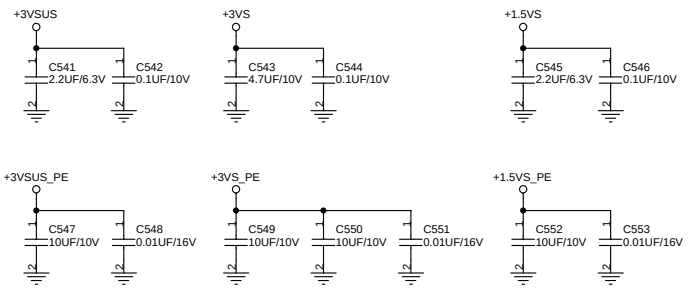


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : MINICARD	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 30 of 52	



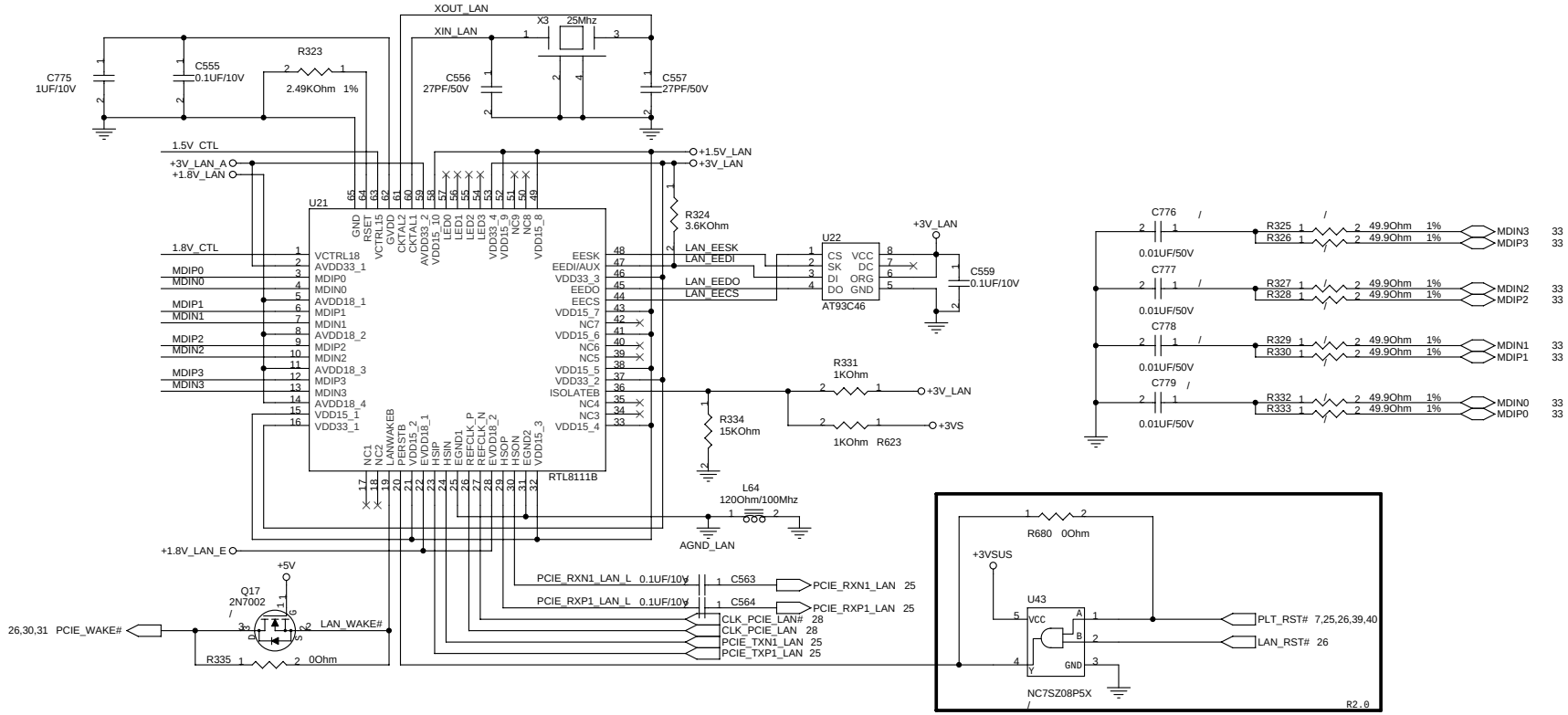
!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

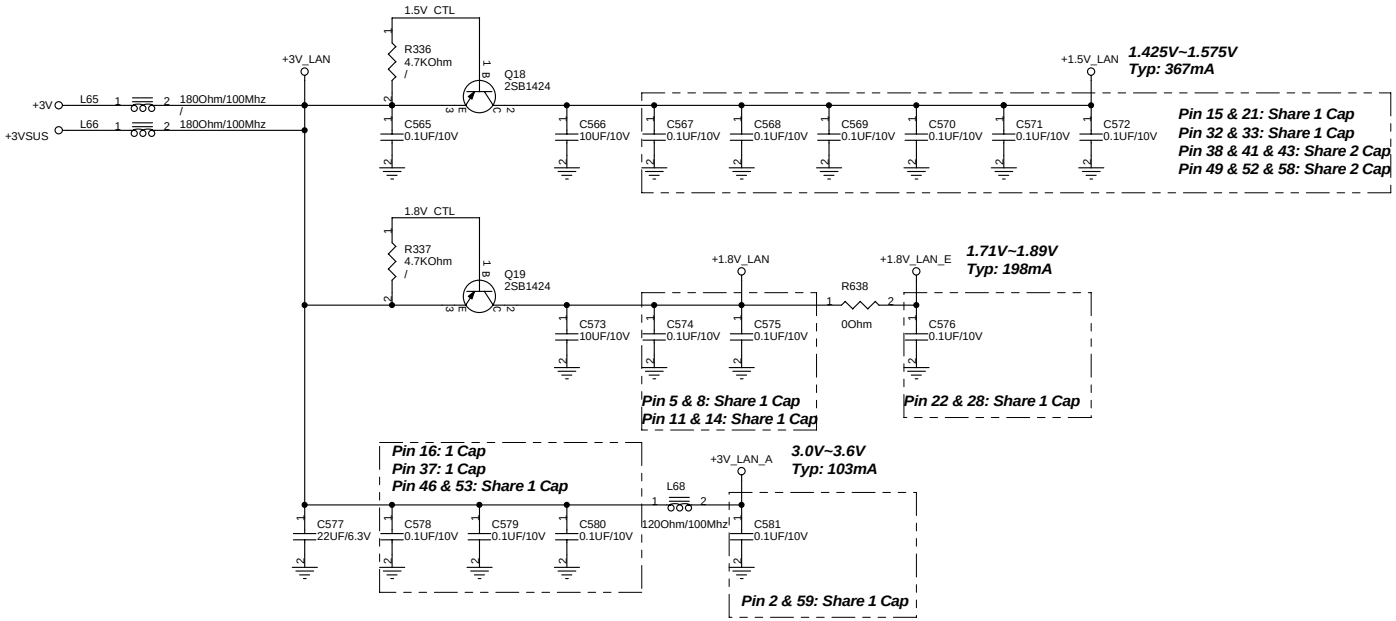


<Variant Name>

Title : NEWCARD

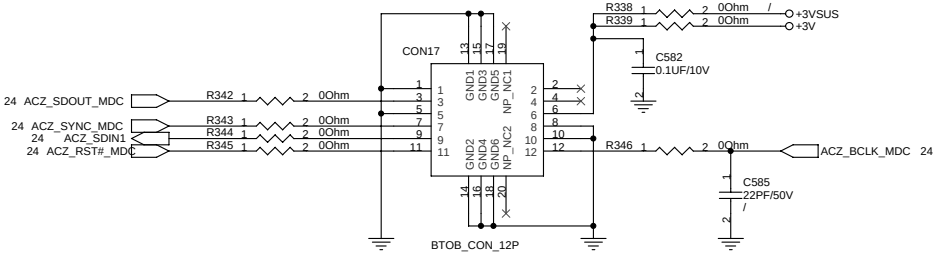
ASUSTeK COMPUTER INC. NB1	**Engineer**	***Mark , Frank***
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 31 of 52	



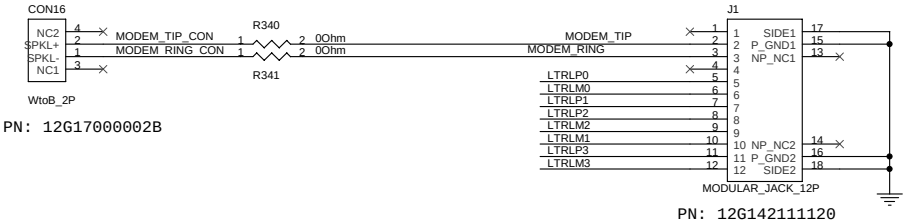


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : GIGALAN-RTL8111B	
	Engineer Mark,Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 32 of 52	

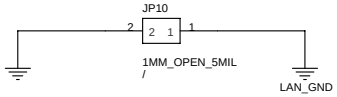


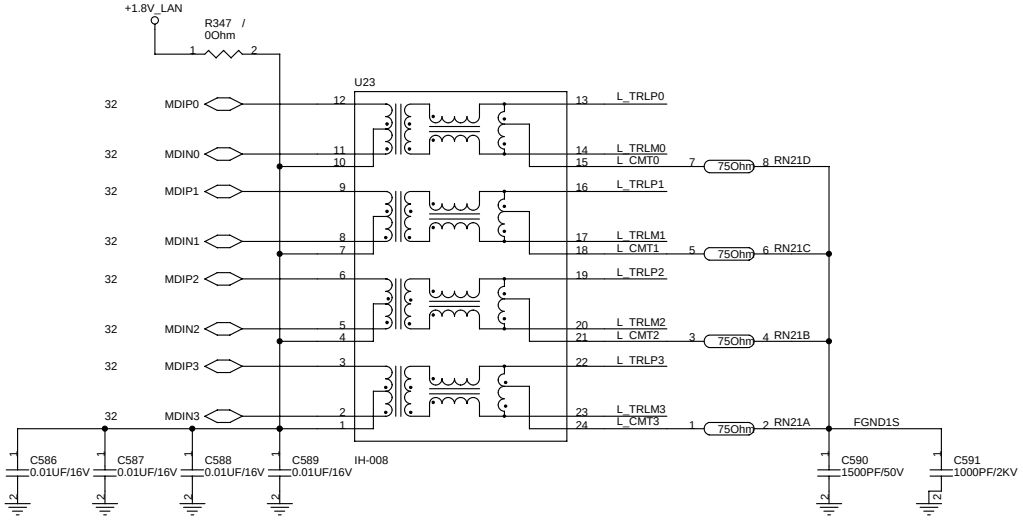
PN: 12G161200120

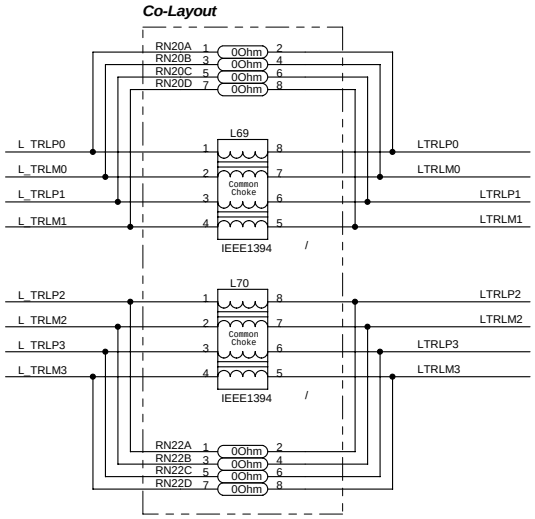


PN: 12G17000002B

PN: 12G142111120







J1.0

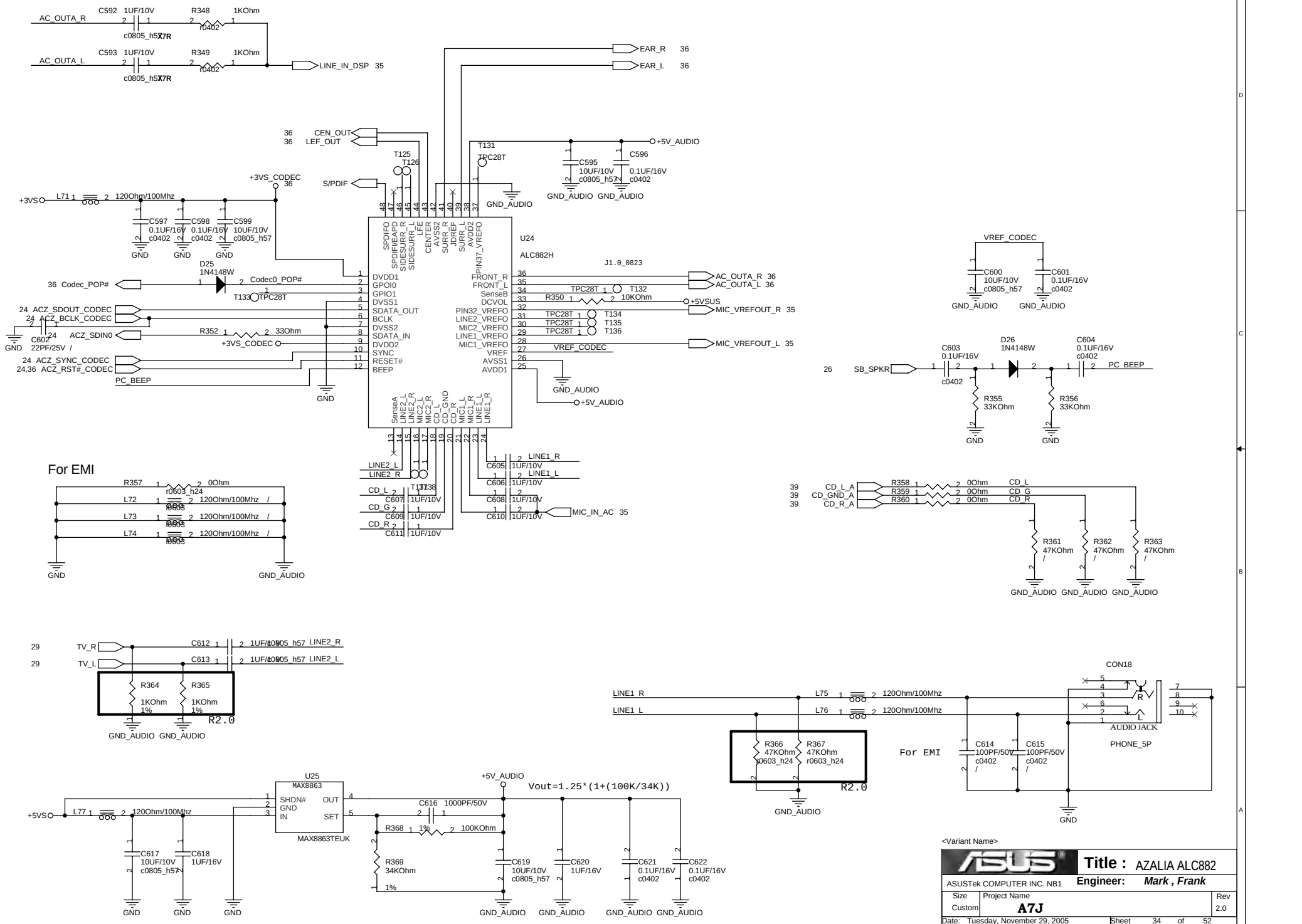
<Variant Name>

Title : RJ45&RJ11

ASUSTeK COMPUTER INC. NB1 Engineer *Mark,Frank*

Size	Project Name	Rev
Custom	**A7J**	2.0

Date Tuesday November 29 2005 Sheet 33 of 52



<Variant Name>

ASUSTek COMPUTER INC. NB1

Title : AZALIA ALC882

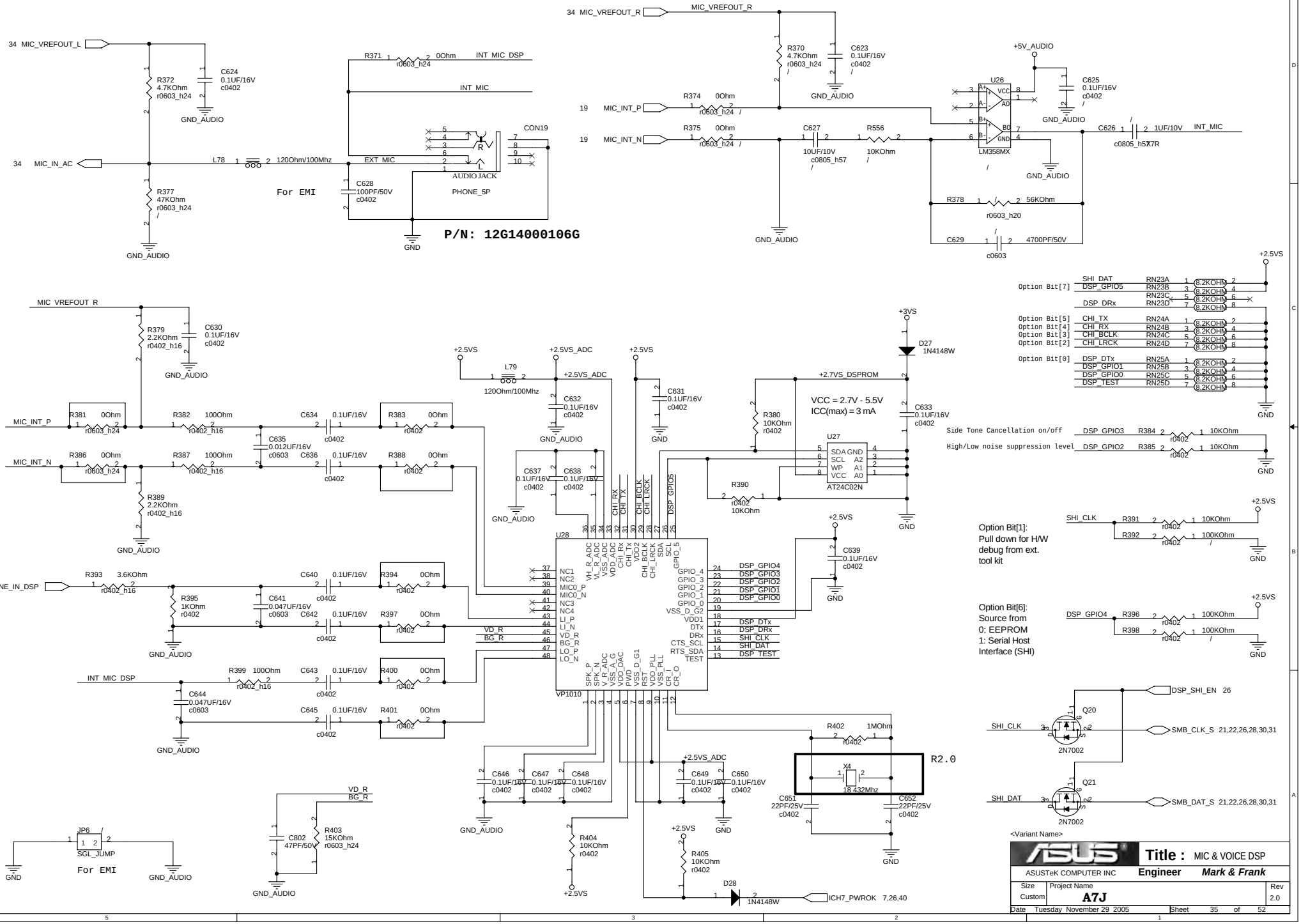
Engineer: *Mark , Frank*

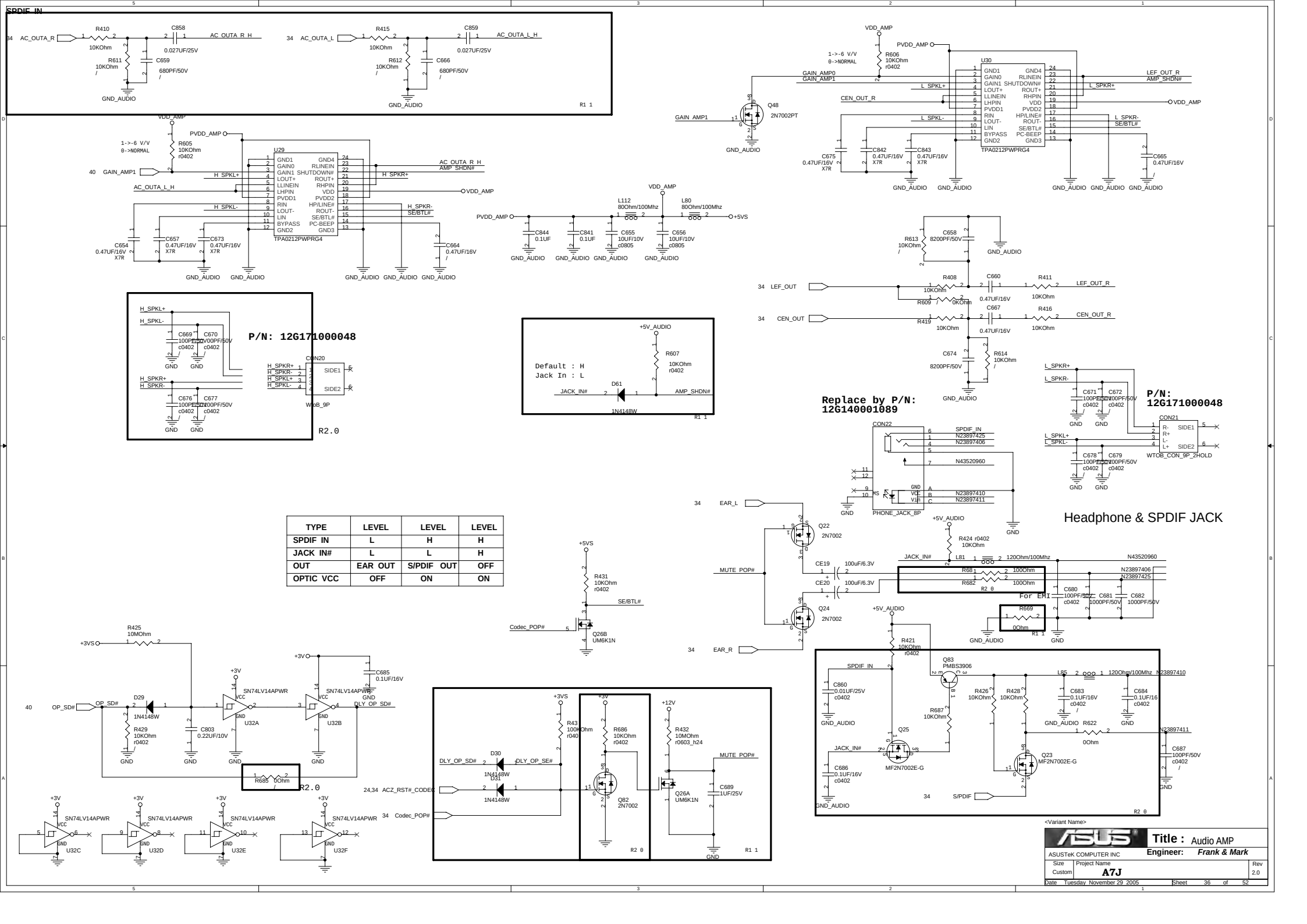
Size	Project Name	Rev
Custom	**A7J**	2.0

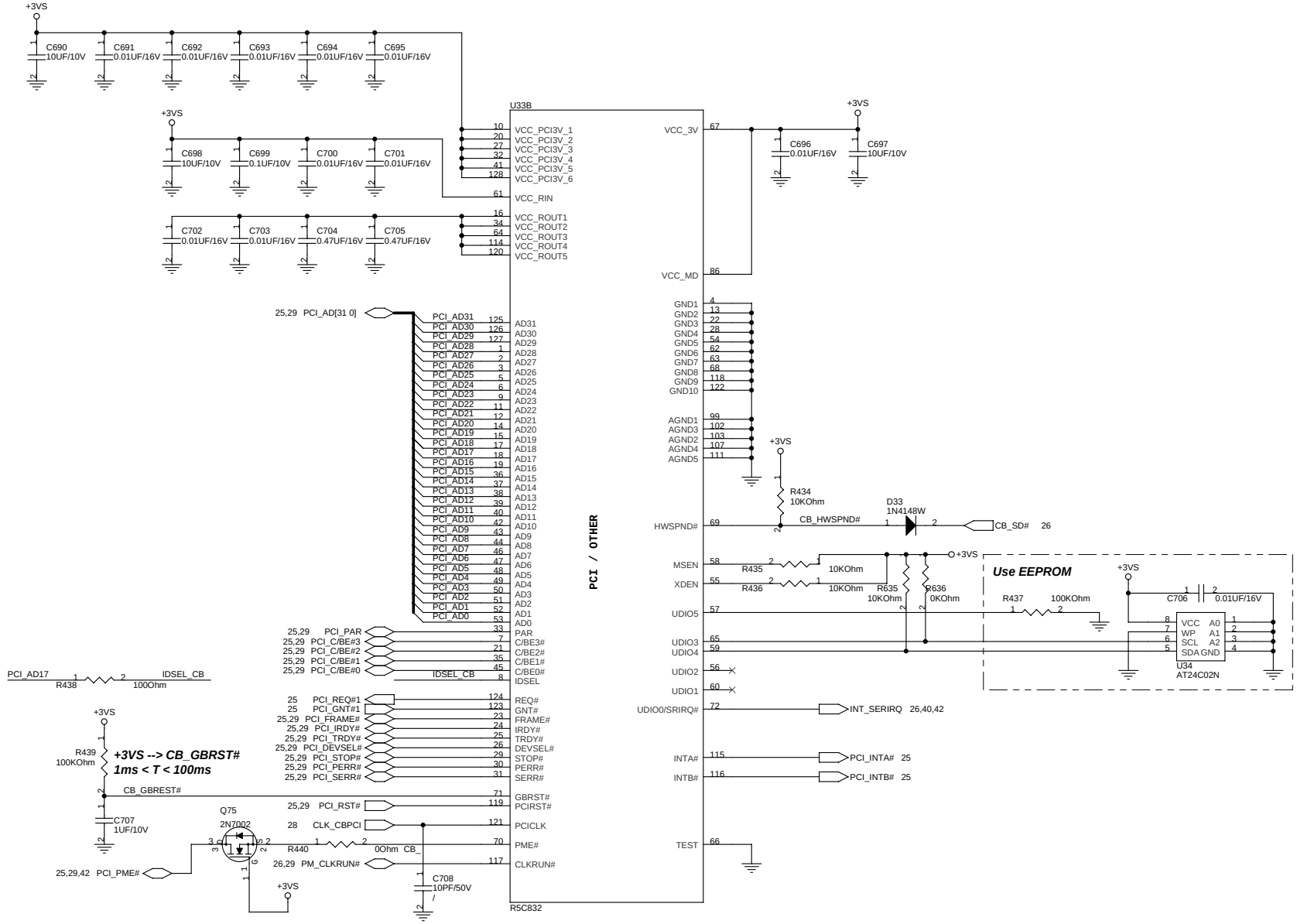
Date: Tuesday, November 29, 2005 Sheet 34 of 52

FL = TBD
FH = TBD

Internal MIC Pre-Amplifier




SPDIF_IN
AC_OUTA_R
R410
10KOhm
C858
0.027UF/25V
AC_OUTA_R_H
R611
10KOhm
C659
680PF/50V
GND_AUDIO
AC_OUTA_L
R415
10KOhm
C859
0.027UF/25V
AC_OUTA_L_H
R612
10KOhm
C666
680PF/50V
GND_AUDIO
R1 1
VDD_AMP
PVDD_AMP
1->6 V/V
0->NORMAL
R605
10KOhm
r0402
GAIN_AMP1
H_SPKL+
H_SPKL-
AC_OUTA_L_H
U29
GND1
GAIN0
GAIN1
LOUT+
LLINEIN
LHPIN
PVDD1
RIN
LOUT-
LIN
BYPASS
GND2
GND4
RLINEIN
SHUTDOWN#
ROUT+
RHPIN
VDD
PVDD2
HP/LINE#
ROUT-
SE/BTL#
PC-BEEP
GND3
TPA0212PWPRG4
AC_OUTA_R_H
AMP_SHDN#
H_SPKR+
H_SPKR-
SE/BTL#
VDD_AMP
C654
0.47UF/16V
X7R
C657
0.47UF/16V
X7R
C673
0.47UF/16V
X7R
C664
0.47UF/16V
GND_AUDIO
VDD_AMP
L112
80Ohm/100Mhz
L80
80Ohm/100Mhz
PVDD_AMP
+5VS
C844
0.1UF
C841
0.1UF
C655
10UF/10V
c0805
C656
10UF/10V
c0805
GND_AUDIO
VDD_AMP
1->6 V/V
0->NORMAL
R606
10KOhm
r0402
GAIN_AMP0
GAIN_AMP1
U30
GND1
GAIN0
GAIN1
LOUT+
LLINEIN
LHPIN
PVDD1
RIN
LOUT-
LIN
BYPASS
GND2
GND4
RLINEIN
SHUTDOWN#
ROUT+
RHPIN
VDD
PVDD2
HP/LINE#
ROUT-
SE/BTL#
PC-BEEP
GND3
TPA0212PWPRG4
L_SPKL+
L_SPKL-
LEF_OUT_R
AMP_SHDN#
L_SPKR+
L_SPKR-
SE/BTL#
VDD_AMP
CEN_OUT_R
GAIN_AMP1
Q48
2N7002PT
C675
0.47UF/16V
X7R
C842
0.47UF/16V
X7R
C843
0.47UF/16V
X7R
C665
0.47UF/16V
GND_AUDIO
R613
10KOhm
C658
8200PF/50V
R408
10KOhm
C660
0.47UF/16V
R411
10KOhm
LEF_OUT_R
LEF_OUT
R609
0KOhm
C667
0.47UF/16V
R416
10KOhm
CEN_OUT_R
CEN_OUT
R419
10KOhm
C674
8200PF/50V
R614
10KOhm
P/N: 12G171000048
H_SPKL+
H_SPKL-
H_SPKR+
H_SPKR-
C669
100PF/50V
c0402
C670
100PF/50V
c0402
C676
100PF/50V
c0402
C677
100PF/50V
c0402
CON20
SIDE1
SIDE2
WtoB_9P
R2.0
Default : H
Jack In : L
+5V_AUDIO
R607
10KOhm
r0402
JACK_IN#
D61
1N4148W
AMP_SHDN#
R1 1
Replace by P/N: 12G140001089
CON22
SPDIF_IN
N23897425
N23897406
N43520960
N23897410
N23897411
PHONE_JACK_8P
L_SPKR+
L_SPKR-
C671
100PF/50V
c0402
C672
100PF/50V
c0402
P/N: 12G171000048
CON21
SIDE1
SIDE2
L_SPKL+
L_SPKL-
C678
100PF/50V
c0402
C679
100PF/50V
c0402
WTOB_CON_9P_2HOLD
Headphone & SPDIF JACK
EAR_L
EAR_R
Q22
2N7002
Q24
2N7002
+5V_AUDIO
R424 r0402
10KOhm
MUTE_POP#
CE19
100uF/6.3V
CE20
100uF/6.3V
JACK_IN#
L81
120Ohm/100Mhz
R681
100Ohm
R682
100Ohm
R2 0
For EMI
C680
100PF/50V
c0402
C681
1000PF/50V
C682
1000PF/50V
R669
0Ohm
R1 1
R421
10KOhm
r0402
SPDIF_IN
Q83
PMBS3906
L85
120Ohm/100Mhz
N23897410
C860
0.01UF/25V
c0402
R426
10KOhm
R428
10KOhm
C683
0.1UF/16V
c0402
C684
0.1UF/16
c0402
R687
10KOhm
Q25
MF2N7002E-G
R622
0Ohm
N23897411
JACK_IN#
C686
0.1UF/16V
c0402
Q23
MF2N7002E-G
C687
100PF/50V
c0402
S/PDIF
R2 0
GND_AUDIO
+5VS
R431
10KOhm
r0402
SE/BTL#
Codec_POP#
Q26B
UM6K1N
R425
10OHm
+3VS
D29
1N4148W
R429
10KOhm
r0402
C803
0.22UF/10V
SN74LV14APWR
U32A
U32B
C685
0.1UF/16V
OP_SD#
DLY_OP_SD#
R685
0Ohm
R2.0
U32C
U32D
U32E
U32F
+3VS
R43
100KOhm
r040
D30
D31
1N4148W
DLY_OP_SD#
DLY_OP_SE#
R686
10KOhm
r0402
Q82
2N7002
+12V
R432
10MOhm
r0603_h24
Q26A
UM6K1N
C689
1UF/25V
MUTE_POP#
24,34 ACZ_RST#_CODEC
34 Codec_POP#
R2 0
R1 1
TYPE | LEVEL | LEVEL | LEVEL
SPDIF IN | L | H | H
JACK IN# | L | L | H
OUT | EAR OUT | S/PDIF OUT | OFF
OPTIC VCC | OFF | ON | ON
<Variant Name>
ASUSTeK COMPUTER INC
Title : Audio AMP
Engineer: Frank & Mark
Size: Custom
Project Name: A7J
Rev: 2.0
Date: Tuesday November 29 2005
Sheet 36 of 52



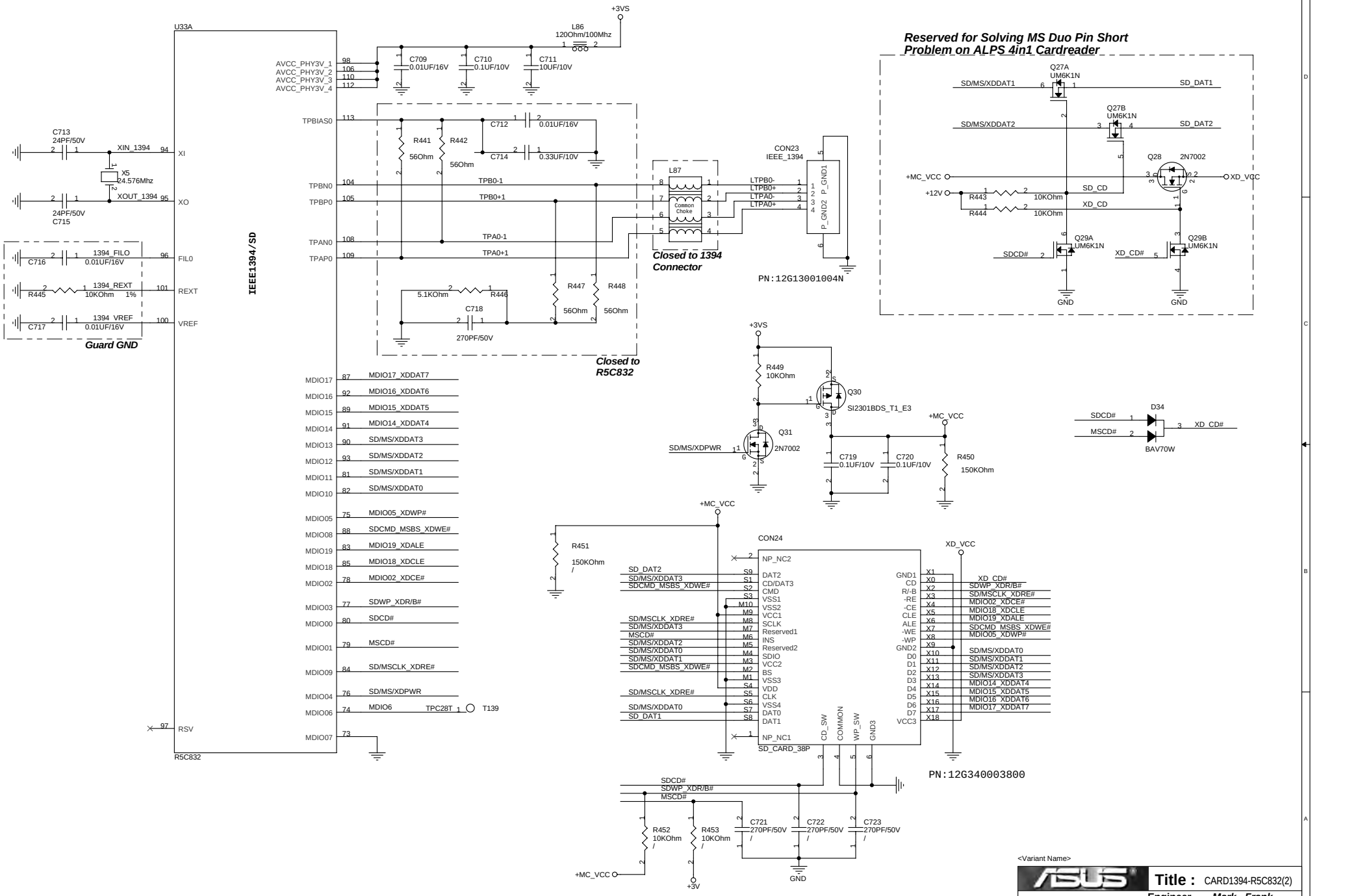
<Variant Name>

Title : CARD1394-R5C832(1)

ASUSTeK COMPUTER INC. NB1 **Engineer** ***Mark , Frank***

Size	Project Name	Rev
Custom	**A7J**	2.0

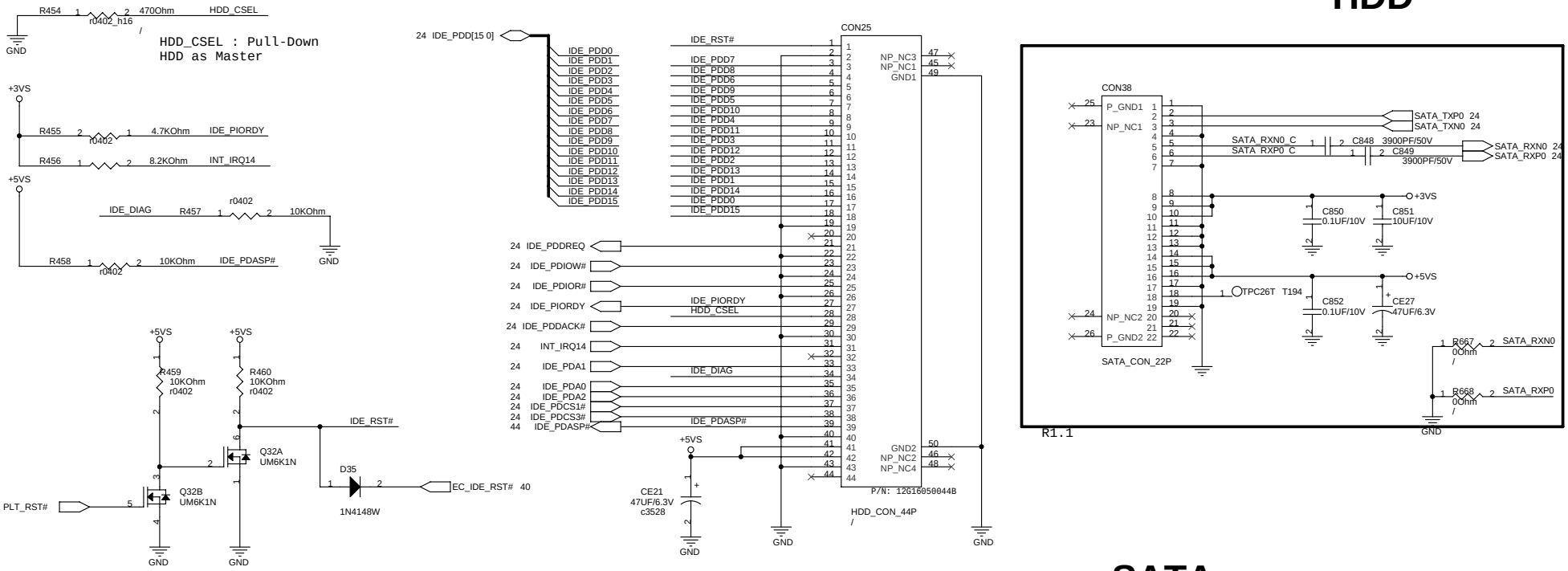
Date Tuesday November 29 2005 Sheet 37 of 52



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 38 of 52	

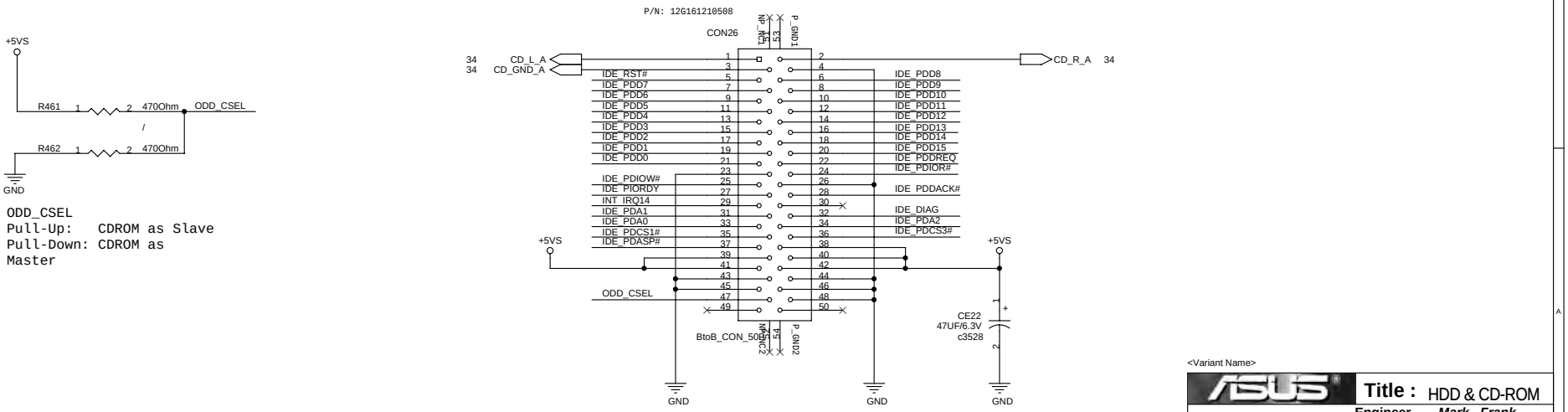
HDD



PATA

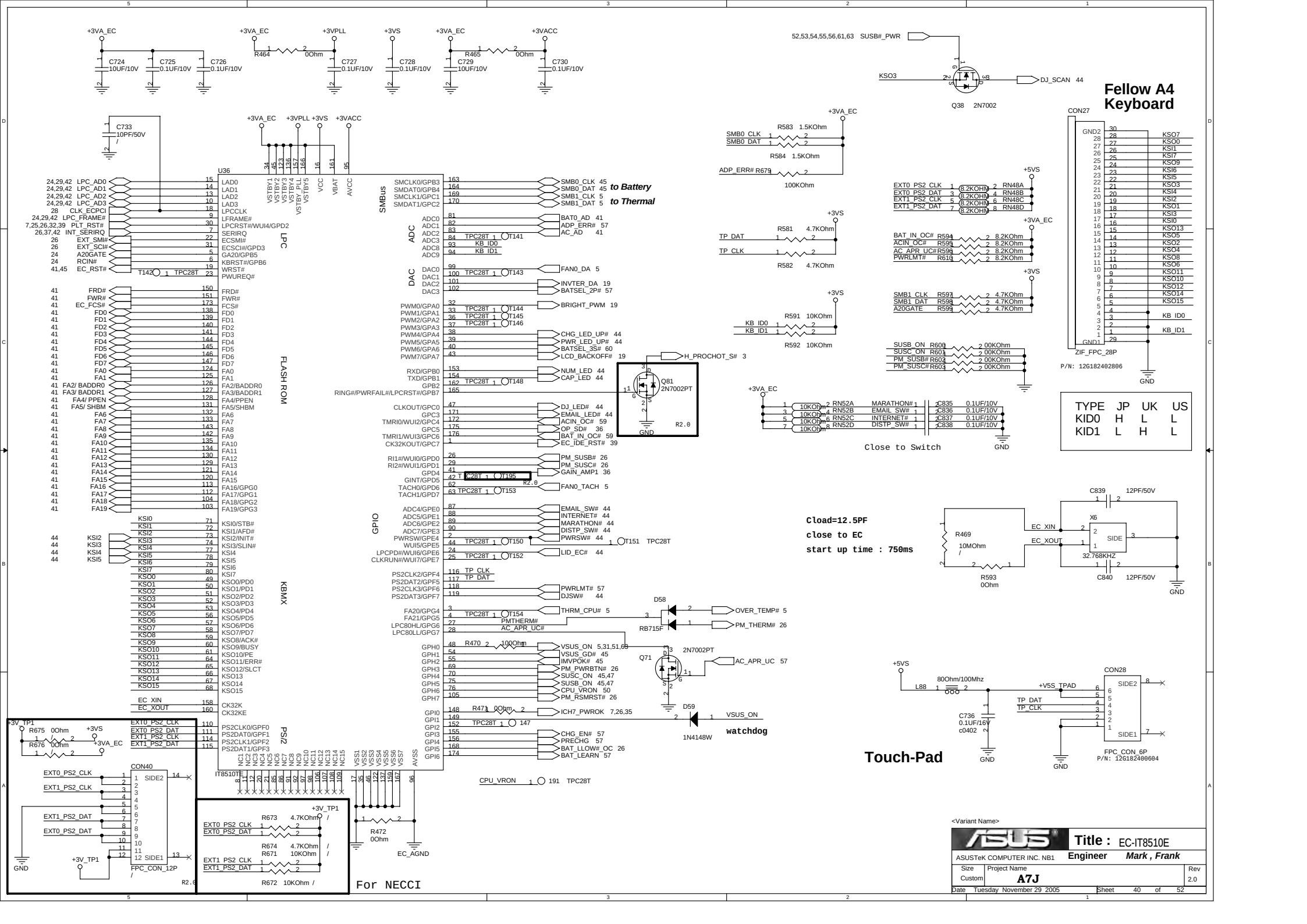
SATA

CD-ROM



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 39 of 52	


Fellow A4 Keyboard
Touch-Pad
U36
IT8510TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
Cload=12.5PF
close to EC
start up time : 750ms
Close to Switch
watchdog
For NECCI
ZIF_FPC_28P
P/N: 12G182402806
FPC_CON_6P
P/N: 12G182400604
FPC_CON_12P
TYPE JP UK US
KID0 H L L
KID1 L H L
Title : EC-IT8510E
ASUSTeK COMPUTER INC. NB1
Engineer Mark , Frank
A7J
Tuesday November 29 2005
Sheet 40 of 52

EC Hardware Strapping

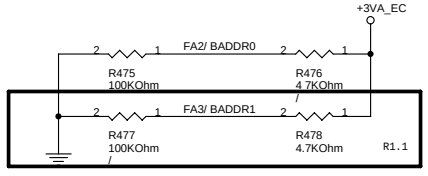
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

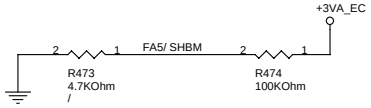


Note: Sampled at VSTBY Power Up Reset

FA5/ SHBM

0: Disable Shared Memory with Host BIOS

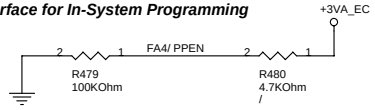
1: Enable Shared Memory with Host BIOS

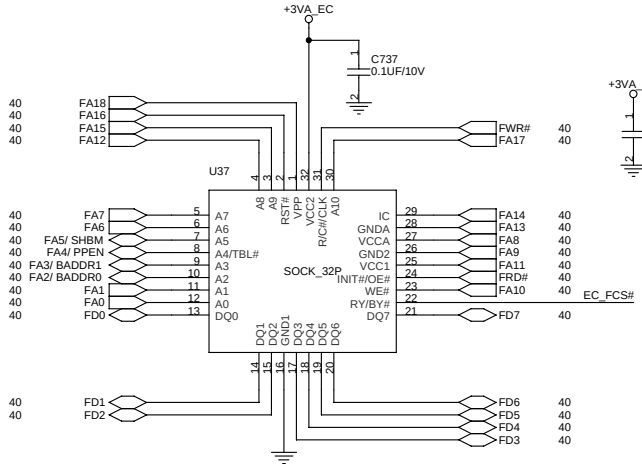


FA4/ PPEN

0: Normal

1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming

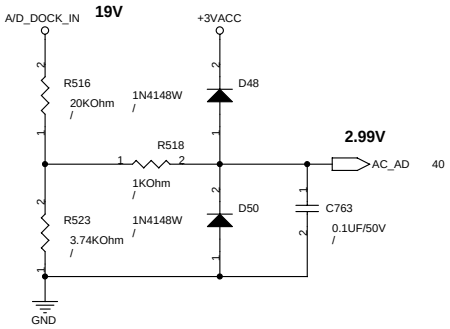




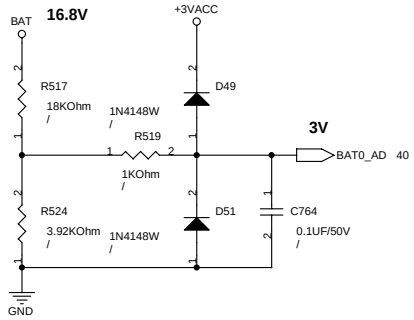
EC ADC

close to EC

Adaptor

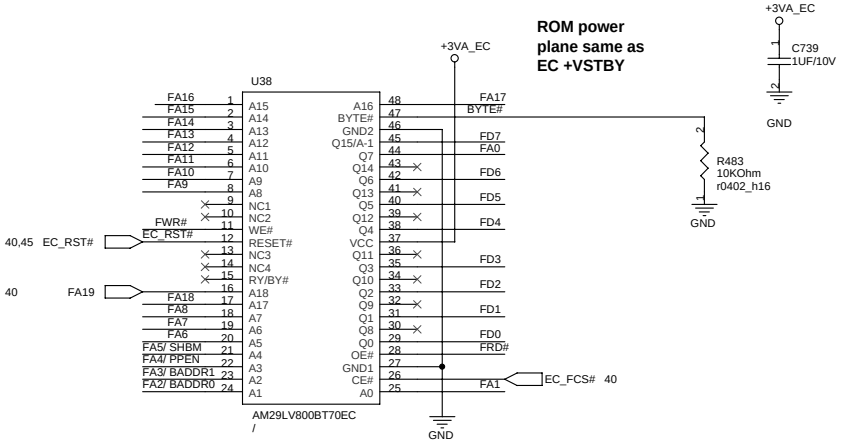


Battery 0



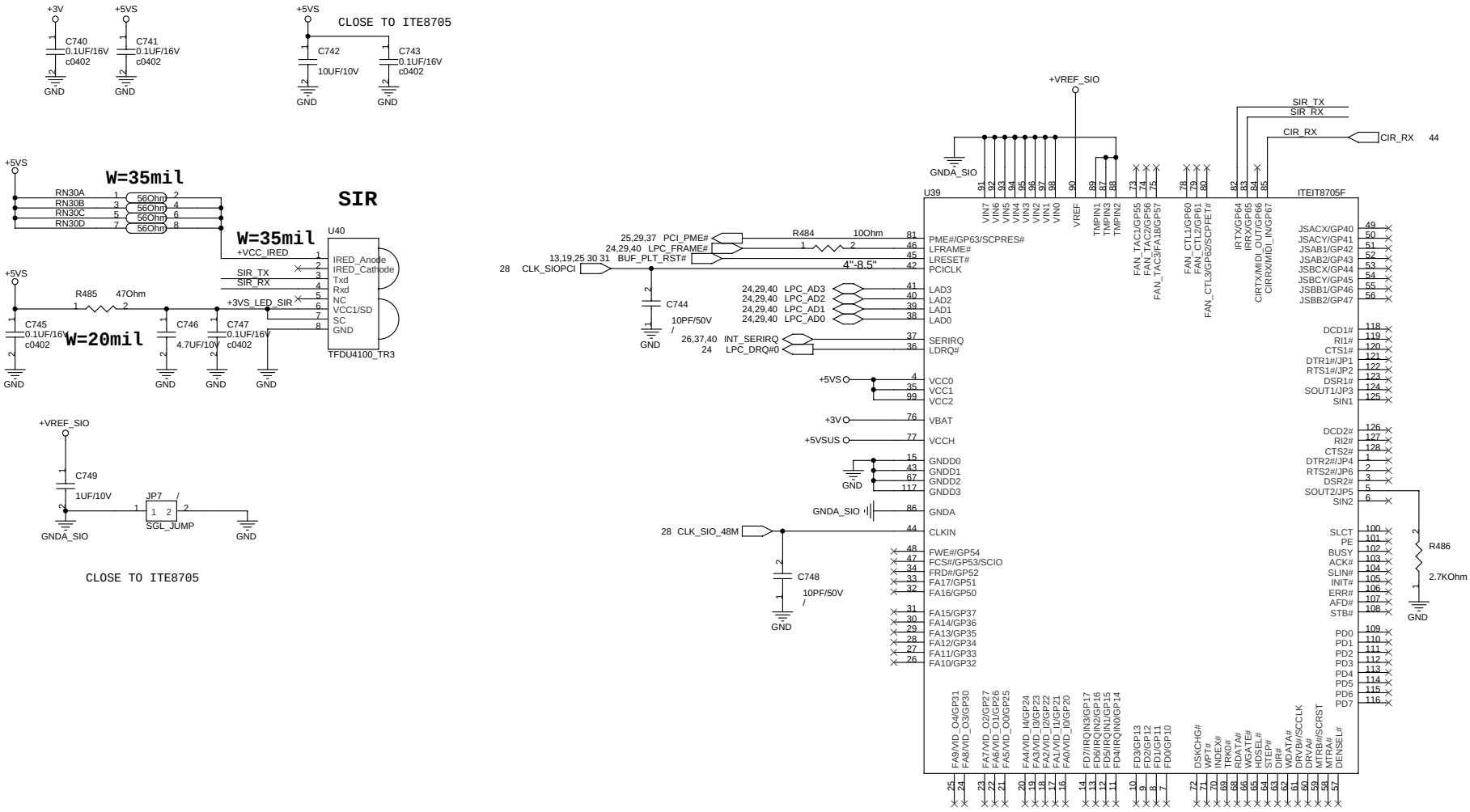
R1.1

ROM power plane same as EC +VSTBY



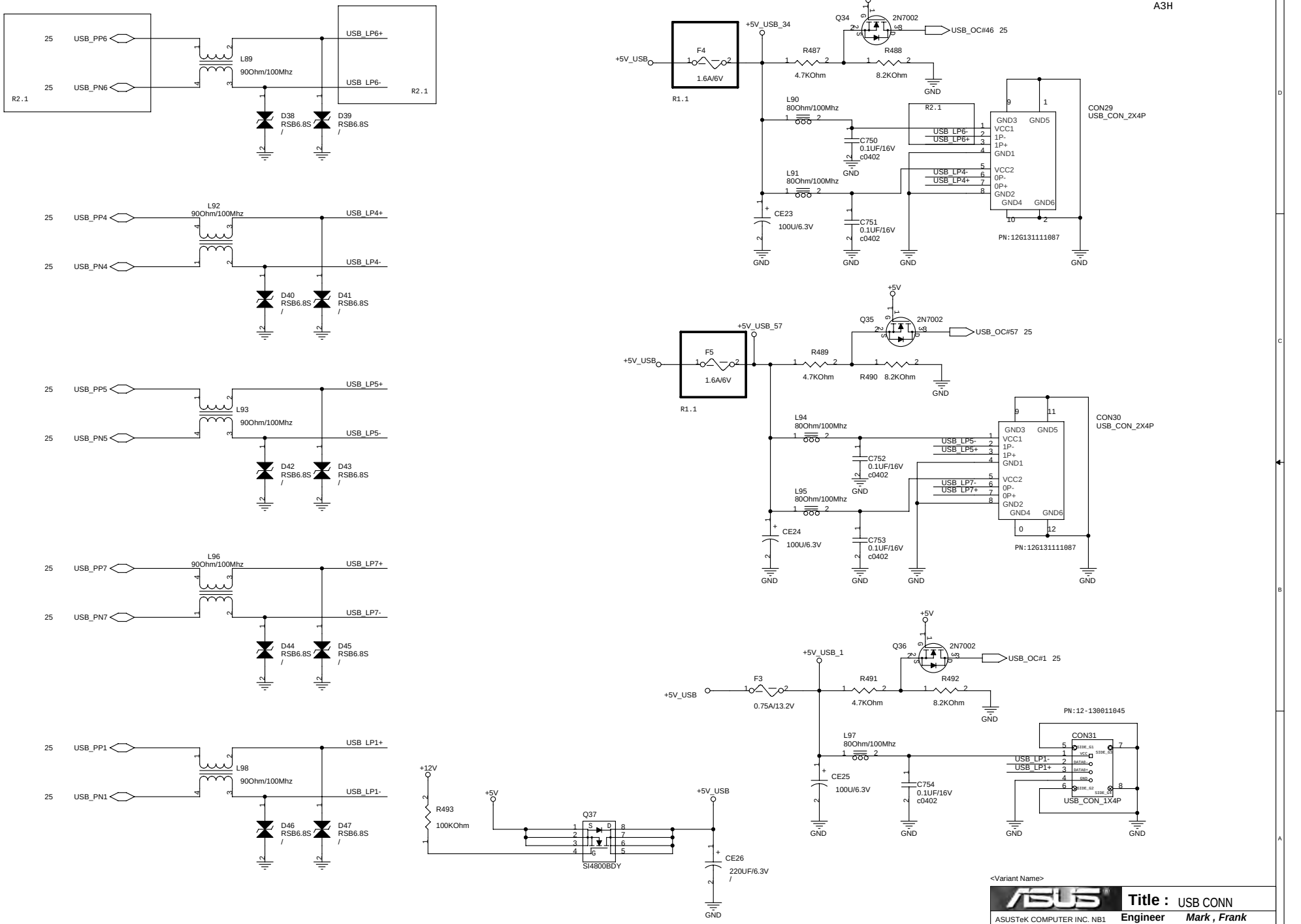
<Variant Name>

ASUSTeK COMPUTER INC. NB1	**Title :** ISA ROM	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 41 of 52	

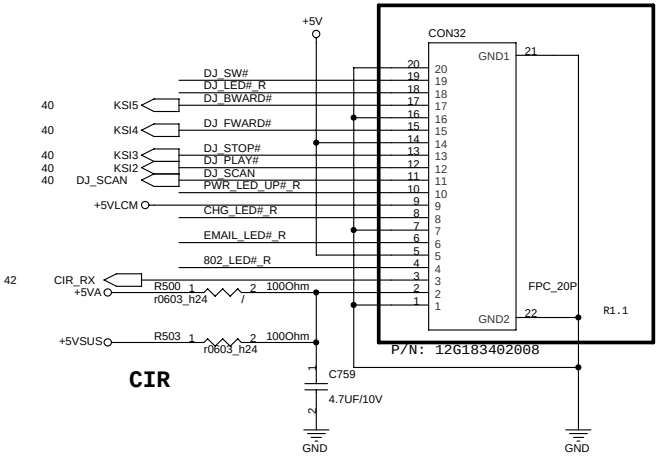


<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : SUPER I/O	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 42 of 52	

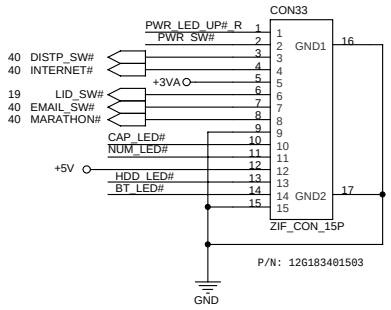

Refer to
A3H
25 USB_PP6
25 USB_PN6
R2.1
L89
90Ohm/100Mhz
USB_LP6+
USB_LP6-
R2.1
D38 RSB6.8S /
D39 RSB6.8S /
L92
90Ohm/100Mhz
25 USB_PP4
25 USB_PN4
USB_LP4+
USB_LP4-
D40 RSB6.8S /
D41 RSB6.8S /
L93
90Ohm/100Mhz
25 USB_PP5
25 USB_PN5
USB_LP5+
USB_LP5-
D42 RSB6.8S /
D43 RSB6.8S /
L96
90Ohm/100Mhz
25 USB_PP7
25 USB_PN7
USB_LP7+
USB_LP7-
D44 RSB6.8S /
D45 RSB6.8S /
L98
90Ohm/100Mhz
25 USB_PP1
25 USB_PN1
USB_LP1+
USB_LP1-
D46 RSB6.8S /
D47 RSB6.8S /
+5V
Q34 2N7002
USB_OC#46 25
+5V_USB_34
+5V_USB
F4
1.6A/6V
R1.1
R487 4.7KOhm
R488 8.2KOhm
GND
L90
80Ohm/100Mhz
L91
80Ohm/100Mhz
C750 0.1UF/16V c0402
C751 0.1UF/16V c0402
CE23 100U/6.3V
R2.1
USB_LP6-
USB_LP6+
USB_LP4-
USB_LP4+
CON29
USB_CON_2X4P
GND3 GND5
VCC1
1P-
1P+
GND1
VCC2
0P-
0P+
GND2
GND4 GND6
PN:12G131111087
+5V
Q35 2N7002
USB_OC#57 25
+5V_USB_57
+5V_USB
F5
1.6A/6V
R1.1
R489 4.7KOhm
R490 8.2KOhm
GND
L94
80Ohm/100Mhz
L95
80Ohm/100Mhz
C752 0.1UF/16V c0402
C753 0.1UF/16V c0402
CE24 100U/6.3V
USB_LP5-
USB_LP5+
USB_LP7-
USB_LP7+
CON30
USB_CON_2X4P
PN:12G131111087
+5V
Q36 2N7002
USB_OC#1 25
+5V_USB_1
+5V_USB
F3
0.75A/13.2V
R491 4.7KOhm
R492 8.2KOhm
GND
L97
80Ohm/100Mhz
C754 0.1UF/16V c0402
CE25 100U/6.3V
USB_LP1-
USB_LP1+
CON31
USB_CON_1X4P
PN:12-130011045
+12V
R493 100KOhm
+5V
Q37
SI4800BDY
+5V_USB
CE26 220UF/6.3V
GND
<Variant Name>
Title : USB CONN
ASUSTeK COMPUTER INC. NB1
Engineer Mark , Frank
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday November 29 2005
Sheet 43 of 52

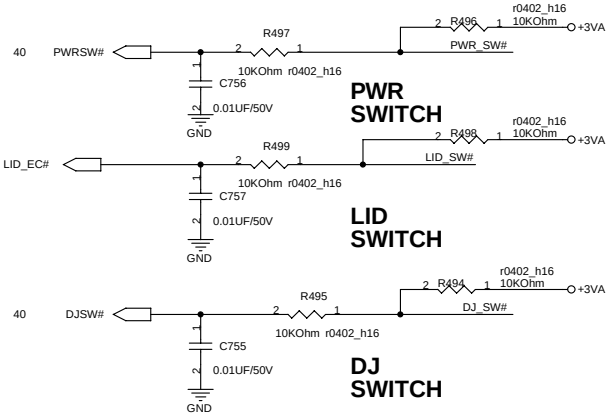
DJ Board Conn.

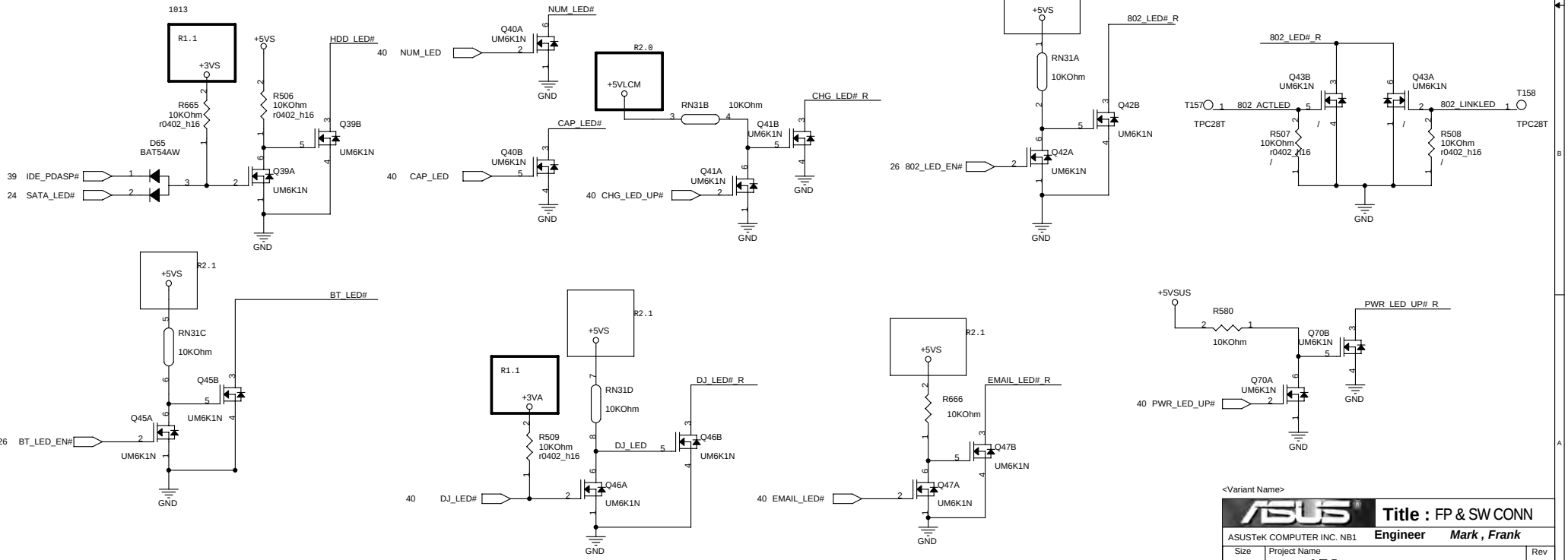


CIR

Launch Board Conn.



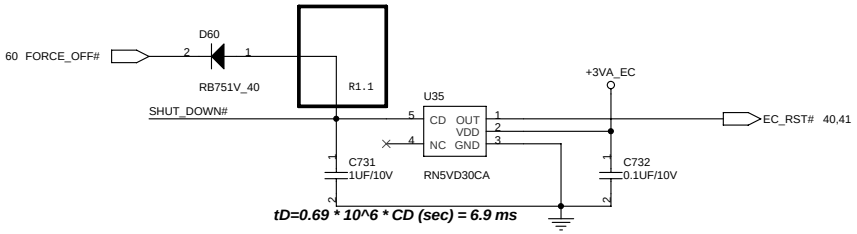


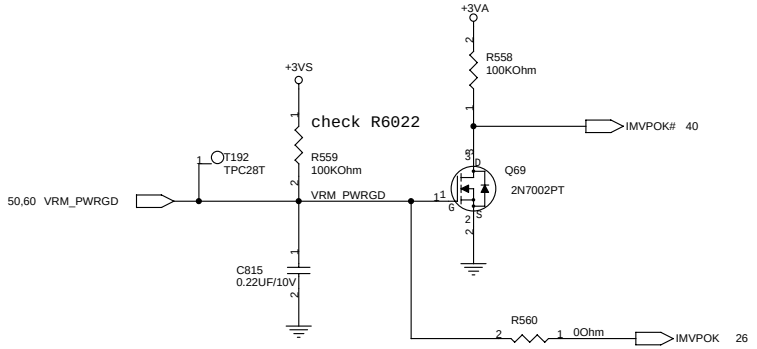


<Variant Name>

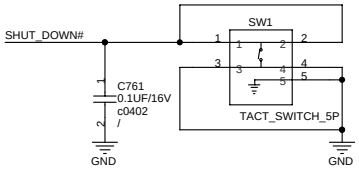
Title : FP & SW CONN

ASUSTeK COMPUTER INC. NB1	Engineer	*Mark , Frank*	
Size: Custom	Project Name: **A7J**		Rev: 2.0
Date: Tuesday November 29 2005	Sheet 44 of 52		

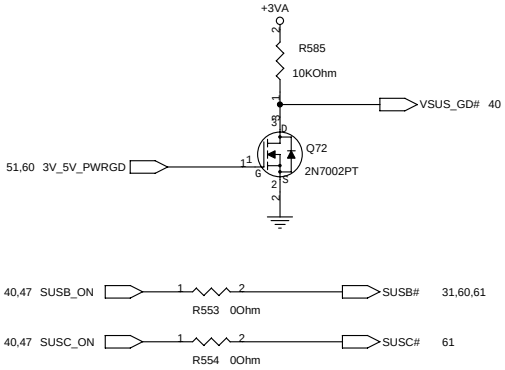


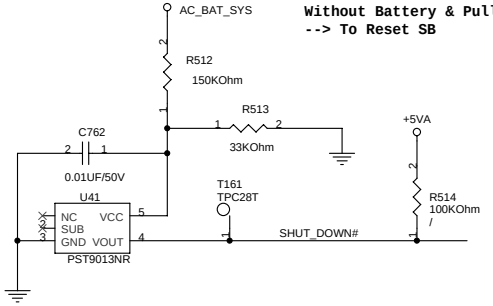


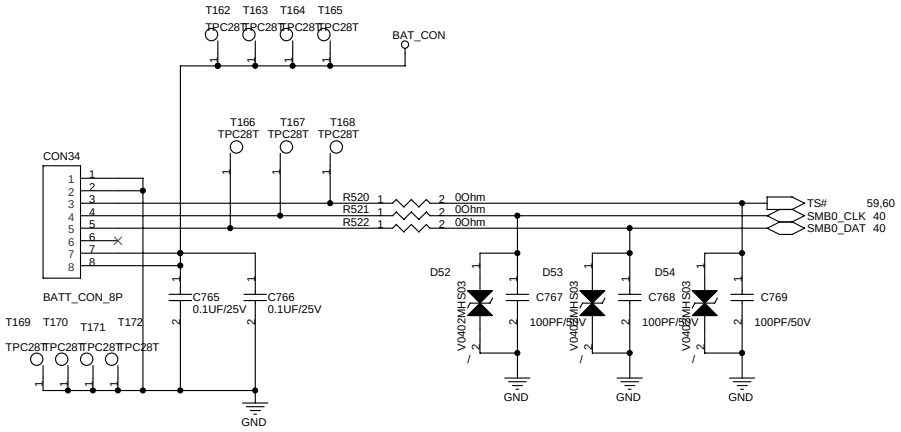
RESET SW.



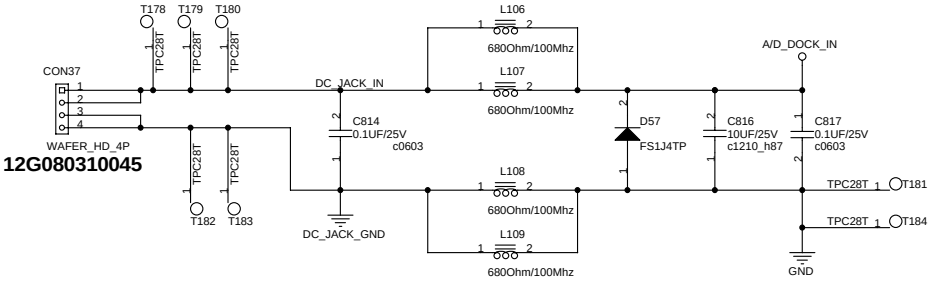
P/N: 12G091030050







Battery_IN Conn.

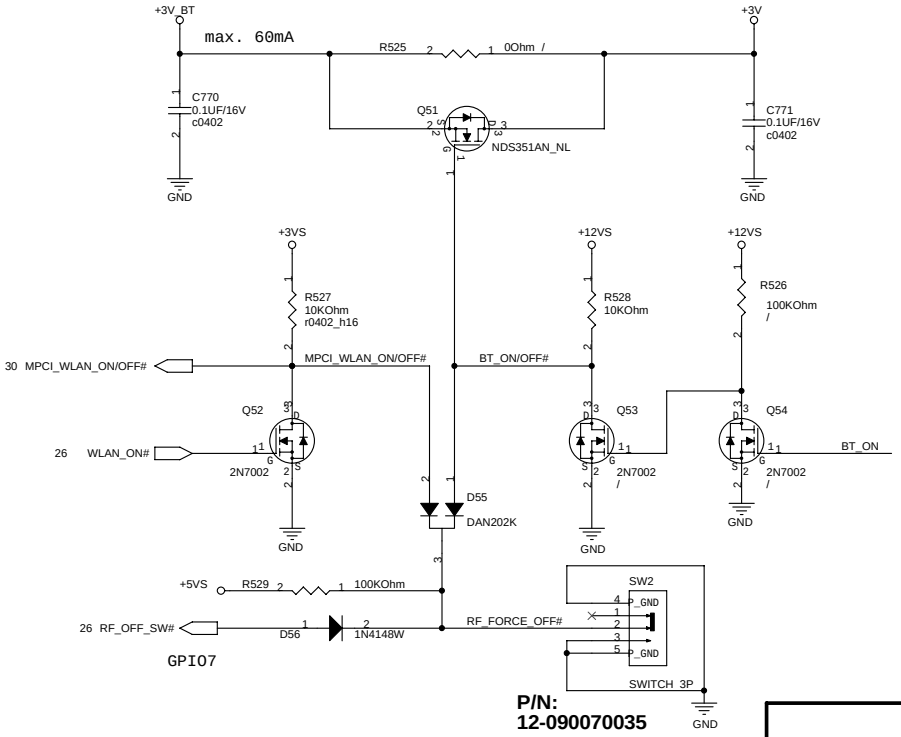


DC_IN Conn.

<Variant Name>

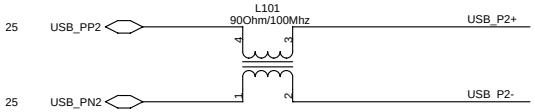
ASUSTeK COMPUTER INC. NB1	Title : BATTERY	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 45 of 52	

WLAN/BT ON/OFF Control

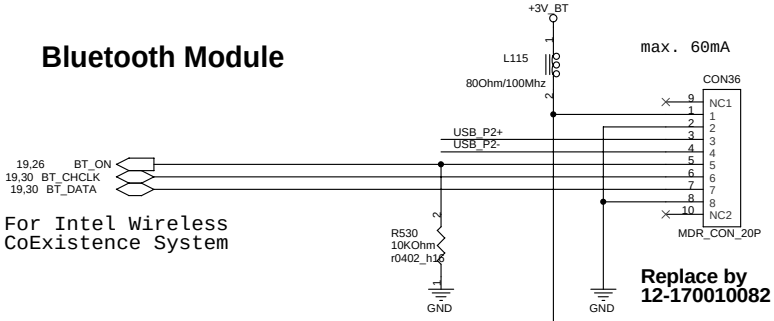


P/N:
12-090070035

For Bluetooth

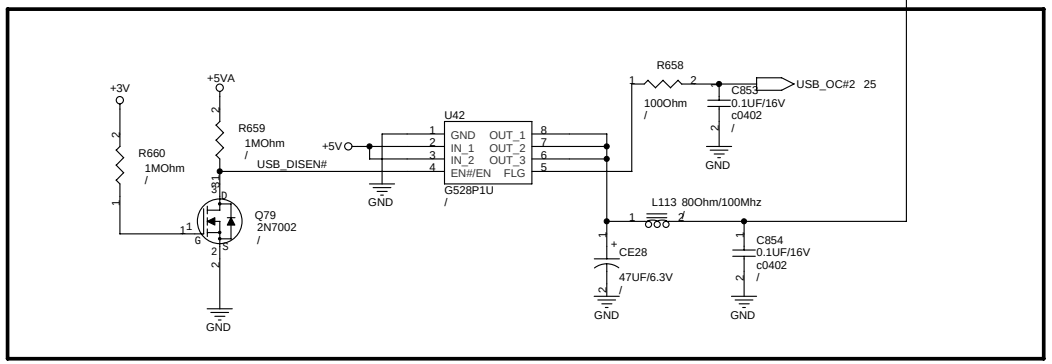


Bluetooth Module



For Intel Wireless CoExistence System

Replace by
12-170010082

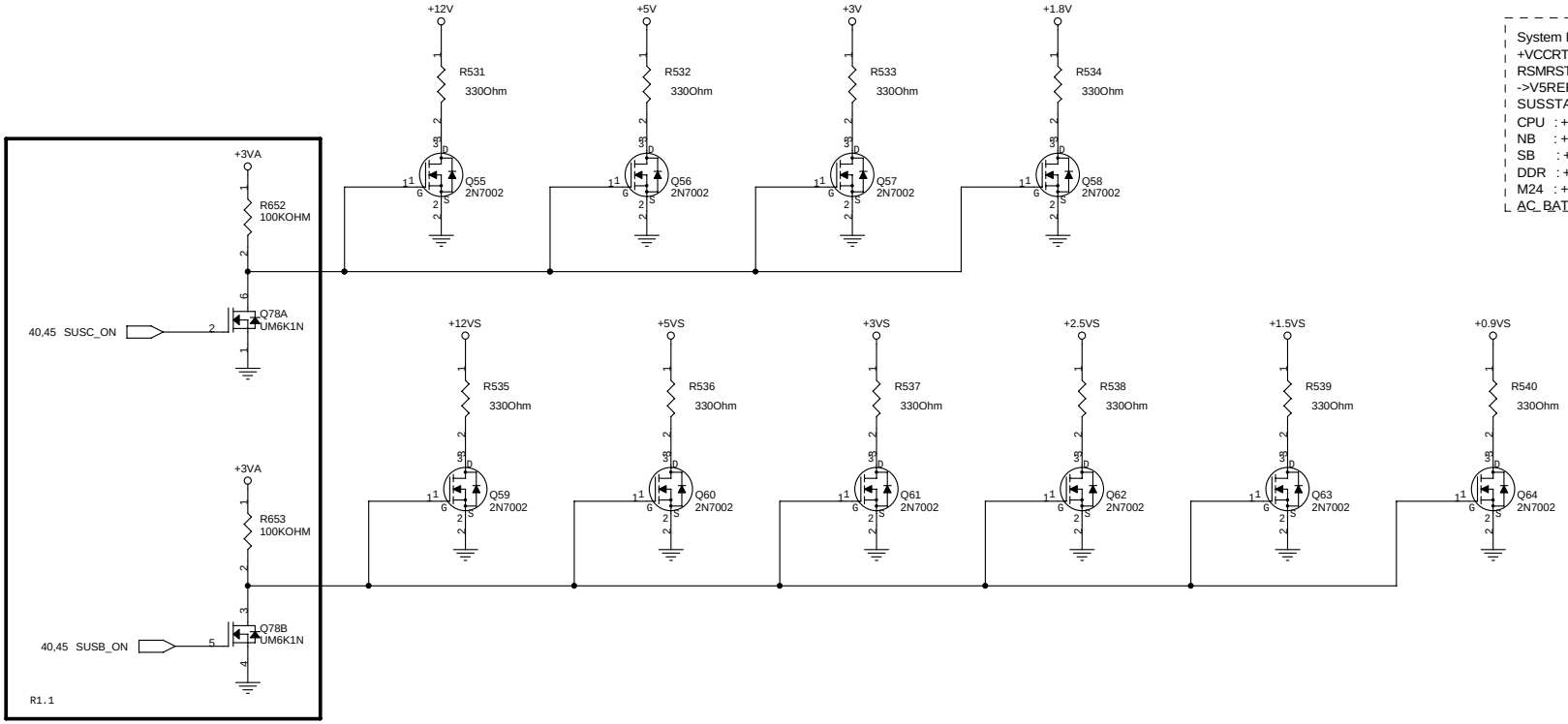


R1.1

For NECCI

<Variant Name>

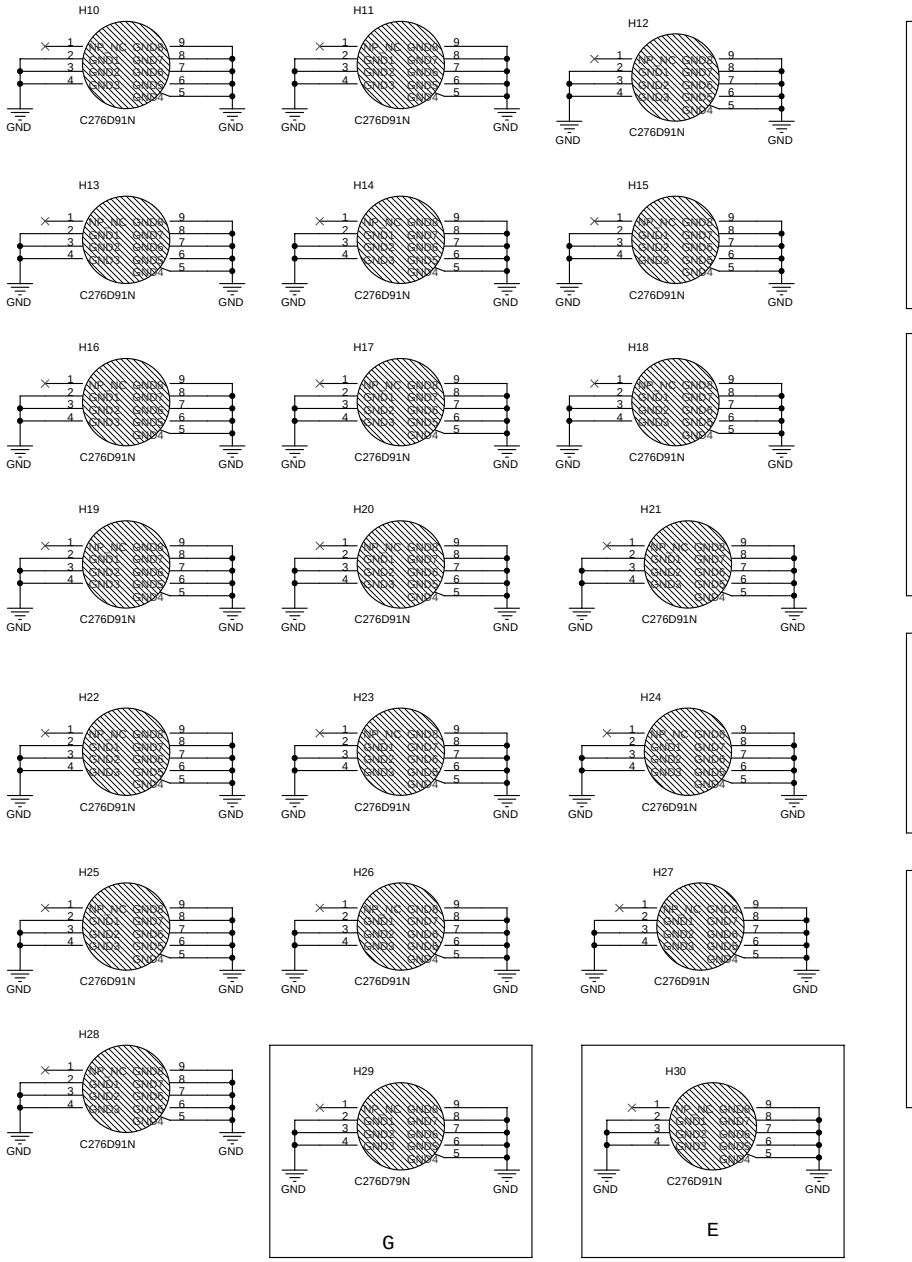
ASUSTeK COMPUTER INC. NB1	**Title :** BlueTooth	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 46 of 52	

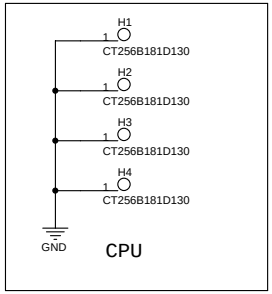


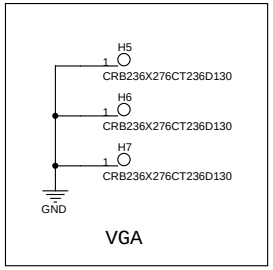
System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#
CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.5VS, +2.5V, +VCCP
SB : +1.5VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS
M24 : +3.3VS, +2.5VS, +1.5VS, +1.8VS,
AC_BAT_SYS

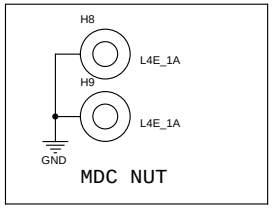
<Variant Name>

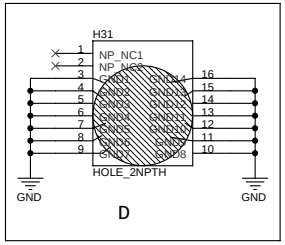
ASUSTeK COMPUTER INC. NB1	**Title :** DISCHARGE CKT	
	Engineer ***Mark , Frank***	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 47 of 52	









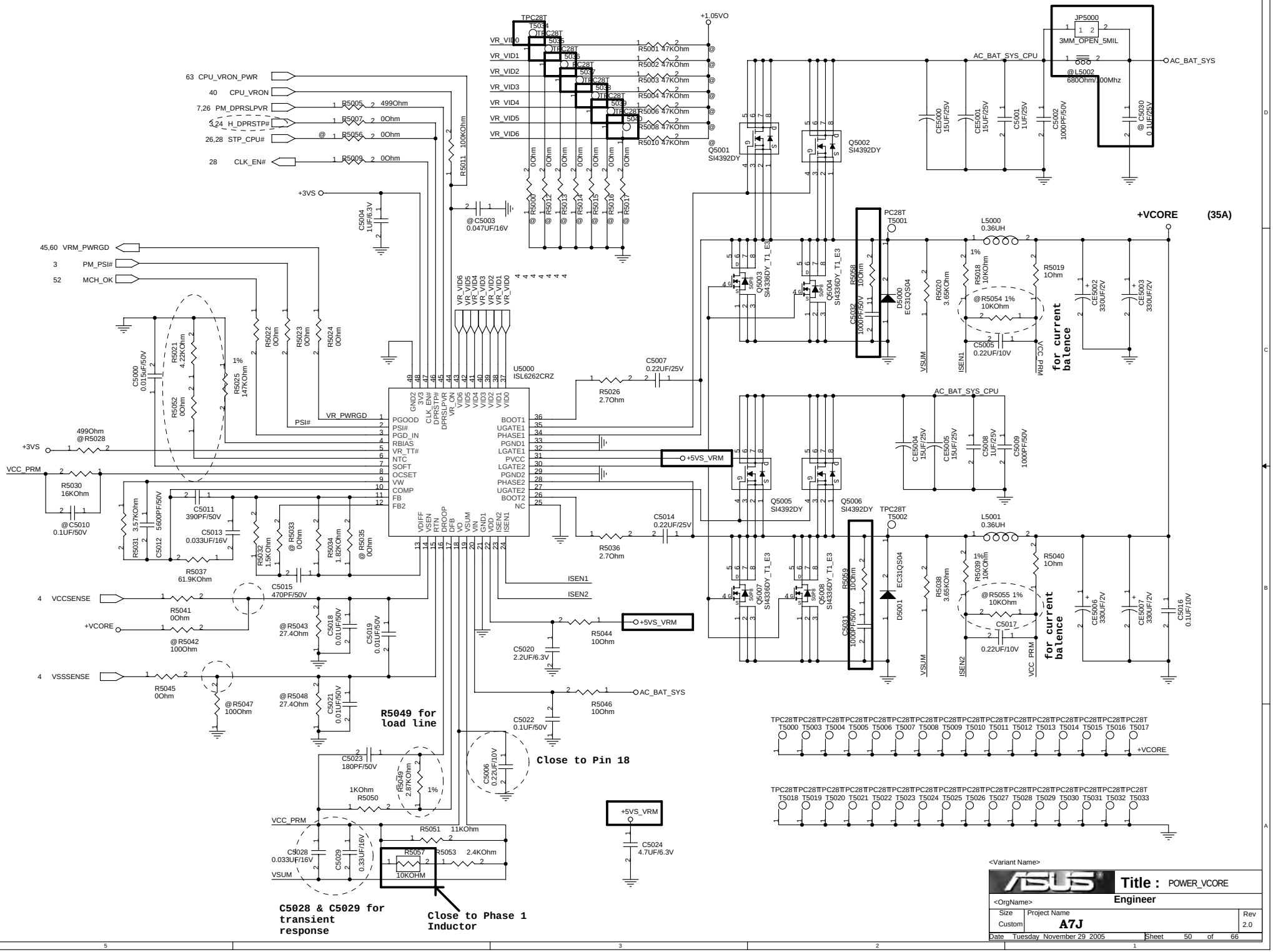


<variant_name>

ASUSTeK COMPUTER INC. NB1	Title : Screw Hole	
	Engineer Mark , Frank	
Size: Custom	Project Name: A7J	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 48 of 52	

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : GPIO SETTING	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday November 29 2005	Sheet 49 of 52	



<Variant Name>

ASUS

Title : POWER_VCORE

<OrgName>

Engineer

Size	Project Name	Rev
Custom	A7J	2.0

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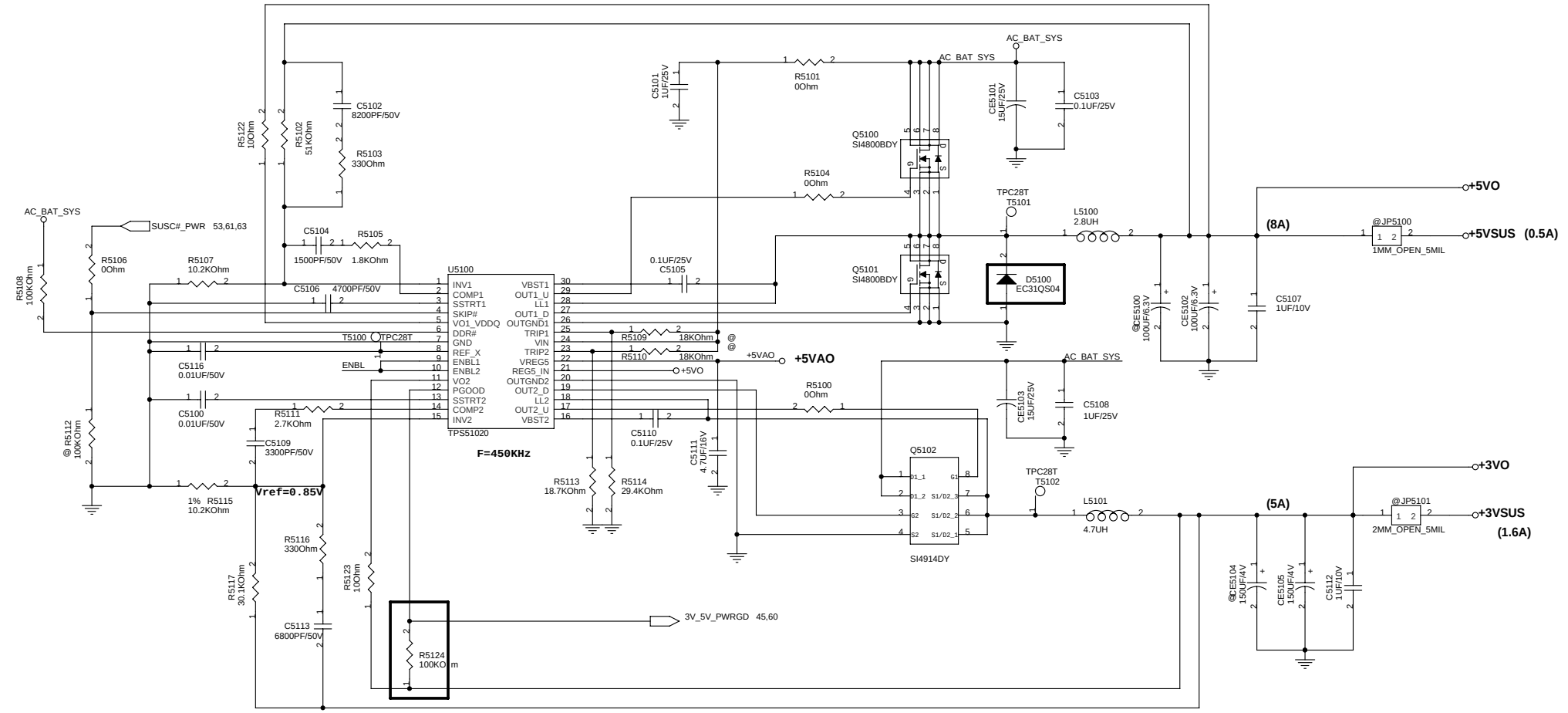
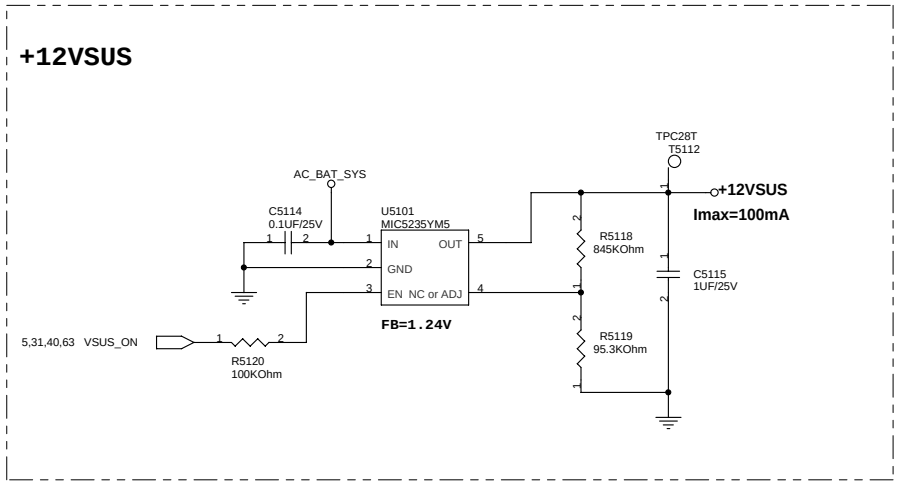
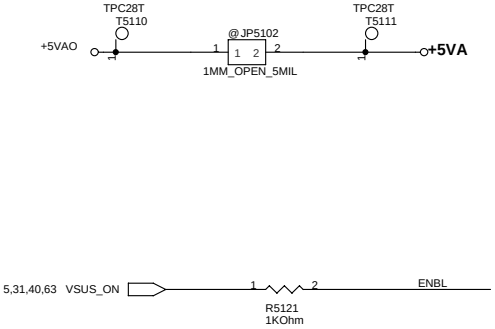
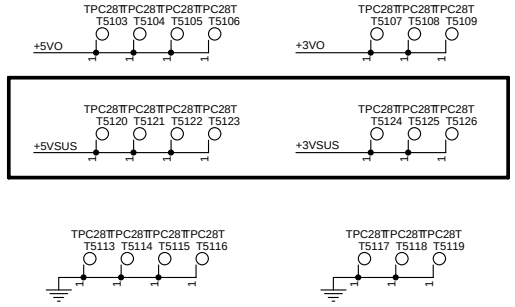

AC_BAT_SYS
SUSC#_PWR 53,61,63
U5100
TPS51020
F=450KHz
Vref=0.85V
ENBL
+5VAO
+5VO
+5VAO
Q5100 SI4800BDY
Q5101 SI4800BDY
Q5102
SI4914DY
D5100 EC31QS04
L5100 2.8UH
L5101 4.7UH
(8A)
(5A)
+5VSUS (0.5A)
+3VSUS (1.6A)
+3VO
1MM_OPEN_5MIL
2MM_OPEN_5MIL
3V_5V_PWRGD 45,60


+12VSUS
AC_BAT_SYS
U5101
MIC5235YM5
FB=1.24V
+12VSUS
Imax=100mA
5,31,40,63 VSUS_ON


+5VAO
@JP5102
1MM_OPEN_5MIL
+5VA
5,31,40,63 VSUS_ON
ENBL


+5VO
+3VO
+5VSUS
+3VSUS

<Variant Name>
Title : POWER_SYSTEM
<OrgName>
Engineer
Size Custom
Project Name A7J
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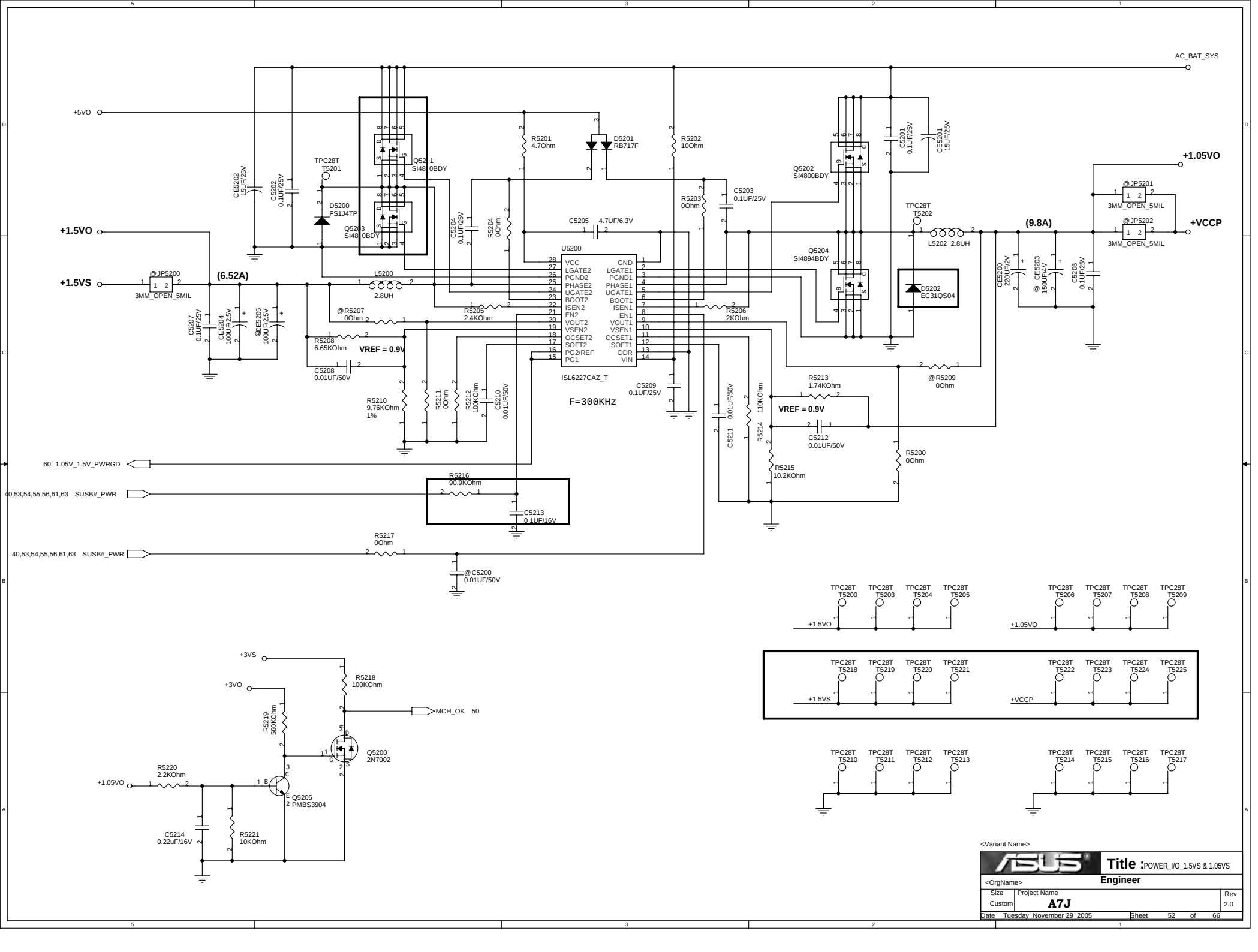
AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
(6.52A)
(9.8A)
3MM_OPEN_5MIL
TPC28T T5201
TPC28T T5202
D5200 FS1J4TP
Q5201 SI4800BDY
Q5203 SI4800BDY
Q5202 SI4800BDY
Q5204 SI4894BDY
D5201 RB717F
D5202 EC31QS04
L5200 2.8UH
L5202 2.8UH
R5201 4.7Ohm
R5202 10Ohm
R5203 0Ohm
R5204 0Ohm
R5205 2.4KOhm
R5206 2KOhm
R5207 0Ohm
R5208 6.65KOhm
R5209 0Ohm
R5210 9.76KOhm 1%
R5211 0Ohm
R5212 100KOhm
R5213 1.74KOhm
R5214 110KOhm
R5215 10.2KOhm
R5216 90.9KOhm
R5217 0Ohm
R5218 100KOhm
R5219 560KOhm
R5220 2.2KOhm
R5221 10KOhm
C5201 0.1UF/25V
C5202 0.1UF/25V
C5203 0.1UF/25V
C5204 0.1UF/25V
C5205 4.7UF/6.3V
C5206 0.1UF/25V
C5207 0.1UF/25V
C5208 0.01UF/50V
C5209 0.1UF/25V
C5210 0.01UF/50V
C5211 0.01UF/50V
C5212 0.01UF/50V
C5213 0.1UF/16V
C5214 0.22uF/16V
CE5200 15UF/25V
CE5201 15UF/25V
CE5203 150UF/4V
CE5204 100UF/2.5V
CE5205 100UF/2.5V
CE5206 220UF/2V
@C5200 0.01UF/50V
@JP5200
@JP5201
@JP5202
@R5207 0Ohm
@R5209 0Ohm
@CE5205 100UF/2.5V
@ CE5203 150UF/4V
U5200
ISL6227CAZ_T
F=300KHz
VREF = 0.9V
VREF = 0.9V
Q5200 2N7002
Q5205 2 PMBS3904
60 1.05V_1.5V_PWRGD
40,53,54,55,56,61,63 SUSB#_PWR
40,53,54,55,56,61,63 SUSB#_PWR
MCH_OK 50
+3VS
+3VO
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
TPC28T T5200
TPC28T T5203
TPC28T T5204
TPC28T T5205
TPC28T T5206
TPC28T T5207
TPC28T T5208
TPC28T T5209
TPC28T T5210
TPC28T T5211
TPC28T T5212
TPC28T T5213
TPC28T T5214
TPC28T T5215
TPC28T T5216
TPC28T T5217
TPC28T T5218
TPC28T T5219
TPC28T T5220
TPC28T T5221
TPC28T T5222
TPC28T T5223
TPC28T T5224
TPC28T T5225
<Variant Name>
Title : POWER_I/O_1.5VS & 1.05VS
<OrgName>
Engineer
Size Custom
Project Name A7J
Rev 2.0
Date Tuesday, November 29, 2005
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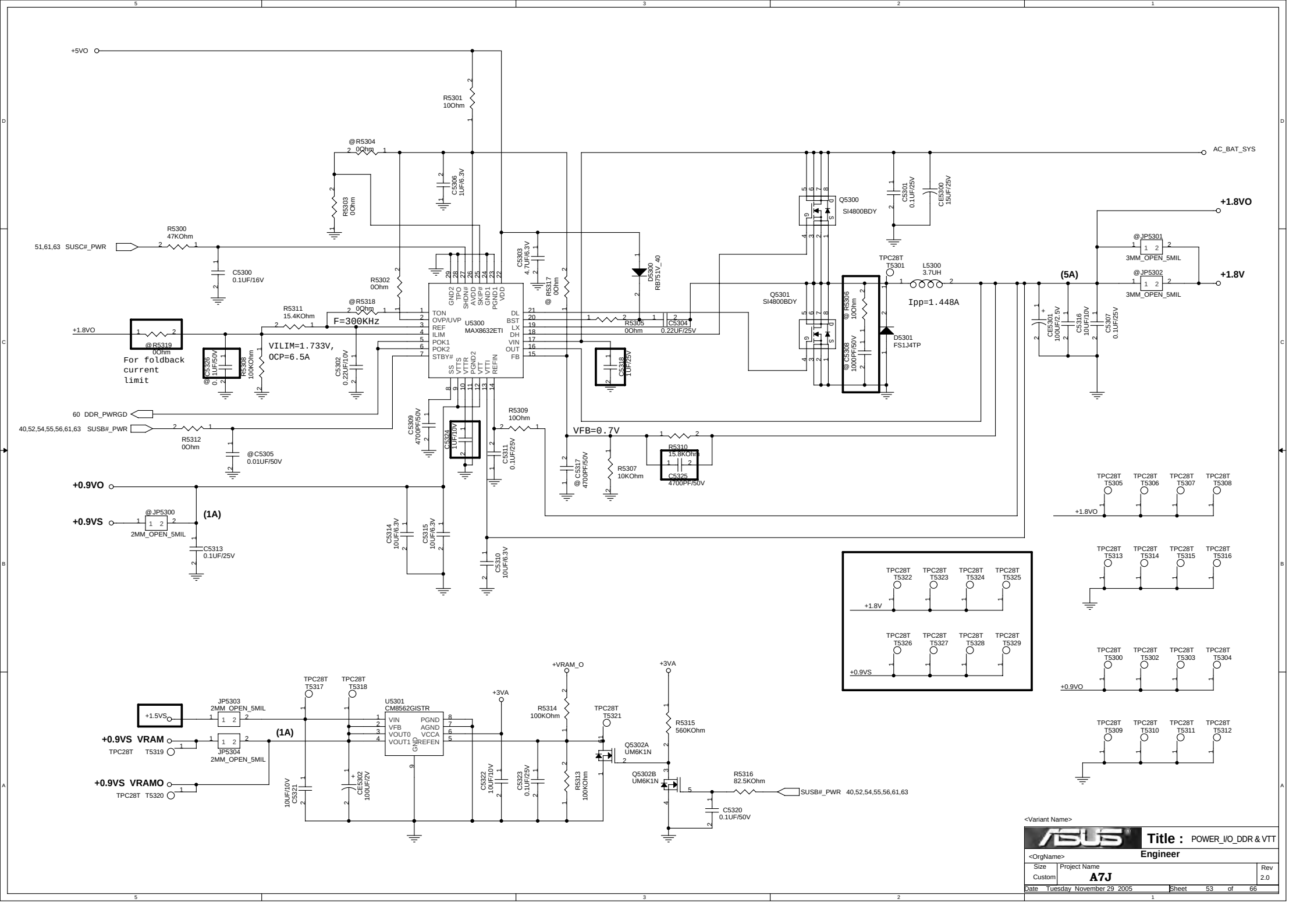

<Variant Name>

Title : POWER_I/O_DDR & VTT

<OrgName> **Engineer**

Size	Project Name	Rev
Custom	**A7J**	2.0

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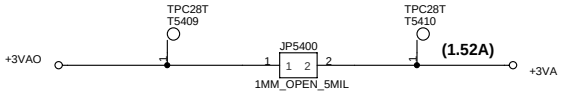
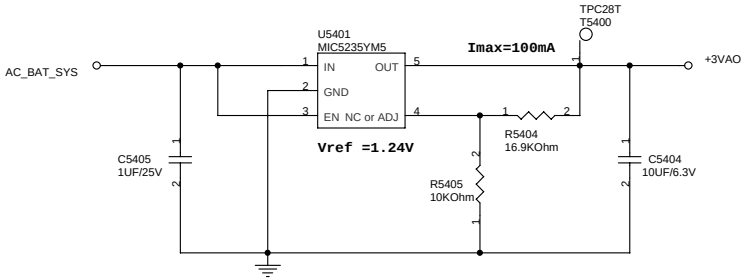
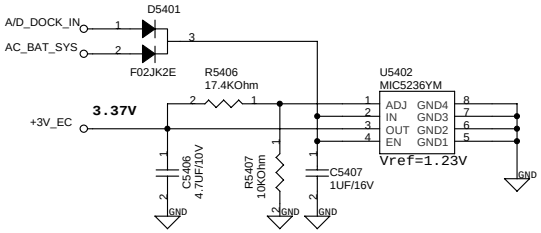
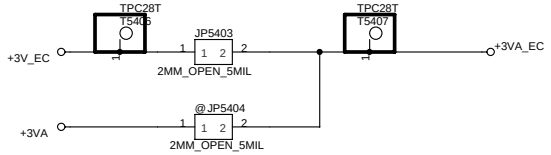
+3VA0



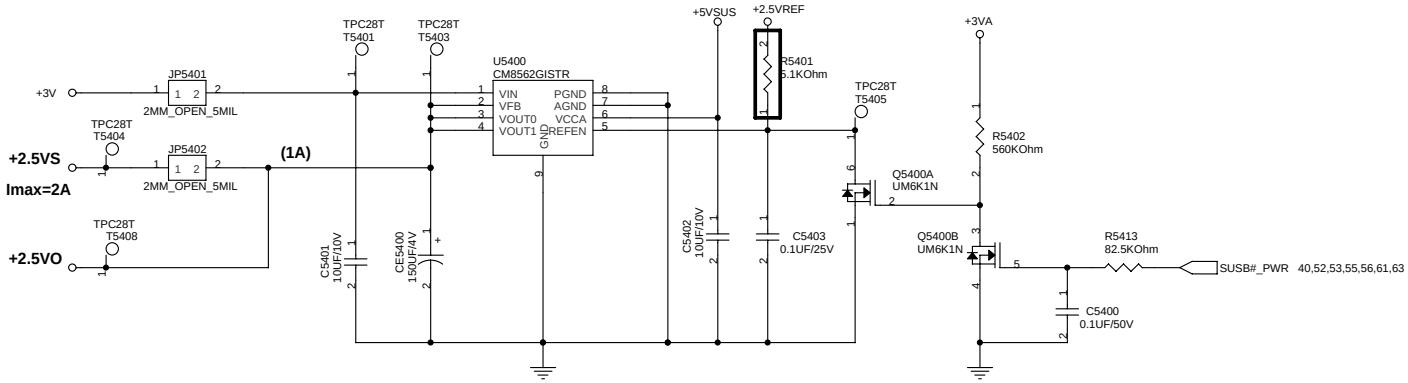


+3VA_EC





+2.5VS



<Variant Name>

ASUS

Title : POWER_I/O_+3VA & +2.5V

<OrgName> **Engineer**

Size	Project Name	Rev
Custom	**A7J**	2.0

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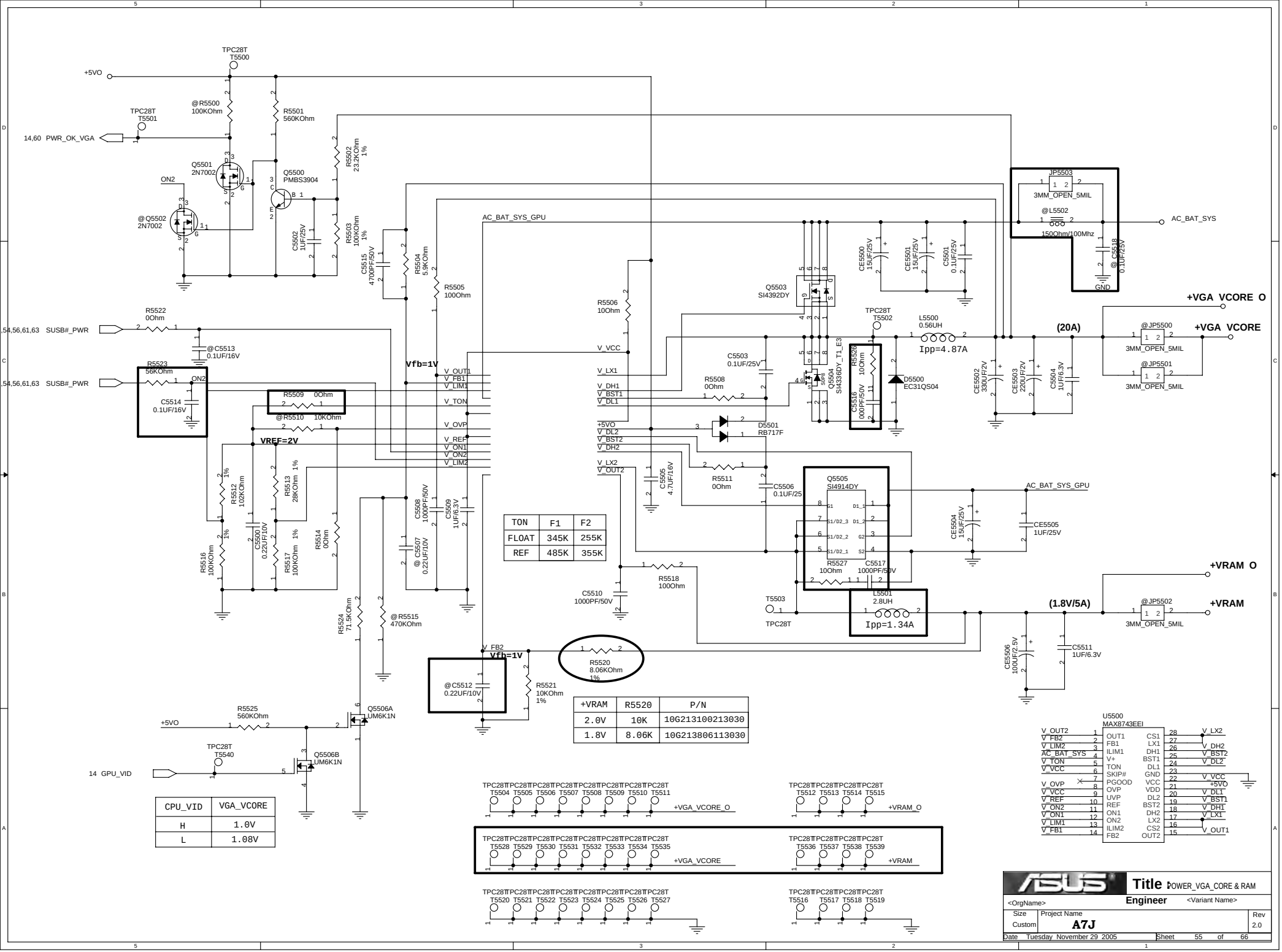

TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

CPU_VID	VGA_VCORE
H	1.0V
L	1.08V

ASUS

Title : POWER_VGA_CORE & RAM

<OrgName> **Engineer** <Variant Name>

Size	Project Name	Rev
Custom	**A7J**	2.0

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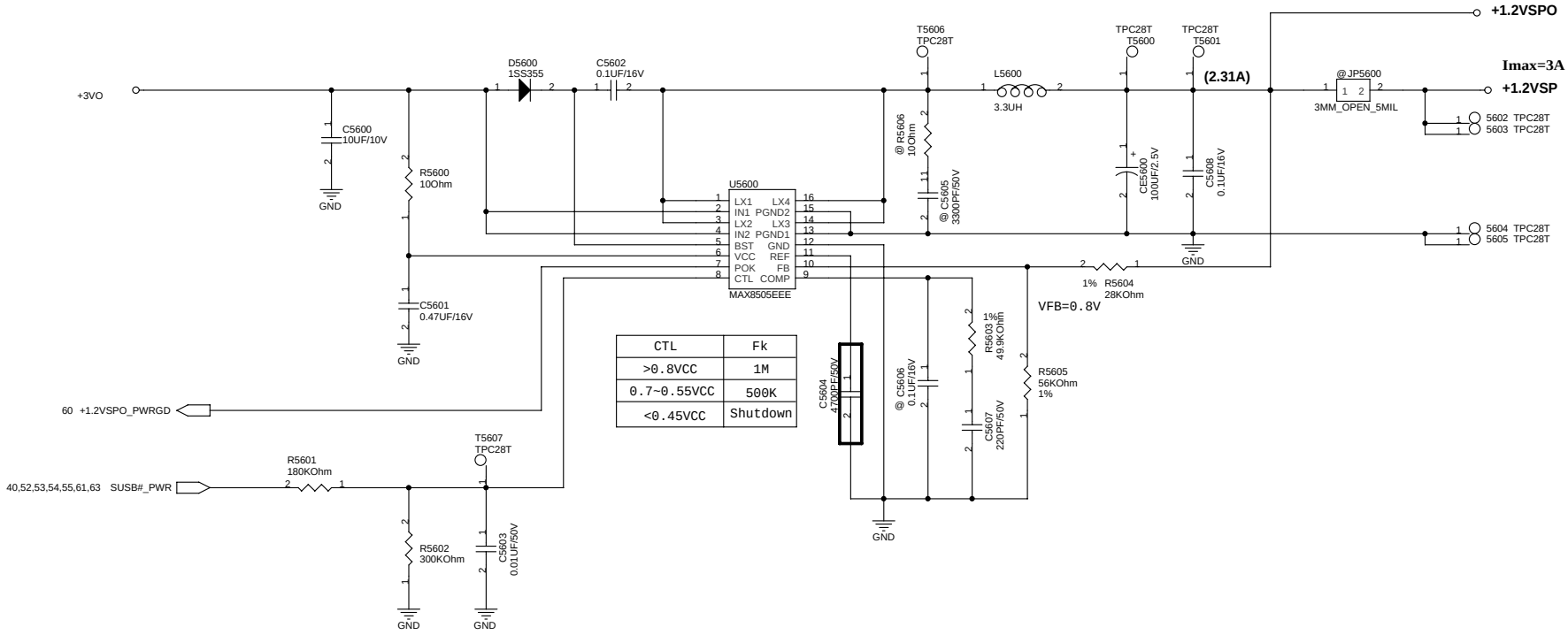
+1.2VSP



CTL	Fk
>0.8VCC	1M
0.7~0.55VCC	500K
<0.45VCC	Shutdown

<Variant Name>

Title : POWER_VGA_+1.2VSP

<OrgName> **Engineer**

Size	Project Name	Rev
Custom	**A7J**	2.0

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TOTAL_POWER=90W
-->4.73A

BATSEL_2P# = H (1P)			
BAT cpapcity	R5712	VICTL(V)	ICHG(A)
2000mAH	41.2K	1.8976	1.39
2200mAH	52.3K	2.0989	1.537
2400mAH	66.5K	2.2918	1.679
2600mAH	86.6K	2.4871	1.822

Charge Current Ichg =
[0.075V/Rsense(CHG)]*[VCLS/4.096V]
Rsense(CHG) 0.025 ohm
VICTL 3.4632V > Ichg 2.53A
VICTL 1.8976V > Ichg 1.39A

Vref 4 096V
VLDO 5 4V

VCTL LDO
> Vbatt 4.2V X CELLS

VICTL 2.506V

CHG_EN#	AC_APR_UC	SWITCH
H	H	OFF
H	L	ON
L	H	ON
L	L	ON

PRE_CHARGE CIRCUIT
Pre-charge voltage 12.6V

Adaptor error circuit for 4S battery
Vth = 17.5V (MAX. 17.8V & MIN. 17.2V)

Power Limit Circuit

Title :	POWER_CHARGER
<OrgName>	Engineer:
Size: C	Project Name: A7J
Rev: 2.0	
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<Variant Name>

Title : POWER_PIC

<OrgName> Engineer

Size	Project Name	Rev
Custom	A7J	2.0

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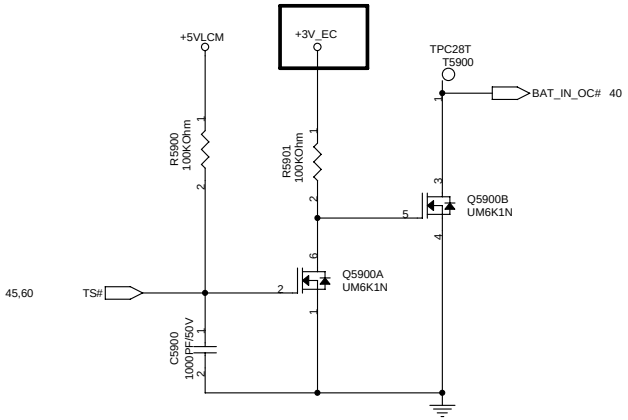
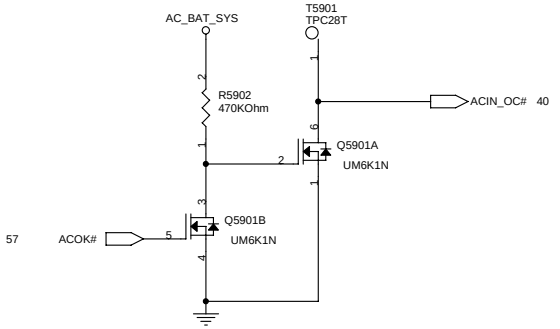
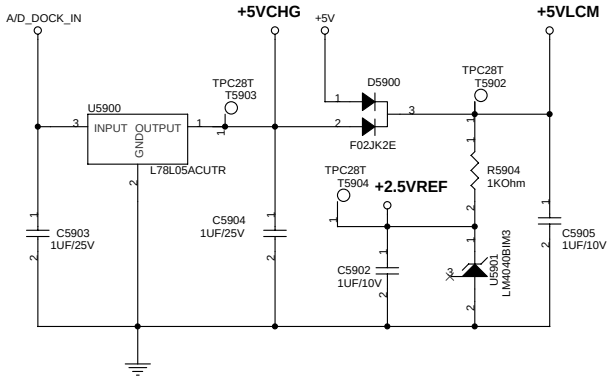
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



<Variant Name>

Title : POWER_DETECT

<OrgName> **Engineer**

Size	Project Name	Rev
Custom	**A7J**	2.0

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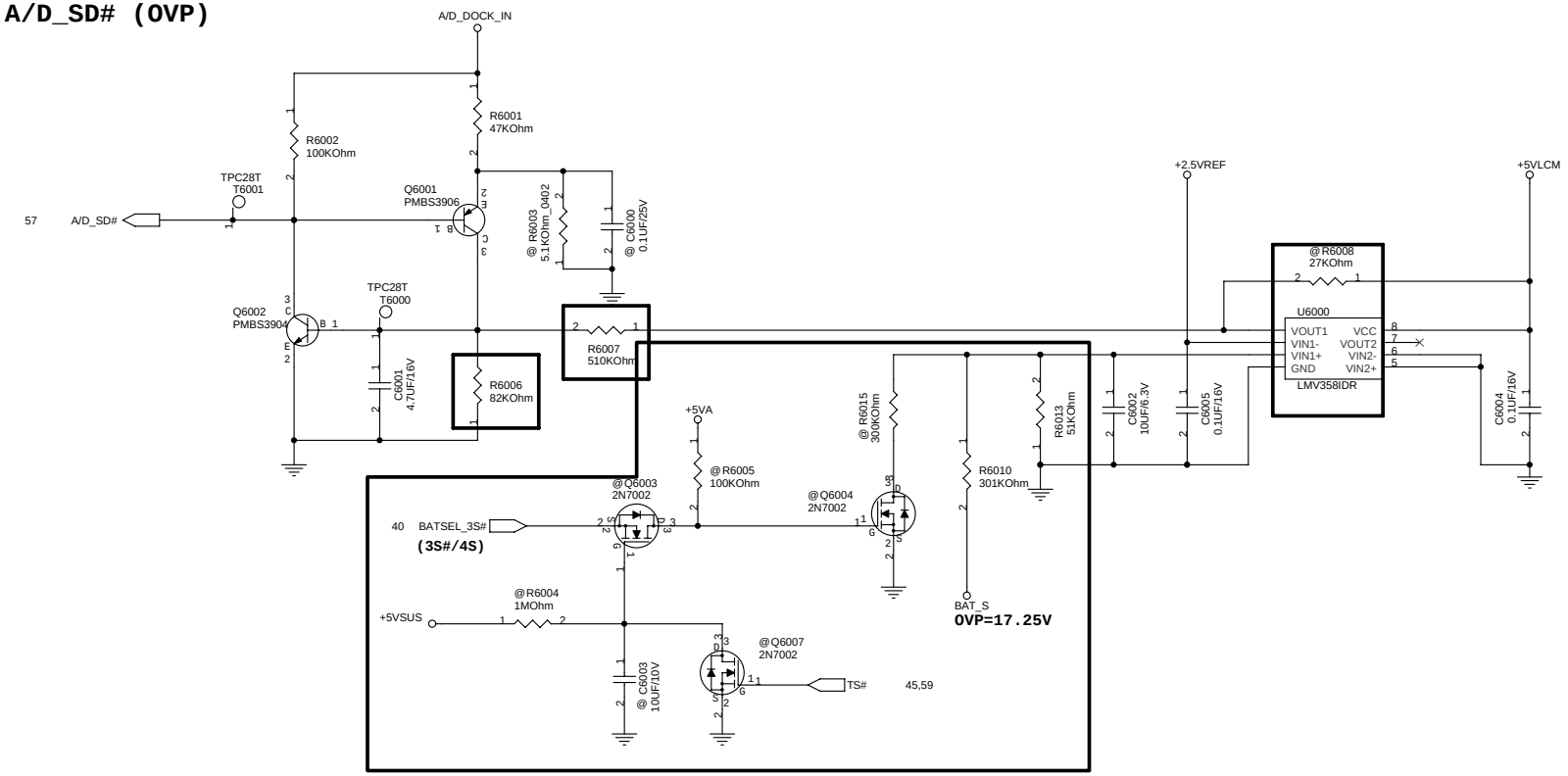
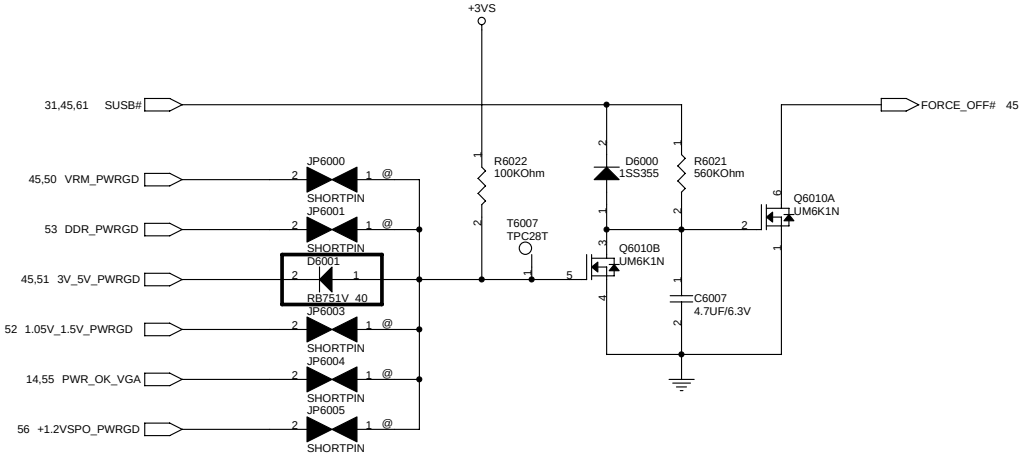
BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER



TPC28T T6003 — VRM_PWRGD

TPC28T T6004 — DDR_PWRGD

TPC28T T6005 — 3V_5V_PWRGD

TPC28T T6006 — 1.05V_1.5V_PWRGD

<Variant Name>

Title : POWER_PROTECT

<OrgName> Engineer

Size	Project Name	Rev
Custom	A7J	2.0

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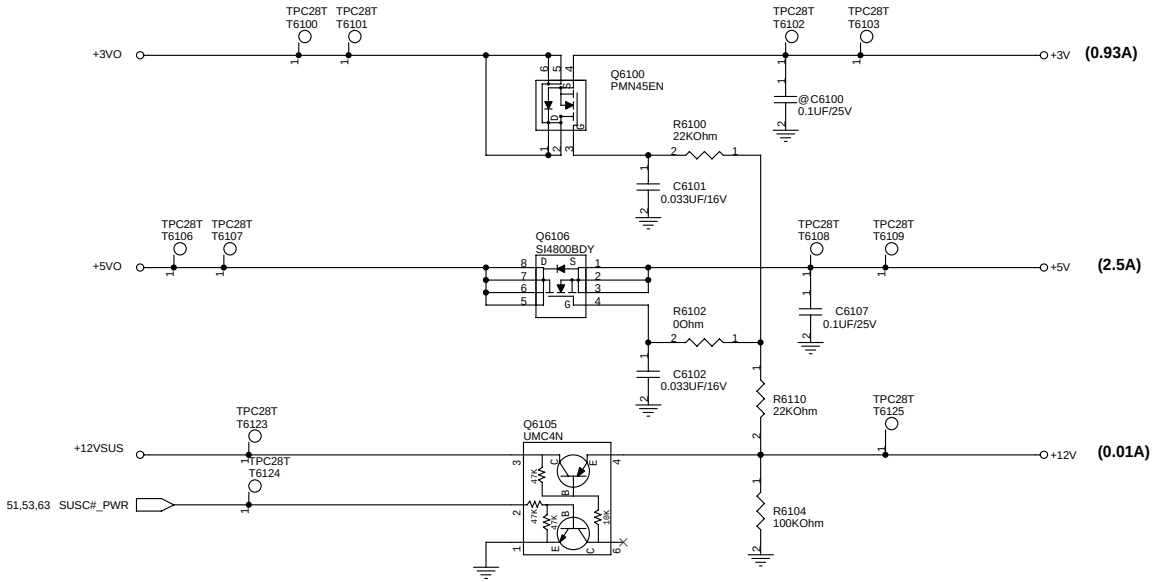
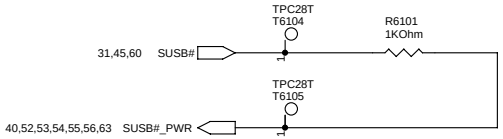
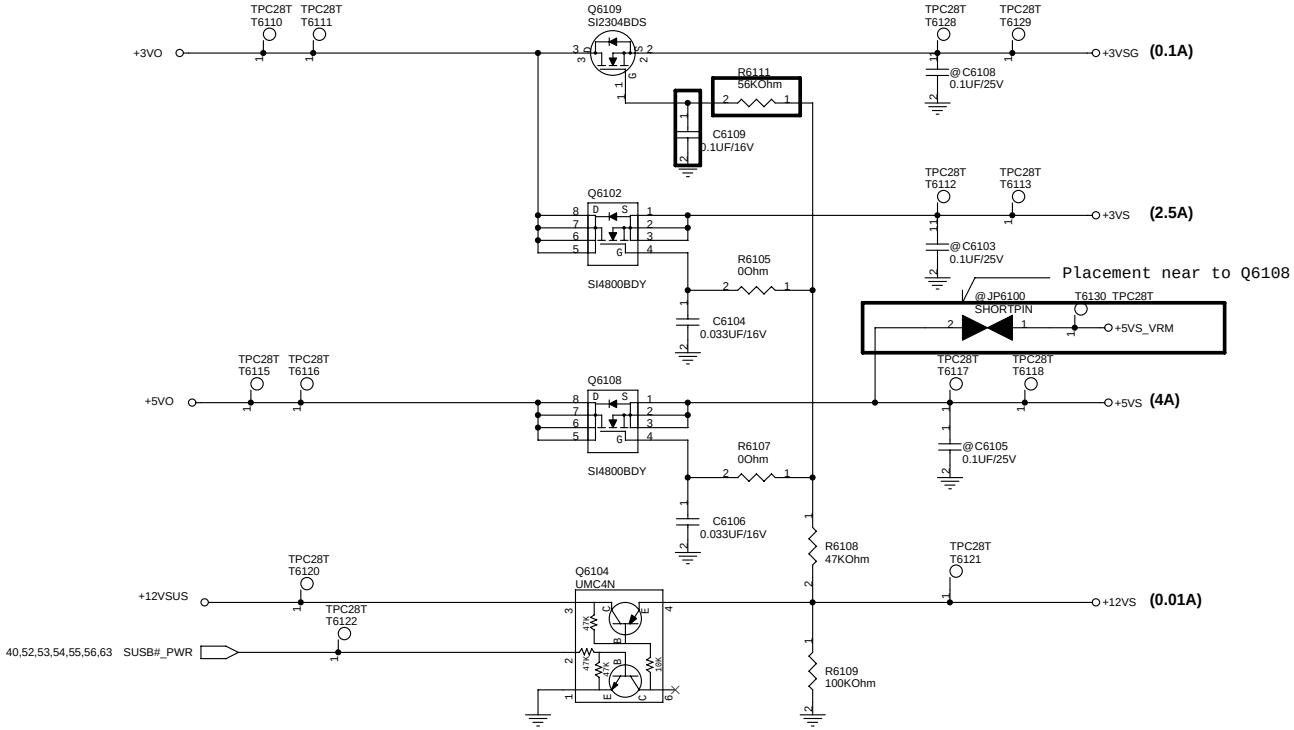
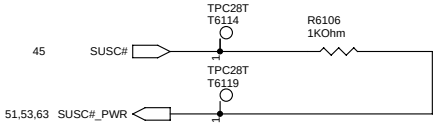
SUSC#_PWR POWER





SUSB#_PWR POWER





<Variant Name>

Title : POWER_LOAD SWITCH

<OrgName> Engineer

Size	Project Name	Rev
Custom	A7J	2.0

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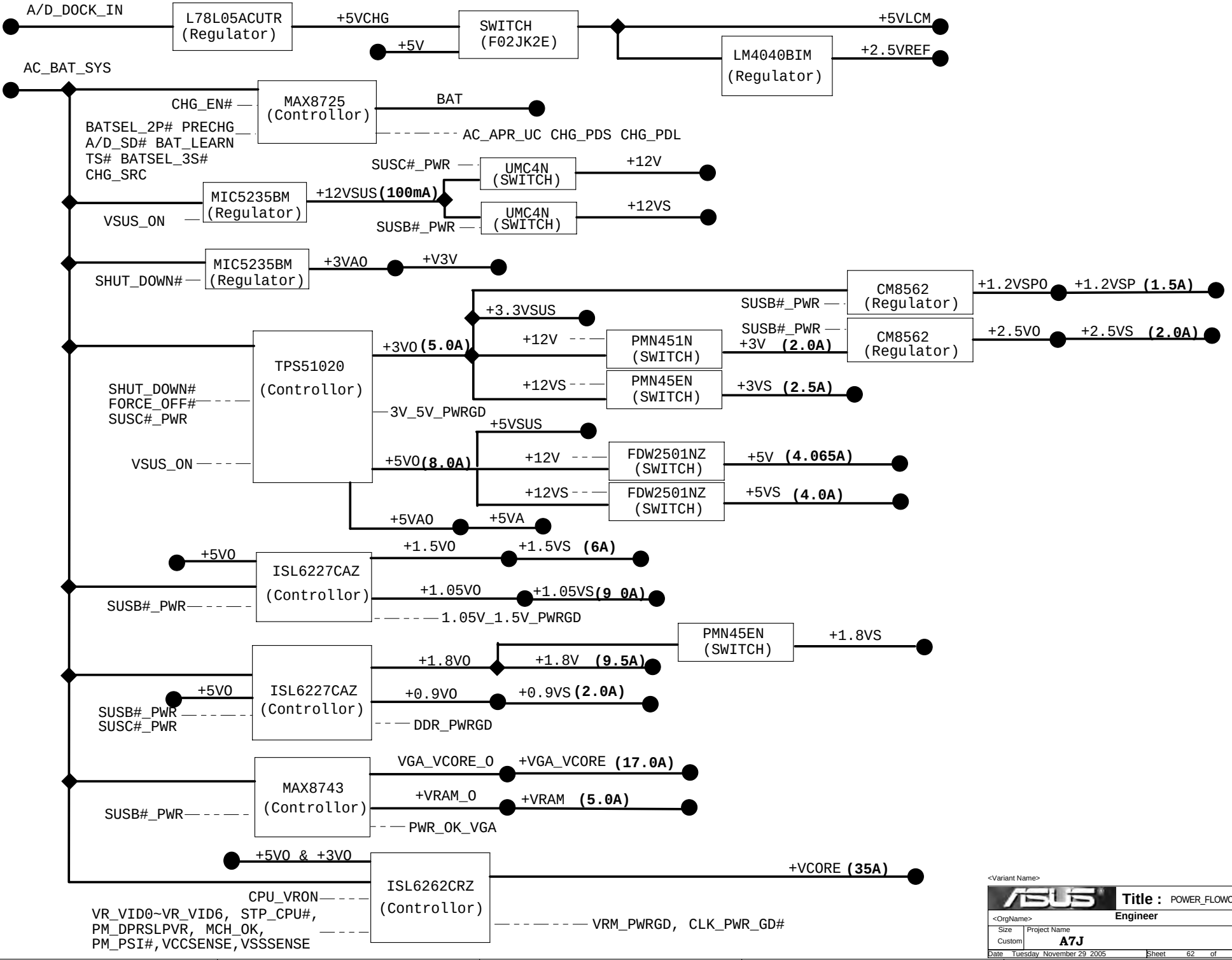

<Variant Name>

ASUS

Title : POWER_FLOWCHART

<OrgName> Engineer

Size	Project Name	Rev
Custom	A7J	2.0

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AC_BAT_SYS → AC_BAT_SYS 19,45,50,51,52,53,54,55,57,59

+3VA → +3VA 5,24,44,45,47,53,54

+5VA → +5VA 44,45,46,51,57,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3V → +3V 19,25,29,30,32,33,36,38,42,46,47,54,61

+3VS → +3VS 5,7,11,13,14,16,19,20,21,22,24,25,26,27,28,29,30,31,32,34,35,36,37,38,39,40,44,45,46,47,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 5,36,38,43,47,61

+12VS → +12VS 19,46,47,61

+5V → +5V 19,32,43,44,46,47,59,61

+5VS → +5VS 5,20,26,27,29,34,36,39,40,42,44,46,47,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 11,14,16,20,35,47,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,21,22,47,53

+0.9VS → +0.9VS 23,47,53

BAT → BAT 41,57

+5VCHG → +5VCHG 57,59

+5VLCM → +5VLCM 44,57,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 4,50

+VGA_VCORE → +VGA_VCORE 14,16,55

+VRAM → +VRAM 15,16,17,18,55

+1.2VSP → +1.2VSP 13,16,56

BAT_CON → BAT_CON 45,57

FOR POWER TEST

+3VA

@JP6300 (1 2 2) SGL_JUMP → CPU_VRON_PWR 50

@JP6301 (1 2 2) SGL_JUMP → SUSB#_PWR → SUSB#_PWR 40,52,53,54,55,56,61

@JP6302 (1 2 2) SGL_JUMP → SUSC#_PWR → SUSC#_PWR 51,53,61

@JP6303 (1 2 2) SGL_JUMP → VSUS_ON → VSUS_ON 5,31,40,51

<Variant Name>

Title : POWER_SIGNAL

<OrgName> Engineer

Size	Project Name	Rev
Custom	A7J	2.0

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PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (TV)	AD16	0	H,G

Host	SM-Bus Device	SM-Bus Address	Device
ICH7-M	Clock Generator	1101001x (D2)	ICS954310
ICH7-M	SO-DIMM 0	1010000x (A0)	DDR SOCKET1
ICH7-M	SO-DIMM 1	1010001x (A2)	DDR SOCKET2
ICH7-M			

ICH7-M GPIO	I/O Mode	Signal	Active	S0 Default	S3/S4	PWR Well
GPIO 0	INPUT	PM_BMBUSY#				+3VS
GPIO 1		PCI_REQ#5				+3VS
GPIO 2		PCI_INTE#				+3VS
GPIO 3		PCI_INTF#				+3VS
GPIO 4		PCI_INTG#				+3VS
GPIO 5		PCI_INTH#				+3VS
GPIO 6						+3VS
GPIO 7	INPUT	RF_OFF_SW#	**LOW**			+3VS
GPIO 8	INPUT	EXTSMI#	LOW			+3VSUS
GPIO 9	INPUT	SATA_DET#0	**LOW**			+3VSUS
GPIO 10						+3VSUS
GPIO 11	INPUT	SMBALERT#				+3VSUS
GPIO 12	INPUT	KB_SCI#	**LOW**			+3VSUS
GPIO 13	INPUT	SIO_SMI#	LOW			+3VSUS
GPIO 14	OUTPUT	802_LED_EN#	LOW	HIGH	Driven	+3VSUS
GPIO 15	OUTPUT	CB_SD#	**LOW**	HIGH	LOW	+3VSUS
GPIO 16		DPRSLPVR				+3VS
GPIO 17		GNT#5	PULL-DOWN:Boot BIOS destinat on select			+3VS
GPIO 18	OUTPUT	STP_PCI#				+3VS
GPIO 19	OUTPUT	PWRLED_1HZ	1 Hz	1 Hz	Off	+3VS
GPIO 20	OUTPUT	STP_CPU#				+3VS
GPIO 21		SATA0GP				+3VS
GPIO 22		REQ4#				+3VS
GPIO 23		LDRQ1#				+3VS
GPIO 24						+3VSUS
GPIO 25	OUTPUT	BT_LED_EN#	**LOW**	HIGH	Driven	+3VSUS
GPIO 26	INPUT	PCB_ID2	Default : 0			+3VSUS
GPIO 27	INPUT	PCB_ID1	Default : 0			+3VSUS
GPIO 28	INPUT	PCB_ID0	Default : 0			+3VSUS
GPIO 29		USB_OC5#				+3VSUS
GPIO 30		USB_OC6#				+3VSUS
GPIO 31		USB_OC7#				+3VSUS
GPIO 32	IN/OUTPUT	PM_CLKRUN#				+3VS
GPIO 33		AZ_DOCK_EN#				+3VSUS
GPIO 34		AZ_DOCK_RST#				+3VS
GPIO 35		SATACLKREQ#				+3VS
GPIO 36		SATA2GP				+3VS
GPIO 37						+3VS
GPIO 38	OUTPUT	BT_ON#	**LOW**	LOW	Off	+3VS
GPIO 39	OUTPUT	WLAN_ON#	**LOW**	LOW	Off	+3VS
GPIO 48		GNT#4	PULL-DOWN:Boot BIOS destinat on select			+3VS
GPIO 49	OUTPUT	H_PWRGD				+Vccp

<Variant Name>

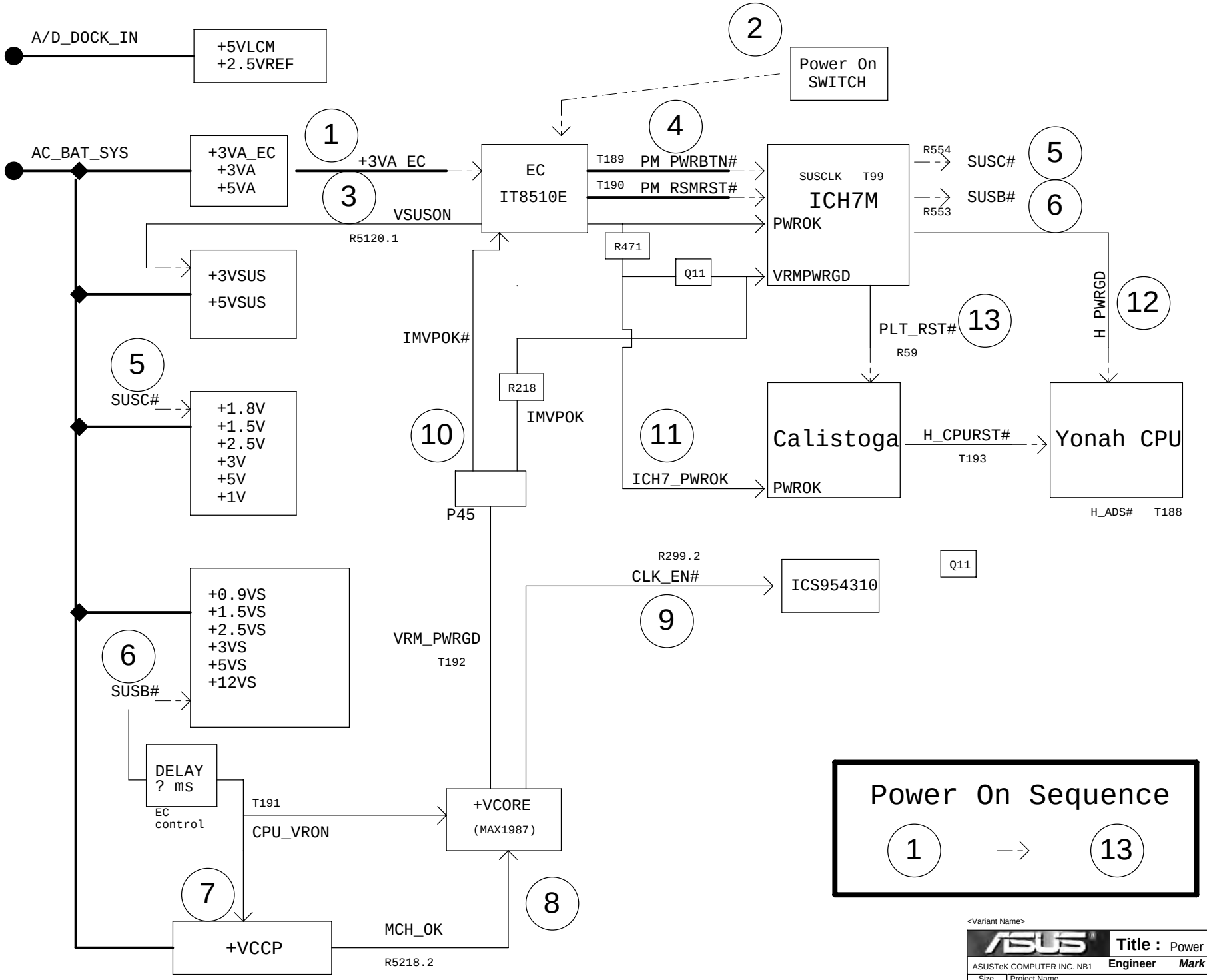
ASUSTeK COMPUTER INC. NB1

Title : System Resource

Engineer: ***Mark , Frank***

Size	Project Name	Rev
Custom	**A7J**	2.0

Date: Tuesday, November 29, 2005 Sheet 64 of 66



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : Power On Sequrnce	
	Engineer *Mark , Frank*	
Size: Custom	Project Name: **A7J**	Rev: 2.0
Date: Tuesday, November 29, 2005	Sheet 65 of 66	

Rev	Date	Description
1.0	05/09/13	Initial release.
1.1		R1.1 release
	P44	DJ Board CON32 Pin define mirror
		Fix leakage problem, R509 pull up +3VA
		Modify Q39~Q47 sequence
	P47	Fix Discharge circuit
	P36	Modify AC_OUTA_R & ACOUTA_L filter
	P40	DEL R463 pull high (internal pull high)
	P41	Modify AC_AD & BAT0_AD
	P43	Change F1 & F2 fuse size
2.0		R2.0 release

Rev	Date	Description

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : REVISION HISTORY

Engineer *Mark , Frank*

Size	Project Name	Rev
Custom	A7J	2.0

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