

iPhone 4S Professional Schematic

Special Thanks!



wins200786

GPA-FORUM

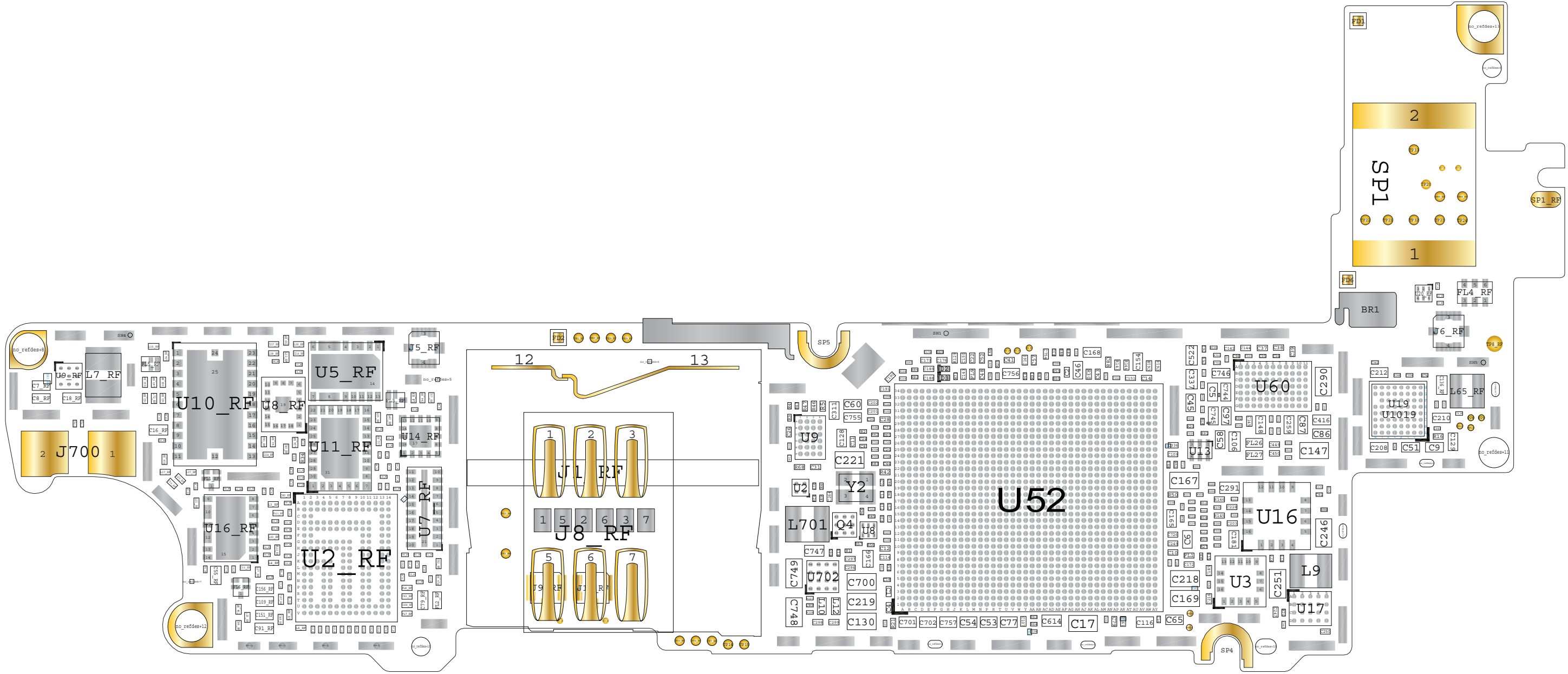
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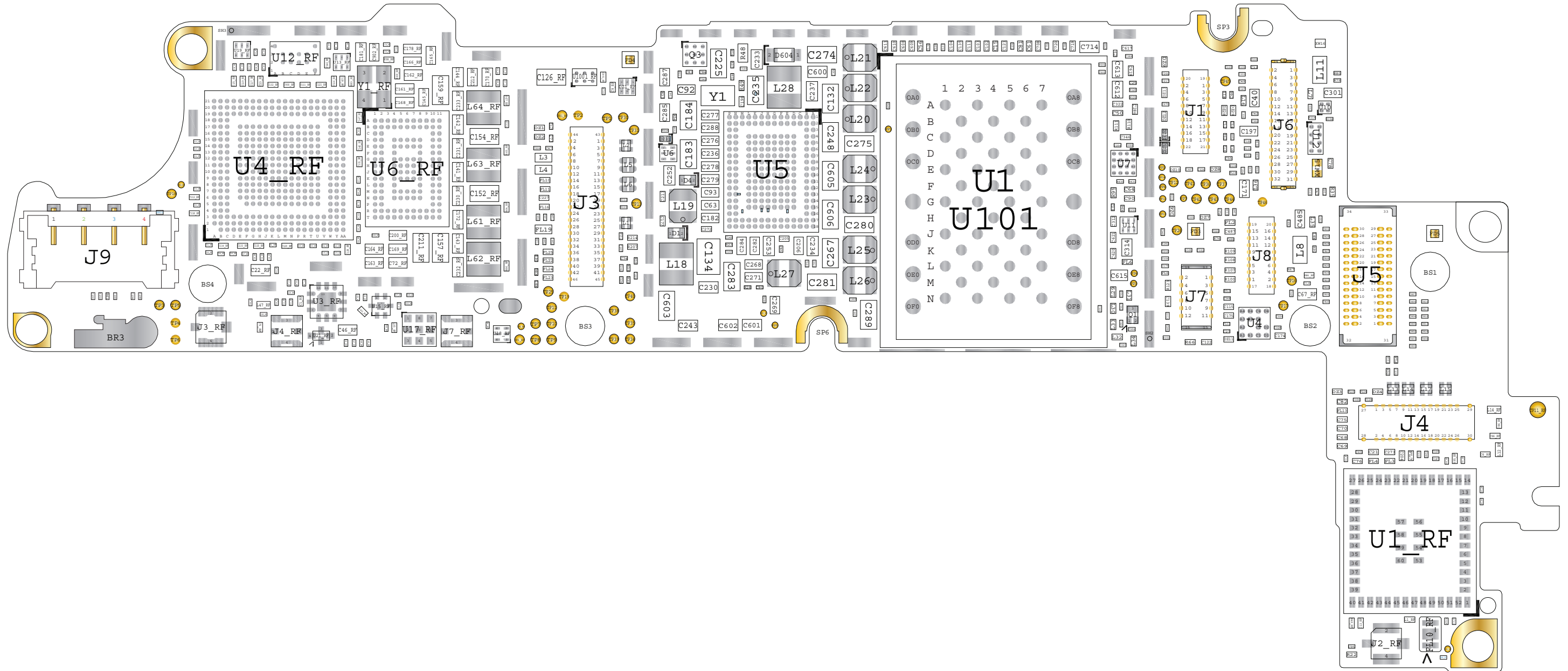
Remake by
Wites OM Tesla



Pagani DVT MLB Top Placement Drawing
PCB:820-3031-11 and 820-3031-12 (no surface PAD difference)



Pagani DVT MLB Bottom Placement Drawing
PCB:820-3031-11 and 820-3031-12 (no surface PAD difference)



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Tue Jul 5 21:36:16 2011

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
12	0001170763	ENGINEERING RELEASED		2011-07-05

N94 POR MLB_V3 DVT FOR BOARD_REV11/REV12

PDF PAGE	CSA PAGE	CONTENTS	SYNC MASTER	DATE
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N94 EEEE BOM LABELS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-2029	1	EEEE FOR 639-1723 (16G)	EEEE_DJF1	Y	EEEE_16G_GUC_US
825-2029	1	EEEE FOR 639-1724 (32G)	EEEE_DJF2	Y	EEEE_32G_GUC_US
825-2029	1	EEEE FOR 639-1777 (64G)	EEEE_DR00	Y	EEEE_64G_GUC_US
825-2029	1	EEEE FOR 639-2727 (16G)	EEEE_DQ5M	Y	EEEE_16G_GU_US
825-2029	1	EEEE FOR 639-2728 (32G)	EEEE_DQ5D	Y	EEEE_32G_GU_US
825-2029	1	EEEE FOR 639-2729 (64G)	EEEE_DQ5G	Y	EEEE_64G_GU_US
825-2029	1	EEEE FOR 639-2788 (16G)	EEEE_DR42	Y	EEEE_16G_GU_EU
825-2029	1	EEEE FOR 639-2789 (32G)	EEEE_DR44	Y	EEEE_32G_GU_EU
825-2029	1	EEEE FOR 639-2790 (64G)	EEEE_DR41	Y	EEEE_64G_GU_EU

N94 SCH & PCB BOM CALLOUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-8890	1	N94_MLB_V3 SCHEMATIC	SCH	Y	?
820-3031	1	N94_MLB_V3 PCB	PCB	Y	?

NAND BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0781	1	16G,HYNIX 26NM PPN10 TLGA52	U1	Y	NAND_16GB_PPN10
335S0782	1	32G,HYNIX 26NM PPN10 TLGA52	U1	Y	NAND_32GB_PPN10
335S0814	1	64G,HYNIX 26NM PPN10 TLGA52	U1	Y	NAND_64GB_PPN10

WIFI/BT MODULE BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0143	1	MURATA WIFI_BT MODULE	U1_RF	Y	WIFI_BT_MODULE

WIFI/BT MODULE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0154	339S0143	WIFI_BT_MODULE	U1_RF	USI WIFI_BT_MODULE
339S0155	339S0143	WIFI_BT_MODULE	U1_RF	SEMCO WIFI_BT_MODULE

UPPER ANTENNA MATCHING BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
131S0318	1	CAP,CER,COG,1.6PF,+/-0.1PF,25V	0201,HQ	C6_RF	Y	UAT_US
152S0562	1	IND,WV,HF,5.1NH,+/-0.2NH,470MA	03015	L12_RF	Y	UAT_US
C66_RF = NOSTUFF						
131S0364	1	CAP,CER,4.7PF,+/-0.1PF,25V,COG	0201,HQ	C86_RF	Y	UAT_US
152S1240	1	IND,WV,HF,4.3NH,+/-0.2NH,530MA	03015	L14_RF	Y	UAT_US
131S0279	1	CAP,CER,COG,1.3PF,+/-0.1PF,25V	0201,HQ	C6_RF	Y	UAT_EU
152S0562	1	IND,WV,HF,5.1NH,+/-0.2NH,470MA	03015	L12_RF	Y	UAT_EU
131S0278	1	CAP,CER,CCOG,HF,1PF,+/-0.1PF,2V	0201,HQ	C66_RF	Y	UAT_EU
131S0449	1	CAP,CER,3.6PF,+/-0.1PF,25V,COG	0201,HQ	C86_RF	Y	UAT_EU
152S1240	1	IND,WV,HF,4.3NH,+/-0.2NH,530MA	03015	L14_RF	Y	UAT_EU

VIDEO BUFFER ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0539	343S0520		U9	INTERSIL VIDEO BUFFER

32KHZ XTAL ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0382	197S0392		Y1	TXC XTAL

STROBE INDUCTOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1173	152S0979		L9	CYNTEC INDUCTOR

CHARGER INDUCTOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1051	152S0927		L28	CYNTEC INDUCTOR

4.3UF CAP ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			MURATA 4.3UF CAP

INVERTER GATE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0549	311S0539		U19_RF	TI INVERTER GATE

AND GATE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0548	311S0398		U18_RF,U20_RF	TI 2-INPUT AND GATE

19.2MHZ ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0402	197S0340		Y1_RF	NDK 19.2MHZ XTAL

LEVEL TRANSLATOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0562	311S0372		U11	TI LEVEL TRANSLATOR

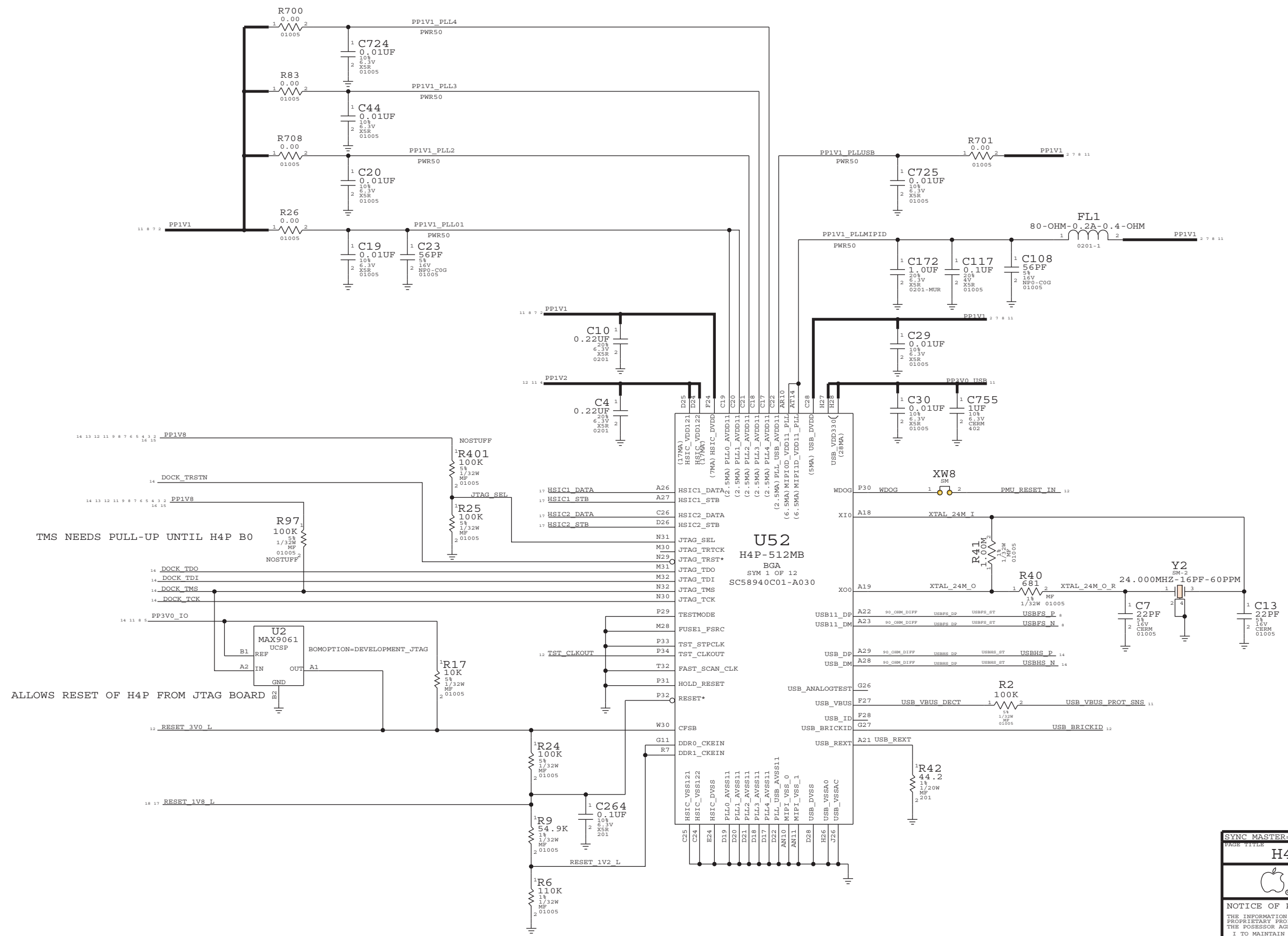
THERMISTOR ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0208	107S0150		R21,R22,R34,R35	MURATA THERMISTOR

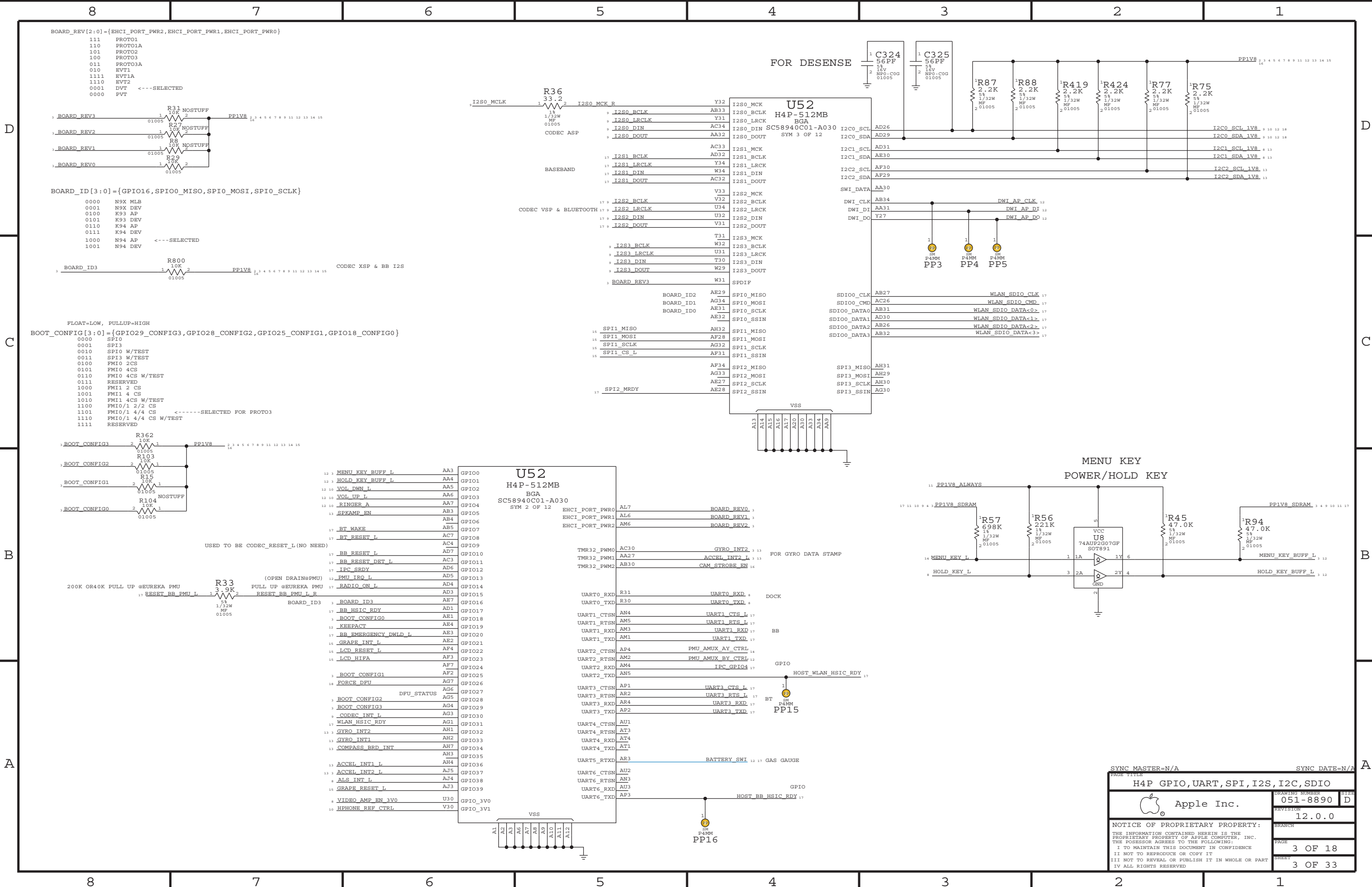
SCH 051-8890
BRD 820-3031
MCO 056-4257

BOM 639-1723(16G,GUC,US)
BOM 639-1724(32G,GUC,US)
BOM 639-1777(64G,GUC,US)
BOM 639-2727(16G,GU,US)
BOM 639-2728(32G,GU,US)
BOM 639-2729(64G,GU,US)
BOM 639-2788(16G,GU,EU)
BOM 639-2789(32G,GU,EU)
BOM 639-2790(64G,GU,EU)

DRAWING TITLE		DRAWING NUMBER		SIZE
N94 MLB_V3		051-8890		D
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PAGE TITLE		SYNC DATE=N/A	
H4P JTAG, USB, PLL			
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		PAGE	2 OF 18
		SHEET	2 OF 33



```

BOARD_REV[2:0] = {EHCI_PORT_PWR2, EHCI_PORT_PWR1, EHCI_PORT_PWR0}
111  PROTO1
110  PROTO1A
101  PROTO2
100  PROTO3
011  PROTO3A
010  EVT1
1111  EVT1A
1110  EVT2
0001  DVT
0000  PVT
    
```

```

BOARD_ID[3:0] = {GPIO16, SPI0_MISO, SPI0_MOSI, SPI0_SCLK}
0000  N9X MLB
0001  N9X DEV
0100  K93 AP
0101  K93 DEV
0110  K94 AP
0111  K94 DEV
1000  N94 AP
1001  N94 DEV
    
```

```

FLOAT=LOW, PULLUP=HIGH
BOOT_CONFIG[3:0] = {GPIO29_CONFIG3, GPIO28_CONFIG2, GPIO25_CONFIG1, GPIO18_CONFIG0}
0000  SPI0
0001  SPI3
0010  SPI0 W/TEST
0011  SPI3 W/TEST
0100  FMIO 2CS
0101  FMIO 4CS
0110  FMIO 4CS W/TEST
0111  RESERVED
1000  FM11 2 CS
1001  FM11 4 CS
1010  FM11 4CS W/TEST
1100  FMIO/1 2/2 CS
1101  FMIO/1 4/4 CS
1110  FMIO/1 4/4 CS W/TEST
1111  RESERVED
    
```

12	MENU_KEY_BUFF_L	AA3	GPIO0
12	HOLD_KEY_BUFF_L	AA4	GPIO1
12	VOL_DWN_L	AA5	GPIO2
12	VOL_UP_L	AA6	GPIO3
12	RINGER_A	AA7	GPIO4
13	SPKAMP_EN	AB3	GPIO5
		AB4	GPIO6
17	BT_WAKE	AB5	GPIO7
		AC7	GPIO8
		AC4	GPIO9
17	BB_RESET_L	AD7	GPIO10
17	BB_RESET_DET_L	AC3	GPIO11
17	IPC_SRDY	AD6	GPIO12
		AD5	GPIO13
		AD4	GPIO14
17	RADIO_ON_L	AD3	GPIO15
3	BOARD_ID3	AE7	GPIO16
17	BB_HSDY	AD1	GPIO17
3	BOOT_CONFIG0	AE1	GPIO18
3	KEEPACT	AE4	GPIO19
17	BB_EMERGENCY_DWLD_L	AE3	GPIO20
15	GRAPE_INT_L	AE2	GPIO21
15	LCD_RESET_L	AF4	GPIO22
15	LCD_HIFA	AF3	GPIO23
		AF7	GPIO24
		AF2	GPIO25
3	BOOT_CONFIG1	AG7	GPIO26
18	FORCE_DFU	AG6	GPIO27
		AG5	GPIO28
3	BOOT_CONFIG2	AG4	GPIO29
3	BOOT_CONFIG3	AG3	GPIO30
9	CODEC_INT_L	AG3	GPIO30
17	WLAN_HSDY	AG1	GPIO31
13	GYRO_INT2	AH1	GPIO32
13	GYRO_INT1	AH2	GPIO33
13	COMPASS_BRD_INT	AH7	GPIO34
		AH3	GPIO35
		AH4	GPIO36
13	ACCEL_INT1_L	AJ5	GPIO37
13	ACCEL_INT2_L	AJ5	GPIO37
8	ALS_INT_L	AJ4	GPIO38
15	GRAPE_RESET_L	AJ3	GPIO39
8	VIDEO_AMP_EN_3V0	U30	GPIO_3V0
10	HPHONE_REF_CTRL	V30	GPIO_3V1

SYNC MASTER=N/A SYNC DATE=N/A

H4P GPIO, UART, SPI, I2S, I2C, SDIO

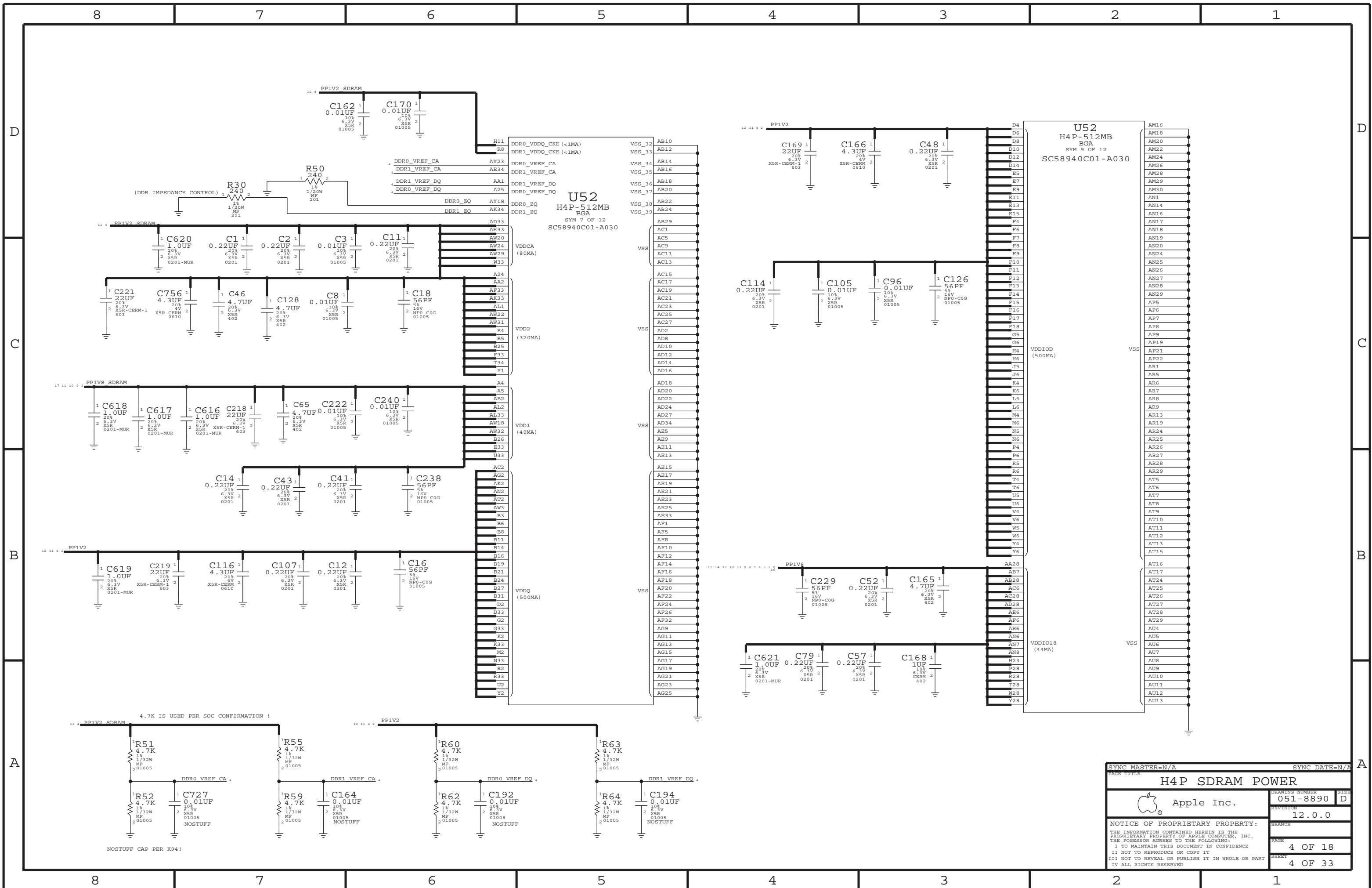
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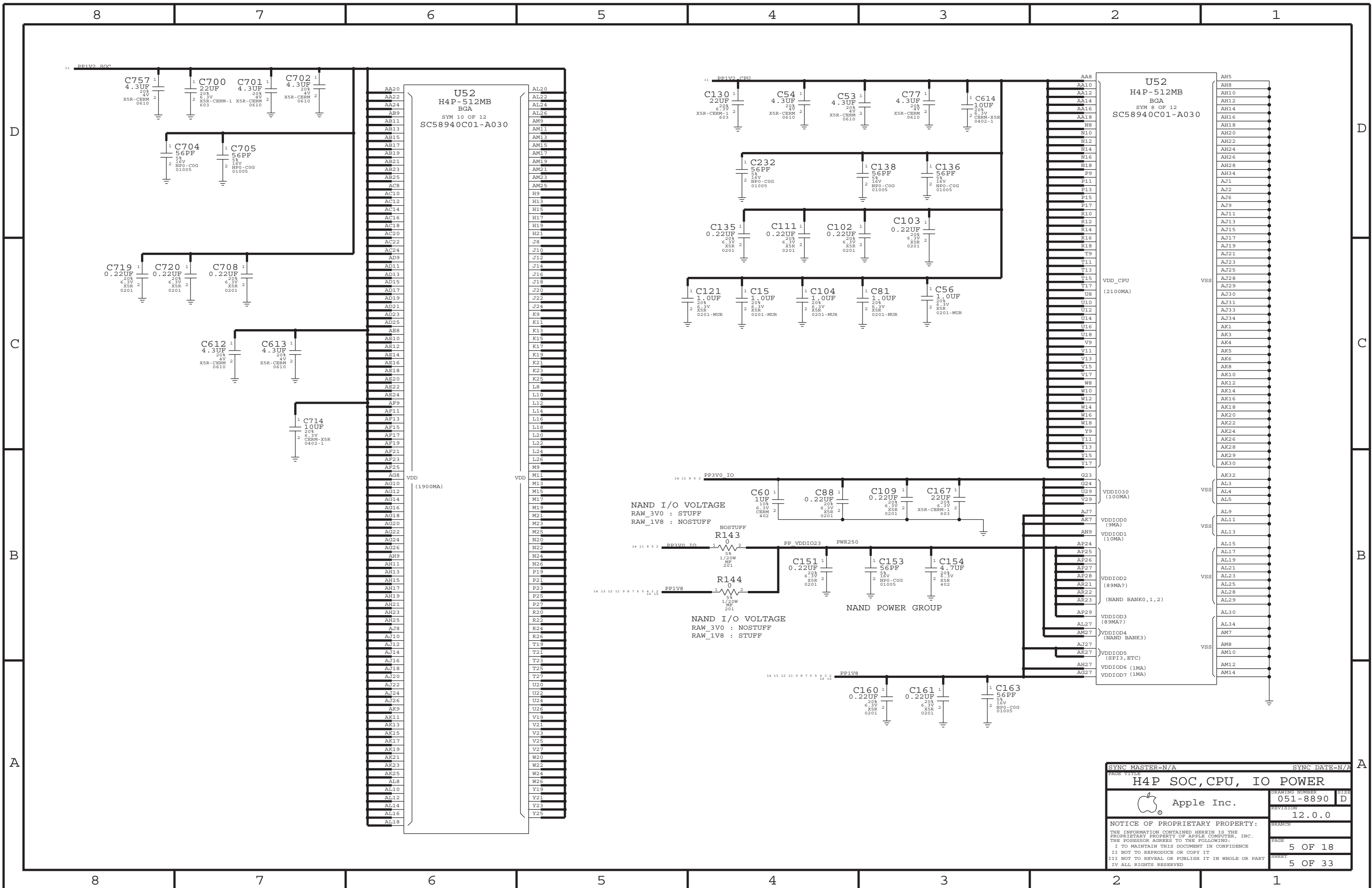
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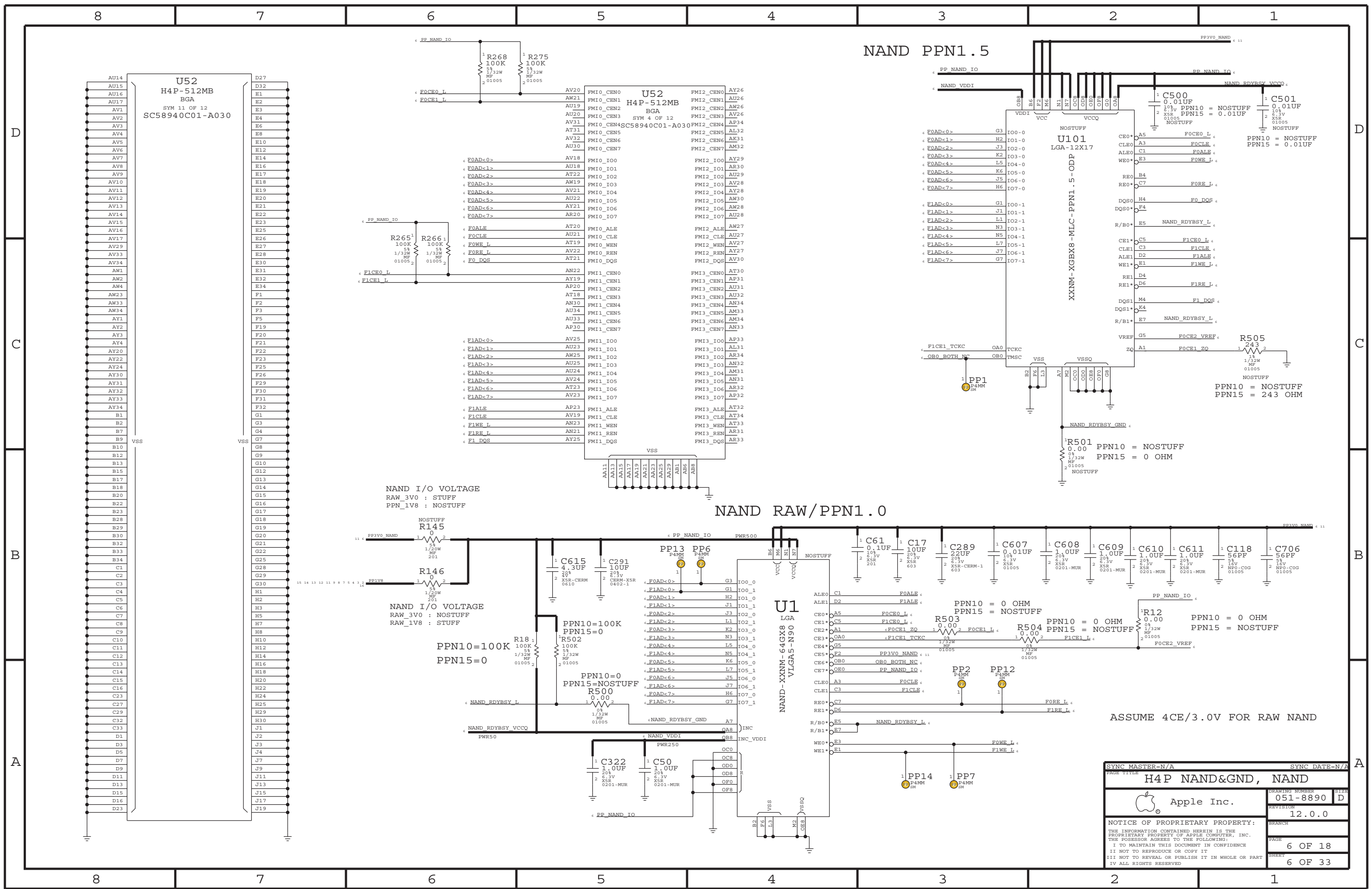
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H4P SDRAM POWER			
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H4P SOC, CPU, IO POWER			
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NAND PPN1.5

NAND RAW/PPN1.0

NAND I/O VOLTAGE
 RAW_3V0 : STUFF
 PPN_1V8 : NOSTUFF

NAND I/O VOLTAGE
 RAW_3V0 : NOSTUFF
 RAW_1V8 : STUFF

PPN10=100K
 PPN15=0

PPN10=100K
 PPN15=0

PPN10=0
 PPN15=NOSTUFF

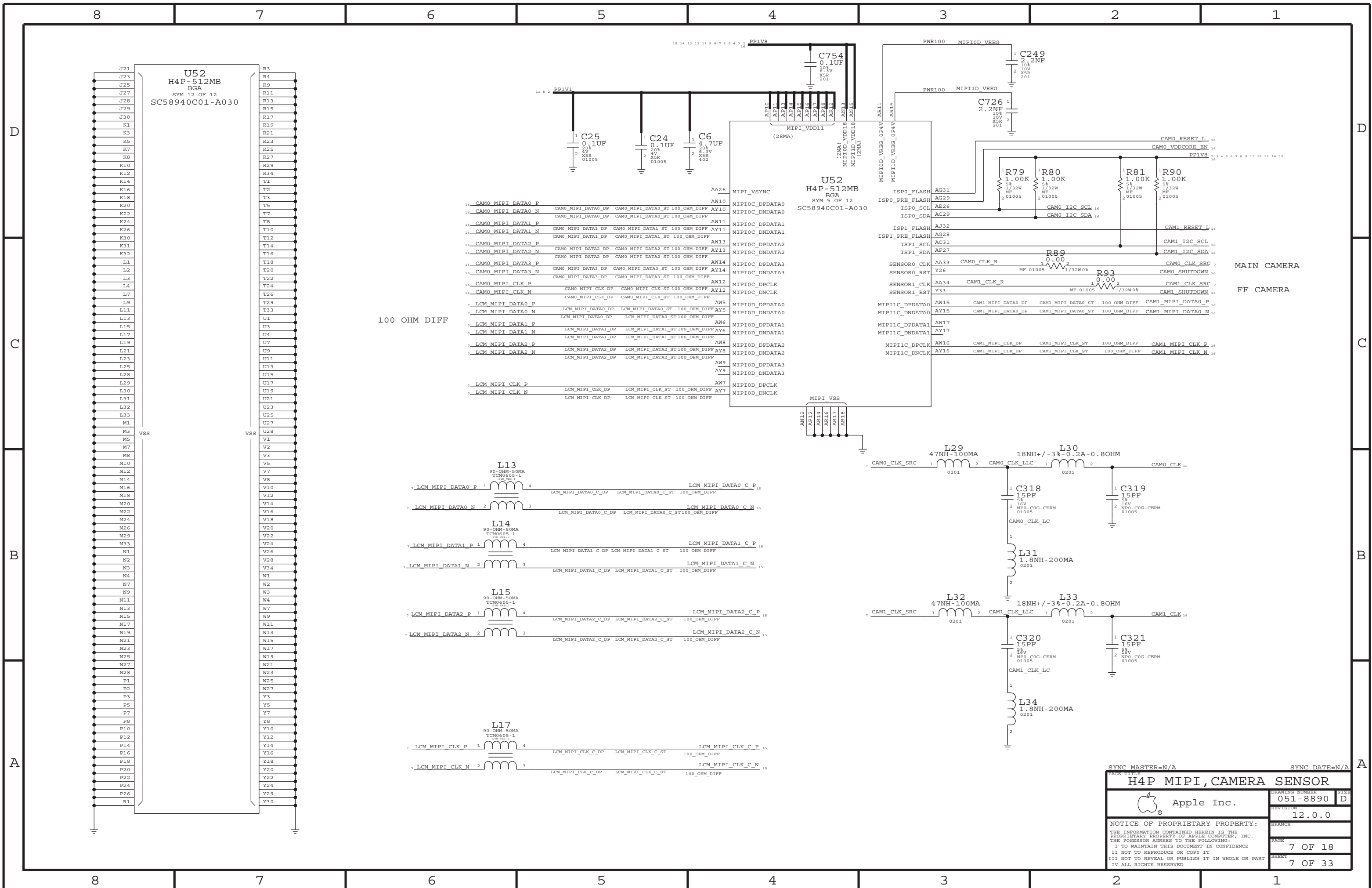
PPN10 = 0 OHM
 PPN15 = NOSTUFF

PPN10 = 0 OHM
 PPN15 = NOSTUFF

PPN10 = 0 OHM
 PPN15 = NOSTUFF

ASSUME 4CE/3.0V FOR RAW NAND

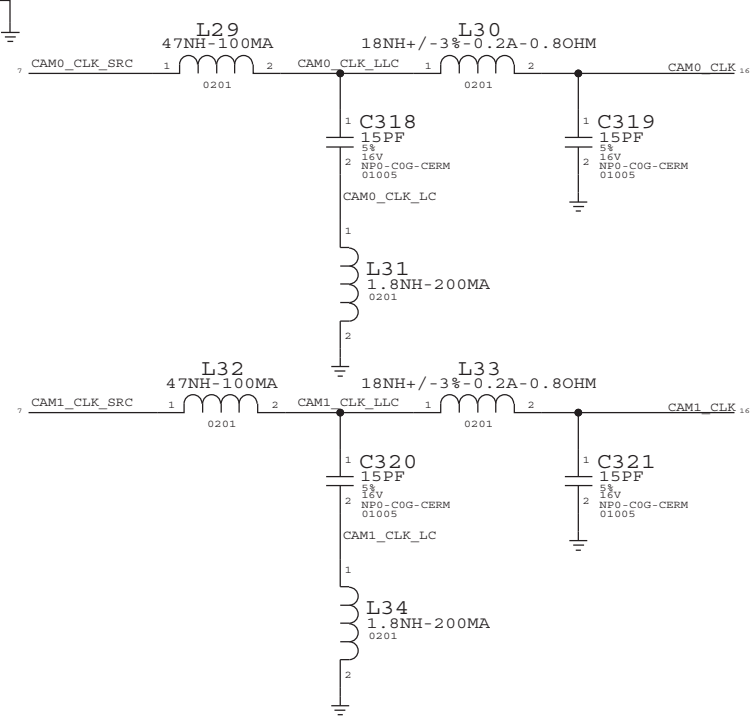
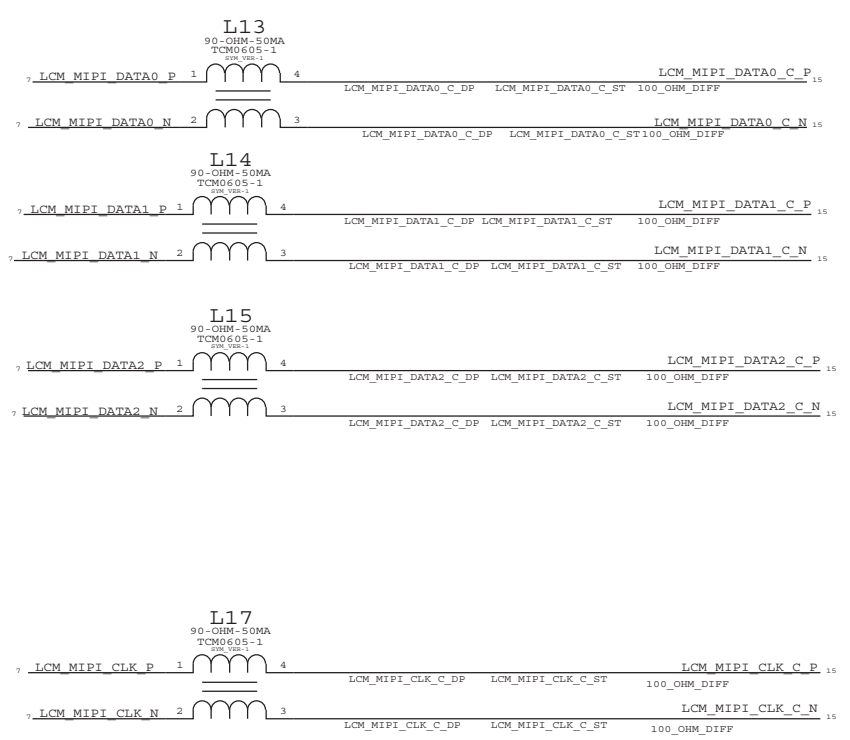
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H4 P NAND&GND, NAND			
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U52
H4P-512MB
BGA
SYM 12 OF 12
SC58940C01-A030

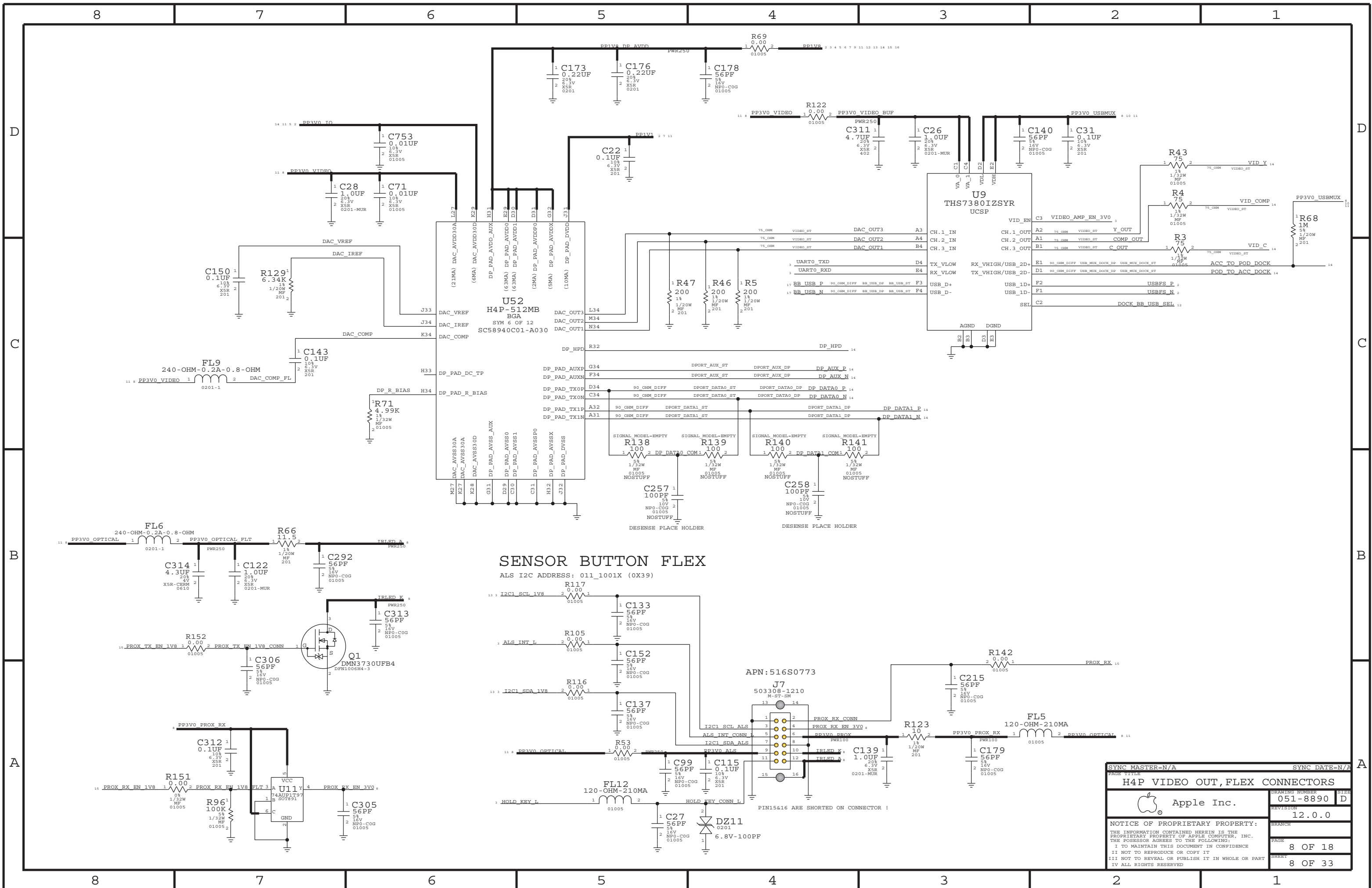
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AW10	MIPI0C_DPDATA0
AY10	MIPI0C_DNDATA0
AW11	MIPI0C_DPDATA1
AY11	MIPI0C_DNDATA1
AW13	MIPI0C_DPDATA2
AY13	MIPI0C_DNDATA2
AW14	MIPI0C_DPDATA3
AY14	MIPI0C_DNDATA3
AW12	MIPI0C_DPCLK
AY12	MIPI0C_DNCLK
AW5	MIPI0D_DPDATA0
AY5	MIPI0D_DNDATA0
AW6	MIPI0D_DPDATA1
AY6	MIPI0D_DNDATA1
AW8	MIPI0D_DPDATA2
AY8	MIPI0D_DNDATA2
AW9	MIPI0D_DPDATA3
AY9	MIPI0D_DNDATA3
AW7	MIPI0D_DPCLK
AY7	MIPI0D_DNCLK

100 OHM DIFF



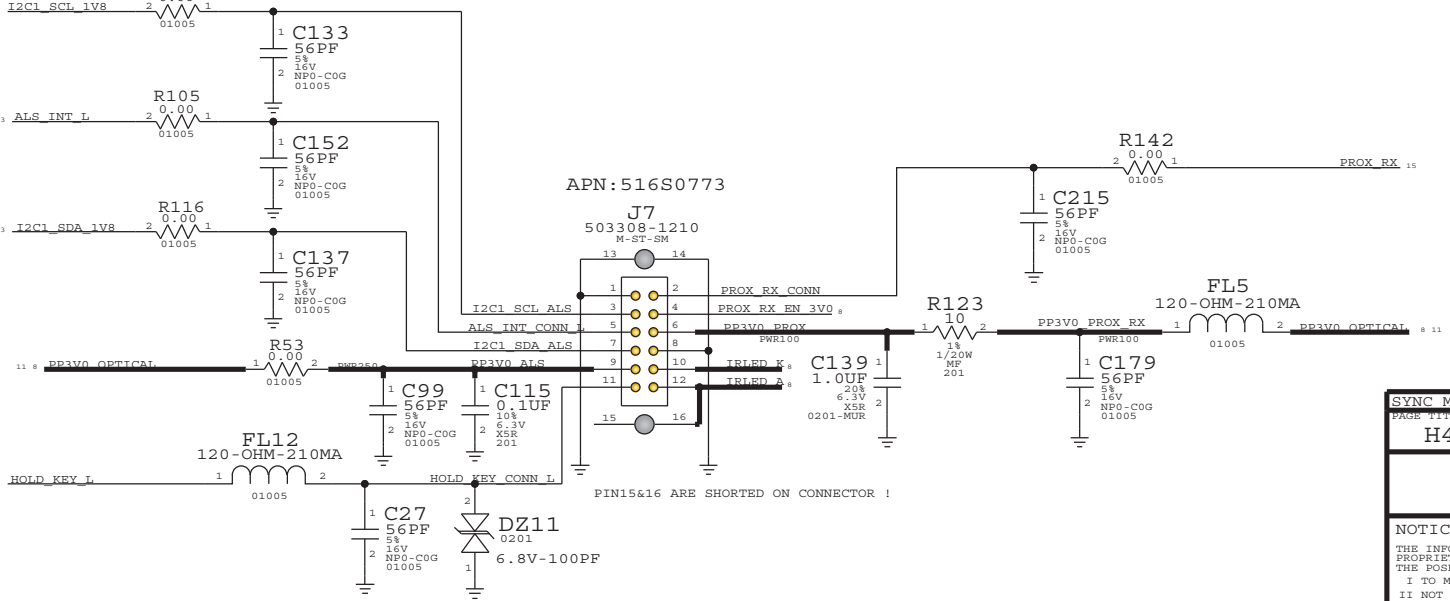
MAIN CAMERA
FF CAMERA

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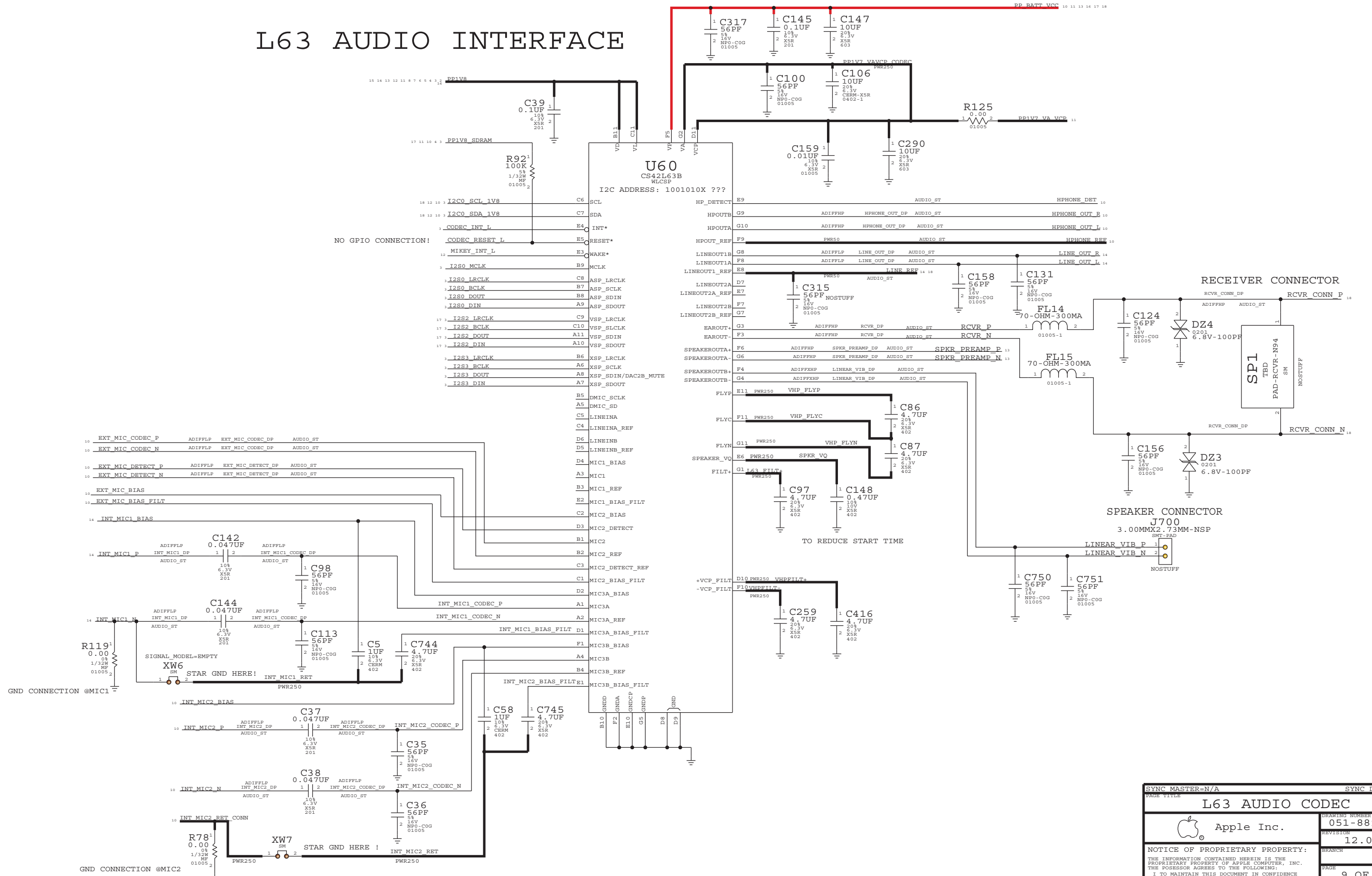
SENSOR BUTTON FLEX

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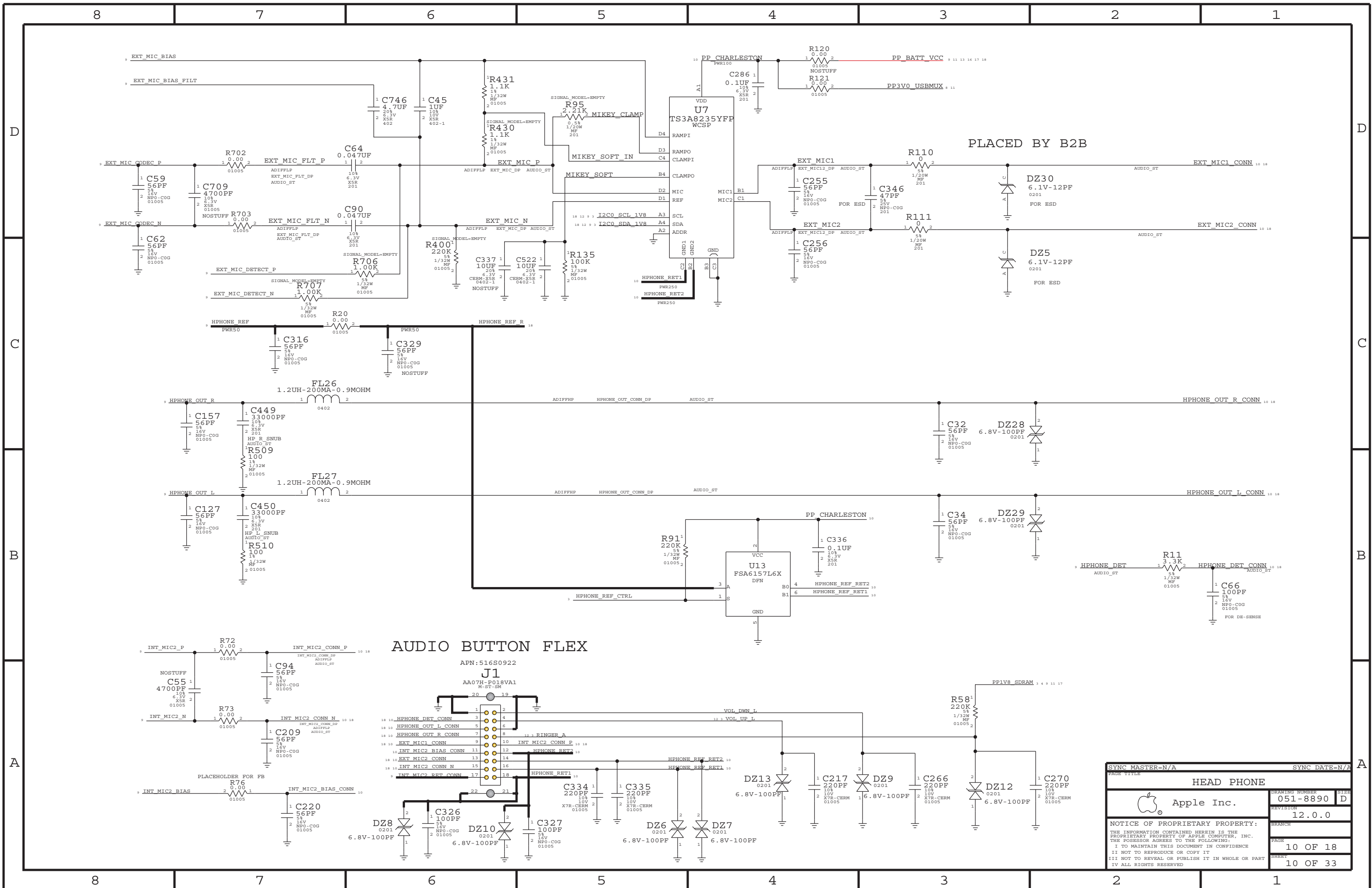


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H4P VIDEO OUT, FLEX CONNECTORS			
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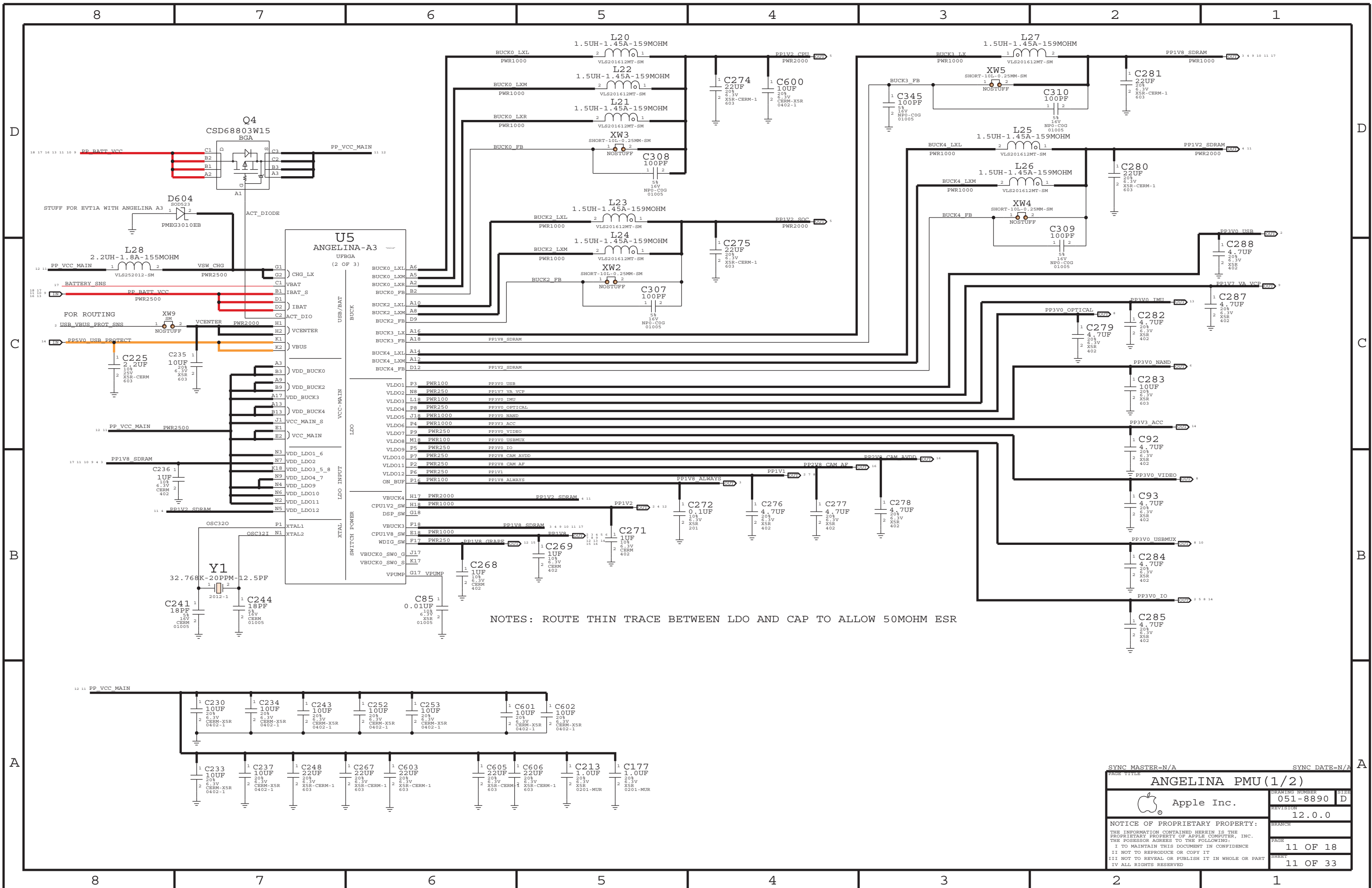
L63 AUDIO INTERFACE



PAGE TITLE		SYNC DATE=N/A	
L63 AUDIO CODEC			
Apple Inc.	DRAWING NUMBER	051-8890	SIZE D
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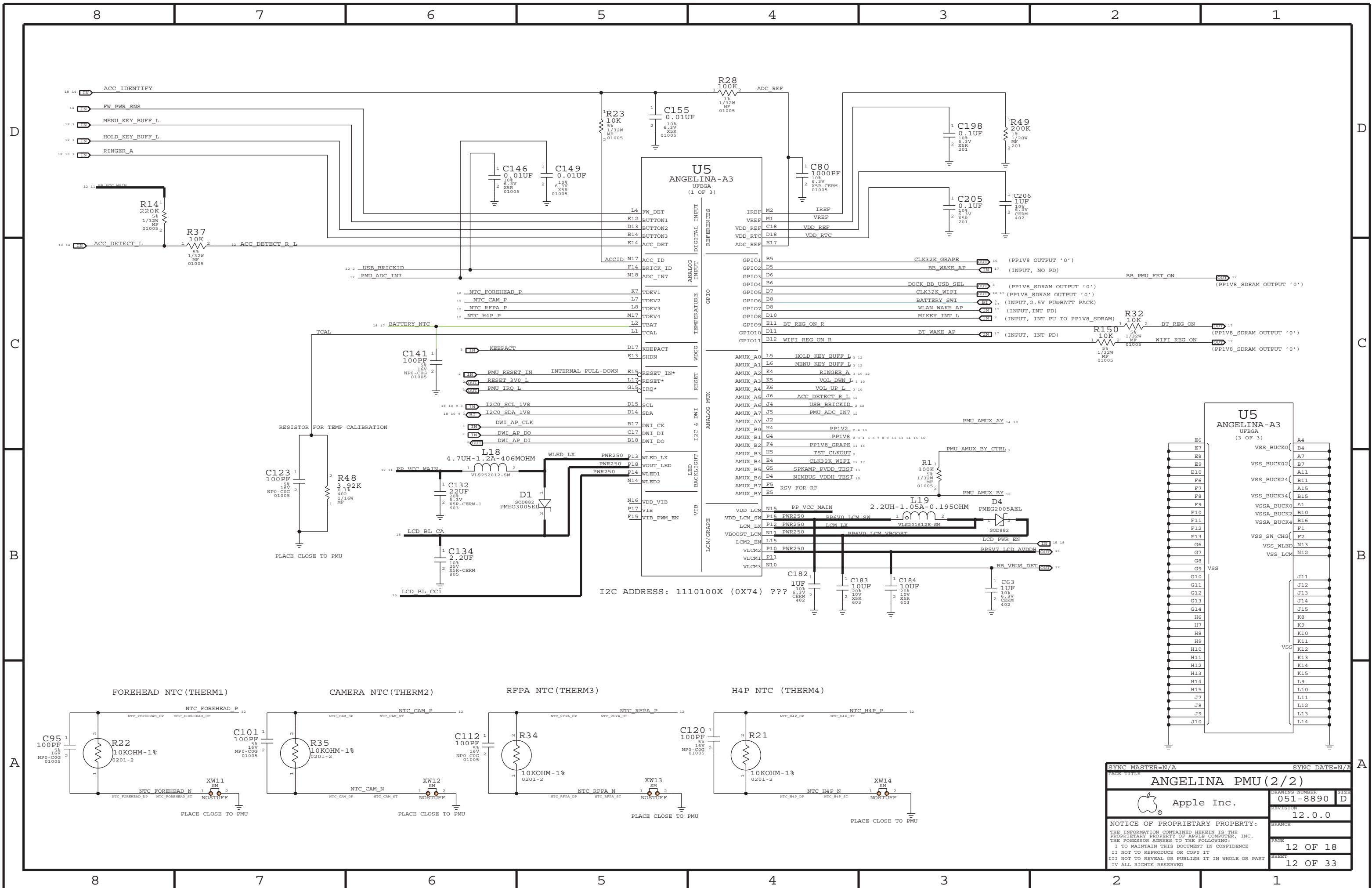


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SHEET		10 OF 33	



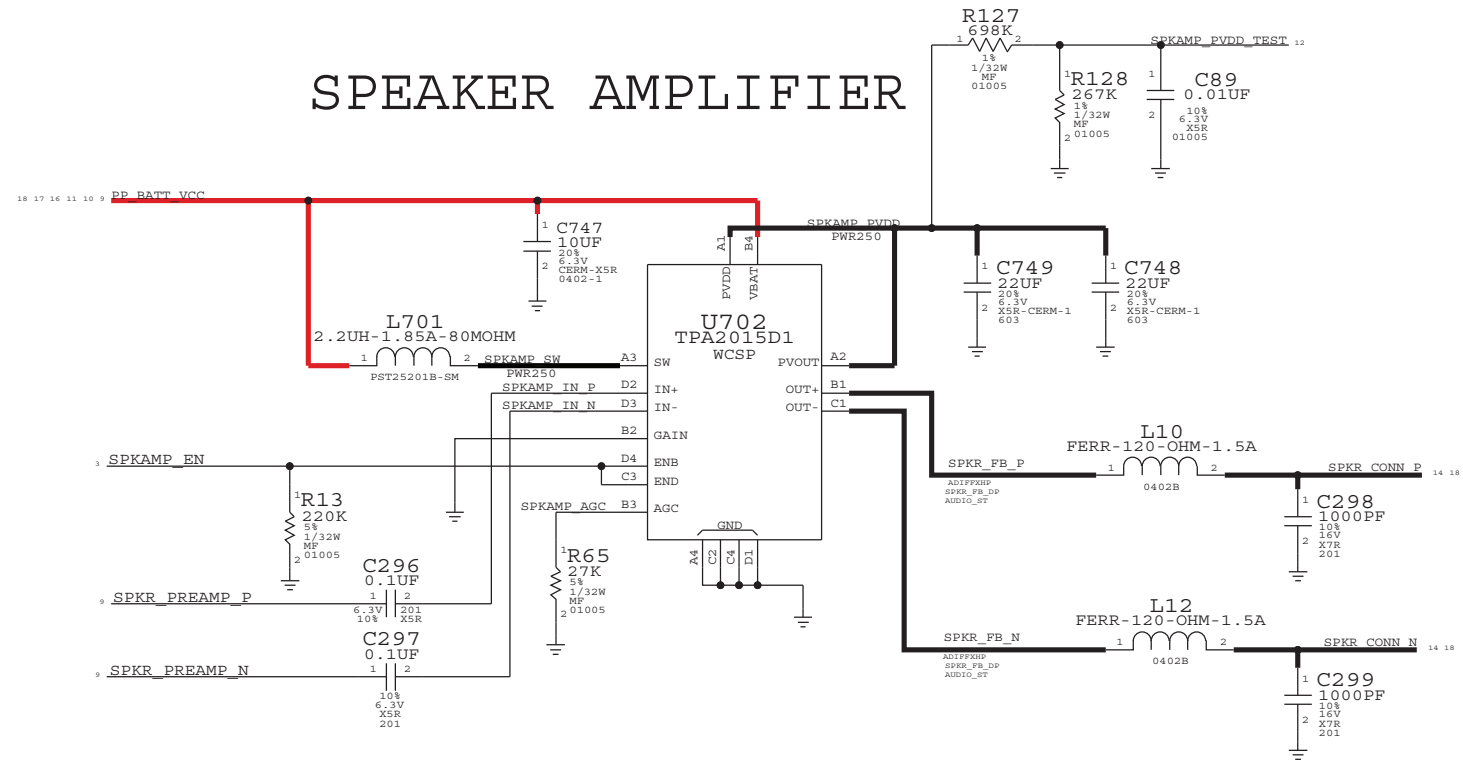
NOTES: ROUTE THIN TRACE BETWEEN LDO AND CAP TO ALLOW 50MOHM ESR

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ANGELINA PMU (1/2)			
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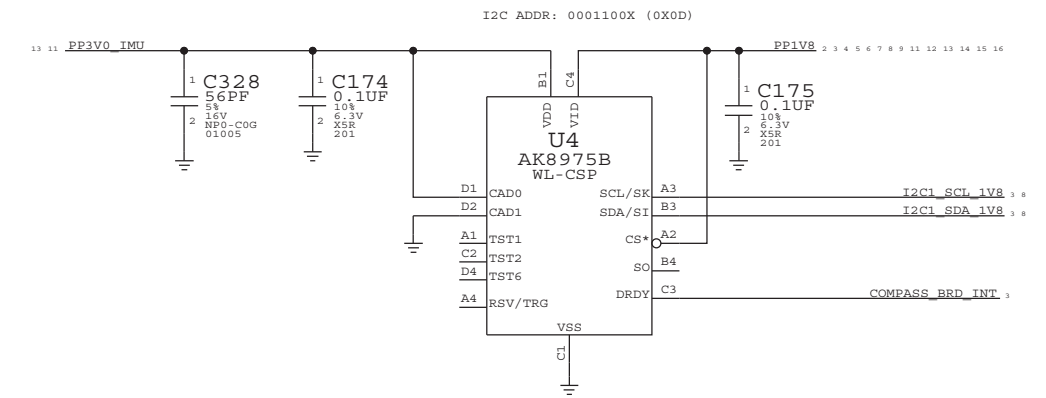


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ANGELINA PMU (2/2)			
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SPEAKER AMPLIFIER

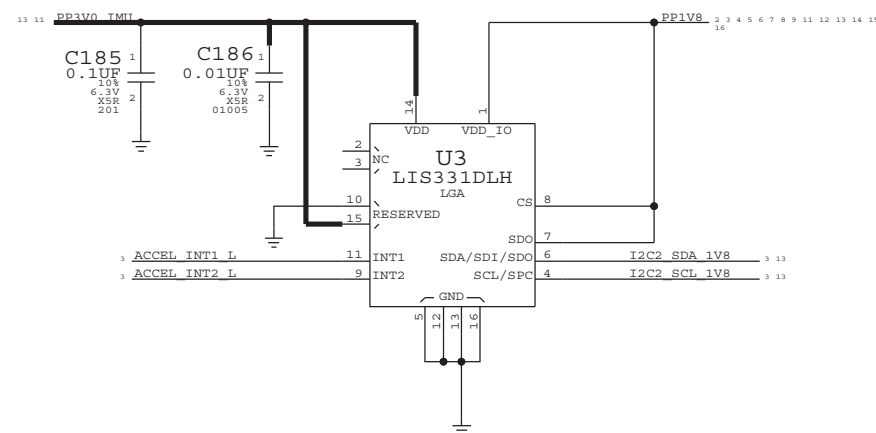


COMPASS OPTION1



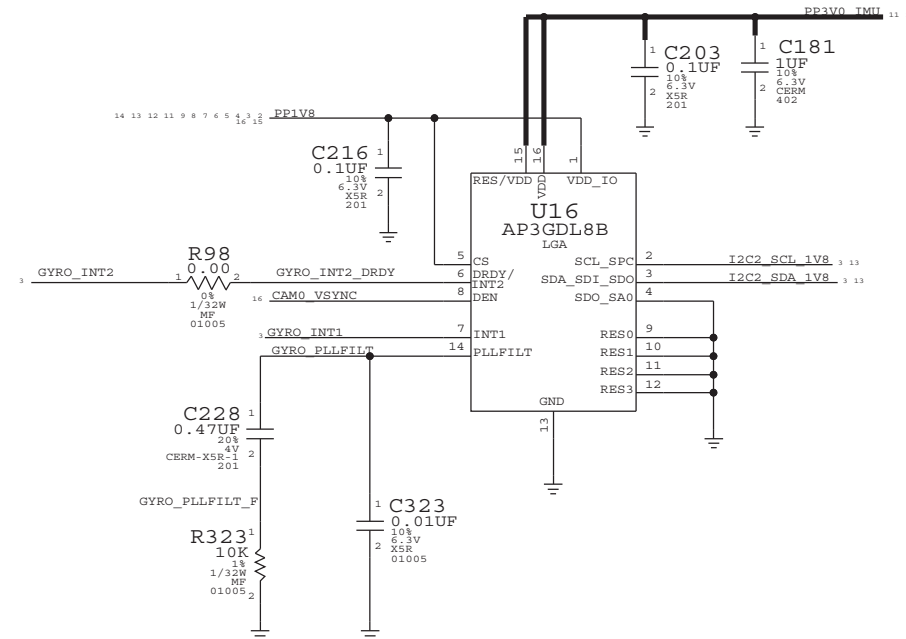
ACCELEROMETER

I2C ADDRESS: 0011101X (0X1D)

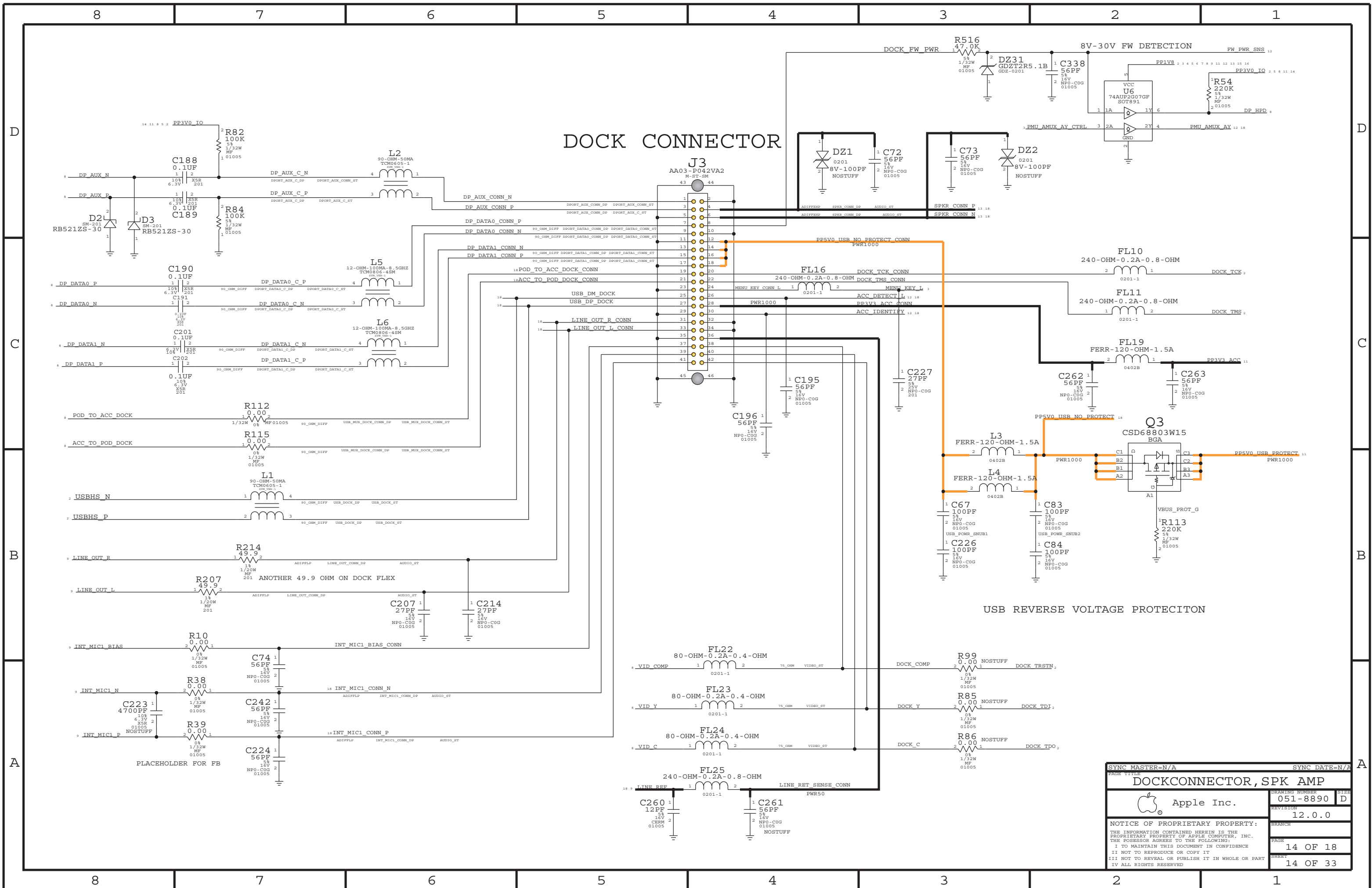


GYRO 8KHZ

I2C ADDRESS: 0XD0



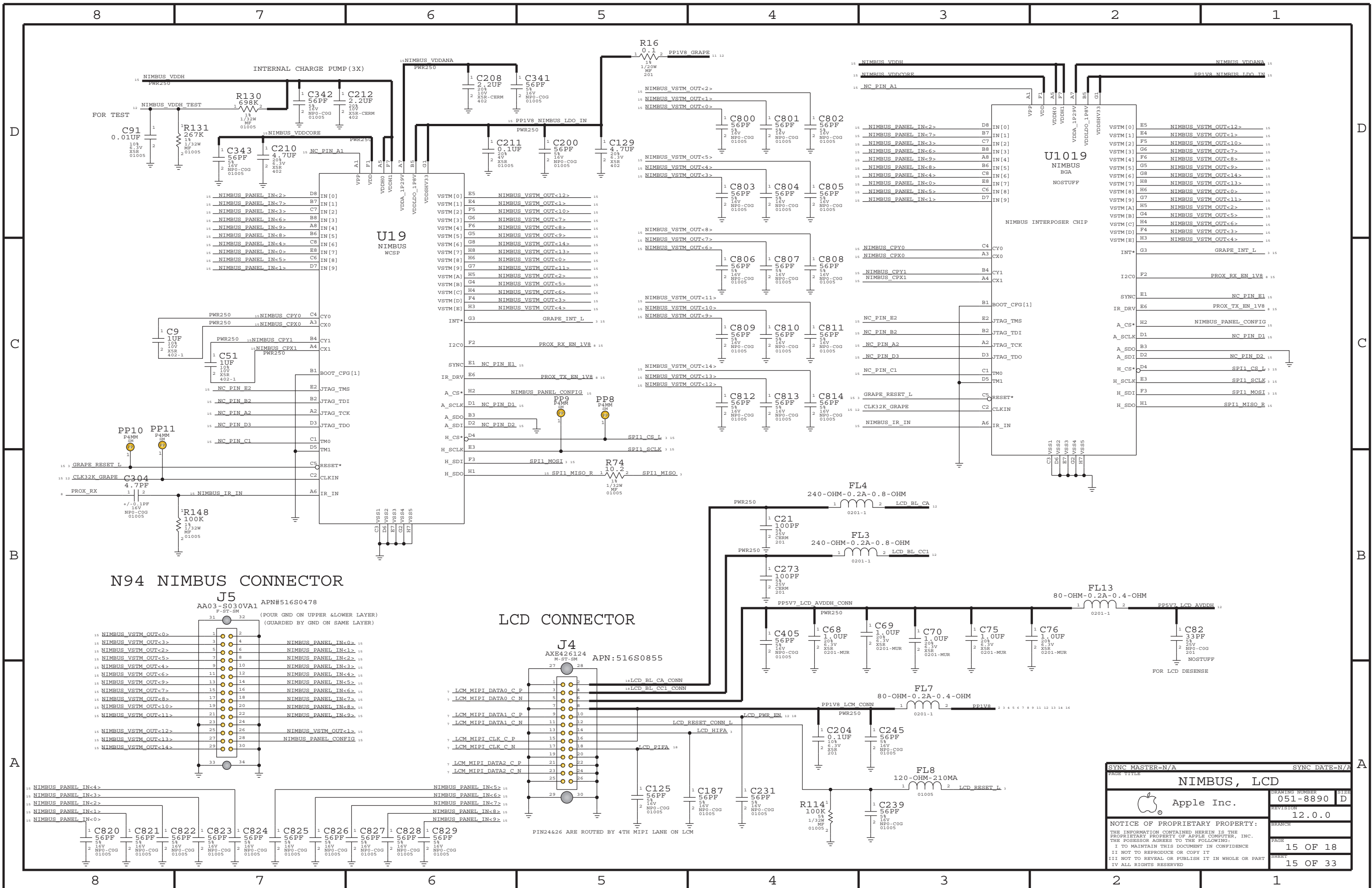
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ACCEL, GYRO, COMPASS, SPK AMP			
DRAWING NUMBER		051-8890	SIZE D
REVISION		12.0.0	
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13 OF 18		SHEET	
13 OF 33			



DOCK CONNECTOR

USB REVERSE VOLTAGE PROTECTITON

PAGE TITLE		SYNC DATE=N/A	
DOCKCONNECTOR, SPK AMP			
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		SHEET	14 OF 33



N94 NIMBUS CONNECTOR

J5
AA03-S030VA1 APN#516S0478

(POUR GND ON UPPER & LOWER LAYER)
(GUARDED BY GND ON SAME LAYER)

LCD CONNECTOR

J4
AXE426124 APN:516S0855

PIN24&26 ARE ROUTED BY 4TH MIPI LANE ON LCM

NIMBUS, LCD



Apple Inc.

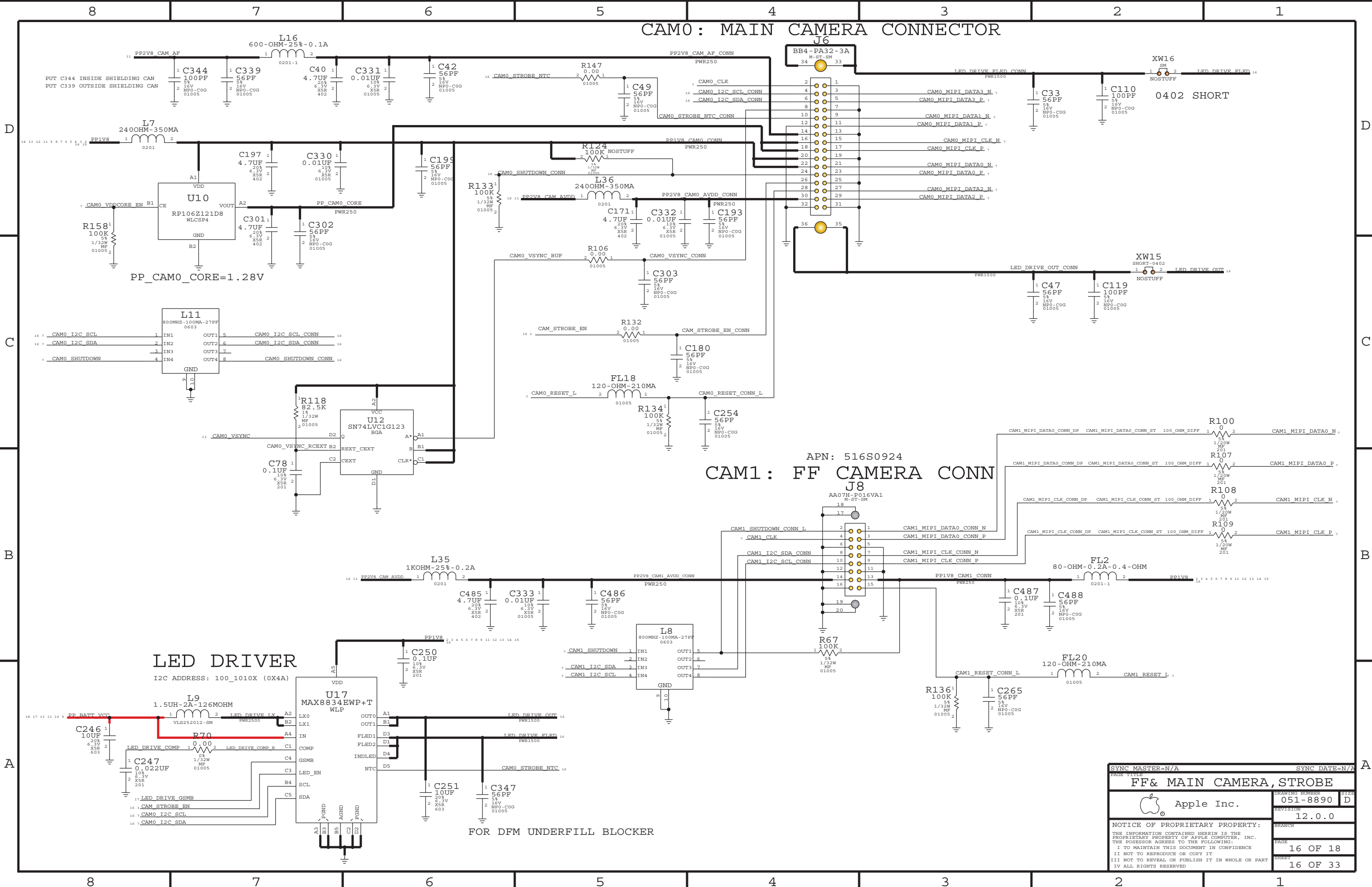
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REVISION: 12.0.0

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BRANCH: 15 OF 18
PAGE: 15 OF 33

SYNC MASTER=N/A SYNC DATE=N/A

CAM0: MAIN CAMERA CONNECTOR



CAM1: FF CAMERA CONN

APN: 516S0924

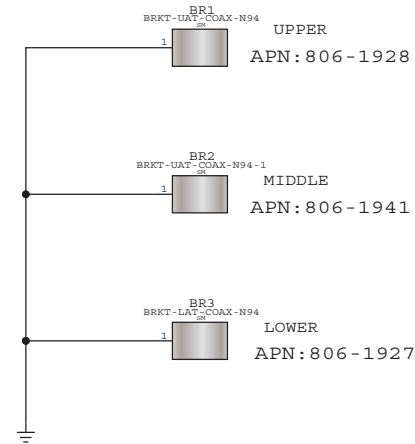
LED DRIVER

I2C ADDRESS: 100_1010X (0X4A)

FOR DFM UNDERFILL BLOCKER

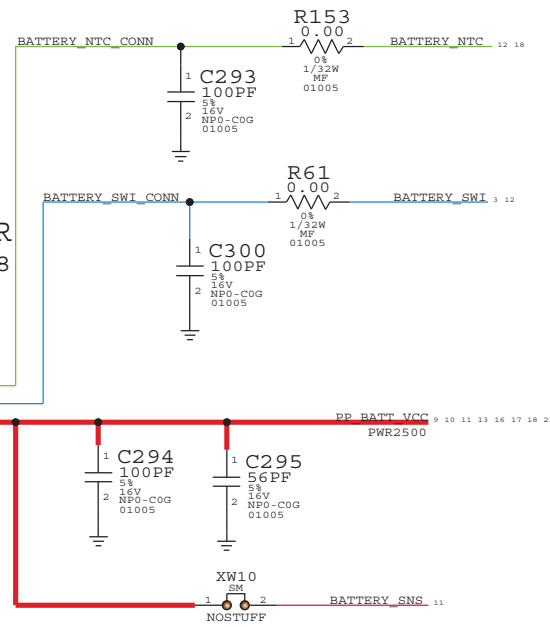
PAGE TITLE		SYNC DATE=N/A	
FF & MAIN CAMERA, STROBE			
Apple Inc.		DRAWING NUMBER	SIZE
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		12.0.0	
		PAGE	
		16 OF 18	
		SHEET	
		16 OF 33	

STRAIN RELIEF BRACKET



BATTERY CONNECTOR

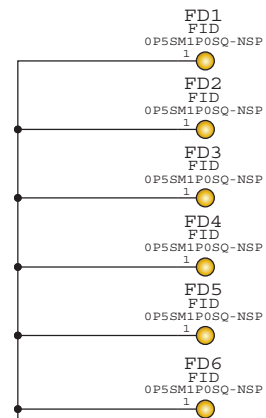
APN: 516S0908
J9
1.8 PITCH
F-ST-SM



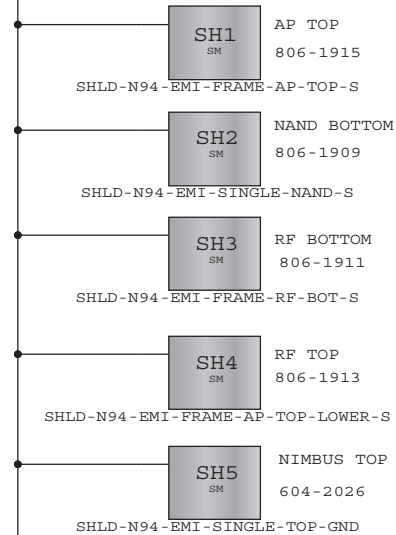
AP/RADIO INTERFACE

REF	VALUE	MAKE BASE=TRUE	NAME
23 18 17 16 13 11 10 9	PP_BATT_VCC	MAKE BASE=TRUE	BATT_VCC
23 3	RADIO_ON_L	MAKE BASE=TRUE	RADIO_ON_N
20 3	BB_RESET_DET_L	MAKE BASE=TRUE	RESET_DET_N
23 12	BB_PMT_FET_ON	MAKE BASE=TRUE	FET_ON (ANGELINA)
23 3	RESET_BB_PMT_L	MAKE BASE=TRUE	RESET_PMT_N (AP - H4P)
20 3	BB_RESET_L	MAKE BASE=TRUE	BB_RST_N
20 11	BB_WAKE_AP	MAKE BASE=TRUE	BB_WAKE_AP
25 18 2	RESET_IV8_L	MAKE BASE=TRUE	RF_RESET_N
20 14	LED_DRIVE_GSM	MAKE BASE=TRUE	GSM_TXBURST_IND
20 3	SPI2_MRDY	MAKE BASE=TRUE	IPC_MRDY
20 1	IPC_SRDY	MAKE BASE=TRUE	IPC_SRDY
20 1	IPC_GPIO4	MAKE BASE=TRUE	IPC_GPIO4
20 12	BB_VBUS_DET	MAKE BASE=TRUE	BB_USB_VBUS
20 4	BB_USB_N	MAKE BASE=TRUE	BB_USB_DN
20 4	BB_USB_P	MAKE BASE=TRUE	BB_USB_DP
20 3	UART1_RTS_L	MAKE BASE=TRUE	BB_UART_CTS_N
20 3	UART1_CTS_L	MAKE BASE=TRUE	BB_UART_RTS_N
20 3	UART1_TXD	MAKE BASE=TRUE	BB_UART_RXD
20 3	UART1_RXD	MAKE BASE=TRUE	BB_UART_TXD
20 3	I2S1_BCLK	MAKE BASE=TRUE	BB_I2S_CLK
20 3	I2S1_DOUT	MAKE BASE=TRUE	BB_I2S_RXD
20 3	I2S1_DIN	MAKE BASE=TRUE	BB_I2S_TXD
20 3	I2S1_LRCLK	MAKE BASE=TRUE	BB_I2S_WS
32 11 10 9 4 3	PP1V8_SDRAM	MAKE BASE=TRUE	WL_BT_VDDIO
32 12	BT_REG_ON	MAKE BASE=TRUE	BT_REG_ON
32 12	WIFI_REG_ON	MAKE BASE=TRUE	WLAN_REG_ON
32 12	WLAN_SDIO_CLK	MAKE BASE=TRUE	WLAN_SDIO_CLK
32 1	WLAN_SDIO_CMD	MAKE BASE=TRUE	WLAN_SDIO_CMD
32 1	WLAN_SDIO_DATA<3..0>	MAKE BASE=TRUE	WLAN_SDIO_DATA<3..0>
32 12	WLAN_WAKE_AP	MAKE BASE=TRUE	HOST_WAKE_WLAN
32 3	BT_WAKE	MAKE BASE=TRUE	BT_WAKE
32 3	CLK32K_WIFI	MAKE BASE=TRUE	CLK32K_AP
32 3	BT_RESET_L	MAKE BASE=TRUE	BT_RESET_N
32 12	BT_WAKE_AP	MAKE BASE=TRUE	HOST_WAKE_BT
32 3	UART3_RTS_L	MAKE BASE=TRUE	BT_UART_CTS_N
32 3	UART3_CTS_L	MAKE BASE=TRUE	BT_UART_RTS_N
32 3	UART3_TXD	MAKE BASE=TRUE	BT_UART_RXD
32 3	UART3_RXD	MAKE BASE=TRUE	BT_UART_TXD
32 9 1	I2S2_BCLK	MAKE BASE=TRUE	BT_PCM_CLK
32 9 1	I2S2_DOUT	MAKE BASE=TRUE	BT_PCM_IN
32 9 1	I2S2_DIN	MAKE BASE=TRUE	BT_PCM_OUT
32 9 1	I2S2_LRCLK	MAKE BASE=TRUE	BT_PCM_SYNC
20 2	HSIC1_DATA	50_OHM HSIC_ST	HSIC_BB_DATA
20 2	HSIC1_STB	50_OHM HSIC_ST	HSIC_BB_STROBE
20 3	HOST_BB_HSIC_RDY	MAKE BASE=TRUE	HOST_BB_HSIC_RDY
20 3	HOST_WLAN_HSIC_RDY	MAKE BASE=TRUE	HOST_WLAN_HSIC_RDY
20 3	BB_HSIC_RDY	MAKE BASE=TRUE	BB_HSIC_RDY
32 2	HSIC2_DATA	50_OHM HSIC_ST	HSIC_WLAN_DATA
32 2	HSIC2_STB	50_OHM HSIC_ST	HSIC_WLAN_STROBE
20 3	BB_EMERGENCY_DWLD_L	MAKE BASE=TRUE	BB_EMERGENCY_DWLD
32 3	WLAN_HSIC_RDY	MAKE BASE=TRUE	WLAN_HSIC_RDY

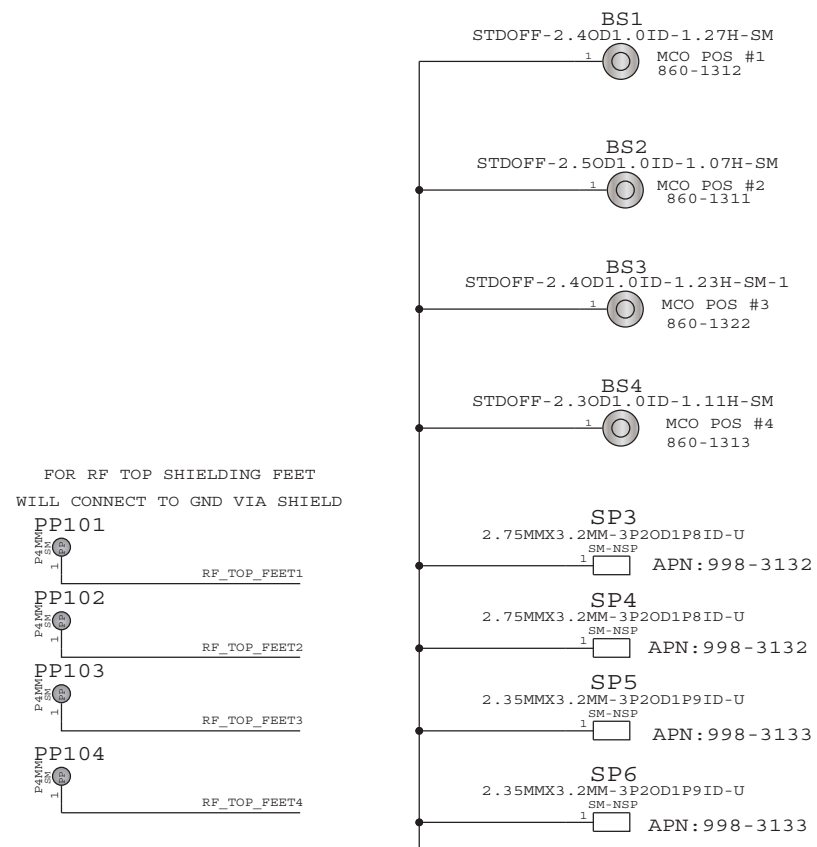
FIDUCIALS



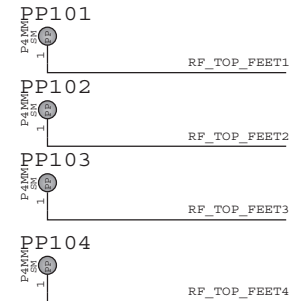
SHIELDS



STANDOFFS



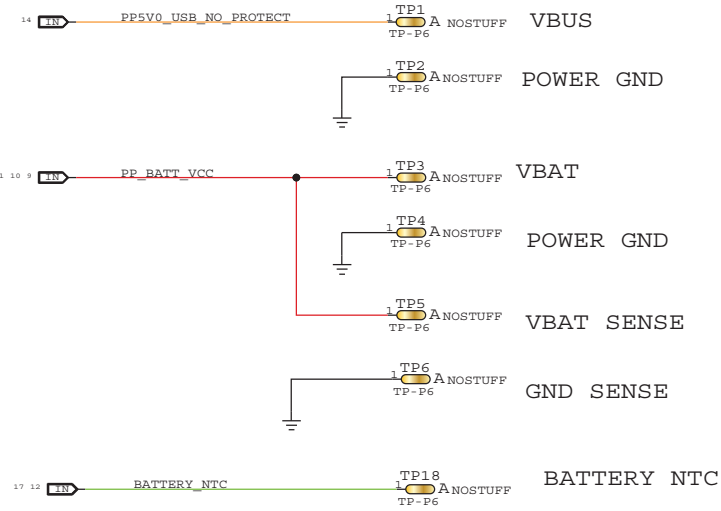
FOR RF TOP SHIELDING FEET
WILL CONNECT TO GND VIA SHIELD



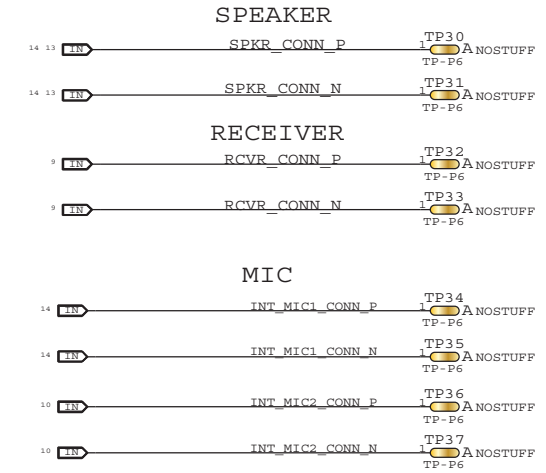
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RF INT, SHIELD, STNDOFFS			
Apple Inc.	DRAWING NUMBER	051-8890	SIZE
	REVISION	12.0.0	
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TEST POINTS

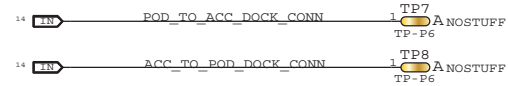
POWER



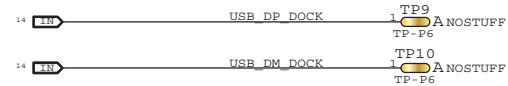
AUDIO



UART



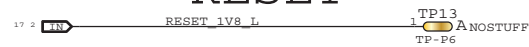
USB



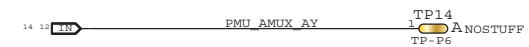
DFU



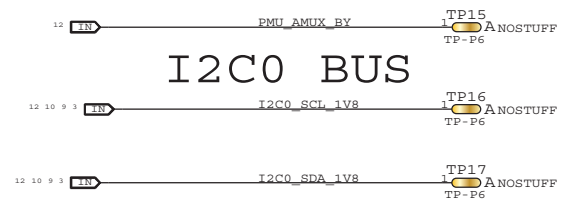
RESET



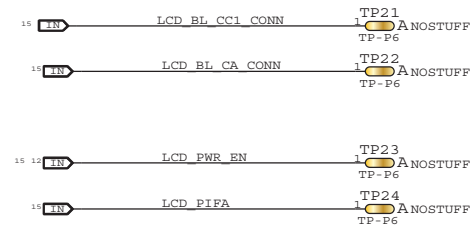
SUPER TP



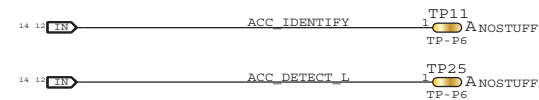
I2C0 BUS



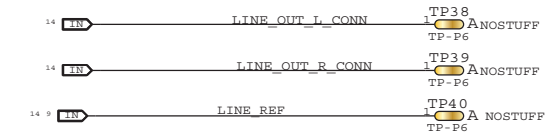
GRAPE/LCM



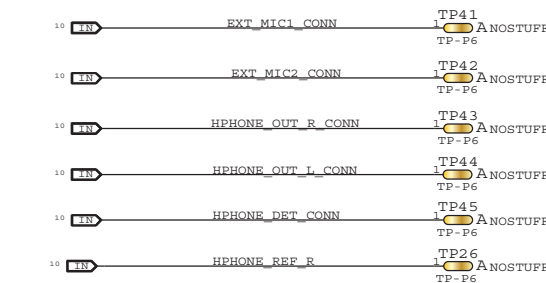
ACCESSORY



LINE OUT



HEADPHONE



SYNC MASTER=N/A		SYNC DATE=N/A	
TEST POINTS			
		DRAWING NUMBER	051-8890
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
12	0001170763	ENGINEERING RELEASED		2011-07-05


N94 RADIO_MLB_V3 SUBDESIGN

RADIO - 07/05/2011: SUBDESIGN

THIS PAGE	CONTENTS
02	BASEBAND
03	BASEBAND MEMORY
04	BASEBAND POWER
05	POWER1: CONTROL
06	POWER2: DIGITAL, ANALOG, RF
07	AP INTERFACE AND DEBUG CONNECTOR
08	RF TRANSCEIVER - RX AND TX
09	RF TRANSCEIVER - POWER DECOUPLING
10	RF TRANSCEIVER AND ASM
11	MMPA AND PA DC/DC CONVERTER
12	B2 AND B5 PADS
13	DIVERSITY AND EXTERNAL GPS LNA
14	WLAN/BT/FM
15	DIVERSITY ANTENNA SWITCH AND SIM

SCH #: 951-1604

BASED ON RADIO_MLB_EVT2_RFPE

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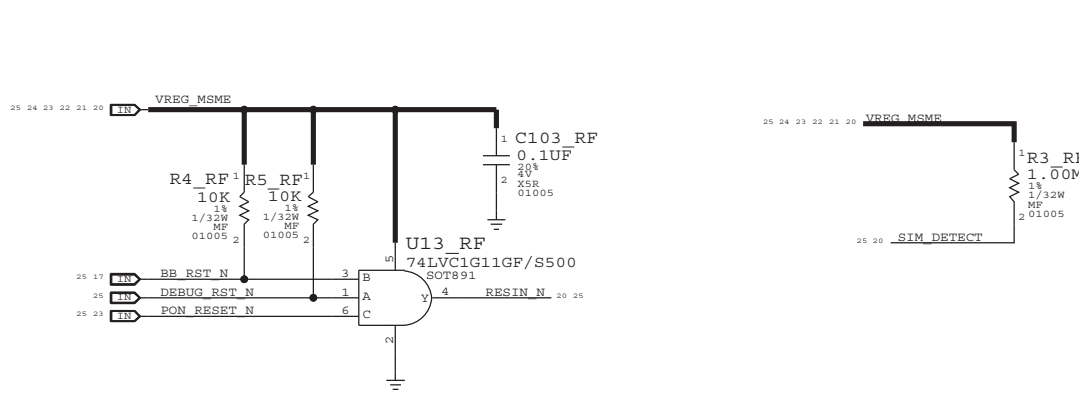
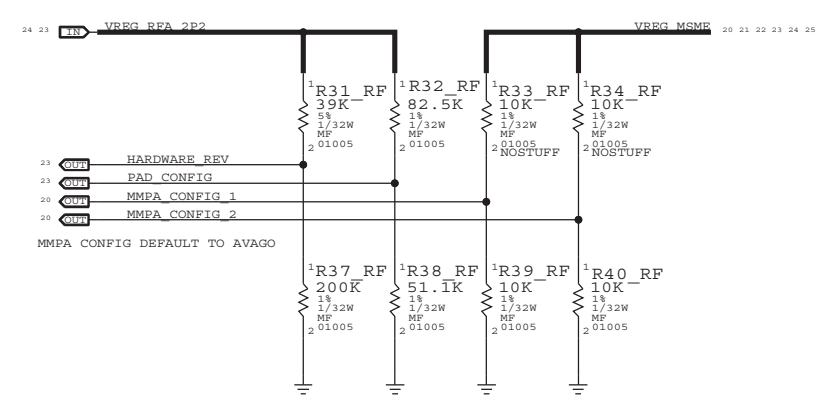
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BASEBAND

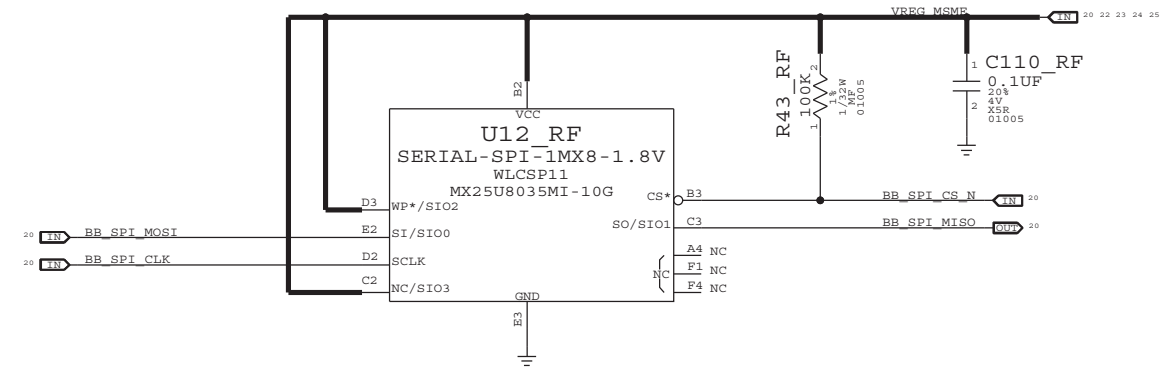
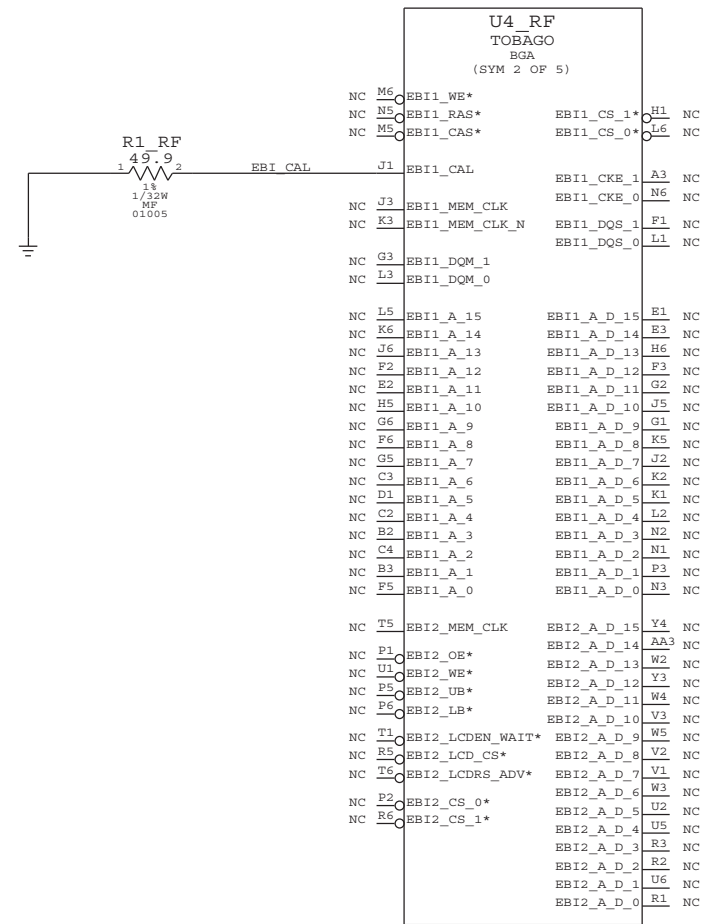
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DEFAULT TO DVT - AVAGO MMPA; TQNT B2; SKWS B5



PAGE TITLE		
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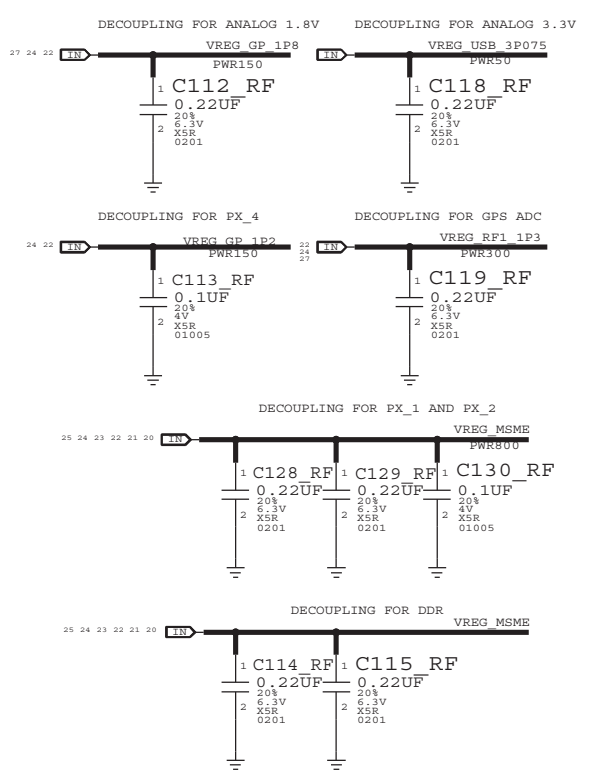
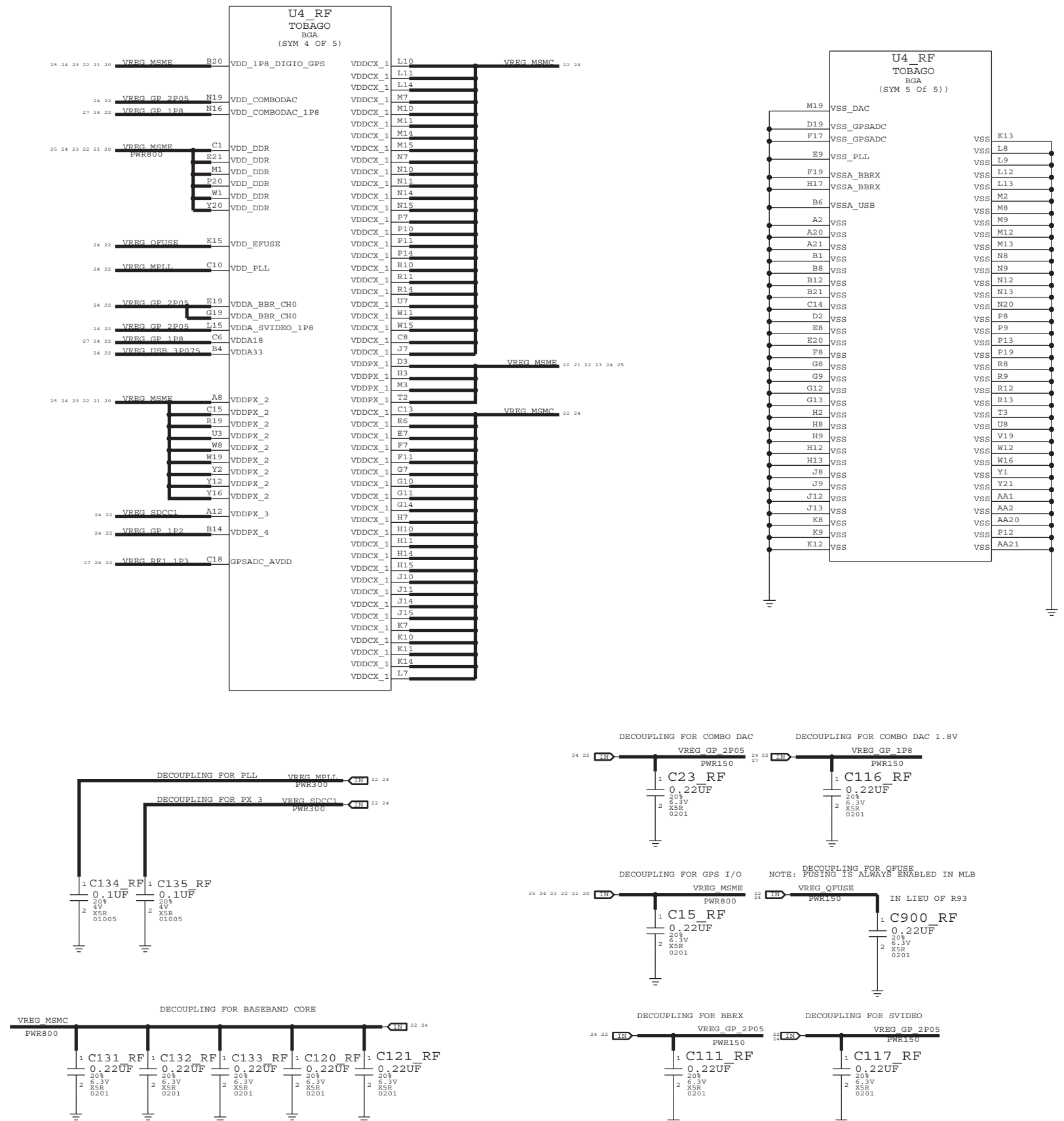


PAGE TITLE BASEBAND MEMORY		
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		SHEET 21 OF 33

8 7 6 5 4 3 2 1

D C B A

D C B A

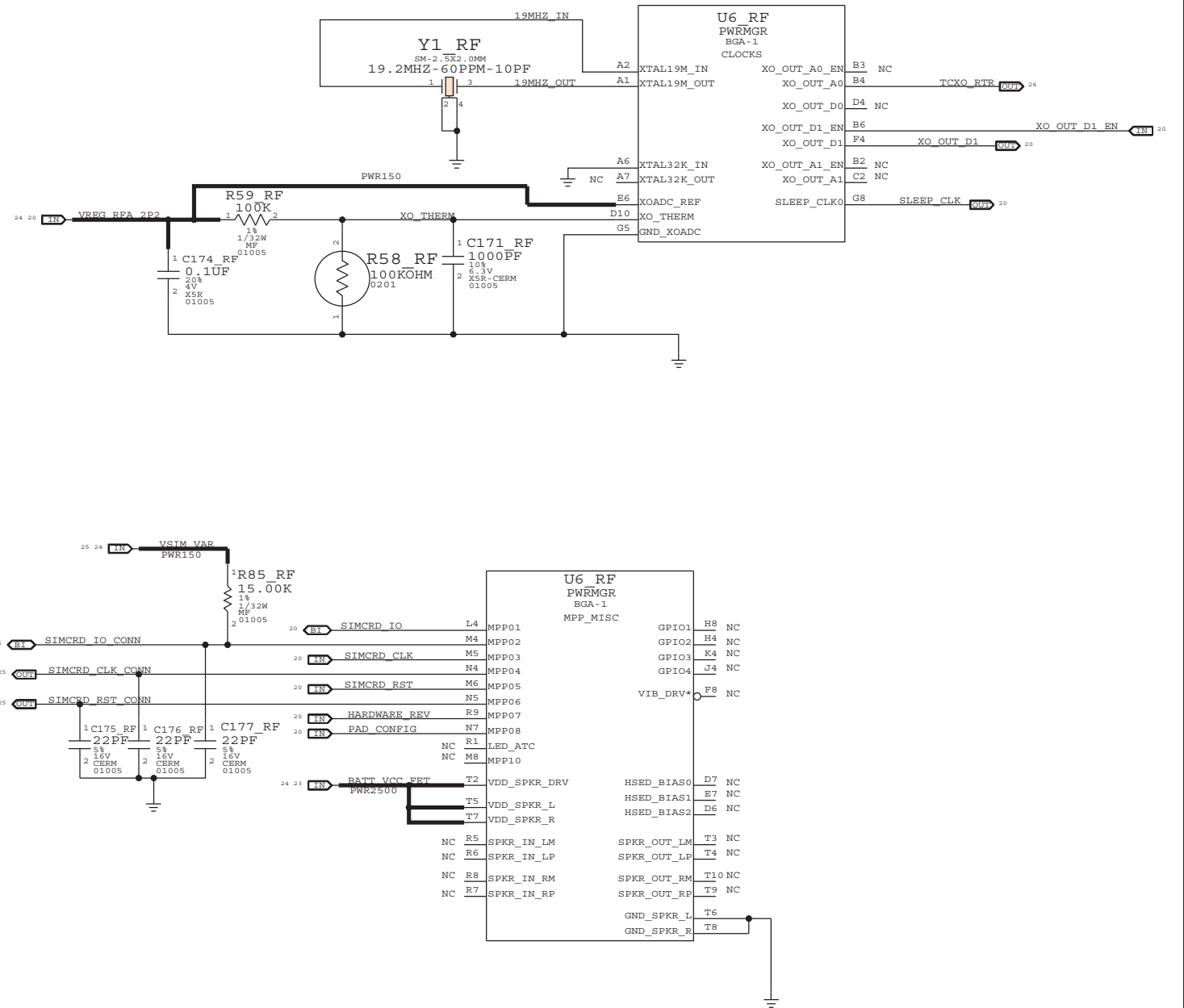
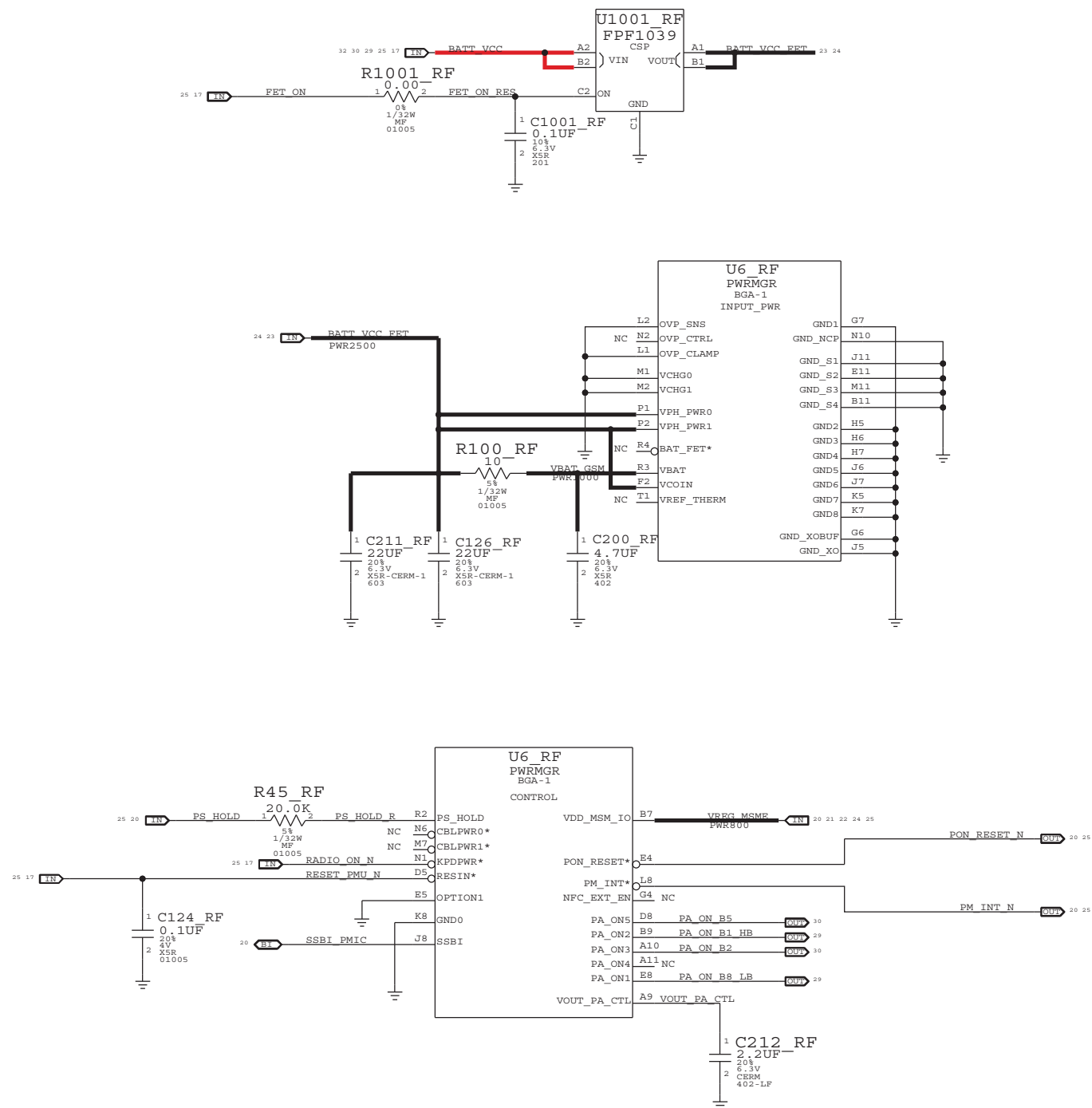


<p>BASEBAND POWER/DECOUPLING</p> Apple Inc.		<p>DRAWING NUMBER 051-8890</p> <p>REVISION 12.0.0</p> <p>BRANCH</p>	<p>SIZE D</p>
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8 7 6 5 4 3 2 1

BASEBAND PMU

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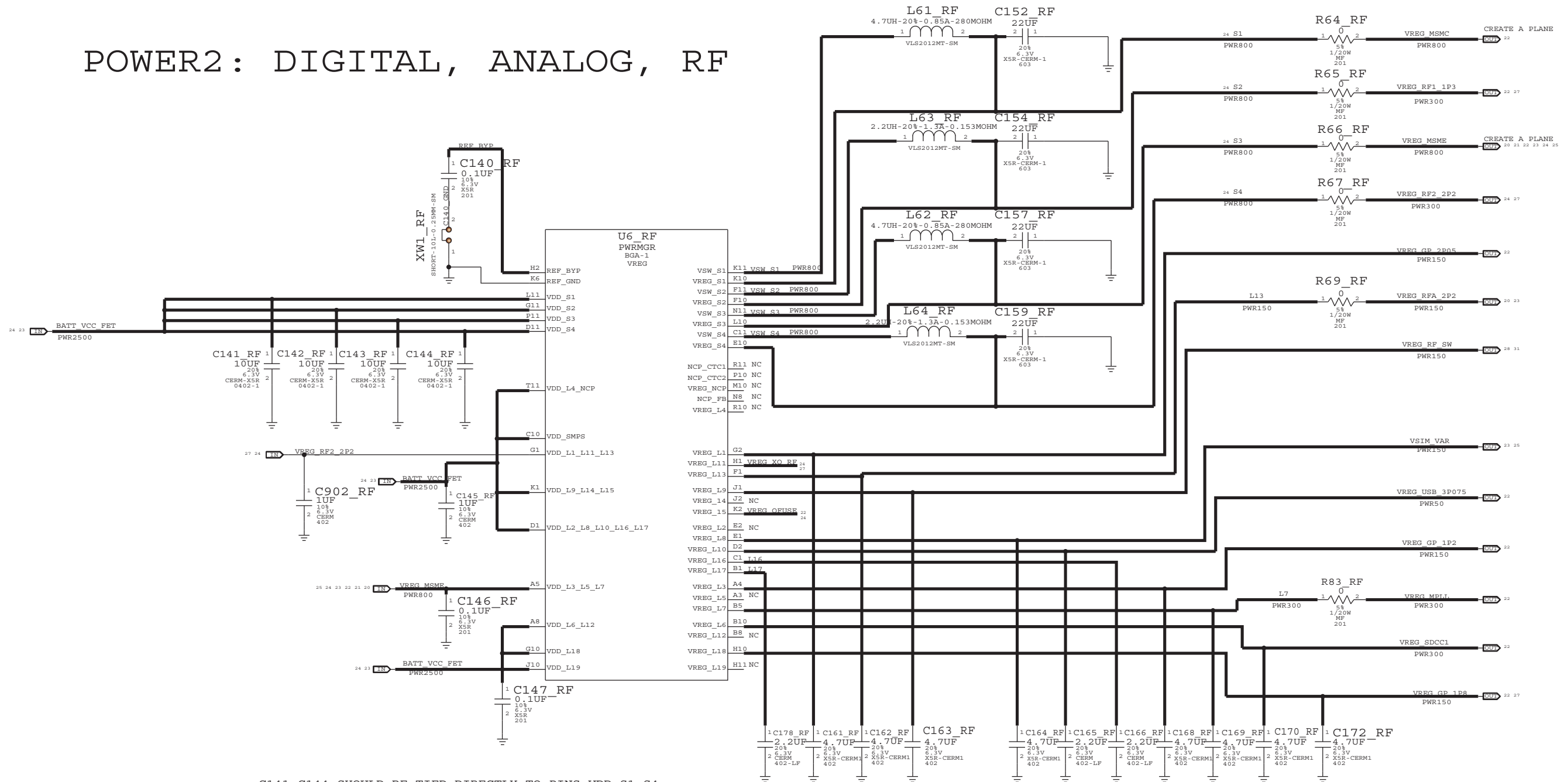


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BASEBAND PMU		
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BRANCH	PAGE	SHEET
	5 OF 15	23 OF 33

BASEBAND PMU CONT.

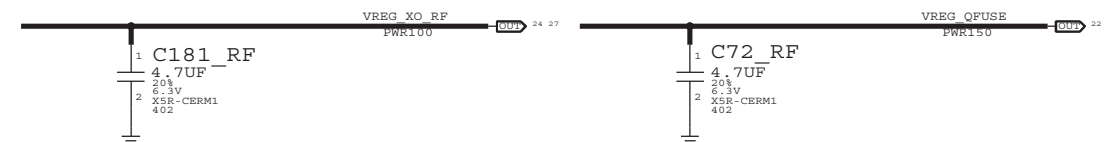
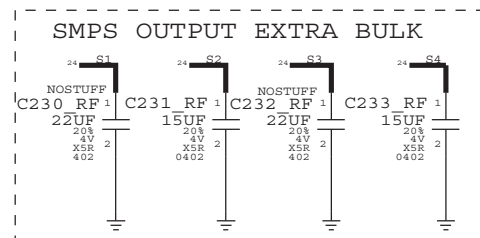
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POWER2: DIGITAL, ANALOG, RF



C141-C144 SHOULD BE TIED DIRECTLY TO PINS VDD_S1-S4

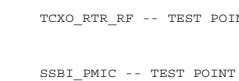
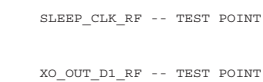
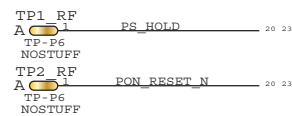
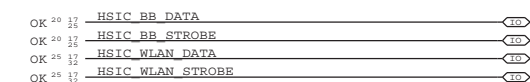
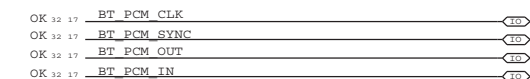
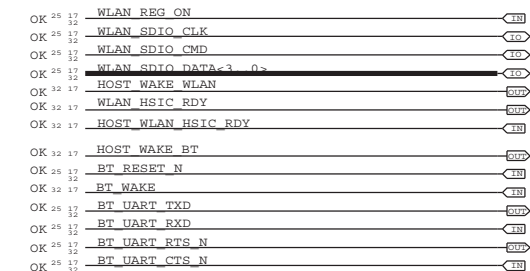
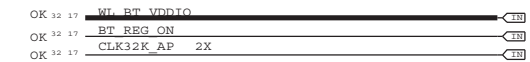
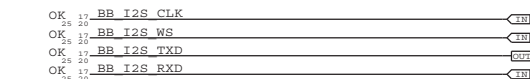
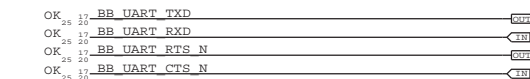
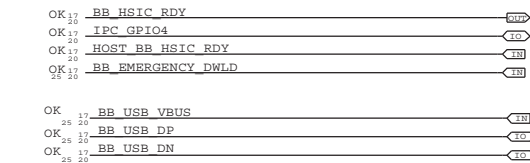
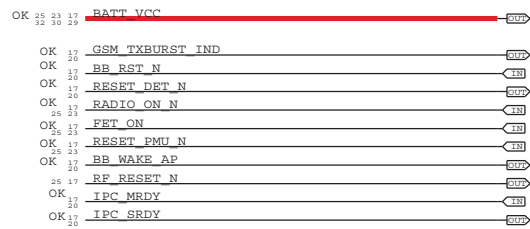
L16 AND L17 DECOUPLED PER EUREKA'S RECOMMENDATION



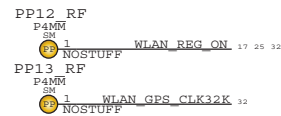
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DEBUG CONNECTOR

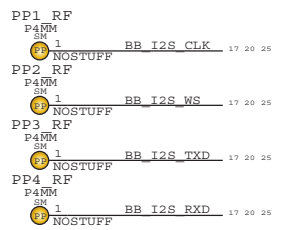
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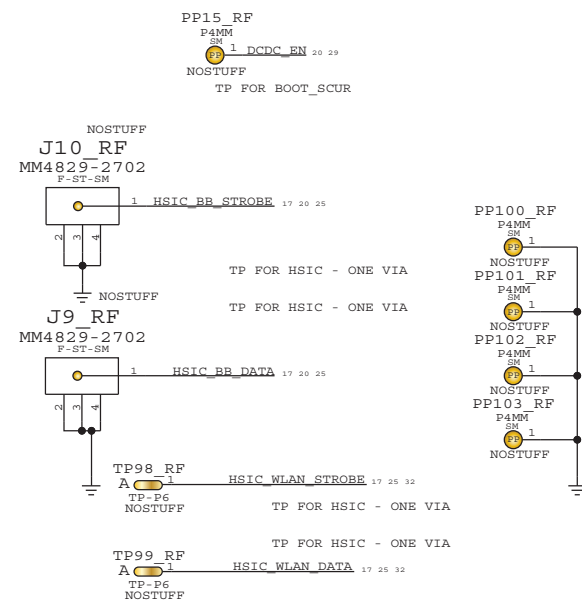
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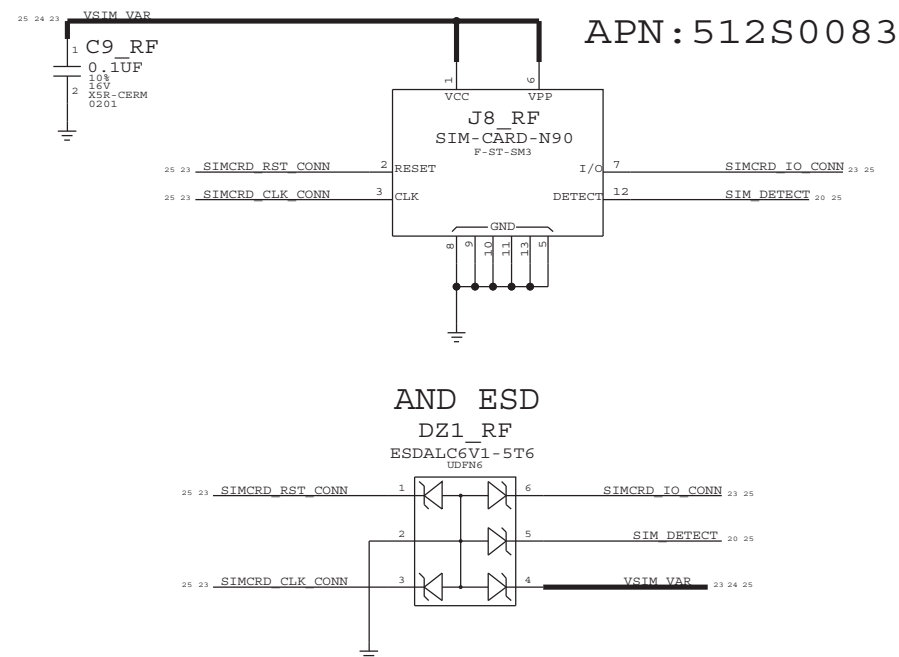
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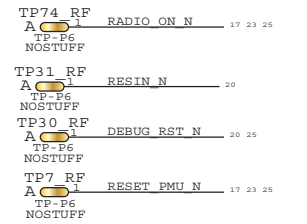
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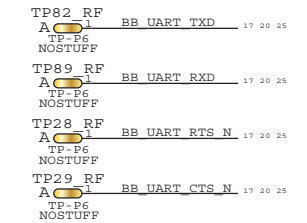
SIM CARD CONNECTOR



CONTROL

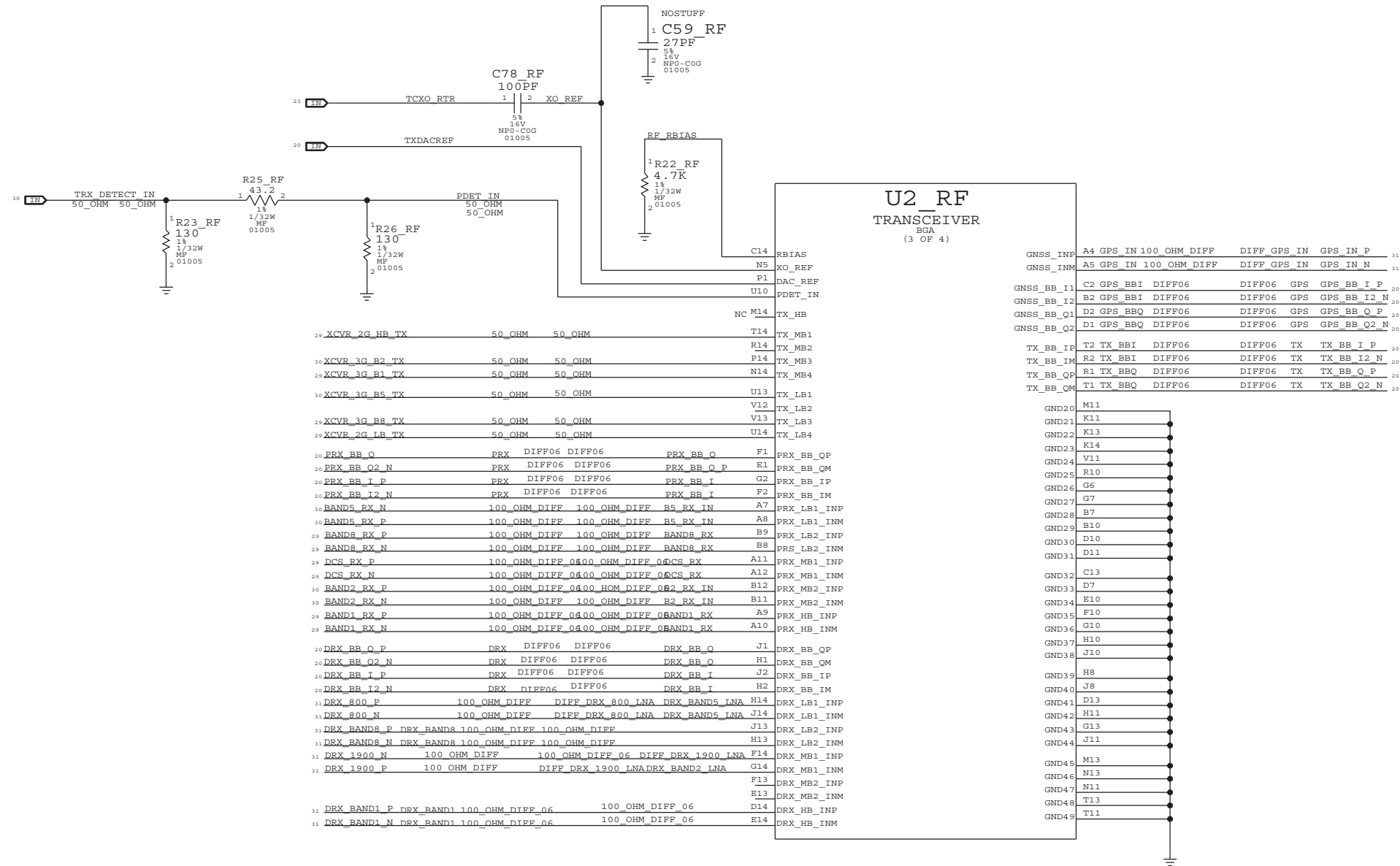


UART



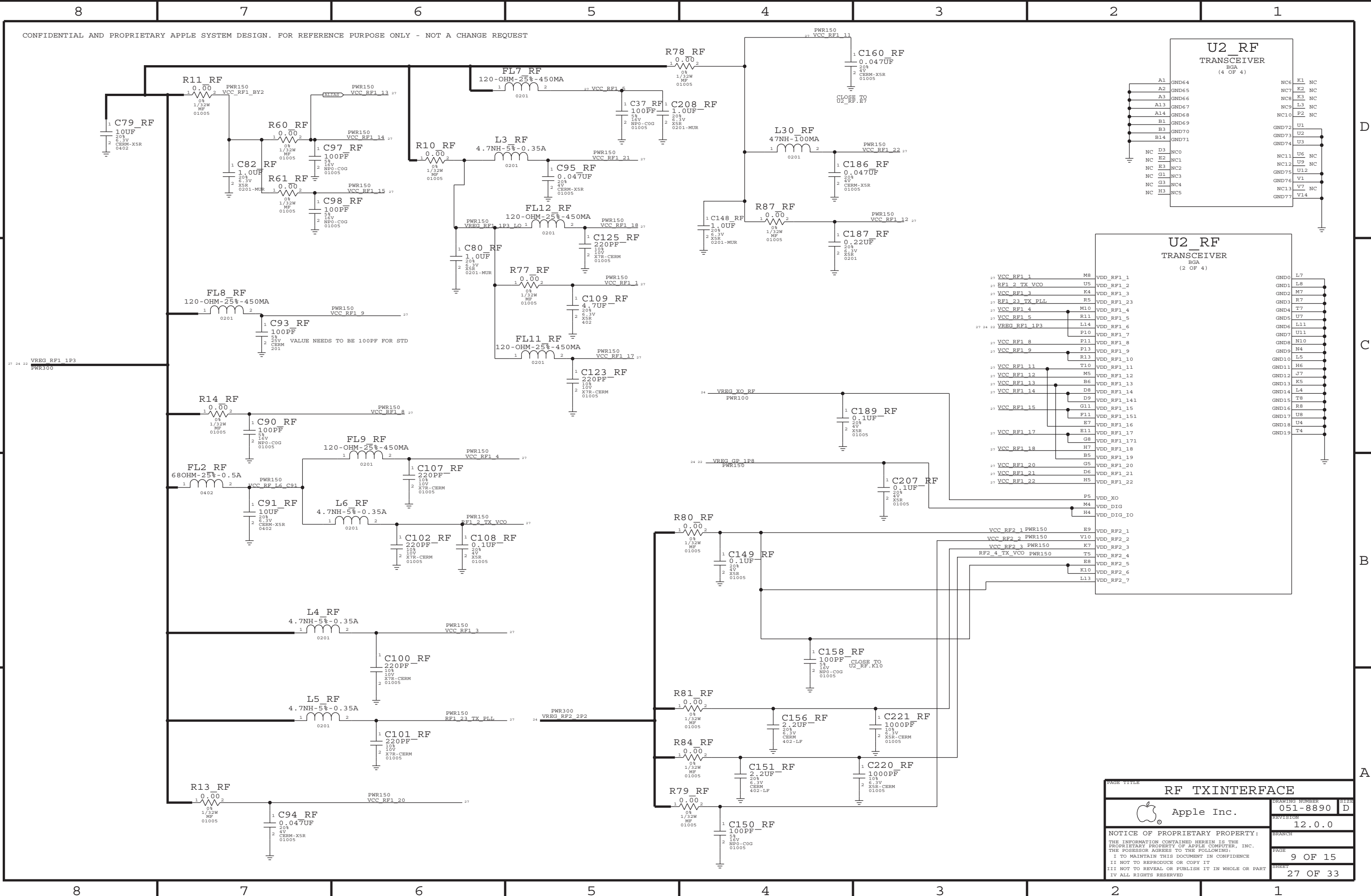
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RF TRANSCEIVER



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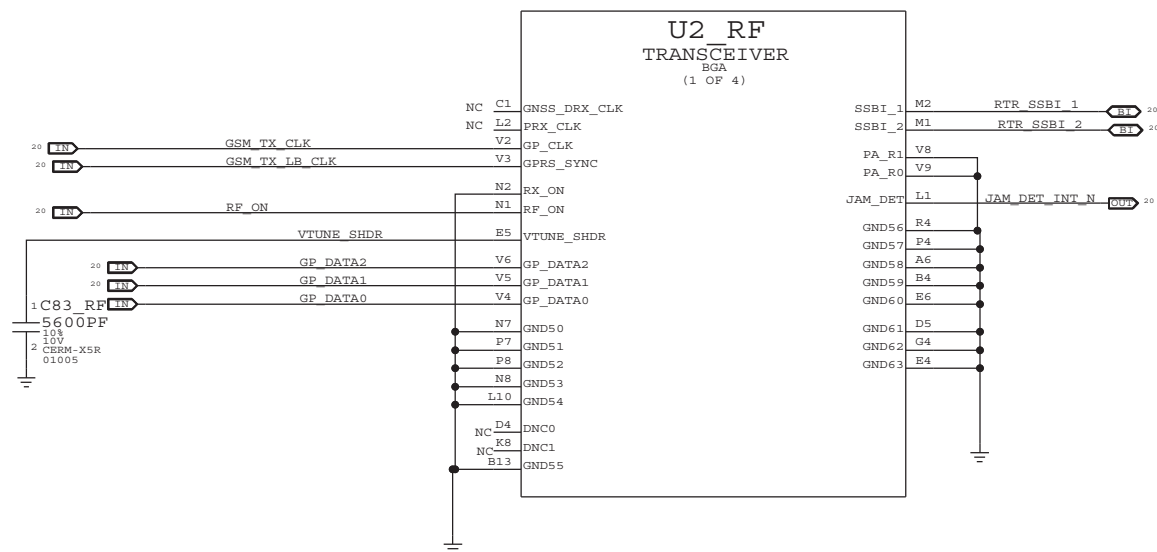
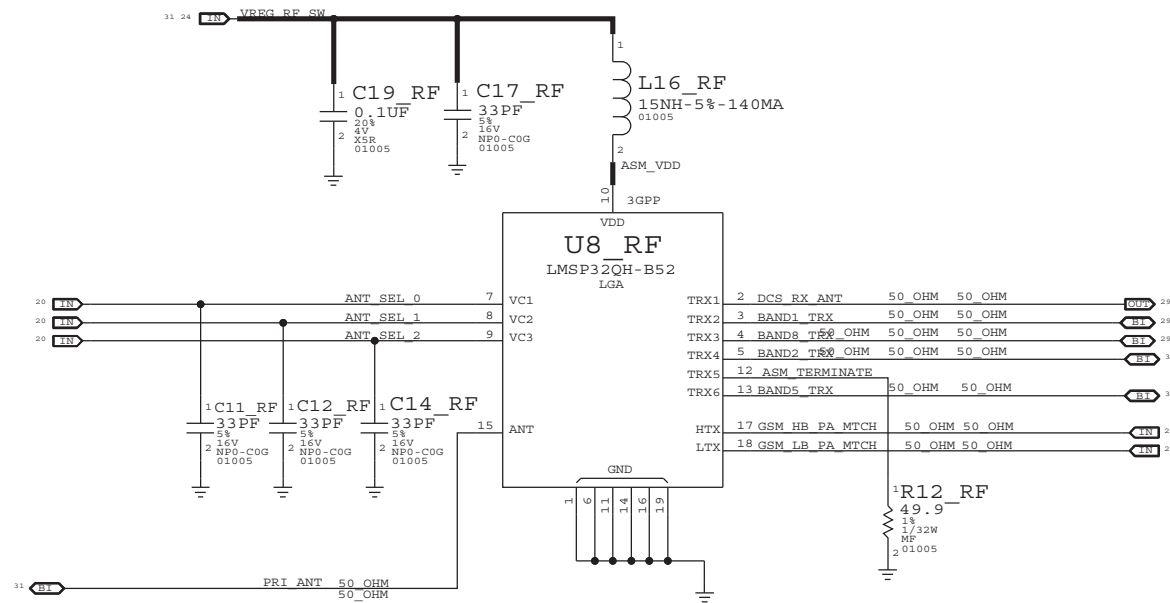
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27 VREG RF1 1P3	M8	VDD_RF1_1	L7
27 VREG RF1 1P3	U5	VDD_RF1_2	L8
27 VREG RF1 1P3	K4	VDD_RF1_3	M7
27 VREG RF1 1P3	R5	VDD_RF1_23	R7
27 VREG RF1 1P3	M10	VDD_RF1_4	T7
27 VREG RF1 1P3	R11	VDD_RF1_5	U7
27 VREG RF1 1P3	L14	VDD_RF1_6	L11
27 VREG RF1 1P3	P10	VDD_RF1_7	U11
27 VREG RF1 1P3	P11	VDD_RF1_8	N10
27 VREG RF1 1P3	P13	VDD_RF1_9	N4
27 VREG RF1 1P3	T10	VDD_RF1_10	L5
27 VREG RF1 1P3	M5	VDD_RF1_11	H6
27 VREG RF1 1P3	B6	VDD_RF1_12	J7
27 VREG RF1 1P3	D8	VDD_RF1_13	K5
27 VREG RF1 1P3	D9	VDD_RF1_14	L4
27 VREG RF1 1P3	G11	VDD_RF1_15	T8
27 VREG RF1 1P3	F11	VDD_RF1_151	R8
27 VREG RF1 1P3	E7	VDD_RF1_16	U8
27 VREG RF1 1P3	E11	VDD_RF1_17	U4
27 VREG RF1 1P3	G8	VDD_RF1_171	T4
27 VREG RF1 1P3	H7	VDD_RF1_18	
27 VREG RF1 1P3	B5	VDD_RF1_19	
27 VREG RF1 1P3	G5	VDD_RF1_20	
27 VREG RF1 1P3	D6	VDD_RF1_21	
27 VREG RF1 1P3	H5	VDD_RF1_22	
	P5	VDD_XO	
	M4	VDD_DIG	
	H4	VDD_DIG_IO	
	E9	VDD_RF2_1	
	V10	VDD_RF2_2	
	K7	VDD_RF2_3	
	T5	VDD_RF2_4	
	E8	VDD_RF2_5	
	K10	VDD_RF2_6	
	L13	VDD_RF2_7	

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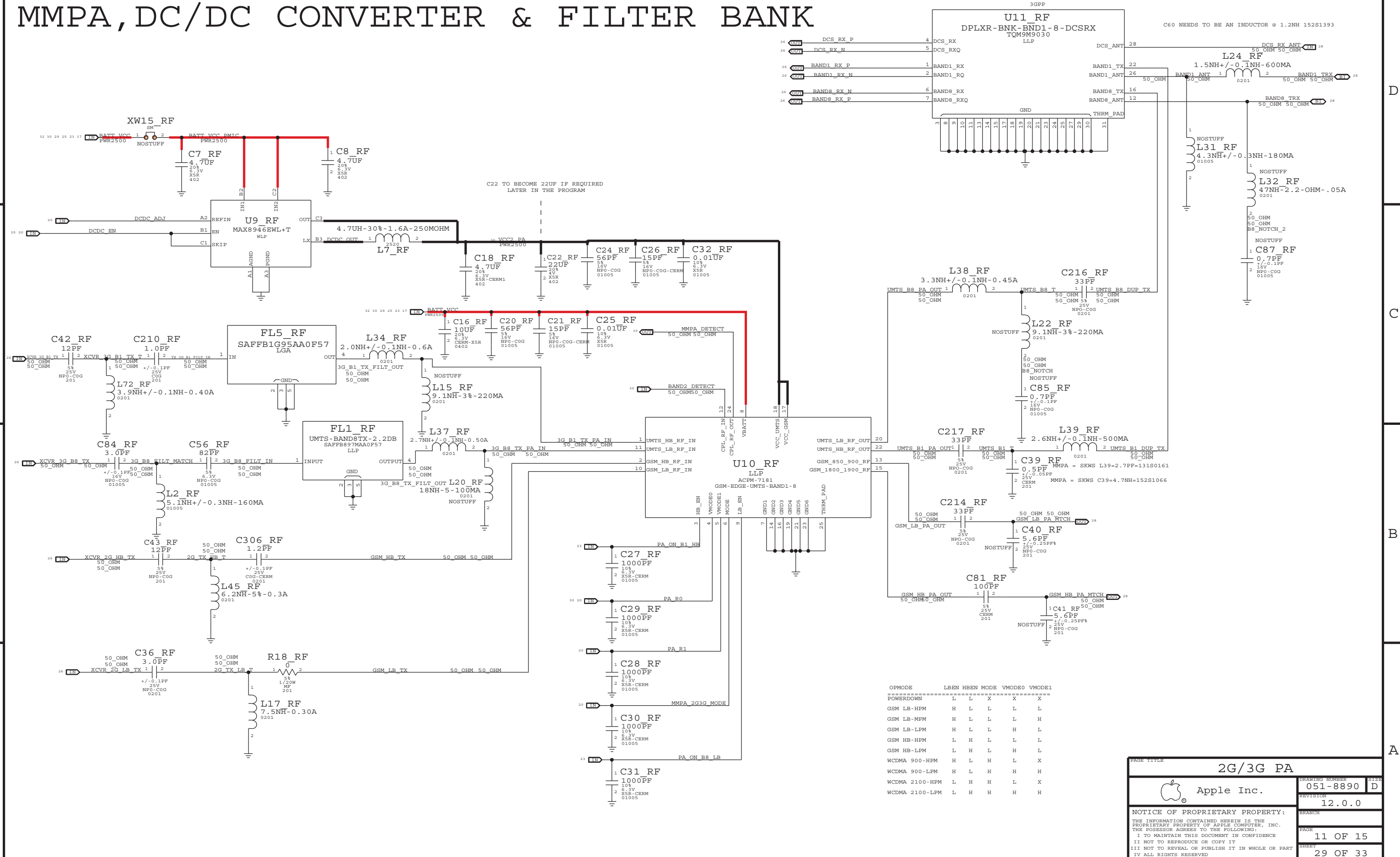
RF TRANSCEIVER AND ASM



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MMPA, DC/DC CONVERTER & FILTER BANK

D
C
B
A



OPMODE	LBEN	HBEN	MODE	VMODE0	VMODE1
POWERDOWN	L	L	X	X	X
GSM LB-HPM	H	L	L	L	L
GSM LB-MPM	H	L	L	L	H
GSM LB-LPM	H	L	L	H	L
GSM HB-HPM	L	H	L	L	L
GSM HB-LPM	L	H	L	H	L
WCDMA 900-HPM	H	L	H	L	X
WCDMA 900-LPM	H	L	H	H	H
WCDMA 2100-HPM	L	H	H	L	X
WCDMA 2100-LPM	L	H	H	H	H

2G/3G PA

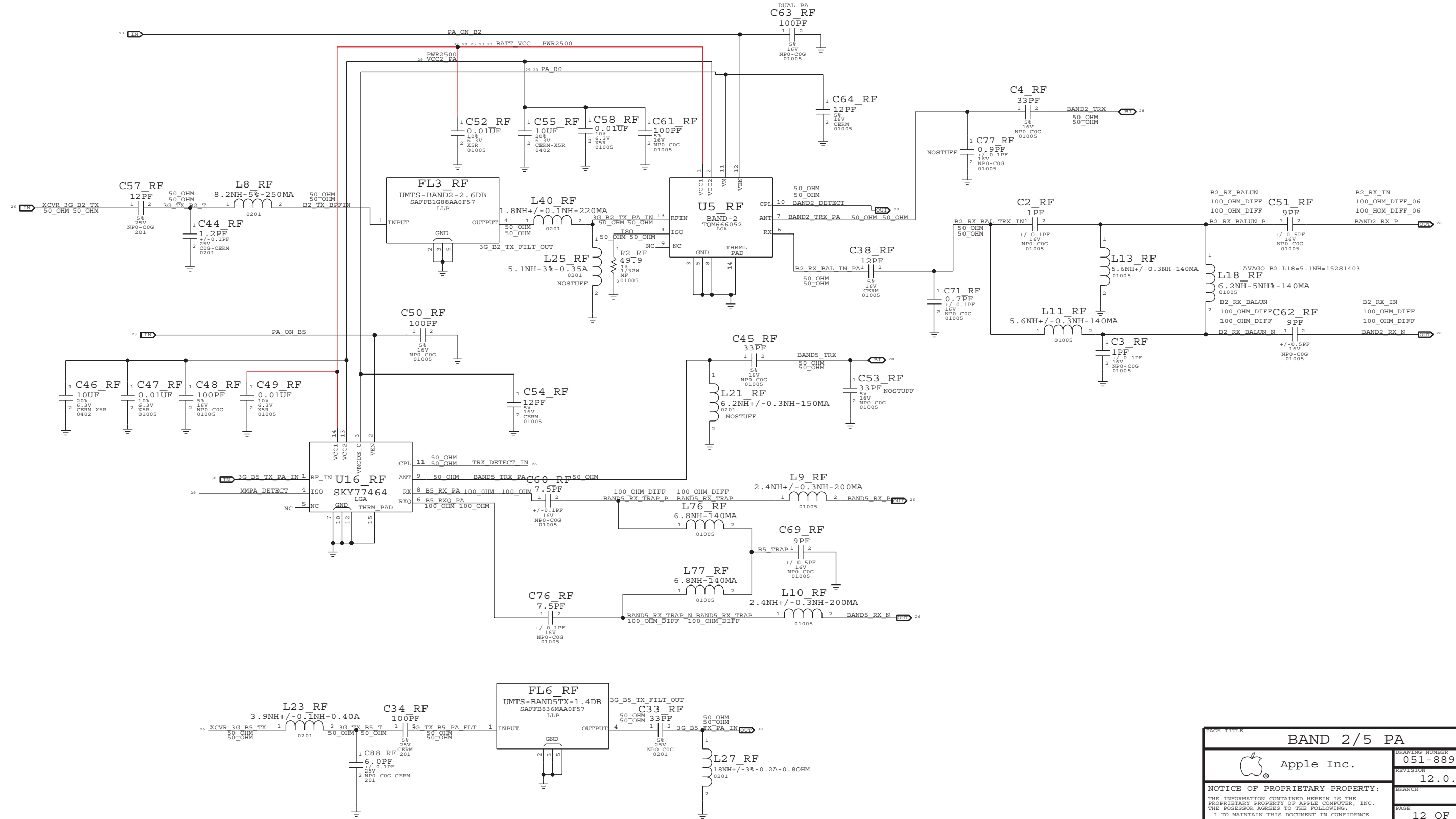
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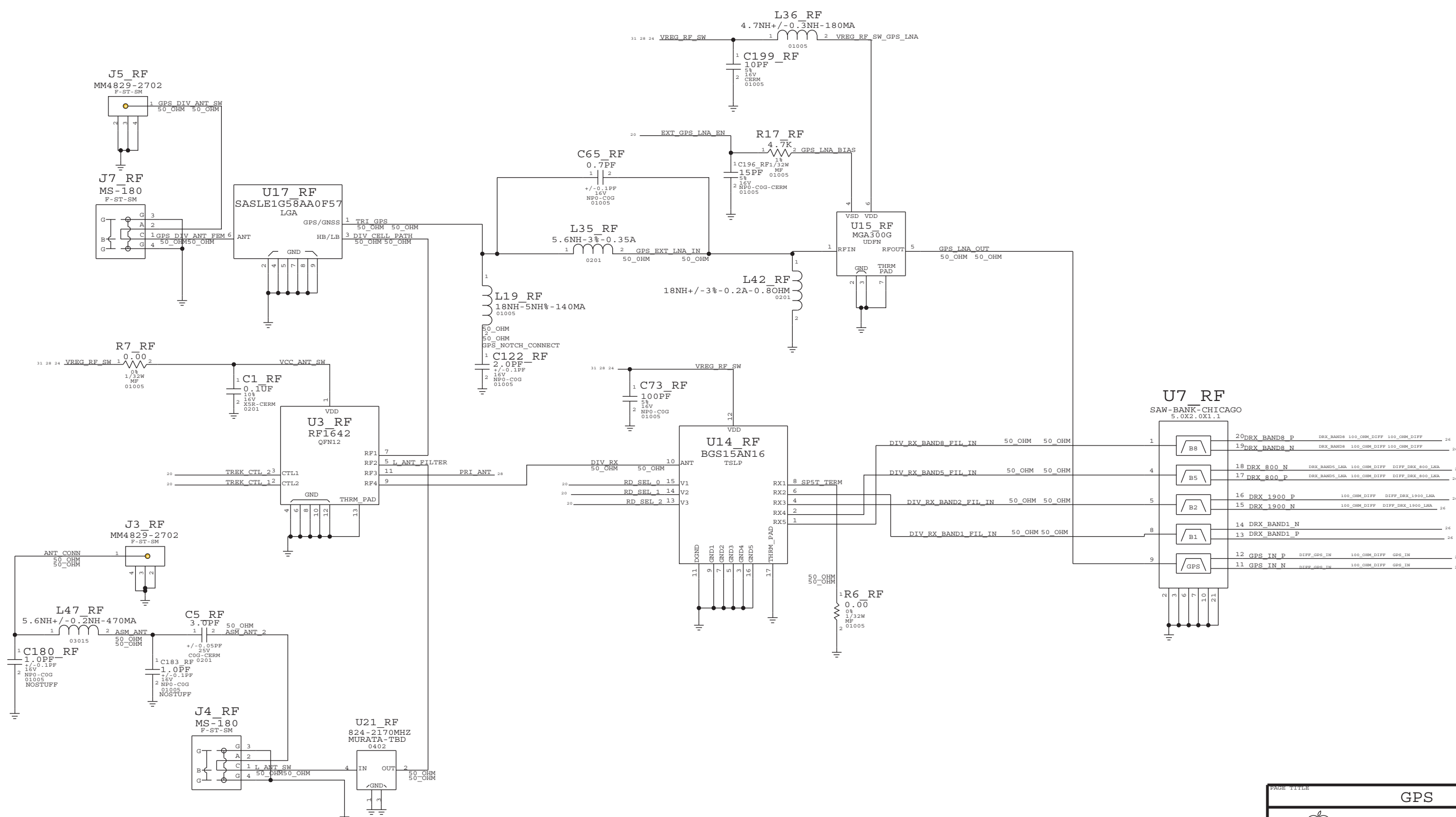
BAND 2 AND BAND 5 PAD



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BAND 2/5 PA		
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DIVERSITY AND EXTERNAL GPS LNA

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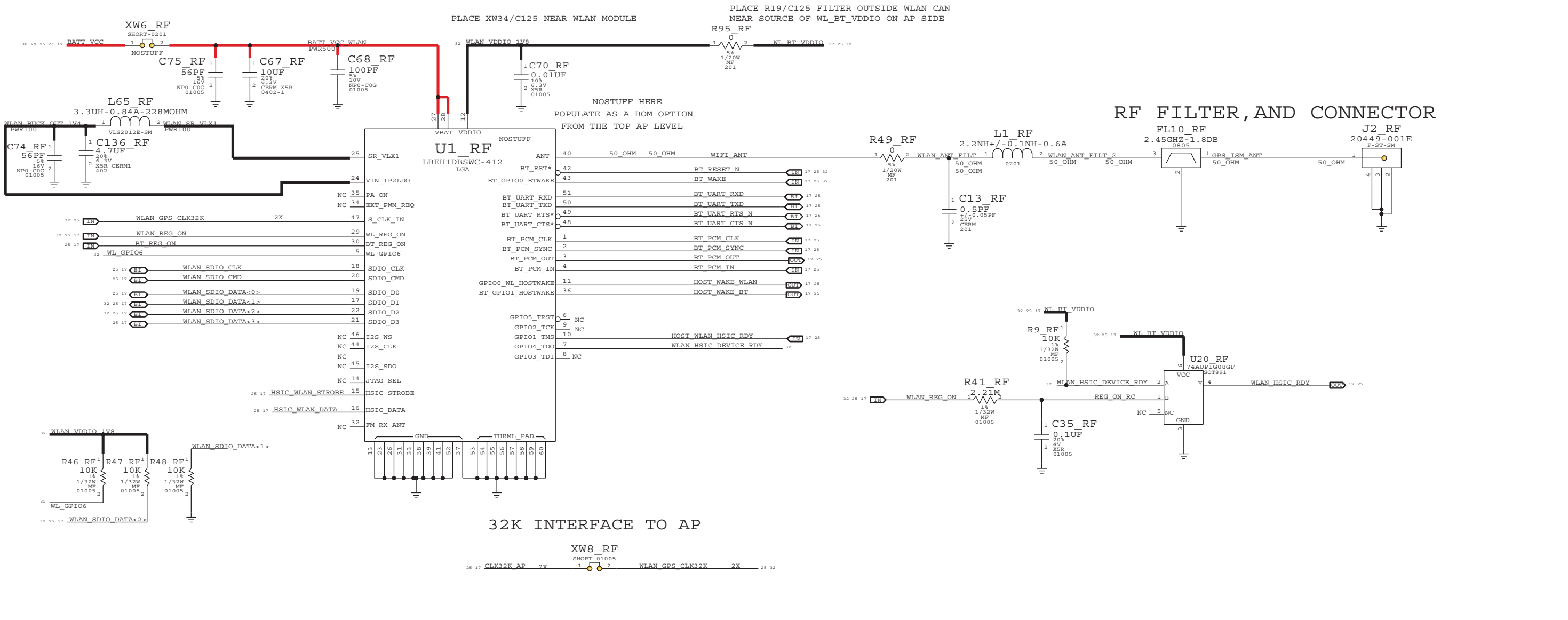


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WLAN/BLUETOOTH

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PLACE R19/C125 FILTER OUTSIDE WLAN CAN NEAR SOURCE OF WL_BT_VDDIO ON AP SIDE

NOSTUFF HERE POPULATE AS A BOM OPTION FROM THE TOP AP LEVEL

RF FILTER, AND CONNECTOR

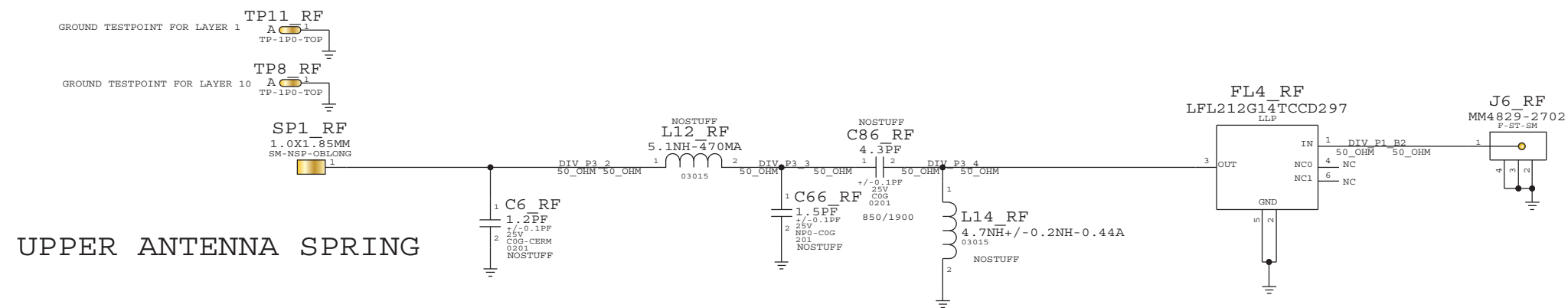
32K INTERFACE TO AP

PULL UP RESISTORS

PULL DOWN RESISTORS

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WIFI/BLUEOOTH/FM RADIO		
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ANTENNA MATCHING



NOTUFF ALL HERE !
 SPECIFIED IN TOP LEVEL FOR US/EU VALUE

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