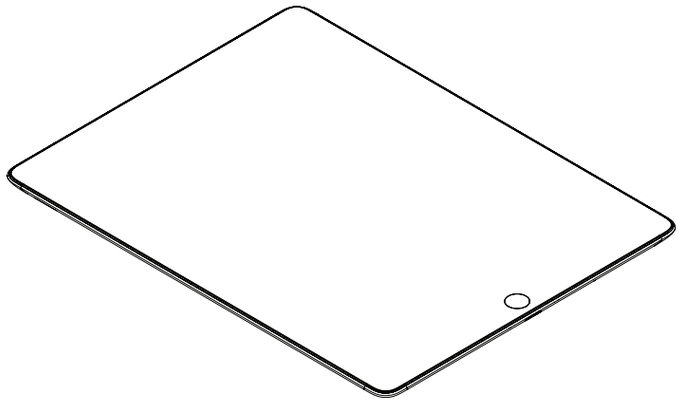
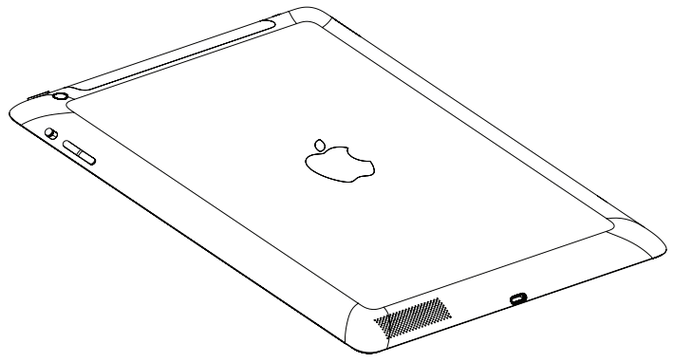
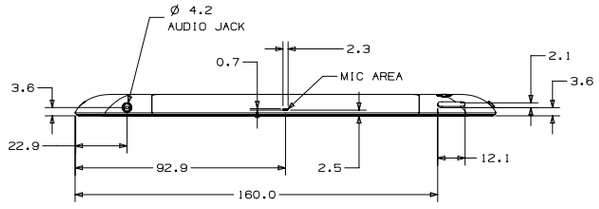
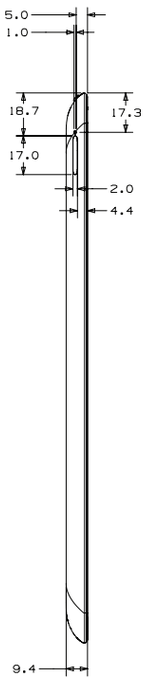
REV	ECO#	DESCRIPTION OF REVISION

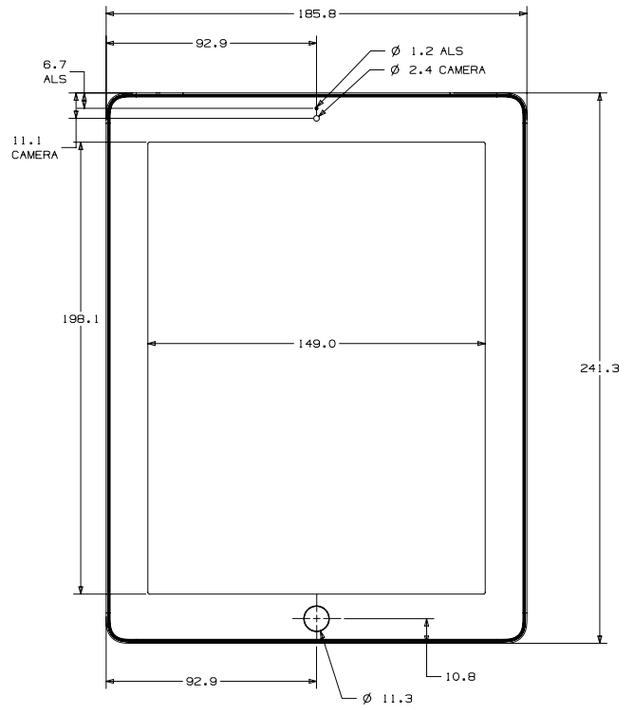
NOTES: (UNLESS OTHERWISE SPECIFIED)

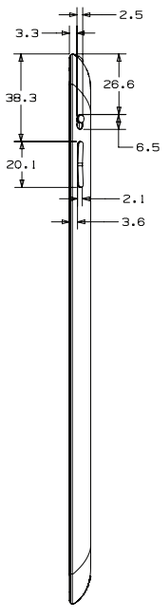


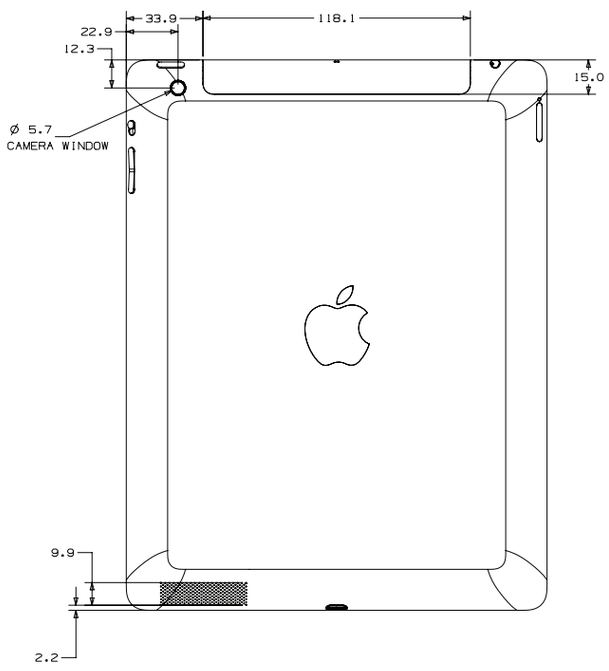


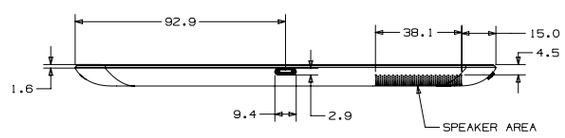


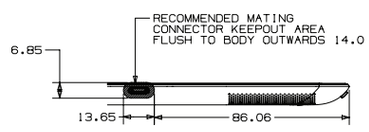


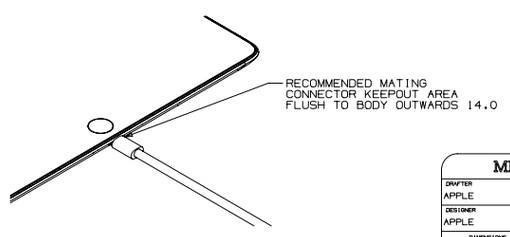








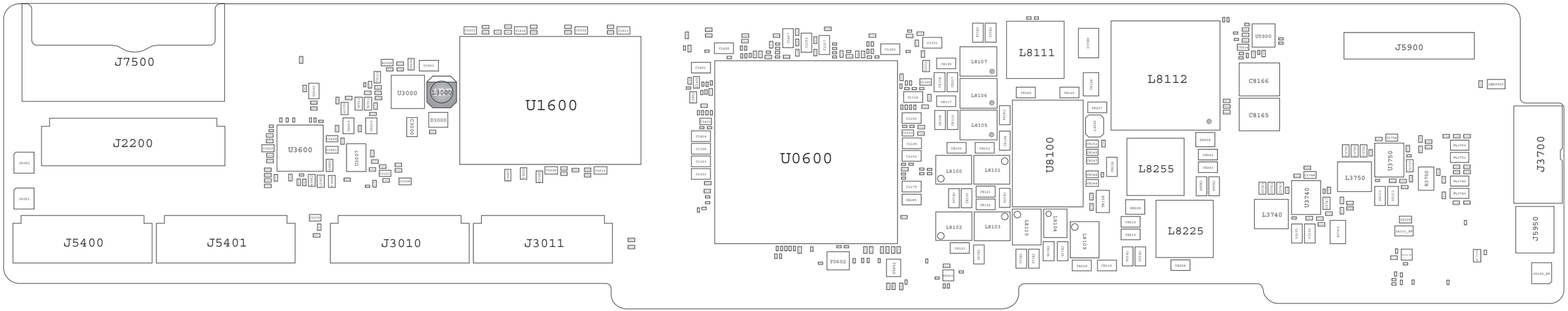




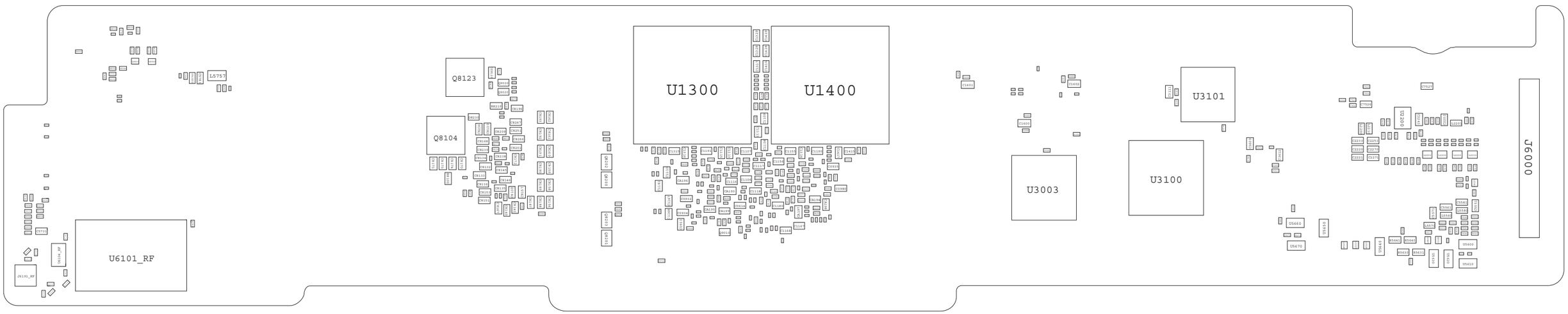
METRIC		Apple Inc.
DRAFTER: APPLE	DATE: 04/05/13	NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: (i) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (ii) NOT TO REPRODUCE OR COPY IT (iii) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART (iv) ALL RIGHTS RESERVED
DESIGNER: APPLE	DATE: 04/05/13	
DIMENSIONS ARE IN MILLIMETERS TOLERANCES X.X ±0.2 X.XX ±0.10 X.XXX ±0.050 ANGLES ±0.5° DO NOT SCALE DRAWINGS		TITLE: IPAD WI-FI + CELLULAR (4TH GENERATION)
		DRAWING NUMBER: REV. 02
THIRD ANGLE PROJECTION	SIZE: B	SCALE: NONE SHT 1 OF 1

NX GENERATED

820-3249-TOP MLB



820-3249-BOT MLB



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001554595	PRODUCTION RELEASED	2012-07-26

iPad 4th Gen

LAST_MODIFIED=Thu Jul 26 10:29:36 2012

DRAWING
MLB
DRAWING

DRAWING TITLE: X140 MLB

Apple Inc.

DRAWING NUMBER: 051-9385 | SIZE: D
REVISION: A.0.0
BRANCH:
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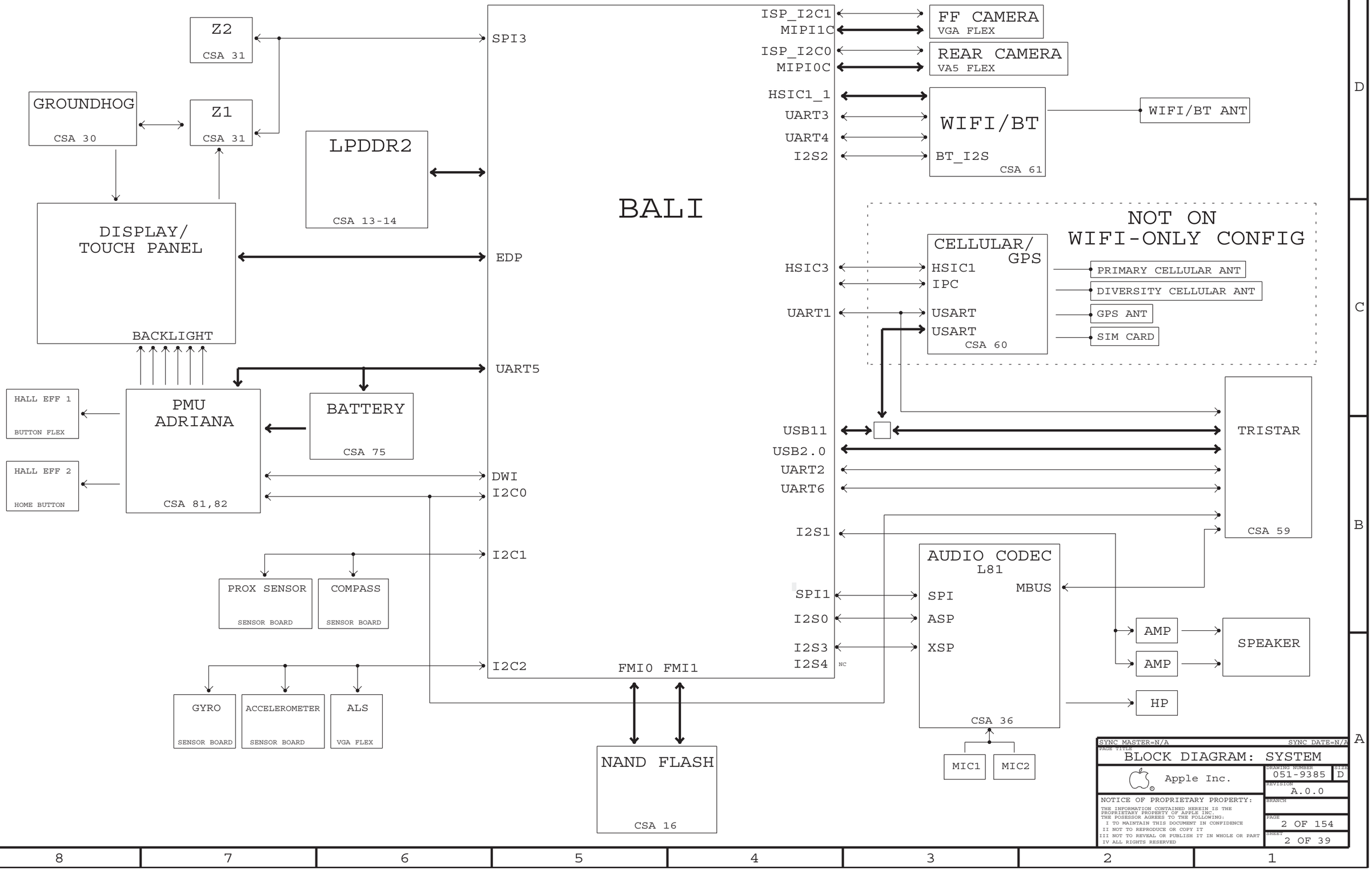

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE

BLOCK DIAGRAM: SYSTEM

Apple Inc.

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD: 16GB CONFIG
32GB_PROD: 32GB CONFIG
64GB_PROD: 64 GB CONFIG
DEV: DEV BOARD ONLY

MLB: MLB BOARD ONLY
MLB_A: WIFI ONLY CONFIG
MLB_B: CELLULAR CONFIG
MLB_C: CELLULAR CONFIG
MLB_D: LEGACY CELLULAR CONFIG
MLB_E: LEGACY CELLULAR CONFIG

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

MECHANICAL PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
NAND	806-4195	1	FENCE,NAND,TOP,MLB,X140	PD_FENCE_NAND	CRITICAL	
SOC/PMU	806-3493	1	FENCE,LARGE,TOP,MLB,X140	PD_FENCE_LARGE	CRITICAL	
AUDIO	806-3956	1	FENCE,AMP,MLB,X140	PD_FENCE_AMP	CRITICAL	
GRAPE	806-4196	1	FENCE,1,BTM,MLB,X140	PD_FENCE_BTM1	CRITICAL	
MEMORY	806-3492	1	FENCE,2,BTM,MLB,X140	PD_FENCE_BTM2	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1W8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-4176 (MLB A 128G)	EEEE_F80Q	CRITICAL	EEEE_MLB_A_128G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWKG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1WC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-4177 (MLB B 128G)	EEEE_F80P	CRITICAL	EEEE_MLB_B_128G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1WG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1W9	CRITICAL	EEEE_MLB_C_64G
825-7838	1	EEEE FOR 639-4178 (MLB C 128G)	EEEE_F80R	CRITICAL	EEEE_MLB_C_128G

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH,MLB,X140	SCH1	CRITICAL	
820-3249	1	PCBF,MLB,X140	PCB1	CRITICAL	

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC,SOC,H5G,FCBGA1089,0.5MM	U0600	CRITICAL	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC,PMU,ADRIANA,D2018A1,FCBGA	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2,533MHZ,512MB,SAMSUNG,35NM	U1300,U1400	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0637	333S0636		U1300,U1400	LPDDR2,533MHZ,HYNIX,38NM
333S0638	333S0636		U1400,U1400	LPDDR2,533MHZ,ELPIDA,38NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PPN1.5 16GB	U1600	CRITICAL	16GB_PROD

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0879	1	TOSHIBA PPN1.5 32GB	U1600	CRITICAL	32GB_PROD

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0880	1	TOSHIBA PPN1.5 64GB	U1600	CRITICAL	64GB_PROD

128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0912	1	TOSHIBA PPN1.5 128GB	U1600	CRITICAL	128GB_PROD

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
BOM TABLES

Apple Inc.

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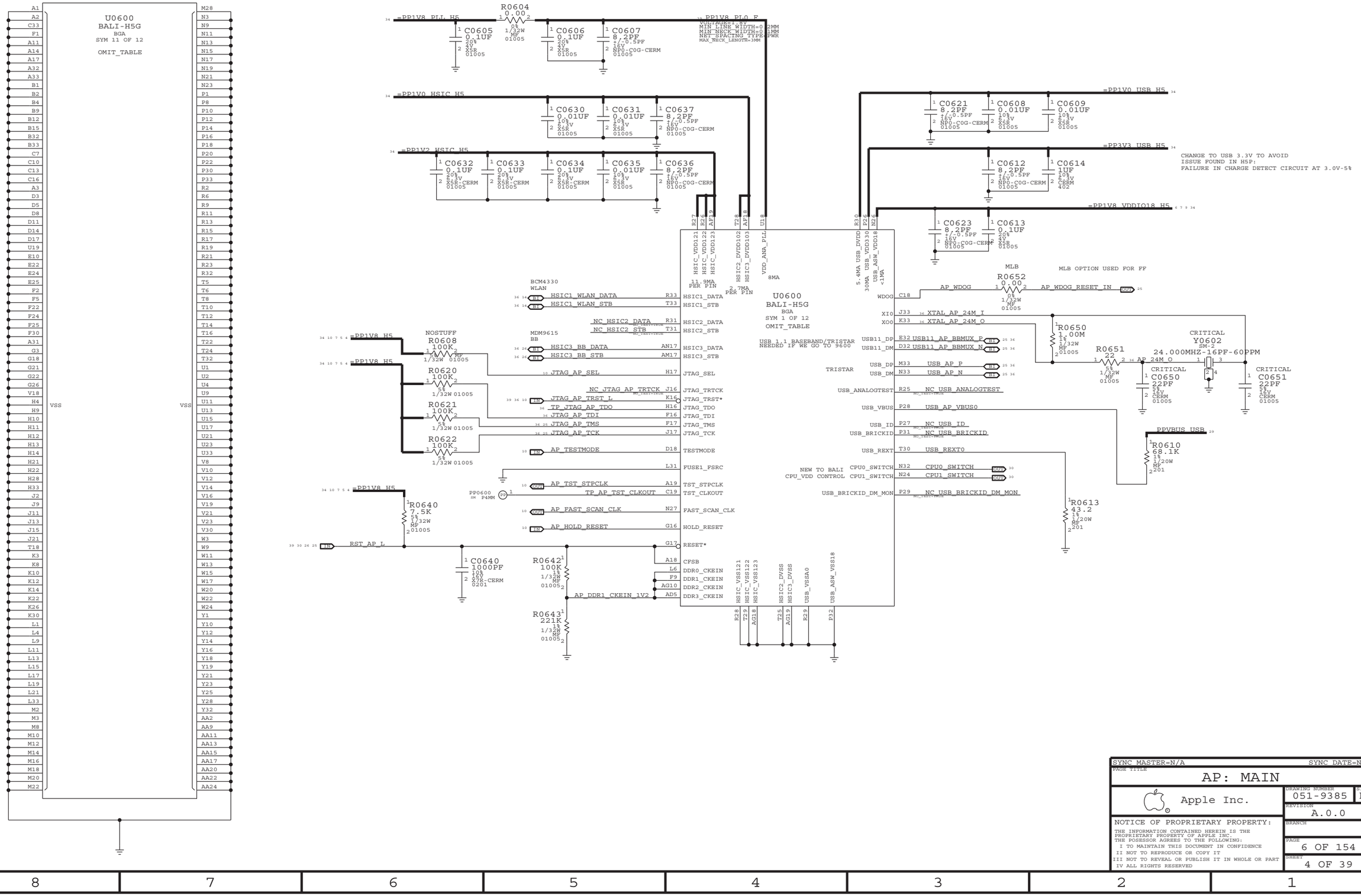

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE

AP: MAIN

Apple Inc.

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REVISION A.0.0

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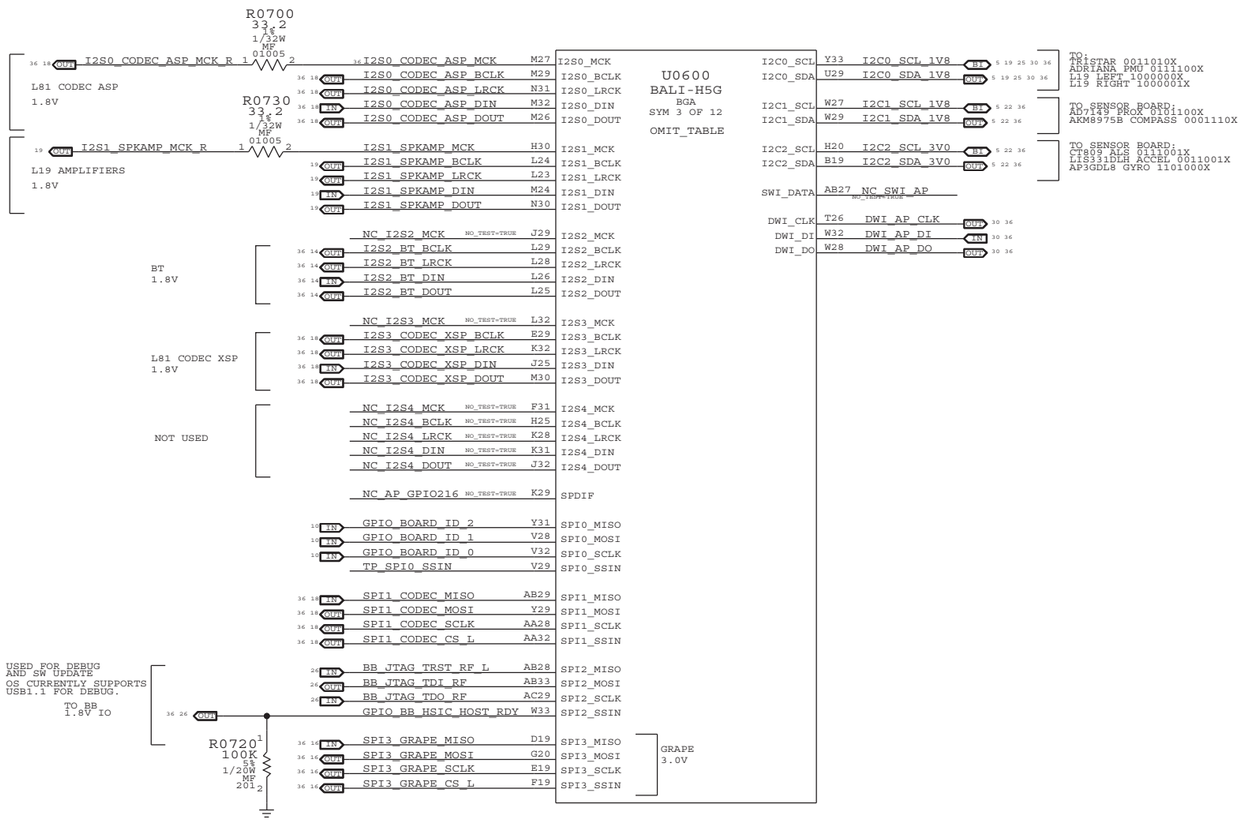

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AP: I/Os

Apple Inc.

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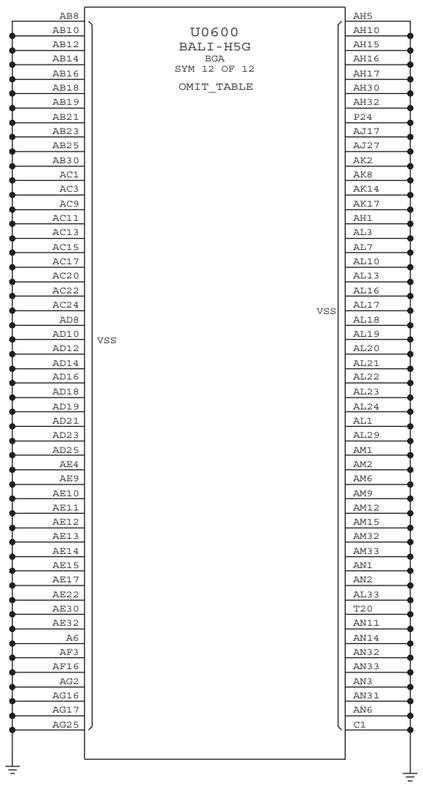

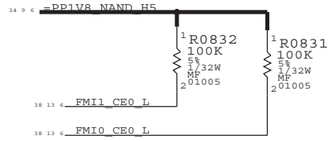

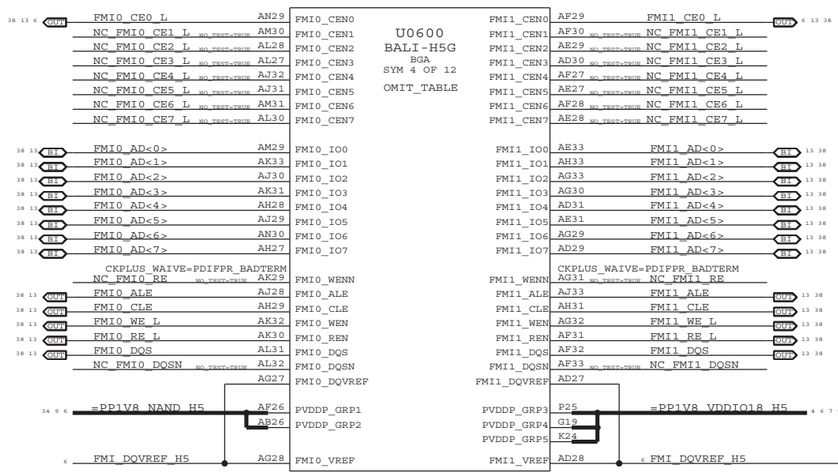

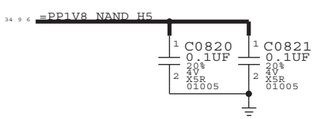

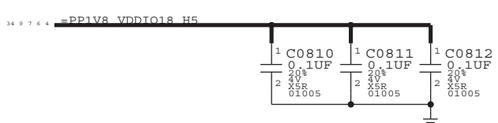

SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE

AP: NAND

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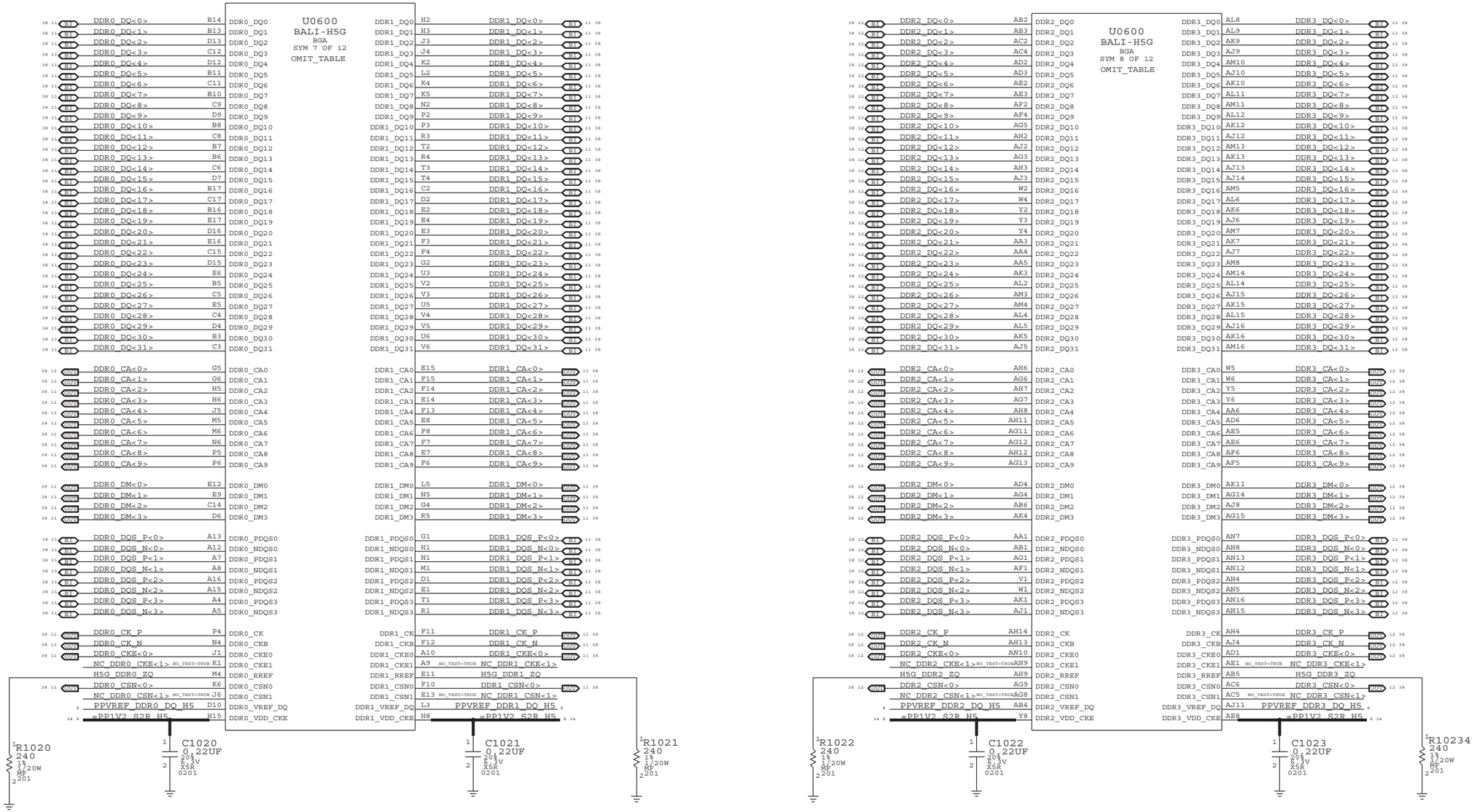
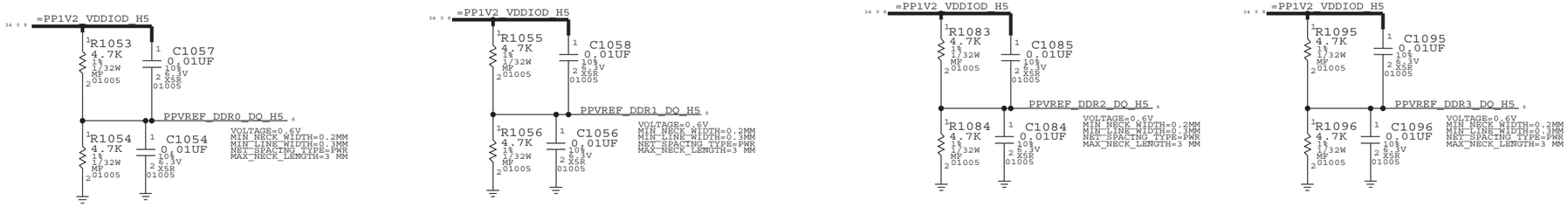
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0725	155S0359	?	FL0910	RDAR://PROBLEM/11104943

=PP1V0_DP_PAD_DVDD_H5 34
C0910 8.2PF ±0.1PF% 25V CERM 0201
=PP1V8_EDP_H5 34
R0911 0 5% 1/20W MF 201
=PP1V8_EDP_AVDD_AUX 33
C0931 56PF 5% 6.3V NPO-C0G 01005
C0928 8.2PF ±0.5PF 16V NPO-C0G-CERM 01005
C0929 8.2PF ±0.5PF 16V NPO-C0G-CERM 01005
C0930 56PF 5% 6.3V NPO-C0G 01005
C0932 0.22UF 20% 6.3V X5R 402
C0933 0.22UF 20% 6.3V X5R 402
C0934 0.22UF 20% 6.3V X5R 402
=PP1V0_EDP_PAD_DVDD_H5 34
C0909 0.1UF 10% 6.3V X5R 201
=PP1V8_DP_H5 34
C0927 0.1UF 20% 4V X5R 01005
C0924 56PF 5% 6.3V NPO-C0G 01005
=PP1V8_VDDIO18_H5 4 6 7 9 34
C0953 0.01UF 10% 6.3V X5R 01005
=PP1V8_VDDIO18_H5 4 6 7 9 34
C0951 0.1UF 20% 4V X5R 01005
C0952 0.01UF 10% 6.3V X5R 01005
NOSTUFF FL0911 240-OHM-0.2A-0.8-OHM 0201
=PP1V8_VDDIO18_H5 34 9 7 6 4
DAC_AP_COMP_FTR
NOSTUFF C0956 0.1UF 10% 6.3V X5R 201
NOSTUFF C0955 0.1UF 10% 6.3V X5R 201
NOSTUFF R0950 6.34K 1% 1/20W MF 201
DAC_AP_VREF 33
DAC_AP_IREF
DAC_AP_COMP
VOLTAGE=1.8V MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM
15MA EDP_PAD_DVDD C31
EDP_PAD_AVDDX B31
22MA EDP_PAD_AVDDP0 D29
10MA EDP_PAD_AVDD3 D25
EDP_PAD_AVDD2 D26
EDP_PAD_AVDD1 C27
EDP_PAD_AVDD0 C28
65MA PER PIN
16MA EDP_PAD_AVDD_AUX D30
15MA DP_PAD_DVDD C24
22MA DP_PAD_AVDDX C23
10MA DP_PAD_AVDDP0 D21
DP_PAD_AVDD3 A20
DP_PAD_AVDD2 B20
DP_PAD_AVDD1 E20
DP_PAD_AVDD0 E21
65MA PER PIN
16MA DP_PAD_AVDD_AUX D22
15MA DAC_AVDD18D H23
15MA DAC_AVDD18A H24
U0600 BALI-H5G BGA SYM 6 OF 12 OMIT_TABLE
DAC_VREF J23
DAC_IREF J24
DAC_COMP K23
EDP_HPD E18
EDP_AUX_P C30
EDP_AUX_N C29
EDP_DATA_P<0> A30
EDP_DATA_N<0> A29
EDP_DATA_P<1> D28
EDP_DATA_N<1> D27
EDP_DATA_P<2> B28
EDP_DATA_N<2> B27
EDP_DATA_P<3> C26
EDP_DATA_N<3> C25
NOTE: 0.6V ANALOG REF
AP_EDP_R_BIAS E28
EDP_PAD_R_BIAS
EDP_PAD_DC_TP F28
NOSTUFF C0957 0.01UF 10% 6.3V X5R 01005
NOSTUFF R0921 4.99K 1% 1/32W MF 01005
TP_EDP_AP_ANALOG_TEST
EDP_PAD_AVSS3 B25
EDP_PAD_AVSS2 B26
EDP_PAD_AVSS1 A27
EDP_PAD_AVSS0 A28
EDP_PAD_DVSS D31
EDP_PAD_AVSSX C32
EDP_PAD_AVSSP0 B29
EDP_PAD_AVSS_AUX B30
DP_PAD_DVSS A24
DP_PAD_AVSSX A23
DP_PAD_AVSSP0 B21
DP_PAD_AVSS3 C20
DP_PAD_AVSS2 F20
DP_PAD_AVSS1 D20
DP_PAD_AVSS0 F21
DP_PAD_AVSS_AUX B22
DAC_AVSS18D G23
DAC_AVSS18A G24
DAC_OUT3 D33 NO_TEST=TRUE NC_DAC_AP_OUT3
DAC_OUT2 E33 NO_TEST=TRUE NC_DAC_AP_OUT2
DAC_OUT1 F33 NO_TEST=TRUE NC_DAC_AP_OUT1
DP_HPD B18 NO_TEST=TRUE NC_DP_HPD
DP_PAD_AUXP A26 NO_TEST=TRUE NC_DP_AUX_P
DP_PAD_AUXN A25 NO_TEST=TRUE NC_DP_AUX_N
DP_PAD_TX0P D24 NO_TEST=TRUE NC_DP_DATA_P<0>
DP_PAD_TX0N D23 NO_TEST=TRUE NC_DP_DATA_N<0>
DP_PAD_TX1P B24 NO_TEST=TRUE NC_DP_DATA_P<1>
DP_PAD_TX1N B23 NO_TEST=TRUE NC_DP_DATA_N<1>
DP_PAD_TX2P C22 NO_TEST=TRUE NC_DP_DATA_P<2>
DP_PAD_TX2N C21 NO_TEST=TRUE NC_DP_DATA_N<2>
DP_PAD_TX3P A22 NO_TEST=TRUE NC_DP_DATA_P<3>
DP_PAD_TX3N A21 NO_TEST=TRUE NC_DP_DATA_N<3>
DP_PAD_R_BIAS E23
DP_PAD_DC_TP F23 TP_DP_AP_ANALOG_TEST
NOTE: 0.6V ANALOG REF
R0920 4.99K 1% 1/32W MF 01005
NOSTUFF C0950 0.01UF 10% 6.3V X5R 01005
FL0910 80-OHM-0.2A-0.4-OHM 0201-1
=PP1V0_MIPI_PLL_H5 34
PP1V0_MIPI_PLL_F 39
VOLTAGE=1.0V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM
C0980 1UF 10% 6.3V CERM 402
C0981 0.01UF 10% 6.3V X5R 01005
C0982 56PF 5% 6.3V NPO-C0G 01005
=PP1V0_MIPI_H5 34
C0935 1UF 10% 6.3V CERM 402
C0908 0.1UF 10% 6.3V X5R 201
C0903 0.1UF 10% 6.3V X5R 201
C0904 8.2PF ±0.5PF 16V NPO-C0G-CERM 01005
=PP1V8_MIPI_H5 34
C0907 0.1UF 10% 6.3V X5R 201
PP0V4_MIPI1D
C0960 2.2NF 10% 10V X5R-CERM 0201
C0961 2.2NF 10% 10V X5R-CERM 0201
VOLTAGE=0.4V MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3MM
AF20 AF21 AF22 AF23 AF24
AH21 AH22 AH23 AH24 AH20
40MA MIPI_VDD10
3.2MA MIPI1D_VDD10_PLL
2MA PER PIN MIPI1D_VDD18
MIPI1D_VREG_0P4V
U0600 BALI-H5G BGA SYM 5 OF 12 OMIT_TABLE
NC_MIPI_VSYNC_H5 NO_TEST=TRUE U27 MIPI_VSYNC
MIPI0C_CAM_RF_DATA_P<0> AN22 MIPI0C_DPDATA0
MIPI0C_CAM_RF_DATA_N<0> AN22 MIPI0C_DNDATA0
MIPI0C_CAM_RF_DATA_P<1> AM21 MIPI0C_DPDATA1
MIPI0C_CAM_RF_DATA_N<1> AN21 MIPI0C_DNDATA1
NC_MIPI0C_CAM_RF_DATA_P<2> NO_TEST=TRUE AM19 MIPI0C_DPDATA2
NC_MIPI0C_CAM_RF_DATA_N<2> NO_TEST=TRUE AN19 MIPI0C_DNDATA2
NC_MIPI0C_CAM_RF_DATA_P<3> NO_TEST=TRUE AM18 MIPI0C_DPDATA3
NC_MIPI0C_CAM_RF_DATA_N<3> NO_TEST=TRUE AN18 MIPI0C_DNDATA3
MIPI0C_CAM_RF_CLK_P AM20 MIPI0C_DPCLK
MIPI0C_CAM_RF_CLK_N AN20 MIPI0C_DNCLK
ISP0_FLASH M25
ISP0_PRE_FLASH M31 NO_TEST=TRUE NC_ISP0_CAM_RF_FLASH
ISP0_SCL AA27 ISP0_CAM_RF_I2C_SCL
ISP0_SDA U28 ISP0_CAM_RF_I2C_SDA
REAR FACING CAM
ISP1_FLASH N25 SOCHOT1_L
ISP1_PRE_FLASH L30 SOCHOT0_L
FRONT FACING CAM
ISP1_SCL AA33 ISP1_CAM_FF_I2C_SCL
ISP1_SDA U30 ISP1_CAM_FF_I2C_SDA
SENSOR0_CLK V31 ISP0_CAM_RF_CLK_R 0.00 R0900 ISP0_CAM_RF_CLK
SENSOR0_RST U32 ISP0_CAM_RF_SHUTDOWN
SHUTDOWN IS ACTIVE HIGH
SENSOR1_CLK U31 ISP1_CAM_FF_CLK_R 0.00 R0940 ISP1_CAM_FF_CLK
SENSOR1_RST T27 ISP1_CAM_FF_SHUTDOWN_L
SHUTDOWN IS ACTIVE LOW
MIPI1C_DPDATA0 AM23 MIPI1C_CAM_FF_DATA_P<0>
MIPI1C_DNDATA0 AN23 MIPI1C_CAM_FF_DATA_N<0>
MIPI1C_DPDATA1 AM25 NO_TEST=TRUE NC_MIPI1C_CAM_FF_DATA_P<1>
MIPI1C_DNDATA1 AN25 NO_TEST=TRUE NC_MIPI1C_CAM_FF_DATA_N<1>
MIPI1C_DPCLK AM24 MIPI1C_CAM_FF_CLK_P
MIPI1C_DNCLK AN24 MIPI1C_CAM_FF_CLK_N
MIPI_VSS
AG20 AG21 AG22 AG23 AG24
=PP1V8_H5 4 5 7 10 34
R0930 1.00K 1% 1/32W MF 01005
R0931 1.00K 1% 1/32W MF 01005
R0932 1.00K 1% 1/32W MF 01005
R0933 1.00K 1% 1/32W MF 01005
NOSTUFF R0942 100K 5% 1/32W MF 01005
NOSTUFF R0941 100K 5% 1/32W MF 01005
SOCHOT1_L PULL-UP ON CSA 90
SOCHOT1_L 32 7
SOCHOT0_L 7

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE
AP: TV,DP,MIPI
Apple Inc.
DRAWING NUMBER 051-9385 SIZE D
REVISION A.0.0
BRANCH
PAGE 9 OF 154
SHEET 7 OF 39





SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AP: DDR

Apple Inc.

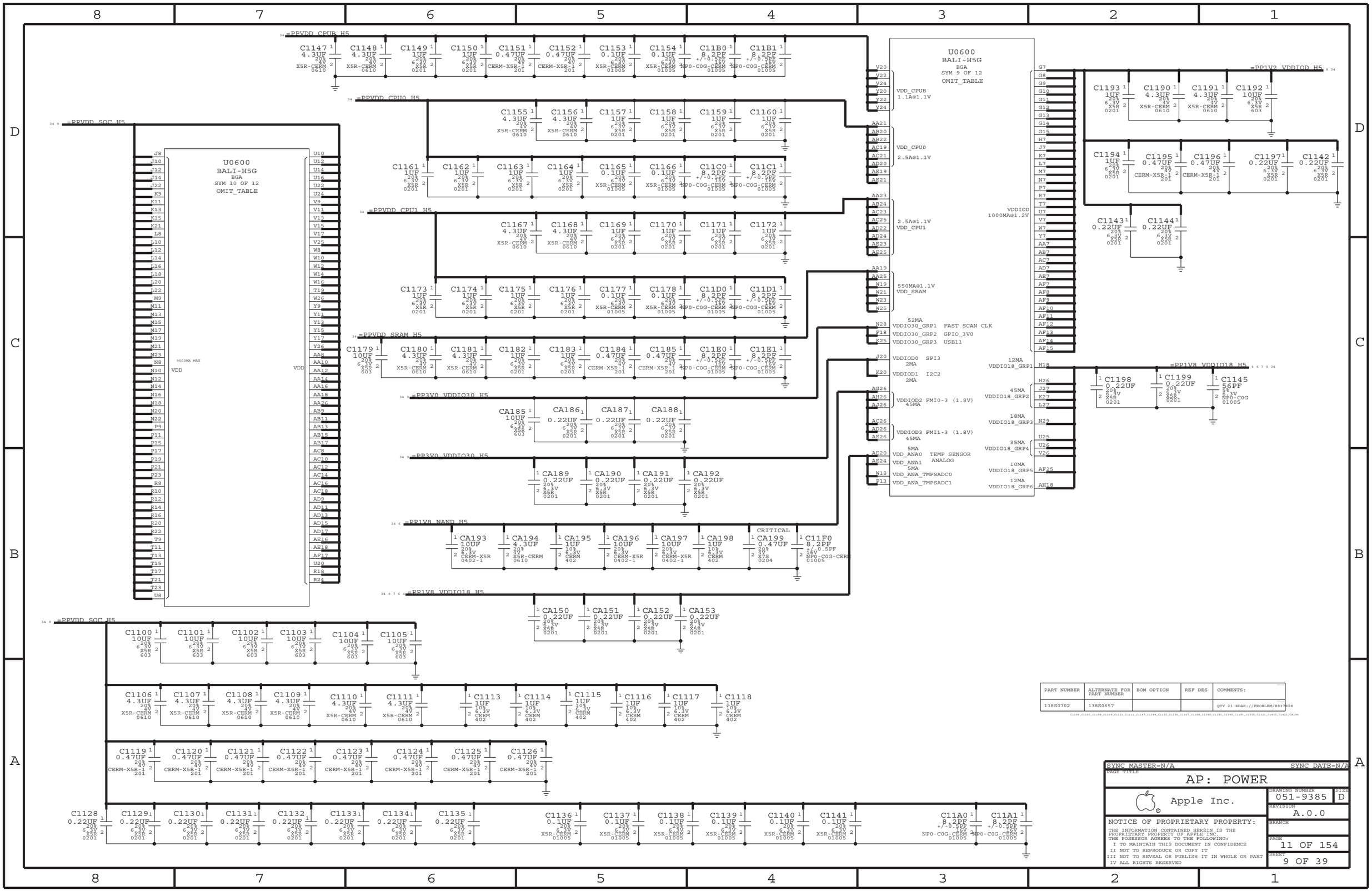
DRAWING NUMBER 051-9385 SIZE D

REVISION A.0.0

BRANCH

PAGE 10 OF 154

SHEET 8 OF 39



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657			QTY 21 RDAR://PROBLEM/8837828

C1104,C1107,C1108,C1109,C1110,C1111,C1147,C1148,C1155,C1156,C1157,C1158,C1160,C1161,C1190,C1191,C1115,C1121,C1415,C1421,C4194

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

AP: POWER

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

REVISION A.0.0

BRANCH

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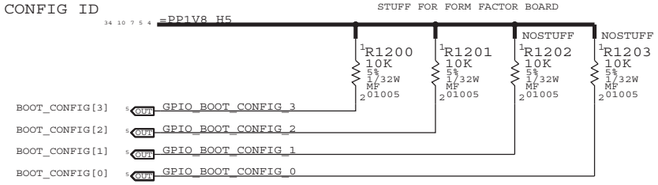
SHEET 9 OF 39

BOOT CONFIG ID



BOOT_CONFIG[3-0]	
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

CURRENT SETTING --->

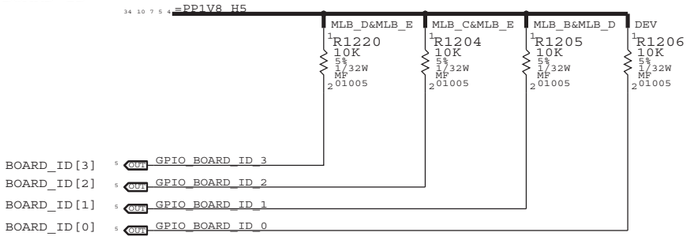
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI1
0010	SPI0 W/TEST
0011	SPI1 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1100	FMI0/1 2/2 CS
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

BOARD ID

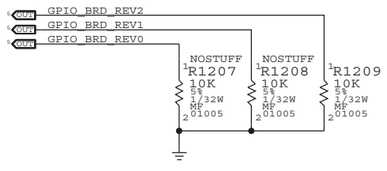


BOARD_ID[3-0]	
0000	X140 AP WLAN (MLB A)
0001	X140 DEV WLAN
0010	X140 AP BB_41 (MLB B)
0011	X140 DEV BB_41
0100	X140 AP BB_42 (MLB C)
0101	X140 DEV BB_42
1010	X140 AP BB_26A (MLB D)
1011	X140 DEV BB_26A
1110	X140 AP BB_26 (MLB E)
1111	X140 DEV BB_26

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



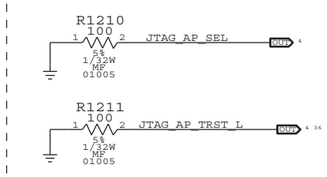
BRD_REV[2-0]	
000	PROTO
001	PROTO 2
010	EVT
011	DVT

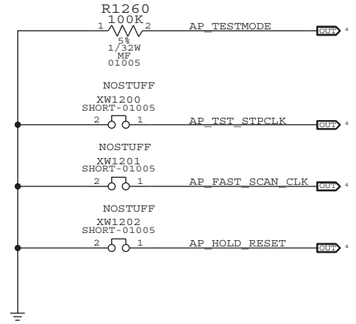
CURRENT SETTING --->

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

JTAG





SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE

AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

REVISION A.0.0

BRANCH

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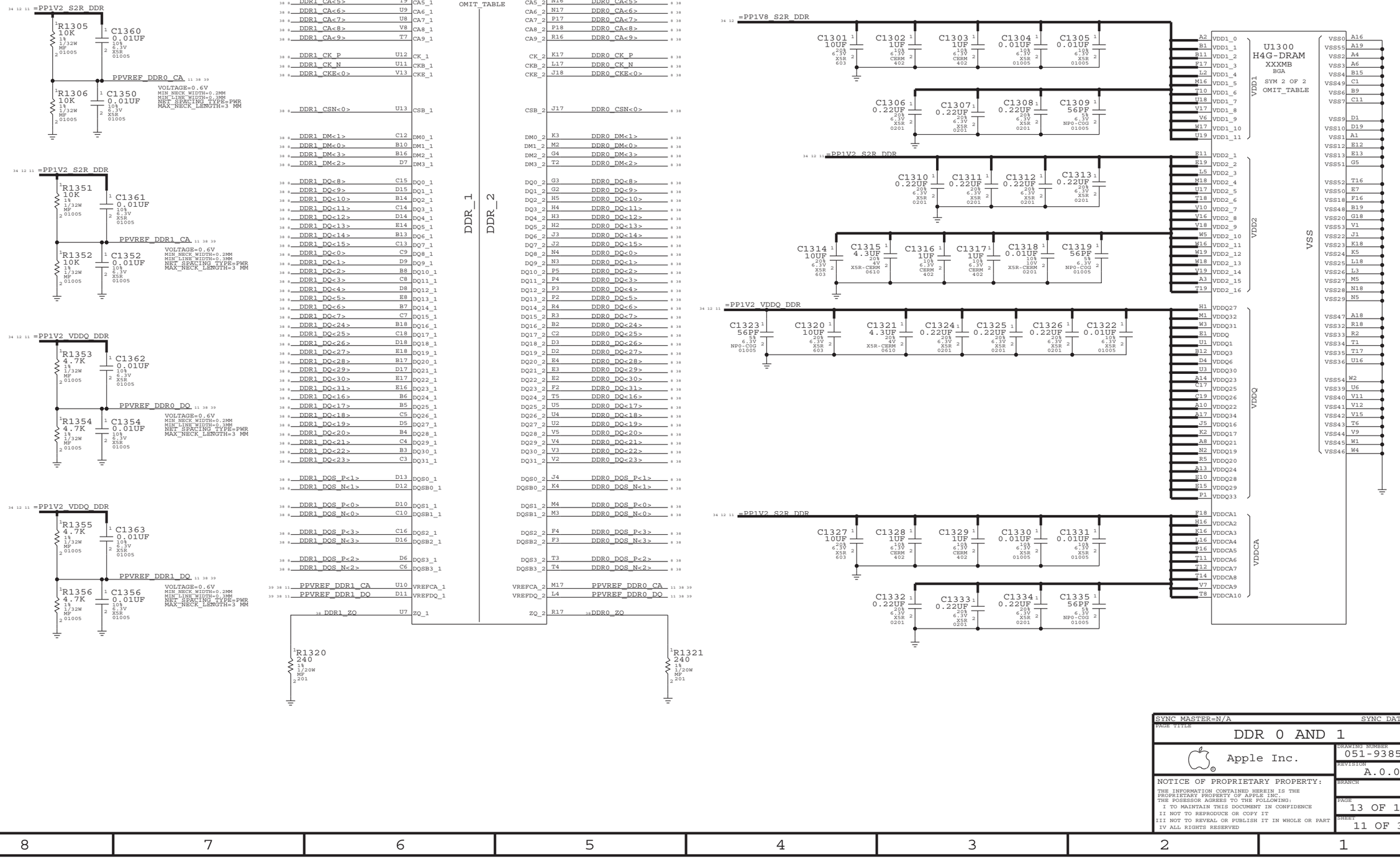
SHEET 10 OF 39



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: DDR 0 AND 1

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: A.0.0

BRANCH:

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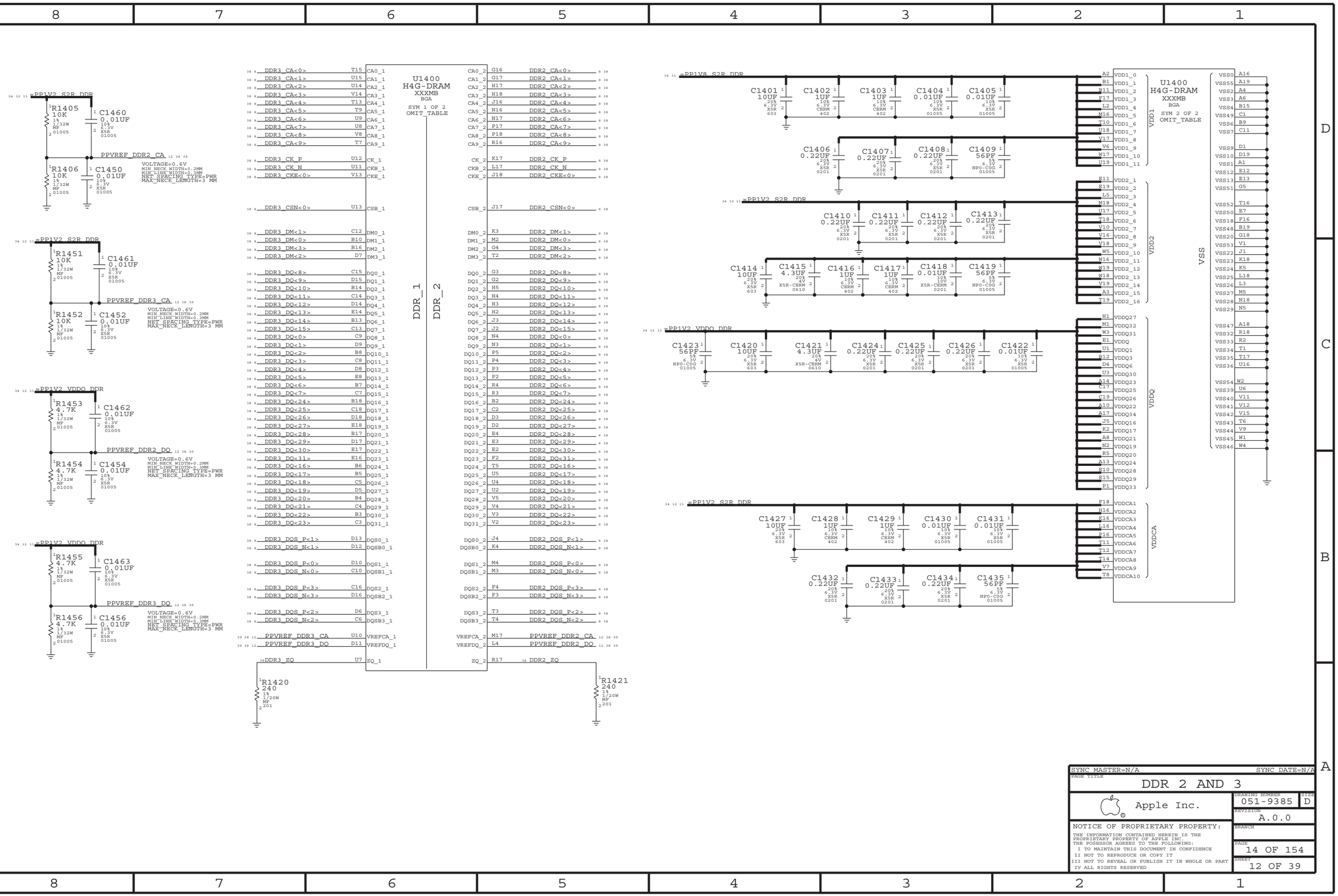
SHEET: 11 OF 39


8
7
6
5
4
3
2
1
D
C
B
A
=PP1V2_S2R_DDR
R1405 10K 1% 1/32W MF 01005
C1460 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR2_CA
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
R1406 10K 1% 1/32W MF 01005
C1450 0.01UF 10% 6.3V X5R 01005
=PP1V2_S2R_DDR
R1451 10K 1% 1/32W MF 01005
C1461 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR3_CA
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
R1452 10K 1% 1/32W MF 01005
C1452 0.01UF 10% 6.3V X5R 01005
=PP1V2_VDDQ_DDR
R1453 4.7K 1% 1/32W MF 01005
C1462 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR2_DQ
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
R1454 4.7K 1% 1/32W MF 01005
C1454 0.01UF 10% 6.3V X5R 01005
=PP1V2_VDDQ_DDR
R1455 4.7K 1% 1/32W MF 01005
C1463 0.01UF 10% 6.3V X5R 01005
PPVREF_DDR3_DQ
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
R1456 4.7K 1% 1/32W MF 01005
C1456 0.01UF 10% 6.3V X5R 01005
U1400
H4G-DRAM
XXXMB
BGA
SYM 1 OF 2
OMIT_TABLE
DDR_1
DDR_2
DDR3_CA<0> T15 CA0_1
DDR3_CA<1> U15 CA1_1
DDR3_CA<2> U14 CA2_1
DDR3_CA<3> V14 CA3_1
DDR3_CA<4> T13 CA4_1
DDR3_CA<5> T9 CA5_1
DDR3_CA<6> U9 CA6_1
DDR3_CA<7> U8 CA7_1
DDR3_CA<8> V8 CA8_1
DDR3_CA<9> T7 CA9_1
DDR3_CK_P U12 CK_1
DDR3_CK_N U11 CKB_1
DDR3_CKE<0> V13 CKE_1
DDR3_CSN<0> U13 CSB_1
DDR3_DM<1> C12 DM0_1
DDR3_DM<0> B10 DM1_1
DDR3_DM<3> B16 DM2_1
DDR3_DM<2> D7 DM3_1
DDR3_DQ<8> C15 DQ0_1
DDR3_DQ<9> D15 DQ1_1
DDR3_DQ<10> B14 DQ2_1
DDR3_DQ<11> C14 DQ3_1
DDR3_DQ<12> D14 DQ4_1
DDR3_DQ<13> E14 DQ5_1
DDR3_DQ<14> B13 DQ6_1
DDR3_DQ<15> C13 DQ7_1
DDR3_DQ<0> C9 DQ8_1
DDR3_DQ<1> D9 DQ9_1
DDR3_DQ<2> B8 DQ10_1
DDR3_DQ<3> C8 DQ11_1
DDR3_DQ<4> D8 DQ12_1
DDR3_DQ<5> E8 DQ13_1
DDR3_DQ<6> B7 DQ14_1
DDR3_DQ<7> C7 DQ15_1
DDR3_DQ<24> B18 DQ16_1
DDR3_DQ<25> C18 DQ17_1
DDR3_DQ<26> D18 DQ18_1
DDR3_DQ<27> E18 DQ19_1
DDR3_DQ<28> B17 DQ20_1
DDR3_DQ<29> D17 DQ21_1
DDR3_DQ<30> E17 DQ22_1
DDR3_DQ<31> E16 DQ23_1
DDR3_DQ<16> B6 DQ24_1
DDR3_DQ<17> B5 DQ25_1
DDR3_DQ<18> C5 DQ26_1
DDR3_DQ<19> D5 DQ27_1
DDR3_DQ<20> B4 DQ28_1
DDR3_DQ<21> C4 DQ29_1
DDR3_DQ<22> B3 DQ30_1
DDR3_DQ<23> C3 DQ31_1
DDR3_DQS_P<1> D13 DQS0_1
DDR3_DQS_N<1> D12 DQSB0_1
DDR3_DQS_P<0> D10 DQS1_1
DDR3_DQS_N<0> C10 DQSB1_1
DDR3_DQS_P<3> C16 DQS2_1
DDR3_DQS_N<3> D16 DQSB2_1
DDR3_DQS_P<2> D6 DQS3_1
DDR3_DQS_N<2> C6 DQSB3_1
PPVREF_DDR3_CA U10 VREFCA_1
PPVREF_DDR3_DQ D11 VREFDQ_1
DDR3_ZQ U7 ZQ_1
R1420 240 1% 1/20W MF 201
CA0_2 G16 DDR2_CA<0>
CA1_2 G17 DDR2_CA<1>
CA2_2 H17 DDR2_CA<2>
CA3_2 H18 DDR2_CA<3>
CA4_2 J16 DDR2_CA<4>
CA5_2 N16 DDR2_CA<5>
CA6_2 N17 DDR2_CA<6>
CA7_2 P17 DDR2_CA<7>
CA8_2 P18 DDR2_CA<8>
CA9_2 R16 DDR2_CA<9>
CK_2 K17 DDR2_CK_P
CKB_2 L17 DDR2_CK_N
CKE_2 J18 DDR2_CKE<0>
CSB_2 J17 DDR2_CSN<0>
DM0_2 K3 DDR2_DM<1>
DM1_2 M2 DDR2_DM<0>
DM2_2 G4 DDR2_DM<3>
DM3_2 T2 DDR2_DM<2>
DQ0_2 G3 DDR2_DQ<8>
DQ1_2 G2 DDR2_DQ<9>
DQ2_2 H5 DDR2_DQ<10>
DQ3_2 H4 DDR2_DQ<11>
DQ4_2 H3 DDR2_DQ<12>
DQ5_2 H2 DDR2_DQ<13>
DQ6_2 J3 DDR2_DQ<14>
DQ7_2 J2 DDR2_DQ<15>
DQ8_2 N4 DDR2_DQ<0>
DQ9_2 N3 DDR2_DQ<1>
DQ10_2 P5 DDR2_DQ<2>
DQ11_2 P4 DDR2_DQ<3>
DQ12_2 P3 DDR2_DQ<4>
DQ13_2 P2 DDR2_DQ<5>
DQ14_2 R4 DDR2_DQ<6>
DQ15_2 R3 DDR2_DQ<7>
DQ16_2 B2 DDR2_DQ<24>
DQ17_2 C2 DDR2_DQ<25>
DQ18_2 D3 DDR2_DQ<26>
DQ19_2 D2 DDR2_DQ<27>
DQ20_2 E4 DDR2_DQ<28>
DQ21_2 E3 DDR2_DQ<29>
DQ22_2 E2 DDR2_DQ<30>
DQ23_2 F2 DDR2_DQ<31>
DQ24_2 T5 DDR2_DQ<16>
DQ25_2 U5 DDR2_DQ<17>
DQ26_2 U4 DDR2_DQ<18>
DQ27_2 U2 DDR2_DQ<19>
DQ28_2 V5 DDR2_DQ<20>
DQ29_2 V4 DDR2_DQ<21>
DQ30_2 V3 DDR2_DQ<22>
DQ31_2 V2 DDR2_DQ<23>
DQS0_2 J4 DDR2_DQS_P<1>
DQSB0_2 K4 DDR2_DQS_N<1>
DQS1_2 M4 DDR2_DQS_P<0>
DQSB1_2 M3 DDR2_DQS_N<0>
DQS2_2 F4 DDR2_DQS_P<3>
DQSB2_2 F3 DDR2_DQS_N<3>
DQS3_2 T3 DDR2_DQS_P<2>
DQSB3_2 T4 DDR2_DQS_N<2>
VREFCA_2 M17 PPVREF_DDR2_CA
VREFDQ_2 L4 PPVREF_DDR2_DQ
ZQ_2 R17 DDR2_ZQ
R1421 240 1% 1/20W MF 201
=PP1V8_S2R_DDR
C1401 10UF 20% 6.3V X5R 603
C1402 1UF 10% 6.3V CERM 402
C1403 1UF 10% 6.3V CERM 402
C1404 0.01UF 10% 16V X5R 01005
C1405 0.01UF 10% 6.3V X5R 01005
C1406 0.22UF 20% 6.3V X5R 0201
C1407 0.22UF 20% 6.3V X5R 0201
C1408 0.22UF 20% 6.3V X5R 0201
C1409 56PF 5% 6.3V NPO-C0G 01005
=PP1V2_S2R_DDR
C1410 0.22UF 20% 6.3V X5R 0201
C1411 0.22UF 20% 6.3V X5R 0201
C1412 0.22UF 20% 6.3V X5R 0201
C1413 0.22UF 20% 6.3V X5R 0201
C1414 10UF 20% 6.3V X5R 603
C1415 4.3UF 20% 4V X5R-CERM 0610
C1416 1UF 10% 6.3V CERM 402
C1417 1UF 10% 6.3V CERM 402
C1418 0.01UF 10% 10V X5R-CERM 0201
C1419 56PF 5% 6.3V NPO-C0G 01005
=PP1V2_VDDQ_DDR
C1423 56PF 5% 6.3V NPO-C0G 01005
C1420 10UF 20% 6.3V X5R 603
C1421 4.3UF 20% 4V X5R-CERM 0610
C1424 0.22UF 20% 6.3V X5R 0201
C1425 0.22UF 20% 6.3V X5R 0201
C1426 0.22UF 20% 6.3V X5R 0201
C1422 0.01UF 10% 6.3V X5R 01005
=PP1V2_S2R_DDR
C1427 10UF 20% 6.3V X5R 603
C1428 1UF 10% 6.3V CERM 402
C1429 1UF 10% 6.3V CERM 402
C1430 0.01UF 10% 6.3V X5R 01005
C1431 0.01UF 10% 6.3V X5R 01005
C1432 0.22UF 20% 6.3V X5R 0201
C1433 0.22UF 20% 6.3V X5R 0201
C1434 0.22UF 20% 6.3V X5R 0201
C1435 56PF 5% 6.3V NPO-C0G 01005
U1400
H4G-DRAM
XXXMB
BGA
SYM 2 OF 2
OMIT_TABLE
A2 VDD1_0
B1 VDD1_1
B11 VDD1_2
F17 VDD1_3
L2 VDD1_4
M16 VDD1_5
T10 VDD1_6
U18 VDD1_7
V17 VDD1_8
V6 VDD1_9
W17 VDD1_10
U19 VDD1_11
VDD1
E11 VDD2_1
E19 VDD2_2
L5 VDD2_3
M18 VDD2_4
U17 VDD2_5
T18 VDD2_6
V10 VDD2_7
V16 VDD2_8
V18 VDD2_9
W5 VDD2_10
W16 VDD2_11
W19 VDD2_12
W18 VDD2_13
V19 VDD2_14
A3 VDD2_15
T19 VDD2_16
VDD2
H1 VDDQ27
M1 VDDQ32
W3 VDDQ31
E1 VDDQ
U1 VDDQ1
B12 VDDQ3
D4 VDDQ6
U3 VDDQ30
A14 VDDQ23
C17 VDDQ25
C19 VDDQ26
A10 VDDQ22
A17 VDDQ34
J5 VDDQ16
K2 VDDQ17
A8 VDDQ21
N2 VDDQ19
R5 VDDQ20
A13 VDDQ24
E10 VDDQ28
E15 VDDQ29
P1 VDDQ33
VDDQ
F18 VDDCA1
H16 VDDCA2
K16 VDDCA3
L16 VDDCA4
P16 VDDCA5
T11 VDDCA6
T12 VDDCA7
T14 VDDCA8
V7 VDDCA9
T8 VDDCA10
VDDCA
VSS0 A16
VSS55 A19
VSS2 A4
VSS3 A6
VSS4 B15
VSS49 C1
VSS6 B9
VSS7 C11
VSS9 D1
VSS10 D19
VSS1 A1
VSS12 E12
VSS13 E13
VSS51 G5
VSS52 T16
VSS50 E7
VSS18 F16
VSS48 B19
VSS20 G18
VSS53 V1
VSS22 J1
VSS23 K18
VSS24 K5
VSS25 L18
VSS26 L3
VSS27 M5
VSS28 N18
VSS29 N5
VSS47 A18
VSS32 R18
VSS33 R2
VSS34 T1
VSS35 T17
VSS36 U16
VSS54 W2
VSS39 U6
VSS40 V11
VSS41 V12
VSS42 V15
VSS43 T6
VSS44 V9
VSS45 W1
VSS46 W4
VSS
SYNC_MASTER=N/A
SYNC_DATE=N/A
PAGE TITLE
DDR 2 AND 3
Apple Inc.
DRAWING NUMBER 051-9385
SIZE D
REVISION A.0.0
BRANCH
PAGE 14 OF 154
SHEET 12 OF 39
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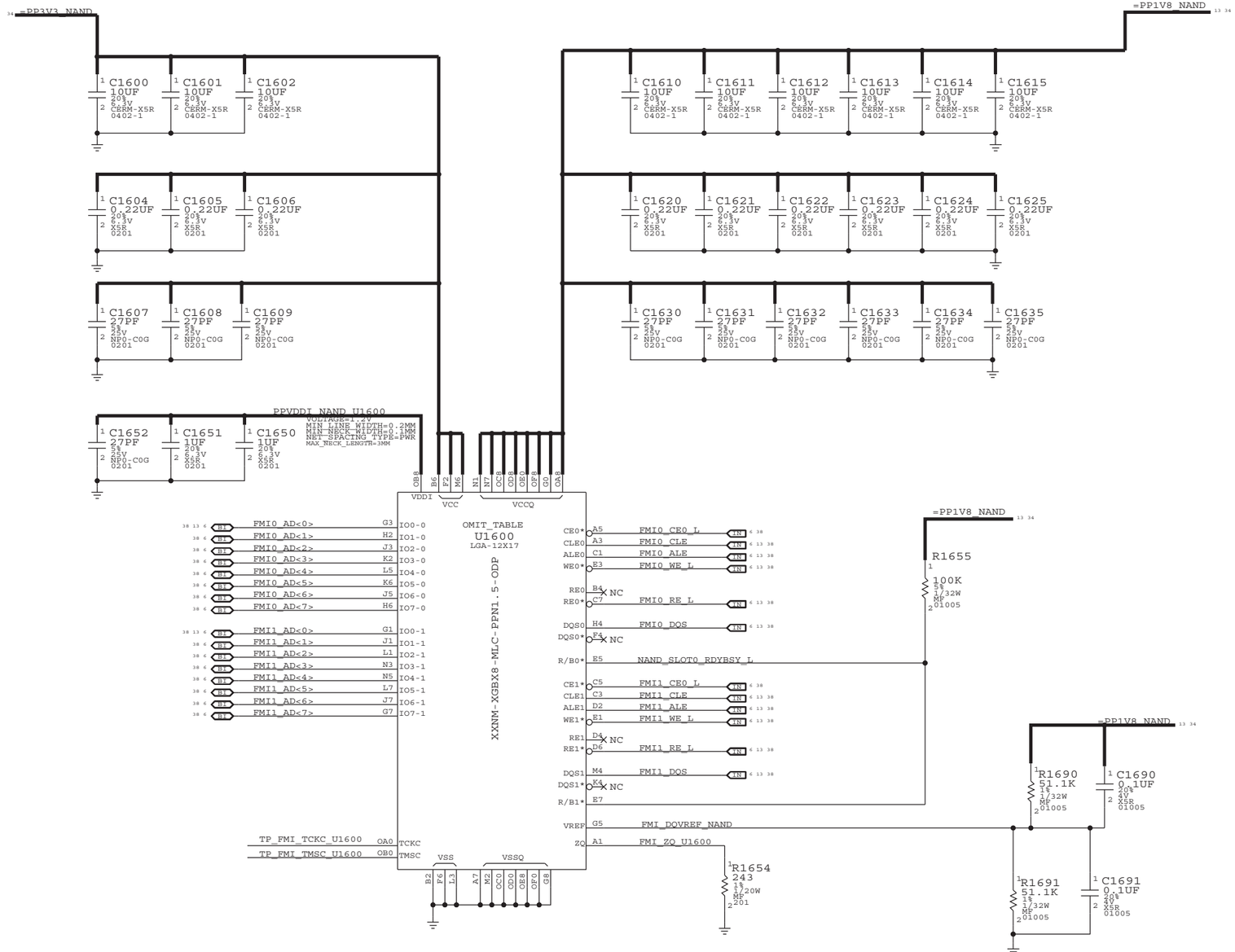
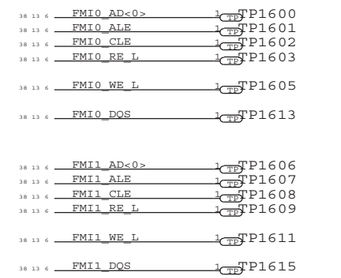


TEST POINTS

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA



SYNC MASTER=N/A	SYNC DATE=N/A
PAGE TITLE	NAND
Apple Inc.	DRAWING NUMBER 051-9385 SIZE D
	REVISION A.0.0
	BRANCH
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WIFI ALIASES

36 4	HSIC1_WLAN_DATA	MAKE_BASE=TRUE	50_HSIC_WLAN_DATA	27
36 4	HSIC1_WLAN_STB	MAKE_BASE=TRUE	50_HSIC_WLAN_STROBE	27
36 5	GPIO_WLAN_HSIC_HOST_RDY	MAKE_BASE=TRUE	AP_HSIC3_RDY	27
36 5	GPIO_WLAN_HSIC_DEV_RDY	MAKE_BASE=TRUE	DEV_HSIC3_RDY	27
30	PMU_GPIO_WLAN_REG_ON	MAKE_BASE=TRUE	WLAN_REG_ON	27
30	PMU_GPIO_WLAN_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_WLAN	27
30	PMU_GPIO_BT_REG_ON	MAKE_BASE=TRUE	BT_REG_ON	27
30	PMU_GPIO_BT_HOST_WAKE	MAKE_BASE=TRUE	HOST_WAKE_BT	27
5	GPIO_BT_WAKE	MAKE_BASE=TRUE	BT_WAKE	27
36 5	UART3_BT_RXD	MAKE_BASE=TRUE	BT_UART_TXD	27
36 5	UART3_BT_TXD	MAKE_BASE=TRUE	BT_UART_RXD	27
36 5	UART3_BT_CTS_L	MAKE_BASE=TRUE	BT_UART_RTS_L	27
36 5	UART3_BT_RTS_L	MAKE_BASE=TRUE	BT_UART_CTS_L	27
36 30	PMU_GPIO_CLK_32K_WLAN	MAKE_BASE=TRUE	CLK32K_AP	27
36 5	I2S2_BT_BCLK	MAKE_BASE=TRUE	BT_PCM_CLK	27
36 5	I2S2_BT_DOUT	MAKE_BASE=TRUE	BT_PCM_IN	27
36 5	I2S2_BT_DIN	MAKE_BASE=TRUE	BT_PCM_OUT	27
36 5	I2S2_BT_LRCK	MAKE_BASE=TRUE	BT_PCM_SYNC	27
36 5	UART4_WLAN_RXD	MAKE_BASE=TRUE	WLAN_UART_TXD	27
36 5	UART4_WLAN_TXD	MAKE_BASE=TRUE	WLAN_UART_RXD	27
5	GPIO_WL_HSIC_RESUME	MAKE_BASE=TRUE	WLAN_HSIC3_RESUME	27
34	VDDIO_WLAN_BT_1V8	MAKE_BASE=TRUE	PP_WL_BT_VDDIO_AP	27

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

ALIASES

Apple Inc.

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EDP CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0667	155S0583		L2242,L5500,L5510,L5520,L5530,L5540,L5930,L5931	RDAR://PROBLEM/8616060, RADAR://PROBLEM/9015335
155S0625	155S0559		L2202,L2212,L2222,L2232	RDAR://PROBLEM/9017591

=PP3V3_LCD

PPVCC_MAIN

C2240 0.1UF 10% 6.3V X5R 201

C2239 0.1UF 10% 6.3V X5R 201

U2200 SLG5AP302 TDFN CRITICAL

VDD CAP ON GND D S

LCD_RAMP

IN PM_LCDVDD_PWREN

R2205 100K 1% 1/20W MF 201

C2241 3900PF 10% 50V X7R 0402

LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

PP3V3_S0_LCD_FERR

C2203 0.1UF 10% 6.3V X5R 201

C2202 1UF 10% 6.3V CERM 402

NOSTUFF R2290 47K 5% 1/20W MF 201

C2230 82PF 5% 25V NPO-C0G-CERM 0201

CRITICAL L2201 FERR-120-OHM-1.5A 0402A

C2232 8.2PF +/-0.1PF% 25V C0G 0201

C2206 1000PF 10% 16V X7R-CERM 0201

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

PP3V3_LCDVDD_SW_F

518S0827
CRITICAL
J2200
502250-8051-B
F-RT-SM

R2242 100K 1% 1/32W MF 01005

EDP_HPD

NCX NC

CONN_EDP_AUX_EMI_P

CONN_EDP_AUX_EMI_N

CONN_EDP_DATA_EMI_N<0>

CONN_EDP_DATA_EMI_P<0>

CONN_EDP_DATA_EMI_N<1>

CONN_EDP_DATA_EMI_P<1>

CONN_EDP_DATA_EMI_N<2>

CONN_EDP_DATA_EMI_P<2>

CONN_EDP_DATA_EMI_N<3>

CONN_EDP_DATA_EMI_P<3>

J2200_29_GND

J2200_36_GND

J2200_43_GND

LED_IO_5_B
LED_IO_3_B
LED_IO_1_B
LED_IO_6_A
LED_IO_4_A
LED_IO_2_A

LED_IO_6_B
LED_IO_4_B
LED_IO_2_B
LED_IO_5_A
LED_IO_3_A
LED_IO_1_A

R2280 1.00M 1% 1/32W MF 01005
C2280 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_N<0>

R2281 1.00M 1% 1/32W MF 01005
C2281 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_P<0>

R2282 1.00M 1% 1/32W MF 01005
C2282 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_N<1>

R2283 1.00M 1% 1/32W MF 01005
C2283 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_P<1>

R2284 1.00M 1% 1/32W MF 01005
C2284 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_N<2>

R2285 1.00M 1% 1/32W MF 01005
C2285 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_P<2>

R2286 1.00M 1% 1/32W MF 01005
C2286 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_N<3>

R2287 1.00M 1% 1/32W MF 01005
C2287 1.2PF +/-0.1PF 16V NPO-C0G 01005 NOSTUFF
CONN_EDP_DATA_EMI_P<3>

PP3V3_S0_LCD_FERR

R2240 100K 1% 1/32W MF 01005

R2241 100K 1% 1/32W MF 01005

EDP_AUX_N → C2250 0.1UF 10% X5R 201 6.3V → EDP_AUX_EMI_N → CRITICAL L2242 90-OHM-50MA TCM0605-1 → CONN_EDP_AUX_EMI_N

EDP_AUX_P → C2251 0.1UF 10% X5R 201 6.3V → EDP_AUX_EMI_P → SYM_VER-2 → CONN_EDP_AUX_EMI_P

EDP_DATA_N<0> → C2242 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_N<0> → CRITICAL → CONN_EDP_DATA_EMI_N<0>

EDP_DATA_P<0> → C2243 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_P<0> → TCM0806-4SM 12-OHM-100MA-8.5GHZ L2212 → CONN_EDP_DATA_EMI_P<0>

EDP_DATA_N<1> → C2244 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_N<1> → CRITICAL → CONN_EDP_DATA_EMI_N<1>

EDP_DATA_P<1> → C2245 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_P<1> → TCM0806-4SM 12-OHM-100MA-8.5GHZ L2222 → CONN_EDP_DATA_EMI_P<1>

EDP_DATA_N<2> → C2246 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_N<2> → CRITICAL → CONN_EDP_DATA_EMI_N<2>

EDP_DATA_P<2> → C2247 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_P<2> → TCM0806-4SM 12-OHM-100MA-8.5GHZ L2232 → CONN_EDP_DATA_EMI_P<2>

EDP_DATA_N<3> → C2248 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_N<3> → CRITICAL → CONN_EDP_DATA_EMI_N<3>

EDP_DATA_P<3> → C2249 0.1UF 10% X5R 201 6.3V → EDP_DATA_EMI_P<3> → TCM0806-4SM 12-OHM-100MA-8.5GHZ L2202 → CONN_EDP_DATA_EMI_P<3>

R2295 0 5% 1/20W MF 201 J2200_29_GND

R2296 0 5% 1/20W MF 201 J2200_36_GND

R2297 0 5% 1/20W MF 201 J2200_43_GND

CRITICAL L2210 FERR-240-OHM-25%-300MA 0402
=PPLED_REG_B → PPLED_BACK_REG_B
VOLTAGE=20.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

C2253 100PF 5% 50V C0G 0402

C2270 820PF 10% 50V C0G 0402

C2271 8.2PF +/-0.25PF 50V C0G 402-1

CRITICAL L2200 FERR-240-OHM-25%-300MA 0402
=PPLED_REG_A → PPLED_BACK_REG_A
VOLTAGE=20.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

C2233 100PF 5% 50V C0G 0402

C2220 820PF 10% 50V C0G 0402

C2221 8.2PF +/-0.25PF 50V C0G 402-1

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
VIDEO: EDP CONNECTOR

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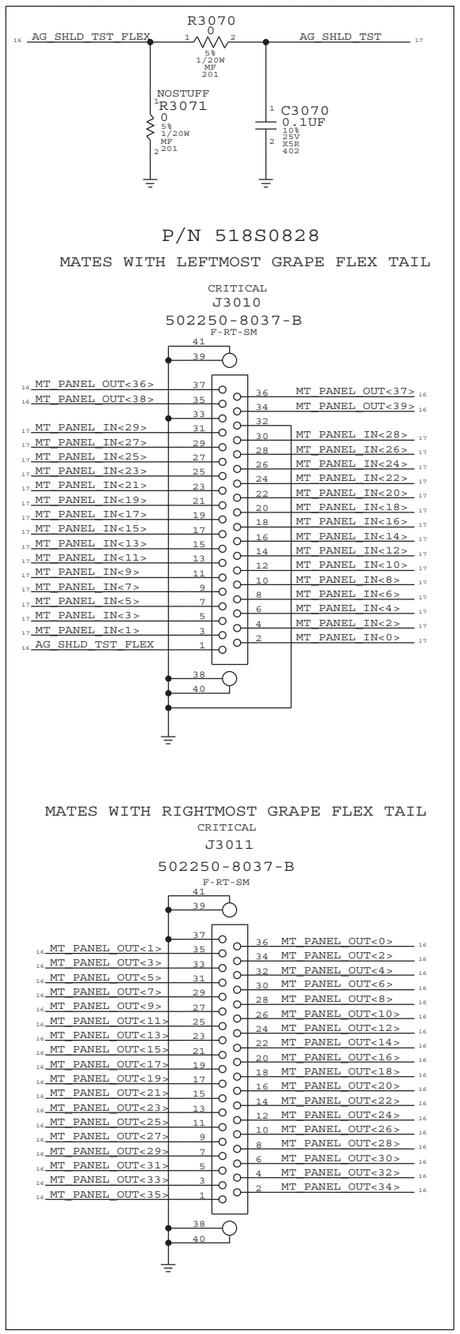
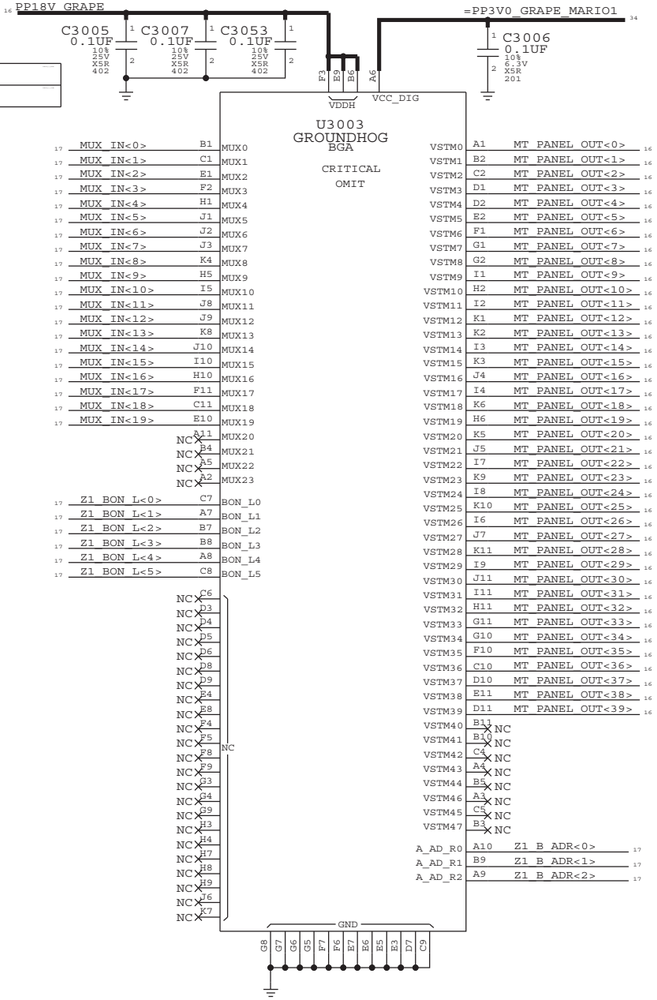
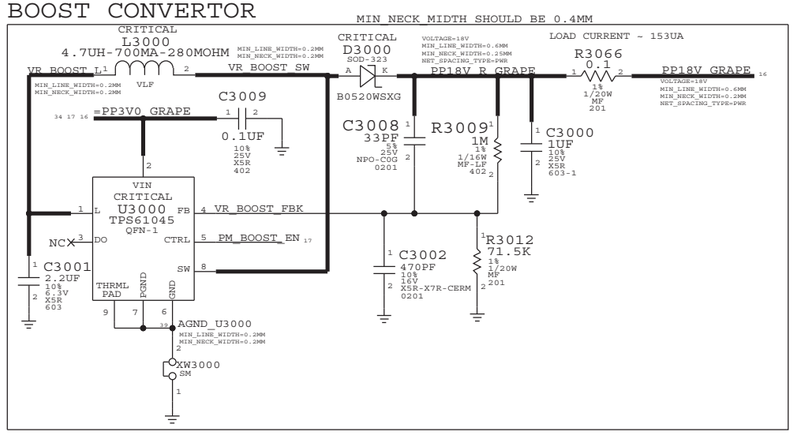
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

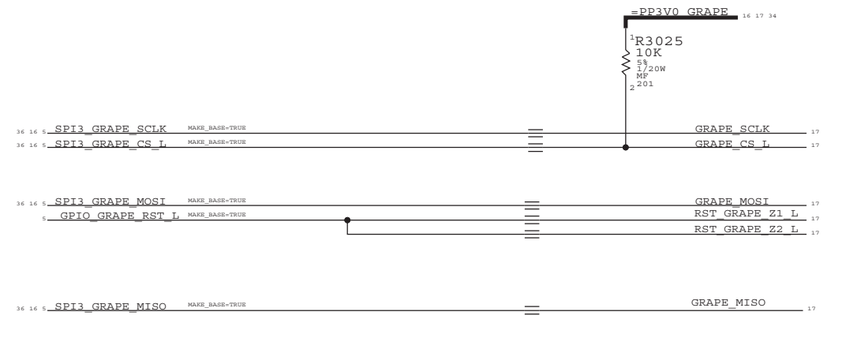
CONNECTORS TO GRAPE FLEX

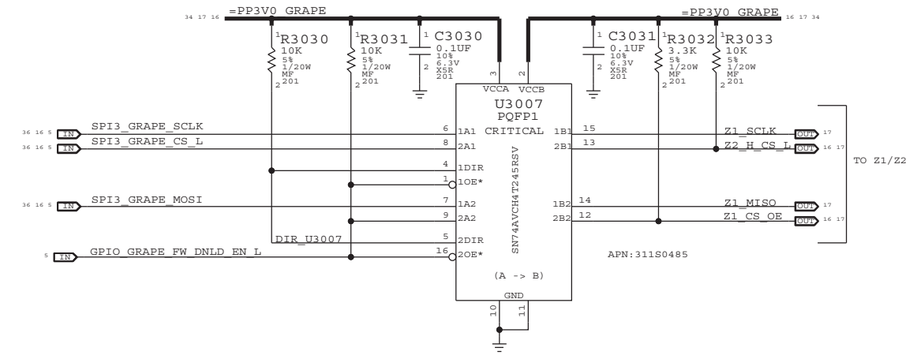


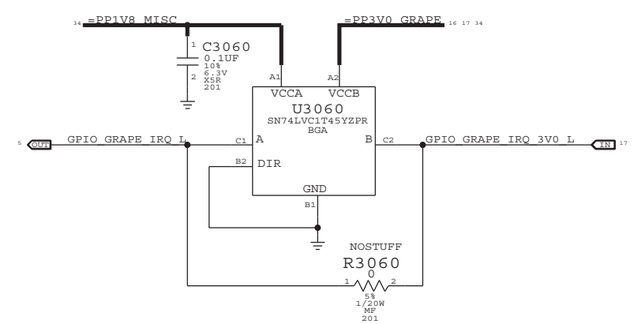


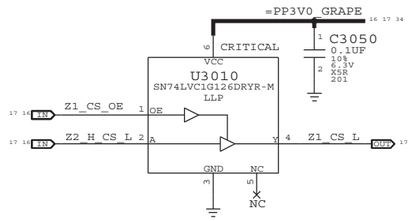
BOOST CONVERTOR

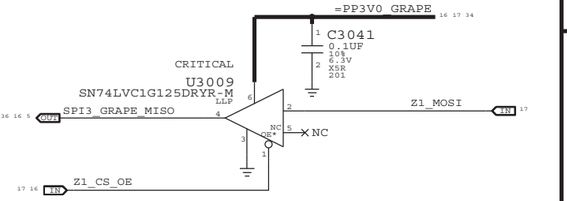












PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

GRAPE: GROUNDHOG,CONN,BOOST

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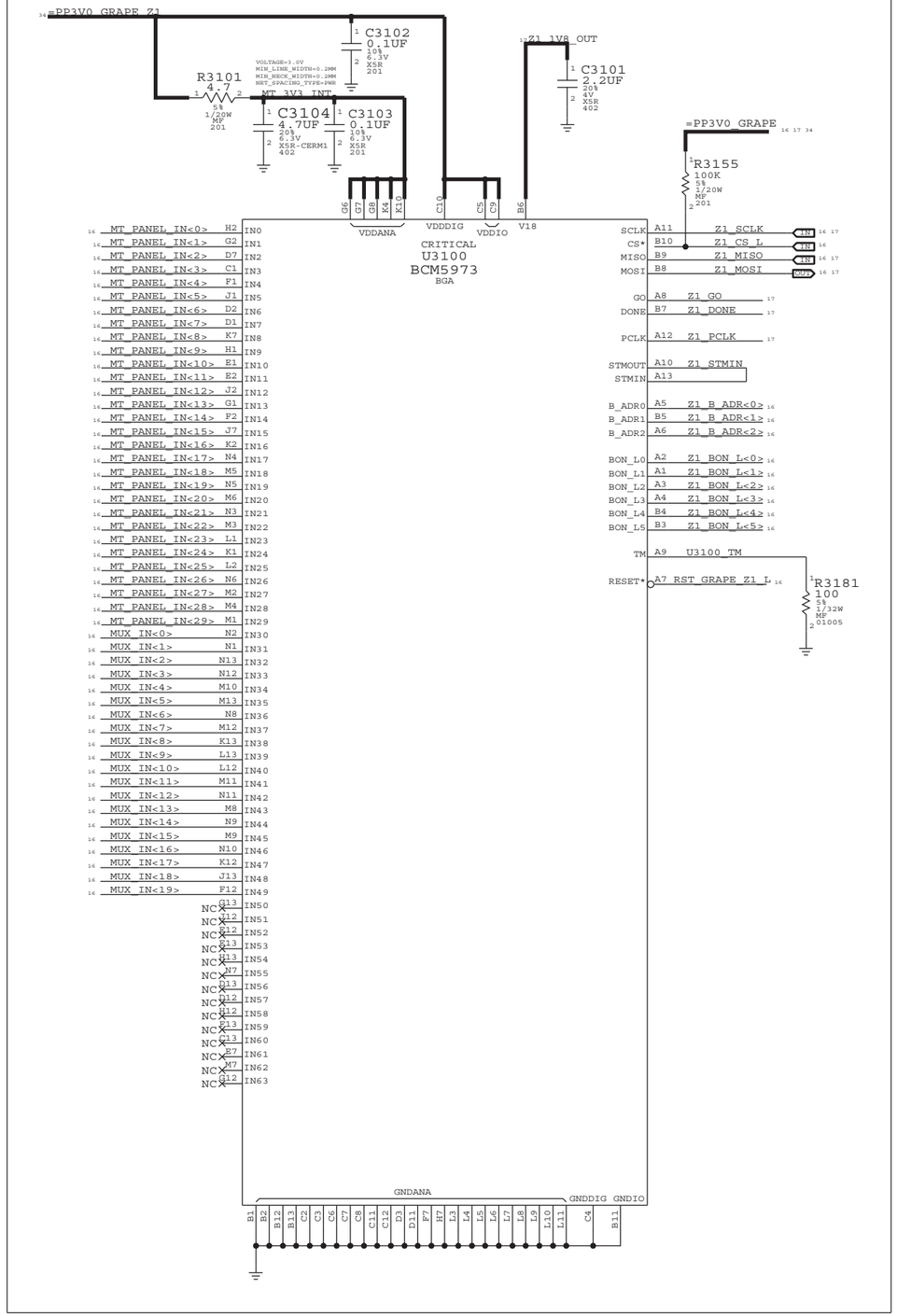
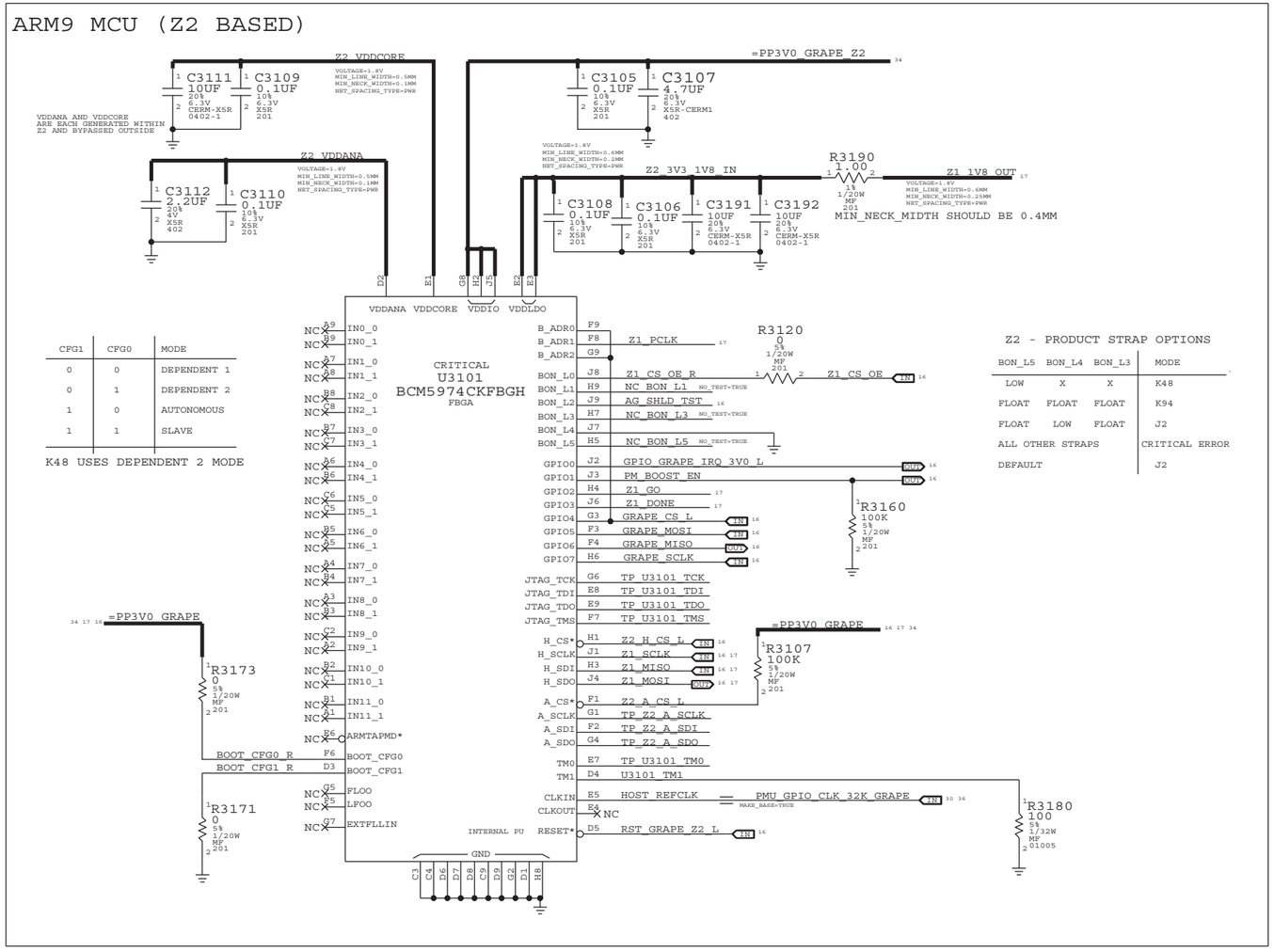
ZEPHYR 1+ ASIC



ARM9 MCU (Z2 BASED)



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

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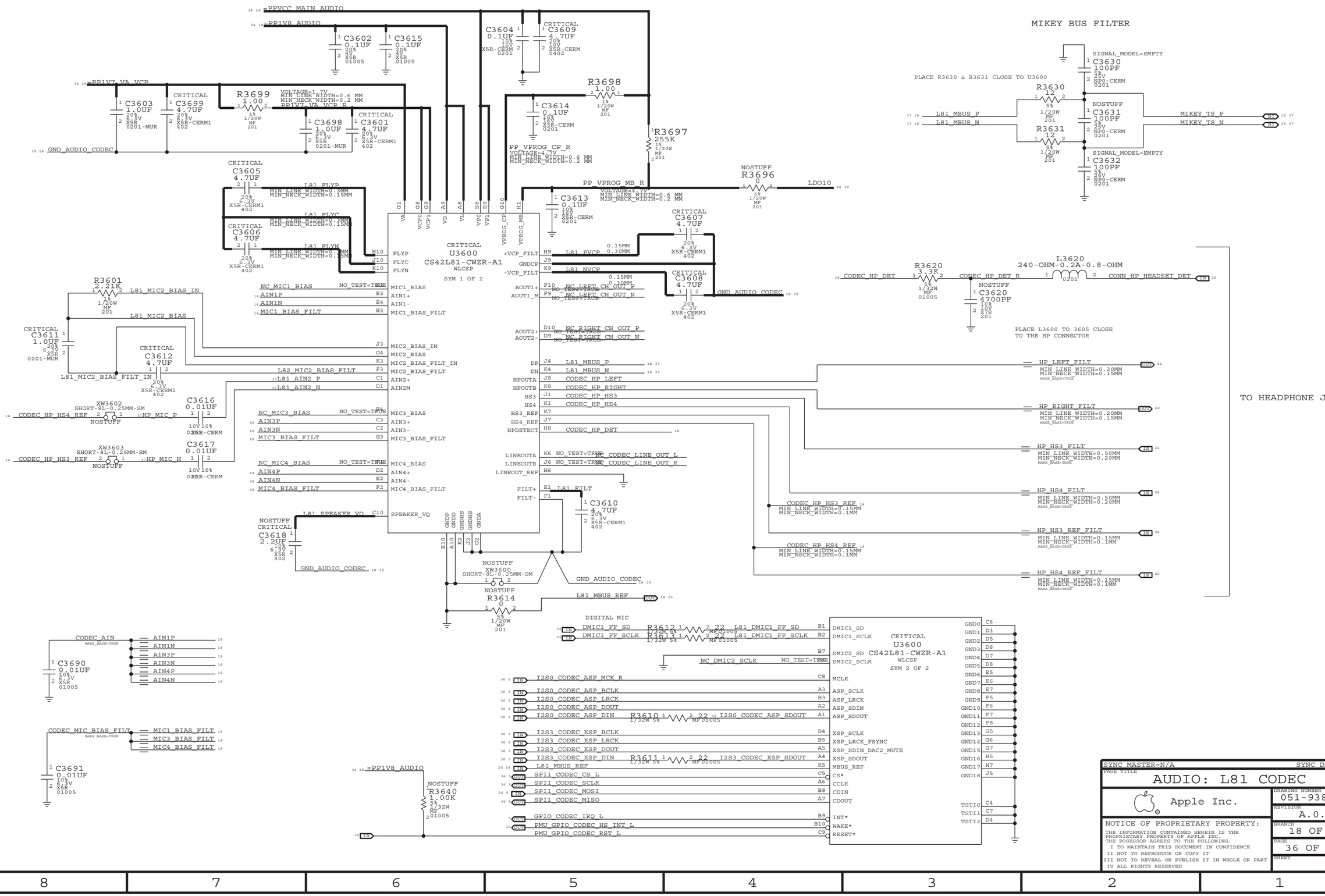
MIKEY BUS FILTER
PLACE R3630 & R3631 CLOSE TO U3600
PLACE L3600 TO 3605 CLOSE TO THE HP CONNECTOR
TO HEADPHONE JACK
CRITICAL U3600 CS42L81-CWZR-A1 WLCSP SYM 1 OF 2
CRITICAL U3600 CS42L81-CWZR-A1 WLCSP SYM 2 OF 2
DIGITAL MIC
SYNC_MASTER=N/A
SYNC_DATE=N/A
PAGE TITLE
AUDIO: L81 CODEC
Apple Inc.
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LEFT SPEAKER AMP

I2C ADDRESS: 1000000X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0002	4	RES,MF,1/20W,0.00HM,5,0201,SMD	R3742,R3743,R3752,R3753	?	?
113S0022	4	RES,MF,1/10W,00HM,5,0603,SMD,LF	FL3740,FL3741,FL3750,FL3751	?	?

=PBVCC_MAIN_AUDIO

CRITICAL C3741 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3742 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3743 4.7UF 20% 10V X5R-CERM 0402
C3744 0.1UF 10% 16V X5R-CERM 0201

L19_L_VBOOST
CRITICAL C3745 22UF 20% 10V X5R-CERM 0603-1
CRITICAL C3710 22UF 20% 10V X5R-CERM 0603-1
C3711 0.1UF 10% 16V X5R-CERM 0201
C3712 27PF 5% 16V NP0-C0G 01005

=PP1V7_VA_VCP 18 19 34
C3713 27PF 5% 16V NP0-C0G 01005
C3746 0.1UF 10% 6.3V X5R 201

C3747 4.7UF 20% 6.3V X5R-CERM1 402
C3748 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3740 2.2UH-20%-3.3A-0.115OHM TFA302610A-SM
L19_L_SWITCH

CRITICAL U3740 CS35L19B-CWZR WLCSP VER1

A1	VBST	
B1	SW	
C1	VP	
D1	VA	
A4		
A5		
F5		
A2		
B2		
D5	SDA	I2C0_SDA_1V8 (36 30 25 19 5)
D6	SCL	I2C0_SCL_1V8 (36 30 25 19 5)
A7	INT*	GPIO_SPKAMP_LEFT_IRQ_L (5)
A6	RESET*	GPIO_SPKAMP_RST_L (19 5)
D7	ALIVE	GPIO_SPKAMP_KEEPALIVE (19 5)
C7	ADO	PP1V7_VA_VCP (39 34 29)
E7	MCLK	I2S1_SPKAMP_MCK_R (19 5)
E6	SCLK	I2S1_SPKAMP_BCLK (19 5)
F6	LRCK/FSYNC	I2S1_SPKAMP_LRCK (19 5)
F7	SDIN	I2S1_SPKAMP_DOUT (19 5)
E5	SDOUT	I2S1_SPKAMP_DIN (19 5)
F2	FILT+	L19_L_FILT
C5	LDO_FILT	L19_L_LDO_FILT
E3	VSENSE-	SPKR_L_VSENSE_N_FILT (37)
E2	VSENSE+	SPKR_L_VSENSE_P_FILT (37)
F1	ISENSE-	SPKR_L_SES_N (37)
E1	ISENSE+	SPKR_L_SES_P (37)
D2	OUT+	SPKR_L_P (37)
C2	OUT-	SPKR_L_N (37)
B7	IREF*	L19_L_IREF
A3, B3, B4, C3, C4, D3, D4	GNDP	
B5, B6, C6, E4, F3, F4	GNDA	

R3741 44.2K 1% 1/20W MF 201

NOSTUFF C3760 0.01UF 10% 10V X5R-CERM 0201

OMIT_TABLE R3743 10 5% 1/20W MF 201
OMIT_TABLE R3742 10 5% 1/20W MF 201
CRITICAL R3740 0.100 1% 1/2W MF 0805

OMIT_TABLE CRITICAL FL3741 220-OHM-2.0A 0603
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM

SPKR_L_FLT
SPKR_L_CONN_P (19 37)

NOSTUFF C3761 18PF 5% 25V NP0-C0G-CERM 0201
C3740 8.2PF +/-0.1PF 25V CER 0201
NOSTUFF C3763 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201

OMIT_TABLE CRITICAL FL3740 220-OHM-2.0A 0603
SPKR_L_CONN_N (19 37)

NOSTUFF C3764 18PF 5% 25V NP0-C0G-CERM 0201
C3749 8.2PF +/-0.1PF 25V CER 0201
NOSTUFF C3766 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201

R3745 10K 5% 1/20W MF 201 SPKR_L_VSENSE_N (19 37)
R3744 10K 5% 1/20W MF 201 SPKR_L_VSENSE_P (19 37)

NOSTUFF C3767 100PF 5% 25V NP0-CERM 0201
NOSTUFF C3768 100PF 5% 25V NP0-CERM 0201

RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X

=PBVCC_MAIN_AUDIO

CRITICAL C3751 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3752 4.7UF 20% 10V X5R-CERM 0402
CRITICAL C3753 4.7UF 20% 10V X5R-CERM 0402
C3754 0.1UF 10% 16V X5R-CERM 0201

L19_R_VBOOST
CRITICAL C3755 22UF 20% 10V X5R-CERM 0603-1
CRITICAL C3720 22UF 20% 10V X5R-CERM 0603-1
C3721 0.1UF 10% 16V X5R-CERM 0201
C3722 27PF 5% 16V NP0-C0G 01005

=PP1V7_VA_VCP 18 19 34
C3723 27PF 5% 16V NP0-C0G 01005
C3756 0.1UF 10% 6.3V X5R 201

C3757 4.7UF 20% 6.3V X5R-CERM1 402
C3758 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3750 2.2UH-20%-3.3A-0.115OHM TFA302610A-SM
L19_R_SWITCH

CRITICAL U3750 CS35L19B-CWZR WLCSP VER1

A1	VBST	
B1	SW	
C1	VP	
D1	VA	
A4		
A5		
F5		
A2		
B2		
D5	SDA	I2C0_SDA_1V8 (36 30 25 19 5)
D6	SCL	I2C0_SCL_1V8 (36 30 25 19 5)
A7	INT*	GPIO_SPKAMP_RIGHT_IRQ_L (5)
A6	RESET*	GPIO_SPKAMP_RST_L (19 5)
D7	ALIVE	GPIO_SPKAMP_KEEPALIVE (19 5)
C7	ADO	PP1V7_VA_VCP (39 34 29)
E7	MCLK	I2S1_SPKAMP_MCK_R (19 5)
E6	SCLK	I2S1_SPKAMP_BCLK (19 5)
F6	LRCK/FSYNC	I2S1_SPKAMP_LRCK (19 5)
F7	SDIN	I2S1_SPKAMP_DOUT (19 5)
E5	SDOUT	I2S1_SPKAMP_DIN (19 5)
F2	FILT+	L19_R_FILT
C5	LDO_FILT	L19_R_LDO_FILT
E3	VSENSE-	SPKR_R_VSENSE_N_FILT (37)
E2	VSENSE+	SPKR_R_VSENSE_P_FILT (37)
F1	ISENSE-	SPKR_R_SES_N (37)
E1	ISENSE+	SPKR_R_SES_P (37)
D2	OUT+	SPKR_R_P (37)
C2	OUT-	SPKR_R_N (37)
B7	IREF*	L19_R_IREF
A3, B3, B4, C3, C4, D3, D4	GNDP	
B5, B6, C6, E4, F3, F4	GNDA	

R3751 44.2K 1% 1/20W MF 201

NOSTUFF C3780 0.01UF 10% 10V X5R-CERM 0201

OMIT_TABLE R3753 10 5% 1/20W MF 201
OMIT_TABLE R3752 10 5% 1/20W MF 201
CRITICAL R3750 0.100 1% 1/2W MF 0805

OMIT_TABLE CRITICAL FL3751 220-OHM-2.0A 0603
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM

SPKR_R_FLT
SPKR_R_CONN_P (19 37)

NOSTUFF C3781 18PF 5% 25V NP0-C0G-CERM 0201
C3750 8.2PF +/-0.1PF 25V CER 0201
NOSTUFF C3783 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201

OMIT_TABLE CRITICAL FL3750 220-OHM-2.0A 0603
SPKR_R_CONN_N (19 37)

NOSTUFF C3784 18PF 5% 25V NP0-C0G-CERM 0201
C3759 8.2PF +/-0.1PF 25V CER 0201
NOSTUFF C3786 3.9PF +/-0.1PF 25V NP0-C0G-CERM 0201

R3755 10K 5% 1/20W MF 201 SPKR_R_VSENSE_N (19 37)
R3754 10K 5% 1/20W MF 201 SPKR_R_VSENSE_P (19 37)

NOSTUFF C3787 100PF 5% 25V NP0-CERM 0201
NOSTUFF C3788 100PF 5% 25V NP0-CERM 0201

SPEAKER CONNECTOR

APN 518S0672
CRITICAL J3700 78171-6006 M-RT-SM

1	SPKR_L_CONN_P	(37 19)
2	SPKR_L_VSENSE_P	(37 19)
3	SPKR_L_CONN_N	(37 19)
4	SPKR_L_VSENSE_N	(37 19)
5	SPK_ID	(5 OUT)
6	SPKR_R_CONN_P	(37 19)
7	SPKR_R_VSENSE_P	(37 19)
8	SPKR_R_CONN_N	(37 19)
	SPKR_R_VSENSE_N	(37 19)

XW3774 SM SIGNAL_MODEL=EMPTY
XW3775 SM SIGNAL_MODEL=EMPTY
XW3776 SM SIGNAL_MODEL=EMPTY
XW3777 SM SIGNAL_MODEL=EMPTY

PLACE XWS CLOSE TO CONNECTOR

NOSTUFF CRITICAL C3770 100PF 5% 16V NP0-C0G 01005
NOSTUFF CRITICAL C3771 100PF 5% 16V NP0-C0G 01005
NOSTUFF CRITICAL C3772 100PF 5% 16V NP0-C0G 01005
NOSTUFF CRITICAL C3773 100PF 5% 16V NP0-C0G 01005

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

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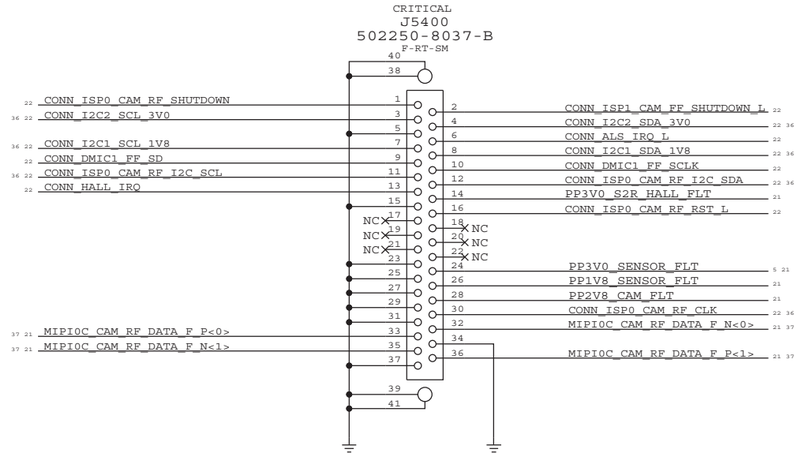
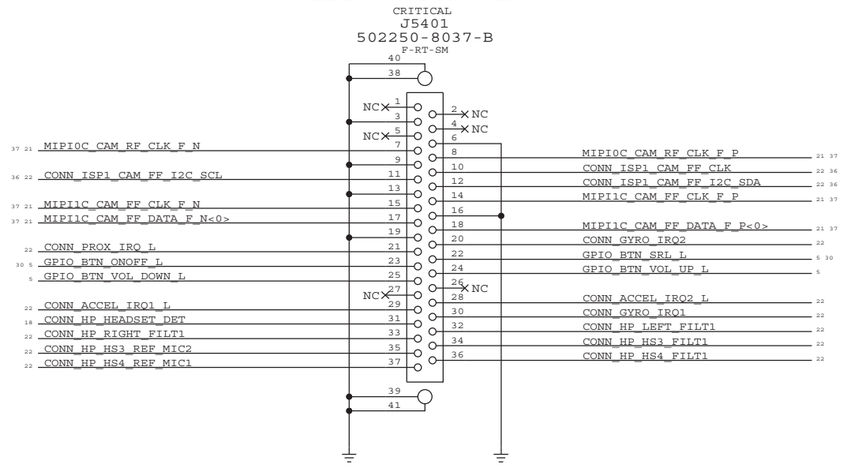
APN: 518S0828



APN: 518S0828



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SENSOR FLEX CONN

Apple Inc.

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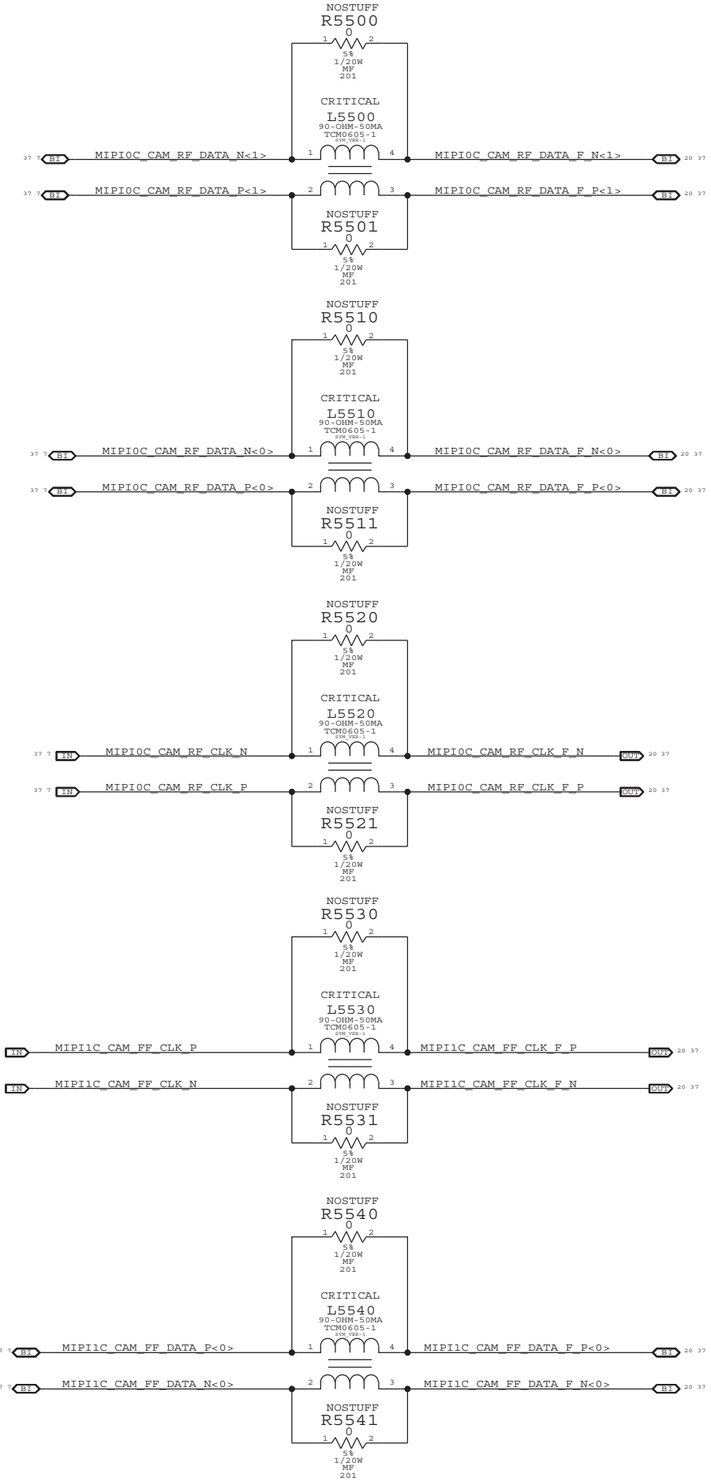

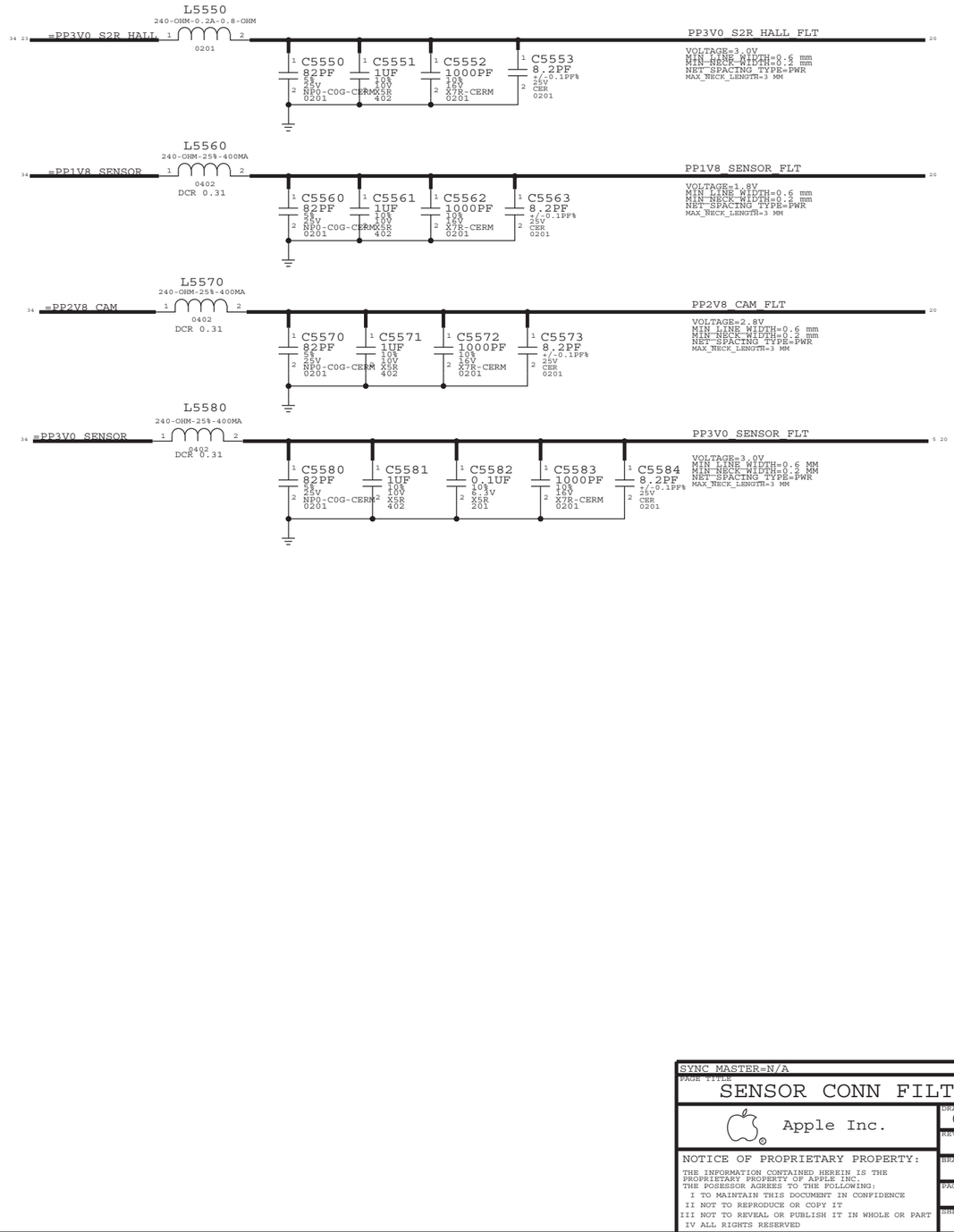

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

SENSOR CONN FILTERS 1

Apple Inc.

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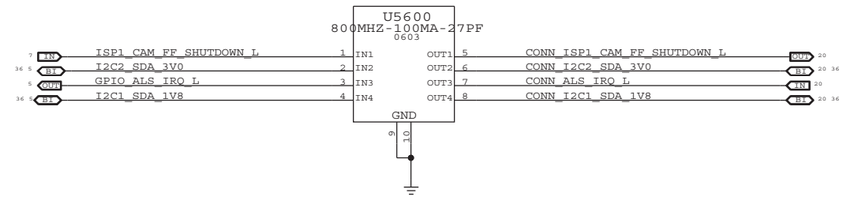
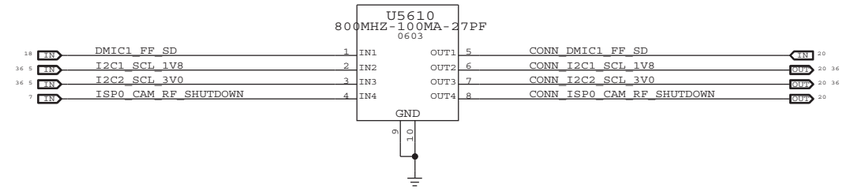
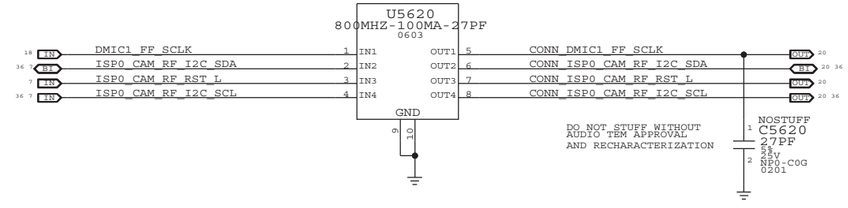
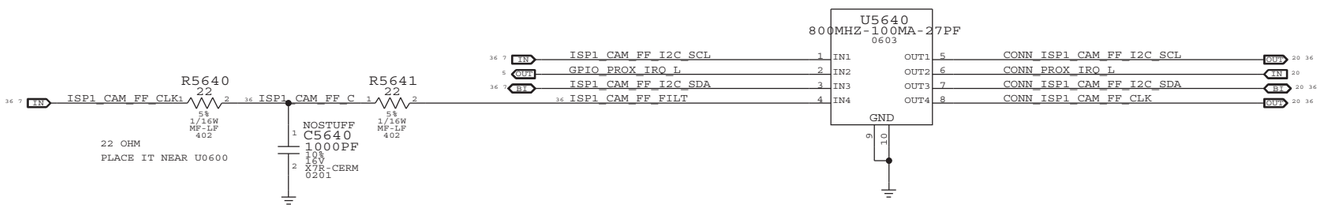
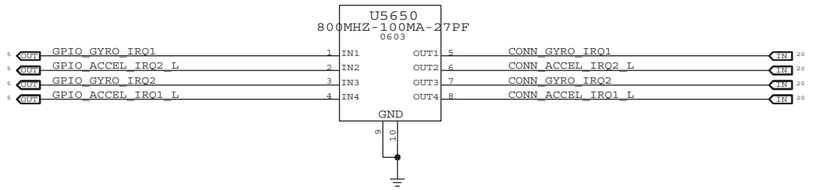
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0643	155S0373	?	U5600,U5610,U5620,U5630,U5640,U5650,U5660,U5670,U5680	RADAR:8376668

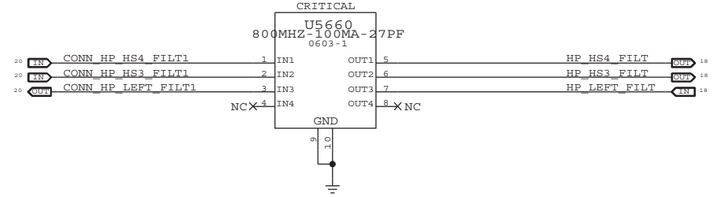


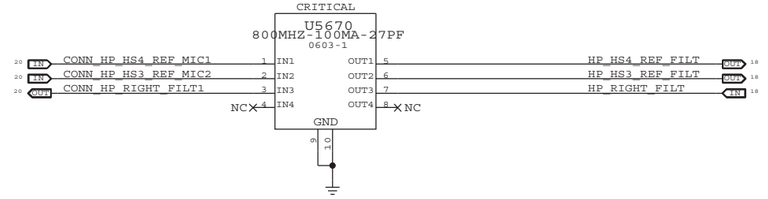












SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SENSOR CONN FILTERS 2

Apple Inc.

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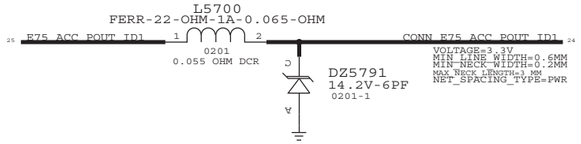
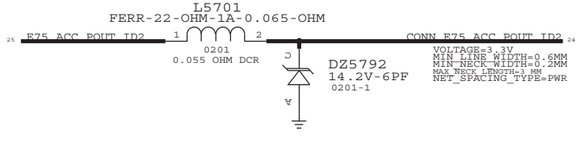
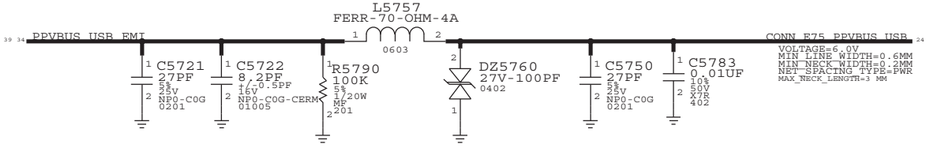
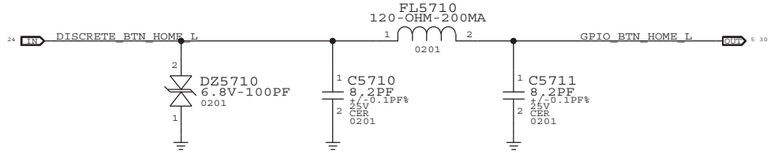
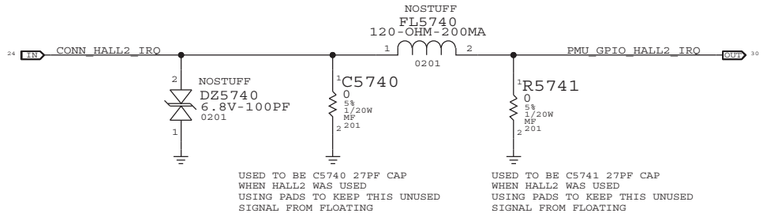


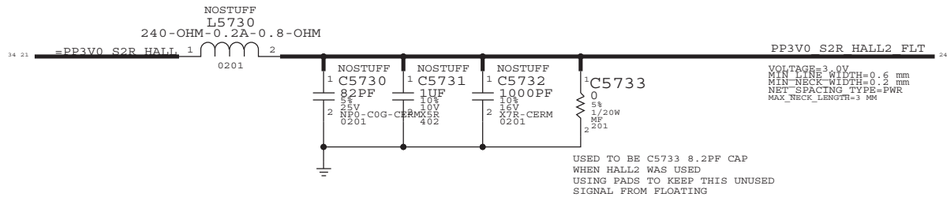




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ5760	RDAR://PROBLEM/8370432
155S0320	155S0513		L5700,L5701	RDAR://PROBLEM/9625601
155S0657	155S0537		FL5710,FL5750	
155S0741	155S0397		L5757	RDAR://PROBLEM/11238851







SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
E75 DOCK SUPPORT

Apple Inc.

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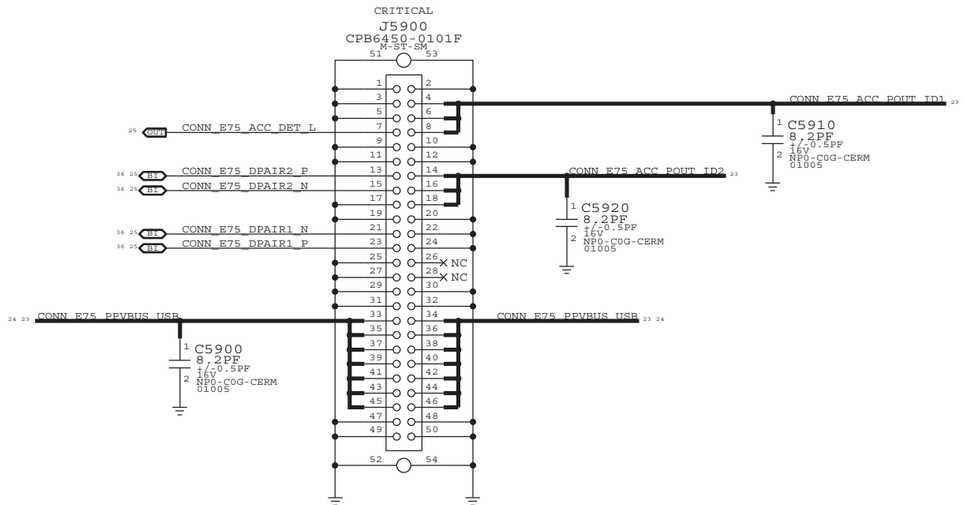
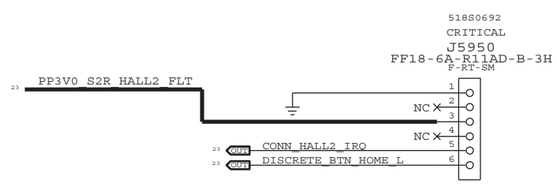
IO FLEX CONNECTOR

PN 516S0542 (PLUG - MALE)





SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE: IO FLEX CONN	
Apple Inc.	DRAWING NUMBER: 051-9385 SIZE: D
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TRISTAR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC,ASIC,TRISTAR,CBTL1608,A1,WLCSP36	U5900	CRITICAL	

=PP3V0_S2R_TRISTAR
C5930 1.0UF 20% 6.3V X5R 0201-MUR
C5935 0.1UF 10% 6.3V X5R 201
C5940 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP1V8_S2R_USBMUX
C5931 0.1UF 10% 6.3V X5R 201
C5941 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
=PP3V3_ACC
C5942 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C5932 0.1UF 10% 6.3V X5R 201
PPVBUS_PROT
C5943 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C5934 1UF 10% 25V X5R 0402

U5900
THS7383IYKAR
WCSP

MIKEY_TS_P	C3	DIG_DP	OMIT_TABLE
MIKEY_TS_N	C4	DIG_DN	
USB_TS_BBMUX_P	A1	USB1_DP	
USB_TS_BBMUX_N	B1	USB1_DN	
USB_BRICKID	C2	BRICK_ID	
USB_AP_P	A3	USB0_DP	
USB_AP_N	B3	USB0_DN	
UART2_TS_ACC_TXD	E2	UART0_TX	
UART2_TS_ACC_RXD	E1	UART0_RX	
UART6_AP_TXD	F2	UART1_TX	
UART6_AP_RXD	F1	UART1_RX	
UART1_BB_RXD	D2	UART2_TX	
UART1_BB_TXD	D1	UART2_RX	
JTAG_AP_TCK_TS_R	A5	JTAG_CLK	
JTAG_AP_TMS_TS_R	B5	JTAG_DIO	
	F6	P_IN	
	C5	ACC1	E75_ACC_POUT_ID1
	E5	ACC2	E75_ACC_POUT_ID2
TS_E75_DPAIR1_P	A2	DP1	
TS_E75_DPAIR1_N	B2	DN1	
TS_E75_DPAIR2_P	A4	DP2	
TS_E75_DPAIR2_N	B4	DN2	
PMU_E75_ACC_DET_L	E3	CON_DET_L	
OVP_SW_EN_L	D6	OVP_SW_EN*	
RST_AP_L	E4	SWITCH_EN	
TS_HOST_RESET	B6	HOST_RESET	
I2C0_SDA_1V8	D3	SDA	
I2C0_SCL_1V8	D4	SCL	
PMU_GPIO_TS_INT	C6	INT	
BYPASS_U5900	E6	BYPASS	
	F5	DVSS	
	C1	DVSS	
	A6	DVSS	
	F3	VDD_1V8	
	F4	VDD_3V0	
	D5	ACC_PWR	

TO BB USB
ACCESSORY USB
ACCESSORY UART
AP DEBUG UART
BB DEBUG UART
(T'S OFF TO H5G UART1)

R5970 100K 5% 1/20W MF 201
R5971 100K 5% 1/20W MF 201
C5944 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
C5933 1.0UF 20% 6.3V X5R 0201-MUR

R5930 0.00 0% 1/32W MF 01005
R5931 0.00 0% 1/32W MF 01005
R5929 0.00 0% 1/32W MF 01005
L81_MBUS_REF

CRITICAL L5930 90-OHM-50MA TCM0605-1
CONN_E75_DPAIR1_P
CONN_E75_DPAIR1_N
CRITICAL DZ5900 ESD0P2RF-02LS TSSLP-2-1
CRITICAL DZ5901 ESD0P2RF-02LS TSSLP-2-1

CRITICAL L5931 90-OHM-50MA TCM0605-1
CONN_E75_DPAIR2_P
CONN_E75_DPAIR2_N
CRITICAL DZ5902 ESD0P2RF-02LS TSSLP-2-1
CRITICAL DZ5903 ESD0P2RF-02LS TSSLP-2-1

PPVCC_MAIN
R5991 100K 5% 1/32W MF 01005
C5991 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0773	155S0453	?	FL5990	RDAR://PROBLEM/10882925

R5990 10K 5% 1/32W MF 01005
PMU_E75_ACC_DET_R_L
FL5990 120-OHM-210MA 01005
C5990 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005
CONN_E75_ACC_DET_L
CRITICAL DZ5990 ESD0P2RF-02LS TSSLP-2-1
CRITICAL D5990 SM-201 DSF01S30SC

TRISTAR BASEBAND USB MUX (NEEDED FOR MDM9600 BB)

=PP3V2_S2R_USBMUX
C5960 0.1UF 10% 6.3V X5R 201
R5961 10K 5% 1/20W MF 201
R5960 10K 5% 1/20W MF 201

U5902
PI3USB102ZLE
TQFN

USB11_AP_BBMUX_P	M+	Y+	USB_BBMUX_BB_P
USB11_AP_BBMUX_N	M-	Y-	USB_BBMUX_BB_N
USB_TS_BBMUX_P	D+		
USB_TS_BBMUX_N	D-		
TS_BBMUX_EN_L	OE*	SEL	PMU_GPIO_BBUSBTODOCK_EN_R

R5962 0.00 0% 1/32W MF 01005
PMU_GPIO_BBUSBTODOCK_EN

SEL	Y+	Y-
0	M+	M-
1	D+	D-

DEFAULT =>

NOTE: ISOLATE SELECT SIGNAL FROM PMU ON MLB_B AND MLB_C SO THE MUX IS PERMANENTLY POINTED TO THE DOCK

BASEBAND USB MUX BYPASS

R5965 0 5% 1/20W MF 201
USB_TS_BBMUX_P — USB_BBMUX_BB_P
R5966 0 5% 1/20W MF 201
USB_TS_BBMUX_N — USB_BBMUX_BB_N

=PP1V8_S2R_USBMUX
C5936 0.1UF 10% 6.3V X5R 201
TS_HOST_RESET
R5934 0.00 0% 1/32W MF 01005
AP_WDOG_RESET_IN
TS_HOST_RESET_R
U5903 74LVC1G32 SOT891
PMU_RESET_IN_R
R5935 22 5% 1/32W MF 01005
PMU_RESET_IN
R5932 220K MF 5% 1/32W 01005
R5933 220K MF 5% 1/32W 01005

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: TRISTAR

Apple Inc.

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CELLULAR/GPS HOTBAR PADS

OMIT

998-3732

J6000

HOT-BAR-PADS

H8-SM

5	IN	BB_JTAG_TMS_RF	1
			2
34		=BATT_POS_F_3G	3
			4
			5
			6
			7
			8
			9
27	IN	WLAN_TX_BLANK	10
39 30 25 4	OUT	RST_AP_L	11
5	IN	GPIO_BB_RADIO_ON_L	12
30	IN	PMU_GPIO_BB_PMU_RST_L	13
5	OUT	GPIO_BB_GSM_TXBURST	14
39 5	IN	GPIO_BB_RST_L	15
5	OUT	GPIO_BB_RESET_DET_L	16
			17
36 5	IN	GPIO_BB_HSIC_HOST_RDY	18
36 5	OUT	GPIO_BB_HSIC_RESUME	19
5	OUT	BB_JTAG_TDO_RF	20
5	IN	BB_JTAG_TDI_RF	21
5	IN	BB_JTAG_TRST_RF_L	22
5	OUT	GPIO_BB_GPS_SYNC	23
30	OUT	PMU_GPIO_BB_HOST_WAKE	24
			25
30	IN	BB_VBUS_DET	26
36 25	BI	USB_BBMUX_BB_P	27
36 25	BI	USB_BBMUX_BB_N	28
			29
36 25 5	OUT	UART1_BB_RXD	30
36 25 5	IN	UART1_BB_TXD	31
36 5	OUT	UART1_BB_CTS_L	32
36 5	IN	UART1_BB_RTS_L	33
			34
5	BI	GPIO_AP_MODEM_WAKE	35
36 5	OUT	GPIO_BB_HSIC_DEV_RDY	36
			37
36 26 4	BI	HSIC3_BB_STB	38
			39
36 26 4	BI	HSIC3_BB_DATA	40
			41
5	IN	BB_JTAG_TCK_RF	42

DEBUG

NOSTUFF

J6050

MM4829-2702

F-ST-SM

36 26 4 HSIC3_BB_STB — 1

NOSTUFF

J6051

MM4829-2702

F-ST-SM

36 26 4 HSIC3_BB_DATA — 1

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: CELLULAR

Apple Inc.

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REVISION A.0.0

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WLAN/BT

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

ANTENNA CONNECTOR

CRITICAL
J6190_RF
MM4829-2702
F-ST-SM

RF_ANT
WIFI 50S
50_OHM

CRITICAL
C6193_RF
3.9PF
+/-0.1PF
50V
NPO-CERM
0402

NOSTUFF
L6190_RF
5.6NH+/-0.3NH
0402

RF_ANT_MATCH1
WIFI 50S
50_OHM

CRITICAL
C6191_RF
0.2PF
+/-0.05PF
50V
NPO-CERM
0402

CONDUCTED TEST PORT

CRITICAL
J6191_RF
MM8030-2600RK0
F-ST-SM

RF_CAL
WIFI 50S
50_OHM

CRITICAL
C6192_RF
8.2PF
+/-0.25PF%
25V
NP0-C0G
0201

NOSTUFF
L6191_RF
5.6NH-3%-0.35A
0201

RF_CAL_MATCH
WIFI 50S
50_OHM

NOSTUFF
L6192_RF
5.6NH-3%-0.35A
0201

CRITICAL
U6104_RF
DPX205850DT-9038A1SJ
SM

XW6102_RF
SHORT-0402

BATT_VCC → BATT_VCC_WLAN

C6101_RF
10UF
20%
6.3V
CERM-X5R
0402-1

C6102_RF
27PF
5%
16V
NP0-C0G
01005

PP_WLAN_VDDIO_1V8
VOLTAGE=1.8V

R6108_RF
0.00
0%
1/32W
MF
01005

PP_WL_BT_VDDIO_AP
VOLTAGE=1.8V

C6103_RF
0.01UF
10%
6.3V
X5R
01005

C6104_RF
27PF
5%
16V
NP0-C0G
01005

NOSTUFF
R6105_RF
10K
5%
1/32W
MF
01005

R6107_RF
10K
5%
1/32W
MF
01005

VDDIO_1P8V
BATT_VCC
VBATT_RF_VCC
VBATT_RF_VCC

32K INTERFACE TO AP

XW6101_RF
SHORT-01005

CLK32K_AP → WLAN_CLK32K

CRITICAL
L6111_RF
2.5UH-30%-0.7A-0.24OHM
0603

C6109
4.7UF
20%
6.3V
X5R-CERM1
402

U6101_RF
LBEE5ZHTWC501
LGA
OMIT_TABLE

CLK32K_AP	32	
GPIO_6	6	
VIN_1P2LDO	29	WLAN_BUCK_OUT
WL_REG_ON	31	WLAN_REG_ON
BT_REG_ON	30	BT_REG_ON
JTAG_SEL	14	JTAG_SEL
SR_VLX	28	WLAN_SR_VLX1
WLAN_HSIC_DATA	24	50_HSIC_WLAN_DATA
WLAN_HSIC_STROBE	25	50_HSIC_WLAN_STROBE
RF_SW_CTRL_3	40	NC (NO LONGER NEEDED BASED ON AND GATE REMOVAL)
2G_ANT	42	50_WLAN_G
5G_ANT	52	50_WLAN_A
HOST_WAKE_BT	34	HOST_WAKE_BT
BT_WAKE	39	BT_WAKE
BT_UART_RXD	38	BT_UART_RXD
BT_UART_TXD	37	BT_UART_TXD
BT_UART_RTS*	35	BT_UART_RTS_L
BT_UART_CTS*	36	BT_UART_CTS_L
BT_PCM_CLK	3	BT_PCM_CLK
BT_PCM_SYNC	5	BT_PCM_SYNC
BT_PCM_OUT	2	BT_PCM_OUT
BT_PCM_IN	4	BT_PCM_IN
GPIO_0	9	HOST_WAKE_WLAN
GPIO_1	8	AP_HSIC3_RDY
GPIO_2	10	WLAN_HSIC3_RESUME
GPIO_3	12	AGG_CHANNEL
GPIO_4	7	WLAN_UART_RXD
GPIO_5	11	WLAN_UART_TXD
GPIO_12	13	HSIC_DEVICE_RDY
GND	17 18 19 20 21 22 1 16 23 26 33 41 43 44 45 48 49 50 51	
THRML_PAD	53 54 55 56 57 58 59 60	

CRITICAL
C6107_RF
8.2PF
+/-0.25PF%
25V
NP0-C0G
0201

50_WLAN_G_1

CRITICAL
C6108_RF
4.7PF
+/-0.1PF
25V
C0G-CERM
0201

50_WLAN_A_DIPLX

NOSTUFF
C6111_RF
0.2PF
+/-0.05PF
25V
C0G-CERM
201

R6111_RF
10K
5%
1/32W
MF
01005

PULL DOWN RESISTORS

GPIO6	SDIO_DATA<1>	SDIO_DATA<2>	MODE	DEFAULT ARM STATE
0	X	X	SDIO	IN RESET
1	X	0	GSPI	IN RESET
1	0	1	HSIC	OUT OF RESET
1	1	1	BOOTLESS HSIC	IN RESET

PP_WL_BT_VDDIO_AP

R6113_RF
10K
5%
1/32W
MF
01005

HSIC_DEVICE_RDY

U6102_RF
74AUP1G08GF
SOT891

R6112_RF
1.00M
1%
1/32W
MF
01005

WLAN_REG_ON → WLAN_REG_ON_RC

C6110_RF
0.22UF
20%
6.3V
X5R
0201

DEV_HSIC3_RDY

R6114_RF
0.00
0%
1/32W
MF
01005

AGG_CHANNEL → WLAN_TX_BLANK

PP6102_RF P4MM — WLAN_REG_ON
PP6103_RF P4MM — HOST_WAKE_WLAN
PP6104_RF P4MM — AP_HSIC3_RDY
PP6105_RF P4MM — DEV_HSIC3_RDY
PP6106_RF P4MM — WLAN_UART_RXD
PP6107_RF P4MM — WLAN_UART_TXD

PP6109_RF P4MM — AGG_CHANNEL
PP6110_RF P4MM — 50_HSIC_WLAN_DATA
PP6111_RF P4MM — 50_HSIC_WLAN_STROBE
PP6112_RF P4MM — HSIC_DEVICE_RDY

CHANGE LIST

07FEB2012 MUSHTAQ COPIED FROM N41, ADDED J2 ANT MATCH/CONN
C6107 FROM 20PF TO 8.2PF, C6108 FROM 10PF TO 4.7PF
U6104 FROM SOSHIN TO MURATA LFD212G45DS5D355

13FEB2012 AMANDA CHANGED OMIT TO OMIT_TABLE AND UPDATED
BOM OPTION TABLES TO ALTERNATE TABLES
REMOVED BOM TABLE FOR C6111_RF (NOW ALWAYS NOSTUFF)

SYNC_MASTER=N/A SYNC_DATE=N/A

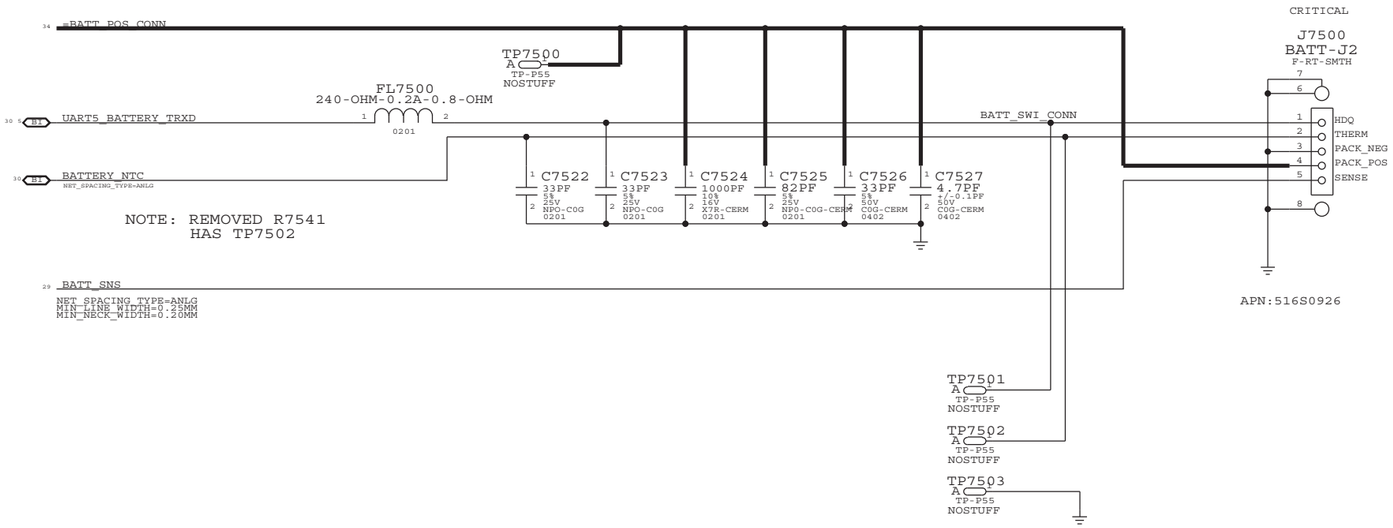
PAGE TITLE: WIFI/BT

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 61 OF 154
SHEET: 27 OF 39

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0644	155S0274	?		RDAR://PROBLEM/11282371

FL7500,L3620,L5550,L5730



SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PAGE TITLE

POWER: BATTERY CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9385 SIZE D

REVISION A.0.0

BRANCH

PAGE 75 OF 154

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VCC MAIN BYPASS

TOTAL CAPS = ~400UF

PLACE ONE 10UF CAP AT EACH VDD INPUT

PLACEMENT_NOTE=PLACE NEAR L8225.1

PPVCC_MAIN

C8166 CRITICAL 150UF 20% 6.3V TANT-1 B15G
C8165 CRITICAL 150UF 20% 6.3V TANT-1 B15G
ESR MAX=70MOHM ESR MAX=70MOHM
C8154 CRITICAL 10UF 20% 6.3V X5R 603
C8155 CRITICAL 10UF 20% 6.3V X5R 603
C8156 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8157 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8162 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8187 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8188 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8193 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8194 CRITICAL 10UF 20% 6.3V X5R 603
C8130 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8131 CRITICAL 1UF 20% 6.3V X5R 0201
C8163 82PF 5% 25V NPO-COG-CERM 0201
C8164 8.2PF +/-0.1PF% 25V C0G 0201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND,1.0UH,20%,59MO,2.74A	L8100,L8101,L8102,L8103,L8109,L8110	CRITICAL	
152S1638	1	IND,1.0UH,20%,64MO,2.3A	L8104	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?		?

C8100,C8101,C8102,C8103,C8104,C8105,C8107,C8108,C8109,C8110,C8111,C8112,C8113,C8114,C8117,C8118,C8119,C8120,C8121,C8122,C8123,C8195

PPVCC_MAIN_CPU0
C8159 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8190 CRITICAL 10UF 20% 6.3V CERM-X5R 0402

PPVCC_MAIN_CPU1
C8158 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8189 CRITICAL 10UF 20% 6.3V CERM-X5R 0402

PPVCC_MAIN_SOC
C8160 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8161 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8191 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8192 CRITICAL 10UF 20% 6.3V CERM-X5R 0402

L8112 CRITICAL 2.2UH-20%-4A-32MOHM PIME101E-SM DCR=32MOHM MAX

OVP_SW_EN_L
R8170 NOSTUFF 4.7K 5% 1/20W MF 201

Q8104 CRITICAL FDMQ6683 MLP3.3X3.3
ID=13.0A @ 0.0136VGS, -2.5V

R8172 0 5% 1/20W MF 201
BATT_SNS
BATT_SNS_R
C8172 NOSTUFF 0.022UF 10% 25V X7R 0402
LAYOUT NOTE - R8172- PLACE NEAR BMU C3172- PLACE NEAR PMU R3173- PLACE NEAR PMU
R8173 499 1% 1/20W MF 201

D8100 CRITICAL PMEG4030ER SOD-123W
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM NET_SPACING_TYPE=SWITCHNODE DIDT=TRUE

PPBATT_VCC
ACT_DIO
MIN_LINE_WIDTH=0.2 MM MIN_NECK_WIDTH=0.1 MM NET_SPACING_TYPE=ANLG

CHG_LX
VBAT
IBAT_S
IBAT
ACT_DIO

PPVBUS_USB
NOSTUFF XW8114 SHORT-0201
MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=6V

PMU_VCENTER
MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.25MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=6V
C8125 CRITICAL 4.7UF 10% 35V X5R-CERM 0603
C8126 CRITICAL 4.7UF 10% 35V X5R-CERM 0603
LAYOUT NOTE: PLACE RIGHT AT THE PIN
VCENTER

PPVBUS_PROT
MIN_LINE_WIDTH=0.60MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=6.0V
DZ8120 CRITICAL BZT52C10LP LLP
NOTE: 10V ZENER
C8124 CRITICAL 2.2UF 10% 25V X5R-CERM 805
LAYOUT NOTE: PLACE RIGHT AT THE PIN
VBUS_PROT_G
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.1MM NET_SPACING_TYPE=ANLG
VBUS

R8116 NOSTUFF 470K 1% 1/20W MF 201
Q8123 CRITICAL FDMC6676BZ MLP3.3X3.3
PPVBUS_USB_DCIN
R8130 220K 1% 1/20W MF 201

USB REVERSE VOLTAGE PROTECTION

R8196 4.7K 1% 1/20W MF 201
OVP_SW_EN_L_R
C8196 NOSTUFF 0.022UF 10% 25V X7R 0402
LAYOUT NOTE: R8196, C8196 CAN BE ANYWHERE BET. TRISTAR AND PMU
VBUS_OVP_OFF

LDO BYPASS

PP3V0_GRAPE
PP1V7_VA_VCP
PP3V2_S2R_USBMUX
PP3V0_S2R_HALL
PP1V0
PP3V3_ACC
LDO5
LDO10

C8133 CRITICAL 4.7UF 20% 6.3V X5R-CERM1 402
C8132 CRITICAL 4.7UF 20% 6.3V X5R-CERM1 402
C8149 CRITICAL 2.2UF 10% 6.3V X5R 402
C8148 CRITICAL 4.7UF 20% 6.3V X5R-CERM1 402
C8146 CRITICAL 1UF 10% 6.3V X5R 402
C8145 CRITICAL 2.2UF 10% 6.3V X5R 402
C8144 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8147 CRITICAL 2.2UF 10% 6.3V X5R 402

PP3V0_SENSOR
PP3V0_IO
PP3V0_S2R_TRISTAR
PP2V8_CAM
PP1V1_SRAM
PP1V8_ALWAYS

C8169 0.22UF 20% 6.3V X5R 0201
C8168 CRITICAL 4.7UF 20% 6.3V X5R-CERM1 402
C8167 CRITICAL 4.7UF 20% 6.3V X5R-CERM1 402
C8153 CRITICAL 2.2UF 10% 6.3V X5R 402
C8152 CRITICAL 4.7UF 20% 6.3V X5R-CERM2 402
C8151 CRITICAL 2.2UF 10% 6.3V X5R 402

PP1V8_S2R
C8135 1UF 10% 6.3V CERM 402
PPVCC_MAIN
C8134 1UF 10% 6.3V CERM 402
C8136 1UF 10% 6.3V CERM 402
1 CAP PER PIN N5 N14
PP1V2_S2R

NOTE: FOR NO BATTERY SITUATION

PPBATT_VCC
C8174 NOSTUFF CRITICAL 10UF 20% 6.3V CERM-X5R 0402-1
C8173 NOSTUFF CRITICAL 10UF 20% 6.3V CERM-X5R 0402-1
C8170 CRITICAL 10UF 20% 6.3V CERM-X5R 0402-1
C8171 CRITICAL 10UF 20% 6.3V CERM-X5R 0402-1
BATT_POS_RC
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=4.6V
R8100 0.5 1% 1/16W MF 402

Y8138 CRITICAL 32.768K-20PPM-12.5PF 2012-1
NET_SPACING_TYPE=CRYSTAL
PMU_XTAL
PMU_EXTAL
C8142 CRITICAL 18PF 5% 25V NPO-C0G 201
C8143 CRITICAL 18PF 5% 25V NPO-C0G 201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8165,C8166	RDAR://PROBLEM/8967213
197S0399	197S0392	?	Y8138	RDAR://PROBLEM/9936684

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

OMIT_TABLE
U8100
D2018
FCBGA
SYM 2 OF 3

USB/BAT BUCK
BUCK0A_LX0 A9
BUCK0A_LX1 B9
BUCK0A_FB A11
BUCK0B_LX0 B11
BUCK0B_LX1 E11
BUCK0B_FB A5
BUCK0C_LX0 B5
BUCK0C_FB A7
BUCK2_LX0 B7
BUCK2_LX1 E6
BUCK2_LX2 E1
BUCK2_LX3 E2
BUCK2_FB F5
BUCK3_LX0 A13
BUCK3_FB B13
BUCK4_LX0 A15
BUCK4_FB B15
BUCK5_LX0 A17
BUCK5_BYP B17
BUCK5_FB A19 NC B19 NC E15

LDO
VCC_MAIN
VLDO1 P9 (150MA; 1.2-3.1V) PP3V0_GRAPE
VLDO2 P4 (100MA; 1.65-1.805V; BUCK3) PP1V7_VA_VCP
VLDO3 N8 (50MA; 2.5-3.3V) PP3V2_S2R_USBMUX
VLDO4 P2 (100MA; 1.8-3.3V) PP3V0_SENSOR
VLDO5 P8 (300MA; 1.7-3.0V) LDO5
VLDO6 P10 (150MA; 2.5-3.6V) PP3V3_ACC
VLDO7 P3 (50MA; 1.2-3.1V) PP3V0_S2R_TRISTAR
VLDO8 M6 (15MA; 2.0-3.55V) PP3V0_S2R_HALL
VLDO9 P11 (300MA; 1.2-3.0V) PP3V0_IO
VLDO10 P6 (200MA; 2.5-3.55V) LDO10
VLDO11 M1 (250MA; 1.7-3.0V) PP2V8_CAM
VLDO12 P5 (150MA; 0.6-1.3V) PP1V0
VLDO16 P14 (650MA; 1.1V) PP1V1_SRAM
ON_BUF M16 (5MA; 1.8V) PP1V8_ALWAYS
NET_SPACING_TYPE=PWR MIN_NECK_WIDTH=0.25 MM

SWITCH POWER
VBUCK4 M2
CPU1V2_SW L1 (RON=0.05 OHM MAX)
CPU1V2_SW L2
VBUCK3 K2
CPU1V8_SW J1 (RON=0.05 OHM MAX)
CPU1V8_SW J2
WDIG_SW K1 (RON=0.2 OHM MAX)
VPUMP K3 PMU_VPUMP
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM VOLTAGE=4.6V
C8137 0.01UF 10% 10V X5R-CERM 0201

INPUT
VCC_MAIN_S L20
VCC_MAIN N15 N16 N17 N18
VDD_LDO1_6 N9
VDD_LDO2 N4
VDD_LDO3_5_8 N7
VDD_LDO4_7 N3
VDD_LDO9 N11
VDD_LDO10 N6
VDD_LDO11 N2
VDD_LDO12 N5
VDD_LDO16 N14

XTAL
XTAL1 N1
XTAL2 P1

VDD_BUCK0A A10
VDD_BUCK0B B10
VDD_BUCK0C A6 B6 D1 D2
VDD_BUCK2_01 A14 B14 A18
VDD_BUCK2_23 B18 H1
VDD_BUCK3 H2 A2
VDD_BUCK4 B2 A22
VDD_BUCK5 B22

PPVCC_MAIN_CPU0 A10
PPVCC_MAIN_CPU1 A6
PPVCC_MAIN D1 D2 H1
PPVCC_MAIN_SOC A14

PPBUS_G3H
C8138 1UF 20% 6.3V X5R 0201
C8140 1UF 10% 6.3V CERM 402
C8139 1UF 10% 6.3V CERM 402
C8141 1UF 10% 6.3V CERM 402

PP1V2_S2R
PP1V2
PP1V8_S2R
PP1V8
TP_PP1V8_GRAPE

PP1V1_CPU0_FET
C8100 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8101 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8120 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8121 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8180 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8181 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8184 NOSTUFF CRITICAL 10UF 20% 6.3V CERM-X5R 0402

PP1V1_CPU1_FET
C8102 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8103 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8122 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8123 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8182 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8183 CRITICAL 10UF 20% 6.3V CERM-X5R 0402
C8185 NOSTUFF CRITICAL 10UF 20% 6.3V CERM-X5R 0402

PP1V1_CPUB
C8104 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8105 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
ADDITIONAL DISTRIBUTED 12UF (NO DERATING)

PP1V2_SOC
C8107 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8108 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8195 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8117 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8118 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8119 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
ADDITIONAL DISTRIBUTED 98UF (NO DERATING)

PP1V8_S2R
C8109 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8110 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
ADDITIONAL DISTRIBUTED 27UF (NO DERATING)

PP1V2_S2R
C8111 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8112 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
ADDITIONAL DISTRIBUTED 64UF (NO DERATING)

PP3V3_OUT
C8113 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
C8114 CRITICAL 22UF 20% 6.3V X5R-CERM-1 603
ADDITIONAL DISTRIBUTED 32UF (NO DERATING)

L8100 CRITICAL OMIT_TABLE 1.0UH-20%-2.74A-59MOHM PSB32251E-SM
L8101 CRITICAL OMIT_TABLE 1.0UH-20%-2.74A-59MOHM PSB32251E-SM
L8102 CRITICAL OMIT_TABLE 1.0UH-20%-2.74A-59MOHM PSB32251E-SM
L8103 CRITICAL OMIT_TABLE 1.0UH-20%-2.74A-59MOHM PSB32251E-SM
L8104 CRITICAL OMIT_TABLE 1.0UH-20%-2.3A-64MOHM PSB25201E-SM
L8105 CRITICAL 1.0UH-20%-3.9A-0.035OHM PILE32251E-SM
L8106 CRITICAL 1.0UH-20%-3.9A-0.035OHM PILE32251E-SM
L8107 CRITICAL 1.0UH-20%-3.9A-0.035OHM PILE32251E-SM
L8109 CRITICAL OMIT_TABLE 1.0UH-20%-2.74A-59MOHM PSB32251E-SM
L8110 CRITICAL OMIT_TABLE 1.0UH-20%-2.74A-59MOHM PSB32251E-SM
L8111 CRITICAL 2.2UH-20%-3.3A-0.064OHM PIME051E-SM

NOSTUFF XW8100 SM
NOSTUFF XW8101 SM
NOSTUFF XW8102 SM
NOSTUFF XW8103 SM
NOSTUFF XW8104 SM
NOSTUFF XW8105 SM
NOSTUFF XW8106 SM

BUCK0A_LX0
BUCK0A_LX1
BUCK0A_FB
BUCK0B_LX0
BUCK0B_LX1
BUCK0B_FB
BUCK0C_LX0
BUCK0C_FB
BUCK2_LX0
BUCK2_LX1
BUCK2_LX2
BUCK2_FB
BUCK3_LX0
BUCK3_FB
BUCK4_LX0
BUCK4_FB
BUCK5_LX0
BUCK5_FB
(PP3V3_OUT)

SYNC_MASTER=MADHAVI	SYNC_DATE=12/06/2011
PAGE TITLE: PMU: ADRIANA PAGE 1	
Apple Inc.	DRAWING NUMBER 051-9385 SIZE D
	REVISION A.0.0
	BRANCH
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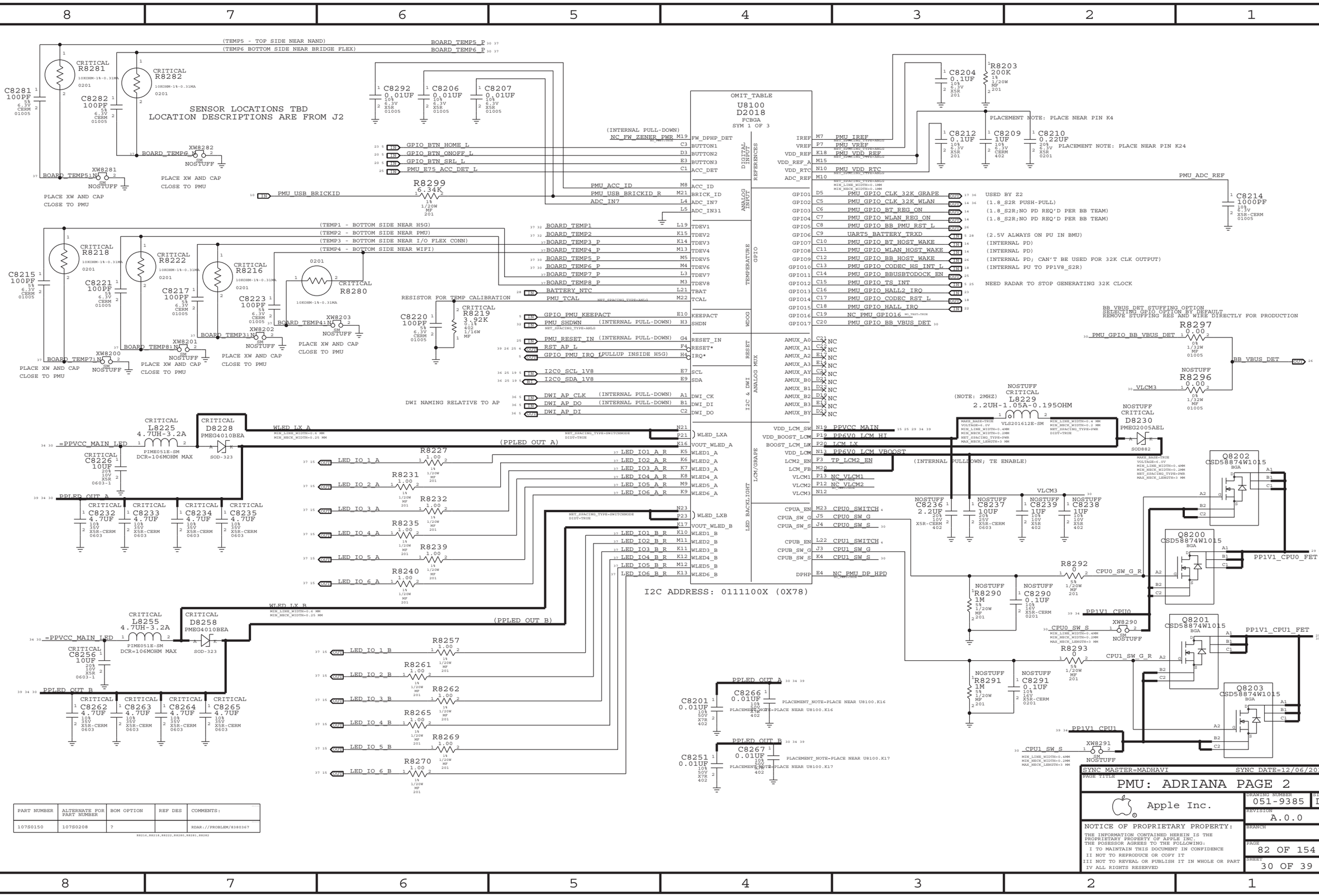
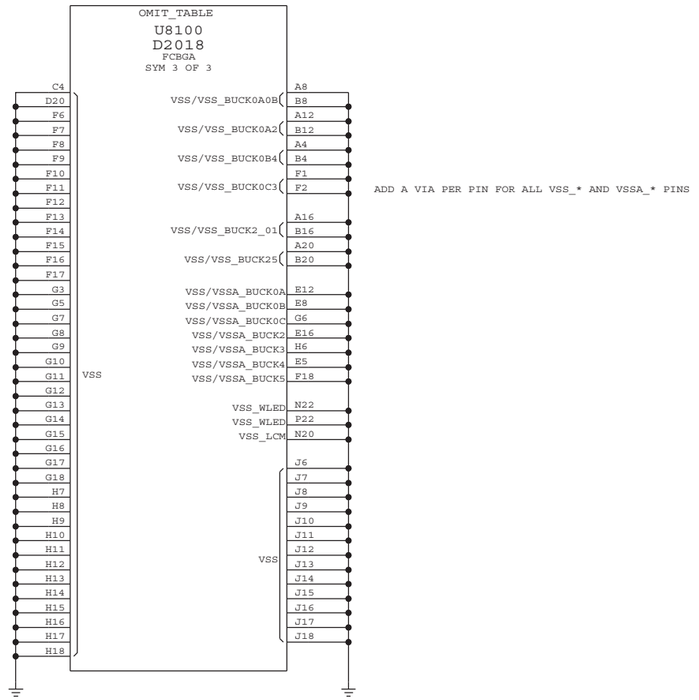
	SHEET 29 OF 39



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	?		RDAR://PROBLEM/8380367

R8216,R8219,R8222,R8280,R8281,R8282



SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PAGE TITLE

PMU: ADRIANA PAGE 3

Apple Inc.

DRAWING NUMBER 051-9385

SIZE D

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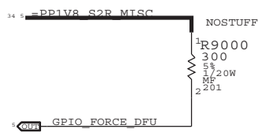
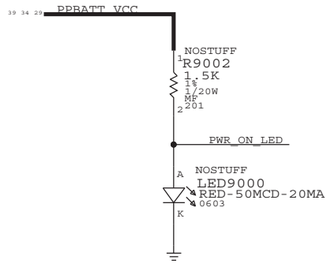
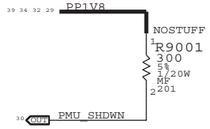
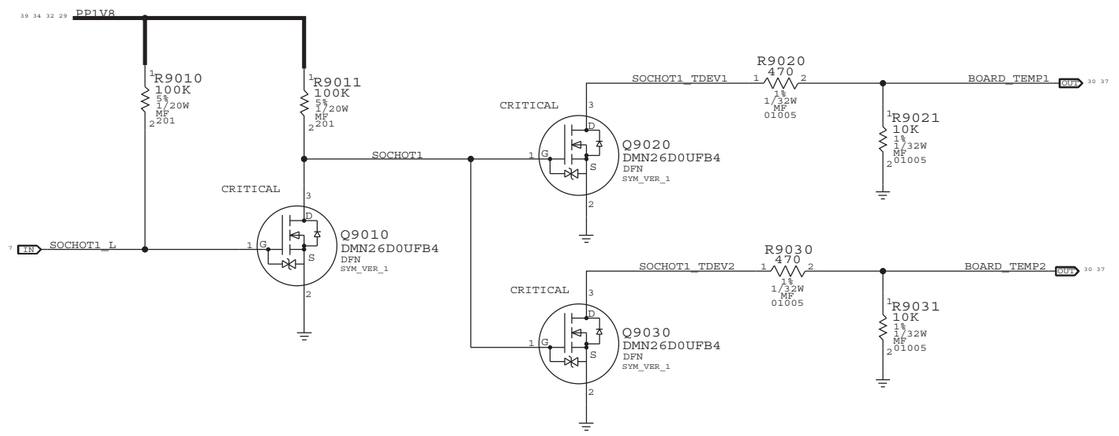
DEBUG RESET ACCESS







SOCHOT TO PMU TDEV1/TDEV2



SYNC_MASTER=MLB SYNC_DATE=11/09/2011

PAGE TITLE

DEBUG/MISC.

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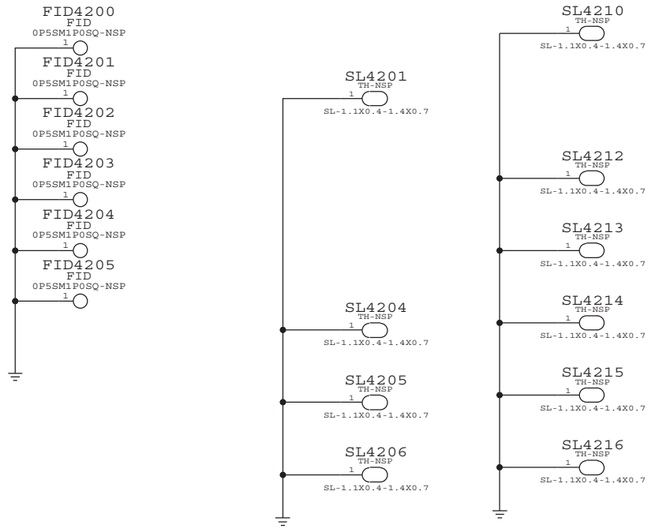
PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=N/A SYNC DATE=N/A

PAGE TITLE
TEST/HOLES/FIDUCUALS

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POWER CONNECTIONS

BUCK0A

39 30 PP1V1_CPU0 = =PPVDD_CPU0_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0B

39 30 PP1V1_CPU1 = =PPVDD_CPU1_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK0C

39 29 PP1V1_CPUB = =PPVDD_CPUB_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK2

39 29 PP1V2_SOC = =PPVDD_SOC_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK3

39 29 PP1V8_S2R = =PP1V8_S2R_MISC 6 32
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= VDDIO_WLAN_BT_1V8 14
= =PP1V8_S2R_USBMUX 25
= =PP1V8_S2R_DDR 11 12

BUCK4

39 29 PP1V2_S2R = =PP1V2_S2R_H5 8
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V2_S2R_DDR 11 12

BUCK3_SW

CPU1V8_SW

32 29 39 PP1V8 = =PP1V8_SENSOR 21
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3MM
= =PP1V8_AUDIO 18
= =PP1V8_VDDIO18_H5 4 6 7 9
= =PP1V8_H5 4 5 7 10
= =PP1V8_MIPI_H5 7
= =PP1V8_DP_H5 7
= =PP1V8_EDP_H5 7
= =PP1V8_NAND_H5 6 9
= =PP1V8_NAND 13
= =PP1V8_PLL_H5 4
= =PP1V8_MISC 16

BUCK4_SW

CPU1V2_SW

39 29 PP1V2 = =PP1V2_VDDQ_DDR 11 12
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V2_VDDIOD_H5 8 9
= =PP1V2_HSIC_H5 4

BUCK5

39 29 PP3V3_OUT = =PP3V3_NAND 13
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V3_USB_H5 4
= =PP3V3_LCD 15

BACKLIGHT BOOST

39 30 PPLED_OUT_A = =PPLED_REG_A 15
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 30 PPLED_OUT_B = =PPLED_REG_B 15
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO1

39 29 PP3V0_GRAPE = =PP3V0_GRAPE 16 17
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_GRAPE_MARIO1 16
= =PP3V0_GRAPE_Z1 17
= =PP3V0_GRAPE_Z2 17

LDO2

39 29 19 PP1V7_VA_VCP = =PP1V7_VA_VCP 18 19
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO3 (NO LONGER NEEDED)

39 29 PP3V2_S2R_USBMUX = =PP3V2_S2R_USBMUX 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO4

39 29 PP3V0_SENSOR = =PP3V0_SENSOR 21
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO6

39 29 PP3V3_ACC = =PP3V3_ACC 25
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO7

29 PP3V0_S2R_TRISTAR = =PP3V0_S2R_TRISTAR 25
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO8

39 29 PP3V0_S2R_HALL = 1927 =PP3V0_S2R_HALL 21 23
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO9

39 29 PP3V0_IO = =PP3V0_VDDIO30_H5 9
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO11

39 29 PP2V8_CAM = =PP2V8_CAM 21
MAKE_BASE=TRUE
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

LDO12

39 29 PP1V0 = =PP1V0_MIPI_H5 7
MAKE_BASE=TRUE
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V0_DP_PAD_DVDD_H5 7
= =PP1V0_EDP_PAD_DVDD_H5 7
= =PP1V0_USB_H5 4
= =PP1V0_HSIC_H5 4
= =PP1V0_MIPI_PLL_H5 7

LDO16

39 29 PP1V1_SRAM = =PP1V8_SRAM_H5 9
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

39 29 PP1V8_ALWAYS = =PP1V8_ALWAYS 5
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

CHARGER MAIN

39 30 29 25 15 PPVCC_MAIN = =PPVCC_MAIN_AUDIO 18 19
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PPVCC_MAIN_LED 30
= =PPVCC_MAIN_CPU0 29
= =PPVCC_MAIN_CPU1 29
= =PPVCC_MAIN_SOC 29

BATTERY

39 32 29 PPBATT_VCC = =BATT_POS_CONN 28
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =BATT_POS_F_3G 24 CELLULAR RADIO
= =BATT_VCC 27 WLAN

USB POWER INPUT

39 23 PPVBUS_USB_EMI = =PPVBUS_USB_DCIN 29
MAKE_BASE=TRUE
VOLTAGE=6V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

SYNC_MASTER=N/A SYNC_DATE=N/A

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POWER ALIASES

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06,BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3,ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2,ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3,ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4,ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5,ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5,ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5,ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP,BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR1000	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

TCF_VERSION NC_UARTS_TXD ← ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?
0P2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC MASTER=MIKE SYNC DATE=11/30/2011

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CONSTRAINTS: MLB RULES

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J6	CLK_50S	CLK	PMU_GPIO_CLK_32K_GRAPE 17 30
J7	CLK_50S	CLK	PMU_GPIO_CLK_32K_WLAN 14 30
J8	CLK_50S	CLK	ISP1_CAM_FF_CLK 7 22
J9	CLK_50S	CLK	CONN_ISP1_CAM_FF_CLK 20 22
J10	CLK_50S	CLK	ISP0_CAM_RF_CLK 7 22
J11	CLK_50S	CLK	CONN_ISP0_CAM_RF_CLK 20 22
J12	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
J13	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
J14	CLK_50S	CLK	ISP0_CAM_RF_CLK_R 7
J15	CLK_50S	CLK	ISP1_CAM_FF_CLK_R 7
J16	CLK_50S	CLK	ISP1_CAM_FF_C 22
J17	CLK_50S	CLK	ISP0_CAM_RF_C 22
J18	CLK_50S	CLK	ISP1_CAM_FF_FILT 22
J19	CLK_50S	CLK	ISP0_CAM_RF_FILT 22

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	3:1_SPACING
UART	UART	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J19	UART_50S	UART	UART2_TS_ACC_RXD 5 25
J18	UART_50S	UART	UART2_TS_ACC_TXD 5 25
J17	UART_50S	UART	UART4_WLAN_RXD 5 14
J16	UART_50S	UART	UART4_WLAN_TXD 5 14
J15	UART_50S	UART	UART1_BB_CTS_L 5 26
J14	UART_50S	UART	UART1_BB_RTS_L 5 26
J13	UART_50S	UART	UART1_BB_TXD 5 25 26
J12	UART_50S	UART	UART1_BB_RXD 5 25 26
J11	UART_50S	UART	UART3_BT_CTS_L 5 14
J10	UART_50S	UART	UART3_BT_RTS_L 5 14
J9	UART_50S	UART	UART3_BT_RXD 5 14
J8	UART_50S	UART	UART3_BT_TXD 5 14
J7	UART_50S	UART	UART6_AP_RXD 5 25
J6	UART_50S	UART	UART6_AP_TXD 5 25

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J19	SPI_50S	SPI	SPI3_GRAPE_MISO 5 16
J18	SPI_50S	SPI	SPI3_GRAPE_MOSI 5 16
J17	SPI_50S	SPI	SPI3_GRAPE_SCLK 5 16
J16	SPI_50S	SPI	SPI3_GRAPE_CS_L 5 16
J15	SPI_50S	SPI	SPI2_IPC_MISO
J14	SPI_50S	SPI	SPI2_IPC_MOSI
J13	SPI_50S	SPI	SPI2_IPC_SCLK
J12	SPI_50S	SPI	GPIO_BB_HSIC_RESUME 5 26
J24	SPI_50S	SPI	SPI1_CODEC_MISO 5 18
J23	SPI_50S	SPI	SPI1_CODEC_MOSI 5 18
J22	SPI_50S	SPI	SPI1_CODEC_SCLK 5 18
J21	SPI_50S	SPI	SPI1_CODEC_CS_L 5 18

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J150		DWI	DWI_AP_CLK 6 30
J151		DWI	DWI_AP_DI 6 30
J154		DWI	DWI_AP_DO 6 30

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J16		JTAG	JTAG_AP_TCK 4 25
J17		JTAG	JTAG_AP_TMS 4 25
J18		JTAG	JTAG_AP_TDI 4
J19		JTAG	TP_JTAG_AP_TDO 4
J20		RST	JTAG_AP_TRST_L 4 10 39

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J1	I2C_50S	I2C	I2C1_SDA_1V8 5 22
J2	I2C_50S	I2C	I2C1_SCL_1V8 5 22
J3	I2C_50S	I2C	I2C0_SDA_1V8 5 19 25 30
J4	I2C_50S	I2C	I2C0_SCL_1V8 5 19 25 30
J5	I2C_50S	I2C	I2C2_SDA_3V0 5 22
J6	I2C_50S	I2C	I2C2_SCL_3V0 5 22
J7	I2C_50S	I2C	ISP0_CAM_RF_I2C_SCL 7 22
J8	I2C_50S	I2C	ISP0_CAM_RF_I2C_SDA 7 22
J9	I2C_50S	I2C	ISP1_CAM_FF_I2C_SCL 7 22
J10	I2C_50S	I2C	ISP1_CAM_FF_I2C_SDA 7 22
J11	I2C_50S	I2C	CONN_I2C1_SDA_1V8 20 22
J12	I2C_50S	I2C	CONN_I2C1_SCL_1V8 20 22
J13	I2C_50S	I2C	CONN_I2C2_SCL_3V0 20 22
J14	I2C_50S	I2C	CONN_I2C2_SDA_3V0 20 22
J15	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SCL 20 22
J16	I2C_50S	I2C	CONN_ISP0_CAM_RF_I2C_SDA 20 22
J17	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SCL 20 22
J18	I2C_50S	I2C	CONN_ISP1_CAM_FF_I2C_SDA 20 22

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J1		CRYSTAL	XTAL_AP_24M_I 4
J2		CRYSTAL	XTAL_AP_24M_O 4
J3		CRYSTAL	AP_24M_O 4
J20		CRYSTAL	PMU_XTAL 29
J21		CRYSTAL	PMU_EXTAL 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J106	I2S_50S	I2S	I2S0_CODEC_ASP_BCLK 5 18
J107	I2S_50S	I2S	I2S0_CODEC_ASP_LRCK 5 18
J108	I2S_50S	I2S	I2S0_CODEC_ASP_DIN 5 18
J109	I2S_50S	I2S	I2S0_CODEC_ASP_DOUT 5 18
J110	I2S_50S	I2S	I2S0_CODEC_ASP_SDOUT 18
J111	I2S_50S	I2S	I2S0_CODEC_ASP_MCK 5 36
J112	I2S_50S	I2S	I2S0_CODEC_ASP_MCK_R 5 18 36
J113	I2S_50S	I2S	I2S3_CODEC_XSP_BCLK 5 18
J114	I2S_50S	I2S	I2S3_CODEC_XSP_LRCK 5 18
J115	I2S_50S	I2S	I2S3_CODEC_XSP_DIN 5 18
J116	I2S_50S	I2S	I2S3_CODEC_XSP_DOUT 5 18
J117	I2S_50S	I2S	I2S0_CODEC_XSP_SDOUT
J118	I2S_50S	I2S	I2S2_BT_BCLK 5 14
J119	I2S_50S	I2S	I2S2_BT_LRCK 5 14
J120	I2S_50S	I2S	I2S2_BT_DIN 5 14
J121	I2S_50S	I2S	I2S2_BT_DOUT 5 14

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J1	USB_90D	USB	USB_AP_P 4 25
J2	USB_90D	USB	USB_AP_N 4 25
J244	USB_90D	USB	USB_BBMUX_BB_P 25 26
J245	USB_90D	USB	USB_BBMUX_BB_N 25 26
J246	USB_90D	USB	USB_TS_BBMUX_P 25
J247	USB_90D	USB	USB_TS_BBMUX_N 25
J248	USB_90D	USB	USB11_AP_BBMUX_P 4 25
J249	USB_90D	USB	USB11_AP_BBMUX_N 4 25
J250	USB_90D	USB	CONN_E75_DPAIR1_P 24 25
J251	USB_90D	USB	CONN_E75_DPAIR1_N 24 25
J252	USB_90D	USB	CONN_E75_DPAIR2_P 24 25
J253	USB_90D	USB	CONN_E75_DPAIR2_N 24 25
J254	USB_90D	USB	TS_E75_DPAIR1_P 25
J255	USB_90D	USB	TS_E75_DPAIR1_N 25
J256	USB_90D	USB	TS_E75_DPAIR2_P 25
J257	USB_90D	USB	TS_E75_DPAIR2_N 25

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	4:1_SPACING
HSIC_RDY	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
J135	HSIC	HSIC	HSIC3_BB_DATA 4 26
J136	HSIC	HSIC	HSIC3_BB_STB 4 26
J137	HSIC	HSIC	HSIC1_WLAN_DATA 4 14
J138	HSIC	HSIC	HSIC1_WLAN_STB 4 14
J139	HSIC	HSIC_RDY	GPIO_BB_HSIC_DEV_RDY 5 26
J140	HSIC	HSIC_RDY	GPIO_BB_HSIC_HOST_RDY 5 26
J141	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
J142	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_HOST_RDY 5 14 36
J143	HSIC	HSIC_RDY	GPIO_WLAN_HSIC_DEV_RDY 5 14

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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
J11A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_P	7 21
J11B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_N	7 21
J11C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<0>	7 21
J12A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<0>	7 21
J12B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<1>	7 21
J12C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<1>	7 21
J13A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_P	20 21
J13B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_N	20 21
J13C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<0>	20 21
J14A	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<0>	20 21
J14B	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<1>	20 21
J14C	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<1>	20 21
J15A	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P	7 21
J15B	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N	7 21
J15C	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0>	7 21
J16A	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0>	7 21
J16B	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P	20 21
J16C	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N	20 21
J17A	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0>	20 21
J17B	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0>	20 21

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E584	AUDIO_DIFF	AUDIO	HP_MIC_P	18
E585	AUDIO_DIFF	AUDIO	HP_MIC_N	18
E587	AUDIO_DIFF	AUDIO	L81_AIN2_P	18
E586	AUDIO_DIFF	AUDIO	L81_AIN2_N	18
E588	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT	19
E589	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT	19
E591	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N	19
E590	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P	19
E592	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT	19
E593	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT	19
E595	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N	19
E594	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P	19
E597	SPEAKER	AUDIO	SPKR_L_P	19
E596	SPEAKER	AUDIO	SPKR_L_N	19
E598	SPEAKER	AUDIO	SPKR_L_CONN_P	19
E599	SPEAKER	AUDIO	SPKR_L_CONN_N	19
E602	SPEAKER	AUDIO	SPKR_R_P	19
E601	SPEAKER	AUDIO	SPKR_R_N	19
E608	SPEAKER	AUDIO	SPKR_R_CONN_P	19
E607	SPEAKER	AUDIO	SPKR_R_CONN_N	19
E610	SPEAKER	AUDIO	SPKR_L_FLR	19
E611	SPEAKER	AUDIO	SPKR_R_FLR	19
E584	AUDIO_DIFF	AUDIO	SPKR_L_SES_N	19
E585	AUDIO_DIFF	AUDIO	SPKR_L_SES_P	19
E587	AUDIO_DIFF	AUDIO	SPKR_R_SES_N	19
E586	AUDIO_DIFF	AUDIO	SPKR_R_SES_P	19
E588	USB_90D	USB	MIKEY_TS_P	18 25
E589	USB_90D	USB	MIKEY_TS_N	18 25
E603	USB_90D	USB	L81_MBUS_P	18
E607	USB_90D	USB	L81_MBUS_N	18

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E430	EDP_90D	EDP	EDP_AUX_P	7 15
E431	EDP_90D	EDP	EDP_AUX_N	7 15
E433	EDP_50S	EDP	EDP_HPD	7 15
E435	EDP_90D	EDP	EDP_DATA_P<0>	7 15
E436	EDP_90D	EDP	EDP_DATA_N<0>	7 15
E438	EDP_90D	EDP	EDP_DATA_P<1>	7 15
E439	EDP_90D	EDP	EDP_DATA_N<1>	7 15
E441	EDP_90D	EDP	EDP_DATA_P<2>	7 15
E442	EDP_90D	EDP	EDP_DATA_N<2>	7 15
E444	EDP_90D	EDP	EDP_DATA_P<3>	7 15
E445	EDP_90D	EDP	EDP_DATA_N<3>	7 15
E447	EDP_90D	EDP	EDP_AUX_EMI_P	15
E448	EDP_90D	EDP	EDP_AUX_EMI_N	15
E450	EDP_90D	EDP	EDP_DATA_EMI_P<0>	15
E451	EDP_90D	EDP	EDP_DATA_EMI_N<0>	15
E453	EDP_90D	EDP	EDP_DATA_EMI_P<1>	15
E454	EDP_90D	EDP	EDP_DATA_EMI_N<1>	15
E456	EDP_90D	EDP	EDP_DATA_EMI_P<2>	15
E457	EDP_90D	EDP	EDP_DATA_EMI_N<2>	15
E459	EDP_90D	EDP	EDP_DATA_EMI_P<3>	15
E460	EDP_90D	EDP	EDP_DATA_EMI_N<3>	15
E462	EDP_90D	EDP	CONN_EDP_AUX_EMI_P	15
E463	EDP_90D	EDP	CONN_EDP_AUX_EMI_N	15
E465	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0>	15
E466	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0>	15
E468	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1>	15
E469	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1>	15
E471	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2>	15
E472	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2>	15
E474	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3>	15
E475	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3>	15

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E480	LED	LEDA	LED_IO1_A_R	30
E481	LED	LEDB	LED_IO1_B_R	30
E483	LED	LEDA	LED_IO2_A_R	30
E482	LED	LEDB	LED_IO2_B_R	30
E485	LED	LEDA	LED_IO3_A_R	30
E484	LED	LEDB	LED_IO3_B_R	30
E486	LED	LEDA	LED_IO4_A_R	30
E488	LED	LEDB	LED_IO4_B_R	30
E490	LED	LEDA	LED_IO5_A_R	30
E491	LED	LEDB	LED_IO5_B_R	30
E492	LED	LEDA	LED_IO6_A_R	30
E493	LED	LEDB	LED_IO6_B_R	30
E494	LED	LEDA	LED_IO_1_A	15 30
E495	LED	LEDB	LED_IO_1_B	15 30
E496	LED	LEDA	LED_IO_2_A	15 30
E497	LED	LEDB	LED_IO_2_B	15 30
E498	LED	LEDA	LED_IO_3_A	15 30
E499	LED	LEDB	LED_IO_3_B	15 30
E500	LED	LEDA	LED_IO_4_A	15 30
E501	LED	LEDB	LED_IO_4_B	15 30
E502	LED	LEDA	LED_IO_5_A	15 30
E504	LED	LEDB	LED_IO_5_B	15 30
E505	LED	LEDA	LED_IO_6_A	15 30
E506	LED	LEDB	LED_IO_6_B	15 30

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
E576		BOARD_TEMP	BOARD_TEMP1	30 32
E574		BOARD_TEMP	BOARD_TEMP2	30 32
E570	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	30
E571	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	30
E573	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	30
E572	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	30
E580	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	30
E581	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	30
E583	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	30
E582	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	30
E602	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	30
E603	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	30
E604	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	30
E605	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	30

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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
J22	DDR_50S	DDR	DDR0_CA<9..0>	8 11
J22	DDR_50S	DDR	DDR0_DM<3..0>	8 11
J22	DDR_90D	DDR	DDR0_CK_P	8 11
J22	DDR_90D	DDR	DDR0_CK_N	8 11
J22	DDR_50S	DDR	DDR0_CKE<1..0>	8 11
J22	DDR_50S	DDR	DDR0_CSN<2..0>	8 11
J22	DDR_50S	DDR	DDR0_ZQ	11
J23	DDR_50S	DDR	DDR0_DQ<7..0>	8 11
J23	DDR_90D	DDR	DDR0_DQS_P<0>	8 11
J23	DDR_90D	DDR	DDR0_DQS_N<0>	8 11
J23	DDR_50S	DDR	DDR0_DQ<15..8>	8 11
J23	DDR_90D	DDR	DDR0_DQS_P<1>	8 11
J23	DDR_90D	DDR	DDR0_DQS_N<1>	8 11
J23	DDR_50S	DDR	DDR0_DQ<23..16>	8 11
J23	DDR_90D	DDR	DDR0_DQS_P<2>	8 11
J23	DDR_90D	DDR	DDR0_DQS_N<2>	8 11
J23	DDR_50S	DDR	DDR0_DQ<31..24>	8 11
J23	DDR_90D	DDR	DDR0_DQS_P<3>	8 11
J24	DDR_90D	DDR	DDR0_DQS_N<3>	8 11
J20	DDR_50S	DDR	DDR1_CA<9..0>	8 11
J20	DDR_50S	DDR	DDR1_DM<3..0>	8 11
J20	DDR_90D	DDR	DDR1_CK_P	8 11
J20	DDR_90D	DDR	DDR1_CK_N	8 11
J20	DDR_50S	DDR	DDR1_CKE<1..0>	8 11
J20	DDR_50S	DDR	DDR1_CSN<2..0>	8 11
J20	DDR_50S	DDR	DDR1_ZQ	11
J21	DDR_50S	DDR	DDR1_DQ<7..0>	8 11
J20	DDR_90D	DDR	DDR1_DQS_P<0>	8 11
J21	DDR_90D	DDR	DDR1_DQS_N<0>	8 11
J21	DDR_50S	DDR	DDR1_DQ<15..8>	8 11
J21	DDR_90D	DDR	DDR1_DQS_P<1>	8 11
J21	DDR_90D	DDR	DDR1_DQS_N<1>	8 11
J21	DDR_50S	DDR	DDR1_DQ<23..16>	8 11
J21	DDR_90D	DDR	DDR1_DQS_P<2>	8 11
J21	DDR_90D	DDR	DDR1_DQS_N<2>	8 11
J21	DDR_50S	DDR	DDR1_DQ<31..24>	8 11
J21	DDR_90D	DDR	DDR1_DQS_P<3>	8 11
J22	DDR_90D	DDR	DDR1_DQS_N<3>	8 11
J18	DDR_50S	DDR	DDR2_CA<9..0>	8 12
J18	DDR_50S	DDR	DDR2_DM<3..0>	8 12
J18	DDR_90D	DDR	DDR2_CK_P	8 12
J18	DDR_90D	DDR	DDR2_CK_N	8 12
J18	DDR_50S	DDR	DDR2_CKE<1..0>	8 12
J18	DDR_50S	DDR	DDR2_CSN<2..0>	8 12
J18	DDR_50S	DDR	DDR2_ZQ	12
J19	DDR_50S	DDR	DDR2_DQ<7..0>	8 12
J18	DDR_90D	DDR	DDR2_DQS_P<0>	8 12
J19	DDR_90D	DDR	DDR2_DQS_N<0>	8 12
J19	DDR_50S	DDR	DDR2_DQ<15..8>	8 12
J19	DDR_90D	DDR	DDR2_DQS_P<1>	8 12
J19	DDR_90D	DDR	DDR2_DQS_N<1>	8 12
J19	DDR_50S	DDR	DDR2_DQ<23..16>	8 12
J19	DDR_90D	DDR	DDR2_DQS_P<2>	8 12
J19	DDR_90D	DDR	DDR2_DQS_N<2>	8 12
J19	DDR_50S	DDR	DDR2_DQ<31..24>	8 12
J19	DDR_90D	DDR	DDR2_DQS_P<3>	8 12
J20	DDR_90D	DDR	DDR2_DQS_N<3>	8 12
J38	DDR_50S	DDR	DDR3_CA<9..0>	8 12
J39	DDR_50S	DDR	DDR3_DM<3..0>	8 12
J41	DDR_90D	DDR	DDR3_CK_P	8 12
J44	DDR_90D	DDR	DDR3_CK_N	8 12
J43	DDR_50S	DDR	DDR3_CKE<1..0>	8 12
J47	DDR_50S	DDR	DDR3_CSN<2..0>	8 12
J48	DDR_50S	DDR	DDR3_ZQ	12
J37	DDR_50S	DDR	DDR3_DQ<7..0>	8 12
J37	DDR_90D	DDR	DDR3_DQS_P<0>	8 12
J37	DDR_90D	DDR	DDR3_DQS_N<0>	8 12
J37	DDR_50S	DDR	DDR3_DQ<15..8>	8 12
J37	DDR_90D	DDR	DDR3_DQS_P<1>	8 12
J37	DDR_90D	DDR	DDR3_DQS_N<1>	8 12
J37	DDR_50S	DDR	DDR3_DQ<23..16>	8 12
J37	DDR_90D	DDR	DDR3_DQS_P<2>	8 12
J37	DDR_90D	DDR	DDR3_DQS_N<2>	8 12
J37	DDR_50S	DDR	DDR3_DQ<31..24>	8 12
J37	DDR_90D	DDR	DDR3_DQS_P<3>	8 12
J38	DDR_90D	DDR	DDR3_DQS_N<3>	8 12

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
H68	NAND_50S	NAND0	FMI0_AD<0>	6 13
H69	NAND_50S	NAND0	FMI0_AD<1>	6 13
H70	NAND_50S	NAND0	FMI0_AD<2>	6 13
H71	NAND_50S	NAND0	FMI0_AD<3>	6 13
H72	NAND_50S	NAND0	FMI0_AD<4>	6 13
H73	NAND_50S	NAND0	FMI0_AD<5>	6 13
H74	NAND_50S	NAND0	FMI0_AD<6>	6 13
H75	NAND_50S	NAND0	FMI0_AD<7>	6 13
H76	NAND_50S	NAND0	FMI0_ALE	6 13
H77	NAND_50S	NAND0	FMI0_CE0_L	6 13
H78	NAND_50S	NAND0	TP_FMI0_CE1_L	
H132	NAND_50S	NAND0	TP_FMI0_CE2_L	
H132	NAND_50S	NAND0	TP_FMI0_CE3_L	
H132	NAND_50S	NAND0	TP_FMI0_CE4_L	
H132	NAND_50S	NAND0	TP_FMI0_CE5_L	
H132	NAND_50S	NAND0	TP_FMI0_CE6_L	
H132	NAND_50S	NAND0	TP_FMI0_CE7_L	
H132	NAND_50S	NAND0	FMI0_CLE	6 13
H132	NAND_50S	NAND0	FMI0_DQS	6 13
H133	NAND_50S	NAND0	FMI0_RE_L	6 13
H133	NAND_50S	NAND0	FMI0_WE_L	6 13
H134	NAND_50S	NAND1	FMI1_AD<0>	6 13
H135	NAND_50S	NAND1	FMI1_AD<1>	6 13
H135	NAND_50S	NAND1	FMI1_AD<2>	6 13
H135	NAND_50S	NAND1	FMI1_AD<3>	6 13
H135	NAND_50S	NAND1	FMI1_AD<4>	6 13
H140	NAND_50S	NAND1	FMI1_AD<5>	6 13
H140	NAND_50S	NAND1	FMI1_AD<6>	6 13
H140	NAND_50S	NAND1	FMI1_AD<7>	6 13
H140	NAND_50S	NAND1	FMI1_ALE	6 13
H140	NAND_50S	NAND1	FMI1_CE0_L	6 13
H140	NAND_50S	NAND1	TP_FMI1_CE2_L	
H140	NAND_50S	NAND1	TP_FMI1_CE4_L	
H140	NAND_50S	NAND1	TP_FMI1_CE5_L	
H150	NAND_50S	NAND1	TP_FMI1_CE6_L	
H150	NAND_50S	NAND1	TP_FMI1_CE7_L	
H150	NAND_50S	NAND1	FMI1_CLE	6 13
H150	NAND_50S	NAND1	FMI1_DQS	6 13
H150	NAND_50S	NAND1	FMI1_RE_L	6 13
H150	NAND_50S	NAND1	FMI1_WE_L	6 13

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
K24	WIFI_50S		50_WLAN_G	27
K24	WIFI_50S		50_WLAN_A	27
K24	WIFI_50S		50_WLAN_G_1	27
K24	WIFI_50S		50_WLAN_A_DIPLX	27
K24	WIFI_50S		50_WIFI_ANT_FD_2	
K25	WIFI_50S		50_WIFI_ANT_FD_1	
K25	WIFI_50S		50_WIFI_ANT_FD	

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
H190		PWR	PPVREF_DDR0_CA	11 39
H190		PWR	PPVREF_DDR0_DQ	11 39
H190		PWR	PPVREF_DDR1_CA	11 39
H190		PWR	PPVREF_DDR1_DQ	11 39
H190		PWR	PPVREF_DDR2_CA	12 39
H190		PWR	PPVREF_DDR2_DQ	12 39
H190		PWR	PPVREF_DDR3_CA	12 39
H190		PWR	PPVREF_DDR3_DQ	12 39

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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PP_PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1.1V	PP_PWR	PWR	BUCK0A_LX0	29
1.1V	PP_PWR	PWR	BUCK0A_LX1	29
1.1V	PP_PWR	PWR	BUCK0A_FB	29
1.1V	PP_PWR	PWR	PP1V1_CPU0_FET	29 30
1.1V	PP_PWR	PWR	BUCK0B_LX0	29
1.1V	PP_PWR	PWR	BUCK0B_LX1	29
1.1V	PP_PWR	PWR	BUCK0B_FB	29
1.1V	PP_PWR	PWR	PP1V1_CPU1_FET	29 30
1.1V	PP_PWR	PWR	BUCK0C_LX0	29
1.1V	PP_PWR	PWR	BUCK0C_FB	29
1.1V	PP_PWR	PWR	PP1V1_CPUB	29 34
1.2V	PP_PWR	PWR	BUCK2_LX0	29
1.2V	PP_PWR	PWR	BUCK2_LX1	29
1.2V	PP_PWR	PWR	BUCK2_LX2	29
1.2V	PP_PWR	PWR	BUCK2_FB	29
1.2V	PP_PWR	PWR	PP1V2_SOC	29 34
1.8V	PP_PWR	PWR	BUCK3_LX0	29
1.8V	PP_PWR	PWR	BUCK3_FB	29
1.8V	PP_PWR	PWR	PP1V8_S2R	29 34
1.2V	PP_PWR	PWR	BUCK4_LX0	29
1.2V	PP_PWR	PWR	BUCK4_FB	29
1.2V	PP_PWR	PWR	PP1V2_S2R	29 34
1.1V	PP_PWR	PWR	BUCK5_LX0	29
1.1V	PP_PWR	PWR	BUCK5_FB	29
3.3V	PP_PWR	PWR	PP3V3_OUT	29 34
3.0V	PP_PWR	PWR	PP3V0_GRAPE	29 34
1.7V	PP_PWR	PWR	PP1V7_VA_VCP	19 29 34
3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
3.2V	PP_PWR	PWR	LDO5	29
3.3V	PP_PWR	PWR	PP3V3_ACC	29 34
3.0V	PP_PWR	PWR	PP3V0_S2R_HALL	29 34
3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
3.0V	PP_PWR	PWR	PP3V0_IO	29 34
3.0V	PP_PWR	PWR	PP3V0_SENSOR	29 34
2.8V	PP_PWR	PWR	PP2V8_CAM	29 34
1.0V	PP_PWR	PWR	PP1V0	29 34
1.1V	PP_PWR	PWR	PP1V1_SRAM	29 34
1.8V	PP_PWR	PWR	PP1V8_ALWAYS	29 34
1.2V	PP_PWR	PWR	PP1V2	29 34
	PP_PWR	PWR	DSP_SW	
1.8V	PP_PWR	PWR	PP1V8	29 32 34
1.8V	PP_PWR	PWR	PP1V8_GRAPE	
4.7V	PP_PWR	PWR	PPVCC_MAIN	15 25 29 30 34
4.2V	PWR500	PWR	PPBATT_VCC	29 32 34
6.0V	PP_PWR	PWR	PP6V0_LCM_HI	30
6.0V	PP_PWR	PWR	LCM_LX	30
6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST	30
5.25V	PP_PWR	PWR	PP5V25_VLCM1	
1.1V	PP_PWR	PWR	PP1V1_CPU0	30 34
1.1V	PP_PWR	PWR	PP1V1_CPU1	30 34
20.4V	PP_PWR	PWR	PPLED_OUT_A	30 34
20.4V	PP_PWR	PWR	PPLED_OUT_B	30 34
1.8V	PP_PWR	PWR	PP1V8_PL0_F	4
1.0V	PP_PWR	PWR	PP1V0_MIPI_PLL_F	7
1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX	7
1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX	
3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR	15
3.3V	PP_PWR	PWR	PP3V3_LCDVDD_SW_F	15
20.4V	PWR500	PWR	PPLED_BACK_REG_B	15
20.4V	PP_PWR	PWR	PPLED_BACK_REG_A	15
6V	PP_PWR	PWR	PPVBUS_USB_EMI	23 34
0.6V	PP_PWR	PWR	PPVREF_DDR0_CA	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR0_DQ	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR1_CA	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR1_DQ	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR2_CA	12 38
0.6V	PP_PWR	PWR	PPVREF_DDR2_DQ	12 38
0.6V	PP_PWR	PWR	PPVREF_DDR3_CA	12 38
0.6V	PP_PWR	PWR	PPVREF_DDR3_DQ	12 38
	PP_PWR	PWR	DAC_AP_VREF	7
4.6V	PP_PWR	PWR	BATT_POS_RC	29
4.6V	PP_PWR	PWR	BATT_VCC_WLAN	27
1.8V	PP_PWR	PWR	PP_WLAN_VDDIO_1V8	27
3.55V	PP_PWR	PWR	LDO10	18 29

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_PH

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
VOLTAGE=0V	GND	GND	GND	
VOLTAGE=0V	GND	GND	GND_AUDIO_CODEC	18
VOLTAGE=0V	GND	GND	GND_SPKR_AMP1	
VOLTAGE=0V	GND	GND	GND_SPKR_AMP2	
VOLTAGE=0V	GND	GND	AGND_U3000	16
VOLTAGE=0V	GND	GND	J2200_29_GND	15
VOLTAGE=0V	GND	GND	J2200_36_GND	15
VOLTAGE=0V	GND	GND	J2200_43_GND	15

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
		RST	BB_TRST_L
		RST	DBG_RST
		RST	DEBUG_RST_L
		RST	GSM_TXBURST_IND
		RST	JTAG_AP_TRST_L 4 10 36
		RST	RST_AP_1V8_L
		RST	RST_AP_L 4 25 26 30
		RST	GPIO_BB_RST_L 5 26
		RST	RST_BB_PMU_L
		RST	RST_BT_L
		RST	RST_DET_L
		GRAPE	RST_GRAPE_L
		RST	RST_L63_L
		RST	RST_PMU_IN
		RST	RST_WLAN_L
		RST	SIMCRD_RST
		RST	UD881_RST
		RST	UD882_RST

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