



Special Thanks!

130877

TRALOL

weaver

wins200786

QueenSoft

Mihail tm

abraziff

iPad 2

Professional Schematic!
A1395, A1396, A1397 (k94ap)
Wites OM Tesla



Special Thanks!

...:Neo:...

~AhmedLeO~

Gecko UK

Mobileinfo

Hobson

Noobfix

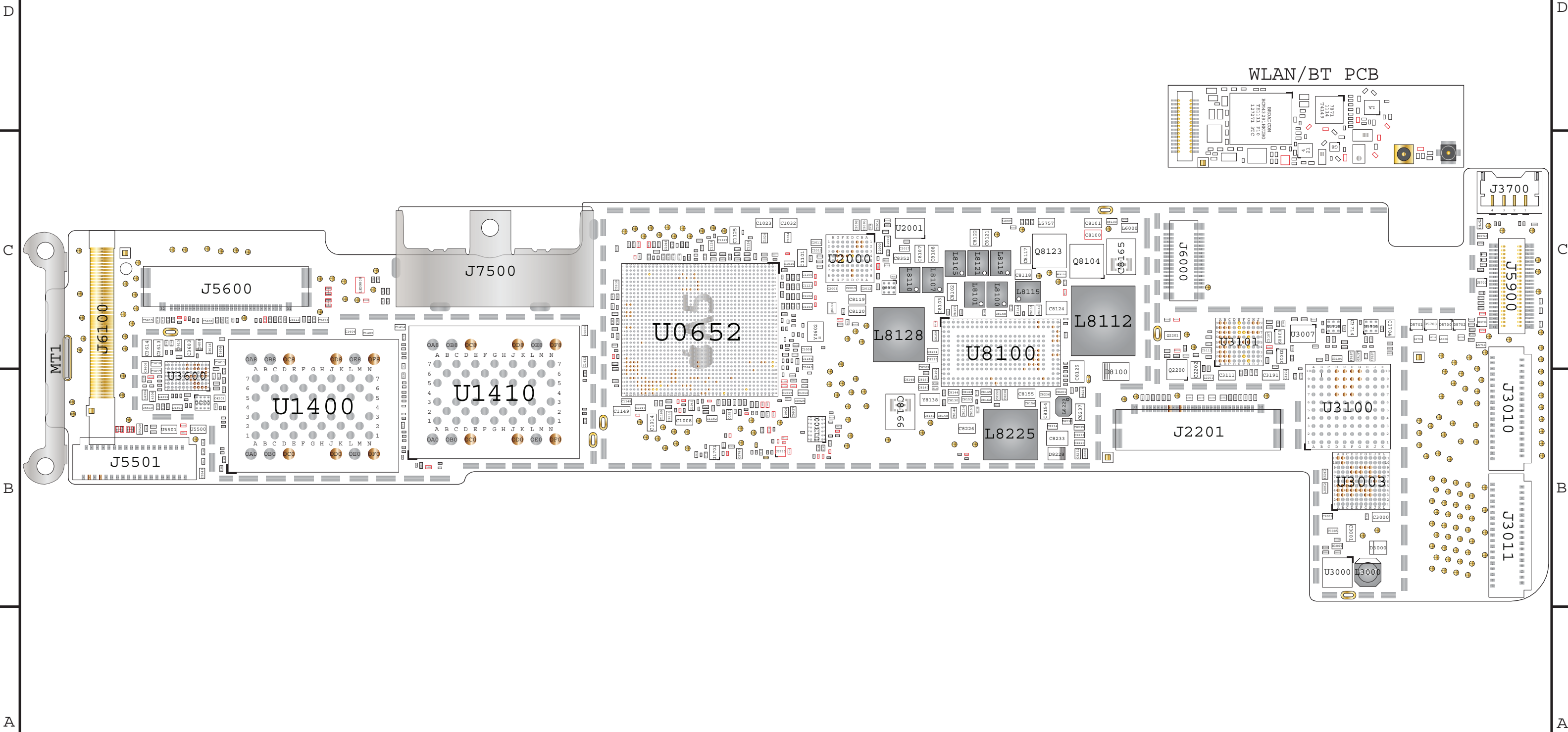
DataRus

Kostelectronics

diesel57

8 7 6 5 4 3 2 1

Wites OM Tesla
 READ BEFORE PROCEED!
 ● PRINTS MARKED WITH COPPER ARE NC, EMPTY!
 ● PRINTS MARKED WITH GOLD ARE CONNECTED ONLY
 TO TEST POINTS NO OTHER CIRCUIT!
 IF YOU REBALL U1300 LOOK CAREFUL IF B9 AND B10
 THAT LOOK LIKE A JUMPER IS REMOVED TOUCH WILL
 NOT WORK IF SO HAPPEN MAKE A JUMPER ON THE IC!
 □ NOSTUFF COMPONENTS JUST LOOK ON BOARD
 THEY ARE NOT MOUNTED (MISSING)!



WLAN/BT PCB

820-2875-05 MLB TOP PCB

8 7 6 5 4 3 2 1



COMPEQ
HF/e1
820-XXXX-X

820-2875-05 MLB BOTTOM PCB

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT REV. A

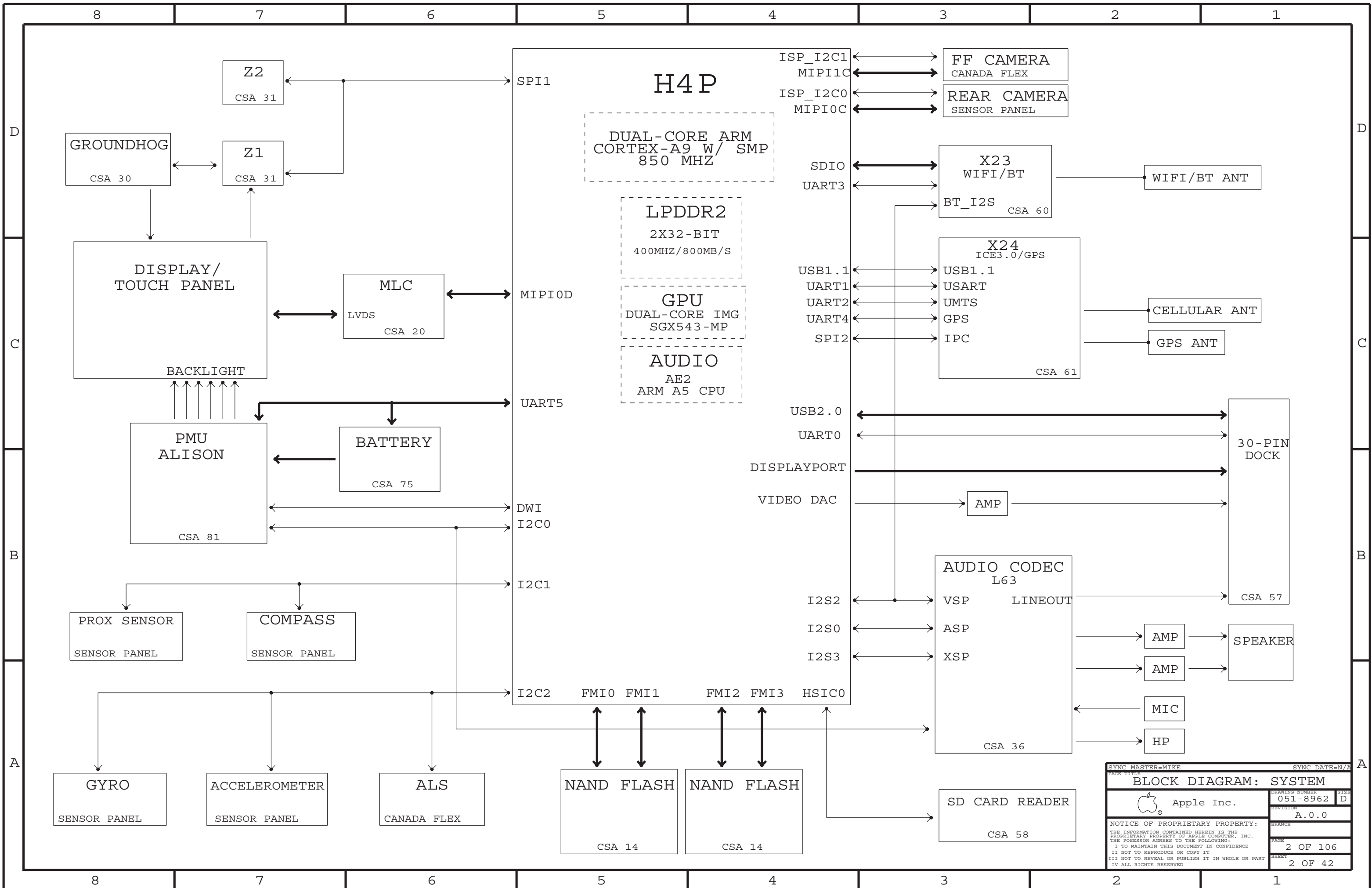
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A	0001052699	PRODUCTION RELEASED	2011-01-10

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

PDF	CSA	CONTENTS	SYNC	MASTER	DATE	PDF	CSA	CONTENTS	SYNC	MASTER	DATE
1	1	TABLE OF CONTENTS		MIKE	N/A	32	73	POWER: ALIASES		YOSH	N/A
2	2	BLOCK DIAGRAM: SYSTEM		MIKE	N/A	33	75	POWER: BATTERY CONNECTOR		YOSH	N/A
3	5	BOM TABLE		MIKE	N/A	34	81	POWER: PMU		YOSH	N/A
4	6	AP: MAIN		JAMES	N/A	35	82	POWER: PMU		YOSH	N/A
5	7	AP: I/Os		JAMES	N/A	36	83	POWER: 3.3V VR		YOSH	N/A
6	8	AP: NAND		JAMES	N/A	37	90	DEBUG AND MISC		MIKE	N/A
7	9	AP: TV,DP,MIPI		JAMES	N/A	38	93	FCT/ICT TEST/BRACKETS		MIKE	N/A
8	10	AP: PWR		JAMES	N/A	39	100	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
9	11	AP: PWR		JAMES	N/A	40	101	CONSTRAINTS: ASSIGNMENTS		MIKE	N/A
10	12	AP: MISC & ALIASES		JAMES	N/A	41	102	CONSTRAINTS: MLB RULES		MIKE	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES		JAMES	N/A	42	106	CONSTRAINTS: RF RULES		MIKE	N/A
12	14	NAND		JONATHAN	N/A						
13	17	VIDEO: DISPLAY PORT		JAMES	N/A						
14	20	VIDEO: MLC		MIKE	N/A						
15	21	VIDEO: MLC ALIASES		MIKE	N/A						
16	22	VIDEO: LVDS CONNECTOR		ALEX	N/A						
17	30	GRAPE: GROUNDHOG, CONN, BOOST		RAMSIN	N/A						
18	31	GRAPE: Z1, Z2		RAMSIN	N/A						
19	36	AUDIO: L63 CODEC		LENG	N/A						
20	37	AUDIO: SPEAKER AMP		LENG	N/A						
21	38	AUDIO: HEADPHONE OUT		LENG	N/A						
22	39	AUDIO: BLANK		LENG	N/A						
23	42	AUDIO: DETECT/MIC BIAS		LENG	N/A						
24	43	AUDIO: HP/MIC FILTERS		LENG	N/A						
25	54	CONNECTOR: CANADA FLEX CONN, SENSOR PANEL ALIASES		MARK B.	N/A						
26	55	CONNECTOR: CANADA FLEX FILTERS		MARK B.	N/A						
27	56	CONNECTOR: SENSOR PANEL CONNECTOR		MARK B.	N/A						
28	57	IO FLEX: DOCK COMPONENTS		JAMES	N/A						
29	59	IO FELX: B2B Connector		JAMES	N/A						
30	60	CONNECTOR: X23 WIFI/BT		MIKE	N/A						
31	61	CONNECTOR: X24 CELLULAR/GPS		MIKE	N/A						

DRAWING TITLE CHOPIN MLB		DRAWING NUMBER 051-8962	SIZE D
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DRAWING
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ABBREV=DRAWING



SYNC MASTER=MIKE		SYNC DATE=N/A	
BLOCK DIAGRAM: SYSTEM			
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE
16GB_PROD
32GB_PROD
64GB_PROD
BKLT_PLL
DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP
JTAG_TAP_NOT
SPEAKER
INTERNAL_MIC
PORTRAIT_DOCK
MLC_DEV
MLC_PROD
K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH, CHOPIN_AUDIO, MLB, K94	SCH1	
820-3069	1	PCBF, CHOPIN_AUDIO, MLB, K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE, GRAPE, MLB, K93/K94	FENCE1	
806-1397	1	CAN, GRAPE, MLB, K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE, CPU, MLB, K93/K94	FENCE2	
806-1399	1	CAN, CPU, MLB, K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE, NAND, MLB, K93/K94	FENCE3	
806-1401	1	CAN, NAND, MLB, K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DPC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DPC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DPC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

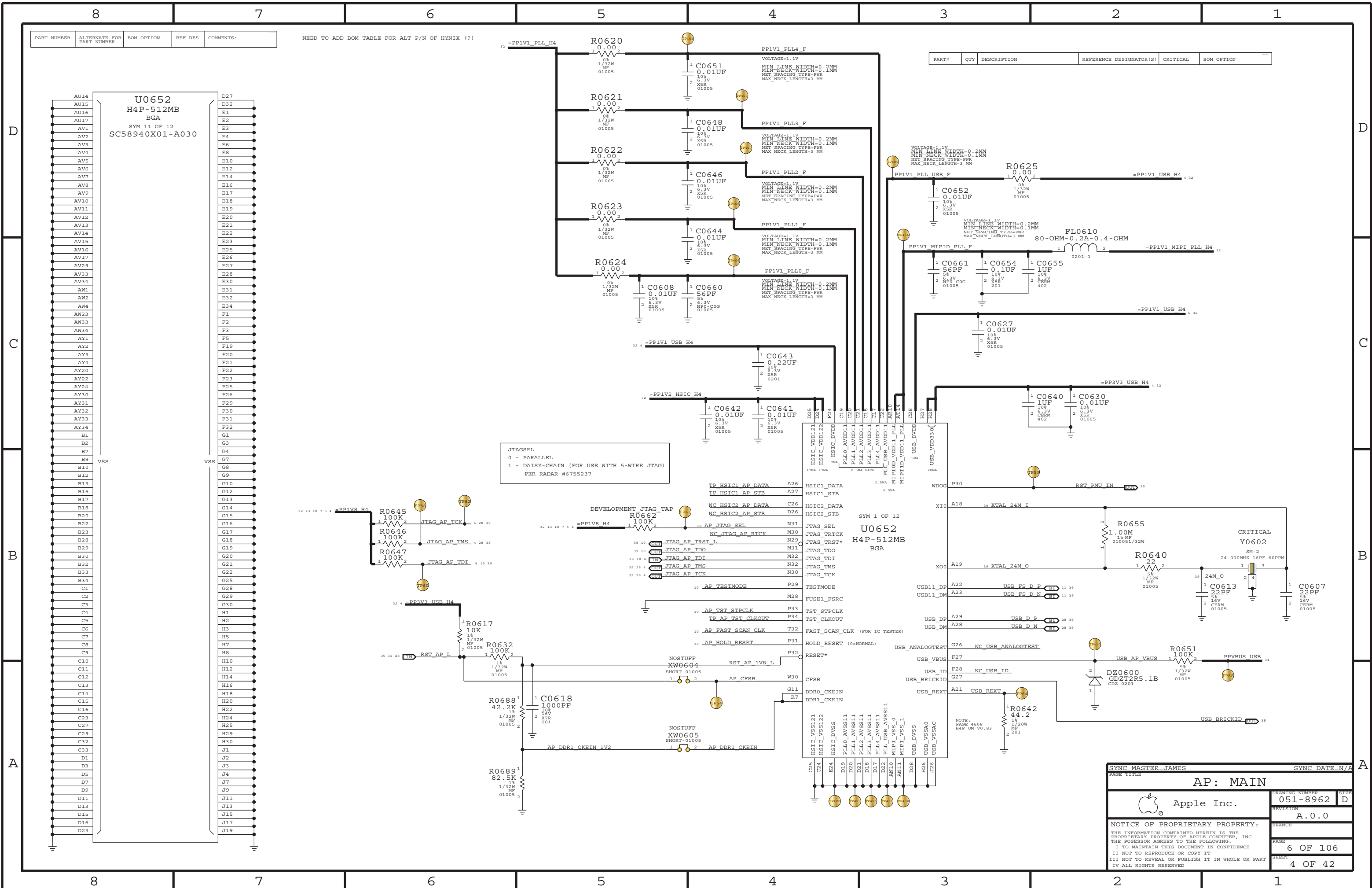
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825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

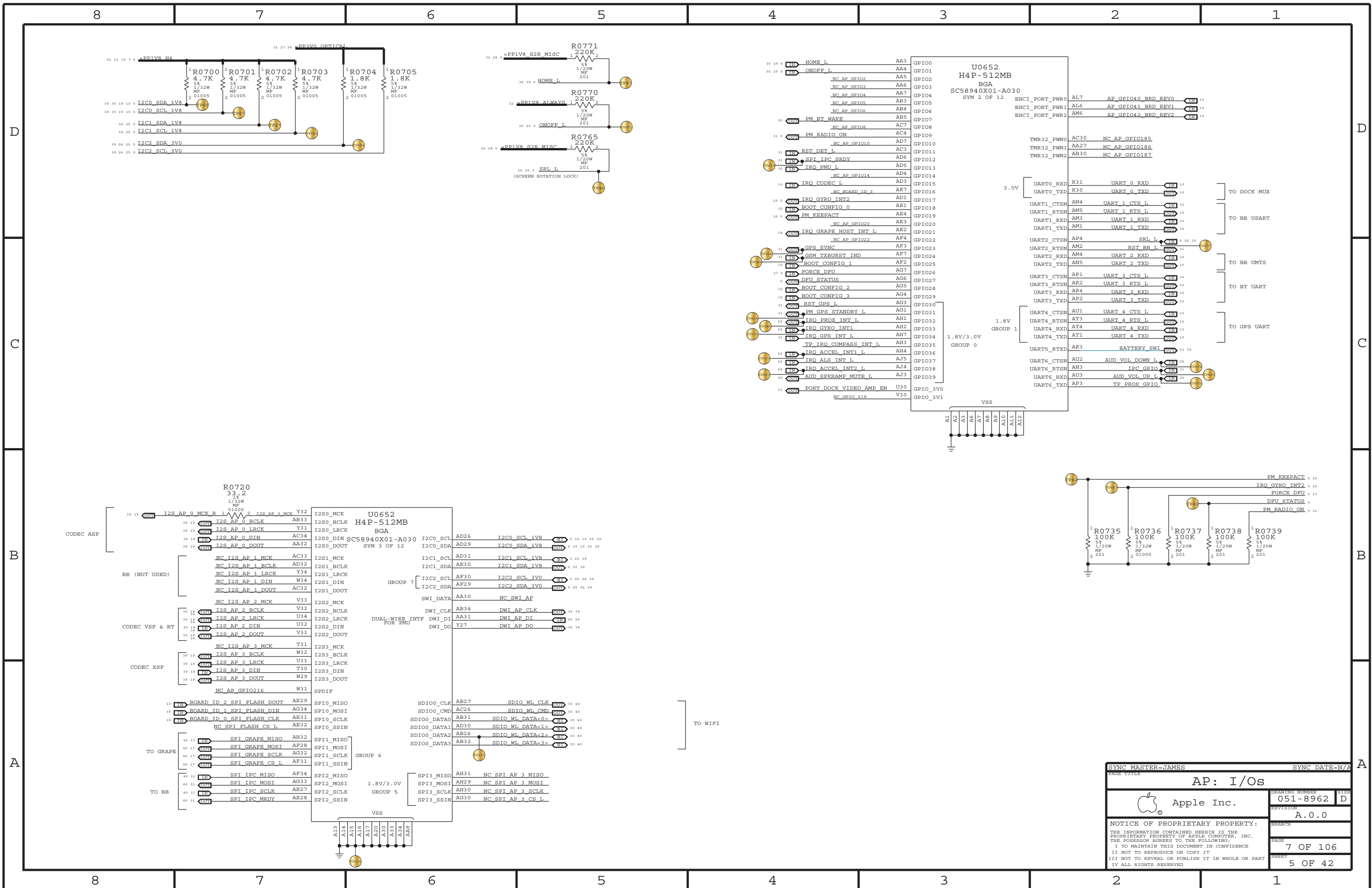
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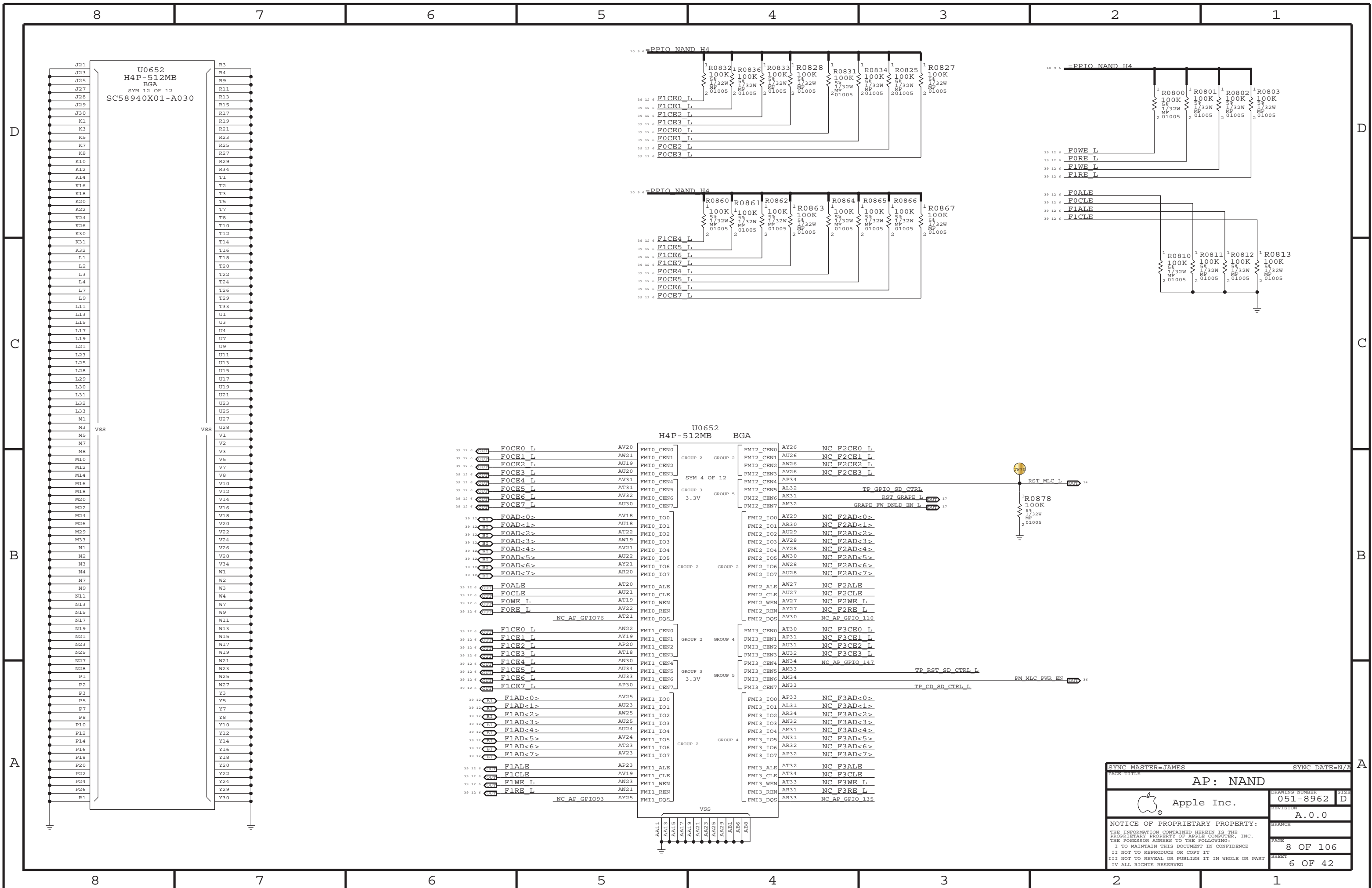
JTAGSEL
 0 - PARALLEL
 1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)
 PER RADAR #6755237

SYM 1 OF 12
 U0652
 H4P-512MB
 BGA

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8 7 6 5 4 3 2 1

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C

C

B

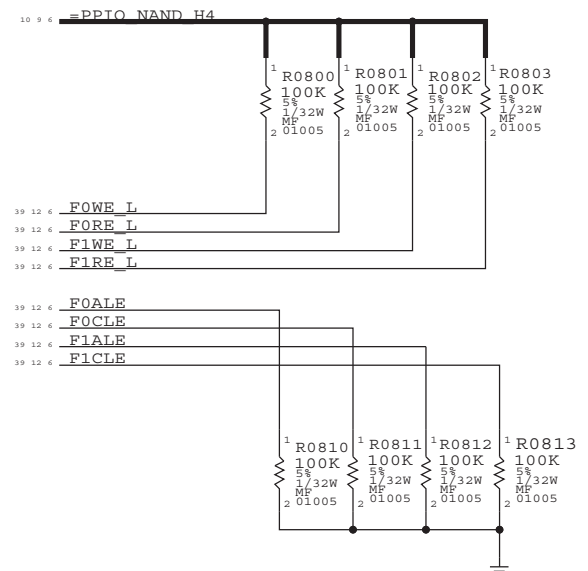
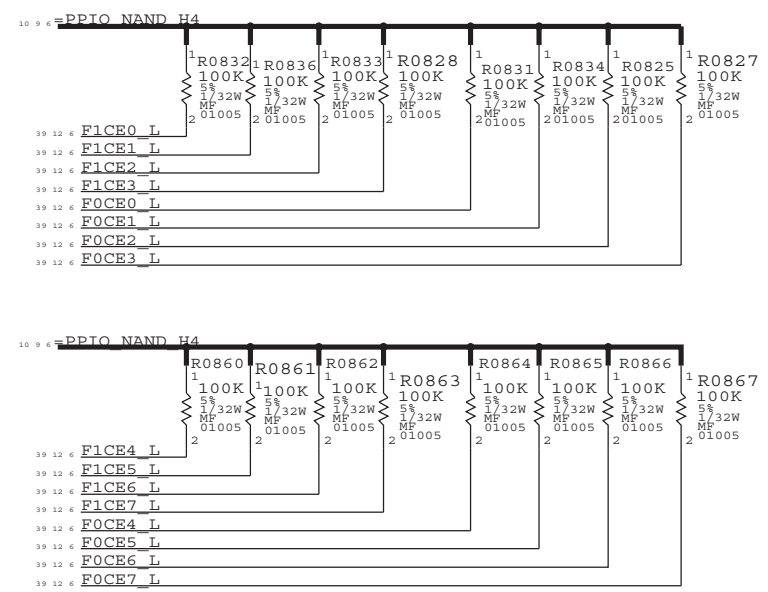
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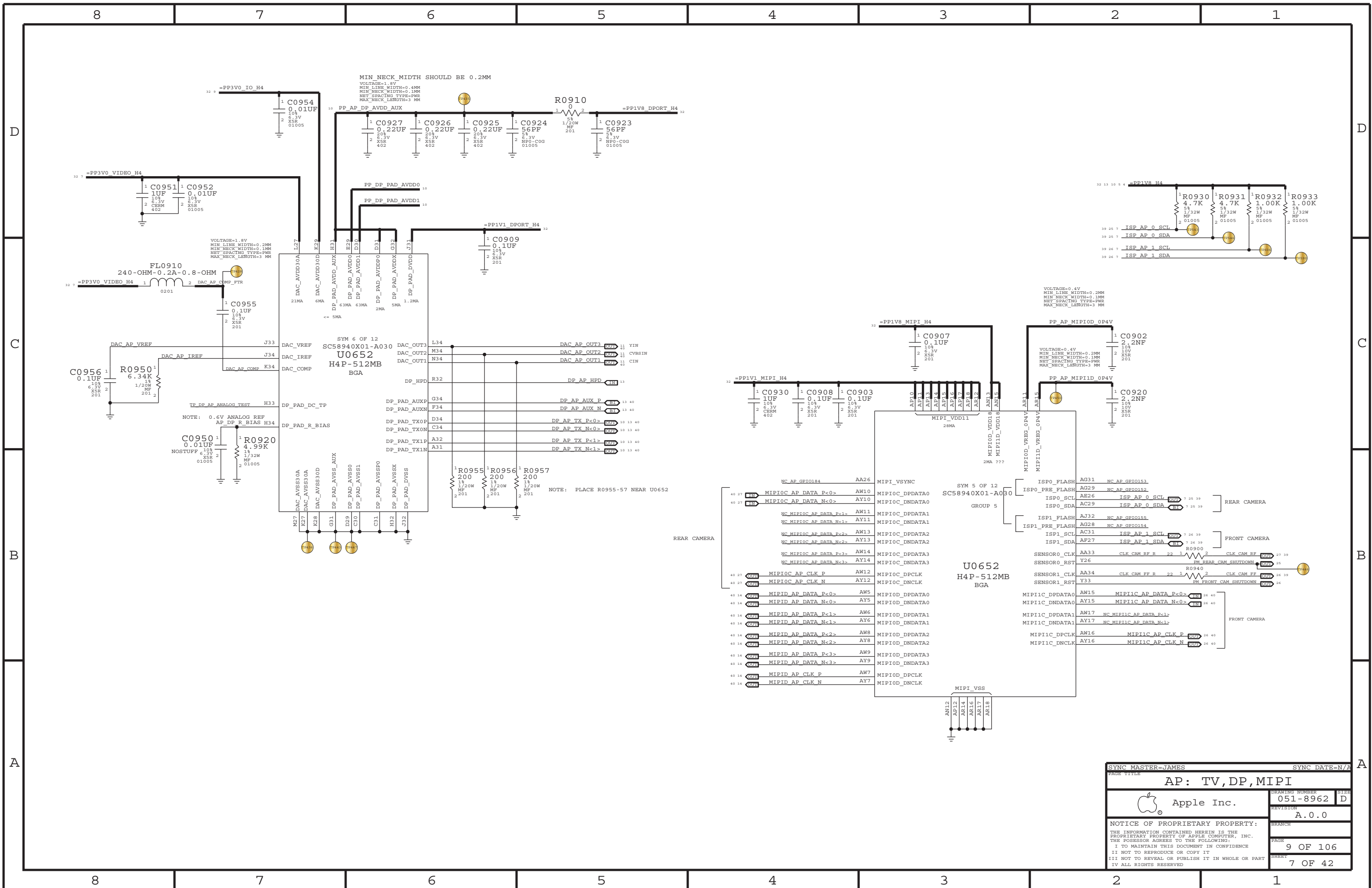
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H4P-512MB
BGA
SYM 12 OF 12
SC58940X01-A030



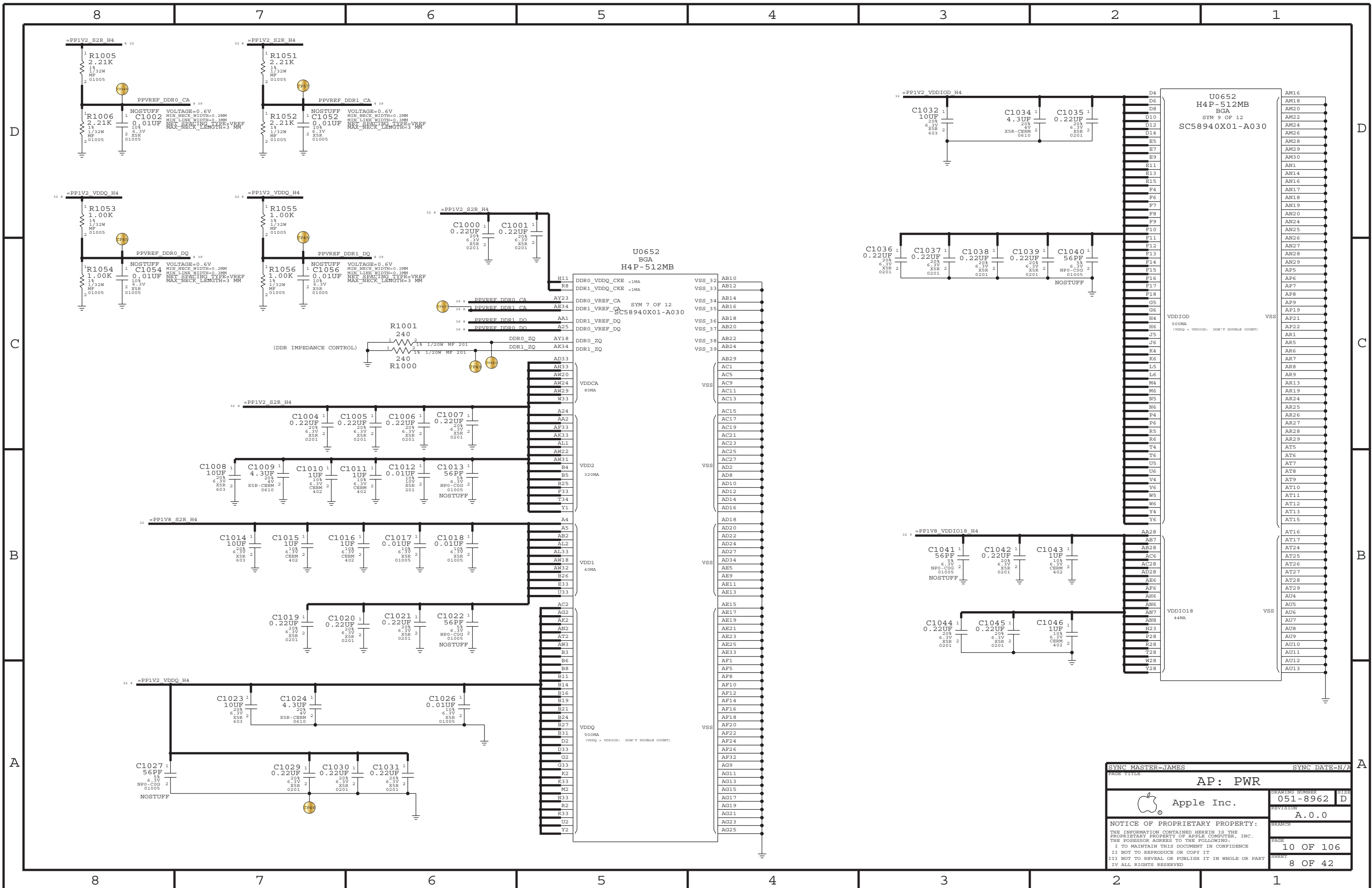
U0652
H4P-512MB
BGA

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	
39 12 6	FOCE0_L	AV20	FMIO_CEN0	GROUP 2	GROUP 2	FMIO_CEN0	AY26	NC F2CE0_L
39 12 6	FOCE1_L	AW21	FMIO_CEN1	GROUP 2	GROUP 2	FMIO_CEN1	AU26	NC F2CE1_L
39 12 6	FOCE2_L	AU19	FMIO_CEN2	GROUP 2	GROUP 2	FMIO_CEN2	AW26	NC F2CE2_L
39 12 6	FOCE3_L	AU20	FMIO_CEN3	GROUP 2	GROUP 2	FMIO_CEN3	AV26	NC F2CE3_L
39 12 6	FOCE4_L	AV31	FMIO_CEN4	GROUP 2	GROUP 2	FMIO_CEN4	AP34	NC F2CE4_L
39 12 6	FOCE5_L	AT31	FMIO_CEN5	GROUP 3	GROUP 5	FMIO_CEN5	AL32	TP GPIO_SD_CTRL
39 12 6	FOCE6_L	AV32	FMIO_CEN6	GROUP 3	GROUP 5	FMIO_CEN6	AK31	RST GRAPE_L
39 12 6	FOCE7_L	AU30	FMIO_CEN7	GROUP 3	GROUP 5	FMIO_CEN7	AM32	GRAPE_FW_DNLD_EN_L
39 12 6	F0AD<0>	AV18	FMIO_IO0	GROUP 2	GROUP 2	FMIO_IO0	AY29	NC F2AD<0>
39 12 6	F0AD<1>	AU18	FMIO_IO1	GROUP 2	GROUP 2	FMIO_IO1	AR30	NC F2AD<1>
39 12 6	F0AD<2>	AT22	FMIO_IO2	GROUP 2	GROUP 2	FMIO_IO2	AU29	NC F2AD<2>
39 12 6	F0AD<3>	AW19	FMIO_IO3	GROUP 2	GROUP 2	FMIO_IO3	AV28	NC F2AD<3>
39 12 6	F0AD<4>	AV21	FMIO_IO4	GROUP 2	GROUP 2	FMIO_IO4	AY28	NC F2AD<4>
39 12 6	F0AD<5>	AU22	FMIO_IO5	GROUP 2	GROUP 2	FMIO_IO5	AW30	NC F2AD<5>
39 12 6	F0AD<6>	AY21	FMIO_IO6	GROUP 2	GROUP 2	FMIO_IO6	AW28	NC F2AD<6>
39 12 6	F0AD<7>	AR20	FMIO_IO7	GROUP 2	GROUP 2	FMIO_IO7	AU28	NC F2AD<7>
39 12 6	FOALE	AT20	FMIO_ALE	GROUP 2	GROUP 2	FMIO_ALE	AW27	NC F2ALE
39 12 6	FOCLE	AU21	FMIO_CLE	GROUP 2	GROUP 2	FMIO_CLE	AU27	NC F2CLE
39 12 6	FOWE_L	AT19	FMIO_WEN	GROUP 2	GROUP 2	FMIO_WEN	AV27	NC F2WE_L
39 12 6	FORE_L	AV22	FMIO_REN	GROUP 2	GROUP 2	FMIO_REN	AY27	NC F2RE_L
39 12 6		AT21	FMIO_DQS	GROUP 2	GROUP 2	FMIO_DQS	AV30	NC AP GPIO 110
39 12 6	FICE0_L	AN22	FMIO_CEN0	GROUP 2	GROUP 4	FMIO_CEN0	AT30	NC F3CE0_L
39 12 6	FICE1_L	AY19	FMIO_CEN1	GROUP 2	GROUP 4	FMIO_CEN1	AP31	NC F3CE1_L
39 12 6	FICE2_L	AP20	FMIO_CEN2	GROUP 2	GROUP 4	FMIO_CEN2	AU31	NC F3CE2_L
39 12 6	FICE3_L	AT18	FMIO_CEN3	GROUP 2	GROUP 4	FMIO_CEN3	AU32	NC F3CE3_L
39 12 6	FICE4_L	AN30	FMIO_CEN4	GROUP 2	GROUP 4	FMIO_CEN4	AN34	NC AP GPIO 147
39 12 6	FICE5_L	AU34	FMIO_CEN5	GROUP 3	GROUP 5	FMIO_CEN5	AM33	TP RST_SD_CTRL_L
39 12 6	FICE6_L	AU33	FMIO_CEN6	GROUP 3	GROUP 5	FMIO_CEN6	AM34	PM MLC_PWR_EN
39 12 6	FICE7_L	AP30	FMIO_CEN7	GROUP 3	GROUP 5	FMIO_CEN7	AN33	TP CD_SD_CTRL_L
39 12 6	F1AD<0>	AV25	FMIO_IO0	GROUP 2	GROUP 4	FMIO_IO0	AP33	NC F3AD<0>
39 12 6	F1AD<1>	AU23	FMIO_IO1	GROUP 2	GROUP 4	FMIO_IO1	AL31	NC F3AD<1>
39 12 6	F1AD<2>	AW25	FMIO_IO2	GROUP 2	GROUP 4	FMIO_IO2	AR34	NC F3AD<2>
39 12 6	F1AD<3>	AU25	FMIO_IO3	GROUP 2	GROUP 4	FMIO_IO3	AN32	NC F3AD<3>
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39 12 6	F1CLE	AV19	FMIO_CLE	GROUP 2	GROUP 4	FMIO_CLE	AT34	NC F3CLE
39 12 6	F1WE_L	AN23	FMIO_WEN	GROUP 2	GROUP 4	FMIO_WEN	AT33	NC F3WE_L
39 12 6	F1RE_L	AN21	FMIO_REN	GROUP 2	GROUP 4	FMIO_REN	AR31	NC F3RE_L
39 12 6		AY25	FMIO_DQS	GROUP 2	GROUP 4	FMIO_DQS	AR33	NC AP GPIO 135

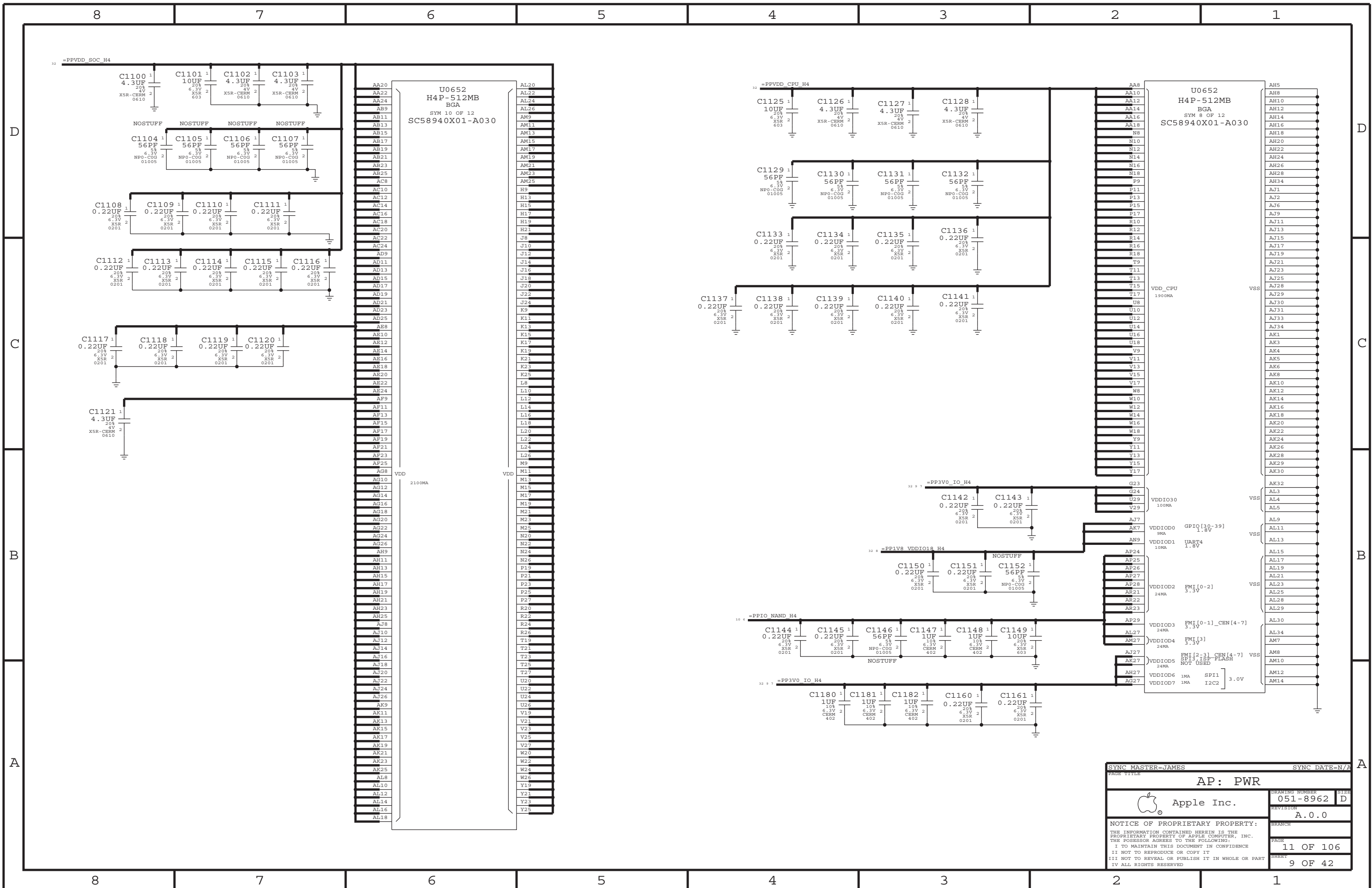
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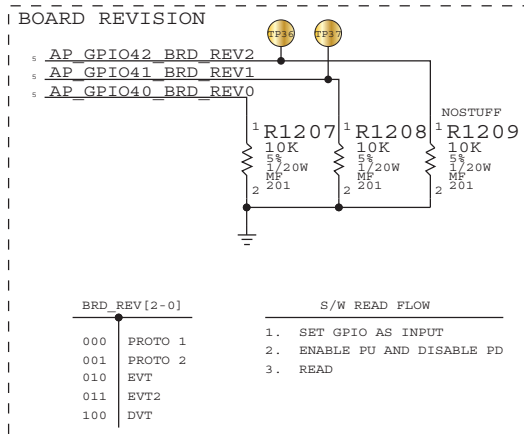
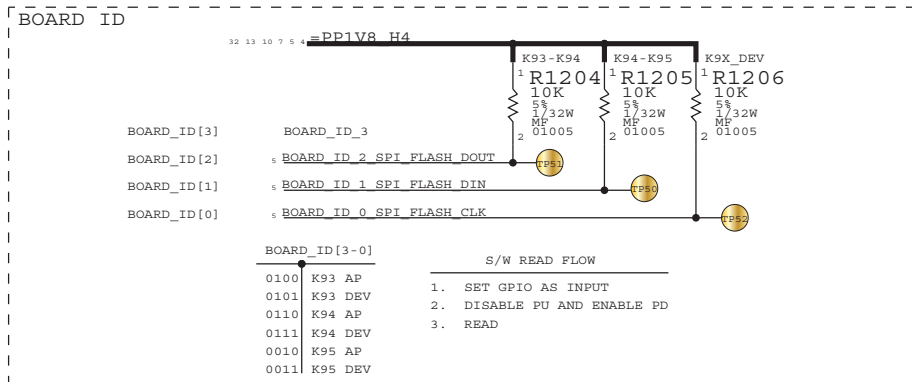
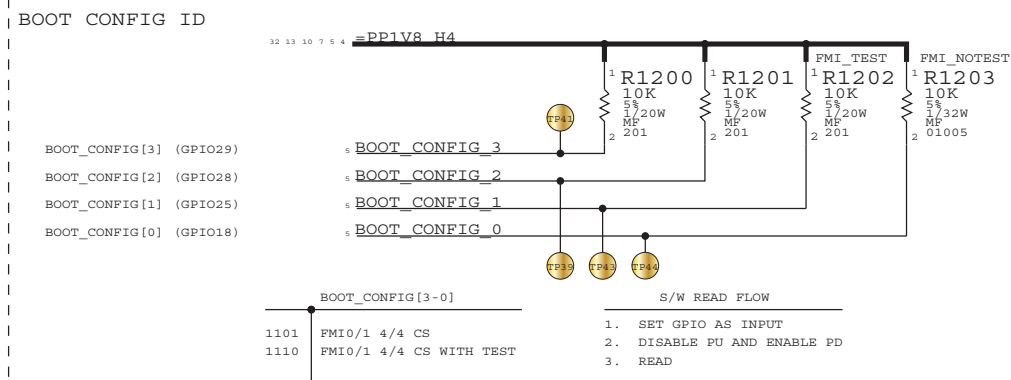
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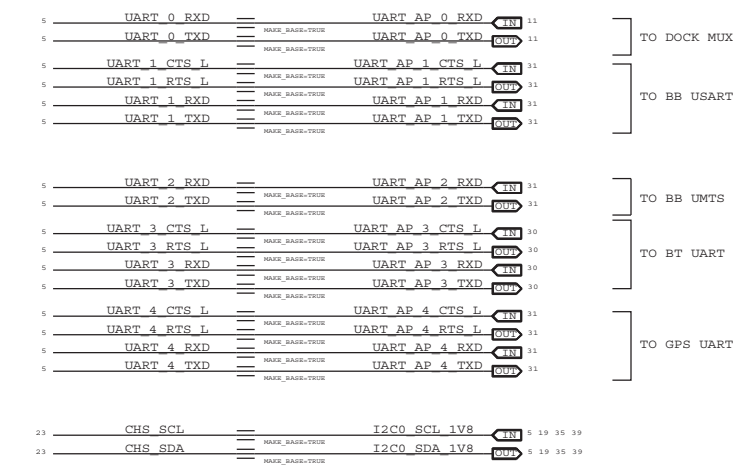
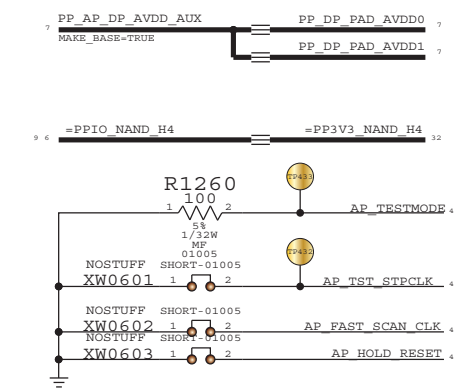
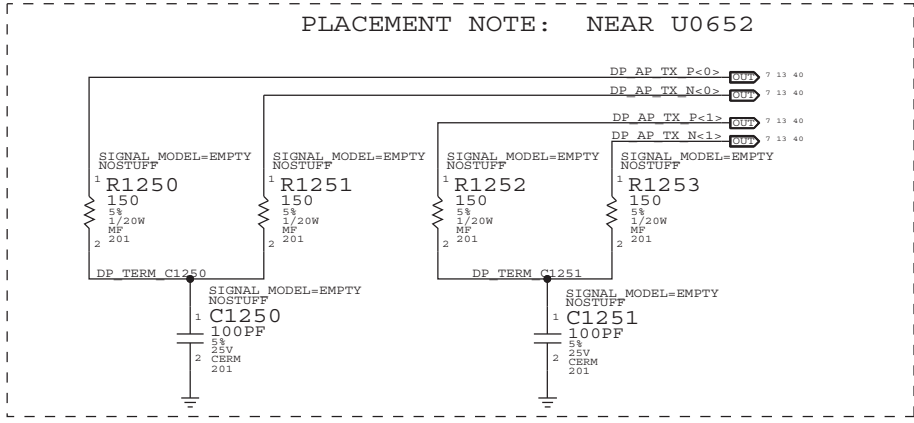
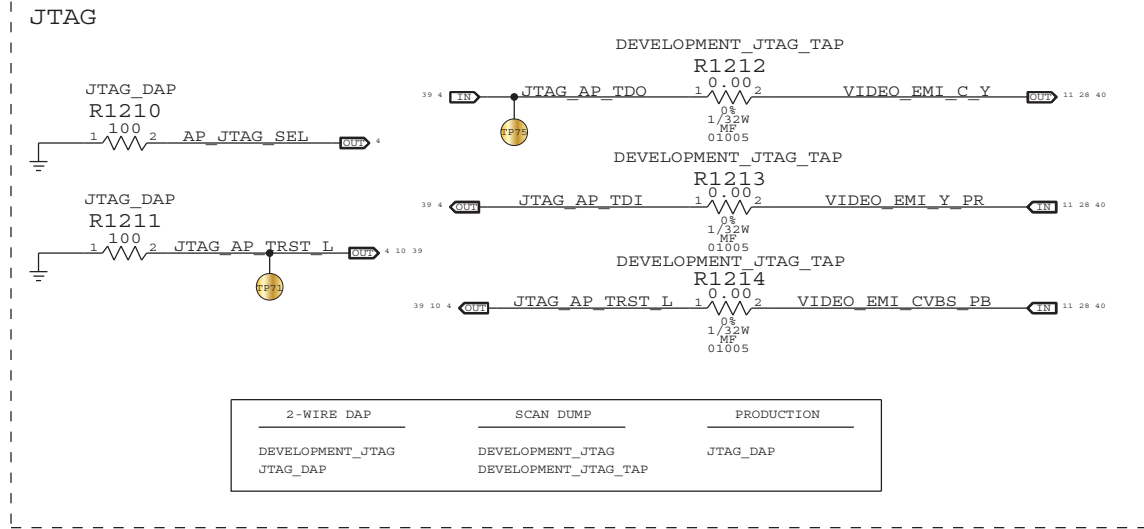
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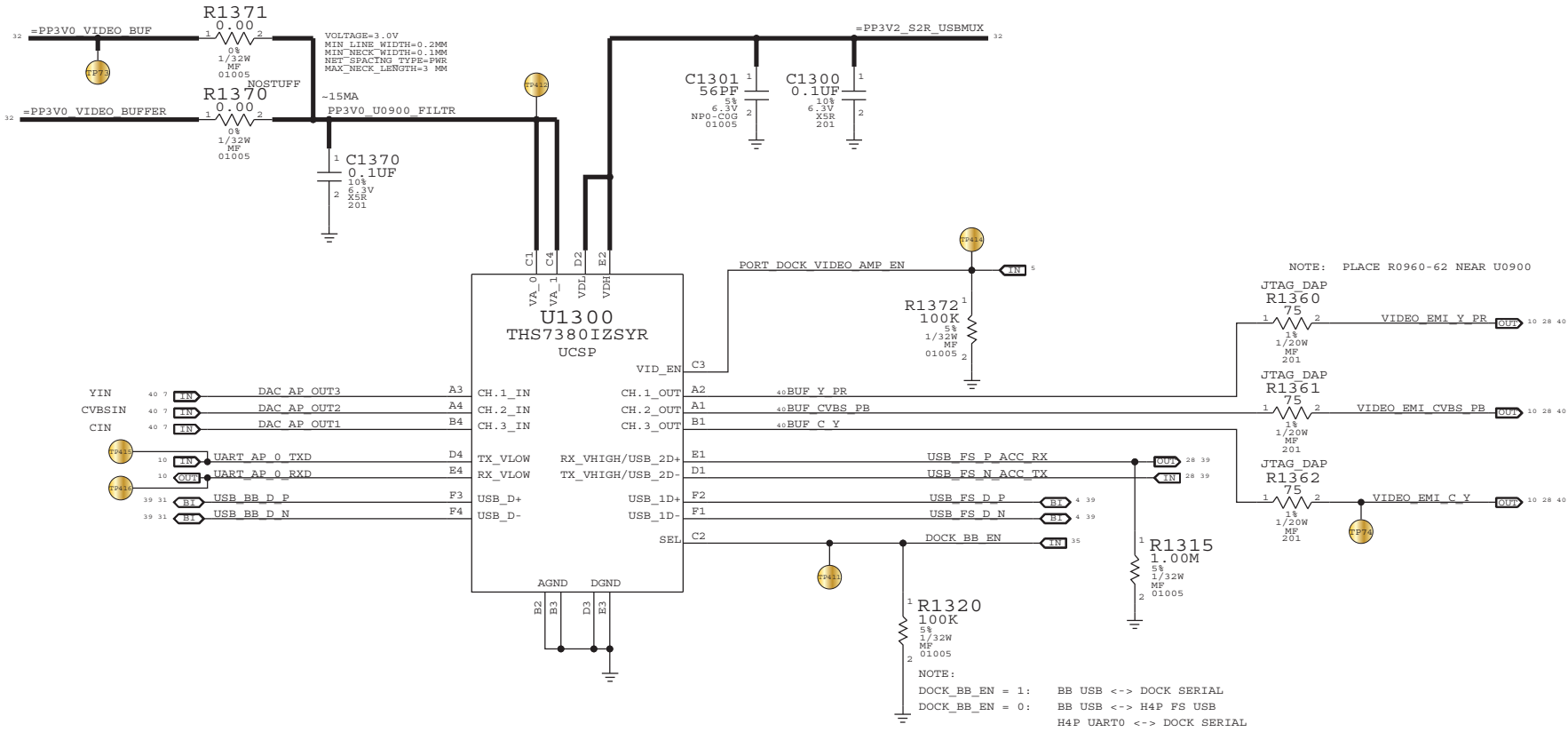
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 0000 SPI0
 0001 SPI3
 0010 SPI0 W/TEST
 0011 SPI3 W/TEST
 0100 FMIO 2CS
 0101 FMIO 4CS
 0110 FMIO 4CS W/TEST
 0111 RESERVED
 1000 FMII 2 CS
 1001 FMII 4 CS
 1010 FMII 4CS W/TEST
 1011 RESERVED
 1100 FMIO/1 2/2 CS
 1101 FMIO/1 4/4 CS
 1110 FMIO/1 4/4 CS W/TEST
 1111 RESERVED

CURRENT SETTING ->
 1100 FMIO/1 2/2 CS
 1101 FMIO/1 4/4 CS
 1110 FMIO/1 4/4 CS W/TEST
 1111 RESERVED



SYNC MASTER=JAMES		SYNC DATE=N/A	
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BRANCH		PAGE	SIZE
		12 OF 106	
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10 OF 42			

NOTE:
 LDO3 PROVIDES 50MA TO BOTH H4P AND U1300
 IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370



PAGE TITLE		SYNC MASTER=JAMES		SYNC DATE=N/A	
AP: VIDEO BUFFER, BB USB MUXES					
DRAWING NUMBER		051-8962		SIZE	
REVISION		A.0.0		D	
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PAGE		13 OF 106		SHEET	
PAGE		11 OF 42		SHEET	

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

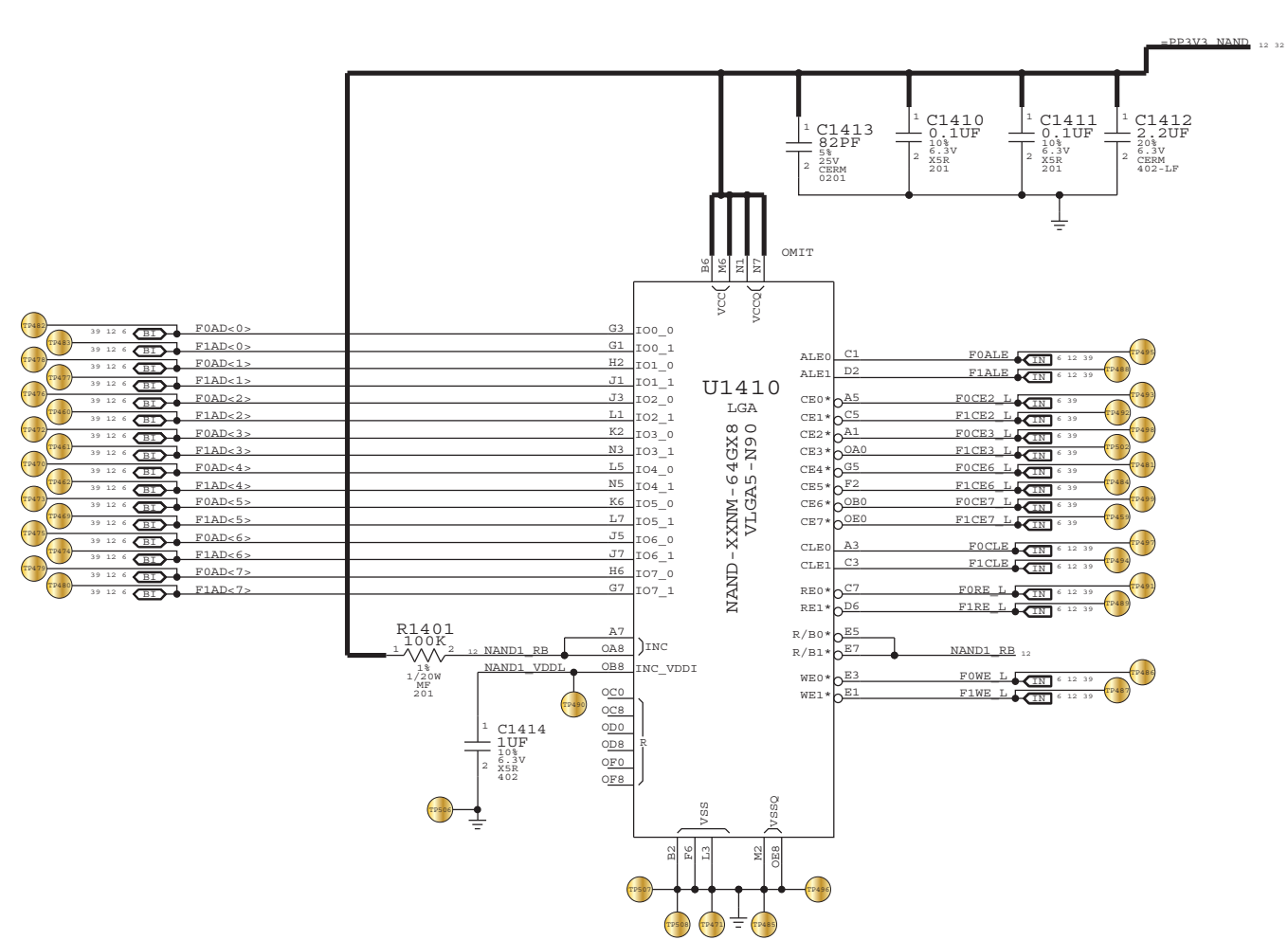
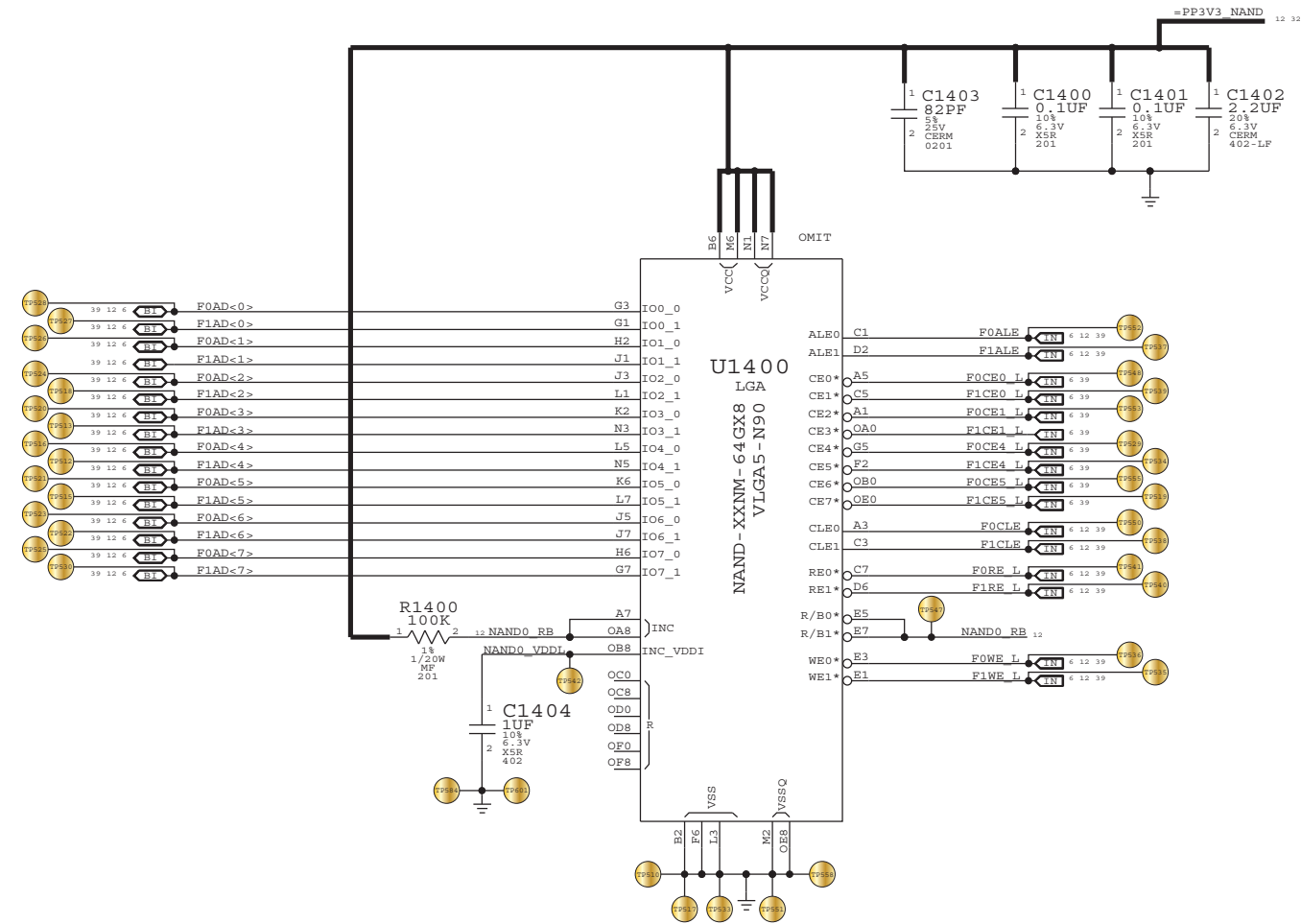
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

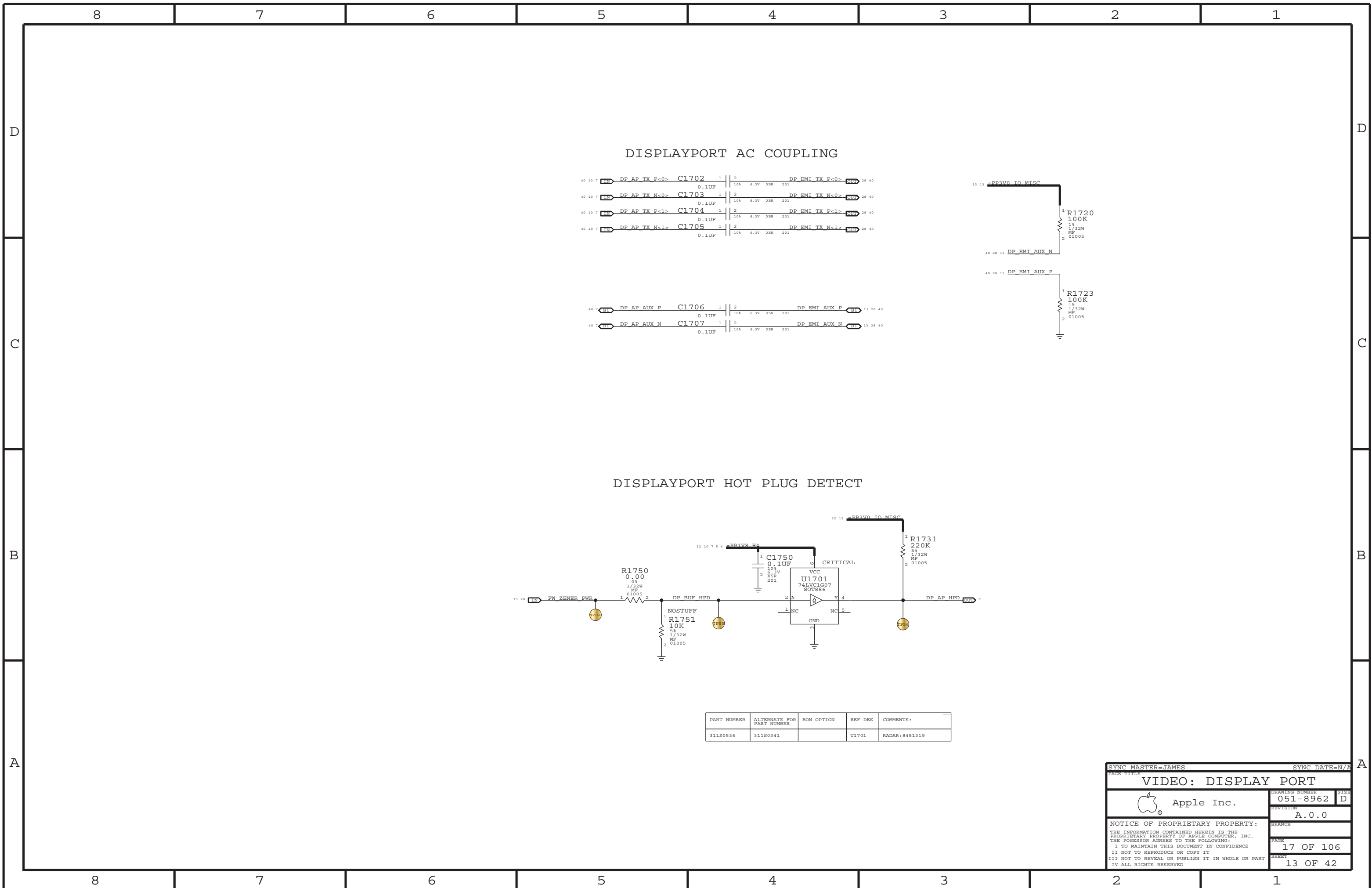
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN

128GB FLASH CONFIGURATIONS



SYNC MASTER=JONATHAN		SYNC DATE=N/A	
NAND			
Apple Inc.		DRAWING NUMBER	SIZE
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC MASTER=JAMES SYNC DATE=N/A

VIDEO: DISPLAY PORT

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

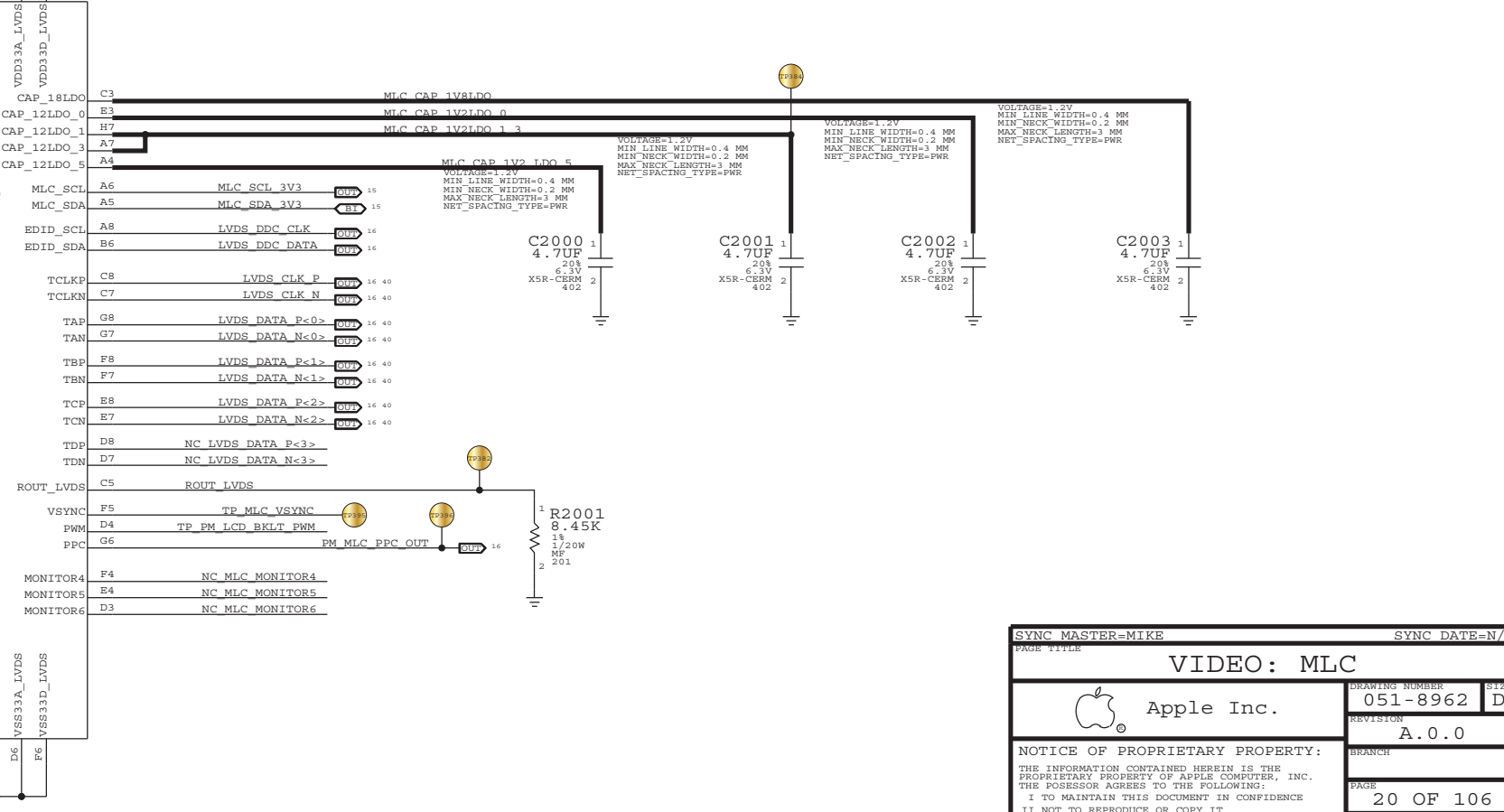
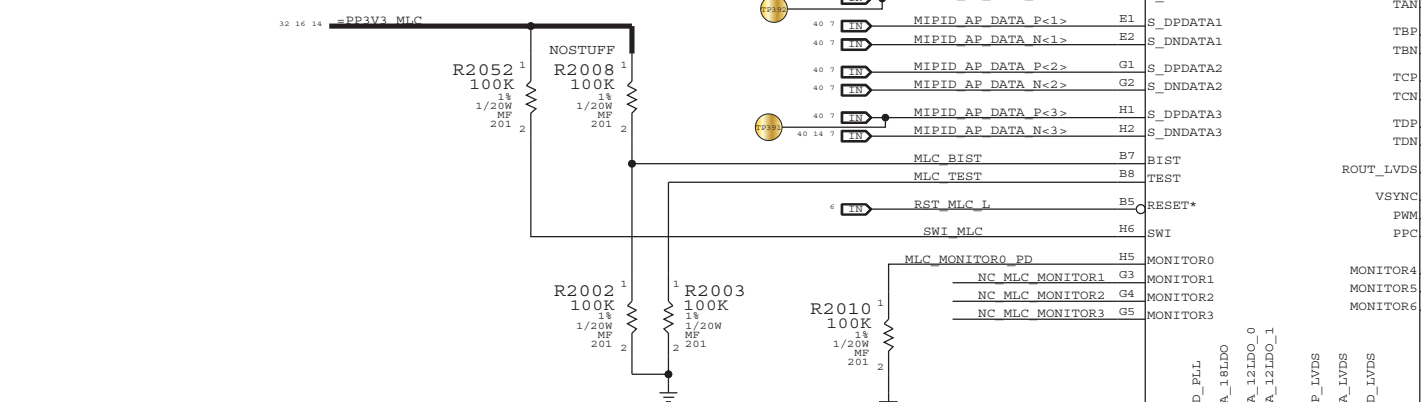
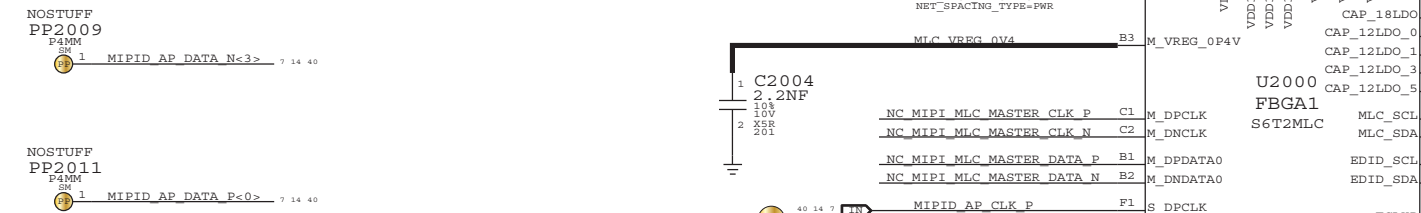
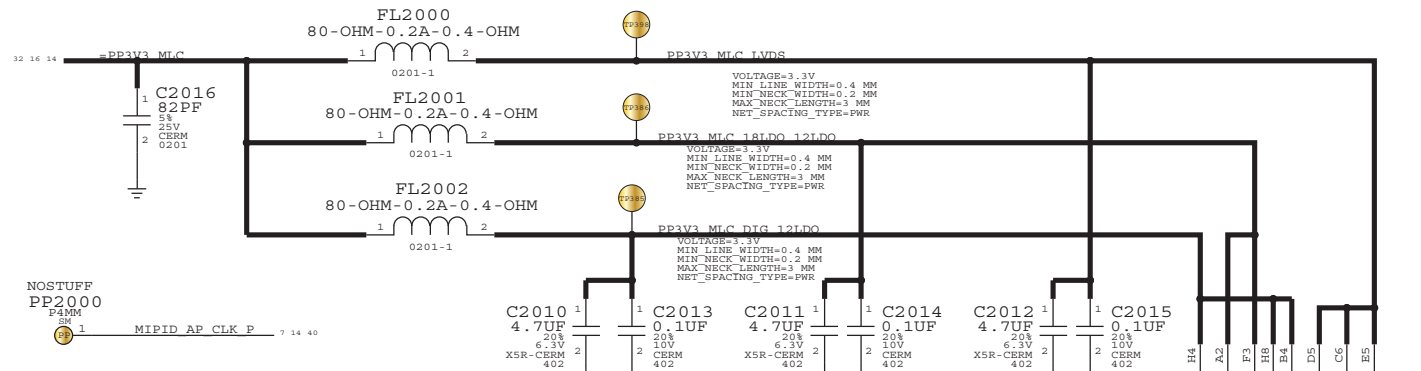
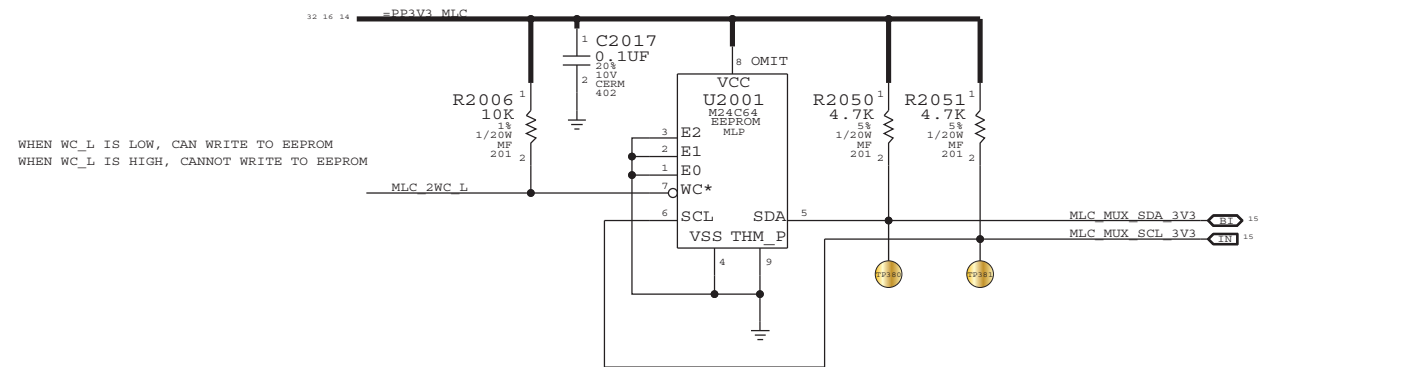
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PAGE: 17 OF 106
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MLC EEPROM:RAW APN 335S0661

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
138S0652	138S0618			RADAR:8377307

SYNC MASTER=MIKE SYNC DATE=N/A

VIDEO: MLC

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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14 MLC_SDA_3V3 == MLC_MUX_SDA_3V3 14
 14 MLC_SCL_3V3 == MLC_MUX_SCL_3V3 14

SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE VIDEO: MLC ALIASES			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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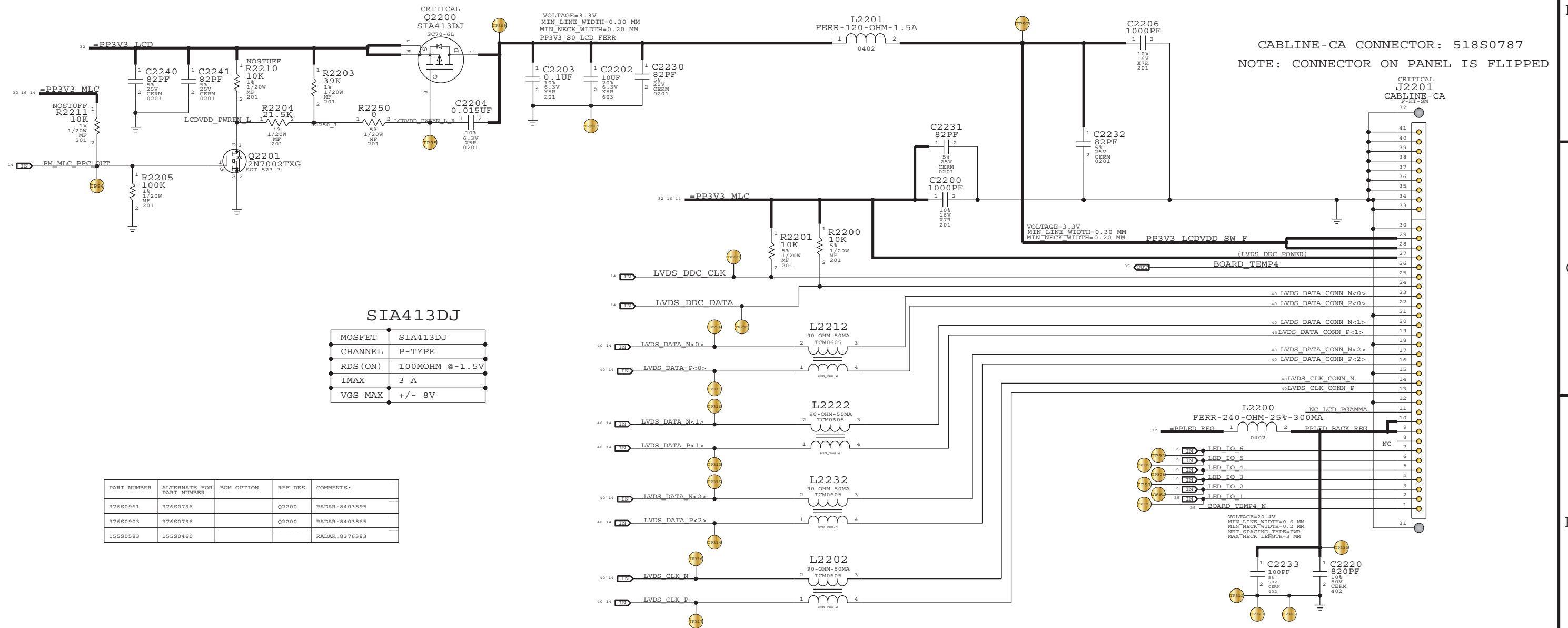
4

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LVDS (LCD) CONNECTOR



SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS (ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

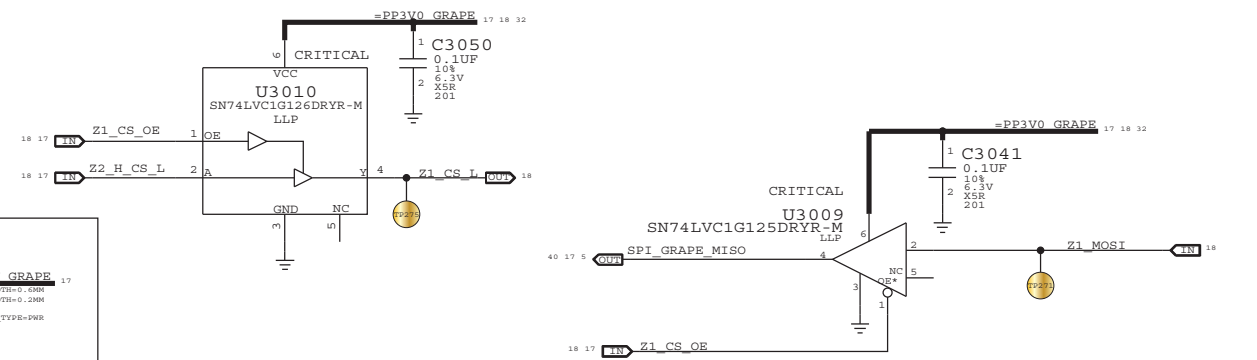
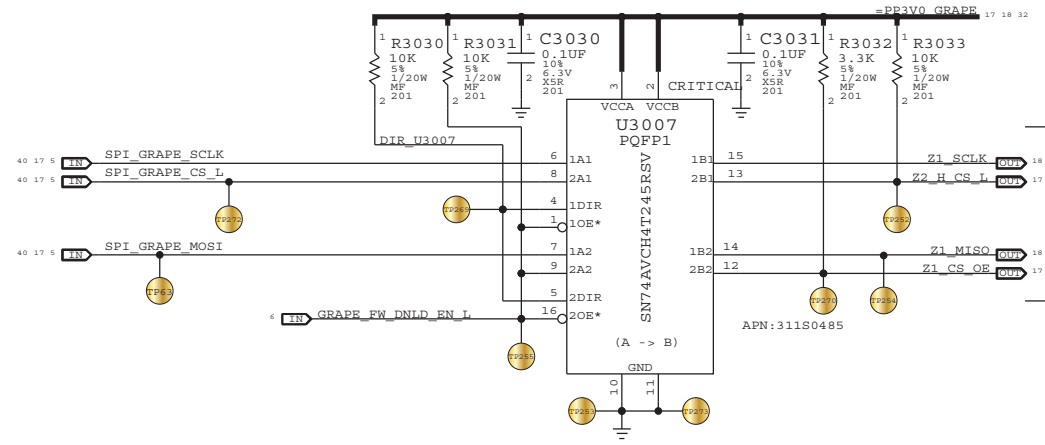
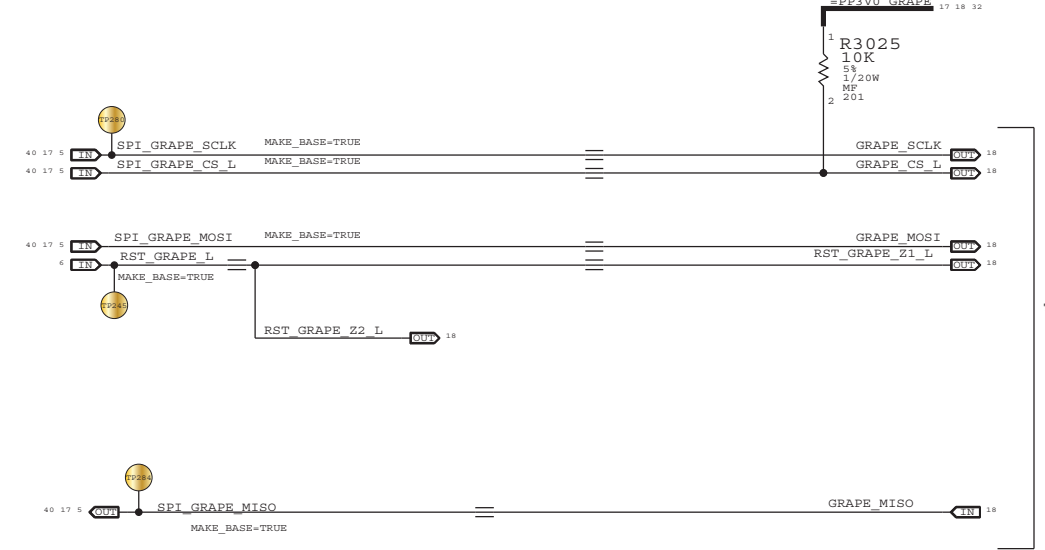
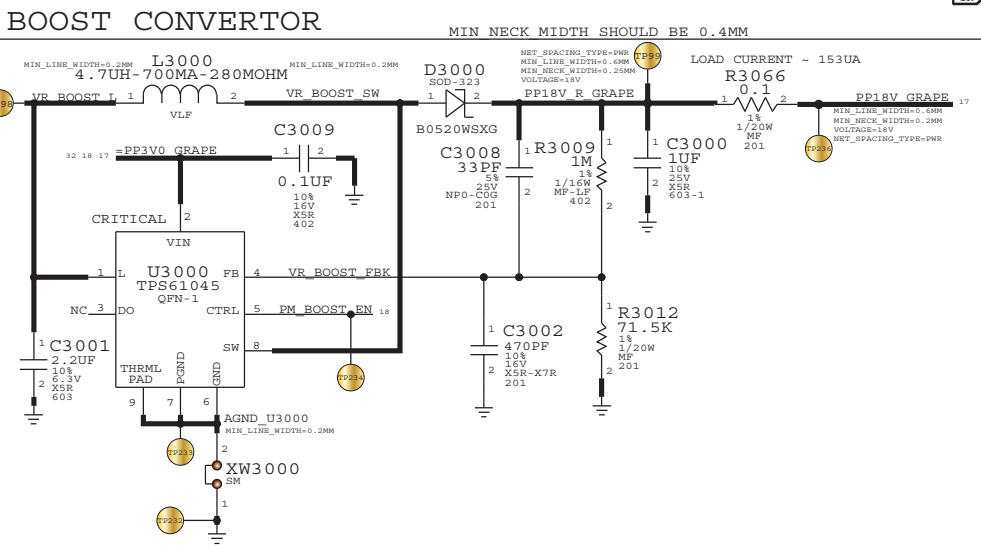
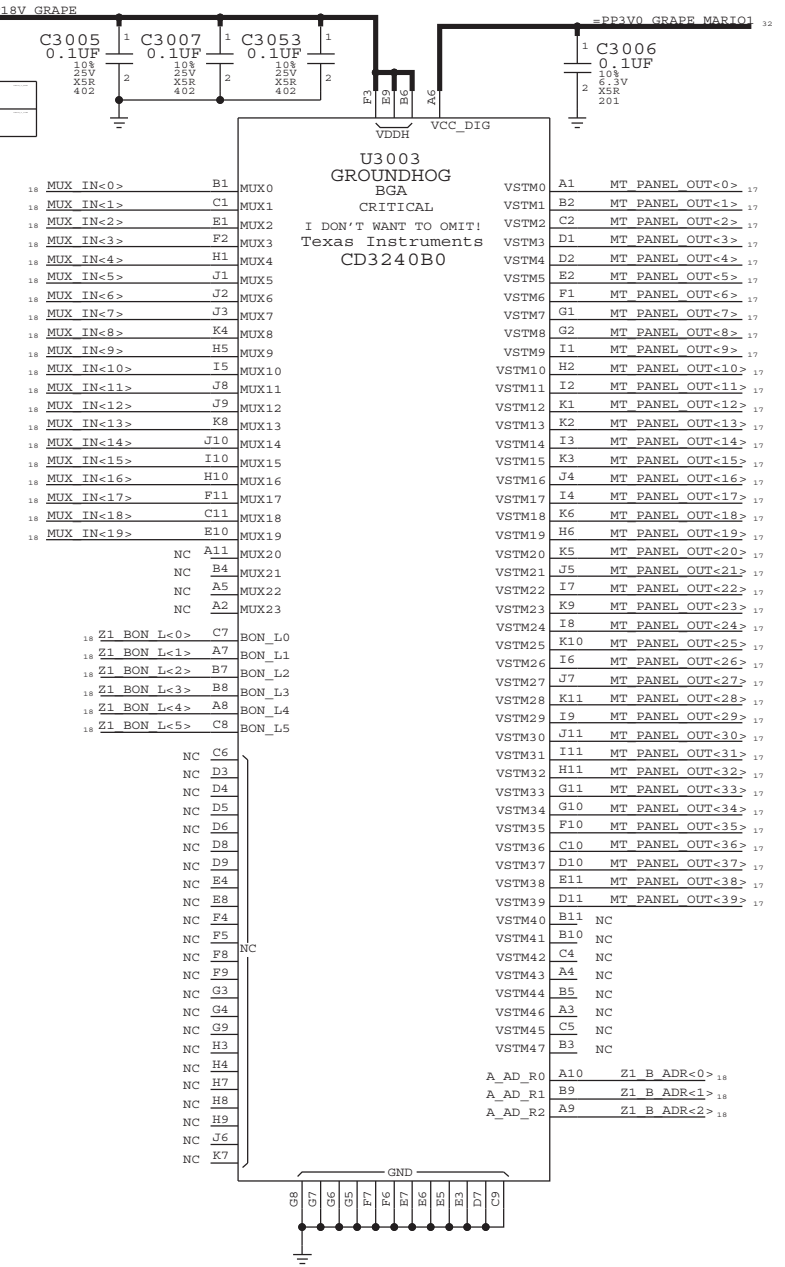
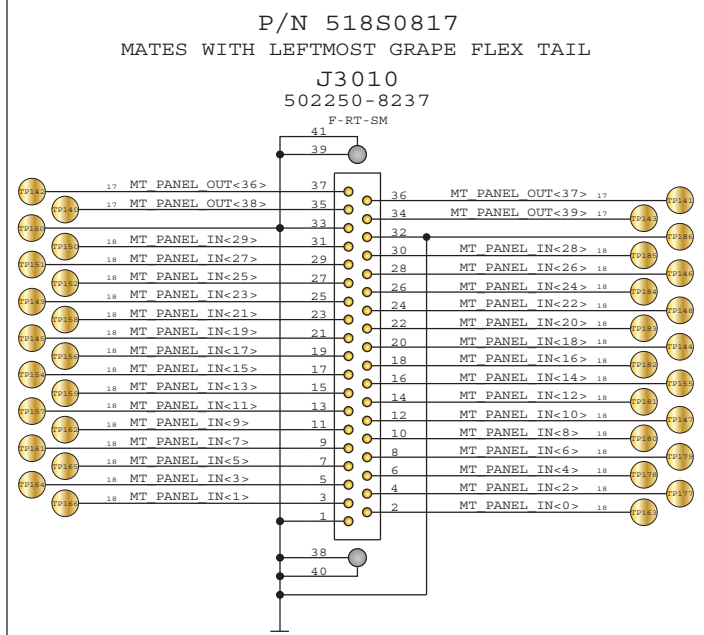
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC MASTER=ALEX		SYNC DATE=N/A	
PAGE TITLE VIDEO: LVDS CONNECTOR			
Apple Inc.		DRAWING NUMBER 051-8962	SIZE D
		REVISION A.0.0	BRANCH
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		PAGE 22 OF 106	SHEET 16 OF 42

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

(TOUCH SCREEN)
CONNECTORS TO GRAPE FLEX



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC MASTER=RAMSN SYNC DATE=N/A

GRAPE: GROUNDHOG, CONN, BOOST

Apple Inc.

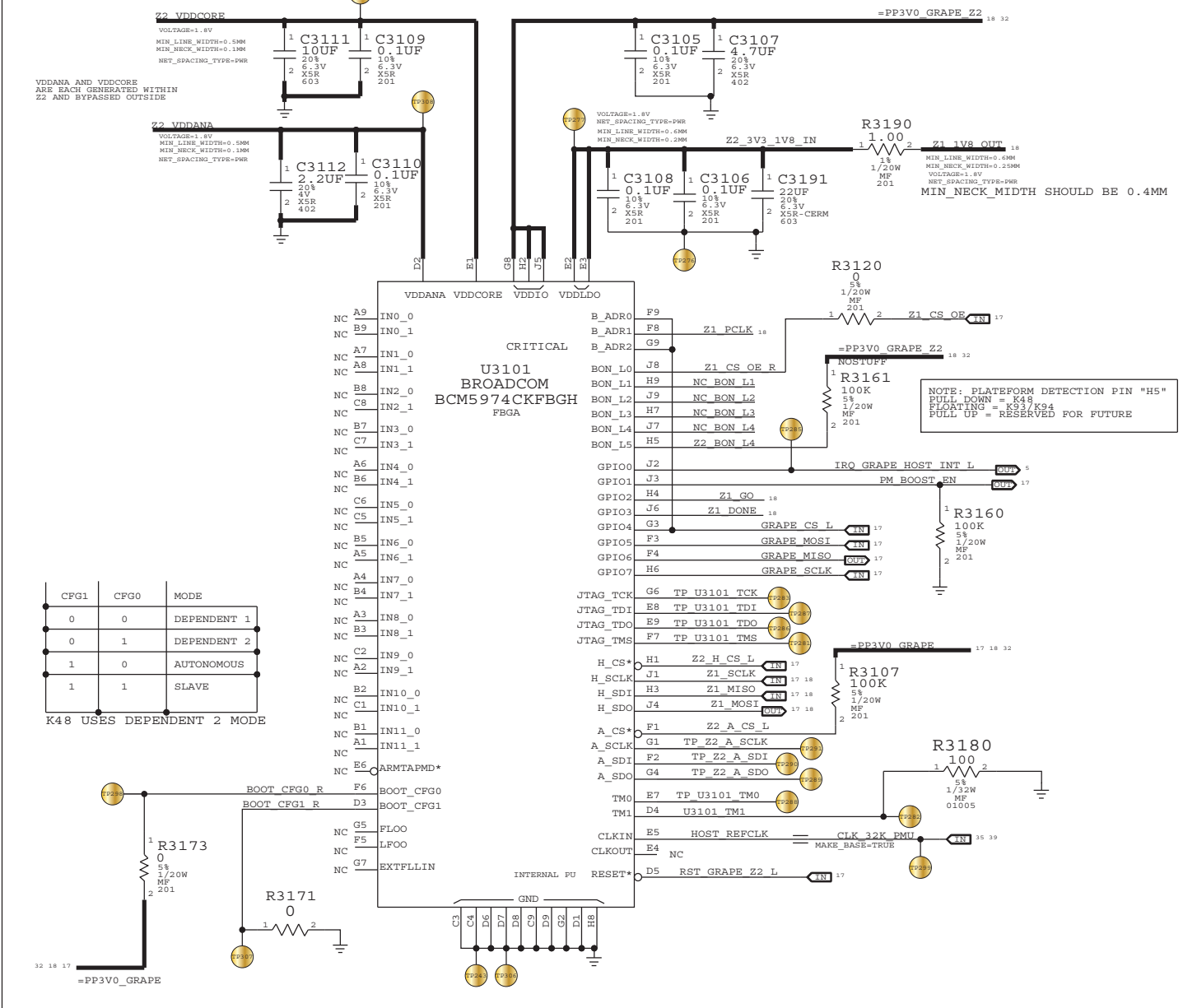
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REVISION: A.0.0

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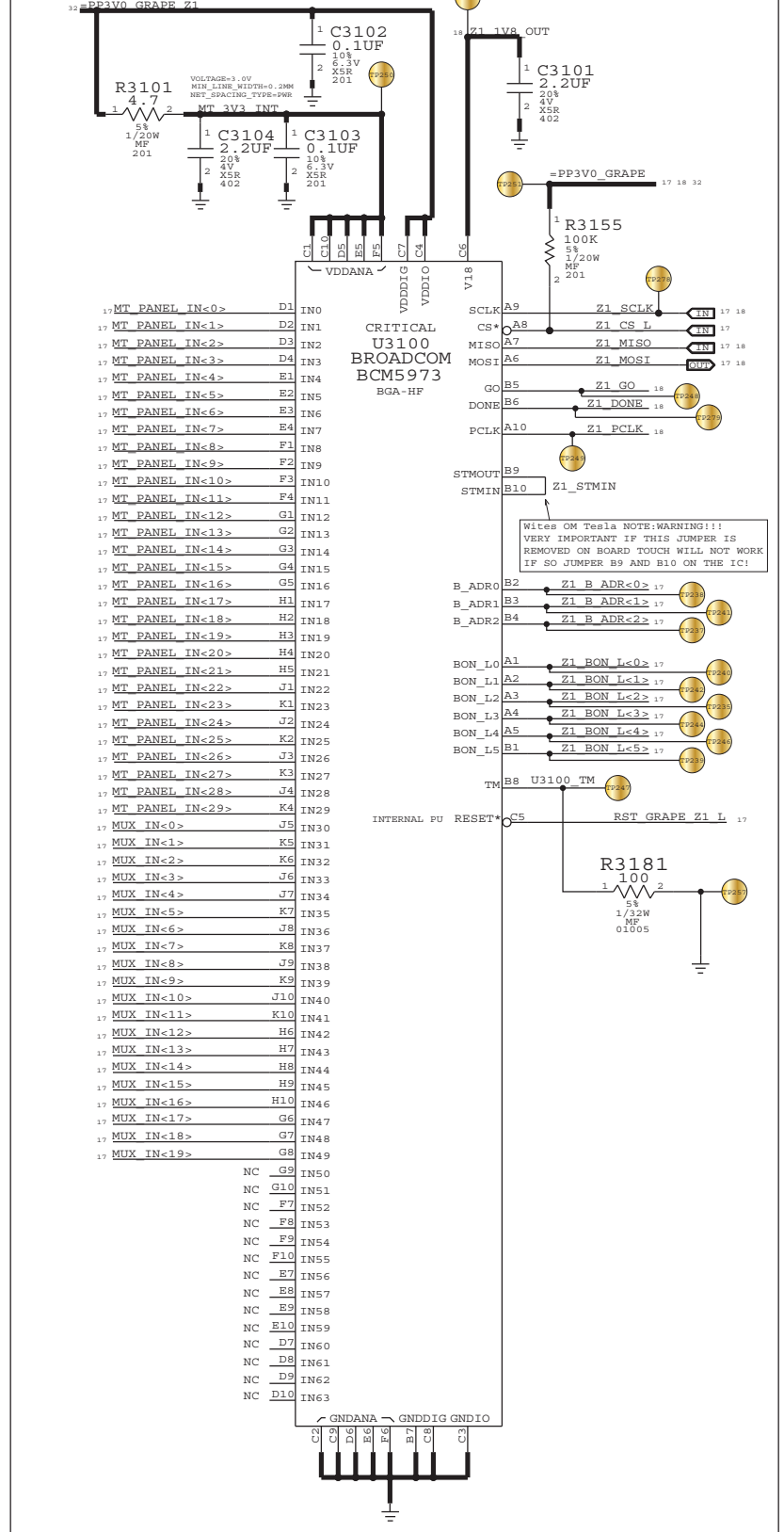
PAGE: 30 OF 106
SHEET: 17 OF 42

ARM9 MCU (Z2 BASED)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR: 8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

ZEPHYR 1+ ASIC



SYNC MASTER=RAMSIN SYNC DATE=N/A

GRAPE: Z1, Z2

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051-8962 D

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L63 AUDIO CODEC

APN:338S0940

8 7 6 5 4 3 2 1

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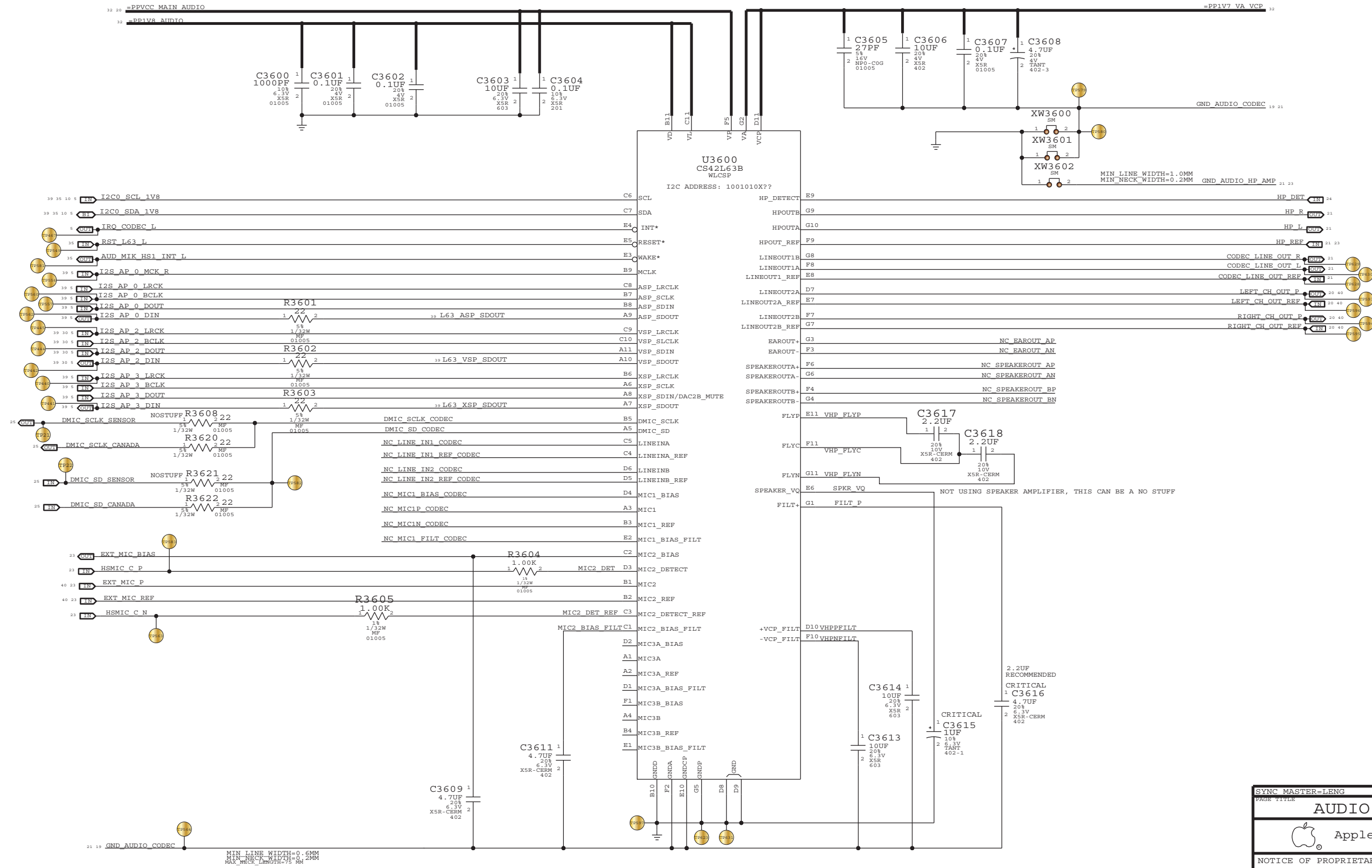
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SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: L63 CODEC			
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		051-8962	D
		REVISION	
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		PAGE	36 OF 106
		SHEET	19 OF 42

8 7 6 5 4 3 2 1

MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.2MM
MAX NECK WIDTH=0.4MM

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SPEAKER AMPLIFIER 1

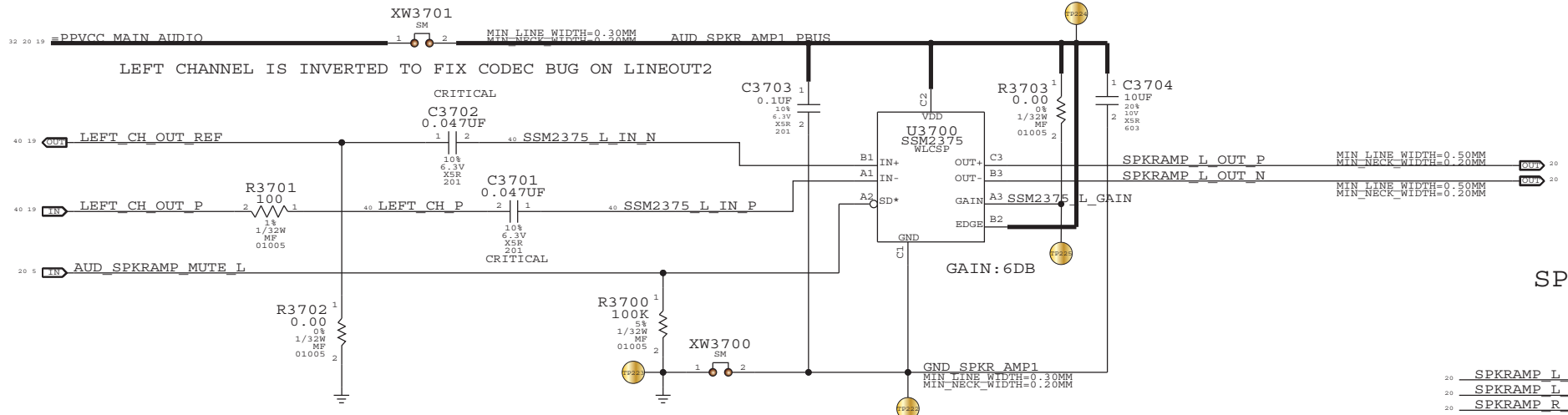
APN:353S2958

TURN ON TIME: 7.5MS

80HZ +/- XXX%

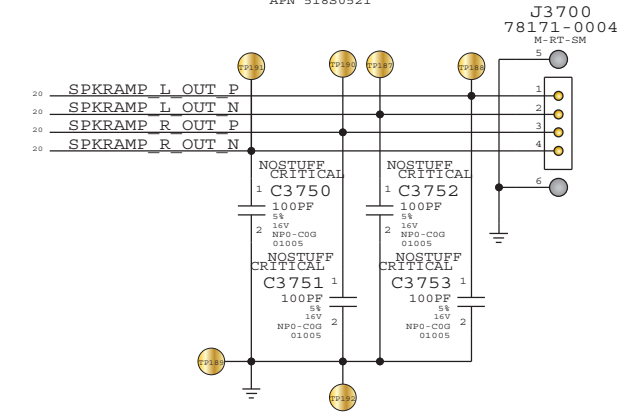
TURN ON DELAY: 20MS

GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT



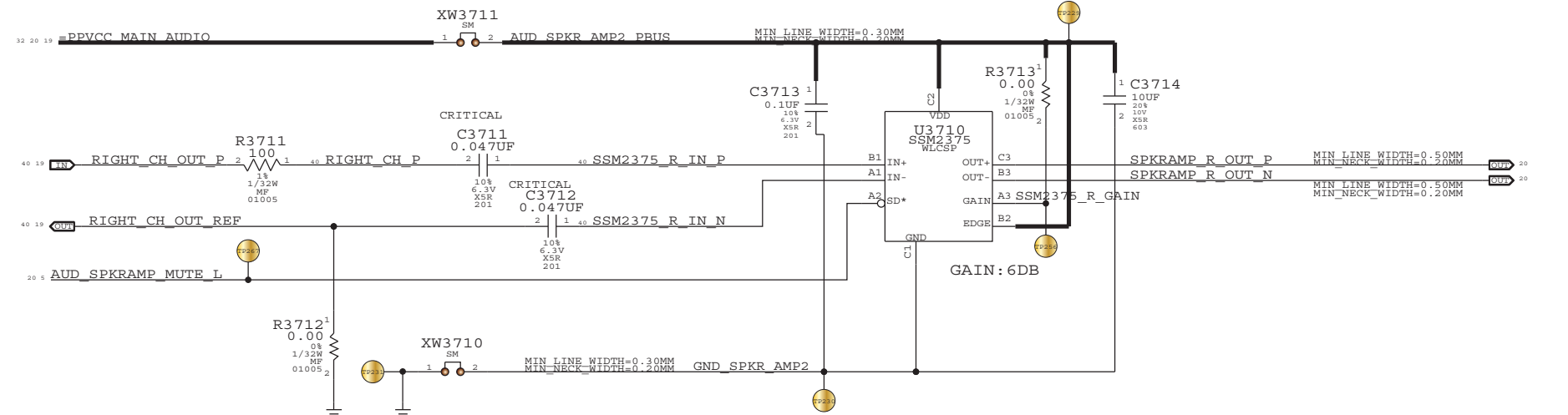
SPEAKER CONNECTOR

APN 518S0521



L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710

SPEAKER AMPLIFIER 2



B

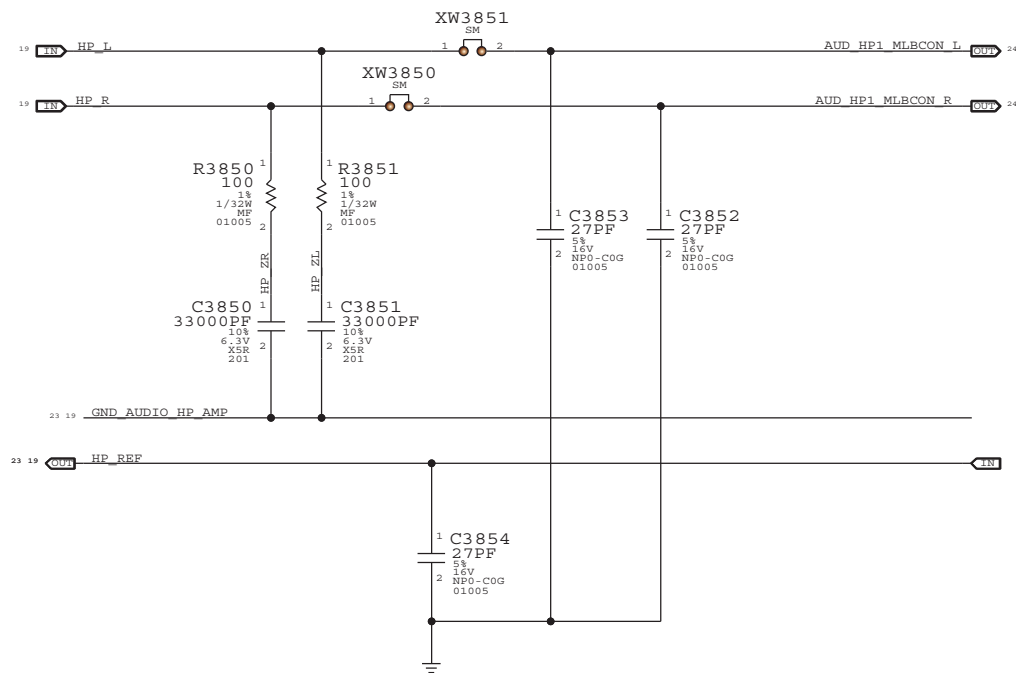
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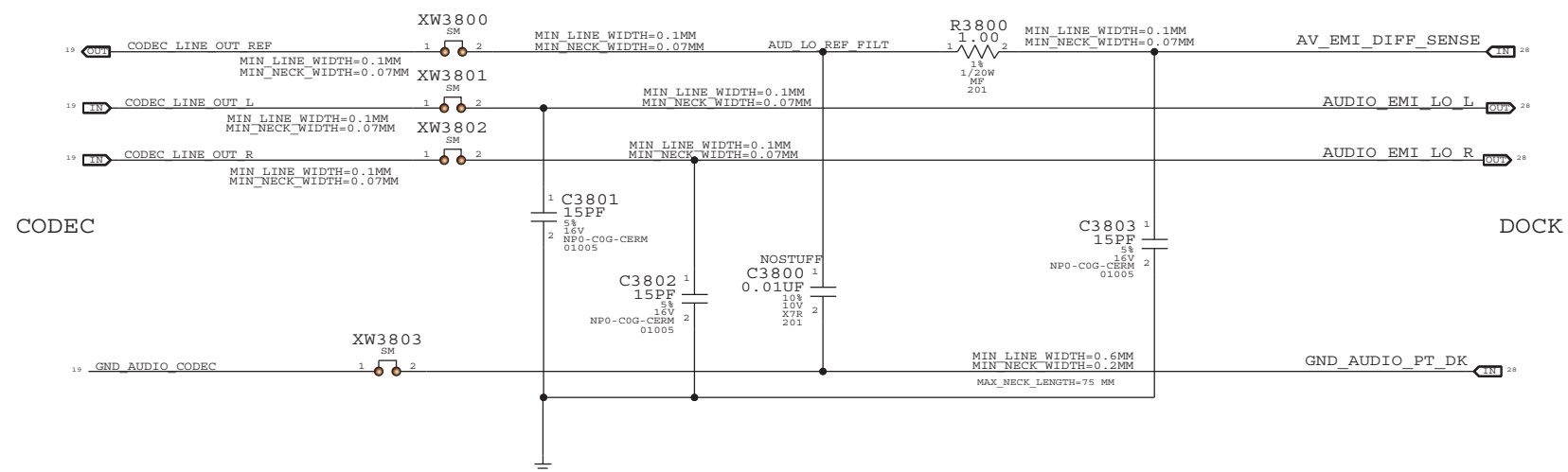
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SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE AUDIO: SPEAKER AMP			
DRAWING NUMBER 051-8962		SIZE D	
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PAGE 37 OF 106		SHEET 20 OF 42	

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE AUDIO: HEADPHONE OUT			
DRAWING NUMBER 051-8962		SIZE D	
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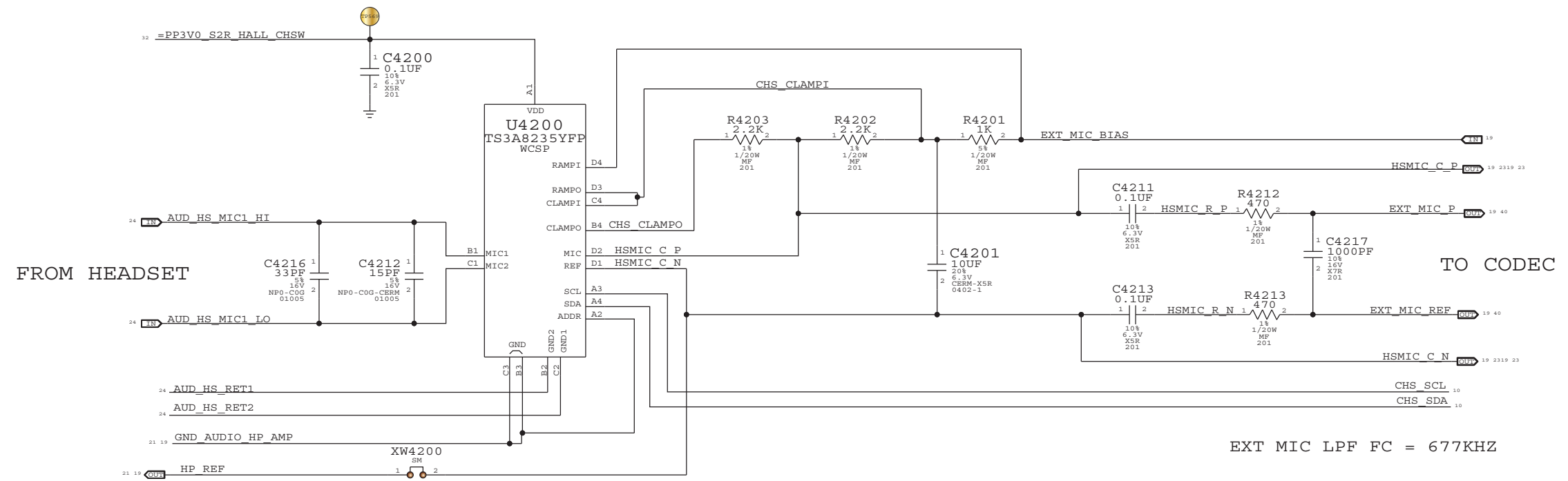
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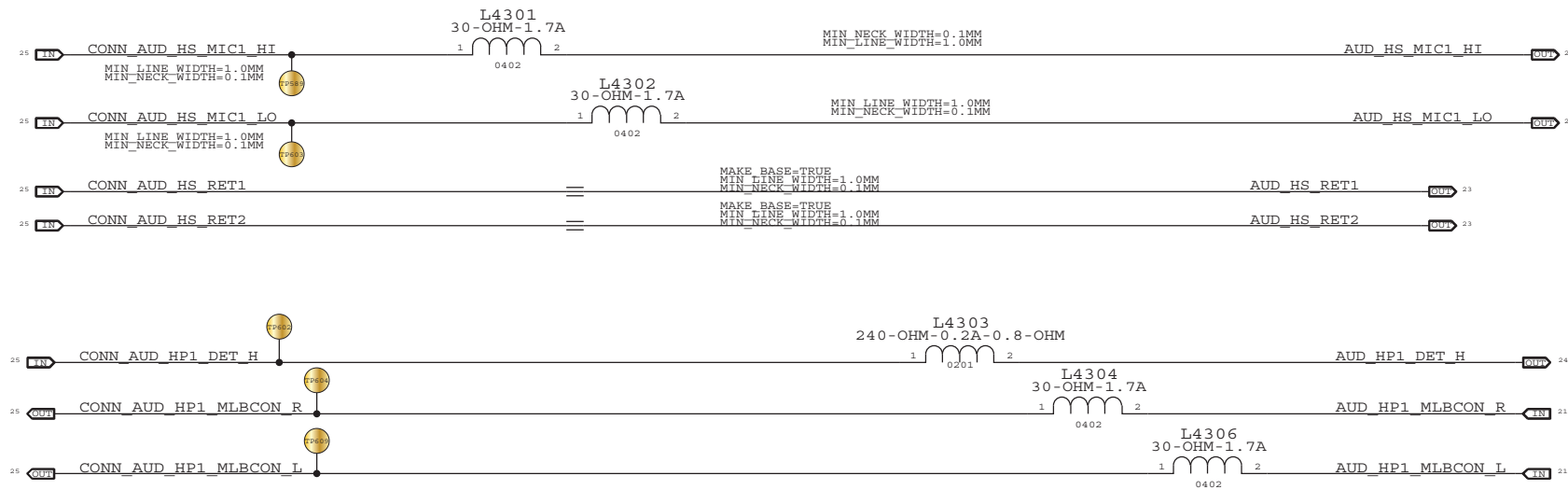
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



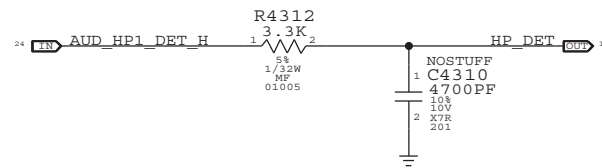
EXT MIC LPF FC = 677KHZ

SYNC MASTER=LENG		SYNC DATE=N/A	
PAGE TITLE AUDIO: DETECT/MIC BIAS			
DRAWING NUMBER 051-8962		SIZE D	
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HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
 PLACE ALL COMPONENTS NEAR J5501



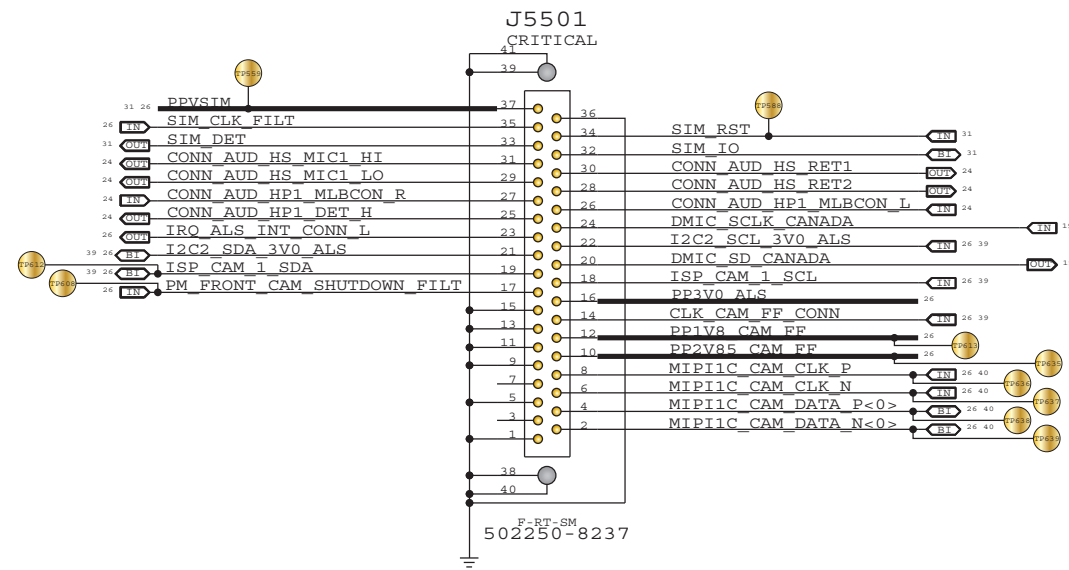
HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG		SYNC DATE=N/A	
AUDIO: HP/MIC FILTERS			
DRAWING NUMBER		SIZE	
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REVISION		BRANCH	
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CANADA FLEXES CONN.

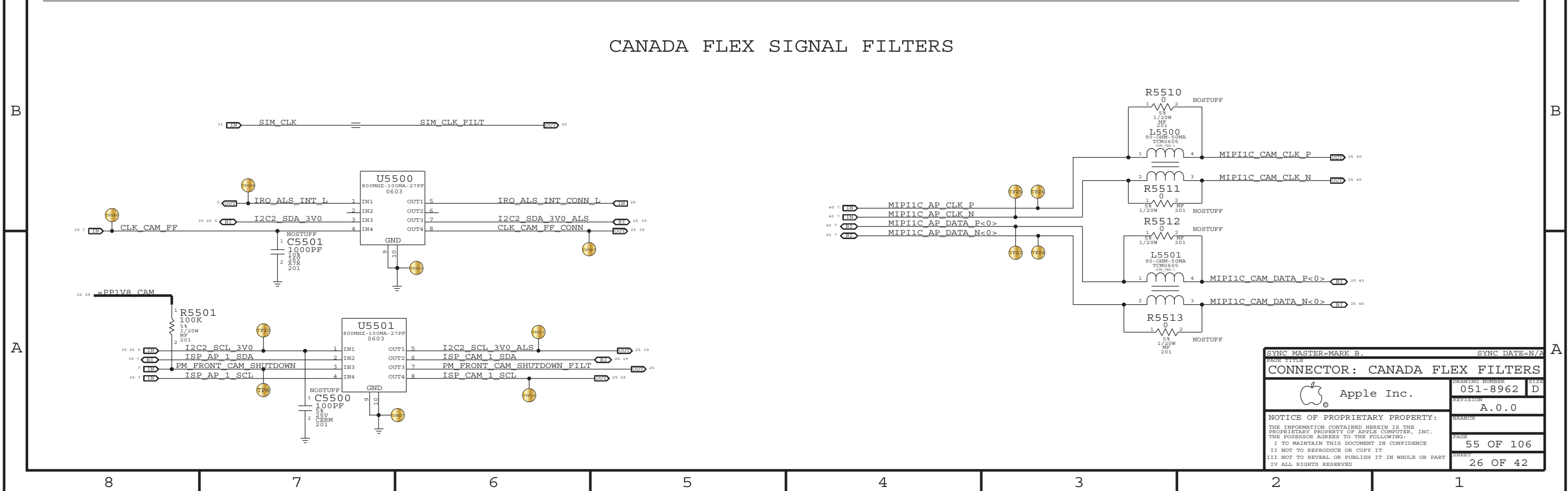
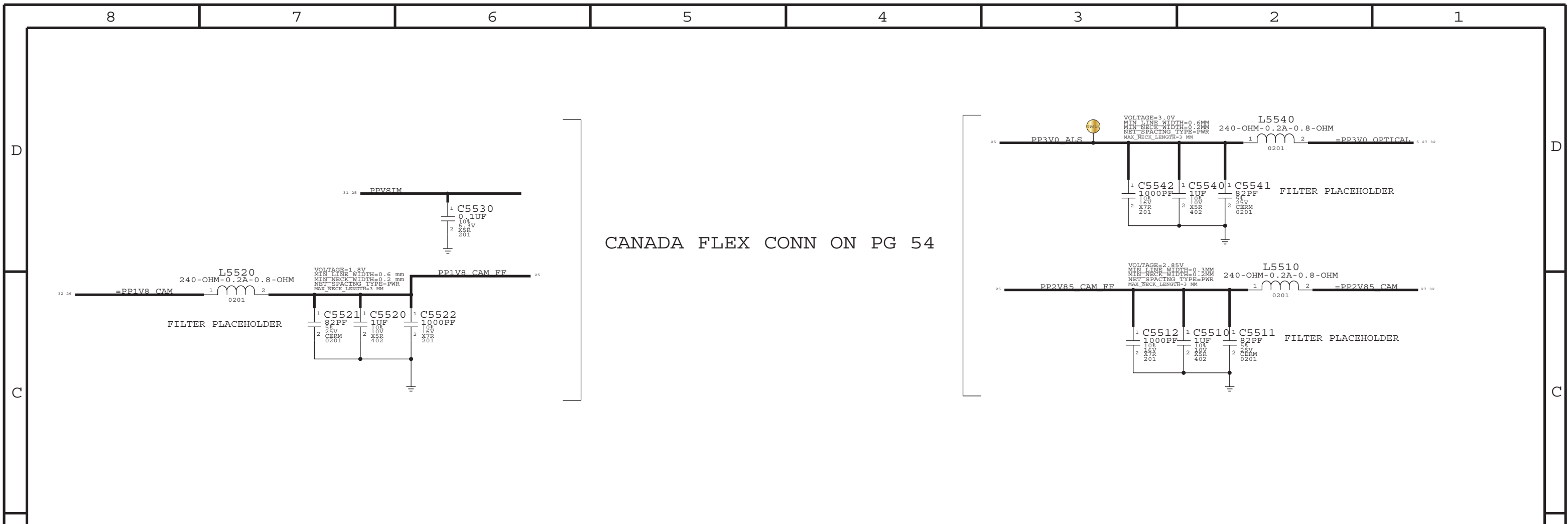
APN: 518S0817



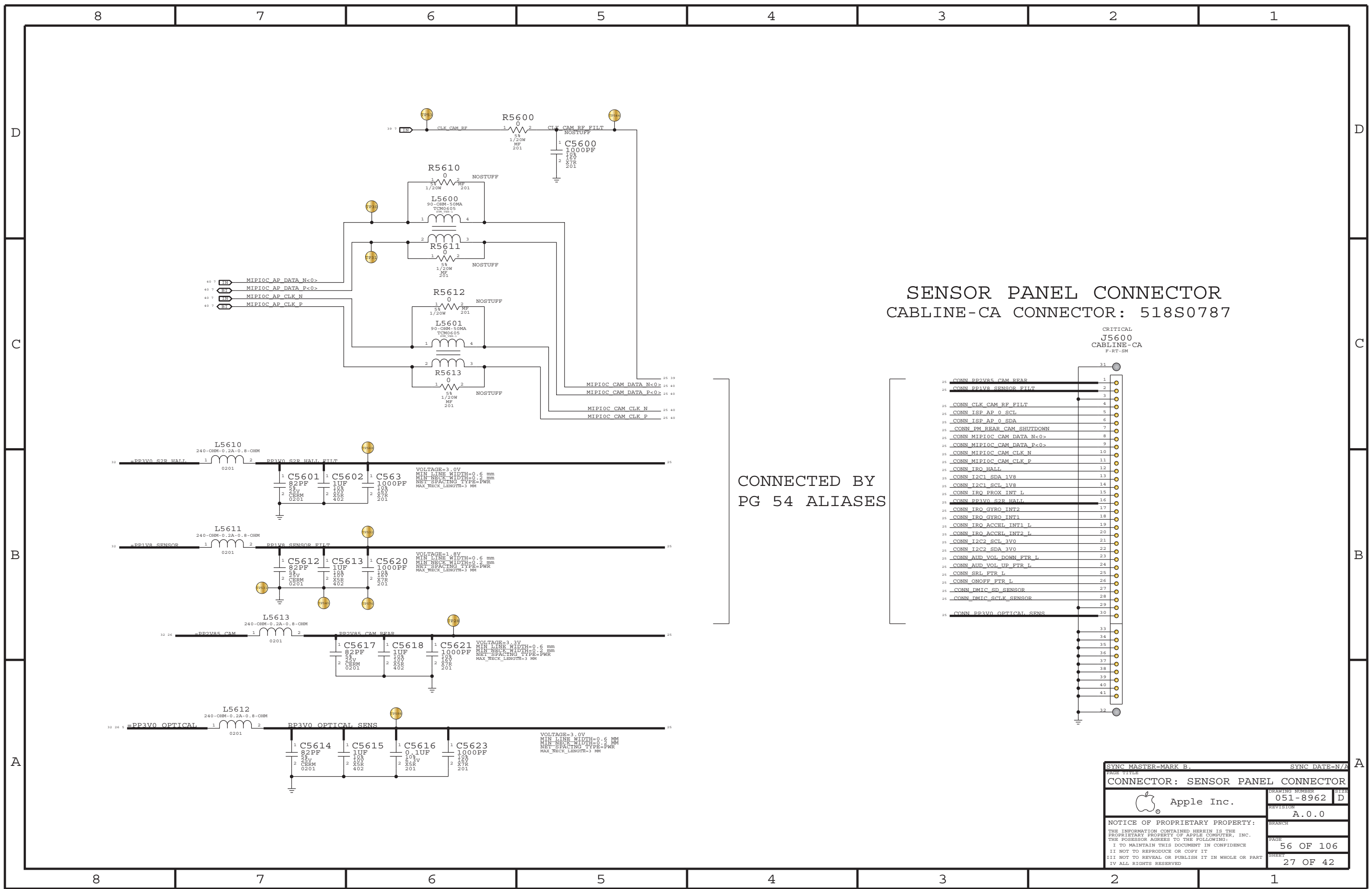
SENSOR BOARD CONN ALIASES

39	CLK CAM RF FILT	==	CONN CLK CAM RF FILT	27
40	MIIPIOC CAM DATA N<0>	MAKE_BASE+TRIG	CONN MIIPIOC CAM DATA N<0>	27
40	MIIPIOC CAM DATA P<0>	MAKE_BASE+TRIG	CONN MIIPIOC CAM DATA P<0>	27
40	MIIPIOC CAM CLK N	MAKE_BASE+TRIG	CONN MIIPIOC CAM CLK N	27
40	MIIPIOC CAM CLK P	MAKE_BASE+TRIG	CONN MIIPIOC CAM CLK P	27
7	PM REAR CAM SHUTDOWN	MAKE_BASE+TRIG	CONN PM REAR CAM SHUTDOWN	27
27	PP1V8 SENSOR FILT	MAKE_BASE+TRIG	CONN PP1V8 SENSOR FILT	27
27	PP2V85 CAM REAR	MAKE_BASE+TRIG	CONN PP2V85 CAM REAR	27
19	DMIC_SD SENSOR	MAKE_BASE+TRIG	CONN DMIC_SD SENSOR	27
19	DMIC_SCLK SENSOR	MAKE_BASE+TRIG	CONN DMIC_SCLK SENSOR	27
19	ISP AP 0_SCL	MAKE_BASE+TRIG	CONN ISP AP 0_SCL	27
19	ISP AP 0_SDA	MAKE_BASE+TRIG	CONN ISP AP 0_SDA	27
19	I2C2_SCL_3V0	MAKE_BASE+TRIG	CONN I2C2_SCL_3V0	27
19	I2C2_SDA_3V0	MAKE_BASE+TRIG	CONN I2C2_SDA_3V0	27
5	IRO ACCEL INT1 L	MAKE_BASE+TRIG	CONN IRO ACCEL INT1 L	27
5	IRO ACCEL INT2 L	MAKE_BASE+TRIG	CONN IRO ACCEL INT2 L	27
5	IRO GYRO INT1	MAKE_BASE+TRIG	CONN IRO GYRO INT1	27
5	IRO GYRO INT2	MAKE_BASE+TRIG	CONN IRO GYRO INT2	27
19	I2C1_SCL_1V8	MAKE_BASE+TRIG	CONN I2C1_SCL_1V8	27
19	I2C1_SDA_1V8	MAKE_BASE+TRIG	CONN I2C1_SDA_1V8	27
19	IRO HALL	MAKE_BASE+TRIG	CONN IRO HALL	27
19	IRO PROX INT L	MAKE_BASE+TRIG	CONN IRO PROX INT L	27
27	PP3V0 S2R HALL FILT	MAKE_BASE+TRIG	CONN PP3V0 S2R HALL	27
15	ONOFF L	MAKE_BASE+TRIG	CONN ONOFF FTR L	27
15	SRL L	MAKE_BASE+TRIG	CONN SRL FTR L	27
15	AUD VOL UP L	MAKE_BASE+TRIG	CONN AUD VOL UP FTR L	27
15	AUD VOL DOWN L	MAKE_BASE+TRIG	CONN AUD VOL DOWN FTR L	27
27	PP3V0 OPTICAL SENS	MAKE_BASE+TRIG	CONN PP3V0 OPTICAL SENS	27

SYNC MASTER=MARK B.		SYNC DATE=N/A	
CONNECTOR: CANADA FLEX CONN, SENSOR PANEL ALIASES			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	D
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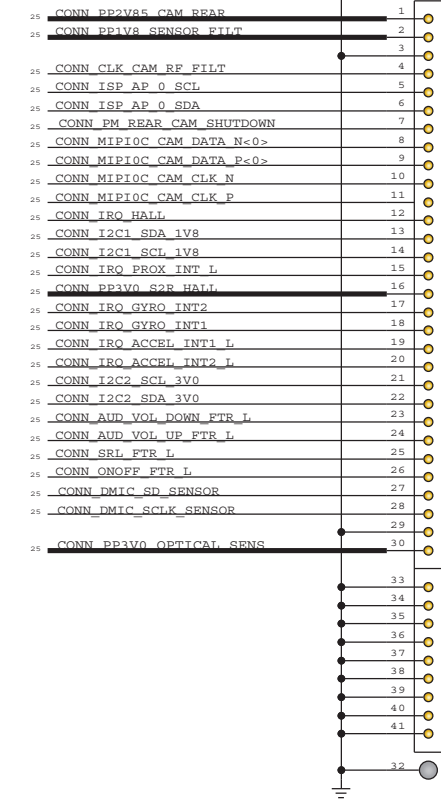
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CONNECTOR: CANADA FLEX FILTERS			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	
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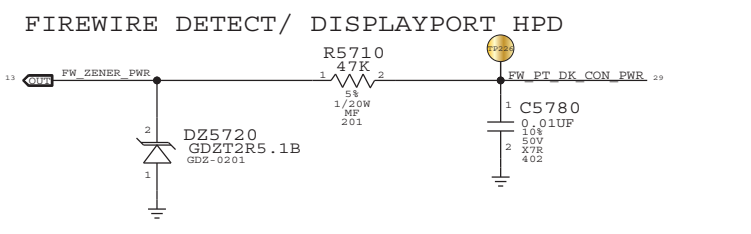
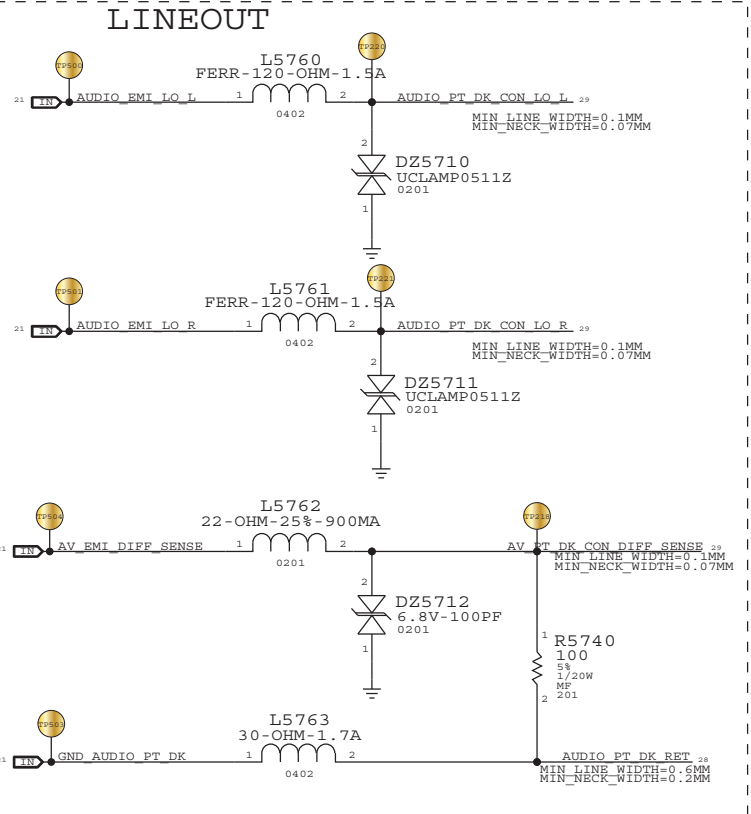
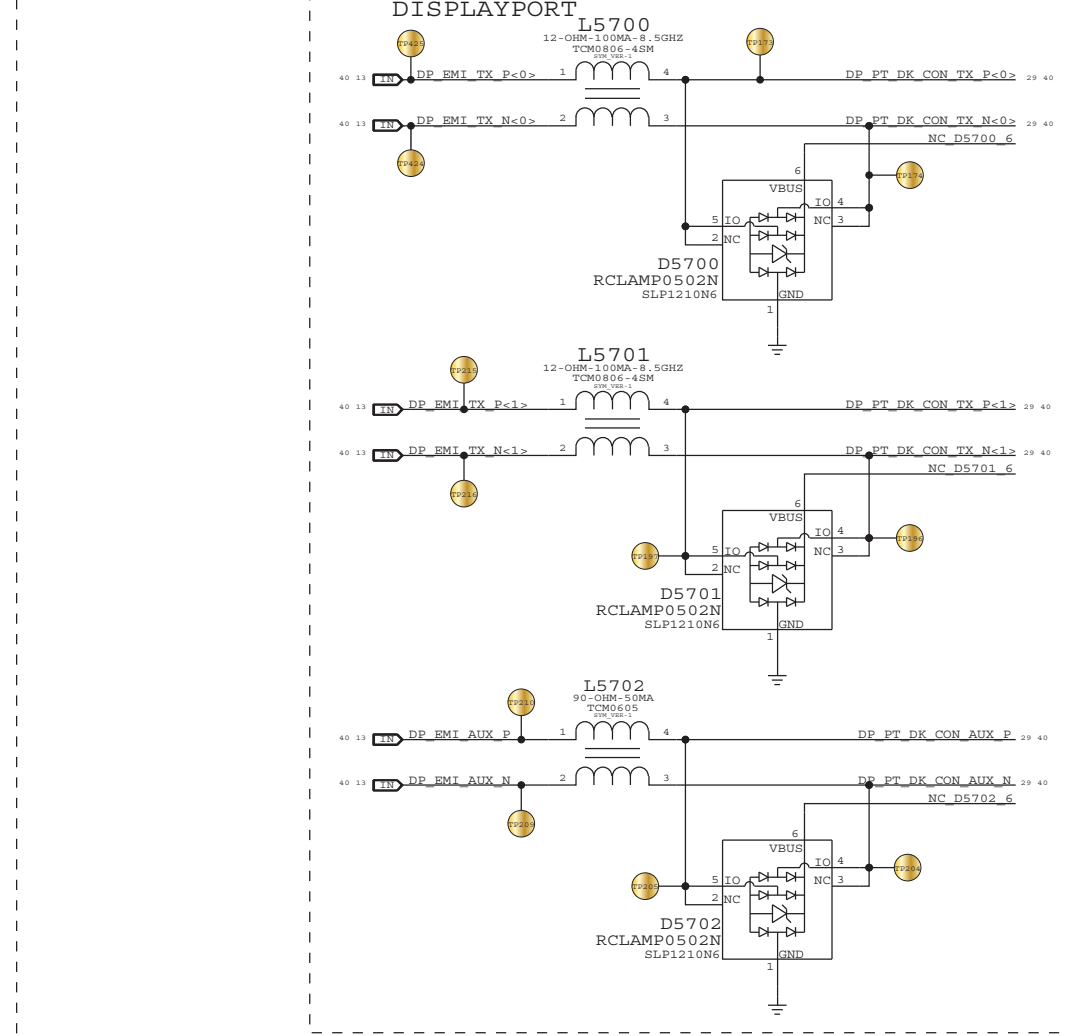
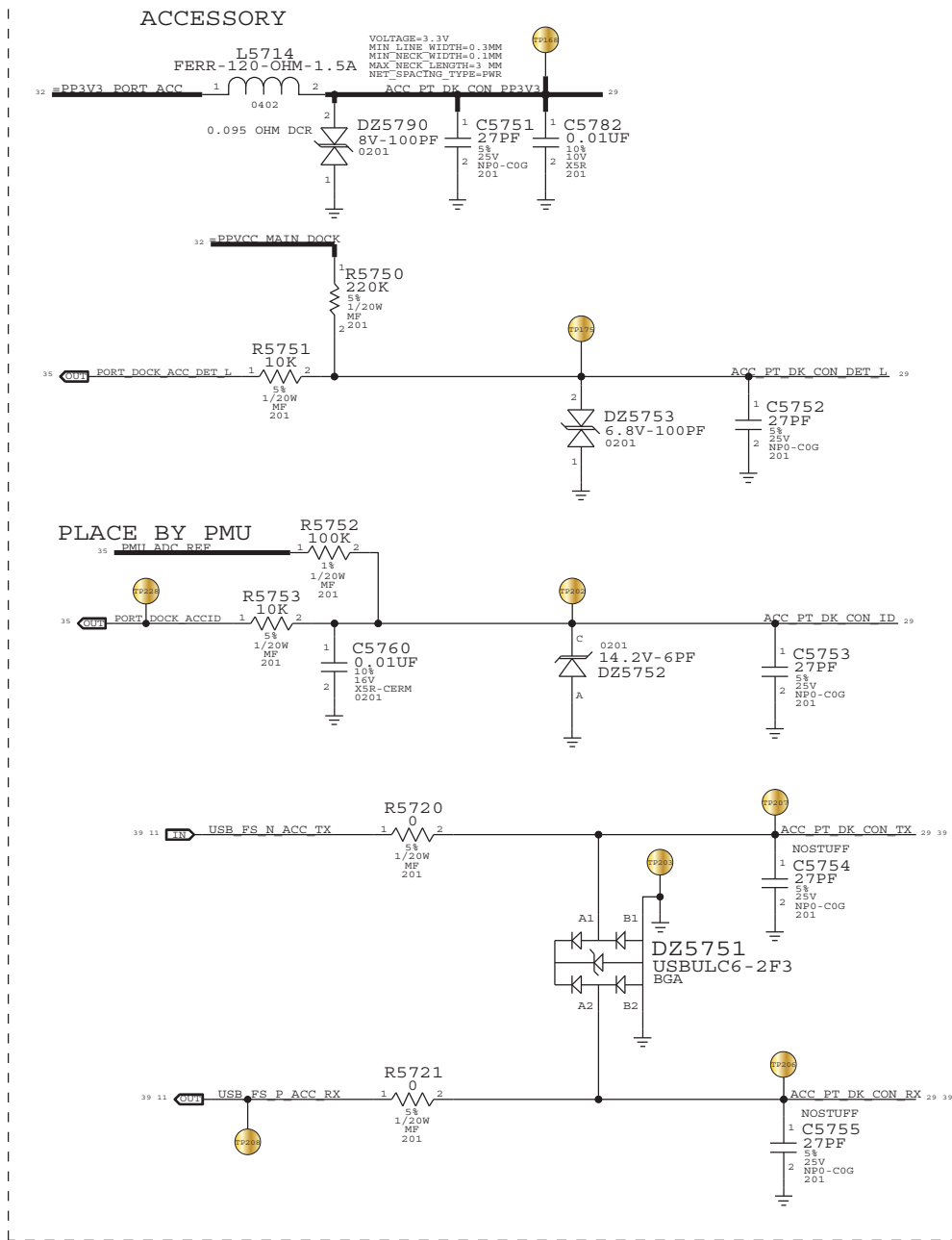
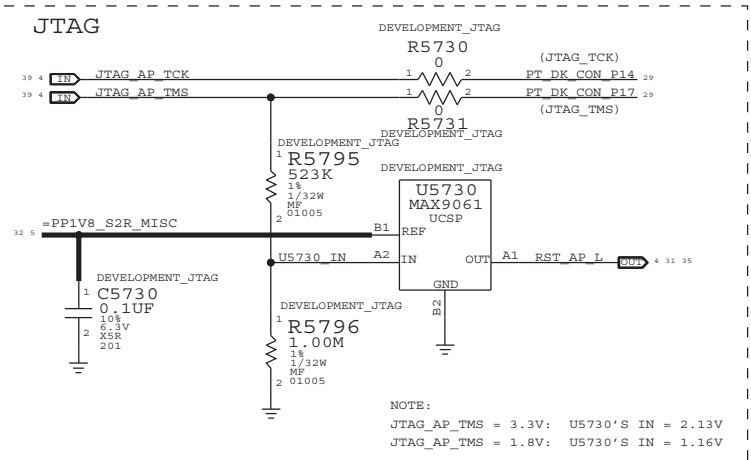
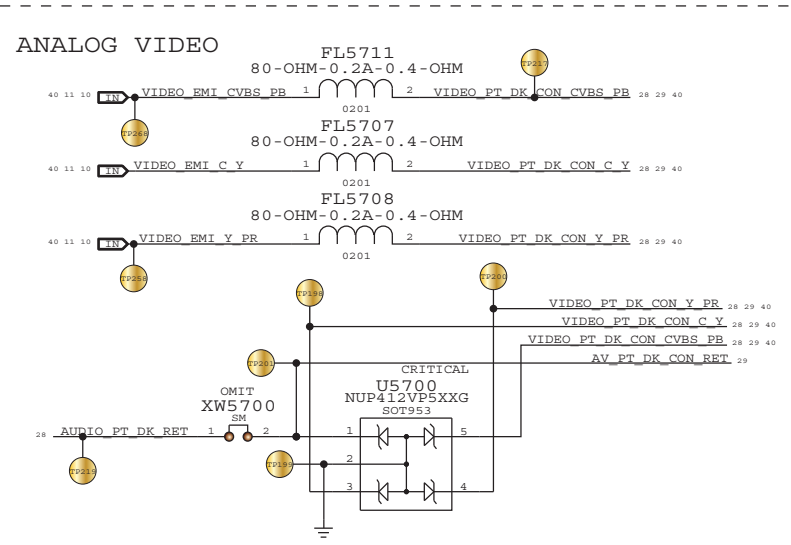
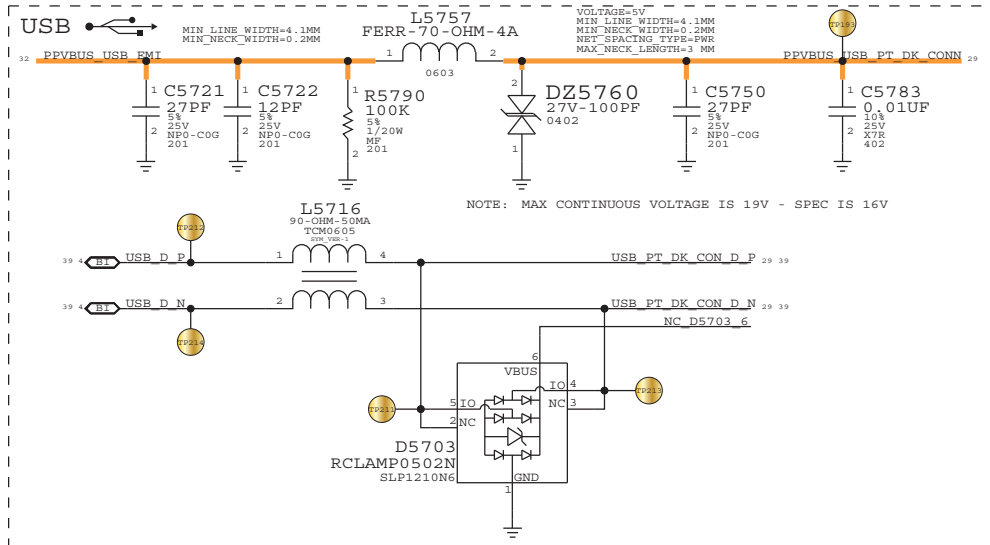
SENSOR PANEL CONNECTOR CABLINE-CA CONNECTOR: 518S0787

CRITICAL
J5600
CABLINE-CA
F-RT-SM

CONNECTED BY
PG 54 ALIASES



PAGE TITLE		SYNC DATE=N/A	
CONNECTOR: SENSOR PANEL CONNECTOR			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DBY10, DBY11	RADAR: 8379541
377S0107	377S0066		DBY10, DBY11	RADAR: 8289785
155S0625	155S0559		L5700, L5702	RADAR: 8423156

SYNC MASTER=JAMES SYNC DATE=N/A

IO FLEX: DOCK COMPONENTS

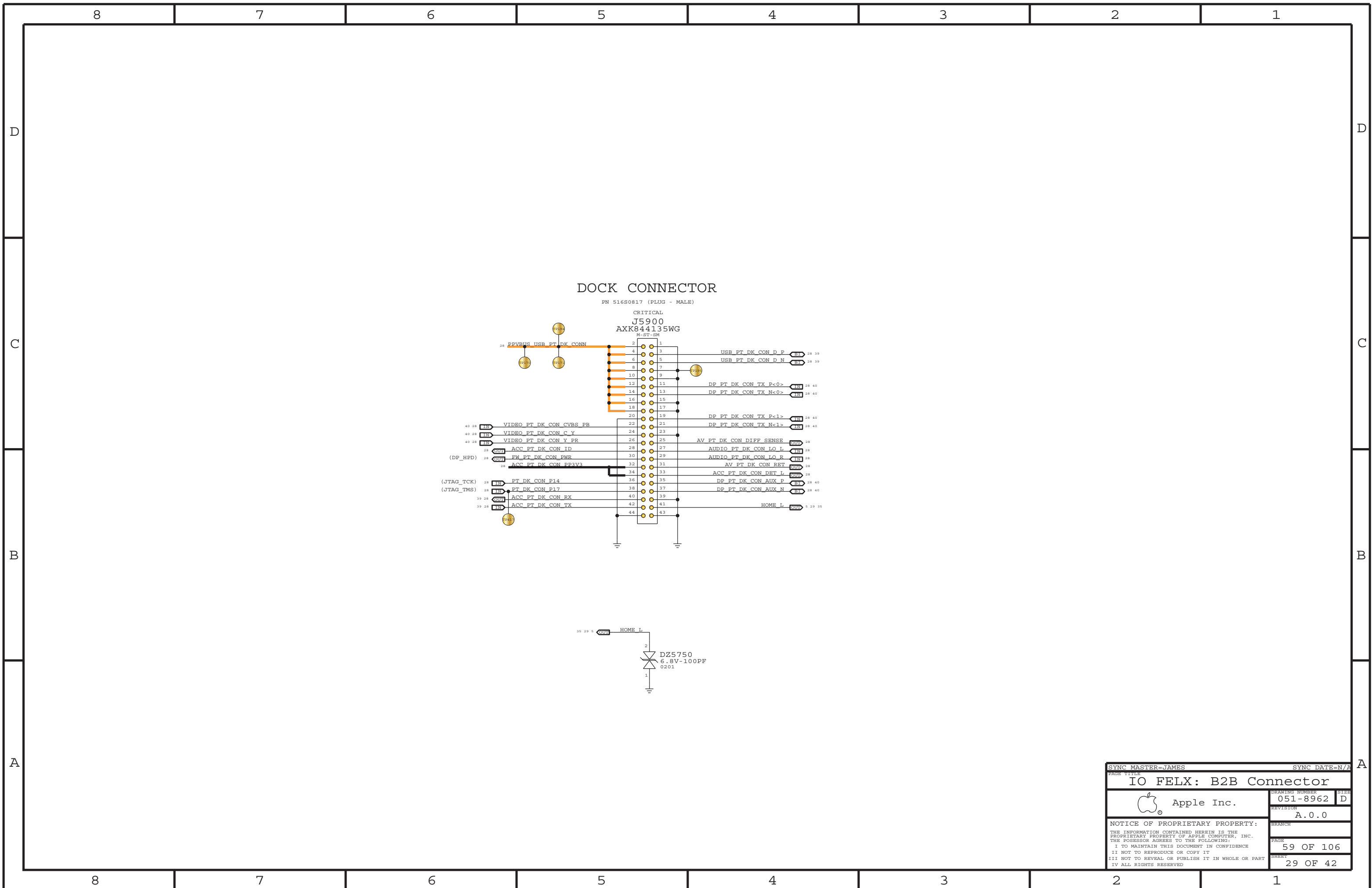
Apple Inc.


DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

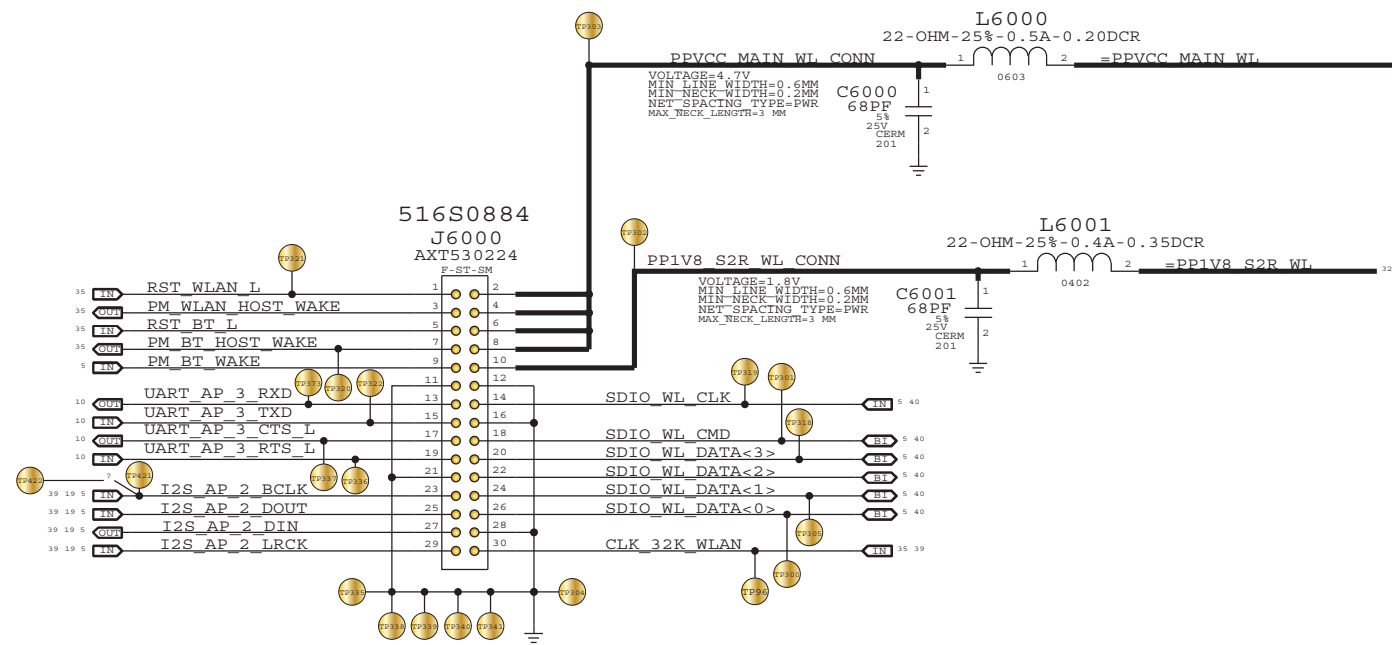
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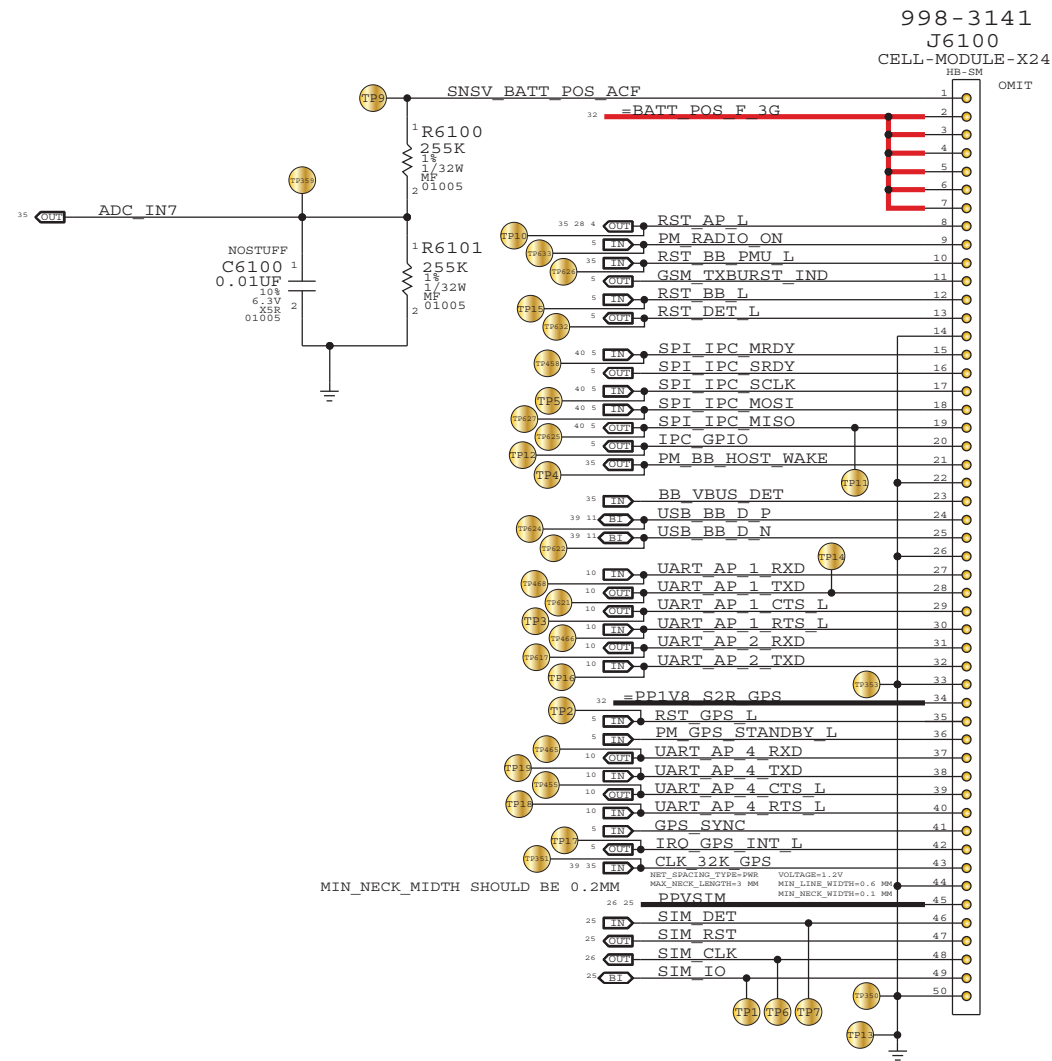
SYNC MASTER=JAMES		SYNC DATE=N/A	
IO FELX: B2B Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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		59 OF 106	
		SHEET	
		29 OF 42	

X23 WIFI/BT CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X23 WIFI/BT			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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X24 CELLULAR/GPS CONNECTOR



SYNC MASTER=MIKE		SYNC DATE=N/A	
CONNECTOR: X24 CELLULAR/GPS			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8962	D
		REVISION	
		A.0.0	
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POWER CONN / ALIAS

LDO RAILS

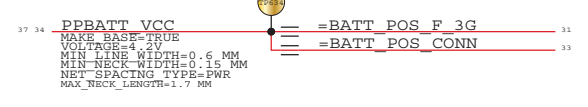
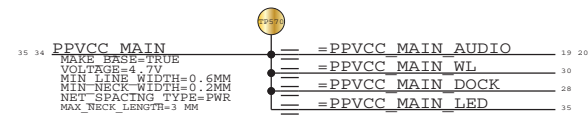
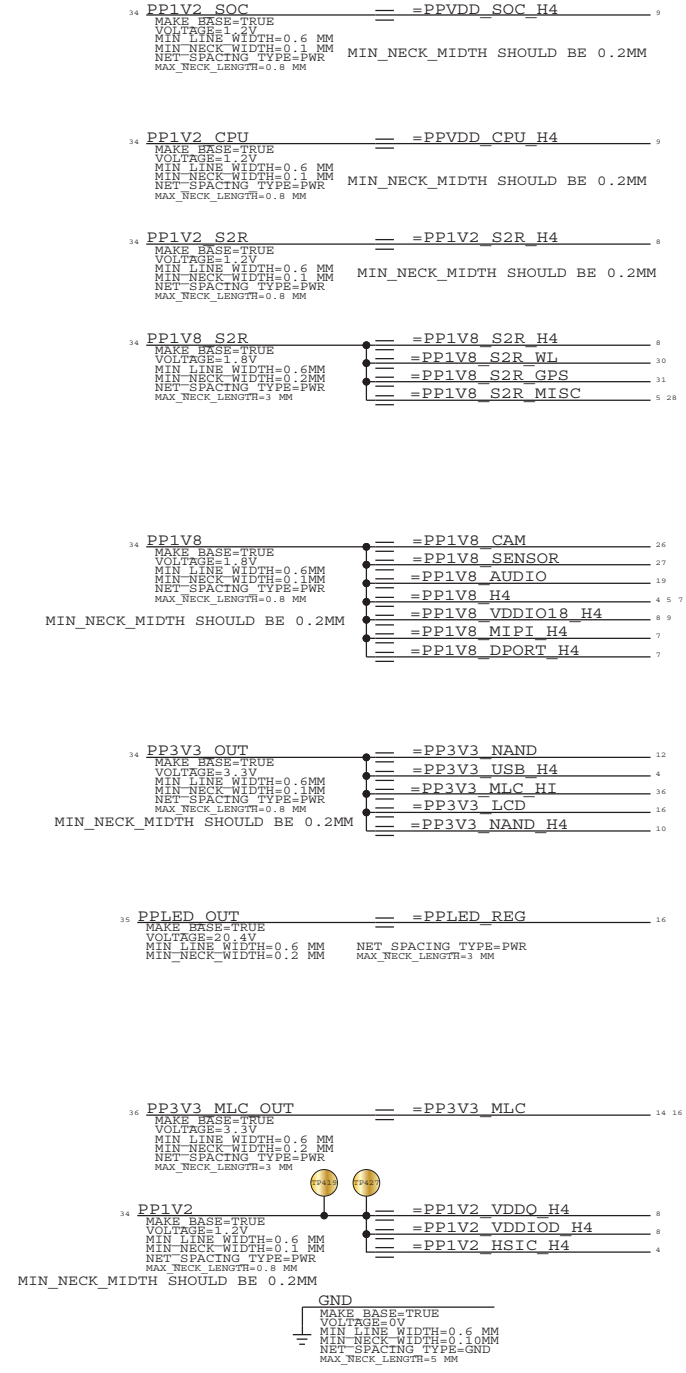
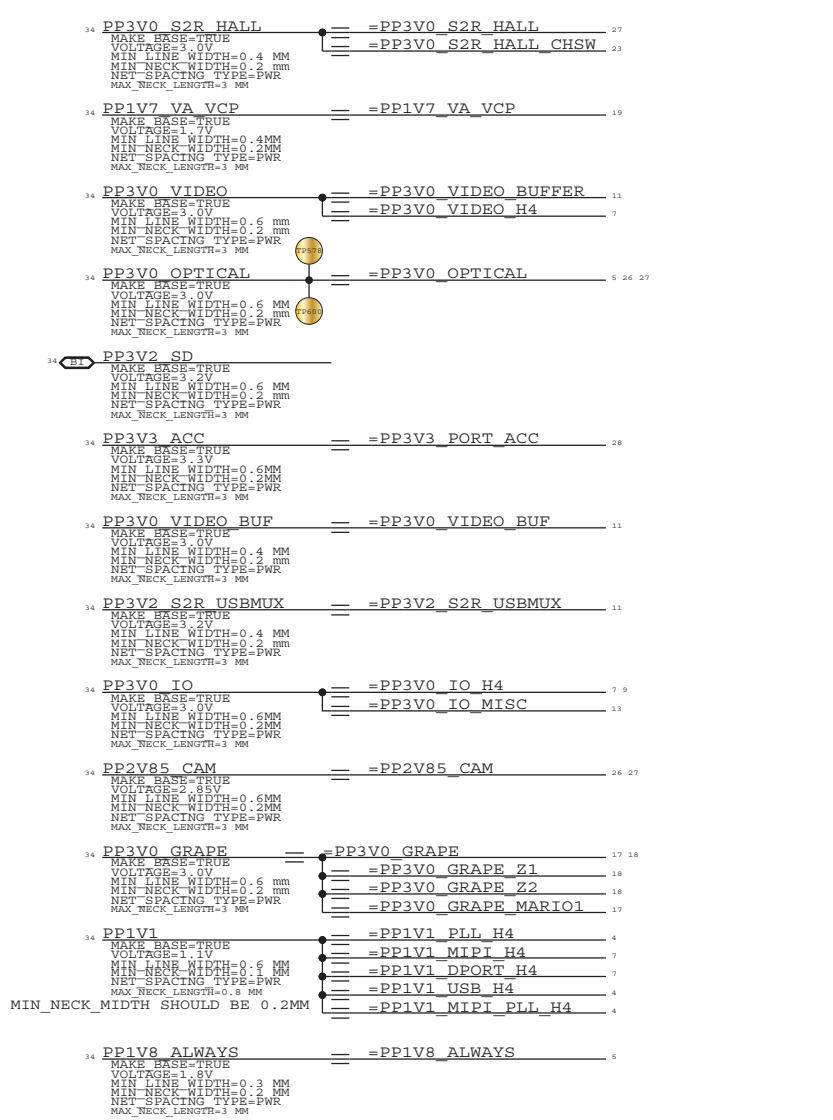
PROGRAMMABLE ON/OFF

BUCK RAILS

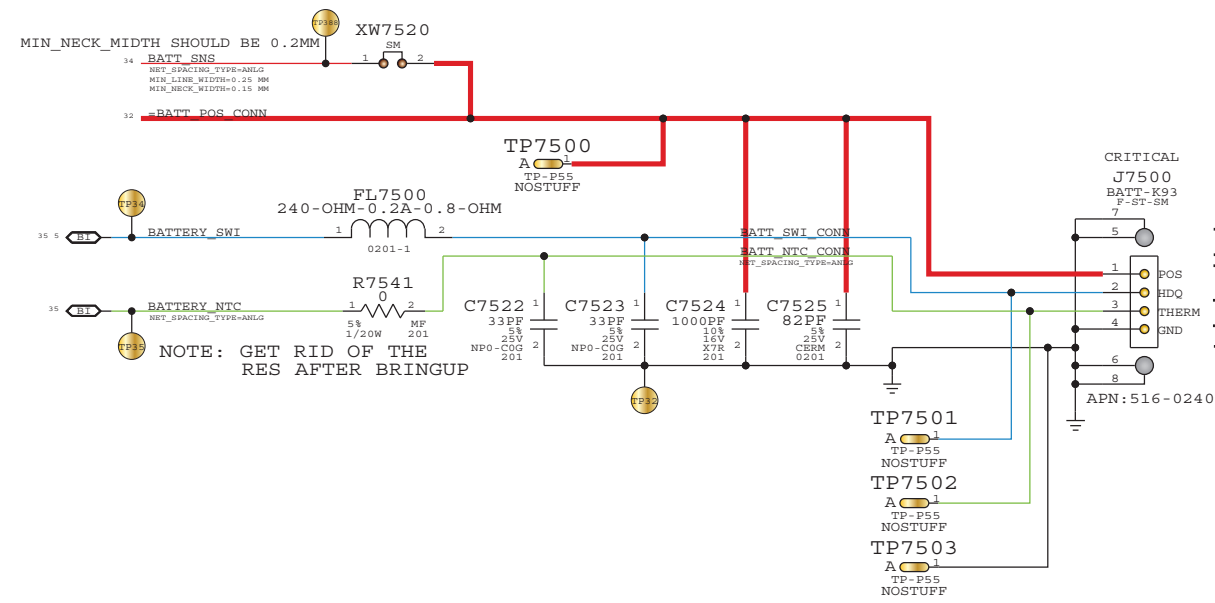
CHARGER MAIN

BATTERY

USB POWER INPUT



PAGE TITLE		SYNC DATE=N/A	
POWER: ALIASES			
Apple Inc.	DRAWING NUMBER	051-8962	SIZE
	REVISION	A.0.0	D
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NOTE:
VERIFY PINOUT OF
BATTERY CONNECTOR
VERIFY MOUNTING CONN TO GND

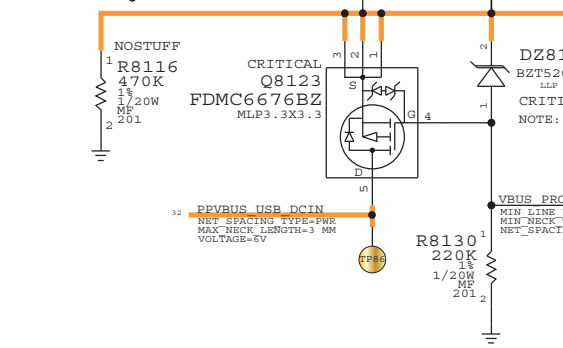
SYNC MASTER=YOSH		SYNC DATE=N/A	
POWER: BATTERY CONNECTOR			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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PAGE 75 OF 106		SHEET 33 OF 42	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34350542	1	IC, PMU, ALISON, D1946A2, OTPXX, UFBGA292	U8100	CRITICAL	

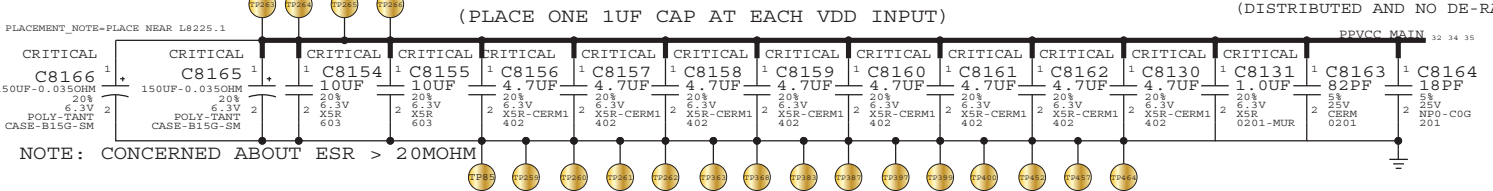
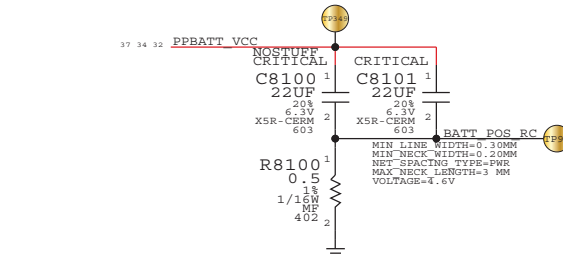
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19750392	19750299		Y8138	ALT FOUNDRY

USB REVERSE VOLTAGE PROTECTION

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



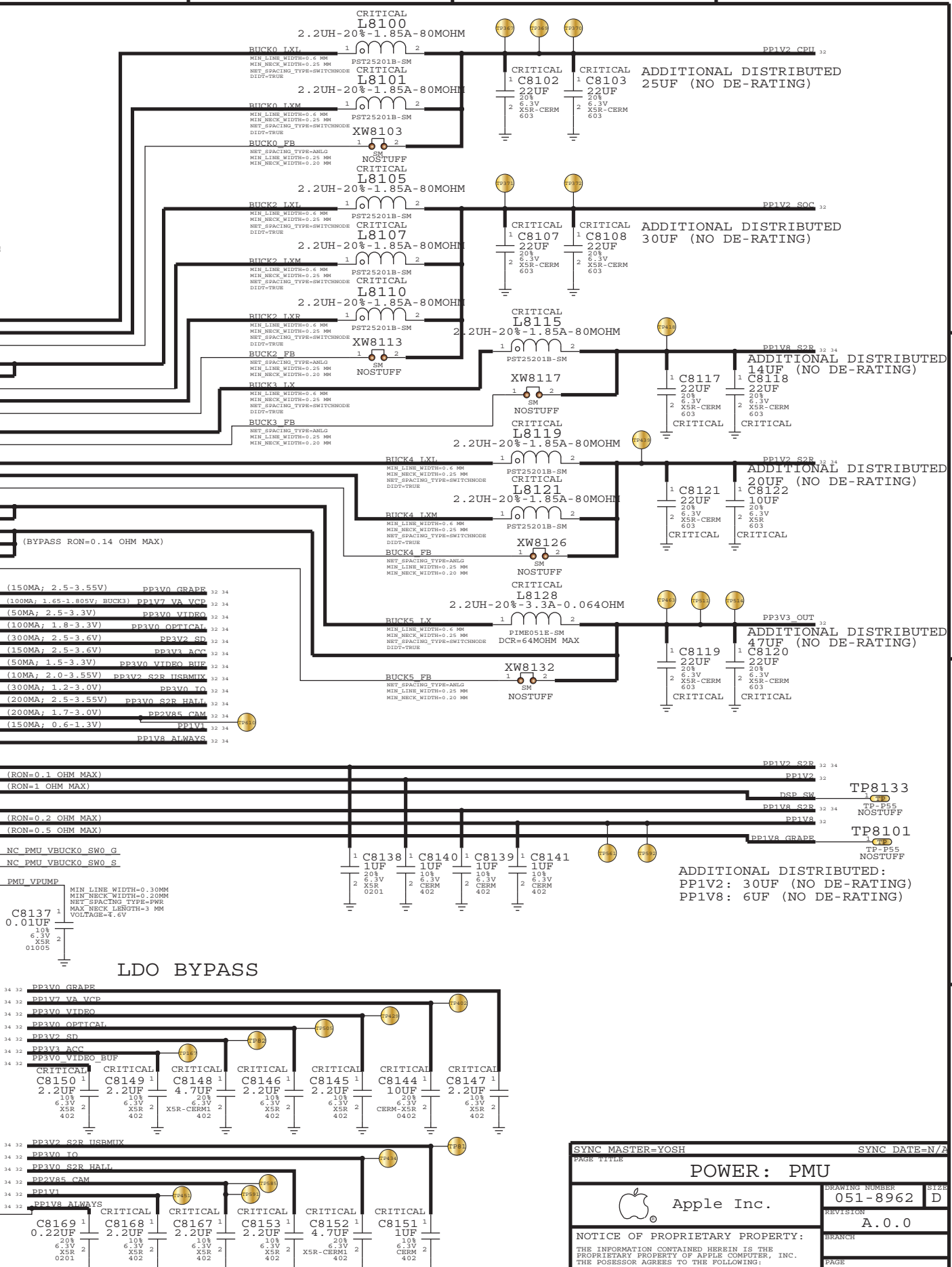
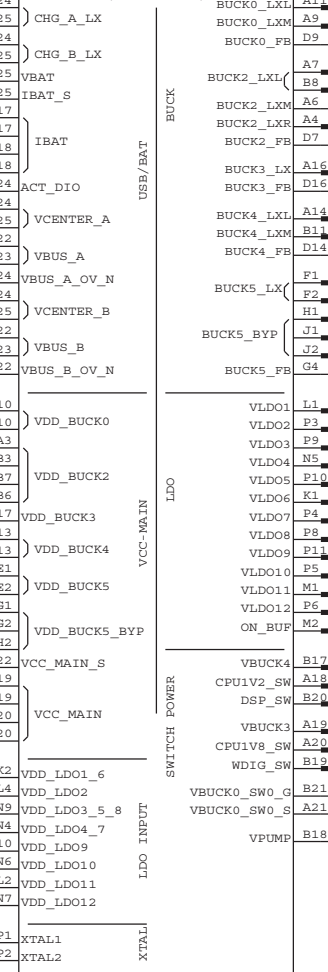
NOTE: FOR NO BATTERY SITUATION



VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)

This bull shits from APPLE have OMIT manufacturer of the PMIC and not only!

U8100
ALISON-A0-OTPXX
D1946A0-110-00
UFBGA
(SYM 2 OF 3)



SYNC MASTER=YOSH SYNC DATE=N/A

POWER: PMU

Apple Inc.

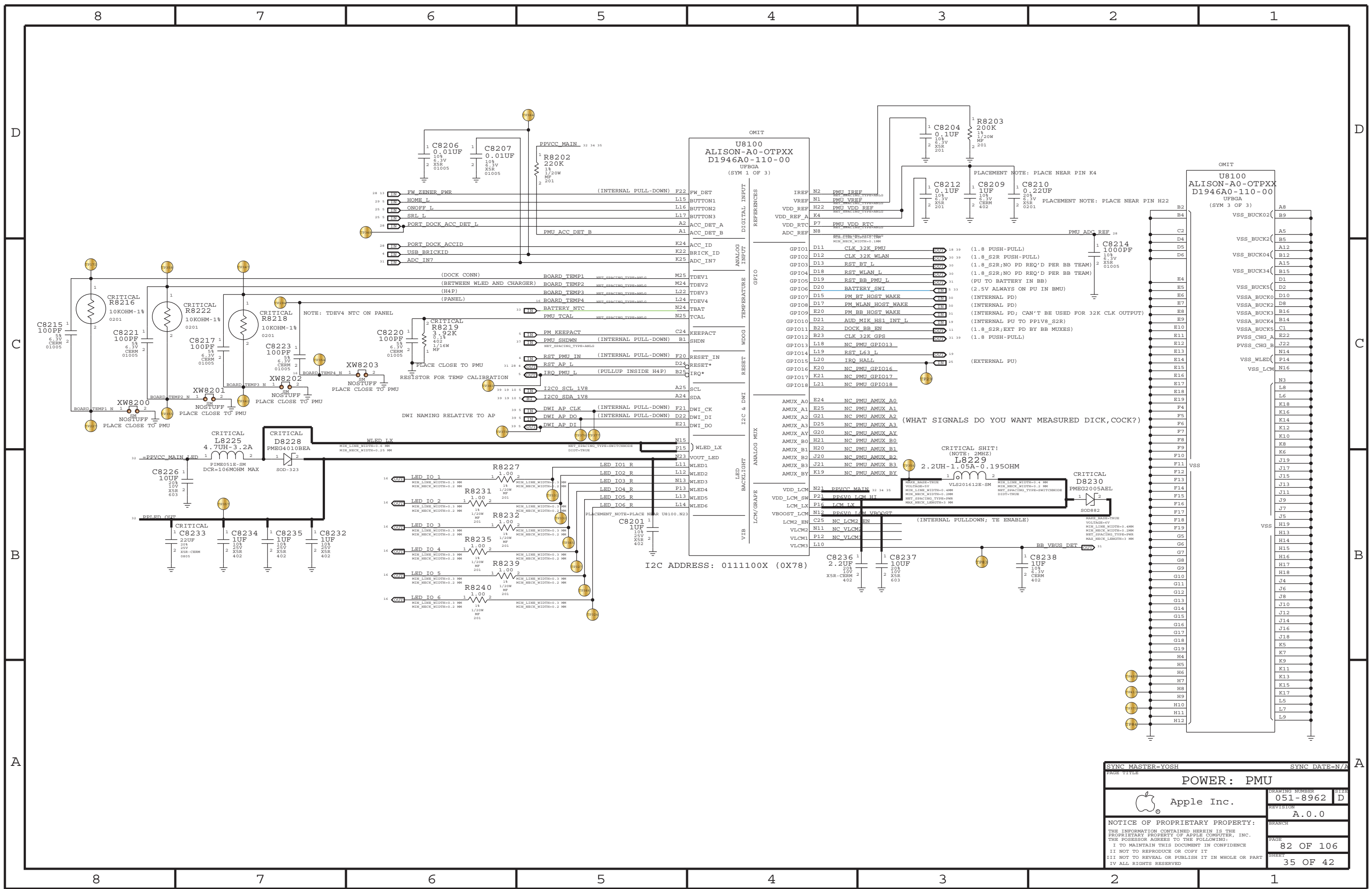
Drawing Number: 051-8962

Revision: A.0.0

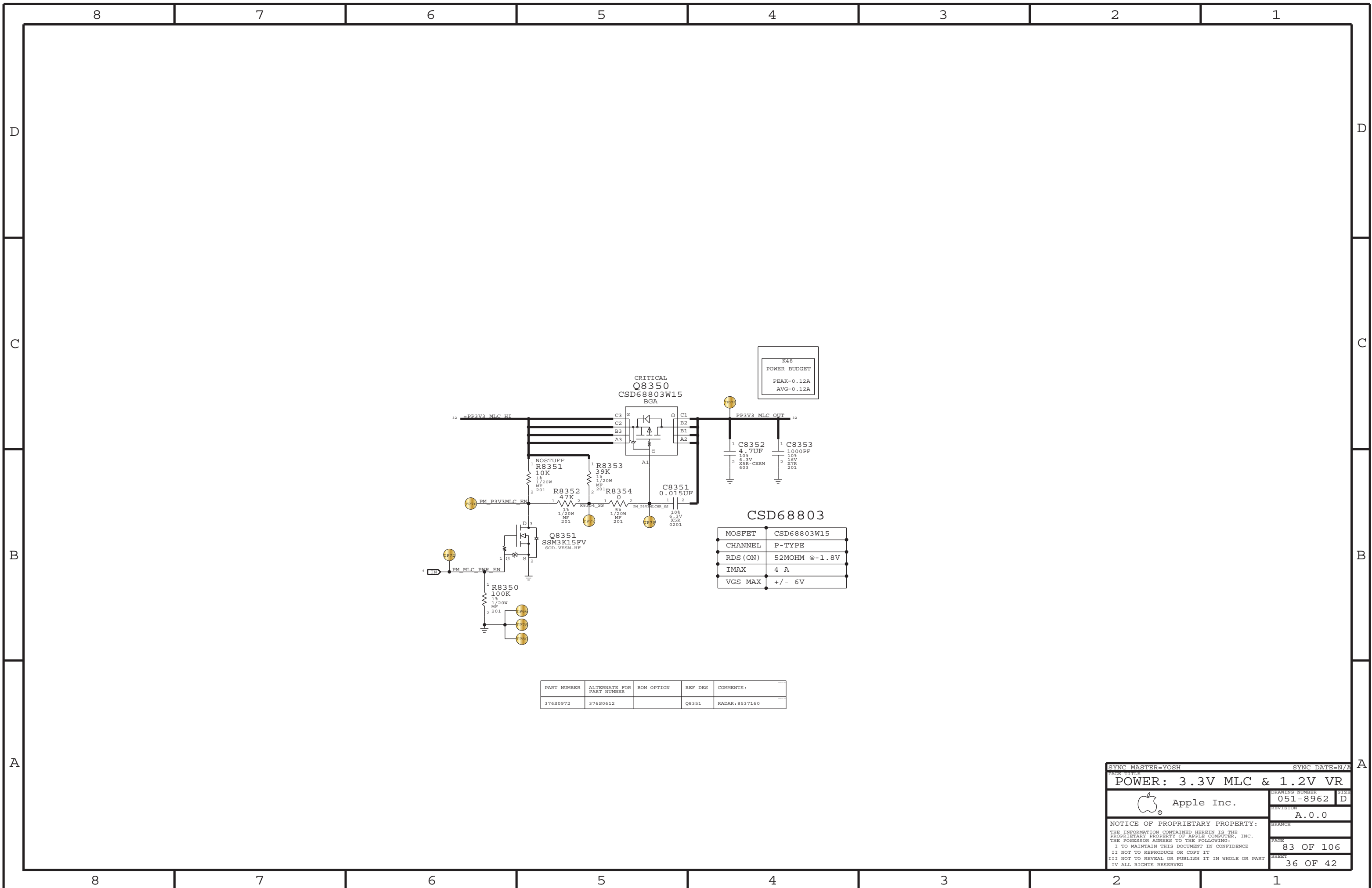
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PAGE TITLE		SYNC DATE=N/A	
POWER: PMU			
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		REVISION	
BRANCH		PAGE	82 OF 106
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K48
POWER BUDGET
PEAK=0.12A
AVG=0.12A

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS (ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0972	376S0612		Q8351	RADAR: 8537160

SYNC MASTER=YOSH SYNC DATE=N/A

POWER: 3.3V MLC & 1.2V VR

Apple Inc.

051-8962 D

REVISION A.0.0

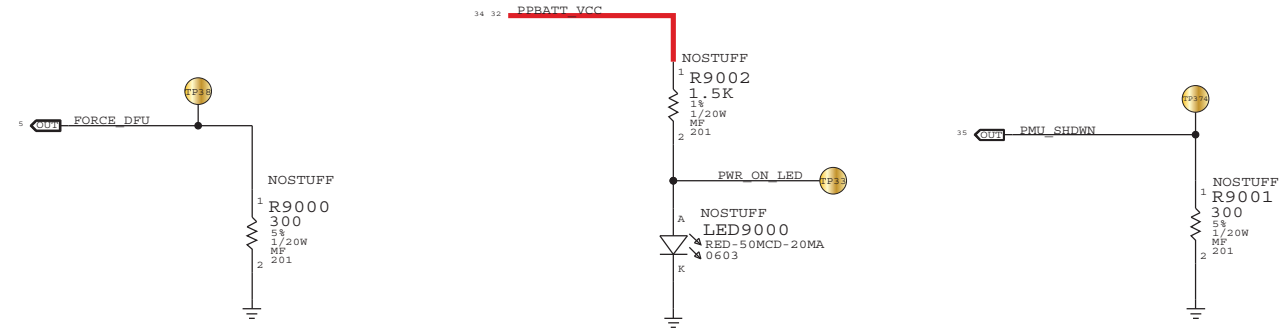
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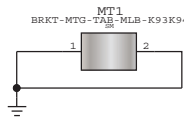
36 OF 42

DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS



SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE DEBUG AND MISC			
DRAWING NUMBER 051-8962		SIZE D	
REVISION A.0.0		BRANCH	
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8

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D

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C

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B

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A

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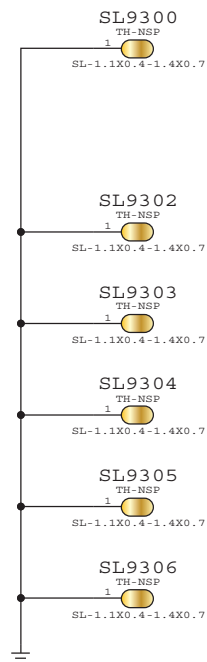
3

2

1

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=MIKE		SYNC DATE=N/A	
PAGE TITLE FCT/ICT TEST/BRACKETS			
DRAWING NUMBER 051-8962		SIZE D	
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Apple Inc.

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	CLK_50S	CLK	CLK 32K PMU 18 35
HE1	CLK_50S	CLK	CLK 32K WLAN 30 35
HE2	CLK_50S	CLK	CLK 32K GPS 31 35
HE3	CLK_50S	CLK	CLK CAM_FF 7 26
HE4	CLK_50S	CLK	CLK CAM_FF_FILT 7 26
HE5	CLK_50S	CLK	CLK CAM_FF_CONN 25 26
HE6	CLK_50S	CLK	CLK CAM_RF 7 27
HE7	CLK_50S	CLK	CLK CAM_RF_FILT 25 27
HE8	CLK_50S	CLK	I2S AP_0_MCK 5
HE9	CLK_50S	CLK	I2S AP_0_MCK_R 5 19
HE10	CLK_50S	CLK	CLK CAM_FF_R 7
HE11	CLK_50S	CLK	CLK CAM_RF_R 7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	NAND_50S	NAND	F0AD<7...0> 6 12
HE1	NAND_50S	NAND	F0CE0 L 4 12
HE2	NAND_50S	NAND	F0CE1 L 4 12
HE3	NAND_50S	NAND	F0CE2 L 4 12
HE4	NAND_50S	NAND	F0CE3 L 4 12
HE5	NAND_50S	NAND	F0CE4 L 4 12
HE6	NAND_50S	NAND	F0CE5 L 4 12
HE7	NAND_50S	NAND	F0CE6 L 4 12
HE8	NAND_50S	NAND	F0CE7 L 4 12
HE9	NAND_50S	NAND	F0CLE 4 12
HE10	NAND_50S	NAND	F0ALE 4 12
HE11	NAND_50S	NAND	F0RE L 4 12
HE12	NAND_50S	NAND	F0WE L 4 12
HE13	NAND_50S	NAND	F0WP L 4 12
HE14	NAND_50S	NAND	F1AD<7...0> 6 12
HE15	NAND_50S	NAND	F1CE0 L 4 12
HE16	NAND_50S	NAND	F1CE1 L 4 12
HE17	NAND_50S	NAND	F1CE2 L 4 12
HE18	NAND_50S	NAND	F1CE3 L 4 12
HE19	NAND_50S	NAND	F1CE4 L 4 12
HE20	NAND_50S	NAND	F1CE5 L 4 12
HE21	NAND_50S	NAND	F1CE6 L 4 12
HE22	NAND_50S	NAND	F1CE7 L 4 12
HE23	NAND_50S	NAND	F1CLE 4 12
HE24	NAND_50S	NAND	F1ALE 4 12
HE25	NAND_50S	NAND	F1RE L 4 12
HE26	NAND_50S	NAND	F1WE L 4 12
HE27	NAND_50S	NAND	F1WP L 4 12
HE28	NAND_50S	NAND	F2AD<7...0> 6 12
HE29	NAND_50S	NAND	F2CE0 L 4 12
HE30	NAND_50S	NAND	F2CE1 L 4 12
HE31	NAND_50S	NAND	F2CE2 L 4 12
HE32	NAND_50S	NAND	F2CE3 L 4 12
HE33	NAND_50S	NAND	F2CLE 4 12
HE34	NAND_50S	NAND	F2ALE 4 12
HE35	NAND_50S	NAND	F2RE L 4 12
HE36	NAND_50S	NAND	F2WE L 4 12
HE37	NAND_50S	NAND	F2WP L 4 12
HE38	NAND_50S	NAND	F3AD<7...0> 6 12
HE39	NAND_50S	NAND	F3CE0 L 4 12
HE40	NAND_50S	NAND	F3CE1 L 4 12
HE41	NAND_50S	NAND	F3CE2 L 4 12
HE42	NAND_50S	NAND	F3CE3 L 4 12
HE43	NAND_50S	NAND	F3CLE 4 12
HE44	NAND_50S	NAND	F3ALE 4 12
HE45	NAND_50S	NAND	F3RE L 4 12
HE46	NAND_50S	NAND	F3WE L 4 12
HE47	NAND_50S	NAND	F3WP L 4 12

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		JTAG	JTAG AP_TCK 4 28
HE1		JTAG	JTAG AP_TMS 4 28
HE2		JTAG	JTAG AP_TDI 4 10
HE3		JTAG	JTAG AP_TDO 4 10
HE4		JTAG	JTAG AP_TRST_L 4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	I2C_50S	I2C	I2C1_SDA_1V8 5 25
HE1	I2C_50S	I2C	I2C1_SCL_1V8 5 25
HE2	I2C_50S	I2C	I2C0_SDA_1V8 5 10 19 35
HE3	I2C_50S	I2C	I2C0_SCL_1V8 5 10 19 35
HE4	I2C_50S	I2C	I2C2_SDA_3V0 5 25 26
HE5	I2C_50S	I2C	I2C2_SCL_3V0 5 25 26
HE6	I2C_50S	I2C	ISP_AP_0_SCL 7 25
HE7	I2C_50S	I2C	ISP_AP_0_SDA 7 25
HE8	I2C_50S	I2C	ISP_AP_1_SCL 7 26
HE9	I2C_50S	I2C	ISP_AP_1_SDA 7 26
HE10	I2C_50S	I2C	I2C2_SCL_3V0_ALS 25 26
HE11	I2C_50S	I2C	I2C2_SDA_3V0_ALS 25 26
HE12	I2C_50S	I2C	ISP_CAM_1_SCL 25 26
HE13	I2C_50S	I2C	ISP_CAM_1_SDA 25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		CRYSTAL	XTAL_24M_I 4
HE1		CRYSTAL	XTAL_24M_O 4
HE2		CRYSTAL	24M_O 4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		VREF	PPVREF_DDR0_CA 8
HE1		VREF	PPVREF_DDR0_DO 8
HE2		VREF	PPVREF_DDR1_CA 8
HE3		VREF	PPVREF_DDR1_DO 8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	USB_90D	USB	USB_D_P 4 28
HE1	USB_90D	USB	USB_D_N 4 28
HE2	USB_90D	USB	USB_PT_DK_CON_D_P 28 29
HE3	USB_90D	USB	USB_PT_DK_CON_D_N 28 29
HE4	USB_90D	USB	USB_BB_D_P 11 31
HE5	USB_90D	USB	USB_BB_D_N 11 31
HE6	USB_90D	USB	USB_FS_D_P 4 11
HE7	USB_90D	USB	USB_FS_D_N 4 11
HE8	USB_90D	USB	USB_FS_N_ACC_TX 11 28
HE9	USB_90D	USB	USB_FS_P_ACC_RX 11 28
HE10	USB_90D	USB	ACC_PT_DK_CON_TX 28 29
HE11	USB_90D	USB	ACC_PT_DK_CON_RX 28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0	I2S_50S	I2S	I2S_AP_0_BCLK 5 19
HE1	I2S_50S	I2S	I2S_AP_0_LRCK 5 19
HE2	I2S_50S	I2S	I2S_AP_0_DIN 5 19
HE3	I2S_50S	I2S	I2S_AP_0_DOUT 5 19
HE4	I2S_50S	I2S	I2S_AP_2_BCLK 5 19 30
HE5	I2S_50S	I2S	I2S_AP_2_LRCK 5 19 30
HE6	I2S_50S	I2S	I2S_AP_2_DIN 5 19 30
HE7	I2S_50S	I2S	I2S_AP_2_DOUT 5 19 30
HE8	I2S_50S	I2S	I2S_AP_3_BCLK 5 19
HE9	I2S_50S	I2S	I2S_AP_3_LRCK 5 19
HE10	I2S_50S	I2S	I2S_AP_3_DIN 5 19
HE11	I2S_50S	I2S	I2S_AP_3_DOUT 5 19
HE12	I2S_50S	I2S	I63_XSP_SDOUT 19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
HE0		DWI	DWI_AP_CLK 5 35
HE1		DWI	DWI_AP_DI 5 35
HE2		DWI	DWI_AP_DO 5 35

SYNC MASTER=MIKE		SYNC DATE=N/A	
CONSTRAINTS: ASSIGNMENTS			
Apple Inc.		DRAWING NUMBER	051-8962
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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E230	VID_50S	ANALOG_VIDEO	DAC AP OUT1	7 11
1E230	VID_50S	ANALOG_VIDEO	DAC AP OUT2	7 11
1E230	VID_50S	ANALOG_VIDEO	DAC AP OUT3	7 11
1E230	VID_50S	ANALOG_VIDEO	BUF C Y	11
1E230	VID_50S	ANALOG_VIDEO	BUF CVBS PB	11
1E230	VID_50S	ANALOG_VIDEO	BUF Y PR	11
1E230	VID_50S	ANALOG_VIDEO	VIDEO EMI CVBS PB	10 11 28
1E230	VID_50S	ANALOG_VIDEO	VIDEO EMI C Y	10 11 28
1E230	VID_50S	ANALOG_VIDEO	VIDEO EMI Y PR	10 11 28
1E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON CVBS PB	28 29
1E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON C Y	28 29
1E230	VID_50S	ANALOG_VIDEO	VIDEO PT DK CON Y PR	28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	LVDS_100D	LVDS	LVDS DATA P<2..0>	14 16
1E240	LVDS_100D	LVDS	LVDS DATA N<2..0>	14 16
1E240	LVDS_100D	LVDS	LVDS DATA CONN P<2..0>	16
1E240	LVDS_100D	LVDS	LVDS DATA CONN N<2..0>	16
1E240	LVDS_100D	LVDS	LVDS CLK P	14 16
1E240	LVDS_100D	LVDS	LVDS CLK N	14 16
1E240	LVDS_100D	LVDS	LVDS CLK CONN P	16
1E240	LVDS_100D	LVDS	LVDS CLK CONN N	16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	DP_100D	DP	DP AP TX P<0>	7 10 13
1E240	DP_100D	DP	DP AP TX N<0>	7 10 13
1E240	DP_100D	DP	DP AP TX P<1>	7 10 13
1E240	DP_100D	DP	DP AP TX N<1>	7 10 13
1E240	DP_100D	DP	DP AP AUX P	7 13
1E240	DP_100D	DP	DP AP AUX N	7 13
1E240	DP_100D	DP	DP EMI TX P<0>	13 28
1E240	DP_100D	DP	DP EMI TX N<0>	13 28
1E240	DP_100D	DP	DP EMI TX P<1>	13 28
1E240	DP_100D	DP	DP EMI TX N<1>	13 28
1E240	DP_100D	DP	DP EMI AUX P	13 28
1E240	DP_100D	DP	DP EMI AUX N	13 28
1E240	DP_100D	DP	DP PT DK CON TX P<0>	28 29
1E240	DP_100D	DP	DP PT DK CON TX N<0>	28 29
1E240	DP_100D	DP	DP PT DK CON TX P<1>	28 29
1E240	DP_100D	DP	DP PT DK CON TX N<1>	28 29
1E240	DP_100D	DP	DP PT DK CON AUX P	28 29
1E240	DP_100D	DP	DP PT DK CON AUX N	28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	MIPI_100D	MIPT	MIPI AP DATA P<0>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<0>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA P<1>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<1>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA P<2>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<2>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA P<3>	7 14
1E240	MIPI_100D	MIPT	MIPI AP DATA N<3>	7 14
1E240	MIPI_100D	MIPT	MIPI AP CLK P	7 14
1E240	MIPI_100D	MIPT	MIPI AP CLK N	7 14
1E240	MIPI_100D	MIPT	MIPI OC AP DATA P<0>	7 27
1E240	MIPI_100D	MIPT	MIPI OC AP DATA N<0>	7 27
1E240	MIPI_100D	MIPT	MIPI OC AP CLK P	7 27
1E240	MIPI_100D	MIPT	MIPI OC AP CLK N	7 27
1E240	MIPI_100D	MIPT	MIPI OC CAM DATA P<0>	25 27
1E240	MIPI_100D	MIPT	MIPI OC CAM DATA N<0>	25 27
1E240	MIPI_100D	MIPT	MIPI OC CAM CLK P	25 27
1E240	MIPI_100D	MIPT	MIPI OC CAM CLK N	25 27
1E240	MIPI_100D	MIPT	MIPI IC AP DATA P<0>	7 26
1E240	MIPI_100D	MIPT	MIPI IC AP DATA N<0>	7 26
1E240	MIPI_100D	MIPT	MIPI IC AP CLK P	7 26
1E240	MIPI_100D	MIPT	MIPI IC AP CLK N	7 26
1E240	MIPI_100D	MIPT	MIPI IC CAM DATA P<0>	25 26
1E240	MIPI_100D	MIPT	MIPI IC CAM DATA N<0>	25 26
1E240	MIPI_100D	MIPT	MIPI IC CAM CLK P	25 26
1E240	MIPI_100D	MIPT	MIPI IC CAM CLK N	25 26

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	AUDIO	AUDIO	LEFT_CH_OUT_P	19 20
1E240	AUDIO	AUDIO	LEFT_CH_OUT_REF	19 20
1E240	AUDIO	AUDIO	LEFT_CH_P	20
1E240	AUDIO	AUDIO	SSM2375_L_IN_P	20
1E240	AUDIO	AUDIO	SSM2375_L_IN_N	20
1E240	AUDIO	AUDIO	RIGHT_CH_OUT_P	19 20
1E240	AUDIO	AUDIO	RIGHT_CH_OUT_REF	19 20
1E240	AUDIO	AUDIO	RIGHT_CH_P	20
1E240	AUDIO	AUDIO	SSM2375_R_IN_P	20
1E240	AUDIO	AUDIO	SSM2375_R_IN_N	20
1E240	AUDIO	AUDIO	EXT_MIC_P	19 23
1E240	AUDIO	AUDIO	EXT_MIC_REF	19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	SDIO_50S	SDIO	SDIO_WL_CLK	5 30
1E240	SDIO_50S	SDIO	SDIO_WL_CLK_R	5 30
1E240	SDIO_50S	SDIO	SDIO_WL_CMD	5 30
1E240	SDIO_50S	SDIO	SDIO_WL_DATA<3..0>	5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	PHYSICAL
	PHYSICAL	SPACING		
1E240	SPI_50S	SPT	SPI GRAPE MISO	5 17
1E240	SPI_50S	SPT	SPI GRAPE MOSI	5 17
1E240	SPI_50S	SPT	SPI GRAPE SCLK	5 17
1E240	SPI_50S	SPT	SPI GRAPE CS_L	5 17
1E240	SPI_50S	SPT	SPI IPC MISO	5 31
1E240	SPI_50S	SPT	SPI IPC MOSI	5 31
1E240	SPI_50S	SPT	SPI IPC SCLK	5 31
1E240	SPI_50S	SPT	SPI IPC MRDY	5 31

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE: CONSTRAINTS: ASSIGNMENTS

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL3, ISL8, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2, ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES

100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP, BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL3, ISL8, ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4, ISL5, ISL6, ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS


POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP, BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

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