1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-01-24

SCHEM,RIO,D2

PIB2B, 03/16/2012

820-3071-10.brd

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8974	1	SCHEM,RIO,J5	SCH	CRITICAL	
820-3071	1	PCBF,RIO,J5	PCB	CRITICAL	

DRAWING
TITLE=TITLE
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 16 13:44:38 2012

DRAWING TITLE: SCHEM,RIO,D2

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION

BRANCH

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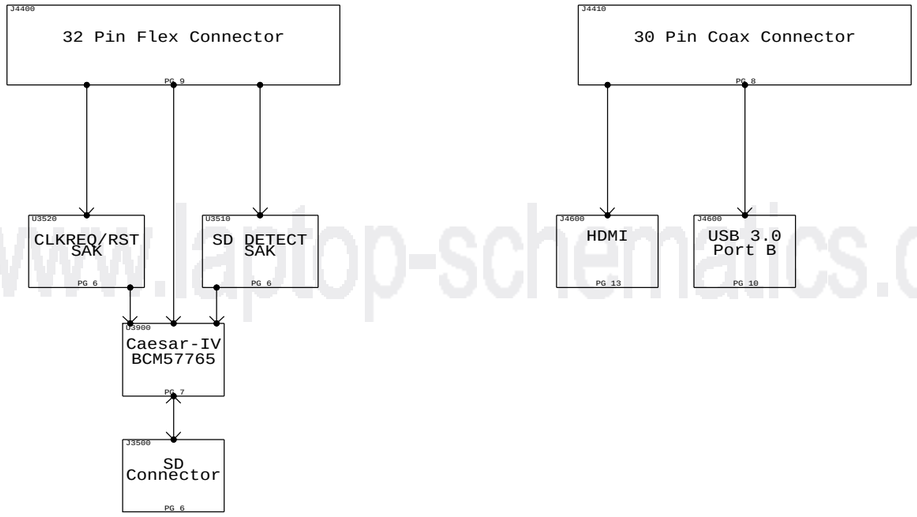
SHEET: 1 OF 15



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
System Block Diagram

Apple Inc.

DRAWING NUMBER | SIZE D

REVISION

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1907	PCBA,RIO,J5	J5_RIO_COMMON,EEEE:DL62
085-2805	PCBA,DEV RIO,J5	J5_RIO_DEVEL:ENG

J5 RIO BOM GROUPS

BOM GROUP	BOM OPTIONS
J5_RIO_COMMON	COMMON,ENETLOWPWR:NO,J5_RIO_PROGPARTS,HDMI_3V3_S0:YES,ALTERNATE
J5_RIO_PROGPARTS	
J5_RIO_DEVEL:ENG	ENET_ROM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0311	128S0329		ALL	NEC alt to Sanyo
197S0450	197S0177		ALL	Alt EPSON Xtal
197S0451	197S0177		ALL	Alt NDK Xtal

Bar Code Labels / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7753	1	TEXT,LABEL,RIO,D2	[EEEE:DL62]	CRITICAL	EEEE:DL62
825-7697	1	LBL,SERIAL NO,BOARDS,D2	TEXT_LABEL	CRITICAL	EEEE:DL62

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Programmables - All builds

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER | SIZE: D

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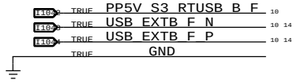
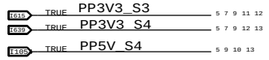
Functional Test Points

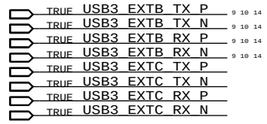
USB PORTS

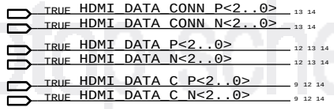


POWER RAILS



NO_TEST=TRUE





SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Functional / ICT Test

Apple Inc.

DRAWING NUMBER | SIZE: D

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SHEET: 4 OF 15

PP5V_S4 — 13 10 9 5 4

PP5V_S4
MIN_LINE_WIDTH=0.5 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE — 4 5 9 10 13
PP5V_S4 — 4 5 9 10 13
PP5V_S4 — 4 5 9 10 13

PP3V3_S4 — 12 9 7 5 4 13

PP3V3_S4
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE — 4 5 7 9 12 13
PP3V3_S4 — 4 5 7 9 12 13
PP3V3_S4 — 4 5 7 9 12 13

PP3V3_S3 — 11 9 7 5 4 12

PP3V3_S3
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE — 4 5 7 9 11 12
PP3V3_S3 — 4 5 7 9 11 12
PP3V3_S3 — 4 5 7 9 11 12
PP3V3_S3 — 4 5 7 9 11 12
PP3V3_S3 — 4 5 7 9 11 12
PP3V3_S3 — 4 5 7 9 11 12

PP3V3_HDMI — 12 5

PP3V3_HDMI
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE — 5 12
PP3V3_HDMI — 5 12
PP3V3_HDMI — 5 12

ENET Rails

PP3V3_ENET — 11 8 7 5

PP3V3_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE — 5 7 8 11
PP3V3_ENET — 5 7 8 11

PP1V2_ENET — 11 8 7 5

PP1V2_ENET
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE — 5 7 8 11
PP1V2_ENET — 5 7 8 11

1.5V Rail

PP1V5_S0 — 12 9 5

PP1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE — 5 9 12
PP1V5_S0 — 5 9 12
PP1V5_S0 — 5 9 12

GND
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER
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APN870-2451
Pogo pins

SH900
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM
1

SH901
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM
1

SH902
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM
1

SH903
POGO-2.3OD-5.5H-SM-LOW-FORCE
SM
1

APN806-2500
can shield

S904
SM
1
SHLD-J5-USB-RIO

APN806-2865
can shield

S905
SM
1
SHLD-J5-HDMI

APN998-1457
SMT GND connuity test pin

T900
1
A
TP-1P0-TOP

Unused ethernet signals

ENET_MDI_P<3..0> = NC_ENET_MDI_P<3..0>
MAKE_BASE=TRUE NO_TEST=TRUE
ENET_MDI_N<3..0> = NC_ENET_MDI_N<3..0>
MAKE_BASE=TRUE NO_TEST=TRUE
NC_ENET_WAKE_L = NC_ENET_WAKE_L
MAKE_BASE=TRUE NO_TEST=TRUE
NC_ENET_MEDIA_SENSE = NC_ENET_MEDIA_SENSE
MAKE_BASE=TRUE NO_TEST=TRUE

SYSCLK_CLK25M_ENET = SYSCLK_CLK25M_ENET
MAKE_BASE=TRUE

APN:998-3975

TH900
TH-NSP
1
SL-1.1X0.45-1.4x0.75

TH901
TH-NSP
1
SL-1.1X0.45-1.4x0.75

TH902
TH-NSP
1
SL-1.1X0.45-1.4x0.75

TH903
TH-NSP
1
SL-1.1X0.45-1.4x0.75

TH900/1 for USB can gnd slot
TH902/3 for HDMI can gnd slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE
Signal Aliases
Apple Inc.
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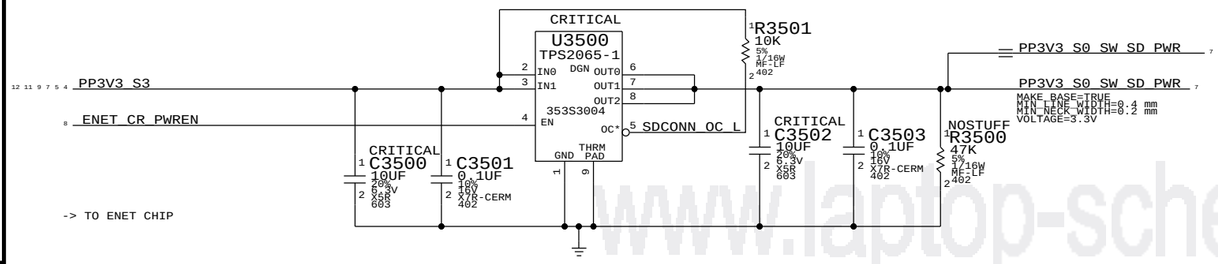
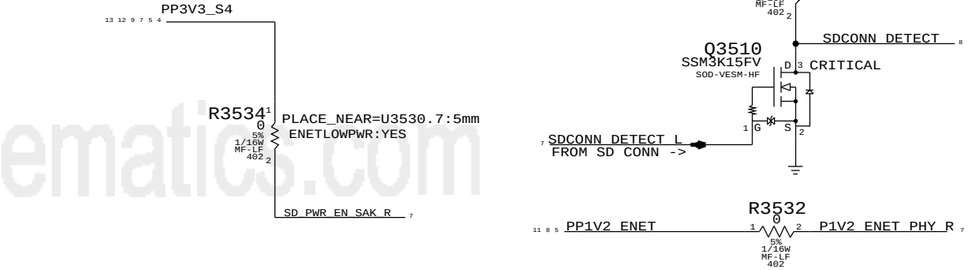
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

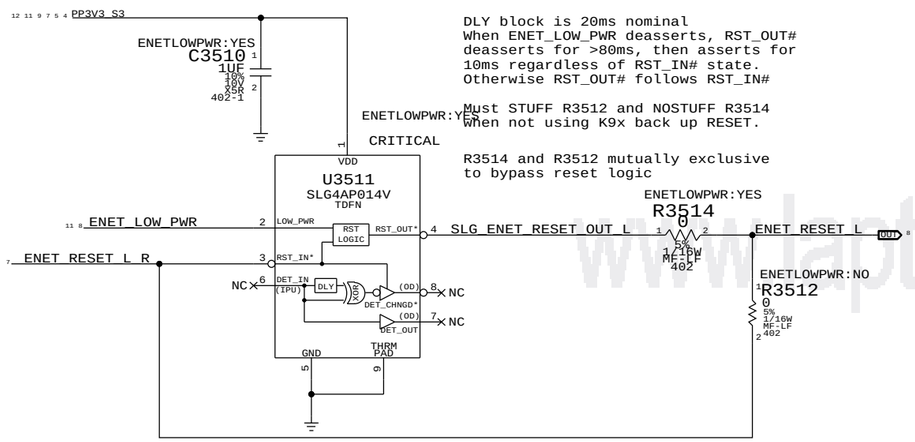
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R3500 IS NOSTUFF.



DETECT ISOLATION CIRCUIT

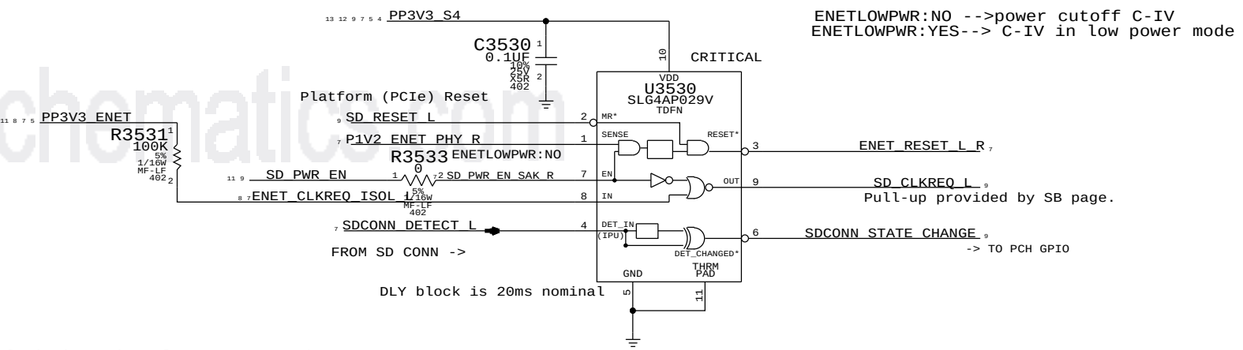


DETECT-CHANGED PCH GPIO LATCH CIRCUIT



Supervisor & CLKREQ# Isolation

SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO LATCH CIRCUIT

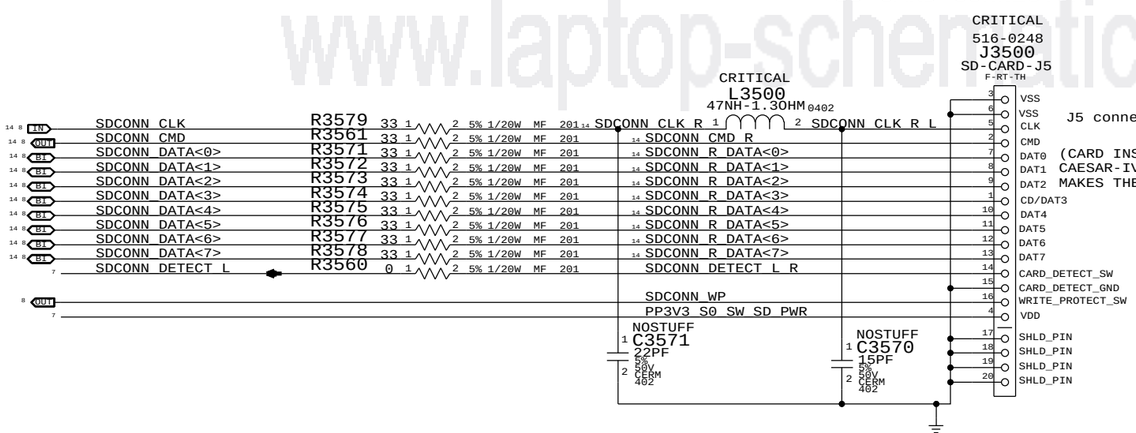


Note logic inversion of K16 connector.
Input to C-IV should remain active low

New part SLGAP029V (APN 343s0563)

ENET_CLKREQ_ISOL_L ═ ENET_CLKREQ_ISOL_L
MAKE_BASE=TRUE

SD CARD CONNECTOR



J5 connector different from K9X connector which was CARD INSERTED = OPEN

(CARD INSERTED = GROUND)
CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
MAKES THE ACTIVE-HIGH CASE UNUSABLE.

SYNC_MASTER=RIO_BEN SYNC_DATE=07/01/2011

PAGE TITLE: SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER | SIZE: D
REVISION
BRANCH
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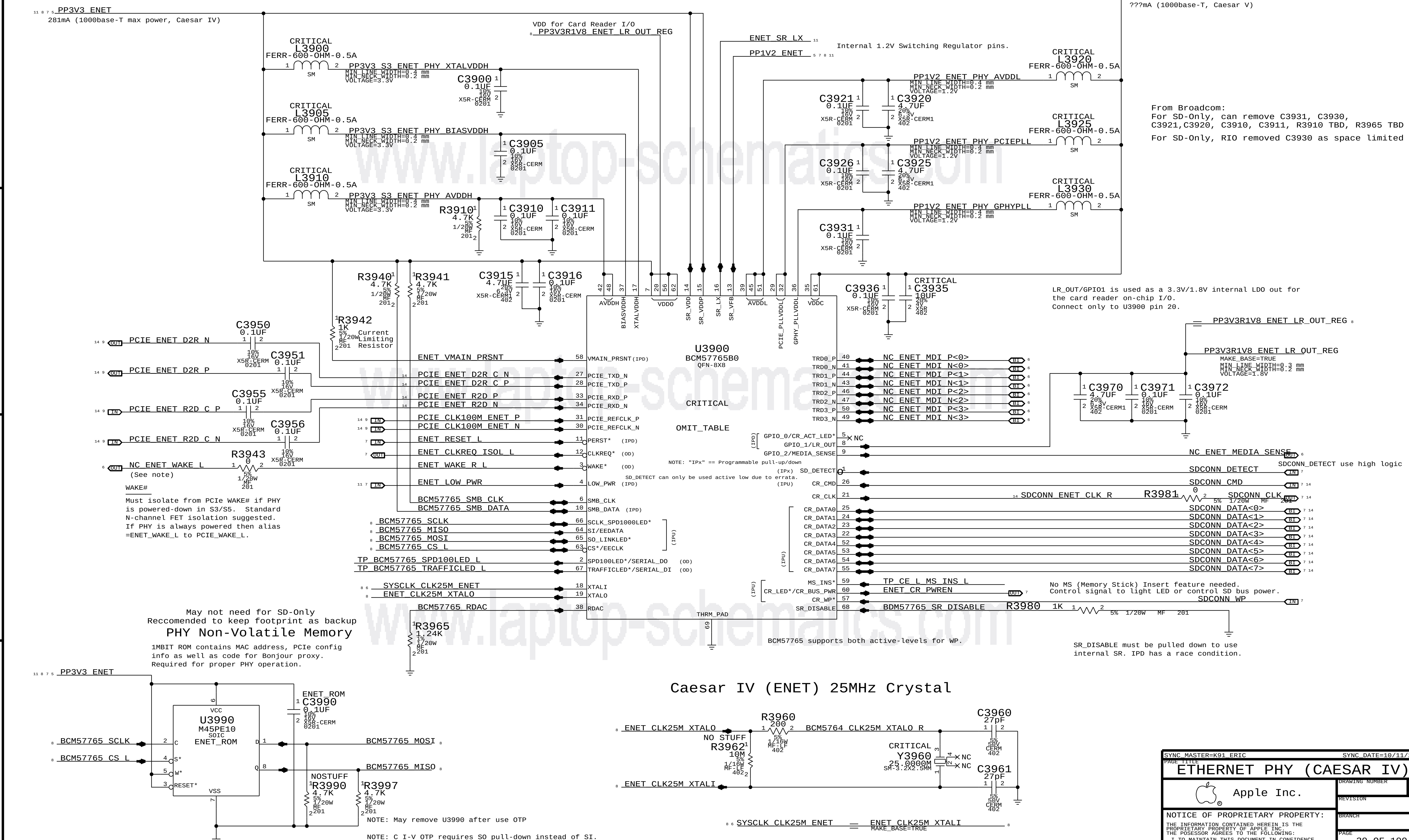
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0591	1	D2, 57100, SD CNTRL ONLY, B0, QFN 8x8	U3900	CRITICAL	

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.



PP3V3_ENET
281mA (1000base-T max power, Caesar IV)
VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG
ENET_SR_LX
PP1V2_ENET
Internal 1.2V Switching Regulator pins.
PP1V2_ENET
???mA (1000base-T, Caesar V)
CRITICAL L3900 FERR-600-OHM-0.5A SM
PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
CRITICAL L3905 FERR-600-OHM-0.5A SM
PP3V3_S3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 16V X5R-CERM 0201
CRITICAL L3910 FERR-600-OHM-0.5A SM
PP3V3_S3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/20W MF 201
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201
CRITICAL L3920 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_AVDDL
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402
CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402
CRITICAL L3930 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X5R-CERM 0201
From Broadcom:
For SD-Only, can remove C3931, C3930, C3921,C3920, C3910, C3911, R3910 TBD, R3965 TBD
For SD-Only, RIO removed C3930 as space limited
R3940 4.7K 5% 1/20W MF 201
R3941 4.7K 5% 1/20W MF 201
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201
C3936 0.1UF 10% 16V X5R-CERM 0201
CRITICAL C3935 10UF 20% 4V X5R 402
LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.
PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C3970 4.7UF 20% 6.3V X5R-CERM1 402
C3971 0.1UF 10% 16V X5R-CERM 0201
C3972 0.1UF 10% 16V X5R-CERM 0201
R3942 1K 5% 1/20W MF 201
Current Limiting Resistor
C3950 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_D2R_N
C3951 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_D2R_P
C3955 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_R2D_C_P
C3956 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_R2D_C_N
R3943 0 5% 1/20W MF 201
NC_ENET_WAKE_L
(See note)
WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.
U3900
BCM57765B0
QFN-8X8
CRITICAL
OMIT_TABLE
AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC
ENET_VMAIN_PRSNT 58 VMAIN_PRSNT (IPD)
PCIE_ENET_D2R_C_N 27 PCIE_TXD_N
PCIE_ENET_D2R_C_P 28 PCIE_TXD_P
PCIE_ENET_R2D_P 33 PCIE_RXD_P
PCIE_ENET_R2D_N 34 PCIE_RXD_N
PCIE_CLK100M_ENET_P 31 PCIE_REFCLK_P
PCIE_CLK100M_ENET_N 30 PCIE_REFCLK_N
ENET_RESET_L 11 PERST* (IPD)
ENET_CLKREQ_ISOL_L 12 CLKREQ* (OD)
ENET_WAKE_R_L 3 WAKE* (OD)
ENET_LOW_PWR 4 LOW_PWR (IPD)
BCM57765_SMB_CLK 6 SMB_CLK
BCM57765_SMB_DATA 10 SMB_DATA (IPD)
BCM57765_SCLK 66 SCLK_SPD1000LED*
BCM57765_MISO 64 SI/EEDATA
BCM57765_MOSI 65 SO_LINKLED*
BCM57765_CS_L 63 CS*/EECLK
(IPU)
TP_BCM57765_SPD100LED_L 2 SPD100LED*/SERIAL_DO (OD)
TP_BCM57765_TRAFFICLED_L 67 TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET 18 XTALI
ENET_CLK25M_XTALO 19 XTALO
BCM57765_RDAC 38 RDAC
THRM_PAD 69
NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.
TRD0_P 40 NC_ENET_MDI_P<0>
TRD0_N 41 NC_ENET_MDI_N<0>
TRD1_P 44 NC_ENET_MDI_P<1>
TRD1_N 43 NC_ENET_MDI_N<1>
TRD2_P 46 NC_ENET_MDI_P<2>
TRD2_N 47 NC_ENET_MDI_N<2>
TRD3_P 50 NC_ENET_MDI_P<3>
TRD3_N 49 NC_ENET_MDI_N<3>
GPIO_0/CR_ACT_LED* 5 NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 NC_ENET_MEDIA_SENSE
(IPx) SD_DETECT 1 SDCONN_DETECT
SDCONN_DETECT use high logic
CR_CMD 26 SDCONN_CMD
CR_CLK 21 SDCONN_ENET_CLK_R
R3981 0 5% 1/20W MF 201 SDCONN_CLK
CR_DATA0 25 SDCONN_DATA<0>
CR_DATA1 24 SDCONN_DATA<1>
CR_DATA2 23 SDCONN_DATA<2>
CR_DATA3 22 SDCONN_DATA<3>
CR_DATA4 52 SDCONN_DATA<4>
CR_DATA5 53 SDCONN_DATA<5>
CR_DATA6 54 SDCONN_DATA<6>
CR_DATA7 55 SDCONN_DATA<7>
MS_INS* 59 TP_CE_L_MS_INS_L
No MS (Memory Stick) Insert feature needed.
CR_LED*/CR_BUS_PWR 60 ENET_CR_PWREN
Control signal to light LED or control SD bus power.
CR_WP* 57 SDCONN_WP
SR_DISABLE 68 BDM57765_SR_DISABLE
R3980 1K 5% 1/20W MF 201
BCM57765 supports both active-levels for WP.
SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.
R3965 1.24K 1% 1/20W MF 201
May not need for SD-Only
Reccomended to keep footprint as backup
PHY Non-Volatile Memory
1MBIT ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Required for proper PHY operation.
PP3V3_ENET
U3990 M45PE10 SOIC ENET_ROM
VCC C S* W* RESET* VSS D Q
BCM57765_SCLK
BCM57765_CS_L
ENET_ROM C3990 0.1UF 10% 16V X5R-CERM 0201
BCM57765_MOSI
BCM57765_MISO
NOSTUFF R3990 4.7K 5% 1/20W MF 201
R3997 4.7K 5% 1/20W MF 201
NOTE: May remove U3990 after use OTP
NOTE: C I-V OTP requires SO pull-down instead of SI.
Caesar IV (ENET) 25MHz Crystal
ENET_CLK25M_XTALO
R3960 200 5% 1/16W MF-LF 402
BCM5764_CLK25M_XTALO_R
NO STUFF R3962 10M 5% 1/16W MF-LF 402
CRITICAL Y3960 25.0000M SM-3.2X2.5MM
NC NC
C3960 27PF 5% 50V CERM 402
C3961 27PF 5% 50V CERM 402
ENET_CLK25M_XTALI
SYSCLK_CLK25M_ENET
ENET_CLK25M_XTALI
MAKE_BASE=TRUE

SYNC_MASTER=K91_ERIC SYNC_DATE=10/11/2010

PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER SIZE D

REVISION

BRANCH

RIO cable will have pin 1 to pin 1 mapping from rev5!!!

CRITICAL

TO RIO FLEX

Flex Connector

516S0853

J4400

AXK732327G

F-ST-SM

			33				
7	OUT	SD_RESET_L	1	2	PM_SLP_S3_L	OUT	9 11 12 13
7	IN	SD_CLKREQ_L	3	4	PM_SLP_S4_L	OUT	10
11 7	OUT	SD_PWR_EN	5	6	HDMI_DDC_LS_CLK	OUT	12
7	IN	SDCONN_STATE_CHANGE	7	8	HDMI_DDC_LS_DATA	BI	12
10	IN	USB_EXTB_OC_L	9	10	HDMI_HPD_L	IN	9 12
12 5		PP1V5_S0	11	12			
			13	14			
12 11 7 5 4		PP3V3_S3	15	16			
13 12 7 5 4		PP3V3_S4	17	18			
12 9		I2C_HDMIRDRV_SCL_CONN	19	20			
12 9		I2C_HDMIRDRV_SDA_CONN	21	22			
			23	24			
			25	26			
			27	28	PP5V_S4		4 5 9 10 13
13 10 9 5 4		PP5V_S4	29	30			
			31	32			
				34			

12 9	I2C_HDMIRDRV_SCL_CONN	MAKE_BASE=TRUE	=	I2C_HDMIRDRV_SCL_CONN	9 12
12 9	I2C_HDMIRDRV_SDA_CONN	MAKE_BASE=TRUE	=	I2C_HDMIRDRV_SDA_CONN	9 12
12 9	HDMI_HPD_L	MAKE_BASE=TRUE	=	HDMI_HPD_L	9 12

13 12 11 9 PM_SLP_S3_L

R4400 1

750K 5% 1/20W MF 201 2

NOSTUFF

B4401 BEAD-PROBE SM 1

14 10 9 4 USB3_EXTB_TX_P

B4402 BEAD-PROBE SM 1

14 10 9 4 USB3_EXTB_TX_N

B4403 BEAD-PROBE SM 1

14 10 9 4 USB3_EXTB_RX_P

B4404 BEAD-PROBE SM 1

14 10 9 4 USB3_EXTB_RX_N

B4405 BEAD-PROBE SM 1

14 12 9 4 HDMI_DATA_C_P<0>

B4406 BEAD-PROBE SM 1

14 12 9 4 HDMI_DATA_C_N<0>

B4407 BEAD-PROBE SM 1

HDMI_DATA_C_P<1>

14 12 9 4

B4408 BEAD-PROBE SM 1

14 12 9 4 HDMI_DATA_C_N<1>

B4409 BEAD-PROBE SM 1

14 12 9 4 HDMI_DATA_C_P<2>

B4410 BEAD-PROBE SM 1

14 12 9 4 HDMI_DATA_C_N<2>

CRITICAL

Coax Connector

518S0829

J4410

20525-130E-01

F-RT-SM

			31				
14 10	BI	USB_EXTB_P	1	2	USB_EXTB_N	BI	14 10
14 10 9 4	OUT	USB3_EXTB_TX_P	3	4	GND_VOID=TRUE		
14 10 9 4	OUT	USB3_EXTB_TX_N	5	6	GND_VOID=TRUE		
14 10 9 4	IN	USB3_EXTB_RX_P	7	8	GND_VOID=TRUE		
14 10 9 4	IN	USB3_EXTB_RX_N	9	10	GND_VOID=TRUE		
14 12 9 4	OUT	HDMI_DATA_C_P<0>	11	12	GND_VOID=TRUE		
14 12 9 4	OUT	HDMI_DATA_C_N<0>	13	14	GND_VOID=TRUE		
14 12 9 4	OUT	HDMI_DATA_C_P<1>	15	16	GND_VOID=TRUE		
14 12 9 4	OUT	HDMI_DATA_C_N<1>	17	18	GND_VOID=TRUE		
14 12 9 4	OUT	HDMI_DATA_C_P<2>	19	20	GND_VOID=TRUE		
14 12 9 4	OUT	HDMI_DATA_C_N<2>	21	22	GND_VOID=TRUE		
14 12	OUT	HDMI_CLK_C_LS_P	23	24			
14 12	OUT	HDMI_CLK_C_LS_N	25	26			
14 8	OUT	PCIE_CLK100M_ENET_P	27	28			
14 8	OUT	PCIE_CLK100M_ENET_N	29	30			
14 8	IN	PCIE_ENET_D2R_P	33	34			
14 8	IN	PCIE_ENET_D2R_N	35	36			
14 8	OUT	PCIE_ENET_R2D_C_P	37	38			
14 8	OUT	PCIE_ENET_R2D_C_N	39	40			
			41				
				32			

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: RIO CONNECTORS

Apple Inc.

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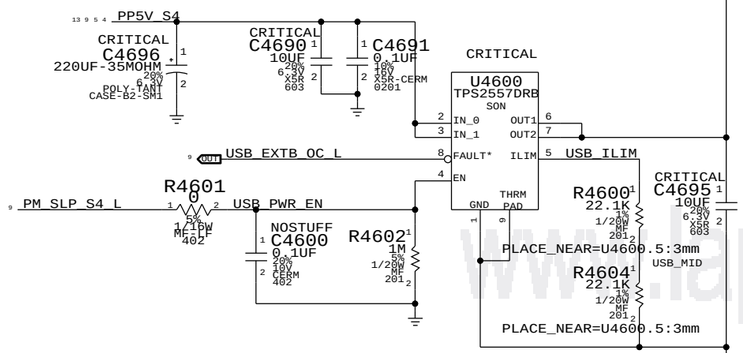
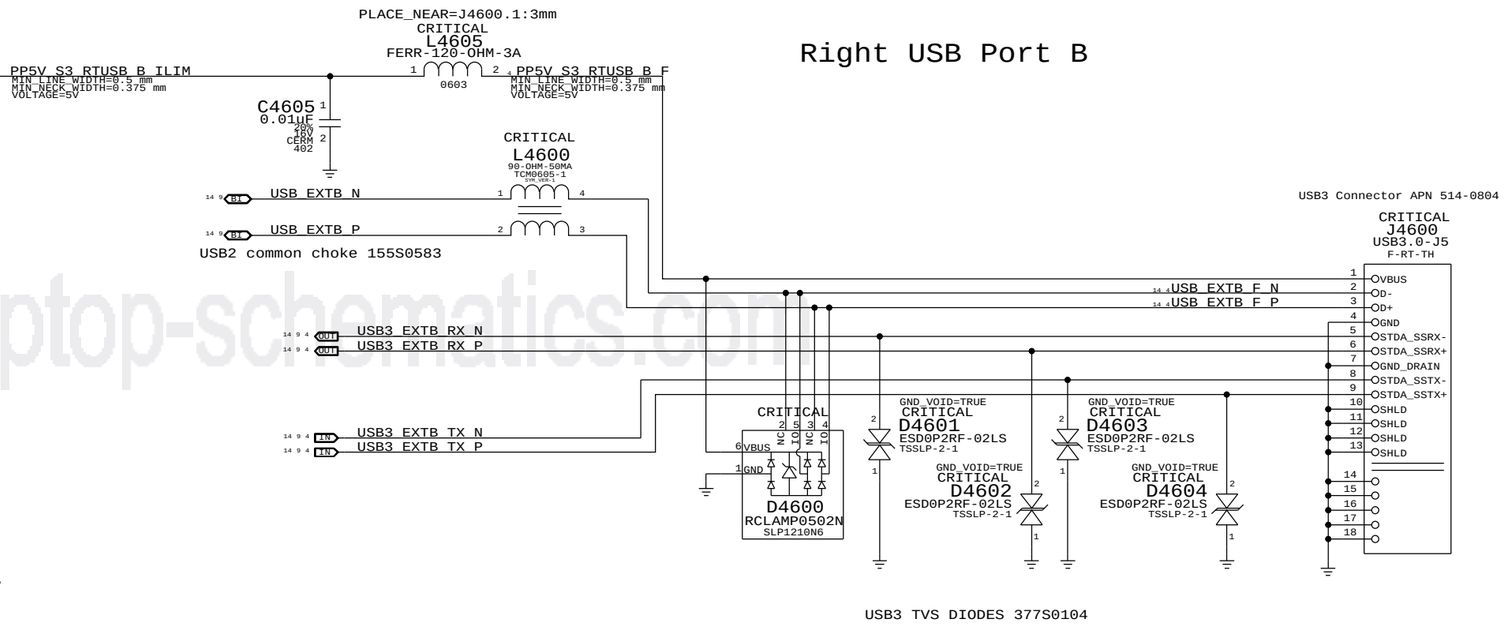
USB Port Power Switch



Right USB Port B



USB3 TVS DIODES 377S0104

Current limit per port (R4600+R4604): 2.19A min / 2.76A max
U4600 Port C is deleted, only keep dummy USBC connector for PD

SYNC_MASTER=RIO_BEN SYNC_DATE=07/01/2011

PAGE TITLE: External USB Connectors

Apple Inc.

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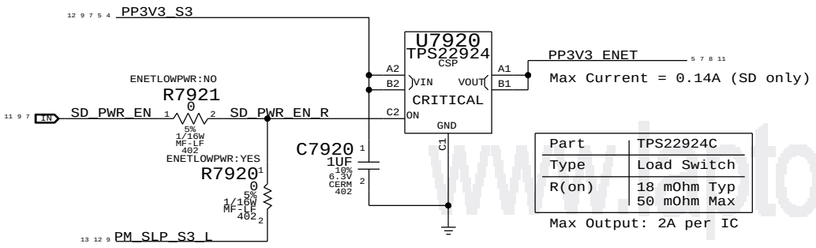
State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

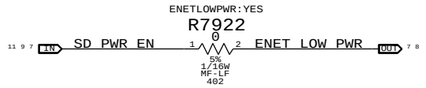
3.3V ENET Switch



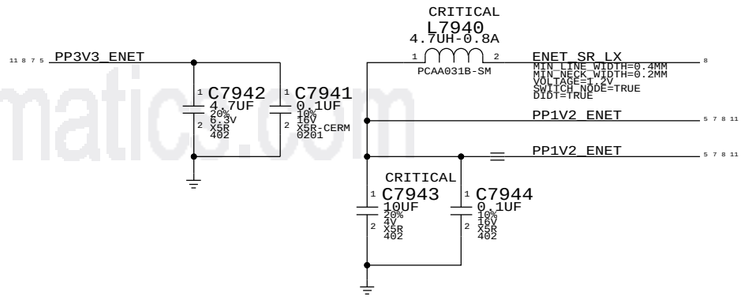
Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

Stuff R7920 & R7921 force ENET switch always on
and connect ENET_LOW_PWR to GPIO instead



CAESAR IV 1.2V INT.VR CMPTS



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

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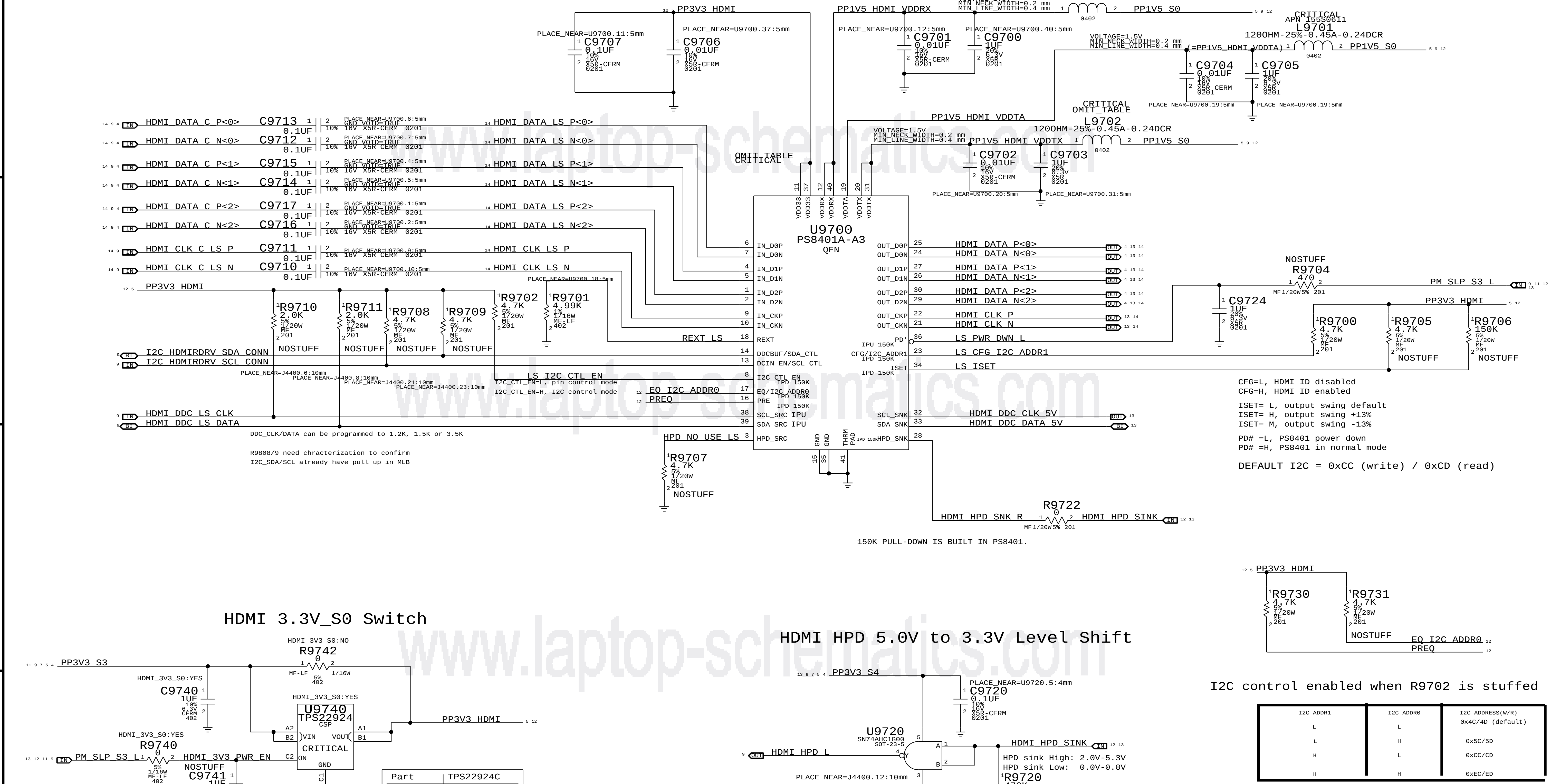
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0731	2	FERR BD,60mOHM, 0402	L9700,L9702	CRITICAL	
338S1089	1	HDMI REPEATER - A3	U9700	CRITICAL	



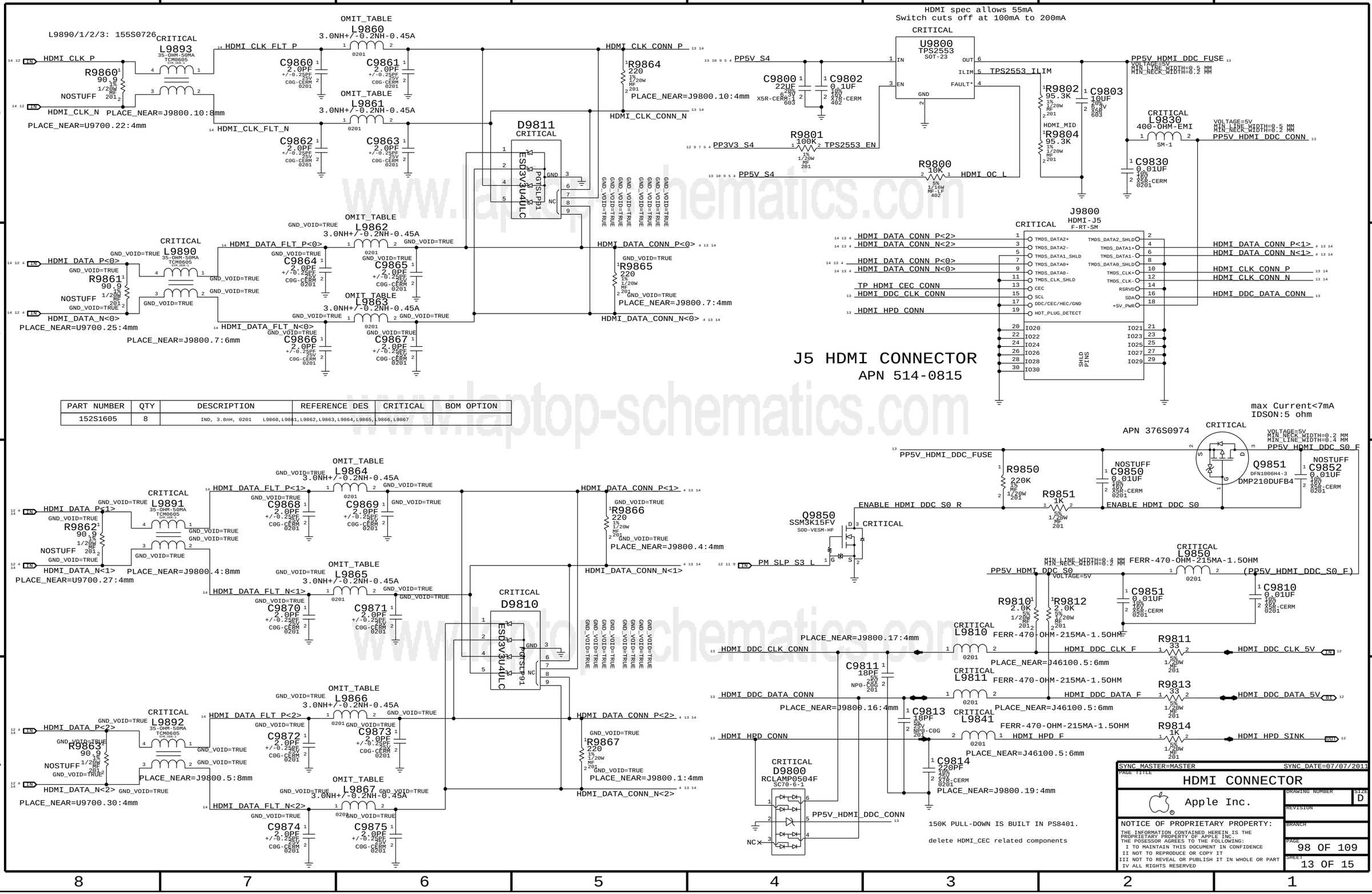
SYNC_MASTER=MASTER SYNC_DATE=07/07/2011

PAGE TITLE: HDMI SHIFTER

Apple Inc.

DRAWING NUMBER | SIZE D

NOTICE OF PROPRIETARY PROPERTY:



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S1605	8	IND, 3.8nH, 0201 L9860,L9861,L9862,L9863,L9864,L9865,L9866,L9867			

SYNC_MASTER=MASTER SYNC_DATE=07/07/2011

PAGE TITLE: HDMI CONNECTOR

Apple Inc.

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HDMI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDMI	TOP,BOTTOM	=5X_DIELECTRIC	?
HDMI	ISL3,ISL5,ISL6	=4X_DIELECTRIC	?

SOURCE: AMD/NV CONSTRAINS

PCIE Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	0.381 MM	?
PCIE	*	0.381 MM	?
CLK_PCIE	*	0.508 MM	?

SOURCE: J5 MLB

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	0.381 MM	?
USB	*	0.381 MM	?

SOURCE: Intel document 467283

USB 3.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	0.381 MM	?
USB3	ISL3,ISL5,ISL6	=4X_DIELECTRIC	?

SOURCE: Intel document 467283

CAESAR IV (SD) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_DATA	*	8 MIL	?

SOURCE: K90i

USB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	DIFF PAIR	
USB_EXTB	USB_85D	USB	USB_EXTB	USB_EXTB_P 9 10
	USB_85D	USB	USB_EXTB	USB_EXTB_N 9 10
USB3_EXTB_TX	USB3_85D	USB3	USB_EXTB_TX	USB3_EXTB_TX_P 4 9 10
	USB3_85D	USB3	USB_EXTB_TX	USB3_EXTB_TX_N 4 9 10
USB3_EXTB_RX	USB3_85D	USB3	USB_EXTB_RX	USB3_EXTB_RX_P 4 9 10
	USB3_85D	USB3	USB_EXTB_RX	USB3_EXTB_RX_N 4 9 10
USB_EXTB	USB_85D	USB	USB_EXTC	USB_EXTB_F_P 4 10
	USB_85D	USB	USB_EXTC	USB_EXTB_F_N 4 10
USB3_EXTB_TX	USB3_85D	USB3	USB_EXTC_TX	USB3_EXTB_TX_F_P 4
	USB3_85D	USB3	USB_EXTC_TX	USB3_EXTB_TX_F_N 4
USB3_EXTB_RX	USB3_85D	USB3	USB_EXTC_RX	USB3_EXTB_RX_F_P 4
	USB3_85D	USB3	USB_EXTC_RX	USB3_EXTB_RX_F_N 4

PCIE Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_P 8
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_N 8
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P 8 9
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N 8 9
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P 8 9
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N 8 9
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P 8
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N 8
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P 8 9
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N 8 9

HDMI Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
HDMI_DATA_LS	HDMI_90D	HDMI	HDMI_DATA_C_P<2..0> 4 9 12
HDMI_DATA_LS	HDMI_90D	HDMI	HDMI_DATA_C_N<2..0> 4 9 12
HDMI_CLK_LS	HDMI_90D	HDMI	HDMI_CLK_C_LS_P 9 12
HDMI_CLK_LS	HDMI_90D	HDMI	HDMI_CLK_C_LS_N 9 12
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_P<2..0> 4 12 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_N<2..0> 4 12 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_P 12 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_N 12 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_CONN_P<2..0> 4 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_CONN_N<2..0> 4 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_CONN_P 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_CONN_N 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_LS_P<2..0> 12
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_LS_N<2..0> 12
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_LS_P 12
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_LS_N 12
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_FLT_P<2..0> 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA_FLT_N<2..0> 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_FLT_P 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK_FLT_N 13

SD Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
CR_DATA	ENET_50S	SD_DATA	SDCONN_DATA<7..0> 7 8
CR_DATA	ENET_50S	SD_DATA	SDCONN_CMD 7 8
CR_CLK	ENET_50S	SD_DATA	SDCONN_CLK 7 8
CR_DATA	ENET_50S	SD_DATA	SDCONN_R_DATA<7..0> 7
CR_DATA	ENET_50S	SD_DATA	SDCONN_CMD_R 7
CR_CLK	ENET_50S	SD_DATA	SDCONN_CLK_R 7
CR_CLK	ENET_50S	SD_DATA	SDCONN_ENET_CLK_R 8

SYNC_MASTER=K92_YUN SYNC_DATE=06/25/2010

PAGE TITLE: PCH Constraints 1

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RIO (J5) Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.110 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3	Y	0.085 MM	0.085 MM			
50_OHM_SE	ISL5,ISL6	Y	0.115 MM	0.115 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL3	Y	0.101 MM	0.101 MM		0.140 MM	0.140 MM
85_OHM_DIFF	ISL5,ISL6	Y	0.118 MM	0.118 MM		0.130 MM	0.130 MM

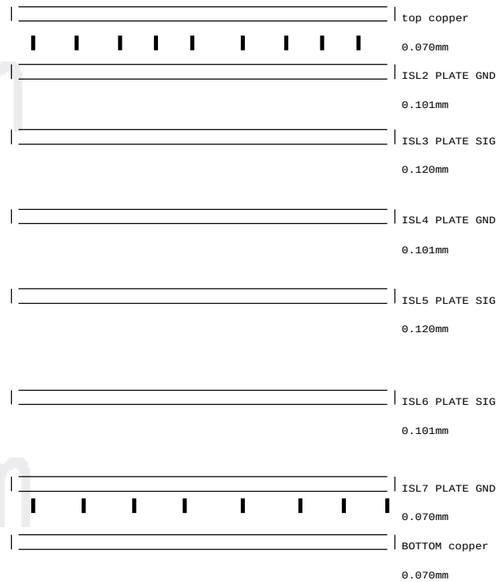
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.130 MM	0.130 MM
90_OHM_DIFF	ISL3	Y	0.092 MM	0.092 MM		0.160 MM	0.160 MM
90_OHM_DIFF	ISL5,ISL6	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP,BOTTOM	0.070 MM	?
1X_DIELECTRIC	ISL3	0.120 MM	?
1X_DIELECTRIC	ISL5	0.120 MM	?
1X_DIELECTRIC	ISL6	0.120 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
3X_DIELECTRIC	ISL3,ISL5,ISL6	0.360 MM	?
4X_DIELECTRIC	ISL3,ISL5,ISL6	0.480 MM	?

HDMI_keepout should be 1.016mm. Howerver use 0.3mm per layout restriction
HDMI_spacing should be 0.635mm. Howerver use 0.3mm per layout restriction

NOTE: Based on RIO (J5) stackup 08/26/11.



SYNC_MASTER=K17_MLB SYNC_DATE=05/14/2010

PAGE TITLE: PCB Rule Definitions

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