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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM, MLB, D1

8/8/12

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9216	1	SCHEM, MLB, D1	SCH	CRITICAL	
820-3462	1	PCBF, MLB (NEW), D1	PCB	CRITICAL	

DRAWING
 TITLE=MLB
 ABBREV=ABBREV
 PART_MODIFIED_BY=THU 9/12/11 10:09 2012

DRAWING TITLE		SCHEM, MLB, D1	
Apple Inc.	DRAWING NUMBER	<SCH_NUM>	SIZE
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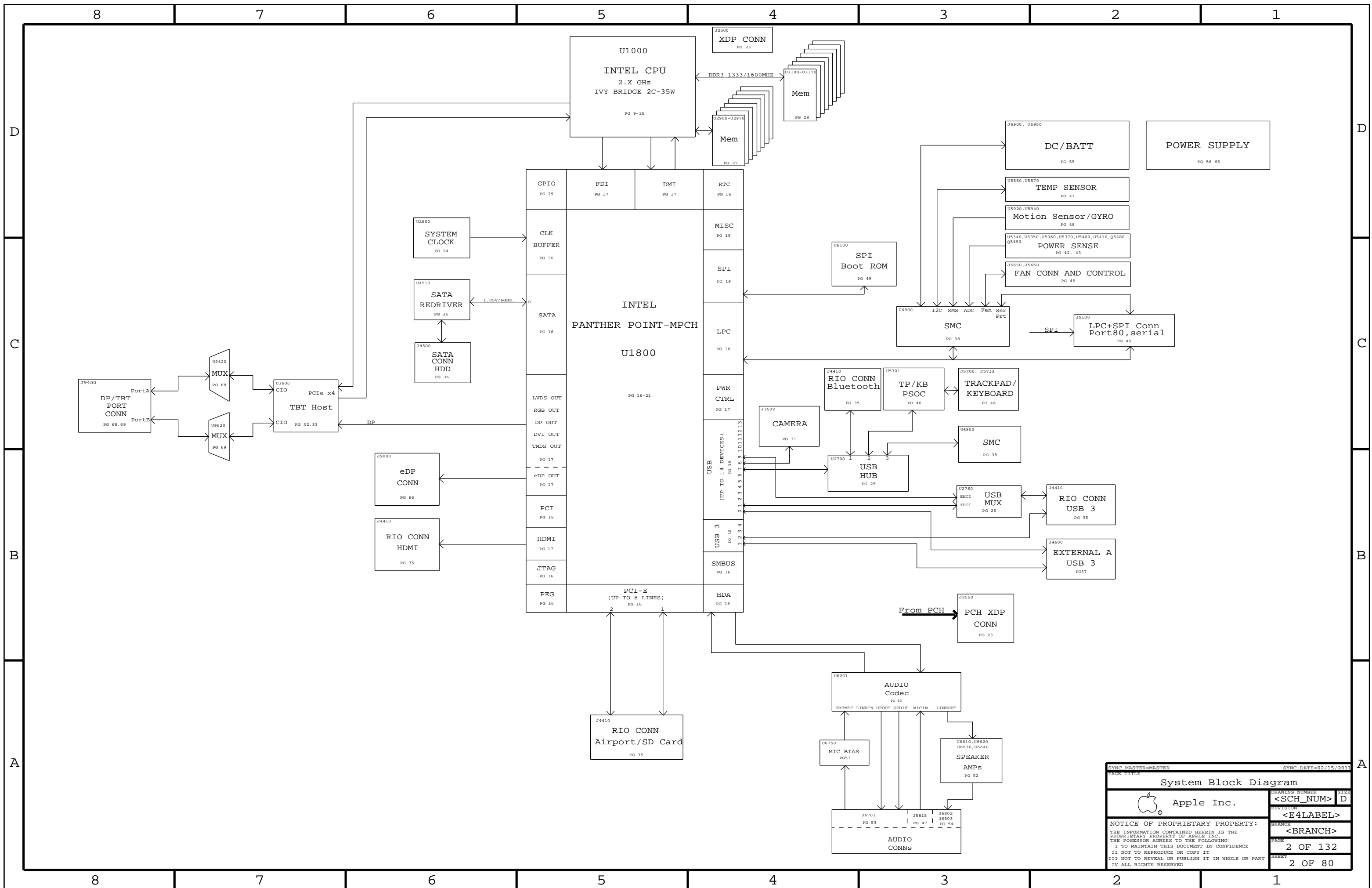
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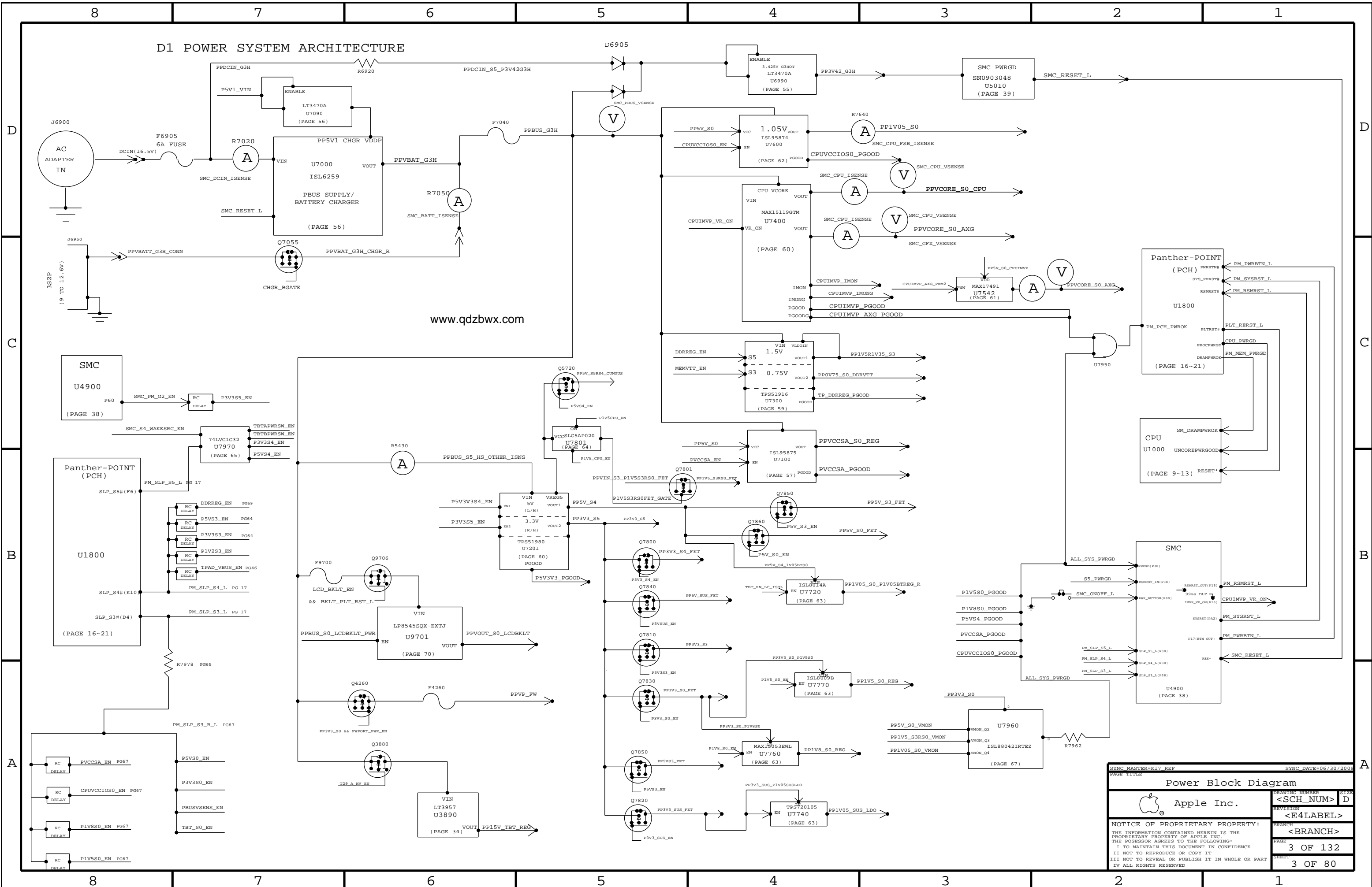
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D1 POWER SYSTEM ARCHITECTURE



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BOM Variants

Table with columns: BOM NUMBER, BOM NAME, BOM OPTIONS. Lists various BOM variants and their options.

Bar Code Labels / EEE #'s

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists bar code labels and their specifications.

Alternate Parts

Table with columns: PART NUMBER, ALTERNATE FOR PART NUMBER, BOM OPTION, REF DES, COMMENTS. Lists alternate parts for various BOM options.

Module Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists module parts and their specifications.

D1 BOM GROUPS

Table with columns: BOM GROUP, BOM OPTIONS. Lists D1 BOM groups and their options.

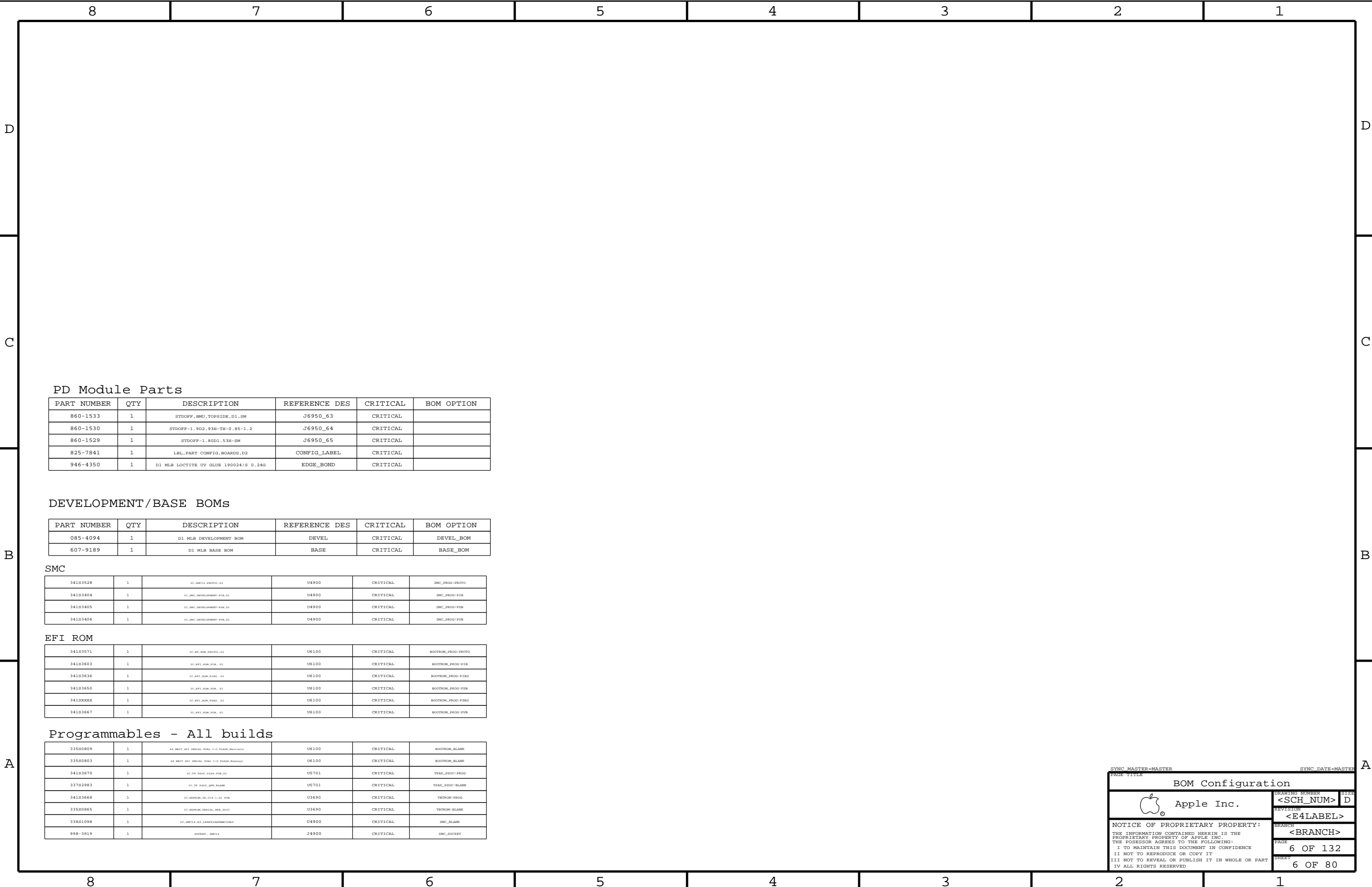
DDR3 SPD STRAPPINGS

Table with columns: BOM GROUP, BOM OPTIONS. Lists DDR3 SPD strappings and their options.

Module Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists module parts and their specifications.

BOM Configuration box containing Apple Inc. logo, drawing number, revision, and a notice of proprietary property.



PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1533	1	STDOFF, BMU, TOPSIDE, D1, SM	J6950_63	CRITICAL	
860-1530	1	STDOFF-1.9D2.93H-TW-0.85-1.2	J6950_64	CRITICAL	
860-1529	1	STDOFF-1.80D1.53H-SM	J6950_65	CRITICAL	
825-7841	1	LBL, PART CONFIG, BOARDS, D2	CONFIG_LABEL	CRITICAL	
946-4350	1	D1 MLB LOCTITE UV GLUE 180024/S 0.24G	EDGE_BOND	CRITICAL	

DEVELOPMENT/BASE BOMS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4094	1	D1 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9189	1	D1 MLB BASE BOM	BASE	CRITICAL	BASE_BOM

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
34183528	1	00_SMC12_PROD00_01	U4900	CRITICAL	SMC_PROD00
34183404	1	00_SMC_DEVELOPMENT_P1B_01	U4900	CRITICAL	SMC_PROD_P1B
34183405	1	00_SMC_DEVELOPMENT_P1B_01	U4900	CRITICAL	SMC_PROD_P1B
34183406	1	00_SMC_DEVELOPMENT_P1B_01	U4900	CRITICAL	SMC_PROD_P1B

EFI ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
34183571	1	00_EFI_ROM_PROD00_01	U6100	CRITICAL	BOOTROM_PROD00
34183603	1	00_EFI_ROM_P1B_01	U6100	CRITICAL	BOOTROM_PROD_P1B
34183636	1	00_EFI_ROM_P1B2_01	U6100	CRITICAL	BOOTROM_PROD_P1B2
34183650	1	00_EFI_ROM_P1B_01	U6100	CRITICAL	BOOTROM_PROD_P1B
3418XXXX	1	00_EFI_ROM_P1B2_01	U6100	CRITICAL	BOOTROM_PROD_P1B2
34183667	1	00_EFI_ROM_P1B_01	U6100	CRITICAL	BOOTROM_PROD_P1B

Programmables - All builds

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33580809	1	64 MBIT SPI SERIAL SERIAL 1/0 FLASH_MEMORY	U6100	CRITICAL	BOOTROM_BLANK
33580803	1	64 MBIT SPI SERIAL SERIAL 1/0 FLASH_MEMORY	U6100	CRITICAL	BOOTROM_BLANK
34183670	1	00_TP_PROD_V224_P1B_01	U5701	CRITICAL	TPAD_PROD_PROD
33782983	1	00_TP_PROD_QFN_BLANK	U5701	CRITICAL	TPAD_PROD_BLANK
34183668	1	00_TSTRON_CK_V14_1_01_P1B	U3690	CRITICAL	TSTRON_PROD
33580865	1	00_TSTRON_SERIAL_BOM_8010	U3690	CRITICAL	TSTRON_BLANK
33881098	1	00_SMC12-AS_LANVLANASSEMBLY	U4900	CRITICAL	SMC_BLANK
998-3919	1	SOCKET, SMC12	J4900	CRITICAL	SMC_SOCKET

SYNC MASTER=MASTER SYNC DATE=MASTER

BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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Functional Test Points

Table of functional test points including headers like J5650 (LEFT FAN CONN), J5660 (RIGHT FAN CONN), J3502 (ALS/CAMERA CONN), J4400 (RIO CABLE CONN), J4410 (RIO FLEX CONN), J4900 (CHAR2 TPS), J6701 (AUDIO JACK CONN), J6802 (AUDIO LEFT SPEAKER CONN), J6803 (AUDIO RIGHT SPEAKER CONN), J6950 (MAIN BATT CONN), J6801 (2 MIC CONN), J3401 & J3402 (AIRPORT/BT/CAMERA CONN), and J4600 (LEFT USB CONN).

POWER RAILS

Table of power rails including headers like J5713 (KEY BOARD CONN), J5700 (1PD FLEX CONN), J6900 (DC POWER CONN), and J5100 (LPC + SPI CONN).

ICT Test Points

Table of ICT test points including headers like J5713 (KEY BOARD CONN), J5700 (1PD FLEX CONN), J6900 (DC POWER CONN), and J5100 (LPC + SPI CONN).

NC NO_TESTS

Table of NC NO_TESTS including headers like CPU_NO_TESTS, NC TBT MONDC0, NC DP TBTSRC ML CP<3>, NC DP TBTSRC ML CN<3>, NC DP TBTSRC ML CP<2>, NC DP TBTSRC ML CN<2>, NC DP TBTSRC ML CP<1>, NC DP TBTSRC ML CN<1>, NC DP TBTSRC ML CP<0>, NC DP TBTSRC ML CN<0>, NC DP TBTSRC AUXCH CP, NC DP TBTSRC AUXCH CN, NC SPT CSI L, NC PCH GPIO8, NC PCH STRP BBS1, NC PCH STRP ESI L, NC PCH TP23, NC PCI CLK33M OUT2, NC PCI CLK100M PEGAN, NC PCI CLK100M PEGAP, NC PM SLP A L, NC PPOVOUT PCH DCPUSUBYP, NC SMC MEM5 LED PWR, NC SMC MEM5 LED CHG, NC SMS INT2, NC MEM A DO<0>, NC MEM A DO<12..2>, NC MEM A DO<19..14>, NC MEM A DO<24..21>, NC MEM A DO<32..26>, NC MEM A DO<42..34>, NC MEM A DO<54..44>, NC MEM A DO<63..58>, NC MEM B DO<2..0>, NC MEM B DO<13..4>, NC MEM B DO<19..15>, NC MEM B DO<25..21>, NC MEM B DO<35..27>, NC MEM B DO<40..37>, NC MEM B DO<47..42>, NC MEM B DO<57..49>, NC MEM B DO<63..59>, NC MEM EVENT L, NC SDVO TVCLKINN, NC SDVO TVCLKINP, NC SDVO STALLN, NC SDVO STALLP, NC SDVO INTN, NC SDVO INTP, NC PCI PME L, NC PCI CLK33M OUT3, NC ISNS LCDBKLT, NC ISNS WLANN, NC ISNS WLANN, NC ISNS LCD PANELN, NC XDP PCH HOOK4, NC XDP PCH HOOK5, NC XDP PCH OBSFN B<0>, NC XDP PCH OBSFN B<1>, NC XDP PCH OBSFN A<0>, NC XDP PCH OBSFN A<1>, NC XDP PCH OBSFN D<0>, NC XDP PCH OBSFN D<1>, NC IV05 S0 PCH VCCAPLLEXP, NC AUD CODEC MICBIAS, NC AUD MIC INRP, NC AUD MIC INRN, NC BKL FAULT, NC LPC DREQ0 L.

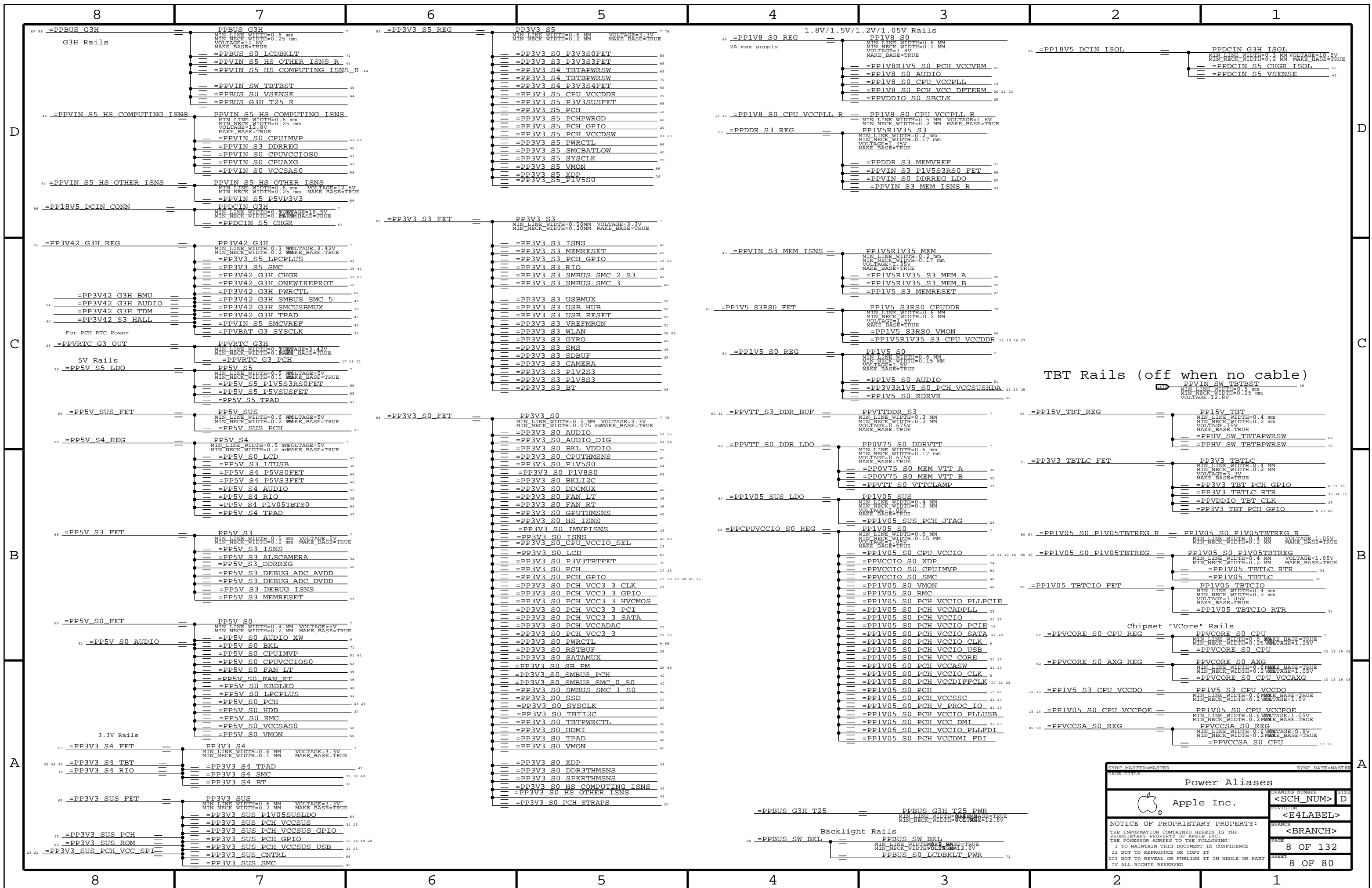
S2 CAMERA PCIE SIGNALS

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PCIE ENET R2D C P

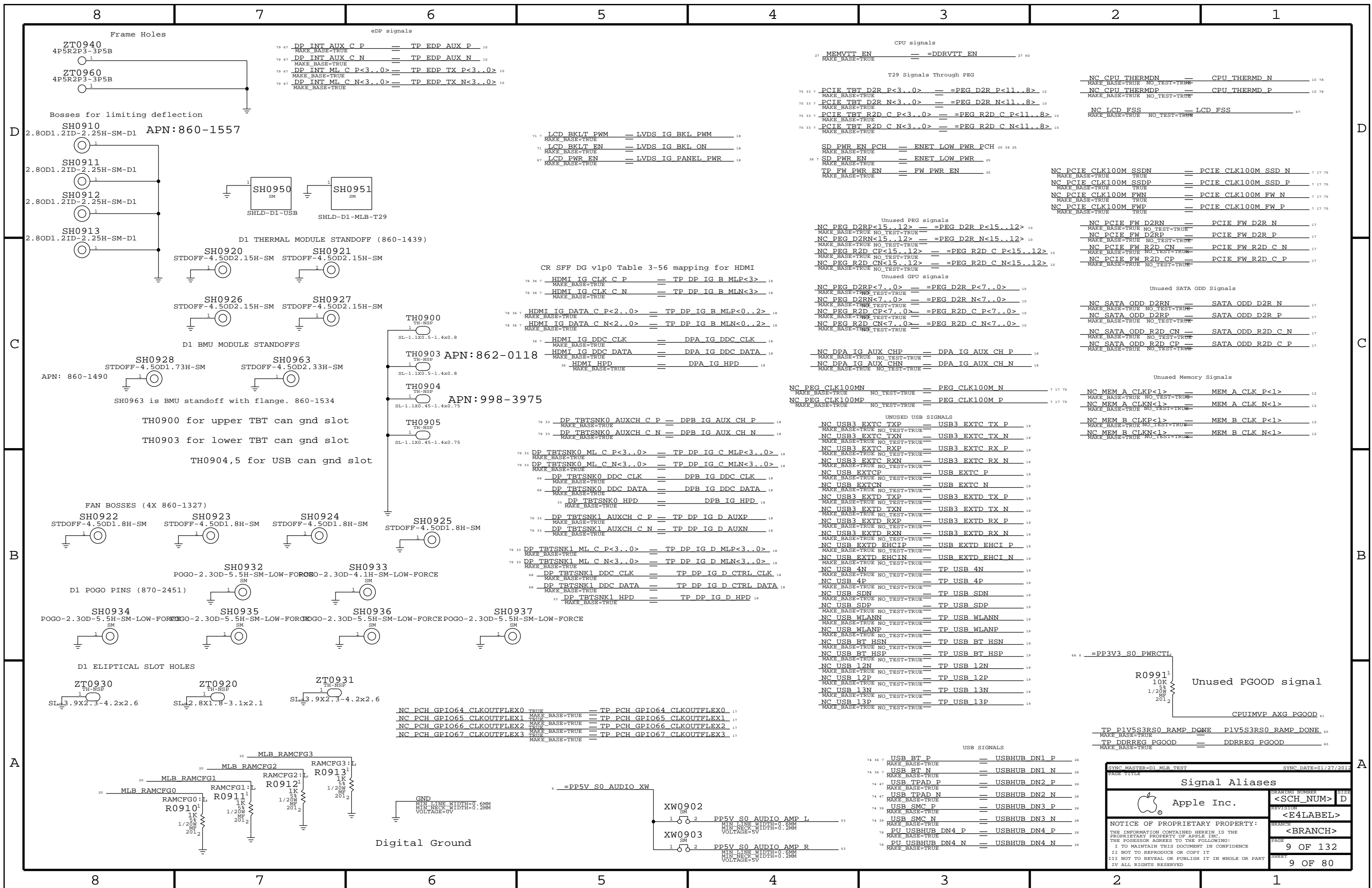
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Functional / ICT Test header with Apple logo, project title, drawing number, revision, and branch information. Includes a notice of proprietary property and page numbers (7 OF 132, 7 OF 80).



TBT Rails (off when no cable)

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Power Aliases		DRAWING NUMBER	SIZE
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NC CPU THERMDN CPU THERMD N

NC CPU THERMDP CPU THERMD P

NC LCD FSS LCD FSS

NC PCIE CLK100M SSDN PCIE CLK100M SSD N

NC PCIE CLK100M SSDP PCIE CLK100M SSD P

NC PCIE CLK100M FWN PCIE CLK100M FW N

NC PCIE CLK100M FWP PCIE CLK100M FW P

NC PCIE FW D2RN PCIE FW D2R N

NC PCIE FW D2RP PCIE FW D2R P

NC PCIE FW R2D CN PCIE FW R2D C N

NC PCIE FW R2D CP PCIE FW R2D C P

NC SATA ODD D2RN SATA ODD D2R N

NC SATA ODD D2RP SATA ODD D2R P

NC SATA ODD R2D CN SATA ODD R2D C N

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NC USB EXTCP USB EXTC P

NC USB EXTCPN USB EXTC N

NC USB3 EXTD TXP USB3 EXTD TX P

NC USB3 EXTD TXN USB3 EXTD TX N

NC USB3 EXTD RXP USB3 EXTD RX P

NC USB3 EXTD RXN USB3 EXTD RX N

NC USB EXTD EHCIP USB EXTD EHCI P

NC USB EXTD EHCIN USB EXTD EHCI N

NC USB 4N TP USB 4N

NC USB 4P TP USB 4P

NC USB SDN TP USB SDN

NC USB SDP TP USB SDP

NC USB WLANN TP USB WLANN

NC USB WLANP TP USB WLANP

NC USB BT HSN TP USB BT HSN

NC USB BT HSP TP USB BT HSP

NC USB 12N TP USB 12N

NC USB 12P TP USB 12P

NC USB 13N TP USB 13N

NC USB 13P TP USB 13P

TP P1V5S3RS0 RAMP DONE P1V5S3RS0 RAMP DONE

TP DDRREG PGOOD DDRREG PGOOD

SYNC MASTER=D1 MLB TEST SYNC DATE=01/27/2012

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Signal Aliases

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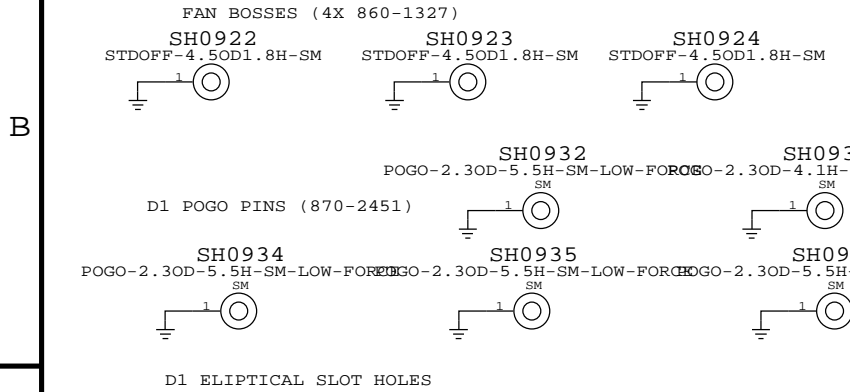
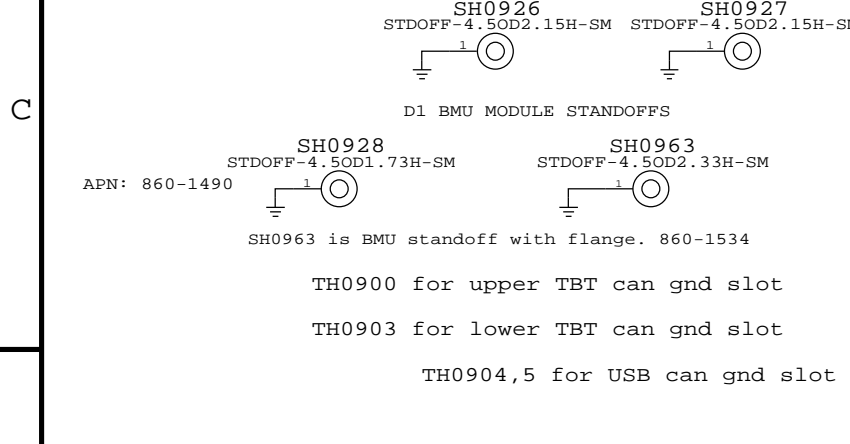
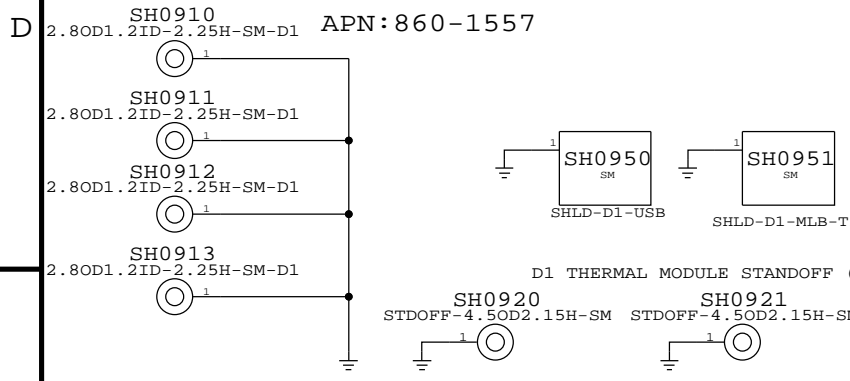
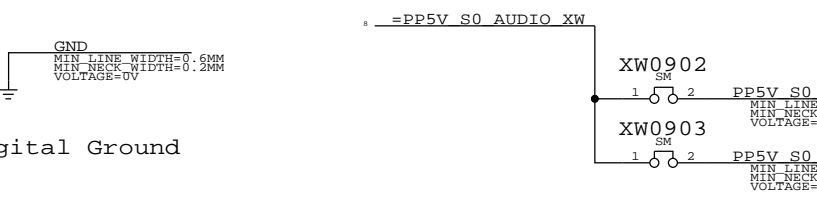
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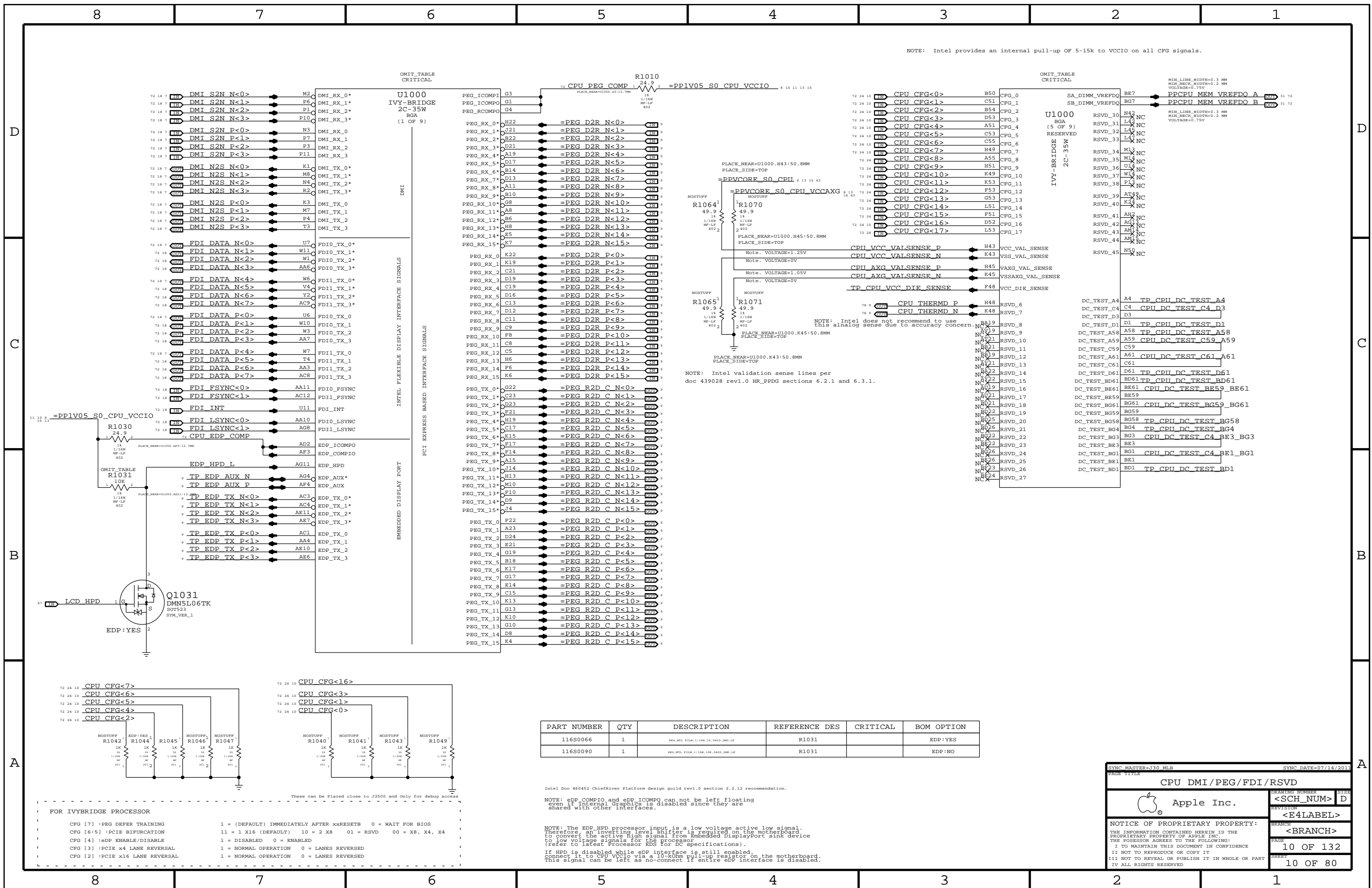
NC PCH GPIO64 CLKOUTFLEX0 TP PCH GPIO64 CLKOUTFLEX0

NC PCH GPIO65 CLKOUTFLEX1 TP PCH GPIO65 CLKOUTFLEX1

NC PCH GPIO66 CLKOUTFLEX2 TP PCH GPIO66 CLKOUTFLEX2

NC PCH GPIO67 CLKOUTFLEX3 TP PCH GPIO67 CLKOUTFLEX3





NOTE: Intel provides an internal pull-up of 5-15k to VCCIO on all CFG signals.

OMIT_TABLE
CRITICAL

OMIT_TABLE
CRITICAL

MIN_LINE_WIDTH=0.3 MM
MIN_SPACE_WIDTH=0.2 MM
VOLTAGE=0.75V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL,1206,1/16W,1%,5402,090,LF	R1031		EDP:YES
116S0090	1	RES,MTL,1206,1/16W,1%,5402,090,LF	R1030		EDP:NO

Intel Doc 460452 ChiefRiver Platform design guild rev1.0 section 2.2.12 recommendation.

NOTE: edp_COMPIO and edp_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

Note: The EDP HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).
If HPD is disabled while EDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire EDP interface is disabled.

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be Placed close to J2500 and Only for debug access

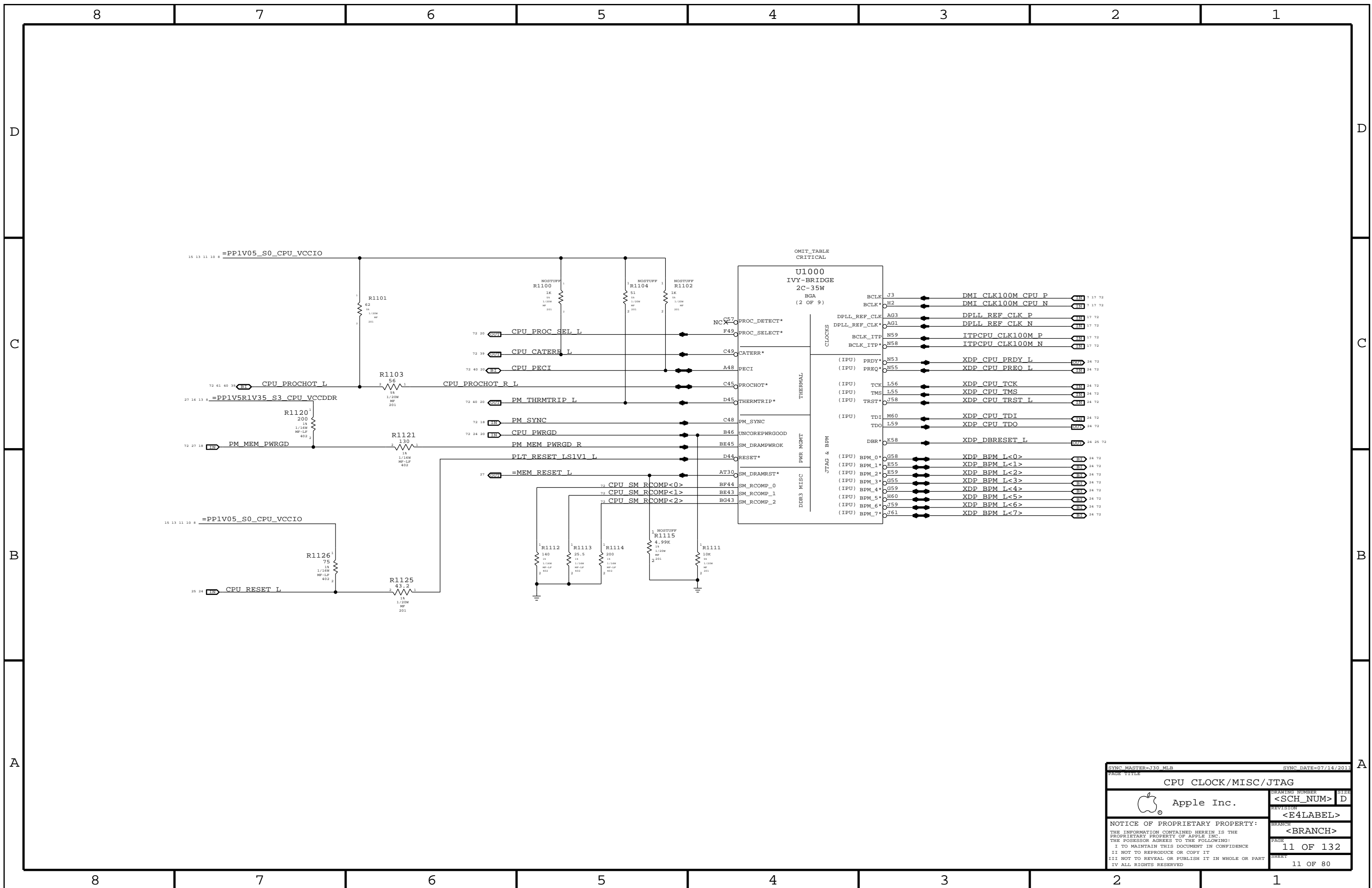
SYNC MASTER=J30 MLB SYNC DATE=07/14/2011

CPU DMI / PEG / FDI / RSVD

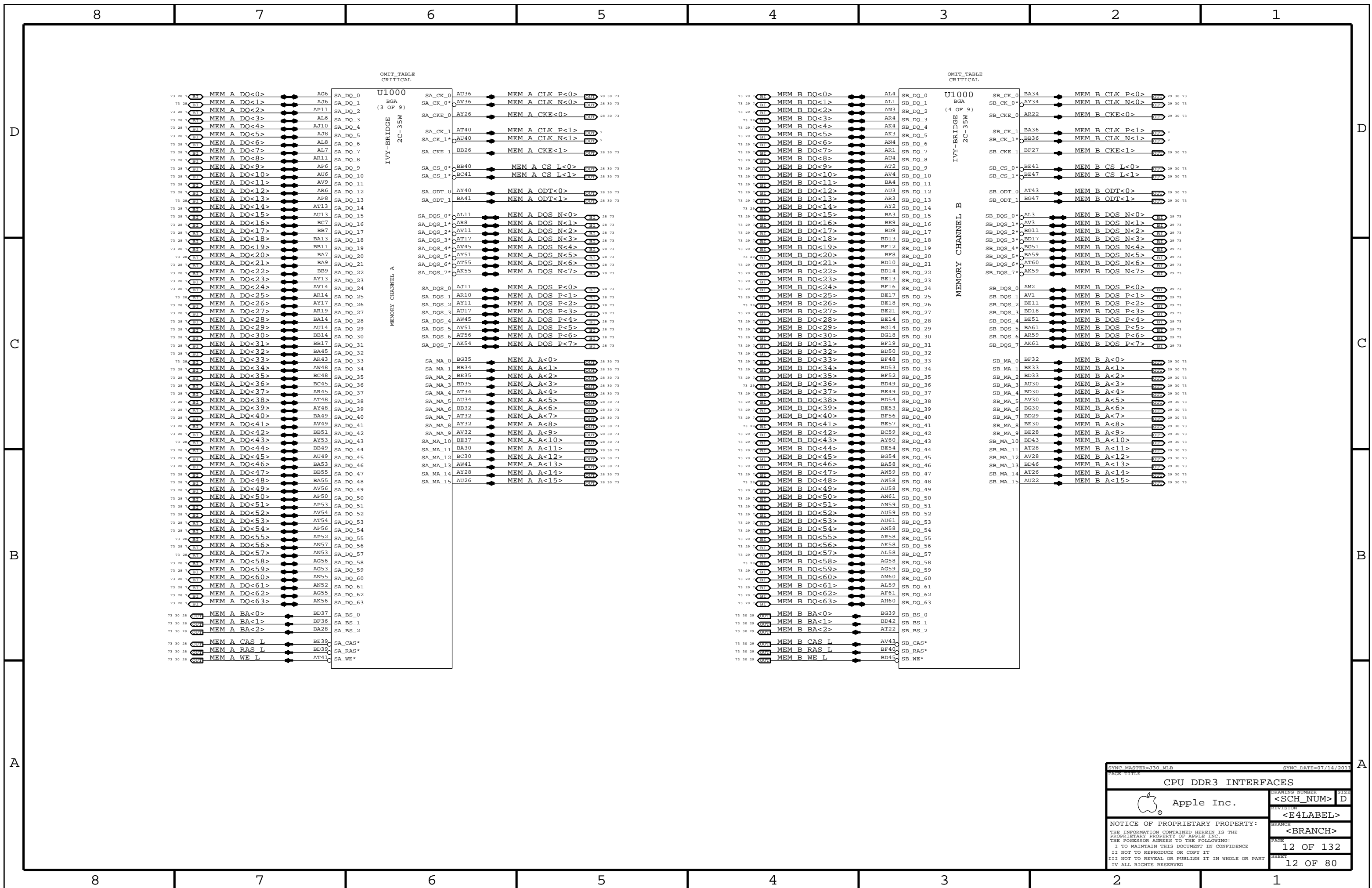
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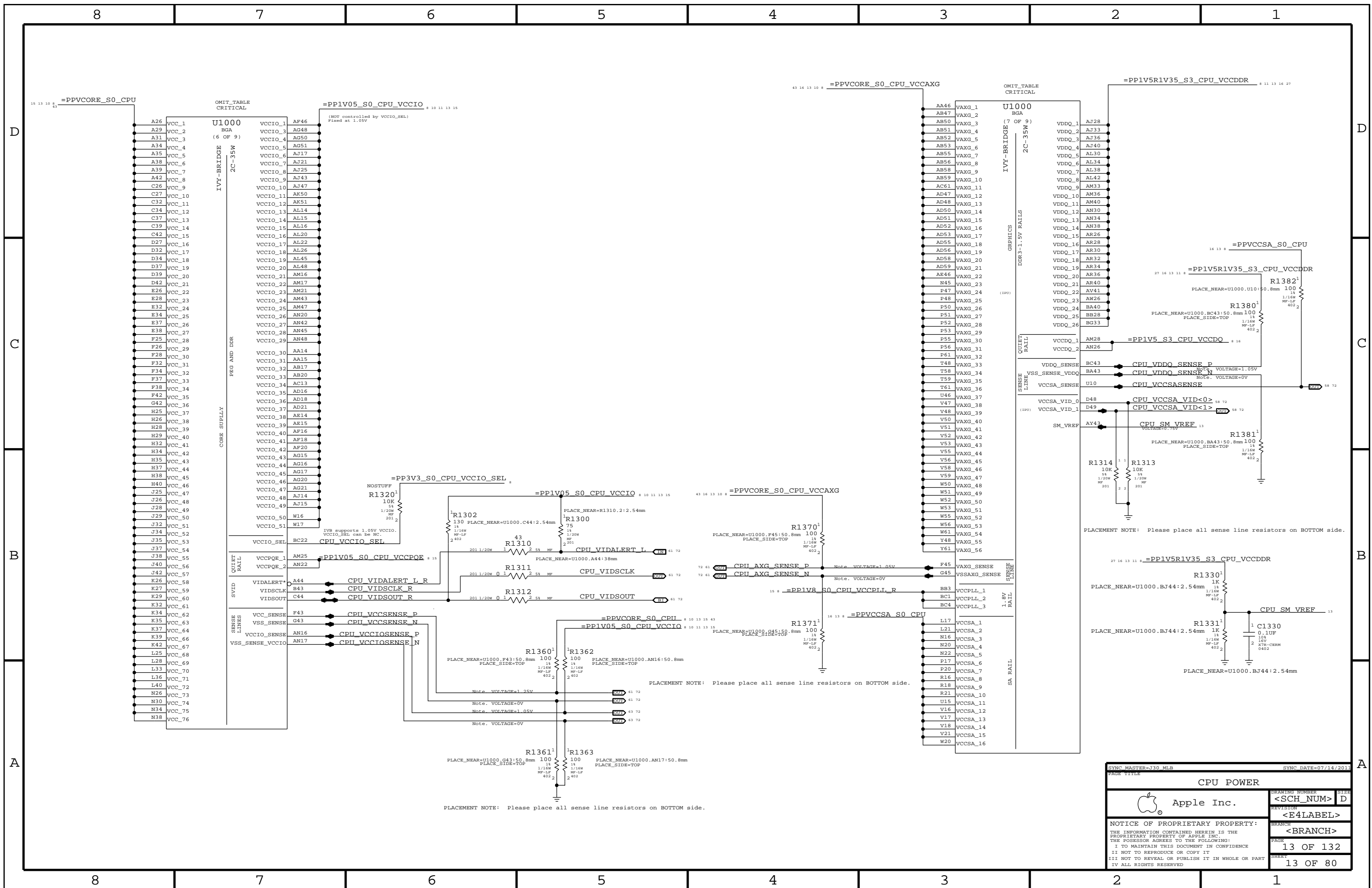
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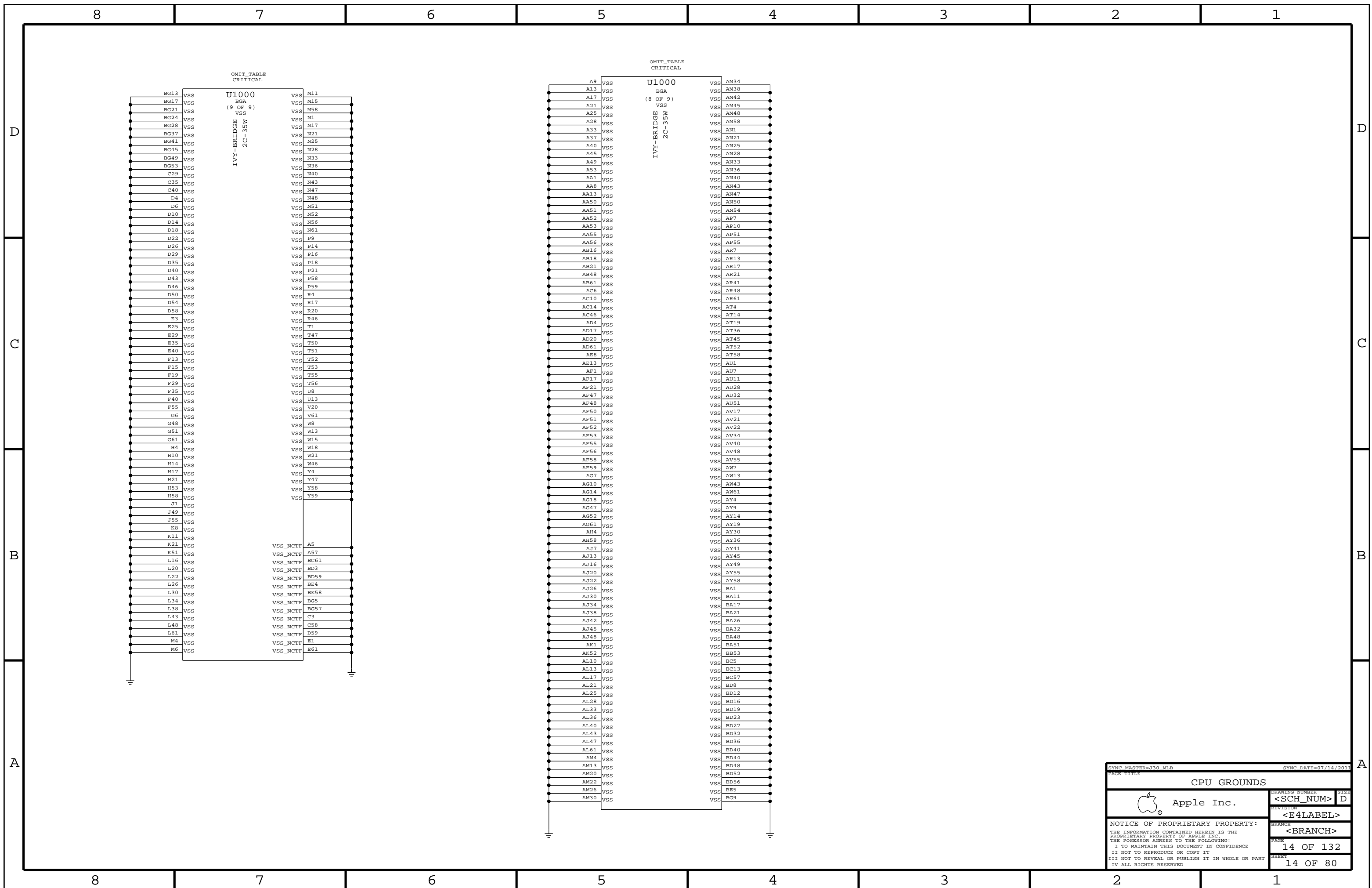
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Apple Inc.		DRAWING NUMBER	SIZE
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 CPU DDR3 INTERFACES
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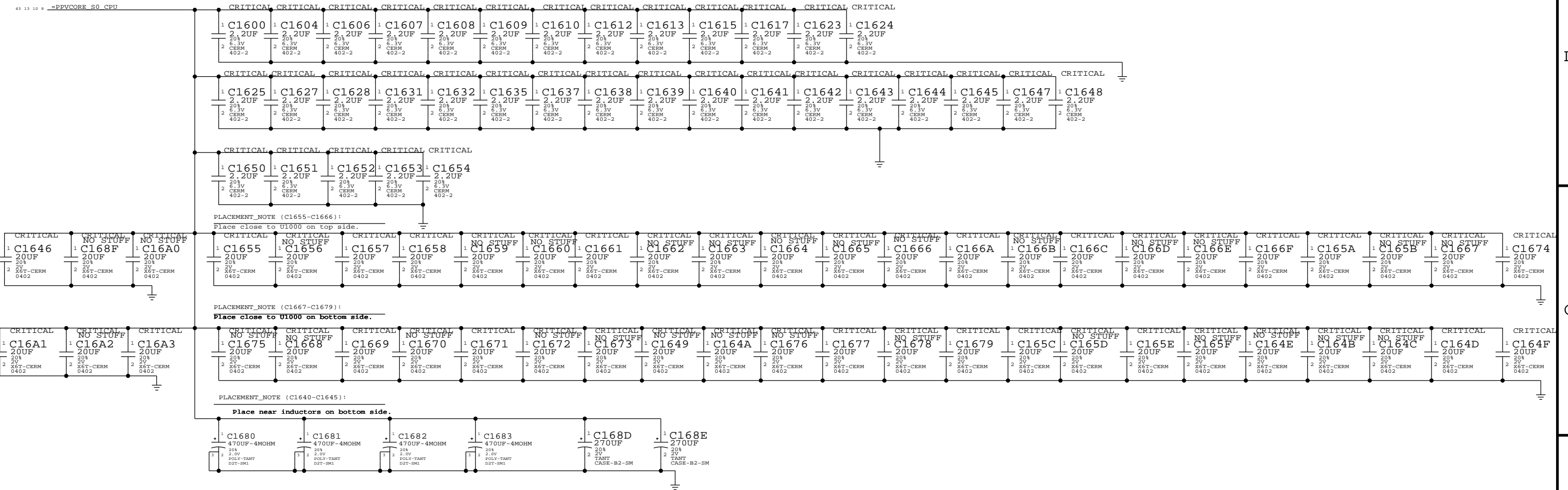
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CPU VCORE DECOUPLING

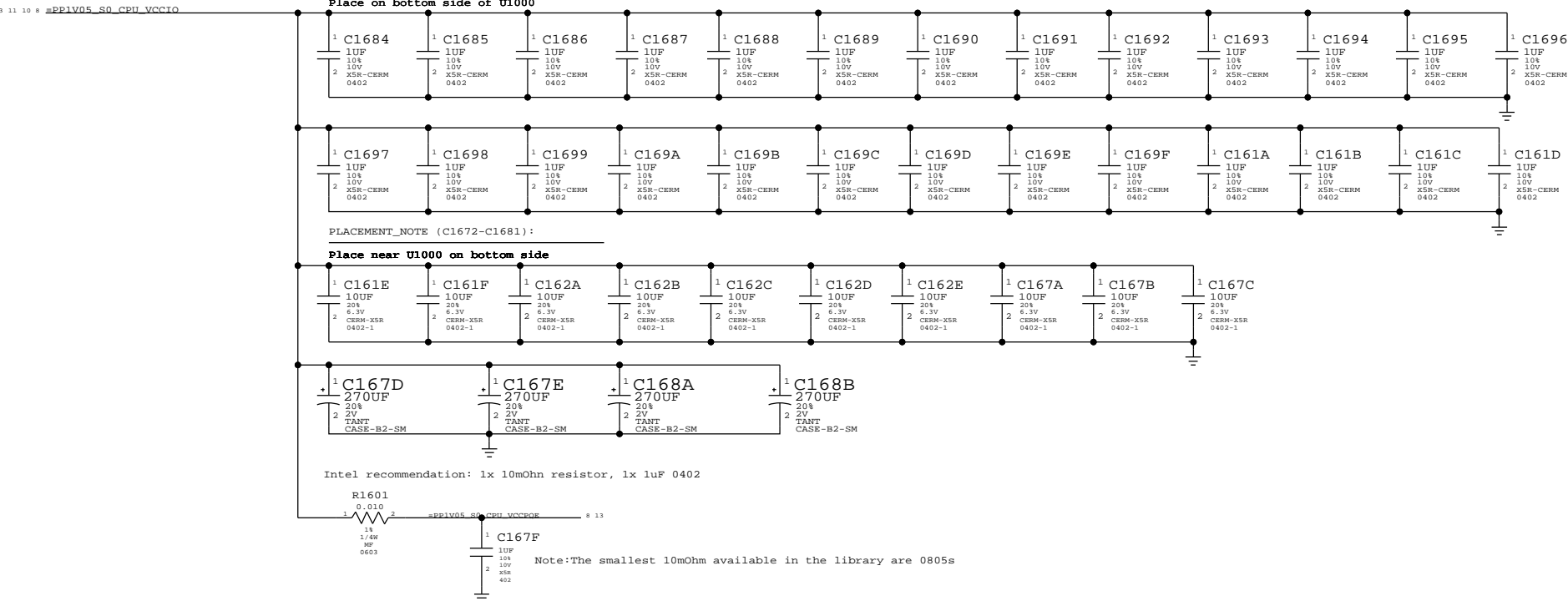
Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF



CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

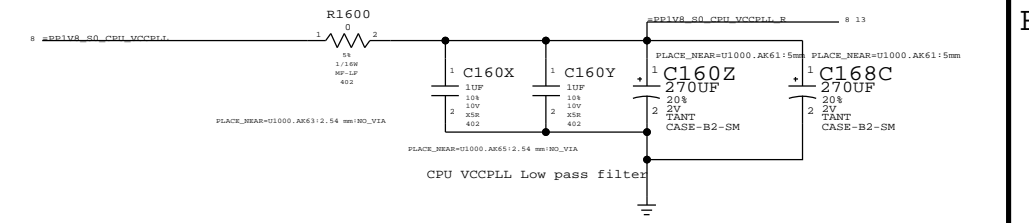
PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000



CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):



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CPU DECOUPLING-I			
	Apple Inc.		DRAWING NUMBER <SCH_NUM> D
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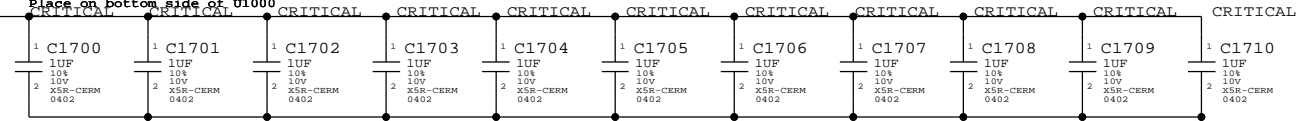
VAXG DECOUPLING

Intel recommendation (Table 7-4) for GT2 3.9mOhm LL: 11x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

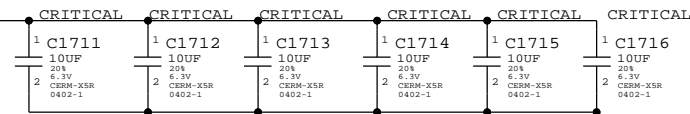
43 13 10 # =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

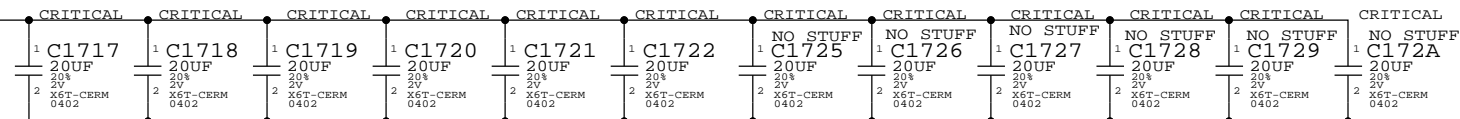
Place on bottom side of U1000



PLACEMENT_NOTE (C1711-C1716):

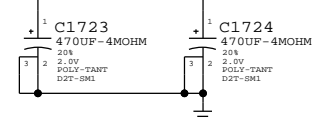


PLACEMENT_NOTE (C1717-C1722):



PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

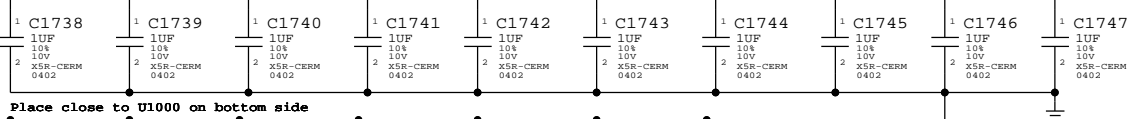


CPU VDDQ/VCCDQ DECOUPLING

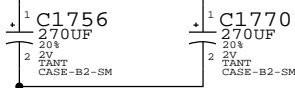
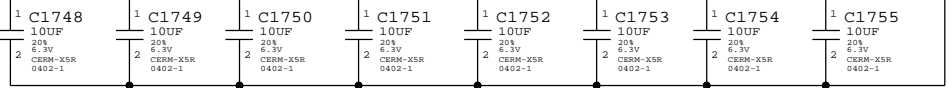
Intel recommendation (Table 7-11): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

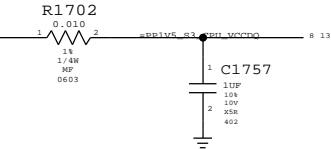
Place on bottom side of U1000



Place close to U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

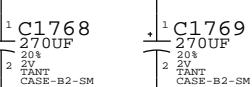
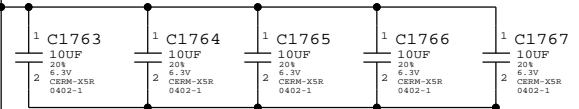
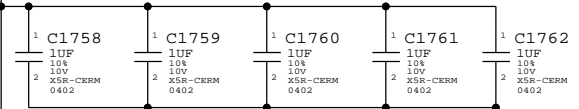


CPU VCCSA DECOUPLING

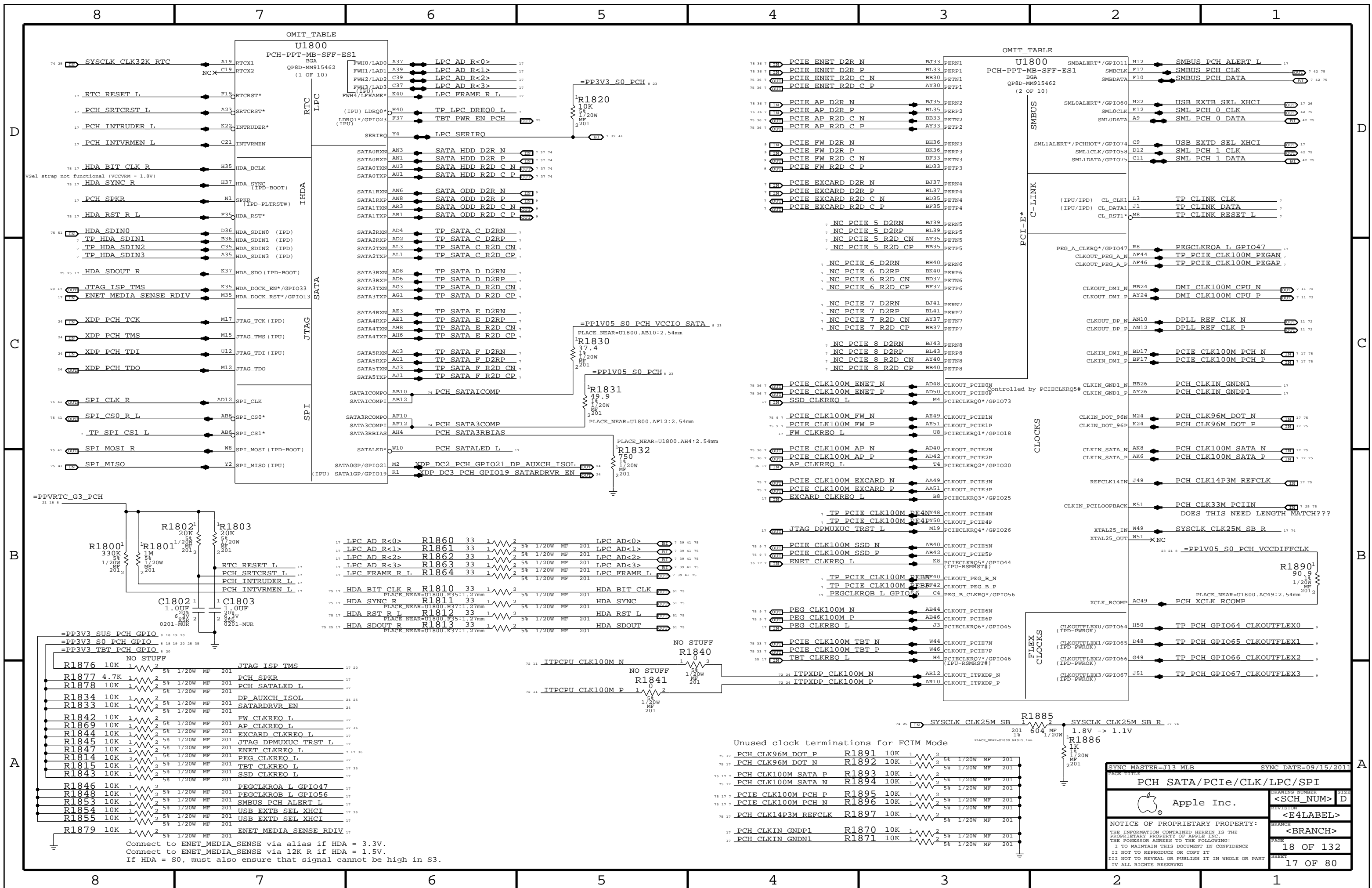
Intel recommendation (Table 7-9): 5x 1uF, 5x 10uF, 1x 330uF

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000



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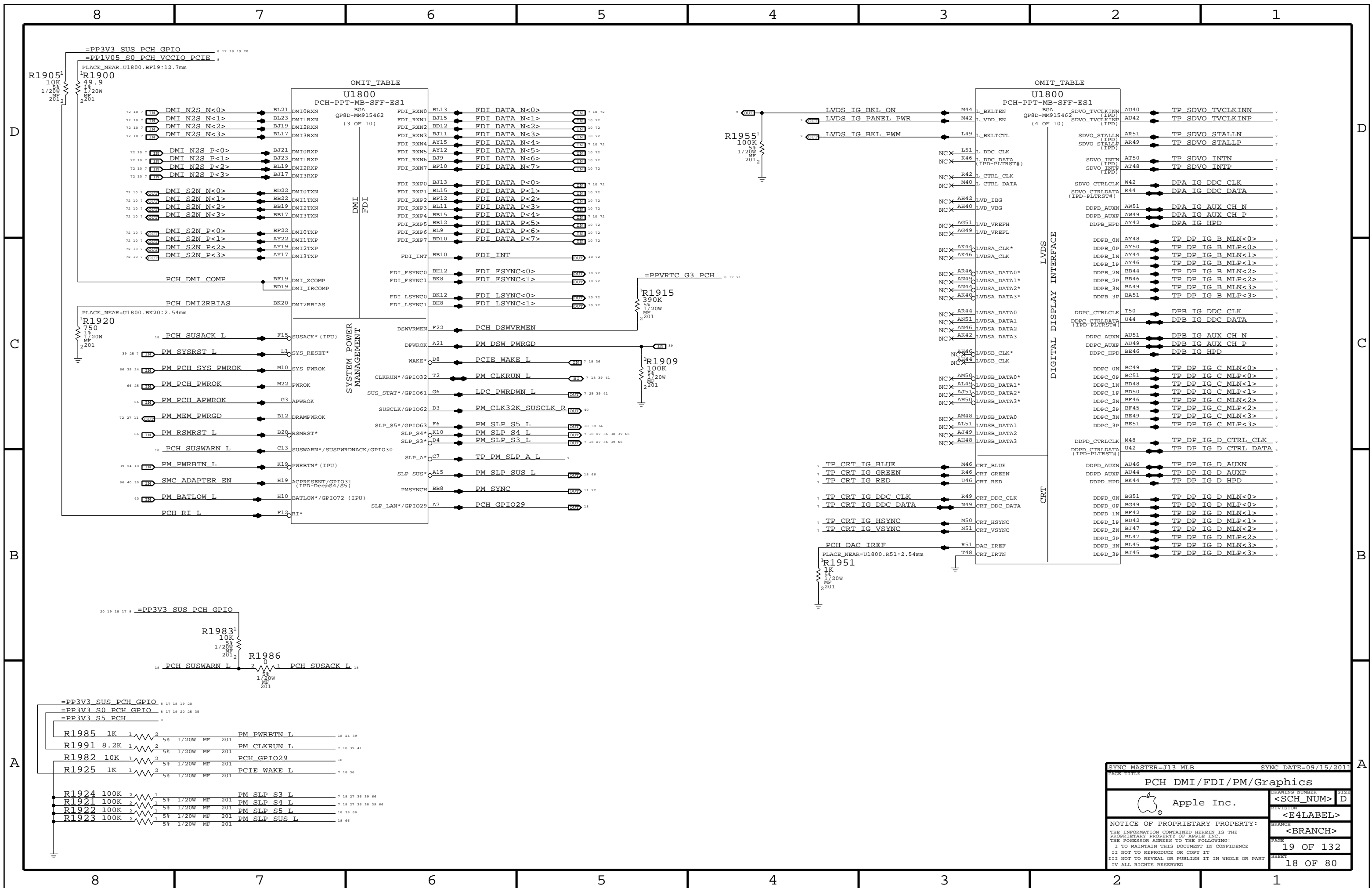
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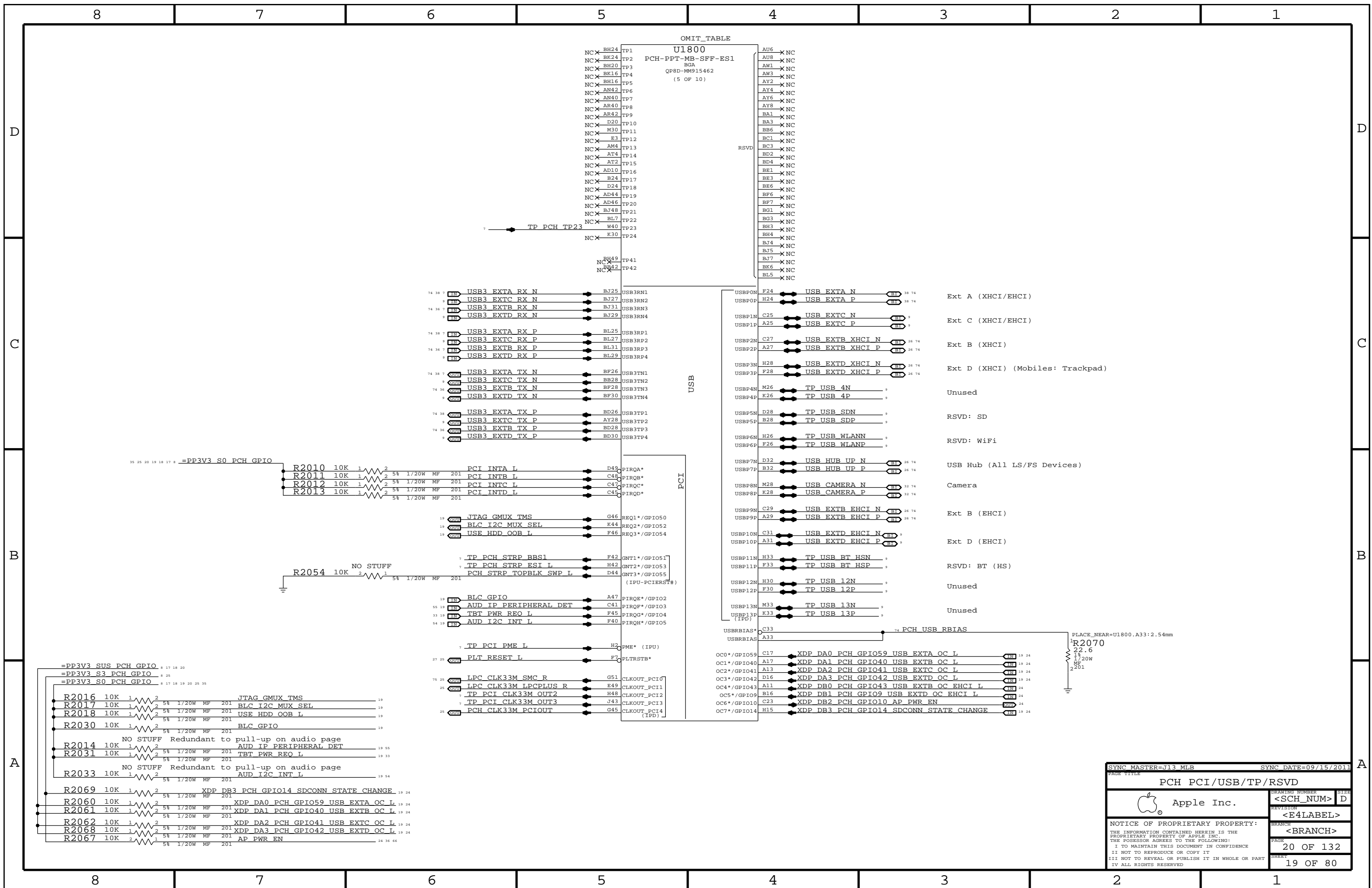
Unused clock terminations for FCIM Mode

R1891	10K	1	2	5%	1/20W	MF	201	PCH CLK96M DOT P
R1892	10K	1	2	5%	1/20W	MF	201	PCH CLK96M DOT N
R1893	10K	1	2	5%	1/20W	MF	201	PCH CLK100M SATA P
R1894	10K	1	2	5%	1/20W	MF	201	PCH CLK100M SATA N
R1895	10K	1	2	5%	1/20W	MF	201	PCIE CLK100M PCH P
R1896	10K	1	2	5%	1/20W	MF	201	PCIE CLK100M PCH N
R1897	10K	1	2	5%	1/20W	MF	201	PCH CLK14P3M REFCLK
R1870	10K	1	2	5%	1/20W	MF	201	PCH CLKIN GNDP1
R1871	10K	1	2	5%	1/20W	MF	201	PCH CLKIN GNDN1

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
 Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
 If HDA = S0, must also ensure that signal cannot be high in S3.



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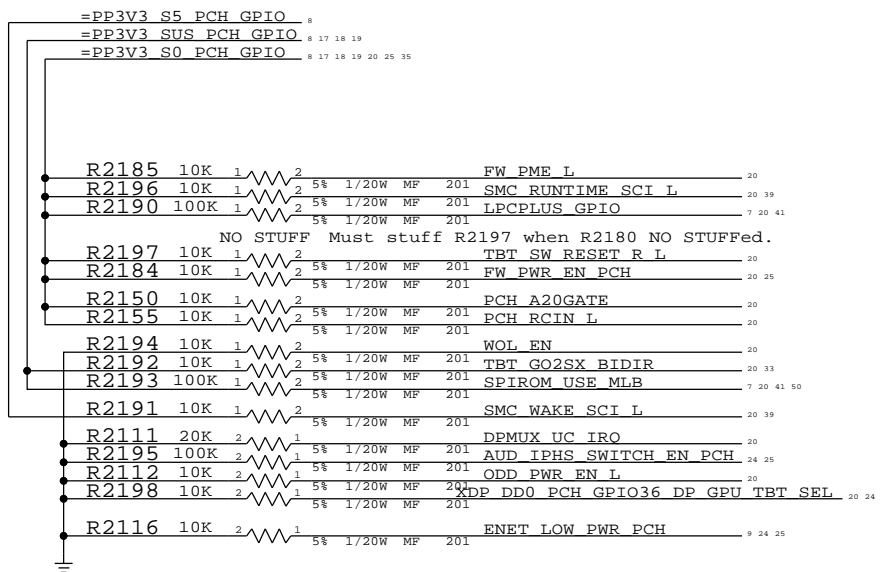
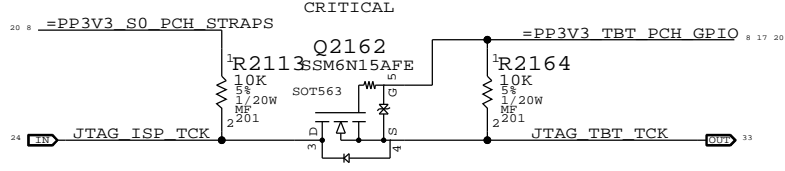
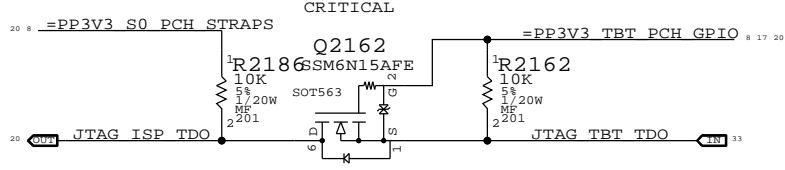
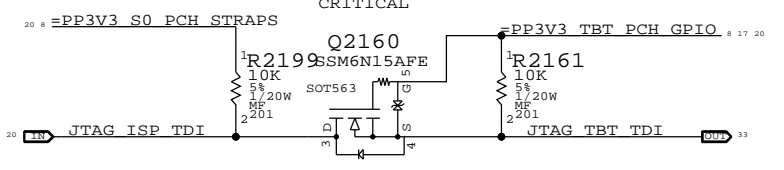
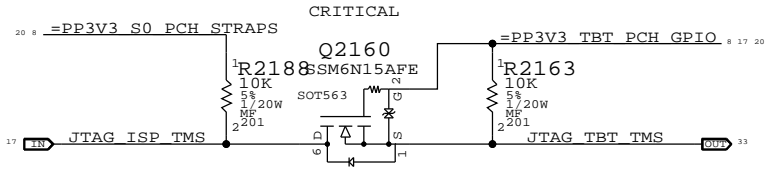
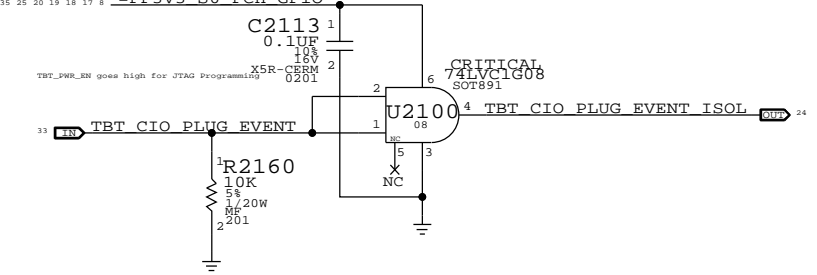
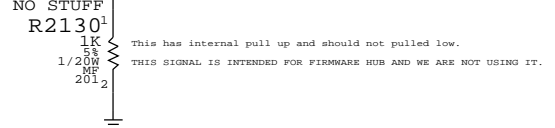
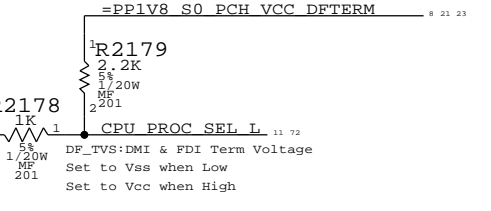
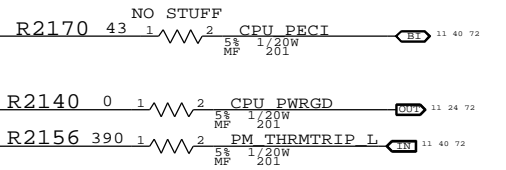
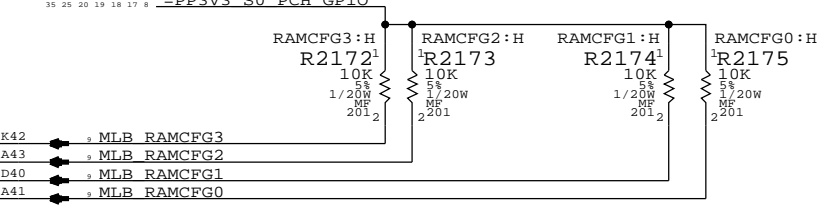
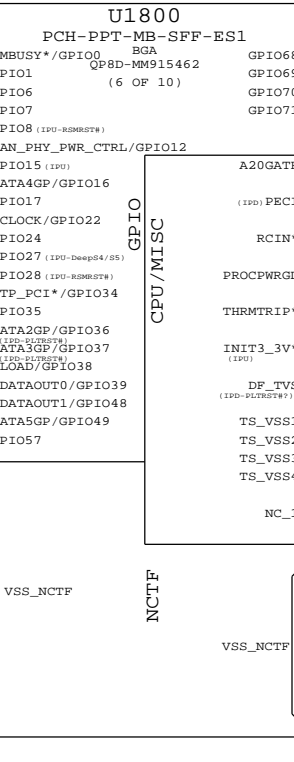
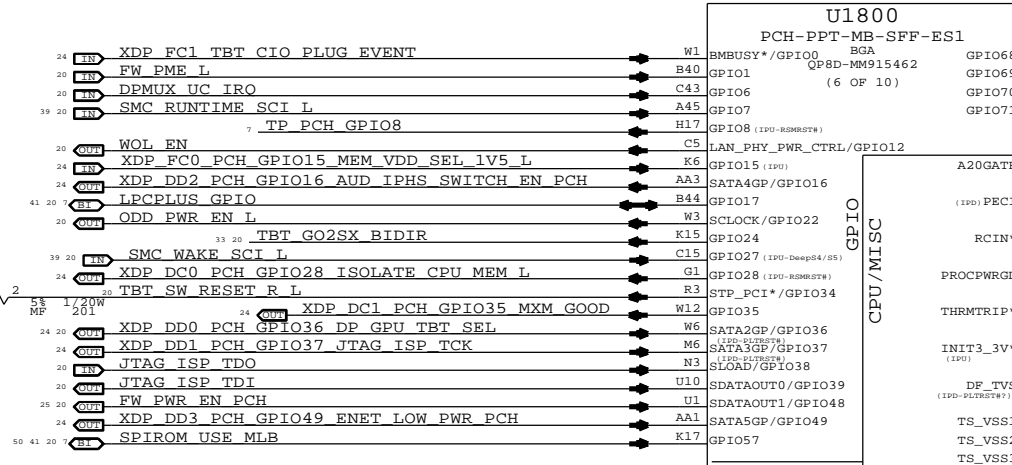
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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H, RAMCFG2:H, RAMCFG1:H, RAMCFG0:H

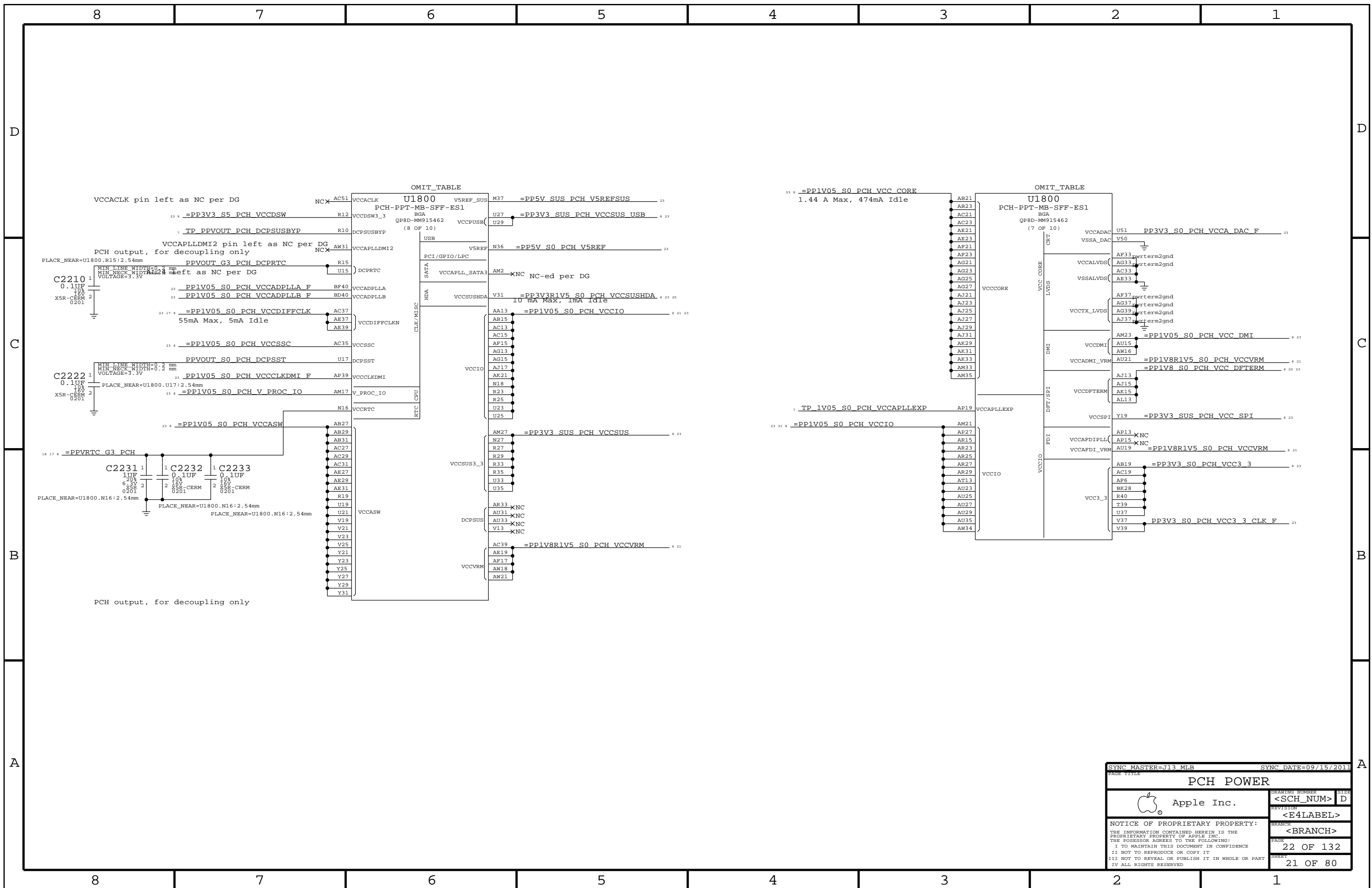
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..

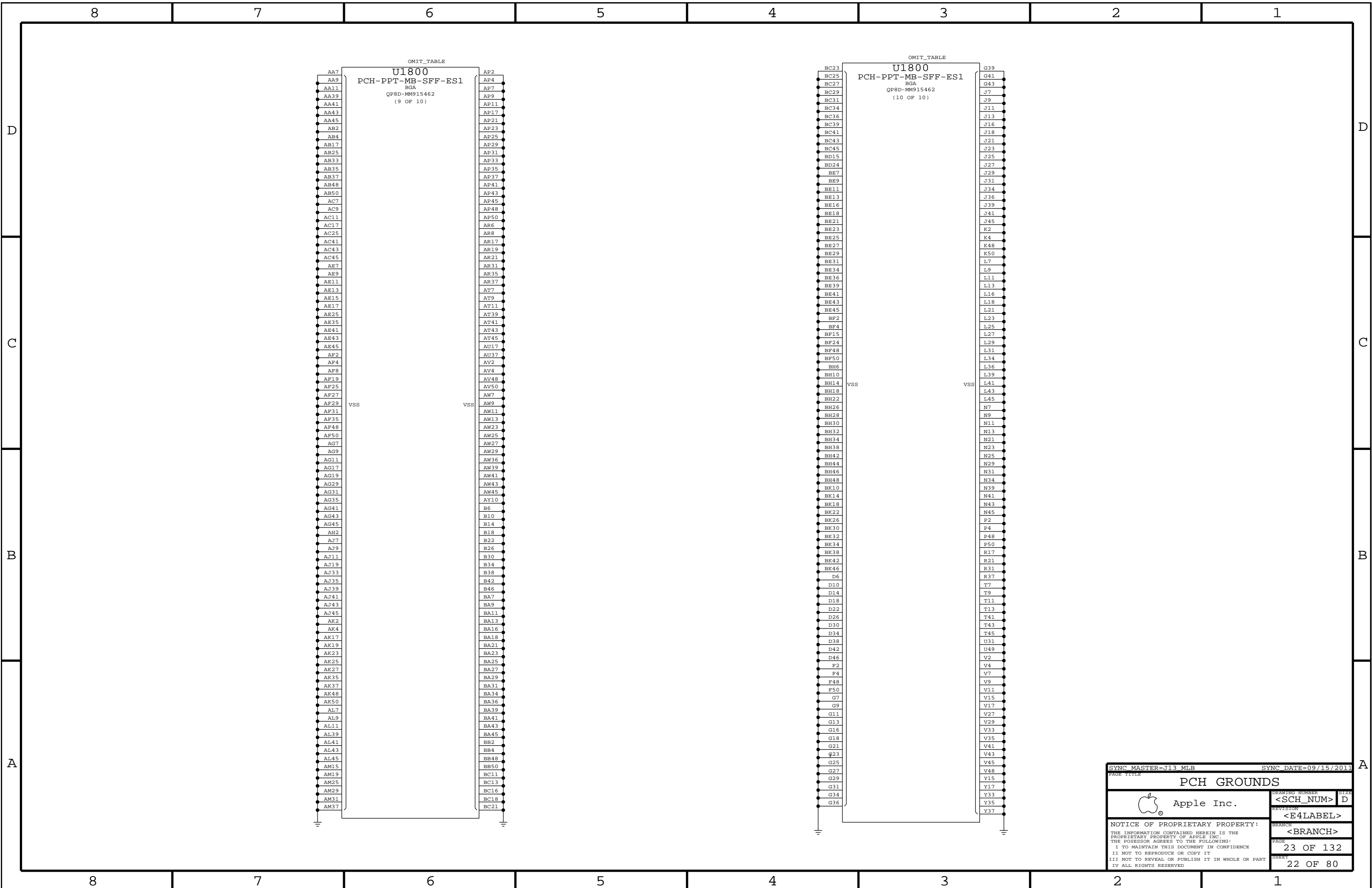



JTAG Isolation due to glitch in and out of sleep
NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CH is Push-Pull CMOS

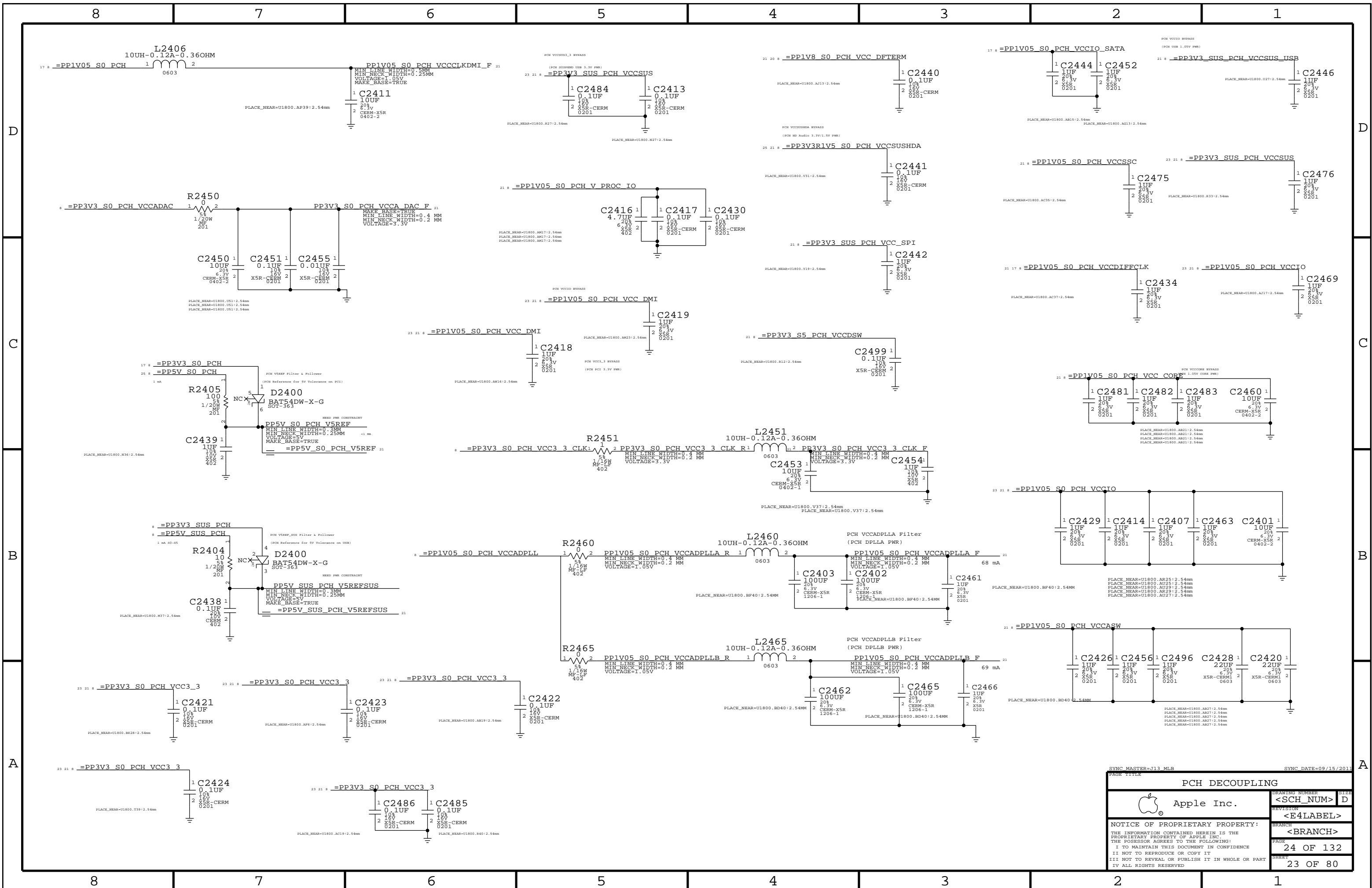
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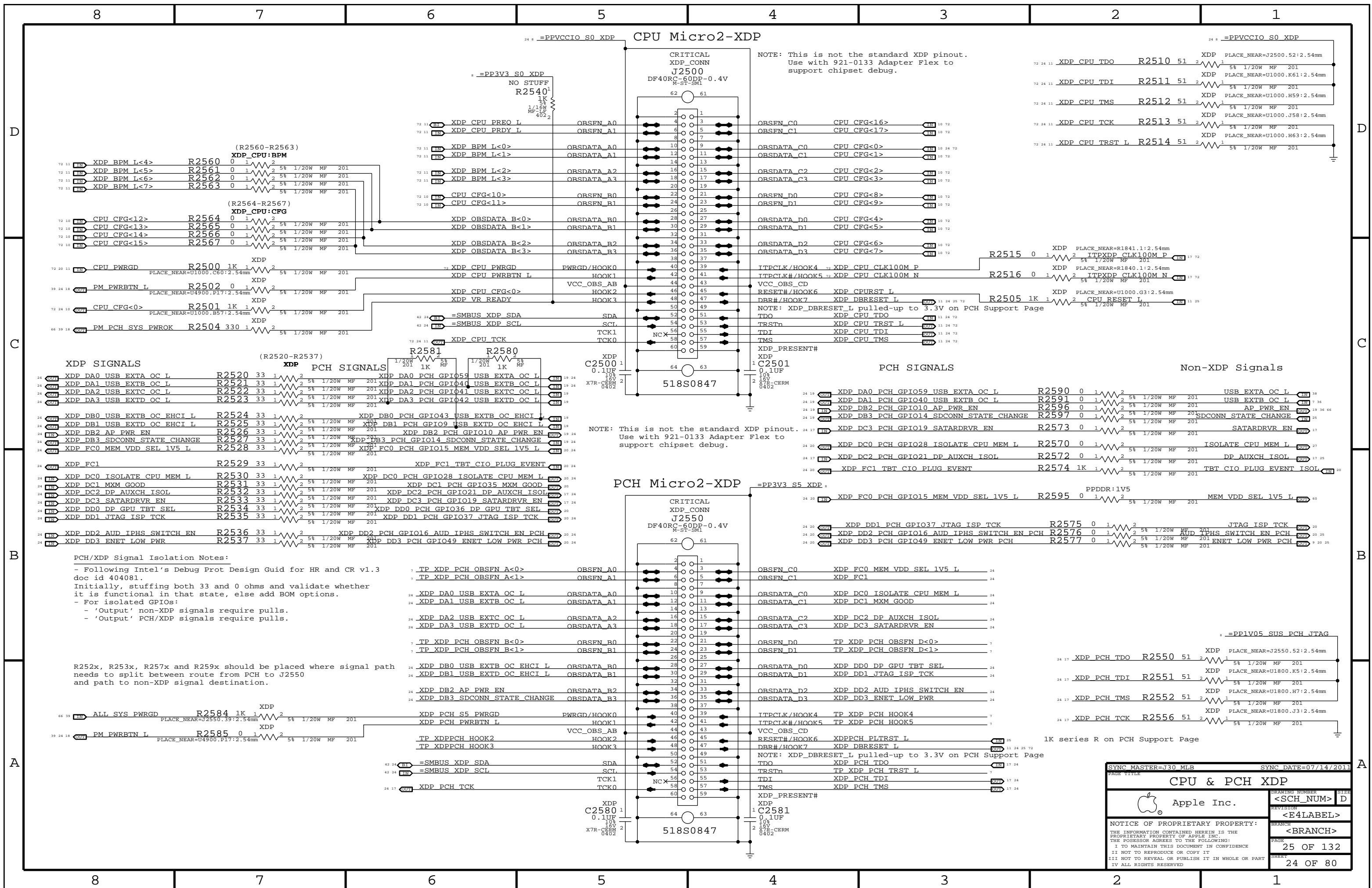
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	PAGE	24 OF 132	
	SHEET	23 OF 80	



NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

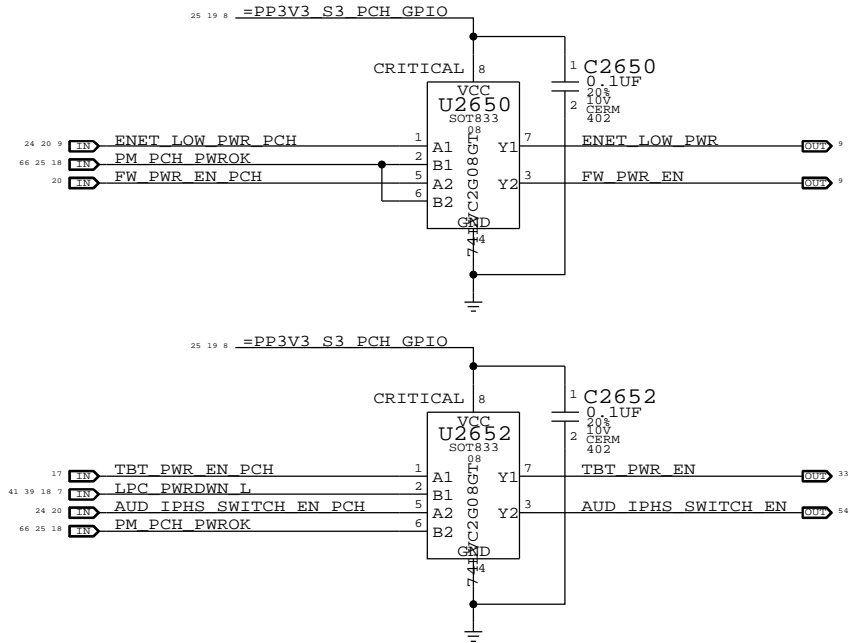
1K series R on PCH Support Page

PCH/XDP Signal Isolation Notes:
 - Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
 Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
 - For isolated GPIOs:
 - 'Output' non-XDP signals require pulls.
 - 'Output' PCH/XDP signals require pulls.

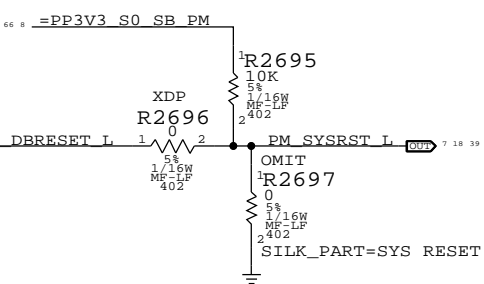
R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

PAGE TITLE		SYNC DATE=07/14/2011	
CPU & PCH XDP		DRAWING NUMBER	SIZE
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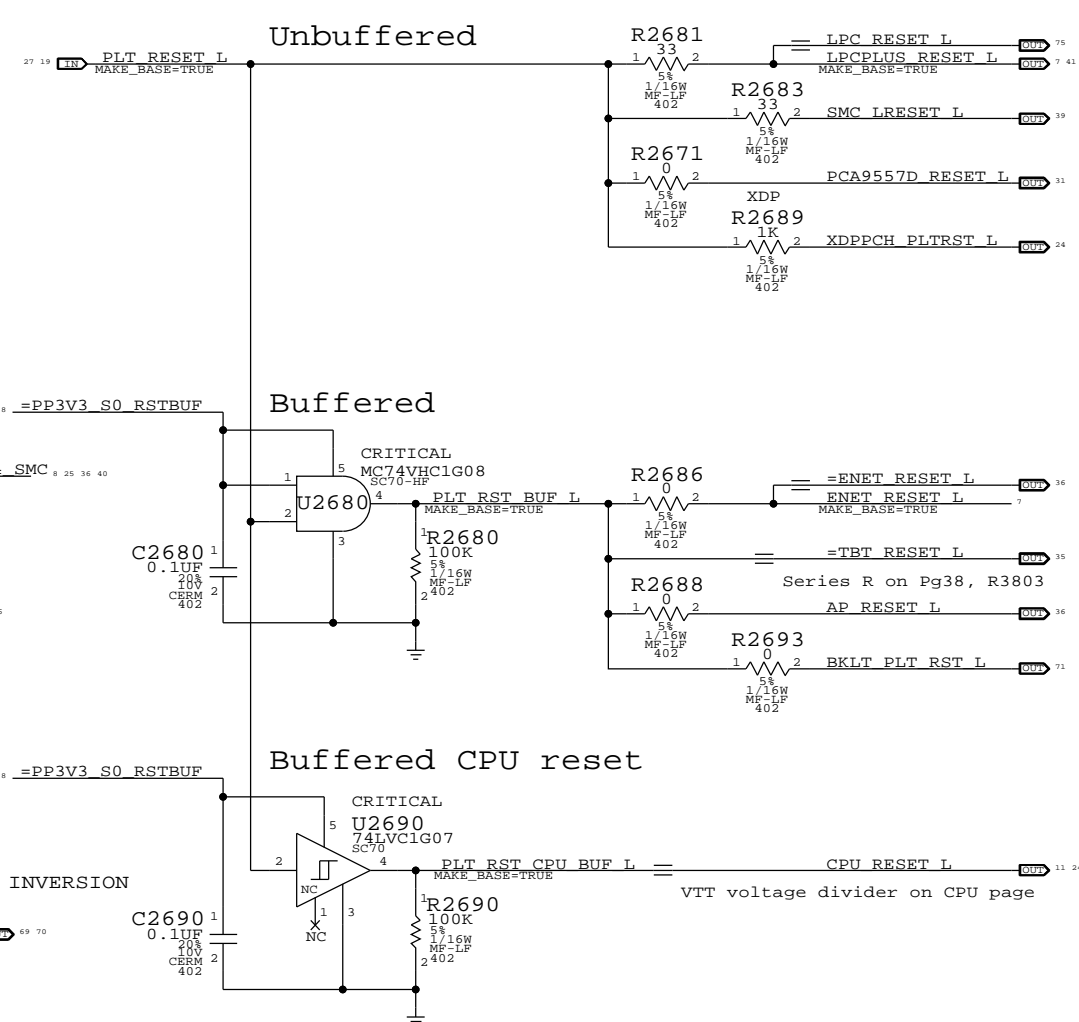
GPIO Glitch Prevention



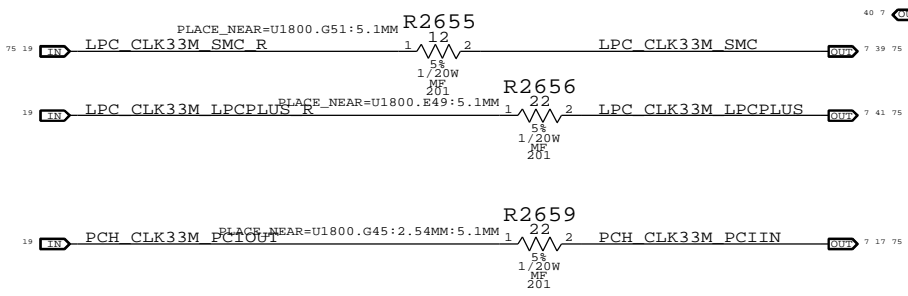
PCH Reset Button



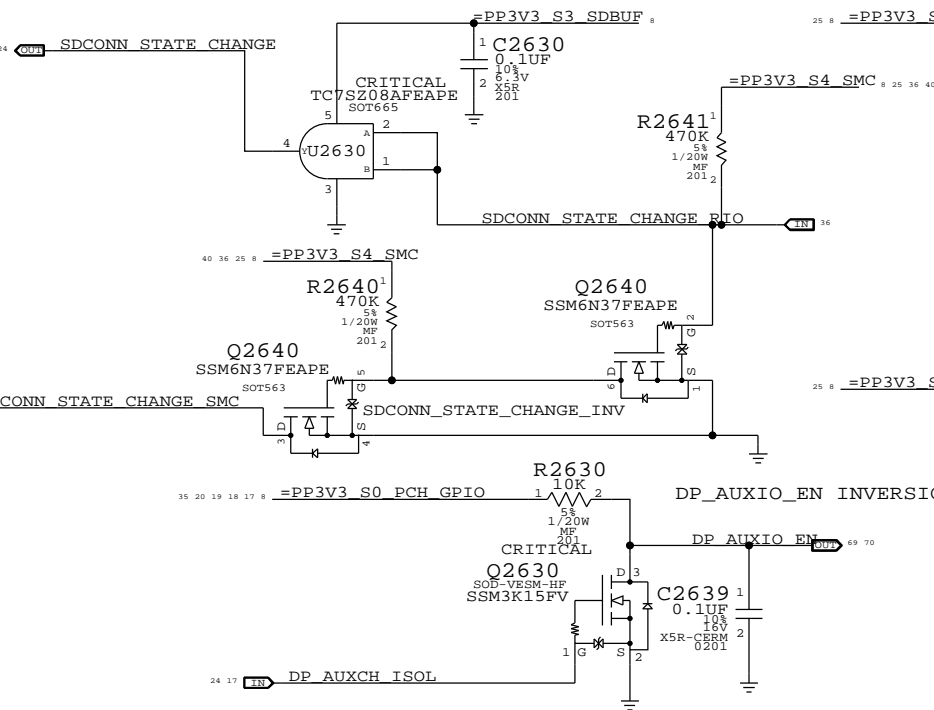
Platform Reset Connections



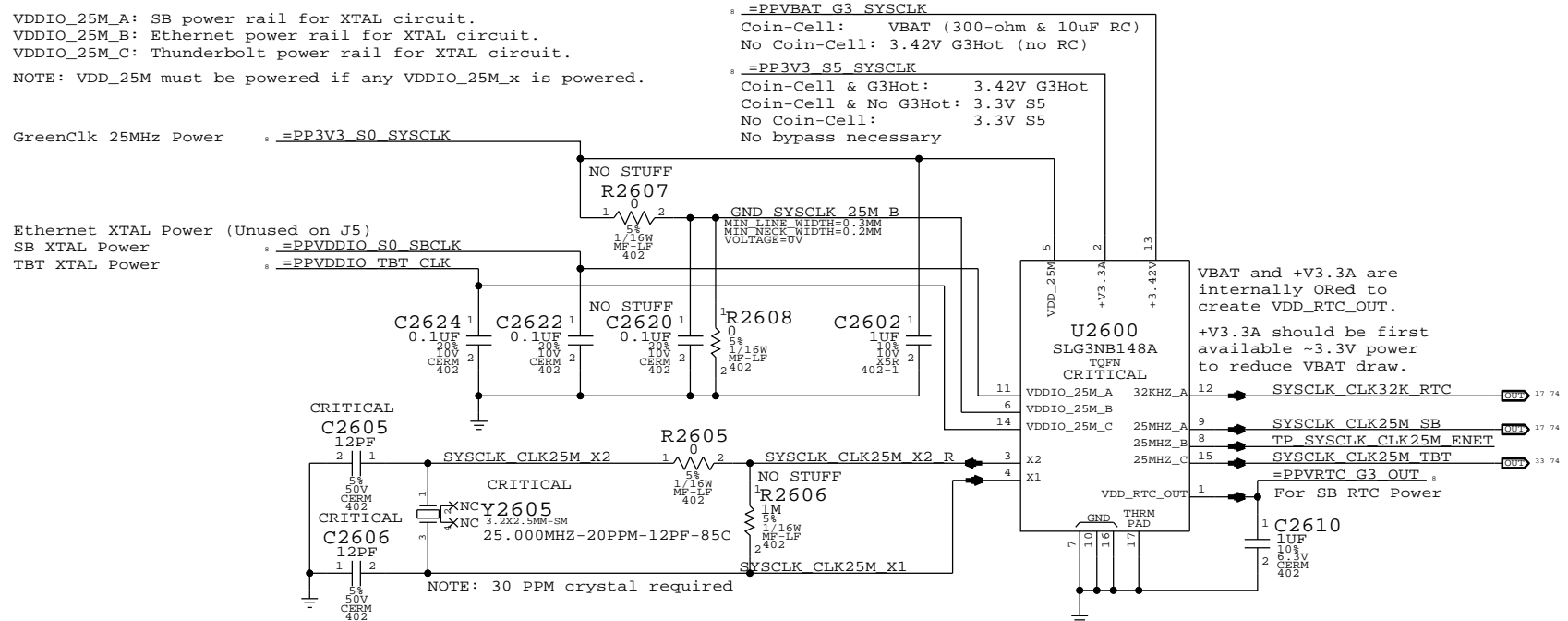
33 MHz Clock Series Termination



SDCONN_STATE_CHANGE ISOLATION

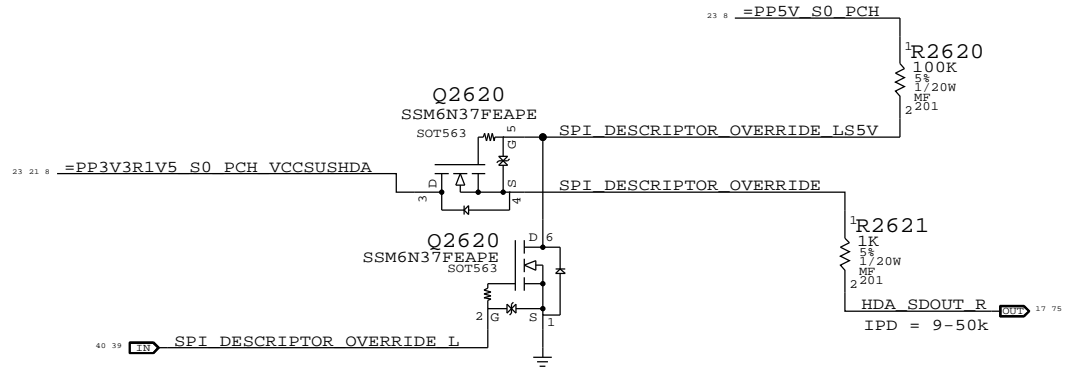


System RTC Power Source & 32kHz / 25MHz Clock Generator



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



PAGE TITLE		SYNC DATE=MASTER	
Chipset Support			
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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0, HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0, HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1, HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1, HUB_NONREM0_1

NON_REM 1 : NON_REM 0
 0 : 0
 1 : 1

STRAP PIN CFG
 ALL PORTS ARE REMOVABLE
 PORT 1 IS NON REMOVABLE
 PORT 1&2 ARE NON REMOVABLE
 PORT 1&2&3 ARE NON REMOVABLE

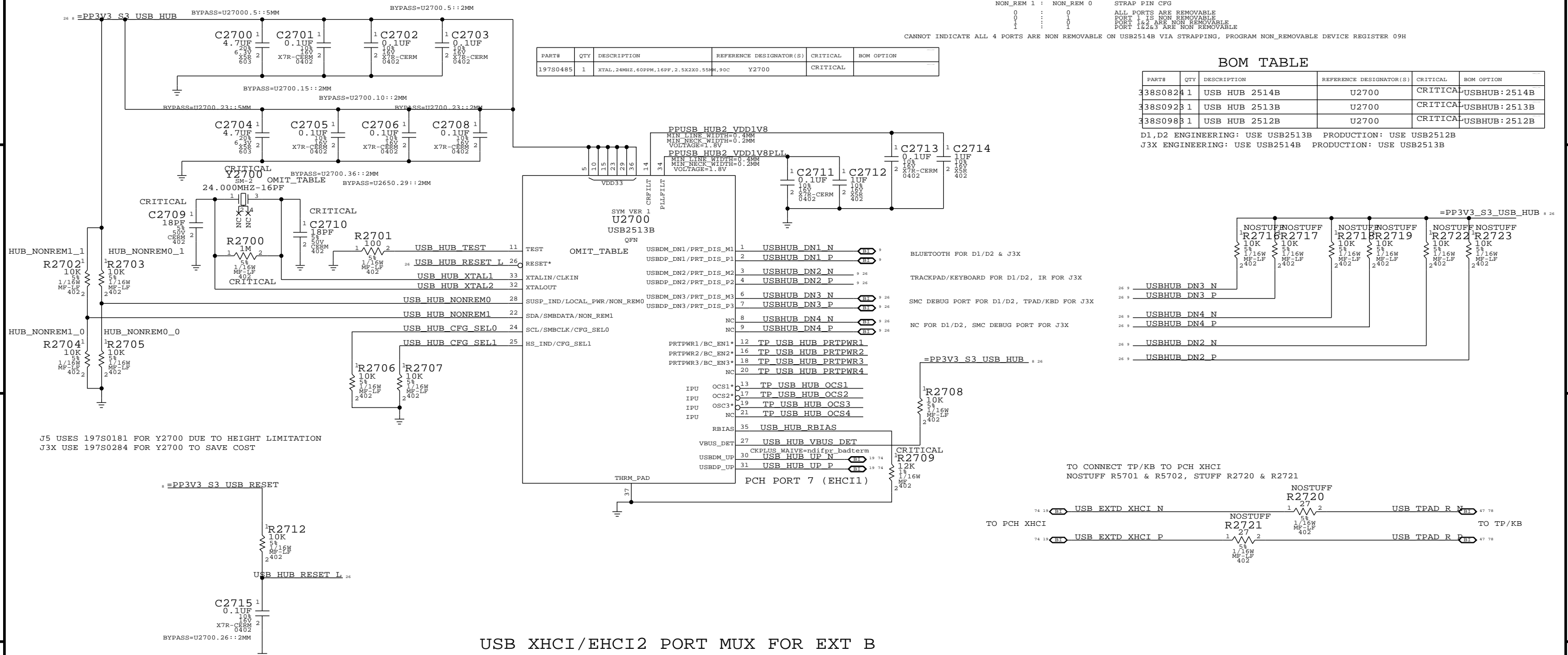
CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STRAPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0485	1	XTAL, 24MHZ, 60PPM, 16PF, 2.5X2X0.55MM, 9DC	Y2700	CRITICAL	

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
38S082	1	USB HUB 2514B	U2700	CRITICAL	USBHUB:2514B
38S092	1	USB HUB 2513B	U2700	CRITICAL	USBHUB:2513B
38S098	1	USB HUB 2512B	U2700	CRITICAL	USBHUB:2512B

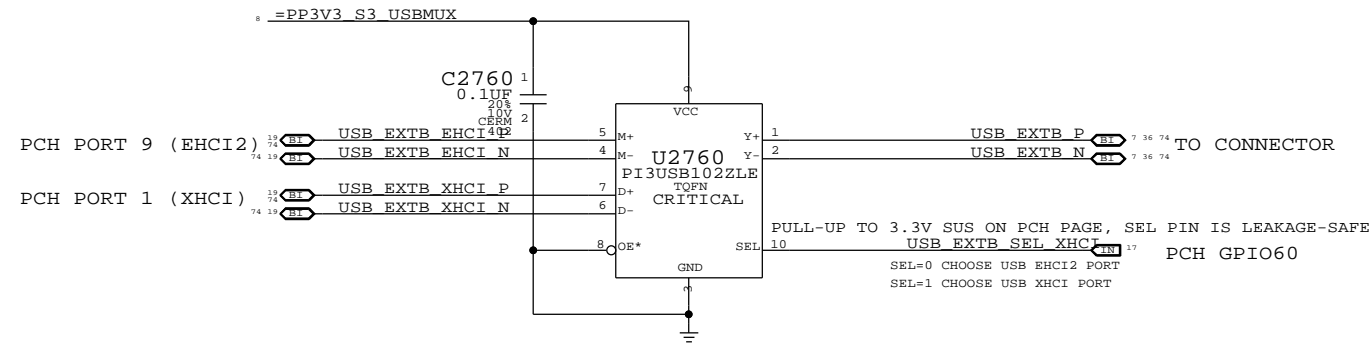
D1,D2 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
 J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
 J3X USE 197S0284 FOR Y2700 TO SAVE COST

TO CONNECT TP/KB TO PCH XHCI
 NOSTUFF R5701 & R5702, STUFF R2720 & R2721

USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC MASTER=J5_AMD		SYNC DATE=08/17/2011	
USB HUB & MUX			
Apple Inc.		DRAWING NUMBER	SIZE
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

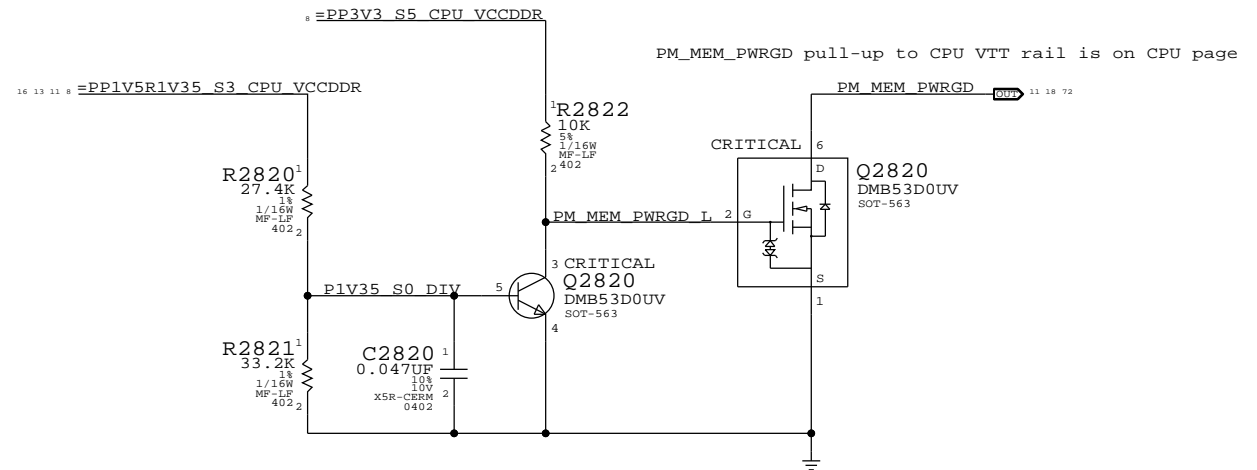
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

$$P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L$$

$$MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L$$

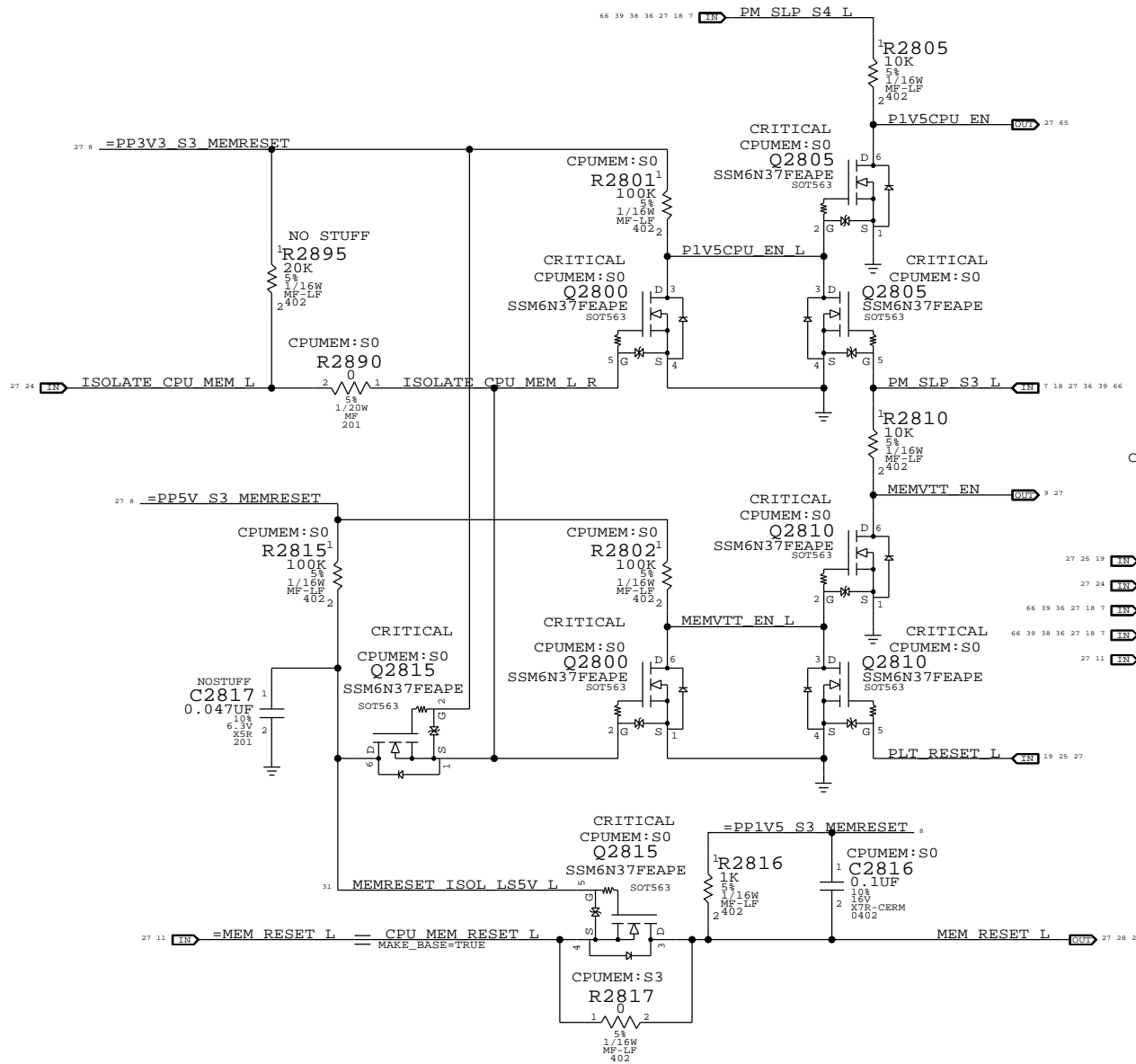
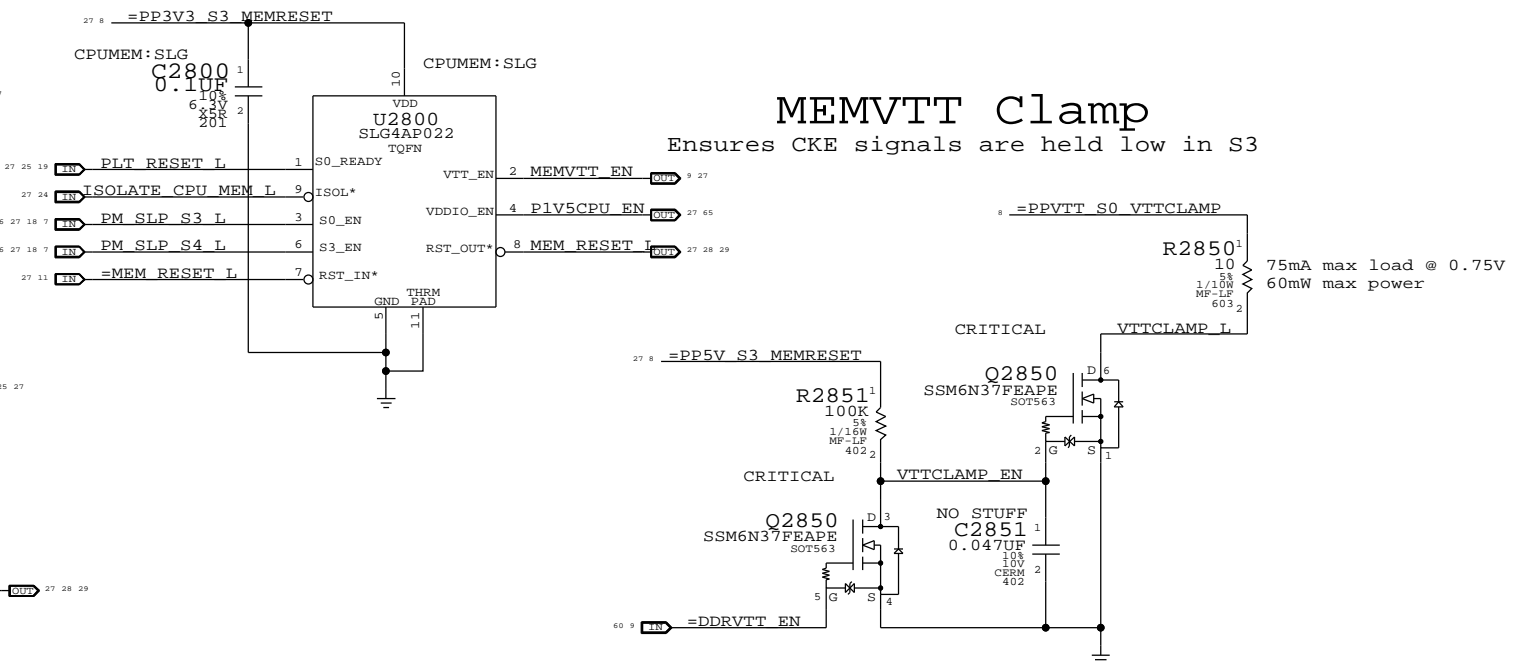
$$MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L$$

1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3

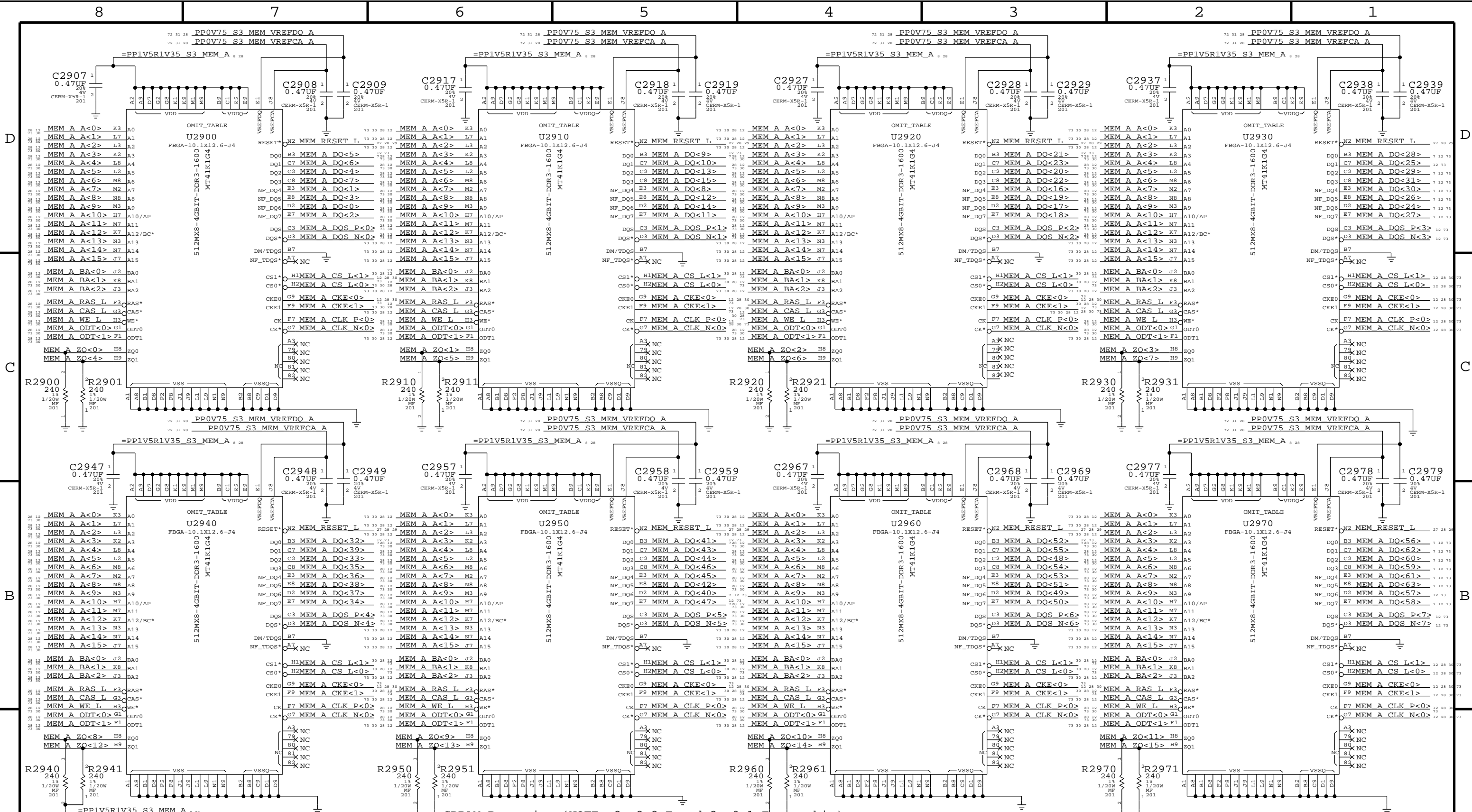


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	1	1
to	1	0	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	1	1

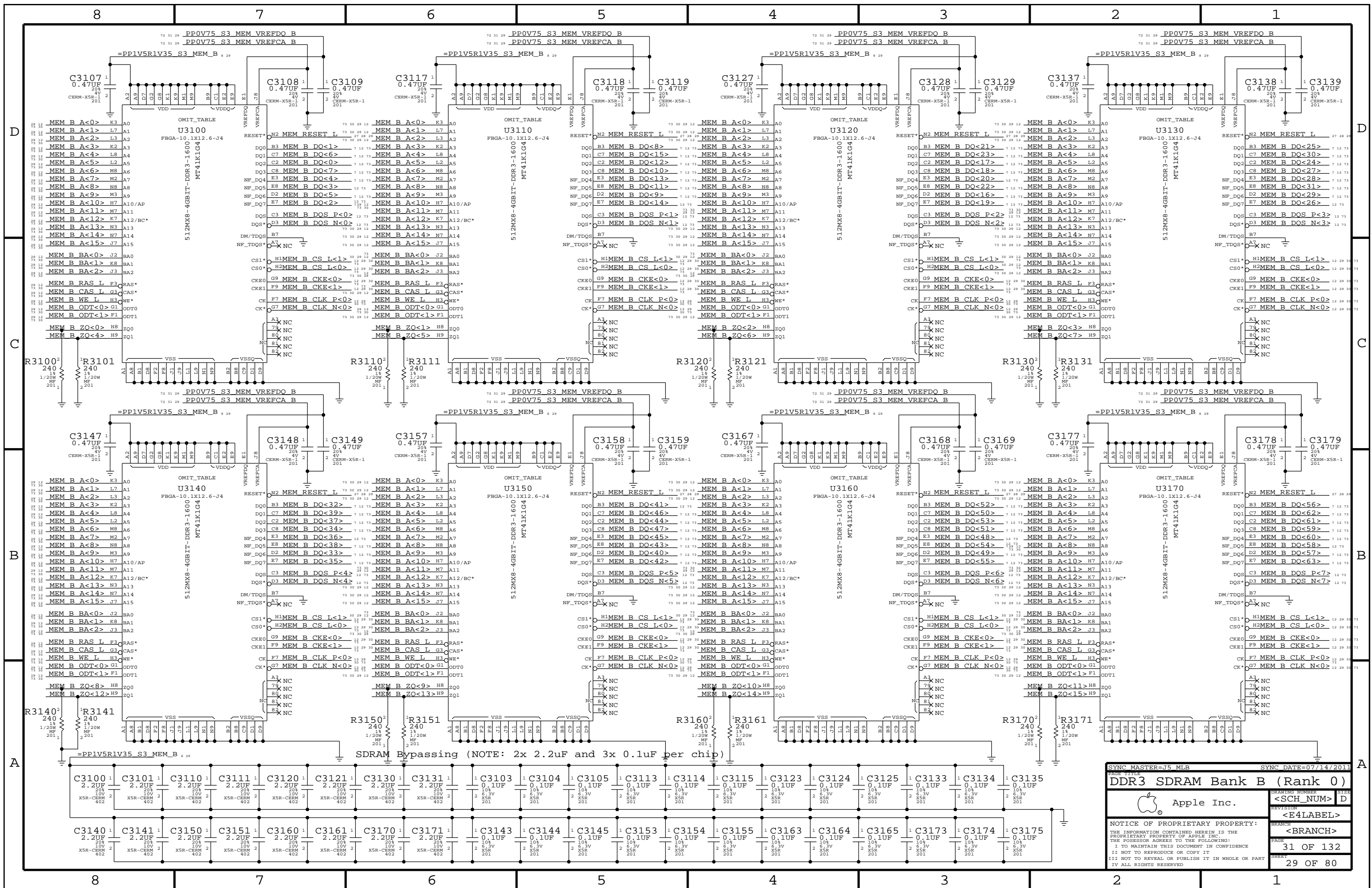
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

PAGE TITLE		DRAWING NUMBER	
CPU Memory S3 Support		<SCH_NUM> D	
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DDR3 SDRAM Bank A (Rank 0)			
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SYNC MASTER=J5 MLB
 SYNC DATE=07/14/2011
DDR3 SDRAM Bank B (Rank 0)
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8

7

6

5

4

3

2

1

JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

D

D

C

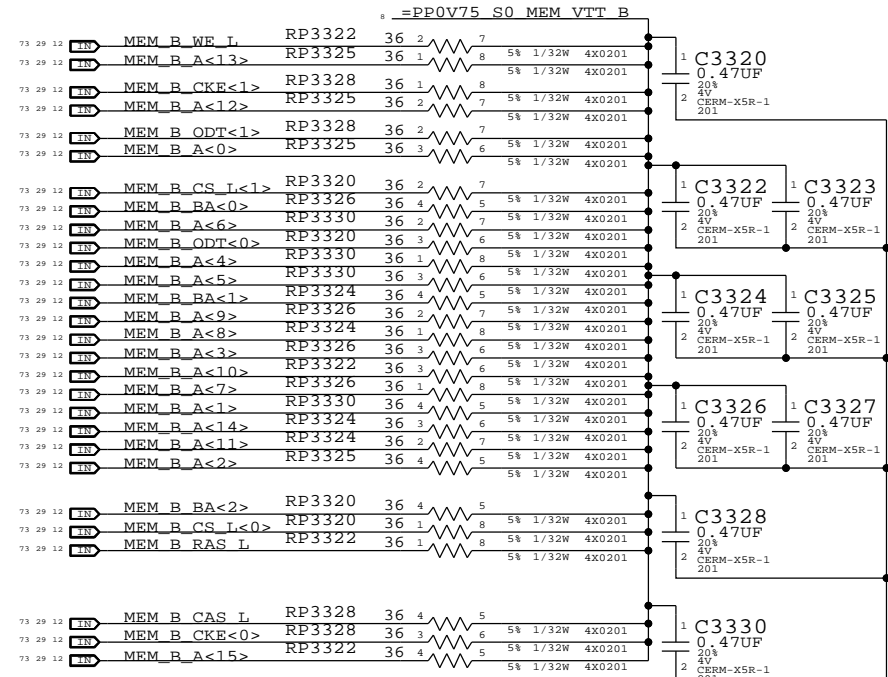
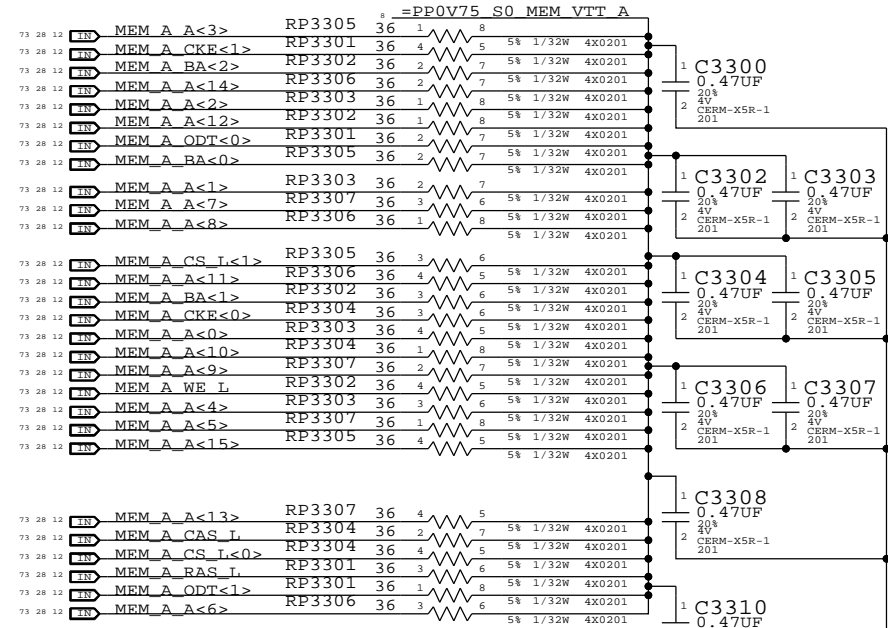
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B

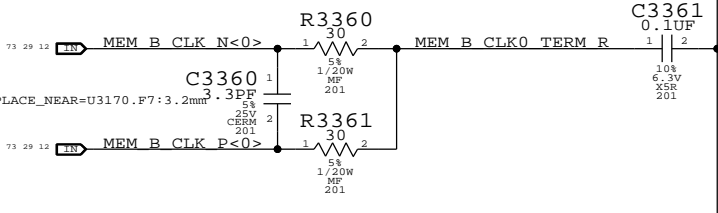
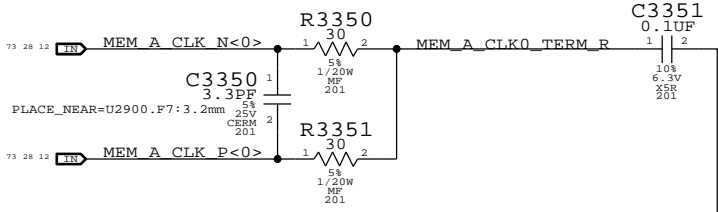
B

A

A



MEM Clock Termination
 Place RC end termination after last DRAM
 Place Source Cterm at neckdown at first DRAM



PAGE TITLE		SYNC DATE=MASTER	
DDR3 Termination			
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8

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5

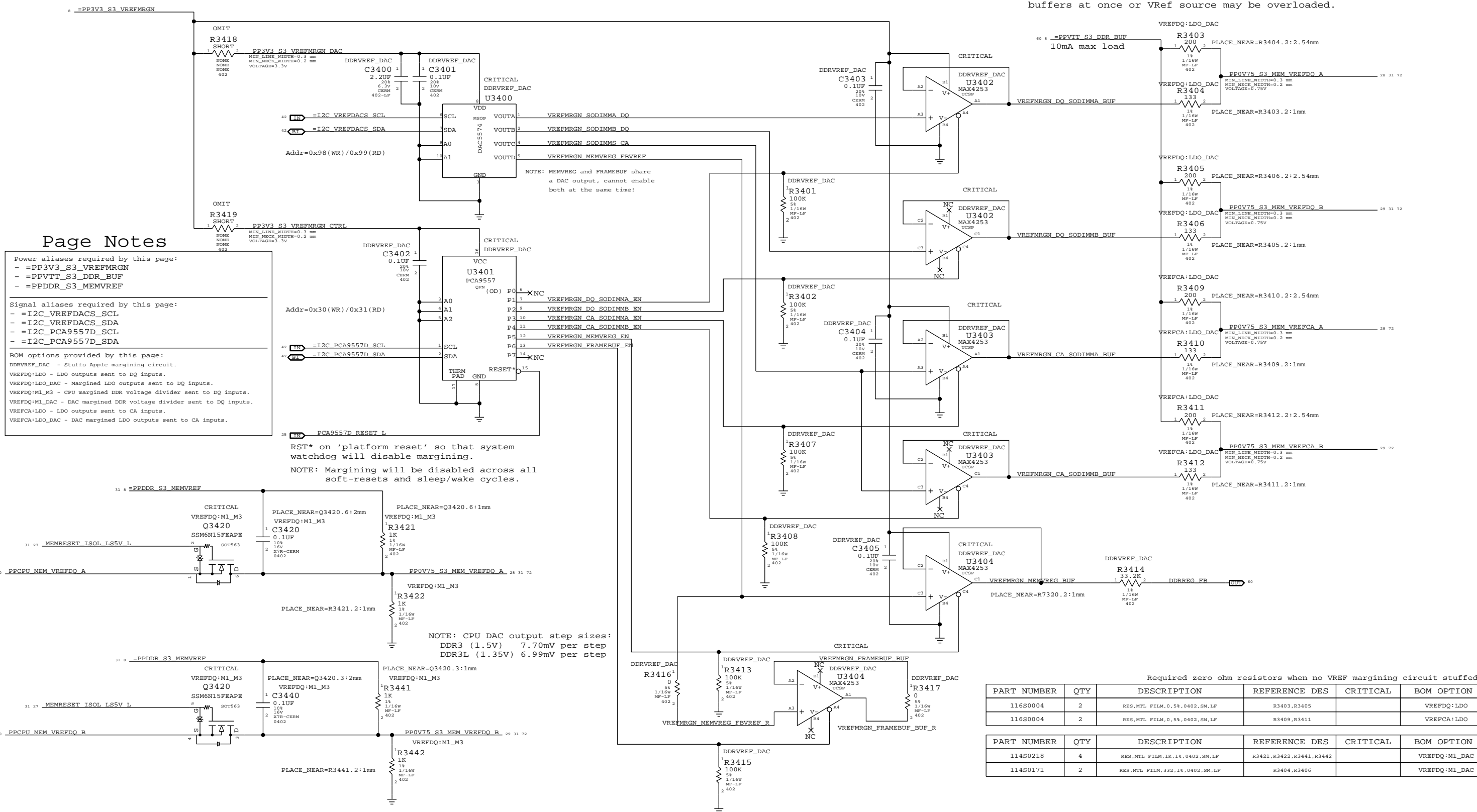
4

3

2

1

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Page Notes

Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PPVTT_S3_DDR_BUF
 - =PPDDR_S3_MEMVREF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 DDRVREF_DAC - Stuffs Apple margining circuit.
 VREFDQ:LDO - LDO outputs sent to DQ inputs.
 VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
 VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
 VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
 VREFCA:LDO - LDO outputs sent to CA inputs.
 VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

31 =PPDDR_S3_MEMVREF

31 27 MEMRESET ISOL LS5V L

72 10 PPCPU MEM VREFDQ A

31 8 =PPDDR_S3_MEMVREF

31 27 MEMRESET ISOL LS5V L

72 10 PPCPU MEM VREFDQ B

RST* on 'platform reset' so that system watchdog will disable margining.
 NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
 DDR3 (1.5V) 7.70mV per step
 DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0.5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1%,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+6.0mA - -6.0mA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

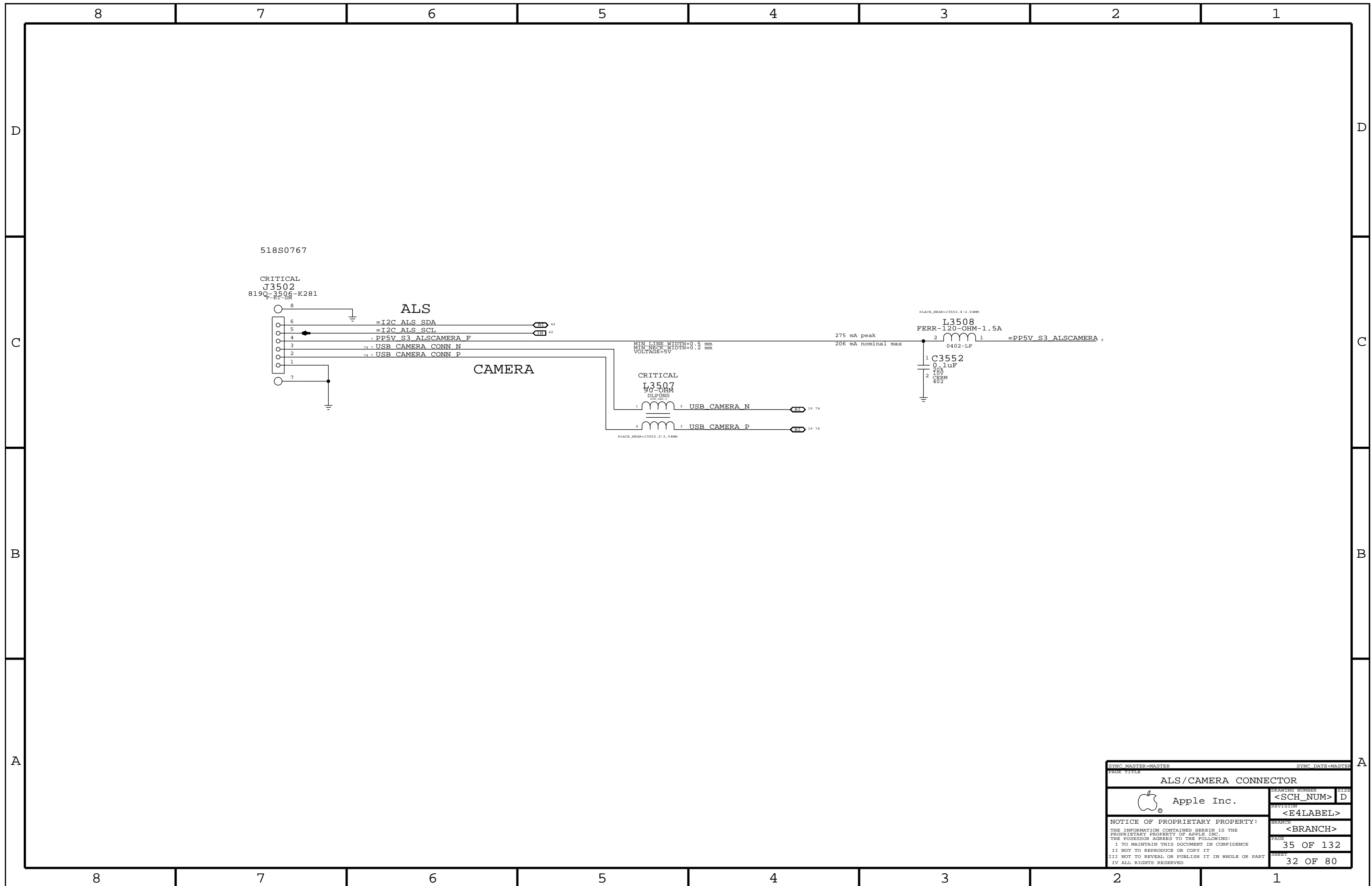
SYNC MASTER=J5_MLB SYNC DATE=07/29/2011

DDR3/FRAMEBUF VREF MARGINING

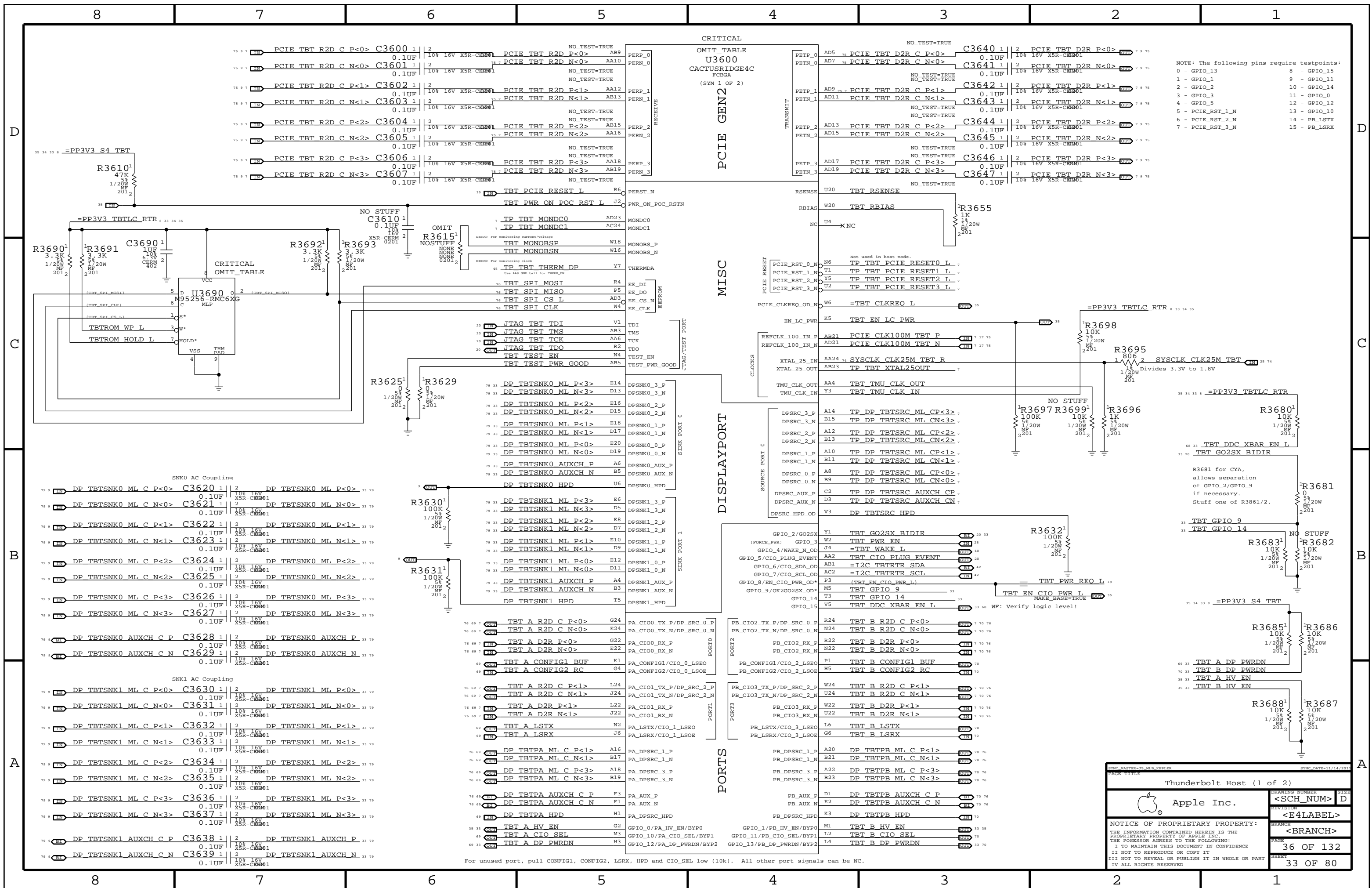
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ALS/CAMERA CONNECTOR			
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NOTE: The following pins require testpoints:
 0 - GPIO_13 8 - GPIO_15
 1 - GPIO_1 9 - GPIO_11
 2 - GPIO_2 10 - GPIO_14
 3 - GPIO_3 11 - GPIO_0
 4 - GPIO_5 12 - GPIO_12
 5 - PCIE_RST_I_N 13 - GPIO_10
 6 - PCIE_RST_2_N 14 - PB_LSTX
 7 - PCIE_RST_3_N 15 - PB_LSRX

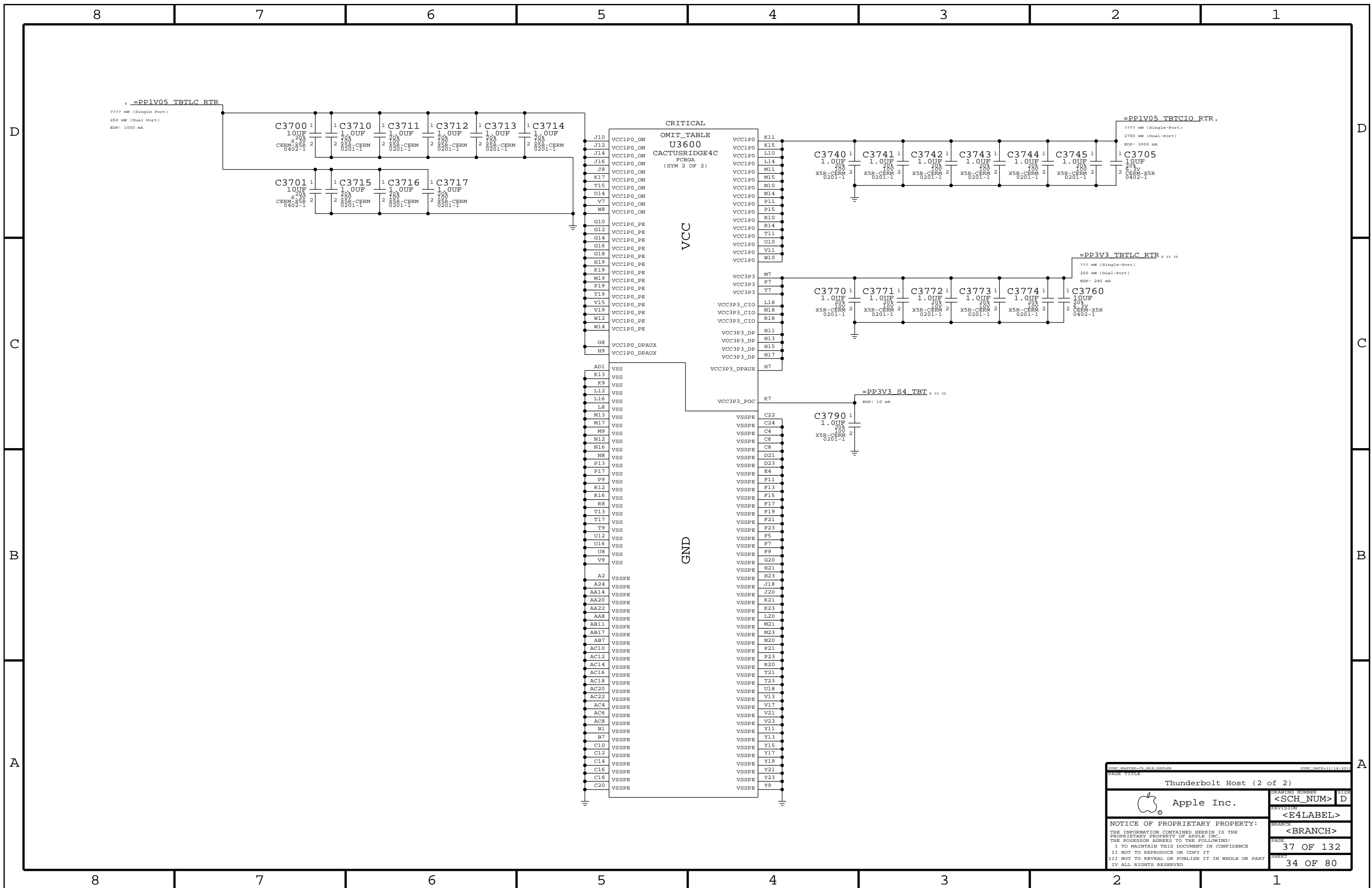
Thunderbolt Host (1 of 2)

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For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.



SYMC PARTS: M18, K1018		SYMC DATE: 11/14/2011	
PAGE TITLE: Thunderbolt Host (2 of 2)			
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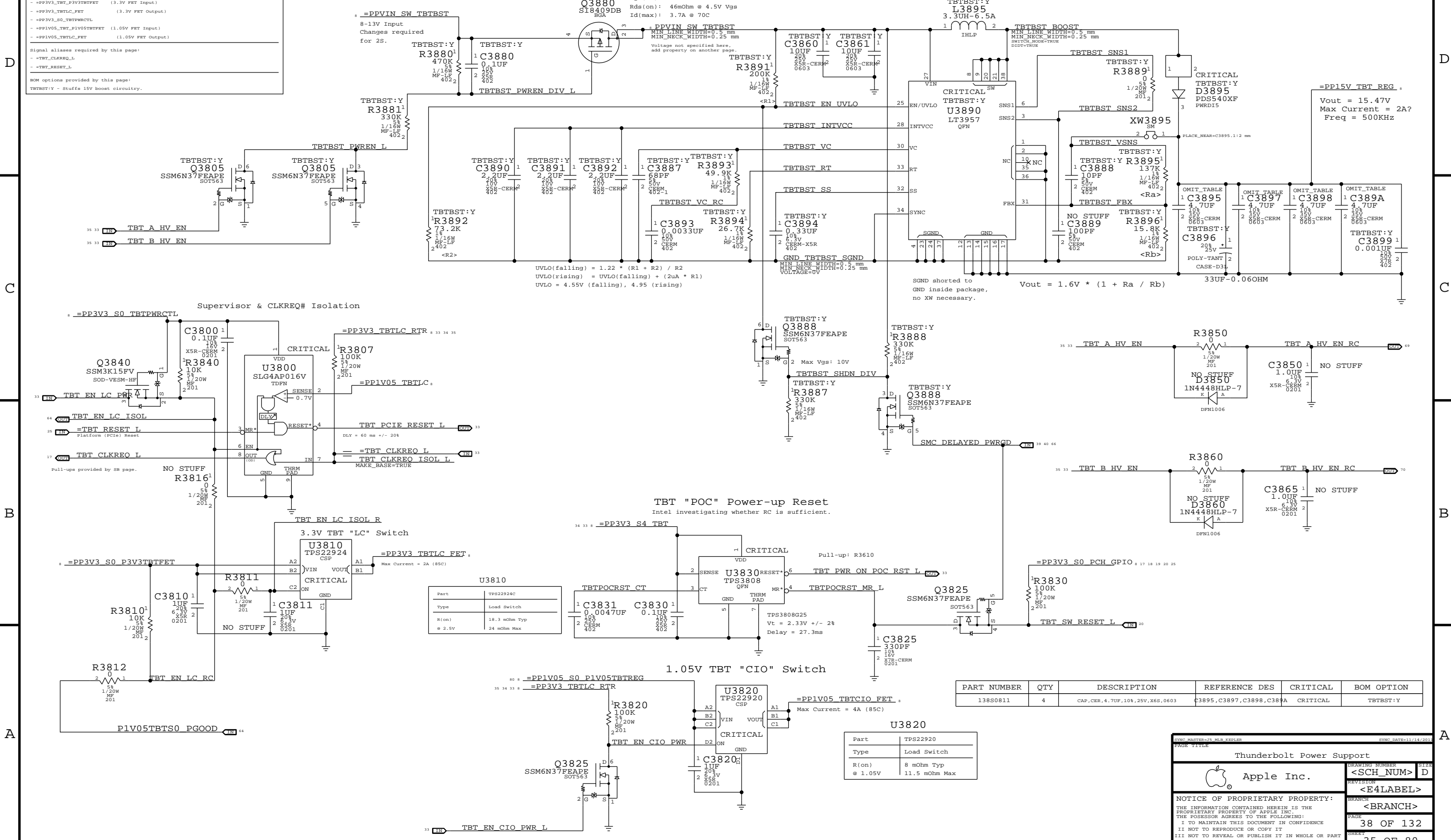
Page Notes

Power aliases required by this page:
 - =PPVIN_SW_TBTBST (8-13V Boost Input)
 - =PP15V_TBT_REG (15V Boost Output)
 - =PP3V3_TBT_P3V3TBTFTET (3.3V FET Input)
 - =PP3V3_TBTLC_FET (3.3V FET Output)
 - =PP3V3_S0_TBTBWRCTL
 - =PP1V05_TBT_P1V05TBTFTET (1.05V FET Input)
 - =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
 - =TBT_CLKREQ_L
 - =TBT_RESET_L

BOM options provided by this page:
 TBTBST:Y - Stuffs 15V boost circuitry.

Thunderbolt 15V Boost Regulator



U3810

Part	TPS22924C
Type	Load Switch
R(on)	18.3 mOhm Typ @ 2.5V
	24 mOhm Max

U3820

Part	TPS22920
Type	Load Switch
R(on)	8 mOhm Typ @ 1.05V
	11.5 mOhm Max

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
13890811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C3895,C3897,C3898,C3899	CRITICAL	TBTBST:Y

Thunderbolt Power Support

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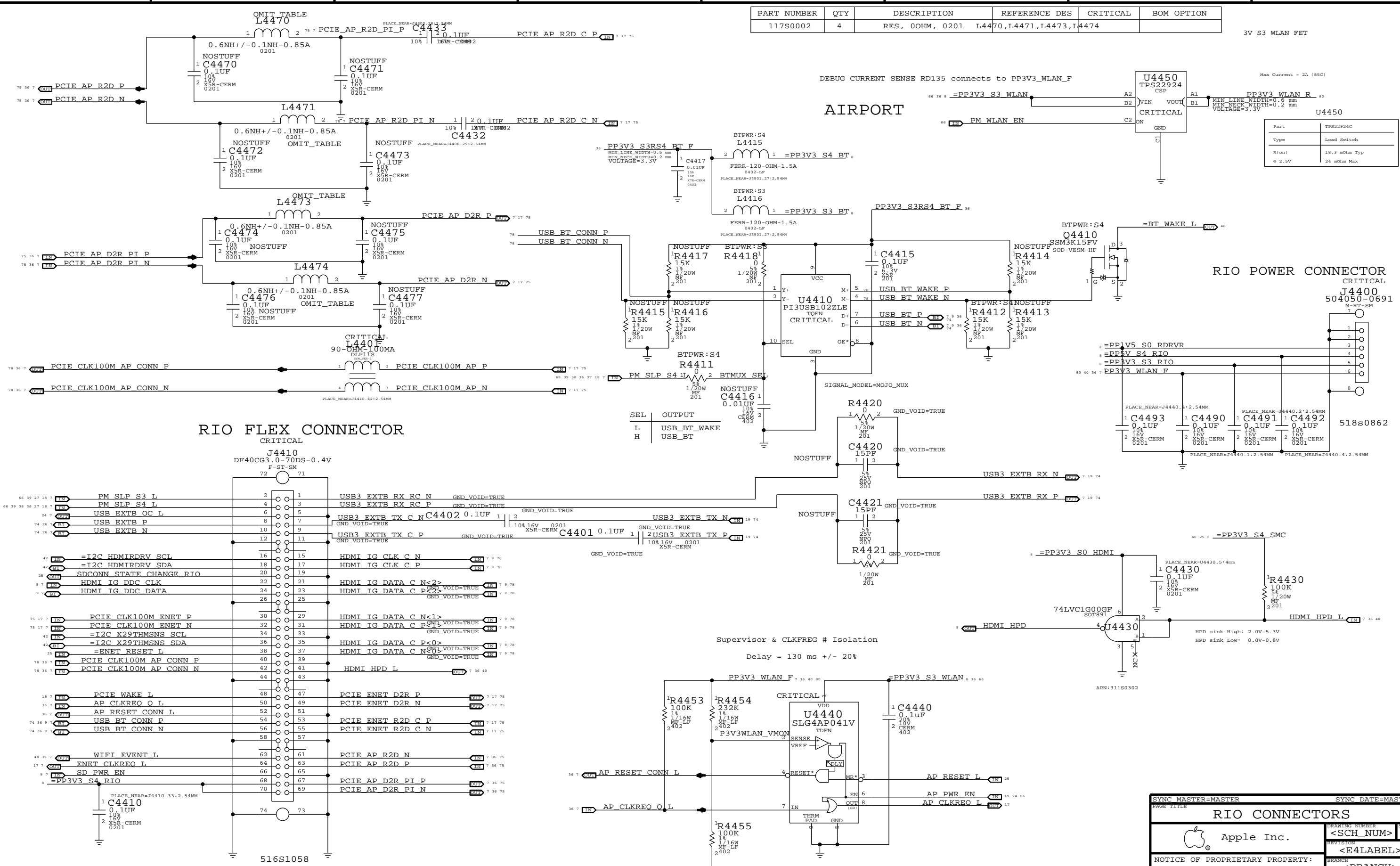
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 00HM, 0201	L4470,L4471,L4473,L4474		

3V S3 WLAN FET

AIRPORT

RIO POWER CONNECTOR

RIO FLEX CONNECTOR



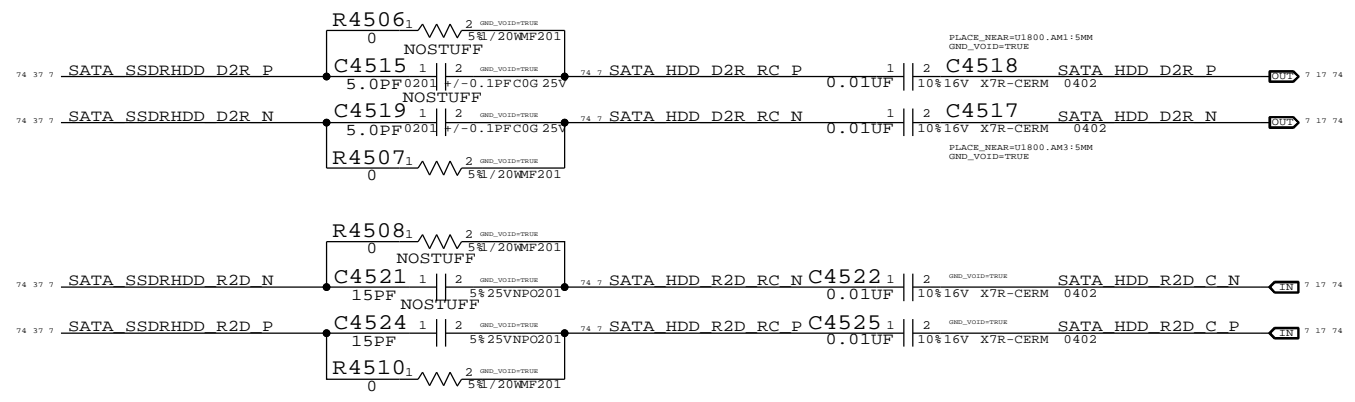
*NOTE: This connector is shielded 70P Hirose Receptacle.

Note: This receptacle mates with the plug with APN 998-4708.

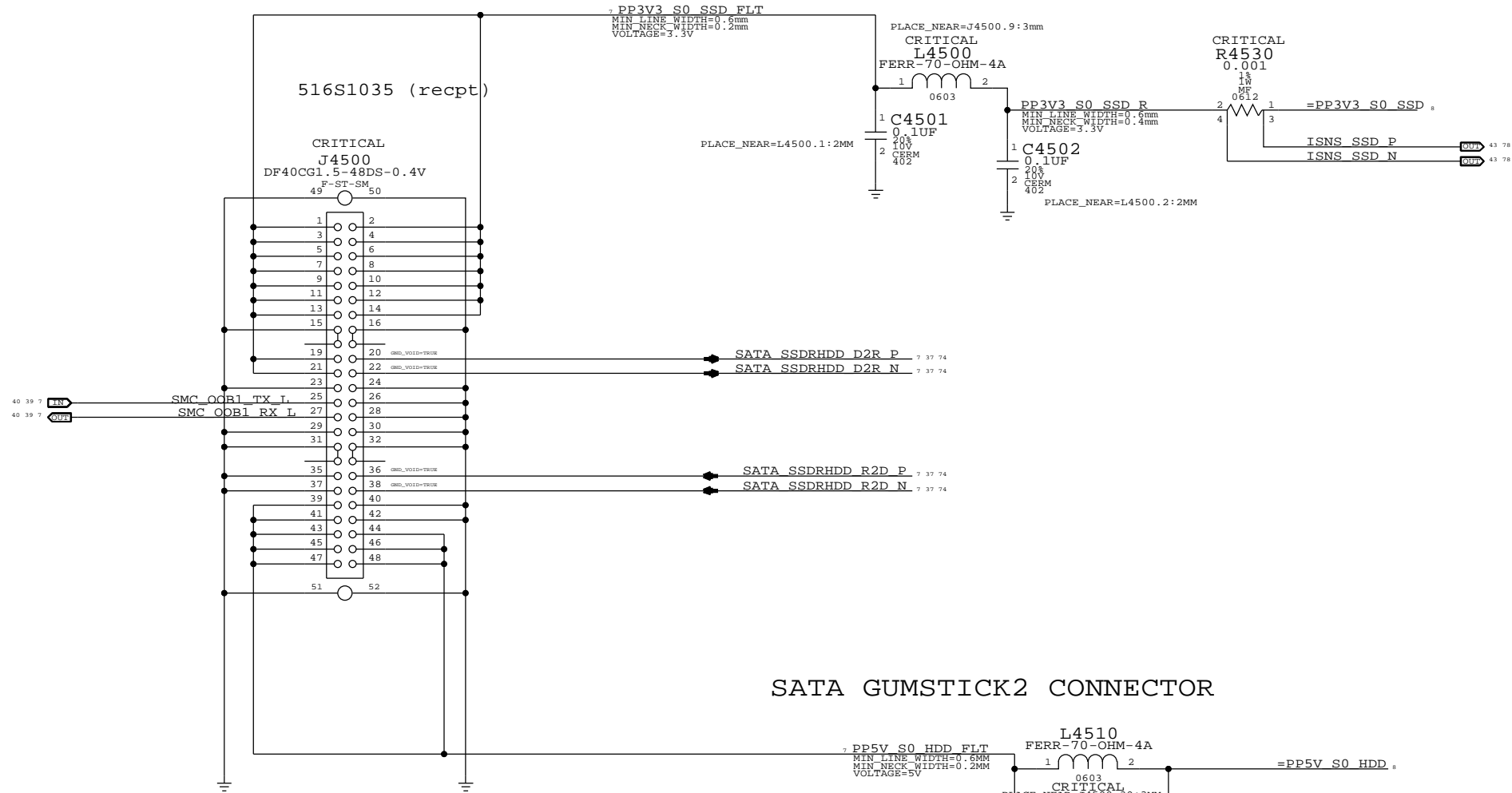
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Apple Inc.		<SCH_NUM>	D
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		BRANCH	<BRANCH>
		PAGE	44 OF 132
		SHEET	36 OF 80

C4518 & C4517 Placement Note:
 It is critical that these two should be near
 to U1800 pin AM1 and AM3.

D2R Passive DeEmphasis
 VALUE: 0.0 DB

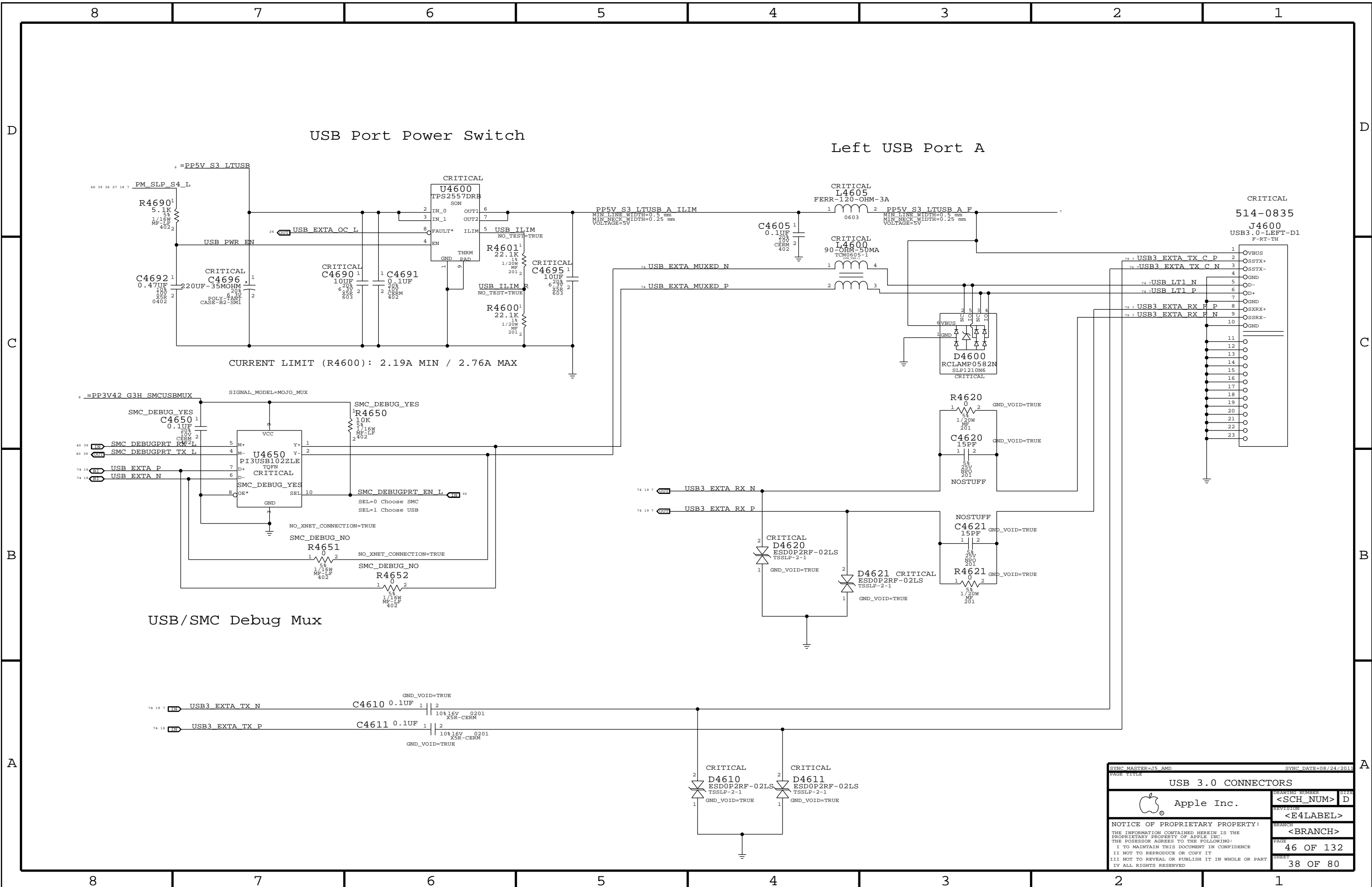


R2D Passive DeEmphasis
 VALUE: 0.0 DB



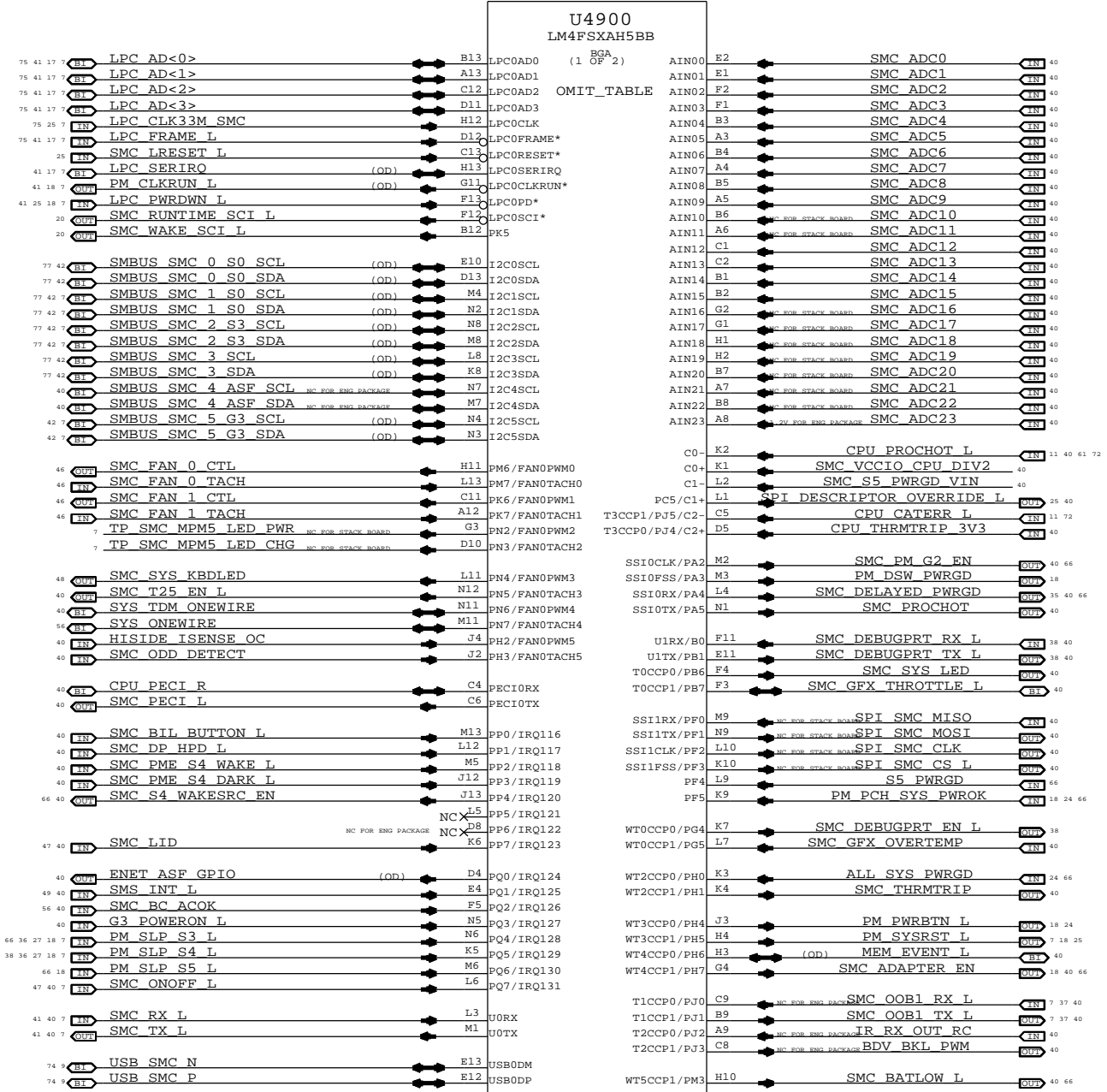
SATA GUMSTICK2 CONNECTOR

SYNC MASTER=MASTER		SYNC DATE=MASTER	
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SSD/HDD Connectors			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	45 OF 132
		SHEET	37 OF 80

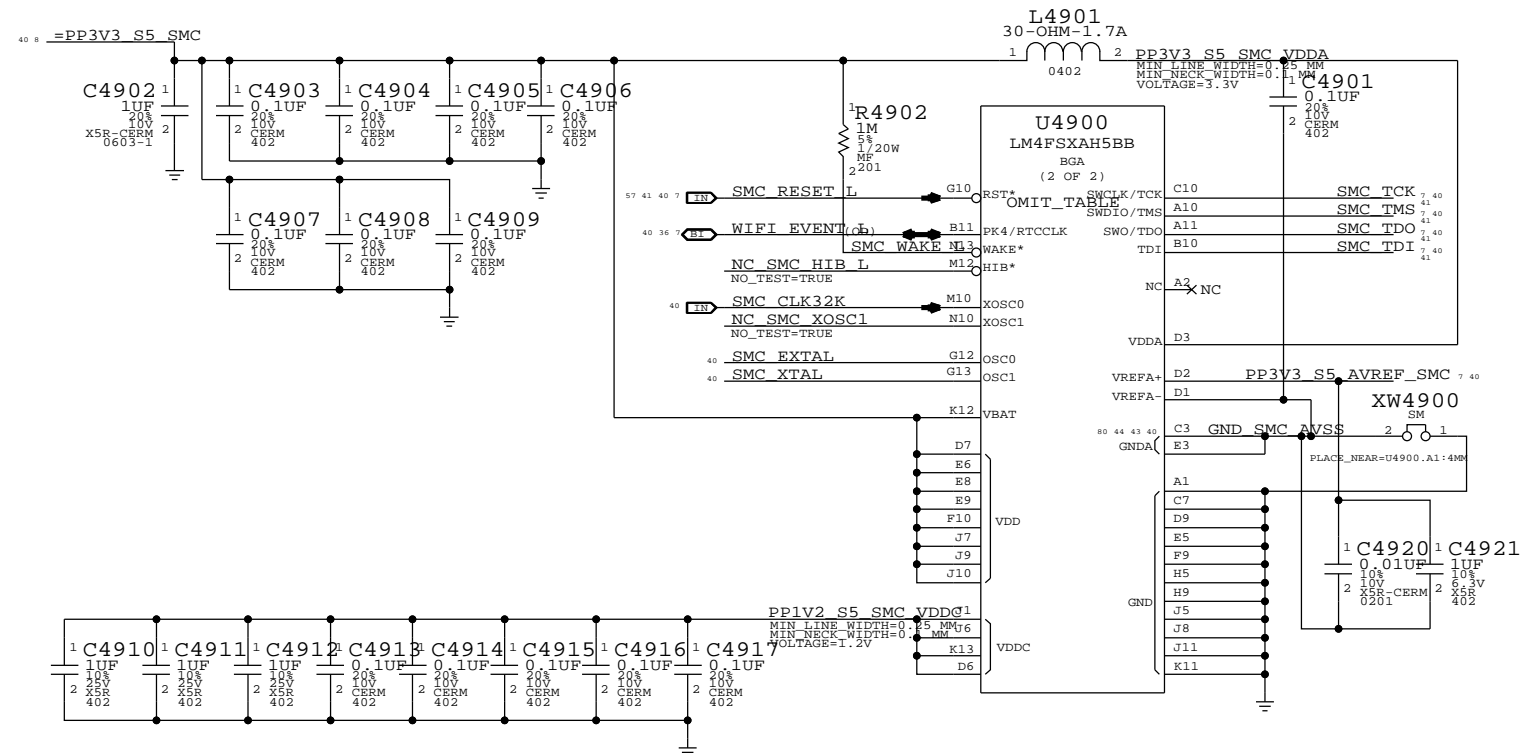


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USB 3.0 CONNECTORS			
Apple Inc.	DRAWING NUMBER	<SCH_NUM> D	
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	PAGE	46 OF 132	
	SHEET	38 OF 80	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

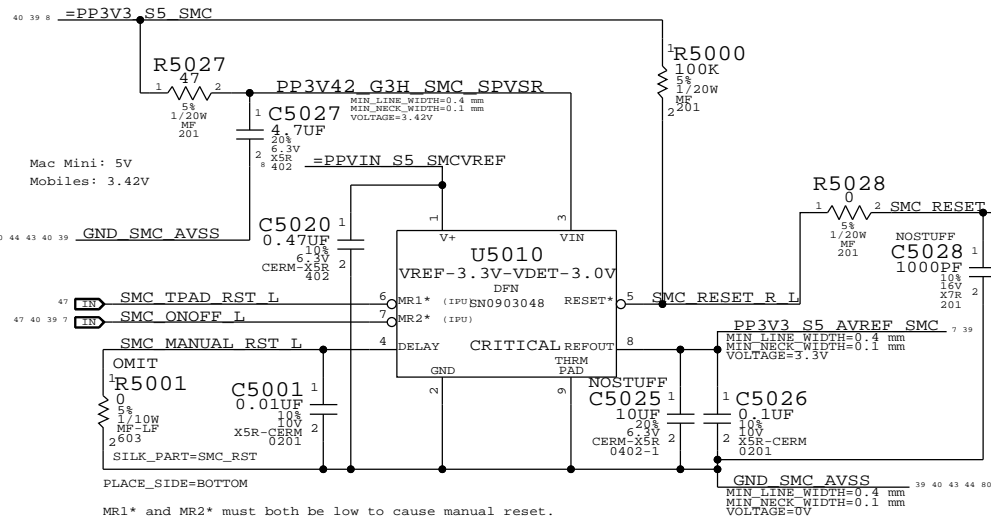


NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



SYNC MASTER=D1 SENSORS		SYNC DATE=02/20/2012	
PAGE TITLE			
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
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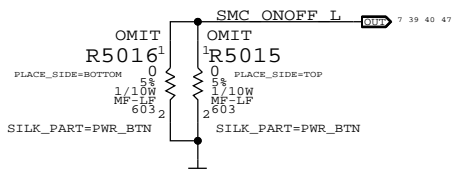
SMC Reset "Button", Supervisor & AVREF Supply



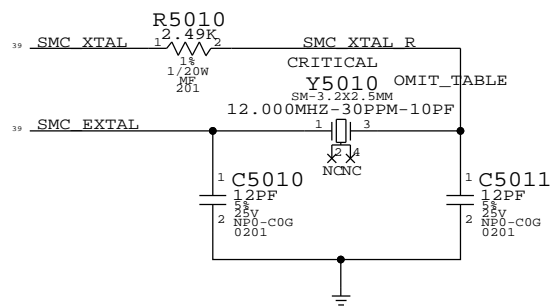
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



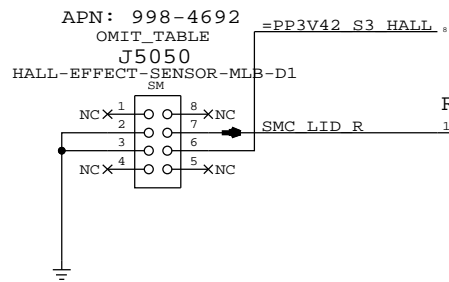
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES: 5,6,8,10,12,16,18,20,24,25 MHz

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,90C	Y5010	CRITICAL	

Hall Effect pads

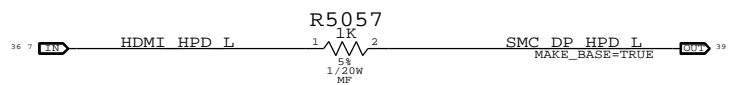


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

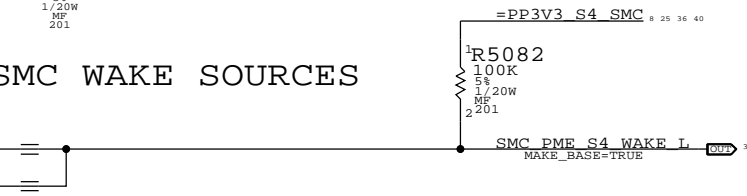
639-3261 (J4 Hall effect board) reports to 607-9320

- 54 =CHGR_ACOK = SMC_BC_ACOK
- 54 =HISIDE_ISENSE_OC = NC_HISIDE_ISENSE_OC
- 39 SMC_ADC0 = SMC_CPU_VSENSE
- 39 SMC_ADC1 = SMC_CPU_ISENSE
- 39 SMC_ADC2 = NC_SMC_GPU_HI_ISENSE
- 39 SMC_ADC3 = SMC_DCIN_VSENSE
- 39 SMC_ADC4 = SMC_DCIN_ISENSE
- 39 SMC_ADC5 = SMC_PBUS_VSENSE
- 39 SMC_ADC6 = SMC_SSD_ISENSE
- 39 SMC_ADC7 = SMC_CPU_HI_ISENSE
- 39 SMC_ADC8 = SMC_OTHER_HI_ISENSE
- 39 SMC_ADC9 = SMC_MEM_ISENSE
- 39 SMC_ADC10 = SMC_VCCIO_ISENSE
- 39 SMC_ADC11 = SMC_VCCIO_ISENSE
- 39 SMC_ADC12 = SMC_AXG_VSENSE
- 39 SMC_ADC13 = SMC_CPU_SA_ISENSE
- 39 SMC_ADC14 = SMC_CPU_SA_VSENSE
- 39 SMC_ADC15 = SMC_LCD_PANEL_ISENSE
- 39 SMC_ADC16 = SMC_LCDKLT_VSENSE
- 39 SMC_ADC17 = SMC_LCDKLT_ISENSE
- 39 SMC_ADC18 = SMC_AXG_ISENSE
- 39 SMC_ADC19 = NC_SMC_GPU_PLV35_ISENSE
- 39 SMC_ADC20 = SMC_T25_ISENSE
- 39 SMC_ADC21 = NC_SMC_PCH_CORE_ISENSE
- 39 SMC_ADC22 = SMC_X29_ISENSE
- 39 SMC_ADC23 = SMC_TBT_ISENSE
- 39 SMBUS_SMC_4_ASF_SCL = NC_SMBUS_SMC_4_ASF_SCL
- 39 SMBUS_SMC_4_ASF_SDA = NC_SMBUS_SMC_4_ASF_SDA
- 39 BDV_BKL_PWM = NC_BDV_BKL_PWM
- 39 SMC_PME_S4_DARK_L = SDCONN_STATE_CHANGE_SMC
- =TBT_WAKE_L

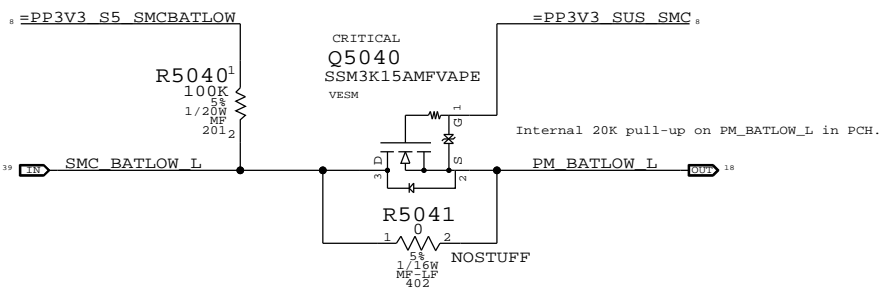
HDMI HPD ESD PROTECTION



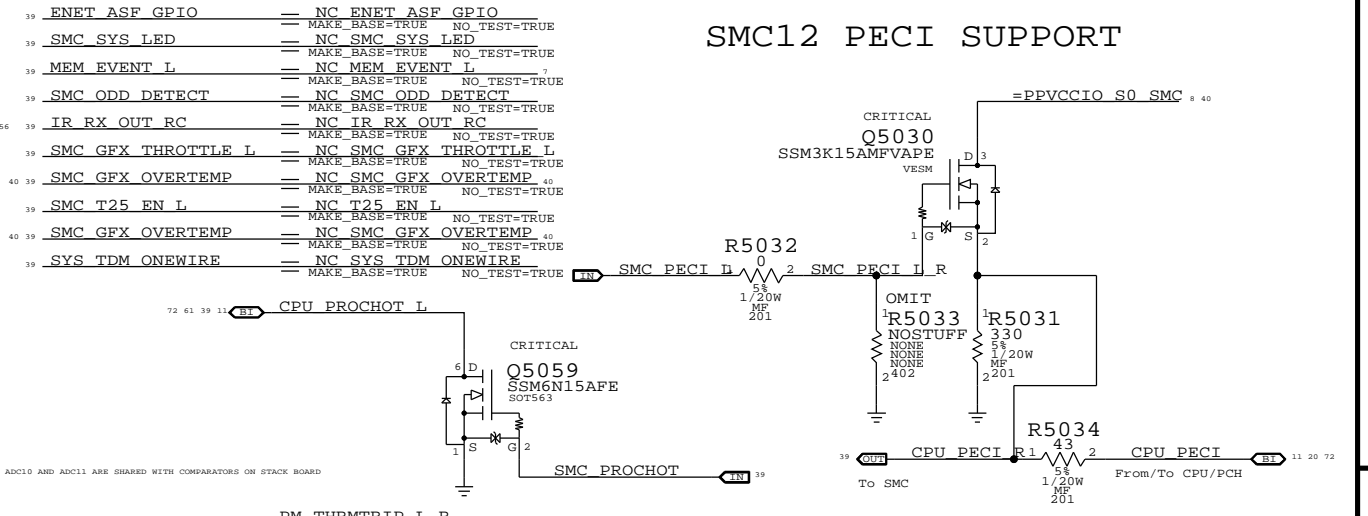
S4 SMC WAKE SOURCES



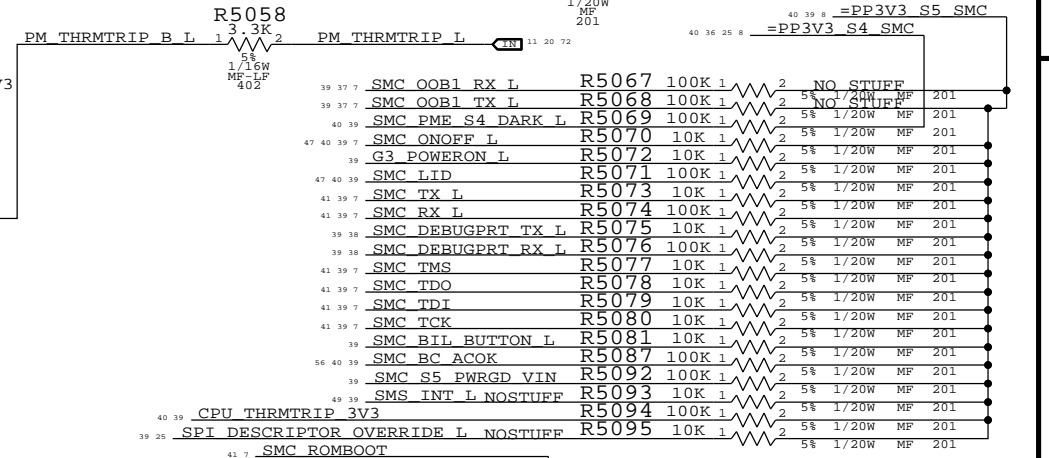
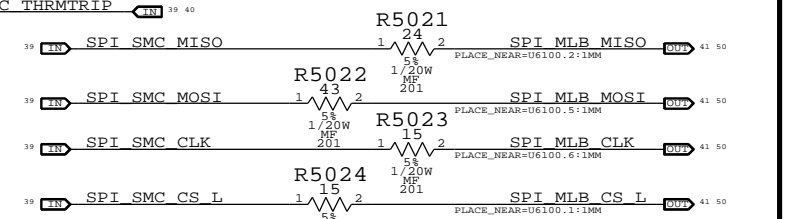
BATLOW# ISOLATION



SMC12 PECCI SUPPORT



SMC12 SPI SUPPORT

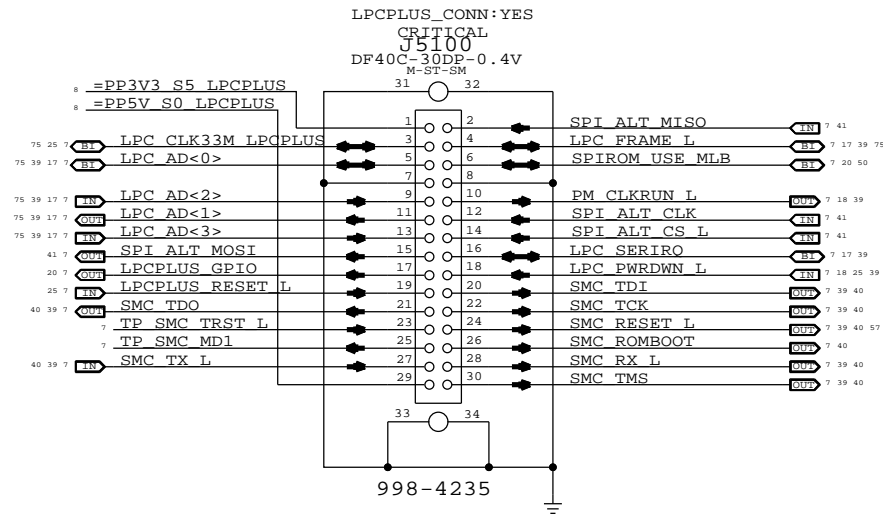


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D

D

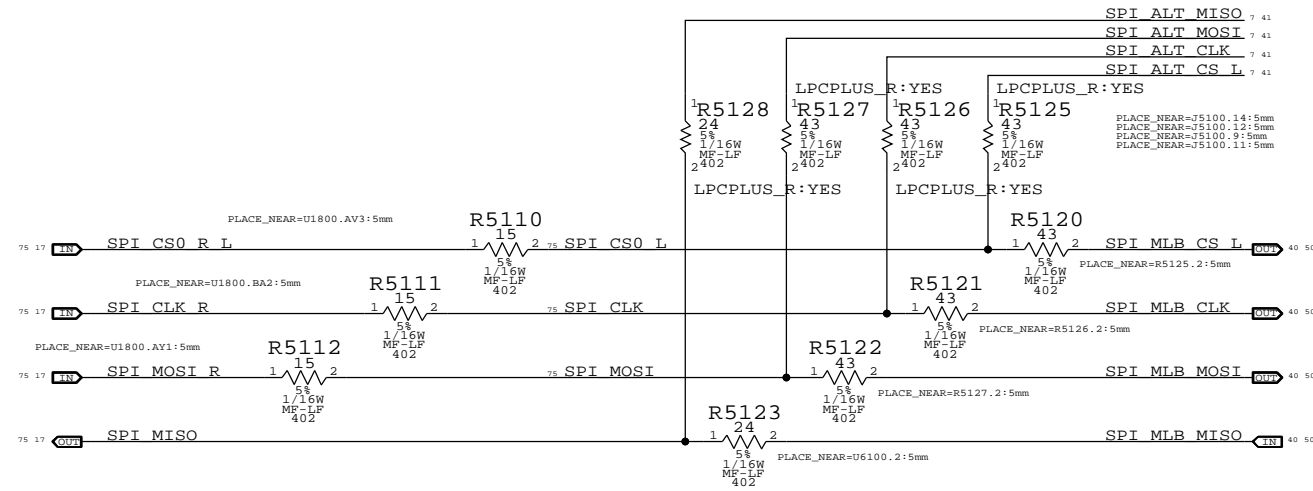
LPC+SPI Connector



C

C

SPI Bus Series Termination



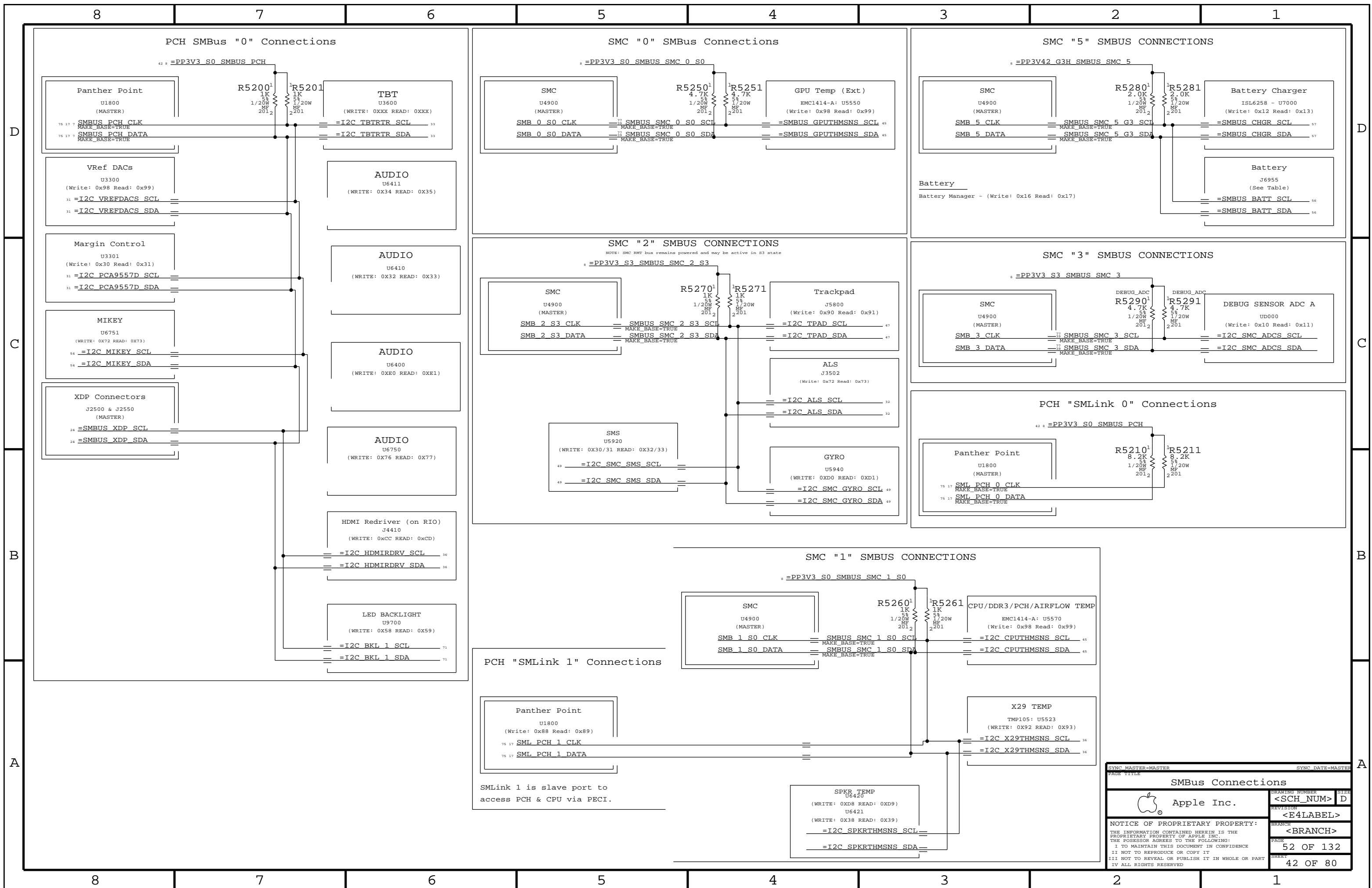
B

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A

A

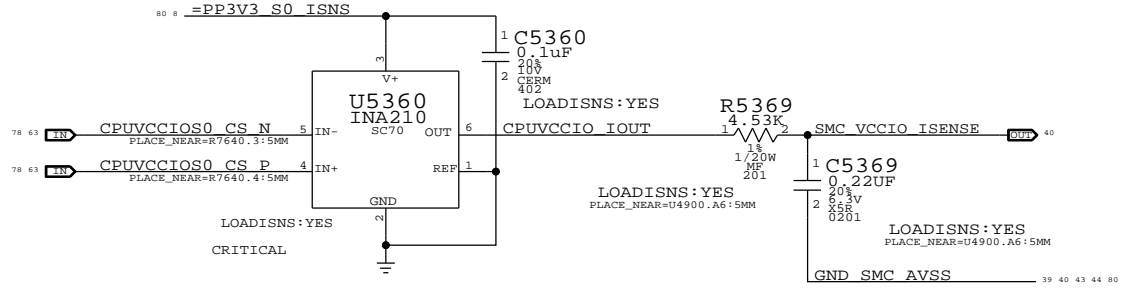
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LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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SMBus Connections			
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		PAGE	SHEET
		52 OF 132	42 OF 80

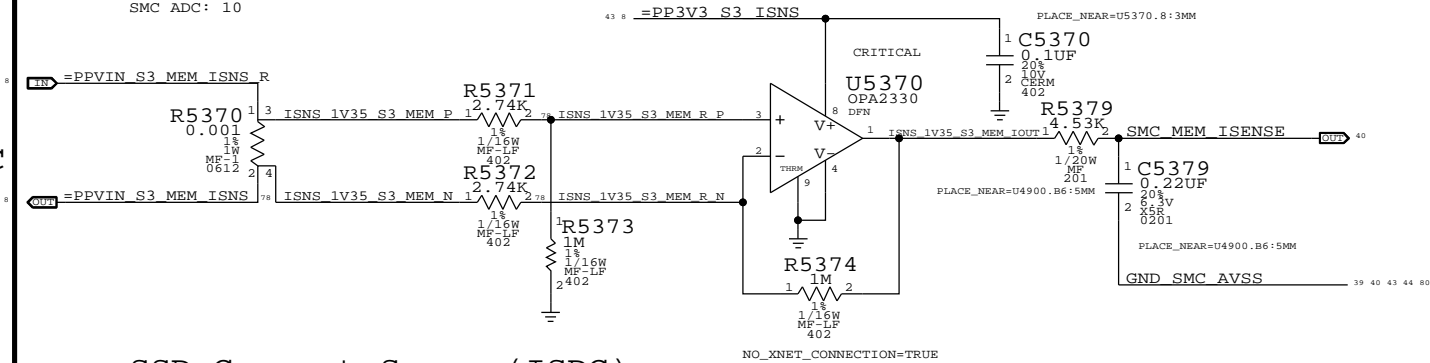
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
 Rsense: 0.001 (R7640)
 V across Rsense: 15 mV
 SMC ADC: 11



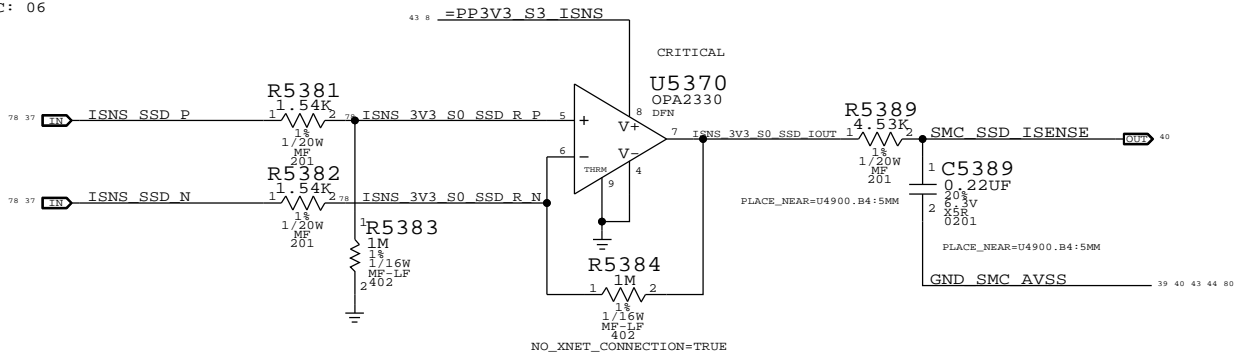
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
 Rsense: 0.001 (R5370)
 V across Rsense: 9 mV
 SMC ADC: 10



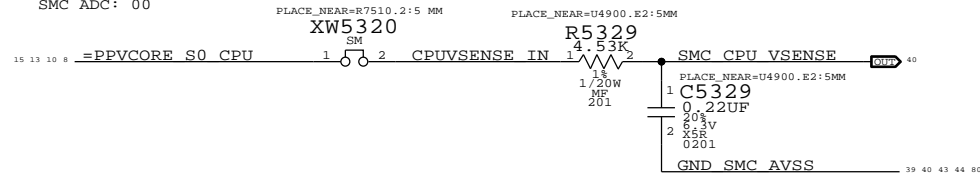
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
 Rsense: 0.001 (R5370)
 V across Rsense: 5 mV
 SMC ADC: 06



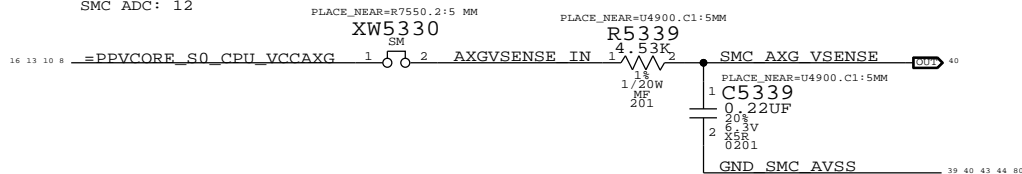
CPU Core Voltage Sense (VC0C)

Gain: 1x
 SMC ADC: 00



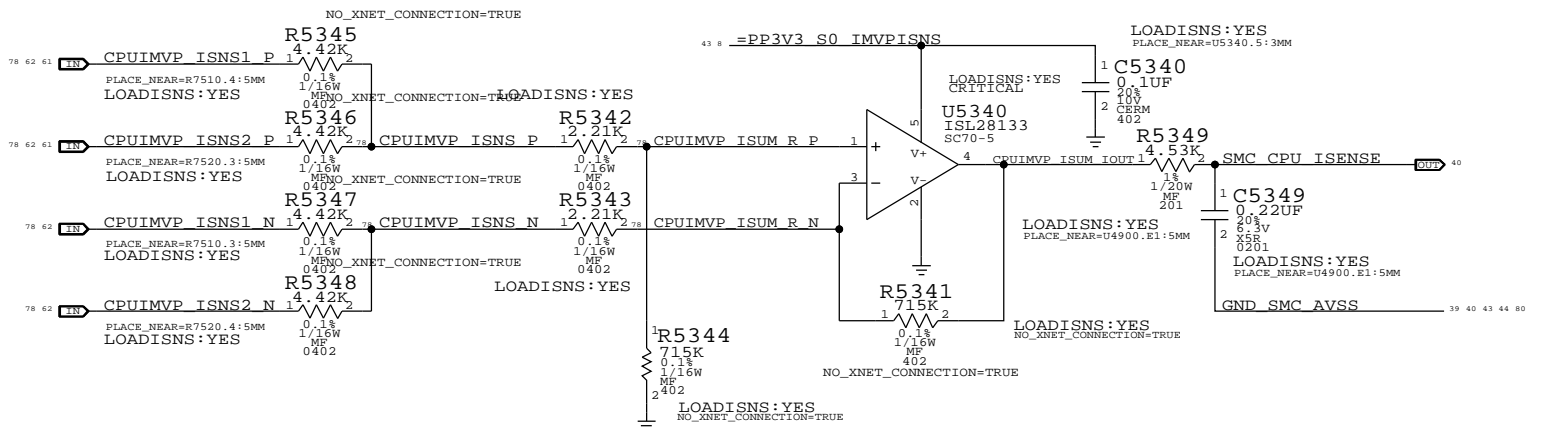
AXG Core Voltage Sense (VN0C)

Gain: 1x
 SMC ADC: 12



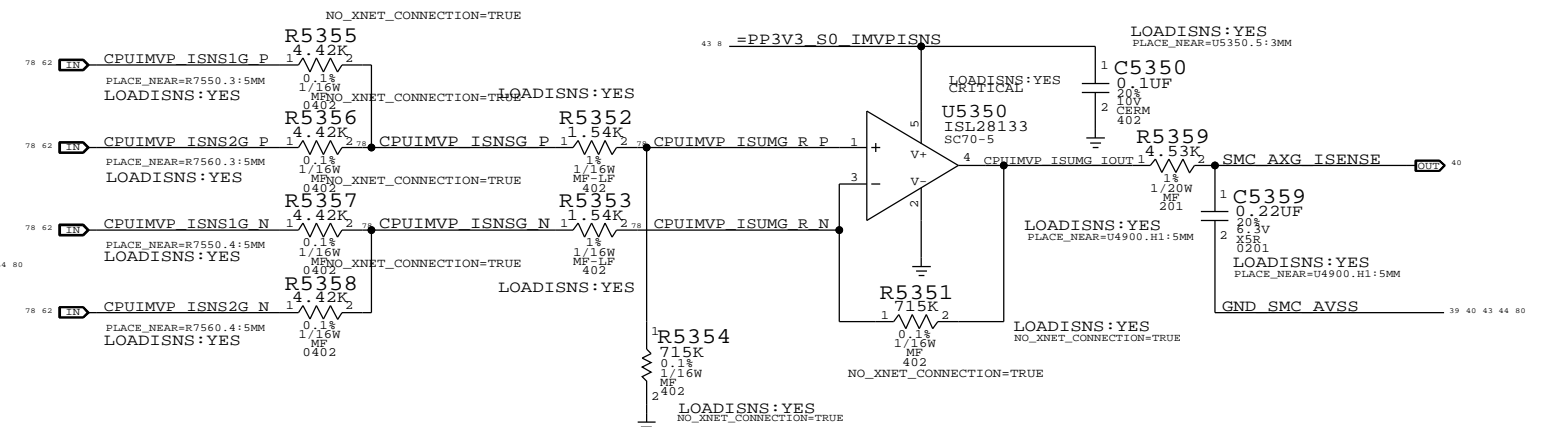
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
 Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
 V across Rsense: 19.8 mV
 SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
 Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
 V across Rsense: 17.25 mV
 SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

Power Sensor: Load Side

Apple Inc.

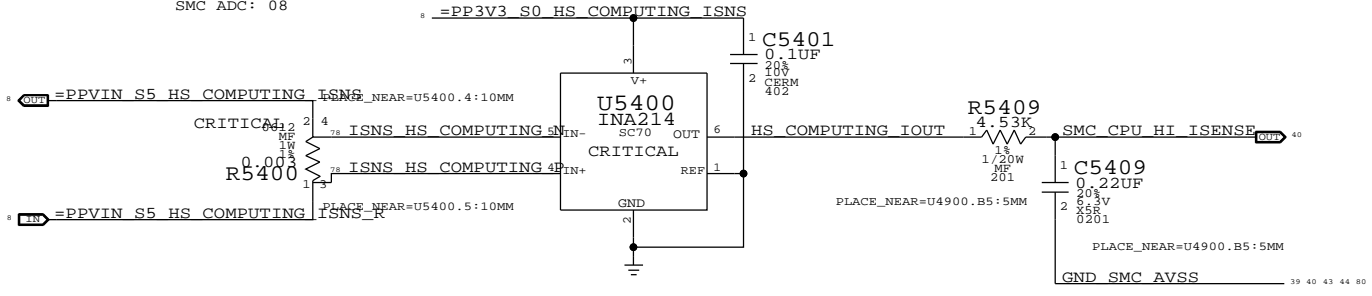
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SYNCH MASTER=D1 SENSORS SYNC DATE=02/20/2012

DRAWING NUMBER: <SCH_NUM> SIZE: D
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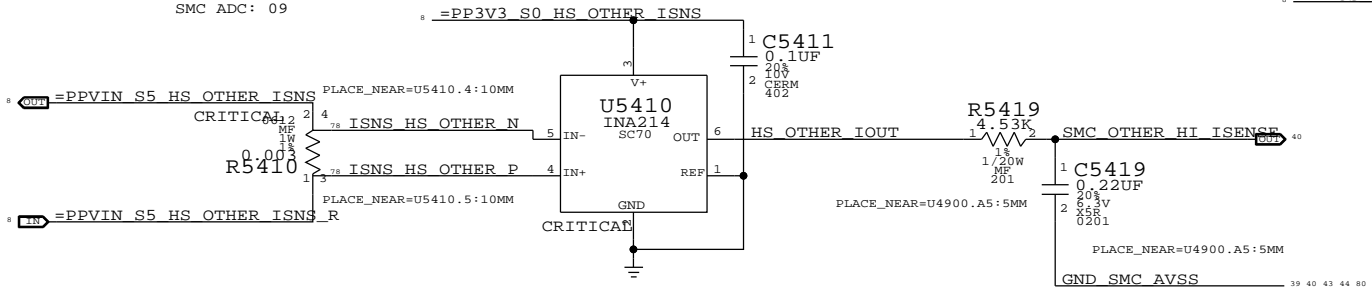
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
 Rsense: 0.003 (R5400)
 V across Rsense: 52.2 mV
 SMC ADC: 08



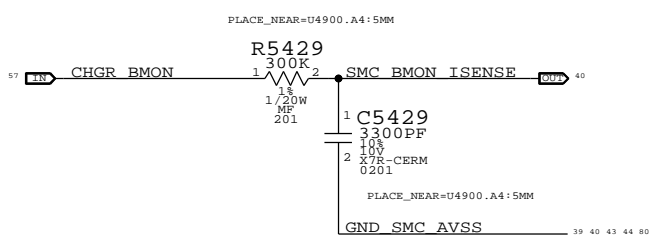
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
 Rsense: 0.003 (R5410)
 V across Rsense: 26.4 mV
 SMC ADC: 09



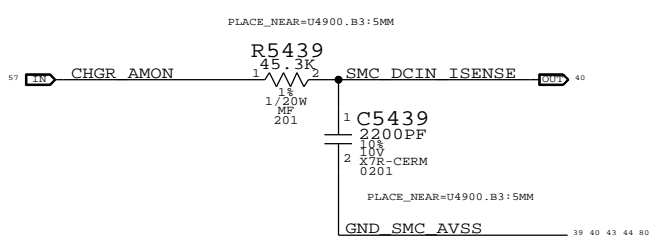
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
 Rsense: 0.010 (R7050)
 SMC ADC: 07



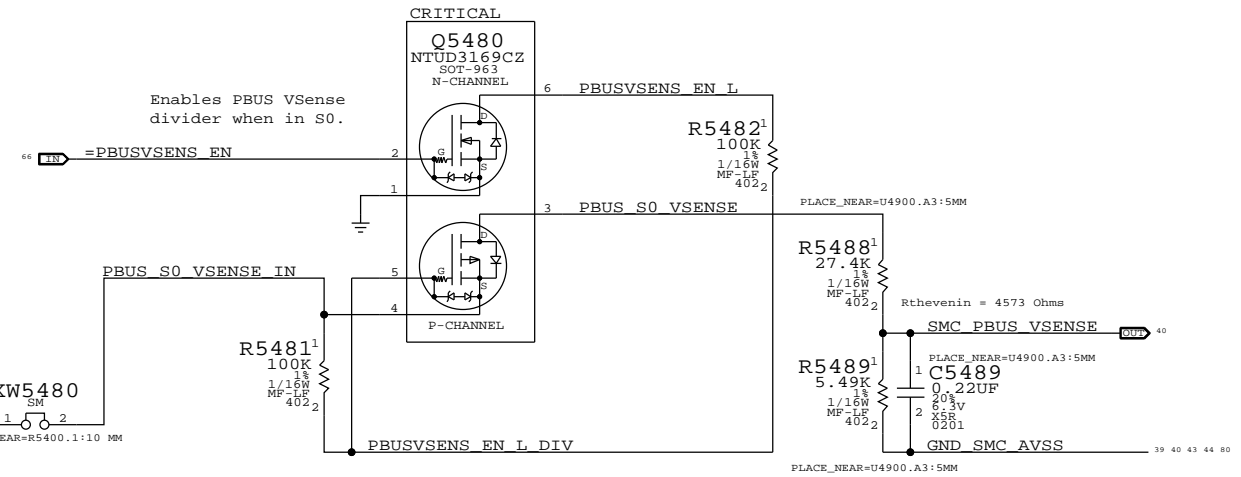
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
 Rsense: 0.020 (R7020)
 SMC ADC: 04



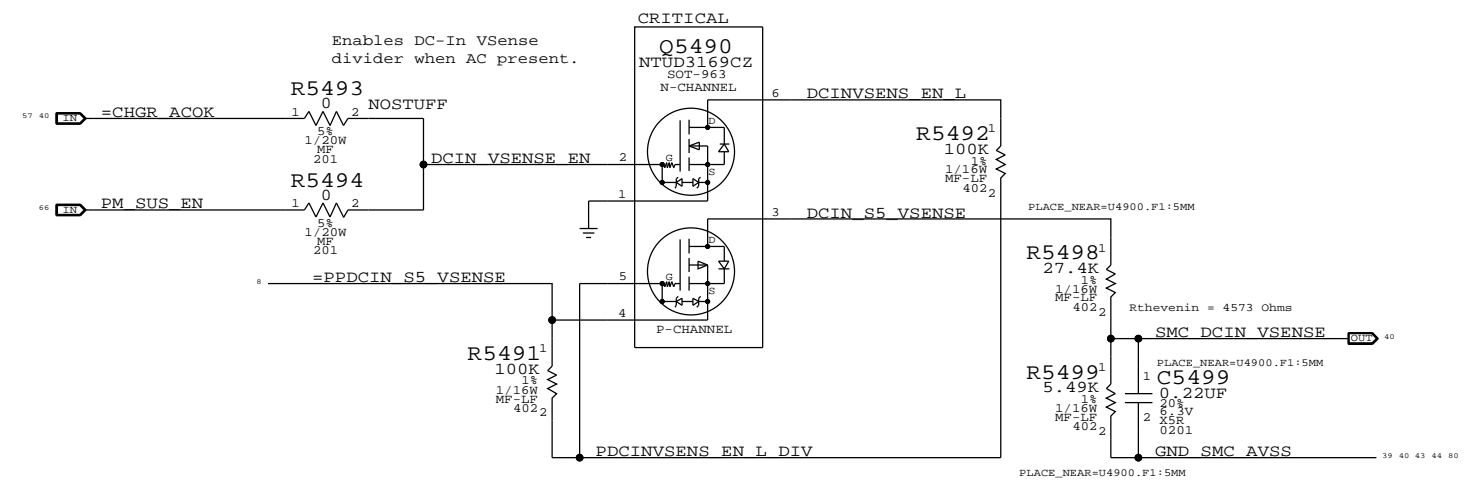
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
 SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

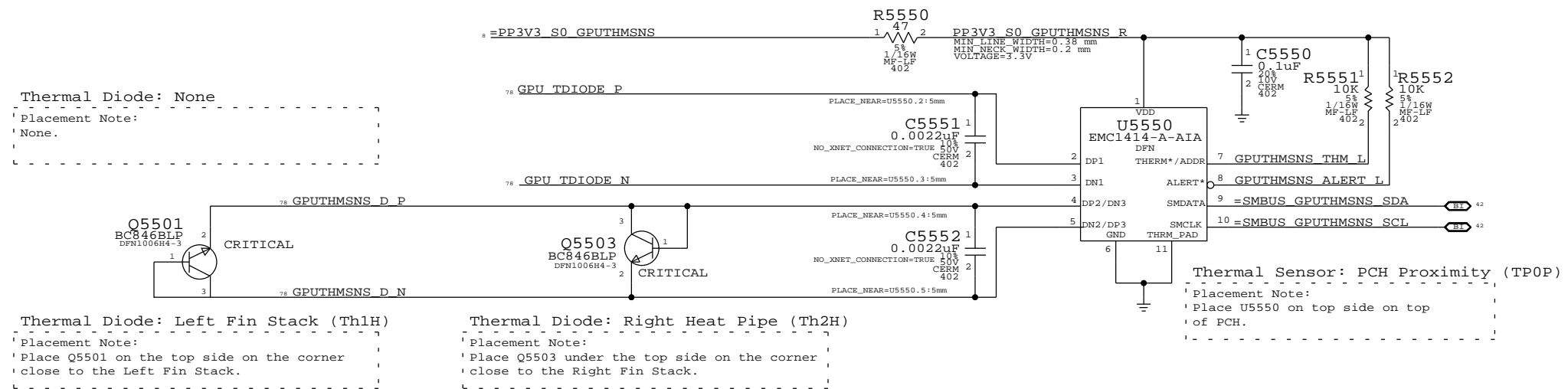
Gain: 0.167x
 SMC ADC: 03



SYNC MASTER=D1 SENSORS		SYNC DATE=02/20/2012	
Power Sensor: High Side			
Apple Inc.		DRAWING NUMBER	SIZE
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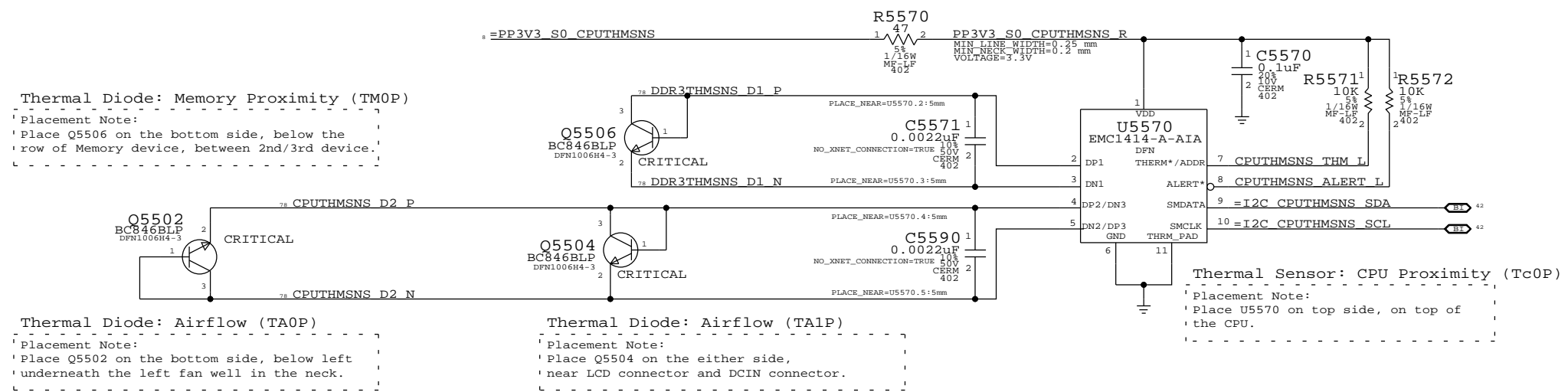
Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99

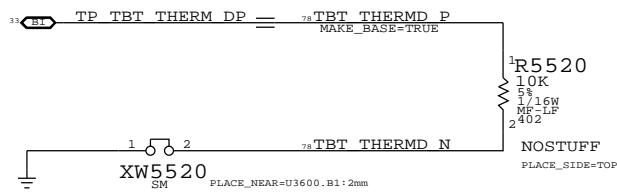


Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

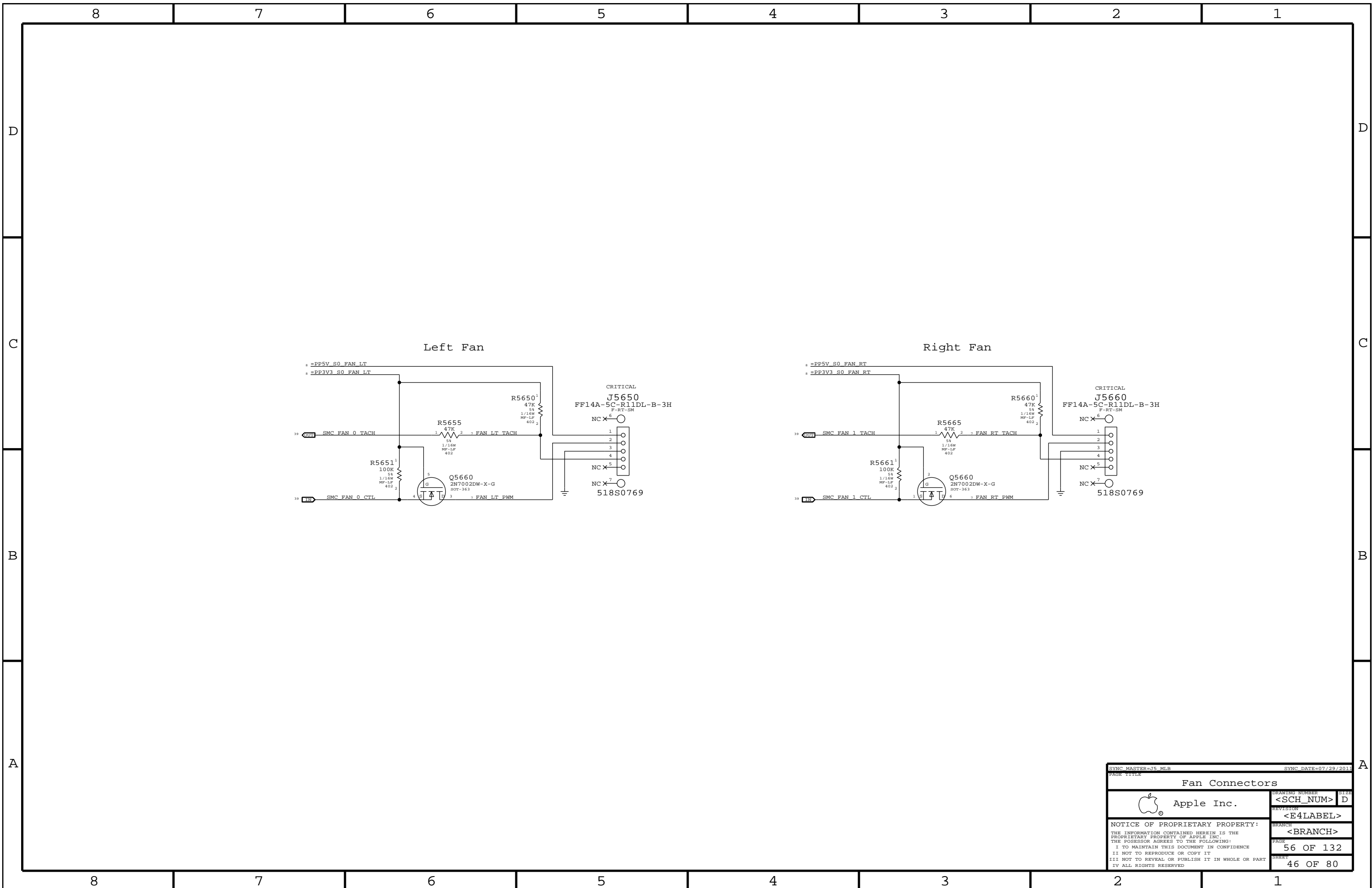
I2C Write: 0x98, I2C Read: 0x99



Thermal Sensor: T29 Die



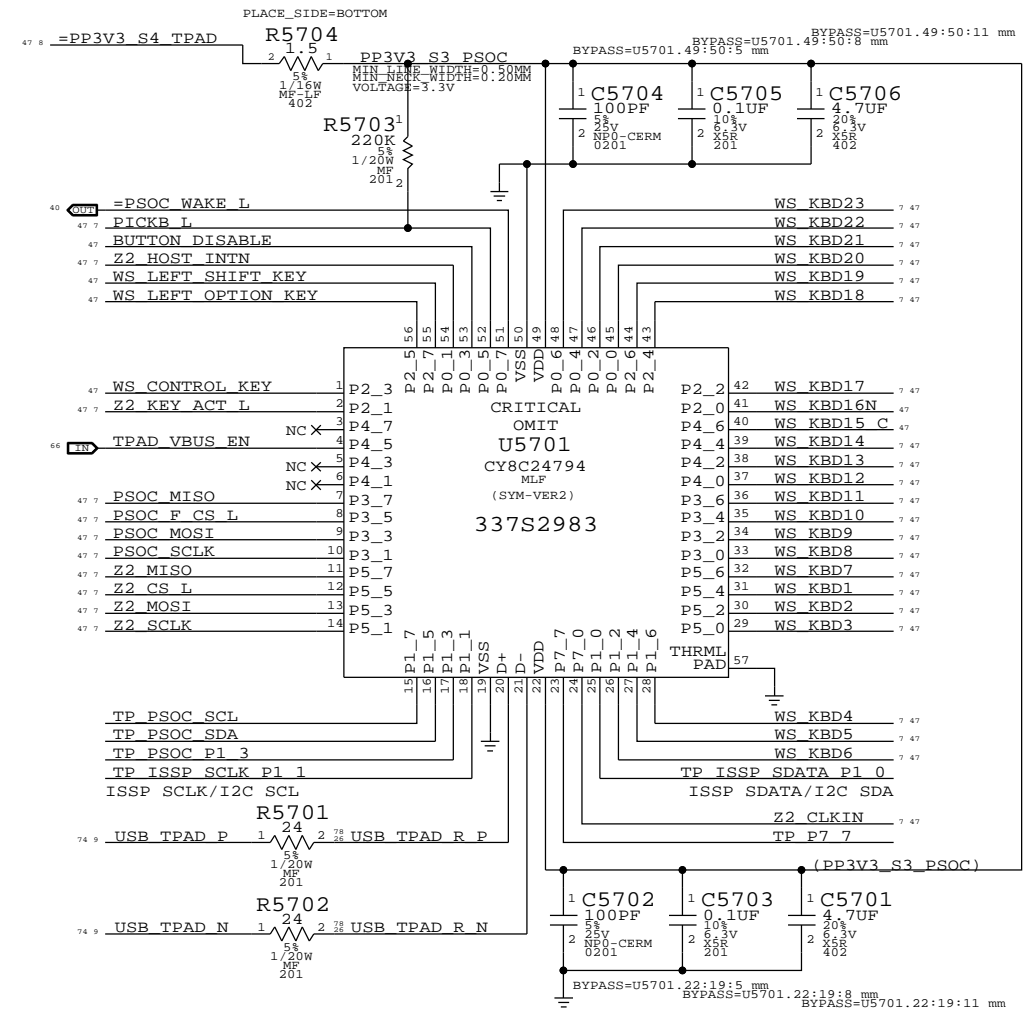
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Fan Connectors			
Apple Inc.		DRAWING NUMBER	SIZE
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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

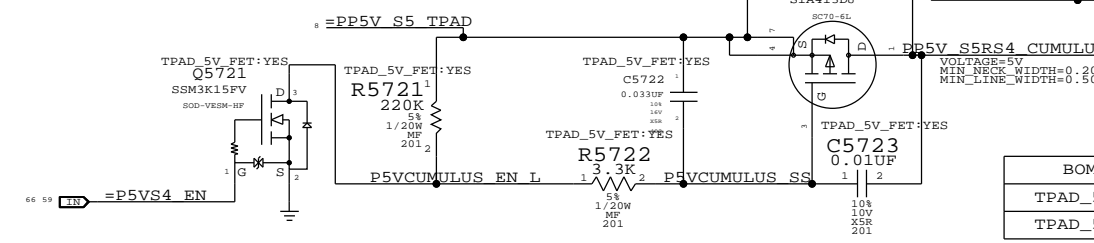


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

BOM Options available to CSA 5
 TPAD_5V:S4 Original implementation off PP5V_S4
 TPAD_5V:LDO_S4 PP5V_S5 LDO power in S4 only
 TPAD_5V:LDO_S5 PP5V_S5 LDO power

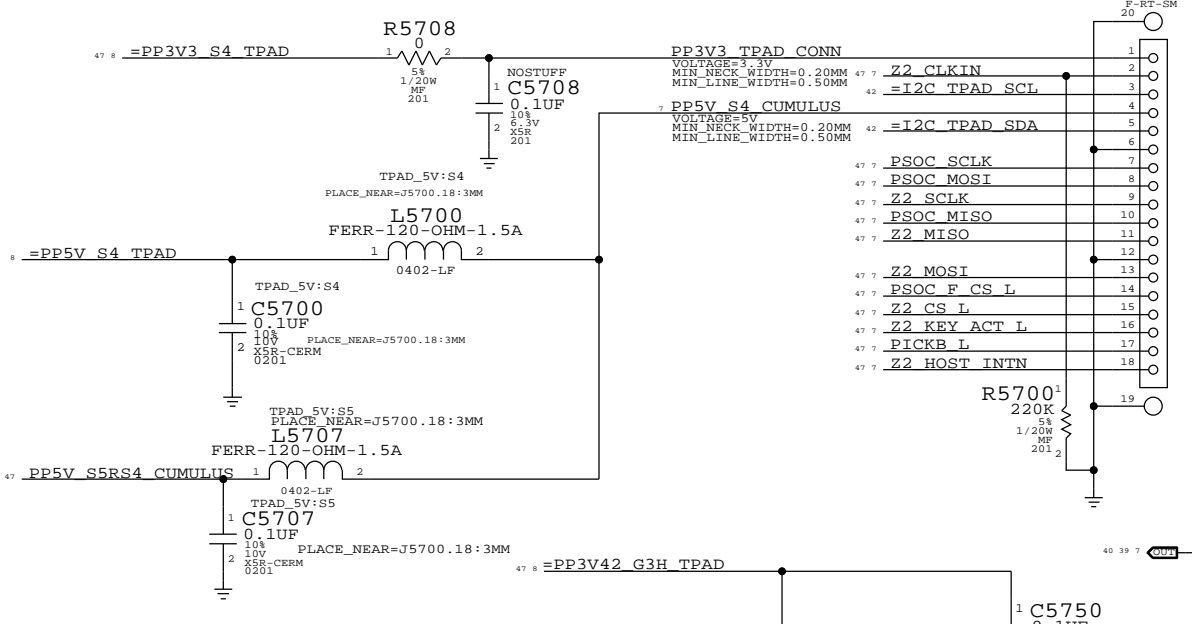
All RC values are TBD

5V TRACKPAD S4 FET



BOM GROUP	BOM OPTIONS
TPAD_5V:LDO:S4	TPAD_5V_FET: YES, TPAD_5V:S5
TPAD_5V:LDO:S5	TPAD_5V_FET:NO, TPAD_5V:S5

IPD Flex Connector

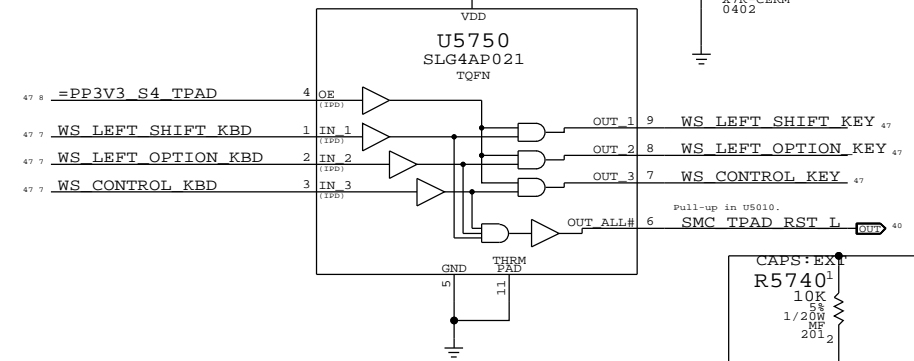
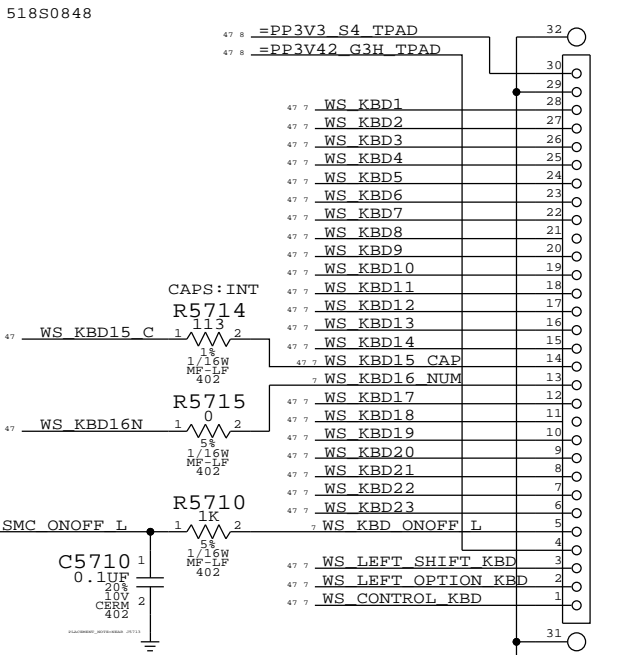


www.qdzbx.com

CRITICAL J5700

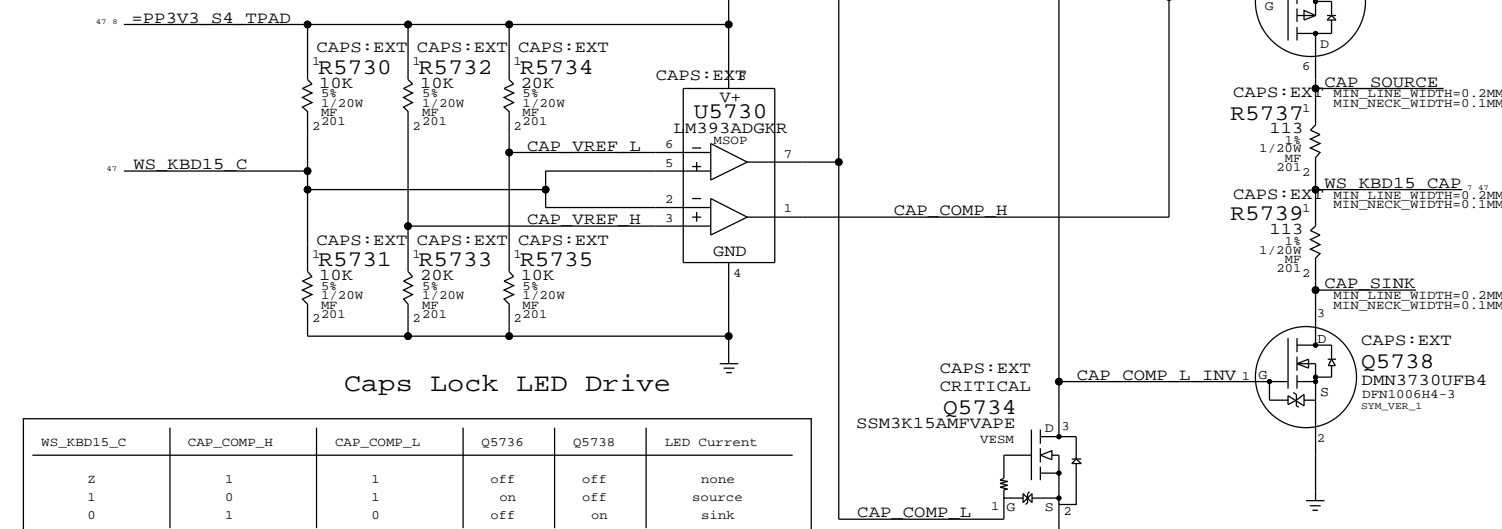
FF14-18C-R11DL

Keyboard Connector



SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDED with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



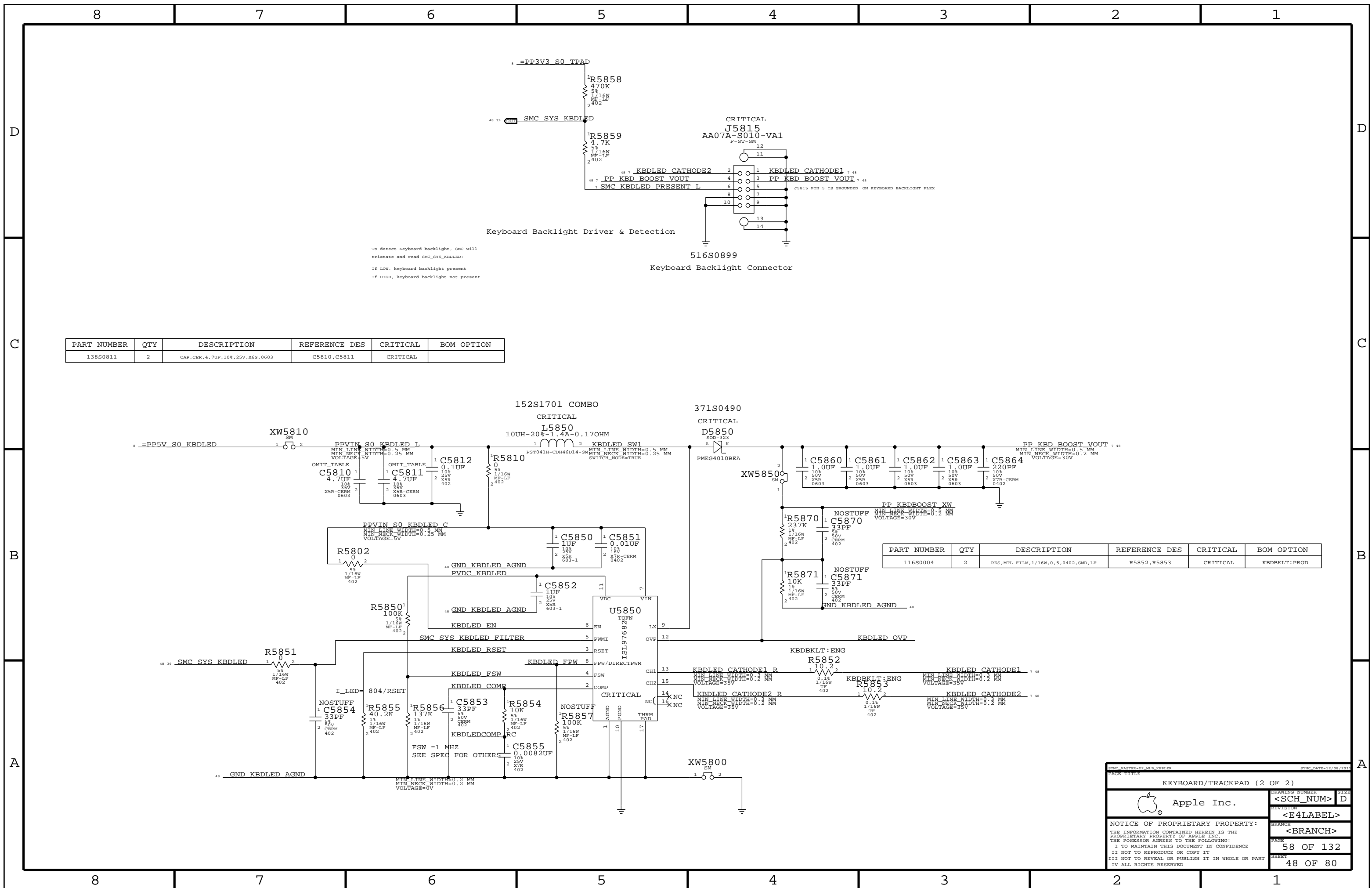
WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

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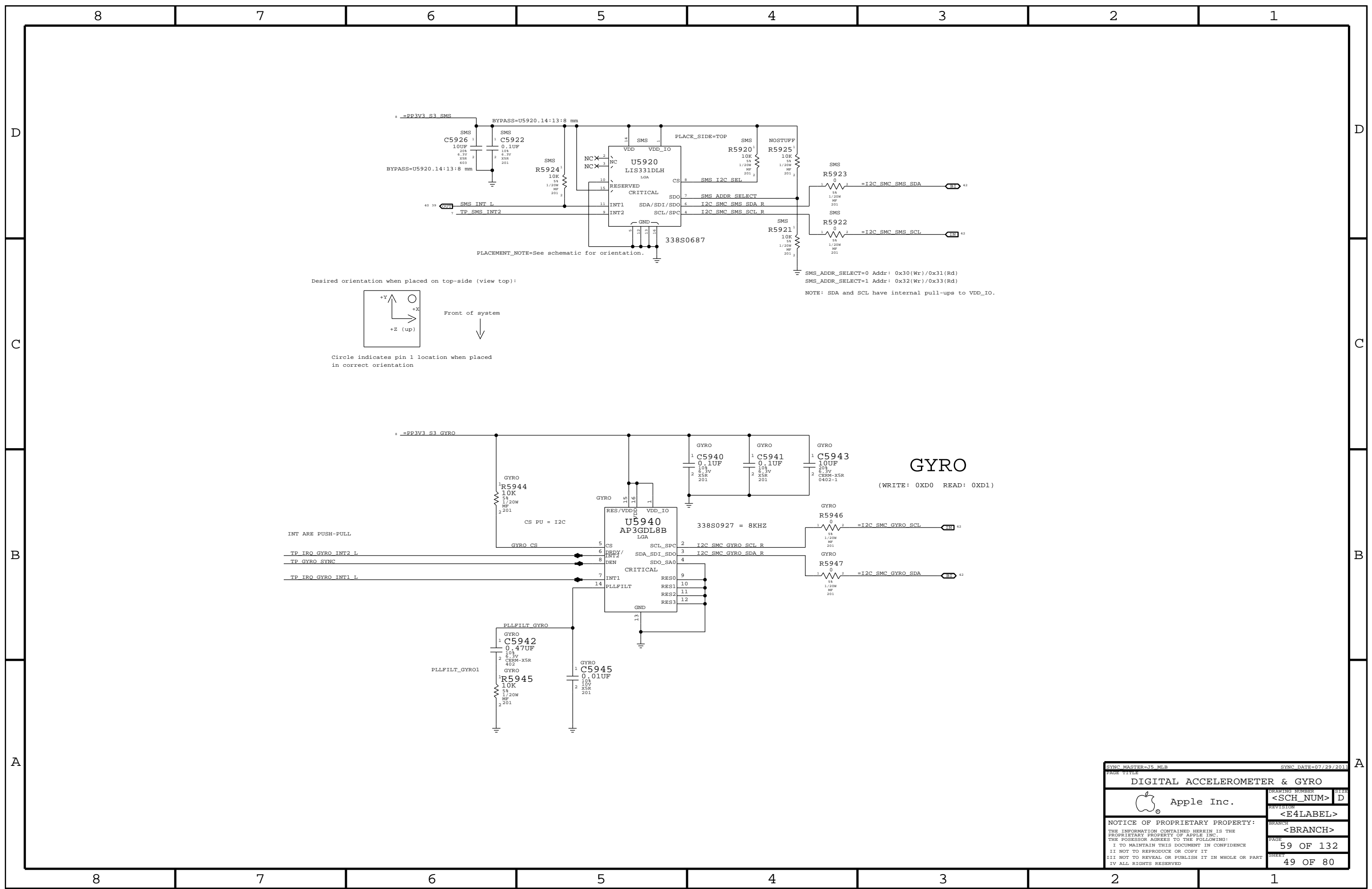
To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
 If LOW, keyboard backlight present
 If HIGH, keyboard backlight not present

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP,CER,4.7UF,10%,25V,X6S,0603	C5810,C5811	CRITICAL	

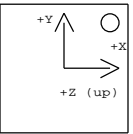
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,1/16W,0.5,0402,SMD,LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

SYMC PART#=00_MLB_KEYPAD SYMC DATE=12/08/2011
 PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)
 Apple Inc.
 DRAWING NUMBER <SCH_NUM> D
 REVISION <E4LABEL>
 BRANCH <BRANCH>
 PAGE 58 OF 132
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Desired orientation when placed on top-side (view top):

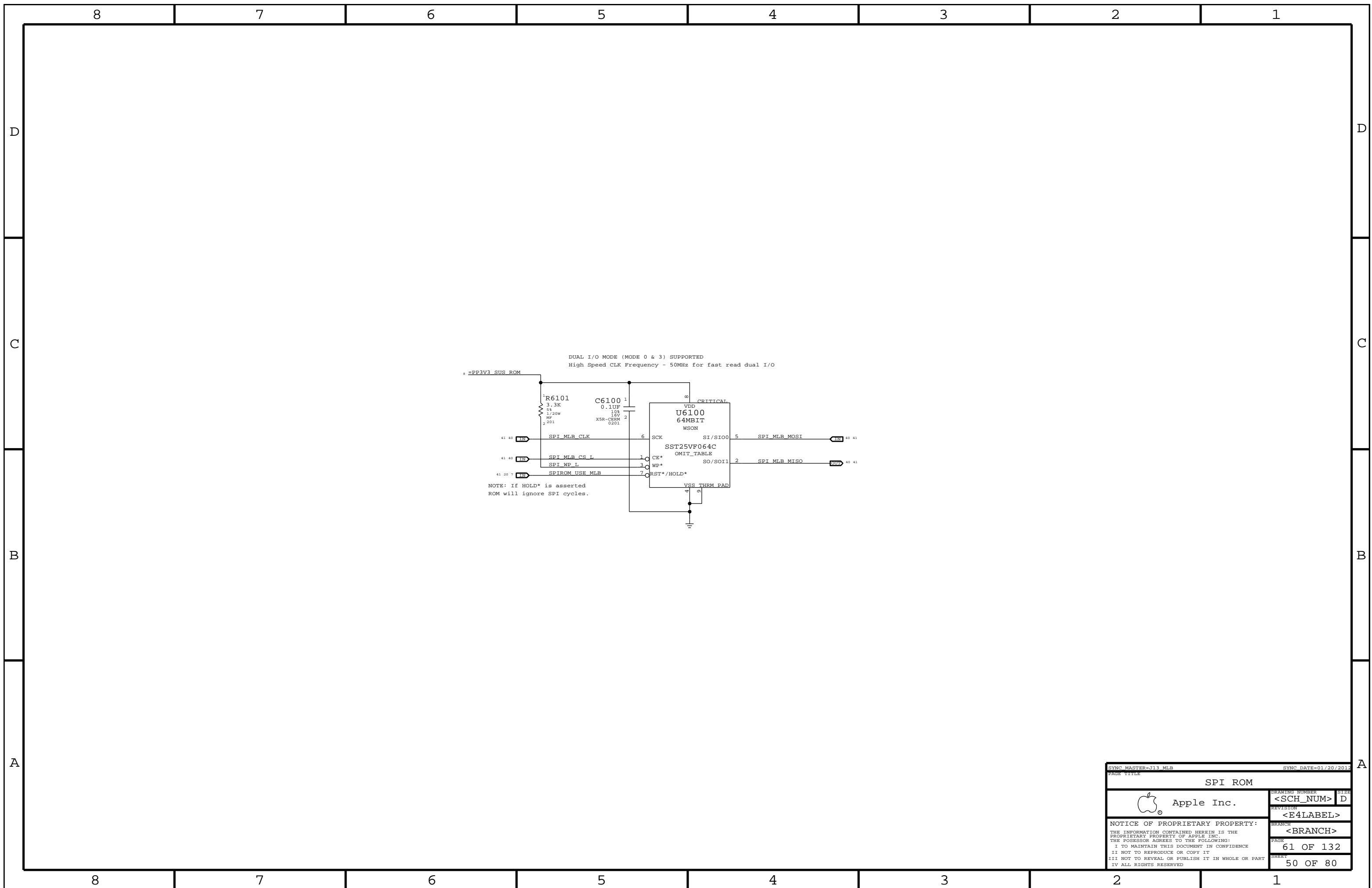


Circle indicates pin 1 location when placed in correct orientation

GYRO

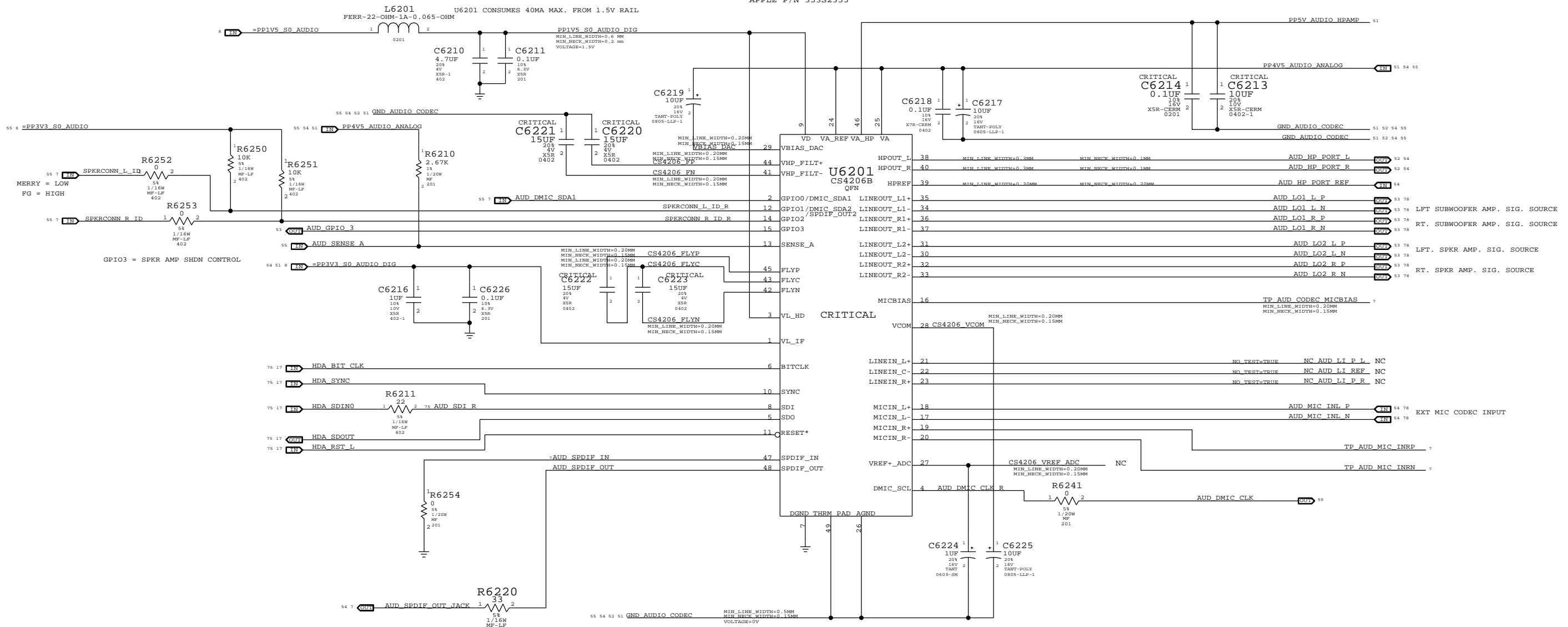
(WRITE: 0XD0 READ: 0XD1)

SYNC MASTER=15 MLR		SYNC DATE=07/29/2011	
PAGE TITLE			
DIGITAL ACCELEROMETER & GYRO			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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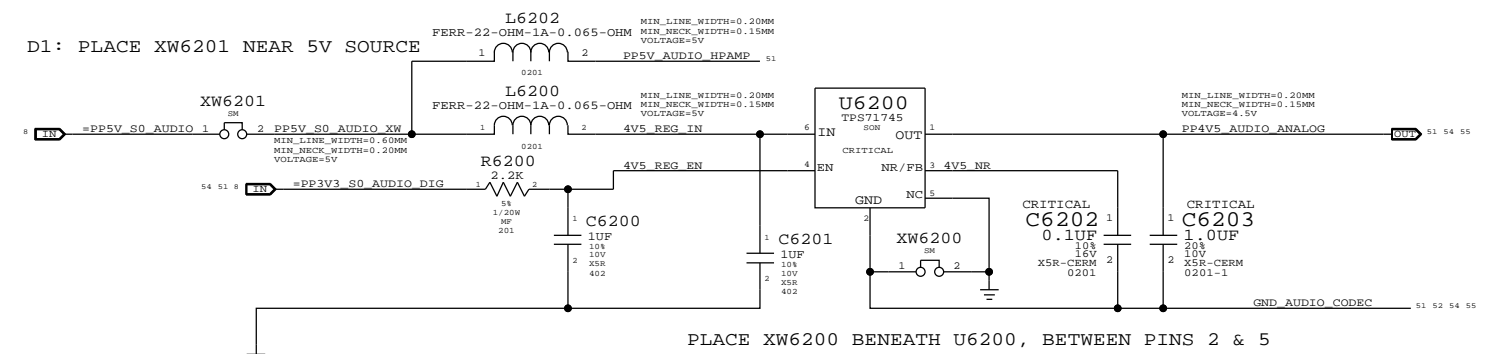
SYNC MASTER=113_MLB		SYNC DATE=01/20/2012	
PAGE TITLE			
SPI ROM			
Apple Inc.		DRAWING NUMBER	SIZE
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AUDIO CODEC
APPLE P/N 353S2355

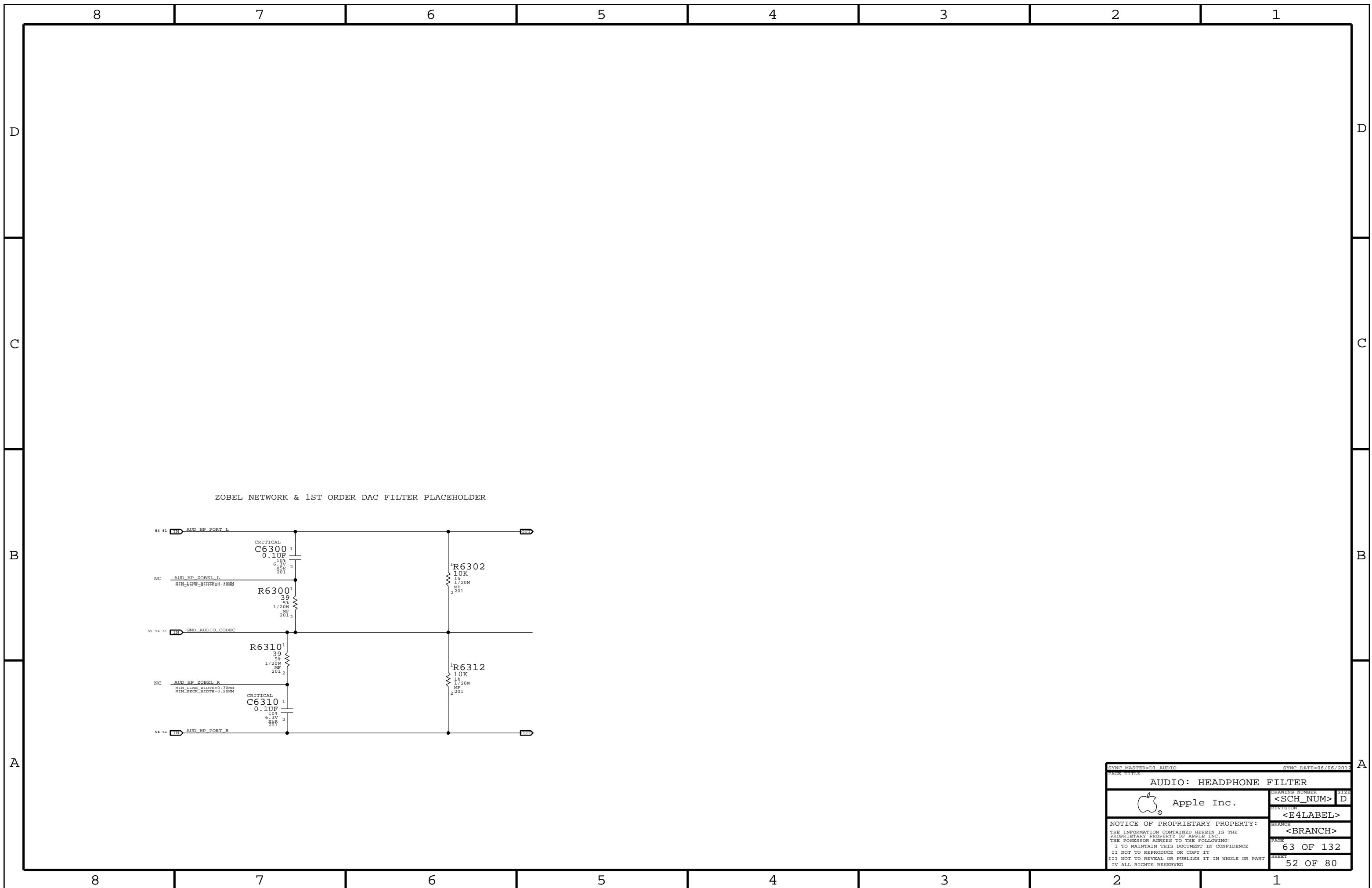


4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456

NOTES ON CODEC I/O
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

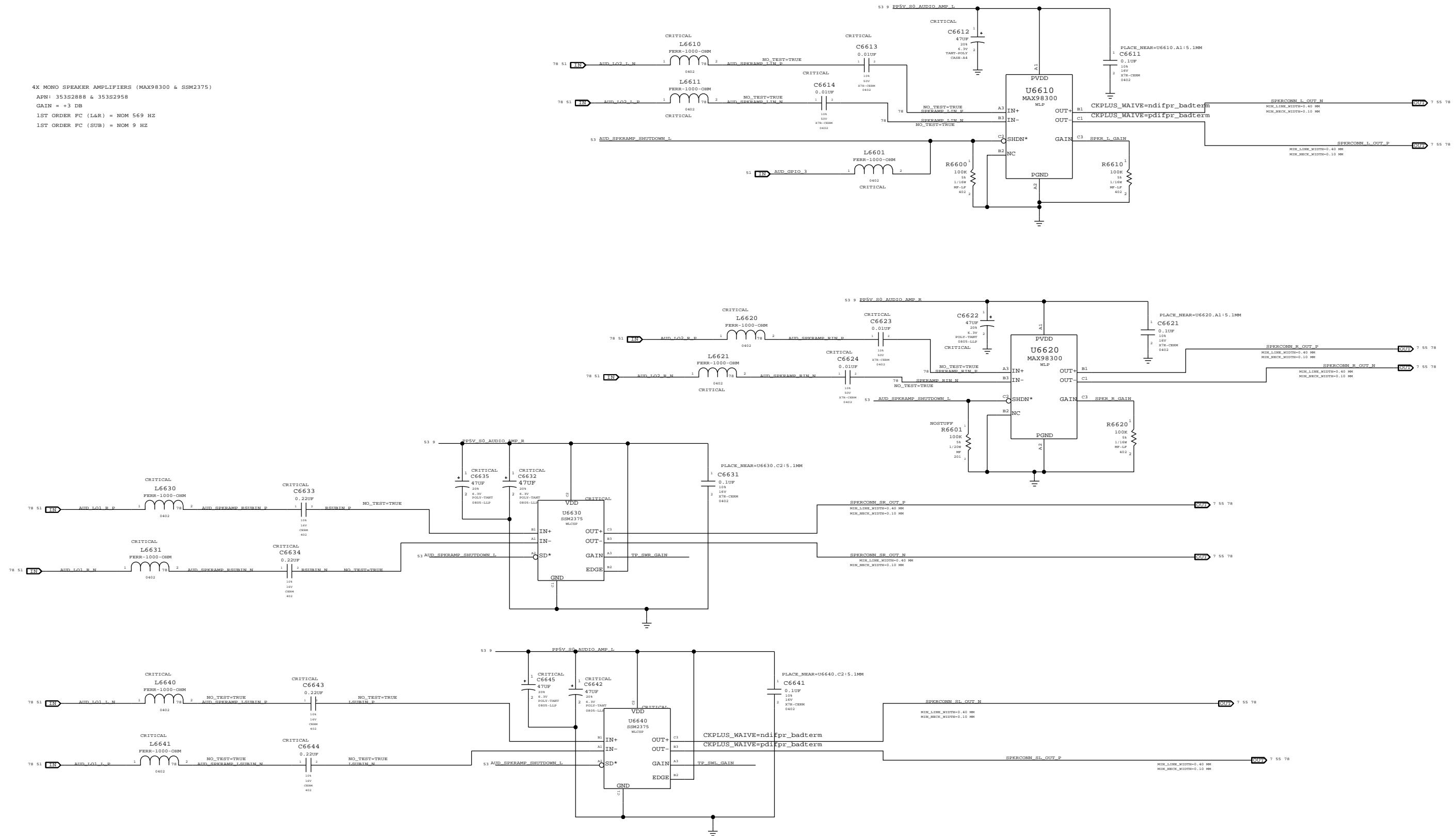



PAGE TITLE		SYNC DATE=06/06/2012	
AUDIO: CODEC/REGULATOR		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
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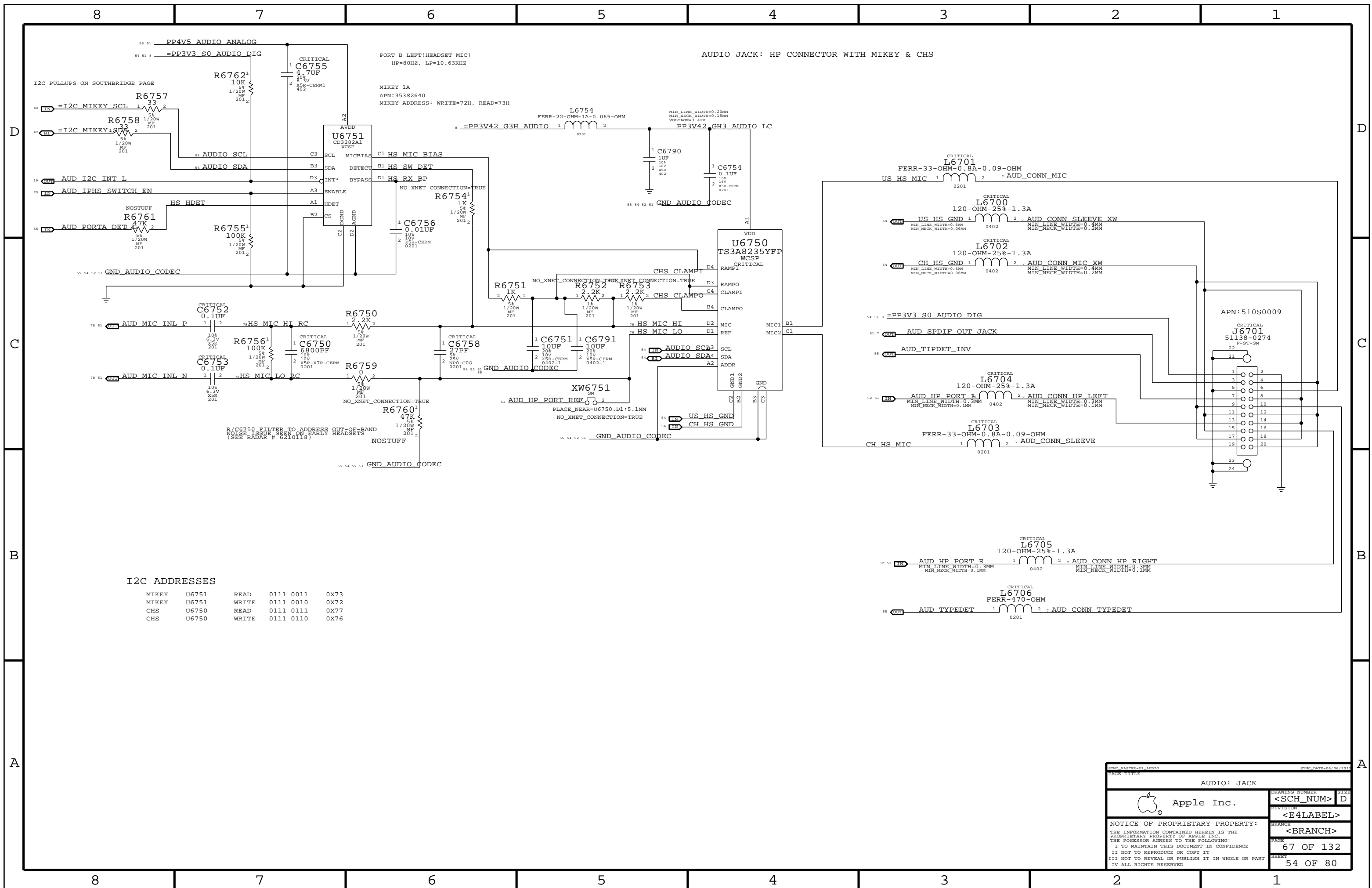


SYNC MASTER=D1 AUDIO		SYNC DATE=06/06/2012	
AUDIO: HEADPHONE FILTER			
Apple Inc.		DRAWING NUMBER	SIZE
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		<BRANCH>	
		PAGE	63 OF 132
		SHEET	52 OF 80

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
 APN: 353S2888 & 353S2958
 GAIN = +3 DB
 1ST ORDER FC (L&R) = NOM 569 HZ
 1ST ORDER FC (SUB) = NOM 9 HZ



SYMC MASTER=01 AUDIO		SYMC_DATE=06/06/2011	
PAGE TITLE			
AUDIO: SPEAKER AMP			
 Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
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	<E4LABEL>	<BRANCH>	
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I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC MASTER=00 AUDIO SYNC DATE=06/06/2011

AUDIO: JACK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> D

REVISION: <E4LABEL>

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	0P10_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	0P10_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

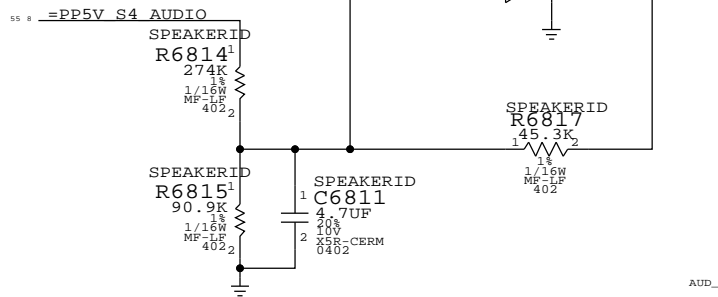
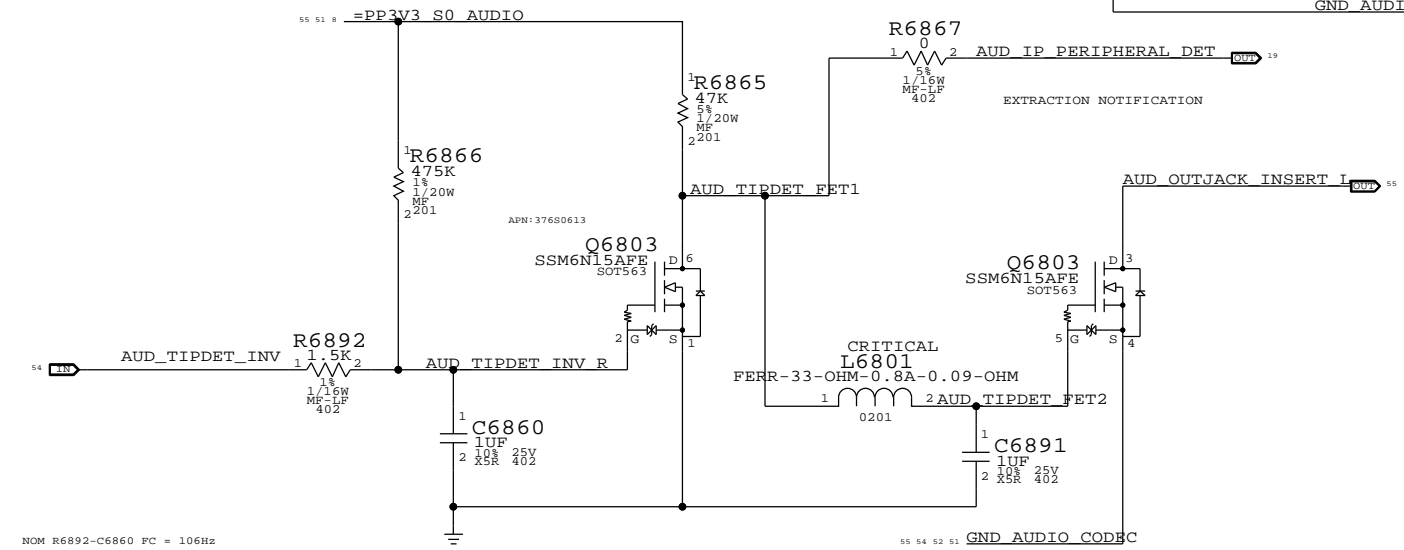
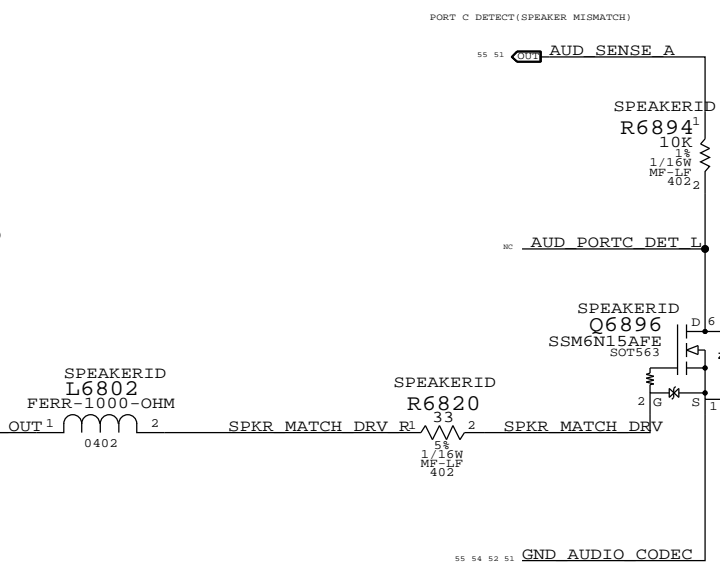
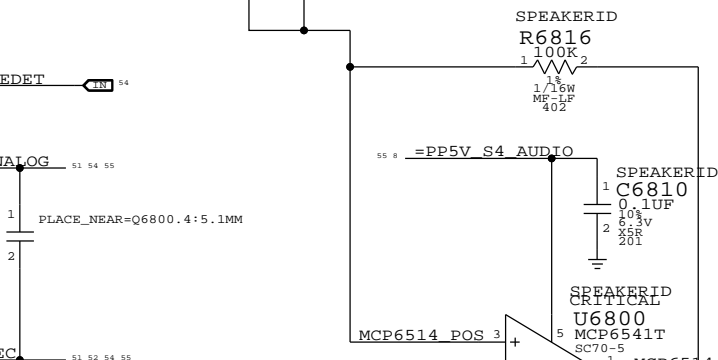
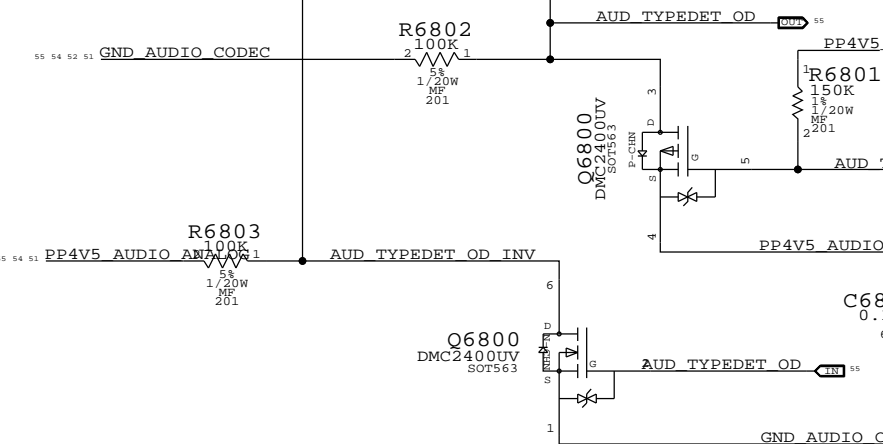
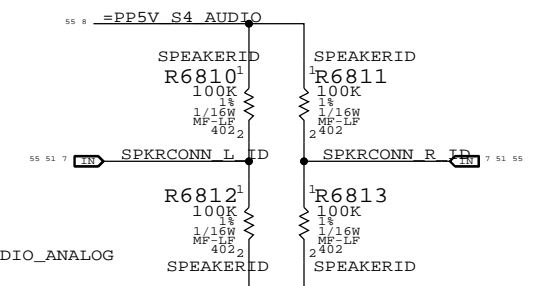
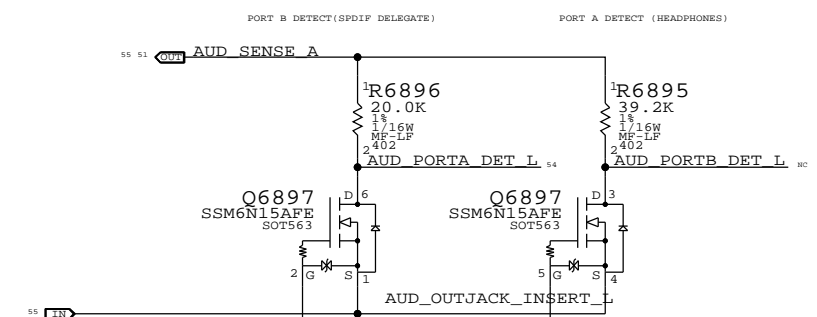
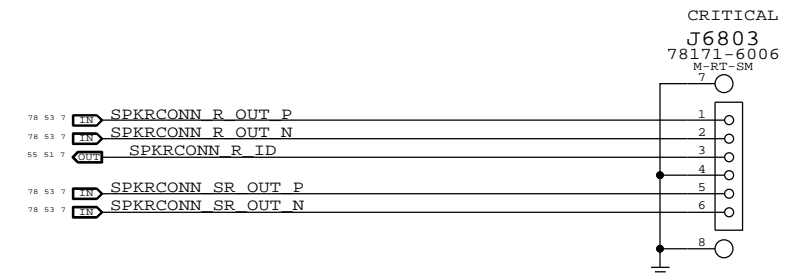
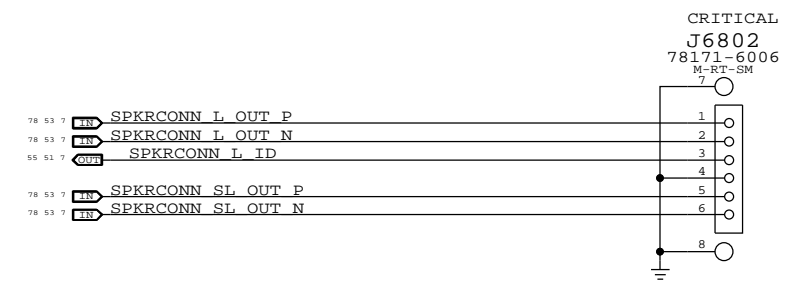
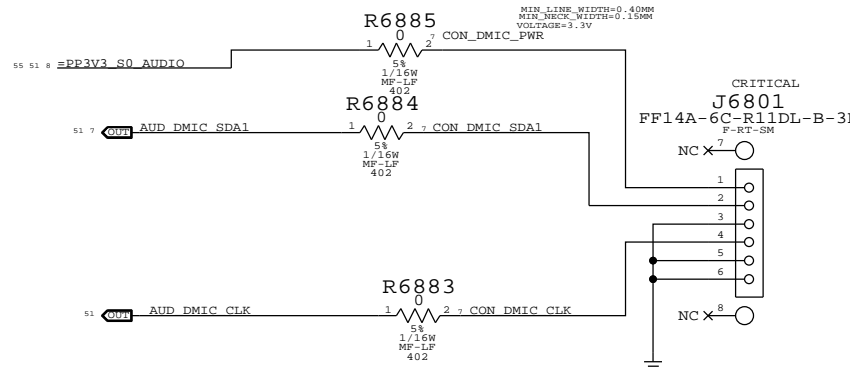
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (0,E)	0V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	0V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LMPT)	MIKEY	MIKEY

SYSTEM INT AND GP10 LINES

FUNCTION	INT	GP10
MIKEY ENABLE	PIRQ N	DATA09/GP10 16
MIKEY INTERRUPT	PIRQ N	GP10 5
PERIPHERAL DETECT	PIRQ P	GP10 3

SPEAKER CONNECTOR HP=80HZ APN: 518S0627

2-MIC CONNECTOR



AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPERDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP
376S0975	376S1081		Q6800	TOSHIBA ALT TO DIODES

NOM R6892-C6860 FC = 106Hz
 SSM6N15FE Vth = 0.8V to 1.5V
 SSM6N15FE IGSS = +/-1uA
 FLEX-SIDE RPUULLDOWN = 100k (TB 49.9k in REV 3)

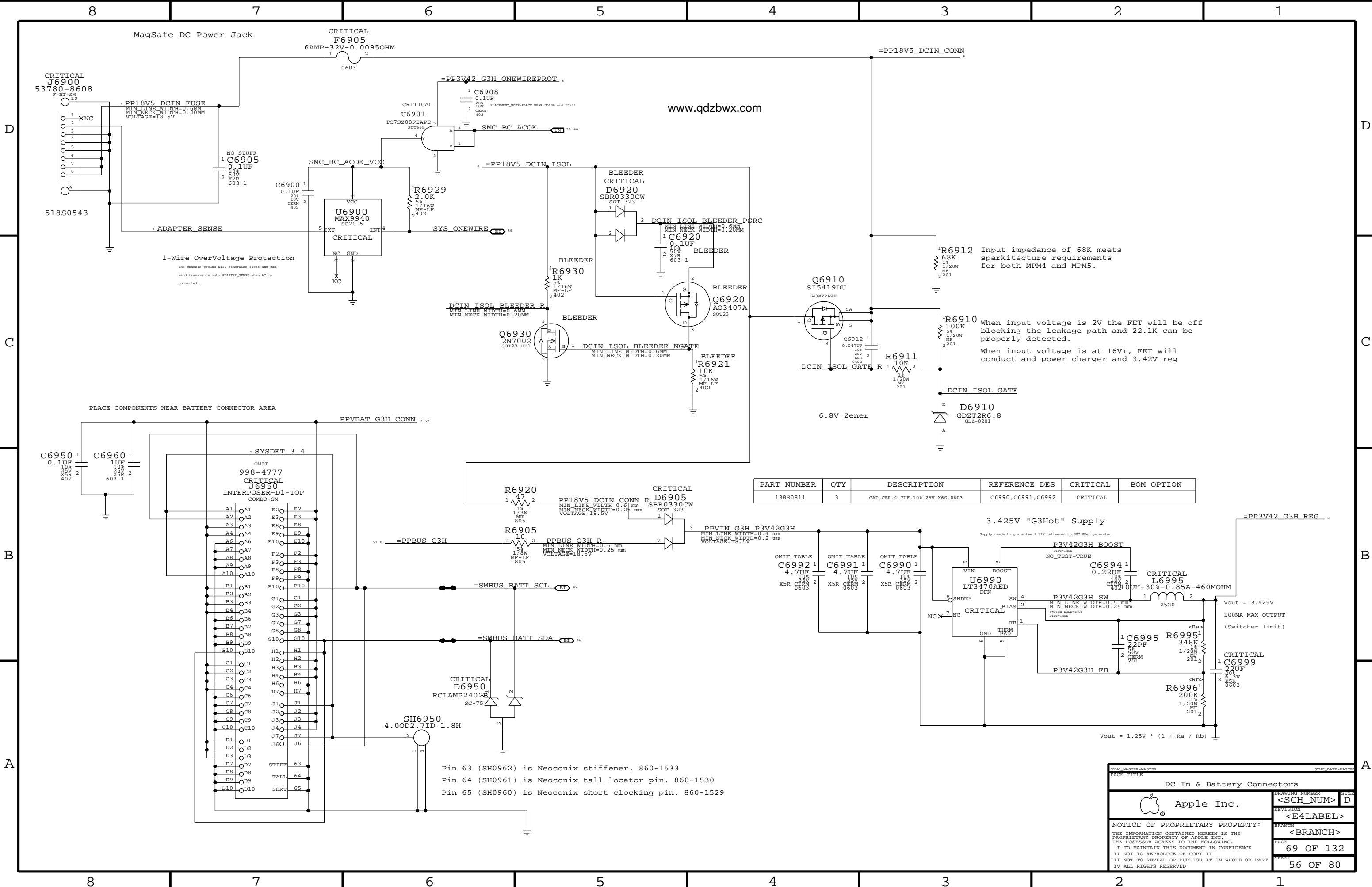
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AUDIO: JACK TRANSLATORS

Apple Inc.

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1-Wire OverVoltage Protection
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

Input impedance of 68K meets sparkiteure requirements for both MPM4 and MPM5.

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.
When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

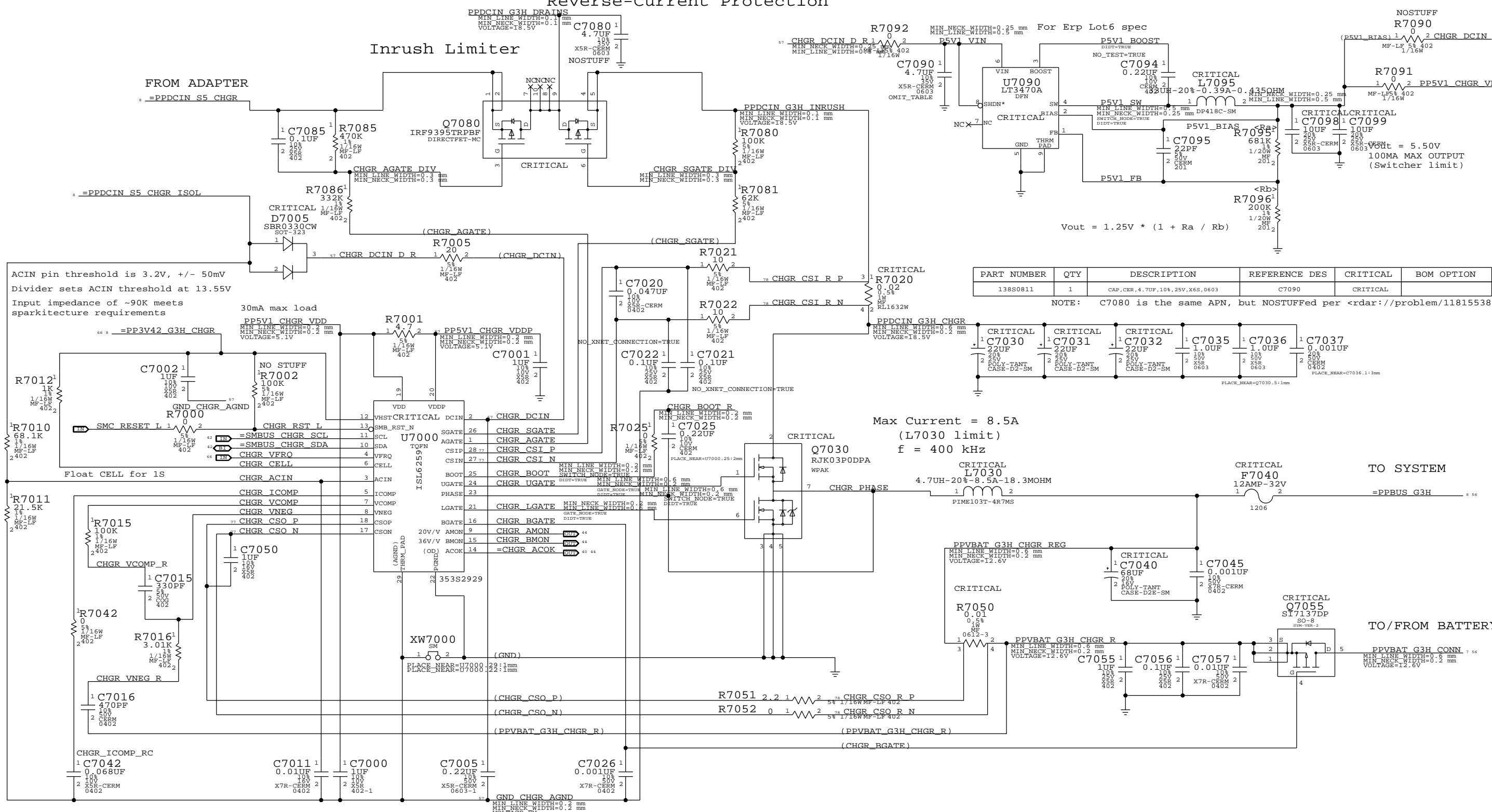
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP, CER, 4.7UF, 10%, 25V, X68, 0603	C6990, C6991, C6992	CRITICAL	

Pin 63 (SH0962) is Neoconix stiffener, 860-1533
Pin 64 (SH0961) is Neoconix tall locator pin. 860-1530
Pin 65 (SH0960) is Neoconix short clocking pin. 860-1529

DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER <SCH_NUM> D
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Reverse-Current Protection

Inrush Limiter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X6S,0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

ACIN pin threshold is 3.2V, +/- 50mV
 Divider sets ACIN threshold at 13.55V
 Input impedance of ~90K meets sparkitecture requirements

30mA max load

Max Current = 8.5A
 (L7030 limit)
 f = 400 kHz

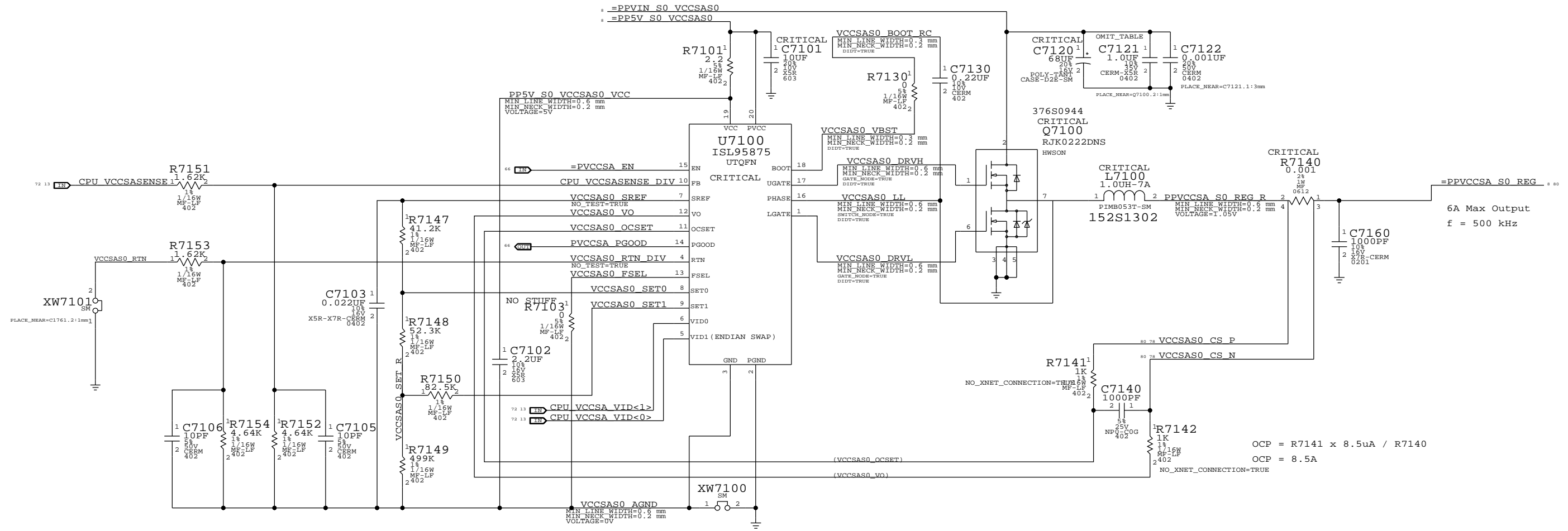
TO SYSTEM
 =PPBUS G3H

TO/FROM BATTERY
 PPVBAT G3H CONN

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PBus Supply & Battery Charger			
Apple Inc.		DRAWING NUMBER	SIZE
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System Agent Power Supply

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7121	CRITICAL	



INTEL TABLE:

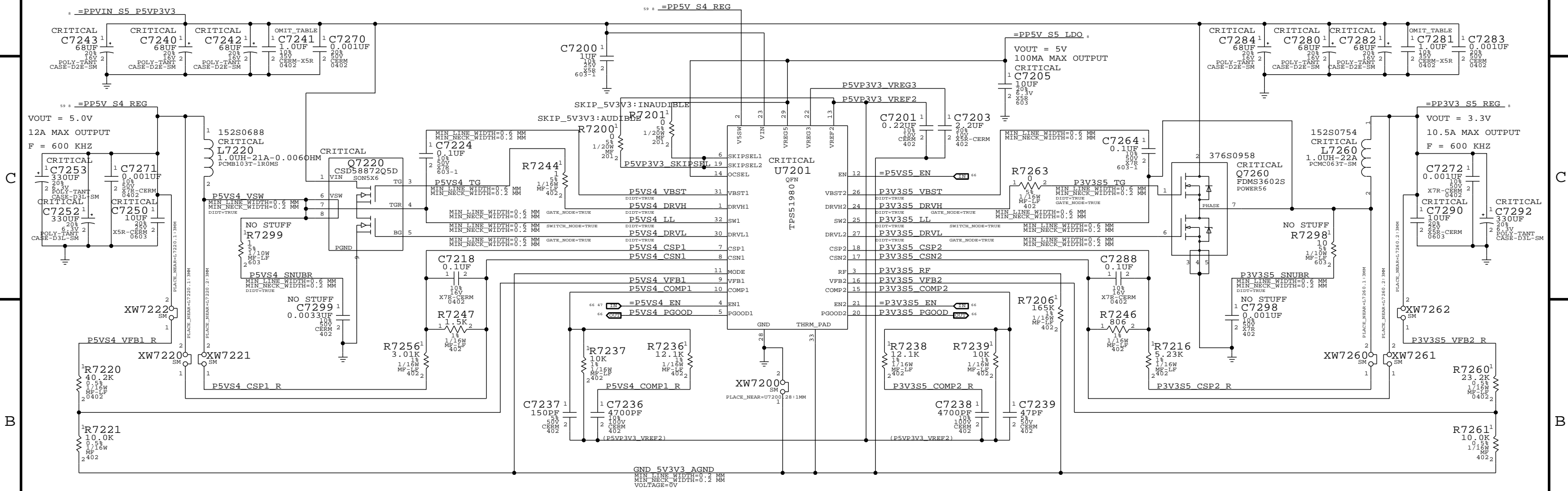
VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

$OCP = R7141 \times 8.5\mu A / R7140$
 $OCP = 8.5A$

SYNC MASTER=MASTER		SYNC DATE=MASTER	
System Agent Supply			
Apple Inc.		DRAWING NUMBER	SIZE
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7241,C7281	CRITICAL	

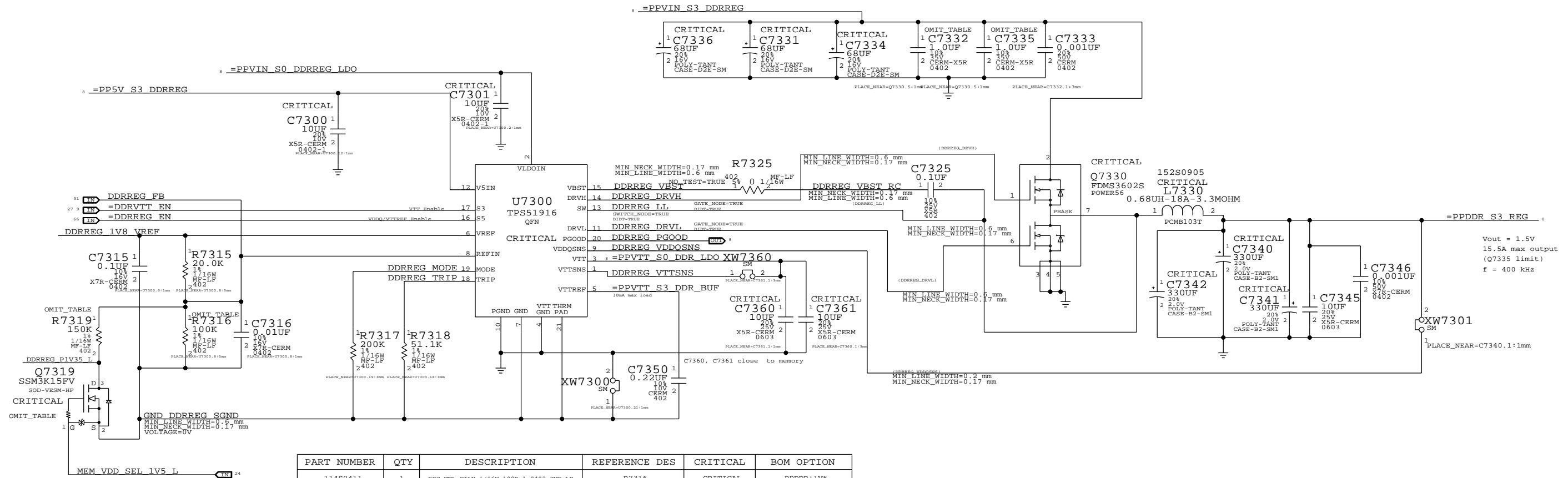


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5V / 3.3V Power Supply		D
DRAWING NUMBER		SIZE
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X5R,0402,MURATA	C7332,C7335	CRITICAL	

DDR3 (1V5R1V35 S3) REGULATOR



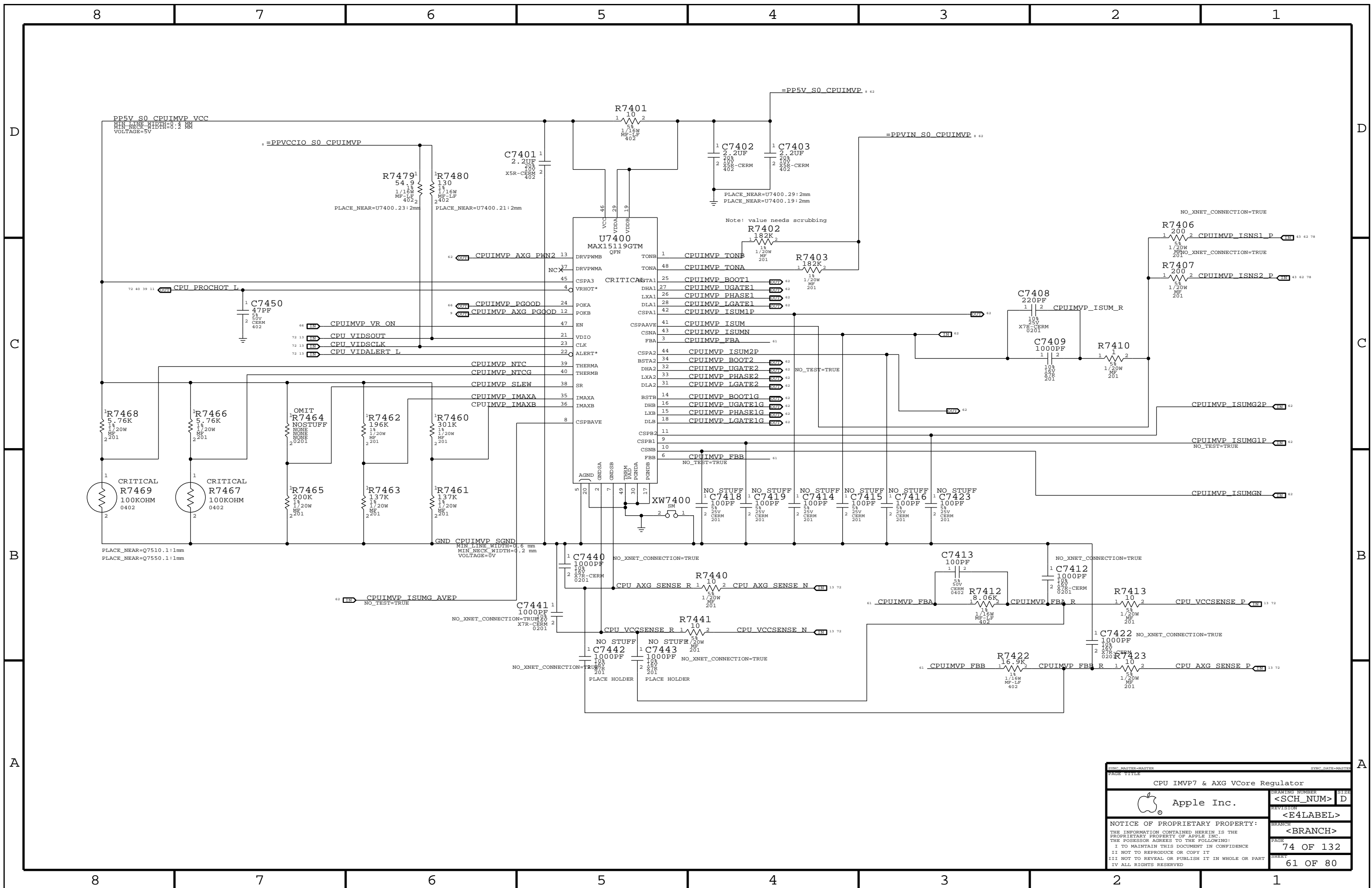
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,50.4K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.00MM,SOT-723,HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150K,0402,SMD,LF	R7319	CRITICAL	PPDDR:1V5

1.5V DDR3 Supply

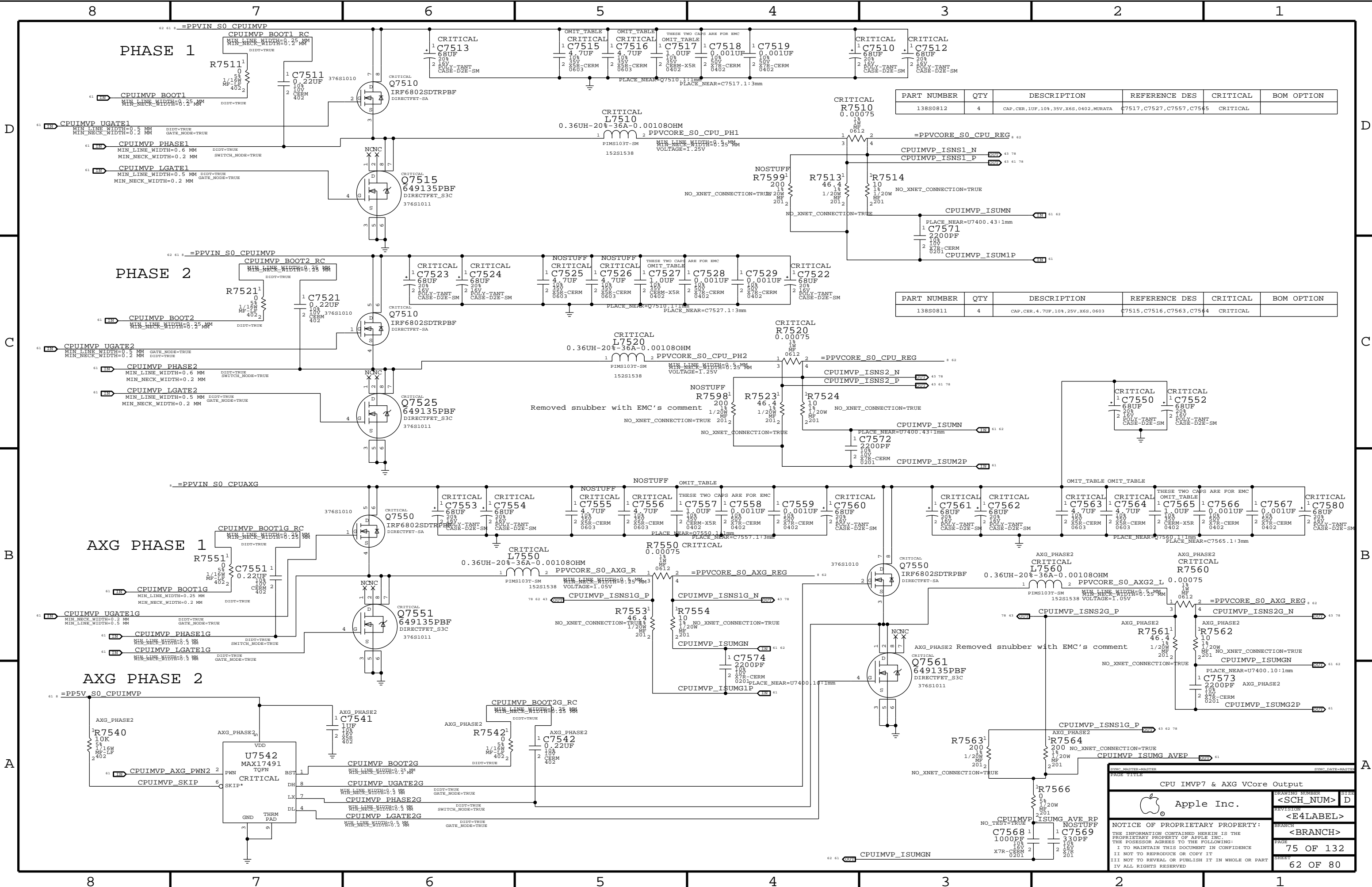
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SYMC MASTER-MASTER		SYMC DATE-MASTER	
PAGE TITLE			
CPU IMVP7 & AXG VCore Regulator			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	4	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7517,C7527,C7557,C7565	CRITICAL	

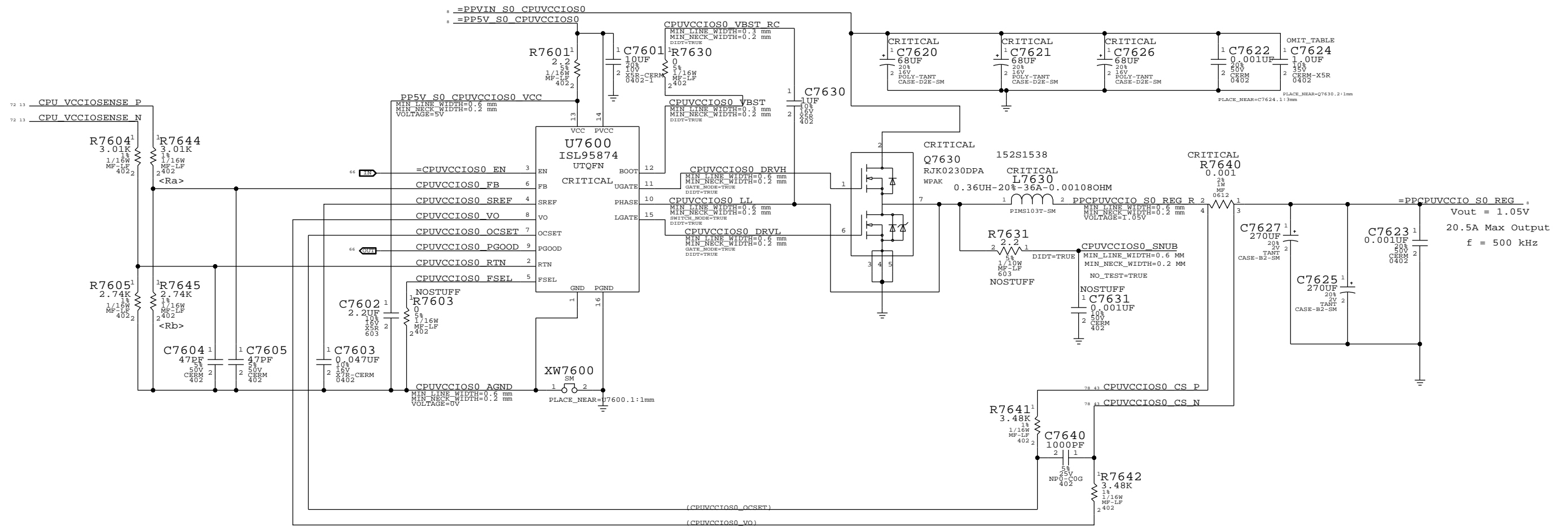
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C7515,C7516,C7563,C7564	CRITICAL	

CPU IMVP7 & AXG VCore Output
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CPU VCCIO (1.05V S0) Regulator

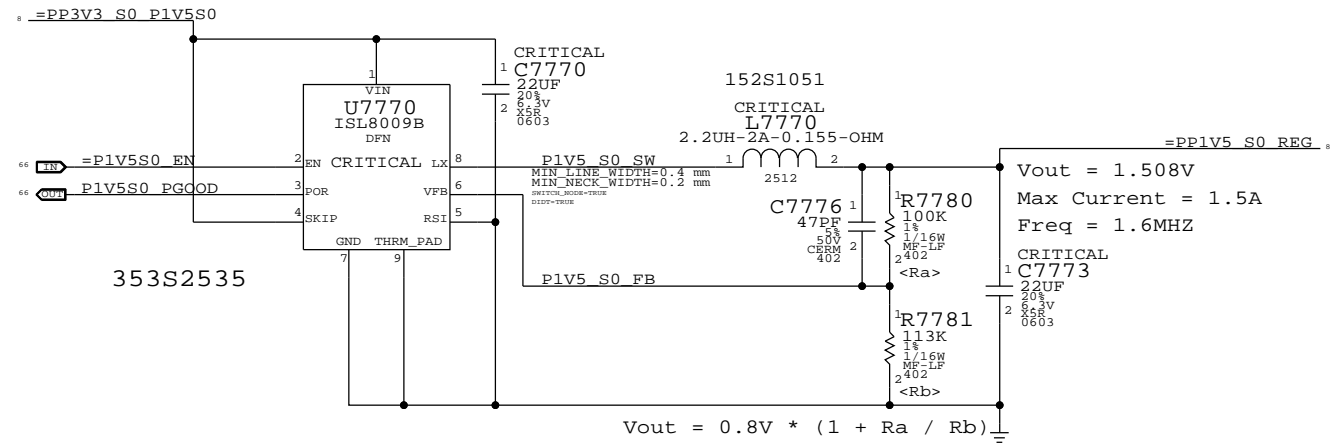
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7624	CRITICAL	



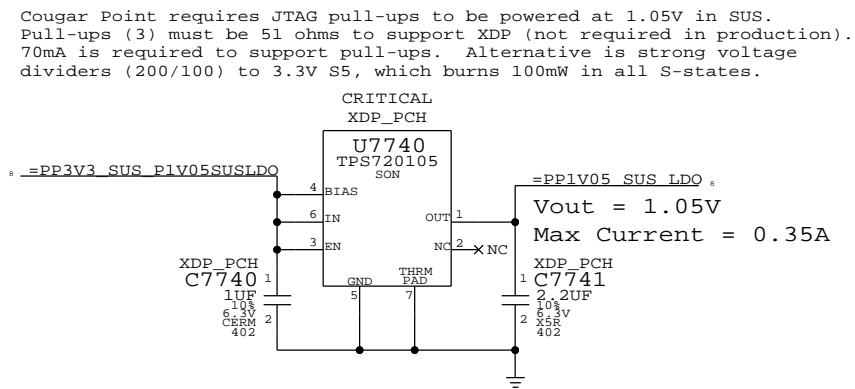
$OCP = R7641 \times 8.5\mu A / R7640$
 $OCP = 26.265A$
 $V_{out} = 0.5V \times (1 + R_a / R_b)$

DRAWING NUMBER		SIZE
CPUVCCIO (1.05V) Power Supply		D
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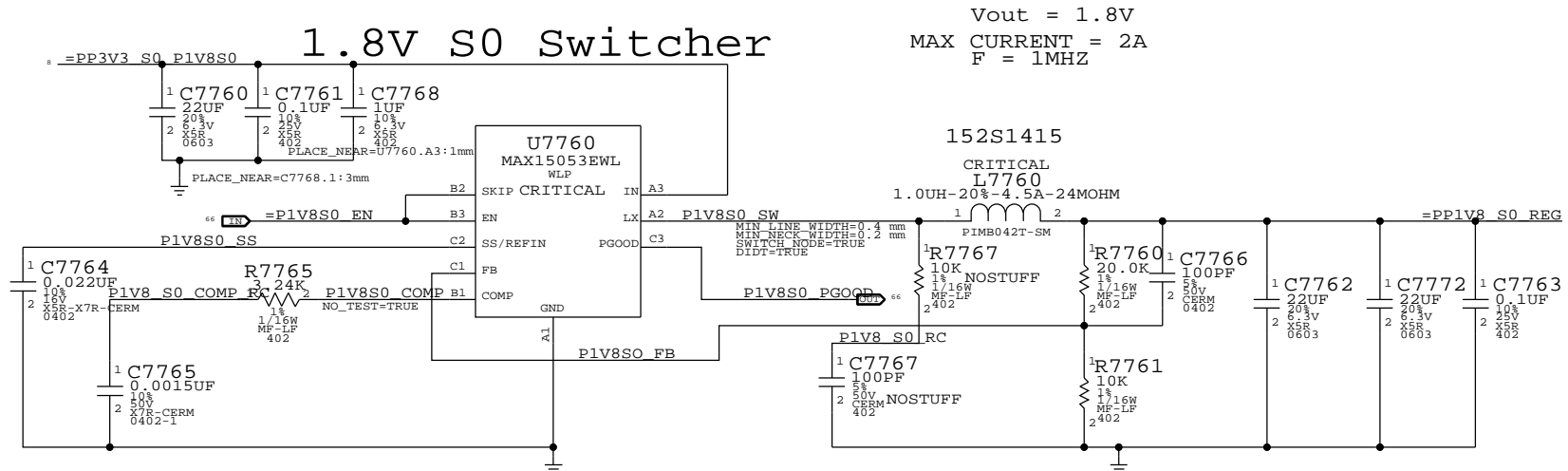
1.5V S0 Switcher



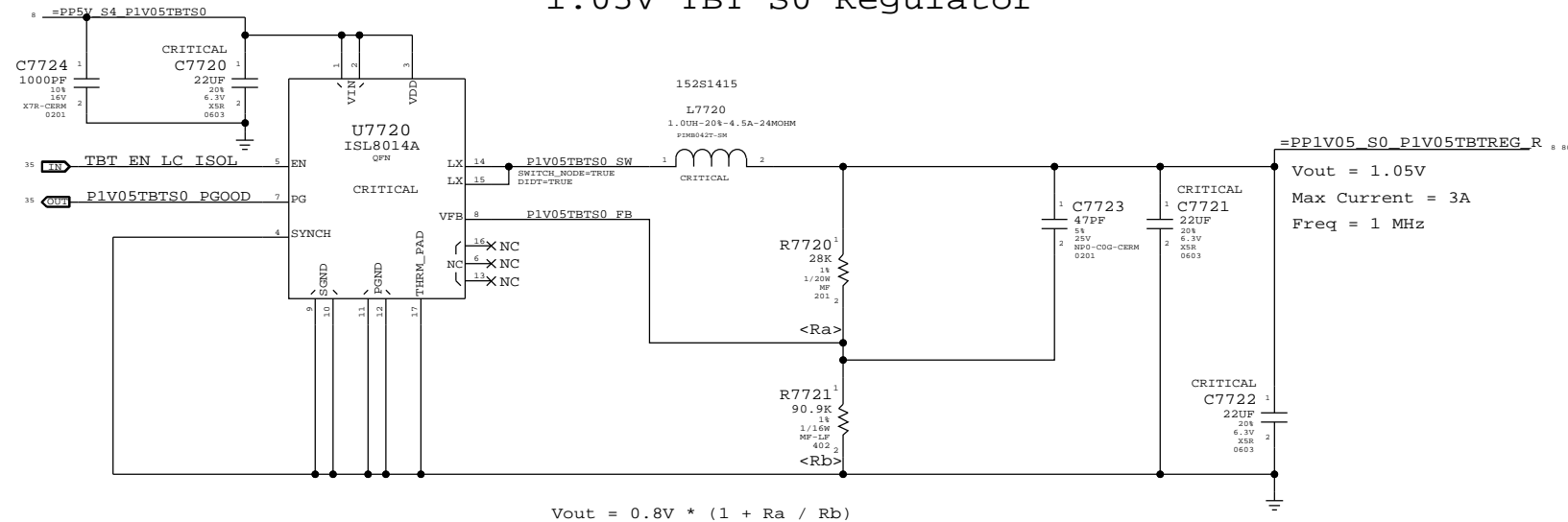
1.05V SUS LDO



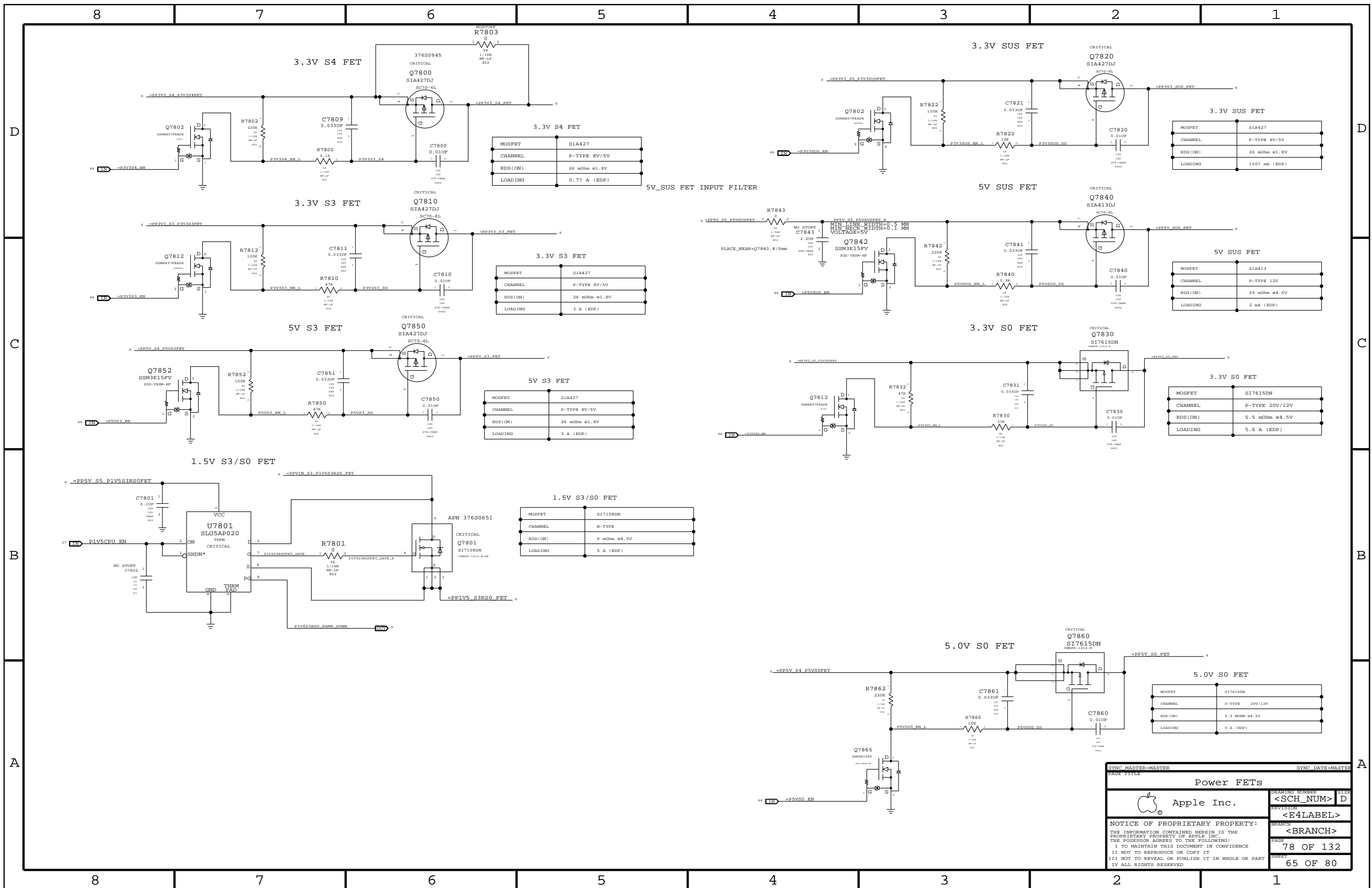
1.8V S0 Switcher



1.05V TBT S0 Regulator



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Misc Power Supplies			
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3.3V S4 FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

5V S3 FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V SUS FET

MOSFET	SIA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SIA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

5.0V S0 FET

MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

Power FETs

Apple Inc.

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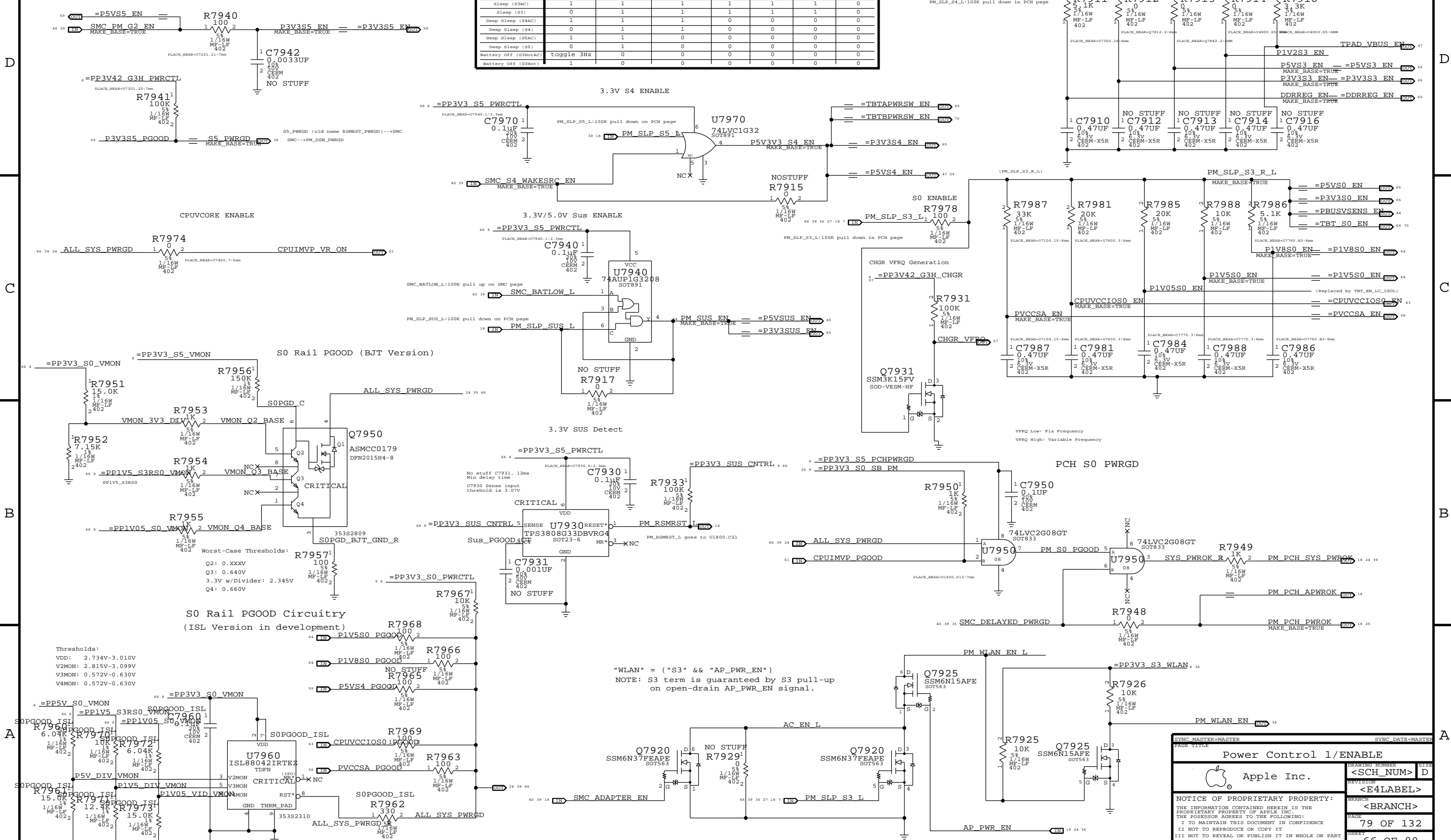
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REVISION	<E4LABEL>	BRANCH	<BRANCH>
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S5 Rail Enables & PGOOD

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	Toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

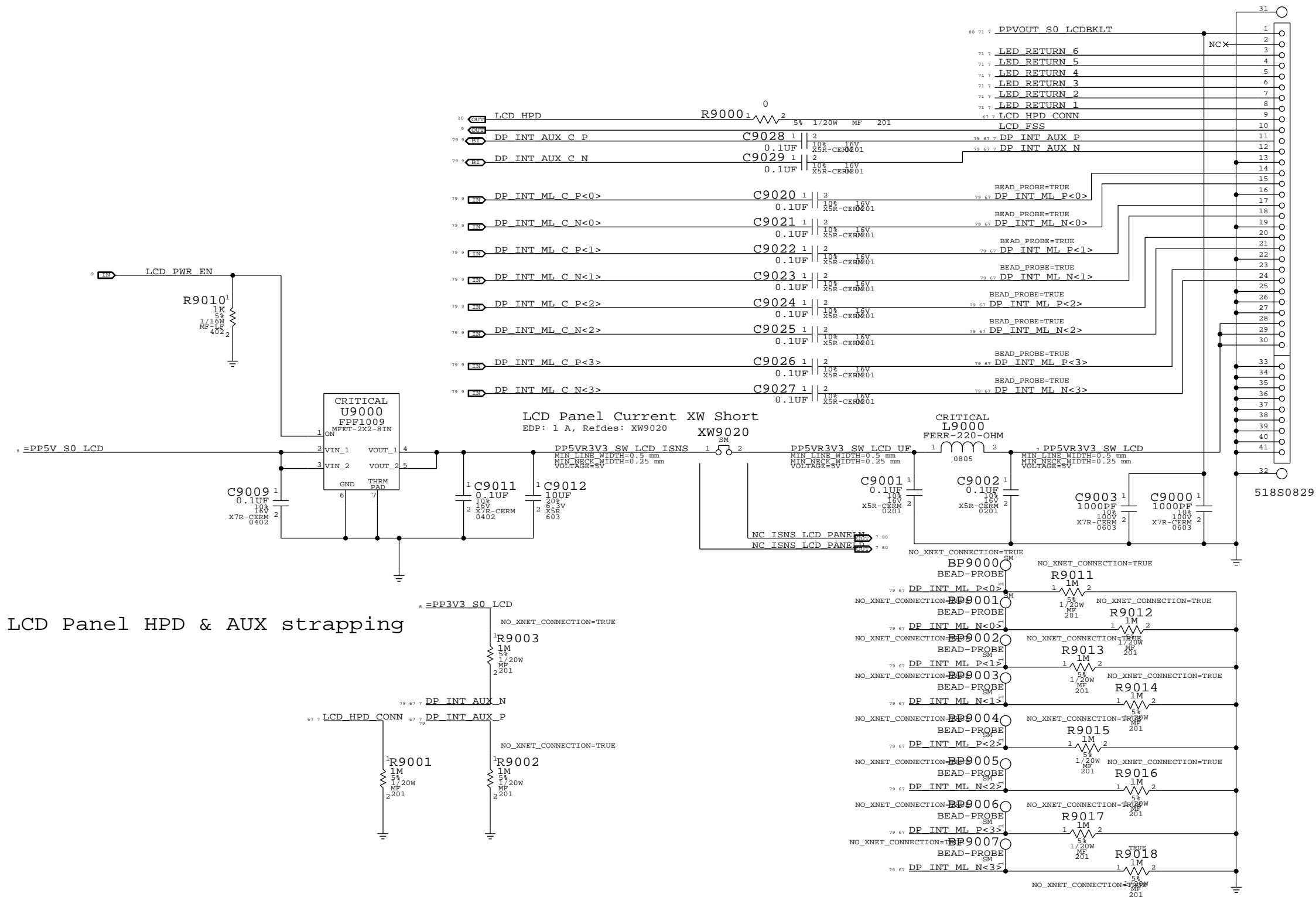
1.2V, 5V, 3.3V, DDR S3 ENABLE



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Power Control 1/ENABLE			
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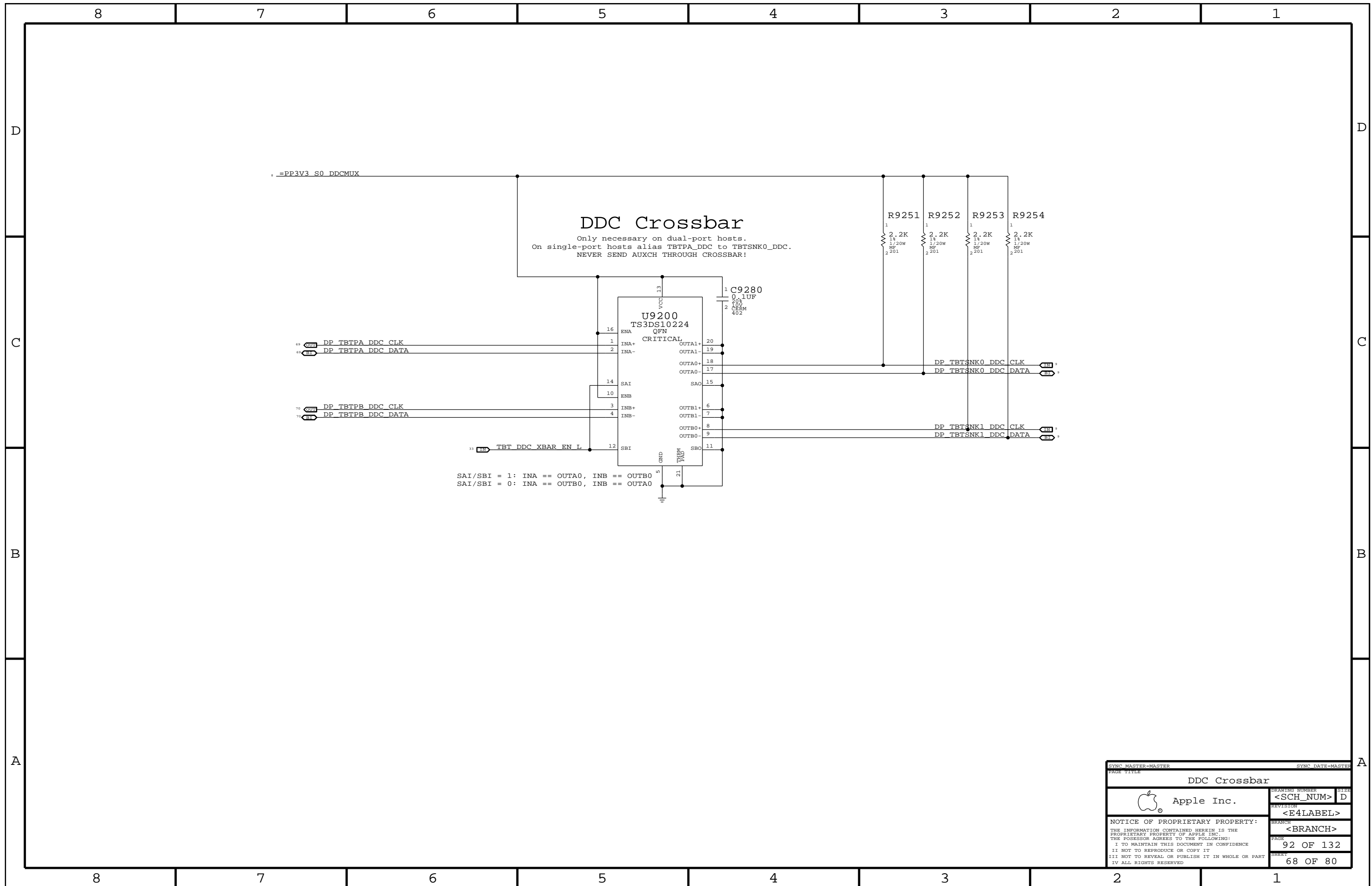
LCD PANEL INTERFACE (eDP)

CRITICAL
J9000
20525-130E-01
F-RT-SM



LCD Panel HPD & AUX strapping

SYNC MASTER=DL SENSORS		SYNC DATE=07/11/2012	
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eDP Display Connector		DRAWING NUMBER	SIZE
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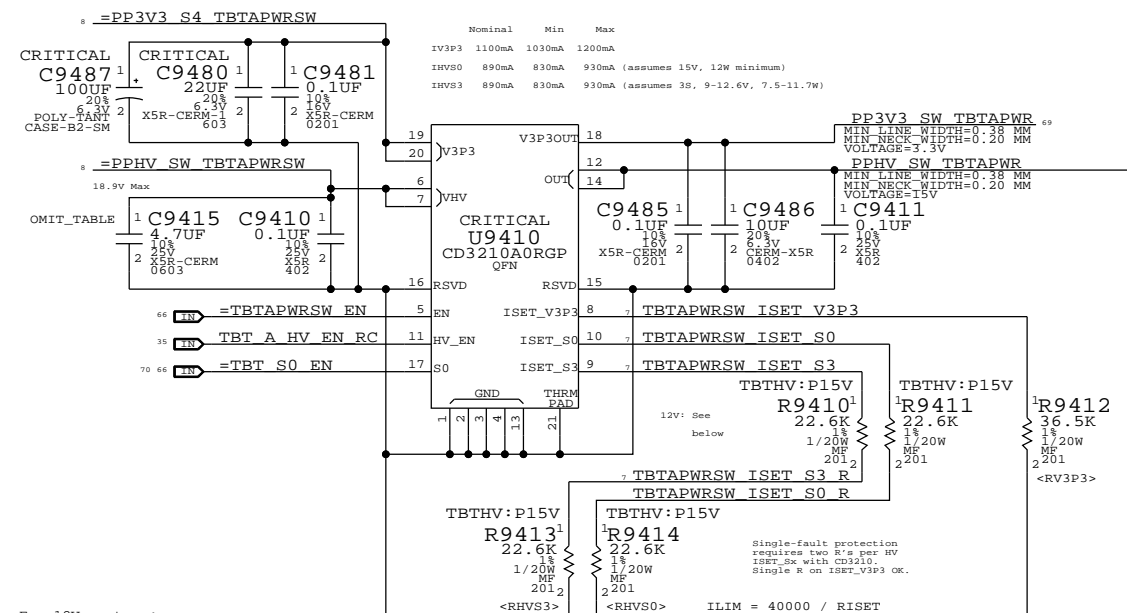


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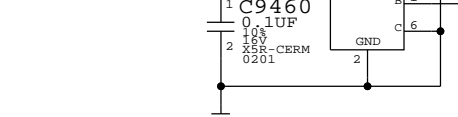
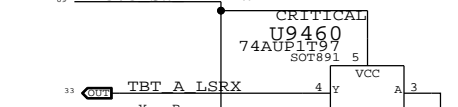
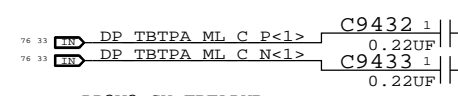
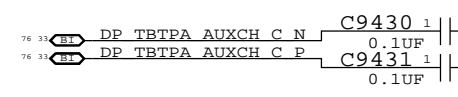
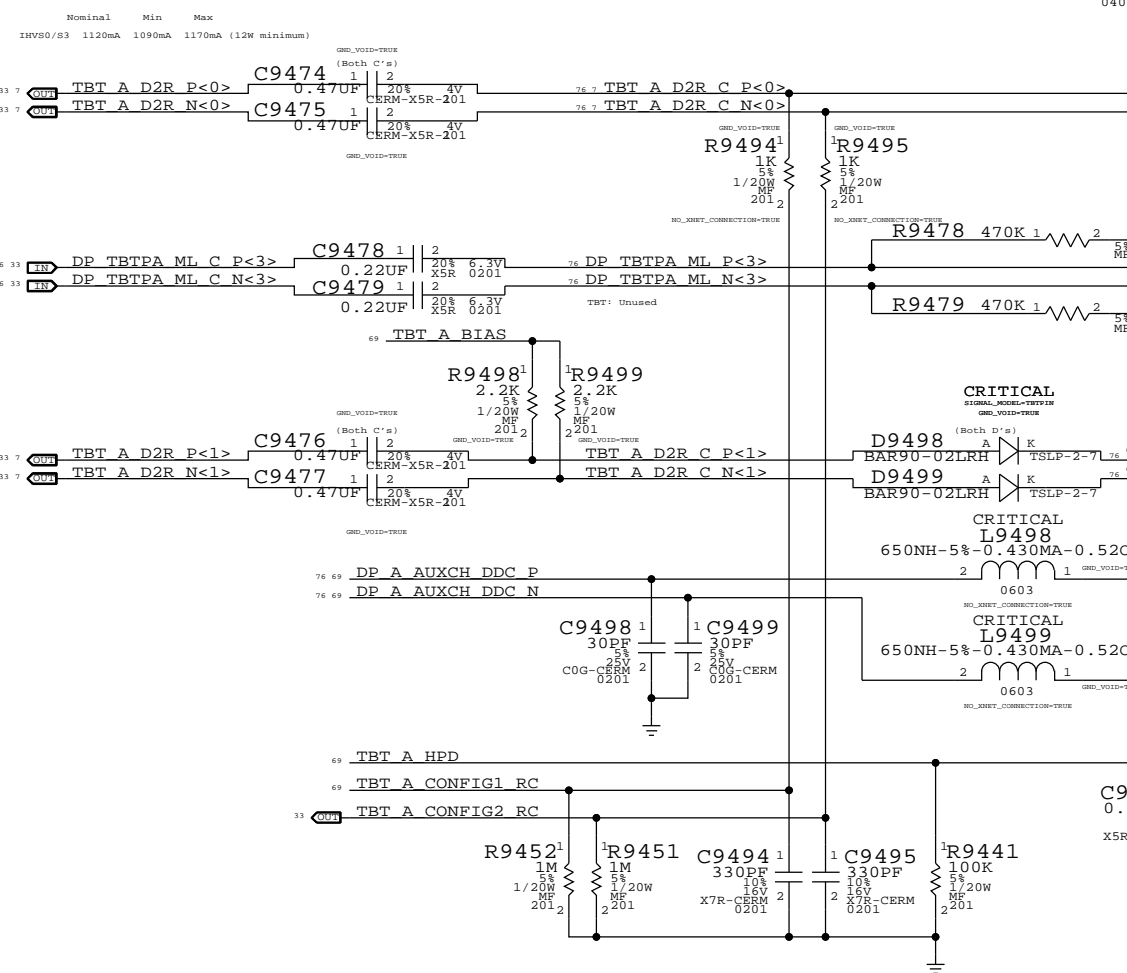
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

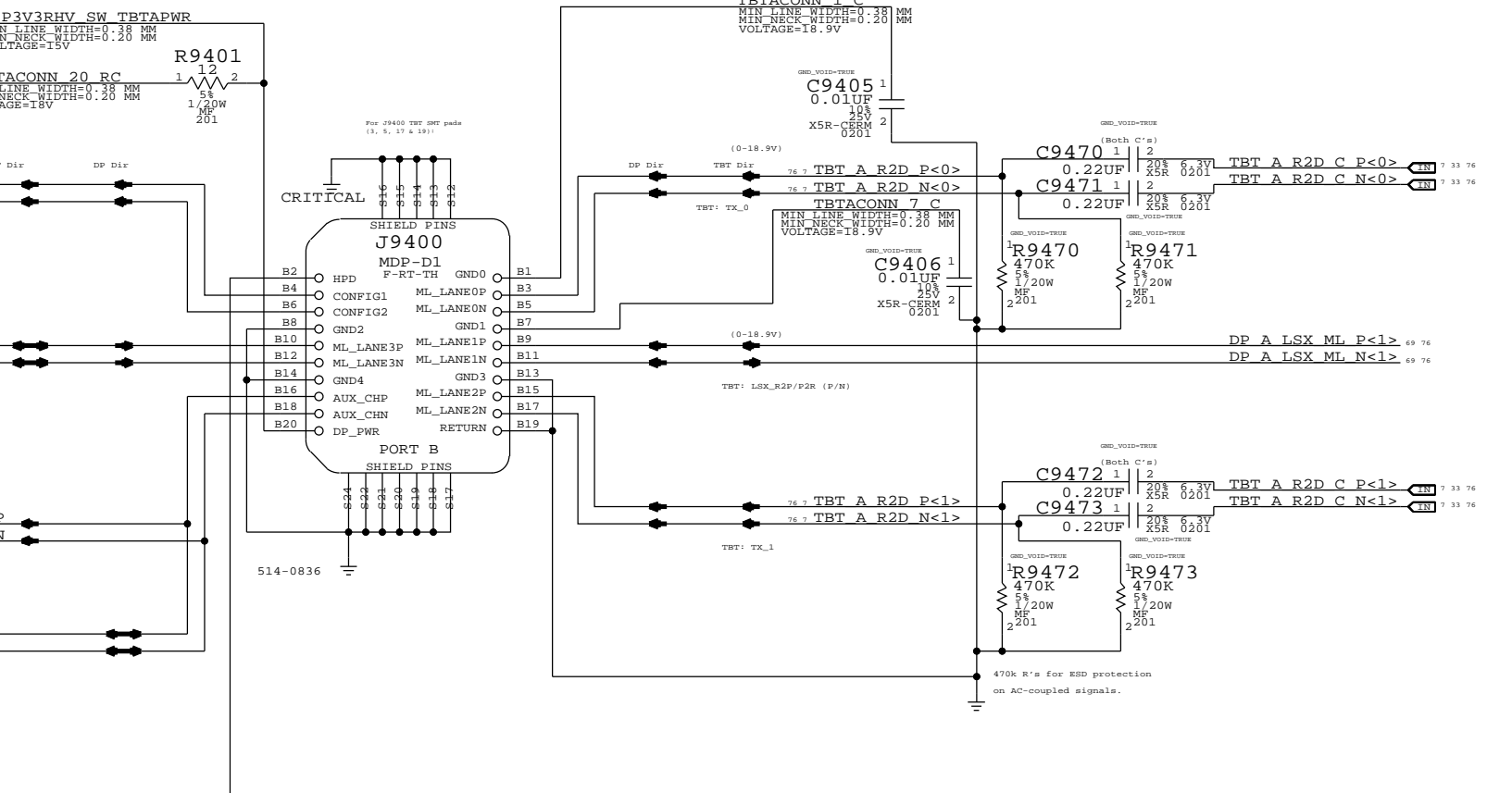
V3P3 must be S4 to support wake from Thunderbolt devices.



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V



Thunderbolt Connector A



DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYMC PARTS: MIB X5R100 SYMC DATE: 11/14/2011

Thunderbolt Connector A

Apple Inc.

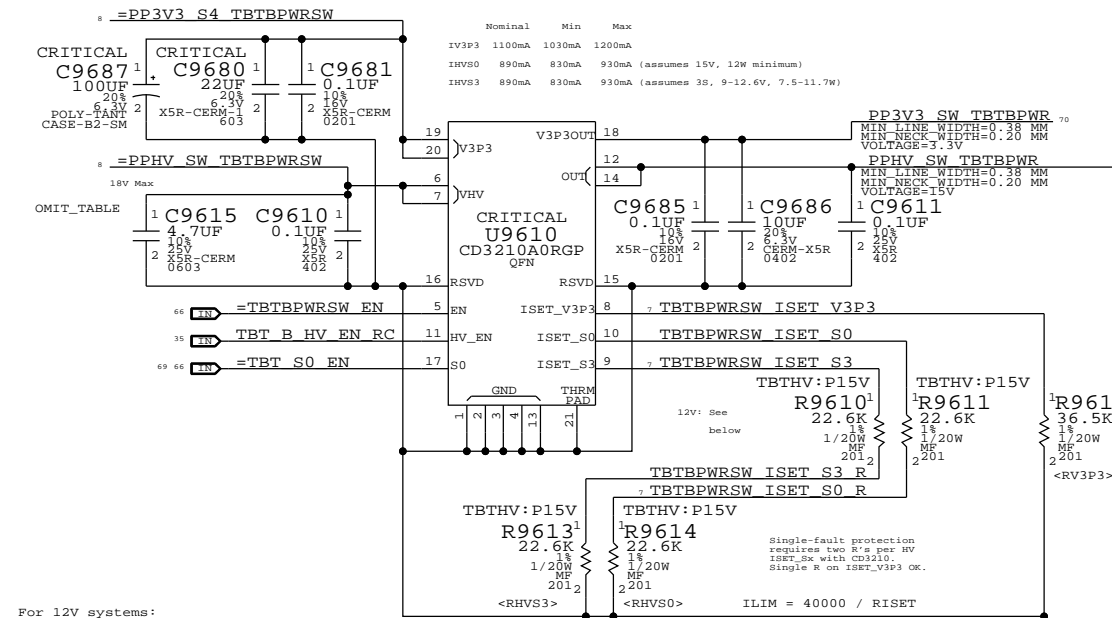
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9615	CRITICAL	

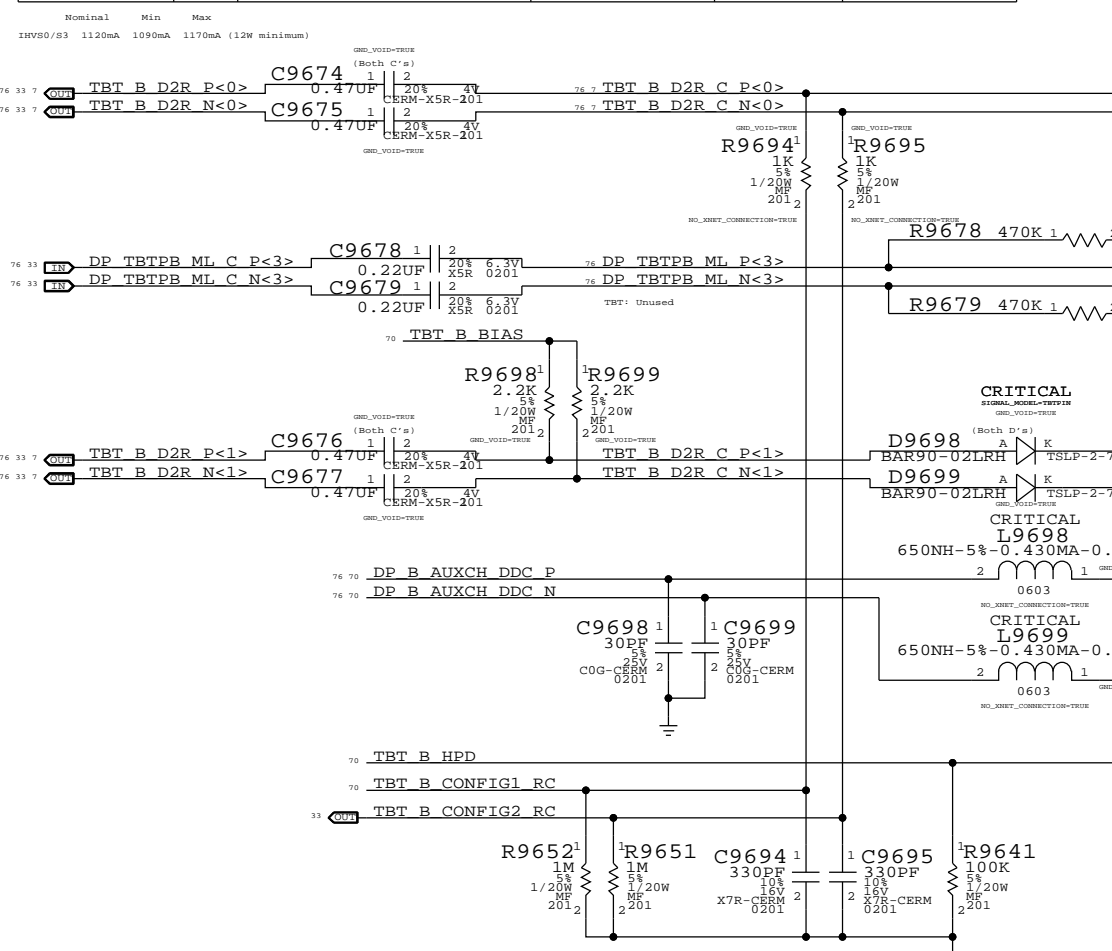
3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.



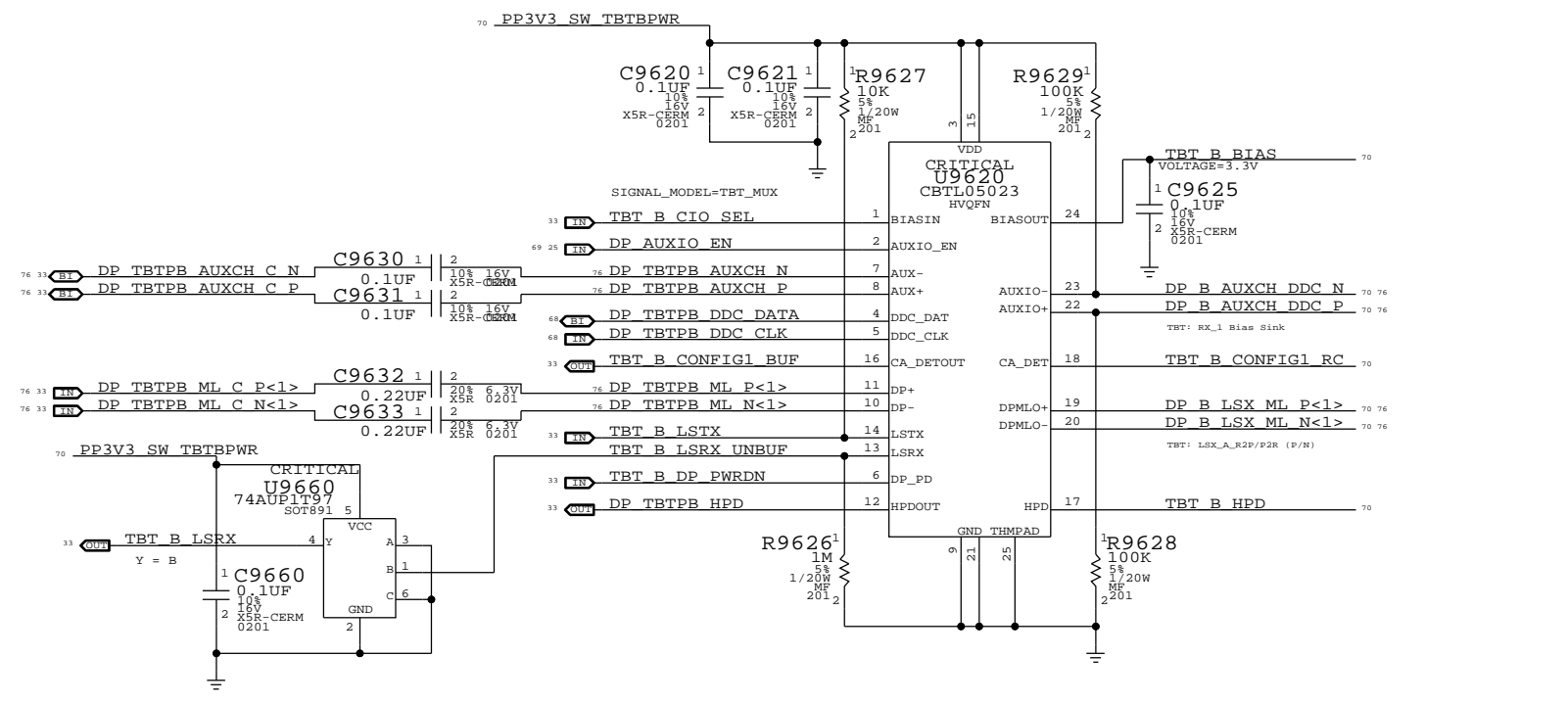
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

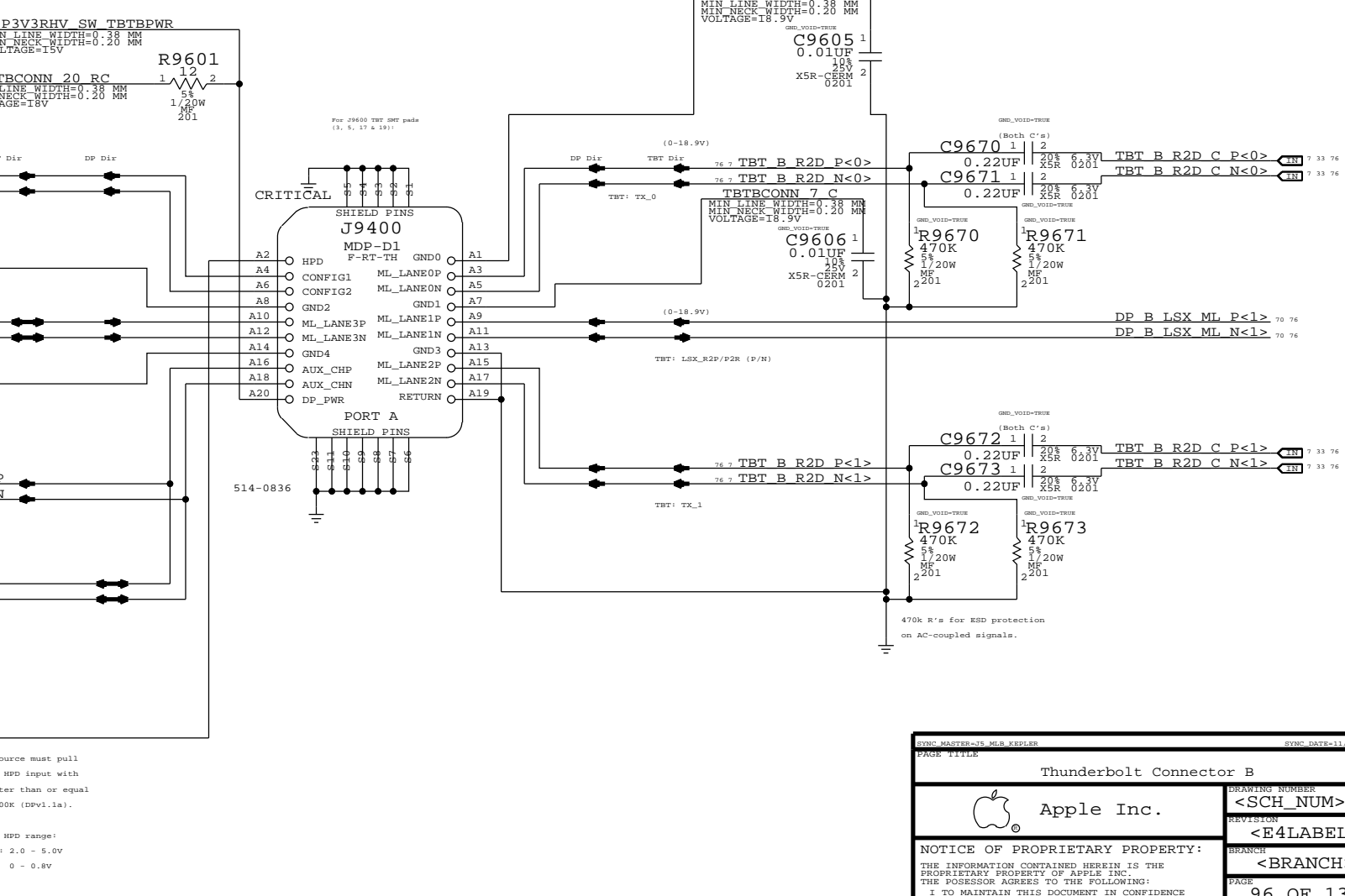


DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V



Thunderbolt Connector B



DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

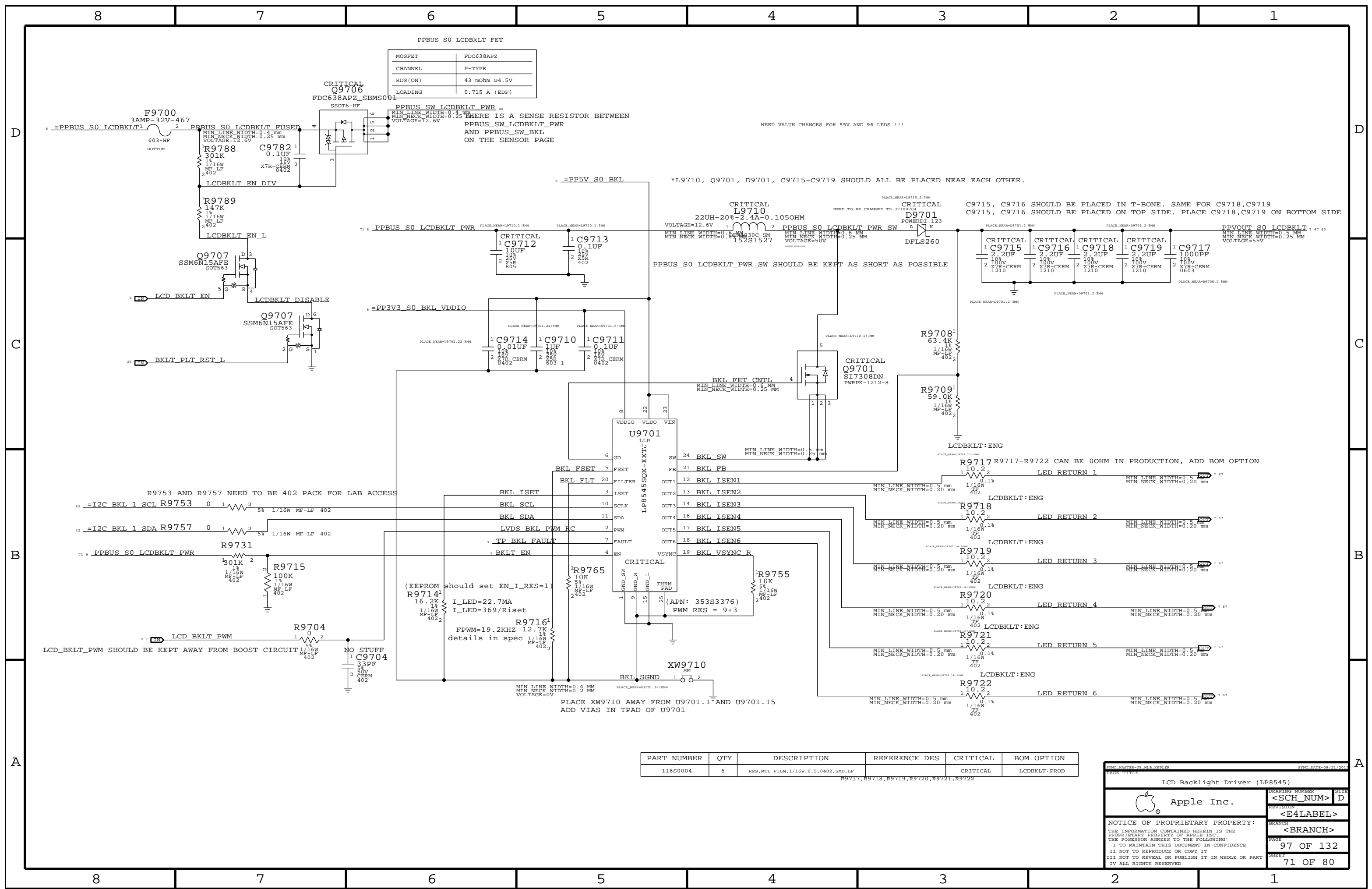
SYMC PARTS: MIB, X5R050
PAGE TITLE
SYMC DATE: 11/14/2011

Thunderbolt Connector B

Apple Inc.

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PPBUS_S0_LCDBKLT_FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

CRITICAL Q9706 FDC638APZ_SBMS091

PPBUS_SW_LCDBKLT_PWR #0
 MIN LINE WIDTH=0.4 MM
 MIN NECK WIDTH=0.25 MM
 VOLTAGE=12.6V
 THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!

*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.

C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718, C9719
 C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718, C9719 ON BOTTOM SIDE

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

R9708¹

R9709¹

R9717 R9717-R9722 CAN BE 0OHM IN PRODUCTION, ADD BOM OPTION

(EEPROM should set EN_I_RES=1)
 R9714¹ 16.2K
 I_LED=22.7MA
 I_LED=369/Riset

R9755¹ 10K
 (APN: 353S3376)
 PWM RES = 9+3

R9716¹ 12.7K
 FPWM=19.2KHZ
 details in spec

PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
 ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES, MTL FILM, 1/16W, 0.5, 0402, SMD, LF		CRITICAL	LCDBKLT:PROD

SYNCH MATTERS: NLS, KDFLES SYNCH DATE: 09/21/2011

PAGE TITLE LCD Backlight Driver (LP8545)

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?	CPU_VID	*	0.457 MM	?
CPU_COMP	*	=4X_DIELECTRIC	?	CPU_VREF	*	12 MIL	?
CPU_ITP	*	=4x_DIELECTRIC	?				
CPU_VCCSENSE	*	=6X_DIELECTRIC	?				

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X_DIELECTRIC	?
CLK_PCIE	*	=5X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
DMT_S2N	BCIE_85D	BCIE		DMI S2N P<3:0>	7 10 18
DMT_S2N	BCIE_85D	BCIE		DMI S2N N<3:0>	7 10 18
DMT_N2S	BCIE_85D	BCIE		DMI N2S P<3:0>	7 10 18
DMT_N2S	BCIE_85D	BCIE		DMI N2S N<3:0>	7 10 18
FDI_DATA	BCIE_85D	BCIE		FDI DATA P<7:0>	7 10 18
FDI_DATA	BCIE_85D	BCIE		FDI DATA N<7:0>	7 10 18
FDI_FSYNC	CPU_50S	CPU_AGTL		FDI FSYNC<1..0>	10 18
FDI_LSYNC	CPU_50S	CPU_AGTL		FDI LSYNC<1..0>	10 18
FDI_INT	CPU_50S	CPU_AGTL		FDI INT	10 18
DMI_CLK100M	CLK_BCIE_90D	CLK_BCIE		DMI CLK100M CPU P	7 11 17
DMI_CLK100M	CLK_BCIE_90D	CLK_BCIE		DMI CLK100M CPU N	7 11 17
CPU_EDP_COMP	CPU_27P4S	CPU_COMP		CPU EDP COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP		CPU PEG COMP	10
CPU_CFG	CPU_50S	CPU_ITP		CPU CFG<17..0>	10 24
XDP_CLK_CPU	CLK_BCIE_90D	CLK_BCIE		ITPCPU CLK100M P	11 17
XDP_CLK_CPU	CLK_BCIE_90D	CLK_BCIE		ITPCPU CLK100M N	11 17
XDP_CLK_BCH	CLK_BCIE_90D	CLK_BCIE		ITPXDP CLK100M P	17 24
XDP_CLK_BCH	CLK_BCIE_90D	CLK_BCIE		ITPXDP CLK100M N	17 24
DPLL_REF_CLK120M	CLK_BCIE_90D	CLK_BCIE		DPLL REF CLK P	11 17
DPLL_REF_CLK120M	CLK_BCIE_90D	CLK_BCIE		DPLL REF CLK N	11 17
XDP_TDI	CPU_50S	CPU_ITP		XDP CPU TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP		XDP CPU TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP		XDP CPU TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP		XDP CPU TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP		XDP CPU TRST L	11 24
XDP_BPM	CPU_50S	CPU_ITP		XDP BPM L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP		XDP BPM L<7..4>	11 24
XDP_DBRESET_L	CPU_50S	CPU_ITP		XDP DBRESET L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP		XDP CPU PRDY L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP		XDP CPU PREQ L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL		CPU CATERR L	11 39
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL		CPU PROC SEL L	11 20
CPU_PECI	CPU_50S	CPU_VID		CPU PECI	11 20 40
CPU_PROCHOT_L	CPU_50S	CPU_AGTL		CPU PROCHOT L	11 39 40 61
XDP_CPU_PWRGD	CPU_50S	CPU_ITP		XDP CPU PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL		PM THRMTRIP L	11 20 40
PM_SYNC	CPU_50S	CPU_AGTL		PM SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL		PM MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL		CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP		CPU SM_RCOMP<2..0>	11
CPU_VIDSOUT	CPU_50S	CPU_VID		CPU VIDSOUT	13 61
CPU_VIDSCLK	CPU_50S	CPU_VID		CPU VIDSCLK	13 61
CPU_VIDALERT_L	CPU_50S	CPU_VID		CPU VIDALERT L	13 61
CPU_VCCSA_VID<1..0>	CPU_55S	CPU_VID		CPU VCCSA_VID<1..0>	13 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_VCCSENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_VCCSENSE_N	13 61
CPU_VCCIOSENSE	CPU_27P4S	CPU_VCCIOSENSE		CPU_VCCIOSENSE_P	13 63
CPU_VCCIOSENSE	CPU_27P4S	CPU_VCCIOSENSE		CPU_VCCIOSENSE_N	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_AXG_SENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_AXG_SENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_VCC_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_VCC_VALSENSE_N	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_AXG_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_AXG_VALSENSE_N	10
CPU_VCCSASENSE	CPU_50S	CPU_AGTL		CPU_VCCSASENSE	13 58
CPU_MEM_VREF		CPU_VREF		PPCPU MEM_VREFDO_A	10 31
CPU_MEM_VREF		CPU_VREF		PPCPU MEM_VREFDO_B	10 31
CPU_MEM_VREF		CPU_VREF		PP0V75_S3_MEM_VREFDO_A	28 31
CPU_MEM_VREF		CPU_VREF		PP0V75_S3_MEM_VREFDO_B	28 31
CPU_MEM_VREF		CPU_VREF		PP0V75_S3_MEM_VREFCA_A	28 31
CPU_MEM_VREF		CPU_VREF		PP0V75_S3_MEM_VREFCA_B	28 31
XDP_CLK_ITP	CLK_BCIE_90D	CLK_BCIE		XDP CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_BCIE_90D	CLK_BCIE		XDP CPU_CLK100M_N	24

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4X_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3X_DIELECTRIC	?
MEM_CTRL2MEM	*	=3X_DIELECTRIC	?
MEM_CMD2CMD	*	=2X_DIELECTRIC	?
MEM_CMD2MEM	*	=3X_DIELECTRIC	?
MEM_DATA2DATA	*	=2X_DIELECTRIC	?
MEM_DATA2MEM	*	=3X_DIELECTRIC	?
MEM_DQS2MEM	*	=4X_DIELECTRIC	?
MEM_2OTHER	*	=6X_DIELECTRIC	?
MEM_DQBL2BL	*	=4X_DIELECTRIC	?
MEM_DQCH2CH	*	=6X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_DQS	MEM_*	*	MEM_DQS2MEM
MEM_*	*	*	MEM_2OTHER

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
 DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
 DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
 CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
 CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
 A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
 DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
 Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.
 SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK P<0>
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK N<0>
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM_A_CKE<1..0>
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM_A_CS L<1>
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM_A_CS L<0>
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM_A_ODT<1>
MEM_A_CNTRL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A A<15..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A BA<2..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A RAS L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A CAS L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A WE L
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A DQ<63..56>
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A DOS P<0>
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A DOS N<0>
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DOS P<1>
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DOS N<1>
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DOS P<2>
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DOS N<2>
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DOS P<3>
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DOS N<3>
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DOS P<4>
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DOS N<4>
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DOS P<5>
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DOS N<5>
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DOS P<6>
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DOS N<6>
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DOS P<7>
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DOS N<7>
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK P<0>
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK N<0>
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM_B_CKE<1>
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM_B_CKE<0>
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM_B_CS L<3..0>
MEM_B_CNTRL	MEM_37S	MEM_CTRL	MEM_B_ODT<1..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B A<15..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B BA<2..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B RAS L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B CAS L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B WE L
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B DQ<63..56>
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B DOS P<0>
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B DOS N<0>
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DOS P<1>
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DOS N<1>
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DOS P<2>
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DOS N<2>
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DOS P<3>
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DOS N<3>
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DOS P<4>
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DOS N<4>
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DOS P<5>
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DOS N<5>
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DOS P<6>
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DOS N<6>
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DOS P<7>
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DOS N<7>

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Digital Video Signal Constraints

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=+90_OHM_DIFF	=+90_OHM_DIFF	=+90_OHM_DIFF	=+90_OHM_DIFF	=+90_OHM_DIFF	=+90_OHM_DIFF
SATA_37SE	*	=+37_OHM_SE	=+37_OHM_SE	=+37_OHM_SE	=+37_OHM_SE	=+37_OHM_SE	=+37_OHM_SE
SATA_55SE	*	=+55_OHM_SE	=+55_OHM_SE	=+55_OHM_SE	=+55_OHM_SE	=+55_OHM_SE	=+55_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=512_SPACING	?	SATA	TOP_BOTTOM	=512_SPACING	?
SATA_ICOMP	*	15 MIL	?				

SOURCE: HK PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=412_SPACING	?	USB	TOP_BOTTOM	=412_SPACING	?
USB_RBIAS	*	15 MIL	?				

SOURCE: HK PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF	=+85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=512_SPACING	?	USB3	TOP_BOTTOM	=512_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2X_DIELECTRIC	?
CLK_25M	*	=5X_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RDRIN P 7
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RDRIN N 7
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RDROUT P 7
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RDROUT N 7
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RDRIN P 7
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RDRIN N 7
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RDROUT N 7
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RDROUT P 7
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RC P 7 37
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R RC N 7 37
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RC N 7 37
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D RC P 7 37
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P 7 17 37
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N 7 17 37
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P 7 17 37
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N 7 17 37
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA SSDRHDD D2R P 7 37
995D	SATA_HDD_D2R	SATA_90D	SATA	SATA SSDRHDD D2R N 7 37
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA SSDRHDD R2D P 7 37
995D	SATA_HDD_R2D	SATA_90D	SATA	SATA SSDRHDD R2D N 7 37
995D	PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH SATA3COMP 17
995D	PCH_SATA3_ICOMP	SATA_37SE	SATA_ICOMP	PCH SATAICOMP 17
995D	USB_EXTR	USB_85D	USB	USB EXT XHCI P 19 26
995D	USB_EXTR	USB_85D	USB	USB EXT XHCI N 19 26
995D	USB_EXTR	USB_85D	USB	USB EXT EHCI P 19 26
995D	USB_EXTR	USB_85D	USB	USB EXT EHCI N 19 26
995D	USB_HUB2_UP	USB_85D	USB	USB HUB UP P 19 26
995D	USB_HUB2_UP	USB_85D	USB	USB HUB UP N 19 26
995D	USB_EXTA	USB_85D	USB	USB EXTA P 19 38
995D	USB_EXTA	USB_85D	USB	USB EXTA N 19 38
995D	USB_EXTR	USB_85D	USB	USB EXTR P 7 26 36
995D	USB_EXTR	USB_85D	USB	USB EXTR N 7 26 36
995D	USB_EXTC	USB_85D	USB	USB EXTD P 19 38
995D	USB_EXTC	USB_85D	USB	USB EXTD N 19 38
995D	USB_CAMERA	USB_85D	USB	USB CAMERA CONN P 7 32
995D	USB_CAMERA	USB_85D	USB	USB CAMERA CONN N 7 32
995D	USB_BT	USB_85D	USB	USB BT P 7 9 36
995D	USB_BT	USB_85D	USB	USB BT N 7 9 36
995D	USB_TPAD	USB_85D	USB	USB TPAD P 9 47
995D	USB_TPAD	USB_85D	USB	USB TPAD N 9 47
995D	USB_SMC	USB_85D	USB	USB SMC P 9 39
995D	USB_SMC	USB_85D	USB	USB SMC N 9 39
995D	PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH USB RBIAS 19
995D	USB_EXTD	USB_85D	USB	USB EXTD XHCI P 19 26
995D	USB_EXTD	USB_85D	USB	USB EXTD XHCI N 19 26
995D	USB_EXTA	USB_85D	USB	USB EXTA MUXED P 38
995D	USB_EXTA	USB_85D	USB	USB EXTA MUXED N 38
995D	USB_CAMERA	USB_85D	USB	USB CAMERA P 19 32
995D	USB_CAMERA	USB_85D	USB	USB CAMERA N 19 32
995D	USB_EXTA	USB_85D	USB	USB LTI P 7 38
995D	USB_EXTA	USB_85D	USB	USB LTI N 7 38
995D	USB3_EXTB_TX	USB3_85D	USB3	USB3 EXTB TX P 19 36
995D	USB3_EXTB_TX	USB3_85D	USB3	USB3 EXTB TX N 19 36
995D	USB3_EXTB_RX	USB3_85D	USB3	USB3 EXTB RX P 7 19 36
995D	USB3_EXTB_RX	USB3_85D	USB3	USB3 EXTB RX N 7 19 36
995D	USB3_EXTA_TX	USB3_85D	USB3	USB3 EXTA TX P 19 38
995D	USB3_EXTA_TX	USB3_85D	USB3	USB3 EXTA TX N 7 19 38
995D	USB3_EXTA_RX	USB3_85D	USB3	USB3 EXTA RX P 7 19 38
995D	USB3_EXTA_RX	USB3_85D	USB3	USB3 EXTA RX N 7 19 38

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
995D	SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK CLK32K RTC 17 25
995D	SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK CLK25M SB 17 25
995D	SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK CLK25M ENET 17
995D	SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK CLK25M TBT 25 33
995D	SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK CLK25M TBT R 33

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PCH Constraints 1

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
LPC_AD	LPC_50S	LPC		LPC AD<3..0>	7 17 39 41
LPC_FRAME_L	LPC_50S	LPC		LPC FRAME L	7 17 39 41
LPC_RESET_L	LPC_50S	LPC		LPC RESET L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC		LPC CLK33M SMC R	19 25
CLK_LPC_50S	CLK_LPC	CLK_LPC		LPC CLK33M SMC	7 25 39
CLK_LPC_50S	CLK_LPC	CLK_LPC		LPC CLK33M LPCPLUS	7 25 41
SMBUS_PCH_CLK	SMB_50S	SMB		SMBUS PCH CLK	7 17 42
SMBUS_PCH_DATA	SMB_50S	SMB		SMBUS PCH DATA	7 17 42
SMBUS_PCH_0_CLK	SMB_50S	SMB		SML PCH 0 CLK	17 42
SMBUS_PCH_0_DATA	SMB_50S	SMB		SML PCH 0 DATA	17 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB		SML PCH 1 CLK	17 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB		SML PCH 1 DATA	17 42
HDA_BIT_CLK	HDA_50S	HDA		HDA BIT CLK	17 51
HDA_BIT_CLK_R	HDA_50S	HDA		HDA BIT CLK R	17
HDA_SYNC	HDA_50S	HDA		HDA SYNC	17 51
HDA_SYNC_R	HDA_50S	HDA		HDA SYNC R	17
HDA_RST_L	HDA_50S	HDA		HDA RST R L	17
HDA_RST_L	HDA_50S	HDA		HDA RST L	17 51
HDA_SDIN0	HDA_50S	HDA		HDA SDIN0	17 51
HDA_SDI_R	HDA_50S	HDA		AUD SDI R	51
HDA_SDOIT	HDA_50S	HDA		HDA SDOIT	17 51
HDA_SDOIT_R	HDA_50S	HDA		HDA SDOIT R	17 25
SPI_CLK	SPI_55S	SPI		SPI CLK R	17 41
SPI_CLK	SPI_55S	SPI		SPI CLK	41
SPI_MOSI	SPI_55S	SPI		SPI MOSI R	17 41
SPI_MOSI	SPI_55S	SPI		SPI MOSI	41
SPI_MISO	SPI_55S	SPI		SPI MISO	17 41
SPI_CS0	SPI_55S	SPI		SPI CS0 R L	17 41
SPI_CS0	SPI_55S	SPI		SPI CS0 L	41
PCIE_ENET_R2D	PCIE_85D	PCIE		PCIE ENET R2D C P	7 17 36
PCIE_ENET_R2D	PCIE_85D	PCIE		PCIE ENET R2D C N	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE		PCIE ENET D2R P	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE		PCIE ENET D2R N	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE		PCIE AP R2D P	7 36
PCIE_AP_R2D	PCIE_85D	PCIE		PCIE AP R2D N	7 36
PCIE_AP_R2D	PCIE_85D	PCIE		PCIE AP R2D C P	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE		PCIE AP R2D C N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE		PCIE AP D2R P	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE		PCIE AP D2R N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE		PCIE AP D2R PI P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE		PCIE AP D2R PI N	7 36
PCIE_AP_D2R	PCIE_85D	PCIE		PCIE AP R2D PI P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE		PCIE AP R2D PI N	7 36
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M PCH P	7 17
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M PCH N	7 17
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M TBT P	7 17 33
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M TBT N	7 17 33
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE		PCH CLK96M DOT P	17
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE		PCH CLK96M DOT N	17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE		PCH CLK100M SATA P	7 17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE		PCH CLK100M SATA N	17
CPU_50S	CLK_PCIE			PCH CLK14P3M REFCLK	17
CPU_50S	CLK_PCIE			PCH CLK33M PCIIN	7 17 25
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M SSD P	7 9 17
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M SSD N	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE		PEG CLK100M P	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE		PEG CLK100M N	7 9 17
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M ENET P	7 17 36
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M ENET N	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M AP P	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M AP N	7 17 36
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M FW P	7 9 17
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M FW N	7 9 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M EXCARD P	7 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE		PCIE CLK100M EXCARD N	7 17
PCIE_TBT_R2D	PCIE_85D	PCIE		PCIE TBT R2D C P<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE		PCIE TBT R2D C N<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE		PCIE TBT R2D P<3..0>	7 33
PCIE_TBT_R2D	PCIE_85D	PCIE		PCIE TBT R2D N<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE		PCIE TBT D2R P<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE		PCIE TBT D2R N<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE		PCIE TBT D2R C P<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE		PCIE TBT D2R C N<3..0>	7 33

SYNC MASTER=15 MLB SYNC DATE=07/29/2011

PAGE TITLE: PCH Constraints 2

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?	TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.

TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.

Proper differential impedance depends on mDP connector used.

For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?	HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT A R2D C P<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT A R2D C N<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT A R2D P<1..0>	7 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT A R2D N<1..0>	7 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C P<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML C N<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML P<3..1:2>	69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP TBTPA ML N<3..1:2>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML P<1>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP A LSX ML N<1>	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT A D2R C P<1>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT A D2R C N<1>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT A D2R C P<0>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT A D2R C N<0>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT A D2R P<1>	7 33 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT A D2R N<1>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT A D2R P<0>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT A D2R N<0>	7 33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C P	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP TBTPA AUXCH C N	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP TBTPA AUXCH P	69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP TBTPA AUXCH N	69
	DP_85D	DISPLAYPORT	DP A AUXCH DDC P	69
	DP_85D	DISPLAYPORT	DP A AUXCH DDC N	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT A D2R1 AUXDDC P	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT A D2R1 AUXDDC N	69
TBT_B_R2D	TBTDP_85D	TBTDP	TBT B R2D C P<1..0>	7 33 70
TBT_B_R2D	TBTDP_85D	TBTDP	TBT B R2D C N<1..0>	7 33 70
TBT_B_R2D	TBTDP_85D	TBTDP	TBT B R2D P<1..0>	7 70
TBT_B_R2D	TBTDP_85D	TBTDP	TBT B R2D N<1..0>	7 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C P<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML C N<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML P<3..1:2>	70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP TBTPB ML N<3..1:2>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML P<1>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP B LSX ML N<1>	70
TBT_B_D2R0	TBTDP_85D	TBTDP	TBT B D2R C P<0>	7 70
TBT_B_D2R0	TBTDP_85D	TBTDP	TBT B D2R C N<0>	7 70
TBT_B_D2R1	TBTDP_85D	TBTDP	TBT B D2R C P<1>	7 70
TBT_B_D2R1	TBTDP_85D	TBTDP	TBT B D2R C N<1>	7 70
TBT_B_D2R0	TBTDP_85D	TBTDP	TBT B D2R P<0>	7 33 70
TBT_B_D2R0	TBTDP_85D	TBTDP	TBT B D2R N<0>	7 33 70
TBT_B_D2R1	TBTDP_85D	TBTDP	TBT B D2R P<1>	7 33 70
TBT_B_D2R1	TBTDP_85D	TBTDP	TBT B D2R N<1>	7 33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C P	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP TBTPB AUXCH C N	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP TBTPB AUXCH P	70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP TBTPB AUXCH N	70
	DP_85D	DISPLAYPORT	DP B AUXCH DDC P	70
	DP_85D	DISPLAYPORT	DP B AUXCH DDC N	70
TBT_B_D2R1	TBTDP_85D	TBTDP	TBT B D2R1 AUXDDC P	70
TBT_B_D2R1	TBTDP_85D	TBTDP	TBT B D2R1 AUXDDC N	70

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP TBTSRC ML C P<3..0>	
	DP_85D	DISPLAYPORT	DP TBTSRC ML C N<3..0>	
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C P	
	DP_85D	DISPLAYPORT	DP TBTSRC AUXCH C N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT SPI CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT SPI MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT SPI MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT SPI CS L	33

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=T29 CR SYNC DATE=08/31/2011

Thunderbolt Constraints

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
<input type="checkbox"/> SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 39 42
<input type="checkbox"/> SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 39 42
<input type="checkbox"/> SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	7 39 42
<input type="checkbox"/> SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	7 39 42
<input type="checkbox"/> SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	39 42
<input type="checkbox"/> SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	39 42
<input type="checkbox"/> SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
<input type="checkbox"/> SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
<input type="checkbox"/> SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	39 42
<input type="checkbox"/> SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	39 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
<input type="checkbox"/> CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	57
<input type="checkbox"/> CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_N	57
<input type="checkbox"/> CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	57
<input type="checkbox"/> CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_N	57

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SMC Constraints			
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations
Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1T01_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1T01_55S	*	SENSE_1T01_55S
THERM_1T01_55S	*	THERM_1T01_55S
DIFFPAIR	*	DIFFPAIR

Graphics SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
SENSE_DIEFPATR	THERM_1T01_55S	THERM		CPUTHMSNS D2 P
SENSE_DIEFPATR	THERM_1T01_55S	THERM		CPUTHMSNS D2 N
SENSE_DIEFPATR	THERM_1T01_55S	THERM		CPU THERMD P
SENSE_DIEFPATR	THERM_1T01_55S	THERM		CPU THERMD N
SENSE_DIEFPATR	THERM_1T01_55S	THERM		GPUTHMSNS D P
SENSE_DIEFPATR	THERM_1T01_55S	THERM		GPUTHMSNS D N
SENSE_DIEFPATR	THERM_1T01_55S	THERM		GPU TDIODE P
SENSE_DIEFPATR	THERM_1T01_55S	THERM		GPU TDIODE N
SENSE_DIEFPATR	THERM_1T01_55S	THERM		TBT THERMD P
SENSE_DIEFPATR	THERM_1T01_55S	THERM		TBT THERMD N
SENSE_DIEFPATR	THERM_1T01_55S	THERM		DDR3THMSNS D1 P
SENSE_DIEFPATR	THERM_1T01_55S	THERM		DDR3THMSNS D1 N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		CPUVCCIOS0 CS P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		CPUVCCIOS0 CS N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		CPU_VDDQ_SENSE_P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		CPU_VDDQ_SENSE_N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS LCD PANEL P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS LCD PANEL N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS 1V35 S3 MEM P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS 1V35 S3 MEM N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS SSD P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS SSD N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS 3V3 S0 SSD R P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS 3V3 S0 SSD R N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS WLAN P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS WLAN N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS LCDBKLT P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS LCDBKLT N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS TBT P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS TBT N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS 1V35 S3 MEM R P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		ISNS 1V35 S3 MEM R N
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		VCCSAS0 CS P
SENSE_DIEFPATR	SENSE_1T01_55S	SENSE		VCCSAS0 CS N
HDMI_CLK	HDMI_90D	HDMI		HDMI IG CLK C P
HDMI_CLK	HDMI_90D	HDMI		HDMI IG CLK C N
HDMI_DATA	HDMI_90D	HDMI		HDMI IG DATA C P<2..0>
HDMI_DATA	HDMI_90D	HDMI		HDMI IG DATA C N<2..0>

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE		PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE		PCIE_CLK100M_AP_CONN_N
1T01_DIEFPATR				CHGR_CSI_R_P
1T01_DIEFPATR				CHGR_CSI_R_N
1T01_DIEFPATR				CHGR_CSO_R_P
1T01_DIEFPATR				CHGR_CSO_R_N
USB_RT	USB_85D	USB		USB_BT_CONN_P
USB_RT	USB_85D	USB		USB_BT_CONN_N
USB_RT	USB_85D	USB		USB_BT_WAKE_P
USB_RT	USB_85D	USB		USB_BT_WAKE_N
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_SL_OUT_P
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_SL_OUT_N
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_SR_OUT_P
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_SR_OUT_N
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_L_OUT_P
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_L_OUT_N
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_R_OUT_P
DIFFPAIR	DIFFPAIR	AUDIO		SPKRCONN_R_OUT_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISNSG_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISNSG_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS1G_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS1G_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS2G_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS2G_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISUMG_R_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISUMG_R_N
SENSE_1T01_55S	SENSE			ISNS_HS_OTHER_P
SENSE_1T01_55S	SENSE			ISNS_HS_OTHER_N
SENSE_1T01_55S	SENSE			ISNS_HS_COMPUTING_P
SENSE_1T01_55S	SENSE			ISNS_HS_COMPUTING_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS1_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS1_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS2_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISNS2_N
SENSE_1T01_55S	SENSE			CPUI MVP_ISUMG_R_P
SENSE_1T01_55S	SENSE			CPUI MVP_ISUMG_R_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO1_L_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO1_L_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO1_R_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO1_R_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO2_L_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO2_L_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO2_R_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_LO2_R_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_MIC_INL_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_MIC_INL_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_LIN_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_LIN_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_RIN_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_RIN_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_LSUBIN_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_LSUBIN_N
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_RSUBIN_P
AUDIODIFF	AUDIODIFF	AUDIO		AUD_SPKRAMP_RSUBIN_N
AUDIODIFF	AUDIODIFF	AUDIO		RSUBIN_P
AUDIODIFF	AUDIODIFF	AUDIO		RSUBIN_N
AUDIODIFF	AUDIODIFF	AUDIO		LSUBIN_P
AUDIODIFF	AUDIODIFF	AUDIO		LSUBIN_N
AUDIODIFF	AUDIODIFF	AUDIO		SPKRAMP_LIN_P
AUDIODIFF	AUDIODIFF	AUDIO		SPKRAMP_LIN_N
AUDIODIFF	AUDIODIFF	AUDIO		SPKRAMP_RIN_P
AUDIODIFF	AUDIODIFF	AUDIO		SPKRAMP_RIN_N
AUDIODIFF	AUDIODIFF	AUDIO		HS_MIC_HI_RC
AUDIODIFF	AUDIODIFF	AUDIO		HS_MIC_LO_RC
AUDIODIFF	AUDIODIFF	AUDIO		HS_MIC_HI
AUDIODIFF	AUDIODIFF	AUDIO		HS_MIC_LO
AUDIODIFF	AUDIODIFF	AUDIO		SPKRCONN_L_OUT_P
AUDIODIFF	AUDIODIFF	AUDIO		SPKRCONN_L_OUT_N
AUDIODIFF	AUDIODIFF	AUDIO		SPKRCONN_R_OUT_P
AUDIODIFF	AUDIODIFF	AUDIO		SPKRCONN_R_OUT_N
USB_TP4D	USB_85D	USB		USB_TP4D_R_P
USB_TP4D	USB_85D	USB		USB_TP4D_R_N
USB_HUB	USB_85D	USB		PV_USBHUB_DN4_P
USB_HUB	USB_85D	USB		PV_USBHUB_DN4_N
SB_POWER				PP3V3_S5
SB_POWER				PP3V3_S0
SB_POWER				PP1V5_S3RS0_CPUDDR
GND				GND

Project Specific Constraints

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D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA, BGA_MEM			MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.124 MM	0.124 MM	0.200 MM	0.200 MM	0.200 MM
72_OHM_DIFF	ISL2, ISL11	Y	0.124 MM	0.124 MM	0.200 MM	0.200 MM	0.200 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.089 MM	0.089 MM	0.180 MM	0.180 MM	0.180 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM	0.180 MM	0.180 MM	0.180 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.081 MM	0.081 MM	0.200 MM	0.200 MM	0.200 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.081 MM	0.081 MM	0.200 MM	0.200 MM	0.200 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

Stackup-Defined Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP, BOTTOM	0.1 MM	?
1:1_SPACING	ISL3, ISL4, ISL9, ISL10	0.1 MM	?
1:1_SPACING	ISL2, ISL11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal, Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3, ISL4, ISL9, ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2, ISL11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH C P
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH C N
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH C P
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH C N
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML C P<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML C N<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML C P<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML C N<3..0>
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH P
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH N
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH P
DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBT_AUXCH N
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML P<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML N<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML P<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBT_ML N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML C P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML C N<3..0>
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX C P
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX C N
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX P
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX N
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML F P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML F N<3..0>
USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX RC P
USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX RC N
USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX F P
USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX F N
USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX C P
USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX C N
USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX C P
USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX C N

SYNC MASTER=J5.MLB SYNC DATE=07/29/2011

PCB Rule Definitions

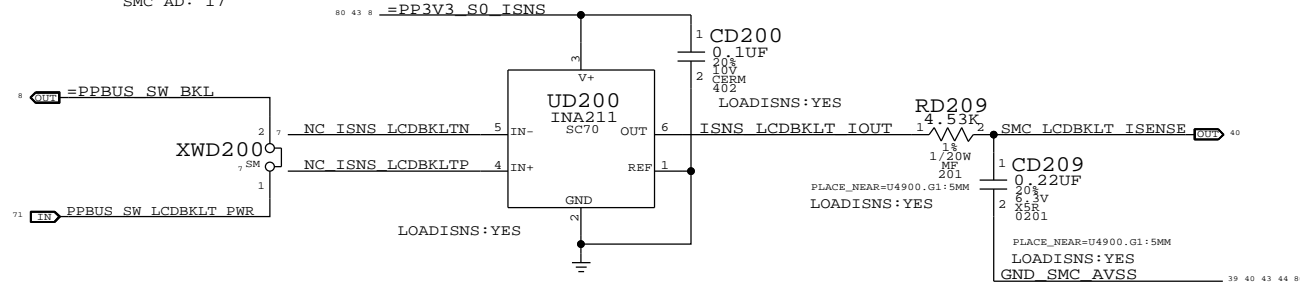
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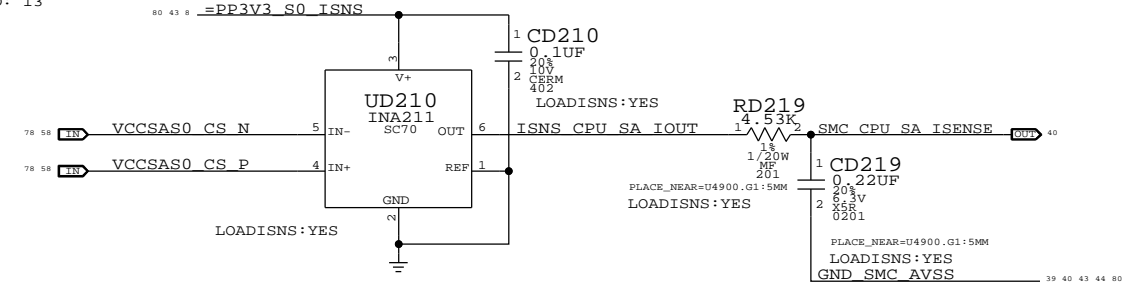
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
 Rsense: 0.005 (RD200 / XWD200)
 V across Rsense: 4.5 mV
 SMC AD: 17



CPU SA Current Sense (IC2C)

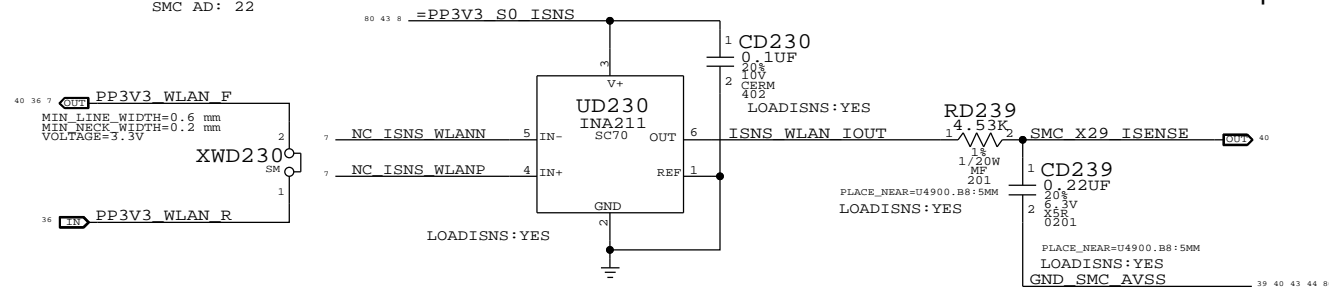
Gain: 500x. EDP: 6 A
 Rsense: 0.001 (R7140)
 V across Rsense: 6 mV
 SMC AD: 13



Airport X29 Current Sense (IAPC)

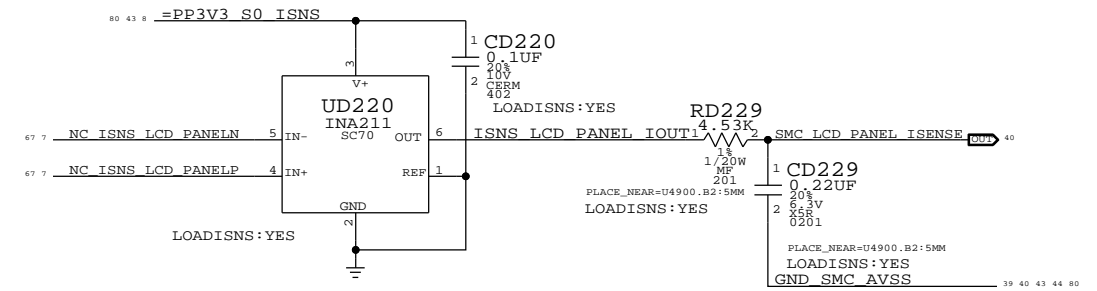
Gain: 500x. EDP: 1.06 A
 Rsense: 0.005 (RD230 / XWD230)
 V across Rsense: 5.3 mV
 SMC AD: 22

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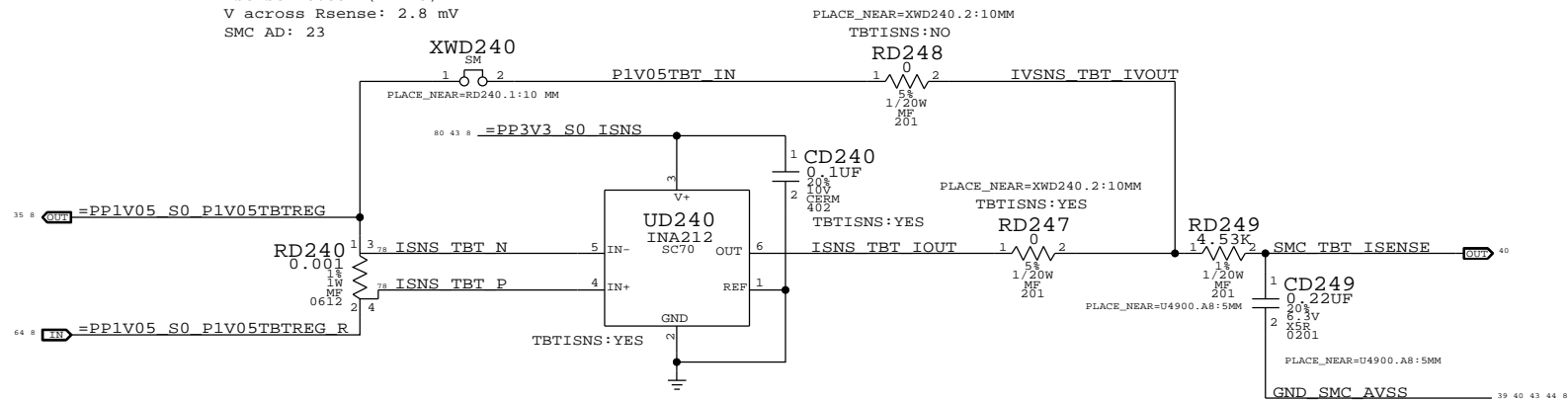
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
 Rsense: 0.005 (R9020, XW9020)
 V across Rsense: 5 mV
 SMC AD: 15



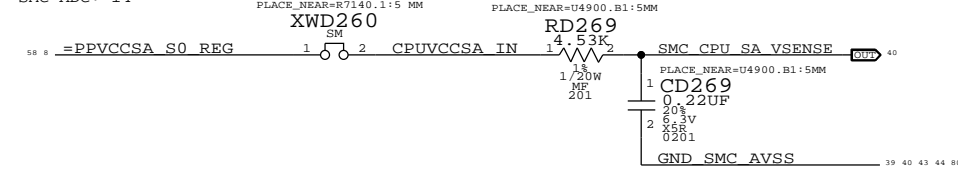
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
 Rsense: 0.001 (RD240)
 V across Rsense: 2.8 mV
 SMC AD: 23



CPU SA Voltage Sense (VC2C)

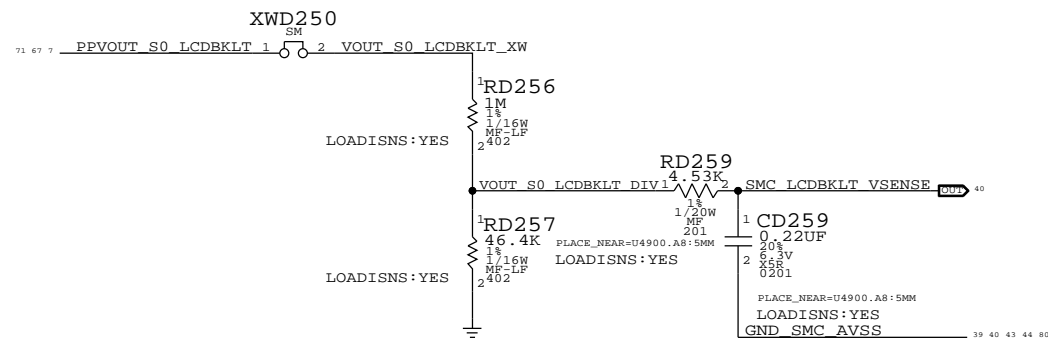
Gain: 1x
 SMC ADC: 14



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



Power Sensors: Extended

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