1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,J45

DVT 8/6/2013

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0456	1	SCHEM,MLB,J45	SCH	CRITICAL	
820-3662	1	PCBF,MLB,J45	PCB	CRITICAL	

DRAWING

TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Tue Aug 6 17:09:28 2013

DRAWING TITLE: <PART_DESCRIPTION>

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0067	COMMON PARTS,MLB,J45	J45_COMMON
985-0045	DEV BOM,MLB,J45	J45_DEVEL:ENG
639-4822	PCBA,MLB,BETTER,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600_S
639-4823	PCBA,MLB,BETTER,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:HYNIX_1600
639-4828	PCBA,MLB,BETTER,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600_S
639-4829	PCBA,MLB,BETTER,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:ELPIDA_1600
639-4834	PCBA,MLB,BETTER,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600_S
639-4835	PCBA,MLB,BETTER,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BETTER,RAM:MICRON_1600
639-4840	PCBA,MLB,BEST,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600_S
639-4841	PCBA,MLB,BEST,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:HYNIX_1600
639-4846	PCBA,MLB,BEST,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600_S
639-4847	PCBA,MLB,BEST,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:ELPIDA_1600
639-4852	PCBA,MLB,BEST,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600_S
639-4853	PCBA,MLB,BEST,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:MICRON_1600
639-4858	PCBA,MLB,CTO,8G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600_S
639-4859	PCBA,MLB,CTO,16G HYN,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:HYNIX_1600
639-4864	PCBA,MLB,CTO,8G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600_S
639-4865	PCBA,MLB,CTO,16G ELP,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:ELPIDA_1600
639-4870	PCBA,MLB,CTO,8G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600_S
639-4871	PCBA,MLB,CTO,16G MIC,J45	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600

J45 BOM Groups

BOM GROUP	BOM OPTIONS
J45_COMMON	ALTERNATE,COMMON,J45_COMMON1,J45_COMMON2,J45_PROGPARTS
J45_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X16,S2_PWR:S0
J45_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45_PVB	BKLT:PROD,SENSOR_NONPROD:N
J45_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:DVT,TBTROM:PROG,TPAD_PSOC:PROG
J45_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,CAM_XTAL:YES
J45_DEVEL:FSB	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,SENSOR_NONPROD_R
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	CRW,SR18J,,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	CRW,SR18H,PRQ,C0,2.3,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	CRW,SR1BS,PRQ,C0,2.6,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QHWV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA		CRITICAL	HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG		CRITICAL	SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P		CRITICAL	ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600_S	HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600_S	SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600_S	ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600_S	MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:SAMSUNG_1600	SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:ELPIDA_1600	ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0067	1	J45 MLB BASE BOM	BASE	CRITICAL	BASE_BOM
985-0045	1	J45 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

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Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S3919	1	IC,EPROM,Falcon RIDGE(V13.9)J44/45	U2890	CRITICAL	TBTROM:PROG
337S4587	1	IC,TP PSOC, QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK
341S3856	1	IC,TRKPD/KYBD,PSOC(V225)	U4801	CRITICAL	TPAD_PSOC:PROG

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3902	1	IC,SMC-B1,EXT,V2.12A54,EVT,J45	U5000	CRITICAL	SMC_PROG:EVT
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK:MACRONIX
335S0812	1	IC,SPI SRL 50MHZ,FLASH,64MBIT,SOIC8	U6100	CRITICAL	BOOTROM_BLANK:NUMONYX
341S3763	1	IC,EFI ROM(VXXXX)PROTO 0,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S3780	1	IC,EFI ROM(V0035)PRE-PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PRE-PROTO1
341S3793	1	IC,EFI ROM(V0041)PROTO 1,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3811	1	IC,EFI ROM(V00xx)PROTO 2,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S3890	1	IC,EFI ROM(V0100)PROTO3-J45 &EVT-J45	U6100	CRITICAL	BOOTROM_PROG:EVT
341S3929	1	IC,EFI ROM(Vxxxx)DVT-J45	U6100	CRITICAL	BOOTROM_PROG:DVT

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7845	1	MBP BARCODE LABEL	LABEL	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0241		ALL	Cyntec alt to TFT
376S1032	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
128S0371	128S0376		ALL	Kemet alt to Sanyo
333S0629	333S0703		ALL	Elpida F die alt
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba (U2030, U7001)

SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE: BOM Configuration

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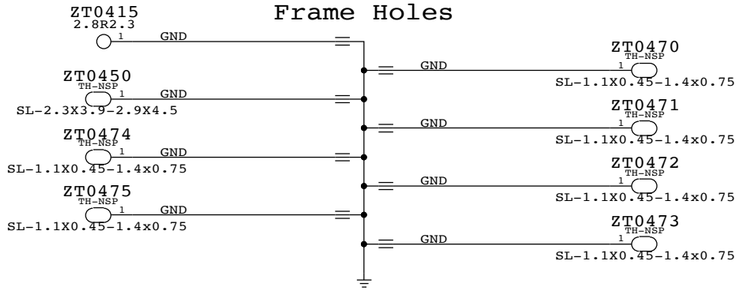
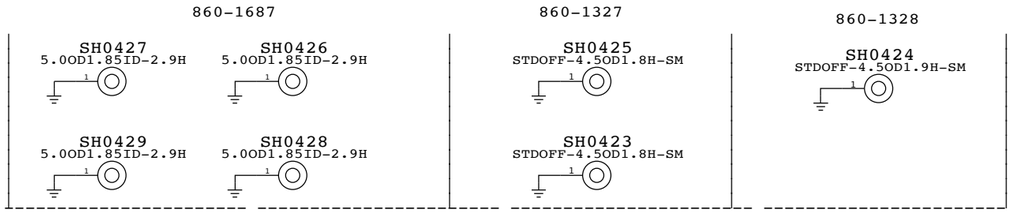
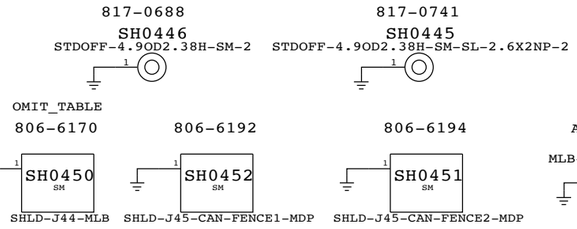
Frame Holes

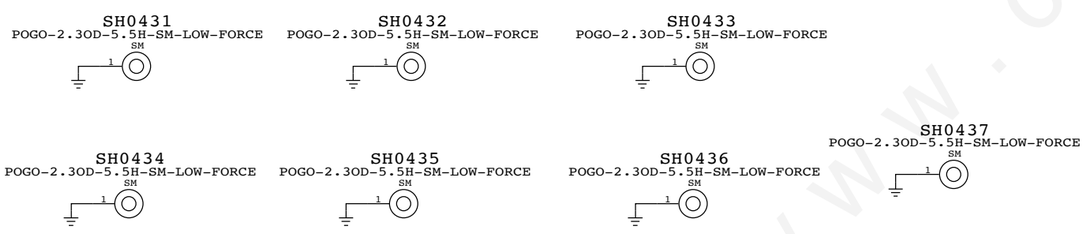


J45 THERMAL MODULE STANDOFF

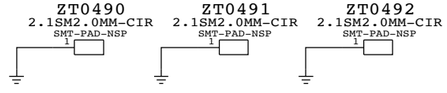




J45 POGO PINS

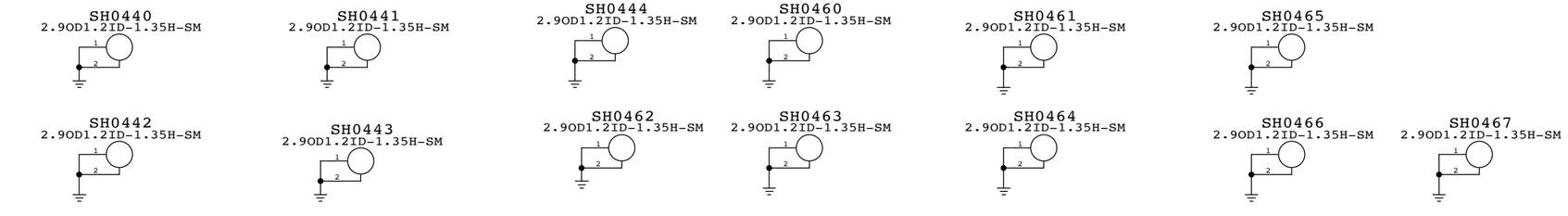


SMT GND TEST PONTS



J45 StAND OFF

860-1448



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
725-1807	1	INSULATOR,REAR,MLB,J45	REAR_INSULATOR	CRITICAL	
725-1877	1	INSULATOR,CPU,J45	CPU_INSULATOR	CRITICAL	
725-1787	1	INSULATOR,PCH,J15	PCH_INSULATOR	CRITICAL	
806-6193	2	CAN COVER,mDP	CAN_COVER1, CAN_COVER2	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
806-9391	1	SHIELD CAN, USB,J45	SH0450	CRITICAL	

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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PD Parts

Apple Inc.

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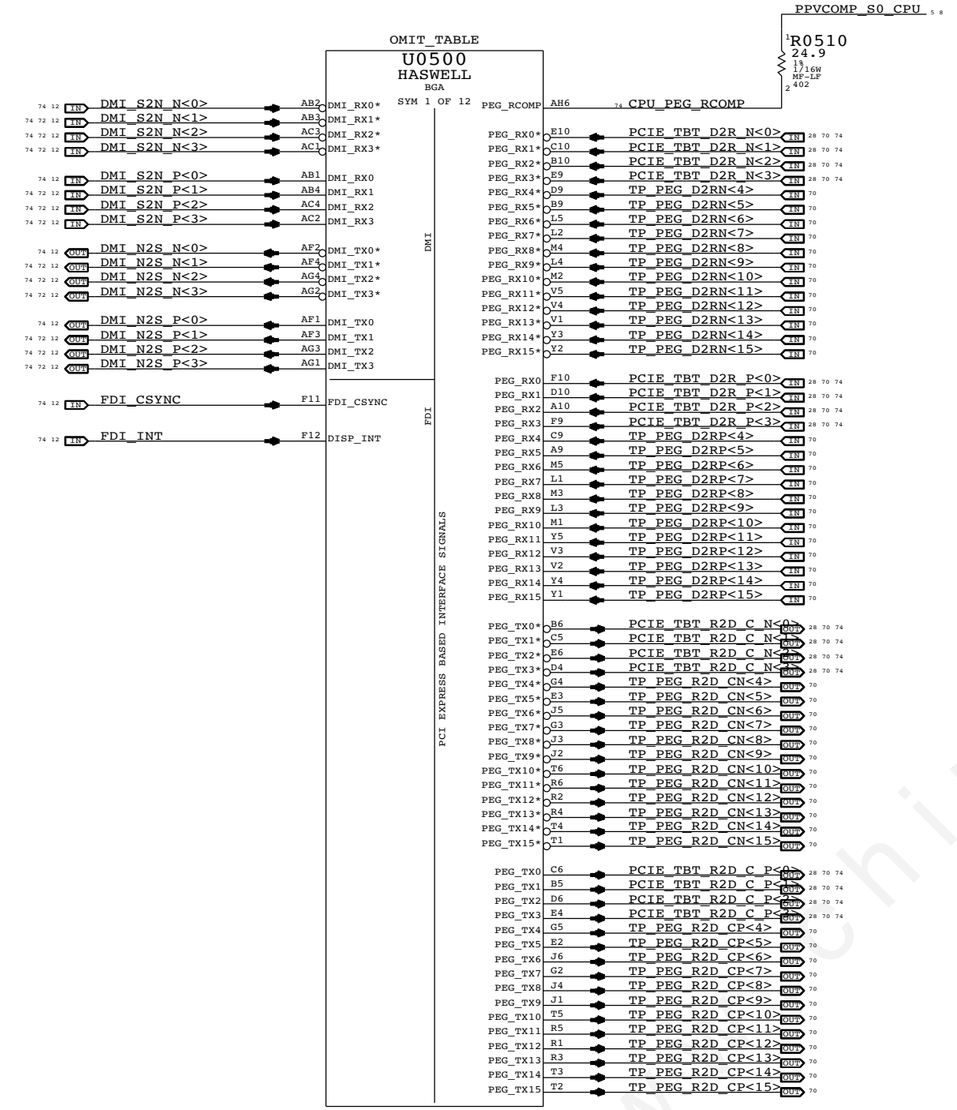

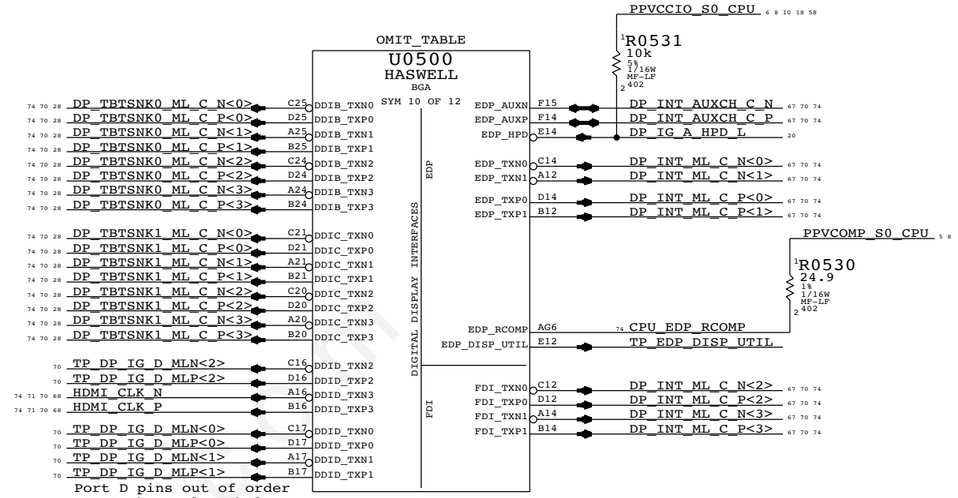

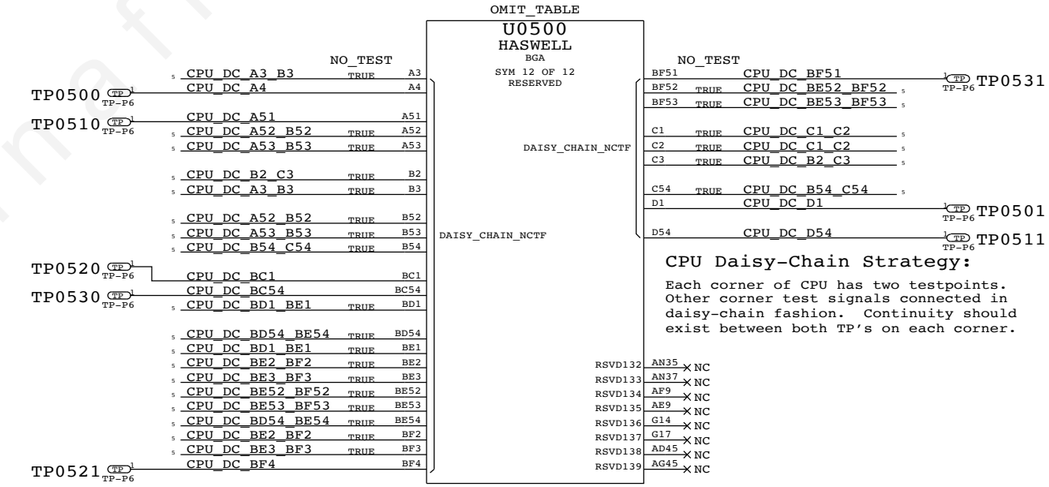

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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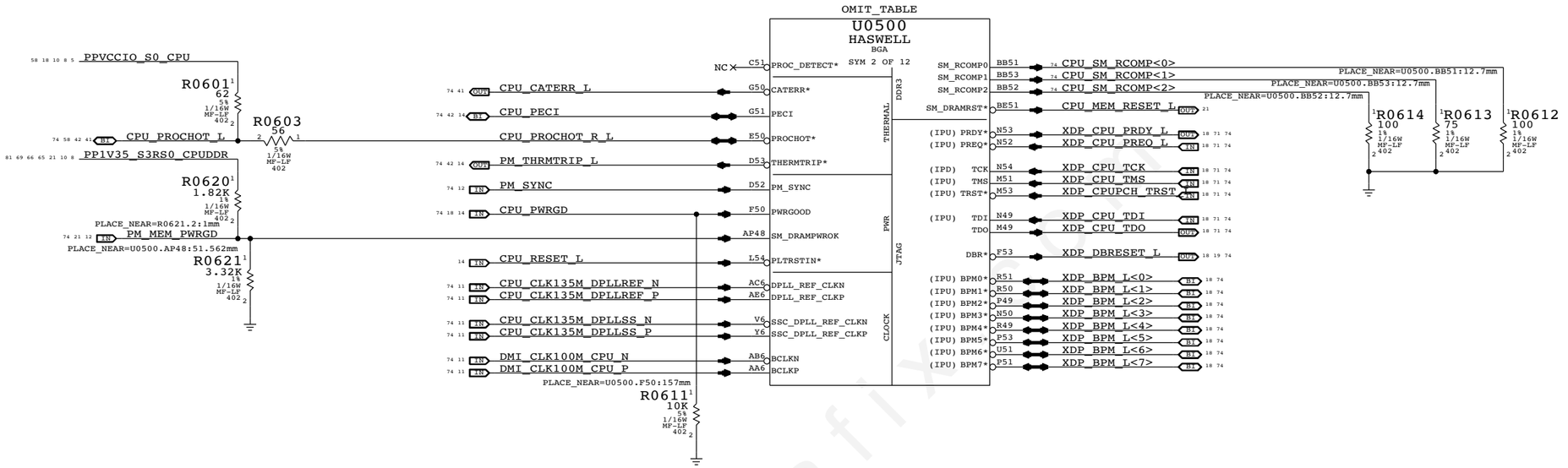
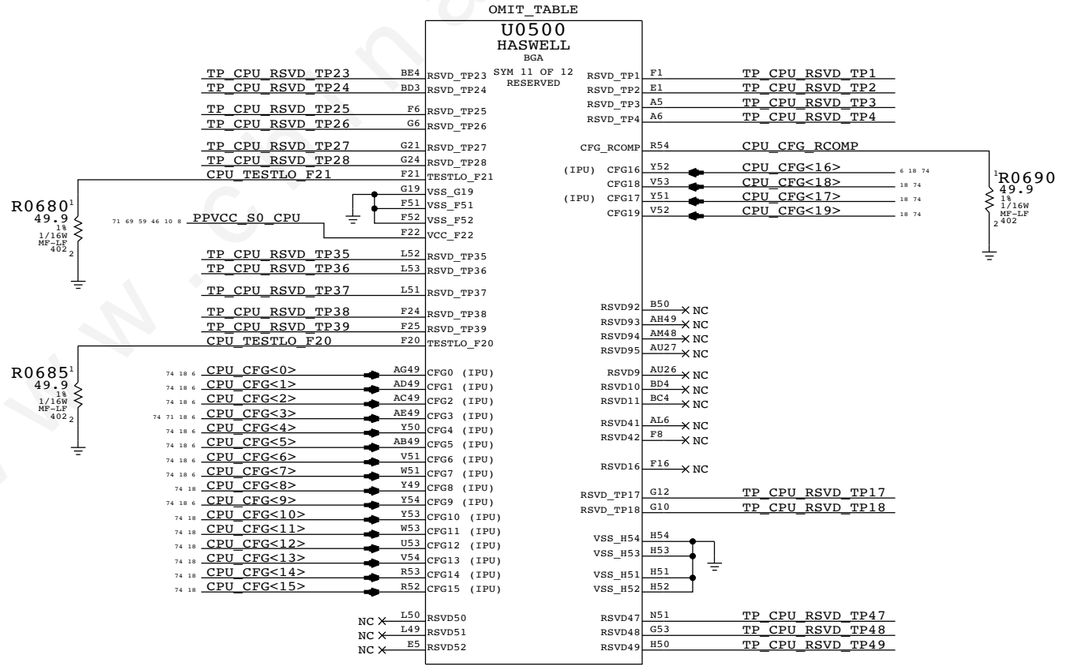
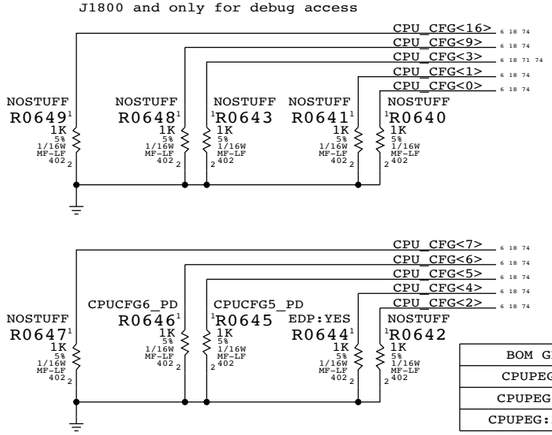





```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION   0 = LANES REVERSED
```

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

Apple Inc.

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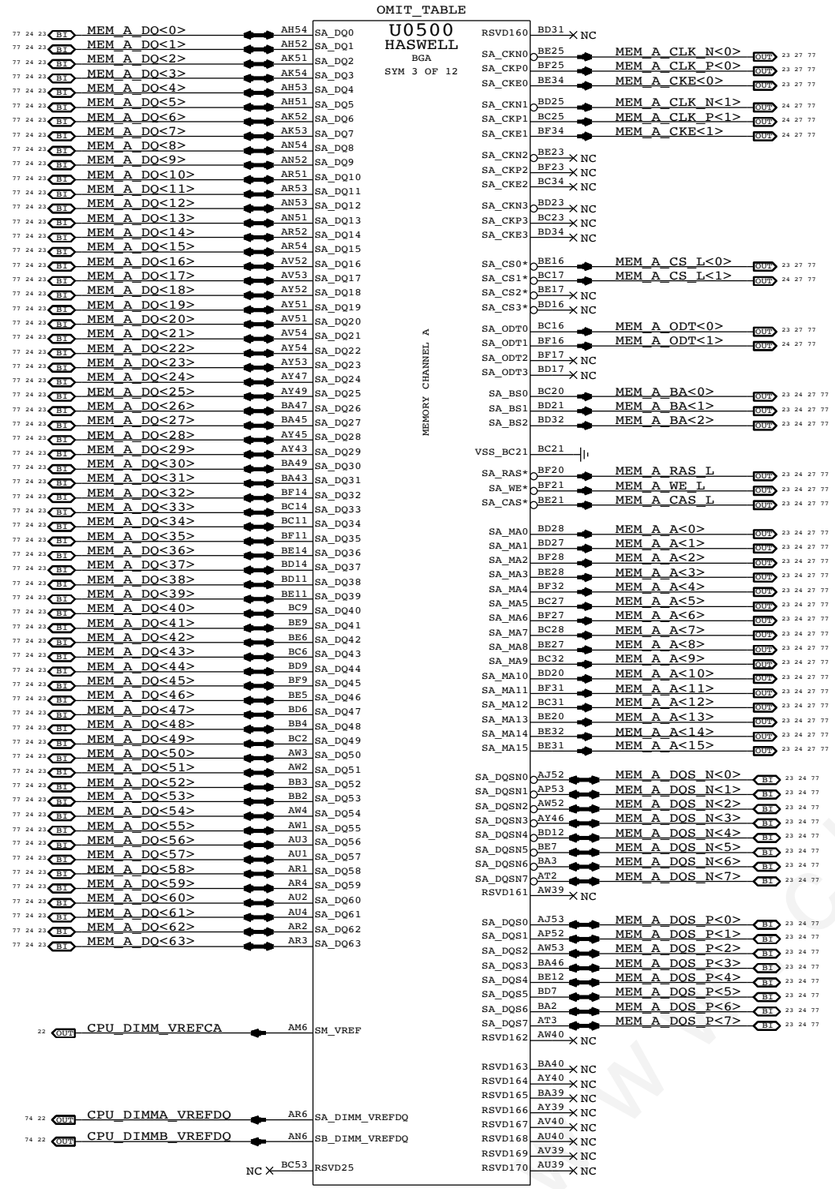

SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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REVISION <E4LABEL>

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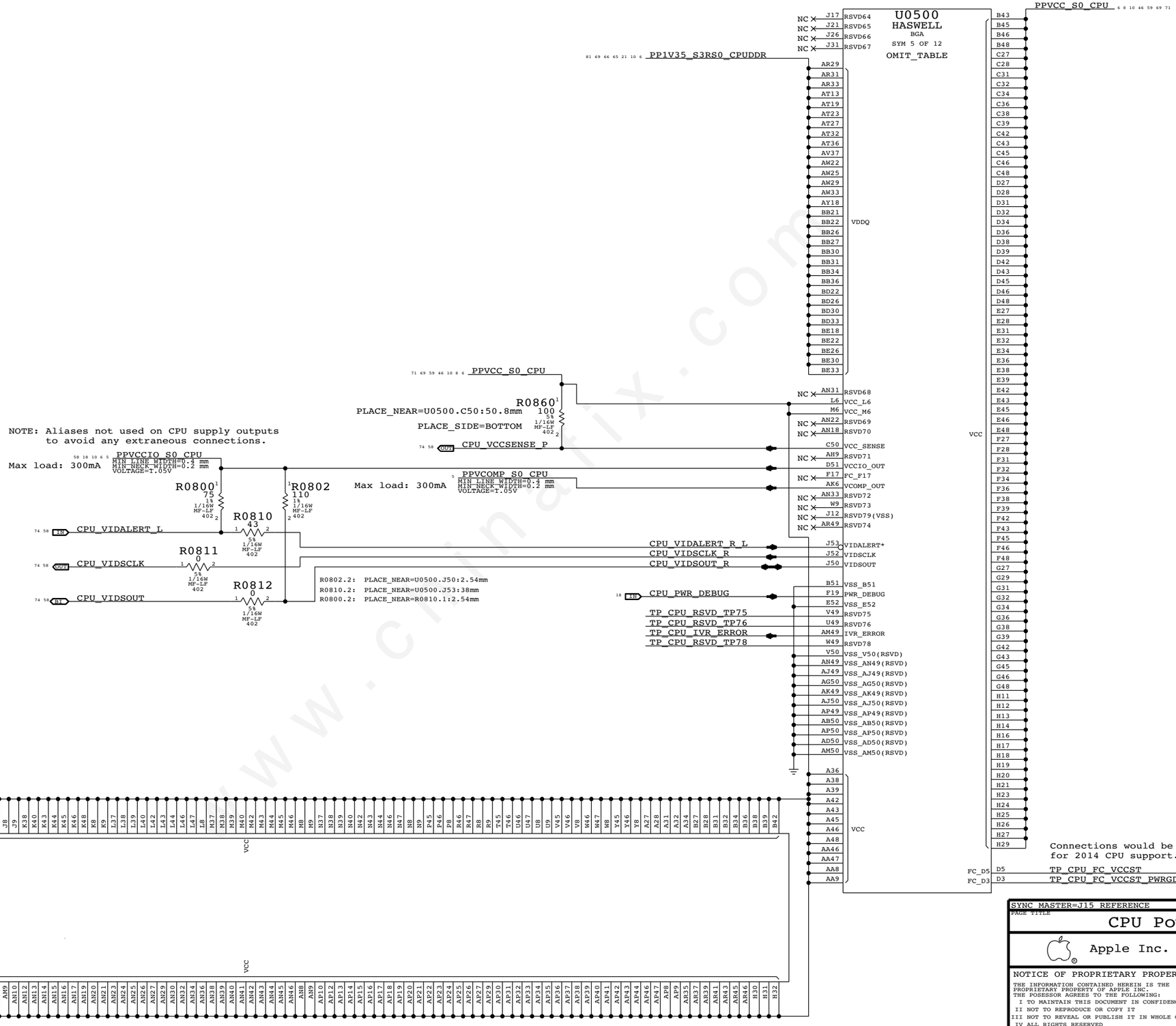

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

CPU Power

Apple Inc.

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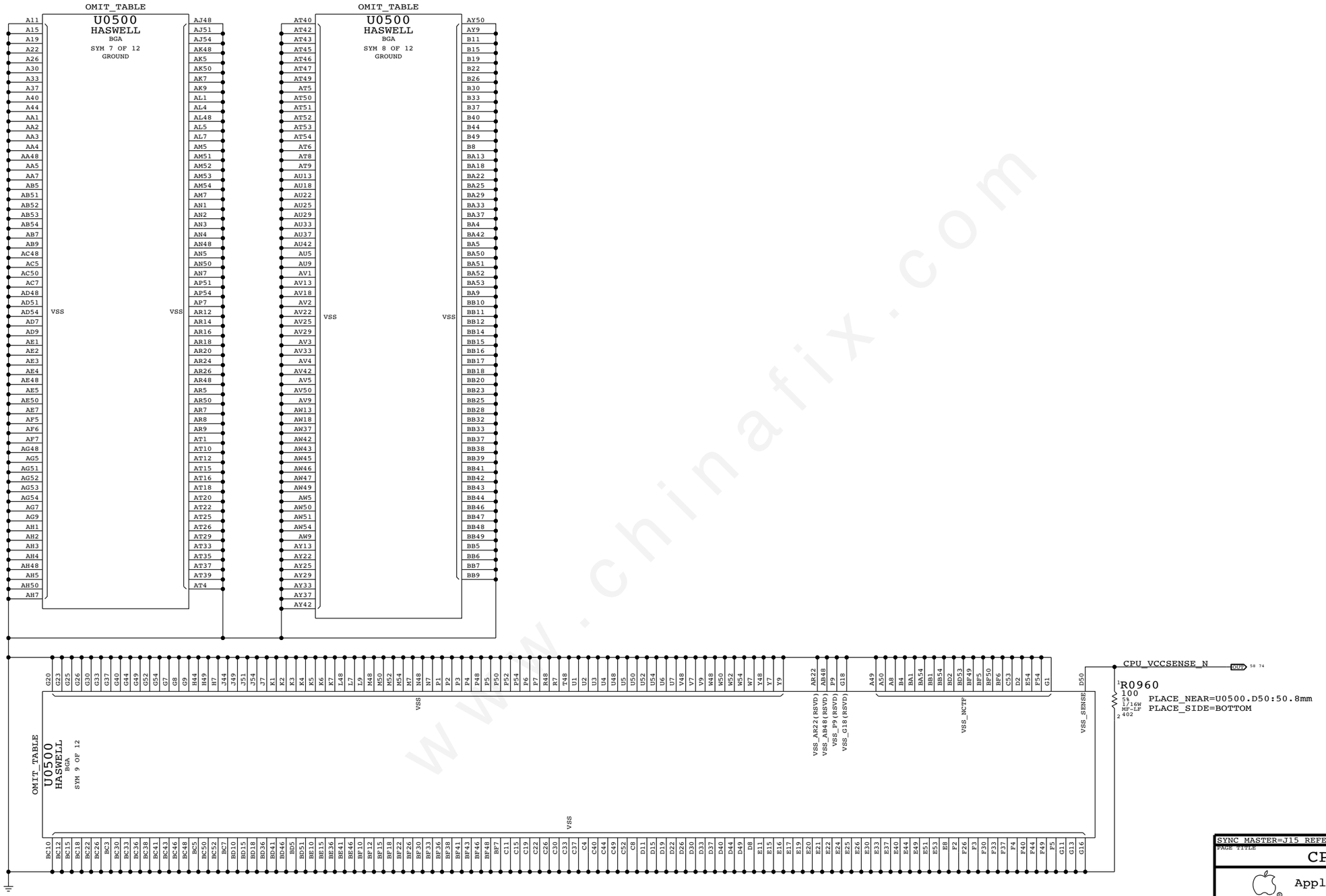

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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CPU Ground

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 8x 210uF(2x nostuff) 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

71 69 59 46 8 6 PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):

Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 | C1001 1UF 10% 10V X6S-CERM 0402 | C1002 1UF 10% 10V X6S-CERM 0402 | C1003 1UF 10% 10V X6S-CERM 0402 | C1004 1UF 10% 10V X6S-CERM 0402 | C1005 1UF 10% 10V X6S-CERM 0402 | C1006 1UF 10% 10V X6S-CERM 0402 | C1007 1UF 10% 10V X6S-CERM 0402 | C1008 1UF 10% 10V X6S-CERM 0402 | C1009 1UF 10% 10V X6S-CERM 0402 | C1010 1UF 10% 10V X6S-CERM 0402 | C1011 1UF 10% 10V X6S-CERM 0402 | C1012 1UF 10% 10V X6S-CERM 0402 | C1013 1UF 10% 10V X6S-CERM 0402 | C1014 1UF 10% 10V X6S-CERM 0402 | C1015 1UF 10% 10V X6S-CERM 0402 | C1016 1UF 10% 10V X6S-CERM 0402 | C1017 1UF 10% 10V X6S-CERM 0402 | C1018 1UF 10% 10V X6S-CERM 0402 | C1019 1UF 10% 10V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1020-C1023):

CAPs for Acoustic control (C109A-C102D)

Place near U0500 on bottom side NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF

C1020 20UF 20% 4V X5R-CERM 0402-2 | C1021 20UF 20% 4V X5R-CERM 0402-2 | C1022 20UF 20% 4V X5R-CERM 0402-2 | C1023 20UF 20% 4V X5R-CERM 0402-2 | C109A 20UF 20% 4V X5R-CERM 0402-2 | C109B 20UF 20% 4V X5R-CERM 0402-2 | C109C 20UF 20% 4V X5R-CERM 0402-2 | C109D 20UF 20% 4V X5R-CERM 0402-2 | C109E 20UF 20% 4V X5R-CERM 0402-2 | C109F 20UF 20% 4V X5R-CERM 0402-2 | C101A 20UF 20% 4V X5R-CERM 0402-2 | C101B 20UF 20% 4V X5R-CERM 0402-2 | C101C 20UF 20% 4V X5R-CERM 0402-2 | C101D 20UF 20% 4V X5R-CERM 0402-2 | C101E 20UF 20% 4V X5R-CERM 0402-2 | C101F 20UF 20% 4V X5R-CERM 0402-2 | C102A 20UF 20% 4V X5R-CERM 0402-2 | C102B 20UF 20% 4V X5R-CERM 0402-2 | C102C 20UF 20% 4V X5R-CERM 0402-2 | C102D 20UF 20% 4V X5R-CERM 0402-2

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1024-C1045):

Place near inductors on bottom side. NO STUFF

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1025 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1026 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1027 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1028 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1029 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1030 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1031 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1032 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1033 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1034 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1035 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1036 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1037 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1038 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1039 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1040 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1041 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1042 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1043 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1044 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1045 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1046-C1067):

Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1047 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1048 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1049 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1050 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1051 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1052 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1053 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1054 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1055 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1056 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1057 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1058 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1059 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1060 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1061 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1062 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1063 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1064 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1065 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1066 20UF 20% 4V X5R-CERM 0402-2 | CRITICAL C1067 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1068-C1076:

CAPs for Acoustic control (C102E-C103F)

NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S | CRITICAL C1077 210UF 20% 2.5V POLY-TANT CASE-B2S

C102E 20UF 20% 4V X5R-CERM 0402-2 | C102F 20UF 20% 4V X5R-CERM 0402-2 | C103A 20UF 20% 4V X5R-CERM 0402-2 | C103B 20UF 20% 4V X5R-CERM 0402-2 | C103C 20UF 20% 4V X5R-CERM 0402-2 | C103D 20UF 20% 4V X5R-CERM 0402-2 | C103E 20UF 20% 4V X5R-CERM 0402-2 | C103F 20UF 20% 4V X5R-CERM 0402-2

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

PLACEMENT_NOTE (C1080-C1089):

66 65 21 8 6 81 89 PP1V35_S3RS0_CPUDDR

Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402 | C1081 1UF 10% 10V X6S-CERM 0402 | C1082 1UF 10% 10V X6S-CERM 0402 | C1083 1UF 10% 10V X6S-CERM 0402 | C1084 1UF 10% 10V X6S-CERM 0402 | C1085 1UF 10% 10V X6S-CERM 0402 | C1086 1UF 10% 10V X6S-CERM 0402 | C1087 1UF 10% 10V X6S-CERM 0402 | C1088 1UF 10% 10V X6S-CERM 0402 | C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):

Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603 | C1091 10UF 20% 4V X6S-CERM 0603 | C1092 10UF 20% 4V X6S-CERM 0603 | C1093 10UF 20% 4V X6S-CERM 0603 | C1094 10UF 20% 4V X6S-CERM 0603 | C1095 10UF 20% 4V X6S-CERM 0603 | C1096 10UF 20% 4V X6S-CERM 0603 | C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 6.3V POLY-TANT D15T-ECGLT-COMBO

CRITICAL C1099 330UF-6MOHM 20% 6.3V POLY-TANT D15T-ECGLT-COMBO

(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

58 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 16V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC MASTER=J15 REFERENCE SYNC DATE=12/18/2012

PAGE TITLE: CPU Decoupling

Apple Inc.

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OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
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SYSCLK_CLK32K_RTC	B5	RTCX1	RTC	
NC	B4	RTCX2		
PCH_SRTCRST_L	B9	SRTCRST*		
PCH_INTRUDER_L	A8	INTRUDER*		
PCH_INTVRMEN_L	G10	INTVRMEN		
RTC_RESET_L	D9	RTCRST*		
HDA_BIT_CLK	B25	HDA_BCLK	AZALIA	
HDA_SYNC	A22	HDA_SYNC (IPD-boot)		
PCH_SPKR	AL10	SPKR (IPD-PLTRST#)		
HDA_RST_L	C24	HDA_RST*		
HDA_SDIN0	L22	HDA_SDI0 (IPD)		
NC_HDA_SDIN1	K22	HDA_SDI1 (IPD)		
NC_HDA_SDIN2	G22	HDA_SDI2 (IPD)		
NC_HDA_SDIN3	F22	HDA_SDI3 (IPD)		
HDA_SDOUT	A24	HDA_SDO (IPD-boot)		
DP_TBT_SEL	B17	(IPD-DOCKEN#?) DOCKEN*/GPIO33		
ENET_MEDIA_SENSE_RDIV	C22	HDA_DOCK_RST*/GPIO13		
XDP_PCH_TCK	AB3	JTAG_TCK (IPD)	JTAG	
XDP_PCH_TMS	AD1	JTAG_TMS (IPU)		
XDP_PCH_TDI	AE2	JTAG_TDI (IPU)		
XDP_PCH_TDO	AD3	JTAG_TDO		
NC	F8	TP25		
NC	C26	TP22		
NC	AB6	TP20		

SATA_RXN0	BC8	NC_SATA_A_D2RN	
SATA_RXP0	BE8	NC_SATA_A_D2RP	
SATA_TXN0	AW8	NC_SATA_A_R2D_CN	
SATA_TXP0	AY8	NC_SATA_A_R2D_CP	
SATA_RXN1	BC10	NC_SATA_B_D2RN	
SATA_RXP1	BE10	NC_SATA_B_D2RP	
SATA_TXN1	AV10	NC_SATA_B_R2D_CN	
SATA_TXP1	AW10	NC_SATA_B_R2D_CP	
SATA_RXN2	BB9	NC_SATA_ODD_D2RN	
SATA_RXP2	BD9	NC_SATA_ODD_D2RP	
SATA_TXN2	AY13	NC_SATA_ODD_R2D_CN	
SATA_TXP2	AW13	NC_SATA_ODD_R2D_CP	
SATA_RXN3	BC12	NC_SATA_D_D2RN	
SATA_RXP3	BE12	NC_SATA_D_D2RP	
SATA_TXN3	AR13	NC_SATA_D_R2D_CN	
SATA_TXP3	AT13	NC_SATA_D_R2D_CP	
SATA_RXN4/PERN1	BD13	TP_PCIE_ENET_D2RN	
SATA_RXP4/PERP1	BB13	TP_PCIE_ENET_D2RP	
SATA_TXN4/PETN1	AV15	TP_PCIE_ENET_R2D_CN	
SATA_TXP4/PETP1	AW15	TP_PCIE_ENET_R2D_CP	
SATA_RXN5/PERN2	BC14	NC_SATA_F_D2RN	
SATA_RXP5/PERP2	BE14	NC_SATA_F_D2RP	
SATA_TXN5/PETN2	AP15	NC_SATA_F_R2D_CN	
SATA_TXP5/PETP2	AR15	NC_SATA_F_R2D_CP	
SATA_RCOMP	AY5	PCH_SATA_RCOMP	
SATALED*	AP3	PCH_SATALED_L	
SATA0GP/GPIO21	AT1	XDP_DC0_DP_AUXCH_ISOL_L	
SATA1GP/GPIO19 (IPU-PLTRST#)	AU2	XDP_DC1_SATARDRVR_EN	
SATA_IREF	BD4		
TP9	BA2	NC	
TP8	BB2	NC	

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCIe:
Reserved: Ethernet
(if not combo w/SD Card)

Unused

PP1V5_S0

R1130 7.5K 1% 1/20W MF 201

PLACE_NEAR=U1100.AY5:2.54mm

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
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PCIE_CLK100M_SSD_N	Y43	CLKOUT_PCIE_N0	
PCIE_CLK100M_SSD_P	Y45	CLKOUT_PCIE_P0	
SSD_CLKREQ_L	AB1	PCIECLKRQ0*/GPIO73	
NC_PCIE_CLK100M_ENETSDN	AA44	CLKOUT_PCIE_N1	
NC_PCIE_CLK100M_ENETSDP	AA42	CLKOUT_PCIE_P1	
XDP_DD2_ENETSD_CLKREQ_L	AF1	PCIECLKRQ1*/GPIO18	
PCIE_CLK100M_AP_N	AB43	CLKOUT_PCIE_N2	
PCIE_CLK100M_AP_P	AB45	CLKOUT_PCIE_P2	
XDP_DD3_AP_CLKREQ_L	AF3	PCIECLKRQ2*/GPIO20/SMI*	
PCIE_CLK100M_CAMERA_N	AD43	CLKOUT_PCIE_N3	
PCIE_CLK100M_CAMERA_P	AD45	CLKOUT_PCIE_P3	
CAMERA_CLKREQ_L	T3	PCIECLKRQ3*/GPIO25	
NC_PCIE_CLK100M_GPUN	AF43	CLKOUT_PCIE_N4	
NC_PCIE_CLK100M_GPUP	AF45	CLKOUT_PCIE_P4	
TBT_CLKREQ_L	V3	PCIECLKRQ4*/GPIO26	
NC_PCIE_CLK100M_PE5N	AE44	CLKOUT_PCIE_N5	
NC_PCIE_CLK100M_PE5P	AE42	CLKOUT_PCIE_P5	
PCH_CLKRQ5_L_GPIO44	AA2	PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)	
NC_PCIE_CLK100M_SWN	AB40	CLKOUT_PCIE_N6	
NC_PCIE_CLK100M_SWP	AB39	CLKOUT_PCIE_P6	
PEG_CLKREQ_L	AE4	PCIECLKRQ6*/GPIO45	
PCIE_CLK100M_TBT_N	AJ44	CLKOUT_PCIE_N7	
PCIE_CLK100M_TBT_P	AJ42	CLKOUT_PCIE_P7	
PCH_CLKRQ7_L_GPIO46	Y3	PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)	
NC_ITPXDP_CLK100MN	AH43	CLKOUT_ITPXDP_N	
NC_ITPXDP_CLK100MP	AH45	CLKOUT_ITPXDP_P	
LPC_CLK33M_SMC_R	D44	CLKOUT_33MHZ0 (IPD-PWROK)	
LPC_CLK33M_LPCPLUS_R	E44	CLKOUT_33MHZ1 (IPD-PWROK)	
NC_PCI_CLK33M_OUT2	B42	CLKOUT_33MHZ2 (IPD-PWROK)	
NC_PCI_CLK33M_OUT3	F41	CLKOUT_33MHZ3 (IPD-PWROK)	
PCH_CLK33M_PCIOUT	A40	CLKOUT_33MHZ4 (IPD-PWROK)	

CLKOUT_PEG_A_N	AB35	NC_PCIE_CLK100M_ENETN	
CLKOUT_PEG_A_P	AB36	NC_PCIE_CLK100M_ENETP	
PEG_A_CLKRQ*/GPIO47	AF6	ENET_CLKREQ_L	
CLKOUT_PEG_B_N	Y39	NC_PCIE_CLK100M_PEGBN	
CLKOUT_PEG_B_P	Y38	NC_PCIE_CLK100M_PEGBP	
PEG_B_CLKRQ*/GPIO56	U4	PCH_PEGCLKRQB_L_GPIO56	
CLKOUT_DMI_N	AF39	DMI_CLK100M_CPU_N	
CLKOUT_DMI_P	AF40	DMI_CLK100M_CPU_P	
CLKOUT_DP_N	AJ40	CPU_CLK135M_DPLLSS_N	
CLKOUT_DP_P	AJ39	CPU_CLK135M_DPLLSS_P	
CLKOUT_DPNS_N	AF35	CPU_CLK135M_DPLLREF_N	
CLKOUT_DPNS_P	AF36	CPU_CLK135M_DPLLREF_P	
CLKIN_DMI_N	AY24	PCIE_CLK100M_PCH_N	
CLKIN_DMI_P	AW24	PCIE_CLK100M_PCH_P	
CLKIN_GND_N	AR24	PCH_CLKIN_GNDN	
CLKIN_GND_P	AT24	PCH_CLKIN_GNDP	
CLKIN_DOT96_N	H33	PCH_CLK96M_DOT_N	
CLKIN_DOT96_P	G33	PCH_CLK96M_DOT_P	
CLKIN_SATA_N	BE6	PCH_CLK100M_SATA_N	
CLKIN_SATA_P	BC6	PCH_CLK100M_SATA_P	
REFCLK14IN	F45	PCH_CLK14P3M_REFCLK	
CLKIN_33MHZLOOPBACK	D17	PCH_CLK33M_PCIIN	
XTAL25_IN	AM43	SYSCLK_CLK25M_SB_R	
XTAL25_OUT	AL44	NC	
(IPD-PWROK) CLKOUTFLEX0/GPIO64	C40	NC_PCH_GPIO64_CLKOUTFLEX0	
(IPD-PWROK) CLKOUTFLEX1/GPIO65	F38	NC_PCH_GPIO65_CLKOUTFLEX1	
(IPD-PWROK) CLKOUTFLEX2/GPIO66	F36	NC_PCH_GPIO66_CLKOUTFLEX2	
(IPD-PWROK) CLKOUTFLEX3/GPIO67	F39	NC_PCH_GPIO67_CLKOUTFLEX3	
ICLK_IREF	AM45	PP1V5_S0	
TP19	AD39	NC	
TP18	AD38	NC	
DIFFCLK_BIASREF	AN44	PCH_DIFFCLK_BIASREF	

CLOCKS

Unused clock terminations for FCIM Mode

R1196 10K 5% 1/20W MF 201 — PCIE_CLK100M_PCH_N
R1195 10K 5% 1/20W MF 201 — PCIE_CLK100M_PCH_P
R1171 10K 5% 1/20W MF 201 — PCH_CLKIN_GNDN
R1170 10K 5% 1/20W MF 201 — PCH_CLKIN_GNDP
R1192 10K 5% 1/20W MF 201 — PCH_CLK96M_DOT_N
R1191 10K 5% 1/20W MF 201 — PCH_CLK96M_DOT_P
R1194 10K 5% 1/20W MF 201 — PCH_CLK100M_SATA_N
R1193 10K 5% 1/20W MF 201 — PCH_CLK100M_SATA_P
R1197 10K 5% 1/20W MF 201 — PCH_CLK14P3M_REFCLK

R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB

1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

R1190 7.5K 1% 1/20W MF 201 — PP1V5_S0

PLACE_NEAR=U1100.AN44:2.54mm

NOTE: ENET pair only used if SD Card Reader is USB3.

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

PPVRTC_G3H

R1100 330K 5% 1/20W MF 201
R1101 1M 5% 1/20W MF 201
R1102 20K 5% 1/20W MF 201
R1103 20K 5% 1/20W MF 201

PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L

C1102 1UF 10% 10V X5R 402
C1103 1UF 10% 10V X5R 402

PP3V3_SUS
PP3V3_S0

R1177	4.7K	5% 1/20W MF 201	PCH_SPKR
R1176	10K	5% 1/20W MF 201	DP_TBT_SEL
R1178	4.7K	5% 1/20W MF 201	PCH_SATALED_L
R1134	10K	5% 1/20W MF 201	DP_AUXCH_ISOL_L
R1133	10K	5% 1/20W MF 201	XDP_DC1_SATARDRVR_EN
R1143	10K	5% 1/20W MF 201	SSD_CLKREQ_L
R1142	10K	5% 1/20W MF 201	XDP_DD2_ENETSD_CLKREQ_L
R1169	10K	5% 1/20W MF 201	AP_CLKREQ_L
R1144	10K	5% 1/20W MF 201	CAMERA_CLKREQ_L
R1145	10K	5% 1/20W MF 201	TBT_CLKREQ_L
R1147	10K	5% 1/20W MF 201	PCH_CLKRQ5_L_GPIO44
R1114	10K	5% 1/20W MF 201	PEG_CLKREQ_L
R1115	10K	5% 1/20W MF 201	PCH_CLKRQ7_L_GPIO46
R1146	10K	5% 1/20W MF 201	ENET_CLKREQ_L
R1148	10K	5% 1/20W MF 201	PCH_PEGCLKRQB_L_GPIO56
R1179	10K	5% 1/20W MF 201	ENET_MEDIA_SENSE_RDIV

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK

Apple Inc.

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SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader
(& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD

OMIT_TABLE

U1100
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PCI-E
USB

72	NC_USB3_SPARE_D2RN	AW31	PERN1_USB3RN3
72	NC_USB3_SPARE_D2RP	AY31	PERP1_USB3RP3
72	NC_USB3_SPARE_R2D_CN	BE32	PETN1_USB3TN3
72	NC_USB3_SPARE_R2D_CP	BC32	PETP1_USB3TP3
76 71 68 20 IN	USB3_SD_D2R_N	AT31	PERN2_USB3RN4
76 71 68 20 IN	USB3_SD_D2R_P	AR31	PERP2_USB3RP4
76 71 68 20 OUT	USB3_SD_R2D_C_N	BD33	PETN2_USB3TN4
76 71 68 20 OUT	USB3_SD_R2D_C_P	BB33	PETP2_USB3TP4
76 34 IN	PCIE_AP_D2R_N	AW33	PERN3
76 34 IN	PCIE_AP_D2R_P	AY33	PERP3
76 34 OUT	PCIE_AP_R2D_C_N	BE34	PETN3
76 34 OUT	PCIE_AP_R2D_C_P	BC34	PETP3
76 37 IN	PCIE_CAMERA_D2R_N	AT33	PERN4
76 37 IN	PCIE_CAMERA_D2R_P	AR33	PERP4
76 37 OUT	PCIE_CAMERA_R2D_C_N	BE36	PETN4
76 37 OUT	PCIE_CAMERA_R2D_C_P	BC36	PETP4
76 35 IN	PCIE_SSD_D2R_N<0>	AW36	PERN5
76 35 IN	PCIE_SSD_D2R_P<0>	AV36	PERP5
76 35 OUT	PCIE_SSD_R2D_C_N<0>	BD37	PETN5
76 35 OUT	PCIE_SSD_R2D_C_P<0>	BB37	PETP5
76 35 IN	PCIE_SSD_D2R_N<1>	AY38	PERN6
76 35 IN	PCIE_SSD_D2R_P<1>	AW38	PERP6
76 35 OUT	PCIE_SSD_R2D_C_N<1>	BC38	PETN6
76 35 OUT	PCIE_SSD_R2D_C_P<1>	BB38	PETP6
76 35 IN	PCIE_SSD_D2R_N<2>	AT40	PERN7
76 35 IN	PCIE_SSD_D2R_P<2>	AT39	PERP7
76 35 OUT	PCIE_SSD_R2D_C_N<2>	BE40	PETN7
76 35 OUT	PCIE_SSD_R2D_C_P<2>	BC40	PETP7
76 35 IN	PCIE_SSD_D2R_N<3>	AN38	PERN8
76 35 IN	PCIE_SSD_D2R_P<3>	AN39	PERP8
76 35 OUT	PCIE_SSD_R2D_C_N<3>	BD42	PETN8
76 35 OUT	PCIE_SSD_R2D_C_P<3>	BD41	PETP8

USB2N0	B37	USB_EXTA_N	B1 38 75
USB2P0	D37	USB_EXTA_P	B1 38 75
USB2N1	A38	NC_USB_EXTCN	B1 72 75
USB2P1	C38	NC_USB_EXTCP	B1 72 75
USB2N2	A36	NC_USB_SDN	72 75
USB2P2	C36	NC_USB_SDP	72 75
USB2N3	A34	NC_USB_WLANN	72
USB2P3	C34	NC_USB_WLANP	72
USB2N4	B33	NC_USB_4N	72
USB2P4	D33	NC_USB_4P	72
USB2N5	F31	NC_USB_PSOCN	72
USB2P5	G31	NC_USB_PSOCP	72
USB2N6	K31	NC_USB_6N	72 75
USB2P6	L31	NC_USB_6P	72 75
USB2N7	G29	NC_USB_7N	72 75
USB2P7	H29	NC_USB_7P	72 75
USB2N8	A32	USB_EXTB_N	B1 68 71 75
USB2P8	C32	USB_EXTB_P	B1 68 71 75
USB2N9	A30	NC_USB_EXTDN	B1 72 75
USB2P9	C30	NC_USB_EXTDP	B1 72 75
USB2N10	B29	TP_USB_CAMERAN	
USB2P10	D29	TP_USB_CAMERAP	
USB2N11	A28	USB_BT_N	B1 34 75
USB2P11	C28	USB_BT_P	B1 34 75
USB2N12	G26	NC_USB_IRN	B1 72 75
USB2P12	F26	NC_USB_IRP	B1 72 75
USB2N13	F24	USB_TPAD_N	B1 39 75
USB2P13	G24	USB_TPAD_P	B1 39 75
(IPD)			
USB3RN1	AR26	USB3_EXTA_D2R_N	IN 38 75
USB3RP1	AP26	USB3_EXTA_D2R_P	IN 38 75
USB3TN1	BE24	USB3_EXTA_R2D_C_N	OUT 38 75
USB3TP1	BD23	USB3_EXTA_R2D_C_P	OUT 38 75
USB3RN2	AW26	USB3_EXTB_D2R_N	IN 68 71 75
USB3RP2	AV26	USB3_EXTB_D2R_P	IN 68 71 75
USB3TN2	BD25	USB3_EXTB_R2D_C_N	OUT 68 75
USB3TP2	BC24	USB3_EXTB_R2D_C_P	OUT 68 75
USB3RN5	AW29	NC_USB3_EXTC_D2RN	IN 72 75
USB3RP5	AV29	NC_USB3_EXTC_D2RP	IN 72 75
USB3TN5	BE26	NC_USB3_EXTC_R2D_GN	OUT 72 75
USB3TP5	BC26	NC_USB3_EXTC_R2D_GP	OUT 72 75
USB3RN6	AR29	NC_USB3_EXTD_D2RN	IN 72 75
USB3RP6	AP29	NC_USB3_EXTD_D2RP	IN 72 75
USB3TN6	BD27	NC_USB3_EXTD_R2D_GN	OUT 72 75
USB3TP6	BE28	NC_USB3_EXTD_R2D_GP	OUT 72 75
USBRBIAS*	K24	PCH_USB_RBIAS	75
USBRBIAS	K26		
TP24	M33	NC	
TP23	L33	NC	
OC0*/GPIO59	P3	XDP_DA0_USB_EXTA_OC_L	IN 13 18
OC1*/GPIO40	V1	XDP_DA1_USB_EXTC_OC_L	IN 13 18
OC2*/GPIO41	U2	XDP_DA2_SSD_PWR_EN	OUT 18
OC3*/GPIO42	P1	XDP_DA3_CAMERA_PWR_EN	OUT 18
OC4*/GPIO43	M3	XDP_DB0_USB_EXTB_OC_L	IN 13 18
OC5*/GPIO9	T1	XDP_DB1_USB_EXTD_OC_L	IN 13 18
OC6*/GPIO10	N2	XDP_DB2_SD_PWR_EN	OUT 18
OC7*/GPIO14	M1	XDP_DB3_SDCONN_STATE_CHANGE_L	IN 13 18

PLACE_NEAR=U1100.K24:11.4mm
R1370 22.6 1% 1/20W MF 201

69 68 66 64 52 19 17 15 12 11 11 PP1V5_S0

R1300 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.BD29:12.7mm

BE30	PCIE_IREF	
NC BC30	TP11	
NC BB29	TP6	
BD29	PCIE_RCOMP	PCH_PCIE_RCOMP

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(3 OF 11)

LPC
SMBUS
C-LINK
SPI

76 71 50 41 BI	LPC_AD<0>	R1340 33 1% 1/20W MF 201	LPC_AD_R<0>
76 71 50 41 BI	LPC_AD<1>	R1341 33 1% 1/20W MF 201	LPC_AD_R<1>
76 71 50 41 BI	LPC_AD<2>	R1342 33 1% 1/20W MF 201	LPC_AD_R<2>
76 71 50 41 BI	LPC_AD<3>	R1343 33 1% 1/20W MF 201	LPC_AD_R<3>
76 71 50 41 OUT	LPC_FRAME_L	R1344 33 1% 1/20W MF 201	LPC_FRAME_R_L

A20	LAD0 (IPU)		LPC_AD_R<0>
C20	LAD1 (IPU)		LPC_AD_R<1>
A18	LAD2 (IPU)		LPC_AD_R<2>
C18	LAD3 (IPU)		LPC_AD_R<3>
B21	LFRAME*		LPC_FRAME_R_L
D21	LDRQ0* (IPU)	72	NC_LPC_DREQ0_L
G20	LDRQ1*/GPIO23 (IPU-LDRQ1#7)	20 13 OUT	TBT_PWR_EN_PCH
AL11	SERIRQ	71 50 41 13 BI	LPC_SERIRQ
N7	SMBALERT*/GPIO11		PCH_SMBALERT_L 13
R10	SMBCLK	OUT	SMBUS_PCH_CLK 18 22 44 63 68 71 76
U11	SMBDATA	BI	SMBUS_PCH_DATA 18 22 44 63 68 71 76
N8	SML0ALERT*/GPIO60		PCH_SML0ALERT_L 13
U8	SML0CLK	OUT	SML_PCH_0_CLK 44 76
R7	SML0DATA	BI	SML_PCH_0_DATA 44 76
H6	SML1ALERT*/PCHHOT*/GPIO74		PCH_SML1ALERT_L 13
K6	SML1CLK/GPIO58	IN	SML_PCH_1_CLK 44 76
N11	SML1DATA/GPIO75	BI	SML_PCH_1_DATA 44 76
AJ11	SPI_CLK	76 50 OUT	SPI_CLK_R
AJ7	SPI_CS0* (IPU)	76 50 OUT	SPI_CS0_R_L
AL7	SPI_CS1* (IPU)		TP_SPI_CS1_L
AJ10	SPI_CS2* (IPU)		TP_SPI_CS2_L
AH1	SPI_MOSI (IPD)	76 50 BI	SPI_MOSI_R
AH3	SPI_MISO (IPU)	76 50 BI	SPI_MISO
AJ4	SPI_IO2 (IPU)	50 13 BI	SPI_IO<2>
AJ2	SPI_IO3 (IPU)	50 13 BI	SPI_IO<3>
AF11	(IPU/IPD) CL_CLK		NC_CLINK_CLK 72
AF10	(IPU/IPD) CL_DATA		NC_CLINK_DATA 72
AF7	CL_RST*		NC_CLINK_RESET_L 72
BA45	TP1	NC	
BC45	TP2	NC	
BE43	TP4	NC	
BE44	TP3	NC	
AY43	TD_IREF		PCH_TD_IREF

R1380 8.2K 1% 1/20W MF 201

PP3V3_SUS 11 12 13 14 15 17 50 64 65 66
PP3V3_SUS 11 12 13 14 15 17 50 64 65 66
PP3V3_S3 20 21 22 44 46 47 65 68 69 71
PP3V3_S3RS0_CAMERA 36 47 69
PP3V3_S0 11 12 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55 65

R1350	10K	LPC_SERIRQ	13 41 50 71
R1351	10K	TBT_PWR_EN_PCH	13 20
R1360	10K	XDP_DA0_USB_EXTA_OC_L	13 18
R1361	10K	XDP_DA1_USB_EXTC_OC_L	13 18
R1362	10K	SD_PWR_EN	18 65
R1368	10K	CAMERA_PWR_EN	18 36
R1320	10K	XDP_DB0_USB_EXTB_OC_L	13 18
R1321	10K	XDP_DB1_USB_EXTD_OC_L	13 18
R1367	10K	SD_PWR_EN	18 68 71
R1369	10K	XDP_DB3_SDCONN_STATE_CHANGE_L	13 18
R1392	1K	SPI_IO<2>	13 50
R1393	1K	SPI_IO<3>	13 50
R1353	10K	PCH_SMBALERT_L	13
R1354	10K	PCH_SML0ALERT_L	13
R1355	10K	PCH_SML1ALERT_L	13

All: 5% 1/20W MF 201

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Reserved: SD (HS)

Reserved: WiFi (HS)

Unused

Reserved: PSOC (Legacy Trackpad)

Unused

Unused

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

Reserved: Camera

BT

IR

Trackpad

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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PCH PCI-E/USB

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE FCBGA
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TBT_CIO_PLUG_EVENT_L	AT8	BMBUSY*/GPIO0	
FW_PME_L	F13	TACH1/GPIO1	
DPMUX_UC_IRQ	A14	TACH2/GPIO6	
SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7	
XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)	
WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12	
MEM_VDD_SEL_1V5_L	AB11	GPIO15	
XDP_DD0_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-Boot/SATA4GP?)	
LPCPLUS_GPIO	C14	TACH0/GPIO17	
JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22	
TBT_GO2SX_BIDIR	Y10	GPIO24	
SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)	
ISOLATE_CPU_MEM_L	AD11	GPIO28	
TBT_POC_RESET_L	AN6	GPIO34	
XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*	
XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)	
XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)	
JTAG_ISP_TDO	AT7	SLOAD/GPIO38	
JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39	
FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48	
XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPU-Boot/SATA5GP?)	
SPIROM_USE_MLB	U12	GPIO57	
MLB_RAMCFG3	C16	TACH4/GPIO68	
MLB_RAMCFG2	D13	TACH5/GPIO69	
SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-Boot?)	
MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-Boot?)	
	BE41		
	BE5		
VSS	C45		
	A5		

CPU/MISC

PCH_A20GATE	AN10	TP14	
PCH_PECI	AY1	(IPD) PECI	
PCH_RCIN_L	AT6	RCIN*	
PCH_PROCPWRGD	AV3	PROCPWRGD	
PM_THRMTRIP_L_R	AV1	THRMTRIP*	
CPU_RESET_L	AU4	PLTRST_PROC*	
	N10	VSS	
	A2		
	A41		
	A43		
	A44		
	B1		
	B2		
	B44		
	B45		
	BA1		
	BC1		
	BD1		
	BD2		
	BD44	VSS	
	BD45		
	BE2		
	BE3		
	D1		
	E1		
	E45		
	A4		

GPIO

PP1V05_S0
NO STUFF
R1457 1K 5% 1/16W MF-LF 402

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L

PP3V3_S0
R1475 10K 5% 1/20W MF 201 — RAMCFG0:H
R1474 10K 5% 1/20W MF 201 — RAMCFG1:H
R1473 10K 5% 1/20W MF 201 — RAMCFG2:H
R1472 10K 5% 1/20W MF 201 — RAMCFG3:H

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	FW_PME_L	14 70
R1411	20K	DPMUX_UC_IRQ	14 70
R1496	10K	SMC_RUNTIME_SCI_L	14 41
R1494	10K	WOL_EN	14 70
R1489	10K	MEM_VDD_SEL_1V5_L	14 70
R1495	100K	XDP_DD0_SSD_PCIE_SEL_L	14 18
R1490	100K	LPCPLUS_GPIO	14 50 71
R1412	10K	JTAG_TBT_TMS_PCH	14 20
R1492	10K	TBT_GO2SX_BIDIR	14 70
R1491	10K	SMC_WAKE_SCI_L	14 41
R1498	10K	XDP_DC2_ODD_PWR_EN_L	14 18
R1413	10K	JTAG_ISP_TCK	18 20
R1486	10K	JTAG_ISP_TDO	14 20
R1499	10K	JTAG_ISP_TDI	14 20
R1484	10K	FW_PWR_EN_PCH	14 70
R1493	100K	SPIROM_USE_MLB	14 50 71

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	PCH_A20GATE	14
R1455	10K	PCH_RCIN_L	14 76

All: 5% 1/20W MF 201

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
PAGE TITLE: PCH GPIO/MISC/NCTF
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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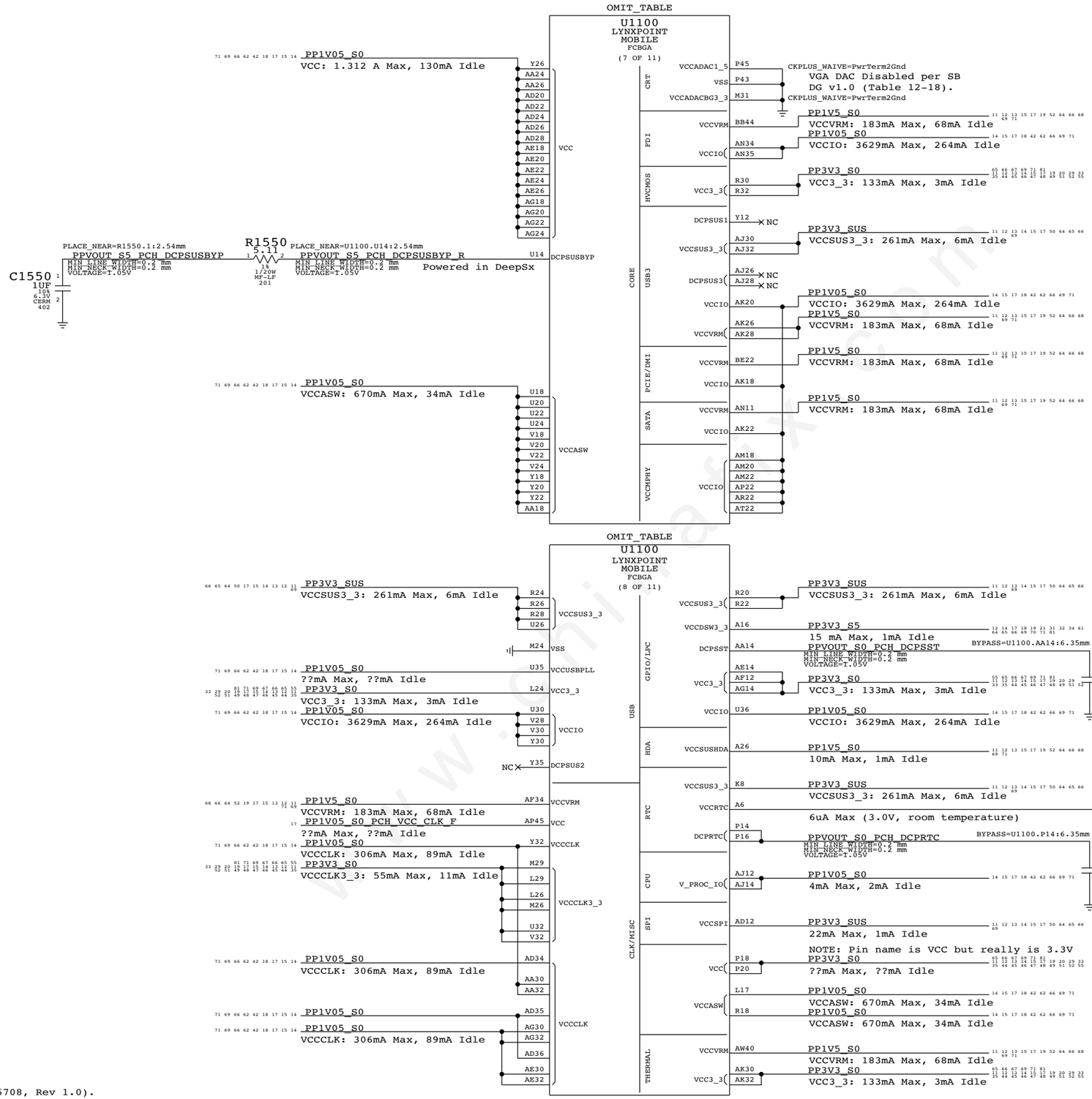

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15 REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Power

Apple Inc.

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BRANCH <BRANCH>

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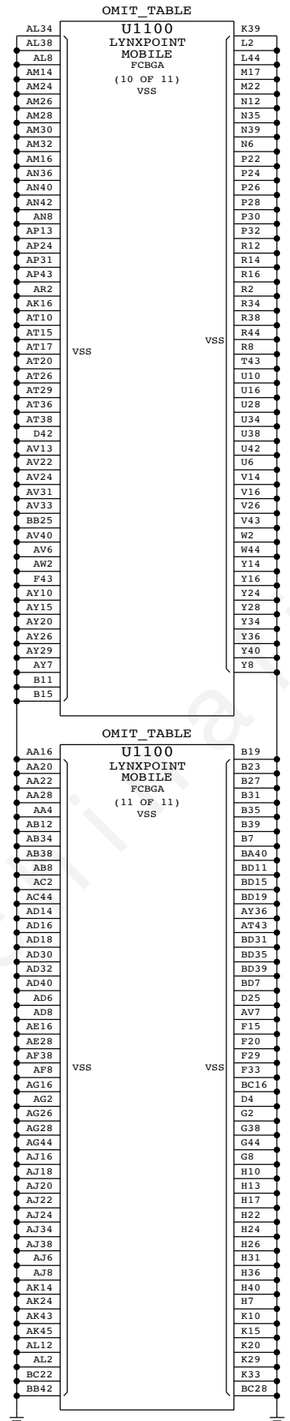

SYNC MASTER=J15 REFERENCE SYNC DATE=12/18/2012

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.A16:6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD12:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.R20:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS
C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.R26:6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.K8:6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0
C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.L26:6.35mm
BYPASS=U1100.L29:6.35mm
BYPASS=U1100.M29:6.35mm
BYPASS=U1100.U32:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0
C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.R30:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0
C1730 0.1UF 20% 10V CERM 402
BYPASS=U1100.L24:6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK30:6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0
C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.P18:6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle
C1750 22UF 20% 6.3V X5R-CERM 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1755 10UF 20% 6.3V X5R 603
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.AG18:12.7mm
BYPASS=U1100.AA24:8.35mm
BYPASS=U1100.AD20:6.35mm
BYPASS=U1100.AE18:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0
C1760 10UF 20% 6.3V X5R 603
C1761 1UF 10% 6.3V CERM 402
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.AK18:12.7mm
BYPASS=U1100.AK18:8.35mm
BYPASS=U1100.AK22:6.35mm
BYPASS=U1100.AK20:6.35mm
BYPASS=U1100.AM18:6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0
C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.U35:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0
C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.AN34:6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1774 0.1UF 20% 10V CERM 402
BYPASS=U1100.U30:6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0
C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.AJ12:12.7mm
BYPASS=U1100.AJ12:6.35mm
BYPASS=U1100.AJ12:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0
C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AE30:6.35mm
BYPASS=U1100.AG30:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0
C1778 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD35:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0
C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.AD34:6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0
C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA30:6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0
C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.A26:6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
C1740 10UF 20% 6.3V X5R 603
BYPASS=U1100.AF34:12.7mm

PP1V05_S0
??mA Max, ??mA Idle
R1790 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT TABLE
L1790 4.7UH-170MA-0.321OHM 0603

PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V

NO STUFF
C1790 10UF 20% 6.3V X5R 603
C1791 1UF 10% 10V X5R 402
BYPASS=U1100.AP45:12.7mm
BYPASS=U1100.AP45:6.35mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402 → XDP

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

CPU_CFG<17> → XDP_CPU_PRESENT_L

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.F50:2.54mm)
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.J3:2.54mm)
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402

XDP_PRESENT# → R1831 1K 5% 1/16W MF-LF 402

C1804 0.1UF 10% 6.3V CERM-X5R 0201
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

XDP_CPU_TDO → R1820 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.H49:28mm) → PP1V05_S0
XDP_CPU_TCK → R1823 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.N54:28mm) → XDP
XDP_CPUPCH_TRST_L → R1824 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.M53:28mm) → XDP

TDI and TMS are terminated in CPU.

R1805 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.AG7:2.54mm)
PLT_RESET_L → XDP

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL
Q1840 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.51:28mm) → XDP_CPU_TDO

CRITICAL
Q1840 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.53:28mm) → XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)

CRITICAL
Q1842 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.55:28mm) → XDP_CPU_TDI

CRITICAL
Q1842 DMN5L06VK-7 SOT-563 (PLACE_NEAR=J1800.57:28mm) → XDP_CPU_TMS

PCH/XDP Signals

OMIT (All 10 R's)

XDP_DA0_USB_EXTA_OC_L	R1890	SHORT		USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT		SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT		CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT		USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT		SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT		SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT		DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN		MAKE_BASE=TRUE		XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L		MAKE_BASE=TRUE		XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT		JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT		SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1		MAKE_BASE=TRUE		XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L		MAKE_BASE=TRUE		XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879	SHORT		AP_CLKREQ_L

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

(TP-P6)

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
ALL_SYS_PWRGD
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC)
R1845 330K 5% 1/20W MF 201
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

XDP_PCH_TDO → R1860 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AD3:28mm)
XDP_PCH_TDI → R1861 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AE2:28mm)
XDP_PCH_TMS → R1862 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AD1:28mm)
XDP_PCH_TCK → R1866 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AB3:28mm)

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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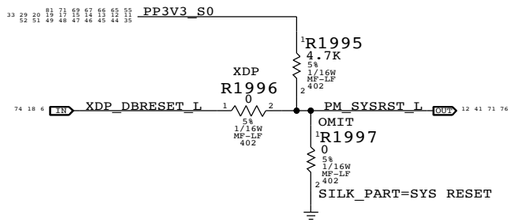
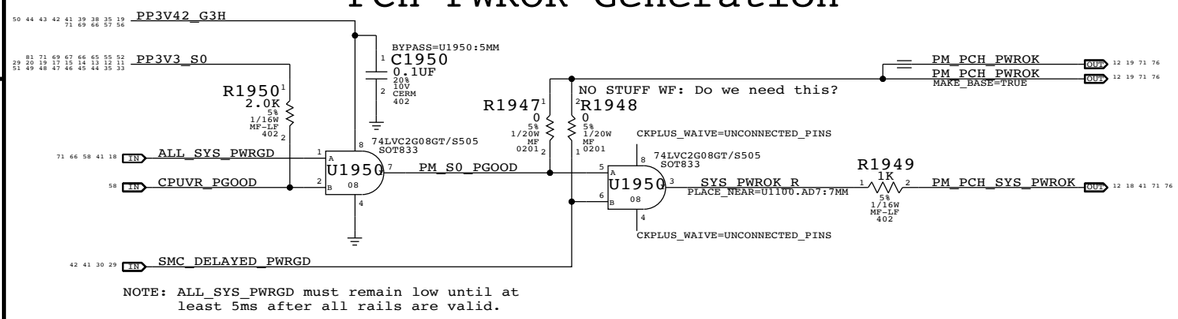
PCH Reset Button

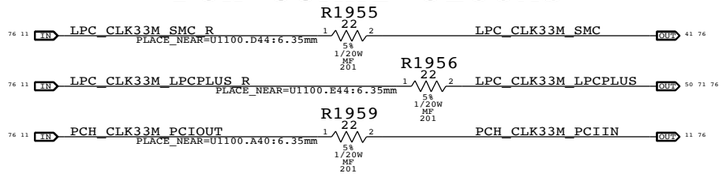


PCH PWROK Generation



NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

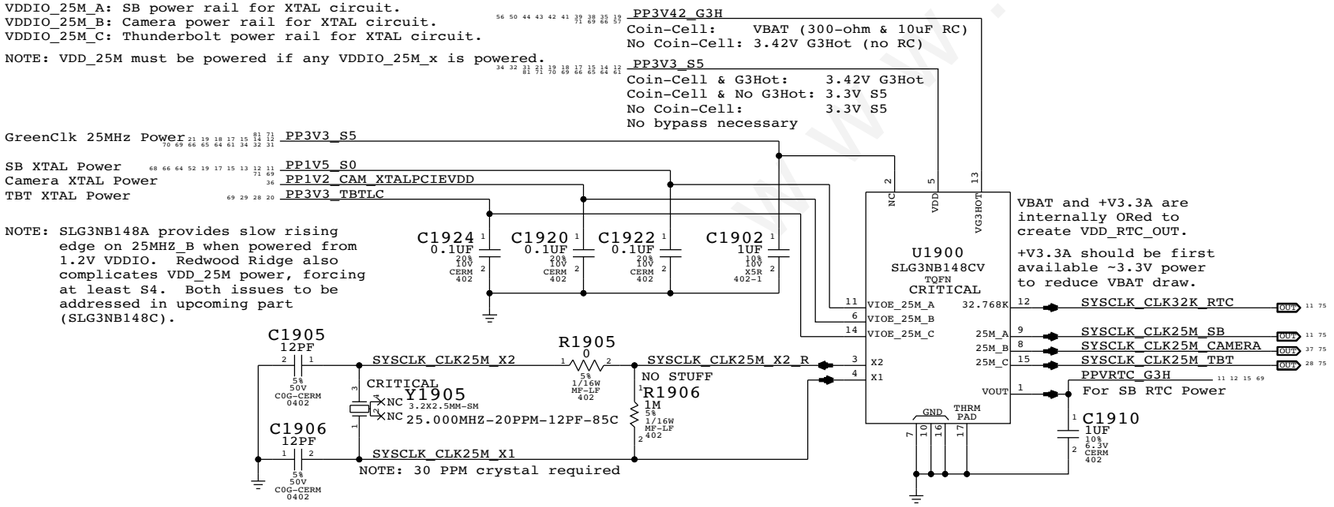
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

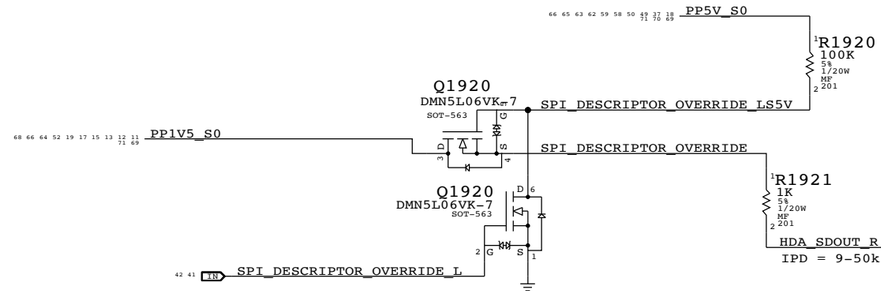


NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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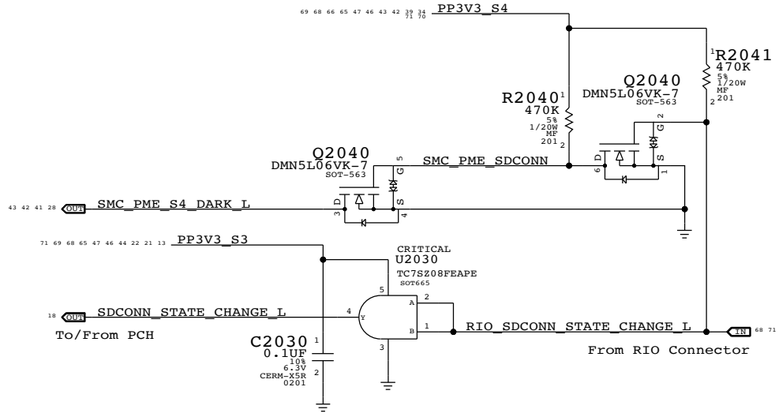
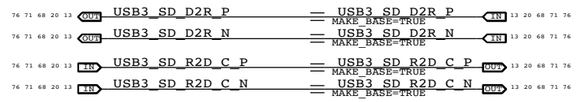
RIO SD Card Reader Support



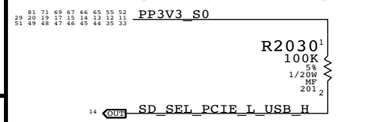
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



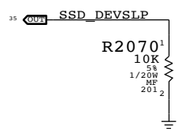
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe



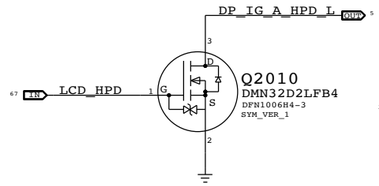
GS3 Connector Support

DEVSLP not supported on LPT-H

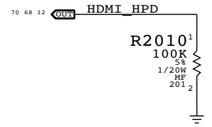


LCD HPD Inverter

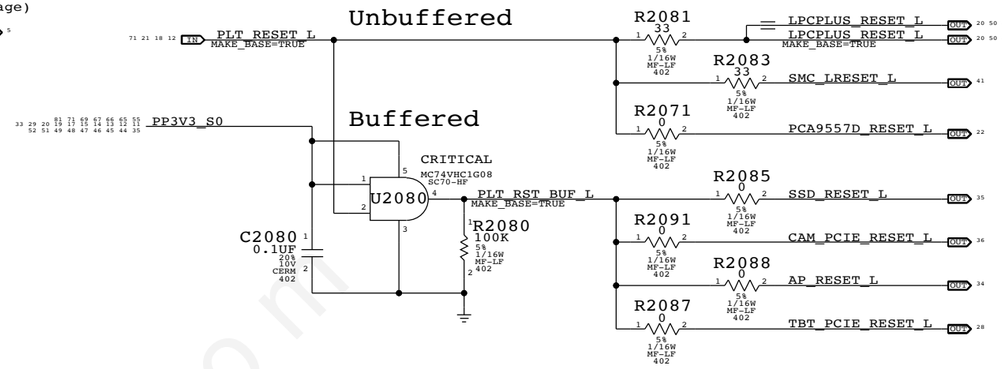
(Pull-Up on CPU Page)



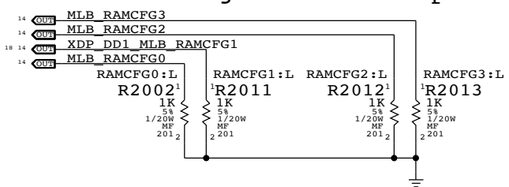
HDMI HPD pull-down



Platform Reset Connections

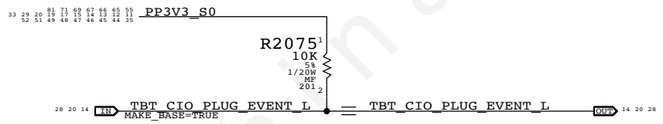


RAM Configuration Straps



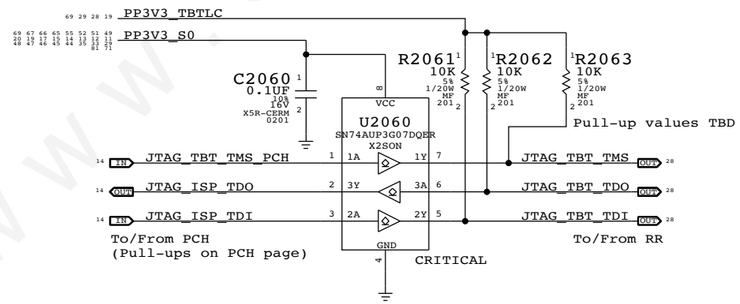
Redwood Ridge Support

RR output is open-drain, no isolation necessary

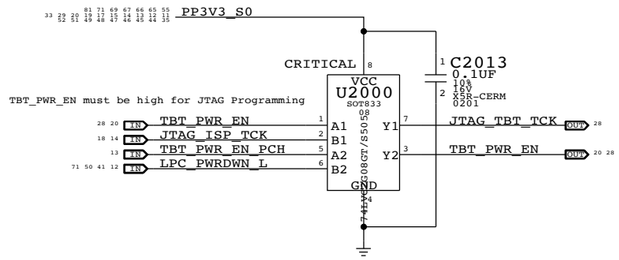


Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



GPIO Glitch Prevention



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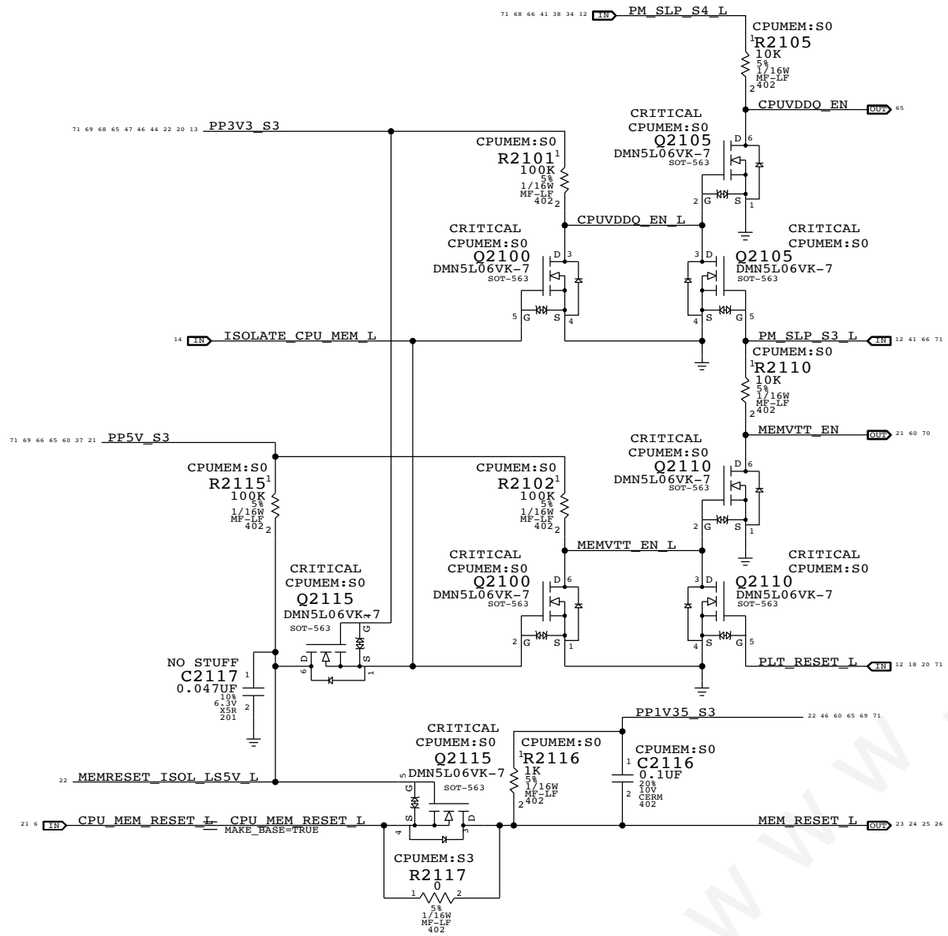
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

```
CPUVDDQ_EN   = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN    = (ISOLATE_CPU_MEM_L + PLT_RST_L)   * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
```



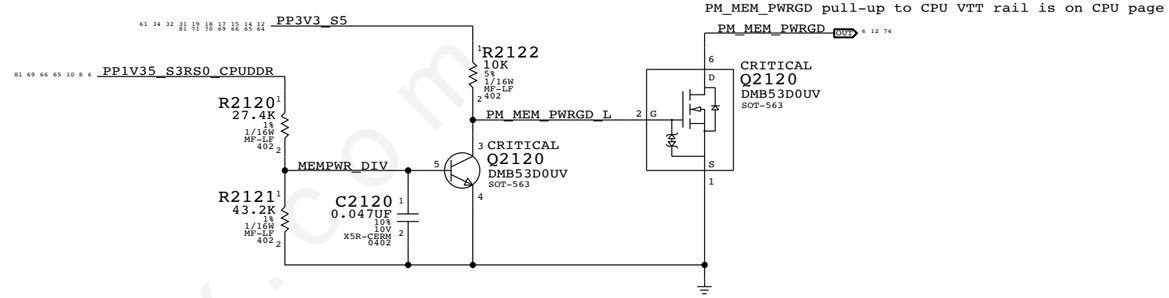
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

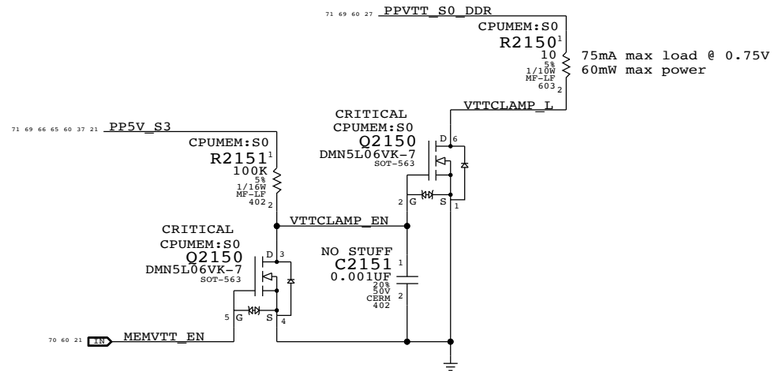
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3

MEMRESET_ISOL_LS5V_L
CPU_DIMMA_VREFDQ
CPU_DIMMB_VREFDQ
CPU_DIMM_VREFCA

CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563
CRITICAL Q2220 DMN5L06VK-7 SOT-563
CRITICAL Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

EN RC's to avoid drain glitches

CPU_MEM_VREFDQ_A_ISOL
DDRVREF_DAC R2225 100K 1% 1/16W MF-LF 402
VREFMRGN_DQ_A_EN_RC
DDRVREF_DAC R2201 100K 5% 1/20W MF 201
DDRVREF_DAC C2225 0.1UF 10% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563
Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

CPU_MEM_VREFDQ_B_ISOL
DDRVREF_DAC R2245 100K 1% 1/16W MF-LF 402
VREFMRGN_DQ_B_EN_RC
DDRVREF_DAC R2202 100K 5% 1/20W MF 201
DDRVREF_DAC C2245 0.1UF 10% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563
Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

CPU_MEM_VREFCA_A_ISOL
DDRVREF_DAC R2265 100K 1% 1/16W MF-LF 402
VREFMRGN_CA_A_EN_RC
DDRVREF_DAC R2207 100K 5% 1/20W MF 201
DDRVREF_DAC C2265 0.1UF 10% 10V CERM 402
CRITICAL DDRVREF_DAC Q2225 DMN5L06VK-7 SOT-563

CPU_MEM_VREFCA_B_ISOL
DDRVREF_DAC R2285 100K 1% 1/16W MF-LF 402
VREFMRGN_CA_B_EN_RC
DDRVREF_DAC R2208 100K 5% 1/20W MF 201
DDRVREF_DAC C2285 0.1UF 10% 10V CERM 402
CRITICAL DDRVREF_DAC Q2265 DMN5L06VK-7 SOT-563

(All 4 R's) DDRVREF_DAC
R2226 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_A_RDIV
R2246 332 1% 1/16W MF-LF 402 VREFMRGN_DQ_B_RDIV
R2266 332 1% 1/16W MF-LF 402 VREFMRGN_CA_A_RDIV
R2286 332 1% 1/16W MF-LF 402 VREFMRGN_CA_B_RDIV

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

PP1V35_S3

MEM_VREFDQ_A_RC: R2223 2 5% 1/20W MF 201; C2220 0.022UF 10% 6.3V X5R-CERM 0201; R2221 1K 1% 1/16W MF-LF 402; R2222 1K 1% 1/16W MF-LF 402; R2220 24.9 1% 1/20W MF 201
PP0V75_S3_MEM_VREFDQ_A
MEM_VREFDQ_B_RC: R2243 2 5% 1/20W MF 201; C2240 0.022UF 10% 6.3V X5R-CERM 0201; R2241 1K 1% 1/16W MF-LF 402; R2242 1K 1% 1/16W MF-LF 402; R2240 24.9 1% 1/20W MF 201
PP0V75_S3_MEM_VREFDQ_B
MEM_VREFCA_A_RC: R2263 2 5% 1/20W MF 201; C2260 0.022UF 10% 6.3V X5R-CERM 0201; R2261 1K 1% 1/16W MF-LF 402; R2262 1K 1% 1/16W MF-LF 402; R2260 24.9 1% 1/20W MF 201
PP0V75_S3_MEM_VREFCA_A
MEM_VREFCA_B_RC: R2283 2 5% 1/20W MF 201; C2280 0.022UF 10% 6.3V X5R-CERM 0201; R2281 1K 1% 1/16W MF-LF 402; R2282 1K 1% 1/16W MF-LF 402; R2280 24.9 1% 1/20W MF 201
PP0V75_S3_MEM_VREFCA_B

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

PP3V3_S3
OMIT R2218 SHORT NONE NONE NONE 402
PP3V3_S3_VREFMRGN
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF
DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2200 DAC55774 MSOP
VDD
SMBUS_PCH_CLK
SMBUS_PCH_DATA
Addr=0x98(WR)/0x99(RD)
SCL SDA A0 A1 GND
VOUTA VREFMRGN_DQ_A
VOUTB VREFMRGN_DQ_B
VOUTC VREFMRGN_CA_AB
VOUTD VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC
U2201 PCA9557 QFN
VCC
Addr=0x30(WR)/0x31(RD)
A0 A1 A2
SMBUS_PCH_CLK
SMBUS_PCH_DATA
SCL SDA
(OD) P0 NC
P1 VREFMRGN_DQ_A_EN
P2 VREFMRGN_DQ_B_EN
P3 VREFMRGN_CA_A_EN
P4 VREFMRGN_CA_B_EN
P5 VREFMRGN_MEMVREG_EN
P6 VREFMRGN_FRAMEBUF_EN
P7 NC
THRM PAD GND
RESET*
PCA9557D_RESET_L

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PP3V3_S3
DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF
DDRVREF_DAC R2214 33.2K 1% 1/16W MF-LF 402
DDRREG_FB

DDRVREF_DAC R2213 100K 5% 1/20W MF 201
CRITICAL DDRVREF_DAC
U2204 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
DDRVREF_DAC R2217 1M 5% 1/16W MF-LF 402

Pins B1 & B4:
CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2215 100K 5% 1/20W MF 201

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

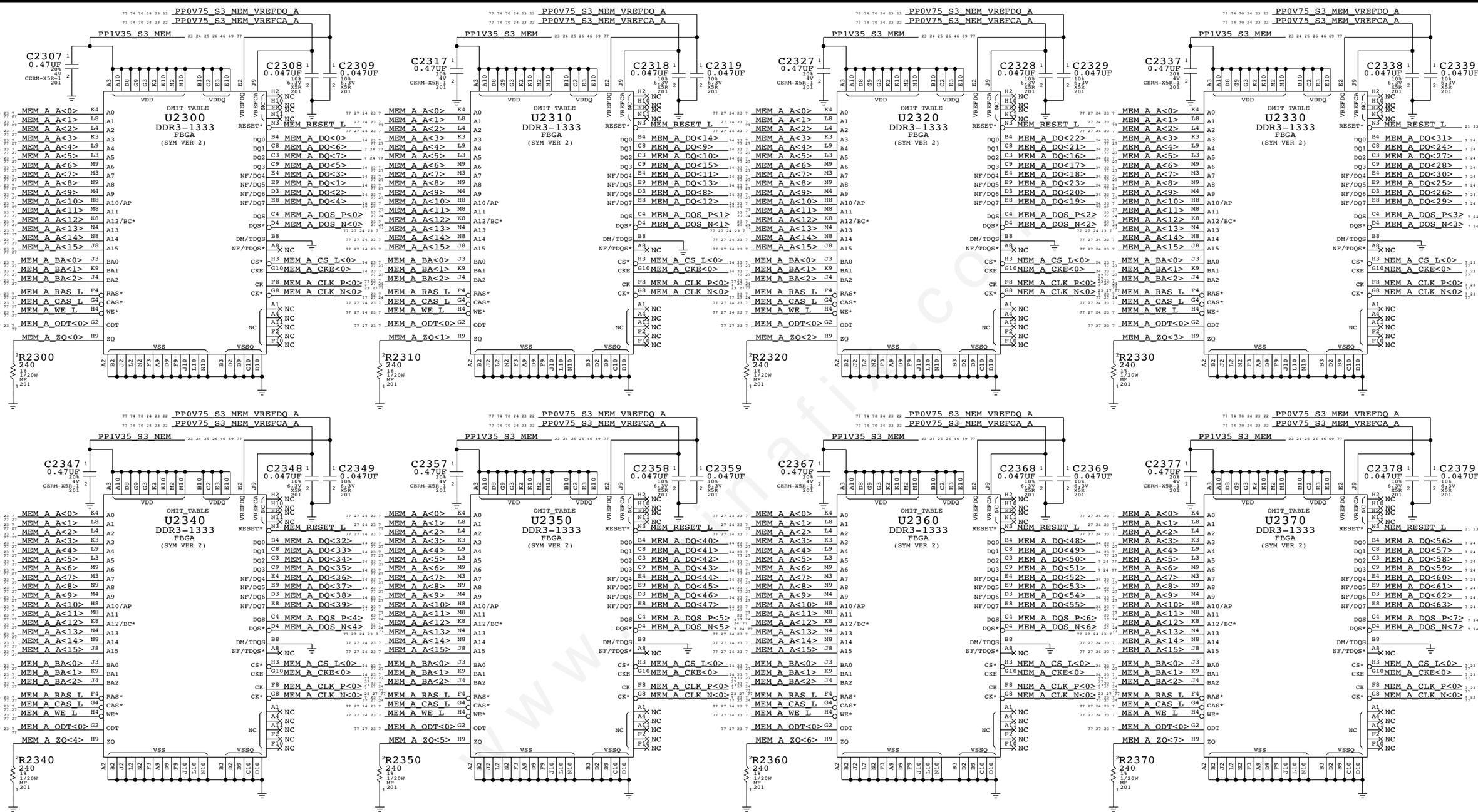
NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 22 OF 118
SHEET: 22 OF 81



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 23 OF 118
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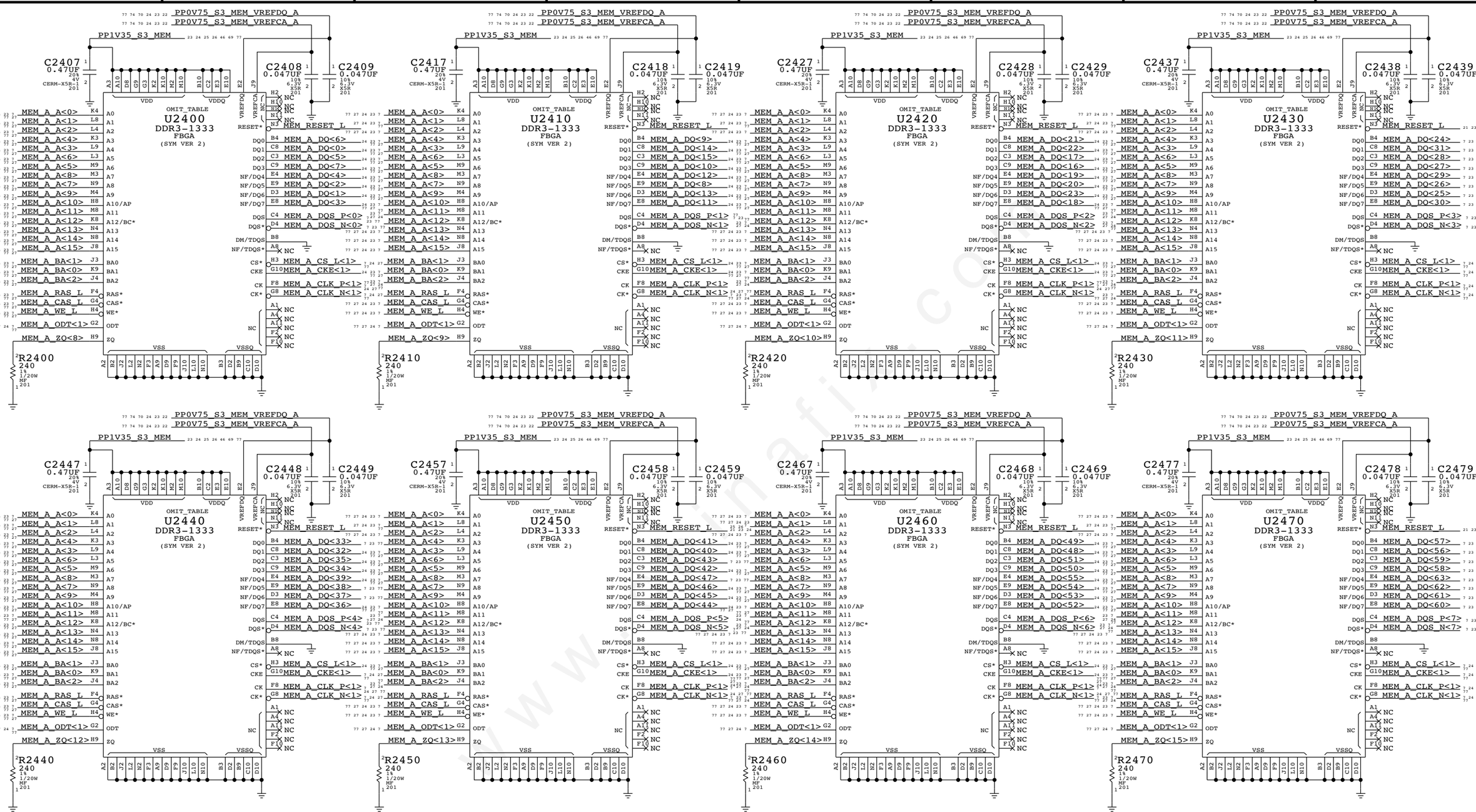

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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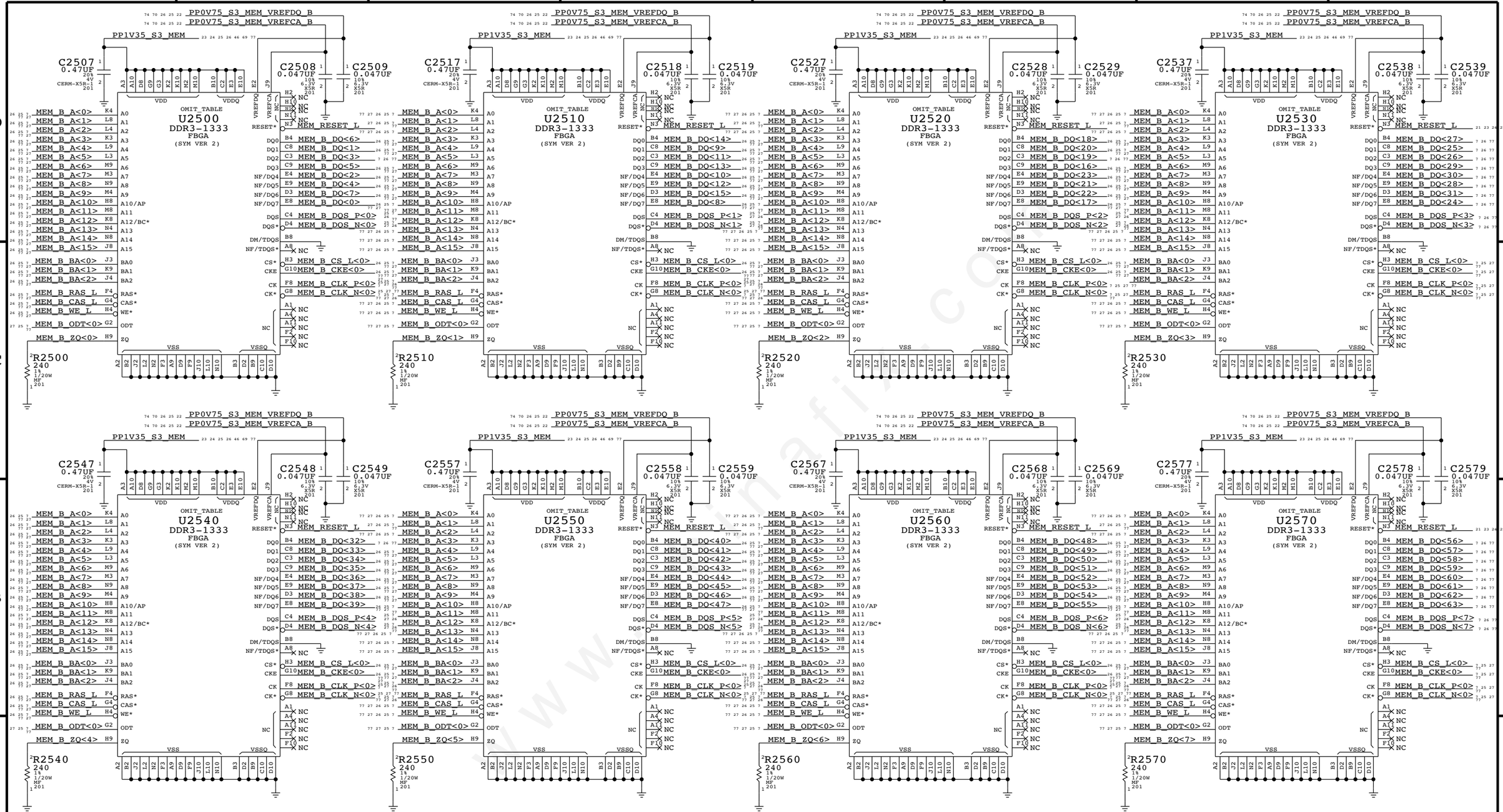

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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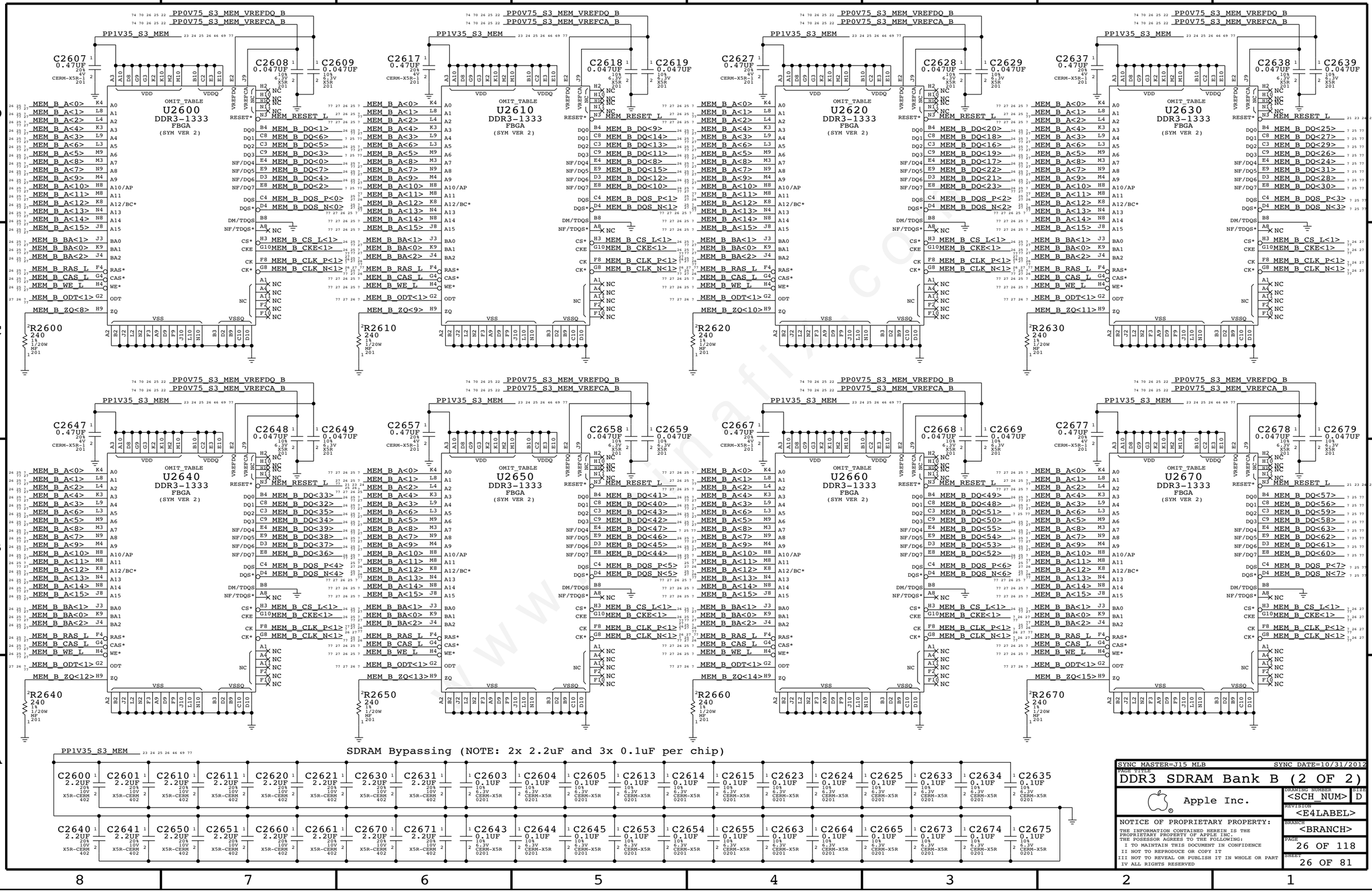
PP0V75_S3_MEM_VREFDQ_B
PP0V75_S3_MEM_VREFCA_B
PP1V35_S3_MEM
C2607 0.47UF 20% 4V CERM-X5R-1 201
C2608 0.047UF 10% 6.3V X5R 201
C2609 0.047UF 10% 6.3V X5R 201
OMIT_TABLE
U2600
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_A<0>
MEM_B_A<1>
MEM_B_A<2>
MEM_B_A<4>
MEM_B_A<3>
MEM_B_A<6>
MEM_B_A<5>
MEM_B_A<8>
MEM_B_A<7>
MEM_B_A<9>
MEM_B_A<10>
MEM_B_A<11>
MEM_B_A<12>
MEM_B_A<13>
MEM_B_A<14>
MEM_B_A<15>
MEM_B_BA<1>
MEM_B_BA<0>
MEM_B_BA<2>
MEM_B_RAS_L
MEM_B_CAS_L
MEM_B_WE_L
MEM_B_ODT<1>
MEM_B_ZQ<8>
MEM_RESET_L
MEM_B_DQ<1>
MEM_B_DQ<6>
MEM_B_DQ<5>
MEM_B_DQ<3>
MEM_B_DQ<0>
MEM_B_DQ<7>
MEM_B_DQ<4>
MEM_B_DQ<2>
MEM_B_DQS_P<0>
MEM_B_DQS_N<0>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
R2600 240 1% 1/20W MF 201
C2617 0.47UF 20% 4V CERM-X5R-1 201
C2618 0.047UF 10% 6.3V X5R 201
C2619 0.047UF 10% 6.3V X5R 201
U2610
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<9>
MEM_B_DQ<14>
MEM_B_DQ<13>
MEM_B_DQ<11>
MEM_B_DQ<8>
MEM_B_DQ<15>
MEM_B_DQ<12>
MEM_B_DQ<10>
MEM_B_DQS_P<1>
MEM_B_DQS_N<1>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<9>
R2610 240 1% 1/20W MF 201
C2627 0.47UF 20% 4V CERM-X5R-1 201
C2628 0.047UF 10% 6.3V X5R 201
C2629 0.047UF 10% 6.3V X5R 201
U2620
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<20>
MEM_B_DQ<18>
MEM_B_DQ<16>
MEM_B_DQ<19>
MEM_B_DQ<17>
MEM_B_DQ<22>
MEM_B_DQ<21>
MEM_B_DQ<23>
MEM_B_DQS_P<2>
MEM_B_DQS_N<2>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<10>
R2620 240 1% 1/20W MF 201
C2637 0.47UF 20% 4V CERM-X5R-1 201
C2638 0.047UF 10% 6.3V X5R 201
C2639 0.047UF 10% 6.3V X5R 201
U2630
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<25>
MEM_B_DQ<27>
MEM_B_DQ<29>
MEM_B_DQ<26>
MEM_B_DQ<24>
MEM_B_DQ<31>
MEM_B_DQ<28>
MEM_B_DQ<30>
MEM_B_DQS_P<3>
MEM_B_DQS_N<3>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<11>
R2630 240 1% 1/20W MF 201
C2647 0.47UF 20% 4V CERM-X5R-1 201
C2648 0.047UF 10% 6.3V X5R 201
C2649 0.047UF 10% 6.3V X5R 201
U2640
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<33>
MEM_B_DQ<32>
MEM_B_DQ<35>
MEM_B_DQ<34>
MEM_B_DQ<39>
MEM_B_DQ<38>
MEM_B_DQ<37>
MEM_B_DQ<36>
MEM_B_DQS_P<4>
MEM_B_DQS_N<4>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<12>
R2640 240 1% 1/20W MF 201
C2657 0.47UF 20% 4V CERM-X5R-1 201
C2658 0.047UF 10% 6.3V X5R 201
C2659 0.047UF 10% 6.3V X5R 201
U2650
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<41>
MEM_B_DQ<40>
MEM_B_DQ<43>
MEM_B_DQ<42>
MEM_B_DQ<47>
MEM_B_DQ<46>
MEM_B_DQ<45>
MEM_B_DQ<44>
MEM_B_DQS_P<5>
MEM_B_DQS_N<5>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<13>
R2650 240 1% 1/20W MF 201
C2667 0.47UF 20% 4V CERM-X5R-1 201
C2668 0.047UF 10% 6.3V X5R 201
C2669 0.047UF 10% 6.3V X5R 201
U2660
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<49>
MEM_B_DQ<48>
MEM_B_DQ<51>
MEM_B_DQ<50>
MEM_B_DQ<54>
MEM_B_DQ<53>
MEM_B_DQ<52>
MEM_B_DQS_P<6>
MEM_B_DQS_N<6>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<14>
R2660 240 1% 1/20W MF 201
C2677 0.47UF 20% 4V CERM-X5R-1 201
C2678 0.047UF 10% 6.3V X5R 201
C2679 0.047UF 10% 6.3V X5R 201
U2670
DDR3-1333
FBGA
(SYM VER 2)
MEM_B_DQ<57>
MEM_B_DQ<56>
MEM_B_DQ<59>
MEM_B_DQ<58>
MEM_B_DQ<63>
MEM_B_DQ<62>
MEM_B_DQ<61>
MEM_B_DQ<60>
MEM_B_DQS_P<7>
MEM_B_DQS_N<7>
MEM_B_CS_L<1>
MEM_B_CKE<1>
MEM_B_CLK_P<1>
MEM_B_CLK_N<1>
MEM_B_ODT<1>
MEM_B_ZQ<15>
R2670 240 1% 1/20W MF 201
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)
C2600 2.2UF 20% 10V X5R-CERM 402
C2601 2.2UF 20% 10V X5R-CERM 402
C2610 2.2UF 20% 10V X5R-CERM 402
C2611 2.2UF 20% 10V X5R-CERM 402
C2620 2.2UF 20% 10V X5R-CERM 402
C2621 2.2UF 20% 10V X5R-CERM 402
C2630 2.2UF 20% 10V X5R-CERM 402
C2631 2.2UF 20% 10V X5R-CERM 402
C2603 0.1UF 10% 6.3V CERM-X5R 0201
C2604 0.1UF 10% 6.3V CERM-X5R 0201
C2605 0.1UF 10% 6.3V CERM-X5R 0201
C2613 0.1UF 10% 6.3V CERM-X5R 0201
C2614 0.1UF 10% 6.3V CERM-X5R 0201
C2615 0.1UF 10% 6.3V CERM-X5R 0201
C2623 0.1UF 10% 6.3V CERM-X5R 0201
C2624 0.1UF 10% 6.3V CERM-X5R 0201
C2625 0.1UF 10% 6.3V CERM-X5R 0201
C2633 0.1UF 10% 6.3V CERM-X5R 0201
C2634 0.1UF 10% 6.3V CERM-X5R 0201
C2635 0.1UF 10% 6.3V CERM-X5R 0201
C2640 2.2UF 20% 10V X5R-CERM 402
C2641 2.2UF 20% 10V X5R-CERM 402
C2650 2.2UF 20% 10V X5R-CERM 402
C2651 2.2UF 20% 10V X5R-CERM 402
C2660 2.2UF 20% 10V X5R-CERM 402
C2661 2.2UF 20% 10V X5R-CERM 402
C2670 2.2UF 20% 10V X5R-CERM 402
C2671 2.2UF 20% 10V X5R-CERM 402
C2643 0.1UF 10% 6.3V CERM-X5R 0201
C2644 0.1UF 10% 6.3V CERM-X5R 0201
C2645 0.1UF 10% 6.3V CERM-X5R 0201
C2653 0.1UF 10% 6.3V CERM-X5R 0201
C2654 0.1UF 10% 6.3V CERM-X5R 0201
C2655 0.1UF 10% 6.3V CERM-X5R 0201
C2663 0.1UF 10% 6.3V CERM-X5R 0201
C2664 0.1UF 10% 6.3V CERM-X5R 0201
C2665 0.1UF 10% 6.3V CERM-X5R 0201
C2673 0.1UF 10% 6.3V CERM-X5R 0201
C2674 0.1UF 10% 6.3V CERM-X5R 0201
C2675 0.1UF 10% 6.3V CERM-X5R 0201
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 26 OF 118
SHEET 26 OF 81
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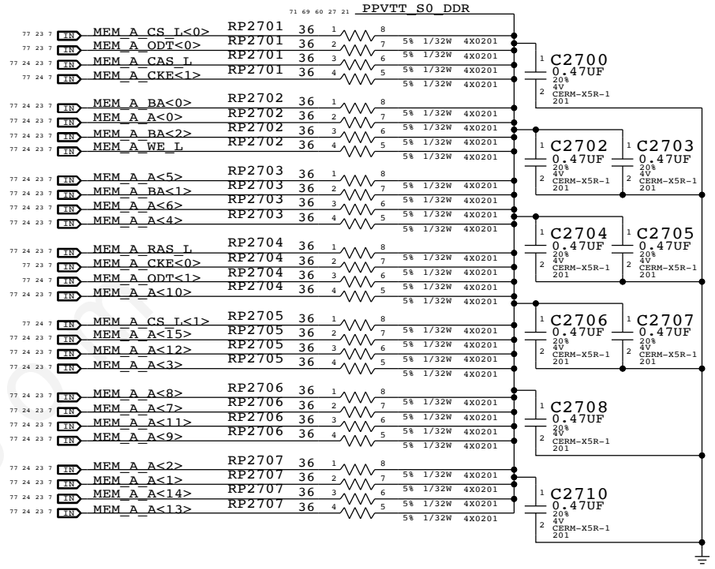
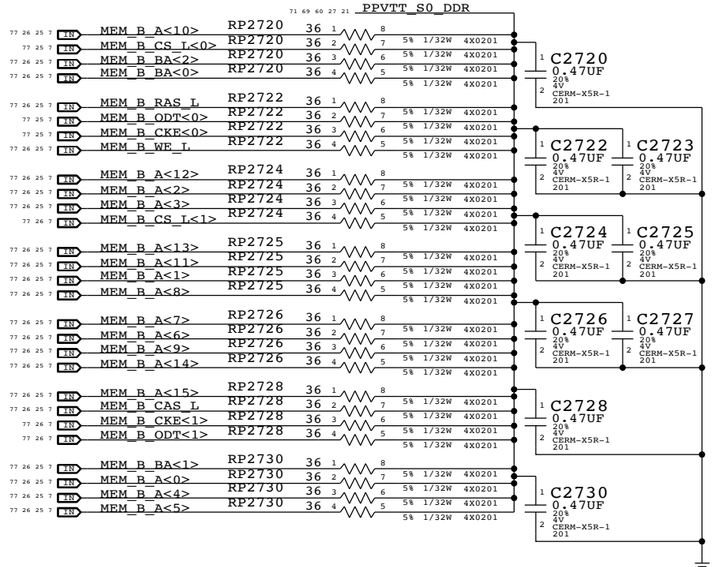
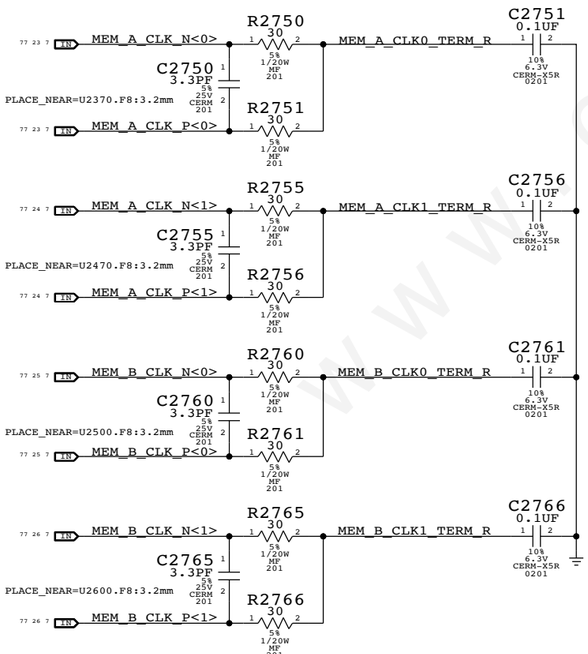
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: DDR3 Termination

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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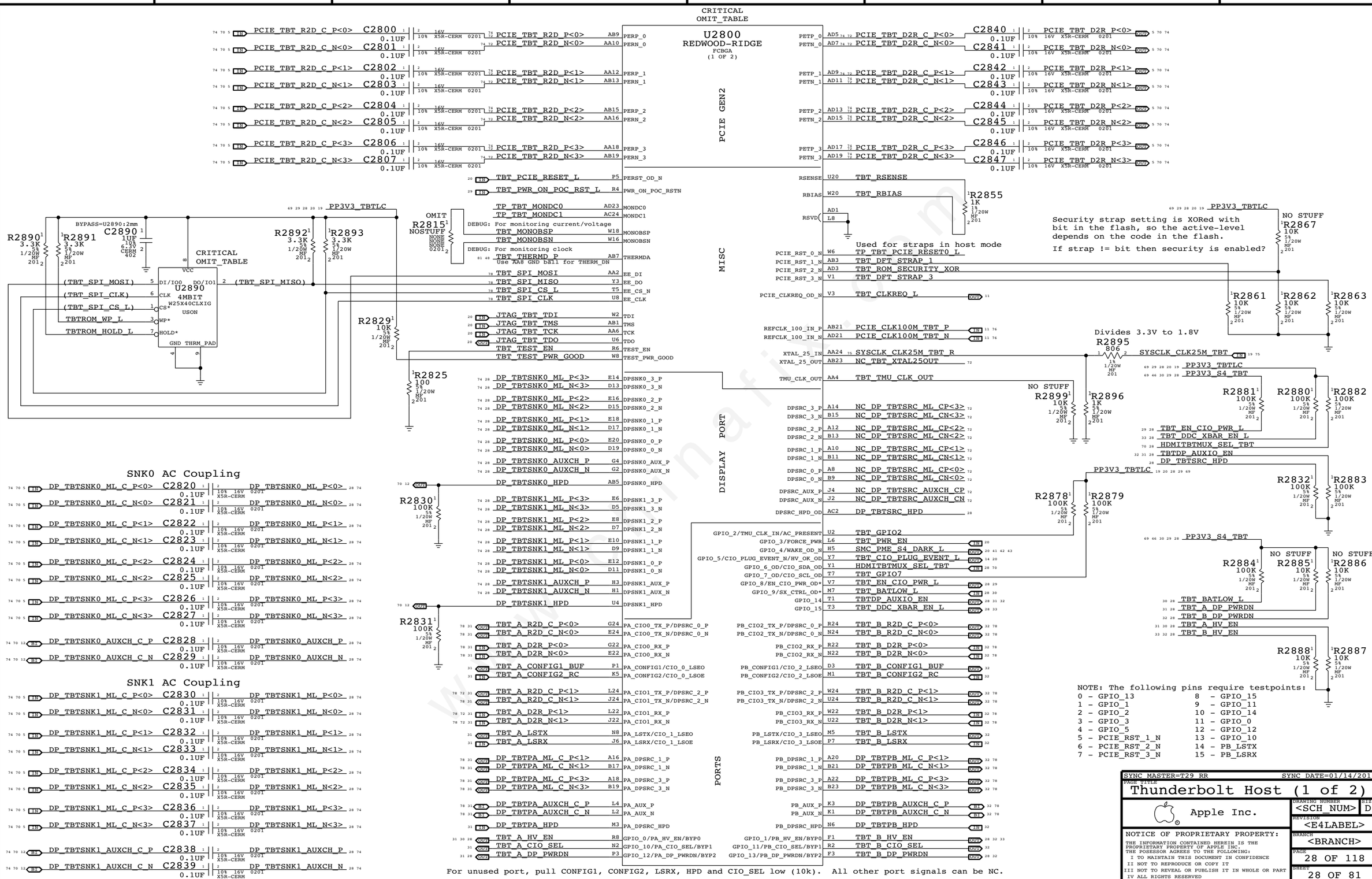
CRITICAL
OMIT_TABLE
U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)
PCIE GEN2
MISC
PORT
DISPLAY
PORTS
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PERP_0
PERN_0
PERP_1
PERN_1
PERP_2
PERN_2
PERP_3
PERN_3
PETP_0
PETN_0
PETP_1
PETN_1
PETP_2
PETN_2
PETP_3
PETN_3
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_C_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_N<3>
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
PERST_OD_N
PWR_ON_POC_RSTN
TP_TBT_MONDC0
TP_TBT_MONDC1
TBT_MONOBSP
TBT_MONOBSN
TBT_THERMD_P
MONDC0
MONDC1
MONOBSP
MONOBSN
THERMDA
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
EE_DI
EE_DO
EE_CS_N
EE_CLK
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
TDI
TMS
TCK
TDO
TEST_EN
TEST_PWR_GOOD
DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_N
DP_TBTSNK0_HPD
DPSNK0_3_P
DPSNK0_3_N
DPSNK0_2_P
DPSNK0_2_N
DPSNK0_1_P
DPSNK0_1_N
DPSNK0_0_P
DPSNK0_0_N
DPSNK0_AUX_P
DPSNK0_AUX_N
DPSNK0_HPD
DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_N
DP_TBTSNK1_HPD
DPSNK1_3_P
DPSNK1_3_N
DPSNK1_2_P
DPSNK1_2_N
DPSNK1_1_P
DPSNK1_1_N
DPSNK1_0_P
DPSNK1_0_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
TBT_TBTPA_ML_C_P<1>
TBT_TBTPA_ML_C_N<1>
TBT_TBTPA_ML_C_P<3>
TBT_TBTPA_ML_C_N<3>
TBT_TBTPA_AUXCH_C_P
TBT_TBTPA_AUXCH_C_N
DP_TBTPA_HPD
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
PA_CIO0_TX_P/DPSRC_0_P
PA_CIO0_TX_N/DPSRC_0_N
PA_CIO0_RX_P
PA_CIO0_RX_N
PA_CONFIG1/CIO_0_LSEO
PA_CONFIG2/CIO_0_LSOE
PA_CIO1_TX_P/DPSRC_2_P
PA_CIO1_TX_N/DPSRC_2_N
PA_CIO1_RX_P
PA_CIO1_RX_N
PA_LSTX/CIO_1_LSEO
PA_LSRX/CIO_1_LSOE
PA_DPSRC_1_P
PA_DPSRC_1_N
PA_DPSRC_3_P
PA_DPSRC_3_N
PA_AUX_P
PA_AUX_N
PA_DPSRC_HPD
GPIO_0/PA_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2
PB_CIO2_TX_P/DPSRC_0_P
PB_CIO2_TX_N/DPSRC_0_N
PB_CIO2_RX_P
PB_CIO2_RX_N
PB_CONFIG1/CIO_2_LSEO
PB_CONFIG2/CIO_2_LSOE
PB_CIO3_TX_P/DPSRC_2_P
PB_CIO3_TX_N/DPSRC_2_N
PB_CIO3_RX_P
PB_CIO3_RX_N
PB_LSTX/CIO_3_LSEO
PB_LSRX/CIO_3_LSOE
PB_DPSRC_1_P
PB_DPSRC_1_N
PB_DPSRC_3_P
PB_DPSRC_3_N
PB_AUX_P
PB_AUX_N
PB_DPSRC_HPD
GPIO_1/PB_HV_EN/BYP0
GPIO_11/PB_CIO_SEL/BYP1
GPIO_13/PB_DP_PWRDN/BYP2
TBT_TBTPB_ML_C_P<1>
TBT_TBTPB_ML_C_N<1>
TBT_TBTPB_ML_C_P<3>
TBT_TBTPB_ML_C_N<3>
TBT_TBTPB_AUXCH_C_P
TBT_TBTPB_AUXCH_C_N
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
NC_DP_TBTSRC_ML_CP<3>
NC_DP_TBTSRC_ML_CN<3>
NC_DP_TBTSRC_ML_CP<2>
NC_DP_TBTSRC_ML_CN<2>
NC_DP_TBTSRC_ML_CP<1>
NC_DP_TBTSRC_ML_CN<1>
NC_DP_TBTSRC_ML_CP<0>
NC_DP_TBTSRC_ML_CN<0>
NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
TBT_GPIO2
TBT_PWR_EN
SMC_PME_S4_DARK_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
TBT_BATLOW_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
TBT_RSENSE
TBT_RBIAS
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
NC_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
PP3V3_TBTLC
Used for straps in host mode
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
Divides 3.3V to 1.8V
SYSCLK_CLK25M_TBT
PP3V3_S4_TBT
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
NO STUFF
OMIT
BYPASS=U2890:2mm
CRITICAL
OMIT_TABLE
U2890
4MBIT
W25X40CLXIG
USON
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
SNK0 AC Coupling
SNK1 AC Coupling
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
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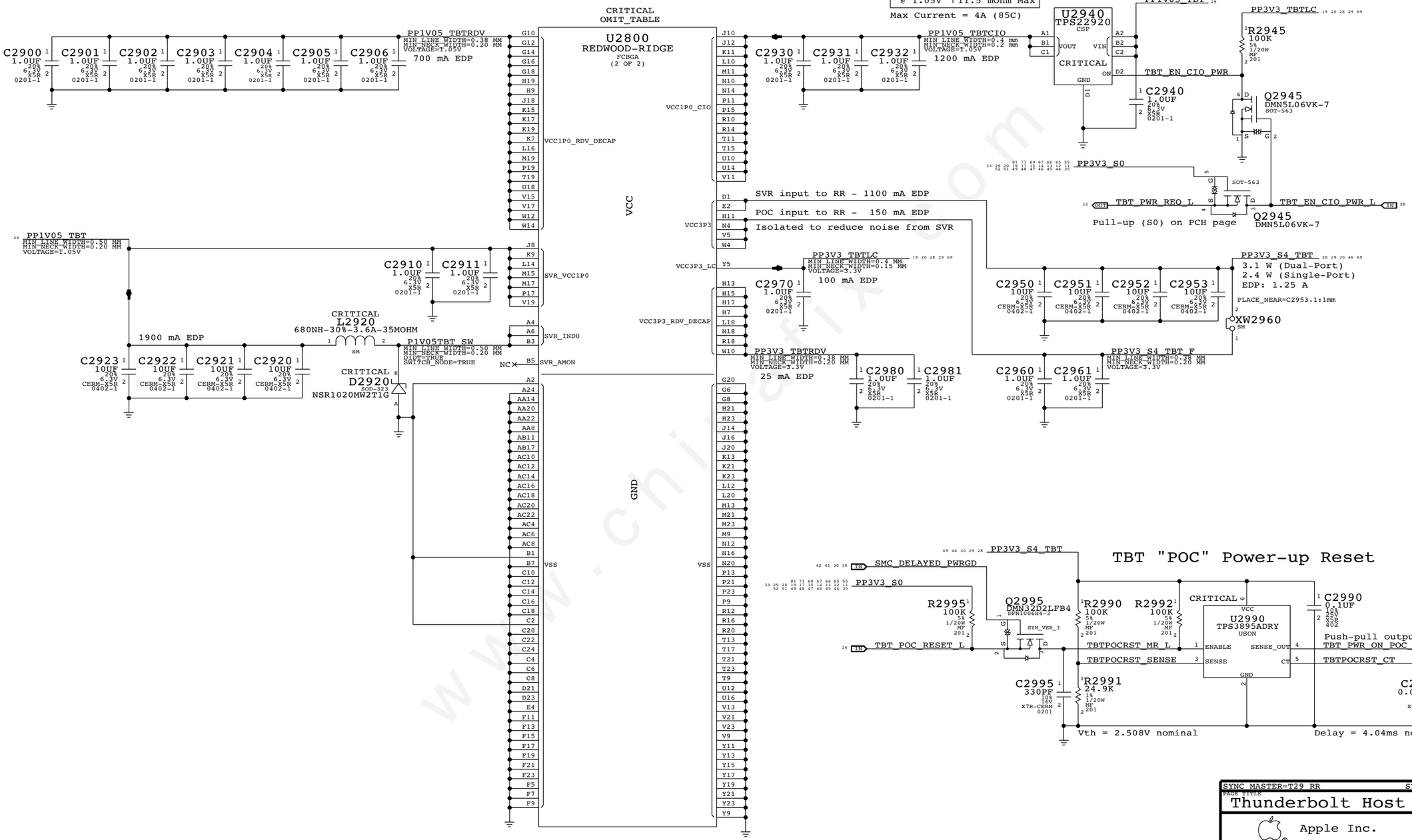

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=T29 RR SYNC_DATE=01/14/2013

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

CRITICAL
Q3080
SI8409DB
BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

71 69 63 57 56 45 PPBUS_G3H
8-13V Input
Changes required for 2S.

R3080 470K 5% 1/16W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/16W MF-LF 402
33 TBTBST_PWREN_L

Q3005
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
31 28 IN TBT_A_HV_EN
Second FET needed for dual-port designs.

49 PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

R3091 200K 1% 1/16W MF-LF 402 <R1>
C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095
3.3UH-6.5A
PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090
LT3957
QFN
VIN 27
SW 8 9 20 21 38
SNS1 6
SNS2 3
NC 1 2 10 35 36
FBX 31
EN/UVLO 25
INTVCC 28
VC 30
RT 33
SS 32
SYNC 34
SGND 4 23 24 37
GND 12 13 14 15 16 17

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS

TBTBST_SNS1
R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
TBTBST_SNS2
XW3095 SM
PLACE_NEAR=C3095.1:2 mm
TBTBST_VSNS
C3088 10PF 5% 50V C0G-CERM 0402
R3095 137K 1% 1/16W MF-LF 402 <Ra>
C3095 33UF-0.06OHM 20% 25V POLY-TANT CASE-D3L
TBTBST_FBX
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>

PP15V_TBT 31 32 69
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz
C3096 10UF 10% 25V X5R 1206-2
NO STUFF
C3097 10UF 10% 25V X5R 805
C3099 0.001UF 10% 50V X7R-CERM 0402

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V C0G-CERM 0402
R3093 49.9K 1% 1/16W MF-LF 402
TBTBST_VC_RC
R3092 73.2K 1% 1/16W MF-LF 402 <R2>
C3092 2.2UF 20% 10V X5R-CERM 402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3094 26.7K 1% 1/16W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Q3088
DMN5L06VK-7
SOT-563
Max Vgs: 10V
R3088 330K 5% 1/16W MF-LF 402
TBTBST_SHDN_DIV
R3087 330K 5% 1/16W MF-LF 402
Q3088
DMN5L06VK-7
SOT-563
SMC_DELAYED_PWRGD IN 19 29 41 42

BATLOW# Isolation

Q3000
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
PP3V3_S4_TBT 28 29 46 69
Pull-up on RR page
43 41 12 IN PM_BATLOW_L
TBT_BATLOW_L OUT 28 30
TBT_BATLOW_L 28 30
MAKE_BASE=TRUE

SYNC_MASTER=T29_RR SYNC_DATE=01/14/2013
PAGE TITLE
Thunderbolt Mobile Support
Apple Inc.
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
CRITICAL
C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
PP15V_TBT
15.75V Max
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 25V X5R 402
CRITICAL
U3210
CD3211A0RGPR
QFN
V3P3
VHV
ENHVU
V3P3OUT
OUT
FAULTZ
PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L
EN
HV_EN
S0
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
VDD
GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V 201 CERM-X5R-1
C3276 0.47UF 20% 4V 201 CERM-X5R-1
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
TBT_A_CONFIG1_RC
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_HPD
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: LSX_A_R2P/P2R (P/N)

Thunderbolt Connector A

CRITICAL
L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
C3200 0.01UF 10% 50V X7R-CERM 0402
C3201 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC
R3201 12 5% 1/20W MF 201
TBT Dir
DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1
C3202 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R-CERM 0201
C3295 330PF 10% 16V X7R-CERM 0201
R3241 100K 5% 1/20W MF 201
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
CRITICAL
J3200
MDP-J44
F-RT-TH
SHIELD PINS
PORT B
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
514-0876
TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3205 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
C3206 0.01UF 10% 25V X5R-CERM 0201
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT: TX_0
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT: TX_1
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
PAGE TITLE
Thunderbolt Connector A
Apple Inc.
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BRANCH <BRANCH>
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
CRITICAL
C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM-1 0603
C3381 0.1UF 10% 16V X5R-CERM 0201
PP15V_TBT
15.75V Max
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 25V X5R 402
CRITICAL
U3310
CD3211A0RGPR
QFN
V3P3
VHV
ENHVU
FAULTZ
V3P3OUT
OUT
EN
HV_EN
S0
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3310 22.6K 1% 1/20W MF 201
R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
R3313 22.6K 1% 1/20W MF 201 <RHVS3>
R3314 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
CRITICAL
U3320
CBTL05024
HVQFN24-COMBO
VDD
GND_VOID=TRUE (Both C's)
C3377 0.47UF 20% 4V 201 CERM-X5R-1
C3376 0.47UF 20% 4V 201 CERM-X5R-1
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
TBT_B_CONFIG1_RC
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD
TBT_B_HPD
TBT_B_CIO_SEL
TBT_B_AUXIO_EN
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
TBT_B_LSX_ML_P<1>
TBT_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
GND_THMPAD

Thunderbolt Connector B

CRITICAL
L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C3300 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V
C3301 0.01UF 10% 50V X7R-CERM 0402
TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3305 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
C3306 0.01UF 10% 25V X5R-CERM 0201
CRITICAL
J3200
MDP-J44
F-RT-TH
SHIELD PINS
PORT A
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
514-0876
DP Dir
TBT Dir
TBT: TX_0
TBT: RX_0
TBT: Unused
TBT: RX_1
TBT: TX_1
TBT: LSX_R2P/P2R (P/N)
GND_VOID=TRUE (Both C's)
C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012
PAGE TITLE
Thunderbolt Connector B
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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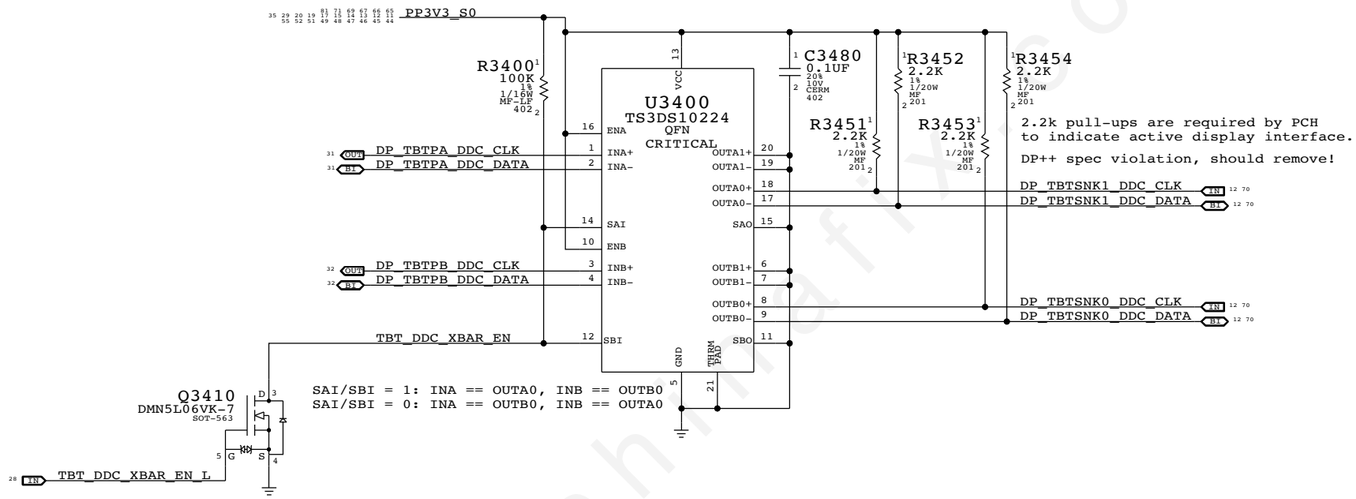
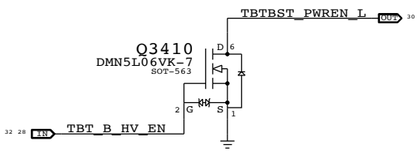
DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!



Second TBT Port HV Boost Enable



SYNC_MASTER=J15_REFERENCE SYNC_DATE=11/16/2012

PAGE TITLE: DDC Crossbar

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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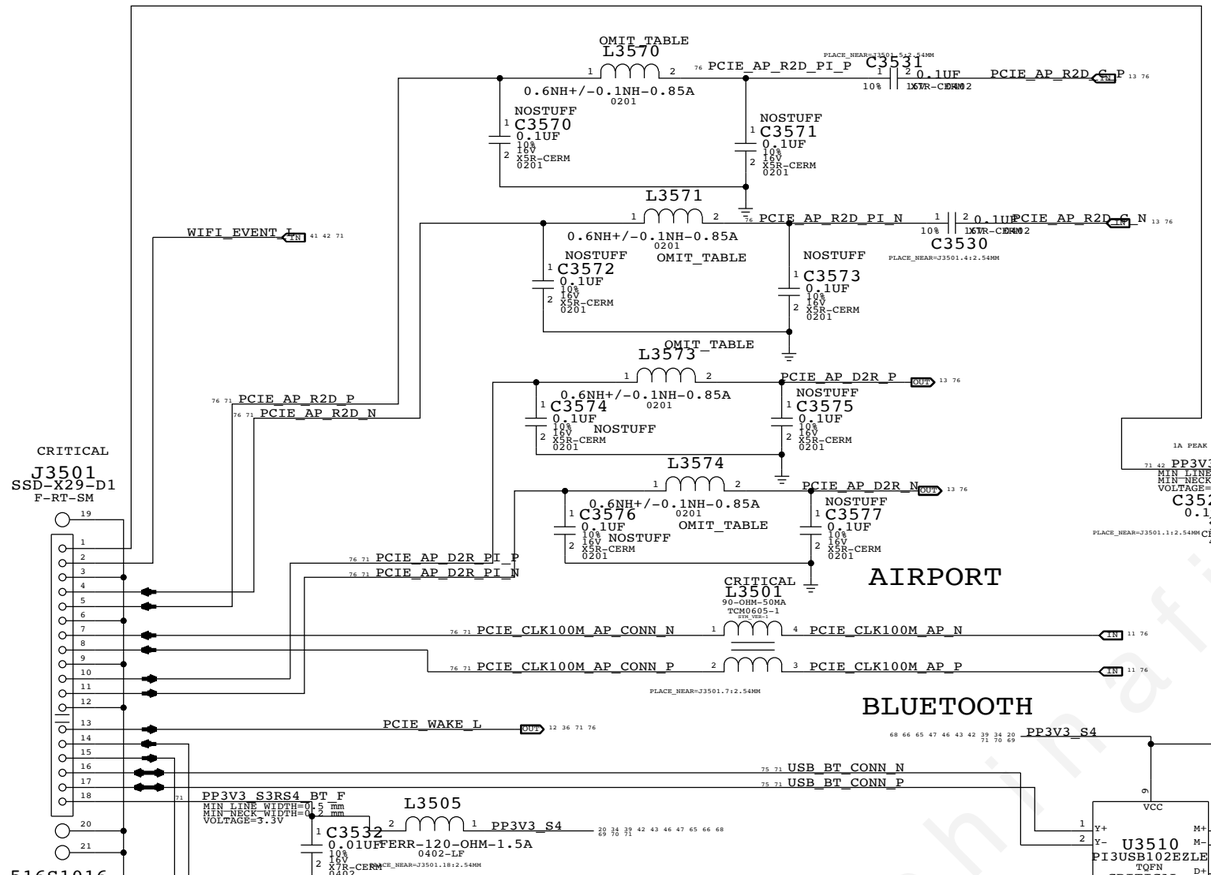
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE

X29C CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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OOB Isolation

PP3V3_S0SW_SSD

C3718 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U3710:5 mm

CRITICAL
74LVC1G08 SOT891
U3710 08
NC

SMC_OOB1_R2D_L (IN)

PP3V3_S0

C3719 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U3711:5 mm

CRITICAL
74LVC1G08 SOT891
U3711 08
NC

SMC_OOB1_D2R_L (OUT)

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603

PP3V3_S0SW_SSD → PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V

C3701 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=L3700.1:1mm
C3702 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=L3700.1:1mm

514S0449
CRITICAL
J3700 SSD-GS3 F-RT-SM

R3700 100K 1% 1/20W MF 201

PP3V3_S0

SSD_RESET_CONN_L
NC_SSD_MFG_RSVD

SMC_OOB1_R2D_CONN_L
SMC_OOB1_D2R_CONN_L
SSD_PCIE_SEL_L (OUT)
SSD_DEVSLP (IN)
SMC_PWRFAIL_WARN_L (IN)
SSD_PWR_FET_EN (IN)

PCIE_SSD_R2D_C_N<3>	C3710 0.1UF	PCIE_SSD_R2D_N<3>	PCIE_SSD_D2R_N<3>
PCIE_SSD_R2D_C_P<3>	C3711 0.1UF	PCIE_SSD_R2D_P<3>	PCIE_SSD_D2R_P<3>
PCIE_SSD_R2D_C_N<2>	C3712 0.1UF	PCIE_SSD_R2D_N<2>	PCIE_SSD_D2R_N<2>
PCIE_SSD_R2D_C_P<2>	C3713 0.1UF	PCIE_SSD_R2D_P<2>	PCIE_SSD_D2R_P<2>
PCIE_SSD_R2D_C_N<1>	C3714 0.1UF	PCIE_SSD_R2D_N<1>	PCIE_SSD_D2R_N<1>
PCIE_SSD_R2D_C_P<1>	C3715 0.1UF	PCIE_SSD_R2D_P<1>	PCIE_SSD_D2R_P<1>
PCIE_SSD_R2D_C_N<0>	C3716 0.1UF	PCIE_SSD_R2D_N<0>	PCIE_SSD_D2R_N<0>
PCIE_SSD_R2D_C_P<0>	C3717 0.1UF	PCIE_SSD_R2D_P<0>	PCIE_SSD_D2R_P<0>

(C3710–C3717: 2 GND_VOID=TRUE, 10% 16V X5R-CERM 0201)

SSD_CLKREQ_CONN_L

PCIE_CLK100M_SSD_N (IN)
PCIE_CLK100M_SSD_P (IN)

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

Gumstick3 Connector

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD
PP3V42_G3H

R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
R3742 100K 1% 1/20W MF 201

CRITICAL
U3740 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, IN, OUT (OD), THRM PAD, GND

C3740 0.1UF 10% 6.3V CERM-X5R 0201

APN 343S0511

P3V3SSD_VMON
SSD_RESET_L (IN)
SSD_PWR_FET_EN (IN)
SSD_CLKREQ_L (OUT)

SSD_PWR_FET_EN — SSD_PWR_FET_EN
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_MLB_KEPLER SYNC_DATE=06/08/2013

PAGE TITLE: SSD Connector

Apple Inc.

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REVISION: <E4LABEL>
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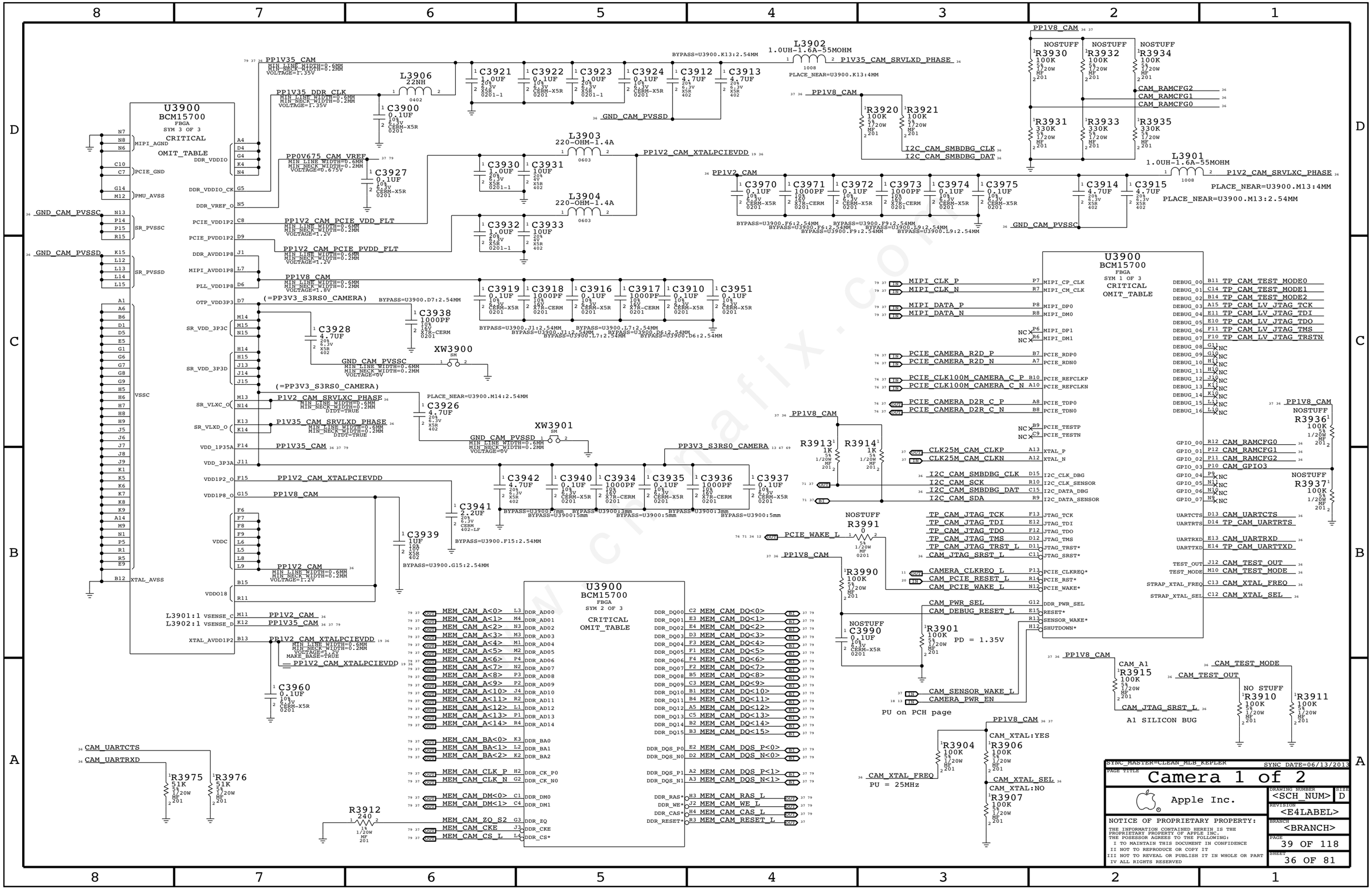
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
XW3900
XW3901
PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PVDD_FLT
PP1V8_CAM
PP1V2_CAM
PP1V2_CAM_XTALPCIEVDD
PP1V35_CAM_SRVLXD_PHASE
PP1V2_CAM_SRVLXC_PHASE
P1V2_CAM_SRVLXC_PHASE
P1V35_CAM_SRVLXD_PHASE
PP3V3_S3RS0_CAMERA
GND_CAM_PVSSD
GND_CAM_PVSSC
I2C_CAM_SMBDBG_CLK
I2C_CAM_SMBDBG_DAT
CAM_RAMCFG2
CAM_RAMCFG1
CAM_RAMCFG0
MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
I2C_CAM_SCK
I2C_CAM_SDA
TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
CAM_PWR_SEL
CAM_DEBUG_RESET_L
CAMERA_PWR_EN
CAM_SENSOR_WAKE_L
PCIE_WAKE_L
CAM_XTAL_FREQ
CAM_XTAL_SEL
CAM_XTAL:YES
CAM_XTAL:NO
CAM_UARTCTS
CAM_UARTRXD
CAM_TEST_MODE
CAM_TEST_OUT
MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
MEM_CAM_CLK_P
MEM_CAM_CLK_N
MEM_CAM_DM<0>
MEM_CAM_DM<1>
MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
MEM_CAM_DQ<0>
MEM_CAM_DQ<1>
MEM_CAM_DQ<2>
MEM_CAM_DQ<3>
MEM_CAM_DQ<4>
MEM_CAM_DQ<5>
MEM_CAM_DQ<6>
MEM_CAM_DQ<7>
MEM_CAM_DQ<8>
MEM_CAM_DQ<9>
MEM_CAM_DQ<10>
MEM_CAM_DQ<11>
MEM_CAM_DQ<12>
MEM_CAM_DQ<13>
MEM_CAM_DQ<14>
MEM_CAM_DQ<15>
MEM_CAM_DQS_P<0>
MEM_CAM_DQS_N<0>
MEM_CAM_DQS_P<1>
MEM_CAM_DQS_N<1>
MEM_CAM_RAS_L
MEM_CAM_WE_L
MEM_CAM_CAS_L
MEM_CAM_RESET_L
PU on PCH page
PU = 25MHz
PU = 1.35V
A1 SILICON BUG
NOSTUFF
NO STUFF
SYNC_MASTER=CLEAN_MLB_KEPLER
SYNC DATE=06/13/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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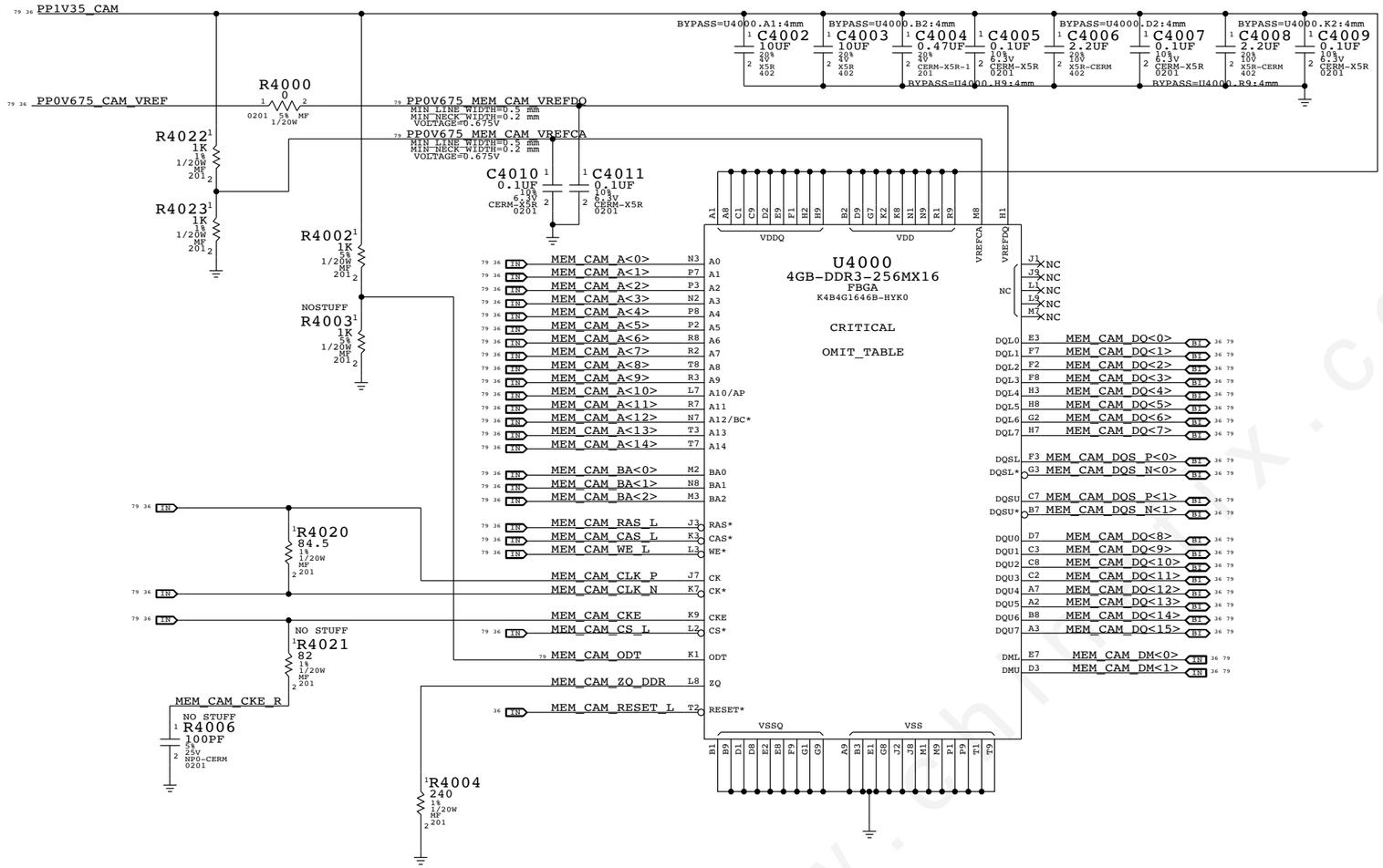


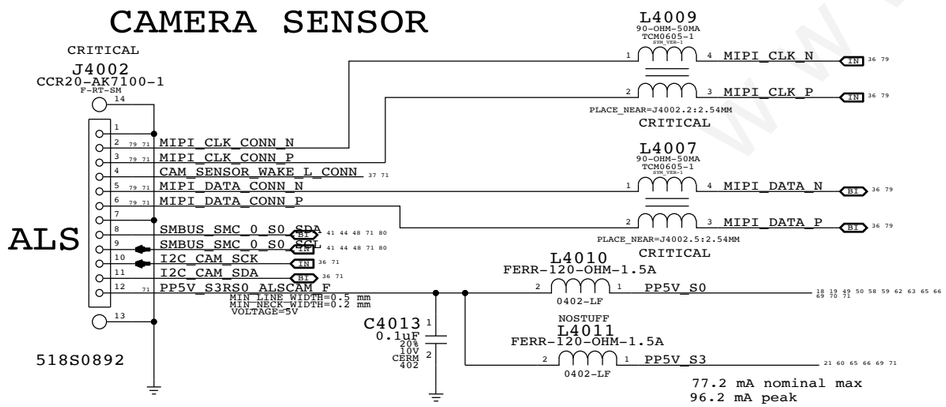
remove DRAM SPD Straps

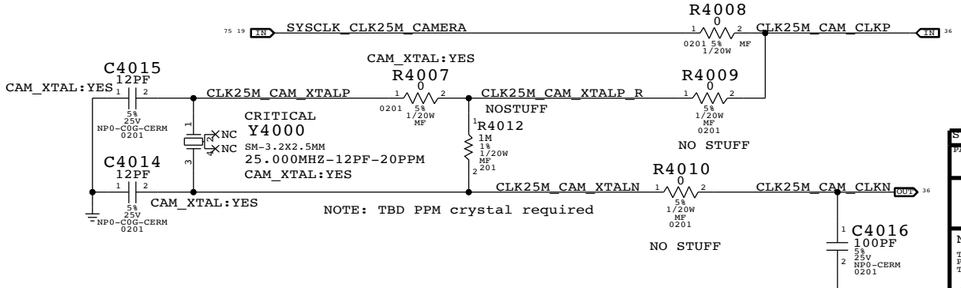
DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR





SYNC_MASTER=CLEAN_MLB_KEPLER	SYNC_DATE=06/13/2013
PAGE TITLE	Camera 2 of 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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USB Port Power Switch

71 69 68 67 66 65 61 51 PP5V_S4

71 68 66 41 34 21 12 PM_SLP_S4_L

R4690 1 0 5% 1/16W MF-LF 402 2

USB_PWR_EN

18 OUT USB_EXTA_OC_L

CRITICAL
U4600
TPS2557DRB
SON

2	IN_0	OUT1	6
3	IN_1	OUT2	7
8	FAULT*	ILIM	5 USB_ILIM
4	EN		
	THRM		
	GND PAD		

NOSTUFF
C4692 1 0.47UF 10% 10V X5R 0402 2

CRITICAL
C4696 1 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1 2

C4690 1 10UF 20% 6.3V X5R 603 2

C4691 1 0.1UF 20% 10V CERM 402 2

R4601 1 22.1K 1% 1/20W MF 201 2

USB_ILIM_R

R4600 1 22.1K 1% 1/16W MF-LF 402 2

C4695 1 10UF 20% 6.3V X5R 603 2

PP5V_S3_LTUSB_A_ILIM
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

Left USB Port A

CRITICAL
L4605
FERR-120-OHM-3A
0603

C4605 1 0.01UF 10% 10V X7R-CERM 0402 2

PP5V_S3_LTUSB_A_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin

CRITICAL
L4600
90-OHM-5MA
TCM0605-1

75 USB_EXTA_MUXED_N

75 USB_EXTA_MUXED_P

CRITICAL
D4601
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
D4600
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
J4600
USB3.0-J44-ALT
F-RT-TH

1	VBUS	13	
2	SSTX+	14	
3	SSTX-	15	
4	GND	16	
5	D-	17	
6	D+	18	
7	GND	19	
8	SSRX+	20	
9	SSRX-	21	
10	GND	22	
11		23	
12			

514-0934

75 USB3_EXTA_R2D_P

75 USB3_EXTA_R2D_N

75 USB_LT1_N

75 USB_LT1_P

75 13 OUT USB3_EXTA_D2R_N

75 13 OUT USB3_EXTA_D2R_P

CRITICAL
D4610
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
D4611
ESD0P2RF-02LS
TSSLP-2-1

USB/SMC Debug Mux

50 44 43 42 41 39 35 19 71 69 66 57 16 PP3V42_G3H

C4650 1 0.1UF 20% 10V CERM 402 2

VCC

R4650 1 100K 5% 1/16W MF-LF 402 2

75 42 41 IN SMC_DEBUGPRT_RX_L

75 42 41 OUT SMC_DEBUGPRT_TX_L

75 13 BI USB_EXTA_P

75 13 BI USB_EXTA_N

U4650
PI3USB102EZLE
TQFN
CRITICAL

5	M+	Y+	1
4	M-	Y-	2
7	D+		
6	D-		
8	OE*	SEL	10
	GND		

SMC_DEBUGPRT_EN_L IN 41

SEL=0 Choose SMC

SEL=1 Choose USB

SIGNAL_MODEL=MOJO_MUX_USBONLY

NOSTUFF
R4651 1 0 5% 1/20W MF 0201 2

NOSTUFF
R4652 1 0 5% 1/20W MF 0201 2

GND_VOID=TRUE

75 13 IN USB3_EXTA_R2D_C_N C4610 0.1UF 10% 16V X5R-CERM 0201 1 2

75 13 IN USB3_EXTA_R2D_C_P C4611 0.1UF 10% 16V X5R-CERM 0201 1 2

GND_VOID=TRUE

CRITICAL
D4612
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
D4613
ESD0P2RF-02LS
TSSLP-2-1

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
USB 3.0 CONNECTORS

Apple Inc.

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REVISION <E4LABEL>

BRANCH <BRANCH>

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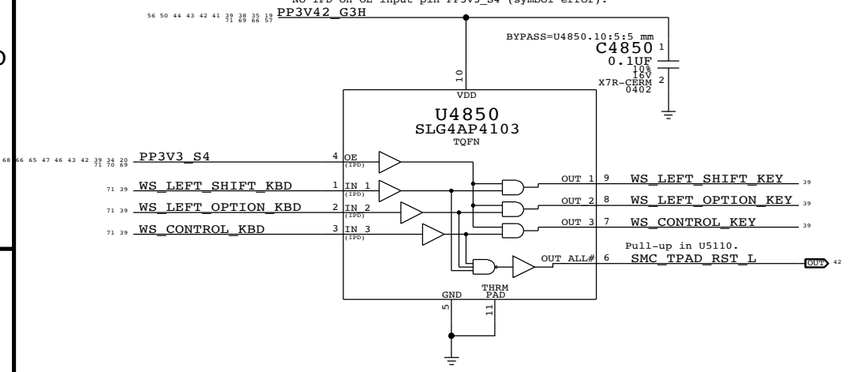
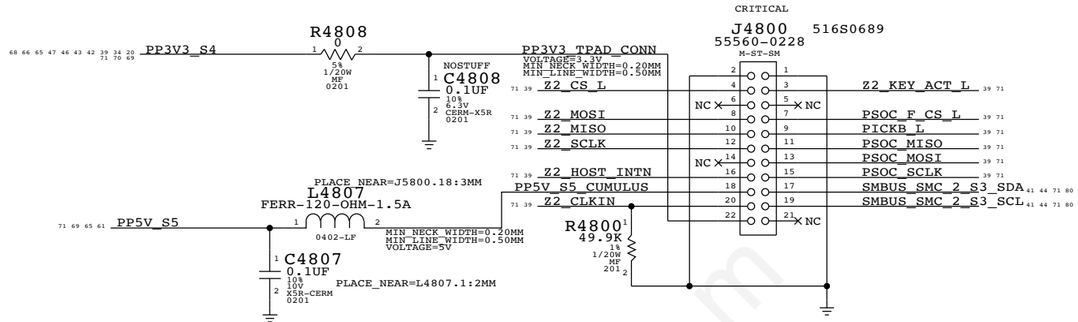
SMC Manual Reset & Isolation

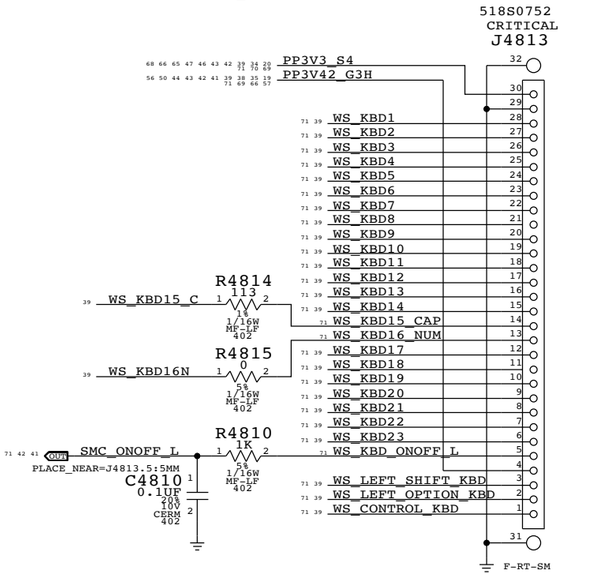
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IPD Flex Connector

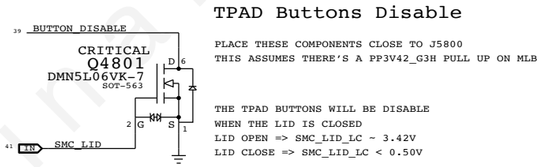


Keyboard Connector



FF14A-30C-R11DL-B-3H

TPAD Buttons Disable

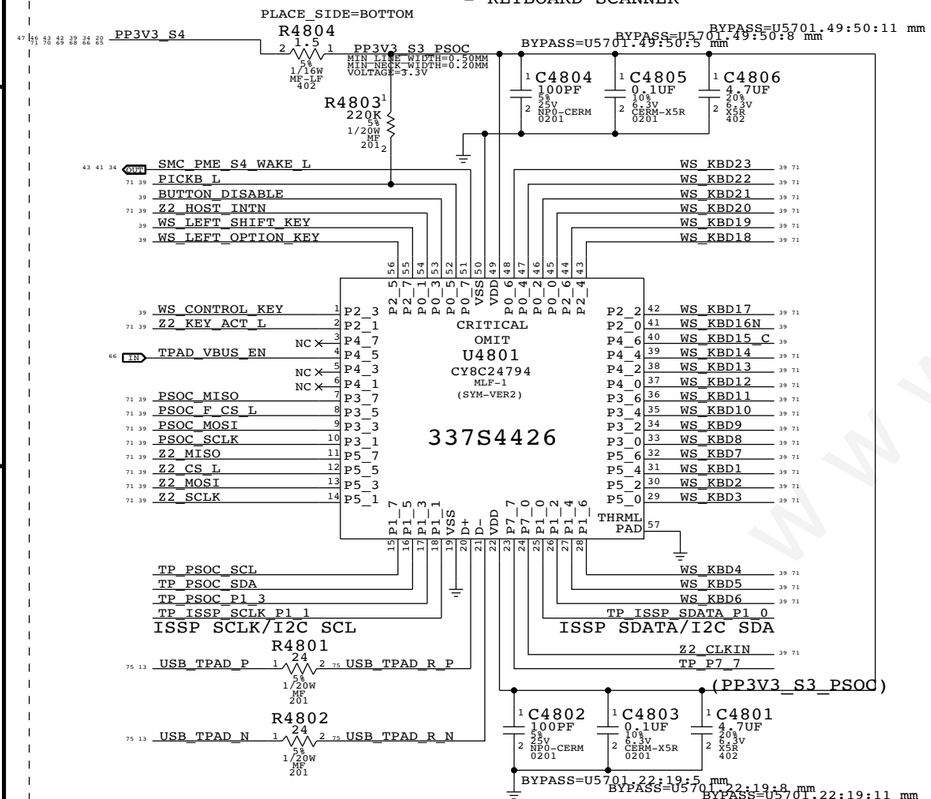


PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC MASTER=CHANG J45 SYNC DATE=03/15/2012

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KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

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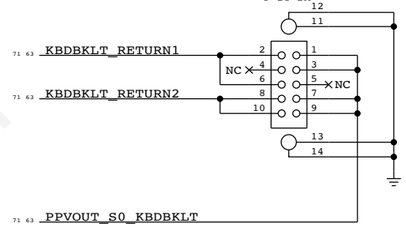
Keyboard Backlight Connector

516S0899
CRITICAL
J4915
AA07A-S010-VA1
F-ST-SM



SYNC MASTER=CHANG J45 SYNC DATE=03/15/2013

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
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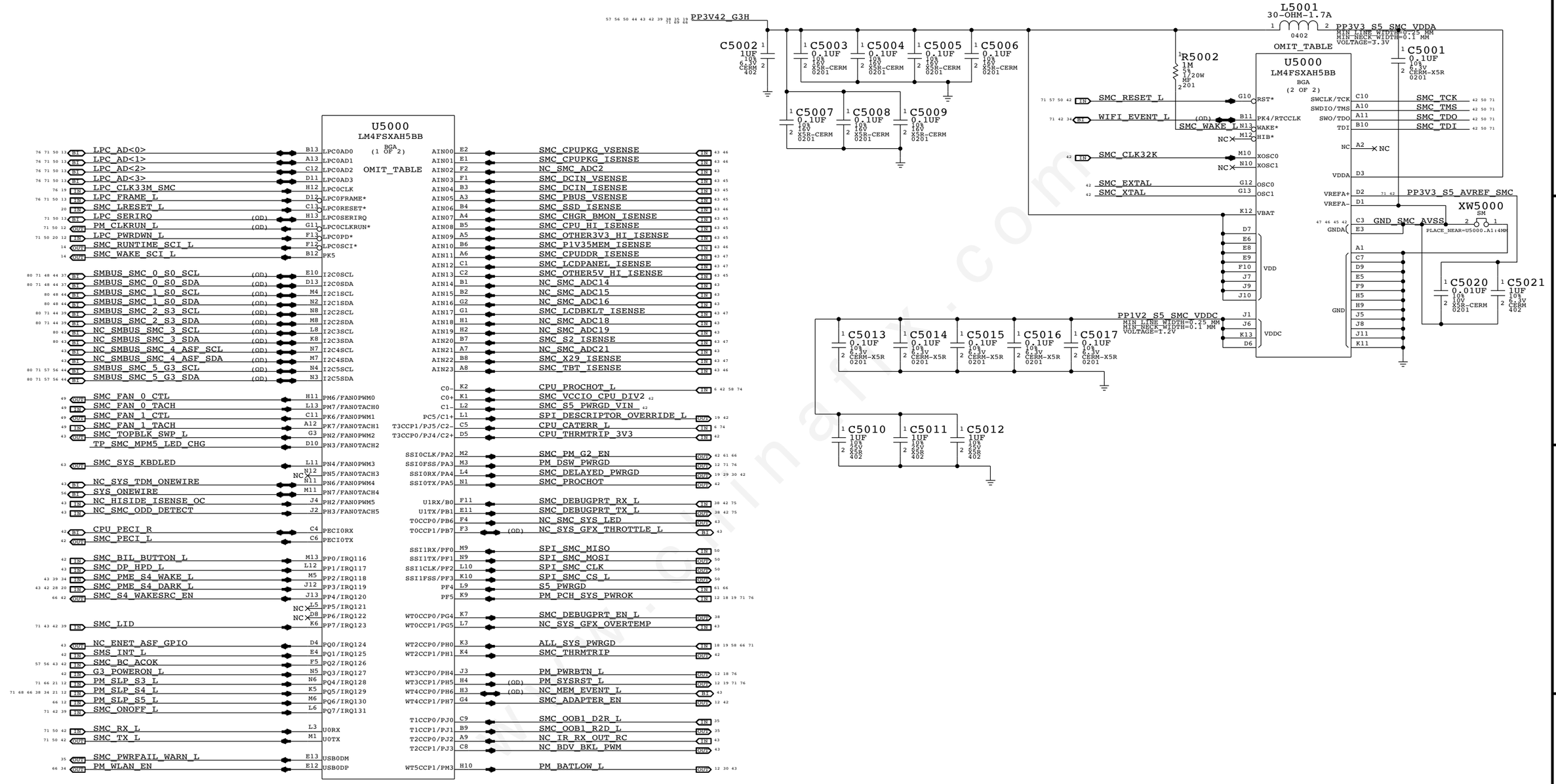
SHEET 40 OF 81

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CHANG J45 SYNC_DATE=03/15/2013

PAGE TITLE: SMC

Apple Inc.

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REVISION: <E4LABEL>

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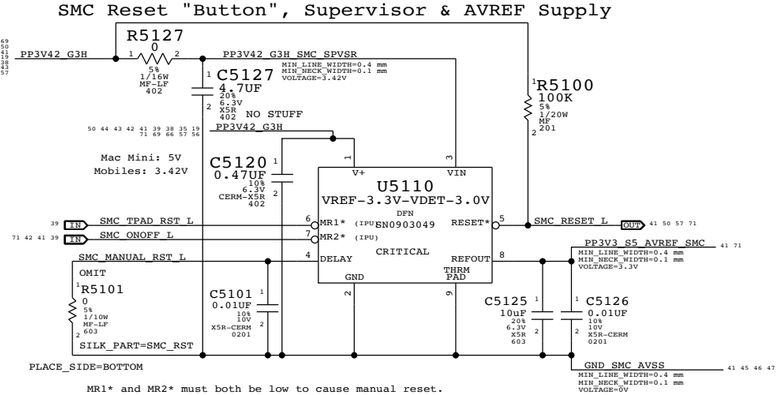
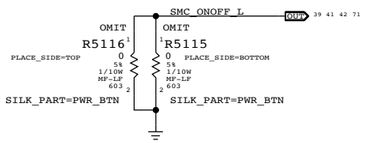
SMC Reset "Button", Supervisor & AVREF Supply



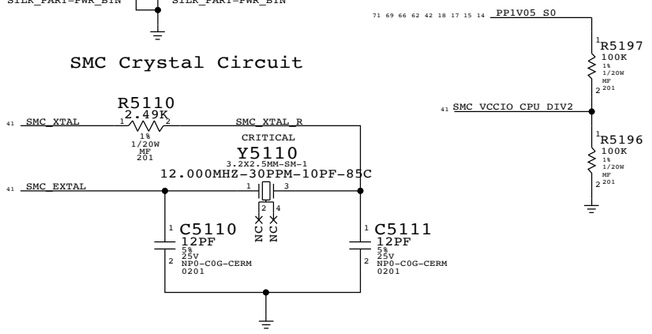
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

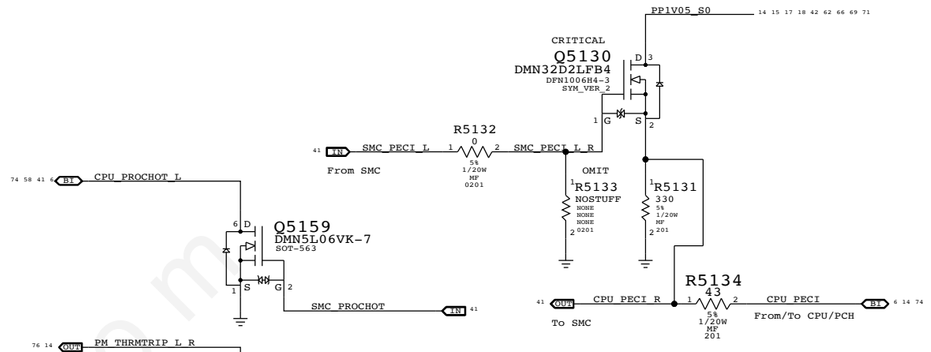


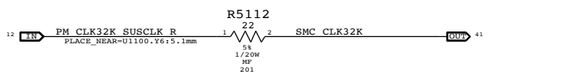
SMC Crystal Circuit

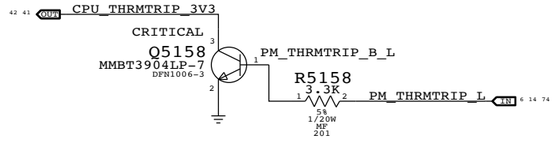


SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

SMC12 PECI SUPPORT







SYNC_MASTER=CHANG J45 SYNC_DATE=11/12/2012

PAGE TITLE: SMC Shared Support

Apple Inc.

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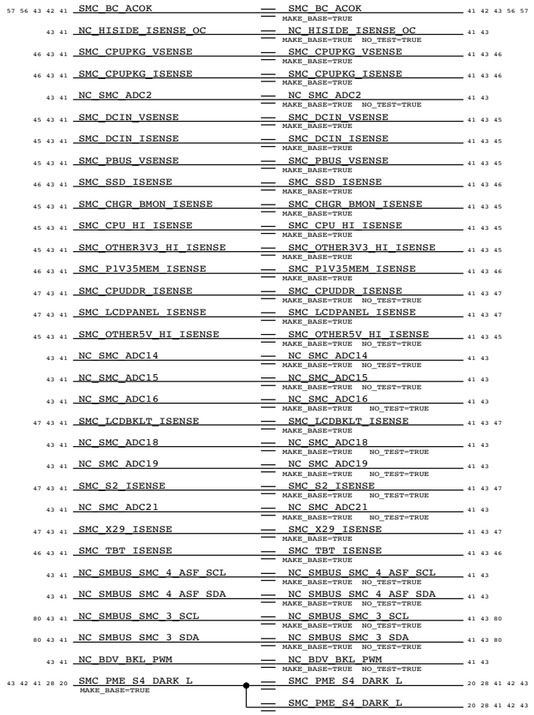
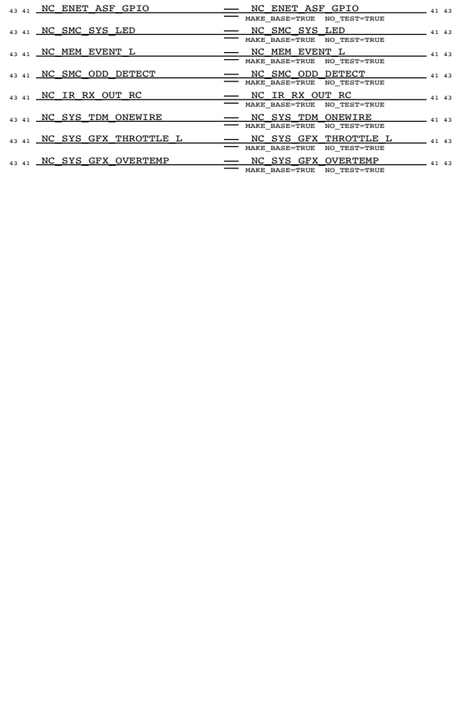
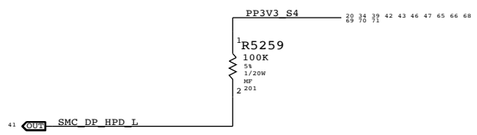
8	7	6	5	4	3	2	1



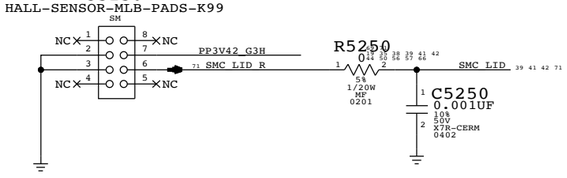


Spare S4 IRQ

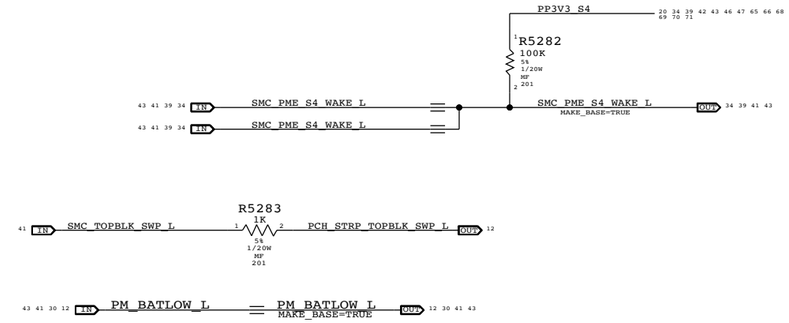


Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	



PAGE TITLE
SMC Project Support

Apple Inc.

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PCH SMBus "0" Connections

PP3V3_S0

R5300 1K 5% 1/16W MF-LF 402
R5301 1K 5% 1/16W MF-LF 402

Lynx Point
U1100
(MASTER)
- SMBUS_PCH_CLK — MAKE_BASE=TRUE
- SMBUS_PCH_DATA — MAKE_BASE=TRUE

VRef DACs
U2200
(Write: 0x98 Read: 0x99)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

Margin Control
U2201
(Write: 0x30 Read: 0x31)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

XDP Connectors
J1800 & J1850
(MASTER)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

LED BACKLIGHT
U7100
(WRITE: 0x58 READ: 0x59)
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

PCH "SMLink 0" Connections

PP3V3_S0

R5310 8.2K 5% 1/16W MF-LF 402
R5311 8.2K 5% 1/16W MF-LF 402

Lynx Point
U1100
(MASTER)
- SML_PCH_0_CLK — MAKE_BASE=TRUE
- SML_PCH_0_DATA — MAKE_BASE=TRUE

PCH "SMLink 1" Connections

PP3V3_S0

NO STUFF
R5320 8.2K 5% 1/20W MF 201
NO STUFF
R5321 8.2K 5% 1/20W MF 201
R5323 0 5% 1/20W MF 0201
R5322 0 5% 1/20W MF 0201

Lynx Point
U1100
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK — MAKE_BASE=TRUE
- SML_PCH_1_DATA — MAKE_BASE=TRUE

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

PP3V3_S0

R5350 2.0K 5% 1/16W MF-LF 402
R5351 2.0K 5% 1/16W MF-LF 402

SMC
U5000
(MASTER)
- SMBUS_SMC_0_S0_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_0_S0_SDA — MAKE_BASE=TRUE

L&R Fin Stack Temp
EMC1412-A: U5860
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

J4002
ALS
(Write: 0x72 Read: 0x73)
- SMBUS_SMC_0_S0_SCL
- SMBUS_SMC_0_S0_SDA

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

PP3V3_S3

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

SMC
U5000
(MASTER)
- SMBUS_SMC_2_S3_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_2_S3_SDA — MAKE_BASE=TRUE

Trackpad
J4801
(Write: 0x90 Read: 0x91)
- SMBUS_SMC_2_S3_SCL
- SMBUS_SMC_2_S3_SDA

SMC "1" SMBUS CONNECTIONS

PP3V3_S0

R5360 1K 5% 1/20W MF 201
R5361 1K 5% 1/20W MF 201

SMC
U5000
(MASTER)
- SMBUS_SMC_1_S0_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_1_S0_SDA — MAKE_BASE=TRUE

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5870
(Write: 0x98 Read: 0x99)
- SMBUS_SMC_1_S0_SCL
- SMBUS_SMC_1_S0_SDA

X29 TEMP
TMP105: U5823
(WRITE: 0X92 READ: 0X93)
- SMBUS_SMC_1_S0_SCL
- SMBUS_SMC_1_S0_SDA

SMC "5" SMBUS CONNECTIONS

PP3V42_G3H

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

SMC
U5000
(MASTER)
- SMBUS_SMC_5_G3_SCL — MAKE_BASE=TRUE
- SMBUS_SMC_5_G3_SDA — MAKE_BASE=TRUE

Battery Charger
ISL6258 - U7100
(Write: 0x12 Read: 0x13)
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA

Battery
J7050
(Write: 0x16 Read: 0x17)
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA

SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SYNC_MASTER=CHANG J45 SYNC_DATE=11/26/2012

PAGE TITLE: SMBus Connections

Apple Inc.

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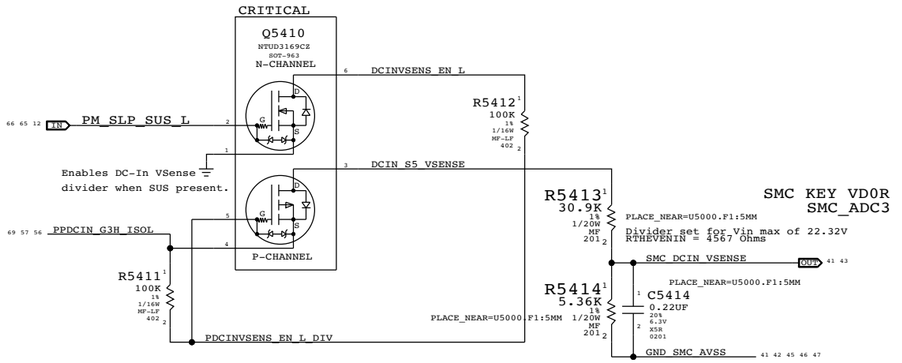
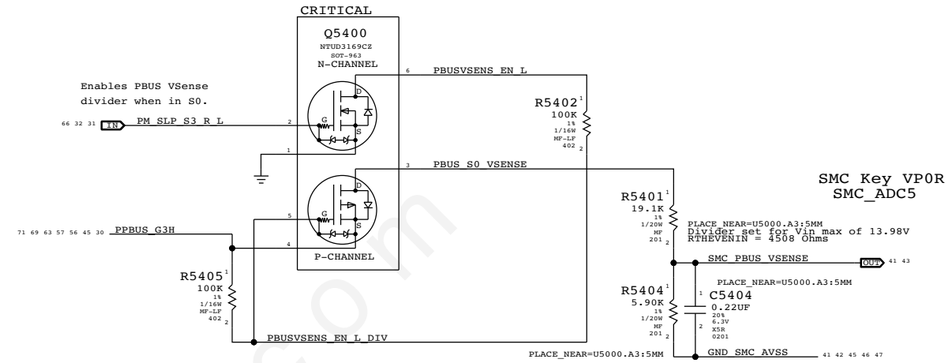
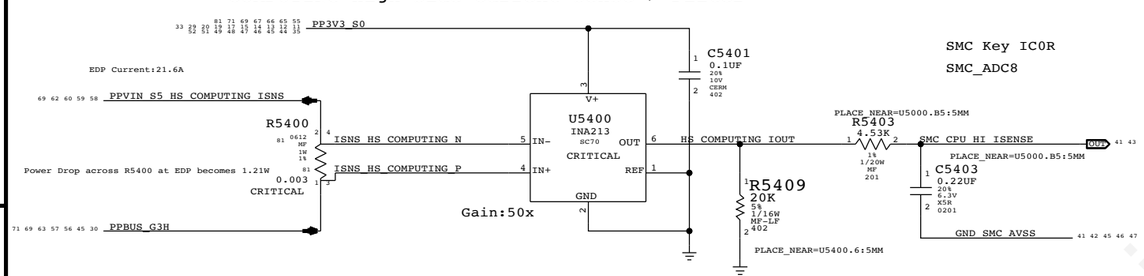
DC-In Voltage Sense Enable & Filter



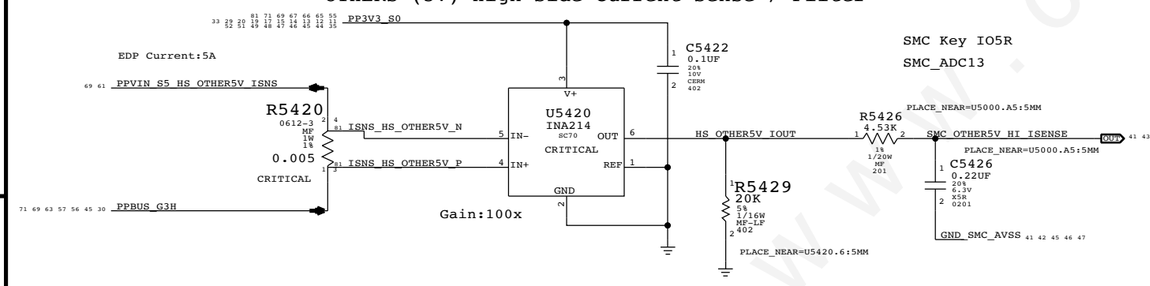
PBUS Voltage Sense Enable & Filter



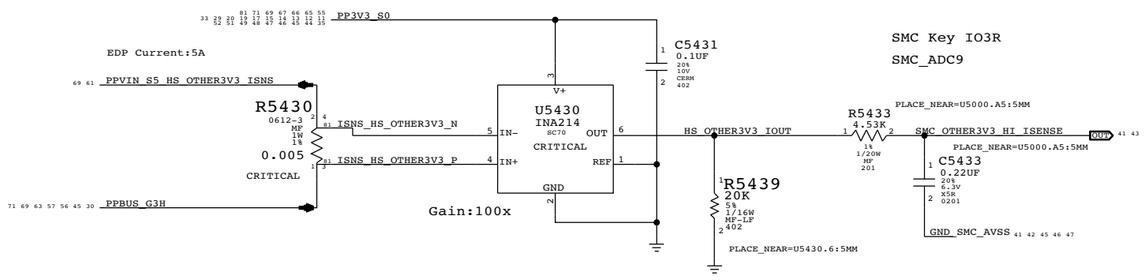
COMPUTING High Side Current Sense / Filter



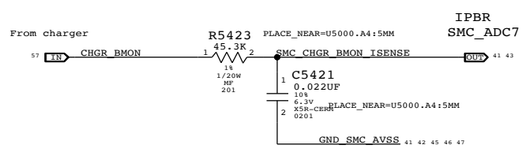
OTHERS (5V) High Side Current Sense / Filter



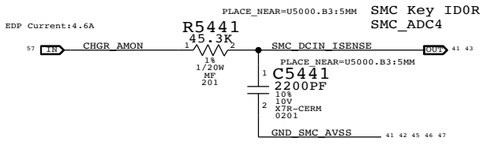
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CHANG J45	SYNC_DATE=12/21/2012
PAGE TITLE: High Side Voltage and Current Sensing	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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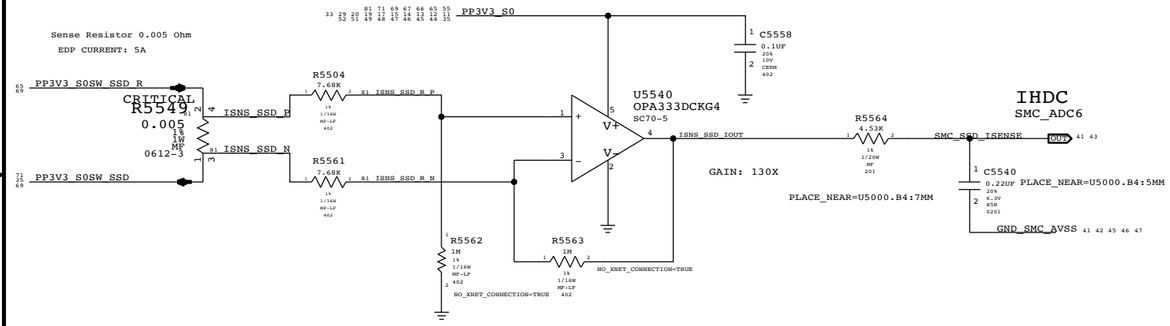
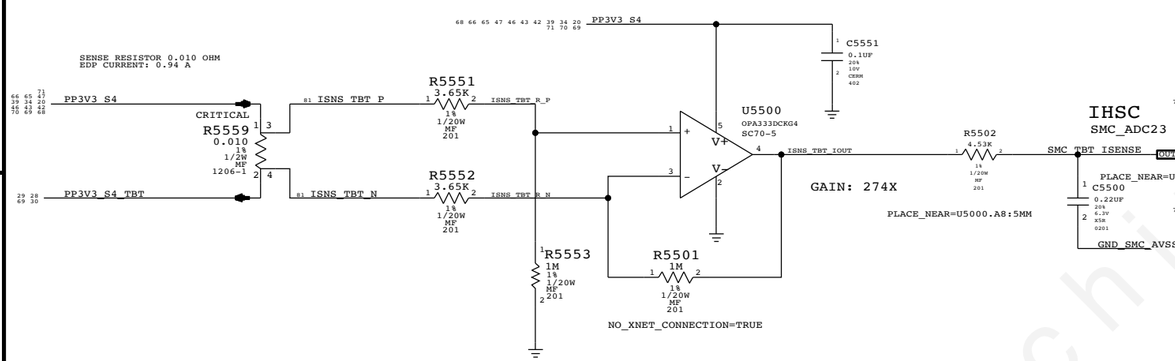
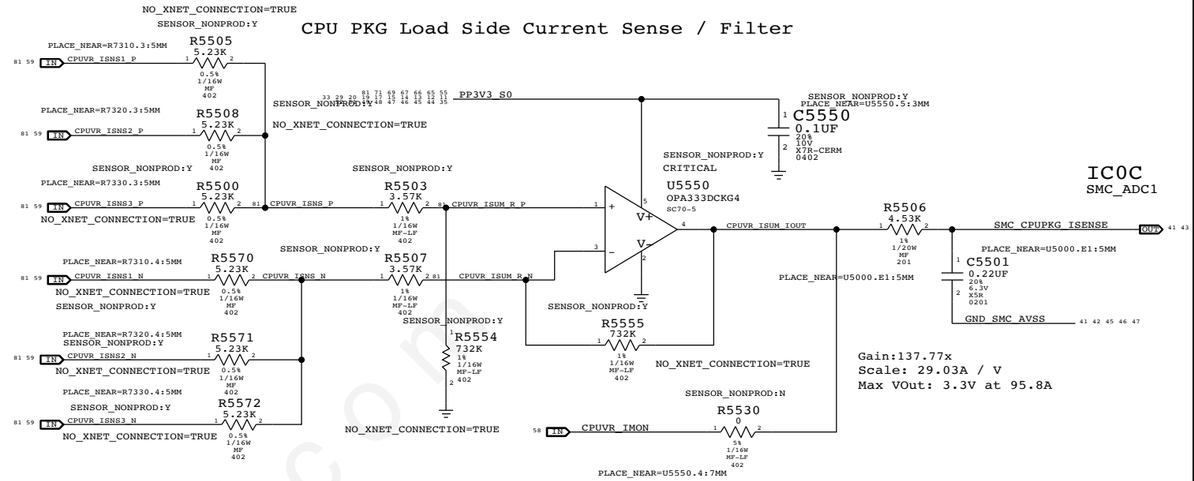
SSD CURRENT SENSE



TBT Router CURRENT SENSE

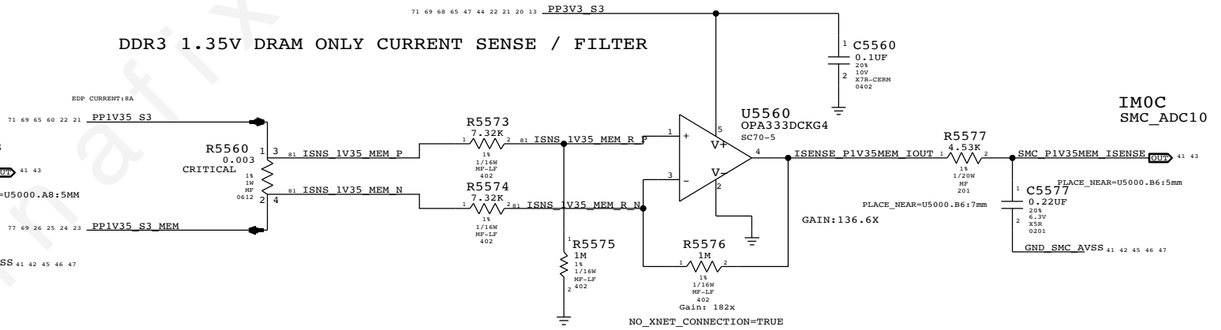


CPU PKG Load Side Current Sense / Filter

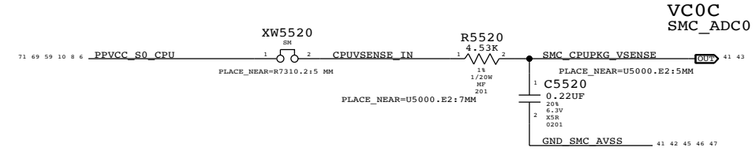


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



CPU Vcore Voltage Sense / Filter



SYNC MASTER=CHANG J45 SYNC DATE=03/15/2013

PAGE TITLE: Load Side Voltage and Current Sensing

Apple Inc.

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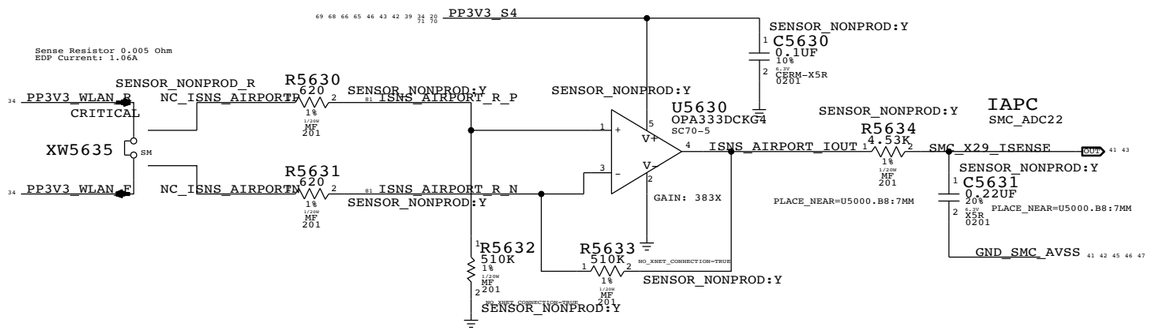
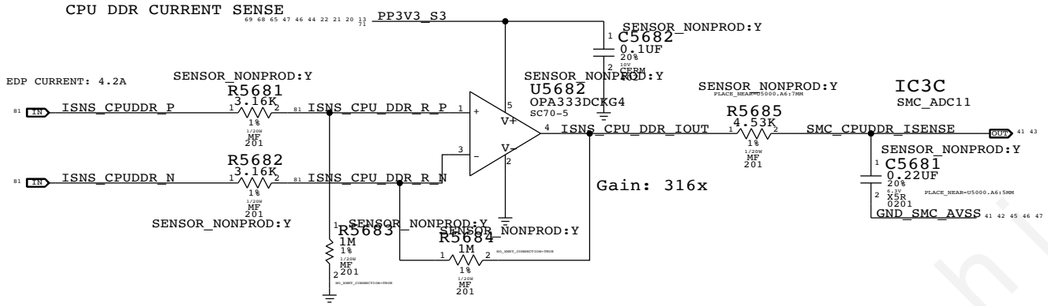
X29 AIRPORT CURRENT SENSE

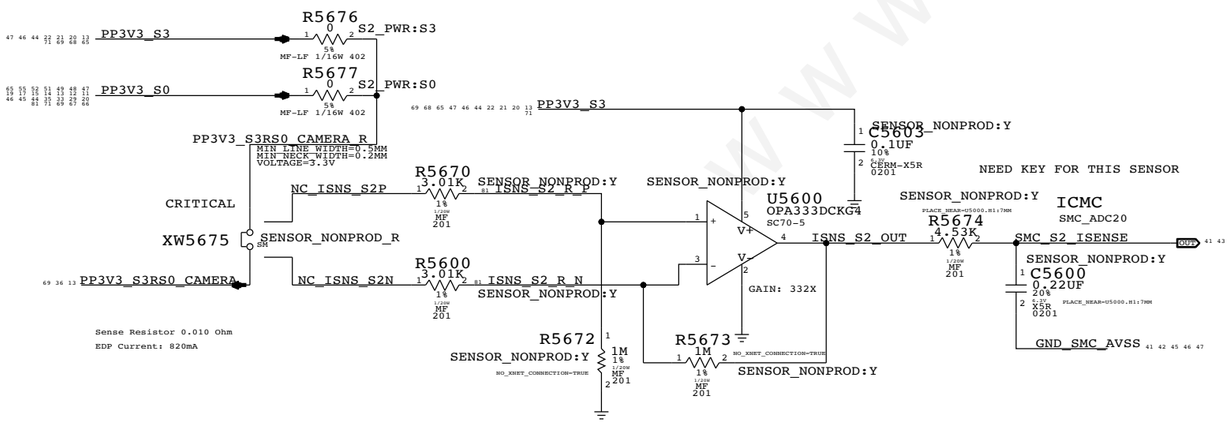


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671,C5610		SENSOR_NONPROD:N

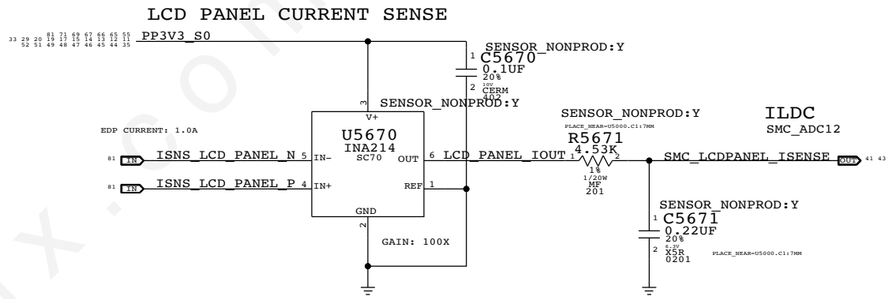
CPU DDR CURRENT SENSE



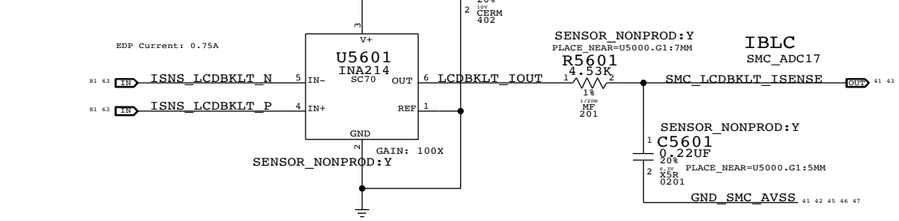
S2 CAMERA CONTROLLER CURRENT SENSE



LCD PANEL CURRENT SENSE



LCD BKLT Current Sense



SYNC MASTER=CHANG J45 SYNC DATE=12/21/2012

PAGE TITLE

Debug Sensors

Apple Inc.

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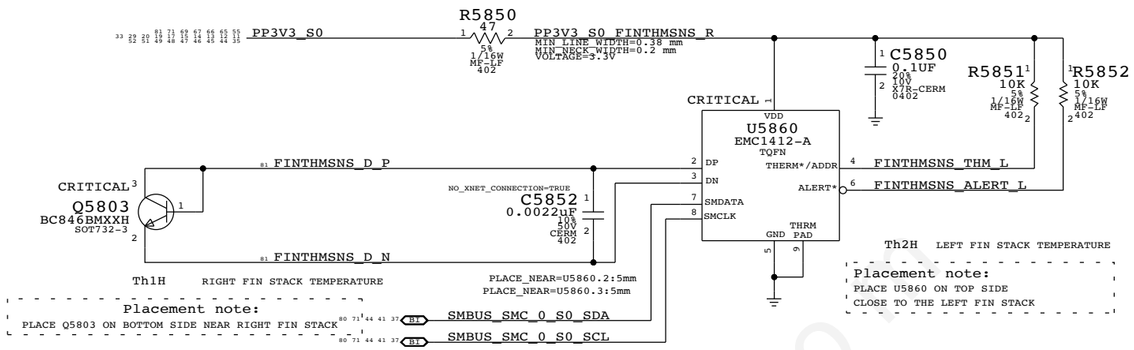
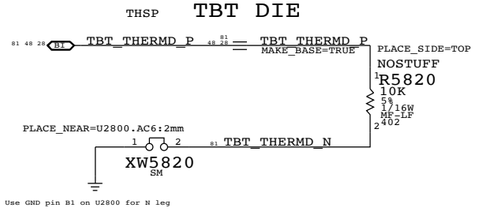
LEFT FIN STACK/RIGHT FIN STACK

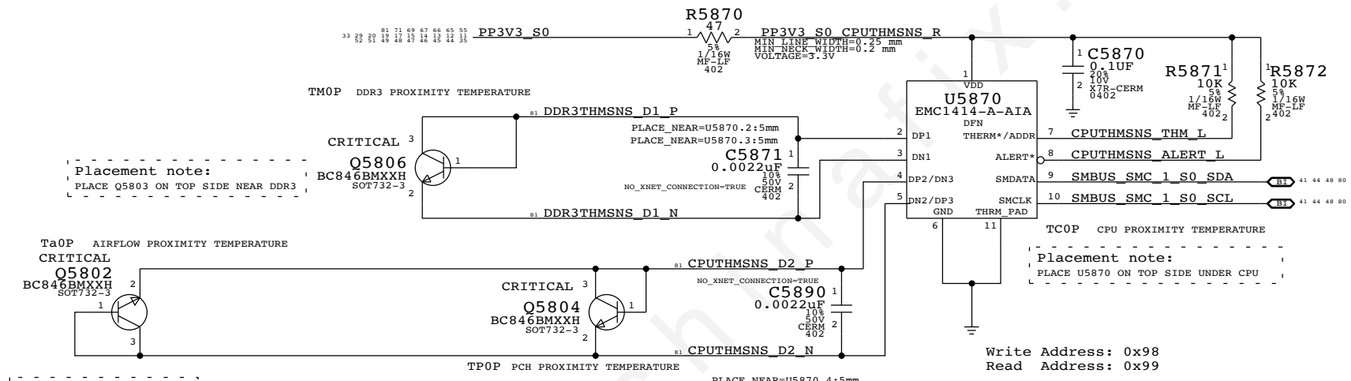


Write Address: 0x98
Read Address: 0x99

TBT DIE

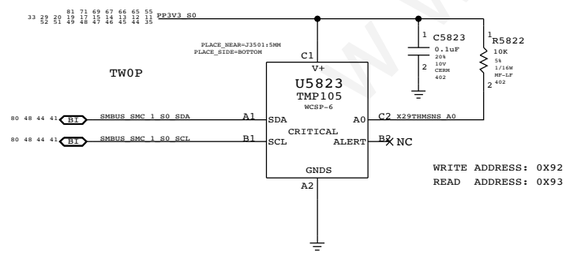


DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



Write Address: 0x98
Read Address: 0x99

X29 PROXIMITY



WRITE ADDRESS: 0X92
READ ADDRESS: 0X93

SYNC_MASTER=CHANG J45 SYNC_DATE=11/26/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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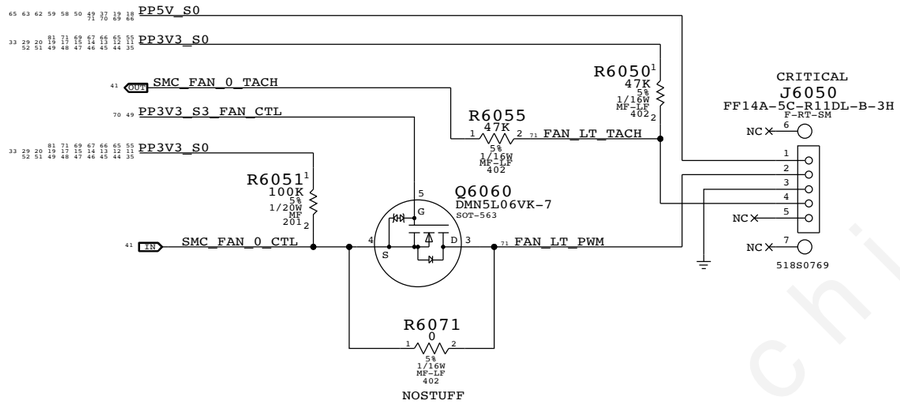
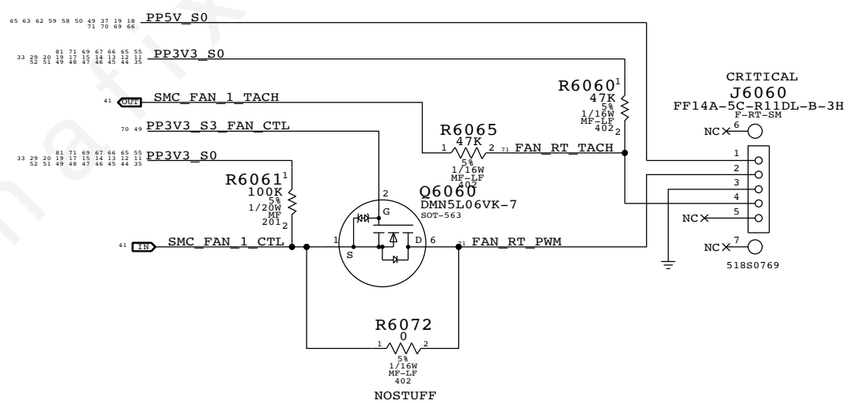
Left Fan



Right Fan



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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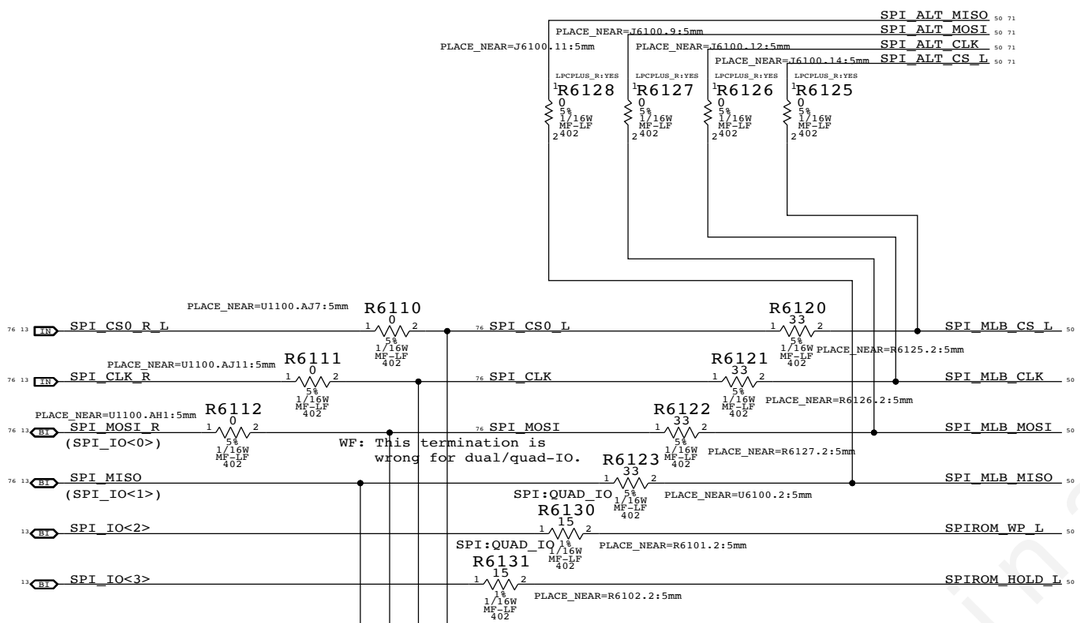
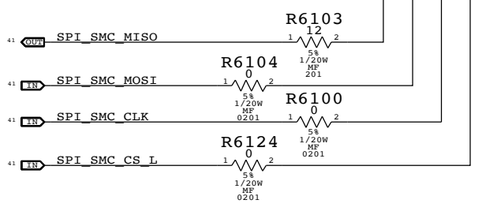
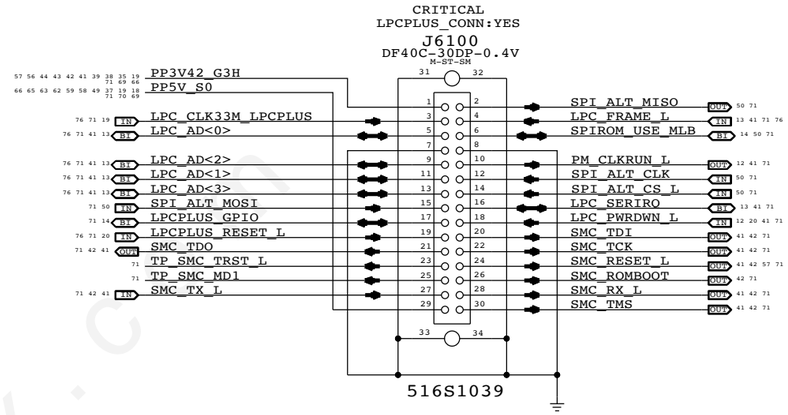
SPI Bus Series Termination



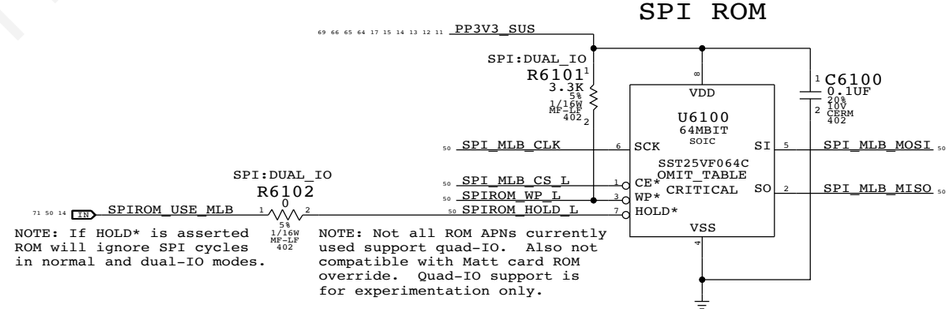
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
SPI ROM / LPC+SPI Conn.

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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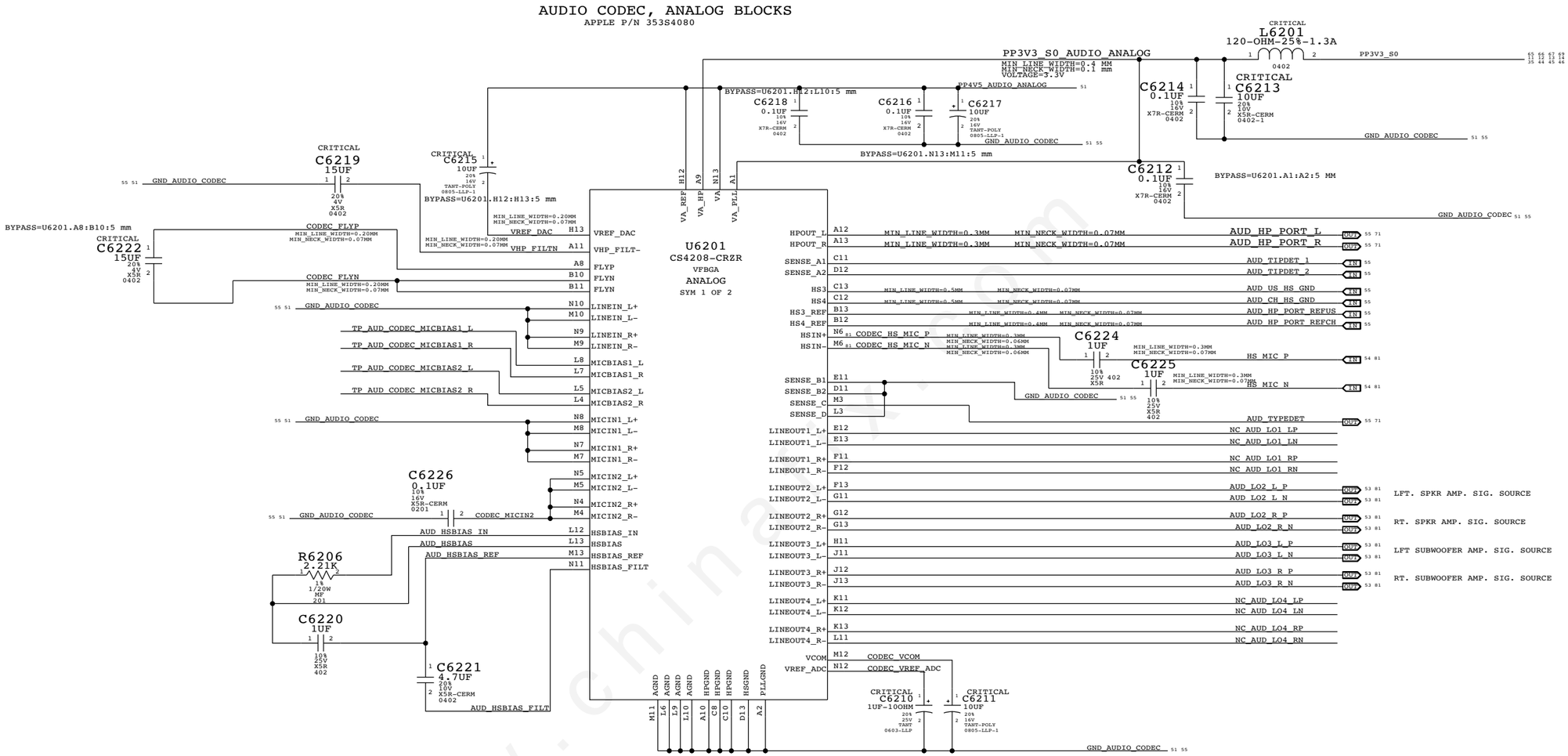
SHEET 50 OF 81

AUDIO CODEC, ANALOG BLOCKS

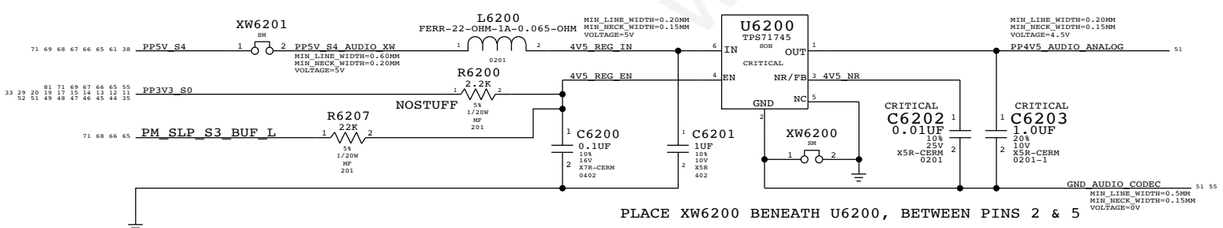
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC_MASTER=JOE_J45	SYNC DATE=07/30/2013
PAGE TITLE: AUDIO:CODEC, ANALOG	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 62 OF 118
	SHEET: 51 OF 81

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.065-OHM
0201

PP1V5_S0 → C6300 4.7UF 20% 4V X5R-1 402 → C6301 0.1UF 10% 16V X7R-CERM 0201 → PP1V5_S0_AUDIO_DIG
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.07MM
VOLTAGE=1.5V

BYPASS=U6201.J2:J1:5 mm

C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.E1:F1:5 mm

BYPASS=U6201.G1:F1:5 mm
C6303 0.1UF 10% 6.3V CERM-X5R 0201
C6304 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.K1:K3:5 mm
C6305 10UF 20% 10V X5R-CERM 0402-1

PP3V3_S0
C6306 10UF 20% 10V X5R-CERM 0402-1
C6307 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.A7:E3:5 mm

PP3V3_S0
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201

OMIT
R6302 SHORT 402

R6323 100K 5% 1/20W MF 201
PD_CS4208_GPIO1
NOSTUFF
R6322 100K 5% 1/20W MF 201

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

GPIO0_SPKR_SHUTDOWN	H3	GPIO0
SPKRCONN_L_ID	H2	GPIO1
SPKRCONN_R_ID	H1	GPIO2
DFET_OPENUS	C4	GPIO3
DFET_OPENCH	C5	GPIO4
	C7	GPIO5
NC_CS4208_GPO0	C9	GPO0
NC_CS4208_GPO1	B9	GPO1
HDA_BIT_CLK	F2	BCLK
HDA_SYNC	E2	SYNC
HDA_SDIN0	D1	SDI0
TP_CS4208_HDA_SDOUT1	C1	SDI1
HDA_SDOUT	D2	SDO0
	C2	SDO1
	C3	SDO2
HDA_RST_L	B1	SDO3
	D3	RST*
NC_CS4208_MCLKA	A5	MCLK_A
NC_CS4208_SCLKA	B2	SCLK_A
NC_CS4208_LRCLKA	B4	LRCK_A
NC_CS4208_SDOUTA	A3	SDOUT_A
	B3	SDIN_A
NC_CS4208_MCLKB	A6	MCLK_B
NC_CS4208_SCLKB	B6	SCLK_B
NC_CS4208_LRCLKB	B5	LRCK_B
NC_CS4208_SDOUTB	B8	SDOUT_B
	A4	SDIN_B
	C6	SDA
	B7	SCL

R6331 22 5% 1/20W MF 201
CS4208_HDA_SDOUT0_R

VD J2, VL_HD E1, VL_SP A7, VL_IF G1, VL_DM K1
DGND J1, LGND F1, LGND E3, LGND F3, LGND J3, LGND K3

SPDIF_IN	G3	CS4208_SPDIF_IN
SPDIF_OUT	G2	CS4208_SPDIF_OUT
DMIC_SDA0	N3	
DMIC_SCL0	N2	NC_DMIC_CLK0
DMIC_SDA1	N1	
DMIC_SCL1	M1	NC_DMIC_CLK1
DMIC_SDA2	M2	
DMIC_SCL2	L1	NC_DMIC_CLK2
DMIC_SDA3	K2	DMIC_SDA3
DMIC_SCL3	L2	DMIC_CLK3_R
NC	F6	
NC	F7	
NC	F8	
NC	G6	
NC	G7	
NC	G8	
NC	H6	
NC	H7	
NC	H8	

R6330 33 5% 1/16W MF-LF 402 → SPDIF_OUT_JACK
R6332 75 1% 1/16W MF-LF 402 → DMIC_CLK3

PP6301 P3MM SM
DMIC_SDA3
PLACE_NEAR=U6201.N3:5 mm

PP6302 P3MM SM
HDA_BIT_CLK
PLACE_NEAR=U6201.F2:5 mm

PP6303 P3MM SM
HDA_SYNC
PLACE_NEAR=U6201.E2:5 mm

PP6304 P3MM SM
HDA_SDOUT
PLACE_NEAR=U6201.D2:5 mm

PP6305 P3MM SM
CS4208_HDA_SDOUT0_R
PLACE_NEAR=U6201.D1:5 mm

SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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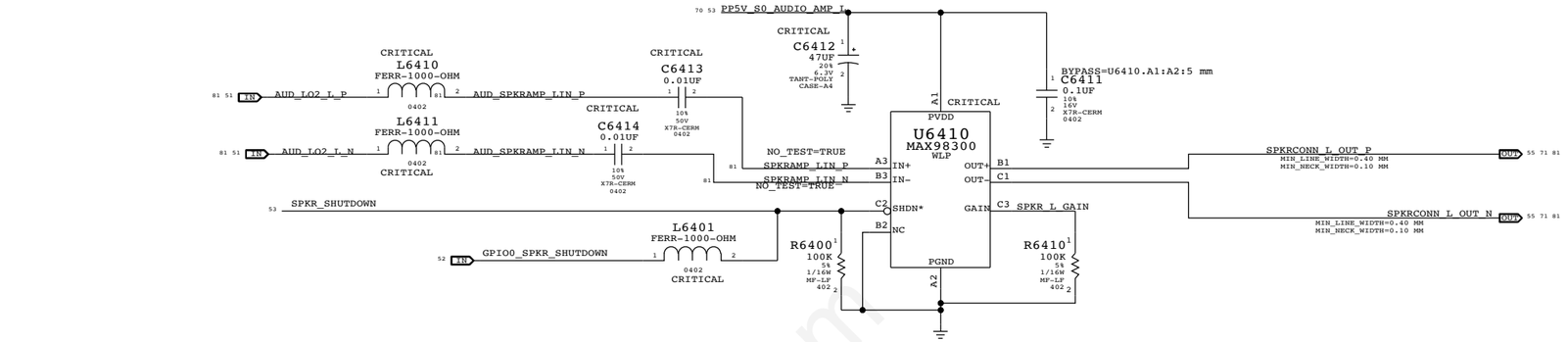
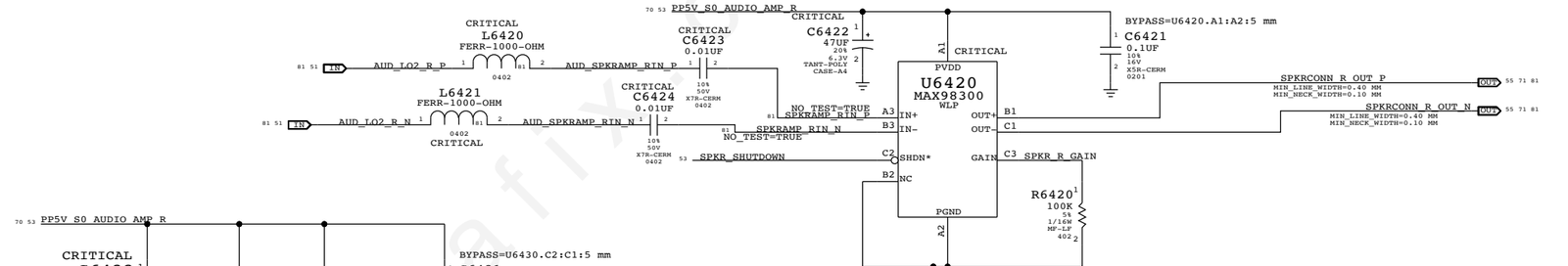
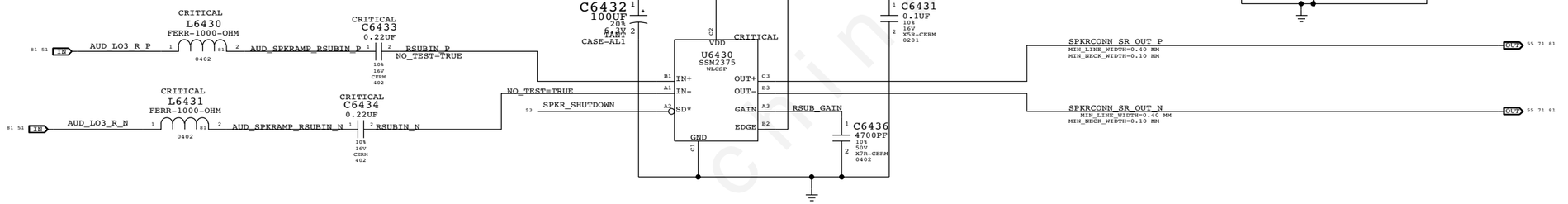
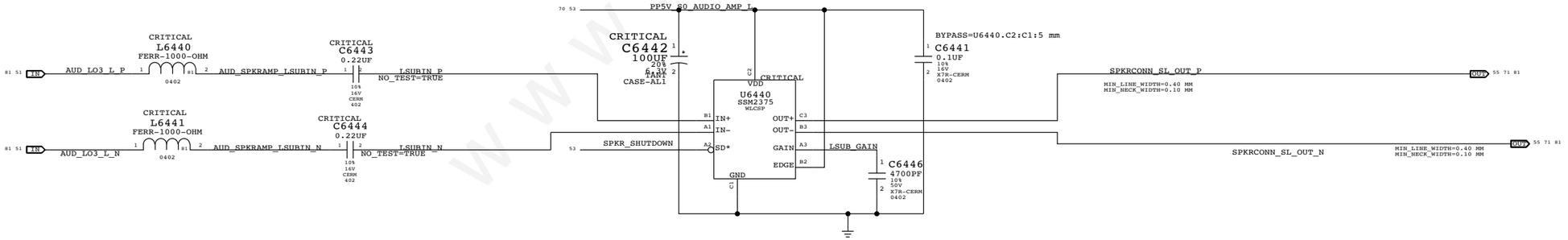
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=JOE J45 SYNC_DATE=07/30/2013

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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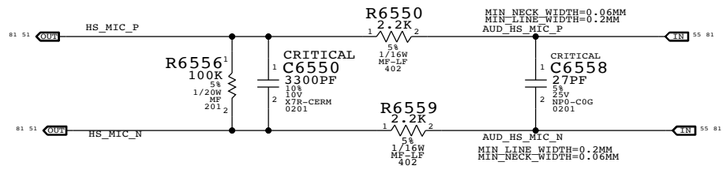

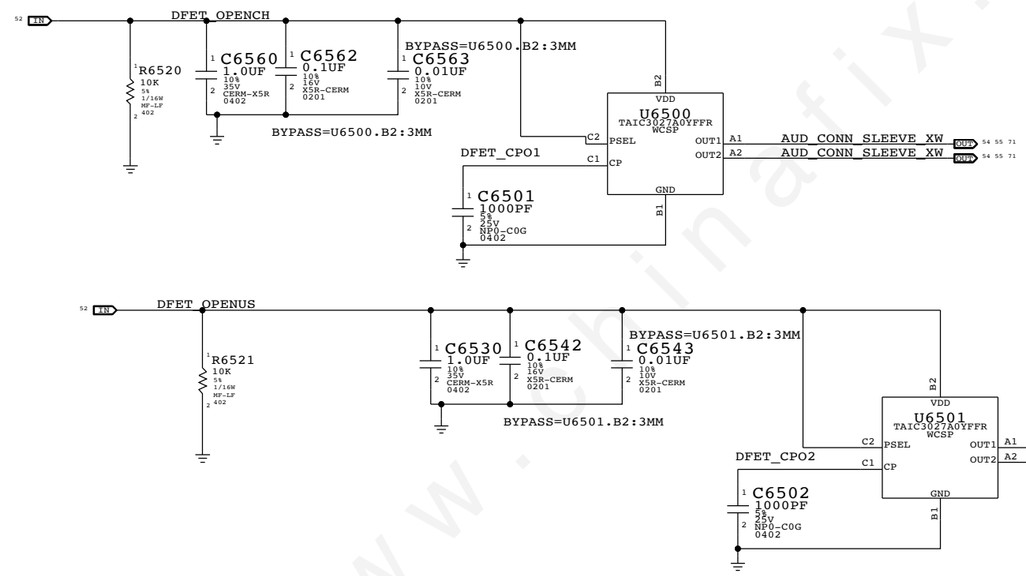

SYNC_MASTER=JOE J45 SYNC_DATE=07/30/2013

PAGE TITLE

AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM

J6603
78171-6006
M-RT-SM

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

AUDIO

OPERATING VOLTAGE 3.3
POF

SYNC MASTER=JOE J45	SYNC DATE=07/30/2013
PAGE TITLE	AUDIO: JACK TRANSLATORS
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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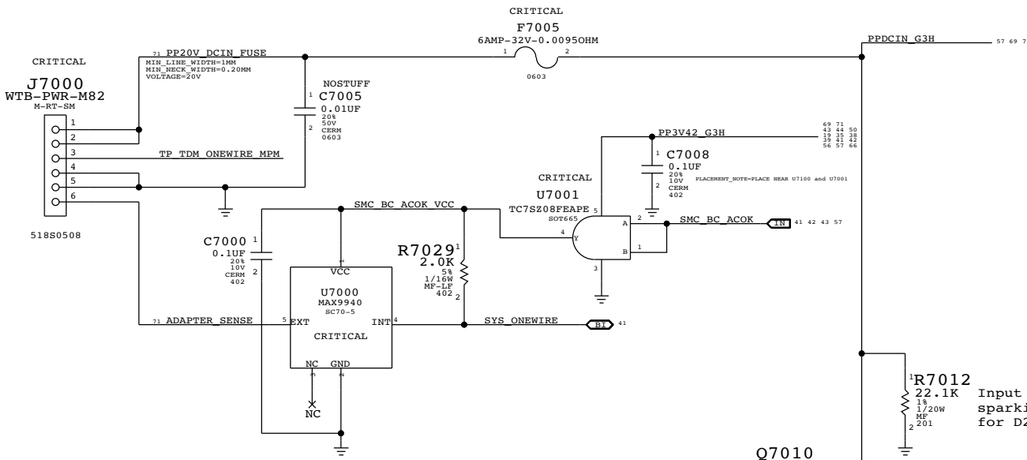
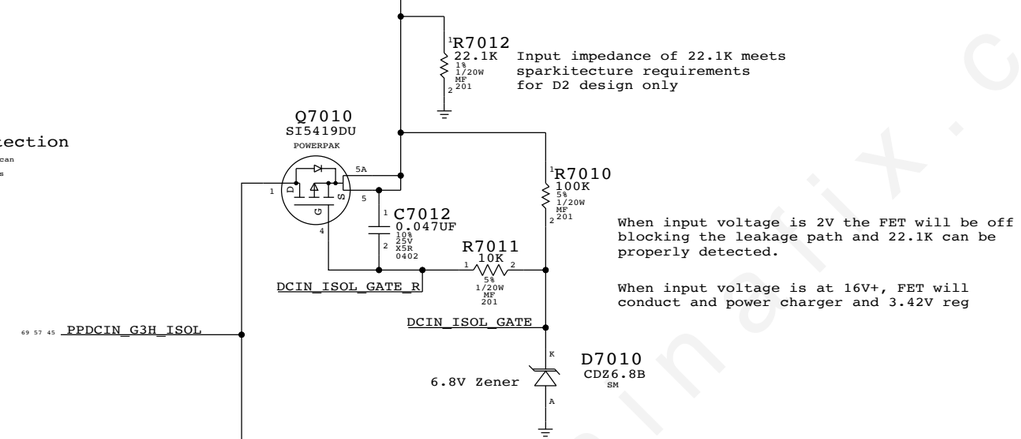
MagSafe DC Power Jack



1-Wire OverVoltage Protection

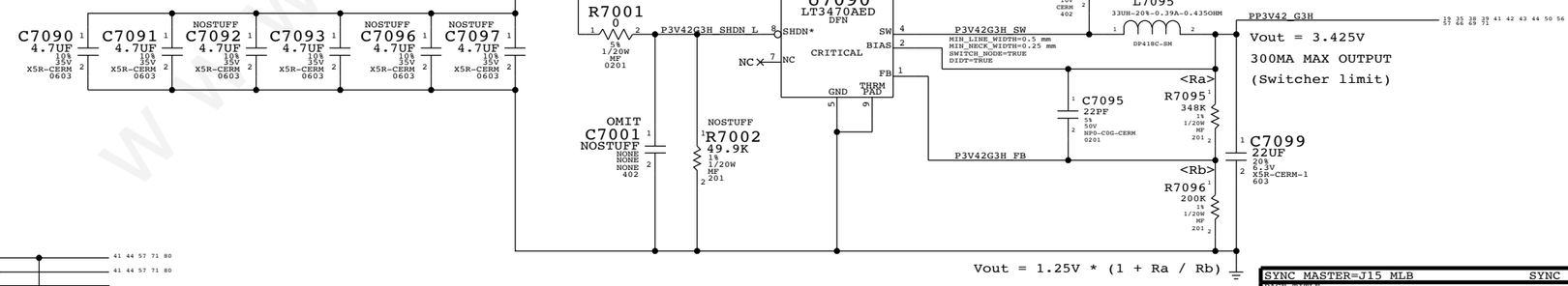
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.



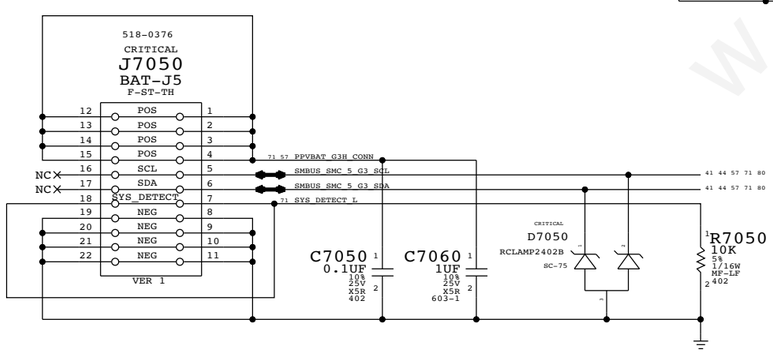
APN:353S3733

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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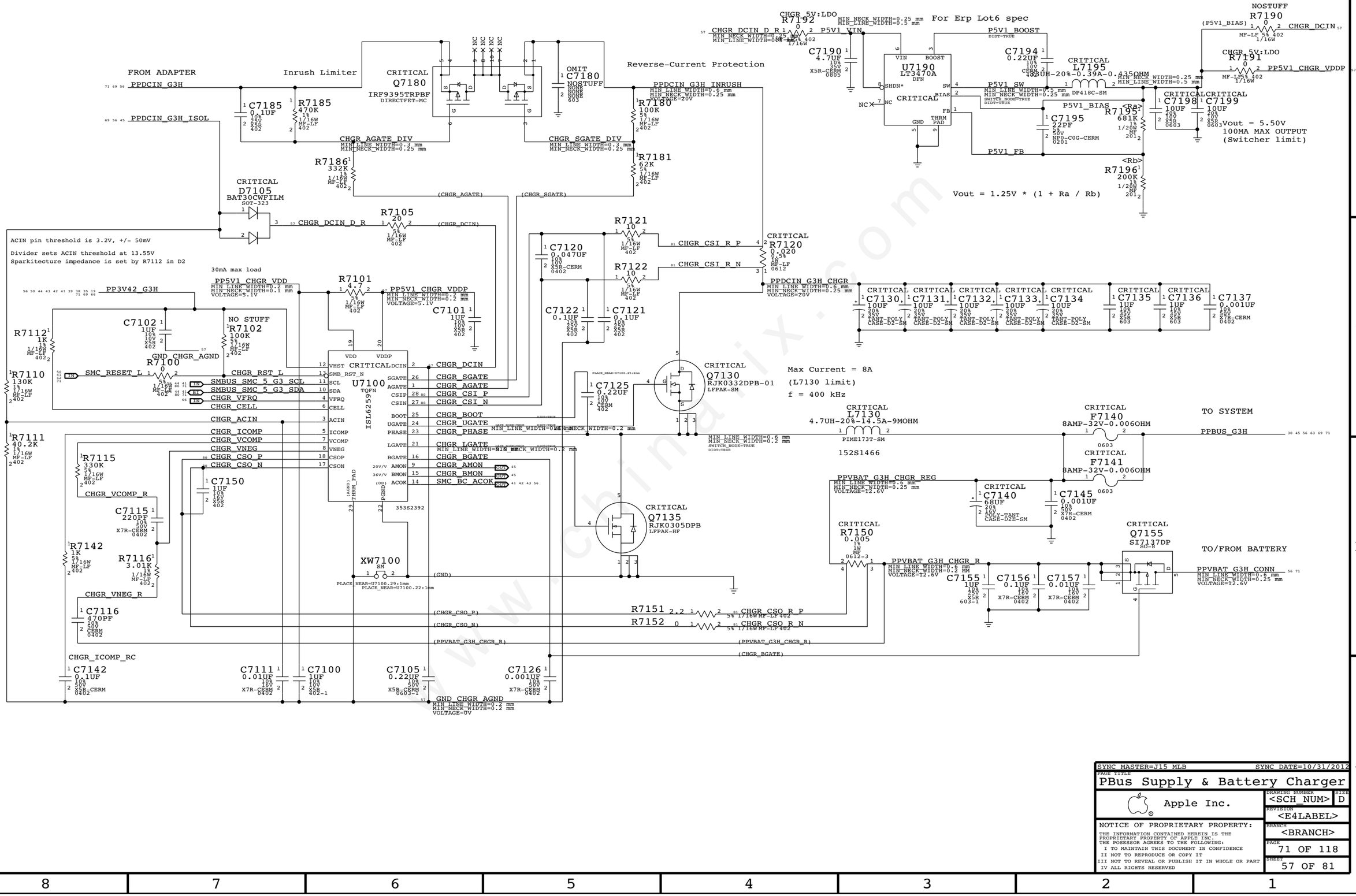
FROM ADAPTER
PPDCIN_G3H
PPDCIN_G3H_ISOL
Inrush Limiter
CRITICAL
Q7180
IRF9395TRPBF
DIRECTFET-MC
OMIT
C7180
NOSTUFF
Reverse-Current Protection
PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V
R7180
100K
R7185
470K
C7185
0.1UF
CHGR_AGATE_DIV
CHGR_SGATE_DIV
R7186
332K
R7181
62K
CRITICAL
D7105
BAT30CWFILM
SOT-323
CHGR_DCIN_D_R
R7105
20
(CHGR_DCIN)
(CHGR_AGATE)
(CHGR_SGATE)
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Sparkitecture impedance is set by R7112 in D2
30mA max load
PP3V42_G3H
PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=5.1V
R7101
4.7
PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V
C7101
1UF
R7112
1K
C7102
1UF
NO STUFF
R7102
100K
GND_CHGR_AGND
R7100
0
R7110
130K
SMC_RESET_L
CHGR_RST_L
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
CHGR_VFRQ
CHGR_CELL
R7111
40.2K
R7115
330K
CHGR_VCOMP_R
C7115
220PF
R7142
1K
R7116
3.01K
CHGR_VNEG_R
C7116
470PF
CHGR_ICOMP_RC
C7142
0.1UF
U7100
ISL6259
TQFN
VDD
VDDP
VHST
SMB_RST_N
SCL
SDA
VFRQ
CELL
ACIN
ICOMP
VCOMP
VNEG
CSOP
CSON
DCIN
SGATE
AGATE
CSIP
CSIN
BOOT
UGATE
PHASE
LGATE
BGATE
AMON
BMON
ACOK
THRM_PAD
PGND
CHGR_DCIN
CHGR_SGATE
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
SMC_BC_ACOK
353S2392
C7150
1UF
C7111
0.01UF
C7100
1UF
C7105
0.22UF
C7126
0.001UF
GND_CHGR_AGND
XW7100
SM
(GND)
R7121
10
R7122
10
CHGR_CSI_R_P
CHGR_CSI_R_N
C7120
0.047UF
C7122
0.1UF
C7121
0.1UF
CRITICAL
R7120
0.020
PPDCIN_G3H_CHGR
C7125
0.22UF
CRITICAL
Q7130
RJK0332DPB-01
LFPAK-SM
CRITICAL
Q7135
RJK0305DPB
LFPAK-HF
Max Current = 8A
(L7130 limit)
f = 400 kHz
CRITICAL
L7130
4.7UH-20%-14.5A-9MOHM
PIME173T-SM
152S1466
TO SYSTEM
PPBUS_G3H
CRITICAL
F7140
8AMP-32V-0.006OHM
CRITICAL
F7141
8AMP-32V-0.006OHM
PPVBAT_G3H_CHGR_REG
C7140
68UF
C7145
0.001UF
CRITICAL
R7150
0.005
PPVBAT_G3H_CHGR_R
C7155
1UF
C7156
0.1UF
C7157
0.01UF
CRITICAL
Q7155
SI7137DP
SO-8
TO/FROM BATTERY
PPVBAT_G3H_CONN
R7151
2.2
R7152
0
CHGR_CSO_R_P
CHGR_CSO_R_N
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
CHGR_5V:LDO
R7192
0
CHGR_DCIN_D_R
P5V1_VIN
C7190
4.7UF
U7190
LT3470A
DFN
VIN
BOOST
SHDN*
SW
BIAS
FB
THRM
GND
PAD
NC
P5V1_BOOST
DIDT=TRUE
C7194
0.22UF
CRITICAL
L7195
2.2UH-20%-0.39A-0.435OHM
P5V1_SW
SWITCH_NODE=TRUE
DP418C-SM
P5V1_BIAS
C7195
22PF
P5V1_FB
<Ra>
R7195
681K
<Rb>
R7196
200K
Vout = 1.25V * (1 + Ra / Rb)
NOSTUFF
R7190
0
(P5V1_BIAS)
CHGR_DCIN
CHGR_5V:LDO
R7191
0
PP5V1_CHGR_VDDP
CRITICAL
C7198
10UF
CRITICAL
C7199
10UF
Vout = 5.50V
100MA MAX OUTPUT
(Switcher limit)
For Erp Lot6 spec
C7130
C7131
C7132
C7133
C7134
C7135
C7136
C7137
0.001UF
10UF
1UF
0.1UF
0.01UF
TANT-POLY
CASE-D2-SM
CERM
X5R
X7R-CERM
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE_TITLE
PBus Supply & Battery Charger
Apple Inc.
DRAWING_NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
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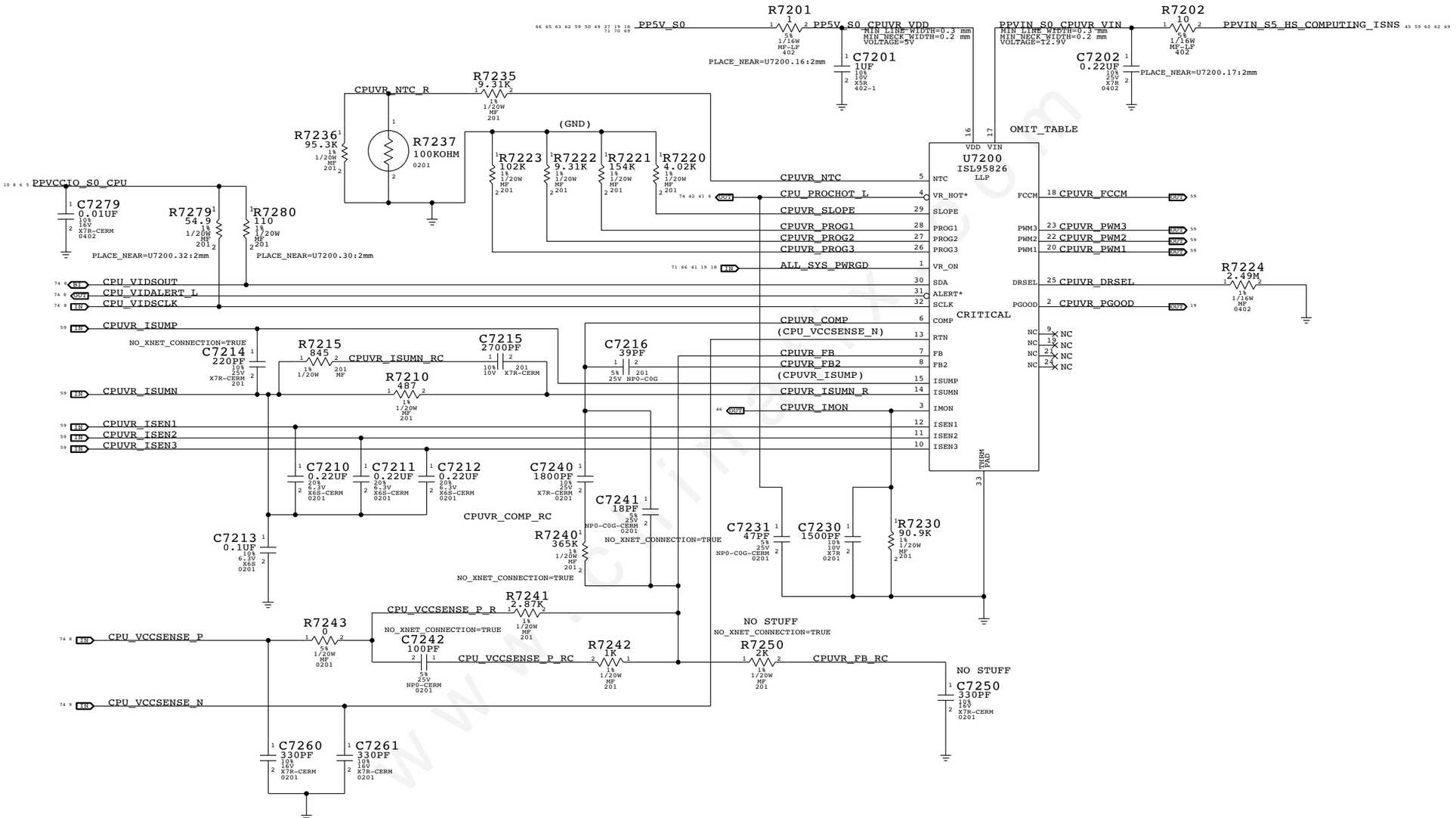
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE

CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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PPVIN_S5_HS_COMPUTING_ISNS
PP5V_S0
PHASE 1
U7310
FDMF6808N
PQFN
CRITICAL
353S3836
VDRV
BOOT
DISB*
GH
GL
PHASE
PWM
ZCD_EN*
THWN*
VCIN
NC
VIN
VSWH
CGND
PGND
C7310 1UF 10% 16V X6S-CERM 0402
C7311 0.22UF 10% 16V CERM 402
R7311 0 5% 1/16W MF-LF 402
CPUVR_BOOT1_RC
CPUVR_BOOT1
CPUVR_PHASE1_K
CPUVR_PWM1
CPUVR_FCCM
L7310 0.36UH-20%-36A-0.00108OHM
PIMS103T-SM 152S1538
CPUVR_PHASE1
PPVCC_S0_CPU_PH1
R7310 0.00075 1% 1W MF 0612
R7312 2.2 5% 1/10W MF-LF 603
C7312 0.001UF 10% 50V X7R-CERM 0402
CPUVR_PH1_SNUB
CPUVR_ISNS1_P
CPUVR_ISNS1_N
R7314 3.9 1% 1/20W MF 201
R7315 1K 1% 1/20W MF 201
R7316 10K 1% 1/20W MF 201
CPUVR_ISUMN
CPUVR_ISEN1
CPUVR_ISUMP
NO_XNET_CONNECTION=TRUE
R7317 10K 1% 1/20W MF 201
R7318 10K 1% 1/20W MF 201
CPUVR_ISNS2_N
CPUVR_ISNS3_N
C7313 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7314 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7315 10UF 20% 16V X6S-CERM 0603
C7316 10UF 20% 16V X6S-CERM 0603
C7317 1UF 10% 16V X6S-CERM 0402
C7318 0.001UF 10% 50V X7R-CERM 0402
C7319 0.001UF 10% 50V X7R-CERM 0402
THESE TWO CAPS ARE FOR EMC
Additonal Input Bulk Caps
C7370 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7371 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7372 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7373 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7374 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7375 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7376 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7377 15UF 20% 16V TANT SM
C7378 15UF 20% 16V TANT SM
C7379 15UF 20% 16V TANT SM
C7380 15UF 20% 16V TANT SM
C7381 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7382 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7383 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7384 68UF 20% 16V POLY-TANT CASE-D2E-SM
PHASE 2
C7320 1UF 10% 16V X6S-CERM 0402
C7321 0.22UF 10% 16V CERM 402
R7321 0 5% 1/16W MF-LF 402
CPUVR_BOOT2_RC
CPUVR_BOOT2
CPUVR_PHASE2_K
CPUVR_PWM2
CPUVR_FCCM
L7320 0.36UH-20%-36A-0.00108OHM
PIMS103T-SM 152S1538
CPUVR_PHASE2
PPVCC_S0_CPU_PH2
R7320 0.00075 1% 1W MF 0612
R7322 2.2 5% 1/10W MF-LF 603
C7322 0.001UF 10% 50V X7R-CERM 0402
CPUVR_PH2_SNUB
CPUVR_ISNS2_P
CPUVR_ISNS2_N
R7324 3.9 1% 1/20W MF 201
R7325 1K 1% 1/20W MF 201
R7326 10K 1% 1/20W MF 201
CPUVR_ISUMN
CPUVR_ISEN2
CPUVR_ISUMP
NO_XNET_CONNECTION=TRUE
R7327 10K 1% 1/20W MF 201
R7328 10K 1% 1/20W MF 201
CPUVR_ISNS1_N
CPUVR_ISNS3_N
C7323 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7324 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7325 10UF 20% 16V X6S-CERM 0603
C7326 10UF 20% 16V X6S-CERM 0603
C7327 1UF 10% 16V X6S-CERM 0402
C7328 0.001UF 10% 50V X7R-CERM 0402
C7329 0.001UF 10% 50V X7R-CERM 0402
PHASE 3
C7330 1UF 10% 16V X6S-CERM 0402
C7331 0.22UF 10% 16V CERM 402
R7331 0 5% 1/16W MF-LF 402
CPUVR_BOOT3_RC
CPUVR_BOOT3
CPUVR_PHASE3_K
CPUVR_PWM3
CPUVR_FCCM
L7330 0.36UH-20%-36A-0.00108OHM
PIMS103T-SM 152S1538
CPUVR_PHASE3
PPVCC_S0_CPU_PH3
R7330 0.00075 1% 1W MF 0612
R7332 2.2 5% 1/10W MF-LF 603
C7332 0.001UF 10% 50V X7R-CERM 0402
CPUVR_PH3_SNUB
CPUVR_ISNS3_P
CPUVR_ISNS3_N
R7334 3.9 1% 1/20W MF 201
R7335 1K 1% 1/20W MF 201
R7336 10K 1% 1/20W MF 201
CPUVR_ISUMN
CPUVR_ISEN3
CPUVR_ISUMP
NO_XNET_CONNECTION=TRUE
R7337 10K 1% 1/20W MF 201
R7338 10K 1% 1/20W MF 201
CPUVR_ISNS1_N
CPUVR_ISNS2_N
C7333 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7334 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7335 10UF 20% 16V X6S-CERM 0603
C7336 10UF 20% 16V X6S-CERM 0603
C7337 1UF 10% 16V X6S-CERM 0402
C7338 0.001UF 10% 50V X7R-CERM 0402
C7339 0.001UF 10% 50V X7R-CERM 0402
PPVCC_S0_CPU
Vout = 1.85V max
95A max output
f = 450 kHz
SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012
PAGE TITLE
CPU VR12.5 VCC Power Stage
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 59 OF 81
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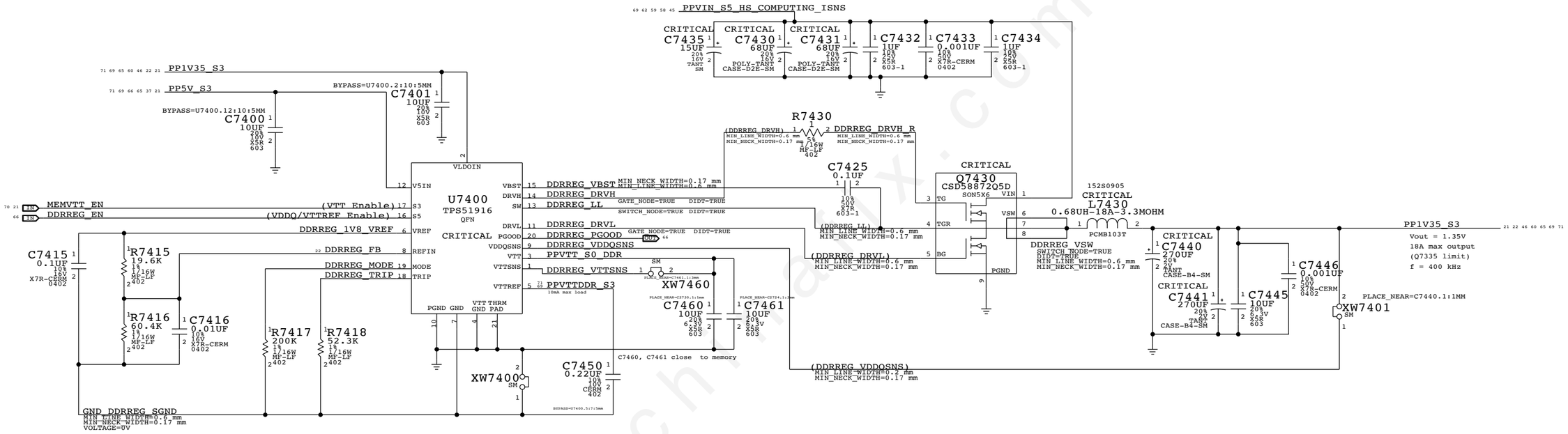
DDR3L (1V35 S3) REGULATOR



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE
1.35V DDR3L SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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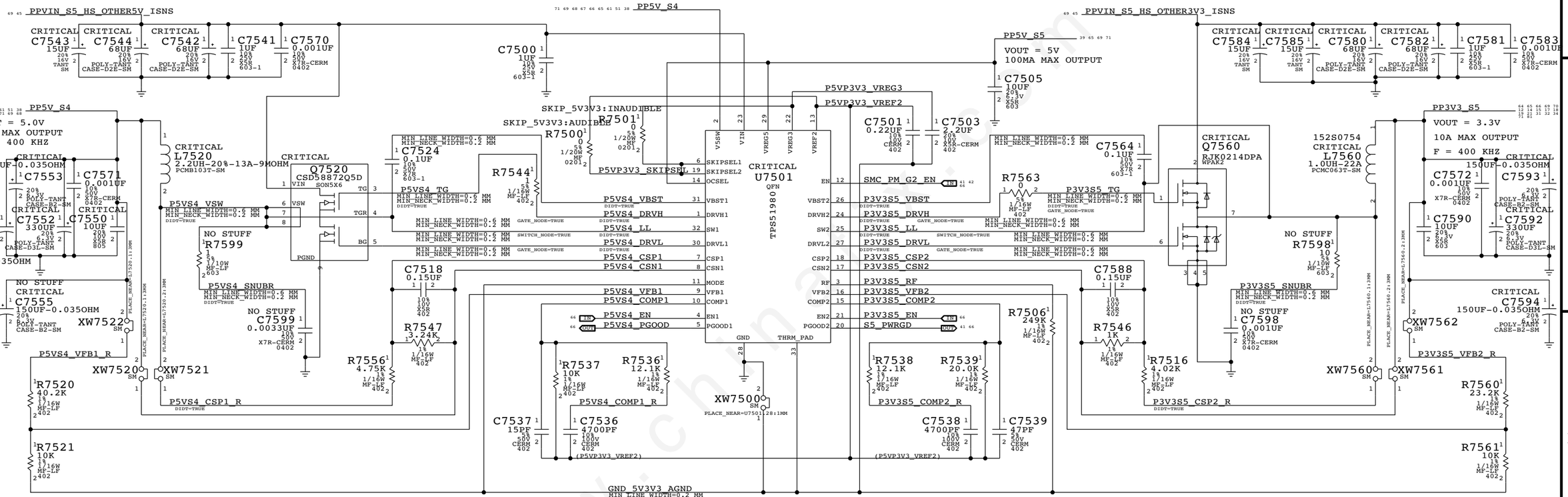

SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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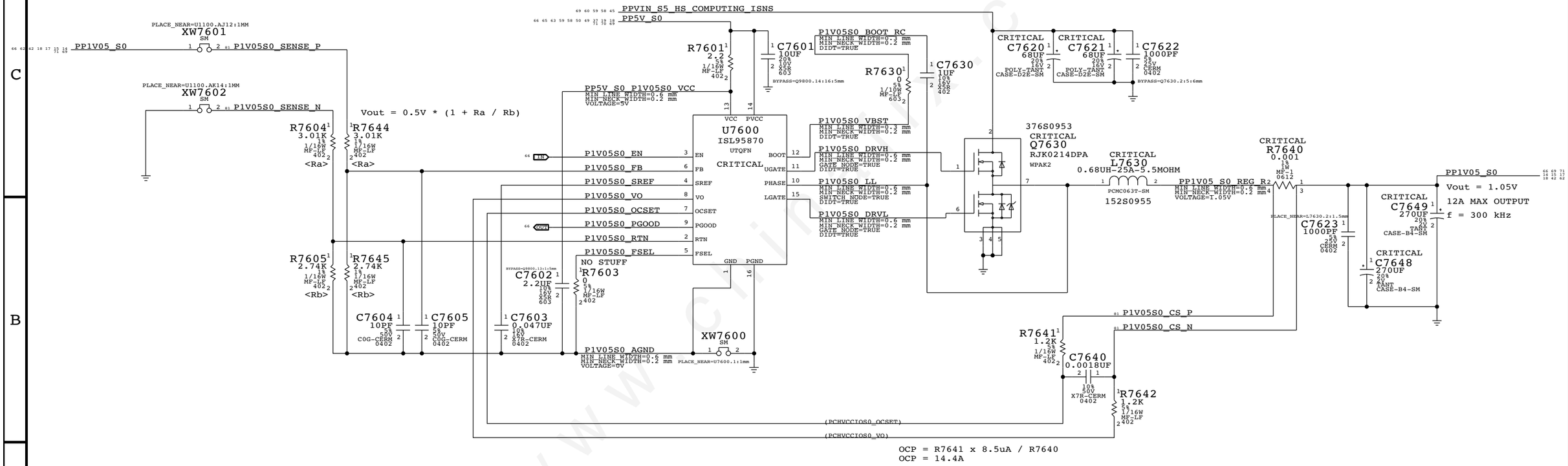
1V05 S0 REGULATOR



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE
1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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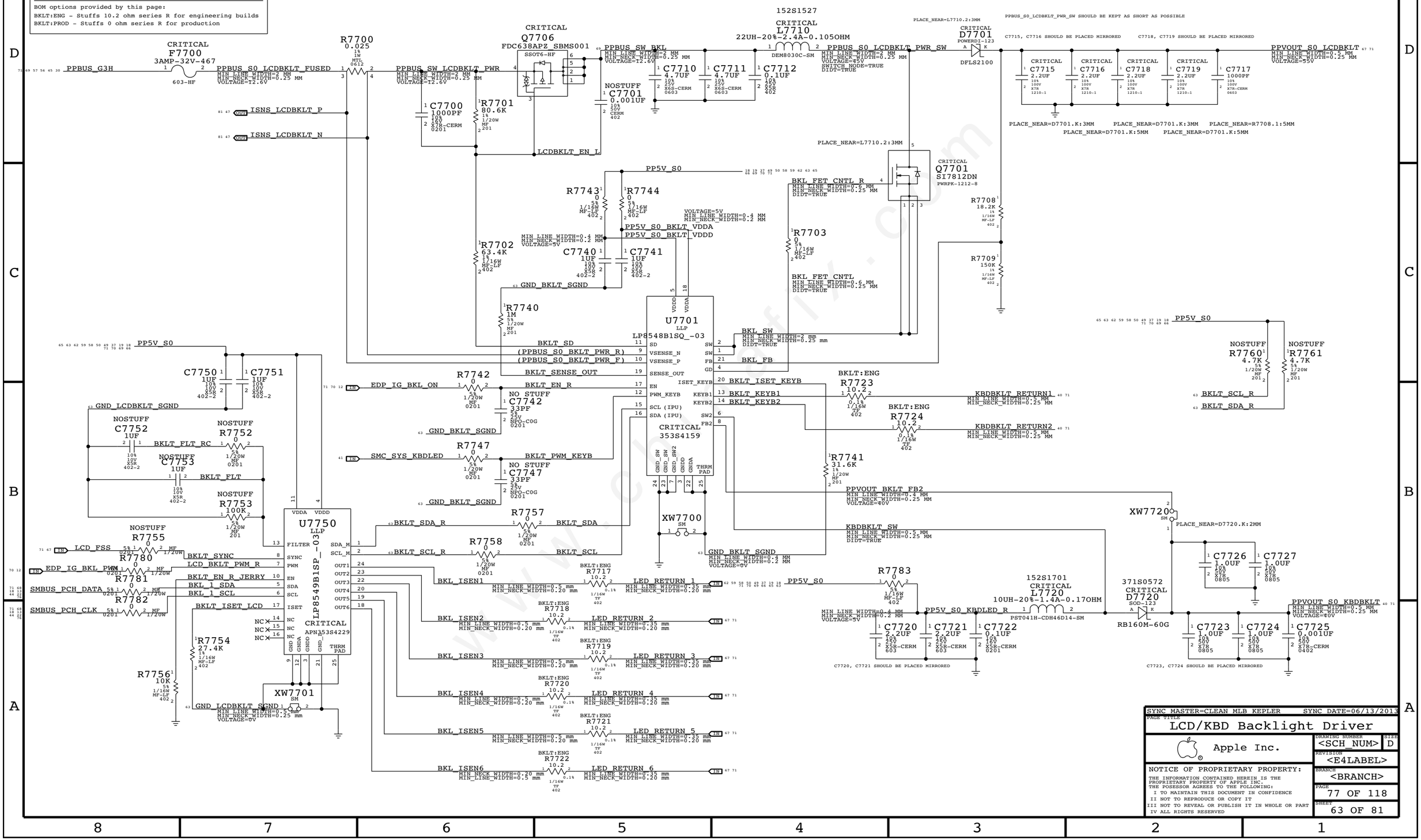
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD



SYNC MASTER=CLEAN_MLB_KEPLER SYNC DATE=06/13/2013

PAGE TITLE
LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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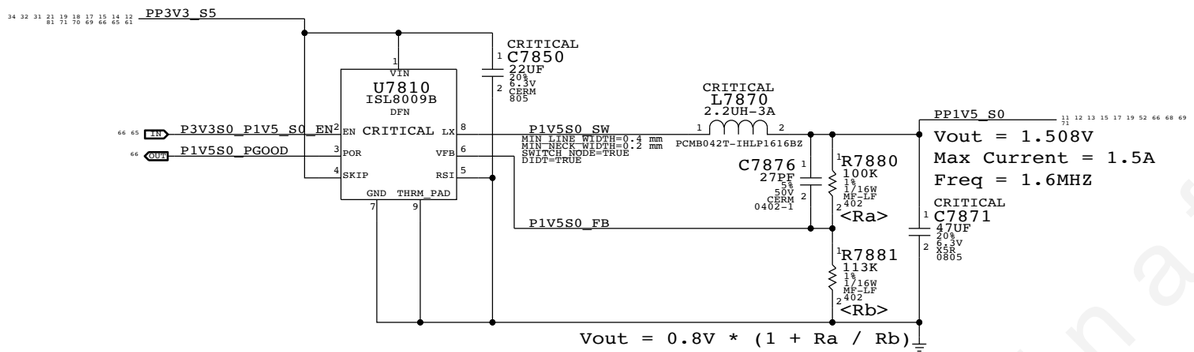
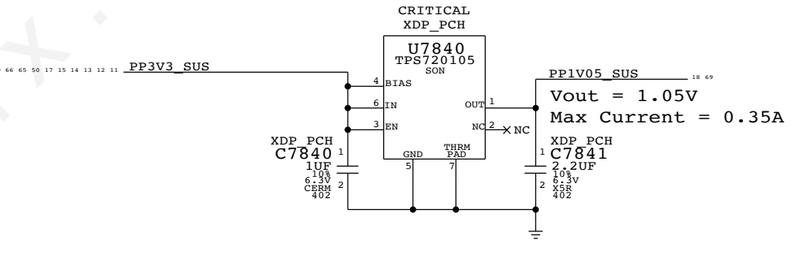
1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC MASTER=J15 MLB SYNC DATE=10/31/2012

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per J45 Power Budget rev5

PP3V3_S5 → Q8002 DMN5L06VK-7 SOT-563 → PP3V3_S4

R8002 220K 5% 1/16W MF-LF 402
C8009 0.033UF 10% 16V X5R 402
R8000 47K 5% 1/16W MF-LF 402
C8000 0.01UF 10% 16V X7R-CERM 0402

EN: R4_PWR_EN
P3V3S4_EN_L
P3V3S3_S4

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70-6L

PP3V3_S5 → Q8012 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 → PP3V3_S3

R8012 47K 5% 1/16W MF-LF 402
C8011 0.033UF 10% 16V X5R 402
R8010 39K 5% 1/16W MF-LF 402
C8010 0.01UF 10% 16V X7R-CERM 0402

EN: P3V3S3_EN
P3V3S3_EN_L
P3V3S3_SS

SSD_PWR_EN:GPIO
SSD_PWR_EN → R8073 0 0201 1/20W 5% MF → SSD_PWR_EN:SOI
R8074 0 0201 1/20W 5% MF
PM_SLP_S3_BUF_L
SSD_PWR_FET_EN

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70-6L

PP5V_S4 → Q8052 DMN5L06VK-7 SOT-563 → PP5V_S3

R8052 200K 5% 1/16W MF-LF 402
C8051 0.033UF 10% 16V X5R 402
R8050 5.1K 5% 1/16W MF-LF 402
C8050 0.01UF 10% 16V X7R-CERM 0402

EN: P5VS3_EN
P5VS3_EN_L
P5VS3_SS

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5
C8001 0.1UF 20% 10V CERM 402
U8001 SLG5AP1438V TDFN CRITICAL
VDD, CAP, ON, GND, D, S
P1V35CPU_SLEW_CTL
CPUVDDQ_EN
C8002 0.018UF 10% 16V X7R 402
Slew rate : 0.8V/ms = 19.75nF

PP1V35_S3

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R
XW8005 SM
PP1V35_S3RS0_FET → PP1V35_S3RS0_CPUDDR
NC_ISNS_CPUDDRN
NC_ISNS_CPUDDRP

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70-6L

PP3V3_S5 → Q8002 DMN5L06VK-7 SOT-563 → PP3V3_SUS

R8022 100K 5% 1/16W MF-LF 402
C8021 0.033UF 10% 16V X5R 402
R8020 12K 5% 1/16W MF-LF 402
C8020 0.01UF 10% 16V X7R-CERM 0402

EN: PM_SLP_SUS_L
P3V3SUS_EN
P3V3SUS_SS

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm
CRITICAL
Q8070
SI7615DN
PWRPK-1212-8

PP3V3_S5 → Q8072 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2 → PP3V3_S0SW_SSD_R

R8072 47K 5% 1/16W MF-LF 402
C8071 0.033UF 10% 16V X5R 402
R8070 33K 5% 1/16W MF-LF 402
C8070 0.01UF 10% 16V X7R-CERM 0402

P3V3_SSD_EN_L
P3V3_SSD_SS

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK-1212-8

PP5V_S4 → PP5V_S0

R8062 270K 5% 1/16W MF-LF 402
C8061 0.12UF 10% 10.0V CERM-X5R 402
R8060 6.2K 5% 1/16W MF-LF 402
C8060 0.47UF 10% 10V X5R 0402

P5V0S0_EN_L
P5V0S0_SS

Q8052 DMN5L06VK-7 SOT-563
EN: P5VS0_EN

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 Switch

APN 353S2741

U8030
TPS22924
CSP
A2, B2, VIN, VOUT, A1, B1, C2, ON, GND
CRITICAL

PP3V3_S5 → PP3V3_S0
P3V3S0_P1V5_S0_EN
C8030 1UF 10% 6.3V X5R 402

Max Current = 2A

U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC MASTER=J15 MLB
SYNC DATE=10/31/2012
PAGE TITLE: Power FETs
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 80 OF 118
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Power State Debug LEDs
(For development only)

PP3V3_S5 → DBGLED PLACE_SIDE=BOTTOM R8194 0 5% 1/16W MF-LF 402 (PP3V3_S5_DBGLED MIN_NECK_WIDTH=0.2 MM, MIN_LINE_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0
R8190 20K 5% 1/20W MF 201	R8191 20K 5% 1/20W MF 201	R8192 20K 5% 1/20W MF 201	R8193 20K 5% 1/20W MF 201
D8190 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S5_ON	D8191 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S4_ON	D8192 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S3_ON	D8193 GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S0_ON
DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0_D	
Q8190 DMN5L06VK-7 SOT-563	Q8190 DMN5L06VK-7 SOT-563	Q8191 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2	

S4_PWR_EN, PM_SLP_S4_L, PM_SLP_S3_BUF_L

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

PP3V3_S5 → C8170 0.1uF 20% 10V CERM 402 (BYPASS=U8170.6:3:2.3mm; PM_SLP_S5_L:100K pull down on PCH page)

PM_SLP_S5_L, SMC_S4_WAKESRC_EN → U8170 74LVC1G32 SOT891 → S4_PWR_EN (MAKE_BASE=TRUE)

S4_PWR_EN → D8174 BAT54XV2T1 SOD-523; R8174 43K 5% 1/16W MF-LF 402 (PLACE_NEAR=R8174.1:6mm); P5VS4_EN_D → R8175 240 5% 1/16W MF-LF 402; C8174 2.2UF 10% 6.3V X5R 402 (PLACE_NEAR=Q7501.4:6mm)

S4_PWR_EN → P5VS4_EN (MAKE_BASE=TRUE)

S4_PWR_EN (OUT) ×3

S3 ENABLE

PM_SLP_S4_L (IN) (PM_SLP_S4_L:100K pull down in PCH page)

R8111 5.1K 5% 1/16W MF-LF 402	R8112 0 5% 1/16W MF-LF 402	R8113 0 5% 1/16W MF-LF 402	R8114 3.3K 5% 1/20W MF 201
C8110 0.47UF 10% 6.3V CERM-X5R 402	C8112 0.47UF 10% 6.3V CERM-X5R 402	C8113 0.47UF 10% 6.3V CERM-X5R 402	NO STUFF C8114 0.47UF 10% 6.3V CERM-X5R 402

TPAD_VBUS_EN (OUT 39)

P5VS3_EN — P5VS3_EN (MAKE_BASE=TRUE) (OUT 65 66)

P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE) (OUT 65 66)

DDRREG_EN — DDRREG_EN (MAKE_BASE=TRUE) (OUT 60 66)

S0 ENABLE

PP3V3_S5 → C8180 0.1uF 20% 10V CERM 402 (BYPASS=U8180.5:3:2.3mm)

PM_SLP_S3_L (IN) → R8178 100 5% 1/16W MF-LF 402 → PM_SLP_S3_R_L (MAKE_BASE=TRUE) (PM_SLP_S3_L:100K pull down in PCH page)

U8180 NC7SZ08 SC70-HF

(PM_SLP_S3_BUF_L) → NO STUFF R8180 100K 5% 1/16W MF-LF 402 → D8185 BAT54XV2T1 SOD-523

R8185 130K 5% 1/16W MF-LF 402 (PLACE_NEAR=U7600.3:6mm)	R8186 20K 5% 1/16W MF-LF 402 (MAKE_BASE=TRUE)	R8187 0 5% 1/16W MF-LF 402 (PLACE_NEAR=Q8052.5:6mm)
C8185 0.82UF 10% 6.3V X5R 402 (PLACE_NEAR=U7600.3:6mm)	C8186 0.68UF 10% 6.3V CERM 402	C8187 0.68UF 10% 6.3V CERM 402 NO STUFF

PM_SLP_S3_BUF_L (OUT 51 65 66 68 71)

P1V05_EN_D → R8138 820 5% 1/16W MF-LF 402 (PLACE_NEAR=R8138.1:6mm)

P1V05S0_EN (MAKE_BASE=TRUE) (OUT 62 66)

P5VS0_EN — P5VS0_EN (MAKE_BASE=TRUE) (OUT 65 66)

P3V3S0_P1V5_S0_EN — P3V3S0_P1V5_S0_EN (MAKE_BASE=TRUE) (OUT 64 65 66)

P1V05S0_EN — P1V05S0_EN (OUT 62 66)

PM_SLP_S3_R_L (OUT 31 32 45 66) ×2

CPUVCORE ENABLE

ALL_SYS_PWRGD — ALL_SYS_PWRGD (MAKE_BASE=TRUE) (OUT 18 19 41 58 66 71)

3.3V SUS Enable

PM_SLP_SUS_L (IN) — PM_SLP_SUS_L (MAKE_BASE=TRUE) (OUT 12 45 65 66)

PM_SLP_SUS_L: 100K pull down on PCH page

PP5V_S0 → R8151 54.9K 1% 1/16W MF-LF 402 → VMON_5V_DIV (5.0V Divider:1.07V) → R8152 15.0K 1% 1/16W MF-LF 402

PP3V3_S5 → R8156 150K 1% 1/16W MF-LF 402 → S0PGD_C

ALL_SYS_PWRGD (18 19 41 58 66 71)

R8153 1K 5% 1/16W MF-LF 402 (VMON_Q2_BASE)

R8154 1K 5% 1/16W MF-LF 402 (NC, VMON_Q3_BASE)

R8155 1K 5% 1/16W MF-LF 402 (NC, VMON_Q4_BASE)

Q8150 ASMCC0179 DFN2015H4-8 353S2809 (Q1, Q2, Q3 CRITICAL, Q4)

S0PGD_BJT_GND_R

PP3V3_S0 → R8158 15.0K 1% 1/16W MF-LF 402 → VMON_3V3_DIV (3V3 Divider:1.07V) → R8159 7.15K 1% 1/16W MF-LF 402

Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA

3.3V SUS Detect

PP3V3_S5 → C8130 0.1uF 20% 10V CERM 402 (BYPASS=U8130.6:2:2.3mm)

PP3V3_SUS → R8133 100K 5% 1/16W MF-LF 402

U8130 TPS3808G33DBVRG4 SOT23-6 (CRITICAL; No stuff C8131, 12ms Min delay time; U8130 Sense input threhold is 3.07V)

SENSE ← PP3V3_SUS; RESET* → PM_RSMRST_L (OUT 12 71 76) → PM_RSMRST_L goes to U1100.C21

CT ← SUS_PGOOD_CT; MR* ← TP_SUS_PGOOD_MR_L; GND

NO STUFF C8131 0.001UF 20% 50V CERM 402

S5 Rail Enables & PGOOD

SMC_PM_G2_EN (IN) — SMC_PM_G2_EN (MAKE_BASE=TRUE) → R8140 100 5% 1/16W MF-LF 402 (PLACE_NEAR=U7501.21:7mm)

P3V3S5_EN — P3V3S5_EN (MAKE_BASE=TRUE) (OUT 61 66)

SMC_PM_G2_EN (OUT 42 66)

NO STUFF C8142 0.0033UF 10% 50V X7R-CERM 402 (PLACE_NEAR=U7501.21:7mm)

PP3V42_G3H (PLACE_NEAR=U7501.20:7mm) → R8141 100K 5% 1/16W MF-LF 402

S5_PWRGD --> SMC
SMC --> PM_DSW_PWRGD

S5_PWRGD — S5_PWRGD (MAKE_BASE=TRUE) (OUT 66 41)

S0 Rail PGOOD (BJT Version)

VMON_5V_DIV (5.0V Divider:1.07V)

VMON_Q2_BASE, VMON_Q3_BASE, VMON_Q4_BASE

VMON_3V3_DIV (3V3 Divider:1.07V)

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.015V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

keep R8171 DDRCPU 1.35V only

PP3V3_S0 → R8195 10 5% 1/16W MF-LF 402 (S0PGOOD_ISL MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V) → PP3V3_S0_VMON_P2

PP3V3_S0_VMON_P7 → R8196 10 5% 1/16W MF-LF 402 (MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V) → PP3V3_S0

C8162 0.1UF 20% 10V X7R-CERM 0402	C8160 0.1UF 20% 10V X7R-CERM 0402	C8161 0.1UF 20% 10V X7R-CERM 0402
C8163 0.1UF 20% 10V X7R-CERM 0402	NOSTUFF R8197 100K 5% 1/16W MF-LF 402	

PP5V_S0 → R8160 6.04K 1% 1/16W MF-LF 402 (P5V_VMON divider 3.16V @4.5V)

PP1V35_S3RS0_CPUDDR → R8161 15.0K 1% 1/16W MF-LF 402 (1V35_VMON divider 0.71V @1.31V)

PP1V05_S0 → R8170 10K 1% 1/16W MF-LF 402; R8172 6.04K 1% 1/16W MF-LF 402; R8171 12.4K 1% 1/16W MF-LF 402; R8173 15.0K 1% 1/16W MF-LF 402 (1V05_VMON divider 0.716V @1.02V)

U8160 ISL88042IRTEZ TDFN (2PU CRITICAL) 353S2310
VDD, V2MON, V3MON, V4MON, GND, THRM_PAD, MR* ← VMON_MR, RST* → S0PGOOD_ISL

S0PGOOD_ISL → R8162 330 5% 1/16W MF-LF 402 → ALL_SYS_PWRGD_R → ALL_SYS_PWRGD

VMON_MR (66)

1V5 S0 "PGOOD" Delay

PM_SLP_S3_BUF_L → R8167 10K 5% 1/16W MF-LF 402 → R8168 100 5% 1/16W MF-LF 402 → P1V5S0_PGOOD (64)

P1V05S0_PGOOD (62) → R8169 100 5% 1/16W MF-LF 402 → PP1V5_S0 (OUT 18 19 41 58 66 71)

R8137 100 5% 1/16W MF-LF 402 (DELAY_1V5S0_PGD_1 → 2 ALL_SYS_PWRGD (OUT 18 19 41 58 66 71))

PP3V3_S5 → R8136 23.7K 1% 1/16W MF-LF 402 → PM_1V5_PGD_I

C8134 2.2UF 10% 6.3V X5R 402

R8139 2.0K 1% 1/16W MF-LF 402 → PM_1V5_PGD_L_R

CRITICAL Q8151 DMB53D0UV SOT-563 (Vgs:0.7V~1.0V)

PM_1V5_PGD_L_R → R8135 54.9K 1% 1/16W MF-LF 402 → PM_1V5_PGD_DIV

R8134 61.9K 1% 1/16W MF-LF 402

CRITICAL Q8151 DMB53D0UV SOT-563 (VBEon: 0.58~0.7V; 1V5 Divider:0.75~0.85V)

PM_SLP_S3_R_L

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency

PP3V42_G3H → R8131 100K 5% 1/16W MF-LF 402 → CHGR_VFRQ (OUT 57)

Unused PGOOD signals

Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

PP5V_S3 → R8120 470K 5% 1/20W MF 201 → PP5V_S4

R8165 470K 5% 1/16W MF-LF 402

DDRREG_PGOOD (60)

P5VS4_PGOOD (61)

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

PP3V3_S4 → R8125 330K 5% 1/20W MF 201 → PM_WLAN_EN (IN) — PM_WLAN_EN (MAKE_BASE=TRUE) (OUT 34 41 66)

SYNC_MASTER=CHANG J45	SYNC_DATE=03/15/2013
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LCD PANEL INTERFACE (eDP)

C8350 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8351 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8352 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8353 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8354 9.1PF ±/-0.1PF C0G-CERM 0201 50V
C8355 9.1PF ±/-0.1PF C0G-CERM 0201 50V

71 63 LED_RETURN_6
71 63 LED_RETURN_5
71 63 LED_RETURN_4
71 63 LED_RETURN_3
71 63 LED_RETURN_2
71 63 LED_RETURN_1

CRITICAL
J8300
20525-130E-01
F-RT-SM

71 63 PPVOUT_S0_LCDBKLT
NC

20 OUT LCD_HPD
R8300 0 5% 1/20W MF 0201
71 67 LCD_HPD_CONN
71 63 OUT LCD_FSS

74 70 5 IN DP_INT_AUXCH_C_P C8328 0.1UF 10% 16V X5R-CERM 0201
74 71 67 DP_INT_AUX_P
74 70 5 IN DP_INT_AUXCH_C_N C8329 0.1UF 10% 16V X5R-CERM 0201
74 71 67 DP_INT_AUX_N

74 70 5 IN DP_INT_ML_C_P<0> C8320 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_P<0>
150OHM-100MA-8.5GHZ DLP0NS
CRITICAL FL8300
74 71 67 DP_INT_ML_P<0>

74 70 5 IN DP_INT_ML_C_N<0> C8321 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_N<0>
74 71 67 DP_INT_ML_N<0>

74 70 5 IN DP_INT_ML_C_P<1> C8322 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_P<1>
150OHM-100MA-8.5GHZ DLP0NS
CRITICAL FL8301
74 71 67 DP_INT_ML_P<1>

74 70 5 IN DP_INT_ML_C_N<1> C8323 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_N<1>
74 71 67 DP_INT_ML_N<1>

74 70 5 IN DP_INT_ML_C_P<2> C8324 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_P<2>
150OHM-100MA-8.5GHZ DLP0NS
CRITICAL FL8302
74 71 67 DP_INT_ML_P<2>

74 70 5 IN DP_INT_ML_C_N<2> C8325 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_N<2>
74 71 67 DP_INT_ML_N<2>

74 70 5 IN DP_INT_ML_C_P<3> C8326 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_P<3>
150OHM-100MA-8.5GHZ DLP0NS
CRITICAL FL8303
74 71 67 DP_INT_ML_P<3>

74 70 5 IN DP_INT_ML_C_N<3> C8327 0.1UF 10% 16V X5R-CERM 0201
74 DP_INT_ML_F_N<3>
74 71 67 DP_INT_ML_N<3>

71 70 12 IN EDP_IG_PANEL_PWR

CRITICAL
U8300
FPF1009
MFET-2X2-8IN
1 ON
2 VIN_1
3 VIN_2
4 VOUT_1
5 VOUT_2
6 GND
7 THRM PAD

71 69 68 66 65 61 51 38 PP5V_S4

C8309 0.1UF 10% 16V X7R-CERM 0402
C8311 0.1UF 10% 16V X7R-CERM 0402
C8312 10UF 20% 6.3V X5R 603

PP5VR3V3_SW_LCD_ISNS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

SENSOR_NONPROD_R
XW8320
SM

NC_ISNS_LCD_PANELN OUT
NC_ISNS_LCD_PANELP OUT

PP5VR3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL
L8300
FERR-220-OHM
0805

C8301 0.1UF 10% 16V X7R-CERM 0402
C8302 0.001UF 10% 50V X7R-CERM 0402

71 PP5VR3V3_SW_LCD
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C8300 1000PF 10% 100V X7R 0603

518S0829

LCD Panel HPD & AUX strapping

81 71 69 66 65 55 33 29 20 19 12 11 52 51 49 48 47 46 45 44 35 14 13
PP3V3_S0

R8303 1M 5% 1/20W MF 201
74 71 67 DP_INT_AUX_N
74 71 67 DP_INT_AUX_P
71 67 LCD_HPD_CONN
R8301 1M 5% 1/20W MF 201
R8302 1M 5% 1/20W MF 201

R8311 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_P<0>
R8312 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_N<0>
R8313 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_P<1>
R8314 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_N<1>
R8315 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_P<2>
R8316 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_N<2>
R8317 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_P<3>
R8318 1M 5% 1/20W MF 201
74 71 67 DP_INT_ML_N<3>

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012
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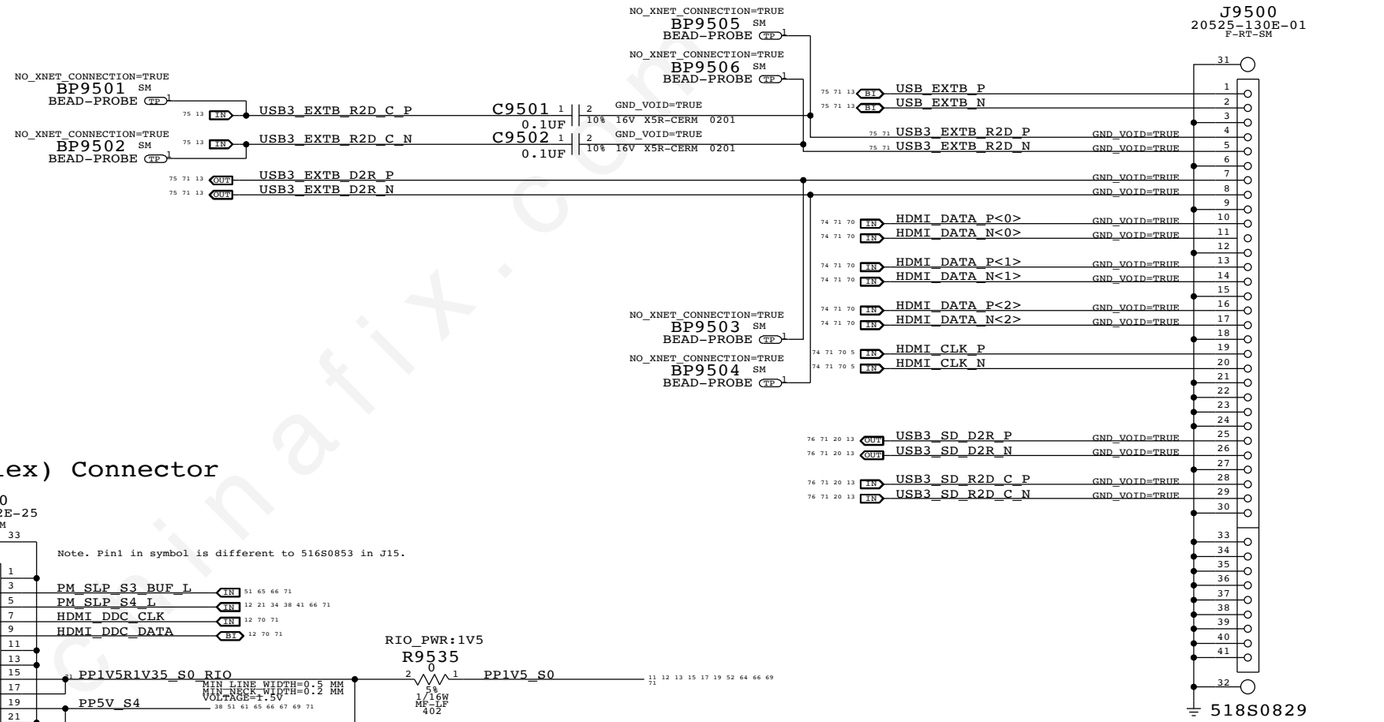
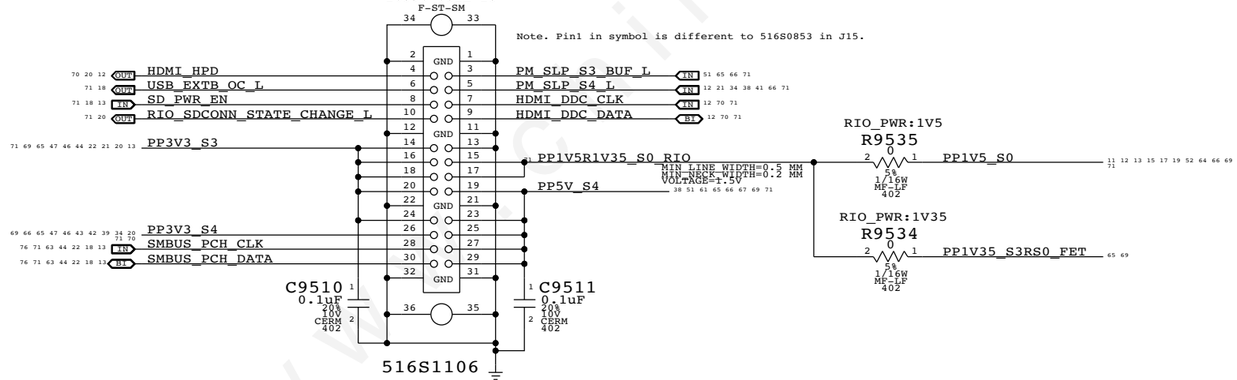
Wire-to-Board (Micro-coax) Connector



Board-to-Board (Flex) Connector



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RIO Connectors

Apple Inc.

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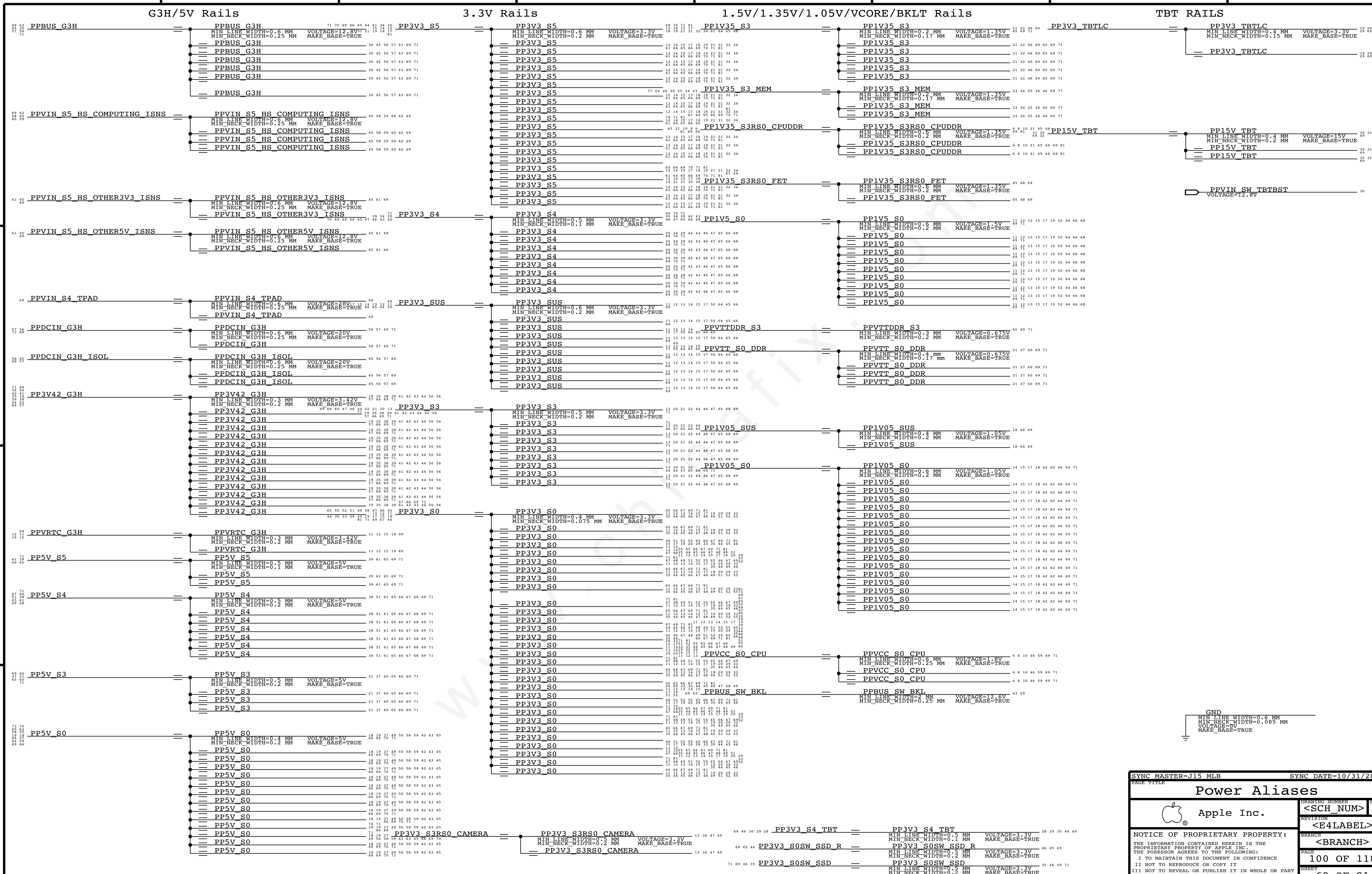

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Power Aliases

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Display Aliases

71 70 67 12 EDP_IG_PANEL_PWR = EDP_IG_PANEL_PWR 12 67 70 71
MAKE_BASE=TRUE

71 70 63 12 EDP_IG_BKL_ON = EDP_IG_BKL_ON 12 63 70 71
MAKE_BASE=TRUE

70 63 12 EDP_IG_BKL_PWM = EDP_IG_BKL_PWM 12 63 70
MAKE_BASE=TRUE

74 67 5 DP_INT_ML_C_P<3..0> = TP_DP_IG_A_MLP<3..0>
MAKE_BASE=TRUE

74 67 5 DP_INT_ML_C_N<3..0> = TP_DP_IG_A_MLN<3..0>
MAKE_BASE=TRUE

74 70 67 5 DP_INT_AUXCH_C_P = DP_INT_AUXCH_C_P 5 67 70 74
MAKE_BASE=TRUE

74 70 67 5 DP_INT_AUXCH_C_N = DP_INT_AUXCH_C_N 5 67 70 74
MAKE_BASE=TRUE

70 28 12 DP_TBTSNK0_HPD = DP_TBTSNK0_HPD 12 28 70
MAKE_BASE=TRUE

74 28 5 DP_TBTSNK0_ML_C_P<3..0> = TP_DP_IG_B_MLP<3..0>
MAKE_BASE=TRUE

74 28 5 DP_TBTSNK0_ML_C_N<3..0> = TP_DP_IG_B_MLN<3..0>
MAKE_BASE=TRUE

74 70 28 12 DP_TBTSNK0_AUXCH_C_P = DP_TBTSNK0_AUXCH_C_P 12 28 70 74
MAKE_BASE=TRUE

74 70 28 12 DP_TBTSNK0_AUXCH_C_N = DP_TBTSNK0_AUXCH_C_N 12 28 70 74
MAKE_BASE=TRUE

70 33 12 DP_TBTSNK0_DDC_DATA = DP_TBTSNK0_DDC_DATA 12 33 70
MAKE_BASE=TRUE

70 33 12 DP_TBTSNK0_DDC_CLK = DP_TBTSNK0_DDC_CLK 12 33 70
MAKE_BASE=TRUE

70 28 12 DP_TBTSNK1_HPD = DP_TBTSNK1_HPD 12 28 70
MAKE_BASE=TRUE

74 28 5 DP_TBTSNK1_ML_C_P<3..0> = TP_DP_IG_C_MLP<3..0>
MAKE_BASE=TRUE

74 28 5 DP_TBTSNK1_ML_C_N<3..0> = TP_DP_IG_C_MLN<3..0>
MAKE_BASE=TRUE

74 70 28 12 DP_TBTSNK1_AUXCH_C_P = DP_TBTSNK1_AUXCH_C_P 12 28 70 74
MAKE_BASE=TRUE

74 70 28 12 DP_TBTSNK1_AUXCH_C_N = DP_TBTSNK1_AUXCH_C_N 12 28 70 74
MAKE_BASE=TRUE

70 33 12 DP_TBTSNK1_DDC_DATA = DP_TBTSNK1_DDC_DATA 12 33 70
MAKE_BASE=TRUE

70 33 12 DP_TBTSNK1_DDC_CLK = DP_TBTSNK1_DDC_CLK 12 33 70
MAKE_BASE=TRUE

70 68 20 12 HDMI_HPD = HDMI_HPD 12 20 68 70
MAKE_BASE=TRUE

74 71 68 HDMI_DATA_P<0..2> = TP_DP_IG_D_MLP<2..0> 5
MAKE_BASE=TRUE

74 71 68 HDMI_DATA_N<0..2> = TP_DP_IG_D_MLN<2..0> 5
MAKE_BASE=TRUE

74 71 70 68 5 HDMI_CLK_P = HDMI_CLK_P 5 68 70 71 74
MAKE_BASE=TRUE

74 71 70 68 5 HDMI_CLK_N = HDMI_CLK_N 5 68 70 71 74
MAKE_BASE=TRUE

71 70 68 12 HDMI_DDC_CLK = HDMI_DDC_CLK 12 68 70 71
MAKE_BASE=TRUE

71 70 68 12 HDMI_DDC_DATA = HDMI_DDC_DATA 12 68 70 71
MAKE_BASE=TRUE

CPU signals

70 60 21 MEMVTT_EN = MEMVTT_EN 21 60 70
MAKE_BASE=TRUE

Thunderbolt Signals Through PEG

74 28 5 IN PCIE_TBT_D2R_P<3..0> = =PEG_D2R_P<3..0> OUT
MAKE_BASE=TRUE

74 28 5 IN PCIE_TBT_D2R_N<3..0> = =PEG_D2R_N<3..0> OUT
MAKE_BASE=TRUE

74 28 5 OUT PCIE_TBT_R2D_C_P<3..0> = =PEG_R2D_C_P<3..0> IN
MAKE_BASE=TRUE

74 28 5 OUT PCIE_TBT_R2D_C_N<3..0> = =PEG_R2D_C_N<3..0> IN
MAKE_BASE=TRUE

Unused PEG Lanes

5 TP_PEG_D2RP<15..4> = =PEG_D2R_P<15..4>
MAKE_BASE=TRUE

5 TP_PEG_D2RN<15..4> = =PEG_D2R_N<15..4>
MAKE_BASE=TRUE

5 TP_PEG_R2D_CP<15..4> = =PEG_R2D_C_P<15..4>
MAKE_BASE=TRUE

5 TP_PEG_R2D_CN<15..4> = =PEG_R2D_C_N<15..4>
MAKE_BASE=TRUE

70 49 PP3V3_S3_FAN_CTL = PP3V3_S3_FAN_CTL 49 70
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

RA201
0
1 2
5%
1/20W
MF
0201
PP3V3_S5 12 14 15 17 18 19 21 31 32 34 41 44 65 66 69 71 81

RA202
0
1 2
5%
1/20W
MF
0201
NOSTUFF
PP3V3_S4 20 34 39 42 43 46 47 65 66 68 69 71

Unused signals

12 BT_PWRRST_L
14 MEM_VDD_SEL_1V5_L
14 FW_PWR_EN_PCH
14 WOL_EN
14 FW_PME_L
11 DP_TBT_SEL
11 ENET_MEDIA_SENSE_RDIV
12 AUD_IPHS_SWITCH_EN_PCH
12 AUD_IP_PERIPHERAL_DET
12 AUD_I2C_INT_L
14 TBT_GO2SX_BIDIR
14 DPMUX_UC_IRQ
11 PEG_CLKREQ_L
11 ENET_CLKREQ_L
12 ENET_LOW_PWR_PCH
28 HDMITBTMUX_SEL_TBT
12 SDCONN_OC_L

		VOLTAGE	MAKE_BASE		
77 74 70 24 23 22	PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70 74
77 74 70 24 23 22	PP0V75_S3_MEM_VREFCA_A	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 74 77
74 70 26 25 22	PP0V75_S3_MEM_VREFCA_B	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B	22 25 26 70 74

65 63 62 59 58 50 49 37 19 18 71 69 66 PP5V_S0

XWA202
SM
1 2
PP5V_S0_AUDIO_AMP_L 53
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XWA203
SM
1 2
PP5V_S0_AUDIO_AMP_R 53
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

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Signal Aliases

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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_O_L	34
TRUE	AP_RESET_CONN_L	34
TRUE	PCIE_AP_D2R_PI_N	34 76
TRUE	PCIE_AP_D2R_PI_P	34 76
TRUE	PCIE_AP_R2D_N	34 76
TRUE	PCIE_AP_R2D_P	34 76
TRUE	PCIE_CLK100M_AP_CONN_N	34 76
TRUE	PCIE_CLK100M_AP_CONN_P	34 76
TRUE	PCIE_WAKE_L	12 34 36 76
TRUE	PP3V3_S3RS4_BT_F	34
TRUE	PP3V3_WLAN	34 42
TRUE	USB_BT_CONN_N	34 75
TRUE	USB_BT_CONN_P	34 75
TRUE	WIFI_EVENT_L	34 41 42
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	37 79
TRUE	MIPI_CLK_CONN_P	37 79
TRUE	CAM_SENSOR_WAKE_L_CONN	37
TRUE	MIPI_DATA_CONN_N	37 79
TRUE	MIPI_DATA_CONN_P	37 79
TRUE	SMBUS_SMC_0_S0_SDA	37 41 44 48 80
TRUE	SMBUS_SMC_0_S0_SCL	37 41 44 48 80
TRUE	I2C_CAM_SCK	36 37
TRUE	I2C_CAM_SDA	36 37
TRUE	PP5V_S3RS0_ALSCAM_F	37
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	5 68 70 74
TRUE	HDMI_CLK_P	5 68 70 74
TRUE	HDMI_DATA_N<0>	68 70 74
TRUE	HDMI_DATA_N<1>	68 70 74
TRUE	HDMI_DATA_N<2>	68 70 74
TRUE	HDMI_DATA_P<0>	68 70 74
TRUE	HDMI_DATA_P<1>	68 70 74
TRUE	HDMI_DATA_P<2>	68 70 74
TRUE	USB3_SD_D2R_N	13 20 68 76
TRUE	USB3_SD_D2R_P	13 20 68 76
TRUE	USB3_SD_R2D_C_N	13 20 68 76
TRUE	USB3_SD_R2D_C_P	13 20 68 76
TRUE	USB3_EXTB_D2R_N	13 68 75
TRUE	USB3_EXTB_D2R_P	13 68 75
TRUE	USB3_EXTB_R2D_N	68 75
TRUE	USB3_EXTB_R2D_P	68 75
TRUE	USB_EXTB_N	13 68 75
TRUE	USB_EXTB_P	13 68 75
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 68
TRUE	PP1V5R1V35_S0_RIO	68
TRUE	HDMI_DDC_CLK	12 68 70
TRUE	HDMI_DDC_DATA	12 68 70
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 18 22 44 63 68 76
TRUE	SMBUS_PCH_DATA	13 18 22 44 63 68 76
TRUE	PM_SLP_S3_BUF_L	51 65 66 68
TRUE	PM_SLP_S4_L	12 21 34 38 41 66 68
TRUE	PP3V3_S3	3X 13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S4	5X 38 51 61 65 66 67 68 69
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 68
TRUE	USB_EXTB_OC_L	18 68
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	SMC_LID_R	43
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 37 49 50 58 59 62 63 65 66 69 70 71
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 50
TRUE	LPCPLUS_RESET_L	20 50 76
TRUE	LPC_AD<0>	13 41 50 76
TRUE	LPC_AD<1>	13 41 50 76
TRUE	LPC_AD<2>	13 41 50 76
TRUE	LPC_AD<3>	13 41 50 76
TRUE	LPC_CLK33M_LPCPLUS	19 50 76
TRUE	LPC_FRAME_L	13 41 50 76
TRUE	LPC_PWRDWN_L	12 20 41 50
TRUE	LPC_SERIRQ	13 41 50
TRUE	PM_CLKRUN_L	12 41 50
TRUE	PP5V_S0	10 19 37 49 50 58 59 62 63 65 68 69 70 71
TRUE	SMC_RESET_L	41 42 50 57
TRUE	SMC_ROMBOOT	42 50
TRUE	SMC_RX_L	41 42 50
TRUE	SMC_TCK	41 42 50
TRUE	SMC_TDI	41 42 50
TRUE	SMC_TDO	41 42 50
TRUE	SMC_TMS	41 42 50
TRUE	SMC_TX_L	41 42 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	SPI_ALT_CLK	50
TRUE	SPI_ALT_CS_L	50
TRUE	SPI_ALT_MISO	50
TRUE	SPI_ALT_MOSI	50
TRUE	TP_SMC_MD1	50
TRUE	TP_SMC_TRST_L	50
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	39
TRUE	Z2_MOSI	39
TRUE	Z2_MISO	39
TRUE	Z2_SCLK	39
TRUE	Z2_HOST_INTN	39
TRUE	Z2_CLKIN	39
TRUE	Z2_KEY_ACT_L	39
TRUE	PSOC_F_CS_L	39
TRUE	PICKB_L	39
TRUE	PSOC_MOSI	39
TRUE	PSOC_MISO	39
TRUE	PSOC_SCLK	39
TRUE	SMBUS_SMC_2_S3_SCL	39 41 44 80
TRUE	SMBUS_SMC_2_S3_SDA	39 41 44 80
TRUE	SMC_LID	39 41 42 43
TRUE	SMC_T101_COM_1	
TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP5V_S5	39 61 65 69 71
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 34 39 42 43 46 47 65 66 68 69 70 71
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	WS_CONTROL_KBD	39
TRUE	WS_KBD1	39
TRUE	WS_KBD10	39
TRUE	WS_KBD11	39
TRUE	WS_KBD12	39
TRUE	WS_KBD13	39
TRUE	WS_KBD14	39
TRUE	WS_KBD15_CAP	39
TRUE	WS_KBD16_NUM	39
TRUE	WS_KBD17	39
TRUE	WS_KBD18	39
TRUE	WS_KBD19	39
TRUE	WS_KBD2	39
TRUE	WS_KBD20	39
TRUE	WS_KBD21	39
TRUE	WS_KBD22	39
TRUE	WS_KBD23	39
TRUE	WS_KBD3	39
TRUE	WS_KBD4	39
TRUE	WS_KBD5	39
TRUE	WS_KBD6	39
TRUE	WS_KBD7	39
TRUE	WS_KBD8	39
TRUE	WS_KBD9	39
TRUE	WS_KBD_ONOFF_L	39
TRUE	WS_LEFT_OPTION_KBD	39
TRUE	WS_LEFT_SHIFT_KBD	39
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 40 63
TRUE	KBDBKLT_RETURN2	2X 40 63
TRUE	PPVOUT_S0_KBDBKLT	40 63
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	51 55
TRUE	AUD_HP_PORT_R	51 55
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	51 55
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	AUD_CONN_SLEEVE_XW	4X 54 55
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 81
TRUE	SPKRCONN_L_OUT_P	53 55 81
TRUE	SPKRCONN_SL_OUT_N	53 55 81
TRUE	SPKRCONN_SL_OUT_P	53 55 81
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 81
TRUE	SPKRCONN_R_OUT_P	53 55 81
TRUE	SPKRCONN_SR_OUT_N	53 55 81
TRUE	SPKRCONN_SR_OUT_P	53 55 81
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	41 44 56 57 80
TRUE	SMBUS_SMC_5_G3_SDA	41 44 56 57 80
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 74
TRUE	DP_INT_AUX_P	67 74
TRUE	DP_INT_ML_N<0>	67 74
TRUE	DP_INT_ML_N<1>	67 74
TRUE	DP_INT_ML_N<2>	67 74
TRUE	DP_INT_ML_N<3>	67 74
TRUE	DP_INT_ML_P<0>	67 74
TRUE	DP_INT_ML_P<1>	67 74
TRUE	DP_INT_ML_P<2>	67 74
TRUE	DP_INT_ML_P<3>	67 74
TRUE	LCD_FSS	63 67
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	63 67
TRUE	LED_RETURN_2	63 67
TRUE	LED_RETURN_3	63 67
TRUE	LED_RETURN_4	63 67
TRUE	LED_RETURN_5	63 67
TRUE	LED_RETURN_6	63 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	63 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 41 66
TRUE	PPVTT_S0_DDR	21 27 60 69
TRUE	PP3V3_S0	65 66 67 69 71 81 11 12 13 14 15 17 19 20 29 33 35 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 22 44 46 47 65 68 69 71
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 34 41 44 65 66 69 70 81
TRUE	PP3V3_S5_AVREF_SMC	41 42
TRUE	PP3V42_G3H	19 35 38 39 41 42 43 44 50 56 57 66 69 71
TRUE	PP5V_S0	10 19 37 49 50 58 59 62 63 65 68 69 70 71
TRUE	PP5V_S3	21 37 60 65 66 69
TRUE	PP5V_S5	39 61 65 69 71
TRUE	PPBUS_G3H	30 45 56 57 63 69
TRUE	PPDCIN_G3H	56 57 69
TRUE	PPVCC_S0_CPU	6 8 10 46 59 69
TRUE	PPVTTDDR_S3	60 69
TRUE	PP3V3_S0SW_SSD	35 46 69
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 66 68 69
TRUE	PP1V35_S3	21 22 46 60 65 69

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 74
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 74
TRUE	XDP_CPU_TDO	6 18 74
TRUE	XDP_CPUPCH_TRST_L	6 18 74
TRUE	XDP_CPU_TMS	6 18 74
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 74
TRUE	XDP_CPU_PRDY_L	6 18 74
TRUE	PM_RSMRST_L	12 66 76
TRUE	PM_PCH_PWROK	12 19 76
TRUE	PM_SYSRST_L	12 19 41 76
TRUE	CPU_CFG<3>	6 18 74
TRUE	PP1V05_S0	14 15 17 18 42 62 66 69
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	39 41 42
TRUE	PM_DSW_PWRGD	12 41 76
TRUE	ALL_SYS_PWRGD	18 19 41 58 66
TRUE	PM_PCH_SYS_PWROK	12 18 19 41 76
TRUE	PLT_RESET_L	12 18 20 21
TRUE	EDP_IG_PANEL_PWR	12 67 70
TRUE	EDP_IG_BKL_ON	12 63 70

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Functional Test Points

Apple Inc.

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NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE	
NC_USB3_SPARE_D2RN	=	TRUE	TRUE	NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP	=	TRUE	TRUE	NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN	=	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP	=	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
NC_USB3_EXTC_D2RN	=	TRUE	TRUE	NC_USB3_EXTC_D2RN
NC_USB3_EXTC_D2RP	=	TRUE	TRUE	NC_USB3_EXTC_D2RP
NC_USB3_EXTC_R2D_CN	=	TRUE	TRUE	NC_USB3_EXTC_R2D_CN
NC_USB3_EXTC_R2D_CP	=	TRUE	TRUE	NC_USB3_EXTC_R2D_CP
NC_USB3_EXTD_D2RN	=	TRUE	TRUE	NC_USB3_EXTD_D2RN
NC_USB3_EXTD_D2RP	=	TRUE	TRUE	NC_USB3_EXTD_D2RP
NC_USB3_EXTD_R2D_CN	=	TRUE	TRUE	NC_USB3_EXTD_R2D_CN
NC_USB3_EXTD_R2D_CP	=	TRUE	TRUE	NC_USB3_EXTD_R2D_CP
NC_PCIE_ENET_D2RN	=	TRUE	TRUE	NC_PCIE_ENET_D2RN
NC_PCIE_ENET_D2RP	=	TRUE	TRUE	NC_PCIE_ENET_D2RP
NC_PCIE_ENET_R2D_CN	=	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
NC_PCIE_ENET_R2D_CP	=	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
NC_SATA_A_D2RN	=	TRUE	TRUE	NC_SATA_A_D2RN
NC_SATA_A_D2RP	=	TRUE	TRUE	NC_SATA_A_D2RP
NC_SATA_A_R2D_CN	=	TRUE	TRUE	NC_SATA_A_R2D_CN
NC_SATA_A_R2D_CP	=	TRUE	TRUE	NC_SATA_A_R2D_CP
NC_SATA_B_D2RN	=	TRUE	TRUE	NC_SATA_B_D2RN
NC_SATA_B_D2RP	=	TRUE	TRUE	NC_SATA_B_D2RP
NC_SATA_B_R2D_CN	=	TRUE	TRUE	NC_SATA_B_R2D_CN
NC_SATA_B_R2D_CP	=	TRUE	TRUE	NC_SATA_B_R2D_CP
NC_SATA_ODD_D2RN	=	TRUE	TRUE	NC_SATA_ODD_D2RN
NC_SATA_ODD_D2RP	=	TRUE	TRUE	NC_SATA_ODD_D2RP
NC_SATA_ODD_R2D_CN	=	TRUE	TRUE	NC_SATA_ODD_R2D_CN
NC_SATA_ODD_R2D_CP	=	TRUE	TRUE	NC_SATA_ODD_R2D_CP
NC_SATA_D_D2RN	=	TRUE	TRUE	NC_SATA_D_D2RN
NC_SATA_D_D2RP	=	TRUE	TRUE	NC_SATA_D_D2RP
NC_SATA_D_R2D_CN	=	TRUE	TRUE	NC_SATA_D_R2D_CN
NC_SATA_D_R2D_CP	=	TRUE	TRUE	NC_SATA_D_R2D_CP
NC_SATA_F_D2RN	=	TRUE	TRUE	NC_SATA_F_D2RN
NC_SATA_F_D2RP	=	TRUE	TRUE	NC_SATA_F_D2RP
NC_SATA_F_R2D_CN	=	TRUE	TRUE	NC_SATA_F_R2D_CN
NC_SATA_F_R2D_CP	=	TRUE	TRUE	NC_SATA_F_R2D_CP
NC_USB_EXTCN	=	TRUE	TRUE	NC_USB_EXTCN
NC_USB_EXTCP	=	TRUE	TRUE	NC_USB_EXTCP
NC_USB_SDN	=	TRUE	TRUE	NC_USB_SDN
NC_USB_SDP	=	TRUE	TRUE	NC_USB_SDP
NC_USB_WLANN	=	TRUE	TRUE	NC_USB_WLANN
NC_USB_WLANP	=	TRUE	TRUE	NC_USB_WLANP
NC_USB_6N	=	TRUE	TRUE	NC_USB_6N
NC_USB_6P	=	TRUE	TRUE	NC_USB_6P
NC_USB_7N	=	TRUE	TRUE	NC_USB_7N
NC_USB_7P	=	TRUE	TRUE	NC_USB_7P
NC_USB_EXTDN	=	TRUE	TRUE	NC_USB_EXTDN
NC_USB_EXTDP	=	TRUE	TRUE	NC_USB_EXTDP
NC_USB_PSOCN	=	TRUE	TRUE	NC_USB_PSOCN
NC_USB_PSOCP	=	TRUE	TRUE	NC_USB_PSOCP
NC_USB_IRN	=	TRUE	TRUE	NC_USB_IRN
NC_USB_IRP	=	TRUE	TRUE	NC_USB_IRP
NC_ITPXDP_CLK100MN	=	TRUE	TRUE	NC_ITPXDP_CLK100MN
NC_ITPXDP_CLK100MP	=	TRUE	TRUE	NC_ITPXDP_CLK100MP
NC_PCI_PME_L	=	TRUE	TRUE	NC_PCI_PME_L
NC_PCI_CLK33M_OUT2	=	TRUE	TRUE	NC_PCI_CLK33M_OUT2
NC_PCI_CLK33M_OUT3	=	TRUE	TRUE	NC_PCI_CLK33M_OUT3
NC_HDA_SDIN1	=	TRUE	TRUE	NC_HDA_SDIN1
NC_HDA_SDIN2	=	TRUE	TRUE	NC_HDA_SDIN2
NC_HDA_SDIN3	=	TRUE	TRUE	NC_HDA_SDIN3
NC_LPC_DREQ0_L	=	TRUE	TRUE	NC_LPC_DREQ0_L
NC_CLINK_CLK	=	TRUE	TRUE	NC_CLINK_CLK
NC_CLINK_DATA	=	TRUE	TRUE	NC_CLINK_DATA
NC_CLINK_RESET_L	=	TRUE	TRUE	NC_CLINK_RESET_L
NC_USB_SMCP	=	TRUE	TRUE	NC_USB_SMCP
NC_USB_SMCN	=	TRUE	TRUE	NC_USB_SMCN
NC_SMC_INTERFACE_2	=	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

		NO_TEST	MAKE_BASE	
NC_TBT_XTAL25OUT	=	TRUE	TRUE	NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3..0>	=	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
TP_DP_TBTSRC_ML_CN<3..0>	=	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
NC_DP_TBTSRC_AUXCH_CP	=	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
NC_DP_TBTSRC_AUXCH_CN	=	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
NC_DP_IG_D_AUXCHN	=	TRUE	TRUE	NC_DP_IG_D_AUXCHN
NC_DP_IG_D_AUXCHP	=	TRUE	TRUE	NC_DP_IG_D_AUXCHP
NC_PCIE_CLK100M_GPUN	=	TRUE	TRUE	NC_PCIE_CLK100M_GPUN
NC_PCIE_CLK100M_GPUP	=	TRUE	TRUE	NC_PCIE_CLK100M_GPUP
NC_PCIE_CLK100M_PE5N	=	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
NC_PCIE_CLK100M_PE5P	=	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
NC_PCIE_CLK100M_ENETSDN	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
NC_PCIE_CLK100M_ENETSDP	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
NC_PCIE_CLK100M_ENETN	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
NC_PCIE_CLK100M_ENETP	=	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
NC_PCIE_CLK100M_PEGBN	=	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
NC_PCIE_CLK100M_PEGBP	=	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
NC_PCIE_CLK100M_SWN	=	TRUE	TRUE	NC_PCIE_CLK100M_SWN
NC_PCIE_CLK100M_SWP	=	TRUE	TRUE	NC_PCIE_CLK100M_SWP
NC_PCH_GPIO64_CLKOUTFLEX0	=	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1	=	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2	=	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3	=	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
NC_USB_4N	=	TRUE	TRUE	NC_USB_4N
NC_USB_4P	=	TRUE	TRUE	NC_USB_4P

TRUE	PCIE_TBT_R2D_P<3..0>		
TRUE	PCIE_TBT_R2D_N<3..0>		
TRUE	PCIE_TBT_D2R_C_P<3..0>		
TRUE	PCIE_TBT_D2R_C_N<3..0>		
R197 TRUE	DMI_S2N_P<3..1>		
R197 TRUE	DMI_S2N_N<3..1>		
R197 TRUE	DMI_N2S_P<3..1>		
R197 TRUE	DMI_N2S_N<3..1>		

PLACEABLE BEAD-PROBES FOR TBT

TBT_A_R2D_C_P<1>	1	SM BEAD-PROBE	BPA535 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_P<1>	1	SM BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
TBT_A_D2R_N<1>	1	SM BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: NC & No Test

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	-	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 72
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 72
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 72
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 71
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 72
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 72
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 71
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 71
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 71
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 71
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 71
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 71
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 71
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 41
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 42
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 41 42 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	6 14 42
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 70
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	22 23 24 70 77
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	22 25 26 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 70
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 70
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 72
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 72
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 72
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 70
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 70

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	5 67 70
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	5 67 70
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 71 74
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 71 74
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	5 67 70
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 71
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 71

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	68 70 71
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	5 68 70 71
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	5 68 70 71
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	5 28 70
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	5 28 70
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	5 28 70
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28
	DP_85D		DP_TBTSNK0_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK0_AUXCH_C_N	12 28 70
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28
TBTSNK1_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28
	DP_85D		DP_TBTSNK1_AUXCH_C_P	12 28 70
	DP_85D		DP_TBTSNK1_AUXCH_C_N	12 28 70

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 72
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 72
I277	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 72
I277	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 72
I299	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 72
I299	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 72
I300	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 72
I300	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 72
I211 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_EXTA	USB_85D	USB	USB_EXTA_P	13 38
	USB_EXTA	USB_85D	USB	USB_EXTA_N	13 38
I245	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
I245	USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
I245	USB_EXTA	USB_85D	USB	USB_LT1_P	38
I245	USB_EXTA	USB_85D	USB	USB_LT1_N	38
	USB_NC	USB_85D	USB	NC_USB_EXTCP	13 72
	USB_NC	USB_85D	USB	NC_USB_EXTCN	13 72
I233	USB_NC	USB_85D	USB	NC_USB_SDP	13 72
I233	USB_NC	USB_85D	USB	NC_USB_SDN	13 72
I277		CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	38 41 42
I275		CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	38 41 42
	USB_SMC	USB_85D	USB	NC_USB_SMCP	72
	USB_SMC	USB_85D	USB	NC_USB_SMCN	72
I228	USB_NC	USB_85D	USB	NC_USB_6P	13 72
I228	USB_NC	USB_85D	USB	NC_USB_6N	13 72
I228	USB_NC	USB_85D	USB	NC_USB_7P	13 72
I228	USB_NC	USB_85D	USB	NC_USB_7N	13 72
	USB_EXTB	USB_85D	USB	USB_EXTB_P	13 68 71
	USB_EXTB	USB_85D	USB	USB_EXTB_N	13 68 71
I260	USB_NC	USB_85D	USB	NC_USB_EXTDP	13 72
I259	USB_NC	USB_85D	USB	NC_USB_EXTDN	13 72
	USB_BT	USB_85D	USB	USB_BT_P	13 34
	USB_BT	USB_85D	USB	USB_BT_N	13 34
		USB_85D	USB	USB_BT_CONN_P	34 71
		USB_85D	USB	USB_BT_CONN_N	34 71
I285	USB_NC	USB_85D	USB	NC_USB_IRP	13 72
I287	USB_NC	USB_85D	USB	NC_USB_IRN	13 72
I281	USB_TPAD	USB_85D	USB	USB_TPAD_P	13 39
I281	USB_TPAD	USB_85D	USB	USB_TPAD_N	13 39
I302		USB_85D	USB	USB_TPAD_R_P	39
I302		USB_85D	USB	USB_TPAD_R_N	39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
I222	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 38
I223	USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 38
I266		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
I266		USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
I238	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	38
I222	USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	38
I266		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 38
I266		USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 38
I222	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 68 71
I223	USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 68 71
I266		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
I266		USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
I223	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	68 71
I223	USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	68 71
I266		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 68
I266		USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 68
I293 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 72
I293 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 72
I293	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 72
I292	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 72
I293 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 72
I293 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 72
I293	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 72
I293	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 72

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I256 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
I255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
I255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
I255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 37
I251 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
I250	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 41 50 71
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 41 50 71
LPC_RESET_L	LPC_45S	LPC	LPCPLUS_RESET_L	20 50 71
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 22 44 63 68 71
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 22 44 63 68 71
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 44
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 44
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 44
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 50
SPI_CLK	SPI_45S	SPI	SPI_CLK	50
	SPI_45S	SPI	SPI_MOSI_R	13 50
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	50
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 50
	SPI_45S	SPI	SPI_CS0_R_L	13 50
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	50
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 68 71
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 68 71
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 68 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	34 71
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	34 71
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 34
P304	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 34
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	34
P305	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 34
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 34
P276	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	34 71
P276	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	34 71
P329 PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	36 37
P329 PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	36 37
P329	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 37
P329	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 37
P330 PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 37
P330 PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 37
P331	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	36 37
P332	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	36 37
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 41
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 50 71
P240	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
P241 PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
P242 PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
P243 PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
P244 PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
P245 PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
P246 PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
P247 PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
P252 PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
P253 PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
P254 PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
P255 PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
P300	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	34 71
P299	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	34 71
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 37
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 37
P334	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	36 37
P334	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	36 37
P281 PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
P282	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
P315 PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
P316 PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
P318 PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
P319 PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
P309 PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 66 71
P307 PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 41 71
P314 PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
P317 PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 71 76
P320 PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 41 71
P315 PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 41 71
P321 PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 41
P322 PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 42
P326 PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 34 36 71
P272 PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
P335 PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 35
P336 PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 35
P338 PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 35
P337 PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 35
P339	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	35
P340	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	35

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 70 74
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A 22 23 24 70 74
		MEM_PWR	PP1V35_S3_MEM 23 24 25 26 46 69

SYNC_MASTER=SIDLE J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31 72
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 72
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=SIDLE J45 SYNC_DATE=12/10/2012

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
E10	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
E12		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
E10	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
E10	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
E10	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
E10	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
E10	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
E10	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
E10	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
E10	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
E12	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
E12	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
E12		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
E12		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
E13	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
E13	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
E13		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
E13		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
E14			S2_MEM_PWR	PP1V35_CAM
E14			S2_MEM_PWR	PP0V675_CAM_VREF
E14			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
E14			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	39 41 44 71
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	39 41 44 71
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	41 44 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	41 44 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	37 41 44 48 71
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	37 41 44 48 71
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_G3_SCL	41 44 56 57 71
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	41 44 56 57 71
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	41 43
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
E429	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P 47
E425	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N 47
E427		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P 47
E423		THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P 48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N 48
E422	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P 47
E424	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N 47
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P 48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N 48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P 48
	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N 48
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P 46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N 46
E419		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P 46
E420		SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N 46
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P 47
		SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N 47
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N 47 63
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P 47 63
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P 45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N 45
E514	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P 45
E515	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N 45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P 45
	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N 45
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P 46
		SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N 46
E516	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P
E517	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N
E429	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P 46 59
E430	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N 46 59
E431	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P 46 59
E432	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N 46 59
E433	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P 46 59
E434	SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N 46 59
E435	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P 46
E436	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N 46
E491	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P 81
E492	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N 81
E507	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P 81
E508	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N 81
E409	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N 46
E408	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P 46
E407		AUDIODIFF	AUDIO	ISNS_TBT_R_N 46
E408		AUDIODIFF	AUDIO	ISNS_TBT_R_P 46
E446	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P 46
E448		THERM_1TO1_45S	THERM	ISNS_SSD_N 46
E447	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P 46
E449		THERM_1TO1_45S	THERM	ISNS_SSD_R_N 46
E449	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P 62
E450		THERM_1TO1_45S	THERM	P1V05S0_CS_N 62
E451	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P 62
E452		THERM_1TO1_45S	THERM	P1V05S0_SENSE_N 62
E453	SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P 28 48
E454		THERM_1TO1_45S	THERM	TBT_THERMD_N 48
E455	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P 57
E456		AUDIODIFF	AUDIO	CHGR_CSI_R_N 57
E457	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P 57
E458		AUDIODIFF	AUDIO	CHGR_CSO_R_N 57
E511	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P
E512	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N
E513	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P 47
E518	SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N 47

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
E460	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P 53
E461	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N 53
E463	AUDIODIFF	AUDIO	RSUBIN_P 53
E464	AUDIODIFF	AUDIO	RSUBIN_N 53
E465	AUDIODIFF	AUDIO	LSUBIN_P 53
E462	AUDIODIFF	AUDIO	LSUBIN_N 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO2_R_P 51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO2_R_N 51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO2_L_P 51 53
	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO2_L_N 51 53
		AUDIODIFF	AUDIO AUD_SPKRAMP_RIN_P 53
		AUDIODIFF	AUDIO AUD_SPKRAMP_RIN_N 53
		AUDIODIFF	AUDIO AUD_SPKRAMP_LIN_P 53
		AUDIODIFF	AUDIO AUD_SPKRAMP_LIN_N 53
E460		AUDIODIFF	AUDIO SPKRAMP_RIN_P 53
E462		AUDIODIFF	AUDIO SPKRAMP_RIN_N 53
E460		AUDIODIFF	AUDIO SPKRAMP_LIN_P 53
E462		AUDIODIFF	AUDIO SPKRAMP_LIN_N 53
E456	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_SL_OUT_P 53 55 71
E457	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_SL_OUT_N 53 55 71
E460	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_SR_OUT_P 53 55 71
E458	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_SR_OUT_N 53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_L_OUT_P 53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_L_OUT_N 53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_R_OUT_P 53 55 71
	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO SPKRCONN_R_OUT_N 53 55 71
E480	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO AUD_MIC_IN1_R_P
E481	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO AUD_MIC_IN1_R_N
E482	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO CODEC_HS_MIC_P 51
E483	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO CODEC_HS_MIC_N 51
E484	AUDIO_DIFFPAIR	DIFFPAIR	AUDIO AUD_MIC_IN1_L_P
E485		DIFFPAIR	AUDIO AUD_MIC_IN1_L_N
E486		DIFFPAIR	AUDIO AUD_HS_MIC_P 54 55
E487		DIFFPAIR	AUDIO AUD_HS_MIC_N 54 55
E488		DIFFPAIR	AUDIO HS_MIC_P 51 54
E488		DIFFPAIR	AUDIO HS_MIC_N 51 54
E490		DIFFPAIR	AUDIO AUD_CONN_HS_MIC_P
E491		DIFFPAIR	AUDIO AUD_CONN_HS_MIC_N
E494	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO3_R_P 51 53
E495	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO3_R_N 51 53
E493	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO3_L_P 51 53
E492	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO AUD_LO3_L_N 51 53
			SB_POWER PP3V3_S5 12 14 15 17 18 19 21 31 32 34
			SB_POWER PP3V3_S0 11 12 13 14 15 17 19 25 50 66 67
			SB_POWER PP1V35_S3RS0_CPUDDR 25 44 45 46 47 48 49 51 52 55 69 71 8 10 21 65 66 69
			GND GND

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