1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-05-09

SCHEM,MLB,KEPLER,2PHASE,D2

FSB,10/10/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9589	1	SCHEM,MLB,KEPLER_2PHASE,D2	SCH	CRITICAL	
820-3332	1	PCBF,MLB,KEPLER_2PHASE,D2	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST MODIFIED=Wed May 9 13 50 52 2012

DRAWING TITLE: SCHEM,MLB,KEPLER,2PHASE,D2

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
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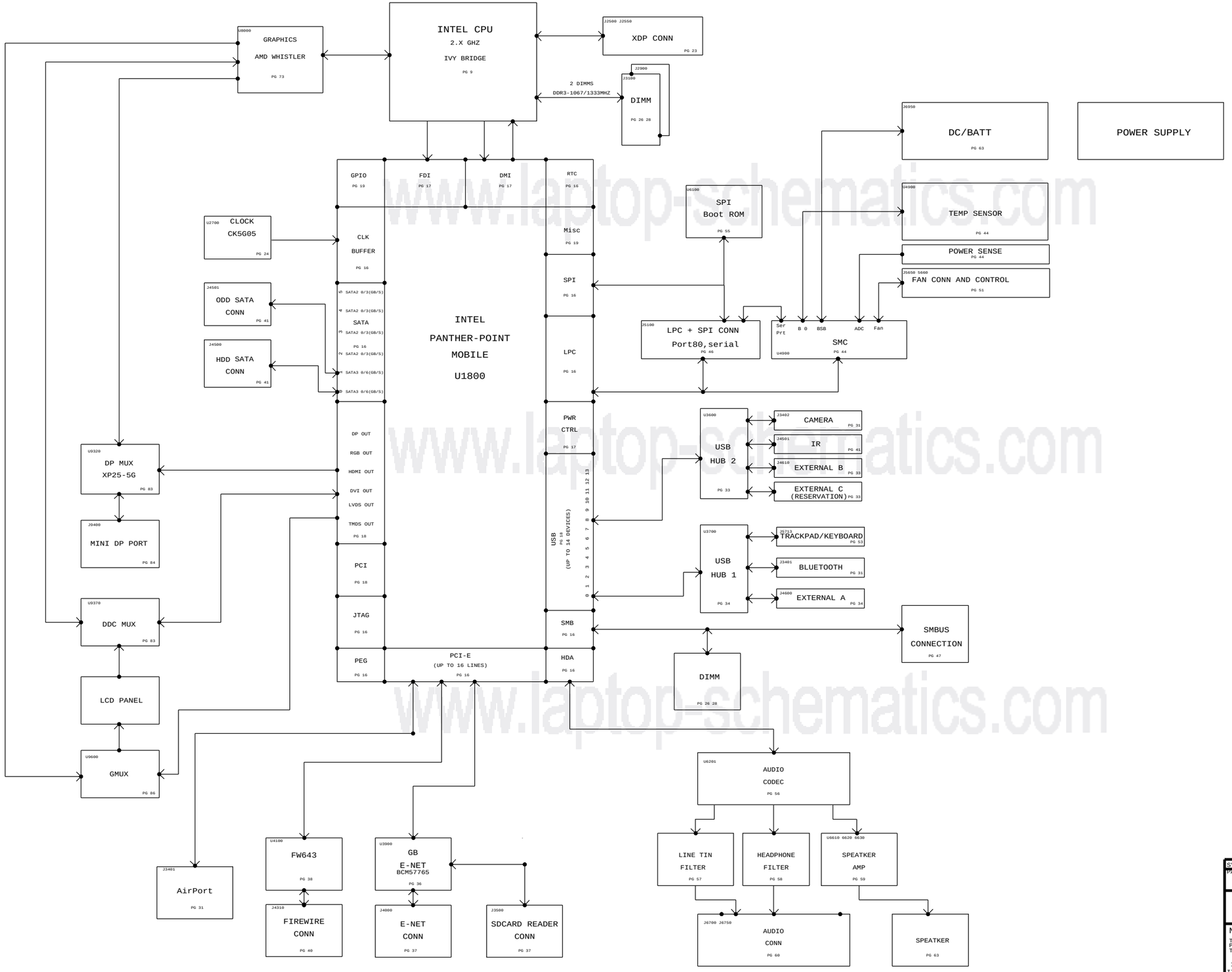

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

System Block Diagram

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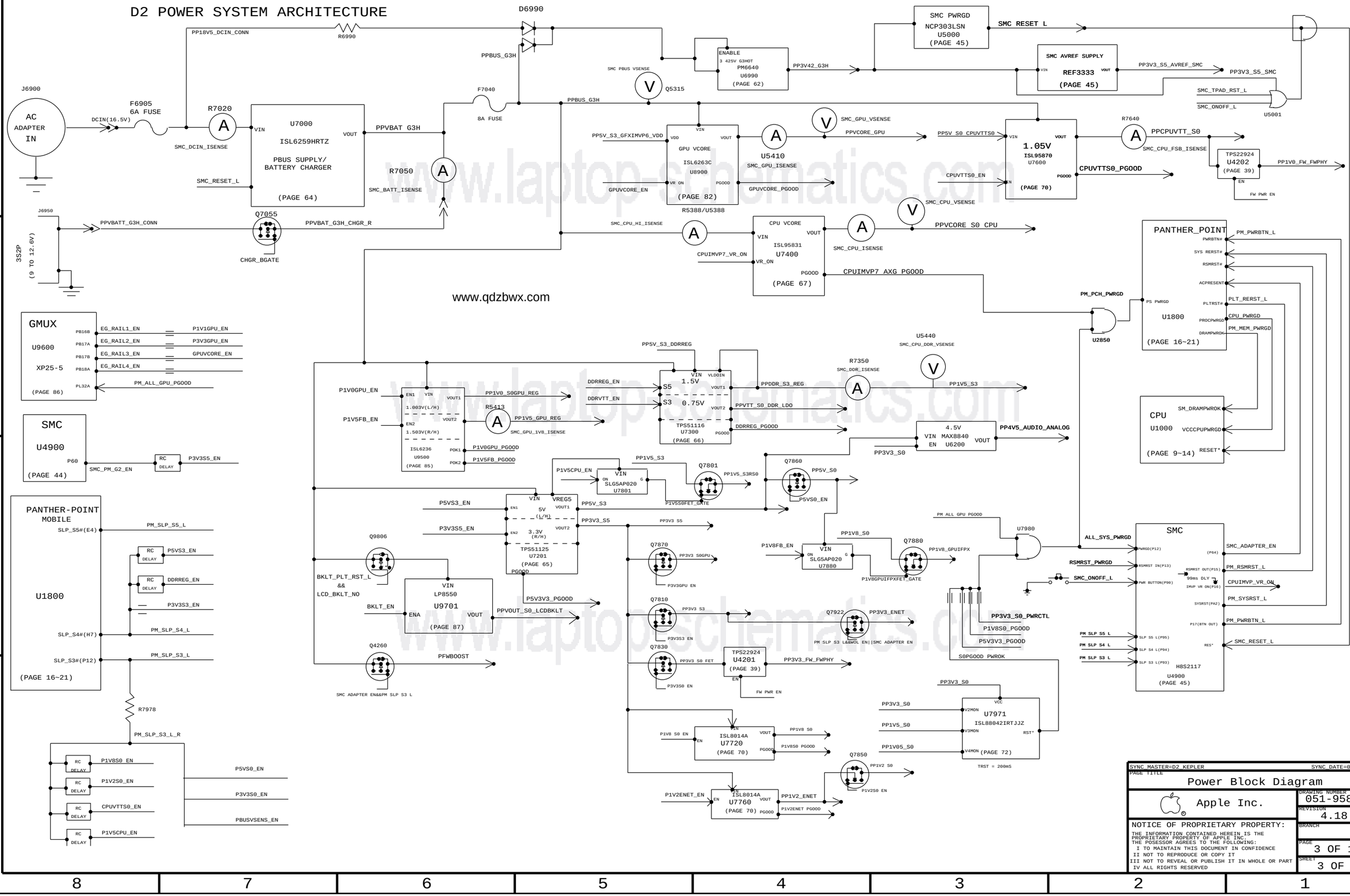
D2 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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Power Block Diagram

Apple Inc.

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Revision History

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BOM Variants (continued on CSA 6)

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3726	D2,MLB,KEPLER,DEV	D2_DEVEL:ENG
085-4776	D2,MLB,KEPLER,FSB DEV	D2_DEVEL:FSB
607-9546	D2,MLB,KEPLER_2PHASE,COMMON	D2_COMMON,POSCAP_MYLAR_PAIR
685-0016	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	PBUS_CAP:KEMET
685-0017	PBUS PAIR,SANYO POSCAP,SHORT MYLAR,D2	PBUS_CAP:SANYO
639-3378	PCBA,2.3G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY3V	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3V,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3379	PCBA,2.3G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY3W	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY3W,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3380	PCBA,2.3G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY3Y	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY3Y,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3381	PCBA,2.3G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY40	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY40,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3384	PCBA,2.3G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DY43	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY43,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3385	PCBA,2.3G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DY44	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY44,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3386	PCBA,2.3G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DY45	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY45,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3387	PCBA,2.3G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DY4C	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY4C,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2821	PCBA,2.6G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,DRF1	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF1,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2825	PCBA,2.6G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,DRF4	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRF4,DEVEL_BOM,RAM_2G_HYNIX_1600
639-2817	PCBA,2.6G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DRDN	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDN,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2815	PCBA,2.6G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,DRDW	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDW,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-2979	PCBA,2.6G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,DT9H	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9H,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2980	PCBA,2.6G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DT9D	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9D,DEVEL_BOM,RAM_4G_HYNIX_1600
639-2981	PCBA,2.6G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,DT9F	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DT9F,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-2982	PCBA,2.6G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,DT9G	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DT9G,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3618	PCBA,2.7G,8G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HN	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HN,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3619	PCBA,2.7G,8G_HYN,VRAM_SAM,MLB_KEPLER,D2,F0HR	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HR,DEVEL_BOM,RAM_2G_HYNIX_1600
639-3561	PCBA,2.7G,8G_SAM,VRAM_HYN,MLB_KEPLER,D2,DYW4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYW4,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3620	PCBA,2.7G,8G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HV	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HV,DEVEL_BOM,RAM_2G_SAMSUNG_1600
639-3627	PCBA,2.7G,16G_HYN,VRAM_HYN,MLB_KEPLER,D2,F0HM	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HM,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3562	PCBA,2.7G,16G_HYN,VRAM_SAM,MLB_KEPLER,D2,DYW5	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:DYW5,DEVEL_BOM,RAM_4G_HYNIX_1600
639-3628	PCBA,2.7G,16G_SAM,VRAM_HYN,MLB_KEPLER,D2,F0HY	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0HY,DEVEL_BOM,RAM_4G_SAMSUNG_1600
639-3629	PCBA,2.7G,16G_SAM,VRAM_SAM,MLB_KEPLER,D2,F0HT	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0HT,DEVEL_BOM,RAM_4G_SAMSUNG_1600

BOM Groups

BOM GROUP	BOM OPTIONS
D2_COMMON	ALTERNATE,COMMON,D2_COMMON1,D2_COMMON2,D2_PROGPARTS,D2_PVB
D2_COMMON1	CPUMEM S0 SMC DEBUG YES DPMUX HOCO TBTRTR PRQ TBTBST Y TBTHV P15V HUB 2NONREM USBHUB2512B SPEAKERID SMC PACKAGE PROD SKIP 5V3V3 AUDIBLE CHGR 5V LDO P1V5S0 LDO
D2_COMMON2	EDP YES MIKEY PPCPUVCCIO IVB PPDDR 1V35 LPCPLUS CONN YES LPCPLUS R YES KBD BL SANDWICH CAPS INT BTPWR S4 XDP XDP CPU BPM GPU 2P TPAD 5V LDO S5
D2_PVB	VREF:PROD,D_BKL:PROD,SENSOR_NONPROD:N
D2_PROGPARTS	SMC_PROG:FSB,BOOTROM_PROG:FSB,DPMUXMCU:PROG,TPAD_PSOC:PROG,TBTROM:PROG
D2_DEVEL:ENG	ALTERNATE IVB PPT XDP S0PGOOD ISL DPMUX DEBUG DDRVREF DAC VREF ENG M3 SENSOR NONPROD Y D BKL DEV
D2_DEVEL:FSB	ALTERNATE IVB PPT XDP
IVB_PPT_XDP	XDP CONN XDP PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4266	1	IVB S RBMP PRQ E1 2 3 45W 4+2 1 2 8M BGA	U1000	CRITICAL	CPU IVY 2 3GHZ
337S4267	1	IVB S RBMM PRQ E1 2 6 45W 4+2 1 2S 8M BGA	U1000	CRITICAL	CPU IVY 2 6GHZ
337S4268	1	IVB S RBMK PRQ E1 2 7 45W 4+2 1 2S 8M BGA	U1000	CRITICAL	CPU IVY 2 7GHZ
337S4269	1	PANTHER POINT C1 SLJ8C PRQ BD82HM77	U1800	CRITICAL	
337S4256	1	IC GPU NV GK107-GTX-PS-A2	U8000	CRITICAL	
338S1113	1	IC TBT CR-4C B1 PRQ C20 22R 12X12 FC-CSP	U3600	CRITICAL	TBTRTR PRQ
333S0622	32	IC SDRAM DDR3-1600 256MX8 78FBGA HYNIX C-DIE 38NM		CRITICAL	2G HYNIX 1600
333S0623	32	IC SDRAM DDR3-1600 256MX8 78FBGA SAMSUNG		CRITICAL	2G SAMSUNG 1600
333S0628	32	IC SDRAM DDR3-1600 256MX8 78FBGA D-DIE ELPIDA		CRITICAL	2G ELPIDA 1600
333S0625	32	IC SDRAM DDR3-1600 512MX8 78FBGA HYNIX		CRITICAL	4G HYNIX 1600
333S0624	32	IC SDRAM DDR3-1600 512MX8 78FBGA C-DIE SAMSUNG		CRITICAL	4G SAMSUNG 1600
333S0629	32	IC SDRAM DDR3-1600 512MX8 78FBGA B-DIE ELPIDA		CRITICAL	4G ELPIDA 1600
333S0630	4	IC SDRAM GDDR5 64MX32 A-DIE HYNIX	U8400 U8450 U8500 U8550	CRITICAL	FB 2G HYNIX A DIE
333S0631	4	IC SDRAM GDDR5 64MX32 D-DIE SAMSUNG	U8400 U8450 U8500 U8550	CRITICAL	FB 2G SAMSUNG
128S0264	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E		CRITICAL	PBUS_CAP:SANYO
128S0257	30	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D,LF		CRITICAL	PBUS_CAP:KEMET
725-1614	1	INSULATOR,SHORT,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:SANYO
725-1648	1	INSULATOR,TALL,REAR,MLB,D2	REAR_INSULATOR	CRITICAL	PBUS_CAP:KEMET
725-1568	1	INSULATOR,CPU,D2	CPU_INSULATOR	CRITICAL	
725-1569	1	INSULATOR,GPU,D2	GPU_INSULATOR	CRITICAL	
725-1621	1	INSULATOR,PCH,D2	PCH_INSULATOR	CRITICAL	
806-2897	2	CAN,COVER,2,J5	CAN_COVER1,CAN_COVER2	CRITICAL	
825-7697	1	TEXT,LABEL,MLB,D2	TEXT_LABEL	CRITICAL	
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	

PD Parts

Bar Code Labels / EEEE #'s (continued on CSA 6)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3V]	CRITICAL	EEEE:DY3V
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3W]	CRITICAL	EEEE:DY3W
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY3Y]	CRITICAL	EEEE:DY3Y
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY40]	CRITICAL	EEEE:DY40
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY43]	CRITICAL	EEEE:DY43
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY44]	CRITICAL	EEEE:DY44
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY45]	CRITICAL	EEEE:DY45
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY4C]	CRITICAL	EEEE:DY4C
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF1]	CRITICAL	EEEE:DRF1
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF4]	CRITICAL	EEEE:DRF4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDN]	CRITICAL	EEEE:DRDN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDW]	CRITICAL	EEEE:DRDW
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9H]	CRITICAL	EEEE:DT9H
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9D]	CRITICAL	EEEE:DT9D
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9F]	CRITICAL	EEEE:DT9F
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DT9G]	CRITICAL	EEEE:DT9G
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HN]	CRITICAL	EEEE:F0HN
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HR]	CRITICAL	EEEE:F0HR
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW4]	CRITICAL	EEEE:DYW4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HV]	CRITICAL	EEEE:F0HV
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HM]	CRITICAL	EEEE:F0HM
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYW5]	CRITICAL	EEEE:DYW5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HY]	CRITICAL	EEEE:F0HY
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0HT]	CRITICAL	EEEE:F0HT

Programmables

341S3584	1	IC TRKPD/KYBD CNTRLR DVB D2	U5701	CRITICAL	TPAD PSOC PROG
337S2983	1	IC TP PSOC QFN BLANK	U5701	CRITICAL	TPAD PSOC BLANK
341S3597	1	IC EEPROM CACTUS RIDGE (8 1) FSB D2	U3690	CRITICAL	TBTROM PROG
335S0865	1	EEPROM 256KBIT SPI SMHZ 1.8V 2X3QFN	U3690	CRITICAL	TBTROM BLANK
335S0852	1	IC GPU ROM D2 BLANK	U8701	CRITICAL	GPUROM BLANK
341S3565	1	IC EDP MUX-95C (RENESAS) V3 2.8 DVB D2	U9100	CRITICAL	DPMUXMCU PROG
337S4313	1	IC MCU H8S/2113 8X8MM TLP-145V	U9100	CRITICAL	DPMUXMCU BLANK

DRAM VREF Configs

BOM GROUP	BOM OPTIONS
VREF:PROD	VREFDQ:M1_M3,VREFCA:LDO
VREF:ENG_M3	VREFDQ:M1_M3,VREFCA:LDO_DAC
VREF:ENG_LDO	VREFDQ:M1_DAC,VREFCA:LDO_DAC

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_1G_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_1600_S	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_1G_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600	2G_SAMSUNG_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_SAMSUNG_1333	RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_2G_HYNIX_1600	2G_HYNIX_1600,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_4G_SAMSUNG_1600	4G_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_4G_HYNIX_1600	4G_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_2G_ELPIDA_1600_S	RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_ELPIDA_1600	2G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600	4G_ELPIDA_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

DEVELOPMENT/BASE BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3726	1	D2 MLB KEPLER DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM
085-4776	1	D2 MLB KEPLER FSB DEVEL BOM	DEVEL_FSB	CRITICAL	DEVEL_FSB_BOM
607-9546	1	D2 MLB KEPLER 2PHASE BASE BOM	BASE	CRITICAL	BASE_BOM
685-0016	1	PBUS PAIR,KEMET POSCAP,TALL MYLAR,D2	POSCAP_MYLAR	CRITICAL	POSCAP_MYLAR_PAIR

SMC

341S3308	1	IC SMC DEVELOPMENT-FSB A3 D2	U4900	CRITICAL	SMC PROG FSB
341S3309	1	IC SMC PVB A3 2 2F36 D2	U4900	CRITICAL	SMC PROG PVB

EFI ROM

341S3595	1	IC EFI ROM FSB D2	U6100	CRITICAL	BOOTROM PROG FSB

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0257	128S0264		ALL	Kemet alt to Sanyo
353S3527	353S3528		ALL	Pericom eDP MUX
353S3526	353S3528		ALL	TI eDP MUX
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0855	376S0613	VREFDQ:M1_M3	ALL	Diodes alt to Toshiba
376S1076	376S0634		ALL	Diodes alt to On Semi
376S0903	376S0796		ALL	Fairchild alt to Siliconix
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0434	197S0343		ALL	Epson Alt to TXC
197S0435	197S0343		ALL	NDK Alt to TXC
197S0432	197S0431		ALL	NDK Alt to Epson
197S0452	197S0181		ALL	Epson Alt to TXC
197S0453	197S0181		ALL	NDK Alt to TXC
685-0017	685-0016		ALL	Sanyo POSCAP/Mylar alt to Kemet
376S0975	376S1081		ALL	Toshiba alt to diodes
371S0709	371S0652		ALL	NXP alt to infineon
371S0713	371S0558		ALL	DDS alt to ST
377S0126	377S0066		ALL	New Semtech package
377S0147	377S0066		ALL	On Semi alt to Semtech
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S0583		ALL	Panasonic alt to TDK
107S0232	107S0129		ALL	Cyntec alt to TFT
197S0466	197S0464		ALL	Epson alt to NDK
341S3564	341S3565		ALL	Avnet eDP MUX alt to Renesas

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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BOM Variants (continued from CSA 5)

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3382	PCBA,2.3G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DY41	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DY41,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3383	PCBA,2.3G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DY42	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DY42,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3445	PCBA,2.3G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DYJ5	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_HYNIX_A_DIE,EEEE:DYJ5,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3446	PCBA,2.3G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DYJ6	BASE_BOM,CPU_IVY:2_3GHZ,FB_2G_SAMSUNG,EEEE:DYJ6,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2818	PCBA,2.6G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRF0	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRF0,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2820	PCBA,2.6G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDP	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDP,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-2823	PCBA,2.6G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,DRDT	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_HYNIX_A_DIE,EEEE:DRDT,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-2819	PCBA,2.6G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,DRDQ	BASE_BOM,CPU_IVY:2_6GHZ,FB_2G_SAMSUNG,EEEE:DRDQ,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3632	PCBA,2.7G,8G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0JD	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0JD,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3633	PCBA,2.7G,8G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0J3	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0J3,DEVEL_BOM,RAM_2G_ELPIDA_1600
639-3630	PCBA,2.7G,16G_ELP,VRAM_HYN,MLB_KEPLER,D2,F0J4	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_HYNIX_A_DIE,EEEE:F0J4,DEVEL_BOM,RAM_4G_ELPIDA_1600
639-3631	PCBA,2.7G,16G_ELP,VRAM_SAM,MLB_KEPLER,D2,F0JC	BASE_BOM,CPU_IVY:2_7GHZ,FB_2G_SAMSUNG,EEEE:F0JC,DEVEL_BOM,RAM_4G_ELPIDA_1600

Bar Code Labels / EEEE #’s (continued from CSA 5)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY41]	CRITICAL	EEEE:DY41
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DY42]	CRITICAL	EEEE:DY42
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ5]	CRITICAL	EEEE:DYJ5
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DYJ6]	CRITICAL	EEEE:DYJ6
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRF0]	CRITICAL	EEEE:DRF0
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDP]	CRITICAL	EEEE:DRDP
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDT]	CRITICAL	EEEE:DRDT
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:DRDQ]	CRITICAL	EEEE:DRDQ
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JD]	CRITICAL	EEEE:F0JD
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J3]	CRITICAL	EEEE:F0J3
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0J4]	CRITICAL	EEEE:F0J4
825-7563	1	LABEL,MLB/LIO,MBA	[EEEE:F0JC]	CRITICAL	EEEE:F0JC

Elipda DQ’d
Keeping for PRQ

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: BOM Variants

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

BRANCH:

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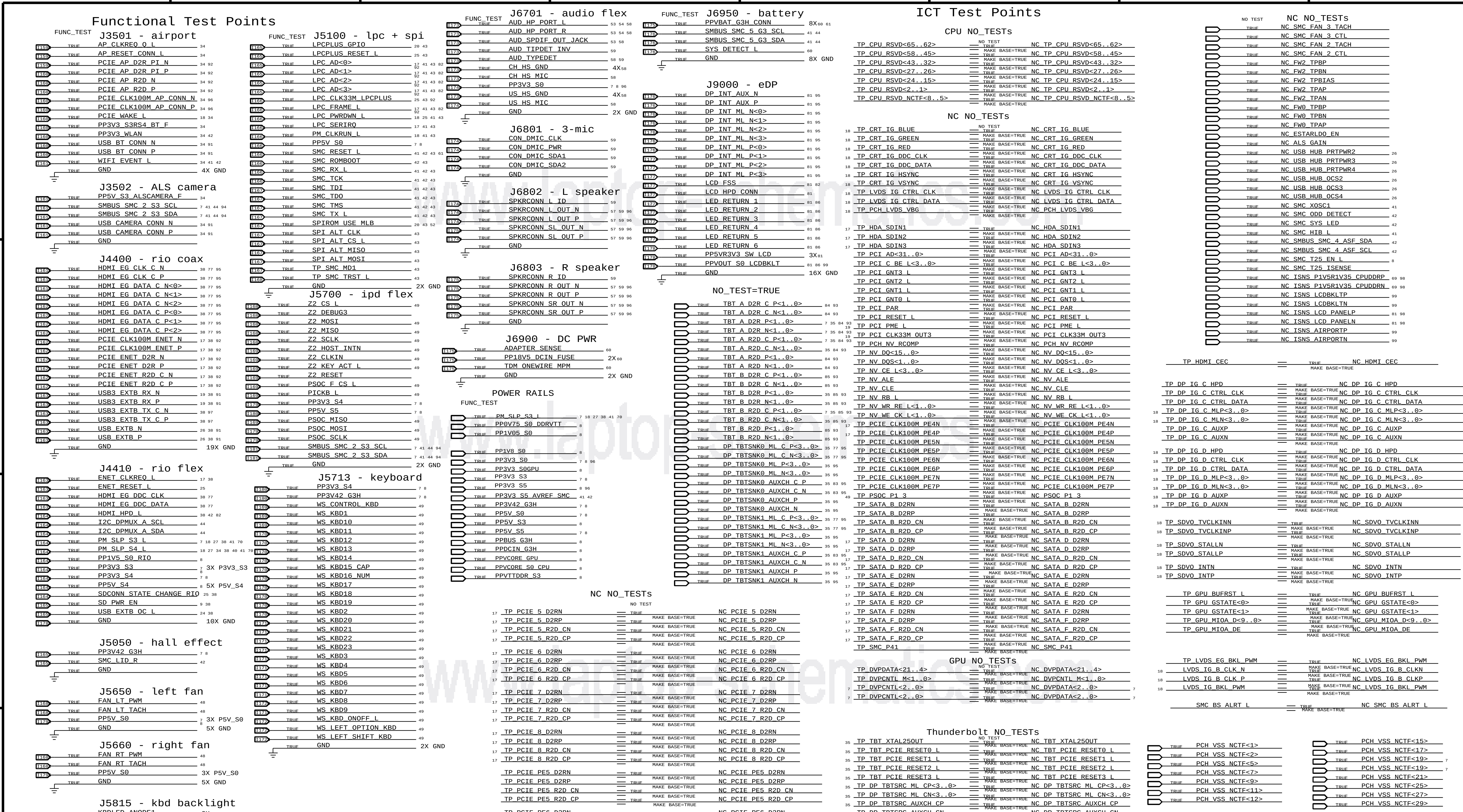

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Functional / ICT Test

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

G3H Rails

=PPBUS_G3H
PPBUS_G3H
MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 25 mm VOLTAGE 12 8V MAKE BASE TRUE
=PPBUS_S0_LCDBKLT
=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_GPU_ISNS_R
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 25 mm VOLTAGE 12 8V MAKE BASE TRUE
=PPVIN_S0_CPUIMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_CPUVCCIOS0
=PPVIN_S0_CPUAXG
=PPVIN_S0_VCCSAS0
=PPVIN_S0_PCHVCCIOS0

=PPVIN_S5_HS_GPU_ISNS
PPVIN_S5_HS_GPU_ISNS
MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 25 mm VOLTAGE 12 8V MAKE BASE TRUE
=PPVIN_S0_GFXIMVP
=PPVIN_S0GPU_P1V5P1V0

=PPVIN_S5_HS_OTHER_ISNS
PPVIN_S5_HS_OTHER_ISNS
MIN LINE WIDTH 0 6 mm MIN NECK WIDTH 0 25 mm VOLTAGE 12 8V MAKE BASE TRUE
=PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN
PPDCIN_G3H
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 25 MM VOLTAGE 18 5V MAKE BASE TRUE
=PPDCIN_S5_CHGR

=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 25 MM VOLTAGE 18 5V MAKE BASE TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

=PP3V42_G3H_REG
PP3V42_G3H
MIN LINE WIDTH 0 3 MM MIN NECK WIDTH 0 2 MM VOLTAGE 3 42V MAKE BASE TRUE
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMC
=PP3V42_G3H_CHGR
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TPAD
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK

=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL
For PCH RTC Power

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN LINE WIDTH 0 3 MM MIN NECK WIDTH 0 2 MM VOLTAGE 3 42V MAKE BASE TRUE
=PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO
PP5V_S5
MIN LINE WIDTH 0 5 MM MIN NECK WIDTH 0 1 MM VOLTAGE 5V MAKE BASE TRUE
=PP5V_S5_P1V5S3RS0FET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD

=PP5V_SUS_FET
PP5V_SUS
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 5V MAKE BASE TRUE
=PP5V_SUS_PCH

=PP5V_S4_REG
PP5V_S4
MIN LINE WIDTH 0 5 MM MIN NECK WIDTH 0 2 MM VOLTAGE 5V MAKE BASE TRUE
=PP5V_S4_RIO
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_ISNS
=PP5V_S4_TPAD
=PP5V_S4_AUDIO

=PP5V_S3_FET
PP5V_S3
MIN LINE WIDTH 0 5 mm MIN NECK WIDTH 0 2 mm VOLTAGE 5V MAKE BASE TRUE
=PP5V_S3_ISNS
=PP5V_S3_ALSCAMERA
=PP5V_S3_DDRREG
=PP5V_S3_DEBUG_ADC_AVDD
=PP5V_S3_DEBUG_ADC_DVDD
=PP5V_S3_DEBUG_ISNS
=PP5V_S3_MEMRESET

=PP5V_S0_FET
PP5V_S0
MIN LINE WIDTH=0 4 MM MIN NECK WIDTH=0 2 MM VOLTAGE=5V MAKE BASE=TRUE
=PP5V_S0GPU_P1V0P1V35_GPU
=PP5V_S0_P1V5_LDO
=PP5V_S0_AUDIO_XW
=PP5V_S0_BKL
=PP5V_S0_CPUIMVP
=PP5V_S0_CPUVCCIOS0
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_GFXIMVP
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_PCHVCCIOS0
=PP5V_S0_RMC
=PP5V_S0_VCCSAS0
=PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET
PP3V3_S4
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 1 MM VOLTAGE 3 3V MAKE BASE TRUE
=PP3V3_S4_TBT_R
=PP3V3_S4_TPAD
=PP3V3_S4_SMC
=PP3V3_S4_RIO
=PP3V3_S4_BT

=PP3V3_SUS_FET
PP3V3_SUS
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM MAKE BASE TRUE
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_CNTRL
=PP3V3_SUS_SMC

=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCC_SPI

=PP3V3_S5_REG
PP3V3_S5
MIN LINE WIDTH=0 6 MM MIN NECK WIDTH=0 2 MM VOLTAGE=3 3V MAKE BASE=TRUE
=PP3V3_GPU_P3V3GPUFET
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_DPAPWRSW
=PP3V3_S4_DPBPWRSW
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_P1V2P1V8
=PP3V3_S5_P1V5S0
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SMCBATLOW
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_XDP
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW

=PP3V3_S3_FET
PP3V3_S3
MIN LINE WIDTH=0 50MM MIN NECK WIDTH=0 20MM VOLTAGE=3 3V MAKE BASE=TRUE
=PP3V3_S3_BT
=PP3V3_S3_DPMUX_UC
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_PCH_GPIO
=PP3V3_S3_RIO
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_SMBUS_SMC_3
=PP3V3_S3_TPAD
=PP3V3_S3_USBMUX
=PP3V3_S3_USB_HUB
=PP3V3_S3_USB_RESET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_GYRO
=PP3V3_S3_SMS
=PP3V3_S3_SDBUF

=PP3V3_S0_FET
PP3V3_S0
MIN LINE WIDTH=0 5 MM MIN NECK WIDTH=0 075 mm VOLTAGE=3 3V MAKE BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_DPMUX
=PP3V3_S0_DPMUXI2C
=PP3V3_S0_DPMUX_UC
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_IMVPISNS
=PP3V3_S0_ISNS
=PP3V3_S0_LCD
=PP3V3_S0_P1V8GPUFET
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SATAMUX
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD
=PP3V3_S0_SYSCLK
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_TPAD
=PP3V3_S0_VMON
=PP3V3_S0_X29THMSNS
=PP3V3_S0_XDP
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS

TBT RAILS

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN LINE WIDTH 0 4 MM VOLTAGE 3 3V MIN NECK WIDTH 0 15 MM MAKE BASE TRUE
=PP3V3_TBT_PCH_GPIO
=PPVDDIO_TBT_CLK
=PP3V3_TBTLC_RTR

=PP1V05_TBTLC_FET
PP1V05_TBTLC
MIN LINE WIDTH 0 4 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 05V MAKE BASE TRUE
=PP1V05_TBTLC_RTR

=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
MIN LINE WIDTH 0 4 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 05V MAKE BASE TRUE
=PP1V05_TBTCIO_RTR

=PP15V_TBT_REG
PP15V_TBT
MIN LINE WIDTH 0 4 MM MIN NECK WIDTH 0 2 MM VOLTAGE 15V MAKE BASE TRUE
=PPHV_SW_TBTAPWRSW
=PPHV_SW_TBTBPWRSW

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG
4A max supply
PP1V8_S0
MIN LINE WIDTH=0 6 MM MIN NECK WIDTH=0 2 MM VOLTAGE=1 5V MAKE BASE=TRUE
=PP1V8R1V5_S0_PCH_VCCVRM
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_GPUFET
=PP1V8_S0_PCH_VCCTX_LVDS
=PP1V8_S0_PCH_VCC_DFTERM
=PPVDDIO_S0_SBCLK
=PP1V8_S0_P1V5_LDO

=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
MIN LINE WIDTH=0 5 MM MIN NECK WIDTH=0 2 MM VOLTAGE=1 8V MAKE BASE=TRUE

=PPDDR_S3_REG
PP1V5R1V35_S3
MIN LINE WIDTH=0 2 mm MIN NECK WIDTH=0 17 mm VOLTAGE=1 5V MAKE BASE=TRUE
=PP1V5_S3_MEMRESET
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V5R1V35_MEM
MIN LINE WIDTH=0 2 mm MIN NECK WIDTH=0 17 mm VOLTAGE=1 5V MAKE BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B

=PP1V5_S3RS0_FET_ISNS
PP1V5_S3RS0_CPUDDR
MIN LINE WIDTH=0 6 MM MIN NECK WIDTH=0 2 MM VOLTAGE=1 5V MAKE BASE=TRUE
=PP1V5_S3RS0_VMON
=PP1V5_S3_CPU_VCCDDR

=PP1V5_S0_REG
PP1V5_S0
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 5V MAKE BASE TRUE
=PP1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA

=PP1V5_S0_RIO_LDO
PP1V5_S0_RIO
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 5V MAKE BASE TRUE
=PP1V5_S0_RIO

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN LINE WIDTH=0 3 MM MIN NECK WIDTH=0 2 MM VOLTAGE=0 75V MAKE BASE=TRUE

=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
MIN LINE WIDTH=2 mm MIN NECK WIDTH=0 17 mm VOLTAGE=0 75V MAKE BASE=TRUE
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN LINE WIDTH=0 4 MM MIN NECK WIDTH=0 2 MM VOLTAGE=1 05V MAKE BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG
PP1V05_S0
MIN LINE WIDTH=0 6 MM MIN NECK WIDTH=0 2 MM VOLTAGE=1 05V MAKE BASE=TRUE
=PP1V05_S0_CPU_VCCIO
=PPVCCIO_S0_XDP
=PPVCCIO_S0_CPUIMVP
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PP1V05_S0_RMC

=PPPCHVCCIO_S0_REG
PP1V05_PCHVCCIO_S0
MIN LINE WIDTH=0 6 MM MIN NECK WIDTH=0 2 MM VOLTAGE=1 05V MAKE BASE=TRUE
=PP1V05_S0_PCH_VCCIO_PLLPCIE
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCCIO_PLLUSB
=PP1V05_S0_PCH_VCC_DMI
=PP1V05_S0_PCH_VCCDMI_FDI
=PP1V05_S0_P1V05TBTFET_R

Defined here since TBT page does not know PBUS voltage
IGEN PPVIN_SW_TBTBST
VOLTAGE 12 8V

Backlight Rails

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN LINE WIDTH 0 5 MM MIN NECK WIDTH 0 25 MM MAKE BASE TRUE VOLTAGE 12 6V
PPBUS_S0_LCDBKLT_PWR

SMC_T25_EN_L
NC_SMC_T25_EN_L
MAKE BASE TRUE

=PP1V05_S0_P1V05TBTFET
PP1V05_S0_P1V05TBTFET
MIN LINE WIDTH 0 4 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 05V MAKE BASE TRUE

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN LINE WIDTH 0 3 MM MIN NECK WIDTH 0 10MM VOLTAGE 3 3V MAKE BASE TRUE
=PP3V3_GPU_IFPX_PLLVDD
=PP3V3_S0_GFX3V3BIAS
=PP3V3_GPU_VDD33

=PP3V3_S0GPU_MISC_FET
PP3V3_S0GPU_MISC
MIN LINE WIDTH 0 3 MM MIN NECK WIDTH 0 10MM VOLTAGE 3 3V MAKE BASE TRUE
=PP3V3_GPU_MISC

TP_P1V8GPU_EN
=P1V8GPU_EN

=PP1V5R1V35_GPU_REG
PP1V5R1V35_S0GPU
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 5V MAKE BASE TRUE
=PP1V35_GPU_FBVDDQ
=PP1V35_GPU_S0_FB

=PP1V8_GPU_FET
TP_GPU_PGOOD2
MAKE BASE TRUE

=PP1V05_S0GPU_REG
PP1V0_S0GPU_ISNS
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 05V MAKE BASE TRUE
=PP1V0_GPU_DPLL
=PP1V0_GPU_DP_AB
=PP1V0_GPU_DP_CD
=PP1V05_GPU_IFPCD_IOVDD
=PP1V05_GPU_IFPEF_IOVDD
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 0V MAKE BASE TRUE
=PPVCORE_GPU
=PPVCORE_S0_GFX_REG

GND
=LVDS_VCCA
MIN LINE WIDTH=0 6MM MIN NECK WIDTH=0 08SMM VOLTAGE=0V MAKE BASE TRUE

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 25 MM MAKE BASE TRUE VOLTAGE 1 25V
=PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM MAKE BASE TRUE VOLTAGE 1 05V
=PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM MAKE BASE TRUE VOLTAGE 1 5V

=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 1 05V MAKE BASE TRUE

=PPVCCSA_S0_REG
PPVCCSA_S0_REG
MIN LINE WIDTH 0 6 MM MIN NECK WIDTH 0 2 MM VOLTAGE 0 9V MAKE BASE TRUE
=PPVCCSA_S0_CPU

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
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Frame Holes

ZT0915 2.8R2.3 — GND_BATT_CHGND

ZT0950 TH-NSP — GND_CHASSIS_FAN — SL-2.3X3.9-2.9X4.5

ZT0974 TH-NSP — GND_CHASSIS_MLBCAN5 — SL-1.1X0.45-1.1x4x0.75

ZT0975 TH-NSP — GND_CHASSIS_MLBCAN6 — SL-1.1X0.45-1.1x4x0.75

GND (MAKE BASE TRUE) — GND_CHASSIS_MLBCAN4

ZT0970 TH-NSP — GND_CHASSIS_MLBCAN1 — SL-1.1X0.45-1.4x0.75

ZT0971 TH-NSP — GND_CHASSIS_MLBCAN2 — SL-1.1X0.45-1.4x0.75

ZT0972 TH-NSP — GND_CHASSIS_MLBCAN3 — SL-1.1X0.45-1.4x0.75

ZT0973 TH-NSP — SL-1.1X0.45-1.4x0.75

THERMAL MODULE STANDOFFS

SH0920 STDOFF-4.5OD2.15H-SM

SH0927 STDOFF-4.5OD2.15H-SM

SH0926 STDOFF-4.5OD2.15H-SM

SH0928 STDOFF-4.5OD2.15H-SM

SH0921 STDOFF-4.5OD2.15H-SM-1

SH0929 STDOFF-4.5OD2.15H-SM

SH0925 STDOFF-4.5OD1.8H-SM

SH0923 STDOFF-4.5OD1.8H-SM

SH0922 STDOFF-4.5OD2.15H-SM

SH0930 STDOFF-4.5OD2.15H-SM

SH0924 STDOFF-4.5OD1.9H-SM

SH0946 STDOFF-4.9OD2.38H-SM-2

SH0945 STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

APN 806-2247

SH0950 SM — SHLD-J5-USB

SH0952 SM — SHLD-J5-CAN-FENCE-MDP-2

SH0951 SM — SHLD-J5-CAN-FENCE-MDP-1

BR0901 MLB-MTG-BRKT-J5

POGO PINS

SH0931 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0932 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0933 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0934 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0935 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0936 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0940 2.8OD1.2ID-1.35H-SM

SH0941 2.8OD1.2ID-1.35H-SM

SH0944 2.8OD1.2ID-1.35H-SM

SH0942 2.8OD1.2ID-1.35H-SM

SH0943 2.8OD1.2ID-1.35H-SM

SMT GND TEST PONTS

ZT0990 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0991 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0992 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0993 2.1SM2.0MM-CIR SMT-PAD-NSP

SH0937 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0960 2.8OD1.2ID-1.35H-SM

SH0961 2.8OD1.2ID-1.35H-SM

Digital Ground

MLB_RAMCFG3 — RAMCFG3:L R0913 1K 5% 1/20W MF 201

MLB_RAMCFG2 — RAMCFG2:L R0912 1K 5% 1/20W MF 201

MLB_RAMCFG1 — RAMCFG1:L R0911 1K 5% 1/20W MF 201

MLB_RAMCFG0 — RAMCFG0:L R0910 1K 5% 1/20W MF 201

T29 / GMUX JTAG Signals

TBT_LSOE<3> — TBT_LSEO_LSOE3 (MAKE BASE TRUE, NO TEST TRUE) — TBT_LSEO<3>

TBT_LSOE<2> — TBT_LSEO_LSOE2 (MAKE BASE=TRUE, NO TEST=TRUE) — TBT_LSEO<2>

GMUX ALIASES

82 EG_RESET_L (MAKE BASE=TRUE) — GPU_RESET_L 71 78

18 LVDS_IG_BKL_ON (MAKE BASE=TRUE) — IG_BKLT_EN 82

18 LVDS_IG_PANEL_PWR (MAKE BASE=TRUE) — IG_LCD_PWR_EN 82

PEX_CLKREQ_L (MAKE BASE=TRUE) — EG_CLKREQ_IN_L 78 82

17 PEG_CLKREQ_L (MAKE BASE=TRUE) — EG_CLKREQ_OUT_L 82

82 DP_TBTSNK0_HPD_IG (MAKE BASE=TRUE) — DPA_IG_HPD 18 82

82 DP_TBTSNK1_HPD_IG (MAKE BASE=TRUE) — DPB_IG_HPD 18 82

17 PCIE_EXCARD_D2R_N (MAKE BASE=TRUE) — NC_PCIE_EXCARD_D2R_N

17 PCIE_EXCARD_D2R_P (MAKE BASE=TRUE) — NC_PCIE_EXCARD_D2R_P

17 PCIE_EXCARD_R2D_C_N (MAKE BASE=TRUE) — NC_PCIE_EXCARD_R2D_C_N

17 PCIE_EXCARD_R2D_C_P (MAKE BASE=TRUE) — NC_PCIE_EXCARD_R2D_C_P

92 17 PCIE_CLK100M_EXCARD_N (MAKE BASE=TRUE) — NC_PCIE_CLK100M_EXCARD_N

92 17 PCIE_CLK100M_EXCARD_P (MAKE BASE=TRUE) — NC_PCIE_CLK100M_EXCARD_P

17 TP_PCH_CLKOUT_DPN (MAKE BASE=TRUE) — DPLL_REF_CLKN 11 89

17 TP_PCH_CLKOUT_DPP (MAKE BASE=TRUE) — DPLL_REF_CLKP 11 89

17 TP_PCH_GPIO64_CLKOUTFLEX0 (MAKE BASE=TRUE) — NC_PCH_GPIO64_CLKOUTFLEX0

17 TP_PCH_GPIO65_CLKOUTFLEX1 (MAKE BASE=TRUE) — NC_PCH_GPIO65_CLKOUTFLEX1

17 TP_PCH_GPIO66_CLKOUTFLEX2 (MAKE BASE=TRUE) — NC_PCH_GPIO66_CLKOUTFLEX2

17 TP_PCH_GPIO67_CLKOUTFLEX3 (MAKE BASE=TRUE) — NC_PCH_GPIO67_CLKOUTFLEX3

SD_PWR_EN_PCH (MAKE BASE=TRUE) — ENET_LOW_PWR_PCH 20 24 25

38 7 SD_PWR_EN (MAKE BASE=TRUE) — ENET_LOW_PWR 25

TP_FW_PWR_EN (MAKE BASE=TRUE) — FW_PWR_EN 25

CPU signals

CPU_VID<0..6> (MAKE BASE=TRUE) — CPUIMVP_VID<0..6>

27 MEMVTT_EN (MAKE BASE=TRUE) — =DDRVTT_EN 27 64

TP_CPU_VTT_SELECT (MAKE BASE=TRUE) — CPU_VTTSELECT

Unused PEG signals

NC_PEG_D2R_P<15..14> (MAKE BASE=TRUE, NO TEST=TRUE) — =PEG_D2R_P<15..14> 10

NC_PEG_D2R_N<15..14> (MAKE BASE=TRUE, NO TEST=TRUE) — =PEG_D2R_N<15..14> 10

NC_PEG_R2D_C_P<15..14> (MAKE BASE=TRUE, NO TEST=TRUE) — =PEG_R2D_C_P<15..14> 10

NC_PEG_R2D_C_N<15..14> (MAKE BASE=TRUE, NO TEST=TRUE) — =PEG_R2D_C_N<15..14> 10

T29 Signals Through PEG

92 35 PCIE_TBT_D2R_P<3..0> (MAKE BASE=TRUE) — =PEG_D2R_P<11..8> 10

92 35 PCIE_TBT_D2R_N<3..0> (MAKE BASE=TRUE) — =PEG_D2R_N<11..8> 10

92 35 PCIE_TBT_R2D_C_P<3..0> (MAKE BASE=TRUE) — =PEG_R2D_C_P<11..8> 10

92 35 PCIE_TBT_R2D_C_N<3..0> (MAKE BASE=TRUE) — =PEG_R2D_C_N<11..8> 10

GPU signals

89 88 71 PEG_D2R_P<7..0> (MAKE BASE=TRUE) — =PEG_D2R_P<7..0> 10

89 88 71 PEG_D2R_N<7..0> (MAKE BASE=TRUE) — =PEG_D2R_N<7..0> 10

89 71 PEG_R2D_C_P<7..0> (MAKE BASE=TRUE) — =PEG_R2D_C_P<7..0> 10

89 71 PEG_R2D_C_N<7..0> (MAKE BASE=TRUE) — =PEG_R2D_C_N<7..0> 10

UNUSED TBT PORTS

TBT_D2R_P<3..2> — NC_TBT_D2RP<3..2> (MAKE BASE=TRUE, NO TEST=TRUE)

TBT_D2R_N<3..2> — NC_TBT_D2RN<3..2> (MAKE BASE=TRUE, NO TEST=TRUE)

TBT_R2D_C_P<3..2> — NC_TBT_R2D_CP<3..2> (MAKE BASE=TRUE, NO TEST=TRUE)

TBT_R2D_C_N<3..2> — NC_TBT_R2D_CN<3..2> (MAKE BASE=TRUE, NO TEST=TRUE)

DPMUX TX & RX

82 DPMUX_UC_BOOT_TX (MAKE BASE=TRUE) — DPMUX_UC_TX 82

82 DPMUX_UC_BOOT_RX (MAKE BASE=TRUE) — DPMUX_UC_RX 82

SSD PCIE SIGNALS

92 39 PCIE_SSD_D2R_P<1..0> (MAKE BASE=TRUE) — =PEG_D2R_P<13..12> 10

92 39 PCIE_SSD_D2R_N<1__0> (MAKE BASE=TRUE) — =PEG_D2R_N<13__12> 10

92 39 PCIE_SSD_R2D_C_P<1..0> (MAKE BASE=TRUE) — =PEG_R2D_C_P<13..12> 10

92 39 PCIE_SSD_R2D_C_N<1..0> (MAKE BASE=TRUE) — =PEG_R2D_C_N<13..12> 10

TP_PCIE_CLK100M_FW_P (MAKE BASE=TRUE) — PCIE_CLK100M_FW_P 17 92

TP_PCIE_CLK100M_FW_N (MAKE BASE=TRUE) — PCIE_CLK100M_FW_N 17 92

UNUSED FDI SIGNALS

NC_PCH_FDI_DATA_N<7..0> (MAKE BASE=TRUE, NO TEST=TRUE) — =FDI_DATA_N<7..0> 18

NC_PCH_FDI_DATA_P<7..0> (MAKE BASE=TRUE, NO TEST=TRUE) — =FDI_DATA_P<7..0> 18

NC_PCH_FDI_FSYNC<1..0> (MAKE BASE=TRUE, NO TEST=TRUE) — =FDI_FSYNC<1..0> 18

NC_PCH_FDI_LSYNC<1..0> (MAKE BASE=TRUE, NO TEST=TRUE) — =FDI_LSYNC<1..0> 18

NC_CPU_FDI_DATA_N<7..0> (MAKE BASE=TRUE, NO TEST=TRUE) — FDI_DATA_N<7..0> 10 89

NC_CPU_FDI_DATA_P<7..0> (MAKE BASE=TRUE, NO TEST=TRUE) — FDI_DATA_P<7..0> 10 89

NC_CPU_FDI_FSYNC<1..0> (MAKE BASE=TRUE, NO TEST=TRUE) — FDI_FSYNC<1..0> 10 89

NC_CPU_FDI_LSYNC<1..0> (MAKE BASE=TRUE, NO TEST=TRUE) — FDI_LSYNC<1..0> 10 89

USB SIGNALS

91 34 USB_BT_P (MAKE BASE=TRUE) — USBHUB_DN1_P 26

91 34 USB_BT_N (MAKE BASE=TRUE) — USBHUB_DN1_N 26

91 49 USB_TPAD_P (MAKE BASE=TRUE) — USBHUB_DN2_P 26

91 49 USB_TPAD_N (MAKE BASE=TRUE) — USBHUB_DN2_N 26

91 41 USB_SMC_P (MAKE BASE=TRUE) — USBHUB_DN3_P 26

91 41 USB_SMC_N (MAKE BASE=TRUE) — USBHUB_DN3_N 26

PU_USBHUB_DN4P (MAKE BASE=TRUE) — USBHUB_DN4_P 26

PU_USBHUB_DN4N (MAKE BASE=TRUE) — USBHUB_DN4_N 26

8 =PP5V_S0_AUDIO_XW

XW0902 SM — PP5V_S0_AUDIO_AMP_L 57
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
VOLTAGE=5V

XW0903 SM — PP5V_S0_AUDIO_AMP_R 57
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 2MM
VOLTAGE=5V

NC_LVDS_IG_A_DATAP<3> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_A_DATA_P<3> 18 91

NC_LVDS_IG_A_DATAN<3> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_A_DATA_N<3> 18 91

NC_LVDS_IG_B_DATAP<3> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_B_DATA_P<3> 18

NC_LVDS_IG_B_DATAN<3> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_B_DATA_N<3> 18

NC_LVDS_IG_A_CLK_N (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_A_CLK_N 18 91

NC_LVDS_IG_A_CLK_P (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_A_CLK_P 18 91

NC_LVDS_IG_A_DATA_N<2..0> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_A_DATA_N<2..0> 18 91

NC_LVDS_IG_A_DATA_P<2..0> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_A_DATA_P<2..0> 18 91

NC_LVDS_IG_B_DATA_N<2..0> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_B_DATA_N<2..0> 18 91

NC_LVDS_IG_B_DATA_P<2..0> (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_B_DATA_P<2..0> 18 91

NC_LVDS_IG_DDC_CLK (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_DDC_CLK 18

NC_LVDS_IG_DDC_DATA (MAKE BASE=TRUE, NO TEST=TRUE) — LVDS_IG_DDC_DATA 18

NC_PCIE_FW_D2RN (MAKE BASE=TRUE, NO TEST=TRUE) — PCIE_FW_D2R_N 17

NC_PCIE_FW_D2RP (MAKE BASE=TRUE, NO TEST=TRUE) — PCIE_FW_D2R_P 17

NC_PCIE_FW_R2D_CN (MAKE BASE=TRUE, NO TEST=TRUE) — PCIE_FW_R2D_C_N 17

NC_PCIE_FW_R2D_CP (MAKE BASE=TRUE, NO TEST=TRUE) — PCIE_FW_R2D_C_P 17

NC_SATA_ODD_D2R_N (MAKE BASE=TRUE) — SATA_ODD_D2R_N 17 91

NC_SATA_ODD_D2R_P (MAKE BASE=TRUE) — SATA_ODD_D2R_P 17 91

NC_SATA_ODD_R2D_C_N (MAKE BASE=TRUE) — SATA_ODD_R2D_C_N 17 91

NC_SATA_ODD_R2D_C_P (MAKE BASE=TRUE) — SATA_ODD_R2D_C_P 17 91

NC_DP_IG_MLP<3..0> (MAKE BASE=TRUE, NO TEST=TRUE) — TP_DP_IG_B_MLP<3..0> 18

NC_DP_IG_MLN<3..0> (MAKE BASE=TRUE, NO TEST=TRUE) — TP_DP_IG_B_MLN<3..0> 18

TBTBST:N

37 8 =PPVIN_SW_TBTBST — R0950 0 5% 1/8W MF LF 805 — =PP15V_TBT_REG 8 37

UNUSED USB SIGNALS

NC_USB3_EXTD_TX_P (MAKE BASE=TRUE, NO TEST=TRUE) — USB3_EXTD_TX_P 19

NC_USB3_EXTD_TX_N (MAKE BASE=TRUE, NO TEST=TRUE) — USB3_EXTD_TX_N 19

NC_USB3_EXTD_RX_P (MAKE BASE=TRUE, NO TEST=TRUE) — USB3_EXTD_RX_P 19

NC_USB3_EXTD_RX_N (MAKE BASE=TRUE, NO TEST=TRUE) — USB3_EXTD_RX_N 19

NC_USB_EXTD_EHCI_P (MAKE BASE=TRUE, NO TEST=TRUE) — USB_EXTD_EHCI_P 19

NC_USB_EXTD_EHCI_N (MAKE BASE=TRUE, NO TEST=TRUE I1187) — USB_EXTD_EHCI_N 19

NC_USB3_EXTC_TX_P (MAKE BASE=TRUE, NO TEST=TRUE I1188) — USB3_EXTC_TX_P 19 91

NC_USB3_EXTC_TX_N (MAKE BASE=TRUE, NO TEST=TRUE I1189) — USB3_EXTC_TX_N 19 91

NC_USB3_EXTC_RX_P (MAKE BASE=TRUE, NO TEST=TRUE I1190) — USB3_EXTC_RX_P 19 91

NC_USB3_EXTC_RX_N (MAKE BASE=TRUE, NO TEST=TRUE I1192) — USB3_EXTC_RX_N 19 91

NC_USB_EXTC_P (MAKE BASE=TRUE, NO TEST=TRUE I1191) — USB_EXTC_P 19 91

NC_USB_EXTC_N (MAKE BASE=TRUE, NO TEST=TRUE) — USB_EXTC_N 19 91

SYNC_MASTER=D2_KEPLER — SYNC_DATE=01/13/2012

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-9589 — SIZE: D

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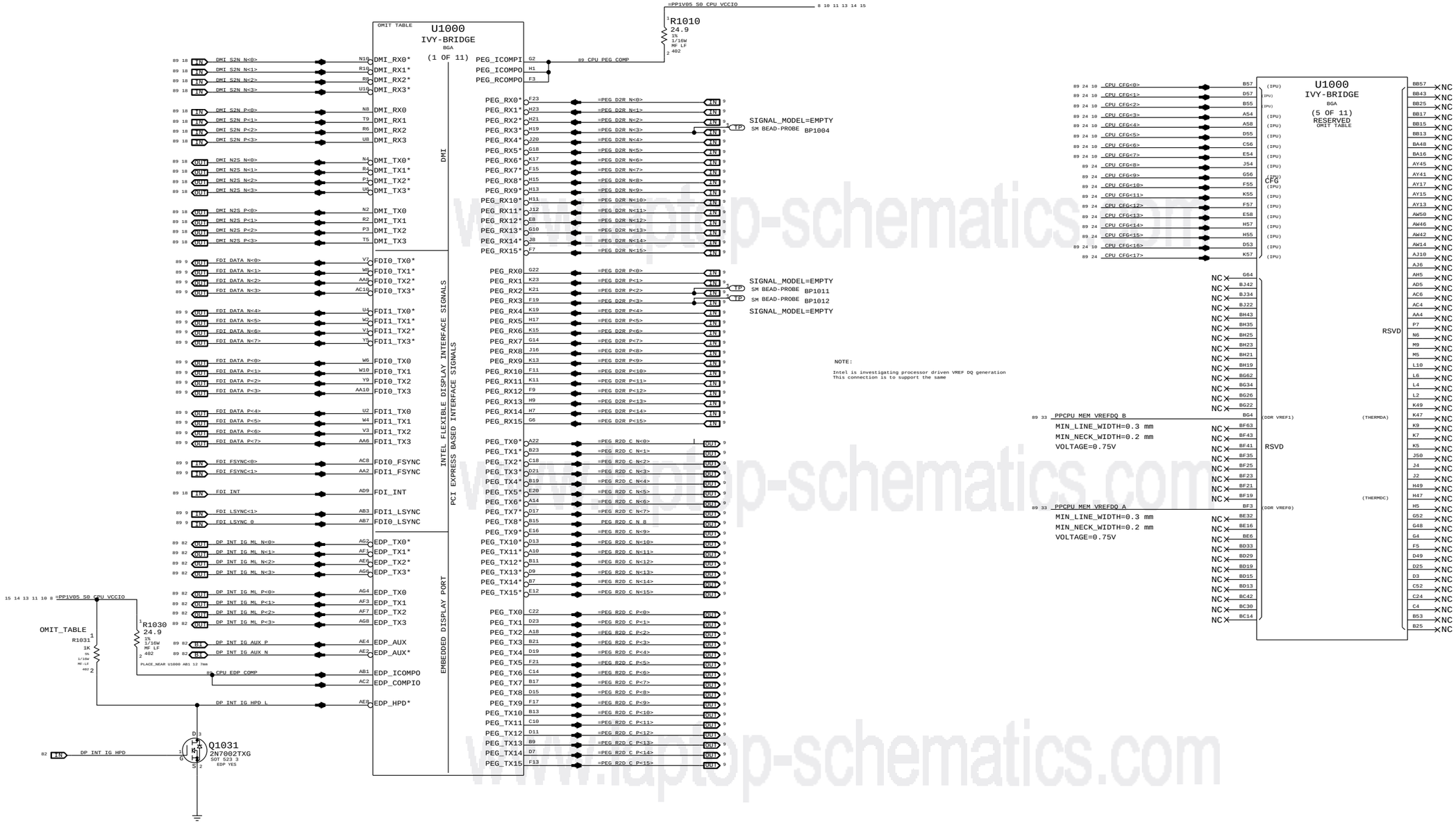

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES MTL FILM 1/16W 1K 0402 SMD LF	R1031		EDP:YES
116S0090	1	RES MTL FILM 1/16W 10K 0402 SMD LF	R1031		EDP:NO

```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION   0 = LANES REVERSED
```

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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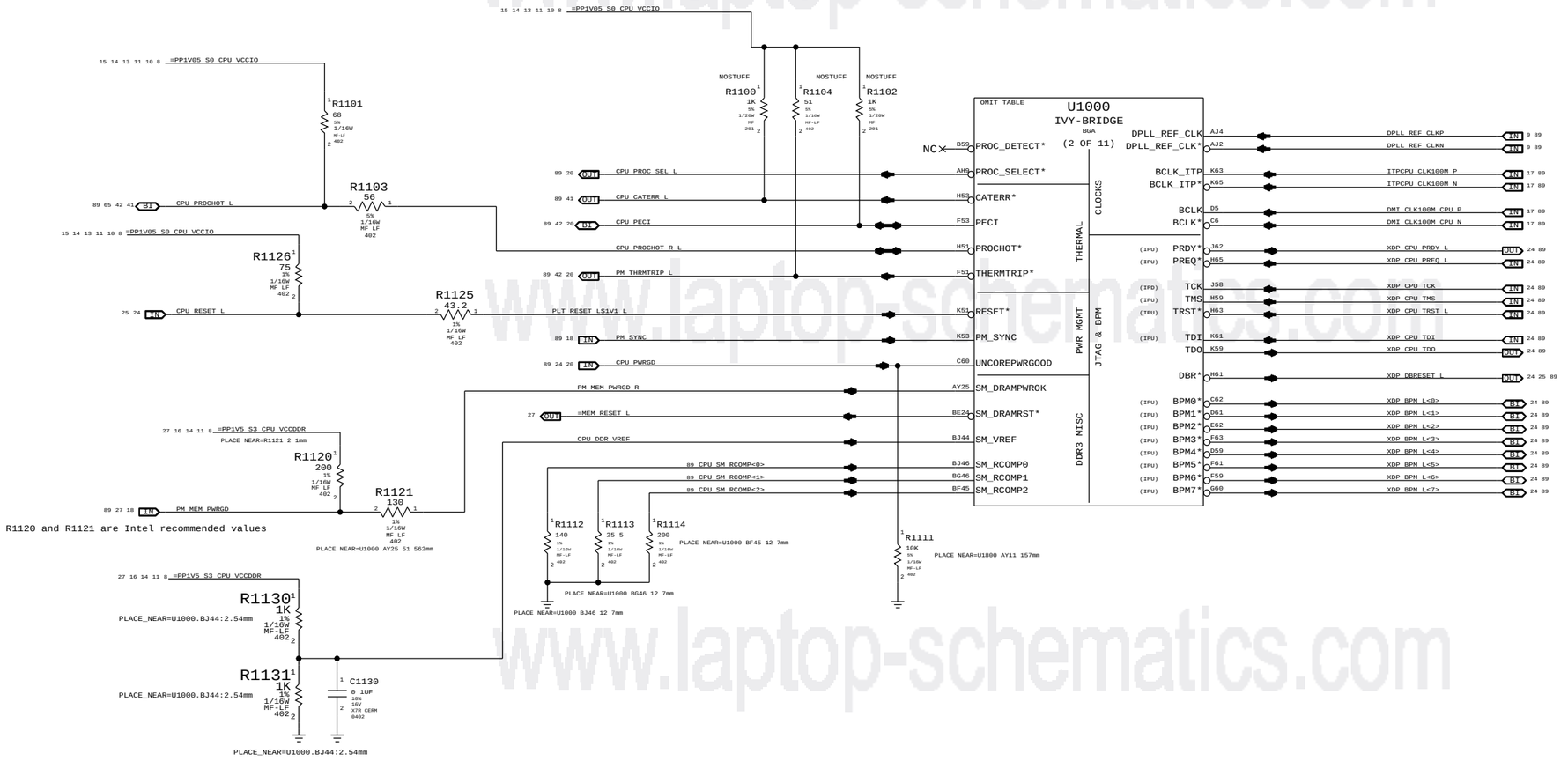

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

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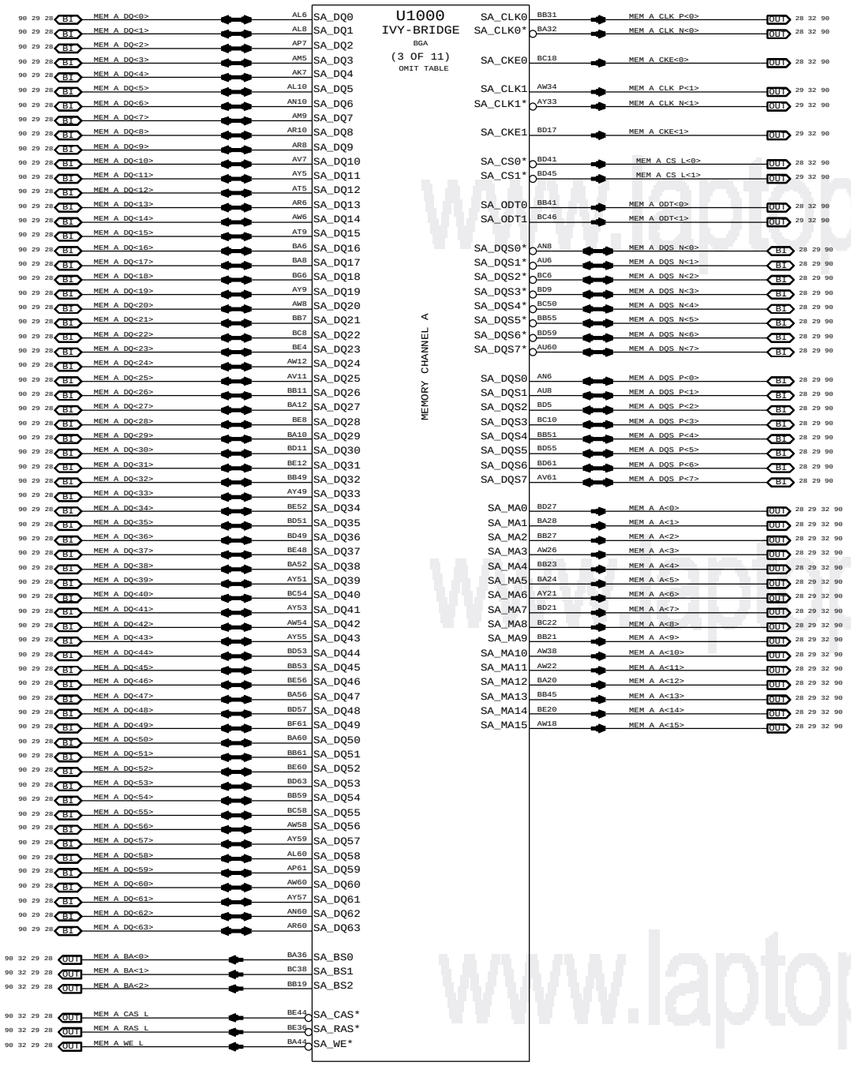

SYNC DATE=01/13/2012

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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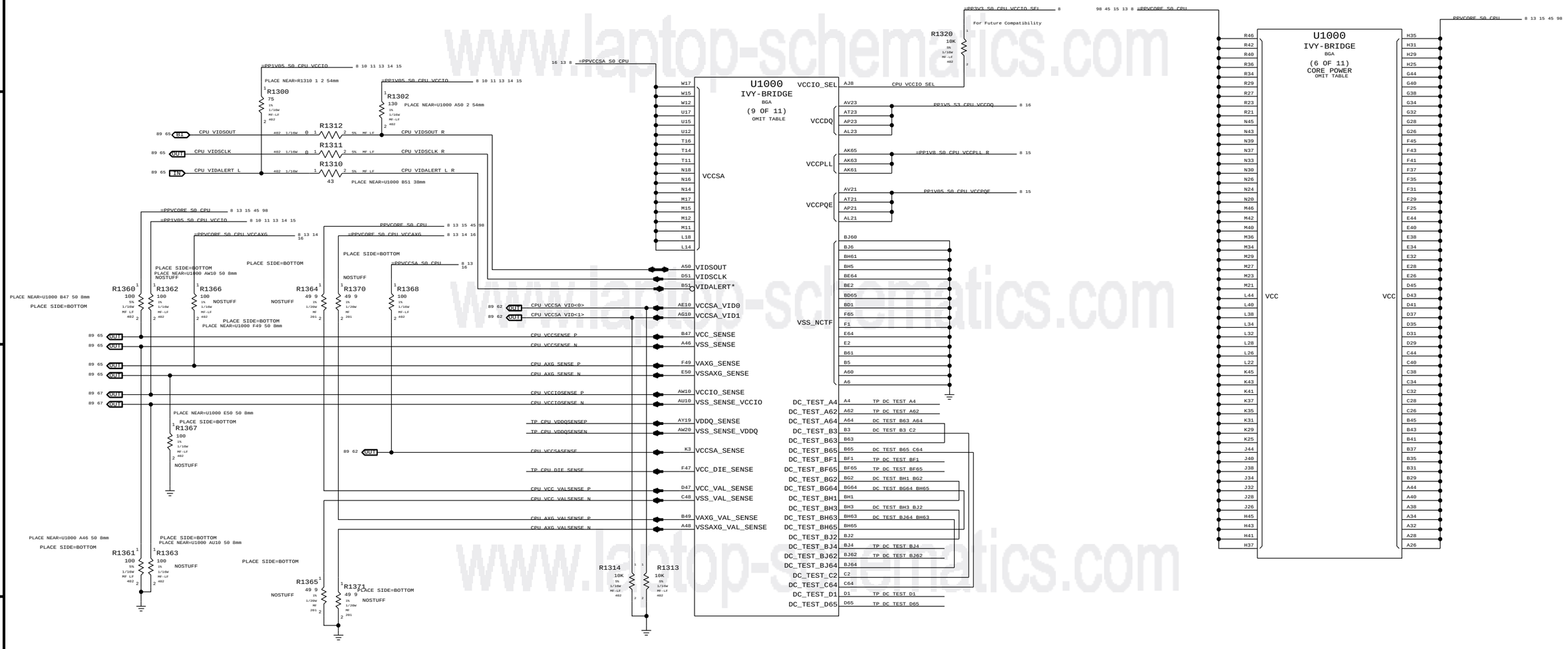

NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: CPU POWER

Apple Inc.

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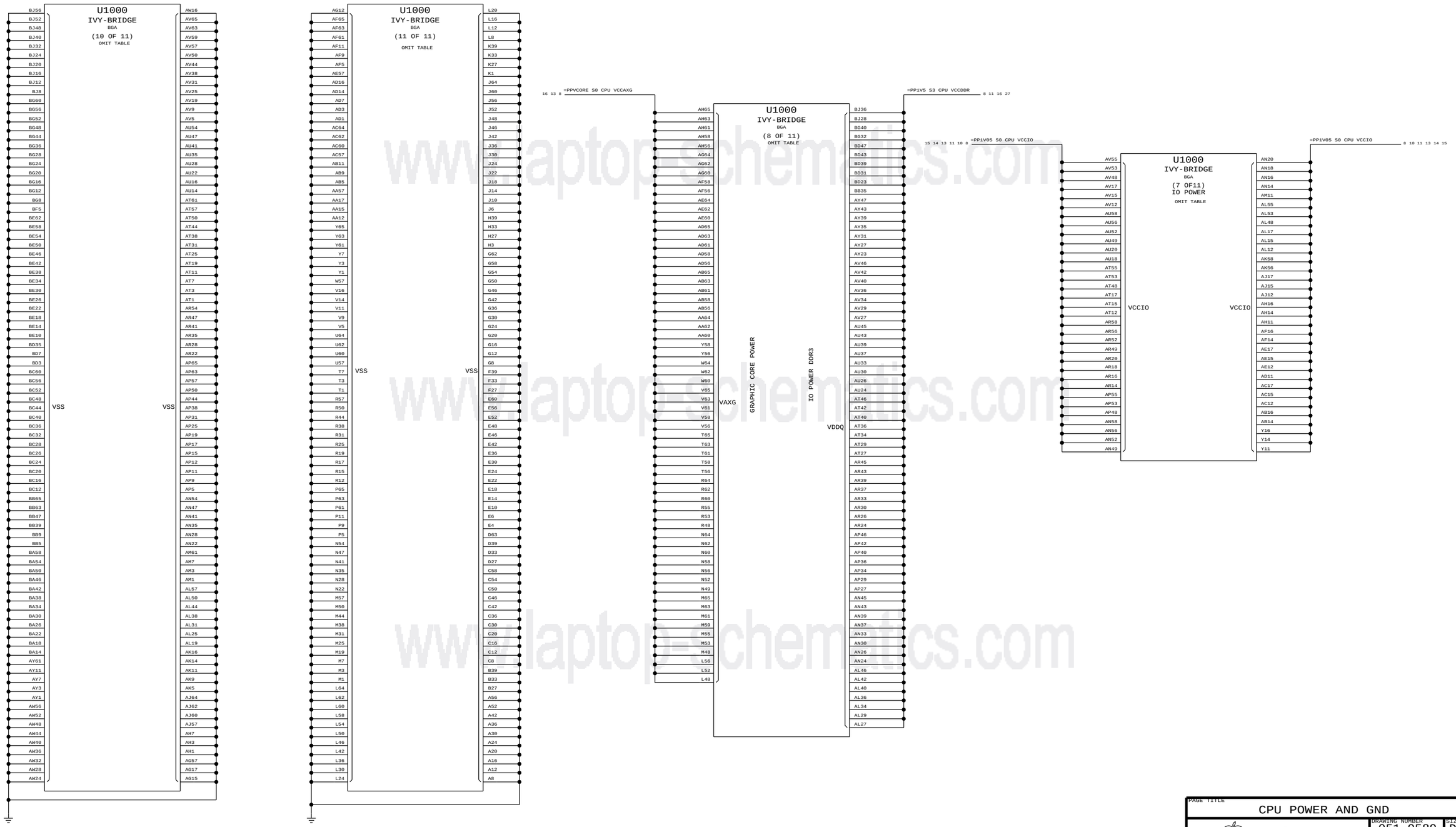

PAGE TITLE
CPU POWER AND GND

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 8x 270uF 6mOhm, 0x 470uF 4mOhm , 16x 22uF 0402, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0402 (NOSTUFF)

98 45 13 8 =PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X6S CERM 0402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 4V CERM X6S 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 4V CERM X6S 0201

PLACEMENT_NOTE (C1620-C1623):
Place near inductors on bottom side.
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 4V X6S 0402

NOSTUFF CRITICAL C1690 C1691 C1698 C1693 C1694 C1695 C1696 NOSTUFF CRITICAL C1699
20UF 20% 2V X6T CERM 0402

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 NOSTUFF C1628 CRITICAL C1629 C1630 C1631 NOSTUFF C1632 NOSTUFF C1633 CRITICAL C1634 CRITICAL C1635 CRITICAL C1636 CRITICAL C1637 CRITICAL C1638 CRITICAL C1639 NOSTUFF C16D0 NOSTUFF C16D1 NOSTUFF C16D2 NOSTUFF C16D3 NOSTUFF C16D4 NOSTUFF C16D5
20UF 20% 2V X6T CERM 0402

PLACEMENT_NOTE (C1640-C1645):

CRITICAL C1640 C1641 C1642 C1643 C1644 C1645 C1688 C1689
270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 11 10 8 14 =PP1V05_S0_CPU_VCCIO

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X6S CERM 0402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X6S CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 4V X6S CERM 0603

CRITICAL C1682 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
CRITICAL C1683 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 2% 1/4W MF 0603
PP1V05_S0_CPU_VCCPQE 8 13
C1684 1UF 10% 10V X6S CERM 0402

CPU VCCPLL DECOUPLING

8 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF LF 402
=PP1V8_S0_CPU_VCCPLL_R 8 13
PLACE_NEAR=U1000.AK61:5MM
C1685 1UF 10% 10V X6S CERM 0402
C1686 1UF 10% 10V X6S CERM 0402
CRITICAL C1687 220UF 20% 2.5V TANT B16 (Z = 1.2mm, place on short side behind CPU)
PLACE NEAR U1000 AK63 2 54 mm NO VIA
PLACE NEAR U1000 AK65 2 54 mm NO VIA

CPU VCCPLL Low pass filter

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: CPU DECOUPLING-I

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VAXG DECOUPLING

INTEL RECOMMENDATION: 2X 470UF 4MOHM, 2X 470UF 4MOHM (NOSTUFF), 6X 22UF 0805, 2X 22UF 0805 (NOSTUFF), 6X 10UF 0603, 2X 10UF 0603 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)
APPLE IMPLEMENTATION: 0X 470UF 4MOHM, 3X 330UF 9MOHM , 6X 22UF 0603, 2X 22UF 0603 (NOSTUFF), 6X 10UF 0402, 2X 10UF 0402 (NOSTUFF), 9X 1UF 0402, 9X 1UF 0402 (NOSTUFF)

14 13 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 NOSTUFF: C1709 C1710 C1711 C1712 C1713 C1714 C1715 C1716 C1717
1UF 10% 10V X6S CERM 0402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 C1719 C1720 C1721 C1722 C1723 NOSTUFF: C1724 C1725
10UF 20% 4V X6S 0402

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 C1727 C1728 C1729 C1730 C1731 NOSTUFF: C1732 C1733
22UF 20% 4V X6S 0603

PLACEMENT_NOTE (C1734-C1735):

CRITICAL C1734 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1735 330UF-6MOHM 20% 2.0V POLY-TANT D15T
CRITICAL C1737 330UF-6MOHM 20% 2.0V POLY-TANT D15T
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

27 14 11 8 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747
1UF 10% 10V X6S CERM 0402

Place close to U1000 on bottom side

C1748 C1749 C1750 C1751 C1752 C1753 C1754 C1755
10UF 20% 4V X6S CERM 0603

Place near inductors on bottom side

C1756 330UF-0.006OHM 20% 2V POLY CASE D2 SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W ME 0603
=PP1V5_S3_CPU_VCCDQ 8 13
C1757 1UF 10% 10V X6S CERM 0402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

13 8 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):
Place on bottom side of U1000

C1758 C1759 C1760 C1761 C1762
1UF 10% 10V X6S CERM 0402

C1763 C1764 C1765 C1766 C1767
10UF 20% 4V X6S CERM 0603

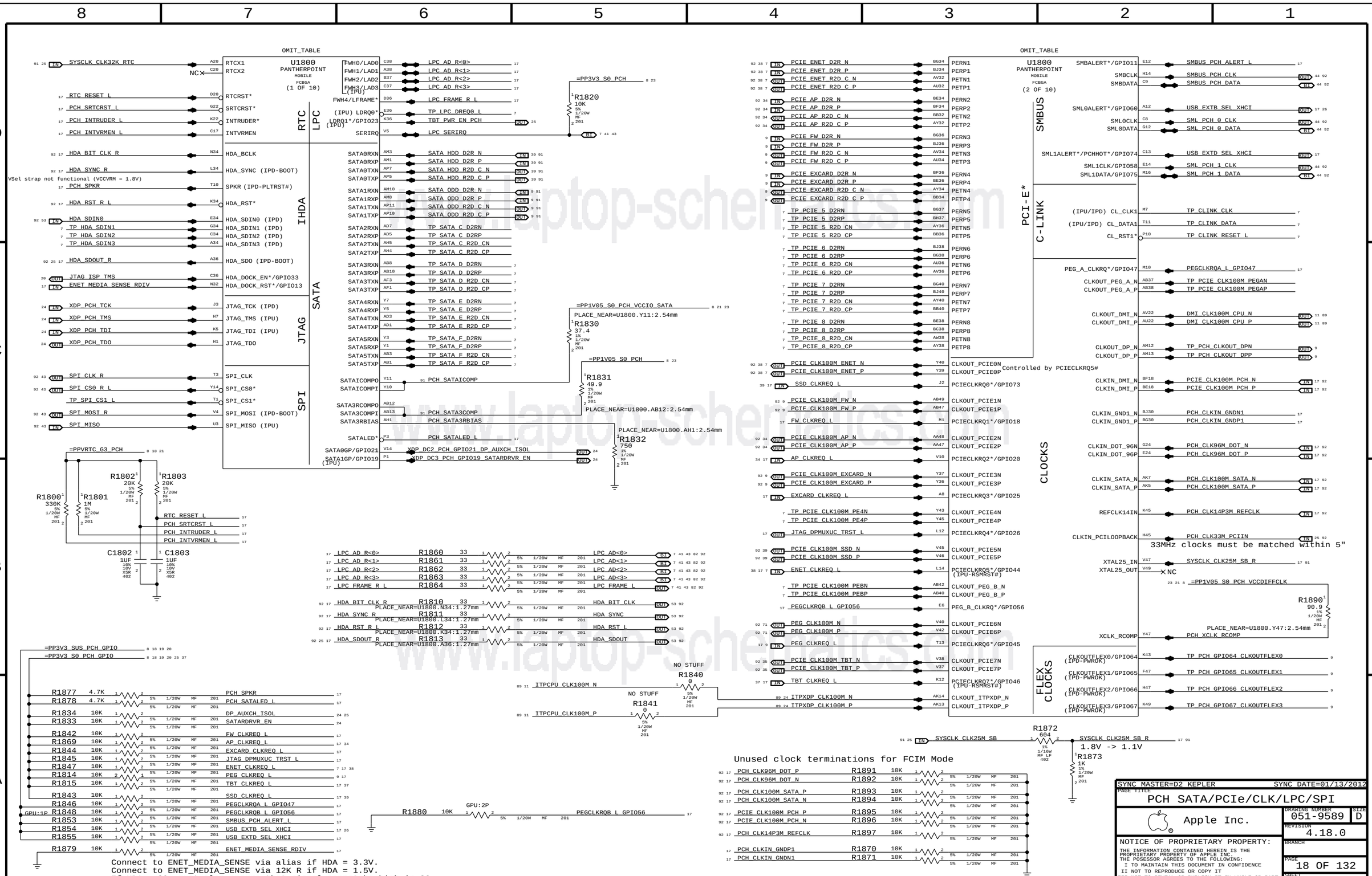
CRITICAL C1768 330UF-6MOHM 20% 2.0V POLY-TANT DIST-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
REVISION: 4.18.0
BRANCH:
PAGE: 17 OF 132
SHEET: 16 OF 99


U1800
PANTHONPOINT
MOBILE
FCBGA
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK_CLK32K_RTC
RTCX1
RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_ISP_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
VSel strap not functional (VCCVRM = 1.8V)
=PPVRTC_G3_PCH
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1UF
C1803 1UF
=PP3V3_S0_PCH
R1820 10K
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.Y11:2.54mm
R1830 37.4
=PP1V05_S0_PCH
R1831 49.9
PLACE_NEAR=U1800.AB12:2.54mm
PLACE_NEAR=U1800.AH1:2.54mm
R1832 750
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1877 4.7K
R1878 4.7K
R1834 10K
R1833 10K
R1842 10K
R1869 10K
R1844 10K
R1845 10K
R1847 10K
R1814 10K
R1815 10K
R1843 10K
R1846 10K
R1848 10K
R1853 10K
R1854 10K
R1855 10K
R1879 10K
R1880 10K
R1810 33
R1811 33
R1812 33
R1813 33
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1840 0
R1841 0
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
OMIT_TABLE
U1800
PANTHONPOINT
MOBILE
FCBGA
(2 OF 10)
SMBUS
PCI-E*
C-LINK
CLOCKS
FLEX CLOCKS
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
TP_PCIE_5_D2RN
TP_PCIE_5_D2RP
TP_PCIE_5_R2D_CN
TP_PCIE_5_R2D_CP
TP_PCIE_6_D2RN
TP_PCIE_6_D2RP
TP_PCIE_6_R2D_CN
TP_PCIE_6_R2D_CP
TP_PCIE_7_D2RN
TP_PCIE_7_D2RP
TP_PCIE_7_R2D_CN
TP_PCIE_7_R2D_CP
TP_PCIE_8_D2RN
TP_PCIE_8_D2RP
TP_PCIE_8_R2D_CN
TP_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
SSD_CLKREQ_L
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L_GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1*
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
CLKOUT_PCIE0N
CLKOUT_PCIE0P
Controlled by PCIECLKRQ5#
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
SMBUS_PCH_ALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEGCLKRQA_L_GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
33MHz clocks must be matched within 5"
=PP1V05_S0_PCH_VCCDIFFCLK
R1890 90.9
PLACE_NEAR=U1800.Y47:2.54mm
SYSCLK_CLK25M_SB
SYSCLK_CLK25M_SB_R
1.8V -> 1.1V
R1872 604
R1873 1K
Unused clock terminations for FCIM Mode
PCH_CLK96M_DOT_P
PCH_CLK96M_DOT_N
PCH_CLK100M_SATA_P
PCH_CLK100M_SATA_N
PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH_N
PCH_CLK14P3M_REFCLK
PCH_CLKIN_GNDP1
PCH_CLKIN_GNDN1
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
R1870 10K
R1871 10K
SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9589
SIZE D
REVISION 4.18.0
BRANCH
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=PP3V3_SUS_PCH_GPIO 8 17 18 19 20
=PP1V05_S0_PCH_VCCIO_PCIE 8
PLACE_NEAR=U1800.BJ24:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (3 OF 10)

DMI

DMI_N2S_N<0>	BC24	DMI0RXN	
DMI_N2S_N<1>	BE20	DMI1RXN	
DMI_N2S_N<2>	BG18	DMI2RXN	
DMI_N2S_N<3>	BG20	DMI3RXN	
DMI_N2S_P<0>	BE24	DMI0RXP	
DMI_N2S_P<1>	BC20	DMI1RXP	
DMI_N2S_P<2>	BJ18	DMI2RXP	
DMI_N2S_P<3>	BJ20	DMI3RXP	
DMI_S2N_N<0>	AW24	DMI0TXN	
DMI_S2N_N<1>	AW20	DMI1TXN	
DMI_S2N_N<2>	BB18	DMI2TXN	
DMI_S2N_N<3>	AV18	DMI3TXN	
DMI_S2N_P<0>	AY24	DMI0TXP	
DMI_S2N_P<1>	AY20	DMI1TXP	
DMI_S2N_P<2>	AY18	DMI2TXP	
DMI_S2N_P<3>	AU18	DMI3TXP	
PCH_DMI_COMP	BJ24	DMI_ZCOMP	
	BG25	DMI_IRCOMP	
PCH_DMI2RBIAS	BH21	DMI2RBIAS	

PLACE_NEAR=U1800.BH21:2.54mm
R1920 750 1% 1/20W MF 201

FDI

	BJ14	FDI_RXN0	=FDI_DATA_N<0>
	AY14	FDI_RXN1	=FDI_DATA_N<1>
	BE14	FDI_RXN2	=FDI_DATA_N<2>
	BH13	FDI_RXN3	=FDI_DATA_N<3>
	BC12	FDI_RXN4	=FDI_DATA_N<4>
	BJ12	FDI_RXN5	=FDI_DATA_N<5>
	BG10	FDI_RXN6	=FDI_DATA_N<6>
	BG9	FDI_RXN7	=FDI_DATA_N<7>
	BG14	FDI_RXP0	=FDI_DATA_P<0>
	BB14	FDI_RXP1	=FDI_DATA_P<1>
	BF14	FDI_RXP2	=FDI_DATA_P<2>
	BG13	FDI_RXP3	=FDI_DATA_P<3>
	BE12	FDI_RXP4	=FDI_DATA_P<4>
	BG12	FDI_RXP5	=FDI_DATA_P<5>
	BJ10	FDI_RXP6	=FDI_DATA_P<6>
	BH9	FDI_RXP7	=FDI_DATA_P<7>
	AW16	FDI_INT	FDI_INT
	AV12	FDI_FSYNC0	=FDI_FSYNC<0>
	BC10	FDI_FSYNC1	=FDI_FSYNC<1>
	AV14	FDI_LSYNC0	=FDI_LSYNC<0>
	BB10	FDI_LSYNC1	=FDI_LSYNC<1>

=PPVRTC_G3_PCH 8 17 21
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201

SYSTEM POWER MANAGEMENT

	A18	DSWVRMEN	PCH_DSWVRMEN
	E22	DPWROK	PM_DSW_PWRGD
	B9	WAKE*	PCIE_WAKE_L
	N3	CLKRUN*/GPIO32	PM_CLKRUN_L
	G8	SUS_STAT*/GPIO61	LPC_PWRDWN_L
	N14	SUSCLK/GPIO62	PM_CLK32K_SUSCLK_R
	D10	SLP_S5*/GPIO63	PM_SLP_S5_L
	H4	SLP_S4*	PM_SLP_S4_L
	F4	SLP_S3*	PM_SLP_S3_L
	G10	SLP_A*	TP_PM_SLP_A_L
	G16	SLP_SUS*	PM_SLP_SUS_L
	AP14	PMSYNCH	PM_SYNC
	K14	SLP_LAN*/GPIO29	MEM_VDD_SEL_1V5_L
PCH_SUSACK_L	C12	SUSACK* (IPU)	
PM_SYSRST_L	K3	SYS_RESET*	
PM_PCH_SYS_PWROK	P12	SYS_PWROK	
PM_PCH_PWROK	L22	PWROK	
PM_PCH_APWROK	L10	APWROK	
PM_MEM_PWRGD	B13	DRAMPWROK	
PM_RSMRST_L	C21	RSMRST*	
PCH_SUSWARN_L	K16	SUSWARN*/SUSPWRDNACK/GPIO30	
PM_PWRBTN_L	E20	PWRBTN* (IPU)	
SMC_ADAPTER_EN	H20	ACPRESENT/GPIO31 (IPD-DeepS4/S5)	
PM_BATLOW_L	E10	BATLOW*/GPIO72 (IPU)	
PCH_RI_L	A10	RI*	

OMIT_TABLE

U1800 PANTHERPOINT MOBILE FCBGA (4 OF 10)

LVDS

LVDS_IG_BKL_ON	J47	L_BKLTEN	
LVDS_IG_PANEL_PWR	M45	L_VDD_EN	
LVDS_IG_BKL_PWM	P45	L_BKLTCTL	
LVDS_IG_DDC_CLK	T40	L_DDC_CLK	
LVDS_IG_DDC_DATA	K47	L_DDC_DATA (IPD-PLTRST#)	
TP_LVDS_IG_CTRL_CLK	T45	L_CTRL_CLK	
TP_LVDS_IG_CTRL_DATA	P39	L_CTRL_DATA	
PCH_LVDS_IBG	AF37	LVD_IBG	
TP_PCH_LVDS_VBG	AF36	LVD_VBG	
	AE48	LVD_VREFH	
	AE47	LVD_VREFL	
LVDS_IG_A_CLK_N	AK39	LVDSA_CLK*	
LVDS_IG_A_CLK_P	AK40	LVDSA_CLK	
LVDS_IG_A_DATA_N<0>	AN48	LVDSA_DATA0*	
LVDS_IG_A_DATA_N<1>	AM47	LVDSA_DATA1*	
LVDS_IG_A_DATA_N<2>	AK47	LVDSA_DATA2*	
LVDS_IG_A_DATA_N<3>	AJ48	LVDSA_DATA3*	
LVDS_IG_A_DATA_P<0>	AN47	LVDSA_DATA0	
LVDS_IG_A_DATA_P<1>	AM49	LVDSA_DATA1	
LVDS_IG_A_DATA_P<2>	AK49	LVDSA_DATA2	
LVDS_IG_A_DATA_P<3>	AJ47	LVDSA_DATA3	
LVDS_IG_B_CLK_N	AF40	LVDSB_CLK*	
LVDS_IG_B_CLK_P	AF39	LVDSB_CLK	
LVDS_IG_B_DATA_N<0>	AH45	LVDSB_DATA0*	
LVDS_IG_B_DATA_N<1>	AH47	LVDSB_DATA1*	
LVDS_IG_B_DATA_N<2>	AF49	LVDSB_DATA2*	
LVDS_IG_B_DATA_N<3>	AF45	LVDSB_DATA3*	
LVDS_IG_B_DATA_P<0>	AH43	LVDSB_DATA0	
LVDS_IG_B_DATA_P<1>	AH49	LVDSB_DATA1	
LVDS_IG_B_DATA_P<2>	AF47	LVDSB_DATA2	
LVDS_IG_B_DATA_P<3>	AF43	LVDSB_DATA3	

CRT

TP_CRT_IG_BLUE	N48	CRT_BLUE	
TP_CRT_IG_GREEN	P49	CRT_GREEN	
TP_CRT_IG_RED	T49	CRT_RED	
TP_CRT_IG_DDC_CLK	T39	CRT_DDC_CLK	
TP_CRT_IG_DDC_DATA	M40	CRT_DDC_DATA	
TP_CRT_IG_HSYNC	M47	CRT_HSYNC	
TP_CRT_IG_VSYNC	M49	CRT_VSYNC	
PCH_DAC_IREF	T43	DAC_IREF	
	T42	CRT_IRTN	

PLACE_NEAR=U1800.AF37:2.54mm
R1950 2.37K 1% 1/20W MF 201
PLACE_NEAR=U1800.T43:2.54mm
R1951 1K 5% 1/20W MF 201

DIGITAL DISPLAY INTERFACE

SDVO_TVCLKINN (IPD)	AP43	TP_SDVO_TVCLKINN	
SDVO_TVCLKINP (IPD)	AP45	TP_SDVO_TVCLKINP	
SDVO_STALLN (IPD)	AM42	TP_SDVO_STALLN	
SDVO_STALLP (IPD)	AM40	TP_SDVO_STALLP	
SDVO_INTN (IPD)	AP39	TP_SDVO_INTN	
SDVO_INTP (IPD)	AP40	TP_SDVO_INTP	
SDVO_CTRLCLK	P38	DPA_IG_DDC_CLK	83
SDVO_CTRLDATA (IPD-PLTRST#)	M39	DPA_IG_DDC_DATA	83
DDPB_AUXN	AT49	DPA_IG_AUX_CH_N	83 95
DDPB_AUXP	AT47	DPA_IG_AUX_CH_P	83 95
DDPB_HPD	AT40	DPA_IG_HPD	9 82
DDPB_0N	AV42	TP_DP_IG_B_MLN<0>	9
DDPB_0P	AV40	TP_DP_IG_B_MLP<0>	9
DDPB_1N	AV45	TP_DP_IG_B_MLN<1>	9
DDPB_1P	AV46	TP_DP_IG_B_MLP<1>	9
DDPB_2N	AU48	TP_DP_IG_B_MLN<2>	9
DDPB_2P	AU47	TP_DP_IG_B_MLP<2>	9
DDPB_3N	AV47	TP_DP_IG_B_MLN<3>	9
DDPB_3P	AV49	TP_DP_IG_B_MLP<3>	9
DDPC_CTRLCLK	P46	DPB_IG_DDC_CLK	83
DDPC_CTRLDATA (IPD-PLTRST#)	P42	DPB_IG_DDC_DATA	83
DDPC_AUXN	AP47	DPB_IG_AUX_CH_N	83 95
DDPC_AUXP	AP49	DPB_IG_AUX_CH_P	83 95
DDPC_HPD	AT38	DPB_IG_HPD	9 82
DDPC_0N	AY47	TP_DP_IG_C_MLN<0>	7
DDPC_0P	AY49	TP_DP_IG_C_MLP<0>	7
DDPC_1N	AY43	TP_DP_IG_C_MLN<1>	7
DDPC_1P	AY45	TP_DP_IG_C_MLP<1>	7
DDPC_2N	BA47	TP_DP_IG_C_MLN<2>	7
DDPC_2P	BA48	TP_DP_IG_C_MLP<2>	7
DDPC_3N	BB47	TP_DP_IG_C_MLN<3>	7
DDPC_3P	BB49	TP_DP_IG_C_MLP<3>	7
DDPD_CTRLCLK	M43	TP_DP_IG_D_CTRL_CLK	7
DDPD_CTRLDATA (IPD-PLTRST#)	M36	TP_DP_IG_D_CTRL_DATA	7
DDPD_AUXN	AT45	TP_DP_IG_D_AUXN	7
DDPD_AUXP	AT43	TP_DP_IG_D_AUXP	7
DDPD_HPD	BH41	TP_DP_IG_D_HPD	7
DDPD_0N	BB43	TP_DP_IG_D_MLN<0>	7
DDPD_0P	BB45	TP_DP_IG_D_MLP<0>	7
DDPD_1N	BF44	TP_DP_IG_D_MLN<1>	7
DDPD_1P	BE44	TP_DP_IG_D_MLP<1>	7
DDPD_2N	BF42	TP_DP_IG_D_MLN<2>	7
DDPD_2P	BE42	TP_DP_IG_D_MLP<2>	7
DDPD_3N	BJ42	TP_DP_IG_D_MLN<3>	7
DDPD_3P	BG42	TP_DP_IG_D_MLP<3>	7

20 19 18 17 8 =PP3V3_SUS_PCH_GPIO
R1983 10K 5% 1/20W MF 201
18 PCH_SUSWARN_L
R1986 0 5% 1/20W MF 201
PCH_SUSACK_L 18

=PP3V3_SUS_PCH_GPIO 8 17 18 19 20
=PP3V3_S0_PCH_GPIO 8 17 19 20 25 37
=PP3V3_S5_PCH 8

R1985	1K	PM_PWRBTN_L	18 24 41
R1991	8.2K	PM_CLKRUN_L	7 18 41 43
R1982	10K	MEM_VDD_SEL_1V5_L	18 64
R1925	1K	PCIE_WAKE_L	7 18 34
R1924	100K	PM_SLP_S3_L	7 18 27 38 41 70
R1921	100K	PM_SLP_S4_L	7 18 27 34 38 40 41 70
R1922	100K	PM_SLP_S5_L	18 41 70
R1923	100K	PM_SLP_SUS_L	18 70
R1981	100K	LVDS_IG_BKL_ON	9 18
R1984	100K	LVDS_IG_PANEL_PWR	9 18

5% 1/20W MF 201

MAKE_BASE=TRUE

NOSTUFF
R1999 0 5% 1/20W MF 201
=TBT_WAKE_L IN 35 42

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
PCH DMI/FDI/PM/Graphics

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OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
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NC	BG26	TP1	RSVD1	AY7	NC
NC	BJ26	TP2	RSVD2	AV7	NC
NC	BH25	TP3	RSVD3	AU3	NC
NC	BJ16	TP4	RSVD4	BG4	NC
NC	BG16	TP5	RSVD5	AT10	NC
NC	AH38	TP6	RSVD6	BC8	NC
NC	AH37	TP7	RSVD7	AU2	NC
NC	AK43	TP8	RSVD8	AT4	NC
NC	AK45	TP9	RSVD9	AT3	NC
NC	C18	TP10	RSVD10	AT1	NC
NC	N30	TP11	RSVD11	AY3	NC
NC	H3	TP12	RSVD12	AT5	NC
NC	AH12	TP13	RSVD13	AV3	NC
NC	AM4	TP14	RSVD14	AV1	NC
NC	AM5	TP15	RSVD15	BB1	NC
NC	Y13	TP16	RSVD16	BA3	NC
NC	K24	TP17	RSVD17	BB5	NC
NC	L24	TP18	RSVD18	BB3	NC
NC	AB46	TP19	RSVD19	BB7	NC
NC	AB45	TP20	RSVD20	BE8	NC
NC	B21	TP21	RSVD21	BD4	NC
NC	M28	TP22	RSVD22	BF6	NC
TP_PCH_TP23	AY16	TP23	RSVD23	AV5	NC
NC	BG46	TP24	RSVD24	AV10	NC
			RSVD25	AT8	NC
			RSVD26	AY5	NC
			RSVD27	BA2	NC
			RSVD28	AT12	NC
			RSVD29	BF3	NC

USB

91 40 IN	USB3_EXTA_RX_N	BE28	USB3RN1	USBP0N	C24	USB_EXTA_N (BI 40 91)
91 38 7 IN	USB3_EXTB_RX_N	BC30	USB3RN2	USBP0P	A24	USB_EXTA_P (BI 40 91)
91 9 IN	USB3_EXTC_RX_N	BE32	USB3RN3	USBP1N	C25	USB_EXTB_XHCI_N (BI 26 91)
9 IN	USB3_EXTD_RX_N	BJ32	USB3RN4	USBP1P	B25	USB_EXTB_XHCI_P (BI 26 91)
91 40 IN	USB3_EXTA_RX_P	BC28	USB3RP1	USBP2N	C26	USB_EXTC_N (BI 9 91)
91 38 7 IN	USB3_EXTB_RX_P	BE30	USB3RP2	USBP2P	A26	USB_EXTC_P (BI 9 91)
91 9 IN	USB3_EXTC_RX_P	BF32	USB3RP3	USBP3N	K28	USB_EXTD_XHCI_N (BI 26 91)
9 IN	USB3_EXTD_RX_P	BG32	USB3RP4	USBP3P	H28	USB_EXTD_XHCI_P (BI 26 91)
91 40 OUT	USB3_EXTA_TX_N	AV26	USB3TN1	USBP4N	E28	TP_USB_4N
91 38 OUT	USB3_EXTB_TX_N	BB26	USB3TN2	USBP4P	D28	TP_USB_4P
91 9 OUT	USB3_EXTC_TX_N	AU28	USB3TN3	USBP5N	C28	TP_USB_SDN
9 OUT	USB3_EXTD_TX_N	AY30	USB3TN4	USBP5P	A28	TP_USB_SDP
91 40 OUT	USB3_EXTA_TX_P	AU26	USB3TP1	USBP6N	C29	TP_USB_WLANN
91 38 OUT	USB3_EXTB_TX_P	AY26	USB3TP2	USBP6P	B29	TP_USB_WLANP
91 9 OUT	USB3_EXTC_TX_P	AV28	USB3TP3	USBP7N	N28	USB_HUB_UP_N (BI 26 91)
9 OUT	USB3_EXTD_TX_P	AW30	USB3TP4	USBP7P	M28	USB_HUB_UP_P (BI 26 91)
				USBP8N	L30	USB_CAMERA_N (BI 34 91)
				USBP8P	K30	USB_CAMERA_P (BI 34 91)
				USBP9N	G30	USB_EXTB_EHCI_N (BI 26 91)
				USBP9P	E30	USB_EXTB_EHCI_P (BI 26 91)
				USBP10N	C30	USB_EXTD_EHCI_N (BI 9)
				USBP10P	A30	USB_EXTD_EHCI_P (BI 9)
				USBP11N	L32	TP_USB_BT_HSN
				USBP11P	K32	TP_USB_BT_HSP
				USBP12N	G32	TP_USB_12N
				USBP12P	E32	TP_USB_12P
				USBP13N	C32	TP_USB_13N
				USBP13P (IPD)	A32	TP_USB_13P

PCI

=PP3V3_S0_PCH_GPIO (37 25 20 19 18 17 8)	R2010 10K 5% 1/20W MF 201	PCI_INTA_L	K40	PIRQA*
	R2011 10K 5% 1/20W MF 201	PCI_INTB_L	K38	PIRQB*
	R2012 10K 5% 1/20W MF 201	PCI_INTC_L	H38	PIRQC*
	R2013 10K 5% 1/20W MF 201	PCI_INTD_L	G38	PIRQD*
		JTAG_GMUX_TMS (19 OUT)	C46	REQ1*/GPIO50
		BLC_I2C_MUX_SEL (19 OUT)	C44	REQ2*/GPIO52
		USE_HDD_OOB_L (19 OUT)	E40	REQ3*/GPIO54
		TP_PCH_STRP_BBS1	D47	GNT1*/GPIO51
		TP_PCH_STRP_ESI_L	E42	GNT2*/GPIO53
	R2054 10K 5% 1/20W MF 201 NO STUFF	PCH_STRP_TOPBLK_SWP_L	F46	GNT3*/GPIO55 (IPU-PCIERST#)
		BLC_GPIO (19 IN)	G42	PIRQE*/GPIO2
		AUD_IP_PERIPHERAL_DET (59 19 IN)	G40	PIRQF*/GPIO3
		TBT_PWR_REQ_L (35 19 IN)	C42	PIRQG*/GPIO4
		AUD_I2C_INT_L (58 19 IN)	D44	PIRQH*/GPIO5
		TP_PCI_PME_L (7 IN)	K10	PME* (IPU)
		PLT_RESET_L (27 25 OUT)	C6	PLTRST*
		LPC_CLK33M_SMC_R (92 25 OUT)	H49	CLKOUT_PCI0
		LPC_CLK33M_LPCPLUS_R (25 OUT)	H43	CLKOUT_PCI1
		TP_PCI_CLK33M_OUT2 (25)	J48	CLKOUT_PCI2
		TP_PCI_CLK33M_OUT3 (7)	K42	CLKOUT_PCI3
		PCH_CLK33M_PCIOUT (25 OUT)	H40	CLKOUT_PCI4 (IPD)

USBRBIAS*	C33	91 PCH_USB_RBIAS		
USBRBIAS	B33			
OC0*/GPIO59	A14	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L (IN 19 24)	R2070 22.6 1% 1/20W MF 201	PLACE_NEAR=U1800.B33:2.54mm
OC1*/GPIO40	K20	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L (IN 19 24)		
OC2*/GPIO41	B17	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L (IN 19 24)		
OC3*/GPIO42	C16	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L (IN 19 24)		
OC4*/GPIO43	L16	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L (IN 19 24)		
OC5*/GPIO9	A16	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L (IN 19 24)		
OC6*/GPIO10	D14	XDP_DB2_PCH_GPIO10_AP_PWR_EN (PWR 24)		
OC7*/GPIO14	C14	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE (IN 19 24)		

Ext A (XHCI/EHCI)

Ext B (XHCI)

Ext C (XHCI/EHCI)

Ext D (XHCI) (Mobiles: Trackpad?)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

Ext B (EHCI)

Ext D (EHCI)

RSVD: BT (HS)

Unused

Unused

=PP3V3_SUS_PCH_GPIO (8 17 18 20)
=PP3V3_S3_PCH_GPIO (8 25)
=PP3V3_S0_PCH_GPIO (8 17 18 19 20 25 37)

R2016 10K 5% 1/20W MF 201	JTAG_GMUX_TMS	19	
R2017 10K 5% 1/20W MF 201	BLC_I2C_MUX_SEL	19	
R2018 10K 5% 1/20W MF 201	USE_HDD_OOB_L	19	
R2030 10K 5% 1/20W MF 201	BLC_GPIO	19	
NO STUFF R2014 10K 5% 1/20W MF 201	AUD_IP_PERIPHERAL_DET	19 59	Redundant to pull-up on audio page
R2031 10K 5% 1/20W MF 201	TBT_PWR_REQ_L	19 35	
NO STUFF R2033 10K 5% 1/20W MF 201	AUD_I2C_INT_L	19 58	Redundant to pull-up on audio page
R2069 10K 5% 1/20W MF 201	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	19 24	
R2060 10K 5% 1/20W MF 201	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	19 24	
R2061 10K 5% 1/20W MF 201	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	19 24	
R2062 10K 5% 1/20W MF 201	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	19 24	
R2068 10K 5% 1/20W MF 201	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	19 24	
R2067 10K 5% 1/20W MF 201	AP_PWR_EN	24 34 70	

(24 19) XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L — R2020 1K 5% 1/20W MF 201 — XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L (19 24)

(24 19) XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L — R2021 1K 5% 1/20W MF 201 — XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L (19 24)

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PCH PCI/USB/TP/RSVD

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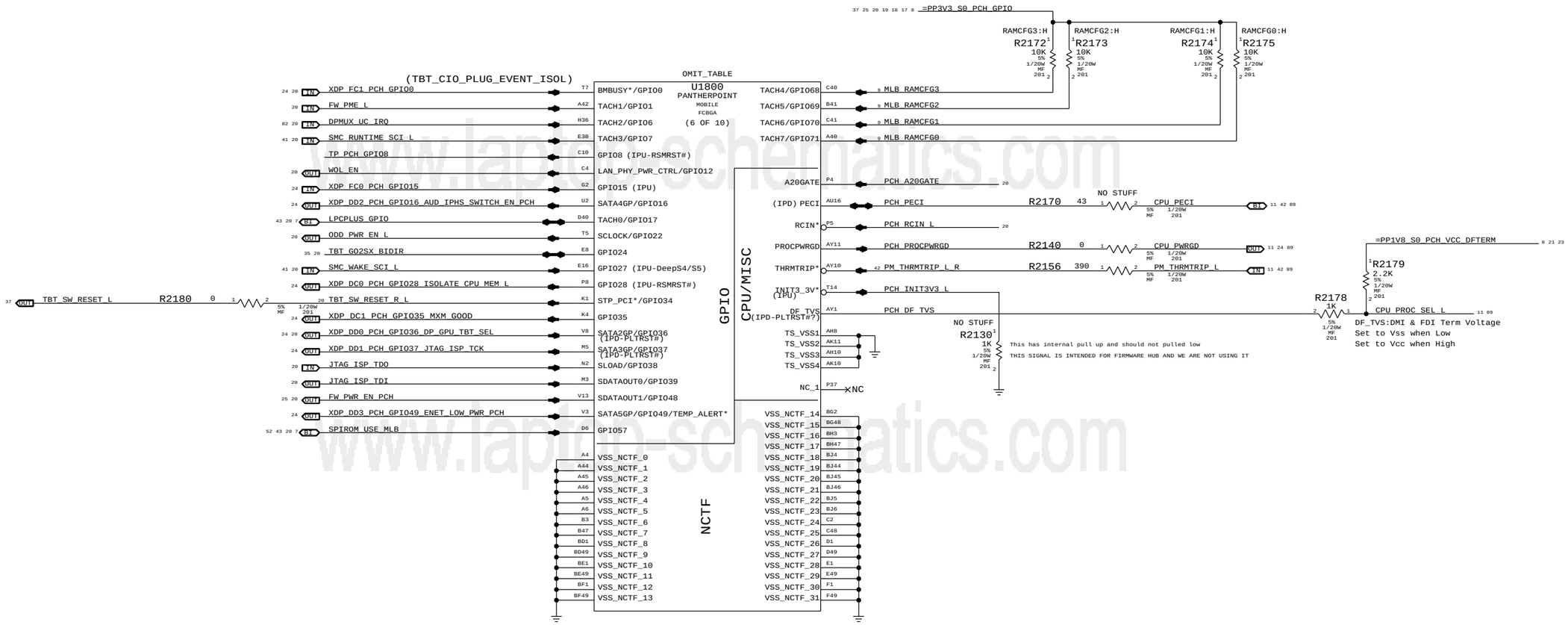
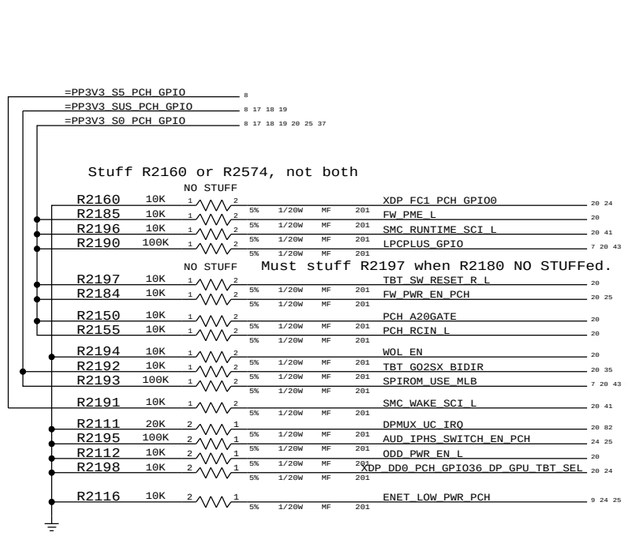
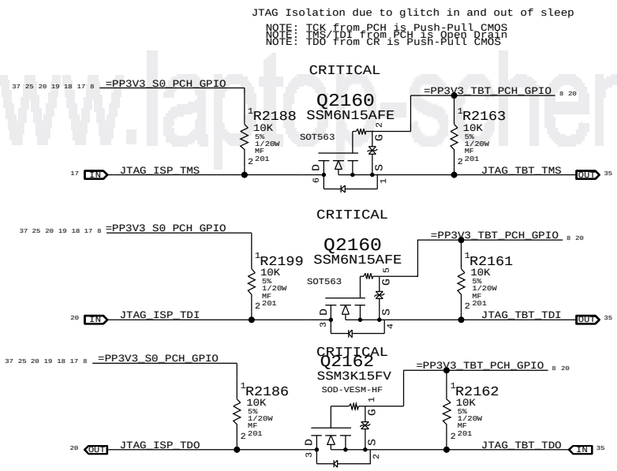
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

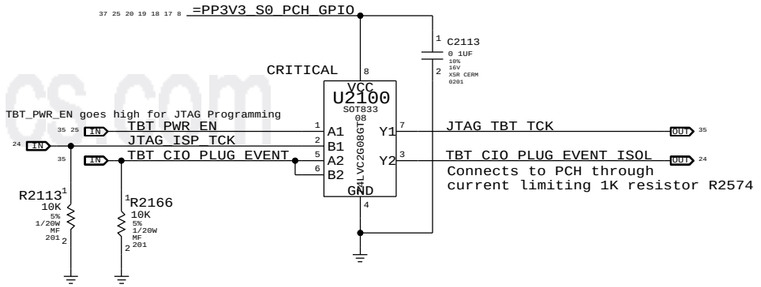
Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.









SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

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SYNC_MASTER=D2_CLEAN SYNC_DATE=03/19/2012

PAGE TITLE: PCH POWER

Apple Inc.

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PANTHERPOINT
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VSS

H5	VSS	VSS	AK38
AA17	VSS	VSS	AK4
AA2	VSS	VSS	AK42
AA3	VSS	VSS	AK46
AA33	VSS	VSS	AK8
AA34	VSS	VSS	AL16
AB11	VSS	VSS	AL17
AB14	VSS	VSS	AL19
AB39	VSS	VSS	AL2
AB4	VSS	VSS	AL21
AB43	VSS	VSS	AL23
AB5	VSS	VSS	AL26
AB7	VSS	VSS	AL27
AC19	VSS	VSS	AL31
AC2	VSS	VSS	AL33
AC21	VSS	VSS	AL34
AC24	VSS	VSS	AL48
AC33	VSS	VSS	AM11
AC34	VSS	VSS	AM14
AC48	VSS	VSS	AM36
AD10	VSS	VSS	AM39
AD11	VSS	VSS	AM43
AD12	VSS	VSS	AM45
AD13	VSS	VSS	AM46
AD19	VSS	VSS	AM7
AD24	VSS	VSS	AN2
AD26	VSS	VSS	AN29
AD27	VSS	VSS	AN3
AD33	VSS	VSS	AN31
AD34	VSS	VSS	AP12
AD36	VSS	VSS	AP19
AD37	VSS	VSS	AP28
AD38	VSS	VSS	AP30
AD39	VSS	VSS	AP32
AD4	VSS	VSS	AP38
AD40	VSS	VSS	AP4
AD42	VSS	VSS	AP42
AD43	VSS	VSS	AP46
AD45	VSS	VSS	AP8
AD46	VSS	VSS	AR2
AD8	VSS	VSS	AR48
AE2	VSS	VSS	AT11
AE3	VSS	VSS	AT13
AF10	VSS	VSS	AT18
AF12	VSS	VSS	AT22
AD14	VSS	VSS	AT26
AD16	VSS	VSS	AT28
AF16	VSS	VSS	AT30
AF19	VSS	VSS	AT32
AF24	VSS	VSS	AT34
AF26	VSS	VSS	AT39
AF27	VSS	VSS	AT42
AF29	VSS	VSS	AT46
AF31	VSS	VSS	AT7
AF38	VSS	VSS	AU24
AF4	VSS	VSS	AU30
AF42	VSS	VSS	AV11
AF46	VSS	VSS	AV16
AF5	VSS	VSS	AV20
AF7	VSS	VSS	AV24
AF8	VSS	VSS	AV30
AG19	VSS	VSS	AV38
AG2	VSS	VSS	AV4
AG31	VSS	VSS	AV43
AG48	VSS	VSS	AV8
AH11	VSS	VSS	AW14
AH3	VSS	VSS	AW18
AH36	VSS	VSS	AW2
AH39	VSS	VSS	AW22
AH40	VSS	VSS	AW26
AH42	VSS	VSS	AW28
AH46	VSS	VSS	AW32
AH7	VSS	VSS	AW34
AJ19	VSS	VSS	AW36
AJ21	VSS	VSS	AW40
AJ24	VSS	VSS	AW48
AJ33	VSS	VSS	AY12
AJ34	VSS	VSS	AY22
AK12	VSS	VSS	AY28
AK3	VSS		

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
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VSS

AY4	VSS	VSS	H46
AY42	VSS	VSS	K18
AY46	VSS	VSS	K26
AY8	VSS	VSS	K39
B11	VSS	VSS	K46
B15	VSS	VSS	K7
B19	VSS	VSS	L18
B23	VSS	VSS	L2
B27	VSS	VSS	L20
B31	VSS	VSS	L26
B35	VSS	VSS	L28
B39	VSS	VSS	L36
B7	VSS	VSS	L48
F45	VSS	VSS	M12
BB12	VSS	VSS	P16
BB16	VSS	VSS	M18
BB20	VSS	VSS	M22
BB22	VSS	VSS	M24
BB24	VSS	VSS	M30
BB28	VSS	VSS	M32
BB30	VSS	VSS	M34
BB38	VSS	VSS	M38
BB4	VSS	VSS	M4
BB46	VSS	VSS	M42
BC14	VSS	VSS	M46
BC18	VSS	VSS	M8
BC2	VSS	VSS	N18
BC22	VSS	VSS	P30
BC26	VSS	VSS	N47
BC32	VSS	VSS	P11
BC34	VSS	VSS	P18
BC36	VSS	VSS	T33
BC40	VSS	VSS	P40
BC42	VSS	VSS	P43
BC48	VSS	VSS	P47
BD46	VSS	VSS	P7
BD5	VSS	VSS	R2
BE22	VSS	VSS	R48
BE26	VSS	VSS	T12
BE40	VSS	VSS	T31
BF10	VSS	VSS	T37
BF12	VSS	VSS	T4
BF16	VSS	VSS	W34
BF20	VSS	VSS	T46
BF22	VSS	VSS	T47
BF24	VSS	VSS	T8
BF26	VSS	VSS	V11
BF28	VSS	VSS	V17
BD3	VSS	VSS	V26
BF30	VSS	VSS	V27
BF38	VSS	VSS	V29
BF40	VSS	VSS	V31
BF8	VSS	VSS	V36
BG17	VSS	VSS	V39
BG21	VSS	VSS	V43
BG33	VSS	VSS	V7
BG44	VSS	VSS	W17
BG8	VSS	VSS	W19
BH11	VSS	VSS	W2
BH15	VSS	VSS	W27
BH17	VSS	VSS	W48
BH19	VSS	VSS	Y12
H10	VSS	VSS	Y38
BH27	VSS	VSS	Y4
BH31	VSS	VSS	Y42
BH33	VSS	VSS	Y46
BH35	VSS	VSS	Y8
BH39	VSS		
BH43	VSS	VSS	BG29
BH7	VSS	VSS	N24
D3	VSS	VSS	AJ3
D12	VSS	VSS	AD47
D16	VSS		
D18	VSS	VSS	B43
D22	VSS	VSS	BE10
D24	VSS	VSS	BG41
D26	VSS		
D30	VSS	VSS	G14
D32	VSS	VSS	H16
D34	VSS		
D38	VSS	VSS	T36
D42	VSS		
D8	VSS	VSS	BG22
E18	VSS	VSS	BG24
E26	VSS	VSS	C22
G18	VSS	VSS	AP13
G20	VSS	VSS	M14
G26	VSS	VSS	AP3
G28	VSS	VSS	AP1
G36	VSS	VSS	BE16
G48	VSS	VSS	BC16
H12	VSS	VSS	BG28
H18	VSS	VSS	BJ28
H22	VSS		
H24	VSS		
H26	VSS		
H30	VSS		
H32	VSS		
H34	VSS		
F3	VSS		

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

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PCH GROUNDS

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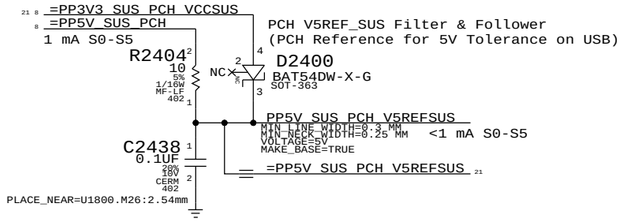

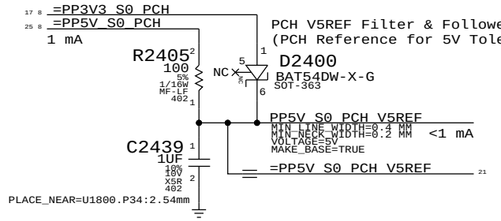

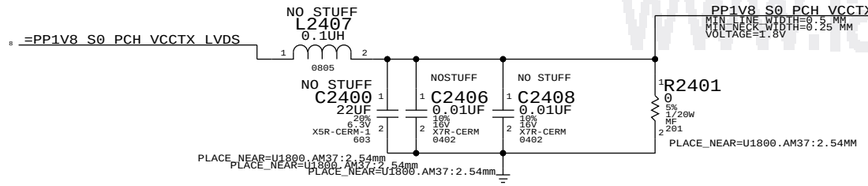

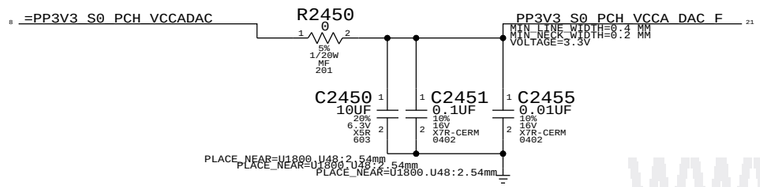

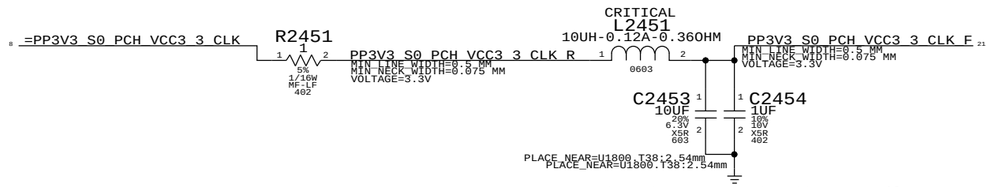

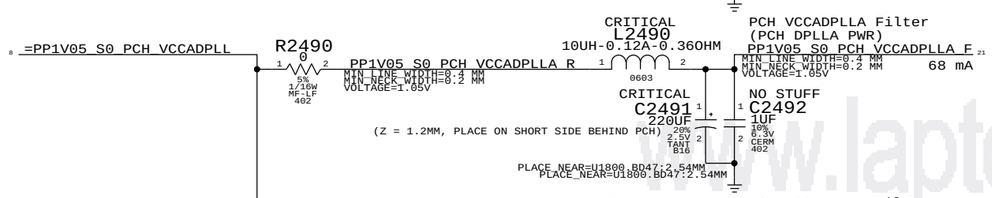

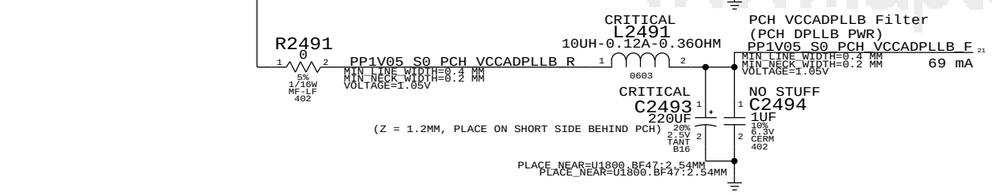

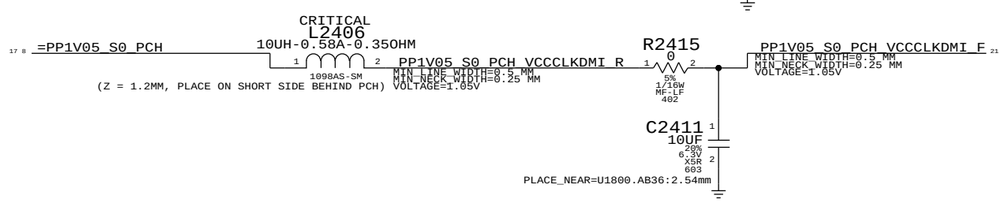

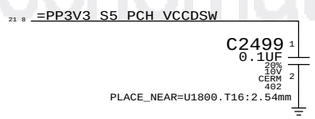

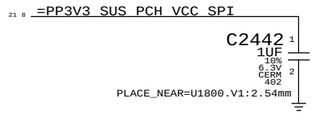

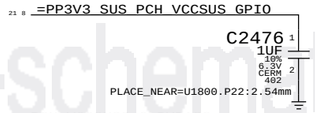

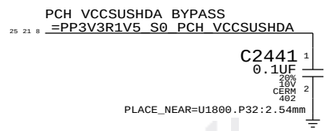

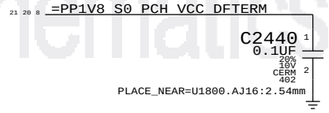

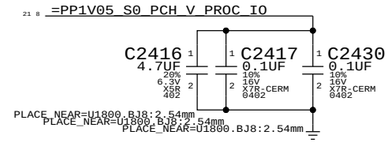

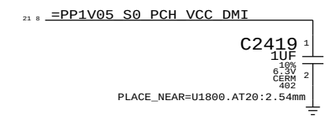

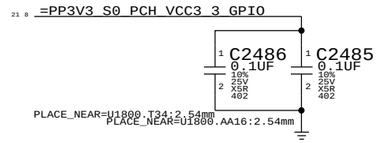

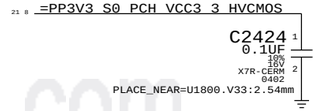

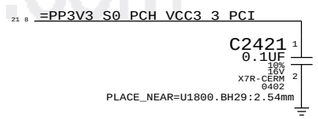

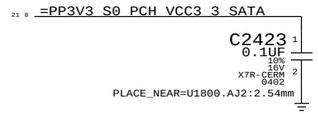

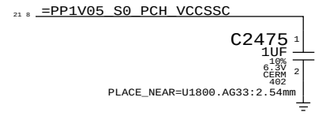

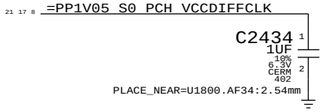

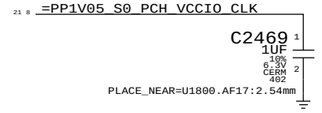

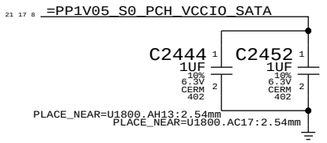

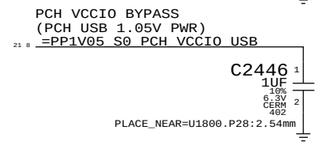

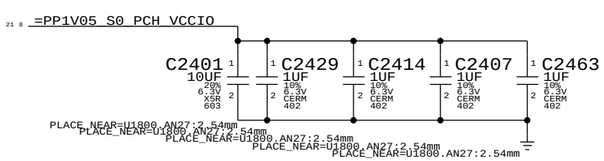

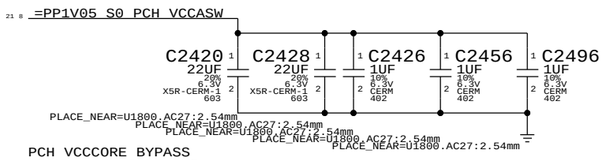

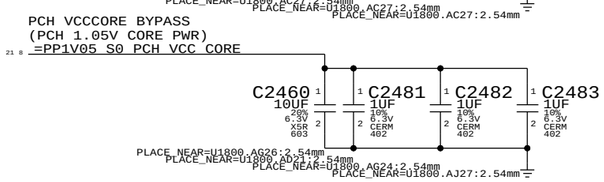

PCH VCCIO BYPASS

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

SYNC_MASTER=D2_CLEAN SYNC_DATE=03/19/2012

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

BRANCH

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CPU Micro2-XDP

=PPVCCIO_S0_XDP (24 8)

=PP3V3_S0_XDP (8) — NO STUFF — R2540[1] 1K 5% 1/16W MF LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M ST SM

998-2516

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

XDP_CPU	J2500	XDP_CPU
XDP_CPU_PREQ_L (BI)	OBSEN_A0	OBSEN_C0 — CPU_CFG<16> (IN)
XDP_CPU_PRDY_L (IN)	OBSEN_A1	OBSEN_C1 — CPU_CFG<17> (IN)
XDP_BPM_L<0> (IN)	OBSDATA_A0	OBSDATA_C0 — CPU_CFG<0> (IN)
XDP_BPM_L<1> (IN)	OBSDATA_A1	OBSDATA_C1 — CPU_CFG<1> (IN)
XDP_BPM_L<2> (IN)	OBSDATA_A2	OBSDATA_C2 — CPU_CFG<2> (IN)
XDP_BPM_L<3> (IN)	OBSDATA_A3	OBSDATA_C3 — CPU_CFG<3> (IN)
CPU_CFG<10> (IN)	OBSEN_B0	OBSEN_D0 — CPU_CFG<8> (IN)
CPU_CFG<11> (IN)	OBSEN_B1	OBSEN_D1 — CPU_CFG<9> (IN)
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0 — CPU_CFG<4> (IN)
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1 — CPU_CFG<5> (IN)
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2 — CPU_CFG<6> (IN)
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3 — CPU_CFG<7> (IN)
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4 — XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 — XDP_CPU_CLK100M_N
	VCC_OBS_AB	VCC_OBS_CD
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6 — XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7 — XDP_DBRESET_L (OUT)
=SMBUS_XDP_SDA (BI)	SDA	TDO — XDP_CPU_TDO (IN)
=SMBUS_XDP_SCL (IN)	SCL	TRSTn — XDP_CPU_TRST_L (OUT)
	TCK1	TDI — XDP_CPU_TDI (OUT)
XDP_CPU_TCK (OUT)	TCK0	TMS — XDP_CPU_TMS (OUT)
	NC	XDP_PRESENT#

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2500 0.1UF 10% 16V X7R CERM 0402 — XDP C2501 0.1UF 10% 16V X7R CERM 0402

(R2560-R2563) XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0	XDP_CPU_TDO — R2510 — 51 — XDP PLACE_NEAR=J2500.52:2.54mm
XDP_BPM_L<5>	R2561	0	XDP_CPU_TDI — R2511 — 51 — XDP PLACE_NEAR=U1000.K61:2.54mm
XDP_BPM_L<6>	R2562	0	XDP_CPU_TMS — R2512 — 51 — XDP PLACE_NEAR=U1000.H59:2.54mm
XDP_BPM_L<7>	R2563	0	XDP_CPU_TCK — R2513 — 51 — XDP PLACE_NEAR=U1000.J58:2.54mm
			XDP_CPU_TRST_L — R2514 — 51 — XDP PLACE_NEAR=U1000.H63:2.54mm

(R2564-R2567) XDP_CPU:CFG

CPU_CFG<12>	R2564	0	
CPU_CFG<13>	R2565	0	
CPU_CFG<14>	R2566	0	
CPU_CFG<15>	R2567	0	

CPU_PWRGD	R2500	1K	XDP PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L	R2502	0	XDP PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0>	R2501	1K	XDP PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK	R2504	330	XDP

R2515 0 — XDP PLACE_NEAR=R1841.1:2.54mm — ITPXDP_CLK100M_P (IN 17 89)
R2516 0 — XDP PLACE_NEAR=R1840.1:2.54mm — ITPXDP_CLK100M_N (IN 17 89)
R2505 1K — XDP PLACE_NEAR=U1000.G3:2.54mm — CPU_RESET_L (IN 11 25)

XDP SIGNALS

(R2520-R2537) XDP

XDP_DA0_USB_EXTA_OC_L (OUT)	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L (IN)
XDP_DA1_USB_EXTB_OC_L (OUT)	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L (IN)
XDP_DA2_USB_EXTC_OC_L (OUT)	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L (IN)
XDP_DA3_USB_EXTD_OC_L (OUT)	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L (IN)
XDP_DB0_USB_EXTB_OC_EHCI_L (OUT)	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L (IN)
XDP_DB1_USB_EXTD_OC_EHCI_L (OUT)	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L (IN)
XDP_DB2_AP_PWR_EN (IN)	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN (OUT)
XDP_DB3_SDCONN_STATE_CHANGE (OUT)	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE (IN)
XDP_FC0 (OUT)	R2528	33	XDP_FC0_PCH_GPIO15 (IN)
XDP_FC1 (OUT)	R2529	33	XDP_FC1_PCH_GPIO0 (IN)
XDP_DC0_ISOLATE_CPU_MEM_L (IN)	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L (OUT)
XDP_DC1_MXM_GOOD (IN)	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD (OUT)
XDP_DC2_DP_AUXCH_ISOL (IN)	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (OUT)
XDP_DC3_SATARDRVR_EN (IN)	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN (OUT)
XDP_DD0_DP_GPU_TBT_SEL (IN)	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL (OUT)
XDP_DD1_JTAG_ISP_TCK (IN)	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK (OUT)
XDP_DD2_AUD_IPHS_SWITCH_EN (IN)	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH (OUT)
XDP_DD3_ENET_LOW_PWR (IN)	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH (OUT)

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L (IN)	R2590	0	USB_EXTA_OC_L (IN)
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L (IN)	R2591	0	USB_EXTB_OC_L (IN)
XDP_DB2_PCH_GPIO10_AP_PWR_EN (OUT)	R2596	0	AP_PWR_EN (OUT)
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE (IN)	R2597	0	SDCONN_STATE_CHANGE (IN)
XDP_DC3_PCH_GPIO19_SATARDRVR_EN (OUT)	R2573	0	SATARDRVR_EN (OUT)
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L (OUT)	R2570	0	ISOLATE_CPU_MEM_L (OUT)
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (IN)	R2572	0	DP_AUXCH_ISOL (OUT)
XDP_FC1_PCH_GPIO0 (OUT)	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL (IN)
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK (OUT)	R2575	0	JTAG_ISP_TCK (OUT)
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH (OUT)	R2576	0	AUD_IPHS_SWITCH_EN_PCH (OUT)
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH (OUT)	R2577	0	ENET_LOW_PWR_PCH (OUT)

Non-XDP Signals

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
  Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

PCH Micro2-XDP

=PP3V3_S5_XDP (8)

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M ST SM

998-2516

XDP_PCH	J2550	XDP_PCH
TP_XDP_PCH_OBSFN_A<0>	OBSEN_A0	OBSEN_C0 — XDP_FC0 (24)
TP_XDP_PCH_OBSFN_A<1>	OBSEN_A1	OBSEN_C1 — XDP_FC1 (24)
XDP_DA0_USB_EXTA_OC_L (24)	OBSDATA_A0	OBSDATA_C0 — XDP_DC0_ISOLATE_CPU_MEM_L (24)
XDP_DA1_USB_EXTB_OC_L (24)	OBSDATA_A1	OBSDATA_C1 — XDP_DC1_MXM_GOOD (24)
XDP_DA2_USB_EXTC_OC_L (24)	OBSDATA_A2	OBSDATA_C2 — XDP_DC2_DP_AUXCH_ISOL (24)
XDP_DA3_USB_EXTD_OC_L (24)	OBSDATA_A3	OBSDATA_C3 — XDP_DC3_SATARDRVR_EN (24)
TP_XDP_PCH_OBSFN_B<0>	OBSEN_B0	OBSEN_D0 — TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_B<1>	OBSEN_B1	OBSEN_D1 — TP_XDP_PCH_OBSFN_D<1>
XDP_DB0_USB_EXTB_OC_EHCI_L (24)	OBSDATA_B0	OBSDATA_D0 — XDP_DD0_DP_GPU_TBT_SEL (24)
XDP_DB1_USB_EXTD_OC_EHCI_L (24)	OBSDATA_B1	OBSDATA_D1 — XDP_DD1_JTAG_ISP_TCK (24)
XDP_DB2_AP_PWR_EN (24)	OBSDATA_B2	OBSDATA_D2 — XDP_DD2_AUD_IPHS_SWITCH_EN (24)
XDP_DB3_SDCONN_STATE_CHANGE (24)	OBSDATA_B3	OBSDATA_D3 — XDP_DD3_ENET_LOW_PWR (24)
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4 — TP_XDP_PCH_HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5 — TP_XDP_PCH_HOOK5
	VCC_OBS_AB	VCC_OBS_CD
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6 — XDPPCH_PLTRST_L (IN 25)
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7 — XDP_DBRESET_L (OUT 11 24 25 89)
=SMBUS_XDP_SDA (44 24) (BI)	SDA	TDO — XDP_PCH_TDO (IN 17 24)
=SMBUS_XDP_SCL (44 24) (IN)	SCL	TRSTn — TP_XDP_PCH_TRST_L
	TCK1	TDI — XDP_PCH_TDI (OUT 17 24)
XDP_PCH_TCK (24 17) (OUT)	TCK0	TMS — XDP_PCH_TMS (OUT 17 24)
	NC	XDP_PRESENT#

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2580 0.1UF 10% 16V X7R CERM 0402 — XDP C2581 0.1UF 10% 16V X7R CERM 0402

ALL_SYS_PWRGD (70 41) (IN)	R2584	1K	XDP PLACE_NEAR=J2550.39:2.54mm
PM_PWRBTN_L (41 24 18) (OUT)	R2585	0	XDP PLACE_NEAR=U4900.P17:2.54mm

1K series R on PCH Support Page

XDP_PCH_TDO (24 17)	R2550	51	XDP PLACE_NEAR=J2550.52:2.54mm
XDP_PCH_TDI (24 17)	R2551	51	XDP PLACE_NEAR=U1800.K5:2.54mm
XDP_PCH_TMS (24 17)	R2552	51	XDP PLACE_NEAR=U1800.H7:2.54mm
XDP_PCH_TCK (24 17)	R2556	51	XDP PLACE_NEAR=U1800.J3:2.54mm

=PP1V05_SUS_PCH_JTAG (8)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: CPU & PCH XDP

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BRANCH
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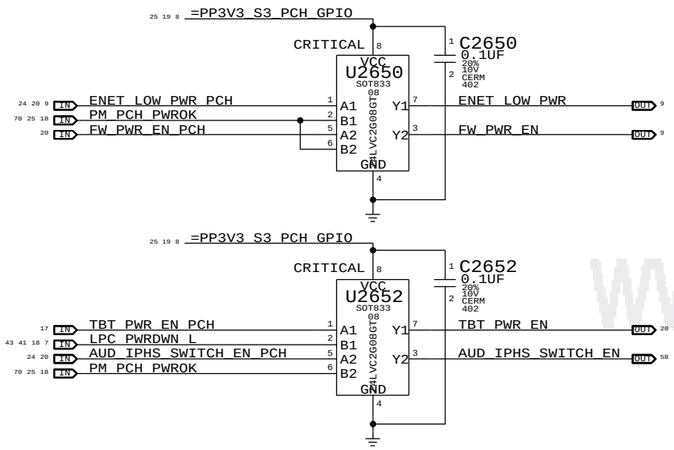
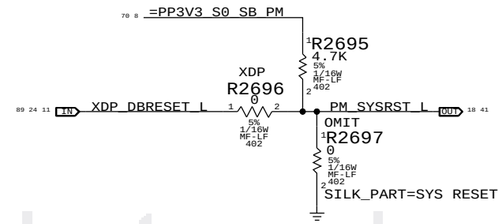
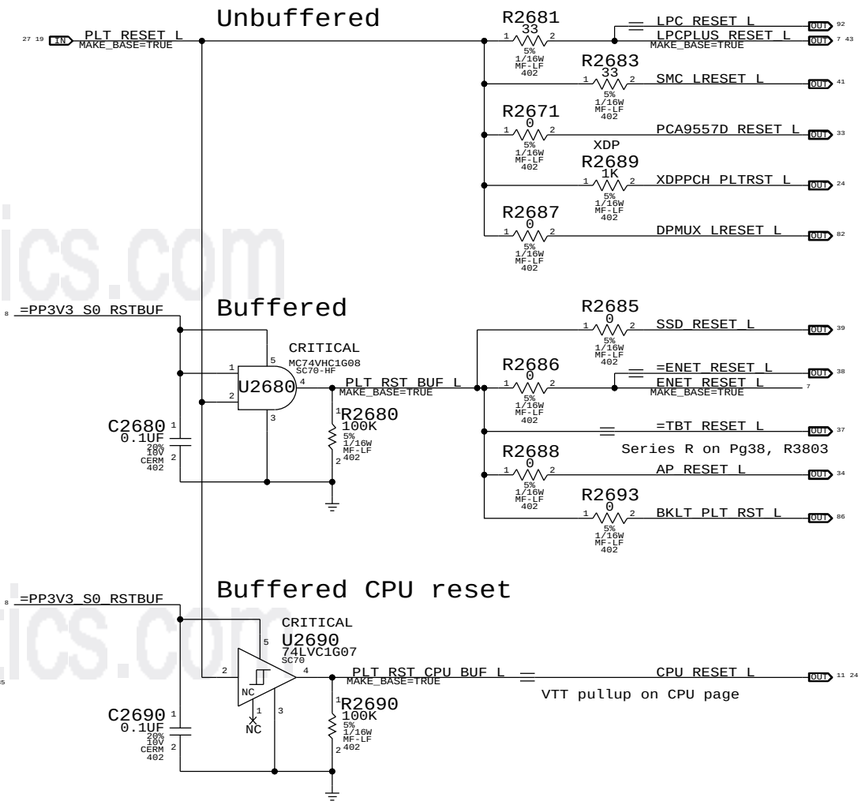
GPIO Glitch Prevention



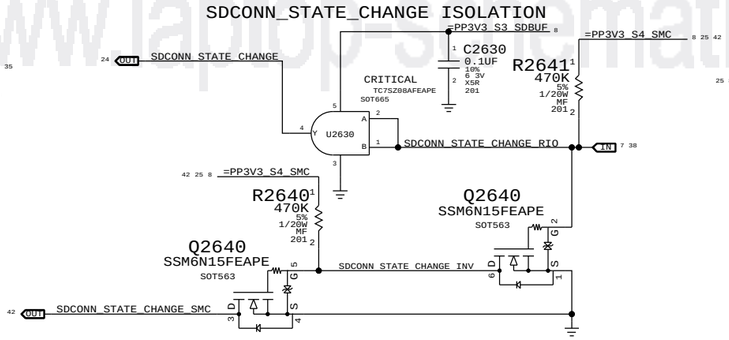
PCH Reset Button



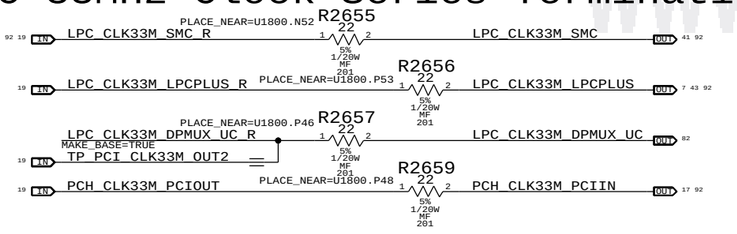
Platform Reset Connections



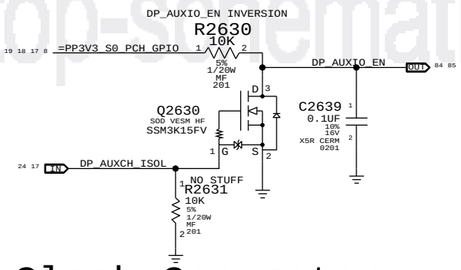
SDCONN_STATE_CHANGE ISOLATION



LPC 33MHz Clock Series Termination



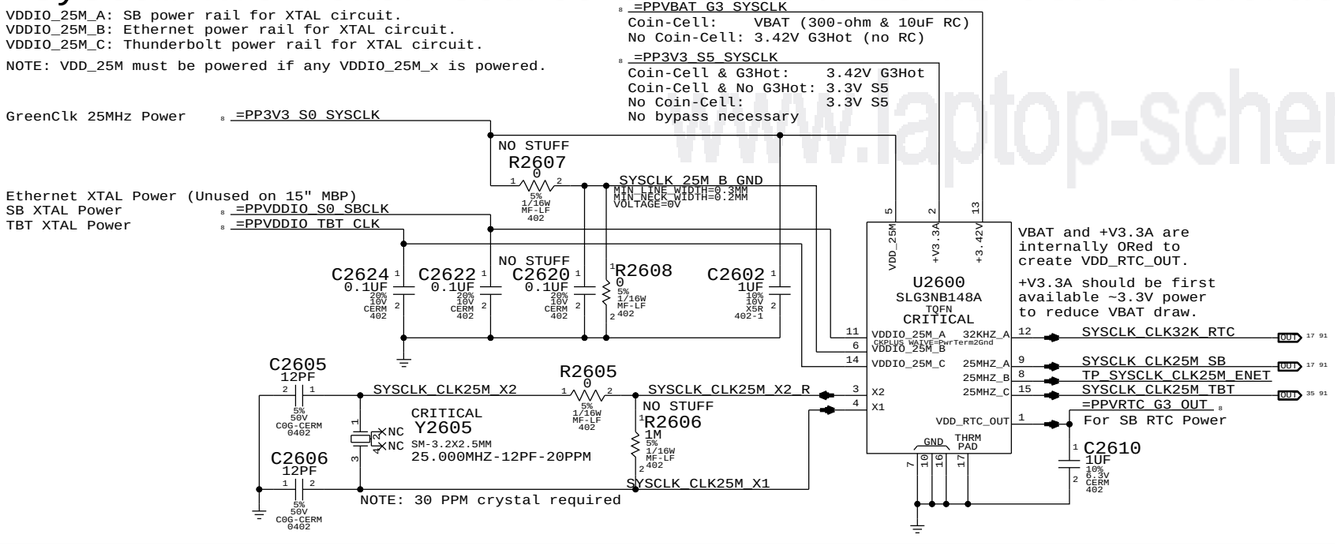
DP_AUXIO_EN INVERSION



System RTC Power Source & 32kHz / 25MHz Clock Generator

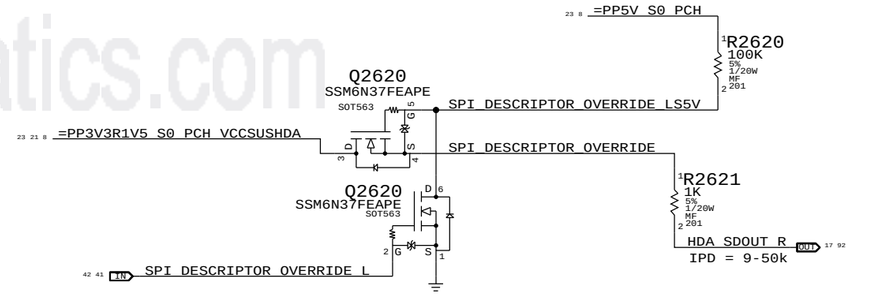
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Chipset Support

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

USB MUX FOR LS/FS INTERNAL DEVICES

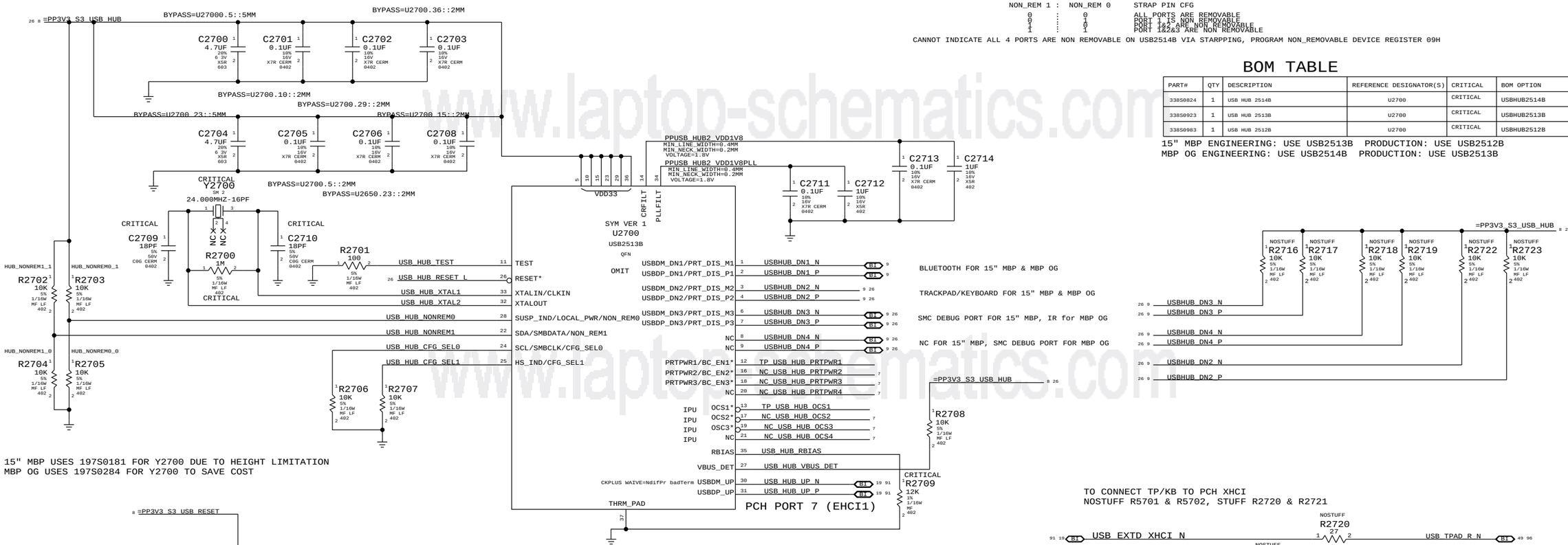
```
NON_REM 1 :  NON_REM 0     STRAP PIN CFG
     0    :      0        ALL PORTS ARE REMOVABLE
     0    :      1        PORT 1 IS NON REMOVABLE
     1    :      0        PORT 1&2 ARE NON REMOVABLE
     1    :      1        PORT 1&2&3 ARE NON REMOVABLE
```

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

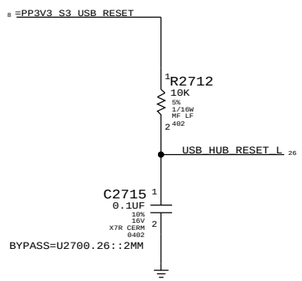
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

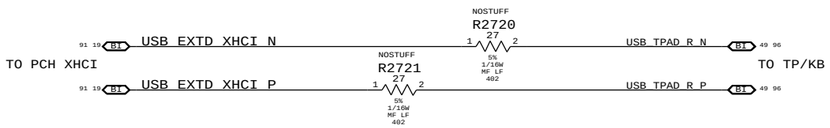
15" MBP ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
MBP OG ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



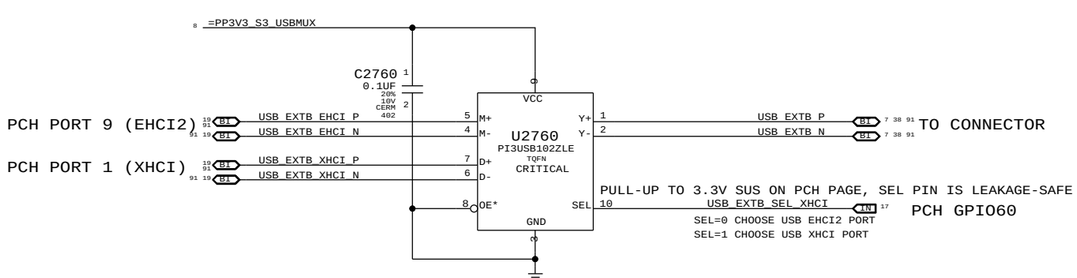
15" MBP USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
MBP OG USES 197S0284 FOR Y2700 TO SAVE COST



TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC_MASTER=D2 KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: USB HUB & MUX

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
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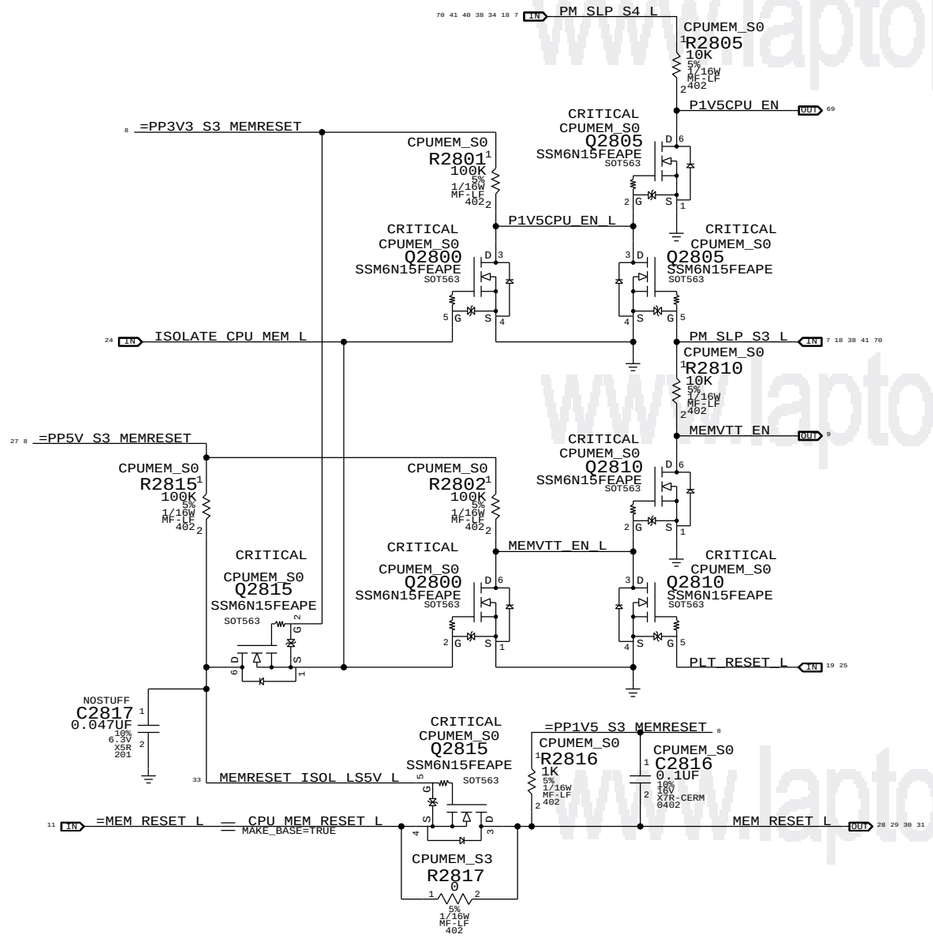
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0365	1	RES MTL FILM 1/16W 33 2K 1 0402 SMD LF	R2821		PPDDR:1V5
114S0376	1	RES MTL FILM 1/16W 43 2K 1 0402 SMD LF	R2821		PPDDR:1V35

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



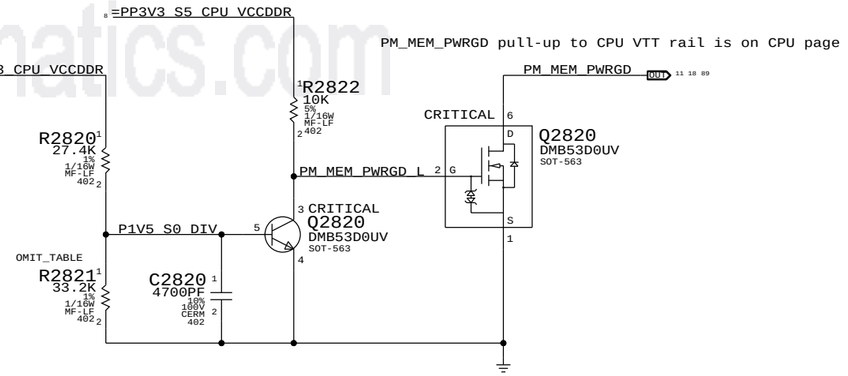
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

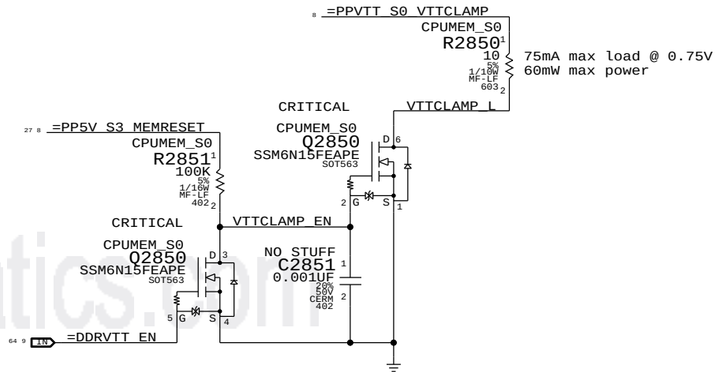
1V5 S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D
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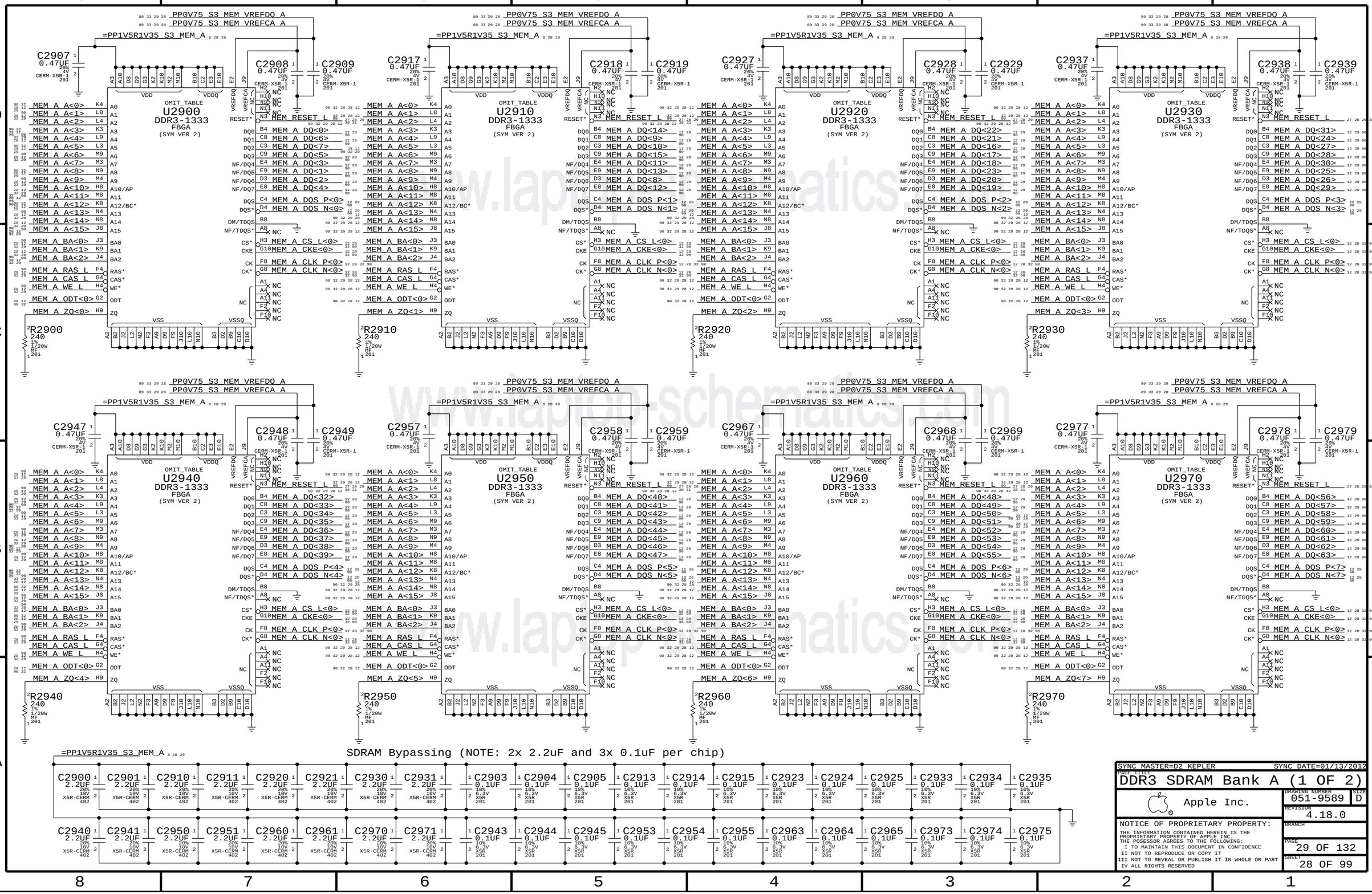

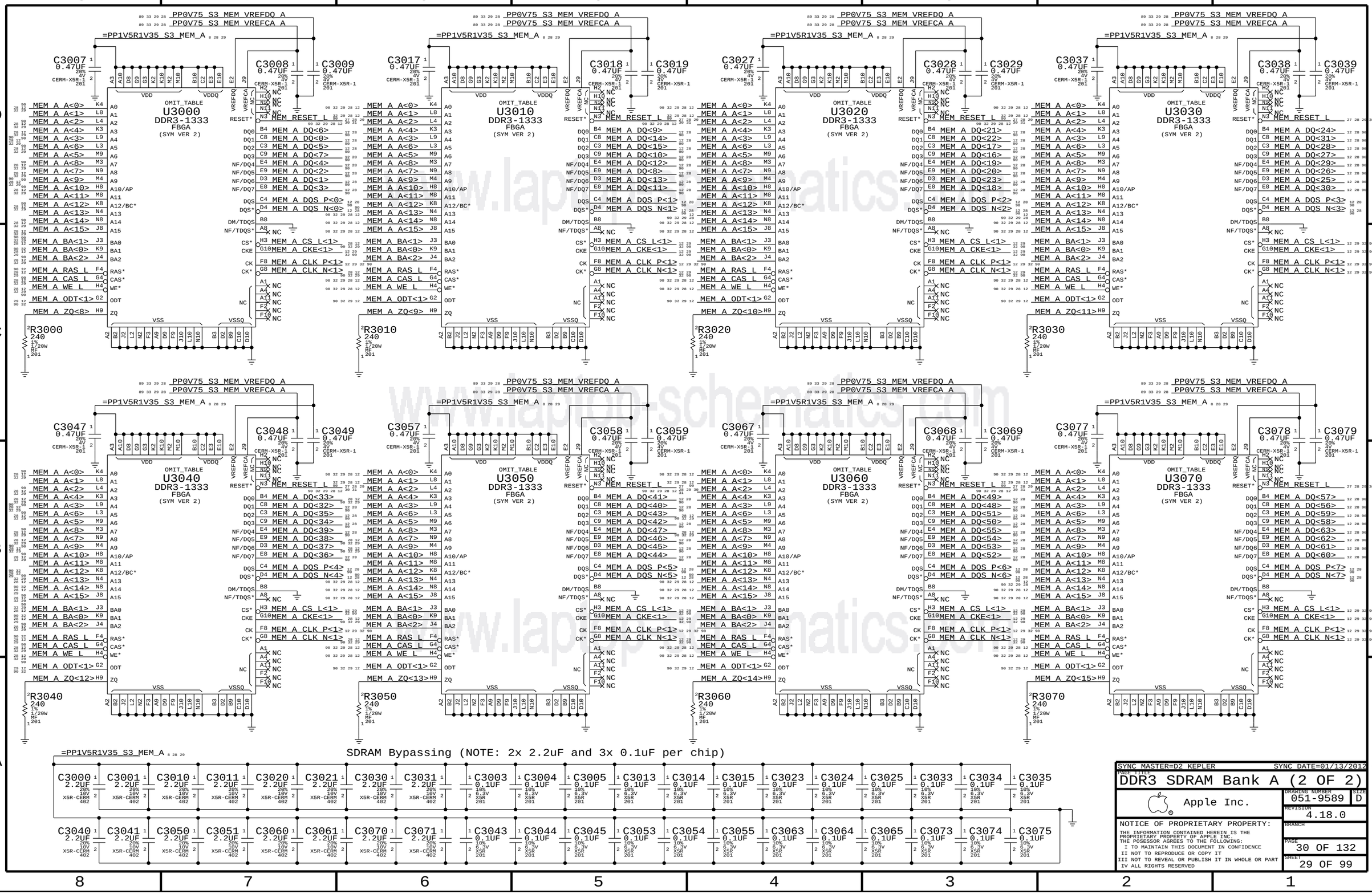

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D
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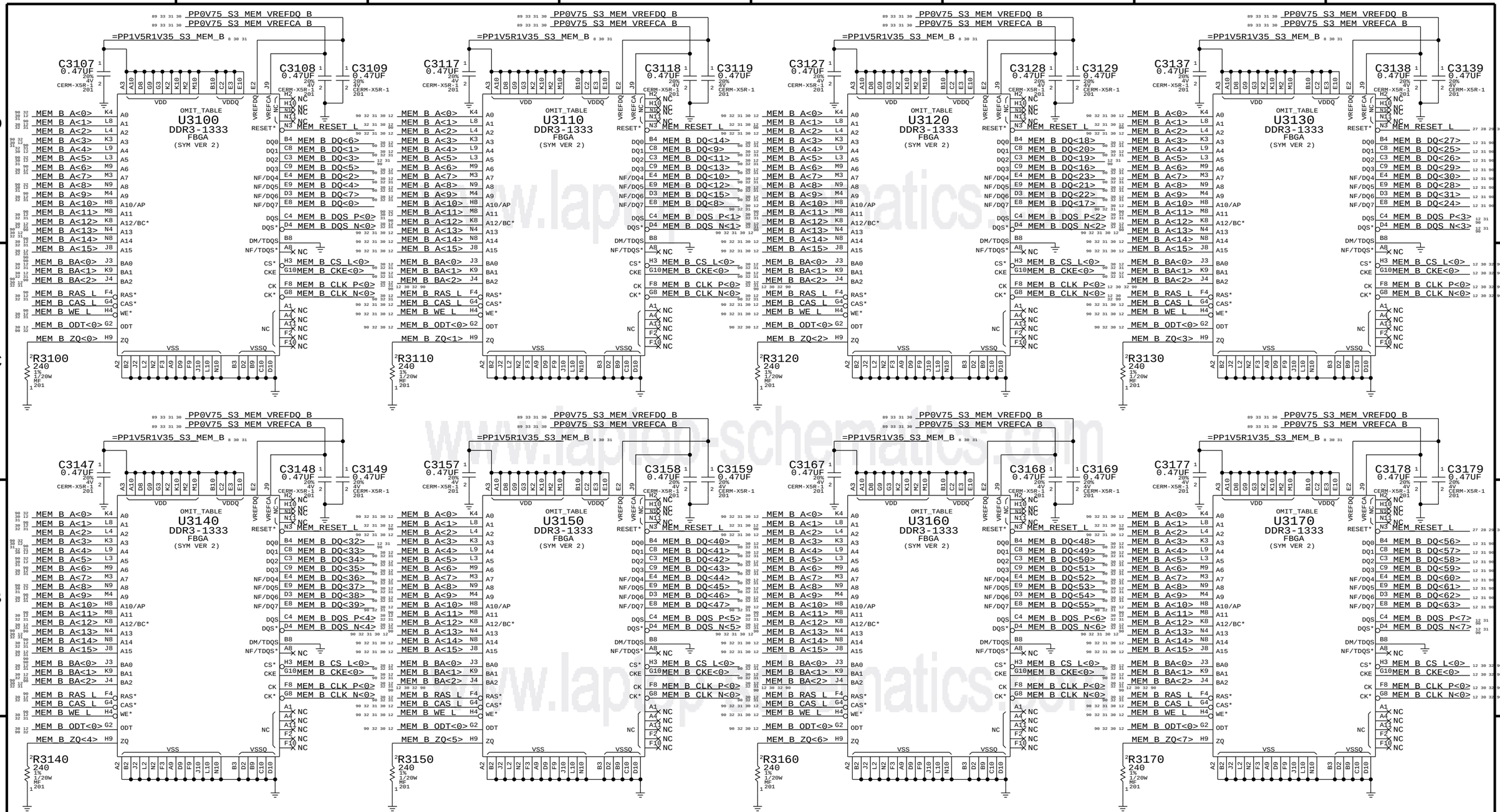

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

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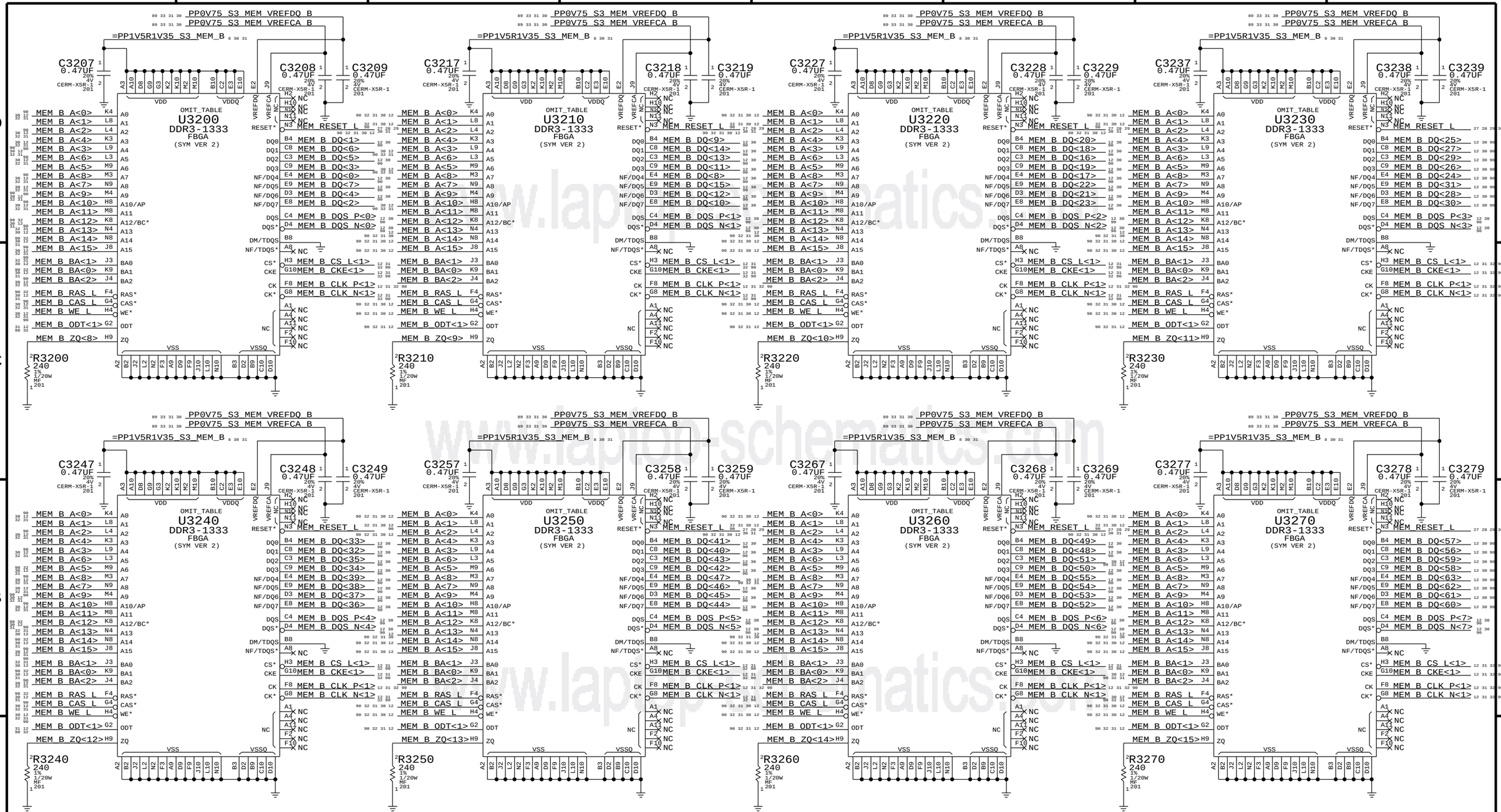

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE_TITLE
DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

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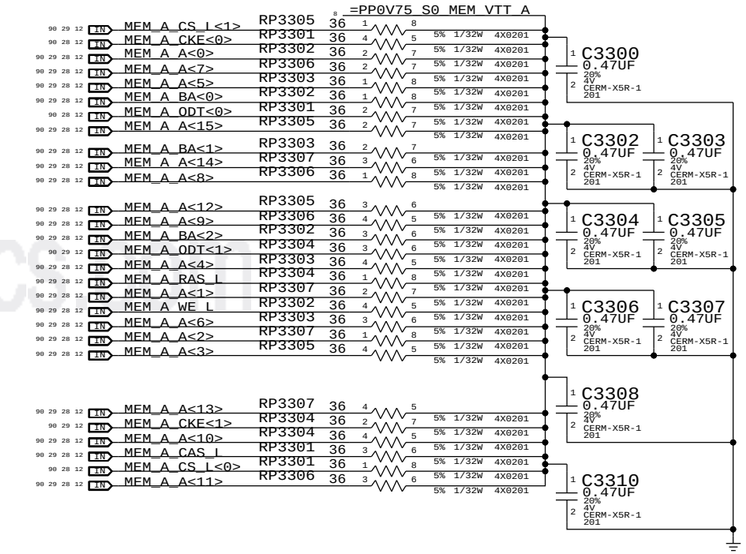
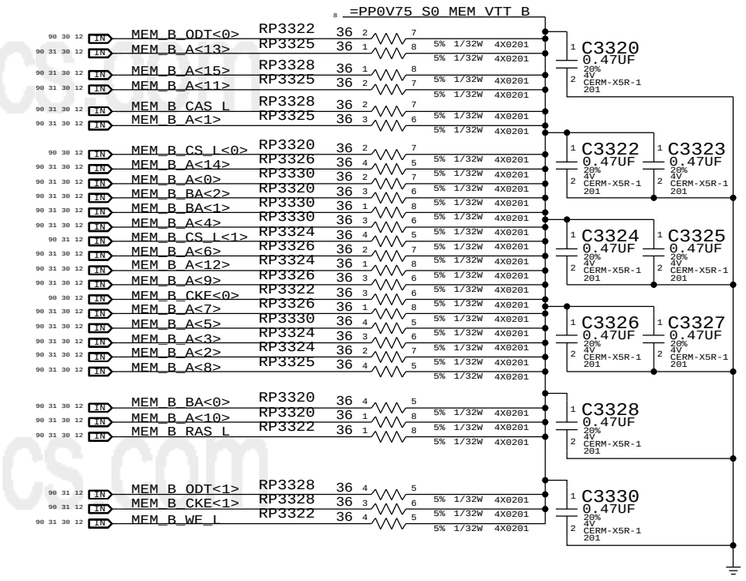
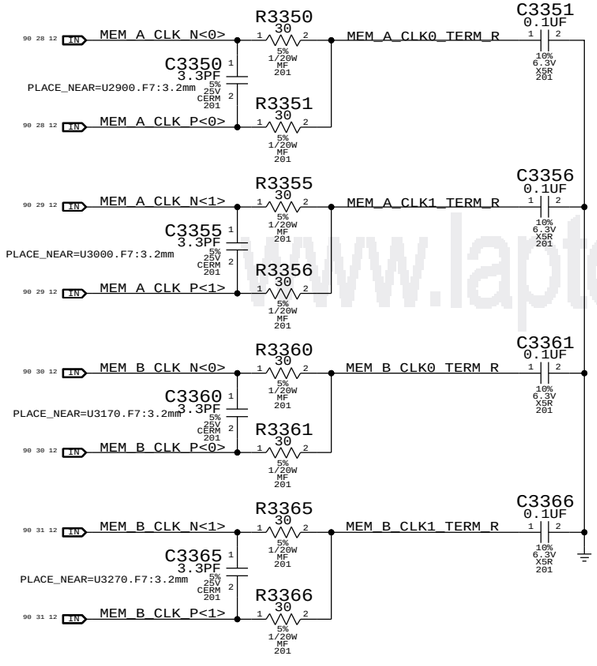
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DDR3 Termination

Apple Inc.

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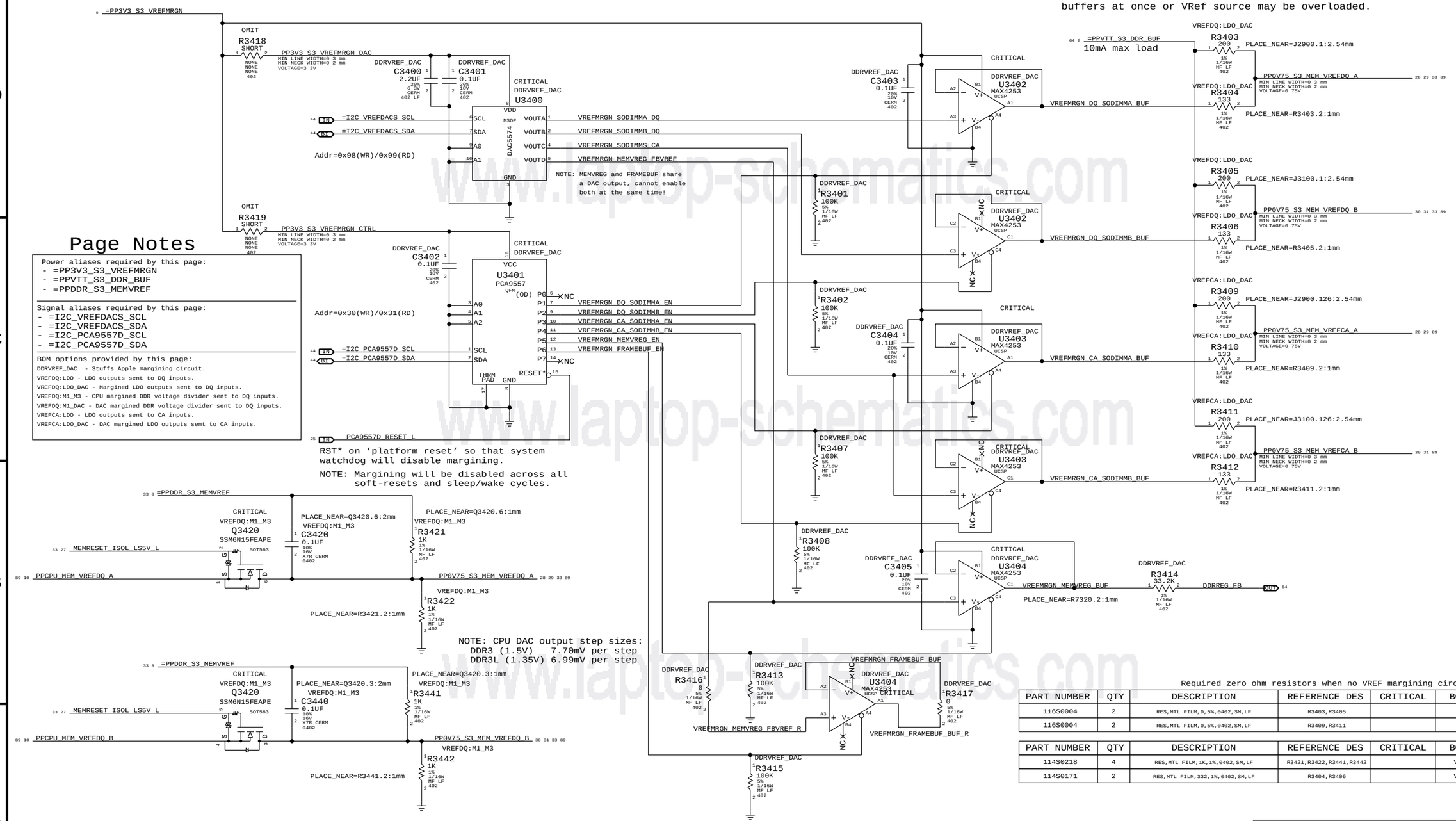

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES 00HM 0201	L3570 L3571 L3573 L3574		

AIRPORT

OMIT_TABLE
L3570
0.6NH+/-0.1NH-0.85A
0201
92 PCIE_AP_R2D_PI_P
PLACE NEAR=J3501 15 2 54MM
C3531
0 1UF 10% 16V X7R CERM0402
PCIE_AP_R2D_C_P IN 17 92
NOSTUFF C3570 0 1UF 10% 16V XSR CERM 0201
NOSTUFF C3571 0 1UF 10% 16V XSR CERM 0201

L3571
0.6NH+/-0.1NH-0.85A
0201
92 PCIE_AP_R2D_PI_N
C3530 0 1UF 10% 16V X7R CERM0402
PCIE_AP_R2D_C_N IN 17 92
PLACE NEAR=J3501 17 2 54MM
WIFI_EVENT_L IN 7 41 42
NOSTUFF C3572 0 1UF 10% 16V XSR CERM 0201
NOSTUFF C3573 0 1UF 10% 16V XSR CERM 0201
OMIT_TABLE

OMIT_TABLE
L3573
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_P OUT 17 92
92 7 PCIE_AP_R2D_P
92 7 PCIE_AP_R2D_N
NOSTUFF C3574 0 1UF 10% 16V XSR CERM 0201
NOSTUFF C3575 0 1UF 10% 16V XSR CERM 0201

L3574
0.6NH+/-0.1NH-0.85A
0201
PCIE_AP_D2R_N OUT 17 92
NOSTUFF C3576 0 1UF 10% 16V XSR CERM 0201
NOSTUFF C3577 0 1UF 10% 16V XSR CERM 0201
OMIT_TABLE
92 7 PCIE_AP_D2R_PI_P
92 7 PCIE_AP_D2R_PI_N

CRITICAL
514S0335
J3501
SSD-K99
F-RT-SM1

CRITICAL
L3501
90 OHM 100MA
DLP11S
SYM_VER 1
96 7 PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_P IN 17 92
96 7 PCIE_CLK100M_AP_CONN_N
PCIE_CLK100M_AP_N IN 17 92
PLACE NEAR=J3501 11 2 54MM

PCIE_WAKE_L OUT 7 18

91 7 USB_BT_CONN_N
91 7 USB_BT_CONN_P

PP3V3_S3RS4_BT_F
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=3.3V
C3532 0 01UF 10% 16V X7R CERM 0402
BTPWR:S4 L3505 FERR-120-OHM-1.5A 0402 LF =PP3V3_S4_BT 8
PLACE NEAR J3501 27 2 54MM
BTPWR:S3 L3506 FERR-120-OHM-1.5A 0402 LF =PP3V3_S3_BT 8
PLACE NEAR J3501 27 2 54MM

BLUETOOTH

PP3V3_S3RS4_BT_F 7 34
NOSTUFF R3517 15K 1% 1/20W MF 201
BTPWR:S3 R3518 0 5% 1/20W MF 201
C3510 0.1UF 10% 6.3V X5R 201
NOSTUFF R3514 15K 1% 1/20W MF 201
SIGNAL_MODEL=EMPTY
BTPWR:S4 Q3510 SSM3K15FV SOD-VESM-HF
=BT_WAKE_L OUT 42
NOSTUFF R3515 15K 1% 1/20W MF 201
NOSTUFF R3516 15K 1% 1/20W MF 201
U3510 PI3USB102ZLE TQFN CRITICAL
USB_BT_WAKE_P
USB_BT_WAKE_N
USB_BT_P BI 9 91
USB_BT_N BI 9 91
BTPWR:S4 R3512 15K 1% 1/20W MF 201
NOSTUFF R3513 15K 1% 1/20W MF 201
BTPWR:S4 R3511 0 5% 1/20W MF 201
PM_SLP_S4_L IN
BTMUX_SEL
NOSTUFF C3511 0.01UF 10% 16V X7R-CERM 0402

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

7 AP_RESET_CONN_L
7 AP_CLKREQ_Q_L

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0767	1	CONN HDR TWIN:AX F 0 4MM GP HF	J3502	CRITICAL	

OMIT
CRITICAL
J3502
CCR20-6K710S
F RT SM
=I2C_ALS_SDA BI 44
=I2C_ALS_SCL IN 44
7 PP5V_S3_ALSCAMERA_F
91 7 USB_CAMERA_CONN_N
91 7 USB_CAMERA_CONN_P

ALS CAMERA

MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=5V
CRITICAL
L3507
90 OHM
DLP0NS
SYM_VER 1
USB_CAMERA_N BI 19 91
USB_CAMERA_P BI 19 91
PLACE NEAR J3502 3 2 54MM

275 mA peak
206 mA nominal max
PLACE NEAR J3502 6 2 54MM
L3508
FERR-120-OHM-1.5A
0402 LF
=PP5V_S3_ALSCAMERA 8
C3552 0.1uF 20% 10V CERM 402

CURRENT SENSE

155S0367
L3504
FERR-120-0HM-3A
1A PEAK
0603
42 7 PP3V3_WLAN
MIN LINE WIDTH=1 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=3.3V
PP3V3_WLAN_F IN 34 99
MIN LINE WIDTH=1 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=3.3V
C3522 0 1uF 20% 10V CERM 402
PLACE NEAR J3501 29 2 54MM
C3521 0 1uF 20% 10V CERM 402
PLACE NEAR J3501 29 2 54MM
PP3V3_WLAN_R OUT
MIN LINE WIDTH=1 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=3.3V

3V S3 WLAN FET

MOSFET	DMP2018LFK
CHANNEL	P TYPE
RDS(ON) @ 2 5V	14 mOhm Typ 20 mOhm Max
LOADING	1 A (EDP)

CRITICAL
Q3550
DMP2018LFK
DFN2563-6
=PP3V3_S3_WLAN 8 34
C3551 0 033UF 10% 16V X5R 402
R3551 10K 5% 1/16W MF LF 402
C3550 0 1UF 10% 16V X7R CERM 0402
R3550 33K 5% 1/16W MF LF 402
P3V3WLAN_SS
PM_WLAN_EN_L IN 70

Supervisor & CLKFREG # Isolation

Delay = 130 ms +/- 20%

PP3V3_WLAN_F 34 99
=PP3V3_S3_WLAN 8 34
R3553 100K 1% 1/16W MF-LF 402
R3554 232K 1% 1/16W MF LF 402
P3V3WLAN_VMON
CRITICAL
U3540
SLG4AP041V
TDFN
SENSE
VREF
DLY
RESET* AP_RESET_L IN 25
MR*
EN AP_PWR_EN IN 19 24 70
OUT AP_CLKREQ_L OUT 17
IN
THRM PAD
GND
C3540 0.1uF 20% 10V CERM 402
R3555 100K 1% 1/16W MF-LF 402

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
X29/ALS/CAMERA CONNECTOR

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SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C3620 0.1UF	DP_TBTSNK0_ML_P<0>	7 35 95
DP_TBTSNK0_ML_C_N<0>	C3621 0.1UF	DP_TBTSNK0_ML_N<0>	7 35 95
DP_TBTSNK0_ML_C_P<1>	C3622 0.1UF	DP_TBTSNK0_ML_P<1>	7 35 95
DP_TBTSNK0_ML_C_N<1>	C3623 0.1UF	DP_TBTSNK0_ML_N<1>	7 35 95
DP_TBTSNK0_ML_C_P<2>	C3624 0.1UF	DP_TBTSNK0_ML_P<2>	7 35 95
DP_TBTSNK0_ML_C_N<2>	C3625 0.1UF	DP_TBTSNK0_ML_N<2>	7 35 95
DP_TBTSNK0_ML_C_P<3>	C3626 0.1UF	DP_TBTSNK0_ML_P<3>	7 35 95
DP_TBTSNK0_ML_C_N<3>	C3627 0.1UF	DP_TBTSNK0_ML_N<3>	7 35 95
DP_TBTSNK0_AUXCH_C_P	C3628 0.1UF	DP_TBTSNK0_AUXCH_P	7 35 95
DP_TBTSNK0_AUXCH_C_N	C3629 0.1UF	DP_TBTSNK0_AUXCH_N	7 35 95

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C3630 0.1UF	DP_TBTSNK1_ML_P<0>	7 35 95
DP_TBTSNK1_ML_C_N<0>	C3631 0.1UF	DP_TBTSNK1_ML_N<0>	7 35 95
DP_TBTSNK1_ML_C_P<1>	C3632 0.1UF	DP_TBTSNK1_ML_P<1>	7 35 95
DP_TBTSNK1_ML_C_N<1>	C3633 0.1UF	DP_TBTSNK1_ML_N<1>	7 35 95
DP_TBTSNK1_ML_C_P<2>	C3634 0.1UF	DP_TBTSNK1_ML_P<2>	7 35 95
DP_TBTSNK1_ML_C_N<2>	C3635 0.1UF	DP_TBTSNK1_ML_N<2>	7 35 95
DP_TBTSNK1_ML_C_P<3>	C3636 0.1UF	DP_TBTSNK1_ML_P<3>	7 35 95
DP_TBTSNK1_ML_C_N<3>	C3637 0.1UF	DP_TBTSNK1_ML_N<3>	7 35 95
DP_TBTSNK1_AUXCH_C_P	C3638 0.1UF	DP_TBTSNK1_AUXCH_P	7 35 95
DP_TBTSNK1_AUXCH_C_N	C3639 0.1UF	DP_TBTSNK1_AUXCH_N	7 35 95

=PP3V3_S4_TBT — R3610 47K 5% 1/20W MF 201

TBT_PCIE_RESET_L → PERST_N

TBT_PWR_ON_POC_RST_L → PWR_ON_POC_RSTN

NO STUFF C3610 0.1UF 10% 10V X5R-CERM 0201

OMIT R3615 NOSTUFF

=PP3V3_TBTLC_RTR — R3690 3.3K, R3691 3.3K, C3690 1UF, R3692 3.3K, R3693 3.3K

CRITICAL OMIT_TABLE

U3690 M95256-RMC6XG MLP

(TBT_SPI_MOSI) (TBT_SPI_CLK) (TBT_SPI_CS_L) TBTROM_WP_L TBTROM_HOLD_L (TBT_SPI_MISO)

R3625 0 5% 1/20W MF 201 — R3629 0 5% 1/20W MF 201

CRITICAL
OMIT_TABLE
U3600 CACTUSRIDGE4C FCBGA (SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_TBT_R2D_C_P<0>	C3600 0.1UF	PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_C_N<0>	C3601 0.1UF	PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_C_P<1>	C3602 0.1UF	PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_C_N<1>	C3603 0.1UF	PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_C_P<2>	C3604 0.1UF	PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_C_N<2>	C3605 0.1UF	PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_C_P<3>	C3606 0.1UF	PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_C_N<3>	C3607 0.1UF	PCIE_TBT_R2D_N<3>

TRANSMIT

PCIE_TBT_D2R_C_P<0>	C3640 0.1UF	PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_C_N<0>	C3641 0.1UF	PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_C_P<1>	C3642 0.1UF	PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_C_N<1>	C3643 0.1UF	PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_C_P<2>	C3644 0.1UF	PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_C_N<2>	C3645 0.1UF	PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_C_P<3>	C3646 0.1UF	PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_C_N<3>	C3647 0.1UF	PCIE_TBT_D2R_N<3>

MISC

RSENSE — TBT_RSENSE

RBIAS — TBT_RBIAS — R3655 1K 1% 1/20W MF 201

NC — NC

Not used in host mode.

PCIE RESET

PCIE_RST_0_N	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	TP_TBT_PCIE_RESET1_L
PCIE_RST_2_N	TP_TBT_PCIE_RESET2_L
PCIE_RST_3_N	TP_TBT_PCIE_RESET3_L

PCIE_CLKREQ_OD_N — =TBT_CLKREQ_L

EN_LC_PWR — TBT_EN_LC_PWR

CLOCKS

REFCLK_100_IN_P	PCIE_CLK100M_TBT_P
REFCLK_100_IN_N	PCIE_CLK100M_TBT_N
XTAL_25_IN	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	TP_TBT_XTAL25OUT
TMU_CLK_OUT	TBT_TMU_CLK_OUT
TMU_CLK_IN	TBT_TMU_CLK_IN

=PP3V3_TBTLC_RTR — R3698 10K — R3695 806 1% 1/20W MF 201 — SYSCLK_CLK25M_TBT — Divides 3.3V to 1.8V

R3697 100K — NO STUFF R3699 10K — R3696 1K

R3681 0 5% 1/20W MF 201

R3632 100K 5% 1/20W MF 201

=PP3V3_TBTLC_RTR — R3680 10K — TBT_DDC_XBAR_EN_L

TBT_GPIO_9

TBT_GPIO_14 — NO STUFF R3683 10K — R3682 10K

CR HPD INPUTS (S4) FORWARDED TO GMUX (S0)

=PP3V3_S0_DPMUX_UC — NOSTUFF U3610 74LVC2G126GT/S500 SOT833

DP_TBTPB_HPD → DP_TBTPB_HPD_BUF

TBT_PWR_REQ_L

TBT_EN_CIO_PWR_L — MAKE BASE TRUE

R3644 100K

NOSTUFF R3642 1K — DP_TBTPB_HPD_BUF_EN

=PP3V3_S0_DPMUX_UC — NOSTUFF U3610 74LVC2G126GT/S500 SOT833

DP_TBTPA_HPD → DP_TBTPA_HPD_BUF

R3645 100K

NOSTUFF R3643 1K — DP_TBTPA_HPD_BUF_EN

=PP3V3_S4_TBT — R3685 10K — R3686 10K

TBT_A_DP_PWRDN

TBT_B_DP_PWRDN

TBT_A_HV_EN

TBT_B_HV_EN — R3688 10K — R3687 10K

DISPLAYPORT

SINK PORT 0

DP_TBTSNK0_ML_P<3>	DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	DPSNK0_AUX_N
DP_TBTSNK0_HPD	DPSNK0_HPD

SINK PORT 1

DP_TBTSNK1_ML_P<3>	DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	DPSNK1_AUX_N
DP_TBTSNK1_HPD	DPSNK1_HPD

SOURCE PORT 0

DPSRC_3_P	TP_DP_TBTSRC_ML_CP<3>
DPSRC_3_N	TP_DP_TBTSRC_ML_CN<3>
DPSRC_2_P	TP_DP_TBTSRC_ML_CP<2>
DPSRC_2_N	TP_DP_TBTSRC_ML_CN<2>
DPSRC_1_P	TP_DP_TBTSRC_ML_CP<1>
DPSRC_1_N	TP_DP_TBTSRC_ML_CN<1>
DPSRC_0_P	TP_DP_TBTSRC_ML_CP<0>
DPSRC_0_N	TP_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P	TP_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N	TP_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD	DP_TBTSRC_HPD

JTAG/TEST PORT

JTAG_TBT_TDI	TDI
JTAG_TBT_TMS	TMS
JTAG_TBT_TCK	TCK
JTAG_TBT_TDO	TDO
TBT_TEST_EN	TEST_EN
TBT_TEST_PWR_GOOD	TEST_PWR_GOOD

EEPROM

TBT_SPI_MOSI	EE_DI
TBT_SPI_MISO	EE_DO
TBT_SPI_CS_L	EE_CS_N
TBT_SPI_CLK	EE_CLK

PORTS

PORT0

TBT_A_R2D_C_P<0>	PA_CIO0_TX_P/DP_SRC_0_P
TBT_A_R2D_C_N<0>	PA_CIO0_TX_N/DP_SRC_0_N
TBT_A_D2R_P<0>	PA_CIO0_RX_P
TBT_A_D2R_N<0>	PA_CIO0_RX_N
TBT_A_CONFIG1_BUF	PA_CONFIG1/CIO_0_LSEO
TBT_A_CONFIG2_RC	PA_CONFIG2/CIO_0_LSOE

PORT1

TBT_A_R2D_C_P<1>	PA_CIO1_TX_P/DP_SRC_2_P
TBT_A_R2D_C_N<1>	PA_CIO1_TX_N/DP_SRC_2_N
TBT_A_D2R_P<1>	PA_CIO1_RX_P
TBT_A_D2R_N<1>	PA_CIO1_RX_N
TBT_A_LSTX	PA_LSTX/CIO_1_LSEO
TBT_A_LSRX	PA_LSRX/CIO_1_LSOE

DP_TBTPA_ML_C_P<1>	PA_DPSRC_1_P
DP_TBTPA_ML_C_N<1>	PA_DPSRC_1_N
DP_TBTPA_ML_C_P<3>	PA_DPSRC_3_P
DP_TBTPA_ML_C_N<3>	PA_DPSRC_3_N
DP_TBTPA_AUXCH_C_P	PA_AUX_P
DP_TBTPA_AUXCH_C_N	PA_AUX_N
DP_TBTPA_HPD	PA_DPSRC_HPD
TBT_A_HV_EN	GPIO_0/PA_HV_EN/BYP0
TBT_A_CIO_SEL	GPIO_10/PA_CIO_SEL/BYP1
TBT_A_DP_PWRDN	GPIO_12/PA_DP_PWRDN/BYP2

PORT2

TBT_B_R2D_C_P<0>	PB_CIO2_TX_P/DP_SRC_0_P
TBT_B_R2D_C_N<0>	PB_CIO2_TX_N/DP_SRC_0_N
TBT_B_D2R_P<0>	PB_CIO2_RX_P
TBT_B_D2R_N<0>	PB_CIO2_RX_N
TBT_B_CONFIG1_BUF	PB_CONFIG1/CIO_2_LSEO
TBT_B_CONFIG2_RC	PB_CONFIG2/CIO_2_LSOE

PORT3

TBT_B_R2D_C_P<1>	PB_CIO3_TX_P/DP_SRC_2_P
TBT_B_R2D_C_N<1>	PB_CIO3_TX_N/DP_SRC_2_N
TBT_B_D2R_P<1>	PB_CIO3_RX_P
TBT_B_D2R_N<1>	PB_CIO3_RX_N
TBT_B_LSTX	PB_LSTX/CIO_3_LSEO
TBT_B_LSRX	PB_LSRX/CIO_3_LSOE

TP_DP_TBTPB_ML_C_P<3>	PB_DPSRC_1_P
TP_DP_TBTPB_ML_C_N<3>	PB_DPSRC_1_N
TP_DP_TBTPB_ML_C_P<2>	PB_DPSRC_3_P
TP_DP_TBTPB_ML_C_N<2>	PB_DPSRC_3_N
TP_DP_TBTPB_AUXCH_C_P	PB_AUX_P
TP_DP_TBTPB_AUXCH_C_N	PB_AUX_N
DP_TBTPB_HPD	PB_DPSRC_HPD
TBT_B_HV_EN	GPIO_1/PB_HV_EN/BYP0
TBT_B_CIO_SEL	GPIO_11/PB_CIO_SEL/BYP1
TBT_B_DP_PWRDN	GPIO_13/PB_DP_PWRDN/BYP2

GPIO_2/GO2SX	TBT_GO2SX_BIDIR
(FORCE_PWR) GPIO_3	TBT_PWR_EN
GPIO_4/WAKE_N_OD	=TBT_WAKE_L
GPIO_5/CIO_PLUG_EVENT	TBT_CIO_PLUG_EVENT
GPIO_6/CIO_SDA_OD	=I2C_TBTRTR_SDA
GPIO_7/CIO_SCL_OD	=I2C_TBTRTR_SCL
GPIO_8/EN_CIO_PWR_OD*	(TBT_EN_CIO_PWR_L)
GPIO_9/OK2GO2SX_OD*	TBT_GPIO_9
GPIO_14	TBT_GPIO_14
GPIO_15	TBT_DDC_XBAR_EN_L

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SYNC_MASTER=D2_KEPLER — SYNC_DATE=01/13/2012

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER 051-9589 — SIZE D

REVISION 4.18.0

BRANCH

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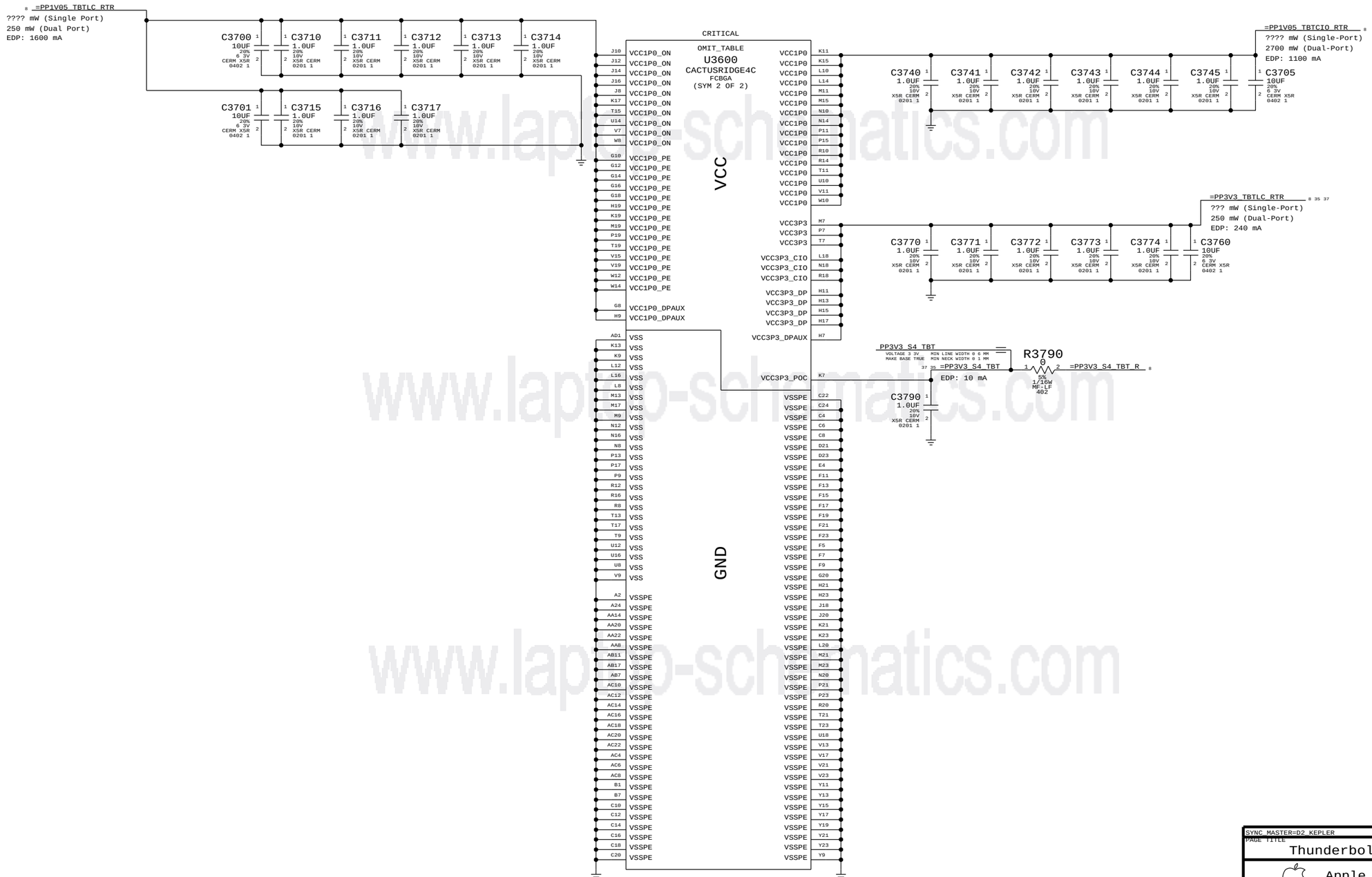

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

BRANCH:

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Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 16V X5R 402
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

CRITICAL TBTBST:Y Q3880 SI8409DB 86A

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.

TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>
TBTBST:Y C3860 10UF 20% 25V X5R-CERM 0603
TBTBST:Y C3861 10UF 20% 25V X5R-CERM 0603

CRITICAL TBTBST:Y L3895 3.3UH-6.5A PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL TBTBST:Y U3890 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

TBTBST:Y C3890 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3891 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3892 2.2UF 20% 10V X5R-CERM 402
TBTBST:Y C3887 68PF 5% 50V C0G-CERM 0402
TBTBST:Y R3893 49.9K 1% 1/16W MF-LF 402
TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3893 0.0033UF 10% 50V X7R-CERM 0402
TBTBST:Y R3894 28.7K 1% 1/16W MF-LF 402
TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX
SGND
GND
NC

TBTBST:Y R3889 0 5% 1/20W MF 201
CRITICAL TBTBST:Y D3895 PDS540XF PWRDI5
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
TBTBST:Y C3888 10PF 5% 50V C0G-CERM 0402
TBTBST:Y R3895 137K 1% 1/16W MF-LF 402 <Ra>
NO STUFF C3889 100PF 5% 50V CERM 402
TBTBST:Y R3896 15.8K 1% 1/16W MF-LF 402 <Rb>
TBTBST:Y C3895 10UF 20% 25V X5R 1206-2
TBTBST:Y C3896 20% 25V POLY-TANT CASE-D3L
NO STUFF C3897 10UF 10% 25V X5R 805
=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 300KHz
TBTBST:Y C3899 0.001UF 10% 50V X7R-CERM 0402

SGND shorted to GND inside package, no XW necessary.
Vout = 1.6V * (1 + Ra / Rb)
33UF-0.060HM

TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBT A HV EN
TBT B HV EN

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
TBTBST:Y R3888 330K 5% 1/10W MF-LF 402
Max Vgs: 10V
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K 5% 1/10W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
C3800 0.1UF 10% 16V X5R CERM 0201
Q3840 SSM3K15FV SOD-VESM-HF
R3840 10K 5% 1/20W MF 201
TBT_EN_LC_PWR
Platform (PCIe) Reset
=TBT_RESET_L
TBT_CLKREQ_L
Pull-ups provided by SB page.

CRITICAL U3800 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
THRM PAD
GND

=PP3V3_TBTLC_RTR
R3807 100K 5% 1/20W MF 201
PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
R3811 36.5K 1% 1/20W MF 201
C3810 1UF 20% 6.3V X5R 0201
C3811 1UF 10% 6.3V CERM 402
TBT_EN_LC_3V3
TBT_EN_LC_ISOL
R3816 0 5% 1/20W MF 201
TBT_EN_LC_1V05

CRITICAL U3810 TPS22924 CSP
VIN VOUT ON GND
=PP3V3_TBTLC_FET
Max Current = 2A (85C)

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

1.05V TBT "LC" Switch

=PP1V05_S0_P1V05TBTFET
C3815 1UF 20% 6.3V X5R 0201
NOSTUFF C3816 1UF 10% 6.3V CERM 402
C3816 must be 10%
RC guarantees minimum 5ms to reach 0.5V

CRITICAL U3815 TPS22924 CSP
VIN VOUT ON GND
=PP1V05_TBTLC_FET
Max Current = 2A (85C)

U3815

Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
CRITICAL U3830 TPS3808 QFN
VDD SENSE CT RESET* MR* GND THRM PAD
Pull-up: R3610
TBTPOCRST_CT
C3831 0.0047UF 10% 25V CERM 0402
C3830 0.1UF 10% 25V X5R 402
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
TBT_PWR_ON_POC_RST_L
TBTPOCRST_MR_L
C3825 330PF 10% 16V X7R-CERM 0201
Q3825 SSM6N37FEAPE SOT563
=PP3V3_S0_PCH_GPIO
R3830 100K 5% 1/20W MF 201
TBT_SW_RESET_L

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTFET
=PP3V3_TBTLC_RTR
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q3825 SSM6N37FEAPE SOT563
TBT_EN_CIO_PWR_L

CRITICAL U3820 TPS22920 CSP
VIN VOUT ON GND
C3820 1UF 20% 6.3V X5R 0201
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	Thunderbolt Power Support
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
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516S0853

J4410
AXK732327G
F-ST-SM

25 IN	=ENET_RESET_L	1	2	PM_SLP_S3_L	IN	7 18 27 41 70	
17 7 OUT	ENET_CLKREQ_L	3	4	PM_SLP_S4_L	IN	7 18 27 34 40 41 70	
9 7 IN	SD_PWR_EN	5	6	HDMI_EG_DDC_CLK	IN	7 77	
25 7 OUT	SDCONN_STATE_CHANGE_RIO	7	8	HDMI_EG_DDC_DATA	BI	7 77	
24 7 OUT	USB_EXTB_OC_L	9	10	HDMI_HPD_L	OUT	7 42 82	
8	=PP1V5_S0_RIO	11	12				
8	=PP3V3_S3_RIO	13	14				
		15	16				
		17	18				
8	=PP3V3_S4_RIO	19	20				
44	=I2C_HDMIRDRV_SCL	21	22				
44	=I2C_HDMIRDRV_SDA	23	24				
		25	26				
		27	28				
8	=PP5V_S4_RIO	29	30				
		31	32				
			34				
			33				

SIGNAL_MODEL=EMPTY
BP4401 BEAD-PROBE SM
BP4402 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY

USB3_EXTB_TX_P — C4401 0.1UF X5R CERM 0201 10% 16V — USB3_EXTB_TX_C_P
USB3_EXTB_TX_N — C4402 0.1UF X5R CERM 0201 10% 16V — USB3_EXTB_TX_C_N
USB3_EXTB_RX_P — 12 R4403 1/20W 1% MF 201 — USB3_EXTB_RX_RC_P
USB3_EXTB_RX_N — 12 R4404 1/20W 1% MF 201 — USB3_EXTB_RX_RC_N

GND_VOID=TRUE
15PF 5% 25V NP0-CERM 0201 C4403
15PF 5% 25V NP0-CERM 0201 C4404

SIGNAL_MODEL=EMPTY
BP4403 BEAD-PROBE SM
BP4404 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
BP4405 BEAD-PROBE SM
SIGNAL_MODEL=EMPTY
BP4406 BEAD-PROBE SM

J4400
20525-130E-01
F-RT-SM

91 26 7 BI	USB_EXTB_P	1	2		
91 26 7 BI	USB_EXTB_N	3			
97 7	USB3_EXTB_TX_C_P		4	GND_VOID=TRUE	
97 7	USB3_EXTB_TX_C_N		5	GND_VOID=TRUE	
		6			
97	USB3_EXTB_RX_RC_P		7	GND_VOID=TRUE	
97	USB3_EXTB_RX_RC_N		8	GND_VOID=TRUE	
		9			
95 77 7 IN	HDMI_EG_DATA_C_P<0>		10	GND_VOID=TRUE	
95 77 7 IN	HDMI_EG_DATA_C_N<0>		11	GND_VOID=TRUE	
		12			
95 77 7 IN	HDMI_EG_DATA_C_P<1>		13	GND_VOID=TRUE	
95 77 7 IN	HDMI_EG_DATA_C_N<1>		14	GND_VOID=TRUE	
		15			
95 77 7 IN	HDMI_EG_DATA_C_P<2>		16	GND_VOID=TRUE	
95 77 7 IN	HDMI_EG_DATA_C_N<2>		17	GND_VOID=TRUE	
		18			
95 77 7 IN	HDMI_EG_CLK_C_P		19		
95 77 7 IN	HDMI_EG_CLK_C_N		20		
		21			
92 17 7 IN	PCIE_CLK100M_ENET_P		22		
92 17 7 IN	PCIE_CLK100M_ENET_N		23		
		24			
92 17 7 OUT	PCIE_ENET_D2R_P		25	GND_VOID=TRUE	
92 17 7 OUT	PCIE_ENET_D2R_N		26	GND_VOID=TRUE	
		27			
92 17 7 IN	PCIE_ENET_R2D_C_P		28	GND_VOID=TRUE	
92 17 7 IN	PCIE_ENET_R2D_C_N		29	GND_VOID=TRUE	
		30			
		31			
		33			
		34			
		35			
		36			
		37			
		38			
		39			
		40			
		41			
		32			

518S0829

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE
RIO CONNECTOR

Apple Inc.

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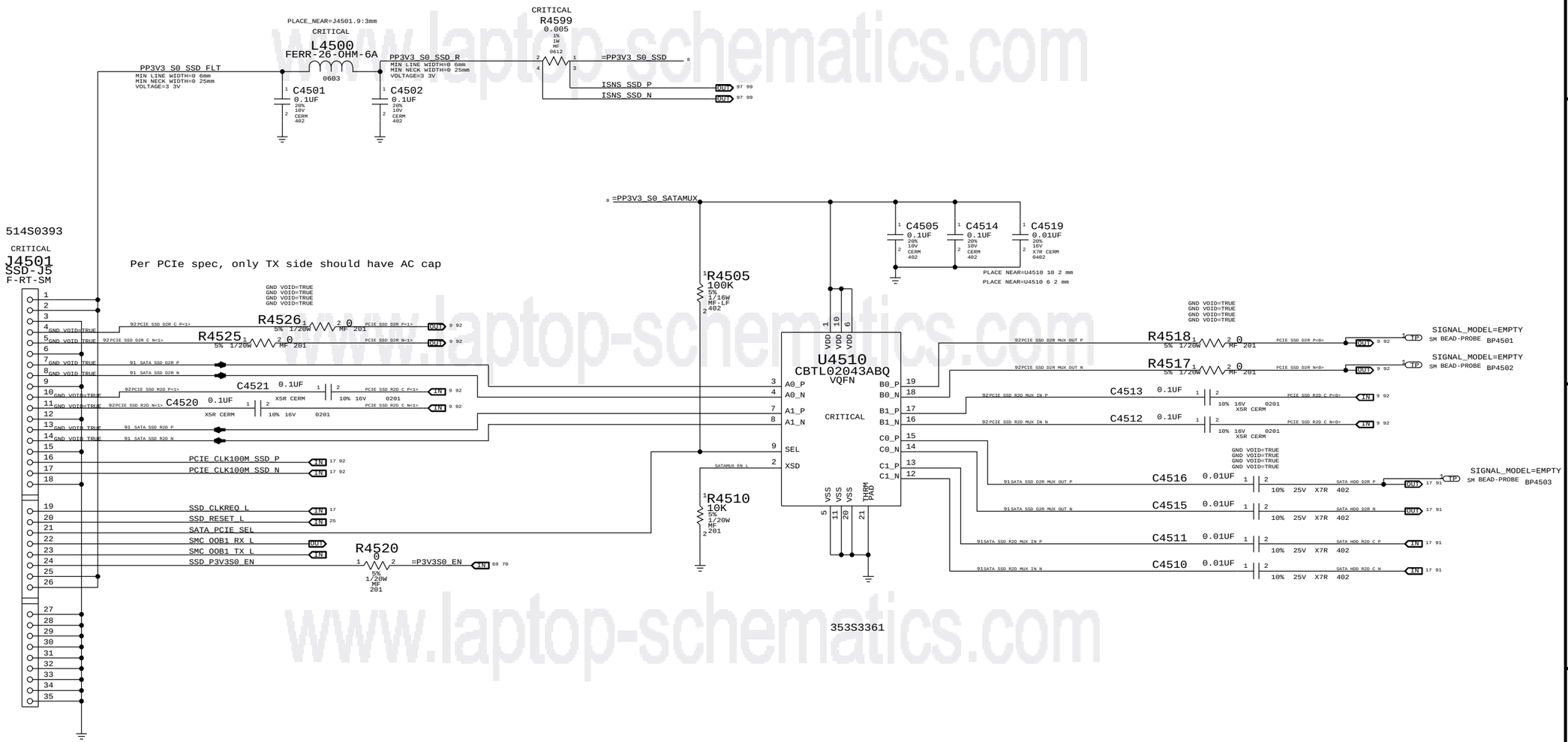

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC_MASTER=D2_KEPLER	SYNC_DATE=01/13/2012
PAGE TITLE	SSD CONNECTOR
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
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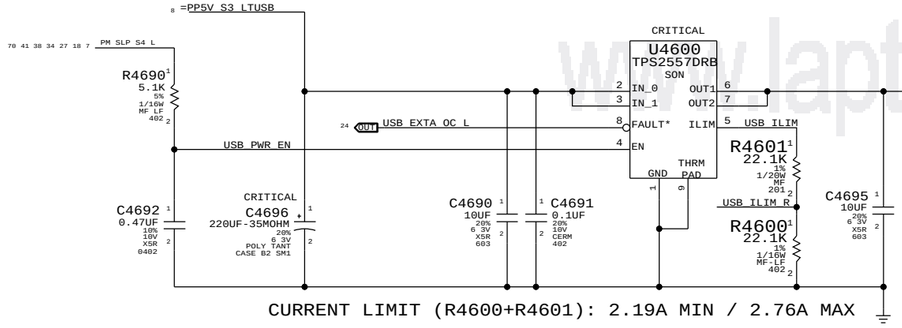
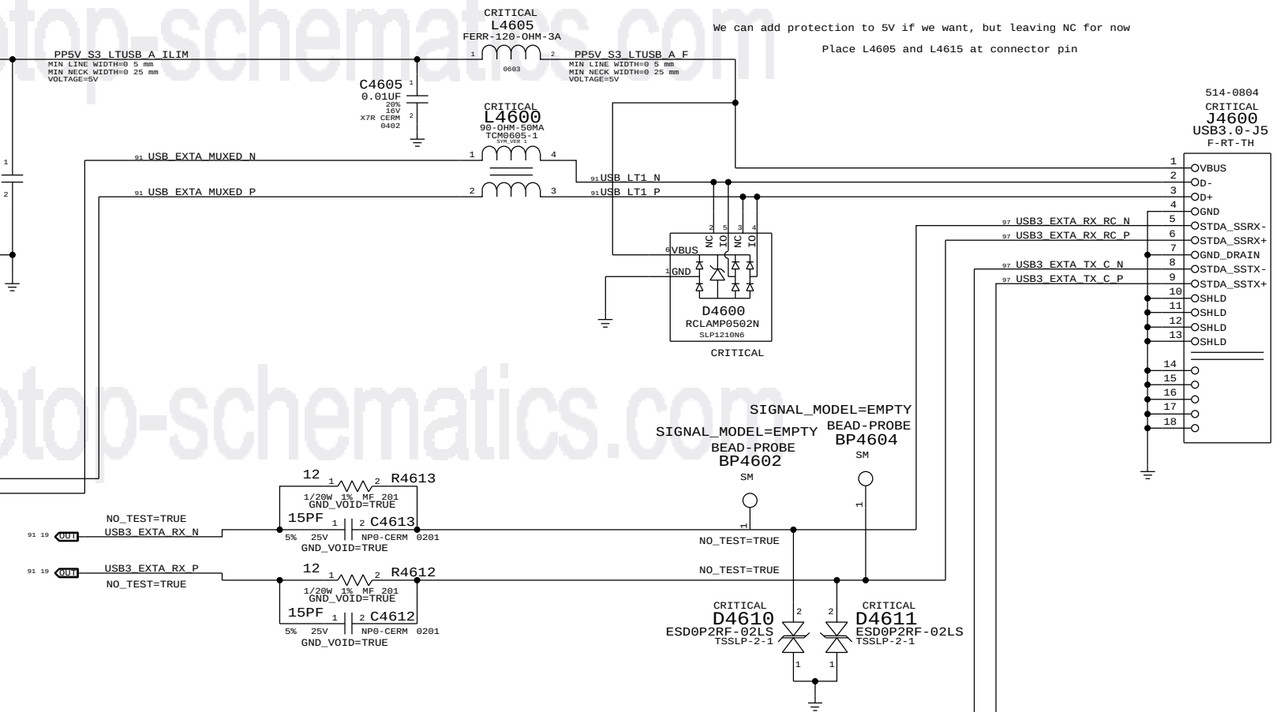
USB Port Power Switch

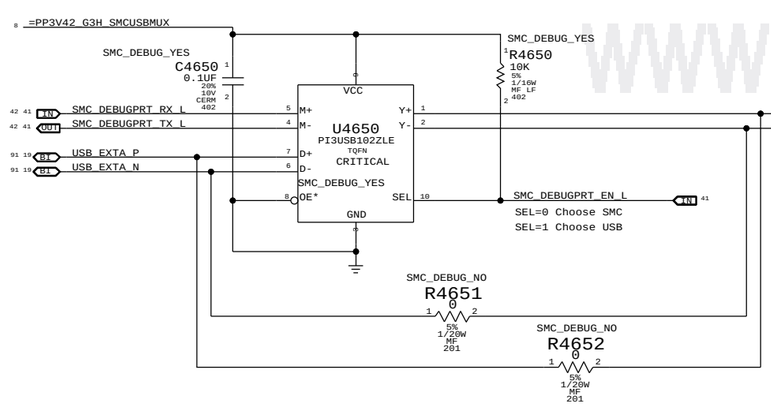


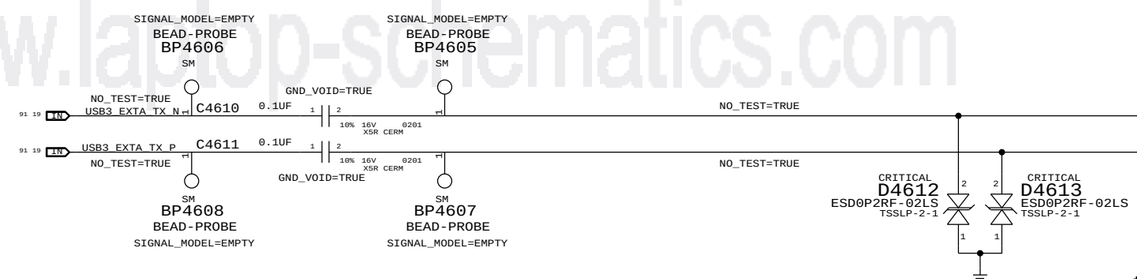
CURRENT LIMIT (R4600+R4601): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

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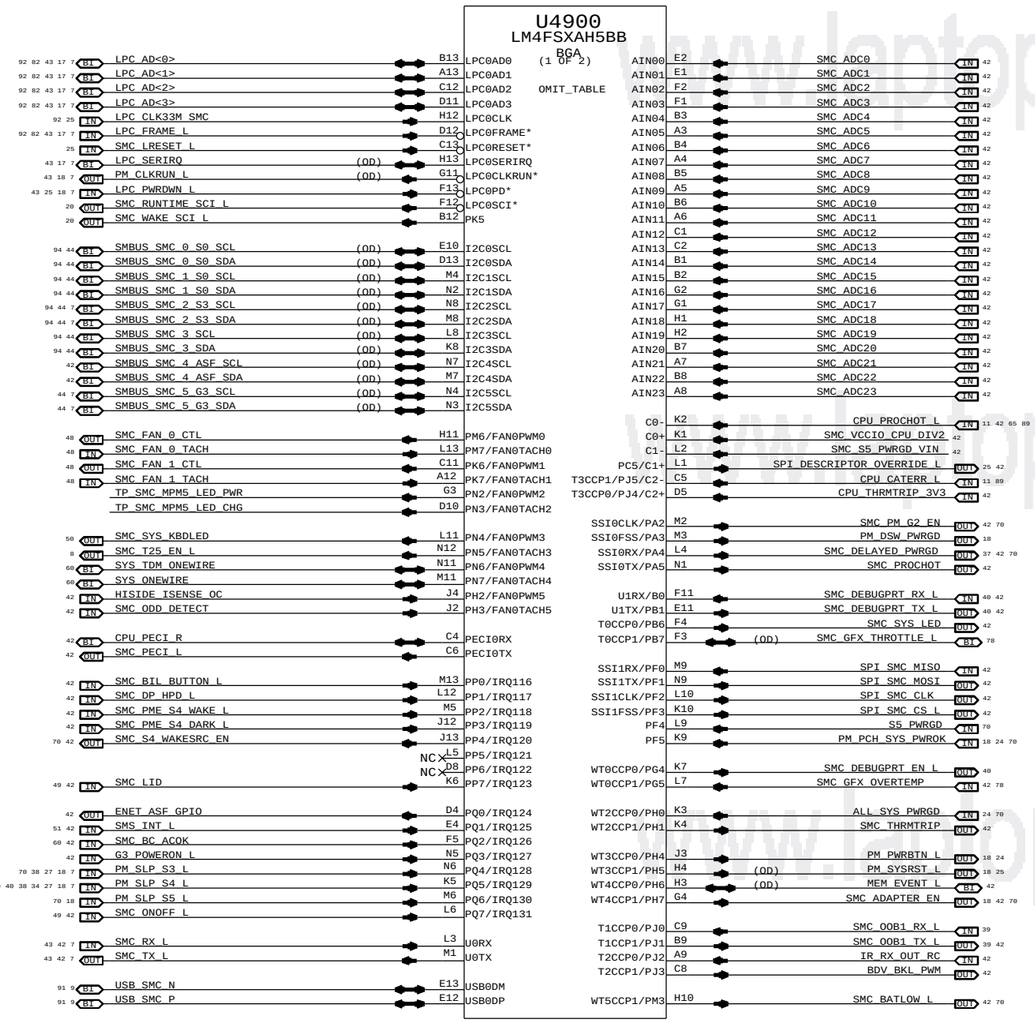
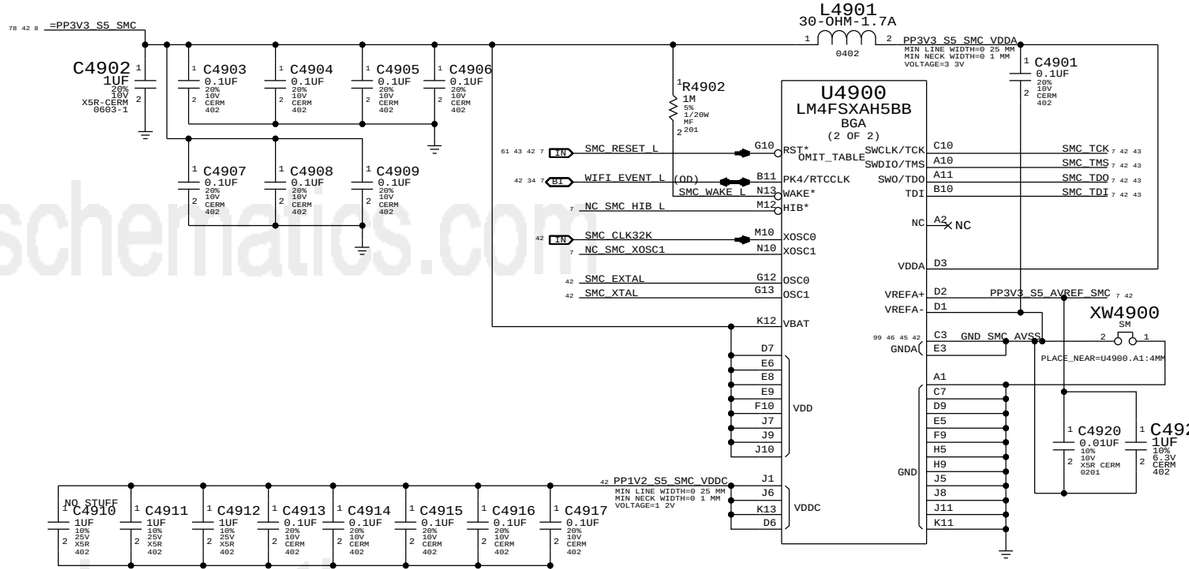
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: SMC

Apple Inc.

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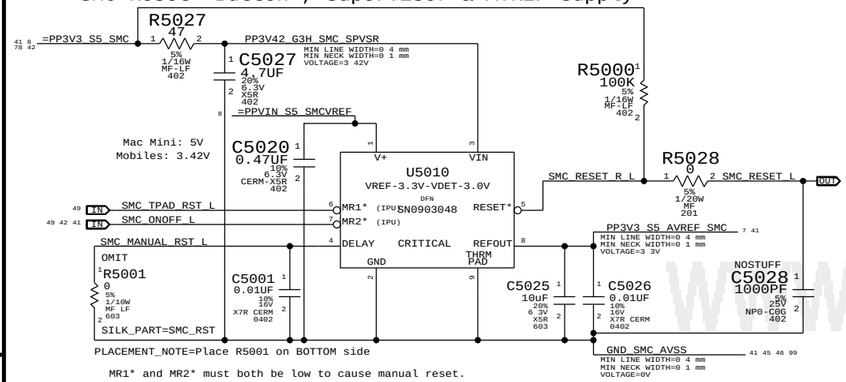
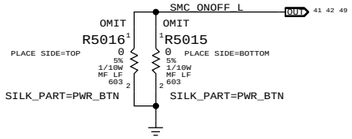
SMC Reset "Button", Supervisor & AVREF Supply



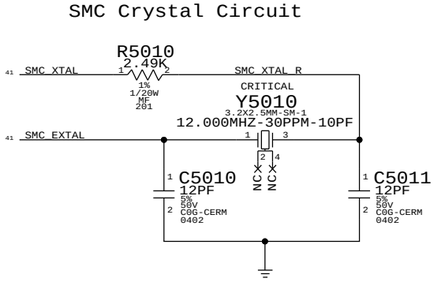
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"

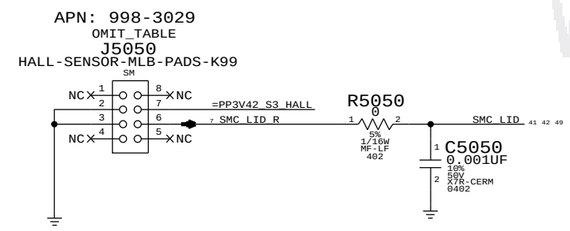


SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

Hall Effect pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5050	CRITICAL	

PP1V2_S5_SMC_VDDC
SMC_PACKAGE:ENG
R5099 0 5% 1/10W MF LF 402
SMC_ADC23

ENG PACKAGE REQUIRES 1.2V ON SMC_ADC23 PIN

=PPVCCIO_S0_SMC
R5097 100K 1% 1/20W MF 201
SMC_VCCIO_CPU_DIV2
R5096 100K 1% 1/20W MF 201

SMC_BC_ACOK — NC_HISIDE_ISENSE_OC — SMC_ADC0 — SMC_ADC1 — SMC_ADC2 — SMC_ADC3 — SMC_ADC4 — SMC_ADC5 — SMC_ADC6 — SMC_ADC7 — SMC_ADC8 — SMC_ADC9 — SMC_ADC10 — SMC_ADC11 — SMC_ADC12 — SMC_ADC13 — SMC_ADC14 — SMC_ADC15 — SMC_ADC16 — SMC_ADC17 — SMC_ADC18 — SMC_ADC19 — SMC_ADC20 — SMC_ADC21 — SMC_ADC22 — SMC_ADC23 — SMBUS_SMC_4_ASF_SCL — SMBUS_SMC_4_ASF_SDA — BDV_BKL_PWM — SMC_PME_S4_DARK_L — SMC_CHGR_ACOK

SMC_BC_ACOK — NC_HISIDE_ISENSE_OC — SMC_CPU_VSENSE — SMC_CPU_ISENSE — SMC_GPU_HI_ISENSE — SMC_DCIN_VSENSE — SMC_DCIN_ISENSE — SMC_PBUS_VSENSE — SMC_SSD_ISENSE — SMC_CHGR_BMON_ISENSE — SMC_CPU_HI_ISENSE — SMC_OTHER_HI_ISENSE — SMC_P1V5MEM_ISENSE — SMC_CPUVCCIO_ISENSE — SMC_GFX_VSENSE — SMC_CPU_SA_ISENSE — SMC_GPU_CORE_VSENSE — SMC_GPU_CORE_ISENSE — SMC_LCDBKLT_VSENSE — SMC_LCDBKLT_ISENSE — SMC_CPU_GFX_ISENSE — SMC_GPU_P1V35_ISENSE — SMC_CPU_SA_VSENSE — SMC_PCH_CORE_ISENSE — SMC_X29_ISENSE — SMC_TBT_ISENSE_R — NC_SMBUS_SMC_4_ASF_SCL — NC_SMBUS_SMC_4_ASF_SDA — NC_BDV_BKL_PWM — SDCONN_STATE_CHANGE_SMC — =TBT_WAKE_L

SMC_TBT_ISENSE — R5013 0 5% 1/10W MF LF 402 — SMC_PACKAGE:PROD

PM_CLK32K_SUSCLK_R — R5012 22 5% 1/20W MF 201 — SMC_CLK32K
PLACE_NEAR=U1800.N14:5.1mm

ENET_ASF_GPIO — NC_ENET_ASF_GPIO
SMC_SYS_LED — NC_SMC_SYS_LED
MEM_EVENT_L — NC_MEM_EVENT_L
SMC_ODD_DETECT — NC_SMC_ODD_DETECT
IR_RX_OUT_RC — NC_IR_RX_OUT_RC
MAKE BASE=TRUE

HDMI HPD ESD PROTECTION

Inversion now taking place on RIO

=PP3V3_S4_SMC
R5059 100K 5% 1/20W MF 201
R5057 1K 5% 1/20W MF 201
SMC_DP_HPD_L
HDMI_HPD_L

1K for ESD protection

CPU_THRMTRIP_3V3
CRITICAL
Q5058 MMBT3904LP-7 DFN1006-3
PM_THRMTRIP_B_L
R5058 3.3K 5% 1/20W MF 201
PM_THRMTRIP_L

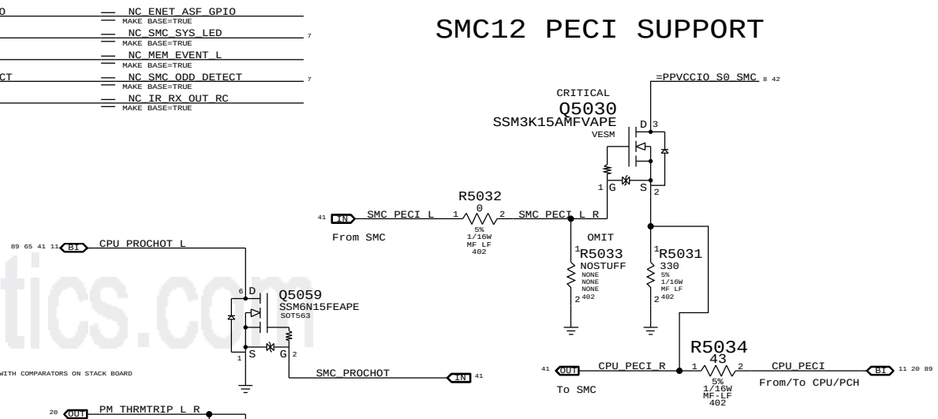
=PP3V3_S4_SMC
R5082 100K 5% 1/20W MF 201
=PSOC_WAKE_L
=BT_WAKE_L
SMC_PME_S4_WAKE_L
MAKE BASE=TRUE

BATLOW# ISOLATION

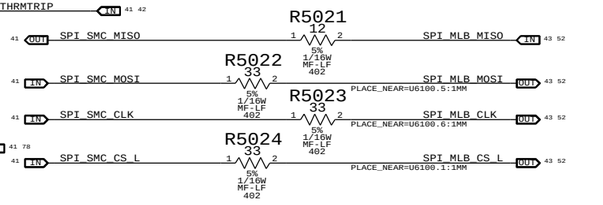
=PP3V3_S5_SMCBATLOW
R5040 100K 5% 1/20W MF 201
SMC_BATLOW_L
Q5040 SSM3K15FV SOD VESM MF
=PP3V3_SUS_SMC
PM_BATLOW_L
R5041 0 5% 1/16W MF LF 402 NOSTUFF

Internal 20K pull-up on PM_BATLOW_L in PCH.

SMC12 PECI SUPPORT



SMC12 SPI SUPPORT



=PP3V3_S5_SMC
=PP3V3_S4_SMC
NO STUFF

SMC_OOB1_TX_L	R5068	100K	1/20W	MF	201	
SMC_PME_S4_DARK_L	R5069	100K	1/20W	MF	201	
SMC_ONOFF_L	R5070	10K	1/20W	MF	201	
G3_POWERON_L	R5072	10K	1/20W	MF	201	
SMC_LID	R5071	100K	1/20W	MF	201	
SMC_TX_L	R5073	10K	1/20W	MF	201	
SMC_RX_L	R5074	100K	1/20W	MF	201	
SMC_DEBUGPRT_TX_L	R5075	10K	1/20W	MF	201	
SMC_DEBUGPRT_RX_L	R5076	100K	1/20W	MF	201	
SMC_TMS	R5077	10K	1/20W	MF	201	
SMC_TDO	R5078	10K	1/20W	MF	201	
SMC_TDI	R5079	10K	1/20W	MF	201	
SMC_TCK	R5080	10K	1/20W	MF	201	
SMC_BIL_BUTTON_L	R5081	10K	1/20W	MF	201	
SMC_BC_ACOK	R5087	470K	1/20W	MF	201	
SMC_S5_PWRGD_VIN	R5092	100K	1/20W	MF	201	
SMS_INT_L	R5093	10K	1/20W	MF	201	
CPU_THRMTRIP_3V3	R5094	100K	1/20W	MF	201	
SPI_DESCRIPTOR_OVERRIDE_L NOSTUFF	R5095	10K	1/20W	MF	201	

SMC_ROMBOOT
R5088 1K 5% 1/20W MF 201
SMC_THRMTRIP — R5086 10K 1/20W MF 201

SMC_DELAYED_PWRGD	R5091	100K	1/20W	MF	201	
SMC_PM_G2_EN	R5098	100K	1/20W	MF	201	
SMC_ADAPTER_EN	R5085	10K	1/20W	MF	201	
SMC_S4_WAKESRC_EN	R5090	100K	1/20W	MF	201	

WIFI_EVENT_L — R5089 10K 1/20W MF 201 — PP3V3_WLAN

SYNC_MASTER=D2_KEPLER
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PAGE TITLE: SMC Support

Apple Inc.

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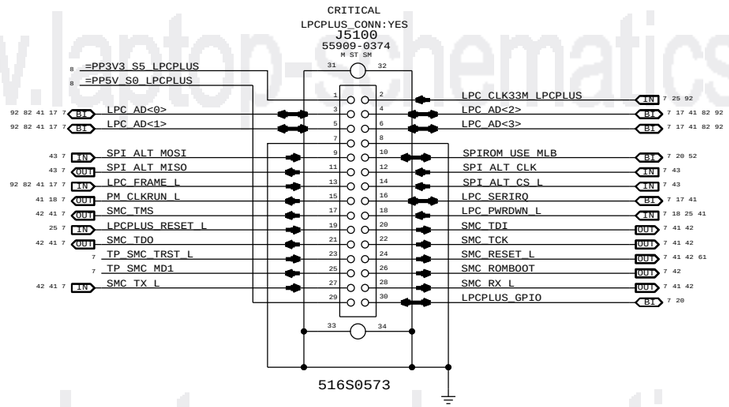
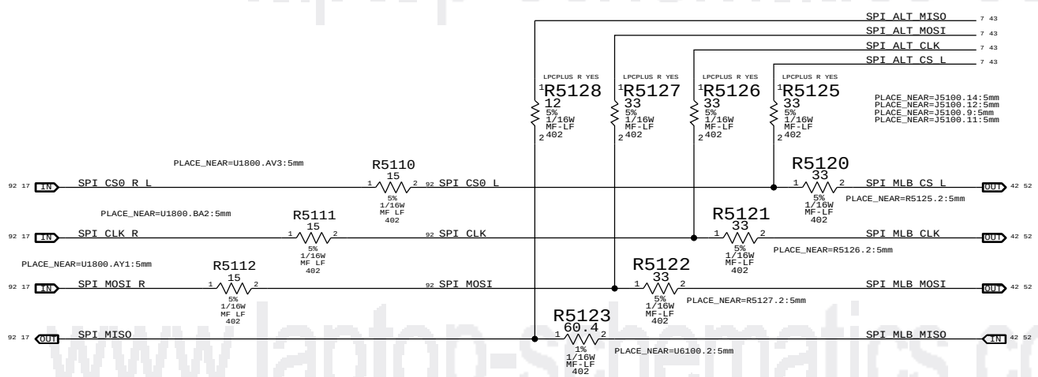
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

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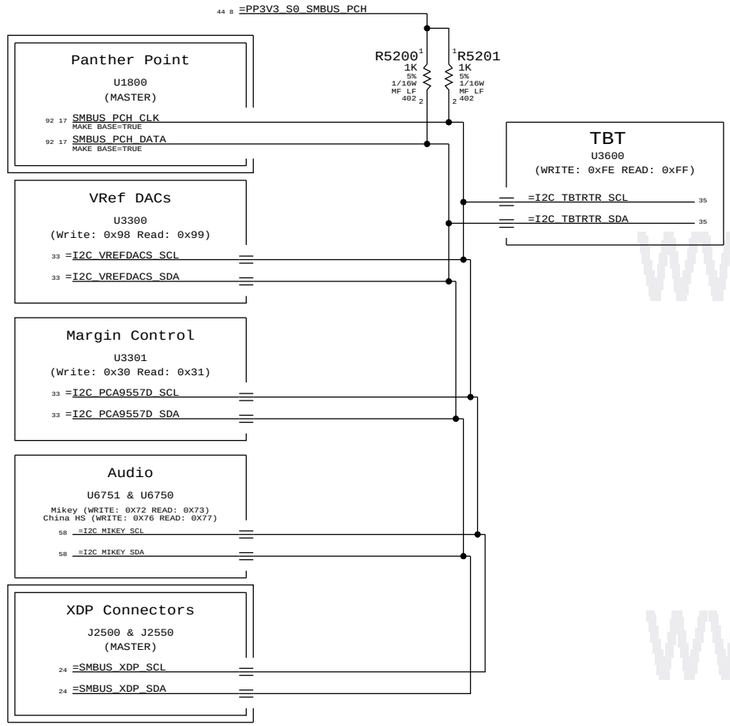
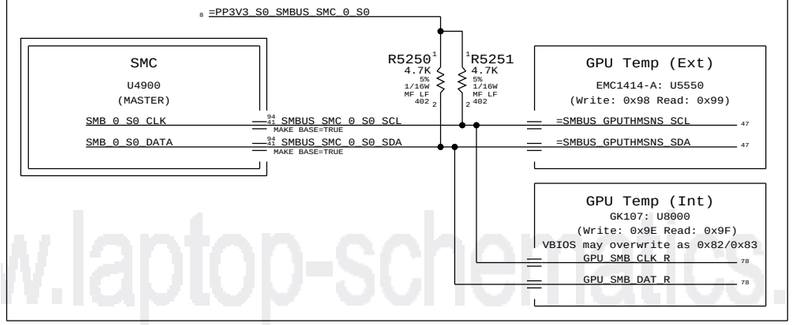
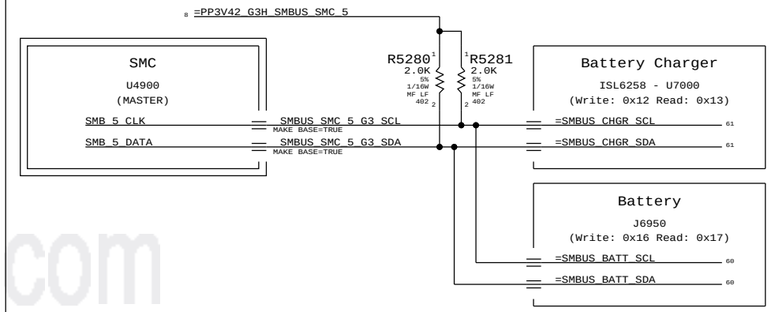
PCH SMBus "0" Connections



SMC "0" SMBus Connections

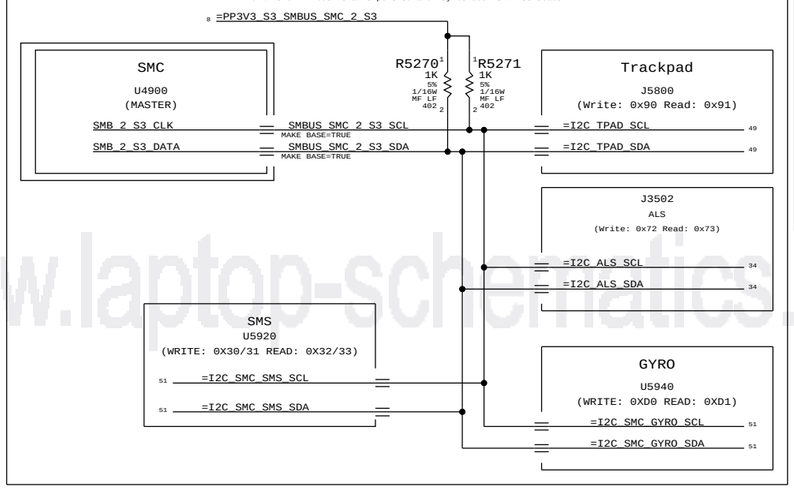


SMC "5" SMBUS CONNECTIONS

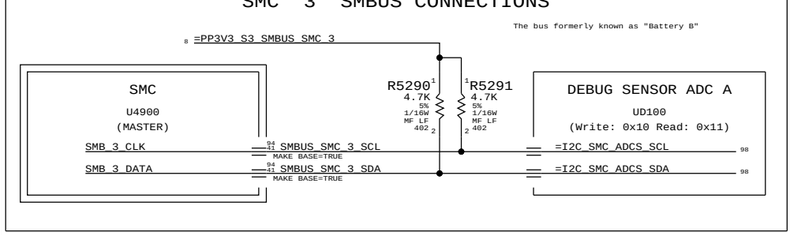


SMC "2" SMBUS CONNECTIONS

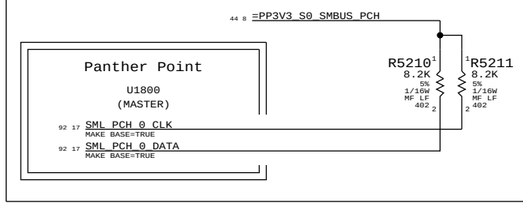
NOTE SMC RMT bus remains powered and may be active in S3 state



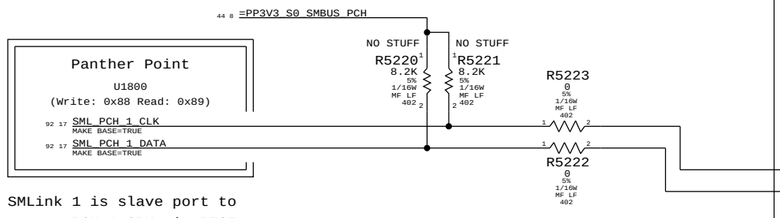
SMC "3" SMBUS CONNECTIONS



PCH "SMLink 0" Connections

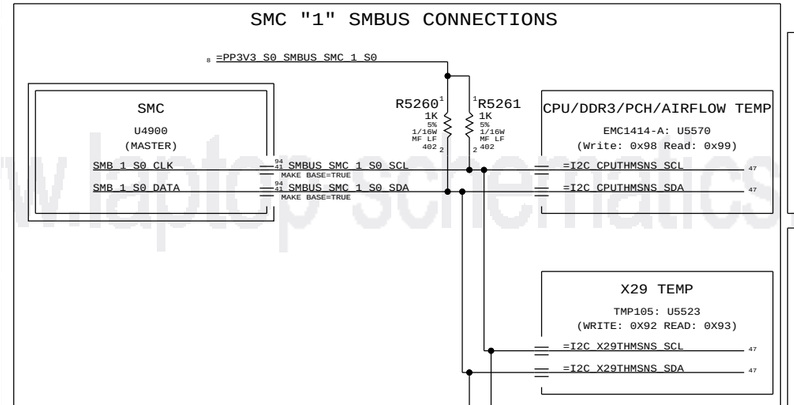


PCH "SMLink 1" Connections

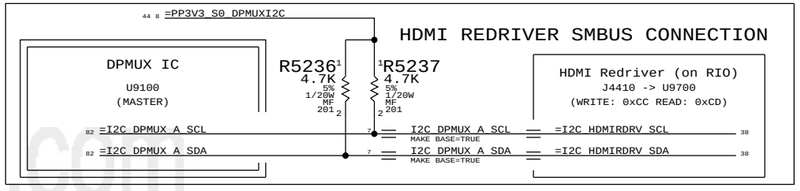


SMLink 1 is slave port to access PCH & CPU via PECI.

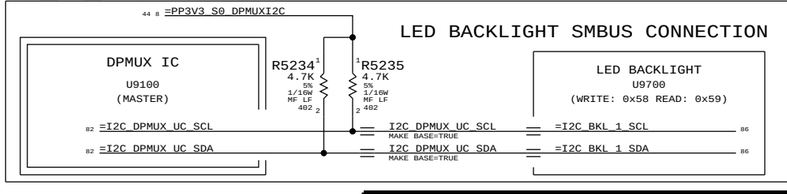
SMC "1" SMBUS CONNECTIONS



HDMI REDRIVER SMBUS CONNECTION



LED BACKLIGHT SMBUS CONNECTION



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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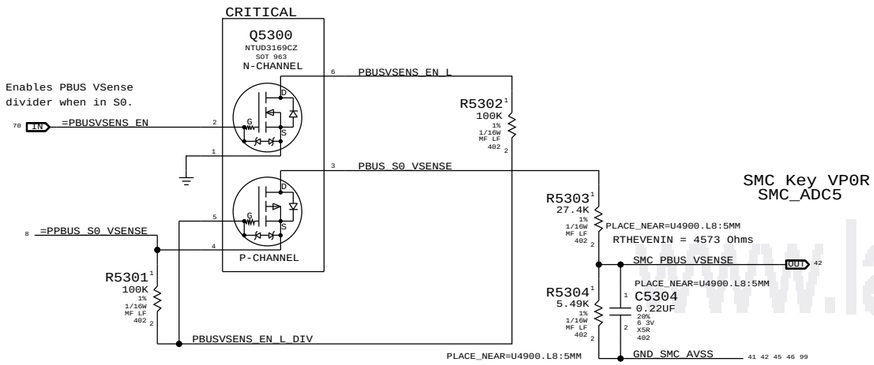
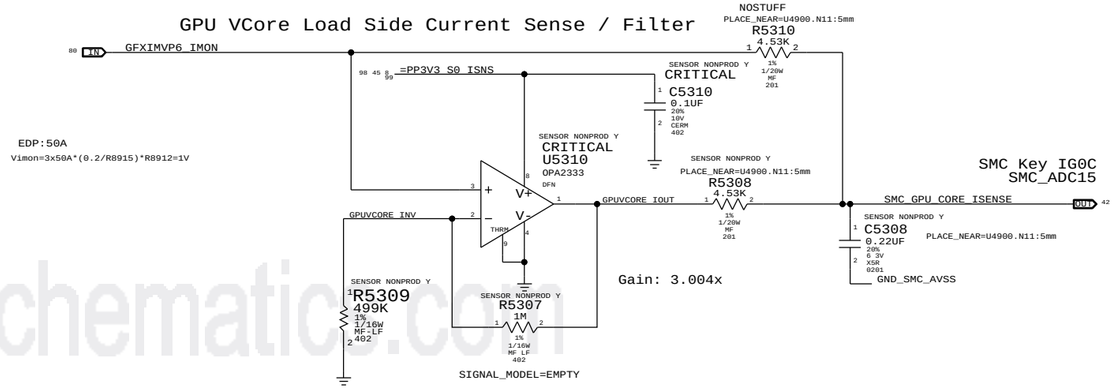
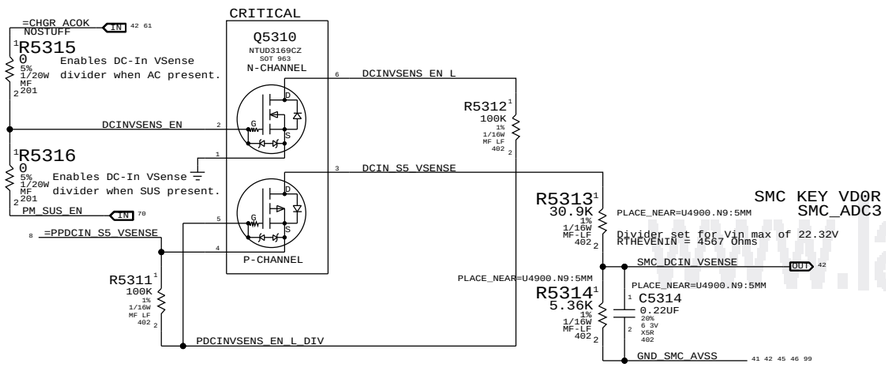
PBUS Voltage Sense Enable & Filter



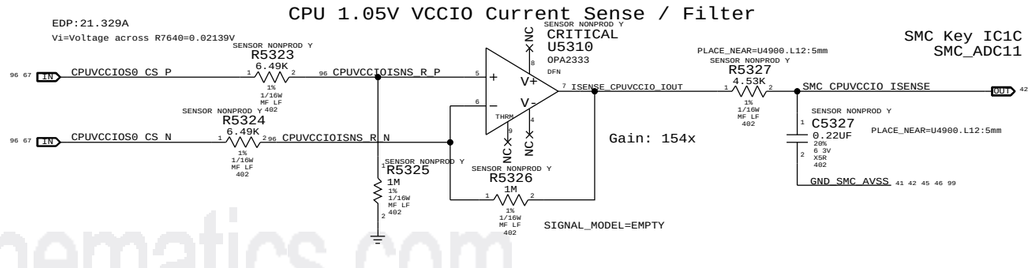
GPU VCore Load Side Current Sense / Filter



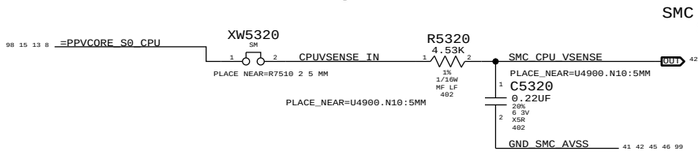
DC-In Voltage Sense Enable & Filter



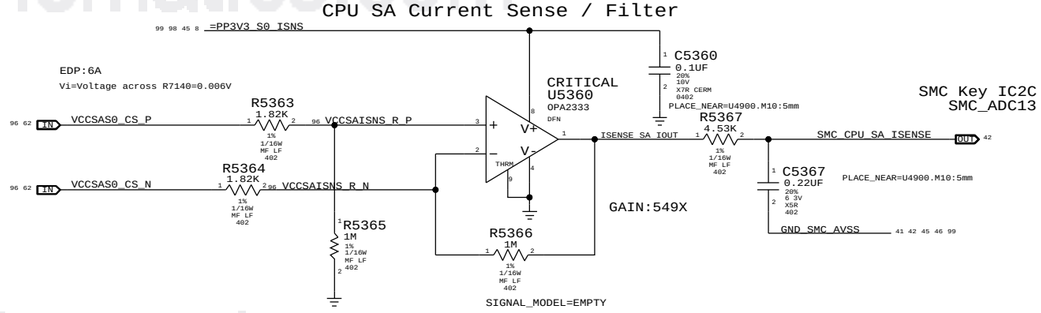
CPU 1.05V VCCIO Current Sense / Filter



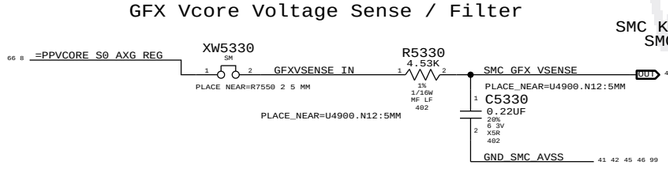
CPU Vcore Voltage Sense / Filter



CPU SA Current Sense / Filter

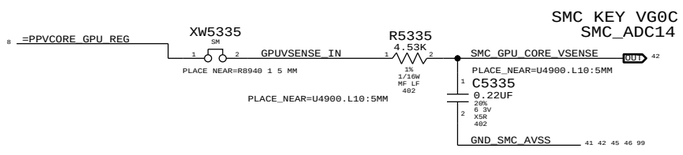


GFX Vcore Voltage Sense / Filter

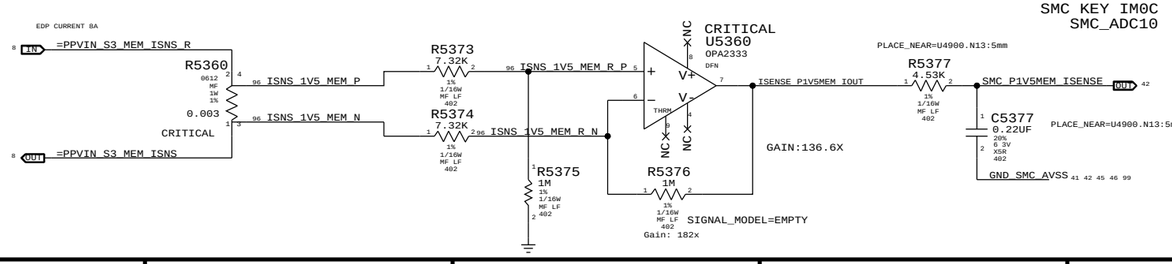


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	1	RES MTL FILM 100K 5 1/16W 0402 SMD LF	C5327		SENSOR NONPROD N
1175O008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5308		SENSOR NONPROD N

GPU Vcore Voltage Sense / Filter



DDR3 1.5V DRAM ONLY CURRENT SENSE / FILTER



SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012

PAGE TITLE
Voltage & Load Side Current Sensing

Apple Inc.

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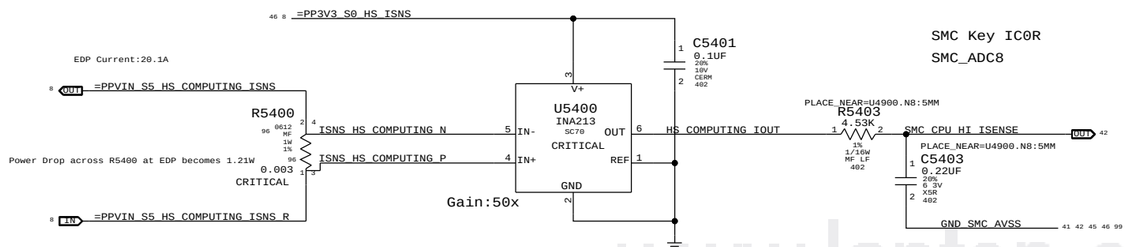
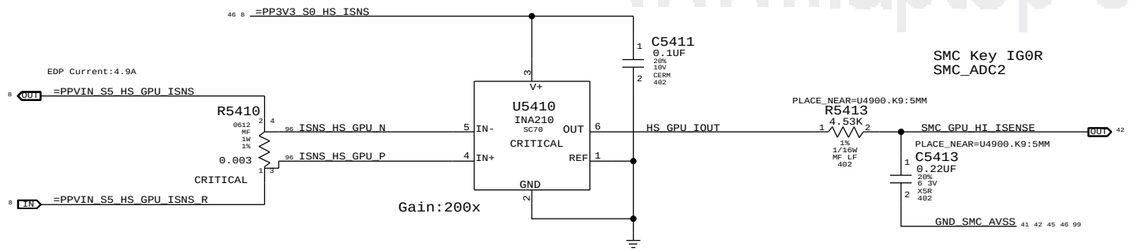
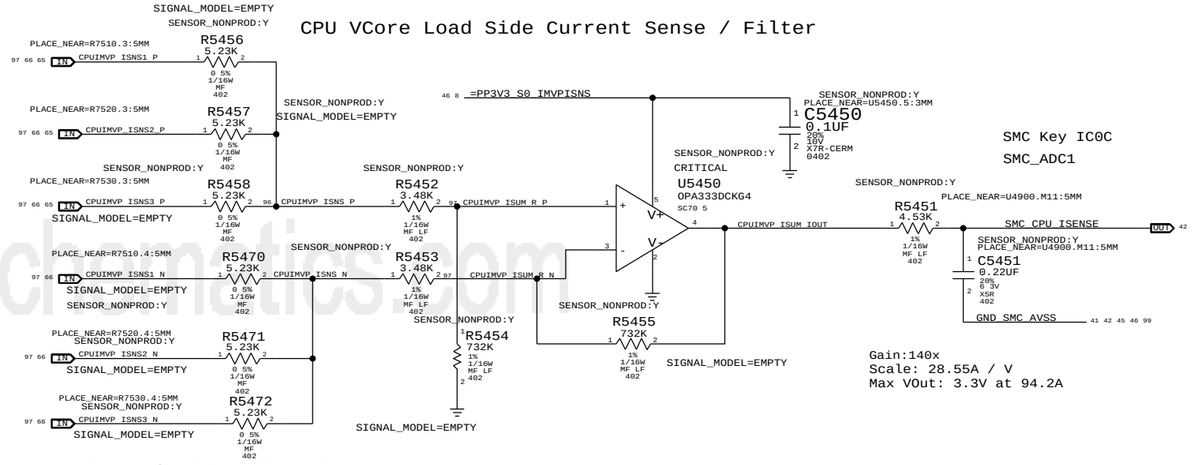
COMPUTING High Side Current Sense / Filter



GRAPHICS High Side Current Sense / Filter



CPU VCore Load Side Current Sense / Filter

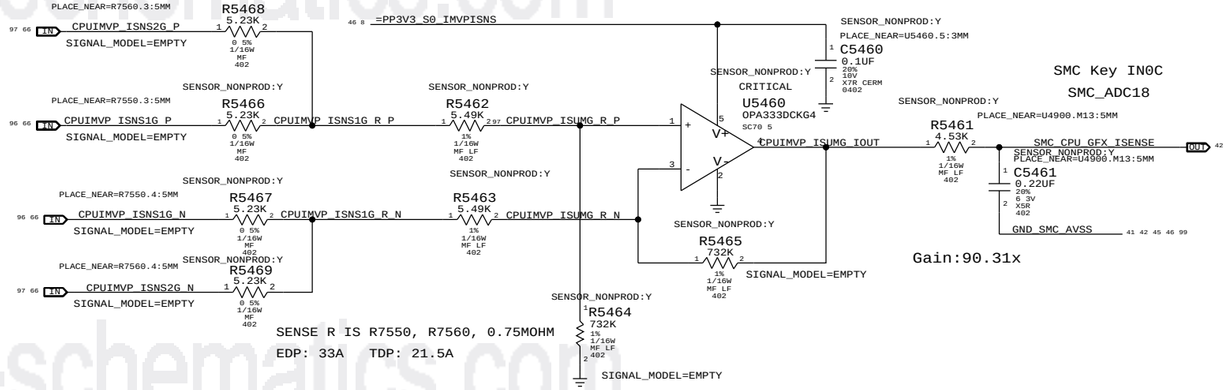


Sense R is R7510, R7520 & R7530
Individual Sense R is 0.75mOhm
EDP: 94A TDP :45A

(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

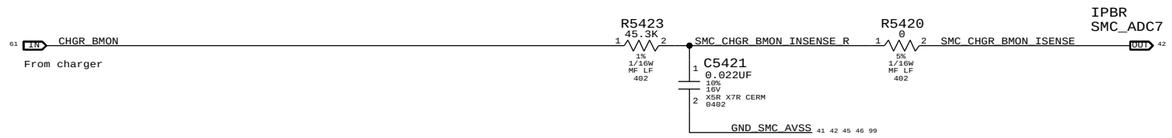
OTHER High Side Current Sense / Filter

GFX/IG VCore Load Side Current Sense / Filter

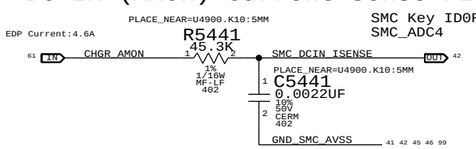


SENSE R IS R7550, R7560, 0.75MOHM
EDP: 33A TDP: 21.5A

CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	2	RES MTL FILM 100K 5 1/16W 0402 SMD LF	C5451 C5461		SENSOR NONPROD N

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE
High Side and CPU/AXG Current Sensing

Apple Inc.

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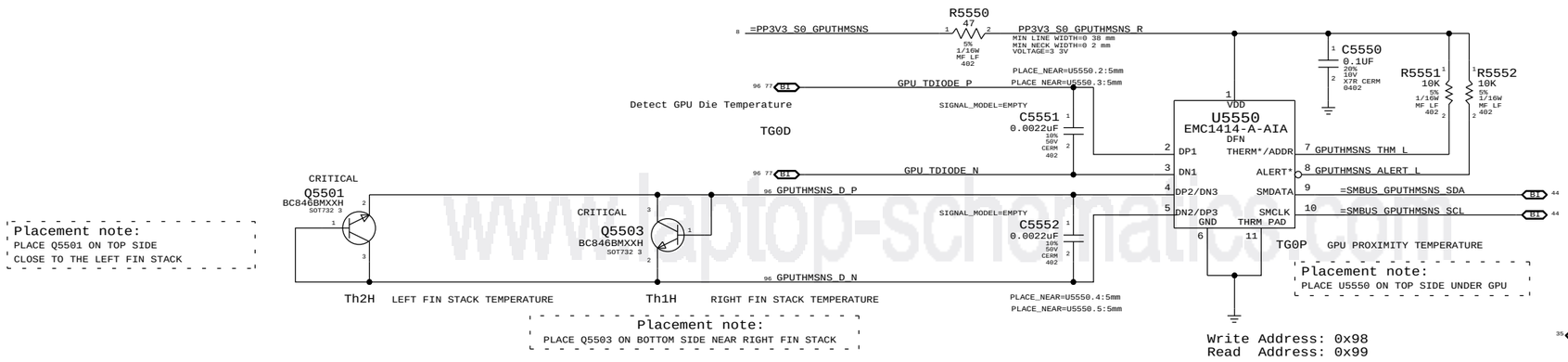
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK

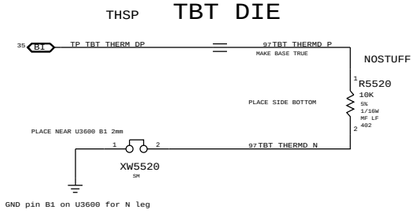


Placement note:
PLACE Q5501 ON TOP SIDE
CLOSE TO THE LEFT FIN STACK

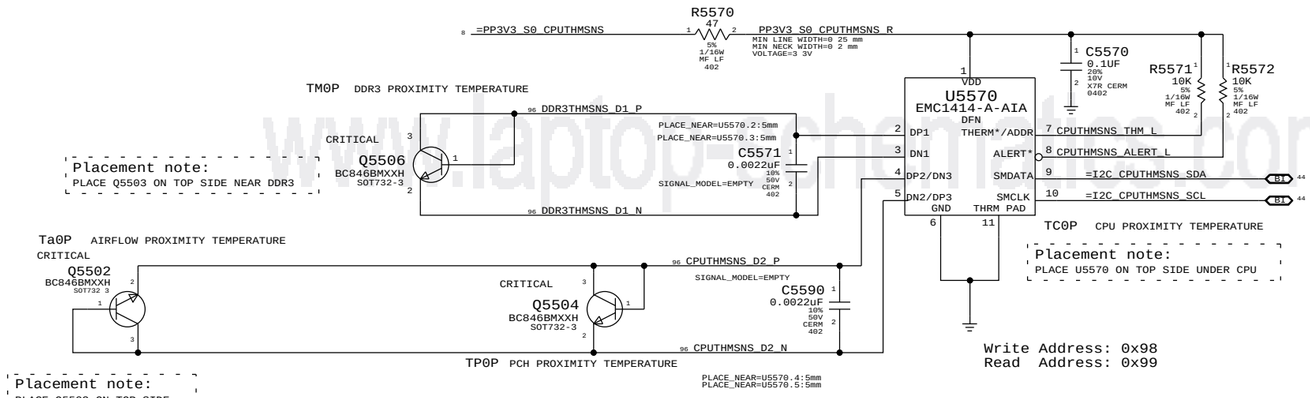
Placement note:
PLACE Q5503 ON BOTTOM SIDE NEAR RIGHT FIN STACK

Placement note:
PLACE U5550 ON TOP SIDE UNDER GPU

TBT DIE



DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



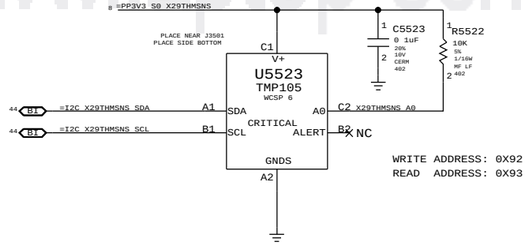
Placement note:
PLACE Q5503 ON TOP SIDE NEAR DDR3

Placement note:
PLACE Q5502 ON TOP SIDE
CLOSE TO BOARD EDGE

Placement note:
PLACE Q5504 ON TOP SIDE UNDER PCH

Placement note:
PLACE U5570 ON TOP SIDE UNDER CPU

X29 PROXIMITY



Placement note:
PLACE U5523 ON BOTTOM NEAR X29 CONN

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

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REVISION: 4.18.0

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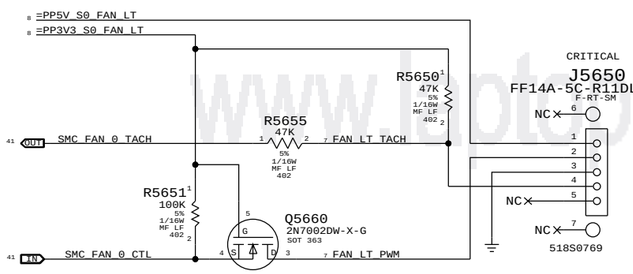
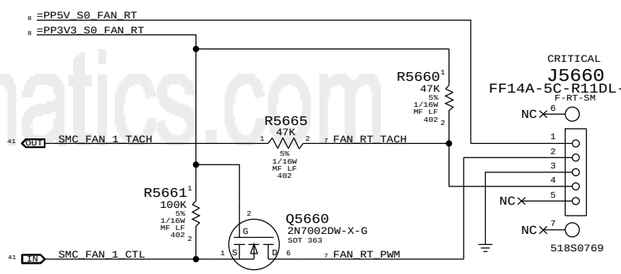
Left Fan



Right Fan



SYNC MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

PAGE TITLE

Fan Connectors

Apple Inc.

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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector

Keyboard Connector

SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

All RC values are TBD

5V TRACKPAD S4 FET

Caps Lock LED Drive

TPAD Buttons Disable

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

BOM Options available to CSA 5

TPAD_5V:SW_S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

BOM GROUP	BOM OPTIONS
TPAD_5V:SW_S4	TPAD_5V_SW_S4
TPAD_5V:LDO_S4	TPAD_5V_FET,TPAD_5V_LDO
TPAD_5V:LDO_S5	TPAD_5V_NO_FET,TPAD_5V_LDO

WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012
PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

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8 =PP3V3_S0_TPAD

R5853 470K 5% 1/10W MF-LF 402

50 43 OUT SMC_SYS_KBDLED

R5854 4.7K 5% 1/10W MF-LF 402

7 SMC_KBDLED_PRESENT_L

J5815 PIN 4 IS GROUNDED
ON KEYBOARD BACKLIGHT FLEX
CRITICAL

J5815
AA07A-S010-VA1
F-ST-SM

12 11 2 1 4 3 6 5 8 7 10 9 13 14

KBDLED_ANODE2 7 50

XNC

KBDLED_ANODE1 7 50

516S0899

Keyboard Backlight Connector

Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will
tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only
grounded when KB BL flex connected.

50 41 IN SMC_SYS_KBDLED

NOSTUFF R5857 10K 5% 1/10W MF-LF 402

SMC_SYS_KBDLED_FILTER

NOSTUFF C5859 10UF 20% 10V X5R 0603

NOSTUFF R5858 120K 5% 1/10W MF-LF 402

NOSTUFF R5859 100K 5% 1/10W MF-LF 402

R5856 0 5% 1/16W MF-LF 402

SMC_SYS_KBDLED_R

8 =PPSV_S0_KBDLED

CRITICAL L5850 15UH-20%-740MA-0.420HM VLF403212MT-SM
MIN LINE WIDTH=0 3 MM
MIN NECK WIDTH=0 25 MM
SWITCH NODE=TRUE

KBDLED_SW1

C5850 1UF 10% 10V X5R 402-1

353S3472 ORDER TABLE

U5850 LT3591 DFN
CTRL VIN SW SW GND PAD LED CAP CAP

KBDLED_ANODE1
MIN LINE WIDTH=0 25 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=35V

R5855 10 1% 1/16W MF-LF 402

KBDLED_CAP1
MIN LINE WIDTH=0 25 MM
MIN NECK WIDTH=0 2 MM

KBD_BL:SANDWICH	KBD_BL:SANDWICH	KBD_BL:TBONE	KBD_BL:TBONE
CRITICAL	CRITICAL	CRITICAL	CRITICAL
C5855 1.0UF 10% 50V X5R 0603	C5856 1.0UF 10% 50V X5R 0603	C5857 1.0UF 10% 50V X7R 0805	C5858 1.0UF 10% 50V X7R 0805

R5866 0 5% 1/16W MF-LF 402 NOSTUFF

SMC_SYS_KBDLED_ANALOG

CRITICAL L5860 15UH-20%-740MA-0.420HM VLF403212MT-SM
MIN LINE WIDTH=0 3 MM
MIN NECK WIDTH=0 25 MM
SWITCH NODE=TRUE

KBDLED_SW2

C5860 1UF 10% 10V X5R 402-1

353S3472 ORDER TABLE

U5860 LT3591 DFN
CTRL VIN SW SW GND PAD LED CAP CAP

50 7 KBDLED_ANODE2
MIN LINE WIDTH=0 25 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=35V

R5865 10 1% 1/16W MF-LF 402

KBDLED_CAP2
MIN LINE WIDTH=0 25 MM
MIN NECK WIDTH=0 2 MM

KBD_BL:SANDWICH	KBD_BL:SANDWICH	KBD_BL:TBONE	KBD_BL:TBONE
CRITICAL	CRITICAL	CRITICAL	CRITICAL
C5865 1.0UF 10% 50V X5R 0603	C5866 1.0UF 10% 50V X5R 0603	C5867 1.0UF 10% 50V X7R 0805	C5868 1.0UF 10% 50V X7R 0805

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1612	2	IC DC/DC CYTR BOOST WHITE LED 1MHZ DFN8	U5850 U5860	CRITICAL	

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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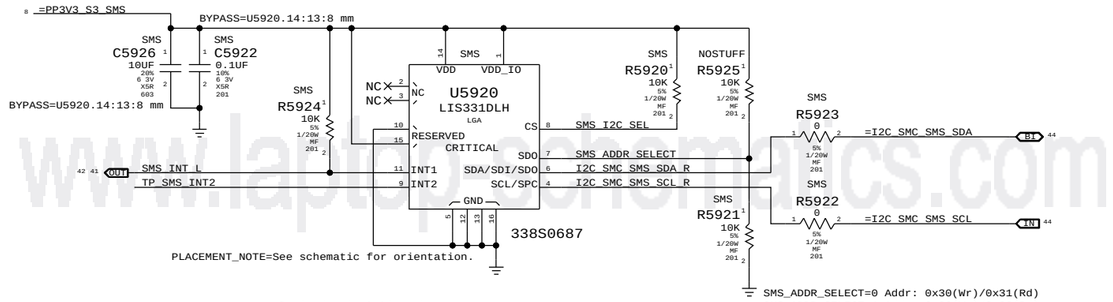

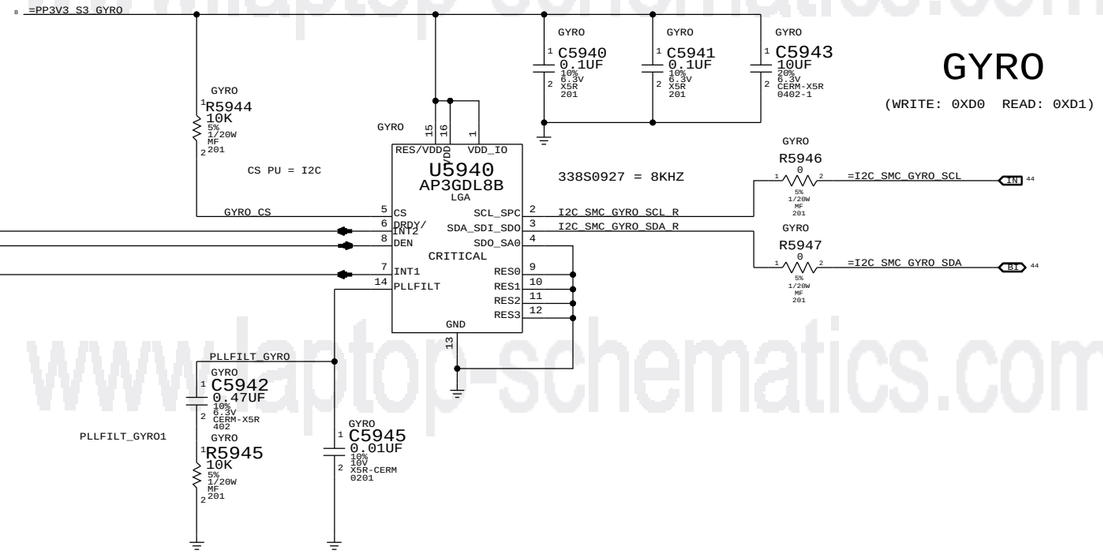

GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: DIGITAL ACCELEROMETER & GYRO

Apple Inc.

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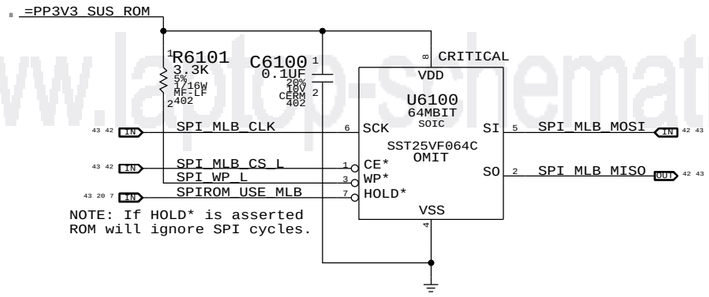

SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

SPI ROM

Apple Inc.

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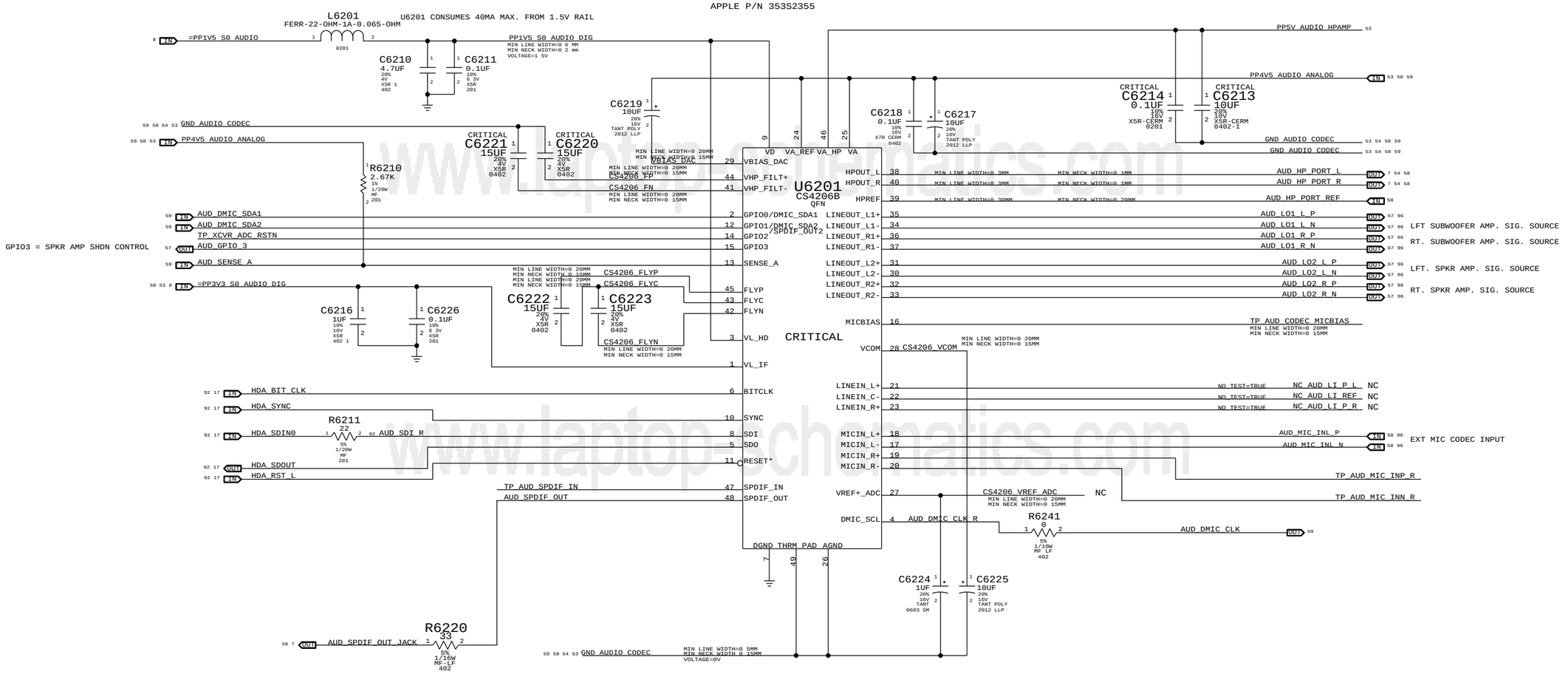
AUDIO CODEC

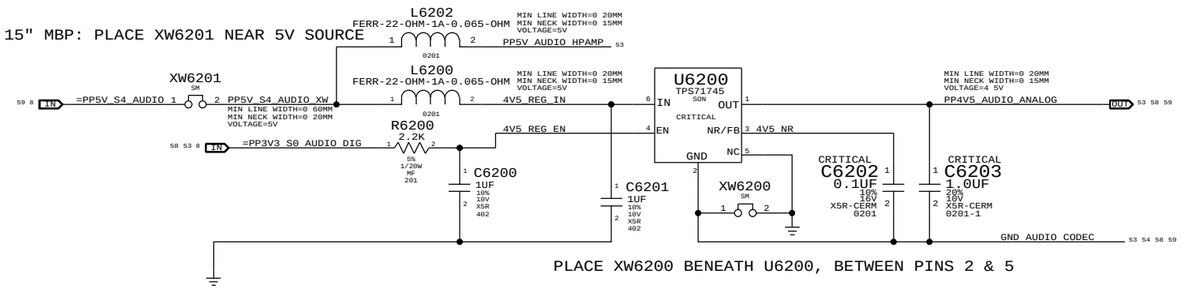
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

15" MBP: PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=D2 CARA
SYNC DATE=03/16/2012
PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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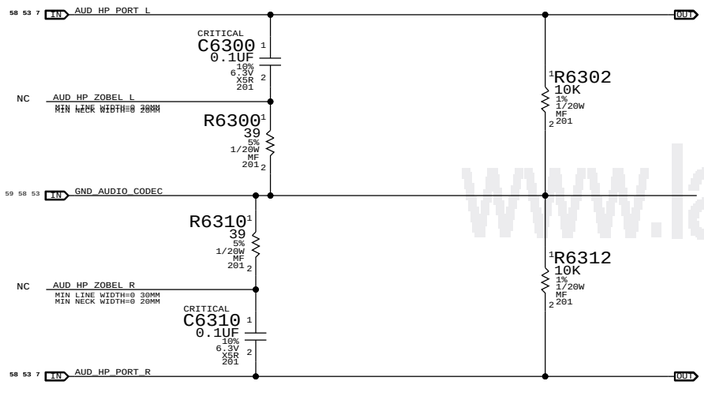
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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SYNC MASTER=D2 CARA SYNC DATE=03/16/2012

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AUDIO: IV SENSE

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SYNC_MASTER=D2_CARA SYNC_DATE=03/16/2012

PAGE TITLE

AUDIO: IV SENSE FILTER

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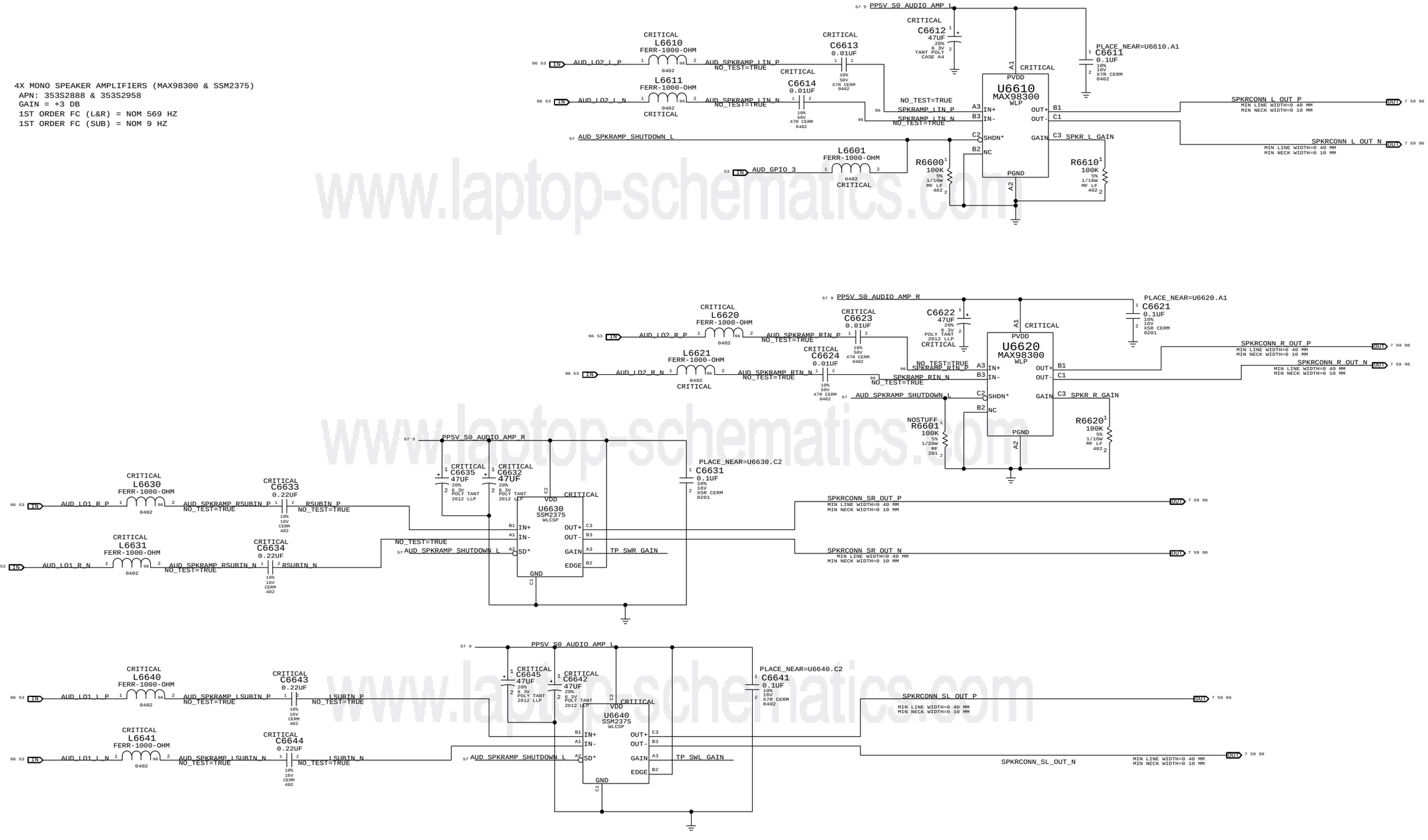
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



SYNC MASTER=D2_CARA
SYNC DATE=03/16/2012

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

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AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE

PP4V5_AUDIO_ANALOG
=PP3V3_S0_AUDIO_DIG
R6762 10K 5% 1/20W MF 201
C6795 1.0UF 20% 10V X5R-CERM 0201-1
C6794 1.0UF 20% 10V X5R-CERM 0201-1
C6755 1.0UF 20% 10V X5R-CERM 0201-1
R6757 33 5% 1/20W MF 201
R6758 33 5% 1/20W MF 201
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

U6751
CD3282A1
WCSP
AVDD
SCL C3
SDA B3
INT* D3
ENABLE A3
HDET A1
CS B2
MICBIAS C1
DETECT B1
BYPASS D1
DGND C2
AGND D2

AUDIO_SCL
AUDIO_SDA
AUD_I2C_INT_L
AUD_IPHS_SWITCH_EN
HS_HDET
NOSTUFF R6761 47K 5% 1/20W MF 201
AUD_PORTA_DET_L
R6755 100K 5% 1/20W MF 201
C6756 0.01UF 10% 16V X5R-CERM 0201
GND_AUDIO_CODEC
NO_TEST=TRUE
HS_MIC_BIAS
HS_SW_DET
HS_RX_BP
MIKEY R6754 1K 5% 1/20W MF 201

L6754
FERR-22-OHM-1A-0.065-OHM 0201
=PP3V42_G3H_AUDIO
MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=3.42V
PP3V42_G3H_AUDIO_LC
C6793 1.0UF 20% 10V X5R CERM 0201
C6792 1.0UF 20% 10V X5R CERM 0201
C6790 1.0UF 20% 10V X5R CERM 0201
C6754 0.1UF 10% 16V X5R CERM 0201
PLACE_NEAR=U6750.A1
GND_AUDIO_CODEC

U6750
TS3A8235YFP
WCSP
CRITICAL
VDD A1
RAMPI D4
RAMPO D3
CLAMPI C4
CLAMPO B4
MIC D2
REF D1
SCL A3
SDA A4
ADDR A2
GND1 C2
GND2 B2
GND B3
C3
CHS_CLAMPI
CHS_CLAMPO
HS_MIC_HI
HS_MIC_LO
MIC1 B1
MIC2 C1

R6751 1K 5% 1/20W MF 201
R6752 2.2K 1% 1/20W MF 201
R6753 2.2K 1% 1/20W MF 201
C6751 10UF 20% 6.3V X5R-CERM 0402-1
C6791 10UF 20% 6.3V X5R-CERM 0402-1
XW6751 SM
PLACE_NEAR=U6750.D1
US_HS_GND
CH_HS_GND

MIKEY CRITICAL C6752 0.1UF 10% 6.3V X5R 201
MIKEY CRITICAL C6753 0.1UF 10% 6.3V X5R 201
AUD_MIC_INL_P
AUD_MIC_INL_N
MIKEY R6756 100K 5% 1/20W MF 201
MIKEY CRITICAL C6750 6800PF 10% 10V X5R-X7R-CERM 0201
MIKEY R6750 2.2K 5% 1/20W MF 201
MIKEY R6759 0 5% 1/20W MF 201
HS_MIC_HI_RC
HS_MIC_LO_RC
MIKEY CRITICAL C6758 27PF 5% 25V NP0-C0G 0201
R/C6750_FILTER_TO_ADDRESS_OUT-OF-BAND NOISE_ISSUE_SEEN_ON_EARLY_HEADSETS (SEE_RADAR_#_6210118)

R6760 47K 5% 1/20W MF 201
NOSTUFF
GND_AUDIO_CODEC

CRITICAL L6701 FERR-33-OHM-0.8A-0.09-OHM 0201
US_HS_MIC
AUD_CONN_MIC

CRITICAL L6700 120-OHM-25%-1.3A 0402
US_HS_GND
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.6MM
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM

CRITICAL L6702 120-OHM-25%-1.3A 0402
CH_HS_GND
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.6MM
AUD_CONN_MIC_XW
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM

CRITICAL L6703 FERR-33-OHM-0.8A-0.09-OHM 0201
CH_HS_MIC
AUD_CONN_SLEEVE

CRITICAL L6704 120-OHM-25%-1.3A 0402
AUD_HP_PORT_L
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM

APN:510S0009
CRITICAL J6701 51138-0274 F-ST-SM
AUD_CONN_TIPDET_INV
=PP3V3_S0_AUDIO_DIG
AUD_SPDIF_OUT_JACK

CRITICAL L6705 120-OHM-25%-1.3A 0402
AUD_HP_PORT_R
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM

CRITICAL L6706 FERR-470-OHM 0201
AUD_TYPEDET
AUD_CONN_TYPEDET

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC MASTER=D2 CARA
SYNC DATE=03/16/2012
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (D,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

3-MIC CONNECTOR

SPEAKER CONNECTOR HP=80HZ

APN: 518S0627

PORT B DETECT(SPDIF DELEGATE) PORT A DETECT (HEADPHONES)

PORT C DETECT(SPEAKER MISMATCH)

EXTRACTION NOTIFICATION

APN:376S0613

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP

SYNC MASTER=D2_CARA SYNC_DATE=03/16/2012

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MagSafe DC Power Jack

CRITICAL
J6900
WTB-PWR-M82
M-RT-SM
518S0508

CRITICAL
F6905
6AMP-32V-0.0095OHM
0603

=PP18V5_DCIN_CONN

PP18V5_DCIN_FUSE
MIN LINE WIDTH=1MM
MIN NECK WIDTH=0 20MM
VOLTAGE=18 5V

C6905 0.01UF 20% 50V CERM 0603

TDM_ONEWIRE_MPM

=PP3V42_G3H_ONEWIREPROT

C6908 0.1UF 20% 10V CERM 402
PLACEMENT NOTE PLACE NEAR U6900 and U6901

CRITICAL
U6901
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC
SMC_BC_ACOK

C6900 0.1UF 20% 10V CERM 402

R6929 2.0K 5% 1/16W MF-LF 402

U6900
MAX9940
SC70 5
CRITICAL
VCC
EXT
INT
NC GND
NC

ADAPTER_SENSE
SYS_ONEWIRE

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER SENSE when AC is connected

=PP3V42_G3H_TDM

TDM:MPM R6977 22 5% 1/20W MF 201

TDM:MLB R6975 2.21K 1% 1/20W MF 201

TDM:MLB R6976 22 5% 1/20W MF 201

SYS_TDM_ONEWIRE
TDM_ONEWIRE_MLB

R6912 22.1K 1% 1/20W MF 201

Input impedance of 22.1K meets sparkitecture requirements for 15" MBP design only

TDM:MLB
U6970
SLG4AP030
TDFN
IN_A
IN_B1
IN_B2
OUT_C
OUT_D1
OUT_D2
VDD
CRITICAL
GND PAD
THRM

TDM_RX_D
TDM_RX
TDM_PD_BASE_R

TDM:MLB CRITICAL D6970 DDZ9694T SOD523

TDM:MLB R6973 24.9K 1% 1/20W MF 201

TDM:MLB R6974 6.34K 1% 1/20W MF 201

LAYOUT NOTE:
Q0220 NEEDS 10 SQ CM
OF 1 OZ CU FOR THERMAL

TDM_PD_BASE

TDM:MLB CRITICAL Q6970 ZXTN619MA DFN

TDM:MLB CRITICAL Q6971 MMBT2222AM3T5G SOT723

TDM:MLB R6972 54.9 1% 1/20W MF 201

TDM_PD_DS

TDM:MLB R6971 12.1 1% 1/8W MF-LF 805

TDM:MLB R6970 12.1 1% 1/8W MF-LF 805

Q6910
SI5419DU
POWERPAK

R6910 100K 5% 1/20W MF 201

C6912 0.047UF 10% 25V X5R 0402

R6911 10K 5% 1/20W MF 201

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE_R
DCIN_ISOL_GATE
=PP18V5_DCIN_ISOL

D6910
GDZT2R6.8
GDZ-0201
6.8V Zener

R6920 47 1% 1/3W MF 805

PP18V5_DCIN_CONN_R
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=18 5V

CRITICAL
D6905
BAT30CWFILM
SOT 323

R6905 10 5% 1/8W MF LF 805

=PPBUS_G3H
PPBUS_G3H_R
MIN LINE WIDTH=0 6 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=18 5V

PPVIN_G3H_P3V42G3H
MIN LINE WIDTH=0 4 mm
MIN NECK WIDTH=0 2 mm
VOLTAGE=18 5V

BATTERY CONNECTOR

518-0376
CRITICAL
J6950
BAT-J5
F-ST-TH

POS 1
POS 2
POS 3
POS 4
SCL 5
SDA 6
SYS_DETECT 7
NEG 8
NEG 9
NEG 10
NEG 11

NC
NC

PPVBAT_G3H_CONN
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA
SYS_DETECT_L

C6950 0.1UF 10% 25V X5R 402

C6960 1UF 10% 25V X5R 603-1

CRITICAL
D6950
RCLAMP2402B
SC 75

R6950 10K 5% 1/16W MF-LF 402

C6990 4.7UF 10% 6.3V X5R-CERM 0603

C6991 4.7UF 10% 6.3V X5R-CERM 0603

NOSTUFF
C6992 4.7UF 10% 6.3V X5R-CERM 0603

C6993 4.7UF 10% 6.3V X5R-CERM 0603

NOSTUFF
C6996 4.7UF 10% 6.3V X5R-CERM 0603

NOSTUFF
C6997 4.7UF 10% 6.3V X5R-CERM 0603

3.425V "G3Hot" Supply

Supply needs to guarantee 3 31V delivered to SMC VRef generator

U6990
LT3470AED
DFN
VIN
BOOST
SHDN*
NC
SW
BIAS
FB
GND PAD
THRM
CRITICAL

P3V42G3H_BOOST
DIDT=TRUE

C6994 0.22UF 10% 10V CERM 402

CRITICAL
L6995
33UH 20% 0 39A 0 435OHM
DP418C SM

P3V42G3H_SW
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

=PP3V42_G3H_REG

Vout = 3.425V
100MA MAX OUTPUT
(Switcher limit)

C6995 22PF 5% 50V NP0 C0G CERM 0201

<Ra>
R6995 348K 1% 1/20W MF 201

C6999 22UF 20% 6 3V X5R-CERM-1 603

<Rb>
R6996 200K 1% 1/20W MF 201

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

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DC-In & Battery Connectors

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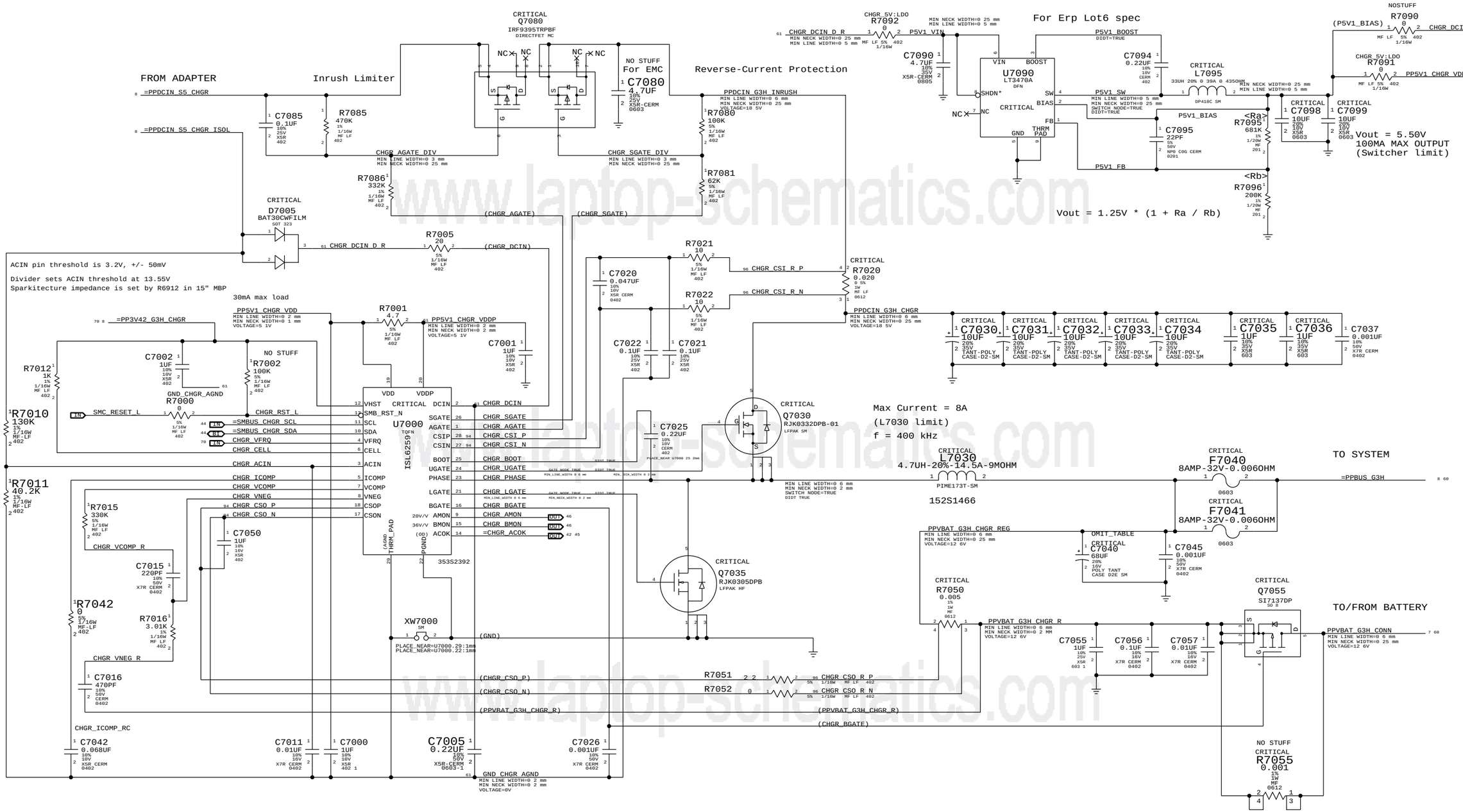

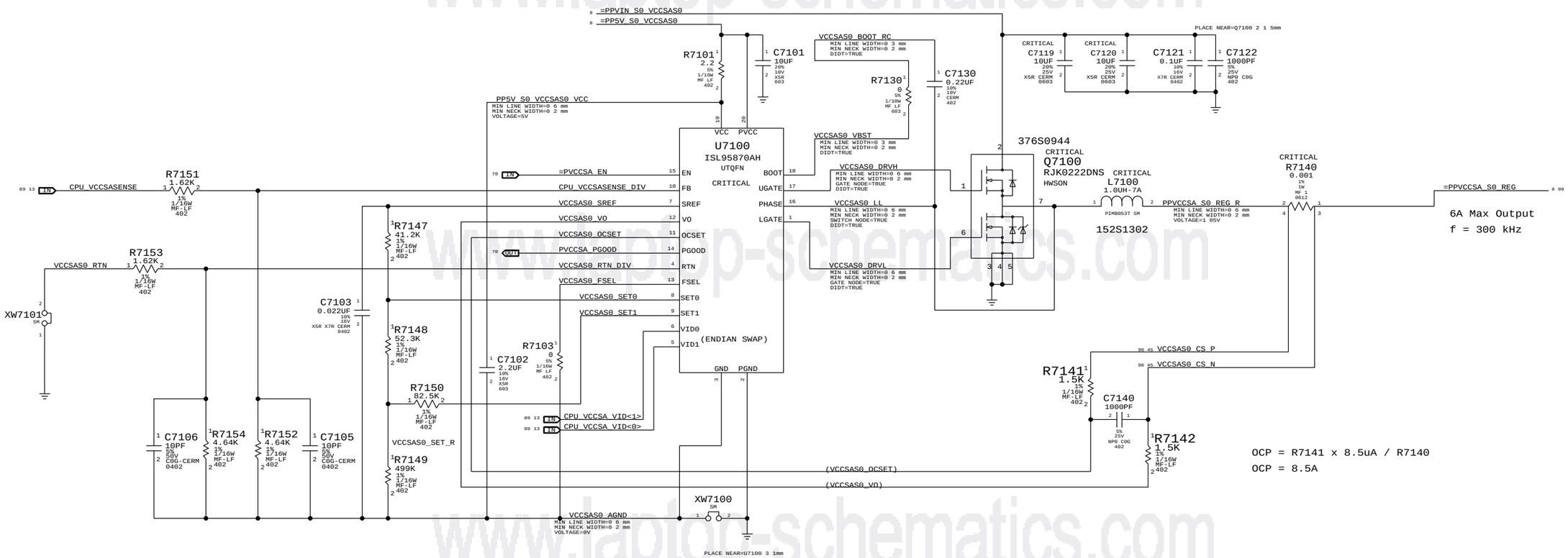

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

fb = (R7151+R7152)/R7152 = 1.349 and Vref = 0.5;

VID1=1, VIC0=1:
Vout<1,1> = Vref x fb;

VID1=0, VID0=1:
Vout<0,1> = Vref x (1+R7147 / (R7148 + R7149)) x fb

VID1=1, VID0=0
Vout<1,0> = Vref x (1+ (R7147 + R7148) / R7149)) x fb

VID1=0, VID0=0
Vout<0,0> = Vref x (1+ (R7147 / (R7148 + R7149 // R7150)) x fb

SYNC MASTER=D2_KEPLER SYNC DATE=01/13/2012

PAGE TITLE

System Agent Supply

Apple Inc.

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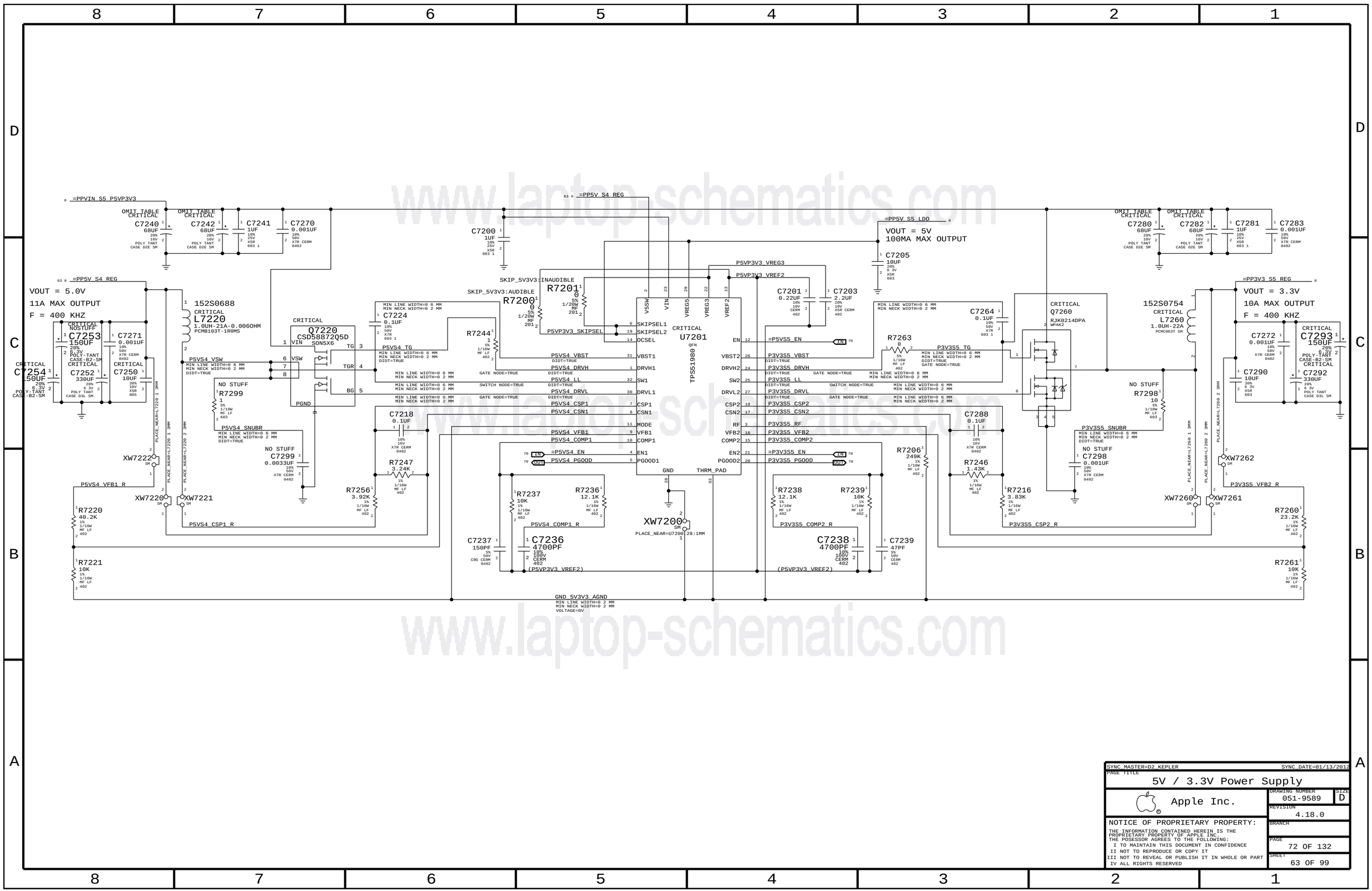
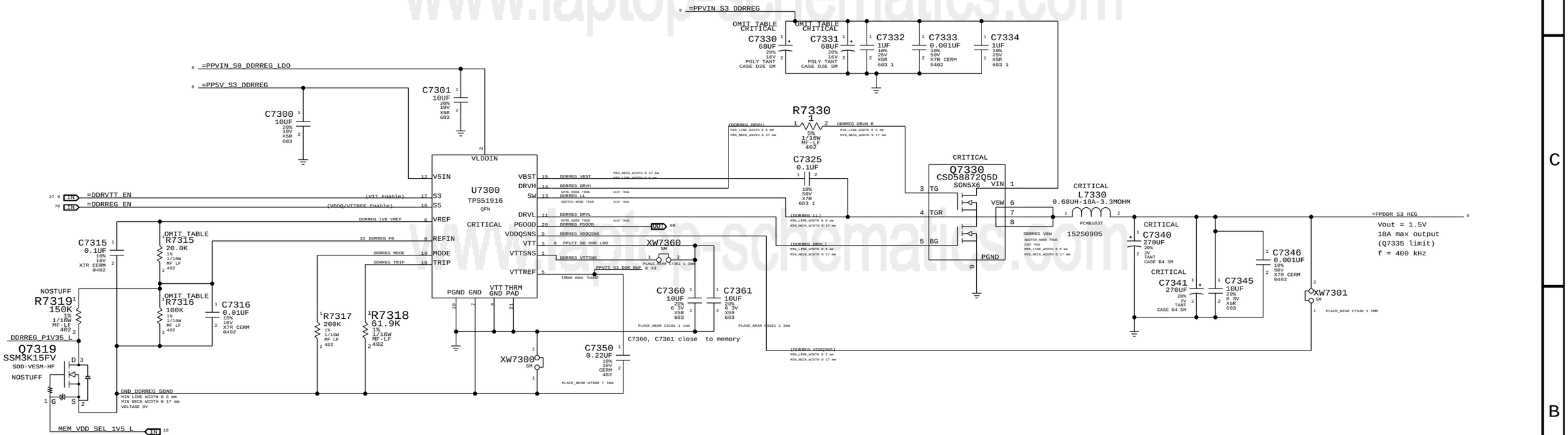


DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0343	1	RES MTL FILM 1/16W 20.0K 1 0402 SMD LF	R7315		PPDDR:1V5
114S0342	1	RES MTL FILM 1/16W 19.6K 1 0402 SMD LF	R7315		PPDDR:1V35
114S0411	1	RES MTL FILM 1/16W 100K 1 0402 SMD LF	R7316		PPDDR:1V5
114S0389	1	RES MTL FILM 1/16W 57.6K 1 0402 SMD LF	R7316		PPDDR:1V35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

1V5R1V35V DDR3 SUPPLY

Apple Inc.

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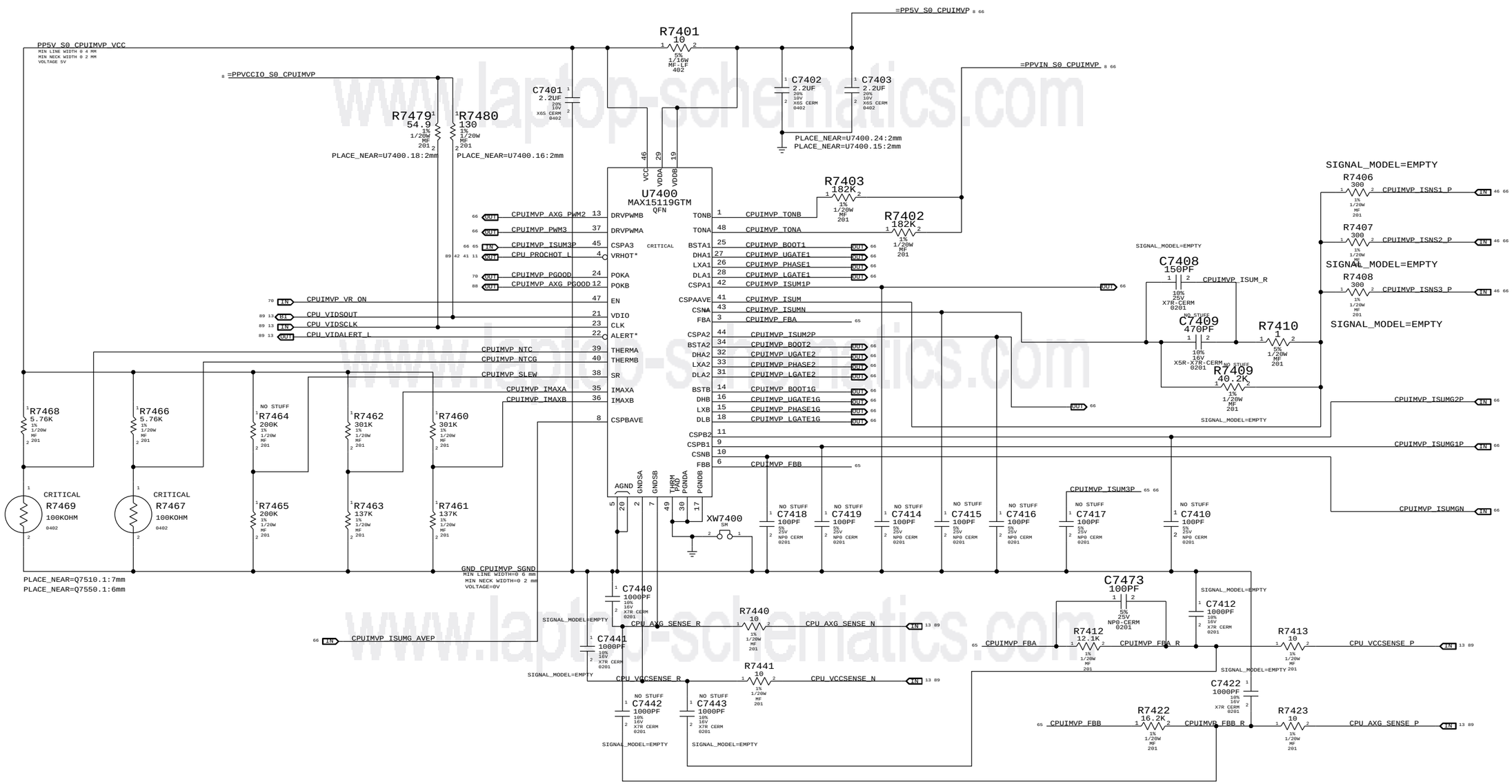

SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012

PAGE TITLE
CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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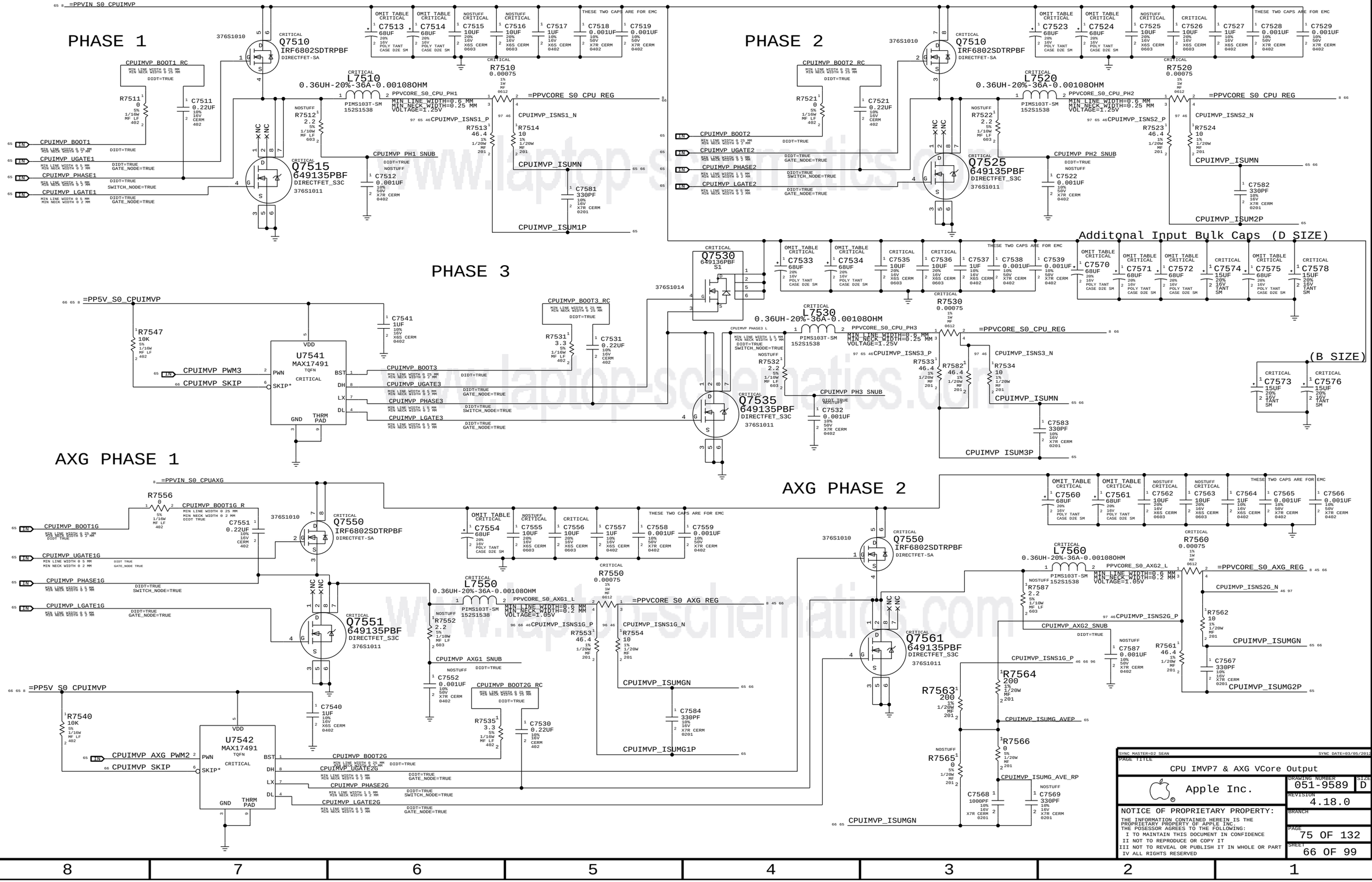
PHASE 1
=PPVIN_S0_CPUIMVP
376S1010
Q7510
IRF6802SDTRPBF
DIRECTFET-SA
CRITICAL
L7510
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
PPVCORE_S0_CPU_PH1
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
R7510
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P
CPUIMVP_ISUMN
CPUIMVP_ISUM1P
CPUIMVP_BOOT1_RC
R7511
C7511
0.22UF
CPUIMVP_BOOT1
CPUIMVP_UGATE1
CPUIMVP_PHASE1
CPUIMVP_LGATE1
R7512
2.2
CPUIMVP_PH1_SNUB
C7512
0.001UF
Q7515
649135PBF
DIRECTFET_S3C
376S1011
C7513
C7514
C7515
C7516
C7517
C7518
0.001UF
C7519
0.001UF
THESE TWO CAPS ARE FOR EMC
PHASE 2
376S1010
Q7510
IRF6802SDTRPBF
DIRECTFET-SA
L7520
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
PPVCORE_S0_CPU_PH2
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
R7520
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS2_N
CPUIMVP_ISNS2_P
CPUIMVP_ISUMN
CPUIMVP_ISUM2P
CPUIMVP_BOOT2_RC
R7521
C7521
0.22UF
CPUIMVP_BOOT2
CPUIMVP_UGATE2
CPUIMVP_PHASE2
CPUIMVP_LGATE2
R7522
2.2
CPUIMVP_PH2_SNUB
C7522
0.001UF
Q7525
649135PBF
DIRECTFET_S3C
376S1011
R7523
46.4
R7524
10
C7582
330PF
C7523
C7524
C7525
C7526
C7527
C7528
0.001UF
C7529
0.001UF
THESE TWO CAPS ARE FOR EMC
Additonal Input Bulk Caps (D SIZE)
PHASE 3
376S1014
Q7530
649136PBF
S1
L7530
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
PPVCORE_S0_CPU_PH3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
R7530
0.00075
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS3_P
CPUIMVP_ISNS3_N
CPUIMVP_ISUMN
CPUIMVP_ISUM3P
=PP5V_S0_CPUIMVP
U7541
MAX17491
TQFN
VDD
PWN
SKIP*
BST
DH
LX
DL
GND
THRM PAD
CPUIMVP_PWM3
CPUIMVP_SKIP
CPUIMVP_BOOT3_RC
R7531
3.3
C7531
0.22UF
CPUIMVP_BOOT3
CPUIMVP_UGATE3
CPUIMVP_PHASE3
CPUIMVP_LGATE3
R7532
2.2
CPUIMVP_PH3_SNUB
C7532
0.001UF
Q7535
649135PBF
DIRECTFET_S3C
376S1011
R7533
46.4
R7534
10
C7583
330PF
R7541
1UF
R7547
10K
C7533
C7534
C7535
C7536
C7537
C7538
0.001UF
C7539
0.001UF
C7570
C7571
C7572
C7574
C7575
C7578
15UF
(B SIZE)
C7573
15UF
C7576
15UF
AXG PHASE 1
=PPVIN_S0_CPUAXG
376S1010
Q7550
IRF6802SDTRPBF
DIRECTFET-SA
L7550
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
PPVCORE_S0_AXG1_L
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
R7550
0.00075
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N
CPUIMVP_ISUMGN
CPUIMVP_ISUMG1P
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
R7556
0
CPUIMVP_BOOT1G_R
C7551
0.22UF
R7552
2.2
CPUIMVP_AXG1_SNUB
C7552
0.001UF
Q7551
649135PBF
DIRECTFET_S3C
376S1011
R7553
46.4
R7554
10
C7584
330PF
C7540
1UF
R7540
10K
C7552
C7553
C7554
C7555
C7556
C7557
C7558
0.001UF
C7559
0.001UF
THESE TWO CAPS ARE FOR EMC
AXG PHASE 2
376S1010
Q7550
IRF6802SDTRPBF
DIRECTFET-SA
L7560
0.36UH-20%-36A-0.001080HM
PIMS103T-SM
152S1538
PPVCORE_S0_AXG2_L
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
R7560
0.00075
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS2G_N
CPUIMVP_ISNS2G_P
CPUIMVP_ISUMGN
CPUIMVP_ISUMG2P
CPUIMVP_AXG2_SNUB
R7587
2.2
C7587
0.001UF
Q7561
649135PBF
DIRECTFET_S3C
376S1011
R7561
46.4
R7562
10
C7567
330PF
CPUIMVP_ISNS1G_P
R7563
200
R7564
200
CPUIMVP_ISUMG_AVEP
R7565
0
R7566
0
CPUIMVP_ISUMG_AVE_RP
C7568
1000PF
C7569
330PF
CPUIMVP_ISUMGN
C7560
C7561
C7562
C7563
C7564
C7565
0.001UF
C7566
0.001UF
CPUIMVP_AXG_PWM2
CPUIMVP_SKIP
CPUIMVP_BOOT2G
CPUIMVP_UGATE2G
CPUIMVP_PHASE2G
CPUIMVP_LGATE2G
CPUIMVP_BOOT2G_RC
R7535
3.3
C7530
0.22UF
C7540
1UF
R7540
10K
U7542
MAX17491
TQFN
VDD
PWN
SKIP*
BST
DH
LX
DL
GND
THRM PAD
CRITICAL
OMIT_TABLE
NOSTUFF
DIDT=TRUE
GATE_NODE=TRUE
SWITCH_NODE=TRUE
SYNC MASTER=D2 SEAN
SYNC DATE=03/05/2012
PAGE TITLE
CPU IMVP7 & AXG VCore Output
Apple Inc.
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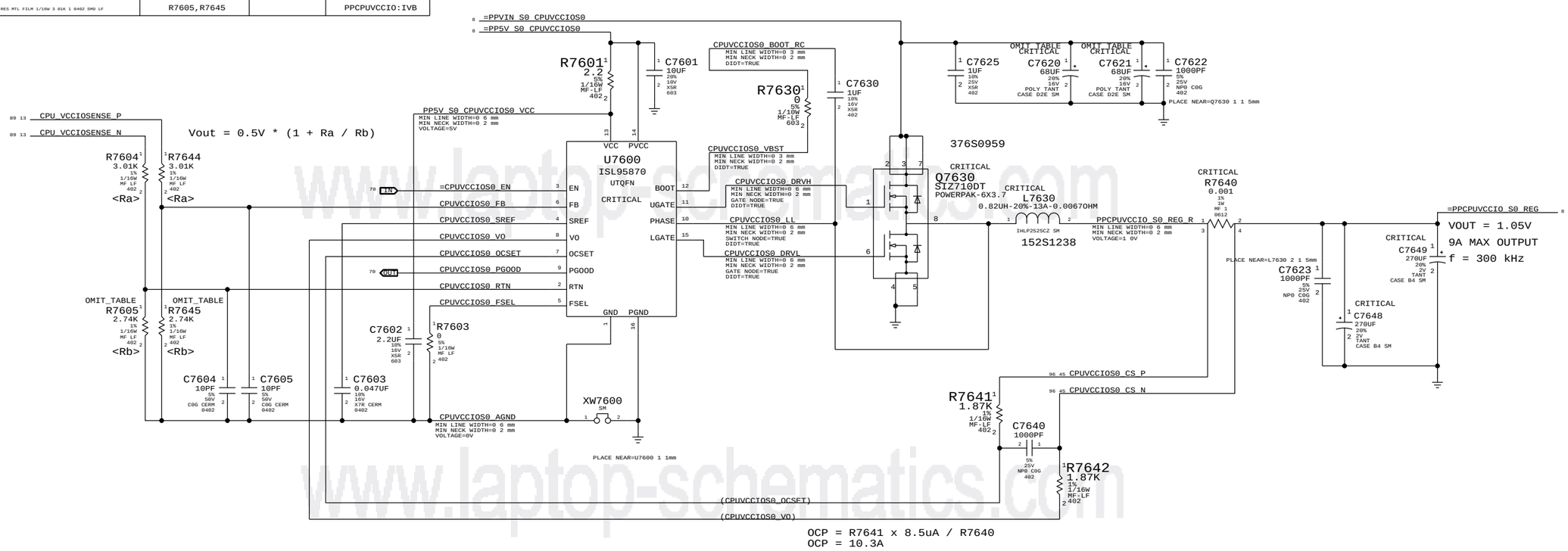
CPU VCCIO (1V0R1V05 S0) REGULATOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0260	2	RES MTL FILM 1/16W 2 74K 1 0402 SMD LF	R7605,R7645		PPCPUVCCIO:SNB
114S0264	2	RES MTL FILM 1/16W 3 01K 1 0402 SMD LF	R7605,R7645		PPCPUVCCIO:IVB



SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

CPU VCCIO (1V0R1V05 S0) POWER SUPPLY

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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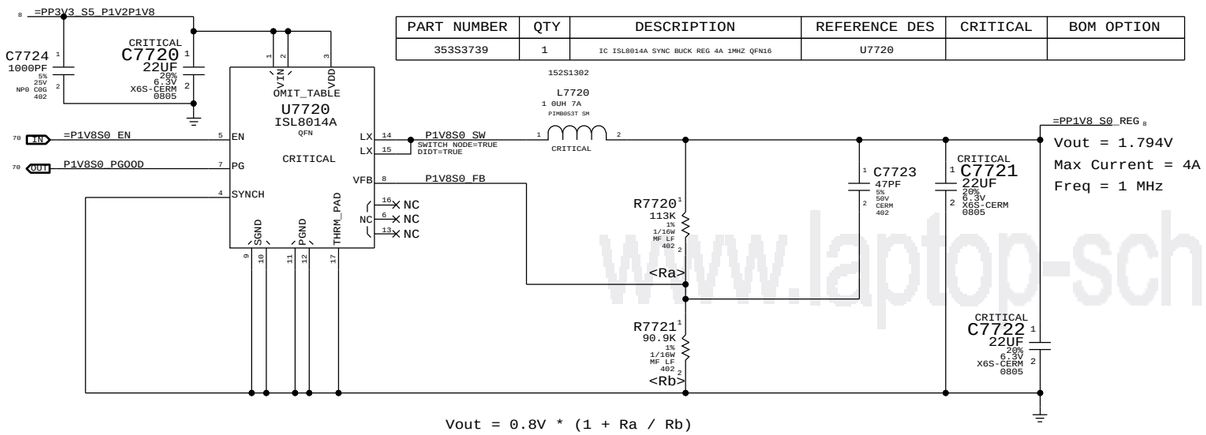
1.8V S0 Regulator

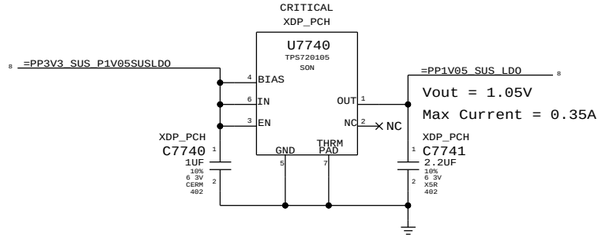
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3739	1	IC ISL8014A SYNC BUCK REG 4A 1MHZ QFN16	U7720		



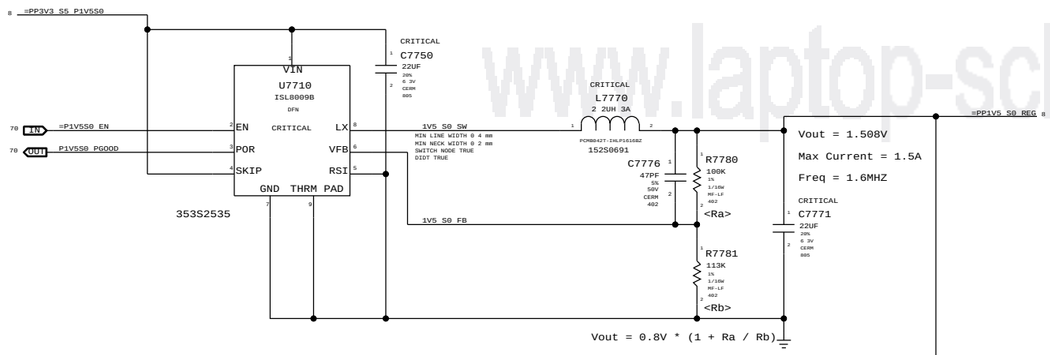
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

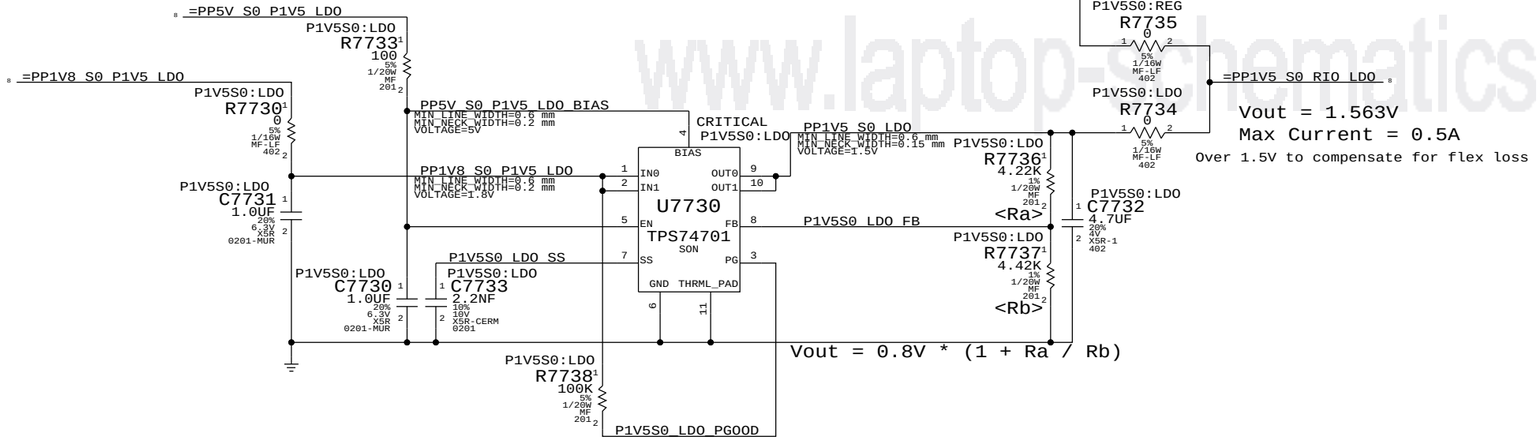
Panther Point-M requires JTAG pull-ups to be powered at 1.05V in Sus.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V Sus, which burns 100mW in all S-states.



1.5V S0 Regulator



1.5V S0 LDO (RIO)



Vout = 0.8V * (1 + Ra / Rb)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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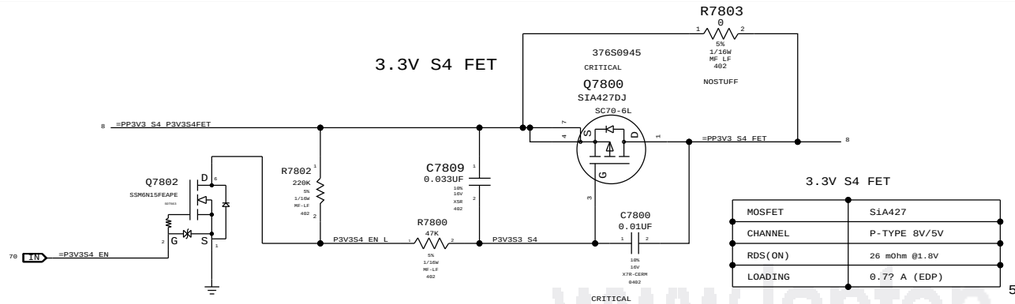
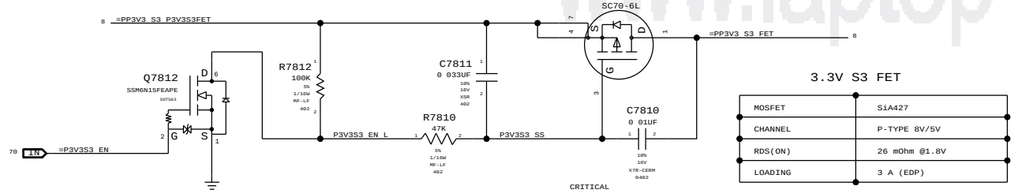
3.3V S4 FET



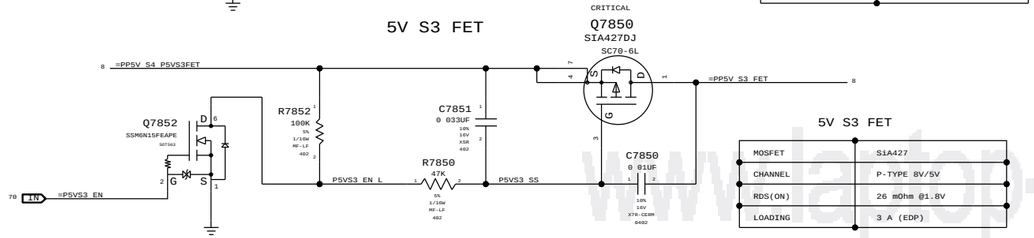
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



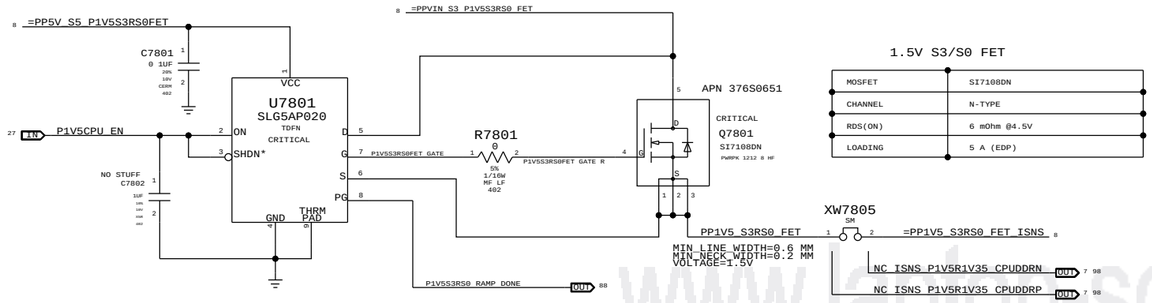
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

5V S3 FET



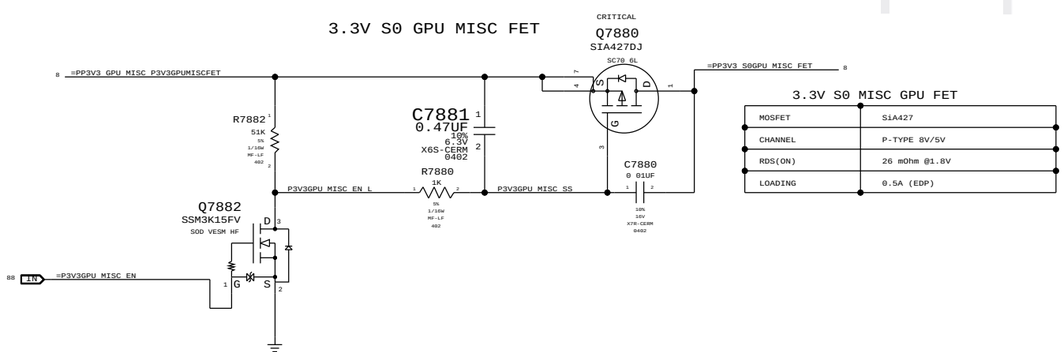
5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3 A (EDP)

1.5V S3/S0 FET



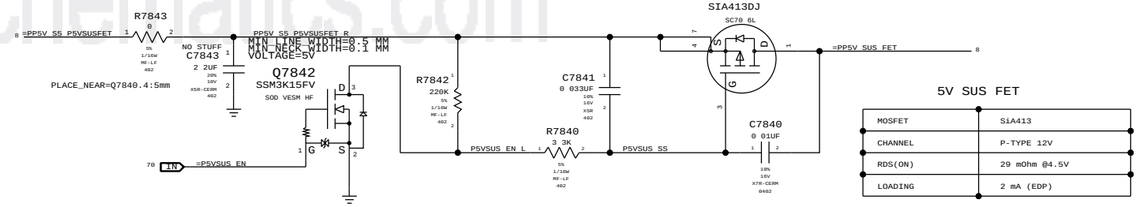
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 GPU MISC FET

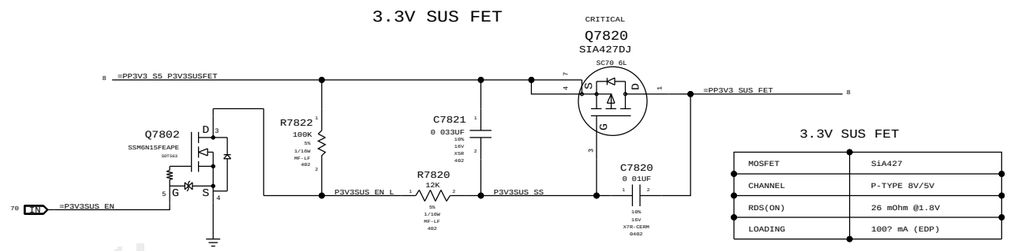


3.3V S0 MISC GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5A (EDP)

5V_SUS FET INPUT FILTER



3.3V SUS FET

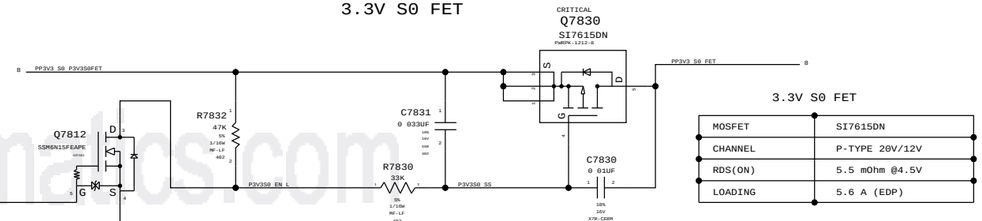


3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

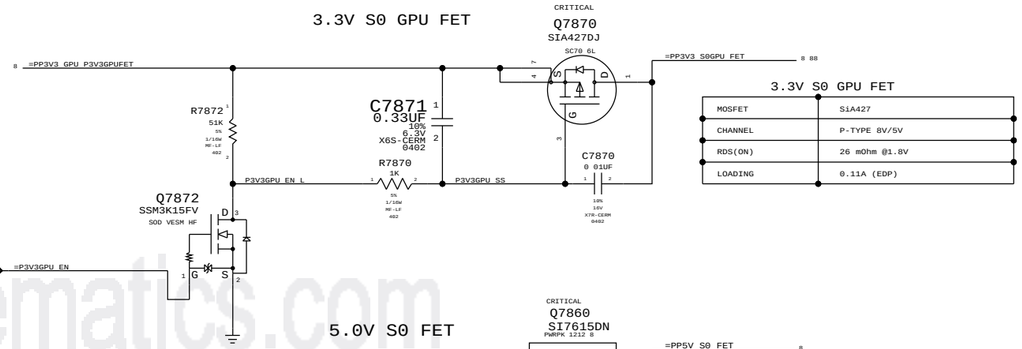
5V SUS FET	
MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	2 mA (EDP)

3.3V S0 FET



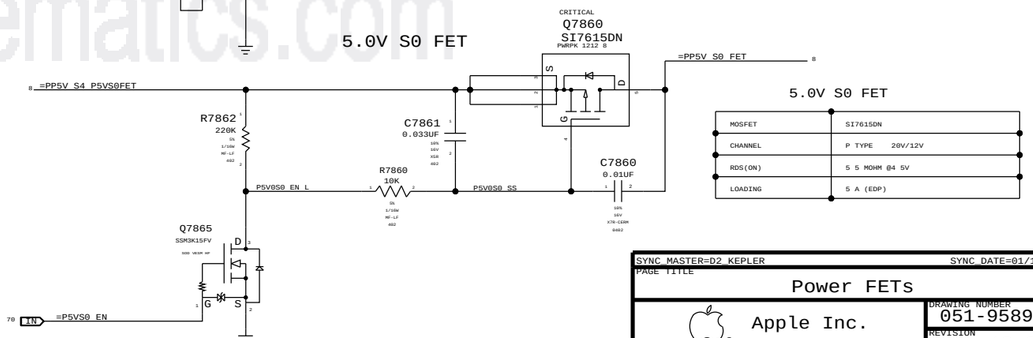
3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P TYPE 20V/12V
RDS(ON)	5 5 MOHM @4 5V
LOADING	5 A (EDP)

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9589 SIZE D

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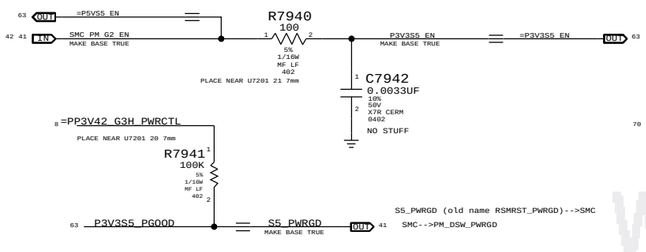
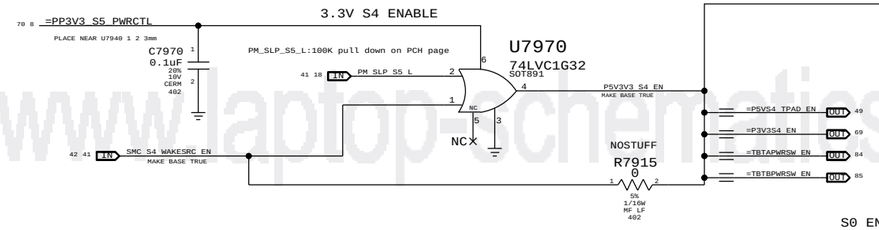
S5 Rail Enables & PGOOD



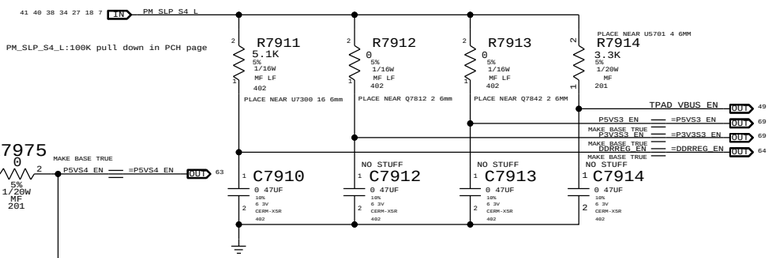
Mobile System Power State Table

State	SMC ADAPTER EN	SMC PM G2 ENABLE	SMC S4 WAKESRC EN	PM SUS EN	PM SLP S5 L	PM SLP S4 L	PM SLP S3 L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

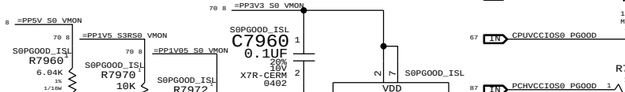
3.3V S4 ENABLE



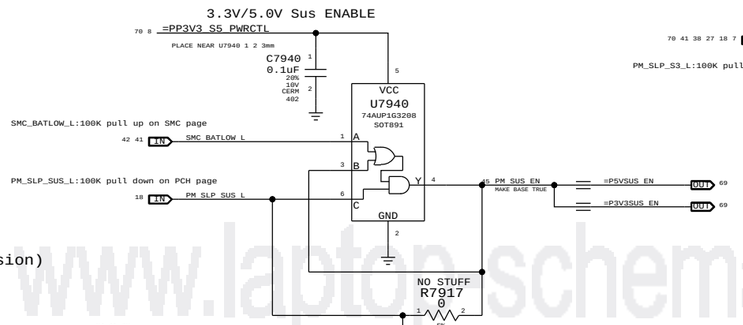
5V, 3.3V, DDR S3 ENABLE



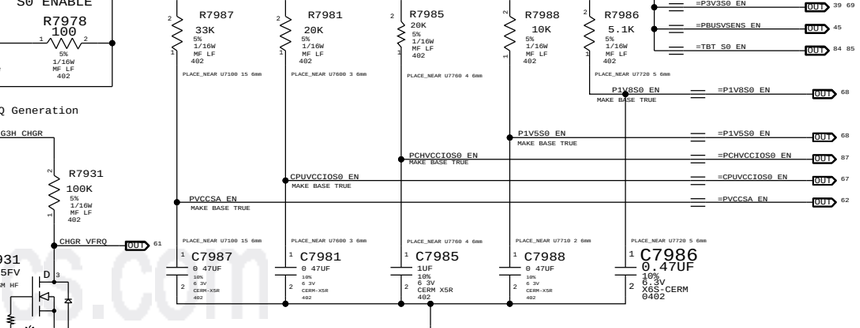
CPUVCORE ENABLE



3.3V/5.0V Sus ENABLE



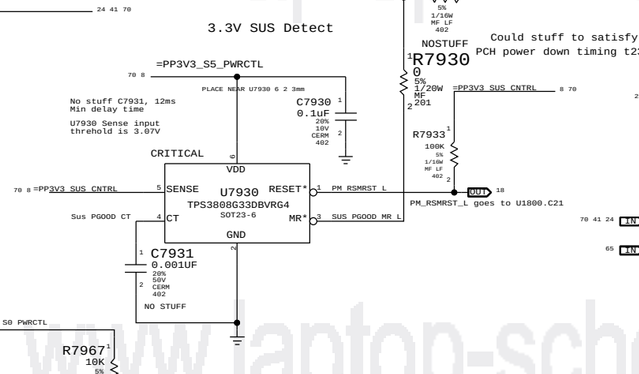
S0 ENABLE



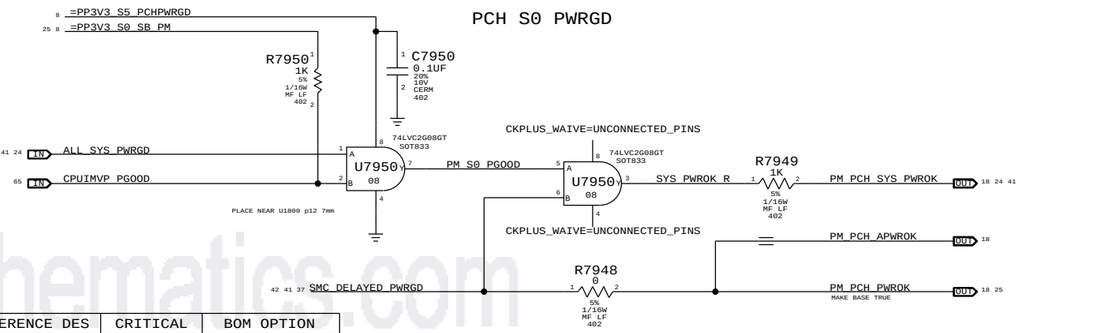
CHGR VFRQ Generation

S0 Rail PGOOD (BJT Version)

3.3V SUS Detect



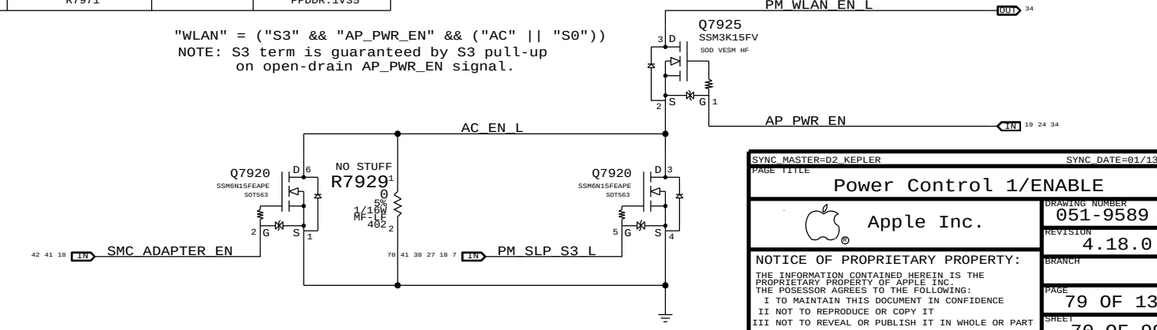
PCH S0 PWRGD



S0 Rail PGOOD Circuitry
(ISL Version in development)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0315	1	RES MTL FILM 1/16W 10K 1 0402 SMD LF	R7971		PPDDR:1V5
114S0323	1	RES MTL FILM 1/16W 12 4K 1 0402 SMD LF	R7971		PPDDR:1V35

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

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Page Notes

Power aliases required by this page

PP3V3 GPU VDD33

Signal aliases required by this page

(NONE)

BOM options provided by this page

(NONE)

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GND_VOID=TRUE 1 2 20% 6.3V X6S CERM 0201

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GND_VOID=TRUE 1 2 20% 6.3V X6S CERM 0201

OMIT_TABLE

U8000
NV-GK107
BGA
(1 OF 10)

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89 88 71	PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7>	71 89
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NC		AP21	PEX_RX8*	PEX_TX8*	AJ20	NC	
NC		AN21	PEX_RX9	PEX_TX9	AH20	NC	
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NC		AN23	PEX_RX10	PEX_TX10	AK21	NC	
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NC		AM24	PEX_RX12*	PEX_TX12*	AJ23	NC	
NC		AN26	PEX_RX13	PEX_TX13	AH23	NC	
NC		AM26	PEX_RX13*	PEX_TX13*	AG23	NC	
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92 17	IN PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	PEX_TSTCLK_O_N	95 92
78 9	IN GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29		
78 71	OUT PEX_CLKREQ_L_R	AK12	PEX_CLKREQ*	PEX_SVDD_3V3	AG12	PP3V3_GPU_PEX_PLL_HVDD	79
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R8001 10K 1% 1/20W MF 201 (1 — 2)

PEX_CLKREQ_L_R 78 71

NOSTUFF R8002 200 1% 1/20W MF 201

R8000 0 5% 1/20W MF 201 (GPU_RESET_L 78 9 IN → GPU_RESET_R_L)

R8005 2.49K 1% 1/20W MF 201

GPU_PEX_TERMP

PP3V3_GPU_PEX_PLL_HVDD 79

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: KEPLER PCI-E

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

BRANCH:

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OMIT_TABLE

=PP1V35_GPU_FBVDDQ
76 75 72 8

U8000
NV-GK107
BGA
(7 OF 10)

AA27			H18
AA30			H19
AB27			H20
AB33			H21
AC27			H22
AD27			H23
AE27			H24
AF27			H8
AG27			H9
B13			L27
B16	FBVDDQ	FBVDDQ	M27
B19			N27
E13			P27
E16			R27
E19			T27
H10			T30
H11			T33
H12			V27
H13			W27
H14			W30
H15			W33
H16			Y27

=PP1V35_GPU_FBVDDQ
8 72 75 76

OMIT_TABLE

=PPVCORE_GPU
79 72 8

U8000
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BGA
(10 OF 10)

AA12			V17
AA14			V18
AA16			V20
AA19			V22
AA21			W12
AA23			W14
AB13			W16
AB15		VDD	W19
AB17			W21
AB18			W23
AB20			Y13
AB22			Y15
AC12			Y17
AC14			Y18
AC16			Y20
AC19			Y22
AC21			U1 NC
AC23			U2 NC
M12			U3 NC
M14			U4 NC
M16			U5 NC
M19			U6 NC
M21			U7 NC
M23			U8 NC
N13			V1 NC
N15			V2 NC
N17		VDD	V3 NC
N18			V4 NC
N20			V5 NC
N22			V6 NC
P12			V7 NC
P14			V8 NC
P16			W2 NC
P19			W3 NC
P21			W4 NC
P23			W5 NC
R13			W7 NC
R15		XVDD	W8 NC
R17			Y1 NC
R18			Y2 NC
R20			Y3 NC
R22			Y4 NC
T12			Y5 NC
T14			Y6 NC
T16			Y7 NC
T19			Y8 NC
T21			AA1 NC
T23			AA2 NC
U13			AA3 NC
U15			AA4 NC
U17			AA5 NC
U18			AA6 NC
U20			AA7 NC
U22			AA8 NC
V13			
V15			

=PPVCORE_GPU
8 72 79

Page Notes

Power aliases required by this page

PPVCORE GPU
PP1V35 GPU FBVDDQ

Signal aliases required by this page

(NONE)

BOM options provided by this page

(NONE)

=PPVCORE_GPU
79 72 8

EDP = 30 A

NOSTUFF C8161 47UF 20% 4V X6S 0805	NOSTUFF C8198 22UF 20% 4V X6S-CERM 0603	NOSTUFF C8199 22UF 20% 4V X6S-CERM 0603	CRITICAL C8162 20UF 20% 2V X6T-CERM 0402	CRITICAL C8163 20UF 20% 2V X6T-CERM 0402	CRITICAL C8164 20UF 20% 2V X6T-CERM 0402	CRITICAL C8165 20UF 20% 2V X6T-CERM 0402	NOSTUFF C8182 20UF 20% 2V X6T-CERM 0402	NOSTUFF C8183 20UF 20% 2V X6T-CERM 0402	C8166 10UF 20% 4V X6S-CERM 0402-1	C8167 10UF 20% 4V X6S-CERM 0402-1

CRITICAL C8145 20UF 20% 2V X6T-CERM 0402	CRITICAL C8146 20UF 20% 2V X6T-CERM 0402	CRITICAL C8147 20UF 20% 2V X6T-CERM 0402	CRITICAL C8148 20UF 20% 2V X6T-CERM 0402	NOSTUFF C8149 20UF 20% 2V X6T-CERM 0402	NOSTUFF C8150 20UF 20% 2V X6T-CERM 0402	NOSTUFF C8151 20UF 20% 2V X6T-CERM 0402	

C8168 10UF 20% 4V X6S-CERM 0402-1	C8169 10UF 20% 4V X6S-CERM 0402-1	C8170 10UF 20% 4V X6S-CERM 0402-1	C8171 10UF 20% 4V X6S-CERM 0402-1	C8172 10UF 20% 4V X6S-CERM 0402-1	C8173 10UF 20% 4V X6S-CERM 0402-1	C8174 10UF 20% 4V X6S-CERM 0402-1	C8175 10UF 20% 4V X6S-CERM 0402-1	C8176 10UF 20% 4V X6S-CERM 0402-1	C8177 10UF 20% 4V X6S-CERM 0402-1

C8178 10UF 20% 4V X6S-CERM 0402-1	C8179 10UF 20% 4V X6S-CERM 0402-1	C8180 10UF 20% 4V X6S-CERM 0402-1	C8181 10UF 20% 4V X6S-CERM 0402-1	C8184 10UF 20% 4V X6S-CERM 0402-1	C8185 10UF 20% 4V X6S-CERM 0402-1	CRITICAL C8186 1UF 20% 4V CERM X6S 0201	CRITICAL C8187 1UF 20% 4V CERM X6S 0201	CRITICAL C8188 1UF 20% 4V CERM X6S 0201	CRITICAL C8189 1UF 20% 4V CERM-X6S 0201

CRITICAL C8190 1UF 20% 4V CERM X6S 0201	C8191 0.1UF 10% 6.3V X6S 0201	C8192 0.1UF 10% 6.3V X6S 0201	C8193 0.1UF 10% 6.3V X6S 0201	C8194 0.1UF 10% 6.3V X6S 0201	C8195 0.1UF 10% 6.3V X6S 0201	C8196 1000PF 10% 16V X7R CERM 0201	C8197 1000PF 10% 16V X7R CERM 0201

GPU VCORE DE-COUPLING

NOTE: ATLEAST 2 GND VIAS & 2 POWER VIAS PER CAP

=PP1V35_GPU_FBVDDQ
76 75 72 8

GPU FB DE-COUPLING

EDP = 6500 MA

C8125 20UF 20% 2V X6T CERM 0402	C8126 20UF 20% 2V X6T CERM 0402	C8127 20UF 20% 2V X6T CERM 0402	C8128 20UF 20% 2V X6T CERM 0402	C8101 10UF 20% 4V X6S CERM 0402 1	C8102 10UF 20% 4V X6S CERM 0402 1	C8103 10UF 20% 4V X6S CERM 0402 1	C8104 10UF 20% 4V X6S CERM 0402 1

C8105 4.7UF 20% 6.3V X6S 0402	C8106 4.7UF 20% 6.3V X6S 0402	C8107 4.7UF 20% 6.3V X6S 0402	C8108 4.7UF 20% 6.3V X6S 0402	C8109 4.7UF 20% 6.3V X6S 0402	C8110 4.7UF 20% 6.3V X6S 0402	C8111 1UF 20% 4V CERM X6S 0201	C8112 1UF 20% 4V CERM X6S 0201	C8113 1UF 20% 4V CERM X6S 0201	C8114 1UF 20% 4V CERM X6S 0201

C8115 0.1UF 10% 6.3V X6S 0201	C8118 0.1UF 10% 6.3V X6S 0201	C8119 0.1UF 10% 6.3V X6S 0201	C8120 0.1UF 10% 6.3V X6S 0201	C8121 0.1UF 10% 6.3V X6S 0201	C8122 0.1UF 10% 6.3V X6S 0201	C8123 0.1UF 10% 6.3V X6S 0201	C8124 0.1UF 10% 6.3V X6S 0201

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE

KEPLER CORE/FB POWER

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NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

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MEM INTERFACE A

FB_A0_DQ<0>	L28	FBA_D0	U30	FBA_CMD0	FB_A0_CS_L	OUT
FB_A0_DQ<1>	M29	FBA_D1	T31	FBA_CMD1	FB_A0_A<3>	OUT
FB_A0_DQ<2>	L29	FBA_D2	U29	FBA_CMD2	FB_A0_A<2>	OUT
FB_A0_DQ<3>	M28	FBA_D3	R34	FBA_CMD3	FB_A0_A<4>	OUT
FB_A0_DQ<4>	N31	FBA_D4	R33	FBA_CMD4	FB_A0_A<5>	OUT
FB_A0_DQ<5>	P29	FBA_D5	U32	FBA_CMD5	FB_A0_WE_L	OUT
FB_A0_DQ<6>	R29	FBA_D6	U33	FBA_CMD6	FB_A0_A<7>	OUT
FB_A0_DQ<7>	P28	FBA_D7	U28	FBA_CMD7	FB_A0_A<6>	OUT
FB_A0_DQ<8>	J28	FBA_D8	V28	FBA_CMD8	FB_A0_ABI_L	OUT
FB_A0_DQ<9>	H29	FBA_D9	V29	FBA_CMD9	FB_A0_A<8>	OUT
FB_A0_DQ<10>	J29	FBA_D10	V30	FBA_CMD10	FB_A0_A<0>	OUT
FB_A0_DQ<11>	H28	FBA_D11	U34	FBA_CMD11	FB_A0_A<1>	OUT
FB_A0_DQ<12>	G29	FBA_D12	U31	FBA_CMD12	FB_A0_RAS_L	OUT
FB_A0_DQ<13>	E31	FBA_D13	V34	FBA_CMD13	FB_A0_RESET_L	OUT 73 75 95
FB_A0_DQ<14>	E32	FBA_D14	V33	FBA_CMD14	FB_A0_CKE_L	OUT 73 75 95
FB_A0_DQ<15>	F30	FBA_D15	Y32	FBA_CMD15	FB_A0_CAS_L	OUT
FB_A0_DQ<16>	C34	FBA_D16	AA31	FBA_CMD16	FB_A1_CS_L	OUT
FB_A0_DQ<17>	D32	FBA_D17	AA29	FBA_CMD17	FB_A1_A<3>	OUT
FB_A0_DQ<18>	B33	FBA_D18	AA28	FBA_CMD18	FB_A1_A<2>	OUT
FB_A0_DQ<19>	C33	FBA_D19	AC34	FBA_CMD19	FB_A1_A<4>	OUT
FB_A0_DQ<20>	F33	FBA_D20	AC33	FBA_CMD20	FB_A1_A<5>	OUT
FB_A0_DQ<21>	F32	FBA_D21	AA32	FBA_CMD21	FB_A1_WE_L	OUT
FB_A0_DQ<22>	H33	FBA_D22	AA33	FBA_CMD22	FB_A1_A<7>	OUT
FB_A0_DQ<23>	H32	FBA_D23	Y28	FBA_CMD23	FB_A1_A<6>	OUT
FB_A0_DQ<24>	P34	FBA_D24	Y29	FBA_CMD24	FB_A1_ABI_L	OUT
FB_A0_DQ<25>	P32	FBA_D25	W31	FBA_CMD25	FB_A1_A<8>	OUT
FB_A0_DQ<26>	P31	FBA_D26	Y30	FBA_CMD26	FB_A1_A<0>	OUT
FB_A0_DQ<27>	P33	FBA_D27	AA34	FBA_CMD27	FB_A1_A<1>	OUT
FB_A0_DQ<28>	L31	FBA_D28	Y31	FBA_CMD28	FB_A1_RAS_L	OUT
FB_A0_DQ<29>	L34	FBA_D29	Y34	FBA_CMD29	FB_A1_RESET_L	OUT 73 75 95
FB_A0_DQ<30>	L32	FBA_D30	Y33	FBA_CMD30	FB_A1_CKE_L	OUT 73 75 95
FB_A0_DQ<31>	L33	FBA_D31	V31	FBA_CMD31	FB_A1_CAS_L	OUT
FB_A1_DQ<0>	AG28	FBA_D32				
FB_A1_DQ<1>	AF29	FBA_D33	R30	FBA_CLK0	FB_A0_CLK_P	OUT
FB_A1_DQ<2>	AG29	FBA_D34	R31	FBA_CLK0*	FB_A0_CLK_N	OUT
FB_A1_DQ<3>	AF28	FBA_D35	AB31	FBA_CLK1	FB_A1_CLK_P	OUT
FB_A1_DQ<4>	AD30	FBA_D36	AC31	FBA_CLK1*	FB_A1_CLK_N	OUT
FB_A1_DQ<5>	AD29	FBA_D37				
FB_A1_DQ<6>	AC29	FBA_D38	P30	FBA_DQM0	FB_A0_DBI_L<0>	BI
FB_A1_DQ<7>	AD28	FBA_D39	F31	FBA_DQM1	FB_A0_DBI_L<1>	BI
FB_A1_DQ<8>	AJ29	FBA_D40	F34	FBA_DQM2	FB_A0_DBI_L<2>	BI
FB_A1_DQ<9>	AK29	FBA_D41	M32	FBA_DQM3	FB_A0_DBI_L<3>	BI
FB_A1_DQ<10>	AJ30	FBA_D42	AD31	FBA_DQM4	FB_A1_DBI_L<0>	BI
FB_A1_DQ<11>	AK28	FBA_D43	AL29	FBA_DQM5	FB_A1_DBI_L<1>	BI
FB_A1_DQ<12>	AM29	FBA_D44	AM32	FBA_DQM6	FB_A1_DBI_L<2>	BI
FB_A1_DQ<13>	AM31	FBA_D45	AF34	FBA_DQM7	FB_A1_DBI_L<3>	BI
FB_A1_DQ<14>	AN29	FBA_D46				
FB_A1_DQ<15>	AM30	FBA_D47	M30	FBA_DQS_RN0	NC	
FB_A1_DQ<16>	AN31	FBA_D48	H30	FBA_DQS_RN1	NC	
FB_A1_DQ<17>	AN32	FBA_D49	E34	FBA_DQS_RN2	NC	
FB_A1_DQ<18>	AP30	FBA_D50	M34	FBA_DQS_RN3	NC	
FB_A1_DQ<19>	AP32	FBA_D51	AF30	FBA_DQS_RN4	NC	
FB_A1_DQ<20>	AM33	FBA_D52	AK31	FBA_DQS_RN5	NC	
FB_A1_DQ<21>	AL31	FBA_D53	AM34	FBA_DQS_RN6	NC	
FB_A1_DQ<22>	AK33	FBA_D54	AF32	FBA_DQS_RN7	NC	
FB_A1_DQ<23>	AK32	FBA_D55				
FB_A1_DQ<24>	AD34	FBA_D56	M31	FBA_DQS_WP0	FB_A0_EDC<0>	IN
FB_A1_DQ<25>	AD32	FBA_D57	G31	FBA_DQS_WP1	FB_A0_EDC<1>	IN
FB_A1_DQ<26>	AC30	FBA_D58	E33	FBA_DQS_WP2	FB_A0_EDC<2>	IN
FB_A1_DQ<27>	AD33	FBA_D59	M33	FBA_DQS_WP3	FB_A0_EDC<3>	IN
FB_A1_DQ<28>	AF31	FBA_D60	AE31	FBA_DQS_WP4	FB_A1_EDC<0>	IN
FB_A1_DQ<29>	AG34	FBA_D61	AK30	FBA_DQS_WP5	FB_A1_EDC<1>	IN
FB_A1_DQ<30>	AG32	FBA_D62	AN33	FBA_DQS_WP6	FB_A1_EDC<2>	IN
FB_A1_DQ<31>	AG33	FBA_D63	AF33	FBA_DQS_WP7	FB_A1_EDC<3>	IN
FB_A0_WCLK_P<0>	K31	FBA_WCK01	K27	FB_DLL_AVDD	PP1V05_GPU_FB_DLL_AVDD	73
FB_A0_WCLK_N<0>	L30	FBA_WCK01*	U27	FBA_PLL_AVDD	PP1V05_GPU_FB_PLL_AVDD	73
FB_A0_WCLK_P<1>	H34	FBA_WCK23	R28	FBA_DEBUG	GPU_FBA_DEBUG0	
FB_A0_WCLK_N<1>	J34	FBA_WCK23*	AC28	FBA_DEBUG	GPU_FBA_DEBUG1	
FB_A1_WCLK_P<0>	AG30	FBA_WCK45	J27	FB_CAL_PD_VDDQ	FB_CAL_PD_VDDQ	73
FB_A1_WCLK_N<0>	AG31	FBA_WCK45*	H27	FB_CAL_PU_GND	FB_CAL_PU_GND	73
FB_A1_WCLK_P<1>	AJ34	FBA_WCK67	H25	FB_CAL_TERM_GND	FB_CAL_TERM_GND	1
FB_A1_WCLK_N<1>	AK34	FBA_WCK67*	E1	82 FB_CLAMP	FB_CLAMP	
	J30	FBA_WCKB01	R32	FB_CMD_RFU	NC	
	J31	FBA_WCKB01*	AC32	FB_CMD_RFU	NC	
	J32	FBA_WCKB23	F1	FB_VDDQ_SENSE	GPU_FBVDDQ_SENSE	OUT 74 97
	J33	FBA_WCKB23*	F2	FB_GND_SENSE	GPU_FBGND_SENSE	OUT 74 97
	AH31	FBA_WCKB45				
	AJ31	FBA_WCKB45*				
	AJ32	FBA_WCKB67				
	AJ33	FBA_WCKB67*				

95 75 73 FB_A0_RESET_L — R8250 10K 1% 1/20W MF 201

95 75 73 FB_A1_RESET_L — R8251 10K 1% 1/20W MF 201

FB_A0_CKE_L 73 75 95 — R8252 10K 1% 1/20W MF 201

FB_A1_CKE_L 73 75 95 — R8253 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 8 73

R8258 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8000 H26 8 4MM

FB_VREF 73

R8259 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8000 H26 8 4MM

NOSTUFF C8260 0.1UF 10% 6.3V X6S 0201

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 8 73

R8203 60.4 1% 1/20W MF 201

R8202 60.4 1% 1/20W MF 201

R8270 100 5% 1/20W MF 201

R8201 60.4 1% 1/20W MF 201 — PLACE NEAR=U8000 H25 8 4MM

R8261 10K MF 1% 1/20W 201

PLACE CLOSE TO BGA

73 FB_CAL_PU_GND — R8204 40.2 1% 1/20W MF 201 — PLACE NEAR=U8000 H27 8 4MM

=PP1V35_GPU_S0_FB 8 73 — R8205 40.2 1% 1/20W MF 201 — PLACE NEAR=U8000 J27 8 4MM

FB_CAL_PD_VDDQ 73

R8271 100 5% 1/20W MF 201

OMIT_TABLE

U8000
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MEM INTRERFACE B

FB_B0_DQ<0>	G9	FBB_D0	D13	FBB_CMD0	FB_B0_CS_L	OUT
FB_B0_DQ<1>	E9	FBB_D1	E14	FBB_CMD1	FB_B0_A<3>	OUT
FB_B0_DQ<2>	G8	FBB_D2	F14	FBB_CMD2	FB_B0_A<2>	OUT
FB_B0_DQ<3>	F9	FBB_D3	A12	FBB_CMD3	FB_B0_A<4>	OUT
FB_B0_DQ<4>	F11	FBB_D4	B12	FBB_CMD4	FB_B0_A<5>	OUT
FB_B0_DQ<5>	G11	FBB_D5	C14	FBB_CMD5	FB_B0_WE_L	OUT
FB_B0_DQ<6>	F12	FBB_D6	B14	FBB_CMD6	FB_B0_A<7>	OUT
FB_B0_DQ<7>	G12	FBB_D7	G15	FBB_CMD7	FB_B0_A<6>	OUT
FB_B0_DQ<8>	G6	FBB_D8	F15	FBB_CMD8	FB_B0_ABI_L	OUT
FB_B0_DQ<9>	F5	FBB_D9	E15	FBB_CMD9	FB_B0_A<8>	OUT
FB_B0_DQ<10>	E6	FBB_D10	D15	FBB_CMD10	FB_B0_A<0>	OUT
FB_B0_DQ<11>	F6	FBB_D11	A14	FBB_CMD11	FB_B0_A<1>	OUT
FB_B0_DQ<12>	F4	FBB_D12	D14	FBB_CMD12	FB_B0_RAS_L	OUT
FB_B0_DQ<13>	G4	FBB_D13	A15	FBB_CMD13	FB_B0_RESET_L	OUT 73 76 95
FB_B0_DQ<14>	E2	FBB_D14	B15	FBB_CMD14	FB_B0_CKE_L	OUT 73 76 95
FB_B0_DQ<15>	F3	FBB_D15	C17	FBB_CMD15	FB_B0_CAS_L	OUT
FB_B0_DQ<16>	C2	FBB_D16	D18	FBB_CMD16	FB_B1_CS_L	OUT
FB_B0_DQ<17>	D4	FBB_D17	E18	FBB_CMD17	FB_B1_A<3>	OUT 76 95 79 73 8
FB_B0_DQ<18>	D3	FBB_D18	F18	FBB_CMD18	FB_B1_A<2>	OUT
FB_B0_DQ<19>	C1	FBB_D19	A20	FBB_CMD19	FB_B1_A<4>	OUT
FB_B0_DQ<20>	B3	FBB_D20	B20	FBB_CMD20	FB_B1_A<5>	OUT
FB_B0_DQ<21>	C4	FBB_D21	C18	FBB_CMD21	FB_B1_WE_L	OUT
FB_B0_DQ<22>	B5	FBB_D22	B18	FBB_CMD22	FB_B1_A<7>	OUT
FB_B0_DQ<23>	C5	FBB_D23	G18	FBB_CMD23	FB_B1_A<6>	OUT
FB_B0_DQ<24>	A11	FBB_D24	G17	FBB_CMD24	FB_B1_ABI_L	OUT
FB_B0_DQ<25>	C11	FBB_D25	F17	FBB_CMD25	FB_B1_A<8>	OUT
FB_B0_DQ<26>	D11	FBB_D26	D16	FBB_CMD26	FB_B1_A<0>	OUT
FB_B0_DQ<27>	B11	FBB_D27	A18	FBB_CMD27	FB_B1_A<1>	OUT
FB_B0_DQ<28>	D8	FBB_D28	D17	FBB_CMD28	FB_B1_RAS_L	OUT
FB_B0_DQ<29>	A8	FBB_D29	A17	FBB_CMD29	FB_B1_RESET_L	OUT 73 76 95
FB_B0_DQ<30>	C8	FBB_D30	B17	FBB_CMD30	FB_B1_CKE_L	OUT 73 76 95
FB_B0_DQ<31>	B8	FBB_D31	E17	FBB_CMD31	FB_B1_CAS_L	OUT
FB_B1_DQ<0>	F24	FBB_D32				
FB_B1_DQ<1>	G23	FBB_D33	D12	FBB_CLK0	FB_B0_CLK_P	OUT
FB_B1_DQ<2>	E24	FBB_D34	E12	FBB_CLK0*	FB_B0_CLK_N	OUT
FB_B1_DQ<3>	G24	FBB_D35	E20	FBB_CLK1	FB_B1_CLK_P	OUT
FB_B1_DQ<4>	D21	FBB_D36	F20	FBB_CLK1*	FB_B1_CLK_N	OUT
FB_B1_DQ<5>	E21	FBB_D37				
FB_B1_DQ<6>	G21	FBB_D38	E11	FBB_DQM0	FB_B0_DBI_L<0>	BI
FB_B1_DQ<7>	F21	FBB_D39	E3	FBB_DQM1	FB_B0_DBI_L<1>	BI
FB_B1_DQ<8>	G27	FBB_D40	A3	FBB_DQM2	FB_B0_DBI_L<2>	BI
FB_B1_DQ<9>	D27	FBB_D41	C9	FBB_DQM3	FB_B0_DBI_L<3>	BI
FB_B1_DQ<10>	G26	FBB_D42	F23	FBB_DQM4	FB_B1_DBI_L<0>	BI
FB_B1_DQ<11>	E27	FBB_D43	F27	FBB_DQM5	FB_B1_DBI_L<1>	BI
FB_B1_DQ<12>	E29	FBB_D44	C30	FBB_DQM6	FB_B1_DBI_L<2>	BI
FB_B1_DQ<13>	F29	FBB_D45	A24	FBB_DQM7	FB_B1_DBI_L<3>	BI
FB_B1_DQ<14>	E30	FBB_D46				
FB_B1_DQ<15>	D30	FBB_D47	D9	FBB_DQS_RN0	NC	
FB_B1_DQ<16>	A32	FBB_D48	E4	FBB_DQS_RN1	NC	
FB_B1_DQ<17>	C31	FBB_D49	B2	FBB_DQS_RN2	NC	
FB_B1_DQ<18>	C32	FBB_D50	A9	FBB_DQS_RN3	NC	
FB_B1_DQ<19>	B32	FBB_D51	D22	FBB_DQS_RN4	NC	
FB_B1_DQ<20>	D29	FBB_D52	D28	FBB_DQS_RN5	NC	
FB_B1_DQ<21>	A29	FBB_D53	A30	FBB_DQS_RN6	NC	
FB_B1_DQ<22>	C29	FBB_D54	B23	FBB_DQS_RN7	NC	
FB_B1_DQ<23>	B29	FBB_D55				
FB_B1_DQ<24>	B21	FBB_D56	D10	FBB_DQS_WP0	FB_B0_EDC<0>	IN
FB_B1_DQ<25>	C23	FBB_D57	D5	FBB_DQS_WP1	FB_B0_EDC<1>	IN
FB_B1_DQ<26>	A21	FBB_D58	C3	FBB_DQS_WP2	FB_B0_EDC<2>	IN
FB_B1_DQ<27>	C21	FBB_D59	B9	FBB_DQS_WP3	FB_B0_EDC<3>	IN
FB_B1_DQ<28>	B24	FBB_D60	E23	FBB_DQS_WP4	FB_B1_EDC<0>	IN
FB_B1_DQ<29>	C24	FBB_D61	E28	FBB_DQS_WP5	FB_B1_EDC<1>	IN
FB_B1_DQ<30>	B26	FBB_D62	B30	FBB_DQS_WP6	FB_B1_EDC<2>	IN
FB_B1_DQ<31>	C26	FBB_D63	A23	FBB_DQS_WP7	FB_B1_EDC<3>	IN
FB_B0_WCLK_P<0>	F8	FBB_WCK01	H17	FBB_PLL_AVDD	PP1V05_GPU_FB_PLL_AVDD	73
FB_B0_WCLK_N<0>	E8	FBB_WCK01*	G14	FBB_DEBUG0	GPU_FBB_DEBUG0	73
FB_B0_WCLK_P<1>	A5	FBB_WCK23	G20	FBB_DEBUG1	GPU_FBB_DEBUG1	73
FB_B0_WCLK_N<1>	A6	FBB_WCK23*	H26	FB_VREF	FB_VREF	73
FB_B1_WCLK_P<0>	D24	FBB_WCK45	C12	FBB_CMD_RFU0	NC	
FB_B1_WCLK_N<0>	D25	FBB_WCK45*	C20	FBB_CMD_RFU1	NC	
FB_B1_WCLK_P<1>	B27	FBB_WCK67				
FB_B1_WCLK_N<1>	C27	FBB_WCK67*				
	D6	FBB_WCKB01				
	D7	FBB_WCKB01*				
	C6	FBB_WCKB23				
	B6	FBB_WCKB23*				
	F26	FBB_WCKB45				
	E26	FBB_WCKB45*				
	A26	FBB_WCKB67				
	A27	FBB_WCKB67*				

C8206 1UF 20% 4V CERM X6S 0201

C8207 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 8 73

R8206 60.4 1% 1/20W MF 201

R8207 60.4 1% 1/20W MF 201

GPU_FBB_DEBUG0 73

GPU_FBB_DEBUG1 73

Page Notes

Power aliases required by this page
PP1V35_GPU_S0_FB
PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page
(NONE)

BOM options provided by this page
(NONE)

L8201
FERR-220-OHM-2A
MIN LINE WIDTH=0.6 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD 8 73 79
PP1V05_GPU_FB_PLL_AVDD 73
0603
CRITICAL
ESR = 0.050OHM

C8201 20UF 20% 2V X6T CERM 0402

C8202 1UF 20% 4V CERM X6S 0402

C8203 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

L8202
FERR-220-OHM-2A
MIN LINE WIDTH=0.6 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD 8 73
PP1V05_GPU_FB_DLL_AVDD 73
0603
CRITICAL
ESR = 0.050OHM

C8208 20UF 20% 2V X6T CERM 0402

C8204 1UF 20% 4V CERM X6S 0201

C8205 0.1UF 10% 6.3V X6S 0201

95 76 73 FB_B0_RESET_L — R8254 10K 1% 1/20W MF 201

95 76 73 FB_B1_RESET_L — R8255 10K 1% 1/20W MF 201

73 76 95 FB_B0_CKE_L — R8256 10K 1% 1/20W MF 201

73 76 95 FB_B1_CKE_L — R8257 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH

76 75 FB_SW_LEG OUT

Q8265 SSM3K15FV SOD-VESM-HF

GPU_ALT_VREF IN 78

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	KEPLER FRAME BUFFER I/F
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 82 OF 132
	SHEET 73 OF 99

GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

GPU 1V05 SUPPLY

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-9589 SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 83 OF 132
	SHEET 74 OF 99

Page Notes

Power aliases required by this page
=PP1V5R1V35 S0 FB VDD

Signal aliases required by this page
(NONE)

BOM options provided by this page

CK TERMINATION - A0

PLACE_NEAR=U8400.J11:8.4MM

R8401 40.2 1% 1/20W MF 201 — FB_A0_CLK_P — FBA0_CK_MID — R8402 40.2 1% 1/20W MF 201 — FB_A0_CLK_N

C8490 0.01UF 10% 10V X7R-CERM 0201

PLACE NEAR=U8400 J12 8 4MM

PLACE NEAR=U8400 J11 8 4MM

R8400 120 1% 1/20W MF 201

R8404 120 1% 1/20W MF 201

R8403 120 1% 1/20W MF 201

CK TERMINATION - A1

PLACE NEAR=U8450 J11 8 4MM

R8451 40.2 1% 1/20W MF 201 — FB_A1_CLK_P — FBA1_CK_MID — R8452 40.2 1% 1/20W MF 201 — FB_A1_CLK_N

C8491 0.01UF 10% 10V X7R-CERM 0201

PLACE NEAR=U8450 J12 8 4MM

PLACE NEAR=U8450 J11 8 4MM

R8450 120 1% 1/20W MF 201

R8454 120 1% 1/20W MF 201

R8453 120 1% 1/20W MF 201

U8400

32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

OMIT_TABLE

FB_A0_A<2>	H11	BA0/A2	
FB_A0_A<5>	K10	BA1/A5	
FB_A0_A<4>	K11	BA2/A4	
FB_A0_A<3>	H10	BA3/A3	
FB_A0_A<7>	K4	A8/A7	
FB_A0_A<1>	H5	A9/A1	
FB_A0_A<0>	H4	A10/A0	
FB_A0_A<6>	K5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	G12	CS*	
FB_A0_WE_L	L12	WE*	
FB_A0_CAS_L	L3	CAS*	
FB_A0_RAS_L	G3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=0)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	C2	EDC0	
FB_A0_EDC<1>	C13	EDC1	
FB_A0_EDC<2>	R13	EDC2	
FB_A0_EDC<3>	R2	EDC3	
FB_A0_WCLK_P<0>	D4	WCK01	
FB_A0_WCLK_N<0>	D5	WCK01*	
FB_A0_WCLK_P<1>	P4	WCK23	
FB_A0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A0_DBI_L<0>	
DBI1*	D13	FB_A0_DBI_L<1>	
DBI2*	P13	FB_A0_DBI_L<2>	
DBI3*	P2	FB_A0_DBI_L<3>	
DQ0	A4	FB_A0_DQ<0>	
DQ1	A2	FB_A0_DQ<1>	
DQ2	B4	FB_A0_DQ<2>	
DQ3	B2	FB_A0_DQ<3>	
DQ4	E4	FB_A0_DQ<4>	
DQ5	E2	FB_A0_DQ<5>	
DQ6	F4	FB_A0_DQ<6>	
DQ7	F2	FB_A0_DQ<7>	
DQ8	A11	FB_A0_DQ<8>	
DQ9	A13	FB_A0_DQ<9>	
DQ10	B11	FB_A0_DQ<10>	
DQ11	B13	FB_A0_DQ<11>	
DQ12	E11	FB_A0_DQ<12>	
DQ13	E13	FB_A0_DQ<13>	
DQ14	F11	FB_A0_DQ<14>	
DQ15	F13	FB_A0_DQ<15>	
DQ16	U11	FB_A0_DQ<16>	
DQ17	U13	FB_A0_DQ<17>	
DQ18	T11	FB_A0_DQ<18>	
DQ19	T13	FB_A0_DQ<19>	
DQ20	N11	FB_A0_DQ<20>	
DQ21	N13	FB_A0_DQ<21>	
DQ22	M11	FB_A0_DQ<22>	
DQ23	M13	FB_A0_DQ<23>	
DQ24	U4	FB_A0_DQ<24>	
DQ25	U2	FB_A0_DQ<25>	
DQ26	T4	FB_A0_DQ<26>	
DQ27	T2	FB_A0_DQ<27>	
DQ28	N4	FB_A0_DQ<28>	
DQ29	N2	FB_A0_DQ<29>	
DQ30	M4	FB_A0_DQ<30>	
DQ31	M2	FB_A0_DQ<31>	
NC	A5, J5, U5	NC	FB_A0_A<8>

U8450

32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

OMIT_TABLE

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_A1_DBI_L<0>	
DBI1*	D13	FB_A1_DBI_L<1>	
DBI2*	P13	FB_A1_DBI_L<2>	
DBI3*	P2	FB_A1_DBI_L<3>	
DQ0	A4	FB_A1_DQ<0>	
DQ1	A2	FB_A1_DQ<1>	
DQ2	B4	FB_A1_DQ<2>	
DQ3	B2	FB_A1_DQ<3>	
DQ4	E4	FB_A1_DQ<4>	
DQ5	E2	FB_A1_DQ<5>	
DQ6	F4	FB_A1_DQ<6>	
DQ7	F2	FB_A1_DQ<7>	
DQ8	A11	FB_A1_DQ<8>	
DQ9	A13	FB_A1_DQ<9>	
DQ10	B11	FB_A1_DQ<10>	
DQ11	B13	FB_A1_DQ<11>	
DQ12	E11	FB_A1_DQ<12>	
DQ13	E13	FB_A1_DQ<13>	
DQ14	F11	FB_A1_DQ<14>	
DQ15	F13	FB_A1_DQ<15>	
DQ16	U11	FB_A1_DQ<16>	
DQ17	U13	FB_A1_DQ<17>	
DQ18	T11	FB_A1_DQ<18>	
DQ19	T13	FB_A1_DQ<19>	
DQ20	N11	FB_A1_DQ<20>	
DQ21	N13	FB_A1_DQ<21>	
DQ22	M11	FB_A1_DQ<22>	
DQ23	M13	FB_A1_DQ<23>	
DQ24	U4	FB_A1_DQ<24>	
DQ25	U2	FB_A1_DQ<25>	
DQ26	T4	FB_A1_DQ<26>	
DQ27	T2	FB_A1_DQ<27>	
DQ28	N4	FB_A1_DQ<28>	
DQ29	N2	FB_A1_DQ<29>	
DQ30	M4	FB_A1_DQ<30>	
DQ31	M2	FB_A1_DQ<31>	
NC	A5, J5, U5	NC	FB_A1_A<8>

U8400

32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ	C5, C10, D11, G1, G4, G11, G14	VDD
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
=PP1V35_GPU_FBVDDQ	L1, L4, L11, L14, P11, R5, R10	VDD
VSS	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	VSSQ
=PP1V35_GPU_FBVDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	VDDQ
FB_A0_VREFC	J14	VREFC
FB_A0_VREFD	A10, U10	VREFD

C8400–C8425 4.7UF 20% 6.3V X6S 0402
C8403–C8413 1UF 20% 4V CERM-X6S 0201
C8414–C8417 1UF 20% 4V CERM-X6S 0201
C8418–C8425 0.1UF 10% 6.3V X6S 0201

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

R8430 549 1% 1/20W MF 201 — PLACE NEAR=U8400 J14 8 4MM
C8431 820PF 10% 25V X7R-CERM 0201 — PLACE NEAR=U8400 J14 8 4MM
R8431 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8400 J14 8 4MM
R8434 931 1% 1/20W MF 201 — PLACE NEAR=U8400 J14 8 4MM
FB_A0_VREFC — FB_SW_LEG

PLACE CLOSE TO U8400

R8432 549 1% 1/20W MF 201 — PLACE NEAR=U8400 U10 8 4MM
C8432 820PF 10% 25V X7R-CERM 0201 — PLACE NEAR=U8400 A10 8 4MM
C8433 820PF 10% 25V X7R-CERM 0201
R8433 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8400 U10 8 4MM
R8435 931 1% 1/20W MF 201 — PLACE NEAR=U8400 U10 8 4MM
FB_A0_VREFD — FB_SW_LEG

U8450

32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ	C5, C10, D11, G1, G4, G11, G14	VDD
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10	
=PP1V35_GPU_FBVDDQ	L1, L4, L11, L14, P11, R5, R10	VDD
VSS	A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14	VSSQ
=PP1V35_GPU_FBVDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14	VDDQ
FB_A1_VREFC	J14	VREFC
FB_A1_VREFD	A10, U10	VREFD

C8450–C8475 4.7UF 20% 6.3V X6S 0402
C8456–C8463 1UF 20% 4V CERM-X6S 0201
C8468–C8475 0.1UF 10% 6.3V X6S 0201

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM

R8480 549 1% 1/20W MF 201 — PLACE NEAR=U8450 J14 8 4MM
C8481 820PF 10% 25V X7R-CERM 0201 — PLACE NEAR=U8450 J14 8 4MM
R8481 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8450 J14 8 4MM
R8484 931 1% 1/20W MF 201 — PLACE NEAR=U8450 J14 8 4MM
FB_A1_VREFC — FB_SW_LEG

PLACE_NEAR=U8450.J14:8.4MM

PLACE CLOSE TO U8450

R8482 549 1% 1/20W MF 201 — PLACE NEAR=U8450 U10 8 4MM
C8482 820PF 10% 25V X7R-CERM 0201 — PLACE NEAR=U8450 A10 8 4MM
C8483 820PF 10% 25V X7R-CERM 0201
R8483 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8450 U10 8 4MM
R8485 931 1% 1/20W MF 201 — PLACE NEAR=U8450 U10 8 4MM
FB_A1_VREFD — FB_SW_LEG

PLACE_NEAR=U8450.U10:8.4MM

SYNC_MASTER=D2_SEAN — SYNC_DATE=03/05/2012

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER: 051-9589 — SIZE: D
REVISION: 4.18.0
BRANCH:
PAGE: 84 OF 132
SHEET: 75 OF 99

Page Notes

Power aliases required by this page
=PP1V5R1V35 S0 FB VDD

Signal aliases required by this page
(NONE)

BOM options provided by this page
(NONE)

CK TERMINATION - B0

R8501 40.2 1% 1/20W MF 201 — FB_B0_CLK_P — FBB0_CK_MID — PLACE NEAR=U8500 J12 8 4MM
R8502 40.2 1% 1/20W MF 201 — FB_B0_CLK_N — PLACE NEAR=U8500 J11 8 4MM
C8590 0.01UF 10% 10V X7R-CERM 0201

CK TERMINATION - B1

R8551 40.2 1% 1/20W MF 201 — FB_B1_CLK_P — FBB1_CK_MID
R8552 40.2 1% 1/20W MF 201 — FB_B1_CLK_N — PLACE NEAR=U8550 J12 8 4MM
C8591 0.01UF 10% 10V X7R-CERM 0201 — PLACE NEAR=U8550 J11 8 4MM

R8500 120 1% 1/20W MF 201
R8504 120 1% 1/20W MF 201
R8503 120 1% 1/20W MF 201

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

OMIT_TABLE

FB_B0_A<2>	H11	BA0/A2	
FB_B0_A<5>	K10	BA1/A5	
FB_B0_A<4>	K11	BA2/A4	
FB_B0_A<3>	H10	BA3/A3	
FB_B0_A<7>	K4	A8/A7	
FB_B0_A<1>	H5	A9/A1	
FB_B0_A<0>	H4	A10/A0	
FB_B0_A<6>	K5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	G12	CS*	
FB_B0_WE_L	L12	WE*	
FB_B0_CAS_L	L3	CAS*	
FB_B0_RAS_L	G3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=0)	
FB_B0_SEN	J10	SEN	
FB_B0_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<0>	C2	EDC0	
FB_B0_EDC<1>	C13	EDC1	
FB_B0_EDC<2>	R13	EDC2	
FB_B0_EDC<3>	R2	EDC3	
FB_B0_WCLK_P<0>	D4	WCK01	
FB_B0_WCLK_N<0>	D5	WCK01*	
FB_B0_WCLK_P<1>	P4	WCK23	
FB_B0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B0_DBI_L<0>	
DBI1*	D13	FB_B0_DBI_L<1>	
DBI2*	P13	FB_B0_DBI_L<2>	
DBI3*	P2	FB_B0_DBI_L<3>	
DQ0	A4	FB_B0_DQ<0>	
DQ1	A2	FB_B0_DQ<1>	
DQ2	B4	FB_B0_DQ<2>	
DQ3	B2	FB_B0_DQ<3>	
DQ4	E4	FB_B0_DQ<4>	
DQ5	E2	FB_B0_DQ<5>	
DQ6	F4	FB_B0_DQ<6>	
DQ7	F2	FB_B0_DQ<7>	
DQ8	A11	FB_B0_DQ<8>	
DQ9	A13	FB_B0_DQ<9>	
DQ10	B11	FB_B0_DQ<10>	
DQ11	B13	FB_B0_DQ<11>	
DQ12	E11	FB_B0_DQ<12>	
DQ13	E13	FB_B0_DQ<13>	
DQ14	F11	FB_B0_DQ<14>	
DQ15	F13	FB_B0_DQ<15>	
DQ16	U11	FB_B0_DQ<16>	
DQ17	U13	FB_B0_DQ<17>	
DQ18	T11	FB_B0_DQ<18>	
DQ19	T13	FB_B0_DQ<19>	
DQ20	N11	FB_B0_DQ<20>	
DQ21	N13	FB_B0_DQ<21>	
DQ22	M11	FB_B0_DQ<22>	
DQ23	M13	FB_B0_DQ<23>	
DQ24	U4	FB_B0_DQ<24>	
DQ25	U2	FB_B0_DQ<25>	
DQ26	T4	FB_B0_DQ<26>	
DQ27	T2	FB_B0_DQ<27>	
DQ28	N4	FB_B0_DQ<28>	
DQ29	N2	FB_B0_DQ<29>	
DQ30	M4	FB_B0_DQ<30>	
DQ31	M2	FB_B0_DQ<31>	
A5	NC		
J5	NC		
U5	NC		
NC		FB_B0_A<8>	

U8500
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ	C5	VDD	
	C10		
	D11		
	G1		
	G4		
	G11		
	G14		
	L1		
	L4		
	L11		
	L14		
	P11		
	R5		
	R10		
	B1	VDDQ	
	B3		
	B12		
	B14		
	D1		
	D3		
	D12		
	D14		
	E5		
	E10		
	F1		
	F3		
	F12		
	F14		
	G2		
	G13		
	H3		
	H12		
	K3		
	K12		
	L2		
	L13		
	M1		
	M3		
	M12		
	M14		
	N5		
	N10		
	P1		
	P3		
	P12		
	P14		
	T1		
	T3		
	T12		
	T14		
FB_B0_VREFC	J14	VREFC	
FB_B0_VREFD	A10	VREFD	
	U10		

B5		
B10		
D10		
G5		
G10		
H1		
H14	VSS	
K1		
K14		
L5		
L10		
P10		
T5		
T10		
A1		
A3		
A12		
A14		
C1		
C3		
C4		
C11		
C12		
E1		
E3		
E12		
E14		
F5		
F10		
H2	VSSQ	
H13		
K2		
K13		
M5		
M10		
N1		
N3		
N12		
N14		
R1		
R3		
R4		
R11		
R12		
R14		
U1		
U3		
U12		
U14		

C8500–C8525 4.7UF 20% 6.3V X6S 0402
C8506–C8513 1UF 20% 4V CERM-X6S 0201
C8514 1UF 20% 4V CERM-X6S 0201
C8515–C8517 1UF 20% 4V CERM-X6S 0201
C8516 0.1UF 10% 6.3V X6S 0201
C8517 0.1UF 10% 6.3V X6S 0201
C8518–C8521 0.1UF 10% 6.3V X6S 0201
C8522–C8525 0.1UF 10% 6.3V X6S 0201

PLACE CLOSE TO U8500

R8530 549 1% 1/20W MF 201 — PLACE NEAR=U8500 J14 8 4MM — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 MM
FB_B0_VREFC
C8531 820PF 10% 25V X7R-CERM 0201
R8531 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8500 J14 8 4MM
R8534 931 1% 1/20W MF 201 — PLACE NEAR=U8500 J14 8 4MM
FB_SW_LEG

R8532 549 1% 1/20W MF 201 — PLACE NEAR=U8500 U10 8 4MM — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 MM
FB_B0_VREFD
C8532 820PF 10% 25V X7R-CERM 0201
R8533 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8500 U10 8 4MM
R8535 931 1% 1/20W MF 201 — PLACE NEAR=U8500 U10 8 4MM
FB_SW_LEG
PLACE NEAR=U8500 A10 8 4MM

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)

OMIT_TABLE

FB_B1_A<2>	H11	BA0/A2	
FB_B1_A<5>	K10	BA1/A5	
FB_B1_A<4>	K11	BA2/A4	
FB_B1_A<3>	H10	BA3/A3	
FB_B1_A<7>	K4	A8/A7	
FB_B1_A<1>	H5	A9/A1	
FB_B1_A<0>	H4	A10/A0	
FB_B1_A<6>	K5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	G12	CS*	
FB_B1_WE_L	L12	WE*	
FB_B1_CAS_L	L3	CAS*	
FB_B1_RAS_L	G3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=0)	
FB_B1_SEN	J10	SEN	
FB_B1_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	C2	EDC0	
FB_B1_EDC<1>	C13	EDC1	
FB_B1_EDC<2>	R13	EDC2	
FB_B1_EDC<3>	R2	EDC3	
FB_B1_WCLK_P<0>	D4	WCK01	
FB_B1_WCLK_N<0>	D5	WCK01*	
FB_B1_WCLK_P<1>	P4	WCK23	
FB_B1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B1_DBI_L<0>	
DBI1*	D13	FB_B1_DBI_L<1>	
DBI2*	P13	FB_B1_DBI_L<2>	
DBI3*	P2	FB_B1_DBI_L<3>	
DQ0	A4	FB_B1_DQ<0>	
DQ1	A2	FB_B1_DQ<1>	
DQ2	B4	FB_B1_DQ<2>	
DQ3	B2	FB_B1_DQ<3>	
DQ4	E4	FB_B1_DQ<4>	
DQ5	E2	FB_B1_DQ<5>	
DQ6	F4	FB_B1_DQ<6>	
DQ7	F2	FB_B1_DQ<7>	
DQ8	A11	FB_B1_DQ<8>	
DQ9	A13	FB_B1_DQ<9>	
DQ10	B11	FB_B1_DQ<10>	
DQ11	B13	FB_B1_DQ<11>	
DQ12	E11	FB_B1_DQ<12>	
DQ13	E13	FB_B1_DQ<13>	
DQ14	F11	FB_B1_DQ<14>	
DQ15	F13	FB_B1_DQ<15>	
DQ16	U11	FB_B1_DQ<16>	
DQ17	U13	FB_B1_DQ<17>	
DQ18	T11	FB_B1_DQ<18>	
DQ19	T13	FB_B1_DQ<19>	
DQ20	N11	FB_B1_DQ<20>	
DQ21	N13	FB_B1_DQ<21>	
DQ22	M11	FB_B1_DQ<22>	
DQ23	M13	FB_B1_DQ<23>	
DQ24	U4	FB_B1_DQ<24>	
DQ25	U2	FB_B1_DQ<25>	
DQ26	T4	FB_B1_DQ<26>	
DQ27	T2	FB_B1_DQ<27>	
DQ28	N4	FB_B1_DQ<28>	
DQ29	N2	FB_B1_DQ<29>	
DQ30	M4	FB_B1_DQ<30>	
DQ31	M2	FB_B1_DQ<31>	
A5	NC		
J5	NC		
U5	NC		
NC		FB_B1_A<8>	

U8550
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)

OMIT_TABLE

=PP1V35_GPU_FBVDDQ	C5	VDD	
	C10		
	D11		
	G1		
	G4		
	G11		
	G14		
	L1		
	L4		
	L11		
	L14		
	P11		
	R5		
	R10		
	B1	VDDQ	
	B3		
	B12		
	B14		
	D1		
	D3		
	D12		
	D14		
	E5		
	E10		
	F1		
	F3		
	F12		
	F14		
	G2		
	G13		
	H3		
	H12		
	K3		
	K12		
	L2		
	L13		
	M1		
	M3		
	M12		
	M14		
	N5		
	N10		
	P1		
	P3		
	P12		
	P14		
	T1		
	T3		
	T12		
	T14		
FB_B1_VREFC	J14	VREFC	
FB_B1_VREFD	A10	VREFD	
	U10		

B5		
B10		
D10		
G5		
G10		
H1		
H14	VSS	
K1		
K14		
L5		
L10		
P10		
T5		
T10		
A1		
A3		
A12		
A14		
C1		
C3		
C4		
C11		
C12		
E1		
E3		
E12		
E14		
F5		
F10		
H2	VSSQ	
H13		
K2		
K13		
M5		
M10		
N1		
N3		
N12		
N14		
R1		
R3		
R4		
R11		
R12		
R14		
U1		
U3		
U12		
U14		

C8550–C8555 4.7UF 20% 6.3V X6S 0402
C8556–C8563 1UF 20% 4V CERM-X6S 0201
C8564–C8567 0.1UF 10% 6.3V X6S 0201
C8568–C8575 0.1UF 10% 6.3V X6S 0201

R8550 120 1% 1/20W MF 201
R8554 120 1% 1/20W MF 201
R8553 120 1% 1/20W MF 201

PLACE CLOSE TO U8550

R8580 549 1% 1/20W MF 201 — PLACE NEAR=U8550 J14 8 4MM — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 MM
FB_B1_VREFC
C8581 820PF 10% 25V X7R-CERM 0201
R8581 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8550 J14 8 4MM
R8584 931 1% 1/20W MF 201 — PLACE NEAR=U8550 J14 8 4MM
FB_SW_LEG
PLACE NEAR=U8550 J14 8 4MM

R8582 549 1% 1/20W MF 201 — PLACE NEAR=U8550 U10 8 4MM — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 MM
FB_B1_VREFD
C8582 820PF 10% 25V X7R-CERM 0201
C8583 820PF 10% 25V X7R-CERM 0201
R8583 1.33K 1% 1/20W MF 201 — PLACE NEAR=U8550 U10 8 4MM
R8585 931 1% 1/20W MF 201 — PLACE NEAR=U8550 U10 8 4MM
FB_SW_LEG
PLACE NEAR=U8550 A10 8 4MM

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9589
	SIZE D
	REVISION 4.18.0
	BRANCH
	PAGE 85 OF 132
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PD FOR AUX CHANNELS (FOR NVIDIA)

DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q

R8614 100K 1% 1/20W MF 201
R8613 100K 1% 1/20W MF 201
R8615 100K 1% 1/20W MF 201
R8616 100K 1% 1/20W MF 201
R8617 100K 1% 1/20W MF 201
R8618 100K 1% 1/20W MF 201
R8627 100K 1% 1/20W MF 201 NO STUFF
R8628 100K 1% 1/20W MF 201 NO STUFF

=PP3V3_GPU_VDD33
R8623 4.7K 1% 1/20W MF 201
R8624 4.7K 1% 1/20W MF 201

DISABLE PHY A & B FOR 15" MBP

PP1V8_GPU_IFPA_IOVDD — R8601 10K 1% 1/20W MF 201
PP3V3_GPU_IFPB_IOVDD — R8602 10K 1% 1/20W MF 201
PP1V05_GPU_IFPAB_PLLVDD — R8603 10K 1% 1/20W MF 201
GPU_TESTMODE — R8608 10K 1% 1/20W MF 201

PD FOR RSET

IFPC_RSET — R8621 1K 1% 1/20W MF 201 PLACE NEAR=U8000 AF8 5MM
IFPD_RSET — R8606 1K 1% 1/20W MF 201 PLACE NEAR=U8000 AN2 5MM
IFPEF_RSET — R8607 1K 1% 1/20W MF 201 PLACE NEAR=U8000 AD6 5MM

Page Notes

Power aliases required by this page
PP3V3_GPU_IFPB_IOVDD
PP1V8_GPU_IFPA_IOVDD
PP1V8_GPU_DPLL
PP1V05_GPU_DPLL
PP3V3_GPU_IFPX_PLLVDD
PP1V05_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPEF_IOVDD
PP3V3_GPU_VDD33

Signal aliases required by this page
(NONE)

BOM options provided by this page
J31 YES
D2 YES

PP1V05_GPU_SP_PLLVDD = PP1V05_GPU_VID_PLLVDD (MAKE BASE=TRUE)

GPU_OSC_27M_XTAL_BUFFOUT_R — R8611 10K 1% 1/20W MF 201 PLACE NEAR=U8000 J4 8 4MM
GPU_OSC_27M_SSIN — R8612 10K 1% 1/20W MF 201 PLACE NEAR=U8000 H1 8 4MM

OMIT_TABLE
CRITICAL
U8000 NV-GK107 BGA (5 OF 10)

PP1V8_GPU_IFPA_IOVDD	AG8	IFPA_IOVDD	
PP3V3_GPU_IFPB_IOVDD	AG9	IFPB_IOVDD	
PP1V05_GPU_IFPCD_IOVDD	AF6	IFPC_IOVDD	
PP1V05_GPU_IFPCD_IOVDD	AG6	IFPD_IOVDD	
PP1V05_GPU_IFPEF_IOVDD	AC7	IFPE_IOVDD	
PP1V05_GPU_IFPEF_IOVDD	AC8	IFPF_IOVDD	
PP1V05_GPU_IFPAB_PLLVDD	AH8	IFPAB_PLLVDD	
NC	AJ8	IFPAB_RSET	
PP3V3_GPU_IFPX_PLLVDD	AF7	IFPC_PLLVDD	
IFPC_RSET	AF8	IFPC_RSET	
PP3V3_GPU_IFPX_PLLVDD	AG7	IFPD_PLLVDD	
IFPD_RSET	AN2	IFPD_RSET	
PP3V3_GPU_IFPX_PLLVDD	AB8	IFPEF_PLLVDD	
IFPEF_RSET	AD6	IFPEF_RSET	

IFPA_TXC	AM6	NC	
IFPA_TXC*	AN6	NC	
IFPA_TXD0	AP3	NC	
IFPA_TXD0*	AN3	NC	
IFPA_TXD1	AN5	NC	
IFPA_TXD1*	AM5	NC	
IFPA_TXD2	AL6	NC	
IFPA_TXD2*	AK6	NC	
IFPA_TXD3	AJ6	NC	
IFPA_TXD3*	AH6	NC	
IFPB_TXC	AJ9	NC	
IFPB_TXC*	AH9	NC	
IFPB_TXD4	AP6	NC	
IFPB_TXD4*	AP5	NC	
IFPB_TXD5	AM7	NC	
IFPB_TXD5*	AL7	NC	
IFPB_TXD6	AN8	NC	
IFPB_TXD6*	AM8	NC	
IFPB_TXD7	AK8	NC	
IFPB_TXD7*	AL8	NC	

DPA_EG_DDC_CLK — R4 — I2CA_SCL
DPA_EG_DDC_DATA — R5 — I2CA_SDA
GPU_SSC_SMB_CLK — R2 — I2CC_SCL
GPU_SSC_SMB_DAT — R3 — I2CC_SDA
GPU_SMB_CLK — T4 — I2CS_SCL
GPU_SMB_DAT — T3 — I2CS_SDA
DPB_EG_DDC_CLK — R7 — I2CB_SCL
DPB_EG_DDC_DATA — R6 — I2CB_SDA

DDC MAPPING
I2CA -> IFPE
I2CB -> IFPF
I2CC -> SSC CLK GEN

IFPC_AUX_I2CW_SCL	AG3	HDMI_EG_DDC_CLK_Q	
IFPC_AUX_I2CW_SDA*	AG2	HDMI_EG_DDC_DATA_Q	
IFPC_L0	AK1	HDMI_EG_DATA_C_P<2>	OUT
IFPC_L0*	AJ1	HDMI_EG_DATA_C_N<2>	OUT
IFPC_L1	AJ3	HDMI_EG_DATA_C_P<1>	OUT
IFPC_L1*	AJ2	HDMI_EG_DATA_C_N<1>	OUT
IFPC_L2	AH3	HDMI_EG_DATA_C_P<0>	OUT
IFPC_L2*	AH4	HDMI_EG_DATA_C_N<0>	OUT
IFPC_L3	AG5	HDMI_EG_CLK_C_P	OUT
IFPC_L3*	AG4	HDMI_EG_CLK_C_N	OUT
IFPD_AUX_I2CX_SCL	AK3	DP_INT_EG_AUX_P	BI
IFPD_AUX_I2CX_SDA*	AK2	DP_INT_EG_AUX_N	BI
IFPD_L0	AM1	DP_INT_EG_ML_P<0>	OUT
IFPD_L0*	AM2	DP_INT_EG_ML_N<0>	OUT
IFPD_L1	AM3	DP_INT_EG_ML_P<1>	OUT
IFPD_L1*	AM4	DP_INT_EG_ML_N<1>	OUT
IFPD_L2	AL3	DP_INT_EG_ML_P<2>	OUT
IFPD_L2*	AL4	DP_INT_EG_ML_N<2>	OUT
IFPD_L3	AK4	DP_INT_EG_ML_P<3>	OUT
IFPD_L3*	AK5	DP_INT_EG_ML_N<3>	OUT
IFPE_AUX_I2CY_SCL	AB3	DP_TBTSNK0_EG_AUXCH_P	BI
IFPE_AUX_I2CY_SDA*	AB4	DP_TBTSNK0_EG_AUXCH_N	BI
IFPE_L0	AD2	DP_TBTSNK0_ML_C_P<0>	OUT
IFPE_L0*	AD3	DP_TBTSNK0_ML_C_N<0>	OUT
IFPE_L1	AD1	DP_TBTSNK0_ML_C_P<1>	OUT
IFPE_L1*	AC1	DP_TBTSNK0_ML_C_N<1>	OUT
IFPE_L2	AC2	DP_TBTSNK0_ML_C_P<2>	OUT
IFPE_L2*	AC3	DP_TBTSNK0_ML_C_N<2>	OUT
IFPE_L3	AC4	DP_TBTSNK0_ML_C_P<3>	OUT
IFPE_L3*	AC5	DP_TBTSNK0_ML_C_N<3>	OUT
IFPF_AUX_I2CZ_SCL	AF3	DP_TBTSNK1_EG_AUXCH_P	BI
IFPF_AUX_I2CZ_SDA*	AF2	DP_TBTSNK1_EG_AUXCH_N	BI
IFPF_L0	AE3	DP_TBTSNK1_ML_C_P<0>	OUT
IFPF_L0*	AE4	DP_TBTSNK1_ML_C_N<0>	OUT
IFPF_L1	AF4	DP_TBTSNK1_ML_C_P<1>	OUT
IFPF_L1*	AF5	DP_TBTSNK1_ML_C_N<1>	OUT
IFPF_L2	AD4	DP_TBTSNK1_ML_C_P<2>	OUT
IFPF_L2*	AD5	DP_TBTSNK1_ML_C_N<2>	OUT
IFPF_L3	AG1	DP_TBTSNK1_ML_C_P<3>	OUT
IFPF_L3*	AF1	DP_TBTSNK1_ML_C_N<3>	OUT
DAC_AVDD	AG10	DACA_VDD	
		DACA_RED	AK9 NC
		DACA_GREEN	AL10 NC
		DACA_BLUE	AL9 NC
	AP9	DACA_VREF	NC
	AP8	DACA_RSET	NC
		DACA_HSYNC	AM9 NC
		DACA_VSYNC	AN9 NC
		CEC	L3 NC

R8600 10K 1% 1/20W MF 201

DDC 3.3V/5V LEVEL TRANSLATOR

SSM6N37FEAPE SOT563 Q8600
HDMI_EG_DDC_CLK — OUT
HDMI_EG_DDC_DATA — BI

OMIT_TABLE
U8000 NV-GK107 BGA (6 OF 10)

=PP3V3_GPU_MISC	J8		
=PP3V3_GPU_VDD33	K8	VDD33	
	L8		
	M8		
GPU_ROM_CS_L	H6	ROM_CS*	
GPU_ROM_SCLK	H4	ROM_SCLK	
GPU_ROM_SI	H5	ROM_SI	
GPU_ROM_SO	H7	ROM_SO	
MULTI_STRAP_REF	J1	MULTI_STRAP_REF0_GND	
GPU_TESTMODE	AK11	TESTMODE	
PP1V05_GPU_SP_PLLVDD	AE8	SP_PLLVDD	
PP1V05_GPU_PLLVDD	AD8	PLLVDD	
PP1V05_GPU_VID_PLLVDD	AD7	VID_PLLVDD	
GPU_OSC_27M_XTALIN	H3	XTAL_IN	
GPU_OSC_27M_XTALOUT	H2	XTAL_OUT	
GPU_OSC_27M_XTAL_BUFFOUT_R	J4	XTAL_OUTBUFF	
GPU_OSC_27M_SSIN	H1	XTAL_SSIN	
GPU_MLS_STRAP0	J2	STRAP0	
GPU_MLS_STRAP1	J7	STRAP1	
GPU_MLS_STRAP2	J6	STRAP2	
GPU_MLS_STRAP3	J5	STRAP3	
GPU_MLS_STRAP4	J3	STRAP4	

R8609 40.2K 0.1% 1/20W MF 0201 PLACE NEAR=U8000 J1 5MM

	P6	GPIO0	GPU_GPIO_0
	M3	GPIO1	GPU_GPIO_1
	L6	GPIO2	GPU_GPIO_2
	P5	GPIO3	GPU_GPIO_3
	P7	GPIO4	GPU_GPIO_4
	L7	GPIO5	GPU_GPIO_5
	M7	GPIO6	GPU_GPIO_6
	N8	GPIO7	GPU_GPIO_7
	M1	GPIO8	GPU_GPIO_8
	M2	GPIO9	GPU_GPIO_9
	L1	GPIO10	GPU_GPIO_10
	M5	GPIO11	GPU_GPIO_11
	N3	GPIO12	GPU_GPIO_12
	M4	GPIO13	GPU_GPIO_13
	N4	GPIO14	GPU_GPIO_14
	P2	GPIO15	GPU_GPIO_15
	R8	GPIO16	GPU_GPIO_16
	M6	GPIO17	GPU_GPIO_17
	R1	GPIO18	GPU_GPIO_18
	P3	GPIO19	GPU_GPIO_19
	P4	GPIO20	GPU_GPIO_20
	P1	GPIO21	GPU_GPIO_21
JTAG_TCK	AM10		GPU_JTAG_TCK (IN)
JTAG_TDI	AM11		GPU_JTAG_TDI (IN)
JTAG_TDO	AP12		GPU_JTAG_TDO (OUT)
JTAG_TMS	AP11		GPU_JTAG_TMS (IN)
JTAG_TRST*	AN11		GPU_JTAG_TRST_L (IN)
THERMDP	K3		GPU_TDIODE_P (IN)
THERMDN	K4		GPU_TDIODE_N (OUT)

CRITICAL
L8604 330 OHM 1 2A 0603
=PP3V3_GPU_IFPX_PLLVDD — PP3V3_GPU_IFPX_PLLVDD (MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 mm, VOLTAGE=3 3V)
IFPX PLLVDD
C8610 10UF 20% 10V X6S CERM 0603
C8611 1UF 10% 25V X6S CERM 0402
C8612 0.1UF 20% 16V X6S-CERM 0201
PLACE BELOW GPU NEAR DISPLAY SECTION
C8613 10UF 20% 10V X6S CERM 0603
C8619 4.7UF 10% 6.3V X6S CERM 0603
C8615 1UF 10% 25V X6S CERM 0402
C8616 1UF 10% 25V X6S CERM 0402
C8617 0.1UF 20% 16V X6S-CERM 0201
C8618 0.1UF 20% 16V X6S-CERM 0201

L8605 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_IFPCD_IOVDD — PP1V05_GPU_IFPCD_IOVDD (MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 mm, VOLTAGE=1 05V)
IFP CD IOVDD
C8625 4.7UF 20% 6.3V X6S 0402
C8626 1UF 20% 4V CERM X6S 0201
C8627 0.1UF 20% 16V X6S-CERM 0201
C8628 0.1UF 20% 16V X6S-CERM 0201
C8655 10UF 20% 4V X6S CERM 0402 1
C8656 1UF 20% 4V CERM X6S 0201
C8657 0.1UF 20% 16V X6S-CERM 0201
C8658 0.1UF 20% 16V X6S-CERM 0201

L8606 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_IFPEF_IOVDD — PP1V05_GPU_IFPEF_IOVDD (MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 mm, VOLTAGE=1 05V)
IFP EF IOVDD
C8629 10UF 20% 4V X6S CERM 0402 1
C8630 1UF 20% 4V CERM X6S 0201
C8631 0.1UF 20% 16V X6S-CERM 0201
C8632 0.1UF 20% 16V X6S-CERM 0201
C8633 4.7UF 20% 6.3V X6S 0402
C8634 4.7UF 20% 6.3V X6S 0402
C8635 1UF 20% 4V CERM X6S 0201
C8636 1UF 20% 4V CERM X6S 0201
C8637 0.1UF 20% 16V X6S-CERM 0201
C8638 0.1UF 20% 16V X6S-CERM 0201

GPU PLL VDD
L8607 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM
=PP1V05_GPU_PEX_PLLVDD — PP1V05_GPU_PLLVDD (MIN LINE WIDTH=0 41 MM, MIN NECK WIDTH=0 2 MM, VOLTAGE=1 05V)
C8651 20UF 20% 2V X6T CERM 0402
C8652 1UF 20% 4V CERM X6S 0201
C8653 0.1UF 20% 16V X6S-CERM 0201
C8654 0.1UF 20% 16V X6S-CERM 0201

GPU 3V3 VDD
=PP3V3_GPU_VDD33
C8640 10UF 20% 10V X6S CERM 0603
C8641 1UF 20% 25V X6S CERM 0402
C8642 1UF 20% 25V X6S CERM 0402
C8643 0.1UF 20% 16V X6S-CERM 0201
C8644 0.1UF 20% 16V X6S-CERM 0201
=PP3V3_GPU_MISC
C8645 4.7UF 20% 6.3V X6S 0402
C8646 4.7UF 20% 6.3V X6S 0402
C8649 0.1UF 20% 16V X6S-CERM 0201
C8650 0.1UF 20% 16V X6S-CERM 0201

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012
PAGE TITLE: KEPLER EDP/DP/GPIO
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GPIOs

77	GPU_GPIO_0	GFXIMVP_VID<4>	80
77	GPU_GPIO_1	GFXIMVP_VID<3>	80
77	GPU_GPIO_2	GFXIMVP_PSI_R_L	80
77	GPU_GPIO_3	EG_LCD_PWR_EN	78 82
77	GPU_GPIO_4	EG_BKLT_EN	78 82
77	GPU_GPIO_5	GFXIMVP_VID<1>	80
77	GPU_GPIO_6	GFXIMVP_VID<2>	80
77	GPU_GPIO_7	FB_CLAMP_TOGGLE_REQ_L	78 82
77	GPU_GPIO_8	SMC_GFX_OVERTEMP_R_L	78
77	GPU_GPIO_9	SMC_GFX_THROTTLE_R_L	78
77	GPU_GPIO_10	GPU_ALT_VREF	73
77	GPU_GPIO_11	GFXIMVP_VID<0>	80
77	GPU_GPIO_12	HDMI_EG_HPD	82
77	GPU_GPIO_13	GFXIMVP_VID<5>	80

GPIOs

77	GPU_GPIO_14	DP_EXTA_CA_DET_EG	82
77	GPU_GPIO_15	DP_EXTB_CA_DET_EG	82
77	GPU_GPIO_16	FBVDD_ALTVO	74 78
77	GPU_GPIO_17	DP_INT_EG_HPD	82
77	GPU_GPIO_18	DP_TBTSNK0_HPD_EG	82
77	GPU_GPIO_19	DP_TBTSNK1_HPD_EG	82
77	GPU_GPIO_20	NC_GPU_GPIO_20_RSVD (NO TEST TRUE)	
77	GPU_GPIO_21	NC_GPU_GPIO_21_RSVD (NO TEST TRUE)	

71 PEX_CLKREQ_L_R — R8795 0 5% 1/20W MF 201 — EG_CLKREQ_IN_L OUT 82

GPU internal Temp isolation

=PP3V3_GPU_VDD33

R8755 10K 5% 1/20W MF 201

Q8702 SSM6N37FEAPE SOT563

77 BI GPU_SMB_DAT — GPU_SMB_DAT_R BI 44

R8780 0 5% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33

R8754 10K 5% 1/20W MF 201

Q8702 SSM6N37FEAPE SOT563

77 OUT GPU_SMB_CLK — GPU_SMB_CLK_R IN 44

R8781 0 5% 1/20W MF 201 NOSTUFF

Unused signals

	TP_GPU_JTAG_TCK	GPU_JTAG_TCK	77
	TP_GPU_JTAG_TDI	GPU_JTAG_TDI	77
	TP_GPU_JTAG_TDO	GPU_JTAG_TDO	77
		GPU_JTAG_TMS	77
		GPU_JTAG_TRST_L	77

Note: PU to non GPU S0 3v3 source

82 35 8 =PP3V3_S0_DPMUX_UC — R8753 10K 5% 1/20W MF 201 NOSTUFF GC6 SUPPORT

82 78 FB_CLAMP_TOGGLE_REQ_L

R8751 10K 5% 1/20W MF 201 NOSTUFF

R8758 10K 5% 1/20W MF 201 NOSTUFF

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0013	1	RES 10KOHM 0201	R8711		FB 2G SAMSUNG
118S0414	1	RES 5 1KOHM 0201	R8711		FB 2G HYNIX M DIE
118S0230	1	RES MF 24 9KOHM 1 1/20W 0201	R8711		FB 2G HYNIX A DIE

Die Rev	Strap
D-DIE	0x1
M-DIE	0x0
A-DIE	0x4

Straps for GK107. GF108 support has been removed.

CONFIG STRAPS - MLPS

=PP3V3_GPU_VDD33

R8700 45.3K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP0

R8701 5.62K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33

NOSTUFF R8708 3.24K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP4

R8709 45.3K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

NOSTUFF R8702 3.24K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP1

R8703 45.3K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

NOSTUFF R8710 3.24K 1% 1/20W MF 201

OUT 77 78 GPU_ROM_SI

R8711 25.5K 1% 1/20W MF 201 OMIT_TABLE

=PP3V3_GPU_VDD33

NOSTUFF R8704 15K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP2

R8705 30K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

R8712 10K 1% 1/20W MF 201

OUT 77 78 GPU_ROM_SO

NOSTUFF R8713 10K 1% 1/20W MF 201

=PP3V3_GPU_VDD33

R8706 20K 1% 1/20W MF 201

OUT 77 GPU_MLS_STRAP3

R8707 5.62K 1% 1/20W MF 201 NOSTUFF

=PP3V3_GPU_VDD33

R8714 24.9K 1% 1/20W MF 201

OUT 77 78 GPU_ROM_SCLK

NOSTUFF R8715 34.8K 1% 1/20W MF 201

GPU GC6 ROM

=PP3V3_GPU_VDD33

GPU_ROM_SI — R8723 33 5% 1/20W MF 201 — GPU_ROM_SI_R

GPU_ROM_SO — R8726 33 5% 1/20W MF 201 — GPU_ROM_SO_R

U8701 1MBIT USON MX25L1005CMI-12G CRITICAL

OMIT_TABLE 8 VCC

GPU_ROM_SI_R 5 SI — SCLK 6 — GPU_ROM_SCLK_R

GPU_ROM_SO_R 2 SO — CS* 1 — GPU_ROM_CS_L_R

WP* 3 — GPU_ROM_WP_L

HOLD* 7

THRM PAD 9 — GND 4

R8720 10K 5% 1/20W MF 201 GPU_ROM:YES

R8721 0 5% 1/20W MF 201 GPU_ROM:YES

C8721 0.1UF 10% 6.3V X6S 0201 GPU_ROM:YES

R8724 33 5% 1/20W MF 201 GPU_ROM_SCLK

R8725 33 5% 1/20W MF 201 GPU_ROM_CS_L

NO STUFF R8722 0 5% 1/20W MF 201

STRAP NOTES:

CURRENTLY STUFFED FOR GF108a/GK107-GTX

STUFF R8704 FOR THICK DIE

STUFF R8705 FOR THIN DIE

GPU overtemp masking

=PP3V3_GPU_VDD33

=PP3V3_S5_SMC

=PP3V3_GPU_VDD33

R8756 0 5% 1/20W MF 201

NOSTUFF R8757 0 5% 1/20W MF 201

R8752 10K 5% 1/20W MF 201

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.1 MM

PP3V3_GPU_OVERTEMP

U8702 74LVC1G08 SOT891

SMC_GFX_OVERTEMP_Q

Q8701 SSM3K15FV SOD-VESM-HF

SMC_GFX_OVERTEMP OUT 78 41 42

NC

78 SMC_GFX_OVERTEMP_R_L

GPU_RESET_L IN

GPU XTAL 27 MHZ

CRITICAL Y8700 2.50X2.000M-SM 27MHZ 30PPM 18PF 60OHM

GPU_OSC_27M_XTALIN OUT 77 95

GPU_OSC_27M_XTALOUT IN 77 95

C8700 18PF 5% 25V NPO C0G CERM 0201 NCX

C8701 18PF 5% 25V NPO C0G CERM 0201 NCX

=PP3V3_GPU_VDD33

R8796 10K 5% 1/20W MF 201

R8797 10K 5% 1/20W MF 201

78 SMC_GFX_OVERTEMP_R_L — R8798 0 NO STUFF 5% 1/20W MF 201 — SMC_GFX_OVERTEMP OUT 41 42 78

78 SMC_GFX_THROTTLE_R_L — R8799 0 5% 1/20W MF 201 — SMC_GFX_THROTTLE_L BI 41

EG_LCD_PWR_EN OUT 78 82

EG_BKLT_EN OUT 78 82

FBVDD_ALTVO OUT 74 78

R8792 10K 5% 1/20W MF 201

R8793 10K 5% 1/20W MF 201

R8794 10K 5% 1/20W MF 201

NO STUFF R8790 10K 5% 1/20W MF 201

NOSTUFF R8791 10K 5% 1/20W MF 201

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: KEPLER GPIOS,CLK & STRAPS

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Page Notes

Power aliases required by this page

PP3V3 GPU VDD33
PP1V05 GPU PEX IOVDD
PP1V05 GPU PEX PLLVDD

Signal aliases required by this page

(NONE)

BOM options provided by this page

(NONE)

GPU SP PLLVDD

=PP1V05 GPU PEX PLLVDD → L8804 FERR-220-OHM-2A (0603, CRITICAL, ESR = 0.050OHM) → PP1V05 GPU SP_PLLVDD

MIN LINE WIDTH=0 6 MM
MIN NECK WIDTH=0 25 MM
VOLTAGE=1 05V

C8830 20UF 20% 2V X6T CERM 0402
C8831 4.7UF 20% 6 3V X6S 0402
C8832 1UF 20% 4V CERM X6S 0201
C8833 1UF 20% 4V CERM X6S 0201
C8834 0.1UF 20% 10V X6S-CERM 0201
C8835 0.1UF 20% 10V X6S-CERM 0201
C8836 0.1UF 20% 10V X6S-CERM 0201
C8837 0.1UF 20% 10V X6S-CERM 0201

XW8801 SM

MIN LINE WIDTH=0 3 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=0V

GND_GPU_SP_PLLVDD

U8000 NV-GK107 BGA (2 OF 10)

OMIT_TABLE

NC	P8	PEX_IOVDD	AG19
NC	AC6	PEX_IOVDD	AG21
NC	AJ28	PEX_IOVDD	AG22
NC	AJ4	PEX_IOVDD	AG24
NC	AJ5	PEX_IOVDD	AH21
NC	AL11	PEX_IOVDD	AH25
NC	C15		
NC	D19		
NC	D20	PEX_IOVDDQ	AG13
NC	D23	PEX_IOVDDQ	AG15
NC	D26	PEX_IOVDDQ	AG16
NC	H31	PEX_IOVDDQ	AG18
NC	T8	PEX_IOVDDQ	AG25
NC	V32	PEX_IOVDDQ	AH15
		PEX_IOVDDQ	AH18
		PEX_IOVDDQ	AH26
		PEX_IOVDDQ	AH27
		PEX_IOVDDQ	AJ27
		PEX_IOVDDQ	AK27
		PEX_IOVDDQ	AL27
		PEX_IOVDDQ	AM28
		PEX_IOVDDQ	AN28
	C16	GND_OPT	
	W32	GND_OPT	
	L4	VDD_SENSE	
	L5	GND_SENSE	
GPU_BUFRSTN	L2	BUFRST*	
		PEX_PLLVDD	AG26
		PEX_PLL_HVDD	AH12

=PP1V05_GPU_PEX_IOVDD (8 73 79)

=PPVCORE_GPU (72 8)

R8810 100 5% 1/20W MF 201

GPUVCORE_SENSE_P (97 80 OUT)

GPUVCORE_SENSE_N (97 80 OUT)

R8811 100 5% 1/20W MF 201

R8800 10K 1% 1/20W MF 201

PEX_PLLVDD

MIN LINE WIDTH=0 6 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=1 05V

PP1V05_GPU_PEX_PLLVDD → R8803 0 5% 1/10W MF-LF 603 → =PP1V05_GPU_PEX_PLLVDD (8 77 79)

C8826 4.7UF 20% 6 3V X6S 0402
C8827 4.7UF 20% 6 3V X6S 0402
C8828 1UF 20% 4V CERM X6S 0201
C8829 0.1UF 10% 6 3V X6S 0201

XW8802 SM

GND_GPU_PEX_PLLVDD

MIN LINE WIDTH=0 3 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=0V

PEX_PLL_HVDD

MIN LINE WIDTH=0 8 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=3 3V

PP3V3_GPU_PEX_PLL_HVDD → R8802 0 5% 1/16W MF-LF 402 → =PP3V3 GPU VDD33 (8 71 77 78)

C8822 4.7UF 20% 6 3V X6S 0402
C8823 4.7UF 20% 6 3V X6S 0402
C8824 1UF 20% 4V CERM X6S 0201
C8825 0.1UF 10% 6 3V X6S 0201

XW8803 SM

GND_GPU_PEX_PLL_HVDD

MIN LINE WIDTH=0 3 MM
MIN NECK WIDTH=0 2 MM
VOLTAGE=0V

PEX IOVDD & PEX IOVDDQ

PLACE XW8800 & XW8804 CLOSE TO C8803

XW8804 SM
P1V05_GPU_PEX_IOVDD_SNS_P (OUT 74 97)
PLACE NEAR=C8803 1 2MM

=PP1V05_GPU_PEX_IOVDD (79 73 8)

C8803 20UF 20% 2V X6T CERM 0402
C8804 20UF 20% 2V X6T CERM 0402
C8805 4.7UF 20% 6 3V X6S 0402

XW8800 SM
P1V05_GPU_PEX_IOVDD_SNS_N (OUT 74 97)
PLACE NEAR=C8803 2 2MM

EDP = 2000 MA

C8800 20UF 20% 2V X6T CERM 0402
C8801 20UF 20% 2V X6T CERM 0402
C8802 4.7UF 20% 6 3V X6S 0402

C8815 10UF 20% 4V X6S CERM 0402 1
C8816 1UF 20% 4V CERM X6S 0201
C8817 0.1UF 10% 6 3V X6S 0201
C8818 100PF 5% 25V NP0 CERM 0201

C8812 10UF 20% 4V X6S CERM 0402 1
C8813 1UF 20% 4V CERM X6S 0201
C8814 0.1UF 10% 6 3V X6S 0201
C8821 100PF 5% 25V NP0 CERM 0201

C8809 10UF 20% 4V X6S CERM 0402 1
C8810 1UF 20% 4V CERM X6S 0201
C8811 0.1UF 10% 6 3V X6S 0201
C8819 100PF 5% 25V NP0 CERM 0201

C8806 10UF 20% 4V X6S CERM 0402 1
C8807 1UF 20% 4V CERM X6S 0201
C8808 0.1UF 10% 6 3V X6S 0201
C8820 100PF 5% 25V NP0 CERM 0201

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OMIT_TABLE

GND

AG11	AK7
A2	AL12
A33	AL14
AA13	AL15
AA15	AL17
AA17	AL18
AA18	AL2
AA20	AL20
AA22	AL21
AB12	AL23
AB14	AL24
AB16	AL26
AB19	AL28
AB2	AL30
AB21	AL32
AB23	AL33
AB28	AL5
AB30	AM13
AB32	AM16
AB5	AM19
AB7	AM22
AC13	AM25
AC15	AN1
AC17	AN10
AC18	AN13
AC20	AN16
AC22	AN19
AE2	AN22
AE28	AN25
AE30	AN30
AE32	AN34
AE33	AN4
AE5	AN7
AE7	AP2
AH10	AP33
AH13	B1
AH16	B10
AH19	B22
AH2	B25
AH22	B28
AH24	B31
AH28	B34
AH29	B4
AH30	B7
AH32	C10
AH33	C13
AH5	C19
AH7	C22
AJ7	C25
AK10	C28

U8000 NV-GK107 BGA (9 OF 10)

OMIT_TABLE

GND

C7	N7
D2	P13
D31	P15
D33	P17
E10	P18
E22	P20
E25	P22
E5	R12
E7	R14
F28	R16
F7	R19
G10	R21
G13	R23
G16	T13
G19	T15
G2	T17
G22	T18
G25	T2
G28	T20
G3	T22
G30	T28
G32	T32
G33	T5
G5	T7
G7	U12
K2	U14
K28	U16
K30	U19
K32	U21
K33	U23
K5	V12
K7	V14
M13	V16
M15	V19
M17	V21
M18	V23
M20	W13
M22	W15
N12	W17
N14	W18
N16	W20
N19	W22
N2	W28
N21	Y12
N23	Y14
N28	Y16
N30	Y19
N32	Y21
N33	Y23
N5	AH11

SYNC_MASTER=D2_SEAN
SYNC_DATE=03/05/2012

PAGE TITLE: KEPLER PEX PWR/GNDS

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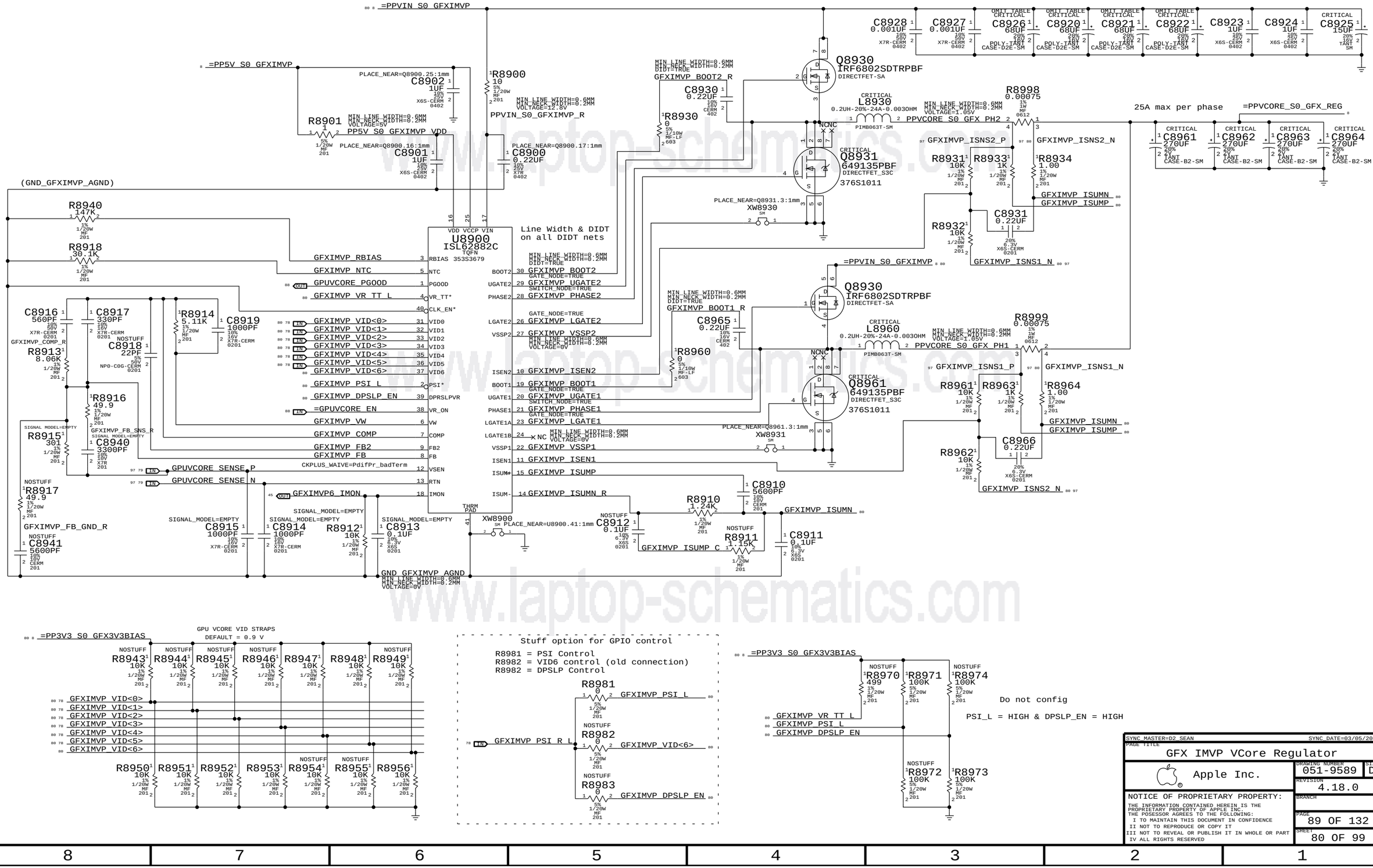

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: GFX IMVP VCore Regulator

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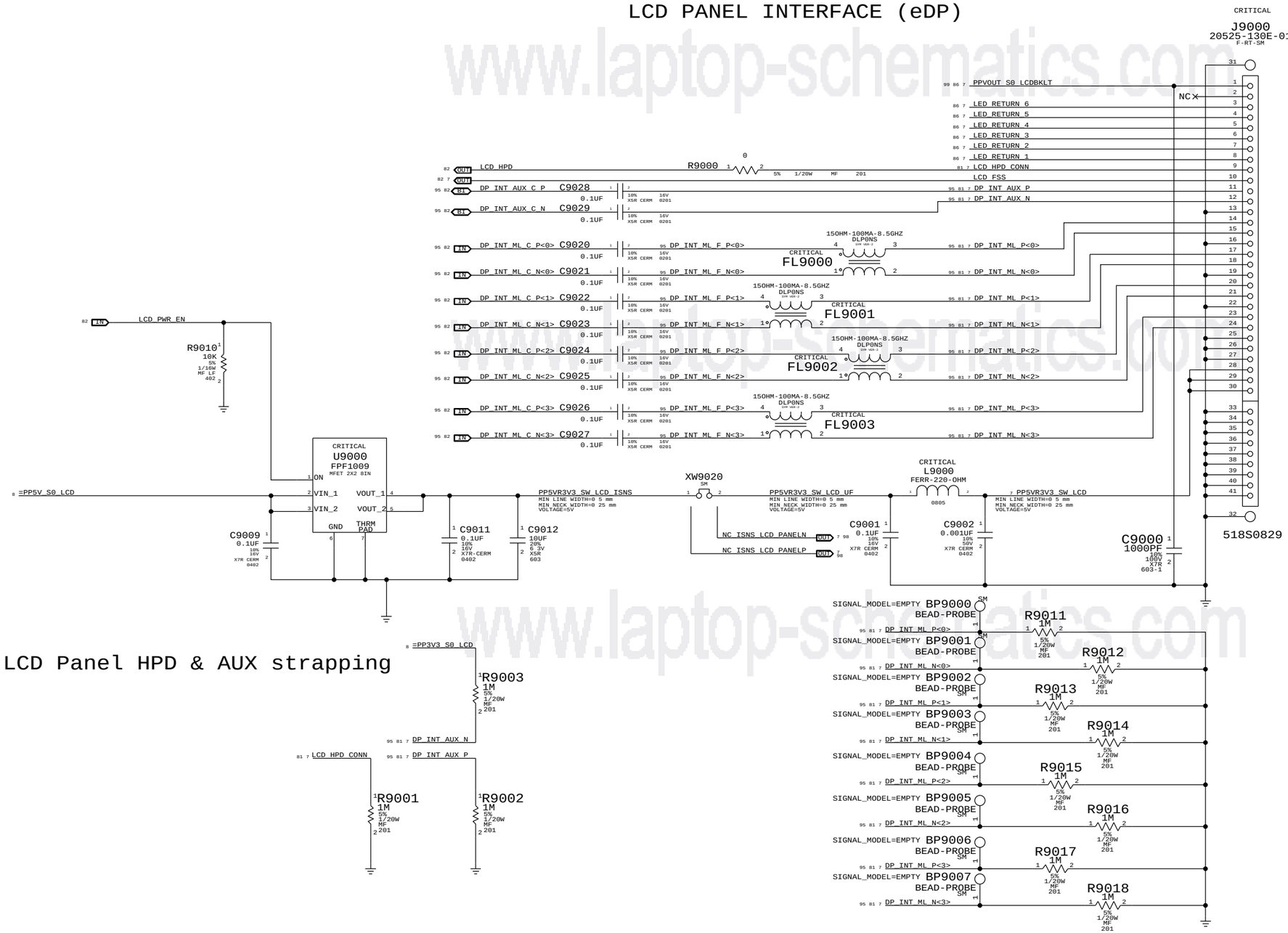
LCD PANEL INTERFACE (eDP)



LCD Panel HPD & AUX strapping

SYNC_MASTER=D2_KEPLER
SYNC_DATE=01/13/2012

PAGE TITLE: eDP Display Connector

Apple Inc.

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OMIT_TABLE

TP_DPMUX_UC_P10	B12	P10/WUE0*	
TP_DPMUX_UC_P11	A13	P11/WUE1*	
TP_DPMUX_UC_P12	A12	P12/WUE2*	
TP_DPMUX_UC_P13	B13	P13/WUE3*	
TP_DPMUX_UC_P14	D11	P14/WUE4*	
TP_DPMUX_UC_P15	C13	P15/WUE5*	
TP_DPMUX_UC_P16	C12	P16/WUE6*	
TP_DPMUX_UC_P17	D10	P17/WUE7*	
EG_RAIL1_EN	D13	P20	
EG_RAIL2_EN	E11	P21	
EG_RAIL3_EN	D12	P22	
EG_RAIL4_EN	F11	P23	
EG_RAIL5_EN	E13	P24	
EG_CLKREQ_OUT_L	E12	P25	
EG_RESET_L	F13	P26	
FB_CLAMP	E10	P27	
LPC_AD<0>	A9	P30/LAD0	
LPC_AD<1>	D9	P31/LAD1	
LPC_AD<2>	C8	P32/LAD2	
LPC_AD<3>	B7	P33/LAD3	
LPC_FRAME_L	A8	P34/LFRAM*	
DPMUX_LRESET_L	D8	P35/LRESET*	
LPC_CLK33M_DPMUX_UC	D7	P36/LCLK	
TP_DPMUX_UC_P37	D6	P37/SERIRQ	
TP_DPMUX_UC_P40	D4	P40/TMI0/TCMCYI0	
TP_DPMUX_UC_P41	A5	P41/TMO0/TCMCKI0/TCMMCI0	
TP_DPMUX_UC_P42	B4	P42/TCMCYI1	
LCD_FSS	A1	P43/TMI1/TCMCKI1/TCMMCI1	
LCD_MUX_SEL	C2	P44/TMO1/PWMU2B/TCMCYI2	
TP_DPMUX_UC_P45	B2	P45/PWMU3B/TCMCKI2/TCMMCI2	
TP_DPMUX_UC_P46	C1	P46/PWMU4B	
TP_DPMUX_UC_P47	C3	P47/PWMU5B	
DPMUX_UC_TX	G2	P50/FTXD	
DPMUX_UC_RX	F3	P51/FRXD	
TP_DPMUX_UC_P52	E4	P52/SCL0	
P60/KIN0*	L13	DP_EXTA_MUX_EN	OUT
P61/KIN1*	K12	DP_EXTA_MUX_SEL_EG	OUT
P62/KIN2*	K11	TP_DPMUX_UC_P62	
P63/KIN3*	J12	TP_DPMUX_UC_P63	
P64/KIN4*	K13	DP_EXTB_MUX_EN	OUT
P65/KIN5*	J10	DP_EXTB_MUX_SEL_EG	OUT
P66/KIN6*	J11	TP_DPMUX_UC_P66	
P67/IRQ7*/KIN7*	H12	TP_DPMUX_UC_P67	
P70/AN0	N10	DPMUX_UC_UNUSED	
P71/AN1	M11	DPMUX_UC_UNUSED	
P72/AN2	L10	DPMUX_UC_UNUSED	
P73/AN3	N11	DPMUX_UC_UNUSED	
P74/AN4	N12	DPMUX_UC_UNUSED	
P75/AN5	M13	DPMUX_UC_UNUSED	
P76/AN6	N13	DPMUX_UC_UNUSED	
P77/AN7	L12	DPMUX_UC_UNUSED	
P80/PME*	A7	TP_DPMUX_UC_P80	
P81/GA20	B6	TP_DPMUX_UC_P81	
P82/CLKRUN*	C7	TP_DPMUX_UC_P82	
P83/LPCPD*	D5	TP_DPMUX_UC_P83	
P84/IRQ3*/TXD1	A6	DPMUX_UC_BOOT_TX	OUT
P85/IRQ4*/RXD1	B5	DPMUX_UC_BOOT_RX	IN
P86/IRQ5*/SCK1	C6	TP_LCD_IRQ	
P90/IRQ2*	J4	DP_TBTPA_HPD_BUF	IN
P91/IRQ1*	G3	DP_TBTPB_HPD_BUF	IN
P92/IRQ0*	H2	DP_TBTSNK0_HPD	IN
P93/IRQ12*	G1	DP_TBTSNK1_HPD	IN
P94/IRQ13*	H4	DP_A_CA_DET_BUF	IN
P95/IRQ14*	G4	DP_B_CA_DET_BUF	IN
P96/EXCL	F4	TP_DPMUX_UC_P96	
P97/SDA0/IRQ15*	F1	TBT_DDC_XBAR_EN_L	IN

U9100 R4F2113NLG TLP-145V SYM 2 OF 3

OMIT_TABLE

PA0/KIN8*/SDA1	N3	=I2C_DPMUX_UC_SDA	BI
PA1/KIN9*/SCL1	N1	=I2C_DPMUX_UC_SCL	BI
PA2/KIN10*/PS2AC	M3	DPMUX_UC_IRQ	OUT
PA3/KIN11*/PS2AD	M2	DPMUX_UC_UNUSED	
PA4/KIN12*/PS2BC	N2	DPMUX_UC_UNUSED	
PA5/KIN13*/PS2BD	L1	DPMUX_UC_UNUSED	
PA6/KIN14*/PS2CC	K3	DPMUX_UC_UNUSED	
PA7/KIN15*/PS2CD	L2	FB_CLAMP_TOGGLE_REQ_L	
PB0/LSMI*	B8	TP_DPA_EG_HPD	
PB1/LSCI	C9	TP_DPB_EG_HPD	
PB2/RI*/PWMU0B	B9	DP_TBTSNK0_HPD_EG	OUT
PB3/DCD*/PWMU1B	A10	DP_TBTSNK1_HPD_EG	OUT
PB4/DSR*/FSIDO	C10	DP_EXTA_CA_DET_EG	OUT
PB5/DTR*/FSIDI	B10	DP_EXTB_CA_DET_EG	OUT
PB6/CTS*/FSICK	C11	HDMI_EG_HPD	OUT
PB7/RTS*/FSISS	A11	DP_INT_EG_HPD	OUT
PC0/TIOCA0/WUE8*	G11	LCD_PWR_EN	OUT
PC1/TIOCB0/WUE9*	G13	LCD_BKLT_EN	OUT
PC2/TIOCC0/TCLKA/WUE10*	F12	TP_DPMUX_UC_PC2	
PC3/TIOCD0/TCLKB/WUE11*	H13	TP_DPMUX_UC_PC3	
PC4/TIOCA1/WUE12*	G10	LCD_MUX_EN	
PC5/TIOCB1/TCLKC/WUE13*	G12	TP_LCD_MUX_REQ	
PC6/TIOCA2/WUE14*	H11	LCD_BKLT_PWM	OUT
PC7/TIOCB2/TCLKD/WUE15*	J13	DP_DDC_MUX_CROSSBAR_L	OUT
PD0/AN8	M10	TP_DPA_IG_HPD	
PD1/AN9	N9	TP_DPB_IG_HPD	
PD2/AN10	K10	DP_TBTSNK0_HPD_IG	OUT
PD3/AN11	L8	DP_TBTSNK1_HPD_IG	OUT
PD4/SSO	M9	TP_DP_EXTA_CA_DET_IG	
PD5/SSI	N8	TP_DP_EXTB_CA_DET_IG	
PD6/SSCK	K9	TP_HDMI_IG_HPD	
PD7/SCS	L7	DP_INT_IG_HPD	OUT
PE0/EXEXCL	K1	DPMUX_UC_CLK32K	
PE1/ETCK	J3	DPMUX_UC_TCK	
PE2/ETDI	K2	DPMUX_UC_TDI	
PE3/ETDO	J1	DPMUX_UC_TDO	
PE4/ETMS	K4	DPMUX_UC_TMS	
PE5/ETRST*	H3	DPMUX_UC_TRST_L	
PF0/IRQ8*/PWMU0A	K5	EG_LCD_PWR_EN	IN
PF1/IRQ9*/PWMU1A	N5	EG_BKLT_EN	IN
PF2/IRQ10*/TMOY	M6	PM_ALL_GPU_PGOOD	IN
PF3/IRQ11*/TMOX	L5	EG_CLKREQ_IN_L	IN
PF4/PWMU2A/EXDSR	M5	GPU_PGOOD4	IN
PF5/PWMU3A/EXDTR	N4	GPU_PGOOD3	IN
PF6/PWMU4A/EXCTS	L4	GPU_PGOOD2	IN
PF7/PWMU5A/EXRTS	M4	GPU_PGOOD1	IN
PG0/EXIRQ8*/TMIX/SDAA	M8	=I2C_DPMUX_A_SDA	BI
PG1/EXIRQ9*/TMIY/SCLA	N7	=I2C_DPMUX_A_SCL	OUT
PG2/EXIRQ10*/SDAB	K8	DPMUX_UC_UNUSED	
PG3/EXIRQ11*/SCLB	K7	DPMUX_UC_UNUSED	
PG4/EXIRQ12*/SDAC	K6	DPMUX_UC_UNUSED	
PG5/EXIRQ13*/SCLC	N6	DPMUX_LRESET_L	IN
PG6/EXIRQ14*/SDAD	M7	HDMI_HPD_BUF	IN
PG7/EXIRQ15*/SCLD	L6	LCD_HPD	IN
PH0/IRQ6*	E2	IG_LCD_PWR_EN	IN
PH1/EXIRQ7*	F2	IG_BKLT_EN	IN
PECI	A4	DPMUX_UC_PECI	
PEVREF	B3	DPMUX_UC_PEVREF	

CONNECT I2C TO LCD BKLT IC

J9100 1909782 M-RT-SM

DPMUX_DEBUG

DPMUX UC DEBUG HEADER

PP3V3_S0_DPMUX_UC_R	1
DPMUX_UC_TX	2
DPMUX_UC_RX	3
DPMUX_UC_RESET_L	4
DPMUX_UC_MD1	5
	6
	7
	8

Q9190 SSM3K15FV SOD-VESM-HF

DPMUX_UC_MD2 — D; DPMUX_UC_MD1 — G; S

R9101 0 5% 1/16W MF LF 402

=PP3V3_S3_DPMUX_UC → PP3V3_S3_DPMUX_UC_R
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

R9100 0 5% 1/16W MF LF 402

=PP3V3_S0_DPMUX_UC → PP3V3_S0_DPMUX_UC_R
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

C9100 0.1UF 20% 10V X7R CERM 0402
C9101 0.1UF 20% 10V X7R CERM 0402
C9102 0.1UF 20% 10V X7R CERM 0402
C9103 0.1UF 20% 10V X7R CERM 0402
C9104 0.1UF 20% 10V X7R CERM 0402

R9102 0 NOSTUFF 5% 1/16W MF LF 402

DPMUX_UC_RESET_L → DPMUX_LRESET_L

DPMUX_UC_VCL

C9105 0.47UF 10% 6.3V X6S CERM 0402

U9100 R4F2113NLG TLP-145V SYM 3 OF 3

OMIT_TABLE

AVCC	M12		
VCC	B1		
VCC	M1		
VCC	H10		
VCL	E1		
VCL	L11		
AVREF	J2		
VBAT			
RES*	D3		
XTAL	A3	DPMUX_UC_XTAL	
EXTAL	A2	DPMUX_UC_EXTAL	
MDCKN	C4		
MD1	D1	DPMUX_UC_MD1	
MD2	H1	DPMUX_UC_MD2	
NMI	E3	DPMUX_UC_NMI	
NC	E5	NC	
VSS	D2		
VSS	L3		
VSS	F10		
VSS	C5		
VSS	B11		
AVSS	L9		

R9151 0 5% 1/20W MF 201

DPMUX:XTAL

Y9100 2.5X2.0MM-SM

20MHZ 30PPM 12PF 50OHM

DPMUX:XTAL_R

C9140 15PF 5% 25V NPO 0201

DPMUX:XTAL — NC

C9141 15PF 5% 25V NPO 0201

DPMUX:XTAL — NC

R9150 10K 5% 1/20W MF 201

DPMUX:HOCO

DPMUX UC PULL-UPS

=PP3V3_S0_DPMUX_UC

DPMUX_UC_NMI	R9110	10K	5% 1/20W MF 201
DPMUX_UC_TRST_L	R9111	10K	5% 1/20W MF 201
DPMUX_UC_MD1	R9112	10K	5% 1/20W MF 201
DPMUX_UC_MD2	R9113	10K	5% 1/20W MF 201
DPMUX_UC_CLK32K	R9114	10K	5% 1/20W MF 201
DPMUX_UC_TCK	R9115	10K	5% 1/20W MF 201
DPMUX_UC_TDI	R9116	10K	5% 1/20W MF 201
DPMUX_UC_TDO	R9117	10K	5% 1/20W MF 201
DPMUX_UC_TMS	R9118	10K	5% 1/20W MF 201
EG_CLKREQ_OUT_L	R9119	100K	NOSTUFF PU on PCH Page
DPMUX_UC_RESET_L	R9140	100K	5% 1/20W MF 201

HDMI HPD INVERSION & ISOLATION

=PP3V3_S0_DPMUX_UC

HDMI_HPD_L → U9110 (74LVC1G00GF SOT891) → HDMI_HPD_BUF

NC

CA_DET ISOLATION

=PP3V3_S0_DPMUX_UC

Q9110 SSM6N37FEAPE SOT563

R9160 100K 5% 1/20W MF 201

TBT_A_CONFIG1_BUF → DP_A_CA_DET_BUF

R9161 100K 5% 1/20W MF 201

TBT_B_CONFIG1_BUF → DP_B_CA_DET_BUF

DP 2:1 ANALOG MUX

=PP3V3_S0_DPMUX

C9150 0.1UF 20% 10V X7R CERM 0402
C9151 0.1UF 20% 10V X7R CERM 0402

U9150 CBTL06142EEE TFBGA CRITICAL

DP_INT_IG_ML_P<0>	B4	DIN1_0+	
DP_INT_IG_ML_N<0>	A4	DIN1_0-	
DP_INT_IG_ML_P<1>	B5	DIN1_1+	
DP_INT_IG_ML_N<1>	A5	DIN1_1-	
DP_INT_IG_ML_P<2>	B6	DIN1_2+	
DP_INT_IG_ML_N<2>	A6	DIN1_2-	
DP_INT_IG_ML_P<3>	A8	DIN1_3+	
DP_INT_IG_ML_N<3>	A9	DIN1_3-	
DP_INT_IG_AUX_P	H9	DAUX1+	
DP_INT_IG_AUX_N	J9	DAUX1-	
NC	H8	DDC_CLK1	
NC	J8	DDC_DAT1	
NC	J2	HPD_1	
DP_INT_EG_ML_P<0>	B8	DIN2_0+	
DP_INT_EG_ML_N<0>	B9	DIN2_0-	
DP_INT_EG_ML_P<1>	D8	DIN2_1+	
DP_INT_EG_ML_N<1>	D9	DIN2_1-	
DP_INT_EG_ML_P<2>	E8	DIN2_2+	
DP_INT_EG_ML_N<2>	E9	DIN2_2-	
DP_INT_EG_ML_P<3>	F8	DIN2_3+	
DP_INT_EG_ML_N<3>	F9	DIN2_3-	
DP_INT_EG_AUX_P	H6	DAUX2+	
DP_INT_EG_AUX_N	J6	DAUX2-	
NC	H5	DDC_CLK2	
NC	J5	DDC_DAT2	
NC	H3	HPD_2	
LCD_MUX_SEL	A1	GPU_SEL	
LCD_MUX_EN	B7	XSD*	
		DDC_AUX_SEL	C2
		DOUT_0+	B2
		DOUT_0-	B1
		DOUT_1+	D2
		DOUT_1-	D1
		DOUT_2+	E2
		DOUT_2-	E1
		DOUT_3+	F2
		DOUT_3-	F1
		AUX+	H2
		AUX-	H1
		HPDIN	J1
		VDD	A2, J4
		GND	B3, C8, G8, H4, H7, G2

DP_INT_ML_C_P<0> → DP_INT_ML_C_N<0> → DOUT
DP_INT_ML_C_P<1> → DP_INT_ML_C_N<1> → DOUT
DP_INT_ML_C_P<2> → DP_INT_ML_C_N<2> → DOUT
DP_INT_ML_C_P<3> → DP_INT_ML_C_N<3> → DOUT
DP_INT_AUX_C_P → DP_INT_AUX_C_N → BI

R9162 100K 1% 1/20W MF 201

DPMUX_HPD_PD

DPMUX UC PULL-DOWNS

DPMUX_UC_RESET_L	R9120	10K	NOSTUFF
EG_RAIL1_EN	R9121	10K	
EG_RAIL2_EN	R9122	10K	
EG_RAIL3_EN	R9123	10K	
EG_RAIL4_EN	R9124	10K	
EG_RAIL5_EN	R9125	10K	
LCD_PWR_EN	R9126	10K	NOSTUFF PD on LCD Page
LCD_BKLT_EN	R9127	10K	
LCD_BKLT_PWM	R9128	10K	
DPMUX_UC_NMI	R9129	10K	NOSTUFF
DPMUX_UC_MD1	R9130	10K	NOSTUFF
DPMUX_UC_MD2	R9131	10K	NOSTUFF
DPMUX_UC_PECI	R9132	10K	
DPMUX_UC_PEVREF	R9133	10K	
DPMUX_UC_UNUSED	R9134	10K	
EG_RESET_L	R9135	100K	
DPA_IG_HPD	R9136	100K	
DP_TBTSNK0_HPD_EG	R9137	100K	
DPB_IG_HPD	R9138	100K	
DP_TBTSNK1_HPD_EG	R9139	100K	
DP_INT_IG_HPD	R9145	100K	
DP_INT_EG_HPD	R9146	100K	

All: 5% 1/20W MF 201

SYNC_MASTER=D2_SEAN	SYNC_DATE=03/05/2012
PAGE TITLE	eDP Mux
Apple Inc.	DRAWING NUMBER 051-9589 · SIZE D
	REVISION 4.18.0
	BRANCH
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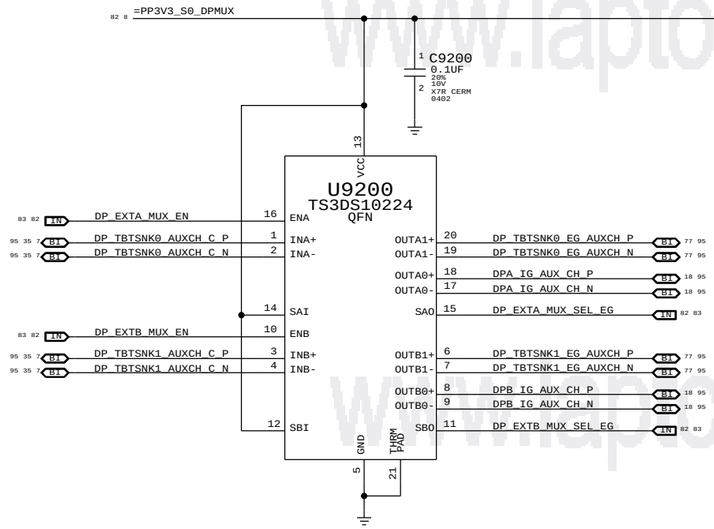
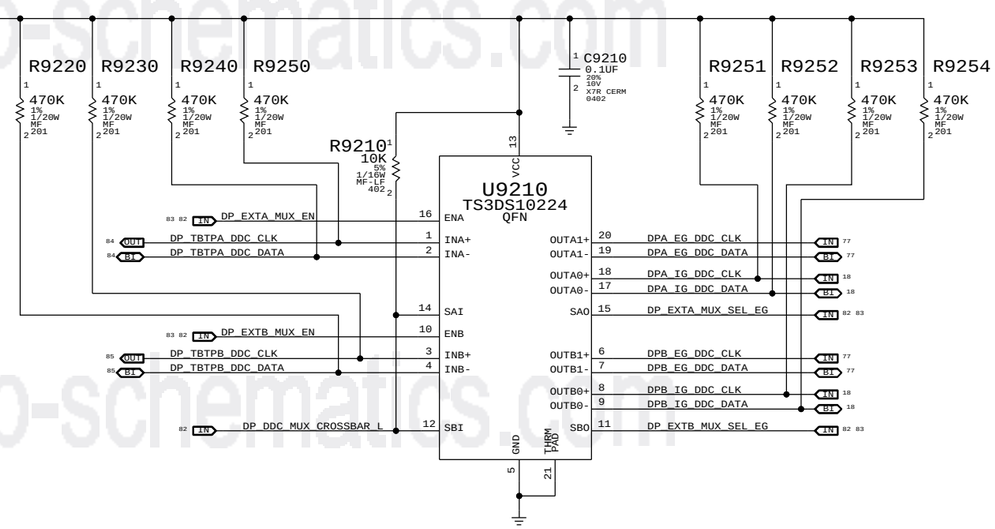
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=D2_SEAN SYNC_DATE=03/05/2012

PAGE TITLE: eDP Muxed Graphics Support

Apple Inc.

DRAWING NUMBER: 051-9589 SIZE: D

REVISION: 4.18.0

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL
C9487 100UF 20% 6.3V POLY TANT CASE B2 SM
C9480 22UF 20% 6.3V X5R CERM 1 603
C9481 0.1UF 10% 16V X5R CERM 0201
=PPHV_SW_TBTAPWRSW
18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 25V X5R 402
CRITICAL
U9410
CD3210A0RGP
QFN
V3P3
VHV
RSVD
EN
HV_EN
S0
V3P3OUT
OUT
RSVD
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
PP3V3_SW_TBTAPWR
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.3V
PPHV_SW_TBTAPWR
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=15V
C9485 0.1UF 10% 16V X5R CERM 0201
C9486 10UF 20% 6.3V CERM X5R 0402
C9411 0.1UF 10% 25V X5R 402
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R9410 22.6K 1% 1/20W MF 201
R9411 22.6K 1% 1/20W MF 201
R9412 36.5K 1% 1/20W MF 201 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/20W MF 201 <RHVS3>
R9414 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R_3_per HV ISET_SX with cd3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES MTL FILM 1/20W 17.8K 1 0201 SMD LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES MTL FILM 1/20W 17.8K 1 0201 SMD LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

GND VOID=TRUE (Both C's)
TBT_A_D2R_P<0> OUT
TBT_A_D2R_N<0> OUT
C9474 0.47UF 20% 4V CERM X5R 1 201
C9475 0.47UF 20% 4V CERM X5R 1 201
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
GND VOID=TRUE
R9494 1K 5% 1/20W MF 201 SIGNAL MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL MODEL=EMPTY
DP_TBTPA_ML_C_P<3> IN
DP_TBTPA_ML_C_N<3> IN
C9478 0.22UF 20% 6.3V X5R 0201
C9479 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
TBT: Unused
TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
GND VOID=TRUE (Both C's)
TBT_A_D2R_P<1> OUT
TBT_A_D2R_N<1> OUT
C9476 0.47UF 20% 4V CERM X5R 1 201
C9477 0.47UF 20% 4V CERM X5R 1 201
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
CRITICAL
SIGNAL MODEL=TBTPIN
GND VOID=TRUE
(Both D's)
D9498 BAR90-02LRH TSLP 2 7
D9499 BAR90-02LRH TSLP 2 7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL
L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL MODEL=EMPTY
L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL MODEL=EMPTY
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V C0G NP0 0402
C9499 30PF 5% 50V C0G NP0 0402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC OUT
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R CERM 0201
C9495 330PF 10% 16V X7R CERM 0201
R9441 100K 5% 1/20W MF 201
C9402 0.01UF 10% 16V X5R CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

Thunderbolt Connector A

CRITICAL
L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=15V
C9400 0.01UF 10% 50V X7R CERM 0402
C9401 0.01UF 10% 50V X7R CERM 0402
TBTACONN_20_RC
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=18V
R9401 12 5% 1/20W MF 201

For J9400 TBT SMT pads (3 5 17 & 19)

TBT Dir
DP Dir
SHIELD PINS
J9400
MDP-D2
F-RT-TH
PORT B
SHIELD PINS
514-0803

B2	HPD	GND0	B1
B4	CONFIG1	ML_LANE0P	B3
B6	CONFIG2	ML_LANE0N	B5
B8	GND2	GND1	B7
B10	ML_LANE3P	ML_LANE1P	B9
B12	ML_LANE3N	ML_LANE1N	B11
B14	GND4	GND3	B13
B16	AUX_CHP	ML_LANE2P	B15
B18	AUX_CHN	ML_LANE2N	B17
B20	DP_PWR	RETURN	B19

SHIELD PINS: S22 S21 S20 S19 S18 S17
SHIELD PINS: S16 S15 S14 S13 S12

TBTACONN_1_C
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=18.9V
GND VOID=TRUE
C9405 0.01UF 10% 25V X5R-CERM 0201
(0-18.9V)
DP Dir
TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
TBTACONN_7_C
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=18.9V
GND VOID=TRUE
C9406 0.01UF 10% 25V X5R-CERM 0201
(0-18.9V)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1

SIGNAL_MODEL=TBT_MUX
TBT_A_CIO_SEL IN
DP_AUXIO_EN IN
DP_TBTPA_AUXCH_C_N IN
DP_TBTPA_AUXCH_C_P IN
C9430 0.1UF 10% 16V X5R CERM01
C9431 0.1UF 10% 16V X5R CERM01
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DAT IN
DP_TBTPA_DDC_CLK IN
TBT_A_CONFIG1_BUF OUT
DP_TBTPA_ML_C_P<1> IN
DP_TBTPA_ML_C_N<1> IN
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX IN
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN IN
DP_TBTPA_HPD OUT
PP3V3_SW_TBTAPWR
CRITICAL
U9460
74AUP1T97
SOT891 5
TBT_A_LSRX OUT
Y = B
C9460 0.1UF 10% 16V X5R-CERM 0201
R9426 1M 5% 1/20W MF 201
VDD
CRITICAL
U9420
CBTL05023
HVQFN
BIASIN
AUXIO_EN
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
DP_PD
HPDOUT
GND THMPAD
BIASOUT
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
TBT_A_BIAS
VOLTAGE=3.3V
C9425 0.1UF 10% 16V X5R CERM 0201
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
R9428 100K 5% 1/20W MF 201

GND VOID=TRUE (Both C's)
C9470 0.22UF 20% 6.3V X5R 0201
C9471 0.22UF 20% 6.3V X5R 0201
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
C9472 0.22UF 20% 6.3V X5R 0201
C9473 0.22UF 20% 6.3V X5R 0201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
470K R's for ESD protection on AC-coupled signals.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW
CRITICAL
C9687 100UF 20% 6.3V POLY TANT CASE B2 SM
C9680 22UF 20% 6.3V X5R CERM 1 603
C9681 0.1UF 10% 16V X5R CERM 0201
=PPHV_SW_TBTBPWRSW
18V Max
C9615 4.7UF 10% 25V X5R-CERM 0603
C9610 0.1UF 10% 25V X5R 402
U9610 CRITICAL
CD3210A0RGP
QFN
V3P3
VHV
RSVD
EN
HV_EN
S0
V3P3OUT
OUT
RSVD
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
PP3V3_SW_TBTBPWR
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=3.3V
PPHV_SW_TBTBPWR
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=15V
C9685 0.1UF 10% 16V X5R CERM 0201
C9686 10UF 20% 6.3V CERM X5R 0402
C9611 0.1UF 10% 25V X5R 402
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R9610 22.6K 1% 1/20W MF 201
R9611 22.6K 1% 1/20W MF 201
R9612 36.5K 1% 1/20W MF 201
<RV3P3>
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
R9613 22.6K 1% 1/20W MF 201
R9614 22.6K 1% 1/20W MF 201
<RHVS3>
<RHVS0>
Single-fault protection requires two R's per HV ISET_SX with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES MTL FILM 1/20W 17 8K 1 0201 SMD LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES MTL FILM 1/20W 17 8K 1 0201 SMD LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

PP3V3_SW_TBTBPWR
C9620 0.1UF 10% 16V X5R CERM 0201
C9621 0.1UF 10% 16V X5R CERM 0201
R9627 10K 5% 1/20W MF 201
R9629 100K 5% 1/20W MF 201
VDD
SIGNAL_MODEL=TBT_MUX
CRITICAL
U9620
CBTL05023
HVQFN
TBT_B_BIAS
VOLTAGE=3.3V
C9625 0.1UF 10% 16V X5R CERM 0201
TBT_B_CIO_SEL
DP_AUXIO_EN
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
C9630 0.1UF 10% 16V X5R CERM01
C9631 0.1UF 10% 16V X5R CERM01
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
C9632 0.22UF 20% 6.3V X5R 0201
C9633 0.22UF 20% 6.3V X5R 0201
TBT_B_LSTX
TBT_B_LSRX_UNBUF
DP_TBTPB_HPD
BIASIN
AUXIO_EN
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
DP_PD
HPDOUT
BIASOUT
AUXIO-
AUXIO+
CA_DET
DPML0+
DPML0-
HPD
GND THMPAD
TBT_B_AUXCH_DDC_N
TBT_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC
TBT_B_LSX_ML_P<1>
TBT_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_HPD
R9626 1M 5% 1/20W MF 201
R9628 100K 5% 1/20W MF 201
PP3V3_SW_TBTBPWR
CRITICAL
U9660
74AUP1T97
SOT891 5
TBT_B_LSRX
Y = B
C9660 0.1UF 10% 16V X5R-CERM 0201
CRITICAL
L9600
FERR-120-OHM-3A
0603
PP3V3RHV_SW_TBTBPWR
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=15V
C9600 0.01UF 10% 50V X7R CERM 0402
TBTBCONN_20_RC
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=18V
C9601 0.01UF 10% 50V X7R CERM 0402
R9601 12 5% 1/20W MF 201
For J9600 TBT SMT pads (3 5 17 & 19)
TBTBCONN_1_C
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=18.9V
C9605 0.01UF 10% 25V X5R-CERM 0201
GND VOID=TRUE (Both C's)
C9670 0.22UF 20% 6.3V X5R 0201
C9671 0.22UF 20% 6.3V X5R 0201
R9670 470K 5% 1/20W MF 201
R9671 470K 5% 1/20W MF 201
TBT_B_R2D_C_P<0>
TBT_B_R2D_N<0>
TBT: TX_0
TBTBCONN_7_C
MIN LINE WIDTH=0.38 MM
MIN NECK WIDTH=0.20 MM
VOLTAGE=18.9V
C9606 0.01UF 10% 16V X5R-CERM 0201
(0-18.9V)
DP Dir
TBT Dir
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT: TX_1
C9672 0.22UF 20% 6.3V X5R 0201
C9673 0.22UF 20% 6.3V X5R 0201
R9672 470K 5% 1/20W MF 201
R9673 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.
J9400
MDP-D2
F-RT-TH
SHIELD PINS
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT A
514-0803
TBT Dir
DP Dir
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
C9674 0.47UF 20% 4V CERM X5R 1 201
C9675 0.47UF 20% 4V CERM X5R 1 201
R9694 1K 5% 1/20W MF 201
R9695 1K 5% 1/20W MF 201
SIGNAL_MODEL=EMPTY
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
C9678 0.22UF 20% 6.3V X5R 0201
C9679 0.22UF 20% 6.3V X5R 0201
TBT: Unused
R9678 470K 5% 1/20W MF 201
R9679 470K 5% 1/20W MF 201
TBT_B_BIAS
R9698 2.2K 5% 1/20W MF 201
R9699 2.2K 5% 1/20W MF 201
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
C9676 0.47UF 20% 4V CERM X5R 1 201
C9677 0.47UF 20% 4V CERM X5R 1 201
CRITICAL
SIGNAL_MODEL=TBTPIN
GND VOID=TRUE
(Both D's)
D9698 BAR90-02LRH
D9699 BAR90-02LRH
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
CRITICAL
L9698
650NH-5%-0.430MA-0.52OHM
0603
SIGNAL_MODEL=EMPTY
CRITICAL
L9699
650NH-5%-0.430MA-0.52OHM
0603
SIGNAL_MODEL=EMPTY
DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N
C9698 30PF 5% 50V C0G NP0 0402
C9699 30PF 5% 50V C0G NP0 0402
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R9652 1M 5% 1/20W MF 201
R9651 1M 5% 1/20W MF 201
C9694 330PF 10% 16V X7R CERM 0201
C9695 330PF 10% 16V X7R CERM 0201
R9641 100K 5% 1/20W MF 201
C9602 0.01UF 10% 16V X5R CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!

*L9710 Q9701 D9701 C9715 C9719 SHOULD ALL BE PLACED NEAR EACH OTHER

C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719

C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS

LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT

(EEPROM should set EN_I_RES=1)

PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES 0OHM 0402	R9717 R9718 R9719 R9720 R9721 R9722		D BKL PROD

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PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

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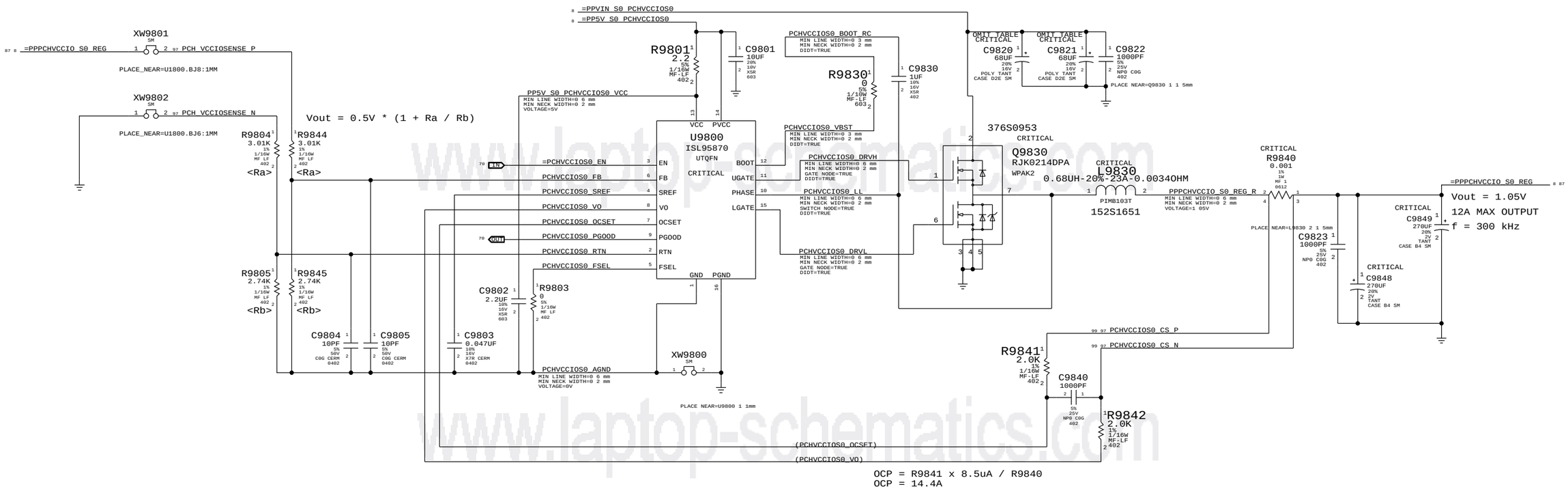
PCH VCCIO (1.05V S0) REGULATOR



SYNC MASTER=D2 KEPLER SYNC DATE=01/13/2012

PAGE TITLE

PCH VCCIO (1.05V) POWER SUPPLY

Apple Inc.

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GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME
up in the following order

1) GPU 3 3V
2) IFPX IOVDD 1 8V
3) GPUVCORE
4) FBVDDQ/GDDR5 1 35V
5) PEXVDD/Q OR IFPY IOVDD 1 05V

82	EG_RAIL1_EN	P3V3GPU EN (MAKE BASE TRUE)	=P3V3GPU MISC EN	OUT 69
			=P3V3GPU EN	OUT 69
82	EG_RAIL2_EN	P1V8GPU EN (MAKE BASE TRUE)	=P1V8GPU EN	OUT 8
82	EG_RAIL3_EN	GPUVCORE EN (MAKE BASE TRUE)	=GPUVCORE EN	OUT 80
82	EG_RAIL4_EN	P1V35GPUFB EN (MAKE BASE TRUE)	=P1V35FB EN	OUT 74
82	EG_RAIL5_EN	P1V05 S0GPU EN (MAKE BASE TRUE)	=P1V05 GPU EN	OUT 74

NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

=PP3V3_S0_PWRCTL
88 70 8

R9900 100K 5% 1/20W MF 201
R9901 100K 5% 1/20W MF 201
R9902 100K 5% 1/20W MF 201

69 8	IN =PP3V3_S0GPU_FET	GPU_PGOOD1	OUT 82
8	IN =PP1V8_GPU_FET	GPU_PGOOD2	OUT 82
80	IN GPUVCORE_PGOOD (MAKE BASE TRUE)	GPU_PGOOD3	OUT 82
74	IN GPUFB_PGOOD (MAKE BASE TRUE)	GPU_PGOOD4	OUT 82
74	IN P1V05_S0GPU_PGOOD (MAKE BASE TRUE)	PM_ALL_GPU_PGOOD	OUT 82

NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

Unused PGOOD signal

88 70 8 =PP3V3_S0_PWRCTL

NO STUFF
R9991 10K 5% 1/16W MF LF 402

CPUIMVP_AXG_PGOOD	IN 65	
TP_DDRREG_PGOOD (MAKE_BASE TRUE)	DDRREG_PGOOD	IN 64
TP_P1V5S3RS0_RAMP_DONE (MAKE_BASE TRUE)	P1V5S3RS0_RAMP_DONE	IN 69

PEG_R2D_P<0> 71 89
R9910 82 5% 1/20W MF 201
NOSTUFF
PEG_R2D_N<0> 71 89

PEG_R2D_P<5> 71 89
R9915 82 5% 1/20W MF 201
NOSTUFF
PEG_R2D_N<5> 71 89

PEG_R2D_P<3> 71 89
R9913 82 5% 1/20W MF 201
NOSTUFF
PEG_R2D_N<3> 71 89

PEG_R2D_P<7> 71 89
R9917 82 5% 1/20W MF 201
NOSTUFF
PEG_R2D_N<7> 71 89

PLACE R9910 - R9917 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_D2R_P<0> 9 71 89
R9920 82 5% 1/20W MF 201
NOSTUFF
PEG_D2R_N<0> 9 71 89

PEG_D2R_P<4> 9 71 89
R9924 82 5% 1/20W MF 201
NOSTUFF
PEG_D2R_N<4> 9 71 89

PEG_D2R_P<7> 9 71 89
R9927 82 5% 1/20W MF 201
NOSTUFF
PEG_D2R_N<7> 9 71 89

PLACE R9920 - R9927 CLOSE TO U1000

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4 OHM SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	85 OHM DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	90 OHM DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	15 MIL	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	15 MIL	?

PEG

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	80 OHM DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_RXRX	*	=4X_DIELECTRIC	?
PEG_TXTX	*	=4X_DIELECTRIC	?
PEG_TXRX	*	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_D2R	PEG_D2R	*	PEG_RXRX
PEG_R2D	PEG_R2D	*	PEG_TXTX
PEG_D2R	PEG_R2D	*	PEG_TXRX

CPU Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 10
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 10
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 10
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 10
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	11 17
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3:0>	10 82
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3:0>	10 82
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	10 82
DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	10 82
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	9 11
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	9 11
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_RESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 41
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 42
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 41 42 65
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_BMIL	PM_THRMTRIP_L	11 20 42
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 65
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 65
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 65
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 62
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 67
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 65
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	13
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	13
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	13
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	13
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 62
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 33
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 29 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	30 31 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 29 33
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	30 31 33
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	71 88
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	71 88
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	9 71
	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	9 71
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R_P<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_N<7..0>	9 71 88
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	71
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	71

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?
MEM_DQBL2BL	*	16 MILS	?
MEM_DQCH2CH	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

DDR3 (Memory Down):
DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	12 28 29 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	12 28 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..2>	
MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..2>	
MEM_A_CNTL1	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 29 32
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 29 32
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 29 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 28 29
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 28 29
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 28 29
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 28 29
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 28 29
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 28 29
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 28 29
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28 29
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28 29
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28 29
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28 29
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28 29
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28 29
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28 29
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28 29
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	12 30 31 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..2>	
MEM_B_CNTL1	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 31 32
MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 30 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 30 31 32
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..1>	12 31 32
MEM_B_CNTL0	MEM_37S	MEM_CTRL	MEM_B_ODT<0>	12 30 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..7>	12 30 31 32
MEM_B_CMD6	MEM_40S	MEM_CMD	MEM_B_A<6>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<5..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 30 31 32
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 30 31 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 30 31
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 30 31
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 30 31
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 30 31
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 30 31
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 30 31
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 30 31
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 30 31
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 30 31
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 30 31
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 30 31
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 30 31
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 30 31
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 30 31
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 30 31
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 30 31

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_DP_90D	*	90 OHM DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	90 OHM DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	1to3 3to4 3to5 1to10	=4:1_SPACING	?
LVDS	1to3 3to4 3to5 1to10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	90 OHM DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	37 OHM SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	50 OHM SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	1to3 3to4 3to5 1to10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	85 OHM DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	1to3 3to4 3to5 1to10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	1to3 3to4 3to5 1to10	=5:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	9 18
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	9 18
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	9 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	9 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	17 39
	SATA_90D	SATA	SATA_HDD_R2D_C_N	17 39
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_D2R_P	17 39
	SATA_90D	SATA	SATA_HDD_D2R_N	17 39
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_P	39
	SATA_90D	SATA	SATA_SSD_D2R_MUX_OUT_N	39
SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_P	39
	SATA_90D	SATA	SATA_SSD_R2D_MUX_IN_N	39
T233 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_D2R_P	39
T233	SATA_90D	SATA	SATA_SSD_D2R_N	39
T235 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSD_R2D_P	39
T235	SATA_90D	SATA	SATA_SSD_R2D_N	39
T218 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	
T219	SATA_90D	SATA	SATA_HDD_R2D_UF_N	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 17
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 17
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_D2R_P	9 17
	SATA_90D	SATA	SATA_ODD_D2R_N	9 17
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_D2R_UF_P	
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	
T213 PCH_SATA3_TCOMP	SATA_50SE	SATA_TCOMP	PCH_SATA3COMP	17
PCH_SATA_TCOMP	SATA_37SE	SATA_TCOMP	PCH_SATAICOMP	17
T235 USB_HUB1_UP	USB_85D	USB	USB_EXTB_XHCI_P	19 26
T237	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_HUB1_UP	USB_85D	USB	USB_EXTB_EHCI_P	19 26
	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 40
	USB_85D	USB	USB_EXTA_N	19 40
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 38
	USB_85D	USB	USB_EXTB_N	7 26 38
USB_EXTC	USB_85D	USB	USB_EXTC_P	9 19
	USB_85D	USB	USB_EXTC_N	9 19
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 34
	USB_85D	USB	USB_CAMERA_CONN_N	7 34
USB_BT	USB_85D	USB	USB_BT_P	9 34
	USB_85D	USB	USB_BT_N	9 34
USB_BT	USB_85D	USB	USB_BT_CONN_P	7 34
	USB_85D	USB	USB_BT_CONN_N	7 34
T260 USB_BT	USB_85D	USB	USB_BT_WAKE_P	34
T259	USB_85D	USB	USB_BT_WAKE_N	34
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 49
	USB_85D	USB	USB_TPAD_N	9 49
USB_IR	USB_85D	USB	USB_SMC_P	9 41
	USB_85D	USB	USB_SMC_N	9 41
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
T231 USB_T29A	USB_85D	USB	USB_EXTD_XHCI_P	19 26
T232	USB_85D	USB	USB_EXTD_XHCI_N	19 26
T241 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	40
T242	USB_85D	USB	USB_EXTA_MUXED_N	40
T247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 34
T248	USB_85D	USB	USB_CAMERA_N	19 34
T245 USB_EXTA	USB_85D	USB	USB_LT1_P	40
T246	USB_85D	USB	USB_LT1_N	40
T226 USB3_EXTB_TX	USB_85D	USB3	USB3_EXTB_TX_P	19 38
T224	USB_85D	USB3	USB3_EXTB_TX_N	19 38
T227 USB3_EXTB_RX	USB_85D	USB3	USB3_EXTB_RX_P	7 19 38
T225	USB_85D	USB3	USB3_EXTB_RX_N	7 19 38
T223 USB3_EXTC_TX	USB_85D	USB3	USB3_EXTC_TX_P	9 19
T220	USB_85D	USB3	USB3_EXTC_TX_N	9 19
T229 USB3_EXTC_RX	USB_85D	USB3	USB3_EXTC_RX_P	9 19
T222	USB_85D	USB3	USB3_EXTC_RX_N	9 19
T238 USB3_EXTA_TX	USB_85D	USB3	USB3_EXTA_TX_P	19 40
T239	USB_85D	USB3	USB3_EXTA_TX_N	19 40
T228 USB3_EXTA_RX	USB_85D	USB3	USB3_EXTA_RX_P	19 40
T240	USB_85D	USB3	USB3_EXTA_RX_N	19 40

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
T255 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
T255 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
T254	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
T253 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
T252	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
T251 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 35
T250	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
LPC_AD	LPC_50S	LPC	LPC_AD<3..0> 7 17 41 43 82
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L 7 17 41 43 82
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L 25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R 19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC 25 41
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS 7 25 43
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK 17 44
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA 17 44
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK 17 44
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA 17 44
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK 17 44
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA 17 44
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK 17 53
	HDA_50S	HDA	HDA_BIT_CLK_R 17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC 17 53
	HDA_50S	HDA	HDA_SYNC_R 17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L 17
	HDA_50S	HDA	HDA_RST_L 17 53
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0 17 53
	HDA_50S	HDA	AUD_SDI_R 53
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT 17 53
	HDA_50S	HDA	HDA_SDOUT_R 17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 17 43
	SPI_55S	SPI	SPI_CLK 43
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 17 43
	SPI_55S	SPI	SPI_MOSI 43
SPI_MISO	SPI_55S	SPI	SPI_MISO 17 43
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 17 43
	SPI_55S	SPI	SPI_CS0_L 43
	PCIE_85D	PCIE	PCIE_ENET_R2D_P
	PCIE_85D	PCIE	PCIE_ENET_R2D_N
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P 7 17 38
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N 7 17 38
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P 7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_N 7 17 38
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N
	PCIE_85D	PCIE	PCIE_AP_R2D_P 7 34
	PCIE_85D	PCIE	PCIE_AP_R2D_N 7 34
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P 17 34
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N 17 34
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P 17 34
	PCIE_85D	PCIE	PCIE_AP_D2R_N 17 34
1270 PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P 7 34
1270	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N 7 34
1270 PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P 34
1270	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N 34
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_P 39
	PCIE_85D	PCIE	PCIE_SSD_D2R_MUX_OUT_N 39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_C_P<1..0> 9 39
	PCIE_85D	PCIE	PCIE_SSD_R2D_C_N<1..0> 9 39
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_P<1..0> 9 39
	PCIE_85D	PCIE	PCIE_SSD_D2R_N<1..0> 9 39
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_P 39
	PCIE_85D	PCIE	PCIE_SSD_R2D_MUX_IN_N 39
1274 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_SSD_D2R_C_P<1> 39
1274	PCIE_85D	PCIE	PCIE_SSD_D2R_C_N<1> 39
1274 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_SSD_R2D_P<1> 39
1274	PCIE_85D	PCIE	PCIE_SSD_R2D_N<1> 39
1253 PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P 17
1254	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N 17
1267 PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P 17 35
1261	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N 17 35
1255	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P 17
1257	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N 17
1266 PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P 17
1262	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N 17
1258	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK 17
1268	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN 17 25
1270 PCIE_CLK100M	1_1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_P 71 95
1280	1_1_DIFFPAIR	CLK_PCIE	PEX_TSTCLK_O_N 71 95
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P 17 71
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N 17 71
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P 7 17 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N 7 17 38
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P 17 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N 17 34
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P 9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N 9 17
1281 PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P 17 39
1282	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N 17 39
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P 9 17
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N 9 17
1263 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0> 9 35
1264 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0> 9 35
1265 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0> 35
1287 PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0> 35
1260 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0> 9 35
1262 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0> 9 35
1270 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0> 35
1269 PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0> 35

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80 OHM DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
TBTDP_85D	*	=85 OHM DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
TBTDP_100D	*	=100 OHM DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Thunderbolt/DP Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0> 7 35 84
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0> 7 35 84
	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0> 7 84
	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0> 7 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2> 35 84
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2> 35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2> 84
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2> 84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 84
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1..0> 7 84
	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1..0> 7 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_P<1..0> 7 35 84
TBT_A_D2R	TBTDP_85D	TBTDP	TBT_A_D2R_N<1..0> 7 35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P 35 84
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N 35 84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P 84
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N 84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P 84
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N 84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P 84
	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N 84
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0> 7 35 85
TBT_B_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0> 7 35 85
	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0> 7 85
	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0> 7 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2> 35 85
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2> 35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2> 85
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2> 85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 85
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1..0> 7 85
	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1..0> 7 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_P<1..0> 7 35 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R_N<1..0> 7 35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P 35 85
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N 35 85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P 85
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N 85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P 85
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N 85
TBT_B_D2R	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P 85
	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N 85

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK 35
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI 35
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO 35
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L 35

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 41 44
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 41 44
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	61
	1TO1_DIFFPAIR		CHGR_CSI_N	61
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	61
	1TO1_DIFFPAIR		CHGR_CSO_N	61

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PAGE TITLE: SMC Constraints

Apple Inc.

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85 OHM DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90 OHM DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

DisplayPort/TMDS intra pair matching should be 0 127mm Inter pair matching should be within 2 54cm Max Length 241 3mm
DIsplayPort AUX CH intra pair matching should be 0 127mm Max length 330 2mm
MAX LENGTH OF DISPLAYPORT/TMDS TRACES 13 INCHES
SOURCE Calpella SFF DG Rev 1 5 (407364) and Family GPU DG 04202 001 v04

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P	73 75
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N	73 75
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P	73 75
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N	73 75
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 A<8..0>	73 75
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 A<8..0>	73 75
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 ABI L	73 75
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 ABI L	73 75
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 RAS L	73 75
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 RAS L	73 75
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CAS L	73 75
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CAS L	73 75
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 WE L	73 75
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 WE L	73 75
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 CKE L	73 75
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 CKE L	73 75
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB A0 CS L	73 75
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB A1 CS L	73 75
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0>	73 75
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1>	73 75
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2>	73 75
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3>	73 75
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0>	73 75
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1>	73 75
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2>	73 75
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3>	73 75
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>	73 75
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>	73 75
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>	73 75
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>	73 75
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>	73 75
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>	73 75
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>	73 75
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>	73 75
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0>	73 75
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0>	73 75
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1>	73 75
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1>	73 75
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0>	73 75
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0>	73 75
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1>	73 75
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1>	73 75
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7..0>	73 75
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15..8>	73 75
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23..16>	73 75
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31..24>	73 75
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7..0>	73 75
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15..8>	73 75
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23..16>	73 75
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31..24>	73 75
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A0 RESET L	73 75
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB A1 RESET L	73 75

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P	73 76
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N	73 76
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P	73 76
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N	73 76
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 A<8..0>	73 76
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 A<8..0>	73 76
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 ABI L	73 76
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 ABI L	73 76
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 RAS L	73 76
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 RAS L	73 76
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CAS L	73 76
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CAS L	73 76
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 WE L	73 76
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 WE L	73 76
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 CKE L	73 76
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 CKE L	73 76
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB B0 CS L	73 76
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB B1 CS L	73 76
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>	73 76
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>	73 76
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>	73 76
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>	73 76
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>	73 76
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>	73 76
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>	73 76
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>	73 76
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>	73 76
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>	73 76
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>	73 76
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>	73 76
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>	73 76
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>	73 76
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>	73 76
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>	73 76
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>	73 76
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>	73 76
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>	73 76
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>	73 76
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>	73 76
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>	73 76
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>	73 76
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>	73 76
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7..0>	73 76
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15..8>	73 76
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23..16>	73 76
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31..24>	73 76
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7..0>	73 76
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15..8>	73 76
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23..16>	73 76
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31..24>	73 76
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B0 RESET L	73 76
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB B1 RESET L	73 76

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	81 82
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	81 82
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	81 82
	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	81 82
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 81
	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 81
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	77 82
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	77 82
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	7 81
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	7 81
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	81
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	81
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	77 82
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	77 82
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	18 83
	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	18 83
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	18 83
	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	18 83
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P	77 83
	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N	77 83
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P	77 83
	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N	77 83
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	7 35 83
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	7 35 83
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	7 35 83
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	7 35 83
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	7 35 77
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	7 35 77
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	7 35 77
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	7 35 77
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	7 35
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	7 35
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	7 35
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	7 35
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	7 35
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	7 35
DP_INT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	7 35
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	7 35

Kepler Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTALIN	77 78
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTALOUT	77 78
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT	
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU_OSC_27M_SSIN	77
	1_1_DIFFPAIR		PEX_TSTCLK_O_P	71 92
	1_1_DIFFPAIR		PEX_TSTCLK_O_N	71 92
HDMI_DATA	HDMI_90D	HDMI	HDMI_EG_DATA_C_P<2..0>	7 38 77
	HDMI_90D	HDMI	HDMI_EG_DATA_C_N<2..0>	7 38 77
HDMI_CLK	HDMI_90D	HDMI	HDMI_EG_CLK_C_P	7 38 77
	HDMI_90D	HDMI	HDMI_EG_CLK_C_N	7 38 77

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE 1TO1 55S	*	1 1_DIFFPAIR	55 OHM SE	55 OHM SE	55 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
THERM 1TO1 55S	*	1 1_DIFFPAIR	55 OHM SE	55 OHM SE	55 OHM SE	1 1 DIFFPAIR	1 1 DIFFPAIR
DIFFPAIR	*	1 1 DIFFPAIR			1 1 DIFFPAIR	1 1 DIFFPAIR	1 1 DIFFPAIR
AUDIODIFF	*	1 1_DIFFPAIR	0 1 MM	0 1 MM	10 MM	0 1 MM	0 1 MM
THERM 55S CPUIMVPISNS1	*	1 1_DIFFPAIR	55 OHM SE	55 OHM SE	55 OHM SE	0 2 MM	0 2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	2 1 SPACING	?
THERM	*	2 1 SPACING	?
AUDIO	*	2 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND P2MM	*	0 20 MM	1000
PWR P2MM	*	0 20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM CLK	*	GND P2MM
GND	MEM CMD	*	GND P2MM
GND	MEM CTRL	*	GND P2MM
GND	MEM * DQ BYTE*	*	GND P2MM
GND	MEM DQS	*	GND P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	GND	*	GND P2MM
CPU VCCSENSE	GND	*	GND P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK PCIE	GND	*	GND P2MM
PCIE	GND	*	GND P2MM
SATA	GND	*	GND P2MM
USB	GND	*	GND P2MM
CLK PCIE	SB POWER	*	PWR P2MM
SATA	SB POWER	*	PWR P2MM
USB	SB POWER	*	PWR P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS 85D	BGA	LVDS 85D
DP 85D	BGA	100 DIFF BGA
SATA 90D	BGA	100 DIFF BGA
CLK PCIE 90D	BGA	100 DIFF BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM 72D	BOTTOM			0 127 MM	6 35 MM		
MEM 85D	TOP			0 1 MM	6 35 MM		

D2 Specific Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	47
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	47
	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	47
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	47
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	47 77
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	47 77
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	45 62
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	45 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	45
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_R_P	45
	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	45 67
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	45 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	45
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	
	SENSE_1TO1_55S	SENSE	GPUISENS_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_N	45
	SENSE_1TO1_55S	SENSE	ISNS_1V5_MEM_P	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	96
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	96
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	96
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	96
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	99
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
	SENSE_1TO1_55S	SENSE	GPUFB_CS_P	74 99
	SENSE_1TO1_55S	SENSE	GPUFB_CS_N	74 99
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	98
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P	74 98
	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N	74 98
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	99
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	99
SENSE_DIFFPAIR_2	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	46 66
SENSE_DIFFPAIR_42	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	46 66
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	46
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	46
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	46
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	46
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_VSENSE_P	
	AUDIODIFF	AUDIO	ADC1_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_VSENSE_P	
	AUDIODIFF	AUDIO	ADC2_VSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC2_ISENSE_P	96
	AUDIODIFF	AUDIO	ADC2_ISENSE_N	96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_R_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_R_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKR_L_RSENSE_P	
	AUDIODIFF	AUDIO	SPKR_L_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO1_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_L_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	53 57
	AUDIODIFF	AUDIO	AUD_LO2_R_N	53 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	53 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	57
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_RSENSE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_INTIV_P	
	AUDIODIFF	AUDIO	LSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_INTIV_P	
	AUDIODIFF	AUDIO	RSPKR_INTIV_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_P	99
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_R_N	99
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	99

D2 Specific Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 34
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 34
	1TO1_DIFFPAIR		CHGR_CSI_R_P	61
	1TO1_DIFFPAIR		CHGR_CSI_R_N	61
	1TO1_DIFFPAIR		CHGR_CSO_R_P	61
	1TO1_DIFFPAIR		CHGR_CSO_R_N	61
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	
	USB_85D	USB	USB_LT2_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	57
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SL_P	
	AUDIODIFF	AUDIO	SSM2375SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375SR_P	
	AUDIODIFF	AUDIO	SSM2375SR_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P_R	
	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N_R	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_P	
	DIFFPAIR	AUDIO	LSPKR_VSENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_P	
	DIFFPAIR	AUDIO	RSPKR_VSENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P_R	
	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N_R	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	7 57 59
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	7 57 59
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	
	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSPKR_ISENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_P	
	DIFFPAIR	AUDIO	RSPKR_ISENSE_FILT_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	RSUBIN_P	57
	DIFFPAIR	AUDIO	RSUBIN_N	57
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	LSUBIN_P	57
	DIFFPAIR	AUDIO	LSUBIN_N	57
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SR_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SR_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SSM4321SL_P	
	DIFFPAIR	AUDIO	SSM4321SL_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_IN_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_IN_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_ISENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_ISENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSPKR_VSENSE_RDIVIDE_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_P	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSPKR_VSENSE_RDIVIDE_N	
	USB_85D	USB	USB_TPAD_R_P	26 49
	USB_85D	USB	USB_TPAD_R_N	26 49
	SB_POWER		PP3V3_S5	7 8
	SB_POWER		PP3V3_S0	7 8
	SB_POWER		PP1V5_S3RS0_CPUDDR	8
	GND		GND	

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Project Specific Constraints

Apple Inc.

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15" MBP BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?

15" MBP Specific Net Properties

	ELECTRICAL CONSTRAINT SET	PHYSICAL	SPACING	NET TYPE	
1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ADC1_ISENSE_P	
2		AUDIODIFF	AUDIO	ADC1_ISENSE_N	
3	SENSE_DIFFPAIR_42	THERM_55S_CPUIMVP7ISNS	THERM	CPUIMVP_ISNS1_P	46 65 66
4		THERM_55S_CPUIMVP7ISNS	THERM	CPUIMVP_ISNS1_N	46 66
5	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISNS2G_P	46 66
6		THERM_1TO1_55S	THERM	CPUIMVP_ISNS2G_N	46 66
7	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISNS2_P	46 65 66
8		THERM_1TO1_55S	THERM	CPUIMVP_ISNS2_N	46 66
9	SENSE_DIFFPAIR	THERM_55S_CPUIMVP7ISNS1	THERM	CPUIMVP_ISNS3_P	46 65 66
10		THERM_55S_CPUIMVP7ISNS1	THERM	CPUIMVP_ISNS3_N	46 66
11	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISUM_R_P	46
12		THERM_1TO1_55S	THERM	CPUIMVP_ISUM_R_N	46
13	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUIMVP_ISUMG_R_P	46
14		THERM_1TO1_55S	THERM	CPUIMVP_ISUMG_R_N	46
15	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_P	80
16		THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_N	80
17	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_P	80
18		THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_N	80
19	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_CPU_DDR_R_P	98
20		THERM_1TO1_55S	THERM	ISNS_CPU_DDR_R_N	98
21	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_LCD_PANEL_P	
22		THERM_1TO1_55S	THERM	ISNS_LCD_PANEL_N	
23	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_P1V5R1V35_CPUDDR_P	
24		THERM_1TO1_55S	THERM	ISNS_P1V5R1V35_CPUDDR_N	
26	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_SSD_P	39 99
25		THERM_1TO1_55S	THERM	ISNS_SSD_N	39 99
28	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	ISNS_SSD_R_P	99
27		THERM_1TO1_55S	THERM	ISNS_SSD_R_N	99
30	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	PCHVCCIO5O_CS_P	87 99
29		THERM_1TO1_55S	THERM	PCHVCCIO5O_CS_N	87 99
32	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	PCH_VCCIOSENSE_P	87
31		THERM_1TO1_55S	THERM	PCH_VCCIOSENSE_N	87
67	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P	79 80
68	SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N	79 80
64		THERM_1TO1_55S	THERM	GPU_FBVDDQ_SENSE	73 74
63		THERM_1TO1_55S	THERM	GPU_FBGND_SENSE	73 74
65		THERM_1TO1_55S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	74 79
66		THERM_1TO1_55S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	74 79
33	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	SPKRL_THMSNS_D2_P	
34		THERM_1TO1_55S	THERM	SPKRL_THMSNS_D2_N	
35	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	SPKR_THMSNS_D2_P	
36		THERM_1TO1_55S	THERM	SPKR_THMSNS_D2_N	
37	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	47
38		THERM_1TO1_55S	THERM	TBT_THERMD_N	47
39	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	X29THMSNS_D2_P	
40		THERM_1TO1_55S	THERM	X29THMSNS_D2_N	
57	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	VDDCIS0_CS_P	
58	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	VDDCIS0_CS_N	
59	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP6_VSEN_P	
60	SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP6_VSEN_N	
41		USB_85D	USB3	USB3_EXTA_TX_F_P	
42		USB_85D	USB3	USB3_EXTA_TX_F_N	
43		USB_85D	USB3	USB3_EXTA_RX_F_P	
44		USB_85D	USB3	USB3_EXTA_RX_F_N	
45		USB_85D	USB3	USB3_EXTA_TX_C_P	40
46		USB_85D	USB3	USB3_EXTA_TX_C_N	40
47		USB_85D	USB3	USB3_EXTB_TX_C_P	7 38
48		USB_85D	USB3	USB3_EXTB_TX_C_N	7 38
49		USB_85D	USB3	USB3_EXTB_RX_RC_P	38
50		USB_85D	USB3	USB3_EXTB_RX_RC_N	38
70		USB_85D	USB3	USB3_EXTA_RX_RC_P	40
69		USB_85D	USB3	USB3_EXTA_RX_RC_N	40
61			CLK_25M	P1V5_GPU_VSNS	
62			CLK_25M	P1V0S0_VSNS	

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP BOTTOM	0.058 MM	?
2:1_SPACING	TOP BOTTOM	0.116 MM	?
3:1_SPACING	TOP BOTTOM	0.174 MM	?
4:1_SPACING	TOP BOTTOM	0.232 MM	?
5:1_SPACING	TOP BOTTOM	0.290 MM	?
1:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.053 MM	?
2:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.106 MM	?
3:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.159 MM	?
4:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.212 MM	?
5:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.265 MM	?
1:1_SPACING	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.101 MM	?
2:1_SPACING	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.202 MM	?
3:1_SPACING	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.303 MM	?
4:1_SPACING	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.404 MM	?
5:1_SPACING	ISL ISL5 ISL6 ISL7 ISL8 I L11	0.505 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP BOTTOM	0.058 MM	?
2x_DIELECTRIC	TOP BOTTOM	0.116 MM	?
3x_DIELECTRIC	TOP BOTTOM	0.174 MM	?
4x_DIELECTRIC	TOP BOTTOM	0.232 MM	?
5x_DIELECTRIC	TOP BOTTOM	0.290 MM	?
1x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.053 MM	?
2x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.106 MM	?
3x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.159 MM	?
4x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.212 MM	?
5x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.265 MM	?
1X_DIELECTRIC	ISL ISL5 ISL6 ISL7 ISL8 ISL11	0.101 MM	?
2x_DIELECTRIC	ISL ISL5 ISL6 ISL7 ISL8 ISL11	0.202 MM	?
3x_DIELECTRIC	ISL ISL5 ISL6 ISL7 ISL8 ISL11	0.303 MM	?
4x_DIELECTRIC	ISL ISL5 ISL6 ISL7 ISL8 ISL11	0.404 MM	?
5x_DIELECTRIC	ISL ISL5 ISL6 ISL7 ISL8 ISL11	0.505 MM	?

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

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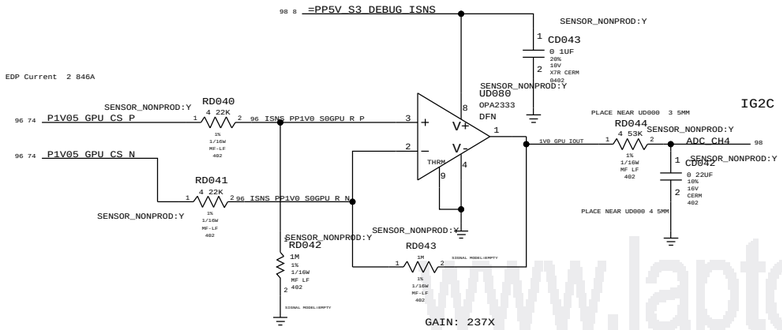
GPU 1.0V CURRENT SENSE



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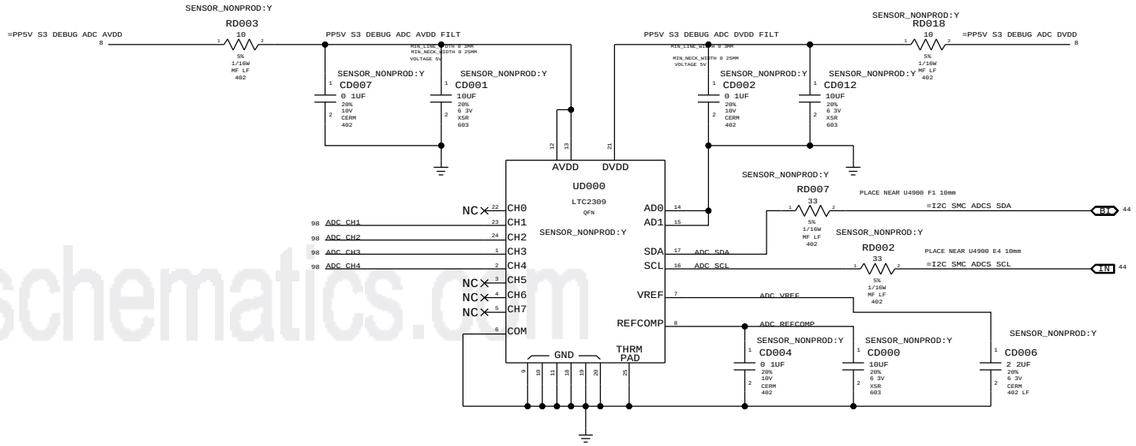
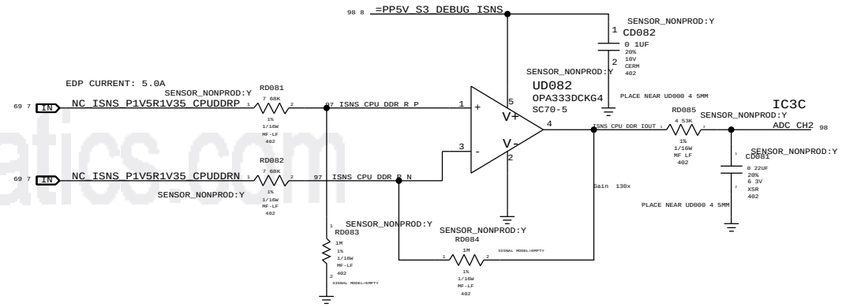
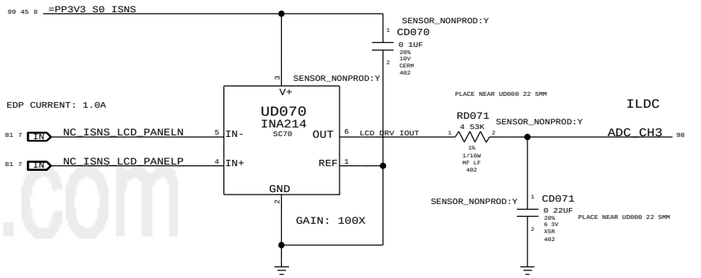
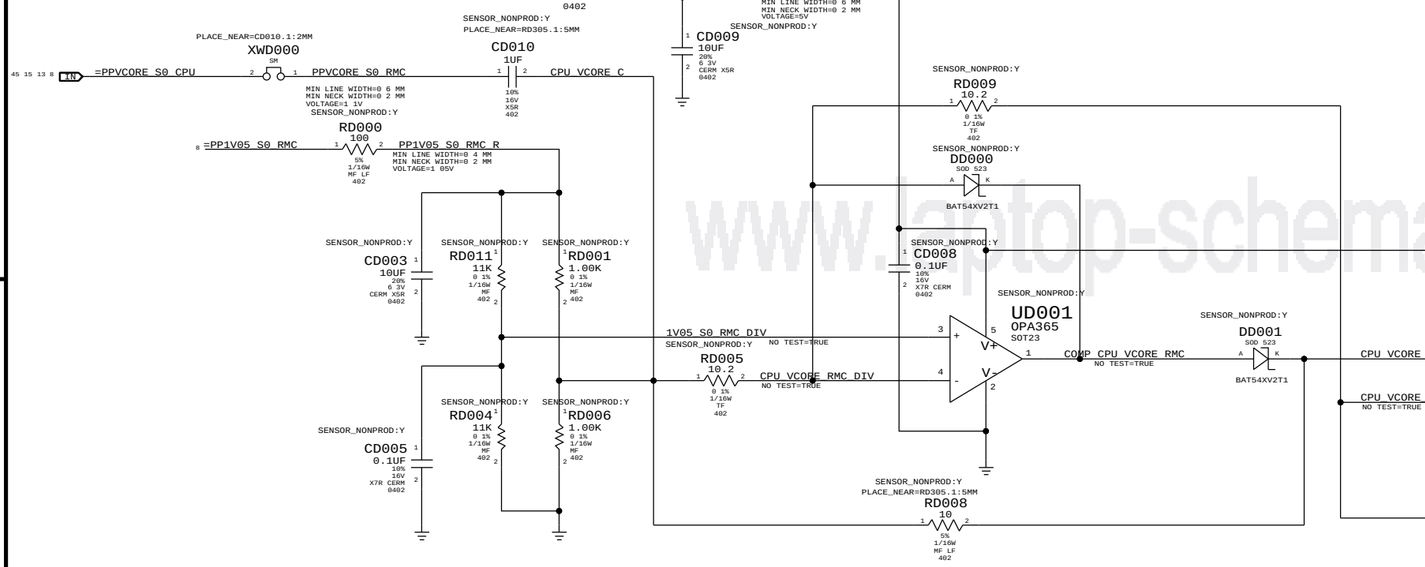


CPU DDR CURRENT SENSE



LCD PANEL CURRENT SENSE





SYNC MASTER=D2_SEAN SYNC DATE=03/05/2013

PAGE TITLE: DEBUG SENSORS AND ADC

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DRAWING NUMBER 051-9589 SIZE D

REVISION 4.18.0

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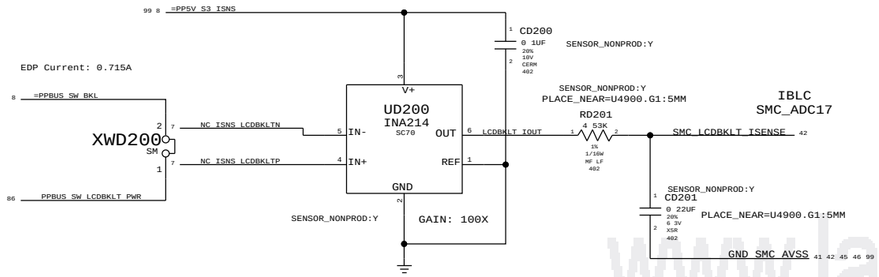
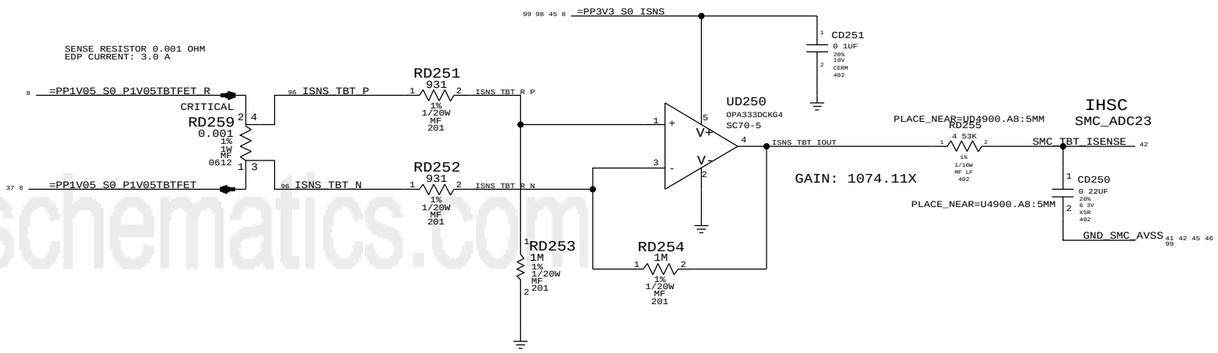
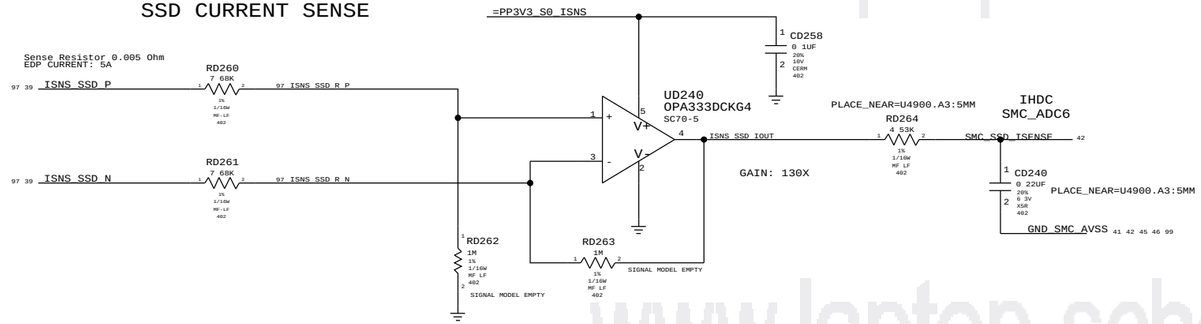
LCD BKLT Current Sense



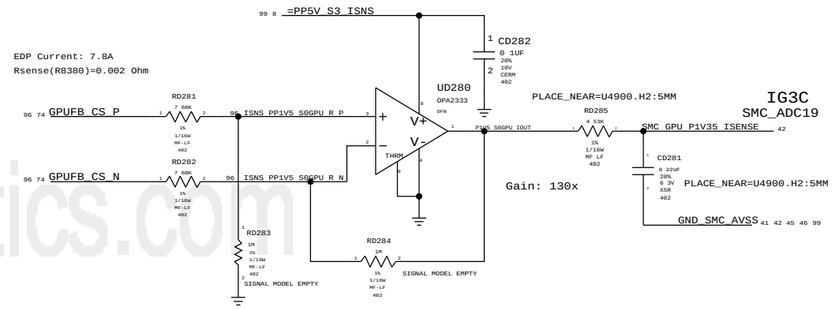
TBT (T29) CURRENT SENSE



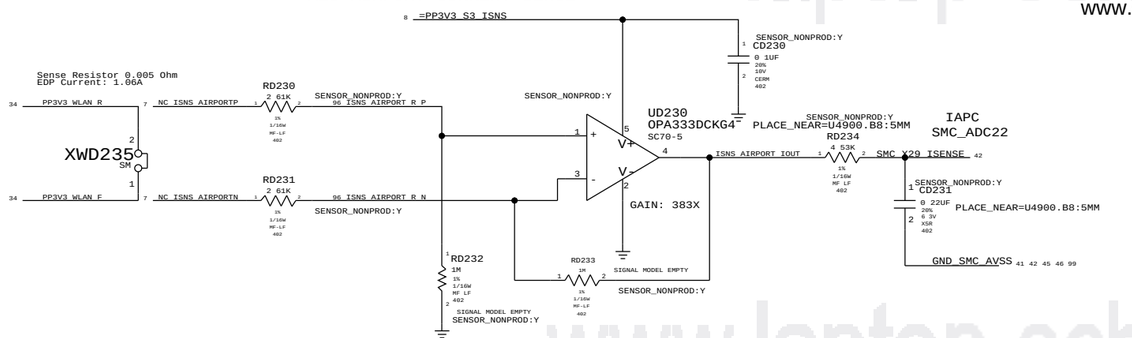
SSD CURRENT SENSE



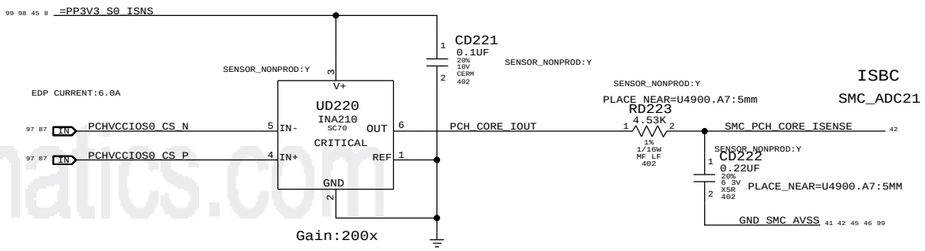
GPU FB (1.35V/1.5V) CURRENT SENSE



X29 AIRPORT CURRENT SENSE

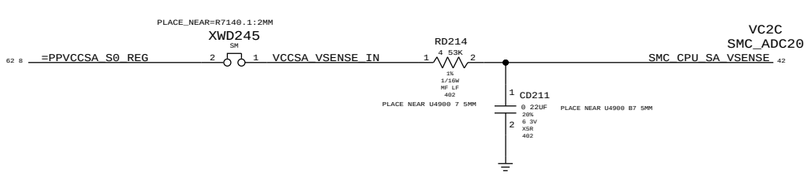


PCH VCORE CURRENT SENSE

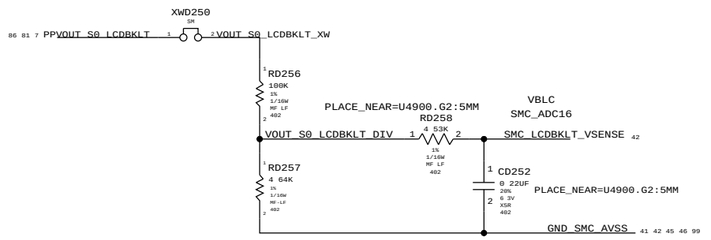


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	4	RES MTL FILM 100K 5 1/16W 0402 SMD LF	CD201 CD222 CD231		SENSOR NONPROD N

CPU VCCSA VOLTAGE SENSE



LCD BKLT Voltage Sense



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