1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-23

J11 MLB PIB SCHEMATIC
2.6.0
02/23/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9276	1	SCHEM,MLB,J11	SCH	CRITICAL	
820-3208	1	PCBF,MLB,J11	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 23 12:05:40 2012

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: SCHEM,MLB,J11

Apple Inc.

DRAWING NUMBER: 051-9276 | SIZE: D
REVISION: 2.7.0
BRANCH:
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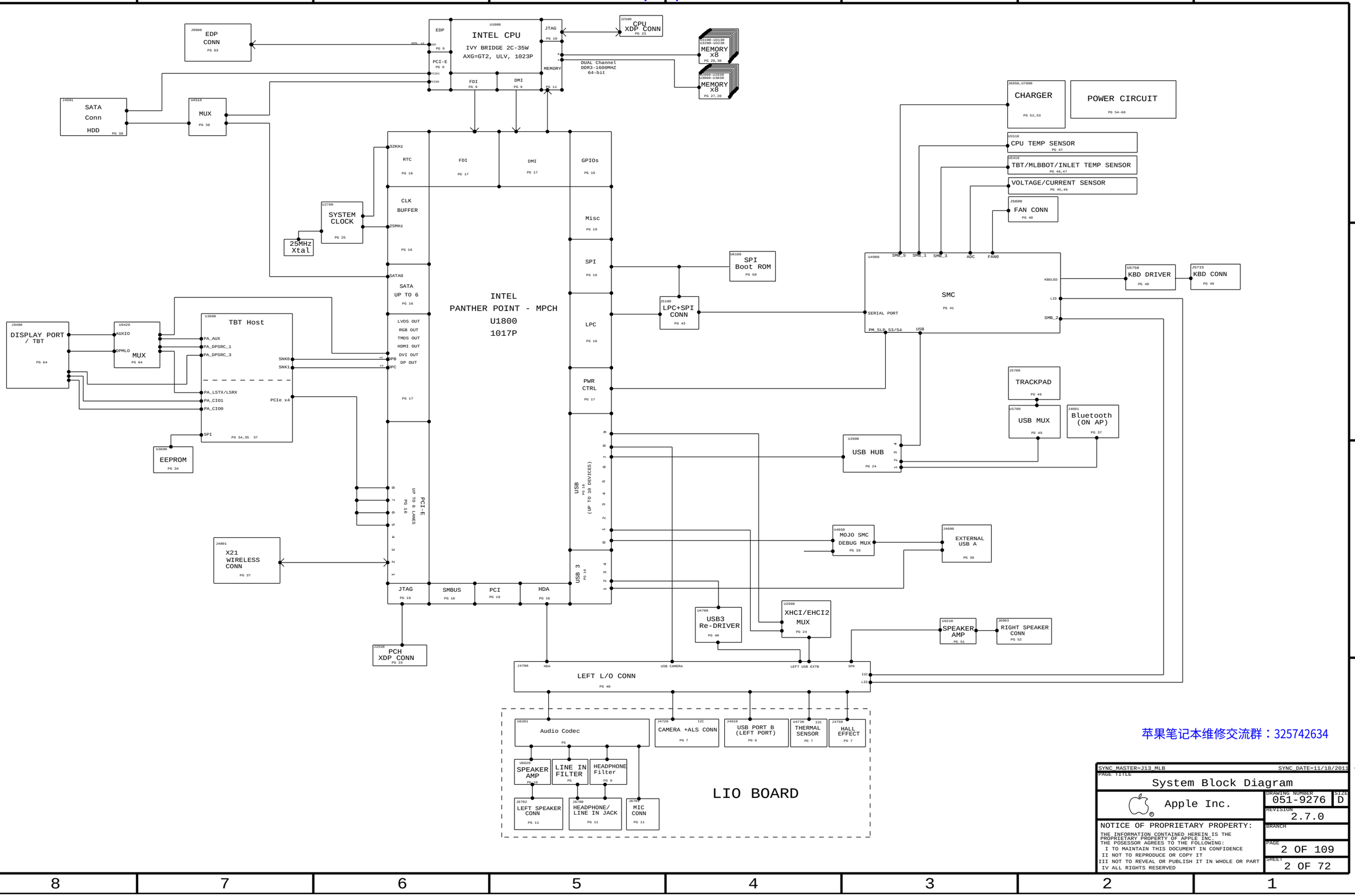
SHEET: 1 OF 72



苹果笔记本维修交流群：325742634

SYNC MASTER=J13_MLB
SYNC_DATE=11/18/2013

PAGE TITLE

System Block Diagram

Apple Inc.

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J11 POWER SYSTEM ARCHITECTURE

J6900 AC ADAPTER IN — DCIN(14.5V) — F6901 6A FUSE — SMC_DCIN_ISENSE — R7020 — VIN U7000 ISL6259HRTZ VOUT — PPVBAT_G3H_CHRG_RET — F7040 — PPBUS_G3H

PBUS SUPPLY/ BATTERY CHARGER (PAGE 53)

SMC_RESET_L (4) — SMC_BATT_ISENSE — R7050

J6950 — PPVBATT_G3H_CONN — 2S3P (6 TO 8.4V) — Q7055 — CHGR_BGATE — PPVBAT_G3H_CHGR_R

Q5310 SMC_GFX_VSENSE — D7005 — ENABLE PP5V5_CHRG_VDDP LT3470A U7090 (PAGE 53) — PP5V5_CHAR_VDDP

PPDCIN_G3H_OR_PBUS — R6905 — PPVIN_G3H_P3V42G3H — R6906 — R0954

Q5300 SMC_PBUS_VSENSE

D6905 — ENABLE 3.425V G3HOT LT3470A U6990 (PAGE 52) — PP3V42_G3H_REG

SMC POWER SN0903048 U5010 (PAGE 42) — SMC_RESET_L (4)

SMC U4900 (PAGE 41) — P60 (6) — RC DELAY — SMC_PM_G2_EN — P3V3S5_EN (7)

R5430 — PPVIN_S5_P5VP3V3 — VIN 5V (L/H) VOUT1 — 3.3V (R/H) VOUT2 — TPS51980 U7201 (PAGE 55) PGOOD — P5VS3_EN (13-1) — P3V3S5_EN (7) — PP5V_S3_REG — PP3V3_S5_REG — PP3V3_S5 (8) — P5VS3_PGOOD (14-1) — P3V3S5_PGOOD (9)

Q7860 — P5VS0_EN — PP5V_S0_FET (15)

PP5V_S0_KBDLED — U5750 MIC2292 — KBDLED_ANPDE

SMC_SYS_KBDLED — PAGE49

F9700 3A 32V — Q9706 — LCD_BKLT_EN — && BKLT_PLT_RST_L — VIN LP8550 U9701 (PAGE 65) — BKL_EN — EN VOUT — PPVOUT_SW_LCDBKLT

Q5300 — PBUSVSENS_EN — SMC_PBUS_VSENSE

Q3880 — T29_A_HV_EN — TBTBST_EN_UVLO — VIN LT3957 U3890 (PAGE 36) — PP15V_T29_REG

COUGAR-POINT (PCH) U1800 (PAGE 16~21)

SLP_S5#(E4) — PM_SLP_S5_L PG 17 — (11)
SLP_SUS# — PM_SLP_SUS_L — U7940 — P5V_3V3_SUS_EN PG61 — (10-1)
RC DELAY — P3V3S3_EN PG62 — (13)
RC DELAY — DDRREG_EN PG62 — USB_PWR_EN — (15)
P5VS3_EN PG62 — (13-2)
SLP_S4#(H4) — PM_SLP_S4_L PG 17 — (13)
SLP_S3#(F4) — PM_SLP_S3_L PG 17 — (14)

R7978 PG62 — PM_SLP_S3_R_L

RC DELAY — 1V05_S0_LDO_EN — (21)
RC DELAY — CPUVCCIOS0_EN — (21)
RC DELAY — PVCCSA_EN — (22)
RC DELAY — P1V5S0_EN — (19)
RC DELAY — P1V8S0_EN — (17)

P5VS0_EN — (14-1)
P3V3S0_EN — (14-1)
PBUSVSENS_EN — (14-1)

PP5V_S0_VCCSA — PVCCSA_EN — CPU_VCCSA_VID<1> — CPU_VCCSA_VID<0> — (22) — ISL95870AH U7100 (PAGE 54) — PPVCCSA_S0_REG — R7140 — (23)

PVCCSA_PGOOD — (23-1)

PP5V_S0_CPUVCCIOS0 — CPUVCCIOS0_EN — (21) — VIN 1.05V VOUT ISL95870 U7600 (PAGE 59) PGOOD — R7640 — PPCPUVCCIO_S0_REG — (22)

SMC_CPU_FSB_ISENSE

CPUVCCIOS0_PGOOD — (22-1)

TPS22920 U3816/U3826 (PAGE 36) — PP1V05_TBTCIO_FET

TBT_PWR_EN — (25)

CPU VCORE MAX15120 U7400 — CPUIMVP_VR_ON — (24) — VIN VOUT VR_ON — R7510 SMC_CPU_ISENSE — PPVCORE_S0_CPU_REG

R7550 SMC_GFX_ISENSE — PPVCORE_S0_AXG_REG (26)

(PAGE 57) — PGOOD — CPUIMVP_PGOOD (25-1) — PGOODG — CPUIMVP_AXG_PGOOD

U2750

DDRREG_EN — DDRVTT_EN — VIN 1.5V VLDOIN — S5 — S3 0.75V VOUT1 VOUT2 — R7350 — PPDDR_S3_REG — (16)

PPVTT_S0_DDR_LDO — (16-1) — DDRREG_PGOOD — TPS51916 U7300 (PAGE 56) PGOOD

Q7801 — P1V5CPU_EN — PP1V5_S3RS0_FET

ALL_SYS_PWRGD

PM_S0_PGOOD (27) — U2760 — SMC_DELAYED_PWRGD

COUGAR-POINT (PCH) U1800 (PAGE 16~21)

PWRBTN# — PM_PWRBTN_L
SYS_RERST# — PM_SYSRST_L
RSMRST# — PM_RSMRST_L
DPWROK — PM_DSW_PWRGD
PLTRST# — PLT_RERST_L (29)
PROCPWRGD — CPU_PWRGD (28)
DRAMPWROK — PM_MEM_PWRGD (30)
PM_PCH_PWRGD

CPU U1000 (PAGE 9~13)

SM_DRAMPWROK — UNCOREPWRGOOD — RESET*

P1V8S0_PGOOD
P5VS3_PGOOD
P3V3S5_PGOOD
CPUVCCIOS0_PGOOD
PVCCSA_PGOOD

SMC U4900 (PAGE 41)

ALL_SYS_PWRGD — (25) — PWRGD(P12)
S5_PWRGD — (9) — RSMRST_IN(P13)
SMC_ONOFF_L — (5) — PWR_BUTTON(P90)

RSMRST_OUT(P15) — PM_RSMRST_L (12)
99ms DLY
IMVP_VR_ON(P16) — CPUIMVP_VR_ON (26)
SYSRST(PA2) — PM_SYSRST_L
P17(BTN_OUT) — PM_PWRBTN_L (6-1)
RST* — SMC_RESET_L (4)

PM_SLP_S5_L — SLP_S5_L(P95)
PM_SLP_S4_L — SLP_S4_L(P94)
PM_SLP_S3_L — SLP_S3_L(P93)

P15 — PM_DSW_PWRGD (10)

R7962 — PP3V3_S0_VMON — VDD U7960 ISL88042IRTEZ (PAGE 62) — V2MON V3MON V4MON — PP5V_S0_VMON — PP1V5_S3RS0_VMON — PP1V05_S0_VMON

TPS720105 U7740 (PAGE 60) — PP3V3_SUS_FET — Q7820 — P5V_3V3_SUS_EN — (10-3) — PP1V05_SUS_LDO — (10-4)

Q7810 — P3V3S3_EN — PP3V3_S3_FET (14-1)

Q7840 — P5V_3V3_SUS_EN — PP5V_SUS_FET (10-2)

Q7830 — P3V3S0_EN — (14)

ISL8014A U7720 (PAGE 60) — P1V8_S0_EN (17) — PP3V3_S0 (16) — P1V8S0_PGOOD — PP1V8_S0_REG — (18)

TPS720105 U7780 (PAGE 60) — 1V05_S0_LDO_EN — PP1V05_S0_LDO. (19)

U7770 TPS72015 (PAGE 60) — EN — PP1V5_S0_REG

TPS22924 U3810 (PAGE 36) — T29_PWR_EN — R7831 — PP3V3_T29_FET — PP1V5S0_EN

R4599 — PP3V3_S0_SSD_R

SYNC_DATE=11/18/2011

PAGE TITLE: Revision History

Apple Inc.

DRAWING NUMBER: 051-9276 — SIZE: D
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3469	PCBA,MLB,1.5GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKL,DDR3:HYNIX_4GB
639-3470	PCBA,MLB,1.5GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKH,DDR3:SAMSUNG_4GB
639-3473	PCBA,MLB,1.5GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:DYKJ,DDR3:HYNIX_8GB
639-3659	PCBA,MLB,1.5GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.5GHZ,EEEE:F0V3,DDR3:ELPIDA_8GB
639-3471	PCBA,MLB,1.7GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKK,DDR3:HYNIX_4GB
639-3472	PCBA,MLB,1.7GHZ,SA 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKF,DDR3:SAMSUNG_4GB
639-3775	PCBA,MLB,1.7GHZ,EL 4GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27J,DDR3:ELPIDA_4GB
639-3474	PCBA,MLB,1.7GHZ,HY 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:DYKG,DDR3:HYNIX_8GB
639-3774	PCBA,MLB,1.7GHZ,SA 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F27D,DDR3:SAMSUNG_8GB
639-3660	PCBA,MLB,1.7GHZ,EL 8GB,J11	J11_CMNPTS,CPU:1.7GHZ,EEEE:F0V4,DDR3:ELPIDA_8GB
639-3776	PCBA,MLB,2.0GHZ,HY 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27K,DDR3:HYNIX_4GB
639-3778	PCBA,MLB,2.0GHZ,SA 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27G,DDR3:SAMSUNG_4GB
639-3780	PCBA,MLB,2.0GHZ,EL 4GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27H,DDR3:ELPIDA_4GB
639-3777	PCBA,MLB,2.0GHZ,HY 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27C,DDR3:HYNIX_8GB
639-3779	PCBA,MLB,2.0GHZ,SA 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F27F,DDR3:SAMSUNG_8GB
639-3781	PCBA,MLB,2.0GHZ,EL 8GB,J11	J11_CMNPTS,CPU:2.0GHZ,EEEE:F279,DDR3:ELPIDA_8GB
085-3937	J11 MLB DEVELOPMENT BOM	J11_DEVEL:ENG
607-9089	CMN PTS,PCBA,MLB,J11	J11_COMMON
939-0479	PCBA,MLB,1.9GHZ,HY 4GB,J11	J11_CMNPTS,CPU:1.9GHZ,EEEE:DYKL,DDR3:HYNIX_4GB

Bar Code Labels / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKL]	CRITICAL	EEEE:DYKL
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKH]	CRITICAL	EEEE:DYKH
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKK]	CRITICAL	EEEE:DYKK
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKF]	CRITICAL	EEEE:DYKF
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKJ]	CRITICAL	EEEE:DYKJ
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_DYKG]	CRITICAL	EEEE:DYKG
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F0V3]	CRITICAL	EEEE:F0V3
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F0V4]	CRITICAL	EEEE:F0V4
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F279]	CRITICAL	EEEE:F279
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27C]	CRITICAL	EEEE:F27C
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27D]	CRITICAL	EEEE:F27D
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27F]	CRITICAL	EEEE:F27F
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27G]	CRITICAL	EEEE:F27G
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27H]	CRITICAL	EEEE:F27H
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27J]	CRITICAL	EEEE:F27J
825-7670	1	LABEL,TEXT,MLB,K21/K78	[EEEE_F27K]	CRITICAL	EEEE:F27K

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3937	1	J11 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9089	1	CMN PTS,PCBA,MLB,J11	CMNPTS	CRITICAL	J11_CMNPTS

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE

K78 BOM Variants

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

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J11 BOM GROUPS

BOM GROUP	BOM OPTIONS
J11_COMMON	ALTERNATE,COMMON,J11_MISC,J11_DEBUG:ENG,J11_PROGPARTS,USBHUB2513B,EDP:YES,PCH_C1
J11_MISC	HUB_3NONREM,TBT,MPM5:YES,CPUMEM_SLG:NO,PP5VS_DCIN:NO,TPAD_PCH:NO,SKIP_5V3V3:INAUDIBLE,BTPWR:S4,TBTHV:P15V,LVDDR3_HW:YES,AXG_ACOUSTICS:NO
J11_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J11_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,XDP_PCH,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
J11_DEVEL:PVT	XDP_CONN
J11_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,XDP_CPU:BPM,LPCPLUS
J11_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
J11_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCPLUS,VREFDQ:LDO,VREFCA:LDO,XDP_CPU:BPM,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U3690	CRITICAL	TBTROM:BLANK
341S3526	1	IC,EEPROM,Cactus Ridge (V1.2) PIB, J11/J13	U3690	CRITICAL	TBTROM:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3434	1	IC,SMC,PIB,J11	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
341S3527	1	IC,EFI ROM,PIB,J11/J13	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
138S0676	138S0691		ALL	Murata alt to Samsung
371S0709	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
152S1085	152S1307		ALL	Toko alt to Cyntec
152S1462	152S1295		ALL	Toko alt to NEC inductor
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S1493	152S1300		ALL	Coilcraft MA5274 alt to Murata
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
353S3238	353S1428		ALL	Intersil alt to OPA2333
372S0186	372S0185		ALL	NXP alt to Diodes
197S0431	197S0432		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0903	376S0796		ALL	Fairchild alt to Siliconix
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0333	998-4435		ALL	Sanyo alt to Kemet
128S0357	998-4435		ALL	Sanyo High Voltage Polymer alt
998-4715	998-4435		ALL	Kemet Rectangular Design alt
998-4716	998-4435		ALL	Kemet Flute Design alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC9E,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZ
337S4296	1	IVB,QC9B,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QBTP,ES2,K0,1.5,17W,2+2,0.95,4M,ULVBGA	U1000	CRITICAL	CPU:1.5GHZTDP
337S4299	1	IVB,QC9E,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG	U1000	CRITICAL	CPU:1.7GHZTDP
337S4296	1	IVB,QC9B,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:2.0GHZTDP
337S4297	1	IVB,QC9C,QS,L1,1.9,17W,2+2,1.15,4M,ULVBG	U1000	CRITICAL	CPU:1.9GHZ
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1TDP
338S1108	1	IC,TBT,CR-4C,LP,ES3,288 FCBGA,12X12MM	U3600	CRITICAL	TBT
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,DDR3L-1600,GEMMA,78P FPGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,D35,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,C-DIE,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB

607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	
946-3116	1	MLB,DYMAX UV EB 0.22 GRAM,K78	GLUE	CRITICAL	

PD Module Parts

806-3706	1	CAN,TOPSIDE,COVER,ALT,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN,TOPSIDE,FENCE,ALT,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3214	1	CAN,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	

SYNC_MASTER=J11_MLB_NON_POR SYNC_DATE=11/09/2011

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BOM Configuration

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F (Need 6 TPs)	36 41
TRUE	WIFI_EVENT_L	36 40 41
TRUE	PCIE_AP_R2D_N	36 68
TRUE	PCIE_AP_R2D_P	36 68
TRUE	PCIE_CLK100M_AP_N	16 36 68
TRUE	PCIE_CLK100M_AP_P	16 36 68
TRUE	USB_BT_CONN_P	36 67
TRUE	USB_BT_CONN_N	36 67
TRUE	PCIE_AP_D2R_P	16 36 68
TRUE	PCIE_AP_D2R_N	16 36 68
TRUE	PCIE_WAKE_L	17 36
TRUE	AP_RESET_CONN_L	36
TRUE	AP_CLKREQ_O_L	36
TRUE	PP3V3_S3RS4_BT_F	36

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST (Need 5 TPs)

TRUE	PP3V3_S0_SSD_FLT	37
TRUE	SATA_SSD_D2R_P	37 67
TRUE	SATA_SSD_D2R_N	37 67
TRUE	SATA_SSD_R2D_N	37 67
TRUE	SATA_SSD_R2D_P	37 67
TRUE	SMC_OOB1_RX_L	37 40
TRUE	SMC_OOB1_TX_L	37 40 41
TRUE	PCIE_SSD_D2R_N<1>	8 37 65
TRUE	PCIE_SSD_D2R_P<1>	8 37 65
TRUE	PCIE_SSD_R2D_N<1>	37 65
TRUE	PCIE_SSD_R2D_P<1>	37 65
TRUE	PCIE_CLK100M_SSD_N	16 37 65
TRUE	PCIE_CLK100M_SSD_P	16 37 65
TRUE	SSD_CLKREQ_L	16 37
TRUE	SSD_RESET_L	25 37
TRUE	SATA_PCIE_SEL	37
TRUE	SSD_P3V3S0_EN	37

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	7 39
TRUE	=PP3V3_S0_AUDIO	7 39
TRUE	=PP3V3R1V5_S0_AUDIO	7 39
TRUE	SYS_ONEWIRE	39 40
TRUE	SMC_BC_ACOK	39 40 41
TRUE	=USB_PWR_EN	38 39 61
TRUE	=I2C_LIO_SDA	39 43
TRUE	=I2C_LIO_SCL	39 43
TRUE	=I2C_MIKEY_SCL	39 43
TRUE	=I2C_MIKEY_SDA	39 43
TRUE	AUD_IPHS_SWITCH_EN	25 39
TRUE	AUD_IP_PERIPHERAL_DET	18 39
TRUE	AUD_I2C_INT_L	18 39
TRUE	AUD_GPIO_3	39 50
TRUE	SPKRAMP_INR_N	39 50 71
TRUE	SPKRAMP_INR_P	39 50 71
TRUE	USB_EXTB_N	24 39 67
TRUE	USB_EXTB_P	24 39 67
TRUE	USB_CAMERA_N	18 39 67
TRUE	USB_CAMERA_P	18 39 67
TRUE	HDA_SDOUT	16 39 68
TRUE	HDA_BIT_CLK	16 39 68
TRUE	HDA_SDIN0	16 39 68
TRUE	USB_EXTB_OC_L	23 39
TRUE	HDA_RST_L	16 39 68
TRUE	HDA_SYNC	16 39 68
TRUE	USB3_EXTB_RX_RC_N	39 67
TRUE	USB3_EXTB_RX_RC_P	39 67
TRUE	USB3_EXTB_TX_C_P	39 67
TRUE	USB3_EXTB_TX_C_N	39 67

(Need to add 5 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	7 42
TRUE	=PP5V_S0_LPCPLUS	7 42
TRUE	LPC_AD<3..0>	16 40 42 68
TRUE	SPI_ALT_MOSI	42
TRUE	SPI_ALT_MISO	42
TRUE	LPC_FRAME_L	16 40 42 68
TRUE	PM_CLKRUN_L	17 40 42
TRUE	SMC_TMS	40 41 42
TRUE	LPCPLUS_RESET_L	25 42 68
TRUE	SMC_TDO	40 41 42
TRUE	TP_SMC_TRST_L	42
TRUE	TP_SMC_MD1	42
TRUE	SMC_TX_L	40 41 42
TRUE	LPC_CLK33M_LPCPLUS	25 42 68
TRUE	SPIROM_USE_MLB	19 42 49
TRUE	SPI_ALT_CLK	42
TRUE	SPI_ALT_CS_L	42
TRUE	LPC_SERIRQ	16 40 42
TRUE	LPC_PWRDWN_L	17 25 40 42
TRUE	SMC_TDI	40 41 42
TRUE	SMC_TCK	40 41 42
TRUE	SMC_RESET_L	40 41 42 52
TRUE	SMC_ROMBOOT	41 42
TRUE	SMC_RX_L	40 41 42
TRUE	LPCPLUS_GPIO	19 42

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	7 47
TRUE	FAN_RT_TACH	47
TRUE	FAN_RT_PWM	47

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	SMC_PME_S4_WAKE_L	40 41 48
TRUE	PP5V_TPAD_FILT	48
TRUE	=PP3V42_G3H_TPAD	7 48
TRUE	PP3V3_TPAD_CONN	48
TRUE	USB_TPAD_P	48 67
TRUE	USB_TPAD_N	48 67
TRUE	=I2C_TPAD_SDA	43 48
TRUE	=I2C_TPAD_SCL	43 48
TRUE	SMC_ONOFF_L	40 41 48
TRUE	SMC_LID	40 41 48 51
TRUE	SMC_TPAD_RST_L	41 48

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	7 51 (Need 4 TPs)
TRUE	=PP5V_S3_LIO_CONN	7 51 (Need 3 TPs)

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	50 51 71
TRUE	SPKRAMP_ROUT_N	50 51 71

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	51 52 (Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	43 51
TRUE	=SMBUS_BATT_SDA	43 51
TRUE	SYS_DETECT_L	51

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	62 64 (Need 2 TPs)
TRUE	PP3V3_SW_LCD	62 (Need 2 TPs)
TRUE	I2C_TCON_SDA_R	62
TRUE	LED_RETURN_6	62 64
TRUE	LED_RETURN_5	62 64
TRUE	LED_RETURN_4	62 64
TRUE	LED_RETURN_3	62 64
TRUE	LED_RETURN_2	62 64
TRUE	LED_RETURN_1	62 64
TRUE	DP_INT_HPD_CONN	62
TRUE	DP_INT_AUX_CH_C_N	62 65
TRUE	DP_INT_AUX_CH_C_P	62 65
TRUE	DP_INT_ML_F_P<0>	62 65
TRUE	DP_INT_ML_F_N<0>	62 65
TRUE	I2C_TCON_SCL_R	62

(Need to add 5 GND TPs)

J5715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_FB	48
TRUE	KBDLED_ANODE	48

(Need to add 2 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST

TRUE	SMC_LID_R	51
TRUE	=PP3V42_G3H_HALL	7 51

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	7 51
TRUE	PPVIN_SW_TBTBST	7 35
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	7
TRUE	PPDCIN_G3H	7
TRUE	PP3V42_G3H	7
TRUE	PPVRTC_G3H	7
TRUE	PP5V_S5	7
TRUE	PP5V_SUS	7
TRUE	PP3V3_S5	7 71
TRUE	PP3V3_SUS	7
TRUE	PP3V3_S3	7
TRUE	PP1V8_S0	7
TRUE	PP3V3_S0	7 71
TRUE	PP1V5_S3	7 66
TRUE	PP1V5_S3RS0	7 66
TRUE	PP1V5_S0	7
TRUE	PP1V05_S0	7
TRUE	PPVTTDDR_S3	7
TRUE	PP0V75_S0_DDRVTT	7
TRUE	PPVCCSA_S0_CPU	7
TRUE	PP1V05_SUS	7
TRUE	PP15V_TBT	7
TRUE	PP3V3_TBTLC	7 (Need to add 27 GND TPs)
TRUE	PP1V05_TBTLC	7 35
TRUE	PP1V05_S0_PCH_VCCADPLL	7
TRUE	PPVCORE_S0_CPU	7
TRUE	PPVCORE_S0_AXG	7
TRUE	PP1V5_S3_CPU_VCCDQ	7
TRUE	PP1V05_S0_CPU_VCCPQE	7
TRUE	PP1V8_S0_CPU_VCCPLL_R	7
TRUE	PP1V05_TBTCIO	7
TRUE	PPBUS_S5_HS_OTHER_ISNS	7
TRUE	PPDCIN_G3H_ISOL	7
TRUE	PP5V_S3	7
TRUE	PP5V_S0	7
TRUE	PP3V3_S4	7

NO_TEST Nets

POWER SIGNALS

16&4	TRUE	VCCSAS0_SREF 53
16&2	TRUE	VCCSAS0_SET1_R 53
16&4	TRUE	VCCSAS0_SET0 53
16&4	TRUE	VCCSAS0_SET1 53

NO_TEST

17	TP_CRT_IG_BLUE	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
	TP_LVDS_IG_CTRL_CLK	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
	TP_LVDS_IG_CTRL_DATA	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
	TP_PCH_LVDS_VBG	TRUE / MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	TRUE / MAKE_BASE=TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	TRUE / MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
16	TP_CLINK_CLK	TRUE / MAKE_BASE=TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	TRUE / MAKE_BASE=TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	TRUE / MAKE_BASE=TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP
17	TP_SDVO_TVCLKINN	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTP
23	TP_XDP_PCH_OBSFN_A<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

	NC_EDP_TXP<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_P<0..3> 9
	NC_EDP_TXN<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_N<0..3> 9
	NC_EDP_AUXP MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_P
	NC_EDP_AUXN MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_N
	NC_CPU_THERMDA MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDA
	NC_CPU_THERMDC MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDC
	NC_CPU_RSVD<30..45> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<8..27>
	NC_PEG_R2D_CP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_P<15..2> 9
	NC_PEG_R2D_CN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_N<15..2> 9
	NC_PEG_D2RP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_P<15..2> 9
	NC_PEG_D2RN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_N<15..2> 9

16	TP_PCIE_CLK100M_PE4N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
16	TP_PCIE_CLK100M_PE4P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
	TP_PCIE_CLK100M_PE5N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
	TP_PCIE_CLK100M_PE5P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
	TP_PCIE_CLK100M_PE6N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
	TP_PCIE_CLK100M_PE6P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
	TP_PCIE_CLK100M_PE7N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
	TP_PCIE_CLK100M_PE7P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
	TP_PSOC_P1_3	TRUE / MAKE_BASE=TRUE	NC_PSOC_P1_3
	TP_SATA_B_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_B_D2RN
	TP_SATA_B_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_B_D2RP
	TP_SATA_B_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_B_R2D_CN
	TP_SATA_B_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_B_R2D_CP
16	TP_SATA_D_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
	TP_PCH_TP18	TRUE / MAKE_BASE=TRUE	NC_PCH_TP18
	TP_PCH_TP17	TRUE / MAKE_BASE=TRUE	NC_PCH_TP17
	TP_PCH_TP16	TRUE / MAKE_BASE=TRUE	NC_PCH_TP16
	TP_PCH_TP15	TRUE / MAKE_BASE=TRUE	NC_PCH_TP15
	TP_PCH_TP14	TRUE / MAKE_BASE=TRUE	NC_PCH_TP14
	TP_PCH_TP13	TRUE / MAKE_BASE=TRUE	NC_PCH_TP13
	TP_PCH_TP12	TRUE / MAKE_BASE=TRUE	NC_PCH_TP12
	TP_PCH_TP10	TRUE / MAKE_BASE=TRUE	NC_PCH_TP10
	TP_PCH_TP9	TRUE / MAKE_BASE=TRUE	NC_PCH_TP9
	TP_PCH_TP8	TRUE / MAKE_BASE=TRUE	NC_PCH_TP8
	TP_PCH_TP7	TRUE / MAKE_BASE=TRUE	NC_PCH_TP7
	TP_PCH_TP6	TRUE / MAKE_BASE=TRUE	NC_PCH_TP6
	TP_PCH_TP5	TRUE / MAKE_BASE=TRUE	NC_PCH_TP5
	TP_PCH_TP4	TRUE / MAKE_BASE=TRUE	NC_PCH_TP4
	TP_PCH_TP3	TRUE / MAKE_BASE=TRUE	NC_PCH_TP3
	TP_PCH_TP2	TRUE / MAKE_BASE=TRUE	NC_PCH_TP2
	TP_PCH_TP1	TRUE / MAKE_BASE=TRUE	NC_PCH_TP1
8	TP_LVDS_IG_B_CLKN	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	TRUE / MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

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"G3Hot" (Always-Present) Rails

52 =PPBUS_G3H → PPBUS_G3H (6 51)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT 64
- =PPBUS_S0_VSENSE 44
- =PPVIN_SW_TBTBST 35
- =PPVIN_S5_HS_COMPUTING_ISNS_R 8
- =PPVIN_S5_HS_OTHER_ISNS_R 45

35 6 PPVIN_SW_TBTBST (VOLTAGE=12.8V)

8 =PPVIN_S5_HS_COMPUTING_ISNS → PPBUS_S5_HS_COMPUTING_ISNS (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP 56 57
- =PPVIN_S3_DDRREG 55
- =PPVIN_S0_CPUVCCIOS0 58
- =PPVIN_S0_VCCSAS0 53
- =PPVIN_S0_CPUAXG 57

45 =PPVIN_S5_HS_OTHER_ISNS → PPBUS_S5_HS_OTHER_ISNS (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
- =PPVIN_S5_P5VP3V3 54

51 =PP18V5_DCIN_ISOL → PPDCIN_G3H_ISOL (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR_ISOL 52
- =PPDCIN_S5_VSENSE 44

51 6 =PP18V5_DCIN_CONN → PPDCIN_G3H (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 52

51 =PP3V42_G3H_REG → PP3V42_G3H (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS 6 42
- =PP3V3_S5_SMC 40 41
- =PP3V42_G3H_HALL 6 51
- =PP3V42_G3H_CHGR 52
- =PP3V42_G3H_PWRCTL 61
- =PP3V42_G3H_SMBUS_SMC_BSA 43
- =PP3V42_G3H_SMCUSBMUX 38
- =PP3V42_G3H_TPAD 6 48
- =PPVIN_S5_SMCVREF 41
- =PPVBAT_G3H_SYSCLK 25
- =PP3V42_G3H_ONEWIRE 6 39

25 =PPVRTC_G3_OUT → PPVRTC_G3H (6)
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 16 17 20

5V Rails

54 =PP5V_S5_LDO → PP5V_S5 (6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET 60
- =PP5V_S5_P5VSUSFET 60
- =PP5V_S5_TPAD 48

60 =PP5V_SUS_FET → PP5V_SUS (6)
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_SUS_PCH 22

54 =PP5V_S3_REG → PP5V_S3 (6)
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_AUDIO_AMP 50
- =PP5V_S3_DDRREG 55
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_P5VS0FET 60
- =PP5V_S3_RTUSB 38
- =PP5V_S3_LIO_CONN 6 51

60 =PP5V_S0_FET → PP5V_S0 (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_BKL 64
- =PP5V_S0_CPUIMVP 56
- =PP5V_S0_CPUVCCIOS0 58
- =PP5V_S0_FAN 6 47
- =PP5V_S0_LPCPLUS 6 42
- =PP5V_S0_VCCSA 53
- =PP5V_S0_PCH 22 25
- =PP5V_S0_VMON 61
- =PP5V_S0_KBDLED 48

3.3V Rails

54 =PP3V3_S5_REG → PP3V3_S5 (6 71)
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S5_XDP 23
- =PP3V3_S0_P3V3S0FET 60
- =PP3V3_S3_P3V3S3FET 60
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S5_LCD 62
- =PP3V3_S5_PCH 17
- =PP3V3_S5_PCHPWRGD 25
- =PP3V3_S5_SMCBATLOW 41
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_SYSCLK 25
- =PP3V3_S5_VMON 61
- =PP3V3_S5_PWRCTL 61
- =PP3V3_S5_PCH_GPIO 19
- =PP3V3_S5_P3V3SUSFET 60
- =PP3V3_S4_P3V3S4FET 60
- =PP3V3_S4_TBTAPWRSW 63

60 =PP3V3_S4_FET → PP3V3_S4 (6)
MIN_LINE_WIDTH=0.60MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_SMC 41
- =PP3V3_S4_TPAD 48
- =PP3V3_S4_BT 36

60 =PP3V3_SUS_FET → PP3V3_SUS (6)
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_ROM 49
- =PP3V3_SUS_PCH_VCCSUS 20 22
- =PP3V3_SUS_PCH_GPIO 16 17 18 19
- =PP3V3_SUS_PCH 22
- =PP3V3_SUS_PWRCTL 61
- =PP3V3_SUS_P1V05SUSLDO 59
- =PP3V3_SUS_SMC 41
- =PP3V3_SUS_PCH_VCC_SPI 20 22
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22

=PP3V3_S4_TBTAPWR → PP3V3_SW_TBTAPWR (63)
MIN_LINE_WIDTH=0.38 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20 MM MAKE_BASE=TRUE
- =PP3V3_S4_TBT 33 34 35

60 =PP3V3_S3_FET → PP3V3_S3 (6)
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3_BT 36
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_SMBUS_SMC_A_S3 43
- =PP3V3_S3_SMBUS_SMC_MGMT 43
- =PP3V3_S3_USB_HUB 8 24
- =PP3V3_S3_USB_RESET 24
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 36
- =PP3V3_S3_WLANISNS 45
- =PP3V3_S3_PCH_GPIO 18 25
- =PP3V3_S3_USBMUX 24
- =PP3V3_S3_1V5S3ISNS 45
- =PP3V3_S3_DBGLEDS 51

60 =PP3V3_S0_FET → PP3V3_S0 (6 71)
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_CPUVCCIOISNS 44
- =PP3V3_S0_AUDIO 6 39
- =PP3V3_S0_BKL_VDDIO 64
- =PP3V3_S0_HS_COMPUTING_ISNS 45
- =PP3V3_S0_CPUTHMSNS 46
- =PP3V3_S0_CPU_VCCIO_SEL 12
- =PP3V3_S0_DP_DDC 8
- =PP3V3_S0_FAN 47
- =PP3V3_S0_P3V3TBTFET 35
- =PP3V3_S0_P1V8S0 59
- =PP3V3_S0_PCH 16 22
- =PP3V3_S0_PCH_GPIO 16 17 18 19 25 35
- =PP3V3_S0_SATAMUX 37
- =PP3V3_S0_PCH_VCC3_3 20 22
- =PP3V3_S0_HS_OTHER_ISNS 45
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PWRCTL 61
- =PP3V3_S0_RSTBUF 25
- =PP3V3_S0_SB_PM 25
- =PP3V3_S0_SMBUS_PCH 43
- =PP3V3_S0_SMBUS_SMC_0_S0 43
- =PP3V3_S0_SMBUS_SMC_B_S0 43
- =PP3V3_S0_SMC 41
- =PP3V3_S0_SSD 37
- =PP3V3_S0_HDDISNS 45
- =PP3V3_S0_VMON 61
- =PP3V3_S0_P1V5S0 59
- =PP3V3_S0_TBTPWRCTL 35
- =PP3V3_S0_3V3S0ISNS 44
- =PP3V3_S0_P1V05S0LDO 59
- =PP3V3_S0_IMVPISNS 44
- =PP3V3_S0_XDP 23
- =PP3V3_S0_BKLTISNS 45
- =PP3V3_S0_SYSCLKGEN 25
- =PP3V3_S0_SAISNS 44
- =PP3V3_S0_PCH_STRAPS 19

1.8V/1.5V/1.2V/1.05V Rails

59 =PP1V8_S0_REG → PP1V8_S0 (6)
2A max supply
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
- =PP1V8_S0_P1V05S0LDO 59
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 25
- =PP1V8_S0_P1V5S0 59

55 =PPDDR_S3_REG → PP1V5_S3 (6 66)
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27 28 32
- =PP1V5_S3_MEM_B 29 30 32
- =PP1V5_S3_P1V5S3RS0_FET 60
- =PPVIN_S0_DDRREG_LDO 55
- =PPDDR_S3_MEMVREF 31

60 =PP1V5_S3RS0_FET → PP1V5_S3RS0 (6 66)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR 10 12 15 26
- =PP1V5_S3RS0_VMON 61

59 =PP1V5_S0_REG → PP1V5_S0 (6)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP3V3R1V5_S0_AUDIO 6 39
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 25

55 31 =PPVTT_S3_DDR_BUF → PPVTTDDR_S3 (6)
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

55 =PPVTT_S0_DDR_LDO → PP0V75_S0_DDRVTT (6)
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A 32
- =PP0V75_S0_MEM_VTT_B 32
- =PPVTT_S0_VTTCLAMP 26

53 =PPVCCSA_S0_REG → PPVCCSA_S0_CPU (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU 12 15
- =PPVCCSA_S0_VSENSE 44

59 =PP1V05_SUS_LDO → PP1V05_SUS (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 23

58 =PPCPUVCCIO_S0_REG → PP1V05_S0 (6)
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_CPU_VCCIO 9 10 12 14
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_VMON 61
- =PPVCCIO_S0_CPUIMVP 56
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_SMC 41
- =PP1V05_S0_P1V05TBTFET 35

TBT Rails (off when no cable)

35 =PP15V_TBT_REG → PP15V_TBT (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE
- =PPHV_SW_TBTAPWRSW 63

35 =PP3V3_TBTLC_FET → PP3V3_TBTLC (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_TBT_CLK 25
- =PP3V3_TBTLC_RTR 33 34 35
- =PP3V3_TBT_PCH_GPIO 19

35 =PP1V05_TBTLC_FET → PP1V05_TBTLC (6 35)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTLC_RTR 34

35 =PP1V05_TBTCIO_FET → PP1V05_TBTCIO (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_TBTCIO_RTR 34

1V05 S0 LDO

59 =PP1V05_S0_LDO → PP1V05_S0_PCH_VCCADPLL (6)
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL 22

Chipset "VCore" Rails

57 =PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 9 12 14
- =PPCPUVCORE_S0_VSENSE 44

57 =PPVCORE_S0_AXG_REG → PPVCORE_S0_AXG (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG 9 12 15
- =PPGFXVCORE_S0_VSENSE 44

15 12 =PP1V5_S3_CPU_VCCDQ → PP1V5_S3_CPU_VCCDQ (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

14 12 =PP1V05_S0_CPU_VCCPQE → PP1V05_S0_CPU_VCCPQE (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R → PP1V8_S0_CPU_VCCPLL_R (6)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE
Power Aliases

Apple Inc.

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CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905 STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914 STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915 STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
870-1938

USB/SD Card Pogo

CRITICAL
ZS0907
POGO-2.0OD-2.95H-K86-K87
870-1940

Can Slots

SL0901 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0902 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x MDP connector
SL0903 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	SL0904 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	2x USB connector
SL0905 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0906 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x TBT pin diodes
SL0907 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	SL0908 TH-NSP, SL-1.1X0.45-1.4x0.75, 998-3975	2x TBT chip
SL0909 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	SL0910 TH-NSP, SL-1.1X0.4-1.4x0.7, 998-2691	2x CPU Vcore

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

CPU signals

MEMVTT_EN (MAKE_BASE=TRUE) — =DDRVTT_EN

DP_TBTSNK0_AUXCH_C_P — DPA_IG_AUX_CH_P
DP_TBTSNK0_AUXCH_C_N — DPA_IG_AUX_CH_N

PCIE_CLK100M_ENET_N — NC_PCIE_CLK100M_ENETN
PCIE_CLK100M_ENET_P — NC_PCIE_CLK100M_ENETP
PCIE_EXCARD_D2R_N — NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P — NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N — NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P — NC_PCIE_EXCARD_R2D_CP
PCIE_CLK100M_EXCARD_N — NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P — NC_PCIE_CLK100M_EXCARDP

PEG_CLK100M_P — NC_PEG_CLK100MP
PEG_CLK100M_N — NC_PEG_CLK100MN

TP_PCH_CLKOUT_DPN — DPLL_REF_CLK_N — DPLL_REF_CLKN
TP_PCH_CLKOUT_DPP — DPLL_REF_CLK_P — DPLL_REF_CLKP

MEM_A_CLK_P<1> — TP_MEM_A_CLKP<1>
MEM_A_CLK_N<1> — TP_MEM_A_CLKN<1>

MEM_B_CLK_P<1> — TP_MEM_B_CLKP<1>
MEM_B_CLK_N<1> — TP_MEM_B_CLKN<1>

USB_EXTC_P — NC_USB_EXTCP
USB_EXTC_N — NC_USB_EXTCN
USB3_EXTC_RX_P — NC_USB3_EXTC_RXP
USB3_EXTC_RX_N — NC_USB3_EXTC_RXN
USB3_EXTC_TX_P — NC_USB3_EXTC_TXP
USB3_EXTC_TX_N — NC_USB3_EXTC_TXN
USB3_EXTD_RX_P — NC_USB3_EXTD_RXP
USB3_EXTD_RX_N — NC_USB3_EXTD_RXN
USB3_EXTD_TX_P — NC_USB3_EXTD_TXP
USB3_EXTD_TX_N — NC_USB3_EXTD_TXN
USB_EXTD_EHCI_P — NC_USB_EXTD_EHCIP
USB_EXTD_EHCI_N — NC_USB_EXTD_EHCIN

TBT_B_R2D_C_P<0> — NC_TBT_B_R2D_CP<0>
TBT_B_R2D_C_N<0> — NC_TBT_B_R2D_CN<0>
TBT_B_R2D_C_P<1> — NC_TBT_B_R2D_CP<1>
TBT_B_R2D_C_N<1> — NC_TBT_B_R2D_CN<1>
TBT_B_D2R_P<0> — NC_TBT_B_D2RP<0>
TBT_B_D2R_N<0> — NC_TBT_B_D2RN<0>
TBT_B_D2R_P<1> — NC_TBT_B_D2RP<1>
TBT_B_D2R_N<1> — NC_TBT_B_D2RN<1>
TBT_B_LSTX — NC_TBT_B_LSTX

DP_TBTPB_ML_C_P<1> — NC_DP_TBTPB_ML_CP<1>
DP_TBTPB_ML_C_N<1> — NC_DP_TBTPB_ML_CN<1>
DP_TBTPB_ML_C_P<3> — NC_DP_TBTPB_ML_CP<3>
DP_TBTPB_ML_C_N<3> — NC_DP_TBTPB_ML_CN<3>

PCIE_CLK100M_FW_N — NC_PCIE_CLK100M_FWN
PCIE_CLK100M_FW_P — NC_PCIE_CLK100M_FWP
=PEG_D2R_P<1..0> — PCIE_SSD_D2R_P<1..0>
=PEG_D2R_N<1..0> — PCIE_SSD_D2R_N<1..0>
=PEG_R2D_C_P<1..0> — PCIE_SSD_R2D_C_P<1..0>
=PEG_R2D_C_N<1..0> — PCIE_SSD_R2D_C_N<1..0>

PCIE_ENET_D2R_N — NC_PCIE_ENET_D2RN
PCIE_ENET_D2R_P — NC_PCIE_ENET_D2RP
PCIE_ENET_R2D_C_N — NC_PCIE_ENET_R2D_CN
PCIE_ENET_R2D_C_P — NC_PCIE_ENET_R2D_CP
PCIE_FW_D2R_N — NC_PCIE_FW_D2RN
PCIE_FW_D2R_P — NC_PCIE_FW_D2RP
PCIE_FW_R2D_C_N — NC_PCIE_FW_R2D_CN
PCIE_FW_R2D_C_P — NC_PCIE_FW_R2D_CP

=PP3V3_S5_DP_DDC
R0920 2.2K 5% 1/20W MF 201
R0921 2.2K 5% 1/20W MF 201
R0922 2.2K 5% 1/20W MF 201 NOSTUFF
R0923 2.2K 5% 1/20W MF 201 NOSTUFF
DPB_IG_DDC_CLK
DPB_IG_DDC_DATA
TP_DP_IG_D_CTRL_CLK — DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA — DP_IG_D_CTRL_DATA

=PP3V3_S5_DP_DDC
R0924 470K 5% 1/20W MF 0612-1
R0925 470K 5% 1/20W MF 0612-1
DP_TBTSNK0_DDC_CLK — DPA_IG_DDC_CLK
DP_TBTSNK0_DDC_DATA — DPA_IG_DDC_DATA
DP_TBTSNK0_HPD — DPA_IG_HPD

CRITICAL
R0910 0.01 0.5% 1W MF 0612-1
PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
=PPBUS_SW_BKL

CRITICAL
R0954 0.002 1% 1W MF 0612
=PPVIN_S5_HS_COMPUTING_ISNS_R — =PPVIN_S5_HS_COMPUTING_ISNS
ISNS_HS_COMPUTING_N
ISNS_HS_COMPUTING_P

UNUSED SDCARD USB Aliases

=PP3V3_S3_USB_HUB
R0901 10K 5% 1/20W MF 201
R0902 10K 5% 1/20W MF 201
USB_SDCARD_N
USB_SDCARD_P

TBT_B_CIO_SEL
DP_TBTPB_HPD
TBT_B_CONFIG2_RC
TBT_B_CONFIG1_BUF
TBT_B_LSRX
R0916 10K 5% 1/20W MF 201
R0917 10K 5% 1/20W MF 201
R0918 10K 5% 1/20W MF 201
R0919 10K 5% 1/20W MF 201
R0914 10K 5% 1/20W MF 201

XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH — ENET_LOW_PWR_PCH
XDP_DC3_PCH_GPIO19_SATARDRVR_EN — SATARDRVR_EN

MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
RAMCFG3:L R0950 10K 5% 1/20W MF 201
RAMCFG2:L R0951 10K 5% 1/20W MF 201
RAMCFG1:L R0952 10K 5% 1/20W MF 201
RAMCFG0:L R0953 10K 5% 1/20W MF 201

TBT DP Ports

DPB_IG_HPD — DP_TBTSNK1_HPD
TP_DP_IG_C_MLP<3..0> — DP_TBTSNK1_ML_C_P<3..0>
TP_DP_IG_C_MLN<3..0> — DP_TBTSNK1_ML_C_N<3..0>
DPB_IG_AUX_CH_P — DP_TBTSNK1_AUXCH_C_P
DPB_IG_AUX_CH_N — DP_TBTSNK1_AUXCH_C_N
TP_DP_IG_D_HPD — DP_IG_D_HPD
DP_TBTPB_AUXCH_C_P — NC_DP_TBTPB_AUXCH_CP
DP_TBTPB_AUXCH_C_N — NC_DP_TBTPB_AUXCH_CN
R0909 100K 5% 1/20W MF 201
TP_DP_IG_B_MLP<3..0> — DP_TBTSNK0_ML_C_P<3..0>
TP_DP_IG_B_MLN<3..0> — DP_TBTSNK0_ML_C_N<3..0>

NC_PCIE_5_R2D_CP — PCIE_TBT_R2D_C_P<0>
NC_PCIE_6_R2D_CP — PCIE_TBT_R2D_C_P<1>
NC_PCIE_7_R2D_CP — PCIE_TBT_R2D_C_P<2>
NC_PCIE_8_R2D_CP — PCIE_TBT_R2D_C_P<3>
NC_PCIE_5_R2D_CN — PCIE_TBT_R2D_C_N<0>
NC_PCIE_6_R2D_CN — PCIE_TBT_R2D_C_N<1>
NC_PCIE_7_R2D_CN — PCIE_TBT_R2D_C_N<2>
NC_PCIE_8_R2D_CN — PCIE_TBT_R2D_C_N<3>
NC_PCIE_5_D2RP — PCIE_TBT_D2R_P<0>
NC_PCIE_6_D2RP — PCIE_TBT_D2R_P<1>
NC_PCIE_7_D2RP — PCIE_TBT_D2R_P<2>
NC_PCIE_8_D2RP — PCIE_TBT_D2R_P<3>
NC_PCIE_5_D2RN — PCIE_TBT_D2R_N<0>
NC_PCIE_6_D2RN — PCIE_TBT_D2R_N<1>
NC_PCIE_7_D2RN — PCIE_TBT_D2R_N<2>
NC_PCIE_8_D2RN — PCIE_TBT_D2R_N<3>

LVDS Aliases

TP_LVDS_IG_B_CLKP — LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN — LVDS_IG_B_CLK_N
NC_LVDS_IG_B_DATAP<0..3> — LVDS_IG_B_DATA_P<0..3>
NC_LVDS_IG_B_DATAN<0..3> — LVDS_IG_B_DATA_N<0..3>
NC_LVDS_IG_A_DATAP<3> — LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> — LVDS_IG_A_DATA_N<3>
LCD_BKLT_PWM — LVDS_IG_BKL_PWM
LCD_IG_PWR_EN — LVDS_IG_PANEL_PWR
LCD_BKLT_EN — LVDS_IG_BKL_ON

SATA Aliases

Unused SATA ODD Signals

SATA_ODD_R2D_C_P — NC_SATA_ODD_R2DCP
SATA_ODD_R2D_C_N — NC_SATA_ODD_R2DCN
SATA_ODD_D2R_P — NC_SATA_ODD_D2RP
SATA_ODD_D2R_N — NC_SATA_ODD_D2RN

SMC Aliases

Unused SMC Signals

SMC_SYS_LED — NC_SMC_SYS_LED
IR_RX_OUT_RC — NC_IR_RX_OUT_RC

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE — P1V5S3RS0_RAMP_DONE
TP_DDRREG_PGOOD — DDRREG_PGOOD

SYNC_MASTER=K91_MLB
SYNC_DATE=05/15/2016
PAGE TITLE: Signal Aliases

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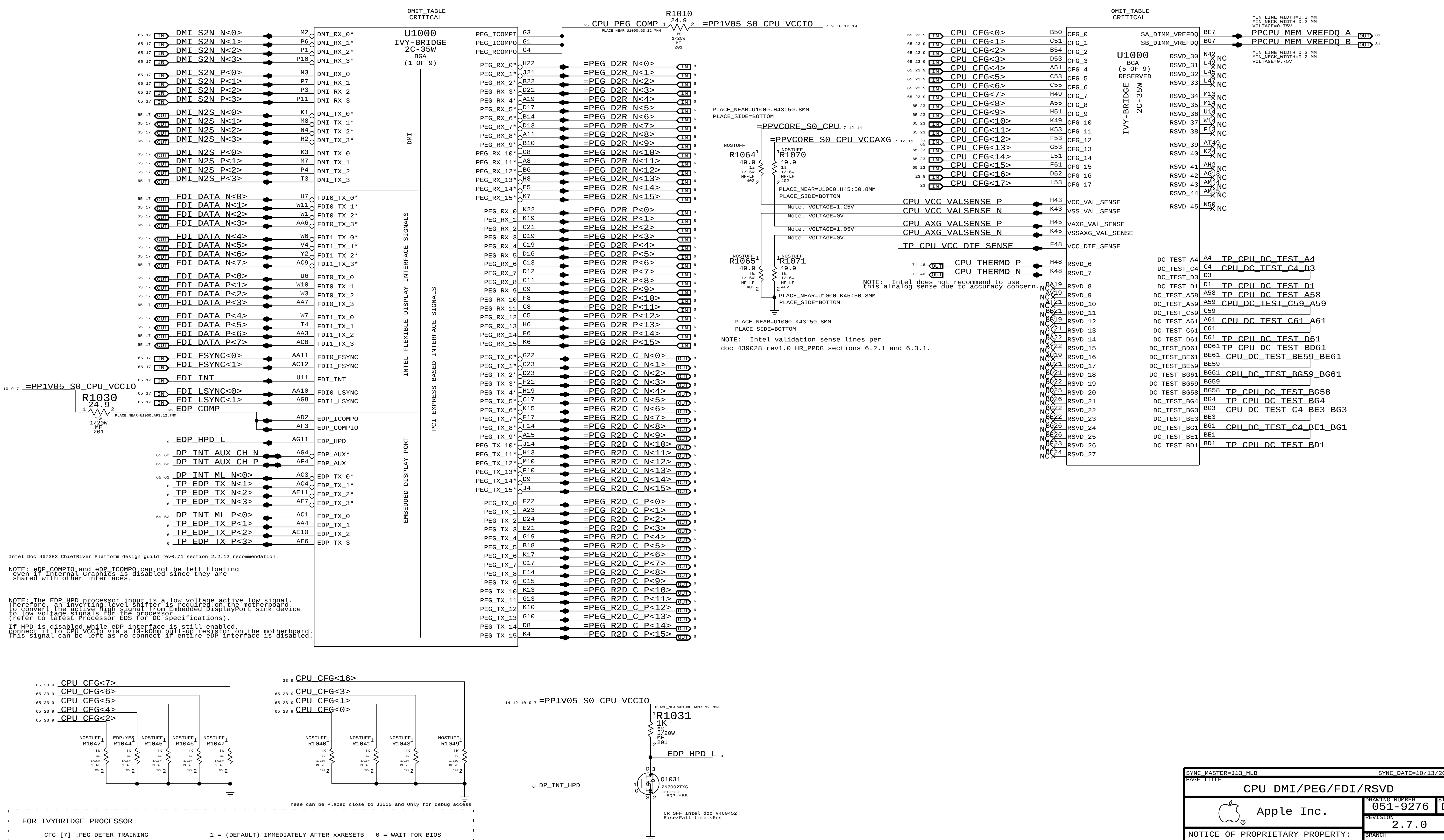
NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU_VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD	00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

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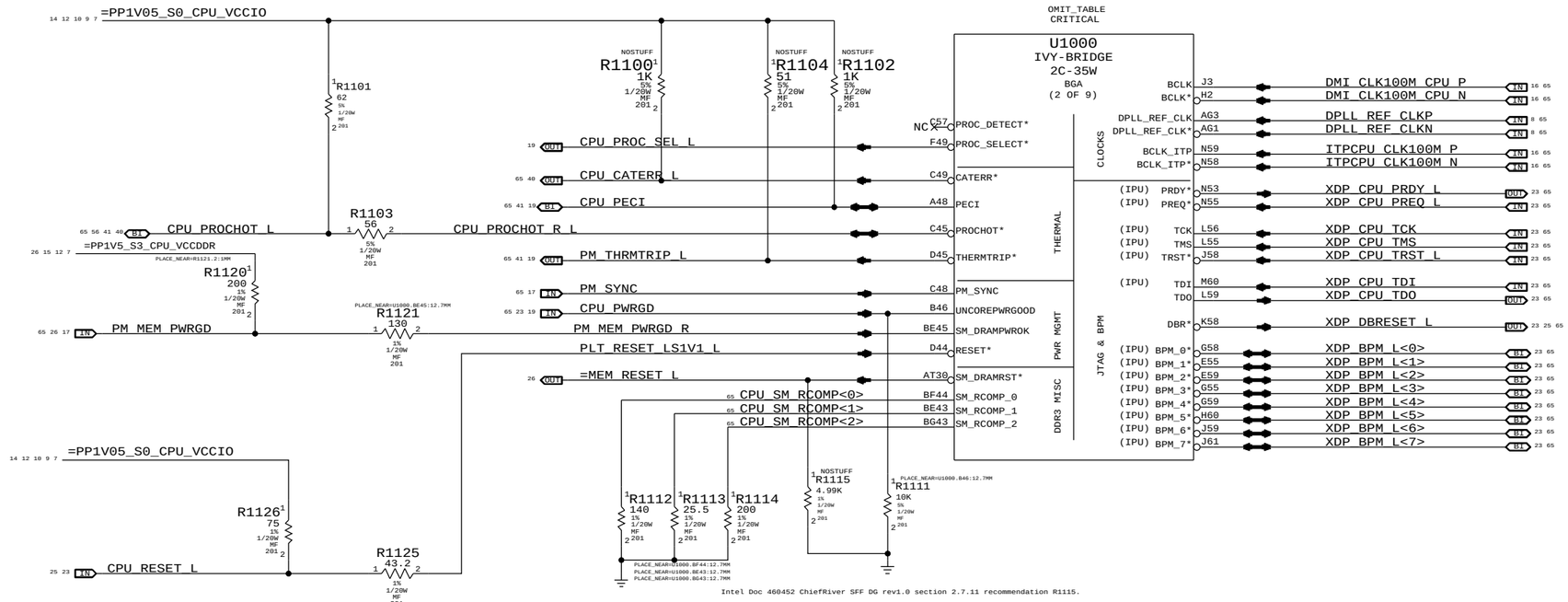

Intel Doc 460452 ChiefRiver SFF DG rev1.0 section 2.7.11 recommendation R1115.

SYNC_MASTER=J13_MLB SYNC_DATE=09/22/2013

PAGE TITLE

CPU CLOCK/MISC/JTAG

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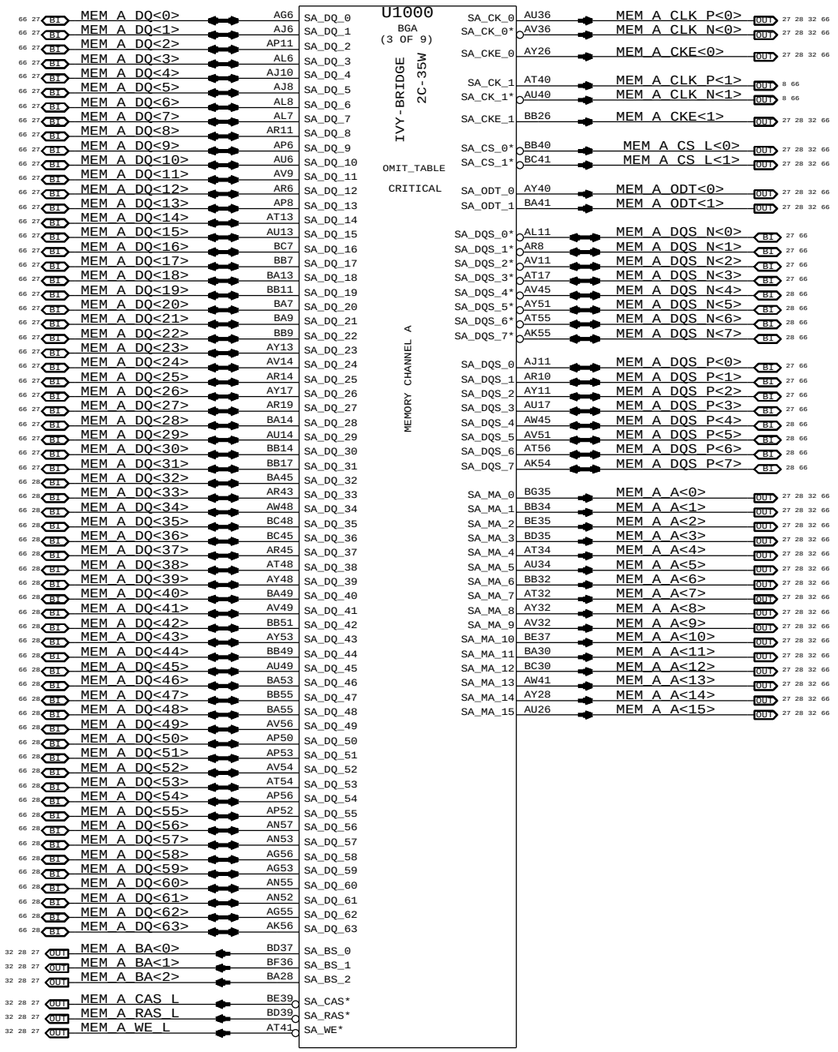

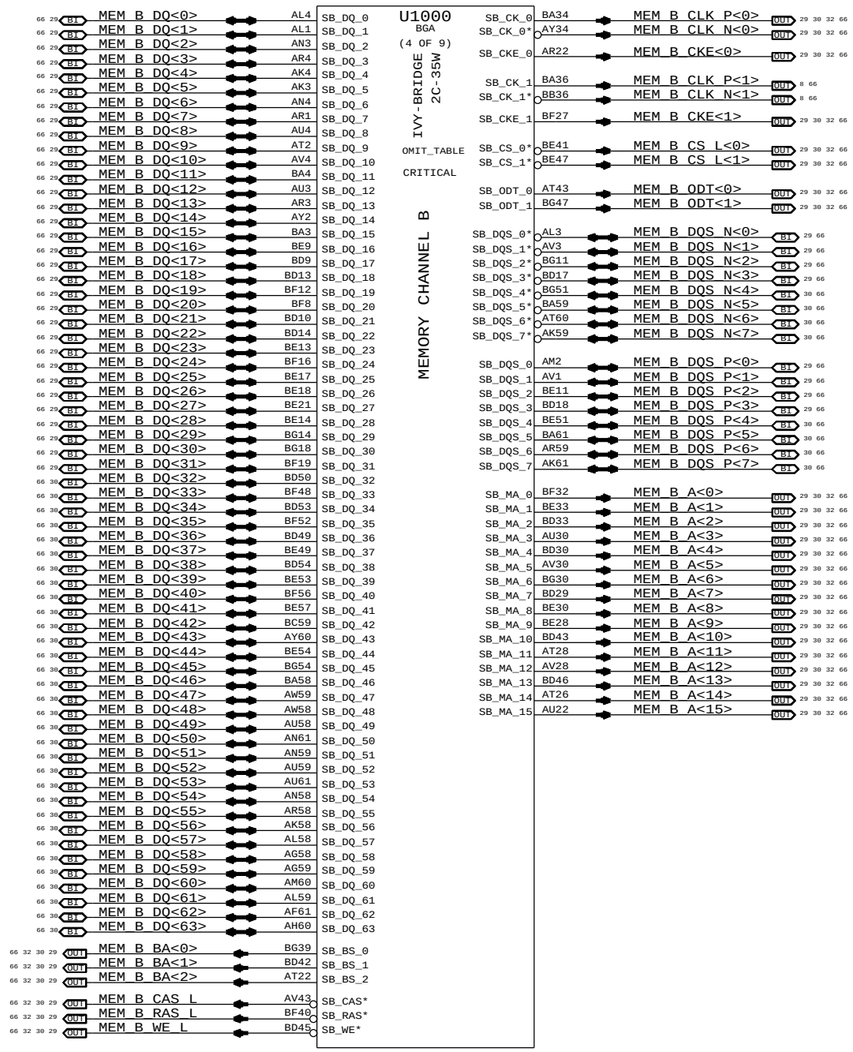

SYNC_DATE=12/13/2010

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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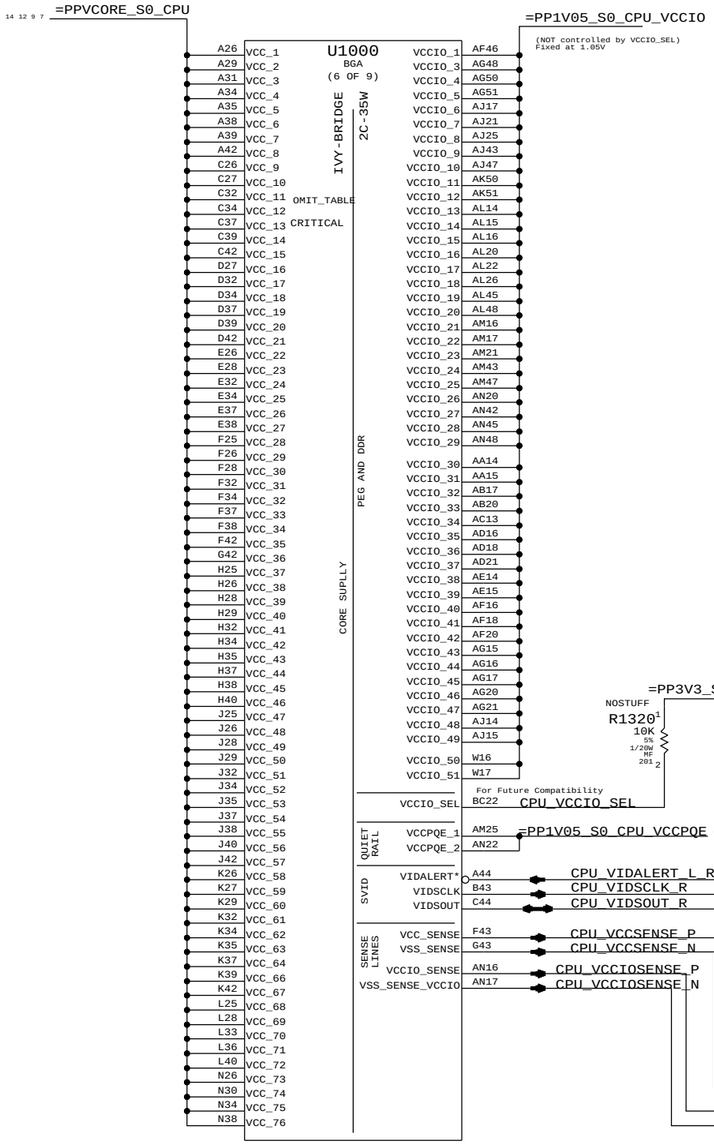

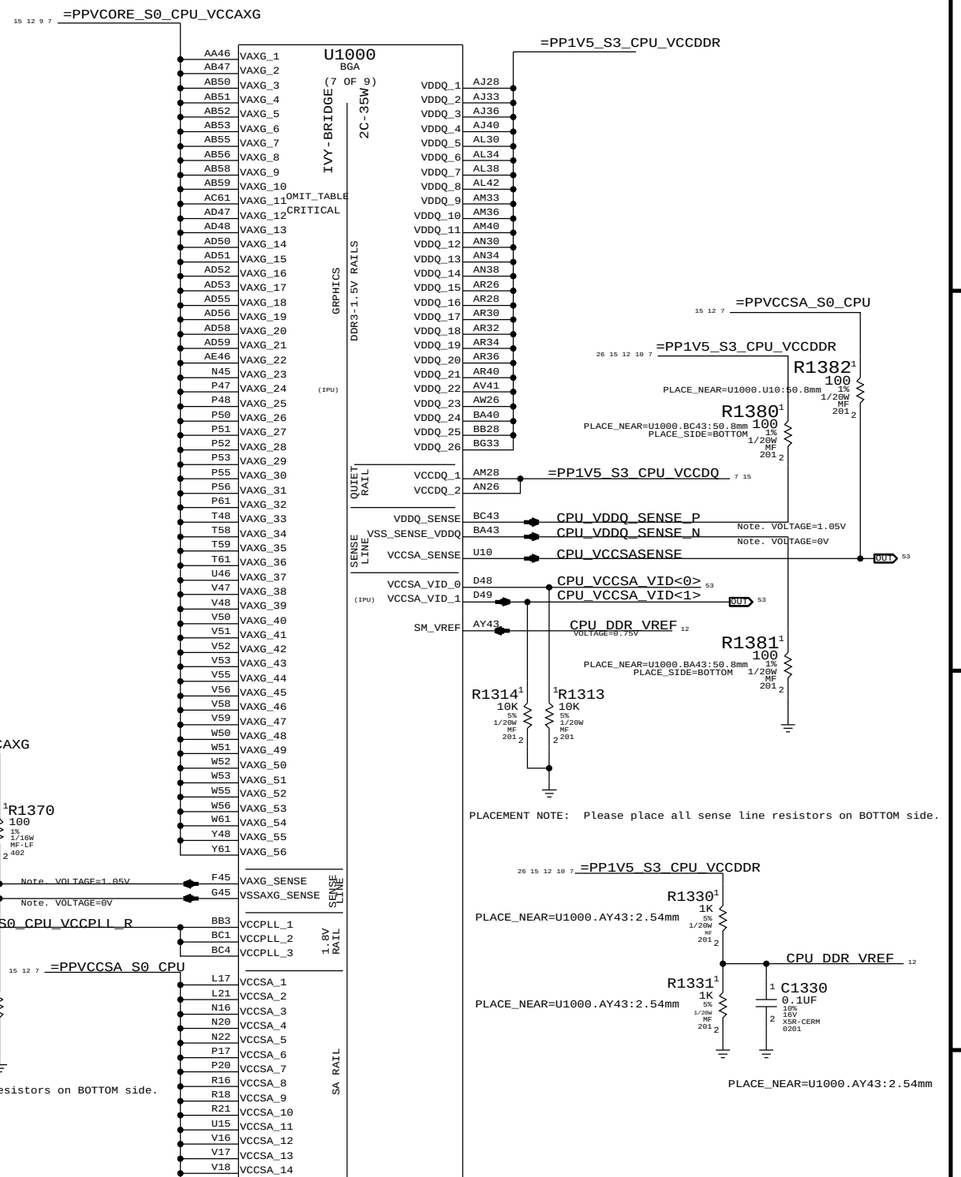

SYNC_MASTER=J11_MLB SYNC_DATE=10/18/2013

PAGE TITLE

CPU POWER

Apple Inc.

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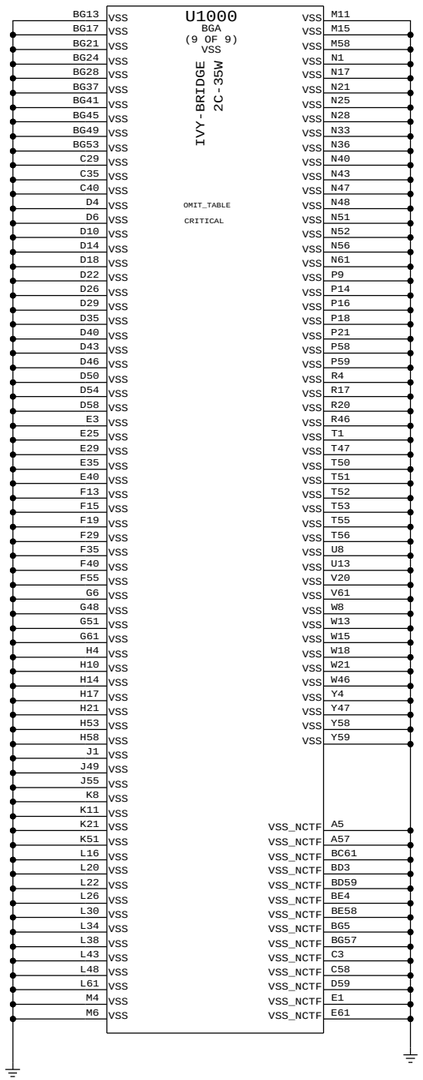

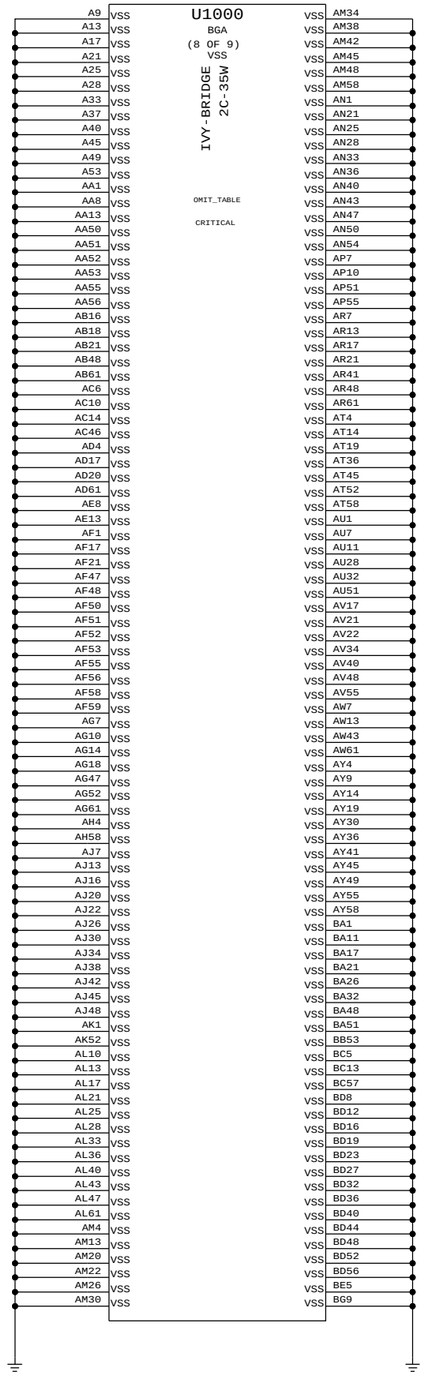

PAGE TITLE

CPU GROUNDS

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

Processor Load Line : -2.9 mOhms

12 9 7 =PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1640 C1641 C1642
1UF 20% 6.3V X6S 0201

C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
1UF 20% 6.3V X6S 0201

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 C1656 C1657 C1658 C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670
10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 C1681 C1682 C1683 C1679
270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
1UF 10% 10V X5R 402

C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C
10UF 20% 6.3V CERM-X5R 0402-1

C167D C167E C167G C167H
270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603

=PP1V05_S0_CPU_VCCPQE 7 12

C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/10W MF-LF 402

=PP1V8_S0_CPU_VCCPLL_R 7 12

C160X C160Y C160Z
1UF 10% 10V X5R 402
270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC_MASTER=J13_MLB SYNC_DATE=08/16/2013

PAGE TITLE: CPU DECOUPLING-I

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VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL

C1700 C1701 C1702 C1703 C1704 C1705 C1706 C1707 C1708 C1709 C1710

1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL

C1711 C1712 C1713 C1714 C1715 C1716

10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL

C1717 C1718 C1719 C1720 C1721 C1722

AXG_ACOUSTICS:NO

22UF 20% 6.3V X5R-CERM1 0603

CRITICAL

C1727 C1728 C1729 C1730 C1731 C1732

AXG_ACOUSTICS:YES

22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1723-C1724):

C1723 C1724 C1725

270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 C1739 C1740 C1741 C1742 C1743 C1744 C1745 C1746 C1747

1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 C1749 C1750 C1751 C1752 C1753 C1754 C1755

10UF 20% 6.3V CERM-X5R 0402-1

C1756

270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702

0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757

1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 C1759 C1760 C1761 C1762

1UF 10% 10V X5R 402

C1763 C1764 C1765 C1766 C1767

10UF 20% 6.3V CERM-X5R 0402-1

C1768

270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)

RTC
SYSCLK_CLK32K_RTC — A19 RTCX1
NC — C19 RTCX2
RTC_RESET_L — F19 RTCRST*
PCH_SRTCRST_L — A23 SRTCRST*
PCH_INTRUDER_L — K22 INTRUDER*
PCH_INTVRMEN_L — C21 INTVRMEN

LPC
FWH0/LAD0 — A37 — LPC_AD_R<0>
FWH1/LAD1 — A39 — LPC_AD_R<1>
FWH2/LAD2 — C39 — LPC_AD_R<2>
FWH3/LAD3 — C37 — LPC_AD_R<3>
FWH4/LFRAME* — K40 — LPC_FRAME_R_L
(IPU) LDRQ0* — H40 — TP_LPC_DREQ0_L
LDRQ1*/GPIO23 (IPU) — F37 — TBT_PWR_EN_PCH (OUT 25)
SERIRQ — Y4 — LPC_SERIRQ
=PP3V3_S0_PCH
R1820 10K 5% 1/20W MF 201

IHDA
HDA_BIT_CLK_R — H35 HDA_BCLK
VSel strap not functional (VCCVRM = 1.8V)
HDA_SYNC_R — H37 HDA_SYNC (IPD-BOOT)
PCH_SPKR — N1 SPKR (IPD-PLTRST#)
HDA_RST_R_L — F35 HDA_RST*
HDA_SDIN0 — D36 HDA_SDIN0 (IPD)
TP_HDA_SDIN1 — B36 HDA_SDIN1 (IPD)
TP_HDA_SDIN2 — C35 HDA_SDIN2 (IPD)
TP_HDA_SDIN3 — A35 HDA_SDIN3 (IPD)
HDA_SDOUT_R — K37 HDA_SDO (IPD-BOOT)
JTAG_ISP_TMS — K35 HDA_DOCK_EN*/GPIO33
ENET_MEDIA_SENSE_RDIV — M35 HDA_DOCK_RST*/GPIO13

JTAG
XDP_PCH_TCK — M17 JTAG_TCK (IPD)
XDP_PCH_TMS — M15 JTAG_TMS (IPU)
XDP_PCH_TDI — U12 JTAG_TDI (IPU)
XDP_PCH_TDO — M12 JTAG_TDO

SPI
SPI_CLK_R — AD12 SPI_CLK
SPI_CS0_R_L — AB8 SPI_CS0*
TP_SPI_CS1_L — AB6 SPI_CS1*
SPI_MOSI_R — W8 SPI_MOSI (IPD-BOOT)
SPI_MISO — Y2 SPI_MISO (IPU)

SATA
SATA0RXN — AN3 — SATA_HDD_D2R_N (IN 37 67)
SATA0RXP — AN1 — SATA_HDD_D2R_P (IN 37 67)
SATA0TXN — AU3 — SATA_HDD_R2D_C_N (OUT 37 67)
SATA0TXP — AU1 — SATA_HDD_R2D_C_P (OUT 37 67)
SATA1RXN — AN6 — SATA_ODD_D2R_N (IN 8)
SATA1RXP — AN8 — SATA_ODD_D2R_P (IN 8)
SATA1TXN — AR3 — SATA_ODD_R2D_C_N (OUT 8)
SATA1TXP — AR1 — SATA_ODD_R2D_C_P (OUT 8)
SATA2RXN — AD4 — TP_SATA_C_D2RN
SATA2RXP — AD2 — TP_SATA_C_D2RP
SATA2TXN — AL3 — TP_SATA_C_R2D_CN
SATA2TXP — AL1 — TP_SATA_C_R2D_CP
SATA3RXN — AD8 — TP_SATA_D_D2RN (6)
SATA3RXP — AD6 — TP_SATA_D_D2RP (6)
SATA3TXN — AG3 — TP_SATA_D_R2D_CN (6)
SATA3TXP — AG1 — TP_SATA_D_R2D_CP (6)
SATA4RXN — AE3 — TP_SATA_E_D2RN (6)
SATA4RXP — AE1 — TP_SATA_E_D2RP (6)
SATA4TXN — AH8 — TP_SATA_E_R2D_CN (6)
SATA4TXP — AH6 — TP_SATA_E_R2D_CP (6)
SATA5RXN — AC3 — TP_SATA_F_D2RN (6)
SATA5RXP — AC1 — TP_SATA_F_D2RP (6)
SATA5TXN — AJ3 — TP_SATA_F_R2D_CN (6)
SATA5TXP — AJ1 — TP_SATA_F_R2D_CP (6)
SATAICOMPO — AB10 (67 PCH_SATAICOMP)
SATAICOMPI — AB12
=PP1V05_S0_PCH_VCCIO_SATA (7 22)
PLACE_NEAR=U1800.AB10:2.54mm
R1830 37.4 1% 1/20W MF 201
=PP1V05_S0_PCH (7 22)
R1831 49.9 1% 1/20W MF 201
SATA3RCOMPO — AF10
SATA3COMPI — AF12 — PCH_SATA3COMP
SATA3RBIAS — AH4 — PCH_SATA3RBIAS
PLACE_NEAR=U1800.AF12:2.54mm
PLACE_NEAR=U1800.AH4:2.54mm
R1832 750 1% 1/20W MF 201
SATALED* — W10 — PCH_SATALED_L (16)
SATA0GP/GPIO21 — M2 — XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (OUT 23)
(IPU) SATA1GP/GPIO19 — R1 — XDP_DC3_PCH_GPIO19_SATARDRVR_EN (OUT 8 23)

=PPVRTC_G3_PCH (20 17 7)
R1800 330K 5% 1/20W MF 201
R1801 1M 5% 1/20W MF 201
R1802 20K 5% 1/20W MF 201
R1803 20K 5% 1/20W MF 201
RTC_RESET_L (16)
PCH_SRTCRST_L (16)
PCH_INTRUDER_L (16)
PCH_INTVRMEN_L (16)
C1802 1.0UF 20% 6.3V X5R 0201-MUR
C1803 1.0UF 20% 6.3V X5R 0201-MUR

LPC_AD_R<0> — R1860 33 — LPC_AD<0> (6 40 42 68)
LPC_AD_R<1> — R1861 33 — LPC_AD<1> (6 40 42 68)
LPC_AD_R<2> — R1862 33 — LPC_AD<2> (6 40 42 68)
LPC_AD_R<3> — R1863 33 — LPC_AD<3> (6 40 42 68)
LPC_FRAME_R_L — R1864 33 — LPC_FRAME_L (6 40 42 68)
HDA_BIT_CLK_R — R1810 33 — HDA_BIT_CLK (6 39 68)
PLACE_NEAR=U1800.H35:1.27mm
HDA_SYNC_R — R1811 33 — HDA_SYNC (6 39 68)
PLACE_NEAR=U1800.R37:1.27mm
HDA_RST_R_L — R1812 33 — HDA_RST_L (6 39 68)
PLACE_NEAR=U1800.F35:1.27mm
HDA_SDOUT_R — R1813 33 — HDA_SDOUT (6 39 68)
PLACE_NEAR=U1800.K37:1.27mm
(all 5% 1/20W MF 201)

=PP3V3_SUS_PCH_GPIO (7 17 18 19)
=PP3V3_S0_PCH_GPIO (7 17 18 19 25 35)

R1877 4.7K — PCH_SPKR (16)
R1878 10K — PCH_SATALED_L (16)
R1834 10K — DP_AUXCH_ISOL (23 25)
R1833 10K — SATARDRVR_EN (8)
R1842 10K — FW_CLKREQ_L (16)
R1869 10K — AP_CLKREQ_L (16 36)
R1844 10K — EXCARD_CLKREQ_L (16)
R1845 10K — JTAG_DPMUXUC_TRST_L (16)
R1847 10K — ENET_CLKREQ_L (16)
R1814 10K — PEG_CLKREQ_L (16)
R1815 10K — TBT_CLKREQ_L (16 35)
R1843 10K — SSD_CLKREQ_L (6 16 37)
R1846 10K — PEGCLKRQA_L_GPIO47 (16)
R1848 10K — PEGCLKRQB_L_GPIO56 (16)
R1853 10K — SMBUS_PCH_ALERT_L (16)
R1854 10K — USB_EXTB_SEL_XHCI (16 24)
R1855 10K — USB_EXTD_SEL_XHCI (16)
R1879 10K — ENET_MEDIA_SENSE_RDIV (16)
(all 5% 1/20W MF 201)

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

ITPCPU_CLK100M_N (65 10)
ITPCPU_CLK100M_P (65 10)
NO STUFF R1840 0 5% 1/20W MF 201
NO STUFF R1841 0 5% 1/20W MF 201

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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PCI-E*
PCIE_ENET_D2R_N — BJ33 PERN1
PCIE_ENET_D2R_P — BL33 PERP1
PCIE_ENET_R2D_C_N — BB30 PETN1
PCIE_ENET_R2D_C_P — AY30 PETP1
PCIE_AP_D2R_N — BJ35 PERN2
PCIE_AP_D2R_P — BL35 PERP2
PCIE_AP_R2D_C_N — BB33 PETN2
PCIE_AP_R2D_C_P — AY33 PETP2
PCIE_FW_D2R_N — BH36 PERN3
PCIE_FW_D2R_P — BK36 PERP3
PCIE_FW_R2D_C_N — BF33 PETN3
PCIE_FW_R2D_C_P — BD33 PETP3
PCIE_EXCARD_D2R_N — BJ37 PERN4
PCIE_EXCARD_D2R_P — BL37 PERP4
PCIE_EXCARD_R2D_C_N — BD35 PETN4
PCIE_EXCARD_R2D_C_P — BF35 PETP4
NC_PCIE_5_D2RN — BJ39 PERN5
NC_PCIE_5_D2RP — BL39 PERP5
NC_PCIE_5_R2D_CN — AY35 PETN5
NC_PCIE_5_R2D_CP — BB35 PETP5
NC_PCIE_6_D2RN — BH40 PERN6
NC_PCIE_6_D2RP — BK40 PERP6
NC_PCIE_6_R2D_CN — BD37 PETN6
NC_PCIE_6_R2D_CP — BF37 PETP6
NC_PCIE_7_D2RN — BJ41 PERN7
NC_PCIE_7_D2RP — BL41 PERP7
NC_PCIE_7_R2D_CN — AY37 PETN7
NC_PCIE_7_R2D_CP — BB37 PETP7
NC_PCIE_8_D2RN — BJ43 PERN8
NC_PCIE_8_D2RP — BL43 PERP8
NC_PCIE_8_R2D_CN — AY40 PETN8
NC_PCIE_8_R2D_CP — BB40 PETP8

CLOCKS
PCIE_CLK100M_ENET_N — AD48 CLKOUT_PCIE0N
PCIE_CLK100M_ENET_P — AD50 CLKOUT_PCIE0P
SSD_CLKREQ_L — M4 PCIECLKRQ0*/GPIO73
(controlled by PCIECLKRQ5#)
PCIE_CLK100M_FW_N — AE49 CLKOUT_PCIE1N
PCIE_CLK100M_FW_P — AE51 CLKOUT_PCIE1P
FW_CLKREQ_L — U8 PCIECLKRQ1*/GPIO18
PCIE_CLK100M_AP_N — AD40 CLKOUT_PCIE2N
PCIE_CLK100M_AP_P — AD42 CLKOUT_PCIE2P
AP_CLKREQ_L — T4 PCIECLKRQ2*/GPIO20
PCIE_CLK100M_EXCARD_N — AA49 CLKOUT_PCIE3N
PCIE_CLK100M_EXCARD_P — AA51 CLKOUT_PCIE3P
EXCARD_CLKREQ_L — B8 PCIECLKRQ3*/GPIO25
TP_PCIE_CLK100M_PE4N — Y48 CLKOUT_PCIE4N
TP_PCIE_CLK100M_PE4P — Y50 CLKOUT_PCIE4P
JTAG_DPMUXUC_TRST_L — M19 PCIECLKRQ4*/GPIO26
PCIE_CLK100M_SSD_N — AB40 CLKOUT_PCIE5N
PCIE_CLK100M_SSD_P — AB42 CLKOUT_PCIE5P
ENET_CLKREQ_L — K8 PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
TP_PCIE_CLK100M_PEBN — AF40 CLKOUT_PEG_B_N
TP_PCIE_CLK100M_PEBP — AF42 CLKOUT_PEG_B_P
PEGCLKRQB_L_GPIO56 — C4 PEG_B_CLKRQ*/GPIO56
PEG_CLK100M_N — AB44 CLKOUT_PCIE6N
PEG_CLK100M_P — AB46 CLKOUT_PCIE6P
PEG_CLKREQ_L — J3 PCIECLKRQ6*/GPIO45
PCIE_CLK100M_TBT_N — W44 CLKOUT_PCIE7N
PCIE_CLK100M_TBT_P — W46 CLKOUT_PCIE7P
TBT_CLKREQ_L — H4 PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
ITPXDP_CLK100M_N — AR12 CLKOUT_ITPXDP_N
ITPXDP_CLK100M_P — AR10 CLKOUT_ITPXDP_P

SMBUS
SMBALERT*/GPIO11 — H12 — SMBUS_PCH_ALERT_L (16)
SMBCLK — F17 — SMBUS_PCH_CLK (OUT 43 68)
SMBDATA — F10 — SMBUS_PCH_DATA (BI 43 68)
SML0ALERT*/GPIO60 — H22 — USB_EXTB_SEL_XHCI (OUT 16 24)
SML0CLK — K12 — SML_PCH_0_CLK (OUT 43 68)
SML0DATA — A9 — SML_PCH_0_DATA (BI 43 68)
SML1ALERT*/PCHHOT*/GPIO74 — C9 — USB_EXTD_SEL_XHCI (OUT 16)
SML1CLK/GPIO58 — D12 — SML_PCH_1_CLK (OUT 43 68)
SML1DATA/GPIO75 — C11 — SML_PCH_1_DATA (BI 43 68)

C-LINK
(IPU/IPD) CL_CLK1 — L3 — TP_CLINK_CLK (6)
(IPU/IPD) CL_DATA1 — J1 — TP_CLINK_DATA (6)
CL_RST1* — M8 — TP_CLINK_RESET_L (6)

CLOCKS
PEG_A_CLKRQ*/GPIO47 — R8 — PEGCLKRQA_L_GPIO47 (16)
CLKOUT_PEG_A_N — AF44 — TP_PCIE_CLK100M_PEGAN
CLKOUT_PEG_A_P — AF46 — TP_PCIE_CLK100M_PEGAP
CLKOUT_DMI_N — BB24 — DMI_CLK100M_CPU_N (OUT 10 65)
CLKOUT_DMI_P — AY24 — DMI_CLK100M_CPU_P (OUT 10 65)
CLKOUT_DP_N — AN10 — TP_PCH_CLKOUT_DPN (OUT 8)
CLKOUT_DP_P — AN12 — TP_PCH_CLKOUT_DPP (OUT 8)
CLKIN_DMI_N — BD17 — PCIE_CLK100M_PCH_N (IN 16 67)
CLKIN_DMI_P — BF17 — PCIE_CLK100M_PCH_P (IN 16 67)
CLKIN_GND1_N — BB26 — PCH_CLKIN_GNDN1 (16)
CLKIN_GND1_P — AY26 — PCH_CLKIN_GNDP1 (16)
CLKIN_DOT_96N — M24 — PCH_CLK96M_DOT_N (IN 16 67)
CLKIN_DOT_96P — K24 — PCH_CLK96M_DOT_P (IN 16 67)
CLKIN_SATA_N — AK8 — PCH_CLK100M_SATA_N (IN 16 67)
CLKIN_SATA_P — AK6 — PCH_CLK100M_SATA_P (IN 16 67)
REFCLK14IN — J49 — PCH_CLK14P3M_REFCLK (IN 16 67)
CLKIN_PCILOOPBACK — E51 — PCH_CLK33M_PCIIN (IN 25 68)
DOES THIS NEED LENGTH MATCH???
XTAL25_IN — W49 — SYSCLK_CLK25M_SB_R (16 68)
XTAL25_OUT — W51 — NC
=PP1V05_S0_PCH_VCCDIFFCLK (22 20 7)
R1890 90.9 1% 1/20W MF 201
PLACE_NEAR=U1800.AC49:2.54mm
XCLK_RCOMP — AC49 — PCH_XCLK_RCOMP

FLEX CLOCKS
CLKOUTFLEX0/GPIO64 (IPD-PWROK) — H50 — TP_PCH_GPIO64_CLKOUTFLEX0 (6)
CLKOUTFLEX1/GPIO65 (IPD-PWROK) — D48 — TP_PCH_GPIO65_CLKOUTFLEX1 (6)
CLKOUTFLEX2/GPIO66 (IPD-PWROK) — G49 — TP_PCH_GPIO66_CLKOUTFLEX2 (6)
CLKOUTFLEX3/GPIO67 (IPD-PWROK) — J51 — TP_PCH_GPIO67_CLKOUTFLEX3 (6)

SYSCLK_CLK25M_SB (68 25 IN)
R1885 604 1% 1/20W MF 201 (PLACE_NEAR=U1800.W49:5.1mm)
SYSCLK_CLK25M_SB_R (16 68)
1.8V -> 1.1V
R1886 1K 1% 1/20W MF 201

Unused clock terminations for FCIM Mode
PCH_CLK96M_DOT_P (67 16) — R1891 10K
PCH_CLK96M_DOT_N (67 16) — R1892 10K
PCH_CLK100M_SATA_P (67 16) — R1893 10K
PCH_CLK100M_SATA_N (67 16) — R1894 10K
PCIE_CLK100M_PCH_P (67 16) — R1895 10K
PCIE_CLK100M_PCH_N (67 16) — R1896 10K
PCH_CLK14P3M_REFCLK (67 16) — R1897 10K
PCH_CLKIN_GNDP1 (16) — R1870 10K
PCH_CLKIN_GNDN1 (16) — R1871 10K
(all 5% 1/20W MF 201)

SYNC_MASTER=J13_MLB SYNC_DATE=02/20/2012
PAGE TITLE: PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
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=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP1V05_S0_PCH_VCCIO_PCIE 7
PLACE_NEAR=U1800.BF19:12.7mm

R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201

OMIT_TABLE

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DMI / FDI

DMI_N2S_N<0>	BL21	DMI0RXN	
DMI_N2S_N<1>	BL23	DMI1RXN	
DMI_N2S_N<2>	BJ19	DMI2RXN	
DMI_N2S_N<3>	BL17	DMI3RXN	
DMI_N2S_P<0>	BJ21	DMI0RXP	
DMI_N2S_P<1>	BJ23	DMI1RXP	
DMI_N2S_P<2>	BL19	DMI2RXP	
DMI_N2S_P<3>	BJ17	DMI3RXP	
DMI_S2N_N<0>	BD22	DMI0TXN	
DMI_S2N_N<1>	BB22	DMI1TXN	
DMI_S2N_N<2>	BB19	DMI2TXN	
DMI_S2N_N<3>	BB17	DMI3TXN	
DMI_S2N_P<0>	BF22	DMI0TXP	
DMI_S2N_P<1>	AY22	DMI1TXP	
DMI_S2N_P<2>	AY19	DMI2TXP	
DMI_S2N_P<3>	AY17	DMI3TXP	
PCH_DMI_COMP	BF19	DMI_ZCOMP	
	BD19	DMI_IRCOMP	
PCH_DMI2RBIAS	BK20	DMI2RBIAS	

FDI_RXN0	BL13	FDI_DATA_N<0>	
FDI_RXN1	BJ15	FDI_DATA_N<1>	
FDI_RXN2	BD12	FDI_DATA_N<2>	
FDI_RXN3	BJ11	FDI_DATA_N<3>	
FDI_RXN4	AY15	FDI_DATA_N<4>	
FDI_RXN5	AY12	FDI_DATA_N<5>	
FDI_RXN6	BJ9	FDI_DATA_N<6>	
FDI_RXN7	BF10	FDI_DATA_N<7>	
FDI_RXP0	BJ13	FDI_DATA_P<0>	
FDI_RXP1	BL15	FDI_DATA_P<1>	
FDI_RXP2	BF12	FDI_DATA_P<2>	
FDI_RXP3	BL11	FDI_DATA_P<3>	
FDI_RXP4	BB15	FDI_DATA_P<4>	
FDI_RXP5	BB12	FDI_DATA_P<5>	
FDI_RXP6	BL9	FDI_DATA_P<6>	
FDI_RXP7	BD10	FDI_DATA_P<7>	
FDI_INT	BB10	FDI_INT	
FDI_FSYNC0	BH12	FDI_FSYNC<0>	
FDI_FSYNC1	BK8	FDI_FSYNC<1>	
FDI_LSYNC0	BK12	FDI_LSYNC<0>	
FDI_LSYNC1	BH8	FDI_LSYNC<1>	

SYSTEM POWER MANAGEMENT

PCH_SUSACK_L	F15	SUSACK*(IPU)	
PM_SYSRST_L	L1	SYS_RESET*	
PM_PCH_SYS_PWROK	M10	SYS_PWROK	
PM_PCH_PWROK	M22	PWROK	
PM_PCH_APWROK	G3	APWROK	
PM_MEM_PWRGD	B12	DRAMPWROK	
PM_RSMRST_L	B20	RSMRST*	
PCH_SUSWARN_L	C13	SUSWARN*/SUSPWRDNACK/GPIO30	
PM_PWRBTN_L	K19	PWRBTN*(IPU)	
SMC_ADAPTER_EN	H19	ACPRESENT/GPIO31 (IPD-DeepS4/S5)	
PM_BATLOW_L	H10	BATLOW*/GPIO72 (IPU)	
PCH_RI_L	F12	RI*	
DSWVRMEN	F22	PCH_DSWVRMEN	
DPWROK	A21	PM_DSW_PWRGD	IN 40
WAKE*	D8	PCIE_WAKE_L	IN 6 17 36
CLKRUN*/GPIO32	T2	PM_CLKRUN_L	B/I 6 17 40 42
SUS_STAT*/GPIO61	G6	LPC_PWRDWN_L	OUT 6 25 40 42
SUSCLK/GPIO62	D3	PM_CLK32K_SUSCLK_R	OUT 41 68
SLP_S5*/GPIO63	F6	PM_SLP_S5_L	OUT 17 40 61
SLP_S4*	K10	PM_SLP_S4_L	OUT 17 26 36 40 48 61
SLP_S3*	D4	PM_SLP_S3_L	OUT 17 26 40 61
SLP_A*	C7	TP_PM_SLP_A_L	
SLP_SUS*	A15	PM_SLP_SUS_L	OUT 17 61
PMSYNCH	BB8	PM_SYNC	OUT 10 65
SLP_LAN*/GPIO29	A7	MEM_VDD_SEL_1V5_L	OUT 17 55

=PPVRTC_G3_PCH 7 16 20

R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201

R1920 750 1% 1/20W MF 201

PLACE_NEAR=U1800.BK20:2.54mm

R1955 100K 5% 1/20W MF 201

LVDS_IG_BKL_ON	M44	L_BKLTEN	
LVDS_IG_PANEL_PWR	M42	L_VDD_EN	
LVDS_IG_BKL_PWM	L49	L_BKLTCTL	
	L51	L_DDC_CLK	
	K46	L_DDC_DATA (IPD-PLTRST#)	
	R42	L_CTRL_CLK	
	M40	L_CTRL_DATA	
	AH42	LVD_IBG	
	AH40	LVD_VBG	
	AG51	LVD_VREFH	
	AG49	LVD_VREFL	
	AK44	LVDSA_CLK*	
	AK46	LVDSA_CLK	
	AR46	LVDSA_DATA0*	
	AN49	LVDSA_DATA1*	
	AN44	LVDSA_DATA2*	
	AK40	LVDSA_DATA3*	
	AR44	LVDSA_DATA0	
	AN51	LVDSA_DATA1	
	AN46	LVDSA_DATA2	
	AK42	LVDSA_DATA3	
	AH46	LVDSB_CLK*	
	AH44	LVDSB_CLK	
	AM50	LVDSB_DATA0*	
	AL49	LVDSB_DATA1*	
	AJ51	LVDSB_DATA2*	
	AH50	LVDSB_DATA3*	
	AM48	LVDSB_DATA0	
	AL51	LVDSB_DATA1	
	AJ49	LVDSB_DATA2	
	AH48	LVDSB_DATA3	

LVDS DIGITAL DISPLAY INTERFACE

OMIT_TABLE

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SDVO_TVCLKINN (IPD)	AU40	TP_SDVO_TVCLKINN	
SDVO_TVCLKINP (IPD)	AU42	TP_SDVO_TVCLKINP	
SDVO_STALLN (IPD)	AR51	TP_SDVO_STALLN	
SDVO_STALLP (IPD)	AR49	TP_SDVO_STALLP	
SDVO_INTN (IPD)	AT50	TP_SDVO_INTN	
SDVO_INTP (IPD)	AT48	TP_SDVO_INTP	
SDVO_CTRLCLK	W42	DPA_IG_DDC_CLK	
SDVO_CTRLDATA (IPD-PLTRST#)	R44	DPA_IG_DDC_DATA	
DDPB_AUXN	AW51	DPA_IG_AUX_CH_N	
DDPB_AUXP	AW49	DPA_IG_AUX_CH_P	
DDPB_HPD	AY42	DPA_IG_HPD	
DDPB_0N	AY48	TP_DP_IG_B_MLN<0>	
DDPB_0P	AY50	TP_DP_IG_B_MLP<0>	
DDPB_1N	AY44	TP_DP_IG_B_MLN<1>	
DDPB_1P	AY46	TP_DP_IG_B_MLP<1>	
DDPB_2N	BB44	TP_DP_IG_B_MLN<2>	
DDPB_2P	BB46	TP_DP_IG_B_MLP<2>	
DDPB_3N	BA49	TP_DP_IG_B_MLN<3>	
DDPB_3P	BA51	TP_DP_IG_B_MLP<3>	
DDPC_CTRLCLK	T50	DPB_IG_DDC_CLK	
DDPC_CTRLDATA (IPD-PLTRST#)	U44	DPB_IG_DDC_DATA	
DDPC_AUXN	AU51	DPB_IG_AUX_CH_N	
DDPC_AUXP	AU49	DPB_IG_AUX_CH_P	
DDPC_HPD	BE46	DPB_IG_HPD	
DDPC_0N	BC49	TP_DP_IG_C_MLN<0>	
DDPC_0P	BC51	TP_DP_IG_C_MLP<0>	
DDPC_1N	BD48	TP_DP_IG_C_MLN<1>	
DDPC_1P	BD50	TP_DP_IG_C_MLP<1>	
DDPC_2N	BF46	TP_DP_IG_C_MLN<2>	
DDPC_2P	BF45	TP_DP_IG_C_MLP<2>	
DDPC_3N	BE49	TP_DP_IG_C_MLN<3>	
DDPC_3P	BE51	TP_DP_IG_C_MLP<3>	
DDPD_CTRLCLK	M48	TP_DP_IG_D_CTRL_CLK	
DDPD_CTRLDATA (IPD-PLTRST#)	U42	TP_DP_IG_D_CTRL_DATA	
DDPD_AUXN	AU46	TP_DP_IG_D_AUXN	
DDPD_AUXP	AU44	TP_DP_IG_D_AUXP	
DDPD_HPD	BK44	TP_DP_IG_D_HPD	
DDPD_0N	BG51	TP_DP_IG_D_MLN<0>	
DDPD_0P	BG49	TP_DP_IG_D_MLP<0>	
DDPD_1N	BF42	TP_DP_IG_D_MLN<1>	
DDPD_1P	BD42	TP_DP_IG_D_MLP<1>	
DDPD_2N	BJ47	TP_DP_IG_D_MLN<2>	
DDPD_2P	BL47	TP_DP_IG_D_MLP<2>	
DDPD_3N	BL45	TP_DP_IG_D_MLN<3>	
DDPD_3P	BJ45	TP_DP_IG_D_MLP<3>	

CRT

TP_CRT_IG_BLUE	M46	CRT_BLUE	
TP_CRT_IG_GREEN	R46	CRT_GREEN	
TP_CRT_IG_RED	U46	CRT_RED	
TP_CRT_IG_DDC_CLK	R49	CRT_DDC_CLK	
TP_CRT_IG_DDC_DATA	N49	CRT_DDC_DATA	
TP_CRT_IG_HSYNC	M50	CRT_HSYNC	
TP_CRT_IG_VSYNC	N51	CRT_VSYNC	
PCH_DAC_IREF	R51	DAC_IREF	
	T48	CRT_IRTN	

PLACE_NEAR=U1800.R51:2.54mm

R1951 1K 5% 1/20W MF 201

19 18 17 16 7 =PP3V3_SUS_PCH_GPIO

R1983 10K 5% 1/20W MF 201

R1986 0 5% 1/20W MF 201

17 PCH_SUSWARN_L — PCH_SUSACK_L 17

=PP3V3_SUS_PCH_GPIO 7 16 17 18 19
=PP3V3_S0_PCH_GPIO 7 16 18 19 25 35
=PP3V3_S5_PCH 7

R1985	1K	PM_PWRBTN_L	17 23 40
R1991	8.2K	PM_CLKRUN_L	6 17 40 42
R1982	10K	MEM_VDD_SEL_1V5_L	17 55
R1925	1K	PCIE_WAKE_L	6 17 36
R1924	100K	PM_SLP_S3_L	17 26 40 61
R1921	100K	PM_SLP_S4_L	17 26 36 40 48 61
R1922	100K	PM_SLP_S5_L	17 40 61
R1923	100K	PM_SLP_SUS_L	17 61

All: 5% 1/20W MF 201

SYNC_MASTER=J13_MLB SYNC_DATE=10/06/2011

PAGE TITLE
PCH DMI/FDI/PM/Graphics

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
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NC	BH24	TP1	
NC	BK24	TP2	
NC	BH20	TP3	
NC	BK16	TP4	
NC	BH16	TP5	
NC	AN42	TP6	
NC	AN40	TP7	
NC	AR40	TP8	
NC	AR42	TP9	
NC	D20	TP10	
NC	M30	TP11	
NC	E3	TP12	
NC	AM4	TP13	
NC	AT4	TP14	
NC	AT2	TP15	
NC	AD10	TP16	
NC	B24	TP17	
NC	D24	TP18	
NC	AD44	TP19	
NC	AD46	TP20	
NC	BJ48	TP21	
NC	BL7	TP22	
TP_PCH_TP23	W40	TP23	
NC	K30	TP24	
	BH49	TP41	
	BB42	TP42	

	AU6		NC
	AU8		NC
	AW1		NC
	AW3		NC
	AY2		NC
	AY4		NC
	AY6		NC
	AY8		NC
	BA1		NC
	BA3		NC
	BB6		NC
	BC1		NC
RSVD	BC3		NC
	BD2		NC
	BD4		NC
	BE1		NC
	BE3		NC
	BE6		NC
	BF6		NC
	BF7		NC
	BG1		NC
	BG3		NC
	BH3		NC
	BH4		NC
	BJ4		NC
	BJ5		NC
	BJ7		NC
	BK6		NC
	BL5		NC

USB

67 38 IN	USB3_EXTA_RX_N	BJ25	USB3RN1
67 39 IN	USB3_EXTB_RX_N	BJ27	USB3RN2
8 IN	USB3_EXTC_RX_N	BJ31	USB3RN3
8 IN	USB3_EXTD_RX_N	BJ29	USB3RN4
67 38 IN	USB3_EXTA_RX_P	BL25	USB3RP1
67 39 IN	USB3_EXTB_RX_P	BL27	USB3RP2
8 IN	USB3_EXTC_RX_P	BL31	USB3RP3
8 IN	USB3_EXTD_RX_P	BL29	USB3RP4
67 38 OUT1	USB3_EXTA_TX_N	BF26	USB3TN1
67 39 OUT1	USB3_EXTB_TX_N	BB28	USB3TN2
8 OUT1	USB3_EXTC_TX_N	BF28	USB3TN3
8 OUT1	USB3_EXTD_TX_N	BF30	USB3TN4
67 38 OUT1	USB3_EXTA_TX_P	BD26	USB3TP1
67 39 OUT1	USB3_EXTB_TX_P	AY28	USB3TP2
8 OUT1	USB3_EXTC_TX_P	BD28	USB3TP3
8 OUT1	USB3_EXTD_TX_P	BD30	USB3TP4

USBP0N	F24	USB_EXTA_N	B1 38 67
USBP0P	H24	USB_EXTA_P	B1 38 67
USBP1N	C25	USB_EXTB_XHCI_N	B1 24 67
USBP1P	A25	USB_EXTB_XHCI_P	B1 24 67
USBP2N	C27	USB_EXTC_N	B1 8
USBP2P	A27	USB_EXTC_P	B1 8
USBP3N	H28	USB_EXTD_XHCI_N	B1 24 67
USBP3P	F28	USB_EXTD_XHCI_P	B1 24 67
USBP4N	M26	TP_USB_4N	
USBP4P	K26	TP_USB_4P	
USBP5N	D28	TP_USB_SDN	
USBP5P	B28	TP_USB_SDP	
USBP6N	H26	TP_USB_WLANN	
USBP6P	F26	TP_USB_WLANP	
USBP7N	D32	USB_HUB_UP_N	B1 24 67
USBP7P	B32	USB_HUB_UP_P	B1 24 67
USBP8N	M28	USB_CAMERA_N	B1 6 39 67
USBP8P	K28	USB_CAMERA_P	B1 6 39 67
USBP9N	C29	USB_EXTB_EHCI_N	B1 24 67
USBP9P	A29	USB_EXTB_EHCI_P	B1 24 67
USBP10N	C31	USB_EXTD_EHCI_N	B1 8
USBP10P	A31	USB_EXTD_EHCI_P	B1 8
USBP11N	H33	TP_USB_BT_HSN	
USBP11P	F33	TP_USB_BT_HSP	
USBP12N	H30	TP_USB_12N	
USBP12P	F30	TP_USB_12P	
USBP13N	M33	TP_USB_13N	
USBP13P	K33	TP_USB_13P	
(IPD)			

Ext A (XHCI/EHCI)

Ext B (XHCI)

Ext C (XHCI/EHCI)

Ext D (XHCI) (Mobiles: Trackpad?)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

Ext B (EHCI)

Ext D (EHCI)

RSVD: BT (HS)

Unused

Unused

USBRBIAS*	C33	67 PCH_USB_RBIAS	
USBRBIAS	A33		

PLACE_NEAR=U1800.A33:2.54mm
R2070 22.6 1% 1/20W MF 201

PCI

18 OUT1	JTAG_GMUX_TMS	G46	REQ1*/GPIO50
18 OUT1	BLC_I2C_MUX_SEL	K44	REQ2*/GPIO52
18 OUT1	PCH_GPIO54	F46	REQ3*/GPIO54
	TP_PCH_STRP_BBS1	F42	GNT1*/GPIO51
	TP_PCH_STRP_ESI_L	H42	GNT2*/GPIO53
	PCH_STRP_TOPBLK_SWP_L	D44	GNT3*/GPIO55
			(IPU-PCIERST#)
18 IN	BLC_GPIO	A47	PIRQE*/GPIO2
39 18 6 IN	AUD_IP_PERIPHERAL_DET	C41	PIRQF*/GPIO3
33 18 IN	TBT_PWR_REQ_L	F45	PIRQG*/GPIO4
39 18 6 IN	AUD_I2C_INT_L	F40	PIRQH*/GPIO5
6	TP_PCI_PME_L	H2	PME* (IPU)
26 25 OUT1	PLT_RESET_L	F7	PLTRSTB*
68 25 OUT1	LPC_CLK33M_SMC_R	G51	CLKOUT_PCI0
68 25 OUT1	LPC_CLK33M_LPCPLUS_R	E49	CLKOUT_PCI1
	TP_PCI_CLK33M_OUT2	H48	CLKOUT_PCI2
6	TP_PCI_CLK33M_OUT3	J43	CLKOUT_PCI3
68 25 OUT1	PCH_CLK33M_PCIOUT	G45	CLKOUT_PCI4
			(IPD)

OC0*/GPIO59	C17	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	IN 18 23
OC1*/GPIO40	A17	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	IN 18 23
OC2*/GPIO41	A13	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	IN 18 23
OC3*/GPIO42	D16	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	IN 18 23
OC4*/GPIO43	A11	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L	IN 23
OC5*/GPIO9	B16	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	IN 23
OC6*/GPIO10	C23	XDP_DB2_PCH_GPIO10_AP_PWR_EN	OUT1 23
OC7*/GPIO14	H15	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	IN 18 23

35 25 19 18 17 16 7 =PP3V3_S0_PCH_GPIO

R2010	10K	5%	1/20W	MF	201	PCI_INTA_L	D49 PIRQA*
R2011	10K	5%	1/20W	MF	201	PCI_INTB_L	C48 PIRQB*
R2012	10K	5%	1/20W	MF	201	PCI_INTC_L	C47 PIRQC*
R2013	10K	5%	1/20W	MF	201	PCI_INTD_L	C45 PIRQD*

NO STUFF

R2054	10K	5%	1/20W	MF	201	PCH_STRP_TOPBLK_SWP_L	(IPU-PCIERST#)

=PP3V3_SUS_PCH_GPIO 7 16 17 19
=PP3V3_S3_PCH_GPIO 7 25
=PP3V3_S0_PCH_GPIO 7 16 17 18 19 25 35

R2016	10K	5%	1/20W	MF	201	JTAG_GMUX_TMS	18
R2017	10K	5%	1/20W	MF	201	BLC_I2C_MUX_SEL	18
R2018	10K	5%	1/20W	MF	201	PCH_GPIO54	18
R2030	10K	5%	1/20W	MF	201	BLC_GPIO	18

NO STUFF Redundant to pull-down on audio page

R2014	10K	5%	1/20W	MF	201	AUD_IP_PERIPHERAL_DET	6 18 39
R2031	10K	5%	1/20W	MF	201	TBT_PWR_REQ_L	18 33

NO STUFF Redundant to pull-up on audio page

R2033	10K	5%	1/20W	MF	201	AUD_I2C_INT_L	6 18 39
R2069	10K	5%	1/20W	MF	201	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	18 23
R2060	10K	5%	1/20W	MF	201	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	18 23
R2061	10K	5%	1/20W	MF	201	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	18 23
R2062	10K	5%	1/20W	MF	201	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	18 23
R2068	10K	5%	1/20W	MF	201	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	18 23
R2067	10K	5%	1/20W	MF	201	AP_PWR_EN	23 36 61

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PAGE TITLE
PCH PCI/USB/TP/RSVD

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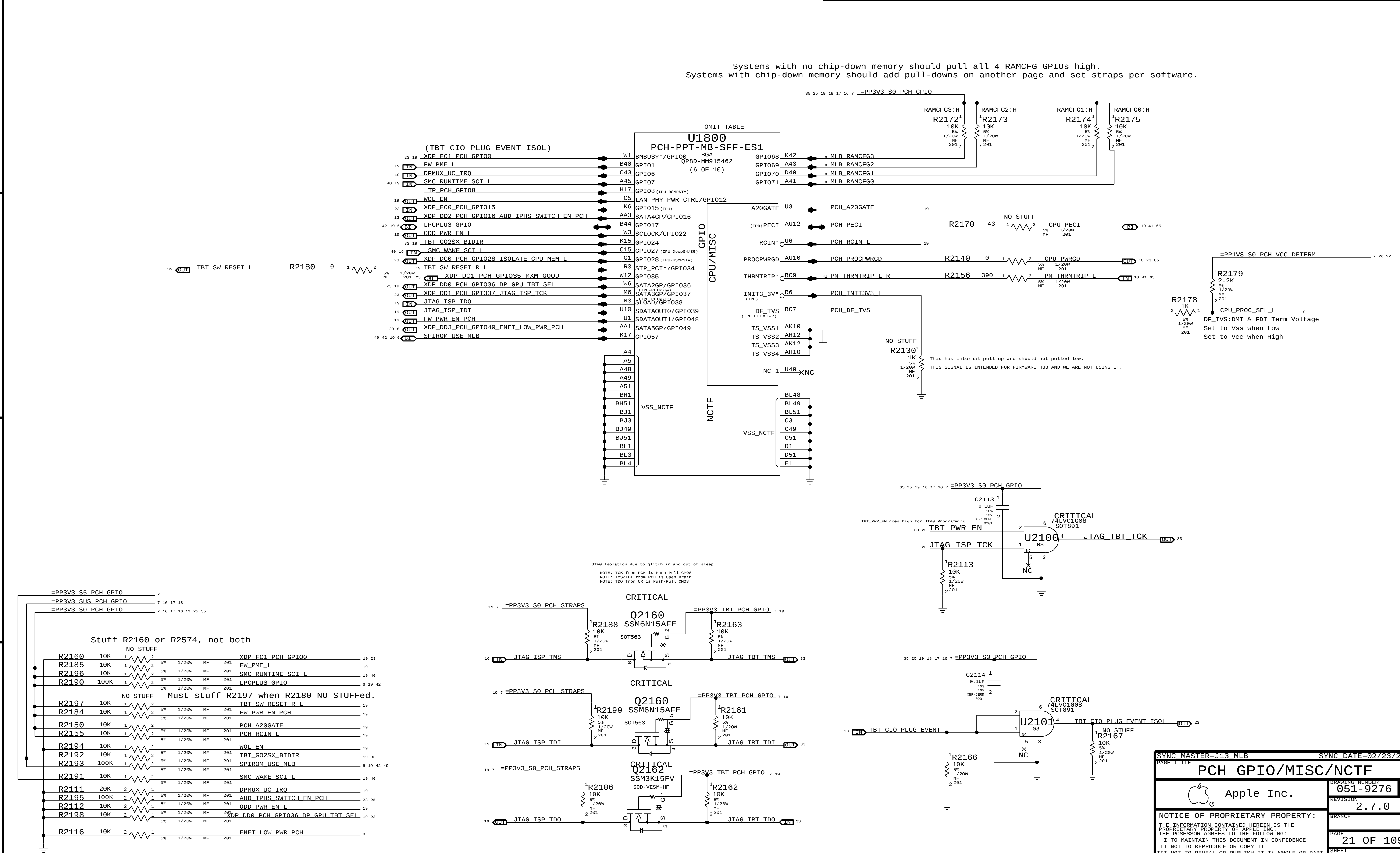
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.



OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(6 OF 10)
GPIO
CPU/MISC
NCTF
(TBT_CIO_PLUG_EVENT_ISOL)
XDP_FC1_PCH_GPIO0
FW_PME_L
DPMUX_UC_IRQ
SMC_RUNTIME_SCI_L
TP_PCH_GPIO8
WOL_EN
XDP_FC0_PCH_GPIO15
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
LPCPLUS_GPIO
ODD_PWR_EN_L
TBT_GO2SX_BIDIR
SMC_WAKE_SCI_L
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
TBT_SW_RESET_R_L
XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
JTAG_ISP_TDO
JTAG_ISP_TDI
FW_PWR_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH
SPIROM_USE_MLB
TBT_SW_RESET_L
R2180
=PP3V3_S0_PCH_GPIO
RAMCFG3:H RAMCFG2:H RAMCFG1:H RAMCFG0:H
R2172 R2173 R2174 R2175
MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
PCH_A20GATE
PCH_PECI
R2170
NO STUFF
CPU_PECI
PCH_RCIN_L
PCH_PROCPWRGD
R2140
CPU_PWRGD
PM_THRMTRIP_L_R
R2156
PM_THRMTRIP_L
PCH_INIT3V3_L
PCH_DF_TVS
=PP1V8_S0_PCH_VCC_DFTERM
R2179
R2178
CPU_PROC_SEL_L
DF_TVS:DMI & FDI Term Voltage
Set to Vss when Low
Set to Vcc when High
NO STUFF
R2130
This has internal pull up and should not pulled low.
THIS SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.
VSS_NCTF
=PP3V3_S0_PCH_GPIO
C2113
CRITICAL
74LVC1G08
SOT891
U2100
TBT_PWR_EN goes high for JTAG Programming
TBT_PWR_EN
JTAG_ISP_TCK
JTAG_TBT_TCK
R2113
JTAG Isolation due to glitch in and out of sleep
NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS
=PP3V3_S5_PCH_GPIO
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
Stuff R2160 or R2574, not both
Must stuff R2197 when R2180 NO STUFFed.
R2160 R2185 R2196 R2190 R2197 R2184 R2150 R2155 R2194 R2192 R2193 R2191 R2111 R2195 R2112 R2198 R2116
XDP_FC1_PCH_GPIO0
FW_PME_L
SMC_RUNTIME_SCI_L
LPCPLUS_GPIO
TBT_SW_RESET_R_L
FW_PWR_EN_PCH
PCH_A20GATE
PCH_RCIN_L
WOL_EN
TBT_GO2SX_BIDIR
SPIROM_USE_MLB
SMC_WAKE_SCI_L
DPMUX_UC_IRQ
AUD_IPHS_SWITCH_EN_PCH
ODD_PWR_EN_L
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
ENET_LOW_PWR_PCH
CRITICAL
Q2160
SSM6N15AFE
=PP3V3_S0_PCH_STRAPS
=PP3V3_TBT_PCH_GPIO
R2188 R2163
JTAG_ISP_TMS
JTAG_TBT_TMS
R2199 R2161
JTAG_ISP_TDI
JTAG_TBT_TDI
Q2162
SSM3K15FV
SOD-VESM-HF
R2186 R2162
JTAG_ISP_TDO
JTAG_TBT_TDO
C2114
U2101
TBT_CIO_PLUG_EVENT
TBT_CIO_PLUG_EVENT_ISOL
R2166
R2167

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PCH GPIO/MISC/NCTF

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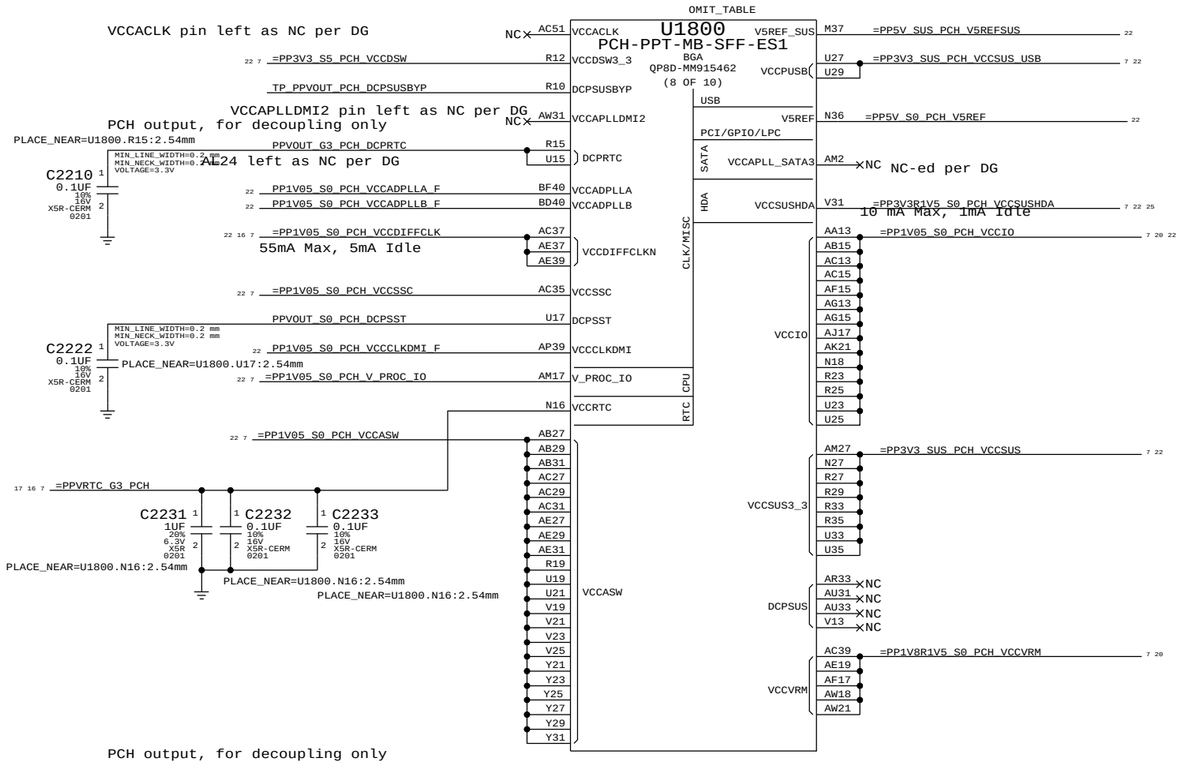

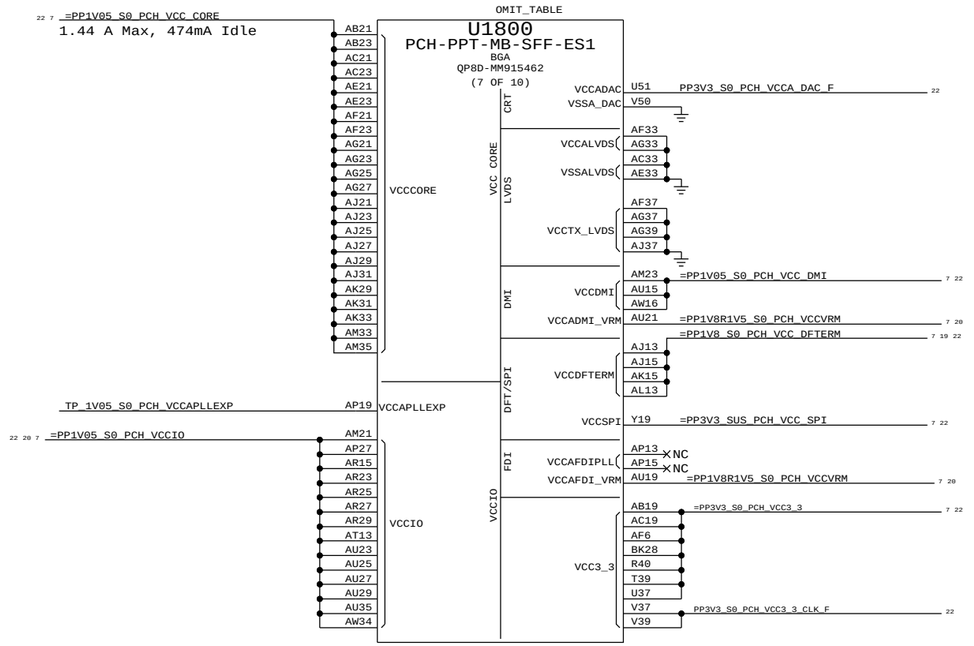

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PAGE TITLE	PCH POWER
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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(9 OF 10)

AA7			AP2
AA9			AP4
AA11			AP7
AA39			AP9
AA41			AP11
AA43			AP17
AA45			AP21
AB2			AP23
AB4			AP25
AB17			AP29
AB25			AP31
AB33			AP33
AB35			AP35
AB37			AP37
AB48			AP41
AB50			AP43
AC7			AP45
AC9			AP48
AC11			AP50
AC17			AR6
AC25			AR8
AC41			AR17
AC43			AR19
AC45			AR21
AE7			AR31
AE9			AR35
AE11			AR37
AE13			AT7
AE15			AT9
AE17			AT11
AE25			AT39
AE35			AT41
AE41			AT43
AE43			AT45
AE45			AU17
AF2			AU37
AF4			AV2
AF8			AV4
AF19			AV48
AF25			AV50
AF27			AW7
AF29	VSS	VSS	AW9
AF31			AW11
AF35			AW13
AF48			AW23
AF50			AW25
AG7			AW27
AG9			AW29
AG11			AW36
AG17			AW39
AG19			AW41
AG29			AW43
AG31			AW45
AG35			AY10
AG41			B6
AG43			B10
AG45			B14
AH2			B18
AJ7			B22
AJ9			B26
AJ11			B30
AJ19			B34
AJ33			B38
AJ35			B42
AJ39			B46
AJ41			BA7
AJ43			BA9
AJ45			BA11
AK2			BA13
AK4			BA16
AK17			BA18
AK19			BA21
AK23			BA23
AK25			BA25
AK27			BA27
AK35			BA29
AK37			BA31
AK48			BA34
AK50			BA36
AL7			BA39
AL9			BA41
AL11			BA43
AL39			BA45
AL41			BB2
AL43			BB4
AL45			BB48
AM15			BB50
AM19			BC11
AM25			BC13
AM29			BC16
AM31			BC18
AM37			BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
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BC23			G39
BC25			G41
BC27			G43
BC29			J7
BC31			J9
BC34			J11
BC36			J13
BC39			J16
BC41			J18
BC43			J21
BC45			J23
BD15			J25
BD24			J27
BE7			J29
BE9			J31
BE11			J34
BE13			J36
BE16			J39
BE18			J41
BE21			J45
BE23			K2
BE25			K4
BE27			K48
BE29			K50
BE31			L7
BE34			L9
BE36			L11
BE39			L13
BE41			L16
BE43			L18
BE45			L21
BF2			L23
BF4			L25
BF15			L27
BF24			L29
BF48			L31
BF50			L34
BH6			L36
BH10			L39
BH14	VSS	VSS	L41
BH18			L43
BH22			L45
BH26			N7
BH28			N9
BH30			N11
BH32			N13
BH34			N21
BH38			N23
BH42			N25
BH44			N29
BH46			N31
BH48			N34
BK10			N39
BK14			N41
BK18			N43
BK22			N45
BK26			P2
BK30			P4
BK32			P48
BK34			P50
BK38			R17
BK42			R21
BK46			R31
D6			R37
D10			T7
D14			T9
D18			T11
D22			T13
D26			T41
D30			T43
D34			T45
D38			U31
D42			U49
D46			V2
F2			V4
F4			V7
F48			V9
F50			V11
G7			V15
G9			V17
G11			V27
G13			V29
G16			V33
G18			V35
G21			V41
G23			V43
G25			V45
G27			V48
G29			Y15
G31			Y17
G34			Y33
G36			Y35
			Y37

SYNC_MASTER=J13_MLB SYNC_DATE=08/12/2011

PAGE TITLE
PCH GROUNDS

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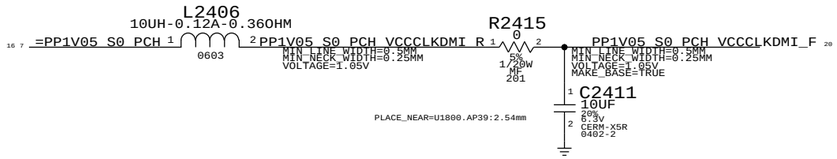

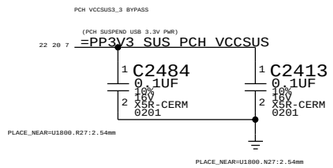

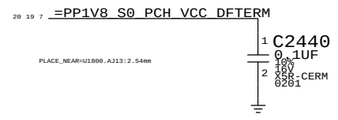

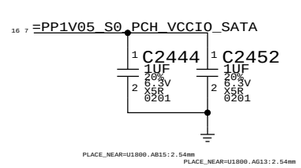

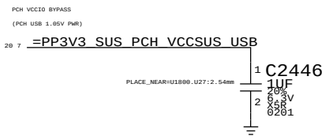

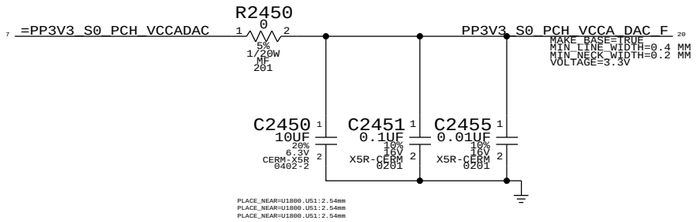

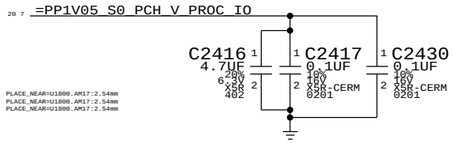

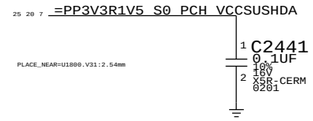

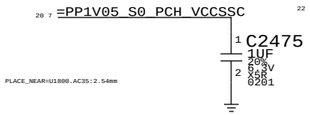

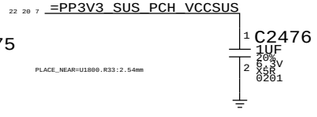

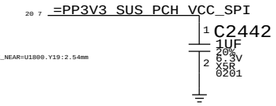

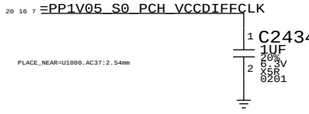

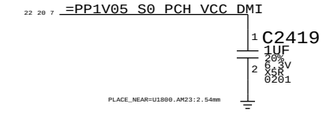

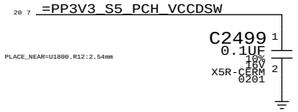

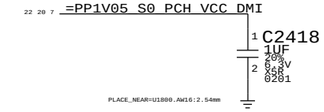

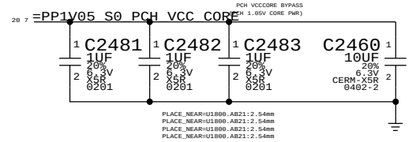

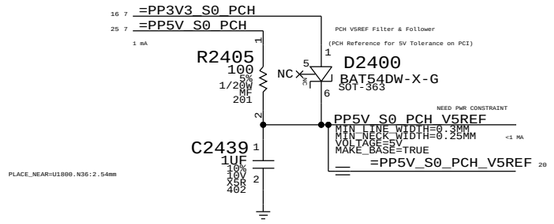

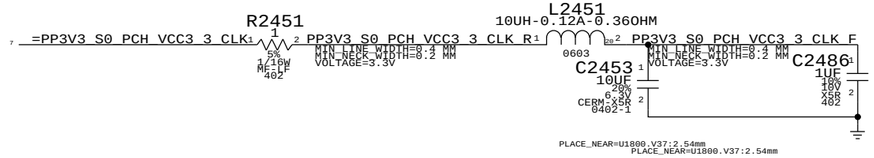

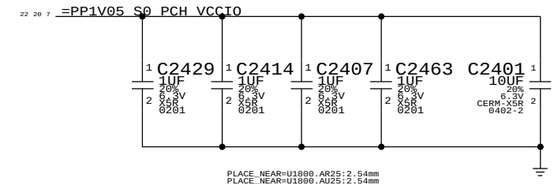

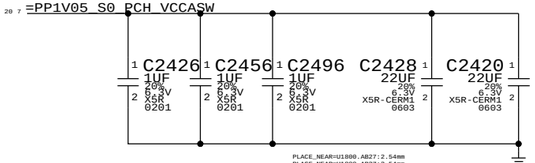

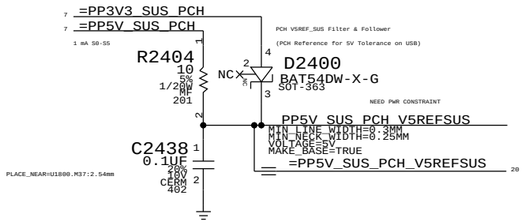

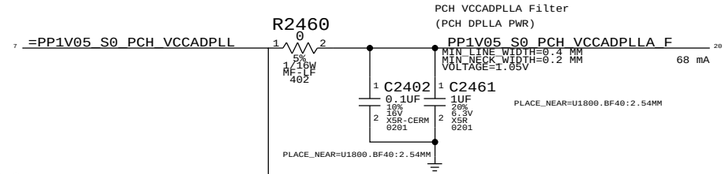

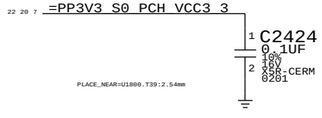

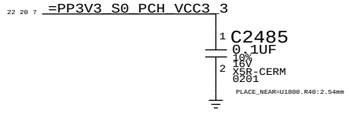

SYNC MASTER=J13_MLB SYNC_DATE=11/18/2013

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
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CPU Micro2-XDP

=PPVCCIO_S0_XDP (23,7)

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

=PP3V3_S0_XDP (7)
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0	PLACE_SIDE=BOTTOM
XDP_BPM_L<5>	R2561	0	PLACE_SIDE=BOTTOM
XDP_BPM_L<6>	R2562	0	
XDP_BPM_L<7>	R2563	0	

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0
CPU_CFG<13>	R2565	0
CPU_CFG<14>	R2566	0
CPU_CFG<15>	R2567	0

CPU_PWRGD	R2500	1K	PLACE_NEAR=U1000.B46:2.54mm
PM_PWRBTN_L	R2502	0	PLACE_NEAR=U4900.J3:2.54mm
CPU_CFG<0>	R2501	1K	PLACE_NEAR=U1000.B50:2.54mm
PM_PCH_SYS_PWROK	R2504	330	

XDP_CPU_PREQ_L	OBSEN_A0	CPU_CFG<16>
XDP_CPU_PRDY_L	OBSEN_A1	CPU_CFG<17>
XDP_BPM_L<0>	OBSDATA_A0	CPU_CFG<0>
XDP_BPM_L<1>	OBSDATA_A1	CPU_CFG<1>
XDP_BPM_L<2>	OBSDATA_A2	CPU_CFG<2>
XDP_BPM_L<3>	OBSDATA_A3	CPU_CFG<3>
CPU_CFG<10>	OBSEN_B0	CPU_CFG<8>
CPU_CFG<11>	OBSEN_B1	CPU_CFG<9>
XDP_OBSDATA_B<0>	OBSDATA_B0	CPU_CFG<4>
XDP_OBSDATA_B<1>	OBSDATA_B1	CPU_CFG<5>
XDP_OBSDATA_B<2>	OBSDATA_B2	CPU_CFG<6>
XDP_OBSDATA_B<3>	OBSDATA_B3	CPU_CFG<7>
XDP_CPU_PWRGD	PWRGD/HOOK0	XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	XDP_CPU_CLK100M_N
XDP_CPU_CFG<0>	VCC_OBS_AB	XDP_CPURST_L
XDP_VR_READY	HOOK2	XDP_DBRESET_L
=SMBUS_XDP_SDA	HOOK3	XDP_CPU_TDO
=SMBUS_XDP_SCL	SDA	XDP_CPU_TRST_L
XDP_CPU_TCK	SCL	XDP_CPU_TDI
	TCK1	XDP_CPU_TMS
	TCK0	XDP_PRESENT#

ITPCLK/HOOK4
ITPCLK#/HOOK5
VCC_OBS_CD
RESET#/HOOK6
DBR#/HOOK7
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
TDO
TRSTn
TDI
TMS
NC

R2581 1K 1/20W MF 201
R2580 1K 1/20W MF 201

XDP C2500 0.1uF 10% 10V X5R 402
XDP C2501 0.1uF 10% 10V X5R 402

518S0847

XDP_CPU_TDO	R2510	51
XDP_CPU_TDI	R2511	51
XDP_CPU_TMS	R2512	51
XDP_CPU_TCK	R2513	51
XDP_CPU_TRST_L	R2514	51

XDP PLACE_NEAR=J2500.52:2.54mm
XDP PLACE_NEAR=U1000.K61:2.54mm
XDP PLACE_NEAR=U1000.H59:2.54mm
XDP PLACE_NEAR=U1000.J58:2.54mm
XDP PLACE_NEAR=U1000.H63:2.54mm

R2515	0	XDP PLACE_NEAR=R1841.1:2.54mm ITPXDP_CLK100M_P
R2516	0	XDP PLACE_NEAR=R1840.1:2.54mm ITPXDP_CLK100M_N
R2505	1K	XDP PLACE_NEAR=U1000.D44:2.54mm CPU_RESET_L

XDP SIGNALS

(R2520-R2537)
XDP

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2592	0
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0
XDP_FC1_PCH_GPIO0	R2574	1K

Non-XDP Signals

USB_EXTA_OC_L	
AP_PWR_EN	
USB_EXTB_OC_L	
ISOLATE_CPU_MEM_L	
DP_AUXCH_ISOL	
JTAG_ISP_TCK	
AUD_IPHS_SWITCH_EN_PCH	
TBT_CIO_PLUG_EVENT_ISOL	

PCH Micro2-XDP

=PP3V3_S5_XDP (7)

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

TP_XDP_PCH_OBSFN_A<0>	OBSFN_A0	OBSFN_C0
TP_XDP_PCH_OBSFN_A<1>	OBSFN_A1	OBSFN_C1
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3
TP_XDP_PCH_OBSFN_B<0>	OBSFN_B0	OBSFN_D0
TP_XDP_PCH_OBSFN_B<1>	OBSFN_B1	OBSFN_D1
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	OBSDATA_D0
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	OBSDATA_D1
XDP_DB2_AP_PWR_EN	OBSDATA_B2	OBSDATA_D2
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	OBSDATA_D3
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5
	VCC_OBS_AB	VCC_OBS_CD
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7
=SMBUS_XDP_SDA	SDA	TDO
=SMBUS_XDP_SCL	SCL	TRSTn
	TCK1	TDI
XDP_PCH_TCK	TCK0	TMS
		XDP_PRESENT#

OBSFN_C0	XDP_FC0
OBSFN_C1	XDP_FC1
OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L
OBSDATA_C1	XDP_DC1_MXM_GOOD
OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL
OBSDATA_C3	XDP_DC3_SATARDRVR_EN
OBSFN_D0	TP_XDP_PCH_OBSFN_D<0>
OBSFN_D1	TP_XDP_PCH_OBSFN_D<1>
OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL
OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK
OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN
OBSDATA_D3	XDP_DD3_ENET_LOW_PWR
ITPCLK/HOOK4	TP_XDP_PCH_HOOK4
ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5
VCC_OBS_CD	
RESET#/HOOK6	XDPPCH_PLTRST_L
DBR#/HOOK7	XDP_DBRESET_L
TDO	XDP_PCH_TDO
TRSTn	TP_XDP_PCH_TRST_L
TDI	XDP_PCH_TDI
TMS	XDP_PCH_TMS
XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2580 0.1uF 10% 10V X5R 402
XDP C2581 0.1uF 10% 10V X5R 402

518S0847

=PP1V05_SUS_PCH_JTAG (7)

XDP_PCH_TDO	R2550	51
XDP_PCH_TDI	R2551	51
XDP_PCH_TMS	R2552	51
XDP_PCH_TCK	R2556	51

XDP PLACE_NEAR=J2550.51:2.54mm
XDP PLACE_NEAR=U1800.U12:2.54mm
XDP PLACE_NEAR=U1800.M15:2.54mm
XDP PLACE_NEAR=U1800.M17:2.54mm

ALL_SYS_PWRGD → XDP_PCH_S5_PWRGD — R2584 1K XDP PLACE_NEAR=J2550.40:2.54mm
PM_PWRBTN_L → XDP_PCH_PWRBTN_L — R2585 0 XDP PLACE_NEAR=U4900.J3:2.54mm

1K series R on PCH Support Page

SYNC_MASTER=J13_MLB	SYNC_DATE=08/04/2011
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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0903	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,36QFN	U2600	CRITICAL	USBHUB2513B

USB XHCI/EHCI2 PORT MUX FOR EXT B

PCH PORT 9 (EHCI2)

PCH PORT 1 (XHCI)

TO LIO CONNECTOR

LIO External D

PULL-UP TO 3.3V SUS ON PCH PAGE, SEL PIN IS LEAKAGE-SAFE

SEL=0 CHOOSE USB EHCI2 PORT

SEL=1 CHOOSE USB XHCI PORT

PCH GPIO60

TO USB HUB

TO TP/KB

TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R2611 & R2615, STUFF R2621,R2622,R2616 & R2617

TO PCH XHCI

SYNC_MASTER=J13_MLB	SYNC_DATE=08/12/2011
PAGE TITLE	USB HUB & MUX
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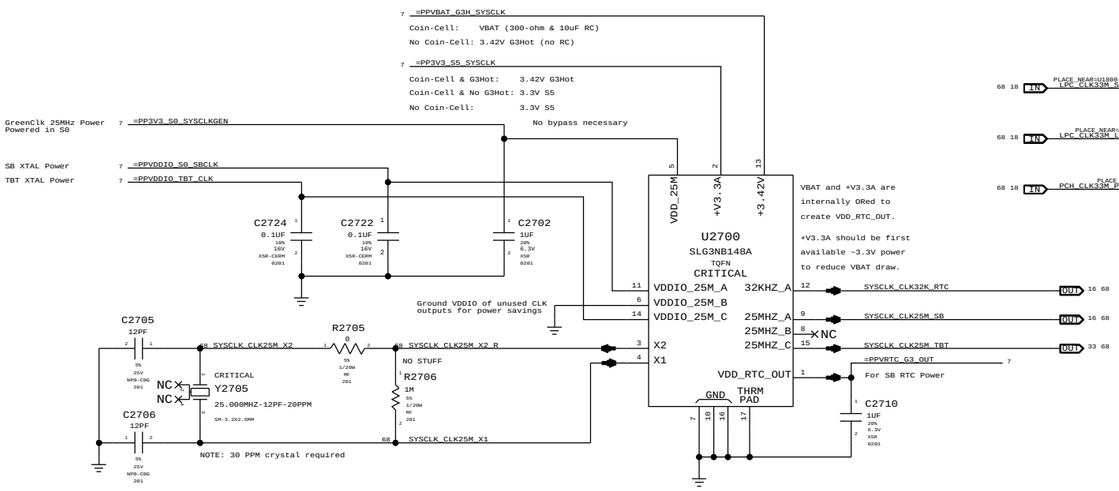
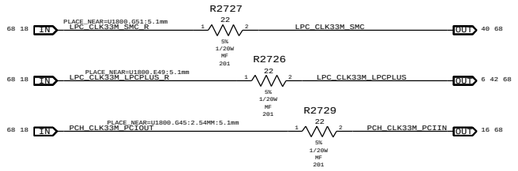
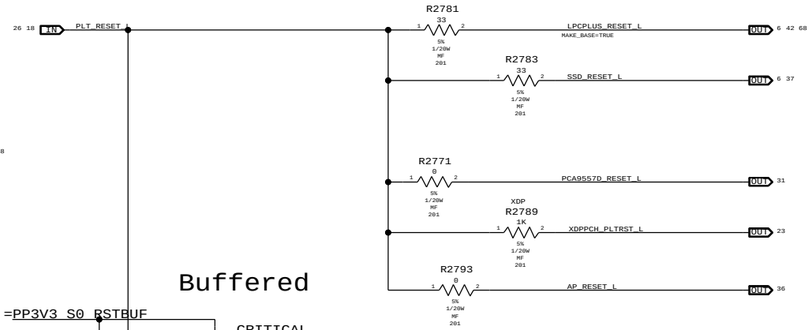
System RTC Power Source & 32kHz / 25MHz Clock Generator



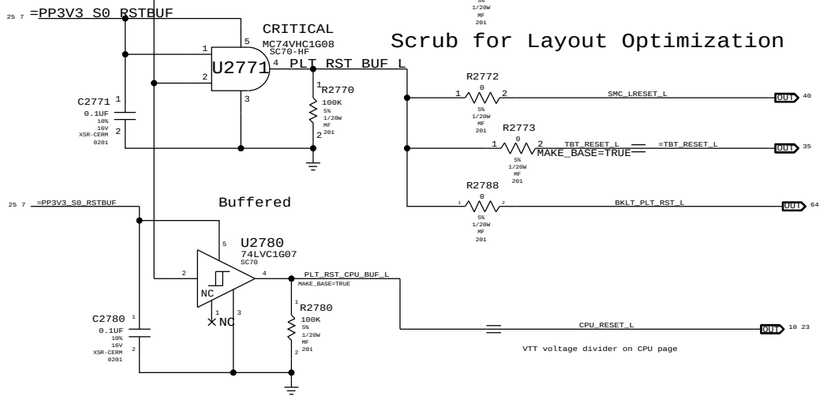


Platform Reset Connections

Unbuffered

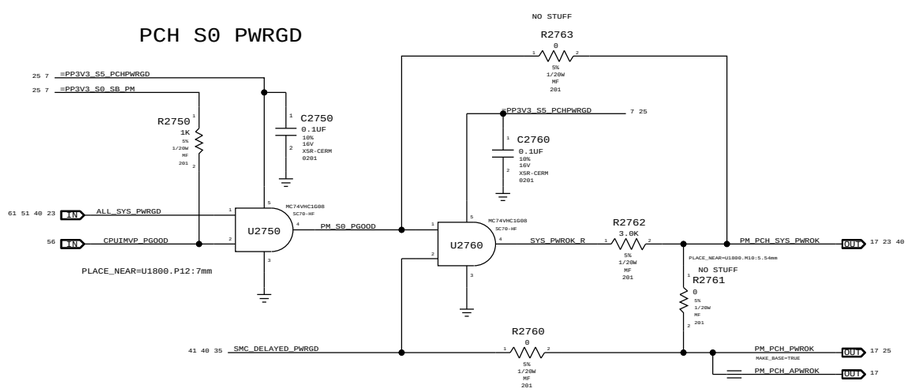


Buffered

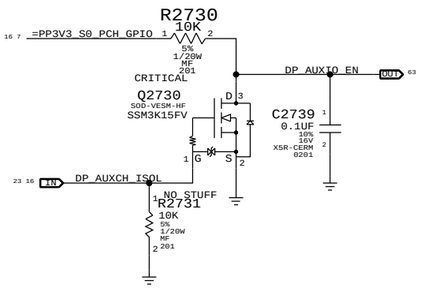


Scrub for Layout Optimization

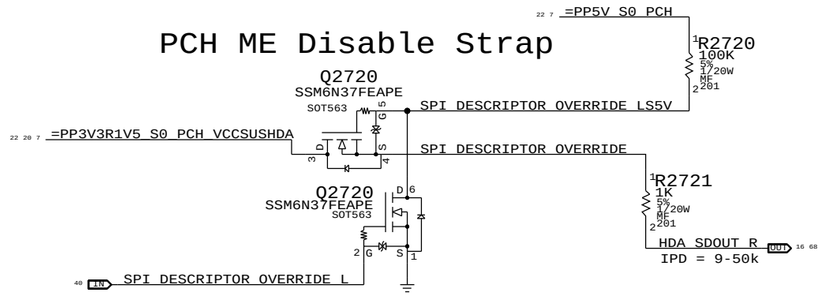
PCH S0 PWRGD



DP_AUXIO_EN Inversion

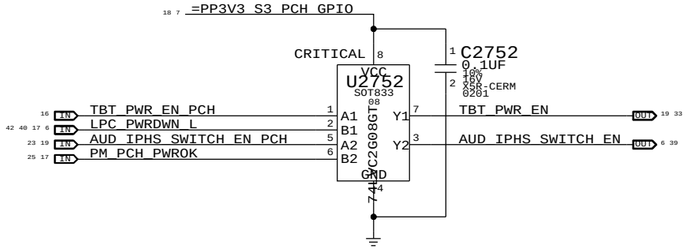


PCH ME Disable Strap

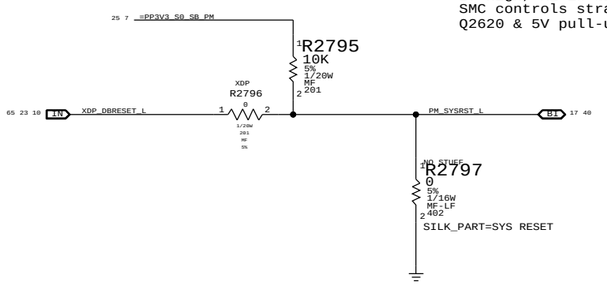


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

GPIO Glitch Prevention



PCH Reset Button



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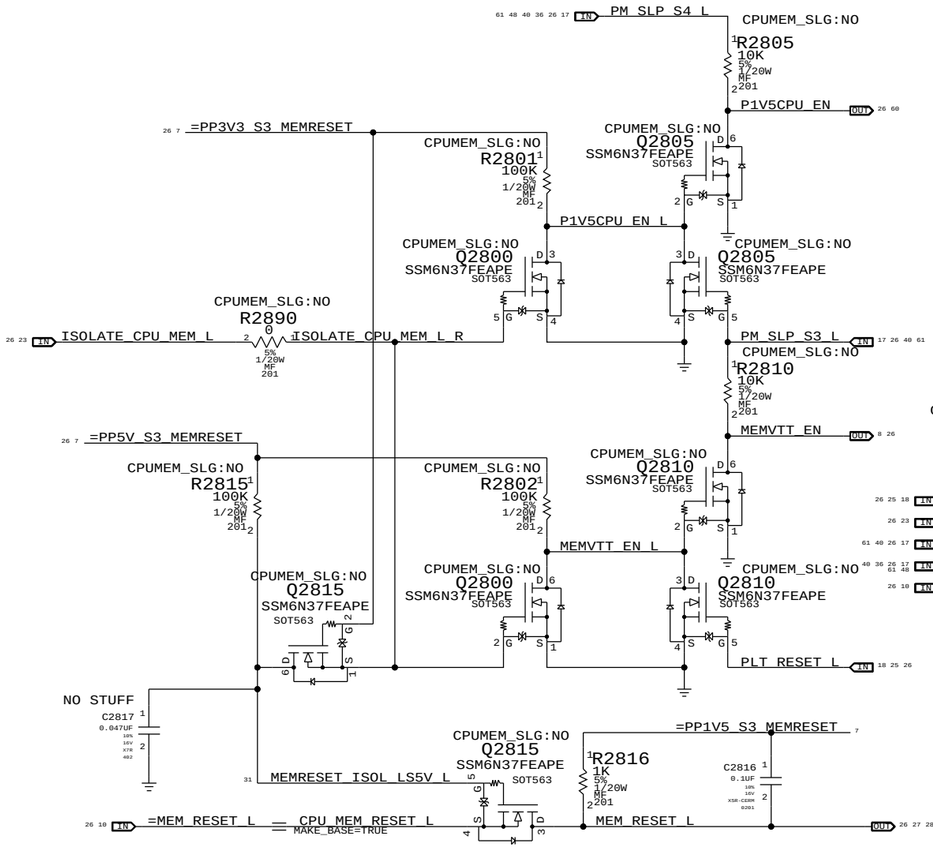
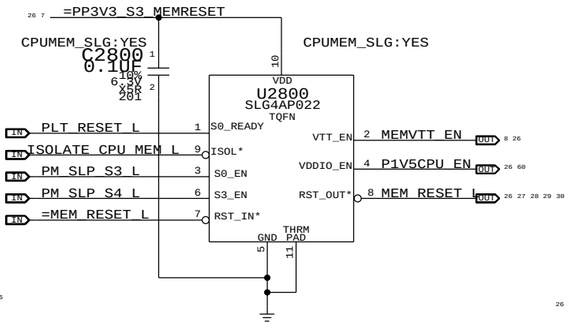
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

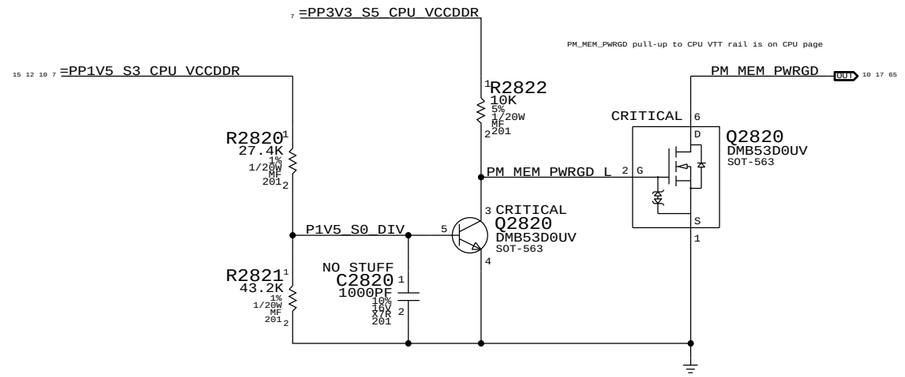
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



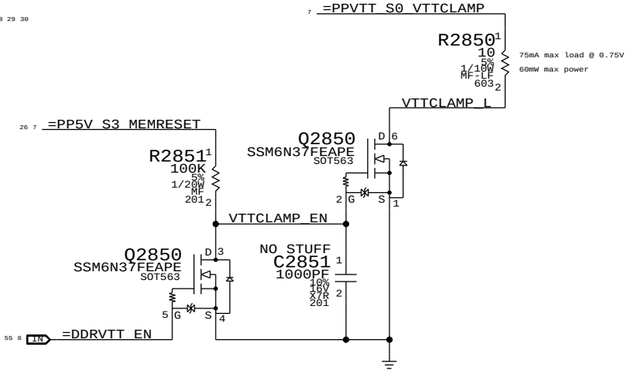


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
S3	2	0	0	1	1	1	0	1
	3	0	0	0	1	X	1	0
	4	0	0	1	1	X	1	0
to	5	0	1	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D
REVISION: 2.7.0
BRANCH:
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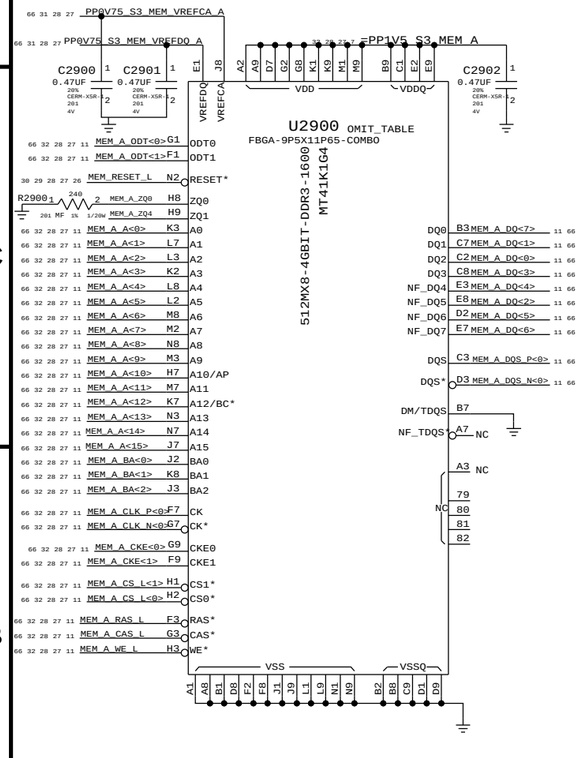
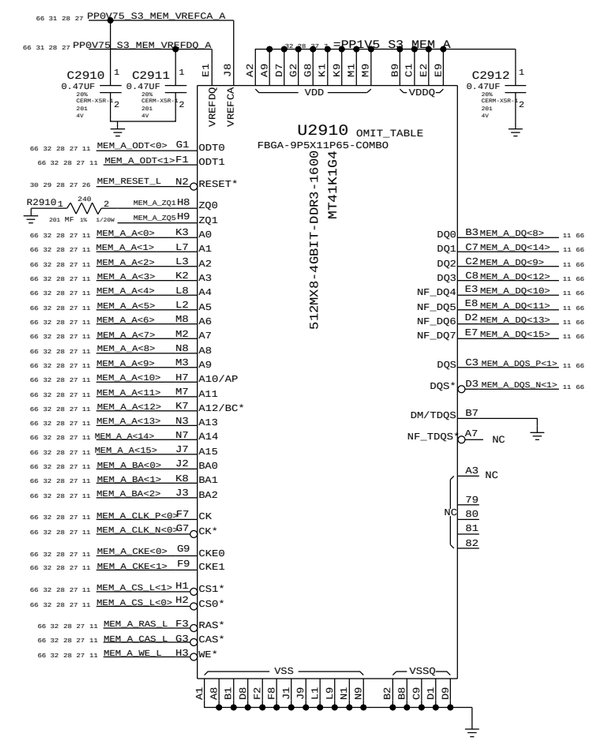
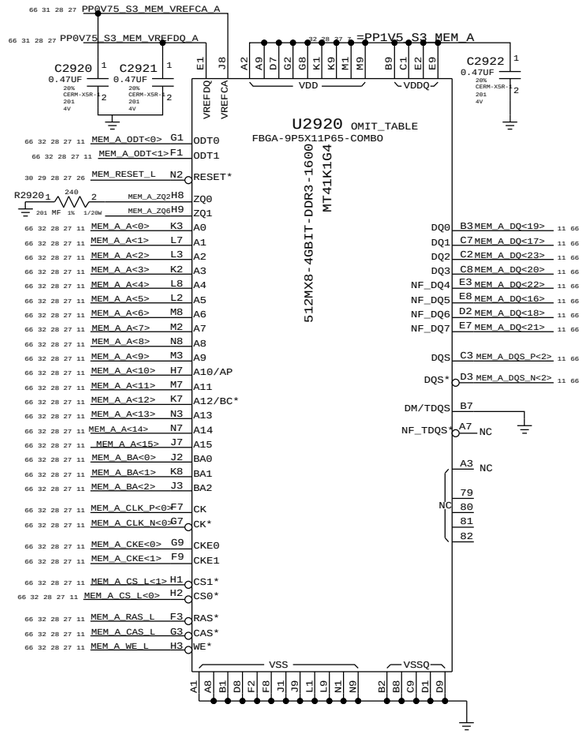
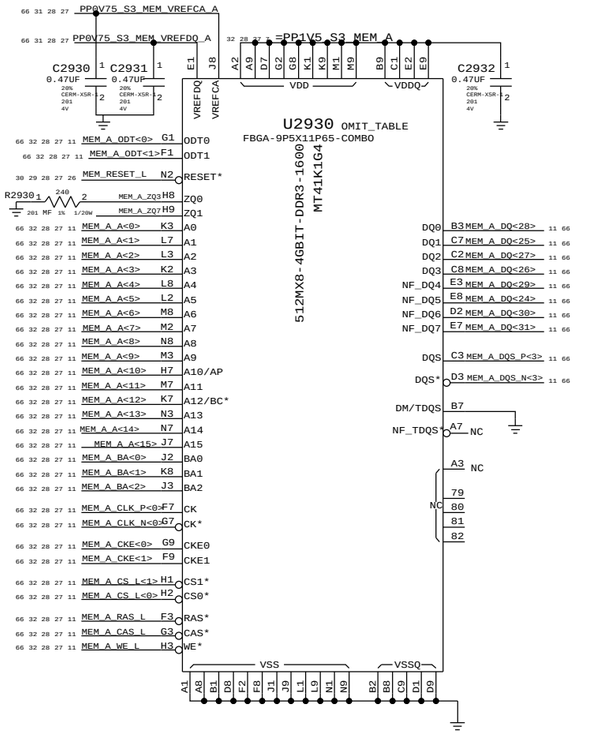
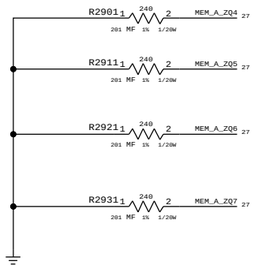








A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2011

PAGE TITLE

DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

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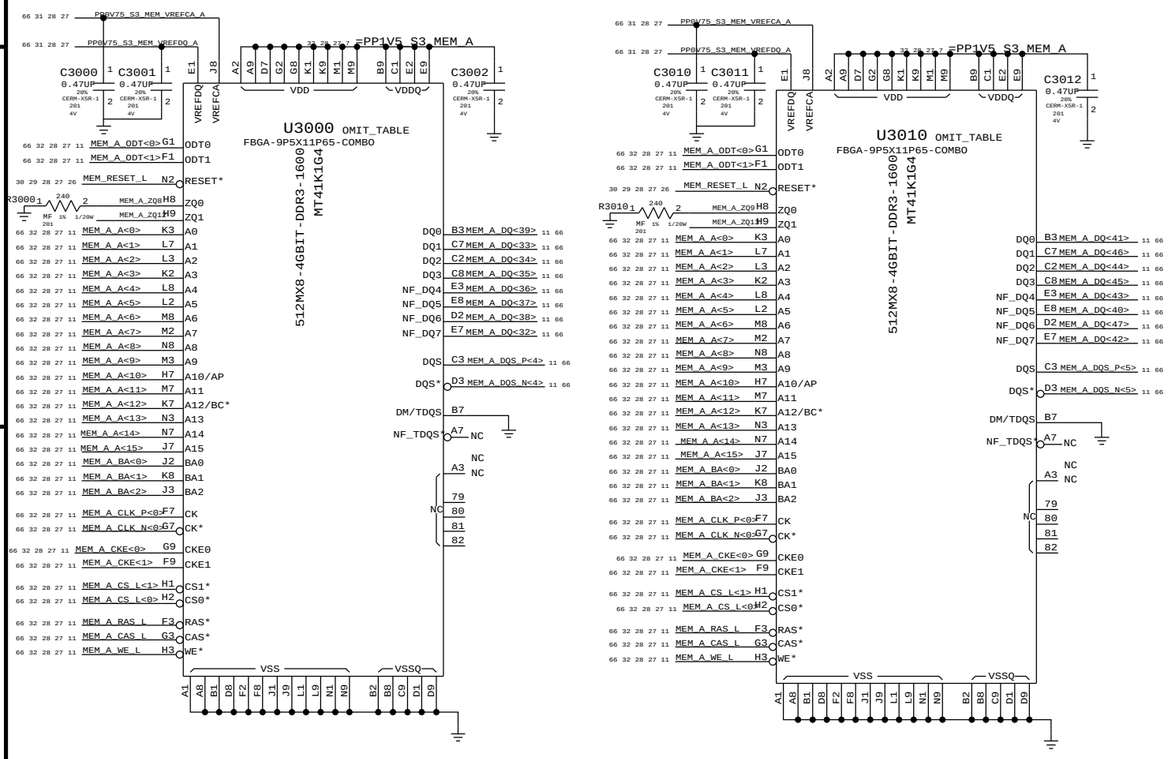
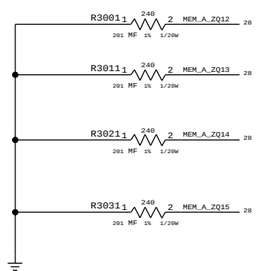


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB
SYNC_DATE=08/29/2011

PAGE TITLE
DDR3 DRAM CHANNEL A (32-63)

Apple Inc.

DRAWING NUMBER 051-9276
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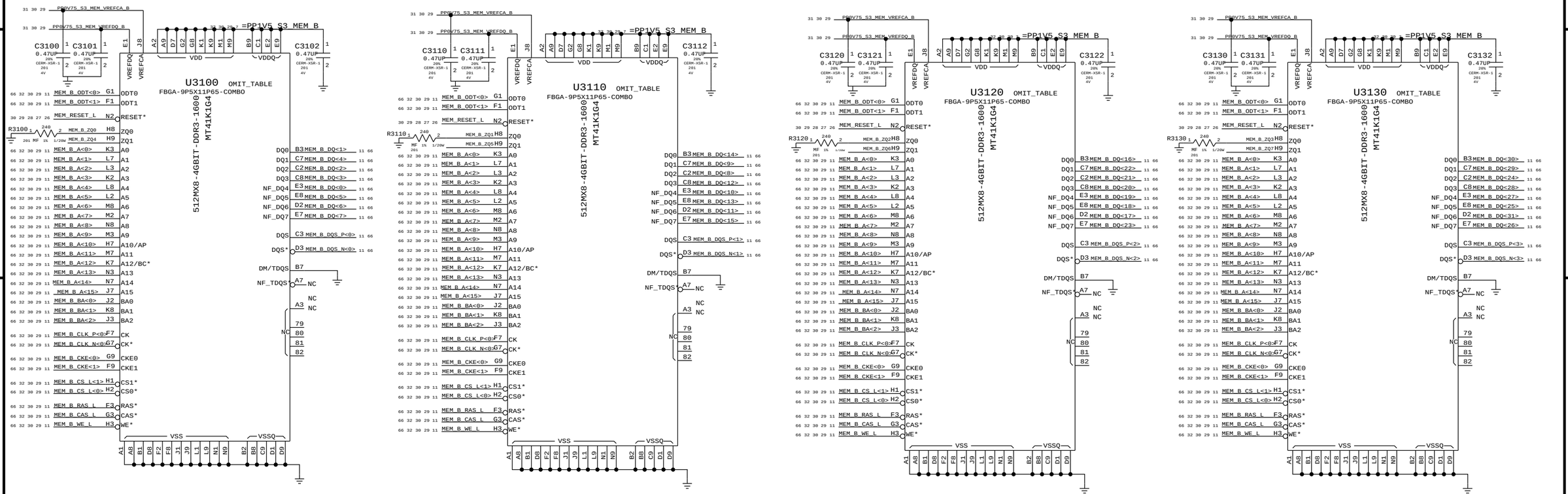
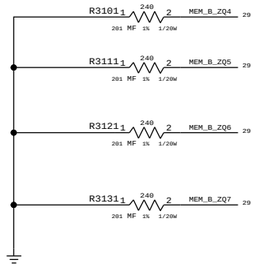


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2013

PAGE TITLE
DDR3 DRAM CHANNEL B (0-31)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
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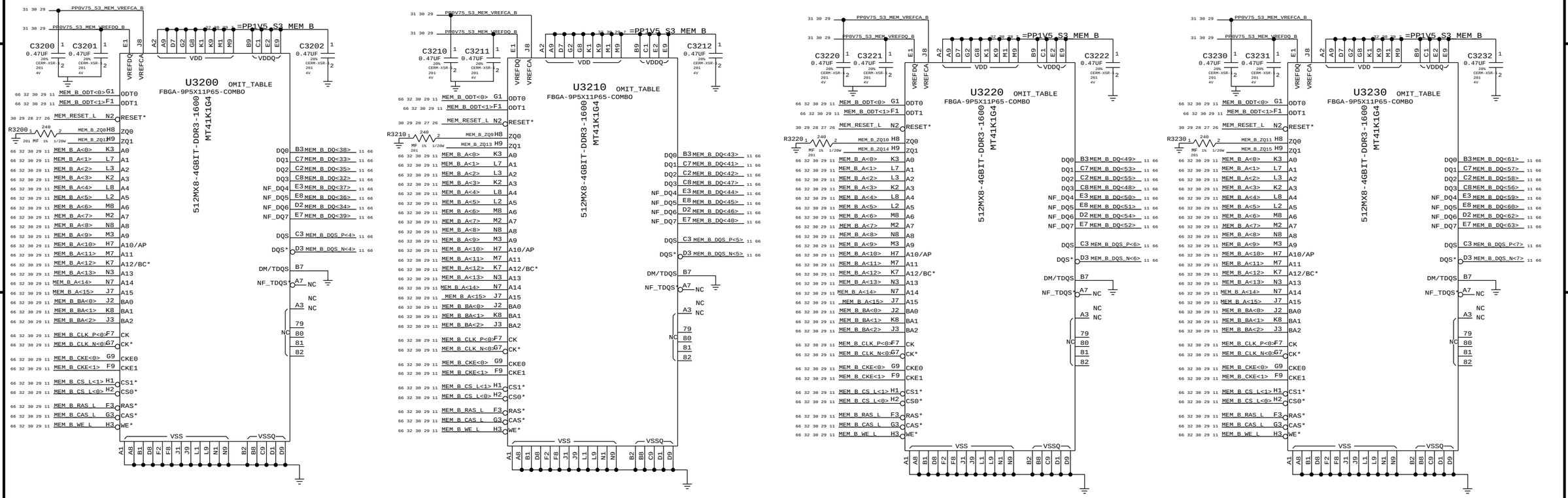
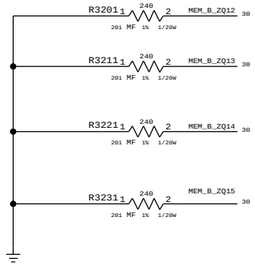


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=J13_MLB SYNC_DATE=08/29/2017

PAGE TITLE
DDR3 DRAM CHANNEL B (32-63)

Apple Inc.

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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0012	4	RES,MF,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
118S0303	1	RES,MF,332OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2013

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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=PP1V5_S3_MEM_A

C3408 2.2UF 20% 6.3V CERM 402-LF
C3400 2.2UF 20% 6.3V CERM 402-LF
C3409 2.2UF 20% 6.3V CERM 402-LF
C3401 2.2UF 20% 6.3V CERM 402-LF
C3410 2.2UF 20% 6.3V CERM 402-LF
C3420 2.2UF 20% 6.3V CERM 402-LF
C3411 2.2UF 20% 6.3V CERM 402-LF
C3421 2.2UF 20% 6.3V CERM 402-LF
C3412 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3404 2.2UF 20% 6.3V CERM 402-LF
C3405 2.2UF 20% 6.3V CERM 402-LF
C3414 2.2UF 20% 6.3V CERM 402-LF
C3424 2.2UF 20% 6.3V CERM 402-LF
C3415 2.2UF 20% 6.3V CERM 402-LF
C3425 2.2UF 20% 6.3V CERM 402-LF
C3416 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

=PP1V5_S3_MEM_A

C3418 2.2UF 20% 6.3V CERM 402-LF
C3430 2.2UF 20% 6.3V CERM 402-LF
C3440 2.2UF 20% 6.3V CERM 402-LF
C3450 2.2UF 20% 6.3V CERM 402-LF
C3419 2.2UF 20% 6.3V CERM 402-LF
C3431 2.2UF 20% 6.3V CERM 402-LF
C3441 2.2UF 20% 6.3V CERM 402-LF
C3451 2.2UF 20% 6.3V CERM 402-LF
C3442 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3434 2.2UF 20% 6.3V CERM 402-LF
C3444 2.2UF 20% 6.3V CERM 402-LF
C3454 2.2UF 20% 6.3V CERM 402-LF
C3435 2.2UF 20% 6.3V CERM 402-LF
C3445 2.2UF 20% 6.3V CERM 402-LF
C3455 2.2UF 20% 6.3V CERM 402-LF
C3446 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

=PP0V75_S0_MEM_VTT_A

MEM_A_CKE<0>	RP3401	36	4 5	5%1/32W 4X0201
MEM_A_WE_L	RP3402	36	2 7	5%1/32W 4X0201
MEM_A_A<7>	RP3406	36	2 7	5%1/32W 4X0201
MEM_A_BA<0>	RP3403	36	1 8	5%1/32W 4X0201
MEM_A_CS_L<0>	RP3402	36	1 8	5%1/32W 4X0201
MEM_A_ODT<0>	RP3401	36	2 7	5%1/32W 4X0201
MEM_A_A<12>	RP3403	36	2 7	5%1/32W 4X0201
MEM_A_A<14>	RP3407	36	3 6	5%1/32W 4X0201
MEM_A_A<2>	RP3406	36	1 8	5%1/32W 4X0201
MEM_A_A<11>	RP3406	36	4 5	5%1/32W 4X0201
MEM_A_A<10>	RP3402	36	3 6	5%1/32W 4X0201
MEM_A_A<3>	RP3404	36	3 6	5%1/32W 4X0201
MEM_A_A<0>	RP3403	36	4 5	5%1/32W 4X0201
MEM_A_A<4>	RP3404	36	1 8	5%1/32W 4X0201
MEM_A_A<8>	RP3407	36	2 7	5%1/32W 4X0201
MEM_A_BA<2>	RP3402	36	4 5	5%1/32W 4X0201
MEM_A_BA<1>	RP3403	36	3 6	5%1/32W 4X0201
MEM_A_A<6>	RP3407	36	1 8	5%1/32W 4X0201
MEM_A_A<13>	RP3407	36	4 5	5%1/32W 4X0201
MEM_A_A<1>	RP3404	36	2 7	5%1/32W 4X0201
MEM_A_A<5>	RP3404	36	4 5	5%1/32W 4X0201
MEM_A_CAS_L	RP3401	36	3 6	5%1/32W 4X0201
MEM_A_RAS_L	RP3401	36	1 8	5%1/32W 4X0201
MEM_A_A<9>	RP3406	36	3 6	5%1/32W 4X0201
MEM_A_CKE<1>	RP3405	36	1 8	5%1/32W 4X0201
MEM_A_ODT<1>	RP3405	36	2 7	5%1/32W 4X0201
MEM_A_CS_L<1>	RP3405	36	3 6	5%1/32W 4X0201
MEM_A_A<15>	RP3405	36	4 5	5%1/32W 4X0201

C3480 0.47UF 20% 4V CERM-X5R-1 201
C3482 0.47UF 20% 4V CERM-X5R-1 201
C3483 0.47UF 20% 4V CERM-X5R-1 201
C3484 0.47UF 20% 4V CERM-X5R-1 201
C3485 0.47UF 20% 4V CERM-X5R-1 201
C3486 0.47UF 20% 4V CERM-X5R-1 201
C3487 0.47UF 20% 4V CERM-X5R-1 201
C3488 0.47UF 20% 4V CERM-X5R-1 201
C3493 0.47UF 20% 4V CERM-X5R-1 201
C3489 0.47UF 20% 4V CERM-X5R-1 201

=PP1V5_S3_MEM_B

C3428 2.2UF 20% 6.3V CERM 402-LF
C3402 2.2UF 20% 6.3V CERM 402-LF
C3429 2.2UF 20% 6.3V CERM 402-LF
C3403 2.2UF 20% 6.3V CERM 402-LF
C3470 2.2UF 20% 6.3V CERM 402-LF
C3422 2.2UF 20% 6.3V CERM 402-LF
C3471 2.2UF 20% 6.3V CERM 402-LF
C3423 2.2UF 20% 6.3V CERM 402-LF
C3472 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3406 2.2UF 20% 6.3V CERM 402-LF
C3407 2.2UF 20% 6.3V CERM 402-LF
C3474 2.2UF 20% 6.3V CERM 402-LF
C3426 2.2UF 20% 6.3V CERM 402-LF
C3475 2.2UF 20% 6.3V CERM 402-LF
C3427 2.2UF 20% 6.3V CERM 402-LF
C3476 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

=PP1V5_S3_MEM_B

C3438 2.2UF 20% 6.3V CERM 402-LF
C3432 2.2UF 20% 6.3V CERM 402-LF
C3490 2.2UF 20% 6.3V CERM 402-LF
C3452 2.2UF 20% 6.3V CERM 402-LF
C3439 2.2UF 20% 6.3V CERM 402-LF
C3433 2.2UF 20% 6.3V CERM 402-LF
C3491 2.2UF 20% 6.3V CERM 402-LF
C3453 2.2UF 20% 6.3V CERM 402-LF
C3492 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

C3436 2.2UF 20% 6.3V CERM 402-LF
C3494 2.2UF 20% 6.3V CERM 402-LF
C3456 2.2UF 20% 6.3V CERM 402-LF
C3437 2.2UF 20% 6.3V CERM 402-LF
C3495 2.2UF 20% 6.3V CERM 402-LF
C3457 2.2UF 20% 6.3V CERM 402-LF
C3496 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

=PP0V75_S0_MEM_VTT_B

MEM_B_RAS_L	RP3413	36	1 8	5%1/32W 4X0201
MEM_B_A<8>	RP3410	36	1 8	5%1/32W 4X0201
MEM_B_CKE<0>	RP3409	36	1 8	5%1/32W 4X0201
MEM_B_A<7>	RP3411	36	4 5	5%1/32W 4X0201
MEM_B_BA<0>	RP3409	36	3 6	5%1/32W 4X0201
MEM_B_A<13>	RP3410	36	3 6	5%1/32W 4X0201
MEM_B_BA<1>	RP3408	36	4 5	5%1/32W 4X0201
MEM_B_ODT<0>	RP3413	36	3 6	5%1/32W 4X0201
MEM_B_A<5>	RP3411	36	2 7	5%1/32W 4X0201
MEM_B_WE_L	RP3413	36	4 5	5%1/32W 4X0201
MEM_B_A<11>	RP3411	36	3 6	5%1/32W 4X0201
MEM_B_BA<2>		36	4 5	5%1/32W 4X0201
MEM_B_A<12>	RP3408	36	2 7	5%1/32W 4X0201
MEM_B_A<0>	RP3408	36	3 6	5%1/32W 4X0201
MEM_B_CS_L<0>	RP3409	36	2 7	5%1/32W 4X0201
MEM_B_A<14>	RP3410	36	4 5	5%1/32W 4X0201
MEM_B_A<4>	RP3414	36	4 5	5%1/32W 4X0201
MEM_B_A<10>	RP3408	36	1 8	5%1/32W 4X0201
MEM_B_A<9>	RP3410	36	2 7	5%1/32W 4X0201
MEM_B_A<3>	RP3414	36	2 7	5%1/32W 4X0201
MEM_B_A<1>	RP3414	36	1 8	5%1/32W 4X0201
MEM_B_CAS_L	RP3413	36	2 7	5%1/32W 4X0201
MEM_B_A<2>	RP3414	36	3 6	5%1/32W 4X0201
MEM_B_A<6>	RP3411	36	1 8	5%1/32W 4X0201
MEM_B_CKE<1>	RP3412	36	1 8	5%1/32W 4X0201
MEM_B_ODT<1>	RP3412	36	2 7	5%1/32W 4X0201
MEM_B_A<15>	RP3412	36	3 6	5%1/32W 4X0201
MEM_B_CS_L<1>	RP3412	36	4 5	5%1/32W 4X0201

C3481 0.47UF 20% 4V CERM-X5R-1 201
C3460 0.47UF 20% 4V CERM-X5R-1 201
C3461 0.47UF 20% 4V CERM-X5R-1 201
C3462 0.47UF 20% 4V CERM-X5R-1 201
C3463 0.47UF 20% 4V CERM-X5R-1 201
C3464 0.47UF 20% 4V CERM-X5R-1 201
C3465 0.47UF 20% 4V CERM-X5R-1 201
C3466 0.47UF 20% 4V CERM-X5R-1 201
C3467 0.47UF 20% 4V CERM-X5R-1 201
C3477 0.47UF 20% 4V CERM-X5R-1 201

MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM

MEM_A_CLK_N<0>
R3468 30 5% 1/20W MF 201
MEM_A_CLK_TERM_R VOLTAGE=0V
C3469 0.1UF 10% X5R 201 6.3V
C3468 3.3PF 5% 25V CERM 201
MEM_A_CLK_P<0>
R3469 30 5% 1/20W MF 201

MEM_B_CLK_N<0>
R3478 30 5% 1/20W MF 201
MEM_B_CLK_TERM_R VOLTAGE=0V
C3479 0.1UF 10% X5R 201 6.3V
C3478 3.3PF 5% 25V CERM 201
MEM_B_CLK_P<0>
R3479 30 5% 1/20W MF 201

SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE: DDR3 DRAM Channel B (32-63)	
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
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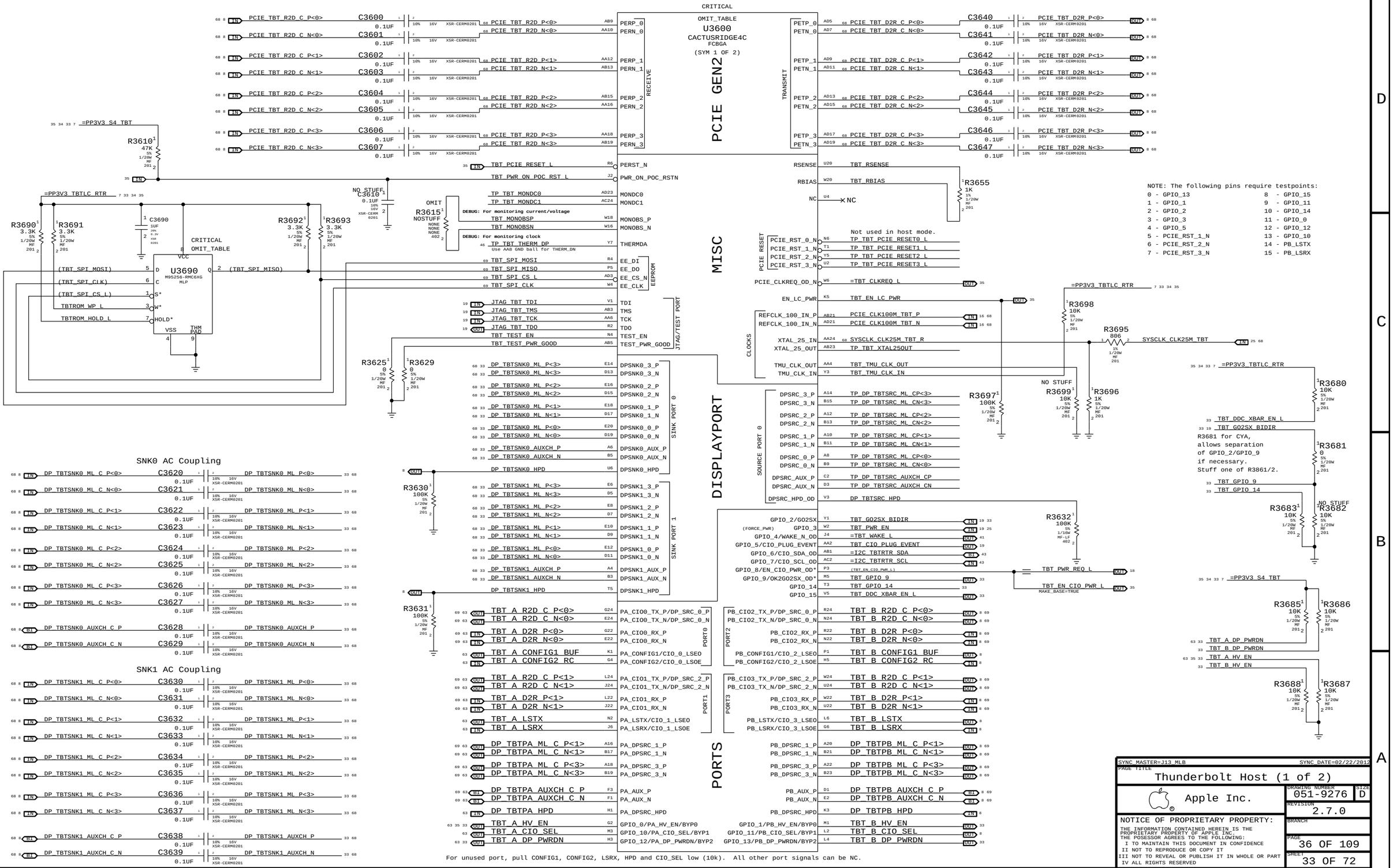

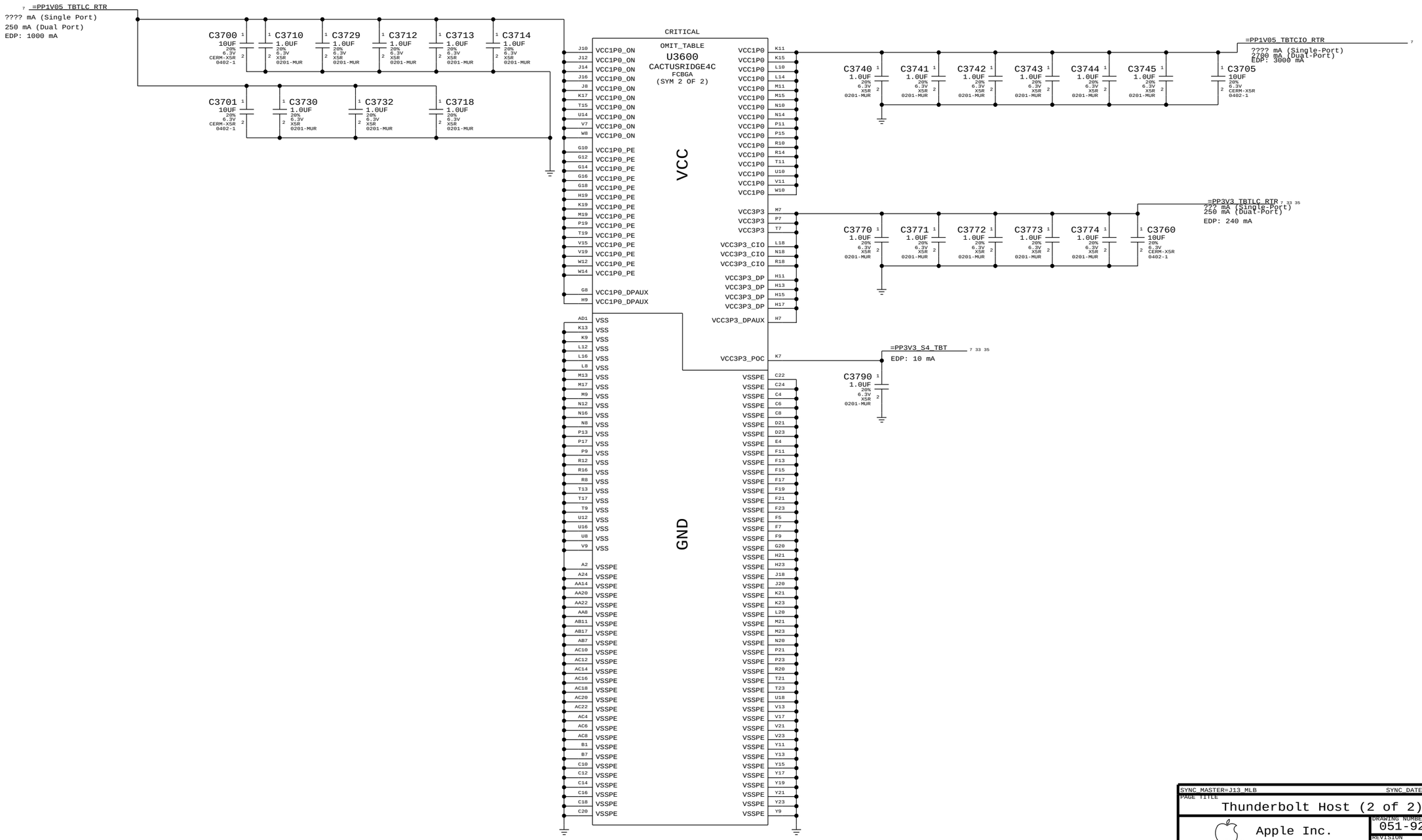

SYNC_MASTER=J13_MLB SYNC_DATE=09/01/2011

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP18V_TBT_REG (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.

TBT 15V Boost Regulator

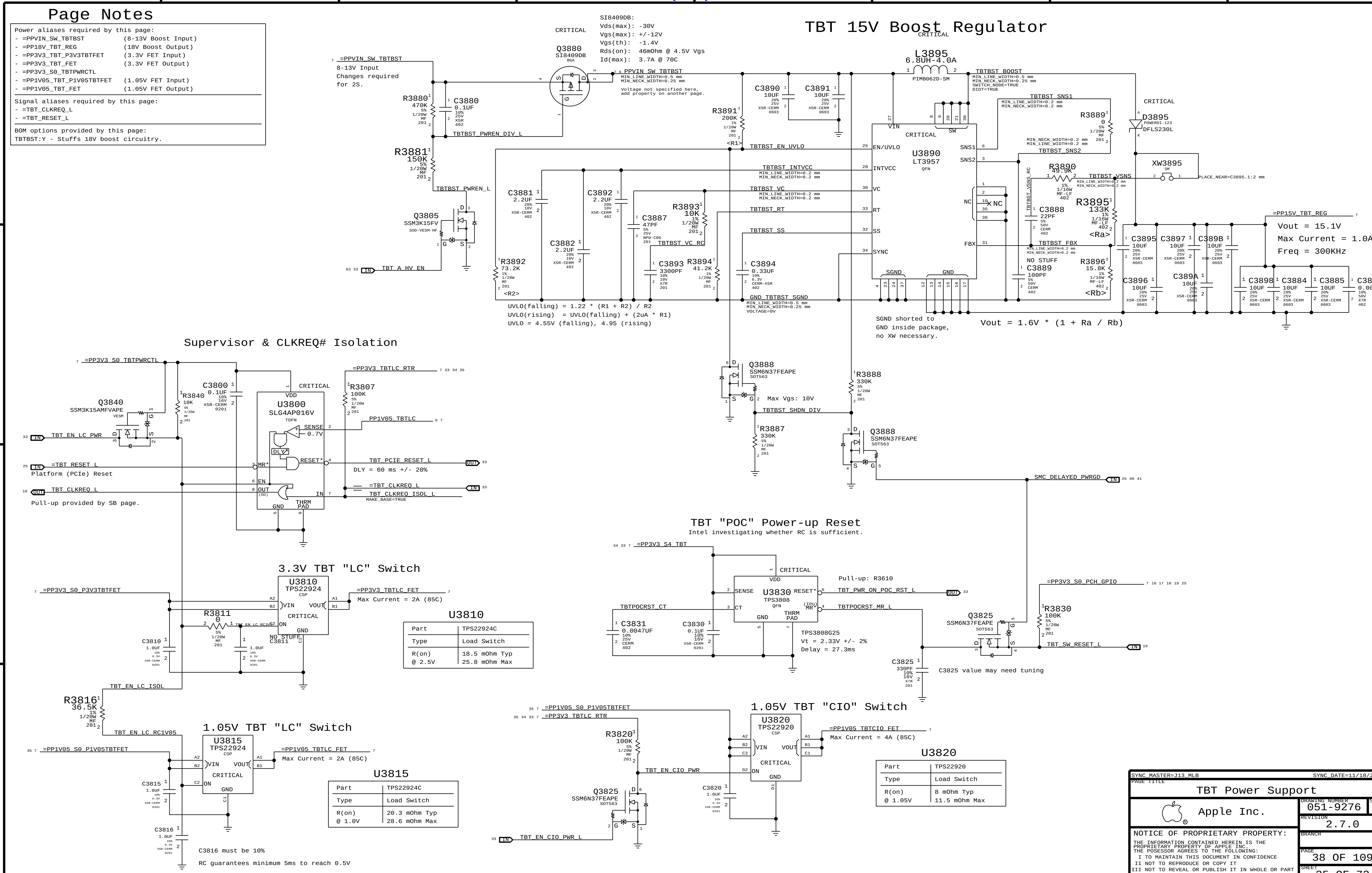
Supervisor & CLKREQ# Isolation

TBT "POC" Power-up Reset

3.3V TBT "LC" Switch

1.05V TBT "LC" Switch

1.05V TBT "CIO" Switch



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

U3815

Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: TBT Power Support

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

AIRPORT

CRITICAL
J4001
SSD-K99
F-RT-SM1

514S0335

PP3V3_S3RS4_BT_F
WIFI_EVENT_L
PCIE_AP_R2D_N
PCIE_AP_R2D_C_N
PCIE_AP_R2D_P
PCIE_AP_R2D_C_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_WAKE_L

C4030 0.1UF 10% 6.3V X5R 201
PLACEMENT_NOTE=Place close to J4001.
C4031 0.1UF 10% 6.3V X5R 201
PLACEMENT_NOTE=Place close to J4001.

BLUETOOTH

USB_BT_CONN_N
USB_BT_CONN_P

R4001 0 5% 1/16W MF-LF 402
=PP3V3_S4_BT
R4002 0 5% 1/16W MF-LF 402
=PP3V3_S3_BT

C4032 0.1UF 10% 6.3V X5R 201
PLACE_NEAR=J4001.18:1.5mm

3V S3 WLAN FET

MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON)	14-20 mOHM @2.5V
LOADING	0.750 A (EDP)

CRITICAL
R4052 0.020 1% 0.25W MF 805
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

PP3V3_WLAN_F
PP3V3_WLAN_R

C4021 0.1UF 10% 6.3V X5R 201
C4020 10UF 20% 16V X5R 603
PLACEMENT_NOTE=Place close to Q4050.

CRITICAL
Q4050
DMP2018LFK
DFN2563-6

C4050 0.1UF 10% 16V X5R-CERM 0201
C4051 0.033UF 10% 16V X5R 402
R4050 100K 5% 1/20W MF 201
P3V3WLAN_SS
R4051 10K 5% 1/20W MF 201
=PP3V3_S3_WLAN
PM_WLAN_EN_L

ISNS_AIRPORT_P
ISNS_AIRPORT_N

NOSTUFF R4017 15K 1% 1/20W MF 201
BTPWR:S3 R4018 0 5% 1/20W MF 201
PP3V3_S3RS4_BT_F
C4010 0.1UF 10% 6.3V X5R 201
NOSTUFF R4014 15K 1% 1/20W MF 201
BTPWR:S4 Q4010 SSM3K15FV SOD-VESM-HF
=BT_WAKE_L

U4010 PI3USB102ZLE TQFN CRITICAL
VCC
USB_BT_WAKE_P
USB_BT_WAKE_N
USB_BT_P
USB_BT_N
SEL
GND
OE*

NOSTUFF R4015 15K 1% 1/20W MF 201
NOSTUFF R4016 15K 1% 1/20W MF 201
BTPWR:S4 R4012 15K 1% 1/20W MF 201
NOSTUFF R4013 15K 1% 1/20W MF 201

BTPWR:S4 R4011 0 5% 1/20W MF 201
PM_SLP_S4_L
BTMUX_SEL
NOSTUFF C4011 0.01UF 10% 16V CERM 402

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

DLY = 60 MS +/- 20%

R4053 100K 5% 1/20W MF 201
R4054 232K 1% 1/20W MF 201
R4055 100K 1% 1/20W MF 201

CRITICAL
U4002
SLG4AP016V
TDFN
VDD
SENSE 0.7V
RESET*
KDLY
MR*
EN
OUT (OD)
IN
THRM PAD
GND

C4053 0.1UF 10% 16V X5R 201

P3V3WLAN_VMON
AP_RESET_CONN_L
AP_CLKREQ_Q_L
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L_R
R4090 0 5% 1/20W MF 201
AP_CLKREQ_L

SYNC MASTER=J13_MLB
SYNC_DATE=10/06/2013
PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9276
SIZE D
REVISION 2.7.0
BRANCH
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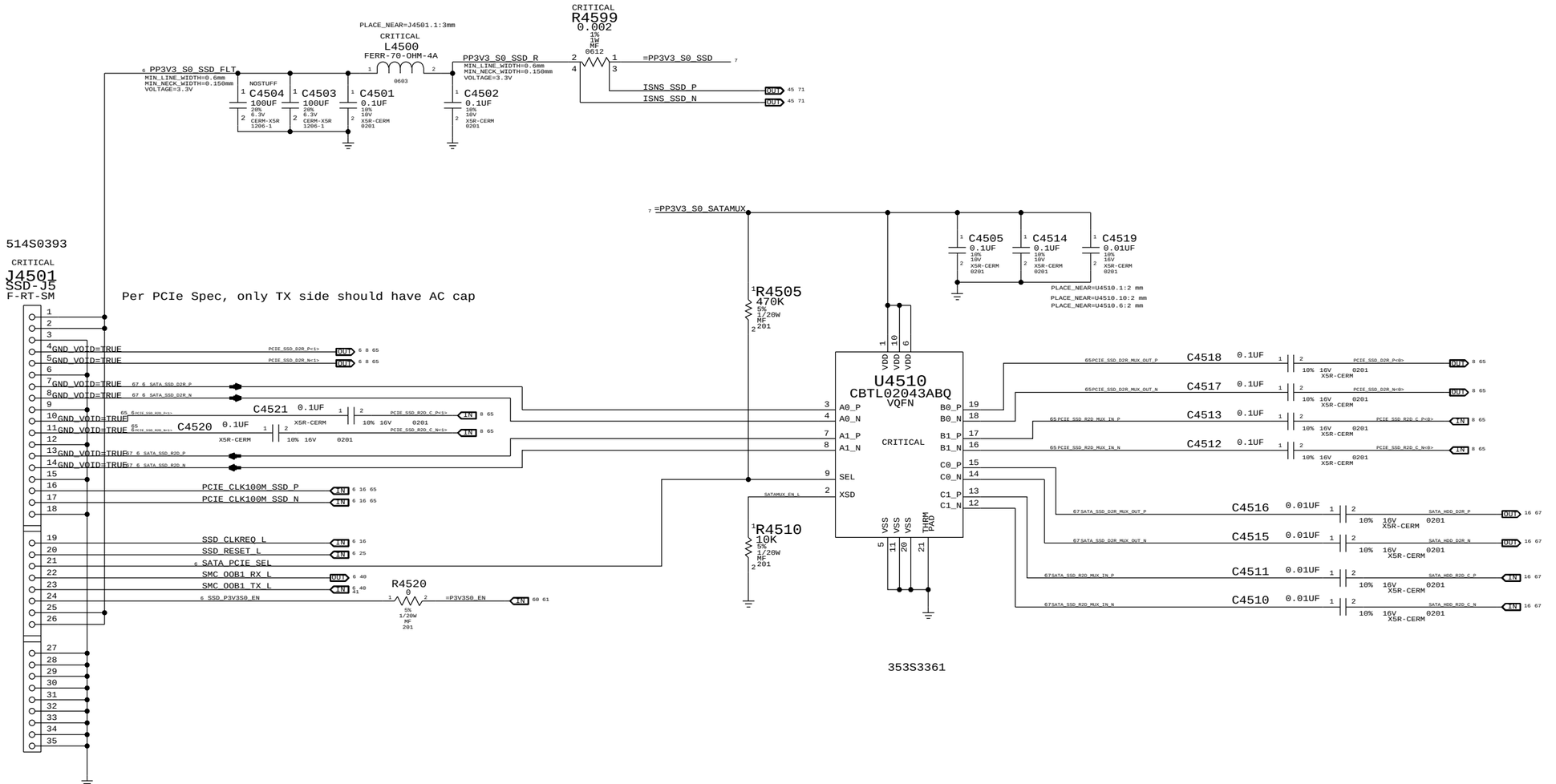

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC_MASTER=J13_MLB	SYNC_DATE=11/18/2011
PAGE TITLE	SSD CONNECTOR
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
	REVISION 2.7.0
	BRANCH
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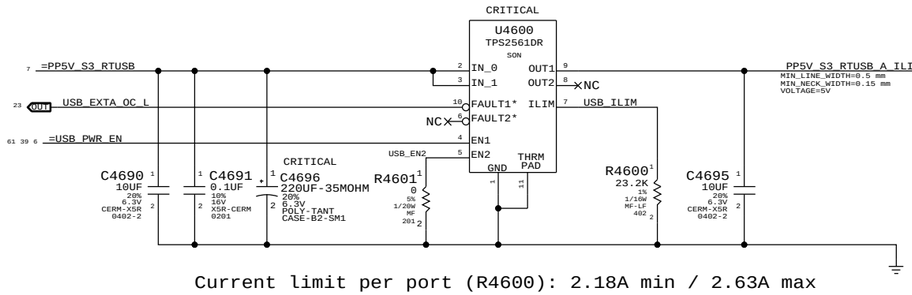
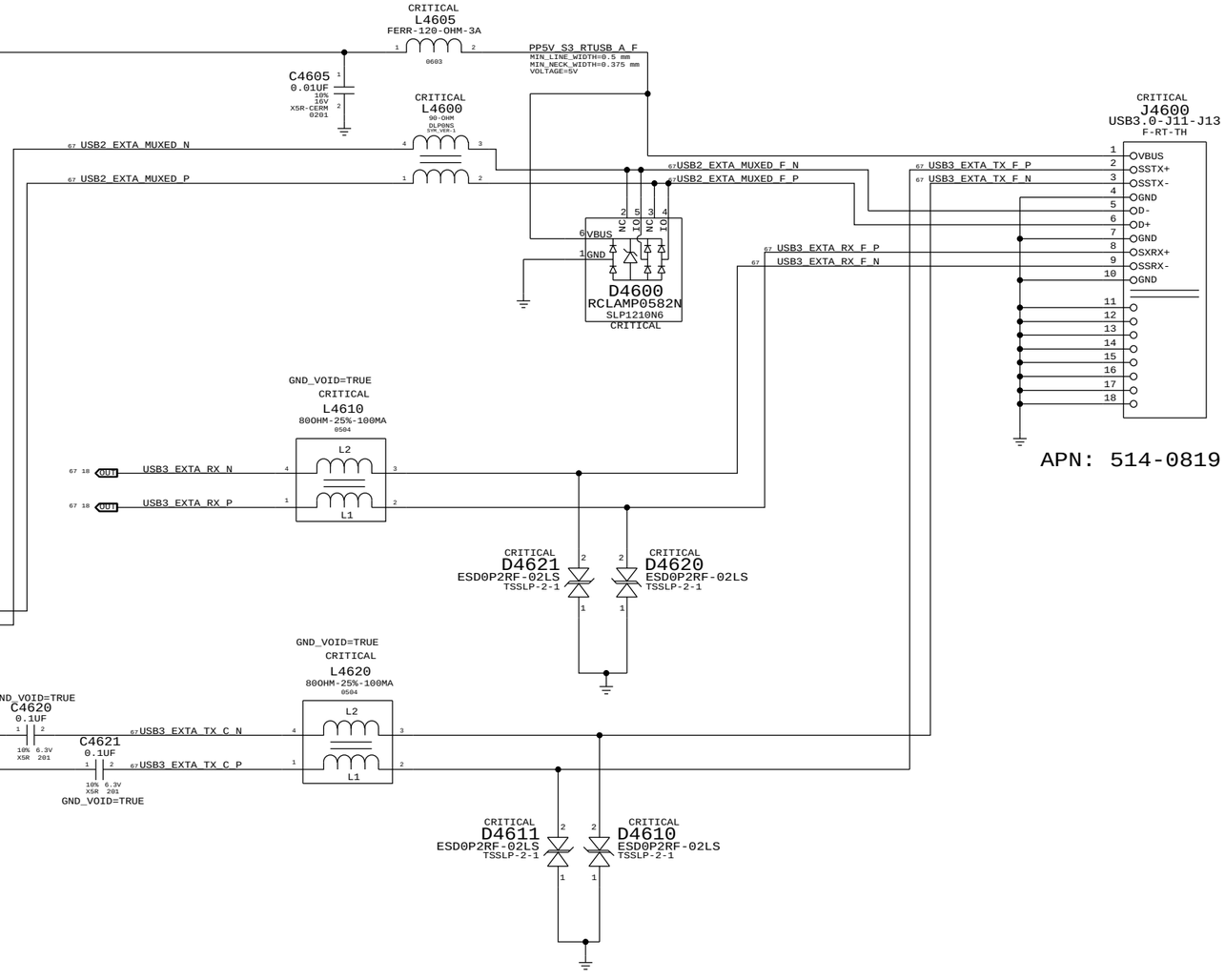
Right USB Port A

USB Port Power Switch

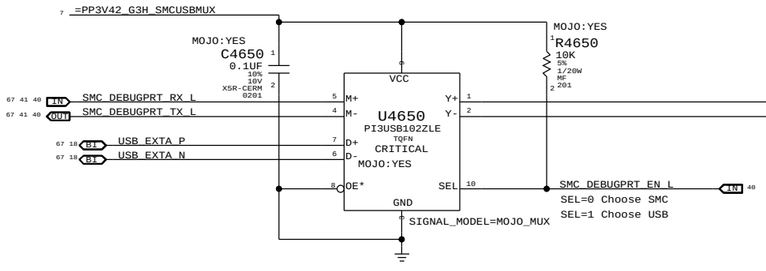


Current limit per port (R4600): 2.18A min / 2.63A max



APN: 514-0819

Mojo SMC Debug Mux



SYNC_MASTER=J13_MLB	SYNC_DATE=10/06/2011
PAGE TITLE: External A USB3 Connector	
Apple Inc.	DRAWING NUMBER: 051-9276 SIZE: D
	REVISION: 2.7.0
	BRANCH:
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LIO CONNECTOR
998-4617 (HIROSE 3.0mm RCPT)

=PP3V3_S0_AUDIO

C4700 0.1UF 10% 16V X5R-CERM 0201 PLACE_NEAR=J4700.5:1.5mm

=PP3V3R1V5_S0_AUDIO

C4720 0.1UF 10% 16V X5R-CERM 0201 PLACE_NEAR=J4700.7:1.5mm

C4710 0.1UF 10% 16V X5R-CERM 0201 PLACE_NEAR=J4700.9:1.5mm

CRITICAL
J4700
DF40CG3.0-48DS-0.4V
F-ST-SM

SPKRAMP_INR_P	1	2	
SPKRAMP_INR_N	3	4	USB_EXTB_P
	5	6	USB_EXTB_N
	7	8	
	9	10	
=PP3V42_G3H_ONEWIRE	11	12	USB3_EXTB_RX_RC_N
AUD_GPIO_3	13	14	USB3_EXTB_RX_RC_P
	15	16	
=I2C_MIKEY_SCL	19	20	USB_CAMERA_P
=I2C_MIKEY_SDA	21	22	USB_CAMERA_N
AUD_IP_PERIPHERAL_DET	23	24	
	25	26	
=I2C_LIO_SCL	27	28	USB3_EXTB_TX_C_N
=I2C_LIO_SDA	29	30	USB3_EXTB_TX_C_P
	31	32	
HDA_RST_L	35	36	AUD_IPHS_SWITCH_EN
HDA_SDIN0	37	38	AUD_I2C_INT_L
	39	40	=USB_PWR_EN
HDA_BIT_CLK	41	42	USB_EXTB_OC_L
HDA_SYNC	43	44	SMC_BC_ACOK
HDA_SDOUT	45	46	SYS_ONEWIRE
	47	48	
	51	52	

GND_VOID=TRUE

CRITICAL
D4711
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
D4710
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
D4720
ESD0P2RF-02LS
TSSLP-2-1

CRITICAL
D4721
ESD0P2RF-02LS
TSSLP-2-1

R4710 0 1/20W 5% MF 201
NOSTUFF C4731 0.1UF X5R-CERM 10% 16V 0201
USB3_EXTB_RX_N

NOSTUFF C4732 0.1UF X5R-CERM 10% 16V 0201
R4720 0 1/20W 5% MF 201
USB3_EXTB_RX_P

C4721 0.1UF X5R-CERM 10% 16V 0201
USB3_EXTB_TX_N

C4722 0.1UF X5R-CERM 10% 16V 0201
USB3_EXTB_TX_P

ON MLB SIDE AS LIO CAN'T FIT CAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
LIO CONNECTORS

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D
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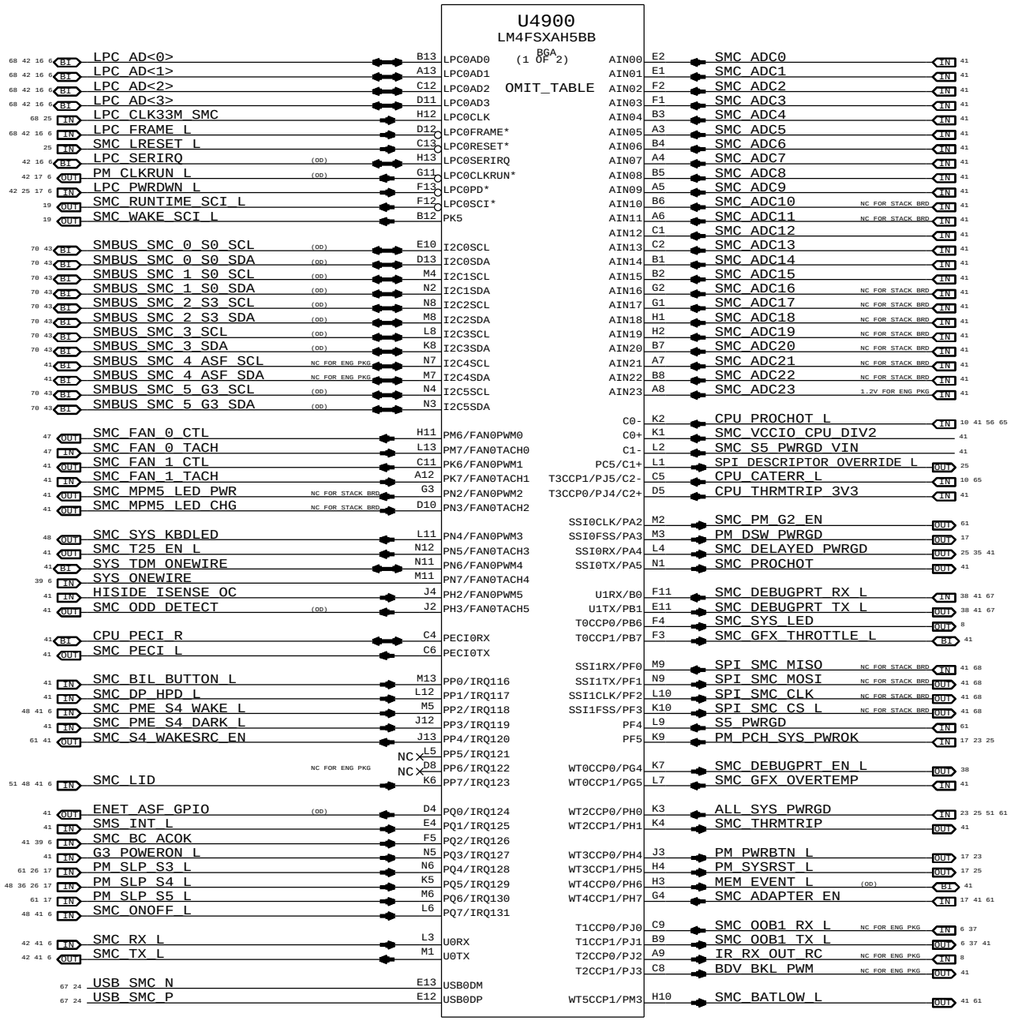

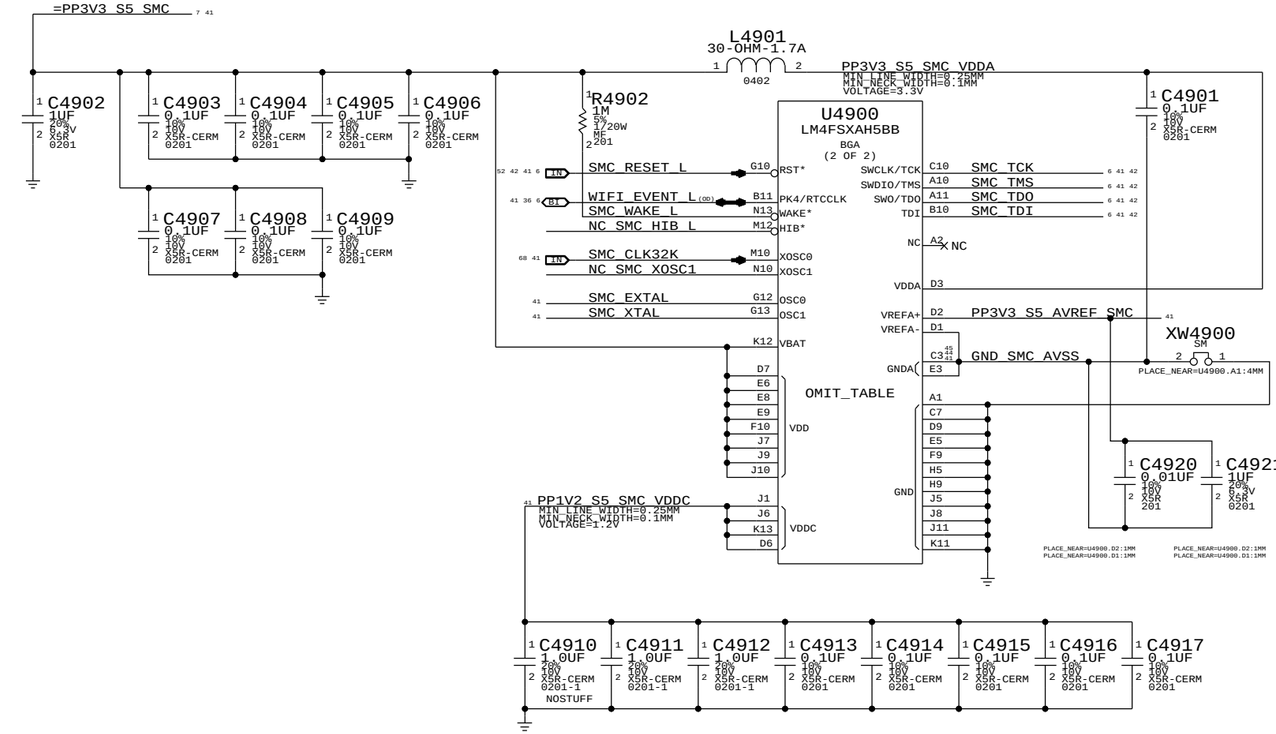

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=J30_MLB SYNC_DATE=07/26/2011

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D
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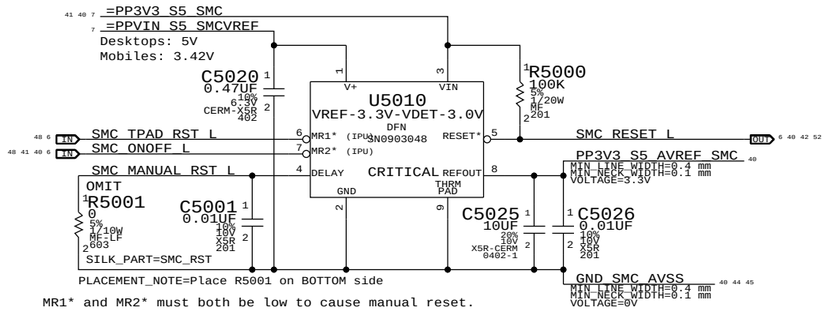
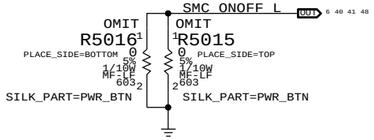
SMC Reset "Button", Supervisor & AVREF Supply



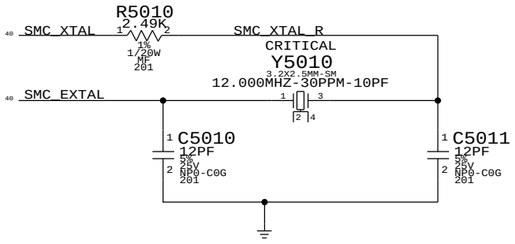
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



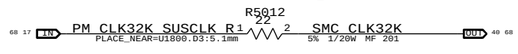
SMC Crystal Circuit

SMC USB Clock require these crystal
values:5,6,8,10,12,16,18,20,24,25 MHz



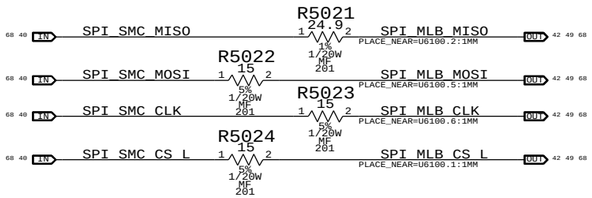
Note:
ADC10 and ADC11 are shared
with comparators on Stack Board.

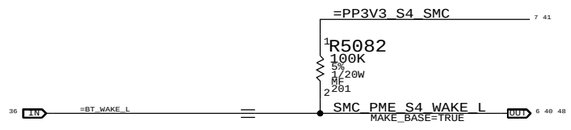
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_VCCSA_VSENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_HS_COMPUTING_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	SMC_CPU_SA_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	SMC_3V3S0_ISENSE	MAKE_BASE=TRUE
SMC_ADC15	SMC_WLAN_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC17	NC_SCM_ADC17	MAKE_BASE=TRUE
SMC_ADC18	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE
SMC_ADC23	SMC_ADC23	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	MAKE_BASE=TRUE
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR	MAKE_BASE=TRUE
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG	MAKE_BASE=TRUE
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	MAKE_BASE=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE
BDV_BKL_PWM	NC_BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	=TBT_WAKE_L	MAKE_BASE=TRUE
SMC_T25_EN_L	NC_SMC_T25_EN_L	MAKE_BASE=TRUE

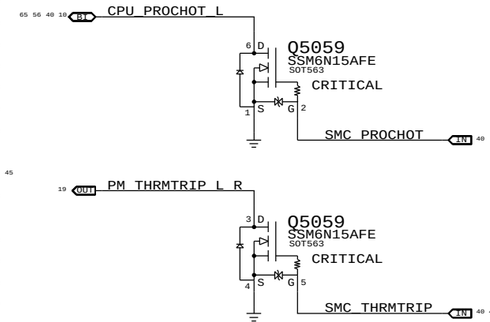


SMC12 SPI Support

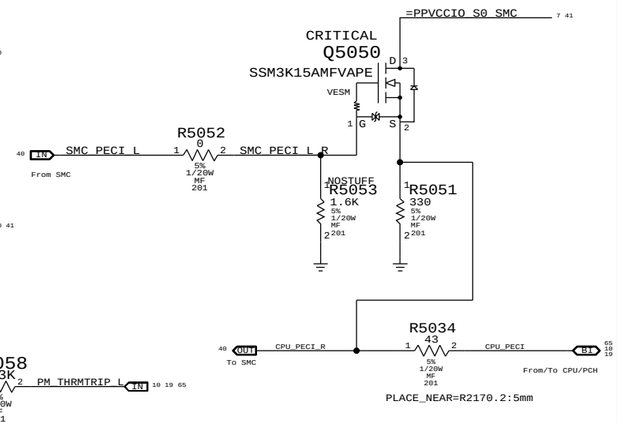
Series resistors are no stuffed until the
topology of 2 SPI Masters are verified.





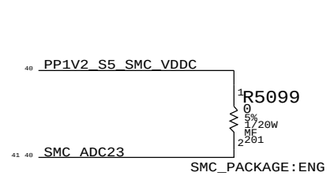


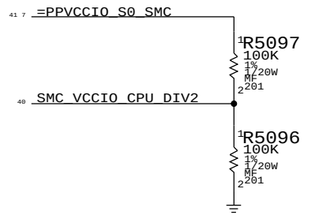
SMC12 PECI Support



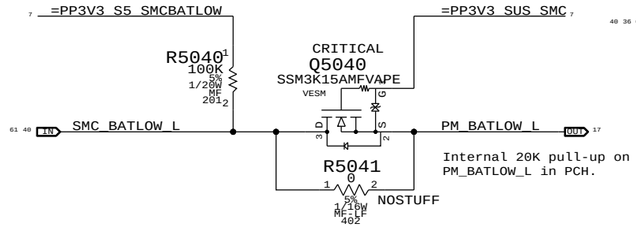
SMC12 Eng Pkg Support

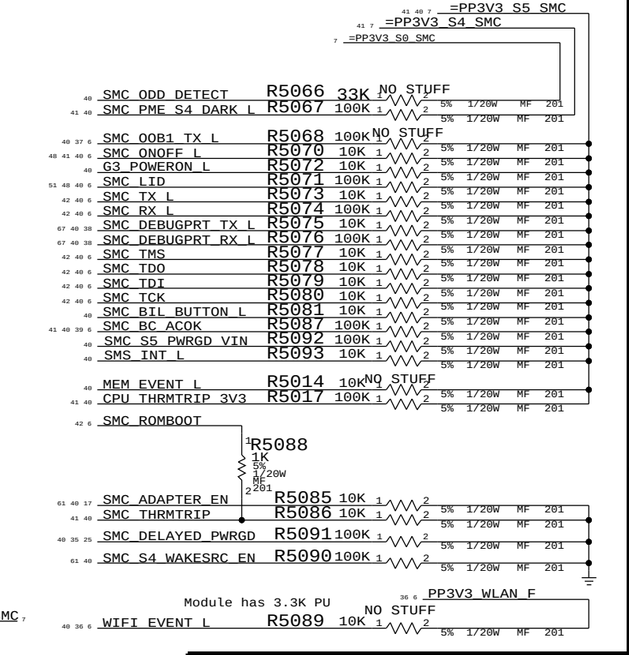
Eng Package requires 1.2V ON SMC_ADC23 pin.





BATLOW# Isolation





SYNC_MASTER=J13_MLB	SYNC_DATE=10/06/2011
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
	REVISION 2.7.0
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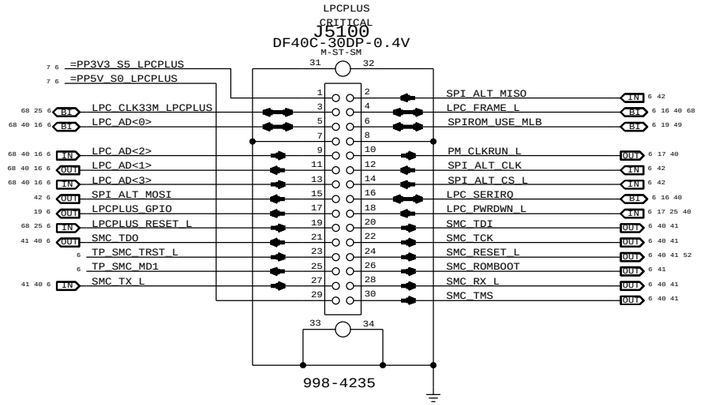
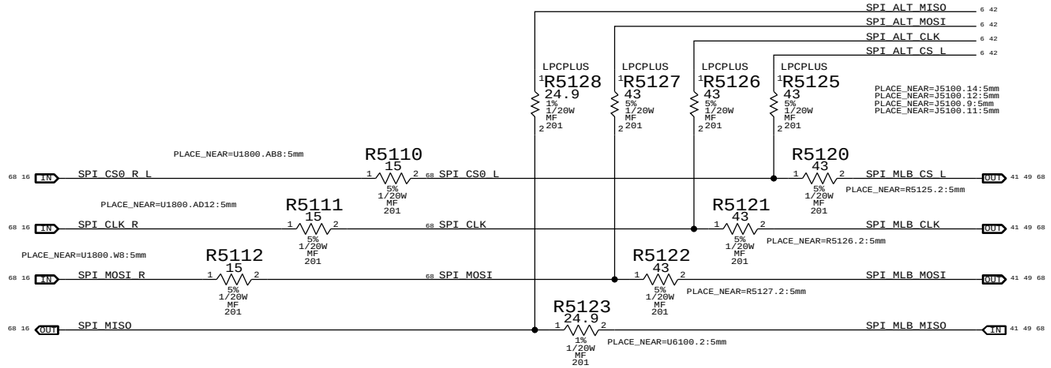
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D
REVISION: 2.7.0
BRANCH:
PAGE: 51 OF 109
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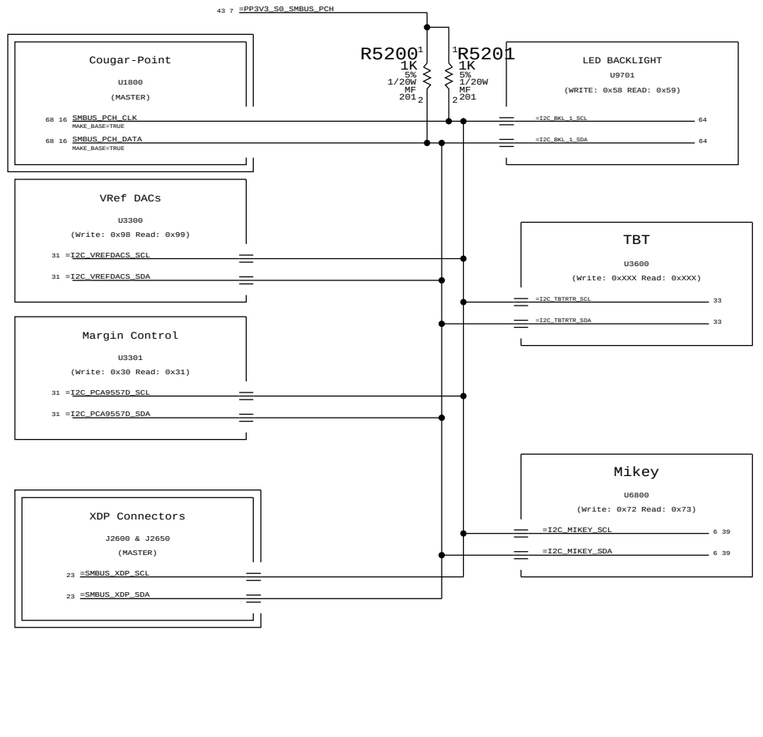
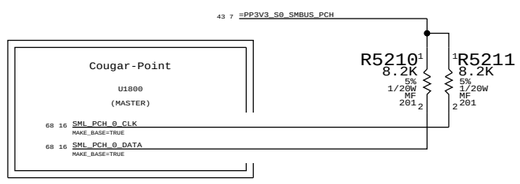
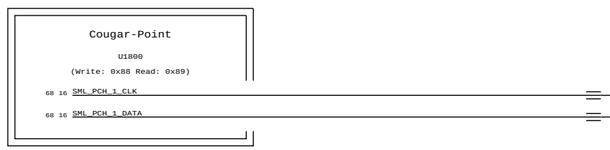
PCH S0 SMBus "0" Connections



PCH S0 "SMLink 0" Connections

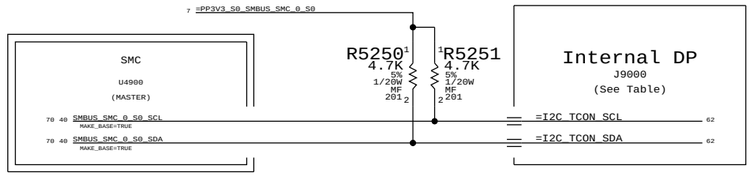


PCH S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

SMC "0" SMBus S0 Connections



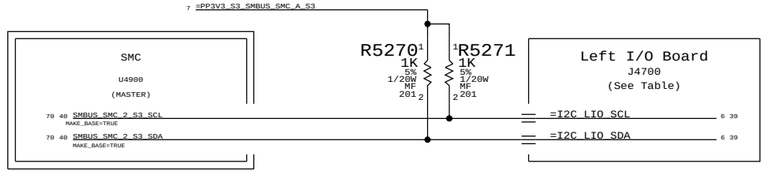
(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

SMC "2" SMBus S3 Connections

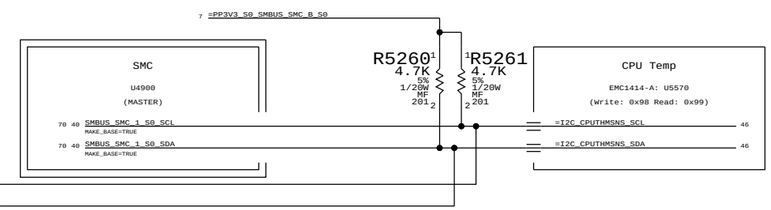
NOTE: SMC RMT bus remains powered and may be active in S3 state



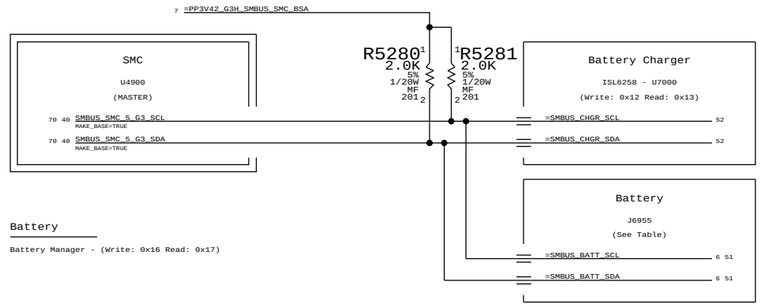
Left I/O Board

ALS - (write: 0x72 Read: 0x73)
Finstack Temp - (Write: 0x92 Read: 0x93)

SMC S0 "1" SMBus Connections



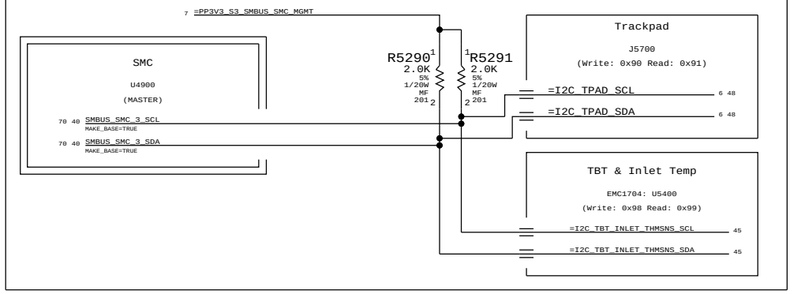
SMC "5" SMBus G3H Connections



Battery

Battery Manager - (Write: 0x16 Read: 0x17)

SMC "3" SMBus S3 Connections



SYNC_MASTER=J13_MLB SYNC_DATE=10/05/2011

PAGE TITLE: SMBus Connections

Apple Inc.

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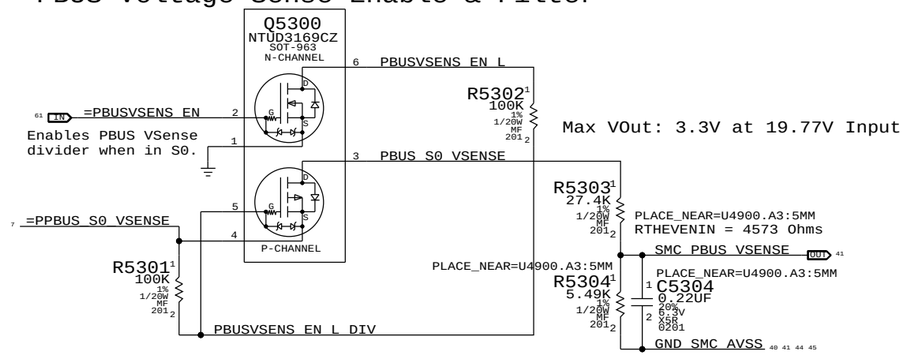
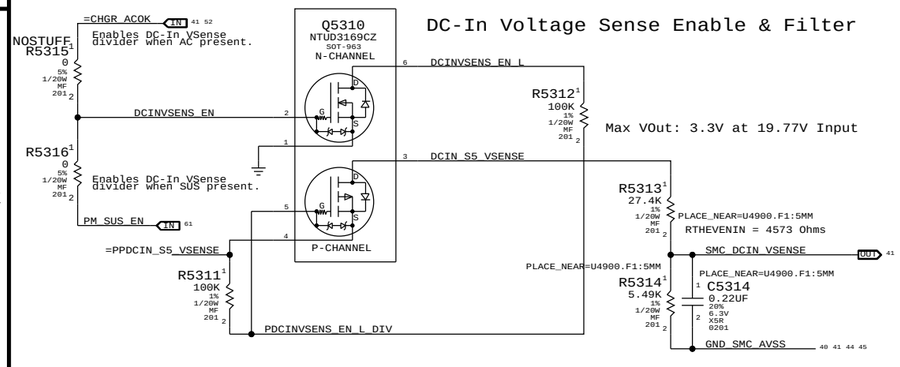
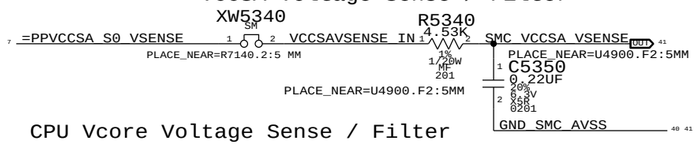
PBUS Voltage Sense Enable & Filter



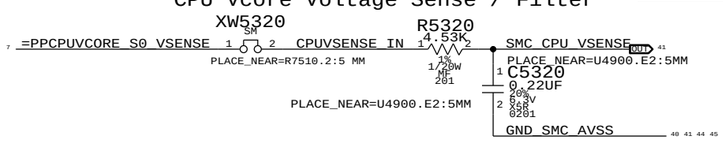
DC-In Voltage Sense Enable & Filter



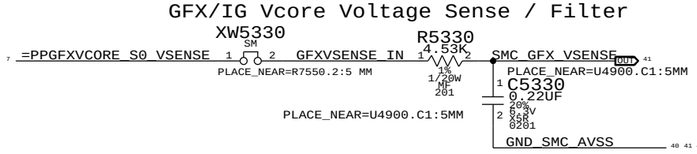
VCCSA Voltage Sense / Filter



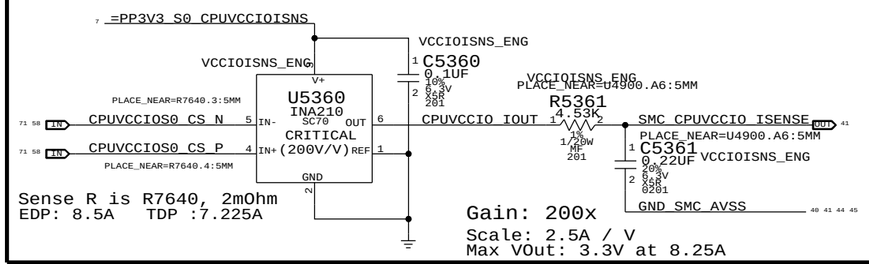
CPU Vcore Voltage Sense / Filter



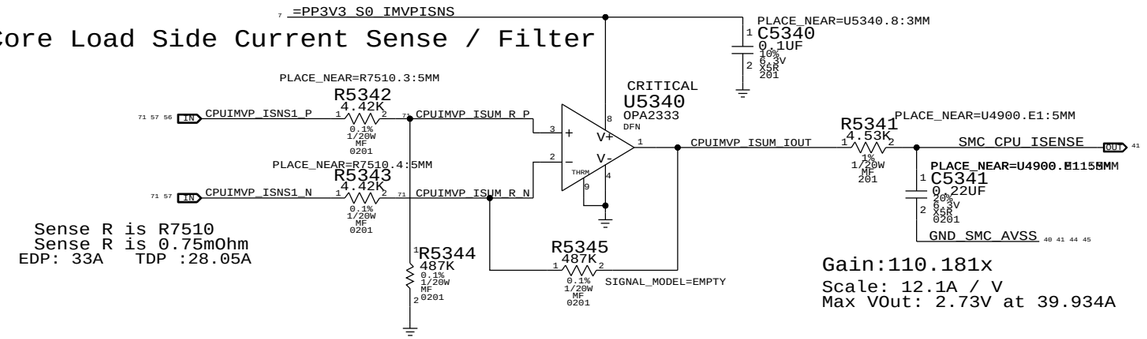
GFX/IG Vcore Voltage Sense / Filter



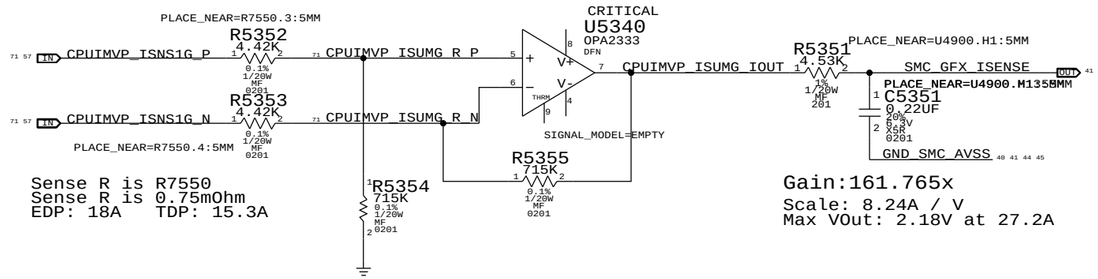
CPU 1.05V VCCIO Current Sense / Filter



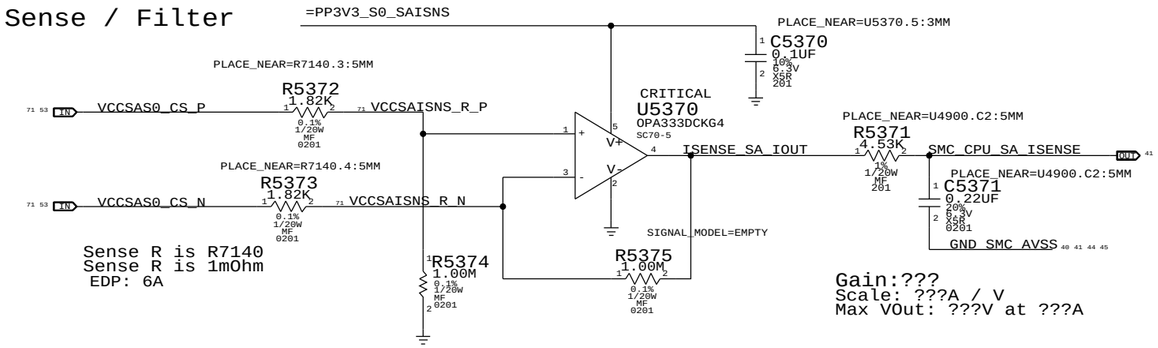
CPU VCore Load Side Current Sense / Filter



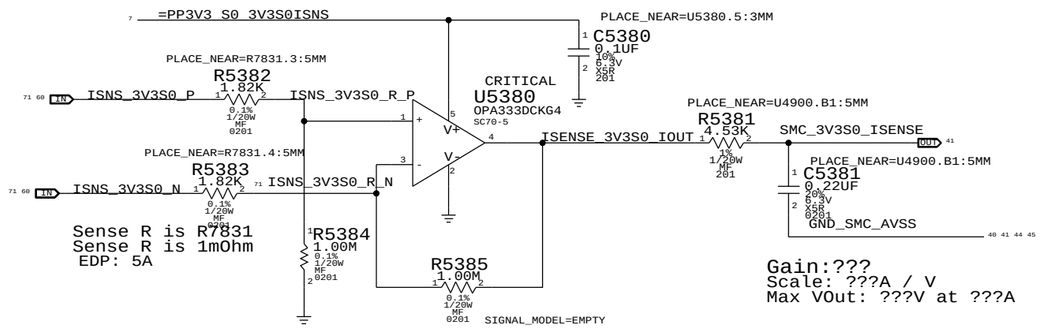
GFX/IG VCore Load Side Current Sense / Filter



CPU SA Current Sense / Filter



3.3V S0 FET Current Sense / Filter



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

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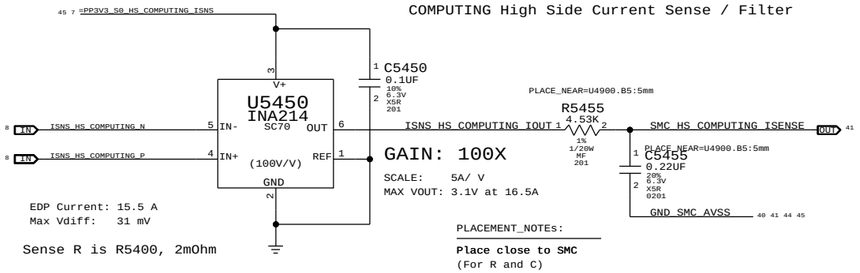
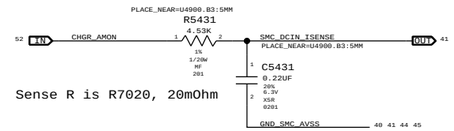
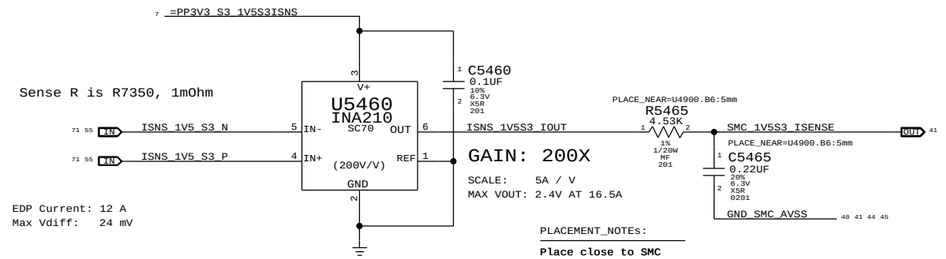
COMPUTING High Side Current Sense / Filter



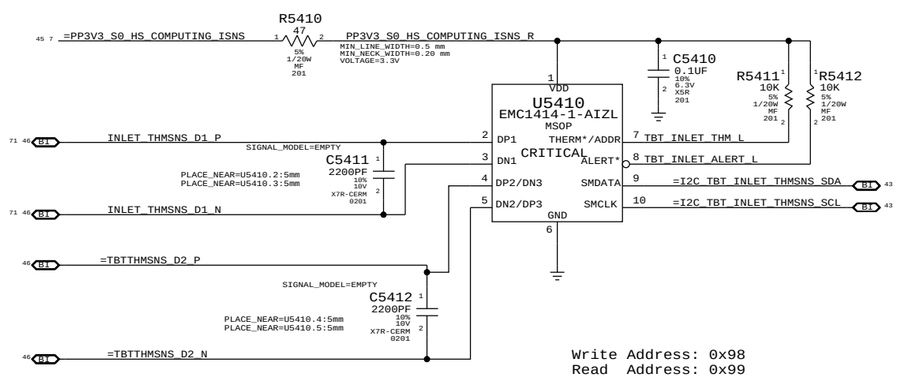
DC-IN (AMON) Current Sense Filter



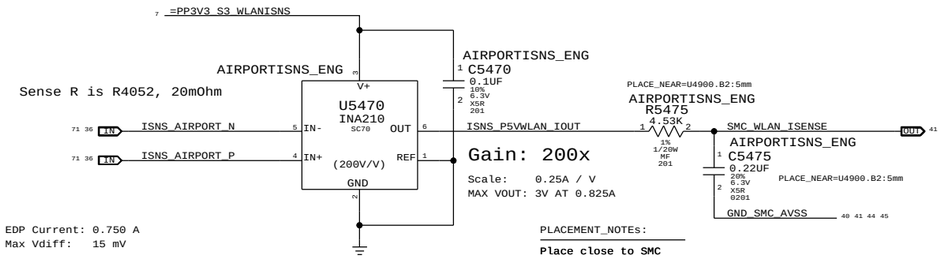
DDR3 1V5R1V35 Current Sense / Filter



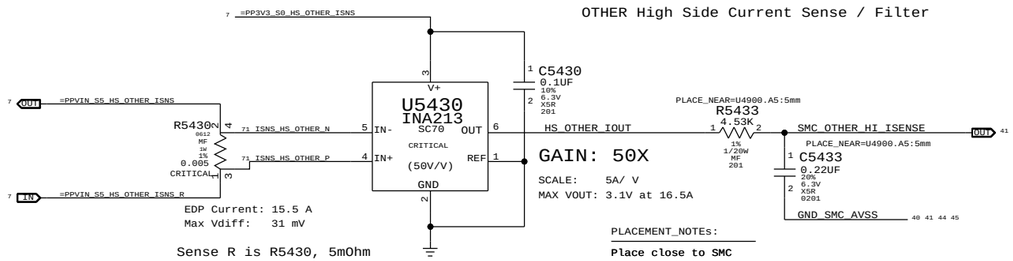
TBT/Inlet Temp Sensor



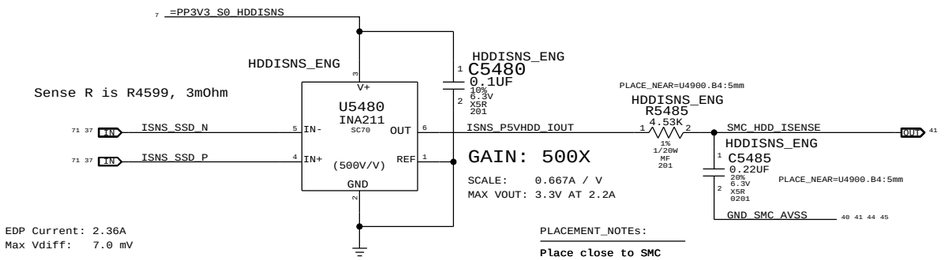
AirPort Current Sense / Filter



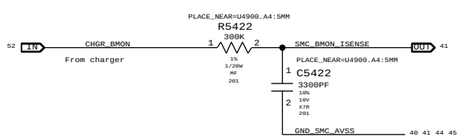
OTHER High Side Current Sense / Filter



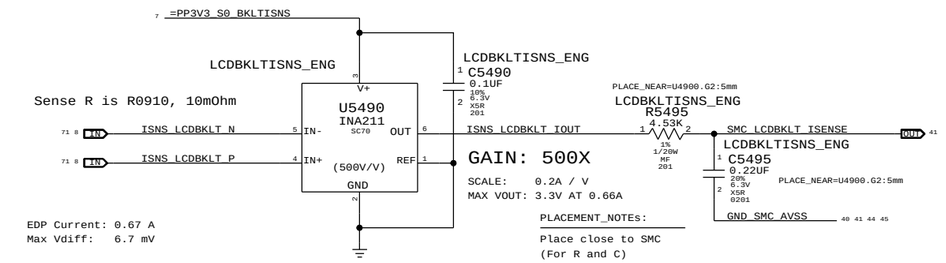
HDD Current Sense / Filter



CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



LCD Backlight Driver Input Current Sense / Filter



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

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Apple Inc.

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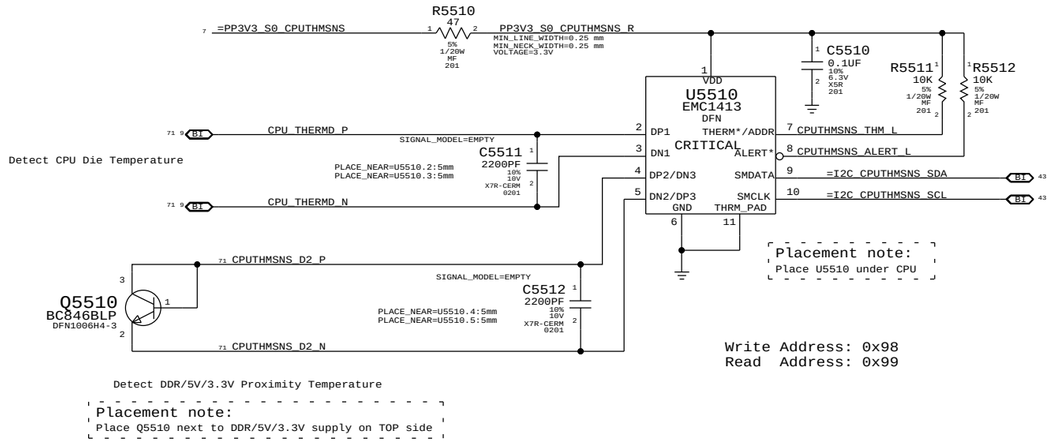
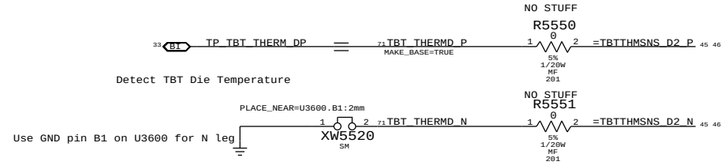
CPU Proximity Sensor



TBT Die

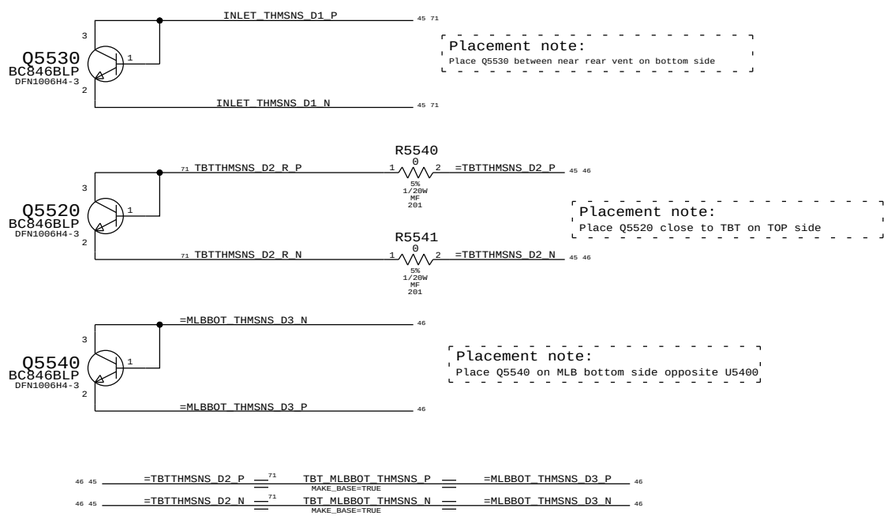


To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors



SYNC_MASTER=J13_MLB SYNC_DATE=08/30/2011

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

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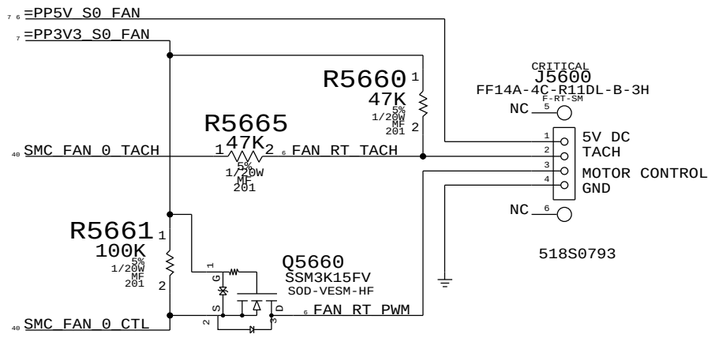
FAN CONNECTOR



SYNC MASTER=K21_MLB	SYNC DATE=12/13/2010
PAGE TITLE: Fan	
Apple Inc.	DRAWING NUMBER: 051-9276 SIZE: D
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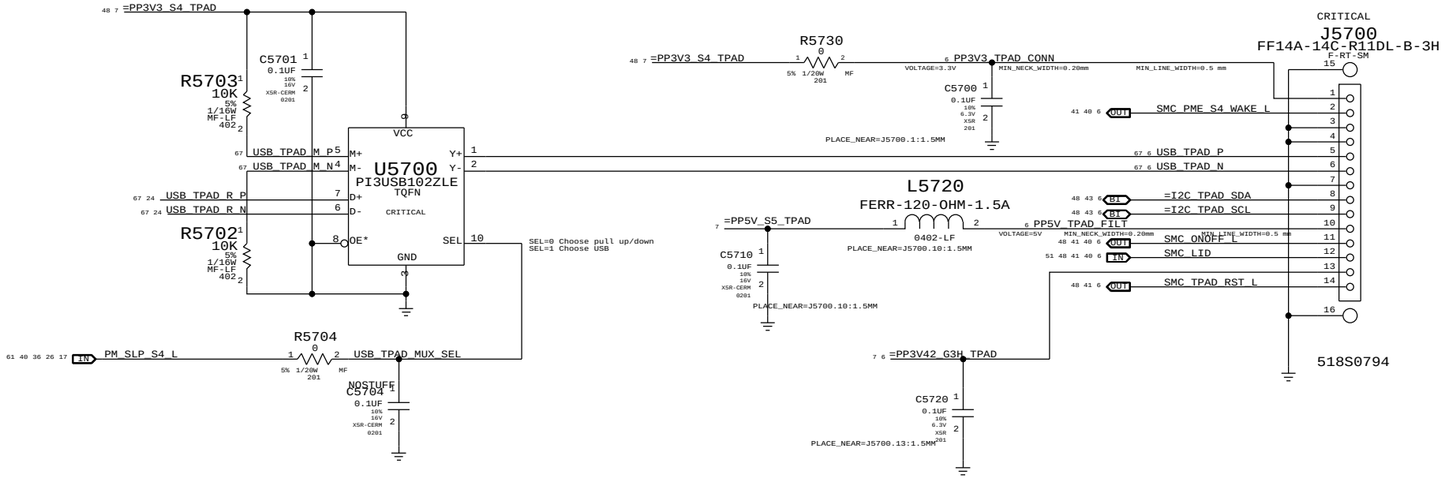
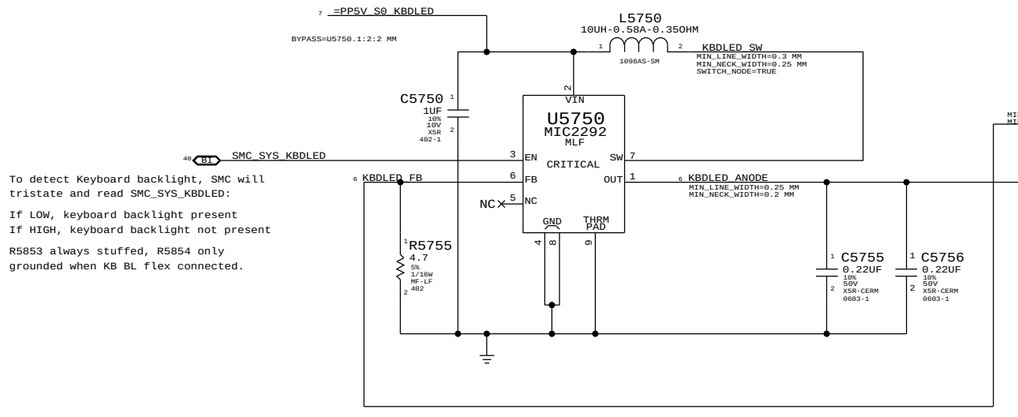
IPD Flex Connector



Keyboard Backlight Driver & Detection

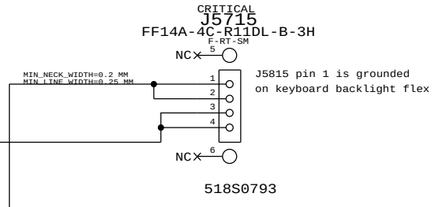


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: IPD / KBD Backlight

Apple Inc.

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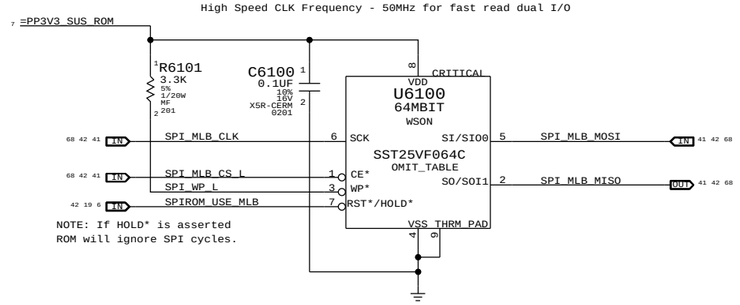
DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011

PAGE TITLE

SPI ROM

Apple Inc.

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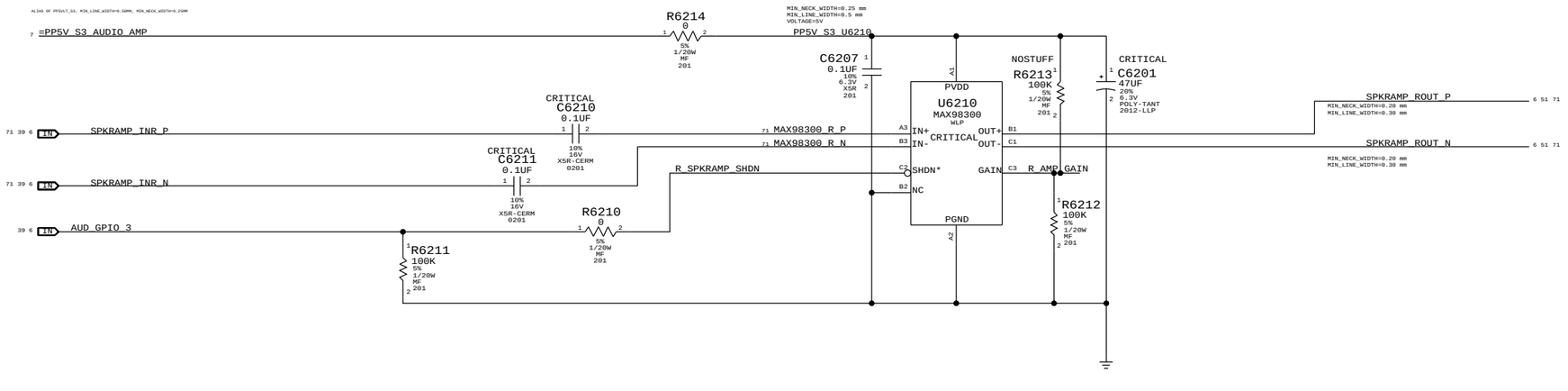
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

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AUDI0: SPEAKER AMP

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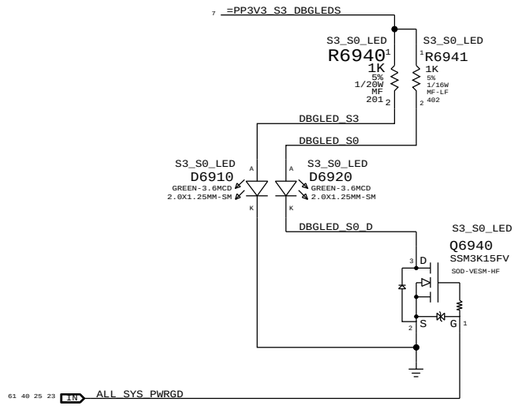
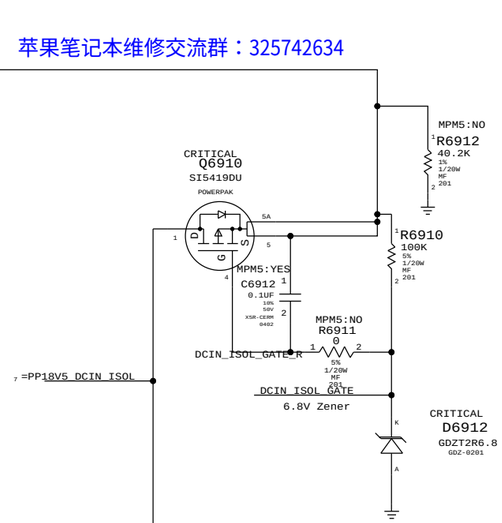
MLB to LIO Power Cable Connector

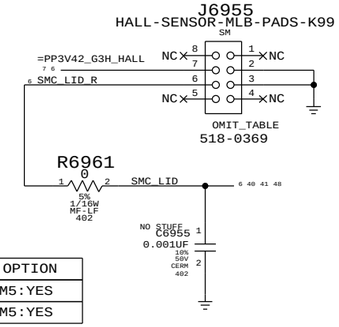
Debug LEDs

(For development only)



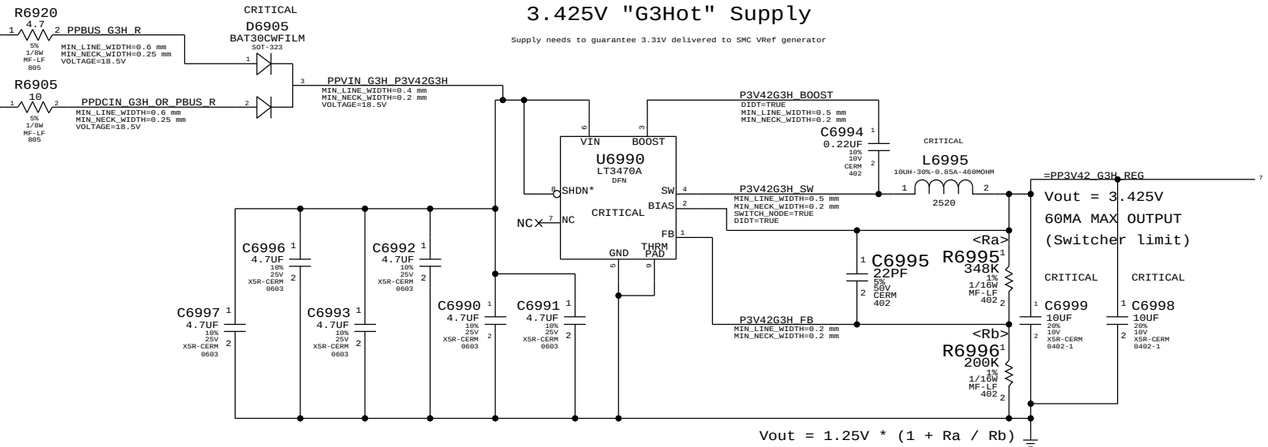


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,90.9KOHM,1,1/20W,0201	R6912	CRITICAL	MPM5:YES
117S0008	1	RES,MF,100KOHM,1,1/20W,0201	R6911	CRITICAL	MPM5:YES

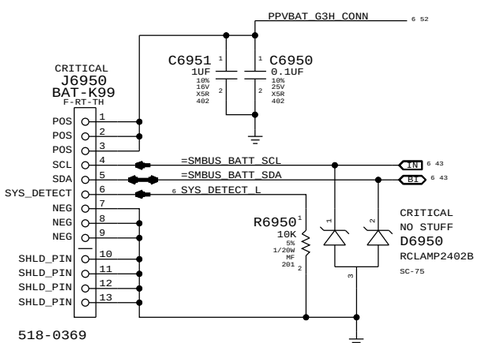


3.425V "G3Hot" Supply

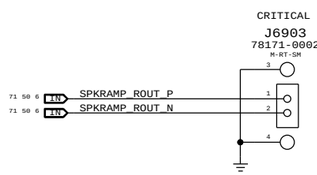
Supply needs to guarantee 3.31V delivered to SMC VRef generator



K99-Specific Battery Connector



Right Speaker Connector



SYNC_MASTER=K21_MLB
SYNC_DATE=11/11/2011

PAGE TITLE: DC-In & Battery Connectors

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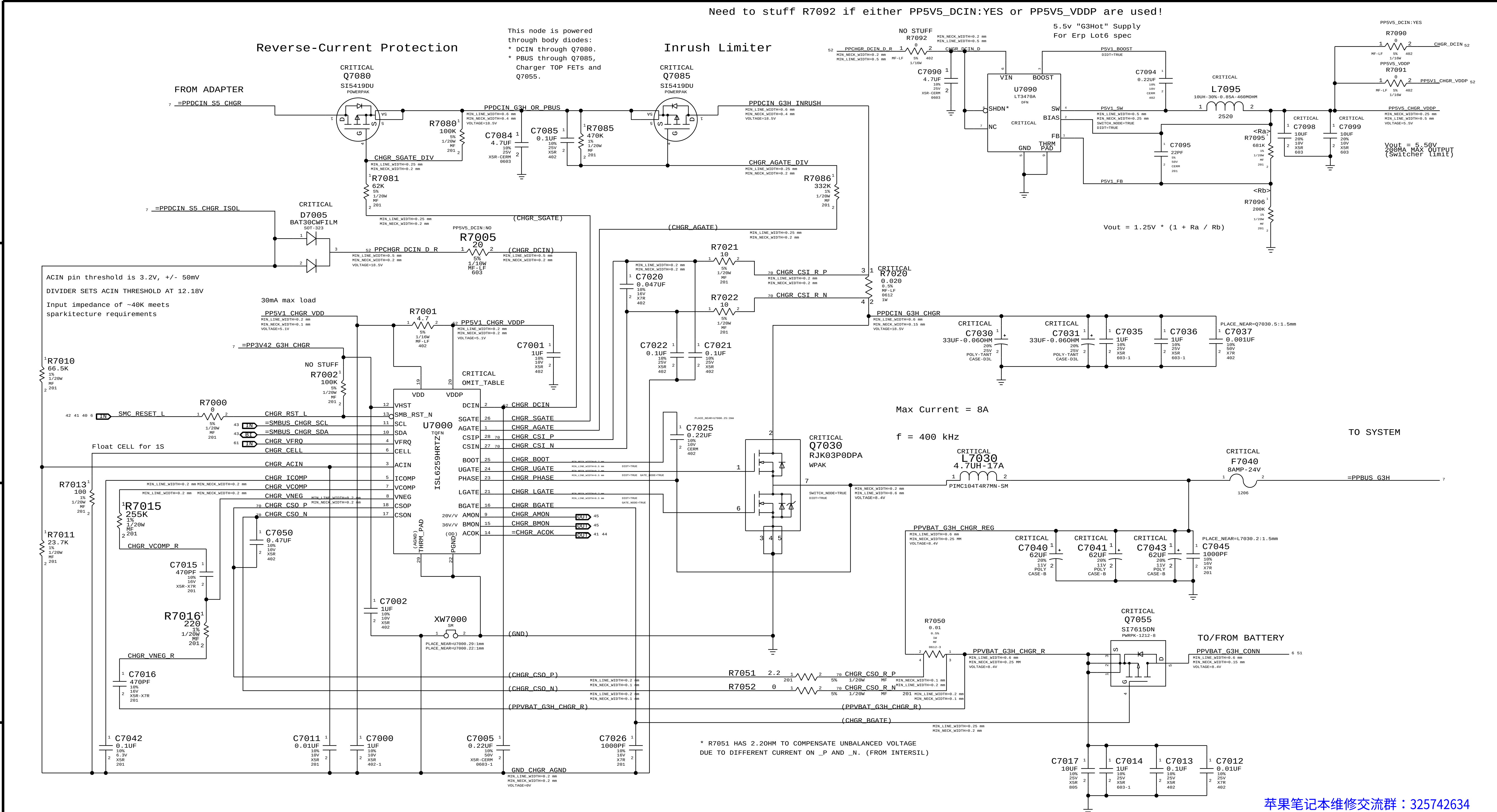


Need to stuff R7092 if either PP5V5_DCIN:YES or PP5V5_VDDP are used!
Reverse-Current Protection
This node is powered through body diodes:
* DCIN through Q7080.
* PBUS through Q7085, Charger TOP FETs and Q7055.
Inrush Limiter
5.5v "G3Hot" Supply
For Erp Lot6 spec
FROM ADAPTER
=PPDCIN_S5_CHGR
CRITICAL
Q7080
SI5419DU
PPDCIN_G3H_OR_PBUS
R7080
C7084
C7085
R7085
Q7085
PPDCIN_G3H_INRUSH
CHGR_SGATE_DIV
CHGR_AGATE_DIV
R7081
R7086
=PPDCIN_S5_CHGR_ISOL
D7005
BAT30CWFILM
PPCHGR_DCIN_D_R
R7005
(CHGR_SGATE)
(CHGR_AGATE)
(CHGR_DCIN)
NO STUFF
R7092
CHGR_DCIN_D
C7090
U7090
LT3470A
VIN
BOOST
SHDN*
SW
BIAS
FB
GND
THRM PAD
NC
C7094
L7095
10UH-30%-0.85A-460MOHM
C7095
R7095
R7096
C7098
C7099
PP5V1_BOOST
PP5V1_SW
PP5V1_FB
PP5V5_CHGR_VDDP
R7090
R7091
CHGR_DCIN
PP5V1_CHGR_VDDP
Vout = 5.50V
200MA MAX OUTPUT
(Switcher limit)
Vout = 1.25V * (1 + Ra / Rb)
ACIN pin threshold is 3.2V, +/- 50mV
DIVIDER SETS ACIN THRESHOLD AT 12.18V
Input impedance of ~40K meets sparkitecture requirements
30mA max load
PP5V1_CHGR_VDD
R7001
PP5V1_CHGR_VDDP
C7001
=PP3V42_G3H_CHGR
R7010
R7002
CRITICAL
OMIT_TABLE
U7000
ISL6259HRTZ
R7000
SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
Float CELL for 1S
R7013
R7015
R7011
C7050
C7015
CHGR_VCOMP_R
R7016
CHGR_VNEG_R
C7016
C7002
XW7000
(GND)
CHGR_DCIN
CHGR_SGATE
CHGR_AGATE
CHGR_CSI_P
CHGR_CSI_N
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_BGATE
CHGR_AMON
CHGR_BMON
=CHGR_ACOK
R7021
R7022
C7020
C7022
C7021
R7020
PPDCIN_G3H_CHGR
C7030
C7031
C7035
C7036
C7037
C7025
Q7030
RJK03P0DPA
Max Current = 8A
f = 400 kHz
L7030
4.7UH-17A
TO SYSTEM
F7040
8AMP-24V
=PPBUS_G3H
PPVBAT_G3H_CHGR_REG
C7040
C7041
C7043
C7045
R7050
Q7055
SI7615DN
TO/FROM BATTERY
PPVBAT_G3H_CHGR_R
PPVBAT_G3H_CONN
R7051
R7052
CHGR_CSO_R_P
CHGR_CSO_R_N
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE
DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)
C7042
C7011
C7000
C7005
C7026
GND_CHGR_AGND
C7017
C7014
C7013
C7012

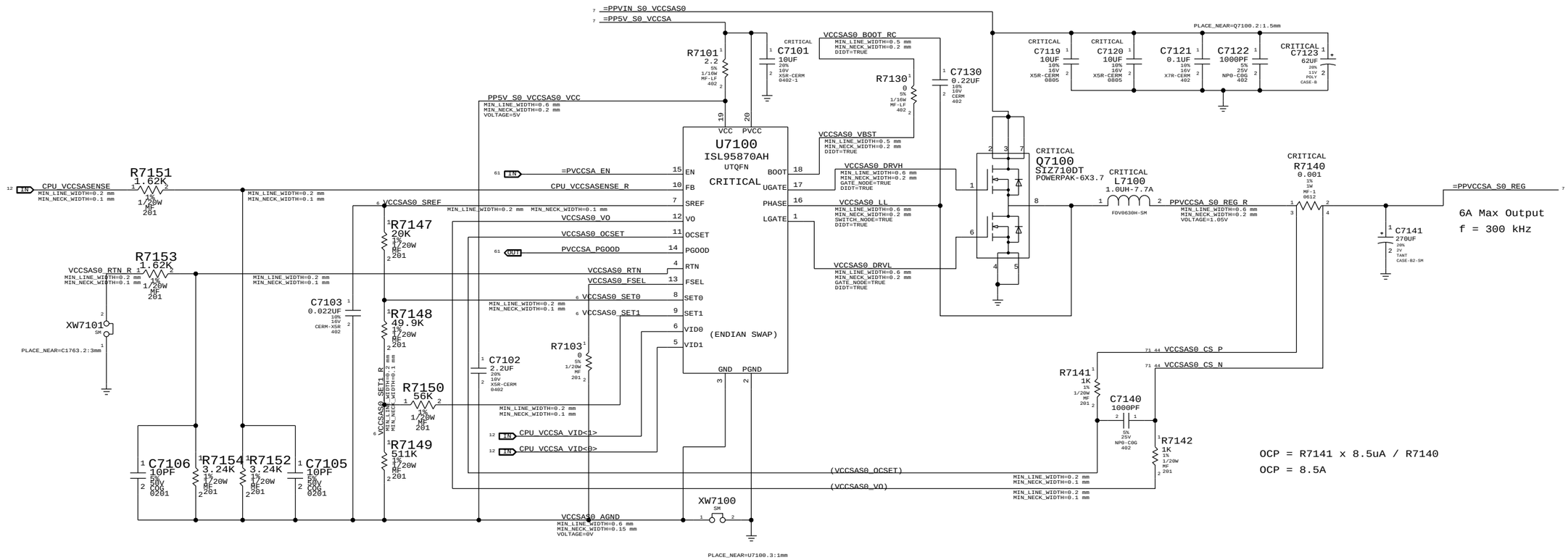
SYNC_MASTER=J13_MLB SYNC_DATE=10/10/2011

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC MASTER=J13_MLB SYNC DATE=09/01/2013

PAGE TITLE

System Agent Supply

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

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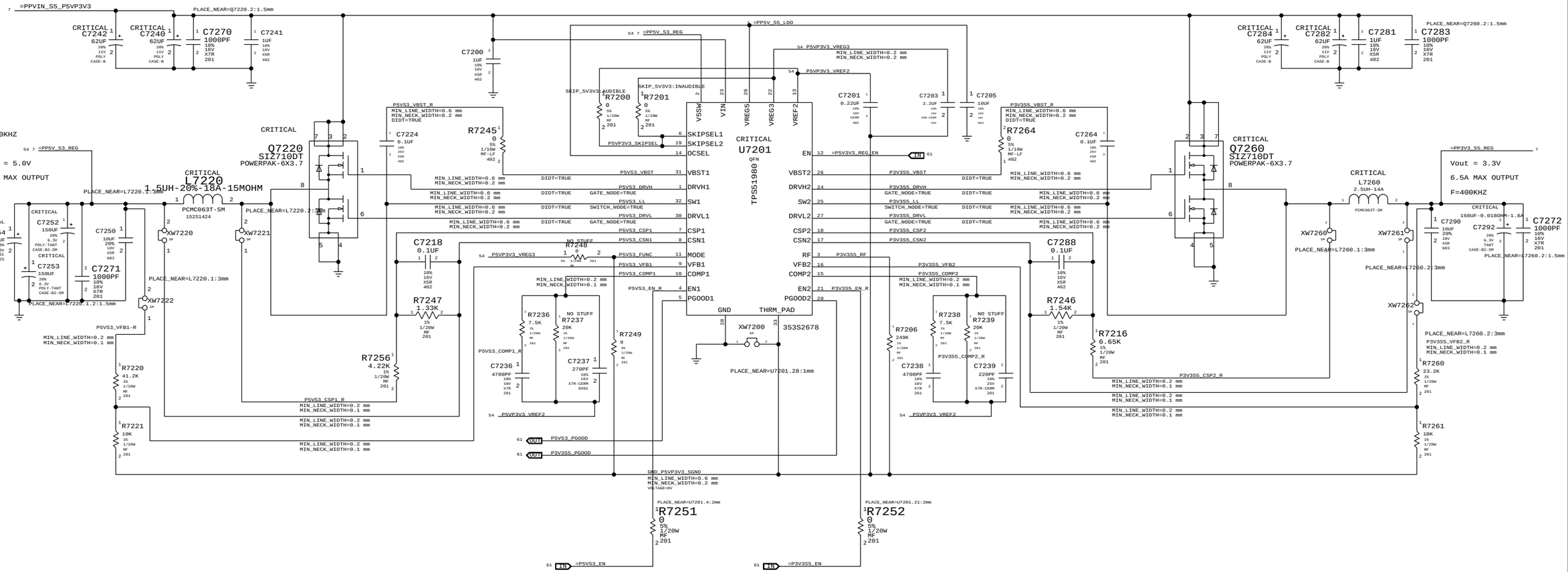
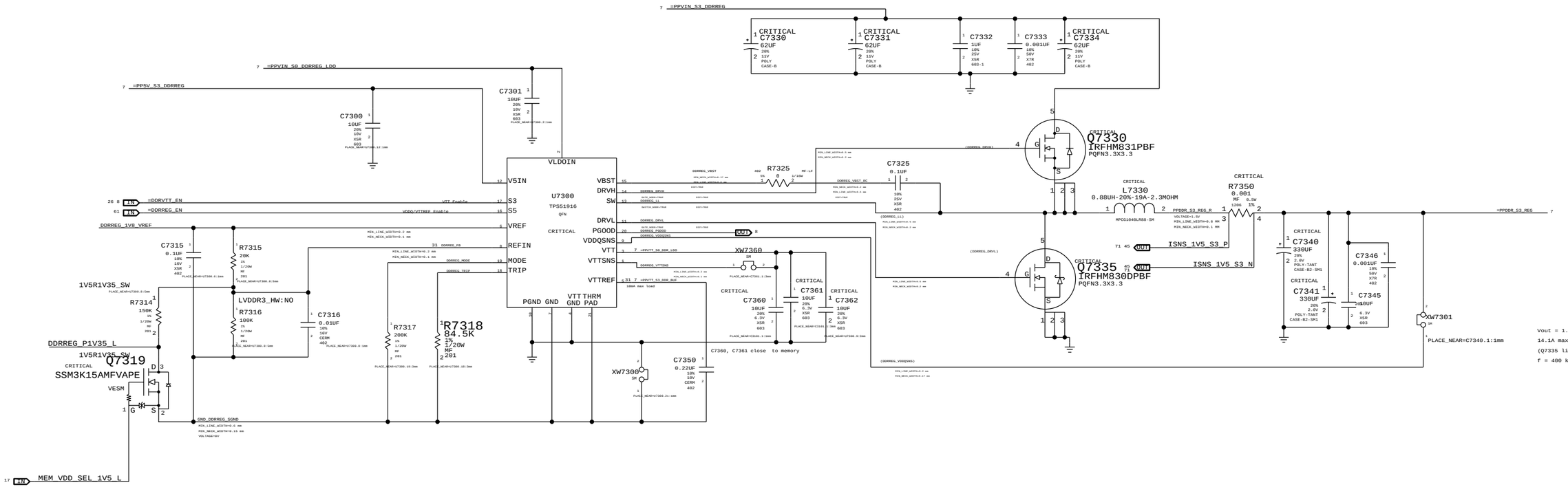


SYNC_MASTER=J13_MLB	SYNC_DATE=11/10/2011
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
	PAGE 72 OF 109
	SHEET 54 OF 72



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

SYNC_MASTER=J13_MLB SYNC_DATE=10/07/2013

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

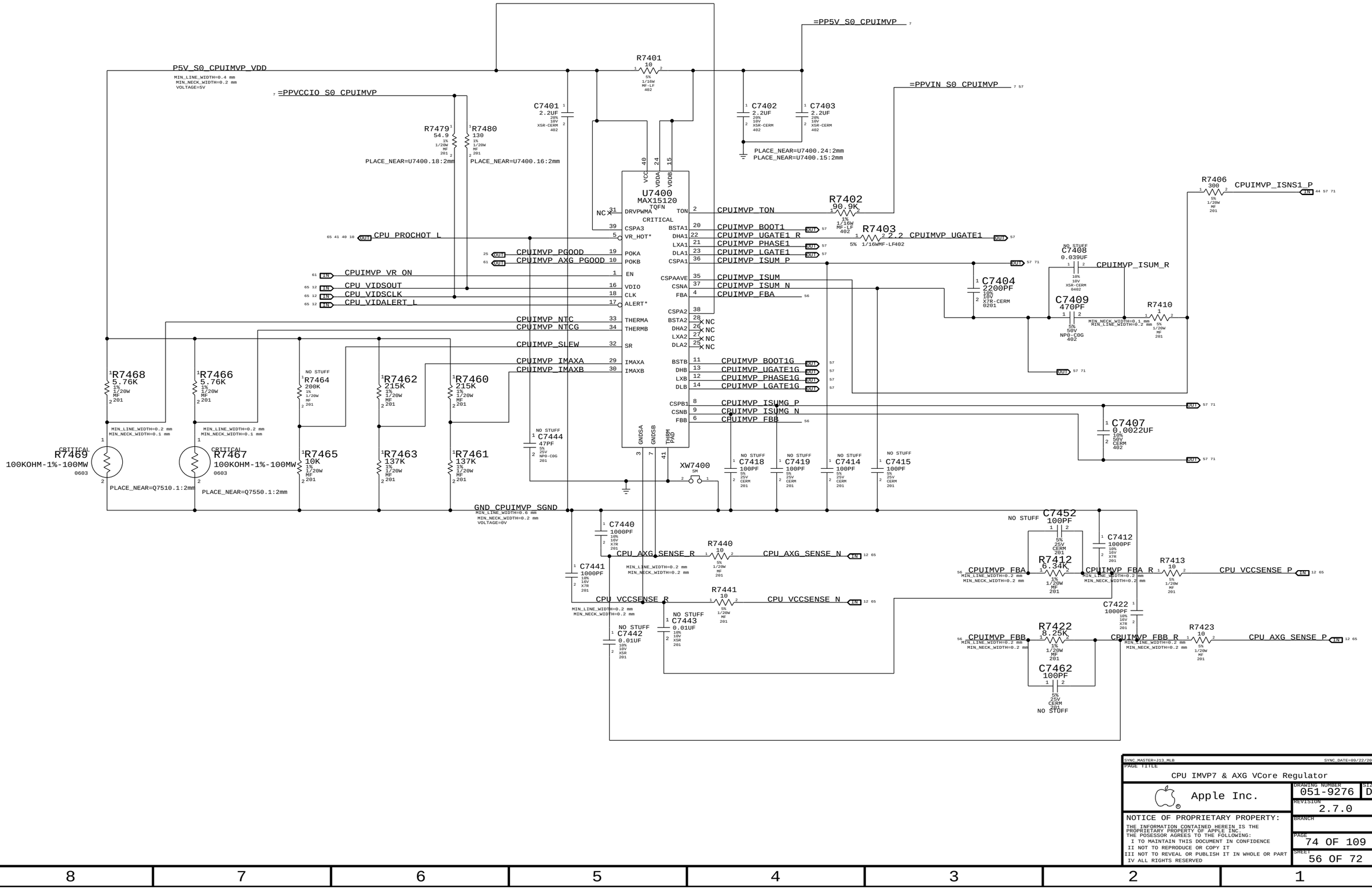
DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

BRANCH

PAGE 73 OF 109

SHEET 55 OF 72



SYNC_MASTER=J13_MLB SYNC_DATE=09/22/2011

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9276 SIZE D

REVISION 2.7.0

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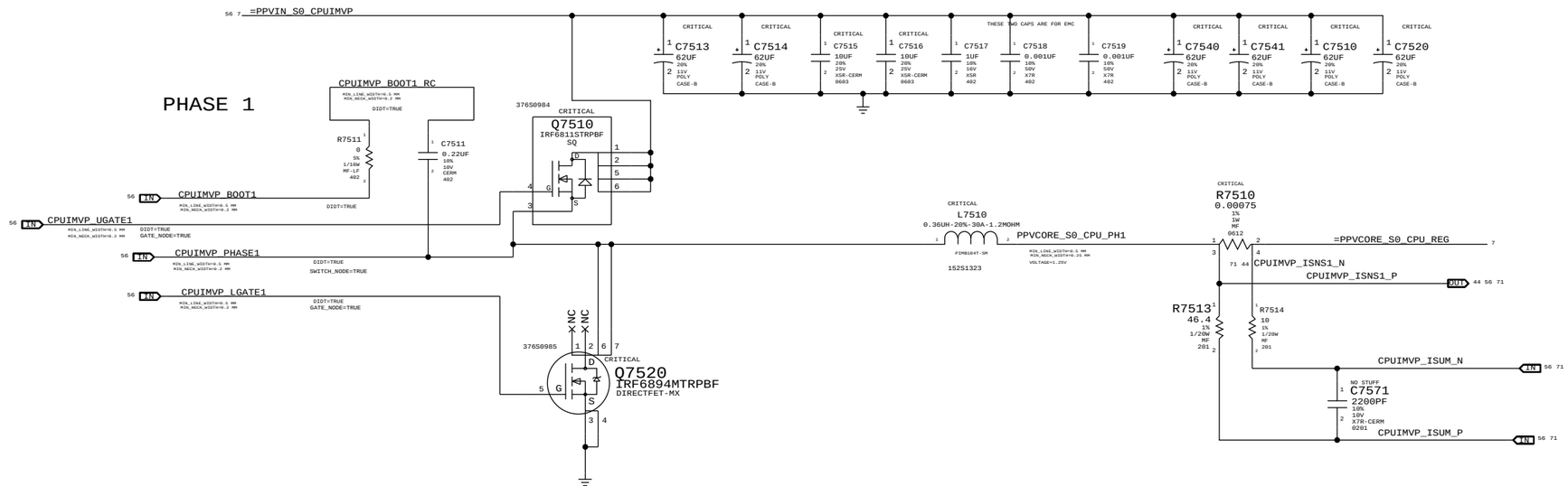
CPU=IV Bridge ULV, AXG=GT2



SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE	CPU IMVP7 & AXG VCore Output
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
	REVISION 2.7.0
	BRANCH
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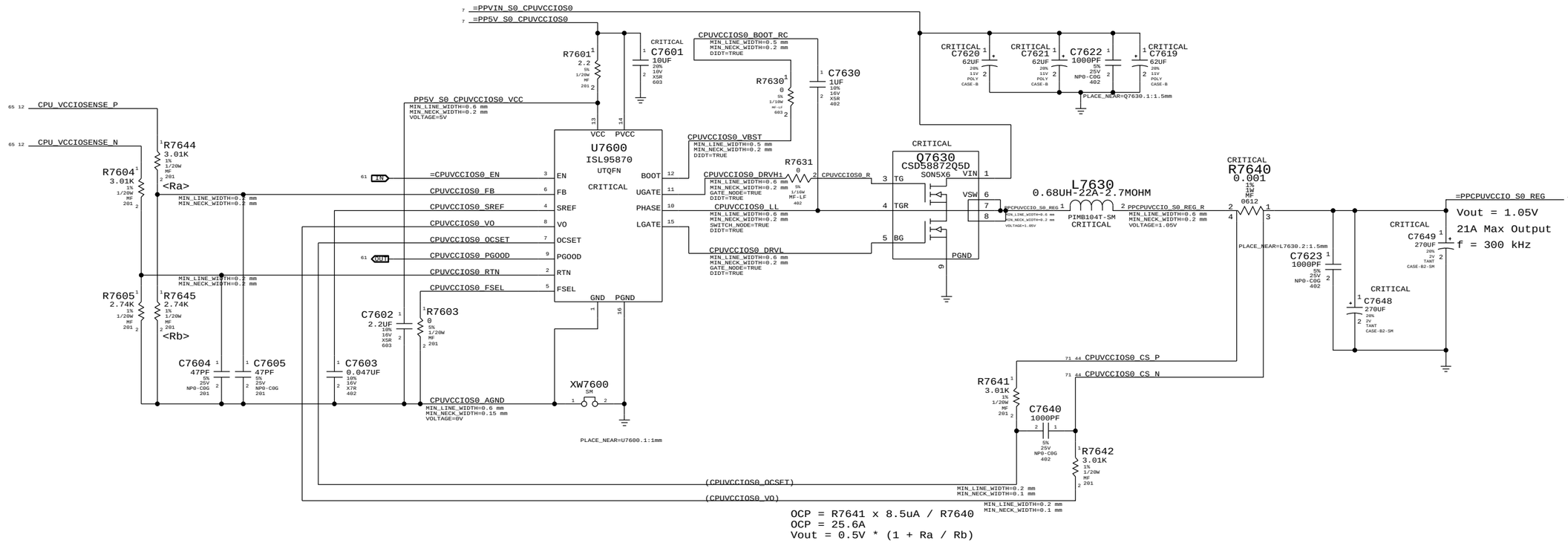
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=J13_MLB	SYNC_DATE=09/01/2011
PAGE TITLE	CPU VCCIO (1.05V) Power Supply
Apple Inc.	DRAWING NUMBER 051-9276 · SIZE D
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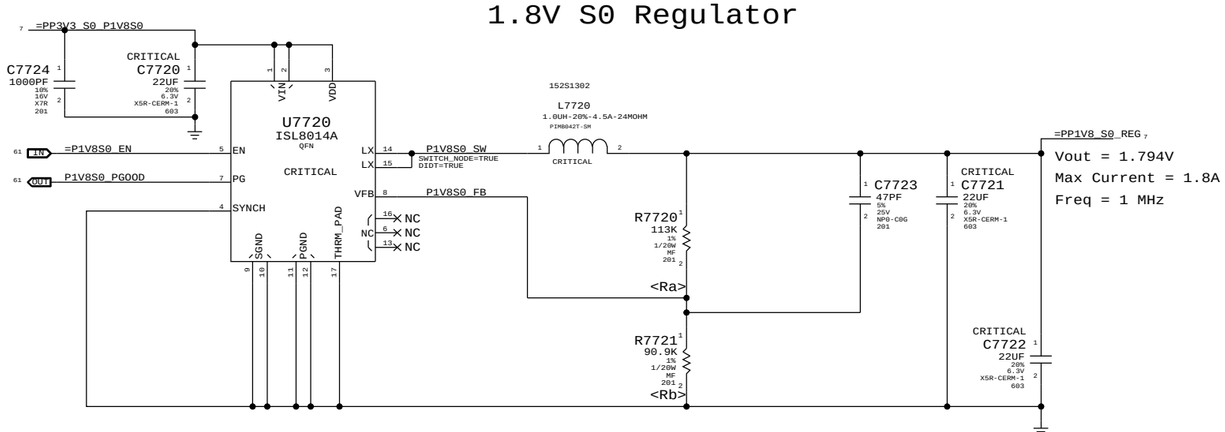
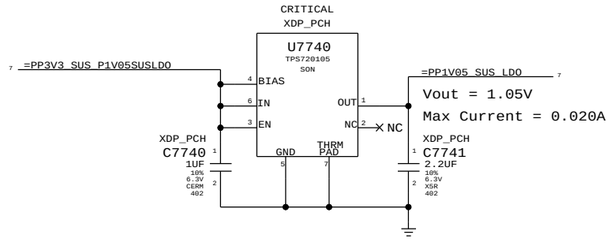
1.8V S0 Regulator

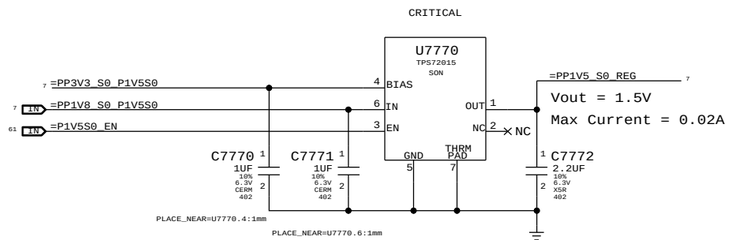


1.05V SUS LDO

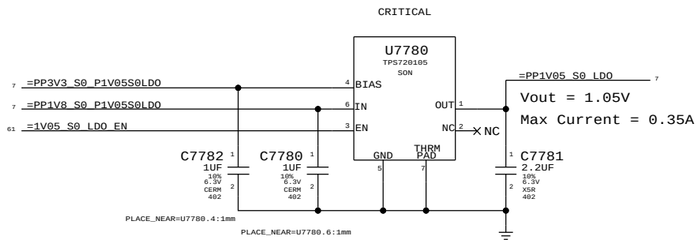
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D
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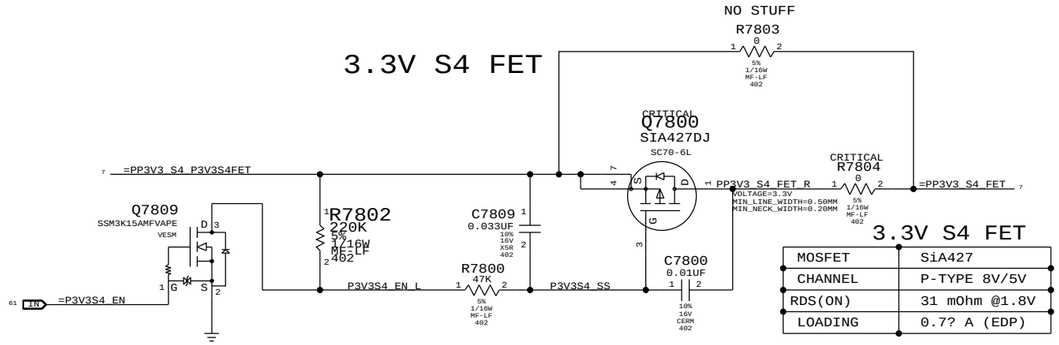
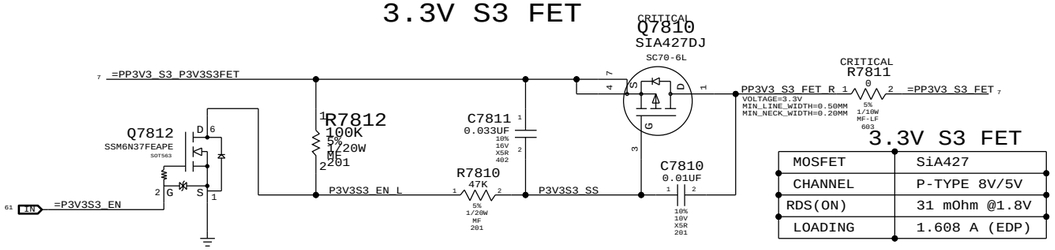
3.3V S4 FET



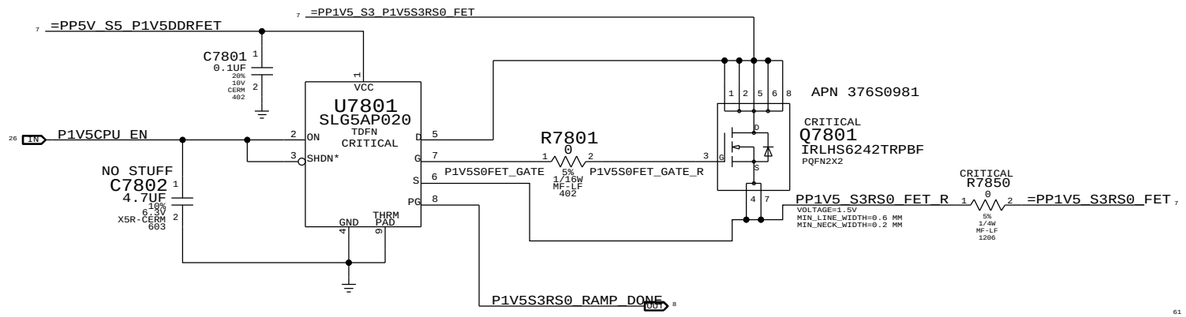
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET



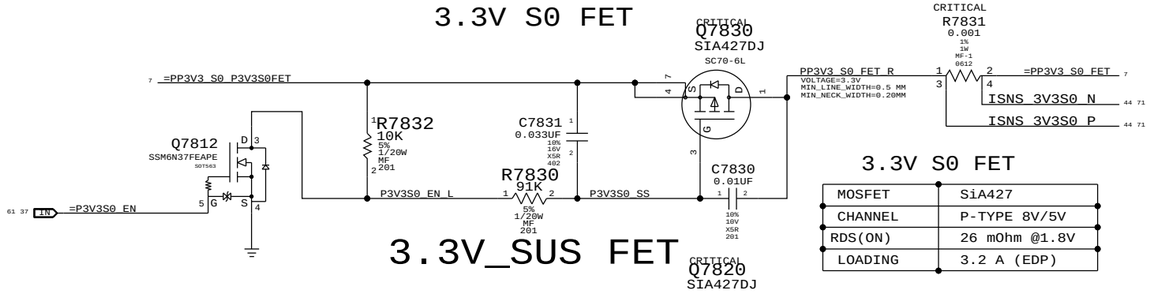
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET



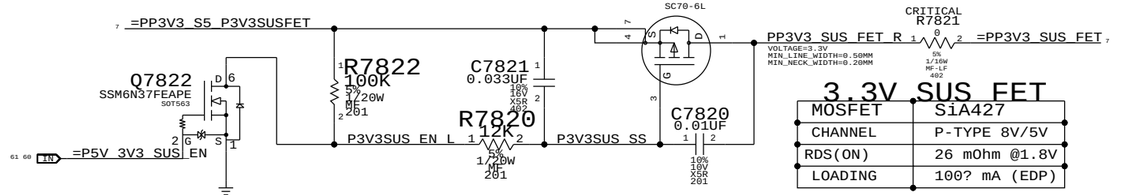
1.5V S3/S0 FET	
MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET



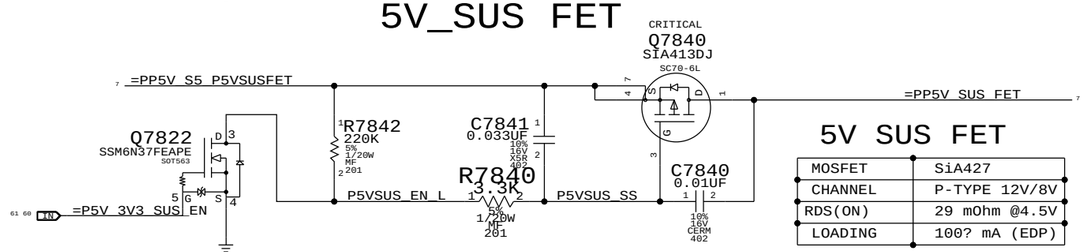
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



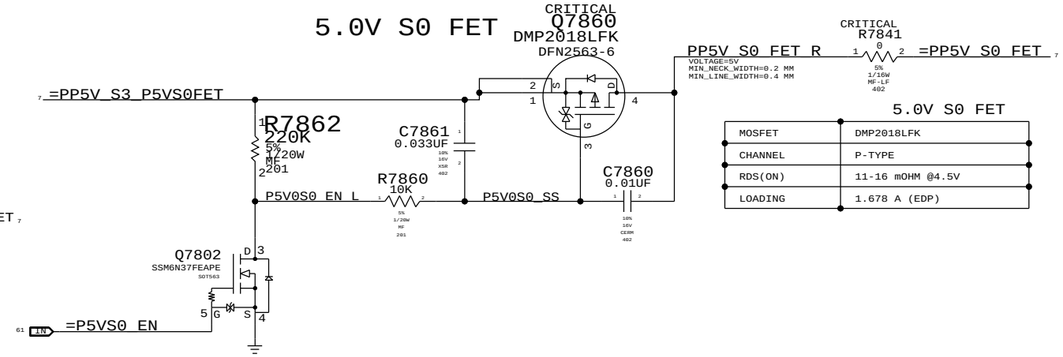
3.3V_SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	DMP2018LFK
CHANNEL	P-TYPE
RDS(ON)	11-16 mOHM @4.5V
LOADING	1.678 A (EDP)

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

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BRANCH:

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S5 Rail Enables & PGOOD

Internal pull-ups 100K +/- 20%

=PP3V42_G3H_PWRCTL

C7940 0.1UF 10% 6.3V X5R 201

U7941 SLG4AP012 TDFN — CRITICAL 343S0497

SMC_PM_G2_EN — MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL

Threshold: ??
DLY > 10 ms
S5PGOOD_DLY

C7941 220PF 10% 25V X7R-CERM 201

R7941 100 5% 1/20W MF 201

C7942 0.033UF 10% 16V X5R 402 — NO STUFF

P3V3S5_EN — MAKE_BASE=TRUE — =P3V3S5_EN

P5V3V3_REG_EN — MAKE_BASE=TRUE — =P5V3V3_REG_EN

S5_PWRGD — MAKE_BASE=TRUE

S5_PWRGD (old name RSMRST_PWRGD)-->SMC
SMC-->PM_DSW_PWRGD

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

3.3V,5V S3 ENABLE

PM_SLP_S4_L — MAKE_BASE=TRUE

R7913 0 5% 1/20W MF 201 — P5VS3_EN — MAKE_BASE=TRUE — =P5VS3_EN

NO STUFF C7913 0.068UF 10% 16V CERM 402

PLACE_NEAR=U7300.16:6mm
R7911 5.1K 5% 1/20W MF 201
R7912 9.1K 5% 1/20W MF 201
PLACE_NEAR=Q7812.2:6mm

P3V3S3_EN — MAKE_BASE=TRUE — =P3V3S3_EN
DDRREG_EN — MAKE_BASE=TRUE — =DDRREG_EN
=USB_PWR_EN

PLACE_NEAR=U7300.16:6mm C7910 0.47UF 10% 6.3V CERM-X5R 402
PLACE_NEAR=Q7812.2:6mm C7912 0.47UF 10% 6.3V CERM-X5R 402

DP S4 Power Enable

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.1:2.3mm

C7970 0.1uF 10% 16V CERM 402

PM_SLP_S5_L:100K pull down on PCH page

U7970 74LVC1G32 SOT891

PM_SLP_S5_L — P5V3V3_S4_EN — MAKE_BASE=TRUE — =TBTAPWRSW_EN — =P3V3S4_EN

SMC_S4_WAKESRC_EN — MAKE_BASE=TRUE

NOSTUFF R7915 0 5% 1/16W MF-LF 402

NC

CPUVCORE ENABLE

R7974 0 5% 1/20W MF 201 — PLACE_NEAR=U7400.1:5mm

ALL_SYS_PWRGD — CPUIMVP_VR_ON

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.5:2.3mm

C7943 0.1UF 10% 6.3V X5R 201

SMC_BATLOW_L:100K pull up on SMC page

U7940 74AUP1G3208 SOT891

SMC_BATLOW_L — PM_SUS_EN — MAKE_BASE=TRUE — =P5V_3V3_SUS_EN

PM_SLP_SUS_L

NO STUFF R7917 0 5% 1/20W MF 201

S0 ENABLE

PM_SLP_S3_L — R7978 100 5% 1/20W MF 201 — PM_SLP_S3_R_L — MAKE_BASE=TRUE

(PM_SLP_S3_R_L)

=PP3V42_G3H_PWRCTL

R7931 10K 5% 1/20W MF 201 — CHGR_VFRQ

Q7931 SSM3K15FV SOD-VESM-HF

R7987 33K 5% 1/20W MF 201 — PLACE_NEAR=U7100.15:6mm
R7981 20K 5% 1/20W MF 201 — PLACE_NEAR=U7600.3:6mm
R7988 39K 5% 1/20W MF 201 — PLACE_NEAR=U7770.3:6mm
R7986 5.1K 5% 1/20W MF 201 — PLACE_NEAR=U7720.5:6mm

=P5VS0_EN
=P3V3S0_EN
=PBUSVSENS_EN
=TBT_S0_EN

P1V8S0_EN — MAKE_BASE=TRUE — =P1V8S0_EN

P1V5S0_EN — MAKE_BASE=TRUE — =P1V5S0_EN

=1V05_S0_LDO_EN

CPUVCCIOS0_EN — MAKE_BASE=TRUE — =CPUVCCIOS0_EN

PVCCSA_EN — MAKE_BASE=TRUE — =PVCCSA_EN

C7987 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7100.15:6mm
C7981 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7600.3:6mm
C7988 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7770.3:6mm
C7986 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7720.5:6mm

CHGR VFRQ Generation

VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S5_VMON

R7956 150K 1% 1/20W MF 201 — S0PGD_C

R7951 15K 1% 1/20W MF 201
R7952 7.15K 1% 1/20W MF 201
VMON_3V3_DIV

R7953 1K 5% 1/20W MF 201 — VMON_Q2_BASE
R7954 1K 5% 1/20W MF 201 — VMON_Q3_BASE
R7955 1K 5% 1/20W MF 201 — =PP1V05_S0_VMON — VMON_Q4_BASE

=PP1V5_S3RS0_VMON — PP1V5_S3RS0

Q7950 ASMCC0179 DFN2015H4-8 — Q1 Q2 Q3 Q4 — NC NC CRITICAL

353S2809 S0PGD_BJT_GND_R

Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

R7957 100 5% 1/20W MF 201

3.3V SUS Detect

NO STUFF R7930 0 5% 1/20W MF 201

Could stuff R7930 to satisfy PCH power down timing tz35

No stuff C7931, 12ms Min delay time

U7930 Sense input threhold is 3.07V

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7930.6:2.3mm

C7930 0.1UF 10% 6.3V X5R 201

R7933 100K 5% 1/20W MF 201 — =PP3V3_SUS_PWRCTL

U7930 TPS3808G33DBVRG4 SOT23-6 (90K IP9)

SENSE RESET* CT MR* GND

=PP3V3_SUS_PWRCTL — PM_RSMRST_L — PM_RSMRST_L goes to U1800.C21

S4_PGOOD_CT

C7931 1000PF 10% 16V X7R 201 — NO STUFF

SUS_PGOOD_MR_L

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

=PP5V_S0_VMON — =PP1V5_S3RS0_VMON — =PP1V05_S0_VMON

R7960 6.04K 1% 1/20W MF 201 — S0PGOOD_ISL
R7970 10K 1% 1/20W MF 201 — S0PGOOD_ISL
R7972 6.04K 1% 1/20W MF 201 — S0PGOOD_ISL
C7960 0.1UF 10% 6.3V X5R 201

P5V_DIV_VMON
R7961 15K 1% 1/20W MF 201 — S0PGOOD_ISL
R7971 12.4K 1% 1/20W MF 201 — S0PGOOD_ISL
P1V5_DIV_VMON
R7973 15K 1% 1/20W MF 201 — S0PGOOD_ISL
P1V05_DIV_VMON

U7960 ISL88042IRTEZ TDFN (IPU) — VDD V2MON V3MON V4MON CRITICAL MR* RST* GND THRM_PAD — NC — ALL_SYS_PWRGD_R

353S2310

=PP3V3_S0_VMON

P1V5S0_PGOOD from U7710

R7967 10K 5% 1/20W MF 201 — NO STUFF
R7968 100 5% 1/20W MF 201 — CPUIMVP_AXG_PGOOD
R7966 100 5% 1/20W MF 201 — P1V8S0_PGOOD
R7965 100 5% 1/20W MF 201 — P3V3S5_PGOOD
R7901 100 5% 1/20W MF 201 — P5VS3_PGOOD
R7964 100 5% 1/20W MF 201 — CPUVCCIOS0_PGOOD
R7963 100 5% 1/20W MF 201 — PVCCSA_PGOOD

R7962 330 5% 1/20W MF 201 — ALL_SYS_PWRGD

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L

Q7925 2N7002DW-X-G SOT-363 — AP_PWR_EN — (AC_EN_L)

AC_EN_L

Q7920 2N7002DW-X-G SOT-363 — SMC_ADAPTER_EN

NO STUFF R7929 0 5% 1/20W MF 201

Q7920 2N7002DW-X-G SOT-363 — (PM_SLP_S3_L)

PM_SLP_S3_L

Q7925 2N7002DW-X-G SOT-363 — NC — Unused fet

SYNC_MASTER=J13_MLB	SYNC_DATE=11/18/2011
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER 051-9276 SIZE D
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CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

=PP3V3_S5_LCD

LCD_IG_PWR_EN

CRITICAL
U9000
FPF1009
MFET-2X2-81N

ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD

PP3V3_SW_LCD_UF
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

R9014 1K 5% 1/20W MF 201
C9009 0.1UF 10% 6.3V X5R 201
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603

=I2C_TCON_SDA
=I2C_TCON_SCL

R9061 0 5% 1/20W MF 201
R9062 0 5% 1/20W MF 201

I2C_TCON_SDA_R
I2C_TCON_SCL_R

Pull-ups on panel side,
4.7 kOhm to 3.3V

DP_INT_HPD

R9060 0 5% 1/20W MF 201

DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

C9015 1000PF 10% 16V X7R 201

R9070 100K 5% 1/20W MF 201

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

DP_INT_AUX_CH_N
DP_INT_AUX_CH_P
DP_INT_ML_P<0>
DP_INT_ML_N<0>

C9024 0.1UF 10% 16V X5R-CERM 0201
C9025 0.1UF 10% 16V X5R-CERM 0201
C9020 0.1UF 10% 16V X5R-CERM 0201
C9021 0.1UF 10% 16V X5R-CERM 0201

(DP_INT_AUX_CH_C_N)
(DP_INT_AUX_CH_C_P)

DP_INT_AUX_CH_C_N
DP_INT_AUX_CH_C_P
DP_INT_ML_F_P<0>
DP_INT_ML_F_N<0>

PPVOUT_SW_LCDBKLT

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

R9018 1M 5% 1/20W MF 201
R9017 1M 5% 1/20W MF 201
PLACE_NEAR=J9000.24:1mm
PLACE_NEAR=J9000.25:1mm

R9050 100K 5% 1/20W MF 201
R9080 100K 5% 1/20W MF 201
PLACE_NEAR=J9000.14:2mm

C9017 1000PF 5% 50V C0G-CERM 603
PLACE_NEAR=J9000.3:2mm

LCD Connector

Internal DP Connector: 518S0829

CRITICAL
J9000
20525-130E-01
F-RT-SM

NC
NC
NC
NC
NC

LED Backlight I/F

DisplayPort I/F

SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2010

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-9276
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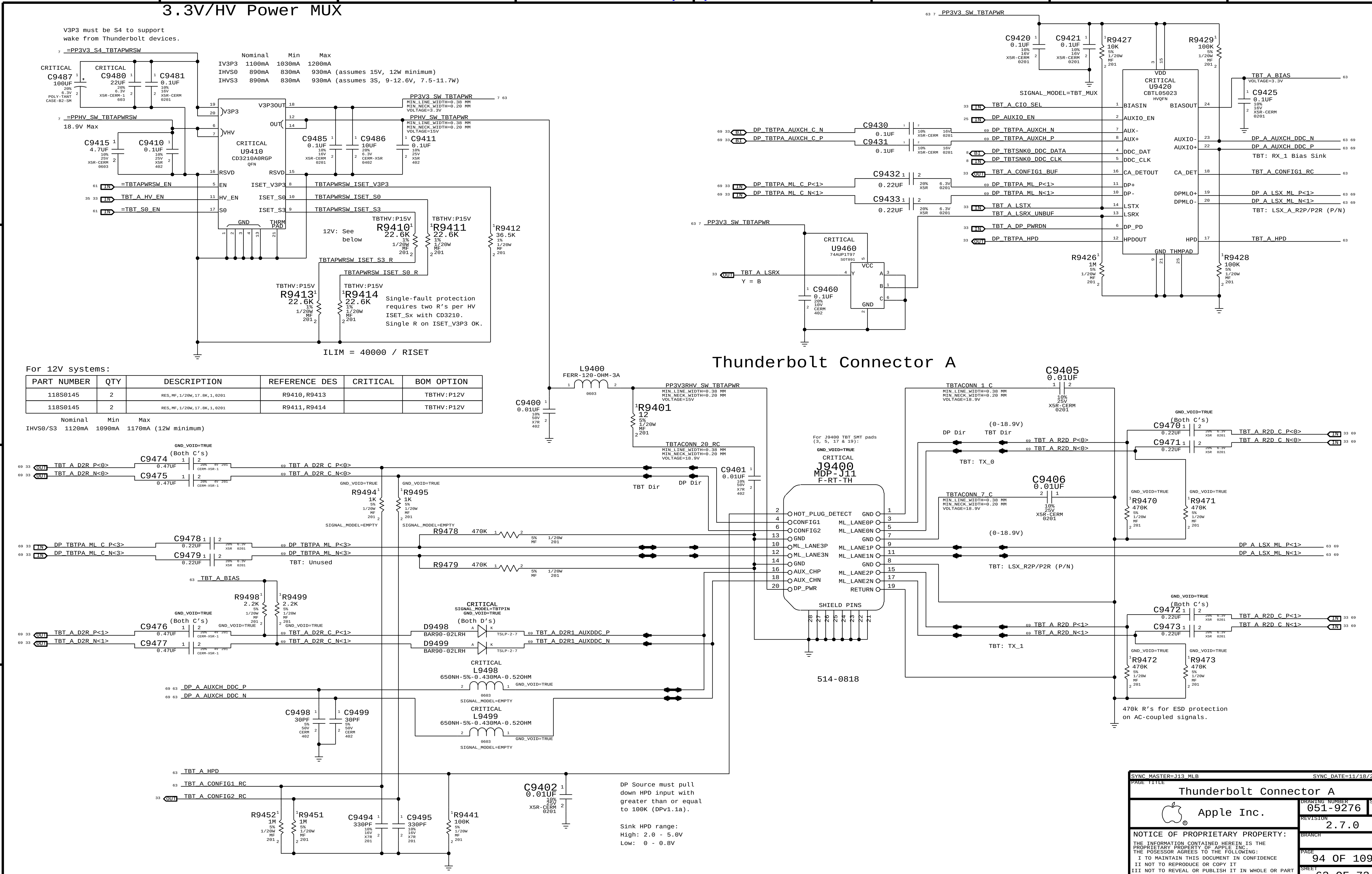
3.3V/HV Power MUX



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

SYNC_MASTER=J13_MLB SYNC_DATE=11/18/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9276 SIZE: D

REVISION: 2.7.0

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

THERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

F9700 3AMP-32V-467 603-HF BOTTOM
=PPBUS_S0_LCDBKLT
PPBUS_S0_LCDBKLT_FUSED MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.6V
R9788 301K 1% 1/20W MF 201
C9782 0.1UF 10% 16V X5R 402
CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF
PPBUS_SW_LCDBKLT_PWR MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.6V
LCDBKLT_EN_DIV
R9789 147K 1% 1/20W MF 201
LCDBKLT_EN_L
Q9707 SSM6N15FEAPE SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
Q9707 SSM6N15FEAPE SOT563
BKLT_PLT_RST_L

=PP5V_S0_BKL
=PPBUS_SW_BKL
CRITICAL C9712 10UF 10% 25V X5R 805
C9713 0.1UF 10% 25V X5R 402
PLACE_NEAR=L9701.1:3mm
CRITICAL L9701 15UH-2.8A PIMB053T-SM
PPBUS_SW_LCDBKLT_PWR_SW MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.150 MM VOLTAGE=50V SWITCH_NODE=TRUE DIDT=TRUE
PLACE_NEAR=L9701.2:3mm
CRITICAL D9701 SOD-123 RB160M-60G
PLACE_NEAR=U9701.A5:3mm
C9796 220PF 10% 50V X7R-CERM 402
CRITICAL C9797 10UF 10% 50V X5R 1210-1
CRITICAL C9799 10UF 10% 50V X5R 1210-1
PLACE_NEAR=D9701.2:5mm
PPVOUT_SW_LCDBKLT MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.375 MM VOLTAGE=50V
PLACE_NEAR=D9701.2:3mm
PLACE_NEAR=U9701.D1:5mm
C9710 1UF 10% 25V X5R 603-1
PLACE_NEAR=U9701.D1:3mm
C9714 0.01UF 10% 10V X5R 201
XW9720 SM
PPVOUT_SW_LCDBKLT_FB VOLTAGE=50V MIN_LINE_WIDTH=0.1 MM MIN_NECK_WIDTH=0.1 MM
PLACE_NEAR=C9797.1:5mm

=PP3V3_S0_BKL_VDDIO
PLACE_NEAR=U9701.C4:4mm
C9711 0.1UF 10% 6.3V X5R 201

U9701 25-BUMP-MICRO LP8550
VDDIO VLDO VIN
VSYNC FILTER ISET FSET SCLK SDA PWM EN FAULT
SW_0 SW_1 FB
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
GND_S GND_L GND_SW GND_SW
CRITICAL

BKL_VSYNC_R
BKL_FLTR
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
TP_BKL_FAULT PLACE_SIDE=BOTTOM
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6

R9741 10K 5% 1/20W MF 201
R9753 0 5% 1/20W MF 201
=I2C_BKL_1_SCL
R9757 0 5% 1/20W MF 201
=I2C_BKL_1_SDA
Addr: 0x58(Wr)/0x59(Rd)
PPBUS_SW_LCDBKLT_PWR
R9731 200K 1% 1/20W MF 201
R9715 100K 1% 1/20W MF 201
R9704 33 5% 1/20W MF 201
LCD_BKLT_PWM
C9704 33PF 5% 25V NP0-C0G 201

Fpwm=9.62kHz
see spec for others
R9755 10K 1% 1/20W MF 201
R9716 90.9K 1% 1/20W MF 201
I_LED=20.3mA
R9714 18.2K 1% 1/20W MF 201
GND_BKL_SGND MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V
XW9710 SM
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)

I_LED=369/Riset
(EEPROM should set EN_I_RES=1)

BKLT:PROD R9717 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E5:10mm
LED_RETURN_1 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

BKLT:PROD R9718 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.D5:10mm
LED_RETURN_2 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

BKLT:PROD R9719 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.C5:10mm
LED_RETURN_3 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

BKLT:PROD R9720 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E3:10mm
LED_RETURN_4 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

BKLT:PROD R9721 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E2:10mm
LED_RETURN_5 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

BKLT:PROD R9722 0 5% 1/16W MF-LF 402 BOTTOM
PLACE_NEAR=U9701.E1:10mm
LED_RETURN_6 MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J13_MLB SYNC_DATE=10/13/2011
PAGE TITLE: LCD Backlight Driver
Apple Inc.
DRAWING NUMBER 051-9276 SIZE D
REVISION 2.7.0
BRANCH
PAGE 97 OF 109
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 103

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	10 19 41
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_45S	CPU_TTP	XDP_DBRESET_L	10 23 25
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	10 23
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	10 23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_45S	CPU_TTP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	10 40
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	10 40 41 56
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	10 19 41
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	8 10
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	23
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L_R_CFG	CPU_45S	CPU_TTP	XDP_BPM_L<7..4>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_TTP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	23
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	12 56
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	12 56
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 58
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 58
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 56
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	12 56
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	12 56
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	12 56
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>	8 37
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>	8 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P	37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N	37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>	8 37
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>	8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P	37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N	37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>	8 37
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>	8 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>	6 37
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>	6 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>	6 8 37
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>	6 8 37
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>	
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	6 16 37
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	6 16 37
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	9 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	9 62
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>	6 62
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	6 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	6 62
	DP_80D	DP_AUX	DP_INT_AUX_CH_P	9 62
	DP_80D	DP_AUX	DP_INT_AUX_CH_N	9 62

DMI/FDI

PCIe SSD

DP

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing	"Real" Spacing
=2x_DIELECTRIC	=2x_DIELECTRIC
=5.7x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=8.6x_DIELECTRIC	=6x_DIELECTRIC
=5.7x_DIELECTRIC	=4x_DIELECTRIC
=PWR_P2MM	=PWR_P2MM
=GND_P2MM	=GND_P2MM
=8.6x_DIELECTRIC	=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	27 28 31

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE: Memory Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	SATA SSD
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	USB Hub nets
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	
USB_BT	USB_80D	USB	USB_BT_N	
	USB_80D	USB	USB_BT_CONN_P	
	USB_80D	USB	USB_BT_CONN_N	
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	
USB_TPAD	USB_80D	USB	USB_TPAD_N	
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	
	USB_80D	USB	USB_TPAD_R_P	
	USB_80D	USB	USB_TPAD_R_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
USB_SMC	USB_80D	USB	USB_SMC_P	
USB_SMC	USB_80D	USB	USB_SMC_N	
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	USB Camera nets
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	
USB_EXTA	USB_80D	USB	USB_EXTA_P	USB EXTA nets (Right USB port)
USB_EXTA	USB_80D	USB	USB_EXTA_N	
	UART_45S	UART	SMC_DEBUGPRT_TX_L	
	UART_45S	UART	SMC_DEBUGPRT_RX_L	
	USB_80D	USB	USB2_EXTA_MUXED_P	
	USB_80D	USB	USB2_EXTA_MUXED_N	
	USB_80D	USB	USB2_EXTA_MUXED_F_P	
	USB_80D	USB	USB2_EXTA_MUXED_F_N	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_P	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_N	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_P	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_N	
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_N	
USB_EXTB	USB_80D	USB	USB_EXTB_P	USB EXTB nets (Left USB port)
USB_EXTB	USB_80D	USB	USB_EXTB_N	
	USB_80D	USB	USB_EXTB_EHCI_P	
	USB_80D	USB	USB_EXTB_EHCI_N	
	USB_80D	USB	USB_EXTB_XHCI_P	
	USB_80D	USB	USB_EXTB_XHCI_N	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	Unused USB nets
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

SYNC_MASTER=CONSTRAINTS		SYNC_DATE=01/11/2012
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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LPC_AD	LPC_45S	LPC	LPC_AD<3..0> 6 16 40 42
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L 6 16 40 42
	LPC_45S	LPC	LPCPLUS_RESET_L 6 25 42
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC 25 40
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R 18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS 6 25 42
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R 18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN 16 25
	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT 18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK 16 43
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA 16 43
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK 16 43
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA 16 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK 16 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA 16 43
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK 6 16 39
	HDA_45S	HDA	HDA_BIT_CLK_R 16
HDA_SYNC	HDA_45S	HDA	HDA_SYNC 6 16 39
	HDA_45S	HDA	HDA_SYNC_R 16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L 16
	HDA_45S	HDA	HDA_RST_L 6 16 39
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0 6 16 39
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT 6 16 39
	HDA_45S	HDA	HDA_SDOUT_R 16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R 17 41
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K 40 41
SPI_CLK	SPI_45S	SPI	SPI_CLK_R 16 42
	SPI_45S	SPI	SPI_CLK 42
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R 16 42
	SPI_45S	SPI	SPI_MOSI 42
SPI_MISO	SPI_45S	SPI	SPI_MISO 16 42
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L 16 42
	SPI_45S	SPI	SPI_CS0_L 42
	SPI_45S	SPI	SPI_SMC_CLK 40 41
	SPI_45S	SPI	SPI_SMC_MOSI 40 41
	SPI_45S	SPI	SPI_SMC_MISO 40 41
	SPI_45S	SPI	SPI_SMC_CS_L 40 41
	SPI_45S	SPI	SPI_MLB_CLK 41 42 49
	SPI_45S	SPI	SPI_MLB_MOSI 41 42 49
	SPI_45S	SPI	SPI_MLB_MISO 41 42 49
	SPI_45S	SPI	SPI_MLB_CS_L 41 42 49
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P 6 36
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N 6 36
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P 16 36
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N 16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P 6 16 36
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N 6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P 6 16 36
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N 6 16 36
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0> 33
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0> 33
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0> 8 33
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0> 8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0> 8 33
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0> 8 33
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0> 33
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0> 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P 16 33
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N 16 33
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P 8 16
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N 8 16
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI 16 23
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO 16 23
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS 16 23
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK 16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0> 33
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0> 33
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0> 8 33
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0> 8 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N 33
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P 8 33
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N 8 33
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0> 33
DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0> 33
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0> 8 33
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0> 8 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P 33
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N 33
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P 8 33
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N 8 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC 16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB 16 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R 16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT 25 33
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R 33
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R 25

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/11/2012

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 33 63
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 33 63
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0> 63
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0> 63
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1> 33 63
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1> 33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3> 33 63
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3> 33 63
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2> 63
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2> 63
	DP_80D	DP_TX	DP_A_LSX_ML_P<1> 63
	DP_80D	DP_TX	DP_A_LSX_ML_N<1> 63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0> 63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0> 63
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1> 33 63
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1> 33 63
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0> 33 63
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0> 33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P 33 63
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N 33 63
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P 63
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N 63
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P 63
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N 63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 63
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 63
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 8 33
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 8 33
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2> 8 33
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2> 8 33
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0> 8 33
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0> 8 33
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P 8 33
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N 8 33
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 33
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 33
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 33
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 33

Only used on hosts supporting Thunderbolt video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	40 43
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	40 43
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	40 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	40 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	52
	1:1_DIFFPAIR		CHGR_CSI_R_P	52
	1:1_DIFFPAIR		CHGR_CSI_R_N	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	52
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	52
	1:1_DIFFPAIR		CHGR_CSO_R_P	52
	1:1_DIFFPAIR		CHGR_CSO_R_N	52

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	45 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	45 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_N	46
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	46
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	46
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	46
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_P	9 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_N	9 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	46
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	44 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	44 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_P	44 56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_N	44 57
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_P	44
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_P	44 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_N	44 57
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_P	44
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_P	44 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_N	44 53
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_P	44
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_P	44 60
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_N	44 60
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_P	44
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_P	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_P	56 57
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N	45 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P	45 55
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	36 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	36 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	37 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	37 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	8 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	8 45
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	50
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	50
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 50 51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 50 51
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

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Project Specific Constraints

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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