1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

MLB,D1,SCH (Prelimimary_Test)

7/7/12

Schematic / PCB #'s

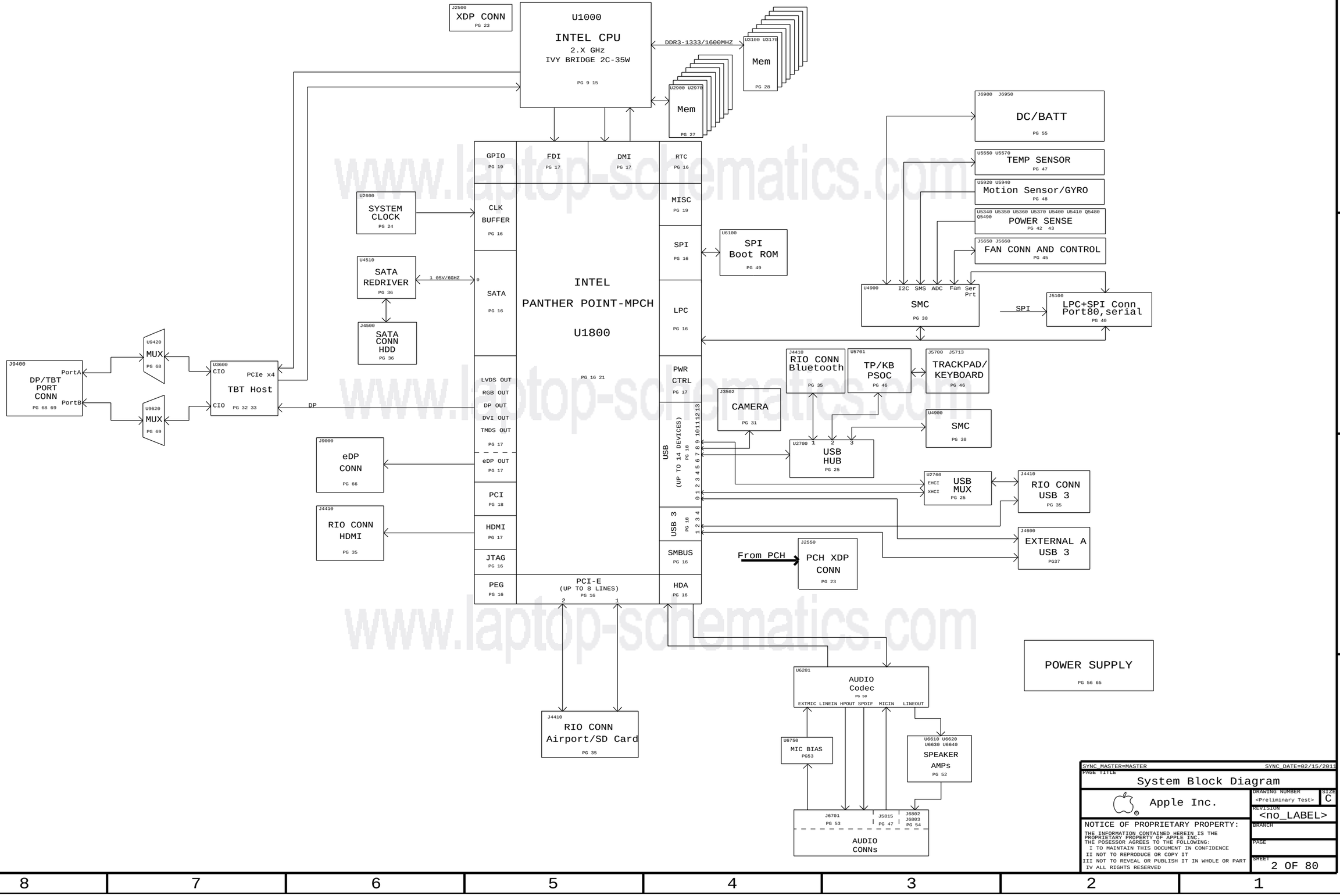
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
Preliminary_Test	1	SCHEM MLB D1	SCH	CRITICAL	
820-3190	1	PCBF MLB(NEW 2) D1	PCB	CRITICAL	

_DRAWING
TITLE=MLB (NEW_2)
ABBREV=ABBREV
LAST MODIFIED=Thu May 10 09 19 18 2012

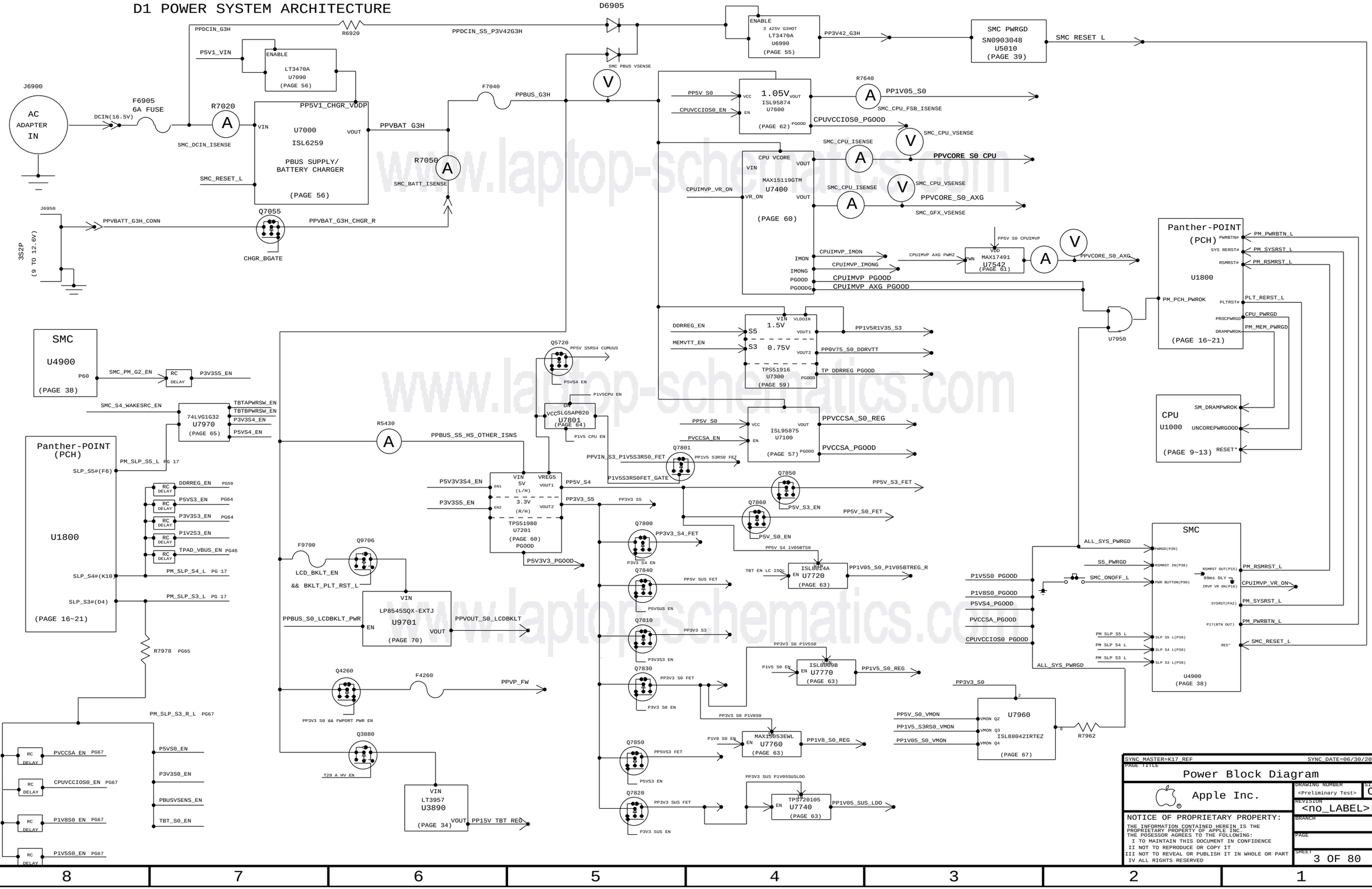
DRAWING TITLE: SCHEM,MLB,D1

Apple Inc.

DRAWING NUMBER: <Preliminary Test>
SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 1 OF 80



D1 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE: Power Block Diagram

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

BRANCH:

PAGE:

SHEET: 3 OF 80

EMPTY

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER <Preliminary Test>

SIZE C

REVISION <no_LABEL>

BRANCH

PAGE

SHEET 4 OF 80

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

D1 BOM GROUPS

BOM GROUP	BOM OPTIONS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

BRANCH

EMPTY

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <Preliminary Test>
SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 6 OF 80

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
- PP5V_S0 — 3 TPs per Fan
- FAN_LT_PWM
- FAN_LT_TACH

J5660 (RIGHT FAN CONN)
- FAN_RT_PWM
- FAN_RT_TACH
- GND — 5 TPs per Fan

J3502 (ALS/CAMERA CONN)
- SMBUS_SMC_2_S3_SDA
- SMBUS_SMC_2_S3_SCL
- PP5V_S3_ALSCAMERA_F

J4400 (RIO CABLE CONN)
- PP3V3_S4
- PP3V3_S3
- PP3V3_WLAN_F
- PP5V_S4
- PP1V5_S0

J4410 (RIO FLEX CONN)
- USB_EXTB_OC_L
- HDMI_IG_DDC_CLK
- HDMI_IG_DDC_DATA
- HDMI_HPD_L
- PM_SLP_S3_L
- PM_SLP_S4_L
- AP_CLKREQ_Q_L
- ENET_RESET_L
- ENET_CLKREQ_L
- SD_PWR_EN
- SDCONN_STATE_CHANGE_SMC
- PCIE_WAKE_L
- AP_CLKREQ_Q_L
- AP_RESET_CONN_L
- WIFI_EVENT_L
- USB_EXTB_P
- USB_EXTB_N
- USB_BT_CONN_P
- USB_BT_CONN_N

- AP_RESET_CONN_L
- SMBUS_PCH_CLK
- SMBUS_PCH_DATA

- SMBUS_SMC_1_S0_SCL
- SMBUS_SMC_1_S0_SDA

J5815 (KBD BACKLIGHT CONN)
- PP_KBD_BOOST_VOUT
- KBDLED_CATHODE1
- KBDLED_CATHODE2
- SMC_KBDLED_PRESENT_L

J6950 (MAIN BATT CONN)
- PPVBAT_G3H_CONN
- SMBUS_SMC_5_G3_SCL
- SMBUS_SMC_5_G3_SDA
- SYS_DETECT_L_R

- SYSDET1
- SYSDET_3_4

J6801 (2 MIC CONN)
- CON_DMIC_PWR
- CON_DMIC_SDA1
- CON_DMIC_CLK

- PCH_VSS_NCTF<19>
- PCH_VSS_NCTF<19>

J4600 (LEFT USB CONN)
- PP5V_S3_LTUSB_A_F
- USB_LT1_N
- USB_LT1_P

FUNC_TEST
- GND
- GND
- GND — 6 TPs

U1000 CHARZ TPS

PCIE_TBT_D2R_P<0>	P2MM SM	PP0700
PCIE_TBT_D2R_N<0>	P2MM SM	PP0701
DMI_S2N_P<0>	P2MM SM	PP0702
DMI_S2N_N<0>	P2MM SM	PP0703
DMI_CLK100M_CPU_P	P2MM SM	PP0721
DMI_CLK100M_CPU_N	P2MM SM	PP0722

U1800 CHARZ TPS

DMI_N2S_P<0>	P2MM SM	PP0704
DMI_N2S_N<0>	P2MM SM	PP0705
FDI_DATA_P<0>	P2MM SM	PP0706
FDI_DATA_N<0>	P2MM SM	PP0707
FDI_DATA_P<4>	P2MM SM	PP0708
FDI_DATA_N<4>	P2MM SM	PP0709
PCIE_AP_D2R_P	P2MM SM	PP0710
PCIE_AP_D2R_N	P2MM SM	PP0711
PCIE_ENET_D2R_P	P2MM SM	PP0712
PCIE_ENET_D2R_N	P2MM SM	PP0713
PCIE_CLK100M_TBT_P	P2MM SM	PP0723
PCIE_CLK100M_TBT_N	P2MM SM	PP0724

U4900 CHARZ TPS

LPC_AD<0>	P2MM SM	PP0714
LPC_AD<1>	P2MM SM	PP0715
LPC_AD<2>	P2MM SM	PP0716
LPC_AD<3>	P2MM SM	PP0717
LPC_FRAME_L	P2MM SM	PP0718
LPC_CLK33M_SMC	P2MM SM	PP0719
AUD_DMIC_SDA1	P2MM SM	PP0720

J6701 (AUDIO JACK CONN)
- AUD_CONN_SLEEVE
- AUD_CONN_MIC_XW
- AUD_CONN_SLEEVE_XW
- AUD_CONN_HP_LEFT
- AUD_CONN_TIPDET_INV
- PP3V3_S0
- AUD_SPDIF_OUT_JACK
- AUD_CONN_HP_RIGHT
- AUD_CONN_TYPEDET
- AUD_CONN_MIC

J6802 (AUDIO LEFT SPEAKER CONN)
- SPKRCONN_L_OUT_P
- SPKRCONN_L_OUT_N
- SPKRCONN_L_ID
- SPKRCONN_SL_OUT_P
- SPKRCONN_SL_OUT_N

J6803 (AUDIO RIGHT SPEAKER CONN)
- SPKRCONN_R_OUT_P
- SPKRCONN_R_OUT_N
- SPKRCONN_R_ID
- SPKRCONN_SR_OUT_P
- SPKRCONN_SR_OUT_N
- GND

J9000 (EDP CONN)
- PP5VR3V3_SW_LCD
- PPVOUT_S0_LCDBKLT — 2 TP needed
- LED_RETURN_6
- LED_RETURN_5
- LED_RETURN_4
- LED_RETURN_3
- LED_RETURN_2
- LED_RETURN_1
- LCD_HPD_CONN
- DP_INT_AUX_P
- DP_INT_AUX_N

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)
- PCIE_CLK100M_AP_CONN_P
- PCIE_CLK100M_AP_CONN_N
- AP_CLKREQ_Q_L
- PCIE_WAKE_L
- AP_RESET_CONN_L
- PP3V3_WLAN_F
- PP5V_S3_ALSCAMERA_F
- SMBUS_SMC_2_S3_SDA
- SMBUS_SMC_2_S3_SCL
- USB_CAMERA_CONN_P
- USB_CAMERA_CONN_N

J5713 (KEY BOARD CONN)
- PP3V3_S4
- PP3V42_G3H
- WS_KBD1
- WS_KBD2
- WS_KBD3
- WS_KBD4
- WS_KBD5
- WS_KBD6
- WS_KBD7
- WS_KBD8
- WS_KBD9
- WS_KBD10
- WS_KBD11
- WS_KBD12
- WS_KBD13
- WS_KBD14
- WS_KBD15_CAP
- WS_KBD16_NUM
- WS_KBD17
- WS_KBD18
- WS_KBD19
- WS_KBD20
- WS_KBD21
- WS_KBD22
- WS_KBD23
- WS_KBD_ONOFF_L
- WS_LEFT_SHIFT_KBD
- WS_LEFT_OPTION_KBD
- WS_CONTROL_KBD

J5700 (IPD FLEX CONN)
- PP3V3_S4
- Z2_CS_L
- Z2_MOSI
- Z2_MISO
- Z2_SCLK
- Z2_HOST_INTN
- PP5V_S4_CUMULUS
- Z2_CLKIN
- SMBUS_SMC_2_S3_SCL
- SMBUS_SMC_2_S3_SDA
- PSOC_SCLK
- PSOC_MOSI
- PSOC_MISO
- PICKB_L
- PSOC_F_CS_L
- Z2_KEY_ACT_L

J6900 (DC POWER CONN)
- TDM_ONEWIRE_MPM
- ADAPTER_SENSE
- PP18V5_DCIN_FUSE
- GND

J4500 (SSD/HDD FLEX CONN)
- PP3V3_S0_SSD_FLT
- SMC_OOB1_TX_L
- SMC_OOB1_RX_L
- PP5V_S0_HDD_FLT
- GND

FUNC_TEST
- BKLT_EN
- LCD_BKLT_PWM
- PM_CLKRUN_L
- PM_SYSRST_L
- SMC_ONOFF_L

J5100 (LPC + SPI CONN)
- PP3V42_G3H
- PP5V_S0
- LPC_CLK33M_LPCPLUS
- LPC_AD<0>
- LPC_AD<2>
- LPC_AD<1>
- LPC_AD<3>
- SPI_ALT_MOSI
- LPCPLUS_GPIO
- LPCPLUS_RESET_L
- SMC_TDO
- TP_SMC_TRST_L
- TP_SMC_MD1
- SMC_TX_L
- SPI_ALT_MISO
- LPC_FRAME_L
- SPIROM_USE_MLB
- PM_CLKRUN_L
- SPI_ALT_CLK
- SPI_ALT_CS_L
- LPC_SERIRQ
- LPC_PWRDWN_L
- SMC_TDI
- SMC_TCK
- SMC_RESET_L
- SMC_ROMBOOT
- SMC_RX_L
- SMC_TMS

POWER RAILS

FUNC_TEST
- PM_SLP_S3_L
- PP0V75_S0_DDRVTT
- PP1V05_S0
- LED_RETURN_2
- LED_RETURN_3
- LED_RETURN_4
- LED_RETURN_5
- LED_RETURN_6
- GND — 4 TPs
- PP3V3_S0
- PP3V3_S3
- PP3V3_S5
- PP3V3_S5_AVREF_SMC
- PP3V42_G3H
- PP5V_S0
- PP5V_S3
- PP5V_S5
- PPBUS_G3H
- PPDCIN_G3H
- PPVCORE_S0_CPU
- PPVTTDDR_S3
- DMI_S2N_P<3..1>
- DMI_S2N_N<3..1>
- DMI_N2S_P<3..1>
- DMI_N2S_N<3..1>

- TBTBPWRSW_ISET_V3P3
- TBTBPWRSW_ISET_S0_R
- TBTBPWRSW_ISET_S3
- TBTAPWRSW_ISET_V3P3
- TBTAPWRSW_ISET_S0
- TBTAPWRSW_ISET_S3
- TBTAPWRSW_ISET_S3_R

- TBT_A_R2D_C_P<1..0>
- TBT_A_R2D_C_N<1..0>
- TBT_A_R2D_P<1..0>
- TBT_A_R2D_N<1..0>
- TBT_A_D2R_C_P<1>
- TBT_A_D2R_C_N<1>
- TBT_A_D2R_C_P<0>
- TBT_A_D2R_C_N<0>

- TBT_A_D2R_P<1>
- TBT_A_D2R_N<1>
- TBT_A_D2R_P<0>
- TBT_A_D2R_N<0>

- TBT_B_R2D_C_P<1..0>
- TBT_B_R2D_C_N<1..0>
- TBT_B_R2D_P<1..0>
- TBT_B_R2D_N<1..0>
- TBT_B_D2R_C_P<0>
- TBT_B_D2R_C_N<0>
- TBT_B_D2R_C_P<1>
- TBT_B_D2R_C_N<1>

- TBT_B_D2R_P<0>
- TBT_B_D2R_N<0>
- TBT_B_D2R_P<1>
- TBT_B_D2R_N<1>

- PCIE_AP_D2R_P
- PCIE_AP_D2R_N
- PCIE_AP_R2D_P
- PCIE_AP_R2D_N

ICT Test Points

CPU NO_TESTs

TP_TBT_MONDC0		NC_TBT_MONDC0
TP_TBT_MONDC1		NC_TBT_MONDC1
TP_TBT_PCIE_RESET0_L		NC_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L		NC_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L		NC_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L		NC_TBT_PCIE_RESET3_L
TP_TBT_XTAL25OUT		NC_TBT_XTAL25OUT
TP_DP_TBTSRC_ML_CP<3>		NC_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>		NC_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>		NC_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>		NC_DP_TBTSRC_ML_CN<2>
TP_DP_TBTSRC_ML_CP<1>		NC_DP_TBTSRC_ML_CP<1>
TP_DP_TBTSRC_ML_CN<1>		NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>		NC_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>		NC_DP_TBTSRC_ML_CN<0>
TP_DP_TBTSRC_AUXCH_CP		NC_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN		NC_DP_TBTSRC_AUXCH_CN
TP_SPI_CS1_L		NC_SPI_CS1_L
TP_PCH_GPIO8		NC_PCH_GPIO8
TP_PCH_STRP_BBS1		NC_PCH_STRP_BBS1
TP_PCH_STRP_ESI_L		NC_PCH_STRP_ESI_L
TP_PCH_TP23		NC_PCH_TP23
TP_PCI_CLK33M_OUT2		NC_PCI_CLK33M_OUT2
TP_PCIE_CLK100M_PEGAN		NC_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP		NC_PCIE_CLK100M_PEGAP
TP_PM_SLP_A_L		NC_PM_SLP_A_L
TP_PPVOUT_PCH_DCPSUSBYP		NC_PPVOUT_PCH_DCPSUSBYP
TP_SMC_MPM5_LED_PWR		NC_SMC_MPM5_LED_PWR
TP_SMC_MPM5_LED_CHG		NC_SMC_MPM5_LED_CHG
TP_SMS_INT2		NC_SMS_INT2

- PCIE_TBT_R2D_C_P<3..0>
- PCIE_TBT_R2D_C_N<3..0>
- PCIE_TBT_R2D_P<3..0>
- PCIE_TBT_R2D_N<3..0>
- PCIE_TBT_D2R_P<3..1>
- PCIE_TBT_D2R_N<3..1>
- PCIE_TBT_D2R_C_P<3..1>
- PCIE_TBT_D2R_C_N<3..1>

- MEM_A_DQ<0>
- MEM_A_DQ<12..2>
- MEM_A_DQ<19..14>
- MEM_A_DQ<24..21>
- MEM_A_DQ<32..26>
- MEM_A_DQ<42..34>
- MEM_A_DQ<54..44>
- MEM_A_DQ<56>
- MEM_A_DQ<63..58>
- MEM_B_DQ<2..0>
- MEM_B_DQ<13..4>
- MEM_B_DQ<19..15>
- MEM_B_DQ<25..21>
- MEM_B_DQ<35..27>
- MEM_B_DQ<40..37>
- MEM_B_DQ<47..42>
- MEM_B_DQ<57..49>
- MEM_B_DQ<63..59>
- NC_MEM_EVENT_L

- HDMI_IG_CLK_C_P
- HDMI_IG_CLK_C_N
- HDMI_IG_DATA_C_P<2..0>
- HDMI_IG_DATA_C_N<2..0>

- PCIE_CLK100M_ENET_P
- PCIE_CLK100M_ENET_N
- USB3_EXTA_TX_C_P
- USB3_EXTB_TX_C_N

- TP_XDP_PCH_HOOK4 — NC_XDP_PCH_HOOK4
- TP_XDP_PCH_HOOK5 — NC_XDP_PCH_HOOK5
- TP_XDP_PCH_OBSFN_B<0> — NC_XDP_PCH_OBSFN_B<0>
- TP_XDP_PCH_OBSFN_B<1> — NC_XDP_PCH_OBSFN_B<1>
- TP_XDP_PCH_OBSFN_A<0> — NC_XDP_PCH_OBSFN_A<0>
- TP_XDP_PCH_OBSFN_A<1> — NC_XDP_PCH_OBSFN_A<1>
- TP_XDP_PCH_OBSFN_D<0> — NC_XDP_PCH_OBSFN_D<0>
- TP_XDP_PCH_OBSFN_D<1> — NC_XDP_PCH_OBSFN_D<1>
- TP_XDP_PCH_TRST_L — NC_XDP_PCH_TRST_L

- TP_1V05_S0_PCH_VCCAPLLEXP — NC_1V05_S0_PCH_VCCAPLLEXP
- TP_AUD_CODEC_MICBIAS — NC_AUD_CODEC_MICBIAS
- TP_AUD_MIC_INRP — NC_AUD_MIC_INRP
- TP_AUD_MIC_INRN — NC_AUD_MIC_INRN
- AUD_SPDIF_IN — AUD_SPDIF_IN
- TP_BKL_FAULT — NC_BKL_FAULT
- TP_LPC_DREQ0_L — NC_LPC_DREQ0_L

S2 CAMERA PCIE SIGNALS

NC_PCIE_CAMERA_D2RP		PCIE_EXCARD_D2R_N
NC_PCIE_CAMERA_D2RN		PCIE_EXCARD_D2R_P
NC_PCIE_CAMERA_R2D_CN		PCIE_EXCARD_R2D_C_N
NC_PCIE_CAMERA_R2D_CP		PCIE_EXCARD_R2D_C_P
NC_PCIE_CLK100M_CAMERAN		PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_CAMERAP		PCIE_CLK100M_EXCARD_P

NO_TEST NC NO_TESTs
- NC_PCIE_5_D2RN
- NC_PCIE_5_D2RP
- NC_PCIE_5_R2D_CN
- NC_PCIE_5_R2D_CP
- NC_PCIE_6_D2RN
- NC_PCIE_6_D2RP
- NC_PCIE_6_R2D_CN
- NC_PCIE_6_R2D_CP
- NC_PCIE_7_D2RN
- NC_PCIE_7_D2RP
- NC_PCIE_7_R2D_CN
- NC_PCIE_7_R2D_CP
- NC_PCIE_8_D2RN
- NC_PCIE_8_D2RP
- NC_PCIE_8_R2D_CN
- NC_PCIE_8_R2D_CP

- TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4N
- TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4P
- TP_PCIE_CLK100M_PEBN — NC_PCIE_CLK100M_PEBN
- TP_PCIE_CLK100M_PEBP — NC_PCIE_CLK100M_PEBP

- TP_SATA_C_D2RN — NC_SATA_C_D2RN
- TP_SATA_C_D2RP — NC_SATA_C_D2RP
- TP_SATA_C_R2D_CN — NC_SATA_C_R2D_CN
- TP_SATA_C_R2D_CP — NC_SATA_C_R2D_CP
- TP_SATA_D_D2RN — NC_SATA_D_D2RN
- TP_SATA_D_D2RP — NC_SATA_D_D2RP
- TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN
- TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP
- TP_SATA_E_D2RN — NC_SATA_E_D2RN
- TP_SATA_E_D2RP — NC_SATA_E_D2RP
- TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN
- TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP
- TP_SATA_F_D2RN — NC_SATA_F_D2RN
- TP_SATA_F_D2RP — NC_SATA_F_D2RP
- TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN
- TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP

- TP_CRT_IG_BLUE — NC_CRT_IG_BLUE
- TP_CRT_IG_GREEN — NC_CRT_IG_GREEN
- TP_CRT_IG_RED — NC_CRT_IG_RED
- TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK
- TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA
- TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC
- TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC

- TP_HDA_SDIN1 — NC_HDA_SDIN1
- TP_HDA_SDIN2 — NC_HDA_SDIN2
- TP_HDA_SDIN3 — NC_HDA_SDIN3

- TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN
- TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP
- TP_SDVO_STALLN — NC_SDVO_STALLN
- TP_SDVO_STALLP — NC_SDVO_STALLP
- TP_SDVO_INTN — NC_SDVO_INTN
- TP_SDVO_INTP — NC_SDVO_INTP

- TP_PCI_PME_L — NC_PCI_PME_L
- TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3

- NC_ISNS_LCDBKLTN
- NC_ISNS_LCDBKLTP
- NC_ISNS_WLANN
- NC_ISNS_WLANP
- NC_ISNS_LCD_PANELN
- NC_ISNS_LCD_PANELP

PCH ALIASES
- NC_LPC_DREQ0_L — TP_LPC_DREQ0_L
- NC_LPC_DREQ1_L — TP_LPC_DREQ1_L
- TP_CLINK_CLK — NC_CLINK_CLK
- TP_CLINK_DATA — NC_CLINK_DATA
- TP_CLINK_RESET_L — NC_CLINK_RESET_L

- PCIE_ENET_R2D_C_P
- PCIE_ENET_R2D_C_N
- PCIE_AP_R2D_C_P
- PCIE_AP_R2D_C_N
- PCIE_AP_D2R_P
- PCIE_AP_D2R_N
- PCIE_AP_D2R_PI_P
- PCIE_AP_D2R_PI_N
- PCIE_AP_R2D_PI_P
- PCIE_AP_R2D_PI_N

- PCIE_CLK100M_PCH_P
- PCIE_CLK100M_PCH_N
- PCIE_CLK100M_TBT_P
- PCIE_CLK100M_TBT_N

- PCH_CLK100M_SATA_P
- PCH_CLK33M_PCIIN

- PCIE_CLK100M_SSD_P
- PCIE_CLK100M_SSD_N
- PEG_CLK100M_P
- PEG_CLK100M_N
- PCIE_CLK100M_ENET_P
- PCIE_CLK100M_ENET_N
- PCIE_CLK100M_AP_P
- PCIE_CLK100M_AP_N
- PCIE_CLK100M_FW_P
- PCIE_CLK100M_FW_N
- PCIE_CLK100M_EXCARD_P
- PCIE_CLK100M_EXCARD_N

- SATA_HDD_R2D_RDRIN_P
- SATA_HDD_R2D_RDRIN_N
- SATA_HDD_D2R_RDROUT_P
- SATA_HDD_D2R_RDROUT_N
- SATA_HDD_D2R_RDRIN_P
- SATA_HDD_D2R_RDRIN_N
- SATA_HDD_R2D_RDROUT_P
- SATA_HDD_R2D_RDROUT_N
- SATA_HDD_D2R_RC_P
- SATA_HDD_D2R_RC_N
- SATA_HDD_R2D_RC_N
- SATA_HDD_R2D_RC_P

- SATA_HDD_R2D_C_P
- SATA_HDD_R2D_C_N
- SATA_HDD_D2R_P
- SATA_HDD_D2R_N

- SATA_SSDRHDD_D2R_P
- SATA_SSDRHDD_D2R_N
- SATA_SSDRHDD_R2D_P
- SATA_SSDRHDD_R2D_N

- USB3_EXTA_RX_F_P
- USB3_EXTA_RX_F_N
- USB3_EXTA_RX_P
- USB3_EXTA_RX_N

- USB3_EXTA_TX_C_P
- USB3_EXTA_TX_C_N
- USB3_EXTA_TX_N
- USB3_EXTA_RX_N

- USB3_EXTB_RX_RC_P
- USB3_EXTB_RX_RC_N
- USB3_EXTB_RX_P
- USB3_EXTB_RX_N

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Functional / ICT Test

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

BRANCH

PAGE

SHEET: 7 OF 80

G3H Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPBUS_S0_LCDBKLT
=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE
=PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S0_CPUIMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_CPUVCCIOS0
=PPVIN_S0_CPUAXG
=PPVIN_S0_VCCSAS0

=PPVIN_S5_HS_OTHER_ISNS
PPVIN_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 mm MAKE_BASE=TRUE
=PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm VOLTAGE=18.5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMC
=PP3V42_G3H_CHGR
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_BMU
=PP3V42_G3H_SMBUS_SMC_5
=PP3V42_G3H_AUDIO
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TDM
=PP3V42_G3H_TPAD
=PP3V42_S3_HALL
=PPVIN_S5_SMCVREF
For PCH RTC Power
=PPVBAT_G3_SYSCLK

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.3 mm VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.1 mm MAKE_BASE=TRUE
=PP5V_S5_P1V5S3RS0FET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD

=PP5V_SUS_FET
PP5V_SUS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_SUS_PCH

=PP5V_S4_REG
PP5V_S4
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S4_AUDIO
=PP5V_S4_RIO
=PP5V_S4_P1V05TBTS0
=PP5V_S4_TPAD

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.5 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S3_ISNS
=PP5V_S3_ALSCAMERA
=PP5V_S3_DDRREG
=PP5V_S3_DEBUG_ADC_AVDD
=PP5V_S3_DEBUG_ADC_DVDD
=PP5V_S3_DEBUG_ISNS
=PP5V_S3_MEMRESET

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 mm VOLTAGE=5V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP5V_S0_AUDIO_XW
=PP5V_S0_AUDIO
=PP5V_S0_BKL
=PP5V_S0_CPUIMVP
=PP5V_S0_CPUVCCIOS0
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_HDD
=PP5V_S0_RMC
=PP5V_S0_VCCSAS0
=PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET
PP3V3_S4
MIN_LINE_WIDTH=0.6 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 mm MAKE_BASE=TRUE
=PP3V3_S4_TBT
=PP3V3_S4_RIO
=PP3V3_S4_TPAD
=PP3V3_S4_SMC
=PP3V3_S4_BT

=PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.6 mm VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_CNTRL
=PP3V3_SUS_SMC

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SMCBATLOW
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_XDP
=PP3V3_S5_P1V5S0

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.508MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.28MM MAKE_BASE=TRUE
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_PCH_GPIO
=PP3V3_S3_RIO
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_SMBUS_SMC_3
=PP3V3_S3_USBMUX
=PP3V3_S3_USB_HUB
=PP3V3_S3_USB_RESET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_GYRO
=PP3V3_S3_SMS
=PP3V3_S3_SDBUF
=PP3V3_S3_CAMERA
=PP3V3_S3_P1V2S3
=PP3V3_S3_P1V8S3
=PP3V3_S3_BT

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 mm MAKE_BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_P1V5S0
=PP3V3_S0_P1V8S0
=PP3V3_S0_BKLI2C
=PP3V3_S0_DDCMUX
=PP3V3_S0_FAN_LT
=PP3V3_S0_FAN_RT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_HS_ISNS
=PP3V3_S0_IMVPISNS
=PP3V3_S0_ISNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_LCD
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_PCI
=PP3V3_S0_PCH_VCC3_3_SATA
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PCH_VCC3_3
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SATAMUX
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD
=PP3V3_S0_SYSCLK
=PP3V3_S0_TBTI2C
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_HDMI
=PP3V3_S0_TPAD
=PP3V3_S0_VMON
=PP3V3_S0_XDP
=PP3V3_S0_DDR3THMSNS
=PP3V3_S0_SPKRTHMSNS
=PP3V3_S0_HS_COMPUTING_ISNS
=PP3V3_S0_HS_OTHER_ISNS
=PP3V3_S0_PCH_STRAPS

=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.2 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPDDR_S3_REG
PP1V5R1V35_S3
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.35V
MAKE_BASE=TRUE
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V5R1V35_MEM
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.35V
MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B
=PP1V5_S3_MEMRESET

=PP1V5_S3RS0_FET
PP1V5_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S3RS0_VMON
=PP1V5R1V35_S3_CPU_VCCDDR

=PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PP1V5_S0_RDRVR

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.675V
MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.675V
MAKE_BASE=TRUE
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU_VCCIO
=PPVCCIO_S0_XDP
=PPVCCIO_S0_CPUIMVP
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON
=PP1V05_S0_RMC
=PP1V05_S0_PCH_VCCIO_PLLPCIE
=PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCIO_USB
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCCIO_CLK
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCCIO_PLLUSB
=PP1V05_S0_PCH_VCC_DMI
=PP1V05_S0_PCH_VCCIO_PLLFDI
=PP1V05_S0_PCH_VCCDMI_FDI

=PPBUS_G3H_T25
PPBUS_G3H_T25_PWR
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=12.6V

Backlight Rails

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.6 MM MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 MM VOLTAGE=12.6V
PPBUS_S0_LCDBKLT_PWR

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG
2A max supply
PP1V8_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8R1V5_S0_PCH_VCCVRM
=PP1V8_S0_AUDIO
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_PCH_VCC_DFTERM
=PPVDDIO_S0_SBCLK

=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.3 MM VOLTAGE=18.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

TBT Rails (off when no cable)

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V

=PP15V_TBT_REG
PP15V_TBT
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=15V
MAKE_BASE=TRUE
=PPHV_SW_TBTAPWRSW
=PPHV_SW_TBTBPWRSW

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_TBT_PCH_GPIO
=PP3V3_TBTLC_RTR
=PPVDDIO_TBT_CLK
=PP3V3_TBT_PCH_GPIO

=PP1V05_S0_P1V05TBTREG_R
PP1V05_S0_P1V05TBTREG_R
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PP1V05_S0_P1V05TBTREG
PP1V05_S0_P1V05TBTREG
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_TBTLC_RTR
=PP1V05_TBTLC

=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_TBTCIO_RTR

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.25V
=PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.05V
=PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 mm MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.5V

=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE

=PPVCCSA_S0_REG
PPVCCSA_S0_REG
MIN_LINE_WIDTH=0.6 mm VOLTAGE=0.9V
MIN_NECK_WIDTH=0.2 mm MAKE_BASE=TRUE
=PPVCCSA_S0_CPU

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE
Power Aliases
Apple Inc.
DRAWING NUMBER <Preliminary Test>
SIZE C
REVISION <no_LABEL>
BRANCH
PAGE
SHEET 8 OF 80

Bosses for limiting deflection

SH0910
2.8OD1.2ID-2.25H-SM-D1
SH0911
2.8OD1.2ID-2.25H-SM-D1
SH0912
2.8OD1.2ID-2.25H-SM-D1
SH0913
2.8OD1.2ID-2.25H-SM-D1

Frame Holes

ZT0940
4P5R2P3-3P5B
ZT0960
4P5R2P3-3P5B

SH0950
SM
SHLD-D1-USB

SH0951
SM
SHLD-D1-MLB-T29

D1 THERMAL MODULE STANDOFF (860-1439)

SH0920
STDOFF-4.50D2.15H-SM
SH0921
STDOFF-4.50D2.15H-SM

SH0926
STDOFF-4.50D2.15H-SM
SH0927
STDOFF-4.50D2.15H-SM

D1 BMU MODULE STANDOFFS

SH0928
STDOFF-4.50D1.73H-SM
APN: 860-1490

SH0963
STDOFF-4.50D2.33H-SM

SH0963 is BMU standoff with flange. 860-1534

TH0900 for upper TBT can gnd slot

TH0903 for lower TBT can gnd slot

TH0904,5 for USB can gnd slot

TH0900
TH-NSP
SL-1.1X0.5-1.4x0.8

TH0903
TH-NSP
SL-1.1X0.5-1.4x0.8

APN:862-0118

TH0904
TH-NSP
SL-1.1X0.45-1.4x0.75

APN:998-3975

TH0905
TH-NSP
SL-1.1X0.45-1.4x0.75

FAN BOSSES (4X 860-1327)

SH0922
STDOFF-4.50D1.8H-SM
SH0923
STDOFF-4.50D1.8H-SM
SH0924
STDOFF-4.50D1.8H-SM
SH0925
STDOFF-4.50D1.8H-SM

D1 POGO PINS (870-2451)

SH0932
POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0933
POGO-2.3OD-4.1H-SM-LOW-FORCE
SH0934
POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0935
POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0936
POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0937
POGO-2.3OD-5.5H-SM-LOW-FORCE

D1 ELIPTICAL SLOT HOLES

ZT0930
TH-NSP
SL-3.9X2.3-4.2x2.6

ZT0920
TH-NSP
SL-2.8X1.8-3.1x2.1

ZT0931
TH-NSP
SL-3.9X2.3-4.2x2.6

MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0
RAMCFG3:L R0913 1K 5% 1/20W MF 2012
RAMCFG2:L R0912 1K 5% 1/20W MF 2012
RAMCFG1:L R0911 1K 5% 1/20W MF 2012
RAMCFG0:L R0910 1K 5% 1/20W MF 2012

LCD_BKLT_PWM — LVDS_IG_BKL_PWM
LCD_BKLT_EN — LVDS_IG_BKL_ON
LCD_PWR_EN — LVDS_IG_PANEL_PWR

eDP signals

DP_INT_AUX_C_P — TP_EDP_AUX_P
DP_INT_AUX_C_N — TP_EDP_AUX_N
DP_INT_ML_C_P<3..0> — TP_EDP_TX_P<3..0>
DP_INT_ML_C_N<3..0> — TP_EDP_TX_N<3..0>

CR SFF DG v1p0 Table 3-56 mapping for HDMI

HDMI_IG_CLK_C_P — TP_DP_IG_B_MLP<3>
HDMI_IG_CLK_C_N — TP_DP_IG_B_MLN<3>
HDMI_IG_DATA_C_P<2..0> — TP_DP_IG_B_MLP<0..2>
HDMI_IG_DATA_C_N<2..0> — TP_DP_IG_B_MLN<0..2>
HDMI_IG_DDC_CLK — DPA_IG_DDC_CLK
HDMI_IG_DDC_DATA — DPA_IG_DDC_DATA
HDMI_HPD — DPA_IG_HPD

DP_TBTSNK0_AUXCH_C_P — DPB_IG_AUX_CH_P
DP_TBTSNK0_AUXCH_C_N — DPB_IG_AUX_CH_N
DP_TBTSNK0_ML_C_P<3..0> — TP_DP_IG_C_MLP<3..0>
DP_TBTSNK0_ML_C_N<3..0> — TP_DP_IG_C_MLN<3..0>
DP_TBTSNK0_DDC_CLK — DPB_IG_DDC_CLK
DP_TBTSNK0_DDC_DATA — DPB_IG_DDC_DATA
DP_TBTSNK0_HPD — DPB_IG_HPD

DP_TBTSNK1_AUXCH_C_P — TP_DP_IG_D_AUXP
DP_TBTSNK1_AUXCH_C_N — TP_DP_IG_D_AUXN
DP_TBTSNK1_ML_C_P<3..0> — TP_DP_IG_D_MLP<3..0>
DP_TBTSNK1_ML_C_N<3..0> — TP_DP_IG_D_MLN<3..0>
DP_TBTSNK1_DDC_CLK — TP_DP_IG_D_CTRL_CLK
DP_TBTSNK1_DDC_DATA — TP_DP_IG_D_CTRL_DATA
DP_TBTSNK1_HPD — TP_DP_IG_D_HPD

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

=PP5V_S0_AUDIO_XW

XW0902
SM
PP5V_S0_AUDIO_AMP_L
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XW0903
SM
PP5V_S0_AUDIO_AMP_R
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

NC_PCH_GPIO64_CLKOUTFLEX0 — TP_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1 — TP_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2 — TP_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3 — TP_PCH_GPIO67_CLKOUTFLEX3

CPU signals

MEMVTT_EN — =DDRVTT_EN

T29 Signals Through PEG

PCIE_TBT_D2R_P<3..0> — =PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0> — =PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0> — =PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0> — =PEG_R2D_C_N<11..8>

SD_PWR_EN_PCH — ENET_LOW_PWR_PCH
SD_PWR_EN — ENET_LOW_PWR
TP_FW_PWR_EN — FW_PWR_EN

Unused PEG signals

NC_PEG_D2RP<15..12> — =PEG_D2R_P<15..12>
NC_PEG_D2RN<15..12> — =PEG_D2R_N<15..12>
NC_PEG_R2D_CP<15..12> — =PEG_R2D_C_P<15..12>
NC_PEG_R2D_CN<15..12> — =PEG_R2D_C_N<15..12>

Unused GPU signals

NC_PEG_D2RP<7..0> — =PEG_D2R_P<7..0>
NC_PEG_D2RN<7..0> — =PEG_D2R_N<7..0>
NC_PEG_R2D_CP<7..0> — =PEG_R2D_C_P<7..0>
NC_PEG_R2D_CN<7..0> — =PEG_R2D_C_N<7..0>

NC_DPA_IG_AUX_CHP — DPA_IG_AUX_CH_P
NC_DPA_IG_AUX_CHN — DPA_IG_AUX_CH_N

NC_PEG_CLK100MN — PEG_CLK100M_N
NC_PEG_CLK100MP — PEG_CLK100M_P

UNUSED USB SIGNALS

NC_USB3_EXTC_TXP — USB3_EXTC_TX_P
NC_USB3_EXTC_TXN — USB3_EXTC_TX_N
NC_USB3_EXTC_RXP — USB3_EXTC_RX_P
NC_USB3_EXTC_RXN — USB3_EXTC_RX_N
NC_USB_EXTCP — USB_EXTC_P
NC_USB_EXTCN — USB_EXTC_N
NC_USB3_EXTD_TXP — USB3_EXTD_TX_P
NC_USB3_EXTD_TXN — USB3_EXTD_TX_N
NC_USB3_EXTD_RXP — USB3_EXTD_RX_P
NC_USB3_EXTD_RXN — USB3_EXTD_RX_N
NC_USB_EXTD_EHCIP — USB_EXTD_EHCI_P
NC_USB_EXTD_EHCIN — USB_EXTD_EHCI_N
NC_USB_4N — TP_USB_4N
NC_USB_4P — TP_USB_4P
NC_USB_SDN — TP_USB_SDN
NC_USB_SDP — TP_USB_SDP
NC_USB_WLANN — TP_USB_WLANN
NC_USB_WLANP — TP_USB_WLANP
NC_USB_BT_HSN — TP_USB_BT_HSN
NC_USB_BT_HSP — TP_USB_BT_HSP
NC_USB_12N — TP_USB_12N
NC_USB_12P — TP_USB_12P
NC_USB_13N — TP_USB_13N
NC_USB_13P — TP_USB_13P

USB SIGNALS

USB_BT_P — USBHUB_DN1_P
USB_BT_N — USBHUB_DN1_N
USB_TPAD_P — USBHUB_DN2_P
USB_TPAD_N — USBHUB_DN2_N
USB_SMC_P — USBHUB_DN3_P
USB_SMC_N — USBHUB_DN3_N
PU_USBHUB_DN4_P — USBHUB_DN4_P
PU_USBHUB_DN4_N — USBHUB_DN4_N

NC_CPU_THERMDN — CPU_THERMD_N
NC_CPU_THERMDP — CPU_THERMD_P
NC_LCD_FSS — LCD_FSS

NC_PCIE_CLK100M_SSDN — PCIE_CLK100M_SSD_N
NC_PCIE_CLK100M_SSDP — PCIE_CLK100M_SSD_P
NC_PCIE_CLK100M_FWN — PCIE_CLK100M_FW_N
NC_PCIE_CLK100M_FWP — PCIE_CLK100M_FW_P
NC_PCIE_FW_D2RN — PCIE_FW_D2R_N
NC_PCIE_FW_D2RP — PCIE_FW_D2R_P
NC_PCIE_FW_R2D_CN — PCIE_FW_R2D_C_N
NC_PCIE_FW_R2D_CP — PCIE_FW_R2D_C_P

Unused SATA ODD Signals

NC_SATA_ODD_D2RN — SATA_ODD_D2R_N
NC_SATA_ODD_D2RP — SATA_ODD_D2R_P
NC_SATA_ODD_R2D_CN — SATA_ODD_R2D_C_N
NC_SATA_ODD_R2D_CP — SATA_ODD_R2D_C_P

Unused Memory Signals

NC_MEM_A_CLKP<1> — MEM_A_CLK_P<1>
NC_MEM_A_CLKN<1> — MEM_A_CLK_N<1>
NC_MEM_B_CLKP<1> — MEM_B_CLK_P<1>
NC_MEM_B_CLKN<1> — MEM_B_CLK_N<1>

=PP3V3_S0_PWRCTL

R0991 10K 5% 1/20W MF 2012

Unused PGOOD signal

CPUIMVP_AXG_PGOOD

TP_P1V5S3RS0_RAMP_DONE — P1V5S3RS0_RAMP_DONE
TP_DDRREG_PGOOD — DDRREG_PGOOD

SYNC_MASTER=D1_MLB_TEST
SYNC_DATE=01/27/2012
PAGE TITLE
Signal Aliases
Apple Inc.
DRAWING NUMBER <Preliminary Test>
SIZE C
REVISION <no_LABEL>
BRANCH
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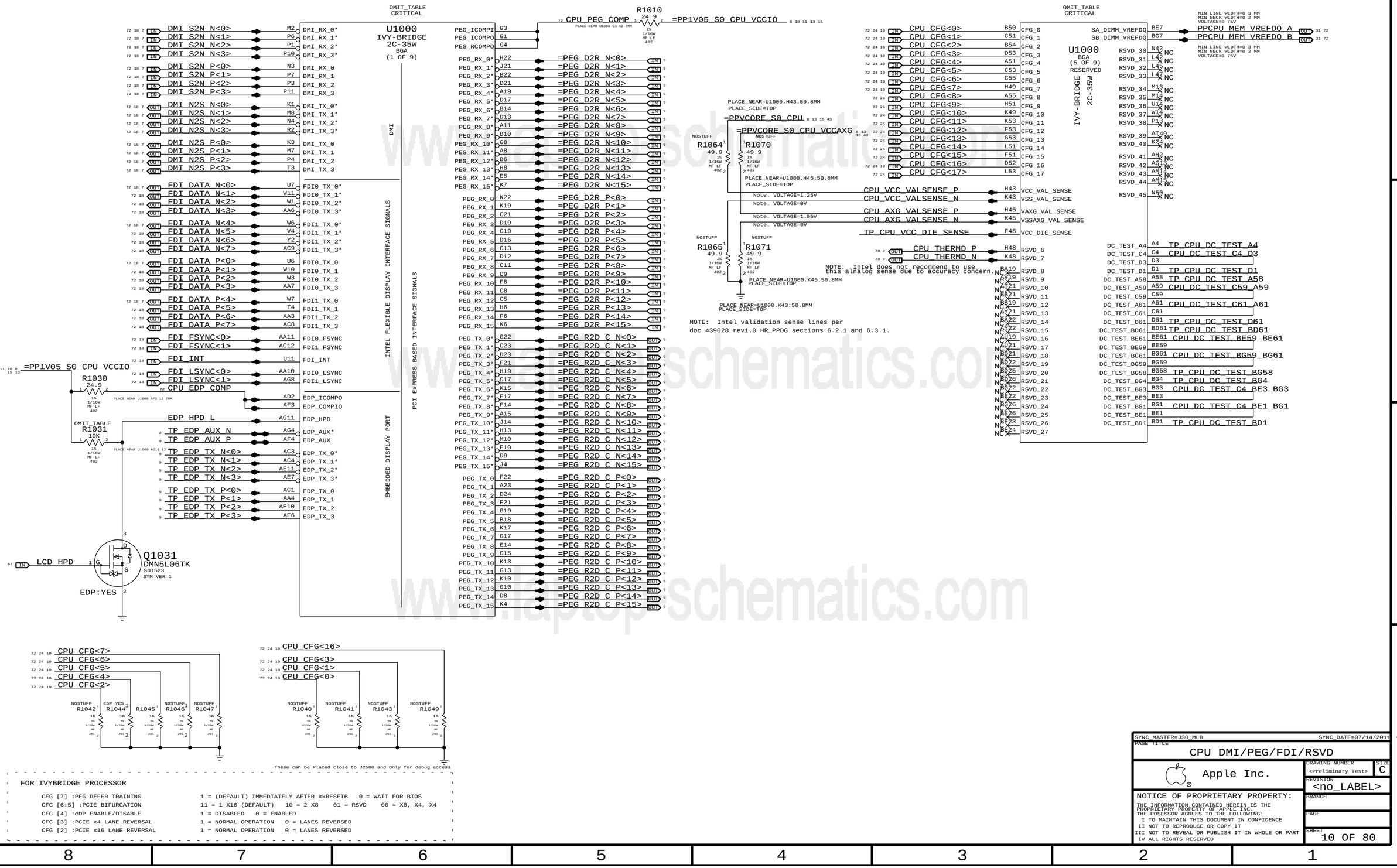
NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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PAGE:

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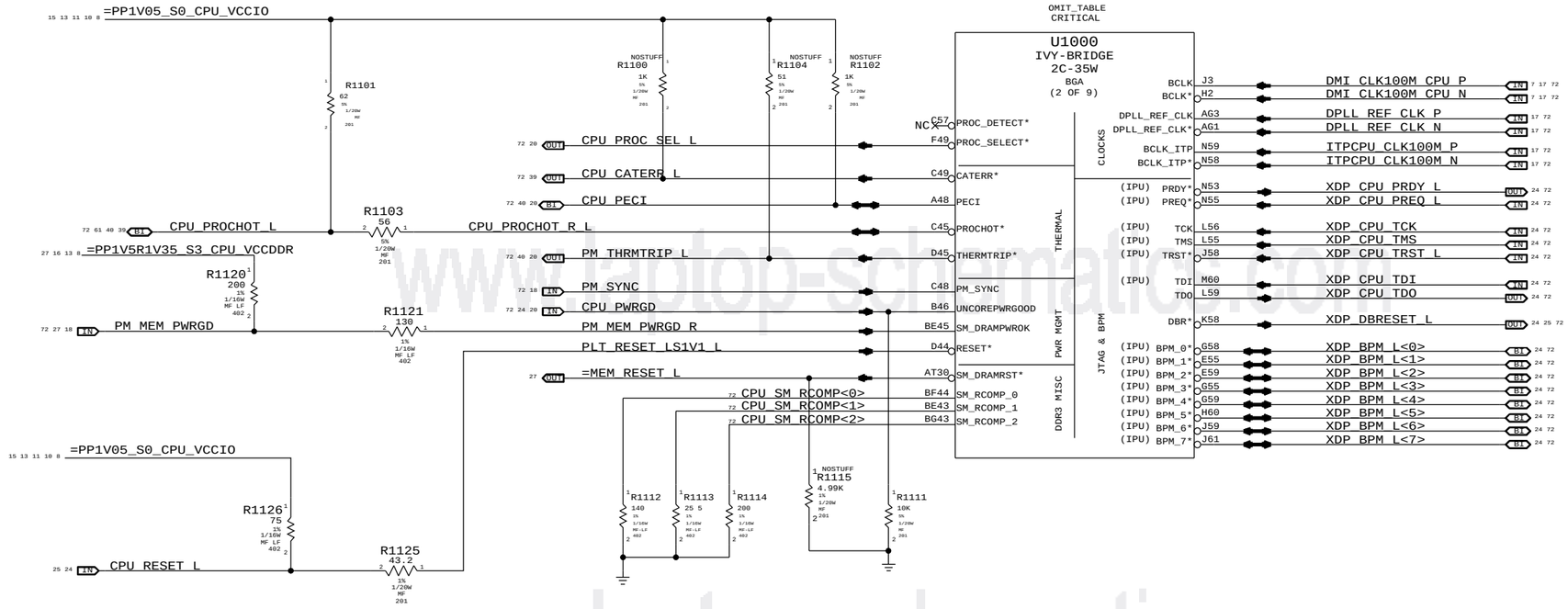

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

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REVISION <no_LABEL>

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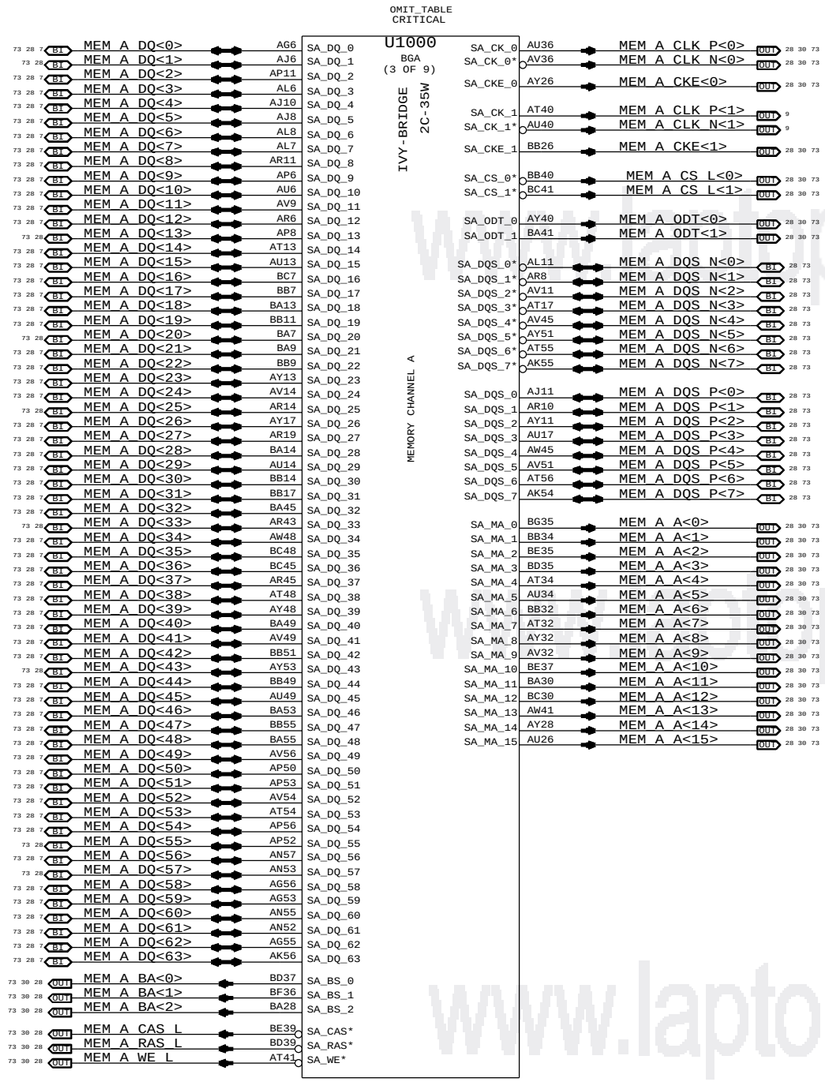

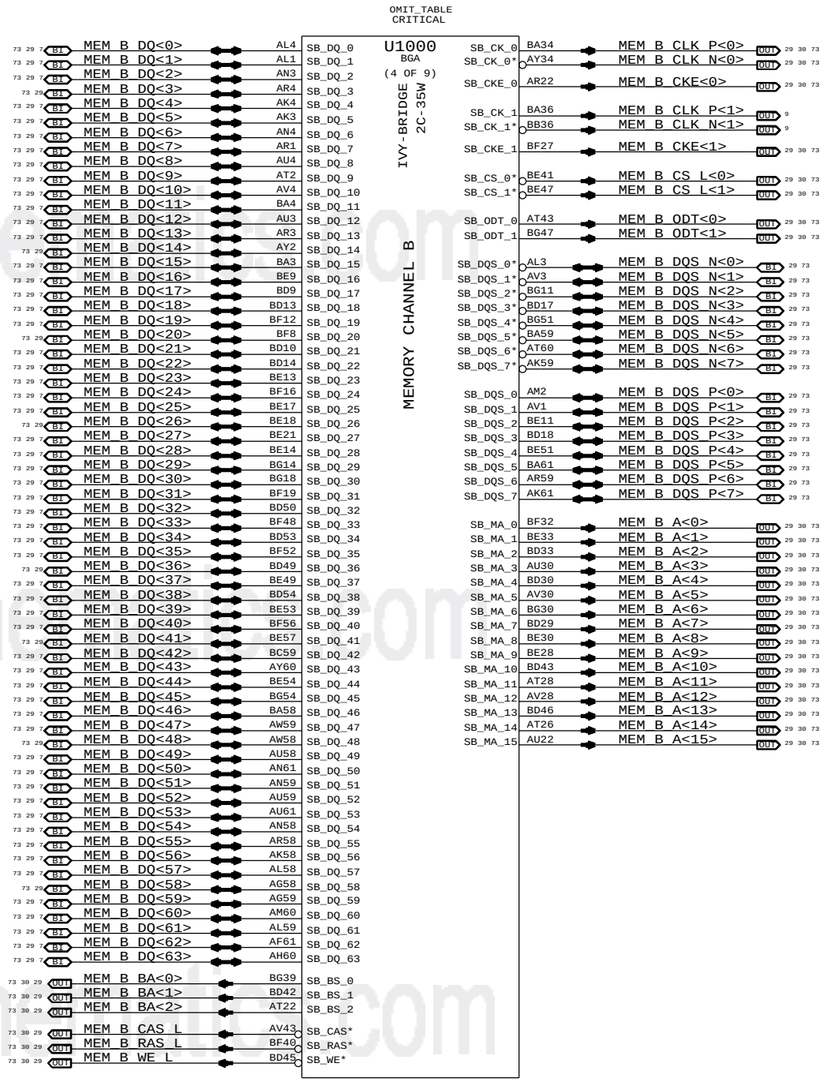

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER <Preliminary Test>

SIZE C

REVISION <no_LABEL>

BRANCH

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=PPVCORE_S0_CPU
15 13 10 8 43

OMIT_TABLE
CRITICAL

U1000
BGA
(6 OF 9)

IVY-BRIDGE 2C-35W

CORE SUPLLY

A26	VCC_1	VCCIO_1	AF46
A29	VCC_2	VCCIO_3	AG48
A31	VCC_3	VCCIO_4	AG50
A34	VCC_4	VCCIO_5	AG51
A35	VCC_5	VCCIO_6	AJ17
A38	VCC_6	VCCIO_7	AJ21
A39	VCC_7	VCCIO_8	AJ25
A42	VCC_8	VCCIO_9	AJ43
C26	VCC_9	VCCIO_10	AJ47
C27	VCC_10	VCCIO_11	AK50
C32	VCC_11	VCCIO_12	AK51
C34	VCC_12	VCCIO_13	AL14
C37	VCC_13	VCCIO_14	AL15
C39	VCC_14	VCCIO_15	AL16
C42	VCC_15	VCCIO_16	AL20
D27	VCC_16	VCCIO_17	AL22
D32	VCC_17	VCCIO_18	AL26
D34	VCC_18	VCCIO_19	AL45
D37	VCC_19	VCCIO_20	AL48
D39	VCC_20	VCCIO_21	AM16
D42	VCC_21	VCCIO_22	AM17
E26	VCC_22	VCCIO_23	AM21
E28	VCC_23	VCCIO_24	AM43
E32	VCC_24	VCCIO_25	AM47
E34	VCC_25	VCCIO_26	AN20
E37	VCC_26	VCCIO_27	AN42
E38	VCC_27	VCCIO_28	AN45
F25	VCC_28	VCCIO_29	AN48
F26	VCC_29	VCCIO_30	AA14
F28	VCC_30	VCCIO_31	AA15
F32	VCC_31	VCCIO_32	AB17
F34	VCC_32	VCCIO_33	AB20
F37	VCC_33	VCCIO_34	AC13
F38	VCC_34	VCCIO_35	AD16
F42	VCC_35	VCCIO_36	AD18
G42	VCC_36	VCCIO_37	AD21
H25	VCC_37	VCCIO_38	AE14
H26	VCC_38	VCCIO_39	AE15
H28	VCC_39	VCCIO_40	AF16
H29	VCC_40	VCCIO_41	AF18
H32	VCC_41	VCCIO_42	AF20
H34	VCC_42	VCCIO_43	AG15
H35	VCC_43	VCCIO_44	AG16
H37	VCC_44	VCCIO_45	AG17
H38	VCC_45	VCCIO_46	AG20
H40	VCC_46	VCCIO_47	AG21
J25	VCC_47	VCCIO_48	AJ14
J26	VCC_48	VCCIO_49	AJ15
J28	VCC_49	VCCIO_50	W16
J29	VCC_50	VCCIO_51	W17
J32	VCC_51		
J34	VCC_52	VCCIO_SEL	BC22
J35	VCC_53		
J37	VCC_54	VCCPQE_1	AM25
J38	VCC_55	VCCPQE_2	AN22
J40	VCC_56		
J42	VCC_57	VIDALERT*	A44
K26	VCC_58	VIDSCLK	B43
K27	VCC_59	VIDSOUT	C44
K29	VCC_60		
K32	VCC_61	VCC_SENSE	F43
K34	VCC_62	VSS_SENSE	G43
K35	VCC_63		
K37	VCC_64	VCCIO_SENSE	AN16
K39	VCC_66	VSS_SENSE_VCCIO	AN17
K42	VCC_67		
L25	VCC_68		
L28	VCC_69		
L33	VCC_70		
L36	VCC_71		
L40	VCC_72		
N26	VCC_73		
N30	VCC_74		
N34	VCC_75		
N38	VCC_76		

=PP1V05_S0_CPU_VCCIO
8 10 11 13 15

(NOT controlled by VCCIO SEL)
Fixed at 1 05V

QUIET RAIL

SVID

SENSE LINES

=PP3V3_S0_CPU_VCCIO_SEL
8

NOSTUFF
R1320[1] 10K 5% 1/20W MF 201 2

IVB supports 1 05V VCCIO
VCCIO SEL can be NC

CPU_VCCIO_SEL

=PP1V05_S0_CPU_VCCPQE
8 15

CPU_VIDALERT_L_R
CPU_VIDSCLK_R
CPU_VIDSOUT_R

CPU_VCCSENSE_P
CPU_VCCSENSE_N

CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N

R1302 130 1% 1/16W MF LF 402 PLACE_NEAR=U1000.C44:2.54mm
R1300 75 1% 1/20W MF 201 PLACE_NEAR=R1310.2:2.54mm
R1310 43 1/20W 1% MF
CPU_VIDALERT_L
PLACE_NEAR=U1000.A44:38mm
R1311 0 1/20W 5% MF
CPU_VIDSCLK
R1312 0 1/20W 5% MF
CPU_VIDSOUT

=PPVCORE_S0_CPU
8 10 13 15 43
=PP1V05_S0_CPU_VCCIO
8 10 11 13 15

R1360[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.F43:50.8mm PLACE_SIDE=TOP
R1362[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.AN16:50.8mm PLACE_SIDE=TOP

Note. VOLTAGE=1.25V OUT 61 72
Note. VOLTAGE=0V OUT 61 72
Note. VOLTAGE=1.05V OUT 63 72
Note. VOLTAGE=0V OUT 63 72

R1361[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.G43:50.8mm PLACE_SIDE=TOP
R1363[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.AN17:50.8mm PLACE_SIDE=TOP

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.

=PPVCORE_S0_CPU_VCCAXG
43 16 13 10 8

OMIT_TABLE
CRITICAL

U1000
BGA
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IVY-BRIDGE 2C-35W GRPHICS DDR3-1.5V RAILS

AA46	VAXG_1	VDDQ_1	AJ28
AB47	VAXG_2	VDDQ_2	AJ33
AB50	VAXG_3	VDDQ_3	AJ36
AB51	VAXG_4	VDDQ_4	AJ40
AB52	VAXG_5	VDDQ_5	AL30
AB53	VAXG_6	VDDQ_6	AL34
AB55	VAXG_7	VDDQ_7	AL38
AB56	VAXG_8	VDDQ_8	AL42
AB58	VAXG_9	VDDQ_9	AM33
AB59	VAXG_10	VDDQ_10	AM36
AC61	VAXG_11	VDDQ_11	AM40
AD47	VAXG_12	VDDQ_12	AN30
AD48	VAXG_13	VDDQ_13	AN34
AD50	VAXG_14	VDDQ_14	AN38
AD51	VAXG_15	VDDQ_15	AR26
AD52	VAXG_16	VDDQ_16	AR28
AD53	VAXG_17	VDDQ_17	AR30
AD55	VAXG_18	VDDQ_18	AR32
AD56	VAXG_19	VDDQ_19	AR34
AD58	VAXG_20	VDDQ_20	AR36
AD59	VAXG_21	VDDQ_21	AR40
AE46	VAXG_22	VDDQ_22	AV41
N45	VAXG_23	VDDQ_23	AW26
P47	VAXG_24	VDDQ_24	BA46
P48	VAXG_25	VDDQ_25	BB28
P50	VAXG_26	VDDQ_26	BG33
P51	VAXG_27		
P52	VAXG_28	VCCDQ_1	AM28
P53	VAXG_29	VCCDQ_2	AN26
P55	VAXG_30		
P56	VAXG_31	VDDQ_SENSE	BC43
P61	VAXG_32	VSS_SENSE_VDDQ	BA43
T48	VAXG_33		
T58	VAXG_34	VCCSA_SENSE	U10
T59	VAXG_35		
T61	VAXG_36	VCCSA_VID_0	D48
U46	VAXG_37	VCCSA_VID_1	D49
V47	VAXG_38		
V48	VAXG_39	SM_VREF	AY43
V50	VAXG_40		
V51	VAXG_41		
V52	VAXG_42		
V53	VAXG_43		
V55	VAXG_44		
V56	VAXG_45		
V58	VAXG_46		
V59	VAXG_47		
W50	VAXG_48		
W51	VAXG_49		
W52	VAXG_50		
W53	VAXG_51		
W55	VAXG_52		
W56	VAXG_53		
W61	VAXG_54		
Y48	VAXG_55		
Y61	VAXG_56		
F45	VAXG_SENSE		
G45	VSSAXG_SENSE		
BB3	VCCPLL_1		
BC1	VCCPLL_2		
BC4	VCCPLL_3		
L17	VCCSA_1		
L21	VCCSA_2		
N16	VCCSA_3		
N20	VCCSA_4		
N22	VCCSA_5		
P17	VCCSA_6		
P20	VCCSA_7		
R16	VCCSA_8		
R18	VCCSA_9		
R21	VCCSA_10		
U15	VCCSA_11		
V16	VCCSA_12		
V17	VCCSA_13		
V18	VCCSA_14		
V21	VCCSA_15		
W20	VCCSA_16		

=PP1V5R1V35_S3_CPU_VCCDDR
8 11 13 16 27

QUIET RAIL

=PP1V5_S3_CPU_VCCDQ
8 16

SENSE LINE

CPU_VDDQ_SENSE_P
CPU_VDDQ_SENSE_N
Note. VOLTAGE=1.05V
Note. VOLTAGE=0V
CPU_VCCSASENSE
OUT 58 72
CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>
OUT 58 72
CPU_SM_VREF
13
VOLTAGE=0 75V

R1382[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.U10:50.8mm
R1380[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.BC43:50.8mm PLACE_SIDE=TOP
R1381[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.BA43:50.8mm PLACE_SIDE=TOP

=PPVCCSA_S0_CPU
16 13 8

=PP1V5R1V35_S3_CPU_VCCDDR
27 16 13 11 8

R1314 10K 5% 1/20W MF 201
R1313 10K 5% 1/20W MF 201

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.

=PP1V5R1V35_S3_CPU_VCCDDR
27 16 13 11 8

R1330[1] 1K 1% 1/16W MF LF 402 PLACE_NEAR=U1000.BJ44:2.54mm
CPU_SM_VREF
13
R1331[1] 1K 1% 1/16W MF LF 402 PLACE_NEAR=U1000.BJ44:2.54mm
C1330 0.1UF 10% 16V X7R_CERM 0402

PLACE_NEAR=U1000.BJ44:2.54mm

=PP1V8_S0_CPU_VCCPLL_R
15 8

1.8V RAIL

=PPVCCSA_S0_CPU
16 13 8

SA RAIL

R1370[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.F45:50.8mm PLACE_SIDE=TOP
R1371[1] 100 1% 1/16W MF LF 402 PLACE_NEAR=U1000.G45:50.8mm PLACE_SIDE=TOP

Note. VOLTAGE=1.05V
Note. VOLTAGE=0V

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.

SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE

CPU POWER

Apple Inc.

DRAWING NUMBER <Preliminary Test> SIZE C

REVISION <no_LABEL>

BRANCH

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OMIT_TABLE
CRITICAL

U1000
BGA
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IVY-BRIDGE
2C-35W

BG13	VSS		VSS	M11
BG17	VSS		VSS	M15
BG21	VSS		VSS	M58
BG24	VSS		VSS	N1
BG28	VSS		VSS	N17
BG37	VSS		VSS	N21
BG41	VSS		VSS	N25
BG45	VSS		VSS	N28
BG49	VSS		VSS	N33
BG53	VSS		VSS	N36
C29	VSS		VSS	N40
C35	VSS		VSS	N43
C40	VSS		VSS	N47
D4	VSS		VSS	N48
D6	VSS		VSS	N51
D10	VSS		VSS	N52
D14	VSS		VSS	N56
D18	VSS		VSS	N61
D22	VSS		VSS	P9
D26	VSS		VSS	P14
D29	VSS		VSS	P16
D35	VSS		VSS	P18
D40	VSS		VSS	P21
D43	VSS		VSS	P58
D46	VSS		VSS	P59
D50	VSS		VSS	R4
D54	VSS		VSS	R17
D58	VSS		VSS	R20
E3	VSS		VSS	R46
E25	VSS		VSS	T1
E29	VSS		VSS	T47
E35	VSS		VSS	T50
E40	VSS		VSS	T51
F13	VSS		VSS	T52
F15	VSS		VSS	T53
F19	VSS		VSS	T55
F29	VSS		VSS	T56
F35	VSS		VSS	U8
F40	VSS		VSS	U13
F55	VSS		VSS	V20
G6	VSS		VSS	V61
G48	VSS		VSS	W8
G51	VSS		VSS	W13
G61	VSS		VSS	W15
H4	VSS		VSS	W18
H10	VSS		VSS	W21
H14	VSS		VSS	W46
H17	VSS		VSS	Y4
H21	VSS		VSS	Y47
H53	VSS		VSS	Y58
H58	VSS		VSS	Y59
J1	VSS			
J49	VSS			
J55	VSS			
K8	VSS			
K11	VSS			
K21	VSS		VSS_NCTF	A5
K51	VSS		VSS_NCTF	A57
L16	VSS		VSS_NCTF	BC61
L20	VSS		VSS_NCTF	BD3
L22	VSS		VSS_NCTF	BD59
L26	VSS		VSS_NCTF	BE4
L30	VSS		VSS_NCTF	BE58
L34	VSS		VSS_NCTF	BG5
L38	VSS		VSS_NCTF	BG57
L43	VSS		VSS_NCTF	C3
L48	VSS		VSS_NCTF	C58
L61	VSS		VSS_NCTF	D59
M4	VSS		VSS_NCTF	E1
M6	VSS		VSS_NCTF	E61

OMIT_TABLE
CRITICAL

U1000
BGA
(8 OF 9)
IVY-BRIDGE
2C-35W

A9	VSS		VSS	AM34
A13	VSS		VSS	AM38
A17	VSS		VSS	AM42
A21	VSS		VSS	AM45
A25	VSS		VSS	AM48
A28	VSS		VSS	AM58
A33	VSS		VSS	AN1
A37	VSS		VSS	AN21
A40	VSS		VSS	AN25
A45	VSS		VSS	AN28
A49	VSS		VSS	AN33
A53	VSS		VSS	AN36
AA1	VSS		VSS	AN40
AA8	VSS		VSS	AN43
AA13	VSS		VSS	AN47
AA50	VSS		VSS	AN50
AA51	VSS		VSS	AN54
AA52	VSS		VSS	AP7
AA53	VSS		VSS	AP10
AA55	VSS		VSS	AP51
AA56	VSS		VSS	AP55
AB16	VSS		VSS	AR7
AB18	VSS		VSS	AR13
AB21	VSS		VSS	AR17
AB48	VSS		VSS	AR21
AB61	VSS		VSS	AR41
AC6	VSS		VSS	AR48
AC10	VSS		VSS	AR61
AC14	VSS		VSS	AT4
AC46	VSS		VSS	AT14
AD4	VSS		VSS	AT19
AD17	VSS		VSS	AT36
AD20	VSS		VSS	AT45
AD61	VSS		VSS	AT52
AE8	VSS		VSS	AT58
AE13	VSS		VSS	AU1
AF1	VSS		VSS	AU7
AF17	VSS		VSS	AU11
AF21	VSS		VSS	AU28
AF47	VSS		VSS	AU32
AF48	VSS		VSS	AU51
AF50	VSS		VSS	AV17
AF51	VSS		VSS	AV21
AF52	VSS		VSS	AV22
AF53	VSS		VSS	AV34
AF55	VSS		VSS	AV40
AF56	VSS		VSS	AV48
AF58	VSS		VSS	AV55
AF59	VSS		VSS	AW7
AG7	VSS		VSS	AW13
AG10	VSS		VSS	AW43
AG14	VSS		VSS	AW61
AG18	VSS		VSS	AY4
AG47	VSS		VSS	AY9
AG52	VSS		VSS	AY14
AG61	VSS		VSS	AY19
AH4	VSS		VSS	AY30
AH58	VSS		VSS	AY36
AJ7	VSS		VSS	AY41
AJ13	VSS		VSS	AY45
AJ16	VSS		VSS	AY49
AJ20	VSS		VSS	AY55
AJ22	VSS		VSS	AY58
AJ26	VSS		VSS	BA1
AJ30	VSS		VSS	BA11
AJ34	VSS		VSS	BA17
AJ38	VSS		VSS	BA21
AJ42	VSS		VSS	BA26
AJ45	VSS		VSS	BA32
AJ48	VSS		VSS	BA48
AK1	VSS		VSS	BA51
AK52	VSS		VSS	BB53
AL10	VSS		VSS	BC5
AL13	VSS		VSS	BC13
AL17	VSS		VSS	BC57
AL21	VSS		VSS	BD8
AL25	VSS		VSS	BD12
AL28	VSS		VSS	BD16
AL33	VSS		VSS	BD19
AL36	VSS		VSS	BD23
AL40	VSS		VSS	BD27
AL43	VSS		VSS	BD32
AL47	VSS		VSS	BD36
AL61	VSS		VSS	BD40
AM4	VSS		VSS	BD44
AM13	VSS		VSS	BD48
AM20	VSS		VSS	BD52
AM22	VSS		VSS	BD56
AM26	VSS		VSS	BE5
AM30	VSS		VSS	BG9

SYNC MASTER=J30_MLB
SYNC DATE=07/14/2013

PAGE TITLE
CPU GROUNDS

Apple Inc.

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REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 14 OF 80

All INTEL recommendations from Intel doc #458544 Chief River Platform Power Design Guide v0p9

CPU VCORE DECOUPLING

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

43 13 10 8 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1604 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1606 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1607 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1608 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1609 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1610 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1612 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1613 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1615 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1617 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1623 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1624 2.2UF 20% 6.3V CERM 402-2

CRITICAL C1625 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1627 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1628 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1631 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1632 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1635 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1637 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1638 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1639 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1640 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1641 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1642 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1643 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1644 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1645 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1647 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1648 2.2UF 20% 6.3V CERM 402-2

CRITICAL C1650 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1651 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1652 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1653 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1654 2.2UF 20% 6.3V CERM 402-2

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1646 20UF 20% 2V X6T-CERM 0402
CRITICAL C168F 20UF 20% 2V X6T-CERM 0402
NO STUFF C16A0 20UF 20% 2V X6T-CERM 0402

CRITICAL C1655 20UF 20% 2V X6T-CERM 0402
NO STUFF C1656 20UF 20% 2V X6T-CERM 0402
CRITICAL C1657 20UF 20% 2V X6T-CERM 0402
CRITICAL C1658 20UF 20% 2V X6T-CERM 0402
NO STUFF C1659 20UF 20% 2V X6T-CERM 0402
NO STUFF C1660 20UF 20% 2V X6T-CERM 0402
CRITICAL C1661 20UF 20% 2V X6T-CERM 0402
NO STUFF C1662 20UF 20% 2V X6T-CERM 0402
NO STUFF C1663 20UF 20% 2V X6T-CERM 0402
NO STUFF C1664 20UF 20% 2V X6T-CERM 0402
NO STUFF C1665 20UF 20% 2V X6T-CERM 0402
NO STUFF C1666 20UF 20% 2V X6T-CERM 0402
CRITICAL C166A 20UF 20% 2V X6T-CERM 0402
NO STUFF C166B 20UF 20% 2V X6T-CERM 0402
CRITICAL C166C 20UF 20% 2V X6T-CERM 0402
NO STUFF C166D 20UF 20% 2V X6T-CERM 0402
NO STUFF C166E 20UF 20% 2V X6T-CERM 0402
CRITICAL C166F 20UF 20% 2V X6T-CERM 0402
CRITICAL C165A 20UF 20% 2V X6T-CERM 0402
NO STUFF C165B 20UF 20% 2V X6T-CERM 0402
NO STUFF C1667 20UF 20% 2V X6T-CERM 0402
CRITICAL C1674 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

CRITICAL C16A1 20UF 20% 2V X6T-CERM 0402
NO STUFF C16A2 20UF 20% 2V X6T-CERM 0402
CRITICAL C16A3 20UF 20% 2V X6T-CERM 0402

NO STUFF C1675 20UF 20% 2V X6T-CERM 0402
NO STUFF C1668 20UF 20% 2V X6T-CERM 0402
CRITICAL C1669 20UF 20% 2V X6T-CERM 0402
NO STUFF C1670 20UF 20% 2V X6T-CERM 0402
CRITICAL C1671 20UF 20% 2V X6T-CERM 0402
NO STUFF C1672 20UF 20% 2V X6T-CERM 0402
NO STUFF C1673 20UF 20% 2V X6T-CERM 0402
NO STUFF C1649 20UF 20% 2V X6T-CERM 0402
NO STUFF C164A 20UF 20% 2V X6T-CERM 0402
NO STUFF C1676 20UF 20% 2V X6T-CERM 0402
CRITICAL C1677 20UF 20% 2V X6T-CERM 0402
NO STUFF C1678 20UF 20% 2V X6T-CERM 0402
CRITICAL C1679 20UF 20% 2V X6T-CERM 0402
NO STUFF C165C 20UF 20% 2V X6T-CERM 0402
NO STUFF C165D 20UF 20% 2V X6T-CERM 0402
CRITICAL C165E 20UF 20% 2V X6T-CERM 0402
NO STUFF C165F 20UF 20% 2V X6T-CERM 0402
NO STUFF C164E 20UF 20% 2V X6T-CERM 0402
NO STUFF C164B 20UF 20% 2V X6T-CERM 0402
NO STUFF C164C 20UF 20% 2V X6T-CERM 0402
CRITICAL C164D 20UF 20% 2V X6T-CERM 0402
CRITICAL C164F 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C1681 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C1682 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C1683 470UF-4MOHM 20% 2 0V POLY TANT D2T SM1
C168D 270UF 20% 2V TANT CASE-B2-SM
C168E 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

13 11 10 8 =PP1V05_S0_CPU_VCCIO

C1684 1UF 10% 10V X5R CERM 0402
C1685 1UF 10% 10V X5R CERM 0402
C1686 1UF 10% 10V X5R CERM 0402
C1687 1UF 10% 10V X5R CERM 0402
C1688 1UF 10% 10V X5R CERM 0402
C1689 1UF 10% 10V X5R CERM 0402
C1690 1UF 10% 10V X5R CERM 0402
C1691 1UF 10% 10V X5R CERM 0402
C1692 1UF 10% 10V X5R CERM 0402
C1693 1UF 10% 10V X5R CERM 0402
C1694 1UF 10% 10V X5R CERM 0402
C1695 1UF 10% 10V X5R CERM 0402
C1696 1UF 10% 10V X5R CERM 0402

C1697 1UF 10% 10V X5R CERM 0402
C1698 1UF 10% 10V X5R CERM 0402
C1699 1UF 10% 10V X5R CERM 0402
C169A 1UF 10% 10V X5R CERM 0402
C169B 1UF 10% 10V X5R CERM 0402
C169C 1UF 10% 10V X5R CERM 0402
C169D 1UF 10% 10V X5R CERM 0402
C169E 1UF 10% 10V X5R CERM 0402
C169F 1UF 10% 10V X5R CERM 0402
C161A 1UF 10% 10V X5R CERM 0402
C161B 1UF 10% 10V X5R CERM 0402
C161C 1UF 10% 10V X5R CERM 0402
C161D 1UF 10% 10V X5R CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM X5R 0402 1
C161F 10UF 20% 6.3V CERM X5R 0402 1
C162A 10UF 20% 6.3V CERM X5R 0402 1
C162B 10UF 20% 6.3V CERM X5R 0402 1
C162C 10UF 20% 6.3V CERM X5R 0402 1
C162D 10UF 20% 6.3V CERM X5R 0402 1
C162E 10UF 20% 6.3V CERM X5R 0402 1
C167A 10UF 20% 6.3V CERM X5R 0402 1
C167B 10UF 20% 6.3V CERM X5R 0402 1
C167C 10UF 20% 6.3V CERM X5R 0402 1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C168A 270UF 20% 2V TANT CASE-B2-SM
C168B 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0 010 1% 1/4W MF 0603 =PP1V05_S0_CPU_VCCPQE 8 13
C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

8 PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/10W MF LF 402
PP1V8_S0_CPU_VCCPLL_R 8 13
PLACE NEAR=U1000.AK61 5mm PLACE NEAR=U1000.AK61 5mm
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM
C168C 270UF 20% 2V TANT CASE-B2-SM
PLACE NEAR U1000.AK63 2.54 mm NO VIA
PLACE NEAR U1000.AK65 2.54 mm NO VIA

CPU VCCPLL Low pass filter

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Apple Inc.
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VAXG DECOUPLING

Intel recommendation (Table 7-4) for GT2 3.9mOhm LL: 11x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

43 13 10 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R CERM 0402
CRITICAL C1701 1UF 10% 10V X5R CERM 0402
CRITICAL C1702 1UF 10% 10V X5R CERM 0402
CRITICAL C1703 1UF 10% 10V X5R CERM 0402
CRITICAL C1704 1UF 10% 10V X5R CERM 0402
CRITICAL C1705 1UF 10% 10V X5R CERM 0402
CRITICAL C1706 1UF 10% 10V X5R CERM 0402
CRITICAL C1707 1UF 10% 10V X5R CERM 0402
CRITICAL C1708 1UF 10% 10V X5R CERM 0402
CRITICAL C1709 1UF 10% 10V X5R CERM 0402
CRITICAL C1710 1UF 10% 10V X5R CERM 0402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1712 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1713 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1714 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1715 10UF 20% 6.3V CERM X5R 0402 1
CRITICAL C1716 10UF 20% 6.3V CERM X5R 0402 1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 20UF 20% 2V X6T-CERM 0402
CRITICAL C1718 20UF 20% 2V X6T-CERM 0402
CRITICAL C1719 20UF 20% 2V X6T-CERM 0402
CRITICAL C1720 20UF 20% 2V X6T-CERM 0402
CRITICAL C1721 20UF 20% 2V X6T-CERM 0402
CRITICAL C1722 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1725 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1726 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1727 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1728 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1729 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C172A 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY TANT D2T SM1
C1724 470UF-4MOHM 20% 2.0V POLY TANT D2T SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Table 7-11): 10x 1uF, 8x 10uF, 1x 330uF

27 13 11 8 =PP1V5R1V35_S3_CPU_VCCDDR

PLACEMENT_NOTE (C1738-C1747):

Place on bottom side of U1000

C1738 1UF 10% 10V X5R CERM 0402
C1739 1UF 10% 10V X5R CERM 0402
C1740 1UF 10% 10V X5R CERM 0402
C1741 1UF 10% 10V X5R CERM 0402
C1742 1UF 10% 10V X5R CERM 0402
C1743 1UF 10% 10V X5R CERM 0402
C1744 1UF 10% 10V X5R CERM 0402
C1745 1UF 10% 10V X5R CERM 0402
C1746 1UF 10% 10V X5R CERM 0402
C1747 1UF 10% 10V X5R CERM 0402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM X5R 0402 1
C1749 10UF 20% 6.3V CERM X5R 0402 1
C1750 10UF 20% 6.3V CERM X5R 0402 1
C1751 10UF 20% 6.3V CERM X5R 0402 1
C1752 10UF 20% 6.3V CERM X5R 0402 1
C1753 10UF 20% 6.3V CERM X5R 0402 1
C1754 10UF 20% 6.3V CERM X5R 0402 1
C1755 10UF 20% 6.3V CERM X5R 0402 1

C1756 270UF 20% 2V TANT CASE-B2-SM
C1770 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0 0 1% 1/4W MF 0603
=PP1V5_S3_CPU_VCCDQ 8 13
C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Table 7-9): 5x 1uf, 5x 10uf, 1x 330uf

13 8 =PPVCCSA_S0_CPU

PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000

C1758 1UF 10% 10V X5R CERM 0402
C1759 1UF 10% 10V X5R CERM 0402
C1760 1UF 10% 10V X5R CERM 0402
C1761 1UF 10% 10V X5R CERM 0402
C1762 1UF 10% 10V X5R CERM 0402

C1763 10UF 20% 6.3V CERM X5R 0402 1
C1764 10UF 20% 6.3V CERM X5R 0402 1
C1765 10UF 20% 6.3V CERM X5R 0402 1
C1766 10UF 20% 6.3V CERM X5R 0402 1
C1767 10UF 20% 6.3V CERM X5R 0402 1

C1768 270UF 20% 2V TANT CASE-B2-SM
C1769 270UF 20% 2V TANT CASE-B2-SM

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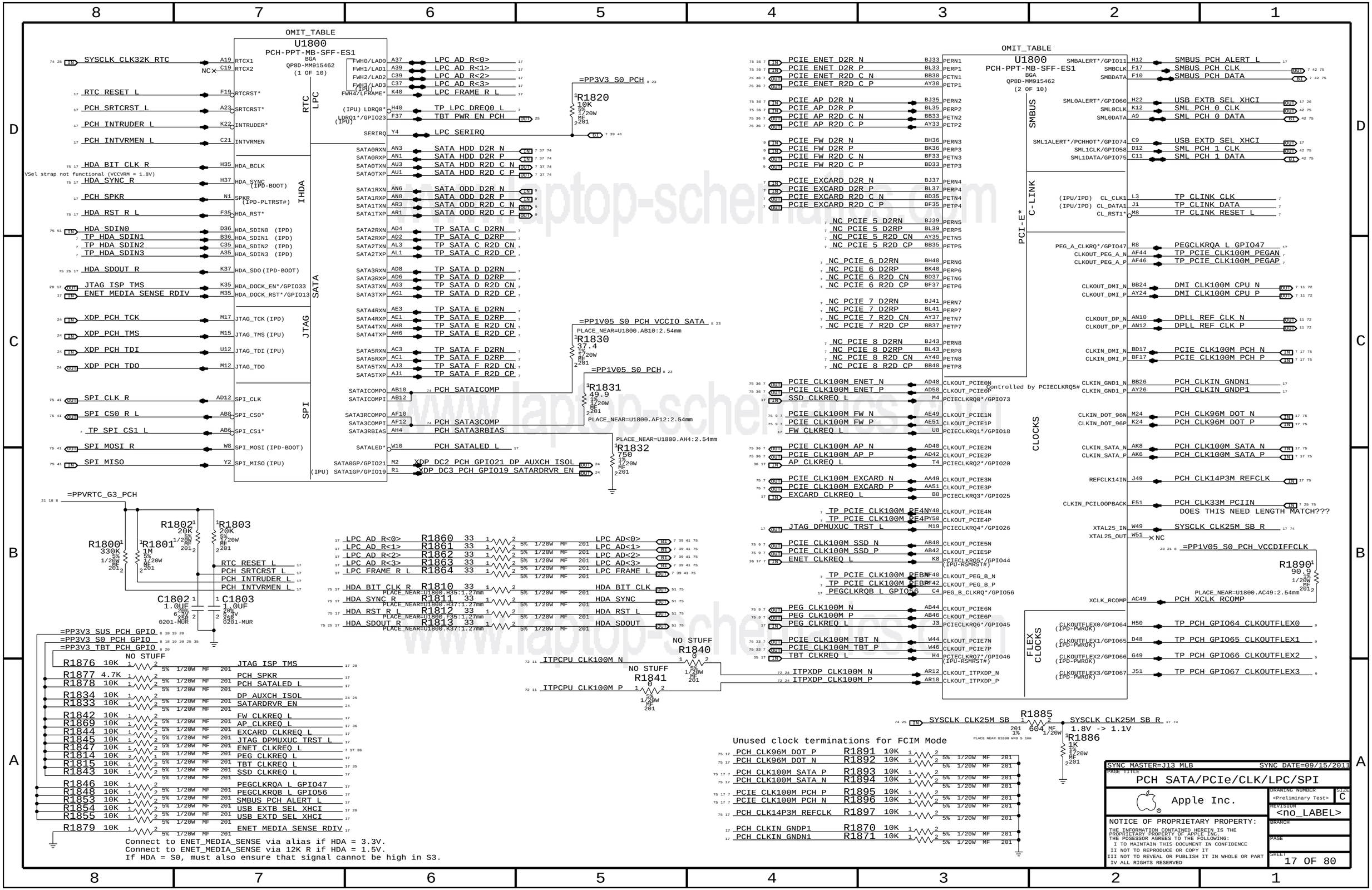

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=PP1V05_S0_PCH_VCCIO_PCIE 8
PLACE_NEAR=U1800.BF19:12.7mm
R1905 10K 5% 1/20W MF 201
R1900 49.9 1% 1/20W MF 201

OMIT_TABLE
U1800 PCH-PPT-MB-SFF-ES1
BGA QP8D-MM915462 (3 OF 10)

DMI N2S N<0> BL21 DMI0RXN
DMI N2S N<1> BL23 DMI1RXN
DMI N2S N<2> BJ19 DMI2RXN
DMI N2S N<3> BL17 DMI3RXN
DMI N2S P<0> BJ21 DMI0RXP
DMI N2S P<1> BJ23 DMI1RXP
DMI N2S P<2> BL19 DMI2RXP
DMI N2S P<3> BJ17 DMI3RXP
DMI S2N N<0> BD22 DMI0TXN
DMI S2N N<1> BB22 DMI1TXN
DMI S2N N<2> BB19 DMI2TXN
DMI S2N N<3> BB17 DMI3TXN
DMI S2N P<0> BF22 DMI0TXP
DMI S2N P<1> AY22 DMI1TXP
DMI S2N P<2> AY19 DMI2TXP
DMI S2N P<3> AY17 DMI3TXP
PCH DMI COMP BF19 DMI_ZCOMP
BD19 DMI_IRCOMP
PCH DMI2RBIAS BK20 DMI2RBIAS
PLACE_NEAR=U1800.BK20:2.54mm
R1920 750 1% 1/20W MF 201

DMI FDI

FDI_RXN0 BL13 FDI DATA N<0>
FDI_RXN1 BJ15 FDI DATA N<1>
FDI_RXN2 BD12 FDI DATA N<2>
FDI_RXN3 BJ11 FDI DATA N<3>
FDI_RXN4 AY15 FDI DATA N<4>
FDI_RXN5 AY12 FDI DATA N<5>
FDI_RXN6 BJ9 FDI DATA N<6>
FDI_RXN7 BF10 FDI DATA N<7>
FDI_RXP0 BJ13 FDI DATA P<0>
FDI_RXP1 BL15 FDI DATA P<1>
FDI_RXP2 BF12 FDI DATA P<2>
FDI_RXP3 BL11 FDI DATA P<3>
FDI_RXP4 BB15 FDI DATA P<4>
FDI_RXP5 BB12 FDI DATA P<5>
FDI_RXP6 BL9 FDI DATA P<6>
FDI_RXP7 BD10 FDI DATA P<7>
FDI_INT BB10 FDI INT
FDI_FSYNC0 BH12 FDI FSYNC<0>
FDI_FSYNC1 BK8 FDI FSYNC<1>
FDI_LSYNC0 BK12 FDI LSYNC<0>
FDI_LSYNC1 BH8 FDI LSYNC<1>

SYSTEM POWER MANAGEMENT

PCH SUSACK L F15 SUSACK*(IPU)
PM SYSRST L L1 SYS_RESET*
PM PCH SYS PWROK M10 SYS_PWROK
PM PCH PWROK M22 PWROK
PM PCH APWROK G3 APWROK
PM MEM PWRGD B12 DRAMPWROK
PM RSMRST L B20 RSMRST*
PCH SUSWARN L C13 SUSWARN*/SUSPWRDNACK/GPIO30
PM PWRBTN L K19 PWRBTN*(IPU)
SMC ADAPTER EN H19 ACPRESENT/GPIO31 (IPD-DeepS4/S5)
PM BATLOW L H10 BATLOW*/GPIO72 (IPU)
PCH RI L F12 RI*

DSWVRMEN F22 PCH DSWVRMEN
DPWROK A21 PM DSW PWRGD
WAKE* D8 PCIE WAKE L
CLKRUN*/GPIO32 T2 PM CLKRUN L
SUS_STAT*/GPIO61 G6 LPC PWRDWN L
SUSCLK/GPIO62 D3 PM CLK32K SUSCLK R
SLP_S5*/GPIO63 F6 PM SLP S5 L
SLP_S4* K10 PM SLP S4 L
SLP_S3* D4 PM SLP S3 L
SLP_A* C7 TP PM SLP A L
SLP_SUS* A15 PM SLP SUS L
PMSYNCH BB8 PM SYNC
SLP_LAN*/GPIO29 A7 PCH GPIO29

=PPVRTC_G3_PCH 8 17 21
R1915 390K 5% 1/20W MF 201
R1909 100K 5% 1/20W MF 201

OMIT_TABLE
U1800 PCH-PPT-MB-SFF-ES1
BGA QP8D-MM915462 (4 OF 10)

LVDS IG BKL ON M44 L_BKLTEN
LVDS IG PANEL PWR M42 L_VDD_EN
LVDS IG BKL PWM L49 L_BKLTCTL
R1955 100K 5% 1/20W MF 201
L51 L_DDC_CLK
K46 L_DDC_DATA (IPD-PLTRST#)
R42 L_CTRL_CLK
M40 L_CTRL_DATA
AH42 LVD_IBG
AH40 LVD_VBG
AG51 LVD_VREFH
AG49 LVD_VREFL

LVDS DIGITAL DISPLAY INTERFACE

AK44 LVDSA_CLK*
AK46 LVDSA_CLK
AR46 LVDSA_DATA0*
AN49 LVDSA_DATA1*
AN44 LVDSA_DATA2*
AK40 LVDSA_DATA3*
AR44 LVDSA_DATA0
AN51 LVDSA_DATA1
AN46 LVDSA_DATA2
AK42 LVDSA_DATA3
AH46 LVDSB_CLK*
AH44 LVDSB_CLK
AM50 LVDSB_DATA0*
AL49 LVDSB_DATA1*
AJ51 LVDSB_DATA2*
AH50 LVDSB_DATA3*
AM48 LVDSB_DATA0
AL51 LVDSB_DATA1
AJ49 LVDSB_DATA2
AH48 LVDSB_DATA3

SDVO_TVCLKINN (IPD) AU40 TP SDVO TVCLKINN
SDVO_TVCLKINP (IPD) AU42 TP SDVO TVCLKINP
SDVO_STALLN (IPD) AR51 TP SDVO STALLN
SDVO_STALLP (IPD) AR49 TP SDVO STALLP
SDVO_INTN (IPD) AT50 TP SDVO INTN
SDVO_INTP (IPD) AT48 TP SDVO INTP
SDVO_CTRLCLK W42 DPA IG DDC CLK
SDVO_CTRLDATA (IPD-PLTRST#) R44 DPA IG DDC DATA
DDPB_AUXN AW51 DPA IG AUX CH N
DDPB_AUXP AW49 DPA IG AUX CH P
DDPB_HPD AY42 DPA IG HPD
DDPB_0N AY48 TP DP IG B MLN<0>
DDPB_0P AY50 TP DP IG B MLP<0>
DDPB_1N AY44 TP DP IG B MLN<1>
DDPB_1P AY46 TP DP IG B MLP<1>
DDPB_2N BB44 TP DP IG B MLN<2>
DDPB_2P BB46 TP DP IG B MLP<2>
DDPB_3N BA49 TP DP IG B MLN<3>
DDPB_3P BA51 TP DP IG B MLP<3>
DDPC_CTRLCLK T50 DPB IG DDC CLK
DDPC_CTRLDATA (IPD-PLTRST#) U44 DPB IG DDC DATA
DDPC_AUXN AU51 DPB IG AUX CH N
DDPC_AUXP AU49 DPB IG AUX CH P
DDPC_HPD BE46 DPB IG HPD
DDPC_0N BC49 TP DP IG C MLN<0>
DDPC_0P BC51 TP DP IG C MLP<0>
DDPC_1N BD48 TP DP IG C MLN<1>
DDPC_1P BD50 TP DP IG C MLP<1>
DDPC_2N BF46 TP DP IG C MLN<2>
DDPC_2P BF45 TP DP IG C MLP<2>
DDPC_3N BE49 TP DP IG C MLN<3>
DDPC_3P BE51 TP DP IG C MLP<3>
DDPD_CTRLCLK M48 TP DP IG D CTRL CLK
DDPD_CTRLDATA (IPD-PLTRST#) U42 TP DP IG D CTRL DATA
DDPD_AUXN AU46 TP DP IG D AUXN
DDPD_AUXP AU44 TP DP IG D AUXP
DDPD_HPD BK44 TP DP IG D HPD
DDPD_0N BG51 TP DP IG D MLN<0>
DDPD_0P BG49 TP DP IG D MLP<0>
DDPD_1N BF42 TP DP IG D MLN<1>
DDPD_1P BD42 TP DP IG D MLP<1>
DDPD_2N BJ47 TP DP IG D MLN<2>
DDPD_2P BL47 TP DP IG D MLP<2>
DDPD_3N BL45 TP DP IG D MLN<3>
DDPD_3P BJ45 TP DP IG D MLP<3>

CRT

TP CRT IG BLUE M46 CRT_BLUE
TP CRT IG GREEN R46 CRT_GREEN
TP CRT IG RED U46 CRT_RED
TP CRT IG DDC CLK R49 CRT_DDC_CLK
TP CRT IG DDC DATA N49 CRT_DDC_DATA
TP CRT IG HSYNC M50 CRT_HSYNC
TP CRT IG VSYNC N51 CRT_VSYNC
PCH DAC IREF R51 DAC_IREF
T48 CRT_IRTN
PLACE_NEAR=U1800.R51:2.54mm
R1951 1K 5% 1/20W MF 201

=PP3V3_SUS_PCH_GPIO 20 19 18 17 8
R1983 10K 5% 1/20W MF 201
R1986 0 5% 1/20W MF 201
PCH_SUSWARN_L 18
PCH_SUSACK_L 18

=PP3V3_SUS_PCH_GPIO 8 17 18 19 20
=PP3V3_S0_PCH_GPIO 8 17 19 20 25 35
=PP3V3_S5_PCH 8

R1985 1K 5% 1/20W MF 201 PM_PWRBTN_L 18 24 39
R1991 8.2K 5% 1/20W MF 201 PM_CLKRUN_L 7 18 39 41
R1982 10K 5% 1/20W MF 201 PCH_GPIO29 18
R1925 1K 5% 1/20W MF 201 PCIE_WAKE_L 7 18 36

R1924 100K 5% 1/20W MF 201 PM_SLP_S3_L 7 18 27 36 39 66
R1921 100K 5% 1/20W MF 201 PM_SLP_S4_L 7 18 27 36 38 39 66
R1922 100K 5% 1/20W MF 201 PM_SLP_S5_L 18 39 66
R1923 100K 5% 1/20W MF 201 PM_SLP_SUS_L 18 66

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011
PAGE TITLE: PCH DMI/FDI/PM/Graphics
Apple Inc.
DRAWING NUMBER: <Preliminary Test> SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 18 OF 80

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(5 OF 10)

NC	BH24	TP1		AU6	NC
NC	BK24	TP2		AU8	NC
NC	BH20	TP3		AW1	NC
NC	BK16	TP4		AW3	NC
NC	BH16	TP5		AY2	NC
NC	AN42	TP6		AY4	NC
NC	AN40	TP7		AY6	NC
NC	AR40	TP8		AY8	NC
NC	AR42	TP9		BA1	NC
NC	D20	TP10		BA3	NC
NC	M30	TP11		BB6	NC
NC	E3	TP12		BC1	NC
NC	AM4	TP13	RSVD	BC3	
NC	AT4	TP14		BD2	NC
NC	AT2	TP15		BD4	NC
NC	AD10	TP16		BE1	NC
NC	B24	TP17		BE3	NC
NC	D24	TP18		BE6	NC
NC	AD44	TP19		BF6	NC
NC	AD46	TP20		BF7	NC
NC	BJ48	TP21		BG1	NC
NC	BL7	TP22		BG3	NC
	W40	TP23		BH3	NC
NC	K30	TP24		BH4	NC
				BJ4	NC
				BJ5	NC
				BJ7	NC
				BK6	NC
				BL5	NC
NC	BH49	TP41			
NC	BB42	TP42			

7 TP_PCH_TP23

USB

74 38 7 IN	USB3_EXTA_RX_N	BJ25	USB3RN1	USBP0N	F24	USB_EXTA_N BI 38 74
9 IN	USB3_EXTC_RX_N	BJ27	USB3RN2	USBP0P	H24	USB_EXTA_P BI 38 74
74 36 7 IN	USB3_EXTB_RX_N	BJ31	USB3RN3	USBP1N	C25	USB_EXTC_N BI 9
9 IN	USB3_EXTD_RX_N	BJ29	USB3RN4	USBP1P	A25	USB_EXTC_P BI 9
74 38 7 IN	USB3_EXTA_RX_P	BL25	USB3RP1	USBP2N	C27	USB_EXTB_XHCI_N BI 26 74
9 IN	USB3_EXTC_RX_P	BL27	USB3RP2	USBP2P	A27	USB_EXTB_XHCI_P BI 26 74
74 36 7 IN	USB3_EXTB_RX_P	BL31	USB3RP3	USBP3N	H28	USB_EXTD_XHCI_N BI 26 74
9 IN	USB3_EXTD_RX_P	BL29	USB3RP4	USBP3P	F28	USB_EXTD_XHCI_P BI 26 74
74 38 7 OUT	USB3_EXTA_TX_N	BF26	USB3TN1	USBP4N	M26	TP_USB_4N 9
9 OUT	USB3_EXTC_TX_N	BB28	USB3TN2	USBP4P	K26	TP_USB_4P 9
74 36 OUT	USB3_EXTB_TX_N	BF28	USB3TN3	USBP5N	D28	TP_USB_SDN 9
9 OUT	USB3_EXTD_TX_N	BF30	USB3TN4	USBP5P	B28	TP_USB_SDP 9
74 38 OUT	USB3_EXTA_TX_P	BD26	USB3TP1	USBP6N	H26	TP_USB_WLANN 9
9 OUT	USB3_EXTC_TX_P	AY28	USB3TP2	USBP6P	F26	TP_USB_WLANP 9
74 36 OUT	USB3_EXTB_TX_P	BD28	USB3TP3	USBP7N	D32	USB_HUB_UP_N BI 26 74
9 OUT	USB3_EXTD_TX_P	BD30	USB3TP4	USBP7P	B32	USB_HUB_UP_P BI 26 74
				USBP8N	M28	USB_CAMERA_N BI 32 74
				USBP8P	K28	USB_CAMERA_P BI 32 74
				USBP9N	C29	USB_EXTB_EHCI_N BI 26 74
				USBP9P	A29	USB_EXTB_EHCI_P BI 26 74
				USBP10N	C31	USB_EXTD_EHCI_N BI 9
				USBP10P	A31	USB_EXTD_EHCI_P BI 9
				USBP11N	H33	TP_USB_BT_HSN 9
				USBP11P	F33	TP_USB_BT_HSP 9
				USBP12N	H30	TP_USB_12N 9
				USBP12P	F30	TP_USB_12P 9
				USBP13N	M33	TP_USB_13N 9
				USBP13P	K33	TP_USB_13P 9
				(IPD)		
				USBRBIAS*	C33	74 PCH_USB_RBIAS
				USBRBIAS	A33	

Ext A (XHCI/EHCI)

Ext C (XHCI/EHCI)

Ext B (XHCI)

Ext D (XHCI) (Mobiles: Trackpad)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

Ext B (EHCI)

Ext D (EHCI)

RSVD: BT (HS)

Unused

Unused

PLACE_NEAR=U1800.A33:2.54mm
1 R2070 22.6 1% 1/20W MF 201 2

OC0*/GPIO59	C17	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	IN	19 24
OC1*/GPIO40	A17	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	IN	19 24
OC2*/GPIO41	A13	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	IN	19 24
OC3*/GPIO42	D16	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	IN	19 24
OC4*/GPIO43	A11	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L	IN	24
OC5*/GPIO9	B16	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	IN	24
OC6*/GPIO10	C23	XDP_DB2_PCH_GPIO10_AP_PWR_EN	OUT	24
OC7*/GPIO14	H15	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	IN	19 24

PCI

	PCI_INTA_L	D49	PIRQA*		
	PCI_INTB_L	C48	PIRQB*		
	PCI_INTC_L	C47	PIRQC*		
	PCI_INTD_L	C45	PIRQD*		
19 OUT	JTAG_GMUX_TMS	G46	REQ1*/GPIO50		
19 OUT	BLC_I2C_MUX_SEL	K44	REQ2*/GPIO52		
19 OUT	USE_HDD_OOB_L	F46	REQ3*/GPIO54		
7	TP_PCH_STRP_BBS1	F42	GNT1*/GPIO51		
7	TP_PCH_STRP_ESI_L	H42	GNT2*/GPIO53		
	PCH_STRP_TOPBLK_SWP_L	D44	GNT3*/GPIO55		
			(IPU-PCIERST#)		
19 IN	BLC_GPIO	A47	PIRQE*/GPIO2		
55 19 IN	AUD_IP_PERIPHERAL_DET	C41	PIRQF*/GPIO3		
33 19 IN	TBT_PWR_REQ_L	F45	PIRQG*/GPIO4		
54 19 IN	AUD_I2C_INT_L	F40	PIRQH*/GPIO5		
7 TP_PCI_PME_L		H2	PME* (IPU)		
27 25 OUT	PLT_RESET_L	F7	PLTRSTB*		
75 25 OUT	LPC_CLK33M_SMC_R	G51	CLKOUT_PCI0		
25 OUT	LPC_CLK33M_LPCPLUS_R	E49	CLKOUT_PCI1		
7	TP_PCI_CLK33M_OUT2	H48	CLKOUT_PCI2		
7	TP_PCI_CLK33M_OUT3	J43	CLKOUT_PCI3		
25 OUT	PCH_CLK33M_PCIOUT	G45	CLKOUT_PCI4		
			(IPD)		

R2054 10K 1/2 5% 1/20W MF 201 — NO STUFF

35 25 20 19 18 17 8 =PP3V3_S0_PCH_GPIO

R2010	10K 1/2 5% 1/20W MF 201	PCI_INTA_L	
R2011	10K 1/2 5% 1/20W MF 201	PCI_INTB_L	
R2012	10K 1/2 5% 1/20W MF 201	PCI_INTC_L	
R2013	10K 1/2 5% 1/20W MF 201	PCI_INTD_L	

=PP3V3_SUS_PCH_GPIO 8 17 18 20
=PP3V3_S3_PCH_GPIO 8 25
=PP3V3_S0_PCH_GPIO 8 17 18 19 20 25 35

R2016	10K 1/2 5% 1/20W MF 201	JTAG_GMUX_TMS 19
R2017	10K 1/2 5% 1/20W MF 201	BLC_I2C_MUX_SEL 19
R2018	10K 1/2 5% 1/20W MF 201	USE_HDD_OOB_L 19
R2030	10K 1/2 5% 1/20W MF 201	BLC_GPIO 19
	NO STUFF Redundant to pull-up on audio page	
R2014	10K 1/2 5% 1/20W MF 201	AUD_IP_PERIPHERAL_DET 19 55
R2031	10K 1/2 5% 1/20W MF 201	TBT_PWR_REQ_L 19 33
	NO STUFF Redundant to pull-up on audio page	
R2033	10K 1/2 5% 1/20W MF 201	AUD_I2C_INT_L 19 54
R2069	10K 1/2 5% 1/20W MF 201	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE 19 24
R2060	10K 1/2 5% 1/20W MF 201	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L 19 24
R2061	10K 1/2 5% 1/20W MF 201	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L 19 24
R2062	10K 1/2 5% 1/20W MF 201	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L 19 24
R2068	10K 1/2 5% 1/20W MF 201	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L 19 24
R2067	10K 2/1 5% 1/20W MF 201	AP_PWR_EN 24 36 66

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH PCI/USB/TP/RSVD

Apple Inc.

DRAWING NUMBER <Preliminary Test> SIZE C
REVISION <no_LABEL>
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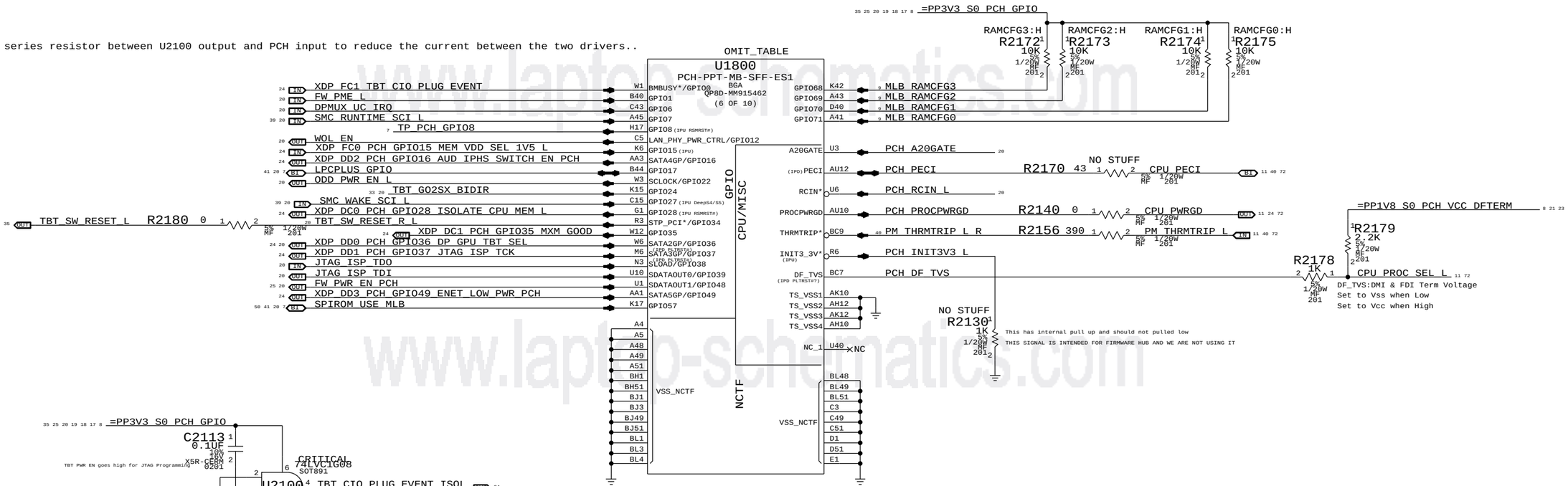
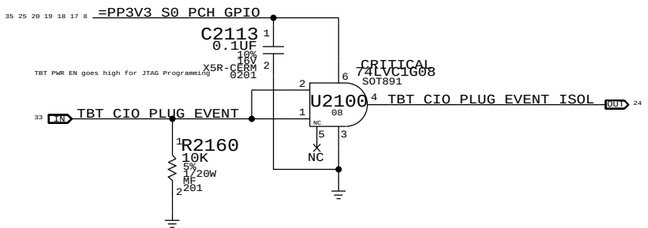
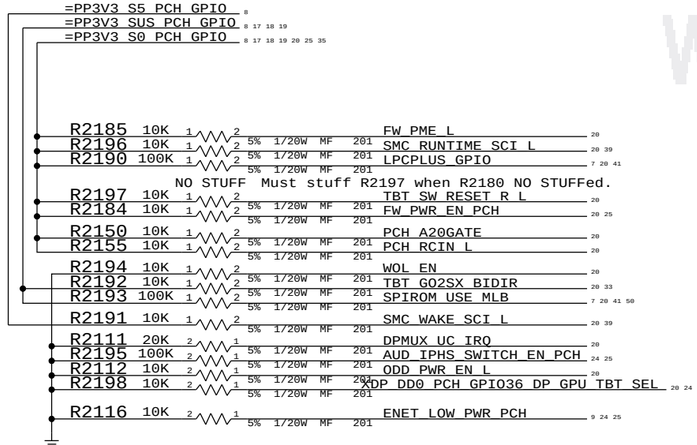
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..

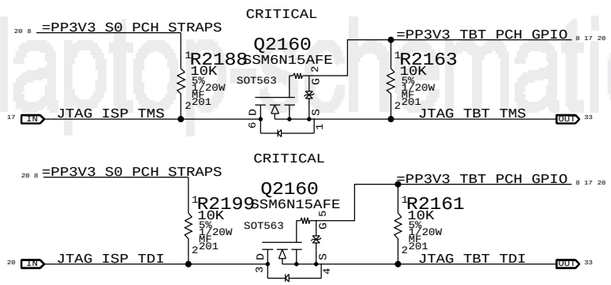


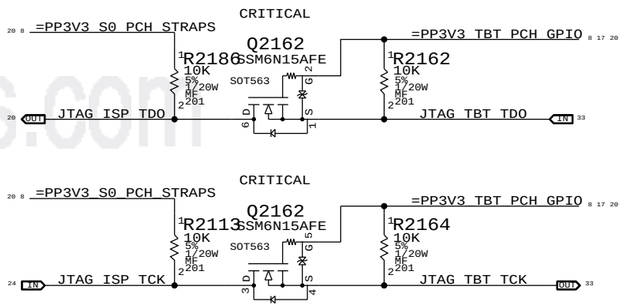




JTAG Isolation due to glitch in and out of sleep

NOTE TCK from PCH is Push Pull CMOS
NOTE TMS/TDI from PCH is Open Drain
NOTE TDO from CR is Push Pull CMOS





SYNC MASTER=J13 MLB	SYNC DATE=09/15/2011
PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER <Preliminary Test> SIZE C
	REVISION <no_LABEL>
	BRANCH
	PAGE
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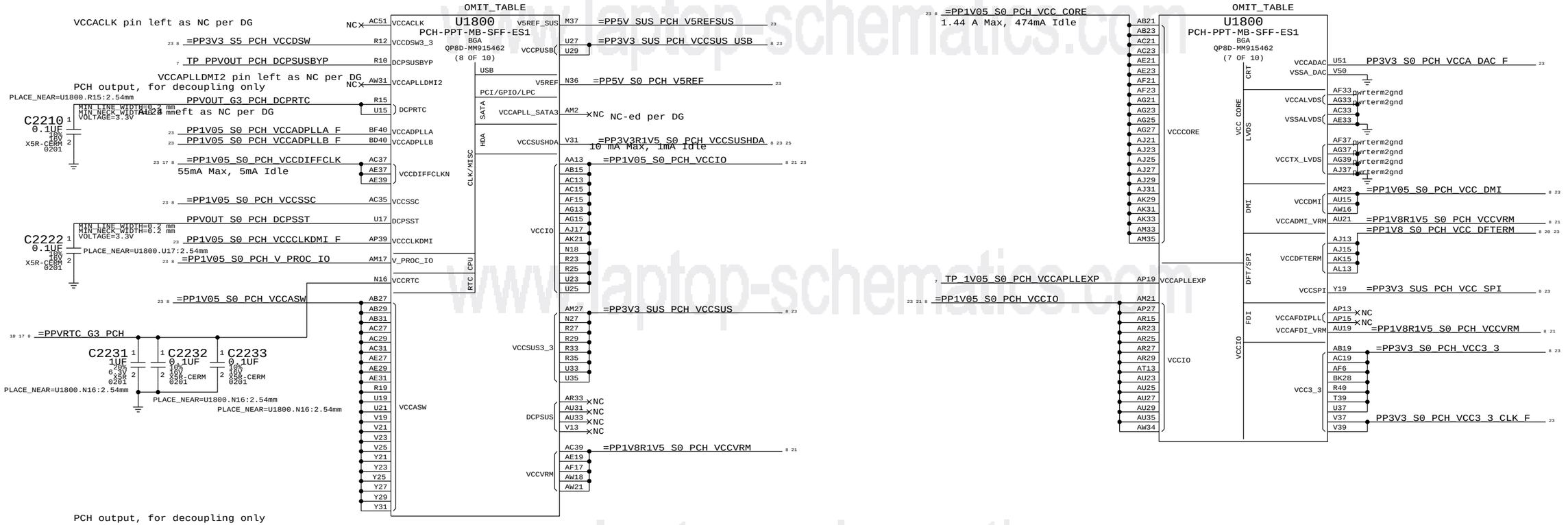

SYNC MASTER=J13_MLB SYNC DATE=09/15/2011

PAGE TITLE: PCH POWER

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(9 OF 10)

AA7			AP2
AA9			AP4
AA11			AP7
AA39			AP9
AA41			AP11
AA43			AP17
AA45			AP21
AB2			AP23
AB4			AP25
AB17			AP29
AB25			AP31
AB33			AP33
AB35			AP35
AB37			AP37
AB48			AP41
AB50			AP43
AC7			AP45
AC9			AP48
AC11			AP50
AC17			AR6
AC25			AR8
AC41			AR17
AC43			AR19
AC45			AR21
AE7			AR31
AE9			AR35
AE11			AR37
AE13			AT7
AE15			AT9
AE17			AT11
AE25			AT39
AE35			AT41
AE41			AT43
AE43			AT45
AE45			AU17
AF2			AU37
AF4			AV2
AF8			AV4
AF19			AV48
AF25			AV50
AF27			AW7
AF29	VSS	VSS	AW9
AF31			AW11
AF35			AW13
AF48			AW23
AF50			AW25
AG7			AW27
AG9			AW29
AG11			AW36
AG17			AW39
AG19			AW41
AG29			AW43
AG31			AW45
AG35			AY10
AG41			B6
AG43			B10
AG45			B14
AH2			B18
AJ7			B22
AJ9			B26
AJ11			B30
AJ19			B34
AJ33			B38
AJ35			B42
AJ39			B46
AJ41			BA7
AJ43			BA9
AJ45			BA11
AK2			BA13
AK4			BA16
AK17			BA18
AK19			BA21
AK23			BA23
AK25			BA25
AK27			BA27
AK35			BA29
AK37			BA31
AK48			BA34
AK50			BA36
AL7			BA39
AL9			BA41
AL11			BA43
AL39			BA45
AL41			BB2
AL43			BB4
AL45			BB48
AM15			BB50
AM19			BC11
AM25			BC13
AM29			BC16
AM31			BC18
AM37			BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(10 OF 10)

BC23			G39
BC25			G41
BC27			G43
BC29			J7
BC31			J9
BC34			J11
BC36			J13
BC39			J16
BC41			J18
BC43			J21
BC45			J23
BD15			J25
BD24			J27
BE7			J29
BE9			J31
BE11			J34
BE13			J36
BE16			J39
BE18			J41
BE21			J45
BE23			K2
BE25			K4
BE27			K48
BE29			K50
BE31			L7
BE34			L9
BE36			L11
BE39			L13
BE41			L16
BE43			L18
BE45			L21
BF2			L23
BF4			L25
BF15			L27
BF24			L29
BF48			L31
BF50			L34
BH6			L36
BH10			L39
BH14	VSS	VSS	L41
BH18			L43
BH22			L45
BH26			N7
BH28			N9
BH30			N11
BH32			N13
BH34			N21
BH38			N23
BH42			N25
BH44			N29
BH46			N31
BH48			N34
BK10			N39
BK14			N41
BK18			N43
BK22			N45
BK26			P2
BK30			P4
BK32			P48
BK34			P50
BK38			R17
BK42			R21
BK46			R31
D6			R37
D10			T7
D14			T9
D18			T11
D22			T13
D26			T41
D30			T43
D34			T45
D38			U31
D42			U49
D46			V2
F2			V4
F4			V7
F48			V9
F50			V11
G7			V15
G9			V17
G11			V27
G13			V29
G16			V33
G18			V35
G21			V41
G23			V43
G25			V45
G27			V48
G29			Y15
G31			Y17
G34			Y33
G36			Y35
			Y37

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH GROUNDS

Apple Inc.

DRAWING NUMBER <Preliminary Test> SIZE C

REVISION <no_LABEL>

BRANCH

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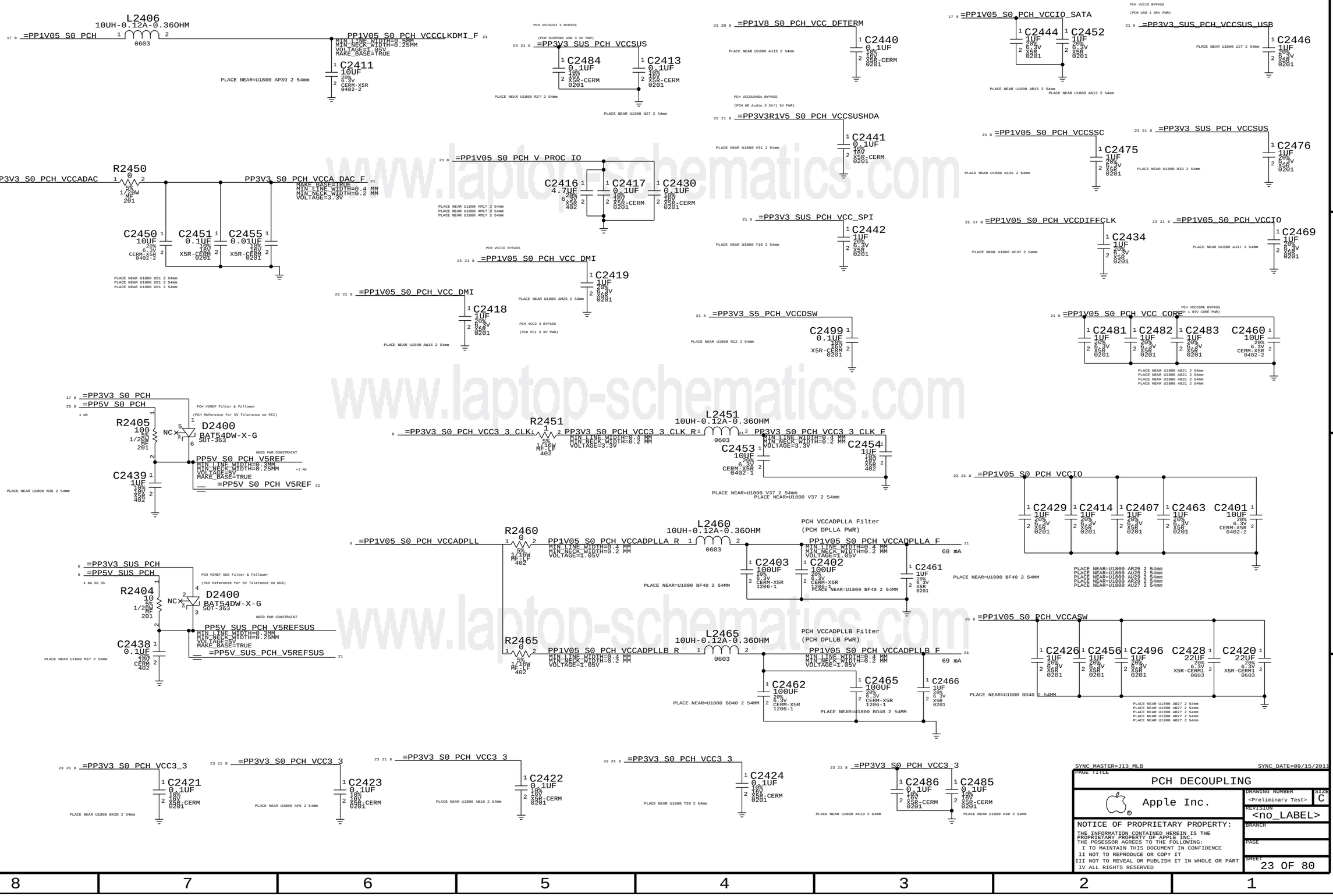

CPU Micro2-XDP

=PPVCCIO_S0_XDP

=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<16>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<17>
XDP_BPM_L<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<0>
XDP_BPM_L<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<1>
XDP_BPM_L<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<2>
XDP_BPM_L<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<3>
CPU_CFG<10>	OBSEN_B0	OBSEN_D0	CPU_CFG<8>
CPU_CFG<11>	OBSEN_B1	OBSEN_D1	CPU_CFG<9>
XDP_OBSDATA_B<0>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<4>
XDP_OBSDATA_B<1>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<5>
XDP_OBSDATA_B<2>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<6>
XDP_OBSDATA_B<3>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<7>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	XDP_CPU_CLK100M_P
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	XDP_CPU_CLK100M_N
	VCC_OBS_AB	VCC_OBS_CD	
XDP_CPU_CFG<0>	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2500 0.1UF 10% 10V X7R-CERM 0402
XDP C2501 0.1UF 10% 10V X7R-CERM 0402
518S0847

R2581 1K 1/20W 5% MF 201
R2580 1K 1/20W 5% MF 201

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0
XDP_BPM_L<5>	R2561	0
XDP_BPM_L<6>	R2562	0
XDP_BPM_L<7>	R2563	0

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0
CPU_CFG<13>	R2565	0
CPU_CFG<14>	R2566	0
CPU_CFG<15>	R2567	0

CPU_PWRGD	R2500	1K	PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L	R2502	0	PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0>	R2501	1K	PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK	R2504	330	

All: XDP, 5% 1/20W MF 201

XDP_CPU_TDO	R2510	51
XDP_CPU_TDI	R2511	51
XDP_CPU_TMS	R2512	51
XDP_CPU_TCK	R2513	51
XDP_CPU_TRST_L	R2514	51

All: XDP, 5% 1/20W MF 201

R2515	0	XDP	PLACE_NEAR=R1841.1:2.54mm
R2516	0	XDP	PLACE_NEAR=R1840.1:2.54mm
R2505	1K	XDP	PLACE_NEAR=U1000.G3:2.54mm

5% 1/20W MF 201

R2515	ITPXDP_CLK100M_P
R2516	ITPXDP_CLK100M_N
R2505	CPU_RESET_L

XDP SIGNALS

(R2520-R2537)
XDP

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0_MEM_VDD_SEL_1V5_L	R2528	33	XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L
XDP_FC1	R2529	33	XDP_FC1_TBT_CIO_PLUG_EVENT
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH

All: XDP, 5% 1/20W MF 201

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC1_TBT_CIO_PLUG_EVENT	R2574	1K	TBT_CIO_PLUG_EVENT_ISOL

5% 1/20W MF 201

Non-XDP Signals

PPDDR:1V5

XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	R2595	0

5% 1/20W MF 201

MEM_VDD_SEL_1V5_L

XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0

5% 1/20W MF 201

R2575	JTAG_ISP_TCK
R2576	AUD_IPHS_SWITCH_EN_PCH
R2577	ENET_LOW_PWR_PCH

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM1

TP_XDP_PCH_OBSFN_A<0>	OBSEN_A0	OBSEN_C0	XDP_FC0_MEM_VDD_SEL_1V5_L
TP_XDP_PCH_OBSFN_A<1>	OBSEN_A1	OBSEN_C1	XDP_FC1
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_MXM_GOOD
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2	XDP_DC2_DP_AUXCH_ISOL
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3	XDP_DC3_SATARDRVR_EN
TP_XDP_PCH_OBSFN_B<0>	OBSEN_B0	OBSEN_D0	TP_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_B<1>	OBSEN_B1	OBSEN_D1	TP_XDP_PCH_OBSFN_D<1>
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_DP_GPU_TBT_SEL
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_JTAG_ISP_TCK
XDP_DB2_AP_PWR_EN	OBSDATA_B2	OBSDATA_D2	XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	OBSDATA_D3	XDP_DD3_ENET_LOW_PWR
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	TP_XDP_PCH_HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	TP_XDP_PCH_HOOK5
	VCC_OBS_AB	VCC_OBS_CD	
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6	XDPPCH_PLTRST_L
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2580 0.1UF 10% 10V X7R-CERM 0402
XDP C2581 0.1UF 10% 10V X7R-CERM 0402
518S0847

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

ALL_SYS_PWRGD	R2584	1K	PLACE_NEAR=J2550.39:2.54mm
PM_PWRBTN_L	R2585	0	PLACE_NEAR=U4900.P17:2.54mm

XDP, 5% 1/20W MF 201

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO	R2550	51
XDP_PCH_TDI	R2551	51
XDP_PCH_TMS	R2552	51
XDP_PCH_TCK	R2556	51

All: XDP, 5% 1/20W MF 201

R2550	PLACE_NEAR=J2550.52:2.54mm
R2551	PLACE_NEAR=U1800.K5:2.54mm
R2552	PLACE_NEAR=U1800.H7:2.54mm
R2556	PLACE_NEAR=U1800.J3:2.54mm

1K series R on PCH Support Page

SYNC_MASTER=J30_MLB
SYNC_DATE=07/14/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: <Preliminary Test>
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BRANCH:
PAGE:
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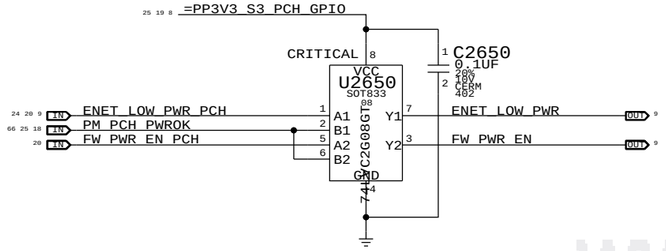
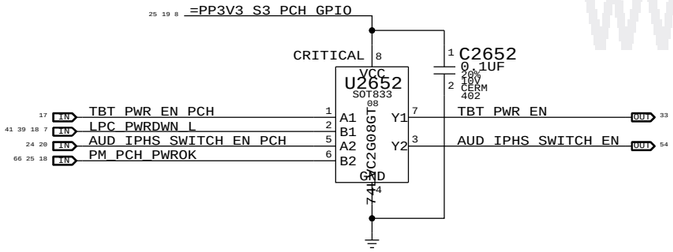
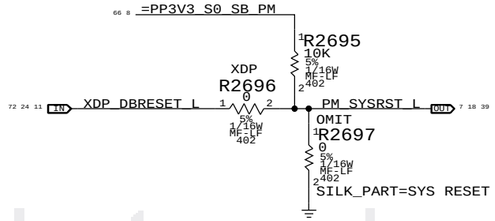
GPIO Glitch Prevention

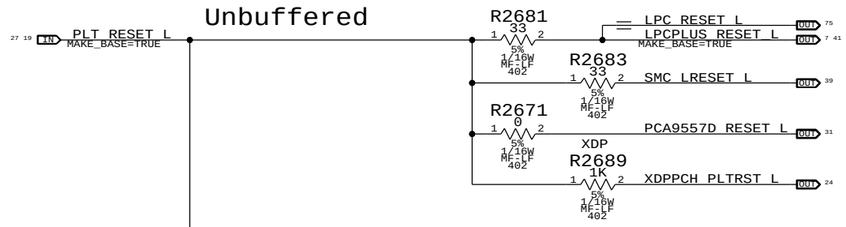




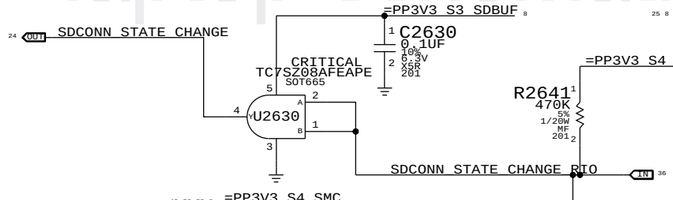
PCH Reset Button



Platform Reset Connections



SDCONN_STATE_CHANGE ISOLATION



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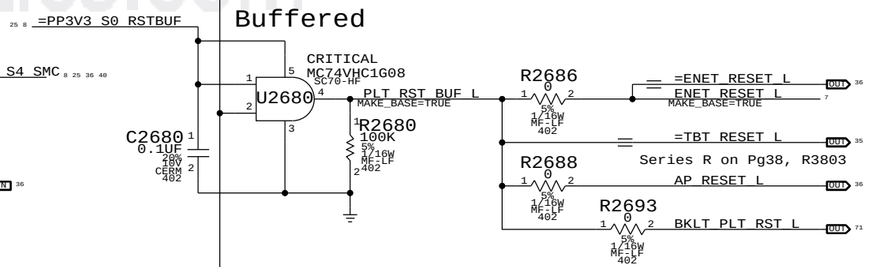
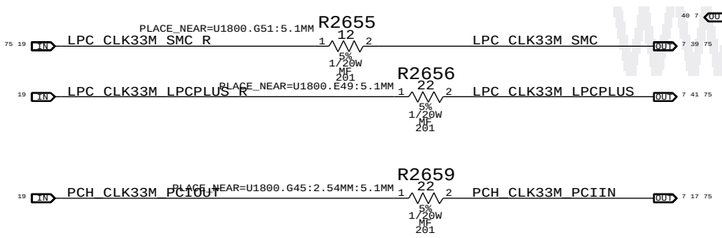
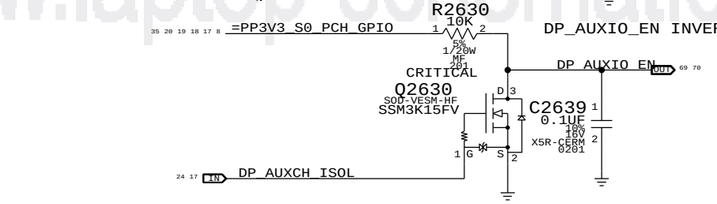
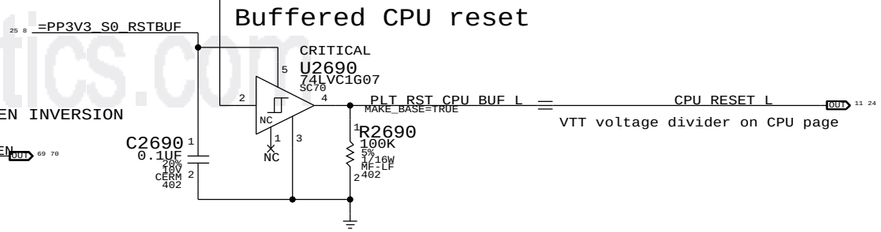


33 MHz Clock Series Termination



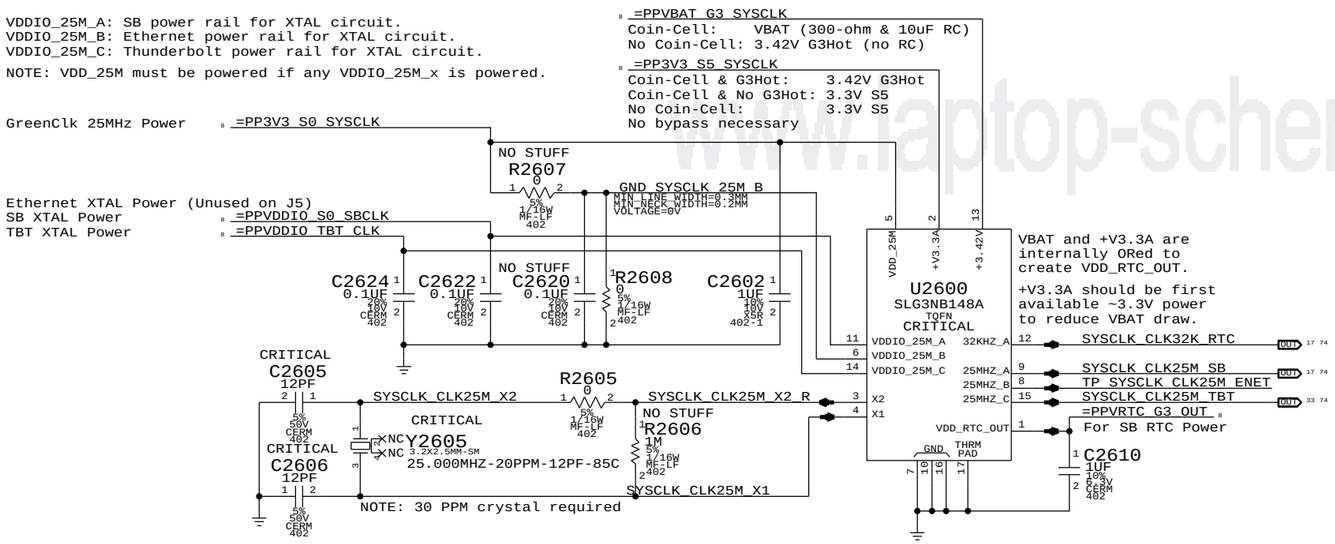




System RTC Power Source & 32kHz / 25MHz Clock Generator

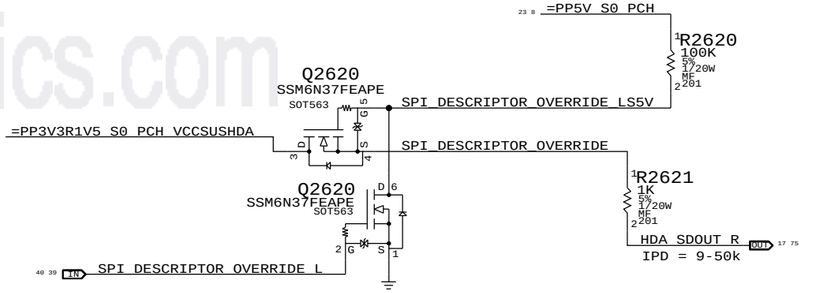
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



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PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER: <Preliminary Test> SIZE: C
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	PAGE:
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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

USB MUX FOR LS/FS INTERNAL DEVICES

NON_REM 1 : NON_REM 0 — STRAP PIN CFG

NON_REM 1	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STRAPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0485	1	XTAL 24MHZ 60PPM 16PF 2 5X2X0 55MM 90C	Y2700	CRITICAL	

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB:2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB:2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB:2512B

D1,D2 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B

=PP3V3_S3_USB_HUB — BYPASS=U27000.5::5MM — BYPASS=U2700.5::2MM

C2700 4.7UF 20% 6.3V X5R 603 — C2701 0.1UF 10% 10V X7R-CERM 0402 — C2702 0.1UF 10% 10V X7R-CERM 0402 — C2703 0.1UF 10% 10V X7R-CERM 0402

BYPASS=U2700.15::2MM — BYPASS=U2700.10::2MM — BYPASS=U2700.23::5MM — BYPASS=U2700.23::2MM

C2704 4.7UF 20% 6.3V X5R 603 — C2705 0.1UF 10% 10V X7R-CERM 0402 — C2706 0.1UF 10% 10V X7R-CERM 0402 — C2708 0.1UF 10% 10V X7R-CERM 0402

CRITICAL
Y2700 SM-2 OMIT_TABLE
24.000MHZ-16PF
BYPASS=U2700.36::2MM — BYPASS=U2650.29::2MM

CRITICAL C2709 18PF 5% 50V CERM 402 — R2700 1M 5% 1/10W MF-LF 402 — CRITICAL C2710 18PF 5% 50V CERM 402 — R2701 100 5% 1/16W MF-LF 402

HUB_NONREM1_1 — R2702 10K 5% 1/16W MF-LF 402 — R2703 10K 5% 1/16W MF-LF 402 — HUB_NONREM0_1

HUB_NONREM1_0 — R2704 10K 5% 1/16W MF-LF 402 — R2705 10K 5% 1/16W MF-LF 402 — HUB_NONREM0_0

R2706 10K 5% 1/16W MF-LF 402 — R2707 10K 5% 1/16W MF-LF 402

J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
J3X USE 197S0284 FOR Y2700 TO SAVE COST

PPUSB_HUB2_VDD1V8 MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.8V
PPUSB_HUB2_VDD1V8PLL MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.8V

C2711 0.1UF 10% 10V X7R-CERM 0402 — C2712 1UF 10% 10V X5R 402 — C2713 0.1UF 10% 10V X7R-CERM 0402 — C2714 1UF 10% 10V X5R 402

VDD33 — CRFILT — PLLFILT

SYM VER 1
U2700 USB2513B QFN OMIT_TABLE

TEST		USB_HUB_TEST	11
RESET*	26	USB_HUB_RESET_L	26
XTALIN/CLKIN		USB_HUB_XTAL1	33
XTALOUT		USB_HUB_XTAL2	32
SUSP_IND/LOCAL_PWR/NON_REM0		USB_HUB_NONREM0	28
SDA/SMBDATA/NON_REM1		USB_HUB_NONREM1	22
SCL/SMBCLK/CFG_SEL0		USB_HUB_CFG_SEL0	24
HS_IND/CFG_SEL1		USB_HUB_CFG_SEL1	25

USBDM_DN1/PRT_DIS_M1	1	USBHUB_DN1_N	BI 9
USBDP_DN1/PRT_DIS_P1	2	USBHUB_DN1_P	BI 9
USBDM_DN2/PRT_DIS_M2	3	USBHUB_DN2_N	9 26
USBDP_DN2/PRT_DIS_P2	4	USBHUB_DN2_P	9 26
USBDM_DN3/PRT_DIS_M3	6	USBHUB_DN3_N	BI 9 26
USBDP_DN3/PRT_DIS_P3	7	USBHUB_DN3_P	BI 9 26
NC	8	USBHUB_DN4_N	BI 9 26
NC	9	USBHUB_DN4_P	BI 9 26
PRTPWR1/BC_EN1*	12	TP_USB_HUB_PRTPWR1	
PRTPWR2/BC_EN2*	16	TP_USB_HUB_PRTPWR2	
PRTPWR3/BC_EN3*	18	TP_USB_HUB_PRTPWR3	
NC	20	TP_USB_HUB_PRTPWR4	
IPU OCS1*	13	TP_USB_HUB_OCS1	
IPU OCS2*	17	TP_USB_HUB_OCS2	
IPU OCS3*	19	TP_USB_HUB_OCS3	
IPU NC	21	TP_USB_HUB_OCS4	
RBIAS	35	USB_HUB_RBIAS	
VBUS_DET	27	USB_HUB_VBUS_DET	
USBDM_UP	30	USB_HUB_UP_N	BI 19 74
USBDP_UP	31	USB_HUB_UP_P	BI 19 74

CKPLUS_WAIVE=ndifpr_badterm
CRITICAL R2709 12K 1% 1/16W MF 402
PCH PORT 7 (EHCI1)
THRM_PAD — 37

BLUETOOTH FOR D1/D2 & J3X
TRACKPAD/KEYBOARD FOR D1/D2, IR FOR J3X
SMC DEBUG PORT FOR D1/D2, TPAD/KBD FOR J3X
NC FOR D1/D2, SMC DEBUG PORT FOR J3X

=PP3V3_S3_USB_HUB
NOSTUFF R2716 10K 5% 1/16W MF-LF 402 — NOSTUFF R2717 10K 5% 1/16W MF-LF 402 — NOSTUFF R2718 10K 5% 1/16W MF-LF 402 — NOSTUFF R2719 10K 5% 1/16W MF-LF 402 — NOSTUFF R2722 10K 5% 1/16W MF-LF 402 — NOSTUFF R2723 10K 5% 1/16W MF-LF 402

26 9 USBHUB_DN3_N
26 9 USBHUB_DN3_P
26 9 USBHUB_DN4_N
26 9 USBHUB_DN4_P
26 9 USBHUB_DN2_N
26 9 USBHUB_DN2_P

=PP3V3_S3_USB_HUB
R2708 10K 5% 1/16W MF-LF 402

=PP3V3_S3_USB_RESET
R2712 10K 5% 1/16W MF-LF 402
USB_HUB_RESET_L 26
C2715 0.1UF 10% 10V X7R-CERM 0402
BYPASS=U2700.26::2MM

TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R5701 & R5702, STUFF R2720 & R2721

NOSTUFF R2720 27 5% 1/16W MF-LF 402
NOSTUFF R2721 27 5% 1/16W MF-LF 402

74 19 BI USB_EXTD_XHCI_N — TO PCH XHCI — USB_TPAD_R_N BI 47 78 — TO TP/KB
74 19 BI USB_EXTD_XHCI_P — USB_TPAD_R_P BI 47 78

USB XHCI/EHCI2 PORT MUX FOR EXT B

8 =PP3V3_S3_USBMUX
C2760 0.1UF 20% 10V CERM 402

PCH PORT 9 (EHCI2)
10 74 BI USB_EXTB_EHCI_P
74 19 BI USB_EXTB_EHCI_N

PCH PORT 1 (XHCI)
10 74 BI USB_EXTB_XHCI_P
74 19 BI USB_EXTB_XHCI_N

U2760 PI3USB102ZLE TQFN CRITICAL
VCC — GND
M+ 5 — M- 4 — D+ 7 — D- 6 — OE* 8
Y+ 1 — Y- 2 — SEL 10

USB_EXTB_P BI 7 36 74 — USB_EXTB_N BI 7 36 74 — TO CONNECTOR

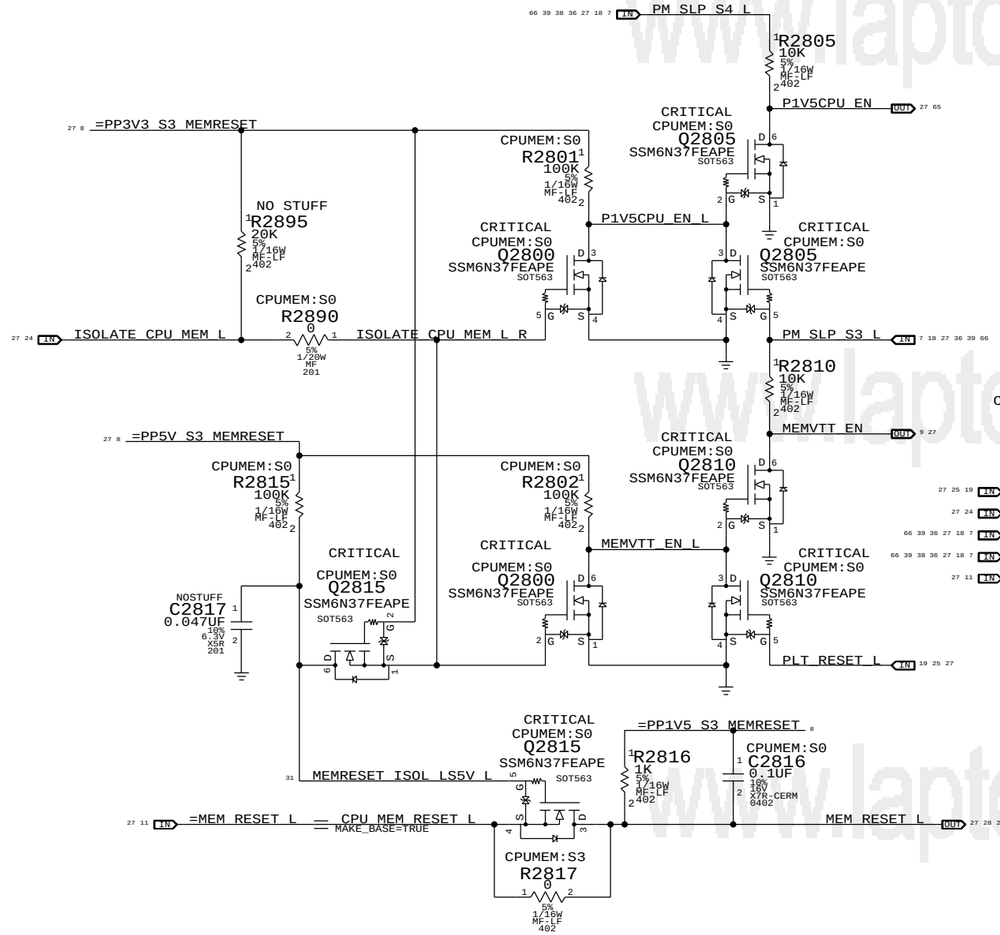
USB_EXTB_SEL_XHCI IN 17 — PCH GPIO60
PULL-UP TO 3.3V SUS ON PCH PAGE, SEL PIN IS LEAKAGE-SAFE
SEL=0 CHOOSE USB EHCI2 PORT
SEL=1 CHOOSE USB XHCI PORT

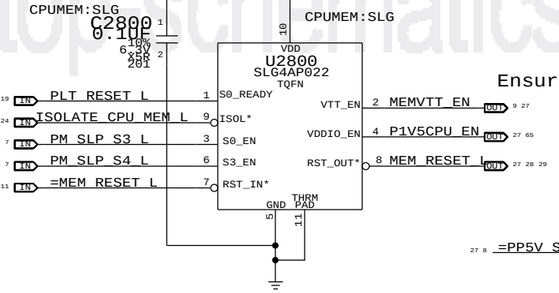
SYNC_MASTER=J5 AMD SYNC_DATE=08/17/2011
PAGE TITLE: USB HUB & MUX
Apple Inc.
DRAWING NUMBER: <Preliminary Test> SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 26 OF 80

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

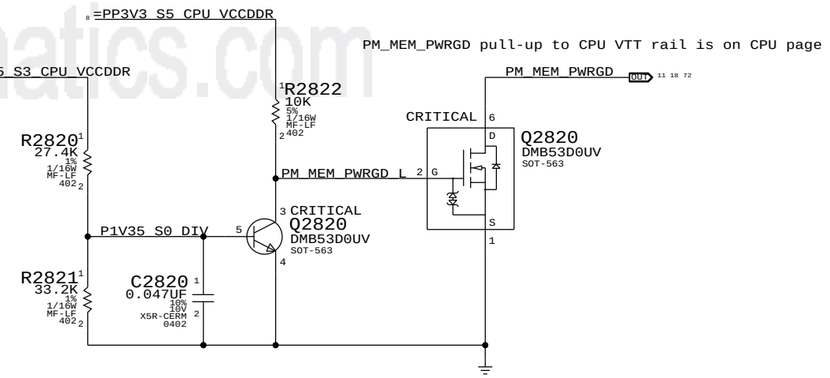
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



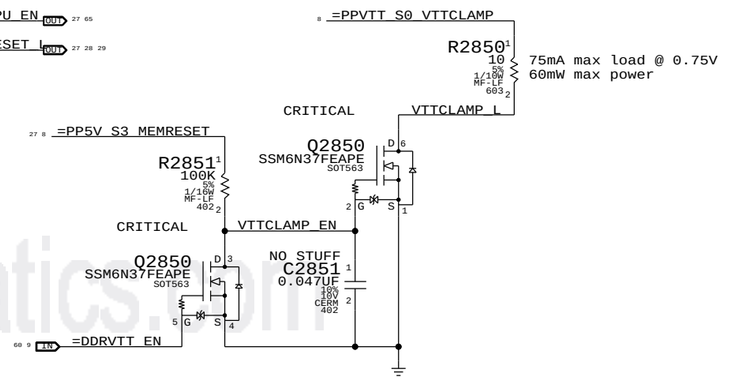


1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 27 OF 80

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ODT<1>
MEM_A_ZQ<0> MEM_A_ZQ<4>
MEM_RESET_L
MEM_A_DQ<5> MEM_A_DQ<6> MEM_A_DQ<4> MEM_A_DQ<7> MEM_A_DQ<1> MEM_A_DQ<3> MEM_A_DQ<0> MEM_A_DQ<2>
MEM_A_DQS_P<0> MEM_A_DQS_N<0>
MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
R2900 240 1% 1/20W MF 201
R2901 240 1% 1/20W MF 201
C2907 0.47UF 20% 4V CERM-X5R-1 201
C2908 0.47UF 20% 4V CERM-X5R-1 201
C2909 0.47UF 20% 4V CERM-X5R-1 201

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ODT<1>
MEM_A_ZQ<8> MEM_A_ZQ<12>
MEM_RESET_L
MEM_A_DQ<32> MEM_A_DQ<39> MEM_A_DQ<33> MEM_A_DQ<35> MEM_A_DQ<36> MEM_A_DQ<38> MEM_A_DQ<37> MEM_A_DQ<34>
MEM_A_DQS_P<4> MEM_A_DQS_N<4>
MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
R2940 240 1% 1/20W MF 201
R2941 240 1% 1/20W MF 201
C2947 0.47UF 20% 4V CERM-X5R-1 201
C2948 0.47UF 20% 4V CERM-X5R-1 201
C2949 0.47UF 20% 4V CERM-X5R-1 201

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ODT<1>
MEM_A_ZQ<1> MEM_A_ZQ<5>
MEM_RESET_L
MEM_A_DQ<9> MEM_A_DQ<10> MEM_A_DQ<13> MEM_A_DQ<15> MEM_A_DQ<8> MEM_A_DQ<12> MEM_A_DQ<14> MEM_A_DQ<11>
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MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
R2910 240 1% 1/20W MF 201
R2911 240 1% 1/20W MF 201
C2917 0.47UF 20% 4V CERM-X5R-1 201
C2918 0.47UF 20% 4V CERM-X5R-1 201
C2919 0.47UF 20% 4V CERM-X5R-1 201

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ODT<1>
MEM_A_ZQ<9> MEM_A_ZQ<13>
MEM_RESET_L
MEM_A_DQ<41> MEM_A_DQ<43> MEM_A_DQ<44> MEM_A_DQ<46> MEM_A_DQ<45> MEM_A_DQ<42> MEM_A_DQ<40> MEM_A_DQ<47>
MEM_A_DQS_P<5> MEM_A_DQS_N<5>
MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
R2950 240 1% 1/20W MF 201
R2951 240 1% 1/20W MF 201
C2957 0.47UF 20% 4V CERM-X5R-1 201
C2958 0.47UF 20% 4V CERM-X5R-1 201
C2959 0.47UF 20% 4V CERM-X5R-1 201

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
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MEM_A_ZQ<2> MEM_A_ZQ<6>
MEM_RESET_L
MEM_A_DQ<1> MEM_A_DQ<0> MEM_A_DQ<3> MEM_A_DQ<2> MEM_A_DQ<7> MEM_A_DQ<5> MEM_A_DQ<4> MEM_A_DQ<6>
MEM_A_DQS_P<0> MEM_A_DQS_N<0>
MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
R2920 240 1% 1/20W MF 201
R2921 240 1% 1/20W MF 201
C2927 0.47UF 20% 4V CERM-X5R-1 201
C2928 0.47UF 20% 4V CERM-X5R-1 201
C2929 0.47UF 20% 4V CERM-X5R-1 201

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
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MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
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MEM_A_ZQ<3> MEM_A_ZQ<7>
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MEM_A_DQ<21> MEM_A_DQ<23> MEM_A_DQ<20> MEM_A_DQ<22> MEM_A_DQ<16> MEM_A_DQ<19> MEM_A_DQ<17> MEM_A_DQ<18>
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MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
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R2931 240 1% 1/20W MF 201
C2937 0.47UF 20% 4V CERM-X5R-1 201
C2938 0.47UF 20% 4V CERM-X5R-1 201
C2939 0.47UF 20% 4V CERM-X5R-1 201

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA_A
=PP1V5R1V35_S3_MEM_A
OMIT_TABLE
U2900 FBGA-10.1X12.6-J4
U2910 FBGA-10.1X12.6-J4
U2920 FBGA-10.1X12.6-J4
U2930 FBGA-10.1X12.6-J4
U2940 FBGA-10.1X12.6-J4
U2950 FBGA-10.1X12.6-J4
U2960 FBGA-10.1X12.6-J4
U2970 FBGA-10.1X12.6-J4
512MX8-4GBIT-DDR3-1600 MT41K1G4
MEM_A_A<0> MEM_A_A<1> MEM_A_A<2> MEM_A_A<3> MEM_A_A<4> MEM_A_A<5> MEM_A_A<6> MEM_A_A<7> MEM_A_A<8> MEM_A_A<9> MEM_A_A<10> MEM_A_A<11> MEM_A_A<12> MEM_A_A<13> MEM_A_A<14> MEM_A_A<15>
MEM_A_BA<0> MEM_A_BA<1> MEM_A_BA<2>
MEM_A_RAS_L MEM_A_CAS_L MEM_A_WE_L MEM_A_ODT<0> MEM_A_ODT<1>
MEM_A_ZQ<11> MEM_A_ZQ<15>
MEM_RESET_L
MEM_A_DQ<28> MEM_A_DQ<25> MEM_A_DQ<29> MEM_A_DQ<31> MEM_A_DQ<30> MEM_A_DQ<26> MEM_A_DQ<24> MEM_A_DQ<27>
MEM_A_DQS_P<3> MEM_A_DQS_N<3>
MEM_A_CS_L<1> MEM_A_CS_L<0>
MEM_A_CKE<0> MEM_A_CKE<1>
MEM_A_CLK_P<0> MEM_A_CLK_N<0>
R2970 240 1% 1/20W MF 201
R2971 240 1% 1/20W MF 201
C2977 0.47UF 20% 4V CERM-X5R-1 201
C2978 0.47UF 20% 4V CERM-X5R-1 201
C2979 0.47UF 20% 4V CERM-X5R-1 201

=PP1V5R1V35_S3_MEM_A

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

C2900 C2901 C2910 C2911 C2920 C2921 C2930 C2931 2.2UF 20% 10V X5R-CERM 402
C2903 C2904 C2905 C2913 C2914 C2915 C2923 C2924 C2925 C2933 C2934 C2935 0.1UF 10% 6.3V X5R 201
C2940 C2941 C2950 C2951 C2960 C2961 C2970 C2971 2.2UF 20% 10V X5R-CERM 402
C2943 C2944 C2945 C2953 C2954 C2955 C2963 C2964 C2965 C2973 C2974 C2975 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=J5_MLB
SYNC_DATE=07/14/2011
PAGE_TITLE: DDR3 SDRAM Bank A (Rank 0)
Apple Inc.
DRAWING_NUMBER: <Preliminary Test>
SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 28 OF 80

=PP1V5R1V35_S3_MEM_B 8 29

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

C3107 0.47UF 20% 4V CERM-X5R-1 201 — C3108 0.47UF 20% 4V CERM-X5R-1 201 — C3109 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3100 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<0>	H8	ZQ0
MEM_B_ZQ<4>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 73 30 29 12 (27 28 29)

DQ0	B3	MEM_B_DQ<1>
DQ1	C7	MEM_B_DQ<6>
DQ2	C2	MEM_B_DQ<0>
DQ3	C8	MEM_B_DQ<7>
NF_DQ4	E3	MEM_B_DQ<4>
NF_DQ5	E8	MEM_B_DQ<3>
NF_DQ6	D2	MEM_B_DQ<5>
NF_DQ7	E7	MEM_B_DQ<2>
DQS	C3	MEM_B_DQS_P<0>
DQS*	D3	MEM_B_DQS_N<0>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3100 240 1% 1/20W MF 201 — R3101 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3117 0.47UF 20% 4V CERM-X5R-1 201 — C3118 0.47UF 20% 4V CERM-X5R-1 201 — C3119 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3110 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<1>	H8	ZQ0
MEM_B_ZQ<5>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 73 30 29 12 (27 28 29)

DQ0	B3	MEM_B_DQ<8>
DQ1	C7	MEM_B_DQ<15>
DQ2	C2	MEM_B_DQ<12>
DQ3	C8	MEM_B_DQ<10>
NF_DQ4	E3	MEM_B_DQ<13>
NF_DQ5	E8	MEM_B_DQ<11>
NF_DQ6	D2	MEM_B_DQ<9>
NF_DQ7	E7	MEM_B_DQ<14>
DQS	C3	MEM_B_DQS_P<1>
DQS*	D3	MEM_B_DQS_N<1>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3110 240 1% 1/20W MF 201 — R3111 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3127 0.47UF 20% 4V CERM-X5R-1 201 — C3128 0.47UF 20% 4V CERM-X5R-1 201 — C3129 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3120 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<2>	H8	ZQ0
MEM_B_ZQ<6>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 73 30 29 12 (27 28 29)

DQ0	B3	MEM_B_DQ<21>
DQ1	C7	MEM_B_DQ<23>
DQ2	C2	MEM_B_DQ<17>
DQ3	C8	MEM_B_DQ<18>
NF_DQ4	E3	MEM_B_DQ<20>
NF_DQ5	E8	MEM_B_DQ<22>
NF_DQ6	D2	MEM_B_DQ<16>
NF_DQ7	E7	MEM_B_DQ<19>
DQS	C3	MEM_B_DQS_P<2>
DQS*	D3	MEM_B_DQS_N<2>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3120 240 1% 1/20W MF 201 — R3121 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3137 0.47UF 20% 4V CERM-X5R-1 201 — C3138 0.47UF 20% 4V CERM-X5R-1 201 — C3139 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3130 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<3>	H8	ZQ0
MEM_B_ZQ<7>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 27 28 29

DQ0	B3	MEM_B_DQ<25>
DQ1	C7	MEM_B_DQ<30>
DQ2	C2	MEM_B_DQ<24>
DQ3	C8	MEM_B_DQ<27>
NF_DQ4	E3	MEM_B_DQ<28>
NF_DQ5	E8	MEM_B_DQ<31>
NF_DQ6	D2	MEM_B_DQ<29>
NF_DQ7	E7	MEM_B_DQ<26>
DQS	C3	MEM_B_DQS_P<3>
DQS*	D3	MEM_B_DQS_N<3>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3130 240 1% 1/20W MF 201 — R3131 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3147 0.47UF 20% 4V CERM-X5R-1 201 — C3148 0.47UF 20% 4V CERM-X5R-1 201 — C3149 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3140 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<8>	H8	ZQ0
MEM_B_ZQ<12>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 73 30 29 12 (27 28 29)

DQ0	B3	MEM_B_DQ<32>
DQ1	C7	MEM_B_DQ<39>
DQ2	C2	MEM_B_DQ<37>
DQ3	C8	MEM_B_DQ<34>
NF_DQ4	E3	MEM_B_DQ<36>
NF_DQ5	E8	MEM_B_DQ<38>
NF_DQ6	D2	MEM_B_DQ<33>
NF_DQ7	E7	MEM_B_DQ<35>
DQS	C3	MEM_B_DQS_P<4>
DQS*	D3	MEM_B_DQS_N<4>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3140 240 1% 1/20W MF 201 — R3141 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3157 0.47UF 20% 4V CERM-X5R-1 201 — C3158 0.47UF 20% 4V CERM-X5R-1 201 — C3159 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3150 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<9>	H8	ZQ0
MEM_B_ZQ<13>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 73 30 29 12 (27 28 29)

DQ0	B3	MEM_B_DQ<41>
DQ1	C7	MEM_B_DQ<46>
DQ2	C2	MEM_B_DQ<44>
DQ3	C8	MEM_B_DQ<47>
NF_DQ4	E3	MEM_B_DQ<45>
NF_DQ5	E8	MEM_B_DQ<43>
NF_DQ6	D2	MEM_B_DQ<40>
NF_DQ7	E7	MEM_B_DQ<42>
DQS	C3	MEM_B_DQS_P<5>
DQS*	D3	MEM_B_DQS_N<5>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3150 240 1% 1/20W MF 201 — R3151 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3167 0.47UF 20% 4V CERM-X5R-1 201 — C3168 0.47UF 20% 4V CERM-X5R-1 201 — C3169 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3160 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<10>	H8	ZQ0
MEM_B_ZQ<14>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 73 30 29 12 (27 28 29)

DQ0	B3	MEM_B_DQ<52>
DQ1	C7	MEM_B_DQ<50>
DQ2	C2	MEM_B_DQ<53>
DQ3	C8	MEM_B_DQ<51>
NF_DQ4	E3	MEM_B_DQ<48>
NF_DQ5	E8	MEM_B_DQ<54>
NF_DQ6	D2	MEM_B_DQ<49>
NF_DQ7	E7	MEM_B_DQ<55>
DQS	C3	MEM_B_DQS_P<6>
DQS*	D3	MEM_B_DQS_N<6>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3160 240 1% 1/20W MF 201 — R3161 240 1% 1/20W MF 201

PP0V75_S3_MEM_VREFDQ_B 72 31 29
PP0V75_S3_MEM_VREFCA_B 72 31 29

=PP1V5R1V35_S3_MEM_B 8 29

C3177 0.47UF 20% 4V CERM-X5R-1 201 — C3178 0.47UF 20% 4V CERM-X5R-1 201 — C3179 0.47UF 20% 4V CERM-X5R-1 201

VDD VDDQ

OMIT_TABLE

U3170 FBGA-10.1X12.6-J4 — 512MX8-4GBIT-DDR3-1600 MT41K1G4

MEM_B_A<0>	K3	A0
MEM_B_A<1>	L7	A1
MEM_B_A<2>	L3	A2
MEM_B_A<3>	K2	A3
MEM_B_A<4>	L8	A4
MEM_B_A<5>	L2	A5
MEM_B_A<6>	M8	A6
MEM_B_A<7>	M2	A7
MEM_B_A<8>	N8	A8
MEM_B_A<9>	M3	A9
MEM_B_A<10>	H7	A10/AP
MEM_B_A<11>	M7	A11
MEM_B_A<12>	K7	A12/BC*
MEM_B_A<13>	N3	A13
MEM_B_A<14>	N7	A14
MEM_B_A<15>	J7	A15
MEM_B_BA<0>	J2	BA0
MEM_B_BA<1>	K8	BA1
MEM_B_BA<2>	J3	BA2
MEM_B_RAS_L	F3	RAS*
MEM_B_CAS_L	G3	CAS*
MEM_B_WE_L	H3	WE*
MEM_B_ODT<0>	G1	ODT0
MEM_B_ODT<1>	F1	ODT1
MEM_B_ZQ<11>	H8	ZQ0
MEM_B_ZQ<15>	H9	ZQ1

RESET* ← N2 MEM_RESET_L 27 28 29

DQ0	B3	MEM_B_DQ<56>
DQ1	C7	MEM_B_DQ<62>
DQ2	C2	MEM_B_DQ<61>
DQ3	C8	MEM_B_DQ<59>
NF_DQ4	E3	MEM_B_DQ<60>
NF_DQ5	E8	MEM_B_DQ<58>
NF_DQ6	D2	MEM_B_DQ<57>
NF_DQ7	E7	MEM_B_DQ<63>
DQS	C3	MEM_B_DQS_P<7>
DQS*	D3	MEM_B_DQS_N<7>
DM/TDQS	B7	
NF_TDQS*	A7	NC

CS1*	H1	MEM_B_CS_L<1>
CS0*	H2	MEM_B_CS_L<0>
CKE0	G9	MEM_B_CKE<0>
CKE1	F9	MEM_B_CKE<1>
CK	F7	MEM_B_CLK_P<0>
CK*	G7	MEM_B_CLK_N<0>

NC: A3, 79, 86, 81, 82

VSS VSSQ

R3170 240 1% 1/20W MF 201 — R3171 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

=PP1V5R1V35_S3_MEM_B 8 29

C3100 2.2UF 20% 10V X5R-CERM 402
C3101 2.2UF 20% 10V X5R-CERM 402
C3110 2.2UF 20% 10V X5R-CERM 402
C3111 2.2UF 20% 10V X5R-CERM 402
C3120 2.2UF 20% 10V X5R-CERM 402
C3121 2.2UF 20% 10V X5R-CERM 402
C3130 2.2UF 20% 10V X5R-CERM 402
C3131 2.2UF 20% 10V X5R-CERM 402
C3103 0.1UF 10% 6.3V X5R 201
C3104 0.1UF 10% 6.3V X5R 201
C3105 0.1UF 10% 6.3V X5R 201
C3113 0.1UF 10% 6.3V X5R 201
C3114 0.1UF 10% 6.3V X5R 201
C3115 0.1UF 10% 6.3V X5R 201
C3123 0.1UF 10% 6.3V X5R 201
C3124 0.1UF 10% 6.3V X5R 201
C3125 0.1UF 10% 6.3V X5R 201
C3133 0.1UF 10% 6.3V X5R 201
C3134 0.1UF 10% 6.3V X5R 201
C3135 0.1UF 10% 6.3V X5R 201

C3140 2.2UF 20% 10V X5R-CERM 402
C3141 2.2UF 20% 10V X5R-CERM 402
C3150 2.2UF 20% 10V X5R-CERM 402
C3151 2.2UF 20% 10V X5R-CERM 402
C3160 2.2UF 20% 10V X5R-CERM 402
C3161 2.2UF 20% 10V X5R-CERM 402
C3170 2.2UF 20% 10V X5R-CERM 402
C3171 2.2UF 20% 10V X5R-CERM 402
C3143 0.1UF 10% 6.3V X5R 201
C3144 0.1UF 10% 6.3V X5R 201
C3145 0.1UF 10% 6.3V X5R 201
C3153 0.1UF 10% 6.3V X5R 201
C3154 0.1UF 10% 6.3V X5R 201
C3155 0.1UF 10% 6.3V X5R 201
C3163 0.1UF 10% 6.3V X5R 201
C3164 0.1UF 10% 6.3V X5R 201
C3165 0.1UF 10% 6.3V X5R 201
C3173 0.1UF 10% 6.3V X5R 201
C3174 0.1UF 10% 6.3V X5R 201
C3175 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=J5 MLB
SYNC_DATE=07/14/2011

PAGE TITLE
DDR3 SDRAM Bank B (Rank 0)

Apple Inc.

DRAWING NUMBER <Preliminary Test>
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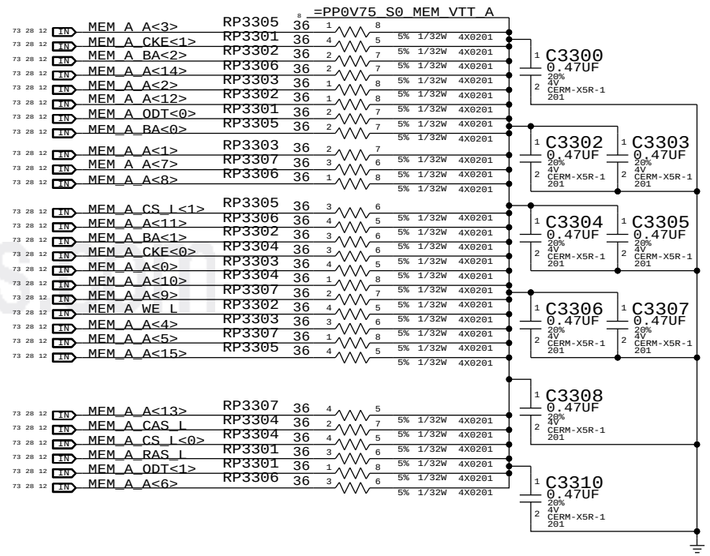
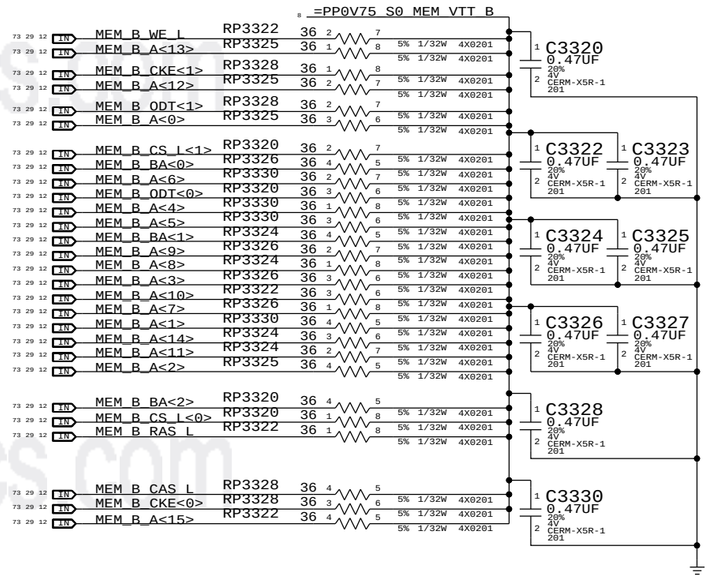
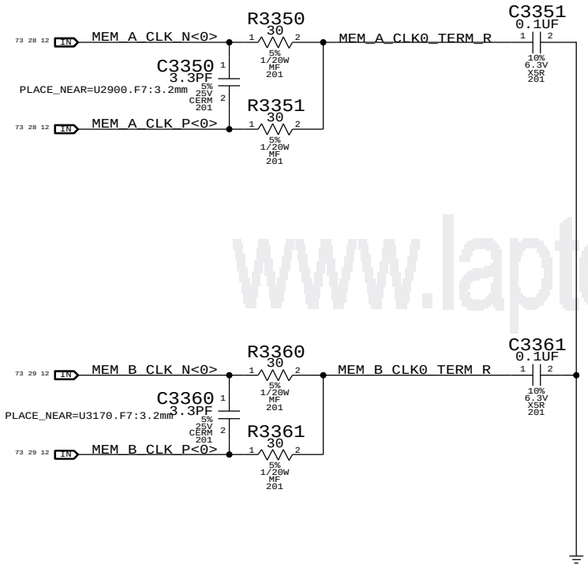
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=MASTER	SYNC DATE=MASTER
PAGE TITLE	DDR3 Termination
Apple Inc.	DRAWING NUMBER <Preliminary Test> SIZE C
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

=PP3V3_S3_VREFMRGN

OMIT R3418 SHORT NONE NONE NONE 402 — PP3V3_S3_VREFMRGN_DAC — MIN LINE WIDTH=0 3 mm, MIN NECK WIDTH=0 2 mm, VOLTAGE=3 3V

DDRVREF_DAC C3400 2.2UF 20% 6.3V CERM 402 LF

DDRVREF_DAC C3401 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3400 DAC5574 MSOP
VDD, GND
SCL ← =I2C_VREFDACS_SCL (IN)
SDA ↔ =I2C_VREFDACS_SDA (BI)
A0, A1
Addr=0x98(WR)/0x99(RD)
VOUTA → VREFMRGN_SODIMMA_DQ
VOUTB → VREFMRGN_SODIMMB_DQ
VOUTC → VREFMRGN_SODIMMS_CA
VOUTD → VREFMRGN_MEMVREG_FBVREF

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

OMIT R3419 SHORT NONE NONE NONE 402 — PP3V3_S3_VREFMRGN_CTRL — MIN LINE WIDTH=0 3 mm, MIN NECK WIDTH=0 2 mm, VOLTAGE=3 3V

DDRVREF_DAC C3402 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3401 PCA9557 QFN (OD)
VCC, GND, THRM PAD
A0, A1, A2
Addr=0x30(WR)/0x31(RD)
SCL ← =I2C_PCA9557D_SCL (IN)
SDA ↔ =I2C_PCA9557D_SDA (BI)
RESET* ← PCA9557D_RESET_L (IN)
P0 NC
P1 → VREFMRGN_DQ_SODIMMA_EN
P2 → VREFMRGN_DQ_SODIMMB_EN
P3 → VREFMRGN_CA_SODIMMA_EN
P4 → VREFMRGN_CA_SODIMMB_EN
P5 → VREFMRGN_MEMVREG_EN
P6 → VREFMRGN_FRAMEBUF_EN
P7 NC

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

=PPDDR_S3_MEMVREF

CRITICAL Q3420 SSM6N15FEAPE SOT563
MEMRESET_ISOL_LS5V_L
PPCPU_MEM_VREFDQ_A
PLACE_NEAR=Q3420.6:2mm — VREFDQ:M1_M3 — C3420 0.1UF 10% 16V X7R CERM 0402
PLACE_NEAR=Q3420.6:1mm — VREFDQ:M1_M3 — R3421 1K 1% 1/16W MF LF 402
PP0V75_S3_MEM_VREFDQ_A
VREFDQ:M1_M3 — R3422 1K 1% 1/16W MF LF 402
PLACE_NEAR=R3421.2:1mm

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

=PPDDR_S3_MEMVREF

CRITICAL Q3420 SSM6N15FEAPE SOT563
MEMRESET_ISOL_LS5V_L
PPCPU_MEM_VREFDQ_B
PLACE_NEAR=Q3420.3:2mm — VREFDQ:M1_M3 — C3440 0.1UF 10% 16V X7R CERM 0402
PLACE_NEAR=Q3420.3:1mm — VREFDQ:M1_M3 — R3441 1K 1% 1/16W MF LF 402
PP0V75_S3_MEM_VREFDQ_B
VREFDQ:M1_M3 — R3442 1K 1% 1/16W MF LF 402
PLACE_NEAR=R3441.2:1mm

=PPVTT_S3_DDR_BUF
10mA max load

DDRVREF_DAC C3403 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3402 MAX4253 UCSP
VREFMRGN_DQ_SODIMMA_BUF

VREFDQ:LDO_DAC R3403 200 1% 1/16W MF LF 402 — PLACE_NEAR=R3404.2:2.54mm
VREFDQ:LDO_DAC R3404 133 1% 1/16W MF LF 402 — PLACE_NEAR=R3403.2:1mm
PP0V75_S3_MEM_VREFDQ_A — MIN LINE WIDTH=0 3 mm, MIN NECK WIDTH=0 2 mm, VOLTAGE=0 75V

DDRVREF_DAC R3401 100K 5% 1/16W MF LF 402

CRITICAL DDRVREF_DAC U3402 MAX4253 UCSP
NC, NC
VREFMRGN_DQ_SODIMMB_BUF

VREFDQ:LDO_DAC R3405 200 1% 1/16W MF LF 402 — PLACE_NEAR=R3406.2:2.54mm
VREFDQ:LDO_DAC R3406 133 1% 1/16W MF LF 402 — PLACE_NEAR=R3405.2:1mm
PP0V75_S3_MEM_VREFDQ_B — MIN LINE WIDTH=0 3 mm, MIN NECK WIDTH=0 2 mm, VOLTAGE=0 75V

DDRVREF_DAC R3402 100K 5% 1/16W MF LF 402

DDRVREF_DAC C3404 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3403 MAX4253 UCSP
VREFMRGN_CA_SODIMMA_BUF

VREFCA:LDO_DAC R3409 200 1% 1/16W MF LF 402 — PLACE_NEAR=R3410.2:2.54mm
VREFCA:LDO_DAC R3410 133 1% 1/16W MF LF 402 — PLACE_NEAR=R3409.2:1mm
PP0V75_S3_MEM_VREFCA_A — MIN LINE WIDTH=0 3 mm, MIN NECK WIDTH=0 2 mm, VOLTAGE=0 75V

DDRVREF_DAC R3407 100K 5% 1/16W MF LF 402

CRITICAL DDRVREF_DAC U3403 MAX4253 UCSP
NC, NC
VREFMRGN_CA_SODIMMB_BUF

VREFCA:LDO_DAC R3411 200 1% 1/16W MF LF 402 — PLACE_NEAR=R3412.2:2.54mm
VREFCA:LDO_DAC R3412 133 1% 1/16W MF LF 402 — PLACE_NEAR=R3411.2:1mm
PP0V75_S3_MEM_VREFCA_B — MIN LINE WIDTH=0 3 mm, MIN NECK WIDTH=0 2 mm, VOLTAGE=0 75V

DDRVREF_DAC R3408 100K 5% 1/16W MF LF 402

DDRVREF_DAC C3405 0.1UF 20% 10V CERM 402

CRITICAL DDRVREF_DAC U3404 MAX4253 UCSP
VREFMRGN_MEMVREG_BUF

DDRVREF_DAC R3414 33.2K 1% 1/16W MF LF 402 — DDRREG_FB (OUT)
PLACE_NEAR=R7320.2:1mm

CRITICAL
VREFMRGN_FRAMEBUF_BUF

DDRVREF_DAC R3416 0 5% 1/16W MF LF 402
DDRVREF_DAC R3413 100K 5% 1/16W MF LF 402
DDRVREF_DAC U3404 MAX4253 UCSP
DDRVREF_DAC R3417 0 5% 1/16W MF LF 402
VREFMRGN_MEMVREG_FBVREF_R
VREFMRGN_FRAMEBUF_BUF_R

DDRVREF_DAC R3415 100K 5% 1/16W MF LF 402

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES MTL FILM 0 5% 0402 SM LF	R3403 R3405		VREFDQ:LDO
116S0004	2	RES MTL FILM 0 5% 0402 SM LF	R3409 R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES MTL FILM 1K 1% 0402 SM LF	R3421 R3422 R3441 R3442		VREFDQ:M1_DAC
114S0171	2	RES MTL FILM 332 1% 0402 SM LF	R3404 R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J5 MLB — SYNC DATE=07/29/2011
PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING
Apple Inc.
DRAWING NUMBER: <Preliminary Test> — SIZE: C
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BRANCH:
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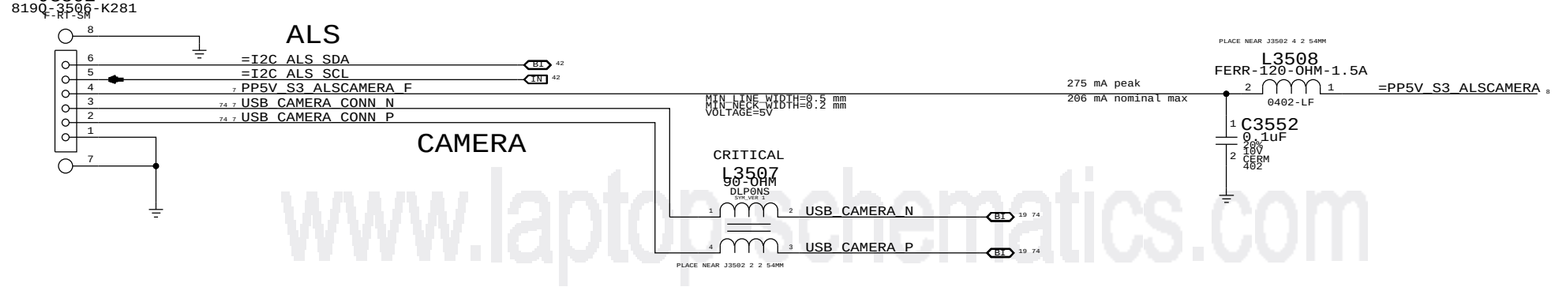
518S0767

CRITICAL
J3502
819Q-3506-K281
F-RT-SM



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER <Preliminary Test> SIZE C

REVISION <no_LABEL>

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PCIE GEN2

CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)

RECEIVE

PCIE_TBT_R2D_C_P<0>	C3600 0.1UF	PCIE_TBT_R2D_P<0> AB9
PCIE_TBT_R2D_C_N<0>	C3601 0.1UF	PCIE_TBT_R2D_N<0> AA10
PCIE_TBT_R2D_C_P<1>	C3602 0.1UF	PCIE_TBT_R2D_P<1> AA12
PCIE_TBT_R2D_C_N<1>	C3603 0.1UF	PCIE_TBT_R2D_N<1> AB13
PCIE_TBT_R2D_C_P<2>	C3604 0.1UF	PCIE_TBT_R2D_P<2> AB15
PCIE_TBT_R2D_C_N<2>	C3605 0.1UF	PCIE_TBT_R2D_N<2> AA16
PCIE_TBT_R2D_C_P<3>	C3606 0.1UF	PCIE_TBT_R2D_P<3> AA18
PCIE_TBT_R2D_C_N<3>	C3607 0.1UF	PCIE_TBT_R2D_N<3> AB19

All: 10% 16V X5R-CERM 0201, NO_TEST=TRUE

TRANSMIT

PCIE_TBT_D2R_C_P<0>	C3640 0.1UF	PCIE_TBT_D2R_P<0> AD5
PCIE_TBT_D2R_C_N<0>	C3641 0.1UF	PCIE_TBT_D2R_N<0> AD7
PCIE_TBT_D2R_C_P<1>	C3642 0.1UF	PCIE_TBT_D2R_P<1> AD9
PCIE_TBT_D2R_C_N<1>	C3643 0.1UF	PCIE_TBT_D2R_N<1> AD11
PCIE_TBT_D2R_C_P<2>	C3644 0.1UF	PCIE_TBT_D2R_P<2> AD13
PCIE_TBT_D2R_C_N<2>	C3645 0.1UF	PCIE_TBT_D2R_N<2> AD15
PCIE_TBT_D2R_C_P<3>	C3646 0.1UF	PCIE_TBT_D2R_P<3> AD17
PCIE_TBT_D2R_C_N<3>	C3647 0.1UF	PCIE_TBT_D2R_N<3> AD19

All: 10% 16V X5R-CERM 0201, NO_TEST=TRUE

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

MISC

=PP3V3_S4_TBT
R3610 47K 5% 1/20W MF 0201

=PP3V3_TBTLC_RTR
R3690 3.3K 5% 1/20W MF 0201
R3691 3.3K 5% 1/20W MF 0201
C3690 1UF 10% 6.3V CERM 402
R3692 3.3K 5% 1/20W MF 0201
R3693 3.3K 5% 1/20W MF 0201

CRITICAL
OMIT_TABLE
U3690
M95256-RMC6XG
MLP

(TBT_SPI_MOSI) (TBT_SPI_CLK) (TBT_SPI_CS_L) (TBT_SPI_MISO)
TBTROM_WP_L
TBTROM_HOLD_L

NO STUFF
C3610 0.1UF 10% 16V X5R-CERM 0201

OMIT
R3615 NOSTUFF NONE NONE NONE 0201

TBT_PCIE_RESET_L	PERST_N R6
TBT_PWR_ON_POC_RST_L	PWR_ON_POC_RSTN J2
TP_TBT_MONDC0	MONDC0 AD23
TP_TBT_MONDC1	MONDC1 AC24
TBT_MONOBSP	MONOBS_P W18
TBT_MONOBSN	MONOBS_N W16
TP_TBT_THERM_DP	THERMDA Y7
TBT_SPI_MOSI	EE_DI R4
TBT_SPI_MISO	EE_DO P5
TBT_SPI_CS_L	EE_CS_N AD3
TBT_SPI_CLK	EE_CLK W4

EEPROM

JTAG_TBT_TDI	TDI V1
JTAG_TBT_TMS	TMS AB3
JTAG_TBT_TCK	TCK AA6
JTAG_TBT_TDO	TDO R2
TBT_TEST_EN	TEST_EN N4
TBT_TEST_PWR_GOOD	TEST_PWR_GOOD AB5

JTAG/TEST PORT

R3625 0 5% 1/20W MF 0201
R3629 0 5% 1/20W MF 0201

Not used in host mode

PCIE_RST_0_N	TP_TBT_PCIE_RESET0_L N6
PCIE_RST_1_N	TP_TBT_PCIE_RESET1_L T1
PCIE_RST_2_N	TP_TBT_PCIE_RESET2_L Y5
PCIE_RST_3_N	TP_TBT_PCIE_RESET3_L U2

PCIE RESET

PCIE_CLKREQ_OD_N	=TBT_CLKREQ_L W6
EN_LC_PWR	TBT_EN_LC_PWR K5

CLOCKS

REFCLK_100_IN_P	PCIE_CLK100M_TBT_P AB21
REFCLK_100_IN_N	PCIE_CLK100M_TBT_N AD21
XTAL_25_IN	SYSCLK_CLK25M_TBT_R AA24
XTAL_25_OUT	TP_TBT_XTAL25OUT AB23
TMU_CLK_OUT	TBT_TMU_CLK_OUT AA4
TMU_CLK_IN	TBT_TMU_CLK_IN Y3

RSENSE U20 TBT_RSENSE
RBIAS W20 TBT_RBIAS
R3655 1K 1% 1/20W MF 0201
NC U4 NC

=PP3V3_TBTLC_RTR
R3698 10K 5% 1/20W MF 0201
R3695 806 1% 1/20W MF 0201 SYSCLK_CLK25M_TBT (Divides 3.3V to 1.8V)

NO STUFF
R3697 100K 5% 1/20W MF 0201
R3699 10K 5% 1/20W MF 0201
R3696 1K 5% 1/20W MF 0201

=PP3V3_TBTLC_RTR
R3680 10K 5% 1/20W MF 0201
TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR

R3681 for CYA,
allows separation
of GPIO_2/GPIO_9
if necessary.
Stuff one of R3861/2.

R3681 0 5% 1/20W MF 0201
TBT_GPIO_9
TBT_GPIO_14

NO STUFF
R3683 10K 5% 1/20W MF 0201
R3682 10K 5% 1/20W MF 0201

=PP3V3_S4_TBT
R3685 10K 5% 1/20W MF 0201
R3686 10K 5% 1/20W MF 0201
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R3688 10K 5% 1/20W MF 0201
R3687 10K 5% 1/20W MF 0201

DISPLAYPORT

SINK PORT 0

DP_TBTSNK0_ML_P<3>	DPSNK0_3_P E14
DP_TBTSNK0_ML_N<3>	DPSNK0_3_N D13
DP_TBTSNK0_ML_P<2>	DPSNK0_2_P E16
DP_TBTSNK0_ML_N<2>	DPSNK0_2_N D15
DP_TBTSNK0_ML_P<1>	DPSNK0_1_P E18
DP_TBTSNK0_ML_N<1>	DPSNK0_1_N D17
DP_TBTSNK0_ML_P<0>	DPSNK0_0_P E20
DP_TBTSNK0_ML_N<0>	DPSNK0_0_N D19
DP_TBTSNK0_AUXCH_P	DPSNK0_AUX_P A6
DP_TBTSNK0_AUXCH_N	DPSNK0_AUX_N B5
DP_TBTSNK0_HPD	DPSNK0_HPD U6

R3630 100K 5% 1/20W MF 0201

SINK PORT 1

DP_TBTSNK1_ML_P<3>	DPSNK1_3_P E6
DP_TBTSNK1_ML_N<3>	DPSNK1_3_N D5
DP_TBTSNK1_ML_P<2>	DPSNK1_2_P E8
DP_TBTSNK1_ML_N<2>	DPSNK1_2_N D7
DP_TBTSNK1_ML_P<1>	DPSNK1_1_P E10
DP_TBTSNK1_ML_N<1>	DPSNK1_1_N D9
DP_TBTSNK1_ML_P<0>	DPSNK1_0_P E12
DP_TBTSNK1_ML_N<0>	DPSNK1_0_N D11
DP_TBTSNK1_AUXCH_P	DPSNK1_AUX_P A4
DP_TBTSNK1_AUXCH_N	DPSNK1_AUX_N B3
DP_TBTSNK1_HPD	DPSNK1_HPD T5

R3631 100K 5% 1/20W MF 0201

R3632 100K 5% 1/20W MF 0201

SOURCE PORT 0

DPSRC_3_P	TP_DP_TBTSRC_ML_CP<3> A14
DPSRC_3_N	TP_DP_TBTSRC_ML_CN<3> B15
DPSRC_2_P	TP_DP_TBTSRC_ML_CP<2> A12
DPSRC_2_N	TP_DP_TBTSRC_ML_CN<2> B13
DPSRC_1_P	TP_DP_TBTSRC_ML_CP<1> A10
DPSRC_1_N	TP_DP_TBTSRC_ML_CN<1> B11
DPSRC_0_P	TP_DP_TBTSRC_ML_CP<0> A8
DPSRC_0_N	TP_DP_TBTSRC_ML_CN<0> B9
DPSRC_AUX_P	TP_DP_TBTSRC_AUXCH_CP C2
DPSRC_AUX_N	TP_DP_TBTSRC_AUXCH_CN D3
DPSRC_HPD_OD	TBT_SRC_HPD V3

GPIO_2/GO2SX	TBT_GO2SX_BIDIR Y1
(FORCE PWR) GPIO_3	TBT_PWR_EN W2
GPIO_4/WAKE_N_OD	=TBT_WAKE_L J4
GPIO_5/CIO_PLUG_EVENT	TBT_CIO_PLUG_EVENT AA2
GPIO_6/CIO_SDA_OD	=I2C_TBTRTR_SDA AB1
GPIO_7/CIO_SCL_OD	=I2C_TBTRTR_SCL AC2
GPIO_8/EN_CIO_PWR_OD*	(TBT_EN_CIO_PWR_L) P3
GPIO_9/OK2GO2SX_OD*	TBT_GPIO_9 M5
GPIO_14	TBT_GPIO_14 T3
GPIO_15	TBT_DDC_XBAR_EN_L V5

TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L (MAKE_BASE=TRUE)
WF: Verify logic level!

PORT0

PA_CIO0_TX_P/DP_SRC_0_P	TBT_A_R2D_C_P<0> G24
PA_CIO0_TX_N/DP_SRC_0_N	TBT_A_R2D_C_N<0> E24
PA_CIO0_RX_P	TBT_A_D2R_P<0> G22
PA_CIO0_RX_N	TBT_A_D2R_N<0> E22
PA_CONFIG1/CIO_0_LSEO	TBT_A_CONFIG1_BUF K1
PA_CONFIG2/CIO_0_LSOE	TBT_A_CONFIG2_RC G4

PORT1

PA_CIO1_TX_P/DP_SRC_2_P	TBT_A_R2D_C_P<1> L24
PA_CIO1_TX_N/DP_SRC_2_N	TBT_A_R2D_C_N<1> J24
PA_CIO1_RX_P	TBT_A_D2R_P<1> L22
PA_CIO1_RX_N	TBT_A_D2R_N<1> J22
PA_LSTX/CIO_1_LSEO	TBT_A_LSTX N2
PA_LSRX/CIO_1_LSOE	TBT_A_LSRX J6

PORT2

PB_CIO2_TX_P/DP_SRC_0_P	TBT_B_R2D_C_P<0> R24
PB_CIO2_TX_N/DP_SRC_0_N	TBT_B_R2D_C_N<0> N24
PB_CIO2_RX_P	TBT_B_D2R_P<0> R22
PB_CIO2_RX_N	TBT_B_D2R_N<0> N22
PB_CONFIG1/CIO_2_LSEO	TBT_B_CONFIG1_BUF P1
PB_CONFIG2/CIO_2_LSOE	TBT_B_CONFIG2_RC H5

PORT3

PB_CIO3_TX_P/DP_SRC_2_P	TBT_B_R2D_C_P<1> W24
PB_CIO3_TX_N/DP_SRC_2_N	TBT_B_R2D_C_N<1> U24
PB_CIO3_RX_P	TBT_B_D2R_P<1> W22
PB_CIO3_RX_N	TBT_B_D2R_N<1> U22
PB_LSTX/CIO_3_LSEO	TBT_B_LSTX L6
PB_LSRX/CIO_3_LSOE	TBT_B_LSRX G6

PORTS

PA_DPSRC_1_P	PB_DPSRC_1_P
PA_DPSRC_1_N	PB_DPSRC_1_N
PA_DPSRC_3_P	PB_DPSRC_3_P
PA_DPSRC_3_N	PB_DPSRC_3_N
PA_AUX_P	PB_AUX_P
PA_AUX_N	PB_AUX_N
PA_DPSRC_HPD	PB_DPSRC_HPD

GPIO_0/PA_HV_EN/BYP0	GPIO_1/PB_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1	GPIO_11/PB_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2	GPIO_13/PB_DP_PWRDN/BYP2

TBT_A_HV_EN	G2
TBT_A_CIO_SEL	M3
TBT_A_DP_PWRDN	H3
TBT_B_HV_EN	M1
TBT_B_CIO_SEL	L2
TBT_B_DP_PWRDN	L4

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C3620 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C3621 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C3622 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C3623 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C3624 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C3625 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C3626 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C3627 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C3628 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C3629 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C3630 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C3631 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C3632 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C3633 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C3634 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C3635 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C3636 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C3637 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C3638 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C3639 0.1UF	DP_TBTSNK1_AUXCH_N

All: 10% 16V X5R-CERM 0201

SYNC_MASTER=J5_MLB_KEPLER	SYNC_DATE=11/14/2011
PAGE TITLE	Thunderbolt Host (1 of 2)
Apple Inc.	DRAWING NUMBER <Preliminary Test>
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	REVISION <no_LABEL>
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	PAGE
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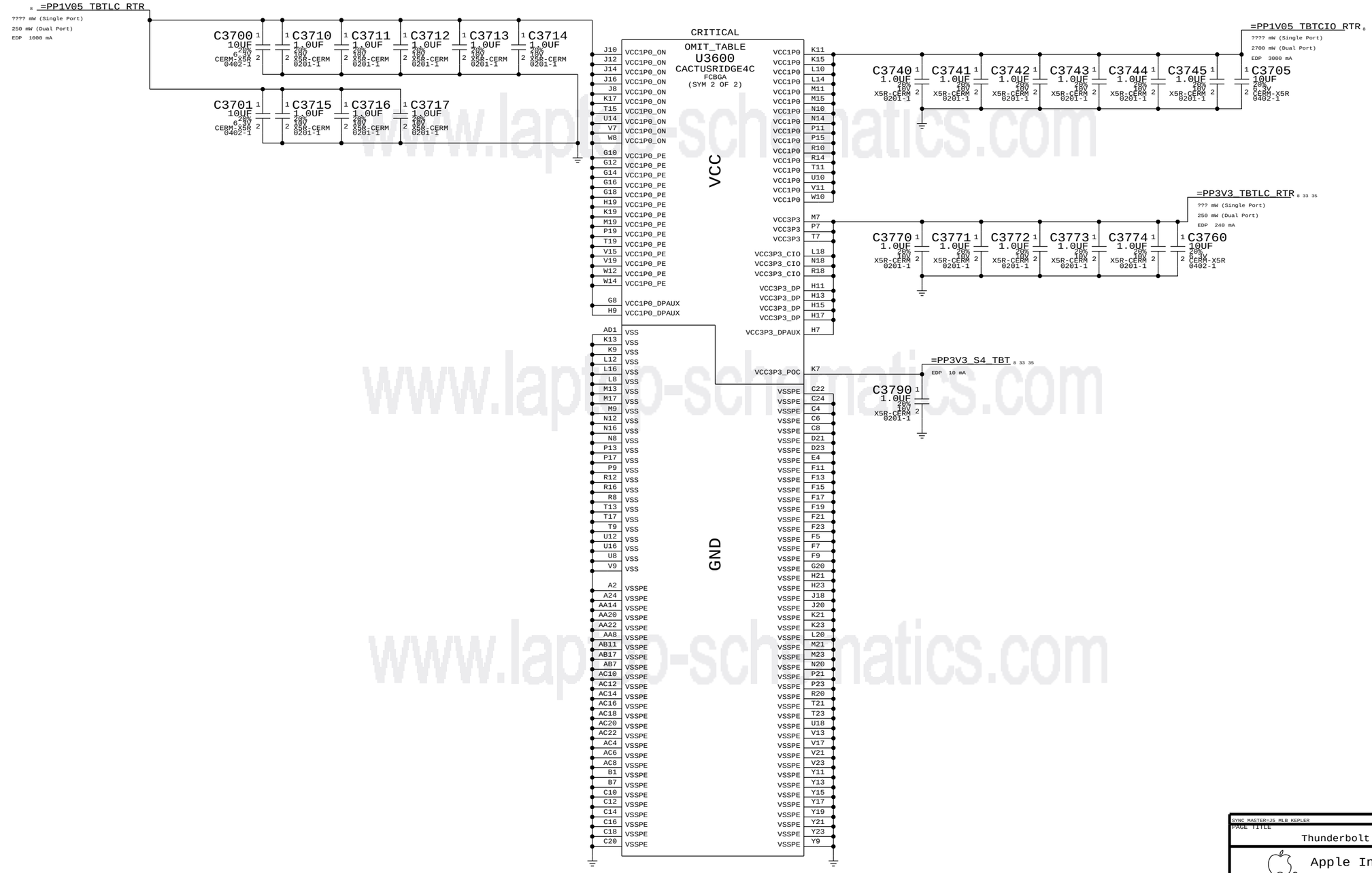

SYNC MASTER=J5 MLB KEPLER SYNC DATE=11/14/2011

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

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Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page
- =PPVIN SW TBTBST (8 13V Boost Input)
- =PP15V TBT REG (15V Boost Output)
- =PP3V3 TBT P3V3TBTFET (3 3V FET Input)
- =PP3V3 TBTLC FET (3 3V FET Output)
- =PP3V3 S0 TBTPWRCTL
- =PP1V05 TBT P1V05TBTFET (1 05V FET Input)
- =PP1V05 TBTLC FET (1 05V FET Output)

Signal aliases required by this page
- =TBT CLKREQ L
- =TBT RESET L

BOM options provided by this page
- TBTBST Y Stuffs 15V boost circuitry

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL TBTBST:Y Q3880 SI8409DB B6A

=PPVIN SW TBTBST — 8-13V Input Changes required for 2S.

PPVIN_SW_TBTBST MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
Voltage not specified here add property on another page

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 16V X5R-CERM 0201
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L
TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>
TBTBST:Y C3860 10UF 20% 25V X5R-CERM 0603
TBTBST:Y C3861 10UF 20% 25V X5R-CERM 0603

CRITICAL TBTBST:Y L3895 3.3UH-6.5A IHLP

TBTBST_BOOST MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE DIDT=TRUE

CRITICAL TBTBST:Y U3890 LT3957 QFN

TBTBST_EN_UVLO — 25 EN/UVLO
TBTBST_INTVCC — 28 INTVCC
TBTBST_VC — 30 VC
TBTBST_RT — 33 RT
TBTBST_SS — 32 SS
34 SYNC
27 VIN
8 9 20 21 38 SW
6 SNS1
3 SNS2
NC 1 2 10 35 36
31 FBX
4 23 24 37 SGND
12 13 14 15 16 17 GND

TBTBST_SNS1
TBTBST:Y R3889 0 5% 1/20W MF 201
CRITICAL TBTBST:Y D3895 PDS540XF PWRDI5
TBTBST_SNS2
XW3895 SM
PLACE NEAR=C3895 1 2 mm
TBTBST_VSNS
TBTBST:Y C3888 10PF 5% 50V CERM 402
TBTBST:Y R3895 137K 1% 1/10W MF-LF 402 <Ra>
NO STUFF TBTBST:Y C3889 100PF 5% 50V CERM 402
TBTBST:Y R3896 15.8K 1% 1/10W MF-LF 402 <Rb>

=PP15V TBT REG
Vout = 15.47V
Max Current = 2A?
Freq = 500KHz

OMIT_TABLE C3895 4.7UF 20% 25V X6S-CERM 0603
OMIT_TABLE C3897 4.7UF 20% 25V X6S-CERM 0603
OMIT_TABLE C3898 4.7UF 20% 25V X6S-CERM 0603
OMIT_TABLE C389A 4.7UF 20% 25V X6S-CERM 0603
TBTBST:Y C3896 20% 25V POLY-TANT CASE-D3L
TBTBST:Y C3899 0.001UF 10% 50V X7R 402

33UF-0.06OHM

Vout = 1.6V * (1 + Ra / Rb)

SGND shorted to GND inside package, no XW necessary.

TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3890 2.2UF 20% 16V X5R-CERM 402
TBTBST:Y C3891 2.2UF 20% 16V X5R-CERM 402
TBTBST:Y C3892 2.2UF 20% 16V X5R-CERM 402
TBTBST:Y C3887 68PF 5% 50V CERM 402
TBTBST_VC_RC
TBTBST:Y C3893 0.0033UF 10% 50V CERM 402
TBTBST:Y R3893 49.9K 1% 1/10W MF-LF 402
TBTBST:Y R3894 26.7K 1% 1/10W MF-LF 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402
GND_TBTBST_SGND MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V

TBT_A_HV_EN — 35 33 IN
TBT_B_HV_EN — 35 33 IN

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL

Q3840 SSM3K15FV SOD-VESM-HF
C3800 0.1UF 10% 16V X5R-CERM 0201
R3840 10K 5% 1/20W MF 201
TBT_EN_LC_PWR — 33 IN
TBT_EN_LC_ISOL — 64 OUT
=TBT_RESET_L — 25 IN — Platform (PCIe) Reset
TBT_CLKREQ_L — 17 OUT
Pull ups provided by SB page

CRITICAL U3800 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

=PP3V3_TBTLC_RTR — 8 33 34 35
R3807 100K 5% 1/20W MF 201
=PP1V05_TBTLC — 8
TBT_PCIE_RESET_L — OUT 33 — DLY = 60 ms +/- 20%
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L — IN 33 — MAKE_BASE=TRUE

NO STUFF R3816 0 5% 1/20W MF 201

TBT_EN_LC_ISOL_R
3.3V TBT "LC" Switch
U3810 TPS22924 CSP
A2 VIN, B2 ON, C2 GND, A1 VOUT, B1 CRITICAL, C1
=PP3V3_S0_P3V3TBTFET — 8
=PP3V3_TBTLC_FET — 8 — Max Current = 2A (85C)
R3811 0 5% 1/20W MF 201
C3810 1UF 20% 6.3V X5R 0201
C3811 1UF 20% 6.3V X5R 0201
NO STUFF
R3810 10K 5% 1/20W MF 201
R3812 0 5% 1/20W MF 201
TBT_EN_LC_RC
P1V05TBTS0_PGOOD — 64 IN

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT — 34 33 8
CRITICAL U3830 TPS3808 QFN
VDD, SENSE, CT, GND, RESET*, MR*, THRM PAD
Pull-up: R3610
TBTPOCRST_CT
C3831 0.0047UF 10% 16V X7R 402
C3830 0.1UF 10% 16V X5R 402
TBTPOCRST_MR_L
TBT_PWR_ON_POC_RST_L — OUT 33
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
C3825 330PF 10% 16V X7R-CERM 0201
Q3825 SSM6N37FEAPE SOT563
=PP3V3_S0_PCH_GPIO — 8 17 18 19 20 25
R3830 100K 5% 1/20W MF 201
TBT_SW_RESET_L — IN 20

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2 5V	18 3 mOhm Typ 24 mOhm Max

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTREG — 80 8
=PP3V3_TBTLC_RTR — 35 34 33 8
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
U3820 TPS22920 CSP
A2 VIN, B2 ON, C2 GND, A1 VOUT, B1 CRITICAL, D2
=PP1V05_TBTCIO_FET — 8 — Max Current = 4A (85C)
C3820 1UF 20% 6.3V X5R 0201
Q3825 SSM6N37FEAPE SOT563
TBT_EN_CIO_PWR_L — 33 IN

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K 5% 1/10W MF-LF 402
TBTBST:Y R3888 330K 5% 1/10W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD — IN 39 40 66

TBT_A_HV_EN — 35 33
R3850 0 5% 1/20W MF 201
TBT_A_HV_EN_RC — OUT 69
C3850 1.0UF 10% 6.3V X5R-CERM 0201 NO STUFF
NO STUFF D3850 1N4448HLP-7 DFN1006

TBT_B_HV_EN — 35 33
R3860 0 5% 1/20W MF 201
TBT_B_HV_EN_RC — OUT 70
C3865 1.0UF 10% 6.3V X5R-CERM 0201 NO STUFF
NO STUFF D3860 1N4448HLP-7 DFN1006

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP CER 4 7UF 10% 25V X6S 0603	C3895,C3897,C3898,C389A	CRITICAL	TBTBST:Y

SYNC MASTER=J5 MLB KEPLER — SYNC DATE=11/14/2011
PAGE TITLE: Thunderbolt Power Support
Apple Inc.
DRAWING NUMBER: <Preliminary Test> SIZE: C
REVISION: <no_LABEL>
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L4470,L4471,L4473,L4474		

3V S3 WLAN FET

DEBUG CURRENT SENSE RD135 connects to PP3V3_WLAN_F

AIRPORT

U4450 TPS22924 CSP — CRITICAL

Max Current = 2A (85C)

Part	TPS22924C
Type	Load Switch
R(on)	18 3 mOhm Typ
@ 2 5V	24 mOhm Max

RIO POWER CONNECTOR

CRITICAL
J4400
504050-0691
M-RT-SM

518s0862

RIO FLEX CONNECTOR

CRITICAL
J4410
DF40CG3.0-70DS-0.4V
F-ST-SM

516S1058

*NOTE: This connector is shielded 70P Hirose Receptacle.

Note: This receptacle mates with the plug with APN 998-4708.

Supervisor & CLKFREG # Isolation

Delay = 130 ms +/- 20%

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

SIGNAL_MODEL=MOJO_MUX

APN:311S0302

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: RIO CONNECTORS

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

BRANCH:

PAGE:

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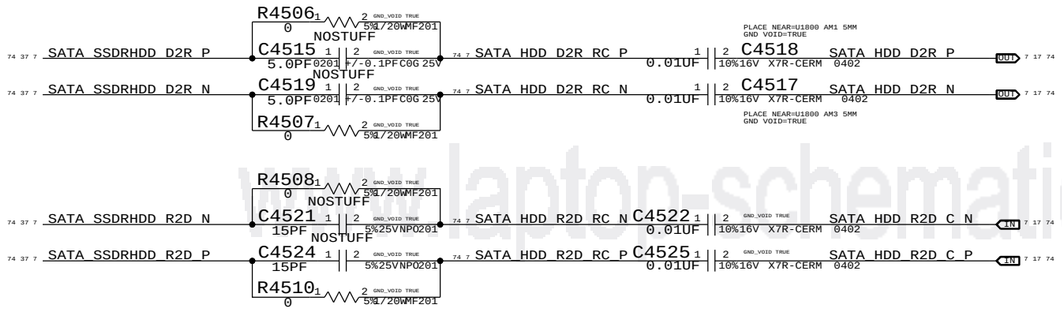
D2R Passive DeEmphasis

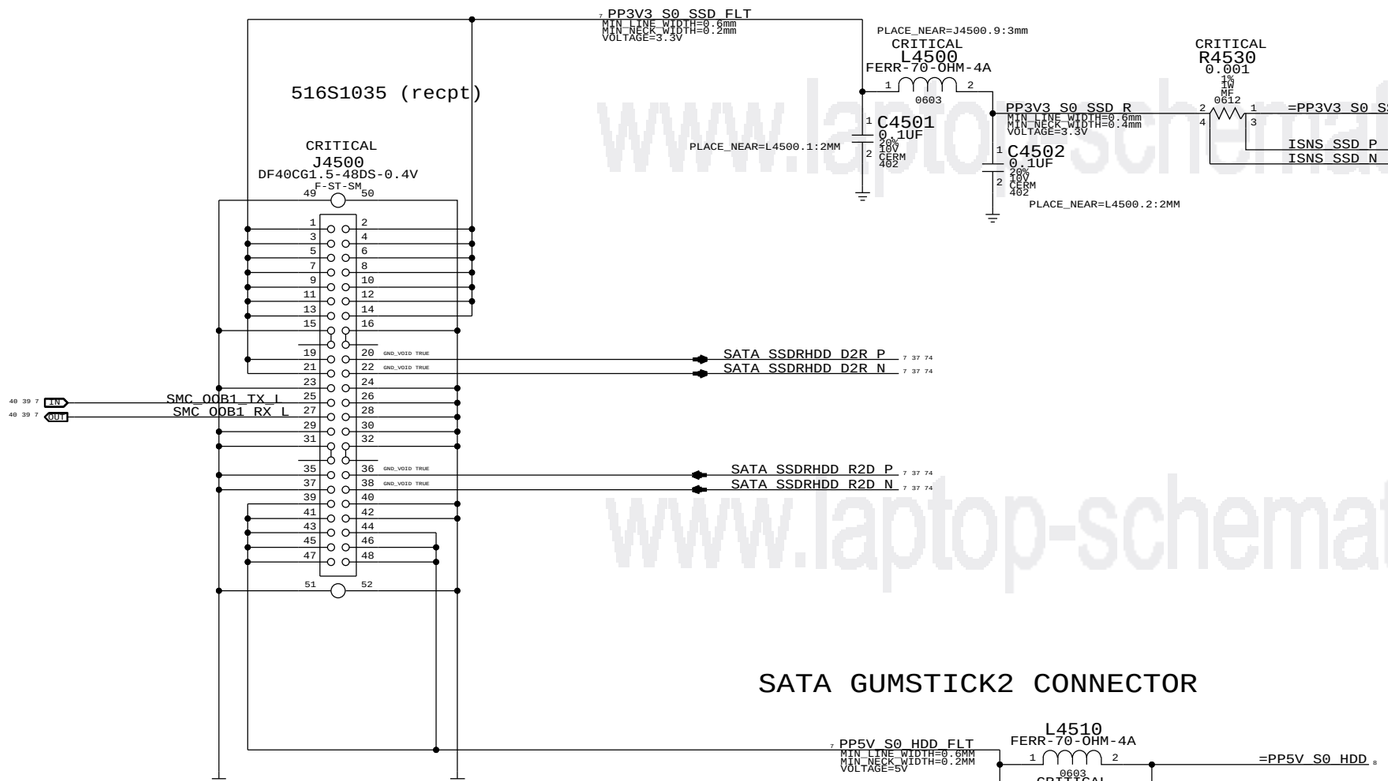
VALUE: 0.0 DB



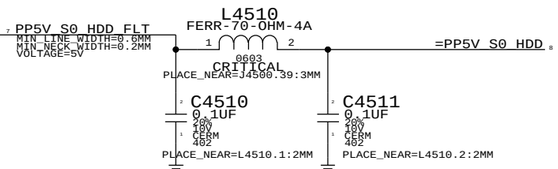
' C4518 & C4517 Placement Note:
' It is critical that these two should be near
' to U1800 pin AM1 and AM3.

R2D Passive DeEmphasis

VALUE: 0.0 DB



SATA GUMSTICK2 CONNECTOR



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: SSD/HDD Connectors

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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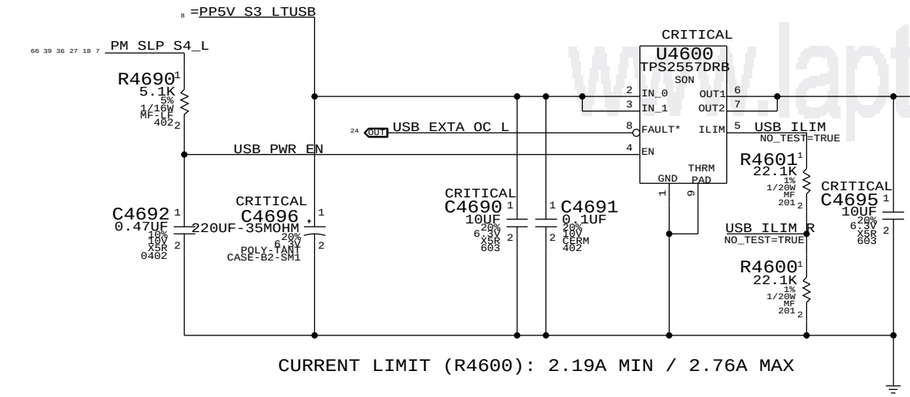
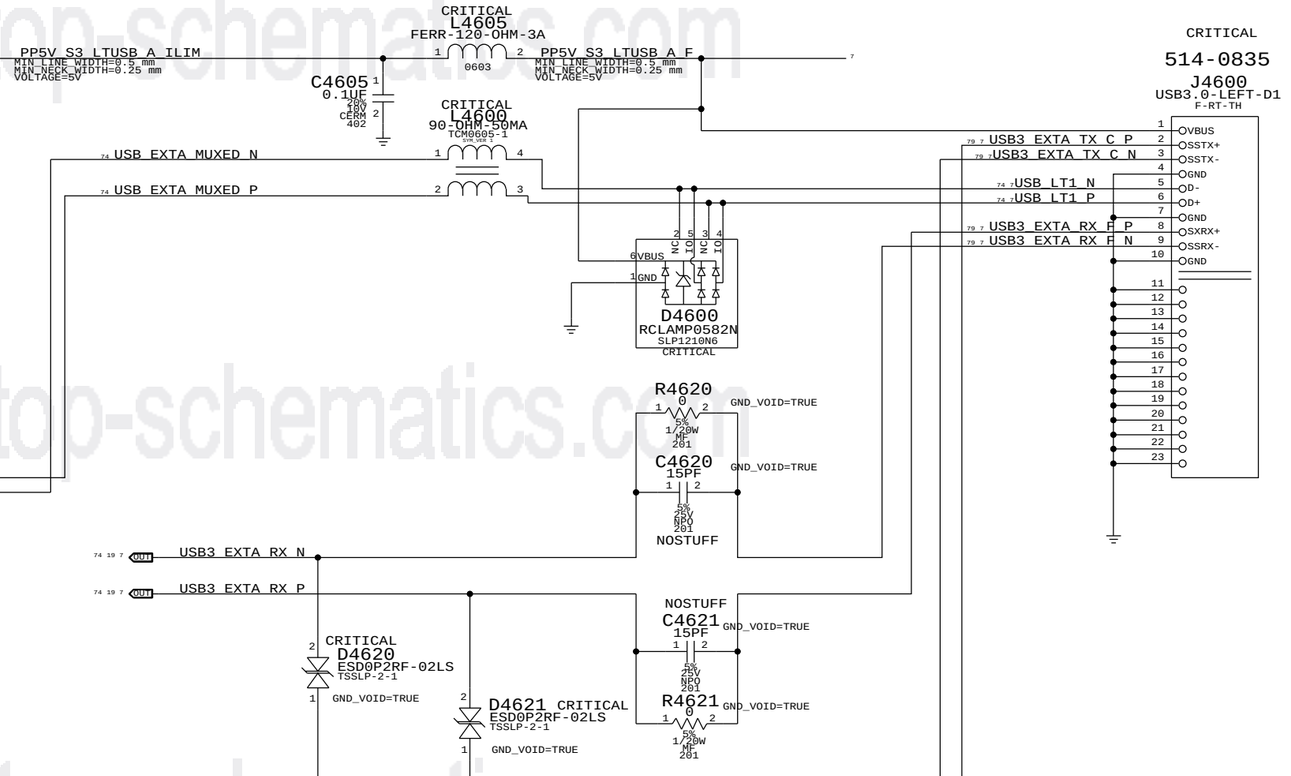
USB Port Power Switch

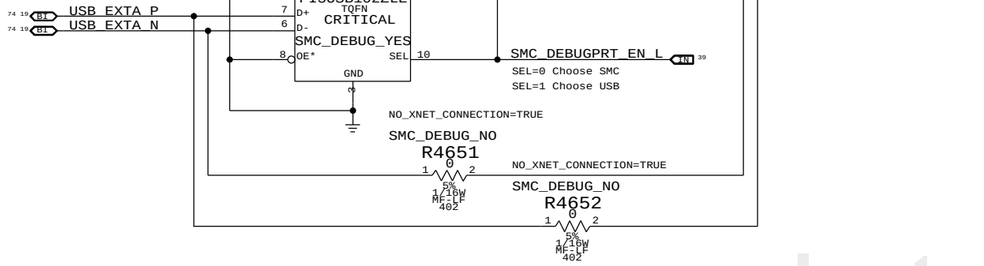


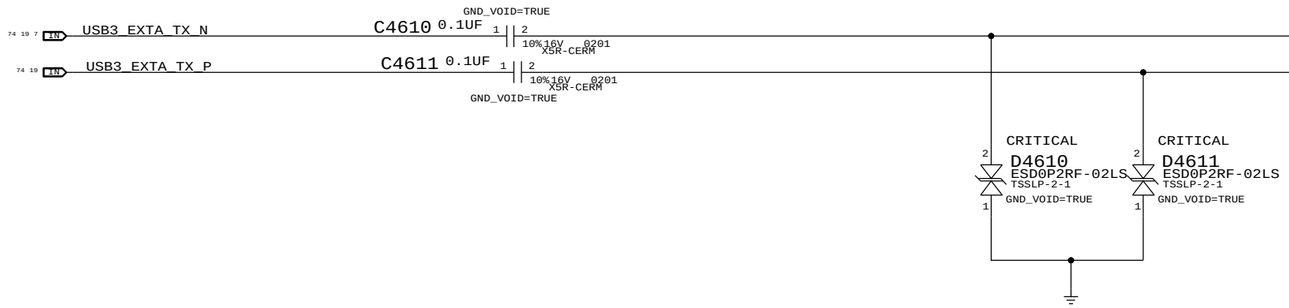
CURRENT LIMIT (R4600): 2.19A MIN / 2.76A MAX

Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=J5_AMD SYNC_DATE=08/24/2013

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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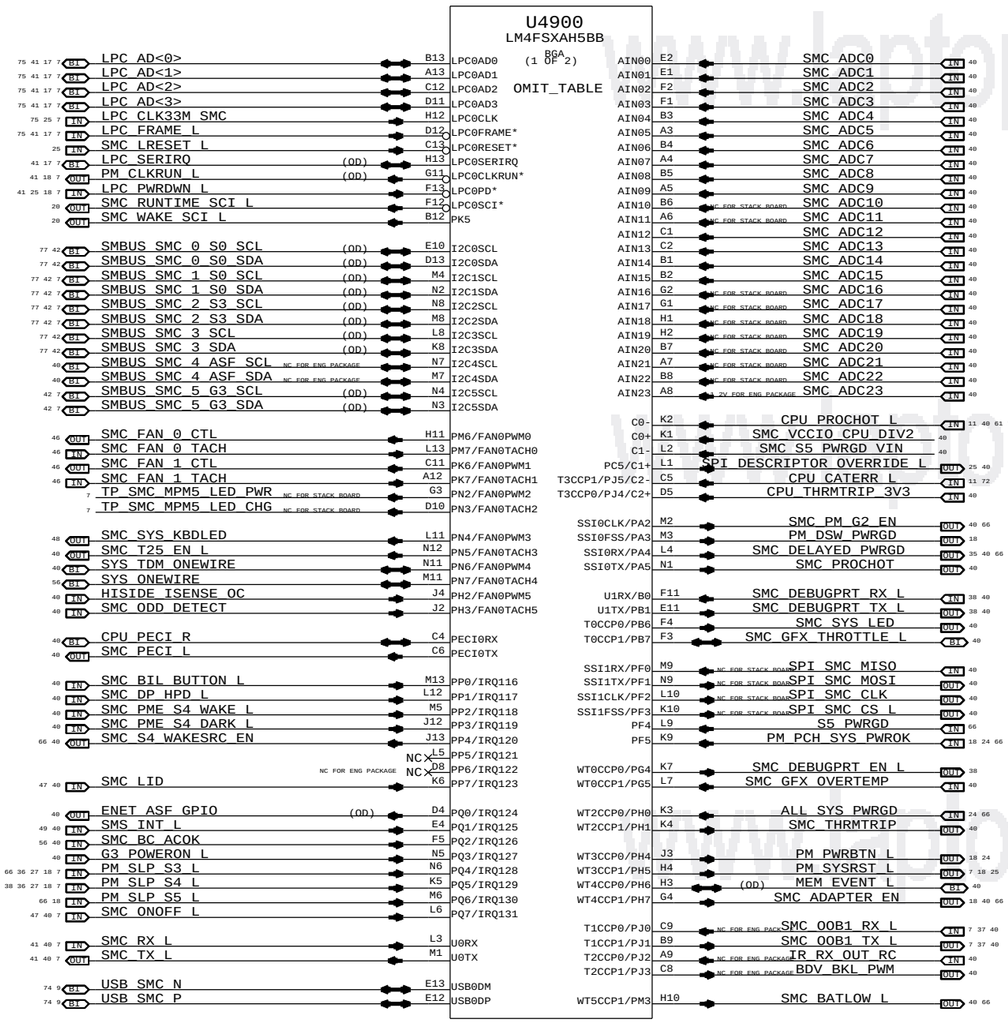
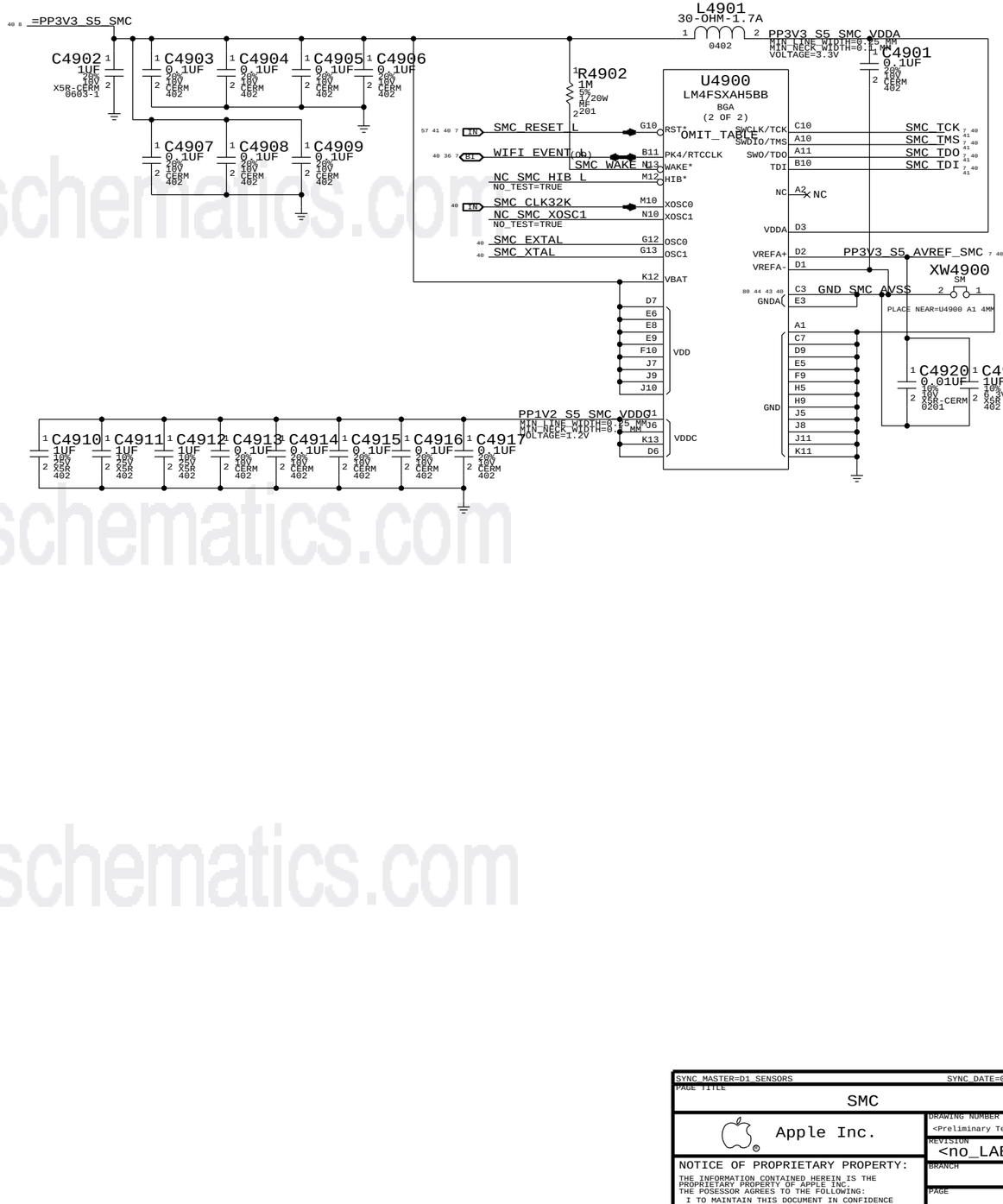
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <Preliminary Test>

SIZE: C

REVISION: <no_LABEL>

BRANCH:

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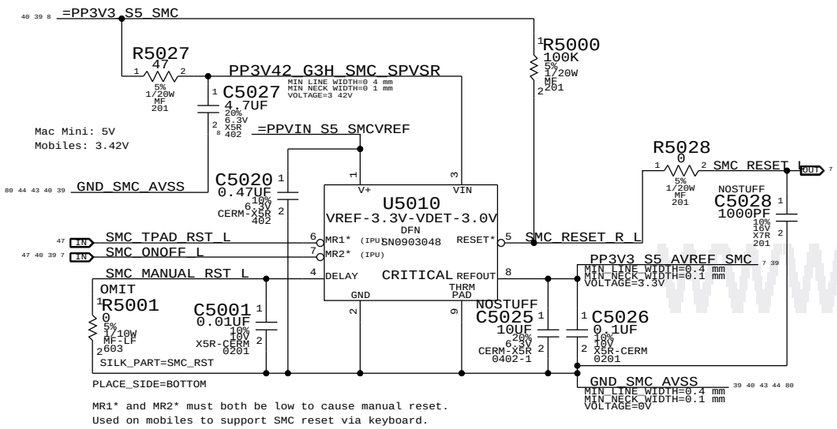
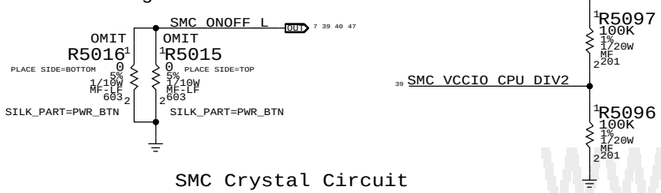
SMC Reset "Button", Supervisor & AVREF Supply



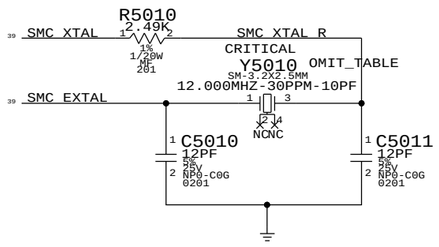
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



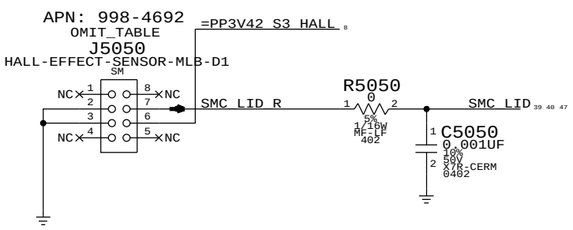
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,9	Y5010	CRITICAL	

Hall Effect pads



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

639-3261 (J4 Hall effect board) reports to 607-9320

=CHGR_ACOK	= SMC_BC_ACOK	
HISIDE_ISENSE_OC	= NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC0	= SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	= SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	= NC_SMC_GPU_HI_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC3	= SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	= SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	= SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	= SMC_SSD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	= SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	= SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	= SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	= SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	= SMC_VCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	= SMC_AXG_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	= SMC_CPU_SA_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	= SMC_CPU_SA_VSENSE	MAKE_BASE=TRUE
SMC_ADC15	= SMC_LCD_PANEL_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	= SMC_LCDBKLT_VSENSE	MAKE_BASE=TRUE
SMC_ADC17	= SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC18	= SMC_AXG_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	= NC_SMC_GPU_P1V35_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC20	= NC_SMC_T25_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC21	= NC_SMC_PCH_CORE_ISENSE	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC22	= SMC_X29_ISENSE	MAKE_BASE=TRUE
SMC_ADC23	= SMC_TBT_ISENSE	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	= NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	= NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
BDV_BKL_PWM	= NC_BDV_BKL_PWM	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	= SDCONN_STATE_CHANGE_SMC	MAKE_BASE=TRUE
	=TBT_WAKE_L	

R5012 22 5% 1/20W MF 201
PM_CLK32K_SUSCLK_R — SMC_CLK32K
PLACE NEAR=U1800 N14 5 1mm

HDMI HPD ESD PROTECTION

R5057 1K 5% 1/20W MF 201
HDMI_HPD_L — SMC_DP_HPD_L
MAKE_BASE=TRUE

S4 SMC WAKE SOURCES

=PSOC_WAKE_L
=BT_WAKE_L
=PP3V3_S4_SMC
R5082 100K 5% 1/20W MF 2 201
SMC_PME_S4_WAKE_L
MAKE_BASE=TRUE

ENET_ASF_GPIO	NC_ENET_ASF_GPIO
SMC_SYS_LED	NC_SMC_SYS_LED
MEM_EVENT_L	NC_MEM_EVENT_L
SMC_ODD_DETECT	NC_SMC_ODD_DETECT
IR_RX_OUT_RC	NC_IR_RX_OUT_RC
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP
SMC_T25_EN_L	NC_T25_EN_L
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE

MAKE_BASE=TRUE NO_TEST=TRUE

CPU_PROCHOT_L
ADC10 AND ADC11 ARE SHARED WITH COMPARATORS ON STACK BOARD
CRITICAL Q5059 SSM6N15AFE SOT563
SMC_PROCHOT

PM_THRMTRIP_L_R
CRITICAL Q5059 SSM6N15AFE SOT563
SMC_THRMTRIP

PM_THRMTRIP_B_L
R5058 3.3K 5% 1/16W MF-LF 402
PM_THRMTRIP_L
CPU_THRMTRIP_3V3
CRITICAL Q5058 MMBT3904LP-7 DFN1006-3

SMC12 PECI SUPPORT

=PPVCCIO_S0_SMC
CRITICAL Q5030 SSM3K15AMFVAPE VESM
SMC_PECI_L
R5032 0 5% 1/20W MF 201
SMC_PECI_L_R
OMIT
R5033 NOSTUFF NONE NONE 2 402
R5031 330 5% 1/20W MF 2 201
R5034 43 5% 1/20W MF 2 201
CPU_PECI_R — CPU_PECI
To SMC
From/To CPU/PCH

SMC12 SPI SUPPORT

SERIES RESISTORS ARE NO STUFFED UNTIL THE TOPOLOGY OF 2 SPI MASTERS IS VERIFIED

SPI_SMC_MISO	R5021 24	SPI_MLB_MISO	PLACE NEAR=U6100 2 1MM
SPI_SMC_MOSI	R5022 43	SPI_MLB_MOSI	PLACE NEAR=U6100 5 1MM
SPI_SMC_CLK	R5023 15	SPI_MLB_CLK	PLACE NEAR=U6100 6 1MM
SPI_SMC_CS_L	R5024 15	SPI_MLB_CS_L	PLACE NEAR=U6100 1 1MM

5% 1/20W MF 201

=PP3V3_S5_SMC
=PP3V3_S4_SMC

SMC_OOB1_RX_L	R5067 100K	NO STUFF
SMC_OOB1_TX_L	R5068 100K	NO STUFF
SMC_PME_S4_DARK_L	R5069 100K	
SMC_ONOFF_L	R5070 10K	
G3_POWERON_L	R5072 10K	
SMC_LID	R5071 100K	
SMC_TX_L	R5073 10K	
SMC_RX_L	R5074 100K	
SMC_DEBUGPRT_TX_L	R5075 10K	
SMC_DEBUGPRT_RX_L	R5076 100K	
SMC_TMS	R5077 10K	
SMC_TDO	R5078 10K	
SMC_TDI	R5079 10K	
SMC_TCK	R5080 10K	
SMC_BIL_BUTTON_L	R5081 10K	
SMC_BC_ACOK	R5087 100K	
SMC_S5_PWRGD_VIN	R5092 100K	
SMS_INT_L NOSTUFF	R5093 10K	
CPU_THRMTRIP_3V3	R5094 100K	
SPI_DESCRIPTOR_OVERRIDE_L NOSTUFF	R5095 10K	
SMC_ROMBOOT		

5% 1/20W MF 201

R5088 1K 5% 1/20W MF 201

SMC_THRMTRIP	R5086 10K	
SMC_ADAPTER_EN	R5085 10K	
SMC_S4_WAKESRC_EN	R5090 100K	
SMC_DELAYED_PWRGD	R5091 100K	
SMC_PM_G2_EN	R5098 100K	

PP3V3_WLAN_F
WIFI_EVENT_L — R5089 10K

BATLOW# ISOLATION

=PP3V3_S5_SMCBATLOW
R5040 100K 5% 1/20W MF 201
SMC_BATLOW_L
CRITICAL Q5040 SSM3K15AMFVAPE VESM
=PP3V3_SUS_SMC
Internal 20K pull-up on PM_BATLOW_L in PCH.
PM_BATLOW_L
R5041 0 5% 1/10W MF-LF 402 NOSTUFF

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012
PAGE TITLE: SMC Support
Apple Inc.
DRAWING NUMBER: <Preliminary Test> SIZE: C
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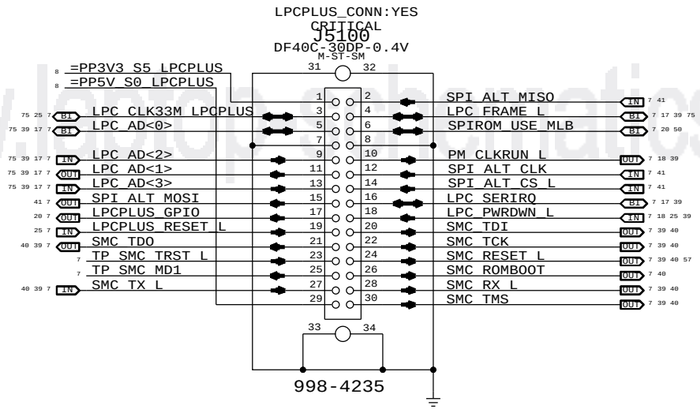
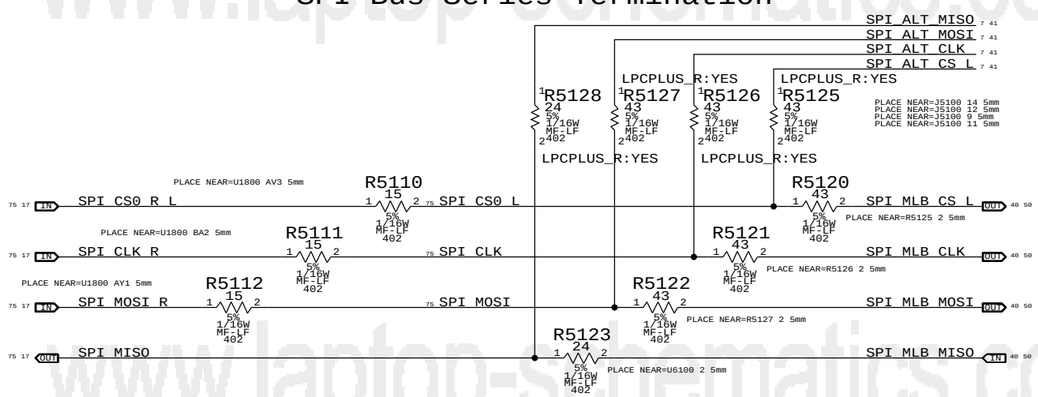
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

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PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SMBUS_PCH_CLK (MAKE_BASE=TRUE)
SMBUS_PCH_DATA (MAKE_BASE=TRUE)

R5200 1K 5% 1/20W MF 201
R5201 1K 5% 1/20W MF 201

TBT
U3600
(WRITE: 0XXX READ: 0XXX)
=I2C_TBTRTR_SCL
=I2C_TBTRTR_SDA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

AUDIO
U6411
(WRITE: 0X34 READ: 0X35)

Margin Control
U3301
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

AUDIO
U6410
(WRITE: 0X32 READ: 0X33)

MIKEY
U6751
(WRITE 0X72 READ 0X73)
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA

AUDIO
U6400
(WRITE: 0XE0 READ: 0XE1)

XDP Connectors
J2500 & J2550
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

AUDIO
U6750
(WRITE: 0X76 READ: 0X77)

HDMI Redriver (on RIO)
J4410
(WRITE: 0xCC READ: 0xCD)
=I2C_HDMIRDRV_SCL
=I2C_HDMIRDRV_SDA

LED BACKLIGHT
U9700
(WRITE: 0X58 READ: 0X59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U4900
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA

R5250 4.7K 5% 1/20W MF 201
R5251 4.7K 5% 1/20W MF 201

SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

SMC "2" SMBUS CONNECTIONS

NOTE SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC
U4900
(MASTER)
SMB_2_S3_CLK
SMB_2_S3_DATA

R5270 1K 5% 1/20W MF 201
R5271 1K 5% 1/20W MF 201

SMBUS_SMC_2_S3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_2_S3_SDA (MAKE_BASE=TRUE)

Trackpad
J5800
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

ALS
J3502
(Write 0x72 Read 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

SMS
U5920
(WRITE: 0X30/31 READ: 0X32/33)
=I2C_SMC_SMS_SCL
=I2C_SMC_SMS_SDA

GYRO
U5940
(WRITE: 0XD0 READ: 0XD1)
=I2C_SMC_GYRO_SCL
=I2C_SMC_GYRO_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

SMC
U4900
(MASTER)
SMB_5_CLK
SMB_5_DATA

R5280 2.0K 5% 1/20W MF 201
R5281 2.0K 5% 1/20W MF 201

SMBUS_SMC_5_G3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_5_G3_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J6955
(See Table)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)

SMC "3" SMBUS CONNECTIONS

=PP3V3_S3_SMBUS_SMC_3

SMC
U4900
(MASTER)
SMB_3_CLK
SMB_3_DATA

DEBUG_ADC
R5290 4.7K 5% 1/20W MF 201
DEBUG_ADC
R5291 4.7K 5% 1/20W MF 201

SMBUS_SMC_3_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_3_SDA (MAKE_BASE=TRUE)

DEBUG SENSOR ADC A
UD000
(Write: 0x10 Read: 0x11)
=I2C_SMC_ADCS_SCL
=I2C_SMC_ADCS_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Panther Point
U1800
(MASTER)
SML_PCH_0_CLK (MAKE_BASE=TRUE)
SML_PCH_0_DATA (MAKE_BASE=TRUE)

R5210 8.2K 5% 1/20W MF 201
R5211 8.2K 5% 1/20W MF 201

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

SMC
U4900
(MASTER)
SMB_1_S0_CLK
SMB_1_S0_DATA

R5260 1K 5% 1/20W MF 201
R5261 1K 5% 1/20W MF 201

SMBUS_SMC_1_S0_SCL (MAKE_BASE=TRUE)
SMBUS_SMC_1_S0_SDA (MAKE_BASE=TRUE)

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

PCH "SMLink 1" Connections

Panther Point
U1800
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA

SMLink 1 is slave port to access PCH & CPU via PECI.

X29 TEMP
TMP105: U5523
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SPKR TEMP
U6420
(WRITE: 0XD8 READ: 0XD9)
U6421
(WRITE: 0X38 READ: 0X39)
=I2C_SPKRTHMSNS_SCL
=I2C_SPKRTHMSNS_SDA

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
SMBus Connections

Apple Inc.

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REVISION <no_LABEL>
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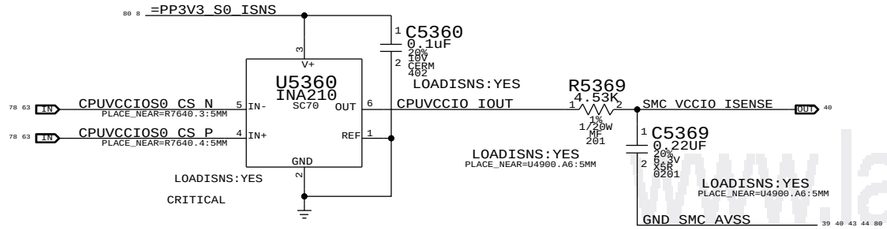
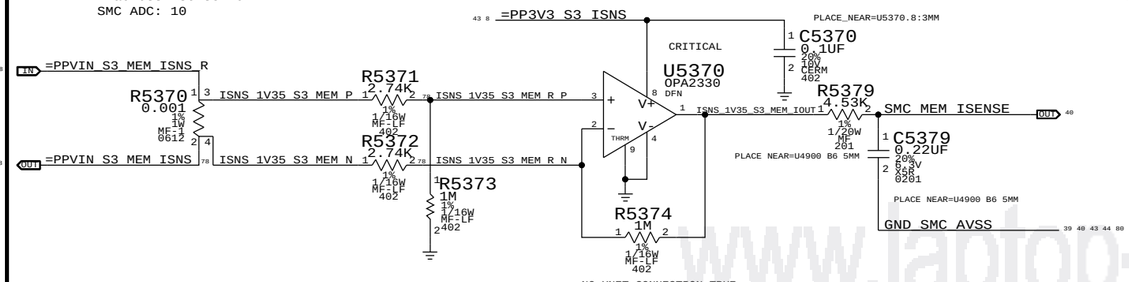
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 15 mV
SMC ADC: 11



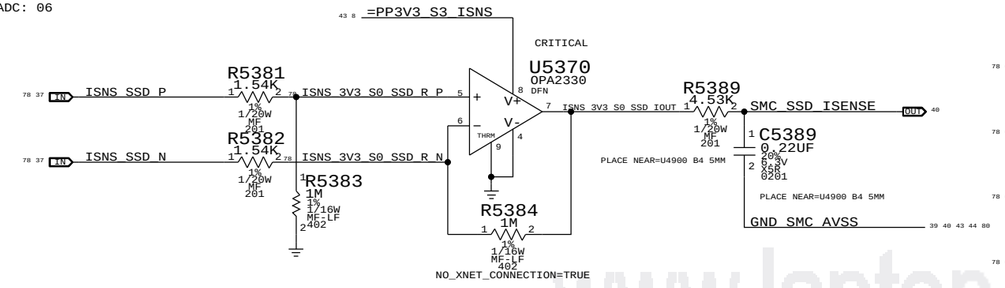
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
SMC ADC: 10



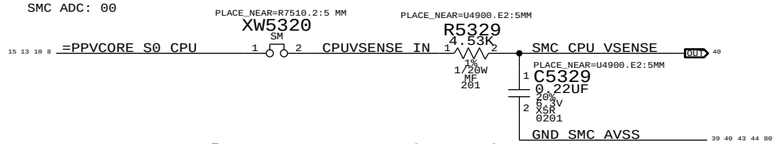
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
Rsense: 0.001 (R5370)
V across Rsense: 5 mV
SMC ADC: 06



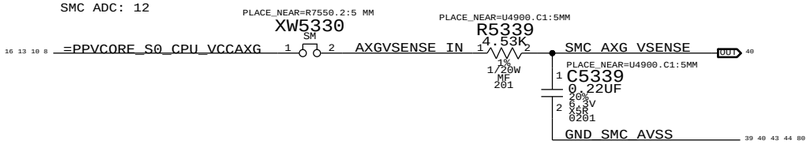
CPU Core Voltage Sense (VC0C)

Gain: 1x
SMC ADC: 00



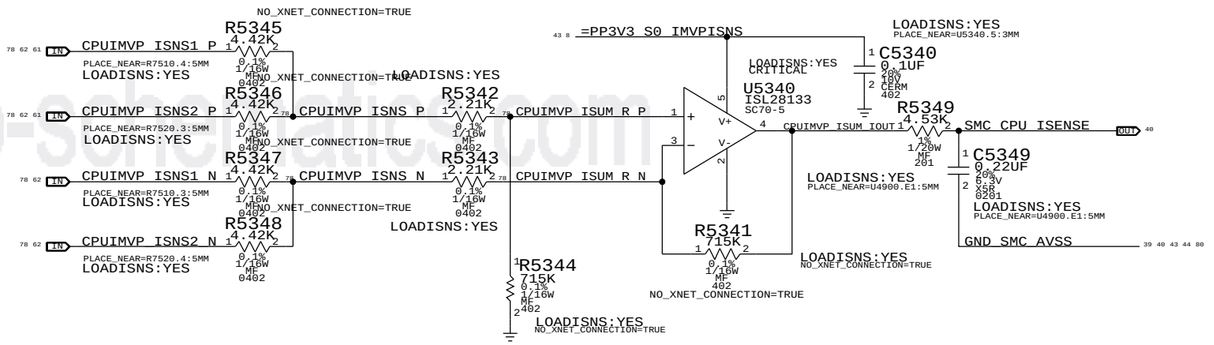
AXG Core Voltage Sense (VN0C)

Gain: 1x
SMC ADC: 12



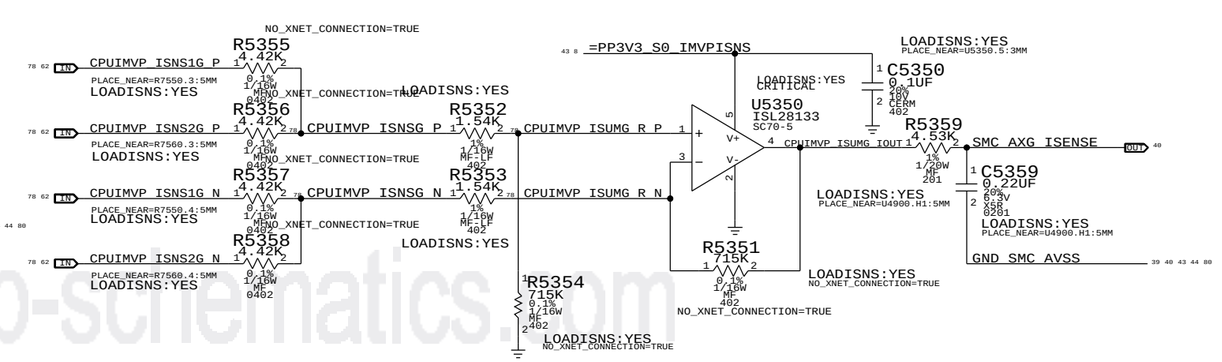
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC_MASTER=D1_SENSORS
SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: Load Side

Apple Inc.

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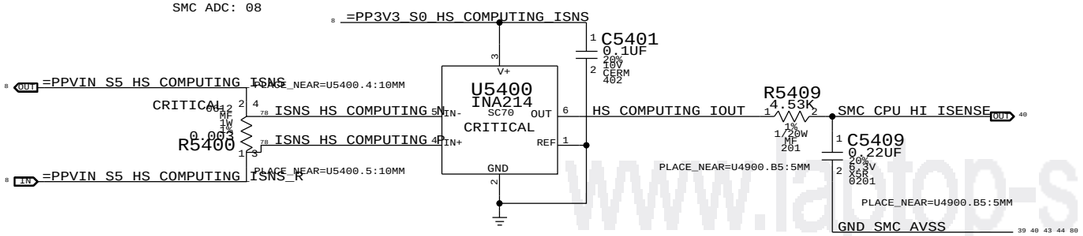
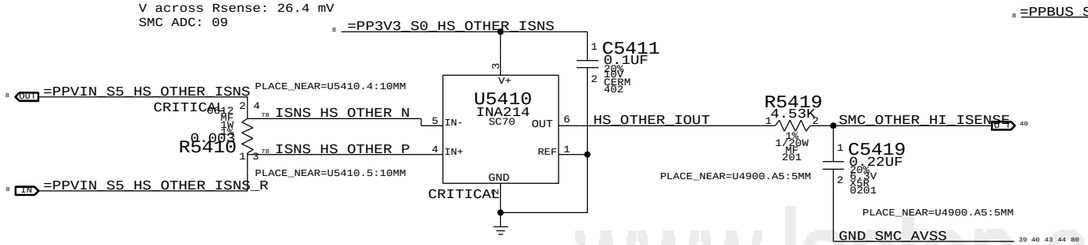
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



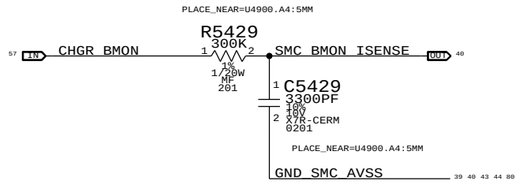
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



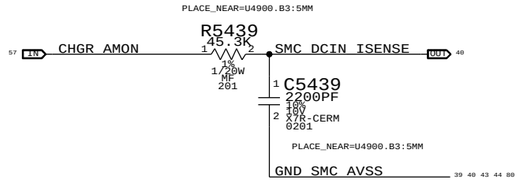
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



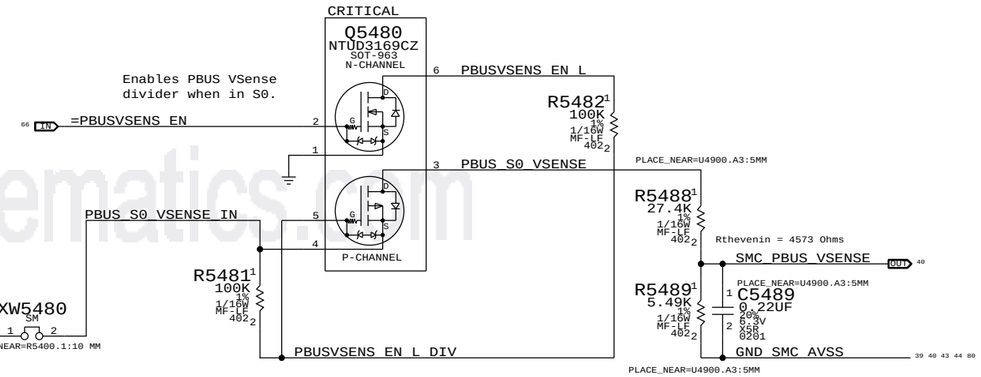
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



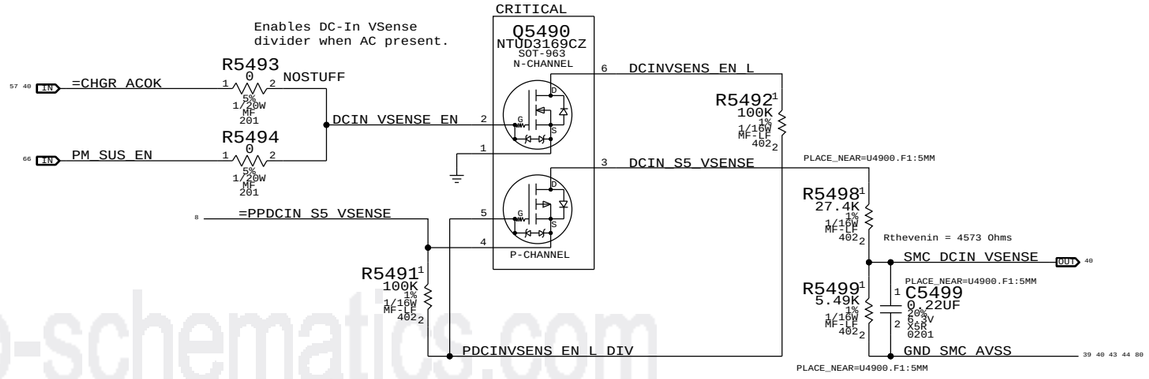
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

Gain: 0.167x
SMC ADC: 03



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: Power Sensor: High Side

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C
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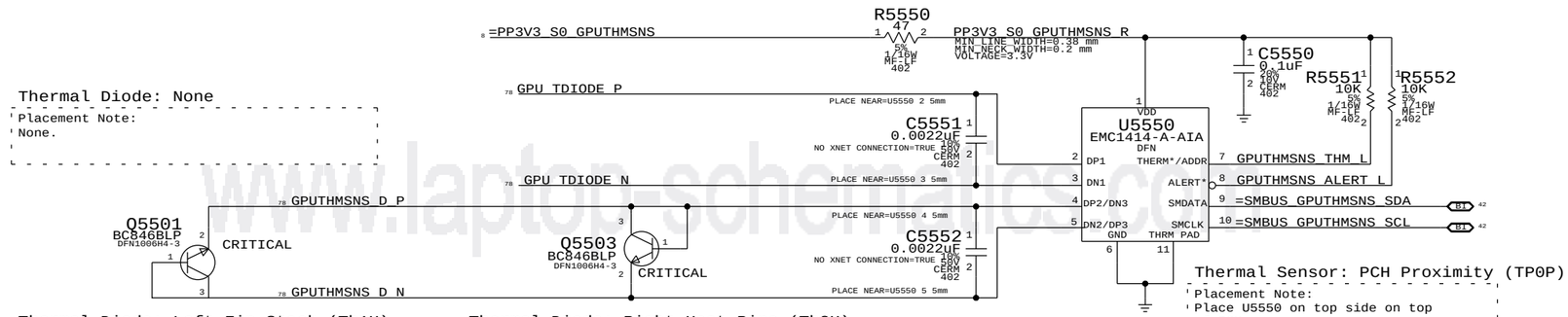
Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: None

Placement Note:
None.

Thermal Sensor: PCH Proximity (TP0P)

Placement Note:
Place U5550 on top side on top of PCH.

Thermal Diode: Left Fin Stack (Th1H)

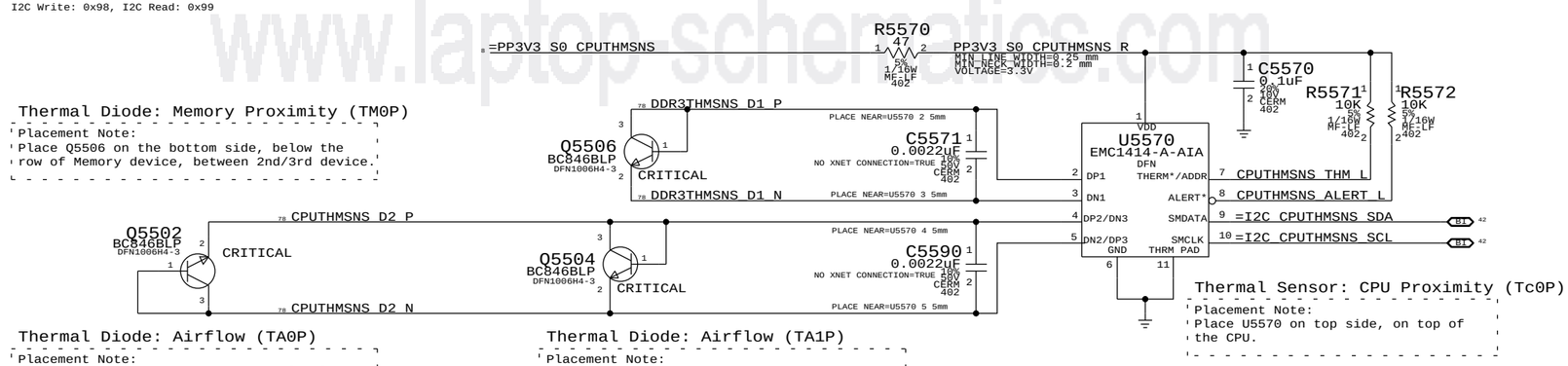
Placement Note:
Place Q5501 on the top side on the corner close to the Left Fin Stack.

Thermal Diode: Right Heat Pipe (Th2H)

Placement Note:
Place Q5503 under the top side on the corner close to the Right Fin Stack.

Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5506 on the bottom side, below the row of Memory device, between 2nd/3rd device.

Thermal Sensor: CPU Proximity (Tc0P)

Placement Note:
Place U5570 on top side, on top of the CPU.

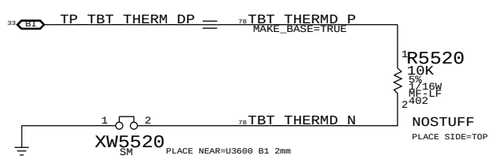
Thermal Diode: Airflow (TA0P)

Placement Note:
Place Q5502 on the bottom side, below left underneath the left fan well in the neck.

Thermal Diode: Airflow (TA1P)

Placement Note:
Place Q5504 on the either side, near LCD connector and DCIN connector.

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

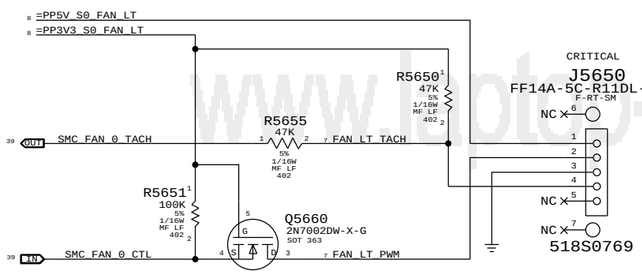
REVISION: <no_LABEL>

BRANCH:

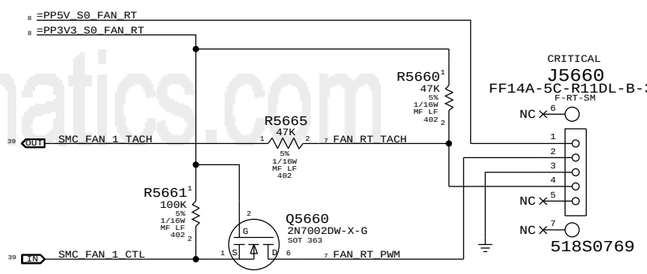
PAGE:

SHEET: 45 OF 80

Left Fan



Right Fan



SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <Preliminary Test>

SIZE C

REVISION <no_LABEL>

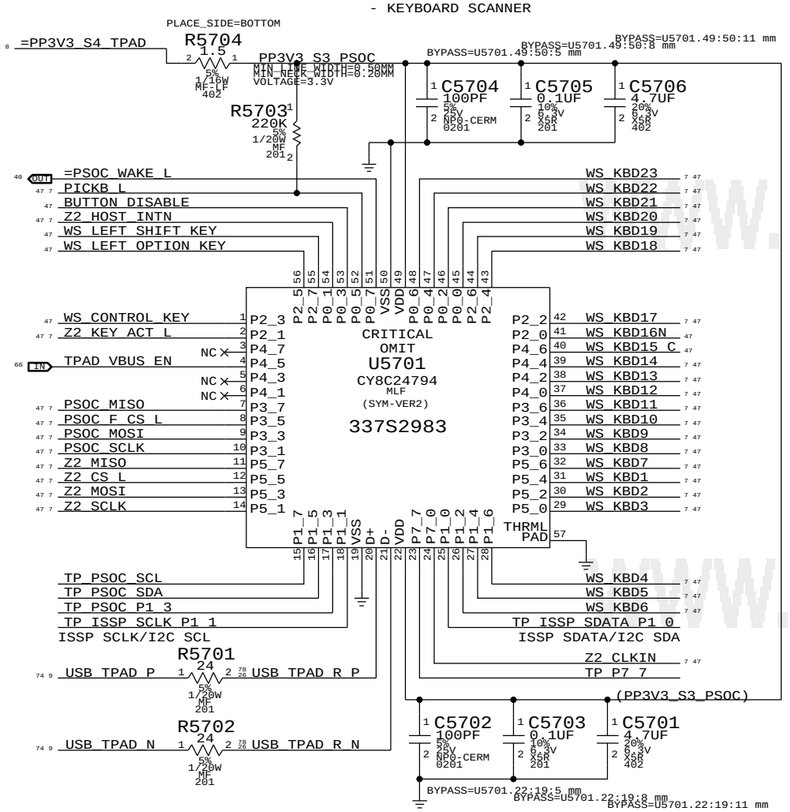
BRANCH

PAGE

SHEET 46 OF 80

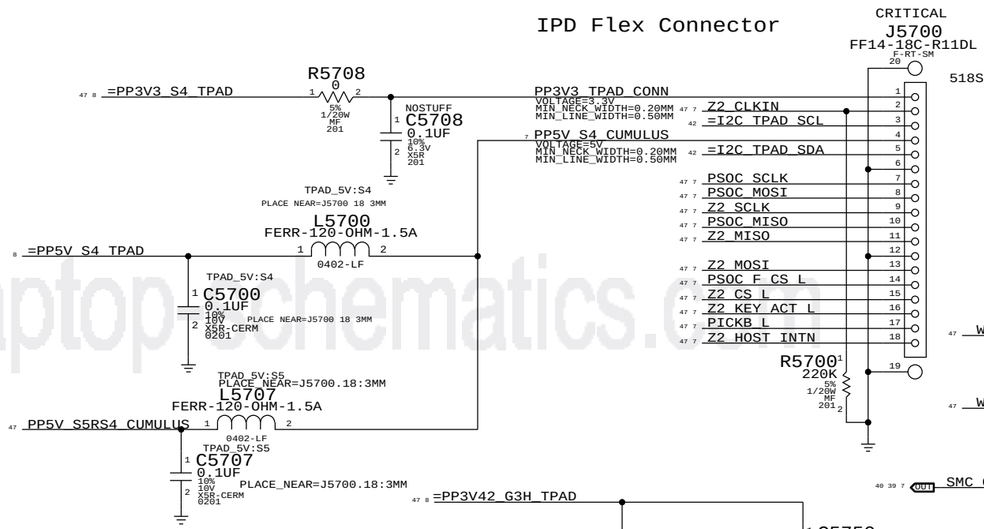
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

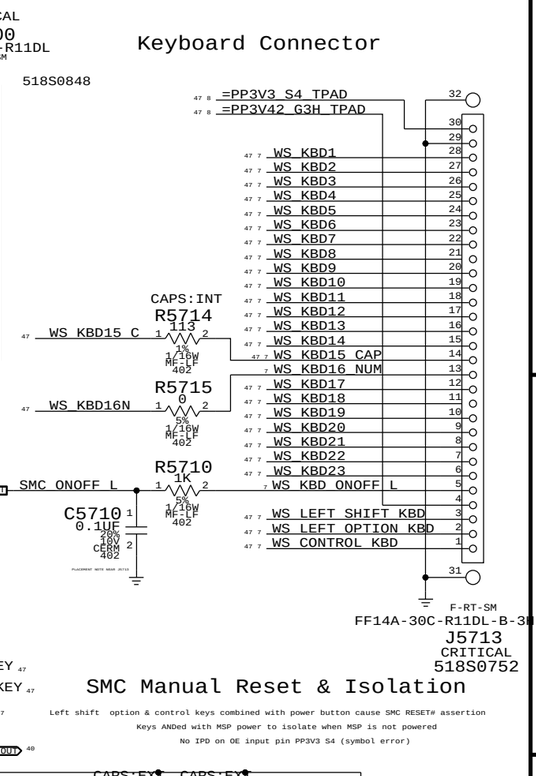


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector



Keyboard Connector



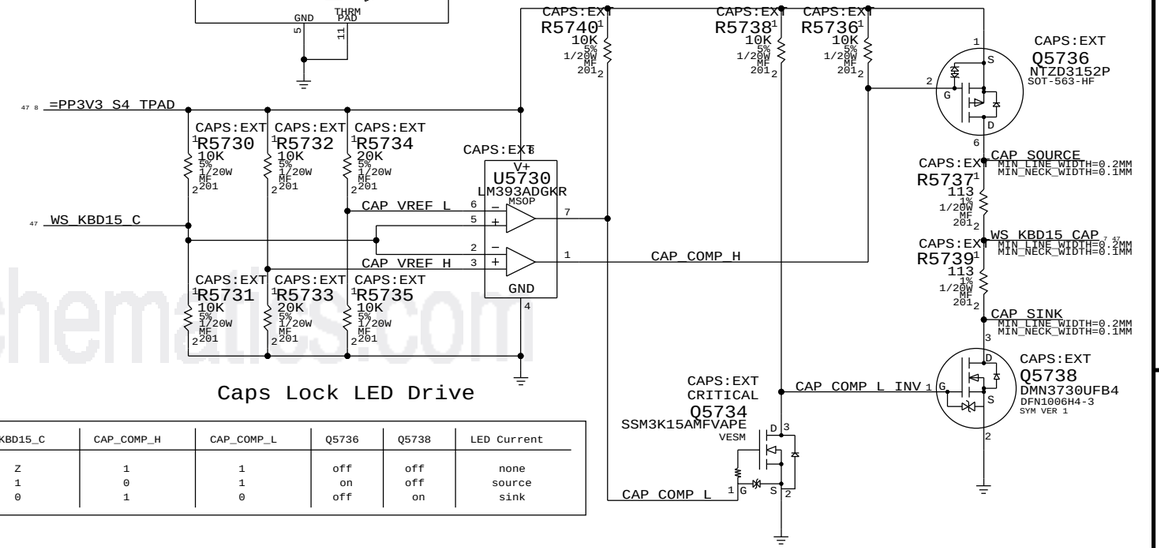
SMC Manual Reset & Isolation

Left shift option & control keys combined with power button cause SMC RESET# assertion

Keys ANDed with MSP power to isolate when MSP is not powered

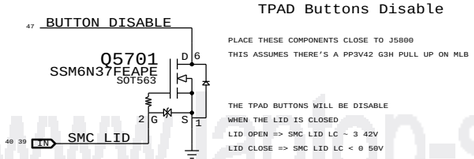
No IPD on OE input pin PP3V3 S4 (symbol error)

Caps Lock LED Drive



WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800

THIS ASSUMES THERE'S A PP3V42 G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE WHEN THE LID IS CLOSED

LID OPEN => SMC LID LC ~ 3 42V

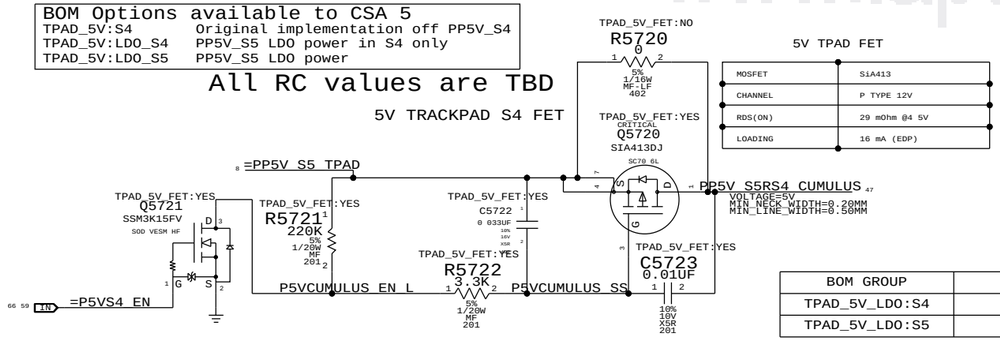
LID CLOSE => SMC LID LC < 0 50V

BOM Options available to CSA 5

TPAD_5V:S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

All RC values are TBD

5V TRACKPAD S4 FET



5V TPAD FET	
MOSFET	SiA413
CHANNEL	P TYPE 12V
RDS(ON)	29 mOhm @4 5V
LOADING	16 mA (EDP)

BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES,TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO,TPAD_5V:S5

SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

BRANCH:

PAGE:

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=PP3V3_S0_TPAD

R5858 470K 5% 1/16W MF-LF 402

SMC_SYS_KBDLED (OUT)

R5859 4.7K 5% 1/16W MF-LF 402

KBDLED_CATHODE2
PP_KBD_BOOST_VOUT
SMC_KBDLED_PRESENT_L

CRITICAL
J5815
AA07A-S010-VA1
F-ST-SM

KBDLED_CATHODE1
PP_KBD_BOOST_VOUT

J5815 PIN 5 IS GROUNDED ON KEYBOARD BACKLIGHT FLEX

Keyboard Backlight Driver & Detection

To detect Keyboard backlight SMC will tristate and read SMC SYS KBDLED

If LOW keyboard backlight present

If HIGH keyboard backlight not present

516S0899
Keyboard Backlight Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP CER 4 7UF 10% 25V X6S 0603	C5810,C5811	CRITICAL	

152S1701 COMBO
CRITICAL
L5850
10UH-20%-1.4A-0.17OHM
PST041H-CDH46D14-SM

KBDLED_SW1
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
SWITCH_NODE=TRUE

371S0490
CRITICAL
D5850
SOD-323
PMEG4010BEA

PP_KBD_BOOST_VOUT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=30V

XW5810 SM

=PP5V_S0_KBDLED
PPVIN_S0_KBDLED_L
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V

OMIT_TABLE
C5810 4.7UF 10% 25V X5R-CERM 0603
OMIT_TABLE
C5811 4.7UF 10% 25V X5R-CERM 0603
C5812 0.1UF 10% 25V X5R 402

R5810 0 5% 1/16W MF-LF 402

XW5850 SM

C5860 1.0UF 10% 50V X5R 0603
C5861 1.0UF 10% 50V X5R 0603
C5862 1.0UF 10% 50V X5R 0603
C5863 1.0UF 10% 50V X5R 0603
C5864 220PF 10% 50V X7R-CERM 0402

PPVIN_S0_KBDLED_C
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=5V

C5850 1UF 10% 25V X5R 603-1
C5851 0.01UF 10% 16V X7R-CERM 0402

R5802 0 5% 1/16W MF-LF 402

GND_KBDLED_AGND
PVDC_KBDLED

C5852 1UF 10% 25V X5R 603-1

R5850 100K 5% 1/16W MF-LF 402

GND_KBDLED_AGND

U5850
TQFN
ISL97682

VDC	11	7	VIN
EN	6	9	LX
PWMI	5	12	OVP
RSET	3		
FPW/DIRECTPWM	8		
FSW	4	13	CH1
COMP	2	15	CH2
AGND	1	14	NC
PGND	10	16	NC
THRM PAD	17		

KBDLED_EN
SMC_SYS_KBDLED_FILTER
KBDLED_RSET
KBDLED_FPW
KBDLED_FSW
KBDLED_COMP

KBDLED_OVP

R5851 0 5% 1/16W MF-LF 402
SMC_SYS_KBDLED

I_LED= 804/RSET

NOSTUFF C5854 33PF 5% 50V CERM 402
R5855 40.2K 1% 1/16W MF-LF 402
R5856 137K 1% 1/16W MF-LF 402
C5853 33PF 5% 50V CERM 402
R5854 10K 5% 1/16W MF-LF 402
KBDLEDCOMP_RC
C5855 0.0082UF 10% 25V X7R 402
NOSTUFF R5857 100K 5% 1/16W MF-LF 402

FSW =1 MHZ
SEE SPEC FOR OTHERS

KBDBKLT:ENG
R5852 10.2 0.1% 1/16W TF 402
KBDLED_CATHODE1_R
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V
KBDLED_CATHODE1
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V

KBDBKLT:ENG
R5853 10.2 0.1% 1/16W TF 402
KBDLED_CATHODE2_R
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V
KBDLED_CATHODE2
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=35V

NOSTUFF R5870 237K 1% 1/16W MF-LF 402
NOSTUFF C5870 33PF 5% 50V CERM 402
PP_KBDBOOST_XW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=30V

NOSTUFF R5871 10K 1% 1/16W MF-LF 402
NOSTUFF C5871 33PF 5% 50V CERM 402
GND_KBDLED_AGND

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES MTL FILM 1/16W 0 5 0402 SMD LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

GND_KBDLED_AGND
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

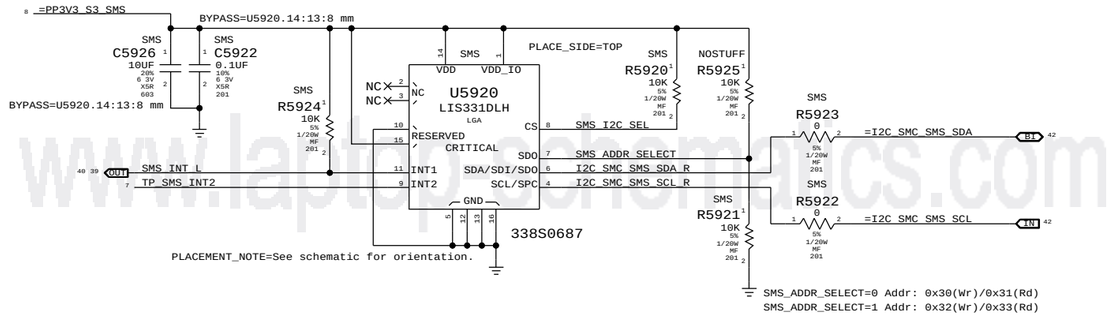
XW5800 SM

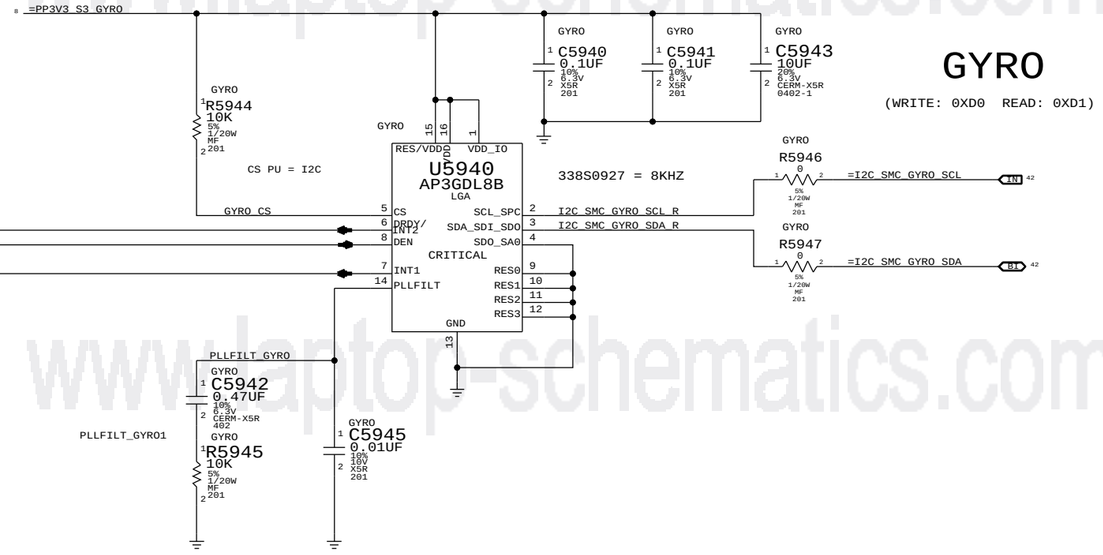
SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE: KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER: <Preliminary Test>
SIZE: C
REVISION: <no_LABEL>
BRANCH:
PAGE:
SHEET: 48 OF 80



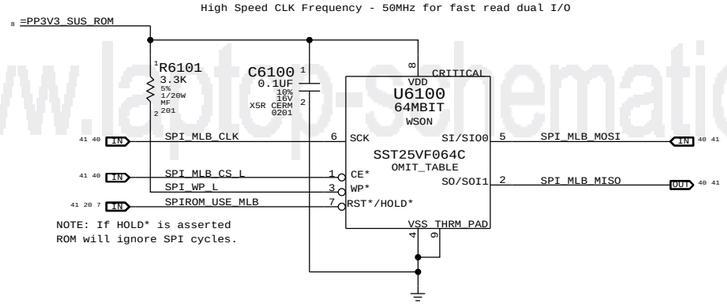


GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=J5_MLB	SYNC_DATE=07/29/2011
PAGE TITLE: DIGITAL ACCELEROMETER & GYRO	
Apple Inc.	DRAWING NUMBER: <Preliminary Test> SIZE: C
	REVISION: <no_LABEL>
	BRANCH:
	PAGE:
	SHEET: 49 OF 80

DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC_MASTER=J13_MLB SYNC_DATE=01/20/2012

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER <Preliminary Test>
SIZE C
REVISION <no_LABEL>
BRANCH
PAGE
SHEET 50 OF 80

AUDIO CODEC

APPLE P/N 353S2355

L6201
FERR-22-OHM-1A-0.065-OHM
0201

U6201 CONSUMES 40MA MAX. FROM 1.5V RAIL

=PP1V5_S0_AUDIO → PP1V5_S0_AUDIO_DIG
MIN LINE WIDTH=0 6 MM
MIN NECK WIDTH=0 2 mm
VOLTAGE=1 5V

C6210 4.7UF 20% 4V X5R 1 402
C6211 0.1UF 10% 6.3V X5R 201

C6219 10UF 20% 16V TANT POLY 0805 LLP 1
C6218 0.1UF 10% 16V X7R CERM 0402
C6217 10UF 20% 16V TANT POLY 0805 LLP 1

CRITICAL C6214 0.1UF 10% 16V X5R-CERM 0201
CRITICAL C6213 10UF 20% 10V X5R-CERM 0402-1

PP5V_AUDIO_HPAMP
PP4V5_AUDIO_ANALOG
GND_AUDIO_CODEC
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG
GND_AUDIO_CODEC

R6250 10K 5% 1/16W MF LF 402
R6251 10K 5% 1/16W MF LF 402
R6210 2.67K 1% 1/20W MF 201
R6252 0 5% 1/16W MF LF 402
R6253 0 5% 1/16W MF LF 402

SPKRCONN_L_ID
SPKRCONN_R_ID
MERRY = LOW
FG = HIGH
GPIO3 = SPKR AMP SHDN CONTROL

CRITICAL C6221 15UF 20% 4V X5R 0402
CRITICAL C6220 15UF 20% 4V X5R 0402
MIN LINE WIDTH=0 20MM
MIN NECK WIDTH=0 15MM
VBIAS_DAC
CS4206_FP
CS4206_FN

AUD_DMIC_SDA1
SPKRCONN_L_ID_R
SPKRCONN_R_ID_R
AUD_GPIO_3
AUD_SENSE_A
SPDIF_OUT2

CS4206_FLYP
CS4206_FLYC
CS4206_FLYN
CRITICAL C6222 15UF 20% 4V X5R 0402
CRITICAL C6223 15UF 20% 4V X5R 0402

C6216 1UF 10% 10V X5R 402 1
C6226 0.1UF 10% 6.3V X5R 201

U6201
CS4206B
QFN

9	VD		
24	VA_REF		
46	VA_HP		
25	VA		
29	VBIAS_DAC		
44	VHP_FILT+		
41	VHP_FILT-		
38		HPOUT_L	AUD_HP_PORT_L
40		HPOUT_R	AUD_HP_PORT_R
39		HPREF	AUD_HP_PORT_REF
2	GPIO0/DMIC_SDA1		
12	GPIO1/DMIC_SDA2		
14	GPIO2/SPDIF_OUT2		
15	GPIO3		
13	SENSE_A		
45	FLYP		
43	FLYC		
42	FLYN		
3	VL_HD		
1	VL_IF		
35		LINEOUT_L1+	AUD_LO1_L_P
34		LINEOUT_L1-	AUD_LO1_L_N
36		LINEOUT_R1+	AUD_LO1_R_P
37		LINEOUT_R1-	AUD_LO1_R_N
31		LINEOUT_L2+	AUD_LO2_L_P
30		LINEOUT_L2-	AUD_LO2_L_N
32		LINEOUT_R2+	AUD_LO2_R_P
33		LINEOUT_R2-	AUD_LO2_R_N
16	MICBIAS		TP_AUD_CODEC_MICBIAS
28	VCOM		CS4206_VCOM
21		LINEIN_L+	NC_AUD_LI_P_L
22		LINEIN_C-	NC_AUD_LI_REF
23		LINEIN_R+	NC_AUD_LI_P_R
18		MICIN_L+	AUD_MIC_INL_P
17		MICIN_L-	AUD_MIC_INL_N
19		MICIN_R+	
20		MICIN_R-	TP_AUD_MIC_INRP
27	VREF+_ADC		CS4206_VREF_ADC
4	DMIC_SCL		AUD_DMIC_CLK_R
7	DGND		
49	THRM_PAD		
26	AGND		

LFT SUBWOOFER AMP. SIG. SOURCE
RT. SUBWOOFER AMP. SIG. SOURCE
LFT. SPKR AMP. SIG. SOURCE
RT. SPKR AMP. SIG. SOURCE
EXT MIC CODEC INPUT

CRITICAL
MIN LINE WIDTH=0 20MM
MIN NECK WIDTH=0 15MM

NO TEST TRUE
NC

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
AUD_SDI_R
HDA_SDOUT
HDA_RST_L

R6211 22 5% 1/16W MF LF 402

6	BITCLK	
10	SYNC	
8	SDI	
5	SDO	
11	RESET*	
47	SPDIF_IN	AUD_SPDIF_IN
48	SPDIF_OUT	AUD_SPDIF_OUT

R6254 0 5% 1/20W MF 201

R6241 0 5% 1/20W MF 201
AUD_DMIC_CLK

C6224 1UF 20% 16V TANT 0603 SM
C6225 10UF 20% 16V TANT POLY 0805 LLP 1

R6220 33 5% 1/10W MF-LF 402
AUD_SPDIF_OUT_JACK

GND_AUDIO_CODEC
MIN LINE WIDTH=0 5MM
MIN NECK WIDTH=0 15MM
VOLTAGE=0V

4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

D1: PLACE XW6201 NEAR 5V SOURCE

L6202 FERR-22-OHM-1A-0.065-OHM 0201
L6200 FERR-22-OHM-1A-0.065-OHM 0201
MIN LINE WIDTH=0 20MM
MIN NECK WIDTH=0 15MM
VOLTAGE=5V

XW6201 SM
=PP5V_S0_AUDIO → PP5V_S0_AUDIO_XW
MIN LINE WIDTH=0 60MM
MIN NECK WIDTH=0 20MM
VOLTAGE=5V

U6200
TPS71745
SON
CRITICAL
IN, OUT, EN, NR/FB, GND, NC

4V5_REG_IN
4V5_REG_EN
4V5_NR

R6200 2.2K 5% 1/20W MF 201

C6200 1UF 10% 10V X5R 402
C6201 1UF 10% 10V X5R 402
CRITICAL C6202 0.1UF 10% 10V X5R-CERM 0201
CRITICAL C6203 1.0UF 20% 10V X5R-CERM 0201-1

XW6200 SM

MIN LINE WIDTH=0 20MM
MIN NECK WIDTH=0 15MM
VOLTAGE=4 5V
PP4V5_AUDIO_ANALOG

=PP3V3_S0_AUDIO_DIG
GND_AUDIO_CODEC

PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=D1_AUDIO
SYNC_DATE=06/06/2012
PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <Preliminary Test>
SIZE C
REVISION <no_LABEL>
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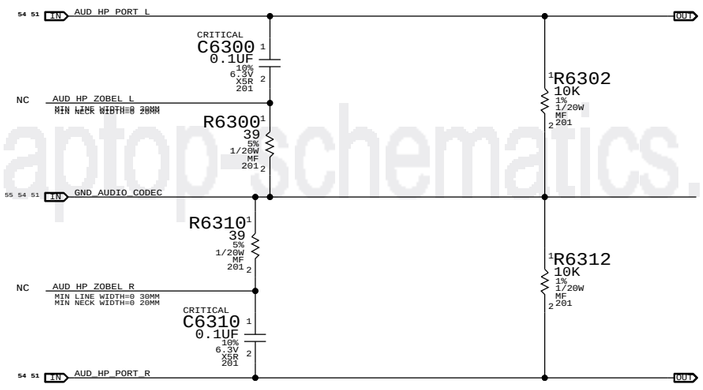
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <Preliminary Test>

SIZE C

REVISION <no_LABEL>

BRANCH

PAGE

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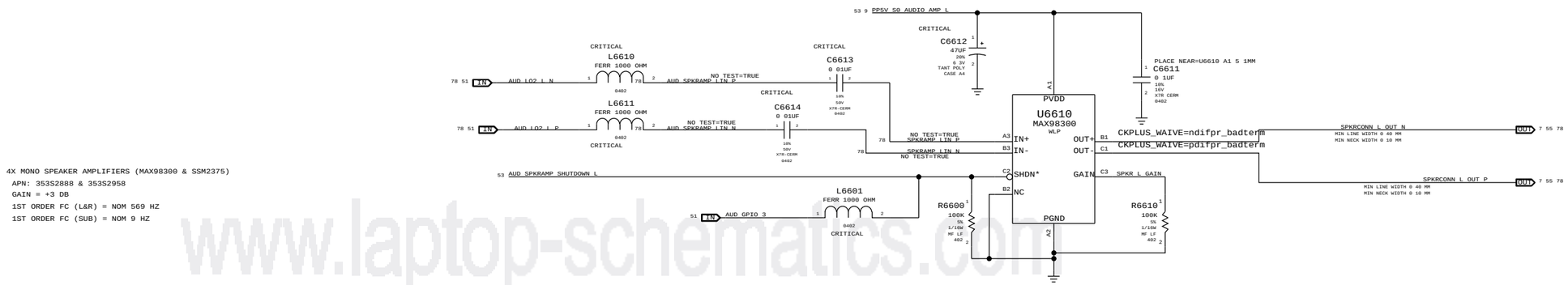
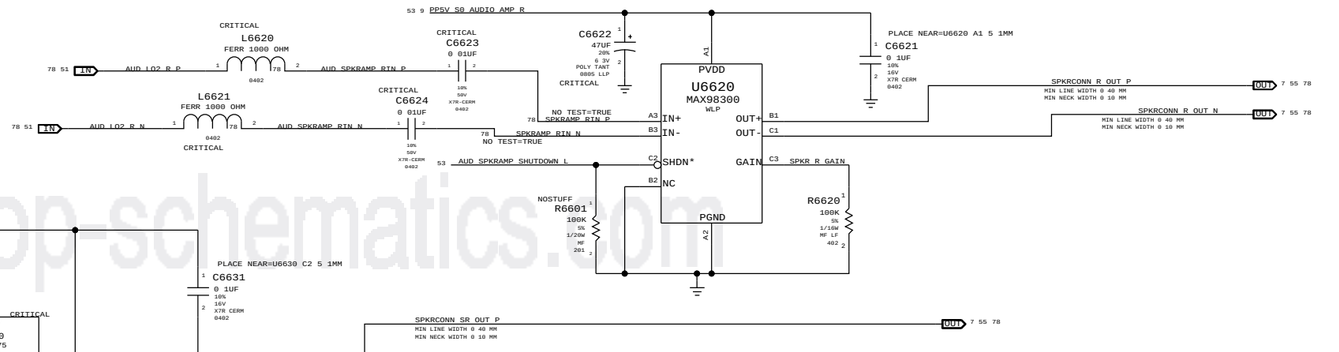
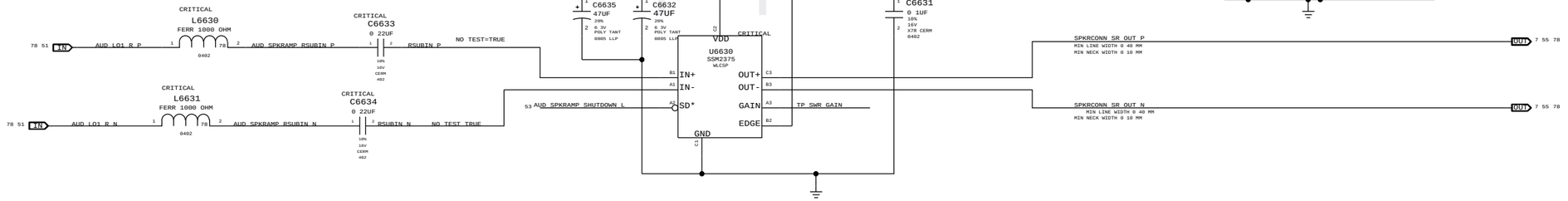
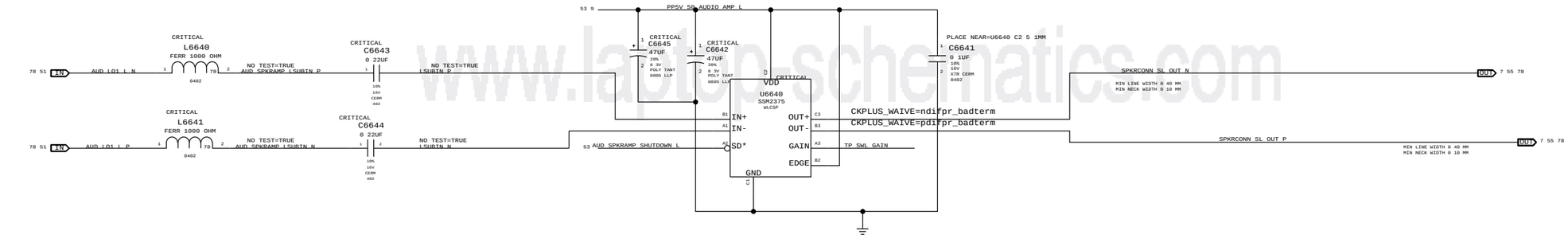
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC MASTER=D1_AUDIO
SYNC DATE=06/06/2012

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <Preliminary Test>
SIZE C
REVISION <no_LABEL>
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PAGE
SHEET 53 OF 80

AUDIO JACK: HP CONNECTOR WITH MIKEY & CHS

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

I2C PULLUPS ON SOUTHBRIDGE PAGE

55 51 PP4V5_AUDIO_ANALOG
54 51 8 =PP3V3_S0_AUDIO_DIG

R6762 10K 5% 1/20W MF 201
C6755 4.7UF 20% 6.3V X5R-CERM1 402

R6757 33 5% 1/20W MF 201
R6758 33 5% 1/20W MF 201
42 IN =I2C_MIKEY_SCL
42 BI =I2C_MIKEY_SDA

U6751
CD3282A1
WCSP

C3	SCL	MICBIAS	C1
B3	SDA	DETECT	B1
D3	INT*	BYPASS	D1
A3	ENABLE		
A1	HDET		
B2	CS		
C2	DGND	AGND	D2

A2 AVDD

54 AUDIO_SCL
54 AUDIO_SDA
19 OUT AUD_I2C_INT_L
25 IN AUD_IPHS_SWITCH_EN
HS_HDET
NOSTUFF R6761 47K 5% 1/20W MF 201
55 IN AUD_PORTA_DET_L
R6755 100K 5% 1/20W MF 201
55 54 52 51 GND_AUDIO_CODEC

HS_MIC_BIAS
HS_SW_DET
HS_RX_BP
NO_XNET_CONNECTION=TRUE
R6754 1K 5% 1/20W MF 201
C6756 0.01UF 10% 16V X5R-CERM 0201

L6754
FERR-22-OHM-1A-0.065-OHM
8 =PP3V42_G3H_AUDIO
0201
MIN LINE WIDTH=0 20MM
MIN NECK WIDTH=0 15MM
VOLTAGE=3 42V
PP3V42_G3H_AUDIO_LC
C6790 1UF 10% 10V X5R 402
C6754 0.1UF 10% 16V X5R CERM 0201
55 54 52 51 GND_AUDIO_CODEC

U6750
TS3A8235YFP
WCSP
CRITICAL

D4	RAMPI	VDD	A1
D3	RAMPO	MIC1	B1
C4	CLAMPI	MIC2	C1
B4	CLAMPO		
D2	MIC		
D1	REF		
B3	SCL		
A4	SDA		
A2	ADDR		
GND1	C2		
GND2	B2		
GND	B3, C3		

CHS_CLAMPI
NO_XNET_CONNECTION=TRUE
R6751 1K 5% 1/20W MF 201
R6752 2.2K 1% 1/20W MF 201
R6753 2.2K 1% 1/20W MF 201
CHS_CLAMPO

78 51 OUT AUD_MIC_INL_P
C6752 0.1UF 10% 6.3V X5R 201
78 HS_MIC_HI_RC
R6750 2.2K 5% 1/20W MF 201
78 HS_MIC_HI
78 HS_MIC_LO
54 IN AUDIO_SCL
54 BI AUDIO_SDA
78 51 OUT AUD_MIC_INL_N
C6753 0.1UF 10% 6.3V X5R 201
78 HS_MIC_LO_RC
R6756 100K 5% 1/20W MF 201
C6750 6800PF 10% 10V X5R-X7R-CERM 0201
C6758 27PF 5% 25V NPO-C0G 0201
C6751 10UF 20% 6.3V X5R-CERM 0402-1
C6791 10UF 20% 6.3V X5R-CERM 0402-1
54 52 51 55 GND_AUDIO_CODEC
R6759 0 5% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
R6760 47K 5% 1/20W MF 201
NOSTUFF
55 54 52 51 GND_AUDIO_CODEC

R/C6759 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210119)

XW6751
51 AUD_HP_PORT_REF
PLACE_NEAR=U6750.D1:5.1MM
NO_XNET_CONNECTION=TRUE
54 IN US_HS_GND
54 IN CH_HS_GND
55 54 52 51 GND_AUDIO_CODEC

I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

L6701
FERR-33-OHM-0.8A-0.09-OHM
US_HS_MIC 1 2 AUD_CONN_MIC
0201

L6700
120-OHM-25%-1.3A
54 OUT US_HS_GND 1 2 AUD_CONN_SLEEVE_XW
0402
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 06MM
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM

L6702
120-OHM-25%-1.3A
54 OUT CH_HS_GND 1 2 AUD_CONN_MIC_XW
0402
MIN LINE WIDTH=0 4MM
MIN NECK WIDTH=0 06MM
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM

54 51 8 =PP3V3_S0_AUDIO_DIG
51 7 OUT AUD_SPDIF_OUT_JACK
55 OUT AUD_TIPDET_INV

APN:510S0009
J6701
51138-0274
F-ST-SM
22 21 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 23 24

L6704
120-OHM-25%-1.3A
52 51 IN AUD_HP_PORT_R 1 2 AUD_CONN_HP_LEFT
0402
MIN LINE WIDTH=0.3MM
MIN NECK WIDTH=0 1MM
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM

L6703
FERR-33-OHM-0.8A-0.09-OHM
CH_HS_MIC 1 2 AUD_CONN_SLEEVE
0201

L6705
120-OHM-25%-1.3A
52 51 IN AUD_HP_PORT_R 1 2 AUD_CONN_HP_RIGHT
0402
MIN LINE WIDTH=0.3MM
MIN NECK WIDTH=0 1MM
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.1MM

L6706
FERR-470-OHM
55 OUT AUD_TYPEDET 1 2 AUD_CONN_TYPEDET
0201

SYNC MASTER=D1_AUDIO SYNC DATE=06/06/2013
PAGE TITLE: AUDIO: JACK
Apple Inc.
DRAWING NUMBER: <Preliminary Test>
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 2)	0X02 (2)	0X09 (9 A)	N/A	0X09 (B)
TWEETERS	0X04 4)	0X04 (4)	0X0B (11)	GPIO 3	N/A
SUB	0X03 3)	0X03 (03)	0X0A (10)	GPIO 3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (D E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12 C)	3V3	0X0C (12 C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13 V22 B LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

2-MIC CONNECTOR

MIN LINE WIDTH=0 40MM
MIN NECK WIDTH=0 15MM
VOLTAGE=3 3V

=PP3V3_S0_AUDIO → R6885 0 5% 1/16W MF-LF 402 → CON_DMIC_PWR
AUD_DMIC_SDA1 → R6884 0 5% 1/16W MF-LF 402 → CON_DMIC_SDA1
AUD_DMIC_CLK → R6883 0 5% 1/16W MF-LF 402 → CON_DMIC_CLK

CRITICAL J6801 FF14A-6C-R11DL-B-3H F-RT-SM
NC, 1 2 3 4 5 6, NC

SPEAKER CONNECTOR HP=80HZ

APN: 518S0627

CRITICAL J6802 78171-6006 M-RT-SM

SPKRCONN_L_OUT_P	1
SPKRCONN_L_OUT_N	2
SPKRCONN_L_ID	3
	4
SPKRCONN_SL_OUT_P	5
SPKRCONN_SL_OUT_N	6
	8

CRITICAL J6803 78171-6006 M-RT-SM

SPKRCONN_R_OUT_P	1
SPKRCONN_R_OUT_N	2
SPKRCONN_R_ID	3
	4
SPKRCONN_SR_OUT_P	5
SPKRCONN_SR_OUT_N	6
	8

PORT B DETECT(SPDIF DELEGATE) — PORT A DETECT (HEADPHONES)

AUD_SENSE_A
R6896 20.0K 1% 1/16W MF-LF 402 → AUD_PORTA_DET_L
R6895 39.2K 1% 1/16W MF-LF 402 → AUD_PORTB_DET_L
Q6897 SSM6N15AFE SOT563 (D 6, G 2, S 1)
Q6897 SSM6N15AFE SOT563 (D 3, G 5, S 4)
AUD_OUTJACK_INSERT_L
AUD_TYPEDET_OD
R6802 100K 5% 1/20W MF 201 → GND_AUDIO_CODEC
Q6800 DMC2400UV SOT563 (P-CHN)
R6801 150K 1% 1/20W MF 201 → PP4V5_AUDIO_ANALOG
AUD_TYPEDET
PP4V5_AUDIO_ANALOG
R6803 100K 5% 1/20W MF 201 → PP4V5_AUDIO_ANALOG
AUD_TYPEDET_OD_INV
C6800 0.1UF 10% 6.3V X5R 201 PLACE_NEAR=Q6800.4:5.1MM → GND_AUDIO_CODEC
Q6800 DMC2400UV SOT563 (P-CHN) AUD_TYPEDET_OD

=PP3V3_S0_AUDIO
R6867 0 5% 1/16W MF-LF 402 → AUD_IP_PERIPHERAL_DET
EXTRACTION NOTIFICATION
R6865 47K 5% 1/20W MF 201 → AUD_TIPDET_FET1
R6866 475K 1% 1/20W MF 201
APN 376S0613
Q6803 SSM6N15AFE SOT563 (D 6, G 2, S 1)
Q6803 SSM6N15AFE SOT563 (D 3, G 5, S 4)
AUD_OUTJACK_INSERT_L
AUD_TIPDET_INV
R6892 1.5K 1% 1/10W MF-LF 402 → AUD_TIPDET_INV_R
C6860 1UF 10% 25V X5R 402
CRITICAL L6801 FERR-33-OHM-0.8A-0.09-OHM 0201 → AUD_TIPDET_FET2
C6891 1UF 10% 25V X5R 402 → GND_AUDIO_CODEC

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

=PP5V_S4_AUDIO
SPEAKERID R6810 100K 1% 1/16W MF-LF 402 → SPKRCONN_L_ID
SPEAKERID R6811 100K 1% 1/16W MF-LF 402 → SPKRCONN_R_ID
R6812 100K 1% 1/16W MF-LF 402 → SPEAKERID
R6813 100K 1% 1/16W MF-LF 402 → SPEAKERID
SPEAKERID R6816 100K 1% 1/16W MF-LF 402
=PP5V_S4_AUDIO
SPEAKERID C6810 0.1UF 10% 6.3V X5R 201
SPEAKERID CRITICAL U6800 MCP6541T SC70-5
MCP6514_POS
MCP6514_NEG
MCP6514_OUT → SPEAKERID L6802 FERR-1000-OHM 0402 → SPKR_MATCH_DRV_R
SPEAKERID R6820 33 5% 1/10W MF-LF 402 → SPKR_MATCH_DRV
=PP5V_S4_AUDIO
SPEAKERID R6814 274K 1% 1/10W MF-LF 402
SPEAKERID R6817 45.3K 1% 1/10W MF-LF 402
SPEAKERID R6815 90.9K 1% 1/10W MF-LF 402
SPEAKERID C6811 4.7UF 20% 10V X5R-CERM 0402

PORT C DETECT(SPEAKER MISMATCH)

AUD_SENSE_A
SPEAKERID R6894 10K 1% 1/16W MF-LF 402
AUD_PORTC_DET_L
SPEAKERID Q6896 SSM6N15AFE SOT563 (D 6, G 2, S 1)
GND_AUDIO_CODEC

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP
376S0975	376S1081		Q6800	TOSHIBA ALT TO DIODES

SYNC MASTER=D1_AUDIO SYNC DATE=06/06/2012
PAGE TITLE
AUDIO: JACK TRANSLATORS
Apple Inc.
DRAWING NUMBER <Preliminary Test> SIZE C
REVISION <no_LABEL>
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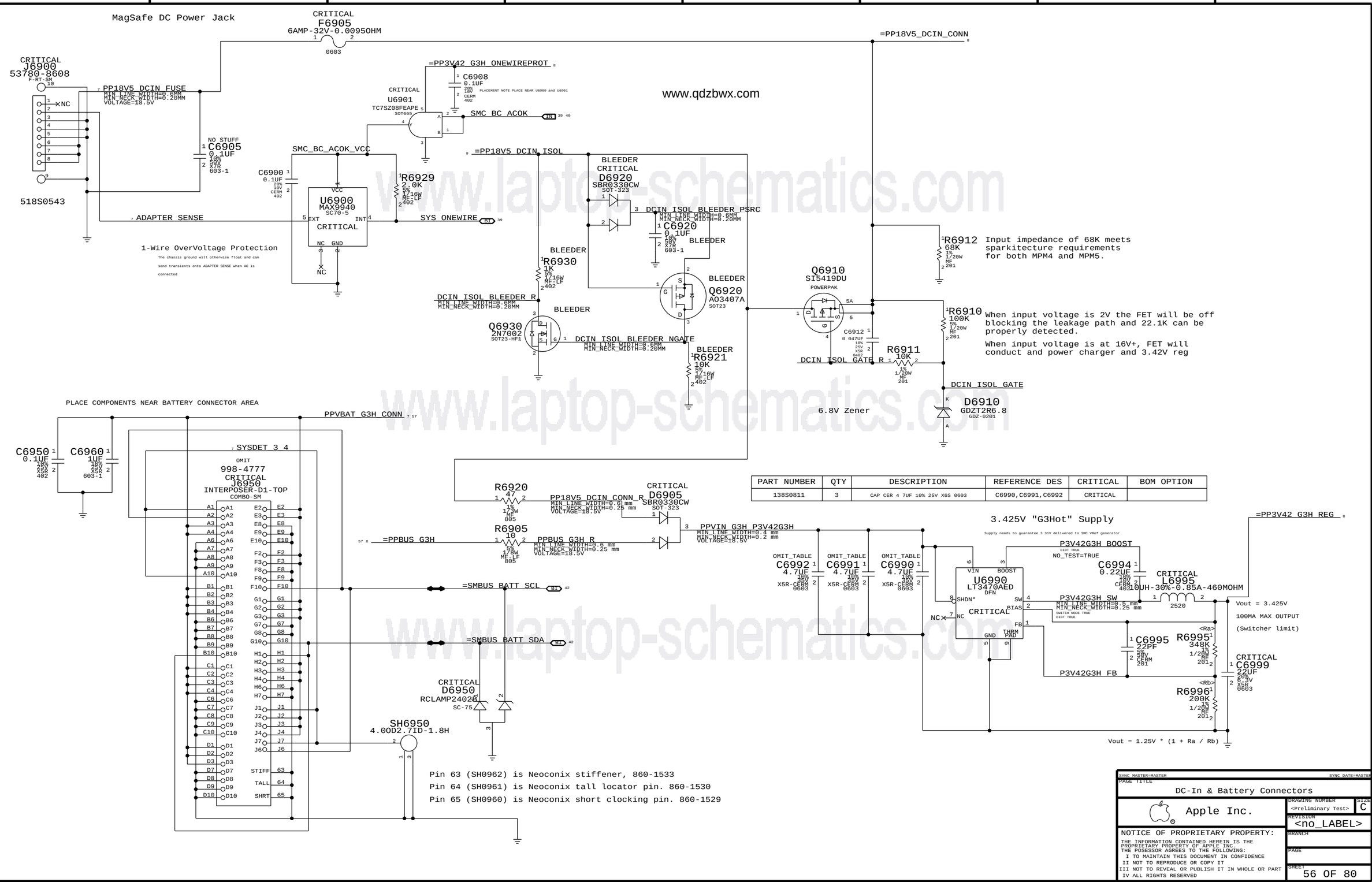

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP CER 4 7UF 10% 25V X6S 0603	C6990,C6991,C6992	CRITICAL	

SYNC MASTER=MASTER
SYNC DATE=MASTER
PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER: <Preliminary Test>
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Reverse-Current Protection

Inrush Limiter

FROM ADAPTER

=PPDCIN S5 CHGR

=PPDCIN S5 CHGR ISOL

PPDCIN G3H DRAINS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=18.5V

C7080 4.7UF 10% 25V X5R-CERM 0603 NOSTUFF

Q7080 IRF9395TRPBF DIRECTFET-MC

CRITICAL

C7085 0.1UF 10% 25V X5R 402

R7085 470K 1% 1/16W MF-LF 402

CHGR AGATE DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7086 332K 1% 1/16W MF-LF 402

CHGR SGATE DIV
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm

R7081 62K 1% 1/16W MF-LF 402

PPDCIN G3H INRUSH
MIN_LINE_WIDTH=0.1 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=18.5V

R7080 100K 1% 1/16W MF-LF 402

CRITICAL D7005 SBR0330CW SOT-323

(CHGR_AGATE)

R7005 20 5% 1/16W MF-LF 402

CHGR DCIN D R

(CHGR_DCIN)

(CHGR_SGATE)

ACIN pin threshold is 3.2V, +/- 50mV

Divider sets ACIN threshold at 13.55V

Input impedance of ~90K meets sparkitecture requirements

30mA max load

=PP3V42_G3H_CHGR

PP5V1_CHGR_VDD
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

R7001 4.7 5% 1/16W MF-LF 402

PP5V1_CHGR_VDDP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5.1V

C7001 1UF 10% 10V X5R 402

C7002 1UF 10% 10V X5R 402

NO STUFF R7002 100K 5% 1/16W MF-LF 402

GND_CHGR_AGND

R7012 1K 1% 1/16W MF-LF 402

R7010 68.1K 1% 1/16W MF-LF 402

R7000 0 5% 1/16W MF-LF 402

SMC_RESET_L

=SMBUS_CHGR_SCL

=SMBUS_CHGR_SDA

CHGR_VFRQ

CHGR_CELL

Float CELL for 1S

CHGR_ACIN

R7011 21.5K 1% 1/16W MF-LF 402

R7015 100K 1% 1/16W MF-LF 402

CHGR_ICOMP

CHGR_VCOMP

CHGR_VNEG

CHGR_CSO_P

CHGR_CSO_N

C7050 1UF 10% 10V X5R 402

CHGR_VCOMP_R

C7015 330PF 5% 50V COG 402

R7042 0 5% 1/16W MF-LF 402

R7016 3.01K 1% 1/16W MF-LF 402

CHGR_VNEG_R

C7016 470PF 10% 16V C0G 0402

CHGR_ICOMP_RC

C7042 0.068UF 10% 16V X5R-CERM 0402

C7011 0.01UF 10% 16V X7R-CERM 0402

C7000 1UF 10% 10V X5R 402-1

C7005 0.22UF 10% 6.3V X5R-CERM 0603-1

C7026 0.001UF 10% 50V X7R-CERM 0402

GND_CHGR_AGND
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

U7000 ISL62559 TQFN

VDD	19	
VDDP	20	
VHST	12	
SMB_RST_N	13	
SCL	11	=SMBUS_CHGR_SCL
SDA	10	=SMBUS_CHGR_SDA
VFRQ	4	CHGR_VFRQ
CELL	6	CHGR_CELL
ACIN	3	CHGR_ACIN
ICOMP	5	CHGR_ICOMP
VCOMP	7	CHGR_VCOMP
VNEG	8	CHGR_VNEG
CSOP	18	CHGR_CSO_P
CSON	17	CHGR_CSO_N
(AGND) THRM_PAD	29	
PGND	22	
DCIN	2	CHGR_DCIN
SGATE	26	CHGR_SGATE
AGATE	1	CHGR_AGATE
CSIP	28	CHGR_CSI_P
CSIN	27	CHGR_CSI_N
BOOT	25	CHGR_BOOT
UGATE	24	CHGR_UGATE
PHASE	23	
LGATE	21	CHGR_LGATE
BGATE	16	CHGR_BGATE
20V/V AMON	9	CHGR_AMON
36V/V BMON	15	CHGR_BMON
(OD) ACOK	14	=CHGR_ACOK

XW7000 SM

(GND)

PLACE_NEAR=U7000.29:1mm
PLACE_NEAR=U7000.22:1mm

NO_XNET_CONNECTION=TRUE

C7020 0.047UF 10% 25V X5R-CERM 0402

C7022 0.1UF 10% 25V X5R 402

C7021 0.1UF 10% 25V X5R 402

R7021 10 5% 1/16W MF-LF 402

R7022 10 5% 1/16W MF-LF 402

CHGR CSI R P

CHGR CSI R N

CRITICAL R7020 0.02 0.5% 1W 6F RL1632W

PPDCIN G3H CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

CHGR_BOOT_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

R7025 0 1/16W MF-LF 402

C7025 0.22UF 10% 10V X5R-CERM 0402
PLACE_NEAR=U7000 25 2mm

CRITICAL Q7030 RJK03P0DPA WPAK

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
DIDT=TRUE

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
GATE_NODE=TRUE
DIDT=TRUE

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.3 mm
GATE_NODE=TRUE
DIDT=TRUE

Max Current = 8.5A
(L7030 limit)
f = 400 kHz

CHGR PHASE

CRITICAL L7030 4.7UH-20%-8.5A-18.3MOHM PIME103T-4R7MS

CRITICAL F7040 12AMP-32V 1206

TO SYSTEM

=PPBUS G3H

PPVBAT G3H CHGR REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

CRITICAL C7040 68UF 20% 16V POLY-TANT CASE-D2E-SM

C7045 0.001UF 10% 50V X7R-CERM 0402

CRITICAL R7050 0.01 0.5% 1W 0612-3

PPVBAT G3H CHGR R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

C7055 1UF 10% 16V X5R 402

C7056 0.1UF 10% 16V X5R 402

C7057 0.01UF 10% 16V X7R-CERM 0402

CRITICAL Q7055 SI7137DP SO-8

TO/FROM BATTERY

PPVBAT G3H CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

R7051 2.2 5% 1/16W MF-LF 402 CHGR CSO R P

R7052 0 5% 1/16W MF-LF 402 CHGR CSO R N

(CHGR_CSO_P)

(CHGR_CSO_N)

(PPVBAT_G3H_CHGR_R)

(CHGR_BGATE)

(PPVBAT_G3H_CHGR_R)

R7092 0 5% 1/16W MF-LF 402
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.6 mm

For Erp Lot6 spec

P5V1_VIN

P5V1_BOOST
DIDT=TRUE
NO_TEST=TRUE

C7090 4.7UF 10% 25V X5R-CERM 0603 OMIT_TABLE

C7094 0.22UF 10% 10V CERM 402

U7090 LT3470A DFN

VIN BOOST SHDN* NC SW BIAS FB THRM GND PAD

CRITICAL L7095 2.2UH-20%-0.39A-0.435OHM DP418C-SM
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.5 mm

P5V1_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

P5V1_FB

P5V1_BIAS

C7095 22PF 5% 50V CERM 201

R7095 <Ra> 681K 1% 1/20W MF 201

R7096 <Rb> 200K 1% 1/20W MF 201

CRITICAL C7098 10UF 20% 6.3V X5R-CERM 0603

CRITICAL C7099 10UF 20% 6.3V X5R-CERM 0603

Vout = 1.25V * (1 + Ra / Rb)

Vout = 5.50V
100MA MAX OUTPUT
(Switcher limit)

NOSTUFF R7090 0 MF-LF 5% 402 1/16W (P5V1_BIAS) CHGR_DCIN

R7091 0 MF-LF 5% 402 1/16W PP5V1_CHGR_VDDP

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP CER 4 7UF 10% 25V X6S 0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

CRITICAL C7030 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7031 22UF 20% 25V POLY-TANT CASE-D2-SM

CRITICAL C7032 22UF 20% 25V POLY-TANT CASE-D2-SM

C7035 1.0UF 10% 50V X5R 0603

C7036 1.0UF 10% 50V X5R 0603
PLACE NEAR=Q7030 5 1mm

C7037 0.001UF 20% 50V CERM 0402
PLACE NEAR=C7036 1 3mm

SYNC MASTER=MASTER	SYNC DATE=MASTER
PAGE TITLE	PBus Supply & Battery Charger
Apple Inc.	DRAWING NUMBER: <Preliminary Test> SIZE: C
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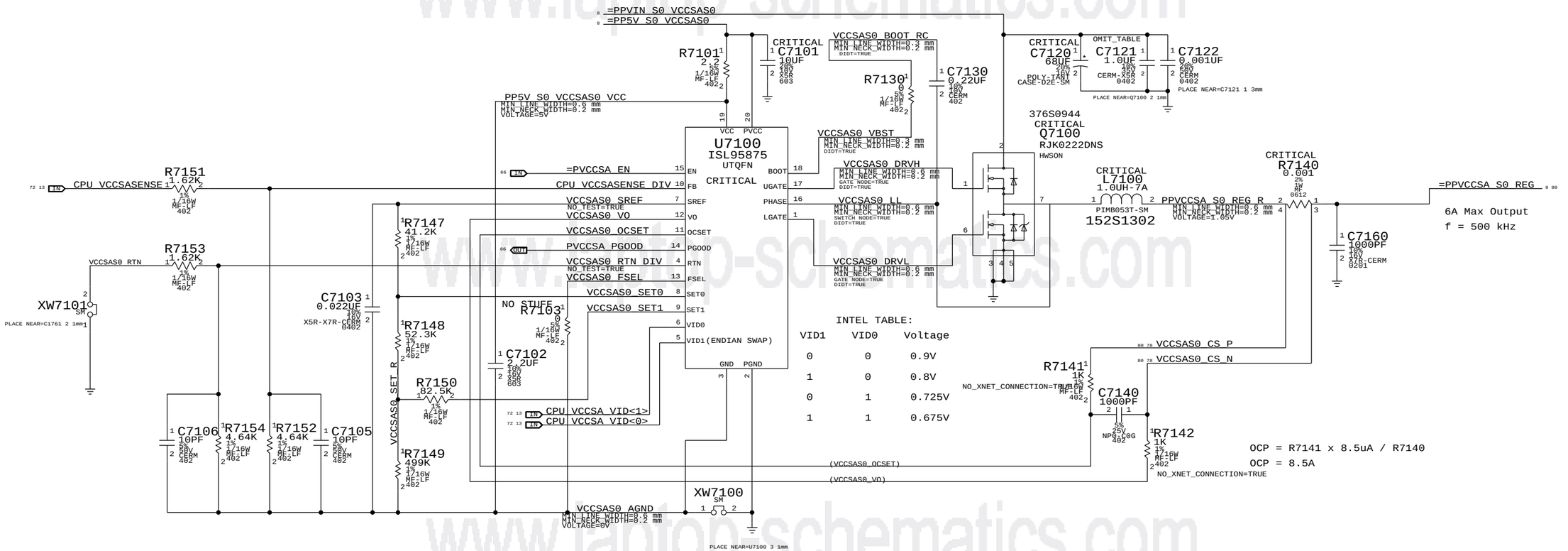
System Agent Power Supply

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7121	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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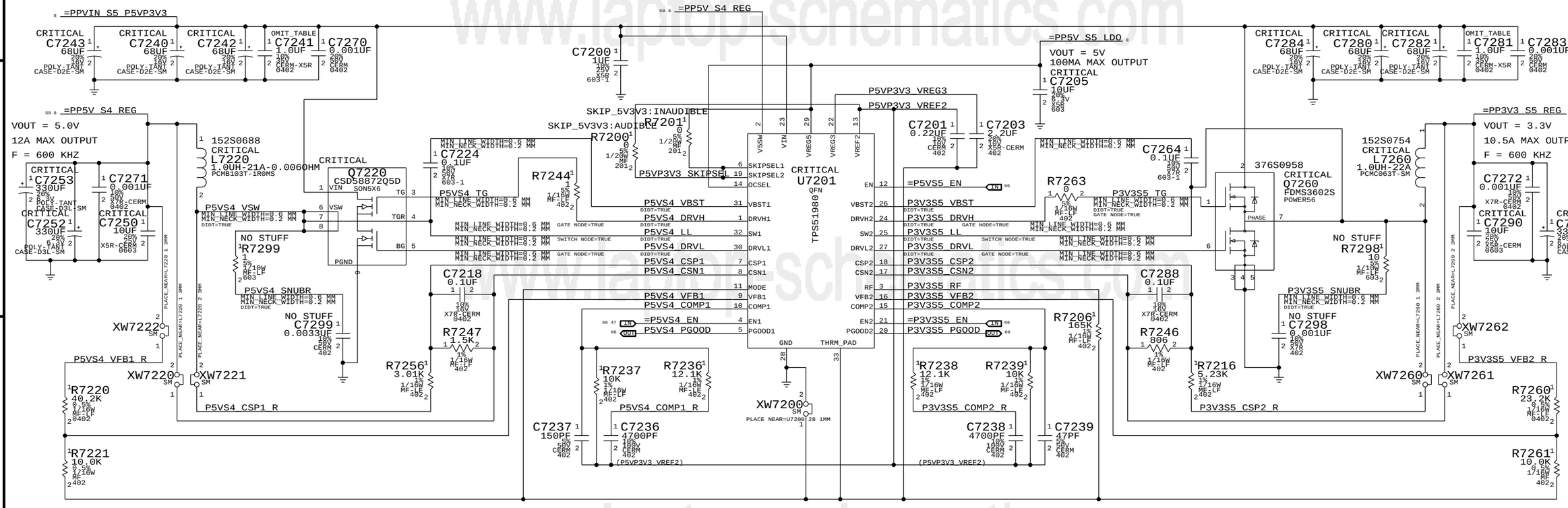
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7241,C7281	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: 5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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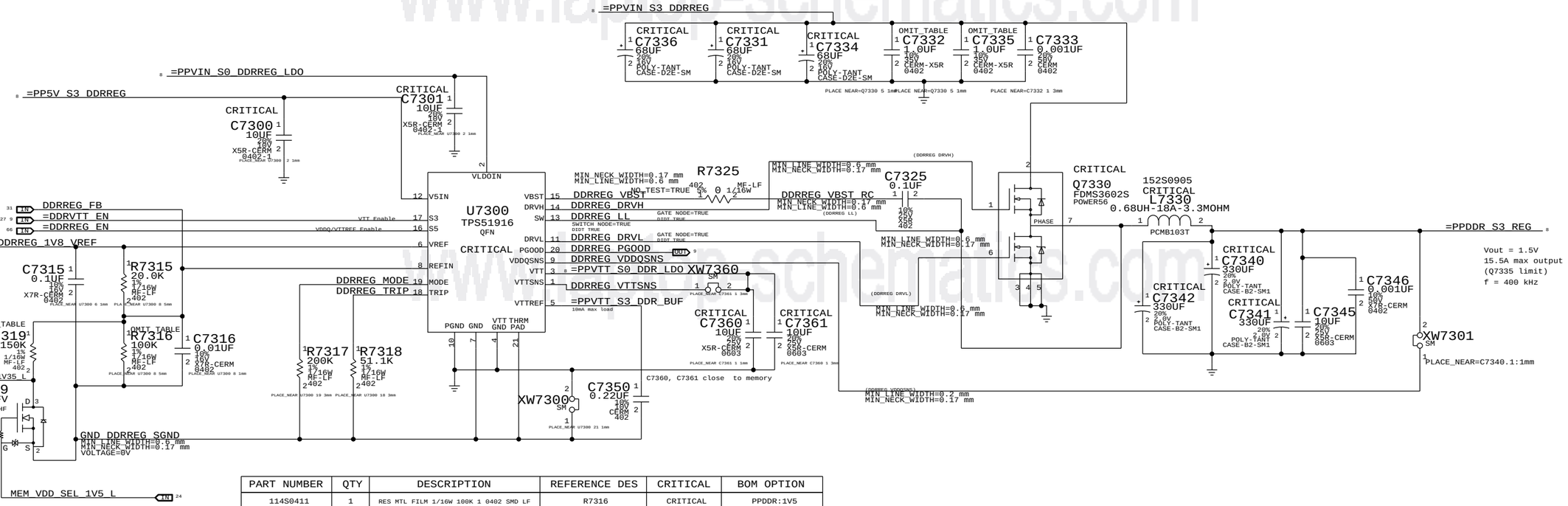
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7332,C7335	CRITICAL	

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES MTL FILM 1/16W 100K 1 0402 SMD LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES MTL FILM 1/16W 60 4K 1 0402 SMD LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET N CH 30V 100MA 7 0OHM SOT 723 HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES MTL FILM 1/16W 150k 0402 SMD LF	R7319	CRITICAL	PPDDR:1V5

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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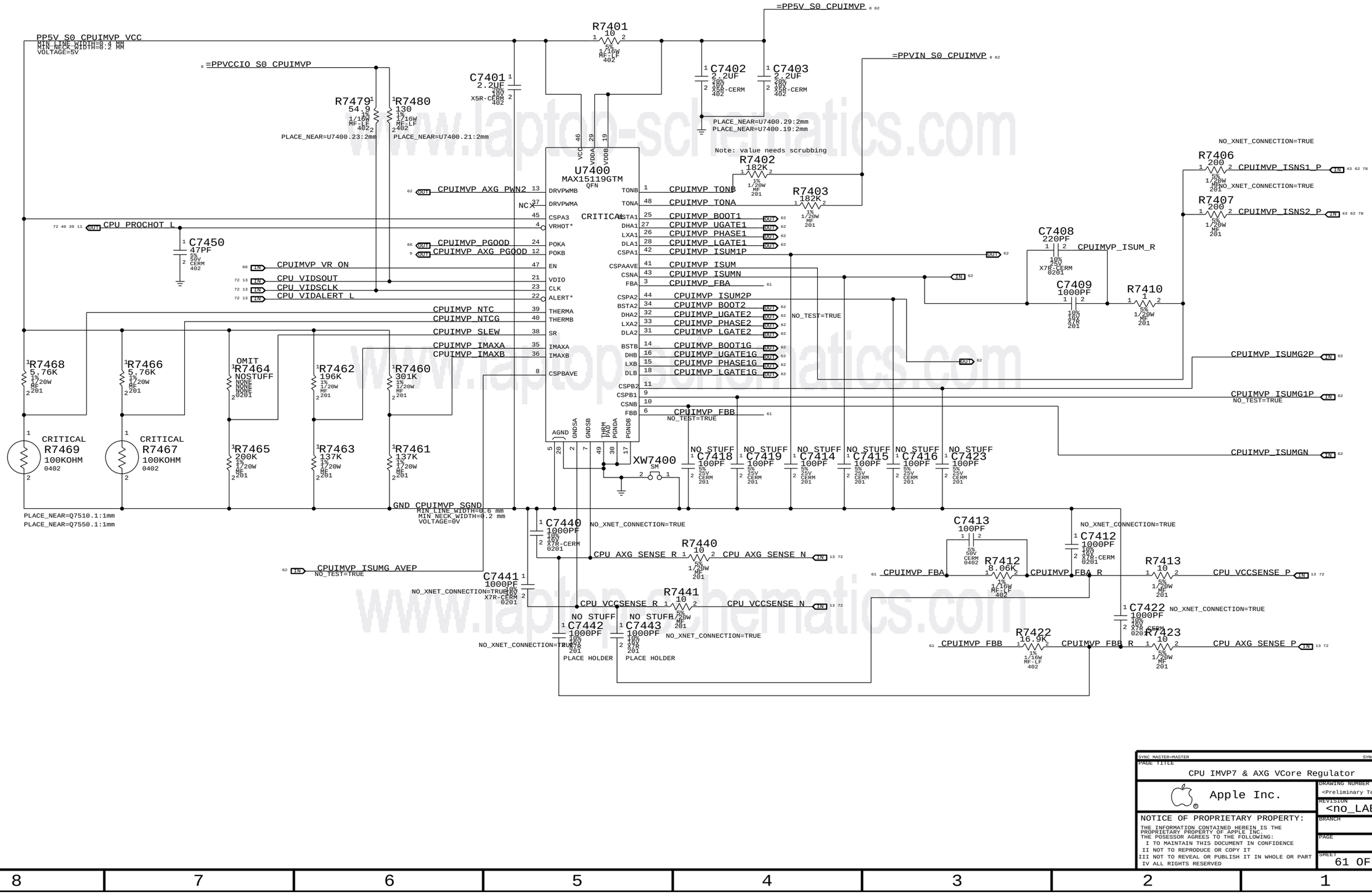

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER <Preliminary Test>

SIZE C

REVISION <no_LABEL>

BRANCH

PAGE

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PHASE 1

=PPVIN_S0_CPUIMVP

CPUIMVP_BOOT1_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
R7511 0 5% 1/10W MF-LF 402
C7511 0.22UF 10% 10V CERM 402 376S1010

CPUIMVP_BOOT1 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
CPUIMVP_UGATE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE NODE=TRUE
CPUIMVP_PHASE1 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH NODE=TRUE
CPUIMVP_LGATE1 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE NODE=TRUE

Q7510 IRF6802SDTRPBF DIRECTFET SA (CRITICAL)
Q7515 649135PBF DIRECTFET_S3C 376S1011 (CRITICAL)

C7513 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7515 OMIT_TABLE CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7516 OMIT_TABLE CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7517 OMIT_TABLE CRITICAL 1.0UF 10% 35V CERM-X5R 0402
THESE TWO CAPS ARE FOR EMC
C7518 0.001UF 10% 50V X7R-CERM 0402
C7519 0.001UF 10% 50V X7R-CERM 0402
C7510 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7512 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7510:1.1mm
PLACE_NEAR=C7517.1:3mm

L7510 CRITICAL 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_CPU_PH1
MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.25V

R7510 CRITICAL 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P

NOSTUFF R7599 200 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R7513 46.4 1% 1/20W MF 201
R7514 10 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE

CPUIMVP_ISUMN
PLACE_NEAR=U7400.43:1mm
C7571 2200PF 10% 16V X7R-CERM 0201
CPUIMVP_ISUM1P

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	4	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7517,C7527,C7557,C7565	CRITICAL	

PHASE 2

=PPVIN_S0_CPUIMVP

CPUIMVP_BOOT2_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
R7521 0 5% 1/10W MF-LF 402
C7521 0.22UF 10% 10V CERM 402 376S1010

CPUIMVP_BOOT2 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE
CPUIMVP_UGATE2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE NODE=TRUE
CPUIMVP_PHASE2 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH NODE=TRUE
CPUIMVP_LGATE2 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, GATE NODE=TRUE

Q7510 IRF6802SDTRPBF DIRECTFET SA (CRITICAL)
Q7525 649135PBF DIRECTFET_S3C 376S1011 (CRITICAL)

C7523 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7524 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7525 NOSTUFF CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7526 NOSTUFF CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7527 OMIT_TABLE CRITICAL 1.0UF 10% 35V CERM-X5R 0402
THESE TWO CAPS ARE FOR EMC
C7528 0.001UF 10% 50V X7R-CERM 0402
C7529 0.001UF 10% 50V X7R-CERM 0402
C7522 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7510.1:1mm
PLACE_NEAR=C7527.1:3mm

L7520 CRITICAL 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_CPU_PH2
MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.25V

R7520 CRITICAL 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS2_N
CPUIMVP_ISNS2_P

NOSTUFF R7598 200 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R7523 46.4 1% 1/20W MF 201
R7524 10 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE

Removed snubber with EMC's comment

CPUIMVP_ISUMN
PLACE_NEAR=U7400.43:1mm
C7572 2200PF 10% 16V X7R-CERM 0201
CPUIMVP_ISUM2P

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP CER 4 7UF 10% 25V X6S 0603	C7515,C7516,C7563,C7564	CRITICAL	

C7550 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7552 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM

=PPVIN_S0_CPUAXG

AXG PHASE 1

CPUIMVP_BOOT1G_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE
R7551 0 5% 1/10W MF-LF 402
C7551 0.22UF 10% 10V CERM 402 376S1010

CPUIMVP_BOOT1G — MIN LINE WIDTH=0 25 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE
CPUIMVP_UGATE1G — MIN NECK WIDTH=0 2 MM, MIN LINE WIDTH=0 5 MM, DIDT=TRUE, GATE NODE=TRUE
CPUIMVP_PHASE1G — MIN LINE WIDTH=0 6 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE, SWITCH NODE=TRUE
CPUIMVP_LGATE1G — MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE, GATE NODE=TRUE

Q7550 IRF6802SDTRPBF DIRECTFET SA (CRITICAL)
Q7551 649135PBF DIRECTFET_S3C 376S1011 (CRITICAL)

C7553 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7554 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7555 NOSTUFF CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7556 NOSTUFF CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7557 OMIT_TABLE CRITICAL 1.0UF 10% 35V CERM-X5R 0402
THESE TWO CAPS ARE FOR EMC
C7558 0.001UF 10% 50V X7R-CERM 0402
C7559 0.001UF 10% 50V X7R-CERM 0402
C7560 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7550.1:1mm
PLACE_NEAR=C7557.1:3mm

L7550 CRITICAL 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_AXG_R
MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM3, VOLTAGE=1.05V

R7550 CRITICAL 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_P
CPUIMVP_ISNS1G_N

R7553 46.4 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R7554 10 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE

CPUIMVP_ISUMGN
C7574 2200PF 10% 16V X7R-CERM 0201
PLACE_NEAR=U7400.10:1mm
CPUIMVP_ISUM1P

AXG PHASE 2

=PP5V_S0_CPUIMVP

R7540 10K 5% 1/16W MF-LF 402 — AXG_PHASE2
CPUIMVP_AXG_PWN2
CPUIMVP_SKIP

U7542 MAX17491 TQFN CRITICAL
PWN, SKIP*, VDD, BST, DH, LX, DL, GND, THRM PAD

C7541 AXG_PHASE2 1UF 10% 10V X5R 402

CPUIMVP_BOOT2G_RC: MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.25 MM, DIDT=TRUE
R7542 AXG_PHASE2 0 5% 1/10W MF-LF 402
C7542 AXG_PHASE2 0.22UF 10% 10V CERM 402

CPUIMVP_BOOT2G — MIN LINE WIDTH=0 25 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE
CPUIMVP_UGATE2G — MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE, GATE NODE=TRUE
CPUIMVP_PHASE2G — MIN LINE WIDTH=0 6 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE, SWITCH NODE=TRUE
CPUIMVP_LGATE2G — MIN LINE WIDTH=0 5 MM, MIN NECK WIDTH=0 2 MM, DIDT=TRUE, GATE NODE=TRUE

Q7561 649135PBF DIRECTFET_S3C 376S1011 (CRITICAL)

C7561 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7562 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7563 CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7564 CRITICAL 4.7UF 10% 35V X5S-CERM 0603
C7565 OMIT_TABLE CRITICAL 1.0UF 10% 35V CERM-X5R 0402
THESE TWO CAPS ARE FOR EMC
C7566 0.001UF 10% 50V X7R-CERM 0402
C7567 0.001UF 10% 50V X7R-CERM 0402
C7580 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
PLACE_NEAR=Q7560.1:1mm
PLACE_NEAR=C7565.1:3mm

L7560 AXG_PHASE2 CRITICAL 0.36UH-20%-36A-0.001080HM PIMS103T-SM 152S1538
PPVCORE_S0_AXG2_L
MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.05V

R7560 AXG_PHASE2 CRITICAL 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS2G_P
CPUIMVP_ISNS2G_N

R7561 AXG_PHASE2 46.4 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R7562 AXG_PHASE2 10 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE

CPUIMVP_ISUMGN
C7573 AXG_PHASE2 2200PF 10% 16V X7R-CERM 0201
PLACE_NEAR=U7400.10:1mm
CPUIMVP_ISUMG2P

Removed snubber with EMC's comment

CPUIMVP_ISNS1G_P
R7563 200 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
R7564 AXG_PHASE2 200 1% 1/20W MF 201 — NO_XNET_CONNECTION=TRUE
CPUIMVP_ISUMG_AVEP

R7566 0 5% 1/20W MF 201
CPUIMVP_ISUMG_AVE_RP
C7568 1000PF 10% 16V X7R-CERM 0201 — NO_TEST=TRUE
C7569 NOSTUFF 330PF 10% 16V X7R 201

CPUIMVP_ISUMGN

SYNC_MASTER=MASTER — SYNC_DATE=MASTER
PAGE TITLE: CPU IMVP7 & AXG VCore Output
Apple Inc.
DRAWING NUMBER: <Preliminary Test>
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REVISION: <no_LABEL>
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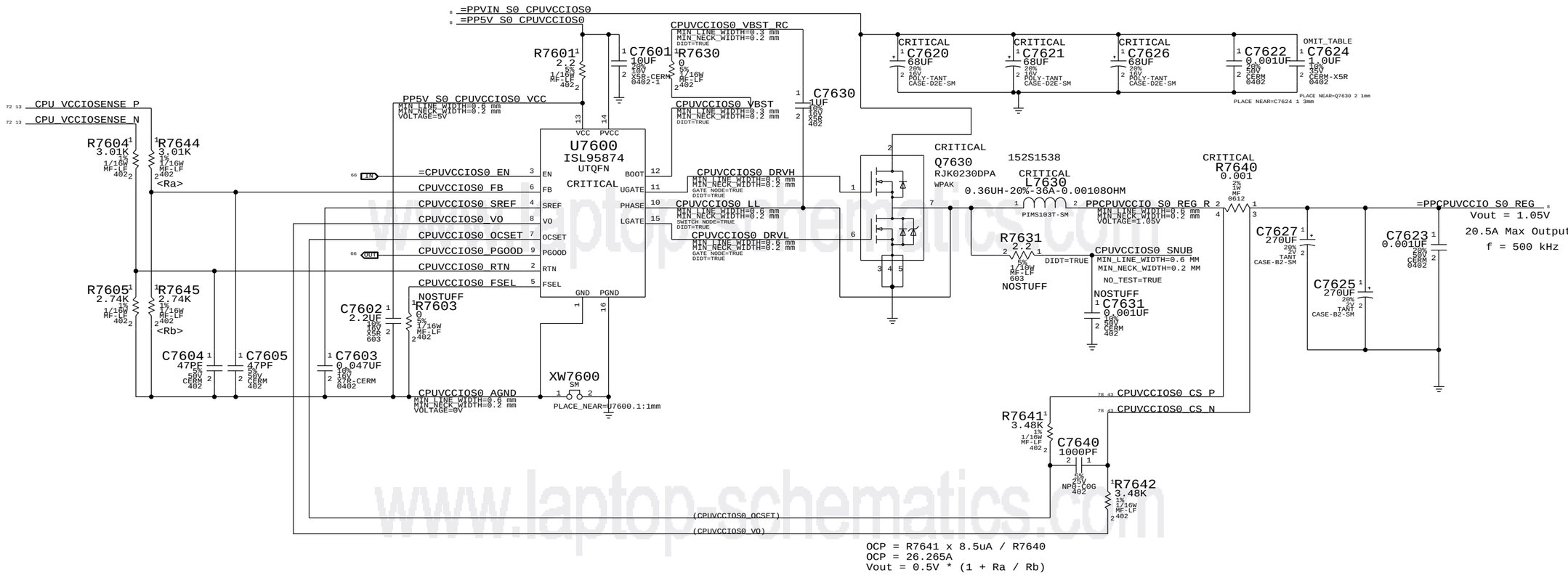
CPU VCCIO (1.05V S0) Regulator

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP CER 1UF 10% 35V X6S 0402 MURATA	C7624	CRITICAL	



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PAGE TITLE: CPUVCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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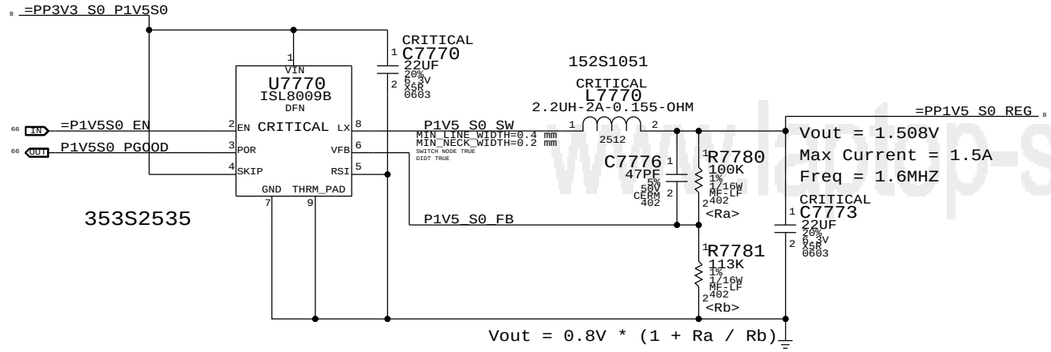
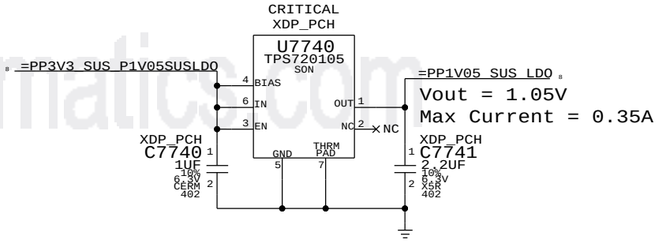
1.5V S0 Switcher



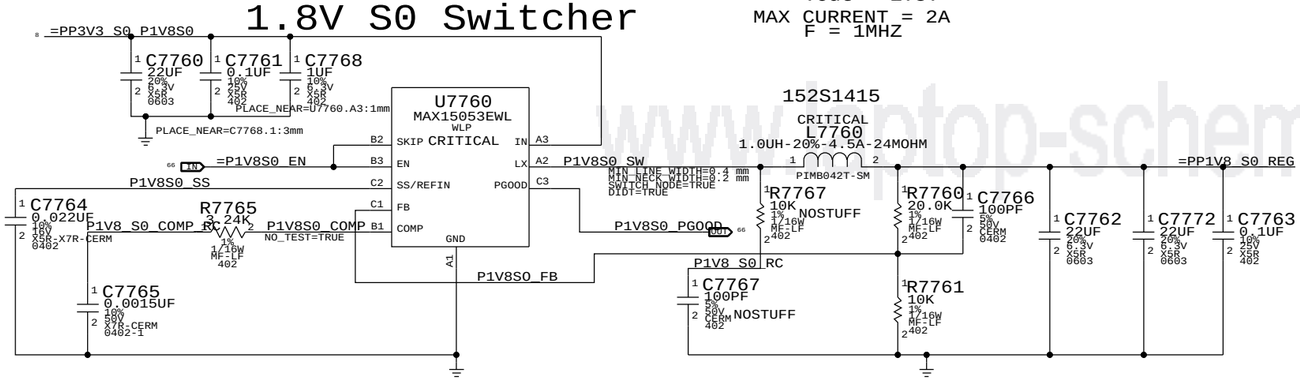
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

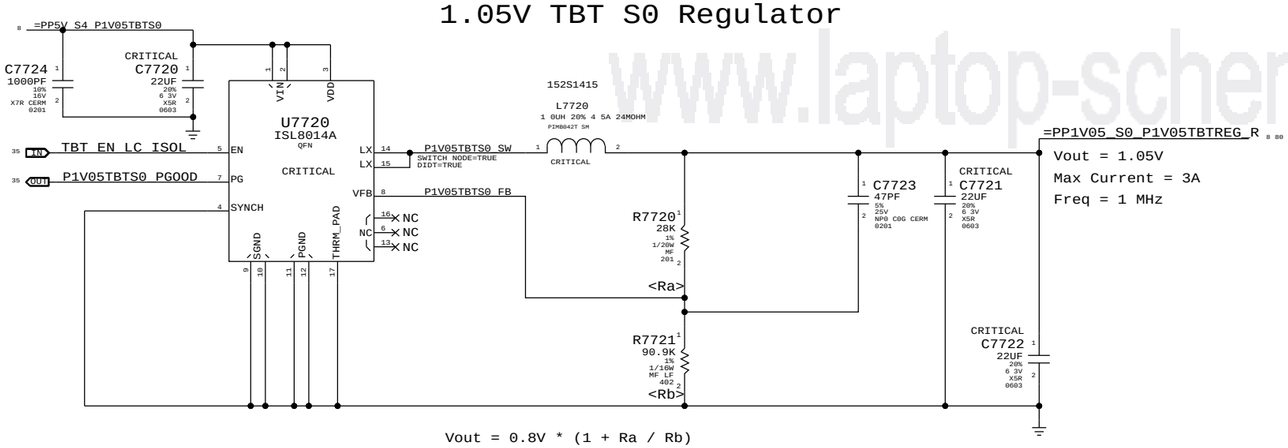


1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.05V TBT S0 Regulator



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PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

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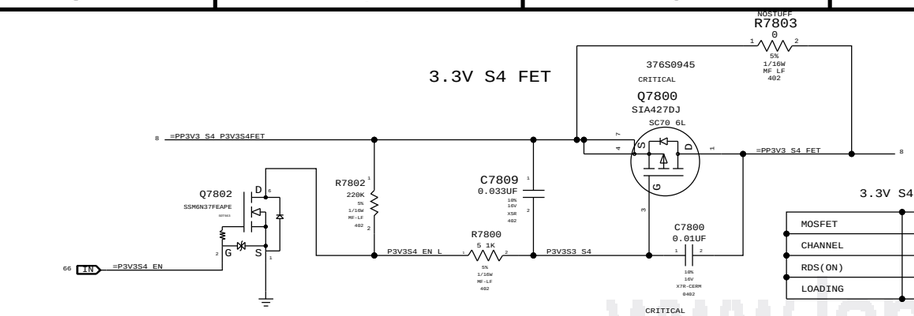
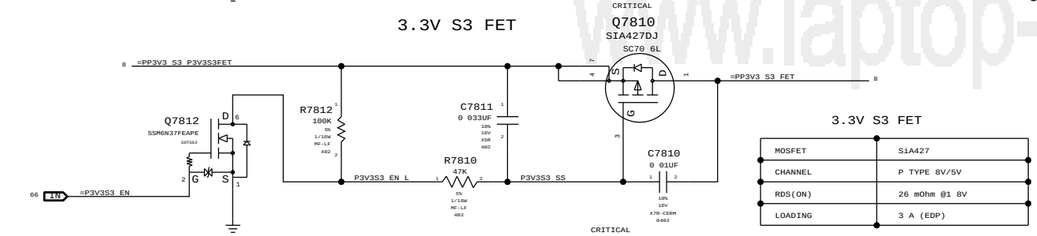
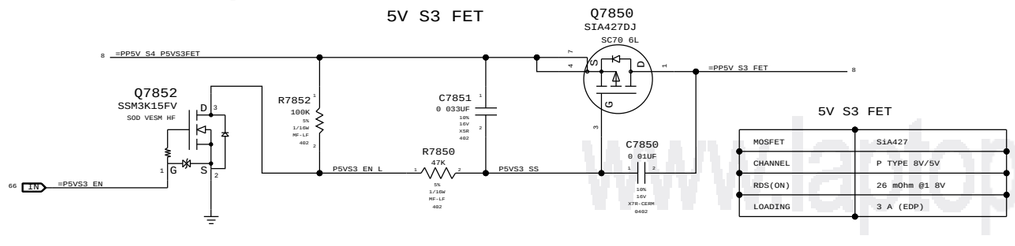


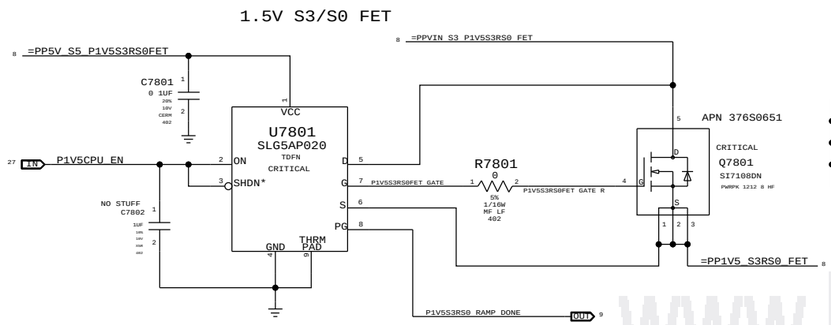
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1 8V
LOADING	0.7? A (EDP)



3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P TYPE 8V/5V
RDS(ON)	26 mOhm @1 8V
LOADING	3 A (EDP)

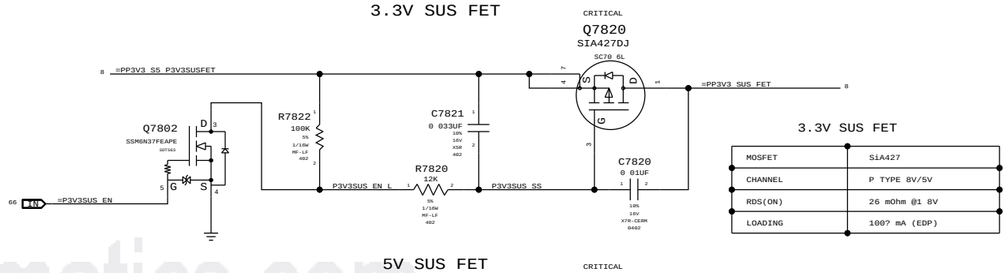


5V S3 FET	
MOSFET	SiA427
CHANNEL	P TYPE 8V/5V
RDS(ON)	26 mOhm @1 8V
LOADING	3 A (EDP)

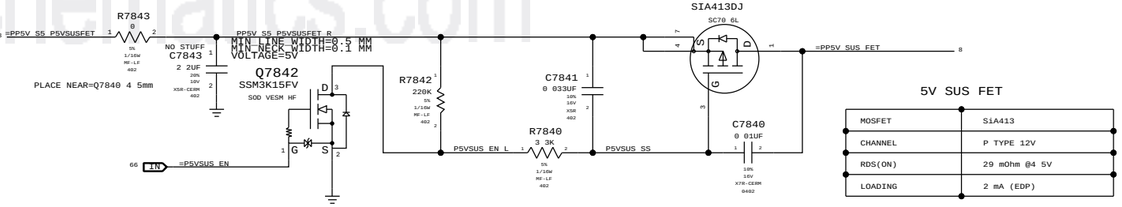


1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N TYPE
RDS(ON)	6 mOhm @4 5V
LOADING	5 A (EDP)

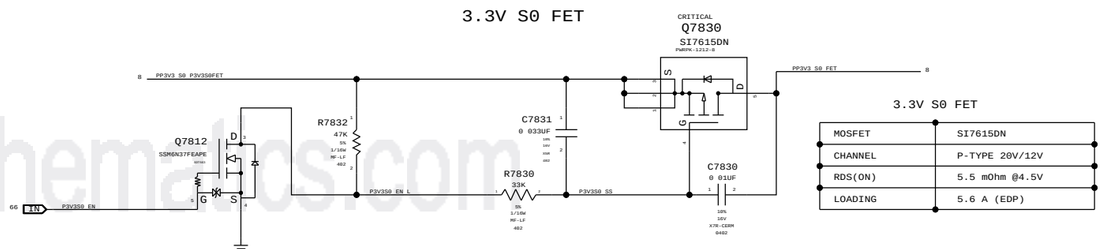
5V_SUS FET INPUT FILTER



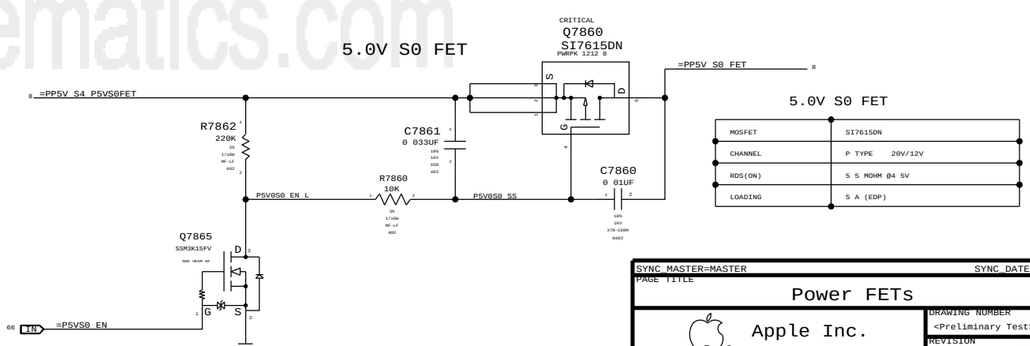
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P TYPE 8V/5V
RDS(ON)	26 mOhm @1 8V
LOADING	100? mA (EDP)



5V SUS FET	
MOSFET	SiA413
CHANNEL	P TYPE 12V
RDS(ON)	29 mOhm @4 5V
LOADING	2 mA (EDP)



3.3V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5.6 A (EDP)



5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P TYPE 20V/12V
RDS(ON)	5 5 MOHM @4 5V
LOADING	5 A (EDP)

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

REVISION: <no_LABEL>

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S5 Rail Enables & PGOOD

=P5VS5_EN (OUT 59) → SMC_PM_G2_EN (IN 40 39) MAKE_BASE=TRUE
R7940 100 5% 1/16W MF-LF 402 — PLACE NEAR U7201 21 7mm
P3V3S5_EN MAKE_BASE=TRUE → =P3V3S5_EN (OUT 59)
C7942 0.0033UF 10% 16V X5R 402 — NO STUFF

=PP3V42_G3H_PWRCTL — PLACE NEAR U7201 20 7mm
R7941 100K 5% 1/16W MF-LF 402
P3V3S5_PGOOD → S5_PWRGD (OUT 39) MAKE_BASE=TRUE
S5 PWRGD (old name RSMRST PWRGD) >SMC
SMC >PM DSW PWRGD

Mobile System Power State Table

State	SMC ADAPTER EN	SMC PM G2 ENABLE	SMC S4 WAKESRC EN	PM SUS EN	PM SLP S5 L	PM SLP S4 L	PM SLP S3 L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

3.3V S4 ENABLE

=PP3V3_S5_PWRCTL — PLACE NEAR U7940 1 2 3mm
C7970 0.1uF 20% 10V X5R 402
PM_SLP_S5_L (IN 39 18) — PM SLP S5 L 100K pull down on PCH page
U7970 74LVC1G32 SOT891
SMC_S4_WAKESRC_EN (IN 40 39) MAKE_BASE=TRUE
NC
P5V3V3_S4_EN MAKE_BASE=TRUE → =P3V3S4_EN (OUT 65)
=TBTAPWRSW_EN (OUT 69)
=TBTBPWRSW_EN (OUT 70)
NOSTUFF R7915 0 5% 1/16W MF-LF 402
=P5VS4_EN (OUT 47 59)

1.2V, 5V, 3.3V, DDR S3 ENABLE

PM_SLP_S4_L (IN 39 38 36 27 18 7) — PM SLP S4 L 100K pull down in PCH page
R7911 5.1K 5% 1/16W MF-LF 402 — PLACE NEAR U7300 10 6mm
R7912 0 5% 1/16W MF-LF 402 — PLACE NEAR Q7812 2 6mm
R7913 0 5% 1/16W MF-LF 402 — PLACE NEAR Q7842 2 6mm
R7914 0 5% 1/16W MF-LF 402 — PLACE NEAR U4900 K5 6MM
R7916 3.3K 5% 1/16W MF-LF 402 — PLACE NEAR U4900 K5 6MM
TPAD_VBUS_EN (OUT 47)
P1V2S3_EN
P5VS3_EN MAKE_BASE=TRUE → =P5VS3_EN (OUT 65)
P3V3S3_EN MAKE_BASE=TRUE → =P3V3S3_EN (OUT 65)
DDRREG_EN MAKE_BASE=TRUE → =DDRREG_EN (OUT 60)
C7910 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7912 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7913 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7914 0.47UF 10% 6.3V CERM-X5R 402
NO STUFF C7916 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD (66 39 24) — R7974 0 5% 1/16W MF-LF 402 — PLACE NEAR U7400 7 5mm
CPUIMVP_VR_ON (OUT 61)

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL — PLACE NEAR U7940 1 2 3mm
C7940 0.1uF 20% 10V CERM 402
SMC_BATLOW_L (IN 40 39) — SMC BATLOW L 100K pull up on SMC page
PM_SLP_SUS_L (IN 18) — PM SLP SUS L 100K pull down on PCH page
U7940 74AUP1G3208 SOT891 (VCC, A, B, C, Y, GND)
PM_SUS_EN MAKE_BASE=TRUE → =P5VSUS_EN (OUT 65), =P3V3SUS_EN (OUT 65)
NO STUFF R7917 0 5% 1/16W MF-LF 402

S0 ENABLE

PM_SLP_S3_L (IN 66 39 36 27 18 7) — PM SLP S3 L 100K pull down in PCH page
R7978 100 5% 1/16W MF-LF 402
PM_SLP_S3_R_L MAKE_BASE=TRUE (PM SLP S3 R L)
R7987 33K 5% 1/16W MF-LF 402 — PLACE NEAR U7100 15 6mm
R7981 20K 5% 1/16W MF-LF 402 — PLACE NEAR U7600 3 6mm
R7985 20K 5% 1/16W MF-LF 402
R7988 10K 5% 1/16W MF-LF 402 — PLACE NEAR U7770 3 6mm
R7986 5.1K 5% 1/16W MF-LF 402 — PLACE NEAR U7760 B3 6mm
=P5VS0_EN (OUT 65)
=P3V3S0_EN (OUT 65)
=PBUSVSENS_EN (OUT 44)
=TBT_S0_EN (OUT 69 70)
P1V8S0_EN MAKE_BASE=TRUE → =P1V8S0_EN (OUT 64)
P1V5S0_EN MAKE_BASE=TRUE → =P1V5S0_EN (OUT 64) (Replaced by TBT EN LC ISOL)
CPUVCCIOS0_EN MAKE_BASE=TRUE → =CPUVCCIOS0_EN (OUT 63)
PVCCSA_EN MAKE_BASE=TRUE → =PVCCSA_EN (OUT 58)
P1V05S0_EN
C7987 0.47UF 10% 6.3V CERM-X5R 402 — PLACE NEAR U7100 15 6mm
C7981 0.47UF 10% 6.3V CERM-X5R 402 — PLACE NEAR U7600 3 6mm
C7984 0.47UF 10% 6.3V CERM-X5R 402 — PLACE NEAR U7770 3 6mm
C7988 0.47UF 10% 6.3V CERM-X5R 402 — PLACE NEAR U7770 3 6mm
C7986 0.47UF 10% 6.3V CERM-X5R 402 — PLACE NEAR U7760 B3 6mm

CHGR VFRQ Generation

=PP3V42_G3H_CHGR (8 57)
R7931 100K 5% 1/16W MF-LF 402
CHGR_VFRQ (OUT 57)
Q7931 SSM3K15FV SOD-VESM-HF

VFRQ Low Fix Frequency
VFRQ High Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON (66 8) — R7951 15.0K 1% 1/16W MF-LF 402
=PP3V3_S5_VMON (8) — R7956 150K 1% 1/16W MF-LF 402
R7953 1K 5% 1/16W MF-LF 402
VMON_3V3_DIV — VMON_Q2_BASE
R7952 7.15K 1% 1/16W MF-LF 402
=PP1V5_S3RS0_VMON (66 8) — PP1V5 S3RS0 — R7954 1K 5% 1/16W MF-LF 402 — VMON_Q3_BASE
=PP1V05_S0_VMON (66 8) — R7955 1K 5% 1/16W MF-LF 402 — VMON_Q4_BASE
Q7950 ASMCC0179 DFN2015H4-8 (Q1, Q2, Q3, Q4) — NC, CRITICAL
S0PGD_C → S0PGD_BJT_GND_R 353S2809
ALL_SYS_PWRGD (24 39 66)

Worst-Case Thresholds:
Q2: 0.XXXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

3.3V SUS Detect

=PP3V3_S5_PWRCTL — PLACE NEAR U7930 6 2 3mm
No stuff C7931 12ms Min delay time
U7930 Sense input threhold is 3 07V
C7930 0.1uF 20% 10V CERM 402
CRITICAL
=PP3V3_SUS_CNTRL (8 66)
R7933 100K 5% 1/16W MF-LF 402
=PP3V3_SUS_CNTRL (66 8) — SENSE
U7930 TPS3808G33DBVRG4 SOT23-6 (VDD, RESET*, MR*, GND)
PM_RSMRST_L (OUT 18) — PM RSMRST L goes to U1800 C21
Sus_PGOOD_4CT
C7931 0.001UF 20% 25V CERM 402
NO STUFF

PCH S0 PWRGD

=PP3V3_S5_PCHPWRGD (8)
=PP3V3_S0_SB_PM (25 8)
R7950 1K 5% 1/16W MF-LF 402
C7950 0.1UF 20% 10V CERM 402
ALL_SYS_PWRGD (66 39 24)
CPUIMVP_PGOOD (61)
U7950 74LVC2G08GT SOT833 (PM_S0_PGOOD)
PLACE NEAR U1800 P12 7mm
R7949 1K 5% 1/16W MF-LF 402
SYS_PWROK_R → PM_PCH_SYS_PWROK (18 24 39)
PM_PCH_APWROK (18)
R7948 0 5% 1/16W MF-LF 402
SMC_DELAYED_PWRGD (40 39 35) → PM_PCH_PWROK MAKE_BASE=TRUE (18 25)

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

=PP5V_S0_VMON (8) — R7960 6.04K 1% 1/16W MF-LF 402
=PP3V3_S0_VMON (66 8) — R7970 10K 1% 1/16W MF-LF 402
=PP1V5_S3RS0_VMON (66 8) — R7972 6.04K 1% 1/16W MF-LF 402
=PP1V05_S0_VMON (66 8) — R7971 15.0K 1% 1/16W MF-LF 402
=PP3V3_S0_VMON (66 8) — R7961 15.0K 1% 1/16W MF-LF 402
R7973 12.4K 1% 1/16W MF-LF 402
C7960 0.1UF 20% 10V CERM 402
S0PGOOD_ISL
U7960 ISL88042IRTEZ TDFN (VDD, V2MON, V3MON, VMON, RST*, GND, THRM_PAD) — CRITICAL
353S2310
=PP3V3_S0_PWRCTL (9 8) — R7967 10K 1% 1/16W MF-LF 402
R7962 330 1% 1/16W MF-LF 402 — ALL_SYS_PWRGD_R
P1V5S0_PGOOD (64) — R7968 100 5% 1/16W MF-LF 402
P1V8S0_PGOOD (64) — R7966 100 5% 1/16W MF-LF 402
P5VS4_PGOOD (59) — R7965 100 5% 1/16W MF-LF 402
CPUVCCIOS0_PGOOD (63) — R7969 100 5% 1/16W MF-LF 402
PVCCSA_PGOOD (58) — R7963 100 5% 1/16W MF-LF 402
(OUT 24 39 66)

"WLAN" = ("S3" && "AP_PWR_EN")

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

SMC_ADAPTER_EN (IN 40 39 18)
Q7920 SSM6N37FEAPE SOT563
NO STUFF R7929 0 5% 1/16W MF-LF 402
AC_EN_L
Q7920 SSM6N37FEAPE SOT563
PM_SLP_S3_L (IN 66 39 36 27 18 7)
Q7925 SSM6N15AFE SOT563
PM_WLAN_EN_L
R7925 10K 5% 1/16W MF-LF 402
Q7925 SSM6N15AFE SOT563
=PP3V3_S3_WLAN (8 36)
R7926 10K 5% 1/16W MF-LF 402
PM_WLAN_EN (OUT 36)
AP_PWR_EN (IN 19 24 36)

SYNC MASTER=MASTER	SYNC DATE=MASTER
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LCD PANEL INTERFACE (eDP)

CRITICAL
J9000
20525-130E-01
F-RT-SM

PPVOUT_S0_LCDBKLT
NC
LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
LCD_HPD_CONN
LCD_FSS
DP_INT_AUX_P
DP_INT_AUX_N
BEAD_PROBE=TRUE DP_INT_ML_P<0>
BEAD_PROBE=TRUE DP_INT_ML_N<0>
BEAD_PROBE=TRUE DP_INT_ML_P<1>
BEAD_PROBE=TRUE DP_INT_ML_N<1>
BEAD_PROBE=TRUE DP_INT_ML_P<2>
BEAD_PROBE=TRUE DP_INT_ML_N<2>
BEAD_PROBE=TRUE DP_INT_ML_P<3>
BEAD_PROBE=TRUE DP_INT_ML_N<3>
518S0829

LCD_HPD — R9000 0 5% 1/20W MF 201
DP_INT_AUX_C_P — C9028 0.1UF 10% 16V X5R-CERM 0201
DP_INT_AUX_C_N — C9029 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_P<0> — C9020 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_N<0> — C9021 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_P<1> — C9022 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_N<1> — C9023 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_P<2> — C9024 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_N<2> — C9025 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_P<3> — C9026 0.1UF 10% 16V X5R-CERM 0201
DP_INT_ML_C_N<3> — C9027 0.1UF 10% 16V X5R-CERM 0201

LCD_PWR_EN — R9010 1K 5% 1/10W MF 402

CRITICAL
U9000
FPF1009
MFET-2X2-8IN
ON
VIN_1 VOUT_1
VIN_2 VOUT_2
GND THRM PAD

=PP5V_S0_LCD
C9009 0.1UF 10% 16V X7R-CERM 0402
C9011 0.1UF 10% 16V X7R-CERM 0402
C9012 10UF 20% 6.3V X5R 603

PP5V_S0_LCD_ISNS — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V
XW9020 SM
PP5VR3V3_SW_LCD_UF — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V

CRITICAL
L9000
FERR-220-OHM
0805

PP5VR3V3_SW_LCD — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V

C9001 0.1UF 10% 16V X5R-CERM 0201
C9002 0.1UF 10% 16V X5R-CERM 0201
C9003 1000PF 10% 100V X7R-CERM 0603
C9000 1000PF 10% 100V X7R-CERM 0603

NC_ISNS_LCD_PANELN
NC_ISNS_LCD_PANELP

LCD Panel Current XW Short

EDP: 1 A, Refdes: XW9020

LCD Panel HPD & AUX strapping

=PP3V3_S0_LCD
R9003 1M 5% 1/20W MF 201
DP_INT_AUX_N
LCD_HPD_CONN
DP_INT_AUX_P
R9001 1M 5% 1/20W MF 201
R9002 1M 5% 1/20W MF 201

NO_XNET_CONNECTION=TRUE

BP9000 BEAD-PROBE SM — DP_INT_ML_P<0> — R9011 1M 5% 1/20W MF 201
BP9001 BEAD-PROBE SM — DP_INT_ML_N<0> — R9012 1M 5% 1/20W MF 201
BP9002 BEAD-PROBE SM — DP_INT_ML_P<1> — R9013 1M 5% 1/20W MF 201
BP9003 BEAD-PROBE SM — DP_INT_ML_N<1> — R9014 1M 5% 1/20W MF 201
BP9004 BEAD-PROBE SM — DP_INT_ML_P<2> — R9015 1M 5% 1/20W MF 201
BP9005 BEAD-PROBE SM — DP_INT_ML_N<2> — R9016 1M 5% 1/20W MF 201
BP9006 BEAD-PROBE SM — DP_INT_ML_P<3> — R9017 1M 5% 1/20W MF 201
BP9007 BEAD-PROBE SM — DP_INT_ML_N<3> — R9018 1M 5% 1/20W MF 201

SYNC_MASTER=D1_SENSORS
SYNC_DATE=07/11/2012
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DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

8 =PP3V3_S0_DDCMUX

R9251 R9252 R9253 R9254
2.2K 1% 1/20W MF 201

C9280 0.1UF 20% 10V CERM 402

U9200
TS3DS10224
QFN
CRITICAL

69 OUT DP_TBTPA_DDC_CLK	1	INA+	
69 BI DP_TBTPA_DDC_DATA	2	INA-	
	16	ENA	
	13	VCC	
	20	OUTA1+	
	19	OUTA1-	
	18	OUTA0+	DP_TBTSNK0_DDC_CLK IN 9
	17	OUTA0-	DP_TBTSNK0_DDC_DATA BI 9
	14	SAI	
	15	SAO	
	10	ENB	
70 OUT DP_TBTPB_DDC_CLK	3	INB+	
70 BI DP_TBTPB_DDC_DATA	4	INB-	
	6	OUTB1+	
	7	OUTB1-	
	8	OUTB0+	DP_TBTSNK1_DDC_CLK IN 9
	9	OUTB0-	DP_TBTSNK1_DDC_DATA BI 9
33 IN TBT_DDC_XBAR_EN_L	12	SBI	
	11	SBO	
	5	GND	
	21	THRM PAD	

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP CER 4 7UF 10% 25V X5R 0603 MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices

=PP3V3_S4_TBTAPWRSW

CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM; CRITICAL C9480 22UF 20% 6.3V X5R-CERM 603; C9481 0.1UF 10% 16V X5R-CERM 0201

=PPHV_SW_TBTAPWRSW

18 9V Max

OMIT_TABLE

C9415 4.7UF 10% 25V X5R-CERM 0603; C9410 0.1UF 10% 25V X5R 402

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S 9 12 6V 7 5 11 7W)

U9410 CRITICAL CD3210A0RGP QFN

V3P3 V3P3OUT; VHV OUT; RSVD RSVD; EN; HV_EN; S0; ISET_V3P3; ISET_S0; ISET_S3; GND; THRM PAD

C9485 0.1UF 10% 16V X5R-CERM 0201; C9486 10UF 20% 6.3V CERM-X5R 0402; C9411 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

=TBTAPWRSW_EN
TBT_A_HV_EN_RC
=TBT_S0_EN

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

R9410 22.6K 1% 1/20W MF 201 <RHVS3> — TBTHV:P15V
R9411 22.6K 1% 1/20W MF 201 <RV3P3> — TBTHV:P15V
R9412 36.5K 1% 1/20W MF 201 <RV3P3>
R9413 22.6K 1% 1/20W MF 201 <RHVS3> — TBTHV:P15V
R9414 22.6K 1% 1/20W MF 201 <RHVS0> — TBTHV:P15V

12V See below

Single fault protection requires two R's per HV ISET Sx with CD3210
Single R on ISET V3P3 OK

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

PP3V3_SW_TBTAPWR

C9420 0.1UF 10% 16V X5R-CERM 0201; C9421 0.1UF 10% 16V X5R-CERM 0201

R9427 10K 5% 1/20W MF 201; R9429 100K 5% 1/20W MF 201

CRITICAL U9420 CBTL05023 HVQFN

SIGNAL_MODEL=TBT_MUX

TBT_A_CIO_SEL	1	BIASIN	BIASOUT 24
DP_AUXIO_EN	2	AUXIO_EN	
DP_TBTPA_AUXCH_C_N	7	AUX-	AUXIO- 23 — DP_A_AUXCH_DDC_N
DP_TBTPA_AUXCH_P	8	AUX+	AUXIO+ 22 — DP_A_AUXCH_DDC_P
DP_TBTPA_DDC_DATA	4	DDC_DAT	
DP_TBTPA_DDC_CLK	5	DDC_CLK	
TBT_A_CONFIG1_BUF	16	CA_DETOUT	CA_DET 18 — TBT_A_CONFIG1_RC
DP_TBTPA_ML_P<1>	11	DP+	DPML0+ 19 — DP_A_LSX_ML_P<1>
DP_TBTPA_ML_N<1>	10	DP-	DPML0- 20 — DP_A_LSX_ML_N<1>
TBT_A_LSTX	14	LSTX	
TBT_A_LSRX_UNBUF	13	LSRX	
TBT_A_DP_PWRDN	6	DP_PD	
DP_TBTPA_HPD	12	HPDOUT	HPD 17 — TBT_A_HPD
		GND THMPAD	

TBT_A_BIAS VOLTAGE=3.3V

C9425 0.1UF 10% 16V X5R-CERM 0201

TBT RX 1 Bias Sink

DP_TBTPA_AUXCH_C_N; DP_TBTPA_AUXCH_C_P — C9430 0.1UF; C9431 0.1UF

DP_TBTPA_ML_C_P<1>; DP_TBTPA_ML_C_N<1> — C9432 0.22UF 20% 6.3V X5R 0201; C9433 0.22UF

PP3V3_SW_TBTAPWR

CRITICAL U9460 74AUP1T97 SOT891

TBT_A_LSRX — Y = B

C9460 0.1UF 10% 16V X5R-CERM 0201

R9426 1M 5% 1/20W MF 201

R9428 100K 5% 1/20W MF 201

L9400 FERR-120-OHM-3A 0603 — PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C9400 0.01UF 10% 16V X7R-CERM 0402

TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

C9401 0.01UF 10% 50V X7R-CERM 0402

R9401 12 5% 1/20W MF 201

For J9400 TBT SMT pads (3 5 17 & 19)

CRITICAL J9400 MDP-D1 F-RT-TH SHIELD PINS

B2	HPD	GND0	B1
B4	CONFIG1	ML_LANE0P	B3
B6	CONFIG2	ML_LANE0N	B5
B8	GND2	GND1	B7
B10	ML_LANE3P	ML_LANE1P	B9
B12	ML_LANE3N	ML_LANE1N	B11
B14	GND4	GND3	B13
B16	AUX_CHP	ML_LANE2P	B15
B18	AUX_CHN	ML_LANE2N	B17
B20	DP_PWR	RETURN	B19

PORT B SHIELD PINS: S24 S22 S21 S20 S19 S18 S17; S16 S15 S14 S13 S12

514-0836

TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V

C9405 0.01UF 10% 25V X5R-CERM 0201

TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V

C9406 0.01UF 10% 25V X5R-CERM 0201

C9470 0.22UF 20% 6.3V X5R 0201; C9471 0.22UF — TBT_A_R2D_C_P<0>; TBT_A_R2D_C_N<0>

R9470 470K 5% 1/20W MF 201; R9471 470K

C9472 0.22UF 20% 6.3V X5R 0201; C9473 0.22UF — TBT_A_R2D_C_P<1>; TBT_A_R2D_C_N<1>

R9472 470K 5% 1/20W MF 201; R9473 470K

TBT_A_R2D_P<0>; TBT_A_R2D_N<0> — C9474 0.47UF 20% 4V CERM-X5R-201; C9475 0.47UF

TBT_A_R2D_C_P<0>; TBT_A_R2D_C_N<0>

R9494 1K 5% 1/20W MF 201; R9495 1K 5% 1/20W MF 201

DP_TBTPA_ML_C_P<3>; DP_TBTPA_ML_C_N<3> — C9478 0.22UF 20% 6.3V X5R 0201; C9479 0.22UF

DP_TBTPA_ML_P<3>; DP_TBTPA_ML_N<3>

R9478 470K 5% 1/20W MF 201; R9479 470K 5% 1/20W MF 201

TBT Unused

TBT_A_BIAS

R9498 2.2K 5% 1/20W MF 201; R9499 2.2K 5% 1/20W MF 201

TBT_A_D2R_P<1>; TBT_A_D2R_N<1> — C9476 0.47UF 20% 4V CERM-X5R-201; C9477 0.47UF

TBT_A_D2R_C_P<1>; TBT_A_D2R_C_N<1>

CRITICAL SIGNAL_MODEL=TBTPIN GND VOID TRUE

D9498 BAR90-02LRH TSLP-2-7 — TBT_A_D2R1_AUXDDC_P
D9499 BAR90-02LRH TSLP-2-7 — TBT_A_D2R1_AUXDDC_N

CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603

DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N

C9498 30PF 5% 25V C0G-CERM 0201; C9499 30PF

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201; R9451 1M 5% 1/20W MF 201

C9494 330PF 10% 16V X7R-CERM 0201; C9495 330PF

R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1 1a)

Sink HPD range
High 2 0 5 0V
Low 0 0 8V

TBT_A_D2R_P<0>; TBT_A_D2R_N<0> — C9474 0.47UF 20% 4V CERM-X5R-201; C9475 0.47UF

TBT_A_D2R_C_P<0>; TBT_A_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201; R9495 1K 5% 1/20W MF 201

TBT_A_D2R_P<1>; TBT_A_D2R_N<1> — C9476 0.47UF 20% 4V CERM-X5R-201; C9477 0.47UF

TBT_A_D2R_C_P<1>; TBT_A_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7 — TBT_A_D2R1_AUXDDC_P
D9499 BAR90-02LRH TSLP-2-7 — TBT_A_D2R1_AUXDDC_N

CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603

DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N

C9498 30PF 5% 25V C0G-CERM 0201; C9499 30PF

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

R9452 1M 5% 1/20W MF 201; R9451 1M 5% 1/20W MF 201

C9494 330PF 10% 16V X7R-CERM 0201; C9495 330PF

R9441 100K 5% 1/20W MF 201

C9402 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1 1a)

Sink HPD range
High 2 0 5 0V
Low 0 0 8V

TBT_A_R2D_P<0>; TBT_A_R2D_N<0> — TBT TX 0

TBT_A_R2D_P<1>; TBT_A_R2D_N<1> — TBT TX 1

DP_A_LSX_ML_P<1>; DP_A_LSX_ML_N<1> — TBT LSX R2P/P2R (P/N)

470k R's for ESD protection on AC coupled signals

SYNC MASTER=J5 MLB KEPLER SYNC DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <Preliminary Test> SIZE: C

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP CER 4 7UF 10% 25V X5R 0603 MURATA	C9615	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices

=PP3V3_S4_TBTBPWRSW

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S 9 12 6V 7 5 11 7W)

CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM; C9680 22UF 20% 6.3V X5R-CERM 603; C9681 0.1UF 10% 16V X5R-CERM 0201

=PPHV_SW_TBTBPWRSW 18V Max

OMIT_TABLE

C9615 4.7UF 10% 25V X5R-CERM 0603; C9610 0.1UF 10% 25V X5R 402

CRITICAL U9610 CD3210A0RGP QFN

19, 20	V3P3	V3P3OUT	18
6, 7	VHV	OUT	12, 14
16	RSVD	RSVD	15
5	EN	ISET_V3P3	8
11	HV_EN	ISET_S0	10
17	S0	ISET_S3	9
GND		THRM PAD	1 2 3 4 13 21

C9685 0.1UF 10% 16V X5R-CERM 0201; C9686 10UF 20% 6.3V CERM-X5R 0402; C9611 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V

PPHV_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

=TBTBPWRSW_EN
TBT_B_HV_EN_RC
=TBT_S0_EN

TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R

TBTHV:P15V R9610 22.6K 1% 1/20W MF 201 <RV3P3>
TBTHV:P15V R9611 22.6K 1% 1/20W MF 201
R9612 36.5K 1% 1/20W MF 201 <RV3P3>
TBTHV:P15V R9613 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R9614 22.6K 1% 1/20W MF 201 <RHVS0>

12V See below

Single fault protection requires two R's per HV ISET Sx with CD3210
Single R on ISET V3P3 OK

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

PP3V3_SW_TBTBPWR

C9620 0.1UF 10% 16V X5R-CERM 0201; C9621 0.1UF 10% 16V X5R-CERM 0201

R9627 10K 5% 1/20W MF 201; R9629 100K 5% 1/20W MF 201

CRITICAL U9620 CBTL05023 HVQFN

SIGNAL_MODEL=TBT_MUX

TBT_B_CIO_SEL	33	BIASIN	1
DP_AUXIO_EN	69 25	AUXIO_EN	2
DP_TBTPB_AUXCH_C_N	76 33	AUX-	7
DP_TBTPB_AUXCH_C_P	76 33	AUX+	8
DP_TBTPB_DDC_DATA	68	DDC_DAT	4
DP_TBTPB_DDC_CLK	68	DDC_CLK	5
TBT_B_CONFIG1_BUF	OUT	CA_DETOUT	16
DP_TBTPB_ML_C_P<1>	76 33	DP+	11
DP_TBTPB_ML_C_N<1>	76 33	DP-	10
TBT_B_LSTX	33	LSTX	14
TBT_B_LSRX_UNBUF		LSRX	13
TBT_B_DP_PWRDN	33	DP_PD	6
DP_TBTPB_HPD	33 OUT	HPDOUT	12
		BIASOUT	24
		AUXIO-	23
		AUXIO+	22
		CA_DET	18
		DPML0+	19
		DPML0-	20
		HPD	17
		VDD	3 15
		GND THMPAD	9 21 25

TBT_B_BIAS VOLTAGE=3.3V — C9625 0.1UF 10% 16V X5R-CERM 0201

TBT_B_AUXCH_DDC_N — TBT RX 1 Bias Sink

TBT_B_AUXCH_DDC_P

TBT_B_CONFIG1_RC

TBT_B_LSX_ML_P<1>

TBT_B_LSX_ML_N<1> — TBT LSX A R2P/P2R (P/N)

TBT_B_HPD

C9630 0.1UF 10% 16V X5R-CERM 0201; C9631 0.1UF 10% 16V X5R-CERM 0201

C9632 0.22UF 20% 6.3V X5R 0201; C9633 0.22UF 20% 6.3V X5R 0201

PP3V3_SW_TBTBPWR

CRITICAL U9660 74AUP1T97 SOT891

TBT_B_LSRX — Y = B

C9660 0.1UF 10% 16V X5R-CERM 0201

R9626 1M 5% 1/20W MF 201; R9628 100K 5% 1/20W MF 201

L9600 FERR-120-OHM-3A 0603 — PP3V3RHV_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

C9600 0.01UF 10% 16V X7R-CERM 0402; C9601 0.01UF 10% 16V X7R-CERM 0402

TBTBCONN_20_RC — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V

R9601 12 5% 1/20W MF 201

For J9600 TBT SMT pads (3 5 17 & 19)

TBTBCONN_1_C — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V

C9605 0.01UF 10% 25V X5R-CERM 0201

C9606 0.01UF 10% 25V X5R-CERM 0201

TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>

TBT Dir — DP Dir — TBT TX 0 — TBT TX 1 — (0 18 9V)

C9670 0.22UF 20% 6.3V X5R 0201; C9671 0.22UF 20% 6.3V X5R 0201

R9670 470K 5% 1/20W MF 201; R9671 470K 5% 1/20W MF 201

C9672 0.22UF 20% 6.3V X5R 0201; C9673 0.22UF 20% 6.3V X5R 0201

R9672 470K 5% 1/20W MF 201; R9673 470K 5% 1/20W MF 201

470k R's for ESD protection on AC coupled signals

CRITICAL J9400 MDP-D1 F-RT-TH SHIELD PINS

A2	HPD	GND0	A1
A4	CONFIG1	ML_LANE0P	A3
A6	CONFIG2	ML_LANE0N	A5
A8	GND2	GND1	A7
A10	ML_LANE3P	ML_LANE1P	A9
A12	ML_LANE3N	ML_LANE1N	A11
A14	GND4	GND3	A13
A16	AUX_CHP	ML_LANE2P	A15
A18	AUX_CHN	ML_LANE2N	A17
A20	DP_PWR	RETURN	A19

PORT A SHIELD PINS: S23 S11 S10 S9 S8 S7 S6

514-0836

TBT_B_D2R_P<0> — C9674 0.47UF 20% 4V CERM-X5R-201
TBT_B_D2R_N<0> — C9675 0.47UF 20% 4V CERM-X5R-201

R9694 1K 5% 1/20W MF 201; R9695 1K 5% 1/20W MF 201

DP_TBTPB_ML_C_P<3> — C9678 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_N<3> — C9679 0.22UF 20% 6.3V X5R 0201

R9678 470K 5% 1/20W MF 201; R9679 470K 5% 1/20W MF 201

TBT Unused

TBT_B_BIAS

R9698 2.2K 5% 1/20W MF 201; R9699 2.2K 5% 1/20W MF 201

TBT_B_D2R_P<1> — C9676 0.47UF 20% 4V CERM-X5R-201
TBT_B_D2R_N<1> — C9677 0.47UF 20% 4V CERM-X5R-201

CRITICAL D9698 BAR90-02LRH TSLP-2-7; D9699 BAR90-02LRH TSLP-2-7 — SIGNAL_MODEL=TRPIN

TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N

CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603

DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N

C9698 30PF 5% 25V C0G-CERM 0201; C9699 30PF 5% 25V C0G-CERM 0201

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC

R9652 1M 1% 1/20W MF 201; R9651 1M 1% 1/20W MF 201

C9694 330PF 10% 16V X7R-CERM 0201; C9695 330PF 10% 16V X7R-CERM 0201

R9641 100K 5% 1/20W MF 201

C9602 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1 1a)

Sink HPD range
High 2 0 5 0V
Low 0 0 8V

SYNC_MASTER=J5_MLB_KEPLER — SYNC_DATE=11/14/2011

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Apple Inc.

DRAWING NUMBER: <Preliminary Test> — SIZE: C

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PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)

=PPBUS_S0_LCDBKLT

F9700 3AMP-32V-467 603-HF BOTTOM

PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL Q9706 FDC638APZ_SBMS001 SSOT6-HF

PPBUS_SW_LCDBKLT_PWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

HERE IS A SENSE RESISTOR BETWEEN PPBUS_SW_LCDBKLT_PWR AND PPBUS_SW_BKL ON THE SENSOR PAGE

NEED VALUE CHANGES FOR 55V AND 96 LEDS !!!

R9788 301K 1% 1/16W MF-LF 402

C9782 0.1UF 10% 16V X7R-CERM 0402

LCDBKLT_EN_DIV

R9789 147K 1% 1/16W MF-LF 402

LCDBKLT_EN_L

Q9707 SSM6N15AFE SOT563

LCD_BKLT_EN

LCDBKLT_DISABLE

Q9707 SSM6N15AFE SOT563

BKLT_PLT_RST_L

=PP5V_S0_BKL

*L9710, Q9701, D9701, C9715-C9719 SHOULD ALL BE PLACED NEAR EACH OTHER.

CRITICAL L9710 22UH-20%-2.4A-0.105OHM 152S1527
VOLTAGE=12.6V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM

CRITICAL D9701 POWERDI-123 DFLS260
VOLTAGE=50V

NEED TO BE CHANGED TO 37150704

C9715, C9716 SHOULD BE PLACED IN T-BONE. SAME FOR C9718,C9719
C9715, C9716 SHOULD BE PLACED ON TOP SIDE. PLACE C9718,C9719 ON BOTTOM SIDE

PPBUS_S0_LCDBKLT_PWR

CRITICAL C9712 10UF 20% 25V X5R 805

C9713 0.1UF 10% 16V X5R 402

PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE

CRITICAL C9715 2.2UF 10% 25V X7R-CERM 1210
CRITICAL C9716 2.2UF 10% 25V X7R-CERM 1210
CRITICAL C9718 2.2UF 10% 25V X7R-CERM 1210
CRITICAL C9719 2.2UF 10% 25V X7R-CERM 1210
C9717 1000PF 10% 100V X7R-CERM 0603

PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=55V

=PP3V3_S0_BKL_VDDIO

C9714 0.01UF 10% 16V X7R-CERM 0402
C9710 1UF 10% 16V X5R 603-1
C9711 0.1UF 10% 16V X7R-CERM 0402

CRITICAL Q9701 SI7308DN PWRPK-1212-8

BKL_FET_CNTL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM

R9708 63.4K 1% 1/10W MF-LF 402

R9709 59.0K 1% 1/10W MF-LF 402

LCDBKLT:ENG

U9701 LP8545SQX-EXTJ LLP

VDDIO VLDO VIN
GD FSET FILTER ISET SCLK SDA PWM FAULT EN
SW FB OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 VSYNC
GND_SW GND_S GND_L THRM PAD

BKL_SW
BKL_FB
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
BKL_VSYNC_R
BKL_FSET
BKL_FLT
BKL_ISET
BKL_SCL
BKL_SDA
LVDS_BKL_PWM_RC
TP_BKL_FAULT
BKL_EN

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

R9717-R9722 CAN BE 0OHM IN PRODUCTION, ADD BOM OPTION

R9717 10.2 0.1% 1/16W TF 402 — LED_RETURN_1
R9718 10.2 0.1% 1/16W TF 402 — LED_RETURN_2
R9719 10.2 0.1% 1/16W TF 402 — LED_RETURN_3
R9720 10.2 0.1% 1/16W TF 402 — LED_RETURN_4
R9721 10.2 0.1% 1/16W TF 402 — LED_RETURN_5
R9722 10.2 0.1% 1/16W TF 402 — LED_RETURN_6

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.20 mm

R9753 AND R9757 NEED TO BE 402 PACK FOR LAB ACCESS

=I2C_BKL_1_SCL R9753 0 5% 1/16W MF-LF 402

=I2C_BKL_1_SDA R9757 0 5% 1/16W MF-LF 402

PPBUS_S0_LCDBKLT_PWR

R9731 301K 1% 1/16W MF-LF 402

R9715 100K 1% 1/16W MF-LF 402

R9704 0 5% 1/16W MF-LF 402

LCD_BKLT_PWM

LCD_BKLT_PWM SHOULD BE KEPT AWAY FROM BOOST CIRCUIT

NO STUFF C9704 33PF 5% 50V C0G CERM 402

(EEPROM should set EN_I_RES=1)

R9714 16.2K 1% 1/16W MF-LF 402
I_LED=22.7MA
I_LED=369/Riset

R9716 FPWM=19.2KHZ 12.7K details in spec 1% 1/16W MF-LF 402

R9765 10K 5% 1/16W MF-LF 402

R9755 10K 5% 1/16W MF-LF 402

(APN: 353S3376)
PWM RES = 9+3

XW9710 SM

BKL_SGND

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

PLACE XW9710 AWAY FROM U9701.1 AND U9701.15
ADD VIAS IN TPAD OF U9701

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES MTL FILM 1/16W 0 5 0402 SMD LF	R9717,R9718,R9719,R9720,R9721,R9722	CRITICAL	LCDBKLT:PROD

SYNC MASTER=J5 MLB KEPLER
SYNC DATE=09/21/201

PAGE TITLE
LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER <Preliminary Test>
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	=4X_DIELECTRIC	?
CPU_ITP	*	=4x_DIELECTRIC	?
CPU_VCCSENSE	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X DIELECTRIC	?
CLK PCIE	*	=5X DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	7 10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	7 10 18
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	10 18
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	10 18
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	7 11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	7 11 17
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_P	11 17
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_N	11 17
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_BRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 39
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 40
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 39 40 61
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 61
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 61
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 61
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 58
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

SYNC_MASTER_J5_MLB SYNC_DATE 09/13/2012

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM 37S	*	=37 OHM SE	=37 OHM SE	=37 OHM SE	=37 OHM SE	=STANDARD	=STANDARD
MEM 40S	*	=40 OHM SE	=40 OHM SE	=40 OHM SE	=40 OHM SE	=STANDARD	=STANDARD
MEM 72D	*	72 OHM DIFF	=72 OHM DIFF	=72 OHM DIFF	=72 OHM DIFF	=72 OHM DIFF	=72 OHM DIFF
MEM 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
MEM 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM CLK2MEM	*	=4X DIELECTRIC	?
MEM CTRL2CTRL	*	=3X DIELECTRIC	?
MEM CTRL2MEM	*	=3X DIELECTRIC	?
MEM CMD2CMD	*	=2X DIELECTRIC	?
MEM CMD2MEM	*	=3X DIELECTRIC	?
MEM DATA2DATA	*	=2X DIELECTRIC	?
MEM DATA2MEM	*	=3X DIELECTRIC	?
MEM DQS2MEM	*	=4X DIELECTRIC	?
MEM 2OTHER	*	=6X DIELECTRIC	?
MEM DQBL2BL	*	=4X DIELECTRIC	?
MEM DQCH2CH	*	=6X DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CLK	MEM *	*	MEM CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CMD	MEM *	*	MEM CMD2MEM
MEM CMD	MEM CMD	*	MEM CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM CTRL	MEM *	*	MEM CTRL2MEM
MEM CTRL	MEM CTRL	*	MEM CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM DQS	MEM *	*	MEM DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM *	*	*	MEM 2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM * DQ BYTE*	MEM *	*	MEM DATA2MEM
MEM * DQ BYTE*	=SAME	*	MEM DATA2DATA
MEM A DQ BYTE*	MEM A DQ BYTE*	*	MEM DQBL2BL
MEM B DQ BYTE*	MEM B DQ BYTE*	*	MEM DQBL2BL
MEM A DQ BYTE*	MEM B DQ BYTE*	*	MEM DQCH2CH

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<0>	12 28 30
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A CKE<1..0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A CS L<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A CS L<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A ODT<1>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A ODT<0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	12 28 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM A DQ<7..0>	7 12 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM A DQ<15..8>	7 12 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM A DQ<23..16>	7 12 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM A DQ<31..24>	7 12 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM A DQ<39..32>	7 12 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM A DQ<47..40>	7 12 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM A DQ<55..48>	7 12 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM A DQ<63..56>	7 12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	12 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<0>	12 29 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B CKE<1>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B CKE<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B ODT<1..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	12 29 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM B DQ<7..0>	7 12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM B DQ<15..8>	7 12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM B DQ<23..16>	7 12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM B DQ<31..24>	7 12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM B DQ<39..32>	7 12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM B DQ<47..40>	7 12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM B DQ<55..48>	7 12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM B DQ<63..56>	7 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	12 29

SYNC_MASTER=J5_MLB SYNC_DATE=09/13/2013

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Digital Video Signal Constraints

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 90D	*	90_OHM_DIFF	90 OHM DIFF	90 OHM DIFF	90 OHM DIFF	90 OHM DIFF	90 OHM DIFF
SATA 37SE	*	37_OHM_SE	37 OHM SE	37 OHM SE	37 OHM SE	37 OHM SE	37 OHM SE
SATA 50SE	*	50_OHM_SE	50 OHM SE	50 OHM SE	50 OHM SE	50 OHM SE	50 OHM SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	5 1 SPACING	?
SATA ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP BOTTOM	5 1 SPACING	?

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USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH USB RBIAS	*	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD	STANDARD
USB 85D	*	85_OHM_DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	4 1 SPACING	?
USB RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	4 1 SPACING	?

SOURCE HR PLATFORM DESIGN GUIDE TABLES 191 193

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3 85D	*	85_OHM_DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	5 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP BOTTOM	5 1 SPACING	?

SOURCE CR SFF PLATFORM DESIGN GUIDE V0 7 TABLE 4 211 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD
CLK 25M 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	=2x DIELECTRIC	?
CLK 25M	*	=5x DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
			NET TYPE
T25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_P 7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_N 7
T25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_P 7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_N 7
T25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_P 7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_N 7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_N 7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_P 7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_P 7 37
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_N 7 37
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_N 7 37
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_P 7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P 7 17 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N 7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P 7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N 7 17 37
T232 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_P 7 37
T233 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_N 7 37
T234 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_P 7 37
T235 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_N 7 37
T33 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP 17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP 17
T236 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P 19 26
T237 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N 19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_P 19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_N 19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P 19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_N 19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P 19 38
USB_EXTA	USB_85D	USB	USB_EXTA_N 19 38
USB_EXTB	USB_85D	USB	USB_EXTB_P 7 26 36
USB_EXTB	USB_85D	USB	USB_EXTB_N 7 26 36
USB_EXTC	USB_85D	USB	USB_EXTD_P
USB_EXTC	USB_85D	USB	USB_EXTD_N
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P 7 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N 7 32
USB_BT	USB_85D	USB	USB_BT_P 7 9 36
USB_BT	USB_85D	USB	USB_BT_N 7 9 36
USB_TPAD	USB_85D	USB	USB_TPAD_P 9 47
USB_TPAD	USB_85D	USB	USB_TPAD_N 9 47
USB_SMC	USB_85D	USB	USB_SMC_P 9 39
USB_SMC	USB_85D	USB	USB_SMC_N 9 39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS 19
T238 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_P 19 26
T239 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_N 19 26
T245 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P 38
T244 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N 38
T247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P 19 32
T246 USB_CAMERA	USB_85D	USB	USB_CAMERA_N 19 32
T245 USB_EXTA	USB_85D	USB	USB_LT1_P 7 38
T243 USB_EXTA	USB_85D	USB	USB_LT1_N 7 38
T221 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_P 19 36
T221 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_N 19 36
T222 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_P 7 19 36
T223 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_N 7 19 36
T230 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_P 19 38
T229 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_N 7 19 38
T228 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_P 7 19 38
T231 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_N 7 19 38

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
			NET TYPE
T206 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC 17 25
T205 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB 17 25
T204	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R 17
T203 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET
T202	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R
T201 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT 25 33
T200	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R 33

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD
CLK LPC 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 50S	*	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	7 17 39 41
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	7 17 39 41
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	19 25
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	7 25 39
	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	7 25 41
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	7 17 42
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	7 17 42
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	17 42
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	17 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SML_PCH_1_CLK	17 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SML_PCH_1_DATA	17 42
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	17 51
	HDA_50S	HDA	HDA_BIT_CLK_R	17
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	17 51
	HDA_50S	HDA	HDA_SYNC_R	17
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	17
	HDA_50S	HDA	HDA_RST_L	17 51
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	17 51
	HDA_50S	HDA	AUD_SDI_R	51
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	17 51
	HDA_50S	HDA	HDA_SDOUT_R	17 25
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	17 41
	SPI_55S	SPI	SPI_CLK	41
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	17 41
	SPI_55S	SPI	SPI_MOSI	41
SPI_MISO	SPI_55S	SPI	SPI_MISO	17 41
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	17 41
	SPI_55S	SPI	SPI_CS0_L	41
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	7 17 36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	7 17 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_P	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_N	7 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	7 17 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_N	7 17 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	7 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	7 36
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	7 17
PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	7 17
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_P	7 17 33
PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_TBT_N	7 17 33
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	17
PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	7 17
PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	17
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	17
	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	7 17 25
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_P	7 9 17
PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_SSD_N	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	7 9 17
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	7 9 17
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 17 36
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	7 17 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	7 17 36
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	7 9 17
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	7 9 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	7 17
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	7 17
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_P<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_C_N<3..0>	7 9 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_P<3..0>	7 33
PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE_TBT_R2D_N<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_P<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_N<3..0>	7 9 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_P<3..0>	7 33
PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE_TBT_D2R_C_N<3..0>	7 33

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2013

PAGE TITLE: PCH Constraints 2

Apple Inc.

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING	
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL 7 39 42
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA 7 39 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL 7 39 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA 7 39 42
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL 39 42
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA 39 42
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL 39 42
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA 39 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING	
CHGR_CSI_P	1TO1_DIFFPAIR		CHGR_CSI_P 57
CHGR_CSI_N	1TO1_DIFFPAIR		CHGR_CSI_N 57
CHGR_CSO_P	1TO1_DIFFPAIR		CHGR_CSO_P 57
CHGR_CSO_N	1TO1_DIFFPAIR		CHGR_CSO_N 57

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING		
TBT_A_R2D_C_P<1..0>	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0> 7 33 69	
TBT_A_R2D_C_N<1..0>	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0> 7 33 69	
TBT_A_R2D_P<1..0>	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0> 7 69	
TBT_A_R2D_N<1..0>	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0> 7 69	
DP_TBTPA_ML_C_P<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2> 33 69	
DP_TBTPA_ML_C_N<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2> 33 69	
DP_TBTPA_ML_P<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2> 69	
DP_TBTPA_ML_N<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2> 69	
DP_LSX_ML_P<1>	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 69	
DP_LSX_ML_N<1>	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 69	
TBT_A_D2R1_C_P<1>	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1> 7 69	
TBT_A_D2R1_C_N<1>	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1> 7 69	
TBT_A_D2R0_C_P<0>	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<0> 7 69	
TBT_A_D2R0_C_N<0>	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<0> 7 69	
TBT_A_D2R1_P<1>	TBTDP_85D	TBTDP	TBT_A_D2R_P<1> 7 33 69	
TBT_A_D2R1_N<1>	TBTDP_85D	TBTDP	TBT_A_D2R_N<1> 7 33 69	
TBT_A_D2R0_P<0>	TBTDP_85D	TBTDP	TBT_A_D2R_P<0> 7 33 69	
TBT_A_D2R0_N<0>	TBTDP_85D	TBTDP	TBT_A_D2R_N<0> 7 33 69	
TBT_A_AUXCH_C_P	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P 33 69	
TBT_A_AUXCH_C_N	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N 33 69	
TBT_A_AUXCH_P	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P 69	
TBT_A_AUXCH_N	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N 69	
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P 69	
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N 69	
TBT_A_D2R1_AUXDDC_P	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P 69	
TBT_A_D2R1_AUXDDC_N	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N 69	
TBT_B_R2D_C_P<1..0>	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0> 7 33 70	Only used on dual-port hosts.
TBT_B_R2D_C_N<1..0>	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0> 7 33 70	
TBT_B_R2D_P<1..0>	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0> 7 70	
TBT_B_R2D_N<1..0>	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0> 7 70	
DP_TBTPB_ML_C_P<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2> 33 70	
DP_TBTPB_ML_C_N<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2> 33 70	
DP_TBTPB_ML_P<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2> 70	
DP_TBTPB_ML_N<3..1:2>	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2> 70	
DP_LSX_ML_P<1>	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 70	
DP_LSX_ML_N<1>	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 70	
TBT_A_D2R0_C_P<0>	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<0> 7 70	
TBT_A_D2R0_C_N<0>	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<0> 7 70	
TBT_A_D2R1_C_P<1>	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1> 7 70	
TBT_A_D2R1_C_N<1>	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1> 7 70	
TBT_A_D2R0_P<0>	TBTDP_85D	TBTDP	TBT_B_D2R_P<0> 7 33 70	
TBT_A_D2R0_N<0>	TBTDP_85D	TBTDP	TBT_B_D2R_N<0> 7 33 70	
TBT_A_D2R1_P<1>	TBTDP_85D	TBTDP	TBT_B_D2R_P<1> 7 33 70	
TBT_A_D2R1_N<1>	TBTDP_85D	TBTDP	TBT_B_D2R_N<1> 7 33 70	
TBT_B_AUXCH_C_P	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P 33 70	
TBT_B_AUXCH_C_N	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N 33 70	
TBT_B_AUXCH_P	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P 70	
TBT_B_AUXCH_N	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N 70	
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P 70	
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N 70	
TBT_A_D2R1_AUXDDC_P	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P 70	
TBT_A_D2R1_AUXDDC_N	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N 70	

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	Only used on hosts supporting Thunderbolt video-in
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK 33	
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI 33	
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO 33	
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L 33	

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PAGE TITLE
Thunderbolt & SMC Constraints

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Apple Inc.

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REVISION <no_LABEL>

BRANCH

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations
Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

Graphics, SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_P	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_N	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_P	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_N	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_N	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	58 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	58 80
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_P	7 9 36
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_N	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_P<2..0>	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_N<2..0>	7 9 36

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE PHYSICAL	NET TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 36
	1TO1_DIFFPAIR		CHGR_CSI_R_P	57
	1TO1_DIFFPAIR		CHGR_CSI_R_N	57
	1TO1_DIFFPAIR		CHGR_CSO_R_P	57
	1TO1_DIFFPAIR		CHGR_CSO_R_N	57
USB_BT	USB_85D	USB	USB_BT_CONN_P	36
USB_BT	USB_85D	USB	USB_BT_CONN_N	36
USB_BT	USB_85D	USB	USB_BT_WAKE_P	36
USB_BT	USB_85D	USB	USB_BT_WAKE_N	36
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	43
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	26 47
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	26 47
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_P	9
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_N	9
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
		SB_POWER	PP1V5_S3RS0_CPUDDR	8
		GND	GND	

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PAGE TITLE
Project Specific Constraints

Apple Inc.

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D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_MEM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3 ISL4 ISL9 ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

Stackup-Defined Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP BOTTOM	0.1 MM	?
1:1_SPACING	ISL3 ISL4 ISL9 ISL10	0.1 MM	?
1:1_SPACING	ISL5 ISL6 ISL7 ISL8 ISL11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3 ISL4 ISL9 ISL10	0.053 MM	?
1x_DIELECTRIC	ISL5 ISL6 ISL7 ISL8 ISL11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET TYPE	
J4P1 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 33
J4P2 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 33
J4P5 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 33
J4P6 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 33
J4P3 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 33
J4P4 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 33
J4P7 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 33
J4P8 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 33
J4P9 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	33
J4P11 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	33
J4P12 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	33
J4P13 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	33
J4P15 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	33
J4P17 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	33
J4P16 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	33
J4P18 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	33
J4P62 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	9 67
J4P64 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	9 67
J4P59 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	9 67
J4P69 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	9 67
J4P57 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 67
J4P58 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 67
J4P56 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67
J4P55 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67
J4P54 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	
J4P53 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	
J4P41 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_P	7 36
J4P42 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_N	7 36
J4P43 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_P	7 38
J4P44 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_N	7 38
J4P45 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_P	7 38
J4P46 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_N	7 38
J4P47 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
J4P48 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36

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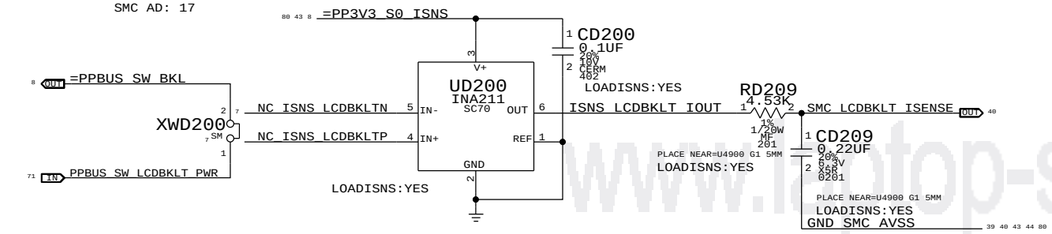
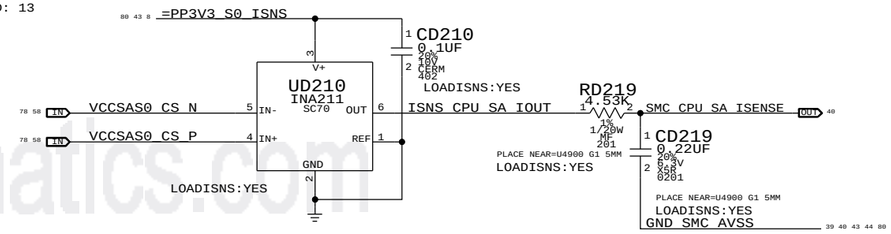
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



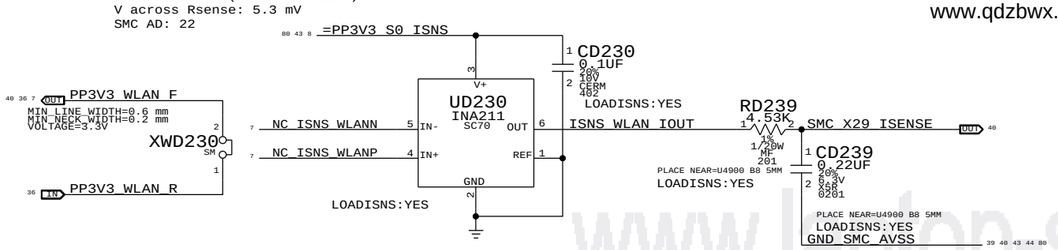
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



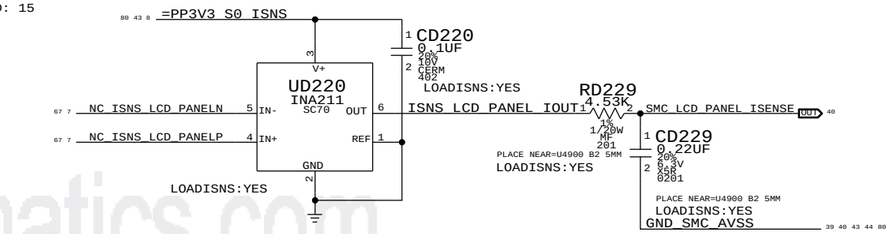
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



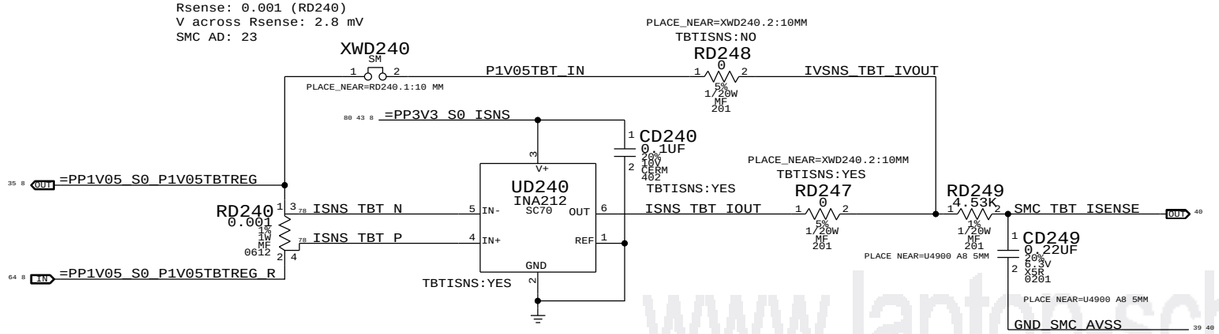
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



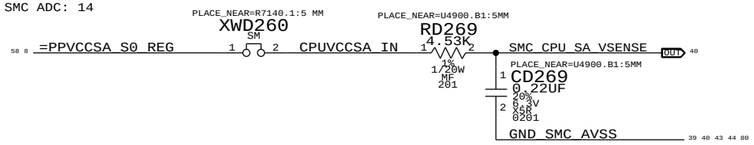
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



CPU SA Voltage Sense (VC2C)

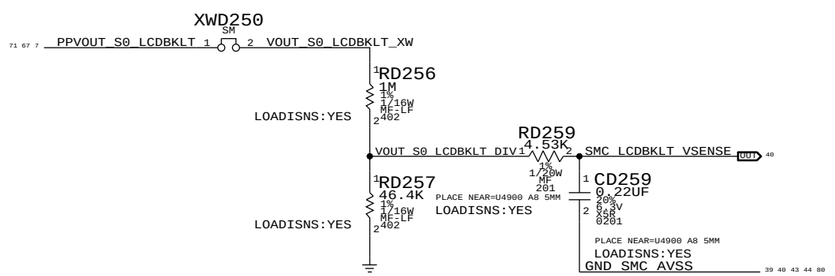
Gain: 1x
SMC ADC: 14



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



SYNC MASTER=01 SENSORS
SYNC DATE=07/11/2012

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