1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0001395489	ENGINEERING RELEASED	2012-03-13

SCHEM,MLB,J30

03/12/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9058	1	SCHEM,MLB,J30	SCH	CRITICAL	
820-3115	1	PCBF,MLB,J30	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Mar 13 14:00:17 2012

DRAWING TITLE: SCHEM,MLB,J30

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D
REVISION: 6.0.0
BRANCH:
PAGE: 1 OF 109
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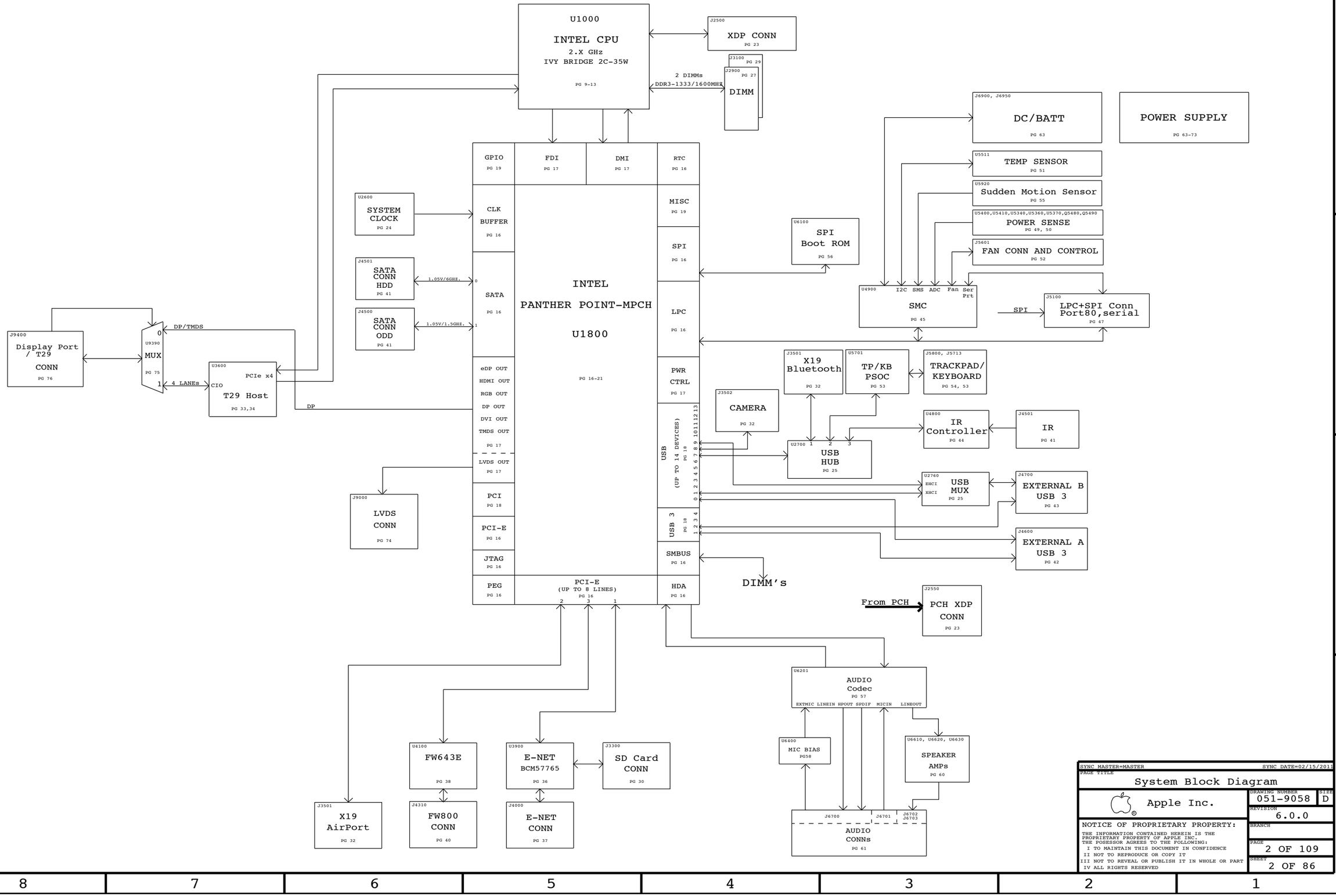

SYNC MASTER=MASTER SYNC DATE=02/15/2011

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System Block Diagram

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DRAWING NUMBER 051-9058 SIZE D

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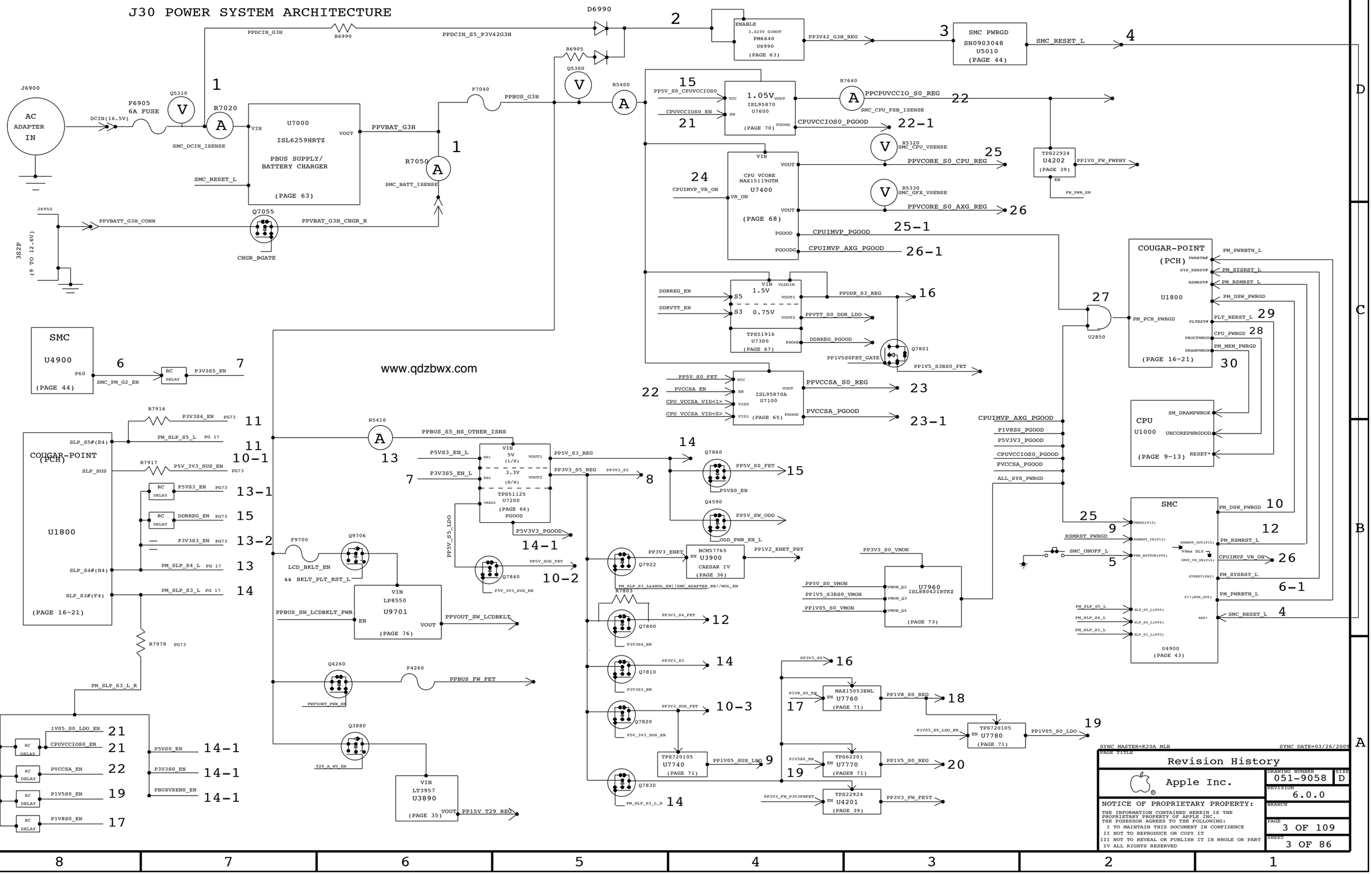
J30 POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
607-8895	CMN PTS,PCBA,MLB,J30	J30_COMMON,FET_PAIR
085-3092	J30 MLB DEVELOPMENT BOM	J30_DEVEL:ENG
607-8721	POWER FETS PAIR,FAIRCHILD,DDR,J30	DDR_POWER_FET:FAIR
607-8722	POWER FETS PAIR,FAIRCHILD,5V_S3,J30	5V_S3_POWER_FET:FAIR
607-8723	POWER FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CHARGER_POWER_FET:FAIR
607-9309	POWER FETS PAIR,RENESAS,DDR,J30	DDR_POWER_FET:REN
607-9310	POWER FETS PAIR,RENESAS,5V_S3,J30	5V_S3_POWER_FET:REN
607-9311	POWER FETS PAIR,RENESAS,PBUS_CHARGER,J30	CHARGER_POWER_FET:REN
639-3752	PCBA,MLB,MOL,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:MOLEX,EEEE_F1YK
639-3756	PCBA,MLB,HYB,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:HYBRID,EEEE_F1YH
639-3753	PCBA,MLB,FOX,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:FOXCONN,EEEE_F1YL
639-3755	PCBA,MLB,HYB,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:HYBRID,EEEE_F1YJ
639-3751	PCBA,MLB,MOL,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:MOLEX,EEEE_F1YM
639-3754	PCBA,MLB,FOX,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:FOXCONN,EEEE_F1YG

J30 BOM GROUPS

BOM GROUP	BOM OPTIONS
J30_COMMON	ALTERNATE,COMMON,J30_COMMON1,J30_COMMON2,J30_DEBUG:ENG,J30_PROGPARTS,T29BST:Y,TBTHV:P15V
J30_COMMON1	BATT_3S,CPUMEM_S0,USBHUB2513B,HUB_3NONREM,T29:YES,SDRV_PD,SDRVI2C:MCU,AXG_PHASE1,BTPWR:S4,UV_GLUE_J30
J30_COMMON2	MIKEY,TPAD:Z2,RAMCFG_SLOT
J30_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
J30_DEVEL:ENG	BKLT:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS_CONN:YES,LOADISNS:YES,DDRVREF_DAC,S0PGOOD_ISL
J30_DEVEL:PVT	LPCPLUS_CONN:YES,XDP_CONN
J30_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,LPCPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO_DAC
J30_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2514B
J30_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCPLUS_R:YES,LOADISNS:NO,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2513B

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4113	1	IC,IVB,2C,35W,1023BGA	U1000	CRITICAL	CPU_IVB_2C
337S4264	1	IVB,S R0N0,PRQ,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4265	1	IVB,S R0MU,PRQ,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_2_9GHZ
337S4269	1	PANTHERPOINT,C1,SLJ8C,PRQ,BD82HM77	U1800	CRITICAL	
343S0534	1	IC,BCM57765B0,ENET&SD,8X8	U3900	CRITICAL	
338S0753	1	IC,FW643E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S1072	1	IC,T29,PRQ,S LJJY,FCBGA,15x15MM,C1	U3600	CRITICAL	T29:YES
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
946-3827	1	J30 MLB DYMAX ADHESIVE 29993-SC 0.48G	UV_GLUE_J30	CRITICAL	UV_GLUE_J30
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,DDR3,P=0.6MM,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,DDR3,P=0.6MM,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,DDR3,P=0.6MM,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YG]	CRITICAL	EEEE_F1YG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YH]	CRITICAL	EEEE_F1YH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YJ]	CRITICAL	EEEE_F1YJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YK]	CRITICAL	EEEE_F1YK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YL]	CRITICAL	EEEE_F1YL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YM]	CRITICAL	EEEE_F1YM

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0862	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,REV F	U3990	CRITICAL	ENET_BLANK
341S3096	1	IC ENET,1|MBITFLAH,CIV REV01,K9x	U3990	CRITICAL	ENET_PROG
335S0550	1	IC,EEPROM,SERIAL,SPI,4Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341S3430	1	IC,T29 EEPROM,LR,J30/J31	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S3365	1	IC,PROGRMD,T29,PORT MCU,K90IA,K91A,K92A	U9330	CRITICAL	T29MCU:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9x9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3300	1	IC,SMC,EXTERNAL,FSB,A3,J30	U4900	CRITICAL	SMC_PROG
335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK
335S0812	1	64 MBIT SPI SRL DUAL I/O FLSH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S3558	1	IC,EFI,V00C7,J30/J31	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IB,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
341S3522	1	IC,PSOC,TP/KB,J30/J31	U5701	CRITICAL	TPAD_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
13880603	13880602		ALL	Murata alt to Samsung
15780058	15780084		ALL	Delta alt to TDK Magnetics
12880303	12880353		ALL	Panasonic alt to Sanyo
13880676	13880691		ALL	Murata alt to Samsung
15280778	15280693		ALL	Cyntec alt to Vishay
37680855	37681032		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37681017		ALL	Rohm alt to Toshiba
37680937	37680845		ALL	Fairchild alt to Renesas
37680777	37680761		ALL	AOM alt to Siliconix
37680957	37680958		ALL	Fairchild alt to Fairchild
37680953	37680958		ALL	Fairchild alt to Renesas
37780107	37780126		ALL	Ohmemi alt to Semtech
37180709	37180652		ALL	NXP alt to Infineon
514-0788	514-0671		ALL	Acon(w litemo) alt to Acon
607-9310	607-8722		ALL	Renesas alternate to fairchild
607-9311	607-8723		ALL	Renesas alternate to fairchild

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15281499	15280864		ALL	Coilcraft alt to Murata
15281493	15281300		ALL	Coilcraft alt to Murata
13880652	13880648		ALL	Samsung/Murata alt to Taiyo
13880684	13880660		ALL	Murata alt to Taiyo
15281512	15281295		ALL	Cyntec alt to NEC
15281019	15281271		ALL	Cyntec alt to TOKO
37681023	37680960		ALL	Silicomia alt to Renesas
35383312	35383055		ALL	NXP alt to Pericom
35383238	35381428		ALL	Interail alt to TI
35383519	35382179		ALL	Interail alt to TI
15580578	15580367		ALL	Taiyo alt to Murata
13880681	13880638		ALL	Taiyo alt to Samsung
13880671	13880673		ALL	Taiyo alt to Murata
37680903	37680796		ALL	Fairchild alt to Vishay
37780124	37780057		ALL	Amotech alt to TDk
34183492	34183096		ALL	Numonix alt to Atmel (ENET ROM)
37681053	37680604		ALL	Diodes alt to fairchild
37681076	37680634		ALL	Diodes alt to onsemi

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3092	1	J30 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8895	1	CMN PTS,PCBA,MLB,J30	CMNPTS	CRITICAL	J30_CMNPTS
607-8721	1	POWER_FETS PAIR,FAIRCHILD,DDR,J30	CSET1	CRITICAL	FET_PAIR
607-8722	1	POWER_FETS PAIR,FAIRCHILD,5V_S3,J30	CSET2	CRITICAL	FET_PAIR
607-8723	1	POWER_FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CSET3	CRITICAL	FET_PAIR

SYNC MASTER=K90I MLB SYNC DATE=02/15/2011

PAGE TITLE

BOM Configuration

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Functional Test Points

Fan Connectors

J4100	TRUE	PP5V_S0	6 7
J4101	TRUE	FAN_RT_PWM	52
J4102	TRUE	FAN_RT_TACH	52

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

J5530	TRUE	BI_MIC_LO	61 62
J5531	TRUE	BI_MIC_HI	61 62
J5532	TRUE	BI_MIC_SHIELD	61 62

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

J2227	TRUE	SPKRAMP_L_N_OUT	60 61 85
J2226	TRUE	SPKRAMP_L_P_OUT	60 61 85
J2228	TRUE	SPKRAMP_R_N_OUT	60 61 85
J2230	TRUE	SPKRAMP_R_P_OUT	60 61 85
J2229	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
J2231	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

LVDS FUNC_TEST

J700	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)	6 74
J701	TRUE	PP3V3_S0_LCD_F	6 74
J702	TRUE	PPVOUT_SW_LCDBKLT (NEED 2 TP)	74 77
J703	TRUE	LVDS_DDC_CLK	8 74
J704	TRUE	LVDS_DDC_DATA	8 74
J705	TRUE	LVDS_IG_A_DATA_N<0>	17 74 80
J706	TRUE	LVDS_IG_A_DATA_P<0>	17 74 80
J707	TRUE	LVDS_IG_A_DATA_N<1>	17 74 80
J708	TRUE	LVDS_IG_A_DATA_P<1>	17 74 80
J709	TRUE	LVDS_IG_A_DATA_N<2>	17 74 80
J710	TRUE	LVDS_IG_A_DATA_P<2>	17 74 80
J711	TRUE	LVDS_CONN_A_CLK_F_N	74 85
J712	TRUE	LVDS_CONN_A_CLK_F_P	74 85
J713	TRUE	LED_RETURN_1	74 77
J714	TRUE	LED_RETURN_2	74 77
J715	TRUE	LED_RETURN_3	74 77
J716	TRUE	LED_RETURN_4	74 77
J717	TRUE	LED_RETURN_5	74 77
J718	TRUE	LED_RETURN_6	74 77

(NEED TO ADD 5 GND TP)

SATA ODD CONN

J724	TRUE	PP5V_SW_ODD (NEED 2 TP)	6 41
J725	TRUE	SMC_ODD_DETECT	41 45
J723	TRUE	SATA_ODD_D2R_C_P	41 85
J722	TRUE	SATA_ODD_D2R_C_N	41 85
J721	TRUE	SATA_ODD_R2D_P	41 80
J720	TRUE	SATA_ODD_R2D_N	41 80
J629	TRUE	SMC_SSD_TEMP_CTL_R	
J627	TRUE	HDD_OOB_TEMP	

(NEED TO ADD 3 GND TP)

SATA HDD/IR/SIL

J316	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	6 41
J314	TRUE	SATA_HDD_R2D_P	41 80
J315	TRUE	SATA_HDD_R2D_N	41 80
J313	TRUE	SATA_HDD_D2R_C_P	41 80
J312	TRUE	SATA_HDD_D2R_C_N	41 80
J307	TRUE	SYS_LED_ANODE_R	41
J306	TRUE	IR_RX_OUT	41 44
J628	TRUE	SMC_SSD_THROTTLE_R	
J311	TRUE	PP5V_S3_IR_R	41

(NEED TO ADD 3 GND TP)

BATT POWER CONN

J322	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
J321	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
J320	TRUE	SYS_DETECT_L	63
J305	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)	63 64

(NEED TO ADD 5 GND TP)

BIL CONN

J323	TRUE	PP3V42_G3H	6 7
J324	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
J325	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
J326	TRUE	SMC_BIL_BUTTON_L	45 46 63
J308	TRUE	SMC_LID_R	63

(NEED TO ADD 2 GND TP)

X19 CONN

J301	TRUE	PP3V3_WLAN (NEED 3 TP)	6 32 46
J302	TRUE	PCIE_AP_D2R_PI_P	32 81
J303	TRUE	PCIE_AP_D2R_PI_N	32 81
J304	TRUE	PCIE_AP_R2D_P	32 81
J305	TRUE	PCIE_AP_R2D_N	32 81
J306	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
J307	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
J308	TRUE	PP3V3_S3RS4_BT_F	32
J309	TRUE	PCIE_WAKE_L	17 24 32
J310	TRUE	USB_BT_CONN_P	32 80
J311	TRUE	USB_BT_CONN_N	32 80
J312	TRUE	AP_CLKREQ_Q_L	32
J313	TRUE	AP_RESET_CONN_L	32
J314	TRUE	AP_TEMP_SMB_SDA_R	32
J315	TRUE	AP_TEMP_SMB_SCL_R	32
J316	TRUE	WIFI_EVENT_L_R	32

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

J330	TRUE	PP3V3_S4	6 7
J331	TRUE	PP18V5_Z2	6 54
J332	TRUE	Z2_CS_L	53 54
J333	TRUE	Z2_DEBUG3	53 54
J334	TRUE	Z2_MOSI	53 54
J335	TRUE	Z2_MISO	53 54
J336	TRUE	Z2_SCLK	53 54
J337	TRUE	Z2_BOOST_EN	54
J338	TRUE	Z2_HOST_INTN	53 54
J339	TRUE	Z2_CLKIN	53 54
J340	TRUE	Z2_KEY_ACT_L	53 54
J341	TRUE	Z2_RESET	53 54
J342	TRUE	PSOC_MISO	53 54
J343	TRUE	PSOC_MOSI	53 54
J344	TRUE	PSOC_SCLK	53 54
J345	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
J346	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
J347	TRUE	PSOC_F_CS_L	53 54
J348	TRUE	PICKB_L	53 54
J629	TRUE	PP5V_S5_CUMULUS	54

(NEED TO ADD 2 GND TP)

KEYBOARD CONN

J350	TRUE	PP3V3_S4	6 7
J351	TRUE	PP3V42_G3H	6 7
J352	TRUE	WS_KBD1	53
J353	TRUE	WS_KBD2	53
J354	TRUE	WS_KBD3	53
J355	TRUE	WS_KBD4	53
J356	TRUE	WS_KBD5	53
J357	TRUE	WS_KBD6	53
J358	TRUE	WS_KBD7	53
J359	TRUE	WS_KBD8	53
J360	TRUE	WS_KBD9	53
J361	TRUE	WS_KBD10	53
J362	TRUE	WS_KBD11	53
J363	TRUE	WS_KBD12	53
J364	TRUE	WS_KBD13	53
J365	TRUE	WS_KBD14	53
J366	TRUE	WS_KBD15_CAP	53
J367	TRUE	WS_KBD16_NUM	53
J368	TRUE	WS_KBD17	53
J369	TRUE	WS_KBD18	53
J370	TRUE	WS_KBD19	53
J371	TRUE	WS_KBD20	53
J372	TRUE	WS_KBD21	53
J373	TRUE	WS_KBD22	53
J374	TRUE	WS_KBD23	53
J375	TRUE	WS_KBD_ONOFF_L	53
J376	TRUE	WS_LEFT_SHIFT_KBD	53
J377	TRUE	WS_LEFT_OPTION_KBD	53
J378	TRUE	WS_CONTROL_KBD	53

(NEED TO ADD 2 GND TP)

KBD BACKLIGHT CONN

J356	TRUE	KBDLED_ANODE	54
J357	TRUE	SMC_KDBLED_PRESENT_L	54

(NEED TO ADD 1 GND TP)

CAMERA/ALS CONN

J400	TRUE	PP5V_S3_ALSCAMERA_F	32
J409	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
J410	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
J397	TRUE	USB_CAMERA_CONN_P	32 80
J396	TRUE	USB_CAMERA_CONN_N	32 80

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

J185	TRUE	PPVCORE_S0_CPU	7
J186	TRUE	PPVCORE_S0_AXG	7
E410	TRUE	PP1V2_S3_ENET_INTREG	71
J188	TRUE	PP1V05_S0	7
J189	TRUE	PP1V5_S3RS0	7 85
J190	TRUE	PP1V8_S0	7
J191	TRUE	PP3V3_S0	7 85
J192	TRUE	PP5V_S0	6 7
J193	TRUE	PP3V3_S3	7
J194	TRUE	PP5V_S3	7
J195	TRUE	PPVCCSA_S0_CPU	7
E410	TRUE	PP3V3_S5	7 85
J197	TRUE	PP3V42_G3H	6 7
J198	TRUE	PPBUS_G3H	7
J199	TRUE	PP3V3_ENET	7
E410	TRUE	PP3V3_WLAN	6 32 46
J192	TRUE	PP5V_SW_ODD	6 41
J193	TRUE	PP5V_S0_HDD_FLT	6 41
J194	TRUE	PP18V5_Z2	6 54
E410	TRUE	PP3V3_S0_LCD_F	6 74
J196	TRUE	PP3V3_LCDVDD_SW_F	6 74
J197	TRUE	PP4V5_AUDIO_ANALOG	57 62
E410	TRUE	PP1V5_S3	7
J198	TRUE	SMC_PM_G2_EN	45 73
J546	TRUE	PM_SLP_S4_L	17 26 32 45 73
J199	TRUE	PM_SLP_S3_L	8 17 26 45 73

(NEED TO ADD 6 GND TP)

DC POWER CONN

(NEED 3 TP)

J302	TRUE	PP18V5_DCIN_FUSE	63
J304	TRUE	ADAPTER_SENSE	63

(NEED TO ADD 4 GND TP)

LPC+SPI DEBUG_CONN

E536	TRUE	LPC_AD<0>	16 45 47 81
E537	TRUE	LPC_AD<1>	16 45 47 81
E538	TRUE	LPC_AD<2>	16 45 47 81
E539	TRUE	LPC_AD<3>	16 45 47 81
E600	TRUE	LPC_CLK33M_LPCPLUS	24 47 81
E601	TRUE	LPC_FRAME_L	16 45 47 81
E602	TRUE	LPC_PWRDWN_L	17 45 47
E603	TRUE	LPC_SERIRQ	16 45 47
E604	TRUE	LPCPLUS_GPIO	19 47
E605	TRUE	LPCPLUS_RESET_L	24 47
E606	TRUE	PM_CLKRUN_L	17 45 47
E607	TRUE	PP3V42_G3H	6 7
E608	TRUE	PP5V_S0	6 7
E609	TRUE	SMC_RX_L	45 46 47
E610	TRUE	SMC_TCK	45 46 47
E611	TRUE	SMC_TDI	45 46 47
E612	TRUE	SMC_TDO	45 46 47
E613	TRUE	SMC_TMS	45 46 47
E614	TRUE	SMC_TX_L	45 46 47
E615	TRUE	SPI_ALT_CLK	47
E616	TRUE	SPI_ALT_CS_L	47
E617	TRUE	SPI_ALT_MISO	47
E618	TRUE	SPI_ALT_MOSI	47
E619	TRUE	SPIROM_USE_MLB	19 47 56

(NEED TO ADD 2 GND TP)

NC NO_TESTs

NO_TEST

17	TP_CRT_IG_BLUE	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
17	TP_LVDS_IG_CTRL_CLK	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
17	TP_LVDS_IG_CTRL_DATA	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
17	TP_PCH_LVDS_VBG	TRUE / MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	TRUE / MAKE_BASE=TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	TRUE / MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
16	TP_CLINK_CLK	TRUE / MAKE_BASE=TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	TRUE / MAKE_BASE=TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	TRUE / MAKE_BASE=TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP
38	TP_FW643_SDA	TRUE / MAKE_BASE=TRUE	NC_FW643_SDA
38	TP_FW643_SM	TRUE / MAKE_BASE=TRUE	NC_FW643_SM
38	TP_FW643_TCK	TRUE / MAKE_BASE=TRUE	NC_FW643_TCK
38	TP_FW643_TMS	TRUE / MAKE_BASE=TRUE	NC_FW643_TMS
38	TP_FW643_FW620_L	TRUE / MAKE_BASE=TRUE	NC_FW643_FW620_L
38	TP_FW643_VBUF	TRUE / MAKE_BASE=TRUE	NC_FW643_VBUF
38	TP_FW643_OCR10_CTL	TRUE / MAKE_BASE=TRUE	NC_FW643_OCR10_CTL
38	TP_FW643_AVREG	TRUE / MAKE_BASE=TRUE	NC_FW643_AVREG
38	TP_FW643_TDI	TRUE / MAKE_BASE=TRUE	NC_FW643_TDI
23	TP_XDP_PCH_OBSFN_A<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC NO_TESTs

NO_TEST

R600	TRUE	NC_FW2_TPBP	40
R599	TRUE	NC_FW2_TPBN	40
R598	TRUE	NC_FW2_TPBIAS	40
R597	TRUE	NC_FW2_TPAP	40
R595	TRUE	NC_FW2_TPAN	40
R596	TRUE	NC_FW0_TPBP	40
R594	TRUE	NC_FW0_TPBN	40
R593	TRUE	NC_FW0_TPAP	40
R592	TRUE	XDP_PCH_AP_PWR_EN	
R591	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	
R611	TRUE	XDP_PCH_SDCONN_STATE_RST_L	
R610	TRUE	XDP_PCH_ENET_PWR_EN	
R562	TRUE	XDP_PCH_SDCONN_DET_L	
R583	TRUE	XDP_PCH_S5_PWRGD	23
R584	TRUE	XDP_PCH_PWRBTN_L	23
R585	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	
R586	TRUE	XDP_FW_CLKREQ_L	
R588	TRUE	XDP_AP_CLKREQ_L	
R589	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	

17	TP_SDVO_TVCLKINN	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTP

NC_EDP_TXP<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_P<0..3>	9
NC_EDP_TXN<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_N<0..3>	9
NC_EDP_AUXP MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_P	9
NC_EDP_AUXN MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_N	9
NC_CPU_THERMDA MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDA	
NC_CPU_THERMDC MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDC	
NC_CPU_RSVD<30..45> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<30..45>	
NC_CPU_RSVD<8..27> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<8..27>	
NC_PEG_R2D_CP<0..7> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_P<0..7>	9
NC_PEG_R2D_CN<0..7> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_N<0..7>	9
NC_PEG_D2RP<0..7> MAKE_BASE=TRUE	TRUE	=PEG_D2R_P<0..7>	9
NC_PEG_D2RN<0..7> MAKE_BASE=TRUE	TRUE	=PEG_D2R_N<0..7>	9
NC_PEG_R2D_CP<8..11> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_P<8..11>	9
NC_PEG_R2D_CN<8..11> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_N<8..11>	9
NC_PEG_D2RP<8..11> MAKE_BASE=TRUE	TRUE	=PEG_D2R_P<8..11>	9
NC_PEG_D2RN<8..11> MAKE_BASE=TRUE	TRUE	=PEG_D2R_N<8..11>	9
16	TP_PCIE_CLK100M_PE4N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
16	TP_PCIE_CLK100M_PE4P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
16	TP_PCIE_CLK100M_PE5N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
16	TP_PCIE_CLK100M_PE5P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
16	TP_PCIE_CLK100M_PE6N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
16	TP_PCIE_CLK100M_PE6P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
16	TP_PCIE_CLK100M_PE7N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
16	TP_PCIE_CLK100M_PE7P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
53	TP_PSOC_P1_3	TRUE / MAKE_BASE=TRUE	NC_PSOC_P1_3
16	TP_SATA_C_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_C_D2RN
16	TP_SATA_C_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_C_D2RP
16	TP_SATA_C_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_C_R2D_CN
16	TP_SATA_C_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_C_R2D_CP
16	TP_SATA_D_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
33	TP_TBT_MONDC0	TRUE / MAKE_BASE=TRUE	NC_TBT_MONDC0
33	TP_TBT_MONDC1	TRUE / MAKE_BASE=TRUE	NC_TBT_MONDC1
33	TP_TBT_MONOBSP	TRUE / MAKE_BASE=TRUE	NC_TBT_MONOBSP
33	TP_TBT_MONOBSN	TRUE / MAKE_BASE=TRUE	NC_TBT_MONOBSN
33	TP_DP_T29SRC_ML_CP<0..3>	TRUE / MAKE_BASE=TRUE	NC_DP_T29SRC_ML_CP<0..3>
33	TP_DP_T29SRC_ML_CN<0..3>	TRUE / MAKE_BASE=TRUE	NC_DP_T29SRC_ML_CN<0..3>
33	TP_DP_T29SRC_AUXCH_CP	TRUE / MAKE_BASE=TRUE	NC_DP_T29SRC_AUXCH_CP
33	TP_DP_T29SRC_AUXCH_CN	TRUE / MAKE_BASE=TRUE	NC_DP_T29SRC_AUXCH_CN
33 6	TP_T29_PCIE_RESET0_L	TRUE / MAKE_BASE=TRUE	TP_T29_PCIE_RESET0_L 6 33
33 6	TP_T29_PCIE_RESET1_L	TRUE / MAKE_BASE=TRUE	TP_T29_PCIE_RESET1_L 6 33
33 6	TP_T29_PCIE_RESET2_L	TRUE / MAKE_BASE=TRUE	TP_T29_PCIE_RESET2_L 6 33
33 6	TP_T29_PCIE_RESET3_L	TRUE / MAKE_BASE=TRUE	TP_T29_PCIE_RESET3_L 6 33

J822	TRUE	PCH_VSS_NCTF<1>	81
J823	TRUE	PCH_VSS_NCTF<2>	81
J820	TRUE	PCH_VSS_NCTF<5>	81
J819	TRUE	PCH_VSS_NCTF<9>	81
J818	TRUE	PCH_VSS_NCTF<11>	81
J817	TRUE	PCH_VSS_NCTF<12>	81
J832	TRUE	PCH_VSS_NCTF<15>	81
J834	TRUE	PCH_VSS_NCTF<17>	81
J833	TRUE	PCH_VSS_NCTF<19>	6 81
J836	TRUE	PCH_VSS_NCTF<19>	6 81
J835	TRUE	PCH_VSS_NCTF<21>	81
J838	TRUE	PCH_VSS_NCTF<25>	81
J837	TRUE	PCH_VSS_NCTF<27>	81
J840	TRUE	PCH_VSS_NCTF<29>	81

8	TP_LVDS_IG_B_CLKN	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	TRUE / MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L

SYNC MASTER=K90I_MLB
PAGE TITLE

FUNC TEST

Apple Inc.

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"G3Hot" (Always-Present) Rails

64 63 =PPBUS_G3H → PPBUS_G3H — MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=12.6V; MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT 77
- =PPBUS_S5_FWPWRSW 39
- =PPBUS_S0_VSENSE 50
- =PPVIN_SW_T29BST 8 35
- =PPVIN_S5_HS_COMPUTING_ISNS_R 50
- =PPVIN_S5_HS_OTHER_ISNS_R 50

35 PPVIN_SW_T29BST (VOLTAGE=12.6V)

50 =PPVIN_S5_HS_COMPUTING_ISNS → PPBUS_S5_HS_COMPUTING_ISNS — MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.25 mm; VOLTAGE=12.6V; MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP 68 69
- =PPVIN_S3_DDRREG 67
- =PPVIN_S0_CPUVCCIOS0 70
- =PPVIN_S0_VCCSAS0 65
- =PPVIN_S0_CPUAXG 69

50 =PPVIN_S5_HS_OTHER_ISNS → PPBUS_S5_HS_OTHER_ISNS — MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=12.6V; MAKE_BASE=TRUE
- =PPVIN_S5_5VS3 66
- =PPVIN_S5_3V3S5 66

63 =PP18V5_DCIN_CONN → PPDCIN_G3H — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.25 MM; VOLTAGE=18.5V; MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 64
- =PPDCIN_S5_VSENSE 50

63 =PP3V42_G3H_REG → PP3V42_G3H — MIN_LINE_WIDTH=0.3 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=3.42V; MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS 47
- =PP3V3_S5_SMC 45 46
- =PP3V42_G3H_BATT 63
- =PP3V42_G3H_CHGR 64
- =PP3V42_G3H_ONEWIREPROT 63
- =PP3V42_G3H_PWRCTL 73
- =PP3V42_G3H_SMBUS_SMC_BSA 48
- =PP3V42_G3H_SMCUSBMUX 42
- =PP3V42_G3H_TPAD 53
- =PPVIN_S5_SMCVREF 46
- =PPVBAT_G3_SYSCLK 24
- =PP3V42_G3H_AUDIO 58

24 =PPVRTC_G3_OUT → PPVRTC_G3H — MIN_LINE_WIDTH=0.2 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=3V; MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 16 17 20

5V Rails

66 =PP5V_S5_LDO → PP5V_S5 — MIN_LINE_WIDTH=0.5 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=5V; MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET 72
- =PP5V_S5_TPAD 54
- =PP5V_S5_P5VSUSFET 72

72 =PP5V_SUS_FET → PP5V_SUS — MIN_LINE_WIDTH=0.50MM; MIN_NECK_WIDTH=0.20MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP5V_SUS_PCH 22

66 =PP5V_S3_REG → PP5V_S3 — MIN_LINE_WIDTH=0.5 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=5V; MAKE_BASE=TRUE
- =PP5V_S3_ALSCAMERA 32
- =PP5V_S3_AUDIO 57
- =PP5V_S3_AUDIO_AMP 60
- =PP5V_S3_DDRREG 67
- =PP5V_S3_IR 41 44
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_ODD 41
- =PP5V_S3_P5VS0FET 72
- =PP5V_S3_USB 42
- =PP5V_S3_SYSLED 46

72 =PP5V_S0_FET → PP5V_S0 — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=5V; MAKE_BASE=TRUE
- =PP5V_S0_BKL 77
- =PP5V_S0_CPUIMVP 68 69
- =PP5V_S0_CPUVCCIOS0 70
- =PP5V_S0_FAN_RT 52
- =PP5V_S0_HDD_ISNS_R 49
- =PP5V_S0_KBDLED 54
- =PP5V_S0_LPCPLUS 47
- =PP5V_S0_VCCSAS0 65
- =PP5V_S0_PCH 22 24
- =PP5V_S0_VMON 73
- =PP5V_S0_ISNS 49
- =PP5V_S0_AUDIO

49 =PP5V_S0_HDD_ISNS → PP5V_S0_HDD — MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.4MM; VOLTAGE=5V; MAKE_BASE=TRUE
- =PP5V_S0_HDD 41

3.3V Rails

66 =PP3V3_S5_REG → PP3V3_S5 — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_S5_XDP 23
- =PP3V3_S0_P3V3S0FET 72
- =PP3V3_S3_P3V3S3FET 72
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S4_P3V3S4FET 72
- =PP3V3_S5_LCD 74
- =PP3V3_S5_PCH 17
- =PP3V3_S5_PCHPWRGD 24
- =PP3V3_S5_SMCBATLOW 46
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_SYSCLK 24
- =PP3V3_S5_VMON 73
- =PP3V3_S5_PWRCTL 73
- =PP3V3_S5_P3V3SUSFET 72
- =PP3V3_S4_TBTAPWRSW 76
- =PP3V3_S5_PCH_GPIO 19

72 =PP3V3_SUS_FET → PP3V3_SUS — MIN_LINE_WIDTH=0.50MM; MIN_NECK_WIDTH=0.20MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22
- =PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
- =PP3V3_SUS_PCH_VCCSUS 20
- =PP3V3_SUS_PCH_GPIO 16 17 18 19
- =PP3V3_SUS_PCH 22
- =PP3V3_SUS_PWRCTL 73
- =PP3V3_SUS_P1V05SUSLDO 71
- =PP3V3_SUS_SMC 46
- =PP3V3_SUS_ROM 56
- =PP3V3_SUS_PCH_VCC_SPI 20 22

72 =PP3V3_S4_FET → PP3V3_S4 — MIN_LINE_WIDTH=0.50MM; MIN_NECK_WIDTH=0.20MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_S4_TPAD 53 54
- =PP3V3_S4_SMC 46
- =PP3V3_S4_SD_HPD 30
- =PP3V3_S4_BT 32

72 =PP3V3_S3_FET → PP3V3_S3 — MIN_LINE_WIDTH=0.50MM; MIN_NECK_WIDTH=0.20MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_S3_BT 32
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_SMBUS_SMC_A_S3 48
- =PP3V3_S3_SMBUS_SMC_MGMT 48
- =PP3V3_S3_SMS 55
- =PP3V3_S3_USB_HUB 25
- =PP3V3_S3_USB_RESET 25
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 32
- =PP3V3_S3_SDBUF 24
- =PP3V3_S3_P3V3ENETFET 73
- =PP3V3_S3_PCH_GPIO 18 24
- =PP3V3_S3_ISNS 49
- =PP3V3_S3_USBMUX 25

72 =PP3V3_S0_FET → PP3V3_S0 — MIN_LINE_WIDTH=0.5 MM; MIN_NECK_WIDTH=0.20MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_S0_HDD 41
- =PP3V3_S0_AUDIO 57 61 62
- =PP3V3_S0_BKL_VDDIO 77
- =PP3V3_S0_ISNS 49
- =PP3V3_S0_HS_COMPUTING_ISNS 50
- =PP3V3_S0_CPUTHMSNS 51
- =PP3V3_S0_LCD 74
- =PP3V3_S0_DP_DDC 8
- =PP3V3_S0_ENETPHY 36
- =PP3V3_S0_FAN_RT 52
- =PP3V3_S0_FWPWRCTL 39
- =PP3V3_S0_FWLATEVG 39 40
- =PP3V3_S0_P3V3T29FET 35
- =PP3V3_S0_SDCARD 30
- =PP3V3_S0_P1V8S0 71
- =PP3V3_S0_ODD 41
- =PP3V3_FW_P3V3FWFET 39
- =PP3V3_S0_PCH 16 22
- =PP3V3_S0_PCH_GPIO 16 17 18 19 30
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_PCH_VCC3_3_GPIO 20 22
- =PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
- =PP3V3_S0_PCH_VCC3_3_PCI 20 22
- =PP3V3_S0_PCH_VCC3_3_SATA 20 22
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PCH_VCCA_LVDS 20
- =PP3V3_S0_PWRCTL 73
- =PP3V3_S0_RSTBUF 24
- =PP3V3_S0_SB_PM 24
- =PP3V3_S0_SMBUS_PCH 48
- =PP3V3_S0_SMBUS_SMC_0_S0 48
- =PP3V3_S0_SMBUS_SMC_B_S0 48
- =PP3V3_S0_SMC 41
- =PP3V3_S0_KBDLED 54
- =PP3V3_S0_VMON 73
- =PPSPD_S0_MEM_A 27
- =PPSPD_S0_MEM_B 29
- =PP3V3_S0_P1V5S0 71
- =PP3V3_S0_T29PWRCTL 35
- =PP3V3_S0_HS_OTHER_ISNS 50
- =PP3V3_S0_DPSDRVA 75
- =PP3V3_S0_P1V05S0LDO 71
- =PP3V3_S0_IMVPISNS 49
- =PP3V3_S0_XDP 23
- =PP3V3_S0_T29I2C 48

1.8V/1.5V/1.2V/1.05V Rails

71 =PP1V8_S0_REG → PP1V8_S0 — MIN_LINE_WIDTH=0.5 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.8V; MAKE_BASE=TRUE
2A max supply
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8_S0_PCH_VCCTX_LVDS 22
- =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
- =PP1V8_S0_P1V05S0LDO 71
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 24

49 =PP1V5_S3_DDR_ISNS → PP1V5_S3_DDR — MIN_LINE_WIDTH=0.8 MM; MIN_NECK_WIDTH=0.1 MM; VOLTAGE=1.5V; MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27
- =PP1V5_S3_MEM_B 29
- =PPVIN_S0_DDRREG_LDO 67
- =PPDDR_S3_MEMVREF 31

67 =PPDDR_S3_REG → PP1V5_S3 — MIN_LINE_WIDTH=0.8 MM; MIN_NECK_WIDTH=0.1 MM; VOLTAGE=1.5V; MAKE_BASE=TRUE
- =PP1V5_S3_P1V5S3RS0_FET 72
- =PP1V5_S3_DDR_ISNS_R 49

72 =PP1V5_S3RS0_FET → PP1V5_S3RS0 — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.5V; MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR 10 12 15 26

71 =PP1V5_S0_REG → PP1V5_S0 — MIN_LINE_WIDTH=2 mm; MIN_NECK_WIDTH=0.17 mm; VOLTAGE=1.5V; MAKE_BASE=TRUE
- =PP1V5_S0_RDRVR 41
- =PP1V8R1V5_S0_AUDIO 57
- =PP3V3R1V5_S0_AUDIO 57
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 24
- =PP1V5_S0_VMON 73

67 31 =PPVTT_S3_DDR_BUF → PPVTTDDR_S3 — MIN_LINE_WIDTH=0.3 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=0.75V; MAKE_BASE=TRUE

67 =PPVTT_S0_DDR_LDO → PP0V75_S0_DDRVTT — MIN_LINE_WIDTH=2 mm; MIN_NECK_WIDTH=0.17 mm; VOLTAGE=0.75V; MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A 27
- =PP0V75_S0_MEM_VTT_B 29
- =PPVTT_S0_VTTCLAMP 26

65 =PPVCCSA_S0_REG → PPVCCSA_S0_CPU — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=0.9V; MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU 12 15

71 =PP1V05_SUS_LDO → PP1V05_SUS — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.05V; MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 23

70 =PPCPUVCCIO_S0_REG → PP1V05_S0 — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1V; MAKE_BASE=TRUE
? mA
- =PP1V05_S0_CPU_VCCIO 9 10 12 14
- =PPVCCIO_S0_CPUIMVP 68
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_SMC 46
- =PP1V05_S0_FWPWRCTL 39
- =PP1V05_FW_P1V0FWFET 39
- =PP1V05_S0_VMON 73
- =PP1V05_S0_P1V05T29FET 35

XW0800 SM 1 2
XW0801 SM 1 2

PP1V05_S0_PCH — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1V; MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCIO_PLLPCIE 20
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 20 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCCIO_USB 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_PCH_VCCIO_CLK 20 22
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCCIO_PLLUSB 20
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PP1V05_S0_PCH_VCCIO_PLLFDI 20
- =PP1V05_S0_PCH_VCCDMI_FDI 20

ENET Rails

73 =PP3V3_ENET_FET → PP3V3_ENET — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_ENET_PHY 24 36 71
- =PP3V3_ENET_SYSCLK 24
- =PPVDDIO_ENET_CLK 24

"FW" (FireWire) Rails

39 =PPBUS_FW_FET → PPVP_FW — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=12.6V; MAKE_BASE=TRUE
- =PPVP_FW_PORT1 40
- =PPVP_FW_PHY_CPS_FET 40

39 =PP3V3_FW_FET → PP3V3_FW_FWPHY — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.25 MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PP3V3_FW_FWPHY 38 39 40
- =PP3V3_S0_P1V05FWFET

39 =PP1V0_FW_FET_R → PP1V0_FW_FWPHY — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.0V; MAKE_BASE=TRUE
- =PP1V0_FW_FWPHY 38 39

T29 Rails (off when no cable)

35 8 =PP15V_T29_REG → PP15V_T29 — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=17.8V; MAKE_BASE=TRUE
- =PPHV_SW_TBTAPWRSW 76

35 =PP3V3_T29_FET → PP3V3_T29 — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=3.3V; MAKE_BASE=TRUE
- =PPVDDIO_T29_CLK 24
- =PP3V3_T29_RTR 33 34 35
- =PP3V3_T29_PCH_GPIO 16 19

35 =PP1V05_T29_FET → PP1V05_T29 — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.05V; MAKE_BASE=TRUE
- =PP1V05_T29_RTR 34

1V05 S0 LDO

71 =PP1V05_S0_LDO → PP1V05_S0_PCH_VCCADPLL — MIN_LINE_WIDTH=0.4 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.05V; MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL 22

Chipset "VCore" Rails

69 =PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.25 MM; VOLTAGE=1.25V; MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 9 12 14
- =PPCPUVCORE_S0_VSENSE 49

69 =PPVCORE_S0_AXG_REG → PPVCORE_S0_AXG — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.05V; MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG 9 12 15
- =PPAXGVCORE_S0_VSENSE 49

15 12 =PP1V5_S3_CPU_VCCDQ → PP1V5_S3_CPU_VCCDQ — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.5V; MAKE_BASE=TRUE

14 12 8 =PP1V05_S0_CPU_VCCPQE → PP1V05_S0_CPU_VCCPQE — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.05V; MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R → PP1V8_S0_CPU_VCCPLL_R — MIN_LINE_WIDTH=0.6 MM; MIN_NECK_WIDTH=0.2 MM; VOLTAGE=1.8V; MAKE_BASE=TRUE

SYNC MASTER=K90I_MLB — SYNC DATE=02/15/2011
PAGE TITLE: Power Aliases

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HEATSINK STANDOFFS

Z0902
STDOFF-4.5OD.98H-1.1-3.48-TH

Z0904
STDOFF-4.5OD.98H-1.1-3.48-TH
BELOW CPU

Z0920
STDOFF-4.5OD.98H-1.1-3.48-TH
LEFT OF CPU

FAN STANDOFF

Z0905
STDOFF-4.5OD.98H-1.1-3.48-TH

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT Z0906 3R2P5

OMIT Z0907 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5
OMIT Z0909 3R2P5
OMIT Z0910 3R2P5
OMIT Z0911 3R2P5
OMIT Z0912 3R2P5

EMI IO (SHORT) POGO PINS

ZS0900 1.4DIA-SHORT-SILVER-K99
ZS0901 1.4DIA-SHORT-SILVER-K99
ZS0902 1.4DIA-SHORT-SILVER-K99
ZS0903 1.4DIA-SHORT-SILVER-K99
ZS0904 1.4DIA-SHORT-SILVER-K99
ZS0905 1.4DIA-SHORT-SILVER-K99

EMI TALL POGO PINS

ZS0904 POGO-2.00D-3.5H-K86-K87
ZS0905 POGO-2.00D-3.5H-K86-K87
ZS0906 POGO-2.00D-3.5H-K86-K87
ZS0907 POGO-2.00D-3.5H-K86-K87

TALL POGO PINS close to DIMM conn.

ZS0920 POGO-2.00D-3.5H-K86-K87 NO STUFF
ZS0921 POGO-2.00D-3.5H-K86-K87 NO STUFF
ZS0922 POGO-2.00D-3.5H-K86-K87 NO STUFF
ZS0923 POGO-2.00D-3.5H-K86-K87 NO STUFF
ZS0924 POGO-2.00D-3.5H-K86-K87 NO STUFF

CPU signals

MEMVTT_EN	MAKE_BASE=TRUE	=DDRVTT_EN	26 67
DP_EXTA_ML_C_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLP<3..0>	81 75 17
DP_EXTA_ML_C_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_B_MLN<3..0>	81 75 17
DP_EXTA_AUXCH_C_P	MAKE_BASE=TRUE	DPA_IG_AUX_CH_P	81 75 17
DP_EXTA_AUXCH_C_N	MAKE_BASE=TRUE	DPA_IG_AUX_CH_N	81 75 17

FW_PLUG_DET_L	MAKE_BASE=TRUE	FW_PME_L	19 39
FW643_WAKE_L	MAKE_BASE=TRUE	=FW_PME_L	39 38 39
TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	SMC_EXCARD_PWR_EN	

PCIE_EXCARD_D2R_N	TRUE	NC_PCIE_EXCARD_D2RN	16
PCIE_EXCARD_D2R_P	TRUE	NC_PCIE_EXCARD_D2RP	16
PCIE_EXCARD_R2D_C_N	TRUE	NC_PCIE_EXCARD_R2D_CN	16
PCIE_EXCARD_R2D_C_P	TRUE	NC_PCIE_EXCARD_R2D_CP	16
PCIE_CLK100M_EXCARD_N	TRUE	NC_PCIE_CLK100M_EXCARDN	81 16
PCIE_CLK100M_EXCARD_P	TRUE	NC_PCIE_CLK100M_EXCARDP	81 16

PCIE_PCH_D2R_N<5..8>	TRUE	NC_PCIE_PCH_D2RN<5..8>	
PCIE_PCH_D2R_P<5..8>	TRUE	NC_PCIE_PCH_D2RP<5..8>	
PCIE_PCH_R2D_C_N<5..8>	TRUE	NC_PCIE_PCH_R2D_CN<5..8>	
PCIE_PCH_R2D_C_P<5..8>	TRUE	NC_PCIE_PCH_R2D_CP<5..8>	
PEG_CLK100M_P		NC_PEG_CLK100MP	81 16
PEG_CLK100M_N		NC_PEG_CLK100MN	81 16

TP_PCH_CLKOUT_DPN	TRUE	NC_PCH_CLKOUT_DPN	16
TP_PCH_CLKOUT_DPP	TRUE	NC_PCH_CLKOUT_DPP	16

T29BST:N

=PPVIN_SW_T29BST — R0960 0 5% 1/8W MF-LF 805 — =PP15V_T29_REG (35 7 / 7 35)

EMI TALL POGO PINS

T29_A_BIAS (76 75 8) — C0960 0.01UF 10% 10V X5R-CERM 0201
DP_A_BIAS0 (75) — C0962 0.01UF 10% 10V X5R-CERM 0201
DP_A_BIAS2 (75) — C0964 0.01UF 10% 10V X5R-CERM 0201

T29_A_BIAS_R2DP1 (75)
T29_A_BIAS_R2DN0 (75)

T29_A_BIAS (76 75 8) — R0970 51 1/20W — T29_A_BIAS_R2DP0 — VOLTAGE=3.3V — C0970 0.01UF 10% 10V X5R-CERM 0201

R0971 51 1/20W — T29_A_BIAS_R2DN1 — VOLTAGE=3.3V — C0971 0.01UF 10% 10V X5R-CERM 0201

R0972 51 1/20W — T29_A_BIAS_D2RP1 — VOLTAGE=3.3V — C0972 0.01UF 10% 10V X5R-CERM 0201

R0973 51 1/20W — T29_A_BIAS_D2RN1 — VOLTAGE=3.3V — C0973 0.01UF 10% 10V X5R-CERM 0201

TBT JTAG

JTAG_ISP_TCK (IN)	MAKE_BASE=TRUE	JTAG_TBT_TCK (OUT)	23 19 33
JTAG_ISP_TDI (IN)	MAKE_BASE=TRUE	JTAG_TBT_TDI (OUT)	19 19 33
JTAG_ISP_TDO (OUT)	MAKE_BASE=TRUE	JTAG_TBT_TDO (IN)	19 33

=PEG_R2D_C_P<12..15>	MAKE_BASE=TRUE	PCIE_T29_R2D_C_P<3..0>	9 33 81
=PEG_R2D_C_N<12..15>	MAKE_BASE=TRUE	PCIE_T29_R2D_C_N<3..0>	9 33 81
=PEG_D2R_P<12..15>	MAKE_BASE=TRUE	PCIE_T29_D2R_P<3..0>	9 33 81
=PEG_D2R_N<12..15>	MAKE_BASE=TRUE	PCIE_T29_D2R_N<3..0>	9 33 81

=PP3V3_S0_DP_DDC (8 7)

R0920 2.2K 5% 1/16W MF-LF 402
R0921 2.2K 5% 1/16W MF-LF 402
R0922 2.2K 5% 1/16W MF-LF 402
R0923 2.2K 5% 1/16W MF-LF 402

TP_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE	DPB_IG_DDC_CLK	17
TP_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE	DPB_IG_DDC_DATA	17
TP_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE	DP_IG_D_CTRL_CLK	17
TP_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE	DP_IG_D_CTRL_DATA	17

=PP3V3_S0_DP_DDC (8 7)

R0924 2.2K 5% 1/16W MF-LF 402
R0925 2.2K 5% 1/16W MF-LF 402

DP_EXTA_DDC_CLK	MAKE_BASE=TRUE	DPA_IG_DDC_CLK	75 17
DP_EXTA_DDC_DATA	MAKE_BASE=TRUE	DPA_IG_DDC_DATA	75 17
DP_EXTA_HPD	MAKE_BASE=TRUE	DPA_IG_HPD	75 17

R0908 100K 5% 1/16W MF-LF 402

R0910 0 5% 1/16W MF-LF 402

PPBUS_SW_LCDBKLT_PWR (77) — R0910 — PPBUS_SW_BKL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V
=PPBUS_SW_BKL (77)

NC_CPU_VCCIO_SEL	MAKE_BASE=TRUE NO_TEST=TRUE	CPU_VCCIO_SEL	12 78

Unused eDP CLK

DPLL_REF_CLK_P	MAKE_BASE=TRUE	DPLL_REF_CLKP	10
DPLL_REF_CLK_N	MAKE_BASE=TRUE	DPLL_REF_CLKN	10

=PP1V05_S0_CPU_VCCPQE (14 12 7)

R0940 1K 5% 1/16W MF-LF 402
R0941 1K 5% 1/16W MF-LF 402

PM_SLP_S3_L	MAKE_BASE=TRUE	=TBT_S0_EN	73 45 26 17 6 76

Unused T29 Ports

T29_D2R_P<2..3> (OUT)	MAKE_BASE=TRUE	NC_T29_D2RP<2..3>	83 33 NO_TEST=TRUE
T29_D2R_N<2..3> (OUT)	MAKE_BASE=TRUE	NC_T29_D2RN<2..3>	83 33 NO_TEST=TRUE
T29_R2D_C_P<2..3> (IN)	MAKE_BASE=TRUE	NC_T29_R2D_CP<2..3>	83 33 NO_TEST=TRUE
T29_R2D_C_N<2..3> (IN)	MAKE_BASE=TRUE	NC_T29_R2D_CN<2..3>	83 33 NO_TEST=TRUE
T29_LSE0<2> (IN)	MAKE_BASE=TRUE	T29_LSE0<2> (OUT)	33 33
T29_LSE0<3> (IN)	MAKE_BASE=TRUE	T29_LSE0<3> (OUT)	33 33

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE	MAKE_BASE=TRUE	P1V5S3RS0_RAMP_DONE (IN)	72
TP_DDRREG_PGOOD	MAKE_BASE=TRUE	DDRREG_PGOOD (IN)	67

T29 DP Ports

DPB_IG_HPD	MAKE_BASE=TRUE	DP_T29SNK0_HPD	17 33

TP_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_P<3..0>	17 33 83
TP_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE	DP_T29SNK0_ML_C_N<3..0>	17 33 83
DPB_IG_AUX_CH_P	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_P	17 33 83
DPB_IG_AUX_CH_N	MAKE_BASE=TRUE	DP_T29SNK0_AUXCH_C_N	17 33 83
TP_DP_IG_D_HPD	MAKE_BASE=TRUE	DP_T29SNK1_HPD	17 33

TP_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE	DP_T29SNK1_ML_C_P<3..0>	17 33 83
TP_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE	DP_T29SNK1_ML_C_N<3..0>	17 33 83
TP_DP_IG_D_AUXP	MAKE_BASE=TRUE	DP_T29SNK1_AUXCH_C_P	17 33 83
TP_DP_IG_D_AUXN	MAKE_BASE=TRUE	DP_T29SNK1_AUXCH_C_N	17 33 83

NC_BCM57765_CE_L_MS_INS_L	MAKE_BASE=TRUE NO_TEST=TRUE	BCM57765_CE_L_MS_INS_L	

TP_LVDS_IG_B_CLKP	MAKE_BASE=TRUE	LVDS_IG_B_CLK_P	6 17 80
TP_LVDS_IG_B_CLKN	MAKE_BASE=TRUE	LVDS_IG_B_CLK_N	6 17 80
NC_LVDS_IG_B_DATAP<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_B_DATA_P<0..3>	17 80
NC_LVDS_IG_B_DATAN<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_B_DATA_N<0..3>	17 80
NC_LVDS_IG_A_DATAP<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_A_DATA_P<3>	17 80
NC_LVDS_IG_A_DATAN<3>	MAKE_BASE=TRUE NO_TEST=TRUE	LVDS_IG_A_DATA_N<3>	17 80
LVDS_DDC_CLK	MAKE_BASE=TRUE	LVDS_IG_DDC_CLK	74 6 17
LVDS_DDC_DATA	MAKE_BASE=TRUE	LVDS_IG_DDC_DATA	74 6 17
LCD_BKLT_PWM	MAKE_BASE=TRUE	LVDS_IG_BKL_PWM	77 17
LCD_IG_PWR_EN		LVDS_IG_PANEL_PWR	74 17
LCD_BKLT_EN	MAKE_BASE=TRUE	LVDS_IG_BKL_ON	77 17

USB Signals

NC_USB3_EXTD_TXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_TX_N	18
NC_USB3_EXTD_TXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_TX_P	18
NC_USB3_EXTD_RXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_RX_N	18
NC_USB3_EXTD_RXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTD_RX_P	18

USB_BT_N	MAKE_BASE=TRUE	USBHUB_DN1_N	80 32 25
USB_BT_P	MAKE_BASE=TRUE	USBHUB_DN1_P	80 32 25
USB_TPAD_N	MAKE_BASE=TRUE	USBHUB_DN3_N	80 53 25
USB_TPAD_P	MAKE_BASE=TRUE	USBHUB_DN3_P	80 53 25
USB_IR_N	MAKE_BASE=TRUE	USBHUB_DN2_N	80 44 25
USB_IR_P	MAKE_BASE=TRUE	USBHUB_DN2_P	80 44 25
USB_SMC_N	MAKE_BASE=TRUE NO_TEST=TRUE	NC_USB_SMCN	80 45
USB_SMC_P	MAKE_BASE=TRUE NO_TEST=TRUE	NC_USB_SMCP	80 45
NC_USB_EXTD_EHCIN	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTD_EHCI_N	18
NC_USB_EXTD_EHCIP	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTD_EHCI_P	18
NC_USB_EXTCN	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTC_N	18 80
NC_USB_EXTCP	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTC_P	18 80
NC_USB3_EXTC_TXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_TX_N	18
NC_USB3_EXTC_TXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_TX_P	18
NC_USB3_EXTC_RXN	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_RX_N	18
NC_USB3_EXTC_RXP	MAKE_BASE=TRUE NO_TEST=TRUE	USB3_EXTC_RX_P	18
NC_USB_EXTD_XHCIN	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTD_XHCI_N	18 80
NC_USB_EXTD_XHCIP	MAKE_BASE=TRUE NO_TEST=TRUE	USB_EXTD_XHCI_P	18 80

TP_CPU_THERMDP	MAKE_BASE=TRUE	CPU_THERMD_P	9 85
TP_CPU_THERMDN	MAKE_BASE=TRUE	CPU_THERMD_N	9 85

TP_CPU_VTT_SELECT	MAKE_BASE=TRUE	CPU_VTTSELECT	

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

SYNC MASTER=K90I MLB — SYNC DATE=02/15/2011
PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-9058 — SIZE D
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NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

OMIT_TABLE
CRITICAL

U1000
IVY-BRIDGE
2C-35W
BGA
(1 OF 9)

DMI
PCI EXPRESS BASED INTERFACE SIGNALS
INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
EMBEDDED DISPLAY PORT

DMI_S2N_N<0>	M2	DMI_RX_0*
DMI_S2N_N<1>	P6	DMI_RX_1*
DMI_S2N_N<2>	P1	DMI_RX_2*
DMI_S2N_N<3>	P10	DMI_RX_3*
DMI_S2N_P<0>	N3	DMI_RX_0
DMI_S2N_P<1>	P7	DMI_RX_1
DMI_S2N_P<2>	P3	DMI_RX_2
DMI_S2N_P<3>	P11	DMI_RX_3
DMI_N2S_N<0>	K1	DMI_TX_0*
DMI_N2S_N<1>	M8	DMI_TX_1*
DMI_N2S_N<2>	N4	DMI_TX_2*
DMI_N2S_N<3>	R2	DMI_TX_3*
DMI_N2S_P<0>	K3	DMI_TX_0
DMI_N2S_P<1>	M7	DMI_TX_1
DMI_N2S_P<2>	P4	DMI_TX_2
DMI_N2S_P<3>	T3	DMI_TX_3
FDI_DATA_N<0>	U7	FDI0_TX_0*
FDI_DATA_N<1>	W11	FDI0_TX_1*
FDI_DATA_N<2>	W1	FDI0_TX_2*
FDI_DATA_N<3>	AA6	FDI0_TX_3*
FDI_DATA_N<4>	W6	FDI1_TX_0*
FDI_DATA_N<5>	V4	FDI1_TX_1*
FDI_DATA_N<6>	Y2	FDI1_TX_2*
FDI_DATA_N<7>	AC9	FDI1_TX_3*
FDI_DATA_P<0>	U6	FDI0_TX_0
FDI_DATA_P<1>	W10	FDI0_TX_1
FDI_DATA_P<2>	W3	FDI0_TX_2
FDI_DATA_P<3>	AA7	FDI0_TX_3
FDI_DATA_P<4>	W7	FDI1_TX_0
FDI_DATA_P<5>	T4	FDI1_TX_1
FDI_DATA_P<6>	AA3	FDI1_TX_2
FDI_DATA_P<7>	AC8	FDI1_TX_3
FDI_FSYNC<0>	AA11	FDI0_FSYNC
FDI_FSYNC<1>	AC12	FDI1_FSYNC
FDI_INT	U11	FDI_INT
FDI_LSYNC<0>	AA10	FDI0_LSYNC
FDI_LSYNC<1>	AG8	FDI1_LSYNC
EDP_COMP	AD2	EDP_ICOMPO
	AF3	EDP_COMPIO
EDP_HPD	AG11	EDP_HPD
TP_EDP_AUX_N	AG4	EDP_AUX*
TP_EDP_AUX_P	AF4	EDP_AUX
TP_EDP_TX_N<0>	AC3	EDP_TX_0*
TP_EDP_TX_N<1>	AC4	EDP_TX_1*
TP_EDP_TX_N<2>	AE11	EDP_TX_2*
TP_EDP_TX_N<3>	AE7	EDP_TX_3*
TP_EDP_TX_P<0>	AC1	EDP_TX_0
TP_EDP_TX_P<1>	AA4	EDP_TX_1
TP_EDP_TX_P<2>	AE10	EDP_TX_2
TP_EDP_TX_P<3>	AE6	EDP_TX_3

=PP1V05_S0_CPU_VCCIO

R1030 24.9 1% 1/16W MF-LF 402 — PLACE_NEAR=U1000.AF3:12.7MM

EDP R1031 10K 1% 1/16W MF-LF 402 — PLACE_NEAR=U1000.AG11:12.7MM

R1010 24.9 1% 1/16W MF-LF 402 — PLACE_NEAR=U1000.G3:12.7MM

CPU_PEG_COMP — =PP1V05_S0_CPU_VCCIO

PEG_ICOMPI	G3	
PEG_ICOMPO	G1	
PEG_RCOMPO	G4	
PEG_RX_0*	H22	=PEG_D2R_N<0>
PEG_RX_1*	J21	=PEG_D2R_N<1>
PEG_RX_2*	B22	=PEG_D2R_N<2>
PEG_RX_3*	D21	=PEG_D2R_N<3>
PEG_RX_4*	A19	=PEG_D2R_N<4>
PEG_RX_5*	D17	=PEG_D2R_N<5>
PEG_RX_6*	B14	=PEG_D2R_N<6>
PEG_RX_7*	D13	=PEG_D2R_N<7>
PEG_RX_8*	A11	=PEG_D2R_N<8>
PEG_RX_9*	B10	=PEG_D2R_N<9>
PEG_RX_10*	G8	=PEG_D2R_N<10>
PEG_RX_11*	A8	=PEG_D2R_N<11>
PEG_RX_12*	B6	=PEG_D2R_N<12>
PEG_RX_13*	H8	=PEG_D2R_N<13>
PEG_RX_14*	E5	=PEG_D2R_N<14>
PEG_RX_15*	K7	=PEG_D2R_N<15>
PEG_RX_0	K22	=PEG_D2R_P<0>
PEG_RX_1	K19	=PEG_D2R_P<1>
PEG_RX_2	C21	=PEG_D2R_P<2>
PEG_RX_3	D19	=PEG_D2R_P<3>
PEG_RX_4	C19	=PEG_D2R_P<4>
PEG_RX_5	D16	=PEG_D2R_P<5>
PEG_RX_6	C13	=PEG_D2R_P<6>
PEG_RX_7	D12	=PEG_D2R_P<7>
PEG_RX_8	C11	=PEG_D2R_P<8>
PEG_RX_9	C9	=PEG_D2R_P<9>
PEG_RX_10	F8	=PEG_D2R_P<10>
PEG_RX_11	C8	=PEG_D2R_P<11>
PEG_RX_12	C5	=PEG_D2R_P<12>
PEG_RX_13	H6	=PEG_D2R_P<13>
PEG_RX_14	F6	=PEG_D2R_P<14>
PEG_RX_15	K6	=PEG_D2R_P<15>
PEG_TX_0*	G22	=PEG_R2D_C_N<0>
PEG_TX_1*	C23	=PEG_R2D_C_N<1>
PEG_TX_2*	D23	=PEG_R2D_C_N<2>
PEG_TX_3*	F21	=PEG_R2D_C_N<3>
PEG_TX_4*	H19	=PEG_R2D_C_N<4>
PEG_TX_5*	C17	=PEG_R2D_C_N<5>
PEG_TX_6*	K15	=PEG_R2D_C_N<6>
PEG_TX_7*	F17	=PEG_R2D_C_N<7>
PEG_TX_8*	F14	=PEG_R2D_C_N<8>
PEG_TX_9*	A15	=PEG_R2D_C_N<9>
PEG_TX_10*	J14	=PEG_R2D_C_N<10>
PEG_TX_11*	H13	=PEG_R2D_C_N<11>
PEG_TX_12*	M10	=PEG_R2D_C_N<12>
PEG_TX_13*	F10	=PEG_R2D_C_N<13>
PEG_TX_14*	D9	=PEG_R2D_C_N<14>
PEG_TX_15*	J4	=PEG_R2D_C_N<15>
PEG_TX_0	F22	=PEG_R2D_C_P<0>
PEG_TX_1	A23	=PEG_R2D_C_P<1>
PEG_TX_2	D24	=PEG_R2D_C_P<2>
PEG_TX_3	E21	=PEG_R2D_C_P<3>
PEG_TX_4	G19	=PEG_R2D_C_P<4>
PEG_TX_5	B18	=PEG_R2D_C_P<5>
PEG_TX_6	K17	=PEG_R2D_C_P<6>
PEG_TX_7	G17	=PEG_R2D_C_P<7>
PEG_TX_8	E14	=PEG_R2D_C_P<8>
PEG_TX_9	C15	=PEG_R2D_C_P<9>
PEG_TX_10	K13	=PEG_R2D_C_P<10>
PEG_TX_11	G13	=PEG_R2D_C_P<11>
PEG_TX_12	K10	=PEG_R2D_C_P<12>
PEG_TX_13	G10	=PEG_R2D_C_P<13>
PEG_TX_14	D8	=PEG_R2D_C_P<14>
PEG_TX_15	K4	=PEG_R2D_C_P<15>

Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-KOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

PLACE_NEAR=U1000.H43:50.8MM
PLACE_SIDE=BOTTOM
=PPVCORE_S0_CPU

=PPVCORE_S0_CPU_VCCAXG

R1064 49.9 1% 1/16W MF-LF 402 NOSTUFF
R1070 49.9 1% 1/16W MF-LF 402 NOSTUFF — PLACE_NEAR=U1000.H45:50.8MM, PLACE_SIDE=BOTTOM

CPU_VCC_VALSENSE_P — Note. VOLTAGE=1.25V
CPU_VCC_VALSENSE_N — Note. VOLTAGE=0V
CPU_AXG_VALSENSE_P — Note. VOLTAGE=1.05V
CPU_AXG_VALSENSE_N — Note. VOLTAGE=0V

R1065 49.9 1% 1/16W MF-LF 402 NOSTUFF
R1071 49.9 1% 1/16W MF-LF 402 NOSTUFF — PLACE_NEAR=U1000.K45:50.8MM, PLACE_SIDE=BOTTOM

PLACE_NEAR=U1000.K43:50.8MM
PLACE_SIDE=BOTTOM

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

CPU_CFG<0>	B50	CFG_0
CPU_CFG<1>	C51	CFG_1
CPU_CFG<2>	B54	CFG_2
CPU_CFG<3>	D53	CFG_3
CPU_CFG<4>	A51	CFG_4
CPU_CFG<5>	C53	CFG_5
CPU_CFG<6>	C55	CFG_6
CPU_CFG<7>	H49	CFG_7
CPU_CFG<8>	A55	CFG_8
CPU_CFG<9>	H51	CFG_9
CPU_CFG<10>	K49	CFG_10
CPU_CFG<11>	K53	CFG_11
CPU_CFG<12>	F53	CFG_12
CPU_CFG<13>	G53	CFG_13
CPU_CFG<14>	L51	CFG_14
CPU_CFG<15>	F51	CFG_15
CPU_CFG<16>	D52	CFG_16
CPU_CFG<17>	L53	CFG_17
CPU_VCC_VALSENSE_P	H43	VCC_VAL_SENSE
CPU_VCC_VALSENSE_N	K43	VSS_VAL_SENSE
CPU_AXG_VALSENSE_P	H45	VAXG_VAL_SENSE
CPU_AXG_VALSENSE_N	K45	VSSAXG_VAL_SENSE
TP_CPU_VCC_DIE_SENSE	F48	VCC_DIE_SENSE
CPU_THERMD_P	H48	RSVD_6
CPU_THERMD_N	K48	RSVD_7
	BA19	RSVD_8
	AY19	RSVD_9
	BA21	RSVD_10
	BB21	RSVD_11
	BB19	RSVD_12
	BA21	RSVD_13
	BB22	RSVD_14
	BA22	RSVD_15
	AY19	RSVD_16
	BA21	RSVD_17
	BB21	RSVD_18
	BA22	RSVD_19
	BB25	RSVD_20
	BB26	RSVD_21
	BA22	RSVD_22
	BB22	RSVD_23
	BB26	RSVD_24
	BB26	RSVD_25
	BB23	RSVD_26
	BB24	RSVD_27

NOTE: Intel does not recommend to use this alnalog sense due to accuracy concern.

OMIT_TABLE
CRITICAL

U1000
BGA
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RESERVED
IVY-BRIDGE
2C-35W

MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V

SA_DIMM_VREFDQ	BE7	PPCPU_MEM_VREFDQ_A
SB_DIMM_VREFDQ	BG7	PPCPU_MEM_VREFDQ_B
RSVD_30	N42	NC
RSVD_31	L42	NC
RSVD_32	L43	NC
RSVD_33	L44	NC
RSVD_34	M13	NC
RSVD_35	M14	NC
RSVD_36	U14	NC
RSVD_37	W14	NC
RSVD_38	P13	NC
RSVD_39	AT49	NC
RSVD_40	K23	NC
RSVD_41	AH2	NC
RSVD_42	AG1	NC
RSVD_43	AM1	NC
RSVD_44	AM3	NC
RSVD_45	N50	NC
DC_TEST_A4	A4	TP_CPU_DC_TEST_A4
DC_TEST_C4	C4	CPU_DC_TEST_C4_D3
DC_TEST_D3	D3	
DC_TEST_D1	D1	TP_CPU_DC_TEST_D1
DC_TEST_A58	A58	TP_CPU_DC_TEST_A58
DC_TEST_A59	A59	CPU_DC_TEST_C59_A59
DC_TEST_C59	C59	
DC_TEST_A61	A61	CPU_DC_TEST_C61_A61
DC_TEST_C61	C61	
DC_TEST_D61	D61	TP_CPU_DC_TEST_D61
DC_TEST_BD61	BD61	TP_CPU_DC_TEST_BD61
DC_TEST_BE61	BE61	CPU_DC_TEST_BE59_BE61
DC_TEST_BE59	BE59	
DC_TEST_BG61	BG61	CPU_DC_TEST_BG59_BG61
DC_TEST_BG59	BG59	
DC_TEST_BG58	BG58	TP_CPU_DC_TEST_BG58
DC_TEST_BG4	BG4	TP_CPU_DC_TEST_BG4
DC_TEST_BG3	BG3	CPU_DC_TEST_C4_BE3_BG3
DC_TEST_BE3	BE3	
DC_TEST_BG1	BG1	CPU_DC_TEST_C4_BE1_BG1
DC_TEST_BE1	BE1	
DC_TEST_BD1	BD1	TP_CPU_DC_TEST_BD1

R1042 1K EDP
R1044 1K NOSTUFF
R1045 1K NOSTUFF
R1046 1K NOSTUFF
R1047 1K NOSTUFF

CPU_CFG<7>
CPU_CFG<6>
CPU_CFG<5>
CPU_CFG<4>
CPU_CFG<2>

R1040 1K NOSTUFF
R1041 1K NOSTUFF
R1043 1K NOSTUFF
R1049 1K NOSTUFF

CPU_CFG<16>
CPU_CFG<3>
CPU_CFG<1>
CPU_CFG<0>

These can be Placed close to J2500 and Only for debug access

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC_MASTER=MASTER
SYNC_DATE=02/15/2011
PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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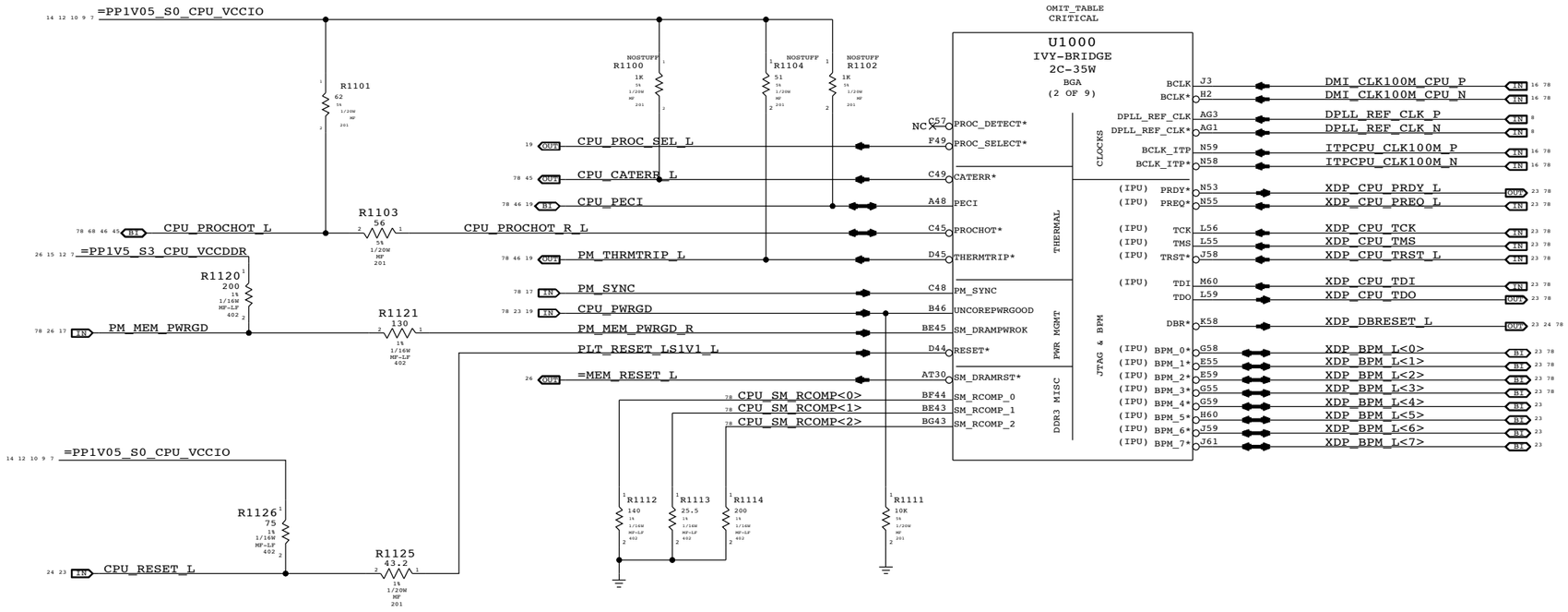

SYNC MASTER=MASTER SYNC DATE=02/15/2013

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CPU CLOCK/MISC/JTAG

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OMIT_TABLE
CRITICAL

U1000
BGA
(3 OF 9)
IVY-BRIDGE
2C-35W
MEMORY CHANNEL A

MEM_A_DQ<0>	AG6	SA_DQ_0	SA_CK_0	AU36	MEM_A_CLK_P<0>	OUT	27 79
MEM_A_DQ<1>	AJ6	SA_DQ_1	SA_CK_0*	AV36	MEM_A_CLK_N<0>	OUT	27 79
MEM_A_DQ<2>	AP11	SA_DQ_2	SA_CKE_0	AY26	MEM_A_CKE<0>	OUT	27 79
MEM_A_DQ<3>	AL6	SA_DQ_3	SA_CK_1	AT40	MEM_A_CLK_P<1>	OUT	27 79
MEM_A_DQ<4>	AJ10	SA_DQ_4	SA_CK_1*	AU40	MEM_A_CLK_N<1>	OUT	27 79
MEM_A_DQ<5>	AJ8	SA_DQ_5	SA_CKE_1	BB26	MEM_A_CKE<1>	OUT	27 79
MEM_A_DQ<6>	AL8	SA_DQ_6	SA_CS_0*	BB40	MEM_A_CS_L<0>	OUT	27 79
MEM_A_DQ<7>	AL7	SA_DQ_7	SA_CS_1*	BC41	MEM_A_CS_L<1>	OUT	27 79
MEM_A_DQ<8>	AR11	SA_DQ_8	SA_ODT_0	AY40	MEM_A_ODT<0>	OUT	27 79
MEM_A_DQ<9>	AP6	SA_DQ_9	SA_ODT_1	BA41	MEM_A_ODT<1>	OUT	27 79
MEM_A_DQ<10>	AU6	SA_DQ_10	SA_DQS_0*	AL11	MEM_A_DQS_N<0>	BI	28 79
MEM_A_DQ<11>	AV9	SA_DQ_11	SA_DQS_1*	AR8	MEM_A_DQS_N<1>	BI	28 79
MEM_A_DQ<12>	AR6	SA_DQ_12	SA_DQS_2*	AV11	MEM_A_DQS_N<2>	BI	28 79
MEM_A_DQ<13>	AP8	SA_DQ_13	SA_DQS_3*	AT17	MEM_A_DQS_N<3>	BI	28 79
MEM_A_DQ<14>	AT13	SA_DQ_14	SA_DQS_4*	AV45	MEM_A_DQS_N<4>	BI	28 79
MEM_A_DQ<15>	AU13	SA_DQ_15	SA_DQS_5*	AY51	MEM_A_DQS_N<5>	BI	28 79
MEM_A_DQ<16>	BC7	SA_DQ_16	SA_DQS_6*	AT55	MEM_A_DQS_N<6>	BI	28 79
MEM_A_DQ<17>	BB7	SA_DQ_17	SA_DQS_7*	AK55	MEM_A_DQS_N<7>	BI	28 79
MEM_A_DQ<18>	BA13	SA_DQ_18	SA_DQS_0	AJ11	MEM_A_DQS_P<0>	BI	28 79
MEM_A_DQ<19>	BB11	SA_DQ_19	SA_DQS_1	AR10	MEM_A_DQS_P<1>	BI	28 79
MEM_A_DQ<20>	BA7	SA_DQ_20	SA_DQS_2	AY11	MEM_A_DQS_P<2>	BI	28 79
MEM_A_DQ<21>	BA9	SA_DQ_21	SA_DQS_3	AU17	MEM_A_DQS_P<3>	BI	28 79
MEM_A_DQ<22>	BB9	SA_DQ_22	SA_DQS_4	AW45	MEM_A_DQS_P<4>	BI	28 79
MEM_A_DQ<23>	AY13	SA_DQ_23	SA_DQS_5	AV51	MEM_A_DQS_P<5>	BI	28 79
MEM_A_DQ<24>	AV14	SA_DQ_24	SA_DQS_6	AT56	MEM_A_DQS_P<6>	BI	28 79
MEM_A_DQ<25>	AR14	SA_DQ_25	SA_DQS_7	AK54	MEM_A_DQS_P<7>	BI	28 79
MEM_A_DQ<26>	AY17	SA_DQ_26	SA_MA_0	BG35	MEM_A_A<0>	OUT	27 79
MEM_A_DQ<27>	AR19	SA_DQ_27	SA_MA_1	BB34	MEM_A_A<1>	OUT	27 79
MEM_A_DQ<28>	BA14	SA_DQ_28	SA_MA_2	BE35	MEM_A_A<2>	OUT	27 79
MEM_A_DQ<29>	AU14	SA_DQ_29	SA_MA_3	BD35	MEM_A_A<3>	OUT	27 79
MEM_A_DQ<30>	BB14	SA_DQ_30	SA_MA_4	AT34	MEM_A_A<4>	OUT	27 79
MEM_A_DQ<31>	BB17	SA_DQ_31	SA_MA_5	AU34	MEM_A_A<5>	OUT	27 79
MEM_A_DQ<32>	BA45	SA_DQ_32	SA_MA_6	BB32	MEM_A_A<6>	OUT	27 79
MEM_A_DQ<33>	AR43	SA_DQ_33	SA_MA_7	AT32	MEM_A_A<7>	OUT	27 79
MEM_A_DQ<34>	AW48	SA_DQ_34	SA_MA_8	AY32	MEM_A_A<8>	OUT	27 79
MEM_A_DQ<35>	BC48	SA_DQ_35	SA_MA_9	AV32	MEM_A_A<9>	OUT	27 79
MEM_A_DQ<36>	BC45	SA_DQ_36	SA_MA_10	BE37	MEM_A_A<10>	OUT	27 79
MEM_A_DQ<37>	AR45	SA_DQ_37	SA_MA_11	BA30	MEM_A_A<11>	OUT	27 79
MEM_A_DQ<38>	AT48	SA_DQ_38	SA_MA_12	BC30	MEM_A_A<12>	OUT	27 79
MEM_A_DQ<39>	AY48	SA_DQ_39	SA_MA_13	AW41	MEM_A_A<13>	OUT	27 79
MEM_A_DQ<40>	BA49	SA_DQ_40	SA_MA_14	AY28	MEM_A_A<14>	OUT	27 79
MEM_A_DQ<41>	AV49	SA_DQ_41	SA_MA_15	AU26	MEM_A_A<15>	OUT	27 79
MEM_A_DQ<42>	BB51	SA_DQ_42					
MEM_A_DQ<43>	AY53	SA_DQ_43					
MEM_A_DQ<44>	BB49	SA_DQ_44					
MEM_A_DQ<45>	AU49	SA_DQ_45					
MEM_A_DQ<46>	BA53	SA_DQ_46					
MEM_A_DQ<47>	BB55	SA_DQ_47					
MEM_A_DQ<48>	BA55	SA_DQ_48					
MEM_A_DQ<49>	AV56	SA_DQ_49					
MEM_A_DQ<50>	AP50	SA_DQ_50					
MEM_A_DQ<51>	AP53	SA_DQ_51					
MEM_A_DQ<52>	AV54	SA_DQ_52					
MEM_A_DQ<53>	AT54	SA_DQ_53					
MEM_A_DQ<54>	AP56	SA_DQ_54					
MEM_A_DQ<55>	AP52	SA_DQ_55					
MEM_A_DQ<56>	AN57	SA_DQ_56					
MEM_A_DQ<57>	AN53	SA_DQ_57					
MEM_A_DQ<58>	AG56	SA_DQ_58					
MEM_A_DQ<59>	AG53	SA_DQ_59					
MEM_A_DQ<60>	AN55	SA_DQ_60					
MEM_A_DQ<61>	AN52	SA_DQ_61					
MEM_A_DQ<62>	AG55	SA_DQ_62					
MEM_A_DQ<63>	AK56	SA_DQ_63					
MEM_A_BA<0>	BD37	SA_BS_0					
MEM_A_BA<1>	BF36	SA_BS_1					
MEM_A_BA<2>	BA28	SA_BS_2					
MEM_A_CAS_L	BE39	SA_CAS*					
MEM_A_RAS_L	BD39	SA_RAS*					
MEM_A_WE_L	AT41	SA_WE*					

OMIT_TABLE
CRITICAL

U1000
BGA
(4 OF 9)
IVY-BRIDGE
2C-35W
MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	SB_CK_0	BA34	MEM_B_CLK_P<0>	OUT	29 79
MEM_B_DQ<1>	AL1	SB_DQ_1	SB_CK_0*	AY34	MEM_B_CLK_N<0>	OUT	29 79
MEM_B_DQ<2>	AN3	SB_DQ_2	SB_CKE_0	AR22	MEM_B_CKE<0>	OUT	29 79
MEM_B_DQ<3>	AR4	SB_DQ_3	SB_CK_1	BA36	MEM_B_CLK_P<1>	OUT	29 79
MEM_B_DQ<4>	AK4	SB_DQ_4	SB_CK_1*	BB36	MEM_B_CLK_N<1>	OUT	29 79
MEM_B_DQ<5>	AK3	SB_DQ_5	SB_CKE_1	BF27	MEM_B_CKE<1>	OUT	29 79
MEM_B_DQ<6>	AN4	SB_DQ_6	SB_CS_0*	BE41	MEM_B_CS_L<0>	OUT	29 79
MEM_B_DQ<7>	AR1	SB_DQ_7	SB_CS_1*	BE47	MEM_B_CS_L<1>	OUT	29 79
MEM_B_DQ<8>	AU4	SB_DQ_8	SB_ODT_0	AT43	MEM_B_ODT<0>	OUT	29 79
MEM_B_DQ<9>	AT2	SB_DQ_9	SB_ODT_1	BG47	MEM_B_ODT<1>	OUT	29 79
MEM_B_DQ<10>	AV4	SB_DQ_10	SB_DQS_0*	AL3	MEM_B_DQS_N<0>	BI	28 79
MEM_B_DQ<11>	BA4	SB_DQ_11	SB_DQS_1*	AV3	MEM_B_DQS_N<1>	BI	28 79
MEM_B_DQ<12>	AU3	SB_DQ_12	SB_DQS_2*	BG11	MEM_B_DQS_N<2>	BI	28 79
MEM_B_DQ<13>	AR3	SB_DQ_13	SB_DQS_3*	BD17	MEM_B_DQS_N<3>	BI	28 79
MEM_B_DQ<14>	AY2	SB_DQ_14	SB_DQS_4*	BG51	MEM_B_DQS_N<4>	BI	28 79
MEM_B_DQ<15>	BA3	SB_DQ_15	SB_DQS_5*	BA59	MEM_B_DQS_N<5>	BI	28 79
MEM_B_DQ<16>	BE9	SB_DQ_16	SB_DQS_6*	AT60	MEM_B_DQS_N<6>	BI	28 79
MEM_B_DQ<17>	BD9	SB_DQ_17	SB_DQS_7*	AK59	MEM_B_DQS_N<7>	BI	28 79
MEM_B_DQ<18>	BD13	SB_DQ_18	SB_DQS_0	AM2	MEM_B_DQS_P<0>	BI	28 79
MEM_B_DQ<19>	BF12	SB_DQ_19	SB_DQS_1	AV1	MEM_B_DQS_P<1>	BI	28 79
MEM_B_DQ<20>	BF8	SB_DQ_20	SB_DQS_2	BE11	MEM_B_DQS_P<2>	BI	28 79
MEM_B_DQ<21>	BD10	SB_DQ_21	SB_DQS_3	BD18	MEM_B_DQS_P<3>	BI	28 79
MEM_B_DQ<22>	BD14	SB_DQ_22	SB_DQS_4	BE51	MEM_B_DQS_P<4>	BI	28 79
MEM_B_DQ<23>	BE13	SB_DQ_23	SB_DQS_5	BA61	MEM_B_DQS_P<5>	BI	28 79
MEM_B_DQ<24>	BF16	SB_DQ_24	SB_DQS_6	AR59	MEM_B_DQS_P<6>	BI	28 79
MEM_B_DQ<25>	BE17	SB_DQ_25	SB_DQS_7	AK61	MEM_B_DQS_P<7>	BI	28 79
MEM_B_DQ<26>	BE18	SB_DQ_26	SB_MA_0	BF32	MEM_B_A<0>	OUT	29 79
MEM_B_DQ<27>	BE21	SB_DQ_27	SB_MA_1	BE33	MEM_B_A<1>	OUT	29 79
MEM_B_DQ<28>	BE14	SB_DQ_28	SB_MA_2	BD33	MEM_B_A<2>	OUT	29 79
MEM_B_DQ<29>	BG14	SB_DQ_29	SB_MA_3	AU30	MEM_B_A<3>	OUT	29 79
MEM_B_DQ<30>	BG18	SB_DQ_30	SB_MA_4	BD30	MEM_B_A<4>	OUT	29 79
MEM_B_DQ<31>	BF19	SB_DQ_31	SB_MA_5	AV30	MEM_B_A<5>	OUT	29 79
MEM_B_DQ<32>	BD50	SB_DQ_32	SB_MA_6	BG30	MEM_B_A<6>	OUT	29 79
MEM_B_DQ<33>	BF48	SB_DQ_33	SB_MA_7	BD29	MEM_B_A<7>	OUT	29 79
MEM_B_DQ<34>	BD53	SB_DQ_34	SB_MA_8	BE30	MEM_B_A<8>	OUT	29 79
MEM_B_DQ<35>	BF52	SB_DQ_35	SB_MA_9	BE28	MEM_B_A<9>	OUT	29 79
MEM_B_DQ<36>	BD49	SB_DQ_36	SB_MA_10	BD43	MEM_B_A<10>	OUT	29 79
MEM_B_DQ<37>	BE49	SB_DQ_37	SB_MA_11	AT28	MEM_B_A<11>	OUT	29 79
MEM_B_DQ<38>	BD54	SB_DQ_38	SB_MA_12	AV28	MEM_B_A<12>	OUT	29 79
MEM_B_DQ<39>	BE53	SB_DQ_39	SB_MA_13	BD46	MEM_B_A<13>	OUT	29 79
MEM_B_DQ<40>	BF56	SB_DQ_40	SB_MA_14	AT26	MEM_B_A<14>	OUT	29 79
MEM_B_DQ<41>	BE57	SB_DQ_41	SB_MA_15	AU22	MEM_B_A<15>	OUT	29 79
MEM_B_DQ<42>	BC59	SB_DQ_42					
MEM_B_DQ<43>	AY60	SB_DQ_43					
MEM_B_DQ<44>	BE54	SB_DQ_44					
MEM_B_DQ<45>	BG54	SB_DQ_45					
MEM_B_DQ<46>	BA58	SB_DQ_46					
MEM_B_DQ<47>	AW59	SB_DQ_47					
MEM_B_DQ<48>	AW58	SB_DQ_48					
MEM_B_DQ<49>	AU58	SB_DQ_49					
MEM_B_DQ<50>	AN61	SB_DQ_50					
MEM_B_DQ<51>	AN59	SB_DQ_51					
MEM_B_DQ<52>	AU59	SB_DQ_52					
MEM_B_DQ<53>	AU61	SB_DQ_53					
MEM_B_DQ<54>	AN58	SB_DQ_54					
MEM_B_DQ<55>	AR58	SB_DQ_55					
MEM_B_DQ<56>	AK58	SB_DQ_56					
MEM_B_DQ<57>	AL58	SB_DQ_57					
MEM_B_DQ<58>	AG58	SB_DQ_58					
MEM_B_DQ<59>	AG59	SB_DQ_59					
MEM_B_DQ<60>	AM60	SB_DQ_60					
MEM_B_DQ<61>	AL59	SB_DQ_61					
MEM_B_DQ<62>	AF61	SB_DQ_62					
MEM_B_DQ<63>	AH60	SB_DQ_63					
MEM_B_BA<0>	BG39	SB_BS_0					
MEM_B_BA<1>	BD42	SB_BS_1					
MEM_B_BA<2>	AT22	SB_BS_2					
MEM_B_CAS_L	AV43	SB_CAS*					
MEM_B_RAS_L	BF40	SB_RAS*					
MEM_B_WE_L	BD45	SB_WE*					

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CPU DDR3 INTERFACES

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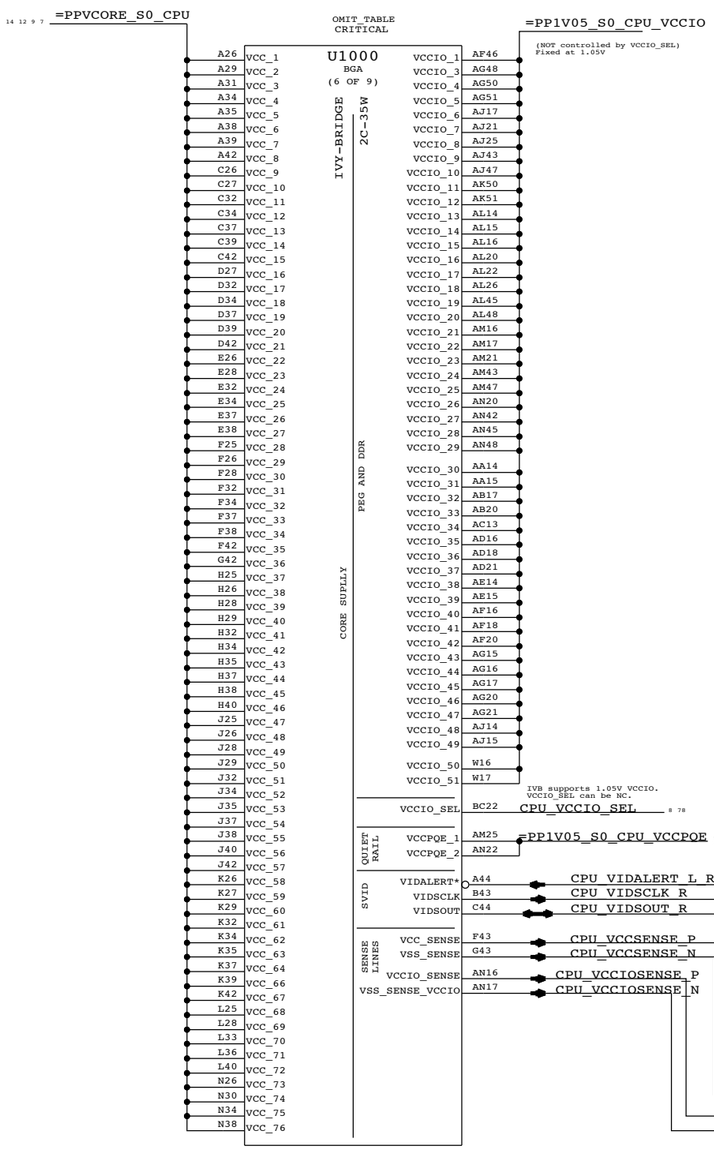

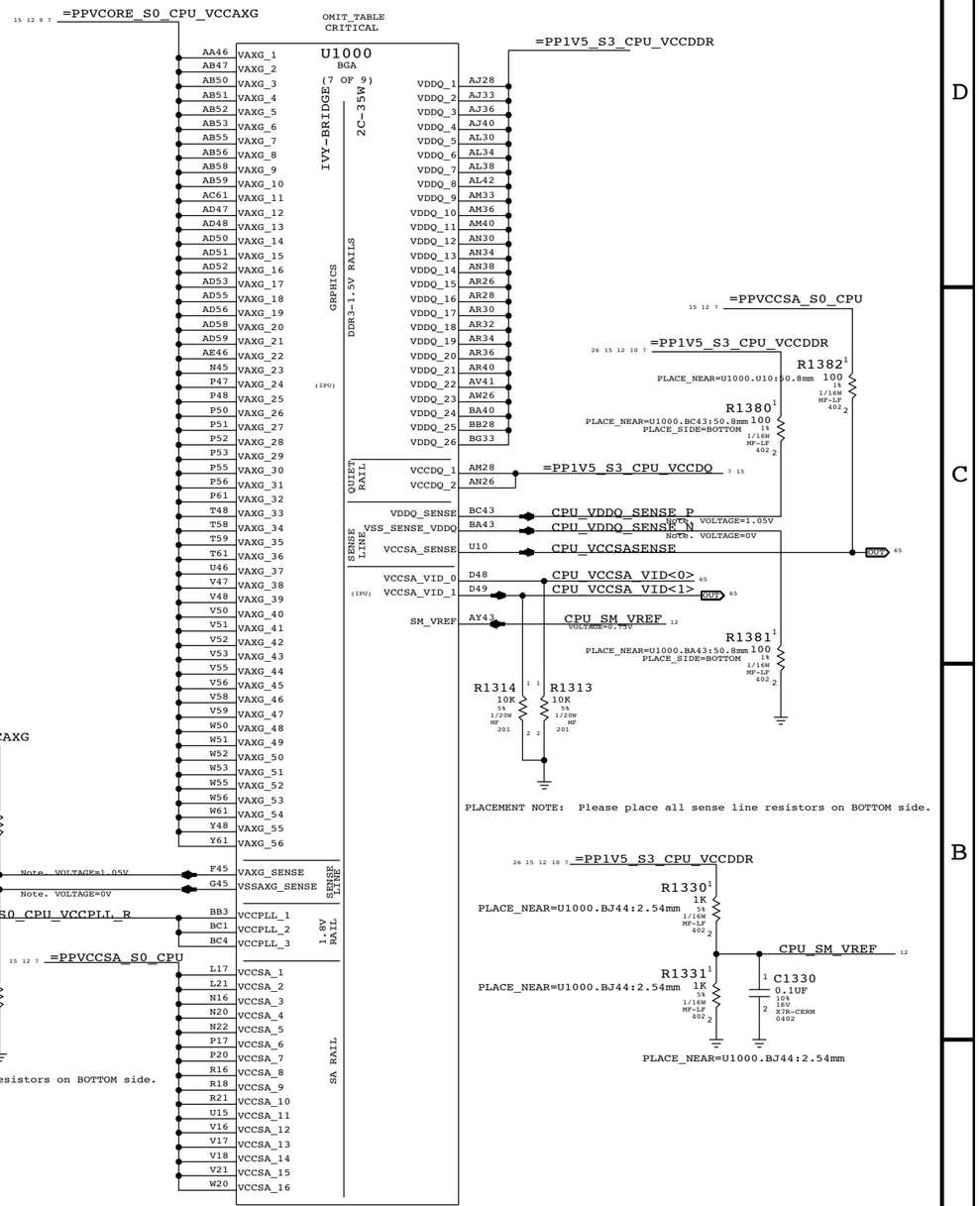

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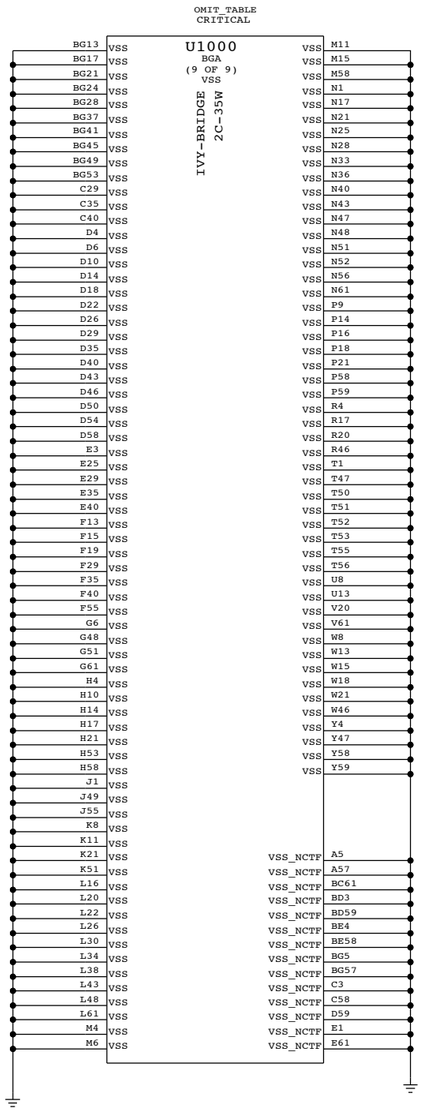

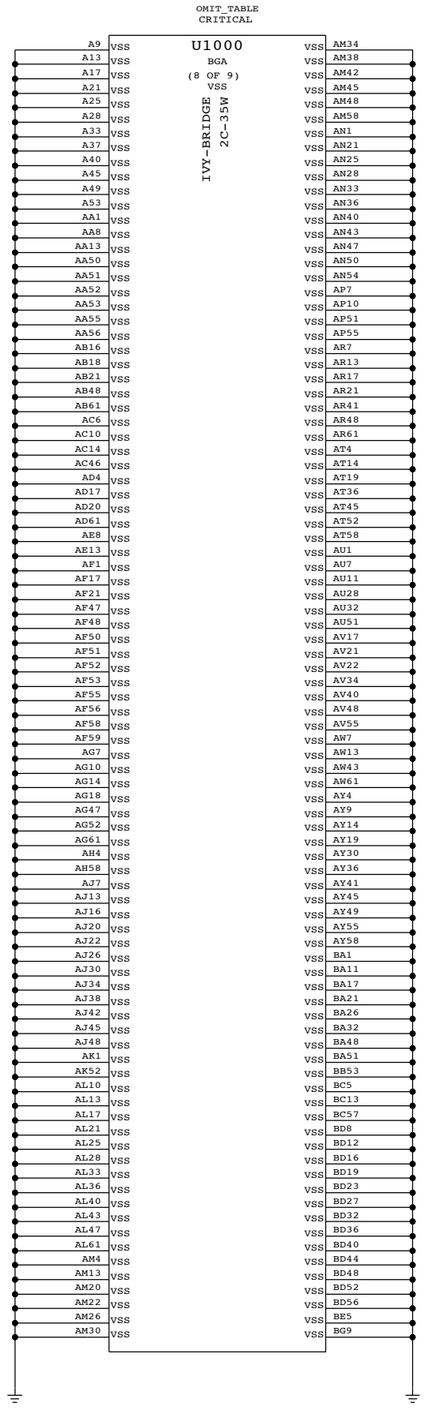

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CPU GROUNDS

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

12 9 7 =PPVCORE_S0_CPU

C1600 C1604 C1606 C1607 C1608 C1609 C1610 C1612 C1613 C1615 C1617 C1623 C1624
2.2UF 20% 4V X5R 402 — CRITICAL

C1625 C1627 C1628 C1631 C1632 C1635 C1637 C1638 C1639 C1640 C1641 C1642 C1643 C1644 C1645 C1647 C1648
2.2UF 20% 4V X5R 402 — CRITICAL

C1650 C1651 C1652 C1653 C1654
2.2UF 20% 4V X5R 402 — CRITICAL

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 C1656 C1657 C1658 C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666
22UF 20% 6.3V X5R-CERM-1 603 — CRITICAL; OMIT; NOSTUFF

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679
22UF 20% 6.3V X5R-CERM-1 603 — CRITICAL; OMIT; NOSTUFF

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 C1681 C1682 C1683
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
1UF 10% 10V X5R 402

C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C
10UF 20% 6.3V CERM-X5R 0402-1

C167D C167E C167G C167H C167J
330UF 20% 2.5V TANT CASE-B2-SM1

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
=PP1V05_S0_CPU_VCCPQE 7 8 12
C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL
R1600 0 5% 1/16W MF-LF 402
=PP1V8_S0_CPU_VCCPLL_R 7 12
PLACE_NEAR=U1000.8C:15mm
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1655,C1660,C1661,C1664,C1666,C1667,C1670,C1677,C1678,C1679,C1657,C1672,C1658,C1669,C1668,C1656	CRITICAL	

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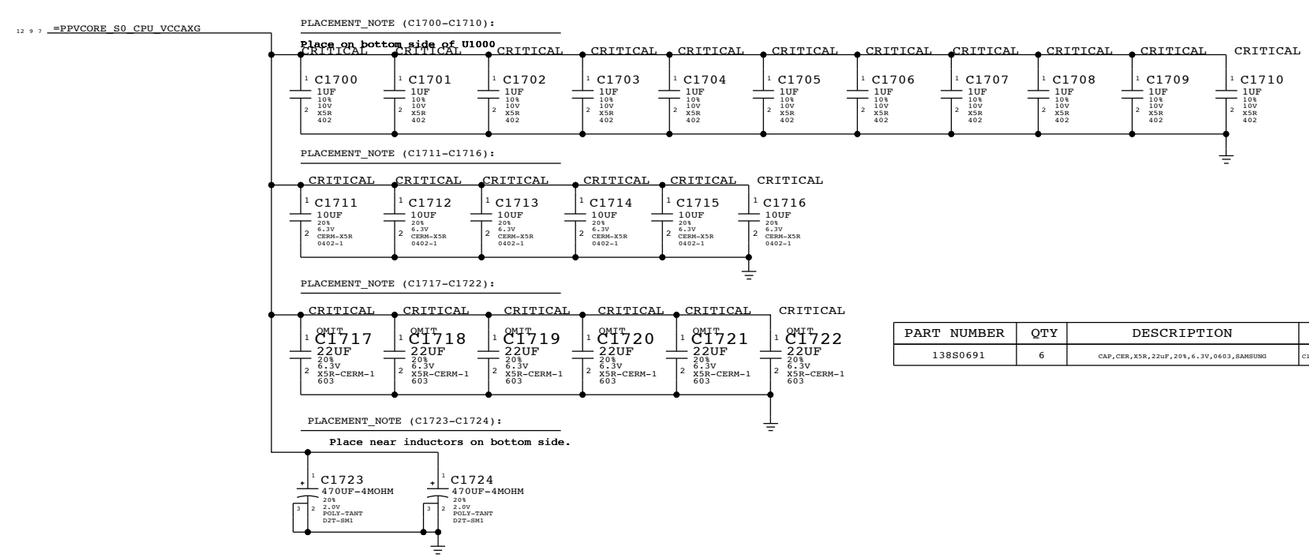
VAXG DECOUPLING

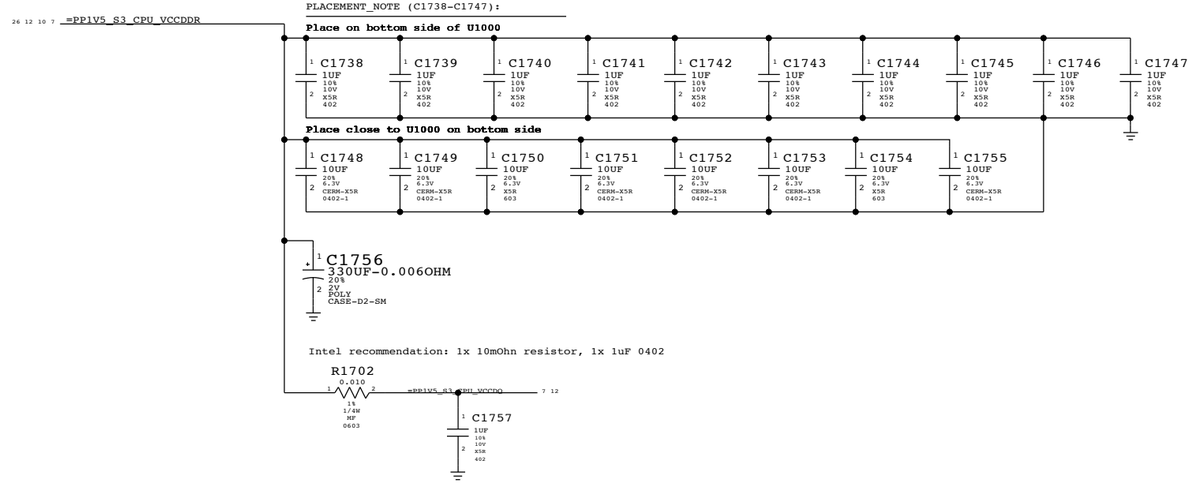
Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1717,C1718,C1719,C1720,C1721,C1722	CRITICAL	

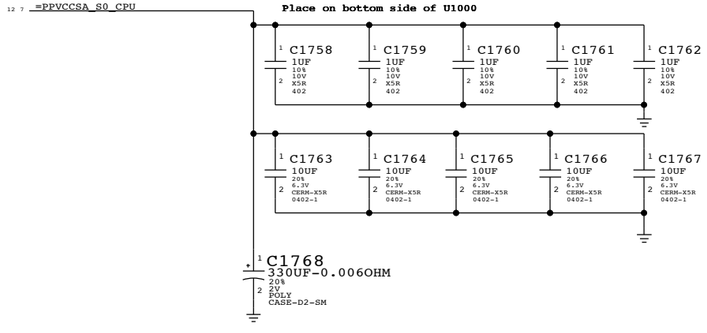
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF



CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf



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OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(1 OF 10)

RTC
LPC
IHDA
SATA
JTAG
SPI

SYSCLK_CLK32K_RTC — RTCX1 (A20)
NC — RTCX2 (C20)
RTC_RESET_L — RTCRST* (D20)
PCH_SRTCRST_L — SRTCRST* (G22)
PCH_INTRUDER_L — INTRUDER* (K22)
PCH_INTVRMEN_L — INTVRMEN (C17)

HDA_BIT_CLK_R — HDA_BCLK (N34)
HDA_SYNC_R — HDA_SYNC (IPD-BOOT) (L34)
VSel strap not functional (VCCVRM = 1.8V)
PCH_SPKR — SPKR (IPD-PLTRST#) (T10)
HDA_RST_R_L — HDA_RST* (K34)
HDA_SDIN0 — HDA_SDIN0 (IPD) (E34)
TP_HDA_SDIN1 — HDA_SDIN1 (IPD) (G34)
TP_HDA_SDIN2 — HDA_SDIN2 (IPD) (C34)
TP_HDA_SDIN3 — HDA_SDIN3 (IPD) (A34)
HDA_SDOUT_R — HDA_SDO (IPD-BOOT) (A36)
JTAG_TBT_TMS — HDA_DOCK_EN*/GPIO33 (C36)
ENET_MEDIA_SENSE_RDIV — HDA_DOCK_RST*/GPIO13 (N32)

XDP_PCH_TCK — JTAG_TCK (IPD) (J3)
XDP_PCH_TMS — JTAG_TMS (IPU) (H7)
XDP_PCH_TDI — JTAG_TDI (IPU) (K5)
XDP_PCH_TDO — JTAG_TDO (H1)

SPI_CLK_R — SPI_CLK (T3)
SPI_CS0_R_L — SPI_CS0* (Y14)
TP_SPI_CS1_L — SPI_CS1* (T1)
SPI_MOSI_R — SPI_MOSI (IPD-BOOT) (V4)
SPI_MISO — SPI_MISO (IPU) (U3)

=PPVRTC_G3_PCH
R1800 330K 5% 1/20W MF 201
R1801 1M 5% 1/20W MF 201
R1802 20K 5% 1/20W MF 201
R1803 20K 5% 1/20W MF 201
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
C1802 1UF 10% 10V X5R 402
C1803 1UF 10% 10V X5R 402

FWH0/LAD0 (C38) — LPC_AD_R<0>
FWH1/LAD1 (A38) — LPC_AD_R<1>
FWH2/LAD2 (B37) — LPC_AD_R<2>
FWH3/LAD3 (C37) — LPC_AD_R<3>
(IPU)
FWH4/LFRAME* (D36) — LPC_FRAME_R_L
(IPU) LDRQ0* (E36) — TP_LPC_DREQ0_L
LDRQ1*/GPIO23 (K36) — TBT_PWR_EN_PCH (OUT 24)
(IPU)
SERIRQ (V5) — LPC_SERIRQ (BI 6 45 47)
=PP3V3_S0_PCH
R1820 10K 5% 1/20W MF 201

SATA0RXN (AM3) — SATA_HDD_D2R_N (IN 41 80)
SATA0RXP (AM1) — SATA_HDD_D2R_P (IN 41 80)
SATA0TXN (AP7) — SATA_HDD_R2D_C_N (OUT 41 80)
SATA0TXP (AP5) — SATA_HDD_R2D_C_P (OUT 41 80)
SATA1RXN (AM10) — SATA_ODD_D2R_N (IN 41 80)
SATA1RXP (AM8) — SATA_ODD_D2R_P (IN 41 80)
SATA1TXN (AP11) — SATA_ODD_R2D_C_N (OUT 41 80)
SATA1TXP (AP10) — SATA_ODD_R2D_C_P (OUT 41 80)
SATA2RXN (AD7) — TP_SATA_C_D2RN (6)
SATA2RXP (AD5) — TP_SATA_C_D2RP (6)
SATA2TXN (AH5) — TP_SATA_C_R2D_CN (6)
SATA2TXP (AH4) — TP_SATA_C_R2D_CP (6)
SATA3RXN (AB8) — TP_SATA_D_D2RN (6)
SATA3RXP (AB10) — TP_SATA_D_D2RP (6)
SATA3TXN (AF3) — TP_SATA_D_R2D_CN (6)
SATA3TXP (AF1) — TP_SATA_D_R2D_CP (6)
SATA4RXN (Y7) — TP_SATA_E_D2RN (6)
SATA4RXP (Y5) — TP_SATA_E_D2RP (6)
SATA4TXN (AD3) — TP_SATA_E_R2D_CN (6)
SATA4TXP (AD1) — TP_SATA_E_R2D_CP (6)
SATA5RXN (Y3) — TP_SATA_F_D2RN (6)
SATA5RXP (Y1) — TP_SATA_F_D2RP (6)
SATA5TXN (AB3) — TP_SATA_F_R2D_CN (6)
SATA5TXP (AB1) — TP_SATA_F_R2D_CP (6)

=PP1V05_S0_PCH_VCCIO_SATA (7 20 22)
PLACE_NEAR=U1800.Y11:2.54mm
R1830 37.4 1% 1/20W MF 201
=PP1V05_S0_PCH (7 22)
R1831 49.9 1% 1/20W MF 201
SATAICOMPO (Y11) — PCH_SATAICOMP (80)
SATAICOMPI (Y10)
PLACE_NEAR=U1800.AB12:2.54mm
SATA3RCOMPO (AB12)
SATA3COMPI (AB13) — PCH_SATA3COMP
SATA3RBIAS (AH1) — PCH_SATA3RBIAS
PLACE_NEAR=U1800.AH1:2.54mm
R1832 750 1% 1/20W MF 201
SATALED* (P3) — PCH_SATALED_L (16)
SATA0GP/GPIO21 (V14) — XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL (OUT 23)
SATA1GP/GPIO19 (P1) (IPU) — XDP_DC3_PCH_GPIO19_SATARDRVR_EN (OUT 23)

LPC_AD_R<0> — R1860 33 5% 1/20W MF 201 — LPC_AD<0> (BI 6 45 47 81)
LPC_AD_R<1> — R1861 33 — LPC_AD<1> (BI 6 45 47 81)
LPC_AD_R<2> — R1862 33 — LPC_AD<2> (BI 6 45 47 81)
LPC_AD_R<3> — R1863 33 — LPC_AD<3> (BI 6 45 47 81)
LPC_FRAME_R_L — R1864 33 — LPC_FRAME_L (OUT 6 45 47 81)
HDA_BIT_CLK_R — R1810 33 PLACE_NEAR=U1800.N34:1.27mm — HDA_BIT_CLK (OUT 57 81)
HDA_SYNC_R — R1811 33 PLACE_NEAR=U1800.L34:1.27mm — HDA_SYNC (OUT 57 81)
HDA_RST_R_L — R1812 33 PLACE_NEAR=U1800.K34:1.27mm — HDA_RST_L (OUT 57 81)
HDA_SDOUT_R — R1813 33 PLACE_NEAR=U1800.A36:1.27mm — HDA_SDOUT (OUT 57 81)

=PP3V3_SUS_PCH_GPIO (7 17 18 19)
=PP3V3_S0_PCH_GPIO (7 17 18 19 30)
=PP3V3_T29_PCH_GPIO (7 19)

R1876 10K — JTAG_TBT_TMS (16 33)
R1877 4.7K — PCH_SPKR (16)
R1878 10K — PCH_SATALED_L (16)
R1834 10K — DP_AUXCH_ISOL (23 75)
R1833 10K — SATARDRVR_EN (23 41)
R1842 10K — FW_CLKREQ_L (16 39)
R1869 10K — AP_CLKREQ_L (16 32)
R1844 10K — EXCARD_CLKREQ_L (16)
R1845 10K — JTAG_DPMUXUC_TRST_L (16)
R1847 10K — ENET_CLKREQ_L (16 36)
R1814 10K — PEG_CLKREQ_L (16)
R1815 10K — TBT_CLKREQ_L (16 35)
R1843 10K — PCIECLKRQ0_L_GPIO73 (16)
R1846 10K — PEGCLKRQA_L_GPIO47 (16)
R1848 10K — PEGCLKRQB_L_GPIO56 (16)
R1853 10K — PCH_GPIO11 (16)
R1854 10K — USB_EXTB_SEL_XHCI (16 25)
R1855 10K — USB_EXTD_SEL_XHCI (16)
R1879 10K — ENET_MEDIA_SENSE_RDIV (16 24)

Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

NO STUFF
R1840 0 5% 1/20W MF 201
ITPCPU_CLK100M_N (78 10)
NO STUFF
R1841 0 5% 1/20W MF 201
ITPCPU_CLK100M_P (78 10)

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(2 OF 10)

PCI-E*
C-LINK
SMBUS
CLOCKS
FLEX CLOCKS

PCIE_ENET_D2R_N (81 36 IN) — PERN1 (BG34)
PCIE_ENET_D2R_P (81 36 IN) — PERP1 (BJ34)
PCIE_ENET_R2D_C_N (81 36 OUT) — PETN1 (AV32)
PCIE_ENET_R2D_C_P (81 36 OUT) — PETP1 (AU32)
PCIE_AP_D2R_N (81 32 IN) — PERN2 (BE34)
PCIE_AP_D2R_P (81 32 IN) — PERP2 (BF34)
PCIE_AP_R2D_C_N (81 32 OUT) — PETN2 (BB32)
PCIE_AP_R2D_C_P (81 32 OUT) — PETP2 (AY32)
PCIE_FW_D2R_N (81 38 IN) — PERN3 (BG36)
PCIE_FW_D2R_P (81 38 IN) — PERP3 (BJ36)
PCIE_FW_R2D_C_N (81 38 OUT) — PETN3 (AV34)
PCIE_FW_R2D_C_P (81 38 OUT) — PETP3 (AU34)
PCIE_EXCARD_D2R_N (8 IN) — PERN4 (BF36)
PCIE_EXCARD_D2R_P (8 IN) — PERP4 (BE36)
PCIE_EXCARD_R2D_C_N (8 OUT) — PETN4 (AY34)
PCIE_EXCARD_R2D_C_P (8 OUT) — PETP4 (BB34)
NC_PCIE_5_D2RN — PERN5 (BG37)
NC_PCIE_5_D2RP — PERP5 (BH37)
NC_PCIE_5_R2D_CN — PETN5 (AY36)
NC_PCIE_5_R2D_CP — PETP5 (BB36)
NC_PCIE_6_D2RN — PERN6 (BJ38)
NC_PCIE_6_D2RP — PERP6 (BG38)
NC_PCIE_6_R2D_CN — PETN6 (AU36)
NC_PCIE_6_R2D_CP — PETP6 (AV36)
NC_PCIE_7_D2RN — PERN7 (BG40)
NC_PCIE_7_D2RP — PERP7 (BJ40)
NC_PCIE_7_R2D_CN — PETN7 (AY40)
NC_PCIE_7_R2D_CP — PETP7 (BB40)
NC_PCIE_8_D2RN — PERN8 (BE38)
NC_PCIE_8_D2RP — PERP8 (BC38)
NC_PCIE_8_R2D_CN — PETN8 (AW38)
NC_PCIE_8_R2D_CP — PETP8 (AY38)

PCIE_CLK100M_ENET_N (81 36 OUT) — CLKOUT_PCIE0N (Y40)
PCIE_CLK100M_ENET_P (81 36 OUT) — CLKOUT_PCIE0P (Y39)
Controlled by PCIECLKRQ5#
PCIECLKRQ0_L_GPIO73 (16) — PCIECLKRQ0*/GPIO73 (J2)
PCIE_CLK100M_FW_N (81 38 OUT) — CLKOUT_PCIE1N (AB49)
PCIE_CLK100M_FW_P (81 38 OUT) — CLKOUT_PCIE1P (AB47)
FW_CLKREQ_L (39 16 IN) — PCIECLKRQ1*/GPIO18 (M1)
PCIE_CLK100M_AP_N (81 32 OUT) — CLKOUT_PCIE2N (AA48)
PCIE_CLK100M_AP_P (81 32 OUT) — CLKOUT_PCIE2P (AA47)
AP_CLKREQ_L (32 16 IN) — PCIECLKRQ2*/GPIO20 (V10)
PCIE_CLK100M_EXCARD_N (81 8 OUT) — CLKOUT_PCIE3N (Y37)
PCIE_CLK100M_EXCARD_P (81 8 OUT) — CLKOUT_PCIE3P (Y36)
EXCARD_CLKREQ_L (16 IN) — PCIECLKRQ3*/GPIO25 (A8)
TP_PCIE_CLK100M_PE4N (6) — CLKOUT_PCIE4N (Y43)
TP_PCIE_CLK100M_PE4P (6) — CLKOUT_PCIE4P (Y45)
JTAG_DPMUXUC_TRST_L (16 OUT) — PCIECLKRQ4*/GPIO26 (L12)
TP_PCIE_CLK100M_PE5N (6) — CLKOUT_PCIE5N (V45)
TP_PCIE_CLK100M_PE5P (6) — CLKOUT_PCIE5P (V46)
ENET_CLKREQ_L (36 16 IN) — PCIECLKRQ5*/GPIO44 (IPU-RSMRST#) (L14)
TP_PCIE_CLK100M_PEBN (6) — CLKOUT_PEG_B_N (AB42)
TP_PCIE_CLK100M_PEBP (6) — CLKOUT_PEG_B_P (AB40)
PEGCLKRQB_L_GPIO56 (16) — PEG_B_CLKRQ*/GPIO56 (E6)
PEG_CLK100M_N (81 8 OUT) — CLKOUT_PCIE6N (V40)
PEG_CLK100M_P (81 8 OUT) — CLKOUT_PCIE6P (V42)
PEG_CLKREQ_L (18 IN) — PCIECLKRQ6*/GPIO45 (T13)
PCIE_CLK100M_T29_N (81 33 OUT) — CLKOUT_PCIE7N (V38)
PCIE_CLK100M_T29_P (81 33 OUT) — CLKOUT_PCIE7P (V37)
TBT_CLKREQ_L (35 16 IN) — PCIECLKRQ7*/GPIO46 (IPU-RSMRST#) (K12)
ITPXDP_CLK100M_N (78 23) — CLKOUT_ITPXDP_N (AK14)
ITPXDP_CLK100M_P (78 23) — CLKOUT_ITPXDP_P (AK13)

SMBALERT*/GPIO11 (E12) — PCH_GPIO11 (16)
SMBCLK (H14) — SMBUS_PCH_CLK (OUT 48 81)
SMBDATA (C9) — SMBUS_PCH_DATA (BI 48 81)
SML0ALERT*/GPIO60 (A12) — USB_EXTB_SEL_XHCI (OUT 16 25)
SML0CLK (C8) — SML_PCH_0_CLK (OUT 48 81)
SML0DATA (G12) — SML_PCH_0_DATA (BI 48 81)
SML1ALERT*/PCHHOT*/GPIO74 (C13) — USB_EXTD_SEL_XHCI (OUT 16)
SML1CLK/GPIO58 (E14) — SML_PCH_1_CLK (OUT 48 81)
SML1DATA/GPIO75 (M16) — SML_PCH_1_DATA (BI 48 81)
(IPU/IPD) CL_CLK1 (M7) — TP_CLINK_CLK (6)
(IPU/IPD) CL_DATA1 (T11) — TP_CLINK_DATA (6)
CL_RST1* (P10) — TP_CLINK_RESET_L (6)

PEG_A_CLKRQ*/GPIO47 (M10) — PEGCLKRQA_L_GPIO47 (16)
CLKOUT_PEG_A_N (AB37) — TP_PCIE_CLK100M_PEGAN
CLKOUT_PEG_A_P (AB38) — TP_PCIE_CLK100M_PEGAP
CLKOUT_DMI_N (AV22) — DMI_CLK100M_CPU_N (OUT 10 78)
CLKOUT_DMI_P (AU22) — DMI_CLK100M_CPU_P (OUT 10 78)
CLKOUT_DP_N (AM12) — TP_PCH_CLKOUT_DPN (OUT 8)
CLKOUT_DP_P (AM13) — TP_PCH_CLKOUT_DPP (OUT 8)
CLKIN_DMI_N (BF18) — PCIE_CLK100M_PCH_N (IN 16 80)
CLKIN_DMI_P (BE18) — PCIE_CLK100M_PCH_P (IN 16 80)
CLKIN_GND1_N (BJ30) — PCH_CLKIN_GNDN1 (16)
CLKIN_GND1_P (BG30) — PCH_CLKIN_GNDP1 (16)
CLKIN_DOT_96N (G24) — PCH_CLK96M_DOT_N (IN 16 80)
CLKIN_DOT_96P (E24) — PCH_CLK96M_DOT_P (IN 16 80)
CLKIN_SATA_N (AK7) — PCH_CLK100M_SATA_N (IN 16 80)
CLKIN_SATA_P (AK5) — PCH_CLK100M_SATA_P (IN 16 80)
REFCLK14IN (K45) — PCH_CLK14P3M_REFCLK (IN 16 80)
CLKIN_PCILOOPBACK (H45) — PCH_CLK33M_PCIIN (IN 24 80)
DOES THIS NEED LENGTH MATCH???
XTAL25_IN (V47) — SYSCLK_CLK25M_SB_R (16 81)
XTAL25_OUT (V49) — NC
=PP1V05_S0_PCH_VCCDIFFCLK (22 20 7)
R1890 90.9 1% 1/20W MF 201
PLACE_NEAR=U1800.Y47:2.54mm
XCLK_RCOMP (Y47) — PCH_XCLK_RCOMP

CLKOUTFLEX0/GPIO64 (K43) (IPD-PWROK) — TP_PCH_GPIO64_CLKOUTFLEX0 (6)
CLKOUTFLEX1/GPIO65 (F47) (IPD-PWROK) — TP_PCH_GPIO65_CLKOUTFLEX1 (6)
CLKOUTFLEX2/GPIO66 (H47) (IPD-PWROK) — TP_PCH_GPIO66_CLKOUTFLEX2 (6)
CLKOUTFLEX3/GPIO67 (K49) (IPD-PWROK) — TP_PCH_GPIO67_CLKOUTFLEX3 (6)

SYSCLK_CLK25M_SB (81 24 IN) — R1872 604 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB_R (16 81)
1.8V -> 1.1V
R1873 1K 1% 1/20W MF 201

Unused clock terminations for FCIM Mode

PCH_CLK96M_DOT_P (80 16) — R1891 10K — PCH_CLK96M_DOT_P
PCH_CLK96M_DOT_N (80 16) — R1892 10K — PCH_CLK96M_DOT_N
PCH_CLK100M_SATA_P (80 16) — R1893 10K — PCH_CLK100M_SATA_P
PCH_CLK100M_SATA_N (80 16) — R1894 10K — PCH_CLK100M_SATA_N
PCIE_CLK100M_PCH_P (80 16) — R1895 10K — PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH_N (80 16) — R1896 10K — PCIE_CLK100M_PCH_N
PCH_CLK14P3M_REFCLK (80 16) — R1897 10K — PCH_CLK14P3M_REFCLK
PCH_CLKIN_GNDP1 (16) — R1870 10K — PCH_CLKIN_GNDP1
PCH_CLKIN_GNDN1 (16) — R1871 10K — PCH_CLKIN_GNDN1

SYNC_MASTER=J31_MLB SYNC_DATE=06/13/2011
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI

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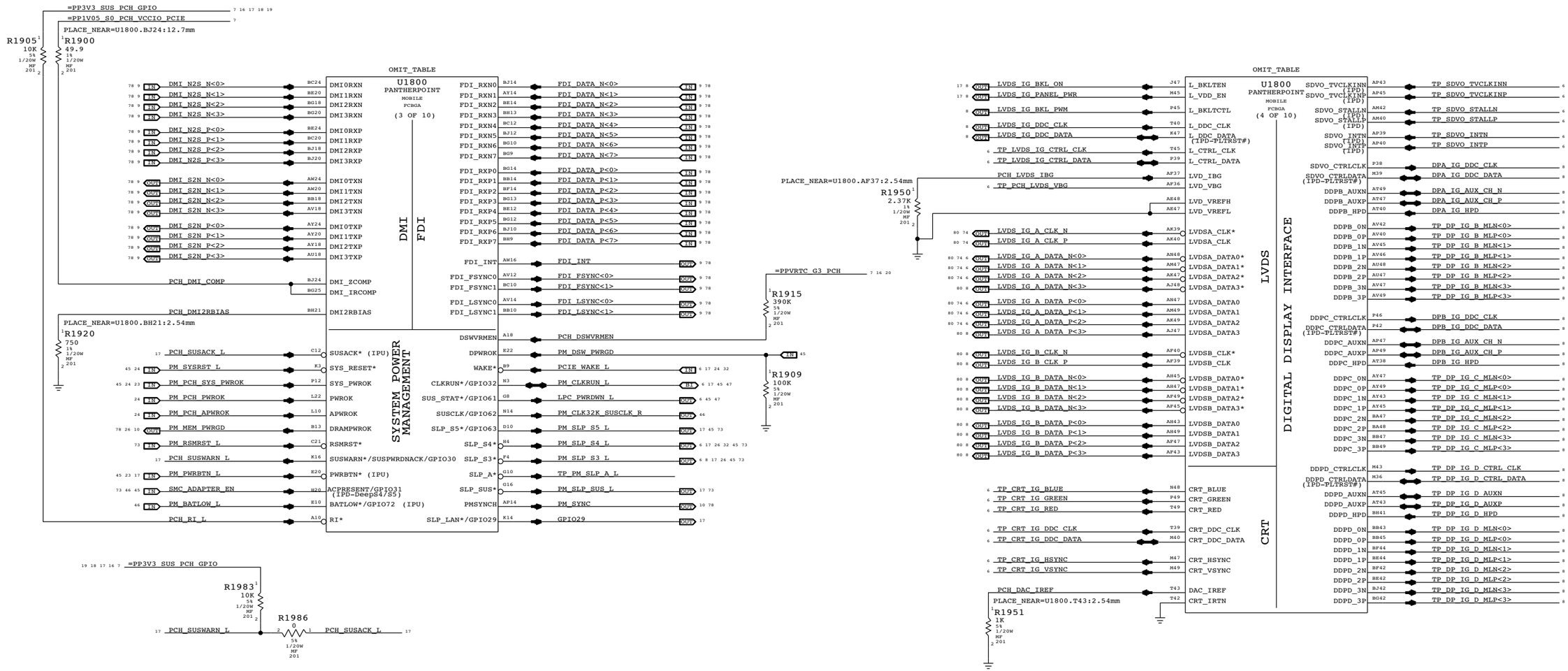

SYNC MASTER=J31 MLB	SYNC DATE=06/13/2011
PAGE TITLE	PCH DMI/FDI/PM/Graphics
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
	REVISION 6.0.0
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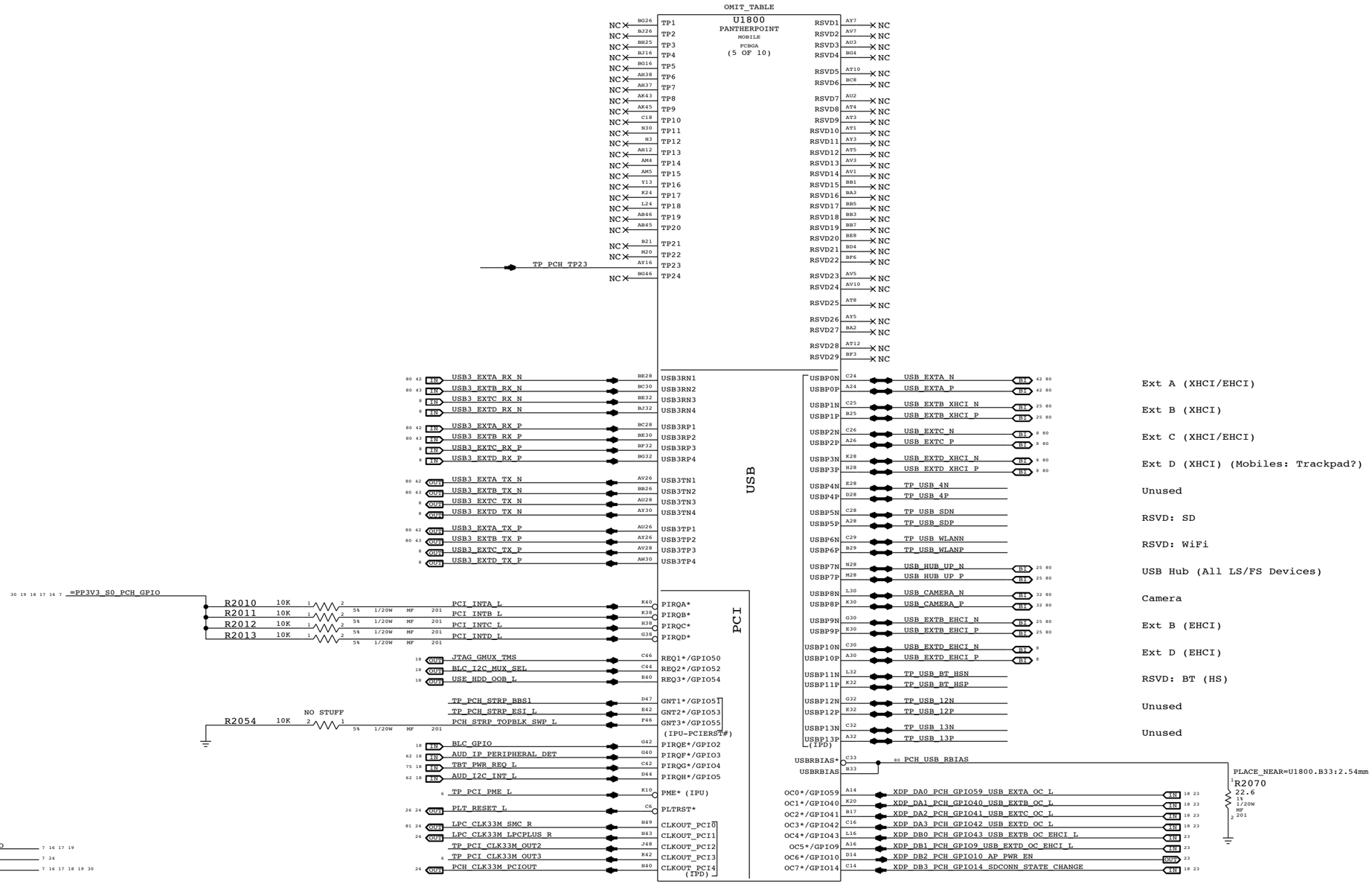

=PP3V3_S0_PCH_GPIO

R2010	10K	5%	1/20W	MF	201	PCI_INTA_L	
R2011	10K	5%	1/20W	MF	201	PCI_INTB_L	
R2012	10K	5%	1/20W	MF	201	PCI_INTC_L	
R2013	10K	5%	1/20W	MF	201	PCI_INTD_L	

=PP3V3_SUS_PCH_GPIO
=PP3V3_S3_PCH_GPIO
=PP3V3_S0_PCH_GPIO

R2016	10K	5%	1/20W	MF	201	JTAG_GMUX_TMS	18
R2017	10K	5%	1/20W	MF	201	BLC_I2C_MUX_SEL	18
R2018	10K	5%	1/20W	MF	201	USE_HDD_OOB_L	18
R2030	10K	5%	1/20W	MF	201	BLC_GPIO	18
R2014	10K	5%	1/20W	MF	201	AUD_IP_PERIPHERAL_DET	18 62
R2031	10K	5%	1/20W	MF	201	TBT_PWR_REQ_L	18 75
R2033	10K	5%	1/20W	MF	201	AUD_I2C_INT_L	18 62
R2069	10K	5%	1/20W	MF	201	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	18 23
R2060	10K	5%	1/20W	MF	201	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	18 23
R2061	10K	5%	1/20W	MF	201	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	18 23
R2062	10K	5%	1/20W	MF	201	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	18 23
R2068	10K	5%	1/20W	MF	201	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	18 23
R2067	10K	5%	1/20W	MF	201	AP_PWR_EN	23 32 73

Redundant to pull-up on audio page

SYNC_MASTER=J31_MLB	SYNC_DATE=06/13/2011
PAGE TITLE: PCH PCI/USB/TP/RSVD	
Apple Inc.	DRAWING NUMBER: 051-9058 SIZE: D
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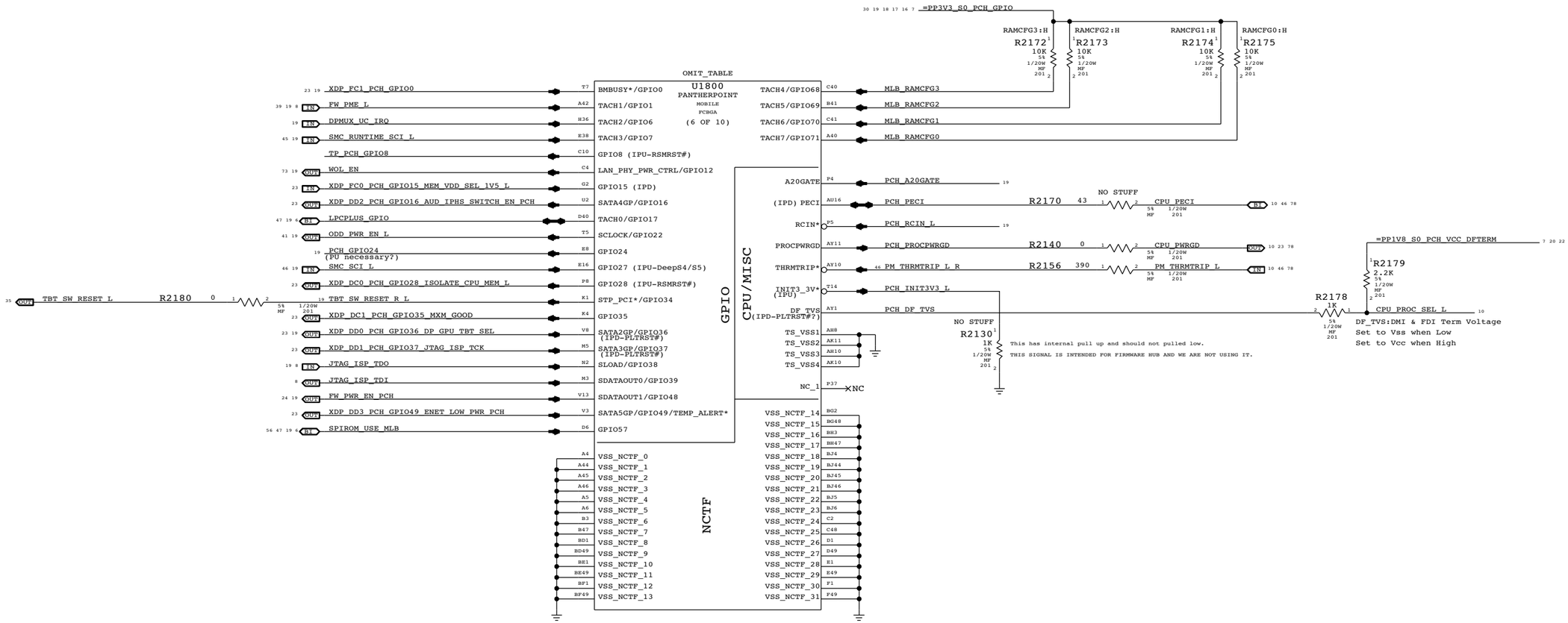
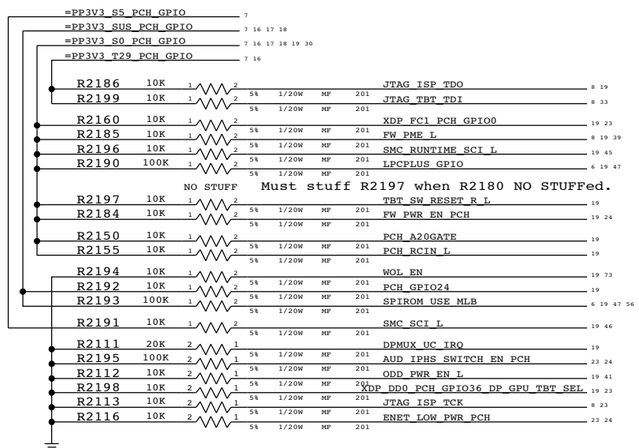
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.

Systems with chip-down memory should add pull-downs on another page and set straps per software.





SYNC MASTER=J31 MLB	SYNC DATE=06/13/2011
PAGE TITLE	PCH GPIO/MISC/NCTF
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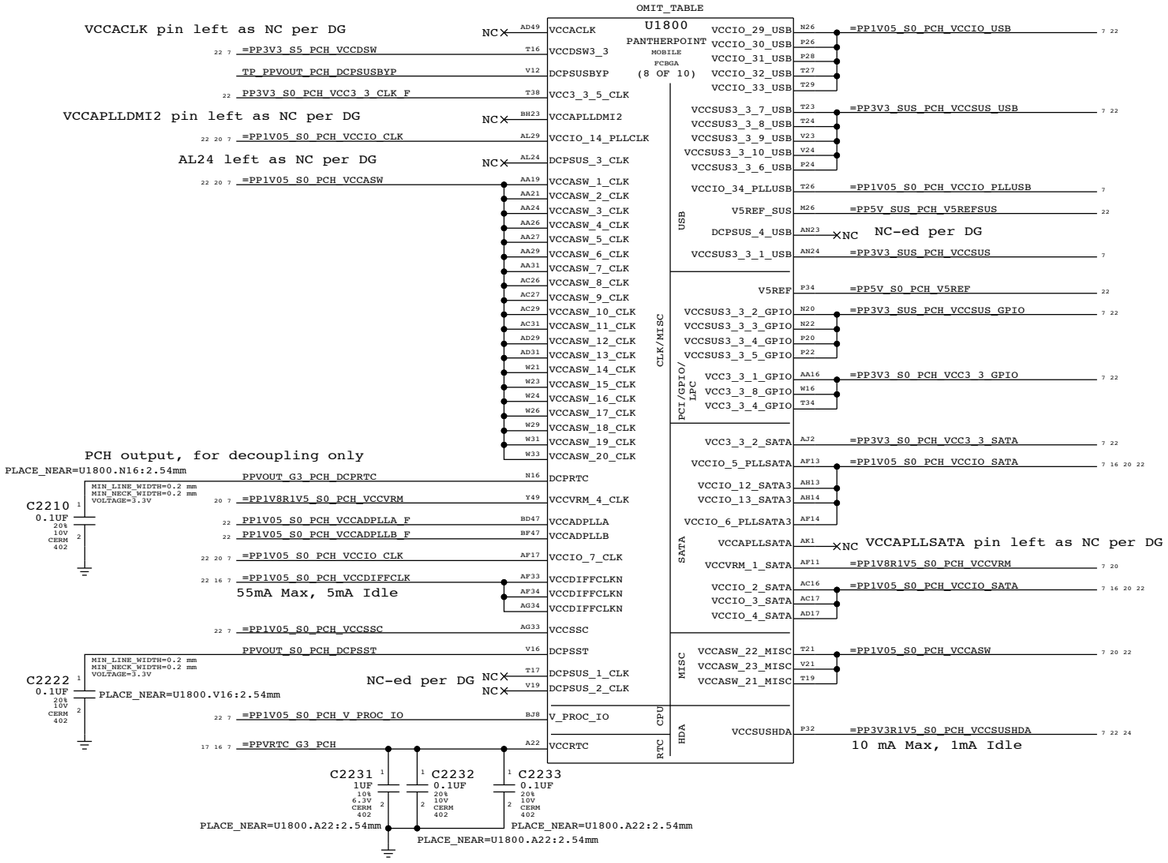

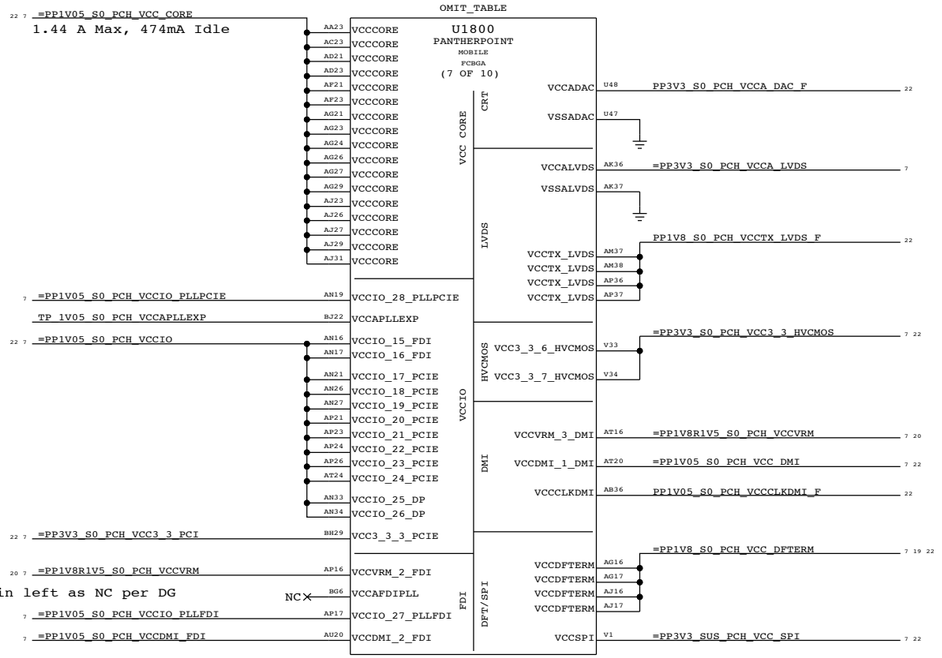

SYNC_MASTER=J31_MLB SYNC_DATE=06/13/2011

PAGE TITLE

PCH POWER

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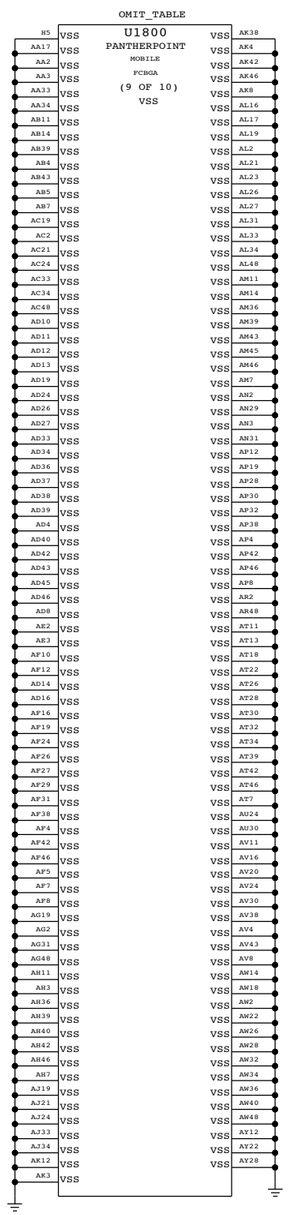

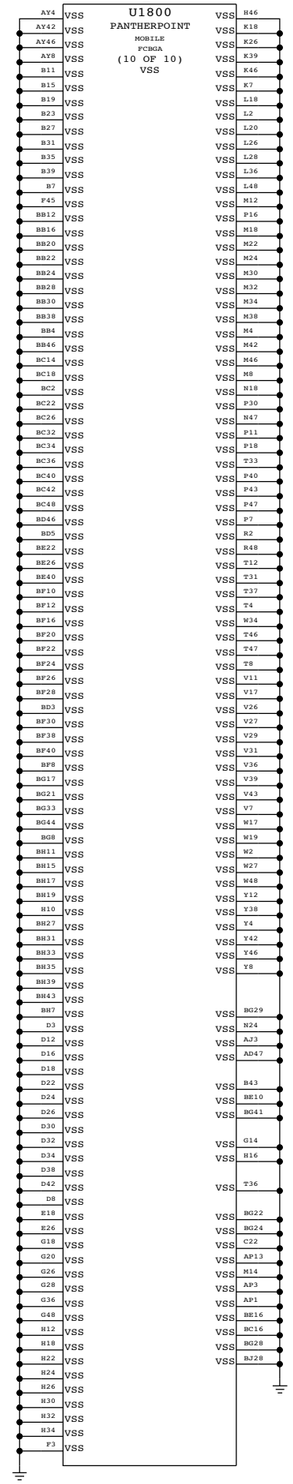

SYNC MASTER=J31 MLB SYNC DATE=06/13/2011

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PCH GROUNDS

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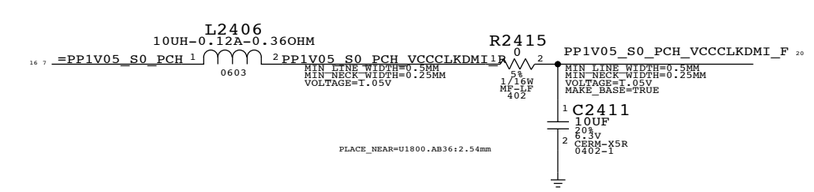

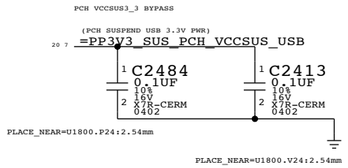

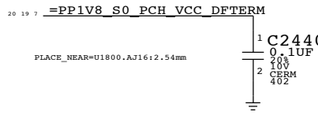

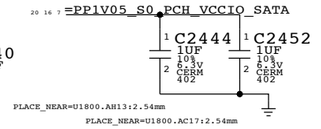

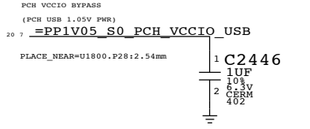

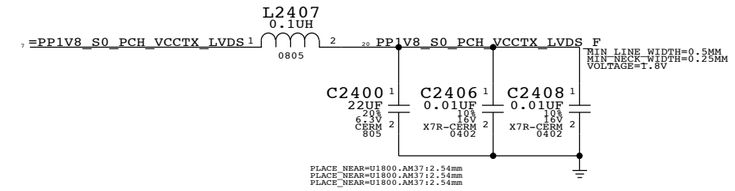

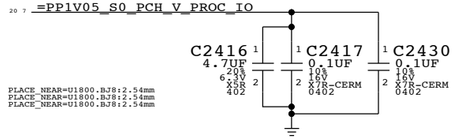

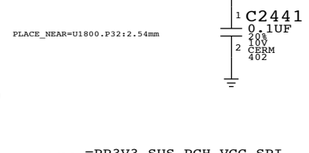

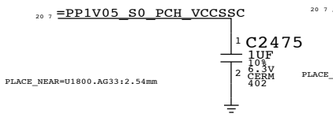

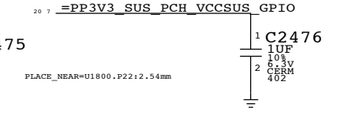

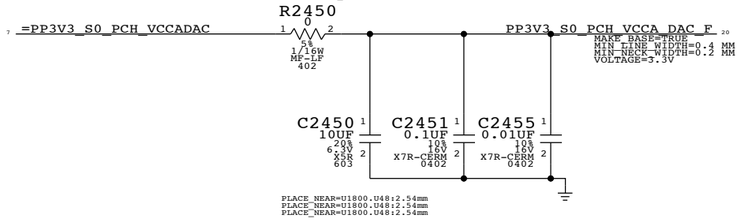

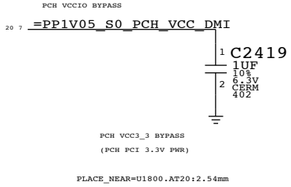

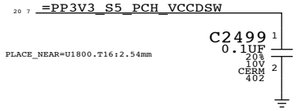

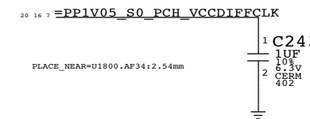

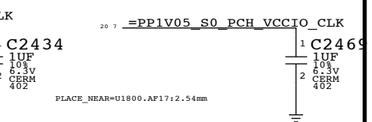

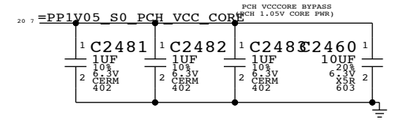

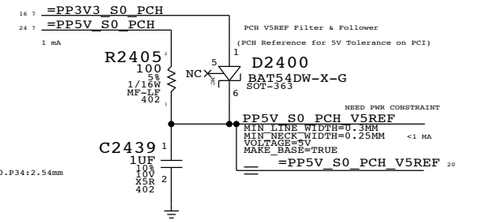

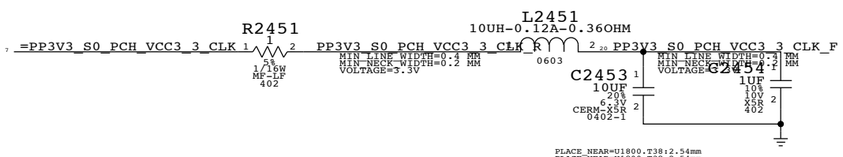

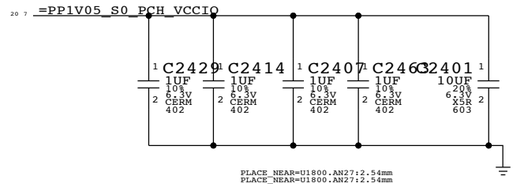

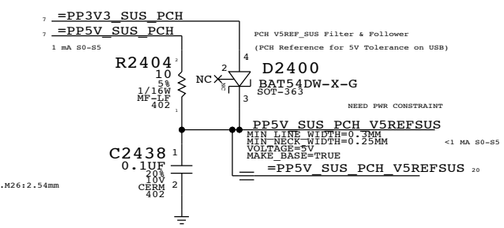

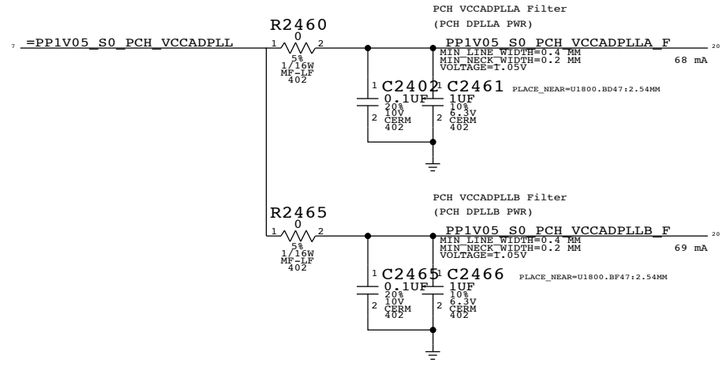

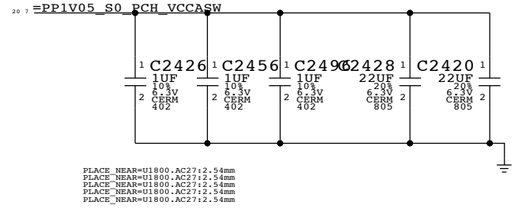

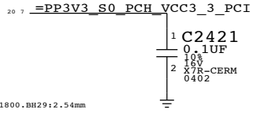

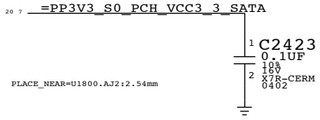

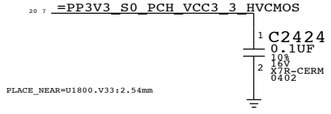

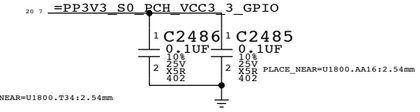

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

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CPU Micro2-XDP

=PPVCCIO_S0_XDP

CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402

(R2560-R2563)
XDP_CPU:BPM

XDP_BPM_L<4>	R2560	0	5% 1/20W MF 201
XDP_BPM_L<5>	R2561	0	5% 1/20W MF 201
XDP_BPM_L<6>	R2562	0	5% 1/20W MF 201
XDP_BPM_L<7>	R2563	0	5% 1/20W MF 201

(R2564-R2567)
XDP_CPU:CFG

CPU_CFG<12>	R2564	0	5% 1/20W MF 201
CPU_CFG<13>	R2565	0	5% 1/20W MF 201
CPU_CFG<14>	R2566	0	5% 1/20W MF 201
CPU_CFG<15>	R2567	0	5% 1/20W MF 201

CPU_PWRGD	R2500	1K	5% 1/20W MF 201
PM_PWRBTN_L	R2502	0	5% 1/20W MF 201
CPU_CFG<0>	R2501	1K	5% 1/20W MF 201
PM_PCH_SYS_PWROK	R2504	330	5% 1/20W MF 201

PLACE_NEAR=U1000.C60:2.54mm
PLACE_NEAR=U4900.P17:2.54mm
PLACE_NEAR=U1000.B57:2.54mm

XDP_BPM_L<0>	OBSDATA_A0	XDP_BPM_L<1>
XDP_BPM_L<2>	OBSDATA_A2	XDP_BPM_L<3>
CPU_CFG<10>	OBSFN_B0	CPU_CFG<11>
XDP_OBSDATA_B<0>	OBSDATA_B0	XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>	OBSDATA_B2	XDP_OBSDATA_B<3>
XDP_CPU_PWRGD	PWRGD/HOOK0	XDP_CPU_PWRBTN_L
	HOOK1	
VCC_OBS_AB	HOOK2	
XDP_CPU_CFG<0>	HOOK3	XDP_VR_READY
=SMBUS_XDP_SDA	SDA	
=SMBUS_XDP_SCL	SCL	
	TCK1	
XDP_CPU_TCK	TCK0	

R2581 1K 1/20W 201 5% MF
R2580 1K 1/20W 201 5% MF

OBSFN_A0	CPU_CFG<16>	OBSFN_C0
OBSFN_A1	CPU_CFG<17>	OBSFN_C1
OBSDATA_A0	CPU_CFG<0>	OBSDATA_C0
OBSDATA_A1	CPU_CFG<1>	OBSDATA_C1
OBSDATA_A2	CPU_CFG<2>	OBSDATA_C2
OBSDATA_A3	CPU_CFG<3>	OBSDATA_C3
OBSFN_B0	CPU_CFG<8>	OBSFN_D0
OBSFN_B1	CPU_CFG<9>	OBSFN_D1
OBSDATA_B0	CPU_CFG<4>	OBSDATA_D0
OBSDATA_B1	CPU_CFG<5>	OBSDATA_D1
OBSDATA_B2	CPU_CFG<6>	OBSDATA_D2
OBSDATA_B3	CPU_CFG<7>	OBSDATA_D3
ITPCLK/HOOK4	XDP_CPU_CLK100M_P	
ITPCLK#/HOOK5	XDP_CPU_CLK100M_N	
VCC_OBS_CD		
RESET#/HOOK6	XDPURST_L	
DBR#/HOOK7	XDP_DBRESET_L	
TDO	XDP_CPU_TDO	
TRSTn	XDP_CPU_TRST_L	
TDI	XDP_CPU_TDI	
TMS	XDP_CPU_TMS	
XDP_PRESENT#		

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2500 0.1UF 10% 16V X7R-CERM 0402
XDP C2501 0.1UF 10% 16V X7R-CERM 0402

998-2516

R2515	0	PLACE_NEAR=R1841.1:2.54mm ITPXDP_CLK100M_P 5% 1/20W MF 201
R2516	0	PLACE_NEAR=R1840.1:2.54mm ITPXDP_CLK100M_N 5% 1/20W MF 201
R2505	1K	PLACE_NEAR=U1000.G3:2.54mm CPU_RESET_L 5% 1/20W MF 201

XDP_CPU_TDO	R2510	51
XDP_CPU_TDI	R2511	51
XDP_CPU_TMS	R2512	51
XDP_CPU_TCK	R2513	51
XDP_CPU_TRST_L	R2514	51

=PPVCCIO_S0_XDP
PLACE_NEAR=J2500.52:2.54mm
PLACE_NEAR=U1000.K61:2.54mm
PLACE_NEAR=U1000.H59:2.54mm
PLACE_NEAR=U1000.J58:2.54mm
PLACE_NEAR=U1000.H63:2.54mm
5% 1/20W MF 201

XDP SIGNALS

(R2520-R2537)
XDP

XDP_DA0_USB_EXTA_OC_L	R2520	33	XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	
XDP_DA1_USB_EXTB_OC_L	R2521	33	XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	
XDP_DA2_USB_EXTC_OC_L	R2522	33	XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L	
XDP_DA3_USB_EXTD_OC_L	R2523	33	XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L	
XDP_DB0_USB_EXTB_OC_EHCI_L	R2524	33	XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI_L	
XDP_DB1_USB_EXTD_OC_EHCI_L	R2525	33	XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L	
XDP_DB2_AP_PWR_EN	R2526	33	XDP_DB2_PCH_GPIO10_AP_PWR_EN	
XDP_DB3_SDCONN_STATE_CHANGE	R2527	33	XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	
XDP_FC0	R2528	33	XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	
XDP_FC1	R2529	33	XDP_FC1_PCH_GPIO0	
XDP_DC0_ISOLATE_CPU_MEM_L	R2530	33	XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	
XDP_DC1_MXM_GOOD	R2531	33	XDP_DC1_PCH_GPIO35_MXM_GOOD	
XDP_DC2_DP_AUXCH_ISOL	R2532	33	XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	
XDP_DC3_SATARDRVR_EN	R2533	33	XDP_DC3_PCH_GPIO19_SATARDRVR_EN	
XDP_DD0_DP_GPU_TBT_SEL	R2534	33	XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL	
XDP_DD1_JTAG_ISP_TCK	R2535	33	XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	
XDP_DD2_AUD_IPHS_SWITCH_EN	R2536	33	XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	
XDP_DD3_ENET_LOW_PWR	R2537	33	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	

PCH SIGNALS

XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L	R2590	0	USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L	R2591	0	USB_EXTB_OC_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN	R2596	0	AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE	R2597	0	SDCONN_STATE_CHANGE
XDP_DC3_PCH_GPIO19_SATARDRVR_EN	R2573	0	SATARDRVR_EN
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L	R2570	0	ISOLATE_CPU_MEM_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL	R2572	0	DP_AUXCH_ISOL
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L	R2574	0	MEM_VDD_SEL_1V5_L

Non-XDP Signals

XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK	R2575	0	JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH	R2576	0	AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	R2577	0	ENET_LOW_PWR_PCH

5% 1/20W MF 201

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J2550
DF40RC-60DP-0.4V
M-ST-SM

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

TP_XDP_PCH_OBSFN_A<0>	OBSFN_A0	OBSFN_C0
TP_XDP_PCH_OBSFN_A<1>	OBSFN_A1	OBSFN_C1
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0
XDP_DA1_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1
XDP_DA2_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2
XDP_DA3_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3
TP_XDP_PCH_OBSFN_B<0>	OBSFN_B0	OBSFN_D0
TP_XDP_PCH_OBSFN_B<1>	OBSFN_B1	OBSFN_D1
XDP_DB0_USB_EXTB_OC_EHCI_L	OBSDATA_B0	OBSDATA_D0
XDP_DB1_USB_EXTD_OC_EHCI_L	OBSDATA_B1	OBSDATA_D1
XDP_DB2_AP_PWR_EN	OBSDATA_B2	OBSDATA_D2
XDP_DB3_SDCONN_STATE_CHANGE	OBSDATA_B3	OBSDATA_D3
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4
XDP_PCH_PWRBTN_L	HOOK1	ITPCLK#/HOOK5
	VCC_OBS_AB	VCC_OBS_CD
TP_XDPPCH_HOOK2	HOOK2	RESET#/HOOK6
TP_XDPPCH_HOOK3	HOOK3	DBR#/HOOK7
=SMBUS_XDP_SDA	SDA	TDO
=SMBUS_XDP_SCL	SCL	TRSTn
	TCK1	TDI
XDP_PCH_TCK	TCK0	TMS
		XDP_PRESENT#

XDP_FC0	XDP_PCH_HOOK4
XDP_FC1	XDP_PCH_HOOK5
XDP_DC0_ISOLATE_CPU_MEM_L	
XDP_DC1_MXM_GOOD	
XDP_DC2_DP_AUXCH_ISOL	
XDP_DC3_SATARDRVR_EN	
TP_XDP_PCH_OBSFN_D<0>	
TP_XDP_PCH_OBSFN_D<1>	
XDP_DD0_DP_GPU_TBT_SEL	
XDP_DD1_JTAG_ISP_TCK	
XDP_DD2_AUD_IPHS_SWITCH_EN	
XDP_DD3_ENET_LOW_PWR	
TP_XDP_PCH_HOOK4	
TP_XDP_PCH_HOOK5	
XDPPCH_PLTRST_L	
XDP_DBRESET_L	
XDP_PCH_TDO	
TP_XDP_PCH_TRST_L	
XDP_PCH_TDI	
XDP_PCH_TMS	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C2580 0.1UF 10% 16V X7R-CERM 0402
XDP C2581 0.1UF 10% 16V X7R-CERM 0402

998-2516

ALL_SYS_PWRGD	R2584	1K
PM_PWRBTN_L	R2585	0

PLACE_NEAR=J2550.39:2.54mm
PLACE_NEAR=U4900.P17:2.54mm
5% 1/20W MF 201

XDP_PCH_TDO	R2550	51
XDP_PCH_TDI	R2551	51
XDP_PCH_TMS	R2552	51
XDP_PCH_TCK	R2556	51

=PP1V05_SUS_PCH_JTAG
PLACE_NEAR=J2550.52:2.54mm
PLACE_NEAR=U1800.K5:2.54mm
PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.J3:2.54mm
5% 1/20W MF 201

1K series R on PCH Support Page

SYNC_MASTER=J31_MLB	SYNC_DATE=06/13/2011
PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
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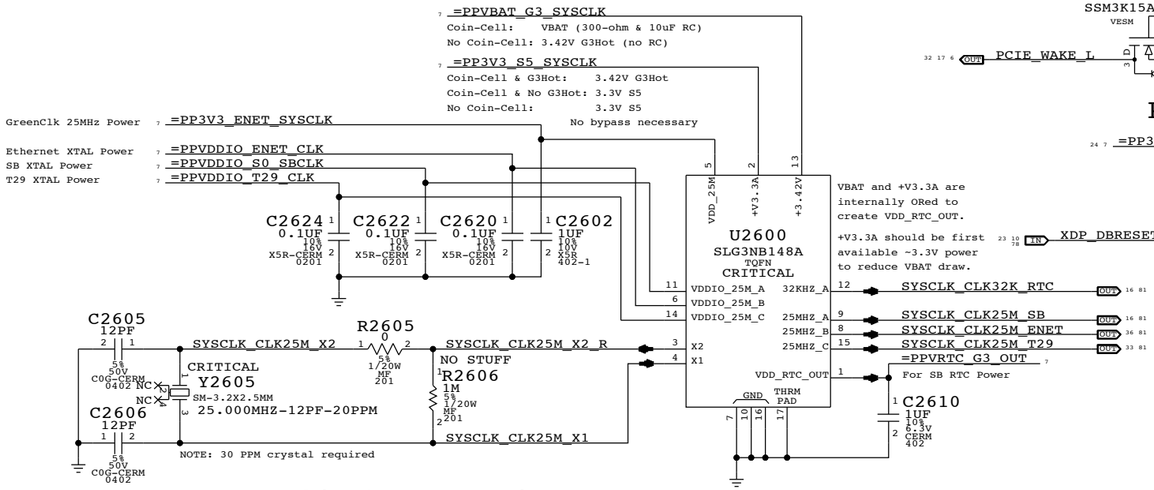
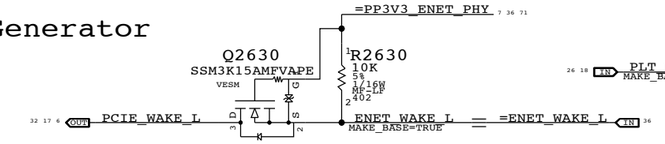
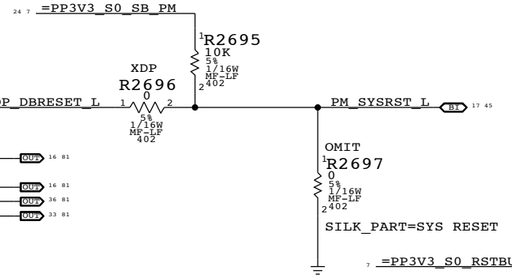
System RTC Power Source & 32kHz / 25MHz Clock Generator



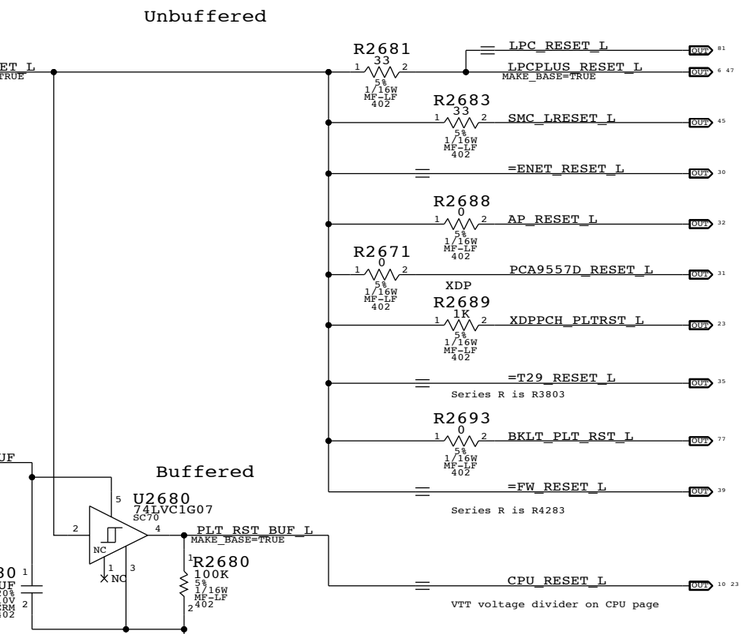
Ethernet WAKE# Isolation



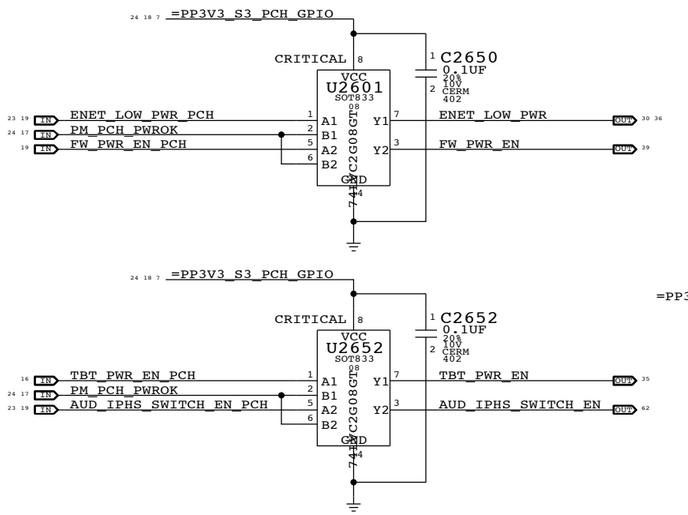
PCH Reset Button



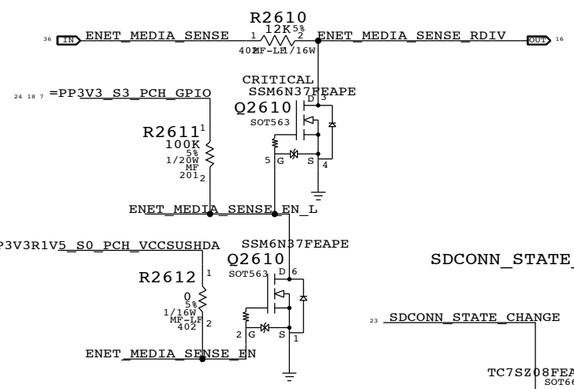
Platform Reset Connections



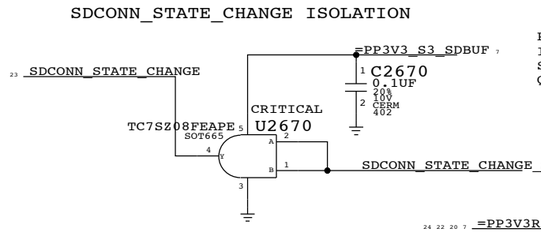
GPIO Glitch Prevention



ENET_MEDIA_SENSE ISOLATION CIRCUIT

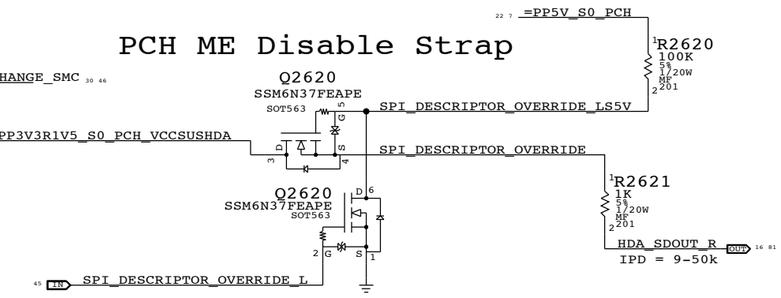


SDCONN_STATE_CHANGE ISOLATION

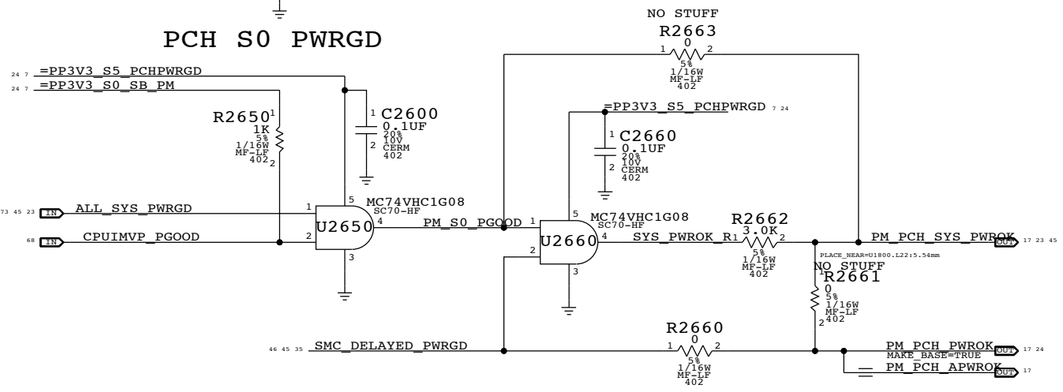


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH ME Disable Strap



PCH S0 PWRGD



Chipset Support

SYNC MASTER=K90I MLB	SYNC DATE=02/15/2011
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER 051-9058
	SIZE D
	REVISION 6.0.0
	BRANCH
	PAGE 26 OF 109
	SHEET 24 OF 86

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USB MUX FOR LS/FS INTERNAL DEVICES

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

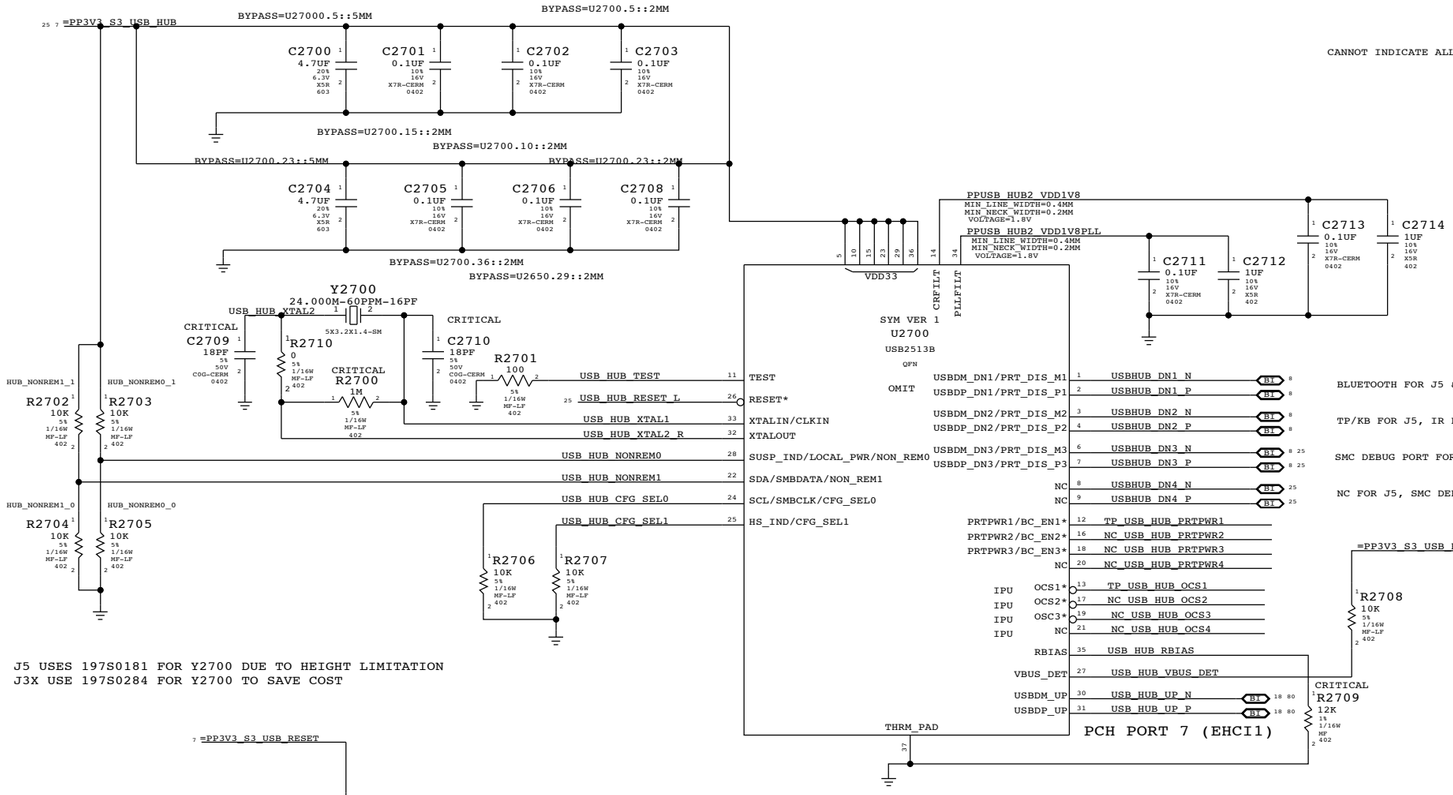
NON_REM 1 : NON_REM 0 STRAP PIN CFG
0 : 0 ALL PORTS ARE REMOVABLE
0 : 1 PORT 1 IS NON REMOVABLE
1 : 0 PORT 1&2 ARE NON REMOVABLE
1 : 1 PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

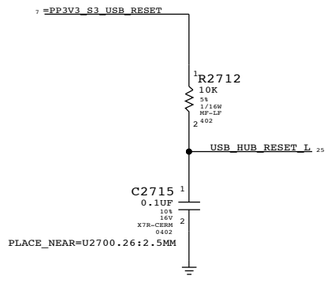
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

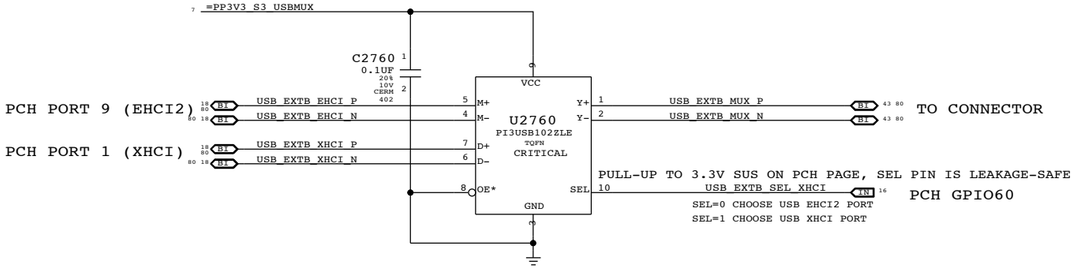
J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
J3X USE 197S0284 FOR Y2700 TO SAVE COST



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC_MASTER=LINDA J30 SYNC_DATE=09/19/2011
PAGE TITLE: USB HUB & MUX
Apple Inc.
DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
BRANCH
PAGE 27 OF 109
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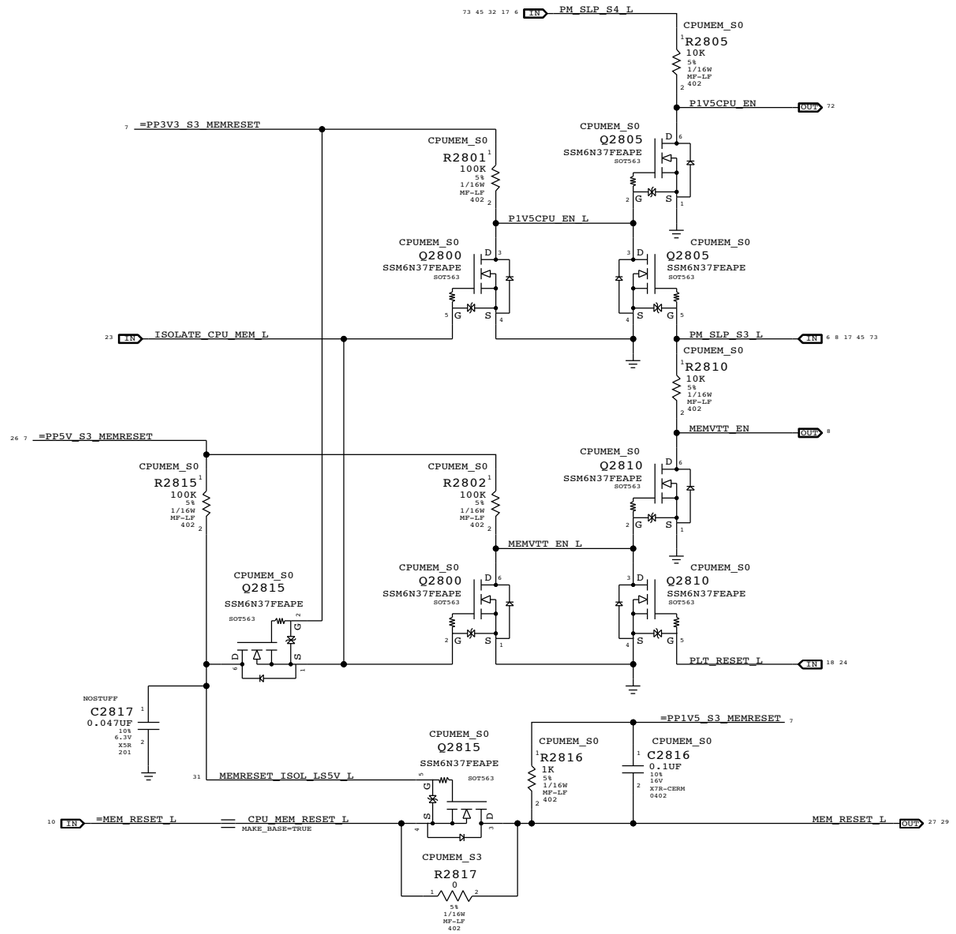
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

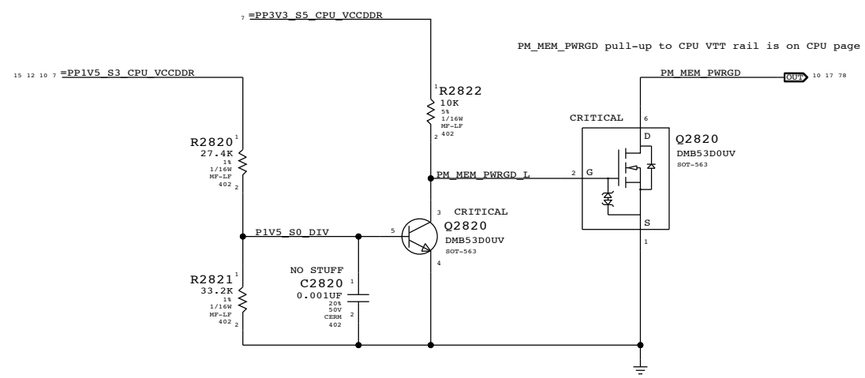


Step		ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
to	3	0	0	0	1	X	1	0	0
S0	4	0	0	1	1	X	1	0	1
	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

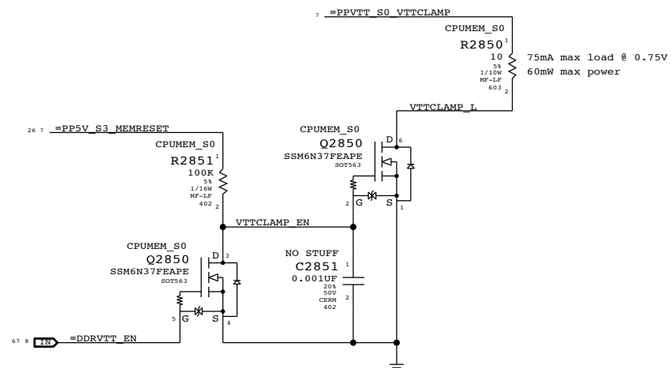
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC MASTER=K90I MLB — SYNC DATE=02/15/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9058 — SIZE: D

REVISION: 6.0.0

BRANCH:

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

7 =PP1V5_S3_MEM_A

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603

31 PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

OMIT_TABLE

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2)
KEY

73	CKE0	CKE1	74
75	VDD	VDD	76
77	NC	A15	78
79	BA2	A14	80
81	VDD	VDD	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD	VDD	88
89	A8	A6	90
91	A5	A4	92
93	VDD	VDD	94
95	A3	A2	96
97	A1	A0	98
99	VDD	VDD	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD	VDD	106
107	A10/AP	BA1	108
109	BA0	RAS*	110
111	VDD	VDD	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD	VDD	118
119	A13	ODT1	120
121	S1*	NC	122
123	VDD	VDD	124
125	TEST	VREFCA	126
127	VSS	VSS	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS	VSS	134
135	DQS4*	DM4	136
137	DQS4	VSS	138
139	VSS	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS	144
145	VSS	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS	150
151	VSS	DQS5*	152
153	DM5	DQS5	154
155	VSS	VSS	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS	VSS	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS	VSS	168
169	DQS6*	DM6	170
171	DQS6	VSS	172
173	VSS	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS	178
179	VSS	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS	184
185	VSS	DQS7*	186
187	DM7	DQS7	188
189	VSS	VSS	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS	VSS	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT	VTT	204

NC: 77, 125, 122

MEM_A_CKE<0>, MEM_A_BA<2>, MEM_A_A<12>, MEM_A_A<9>, MEM_A_A<8>, MEM_A_A<5>, MEM_A_A<3>, MEM_A_A<1>, MEM_A_CLK_P<0>, MEM_A_CLK_N<0>, MEM_A_A<10>, MEM_A_BA<0>, MEM_A_WE_L, MEM_A_CAS_L, MEM_A_A<13>, MEM_A_CS_L<1>
MEM_A_CKE<1>, MEM_A_A<15>, MEM_A_A<14>, MEM_A_A<11>, MEM_A_A<7>, MEM_A_A<6>, MEM_A_A<4>, MEM_A_A<2>, MEM_A_A<0>, MEM_A_CLK_P<1>, MEM_A_CLK_N<1>, MEM_A_BA<1>, MEM_A_RAS_L, MEM_A_CS_L<0>, MEM_A_ODT<0>, MEM_A_ODT<1>
MEM_A_DQ<32>, MEM_A_DQ<33>, MEM_A_DQS_N<4>, MEM_A_DQS_P<4>, MEM_A_DQ<34>, MEM_A_DQ<35>, MEM_A_DQ<40>, MEM_A_DQ<41>, MEM_A_DM<5>, MEM_A_DQ<42>, MEM_A_DQ<43>, MEM_A_DQ<48>, MEM_A_DQ<49>, MEM_A_DQS_N<6>, MEM_A_DQS_P<6>, MEM_A_DQ<50>, MEM_A_DQ<51>, MEM_A_DQ<56>, MEM_A_DQ<57>, MEM_A_DM<7>, MEM_A_DQ<58>, MEM_A_DQ<59>
MEM_A_DQ<36>, MEM_A_DQ<37>, MEM_A_DM<4>, MEM_A_DQ<38>, MEM_A_DQ<39>, MEM_A_DQ<44>, MEM_A_DQ<45>, MEM_A_DQS_N<5>, MEM_A_DQS_P<5>, MEM_A_DQ<46>, MEM_A_DQ<47>, MEM_A_DQ<52>, MEM_A_DQ<53>, MEM_A_DM<6>, MEM_A_DQ<54>, MEM_A_DQ<55>, MEM_A_DQ<60>, MEM_A_DQ<61>, MEM_A_DQS_N<7>, MEM_A_DQS_P<7>, MEM_A_DQ<62>, MEM_A_DQ<63>
MEM_EVENT_L
=I2C_SODIMMA_SDA
=I2C_SODIMMA_SCL

OMIT_TABLE

J2900 F-RT-THB
DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2)
CRITICAL
KEY

1	VREFDQ	VSS	2
3	VSS	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS	8
9	VSS	DQS0*	10
11	DM0	DQS0	12
13	VSS	VSS	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS	VSS	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS	VSS	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS	VSS	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS	VSS	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS	VSS	44
45	DQS2*	DM2	46
47	DQS2	VSS	48
49	VSS	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS	54
55	VSS	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS	60
61	VSS	DQS3*	62
63	DM3	DQS3	64
65	VSS	VSS	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS	VSS	72

MEM_A_DQ<0>, MEM_A_DQ<1>, MEM_A_DM<0>, MEM_A_DQ<2>, MEM_A_DQ<3>, MEM_A_DQ<8>, MEM_A_DQ<9>, MEM_A_DQS_N<1>, MEM_A_DQS_P<1>, MEM_A_DQ<10>, MEM_A_DQ<11>, MEM_A_DQ<16>, MEM_A_DQ<17>, MEM_A_DQS_N<2>, MEM_A_DQS_P<2>, MEM_A_DQ<18>, MEM_A_DQ<19>, MEM_A_DQ<24>, MEM_A_DQ<25>, MEM_A_DM<3>, MEM_A_DQ<26>, MEM_A_DQ<27>
MEM_A_DQ<4>, MEM_A_DQ<5>, MEM_A_DQS_N<0>, MEM_A_DQS_P<0>, MEM_A_DQ<6>, MEM_A_DQ<7>, MEM_A_DQ<12>, MEM_A_DQ<13>, MEM_A_DM<1>, MEM_RESET_L, MEM_A_DQ<14>, MEM_A_DQ<15>, MEM_A_DQ<20>, MEM_A_DQ<21>, MEM_A_DM<2>, MEM_A_DQ<22>, MEM_A_DQ<23>, MEM_A_DQ<28>, MEM_A_DQ<29>, MEM_A_DQS_N<3>, MEM_A_DQS_P<3>, MEM_A_DQ<30>, MEM_A_DQ<31>

PP0V75_S3_MEM_VREFCA_A 31

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

7 =PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

MEM_A_SA<0>
MEM_A_SA<1>
SPD ADDR=0xA0(WR)/0xA1(RD)

7 =PP0V75_S0_MEM_VTT_A

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011
PAGE TITLE: DDR3 SO-DIMM Connector A
Apple Inc.
DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

79 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	27
79 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	27
		MAKE_BASE=TRUE	=MEM_A_DM<0>	27
79 11	MEM_A_DQ<7>		=MEM_A_DQ<3>	27
79 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	27
79 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	27
79 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	27
79 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	27
79 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	27
79 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	27
79 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

79 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	27
79 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	27
		MAKE_BASE=TRUE	=MEM_A_DM<1>	27
79 11	MEM_A_DQ<15>		=MEM_A_DQ<11>	27
79 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	27
79 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	27
79 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	27
79 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	27
79 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	27
79 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	27
79 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

79 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	27
79 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	27
		MAKE_BASE=TRUE	=MEM_A_DM<2>	27
79 11	MEM_A_DQ<23>		=MEM_A_DQ<23>	27
79 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	27
79 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	27
79 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	27
79 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	27
79 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	27
79 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	27
79 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

79 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	27
79 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	27
		MAKE_BASE=TRUE	=MEM_A_DM<3>	27
79 11	MEM_A_DQ<31>		=MEM_A_DQ<26>	27
79 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	27
79 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	27
79 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	27
79 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	27
79 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	27
79 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	27
79 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

79 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	27
79 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	27
		MAKE_BASE=TRUE	=MEM_A_DM<4>	27
79 11	MEM_A_DQ<39>		=MEM_A_DQ<38>	27
79 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	27
79 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	27
79 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	27
79 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	27
79 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	27
79 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	27
79 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

79 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	27
79 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	27
		MAKE_BASE=TRUE	=MEM_A_DM<5>	27
79 11	MEM_A_DQ<47>		=MEM_A_DQ<46>	27
79 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	27
79 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	27
79 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	27
79 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	27
79 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	27
79 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	27
79 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

79 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	27
79 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	27
		MAKE_BASE=TRUE	=MEM_A_DM<6>	27
79 11	MEM_A_DQ<55>		=MEM_A_DQ<51>	27
79 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	27
79 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	27
79 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	27
79 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	27
79 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	27
79 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	27
79 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

79 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	27
79 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	27
		MAKE_BASE=TRUE	=MEM_A_DM<7>	27
79 11	MEM_A_DQ<63>		=MEM_A_DQ<58>	27
79 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	27
79 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	27
79 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	27
79 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	27
79 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	27
79 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	27
79 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	27
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

79 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	29
79 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	29
		MAKE_BASE=TRUE	=MEM_B_DM<0>	29
79 11	MEM_B_DQ<7>		=MEM_B_DQ<3>	29
79 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	29
79 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	29
79 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	29
79 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	29
79 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	29
79 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	29
79 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

79 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	29
79 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	29
		MAKE_BASE=TRUE	=MEM_B_DM<1>	29
79 11	MEM_B_DQ<15>		=MEM_B_DQ<15>	29
79 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	29
79 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	29
79 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	29
79 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	29
79 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	29
79 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	29
79 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

79 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	29
79 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	29
		MAKE_BASE=TRUE	=MEM_B_DM<2>	29
79 11	MEM_B_DQ<23>		=MEM_B_DQ<23>	29
79 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	29
79 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	29
79 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	29
79 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	29
79 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	29
79 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	29
79 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

79 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	29
79 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	29
		MAKE_BASE=TRUE	=MEM_B_DM<3>	29
79 11	MEM_B_DQ<31>		=MEM_B_DQ<26>	29
79 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	29
79 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	29
79 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	29
79 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	29
79 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	29
79 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	29
79 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

79 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	29
79 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	29
		MAKE_BASE=TRUE	=MEM_B_DM<4>	29
79 11	MEM_B_DQ<39>		=MEM_B_DQ<38>	29
79 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	29
79 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	29
79 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	29
79 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	29
79 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	29
79 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	29
79 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

79 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	29
79 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	29
		MAKE_BASE=TRUE	=MEM_B_DM<5>	29
79 11	MEM_B_DQ<47>		=MEM_B_DQ<43>	29
79 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	29
79 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	29
79 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	29
79 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	29
79 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	29
79 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	29
79 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

79 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	29
79 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	29
		MAKE_BASE=TRUE	=MEM_B_DM<6>	29
79 11	MEM_B_DQ<55>		=MEM_B_DQ<54>	29
79 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	29
79 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	29
79 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	29
79 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	29
79 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	29
79 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	29
79 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

79 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	29
79 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	29
		MAKE_BASE=TRUE	=MEM_B_DM<7>	29
79 11	MEM_B_DQ<63>		=MEM_B_DQ<56>	29
79 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	29
79 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	29
79 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	29
79 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	29
79 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	29
79 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	29
79 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	29
		MAKE_BASE=TRUE		

NOTE: Ivybridge does not use DM signals per doc 460452 CR SFF DG Section 2.6.14

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

BRANCH

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM8B_SCL
- =I2C_SODIMM8B_SDA

BOM options provided by this page:
(NONE)

7 =PP1V5_S3_MEM_B

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 C3118 C3119 C3120 C3121 C3122 C3123 0.1UF 20% 10V CERM 402

31 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (2 OF 2)

KEY

	CKE0	CKE1	MEM_B_CKE<1>
NC	VDD	VDD	
	NC	A15	MEM_B_A<15>
MEM_B_BA<2>	BA2	A14	MEM_B_A<14>
	VDD	VDD	
MEM_B_A<12>	A12/BC*	A11	MEM_B_A<11>
MEM_B_A<9>	A9	A7	MEM_B_A<7>
	VDD	VDD	
MEM_B_A<8>	A8	A6	MEM_B_A<6>
MEM_B_A<5>	A5	A4	MEM_B_A<4>
	VDD	VDD	
MEM_B_A<3>	A3	A2	MEM_B_A<2>
MEM_B_A<1>	A1	A0	MEM_B_A<0>
	VDD	VDD	
MEM_B_CLK_P<0>	CK0	CK1	MEM_B_CLK_P<1>
MEM_B_CLK_N<0>	CK0*	CK1*	MEM_B_CLK_N<1>
	VDD	VDD	
MEM_B_A<10>	A10/AP	BA1	MEM_B_BA<1>
MEM_B_BA<0>	BA0	RAS*	MEM_B_RAS_L
	VDD	VDD	
MEM_B_WE_L	WE*	S0*	MEM_B_CS_L<0>
MEM_B_CAS_L	CAS*	ODT0	MEM_B_ODT<0>
	VDD	VDD	
MEM_B_A<13>	A13	ODT1	MEM_B_ODT<1>
MEM_B_CS_L<1>	S1*	NC	NC
	VDD	VDD	
NC	TEST	VREFCA	
	VSS	VSS	
MEM_B_DQ<32>	DQ32	DQ36	MEM_B_DQ<36>
MEM_B_DQ<33>	DQ33	DQ37	MEM_B_DQ<37>
	VSS	VSS	
MEM_B_DQS_N<4>	DQS4*	DM4	MEM_B_DM<4>
MEM_B_DQS_P<4>	DQS4	VSS	
	VSS	DQ38	MEM_B_DQ<38>
MEM_B_DQ<34>	DQ34	DQ39	MEM_B_DQ<39>
MEM_B_DQ<35>	DQ35	VSS	
	VSS	DQ44	MEM_B_DQ<44>
MEM_B_DQ<40>	DQ40	DQ45	MEM_B_DQ<45>
MEM_B_DQ<41>	DQ41	VSS	
	VSS	DQS5*	MEM_B_DQS_N<5>
MEM_B_DM<5>	DM5	DQS5	MEM_B_DQS_P<5>
	VSS	VSS	
MEM_B_DQ<42>	DQ42	DQ46	MEM_B_DQ<46>
MEM_B_DQ<43>	DQ43	DQ47	MEM_B_DQ<47>
	VSS	VSS	
MEM_B_DQ<48>	DQ48	DQ52	MEM_B_DQ<52>
MEM_B_DQ<49>	DQ49	DQ53	MEM_B_DQ<53>
	VSS	VSS	
MEM_B_DQS_N<6>	DQS6*	DM6	MEM_B_DM<6>
MEM_B_DQS_P<6>	DQS6	VSS	
	VSS	DQ54	MEM_B_DQ<54>
MEM_B_DQ<50>	DQ50	DQ55	MEM_B_DQ<55>
MEM_B_DQ<51>	DQ51	VSS	
	VSS	DQ60	MEM_B_DQ<60>
MEM_B_DQ<56>	DQ56	DQ61	MEM_B_DQ<61>
MEM_B_DQ<57>	DQ57	VSS	
	VSS	DQS7*	MEM_B_DQS_N<7>
MEM_B_DM<7>	DM7	DQS7	MEM_B_DQS_P<7>
	VSS	VSS	
MEM_B_DQ<58>	DQ58	DQ62	MEM_B_DQ<62>
MEM_B_DQ<59>	DQ59	DQ63	MEM_B_DQ<63>
	VSS	VSS	
MEM_B_SA<0>	SA0	EVENT*	MEM_EVENT_L
	VDDSPD	SDA	=I2C_SODIMM8B_SDA
MEM_B_SA<1>	SA1	SCL	=I2C_SODIMM8B_SCL
	VTT	VTT	=PP0V75_S0_MEM_VTT_B
MTG PINS			
MTG PIN	MTG PIN	MTG PIN	MTG PIN
MTG PIN	MTG PIN	MTG PIN	MTG PIN
MTG PIN	MTG PIN	MTG PIN	MTG PIN
MTG PIN	MTG PIN	MTG PIN	MTG PIN

OMIT_TABLE

J3100 F-RT-BGA6 DDR3-SODIMM (1 OF 2)

CRITICAL

VREFDQ		VSS	
VSS		DQ4	=MEM_B_DQ<4>
DQ0		DQ5	=MEM_B_DQ<5>
DQ1		VSS	
VSS		DQS0*	=MEM_B_DQS_N<0>
DM0		DQS0	=MEM_B_DQS_P<0>
VSS		VSS	
DQ2		DQ6	=MEM_B_DQ<6>
DQ3		DQ7	=MEM_B_DQ<7>
VSS		VSS	
DQ8		DQ12	=MEM_B_DQ<12>
DQ9		DQ13	=MEM_B_DQ<13>
VSS		DM1	=MEM_B_DM<1>
DQS1*		RESET*	MEM_RESET_L
DQS1		VSS	
VSS		DQ14	=MEM_B_DQ<14>
DQ10		DQ15	=MEM_B_DQ<15>
DQ11		VSS	
VSS		DQ20	=MEM_B_DQ<20>
DQ16		DQ21	=MEM_B_DQ<21>
DQ17		VSS	
VSS		DM2	=MEM_B_DM<2>
DQS2*		VSS	
DQS2		DQ22	=MEM_B_DQ<22>
VSS		DQ23	=MEM_B_DQ<23>
DQ18		VSS	
DQ19		DQ28	=MEM_B_DQ<28>
VSS		DQ29	=MEM_B_DQ<29>
DQ24		VSS	
DQ25		DQS3*	=MEM_B_DQS_N<3>
VSS		DQS3	=MEM_B_DQS_P<3>
DM3		VSS	
VSS		DQ30	=MEM_B_DQ<30>
DQ26		DQ31	=MEM_B_DQ<31>
DQ27		VSS	

KEY

PP0V75_S3_MEM_VREFCA_B 31

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

7 =PPSPD_S0_MEM_B

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

SPD ADDR=0xA4(WR)/0xA5(RD)

7 =PP0V75_S0_MEM_VTT_B

C3150 C3151 C3152 C3153 1UF 10% 10V X5R 402

"Expansion" (bottom) slot

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

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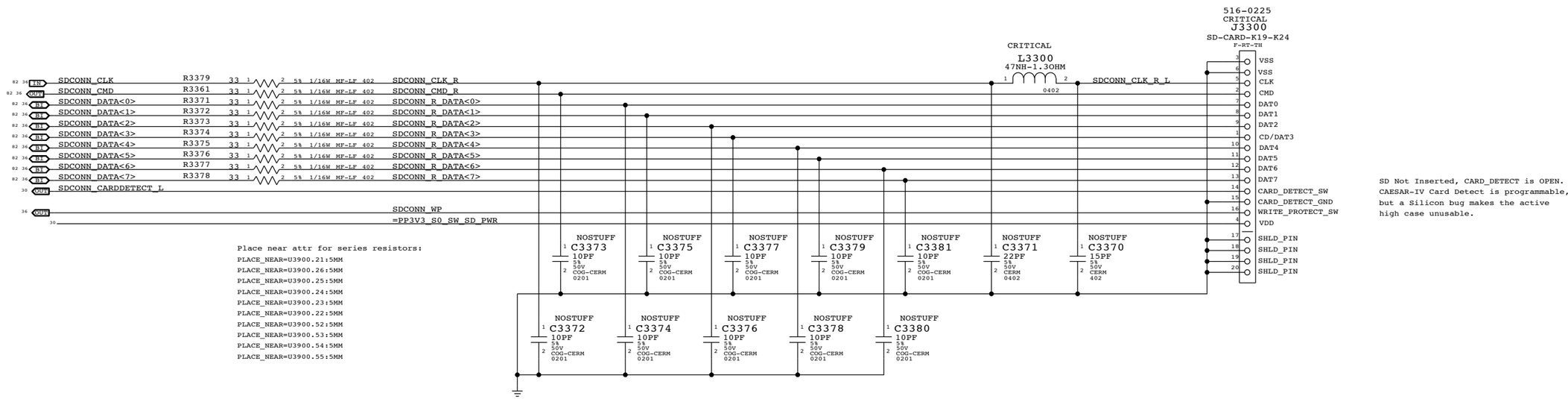
SD Card Connector



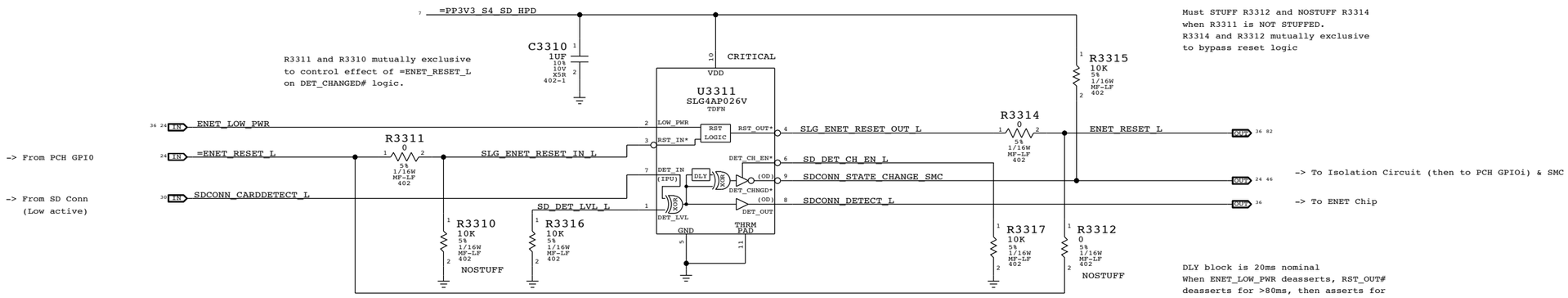
Place near attr for series resistors:

PLACE_NEAR=U3900.21:5MM
PLACE_NEAR=U3900.26:5MM
PLACE_NEAR=U3900.25:5MM
PLACE_NEAR=U3900.24:5MM
PLACE_NEAR=U3900.23:5MM
PLACE_NEAR=U3900.22:5MM
PLACE_NEAR=U3900.52:5MM
PLACE_NEAR=U3900.53:5MM
PLACE_NEAR=U3900.54:5MM
PLACE_NEAR=U3900.55:5MM

SD Not Inserted, CARD_DETECT is OPEN.
CAESAR-IV Card Detect is programmable,
but a Silicon bug makes the active
high case unusable.

SD Detect & Reset Logic

SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses.

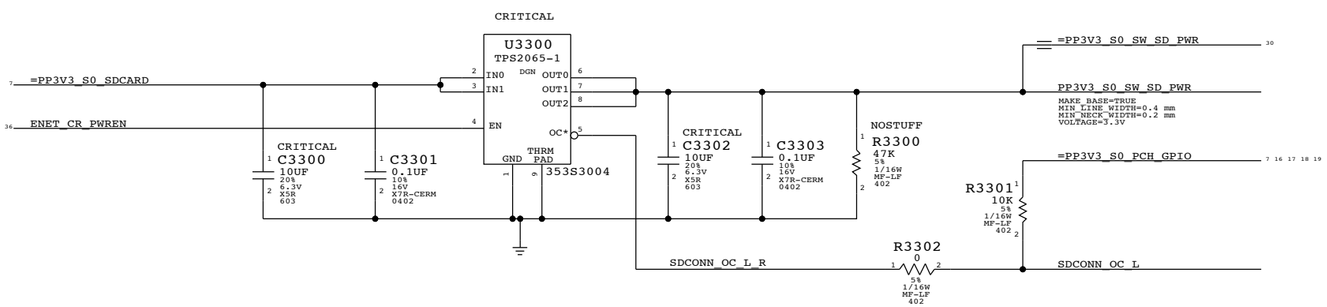


Must STUFF R3312 and NOSTUFF R3314
when R3311 is NOT STUFFED.
R3314 and R3312 mutually exclusive
to bypass reset logic

DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT#
deasserts for >80ms, then asserts for
10ms regardless ofmove RST_IN# state.
Otherwise RST_OUT# follows RST_IN#

SD Card 3.3V Overcurrent Protection

TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SYNC_MASTER=YONAS_J30	SYNC_DATE=11/03/2011
PAGE TITLE	SD Card Connector
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Addr=0x98(WR)/0x99(RD)

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

Addr=0x30(WR)/0x31(RD)

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J31 MLB SYNC DATE=06/13/2011

PAGE TITLE: DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D
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AIRPORT

C3531 0.1UF 10% 16V X5R-CERM 0201 — PCIE_AP_R2D_C_P, PCIE_AP_R2D_C_N
C3530 0.1UF 10% 16V X5R-CERM 0201

R3510 0 5% 1/20W MF 201 — PCIE_AP_D2R_P
R3511 0 5% 1/20W MF 201 — PCIE_AP_D2R_N

R3500 0 5% 1/16W MF-LF 402 — AP_TEMP_SMB_SDA_R — =AP_TEMP_SMB_SDA
R3501 0 5% 1/16W MF-LF 402 — AP_TEMP_SMB_SCL_R — =AP_TEMP_SMB_SCL
R3502 0 5% 1/16W MF-LF 402 — WIFI_EVENT_L_R — WIFI_EVENT_L

516S0582
CRITICAL
J3501
500913-0302
F-ST-SM

PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N

CRITICAL
L3501
330-OHM-80MA
DLP11S
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N

PP3V3_S3RS4_BT_F
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.5 mm

C3532 0.01UF 10% 16V X7R-CERM 0402
L3505 BTPWR:S4 FERR-120-OHM-1.5A 0402-LF =PP3V3_S4_BT
L3506 BTPWR:S3 FERR-120-OHM-1.5A 0402-LF =PP3V3_S3_BT

BLUETOOTH

NOSTUFF R3517 15K 5% 1/20W MF 201
BTPWR:S3 R3518 0 5% 1/20W MF 201
NOSTUFF R3515 15K 5% 1/20W MF 201
NOSTUFF R3516 15K 5% 1/20W MF 201
BTPWR:S4 R3519 0 5% 1/20W MF 201

U3510 PI3USB102ZLE TQFN CRITICAL
VCC, GND, SEL
Y+, Y-, M+, M-, D+, D-, OE*
USB_BT_WAKEP
USB_BT_WAKEN
USB_BT_P
USB_BT_N

PM_SLP_S4_L
BTMUX_SEL

NOSTUFF C3511 0.01UF 10% 16V X7R-CERM 0402

SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

PP3V3_S3RS4_BT_F
C3510 0.1UF 10% 6.3V X5R 201
NOSTUFF R3514 15K 5% 1/20W MF 201
BTPWR:S4 R3512 15K 5% 1/20W MF 201
NOSTUFF R3513 15K 5% 1/20W MF 201

BTPWR:S4
CRITICAL
Q3510 SSM3K15AMFVAPE
=BT_WAKE_L

Supervisor & CLKFREG # ISolation

Delay = 60 ms +/- 20%

PP3V3_WLAN_F
R3553 100K 5% 1/16W MF-LF 402
R3554 232K 1% 1/16W MF-LF 402
P3V3WLAN_VMON
R3555 100K 5% 1/16W MF-LF 402

CRITICAL
U3540
SLG4AP016V
TDFN
VDD, SENSE, 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, THRM PAD, GND

=PP3V3_S3_WLAN
C3540 0.1uF 20% 10V CERM 402

AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L

518S0815
CRITICAL
J3502
8190-3506-K281
F-RT-SM1

PCIE_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L

PP5V_S3_ALSCAMERA_F
=I2C_ALS_SCL
=I2C_ALS_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm

ALS CAMERA

275 mA peak
206 mA nominal max

CRITICAL
L3507
90-OHM
DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACE_NEAR=J3502.2:2.54MM

PLACE_NEAR=J3502.6:2.54MM
L3508 FERR-120-OHM-1.5A 0402-LF =PP5V_S3_ALSCAMERA
C3552 0.1uF 20% 10V CERM 402

727 MA PEAK
606 MA NOMINAL MAX
15580367
L3504 FERR-120-OHM-3A
PP3V3_WLAN — PP3V3_WLAN_F
MIN_NECK_WIDTH=0.4 mm
MIN_LINE_WIDTH=1 mm
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.2 mm
C3522 0.1uF 20% 10V CERM 402
C3521 0.1uF 20% 10V CERM 402
C3520 10UF 20% 10V X5R 805

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

CRITICAL
Q3550
DMP2018LFK
DFN2563-6
C3550 0.1UF 10% 16V X5R 402-1
P3V3WLAN_SS
C3551 0.033UF 10% 16V X5R 402
R3550 33K 5% 1/16W MF-LF 402
R3551 10K 5% 1/16W MF-LF 402
PM_WLAN_EN_L

SYNC MASTER=K90I_MLB
SYNC DATE=02/15/2011

PAGE TITLE
X19/ALS/CAMERA CONNECTOR

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CRITICAL

OMIT_TABLE

U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_R2D_C_P<0>	C3600 0.1UF	PCIE_T29_R2D_P<0>	V19 PER_0_P
PCIE_T29_R2D_C_N<0>	C3601 0.1UF	PCIE_T29_R2D_N<0>	T19 PER_0_N
PCIE_T29_R2D_C_P<1>	C3602 0.1UF	PCIE_T29_R2D_P<1>	P19 PER_1_P
PCIE_T29_R2D_C_N<1>	C3603 0.1UF	PCIE_T29_R2D_N<1>	M19 PER_1_N
PCIE_T29_R2D_C_P<2>	C3604 0.1UF	PCIE_T29_R2D_P<2>	K19 PER_2_P
PCIE_T29_R2D_C_N<2>	C3605 0.1UF	PCIE_T29_R2D_N<2>	H19 PER_2_N
PCIE_T29_R2D_C_P<3>	C3606 0.1UF	PCIE_T29_R2D_P<3>	F19 PER_3_P
PCIE_T29_R2D_C_N<3>	C3607 0.1UF	PCIE_T29_R2D_N<3>	D19 PER_3_N

TRANSMIT

PET_0_P V21	PCIE_T29_D2R_C_P<0>	C3640 0.1UF	PCIE_T29_D2R_P<0> OUT
PET_0_N T21	PCIE_T29_D2R_C_N<0>	C3641 0.1UF	PCIE_T29_D2R_N<0> OUT
PET_1_P P21	PCIE_T29_D2R_C_P<1>	C3642 0.1UF	PCIE_T29_D2R_P<1> OUT
PET_1_N M21	PCIE_T29_D2R_C_N<1>	C3643 0.1UF	PCIE_T29_D2R_N<1> OUT
PET_2_P K21	PCIE_T29_D2R_C_P<2>	C3644 0.1UF	PCIE_T29_D2R_P<2> OUT
PET_2_N H21	PCIE_T29_D2R_C_N<2>	C3645 0.1UF	PCIE_T29_D2R_N<2> OUT
PET_3_P F21	PCIE_T29_D2R_C_P<3>	C3646 0.1UF	PCIE_T29_D2R_P<3> OUT
PET_3_N D21	PCIE_T29_D2R_C_N<3>	C3647 0.1UF	PCIE_T29_D2R_N<3> OUT

TP_TBT_MONDC0	B21	MONDC0
TP_TBT_MONDC1	A20	MONDC1

DEBUG: For monitoring current/voltage

TP_TBT_MONOBSP	K17	MONOBSP
TP_TBT_MONOBSN	M17	MONOBSN

DEBUG: For monitoring clock

WAKE* F1 T29_PCIE_WAKE_L — R3651 10K 5% 1/20W MF 201 — =PP3V3_T29_RTR

PERST* E6 T29_RESET_L IN

RSENSE E14 T29_RSENSE — R3655 1K 1% 1/16W MF-LF 402

RBIAS E16 T29_RBIAS

MISC

CLK REQUEST

=T29_CLKREQ_L	P3	PCIE_CLKREQ_0*
T29_GIO<1>	N4	PCIE_CLKREQ_1*
T29_GIO<2>	M3	PCIE_CLKREQ_2*
T29_RSVD	L4	PCIE_CLKREQ_3*

EEPROM

T29_SPI_MOSI	P1	EE_DI
T29_SPI_MISO	M1	EE_DO
T29_SPI_CS_L	N2	EE_CS*
T29_SPI_CLK	L2	EE_CLK

TP_T29_THERM_DP (Use B1 GND ball for THERM_DN)	A2	THERM_DP

TEST PORT

T29_TEST_EN	E4	TEST_EN
TP_T29_TEST_POINT_0	P5	TEST_POINT_0
TP_T29_TEST_POINT_1	N6	TEST_POINT_1
TP_T29_TEST_POINT_2	M5	TEST_POINT_2
T29_TEST_POINT_3	L6	TEST_POINT_3

POWER ON RESET

PCIE_RST_0*	K1	TP_T29_PCIE_RESET0_L
PCIE_RST_1*	J2	TP_T29_PCIE_RESET1_L
PCIE_RST_2*	K3	TP_T29_PCIE_RESET2_L
PCIE_RST_3*	J4	TP_T29_PCIE_RESET3_L

Not used in host mode.

JTAG

TDI	T3	JTAG_TBT_TDI IN
TMS	R4	JTAG_TBT_TMS IN
TCK	R2	JTAG_TBT_TCK IN
TDO	T1	JTAG_TBT_TDO OUT

CLOCKS

REFCLK_100_IN_P	H17	PCIE_CLK100M_T29_P IN
REFCLK_100_IN_N	G16	PCIE_CLK100M_T29_N IN
XTAL_25_IN	P17	SYSCLK_CLK25M_T29_R — R3695 806 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_T29 IN
XTAL_25_OUT	R16	TP_T29_XTAL25OUT
TMU_CLK_OUT	U2	T29_TMU_CLK_OUT
TMU_CLK_IN	E2	T29_TMU_CLK_IN

R3690 3.3K 5% 1/16W MF-LF 402 — R3691 3.3K 5% 1/16W MF-LF 402 — C3690 1UF 10% 6.3V CERM 402 — R3692 3.3K 5% 1/16W MF-LF 402 — R3623 10K 5% 1/16W MF-LF 402 — R3622 10K 5% 1/16W MF-LF 402 — R3621 10K 5% 1/16W MF-LF 402 — R3693 3.3K 5% 1/16W MF-LF 402 — =PP3V3_T29_RTR

CRITICAL
OMIT_TABLE

U3690 M95320-RMC6XG MLP

(T29_SPI_MOSI)	D	
(T29_SPI_CLK)	C	
(T29_SPI_CS_L)	S_L	
T29ROM_WP_L	W_L	
T29ROM_HOLD_L	HOLD_L	
(T29_SPI_MISO)	Q	
VCC		
VSS, THM PAD		

R3625 0 5% 1/16W MF-LF 402 — R3629 0 5% 1/16W MF-LF 402

R3698 10K 5% 1/16W MF-LF 402 — R3696 1K 5% 1/16W MF-LF 402 — NO STUFF R3699 10K 5% 1/16W MF-LF 402

DISPLAY

SINK PORT 0

DP_T29SNK0_ML_P<3>	AA4	DPSNK0_ML_LANE_3P
DP_T29SNK0_ML_N<3>	Y3	DPSNK0_ML_LANE_3N
DP_T29SNK0_ML_P<2>	AA6	DPSNK0_ML_LANE_2P
DP_T29SNK0_ML_N<2>	Y5	DPSNK0_ML_LANE_2N
DP_T29SNK0_ML_P<1>	AA8	DPSNK0_ML_LANE_1P
DP_T29SNK0_ML_N<1>	Y7	DPSNK0_ML_LANE_1N
DP_T29SNK0_ML_P<0>	AA10	DPSNK0_ML_LANE_0P
DP_T29SNK0_ML_N<0>	Y9	DPSNK0_ML_LANE_0N
DP_T29SNK0_AUXCH_P	V1	DPSNK0_AUX_CHP
DP_T29SNK0_AUXCH_N	W2	DPSNK0_AUX_CHN
DP_T29SNK0_HPD	V5	DPSNK0_HOT_PLUG_DET

R3630 100K 5% 1/16W MF-LF 402

SINK PORT 1

DP_T29SNK1_ML_P<3>	V9	DPSNK1_ML_LANE_3P
DP_T29SNK1_ML_N<3>	U8	DPSNK1_ML_LANE_3N
DP_T29SNK1_ML_P<2>	V11	DPSNK1_ML_LANE_2P
DP_T29SNK1_ML_N<2>	U10	DPSNK1_ML_LANE_2N
DP_T29SNK1_ML_P<1>	V13	DPSNK1_ML_LANE_1P
DP_T29SNK1_ML_N<1>	U12	DPSNK1_ML_LANE_1N
DP_T29SNK1_ML_P<0>	V15	DPSNK1_ML_LANE_0P
DP_T29SNK1_ML_N<0>	U14	DPSNK1_ML_LANE_0N
DP_T29SNK1_AUXCH_P	V7	DPSNK1_AUX_CHP
DP_T29SNK1_AUXCH_N	U6	DPSNK1_AUX_CHN
DP_T29SNK1_HPD	U4	DPSNK1_HOT_PLUG_DET

R3631 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

DPSRC0_ML_LANE_3P	AA18	TP_DP_T29SRC_ML_CP<3>
DPSRC0_ML_LANE_3N	Y17	TP_DP_T29SRC_ML_CN<3>
DPSRC0_ML_LANE_2P	AA16	TP_DP_T29SRC_ML_CP<2>
DPSRC0_ML_LANE_2N	Y15	TP_DP_T29SRC_ML_CN<2>
DPSRC0_ML_LANE_1P	AA14	TP_DP_T29SRC_ML_CP<1>
DPSRC0_ML_LANE_1N	Y13	TP_DP_T29SRC_ML_CN<1>
DPSRC0_ML_LANE_0P	AA12	TP_DP_T29SRC_ML_CP<0>
DPSRC0_ML_LANE_0N	Y11	TP_DP_T29SRC_ML_CN<0>
DPSRC0_AUX_CHP	W16	TP_DP_T29SRC_AUXCH_CP
DPSRC0_AUX_CHN	U16	TP_DP_T29SRC_AUXCH_CN
DPSRC0_HOT_PLUG_DET	V3	DP_T29SRC_HPD

DP_ATEST	Y19	T29_DP_ATEST
DP_RES_0	Y21	
DP_RES_1	AA20	T29_DP_RES

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm

C3685 100PF 5% 50V CERM 0402 — C3686 0.01UF 10% 16V X7R-CERM 0402

R3685 14.0K 1% 1/16W MF-LF 402 — R3632 100K 5% 1/16W MF-LF 402

PORTS

PORT0

T29_R2D_C_P<0>	A6	PRT0_T29T_P
T29_R2D_C_N<0>	A4	PRT0_T29T_N
T29_D2R_P<0>	C4	PRT0_T29R_P
T29_D2R_N<0>	C2	PRT0_T29R_N
T29_LSEO<0>	J6	T29_0_LSEO
T29_LSOE<0>	K5	T29_0_LSOE

PORT1

T29_R2D_C_P<1>	A10	PRT1_T29T_P
T29_R2D_C_N<1>	A8	PRT1_T29T_N
T29_D2R_P<1>	C8	PRT1_T29R_P
T29_D2R_N<1>	C6	PRT1_T29R_N
T29_LSEO<1>	G6	T29_1_LSEO
T29_LSOE<1>	H5	T29_1_LSOE

I2C_T29_SDA	F3	T29_SDA
I2C_T29_SCL	F5	T29_SCL

PORT2

PRT2_T29T_P	A14	T29_R2D_C_P<2>
PRT2_T29T_N	A12	T29_R2D_C_N<2>
PRT2_T29R_P	C12	T29_D2R_P<2>
PRT2_T29R_N	C10	T29_D2R_N<2>
T29_2_LSEO	G4	T29_LSEO<2>
T29_2_LSOE	H3	T29_LSOE<2>

PORT3

PRT3_T29T_P	A18	T29_R2D_C_P<3>
PRT3_T29T_N	A16	T29_R2D_C_N<3>
PRT3_T29R_P	C16	T29_D2R_P<3>
PRT3_T29R_N	C14	T29_D2R_N<3>
T29_3_LSEO	G2	T29_LSEO<3>
T29_3_LSOE	H1	T29_LSOE<3>

NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).

SNK0 AC Coupling

DP_T29SNK0_ML_C_P<0>	C3620 0.1UF	DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_C_N<0>	C3621 0.1UF	DP_T29SNK0_ML_N<0>
DP_T29SNK0_ML_C_P<1>	C3622 0.1UF	DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_C_N<1>	C3623 0.1UF	DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_C_P<2>	C3624 0.1UF	DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_C_N<2>	C3625 0.1UF	DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_C_P<3>	C3626 0.1UF	DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_C_N<3>	C3627 0.1UF	DP_T29SNK0_ML_N<3>
DP_T29SNK0_AUXCH_C_P	C3628 0.1UF	DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_C_N	C3629 0.1UF	DP_T29SNK0_AUXCH_N

SNK1 AC Coupling

DP_T29SNK1_ML_C_P<0>	C3630 0.1UF	DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_C_N<0>	C3631 0.1UF	DP_T29SNK1_ML_N<0>
DP_T29SNK1_ML_C_P<1>	C3632 0.1UF	DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_C_N<1>	C3633 0.1UF	DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_C_P<2>	C3634 0.1UF	DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_C_N<2>	C3635 0.1UF	DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_C_P<3>	C3636 0.1UF	DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_C_N<3>	C3637 0.1UF	DP_T29SNK1_ML_N<3>
DP_T29SNK1_AUXCH_C_P	C3638 0.1UF	DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_C_N	C3639 0.1UF	DP_T29SNK1_AUXCH_N

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: T29 Host (1 of 2)

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DRAWING NUMBER: 051-9058 SIZE: D
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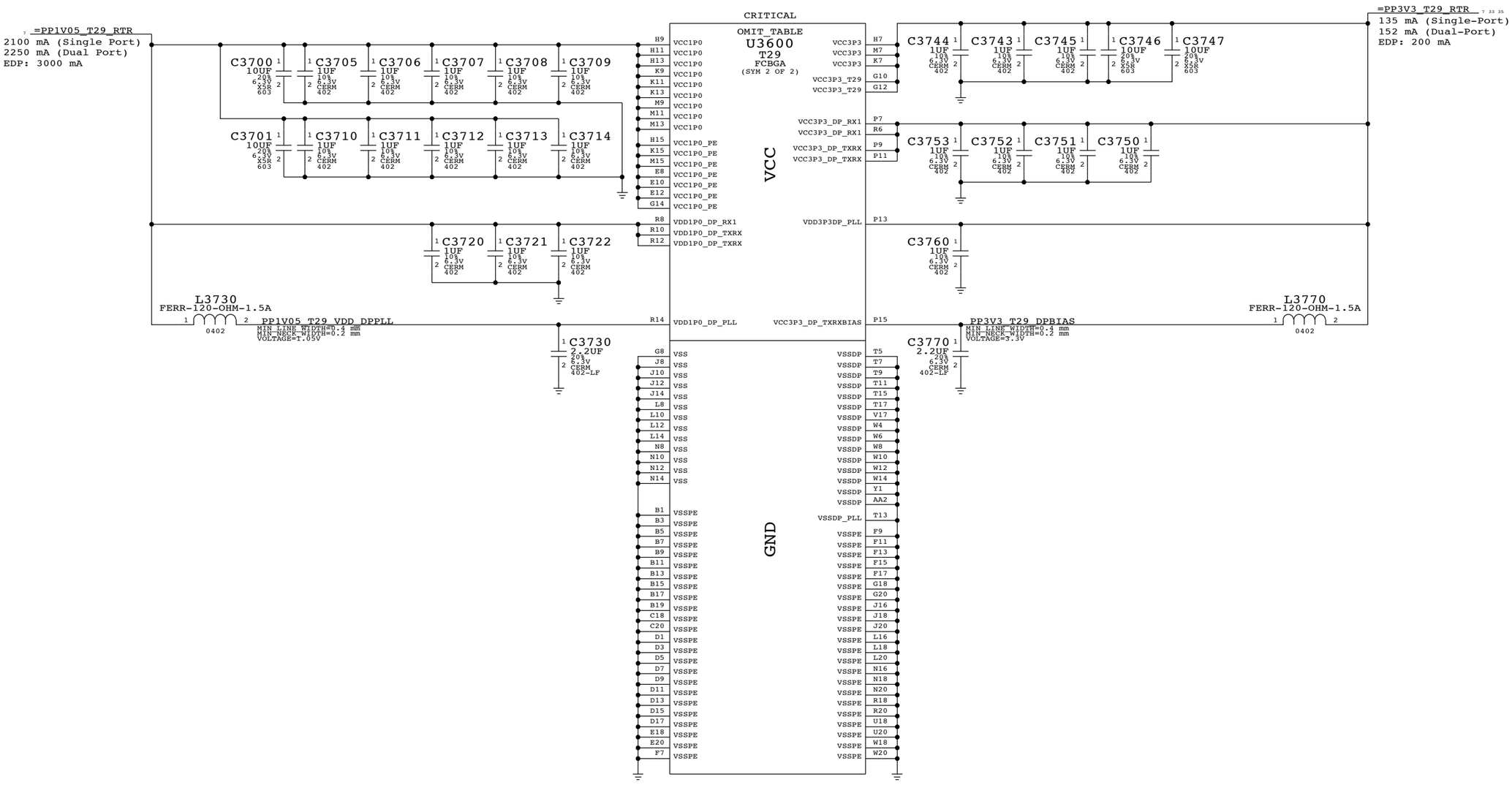

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=K90I MLB SYNC DATE=02/15/2011

PAGE TITLE: T29 Host (2 of 2)

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

T29 15V Boost Regulator

=PPVIN_SW_T29BST
8-13V Input
Changes required for 2S.

CRITICAL T29BST:Y Q3880 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

Voltage not specified here, add property on another page.

T29BST:Y R3880 470K 5% 1/16W MF-LF 402
T29BST:Y C3880 0.1UF 10% 25V X5R 402
T29BST_PWREN_DIV_L
T29BST:Y R3881 330K 5% 1/16W MF-LF 402
T29BST_PWREN_L
Q3805 SSM3K15AMFVAPE VESM
TBT_A_HV_EN

T29BST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>
T29BST:Y C3890 10UF 10% 25V X5R 805
T29BST:Y C3891 10UF 10% 25V X5R 805

CRITICAL T29BST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS

T29BST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL T29BST:Y U3890 LT3957 QFN

T29BST_EN_UVLO
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
GND_T29BST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

T29BST:Y C3892 4.7UF 10% 10V X5R 805
T29BST:Y C3887 47PF 5% 50V CERM 402
T29BST:Y R3893 10K 1% 1/16W MF-LF 402
T29BST_VC_RC
T29BST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
T29BST:Y C3893 0.0033UF 10% 50V X7R-CERM 0402
T29BST:Y R3894 41.2K 1% 1/16W MF-LF 402
T29BST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

T29BST_SNS1
T29BST_SNS2
T29BST_VSNS
T29BST_VSNS_RC
T29BST_FBX
SGND
GND

T29BST:Y R3889 0 5% 1/16W MF-LF 402
CRITICAL T29BST:Y D3895 POWERDI-123 DFLS230L
PLACE_NEAR=C3897.1:2 mm
XW3895 SM
T29BST:Y R3890 49.9K 1% 1/16W MF-LF 402
T29BST:Y R3895 137K 1% 1/16W MF-LF 402 <Ra>
T29BST:Y C3888 22PF 5% 50V CERM 0402
NO STUFF T29BST:Y C3889 100PF 5% 50V CERM 0402
T29BST:Y R3896 15.8K 1% 1/16W MF-LF 402 <Rb>

=PP15V_T29_REG
Vout = 18.3V
Max Current = 0.8A
Freq = 300KHz

T29BST:Y C3895 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3896 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3897 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3898 4.7UF 10% 50V X7R-CERM 1206
T29BST:Y C3899 0.001UF 10% 50V X7R-CERM 0402

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

T29BST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
T29BST:Y R3888 330K 5% 1/20W MF 201
T29BST_SHDN_DIV
T29BST:Y R3887 330K 5% 1/20W MF 201
T29BST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation

=PP3V3_S0_T29PWRCTL
C3800 0.1UF 10% 25V X5R 402
CRITICAL U3800 SLG4AP016V TDFN
=PP3V3_T29_RTR
R3807 100K 5% 1/16W MF-LF 402
PP1V05_T29

Platform (PCIe) Reset
=T29_RESET_L
R3803 10K 5% 1/16W MF-LF 402
Open-Drain GPIO
TBT_SW_RESET_L
TBT_PWR_EN
TBT_CLKREQ_L
Pull-up provided by SB page.

SENSE 0.7V
DLY
RESET*
T29_RESET_L
DLY = 60 ms +/- 20%
=T29_CLKREQ_L
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V T29 Switch

=PP3V3_S0_P3V3T29FET
U3810 TPS22924 CSP
=PP3V3_T29_FET
Max Current = 2A (85C)
C3810 1UF 10% 6.3V CERM 402
CRITICAL
R3816 0 5% 1/16W MF-LF 402
TBT_PWR_EN_RC

U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

1.05V T29 Switch

=PP1V05_S0_P1V05T29FET
U3815 TPS22920 CSP
=PP1V05_T29_FET
Max Current = 4A (85C)
C3815 1UF 10% 6.3V CERM 402
CRITICAL
NO STUFF C3816 1UF 10% 6.3V CERM 402

U3815	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: T29 Power Support

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D
REVISION: 6.0.0
BRANCH:
PAGE: 38 OF 109
SHEET: 35 OF 86

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

71 36 24 7 =PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
36 =PP3V3R1V8_ENET_LR_OUT

CRITICAL L3900 FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3900 0.1UF 10% 16V X7R-CERM 0402

CRITICAL L3905 FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3905 0.1UF 10% 16V X7R-CERM 0402

CRITICAL L3910 FERR-600-OHM-0.5A
PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 0402
C3911 0.1UF 10% 16V X7R-CERM 0402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 0402

7 =PP3V3_S0_ENETPHY
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

ENET_SR_LX 71
ENET_SR_VFB 71

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 71
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 16V X7R-CERM 0402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 16V X7R-CERM 0402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A
PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3931 0.1UF 10% 16V X7R-CERM 0402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 0402
CRITICAL C3935 10UF 10% 6.3V X5R 805

AVDDH 42,48 | BIASVDDH 37 | XTALVDDH 17 | VDDO 7,20,56,62 | SR_VDD 14 | SR_VDDP 15 | SR_LX 16 | SR_VFB 13 | AVDDL 39,45,51 | PCIE_PLLVDDL 29,32 | GPHY_PLLVDDL 36 | VDDC 35,61

U3900
BCM57765B0
QFN-8X8

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT 36
PP3V3R1V8_ENET_LR_OUT_REG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.8V
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 0402
C3972 0.1UF 10% 16V X7R-CERM 0402

81 16 OUT PCIE_ENET_D2R_N → C3950 0.1UF → ENET_VMAIN_PRSNT → 58 VMAIN_PRSNT (IPD)
81 16 OUT PCIE_ENET_D2R_P → C3951 0.1UF → 81 PCIE_ENET_D2R_C_N → 27 PCIE_TXD_N
81 PCIE_ENET_D2R_C_P → 28 PCIE_TXD_P
81 16 IN PCIE_ENET_R2D_C_P → C3955 0.1UF → 81 PCIE_ENET_R2D_P → 33 PCIE_RXD_P
81 PCIE_ENET_R2D_N → 34 PCIE_RXD_N
81 16 IN PCIE_ENET_R2D_C_N → C3956 0.1UF → 81 16 IN PCIE_CLK100M_ENET_P → 31 PCIE_REFCLK_P
81 16 IN PCIE_CLK100M_ENET_N → 30 PCIE_REFCLK_N
82 30 IN ENET_RESET_L → 11 PERST* (IPD)
16 OUT ENET_CLKREQ_L → 12 CLKREQ* (OD)
24 OUT =ENET_WAKE_L (See note) → R3943 0 5% 1/16W MF-LF 402 → ENET_WAKE_R_L → 3 WAKE* (OD)
30 24 IN ENET_LOW_PWR → 4 LOW_PWR (IPD)
BCM57765_SMB_CLK → 6 SMB_CLK
BCM57765_SMB_DATA → 10 SMB_DATA (IPD)
36 BCM57765_SCLK → 66 SCLK_SPD1000LED*
36 BCM57765_MISO → 64 SI/EEDATA
36 BCM57765_MOSI → 65 SO_LINKLED*
36 BCM57765_CS_L → 63 CS*/EECLK
(IPD)
TP_BCM57765_SPD100LED_L → 2 SPD100LED*/SERIAL_DO (OD)
TP_BCM57765_TRAFFICLED_L → 67 TRAFFICLED*/SERIAL_DI (OD)
81 24 IN SYSCLK_CLK25M_ENET → 18 XTALI
NC → 19 XTALO
BCM57765_RDAC → 38 RDAC
THRM_PAD 69

NOTE: "IPx" == Programmable pull-up/down

(IPD) GPIO_0/CR_ACT_LED* 5 NC
GPIO_1/LR_OUT 8
GPIO_2/MEDIA_SENSE 9 → ENET_MEDIA_SENSE → OUT 24
(IPx) SD_DETECT* 1 → SDCONN_DETECT_L → IN 30
(IPU) CR_CMD 26 → SDCONN_CMD → IN 30 82
CR_CLK 21 → SDCONN_CLK → OUT 30 82
(IPU) CR_DATA0 25 → SDCONN_DATA<0> → BI 30 82
CR_DATA1 24 → SDCONN_DATA<1> → BI 30 82
CR_DATA2 23 → SDCONN_DATA<2> → BI 30 82
CR_DATA3 22 → SDCONN_DATA<3> → BI 30 82
CR_DATA4 52 → SDCONN_DATA<4> → BI 30 82
CR_DATA5 53 → SDCONN_DATA<5> → BI 30 82
CR_DATA6 54 → SDCONN_DATA<6> → BI 30 82
CR_DATA7 55 → SDCONN_DATA<7> → BI 30 82
(IPD) MS_INS* 59 → TP_CE_L_MS_INS_L
CR_LED*/CR_BUS_PWR 60 → ENET_CR_PWREN → OUT 30
CR_WP* 57 → SDCONN_WP → IN 30
SR_DISABLE 68 → BDM57765_SR_DISABLE → R3980 1K 5% 1/16W MF-LF 402

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

R3965 1.24K 1% 1/16W MF-LF 402

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

71 36 24 7 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X7R-CERM 0402
U3990 AT45DB011D SOIC-8S1
VCC 8
SCK 2 ← 36 BCM57765_SCLK
SI 1 ← BCM57765_MOSI 36
SO 8 → BCM57765_MISO 36
CS* 4 ← 36 BCM57765_CS_L
WP* 5 OMIT
RESET* 3
GND 7
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=J31 MLB | SYNC DATE=06/15/2011
PAGE TITLE
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-9058 | SIZE D
REVISION 6.0.0
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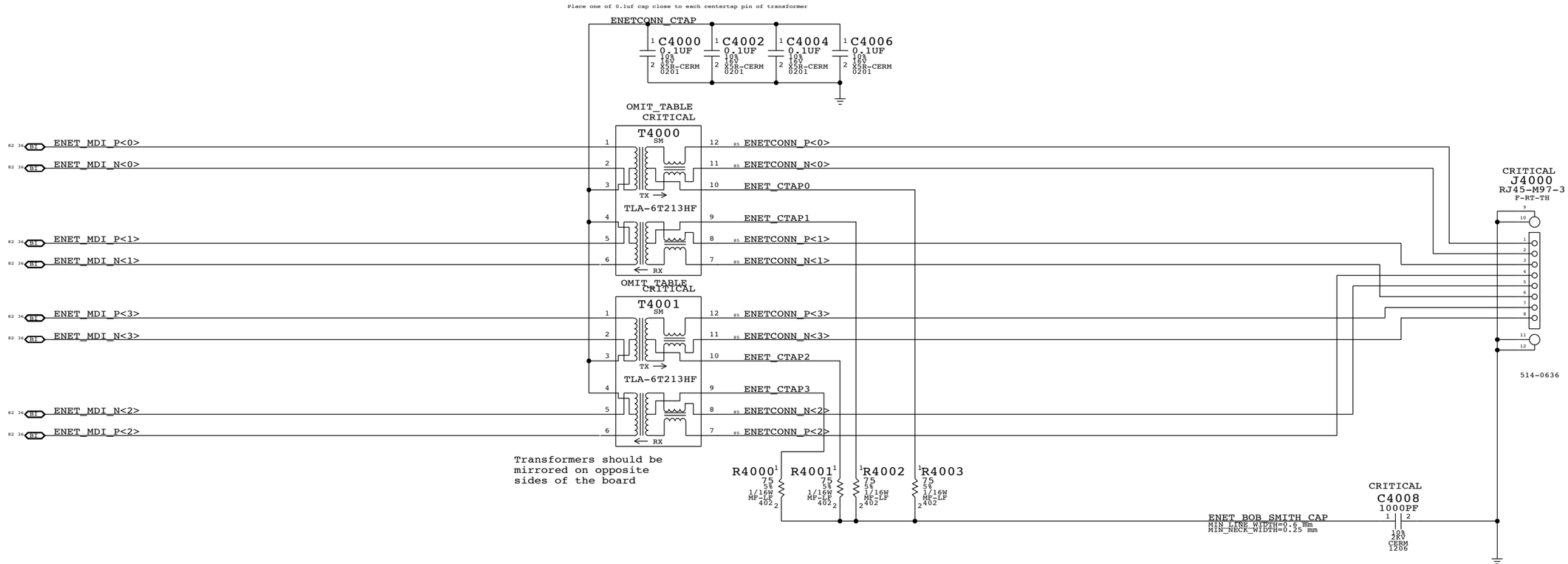
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
157S0084	2	XFMR,ISO,HALF-PORT,1000T,12P,SMD,HF	T4000,T4001	CRITICAL	

SYNC MASTER=K90I MLB — SYNC DATE=02/15/2011

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-9058 — SIZE: D
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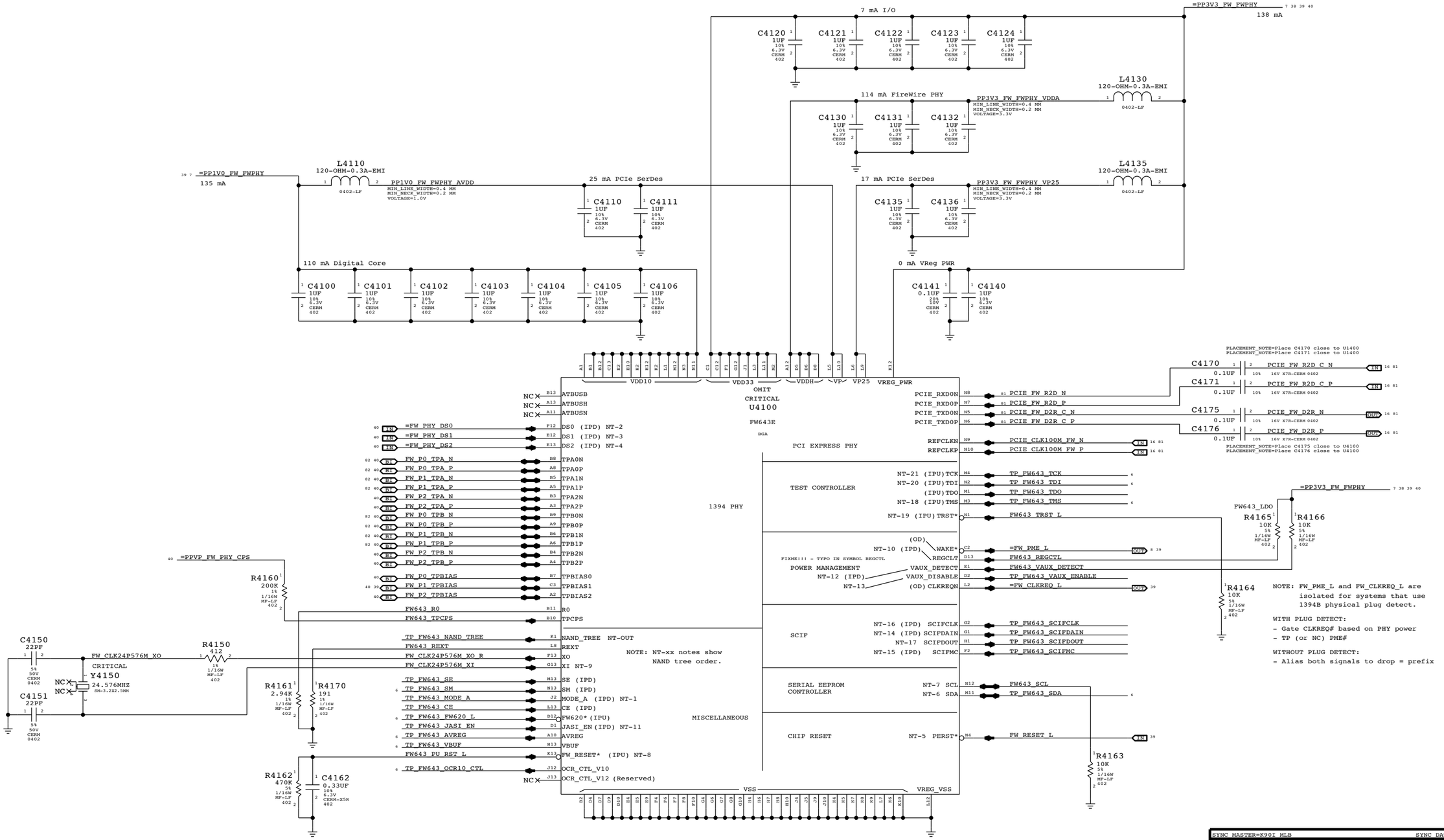

SYNC MASTER=K90I MLB
SYNC DATE=02/15/2013

PAGE TITLE

FireWire LLC/PHY (FW643E)

Apple Inc.

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SIZE D
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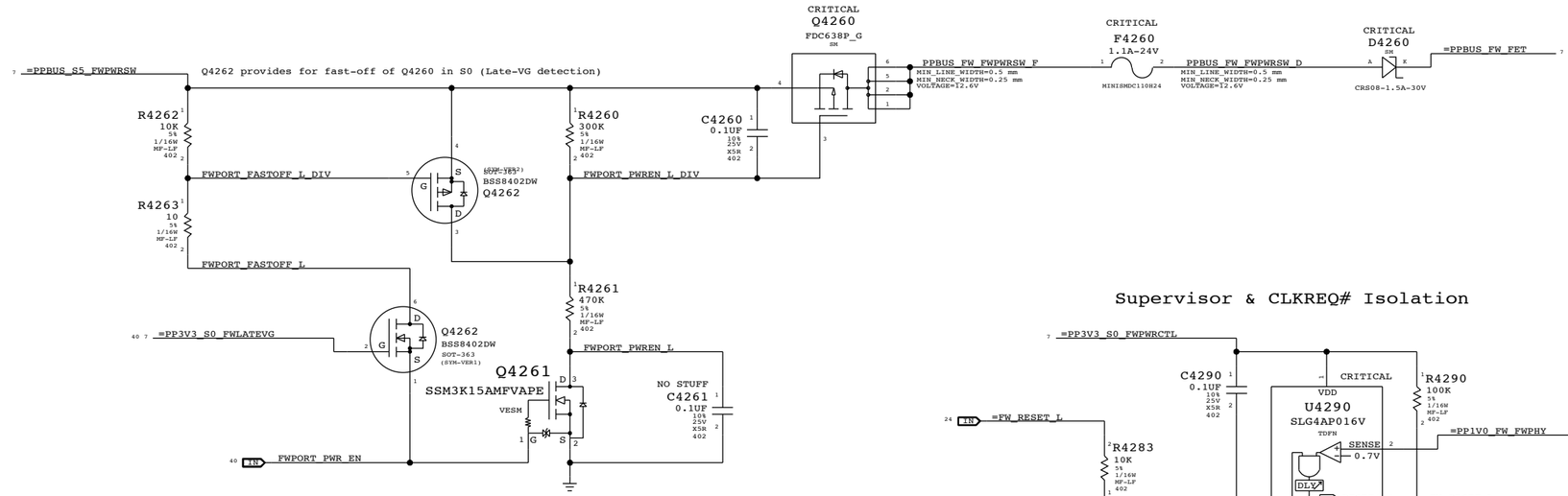
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

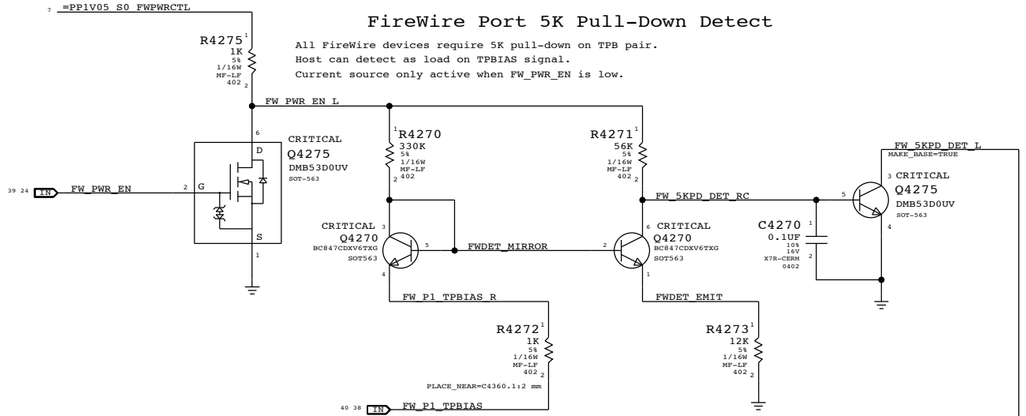
BOM options provided by this page:
(NONE)

FireWire Port Power Switch



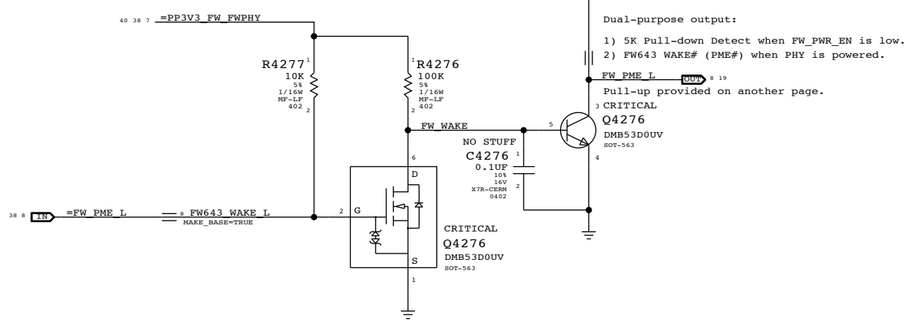
Supervisor & CLKREQ# Isolation

FireWire Port 5K Pull-Down Detect

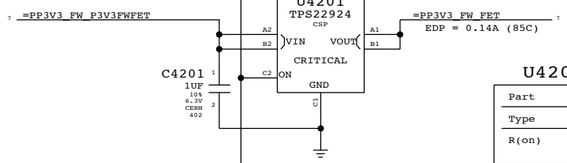


FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



3.3V FW Switch

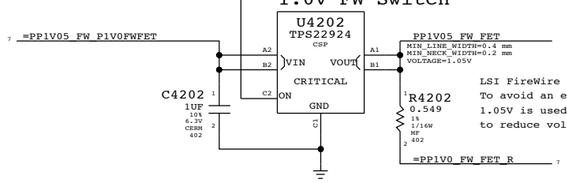


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=K90I_MLB SYNC DATE=06/23/2011

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
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Page Notes

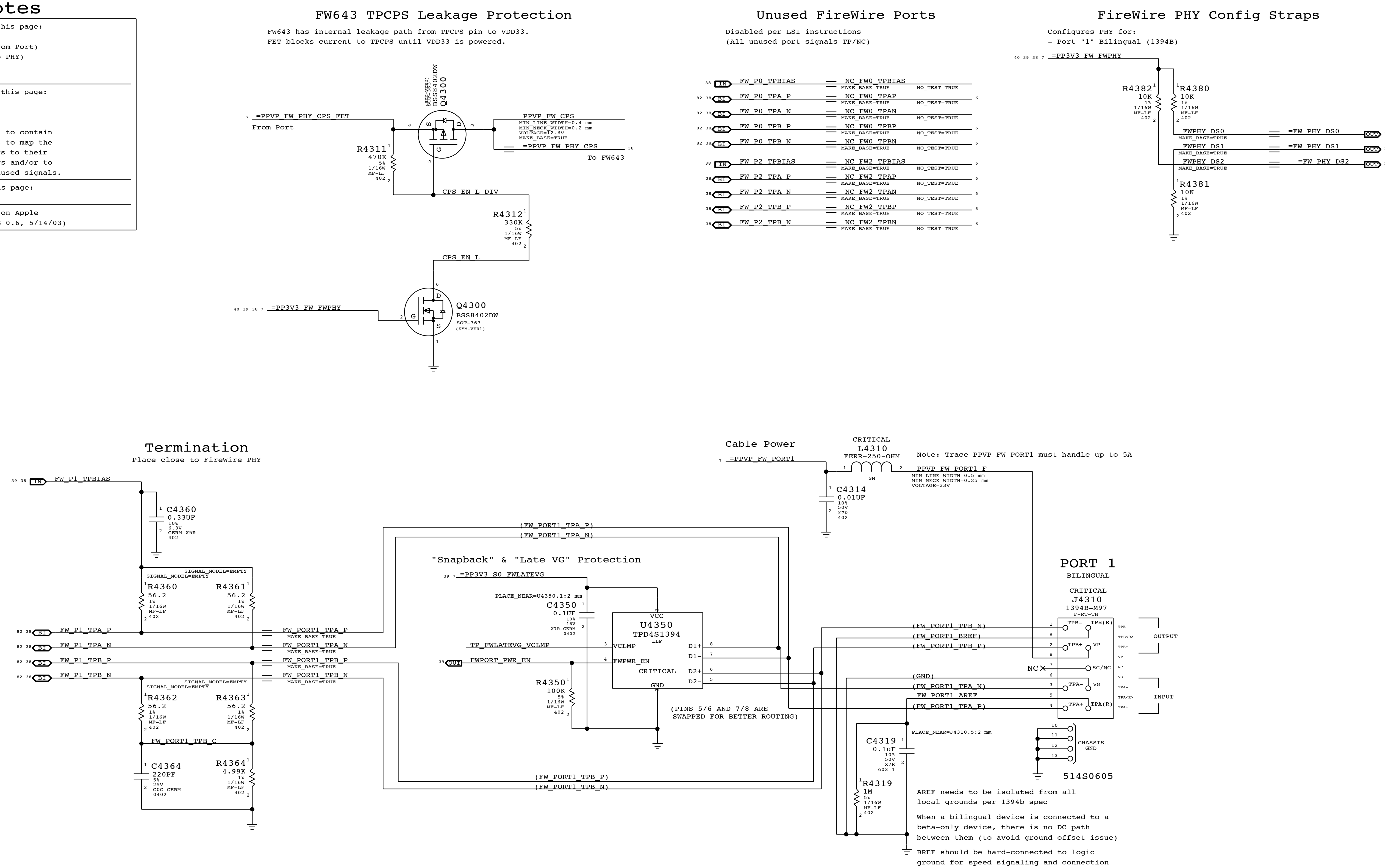
Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



FW643 TPCPS Leakage Protection
FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.
=PPVP_FW_PHY_CPS_FET
From Port
PPVP_FW_CPS
=PPVP_FW_PHY_CPS
To FW643
Q4300
BSS8402DW
R4311
470K
CPS_EN_L_DIV
R4312
330K
CPS_EN_L
=PP3V3_FW_FWPHY
Q4300
BSS8402DW
SOT-363
Unused FireWire Ports
Disabled per LSI instructions
(All unused port signals TP/NC)
FW_P0_TPBIAS
NC_FW0_TPBIAS
FW_P0_TPA_P
NC_FW0_TPAP
FW_P0_TPA_N
NC_FW0_TPAN
FW_P0_TPB_P
NC_FW0_TPBP
FW_P0_TPB_N
NC_FW0_TPBN
FW_P2_TPBIAS
NC_FW2_TPBIAS
FW_P2_TPA_P
NC_FW2_TPAP
FW_P2_TPA_N
NC_FW2_TPAN
FW_P2_TPB_P
NC_FW2_TPBP
FW_P2_TPB_N
NC_FW2_TPBN
FireWire PHY Config Straps
Configures PHY for:
- Port "1" Bilingual (1394B)
=PP3V3_FW_FWPHY
R4382
10K
R4380
10K
FWPHY_DS0
=FW_PHY_DS0
FWPHY_DS1
=FW_PHY_DS1
FWPHY_DS2
=FW_PHY_DS2
R4381
10K
Termination
Place close to FireWire PHY
FW_P1_TPBIAS
C4360
0.33UF
R4360
56.2
R4361
56.2
FW_P1_TPA_P
FW_P1_TPA_N
FW_P1_TPB_P
FW_P1_TPB_N
FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N
R4362
56.2
R4363
56.2
FW_PORT1_TPB_C
C4364
220PF
R4364
4.99K
"Snapback" & "Late VG" Protection
=PP3V3_S0_FWLATEVG
PLACE_NEAR=U4350.1:2 mm
C4350
0.1UF
U4350
TPD4S1394
TP_FWLATEVG_VCLMP
FWPORT_PWR_EN
R4350
100K
(PINS 5/6 AND 7/8 ARE SWAPPED FOR BETTER ROUTING)
Cable Power
=PPVP_FW_PORT1
CRITICAL
L4310
FERR-250-OHM
Note: Trace PPVP_FW_PORT1 must handle up to 5A
PPVP_FW_PORT1_F
C4314
0.01UF
PORT 1
BILINGUAL
CRITICAL
J4310
1394B-M97
F-RT-TH
(FW_PORT1_TPB_N)
(FW_PORT1_BREF)
(FW_PORT1_TPB_P)
(GND)
(FW_PORT1_TPA_N)
FW_PORT1_AREF
(FW_PORT1_TPA_P)
OUTPUT
INPUT
CHASSIS GND
514S0605
C4319
0.1uF
PLACE_NEAR=J4310.5:2 mm
R4319
1M
AREF needs to be isolated from all local grounds per 1394b spec
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)
BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: FireWire Connector

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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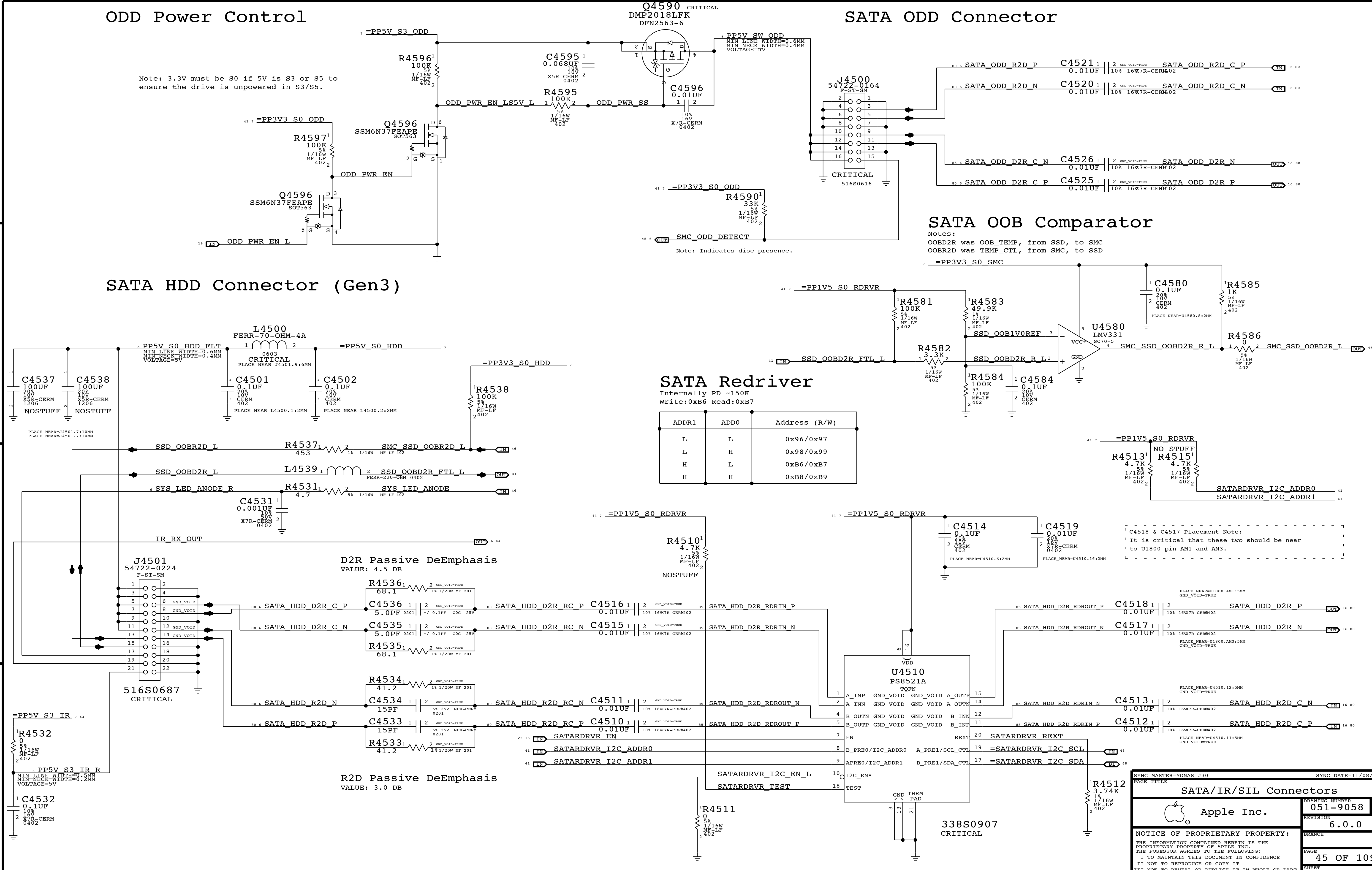

ODD Power Control
Note: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.
=PP5V_S3_ODD
R4596 100K 5% 1/16W MF-LF 402
C4595 0.068UF 10% 10V X5R-CERM 0402
Q4590 CRITICAL DMP2018LFK DFN2563-6
PP5V_SW_ODD MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.4MM VOLTAGE=5V
R4595 100K 5% 1/16W MF-LF 402
ODD_PWR_EN_LS5V_L
ODD_PWR_SS
C4596 0.01UF 10% 16V X7R-CERM 0402
=PP3V3_S0_ODD
Q4596 SSM6N37FEAPE SOT563
R4597 100K 5% 1/16W MF-LF 402
ODD_PWR_EN
ODD_PWR_EN_L
SATA ODD Connector
J4500 54722-0164 F-ST-SM CRITICAL 516S0616
SATA_ODD_R2D_P
SATA_ODD_R2D_N
SATA_ODD_D2R_C_N
SATA_ODD_D2R_C_P
C4521 0.01UF 10% 16V X7R-CERM 0402
C4520 0.01UF 10% 16V X7R-CERM 0402
C4526 0.01UF 10% 16V X7R-CERM 0402
C4525 0.01UF 10% 16V X7R-CERM 0402
SATA_ODD_R2D_C_P
SATA_ODD_R2D_C_N
SATA_ODD_D2R_N
SATA_ODD_D2R_P
=PP3V3_S0_ODD
R4590 33K 5% 1/16W MF-LF 402
SMC_ODD_DETECT
Note: Indicates disc presence.
SATA OOB Comparator
Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD
=PP3V3_S0_SMC
=PP1V5_S0_RDRVR
R4581 100K 5% 1/16W MF-LF 402
R4583 49.9K 1% 1/16W MF-LF 402
C4580 0.1UF 20% 10V CERM 402
R4585 1K 5% 1/16W MF-LF 402
U4580 LMV331 SC70-5
SSD_OOB1V0REF
R4582 3.3K 5% 1/16W MF-LF 402
SSD_OOBD2R_FTL_L
SSD_OOBD2R_R_L
SMC_SSD_OOBD2R_R_L
R4586 0 5% 1/16W MF-LF 402
SMC_SSD_OOBD2R_L
R4584 100K 5% 1/16W MF-LF 402
C4584 0.1UF 20% 10V CERM 402
SATA HDD Connector (Gen3)
L4500 FERR-70-OHM-4A 0603 CRITICAL
PP5V_S0_HDD_FLT MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.4MM VOLTAGE=5V
=PP5V_S0_HDD
C4537 100UF 20% 10V X5R-CERM 1206 NOSTUFF
C4538 100UF 20% 10V X5R-CERM 1206 NOSTUFF
C4501 0.1UF 20% 10V CERM 402
C4502 0.1UF 20% 10V CERM 402
=PP3V3_S0_HDD
R4538 100K 5% 1/16W MF-LF 402
SSD_OOBR2D_L
R4537 453 1% 1/16W MF-LF 402
SMC_SSD_OOBR2D_L
SSD_OOBD2R_L
L4539 FERR-220-OHM 0402
SSD_OOBD2R_FTL_L
SYS_LED_ANODE_R
R4531 4.7 5% 1/16W MF-LF 402
SYS_LED_ANODE
C4531 0.001UF 10% 50V X7R-CERM 0402
IR_RX_OUT
J4501 54722-0224 F-ST-SM 516S0687 CRITICAL
D2R Passive DeEmphasis VALUE: 4.5 DB
R4536 68.1
C4536 5.0PF
C4535 5.0PF
R4535 68.1
SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N
SATA_HDD_D2R_RC_P
SATA_HDD_D2R_RC_N
C4516 0.01UF
C4515 0.01UF
SATA_HDD_D2R_RDRIN_P
SATA_HDD_D2R_RDRIN_N
R4534 41.2
C4534 15PF
C4533 15PF
R4533 41.2
SATA_HDD_R2D_N
SATA_HDD_R2D_P
SATA_HDD_R2D_RC_N
SATA_HDD_R2D_RC_P
C4511 0.01UF
C4510 0.01UF
SATA_HDD_R2D_RDROUT_N
SATA_HDD_R2D_RDROUT_P
R2D Passive DeEmphasis VALUE: 3.0 DB
=PP5V_S3_IR
R4532 0 5% 1/16W MF-LF 402
PP5V_S3_IR_R MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
C4532 0.1UF 10% 16V X7R-CERM 0402
SATA Redriver
Internally PD ~150K
Write:0xB6 Read:0xB7
=PP1V5_S0_RDRVR
R4510 4.7K 5% 1/16W MF-LF 402 NOSTUFF
C4514 0.1UF 20% 10V CERM 402
C4519 0.01UF 20% 16V X7R-CERM 0402
C4518 & C4517 Placement Note:
It is critical that these two should be near to U1800 pin AM1 and AM3.
R4513 4.7K 5% 1/16W MF-LF 402
NO STUFF R4515 4.7K 5% 1/16W MF-LF 402
SATARDRVR_I2C_ADDR0
SATARDRVR_I2C_ADDR1
U4510 PS8521A TQFN 338S0907 CRITICAL
SATA_HDD_D2R_RDROUT_P
SATA_HDD_D2R_RDROUT_N
C4518 0.01UF
C4517 0.01UF
SATA_HDD_D2R_P
SATA_HDD_D2R_N
SATA_HDD_R2D_RDRIN_N
SATA_HDD_R2D_RDRIN_P
C4513 0.01UF
C4512 0.01UF
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATARDRVR_EN
SATARDRVR_REXT
=SATARDRVR_I2C_SCL
=SATARDRVR_I2C_SDA
SATARDRVR_I2C_EN_L
SATARDRVR_TEST
R4511 0 5% 1/16W MF-LF 402
R4512 3.74K 1% 1/16W MF-LF 402

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SYNC_MASTER=YONAS_J30 SYNC_DATE=11/08/2011

PAGE TITLE: SATA/IR/SIL Connectors

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

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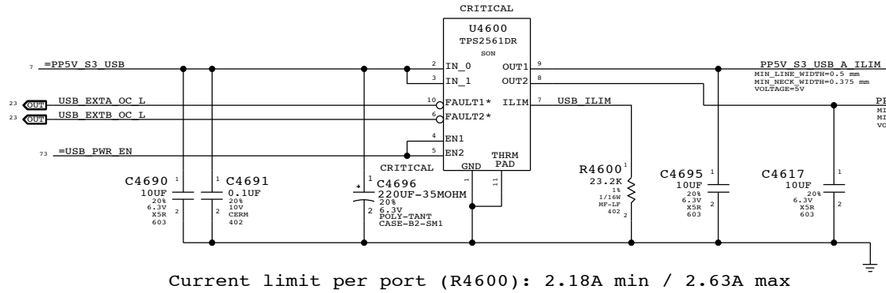
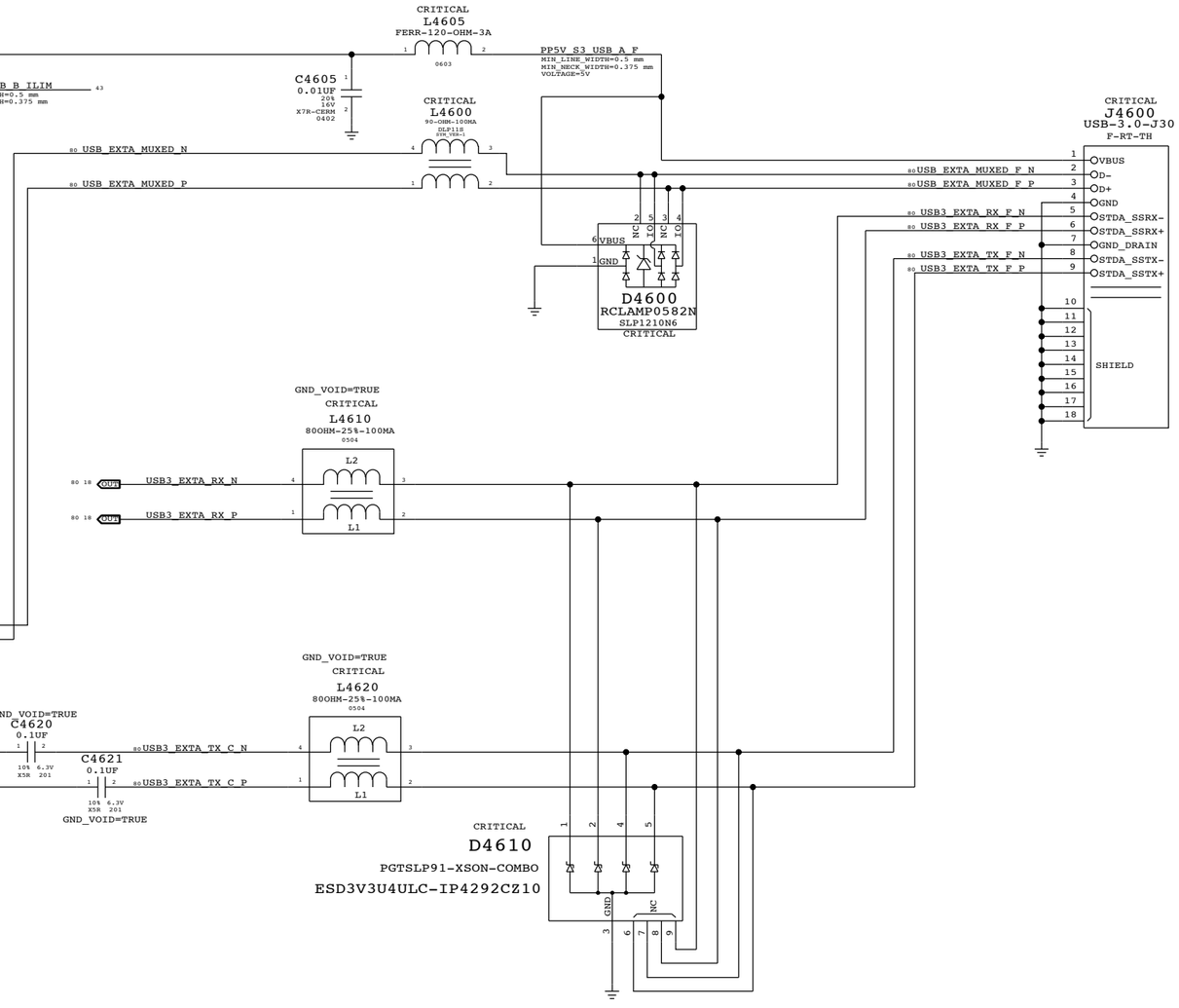
USB Port Power Switch



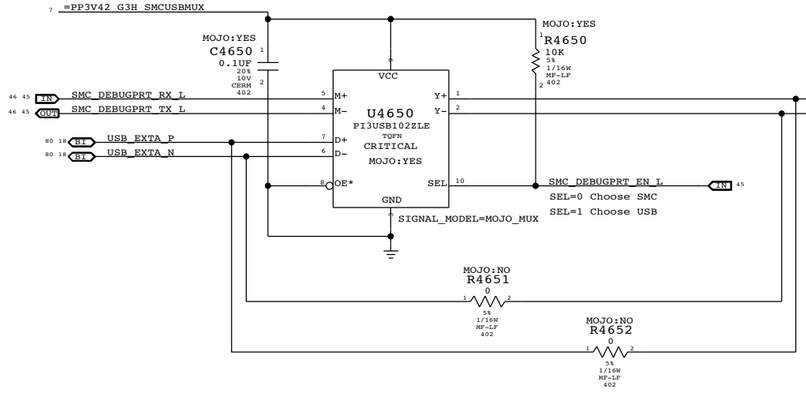
Current limit per port (R4600): 2.18A min / 2.63A max

www.qdzbwx.com

USB Port A (Front Port)



Mojo SMC Debug Mux



SYNC MASTER=J31 MLB	SYNC DATE=07/08/2011
PAGE TITLE	External A USB3 Connector
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
	REVISION 6.0.0
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	PAGE 46 OF 109
	SHEET 42 OF 86

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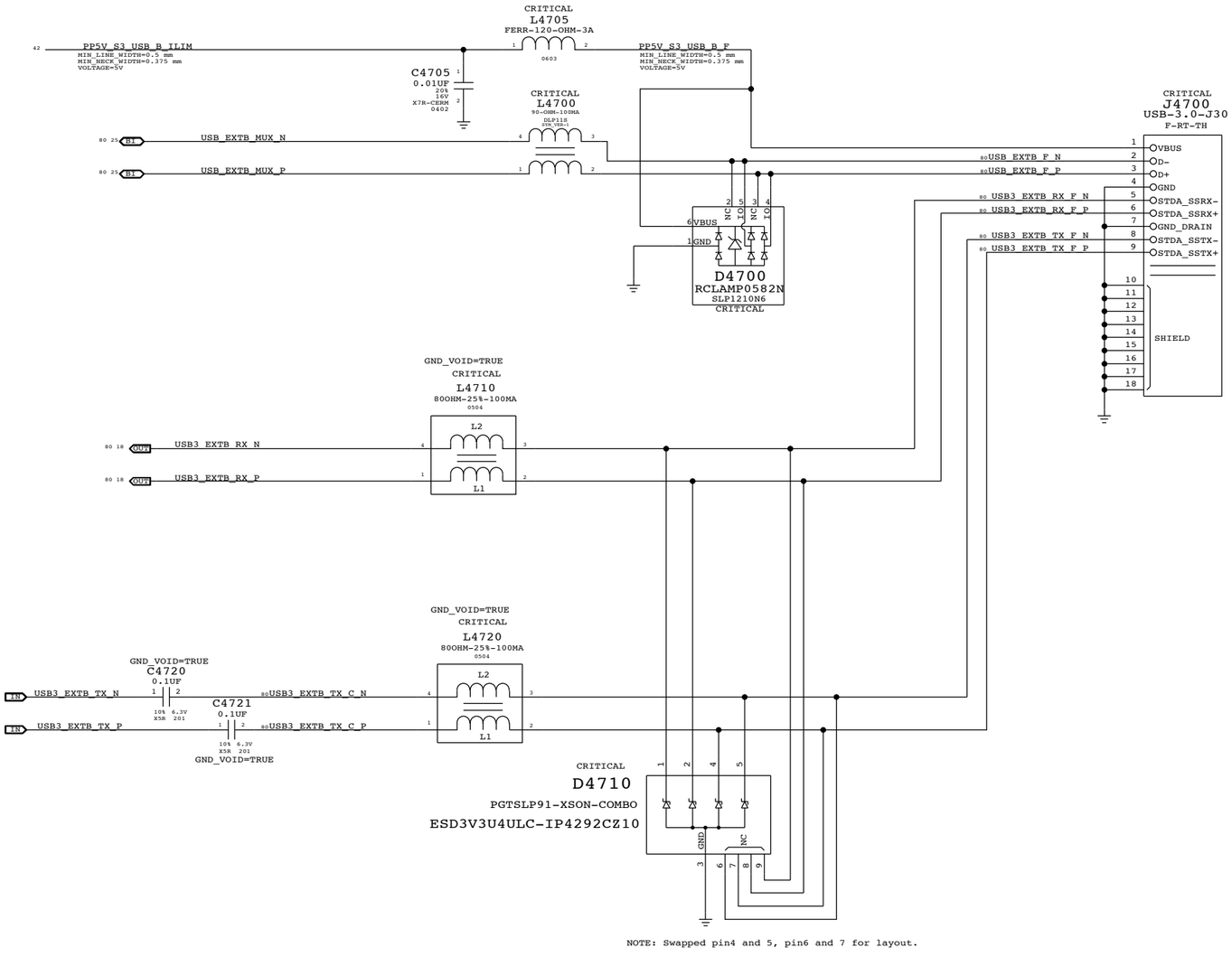
USB Port B (Back Port)



NOTE: Swapped pin4 and 5, pin6 and 7 for layout.

SYNC MASTER=J31 MLB | SYNC DATE=07/08/2011

PAGE TITLE

External B USB3 Connector

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DRAWING NUMBER 051-9058 | SIZE D

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SHEET 43 OF 86

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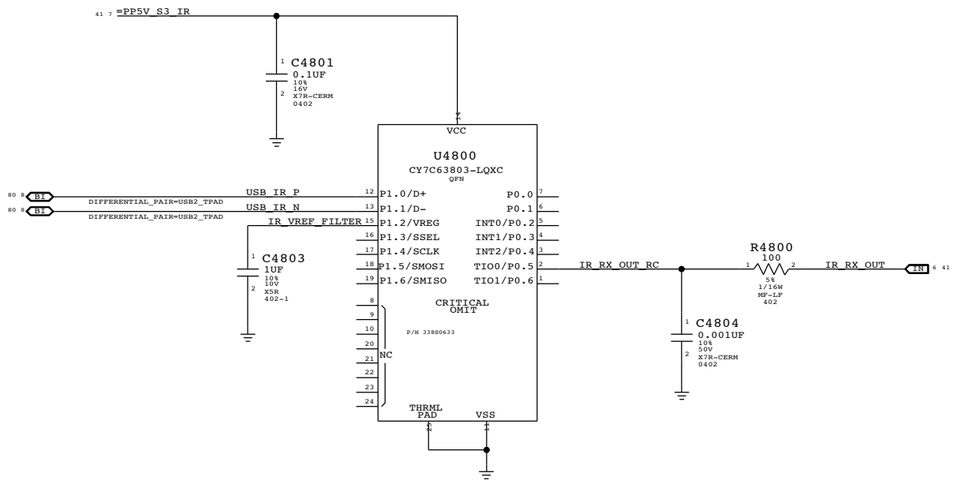
IR SUPPORT



SYNC MASTER=K90I MLB SYNC DATE=02/15/2011

PAGE TITLE

Front Flex Support

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DRAWING NUMBER 051-9058 SIZE D

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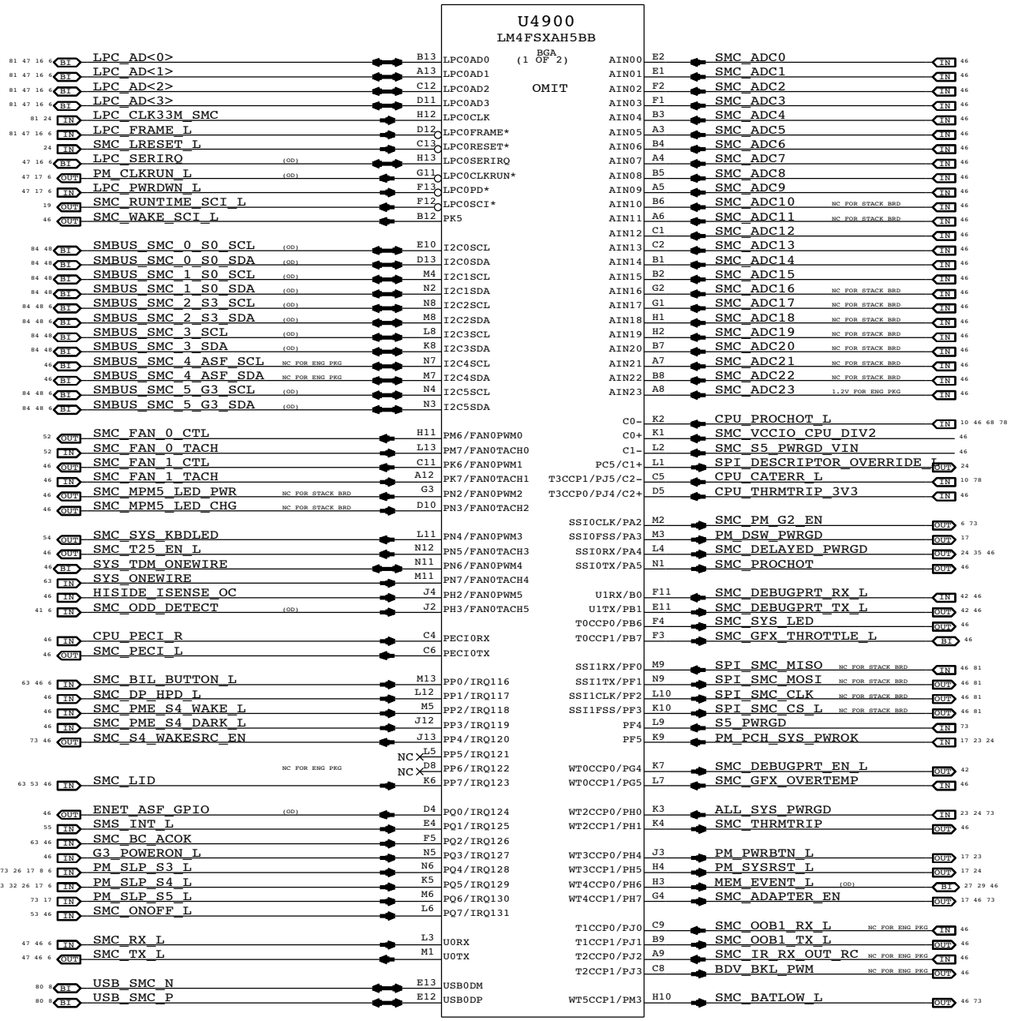

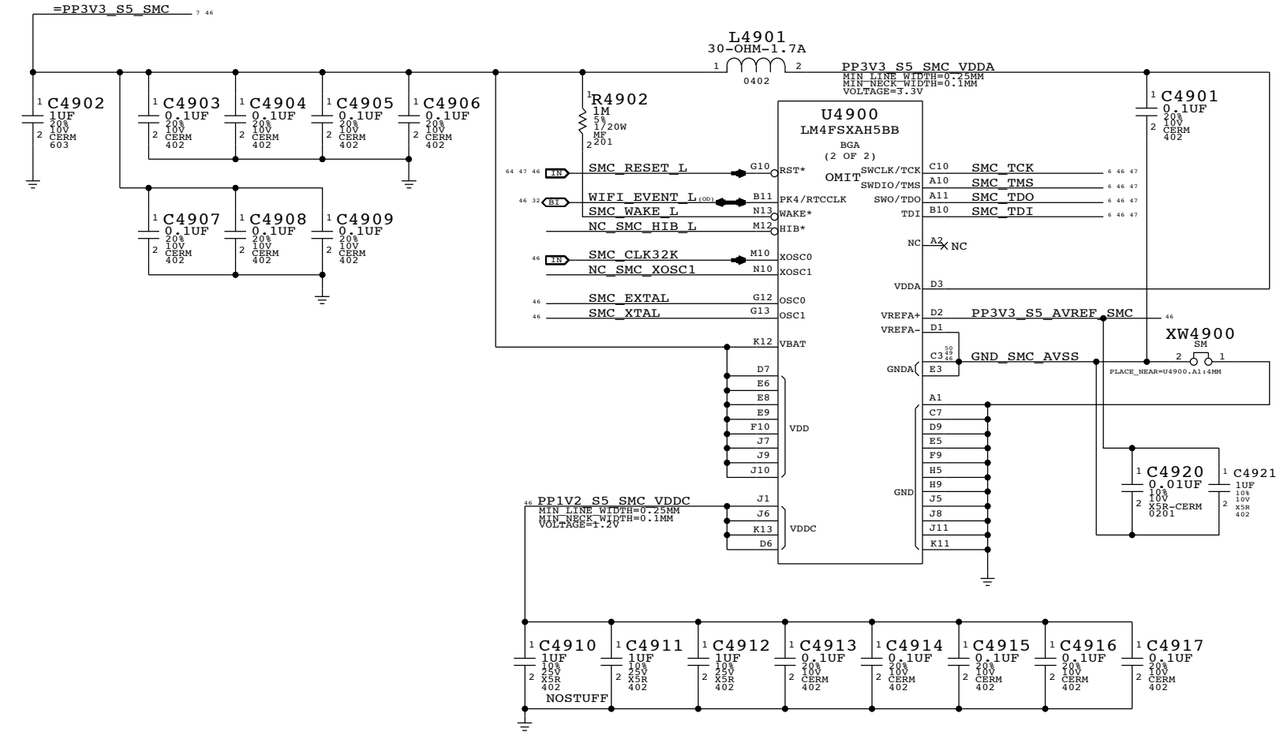

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=YONAS J30 SYNC DATE=12/21/2011

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
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PAGE 49 OF 109
SHEET 45 OF 86

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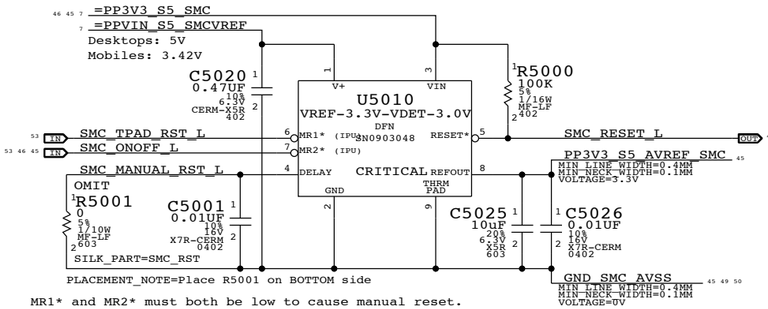
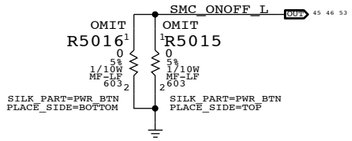
SMC Reset "Button", Supervisor & AVREF Supply



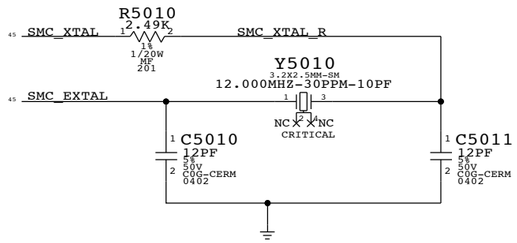
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



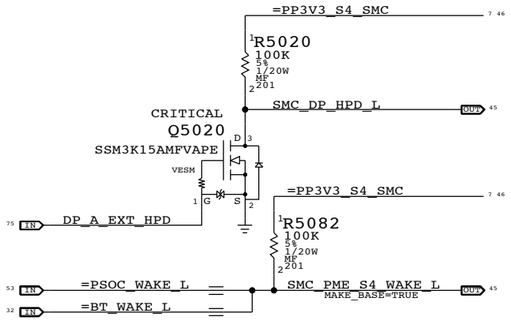
Note:
ADC10 and ADC11 are shared with comparators on Stack Board.

Note:
Pull-up for SMC_PME_S4_DARK_L are in page33 (R3315).

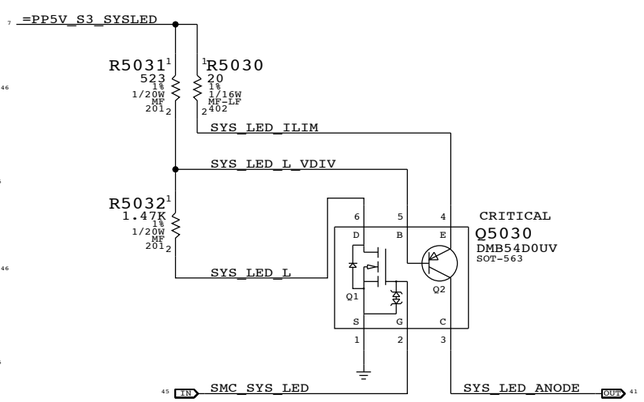
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	NC_SMC_ADC2	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_MEM_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_AXG_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	NC_SMC_ADC13	MAKE_BASE=TRUE
SMC_ADC14	NC_SMC_ADC14	MAKE_BASE=TRUE
SMC_ADC15	NC_SMC_ADC15	MAKE_BASE=TRUE
SMC_ADC16	NC_SMC_ADC16	MAKE_BASE=TRUE
SMC_ADC17	NC_SCM_ADC17	MAKE_BASE=TRUE
SMC_ADC18	SMC_AXG_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE
SMC_ADC23	SMC_ADC23	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	MAKE_BASE=TRUE
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR	MAKE_BASE=TRUE
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG	MAKE_BASE=TRUE
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	MAKE_BASE=TRUE
SMC_OOB1_RX_L	SMC_SSD_OOBD2R_L	MAKE_BASE=TRUE
SMC_OOB1_TX_L	SMC_SSD_OOBR2D_L	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE
BDV_BKL_PWM	NC_BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC	
SMC_SCI_L	SMC_WAKE_SCI_L	MAKE_BASE=TRUE
SMC_T25_EN_L	NC_SMC_T25_EN_L	MAKE_BASE=TRUE
SMC_IR_RX_OUT_RC	NC_SMC_IR_RX_OUT_RC	MAKE_BASE=TRUE

PM_CLK32K_SUSCLK_R — R5012 22 5% 1/20W MF 201 — SMC_CLK32K
PLACE_NEAR=U1800.N14:5MM

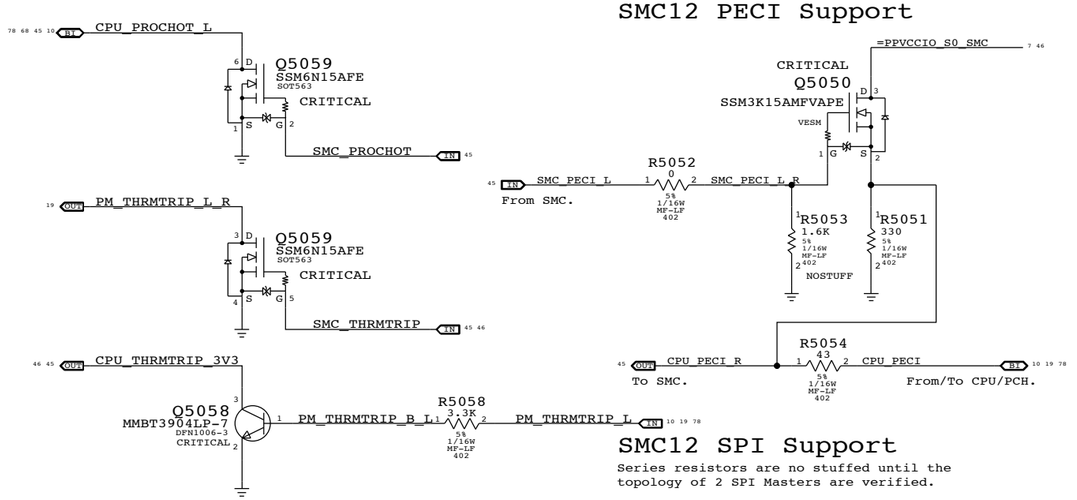
S4 HPD SMC Wake Source



System (Sleep) LED Circuit

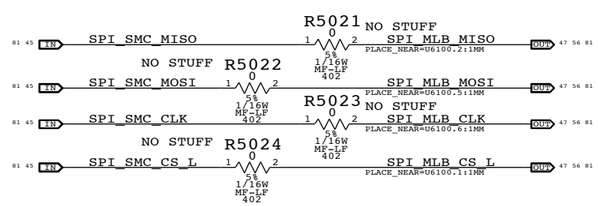


SMC12 PECI Support



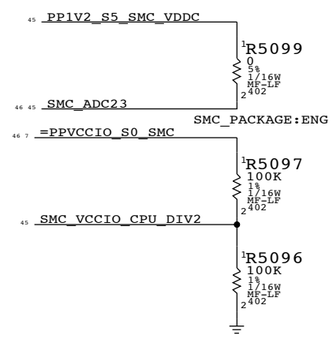
SMC12 SPI Support

Series resistors are no stuffed until the topology of 2 SPI Masters are verified.

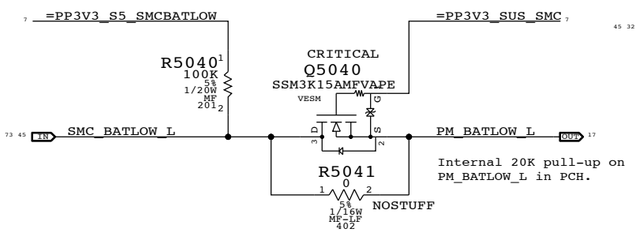


Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD

SCM12 Eng Pkg Support



BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SMC_ONOFF_L	R5070	10K	5%	1/20W	MF 201
G3_POWERON_L	R5072	10K	5%	1/20W	MF 201
SMC_LID	R5071	100K	5%	1/20W	MF 201
SMC_TX_L	R5073	10K	5%	1/20W	MF 201
SMC_RX_L	R5074	100K	5%	1/20W	MF 201
SMC_DEBUGPRT_TX_L	R5075	10K	5%	1/20W	MF 201
SMC_DEBUGPRT_RX_L	R5076	100K	5%	1/20W	MF 201
SMC_TMS	R5077	10K	5%	1/20W	MF 201
SMC_TDO	R5078	10K	5%	1/20W	MF 201
SMC_TDI	R5079	10K	5%	1/20W	MF 201
SMC_TCK	R5080	10K	5%	1/20W	MF 201
SMC_BIL_BUTTON_L	R5081	10K	5%	1/20W	MF 201
SMC_BC_ACOK	R5087	470K	5%	1/20W	MF 201
SMC_S5_PWRGD_VIN	R5092	100K	5%	1/20W	MF 201
MEM_EVENT_L	R5014	10K	5%	1/20W	MF 201
CPU_THRMTRIP_3V3	R5017	100K	5%	1/20W	MF 201
SMC_ROMBOOT					
SMC_THRMTRIP	R5086	10K	5%	1/20W	MF 201
SMC_ADAPTER_EN	R5085	10K	5%	1/20W	MF 201
SMC_DELAYED_PWRGD	R5091	100K	5%	1/20W	MF 201
SMC_S4_WAKESRC_EN	R5090	100K	5%	1/20W	MF 201
WIFI_EVENT_L	R5089	10K	5%	1/20W	MF 201

R5088 1K 5% 1/20W MF 201

=PP3V3_S5_SMC
PP3V3_WLAN

SYNC MASTER=YONAS J30 SYNC DATE=01/02/2012
PAGE TITLE
SMC Support
Apple Inc.
DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
BRANCH
PAGE 50 OF 109
SHEET 46 OF 86

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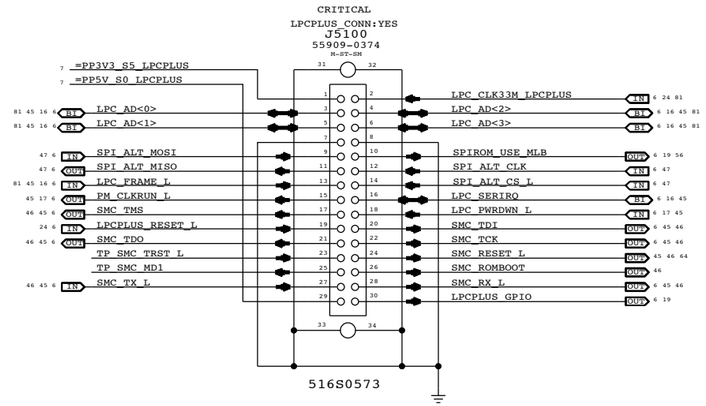
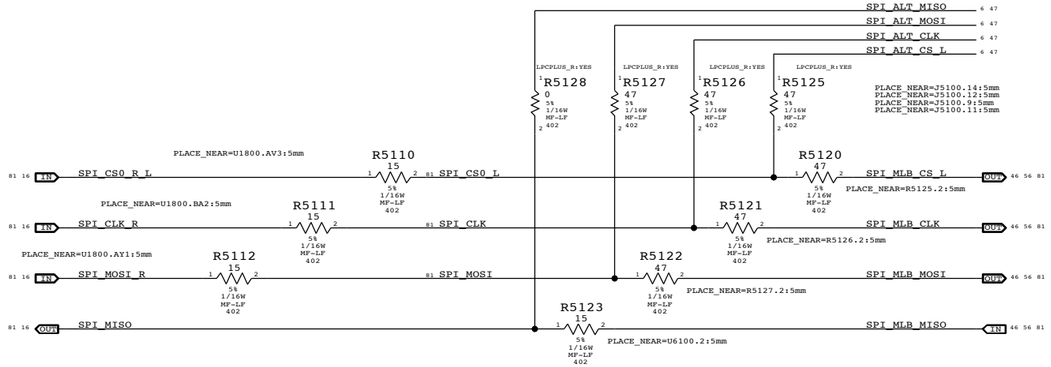
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=J31 MLB | SYNC DATE=06/15/2011

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-9058 | SIZE: D

REVISION: 6.0.0

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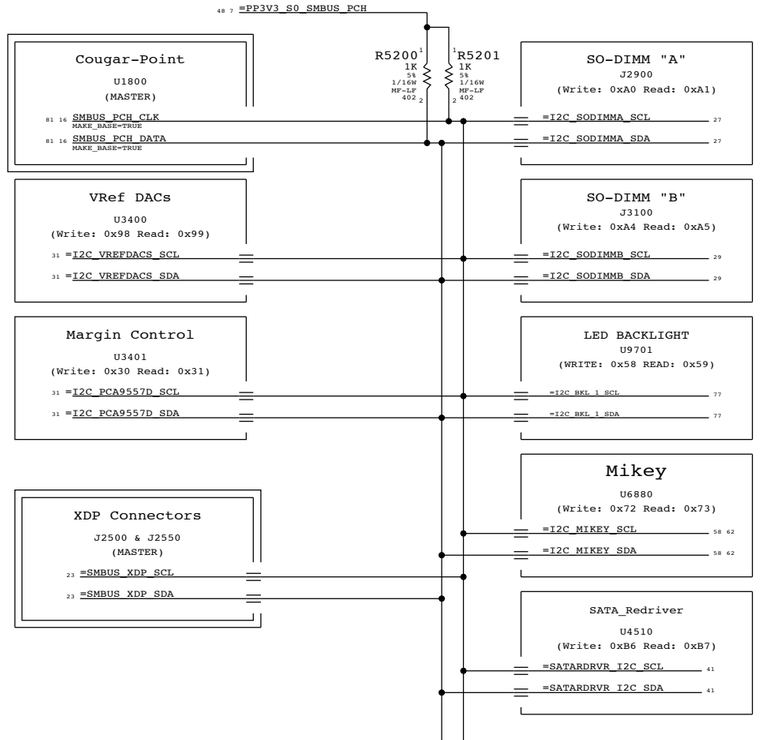
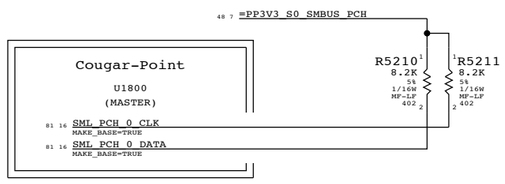
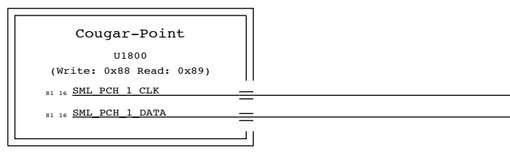
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

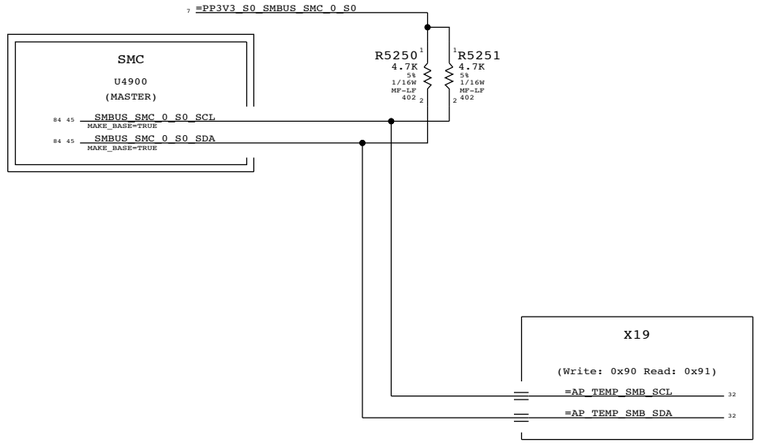


PCH "SMLink 1" Connections



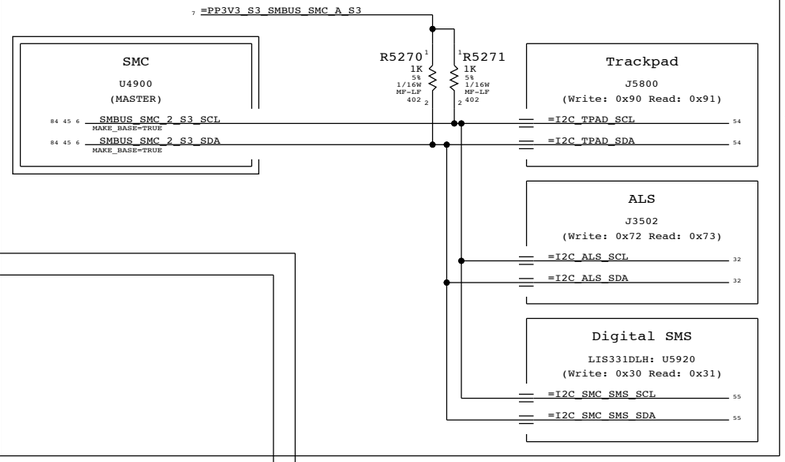
SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

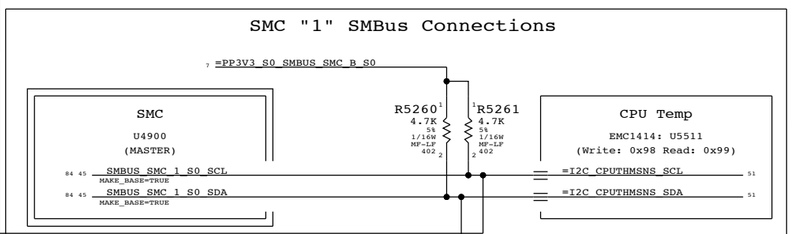


SMC "2" SMBus Connections

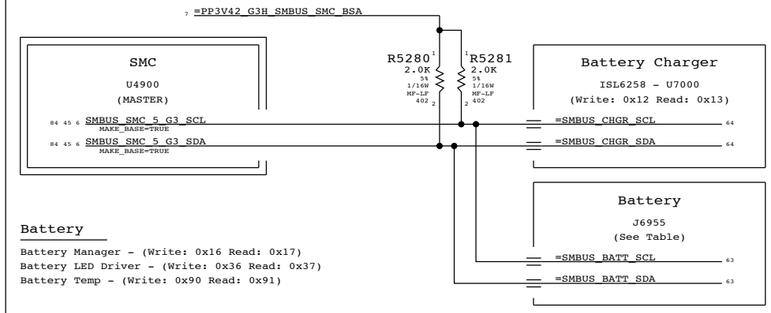
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "1" SMBus Connections



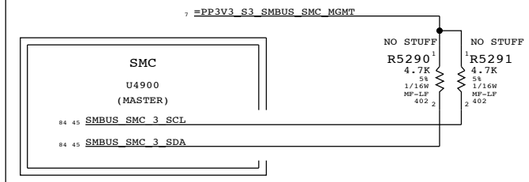
SMC "5" SMBus Connections



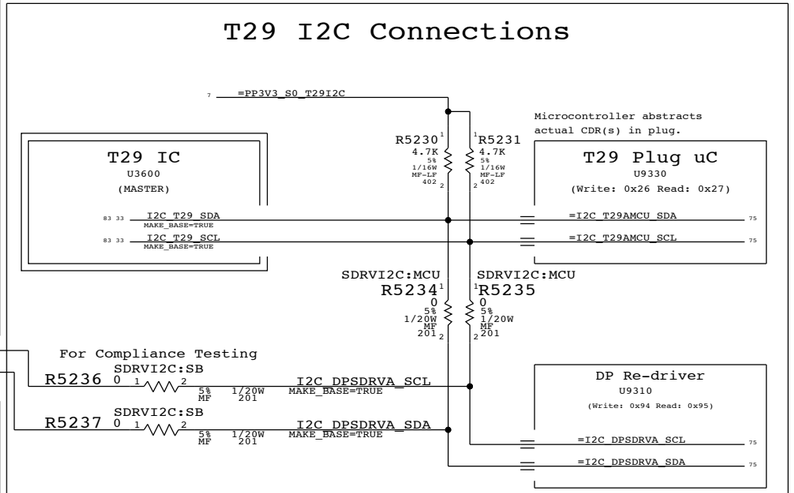
Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "3" SMBus Connections



T29 I2C Connections



SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
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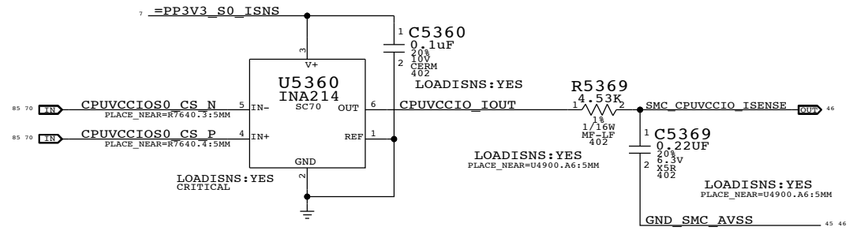
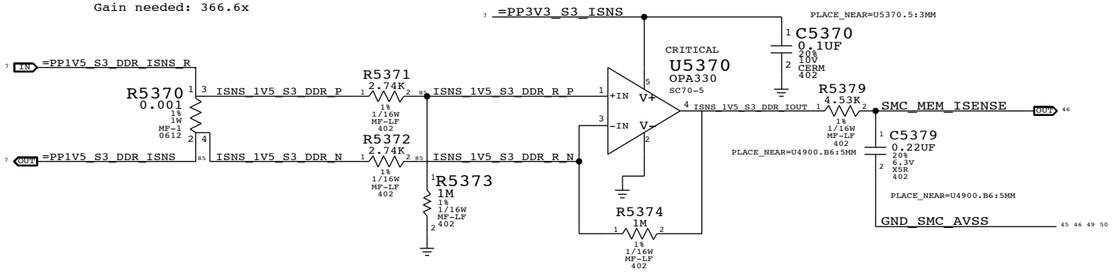
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 100x, EDP: 20.1 A
Rsense: 0.001 (R7640)
V across Rsense: 20.1 mV
Gain needed: 164.2x



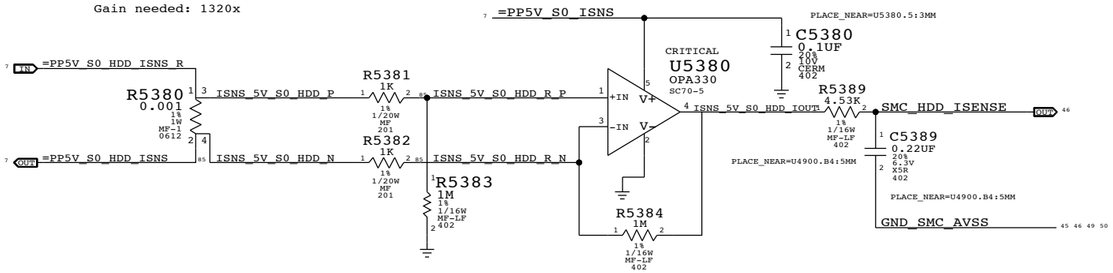
DDR 1.5V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 366.6x

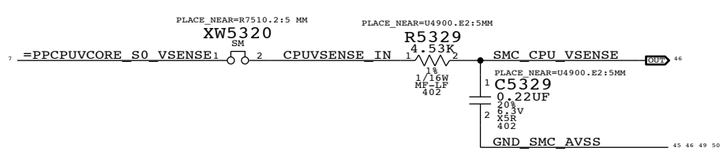


HDD Current Sense (IHDC)

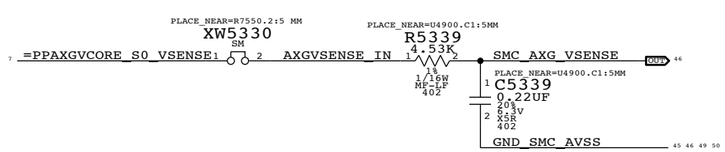
Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R5380)
V across Rsense: 2.5 mV
Gain needed: 1320x



CPU Core Voltage Sense (VC0C)

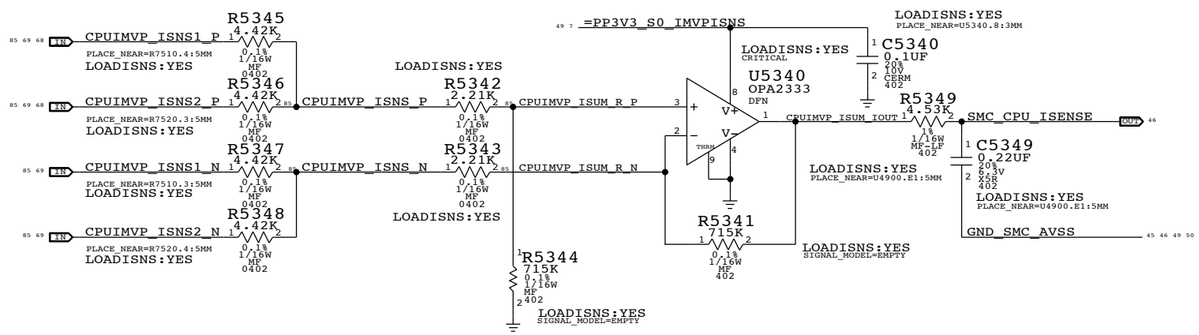


AXG Core Voltage Sense (VN0C)



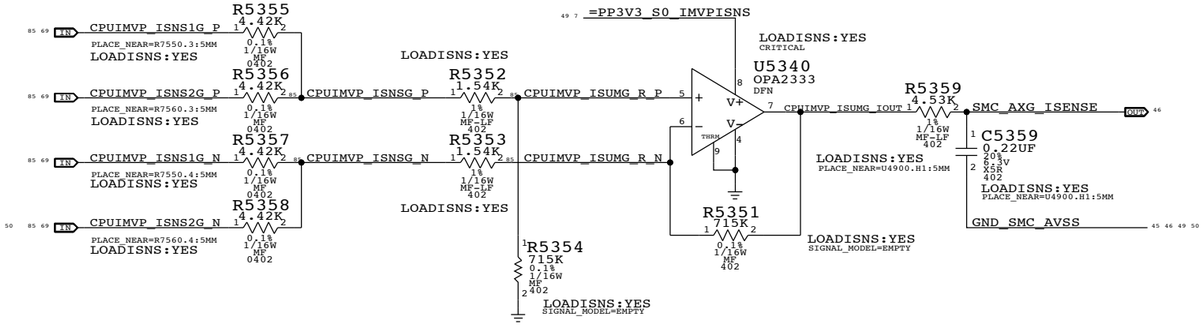
CPU Core Load Side Current Sense (IC0C)

Gain: 161.5x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
Gain needed: 166.1x



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
Gain needed: 191.3x



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	3	RES,MTL FLIM,100K,1/16W,0402,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=LINDA J30 SYNC DATE=09/28/2011

PAGE TITLE: Power Sensors: Load Side

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D
REVISION: 6.0.0
BRANCH:
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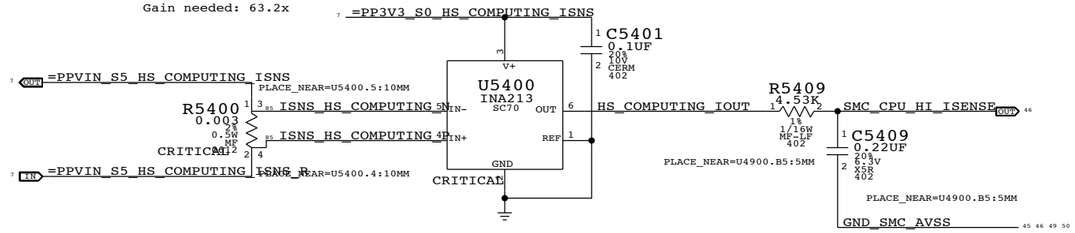
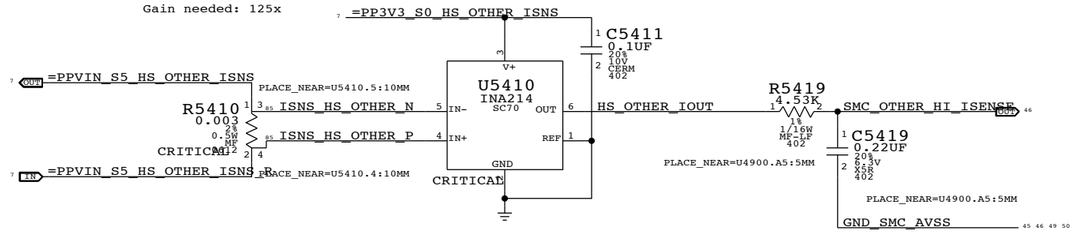
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
Gain needed: 63.2x



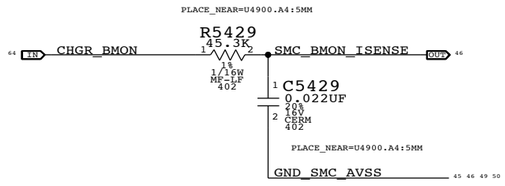
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
Gain needed: 125x



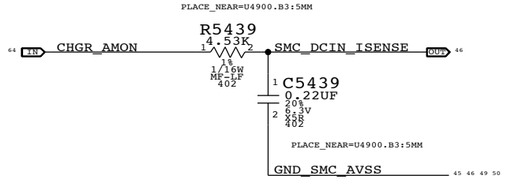
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Current Measured: 9.2 A

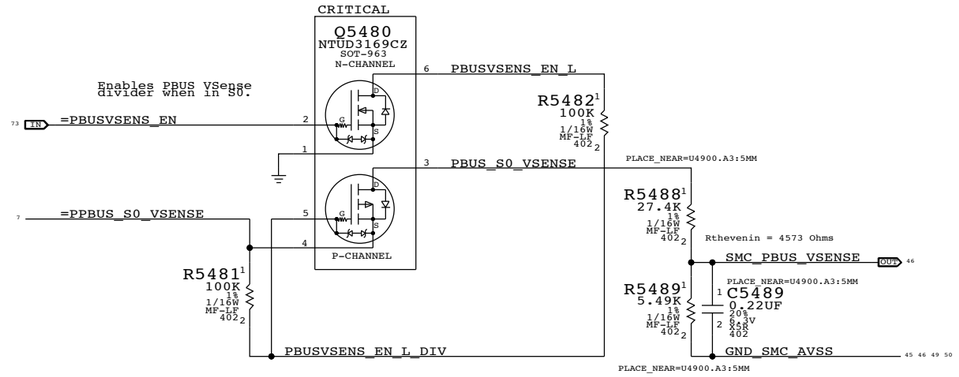


DC-In (AMON) Current Sense (ID0R)

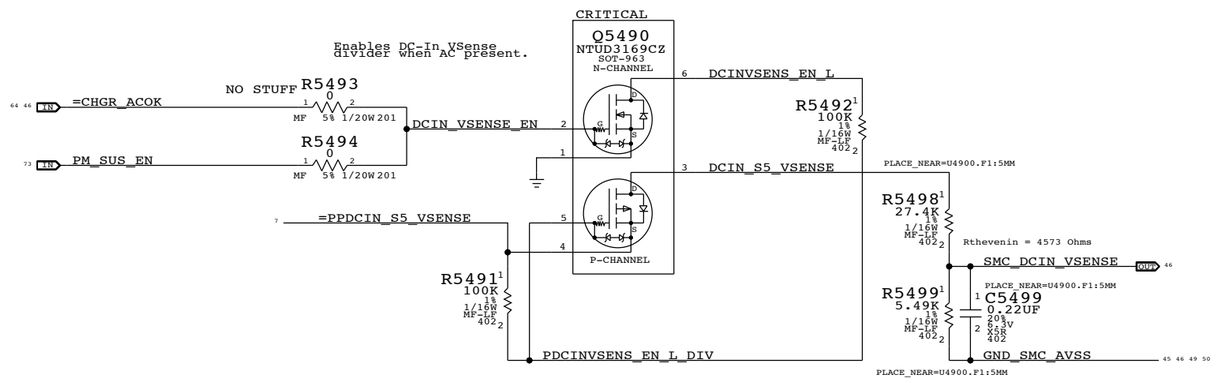
Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Current Measured: 8.3 A



PBUS Voltage Sense & Enable (VP0R)



DC In Voltage Sense & Enable (VD0R)



SYNC MASTER=YONAS J30 SYNC DATE=11/03/2011

PAGE TITLE

Power Sensors: High Side

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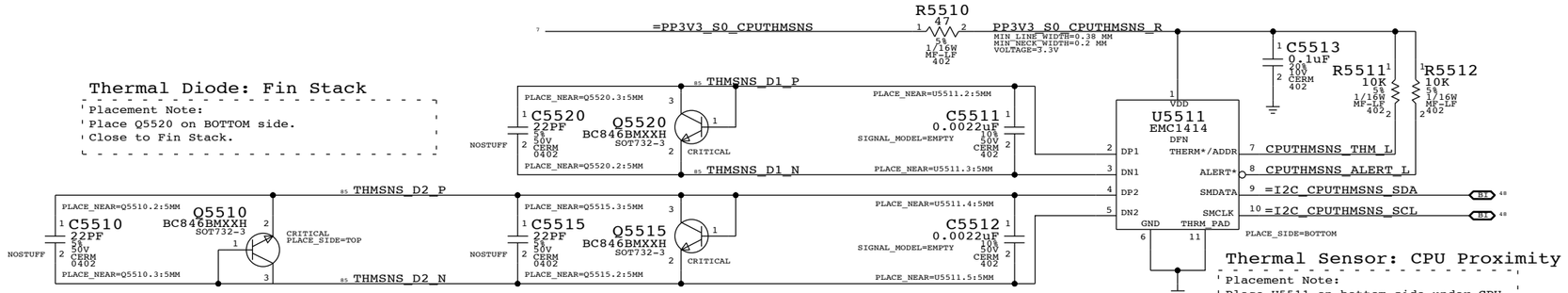
Thermal Sensor:
CPU Proximity, Fin Stack, Memory Proximity, 5V/3.3V Proximity

I2C Write, 0x98, I2C Read: 0x99



Thermal Diode: Fin Stack

Placement Note:
Place Q5520 on BOTTOM side.
Close to Fin Stack.

Thermal Diode: 5V/3.3V Proximity

Placement Note:
Place Q5510 on the TOP side,
Next to 5V and 3.3V power supplies.

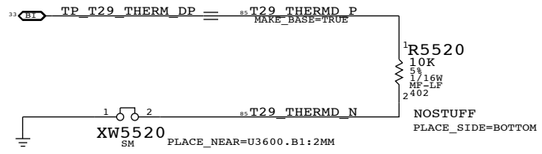
Thermal Diode: Memory Proximity

Placement Note:
Place Q5515 on the EITHER side, on the
right of DIMM connectors.

Thermal Sensor: CPU Proximity

Placement Note:
Place U5511 on bottom side under CPU

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC MASTER=YONAS J30 SYNC DATE=08/01/2011

PAGE TITLE: Thermal Sensors

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DRAWING NUMBER: 051-9058 SIZE: D
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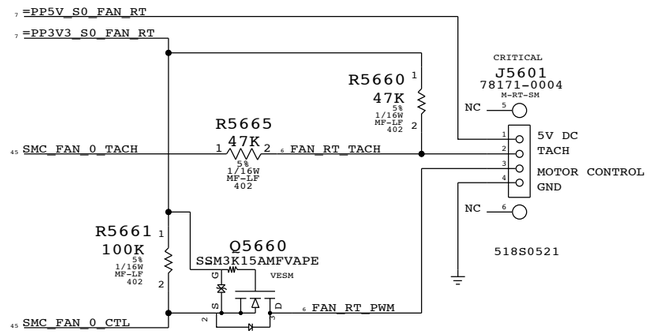

SYNC MASTER=K90I MLB SYNC DATE=02/15/2011

PAGE TITLE

Fan

Apple Inc.

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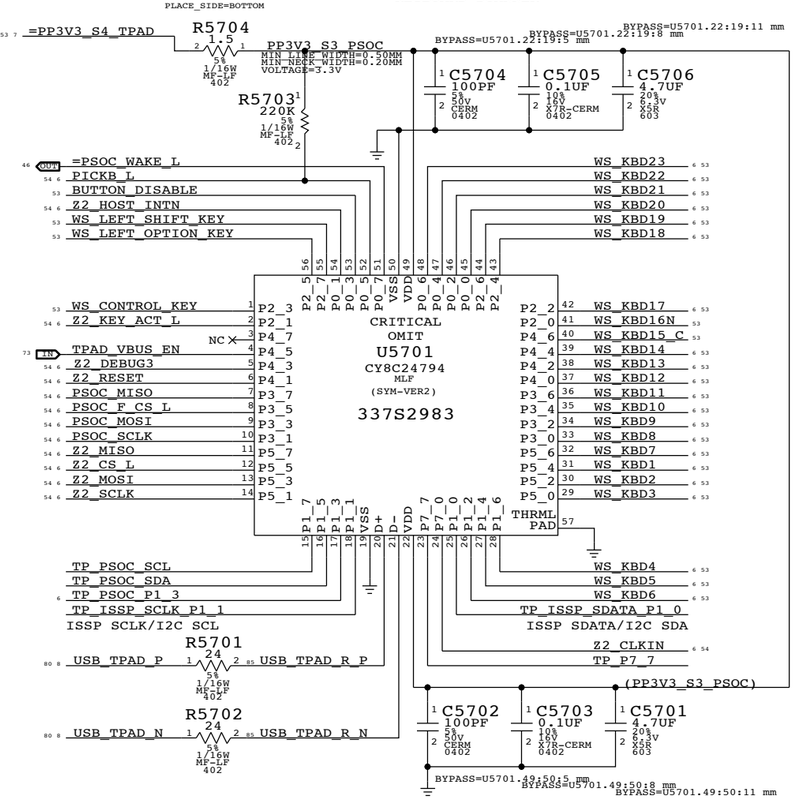
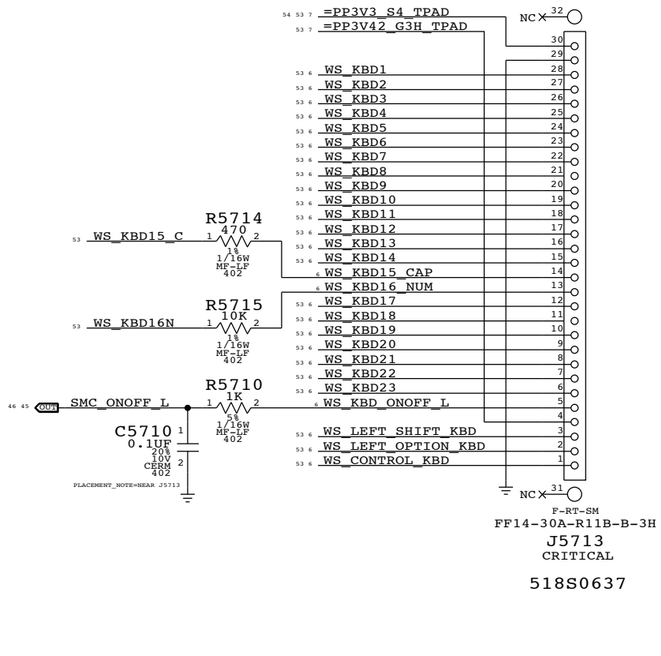
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

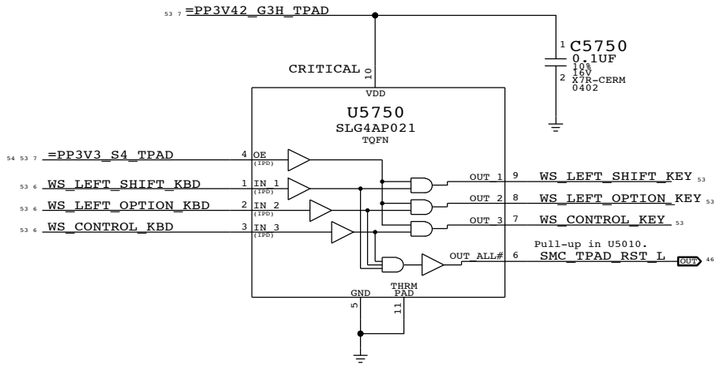
Keyboard Connector



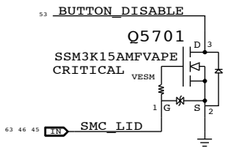
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=J31_MLB SYNC_DATE=07/01/2011

PAGE TITLE: WELLSPRING 1

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DRAWING NUMBER: 051-9058 SIZE: D
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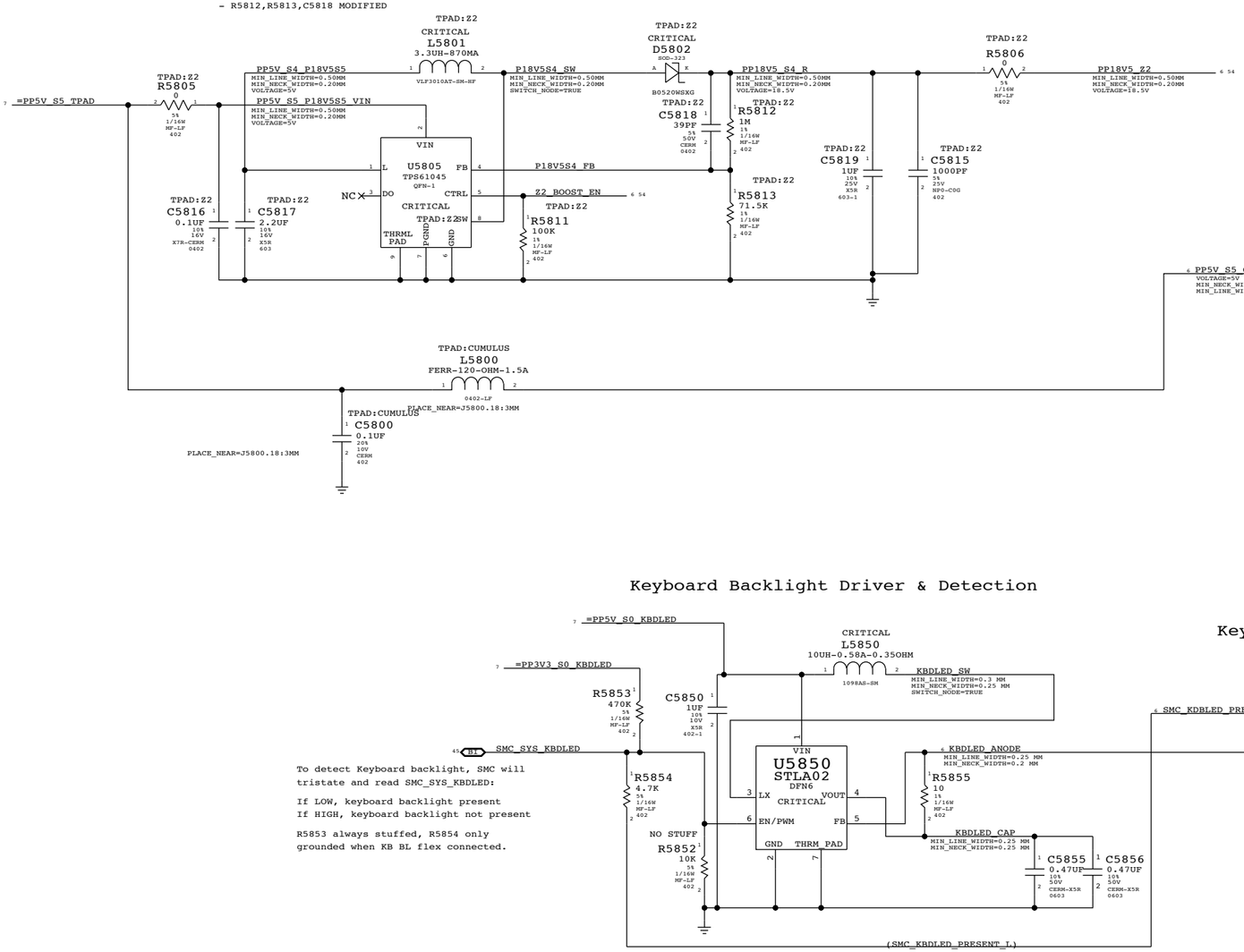
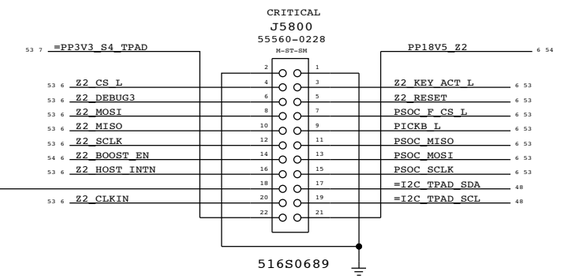
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

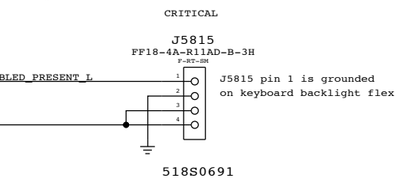
Keyboard Backlight Driver & Detection

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



SYNC MASTER=JACK J30 SYNC DATE=09/28/2011

PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D
REVISION: 6.0.0
BRANCH:
PAGE: 58 OF 109
SHEET: 54 OF 86

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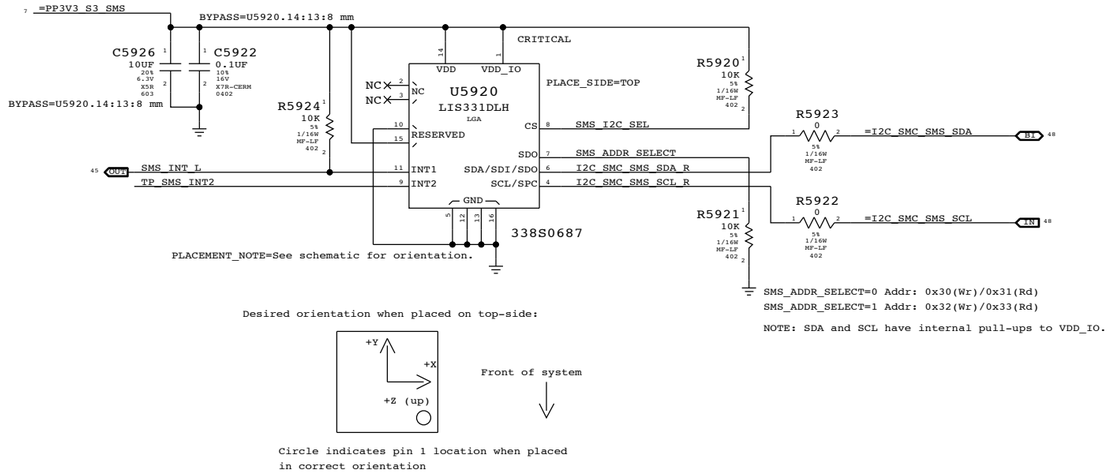

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE

Digital Accelerometer

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

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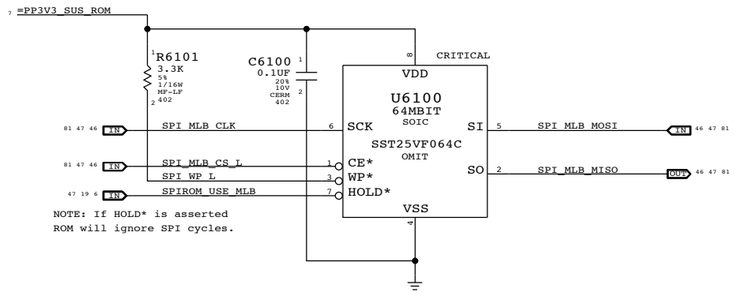

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE

SPI ROM

Apple Inc.

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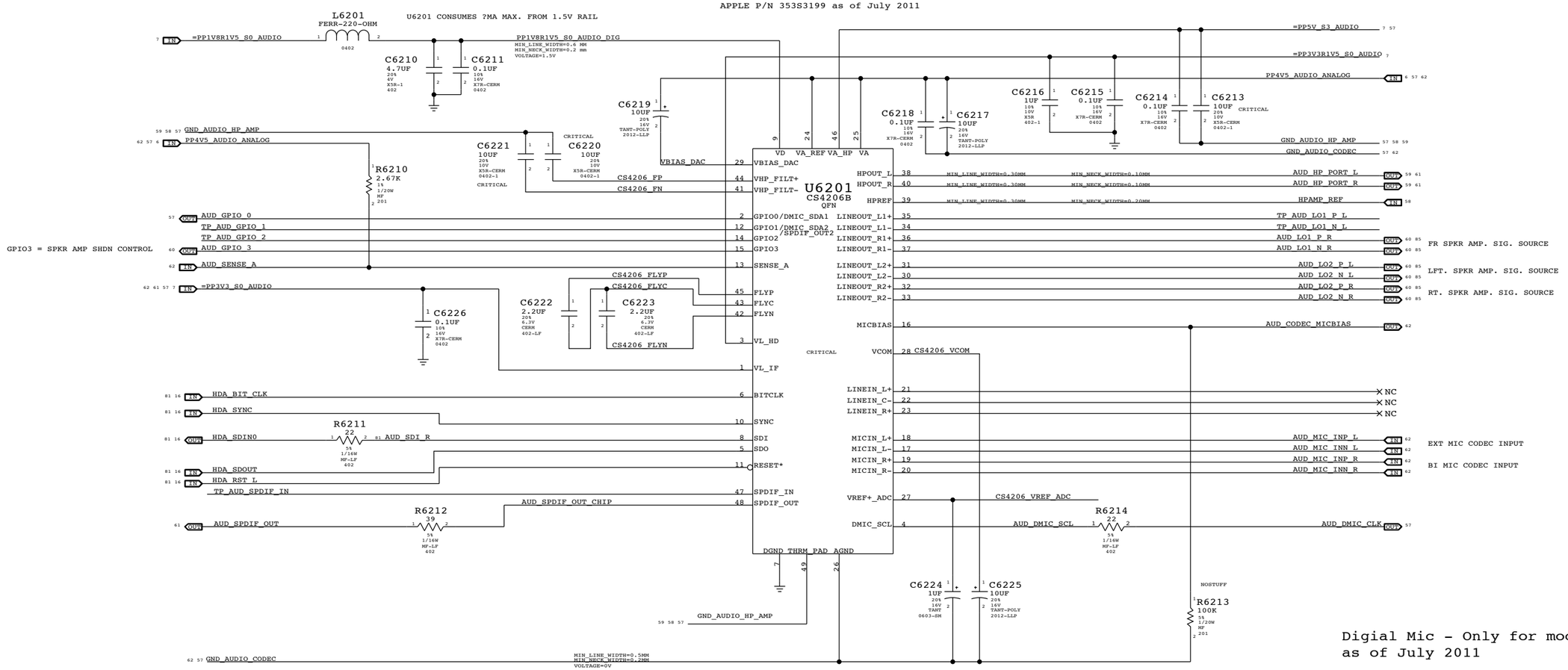
AUDIO CODEC

APPLE P/N 353S3199 as of July 2011



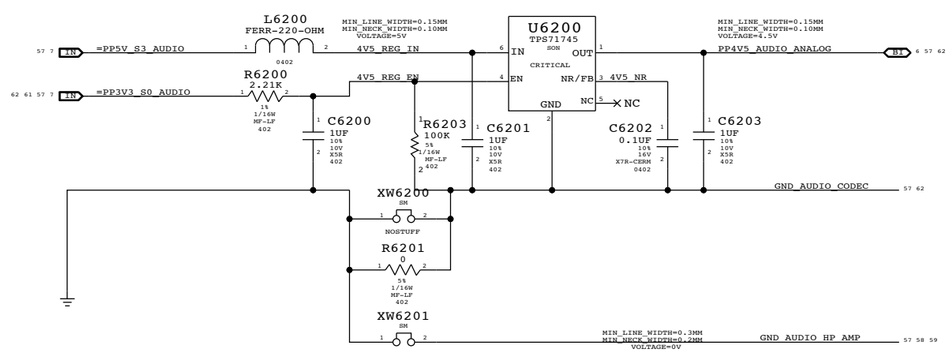
Digial Mic - Only for mock ups
as of July 2011

AUD_DMIC_CLK = TP_AUD_DMIC_CLK
MAKE_BASE=TRUE

AUD_GPIO_0 = TP_AUD_DMIC_SDATA
MAKE_BASE=TRUE

4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2281 as of July 2011



NOTES ON J30 audio

Codec HPamp used for Lineout/HPout. No external HPamp.
3 Spk amplifiers - 2 tweeters and a sub woofer
No line input capability
SPDIF out
China headset support

www.qdzbwx.com

SYNC MASTER=KAVITHA J30 | SYNC DATE=07/25/2011

PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER: 051-9058 | SIZE: D
REVISION: 6.0.0
BRANCH:
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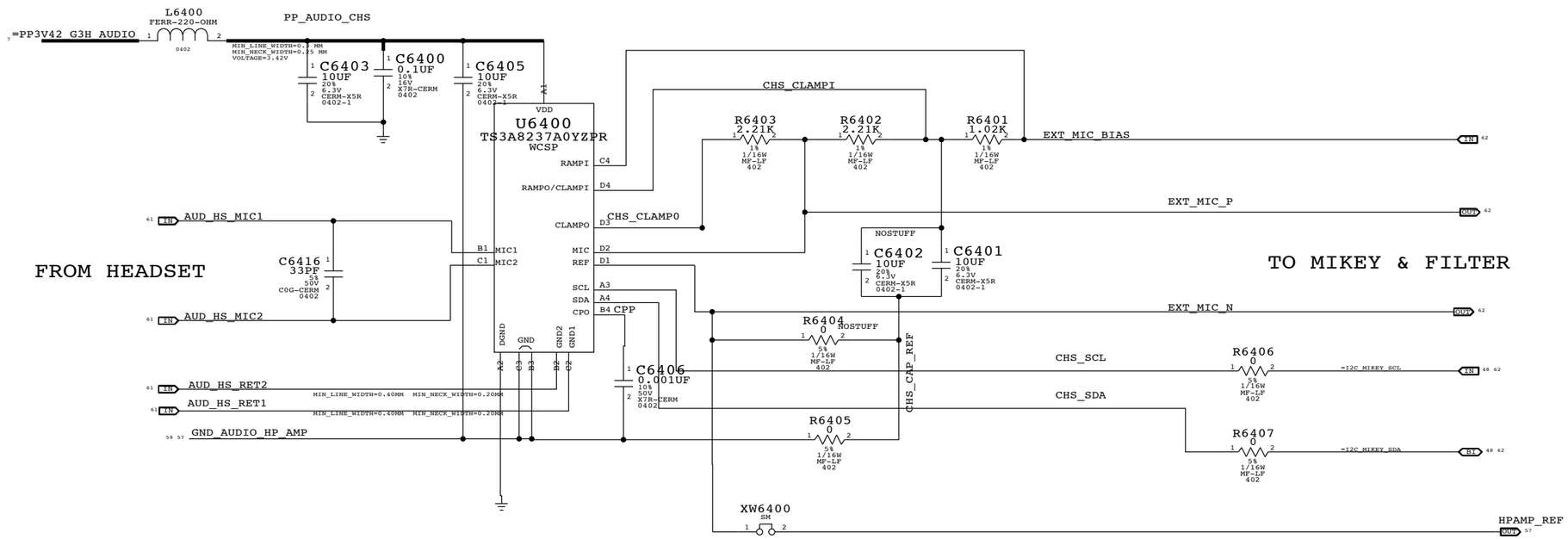
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY APN:353S3066 as of July 2011



I2C ADDRESSES: CHS uses SMBus 0 connections

CHS	U6400	READ	0111	0111	0x77
CHS	U6400	WRITE	0111	0110	0x76

SYNC MASTER=DIRK J30 SYNC DATE=02/16/2012

PAGE TITLE
AUDIO: DETECT/MIC BIAS

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
BRANCH
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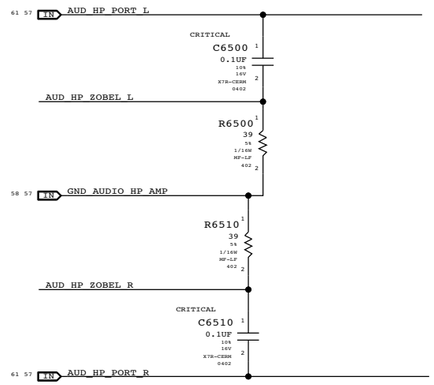
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER=KAVITHA J30 SYNC DATE=07/25/2011

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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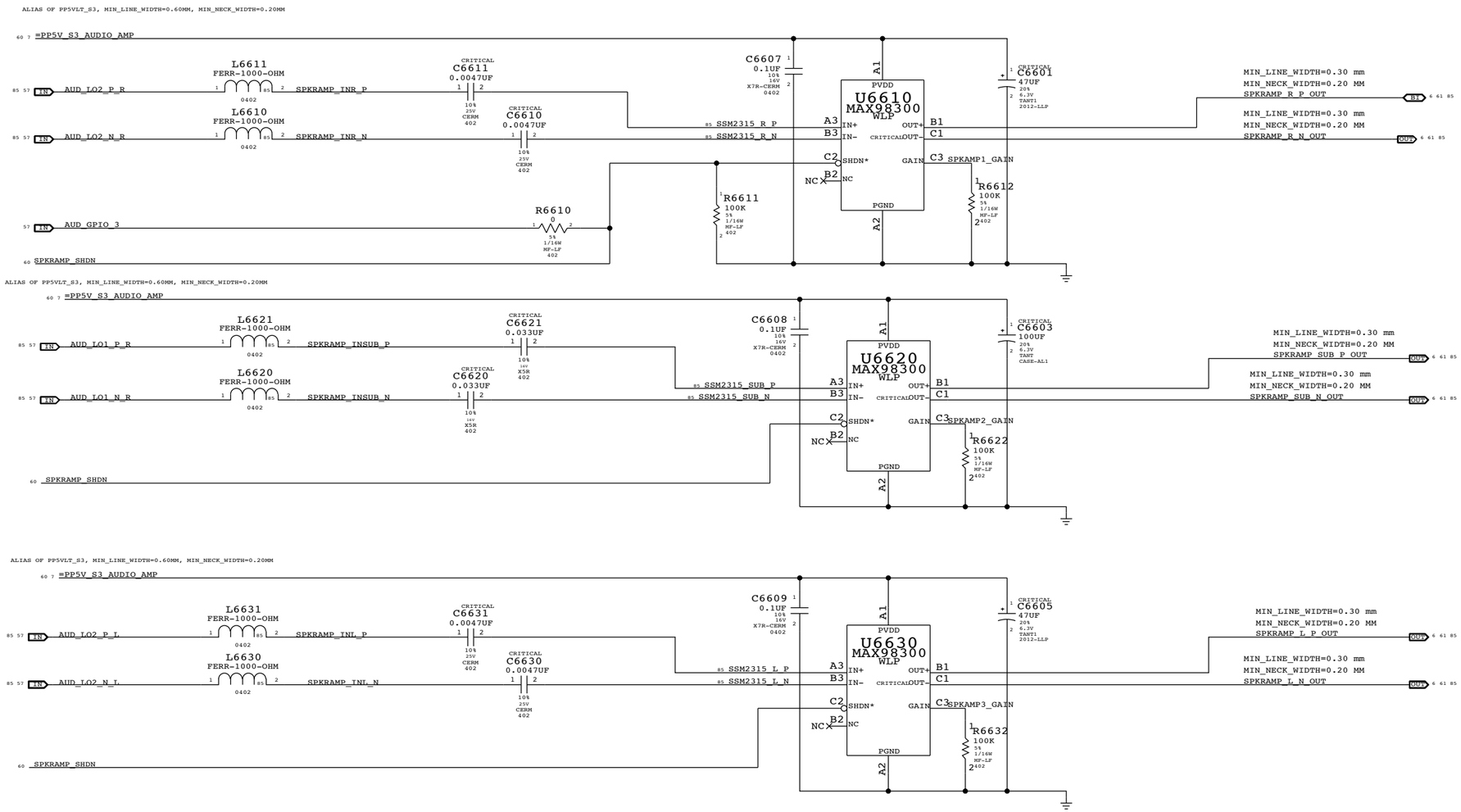
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2888 as of July 2011

SATELLITE	FC=1.2kHz typical
SUB	FC= 172 HZ typical
GAIN	3DB with Rin=28k typical

Gain Pin	Gain dB
Connect to VDD	12
Connect to VDD through 100k	9
Not connected	6
Connect to GND through 100k	3
Connect to GND	0



SYNC MASTER=KAVITHA J30 SYNC DATE=07/25/2011

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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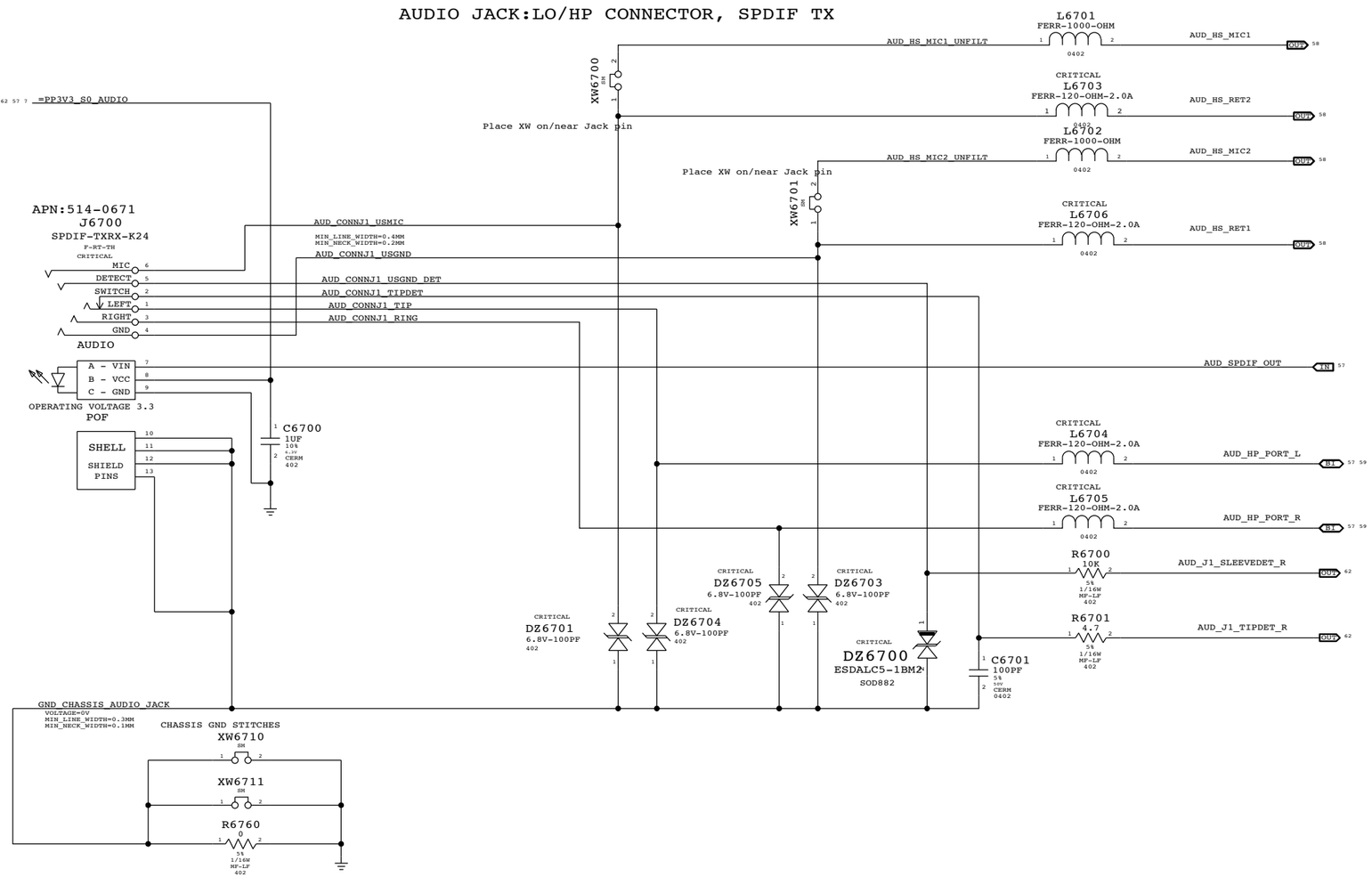
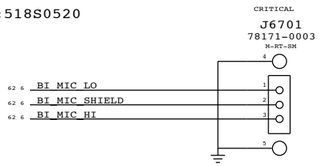
AUDIO JACK:LO/HP CONNECTOR, SPDIF TX



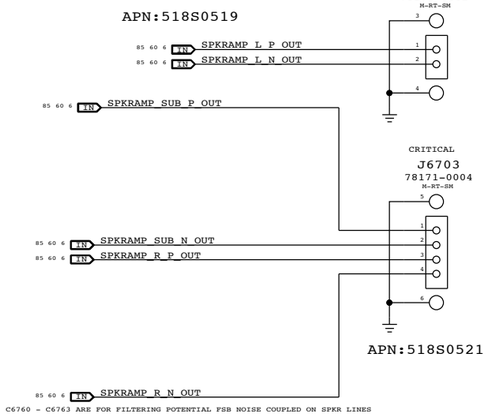
ANALOG MIC CONNECTOR

APN:518S0520



SPEAKER CONNECTOR

APN:518S0519



C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

SYNC MASTER=DIRK J30 SYNC DATE=11/10/2011

PAGE TITLE

AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SOUTHBRIDGE RESOURCES

FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	PANTHER_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	PANTHER_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	PANTHER_POINT GPIO3/PIRQH

PORT A DETECT (HEADPHONES)

PORT B DETECT(SPDIF DELEGATE)

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ

PORT B RIGHT(BUILT-IN MIC)

HP=80HZ

EXTRACTION NOTIFICATION

I2C addresses: Mikey uses SMBus 0

MIKEY	U6880	READ	0111	0011	0x73
MIKEY	U6880	WRITE	0111	0010	0x72

SYNC MASTER=DIRK J30	SYNC DATE=02/20/2012
PAGE TITLE	AUDIO:Jack Translators
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
	REVISION 6.0.0
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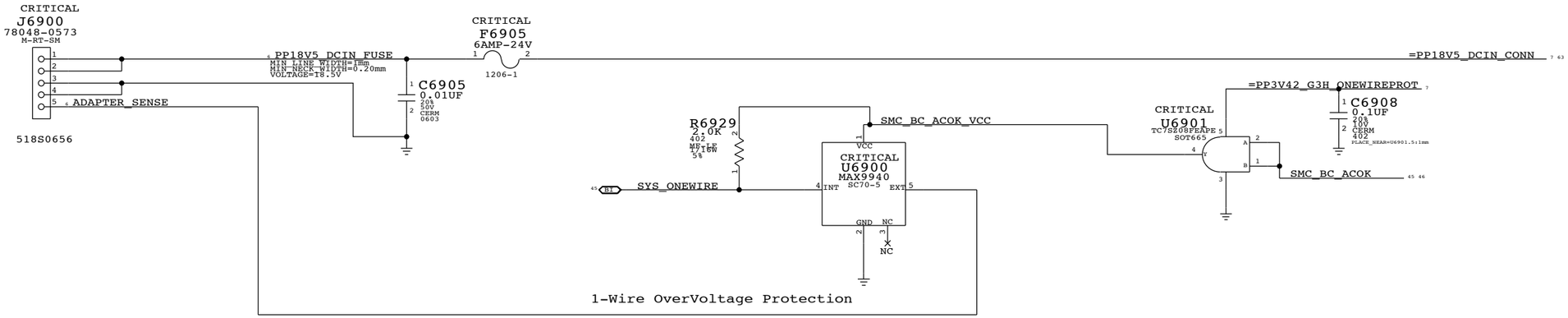
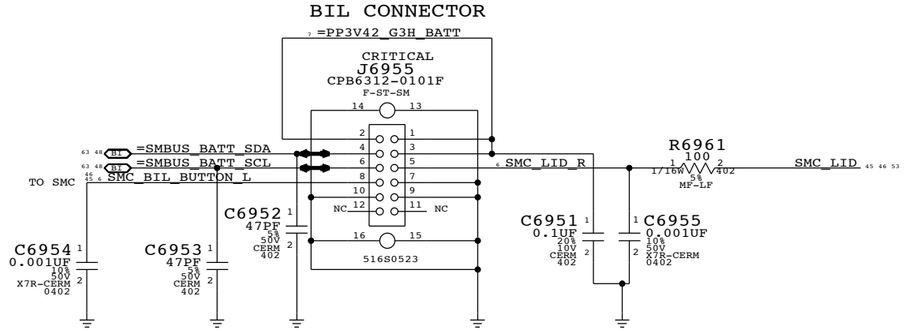
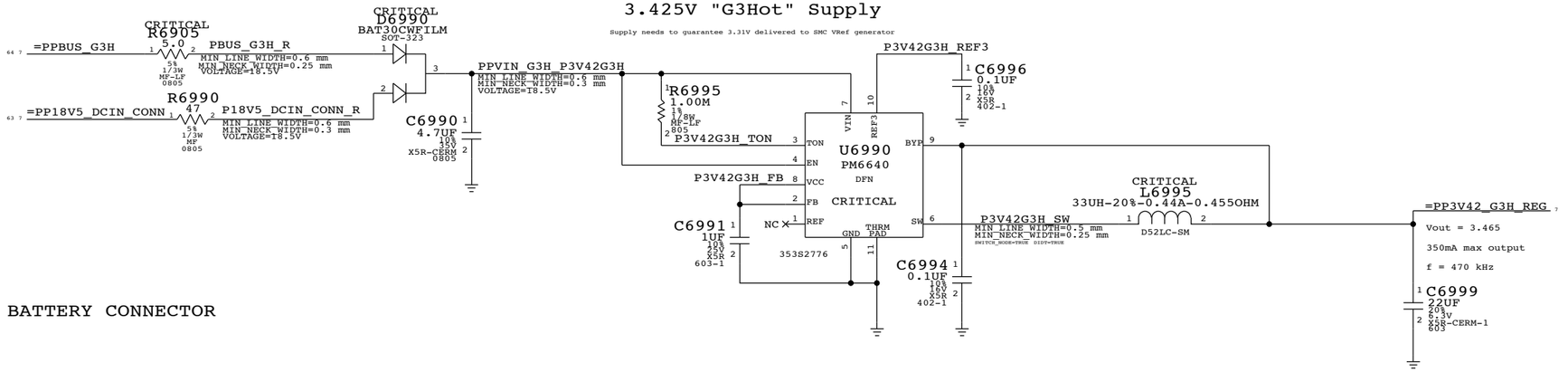
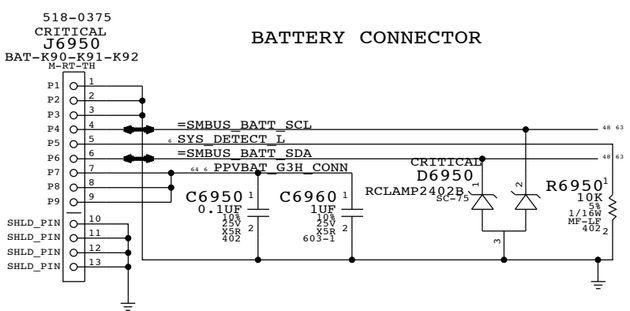
MagSafe DC Power Jack









SYNC MASTER=JACK J30	SYNC DATE=07/29/2011
PAGE TITLE	DC-In & Battery Connectors
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
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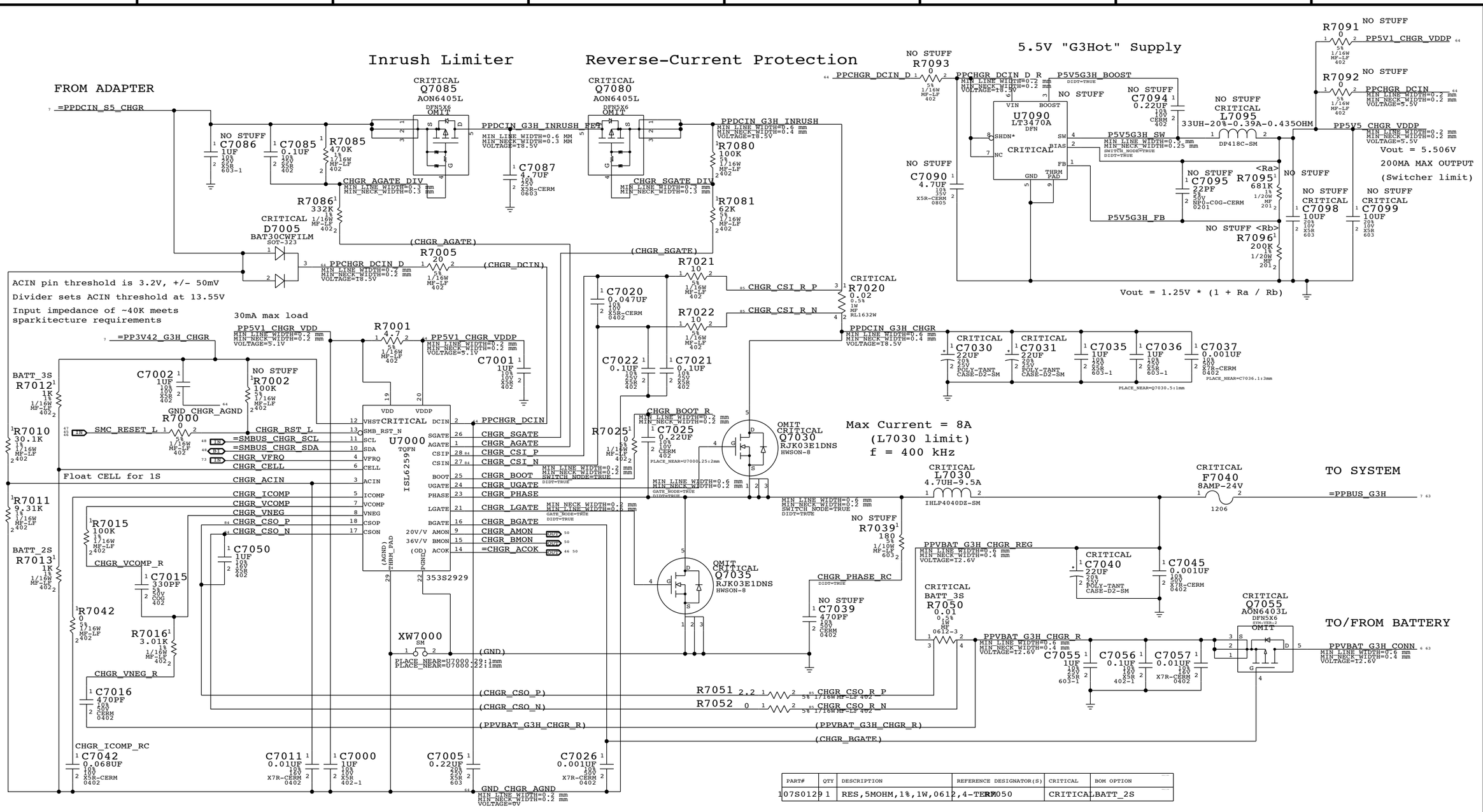

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0129	1	RES,5MOHM,1%,1W,0612,4-TERM	R7050	CRITICAL	BATT_2S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	2	FDMC3020DC	Q7030,Q7035	CRITICAL	CHARGER_POWER_FET:FAIR
376S0966	2	RJK03E1DNS	Q7030,Q7035	CRITICAL	CHARGER_POWER_FET:REN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0761	1	SI7137DP	Q7055	CRITICAL	
376S0845	1	SI7149DP	Q7080	CRITICAL	
376S0845	1	SI7149DP	Q7085	CRITICAL	

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC MASTER=JACK J30 SYNC DATE=09/27/2013

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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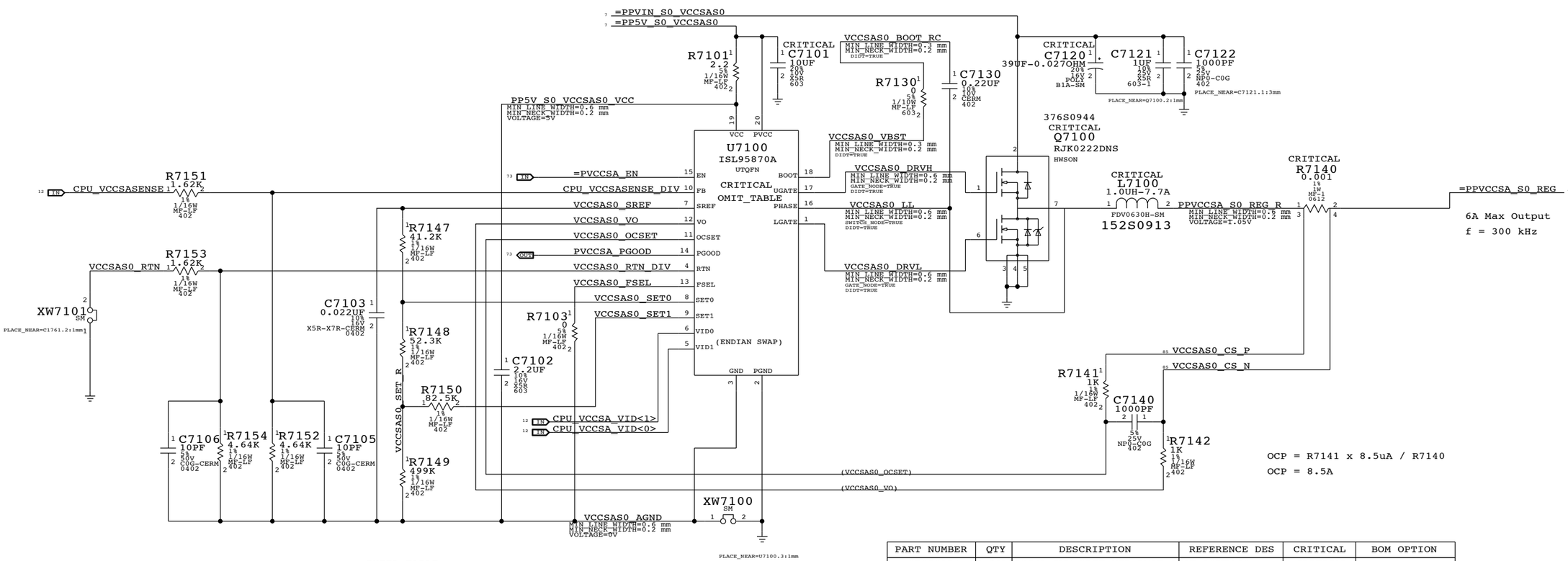
System Agent Power Supply



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20	U7100	CRITICAL	

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=JACK J30 SYNC_DATE=09/28/2011

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

BRANCH:

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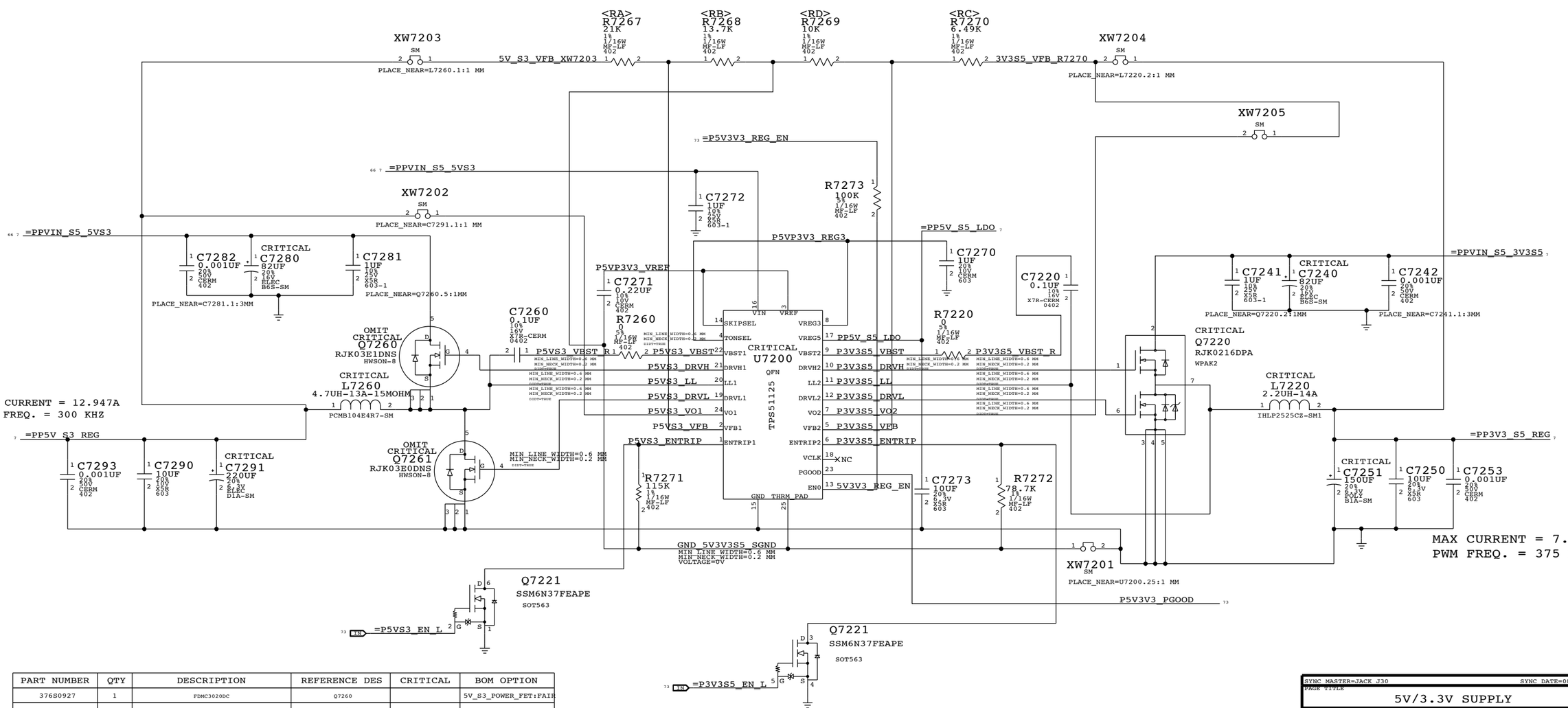
5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	1	FDMC3020DC	Q7260		5V_S3_POWER_FET:FAIR
376S0928	1	FDMC2514SDC	Q7261		5V_S3_POWER_FET:FAIR
376S0966	1	RJK03E1DNS	Q7260		5V_S3_POWER_FET:REN
376S0895	1	RJK03E0DNS	Q7261		5V_S3_POWER_FET:REN

SYNC MASTER=JACK J30 SYNC DATE=08/22/2011

PAGE TITLE

5V/3.3V SUPPLY

Apple Inc.

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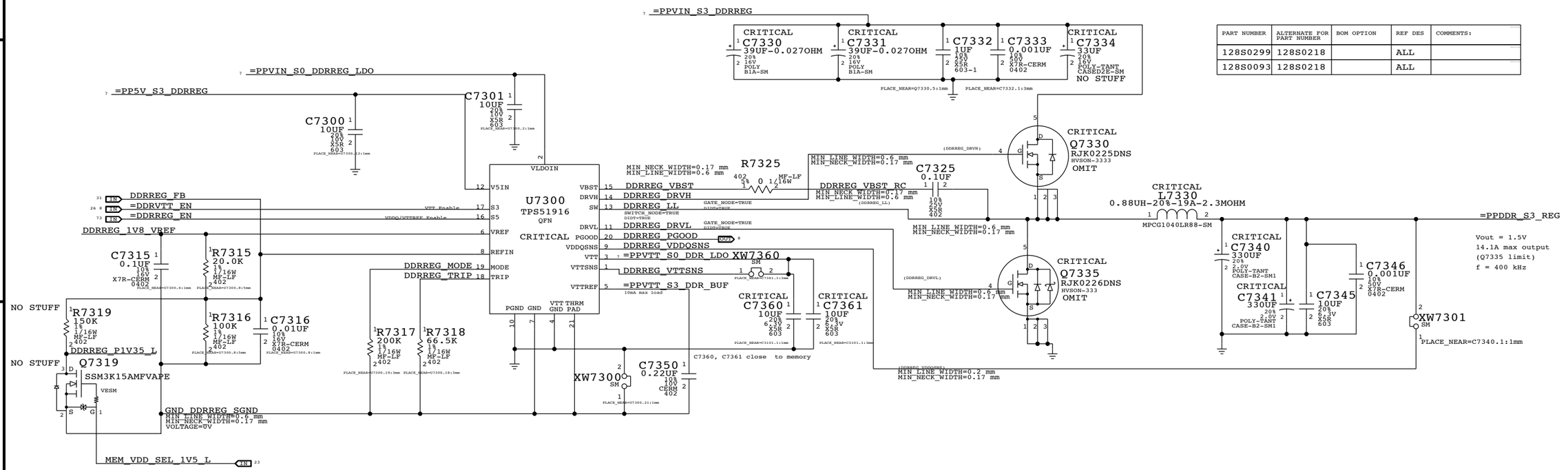

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0979	1	FDMC0225	Q7330		DDR_POWER_FET:FAIR
376S0874	1	FDMC0202S	Q7335		DDR_POWER_FET:FAIR

SYNC_MASTER=JACK_J30 SYNC_DATE=07/28/2011

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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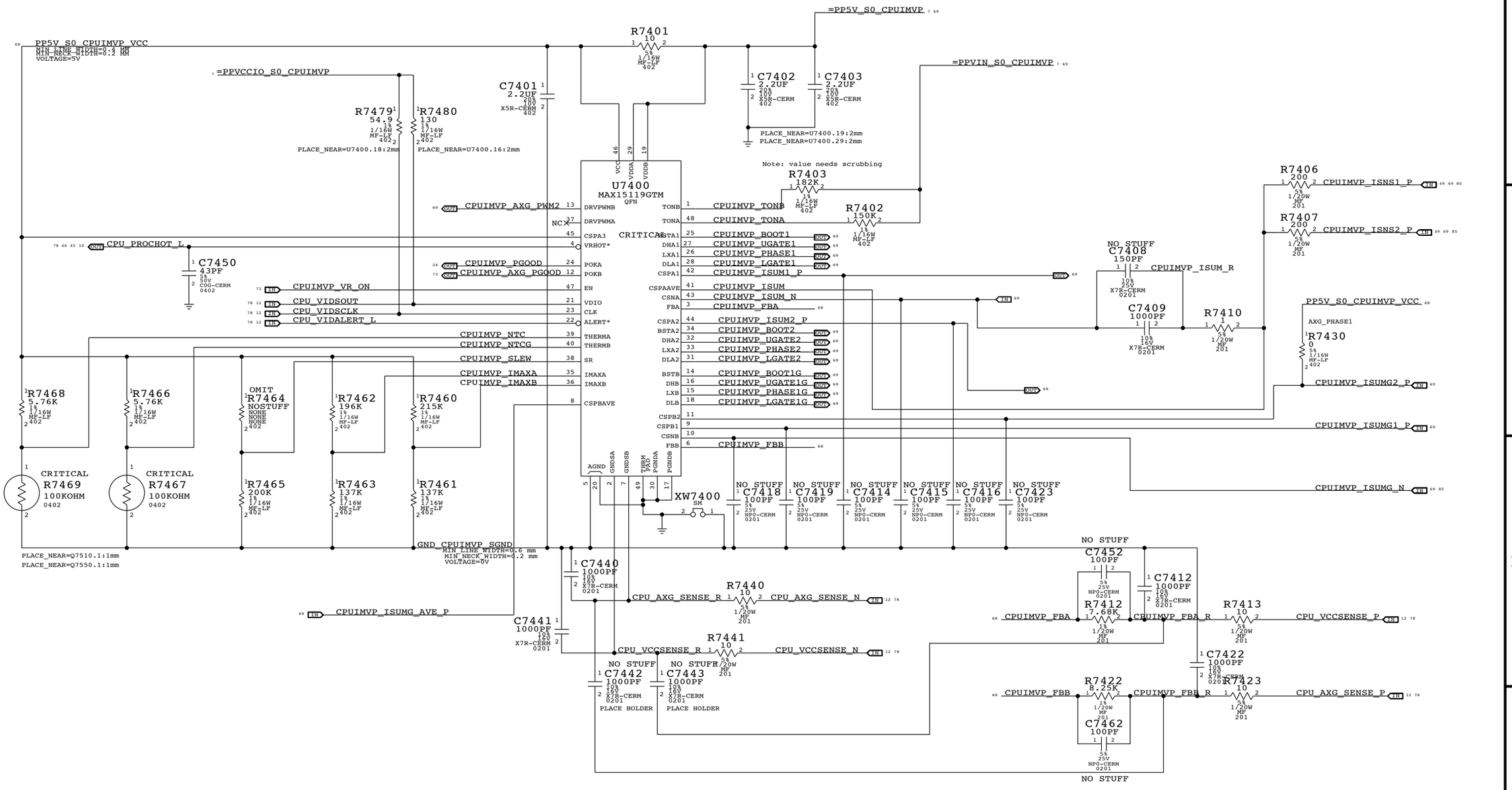

SYNC_MASTER=JACK_J30 SYNC_DATE=08/03/2011

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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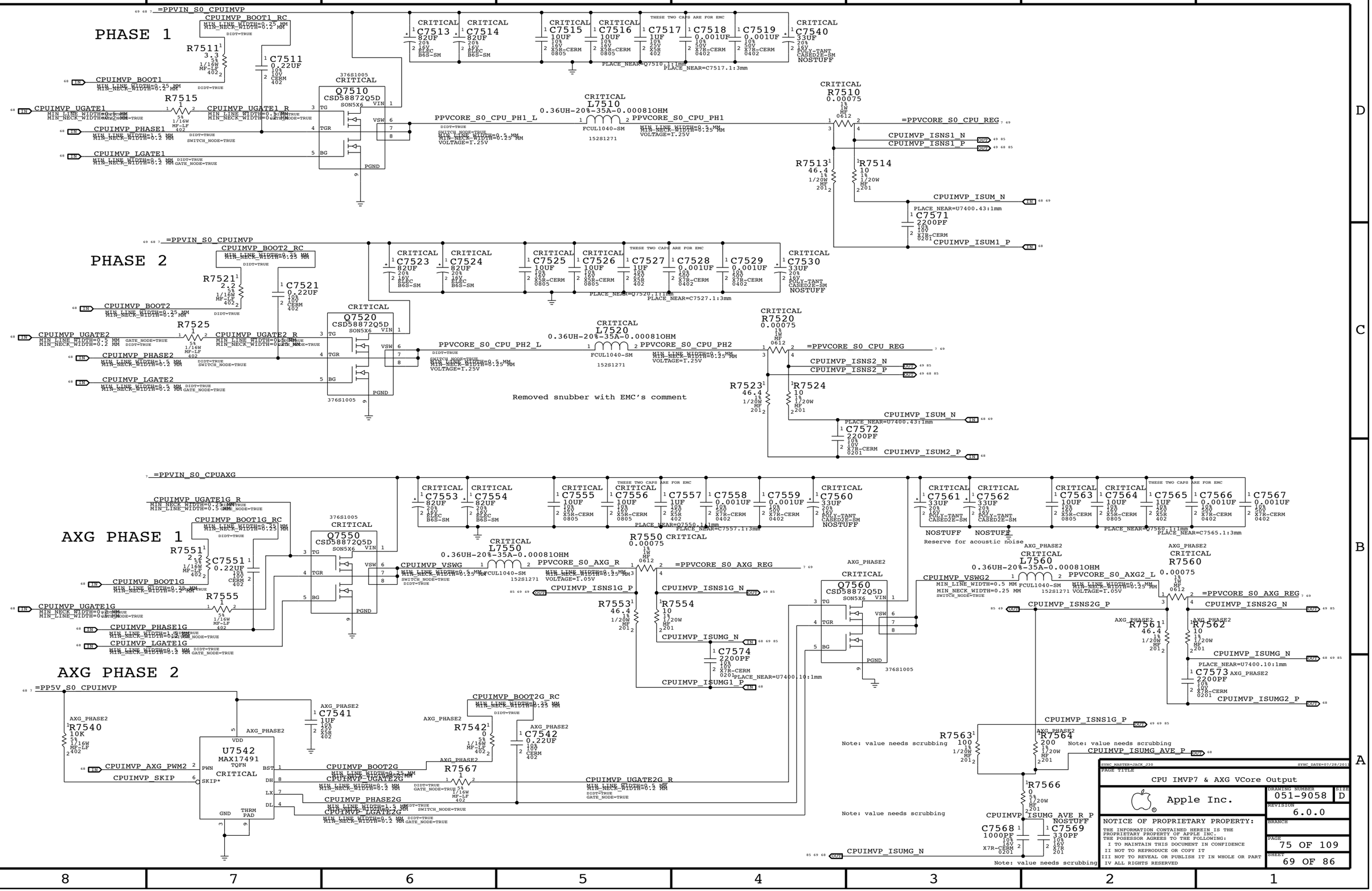
PHASE 1
=PPVIN_S0_CPUIMVP
CPUIMVP_BOOT1_RC
R7511 3.3 5% 1/16W MF-LF 402
C7511 0.22UF 10% 10V CERM 402
CPUIMVP_BOOT1
CPUIMVP_UGATE1
R7515 1 5% 1/16W MF-LF 402
CPUIMVP_UGATE1_R
CPUIMVP_PHASE1
CPUIMVP_LGATE1
376S1005
CRITICAL
Q7510
CSD58872Q5D
SON5X6
TG
TGR
BG
VIN
VSW
PGND
C7513 82UF 20% 16V ELEC B6S-SM
C7514 82UF 20% 16V ELEC B6S-SM
C7515 10UF 10% 16V X5R-CERM 0805
C7516 10UF 10% 16V X5R-CERM 0805
THESE TWO CAPS ARE FOR EMC
C7517 1UF 10% 25V X5R 402
C7518 0.001UF 10% 50V X7R-CERM 0402
C7519 0.001UF 10% 50V X7R-CERM 0402
C7540 33UF 20% 16V POLY-TANT CASED2E-SM NOSTUFF
PLACE_NEAR=Q7510.11mm
PLACE_NEAR=C7517.1:3mm
L7510 0.36UH-20%-35A-0.00081OHM FCUL1040-SM 152S1271
PPVCORE_S0_CPU_PH1_L
PPVCORE_S0_CPU_PH1
R7510 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS1_N
CPUIMVP_ISNS1_P
R7513 46.4 1% 1/20W MF 201
R7514 10 1% 1/20W MF 201
CPUIMVP_ISUM_N
C7571 2200PF 10% 10V X7R-CERM 0201
CPUIMVP_ISUM1_P
PHASE 2
=PPVIN_S0_CPUIMVP
CPUIMVP_BOOT2_RC
R7521 2.2 5% 1/16W MF-LF 402
C7521 0.22UF 10% 10V CERM 402
CPUIMVP_BOOT2
CPUIMVP_UGATE2
R7525 1 5% 1/16W MF-LF 402
CPUIMVP_UGATE2_R
CPUIMVP_PHASE2
CPUIMVP_LGATE2
Q7520
CSD58872Q5D
C7523 82UF 20% 16V ELEC B6S-SM
C7524 82UF 20% 16V ELEC B6S-SM
C7525 10UF 10% 16V X5R-CERM 0805
C7526 10UF 10% 16V X5R-CERM 0805
C7527 1UF 10% 25V X5R 402
C7528 0.001UF 10% 50V X7R-CERM 0402
C7529 0.001UF 10% 50V X7R-CERM 0402
C7530 33UF 20% 16V POLY-TANT CASED2E-SM NOSTUFF
PLACE_NEAR=Q7520.11mm
PLACE_NEAR=C7527.1:3mm
L7520 0.36UH-20%-35A-0.00081OHM FCUL1040-SM 152S1271
PPVCORE_S0_CPU_PH2_L
PPVCORE_S0_CPU_PH2
R7520 0.00075 1% 1W MF 0612
=PPVCORE_S0_CPU_REG
CPUIMVP_ISNS2_N
CPUIMVP_ISNS2_P
R7523 46.4 1% 1/20W MF 201
R7524 10 1% 1/20W MF 201
CPUIMVP_ISUM_N
C7572 2200PF 10% 10V X7R-CERM 0201
CPUIMVP_ISUM2_P
Removed snubber with EMC's comment
=PPVIN_S0_CPUAXG
AXG PHASE 1
CPUIMVP_UGATE1G_R
CPUIMVP_BOOT1G_RC
R7551 2.2 5% 1/16W MF-LF 402
C7551 0.22UF 10% 10V CERM 402
CPUIMVP_BOOT1G
CPUIMVP_UGATE1G
R7555 1 5% 1/16W MF-LF 402
CPUIMVP_PHASE1G
CPUIMVP_LGATE1G
Q7550
CSD58872Q5D
C7553 82UF 20% 16V ELEC B6S-SM
C7554 82UF 20% 16V ELEC B6S-SM
C7555 10UF 10% 16V X5R-CERM 0805
C7556 10UF 10% 16V X5R-CERM 0805
C7557 1UF 10% 25V X5R 402
C7558 0.001UF 10% 50V X7R-CERM 0402
C7559 0.001UF 10% 50V X7R-CERM 0402
C7560 33UF 20% 16V POLY-TANT CASED2E-SM NOSTUFF
PLACE_NEAR=Q7550.11mm
PLACE_NEAR=C7557.1:3mm
L7550 0.36UH-20%-35A-0.00081OHM FCUL1040-SM 152S1271
CPUIMVP_VSWG
PPVCORE_S0_AXG_R
R7550 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS1G_N
CPUIMVP_ISNS1G_P
R7553 46.4 1% 1/20W MF 201
R7554 10 1% 1/20W MF 201
CPUIMVP_ISUMG_N
C7574 2200PF 10% 10V X7R-CERM 0201
CPUIMVP_ISUMG1_P
Q7560
CSD58872Q5D
C7561 33UF 20% 16V POLY-TANT CASED2E-SM NOSTUFF
C7562 33UF 20% 16V POLY-TANT CASED2E-SM NOSTUFF
C7563 10UF 10% 16V X5R-CERM 0805
C7564 10UF 10% 16V X5R-CERM 0805
C7565 1UF 10% 25V X5R 402
C7566 0.001UF 10% 50V X7R-CERM 0402
C7567 0.001UF 10% 50V X7R-CERM 0402
PLACE_NEAR=Q7560.11mm
PLACE_NEAR=C7565.1:3mm
Reserve for acoustic noise
L7560 0.36UH-20%-35A-0.00081OHM FCUL1040-SM 152S1271
CPUIMVP_VSWG2
PPVCORE_S0_AXG2_L
R7560 0.00075 1% 1W MF 0612
=PPVCORE_S0_AXG_REG
CPUIMVP_ISNS2G_P
CPUIMVP_ISNS2G_N
R7561 46.4 1% 1/20W MF 201
R7562 10 1% 1/20W MF 201
CPUIMVP_ISUMG_N
C7573 2200PF 10% 10V X7R-CERM 0201
CPUIMVP_ISUMG2_P
AXG PHASE 2
=PP5V_S0_CPUIMVP
R7540 10K 5% 1/16W MF-LF 402
C7541 1UF 10% 10V X5R 402
CPUIMVP_AXG_PWM2
CPUIMVP_SKIP
U7542
MAX17491
TQFN
CRITICAL
PWN
SKIP*
BST
DH
LX
DL
VDD
GND
THRM PAD
CPUIMVP_BOOT2G_RC
R7542 0 5% 1/16W MF-LF 402
C7542 0.22UF 10% 10V CERM 402
R7567 1 5% 1/16W MF-LF 402
CPUIMVP_BOOT2G
CPUIMVP_UGATE2G
CPUIMVP_PHASE2G
CPUIMVP_LGATE2G
CPUIMVP_UGATE2G_R
Note: value needs scrubbing
R7563 100 1% 1/20W MF 201
R7564 200 1% 1/20W MF 201
R7566 0 5% 1/20W MF 201
C7568 1000PF 10% 16V X7R-CERM 0201
C7569 330PF 10% 16V X7R 201
CPUIMVP_ISUMG_AVE_P
CPUIMVP_ISUMG_AVE_R_P
CPUIMVP_ISNS1G_P
CPUIMVP_ISUMG_N
SYNC_MASTER=JACK_J30
SYNC_DATE=07/28/2011
PAGE TITLE
CPU IMVP7 & AXG VCore Output
Apple Inc.
DRAWING NUMBER 051-9058
SIZE D
REVISION 6.0.0
BRANCH
PAGE 75 OF 109
SHEET 69 OF 86
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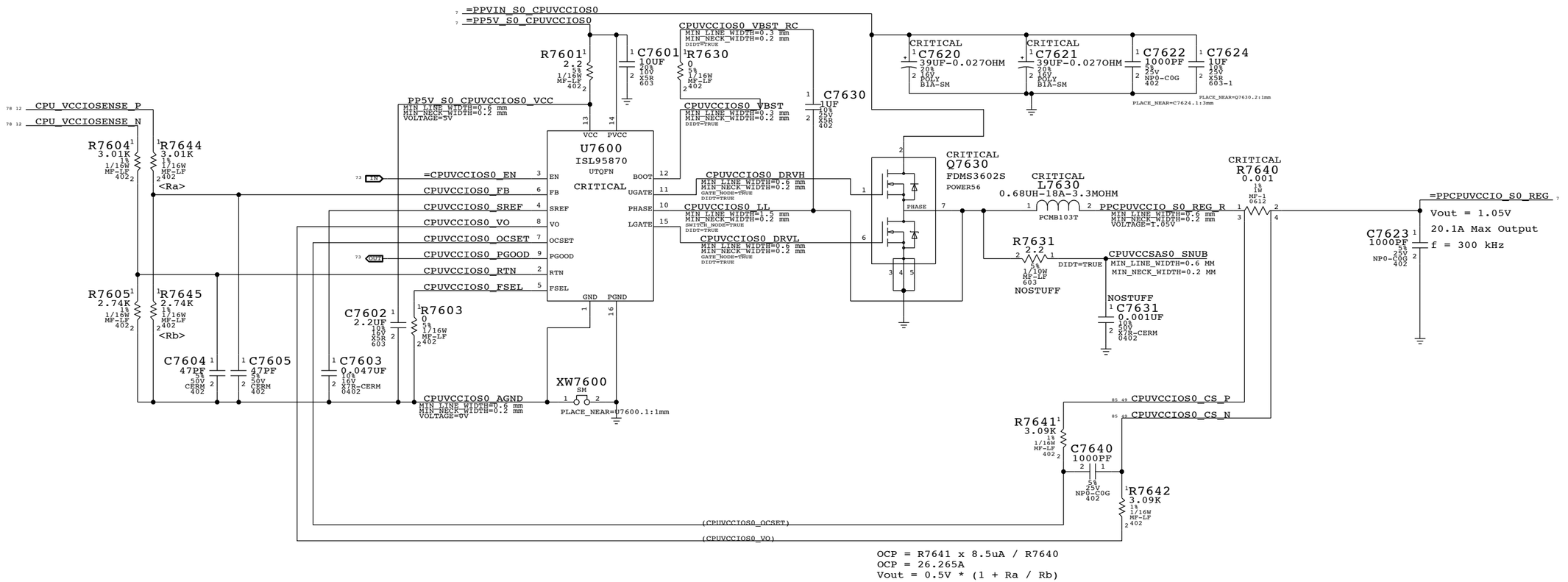
CPU VCCIO (1.05V S0) Regulator



SYNC MASTER=JACK J30	SYNC DATE=09/28/2011
PAGE TITLE	CPUVCCIO (1.05V) Power Supply
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
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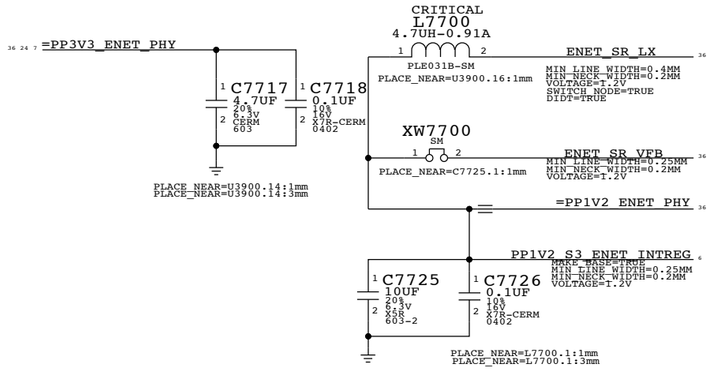
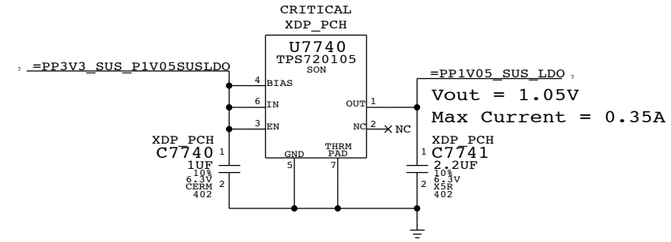
CAESAR IV 1.2V INT.VR CMPTS

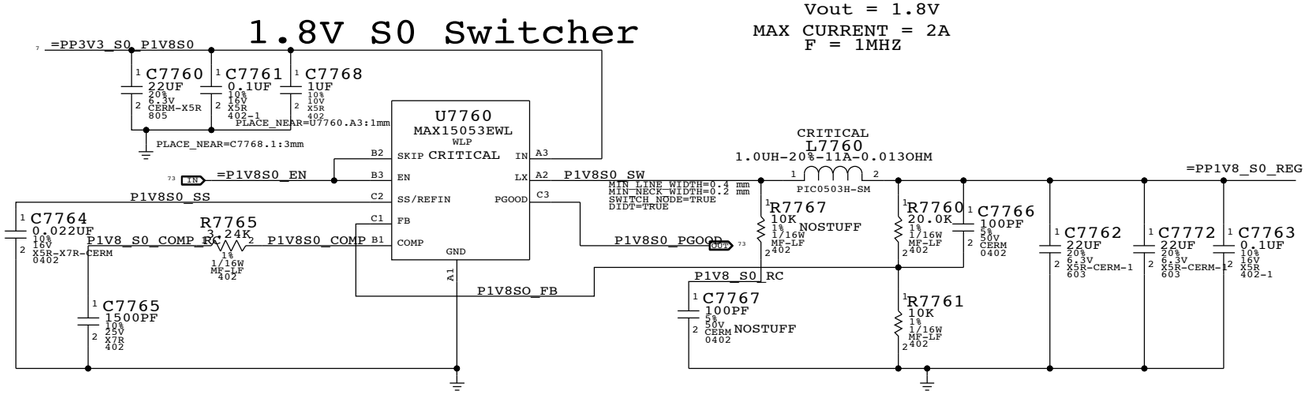


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

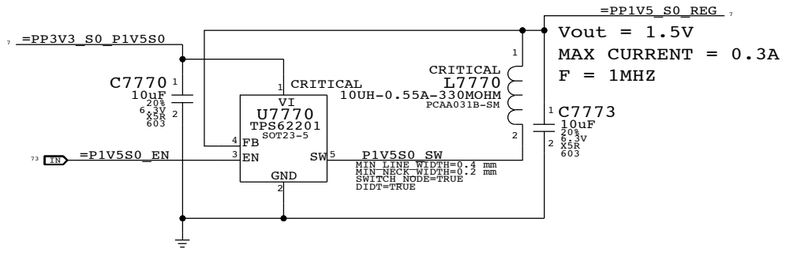


1.8V S0 Switcher

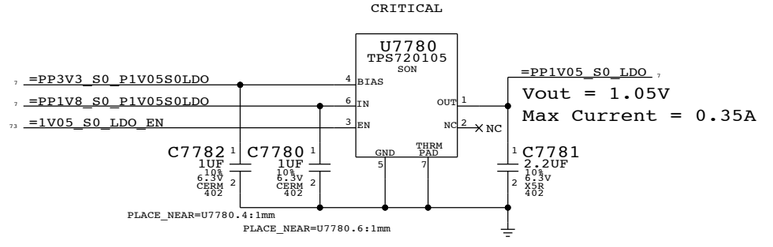


Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ

1.5V S0 Switcher



1.05V S0 LDO



SYNC_MASTER=JACK J30 SYNC_DATE=07/28/2011

PAGE TITLE
Misc Power Supplies

Apple Inc.

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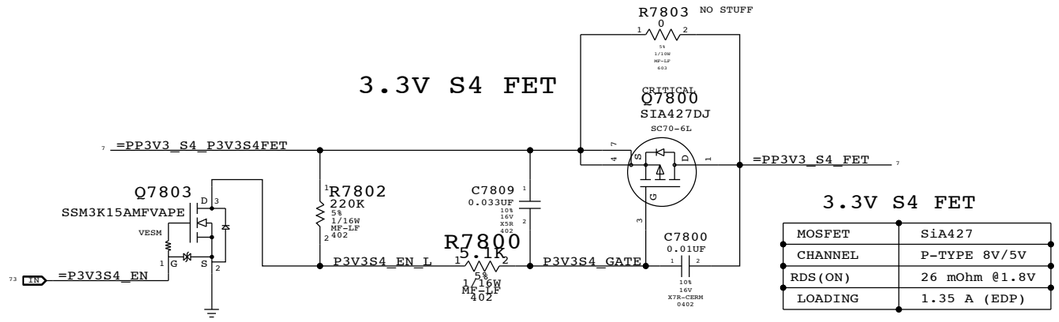
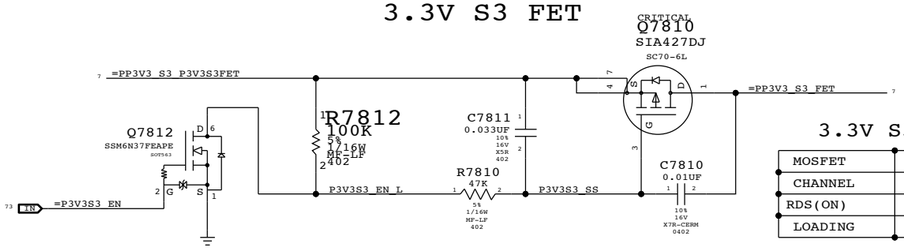
3.3V S4 FET



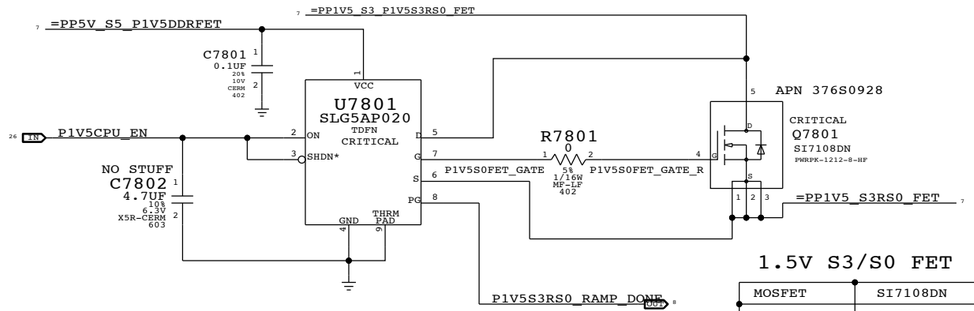
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)

3.3V S3 FET



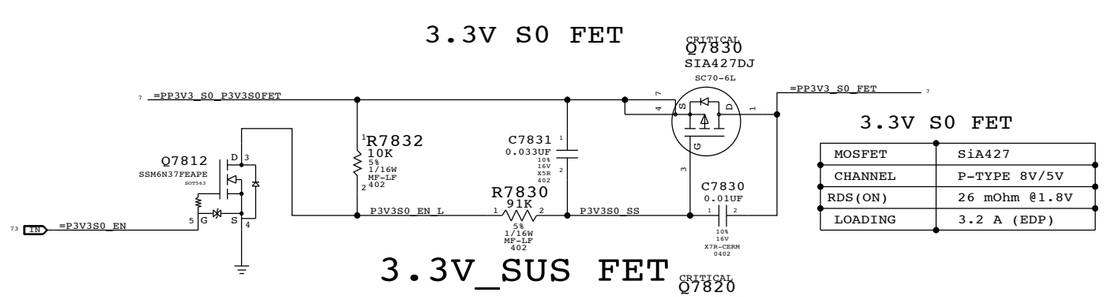
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET



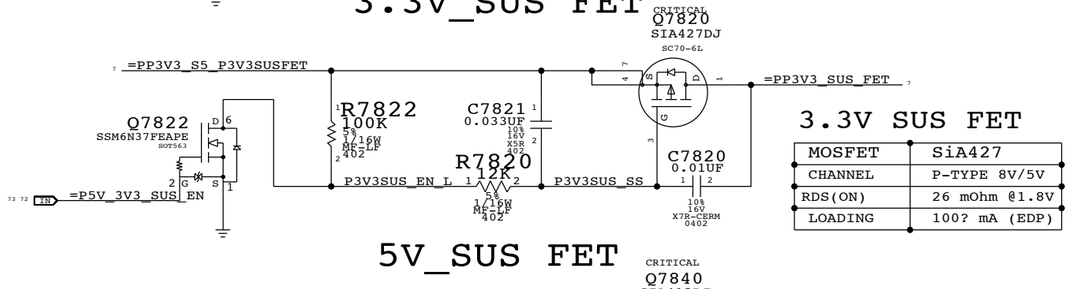
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET



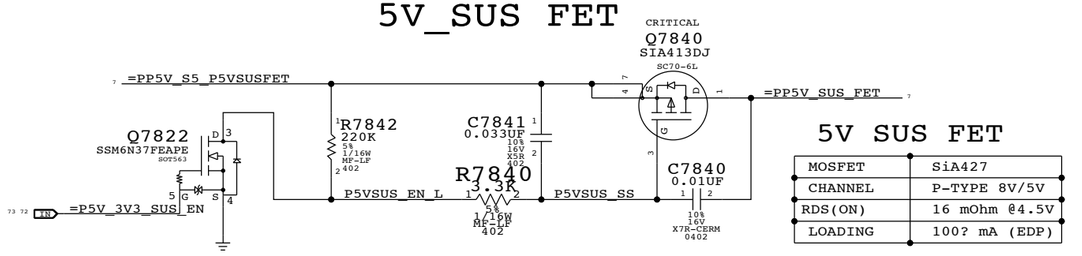
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



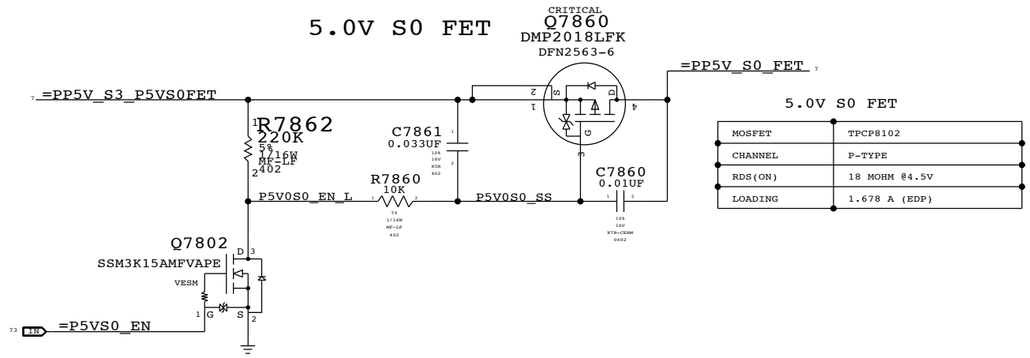
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K90I MLB SYNC DATE=02/15/2011

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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S5 Rail Enables & PGOOD

=PP3V42_G3H_PWRCTL

Internal pull-ups 100K +/- 20%

C7940 0.1uF 20% 10V CERM 402

U7941 SLG4AP012 TDFN — CRITICAL — VDD 343S0497

SMC_PM_G2_EN — MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 5% 25V C0G-CERM 0402

R7941 100 5% 1/16W MF-LF 402

C7942 0.033UF 10% 16V X5R 402 — NO STUFF

P3V3S5_EN_L — MAKE_BASE=TRUE

=P3V3S5_EN_L

P3V3S5_EN_L_R — MAKE_BASE=TRUE

P5V3V3_REG_EN — MAKE_BASE=TRUE

=P5V3V3_REG_EN

S5_PWRGD — MAKE_BASE=TRUE

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V S4 ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7970.6:3mm

C7970 0.1UF 10% 10V X5R-CERM 0201

PM_SLP_S5_L

U7970 74LVC1G32 SOT891

P3V3_S4_EN — MAKE_BASE=TRUE

=P3V3S4_EN

=TBTAPWRSW_EN

SMC_S4_WAKESRC_EN

NO STUFF R7919 0 5% 1/16W MF-LF 402

R7978 100 5% 1/16W MF-LF 402 — PM_SLP_S3_L

PLACE_NEAR=U1800.G18:5mm

3.3V,5V S3 ENABLE

=PP3V42_G3H_PWRCTL

R7913 68K 5% 1/16W MF-LF 402 — P5VS3_EN_L — MAKE_BASE=TRUE — =P5VS3_EN_L

C7913 0.068UF 10% 10V X5R-CERM 0402 — NO STUFF

R7914 3.3K 5% 1/16W MF-LF 402 — TPAD_VBUS_EN

PM_SLP_S4_L — MAKE_BASE=TRUE

R7911 5.1K 5% 1/16W MF-LF 402

R7912 9.1K 5% 1/16W MF-LF 402

PLACE_NEAR=U5701.3:6mm

PLACE_NEAR=Q7812.2:6mm

Q7911 SSM3K15AMFVAPE VESM

PLACE_NEAR=U7300.16:6mm

P3V3S3_EN — MAKE_BASE=TRUE — =P3V3S3_EN

DDRREG_EN — MAKE_BASE=TRUE — =DDRREG_EN

=USB_PWR_EN

C7910 0.47UF 10% 6.3V CERM-X5R 402

C7912 0.47UF 10% 6.3V CERM-X5R 402

PLACE_NEAR=U7300.16:6mm

PLACE_NEAR=Q7812.2:6mm

CPUVCORE ENABLE

ALL_SYS_PWRGD

R7974 0 5% 1/16W MF-LF 402

PLACE_NEAR=U7400.7:5mm

CPUIMVP_VR_ON

S0 ENABLE

PM_SLP_S3_L

R7987 33K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7100.15:6mm

R7981 20K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7600.3:6mm

R7988 39K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7770.3:6mm

R7986 5.1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7760.B3:6mm

(PM_SLP_S3_R_L)

PM_SLP_S3_R_L — MAKE_BASE=TRUE

=P5V5_EN

=P3V3S0_EN

=PBUSVSENS_EN

P1V8S0_EN — MAKE_BASE=TRUE — =P1V8S0_EN

P1V5S0_EN — MAKE_BASE=TRUE — =P1V5S0_EN

=1V05_S0_LDO_EN

CPUVCCIOS0_EN — MAKE_BASE=TRUE — =CPUVCCIOS0_EN

PVCCSA_EN — MAKE_BASE=TRUE — =PVCCSA_EN

C7987 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7100.15:6mm

C7981 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7600.3:6mm

C7988 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7770.3:6mm

C7986 0.47UF 10% 6.3V CERM-X5R 402 — PLACE_NEAR=U7760.B3:6mm

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.1:2.3mm

C7943 0.1uF 20% 10V CERM 402

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L

U7940 74AUP1G32GS SOT891

ALL_SYS_PWRGD

PM_SLP_SUS_L

PM_SUS_EN — MAKE_BASE=TRUE — =P5V_3V3_SUS_EN

NO STUFF R7917 0 5% 1/16W MF-LF 402

=PP3V42_G3H_PWRCTL

R7931 10K 5% 1/16W MF-LF 402

CHGR_VFRQ

Q7931 SSM3K15AMFVAPE VESM

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

CHGR VFRQ Generation

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON

R7951 15.0K 1% 1/16W MF-LF 402

R7952 7.15K 1% 1/16W MF-LF 402

=PP3V3_S5_VMON

R7956 150K 1% 1/16W MF-LF 402

S0PGD_C

VMON_3V3_DIV

R7953 1K 5% 1/16W MF-LF 402

VMON_Q2_BASE

R7954 1K 5% 1/16W MF-LF 402

=PP1V5_S0_VMON — PP1V5_S0

VMON_Q3_BASE

R7955 1K 5% 1/16W MF-LF 402

=PP1V05_S0_VMON

VMON_Q4_BASE

Q7950 ASMCC0179 DFN2015H4-8 — CRITICAL

NC

353S2809

S0PGD_BJT_GND_R

R7957 100 5% 1/16W MF-LF 402

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V SUS Detect

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7930.6:2.3mm

No stuff C7931, 12ms Min delay time

U7930 Sense input threhold is 3.07V

C7930 0.1uF 20% 10V CERM 402

=PP3V3_SUS_PWRCTL

R7933 100K 5% 1/16W MF-LF 402

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 — VDD SENSE RESET* CT GND MR* (90K TYP)

PM_RSMRST_L

PM_RSMRST_L goes to U1800.C21

S4_PGOOD_CT

C7931 0.001UF 10% 25V CERM 402 — NO STUFF

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

3.3V ENET FET

CRITICAL Q7922 NTR4101P SOT-23-HF

=PP3V3_S3_P3V3ENETFET

R7921 10K 5% 1/16W MF-LF 402

C7921 0.033UF 10% 16V X5R 402

R7922 100K 5% 1/16W MF-LF 402

P3V3ENET_SS

C7922 0.01UF 10% 16V X7R-CERM 0402

=PP3V3_ENET_FET

PM_ENET_EN_L

Q7925 2N7002DW-X-G SOT-363

WOL_EN

Q7921 SSM3K15AMFVAPE VESM

PM_SLP_S3_L

Q7920 2N7002DW-X-G SOT-363

AC_EN_L

(AC_EN_L)

R7929 0 5% 1/16W MF-LF 402 — NO STUFF

SMC_ADAPTER_EN

(PM_SLP_S3_L)

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L

Q7925 2N7002DW-X-G SOT-363

AP_PWR_EN

S0 Rail PGOOD Circuitry

Thresholds: (ISL Version in development)

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

=PP3V3_S0_PWRCTL

R7967 10K 5% 1/16W MF-LF 402

NO STUFF R7968 100 5% 1/16W MF-LF 402

P1V5S0_PGOOD from U7710

R7966 100 5% 1/16W MF-LF 402

R7965 100 5% 1/16W MF-LF 402

R7964 100 5% 1/16W MF-LF 402

R7963 100 5% 1/16W MF-LF 402

=PP3V3_S0_VMON

=PP5V_S0_VMON

=PP1V5_S0_VMON

=PP1V05_S0_VMON

S0PGOOD_ISL

R7960 6.04K 1% 1/16W MF-LF 402

R7970 10K 1% 1/16W MF-LF 402

R7972 6.04K 1% 1/16W MF-LF 402

C7960 0.1uF 20% 10V CERM 402

U7960 ISL88042IRTEZ TDFN (TPU) CRITICAL — VDD V2MON V3MON V4MON RST* NC

P5V_DIV_VMON

P1V5_DIV_VMON

P1V05_DIV_VMON

R7961 15.0K 1% 1/16W MF-LF 402

R7971 10K 1% 1/16W MF-LF 402

R7973 15.0K 1% 1/16W MF-LF 402

GND THRM_PAD

353S2310

ALL_SYS_PWRGD_R

R7962 330 5% 1/16W MF-LF 402

S0PGOOD_ISL

ALL_SYS_PWRGD

CPUIMVP_AXG_PGOOD

P1V8S0_PGOOD

P5V3V3_PGOOD

CPUVCCIOS0_PGOOD

PVCCSA_PGOOD

SYNC_MASTER=K90I_MLB — SYNC_DATE=02/15/2011

PAGE TITLE

Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER 051-9058 — SIZE D

REVISION 6.0.0

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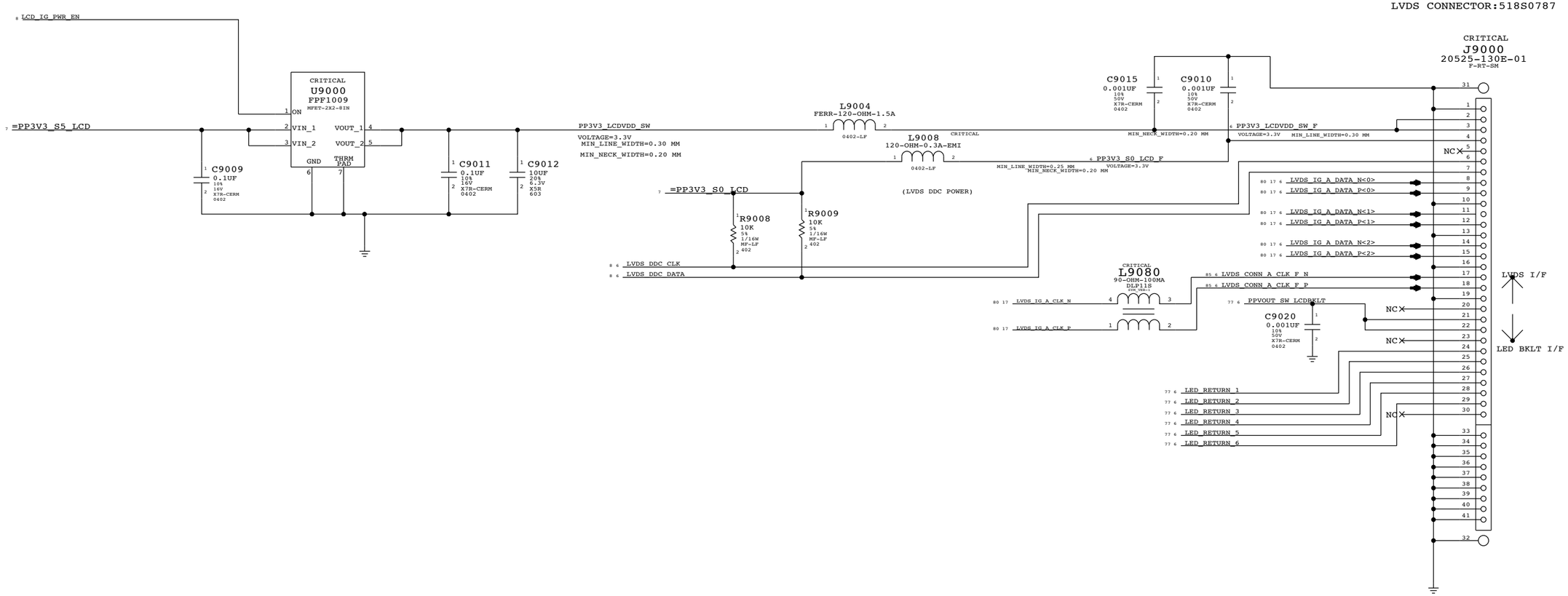
LCD CONNECTOR

LVDS CONNECTOR:518S0787



SYNC MASTER=K90I MLB — SYNC DATE=02/15/2011

PAGE TITLE: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-9058 — SIZE: D

REVISION: 6.0.0

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T29 A High-Speed Signals

DP_EXTA_ML_C_P<0> C9300 0.1UF DP_EXTA_ML_P<0>
DP_EXTA_ML_C_N<0> C9301 0.1UF DP_EXTA_ML_N<0>
DP_EXTA_ML_C_P<1> C9302 0.1UF DP_EXTA_ML_P<1>
DP_EXTA_ML_C_N<1> C9303 0.1UF DP_EXTA_ML_N<1>
DP_EXTA_ML_C_P<2> C9304 0.1UF DP_EXTA_ML_P<2>
DP_EXTA_ML_C_N<2> C9305 0.1UF DP_EXTA_ML_N<2>
DP_EXTA_ML_C_P<3> C9306 0.1UF DP_EXTA_ML_P<3>
DP_EXTA_ML_C_N<3> C9307 0.1UF DP_EXTA_ML_N<3>
DP_EXTA_AUXCH_C_P C9308 0.1UF DP_EXTA_AUXCH_P
DP_EXTA_AUXCH_C_N C9309 0.1UF DP_EXTA_AUXCH_N

R9309 1M =PP3V3_S0_DPSDRVA
R9308 1M

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29 signals are P/N-swapped after AC caps to improve layout.

T29_D2R_N<0> T29_D2R_P<0>
T29_R2D_C_N<0> T29_R2D_C_P<0>
T29_D2R_N<1> T29_D2R_P<1>
T29_R2D_C_N<1> T29_R2D_C_P<1>

T29_A_BIAS_R2DP0 T29_A_BIAS_R2DN0 GND_VOID=TRUE (C9370/C9371)
C9370 0.47UF
C9371 0.47UF
C9372 0.47UF
C9373 0.47UF

T29 Path Biasing

R9372 1.5K R9373 1.5K

T29_A_BIAS_R2DP1 T29_A_BIAS_R2DN1 GND_VOID=TRUE (C9380/C9381)
C9380 0.47UF
C9381 0.47UF
C9382 0.47UF
C9383 0.47UF

R9382 1.5K R9383 1.5K

D9364 D9372 D9373 D9365 BAR90-02LRH TSLP-2-7

CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY

T29: TX_0
T29DPA_ML_C_P<0> T29DPA_ML_C_N<0>
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)

R9374 1.5K R9375 1.5K

T29_D2R_C_P<0> T29_D2R_C_N<0>
T29_D2R_C_P<1> T29_D2R_C_N<1>

D9360 D9382 D9383 D9361 BAR90-02LRH TSLP-2-7

CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)

GND_VOID=TRUE (D9360.2)
T29: TX_1
T29DPA_ML_C_P<2> T29DPA_ML_C_N<2>
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)

R9384 1.5K R9385 1.5K

Both R's must connect to C in star topology.

DP A Super-Driver

=PP3V3_S0_DPSDRVA

C9310 2.2UF C9311 0.1UF C9312 0.1UF

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K R9310 1K
R9312 1K

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP_EXTA_ML_P<0>	1 IN_D0P	OUT_D0P 30	DP_SDRVA_ML_C_P<0>
DP_EXTA_ML_N<0>	2 IN_D0N	OUT_D0N 29	DP_SDRVA_ML_C_N<0>
DP_EXTA_ML_P<1>	4 IN_D1P	OUT_D1P 28	DP_SDRVA_ML_C_P<1>
DP_EXTA_ML_N<1>	5 IN_D1N	OUT_D1N 27	DP_SDRVA_ML_C_N<1>
DP_EXTA_ML_P<2>	7 IN_D2P	OUT_D2P 25	DP_SDRVA_ML_C_P<2>
DP_EXTA_ML_N<2>	8 IN_D2N	OUT_D2N 24	DP_SDRVA_ML_C_N<2>
DP_EXTA_ML_P<3>	9 IN_D3P	OUT_D3P 23	DP_SDRVA_ML_C_P<3>
DP_EXTA_ML_N<3>	10 IN_D3N	OUT_D3N 22	DP_SDRVA_ML_C_N<3>
DP_EXTA_DDC_CLK	14 IN_SCL	AC_AUXP 20	DP_SDRVA_AUXCH_C_P
DP_EXTA_DDC_DATA	13 IN_SDA	AC_AUXN 19	DP_SDRVA_AUXCH_C_N
DP_EXTA_AUXCH_P	16 IN_AUXP	OUT_AUXP_SCL 18	(DP_SDRVA_AUXCH_P)
DP_EXTA_AUXCH_N	15 IN_AUXN	OUT_AUXN_SDA 17	(DP_SDRVA_AUXCH_N)
DP_EXTA_HPD	3 IN_HPD	(IPD) OUT_HPD 31	(DP_SDRVA_HPD)
DPSDRVA_I2C_CTL_EN	26 I2C_CTL_EN (IPU)	CA_DET 32	DP_A_CA_DET
DPSDRVA_I2C_ADDR0	36 I2C_ADDR0 (IPD)	CEXT 11	DPSDRVA_CEXT
DPSDRVA_I2C_ADDR1	35 I2C_ADDR1 (IPD)		
=I2C_DPSDRVA_SCL	38 SCL_CTL		
=I2C_DPSDRVA_SDA	37 SDA_CTL		
DPSDRVA_REXT	12 REXT		
DP_AUXCH_ISOL	39 AUXDDC_OFF (IPD)		
DP_A_PWRDWN_R	34 PD (IPD)		

C9363 0.1UF C9362 0.1UF
C9367 0.1UF C9366 0.1UF
C9369 0.1UF C9368 0.1UF

AUXCH Snoop Port, used by PS8301 during training.

C9319 2.2UF

SDRV_PD R9318 0 R9319 4.22K

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9354 30 R9355 30 R9350 30 R9351 30

DP_SDRVA_ML_R_P<0>	C9364 0.22UF	DP_SDRVA_ML_P<0>	
DP_SDRVA_ML_R_N<0>	C9365 0.22UF	DP_SDRVA_ML_N<0>	
DP_SDRVA_ML_R_P<2>	C9360 0.22UF	DP_SDRVA_ML_P<2>	
DP_SDRVA_ML_R_N<2>	C9361 0.22UF	DP_SDRVA_ML_N<2>	

R9352 270 R9353 270

=PP3V3_S0_DPSDRVA
C9359 0.1UF
DP_A_PWRDWN
CRITICAL U9359 74LVC1G04DBVCK SC70
DP_A_BIAS

IC supports input high while Vcc = 0V.

DP Path Biasing

R9361 1.5K R9360 1.5K R9365 1.5K R9364 1.5K

DP_A_BIAS0 VOLTAGE=3.3V
DP_A_BIAS2 VOLTAGE=3.3V
R9363 51 R9362 51
C9358 0.1UF

DP/T29 A Low-Speed MUX

PP3V3_SW_TBTAPWR
Must be 3.3V DP A port power

C9390 0.1UF C9391 0.1UF

OMIT_TABLE
U9390 CBTL04DP081 HVQFN
R9399 100K

DP_SDRVA_ML_N<3>	31 DIN1_0+	DOUT_0+ 1	T29DPA_ML_N<3>
DP_SDRVA_ML_P<3>	30 DIN1_0-	DOUT_0- 2	T29DPA_ML_P<3>
DP_SDRVA_ML_N<1>	27 DIN1_1+	DOUT_1+ 4	T29DPA_ML_N<1>
DP_SDRVA_ML_P<1>	26 DIN1_1-	DOUT_1- 5	T29DPA_ML_P<1>
DP_SDRVA_AUXCH_P	19 AUX1+	AUX+ 6	DP_A_EXT_AUXCH_P
DP_SDRVA_AUXCH_N	18 AUX1-	AUX- 7	DP_A_EXT_AUXCH_N
DP_SDRVA_HPD	17 HPD_1	HPD_IN 8	DP_A_EXT_HPD
T29_A_RSVD_N	25 DIN2_0+		
T29_A_RSVD_P	24 DIN2_0-		
(T29_A_LSX_P2R)	23 DIN2_1+		
(T29_A_LSX_R2P)	22 DIN2_1-		
T29_D2R1_BIASP	15 AUX2+		
T29_D2R1_BIASN	14 AUX2-		
	13 HPD_2		
DP_A_PWRDWN	10 GPU_SEL		
T29_A_BIAS	32 AUX_SEL		
	11 NC		

CKPLUS_WAIVE=NdifPr_badTerm
CRITICAL
T29: Unused
T29: LSX_A_R2P/P2R (P/N)
T29: RX_1 Bias Sink
LO=Port A HI=Port B
THMPAD GND
SIGNAL_MODEL=T29DP_MUX

R9396 1K R9397 1K

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

R9392 51 R9393 51

Port A MCU

PP3V3_SW_TBTAPWR Must be 3.3V DP A port power

C9330 0.1UF C9331 0.1UF

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP_A_CA_DET	1 RESET#/PIO0_0	R/PIO1_0/AD1 16	T29DPA_CONFIG1_RC
	2 PIO0_1/CLKOUT	R/PIO1_1/AD2 17	T29DPA_CONFIG2_RC
T29_LSEO<0>	7 PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18	TBT_A_HV_EN_R
=I2C_T29AMCU_SCL	8 PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19	T29_A_UC_ADDR
=I2C_T29AMCU_SDA	9 PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20	DP_A_EXT_HPD
T29DPA_HPD	10 PIO0_6/SCK	PIO1_6/RXD 23	T29_A_LSX_P2R
T29_A_BIAS_R	11 PIO0_7/CTS#	PIO1_7/TXD 24	T29_A_LSX_R2P
T29_LSOE<0>	12 PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6	T29_LSEO<1>
T29_LSOE<1>	13 PIO0_9/MOSI/CT16B0_MAT1		
TBT_PWR_REQ_L	14 SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
	15 R/PIO0_11/AD0 (OD)	XTALIN 4	
	VSS 3 21	THRM PAD 25	

R9338 10K R9334 10K TBT_A_HV_EN

P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr: 0x26/0x27 (Wr/Rd)

R9339 1M

R9335 1K R9336 10K

=TBT_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=TBT_WAKE_L OMIT R9330 0 SWCLK SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

R9398 100K

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC_MASTER=K90I MLB	SYNC_DATE=02/15/2011
PAGE TITLE	DisplayPort/T29 A MUXing
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
	REVISION 6.0.0
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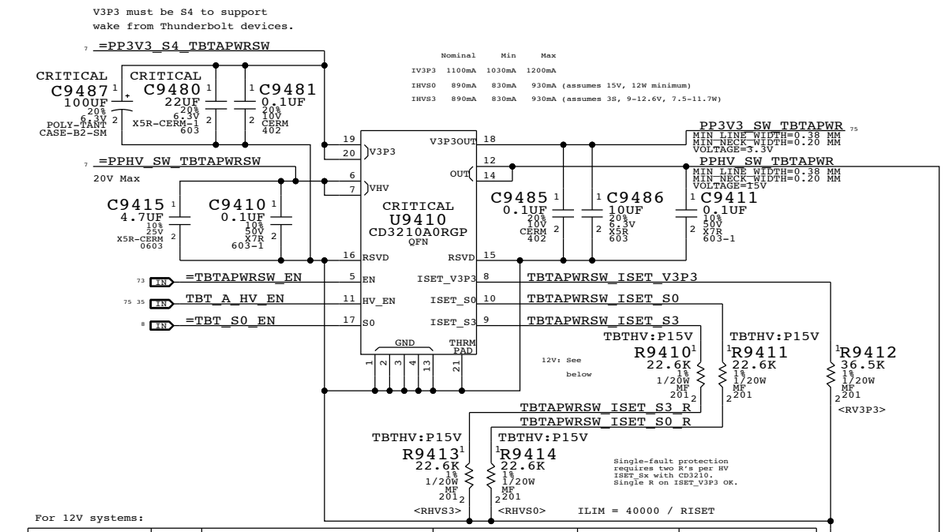
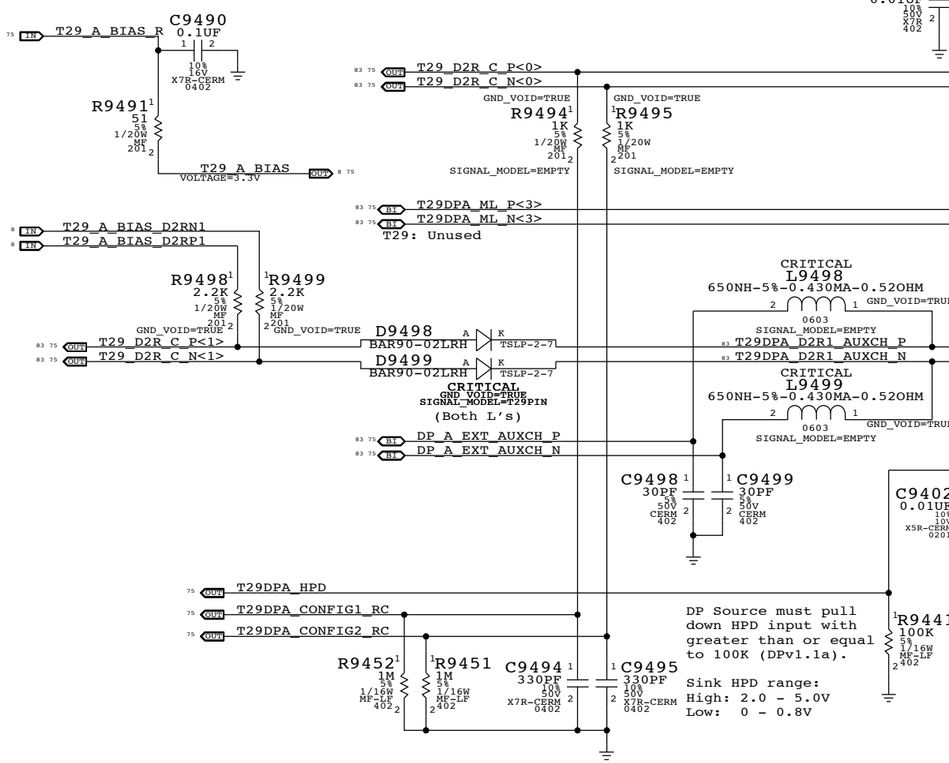
3.3V/HV Power MUX



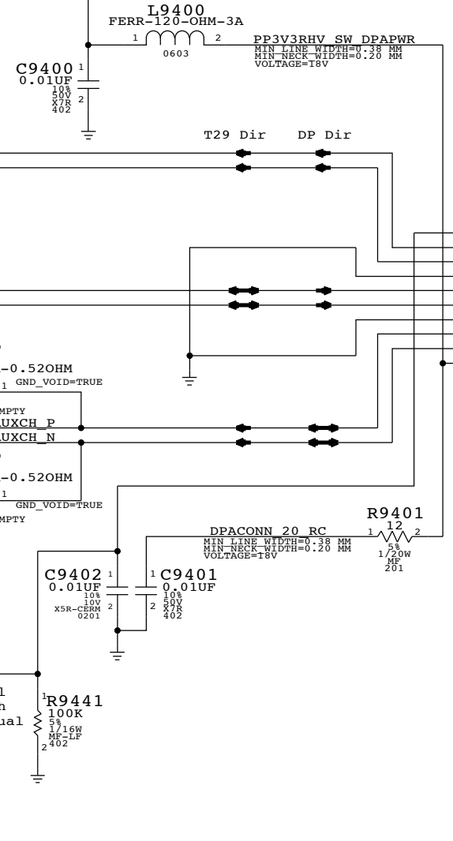
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)



Thunderbolt Connector A



SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

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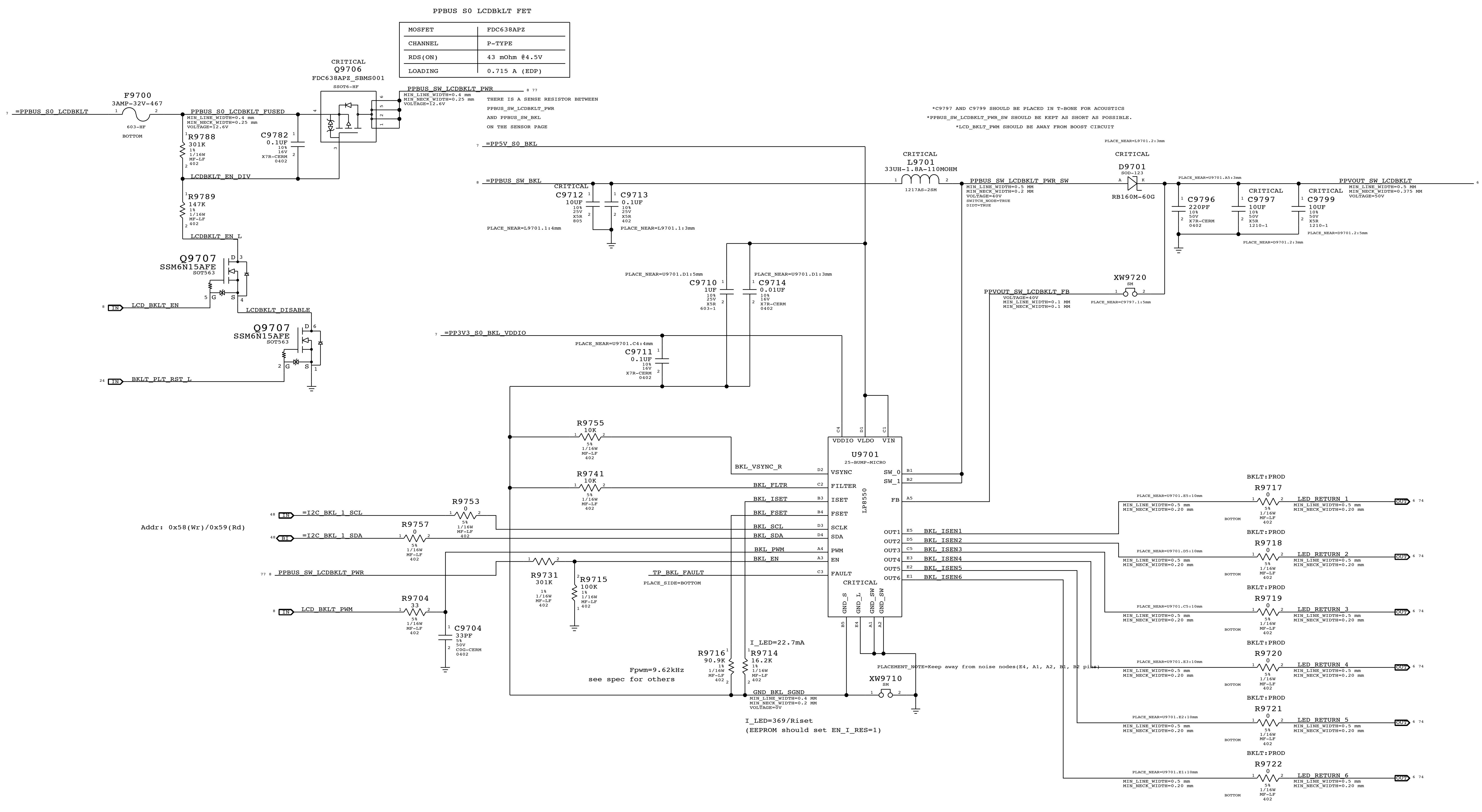
PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)



=PPBUS_S0_LCDBKLT
F9700
3AMP-32V-467
603-HF
BOTTOM
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL
Q9706
FDC638APZ_SBMS001
SSOT6-HF
PPBUS_SW_LCDBKLT_PWR
THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE
R9788
301K
C9782
0.1UF
LCDBKLT_EN_DIV
R9789
147K
LCDBKLT_EN_L
Q9707
SSM6N15AFE
SOT563
LCD_BKLT_EN
LCDBKLT_DISABLE
BKLT_PLT_RST_L
=PP5V_S0_BKL
=PPBUS_SW_BKL
C9712
10UF
C9713
0.1UF
PLACE_NEAR=L9701.1:4mm
PLACE_NEAR=L9701.1:3mm
CRITICAL
L9701
33UH-1.8A-110MOHM
1217AS-2SM
PPBUS_SW_LCDBKLT_PWR_SW
CRITICAL
D9701
SOD-123
RB160M-60G
*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT
PPVOUT_SW_LCDBKLT
C9796
220PF
C9797
10UF
C9799
10UF
XW9720
PPVOUT_SW_LCDBKLT_FB
PLACE_NEAR=U9701.D1:5mm
PLACE_NEAR=U9701.D1:3mm
C9710
1UF
C9714
0.01UF
=PP3V3_S0_BKL_VDDIO
PLACE_NEAR=U9701.C4:4mm
C9711
0.1UF
R9755
10K
R9741
10K
BKL_VSYNC_R
BKL_FLTR
R9753
0
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA
R9757
0
Addr: 0x58(Wr)/0x59(Rd)
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
PPBUS_SW_LCDBKLT_PWR
R9731
301K
R9715
100K
TP_BKL_FAULT
PLACE_SIDE=BOTTOM
R9704
33
LCD_BKLT_PWM
C9704
33PF
U9701
25-BUMP-MICRO
LP8550
VDDIO VLDO VIN
VSYNC
FILTER
ISET
FSET
SCLK
SDA
PWM
EN
FAULT
SW_0
SW_1
FB
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
CRITICAL
GND_S
GND_L
GND_SW
GND_SW
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
I_LED=22.7mA
R9716
90.9K
R9714
16.2K
Fpwm=9.62kHz
see spec for others
GND_BKL_SGND
XW9710
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)
BKLT:PROD
R9717
LED_RETURN_1
R9718
LED_RETURN_2
R9719
LED_RETURN_3
R9720
LED_RETURN_4
R9721
LED_RETURN_5
R9722
LED_RETURN_6

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J31_MLB SYNC_DATE=07/08/2011

PAGE TITLE

LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_PCH_TX2TX	*	=3X_DIELECTRIC	?
PCIE_PCH_TX2RX	*	=4X_DIELECTRIC	?
PCIE_PCH_RX2RX	*	=3x_DIELECTRIC	?
PCIE_PCH_RX2TX	*	=4x_DIELECTRIC	?
PCIE_PCH_2OTHER	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_PCH_TX2TX	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_PCH_TX2RX	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_PCH_RX2RX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_RX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	*_PCH_TX	*	PCIE_PCH_TX2TX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_PCH_TX2RX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_PCH_RX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_PCH_RX2TX
PCIE_PCH_TX	*	*	PCIE_PCH_2OTHER
PCIE_PCH_RX	*	*	PCIE_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	CPU_COMP	CPU_PECI	10 19 46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 24
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10 45
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_RMTL	PM_THRMTRIP_L	10 19 46
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 68
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines
per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 28

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_PCH	*	=3x_DIELECTRIC	?
DP_PCH_TX	*	=3x_DIELECTRIC	?
LVDS_PCH_TX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_PCH	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_PCH_TX	*	=3x_DIELECTRIC	?
SATA_PCH_RX	*	=3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_PCH_RX	TOP,BOTTOM	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_PCH_TX2TX	*	=4X_DIELECTRIC	?
SATA3_PCH_TX2RX	*	=5X_DIELECTRIC	?
SATA3_PCH_RX2RX	*	=4x_DIELECTRIC	?
SATA3_PCH_RX2TX	*	=5x_DIELECTRIC	?
SATA3_PCH_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_PCH_TX2TX	TOP,BOTTOM	=5X_DIELECTRIC	?
SATA3_PCH_TX2RX	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA3_PCH_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_PCH_RX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_PCH_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	*_PCH_TX	*	SATA3_PCH_TX2TX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_PCH_TX2RX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_PCH_RX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_PCH_RX2TX
SATA3_PCH_TX	*	*	SATA3_PCH_2OTHER
SATA3_PCH_RX	*	*	SATA3_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX2TX	*	=4X_DIELECTRIC	?
USB3_PCH_TX2RX	*	=5X_DIELECTRIC	?
USB3_PCH_RX2RX	*	=4x_DIELECTRIC	?
USB3_PCH_RX2TX	*	=5x_DIELECTRIC	?
USB3_PCH_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX2TX	TOP,BOTTOM	=5X_DIELECTRIC	?
USB3_PCH_TX2RX	TOP,BOTTOM	=6X_DIELECTRIC	?
USB3_PCH_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	*_PCH_TX	*	USB3_PCH_TX2TX
USB3_PCH_TX	*_PCH_RX	*	USB3_PCH_TX2RX
USB3_PCH_RX	*_PCH_RX	*	USB3_PCH_RX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_PCH_RX2TX
USB3_PCH_TX	*	*	USB3_PCH_2OTHER
USB3_PCH_RX	*	*	USB3_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_IG_A_CLK	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_CLK_P	17 74
LVDS_IG_A_CLK	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_CLK_N	17 74
LVDS_IG_A_DATA	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_P<2..0>	6 17 74
LVDS_IG_A_DATA	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_N<2..0>	6 17 74
	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_P<3>	8 17
	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_N<3>	8 17
	LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_DATA_P<3..0>	8 17
	LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_DATA_N<3..0>	8 17
	LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_CLK_P	8 17
	LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_CLK_N	8 17
SATA_HDD_R2D	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 41
SATA_HDD_R2D	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_P	6 41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_N	6 41
SATA_HDD_D2R	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 41
SATA_HDD_D2R	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_C_P	6 41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_C_N	6 41
SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_C_P	16 41
SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_C_N	16 41
SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_P	6 41
SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_N	6 41
SATA_ODD_D2R	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_P	16 41
SATA_ODD_D2R	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_N	16 41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RC_P	41
SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RC_N	41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RC_P	41
SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RC_N	41
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB_UP_P	18 25
	USB_85D	USB	USB_HUB_UP_N	18 25
USB_EXTA	USB_85D	USB	USB_EXTA_P	18 42
USB_EXTA	USB_85D	USB	USB_EXTA_N	18 42
USB_EXTB	USB_85D	USB	USB_EXTB_MUX_P	25 43
	USB_85D	USB	USB_EXTB_MUX_N	25 43
	USB_85D	USB	USB_EXTA_MUXED_F_P	42
	USB_85D	USB	USB_EXTA_MUXED_F_N	42
	USB_85D	USB	USB_EXTB_F_P	43
	USB_85D	USB	USB_EXTB_F_N	43
	USB_85D	USB	USB_EXTA_MUXED_P	42
	USB_85D	USB	USB_EXTA_MUXED_N	42
	USB_85D	USB	USB_EXTD_XHCI_P	8 18
	USB_85D	USB	USB_EXTD_XHCI_N	8 18
	USB_85D	USB	USB_EXTB_EHCI_P	18 25
	USB_85D	USB	USB_EXTB_EHCI_N	18 25
	USB_85D	USB	USB_EXTB_XHCI_P	18 25
	USB_85D	USB	USB_EXTB_XHCI_N	18 25
USB3_EXT_RX	USB_85D	USB3_PCH_RX	USB3_EXTA_RX_P	18 42
	USB_85D	USB3_PCH_RX	USB3_EXTA_RX_N	18 42
USB3_EXT_TX	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_P	18 42
	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_N	18 42
USB3_EXT_RX	USB_85D	USB3_PCH_RX	USB3_EXTB_RX_P	18 43
	USB_85D	USB3_PCH_RX	USB3_EXTB_RX_N	18 43
USB3_EXT_TX	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_P	18 43
	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_N	18 43
	USB_85D	USB3_PCH_RX	USB3_EXTA_RX_F_P	42
	USB_85D	USB3_PCH_RX	USB3_EXTA_RX_F_N	42
	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_F_P	42
	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_F_N	42
	USB_85D	USB3_PCH_RX	USB3_EXTB_RX_F_P	43
	USB_85D	USB3_PCH_RX	USB3_EXTB_RX_F_N	43
	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_F_P	43
	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_F_N	43
	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_C_P	42
	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_C_N	42
	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_C_P	43
	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_C_N	43
USB_EXTA	USB_85D	USB	USB_SMC_P	8 45
	USB_85D	USB	USB_SMC_N	8 45
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 18
	USB_85D	USB	USB_EXTC_N	8 18
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	18 32
	USB_85D	USB	USB_CAMERA_N	18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 32
	USB_85D	USB	USB_CAMERA_CONN_N	6 32
USB_BT	USB_85D	USB	USB_BT_P	8 32
USB_BT	USB_85D	USB	USB_BT_N	8 32
USB_BT	USB_85D	USB	USB_BT_CONN_P	6 32
USB_BT	USB_85D	USB	USB_BT_CONN_N	6 32
USB_TPAD	USB_85D	USB	USB_TPAD_P	8 53
	USB_85D	USB	USB_TPAD_N	8 53
USB_IR	USB_85D	USB	USB_IR_P	8 44
	USB_85D	USB	USB_IR_N	8 44
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 24

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

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PCH Constraints 1

Apple Inc.

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCI-Express Signal Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	*	=3X_DIELECTRIC	?
PCIE_T29_TX2RX	*	=4X_DIELECTRIC	?
PCIE_T29_RX2RX	*	=3x_DIELECTRIC	?
PCIE_T29_RX2TX	*	=4x_DIELECTRIC	?
PCIE_T29_2OTHER	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_T29_TX2RX	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_T29_RX2RX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_RX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_T29_TX	*_TX	*	PCIE_T29_TX2TX
PCIE_T29_TX	*_RX	*	PCIE_T29_TX2RX
PCIE_T29_RX	*_RX	*	PCIE_T29_RX2RX
PCIE_T29_RX	*_TX	*	PCIE_T29_RX2TX
PCIE_T29_TX	*	*	PCIE_T29_2OTHER
PCIE_T29_RX	*	*	PCIE_T29_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	24
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 24
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	24 45
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 24 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 48
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 48
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16 24
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_50S	SPI	SPI_CLK_R	16 47
	SPI_50S	SPI	SPI_CLK	47
SPI_MOSI	SPI_50S	SPI	SPI_MOSI_R	16 47
	SPI_50S	SPI	SPI_MOSI	47
SPI_MISO	SPI_50S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_50S	SPI	SPI_CS0_R_L	16 47
	SPI_50S	SPI	SPI_CS0_L	47
	SPI_50S	SPI	SPI_MLB_CLK	46 47 56
	SPI_50S	SPI	SPI_MLB_CS_L	46 47 56
	SPI_50S	SPI	SPI_MLB_MOSI	46 47 56
	SPI_50S	SPI	SPI_MLB_MISO	46 47 56
	SPI_50S	SPI	SPI_SMC_MISO	45 46
	SPI_50S	SPI	SPI_SMC_MOSI	45 46
	SPI_50S	SPI	SPI_SMC_CLK	45 46
	SPI_50S	SPI	SPI_SMC_CS_L	45 46
	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_N	16 32
	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_C_N	38
PCIE_AP_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_PI_P	6 32
	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_PI_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE_PCH_RX	PCIE_AP_R2D_PI_P	
	PCIE_85D	PCIE_PCH_RX	PCIE_AP_R2D_PI_N	
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_EXTA_ML	DP_85D	DP_PCH_TX	DP_EXTA_ML_C_P<3..0>	8 75
DP_EXTA_ML	DP_85D	DP_PCH_TX	DP_EXTA_ML_C_N<3..0>	8 75
	DP_85D	DP_PCH_TX	DP_EXTA_ML_P<3..0>	75
	DP_85D	DP_PCH_TX	DP_EXTA_ML_N<3..0>	75
DP_EXTA_AUXCH	DP_85D	DP_PCH	DP_EXTA_AUXCH_C_P	8 75
DP_EXTA_AUXCH	DP_85D	DP_PCH	DP_EXTA_AUXCH_C_N	8 75
	DP_85D	DP_PCH	DP_EXTA_AUXCH_P	75
	DP_85D	DP_PCH	DP_EXTA_AUXCH_N	75
PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_C_P<3..0>	8 33
PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_C_N<3..0>	8 33
PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_P<3..0>	33
PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_N<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_P<3..0>	8 33
PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_N<3..0>	8 33
PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_C_P<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_C_N<3..0>	33
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 24
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 24
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	24 36
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	24 33
	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	33

SYNC MASTER=K90I MLB — SYNC DATE=02/15/2011

PAGE TITLE: PCH Constraints 2

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	30 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	
CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK	
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	30 36
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD	30 36
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK	30 36
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK_L	

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	38 40
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	38 40
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	38 40
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	38 40
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	38 40
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	38 40

Port 2 Not Used

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
E2	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	75
E3	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	75
E4	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	75
E5	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	75
E6		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	
E7		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	
E8	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	75 76
E9	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	75 76
E10	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	75 76
E11	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	75 76
E12		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	76
E13		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	76
E14		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	75
E15		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	75
E16		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	75
E17		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	75
E18	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	75 83
E19	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	75 83
E20	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	75
E21	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	75
E22	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	75
E23	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	75
E24		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	75
E25		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	75
E26		T29DP_80D	T29DP	T29DPA_ML_P<3..0>	75 76
E27		T29DP_80D	T29DP	T29DPA_ML_N<3..0>	75 76
E28		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	75 76
E29		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	75 76
E30		T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	75 76
E31		T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	75 76
E32	T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
E33	T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
E34	T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
E35	T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
E36		T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
E37		T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
E38	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
E39	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
E40	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
E41	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
E42		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
E43		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
E44		T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
E45		T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
E46		T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
E47		T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
E48	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	83
E49	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	83
E50	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
E51	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
E52	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
E53	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
E54		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
E55		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
E56		T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
E57		T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
E58		T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
E59		T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
E60		T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
E61		T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)		
E62		DP_85D	DP_PCH_TX	DP_T29SNK0_ML_C_P<3..0>	8 33
E63		DP_85D	DP_PCH_TX	DP_T29SNK0_ML_C_N<3..0>	8 33
E64	DP_T29SNK0_ML	DP_85D	DP_PCH_TX	DP_T29SNK0_ML_P<3..0>	33
E65	DP_T29SNK0_ML	DP_85D	DP_PCH_TX	DP_T29SNK0_ML_N<3..0>	33
E66		DP_85D	DP_PCH	DP_T29SNK0_AUXCH_C_P	8 33
E67		DP_85D	DP_PCH	DP_T29SNK0_AUXCH_C_N	8 33
E68	DP_T29SNK0_AUXCH	DP_85D	DP_PCH	DP_T29SNK0_AUXCH_P	33
E69	DP_T29SNK0_AUXCH	DP_85D	DP_PCH	DP_T29SNK0_AUXCH_N	33
E70		DP_85D	DP_PCH_TX	DP_T29SNK1_ML_C_P<3..0>	8 33
E71		DP_85D	DP_PCH_TX	DP_T29SNK1_ML_C_N<3..0>	8 33
E72	DP_T29SNK1_ML	DP_85D	DP_PCH_TX	DP_T29SNK1_ML_P<3..0>	33
E73	DP_T29SNK1_ML	DP_85D	DP_PCH_TX	DP_T29SNK1_ML_N<3..0>	33
E74		DP_85D	DP_PCH	DP_T29SNK1_AUXCH_C_P	8 33
E75		DP_85D	DP_PCH	DP_T29SNK1_AUXCH_C_N	8 33
E76	DP_T29SNK1_AUXCH	DP_85D	DP_PCH	DP_T29SNK1_AUXCH_P	33
E77	DP_T29SNK1_AUXCH	DP_85D	DP_PCH	DP_T29SNK1_AUXCH_N	33
E78		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
E79		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
E80		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
E81		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	

Only used on hosts supporting T29 video-in

E82		T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 48
E83		T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 48
E84	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
E85	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
E86	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
E87	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
E88		T29DP_80D	T29DP	T29_R2D_C_P<3..0>	8 33 75
E89		T29DP_80D	T29DP	T29_R2D_C_N<3..0>	8 33 75
E90		T29DP_100D	T29DP	T29_D2R_P<3..0>	8 33 75
E91		T29DP_100D	T29DP	T29_D2R_N<3..0>	8 33 75

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	6 45 48
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	6 45 48
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	45 48
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	45 48
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	45 48
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	45 48
SMBUS_SMC_RSA_SCL	SMB_50S	SMB	SMBUS_SMC_5_G3_SCL	6 45 48
SMBUS_SMC_RSA_SDA	SMB_50S	SMB	SMBUS_SMC_5_G3_SDA	6 45 48
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	45 48
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	LVDS*	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

J30 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_C_P	6 41
	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_C_N	6 41
	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RDROUT_P	41
	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RDROUT_N	41
	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDRIN_P	41
	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDRIN_N	41
L293	SATA_90D	SATA3_PCH_TX	SATA_HDD_D2R_RDRIN_P	41
L291	SATA_90D	SATA3_PCH_TX	SATA_HDD_D2R_RDRIN_N	41
L292	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDROUT_P	41
L290	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDROUT_N	41
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	THMSNS_D1_P	51
	THERM_1TO1_55S	THERM	THMSNS_D1_N	51
L287	THERM_1TO1_55S	THERM	THMSNS_D2_P	51
L288	THERM_1TO1_55S	THERM	THMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29THMSNS_D2_P	
	THERM_1TO1_55S	THERM	T29THMSNS_D2_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 69
L315 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	49 69
L316	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	49
L322 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P	49
L321	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
L349 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	65
L350	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	65
L352 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	
L353	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	68 69
L355 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_THERMD_P	8 9
L354	SENSE_1TO1_55S	SENSE	CPU_THERMD_N	8 9
L356 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_N	49
L355	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_P	49
L281 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_R_N	49
L282	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_R_P	49
L283 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
L284	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
L292 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_P	49
L291	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_N	49
L315 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_R_P	49
L320	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_R_N	49
L297	LVDS_90D	LVDS_RCV_TX	LVDS_CONN_A_CLK_F_N	6 74
L298	LVDS_90D	LVDS_RCV_TX	LVDS_CONN_A_CLK_F_P	6 74

J30 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	64
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 60 61
L299 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	60
L300 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	60
L302 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	60
L303 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	60
L304 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	60
L305 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	60
L306 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	57 60
L307 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	57 60
L308 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	57 60
L310 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	57 60
L309 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	57 60
L311 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	57 60
L314 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	60
L312 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	60
L313 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	60
L316 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	60
L315 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	60
L316 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	60
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PPJV3_S5	6 7
		SB_POWER	PPJV3_S0	6 7
		SB_POWER	PPJV5_S3RS0	6 7
		GND	GND	

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Project Specific Constraints

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	ISL3,ISL4,ISL9	Y	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SE	ISL10	N	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
6X_DIELECTRIC	*	0.420 MM	?
7X_DIELECTRIC	*	0.490 MM	?

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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PAGE TITLE

PCB Rule Definitions

Apple Inc.

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