

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2011-04-08

K78 MLB SCHEMATIC

04/08/11


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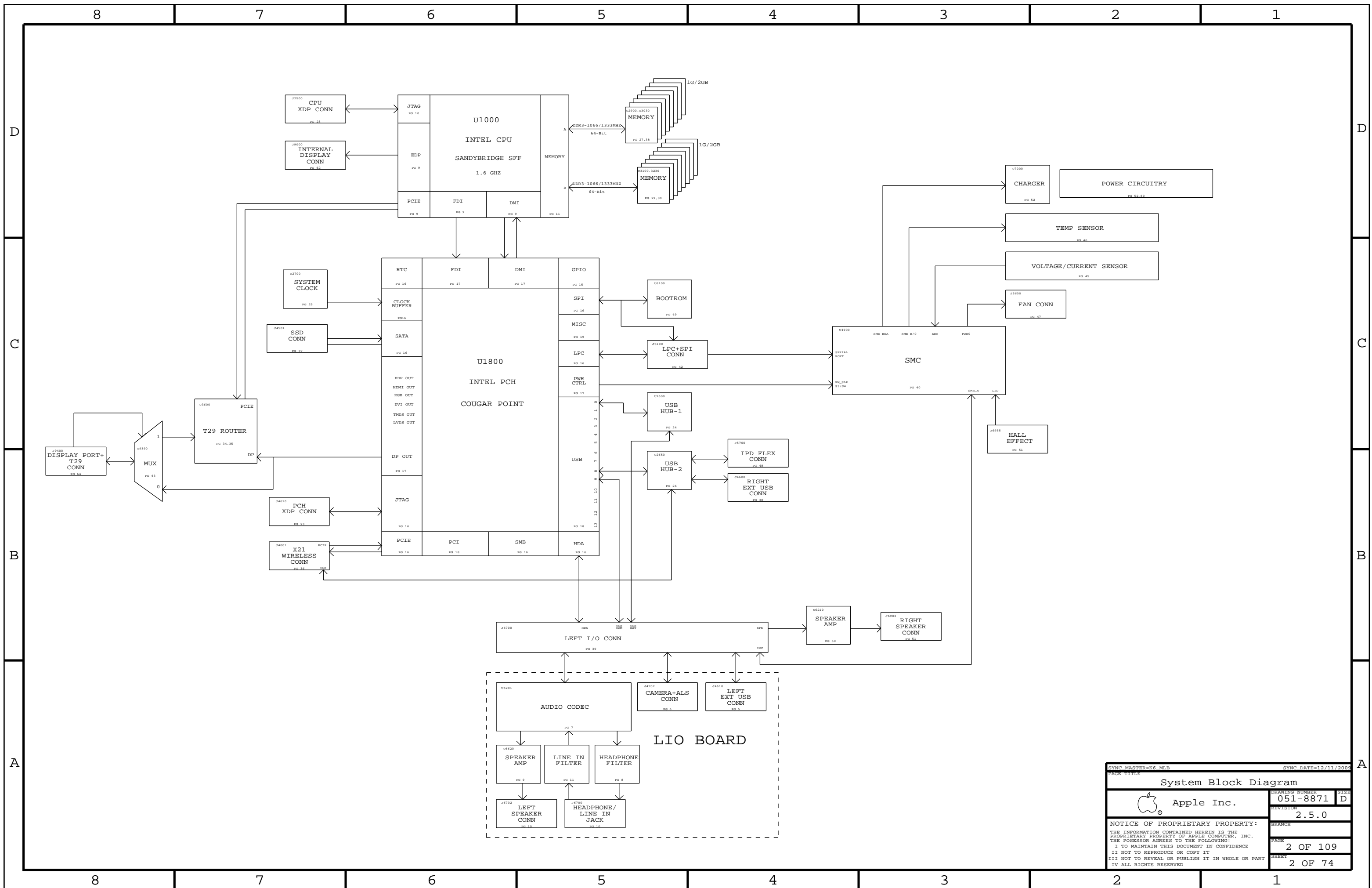
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Schematic / PCB #'s

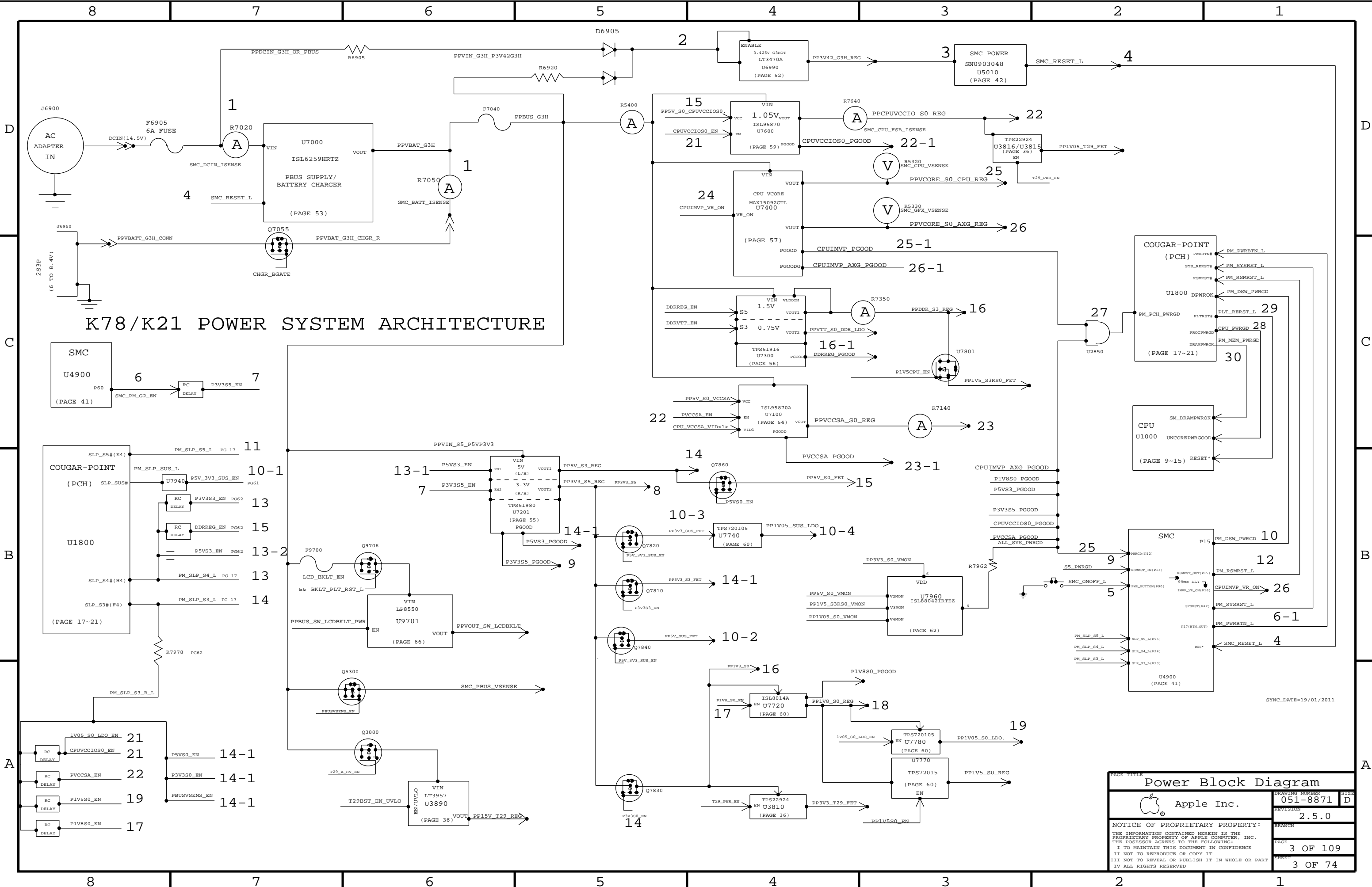
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8871	1	SCHEM_MLB_K78	SCH	CRITICAL	
820-3024	1	PCBF_MLB_K78	PCB	CRITICAL	

PRODUCT SAFETY REQUIREMENTS:
 PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
 PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
 NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE		SCHEM,MLB,K78	
 Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
	REVISION	2.5.0	
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SYNC MASTER=K6 MLR		SYNC DATE=12/11/2009	
PAGE TITLE			
System Block Diagram			
Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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K78/K21 POWER SYSTEM ARCHITECTURE

Power Block Diagram Apple Inc.		DRAWING NUMBER 051-8871	SIZE D
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SYNC_DATE=19/01/2011

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BOM Variants


BOM NUMBER	BOM NAME	BOM OPTIONS
639-1808	PCBA,MLB,K78	K78_OBNPTS,CPU1.6GHZ,EEEE:DK9L,DDR3:HYNIX_4GB
639-1889	PCBA,MLB,1.6GHZ,HY 4GB,K78	K78_OBNPTS,CPU1.6GHZ,EEEE:DLCL,DDR3:HYNIX_4GB
639-1990	PCBA,MLB,1.6GHZ,SA 2GB,K78	K78_OBNPTS,CPU1.6GHZ,EEEE:DLCT,DDR3:SAMSUNG_2GB
639-1999	PCBA,MLB,1.6GHZ,SA 4GB,K78	K78_OBNPTS,CPU1.6GHZ,EEEE:DLG6,DDR3:SAMSUNG_4GB
639-1987	PCBA,MLB,1.6GHZ,MI 2GB,K78	K78_OBNPTS,CPU1.6GHZ,EEEE:DLCP,DDR3:MICRON_2GB
639-1995	PCBA,MLB,1.6GHZ,EL 4GB,K78	K78_OBNPTS,CPU1.6GHZ,EEEE:DLD1,DDR3:ELPIDA_4GB
639-1998	PCBA,MLB,1.5GHZ,HY 2GB,K78	K78_OBNPTS,CPU1.5GHZ,EEEE:DLD4,DDR3:HYNIX_2GB
639-1991	PCBA,MLB,1.5GHZ,HY 4GB,K78	K78_OBNPTS,CPU1.5GHZ,EEEE:DLCT,DDR3:HYNIX_4GB
639-1986	PCBA,MLB,1.5GHZ,SA 2GB,K78	K78_OBNPTS,CPU1.5GHZ,EEEE:DLCH,DDR3:SAMSUNG_2GB
639-1985	PCBA,MLB,1.5GHZ,SA 4GB,K78	K78_OBNPTS,CPU1.5GHZ,EEEE:DLCH,DDR3:SAMSUNG_4GB
639-1992	PCBA,MLB,1.5GHZ,MI 2GB,K78	K78_OBNPTS,CPU1.5GHZ,EEEE:DLCH,DDR3:MICRON_2GB
639-1993	PCBA,MLB,1.5GHZ,EL 4GB,K78	K78_OBNPTS,CPU1.5GHZ,EEEE:DLCT,DDR3:ELPIDA_4GB
639-1994	PCBA,MLB,1.4GHZ,HY 2GB,K78	K78_OBNPTS,CPU1.4GHZ,EEEE:DLG0,DDR3:HYNIX_2GB
639-1988	PCBA,MLB,1.4GHZ,HY 4GB,K78	K78_OBNPTS,CPU1.4GHZ,EEEE:DLG0,DDR3:HYNIX_4GB
639-1997	PCBA,MLB,1.4GHZ,SA 2GB,K78	K78_OBNPTS,CPU1.4GHZ,EEEE:DLG3,DDR3:SAMSUNG_2GB
639-1984	PCBA,MLB,1.4GHZ,SA 4GB,K78	K78_OBNPTS,CPU1.4GHZ,EEEE:DLCT,DDR3:SAMSUNG_4GB
639-2000	PCBA,MLB,1.4GHZ,MI 2GB,K78	K78_OBNPTS,CPU1.4GHZ,EEEE:DLG5,DDR3:MICRON_2GB
639-1996	PCBA,MLB,1.4GHZ,EL 4GB,K78	K78_OBNPTS,CPU1.4GHZ,EEEE:DLG2,DDR3:ELPIDA_4GB
085-2714	K78 MLB DEVELOPMENT BOM	K78_DEVEL:EMG
607-8084	OMN PTS,PCBA,MLB,K78	K78_COMMON

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,L10,K99	[EEEE:DK9L]	CRITICAL	EEEE:DK9L
825-7563	1	LABEL,L10,K99	[EEEE:DLCL]	CRITICAL	EEEE:DLCL
825-7563	1	LABEL,L10,K99	[EEEE:DLCH]	CRITICAL	EEEE:DLCH
825-7563	1	LABEL,L10,K99	[EEEE:DLCH]	CRITICAL	EEEE:DLCH
825-7563	1	LABEL,L10,K99	[EEEE:DLCP]	CRITICAL	EEEE:DLCP
825-7563	1	LABEL,L10,K99	[EEEE:DLGQ]	CRITICAL	EEEE:DLGQ
825-7563	1	LABEL,L10,K99	[EEEE:DLCR]	CRITICAL	EEEE:DLCR
825-7563	1	LABEL,L10,K99	[EEEE:DLCT]	CRITICAL	EEEE:DLCT
825-7563	1	LABEL,L10,K99	[EEEE:DLCV]	CRITICAL	EEEE:DLCV
825-7563	1	LABEL,L10,K99	[EEEE:DLG6]	CRITICAL	EEEE:DLG6
825-7563	1	LABEL,L10,K99	[EEEE:DLCH]	CRITICAL	EEEE:DLCH
825-7563	1	LABEL,L10,K99	[EEEE:DLCT]	CRITICAL	EEEE:DLCT
825-7563	1	LABEL,L10,K99	[EEEE:DLG0]	CRITICAL	EEEE:DLG0
825-7563	1	LABEL,L10,K99	[EEEE:DLG3]	CRITICAL	EEEE:DLG3
825-7563	1	LABEL,L10,K99	[EEEE:DLG4]	CRITICAL	EEEE:DLG4
825-7563	1	LABEL,L10,K99	[EEEE:DLG5]	CRITICAL	EEEE:DLG5
825-7563	1	LABEL,L10,K99	[EEEE:DLG6]	CRITICAL	EEEE:DLG6

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-2714	1	K78 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-8084	1	OMN PTS,PCBA,MLB,K78	OMNPTS	CRITICAL	K78_COMMON

SYNC MASTER=K21_MLB		SYNC DATE=11/16/2010	
K78 BOM Variants			
 Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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K78 BOM GROUPS

BOM GROUP	BOM OPTIONS
K78_COMMON	ALTERNATE,COMMON,K78_MISC,K78_DEBUG:ENG,K78_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP
K78_MISC	PCH:B3,CPUMEM_S0,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRVI2C:MCU,SDRV_PD,KB_BL
K78_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K78_DEVEL:ENG	BLKT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:HW,XDP_PCH,LPPLUS,VREFMGN,SDG00D_ISL,S0_S0_LED,VCCIO1SNS_BNG,AIRPORT1SNS_BNG,VE1SNS_BNG,LCDBLKT1SNS_BNG
K78_DEVEL:PVT	LPPLUS,XDP_CONN,XDP_PCH
K78_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K78_DEBUG:PVT	DEVEL_BOM,BLKT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMGN_NOT
K78_DEBUG:PROD	BLKT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMGN_NOT,LPPLUS,VCCIO1SNS_PROD,AIRPORT1SNS_PROD,HDD1SNS_PROD,LCDBLKT1SNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33580550	1	EEPROM_32KBIT_2X1024	U3690	CRITICAL	T29ROM:BLANK
341T0354	1	IC,T29-ROM,K78	U3690	CRITICAL	T29ROM:PROG
33783997	1	IC,MCU,32M,LP1112A,16KB/2KB,HWQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0355	1	IC,T29-MCU,K78	U9330	CRITICAL	T29MCU:PROG
33880895	1	IC,SMC,RENESAS,H8S/21178P,98M,TLS,HP	U4900	CRITICAL	SMC:BLANK
341T0350	1	IC,SMC,K78	U4900	CRITICAL	SMC:PROG
33580809	1	44 MBIT SPI SERIAL DUAL I/O FLASH,REED:4	U6100	CRITICAL	BOOTROM:BLANK
33580803	1	44 MBIT SPI SERIAL DUAL I/O FLASH,REED:4	U6100	CRITICAL	BOOTROM:BLANK
341T0349	1	IC,SPI ROM,K21 K78	U6100	CRITICAL	BOOTROM:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Resist alt to Toshiba
37780307	37780066		ALL	OSRAM alt to Samsco
13880676	13880691		ALL	Murata alt to Samsung
37180679	37180652		ALL	NDP alt to NDP
13880671	13880673		ALL	Taiyo alt to Murata
13880679	13880678		ALL	Murata/Samsung alt to Taiyo
35383312	35383055		ALL	NDP ALT TO PERICOM
10480035	10480011		ALL	Panasonic alt to Cystec
15281085	15281307		ALL	Toko alt to Cystec
15281462	15281295		ALL	Toko alt to NWC inductor
12880333	12880294		ALL	Sanyo alt to Sanyo/Fredrick
33784092	33784100		ALL	EARLY 1.5GHZ CPU SAMPLES
33784093	33784101		ALL	EARLY 1.4GHZ CPU SAMPLES
37680874	37680895		ALL	FM9C0202 alt to AJK030202
37681018	37680617		ALL	FM9C0349 alt to AJK030309
37680826	37680917		ALL	AJK03209 alt to FM9C0355
514-0744	998-3941		ALL	NDP connector alt

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2	DIE REV	CFG 3
2GB	0	A	0
4GB	1	B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33784101	1	SNB,QAM1_QE,J1.1.6,17M,2+2.1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
33784100	1	SNB,QAM2_QE,J1.1.5,17M,2+2.1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
33784099	1	SNB,QAM3_QE,J1.1.4,17M,2+2.1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
33784098	1	SNB,QAMV_QE,J1.1.3,17M,2+2.1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
33784080	1	COUGAR POINT,SLHAG,PRO,8D92Q567	U1800	CRITICAL	PCH:B2
33784091	1	COUGAR POINT,B3,SL4K,PRO,8D92Q567	U1800	CRITICAL	PCH:B3
338S0976	1	IC,T29,FCBGA,PRQ 8x998	U3600	CRITICAL	T29:YES
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,VE8A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,VE8A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,VE8A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,VE8A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
607-6811	1	ASSEMBLY,SUBASBY,PCBA,HALL EFFECT,X99	J6955	CRITICAL	
353S2929	1	IC,12L6259,BATCHCHARGER,1%,4C48M,QFN28	U7000	CRITICAL	

SYMC PARTSHEET MGR SYMC DATE:11/16/2011

PAGE TITLE: BOM Configuration

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH:

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SHEET: 5 OF 74

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Functional Test Points

8 7 6 5 4 3 2 1

J4001: AirPort / BT Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for AirPort / BT Connector.

J5600: Fan Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for Fan Connector.

J5700: IPD Flex Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for IPD Flex Connector.

J4501: SATA SSD Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for SATA SSD Connector.

J6900: DC-In Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for DC-In Connector.

J6903: Speaker Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for Speaker Connector.

J4700: LIO Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for LIO Connector.

J6950: Battery Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for Battery Connector.

J9000: Internal DP Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for Internal DP Connector.

J5715: KB BFLT Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for KB BFLT Connector.

J6955: HALL EFFECT Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for HALL EFFECT Connector.

J5100: LPC+SPI Connector

Table with columns: FUNC_TEST, TP, and TP. Lists test points for LPC+SPI Connector.

Misc Voltages & Control Signals

Table with columns: FUNC_TEST, TP, and TP. Lists test points for Misc Voltages & Control Signals.

NO_TEST Nets

Large table listing NO_TEST Nets with columns for TP, MAKE_BASE+TRUE, and TP. Includes various test point identifiers.

Table listing test points for various components like NC EDP TXP, NC CPU THERMDC, etc.

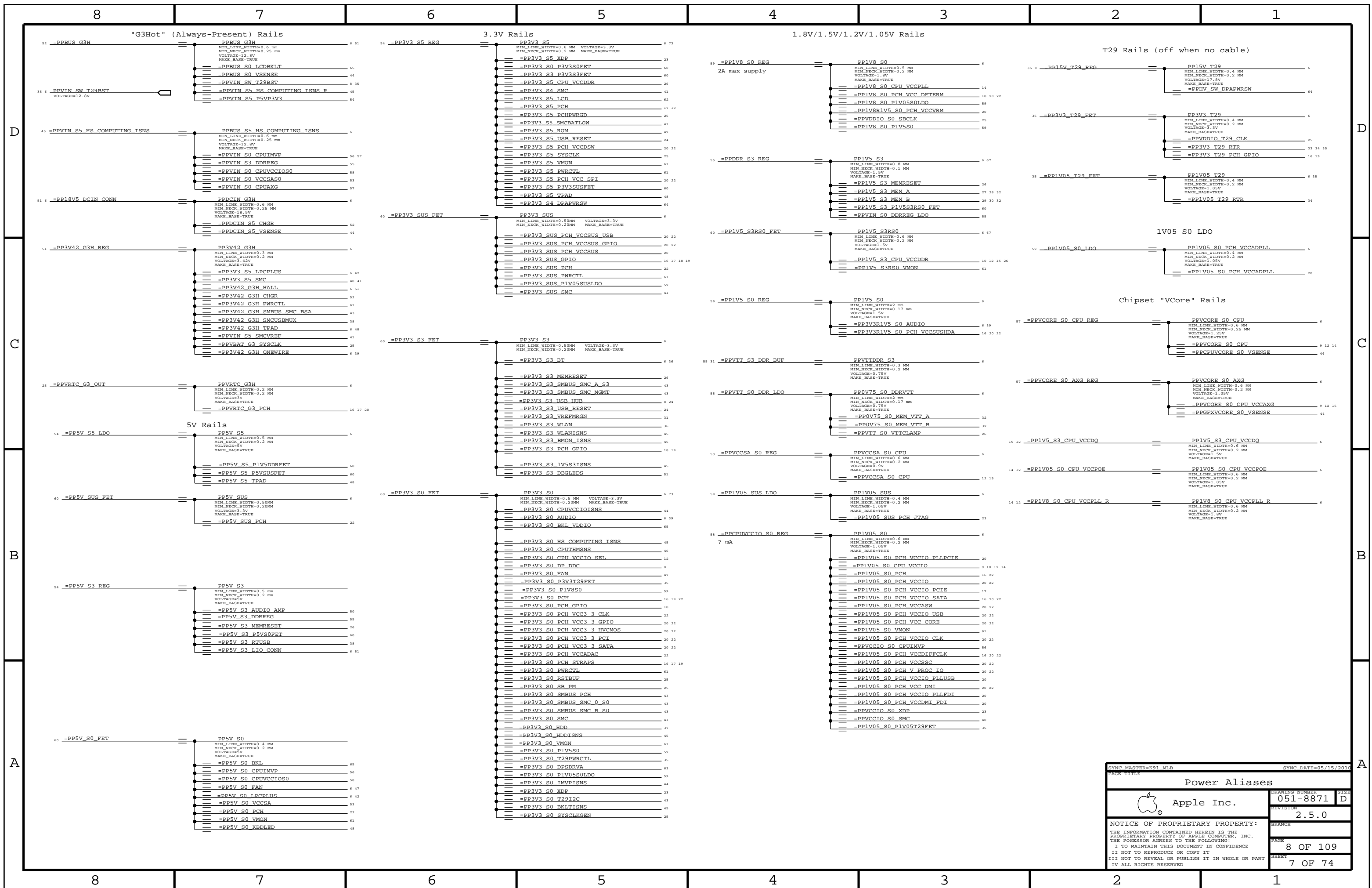
Table listing test points for various components like TP PCIE CLK100M PE4N, TP SATA B D2RN, etc.

Table listing test points for various components like TP PCH TP18, TP PCH TP17, etc.

Table listing test points for various components like TP PCH VSS NTFP<1>, TP LVDS IG B CLKN, etc.

Functional Test / No Test header with Apple logo, drawing number 051-8871, revision 2.5.0, and a notice of proprietary property.

8 7 6 5 4 3 2 1



SYNC MASTER=K91 MLB SYNC DATE=05/15/2011

Power Aliases

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

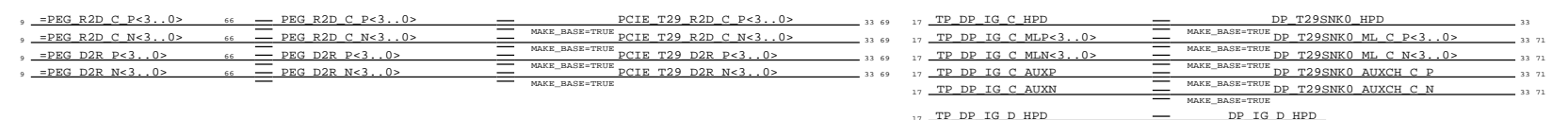
BRANCH:

PAGE: 8 OF 109

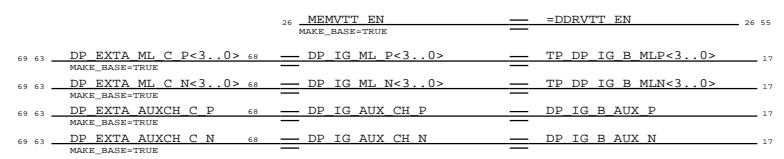
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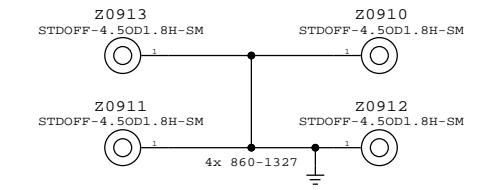
T29 DP Ports



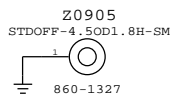
CPU signals



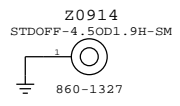
CPU Heat Sink Mounting Bosses



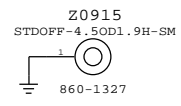
Fan Boss



X21 Boss

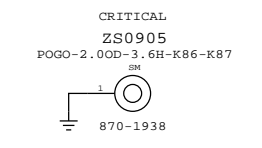


SSD Boss

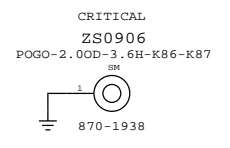


EMI I/O Pogo Pins

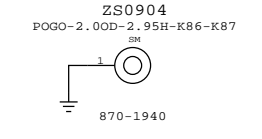
DisplayPort Pogo



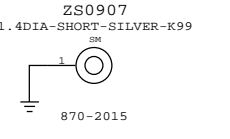
USB/SD Card Pogo



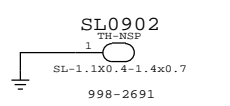
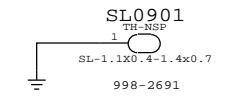
DisplayPort Pogo



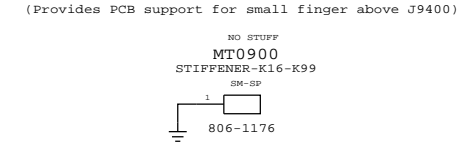
USB/SD Card Pogo



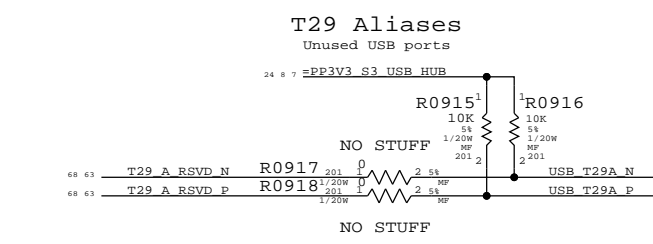
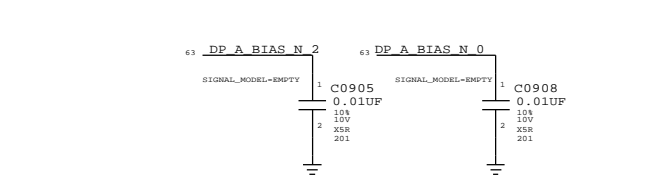
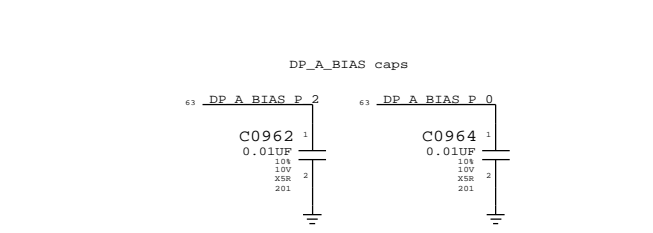
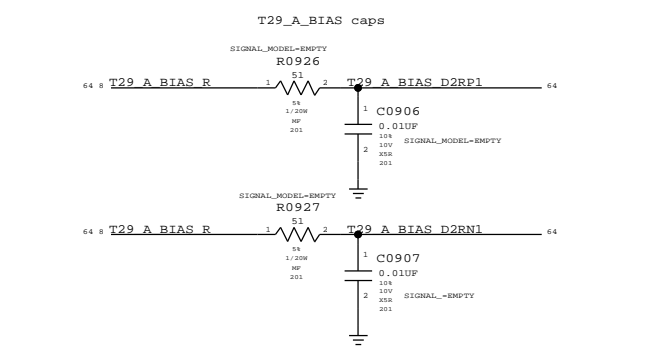
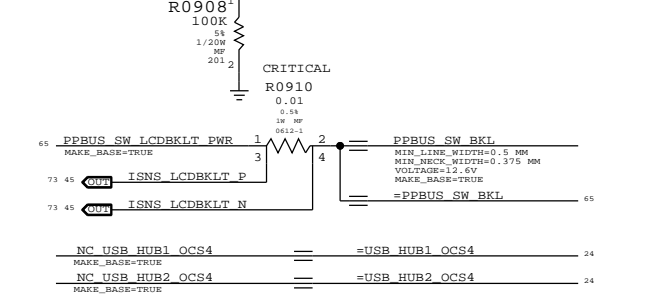
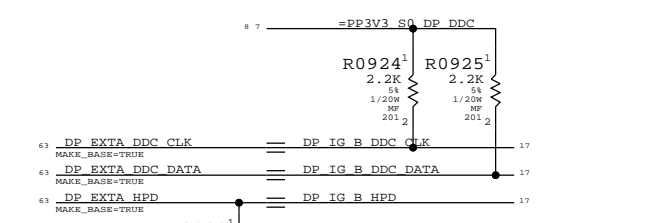
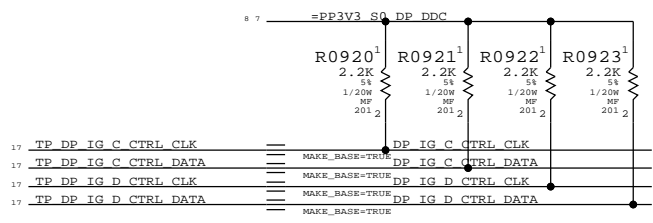
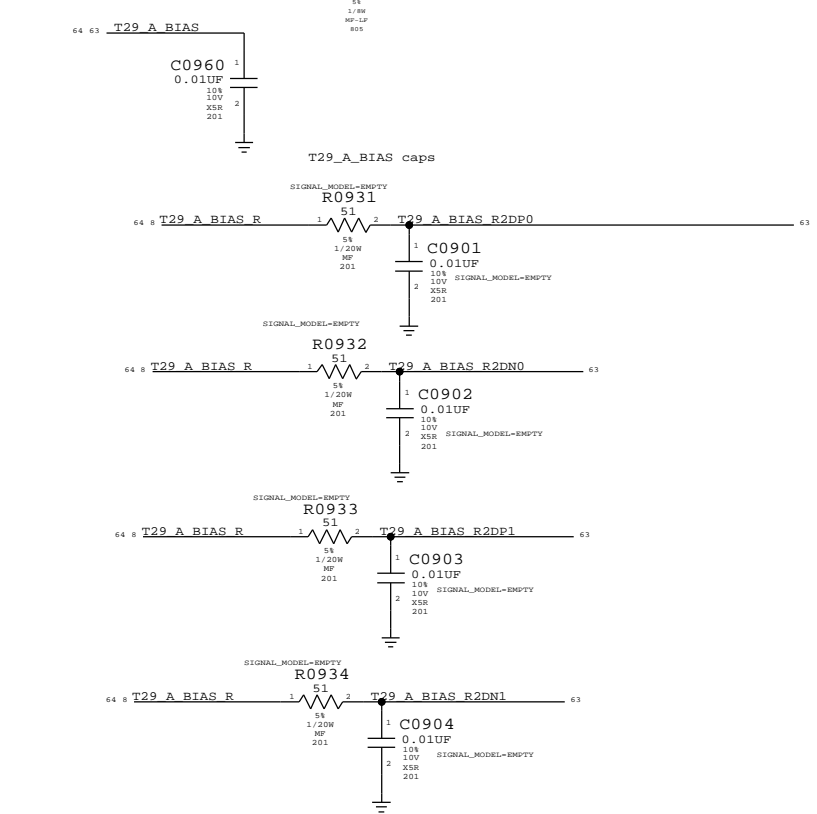
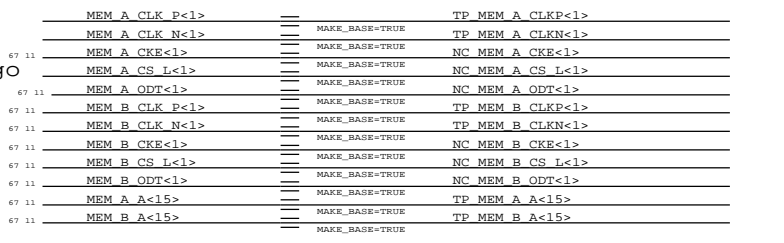
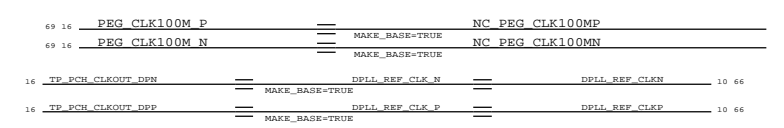
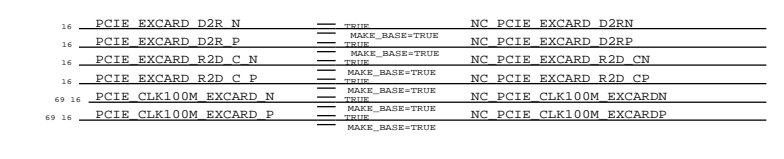
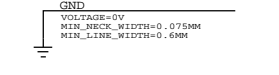
T29 Can Slots



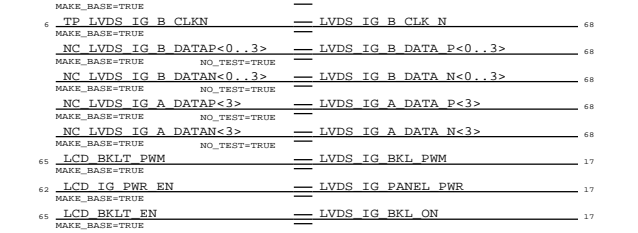
DisplayPort PCB Stiffener



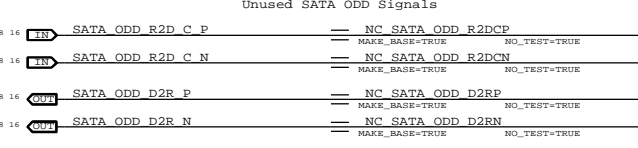
Digital Ground



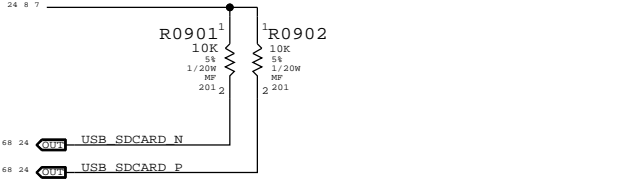
LVDS Aliases



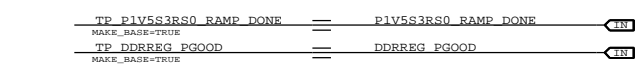
SATA Aliases



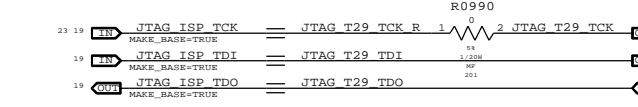
UNUSED SDCARD USB Aliases



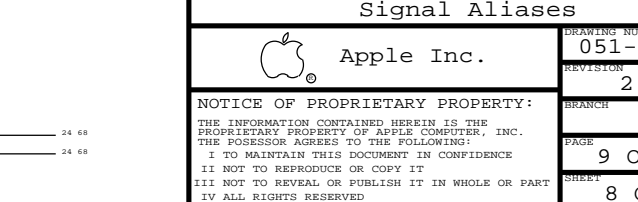
Unused PGOOD signal



T29 JTAG



Signal Aliases



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D

C

B

A

D

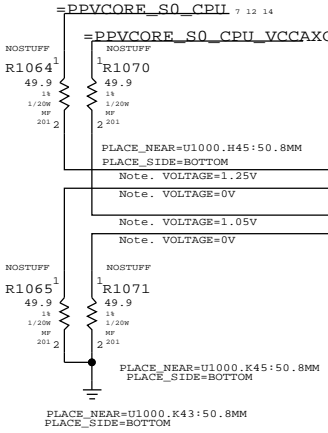
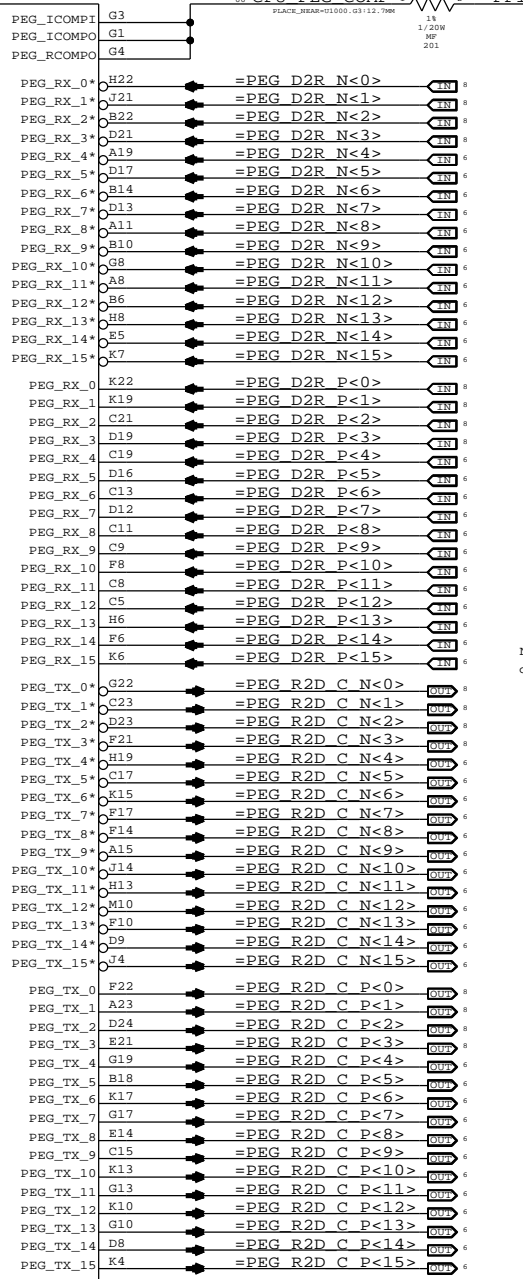
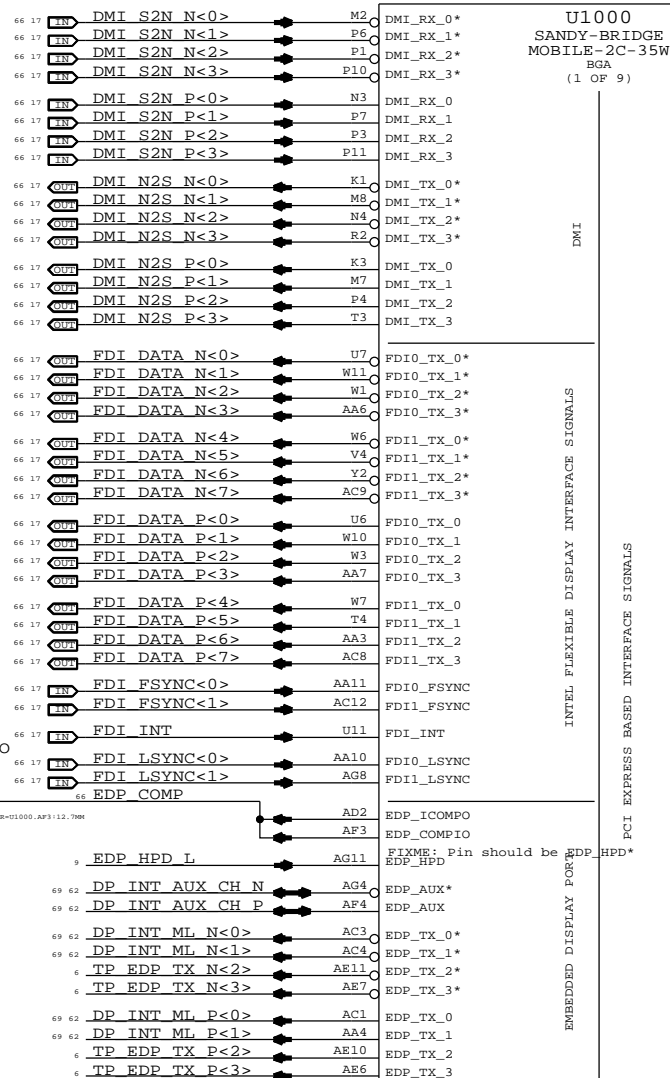
C

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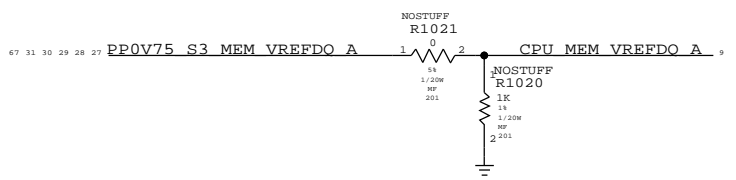
A

OMIT TABLE CRITICAL

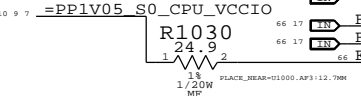
NOTE: Intel provides an internal pull-up of 5-15k to VCCIO on all CFG signals.
OMIT TABLE CRITICAL



NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.



NOTE: Intel is investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls BE7 and BG7 for Sandy Bridge 2-core to SO-DIMM connectors directly. FETs are needed in order to avoid potential leakage while system is in S3 state.

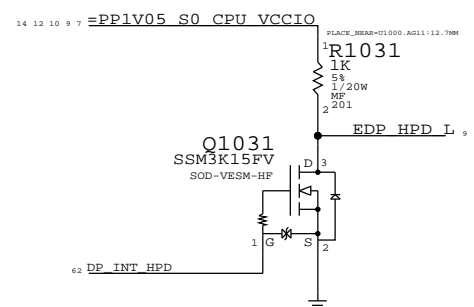
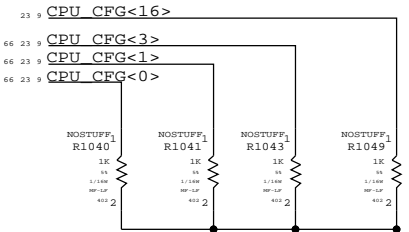
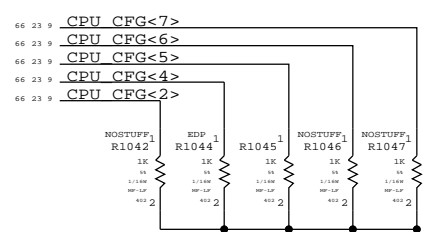


Intel Doc 438297 Huron River SFF DG rev1.0 section 2.2.1 recommendation.

NOTE: eDP_COMP0 and eDP_ICOMP0 can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPDP processor input is a low voltage active low signal. Therefore an inverting level shifter is required on the motherboard to convert the active high signal from Embedded Display Port sink device to low voltage signals for EDP processor. (refer to latest Processor for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.



FOR SANDYBRIDGE PROCESSOR

CFG [7] : PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xRESETB	0 = WAIT FOR BIOS
CFG [6:5] : PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8
CFG [4] : eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] : PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] : PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

CPU DMI/PEG/FDI/RSVD

Apple Inc.

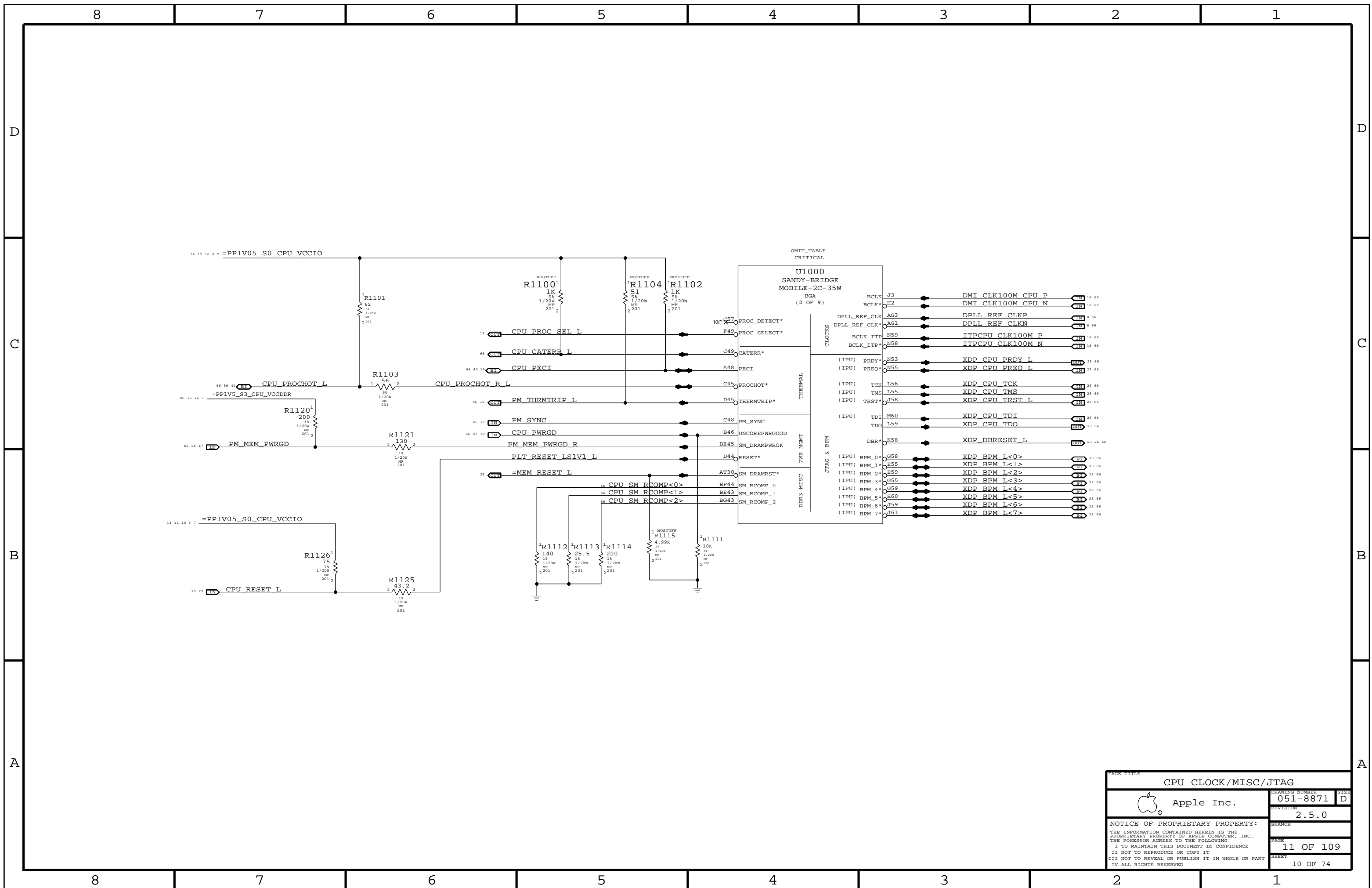
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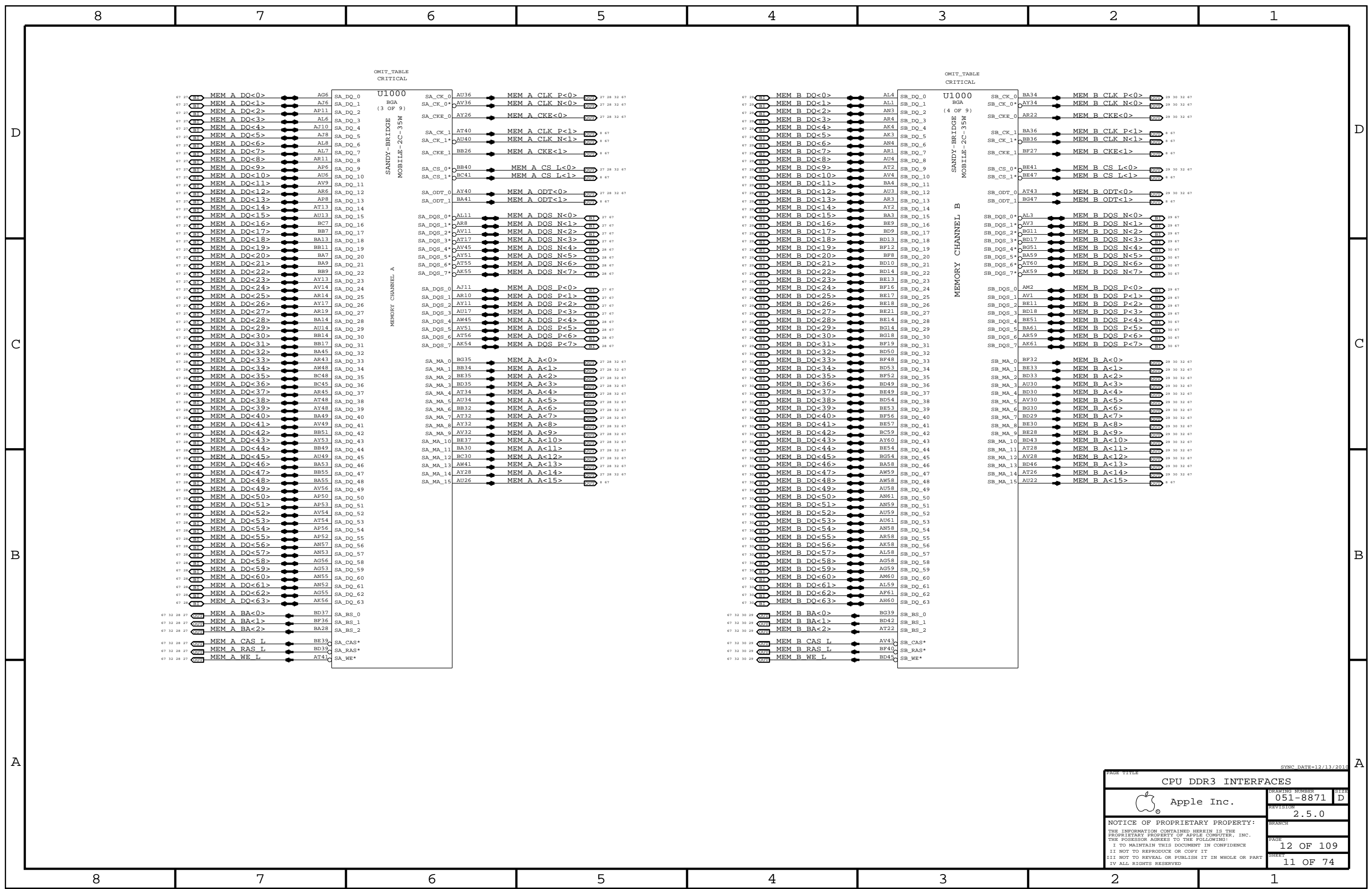
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	PAGE	11 OF 109
	SHEET	10 OF 74



OMIT_TABLE
CRITICAL

OMIT_TABLE
CRITICAL

U1000
BGA
(3 OF 9)

U1000
BGA
(4 OF 9)

SANDY-BRIDGE
MOBILE-2C-35W

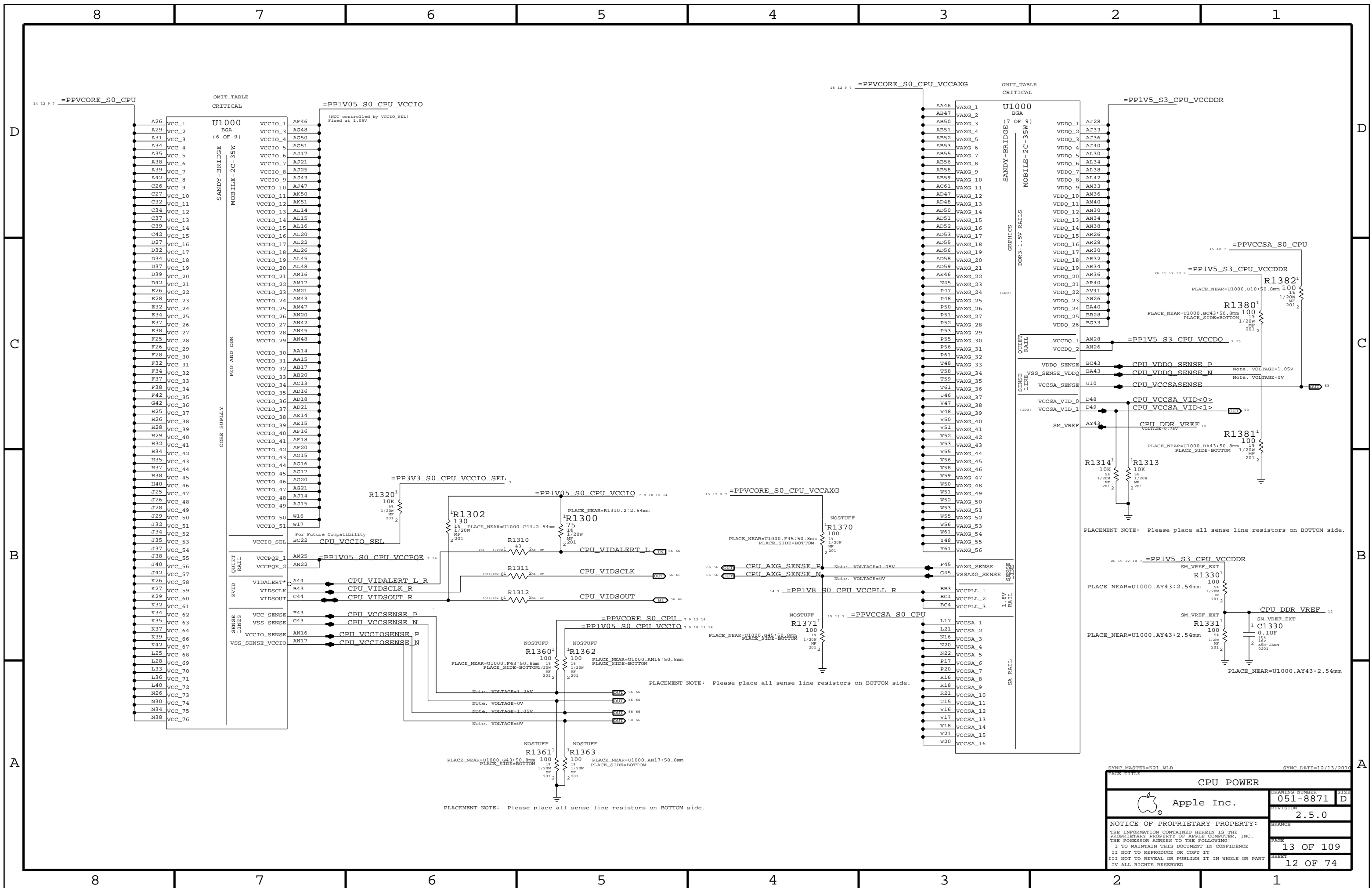
SANDY-BRIDGE
MOBILE-2C-35W

MEMORY CHANNEL A

MEMORY CHANNEL B

SYNC DATE=12/13/2016

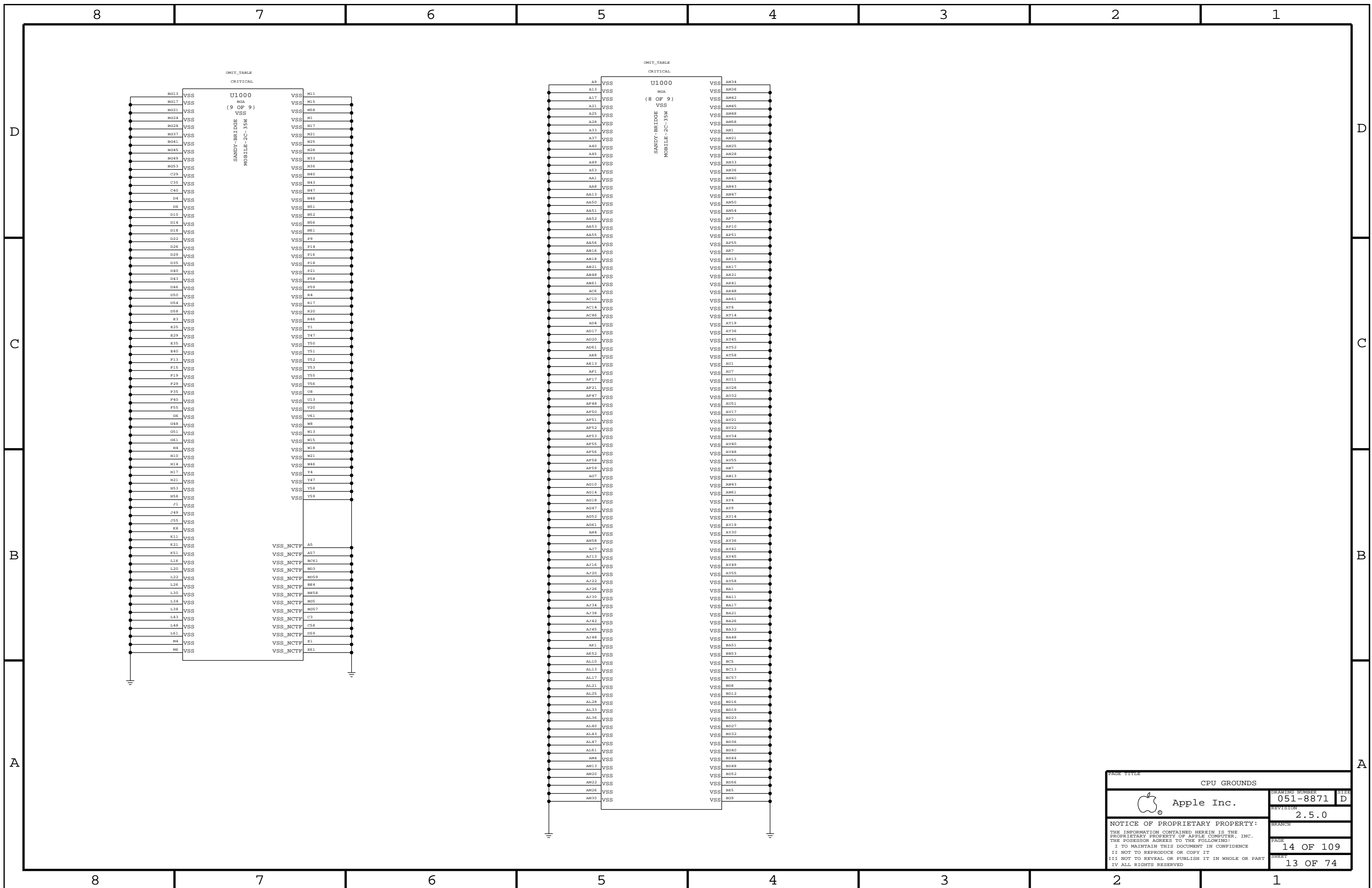
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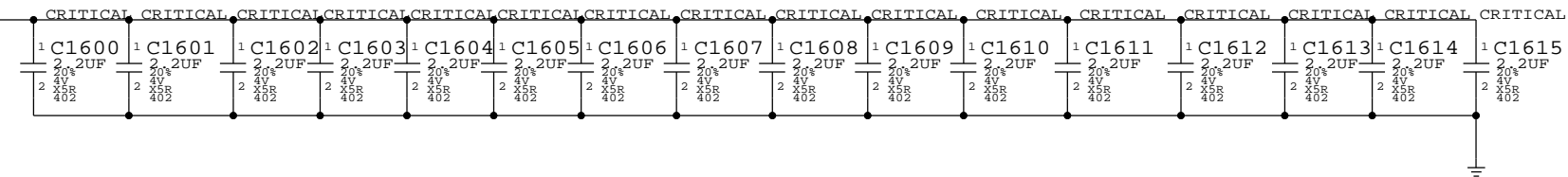
PAGE TITLE		CPU GROUNDS	
	DRAWING NUMBER	051-8871	SIZE
	REVISION	2.5.0	D
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Processor Load Line : -2.9 mOhms

CPU VCORE DECOUPLING

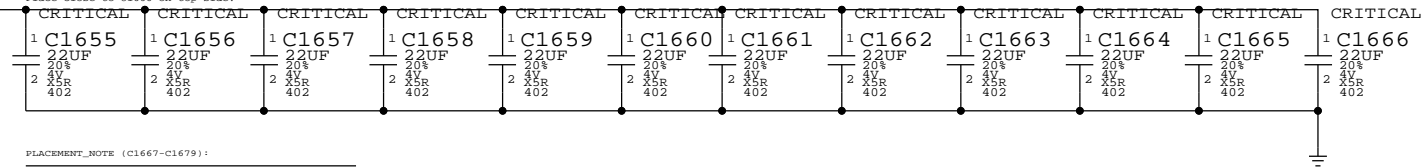
Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU



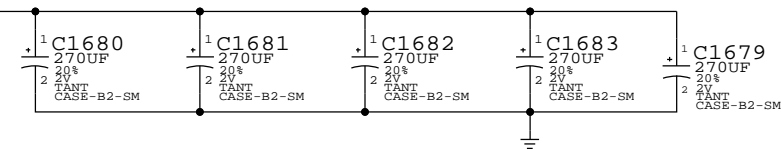
PLACEMENT_NOTE (C1655-C1666):

Place close to U1000 on top side.



PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):



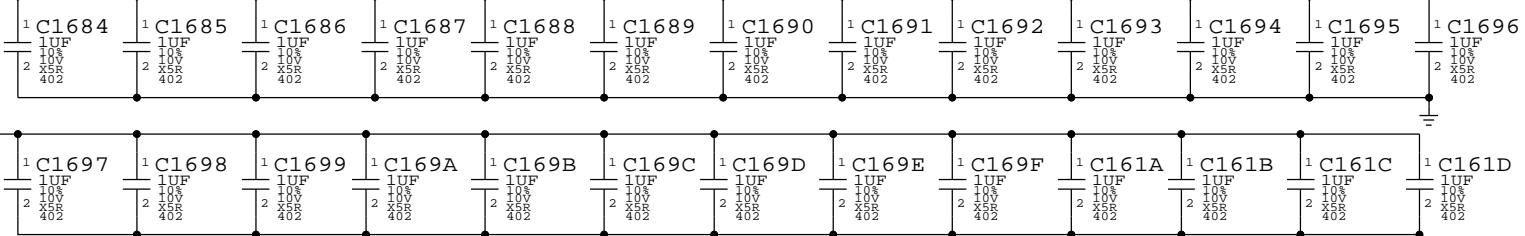
CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C1697):

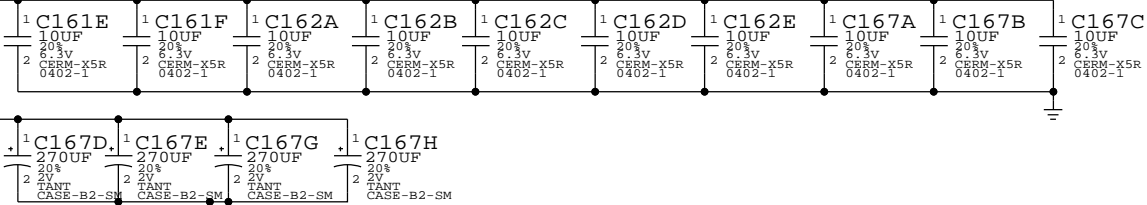
Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

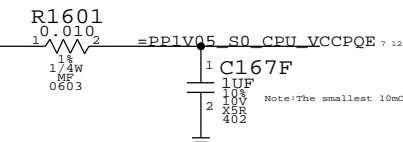


PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



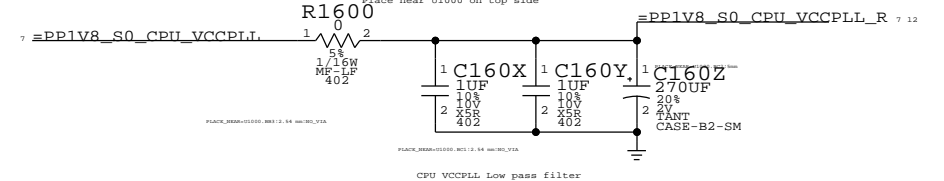
Note: The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side



CPU VCCPLL Low pass filter

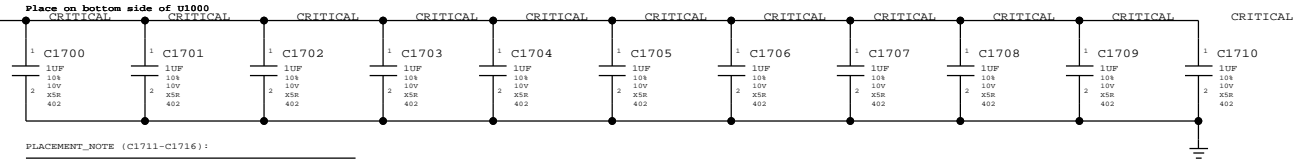
CPU DECOUPLING-I		DRAWING NUMBER	051-8871	SIZE	D
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VAXG DECOUPLING

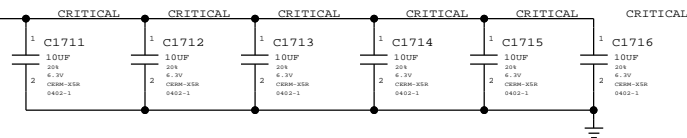
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

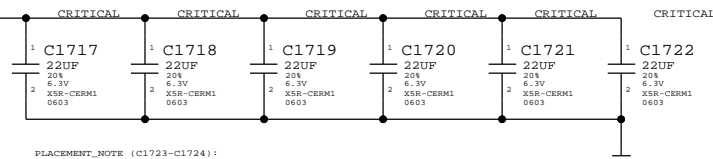
PLACEMENT_NOTE (C1700-C1710):



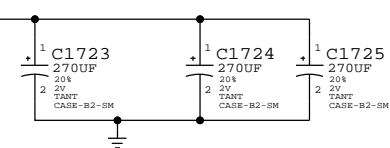
PLACEMENT_NOTE (C1711-C1716):



PLACEMENT_NOTE (C1717-C1722):



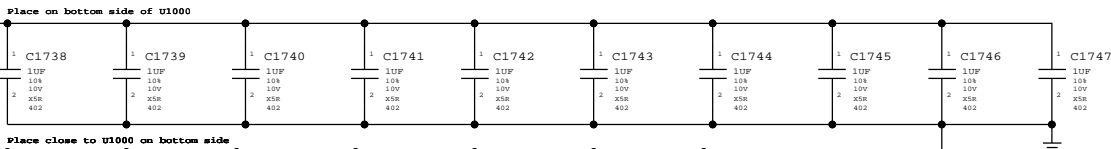
PLACEMENT_NOTE (C1723-C1724):



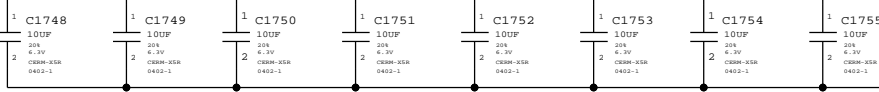
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

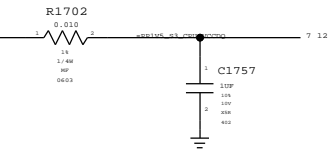
PLACEMENT_NOTE (C1738-C1747):



Place close to U1000 on bottom side



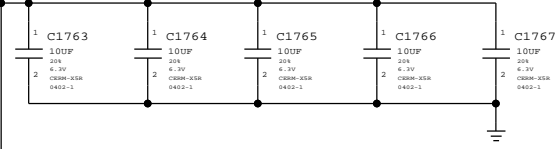
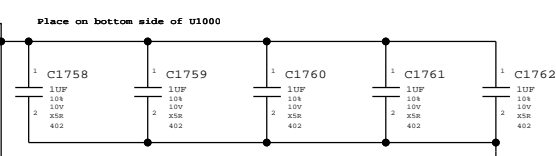
Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402



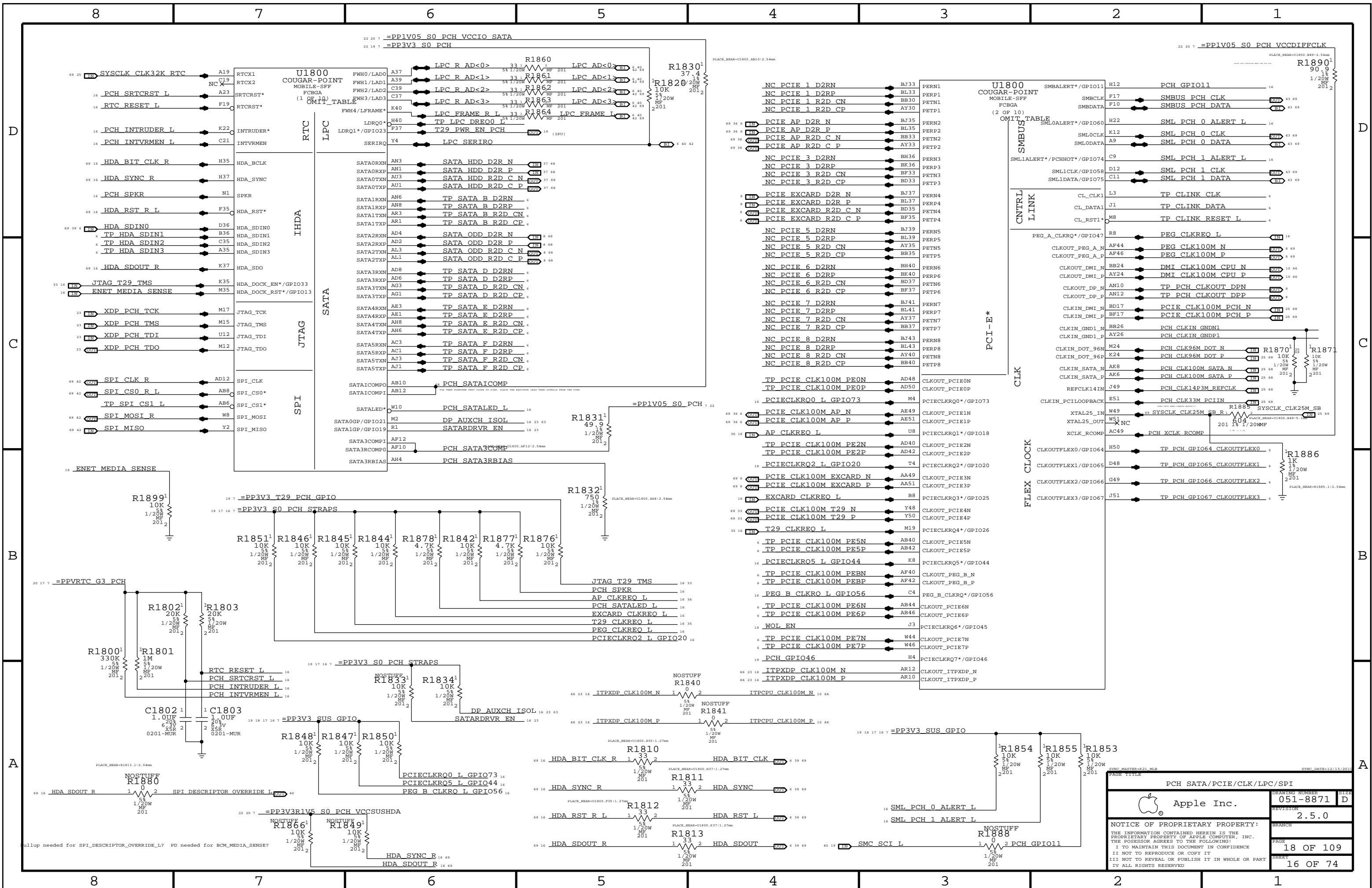
CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uF, 3x 10uF, 1x 330uF

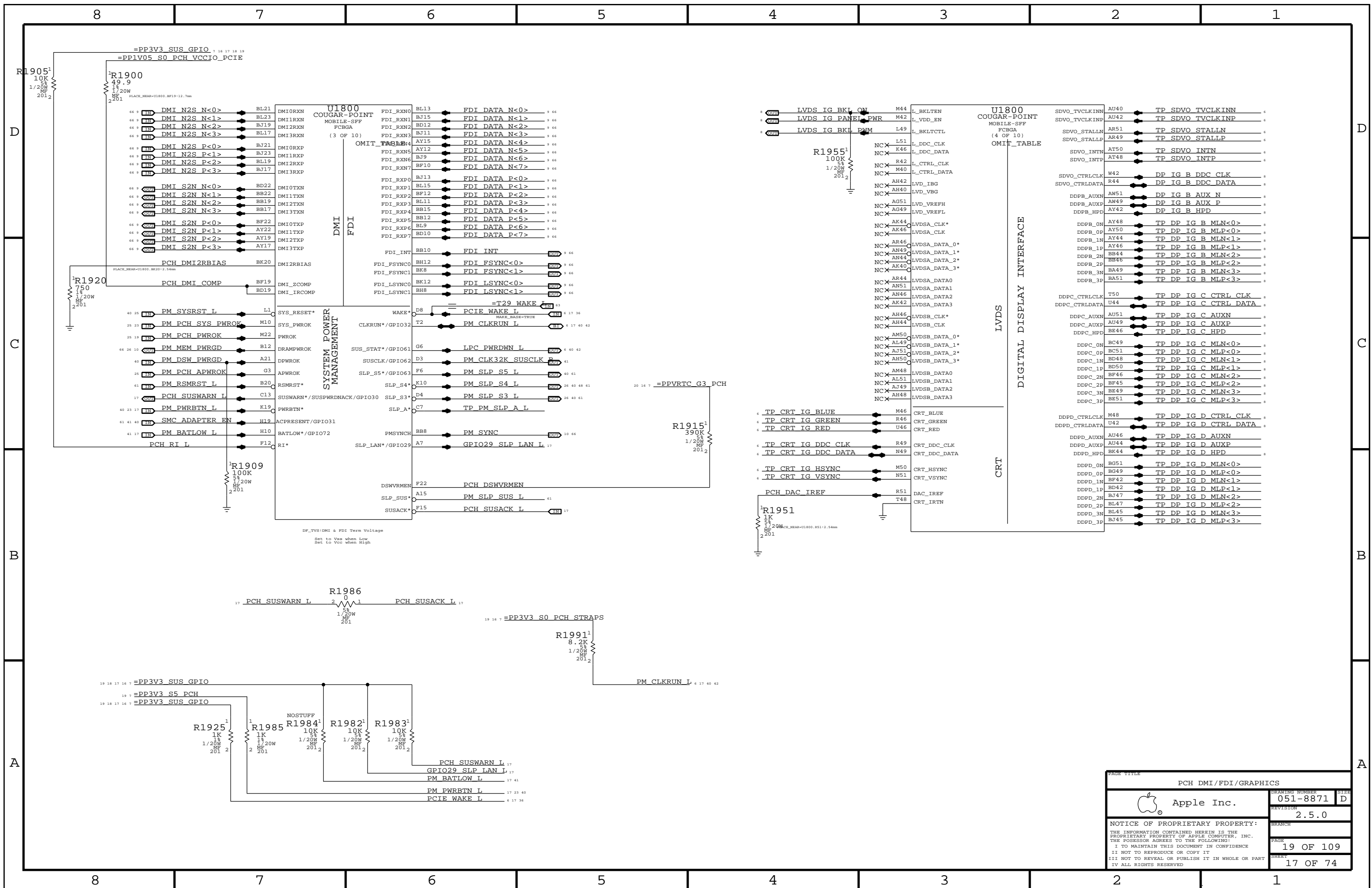
PLACEMENT_NOTE (C1758-C1762):

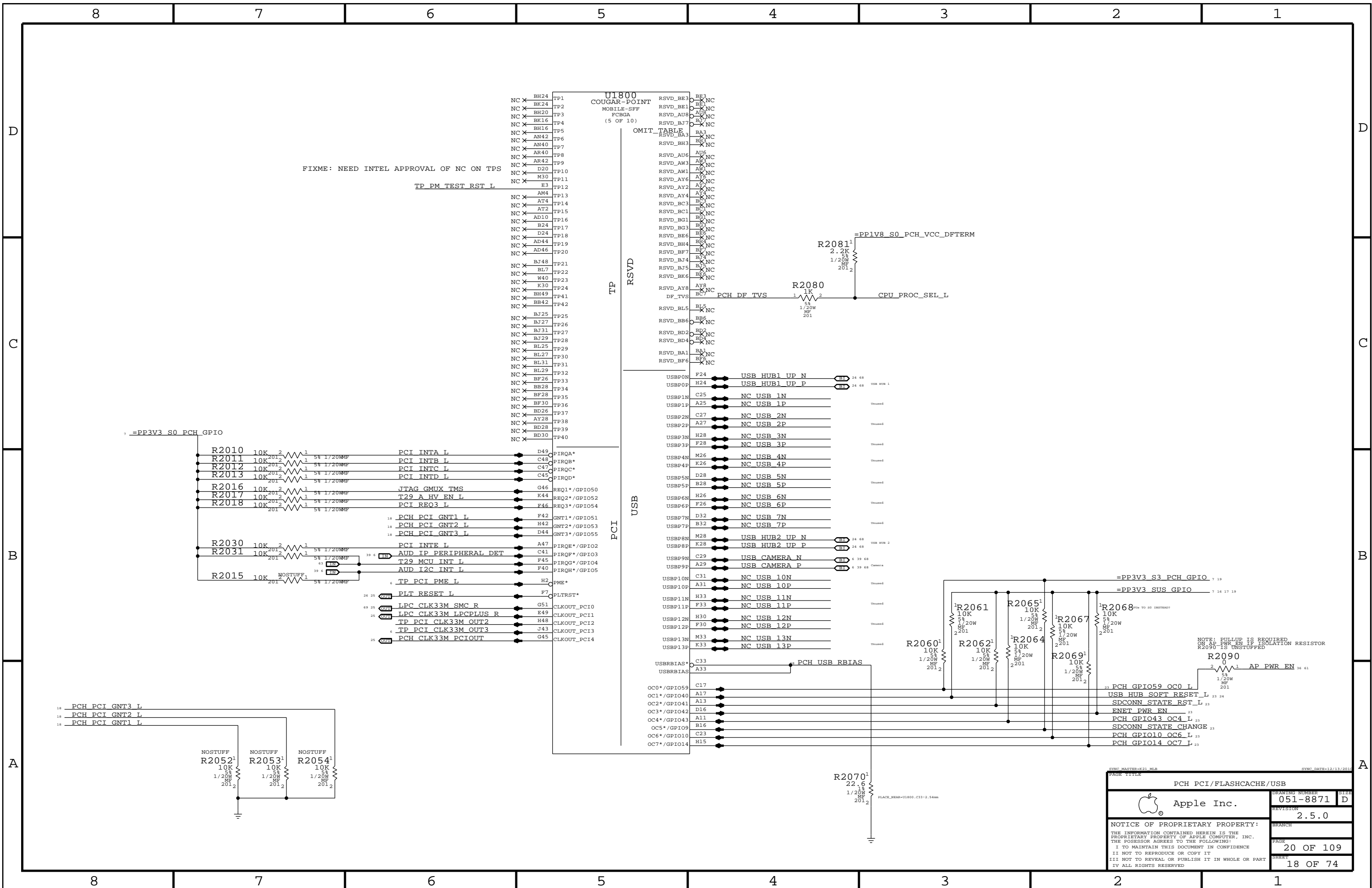


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CPU DECOUPLING-II		051-8871		D
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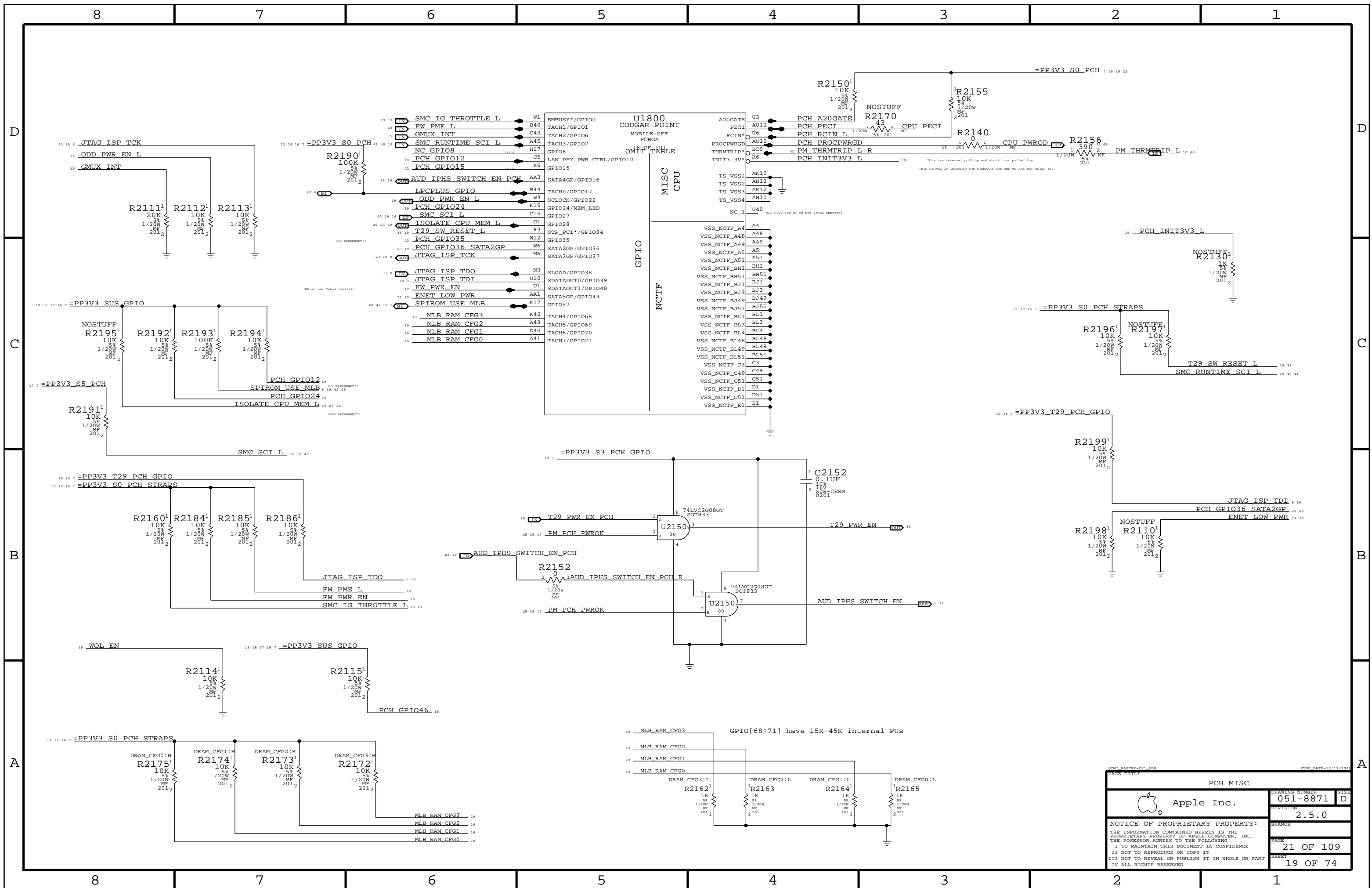
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PAGE TITLE		PCH SATA/PCIe/CLK/LPC/SPI		DRAWING DATE: 12/13/2011	
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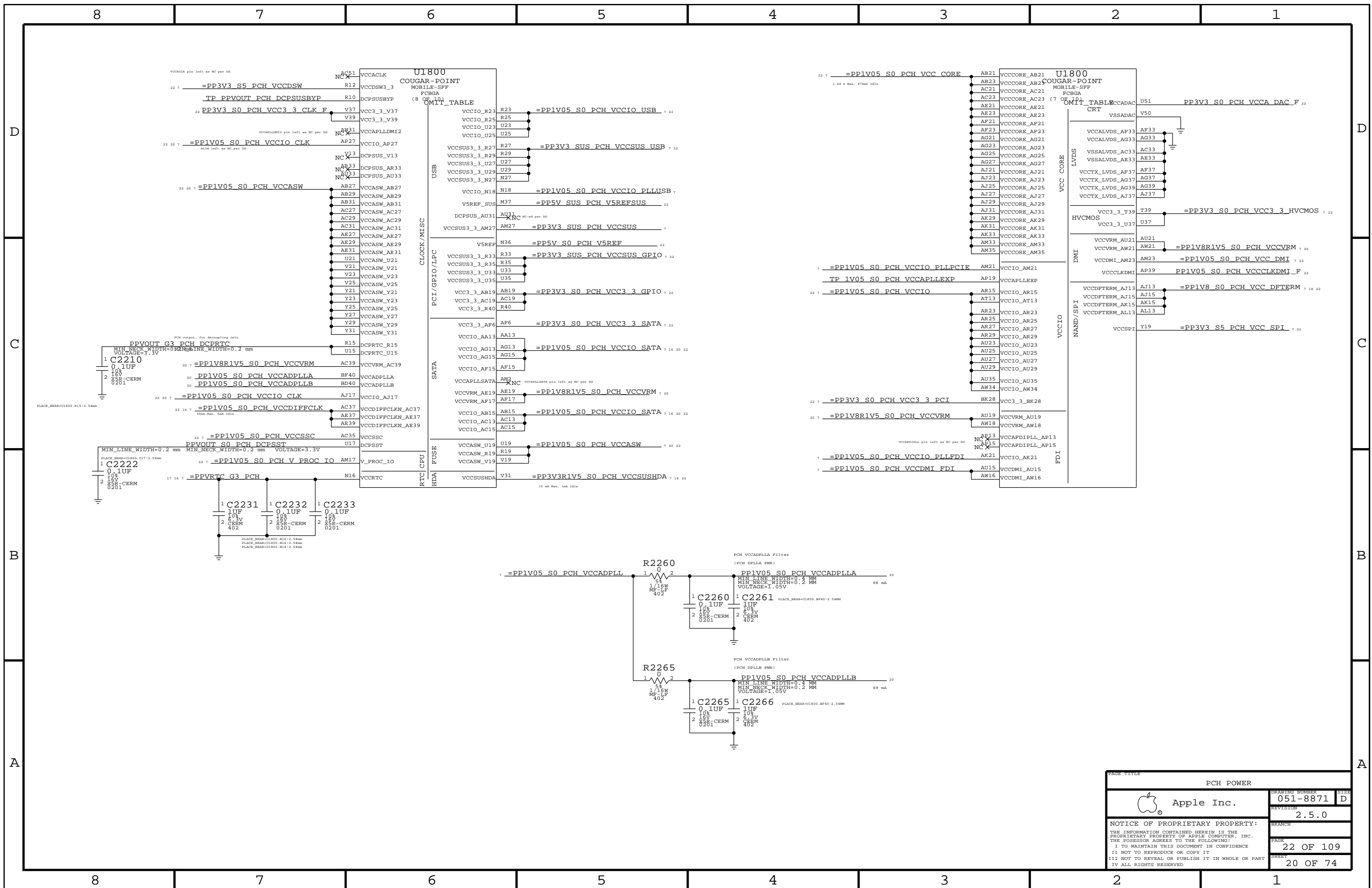
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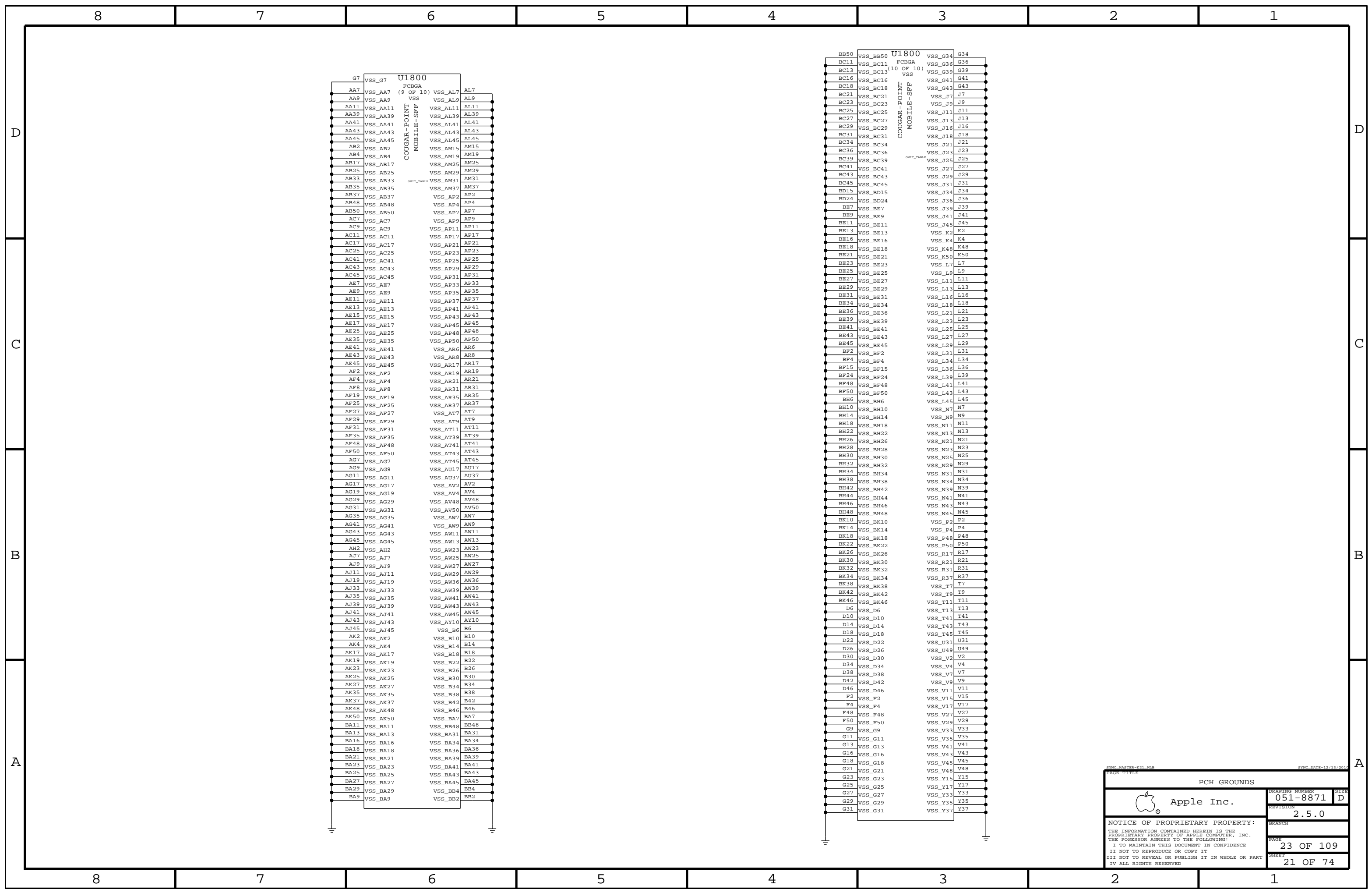


PCH MISC		DRAWING NUMBER	SIZE
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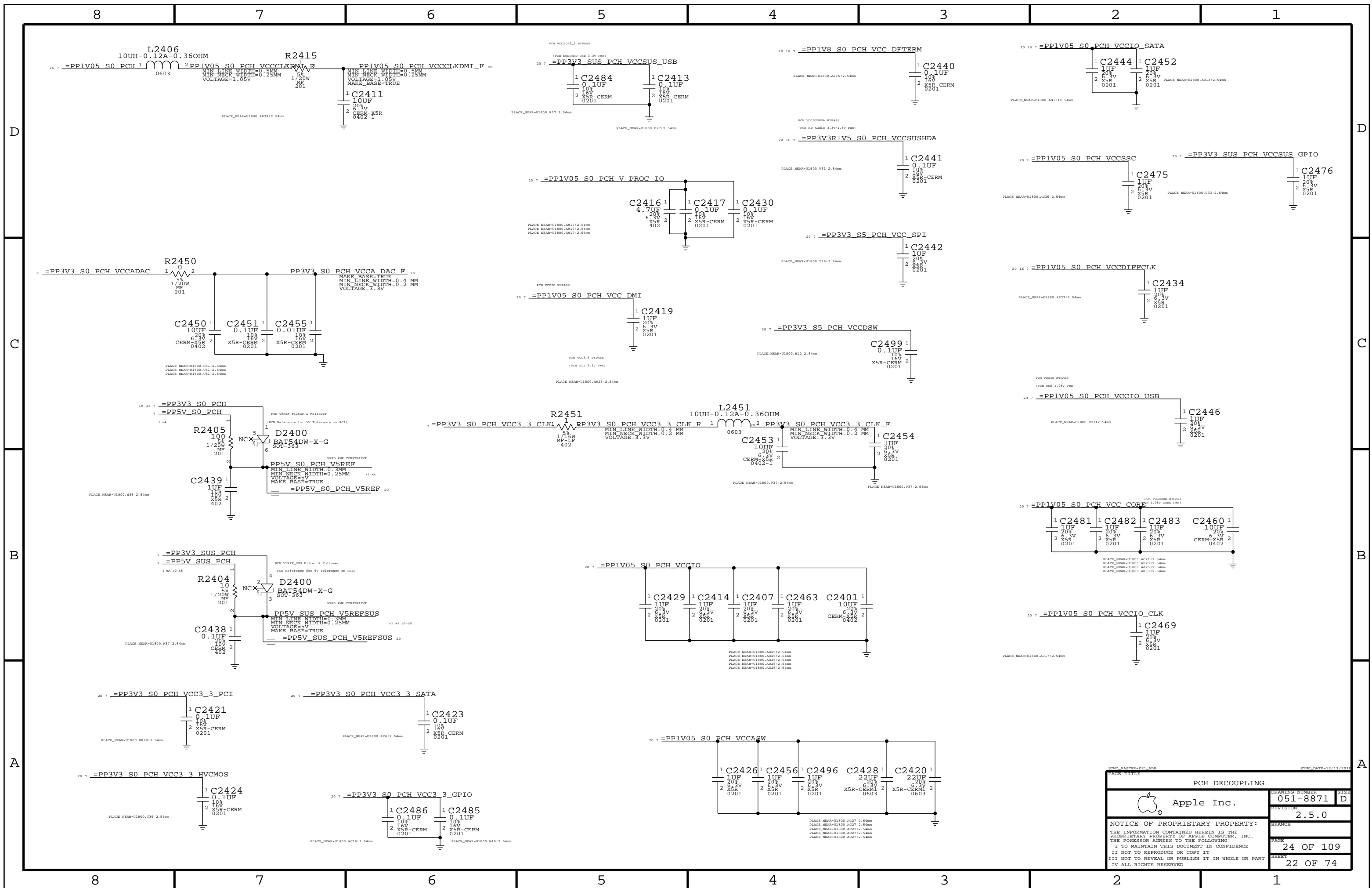
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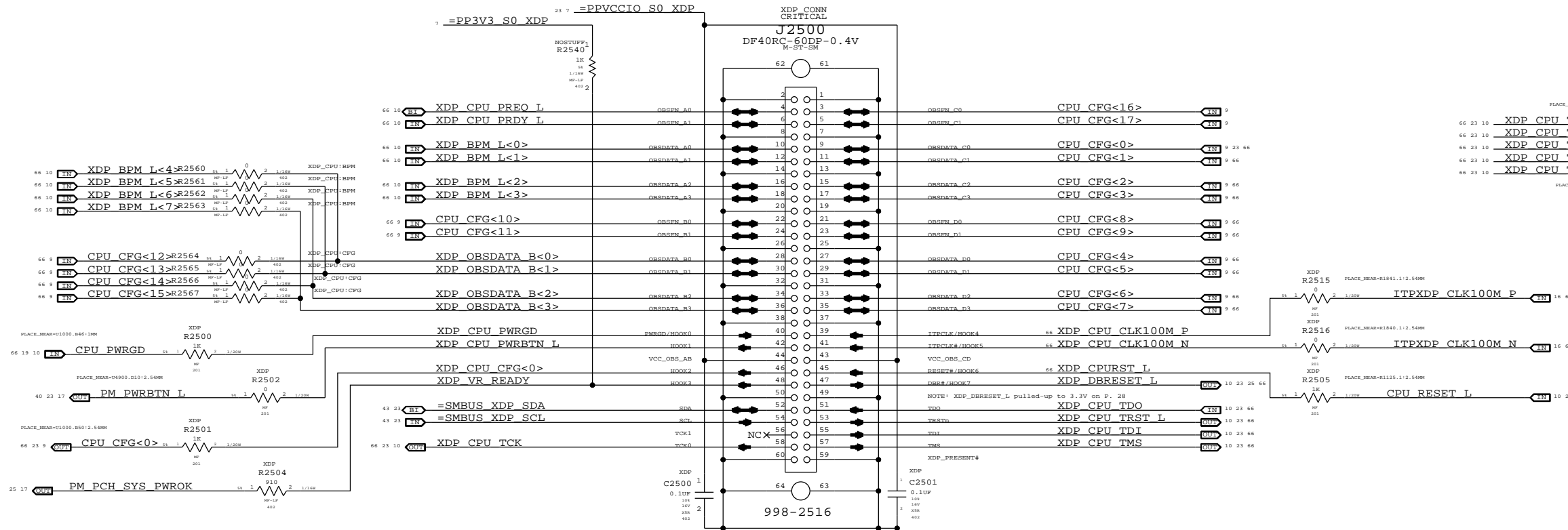
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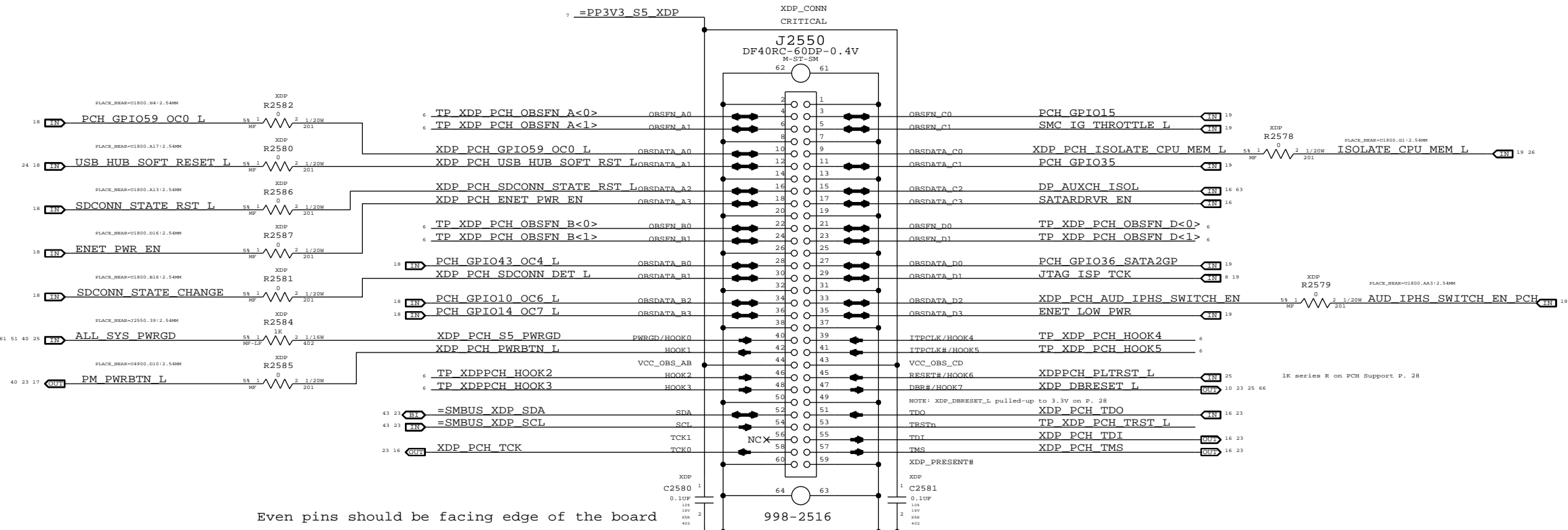
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PROCESSOR MICRO2-XDP CONNECTOR
 NOTE: This is not the standard XDP pinout
 Use with 920-0782 Adapter Flex to support chipset debug

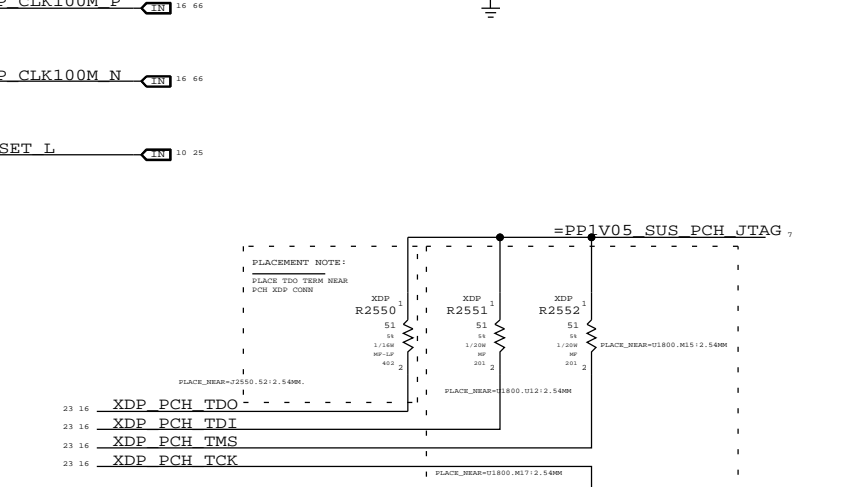
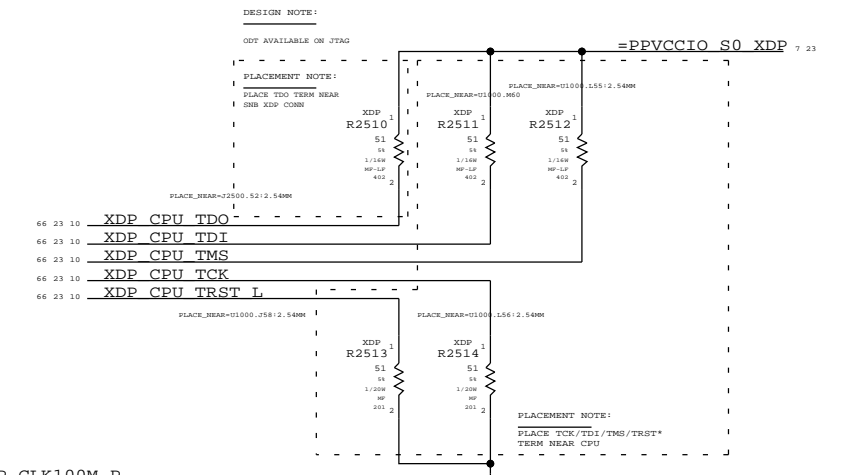


Even pins should be facing edge of the board

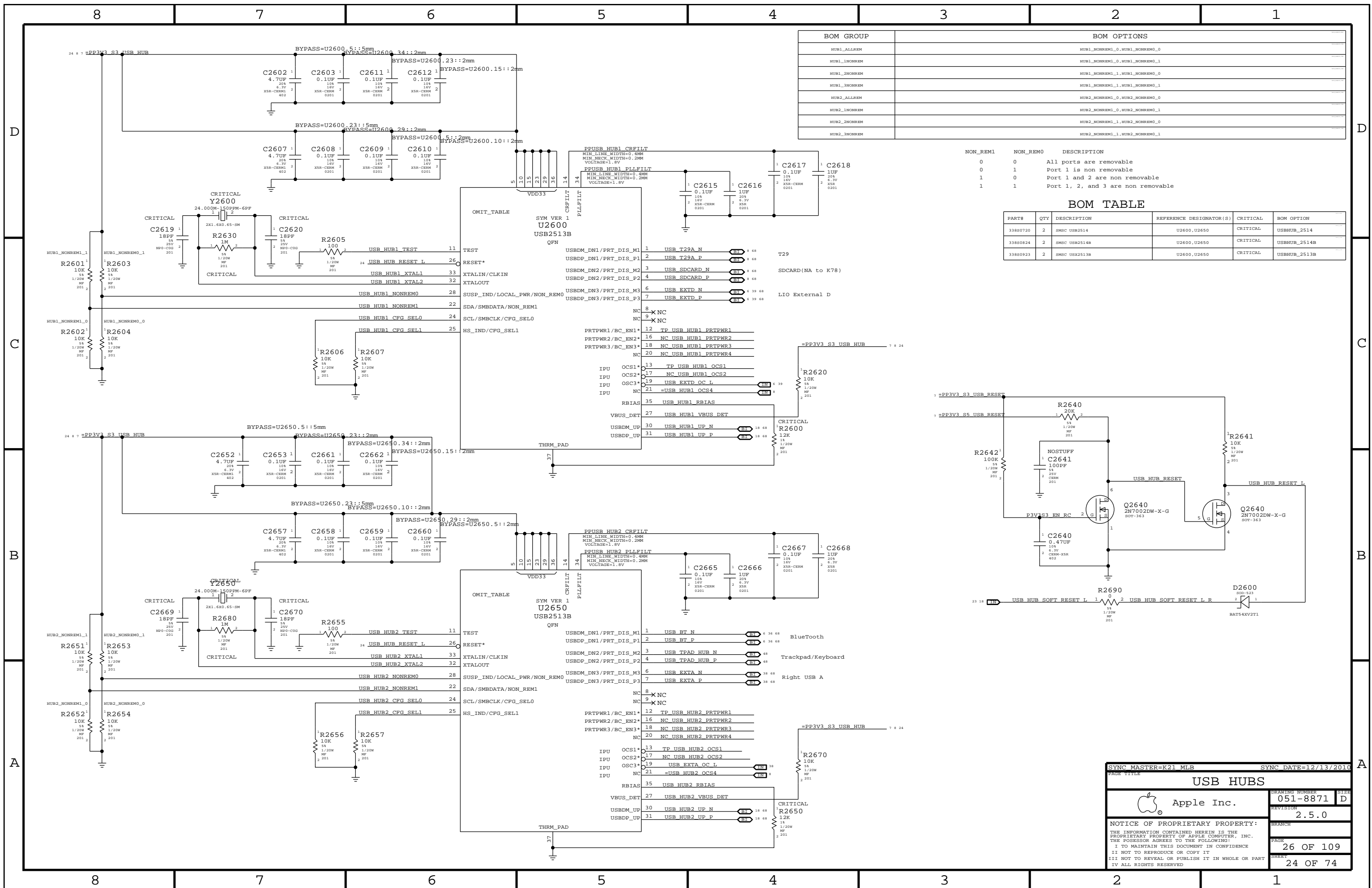
PCH MICRO2-XDP CONNECTOR
 NOTE: This is not the standard XDP pinout
 Use with 920-0782 Adapter Flex to support chipset debug



Even pins should be facing edge of the board



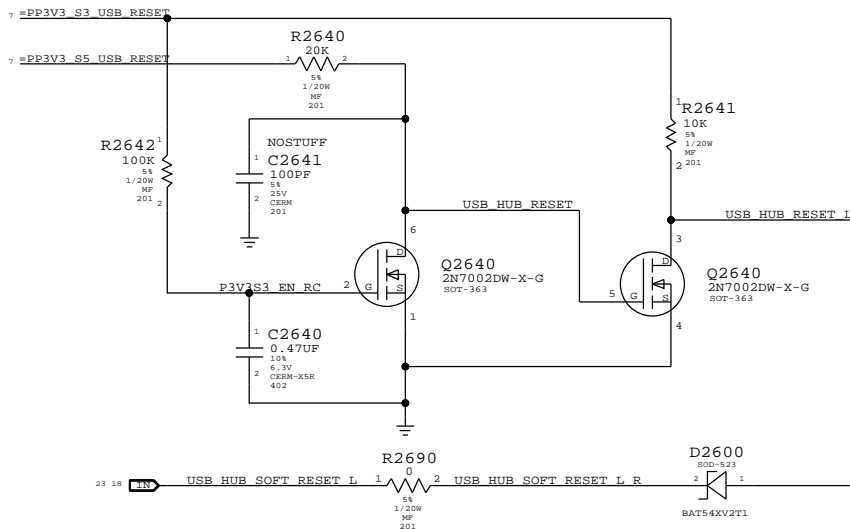
SYNC MASTER=K21 MLB		SYNC DATE=12/13/2016	
CPU & PCH XDP			
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM0, HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0, HUB1_NONREM1_1
HUB1_2NONREM	HUB1_NONREM1_1, HUB1_NONREM1_0
HUB1_3NONREM	HUB1_NONREM1_1, HUB1_NONREM1_1
HUB2_ALLREM	HUB2_NONREM0_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM1_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM1_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM1_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880720	2	SMSC USB2514	U2600, U2650	CRITICAL	USBHUB_2514
33880824	2	SMSC USB2514H	U2600, U2650	CRITICAL	USBHUB_2514H
33880923	2	SMSC USB2513B	U2600, U2650	CRITICAL	USBHUB_2513B



SYNC MASTER=K21 MLB SYNC DATE=12/13/2010

USB HUBS

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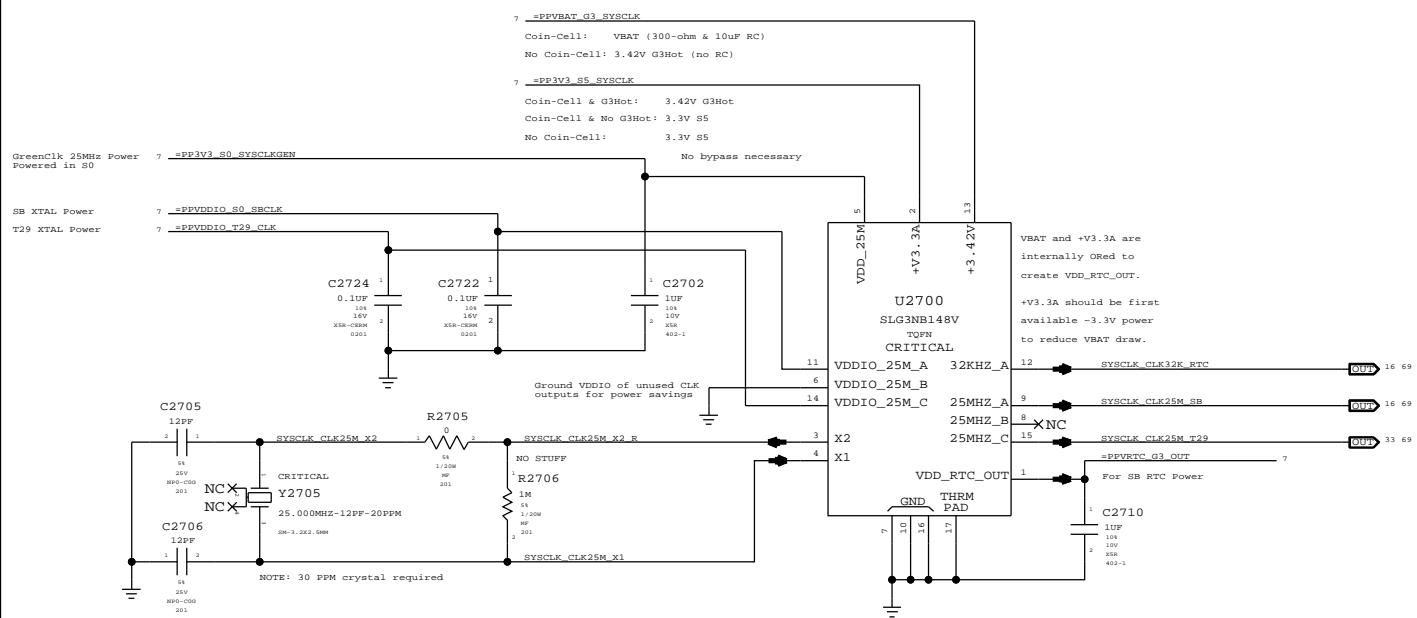
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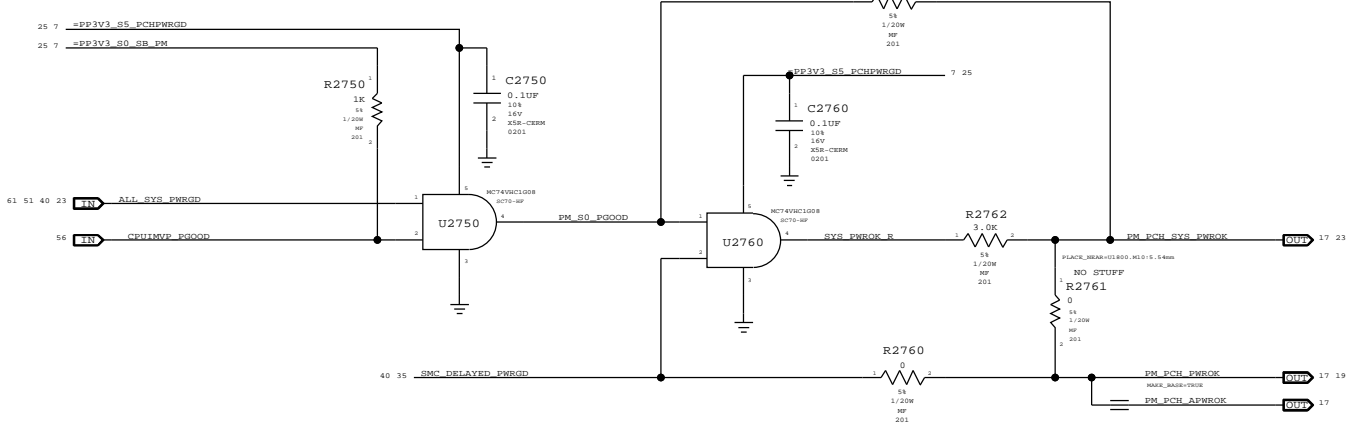
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System RTC Power Source & 32kHz / 25MHz Clock Generator

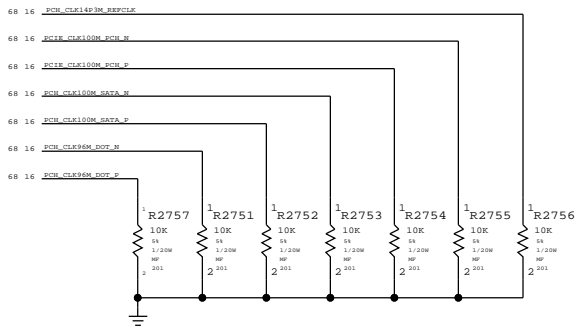


PCH S0 PWRGD

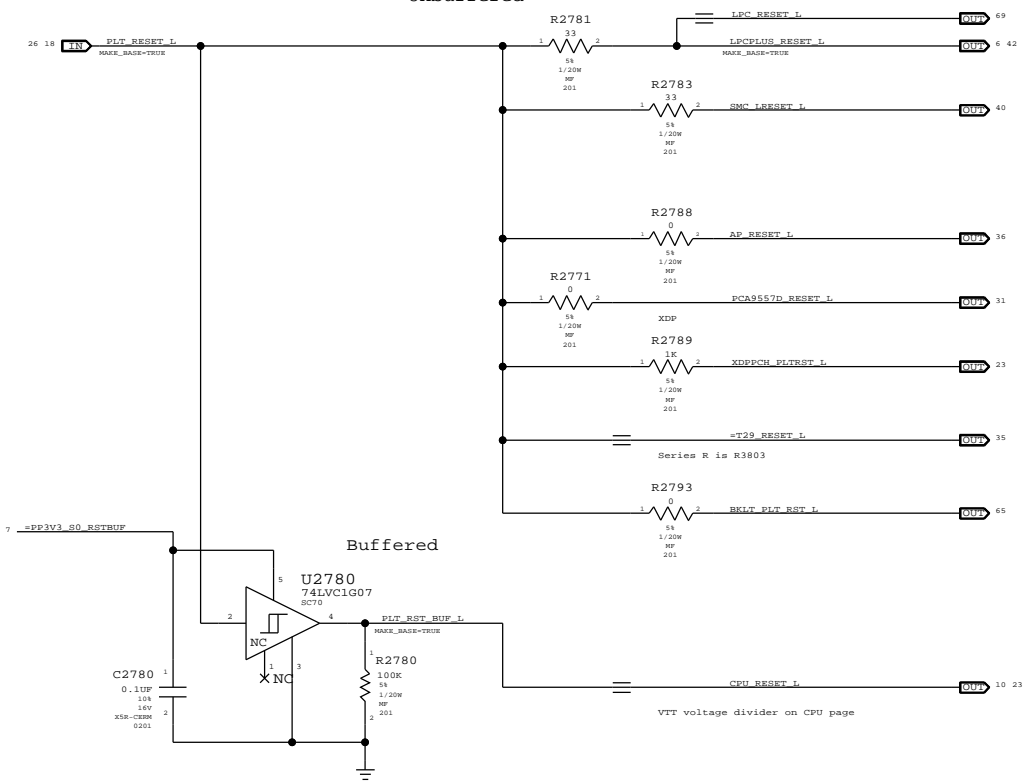


CLOCK (CK505)

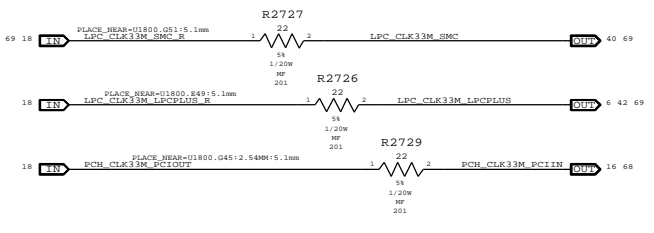
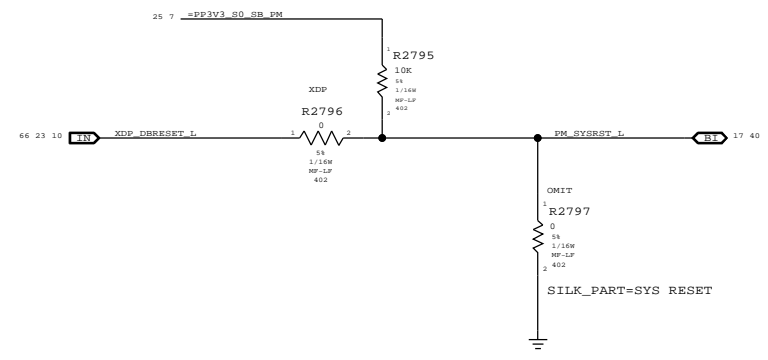
UNUSED clock terminations for PCIM MODE



Platform Reset Connections



PCH Reset Button



PAGE TITLE		DRAWING NUMBER		SIZE	
Clock (CK505) and Chipset Support		051-8871		D	
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

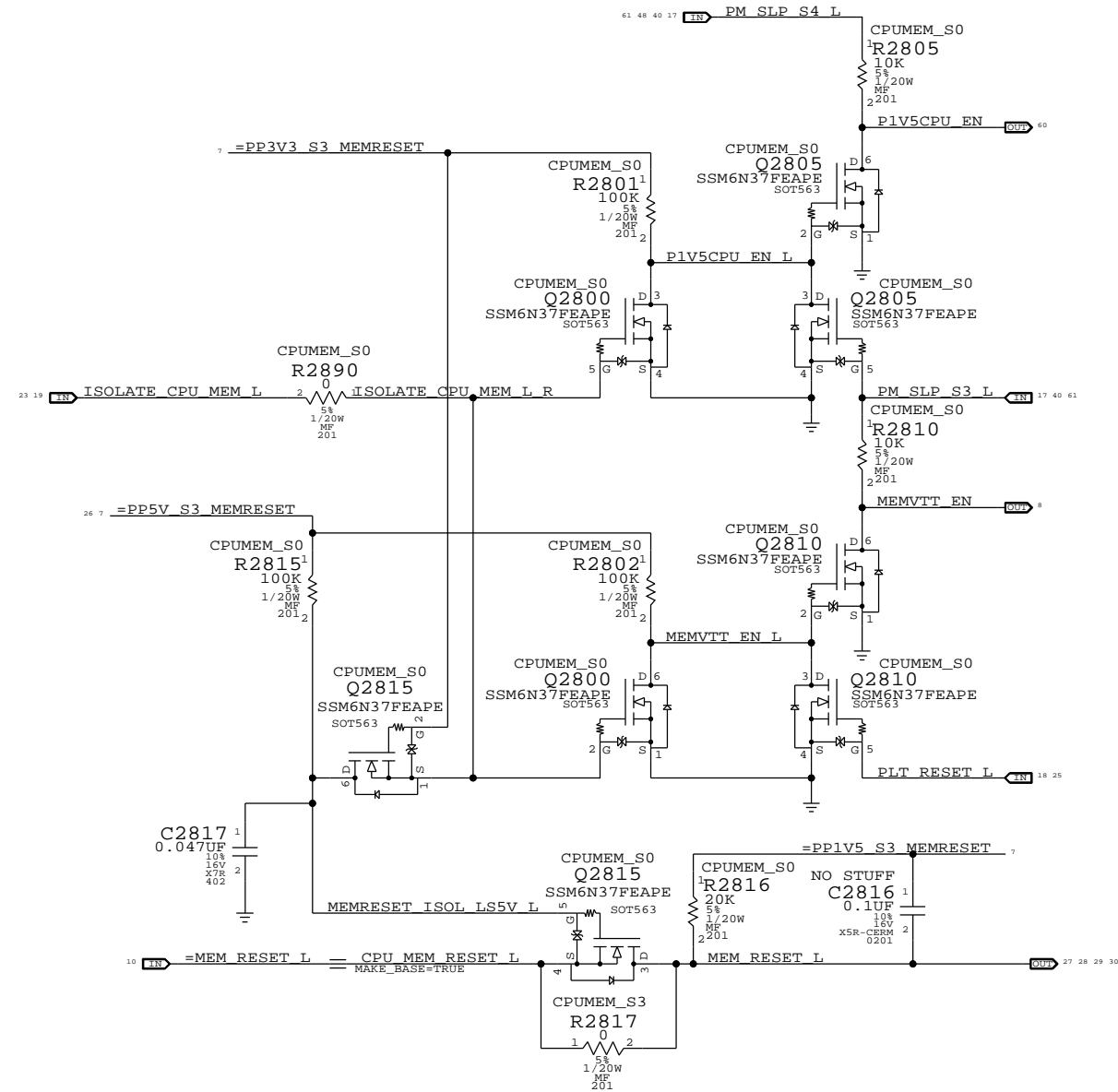
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

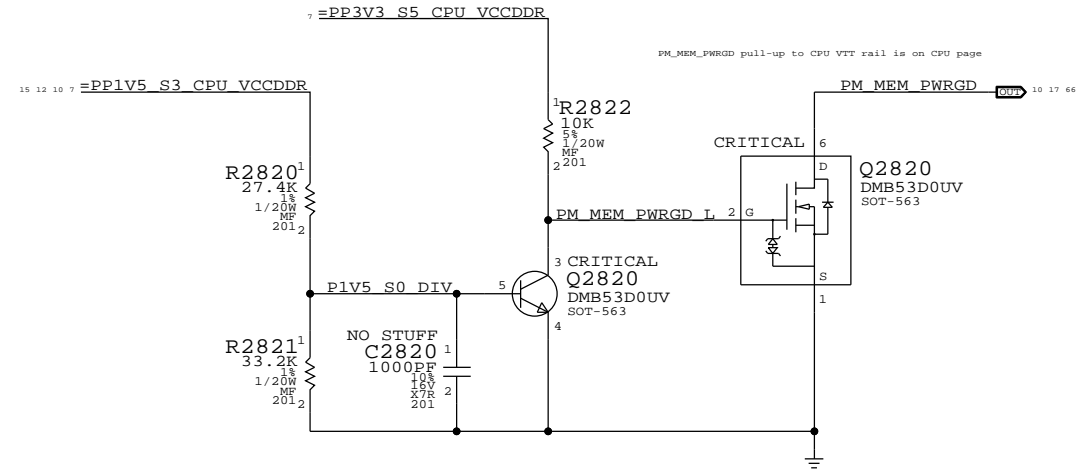
$P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L$

$MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L$

$MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L$

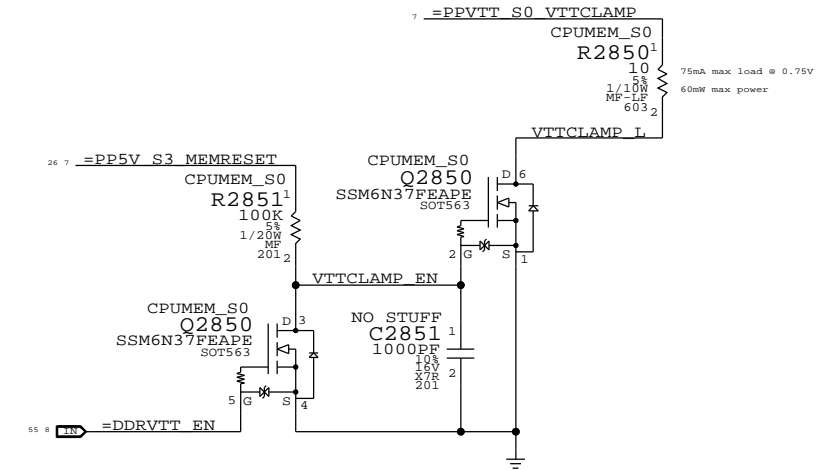


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3

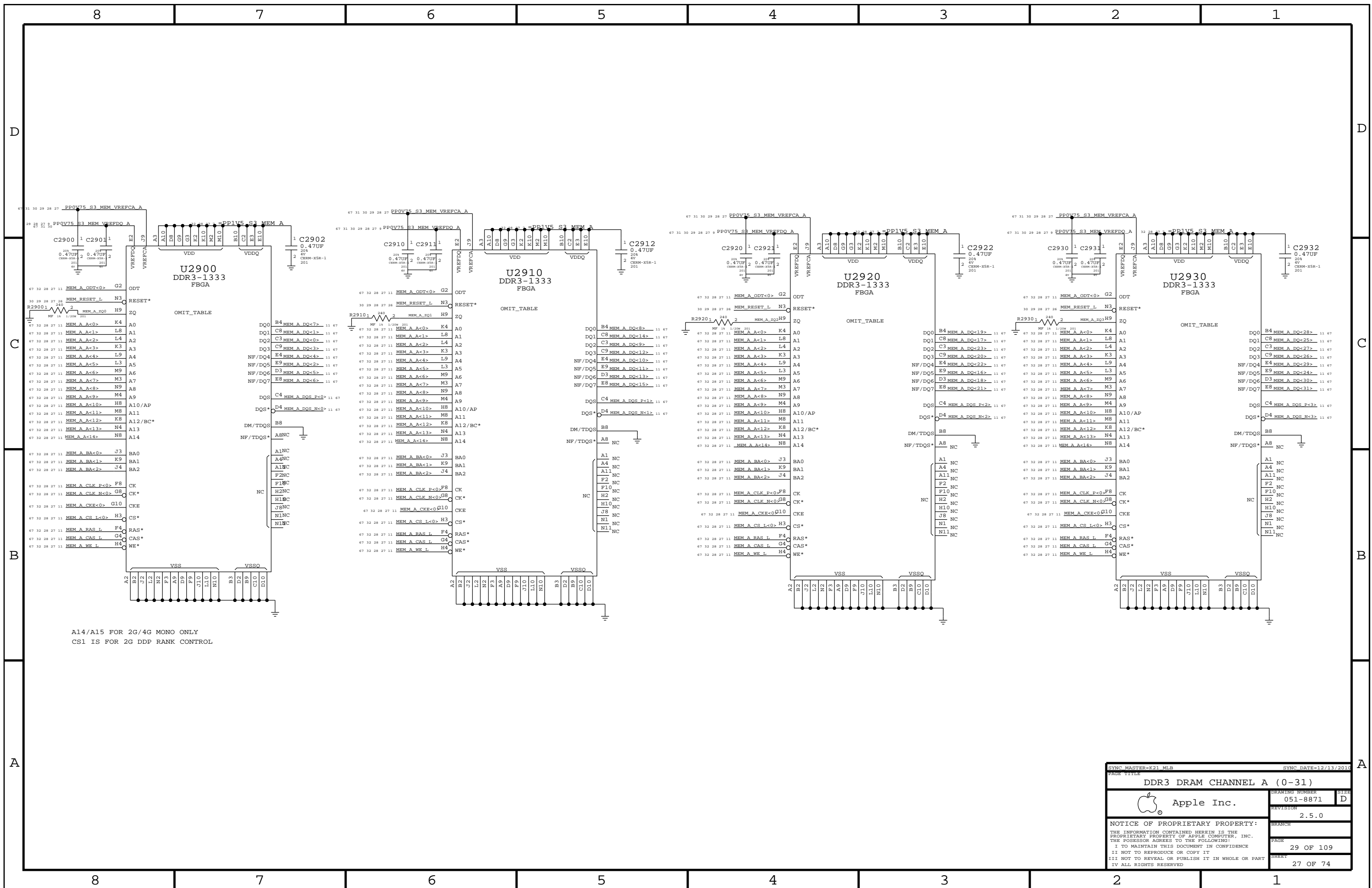


Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPUMEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPUMEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	0	1	1	0	0	1
3	0	0	0	1	X	0	0	1
S3	4	0	0	1	X	0	0	1
to	5	0	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPUMEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PMEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

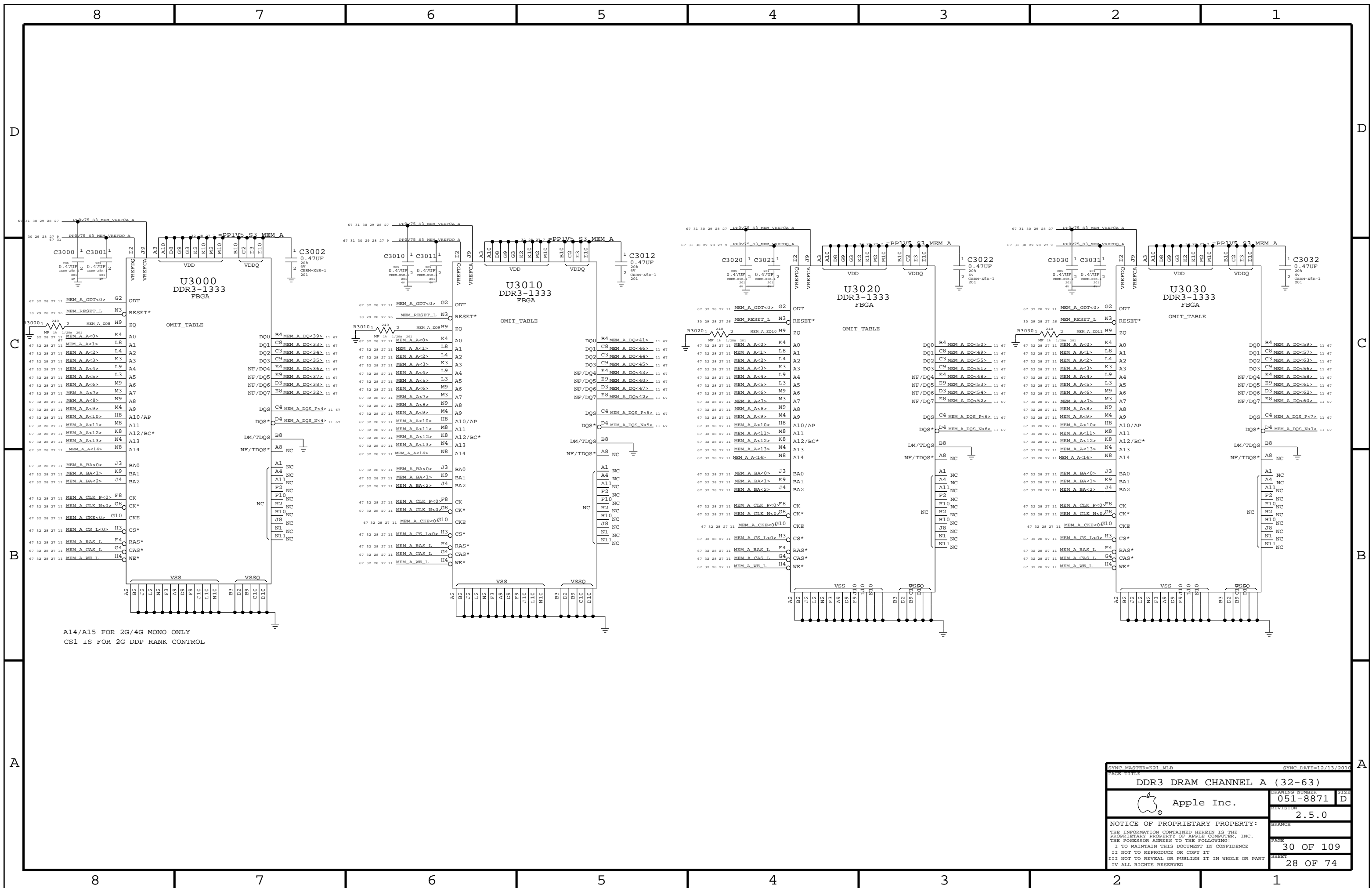
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

CPU Memory S3 Support		DRAWING NUMBER	051-8871	SIZE	D
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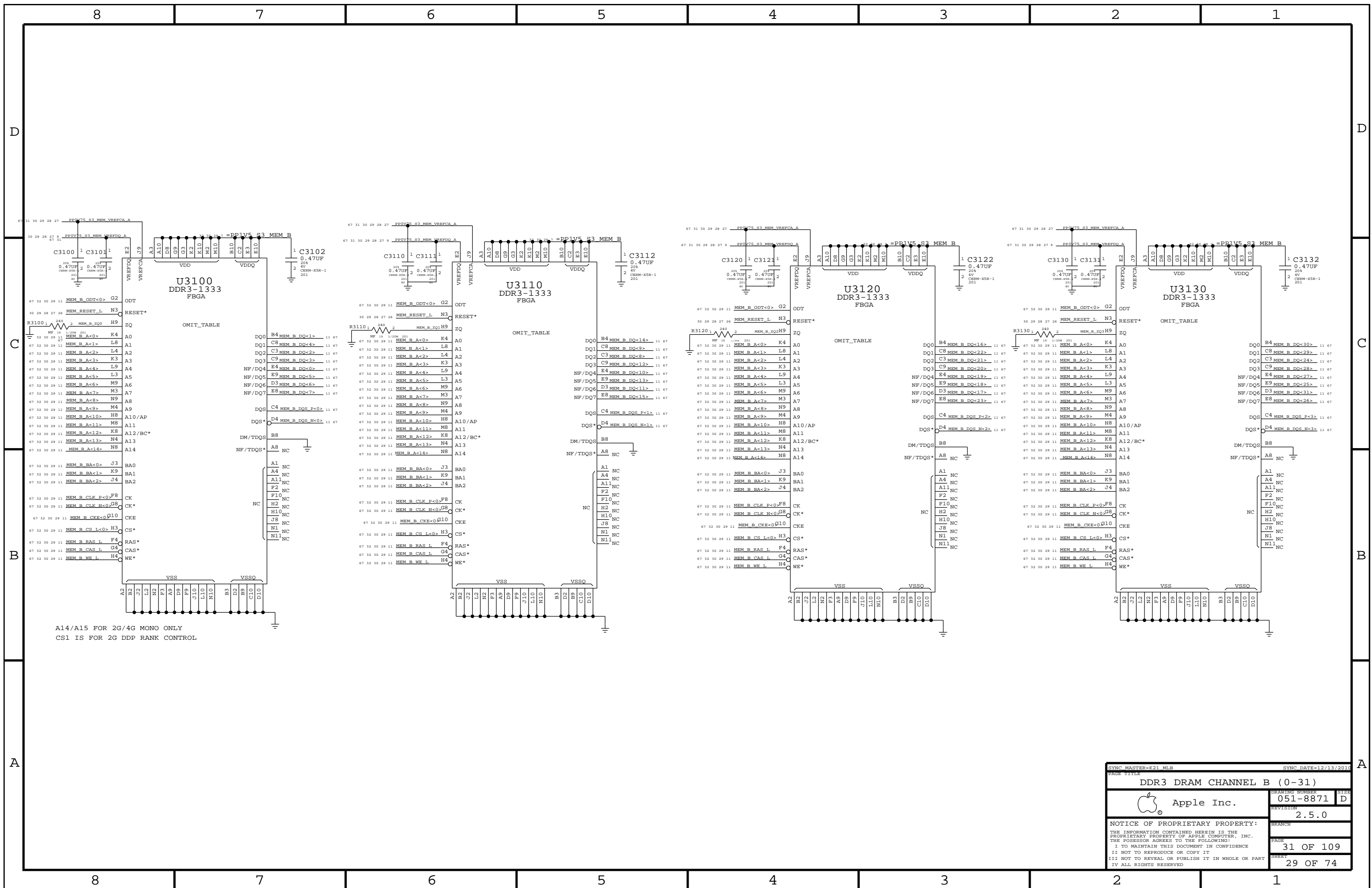
A14/A15 FOR 2G/4G MONO ONLY
 CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
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DDR3 DRAM CHANNEL A (0-31)			
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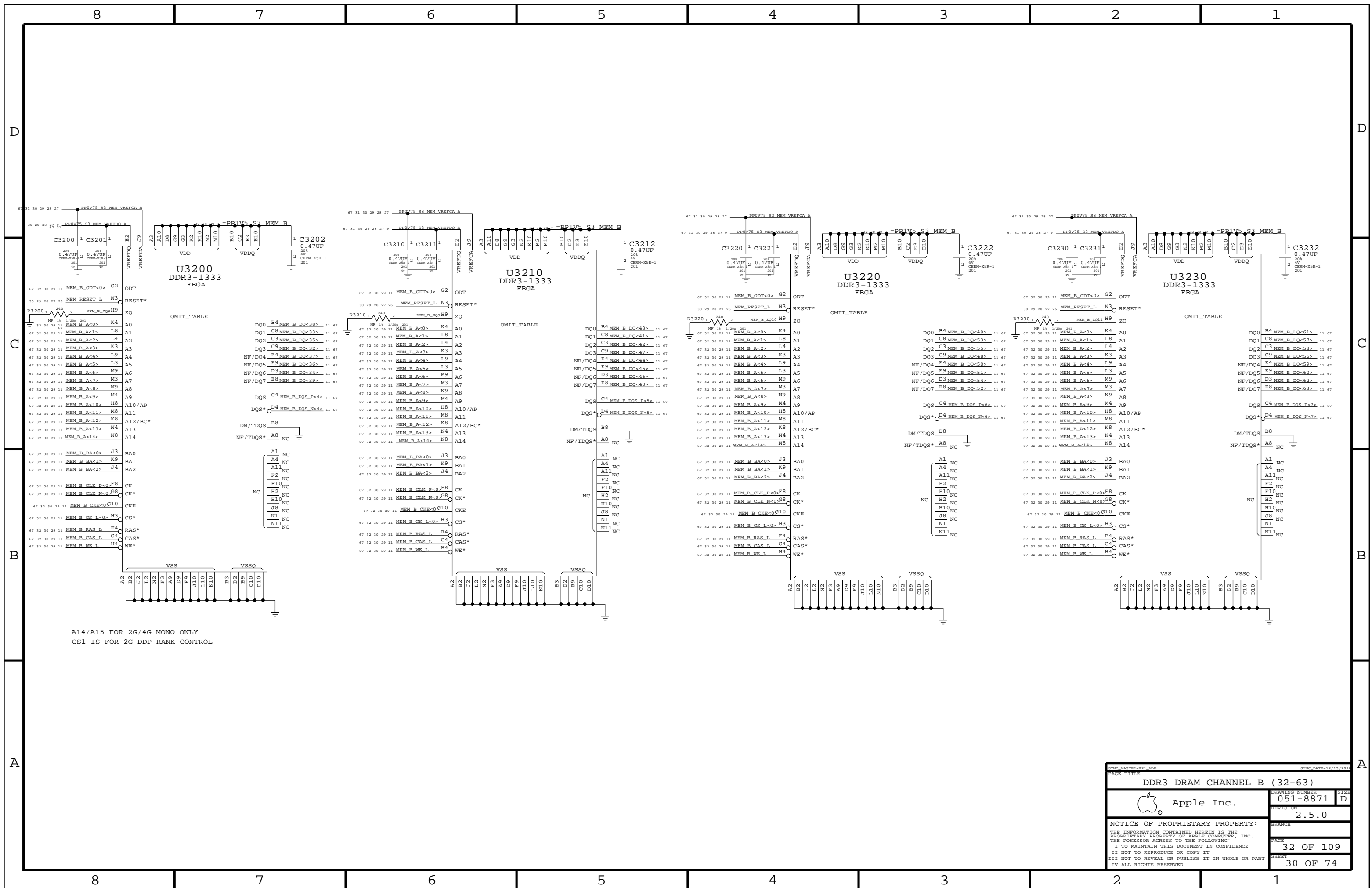
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PAGE TITLE			
DDR3 DRAM CHANNEL A (32-63)			
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SYMC_WAFFER=K11_MER
 SYMC_DATE=12/13/2011

DDR3 DRAM CHANNEL B (32-63)

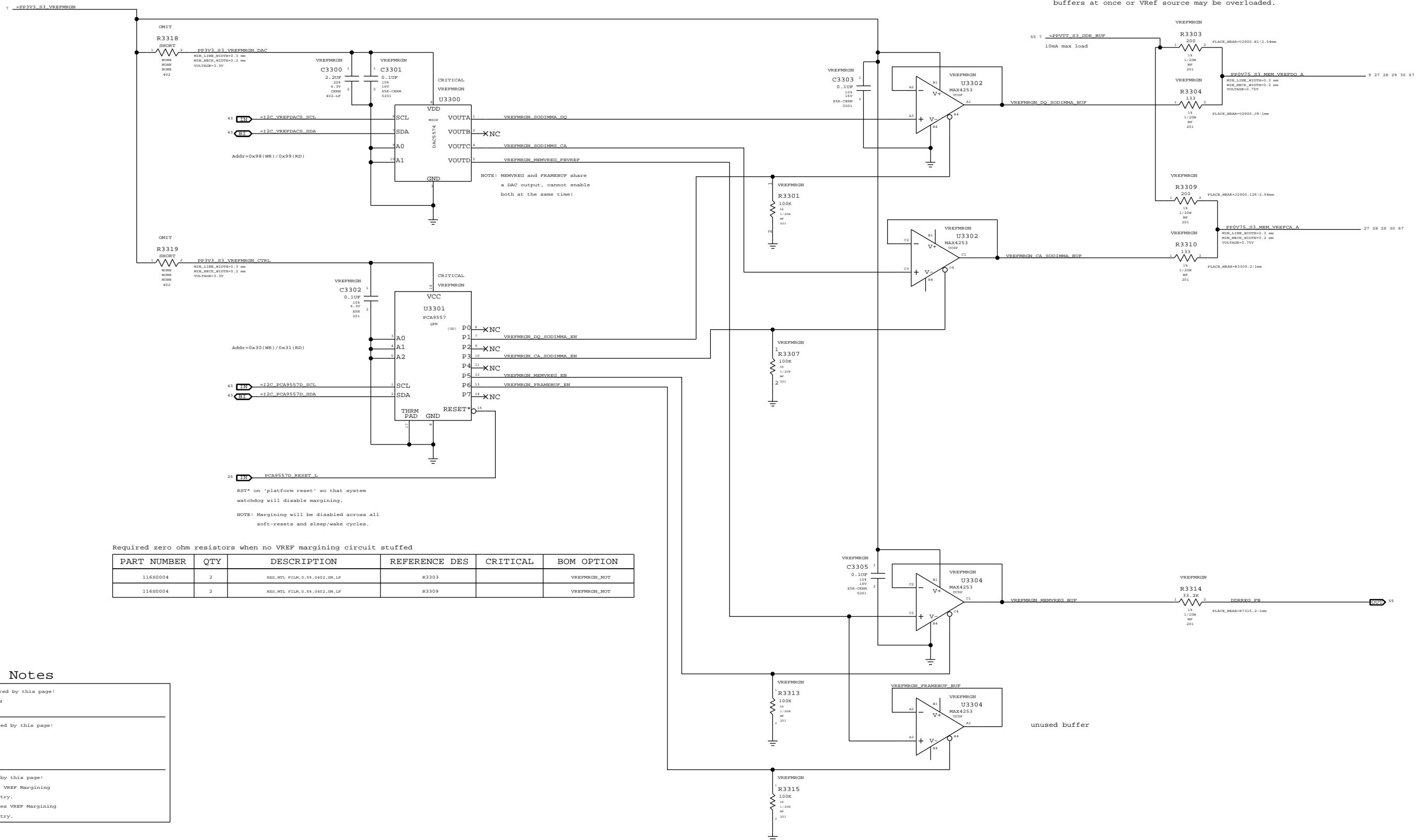
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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuitry stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11680004	2	RES_MTL_FILM,0.5%,0402,SM,LF	R3303		VREFMGRN_NOT
11680004	2	RES_MTL_FILM,0.5%,0402,SM,LF	R3309		VREFMGRN_NOT

Page Notes

Power aliases required by this page:
 - #PP3V3_S3_VREFMGRN
 - #PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - #I2C_VREFDACS_SCL
 - #I2C_VREFDACS_SDA
 - #I2C_PCA9557D_SCL
 - #I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMGRN - Stuffs VREF Margining Circuitry.
 VREFMGRN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC current:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

SYNOPSIS: FSB/DDR3/FB/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER: 051-8871

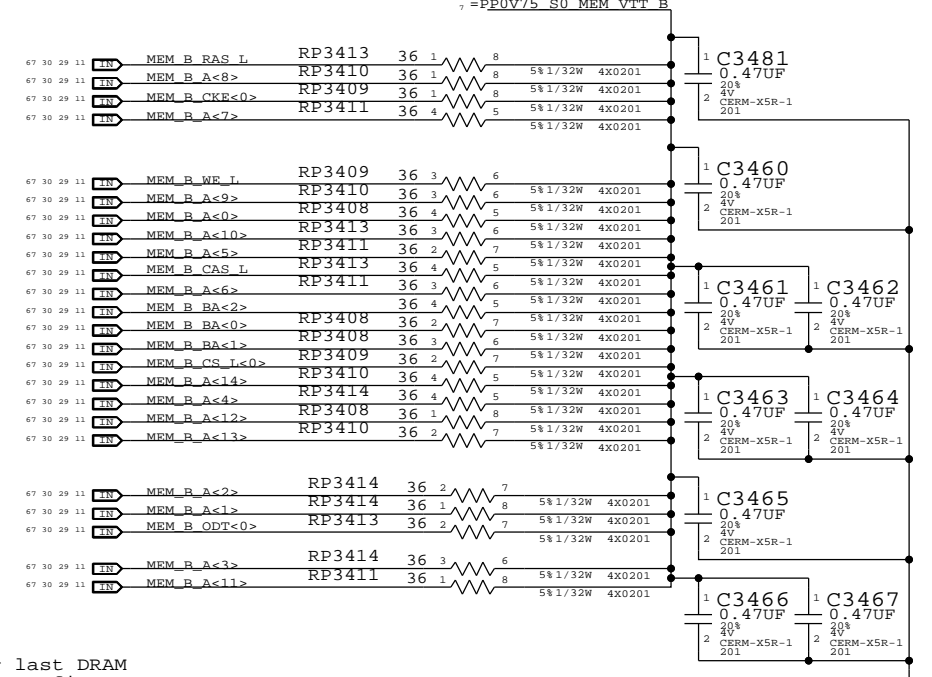
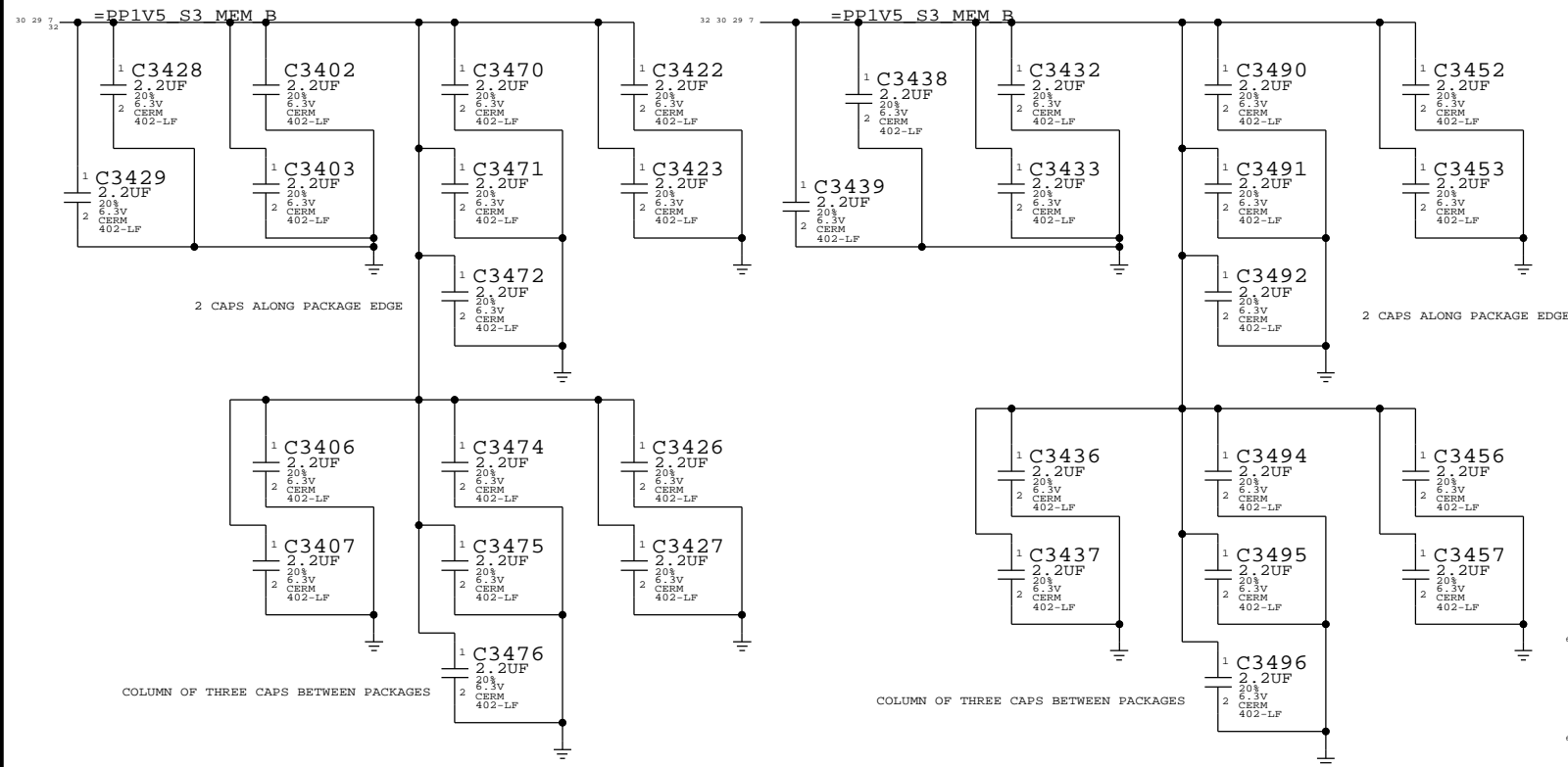
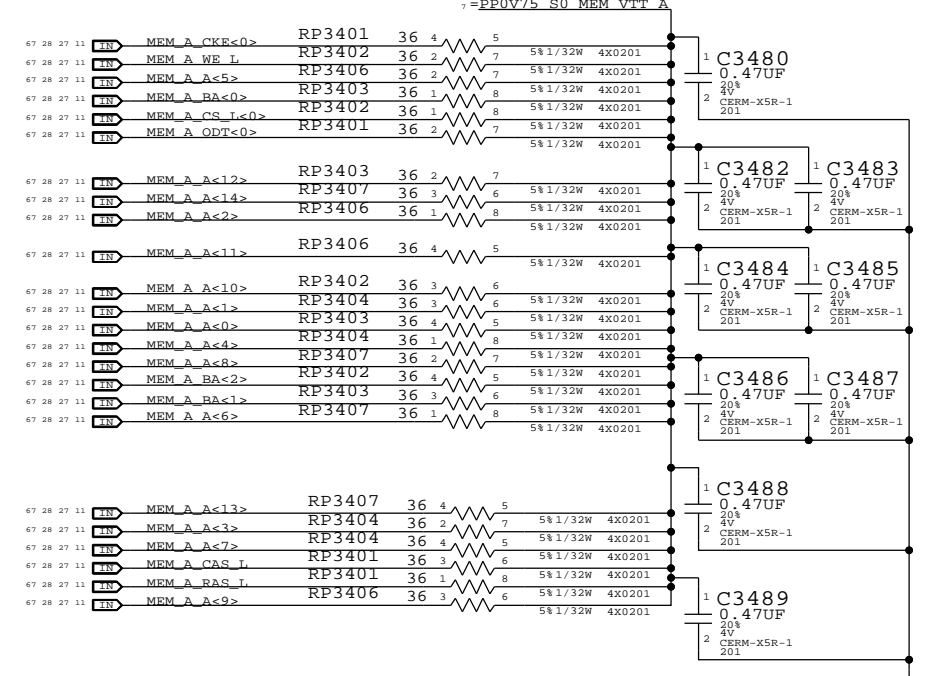
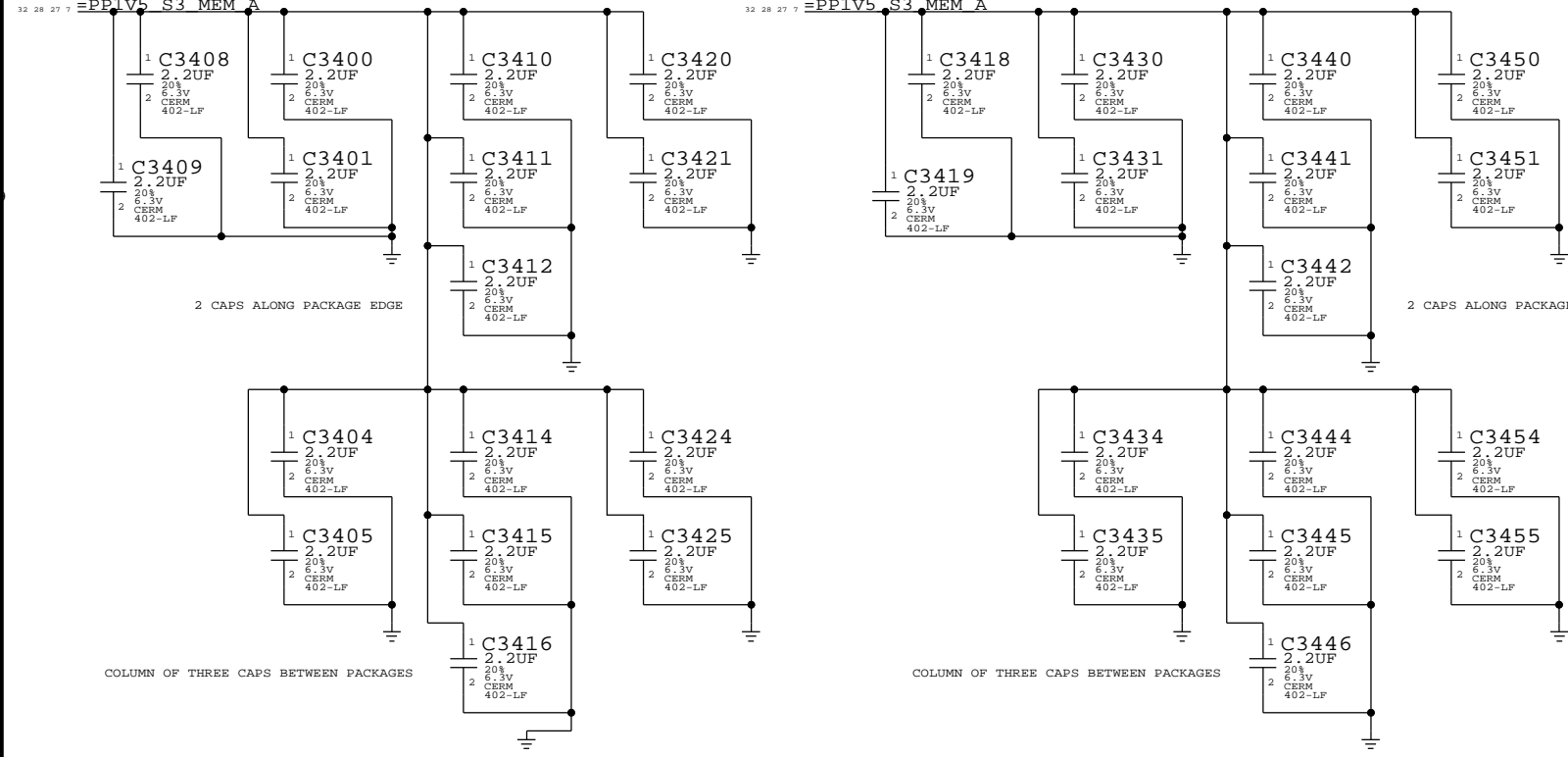
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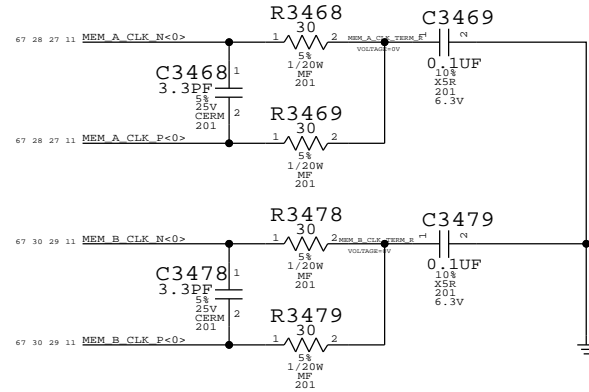
PAGE: 33 OF 109

SHEET: 31 OF 74

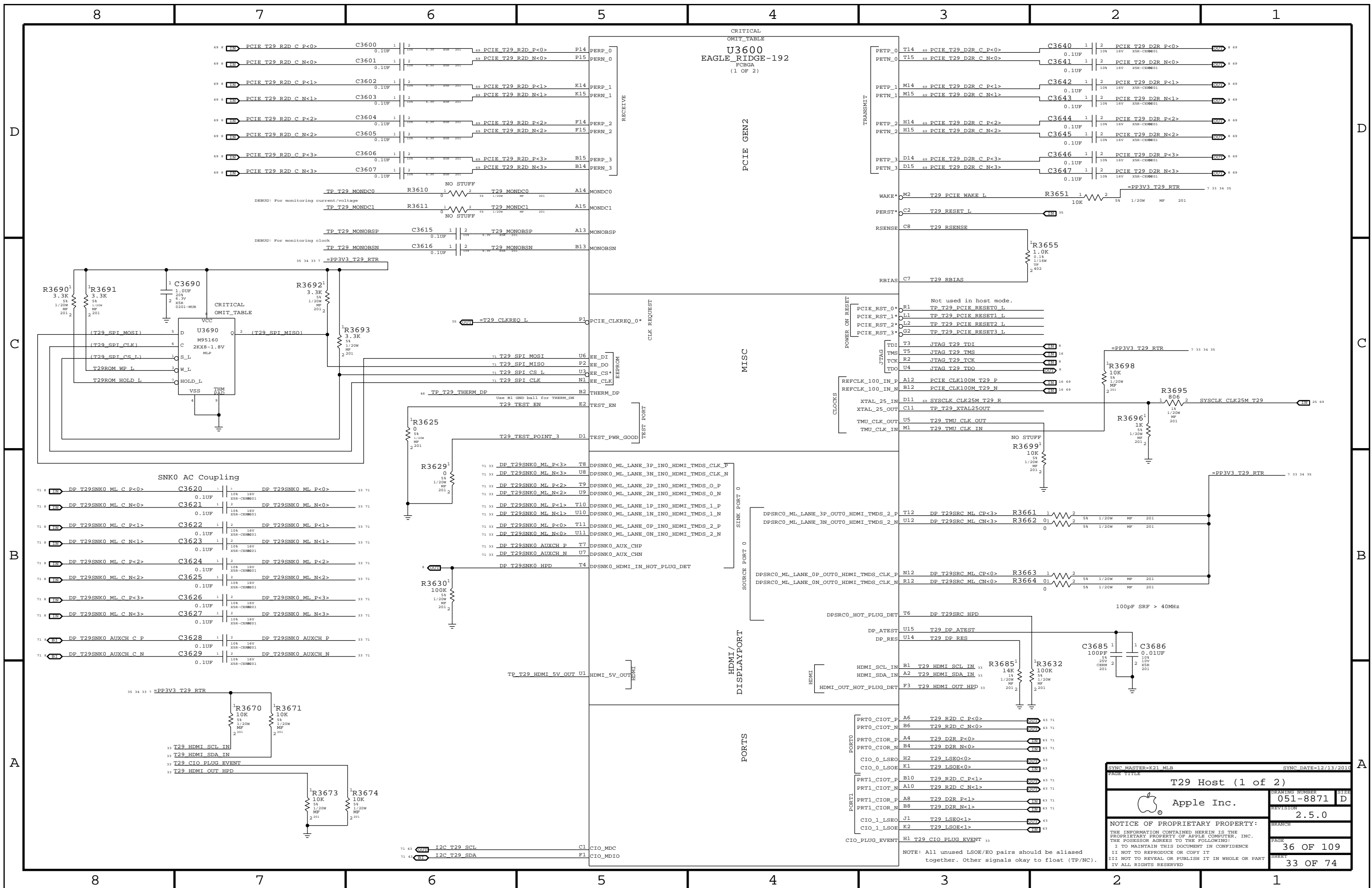
JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



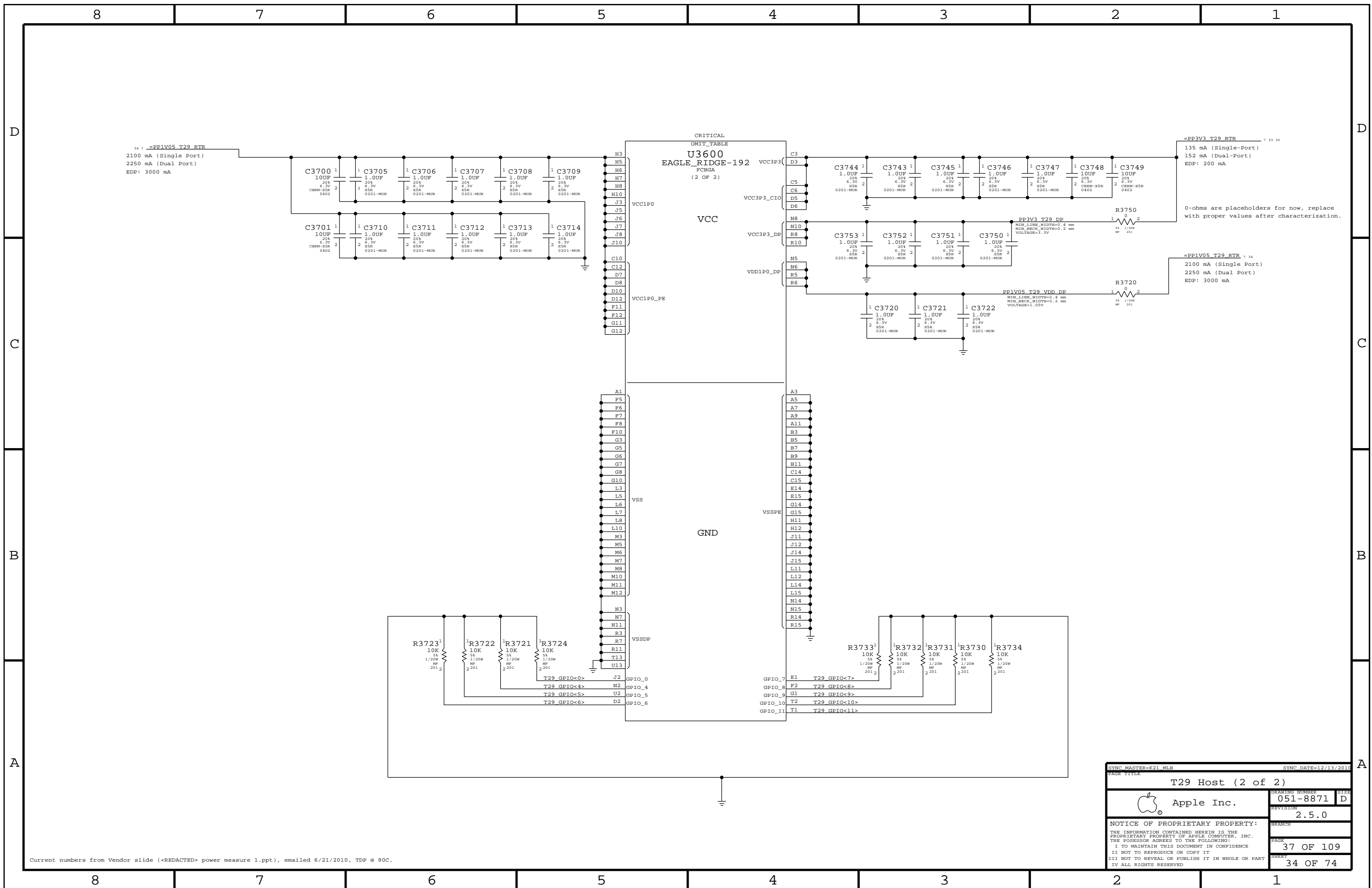
SYNC MASTER=K21 MLB		SYNC DATE=12/13/2011	
PAGE TITLE			
DDR3 DRAM Channel B (32-63)			
Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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		PAGE	34 OF 109
		SHEET	32 OF 74



CRITICAL OMIT_TABLE
U3600
EAGLE RIDGE-192
 PCBGA
 (1 OF 2)

PAGE TITLE		SYNC DATE=12/13/2011	
T29 Host (1 of 2)			
 Apple Inc.	DRAWING NUMBER	051-8871	SIZE
	REVISION	2.5.0	
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PAGE	36 OF 109		SHEET
		33 OF 74	

NOTE: All unused LSEO/EO pairs should be aliased together. Other signals may be aliased to float (TP/NC).



34 7 =PP1V05 T29_RTR
 2100 mA (Single Port)
 2250 mA (Dual Port)
 EDP: 3000 mA

=PP3V3 T29_RTR 7 33 35
 135 mA (Single-Port)
 152 mA (Dual-Port)
 EDP: 200 mA

0-ohms are placeholders for now, replace with proper values after characterization.

=PP1V05 T29_RTR 7 34
 2100 mA (Single Port)
 2250 mA (Dual Port)
 EDP: 3000 mA

R3723¹
 10K
 5%
 1/20W
 MF
 201 2

R3722¹
 10K
 5%
 1/20W
 MF
 201

R3721¹
 10K
 5%
 1/20W
 MF
 201

R3724¹
 10K
 5%
 1/20W
 MF
 201

R3733¹
 10K
 5%
 1/20W
 MF
 201 2

R3732¹
 10K
 5%
 1/20W
 MF
 201

R3731¹
 10K
 5%
 1/20W
 MF
 201

R3730¹
 10K
 5%
 1/20W
 MF
 201

R3734¹
 10K
 5%
 1/20W
 MF
 201

SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
PAGE TITLE T29 Host (2 of 2)			
Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
	REVISION	2.5.0	
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		PAGE	37 OF 109
		SHEET	34 OF 74

Page Notes

Power aliases required by this page:

- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

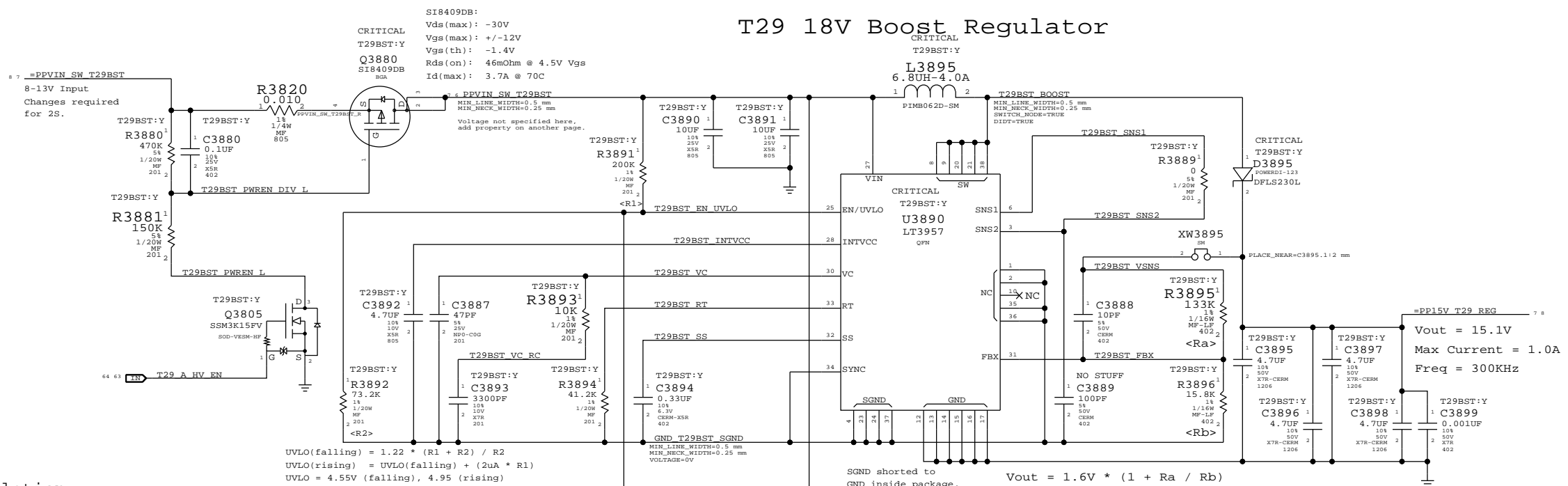
Signal aliases required by this page:

- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:

- T29BST:Y - Stuffs 18V boost circuitry.

T29 18V Boost Regulator



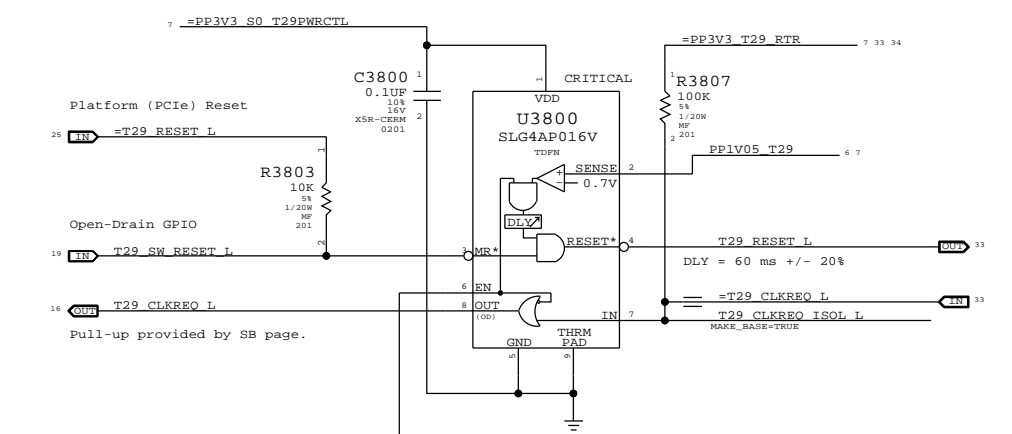
$$UVLO(\text{falling}) = 1.22 * (R1 + R2) / R2$$

$$UVLO(\text{rising}) = UVLO(\text{falling}) + (2\mu A * R1)$$

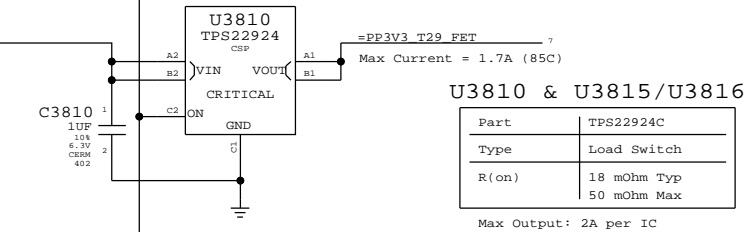
$$UVLO = 4.55V (\text{falling}), 4.95V (\text{rising})$$

$$V_{out} = 1.6V * (1 + R_a / R_b)$$

Supervisor & CLKREQ# Isolation



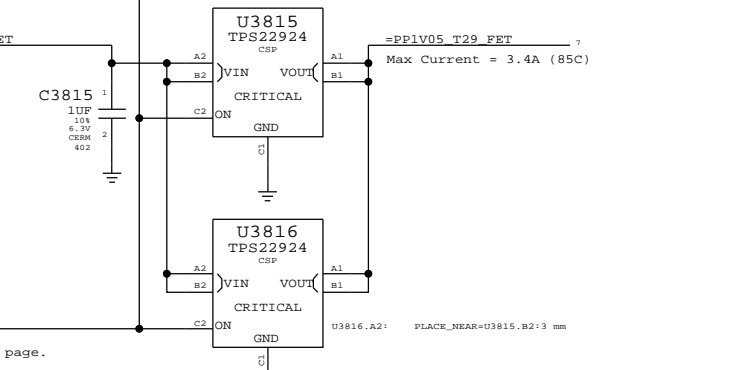
3.3V T29 Switch



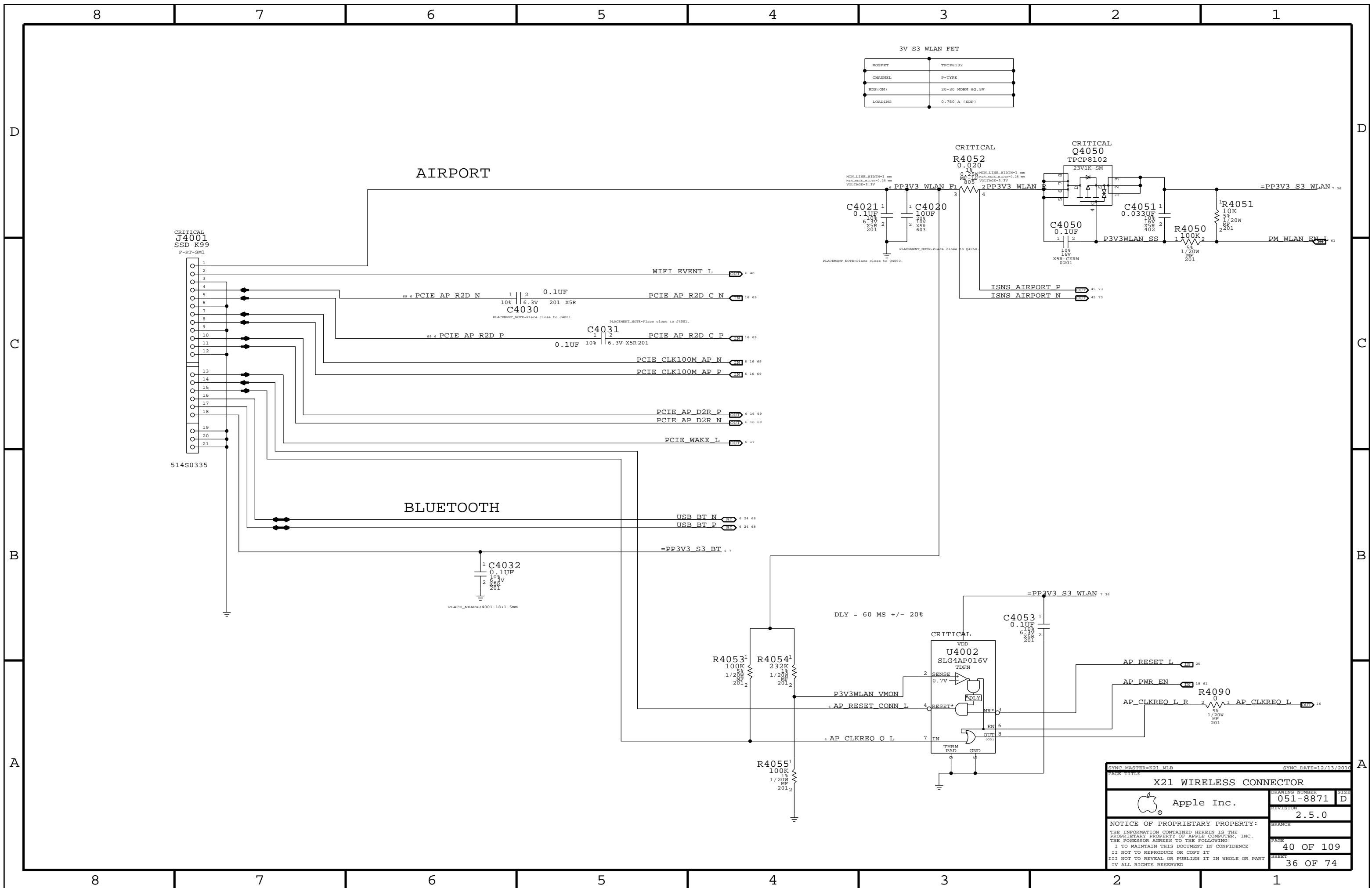
U3810 & U3815/U3816

Part	TPS22924
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
Max Output	2A per IC

1.05V T29 Switch




SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
T29 Power Support			
Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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		SHEET	35 OF 74

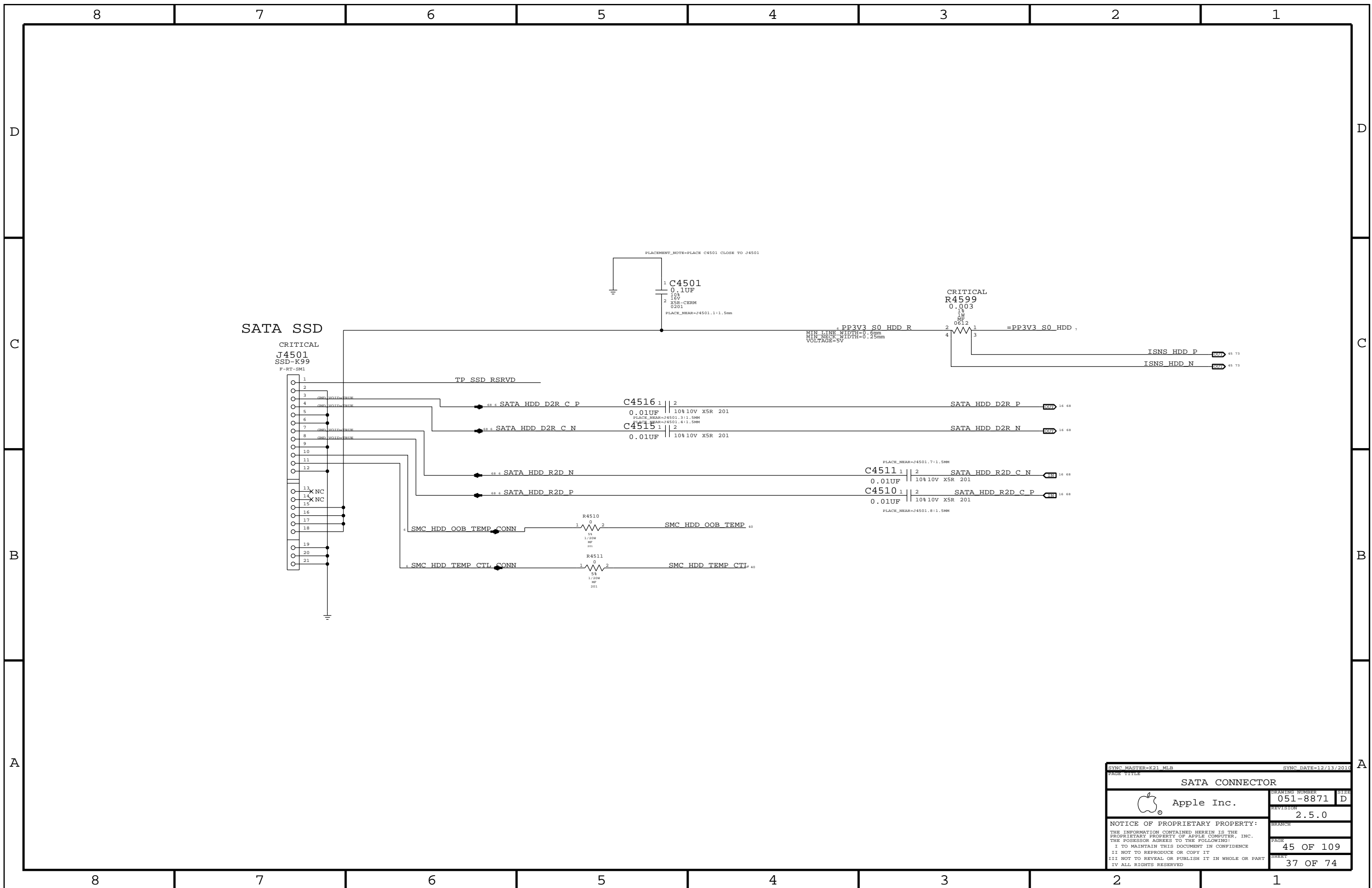


3V S3 WLAN FET	
MOUSEFET	TPCP8102
CHANNEL	P-TYPE
RDS (ON)	20-30 MOHM @2.5V
LOADING	0.750 A (RDP)

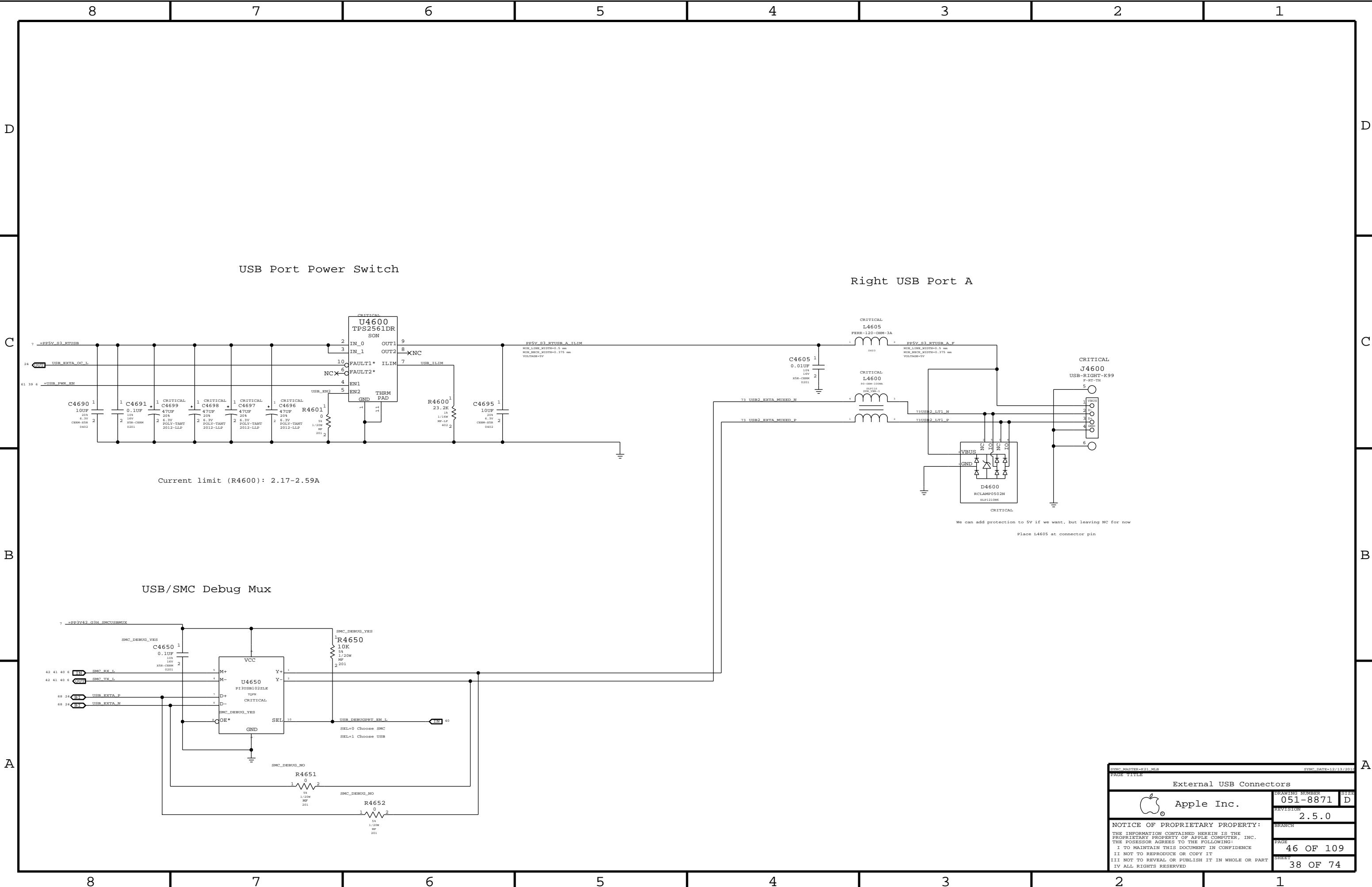
AIRPORT

BLUETOOTH

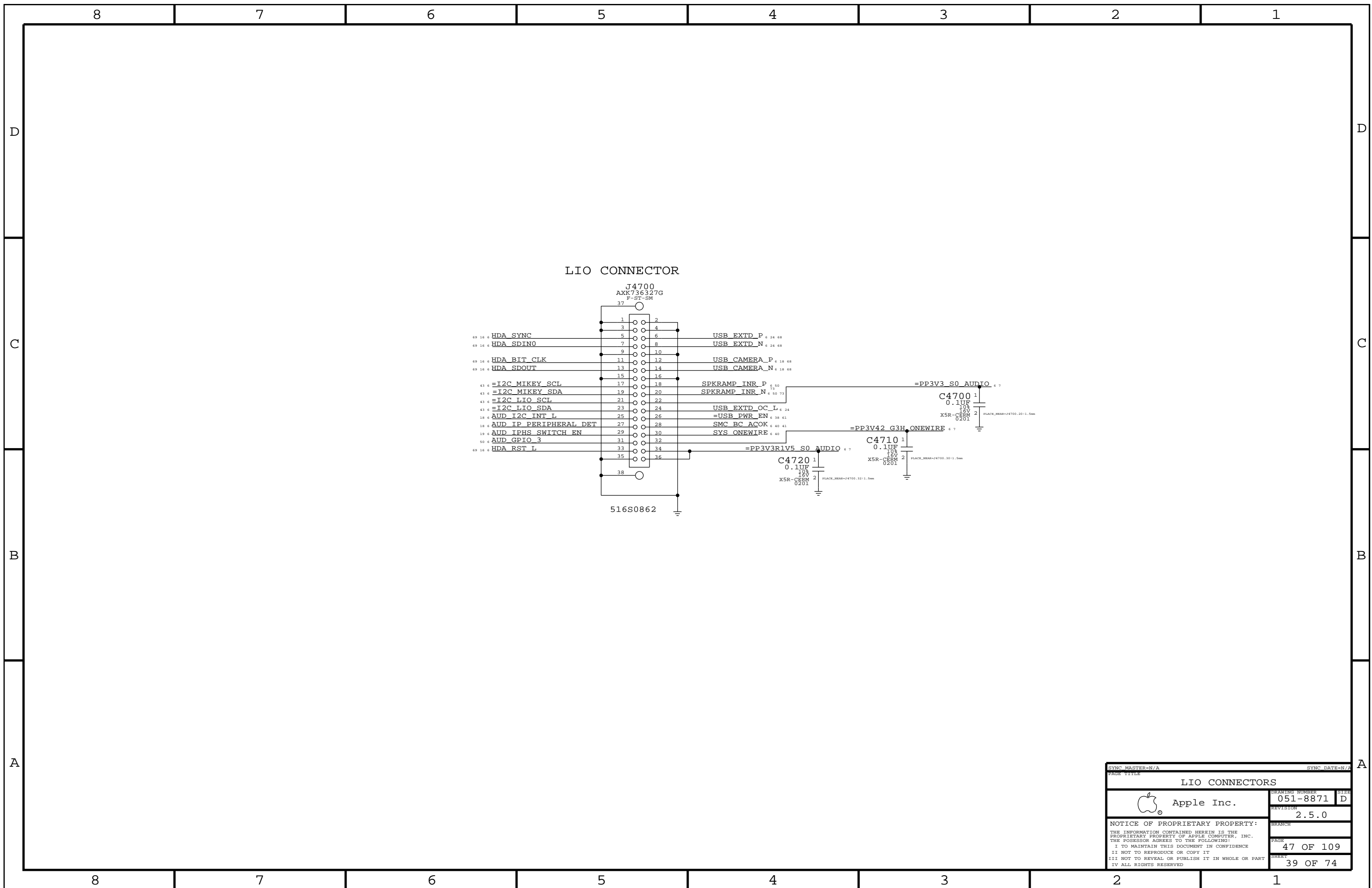
SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
X21 WIRELESS CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8871
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PAGE TITLE			
SATA CONNECTOR		DRAWING NUMBER	SIZE
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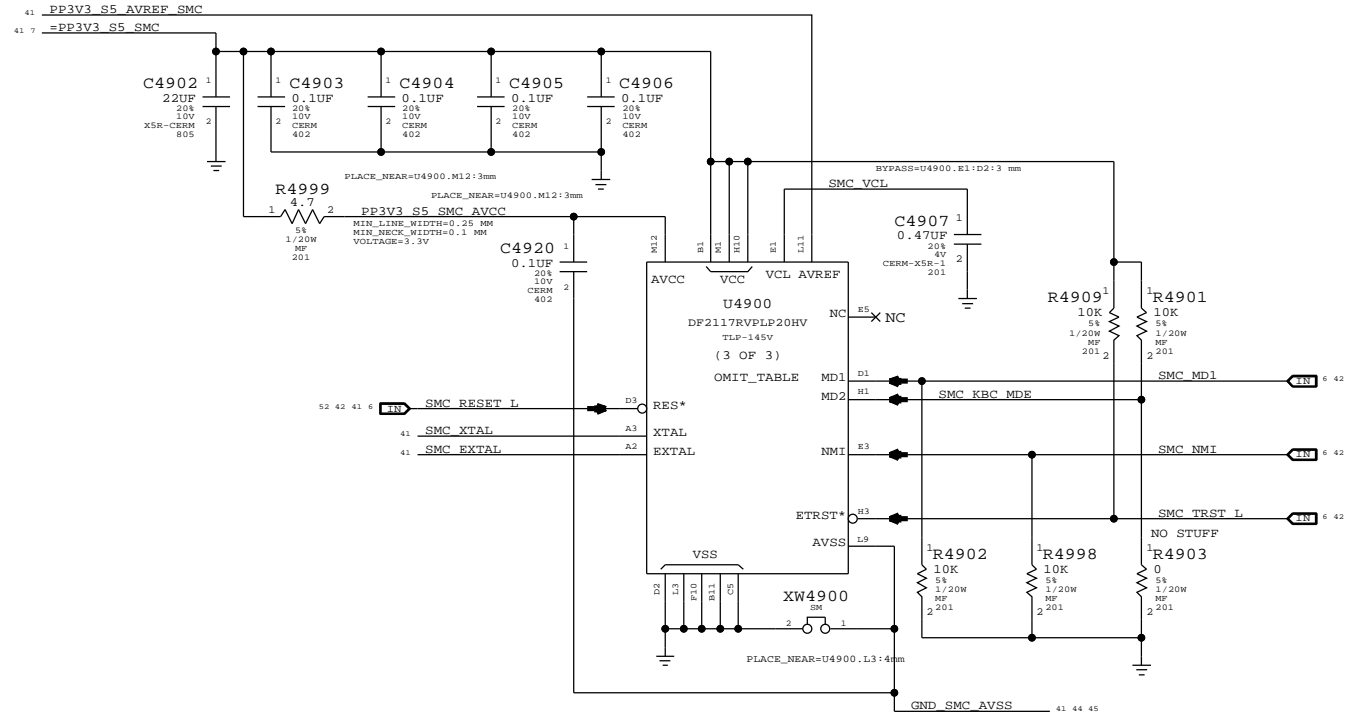
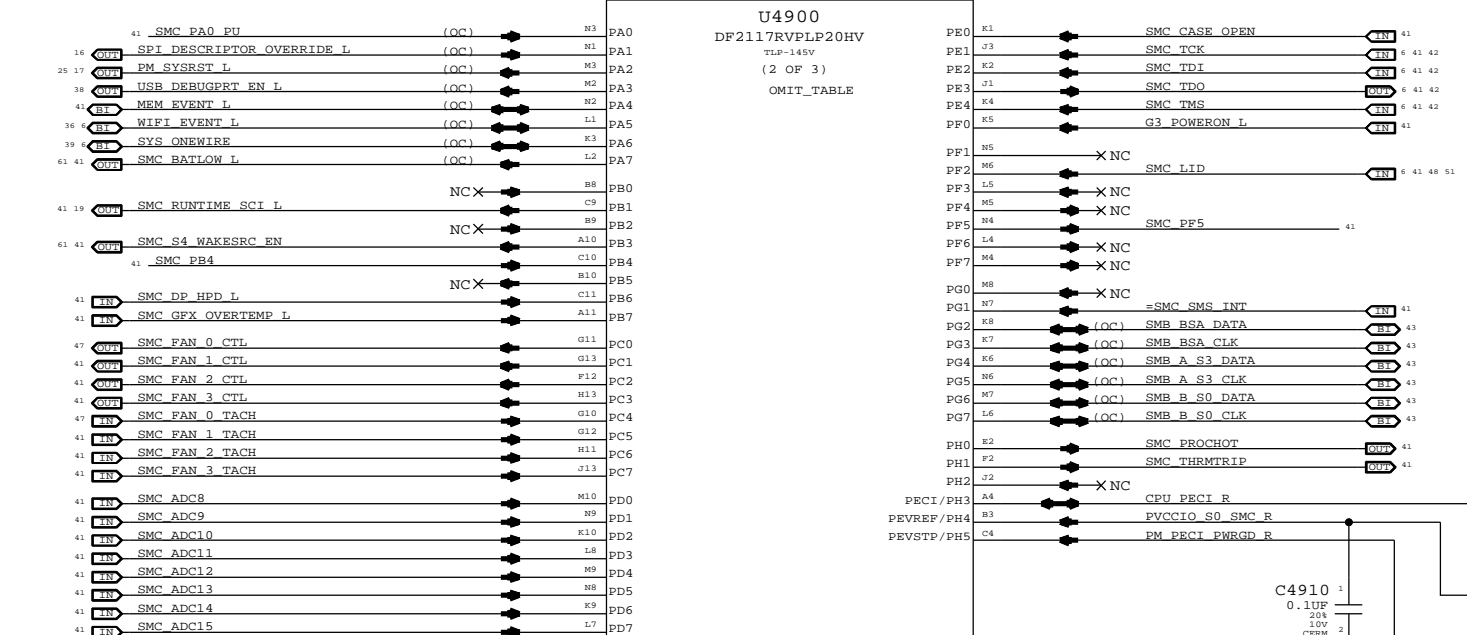
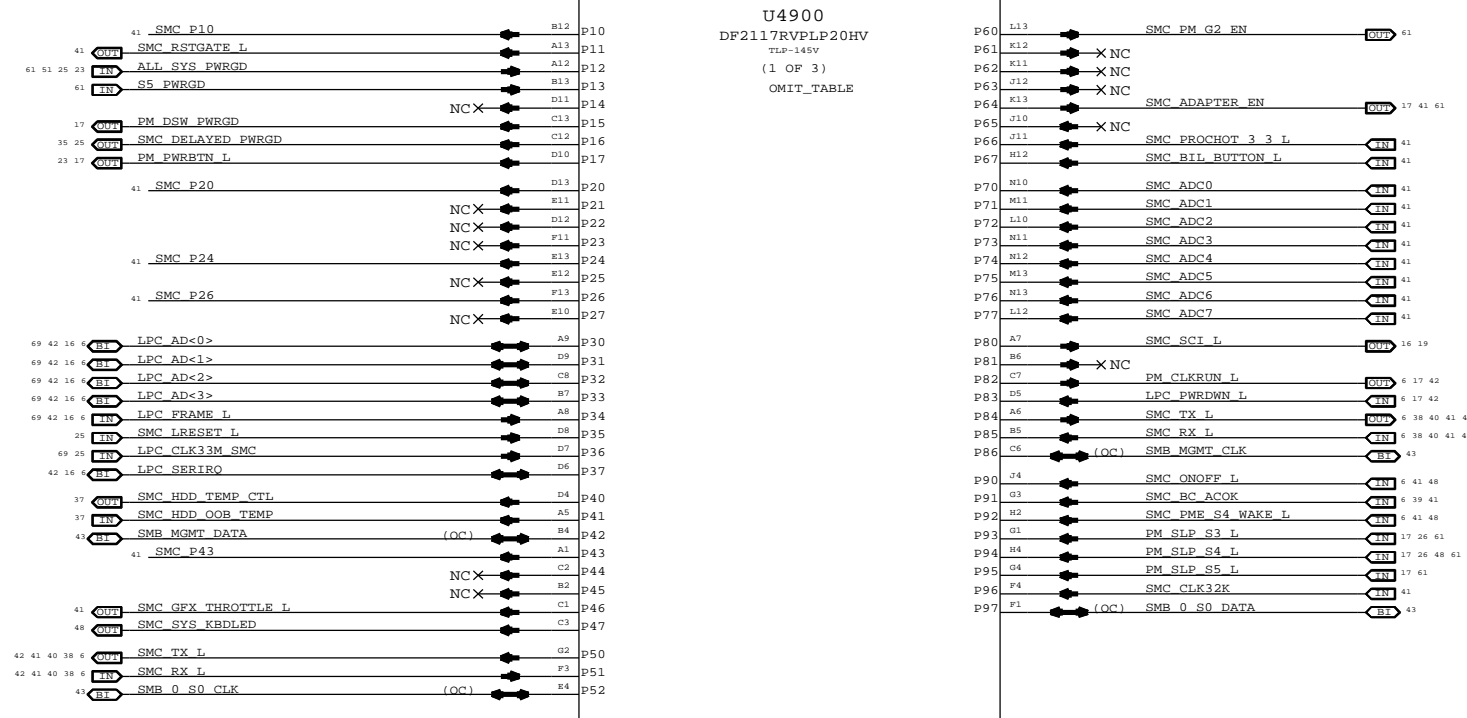


SYMC_MASTER_K11_MCB		SYMC_DATE=12/13/2015	
External USB Connectors			
Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
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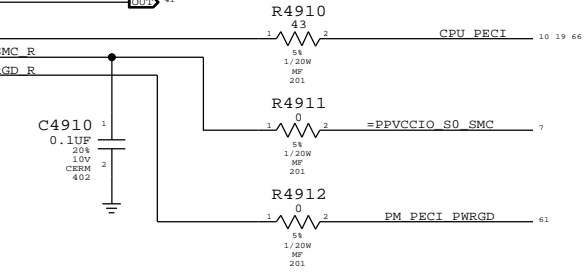


SYNC MASTER=N/A		SYNC DATE=N/A	
LIO CONNECTORS			
Apple Inc.		DRAWING NUMBER	051-8871
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		PAGE	47 OF 109
		SHEET	39 OF 74

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

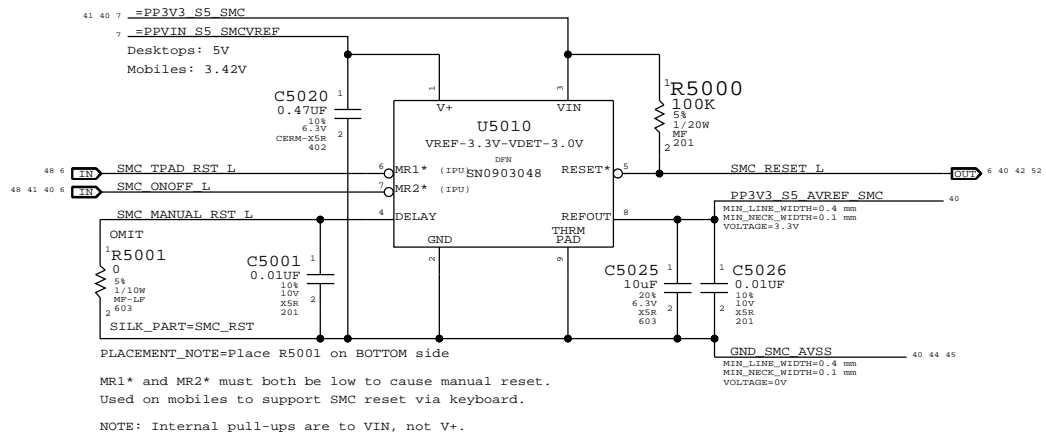


NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

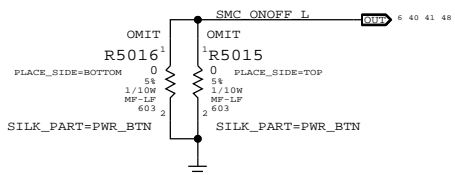


SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
SMC			
Apple Inc.		DRAWING NUMBER	SIZE
Apple logo		051-8871	D
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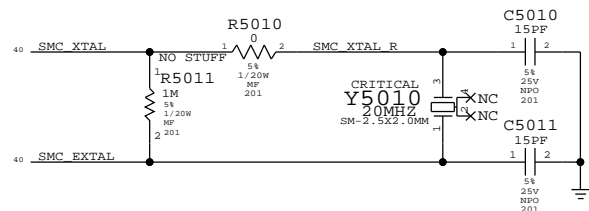
SMC Reset "Button", Supervisor & AVREF Supply



Debug Power "Buttons"

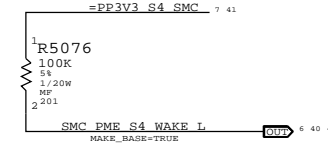
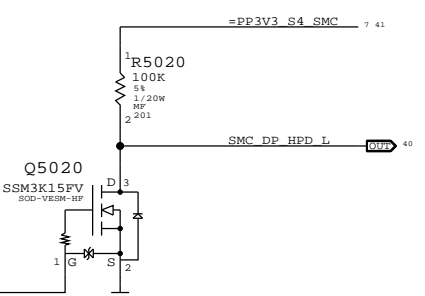
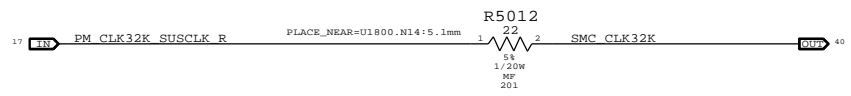
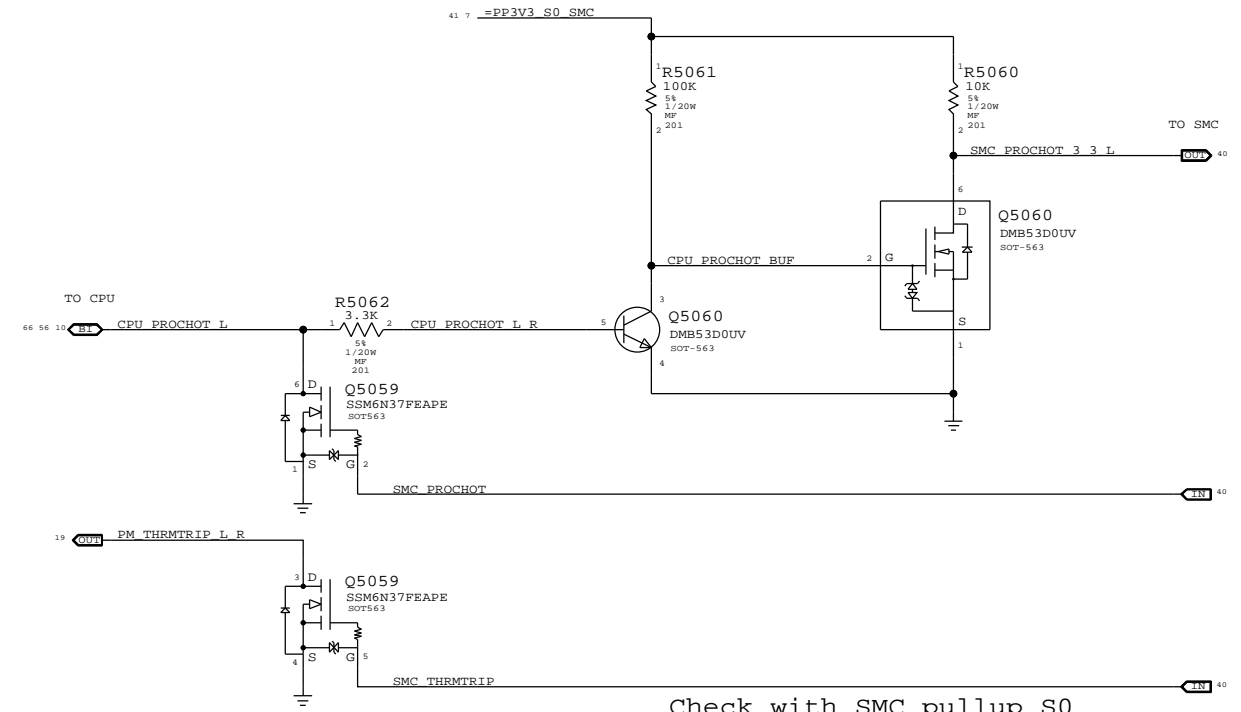


SMC Crystal Circuit



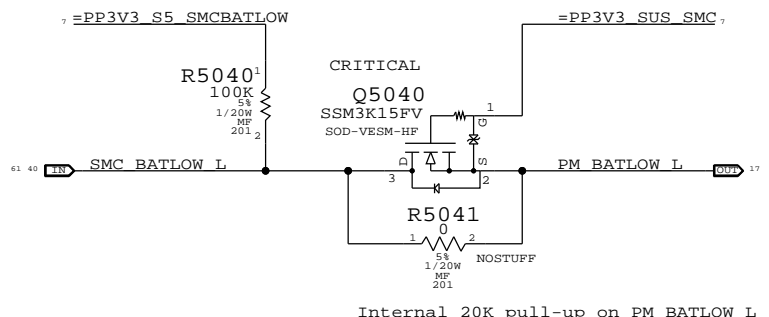
40	_SMC_FAN_2_CTL	==	NC_SMC_FAN_2_CTL	40
40	_SMC_FAN_2_TACH	==	NC_SMC_FAN_2_TACH	40
40	_SMC_FAN_3_CTL	==	NC_SMC_FAN_3_CTL	40
40	_SMC_FAN_3_TACH	==	NC_SMC_FAN_3_TACH	40
54	_CHGR_ACOK	==	SMC_BC_ACOK	6 39 40 41
40	_SMC_SMS_INT	==	SMC_INT_L	44
40	_SMC_ADC0	==	SMC_CPU_VSENSE	44
40	_SMC_ADC1	==	SMC_CPU_ISENSE	44
40	_SMC_ADC2	==	SMC_DCIN_VSENSE	44
40	_SMC_ADC3	==	SMC_DCIN_ISENSE	44
40	_SMC_ADC4	==	SMC_GFX_VSENSE	44
40	_SMC_ADC5	==	SMC_GFX_ISENSE	44
40	_SMC_ADC6	==	SMC_1V5S3_ISENSE	44
40	_SMC_ADC7	==	SMC_CPUVCCIO_ISENSE	44
40	_SMC_ADC8	==	SMC_LCDBKLT_ISENSE	44
40	_SMC_ADC9	==	SMC_WLAN_ISENSE	44
40	_SMC_ADC10	==	SMC_HDD_ISENSE	44
40	_SMC_ADC11	==	SMC_PBUS_VSENSE	44
40	_SMC_ADC12	==	SMC_BMON_ISENSE	44
40	_SMC_ADC13	==	TP_SMC_ADC13	44
40	_SMC_ADC15	==	TP_SMC_ADC15	44
40	_SMC_P10	==	TP_SMC_P10	44
40	_SMC_P20	==	TP_SMC_P20	44
40	_SMC_P24	==	TP_SMC_P24	44
40	_SMC_P26	==	SMC_BMON_MUX_SEL	44
40	_SMC_P43	==	TP_SMC_P43	44
40	_SMC_P45	==	TP_SMC_P45	44
40	_SMC_P45	==	TP_SMC_P45	44
40	_SMC_RSTGATE_L	==	TP_SMC_RSTGATE_L	44

PROCHOT Level Shifting to 3V3



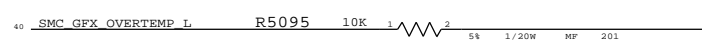
40	MEM_EVENT_L	R5075	10K	1	54	1/20W	MF	201
41	PP3V3_S0_SMC							
48	SMC_ONOFF_L	R5070	10K	1	54	1/20W	MF	201
40	G3_POWERON_L	R5072	10K	1	54	1/20W	MF	201
51	SMC_LID	R5071	100K	1	54	1/20W	MF	201
42	SMC_TX_L	R5073	10K	1	54	1/20W	MF	201
42	SMC_RX_L	R5074	100K	1	54	1/20W	MF	201
42	SMC_TMS	R5077	10K	1	54	1/20W	MF	201
42	SMC_TDO	R5078	10K	1	54	1/20W	MF	201
42	SMC_TDI	R5079	10K	1	54	1/20W	MF	201
42	SMC_TCK	R5080	10K	1	54	1/20W	MF	201
40	SMC_BIL_BUTTON_L	R5081	10K	1	54	1/20W	MF	201
41	SMC_BC_ACOK	R5087	470K	1	54	1/20W	MF	201
41	SMS_INT_L	R5093	10K	1	54	1/20W	MF	201
41	SMC_PA0_PU	R5091	100K	1	54	1/20W	MF	201
40	SMC_RUNTIME_SCT_L	R5094	100K	1	54	1/20W	MF	201
61	SMC_ADAPTER_EN	R5085	10K	1	54	1/20W	MF	201
40	SMC_CASE_OPEN	R5086	10K	1	54	1/20W	MF	201
40	SMC_PB4	R5088	10K	1	54	1/20W	MF	201
61	SMC_S4_WAKESRC_EN	R5090	100K	1	54	1/20W	MF	201

BATLOW# Isolation



Below connections are different from K91

40	SMC_PA0_PU	==	HISIDE_ISENSE_OC	45
40	SMC_FAN_1_CTL	==	NC_SMC_FAN_1_CTL	45
40	SMC_FAN_1_TACH	==	NC_SMC_FAN_1_TACH	45
40	SMC_ADC14	==	SMC_HS_COMPUTING_ISENSE	45
40	SMC_GFX_THROTTLE_L	==	TP_SMC_GFX_THROTTLE_L	45



SYNC MASTER=K21_MLB SYNC DATE=12/13/2011

SMC Support

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

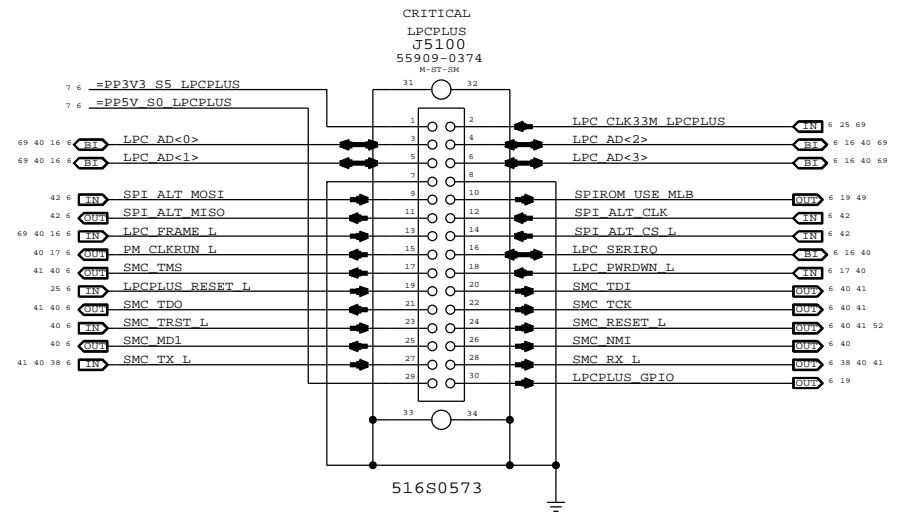
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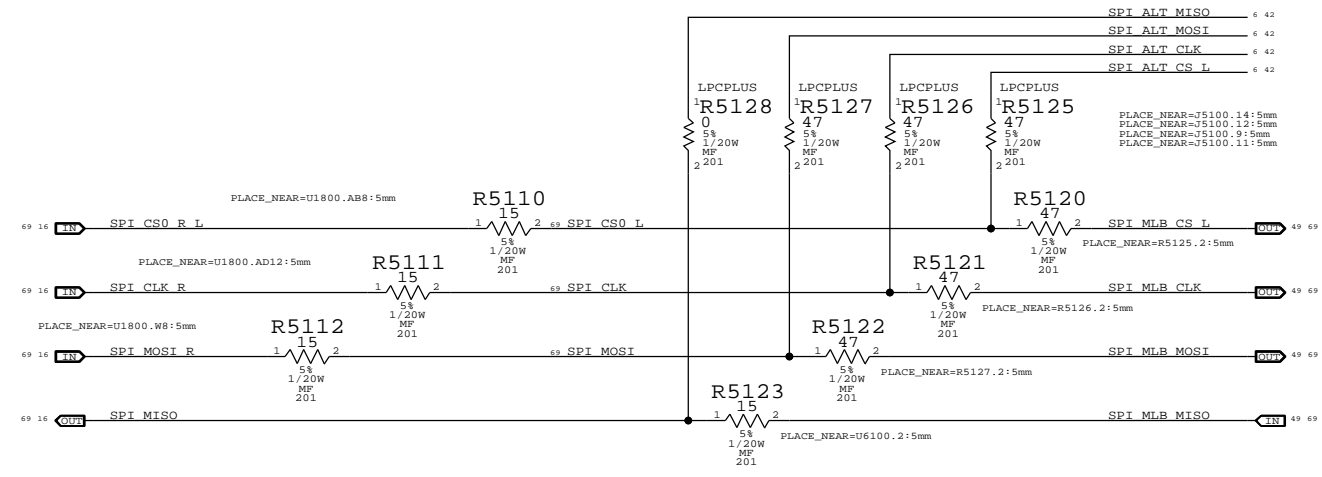
PAGE: 50 OF 109 SHEET: 41 OF 74

D
C
B
A

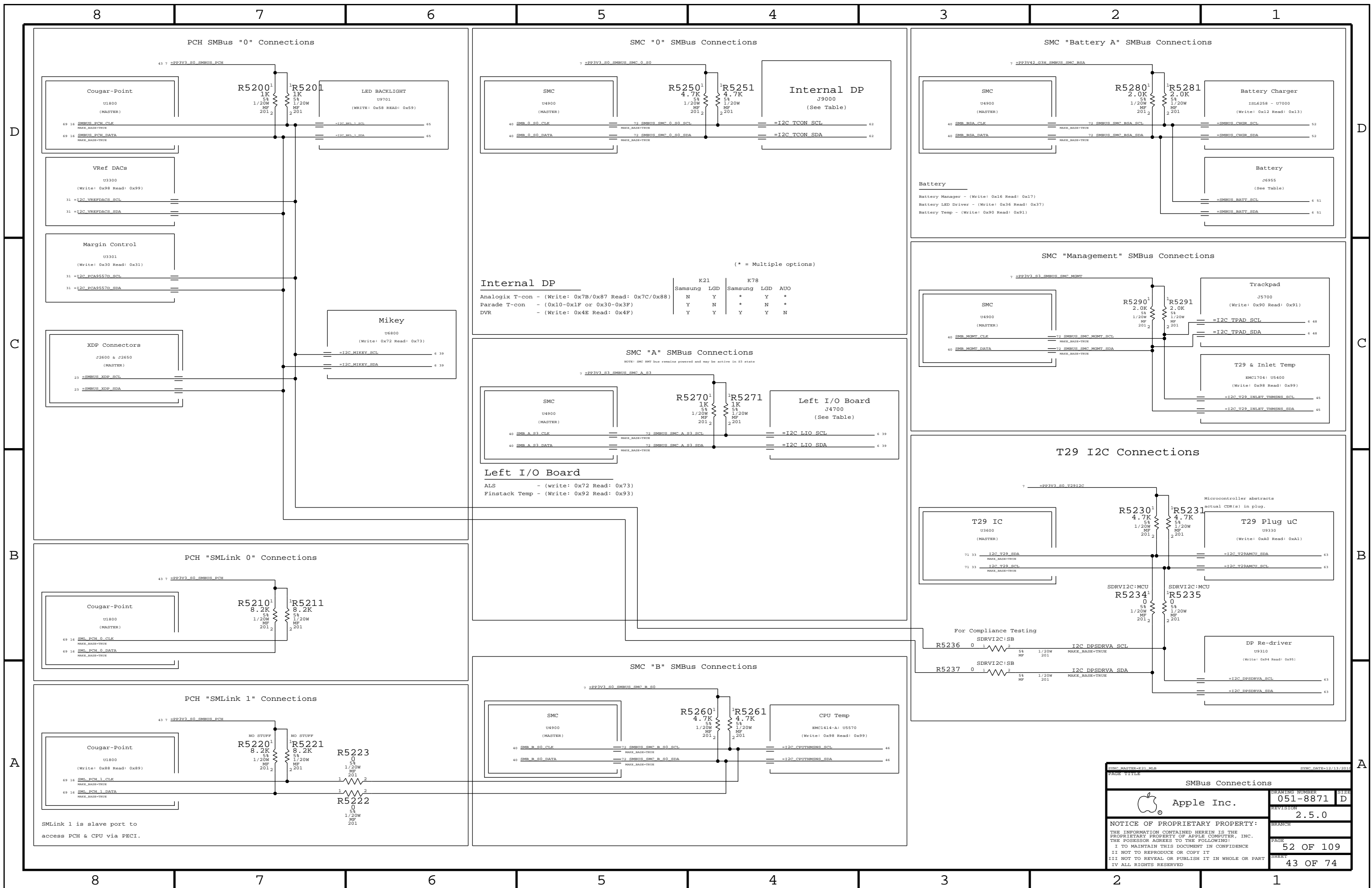
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	SIZE
		051-8871	D
		REVISION	
		2.5.0	BRANCH
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Internal DP

Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)
 Parade T-con - (0x10-0x1F or 0x30-0x3F)
 DVR - (Write: 0x4E Read: 0x4F)

(* = Multiple options)

	K21	K78		
	Samsung	LGD	Samsung	LGD AUO
Y	Y	*	Y	*
N	N	*	N	*
Y	Y	Y	Y	N

Left I/O Board

ALS - (write: 0x72 Read: 0x73)
 Finstack Temp - (Write: 0x92 Read: 0x93)

SYMC_MASTER=K11_MCB SYMC_DATE=12/13/2015
 PAGE TITLE

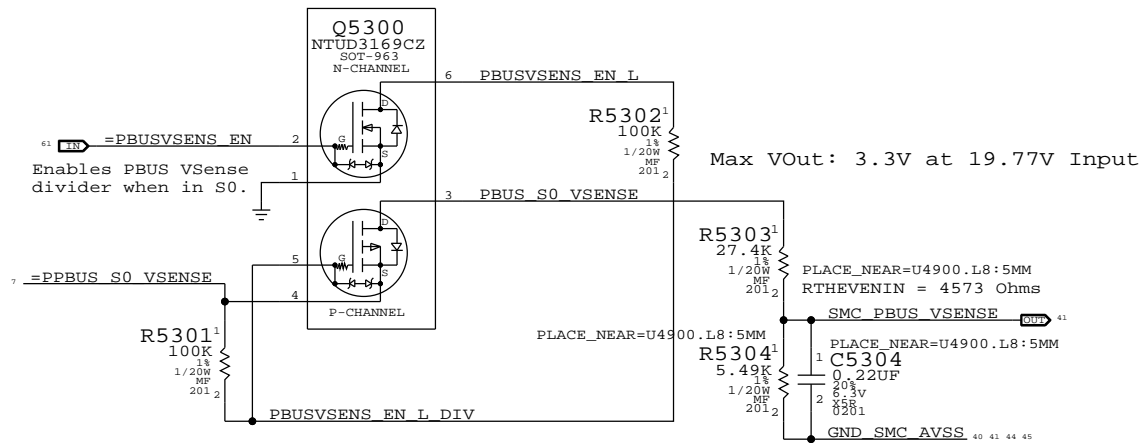
SMBus Connections

Apple Inc.

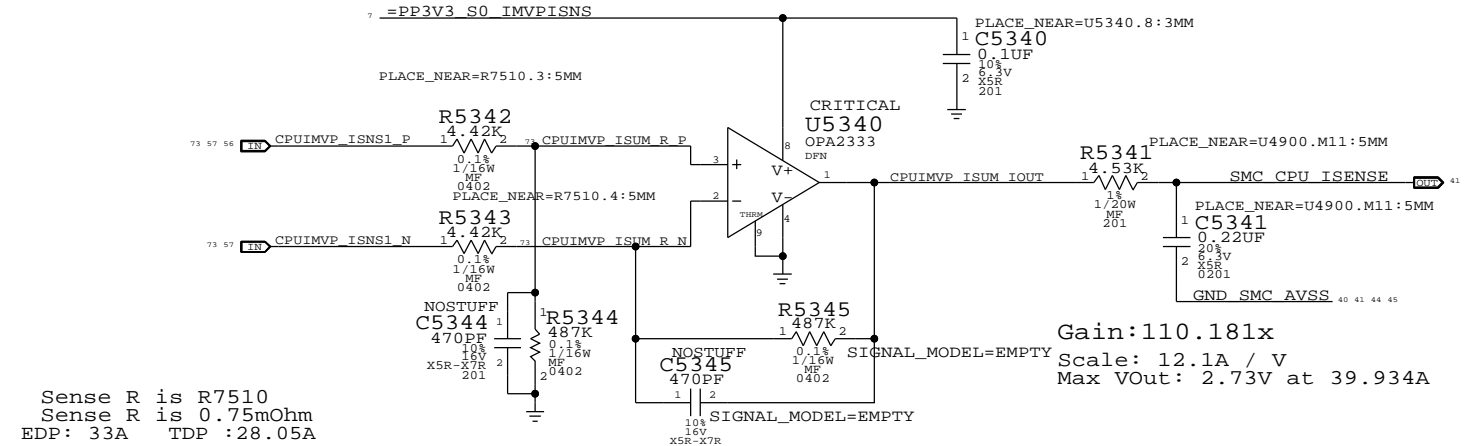
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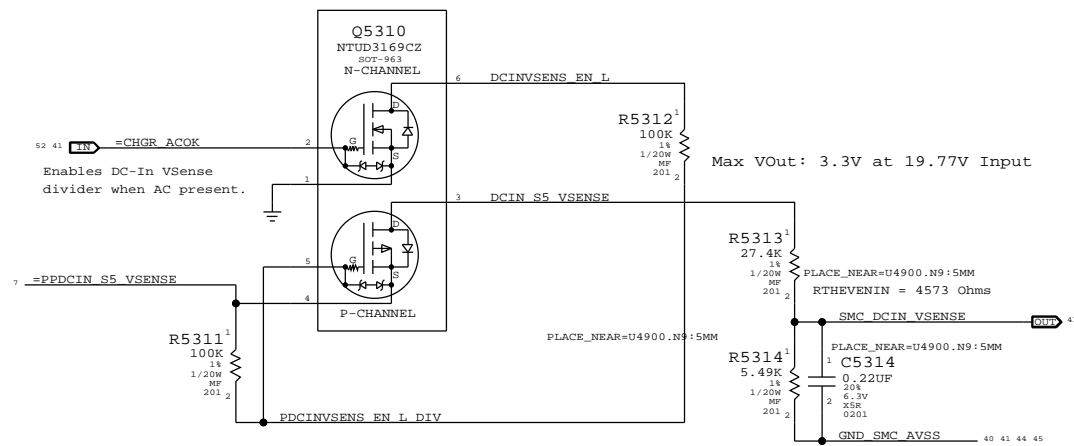
PBUS Voltage Sense Enable & Filter



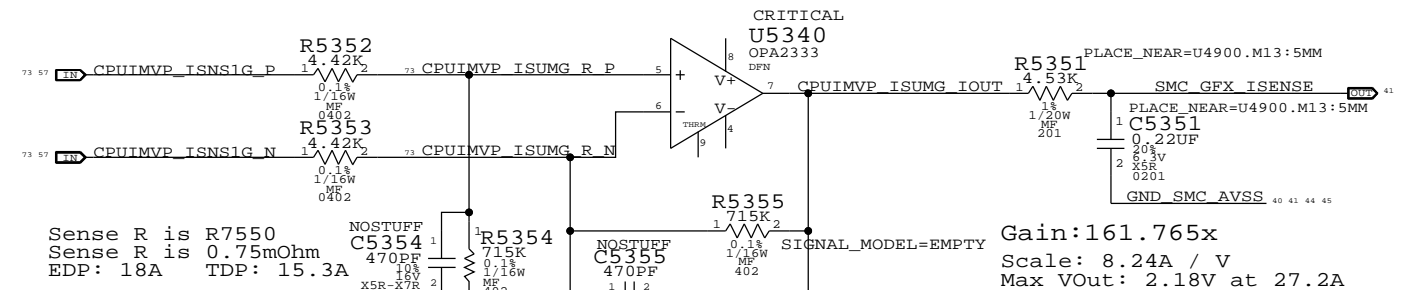
CPU VCore Load Side Current Sense / Filter



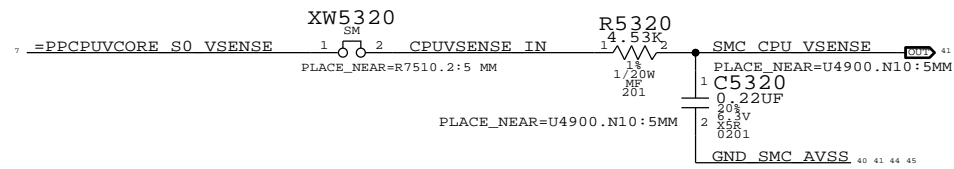
DC-In Voltage Sense Enable & Filter



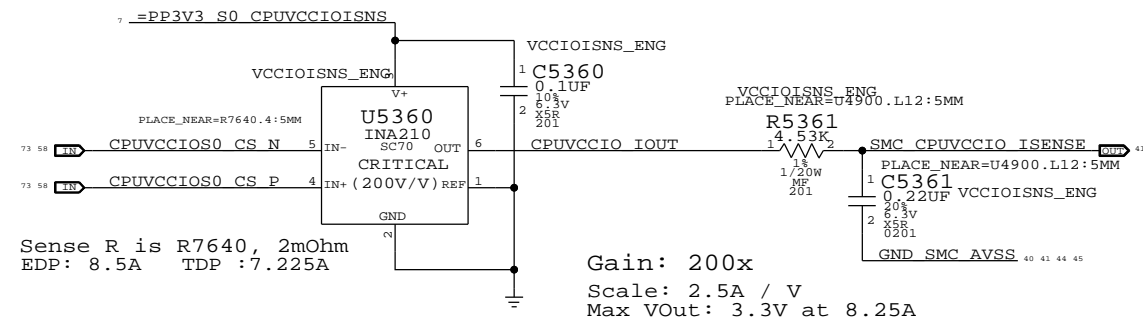
GFX/IG VCore Load Side Current Sense / Filter



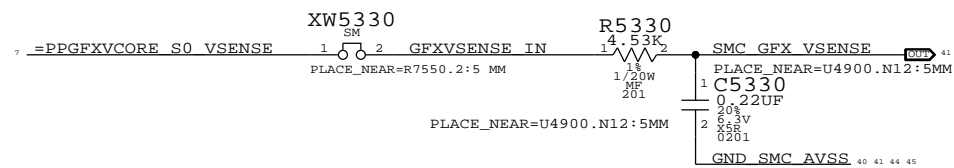
CPU Vcore Voltage Sense / Filter



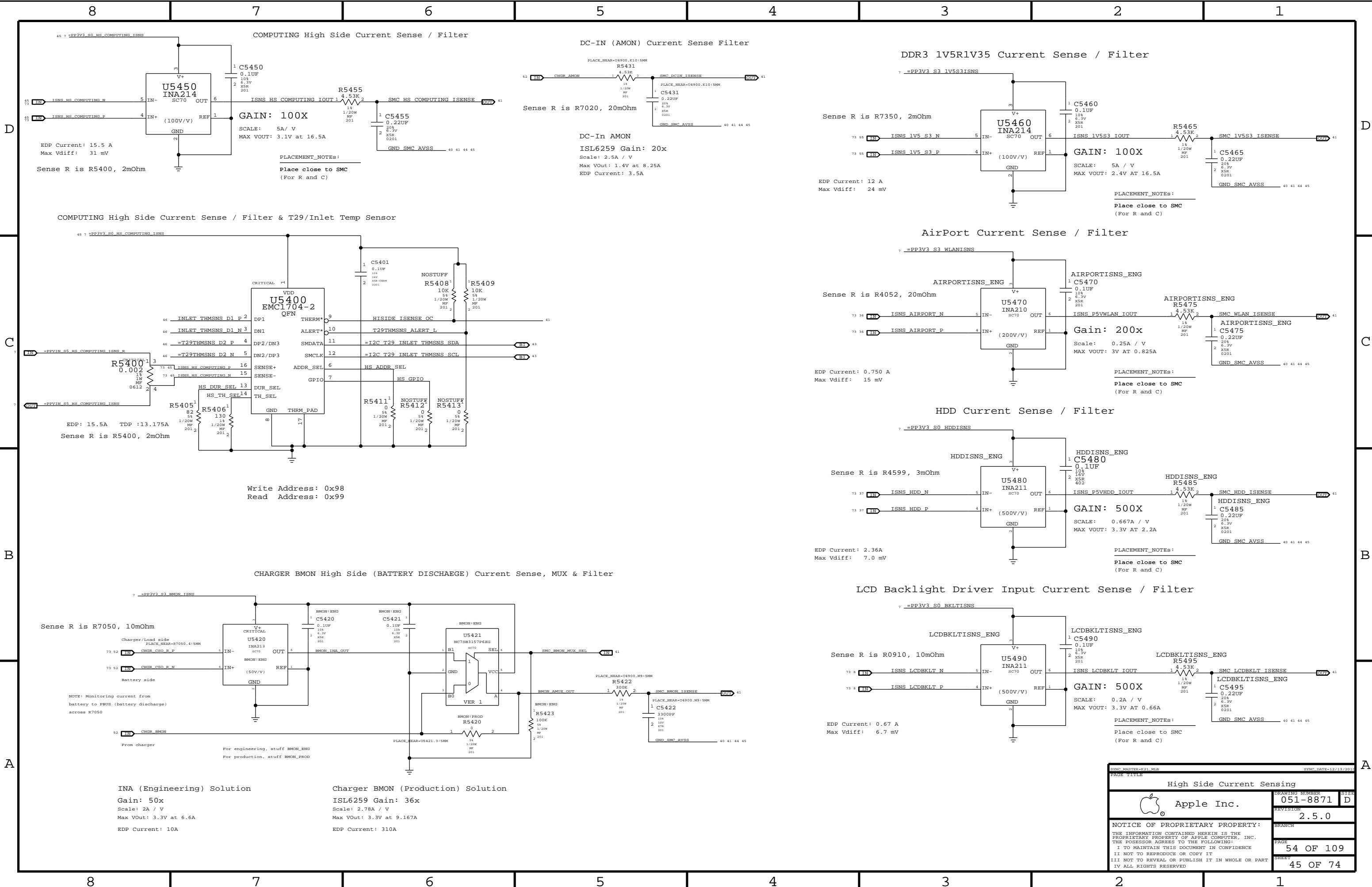
CPU 1.05V VCCIO Current Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
Voltage & Load Side Current Sensing			
Apple Inc.		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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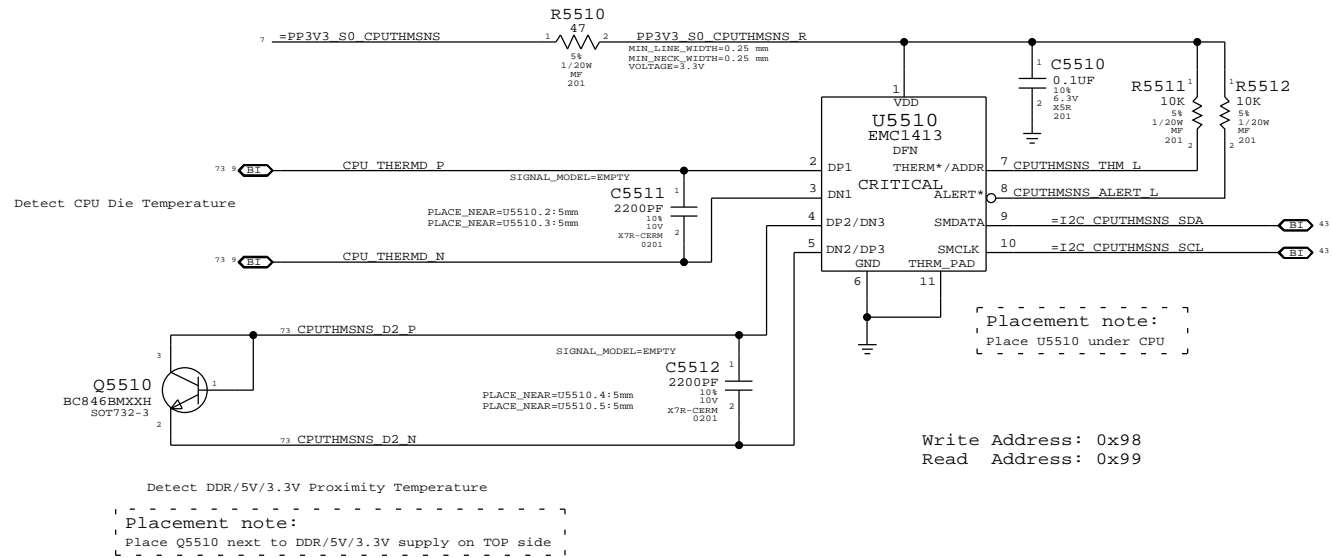


INA (Engineering) Solution
 Gain: 50x
 Scale: 2A / V
 Max Vout: 3.3V at 6.6A
 EDP Current: 10A

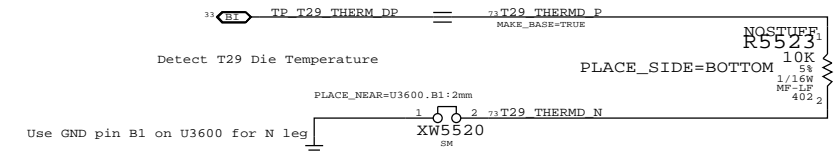
Charger BMON (Production) Solution
 ISL6259 Gain: 36x
 Scale: 2.78A / V
 Max Vout: 3.3V at 9.167A
 EDP Current: 310A

SMC PARTS=K11_MCB		SYMC DATE=12/13/2016	
PAGE TITLE			
High Side Current Sensing			DRAWING NUMBER
Apple Inc.			051-8871
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CPU Proximity Sensor



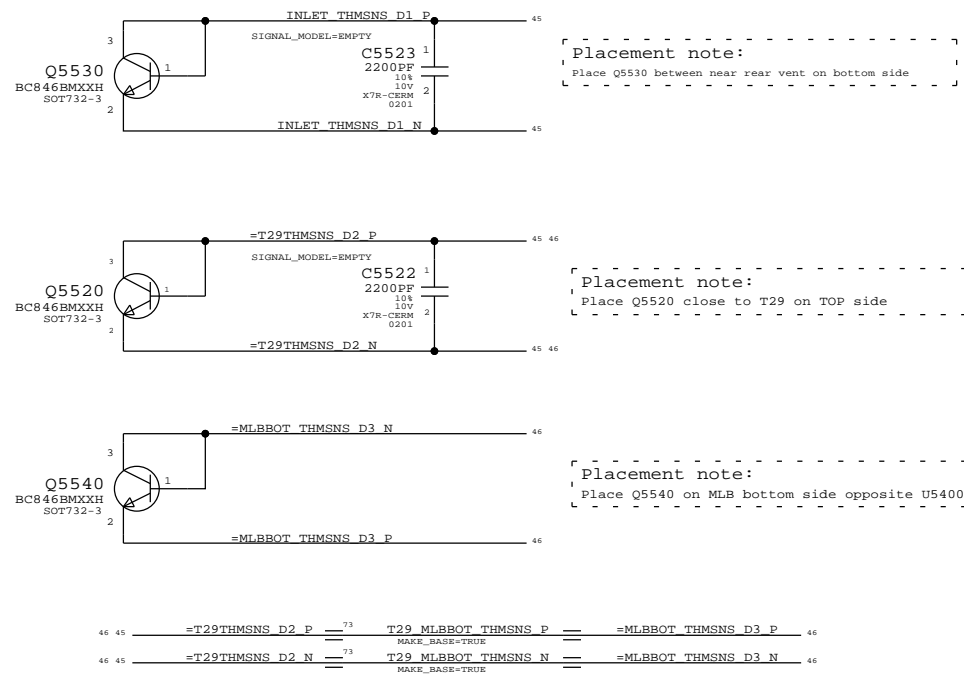
T29 Die



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MP,1/20W,100K OHM,5,0201,SMD	C5495		LDCBKLTISNS_PROD

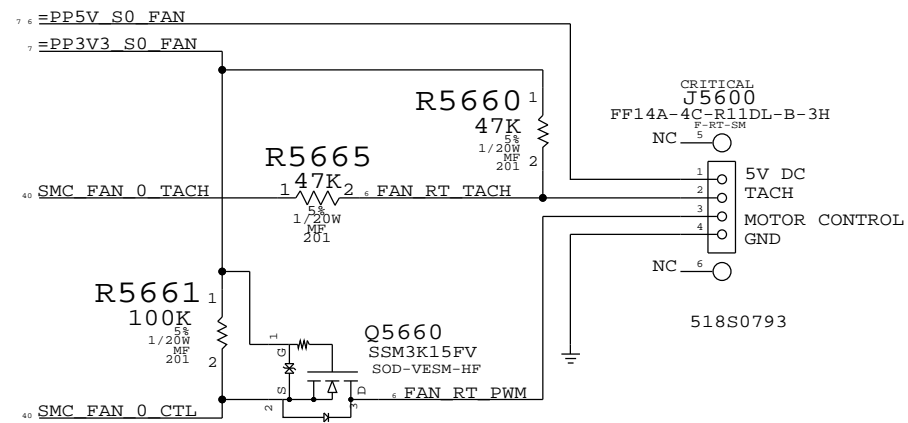
Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors



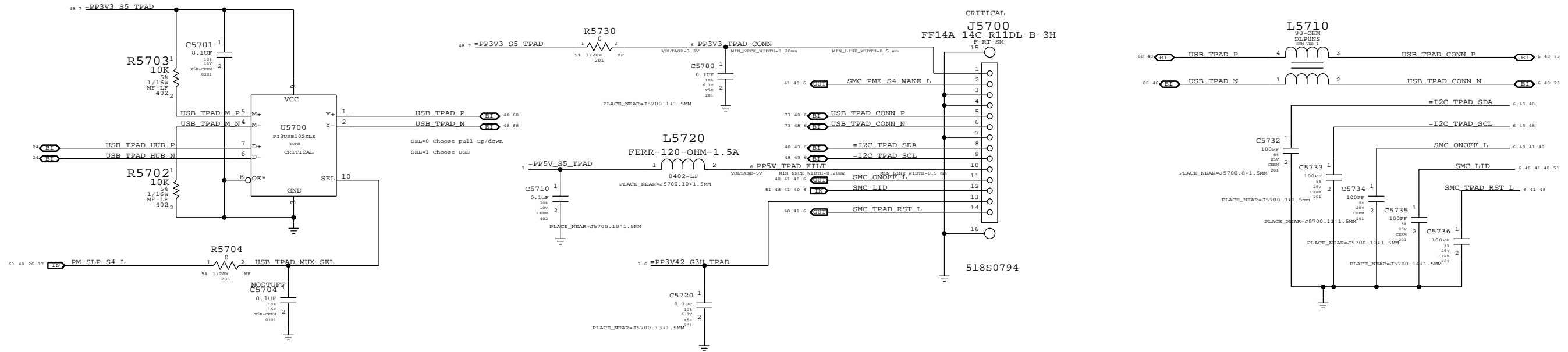
SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
PAGE TITLE			
Thermal Sensors			
		DRAWING NUMBER	051-8871
		REVISION	2.5.0
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		SHEET	46 OF 74

FAN CONNECTOR

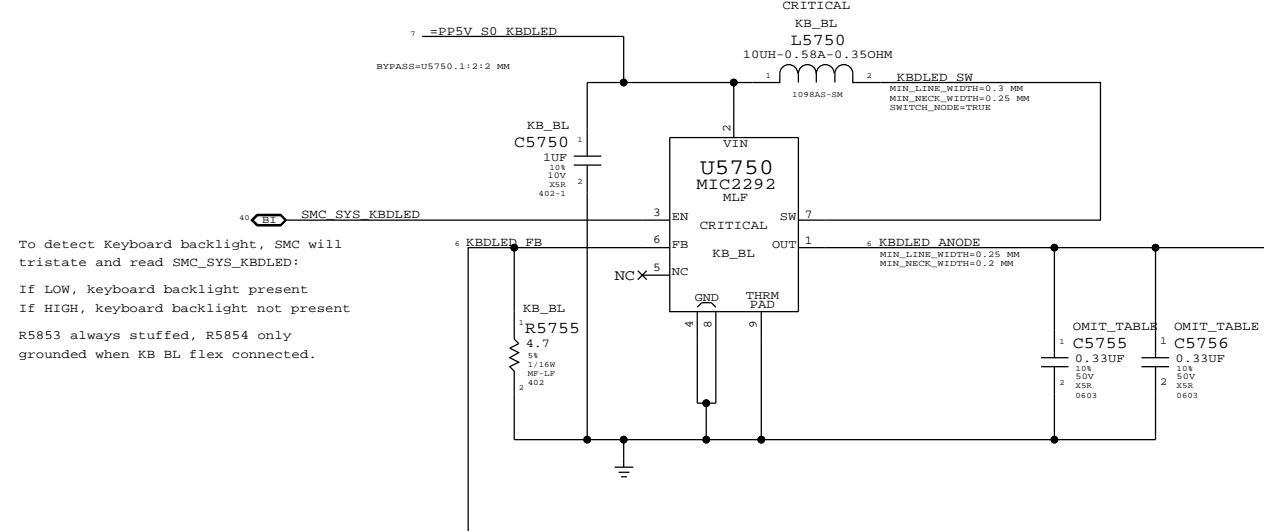


SYNC MASTER=K21_MLB		SYNC DATE=12/13/2010	
PAGE TITLE Fan			
DRAWING NUMBER 051-8871		SIZE D	
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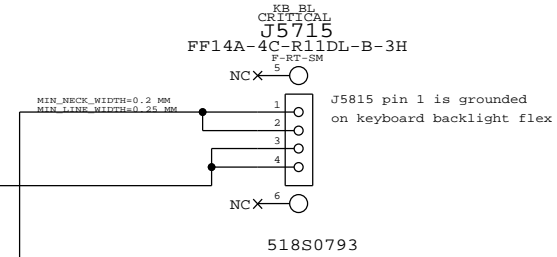
IPD Flex Connector



Keyboard Backlight Driver & Detection

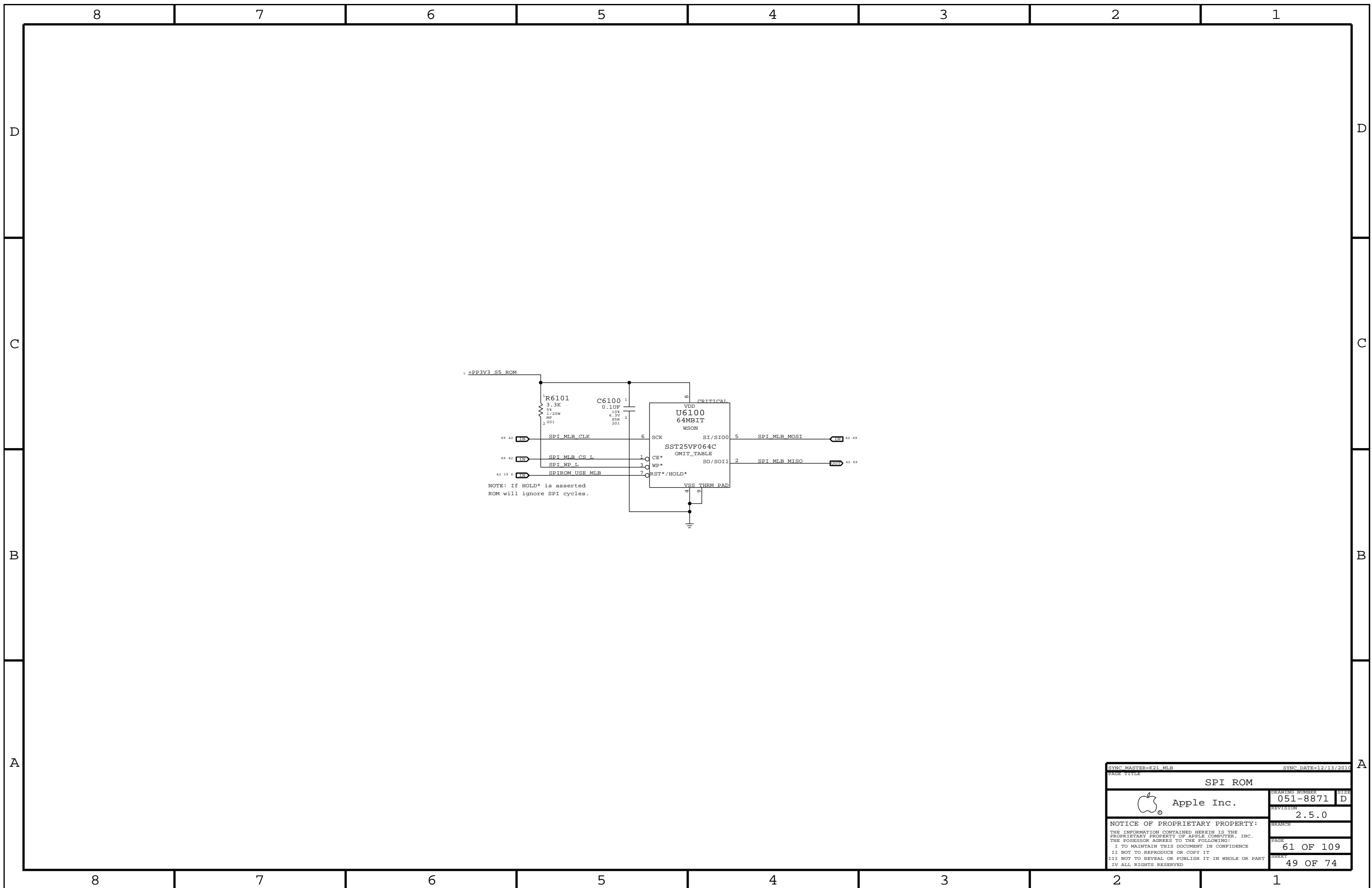


Keyboard Backlight Connector



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP, CER, 0.22UF, 10V, 50V, X5R, 0603	C5756, C5755		KB_BL

SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
PAGE TITLE			
IPD / KBD Backlight		DRAWING NUMBER	051-8871
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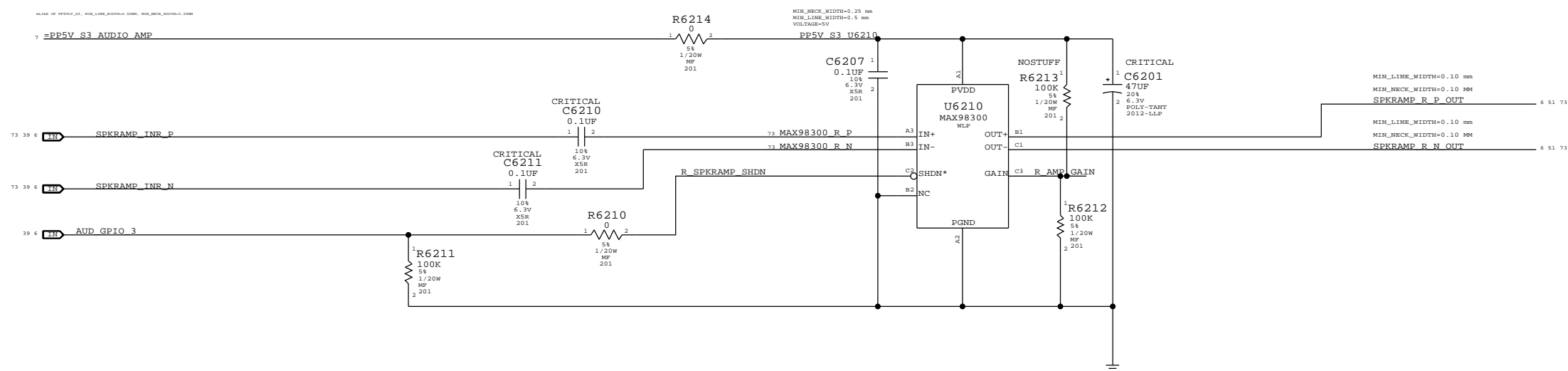
SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
PAGE TITLE SPI ROM			
DRAWING NUMBER 051-8871		SIZE D	
REVISION 2.5.0		BRANCH	
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8 7 6 5 4 3 2 1

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ
GAIN 6DB



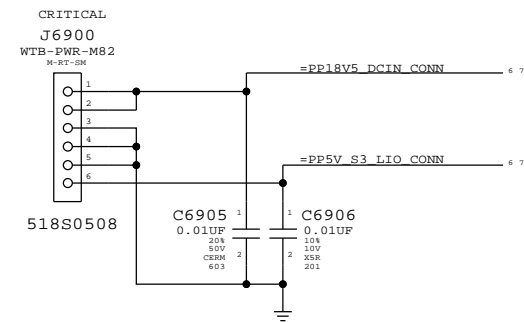
D
C
B
A

D
C
B
A

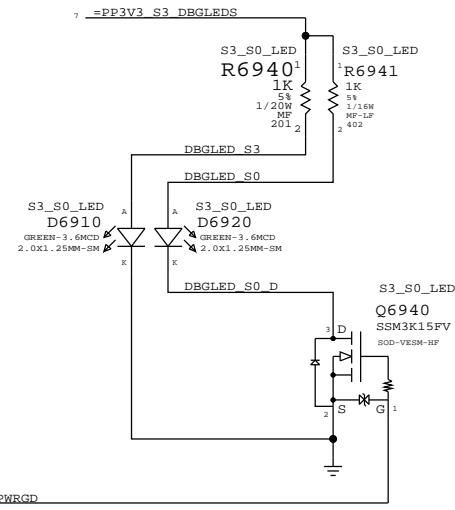
SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
PAGE TITLE AUDIO: SPEAKER AMP			
DRAWING NUMBER 051-8871		SIZE D	
REVISION 2.5.0		BRANCH	
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8 7 6 5 4 3 2 1

MLB to LIO Power Cable Connector

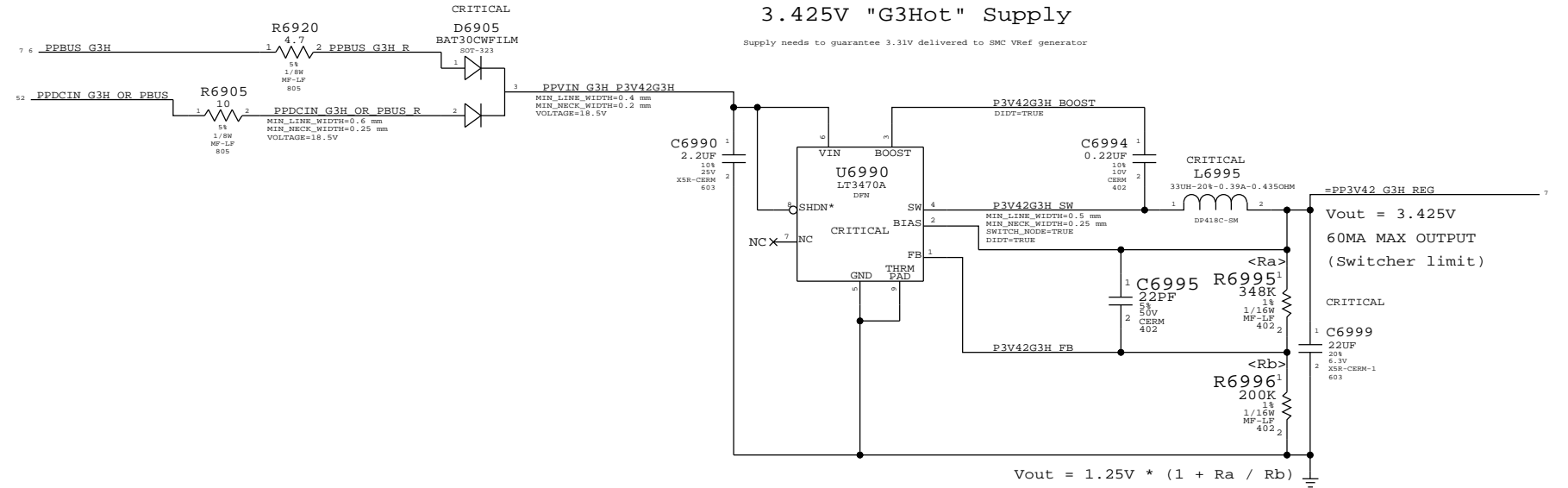


Debug LEDs
(For development only)

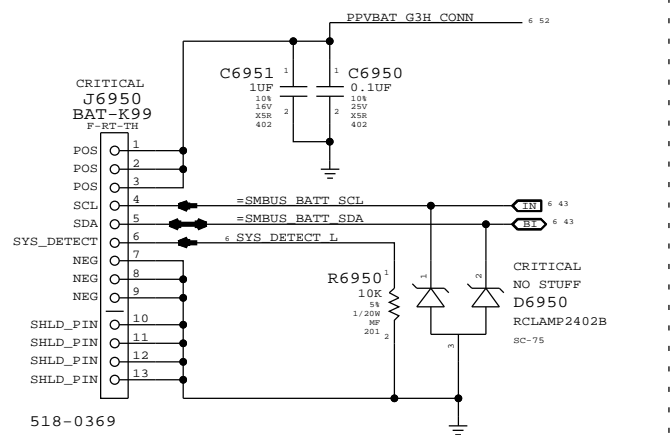


3.425V "G3Hot" Supply

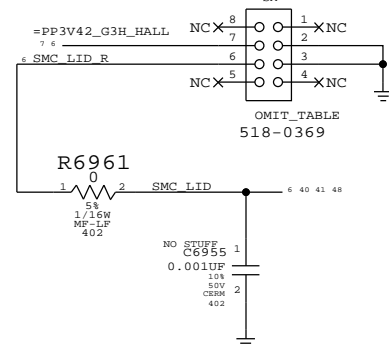
Supply needs to guarantee 3.31V delivered to SMC Vref generator



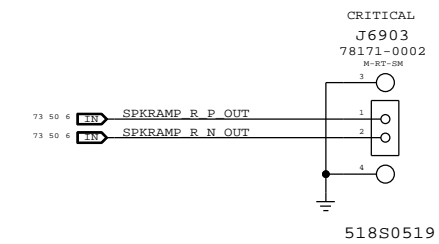
K99-Specific
Battery Connector



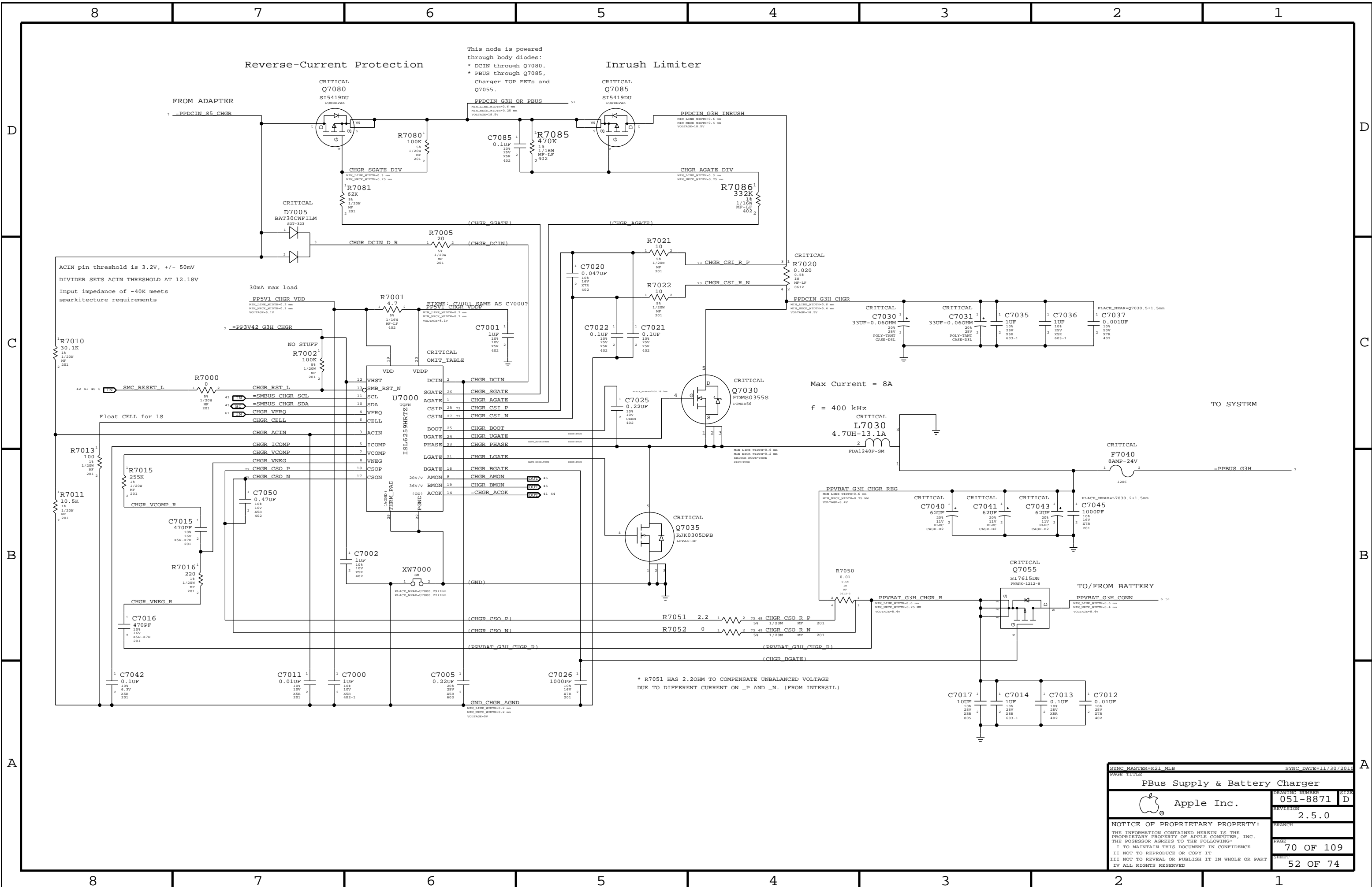
J6955
HALL-SENSOR-MLB-PADS-K99



Right Speaker Connector



DC-In & Battery Connectors		DRAWING NUMBER	051-8871	SIZE	D
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This node is powered through body diodes:
 * DCIN through Q7080.
 * PBUS through Q7085, Charger TOP FETs and Q7055.

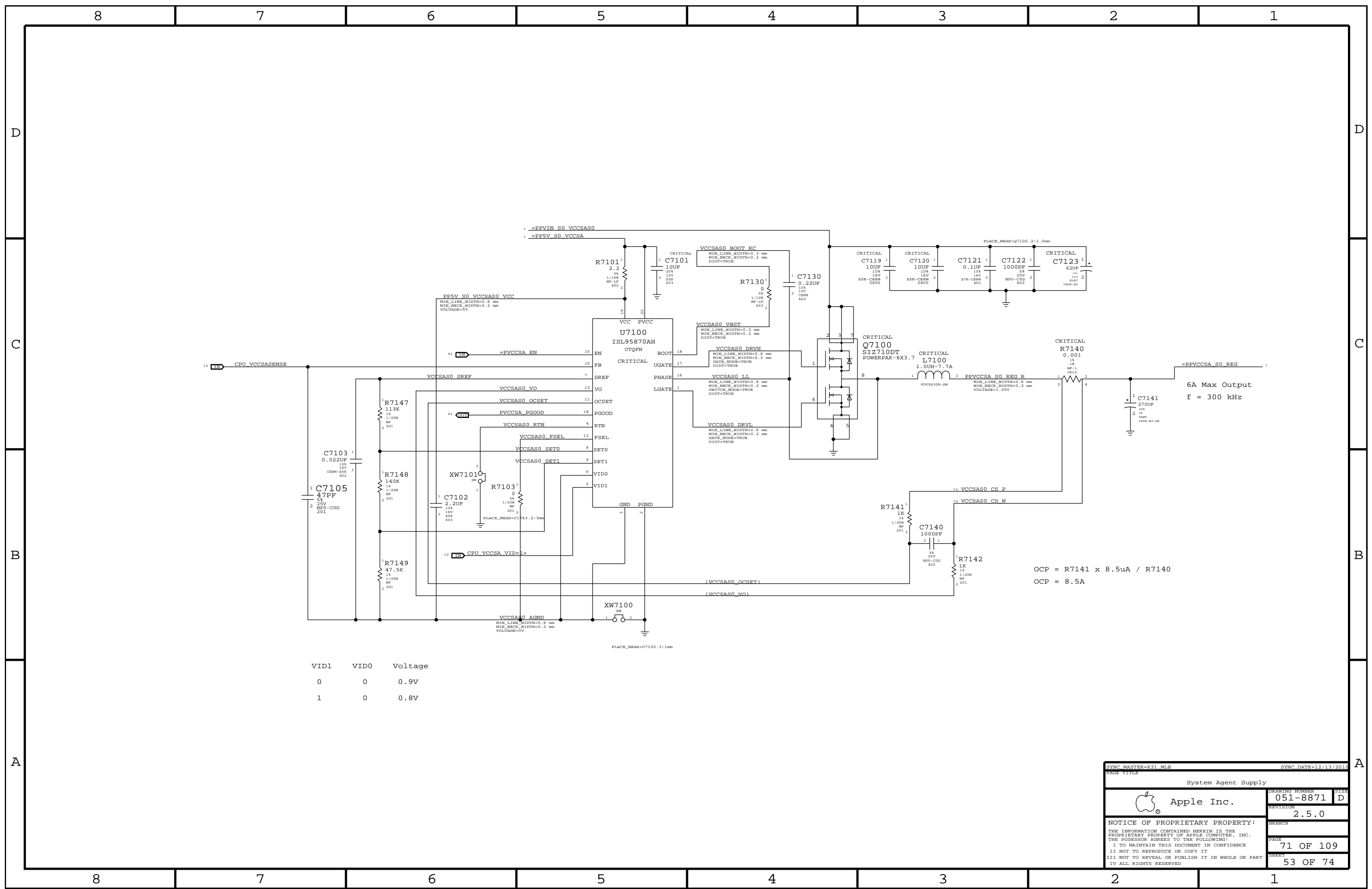
ACIN pin threshold is 3.2V, +/- 50mV
 DIVIDER SETS ACIN THRESHOLD AT 12.18V
 Input impedance of ~40K meets sparkitecture requirements

Max Current = 8A

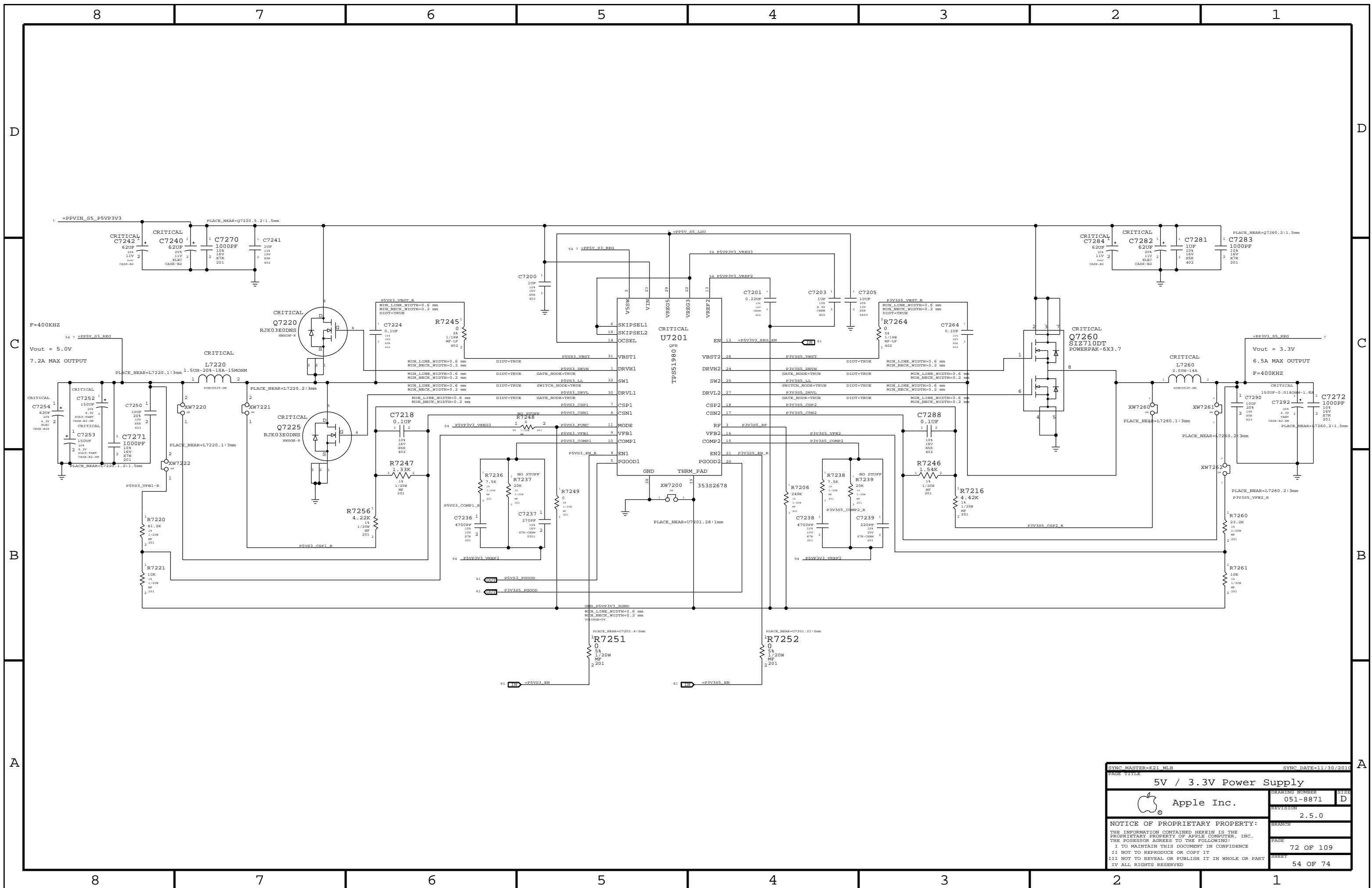
f = 400 kHz

* R7051 HAS 2.2OHM TO COMPENSATE UNBALANCED VOLTAGE DUE TO DIFFERENT CURRENT ON _P AND _N. (FROM INTERSIL)

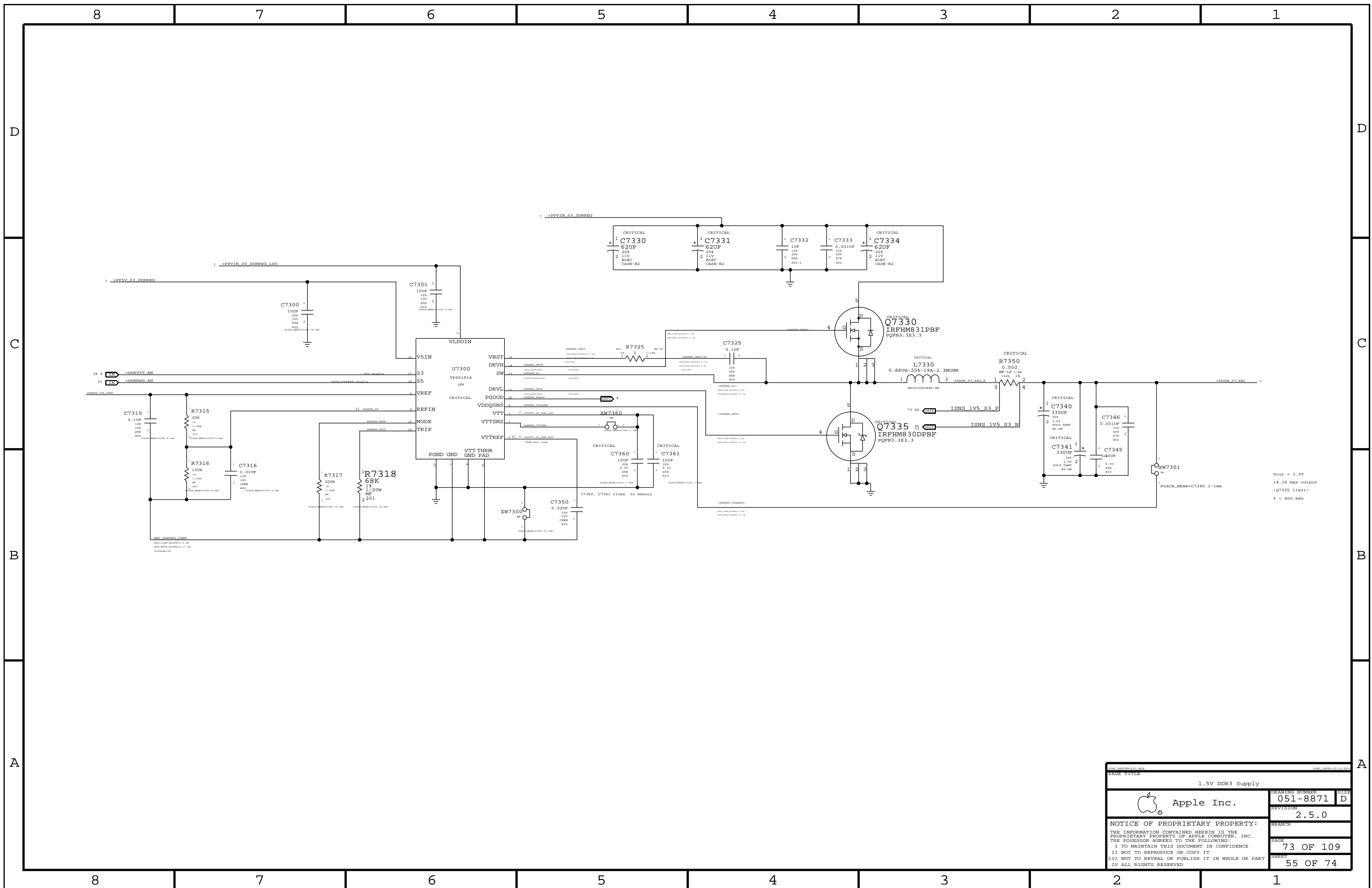
SYNC MASTER=K21_MLB		SYNC DATE=11/30/2011	
PAGE TITLE PBus Supply & Battery Charger			
DRAWING NUMBER 051-8871		SIZE D	
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PAGE TITLE			
System Agent Supply			
Apple Inc.	DRAWING NUMBER	051-8871	SIZE
	REVISION	2.5.0	D
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PAGE TITLE			
5V / 3.3V Power Supply			
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Apple Inc.		051-8871	D
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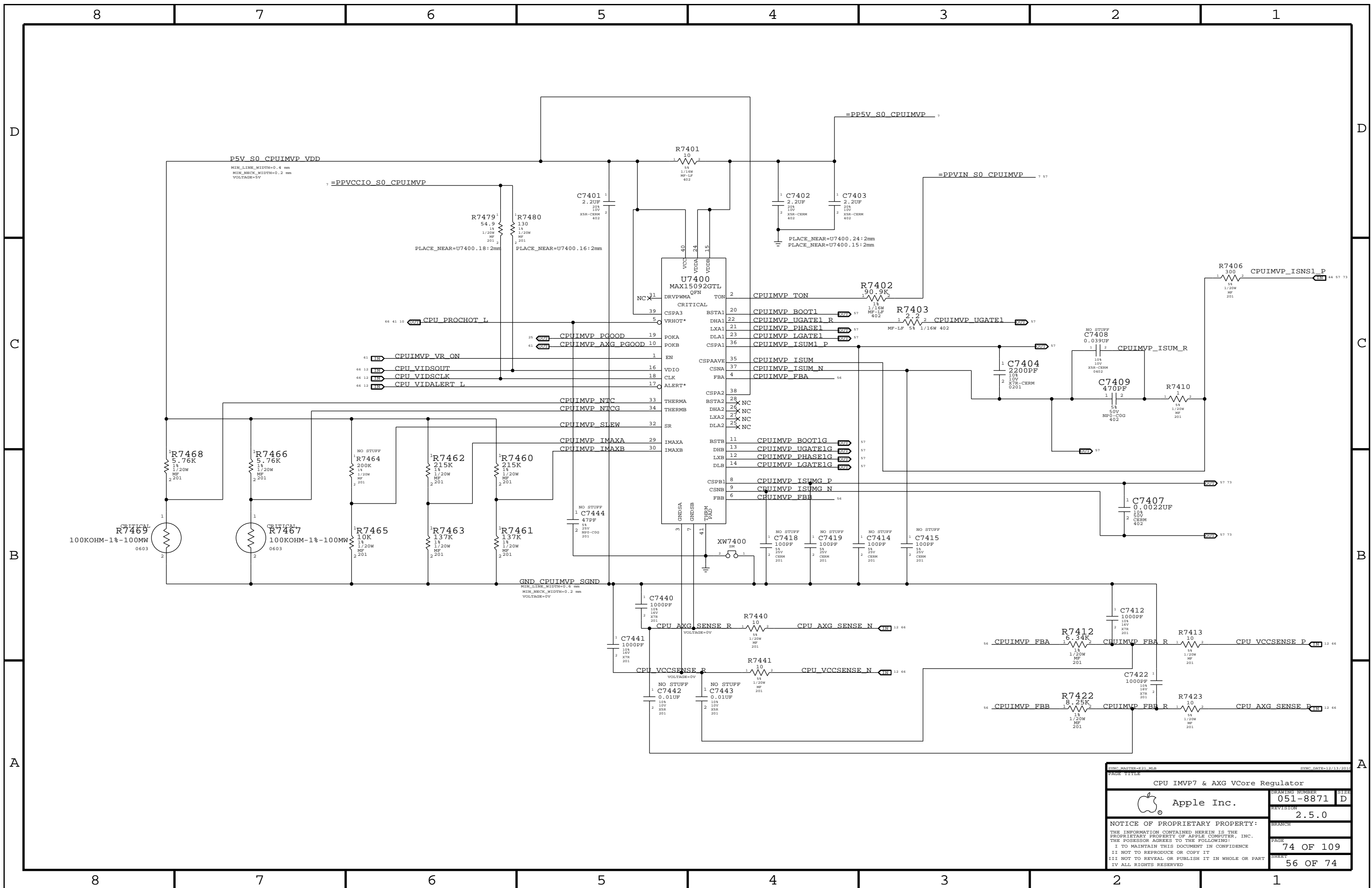


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REVISION		2.5.0	BRANCH	
PAGE		73 OF 109	SHEET	
SHEET		55 OF 74		

1.5V DDR3 Supply

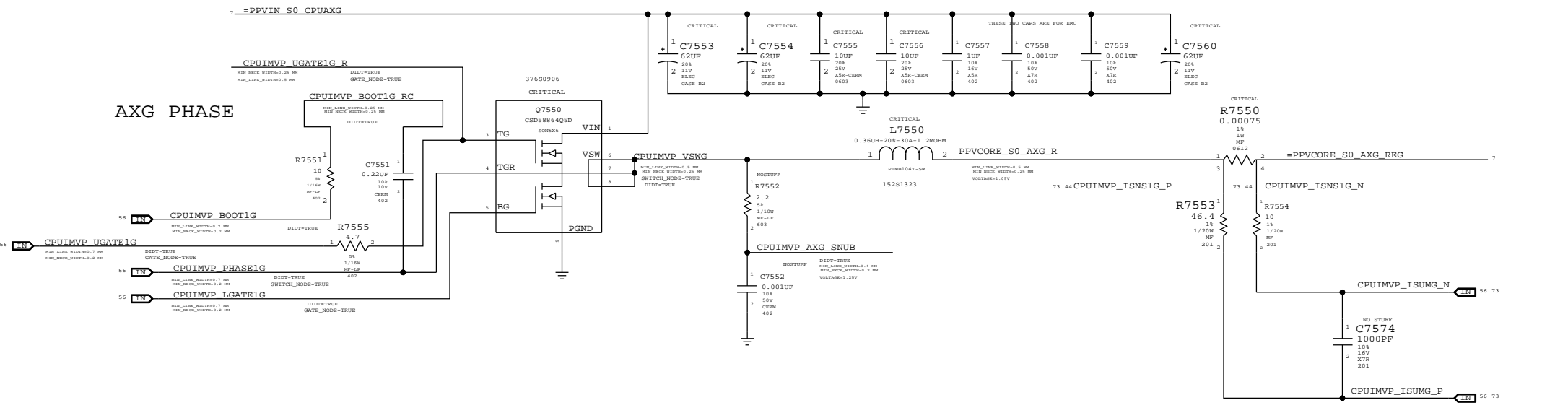
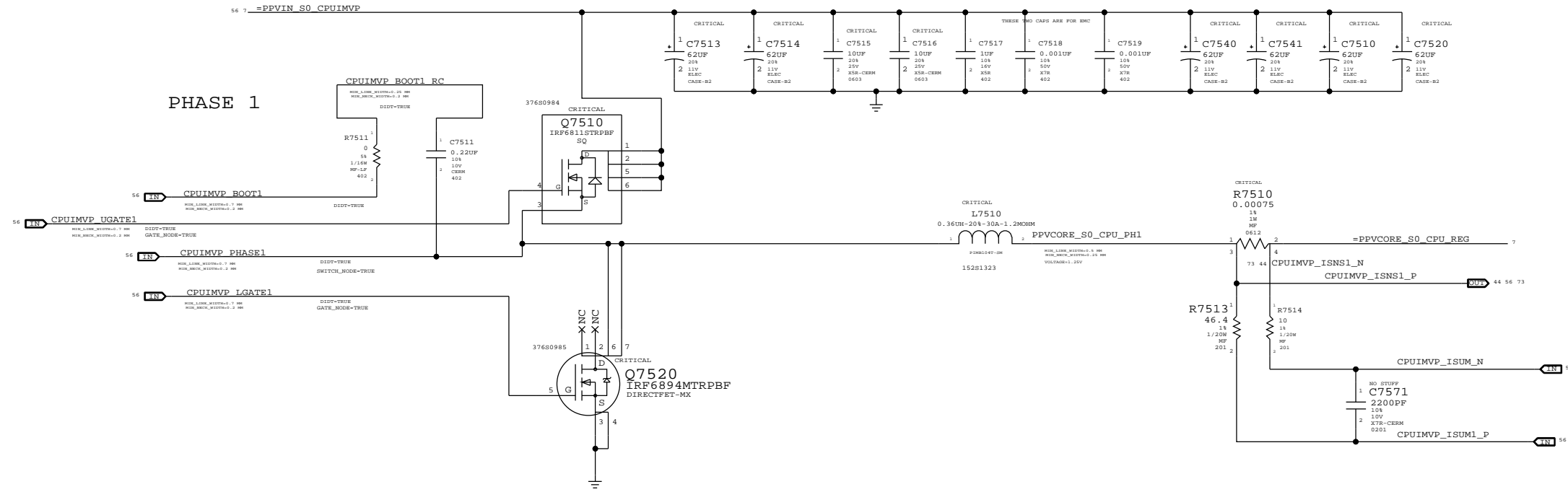
Apple Inc.

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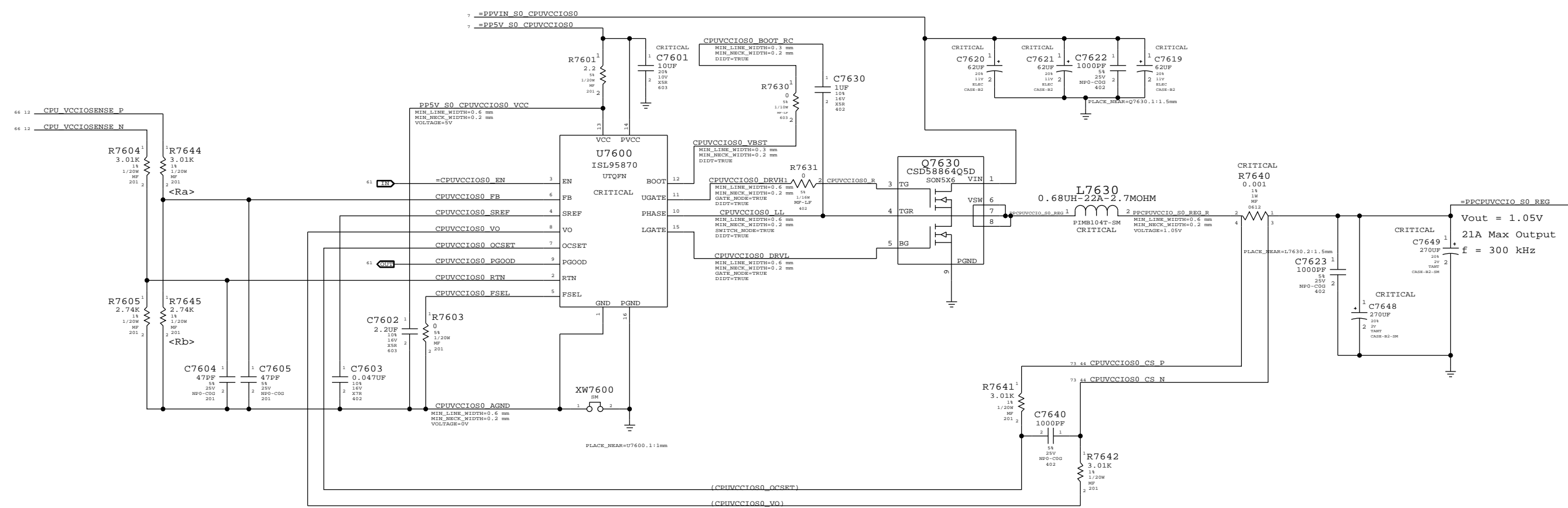
CPU IMVP7 & AXG VCore Regulator	
Apple Inc.	DRAWING NUMBER: 051-8871
REVISION: 2.5.0	SIZE: D
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CPU=Sandy Bridge ULV, AXG=GT2



CPU IMPV7 & AXG VCore Output		
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		PAGE 75 OF 109
		SHEET 57 OF 74

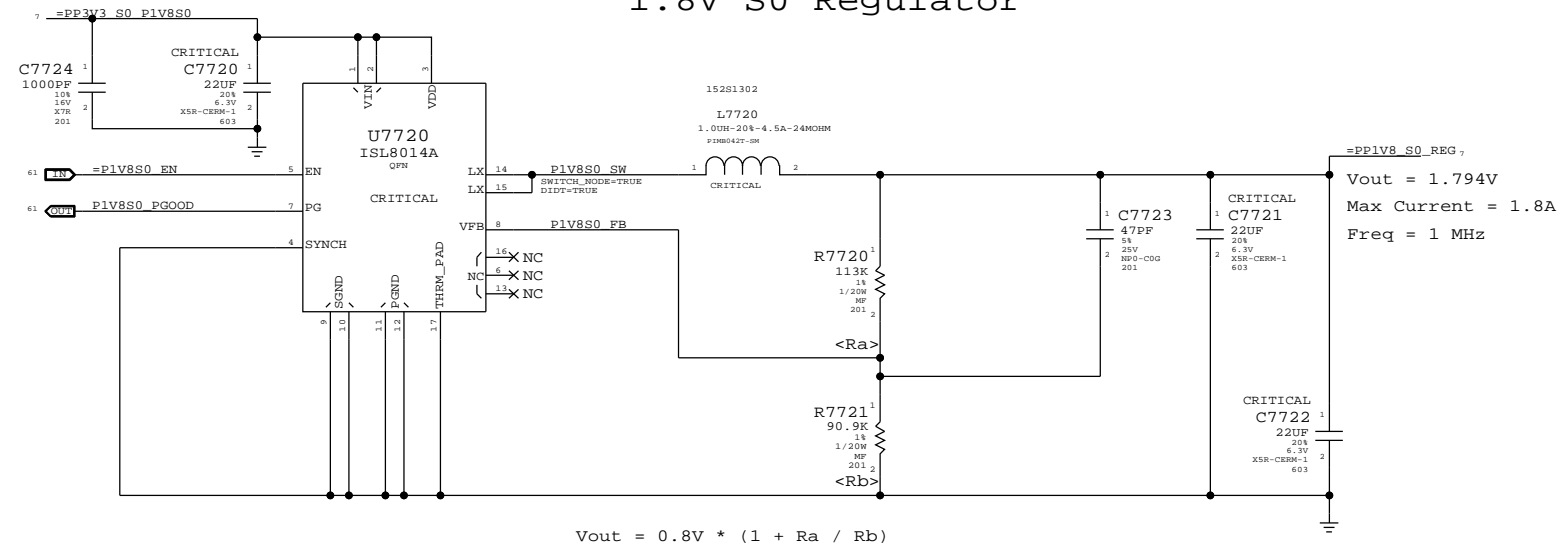
CPU VCCIO (1.05V S0) Regulator



$OCP = R7641 \times 8.5\mu A / R7640$
 $OCP = 25.6A$
 $V_{out} = 0.5V * (1 + R_a / R_b)$

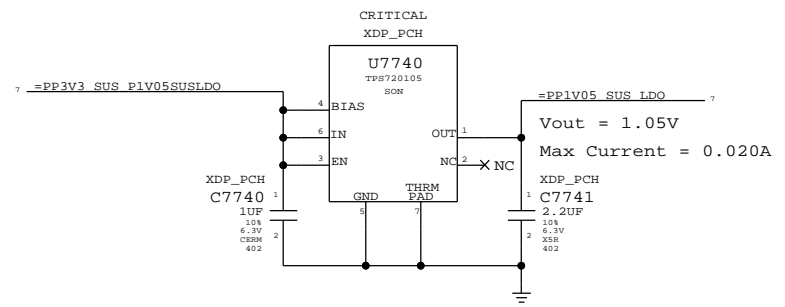
SYMC_WAFFER=K11_MCB		SYMC_DATE=12/15/2016	
PAGE TITLE			
CPU VCCIO (1.05V) Power Supply			
Apple Inc.	DRAWING NUMBER	051-8871	SIZE D
	REVISION	2.5.0	
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1.8V S0 Regulator

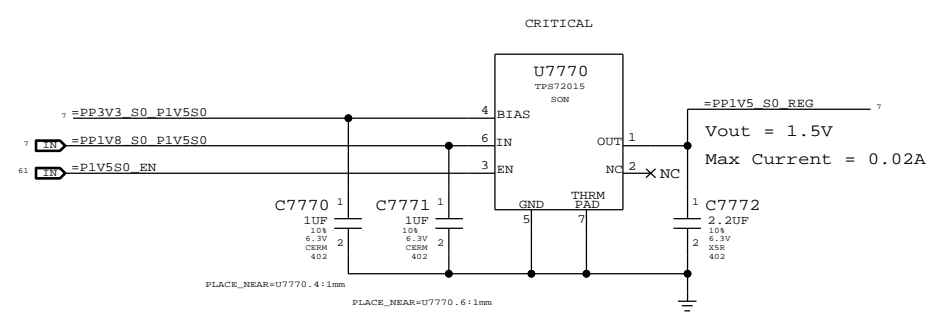


1.05V SUS LDO

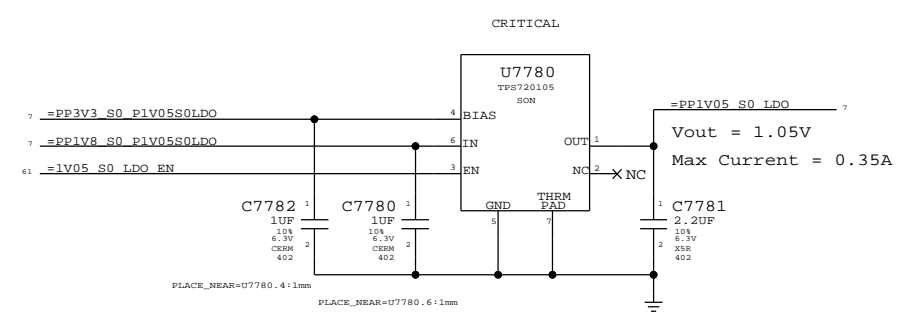
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



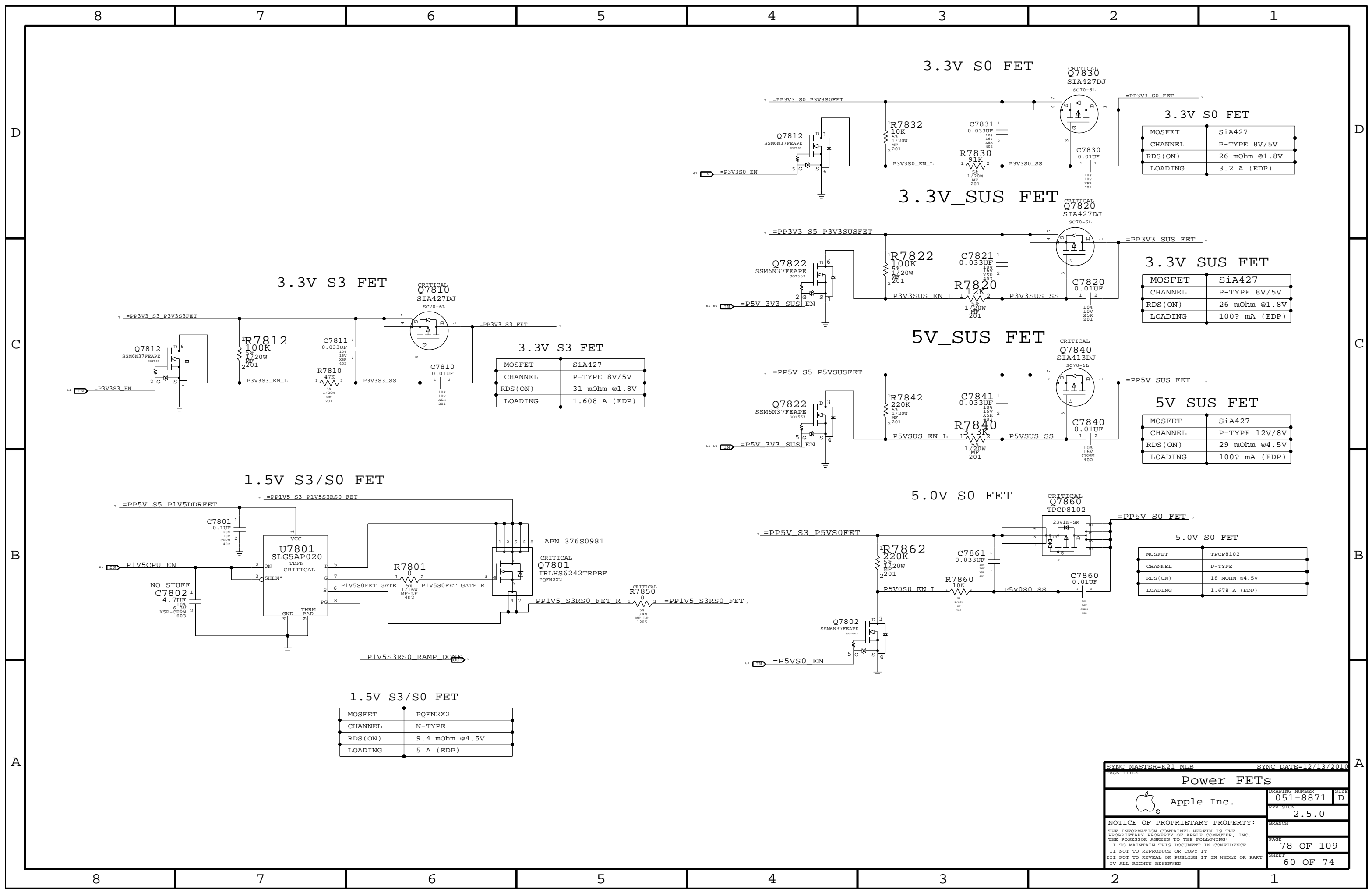
1.5V S0 LDO



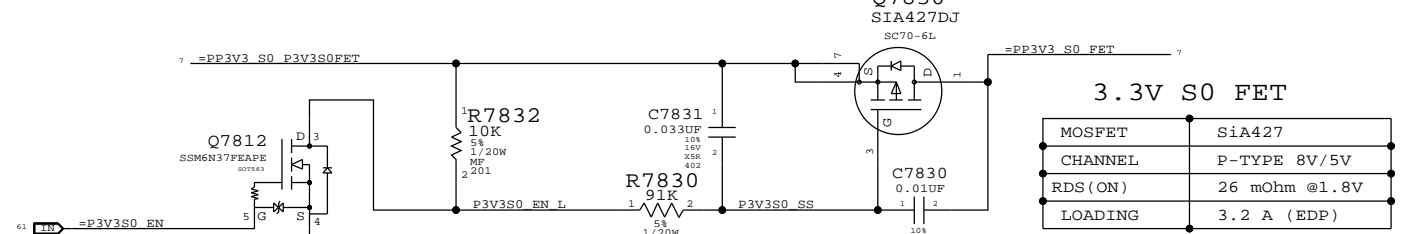
1.05V S0 LDO



SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
PAGE TITLE: Misc Power Supplies			
Apple Inc.	DRAWING NUMBER	051-8871	SIZE
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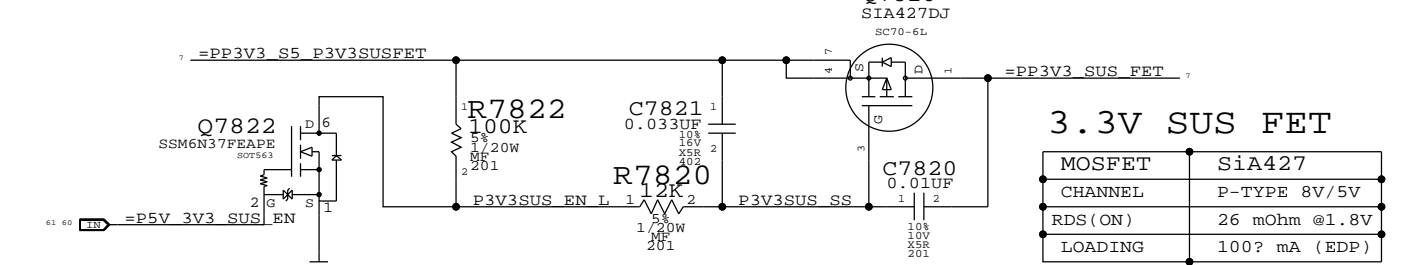


3.3V S0 FET



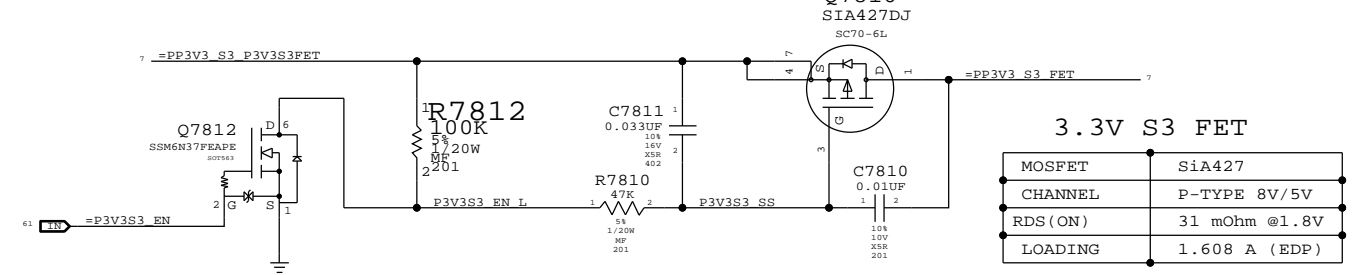
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



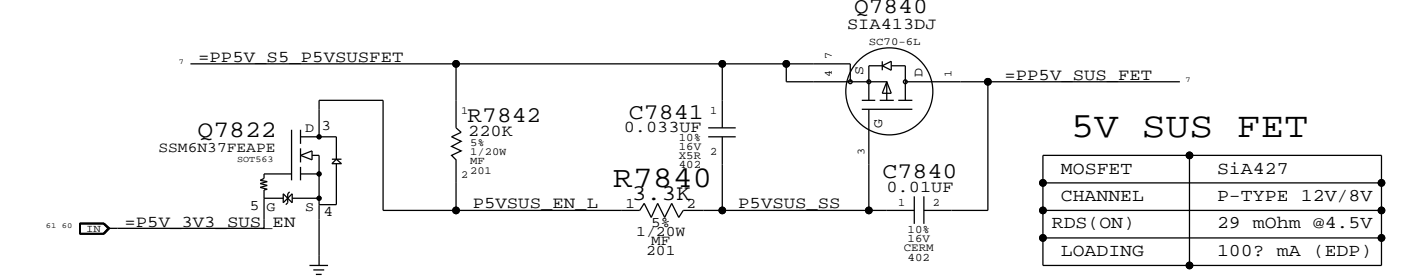
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

3.3V S3 FET



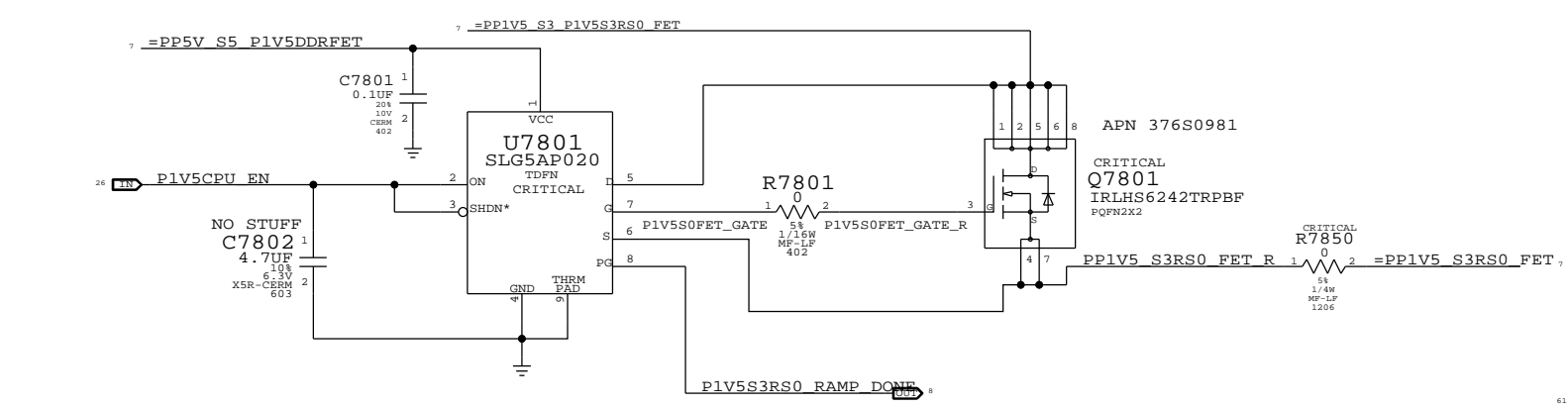
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

5V_SUS FET



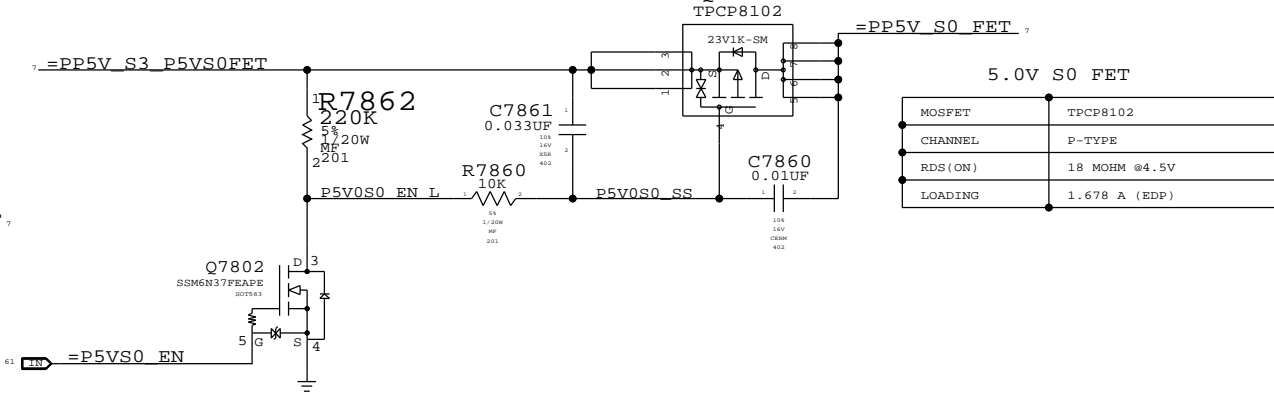
MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

1.5V S3/S0 FET



MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET



MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K21_MLB SYNC DATE=12/13/2010

Power FETs

Apple Inc.

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REVISION	2.5.0	BRANCH	
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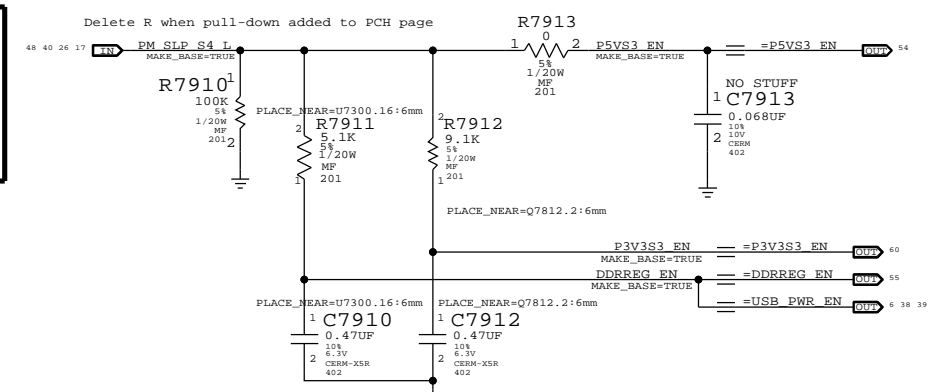
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S5 Rail Enables & PGOOD

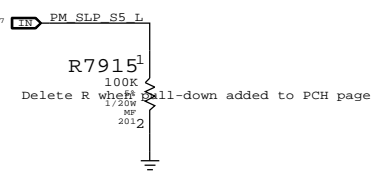
=PP3V42 G3H PWRCTL Internal pull-ups 100K +/- 20%

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

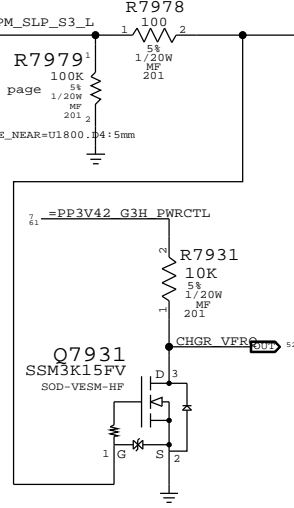
3.3V, 5V S3 ENABLE



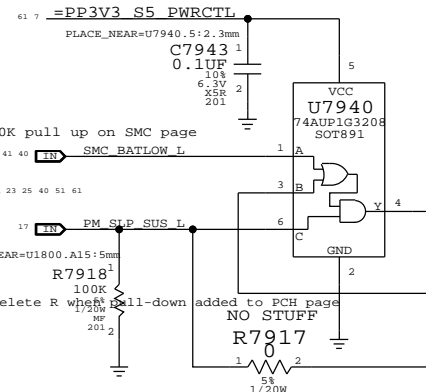
3.3V S4 ENABLE



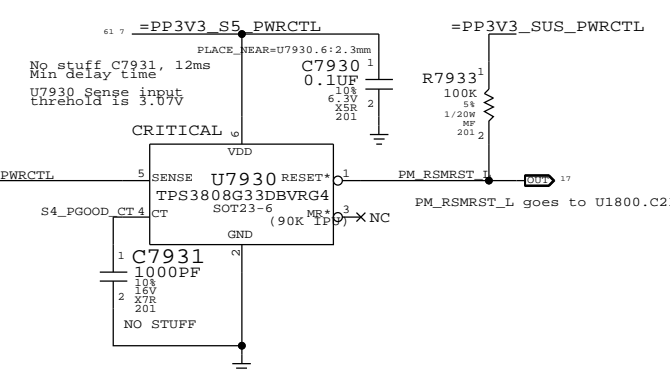
S0 ENABLE



3.3V/5.0V Sus ENABLE

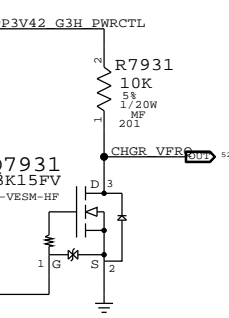


3.3V SUS Detect

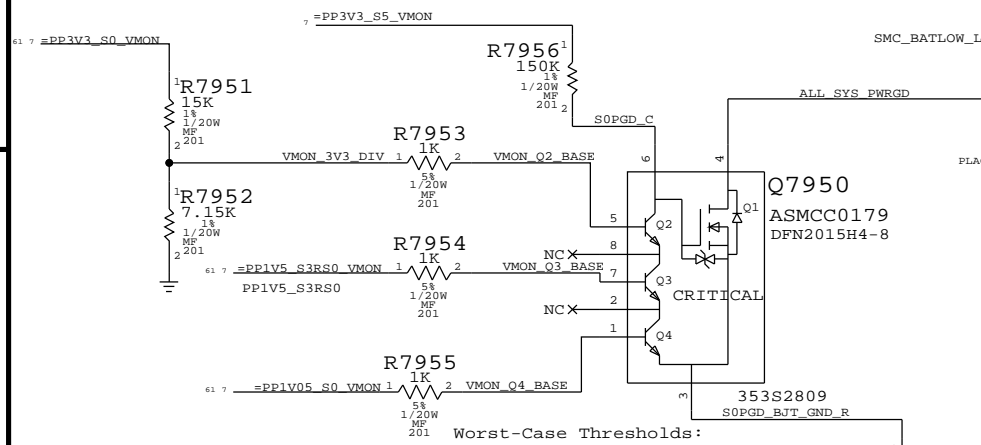


VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

CHGR VFRQ Generation



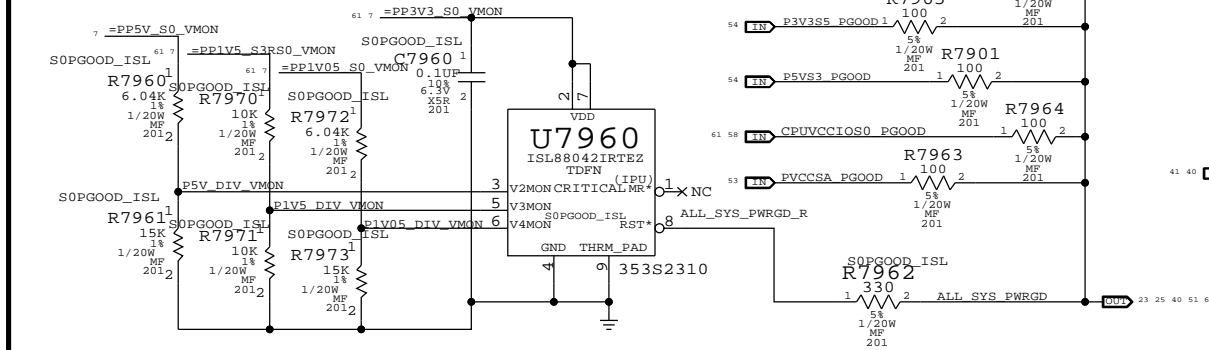
S0 Rail PGOOD (BJT Version)



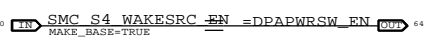
Worst-Case Thresholds:
Q2: 0.3XXV
Q3: 0.640V
3.3V w/Divider: 2.345V
Q4: 0.660V

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 2.815V-3.099V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V



DP S4 Power Enable

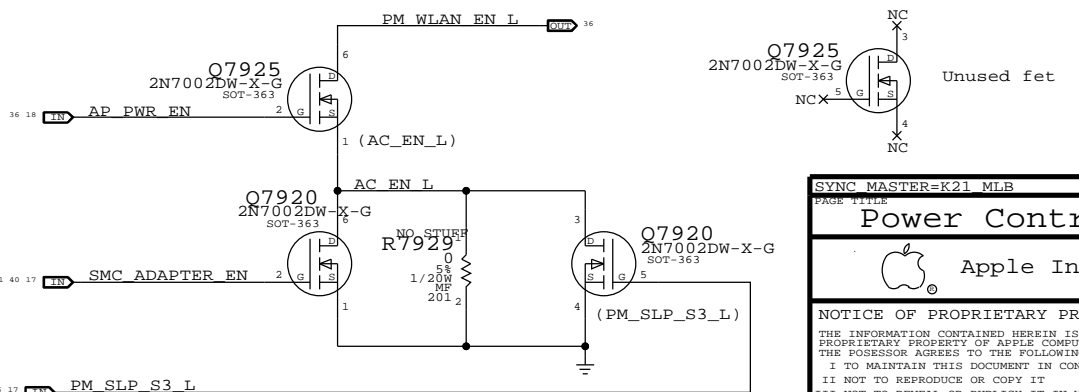


PSOC USB Power Enable



WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



SYNC MASTER=K21_MLB SYNC DATE=12/13/2010

Power Control 1/ENABLE

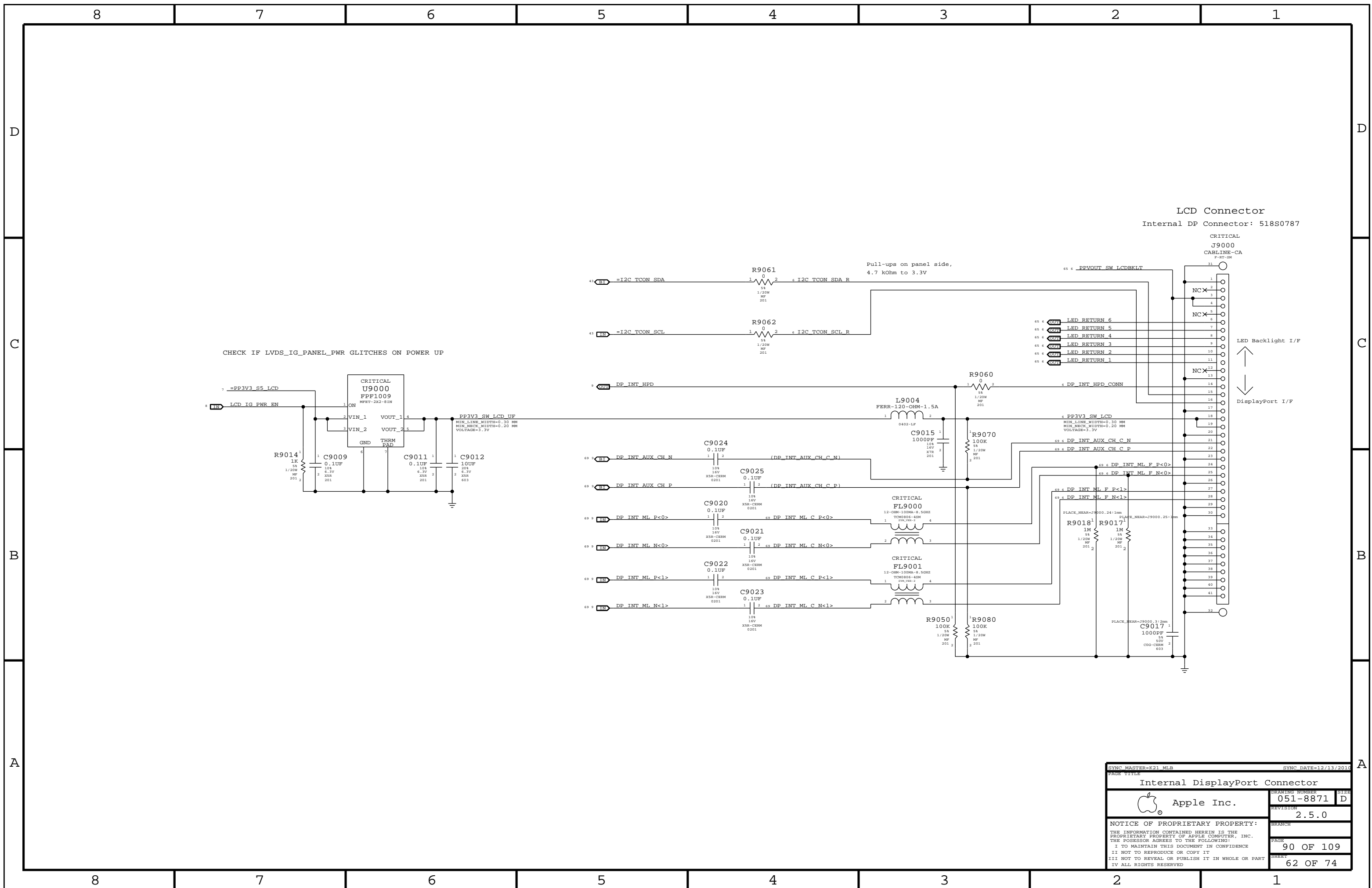
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DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

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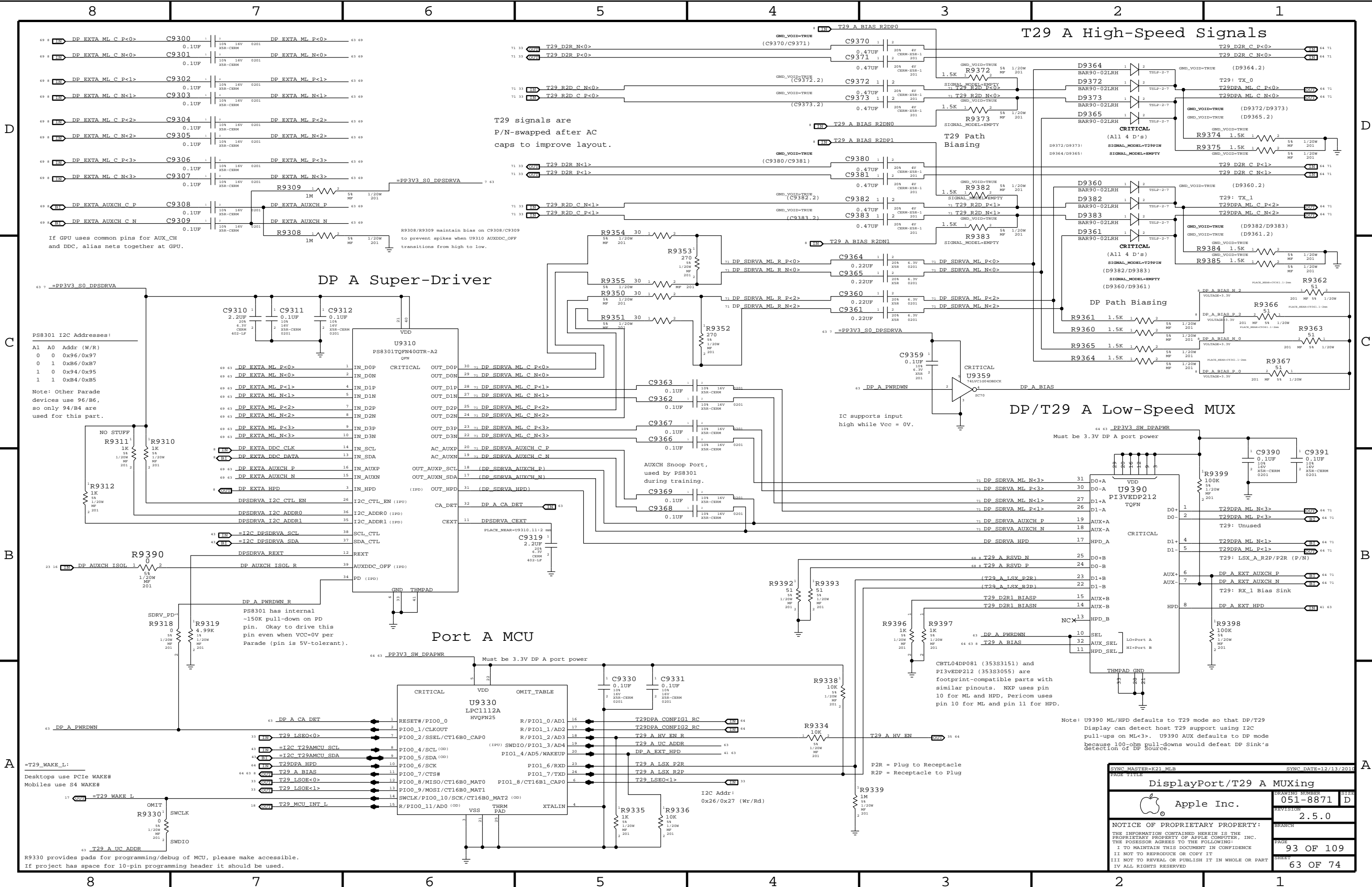
LCD Connector
Internal DP Connector: 518S0787

CRITICAL
J9000
CABLINE-CA
F-RT-SM

LED Backlight I/F
↑
DisplayPort I/F
↓

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

SYNC MASTER=K21_MLB		SYNC DATE=12/13/2011	
Internal DisplayPort Connector			
DRAWING NUMBER		051-8871	
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T29 signals are P/N-swapped after AC caps to improve layout.

PS8301 I2C Addresses:
 A1 A0 Addr (W/R)
 0 0 0x96/0x97
 0 1 0x86/0xB7
 1 0 0x94/0x95
 1 1 0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

PS8301 has internal -150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

AUXCH Snoop Port, used by PS8301 during training.

IC supports input high while Vcc = 0V.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

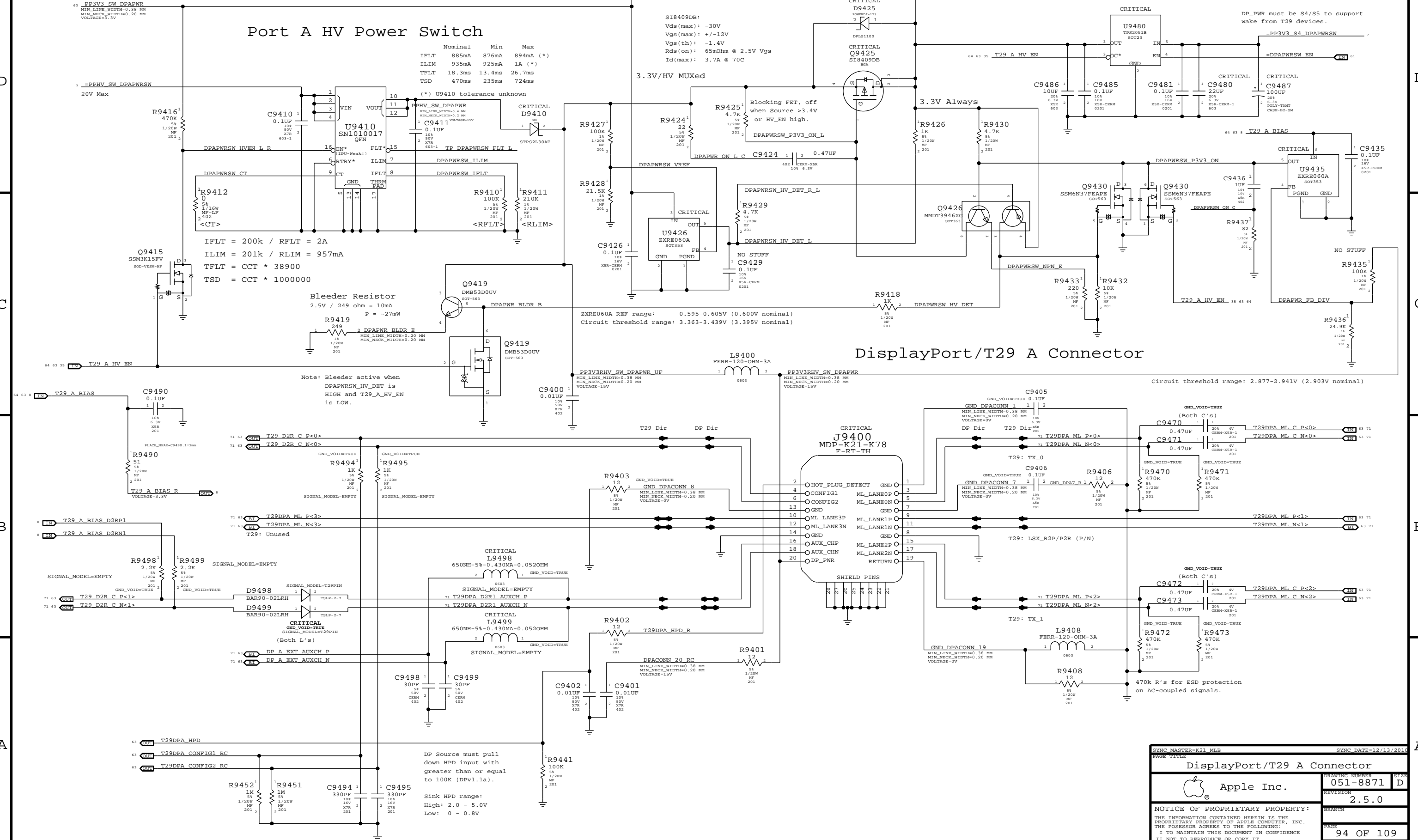
R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

SYNC MASTER=K21 MLB		SYNC DATE=12/13/2011	
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3.3V/HV Power MUX

Port A 3.3V Power Switch

Port A HV Power Switch



	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	1A (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

3.3V/HV MUXED

3.3V Always

DisplayPort/T29 A Connector

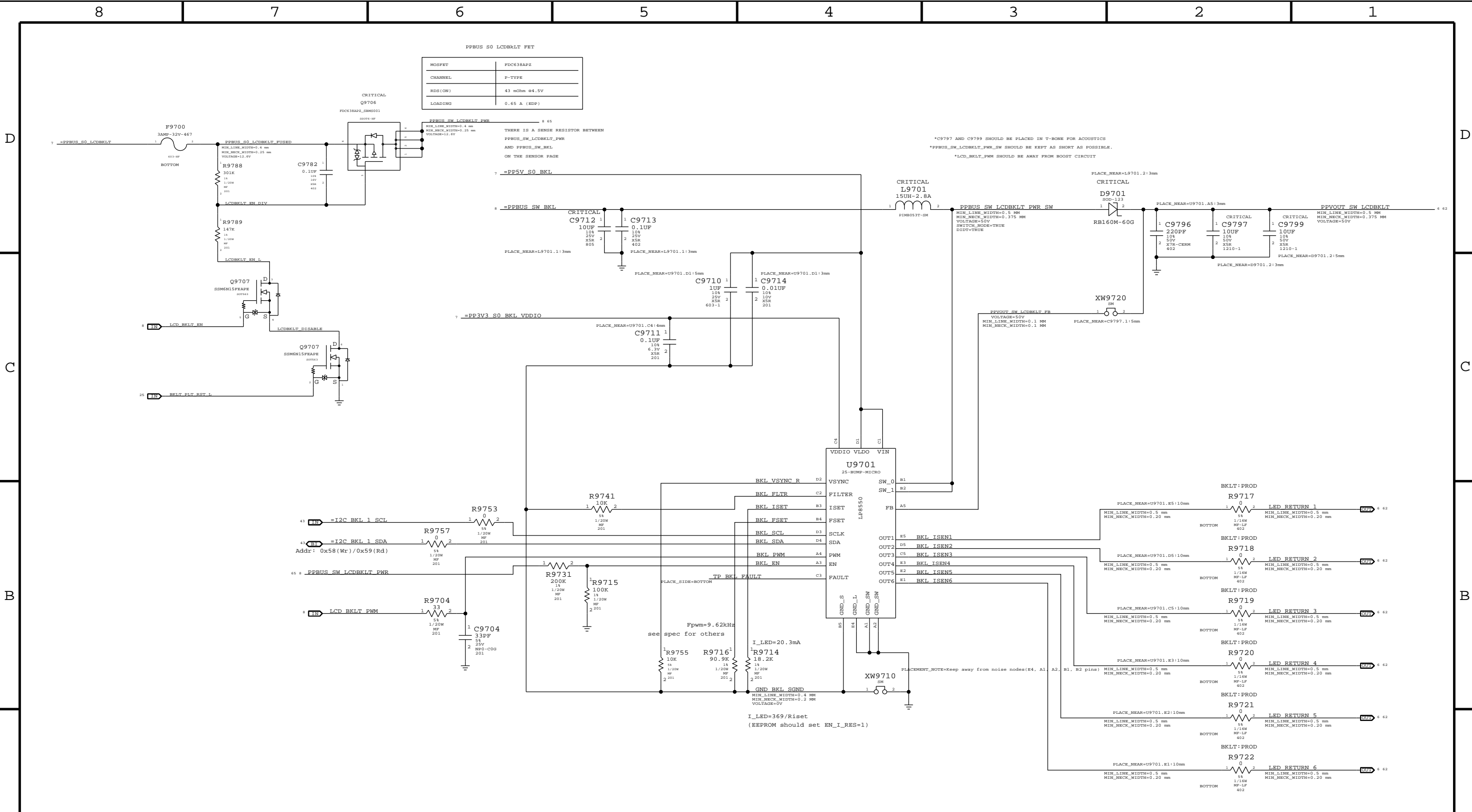
Circuit threshold range: 2.877-2.941V (2.903V nominal)

DP Source must pull down HPD input with greater than or equal to 100k (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC MASTER=K21.MLB		SYNC DATE=12/13/2011	
PAGE TITLE			
DisplayPort/T29 A Connector		DRAWING NUMBER	SIZE
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PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APE
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EOP)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9717, R9718, R9719		BKLT:ENG
103S0198	3	RES, THIN FILM, 1/16W, 10.2 OHM, 0.1, 0402, SM	R9720, R9721, R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K21_MLB SYNC DATE=12/13/2011

PAGE TITLE: LCD Backlight Driver

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BRANCH: PAGE: 97 OF 109 SHEET: 65 OF 74

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	-55_OHM_SE	-50_OHM_SE	-50_OHM_SE	-50_OHM_SE	-STANDARD	-STANDARD
CPU_55S	*	-55_OHM_SE	-55_OHM_SE	-55_OHM_SE	-55_OHM_SE	-STANDARD	-STANDARD
CPU_27P4S	*	-27P4_OHM_SE	-27P4_OHM_SE	-27P4_OHM_SE	-27P4_OHM_SE	7 MIL	7 MIL
CPU_XDP_BPM	TOP,BOTTOM	100 MIL	100 MIL	100 MIL	100 MIL	-STANDARD	-STANDARD
CPU_XDP_BPM	*	+CPU_50S	+CPU_50S	+CPU_50S	+CPU_50S	-STANDARD	-STANDARD

NOTE: CPU_XDP_BPM physical constraint is to prevent routing on outer layers.
 NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	-STANDARD	?	CPU_AGTL	TOP,BOTTOM	-2x_DIELECTRIC	?
CPU_BML	*	8 MIL	?				
CPU_COMP	*	20 MIL	?				
CPU_ITP	*	+2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended.
 Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
CLK_PCIE_90D	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	+3x_DIELECTRIC	?	PCIE	TOP,BOTTOM	+4x_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
DMI_S2N	PCIE_85D	PCIE		DMI S2N P<3:0> 9 17
DMI_S2N	PCIE_85D	PCIE		DMI S2N N<3:0> 9 17
DMI_N2S	PCIE_85D	PCIE		DMI N2S P<3:0> 9 17
DMI_N2S	PCIE_85D	PCIE		DMI N2S N<3:0> 9 17
FDI_DATA	PCIE_85D	PCIE		FDI DATA P<7:0> 9 17
FDI_DATA	PCIE_85D	PCIE		FDI DATA N<7:0> 9 17
	CPU_50S	CPU_AGTL		FDI FSYNCL<1..0> 9 17
	CPU_50S	CPU_AGTL		FDI LSYNCL<1..0> 9 17
	CPU_50S	CPU_AGTL		FDI INT 9 17
	CPU_50S	PCIE		CPU PECCI 10 19 40
PM_SYNC	CPU_50S	CPU_AGTL		PM SYNC 10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL		PM MEM PWRGD 10 17 26
	CPU_50S	CPU_ITP		XDP DBRESET L 10 23 25
	CPU_50S	CPU_ITP		XDP CPU PRDY L 10 23
	CPU_50S	CPU_ITP		XDP CPU PREO L 10 23
	CPU_50S	CPU_AGTL		PM EXT TS L<0> 10
	CPU_50S	CPU_AGTL		PM EXT TS L<1> 10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP		CPU SM RCOMP<0> 10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP		CPU SM RCOMP<1> 10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP		CPU SM RCOMP<2> 10
	CPU_50S	CPU_ITP		CPU CFG<11..0> 9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL		CPU CATERR L 10
	CPU_50S	CPU_AGTL		CPU VCCIO SEL 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL		CPU PROCHOT L 10 41 56
CPU_PWRGD	CPU_50S	CPU_AGTL		CPU PWRGD 10 19 23
PM_THERMTRIP_L	CPU_50S	CPU_BMTL		PM THERMTRIP L 10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE		DMI CLK100M CPU P 10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE		DMI CLK100M CPU N 10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE		DPLL REF CLK 8 10
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE		DPLL REF CLKN 8 10
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE		ITPCPU CLK100M P 10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE		ITPCPU CLK100M N 10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE		ITPXDP CLK100M P 16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE		ITPXDP CLK100M N 16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE		XDP CPU CLK100M P 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE		XDP CPU CLK100M N 23
	CPU_27P4S	CPU_COMP		EDP COMP 9
	CPU_27P4S	CPU_COMP		CPU PEG COMP 9
XDP_TDI	CPU_50S	CPU_ITP		XDP CPU TDI 10 23
XDP_TDO	CPU_50S	CPU_ITP		XDP CPU TDO 10 23
XDP_TMS	CPU_50S	CPU_ITP		XDP CPU TMS 10 23
XDP_TCK	CPU_50S	CPU_ITP		XDP CPU TCK 10 23
XDP_TRST_L	CPU_50S	CPU_ITP		XDP CPU TRST L 10 23
XDP_BPM_L	CPU_XDP_BPM	CPU_ITP		XDP BPM L<7..0> 10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP		CPU CFG<15..12> 9 23
(ESP_CREST_L)	CPU_50S	CPU_ITP		XDP CPURST L 23
CPU_VCCXNG_SENSE	CPU_27P4S	CPU_VCCSENSE		CPU VCCSENSE P 12 56
CPU_VCCXNG_SENSE	CPU_27P4S	CPU_VCCSENSE		CPU VCCSENSE N 12 56
CPU_VCCIOSENSE	CPU_27P4S	CPU_VCCIOSENSE		CPU VCCIOSENSE P 12 58
CPU_VCCIOSENSE	CPU_27P4S	CPU_VCCIOSENSE		CPU VCCIOSENSE N 12 58
CPU_VCCXNG_SENSE	CPU_27P4S	CPU_VCCSENSE		CPU AXG SENSE P 12 56
CPU_VCCXNG_SENSE	CPU_27P4S	CPU_VCCSENSE		CPU AXG SENSE N 12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE		CPU VDDO SENSE P 12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE		CPU VDDO SENSE N 12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE		CPU AXG VALSENSE P 9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE		CPU AXG VALSENSE N 9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE		CPU VCC VALSENSE P 9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE		CPU VCC VALSENSE N 9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP		CPU VIDALERT_L 12 56
CPU_SVIDSCLK	CPU_50S	CPU_COMP		CPU VIDSCLK 12 56
CPU_SVIDSOUT	CPU_50S	CPU_COMP		CPU VIDSOUT 12 56
	PCIE_85D	PCIE		PEG R2D P<15..0> 8
	PCIE_85D	PCIE		PEG R2D N<15..0> 8
	PCIE_85D	PCIE		PEG R2D C P<15..0> 8
	PCIE_85D	PCIE		PEG R2D C N<15..0> 8
	PCIE_85D	PCIE		PEG D2R P<15..0> 8
	PCIE_85D	PCIE		PEG D2R N<15..0> 8
	PCIE_85D	PCIE		PEG D2R C P<15..0> 8
	PCIE_85D	PCIE		PEG D2R C N<15..0> 8

CPU_VCCSA_VID<0>
 CPU_VCCSA_VID<1>

SYNOPSIS: CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37E	*	+37_OHM_SE	+37_OHM_SE	+37_OHM_SE	+37_OHM_SE	-STANDARD	-STANDARD
MEM_40E	*	+40_OHM_SE	+40_OHM_SE	+40_OHM_SE	+40_OHM_SE	-STANDARD	-STANDARD
MEM_55E	*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	-STANDARD	-STANDARD
MEM_72D	*	+72_OHM_DIFF	+72_OHM_DIFF	+72_OHM_DIFF	+72_OHM_DIFF	-STANDARD	-STANDARD
MEM_50S	TOP_BOTTOM	Y	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	-STANDARD	-STANDARD
MEM_85D	TOP_BOTTOM	Y	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	-STANDARD	-STANDARD
MEM_50S	ISL3, ISL4, ISL9, ISL10	Y	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	-STANDARD	-STANDARD
MEM_85D	ISL3, ISL4, ISL9, ISL10	Y	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	-STANDARD	-STANDARD

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_S2SR	*	+DNR_P2MM	?
MEM_S2SD	*	+GND_P2MM	?
MEM_S2SBR	*	0.6 MM	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_S2SR
MEM_CTRL	MEM_PWR	*	MEM_S2SR
MEM_CMD	MEM_PWR	*	MEM_S2SR
MEM_DATA	MEM_PWR	*	MEM_S2SR
MEM_DQS	MEM_PWR	*	MEM_S2SR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_S2SD
MEM_CTRL	GND	*	MEM_S2SD
MEM_CMD	GND	*	MEM_S2SD
MEM_DATA	GND	*	MEM_S2SD
MEM_DQS	GND	*	MEM_S2SD

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow xPGA guidelines per Huron River SFF DG rev1.0 (#438297).
 DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
 DQ to DQS matching per byte lane should be within 0.127mm.
 DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
 CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
 CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
 A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
 DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
 Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from processor ball to SODIMM pad is 88.9mm.
 SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	PROPERTY	VALUE	MIN	MAX
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32		
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM A CKE<3..0>	8 11 27 28 32		
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM A CS L<3..0>	8 11 27 28 32		
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM A ODT<3..0>	8 11 27 28 32		
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM A A<15..0>	8 11 27 28 32		
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM A BA<2..0>	11 27 28 32		
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM A RAS L	11 27 28 32		
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM A CAS L	11 27 28 32		
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM A WE L	11 27 28 32		
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_DATA	MEM A DQ<7..0>	11 27		
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<15..8>	11 27		
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<23..16>	11 27		
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<31..24>	11 27		
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<39..32>	11 28		
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<47..40>	11 28		
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<55..48>	11 28		
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_DATA	MEM A DO<63..56>	11 28		
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<0>	11 27		
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<0>	11 27		
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<1>	11 27		
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<1>	11 27		
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<2>	11 27		
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<2>	11 27		
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<3>	11 27		
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<3>	11 27		
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<4>	11 28		
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<4>	11 28		
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<5>	11 28		
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<5>	11 28		
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<6>	11 28		
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<6>	11 28		
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS P<7>	11 28		
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM A DOS N<7>	11 28		
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32		
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32		
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM B CKE<3..0>	8 11 29 30 32		
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM B CS L<3..0>	8 11 29 30 32		
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM_CTRL	MEM B ODT<3..0>	8 11 29 30 32		
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM B A<15..0>	8 11 29 30 32		
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM B BA<2..0>	11 29 30 32		
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM B RAS L	11 29 30 32		
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM B CAS L	11 29 30 32		
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_CMD	MEM B WE L	11 29 30 32		
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_DATA	MEM B DQ<7..0>	11 29		
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<15..8>	11 29		
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<23..16>	11 29		
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<31..24>	11 29		
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<39..32>	11 30		
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<47..40>	11 30		
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<55..48>	11 30		
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_DATA	MEM B DO<63..56>	11 30		
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<0>	11 29		
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<0>	11 29		
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<1>	11 29		
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<1>	11 29		
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<2>	11 29		
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<2>	11 29		
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<3>	11 29		
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<3>	11 29		
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<4>	11 30		
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<4>	11 30		
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<5>	11 30		
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<5>	11 30		
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<6>	11 30		
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<6>	11 30		
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS P<7>	11 30		
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_DQS	MEM B DOS N<7>	11 30		
		MEM_PWR		PP1V5 S3RS0	6 7		
		MEM_PWR		PP1V5 S3	6 7		
		MEM_PWR		PP0V75 S3 MEM VREFCA A	27 28 29 30 31		
		MEM_PWR		PP0V75 S3 MEM VREFDO A	9 27 28 29 30 31		

SYMC: MEMPHYS-CONSTRAINTS		SYMC: DATA-04/06/2011	
PAGE TITLE			
Memory Constraints			
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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	-85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
LVDS_90D	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	+3x_DIELECTRIC	?	DISPLAYPORT	TOP_BOTTOM	+4x_DIELECTRIC	?
LVDS	*	+3x_DIELECTRIC	?	LVDS	TOP_BOTTOM	+4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	+4x_DIELECTRIC	?	SATA	TOP_BOTTOM	+3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCB_USB_BIAS	*	-STANDARD	8 MIL	8 MIL	-STANDARD	-STANDARD	-STANDARD
USB_85D	*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	+2x_DIELECTRIC	?	USB	TOP_BOTTOM	+4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
DP_ML	DP_85D	DISPLAYPORT		DP IG ML P<3..0>
DP_ML	DP_85D	DISPLAYPORT		DP IG ML N<3..0>
DP_EXTN_AUXCH	DP_85D	DISPLAYPORT		DP IG AUX CH P
DP_EXTN_AUXCH	DP_85D	DISPLAYPORT		DP IG AUX CH N
LVDS_IG_A_CLK	LVDS_90D	LVDS		LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_90D	LVDS		LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_90D	LVDS		LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_90D	LVDS		LVDS IG A DATA N<2..0>
	LVDS_90D	LVDS		LVDS IG A DATA P<3>
	LVDS_90D	LVDS		LVDS IG A DATA N<3>
	LVDS_90D	LVDS		LVDS IG B DATA P<3..0>
	LVDS_90D	LVDS		LVDS IG B DATA N<3..0>
	LVDS_90D	LVDS		LVDS IG B CLK P
	LVDS_90D	LVDS		LVDS IG B CLK N
	SATA_90D	SATA		SATA HDD R2D C P
	SATA_90D	SATA		SATA HDD R2D C N
	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P
	SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N
	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA		SATA HDD D2R C P
	SATA_90D	SATA		SATA HDD D2R C N
	SATA_90D	SATA		SATA ODD R2D C P
	SATA_90D	SATA		SATA ODD R2D C N
	SATA_90D	SATA		SATA ODD R2D P
	SATA_90D	SATA		SATA ODD R2D N
	SATA_90D	SATA		SATA ODD D2R P
	SATA_90D	SATA		SATA ODD D2R N
	SATA_90D	SATA		SATA HDD R2D RC P
	SATA_90D	SATA		SATA HDD R2D RC N
	SATA_90D	SATA		SATA HDD D2R RC P
	SATA_90D	SATA		SATA HDD D2R RC N
PCH_SATA_ICOMP		SATA_ICOMP		PCH_SATAICOMP
USB_HUB1_UP	USB_85D	USB		USB_HUB1_UP_P
	USB_85D	USB		USB_HUB1_UP_N
USB_HUB2_UP	USB_85D	USB		USB_HUB2_UP_P
	USB_85D	USB		USB_HUB2_UP_N
USB_EXTN	USB_85D	USB		USB_EXTN_P
	USB_85D	USB		USB_EXTN_N
USB_EXTR	USB_85D	USB		USB_EXTR_P
	USB_85D	USB		USB_EXTR_N
USB_EXTC	USB_85D	USB		USB_EXTC_P
	USB_85D	USB		USB_EXTC_N
USB_EXTD	USB_85D	USB		USB_EXTD_P
	USB_85D	USB		USB_EXTD_N
USB_EXTD	USB_85D	USB		USB_T29A_P
	USB_85D	USB		USB_T29A_N
	USB_85D	USB		T29 A RSVD P
	USB_85D	USB		T29 A RSVD N
USB_CAMERA	USB_85D	USB		USB_CAMERA_P
	USB_85D	USB		USB_CAMERA_N
USB_CAMERA	USB_85D	USB		USB_CAMERA_CONN_P
	USB_85D	USB		USB_CAMERA_CONN_N
USB_BT	USB_85D	USB		USB_BT_P
	USB_85D	USB		USB_BT_N
USB_TPAD	USB_85D	USB		USB_TPAD_P
	USB_85D	USB		USB_TPAD_N
USB_IR	USB_85D	USB		USB_IR_P
	USB_85D	USB		USB_IR_N
USB_SDCARD	USB_85D	USB		USB_SDCARD_P
	USB_85D	USB		USB_SDCARD_N
USB_BRCRYPT	USB_85D	USB		USB_BRCRYPT_P
	USB_85D	USB		USB_BRCRYPT_N
PCH_USB_BIAS	PCH_USB_BIAS			PCH_USB_BIAS
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE		PCIE_CLK100M_PCH_P
	CLK_PCIE_90D	CLK_PCIE		PCIE_CLK100M_PCH_N
	CLK_PCIE_90D	CLK_PCIE		FSB_CLK133M_PCH_P
	CLK_PCIE_90D	CLK_PCIE		FSB_CLK133M_PCH_N
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE		PCH_CLK96M_DOT_P
	CLK_PCIE_90D	CLK_PCIE		PCH_CLK96M_DOT_N
PCH_DIFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE		PCH_CLK100M_SATA_P
	CLK_PCIE_90D	CLK_PCIE		PCH_CLK100M_SATA_N
	CPH_50S	CLK_PCIE		PCH_CLK14P3M_REFCLK
	CPH_50S	CLK_PCIE		PCH_CLK33M_PCIEIN
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE		GFX_CLK120M_DPLLSS_P
	CLK_PCIE_90D	CLK_PCIE		GFX_CLK120M_DPLLSS_N

SYNOPSIS: PCH Constraints 1
 DRAWING NUMBER: 051-8871
 REVISION: 2.5.0
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LPC Bus Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include LPC_50S and CLK_LPC_50S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include LPC and CLK_LPC.

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes SMB_50S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes SMB.

HD Audio Interface Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes HDA_50S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes HDA.

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes CLK_SLOW_55S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes CLK_SLOW.

SPI Interface Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes SPT_55S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes SPT.

DisplayPort Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes DP_85D.

Table with 8 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes DISPLAYPORT.

PCI-Express Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include PCIe_85D and CLK_Pcie_90D.

Table with 8 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes PCIe.

System Clock Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include CLK_SLOW_55S and CLK_25M_55S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include CLK_SLOW and CLK_25M.

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists various electrical constraints for PCH nets like IEC_AD, SMBUS_PCH_CLK, HDA_BIT_CLK, etc.

Chipset Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists various electrical constraints for chipset nets like DP_EXTA_ML, PCIE_T29_R2D_C, etc.

Clock Net Properties

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists clock net properties like SYSCLK_CLK32K_RTC, SYSCLK_CLK25M_SB, etc.

Apple Inc. PCH Constraints 2. Drawing number 051-8871. Revision 2.5.0. Includes a notice of proprietary property and page information (103 OF 109, 69 OF 74).

CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50G	*	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	+50_OHM_SE	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	+3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	+110_OHM_DIFF	+110_OHM_DIFF	+110_OHM_DIFF	+110_OHM_DIFF	+110_OHM_DIFF	+110_OHM_DIFF


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	+3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	ENET_50S	ENET_3X	BCM5764 CLK25M XTALI
	ENET_50S	ENET_3X	BCM5764 CLK25M XTALO
	ENET_50S	ENET_3X	ENET RESET L
	ENET_100D	ENET_MDI	ENET MDI P<3..0>
	ENET_100D	ENET_MDI	ENET MDI N<3..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
	ENET_50S	ENET_CR_DATA	SDCONN DATA<7..0>
	ENET_50S	ENET_CR_DATA	SDCONN CMD
	ENET_50S	ENET_CR_DATA	SDCONN CLK

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	FW_110D	FW_TP	FW P0 TPA P
	FW_110D	FW_TP	FW P0 TPA N
	FW_110D	FW_TP	FW P0 TPB P
	FW_110D	FW_TP	FW P0 TPB N
	FW_110D	FW_TP	FW P1 TPA P
	FW_110D	FW_TP	FW P1 TPA N
	FW_110D	FW_TP	FW P1 TPB P
	FW_110D	FW_TP	FW P1 TPB N
	Port 2 Not Used		

SYMC_MASTER-CONSTRAINTS		SYMC_DATE=04/05/2011	
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Ethernet/FW Constraints			
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	+2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	-STANDARD	-STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	+2x_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF	+80_OHM_DIFF
T29DP_100D	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	+5x_DIELECTRIC	?	T29DP	TOP_BOTTOM	+7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0> 8 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0> 8 33
DP_T29SNK0_MI	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0> 33
DP_T29SNK0_MI	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0> 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P 8 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N 8 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0> 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0> 33
DP_T29SNK1_MI	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0> 33
DP_T29SNK1_MI	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0> 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P 33
DP_85D	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N 33
T29_I2C_55S	T29_I2C	I2C T29 SCL	33 43
T29_I2C_55S	T29_I2C	I2C T29 SDA	33 43
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK 33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI MOSI 33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI MISO 33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI CS L 33
T29DP_80D	T29DP	T29 R2D C P<3..0>	33 63
T29DP_80D	T29DP	T29 R2D C N<3..0>	33 63
T29DP_80D	T29DP	T29 D2R P<3..0>	33 63
T29DP_80D	T29DP	T29 D2R N<3..0>	33 63
T29DP_80D	T29DP	T29 R2D P<0>	63
T29DP_80D	T29DP	T29 R2D N<0>	63
T29DP_80D	T29DP	T29 R2D P<1>	63
T29DP_80D	T29DP	T29 R2D N<1>	63
T29DP_80D	T29DP	T29 R2D C F P<1..0>	63
T29DP_80D	T29DP	T29 R2D C F N<1..0>	63
T29DP_80D	T29DP	T29 D2R C P<0>	63 64
T29DP_80D	T29DP	T29 D2R C N<0>	63 64
T29DP_80D	T29DP	T29 D2R C P<1>	63 64
T29DP_80D	T29DP	T29 D2R C N<1>	63 64
T29DP_80D	T29DP	T29DPA D2R1 AUXCH P	64
T29DP_80D	T29DP	T29DPA D2R1 AUXCH N	64
T29DP_80D	T29DP	DP SDRVA ML C P<3..0>	63
T29DP_80D	T29DP	DP SDRVA ML C N<3..0>	63
T29DP_80D	T29DP	DP SDRVA ML R P<3..0>	63
T29DP_80D	T29DP	DP SDRVA ML R N<3..0>	63
DP_SDRVA_MI_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<0>
DP_SDRVA_MI_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<0>
DP_SDRVA_MI_ODD	T29DP_80D	T29DP	DP SDRVA ML P<1>
DP_SDRVA_MI_ODD	T29DP_80D	T29DP	DP SDRVA ML N<1>
DP_SDRVA_MI_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<2>
DP_SDRVA_MI_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<2>
DP_SDRVA_MI_ODD	T29DP_80D	T29DP	DP SDRVA ML P<3>
DP_SDRVA_MI_ODD	T29DP_80D	T29DP	DP SDRVA ML N<3>
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH P
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH N
T29DP_80D	T29DP	T29DP	DP SDRVA AUXCH C P
T29DP_80D	T29DP	T29DP	DP SDRVA AUXCH C N
T29DPA_MI_ODD			T29DPA ML P<1>
T29DPA_MI_ODD			T29DPA ML N<1>
T29DPA_MI_ODD			T29DPA ML P<3>
T29DPA_MI_ODD			T29DPA ML N<3>
T29DP_80D	T29DP	T29DP	T29DPA ML P<3..0>
T29DP_80D	T29DP	T29DP	T29DPA ML N<3..0>
T29DP_80D	T29DP	T29DP	T29DPA ML C P<3..0>
T29DP_80D	T29DP	T29DP	T29DPA ML C N<3..0>
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP A EXT AUXCH P
DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP A EXT AUXCH N

T29 IC Net Properties

T29/DP Net Properties

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	-STANDARD	-STANDARD	-STANDARD	-STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB		SMBUS_SMC_A_S3_SCL 43
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB		SMBUS_SMC_A_S3_SDA 43
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB		SMBUS_SMC_B_S0_SCL 43
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB		SMBUS_SMC_B_S0_SDA 43
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB		SMBUS_SMC_0_S0_SCL 43
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB		SMBUS_SMC_0_S0_SDA 43
SMBUS_SMC_BSA_SCL	SMB_50S	SMB		SMBUS_SMC_BSA_SCL 43
SMBUS_SMC_BSA_SDA	SMB_50S	SMB		SMBUS_SMC_BSA_SDA 43
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB		SMBUS_SMC_MGMT_SCL 43
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB		SMBUS_SMC_MGMT_SDA 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
CHGR_CSI	1T01_DIFFPAIR			CHGR_CSI_P 92
	1T01_DIFFPAIR			CHGR_CSI_N 92
CHGR_CSO	1T01_DIFFPAIR			CHGR_CSO_P 92
	1T01_DIFFPAIR			CHGR_CSO_N 92

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SMC CONSTRAINTS		SMC CONSTRAINTS	
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_1T01_55S	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR	+55_OHM_SE	+55_OHM_SE	+55_OHM_SE	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	+2:1_SPACING	?
THERM	*	+2:1_SPACING	?
AUDIO	*	+2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	+STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P20M
MEM_CMD	GND	*	GND_P20M
MEM_CTRL	GND	*	GND_P20M
MEM_DATA	GND	*	GND_P20M
MEM_SQS	GND	*	GND_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
MEM_72D	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
MEM_72S	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
MEM_85D	*	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
PCIE_85D	*	OVERWRITE	OVERWRITE	0.076 MM	10 MM	OVERWRITE	OVERWRITE
USB_85D	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
CPU_27P4S	TOP	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE
CLK_PCIE_85D	TOP	OVERWRITE	OVERWRITE	0.09 MM	400 MIL	OVERWRITE	OVERWRITE

A Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
ENET_100D	ENETCONN	ENETCONN	ENETCONN P<3..0>
ENET_100D	ENETCONN	ENETCONN	ENETCONN N<3..0>
SATA_90D	SATA	SATA	SATA ODD D2R UF P
SATA_90D	SATA	SATA	SATA ODD D2R UF N
SATA_90D	SATA	SATA	SATA HDD D2R RDRVR OUT P
SATA_90D	SATA	SATA	SATA HDD D2R RDRVR OUT N
SATA_90D	SATA	SATA	SATA HDD R2D RDRVR IN P
SATA_90D	SATA	SATA	SATA HDD R2D RDRVR IN N
SATA_90D	SATA	SATA	SATA HDD D2R RDRVR IN P
SATA_90D	SATA	SATA	SATA HDD D2R RDRVR IN N
SATA_90D	SATA	SATA	SATA HDD R2D RDRVR OUT P
SATA_90D	SATA	SATA	SATA HDD R2D RDRVR OUT N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU THMSNS D2 P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	CPU THMSNS D2 N
CPU_THERMD	THERM_1T01_55S	THERM	CPU THERMD P
CPU_THERMD	THERM_1T01_55S	THERM	CPU THERMD N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29 THERMD P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29 THERMD N
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29 MLBBOT THMSNS P
SENSE_DIFFPAIR	THERM_1T01_55S	THERM	T29 MLBBOT THMSNS N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HS COMPUTING N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HS COMPUTING P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HS OTHER N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HS OTHER P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0 CS N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUVCCIOS0 CS P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS1 P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS1 N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS2 P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS2 N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS1G P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS1G N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISUM R P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISUM R N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISUMG R P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISUMG R N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISNS N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSAS0 CS P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	VCCSAS0 CS N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISUMG P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	CPUI MVP ISUMG N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS CPU N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS CPU P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HDD N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HDD P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HDD R N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS HDD R P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LCDBKLT P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS ODD N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS ODD P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS ODD R N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS ODD R P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LV5 S3 N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS LV5 S3 P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS P1V8GPU R N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS P1V8GPU R P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS AIRPORT N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	ISNS AIRPORT P
LVDS_90D	LVDS	LVDS	LVDS CONN A CLK F N
LVDS_90D	LVDS	LVDS	LVDS CONN A CLK F P

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP INR P
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP INR N
MAX98300_R	DIFFPAIR	AUDIO	MAX98300 R P
MAX98300_R	DIFFPAIR	AUDIO	MAX98300 R N

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN P
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN N
1T01_DIFFPAIR			CHGR CSI R P
1T01_DIFFPAIR			CHGR CSI R N
1T01_DIFFPAIR			CHGR CSO R P
1T01_DIFFPAIR			CHGR CSO R N
USB_EXTN	USB_85D	USB	USB2 EXTA MUXED P
USB_EXTN	USB_85D	USB	USB2 EXTA MUXED N
USB_EXTN	USB_85D	USB	USB2 LT1 P
USB_EXTN	USB_85D	USB	USB2 LT1 N
USB_85D	USB		CONN USB2 BT P
USB_85D	USB		CONN USB2 BT N
USB_85D	USB		USB LT2 P
USB_85D	USB		USB LT2 N
DP_85D	DISPLAYPORT		DP IG AUX CH C P
DP_85D	DISPLAYPORT		DP IG AUX CH C N
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP L P OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP L N OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP SUB P OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP SUB N OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP R P OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP R N OUT
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315 SUB N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315 SUB P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315 L N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315 L P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315 R N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315 R P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD LO2 N R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD LO2 P R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD LO1 N R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD LO1 P R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD LO2 N L
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD LO2 P L
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INL P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INL N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INSUB P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INSUB N
USB_85D	USB		USB TPAD R P
USB_85D	USB		USB TPAD R N
SB_POWER			PP3V3 S5
SB_POWER			PP3V3 S0
GND			GND

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
USB_EXTN	USB_85D	USB	USB EXTA MUXED P
USB_EXTN	USB_85D	USB	USB EXTA MUXED N
USB_EXTN	USB_85D	USB	USB LT1 P
USB_EXTN	USB_85D	USB	USB LT1 N
USB_TPAD	USB_85D	USB	USB TPAD CONN P
USB_TPAD	USB_85D	USB	USB TPAD CONN N
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C SMC SMS SDA R
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C SMC SMS SCL R
SMB_55S	SMB		I2C TCON SCL
SMB_55S	SMB		I2C TCON SDA
SMB_55S	SMB		I2C TCON SCL CONN
SMB_55S	SMB		I2C TCON SDA CONN

SYMC_MATER_CONSTRAINTS PAGE TITLE SYMC_DATE=06/06/2011

Project Specific Constraints

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K901 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL. OF MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3, ISL4, ISL9, ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3, ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4, ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4, ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4, ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4, ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4, ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K901.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP, BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4, ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM


NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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