

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2010-08-05

SCHEM, FLYING_CLOUD, MLB, K90i

"EVT3" 11/22/10

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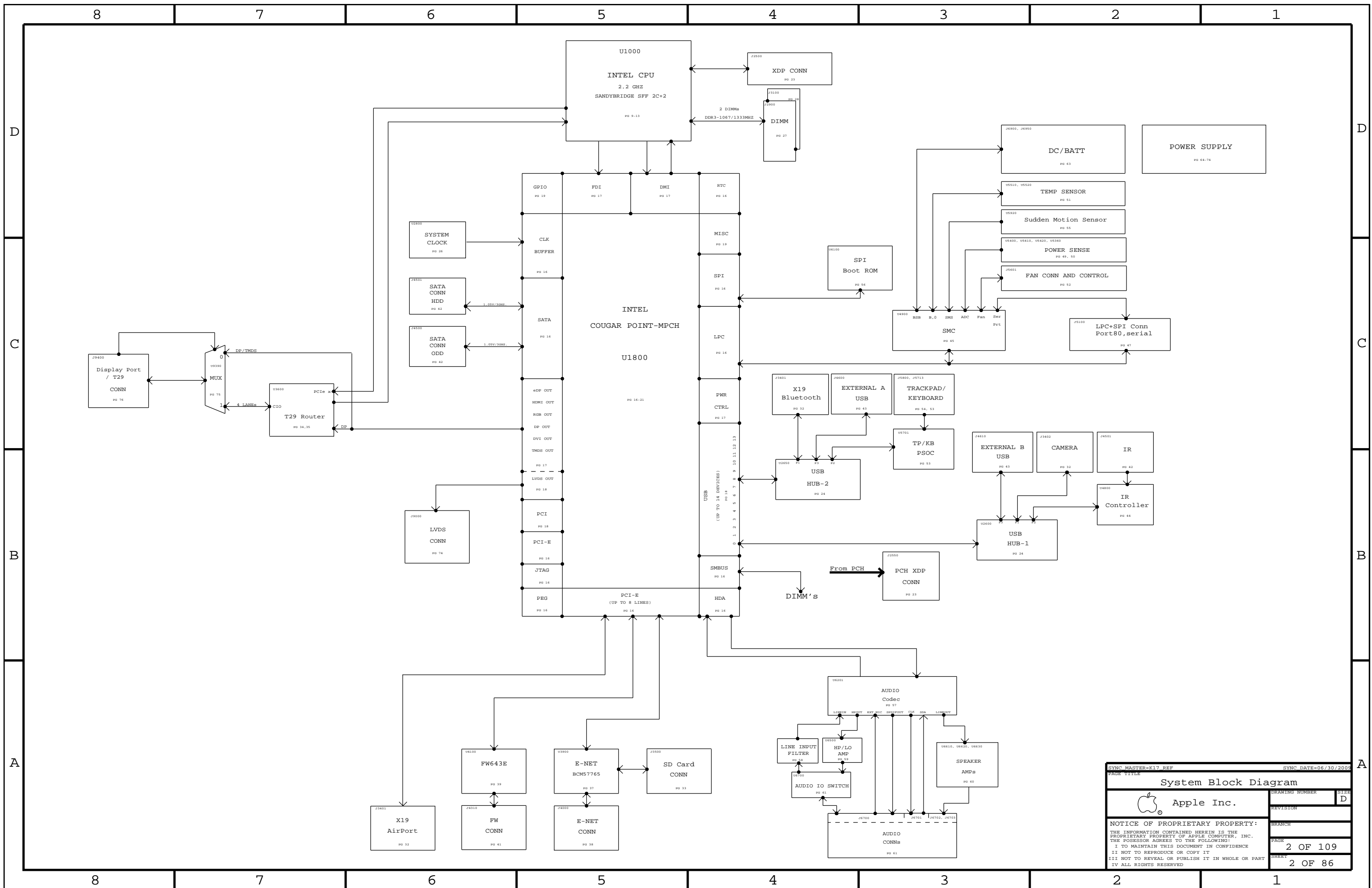
ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8658	1	SCHEM,MLB,K90I	SCH	CRITICAL	
820-2936	1	PCHP,MLB,K90I	PCB	CRITICAL	

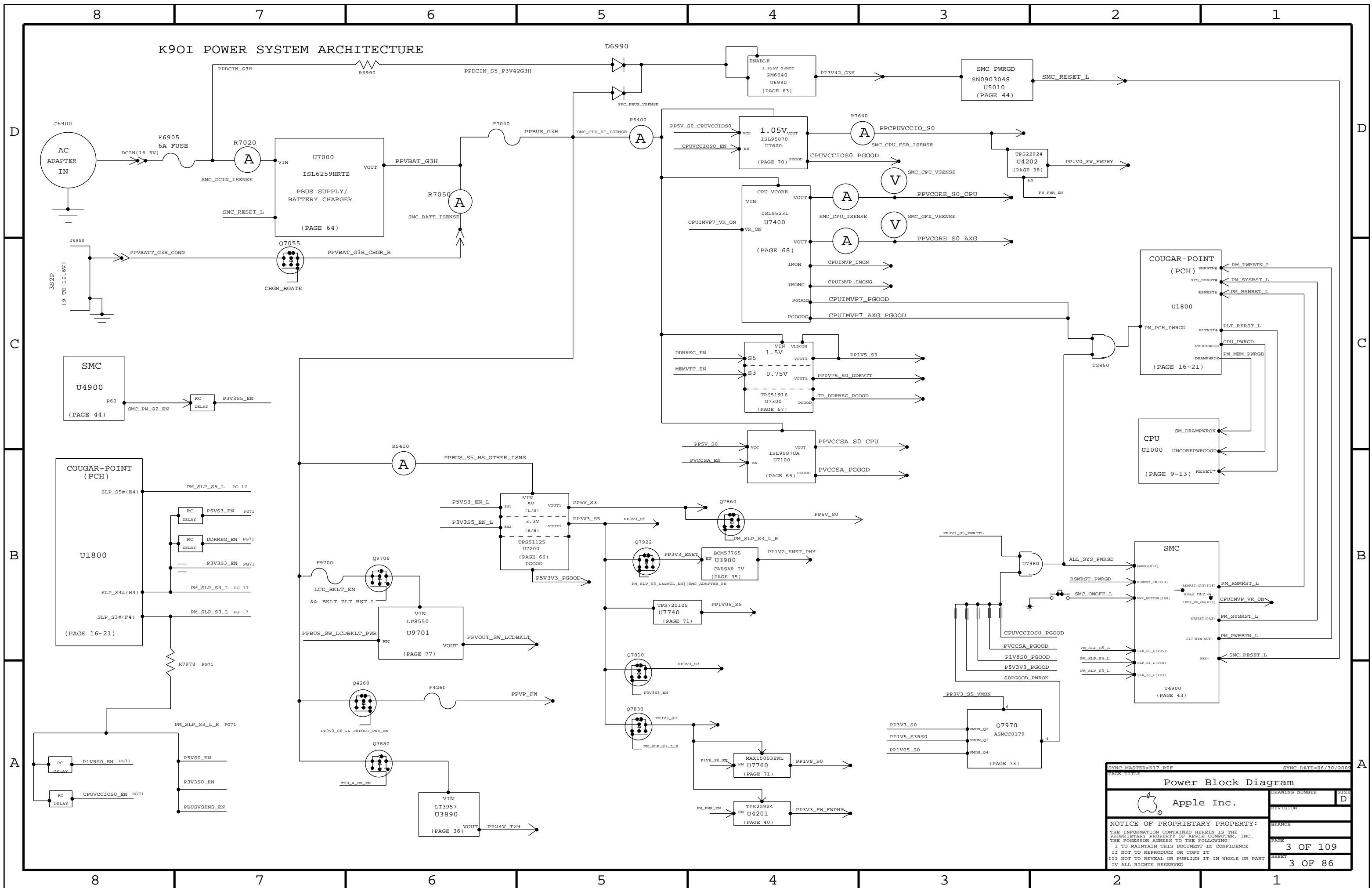
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K90I POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1294	PCBA, 2.5G, K901	K901_COMMON, CPU_2_5GHZ, EEEE_DDRQ
639-1581	PCBA, 2.7G, K901	K901_COMMON, CPU_2_7GHZ, EEEE_DH78
639-1698	PCBA, 2.6G, K901	K901_COMMON, CPU_2_6GHZ, EEEE_DH8F
639-1699	PCBA, 2.3G, K901	K901_COMMON, CPU_2_3GHZ, EEEE_DH8G
085-1998	K901 MLB DEVELOPMENT BOM	K901_DEVEL:ENG

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DDRQ]	CRITICAL	EEEE_DDRQ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH78]	CRITICAL	EEEE_DH78
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH8F]	CRITICAL	EEEE_DH8F
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEEE:DH8G]	CRITICAL	EEEE_DH8G

K901 BOM GROUPS

BOM GROUP	BOM OPTIONS
K901_COMMON	ALTERNATE, COMMON, K901_COMMON1, K901_COMMON2, K901_DEBUG:ENG, K901_PROGPARTS, USBHUB_2513B, T29BST:Y
K901_COMMON1	BATT_3S, CPUMEM_S0, SMC_DEBUG_YES, HUB1_2NONREM, HUB2_3NONREM, T29:YES, DP_SDRV:A2, SDRV_PD, SDRVI2C:MCU
K901_COMMON2	MIKEY, KB_BL
K901_PROGPARTS	BOOTROM_PROG, SMC_PROG, TPAD_PROG, ENET_PROG, T29ROM:PROG, T29MCU:PROG
K901_DEVEL:ENG	BKLT:ENG, BMON:ENG, XDP_CONN, XDP_CPU:BPM, XDP_PCH, LPCPLUS, VREFMRGN, SOPGOOD_ISL, IMPV1SMS_ENG
K901_DEVEL:PVT	LPCPLUS, XDP_CONN, XDP_PCH
K901_DEBUG:ENG	DEVEL_BOM, SMC_DEBUG_YES, XDP
K901_DEBUG:PVT	DEVEL_BOM, BKLT:PROD, BMON:PROD, SMC_DEBUG_YES, XDP, VREFMRGN_NOT
K901_DEBUG:PROD	BKLT:PROD, BMON:PROD, SMC_DEBUG_YES, XDP, VREFMRGN_NOT, LPCPLUS

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to THE Magnetec
516S0805	516S0806		ALL	Molex alt to Foxconn
128S0303	128S0282		ALL	Panasonic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
152S0778	152S0693		ALL	Cyntec alt to Vishay
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Robm alt to Toshiba
376S0927	376S0966		ALL	Fairchild alt to Renesas
376S0927	376S0790		ALL	Fairchild alt to CICOLOM
376S0960	376S0801		ALL	Renesas alt to Renesas
376S0790	376S0928		ALL	CICOLOM alt to Fairchild
376S0928	376S0895		ALL	Fairchild alt to Renesas
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0777	376S0761		ALL	AGW alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
353S3085	353S1658		ALL	StMicro alt to LT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3934	1	SNB, 2C, QXXX, RES, 2.2, 15M, B2, 3M, 0T1, BGA	U1000	CRITICAL	CPU_2_2GHZ
337S4058	1	SNB, Q18A, QS, J1, 2.5, 35M, 2+2.1.30, 3M, BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4057	1	SNB, Q183, QS, J1, 2.7, 35M, 2+2.1.30, 4M, BGA	U1000	CRITICAL	CPU_2_7GHZ
337S4024	1	SNB, Q189, QS, J1, 2.3, 35M, 2+2.1.30, 3M, BGA	U1000	CRITICAL	CPU_2_3GHZ
337S4064	1	SNB, Q187, QS, J1, 2.6, 35M, 2+2.1.30, 3M, BGA	U1000	CRITICAL	CPU_2_6GHZ
337S4029	1	IC, PCH, COUGARPOINT, SLH9D, FRQ, BDB28M65	U1800	CRITICAL	
343S0534	1	IC, BCM5776580, ENET6SD, 8X8	U3900	CRITICAL	
338S0753	1	IC, P9643-E2, 13948 800/OHCI 1.18M/PCI-E, 12	U4100	CRITICAL	
338S0921	1	IC, T29-C0, 220 PCBGA, 15x15MM	U3600	CRITICAL	T29:YES
353S3055	1	IC, P13VED9212, X2 DISPLAYPORT 2/1 MIX, QFN	U9390	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0663	1	IC, FLASH, SERIAL, SPI, 1MBIT, 2V7, EP, 801C	U3990	CRITICAL	ENET_BLANK
341S3026	1	IC, ENET, 11MBIT/FLAN, CIV REV01, K60/K62	U3990	CRITICAL	ENET_PROG
335S0777	1	IC, EEPROM, SERIAL, SPI, 1Kx8, 1.8V, MLP8, LF	U3690	CRITICAL	T29ROM:BLANK
341T0317	1	IC, T29 ASSY	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC, MCU, 32B, LPC1112A, 16KB/2KB, HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC, PROGRAMD, LPC1112A, T29 PORT MCU, HVQFN25	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC, SMC, HSB/2117/9MMx9MM, TLP	U4900	CRITICAL	SMC_BLANK
341T0300	1	IC, SMC, K901	U4900	CRITICAL	SMC_PROG
335S0770	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
335S0769	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341T0299	1	IC, EFI ROM, K901	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	18, ENCORE II, CY7C6303-LQXC	U4800	CRITICAL	
341S3024	1	IC, TP, FSOC, K90, K91, K91F, K92	U5701	CRITICAL	TPAD_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1998	1	K901 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

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PAGE TITLE: BOM Configuration

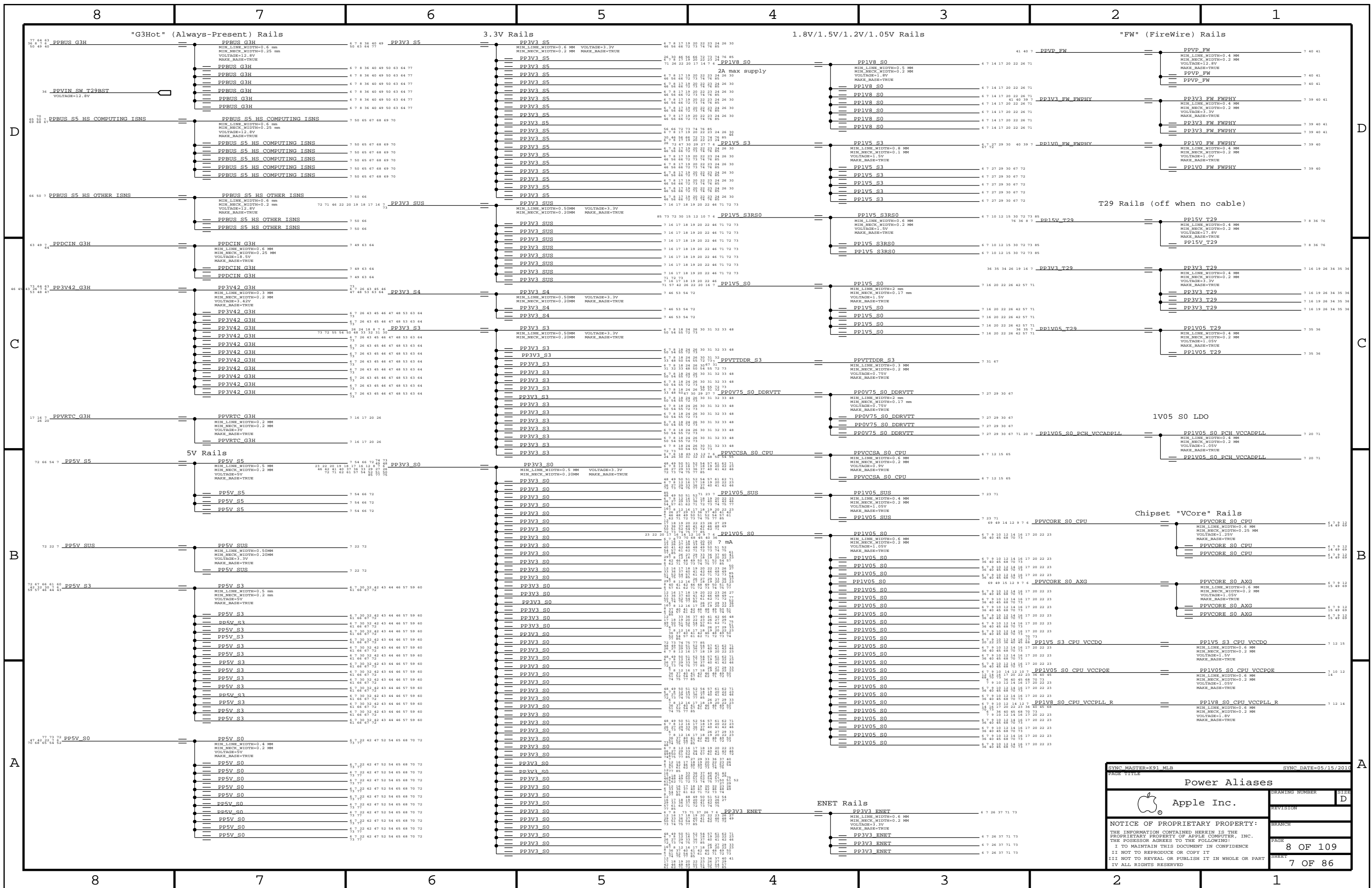
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Functional Test Points

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Fan Connectors TRUE PP5V_S0 TRUE FAN_RT_PWM TRUE FAN_RT_TACH (NEED TO ADD 1 GND TP)		X19 CONN TRUE PP3V3_WLAN (NEED 3 TP) TRUE PCIE_AP_D2R_PI_P TRUE PCIE_AP_D2R_PI_N TRUE PCIE_AP_R2D_P TRUE PCIE_AP_R2D_N TRUE PCIE_CLK100M_AP_CONN_P TRUE PCIE_CLK100M_AP_CONN_N TRUE PP3V3_S3_BT_F TRUE PCIE_WAKE_L TRUE SMBUS_SMC_0_S0_SCL TRUE SMBUS_SMC_0_S0_SDA TRUE USB_BT_P TRUE USB_BT_N TRUE AP_CLKREQ_O_L TRUE AP_RESET_CONN_L TRUE AP_TEMP_SMB_SDA_R TRUE AP_TEMP_SMB_SCL_R TRUE WIFI_EVENT_L_R (NEED TO ADD 5 GND TP)		DEBUG VOLTAGE TRUE PPVCORE_S0_CPU TRUE PPVCORE_S0_AXG TRUE PP1V2_S3_ENET_INTREG TRUE PP1V05_S0 TRUE PP1V5_S3RS0 TRUE PP1V8_S0 TRUE PP3V3_S0 TRUE PP5V_S0 TRUE PP3V3_S3 TRUE PP5V_S3 TRUE PPVCCSA_S0_CPU TRUE PP3V3_S5 TRUE PP3V42_G3H TRUE PPBUS_G3H TRUE PP3V3_ENET TRUE PP3V3_WLAN TRUE PP5V_SW_ODD TRUE PP5V_S0_HDD_FLT TRUE PP18V5_S5 TRUE PP3V3_S0_LCD_F TRUE PP3V3_LCDVDD_SW_F TRUE PP4V5_AUDIO_ANALOG TRUE PPMV5_S3 TRUE SMC_PM_G2_EN TRUE PM_SLP_S4_L TRUE PM_SLP_S3_L (NEED TO ADD 6 GND TP)		DC POWER CONN (NEED 3 TP) TRUE PP18V5_DCIN_FUSE TRUE ADAPTER_SENSE (NEED TO ADD 4 GND TP)		NC NO_TESTS NC CRT IG BLUE NC CRT IG GREEN NC CRT IG RED NC CRT IG DDC CLK NC CRT IG DDC DATA NC CRT IG HSYNC NC CRT IG VSYNC NC LVDS IG_CTRL_CLK NC LVDS IG_CTRL_DATA NC PCH LVDS_VBG NC HDA_SDN1 NC HDA_SDN2 NC HDA_SDN3 NC PCI_PME_L NC PCI_CLK33M_OUT3 NC CLINK_CLK NC CLINK_DATA NC CLINK_RESET_L NC PCIE_CLK100M_PEBN NC PCIE_CLK100M_PEBP NC FW643_SDA NC FW643_SM NC FW643_TCK NC FW643_TMS NC FW643_FW620_L NC FW643_VBUF NC FW643_OCR10_CTL NC FW643_AVREG NC FW643_TDI TP_XDP_PCH_OBSFN_A<0..1> TP_XDP_PCH_OBSFN_B<0..1> NC_TP_XDPPCH_HOOK2 NC_TP_XDPPCH_HOOK3 TP_XDP_PCH_OBSFN_D<0..1> NC_TP_XDP_PCH_HOOK4 NC_TP_XDP_PCH_HOOK5 NC_PCH_GPIO64_CLKOUTFLEX0 NC_PCH_GPIO65_CLKOUTFLEX1 NC_PCH_GPIO66_CLKOUTFLEX2 NC_PCH_GPIO67_CLKOUTFLEX3 NC FW2_TBPB NC FW2_TBBN NC FW2_TBIAS NC FW2_TPAP NC FW2_TPAN NC FW0_TBPB NC FW0_TBBN NC FW0_TPAP XDP_PCH_AP_PWR_EN XDP_PCH_USB_HUB_SOFT_RST_L XDP_PCH_SDCONN_STATE_RST_L XDP_PCH_ENET_PWR_EN XDP_PCH_SDCONN_DET_L XDP_PCH_S5_PWRGD XDP_PCH_PWRBTN_L XDP_PCH_ISOLATE_CPU_MEM_L XDP_FW_CLKREQ_L XDP_AP_CLKREQ_L XDP_PCH_AUD_IPHS_SWITCH_EN NC_SDVO_TVCLKINN NC_SDVO_TVCLKINP NC_SDVO_STALLN NC_SDVO_STALLP NC_SDVO_INTN NC_SDVO_INTP		NC NO_TESTS TP EDP_TX_P<0..3> TP EDP_TX_N<0..3> NC_EDP_AUXP NC_EDP_AUXN NC_CPU_THERMDA NC_CPU_THERMDC NC_CPU_RSVD<30..45> NC_CPU_RSVD<8..27> =PEG_R2D_C_P<0..7> =PEG_R2D_C_N<0..7> =PEG_D2R_P<0..7> =PEG_D2R_N<0..7> =PEG_R2D_C_P<12..15> =PEG_R2D_C_N<12..15> =PEG_D2R_P<12..15> =PEG_D2R_N<12..15> NC_PCIE_CLK100M_PEA4 NC_PCIE_CLK100M_PEA6 NC_PCIE_CLK100M_PEA8 NC_PCIE_CLK100M_PEB4 NC_PCIE_CLK100M_PEB6 NC_PCIE_CLK100M_PEB8 NC_PCIE_CLK100M_PEN4 NC_PCIE_CLK100M_PEN6 NC_PCIE_CLK100M_PEN8 NC_PCIE_CLK100M_PEP4 NC_PCIE_CLK100M_PEP6 NC_PCIE_CLK100M_PEP8 NC_PSOC_P1_3 NC_SATA_B_D2RN NC_SATA_B_D2RP NC_SATA_B_R2D_CN NC_SATA_B_R2D_CP NC_SATA_D_D2RN NC_SATA_D_D2RP NC_SATA_D_R2D_CN NC_SATA_D_R2D_CP NC_SATA_E_D2RN NC_SATA_E_D2RP NC_SATA_E_R2D_CN NC_SATA_E_R2D_CP NC_SATA_F_D2RN NC_SATA_F_D2RP NC_SATA_F_R2D_CN NC_SATA_F_R2D_CP NC_PCH_TP18 NC_PCH_TP17 NC_PCH_TP16 NC_PCH_TP15 NC_PCH_TP14 NC_PCH_TP13 NC_PCH_TP12 NC_PCH_TP10 NC_PCH_TP9 NC_PCH_TP8 NC_PCH_TP7 NC_PCH_TP6 NC_PCH_TP5 NC_PCH_TP4 NC_PCH_TP3 NC_PCH_TP2 NC_PCH_TP1 PCH_VSS_NCTF<1> PCH_VSS_NCTF<2> PCH_VSS_NCTF<5> PCH_VSS_NCTF<9> PCH_VSS_NCTF<11> PCH_VSS_NCTF<12> TP_LVDS_IG_B_CLKN TP_LVDS_IG_B_CLKP NC_LVDS_IG_BKL_PWM NC_SMC_BS_ALERT_L		SPEAKER FUNC_TEST TRUE SPKRAMP_L_N_OUT TRUE SPKRAMP_L_P_OUT TRUE SPKRAMP_R_N_OUT TRUE SPKRAMP_R_P_OUT TRUE SPKRAMP_SUB_N_OUT TRUE SPKRAMP_SUB_P_OUT		IPD_FLEX_CONN TRUE PP3V3_S5 TRUE PP18V5_S5 TRUE Z2_CS_L TRUE Z2_DEBUG3 TRUE Z2_MOSI TRUE Z2_MISO TRUE Z2_SCLK TRUE Z2_BOOST_EN TRUE Z2_HOST_INTN TRUE Z2_CLKIN TRUE Z2_KEY_ACT_L TRUE Z2_RESET TRUE PSOC_MISO TRUE PSOC_MOSI TRUE PSOC_SCLK TRUE SMBUS_SMC_A_S3_SDA TRUE SMBUS_SMC_A_S3_SCL TRUE PSOC_F_CS_L TRUE PICKB_L (NEED TO ADD 2 GND TP)		KEYBOARD CONN TRUE PP3V3_S5 TRUE PP3V42_G3H TRUE WS_KBD1 TRUE WS_KBD2 TRUE WS_KBD3 TRUE WS_KBD4 TRUE WS_KBD5 TRUE WS_KBD6 TRUE WS_KBD7 TRUE WS_KBD8 TRUE WS_KBD9 TRUE WS_KBD10 TRUE WS_KBD11 TRUE WS_KBD12 TRUE WS_KBD13 TRUE WS_KBD14 TRUE WS_KBD15_CAP TRUE WS_KBD16_NUM TRUE WS_KBD17 TRUE WS_KBD18 TRUE WS_KBD19 TRUE WS_KBD20 TRUE WS_KBD21 TRUE WS_KBD22 TRUE WS_KBD23 TRUE WS_KBD_ONOFF_L TRUE WS_LEFT_SHIFT_KBD TRUE WS_LEFT_OPTION_KBD TRUE WS_CONTROL_KBD (NEED TO ADD 2 GND TP)		LPC+SPI DEBUG_CONN TRUE LEC_AD<0> TRUE LEC_AD<1> TRUE LEC_AD<2> TRUE LEC_AD<3> TRUE LPC_CLK33M_LPCPLUS TRUE LPC_FRAME_L TRUE LPC_PWRDWN_L TRUE LPC_SERIRO TRUE LPCPLUS_GPIO TRUE LPCPLUS_RESET_L TRUE PM_CLKRUN_L TRUE PP3V42_G3H TRUE PP5V_S0 TRUE SMC_MD1 TRUE SMC_RX_L TRUE SMC_TCK TRUE SMC_TDI TRUE SMC_TDO TRUE SMC_TMS TRUE SMC_TRST_L TRUE SMC_TX_L TRUE SPI_ALT_CLK TRUE SPI_ALT_CS_L TRUE SPI_ALT_MISO TRUE SPI_ALT_MOSI TRUE SPIROM_USE_MLB (NEED TO ADD 2 GND TP)		DC POWER CONN (NEED 3 TP) TRUE PP18V5_DCIN_FUSE TRUE ADAPTER_SENSE (NEED TO ADD 4 GND TP)		NC NO_TESTS NC FW2_TBPB NC FW2_TBBN NC FW2_TBIAS NC FW2_TPAP NC FW2_TPAN NC FW0_TBPB NC FW0_TBBN NC FW0_TPAP XDP_PCH_AP_PWR_EN XDP_PCH_USB_HUB_SOFT_RST_L XDP_PCH_SDCONN_STATE_RST_L XDP_PCH_ENET_PWR_EN XDP_PCH_SDCONN_DET_L XDP_PCH_S5_PWRGD XDP_PCH_PWRBTN_L XDP_PCH_ISOLATE_CPU_MEM_L XDP_FW_CLKREQ_L XDP_AP_CLKREQ_L XDP_PCH_AUD_IPHS_SWITCH_EN NC_SDVO_TVCLKINN NC_SDVO_TVCLKINP NC_SDVO_STALLN NC_SDVO_STALLP NC_SDVO_INTN NC_SDVO_INTP		NC NO_TESTS TP EDP_TX_P<0..3> TP EDP_TX_N<0..3> NC_EDP_AUXP NC_EDP_AUXN NC_CPU_THERMDA NC_CPU_THERMDC NC_CPU_RSVD<30..45> NC_CPU_RSVD<8..27> =PEG_R2D_C_P<0..7> =PEG_R2D_C_N<0..7> =PEG_D2R_P<0..7> =PEG_D2R_N<0..7> =PEG_R2D_C_P<12..15> =PEG_R2D_C_N<12..15> =PEG_D2R_P<12..15> =PEG_D2R_N<12..15> NC_PCIE_CLK100M_PEA4 NC_PCIE_CLK100M_PEA6 NC_PCIE_CLK100M_PEA8 NC_PCIE_CLK100M_PEB4 NC_PCIE_CLK100M_PEB6 NC_PCIE_CLK100M_PEB8 NC_PCIE_CLK100M_PEN4 NC_PCIE_CLK100M_PEN6 NC_PCIE_CLK100M_PEN8 NC_PCIE_CLK100M_PEP4 NC_PCIE_CLK100M_PEP6 NC_PCIE_CLK100M_PEP8 NC_PSOC_P1_3 NC_SATA_B_D2RN NC_SATA_B_D2RP NC_SATA_B_R2D_CN NC_SATA_B_R2D_CP NC_SATA_D_D2RN NC_SATA_D_D2RP NC_SATA_D_R2D_CN NC_SATA_D_R2D_CP NC_SATA_E_D2RN NC_SATA_E_D2RP NC_SATA_E_R2D_CN NC_SATA_E_R2D_CP NC_SATA_F_D2RN NC_SATA_F_D2RP NC_SATA_F_R2D_CN NC_SATA_F_R2D_CP NC_PCH_TP18 NC_PCH_TP17 NC_PCH_TP16 NC_PCH_TP15 NC_PCH_TP14 NC_PCH_TP13 NC_PCH_TP12 NC_PCH_TP10 NC_PCH_TP9 NC_PCH_TP8 NC_PCH_TP7 NC_PCH_TP6 NC_PCH_TP5 NC_PCH_TP4 NC_PCH_TP3 NC_PCH_TP2 NC_PCH_TP1 PCH_VSS_NCTF<1> PCH_VSS_NCTF<2> PCH_VSS_NCTF<5> PCH_VSS_NCTF<9> PCH_VSS_NCTF<11> PCH_VSS_NCTF<12> TP_LVDS_IG_B_CLKN TP_LVDS_IG_B_CLKP NC_LVDS_IG_BKL_PWM NC_SMC_BS_ALERT_L	
BATT POWER CONN TRUE SMBUS_SMC_BSA_SCL TRUE SMBUS_SMC_BSA_SDA TRUE SYS_DETECT_L TRUE PPVBT_G3H_CONN (NEED 5 TP) (NEED TO ADD 5 GND TP)		KBD BACKLIGHT CONN TRUE KBDLED_ANODE TRUE SMC_KBDLED_PRESENT_L (NEED TO ADD 1 GND TP)		CAMERA/ALS CONN TRUE PP5V_S3_ALSCAMERA_F TRUE SMBUS_SMC_A_S3_SCL TRUE SMBUS_SMC_A_S3_SDA TRUE USB_CAMERA_CONN_P TRUE USB_CAMERA_CONN_N (NEED TO ADD 2 GND TP)		FUNC TEST DRAWING NUMBER: D REVISION: BRANCH: PAGE: 7 OF 109 SHEET: 6 OF 86																			



SYNC MASTER=K91 MLB SYNC DATE=05/15/2011

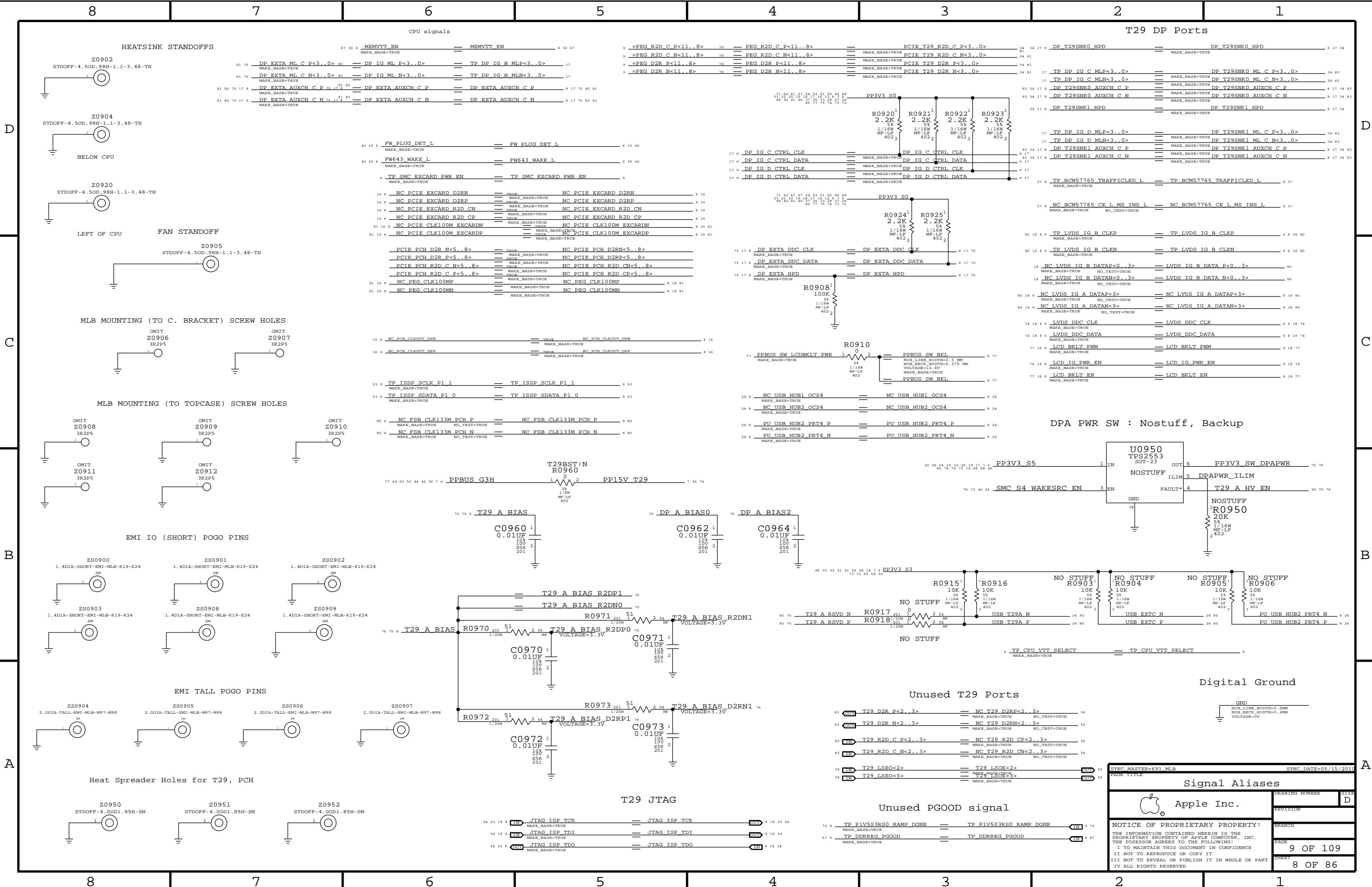
PAGE TITLE

Power Aliases

Apple Inc.

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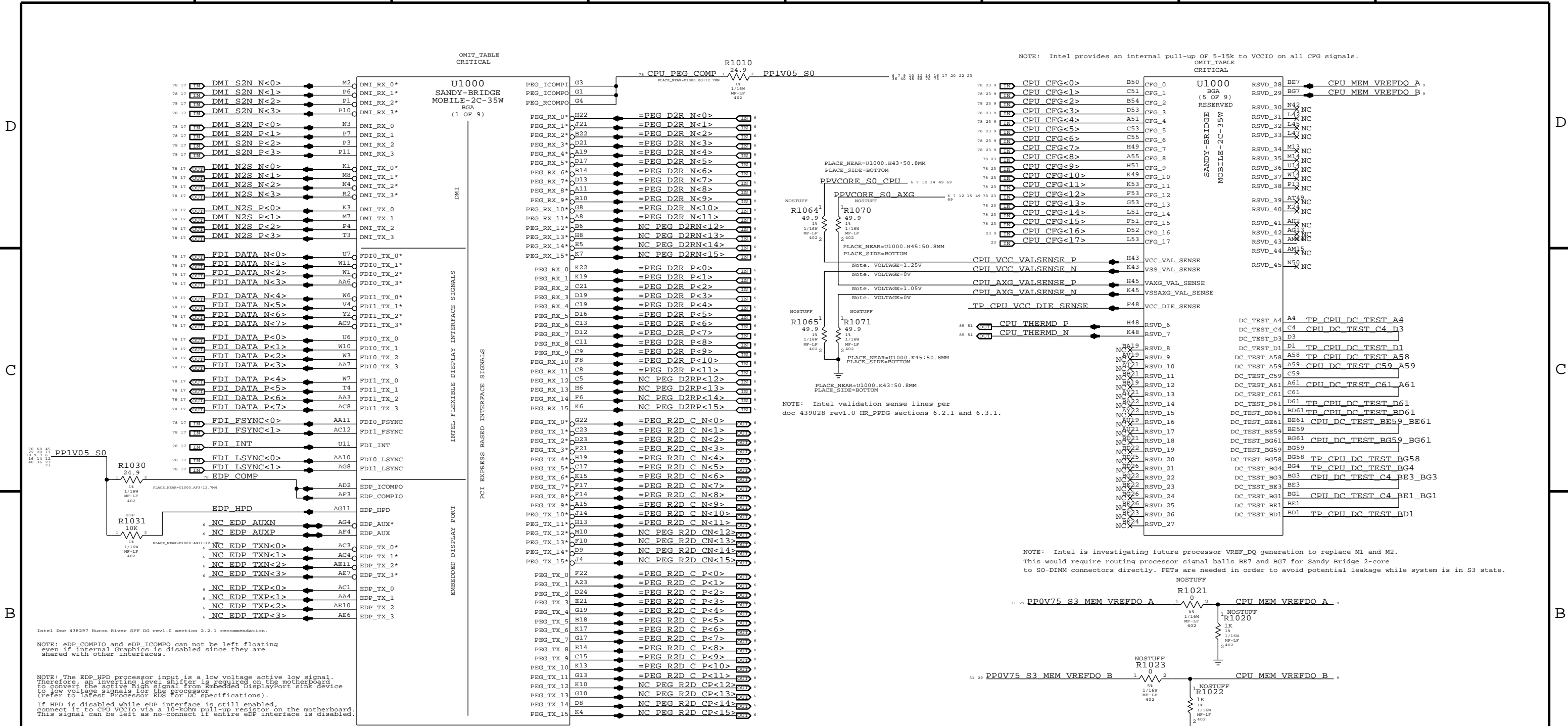
REVISION: **9 OF 109**

SHEET: **8 OF 86**

DATE: 05/15/2011

SYNC MASTER: K91.MLB

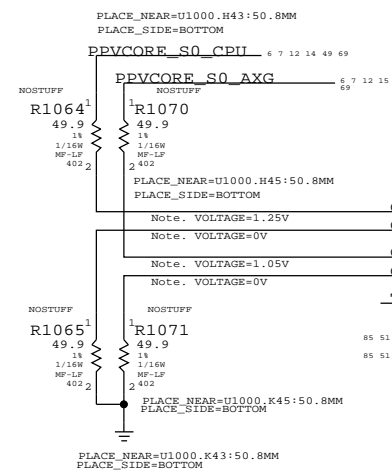
PAGE TITLE: Signal Aliases



NOTE: Intel provides an internal pull-up of 5-15k to VCCIO on all CFG signals.

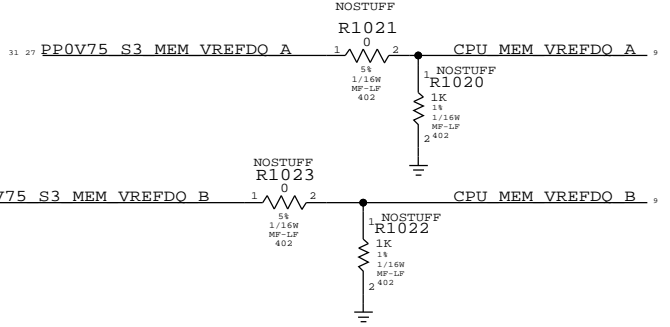
OMIT_TABLE CRITICAL

OMIT_TABLE CRITICAL



NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

NOTE: Intel is investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal halls BE7 and BG7 for Sandy Bridge 2-core to SO-DIMM connectors directly. FETs are needed in order to avoid potential leakage while system is in S3 state.

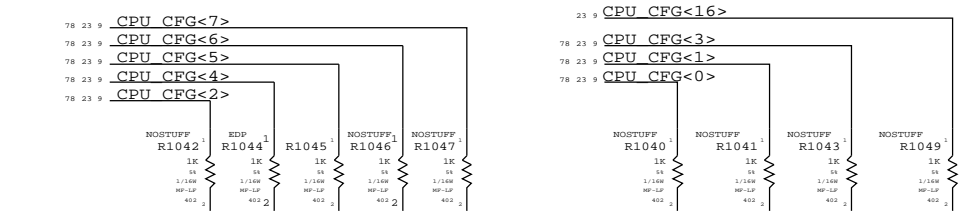


Intel Doc 438297 Huron River SFF DG rev1.0 section 2.2.1 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor. (refer to latest Processor for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.



FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING 1 = (DEFAULT) IMMEDIATELY AFTER xRESETB 0 = WAIT FOR BIOS

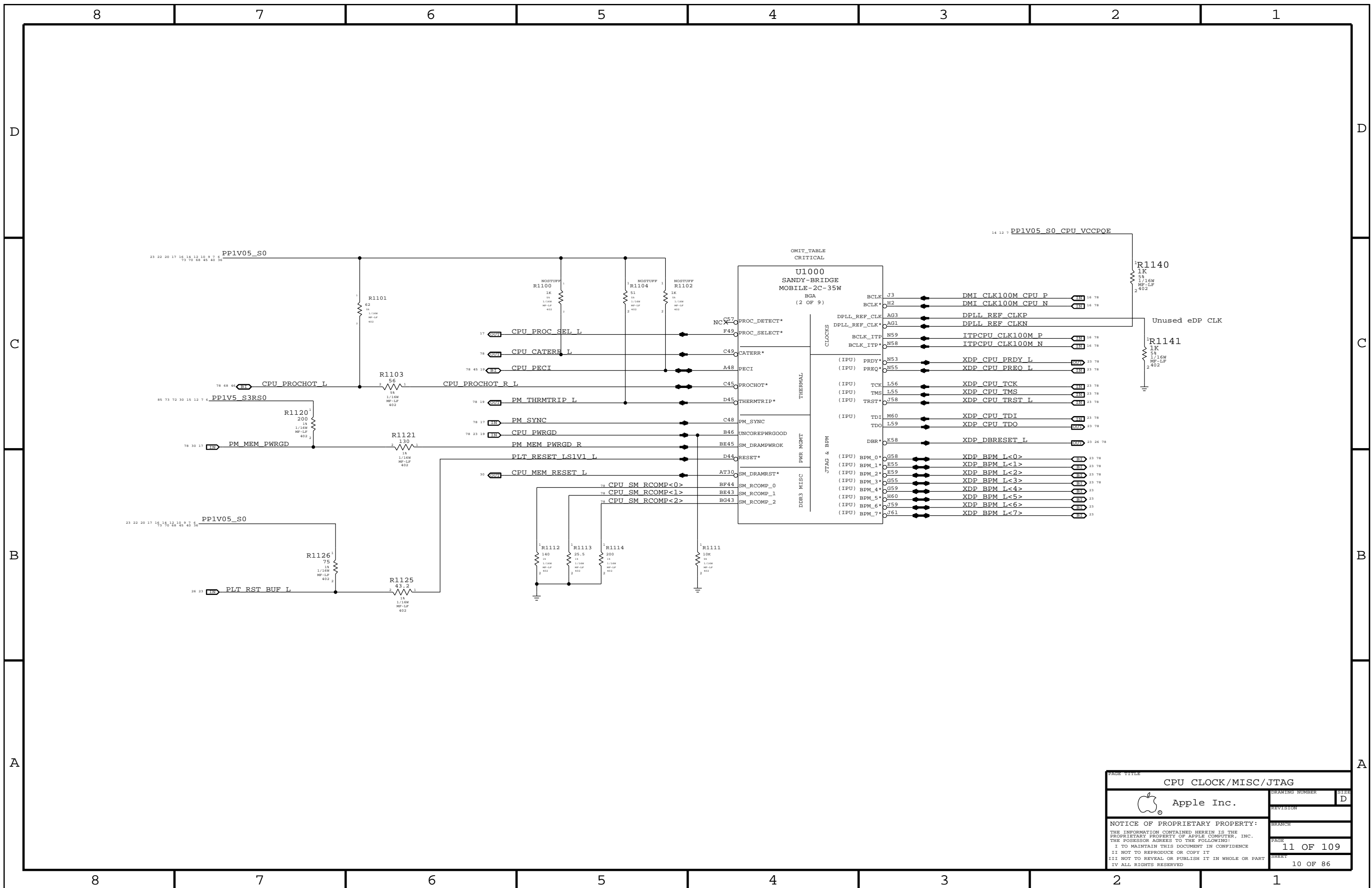
CFG [6:5] :PCIE BIFURCATION 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4

CFG [4] :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED

CFG [3] :PCIE x4 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

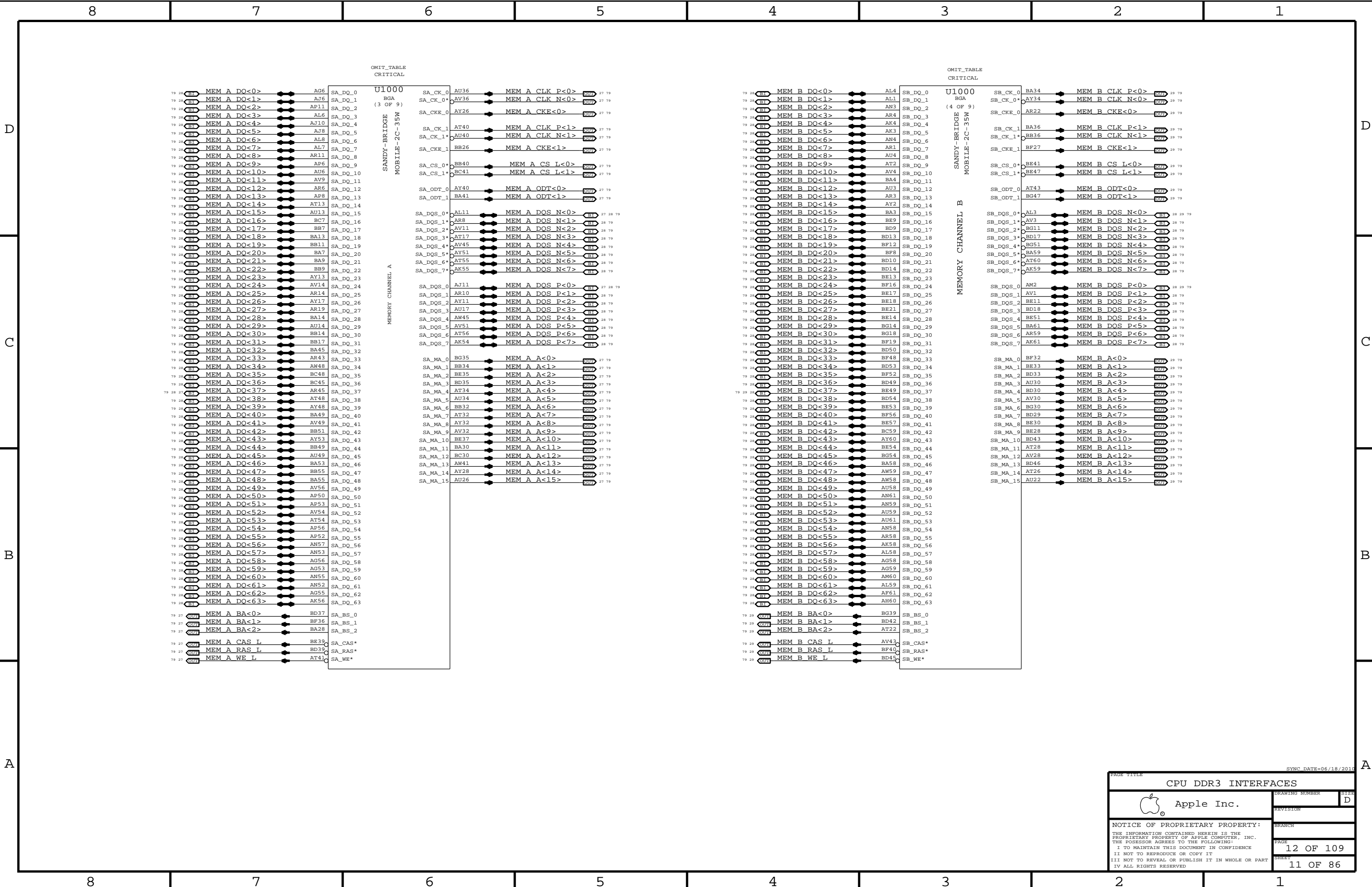
CFG [2] :PCIE x16 LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

CPU DMI/PEG/FDI/RSVD		DRAWING NUMBER	SIZE
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OMIT_TABLE
CRITICAL

OMIT_TABLE
CRITICAL

U1000
BGA
(3 OF 9)

U1000
BGA
(4 OF 9)

SANDY-BRIDGE
MOBILE-2C-35W

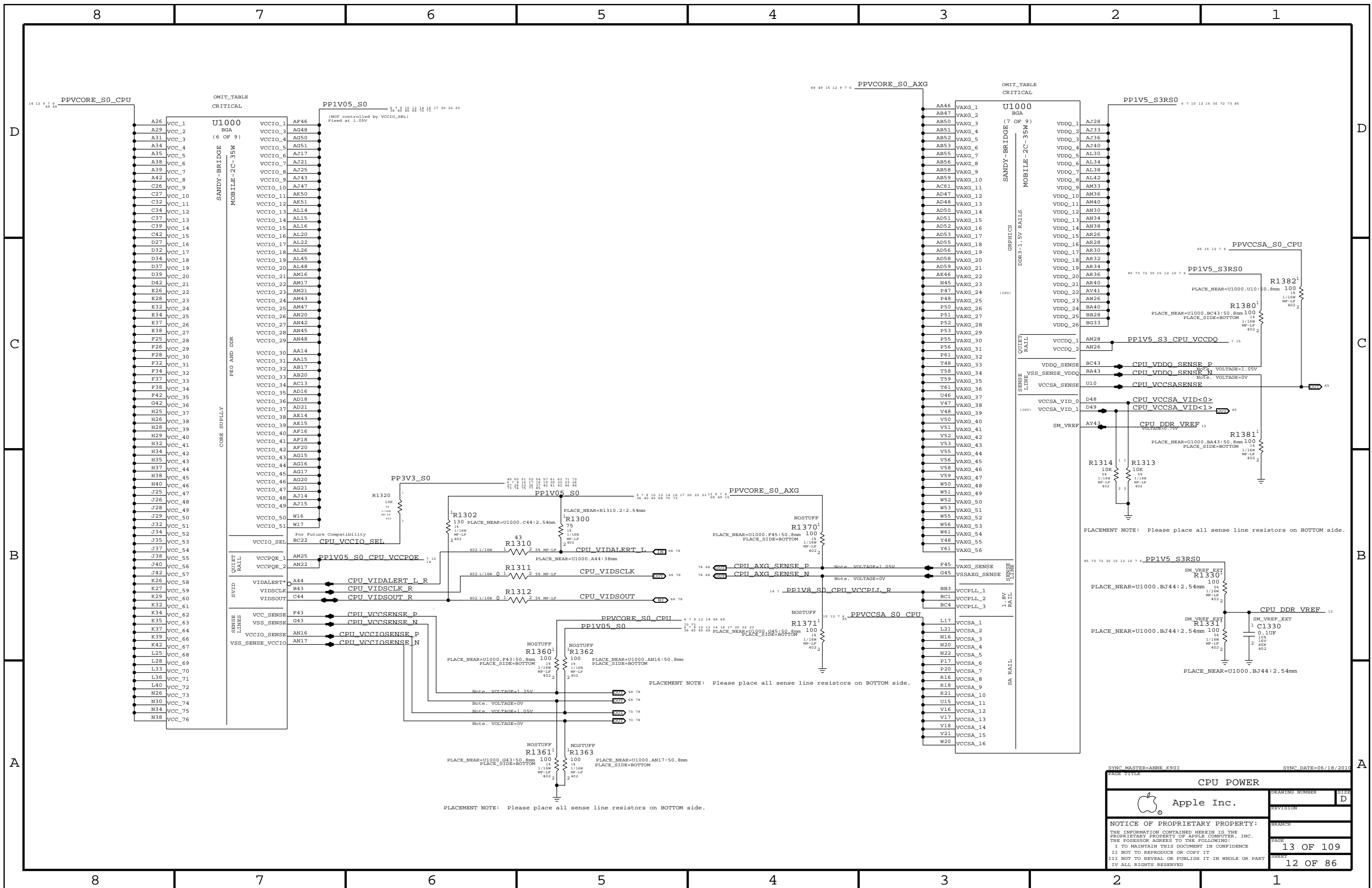
SANDY-BRIDGE
MOBILE-2C-35W

MEMORY CHANNEL A

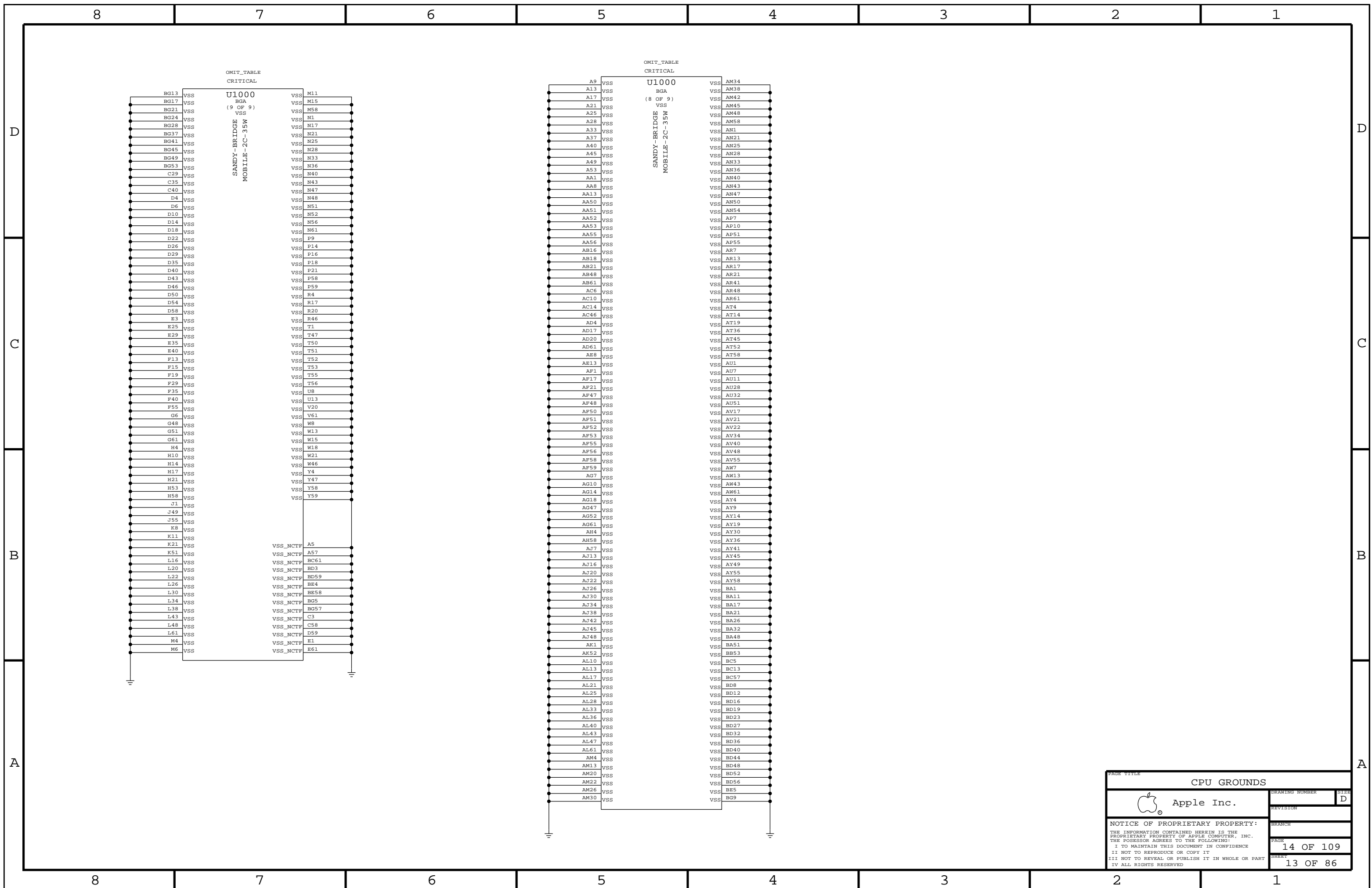
MEMORY CHANNEL B

SYNC DATE=06/18/2011

CPU DDR3 INTERFACES		DRAWING NUMBER	SIZE
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		SHEET	11 OF 86



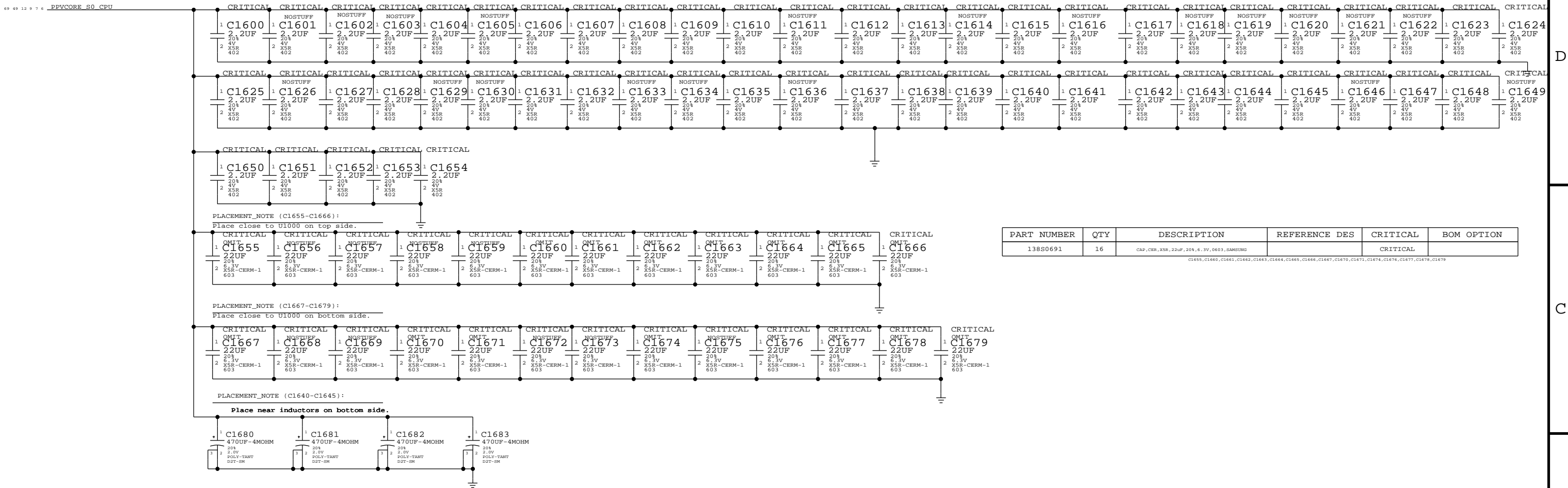
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CPU GROUNDS		DRAWING NUMBER	SIZE
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CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

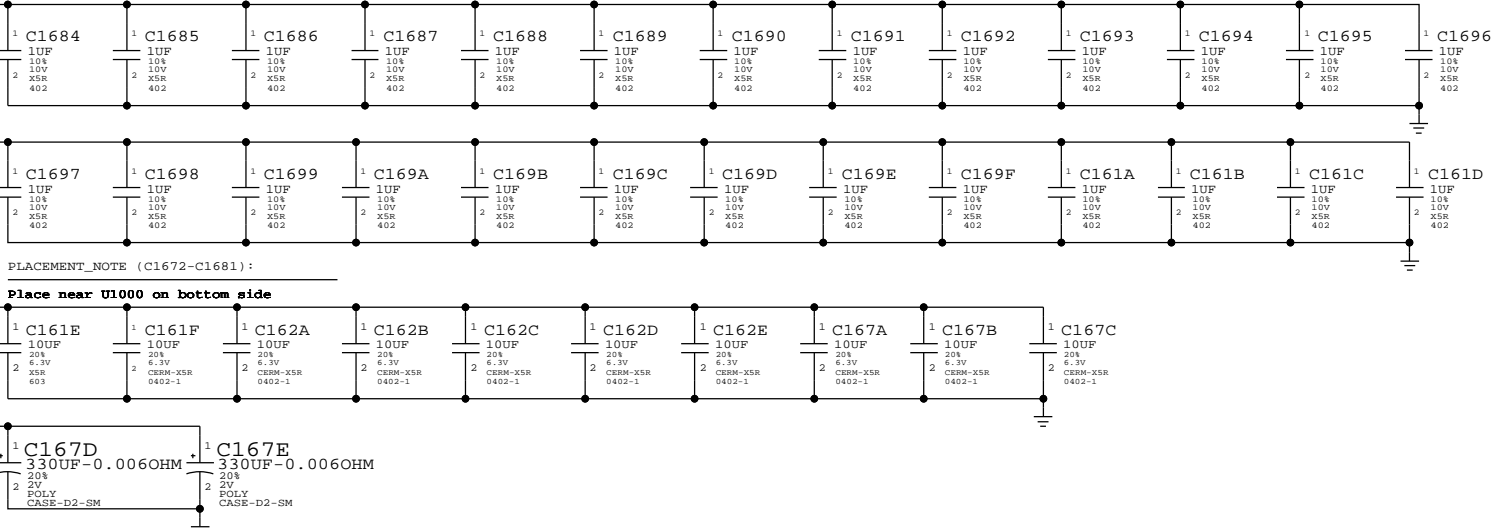


CPU VCCIO/VCCPQ DECOUPLING

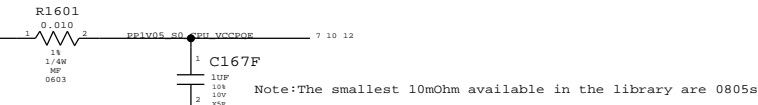
Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

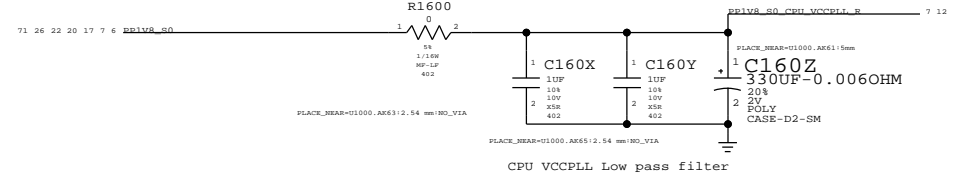


CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side



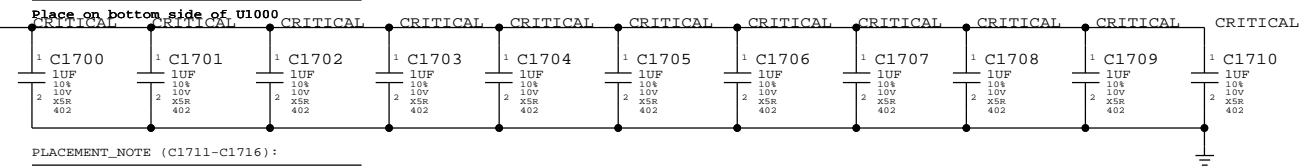
SYNC MASTER=JACK K901		SYNC DATE=06/28/2016	
CPU DECOUPLING-I			
Apple Inc.		DRAWING NUMBER	SIZE
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VAXG DECOUPLING

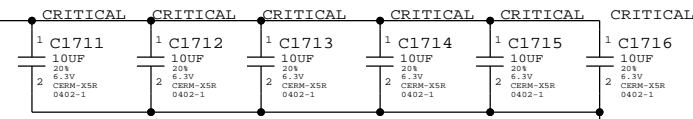
Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

PLACEMENT_NOTE (C1700-C1710):

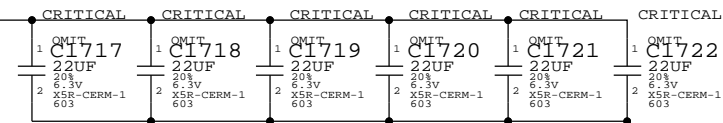
Place on bottom side of U1000



PLACEMENT_NOTE (C1711-C1716):

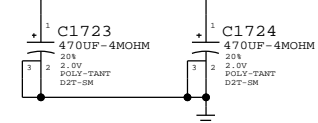


PLACEMENT_NOTE (C1717-C1722):



PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.



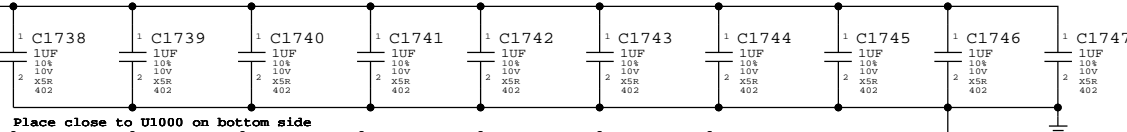
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP, CER, XSR, 22UF, 20V, 6.3V, 0603, SAMSUNG	C1717, C1718, C1719, C1720, C1721, C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

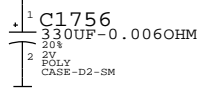
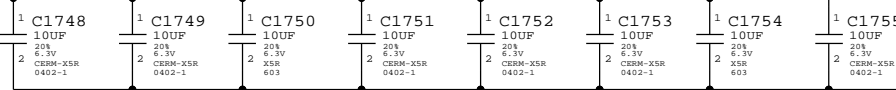
Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

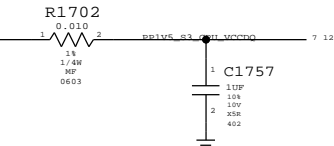
Place on bottom side of U1000



Place close to U1000 on bottom side



Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

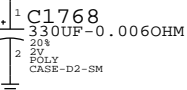
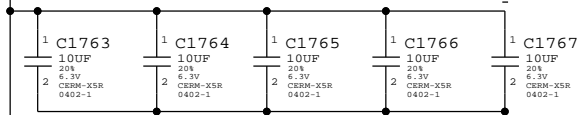
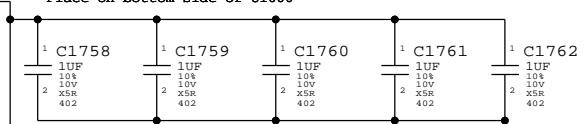


CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uF, 5x 10uF, 1x 330uF

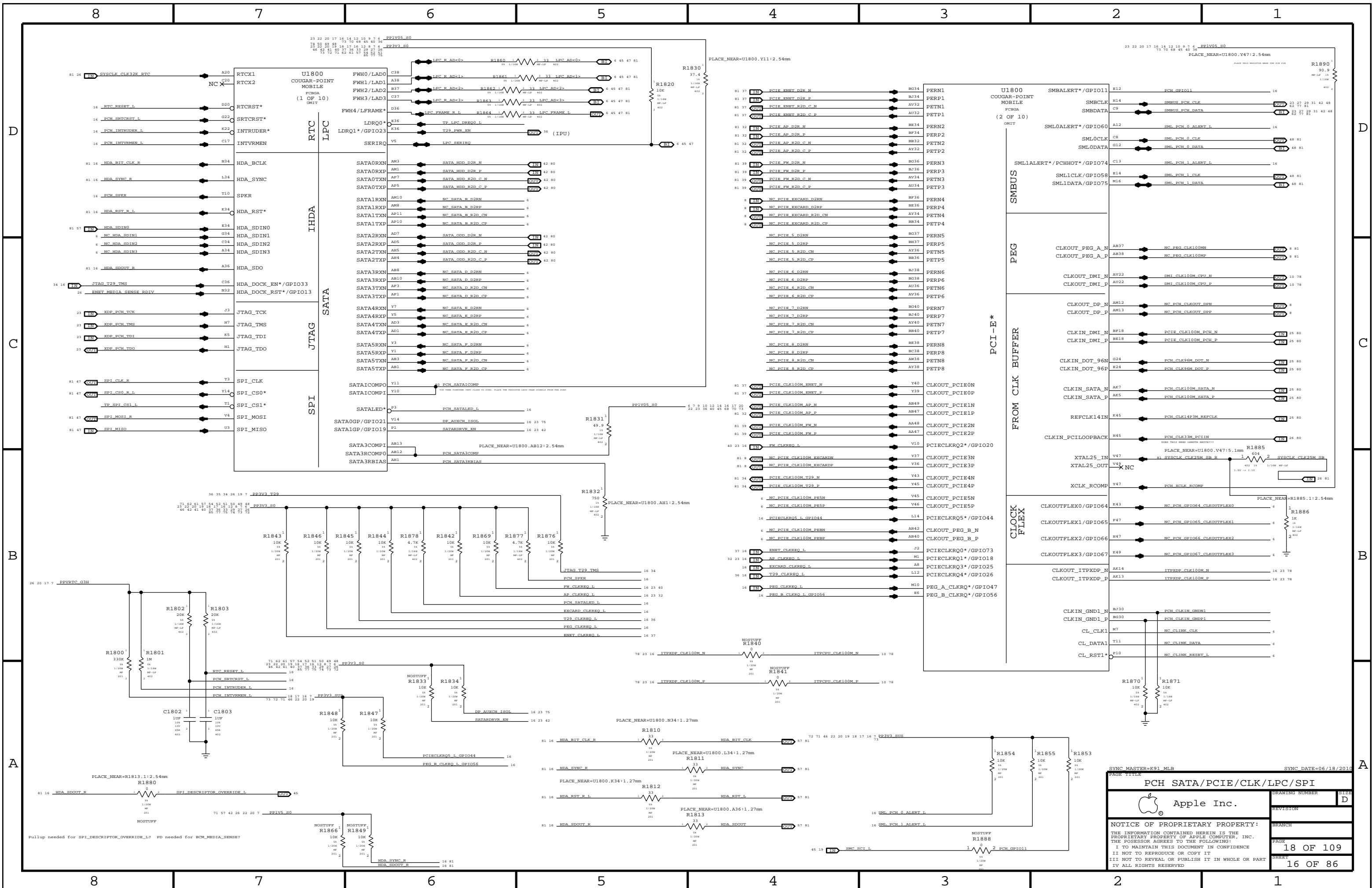
PLACEMENT_NOTE (C1758-C1762):

Place on bottom side of U1000



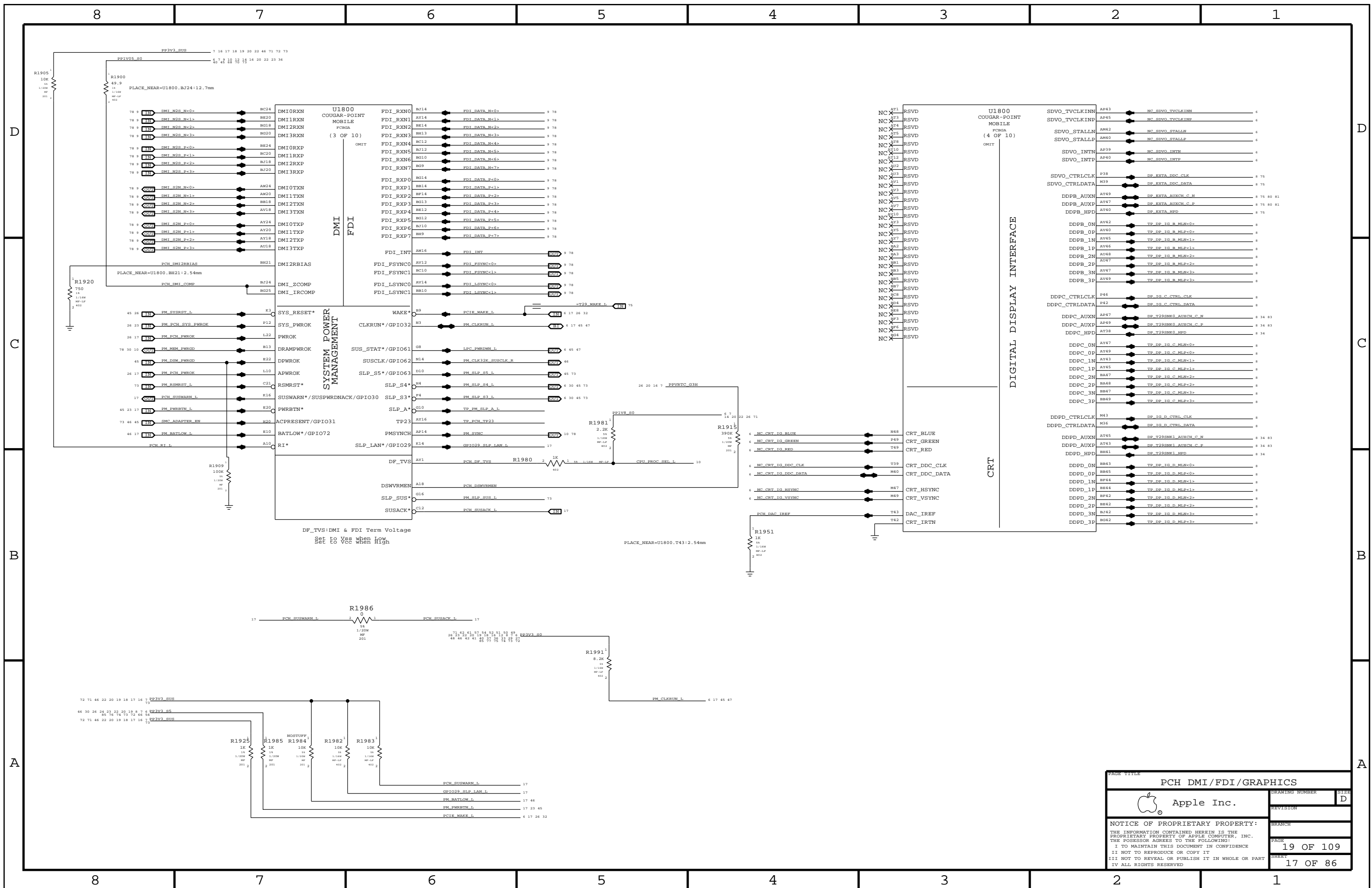
SYNC MASTER=JACK_K90I SYNC DATE=06/28/2010

CPU DECOUPLING-II		DRAWING NUMBER	SIZE
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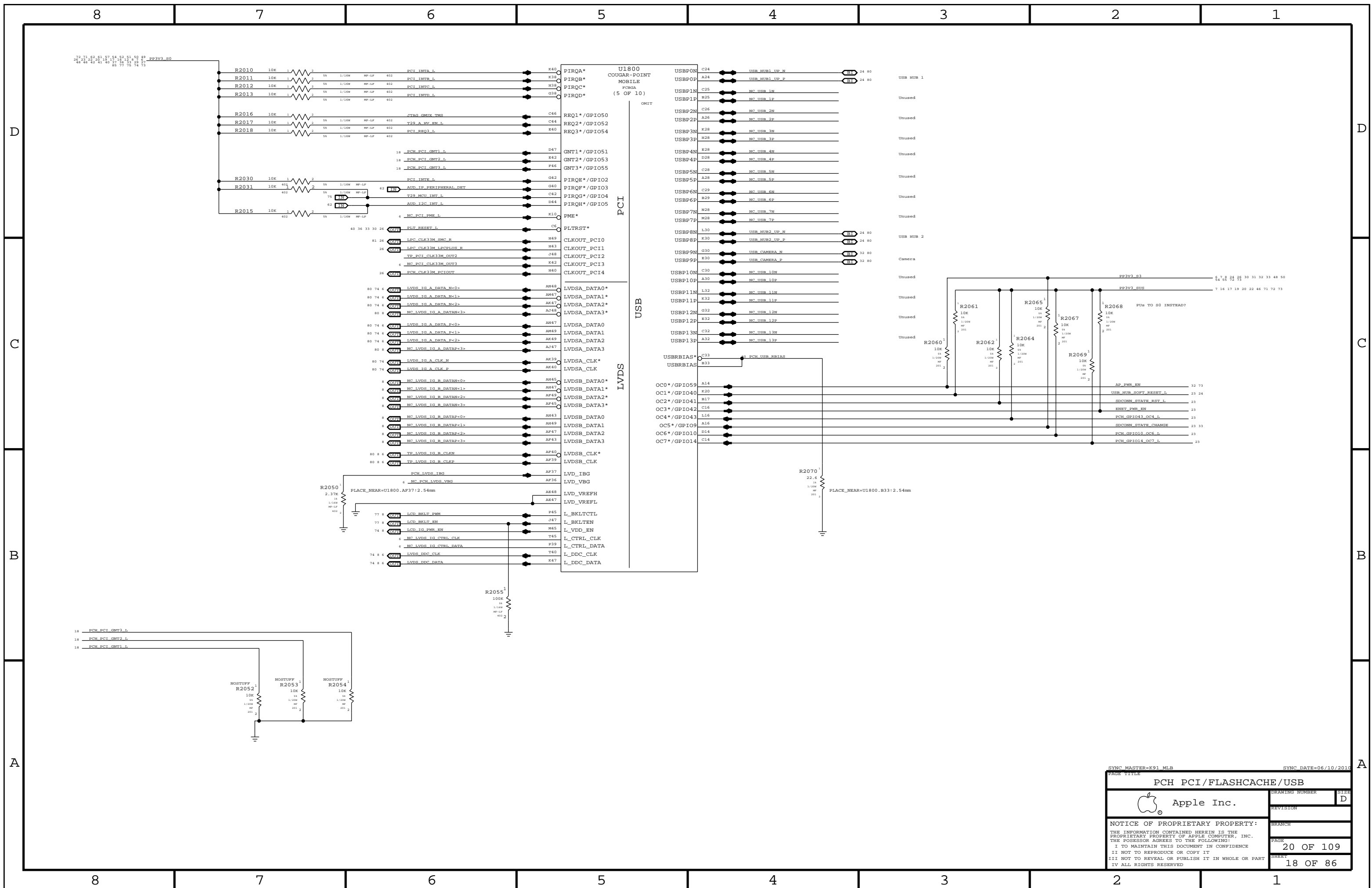


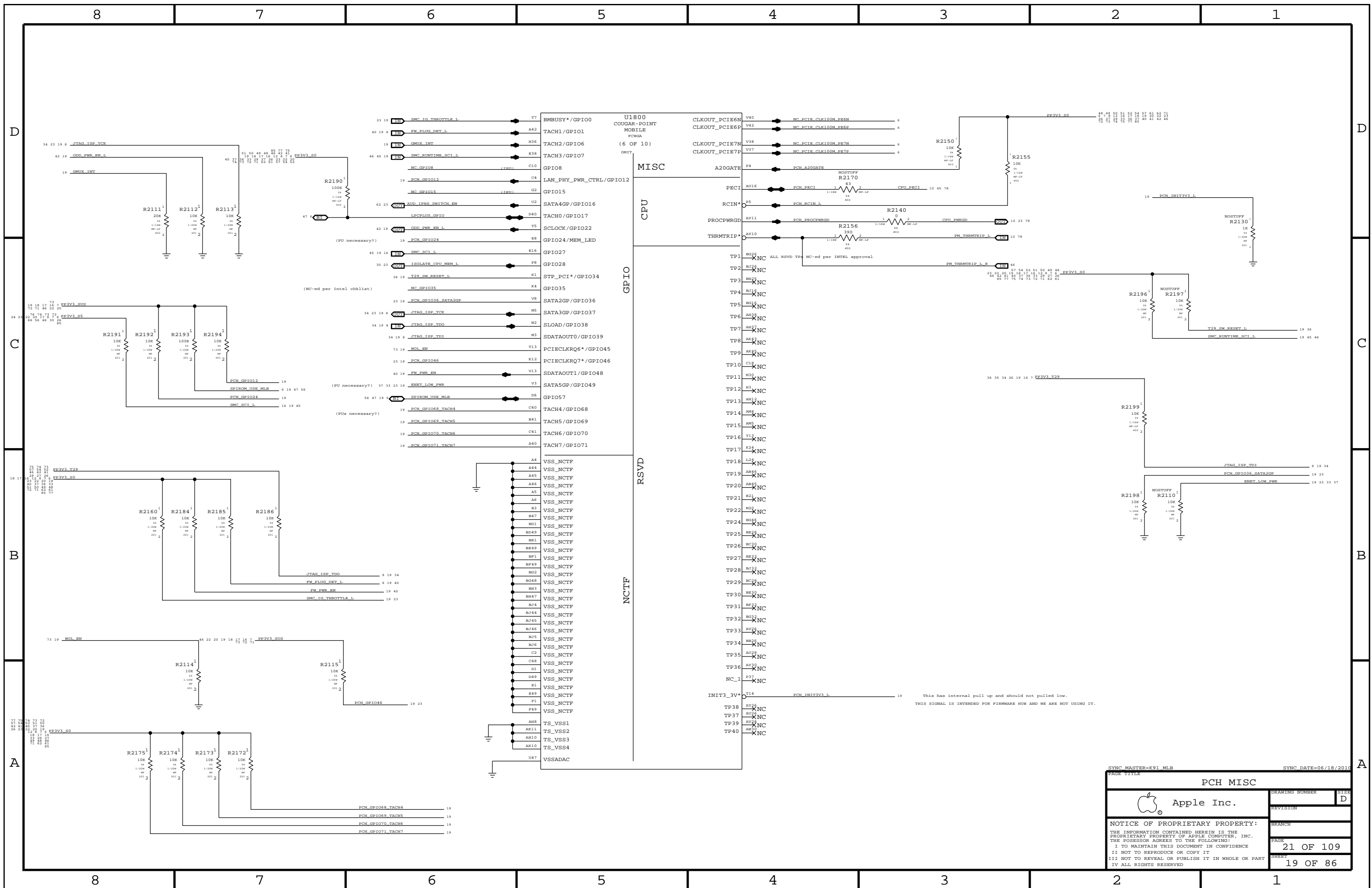
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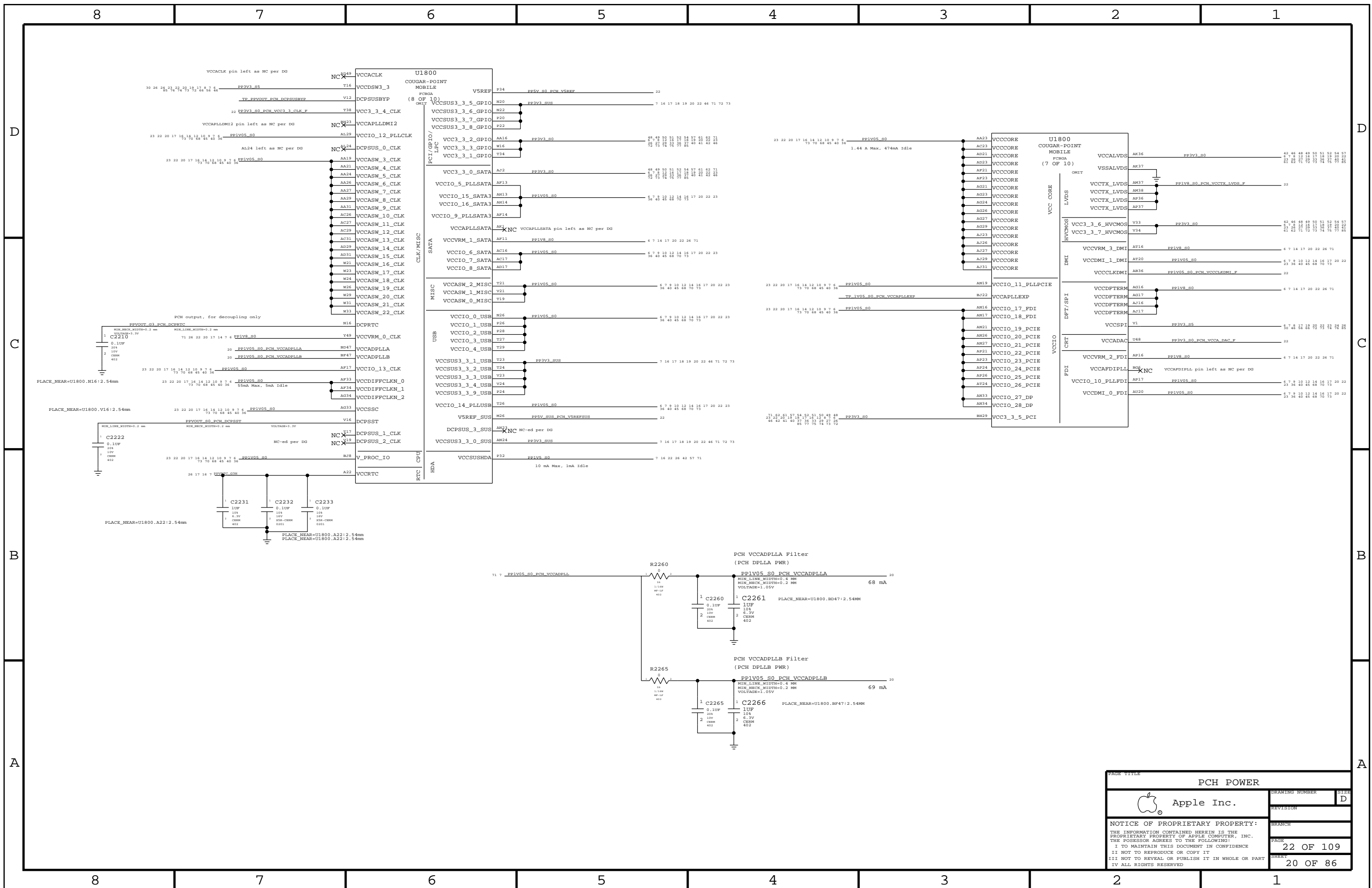


PCH DMI/FDI/GRAPHICS		DRAWING NUMBER	SIZE
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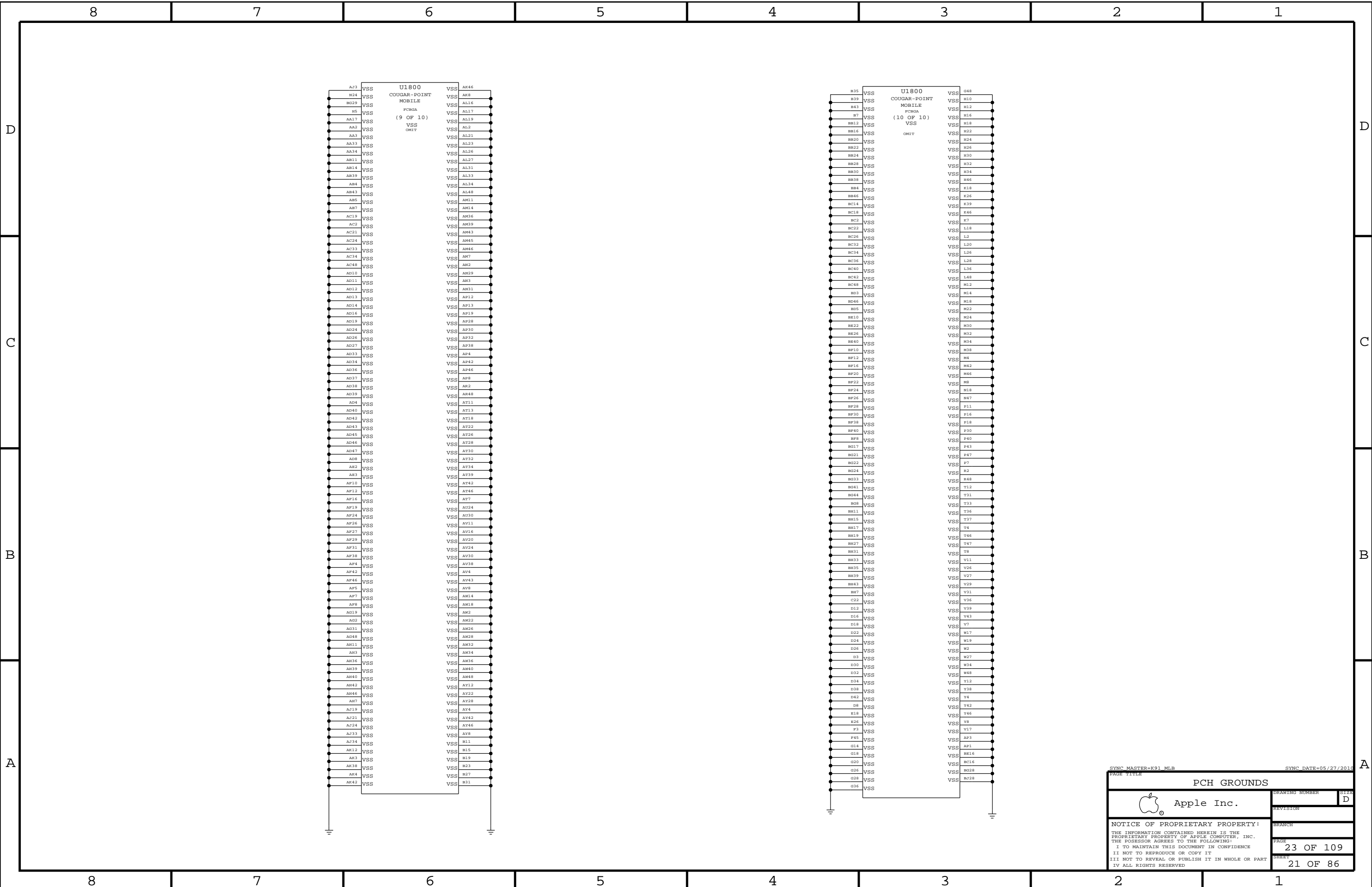




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PCH MISC
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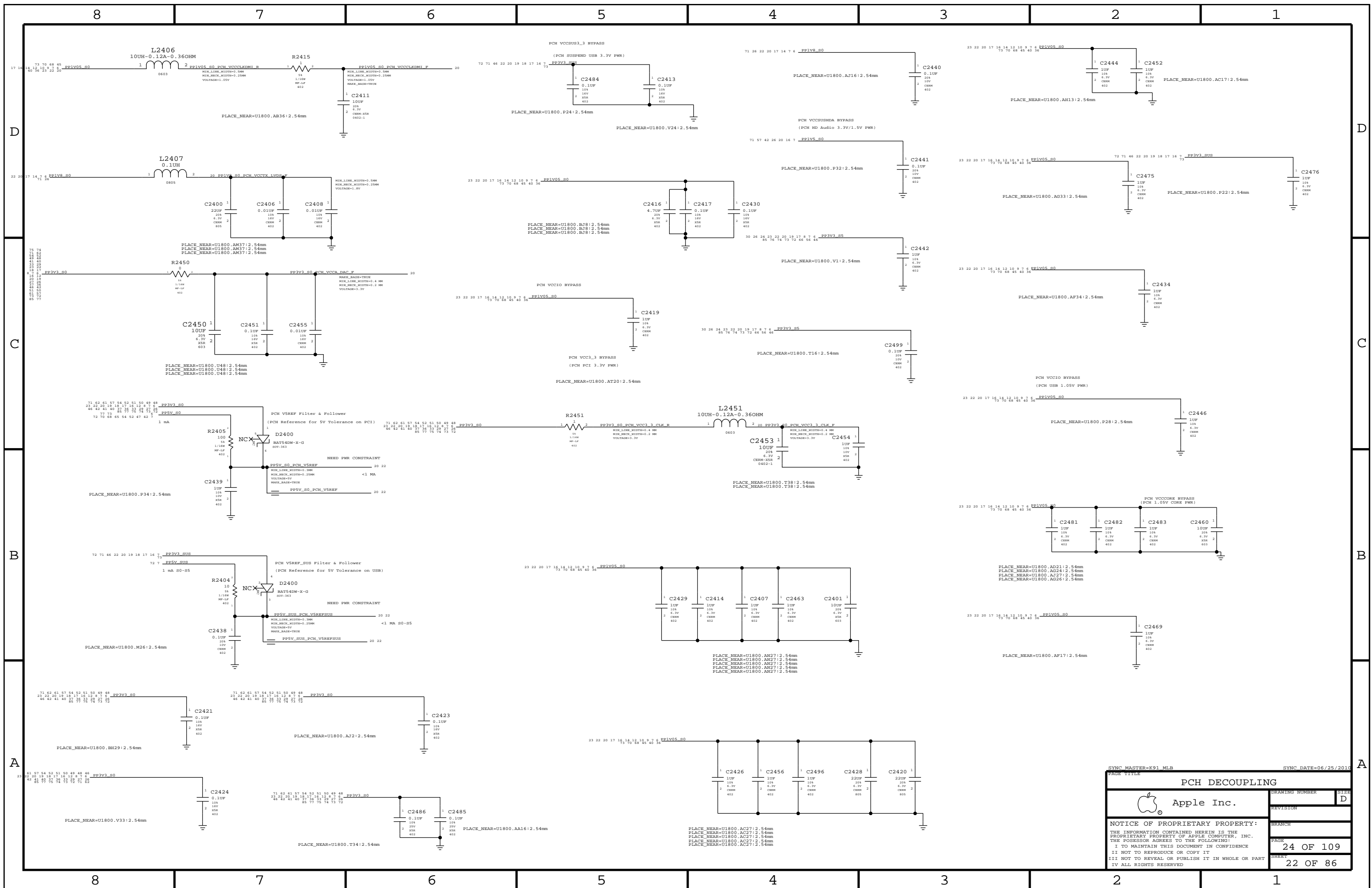
SYNC MASTER=K91 MLB SYNC DATE=05/27/2010

PAGE TITLE: PCH GROUNDS


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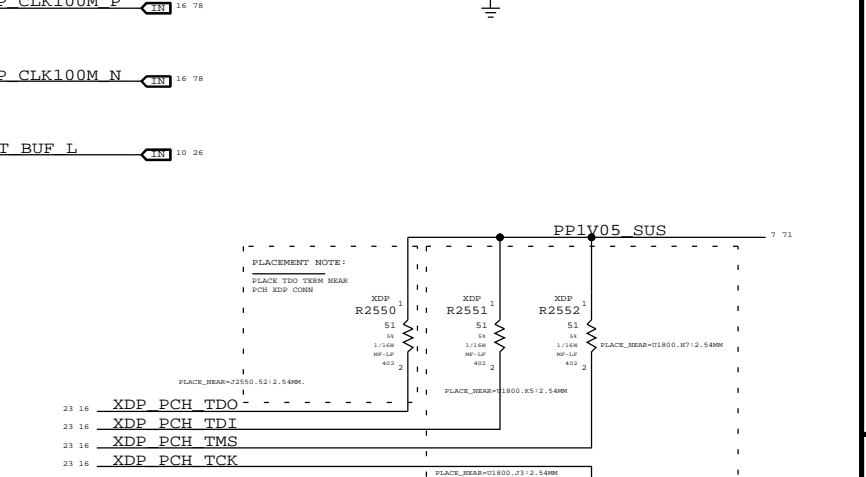
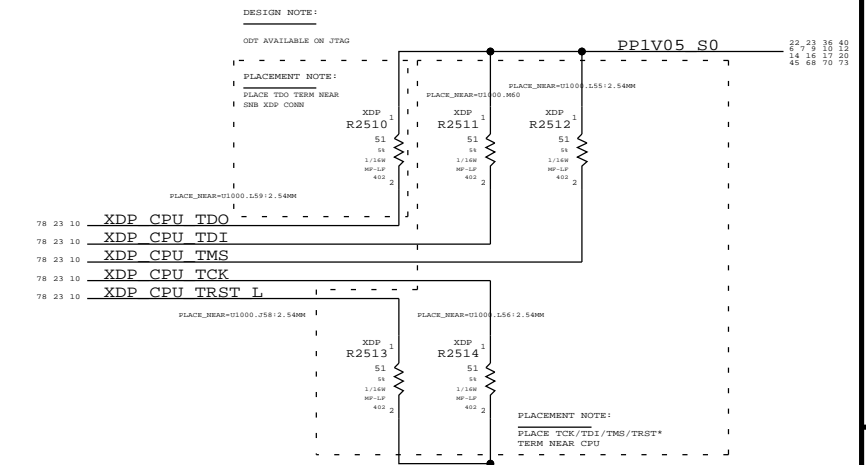
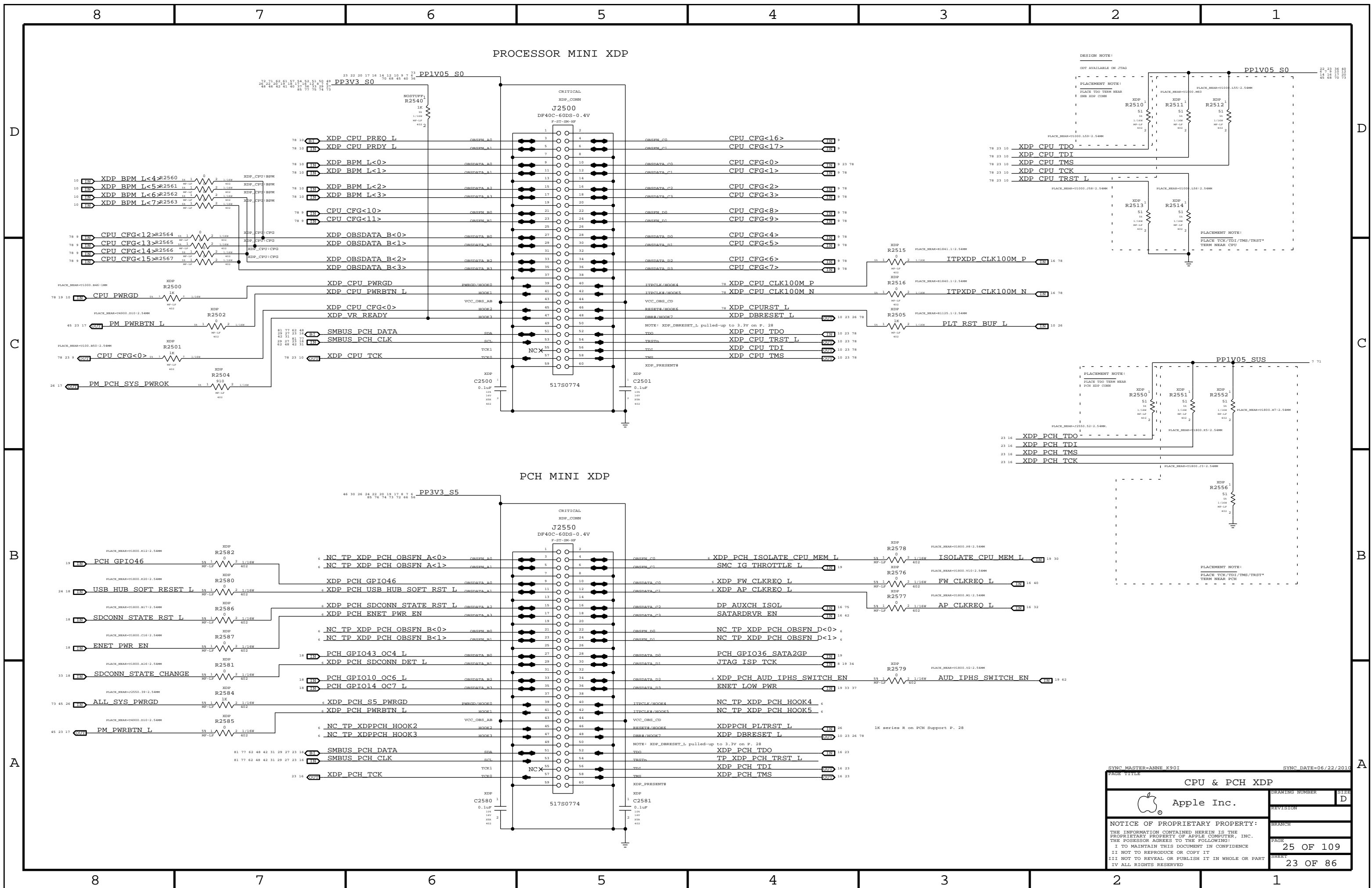
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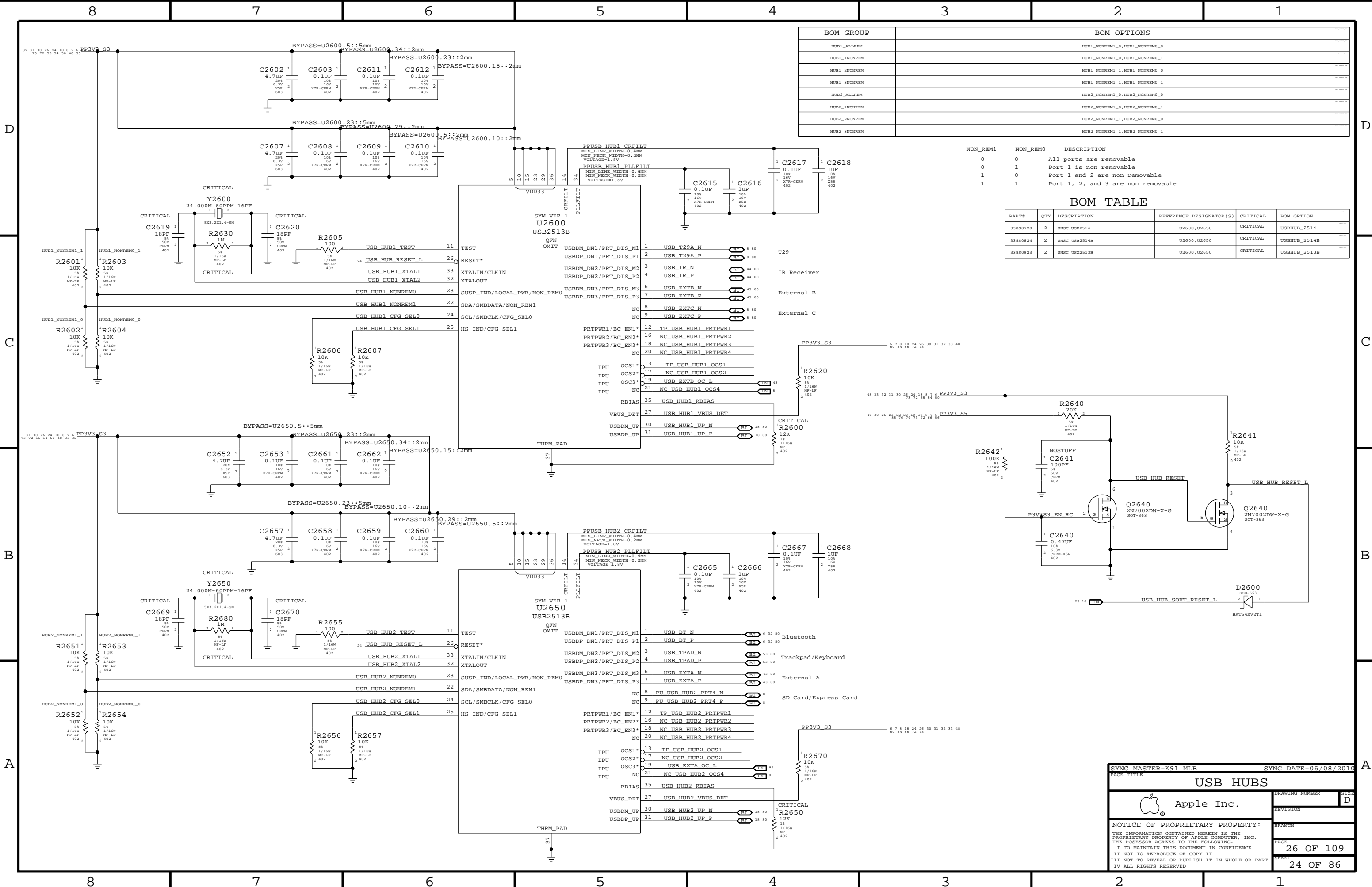
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CPU & PCH XDP		DRAWING NUMBER	SIZE
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		PAGE	25 OF 109
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0, HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0, HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1, HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1, HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0, HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0, HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1, HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1, HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE					
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33880720	2	SMSC USB2514	U2600, U2650	CRITICAL	USBHUB_2514
33880824	2	SMSC USB2514H	U2600, U2650	CRITICAL	USBHUB_2514H
33880923	2	SMSC USB2513B	U2600, U2650	CRITICAL	USBHUB_2513B

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USB HUBS

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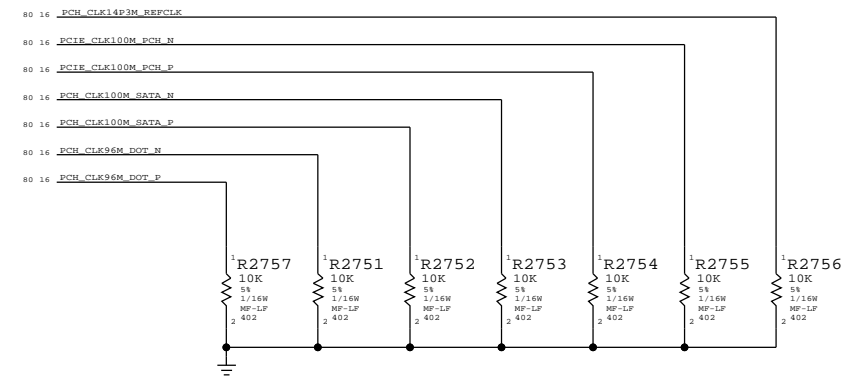
DRAWING NUMBER: D
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8 7 6 5 4 3 2 1

D
C
B
A

D
C
B
A

UNUSED clock terminations for FCIM MODE



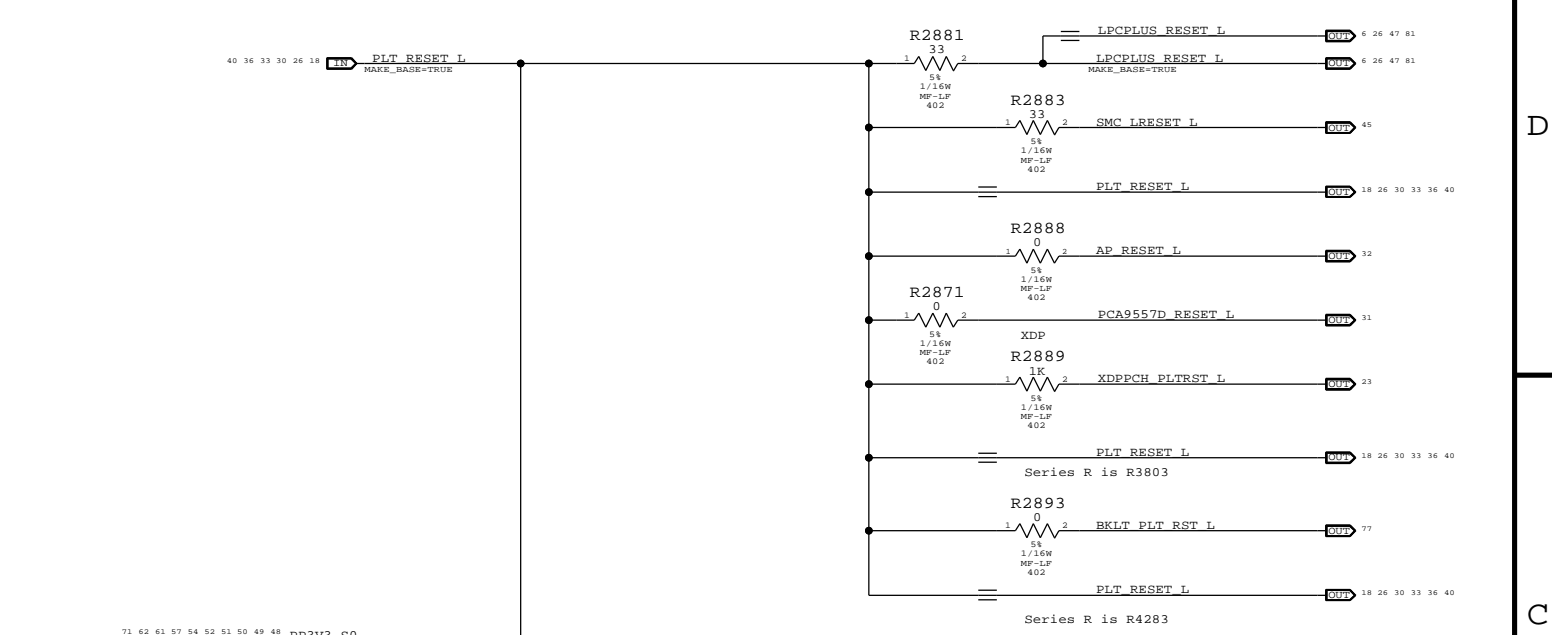
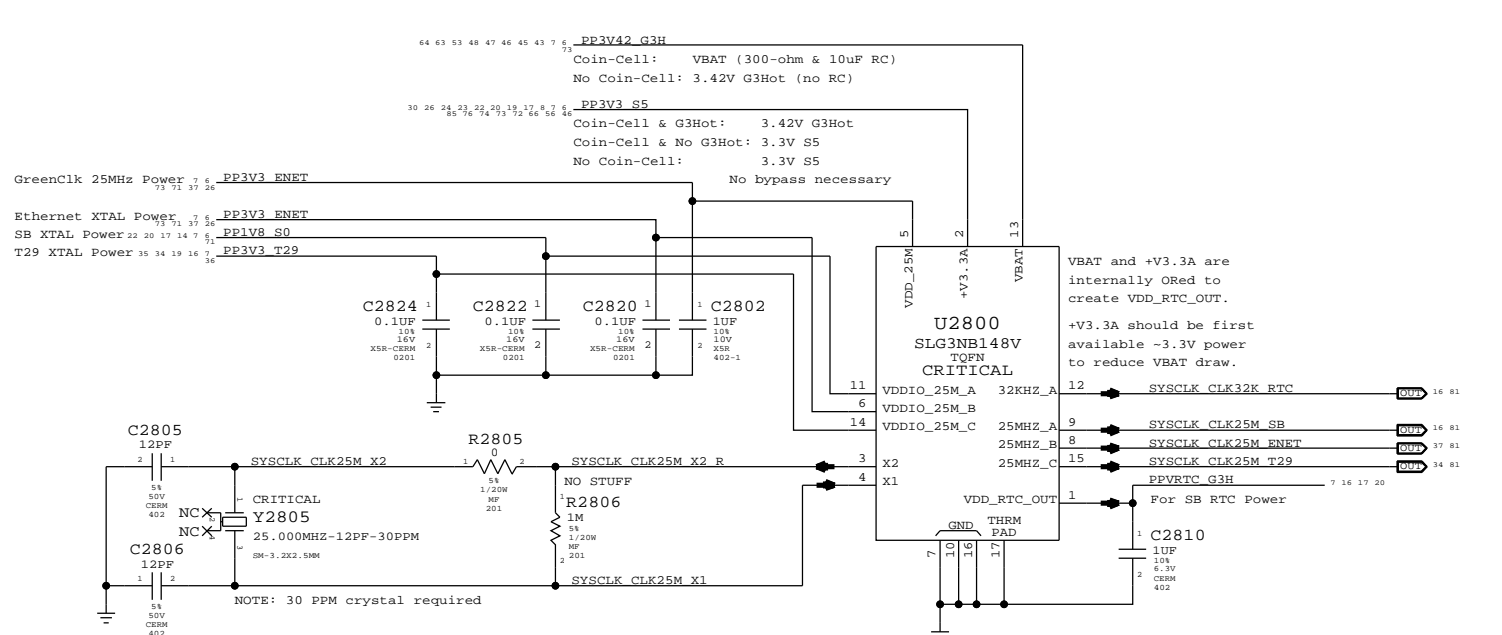
SYMC_MASTER=K11_MCB		SYMC_DATE=06/21/2011	
PAGE TITLE			
Clock (CK505)			
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		D	
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SHEET		25 OF 86	

8 7 6 5 4 3 2 1

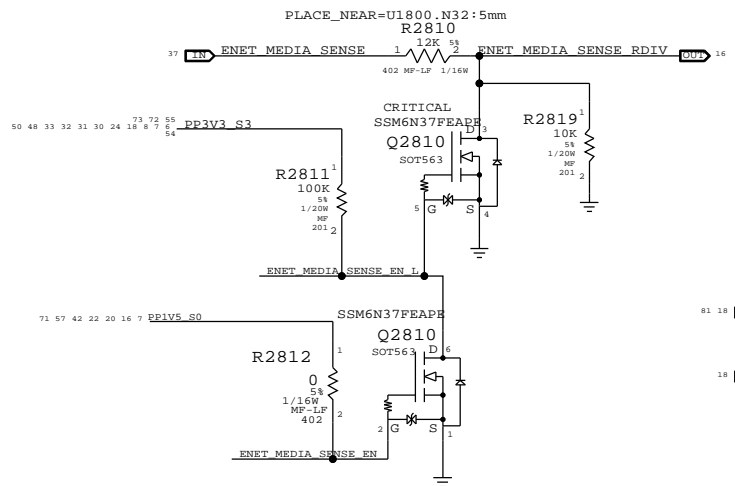
System RTC Power Source & 32kHz / 25MHz Clock Generator

Platform Reset Connections

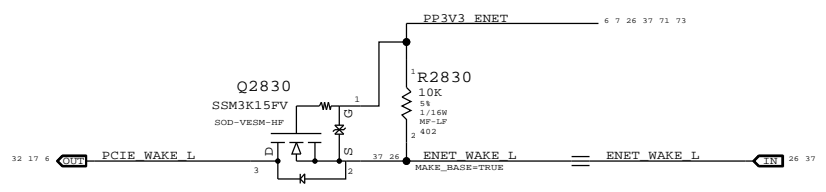
D
C
B
A



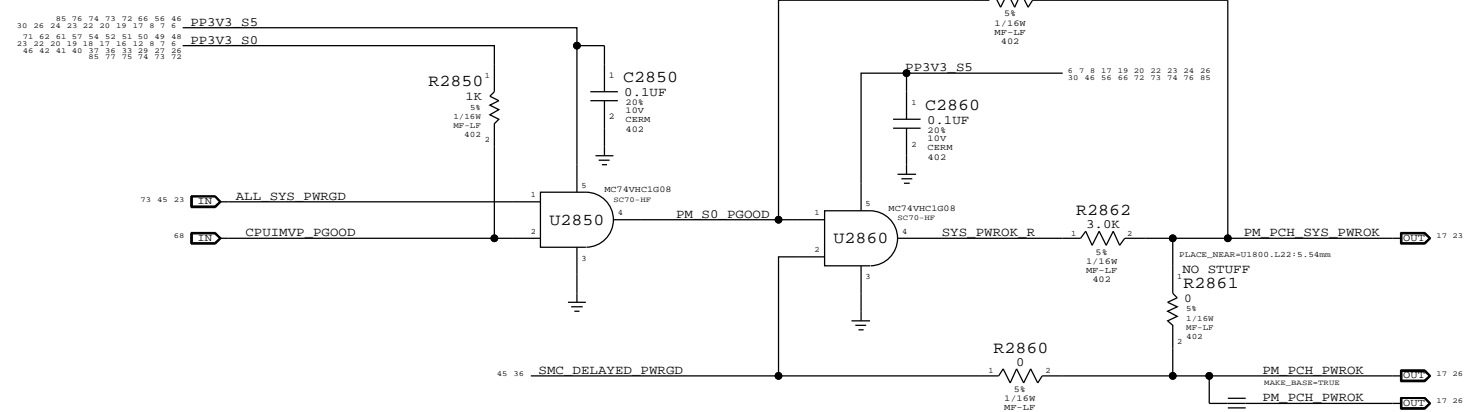
ENET_MEDIA_SENSE ISOLATION CIRCUIT



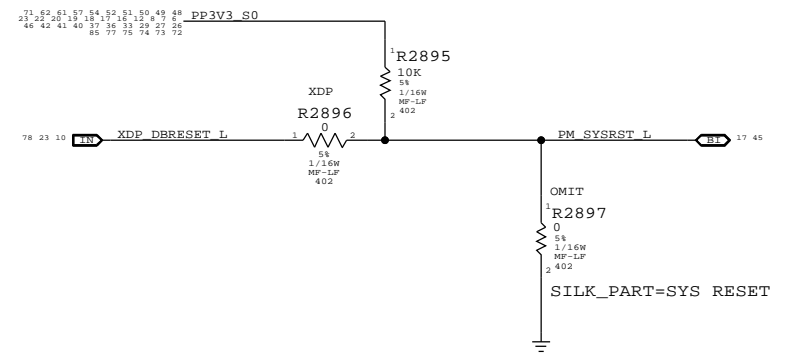
Ethernet WAKE# Isolation



PCH S0 PWRGD



PCH Reset Button



SYNC MASTER=LINDA_K901		SYNC DATE=07/08/2011	
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Chipset Support		DRAWING NUMBER	SIZE
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8 7 6 5 4 3 2 1

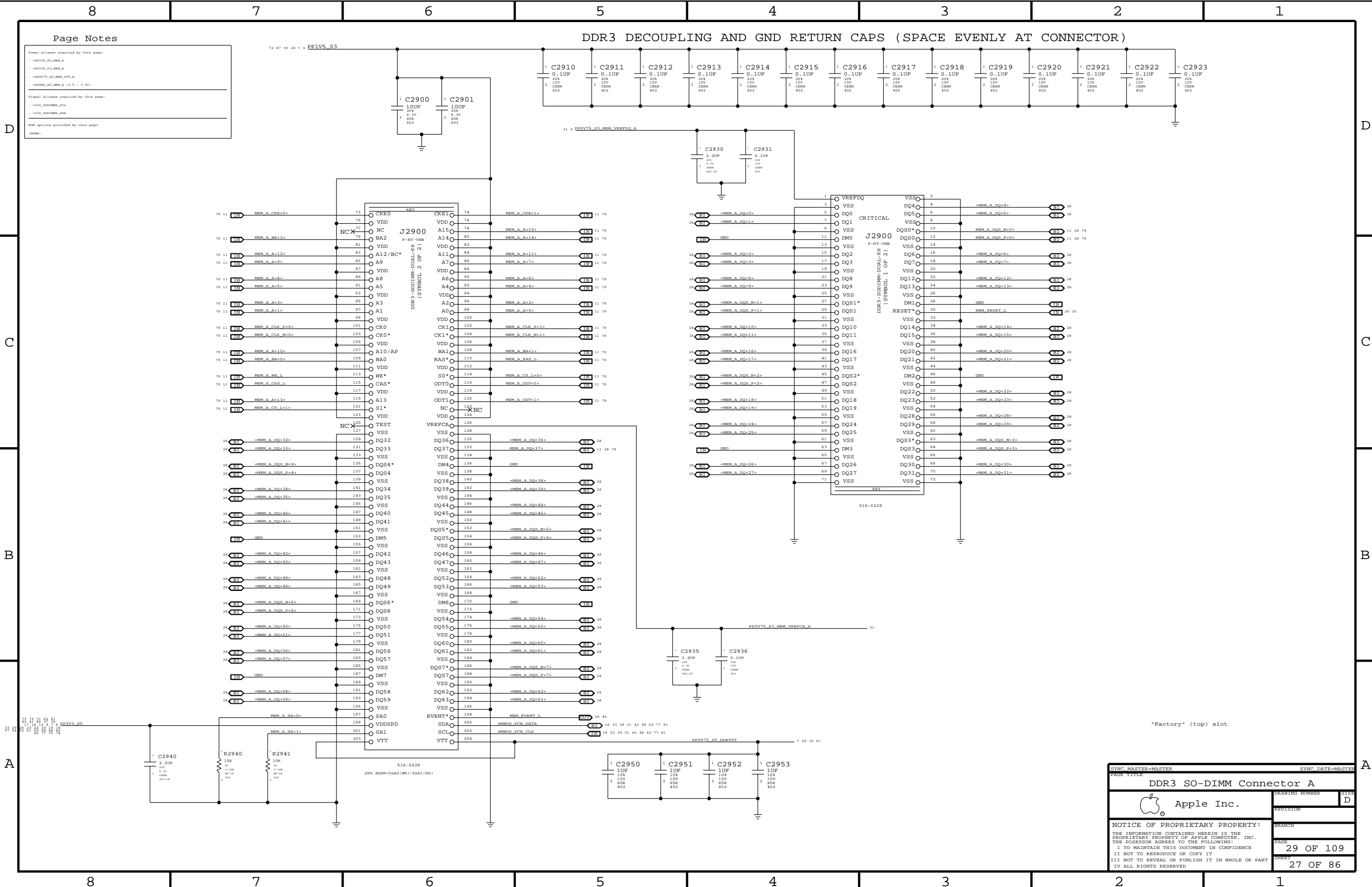
Page Notes

Power aliases required by this page:
 - P1V5_S3_MEM_A
 - P1V5_S3_MEM_A
 - P1V5_S3_MEM_VTT_A
 - P1V5_S3_MEM_A (2.5 - 3.3V)

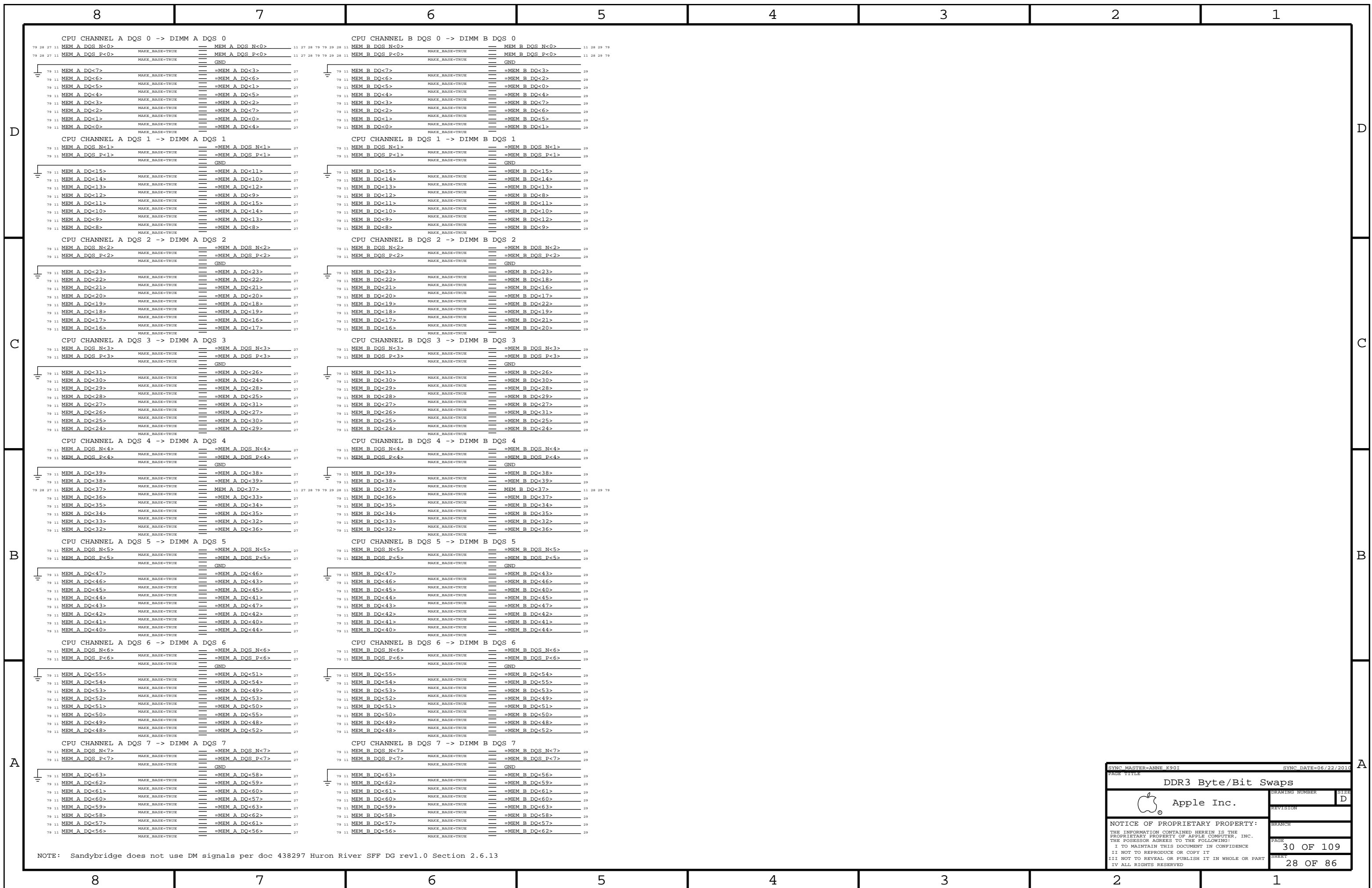
Signal aliases required by this page:
 - I2C_SDDIMM_SCL
 - I2C_SDDIMM_SDA

DRM options provided by this page:
 (NONE)


DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
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NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13

SYNC MASTER=ANNE K901		SYNC DATE=06/22/2011	
PAGE TITLE			
DDR3 Byte/Bit Swaps			
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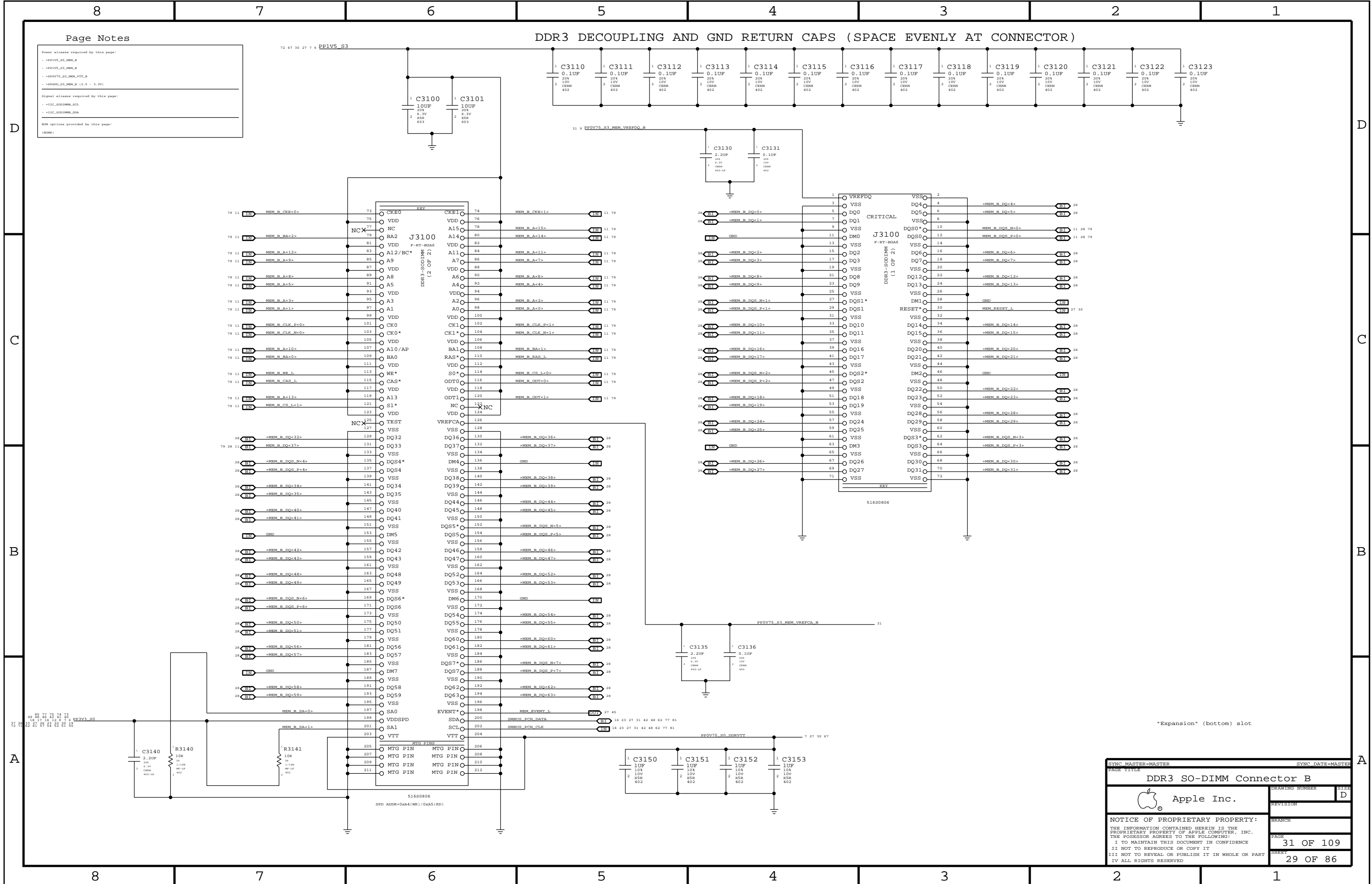
Page Notes

Power aliases required by this page:
 ->PPIV5_S3_MEM_B
 ->PPIV5_S3_MEM_B
 ->PPIV5_S3_MEM_VTT_B
 ->PPIV5_S3_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
 ->I2C_S0D0MMB_SCL
 ->I2C_S0D0MMB_SDA

MEM options provided by this page:
 (NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



SYNC MASTER=MASTER SYNC DATE=MASTER

DDR3 SO-DIMM Connector B

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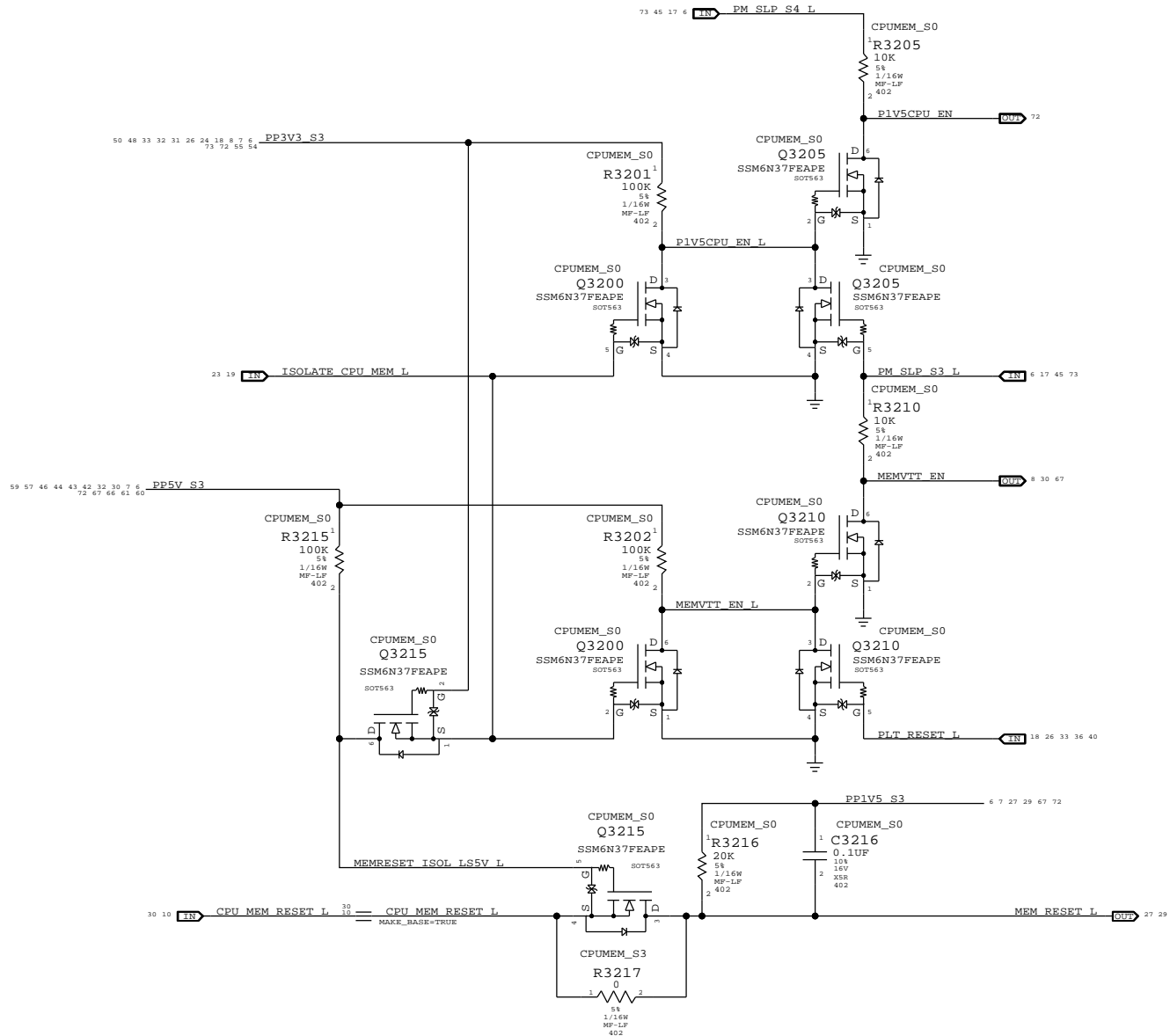
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3->S0 transitions determines behavior of signals.

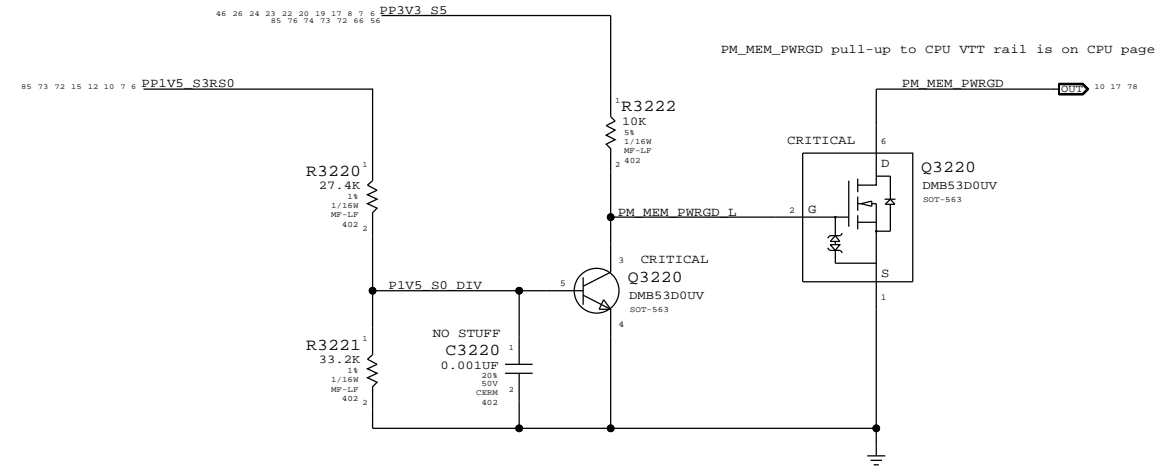
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
 MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
 MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

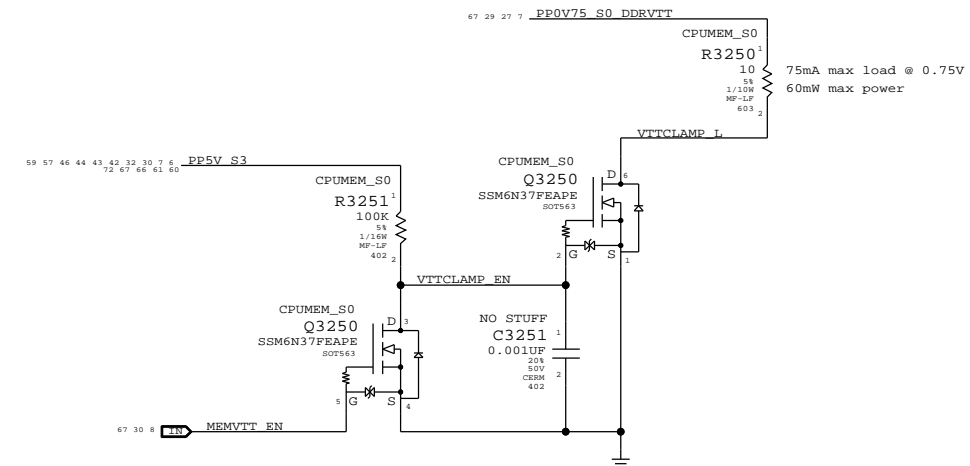


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RST_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
1	0	1	1	1	1	1	1	1
2	0	0	1	1	1	1	0	1
3	0	0	0	1	X	1	0	0
4	0	0	1	1	X	1	0	1
5	0	1	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=ANNE K901 SYNC DATE=06/22/2011

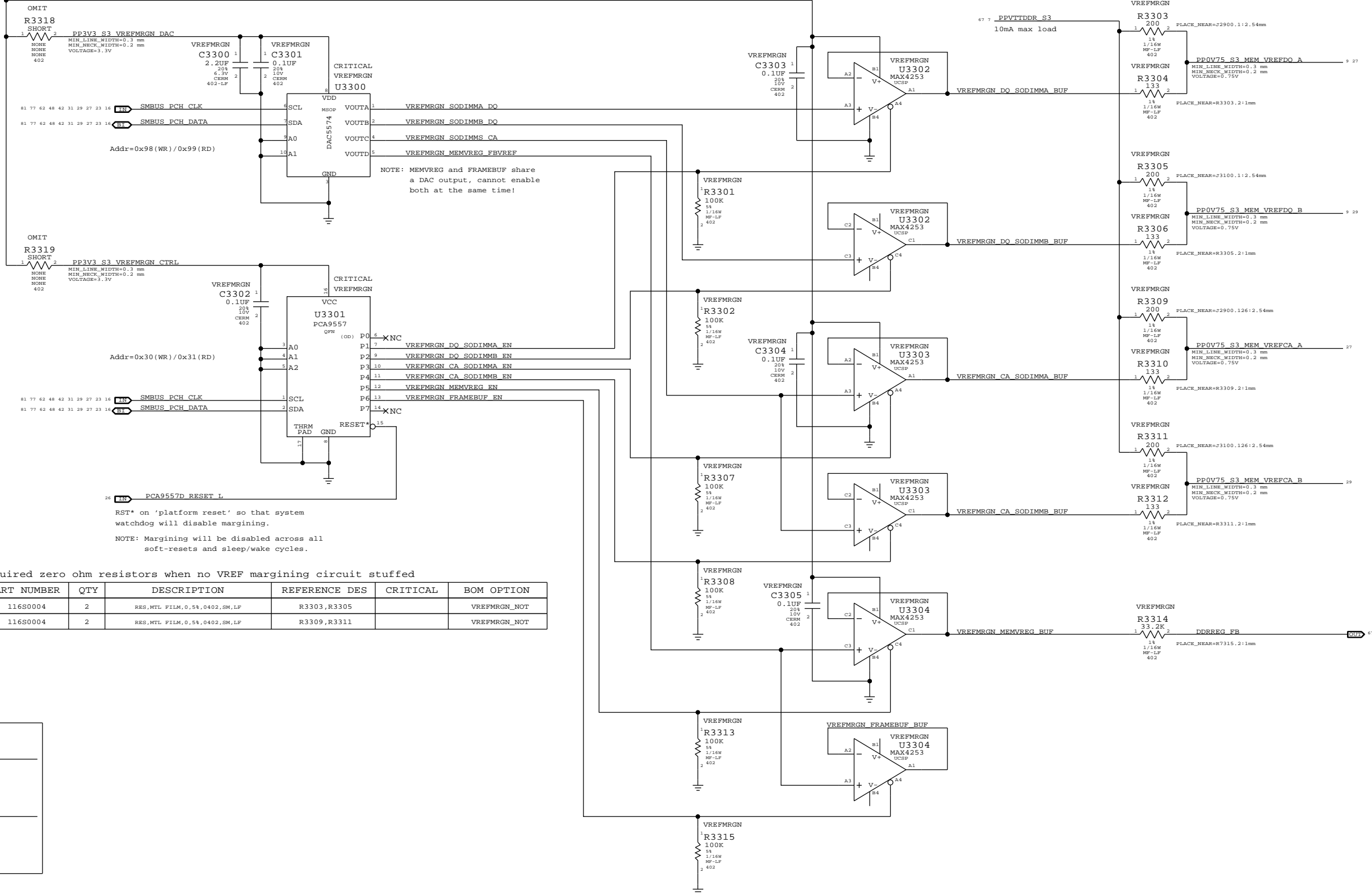
CPU Memory S3 Support

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NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Page Notes

Power aliases required by this page:
 - PP3V3_S3_VREFMRGN
 - PPTTDDR_S3_DDR_BUF

Signal aliases required by this page:
 - I2C_VREFDACS_SCL
 - I2C_VREFDACS_SDA
 - I2C_PCA9557D_SCL
 - I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN - Stuffs VREF Margining Circuitry.
 VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% Vref)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value		0.75V (DAC: 0x3A)			1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 45mV)			1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)			0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
Vref current:		+3.4mA - -3.4mA (- = sourced)			+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:		7.69mV / step @ output			8.59mV / step @ output	1.51mV / step @ output

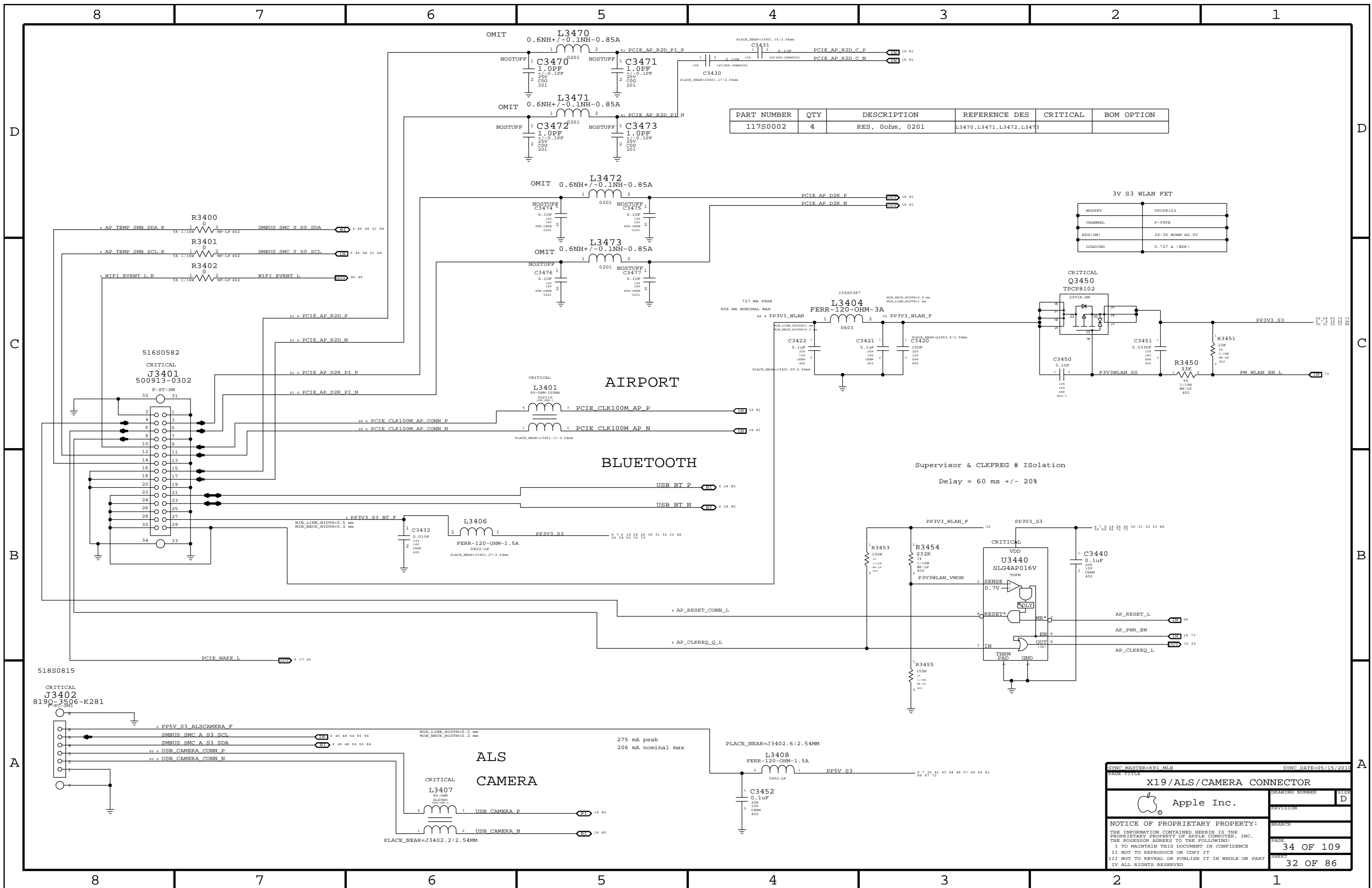
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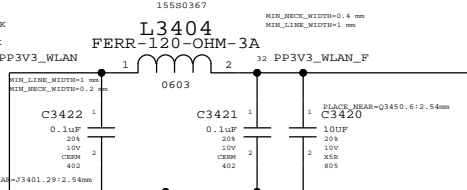
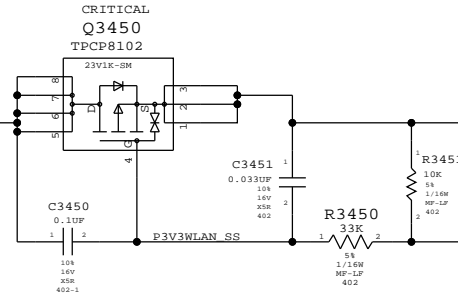
DRAWING NUMBER: 31 OF 109
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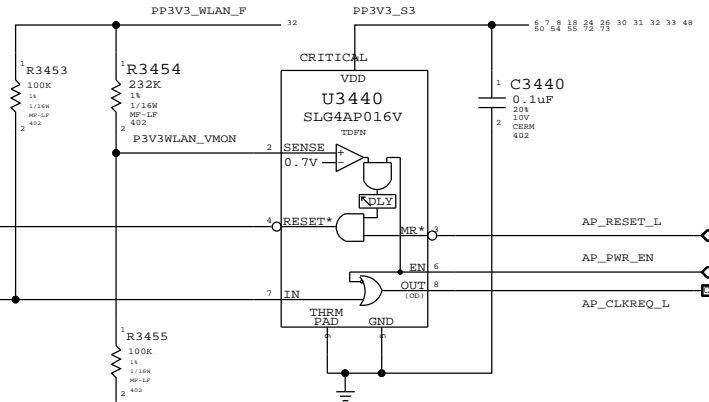
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470, L3471, L3472, L3473		

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (RDP)



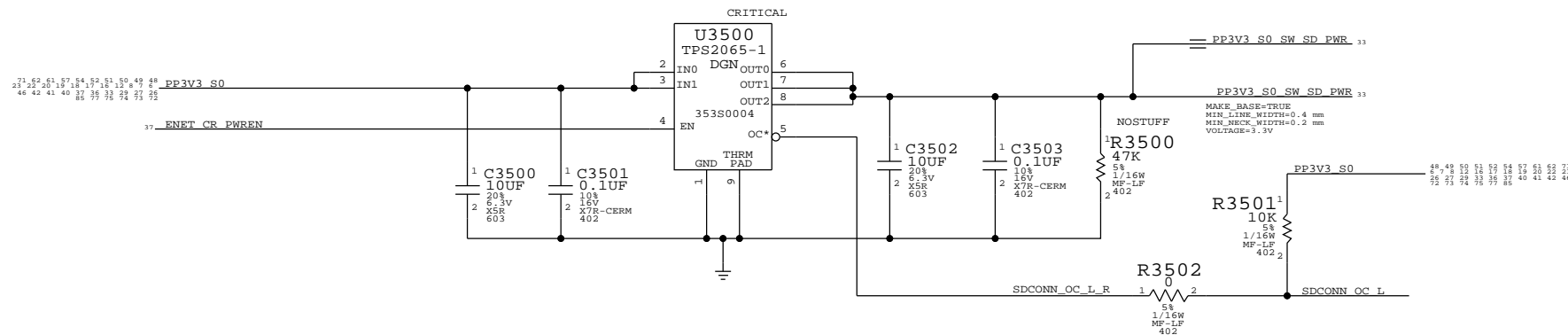
Supervisor & CLKFREQ # ISolation
Delay = 60 ms +/- 20%



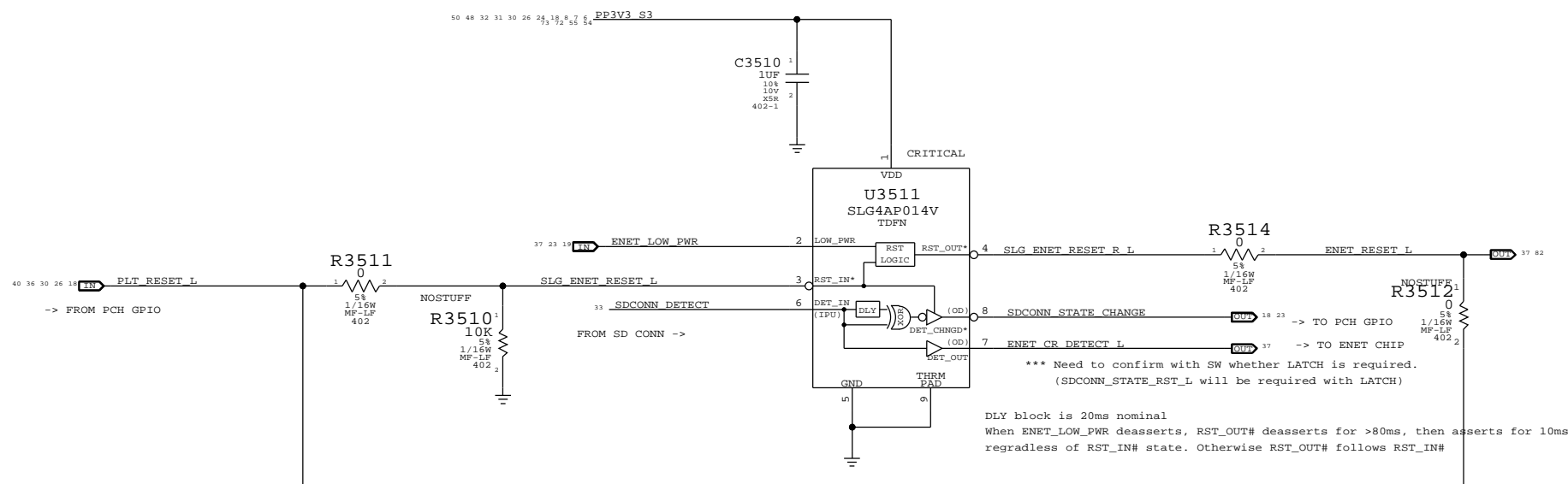
SYNC MASTER=K91_MLB		SYNC DATE=05/15/2011	
PAGE TITLE: X19/ALS/CAMERA CONNECTOR			
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SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

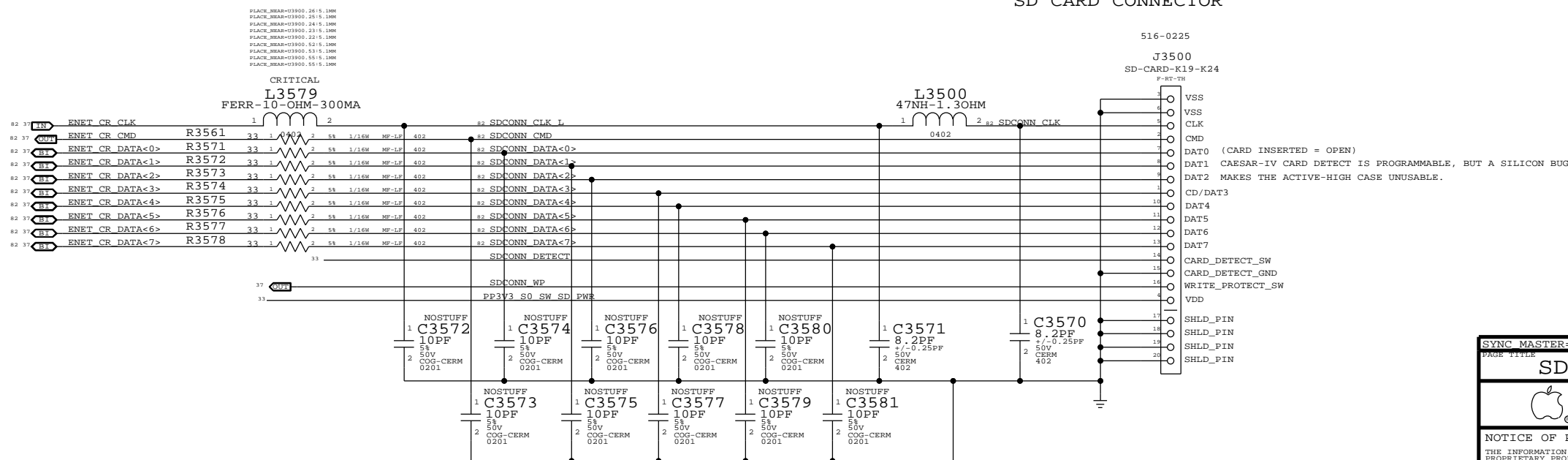
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



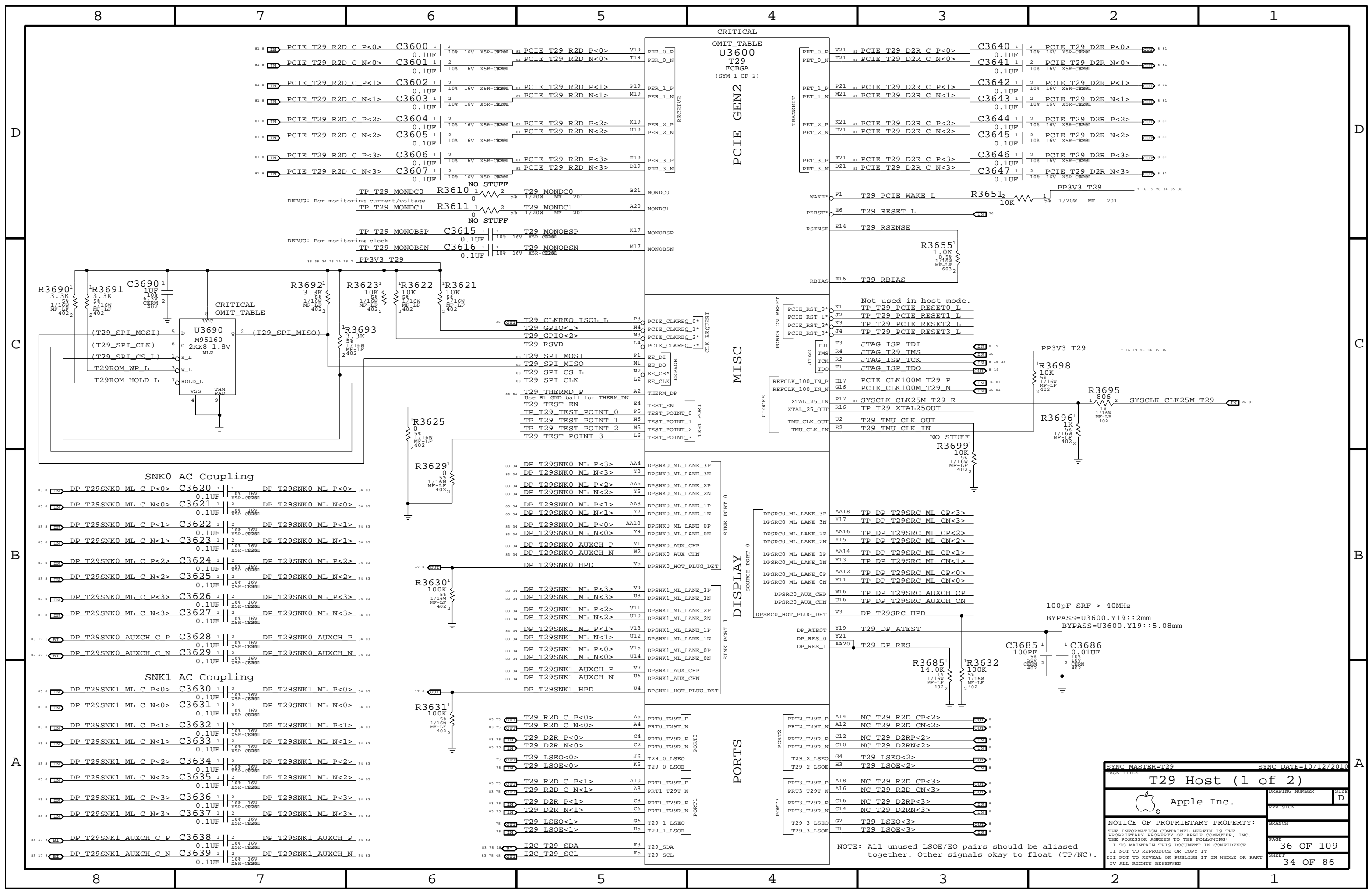
SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SD CARD CONNECTOR



SYNC MASTER=K91 MLB		SYNC DATE=05/26/2010	
SD READER CONNECTOR			
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SYNC MASTER=T29 SYNC DATE=10/12/2010

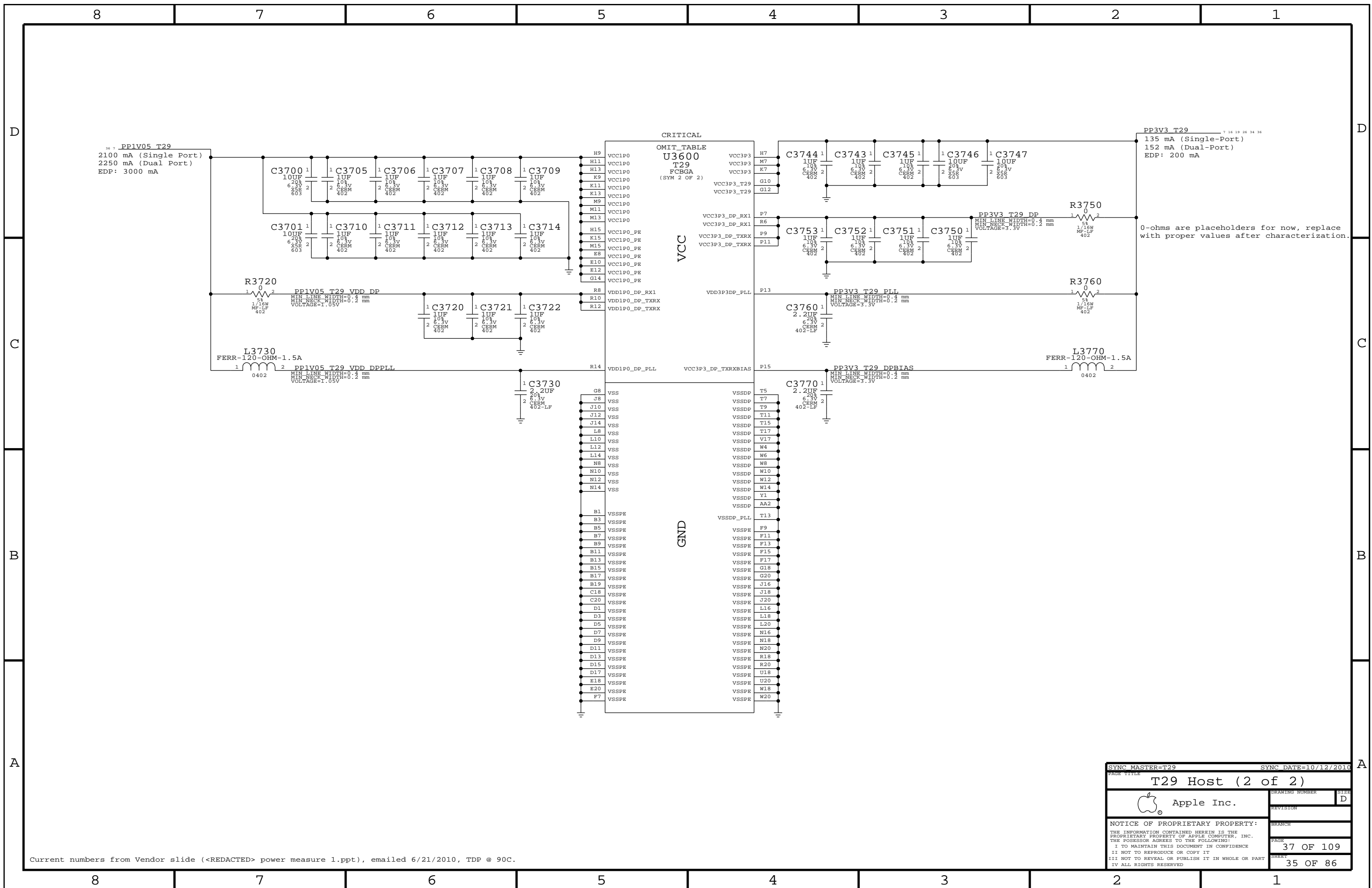
T29 Host (1 of 2)

Apple Inc.

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DRAWING NUMBER: D
 REVISION: 1
 PAGE: 36 OF 109
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NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).



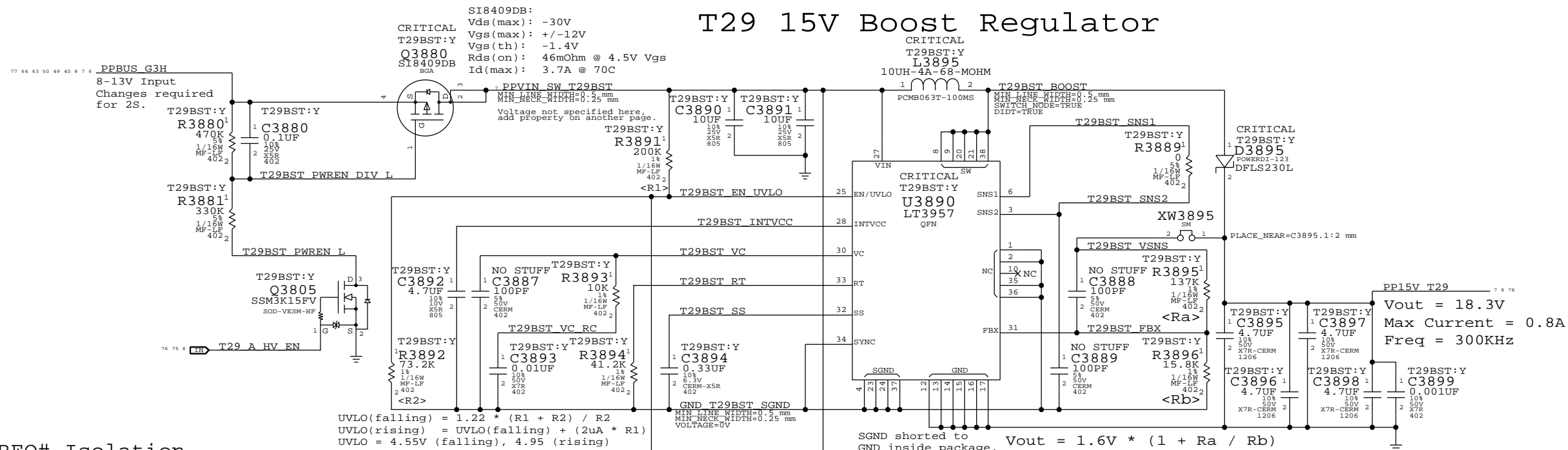
Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC MASTER=T29		SYNC DATE=10/12/2010	
PAGE TITLE T29 Host (2 of 2)			
Apple Inc.		DRAWING NUMBER	SIZE D
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		PAGE	37 OF 109
		SHEET	35 OF 86

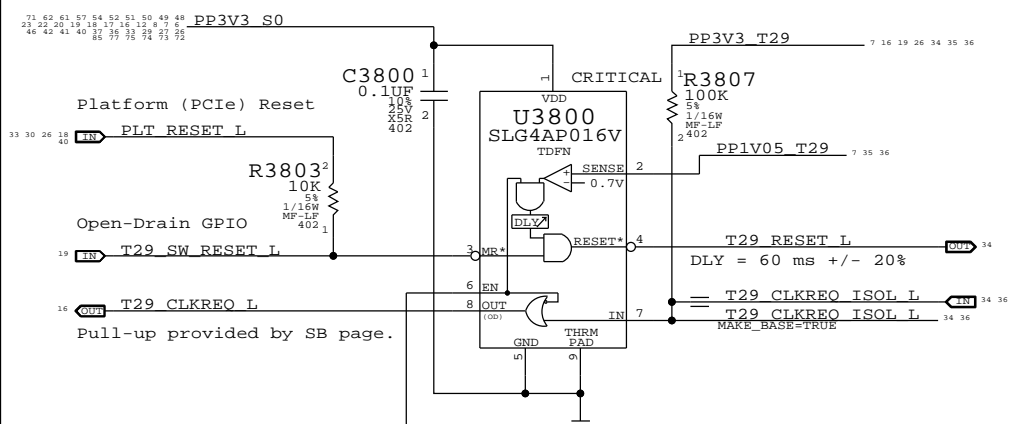
Page Notes

- Power aliases required by this page:
- PPVIN_SW_T29BST (8-13V Boost Input)
 - PP18V_T29_REG (18V Boost Output)
 - PP3V3_T29_P3V3T29FET (3.3V FET Input)
 - PP3V3_T29_FET (3.3V FET Output)
 - PP3V3_S0_T29PWRCTL
 - PP1V05_T29_P1V05T29FET (1.05V FET Input)
 - PP1V05_T29_FET (1.05V FET Output)
- Signal aliases required by this page:
- T29_CLKREQ_L
 - T29_RESET_L
- BOM options provided by this page:
- T29BST:Y - Stuffs 18V boost circuitry.

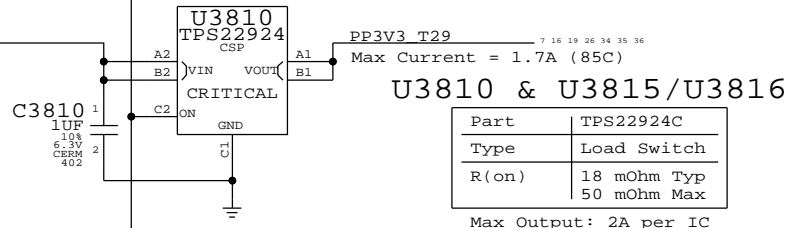
T29 15V Boost Regulator



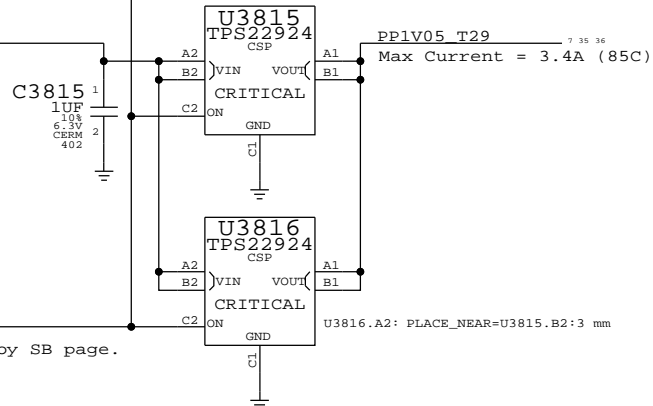
Supervisor & CLKREQ# Isolation



3.3V T29 Switch



1.05V T29 Switch



SYNC MASTER=T29		SYNC DATE=10/12/2010	
PAGE TITLE			
T29 Power Support			
Apple Inc.		DRAWING NUMBER	SIZE
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
 If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
 If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
 Special Star routing needed on these pins. Decoupling on Pg 37.

73 71 37 26 7 6 PP3V3 ENET
 281mA (1000base-T max power, Caesar IV)

PP1V2 S3 ENET INTREG 6 71
 ???mA (1000base-T, Caesar V)

D

D

C

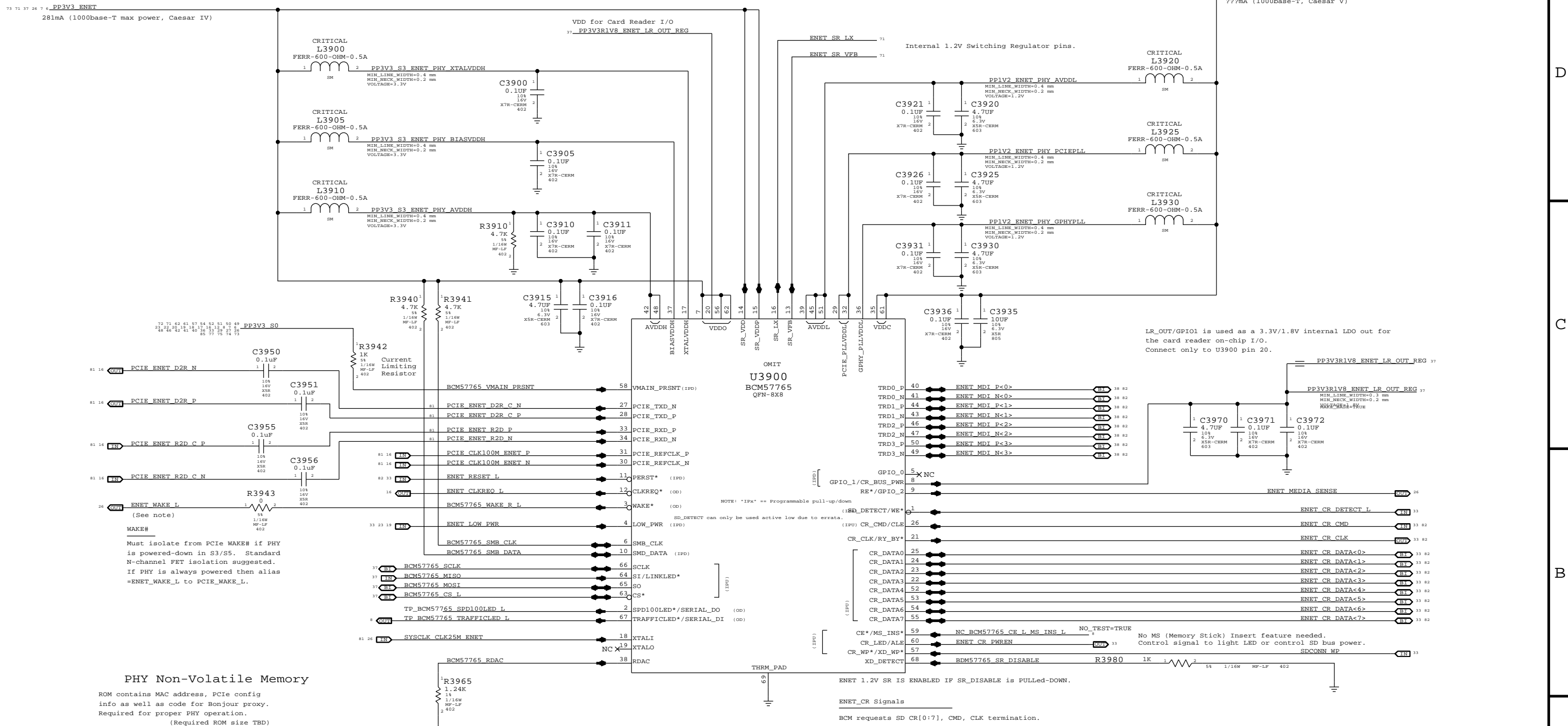
C

B

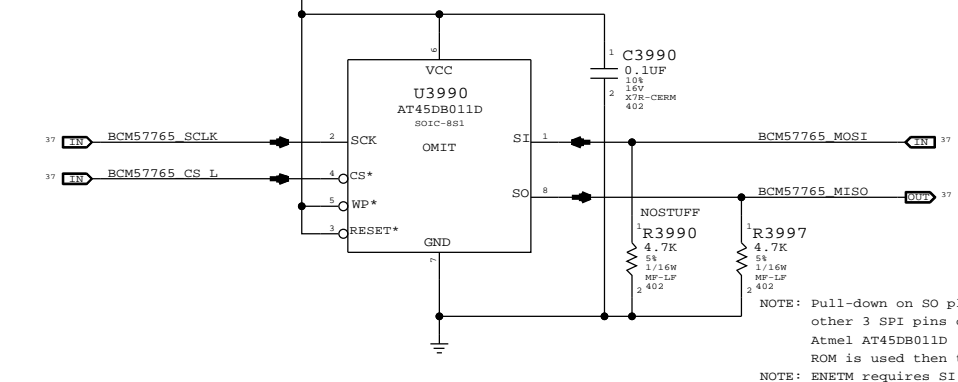
B

A

A



73 71 37 26 7 6 PP3V3 ENET



SYNC MASTER=K91 MLB SYNC DATE=05/26/2011

ETHERNET PHY (CAESAR IV)

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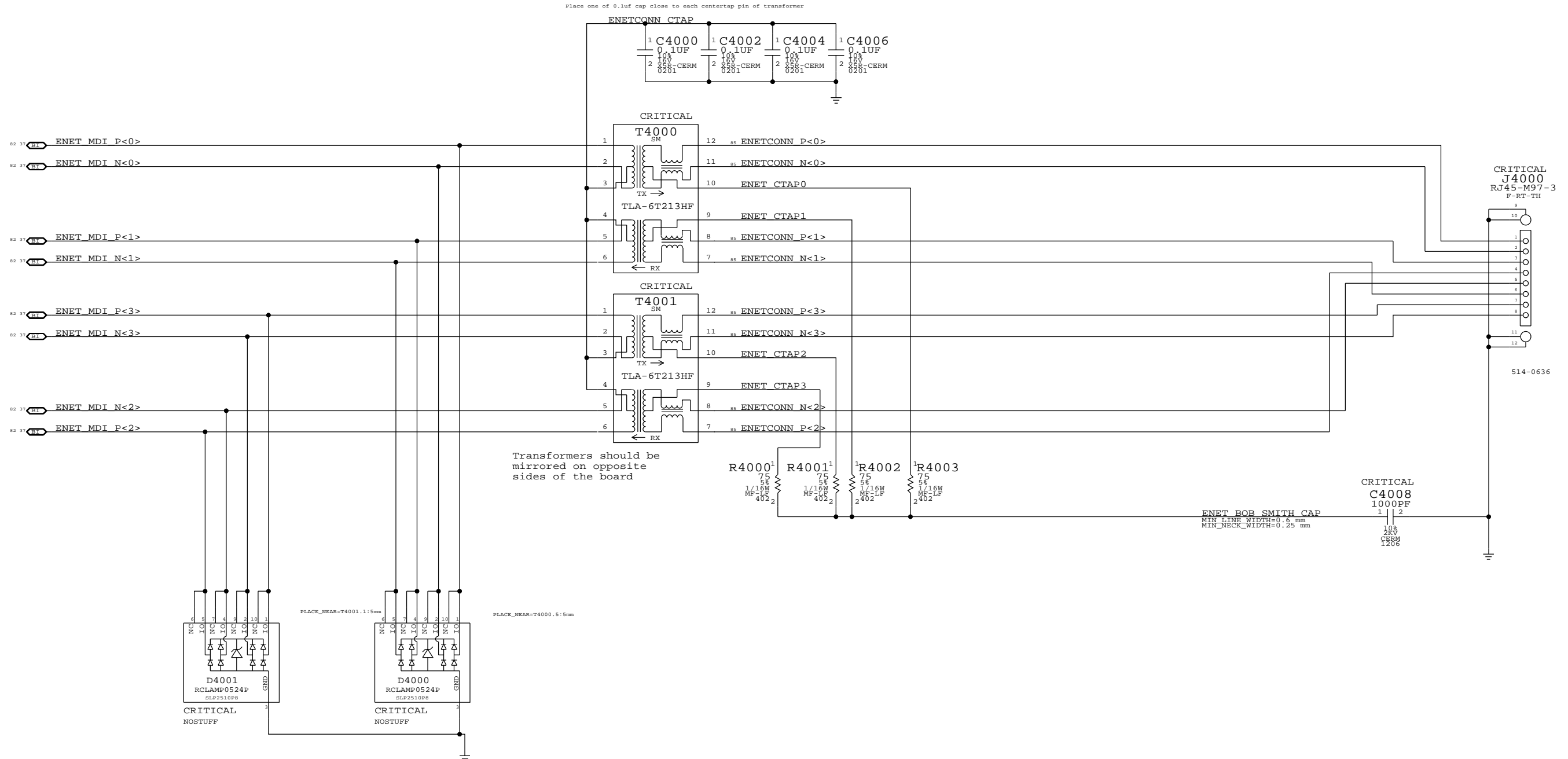
DRAWING NUMBER: SIZE D
 REVISION: _____
 BRANCH: _____
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Page Notes

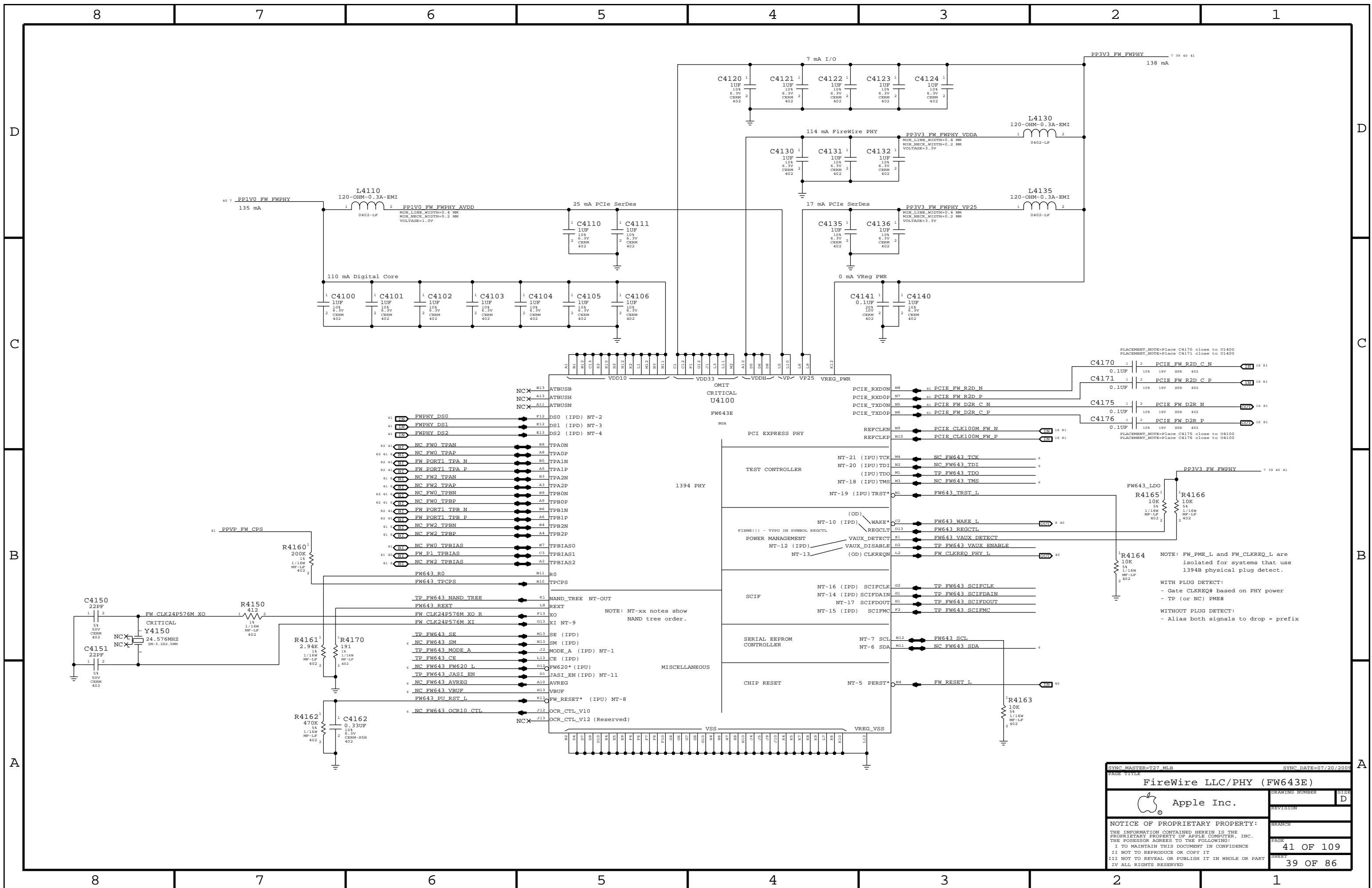
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K91_MLB		SYNC DATE=05/26/2011	
PAGE TITLE			
Ethernet Connector			
Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=T27_MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
FireWire LLC/PHY (FW643E)			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	41 OF 109
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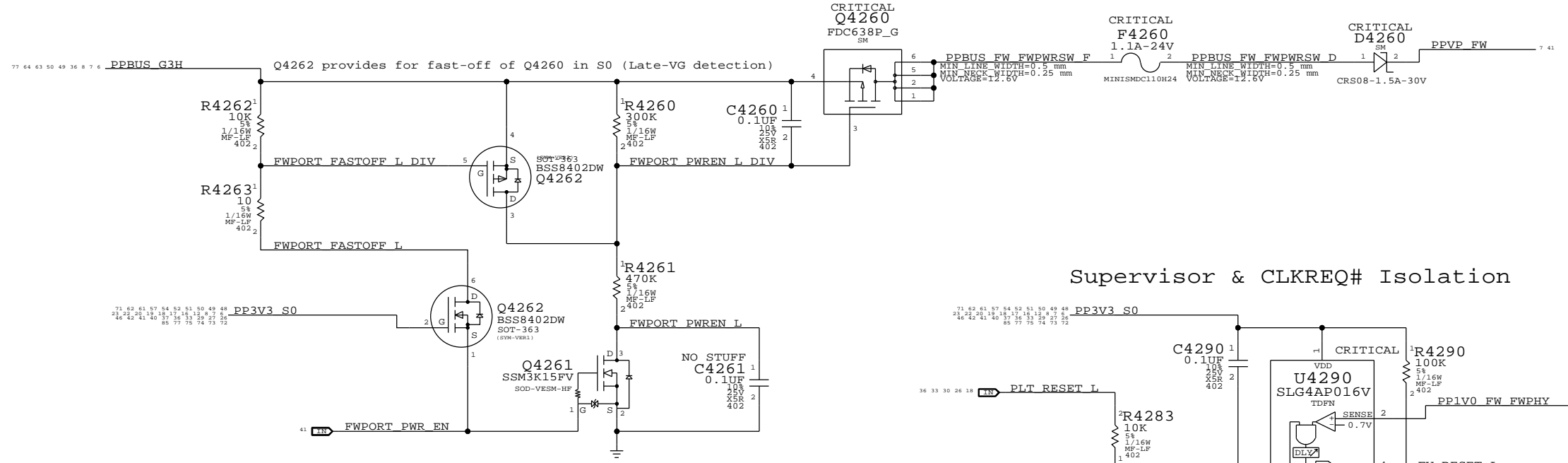
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWRSW (FW VP FET Input)
 - =PPBUS_FW_FET (FW VP FET Output)
 - =PP3V3_FW_P3V3FWFET (3.3V FET Input)
 - =PP3V3_FW_FET (3.3V FET Output)
 - =PP3V3_FW_FWPHY (PHY 3.3V Power)
 - =PP3V3_S0_FWLATEVG
 - =PP3V3_S0_FWPWRCTL (5KPD Bias Rail)
 - =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
 - =PP1V05_FW_P1V05FWFET (1.0V FET Input)
 - =PP1V0_FW_FET_R (1.0V FET Output)
 - =PP1V0_FW_FWPHY (PHY 1.0V)

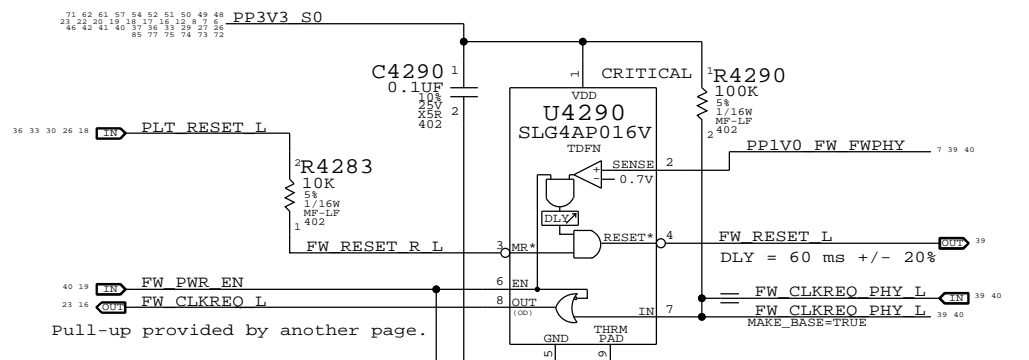
Signal aliases required by this page:
 - =FW_CLKREQ_L
 - =FW_PME_L

BOM options provided by this page:
 (NONE)

FireWire Port Power Switch

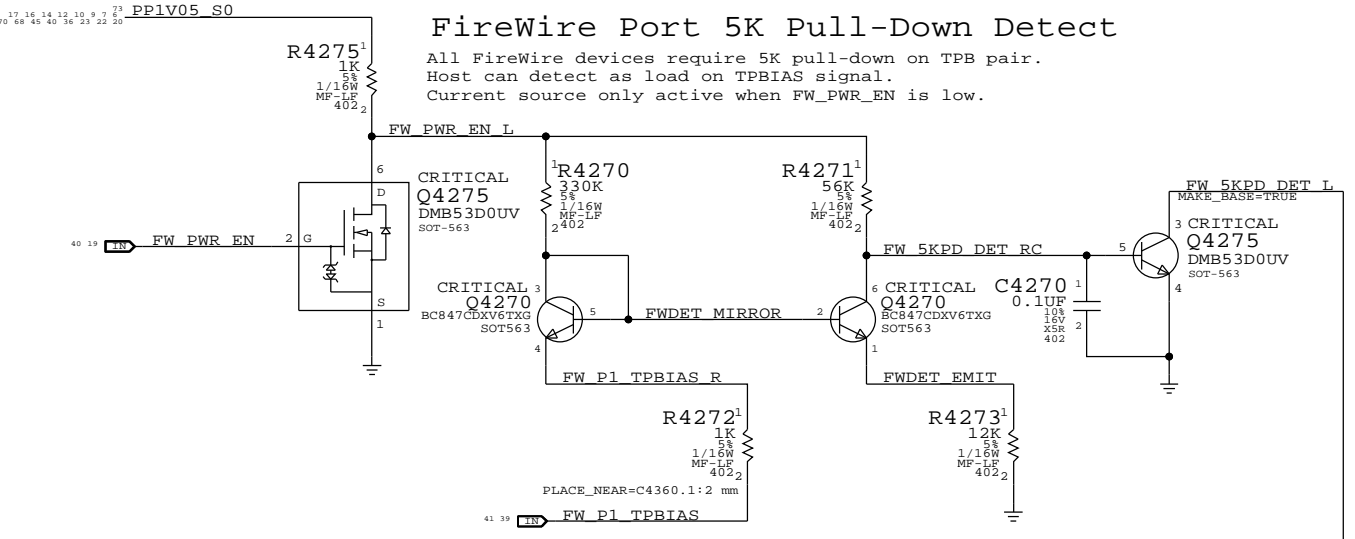


Supervisor & CLKREQ# Isolation



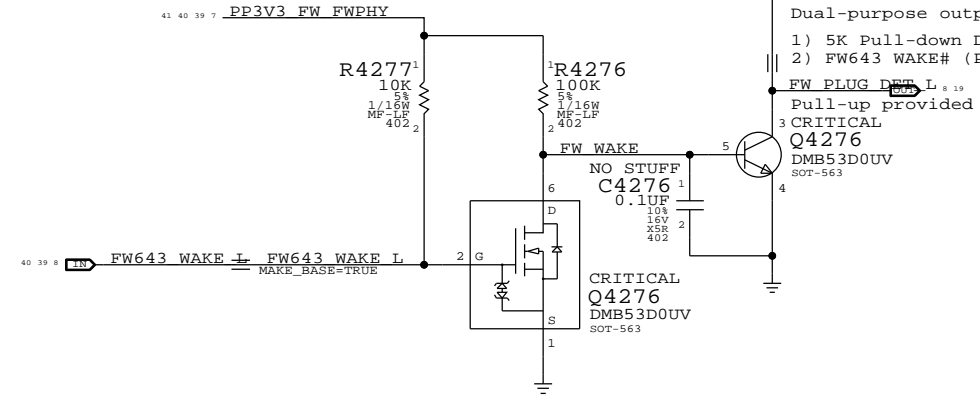
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair. Host can detect as load on TPBIAS signal. Current source only active when FW_PWR_EN is low.



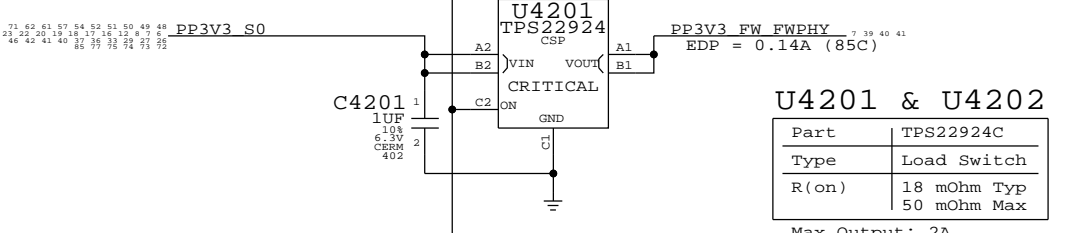
FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

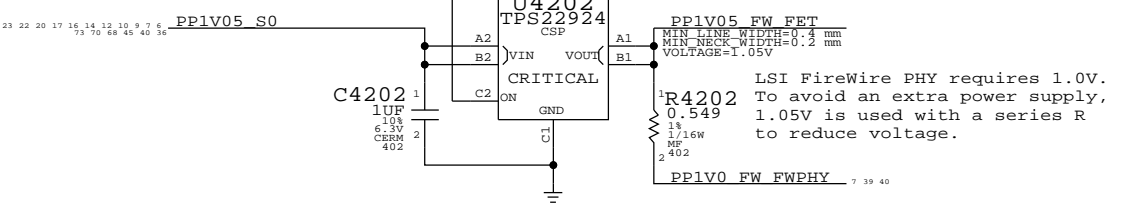


- Dual-purpose output:
 1) 5K Pull-down Detect when FW_PWR_EN is low.
 2) FW643 WAKE# (PME#) when PHY is powered.
 Pull-up provided on another page.

3.3V FW Switch



1.0V FW Switch



TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=T27 MLB SYNC DATE=12/15/2009

FireWire Port & PHY Power

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DRAWING NUMBER: D
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Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT1
 - =PPVP_FW_PHY_CPS_FET (From Port)
 - =PPVP_FW_PHY_CPS (To PHY)
 - =PP3V3_FW_FWPHY
 - =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
 - =FW_PHY_DS0
 - =FW_PHY_DS1
 - =FW_PHY_DS2

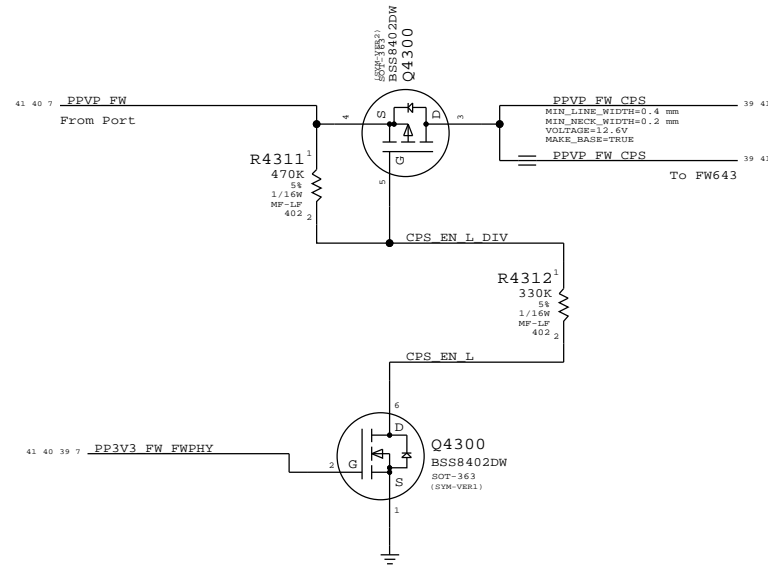
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

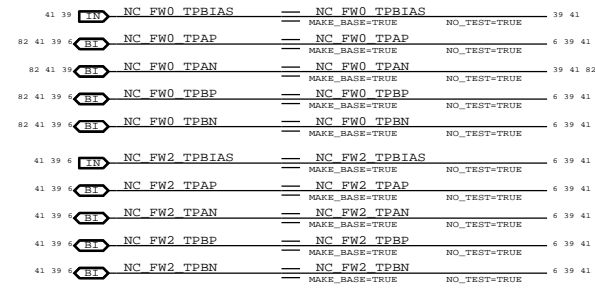
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
 FET blocks current to TPCPS until VDD33 is powered.



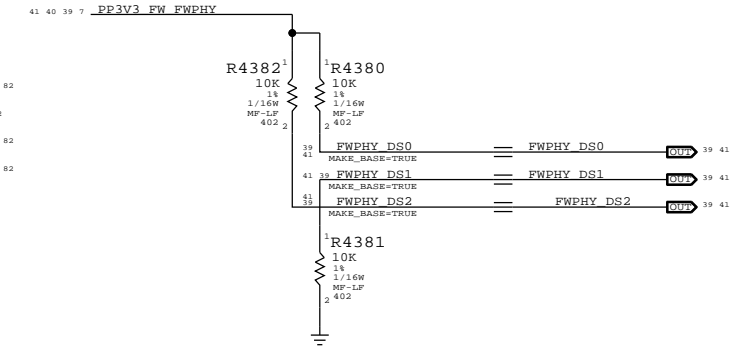
Unused FireWire Ports

Disabled per LSI instructions
 (All unused port signals TP/NC)



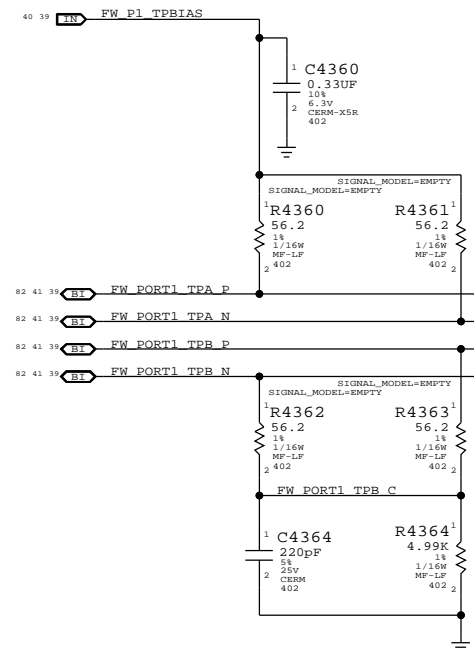
FireWire PHY Config Straps

Configures PHY for:
 - Port "1" Bilingual (1394B)



Termination

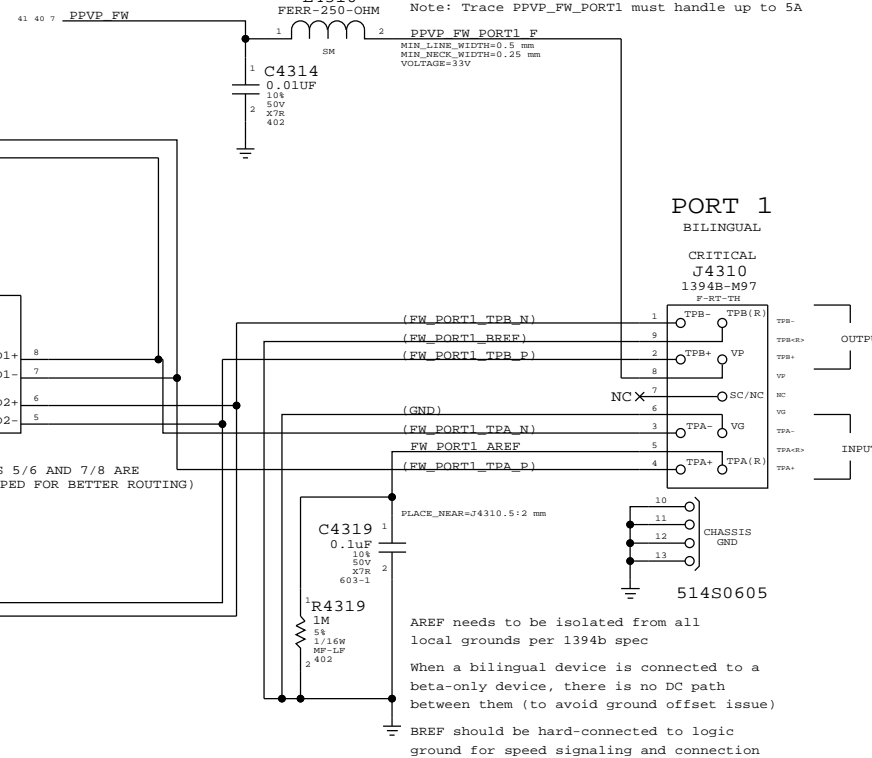
Place close to FireWire PHY



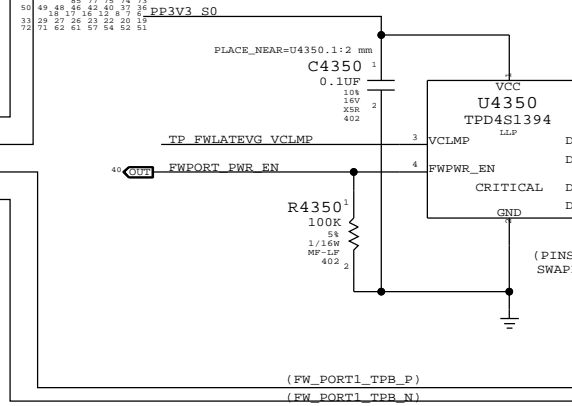
Cable Power

CRITICAL
 L4310
 FERR-250-OHM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

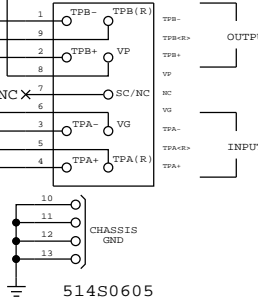


"Snapback" & "Late VG" Protection



PORT 1 BILINGUAL

CRITICAL
 J4310
 1394B-M97
 F-RT-TH



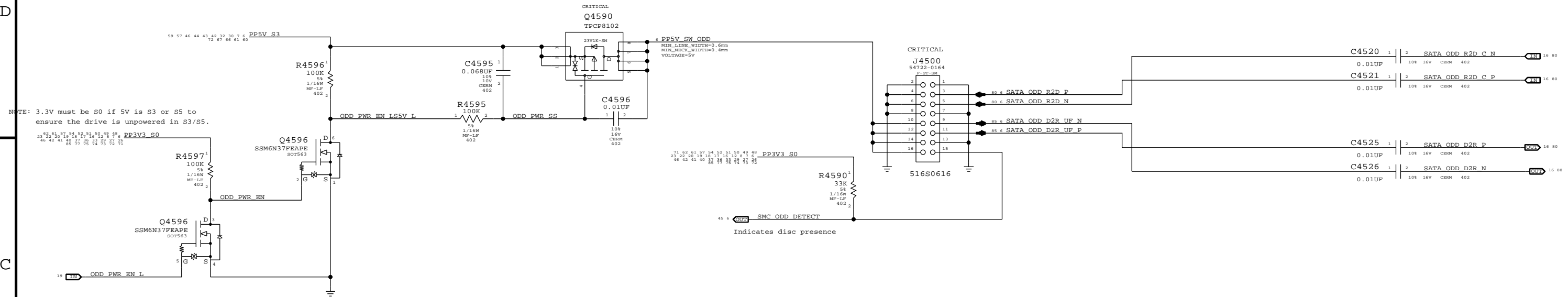
AREF needs to be isolated from all local grounds per 1394b spec
 When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)
 BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

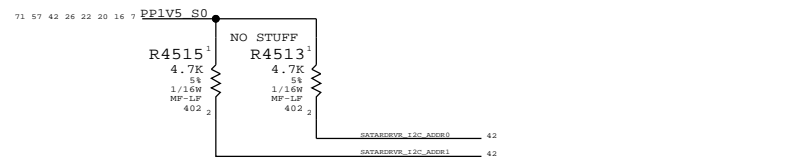
SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
PAGE TITLE			
FireWire Connector		DRAWING NUMBER	SIZE
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ODD Power Control

SATA ODD Connector



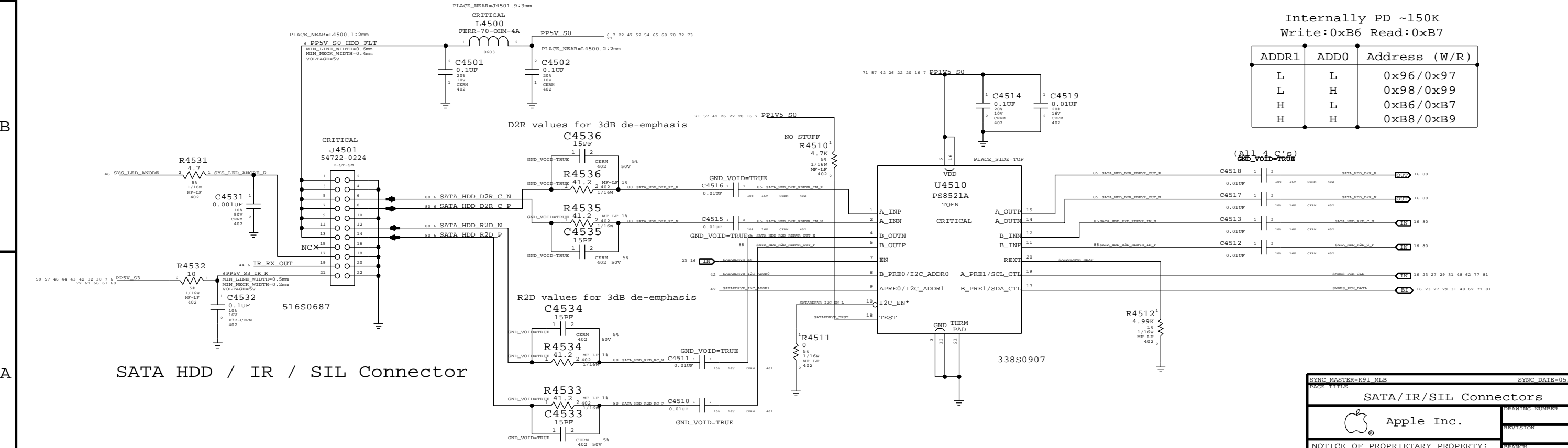
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.



Internally PD ~150K
Write: 0xB6 Read: 0xB7

ADDR1	ADD0	Address (W/R)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD / IR / SIL Connector



(All 4 C's)
GND_VOID=TRUE

SYNC MASTER=K91_MLB SYNC DATE=05/15/2011

SATA/IR/SIL Connectors

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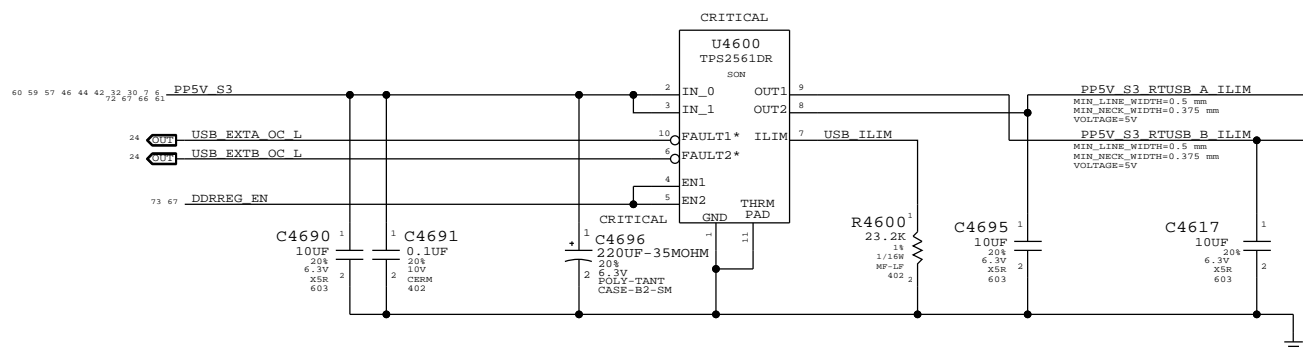
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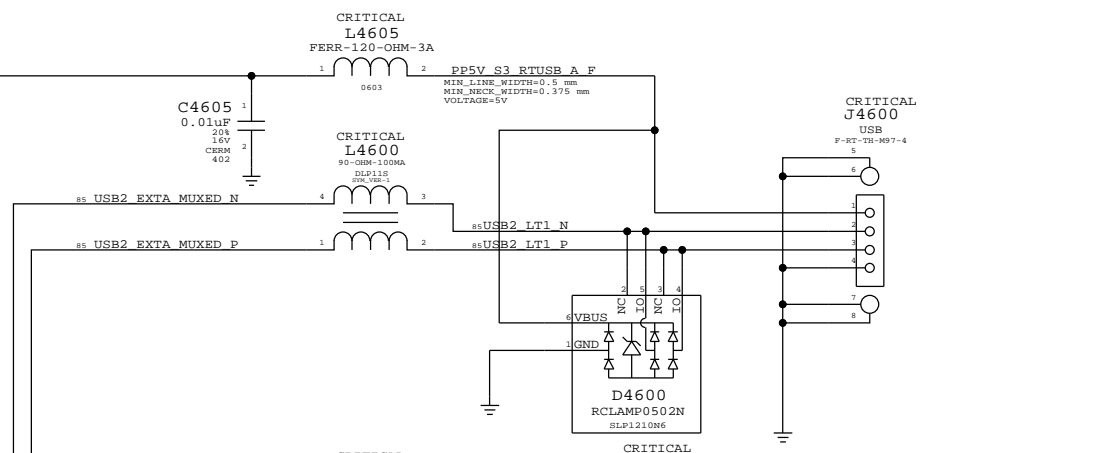
SHEET: **42 OF 86**

USB Port Power Switch



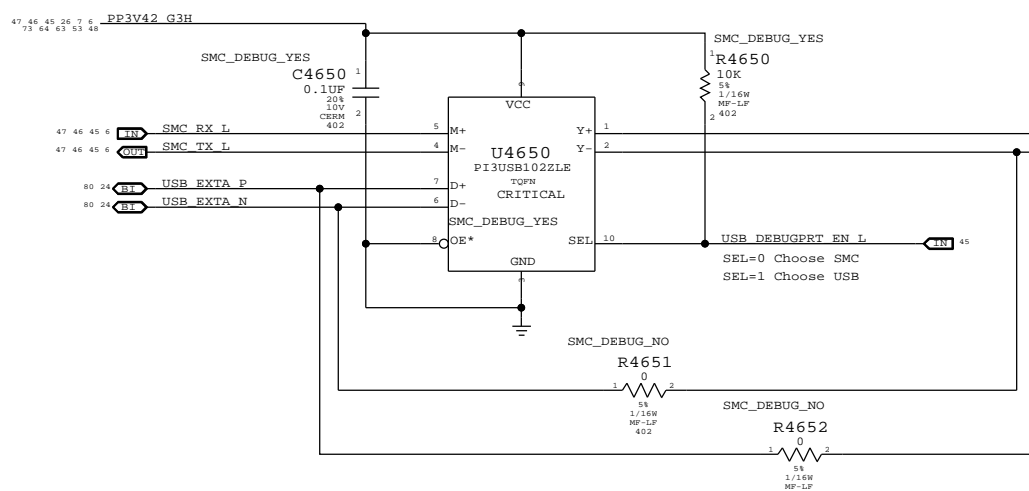
Current limit per port (R4600): 2.18A min / 2.63A max

Left USB Port A

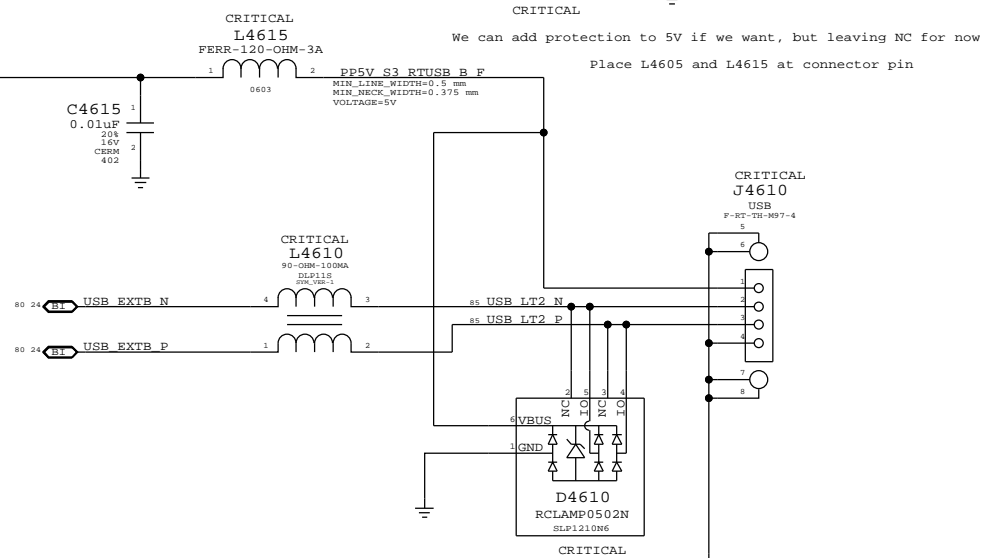


We can add protection to 5V if we want, but leaving NC for now
Place L4605 and L4615 at connector pin

USB/SMC Debug Mux

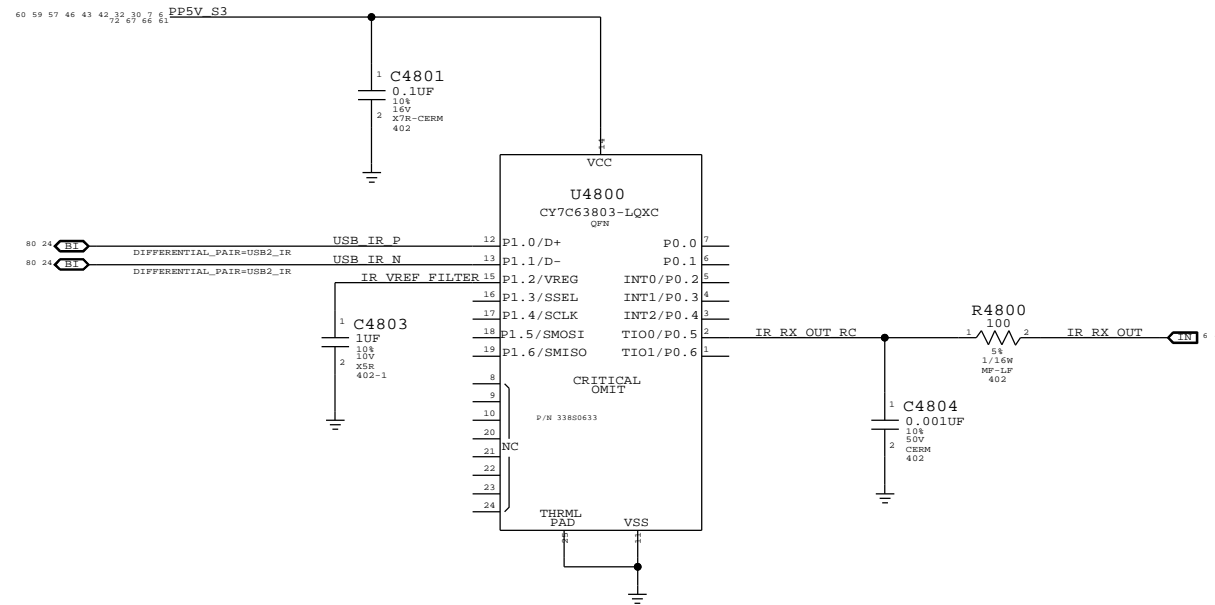


Left USB Port B



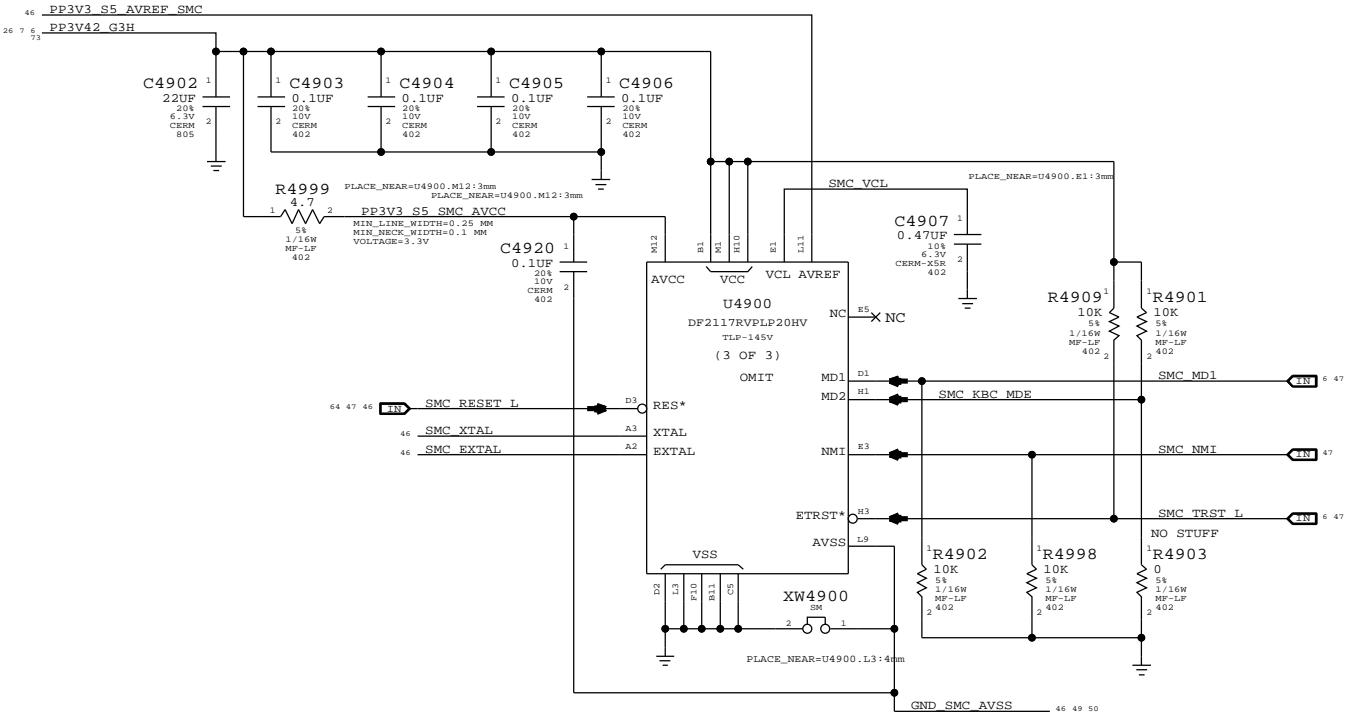
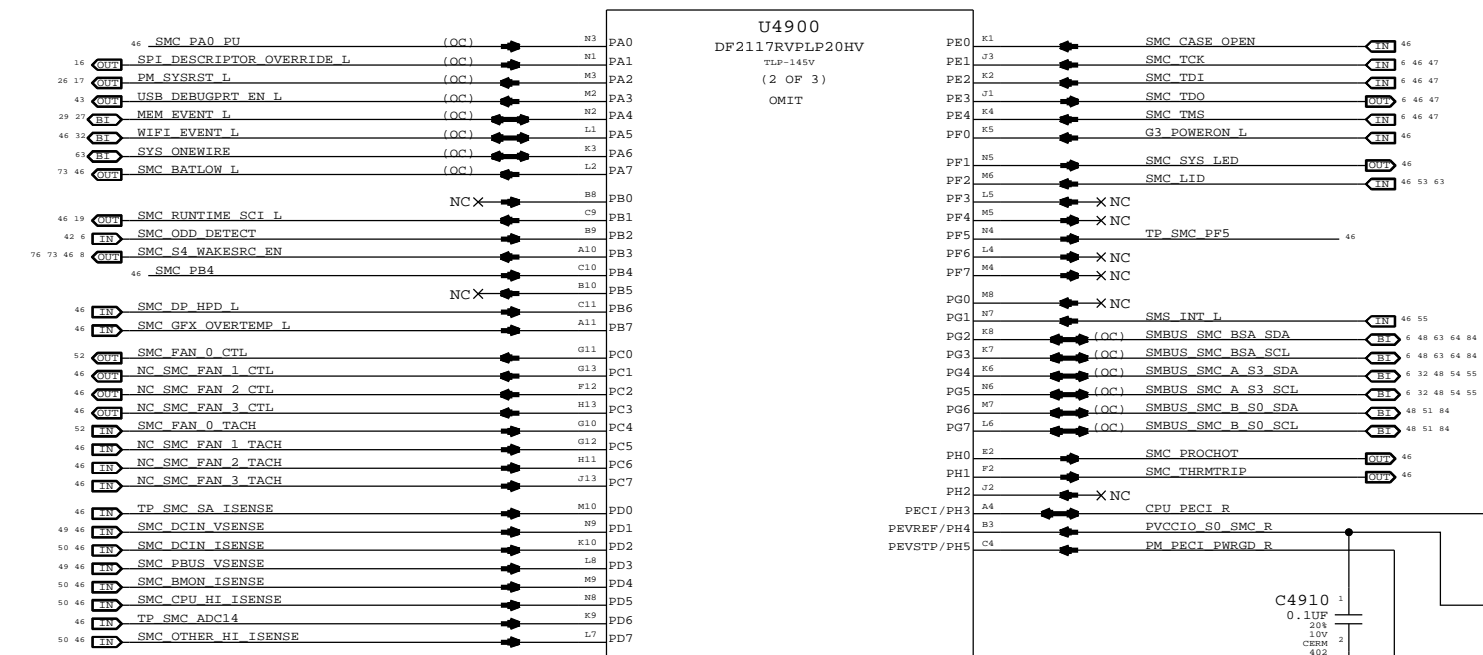
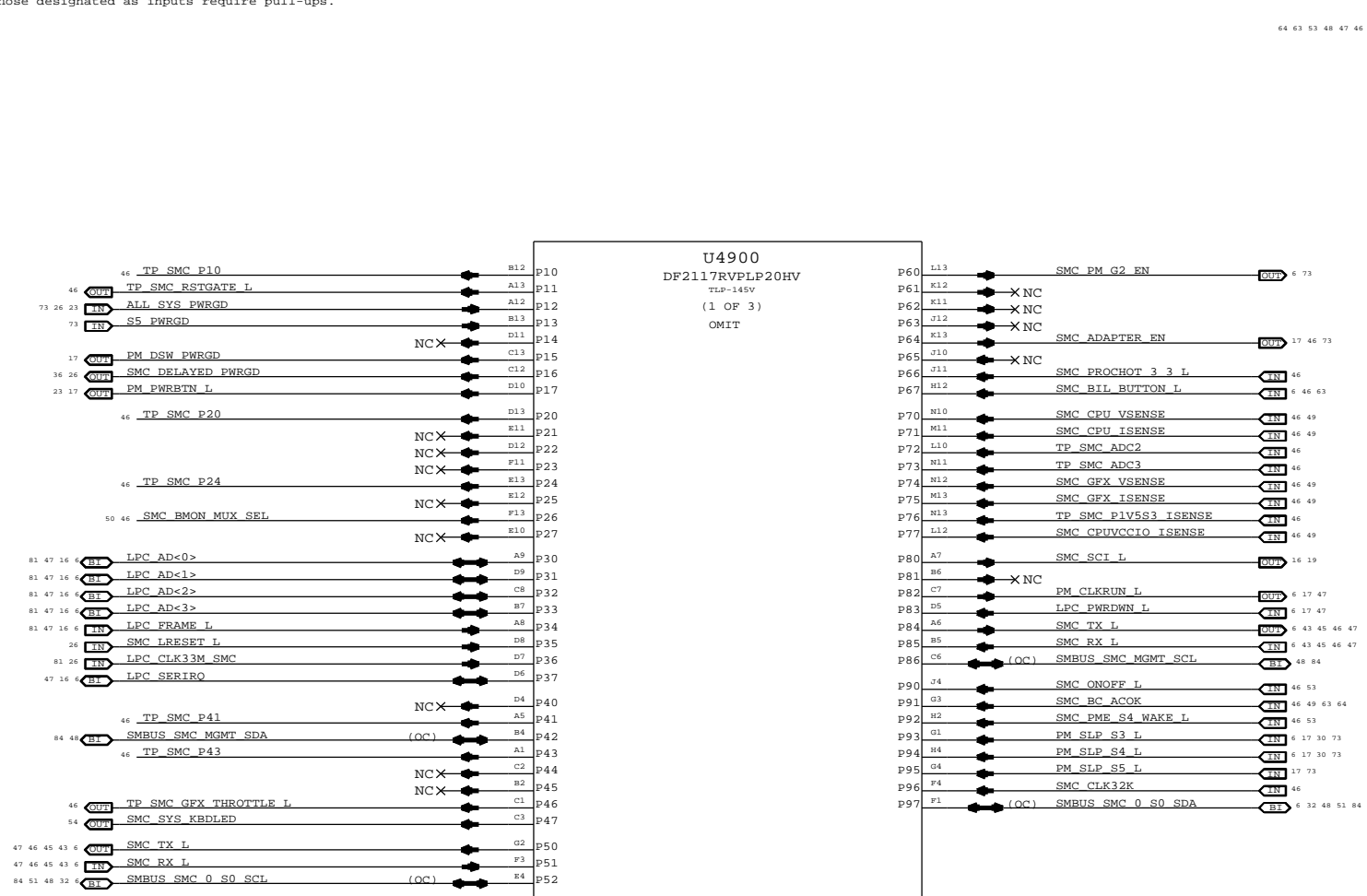
SYNC MASTER=K91_MLB		SYNC DATE=06/01/2011	
External USB Connectors			
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IR SUPPORT

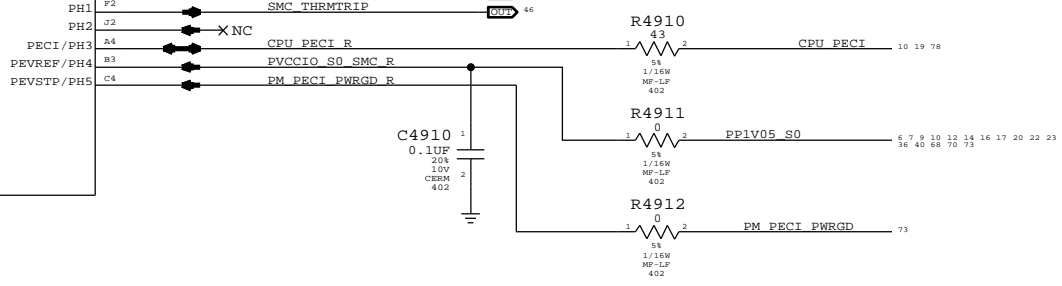


SYNC MASTER=K91_MLB		SYNC DATE=05/15/2010	
PAGE TITLE Front Flex Support			
DRAWING NUMBER		SIZE	
		D	
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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

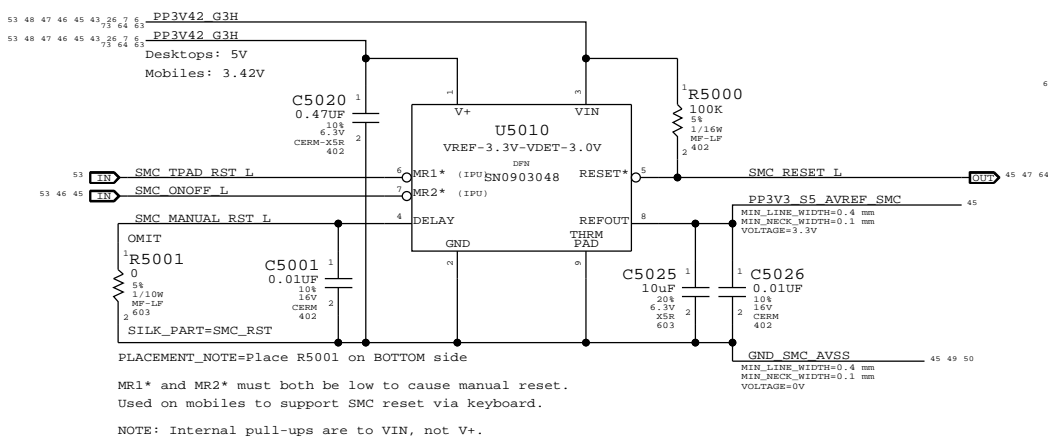


NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

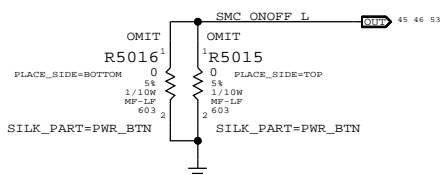


SYNC MASTER=LINDA_K901		SYNC DATE=07/07/2011	
PAGE TITLE		SMC	
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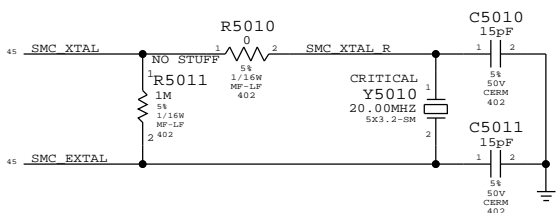
SMC Reset "Button", Supervisor & AVREF Supply



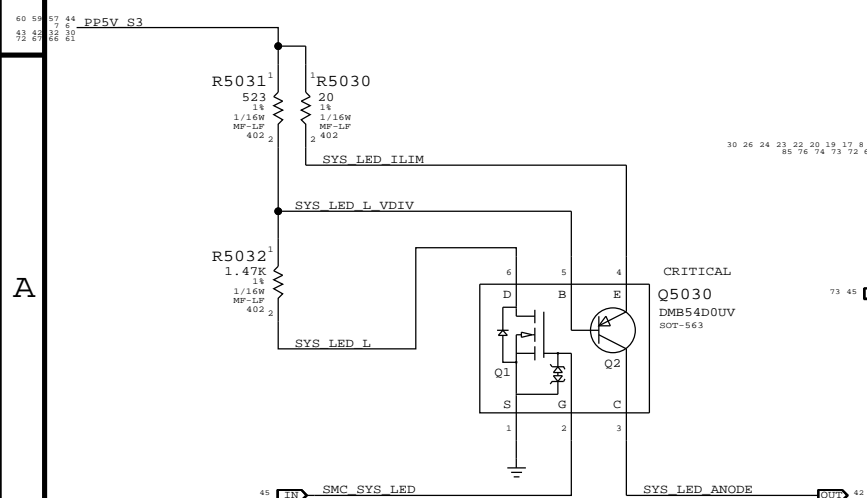
Debug Power "Buttons"



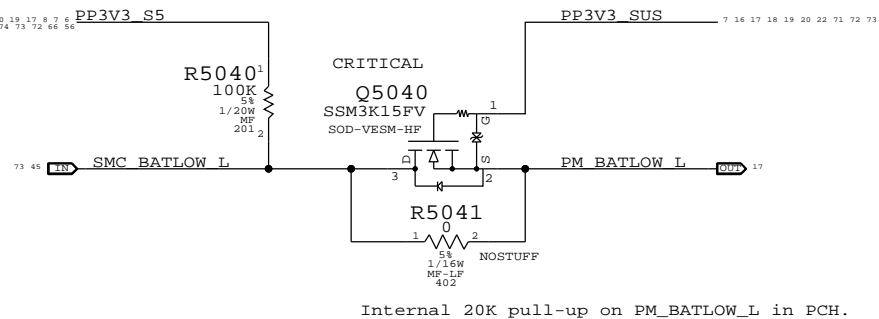
SMC Crystal Circuit



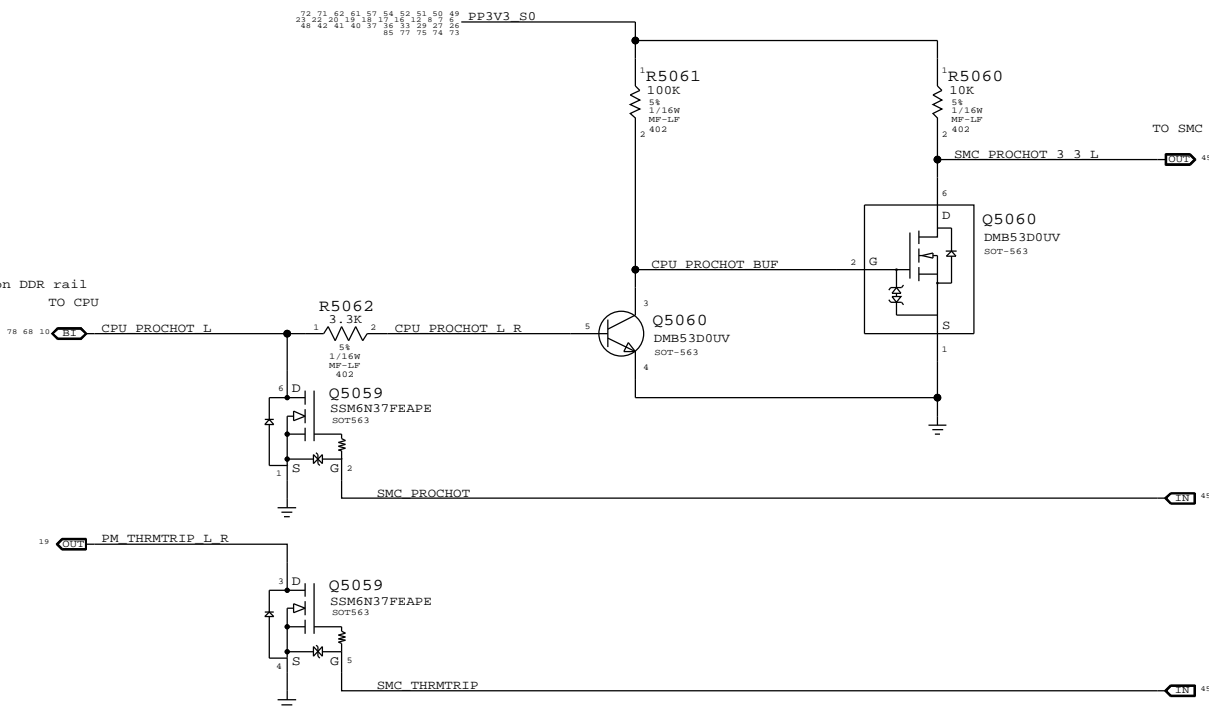
System (Sleep) LED Circuit



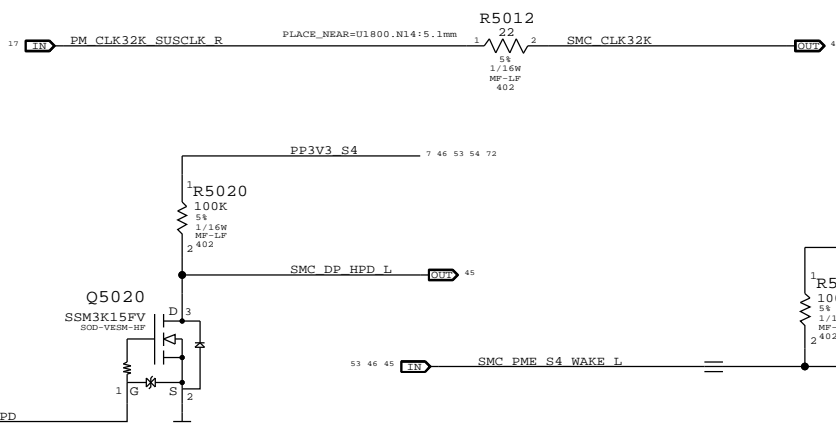
BATLOW# Isolation



SMC FSB to 3.3V Level Shifting



45 45	NC SMC FAN 2 CTL	==	NC SMC FAN 2 CTL	45 45
45 45	NC SMC FAN 2 TACH	==	NC SMC FAN 2 TACH	45 45
45 45	NC SMC FAN 3 CTL	==	NC SMC FAN 3 CTL	45 45
45 45	NC SMC FAN 3 TACH	==	NC SMC FAN 3 TACH	45 45
64 63 49 46 45	SMC BC ACOK	==	SMC BC ACOK	45 46 49 63 64
55 45 45	SMC INT L	==	SMC INT L	45 45 55
49 45 45	SMC CPU VSENSE	==	SMC CPU VSENSE	45 46 49
49 45 45	SMC CPU ISENSE	==	SMC CPU ISENSE	45 46 49
49 45 45	SMC GFX VSENSE	==	SMC GFX VSENSE	45 46 49
49 45 45	SMC GFX ISENSE	==	SMC GFX ISENSE	45 46 49
49 45 45	TP SMC P1V5S3 ISENSE	==	TP SMC P1V5S3 ISENSE	45 46 49
49 45 45	SMC CPUVCCIO ISENSE	==	SMC CPUVCCIO ISENSE	45 46 49
49 45 45	TP SMC SA ISENSE	==	TP SMC SA ISENSE	45 46 49
49 45 45	SMC DCIN VSENSE	==	SMC DCIN VSENSE	45 46 49
50 45 45	SMC DCIN ISENSE	==	SMC DCIN ISENSE	45 46 50
49 45 45	SMC PBUS VSENSE	==	SMC PBUS VSENSE	45 46 49
49 45 45	SMC BMON ISENSE	==	SMC BMON ISENSE	45 46 50
49 45 45	SMC CPU HI ISENSE	==	SMC CPU HI ISENSE	45 46 50
50 45 45	SMC OTHER HI ISENSE	==	SMC OTHER HI ISENSE	45 46 50
49 45 45	TP SMC P10	==	TP SMC P10	45 46 49
49 45 45	TP SMC P20	==	TP SMC P20	45 46 49
49 45 45	TP SMC P24	==	TP SMC P24	45 46 49
49 45 45	SMC BMON MUX SEL	==	SMC BMON MUX SEL	45 46 50
49 45 45	TP SMC P41	==	TP SMC P41	45 46 49
49 45 45	TP SMC P43	==	TP SMC P43	45 46 49
49 45 45	TP SMC PF5	==	TP SMC PF5	45 46 49
49 45 45	TP SMC RSTGATE L	==	TP SMC RSTGATE L	45 46 49



53 46 45	SMC ONOFF L	R5070	10K	1	54	1/16W	MP-LF	402
45	G3 POWERON L	R5072	10K	1	54	1/16W	MP-LF	402
63 53 45	SMC LID	R5071	100K	1	54	1/16W	MP-LF	402
47 45 43 6	SMC TX L	R5073	10K	1	54	1/16W	MP-LF	402
47 45 43 6	SMC RX L	R5074	100K	1	54	1/16W	MP-LF	402
47 45 43 6	SMC TMS	R5077	10K	1	54	1/16W	MP-LF	402
47 45 43 6	SMC TDO	R5078	10K	1	54	1/16W	MP-LF	402
47 45 43 6	SMC TDI	R5079	10K	1	54	1/16W	MP-LF	402
47 45 43 6	SMC TCK	R5080	10K	1	54	1/16W	MP-LF	402
63 45 43 6	SMC BIL BUTTON L	R5081	10K	1	54	1/16W	MP-LF	402
64 63 49 46 45	SMC BC ACOK	R5087	470K	1	54	1/16W	MP-LF	402
55 46 45	SMC INT L	R5093	10K	1	54	1/16W	MP-LF	402
45	SMC PA0 PU	R5091	100K	1	54	1/16W	MP-LF	402
45 19	SMC RUNTIME SCT L	R5094	100K	1	54	1/16W	MP-LF	402
73 45 17	SMC ADAPTER EN	R5085	10K	1	54	1/16W	MP-LF	402
45	SMC CASE OPEN	R5086	10K	1	54	1/16W	MP-LF	402
45	SMC PB4	R5088	10K	1	54	1/16W	MP-LF	402
76 73 45 8	SMC S4 WAKESRC EN	R5090	100K	1	54	1/16W	MP-LF	402
45 32	WIFI_EVENT L	R5089	10K	1	54	1/16W	MP-LF	402

Below connections are different from K91

45 45	NC SMC FAN 1 CTL	==	NC SMC FAN 1 CTL	45 45				
45 45	NC SMC FAN 1 TACH	==	NC SMC FAN 1 TACH	45 45				
45 45	TP SMC ADC2	==	TP SMC ADC2	45 45				
45 45	TP SMC ADC3	==	TP SMC ADC3	45 45				
45 45	TP SMC ADC14	==	TP SMC ADC14	45 45				
45 45	TP SMC GFX THROTTLE L	==	TP SMC GFX THROTTLE L	45 45				
45	SMC GFX OVERTEMP L	R5095	10K	1	54	1/16W	MP-LF	402

SMC Support

Apple Inc.

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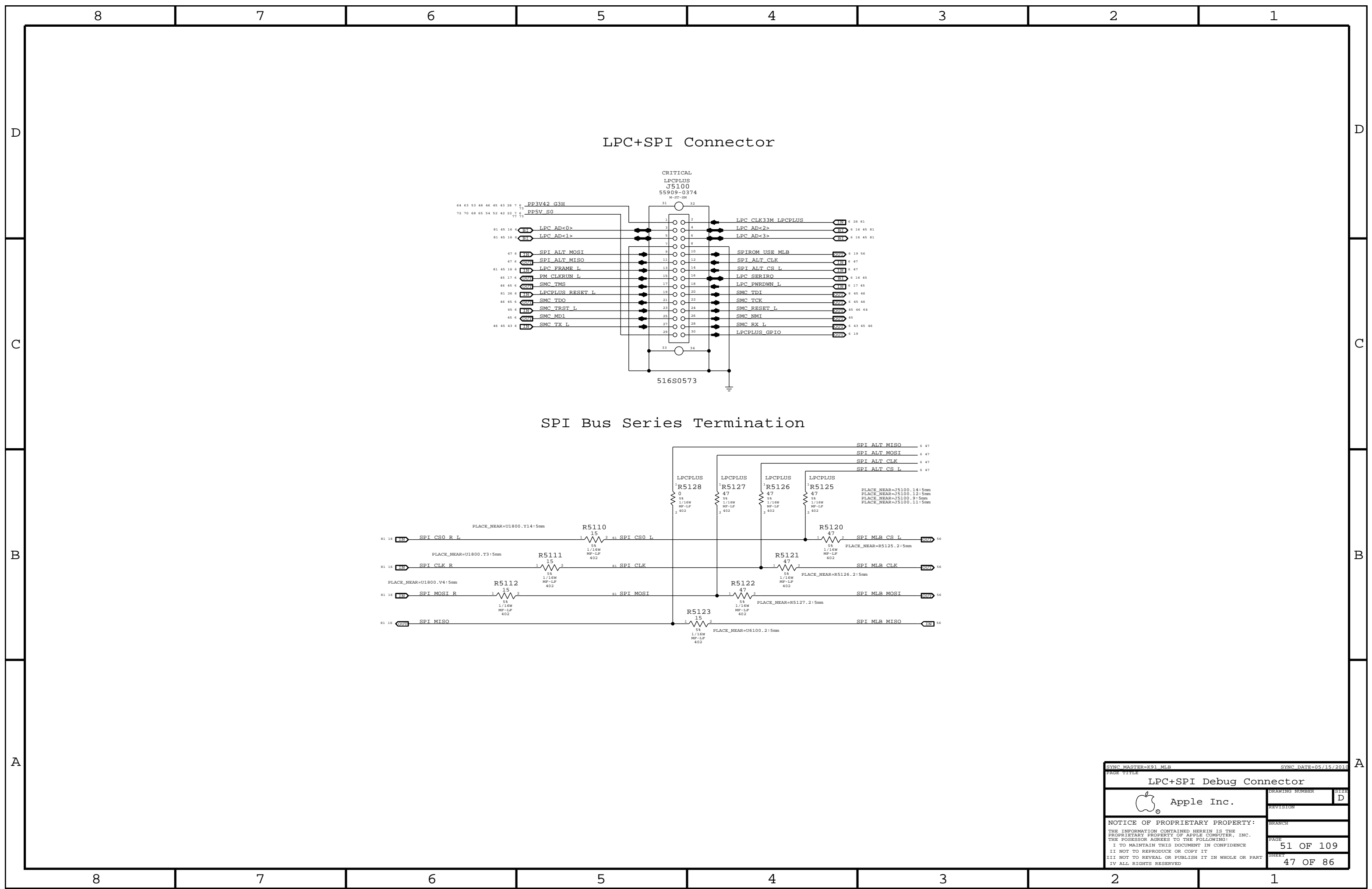
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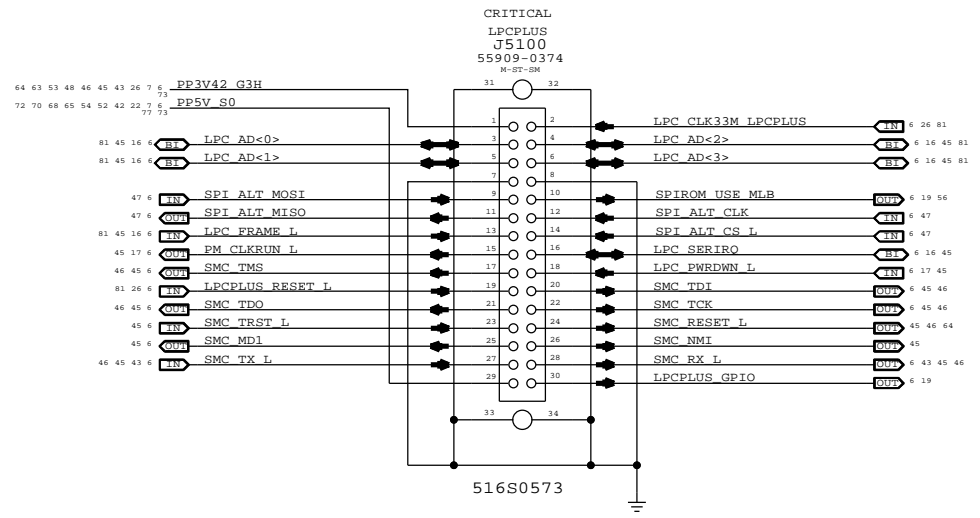
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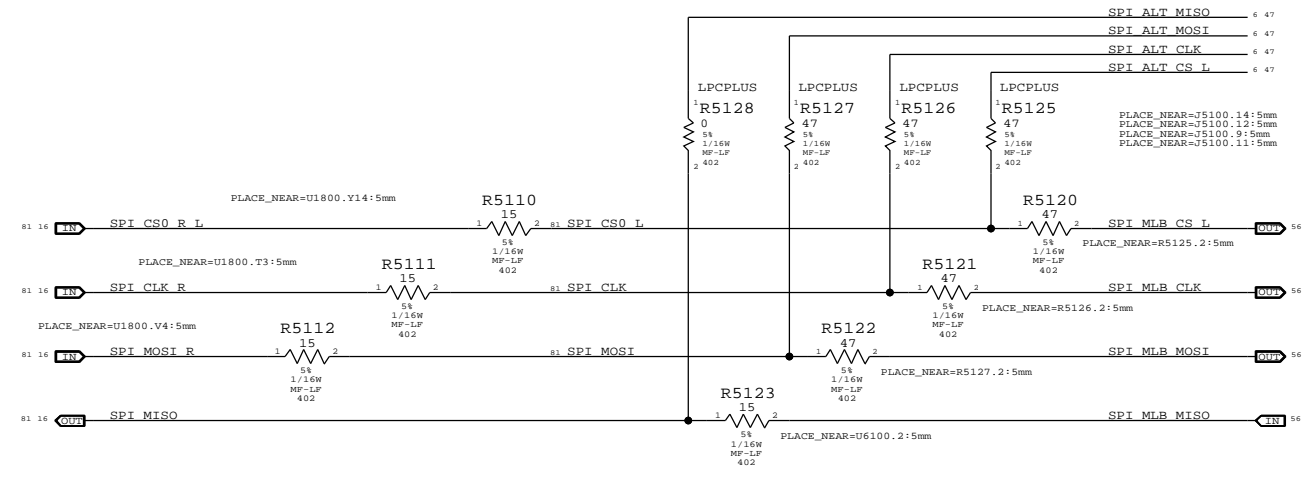
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REVISION	D
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LPC+SPI Connector



SPI Bus Series Termination



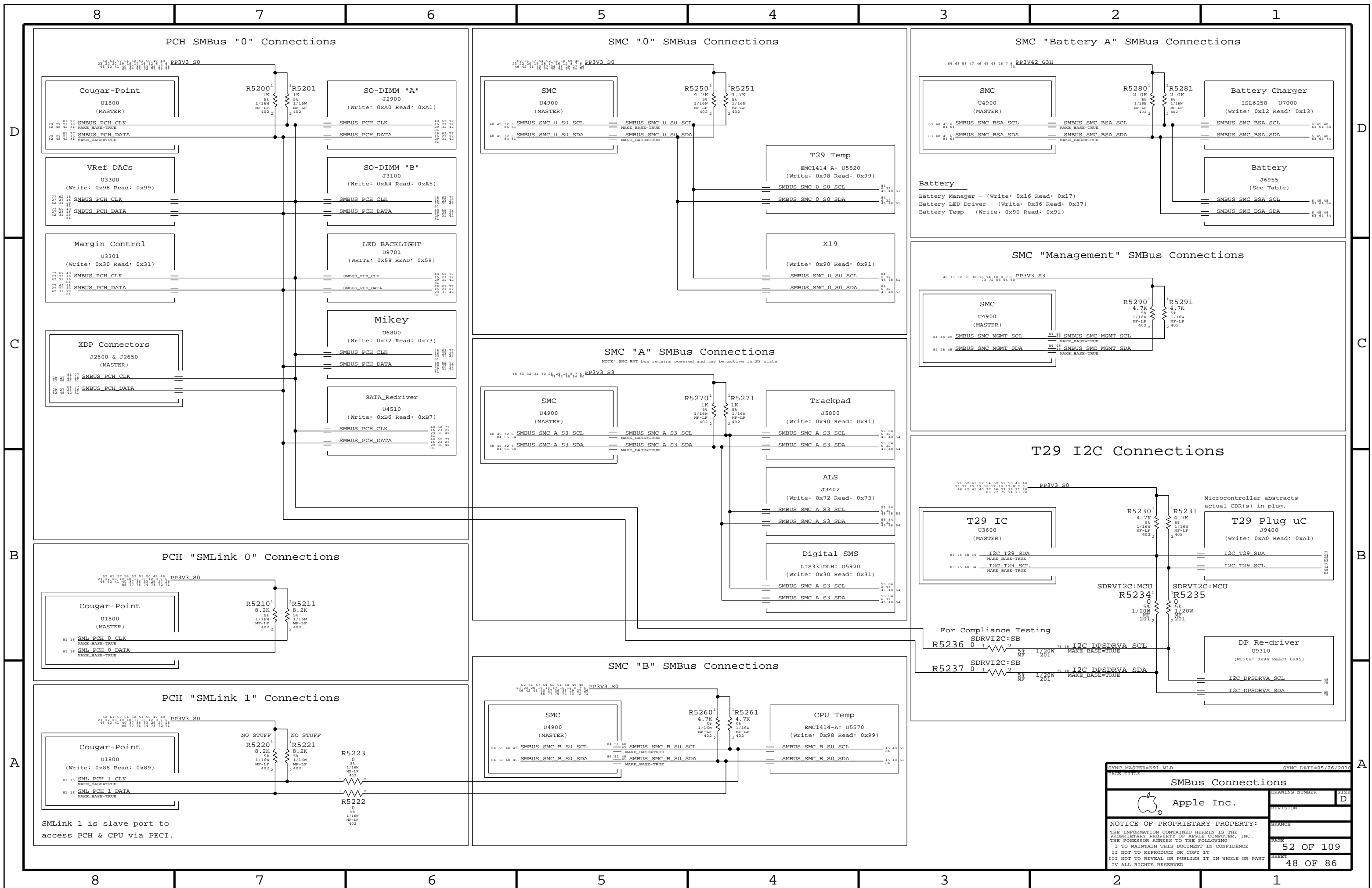
SYNC MASTER=K91 MLB SYNC DATE=05/15/2011

LPC+SPI Debug Connector

Apple Inc.

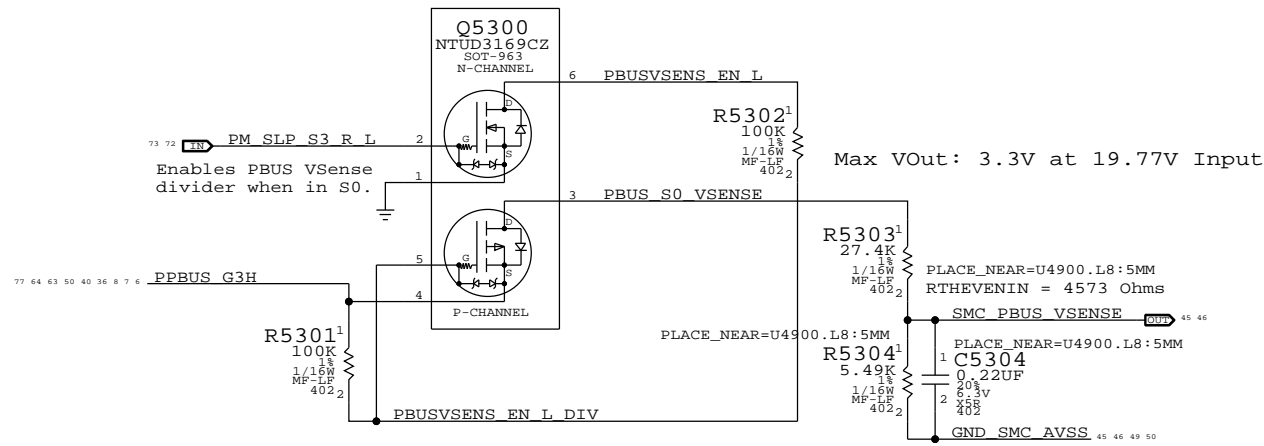
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REVISION	D
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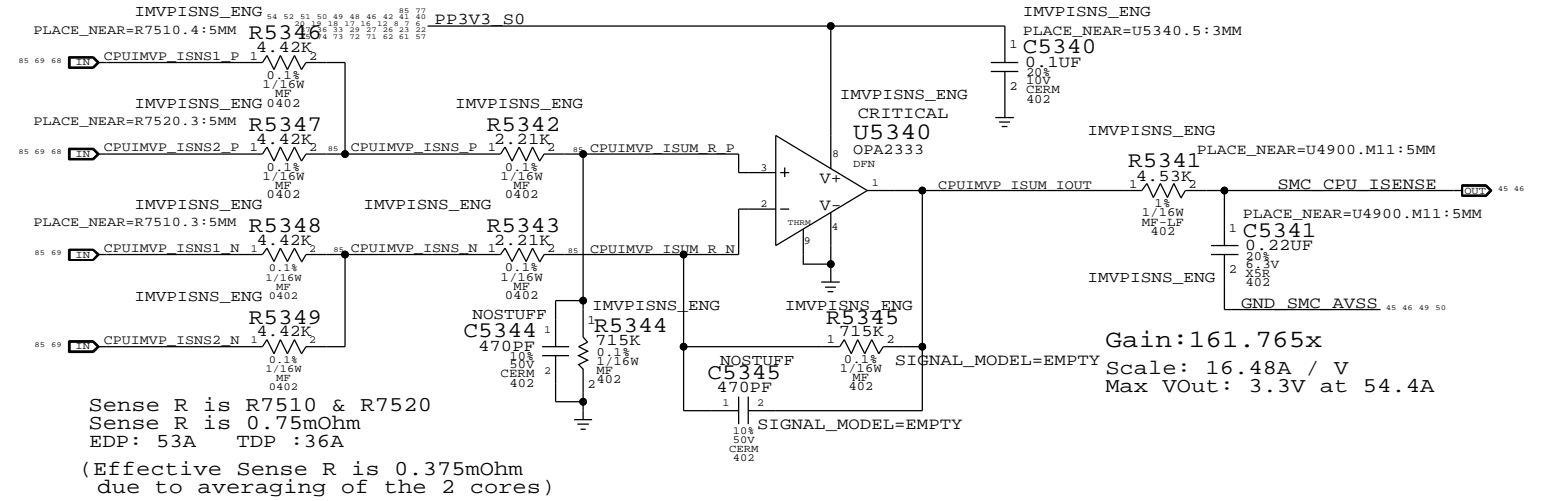


SYNC MASTER=K91_MLB		SYNC DATE=05/26/2011	
PAGE TITLE			
SMBus Connections			SIZE
Apple Inc.			D
DRAWING NUMBER			REVISION
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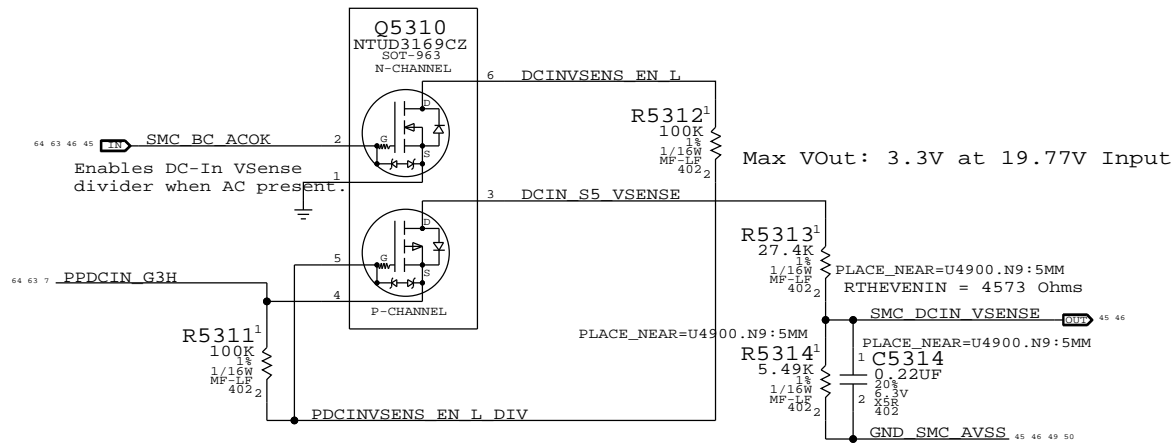
PBUS Voltage Sense Enable & Filter



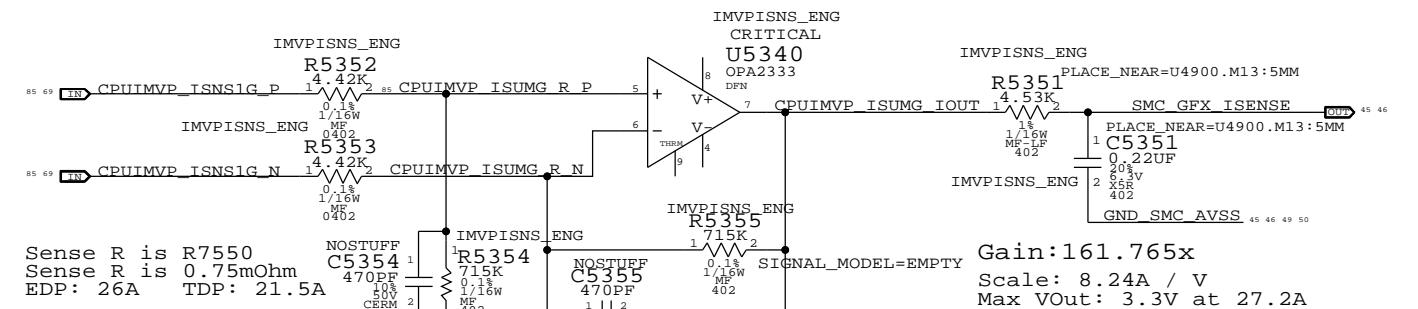
CPU VCore Load Side Current Sense / Filter



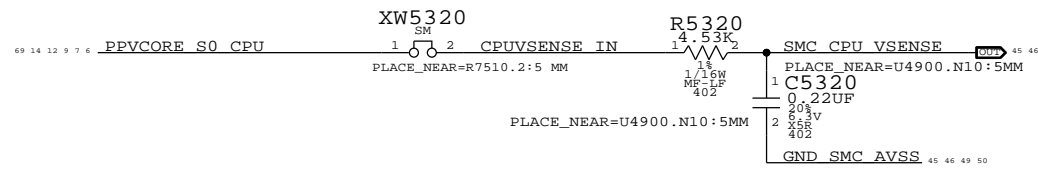
DC-In Voltage Sense Enable & Filter



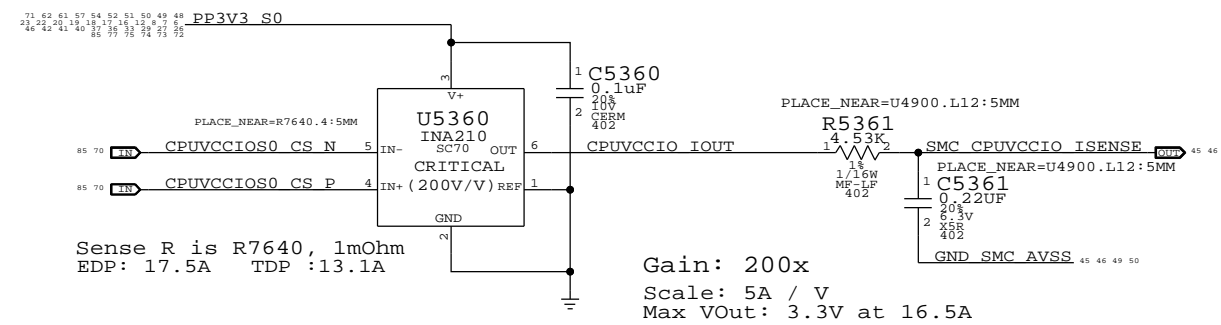
GFX/IG VCore Load Side Current Sense / Filter



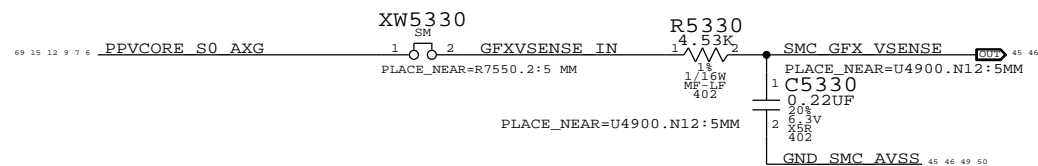
CPU Vcore Voltage Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter

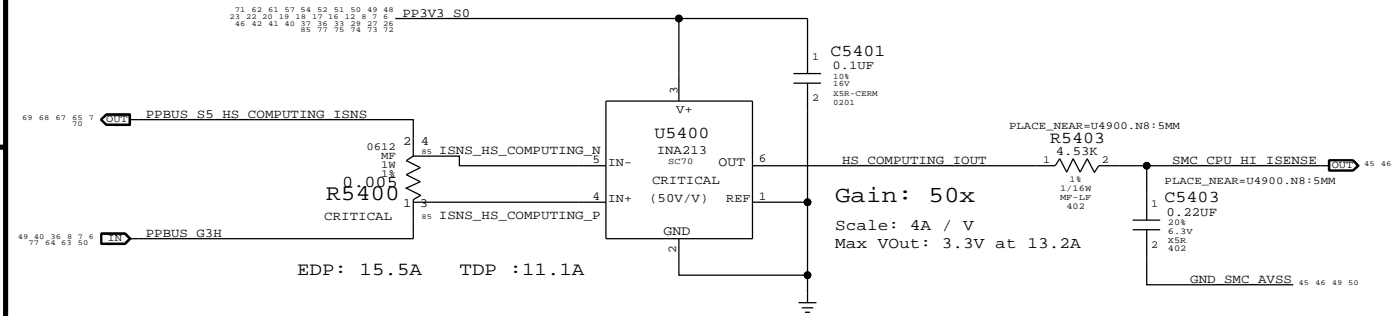


GFX/IG Vcore Voltage Sense / Filter

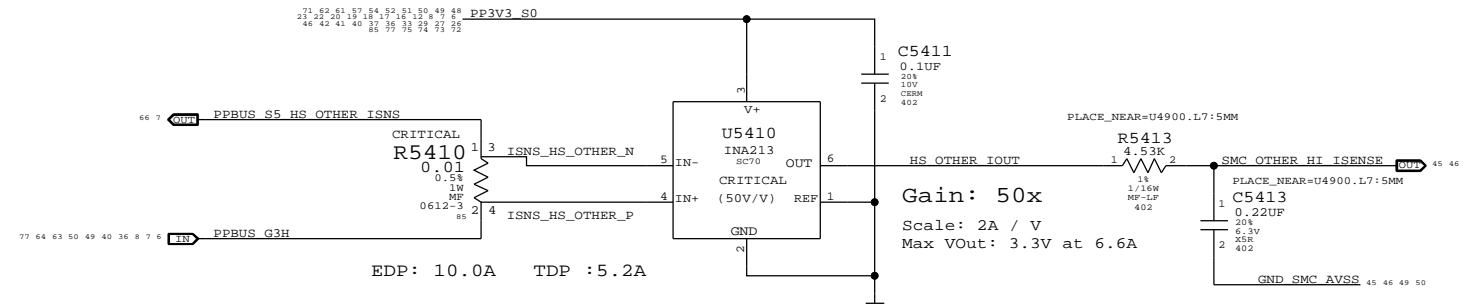


SYNC MASTER=LINDA K90I		SYNC DATE=10/22/2010	
Voltage & Load Side Current Sensing			
Apple Inc.		DRAWING NUMBER	SIZE
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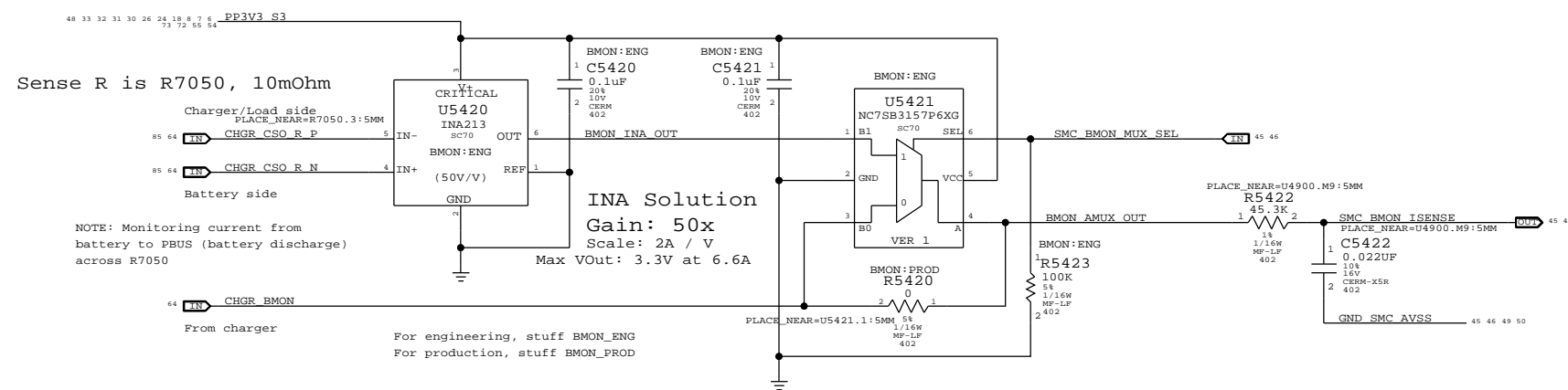
COMPUTING High Side Current Sense / Filter



OTHER High Side Current Sense / Filter



CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter

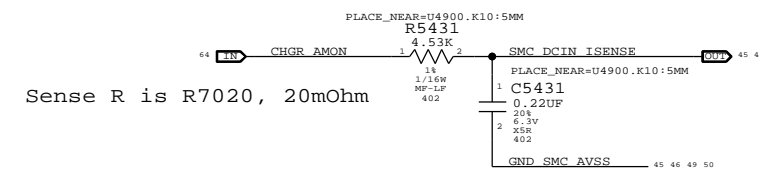


Sense R is R7050, 10mOhm

INA Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A

DC-IN (AMON) Current Sense Filter



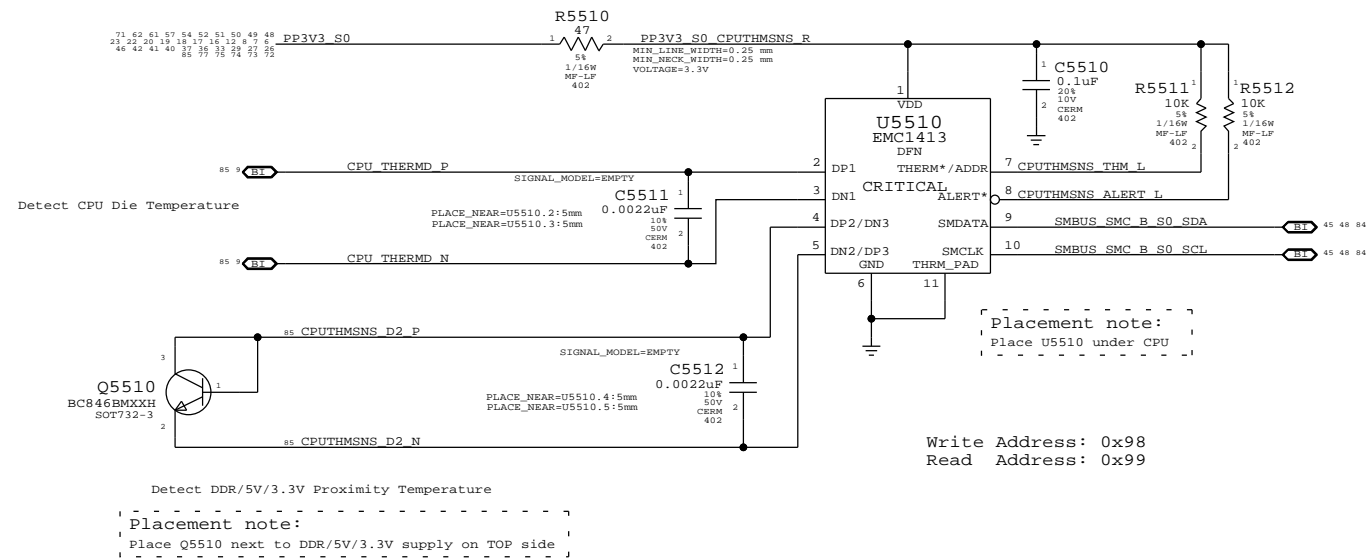
Sense R is R7020, 20mOhm

DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

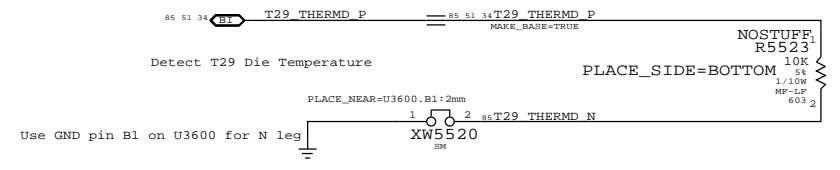
INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

SYNC MASTER=LINDA.K901		SYNC DATE=10/22/2011	
High Side Current Sensing			
Apple Inc.		DRAWING NUMBER	SIZE
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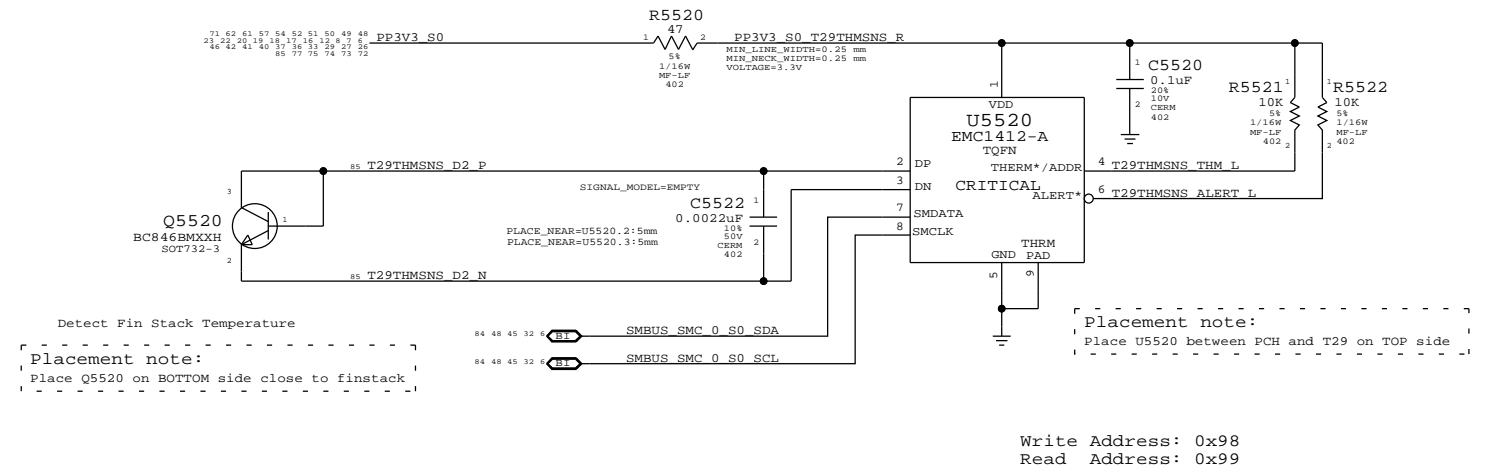
CPU Proximity/CPU Die/5V-3.3V Proximity



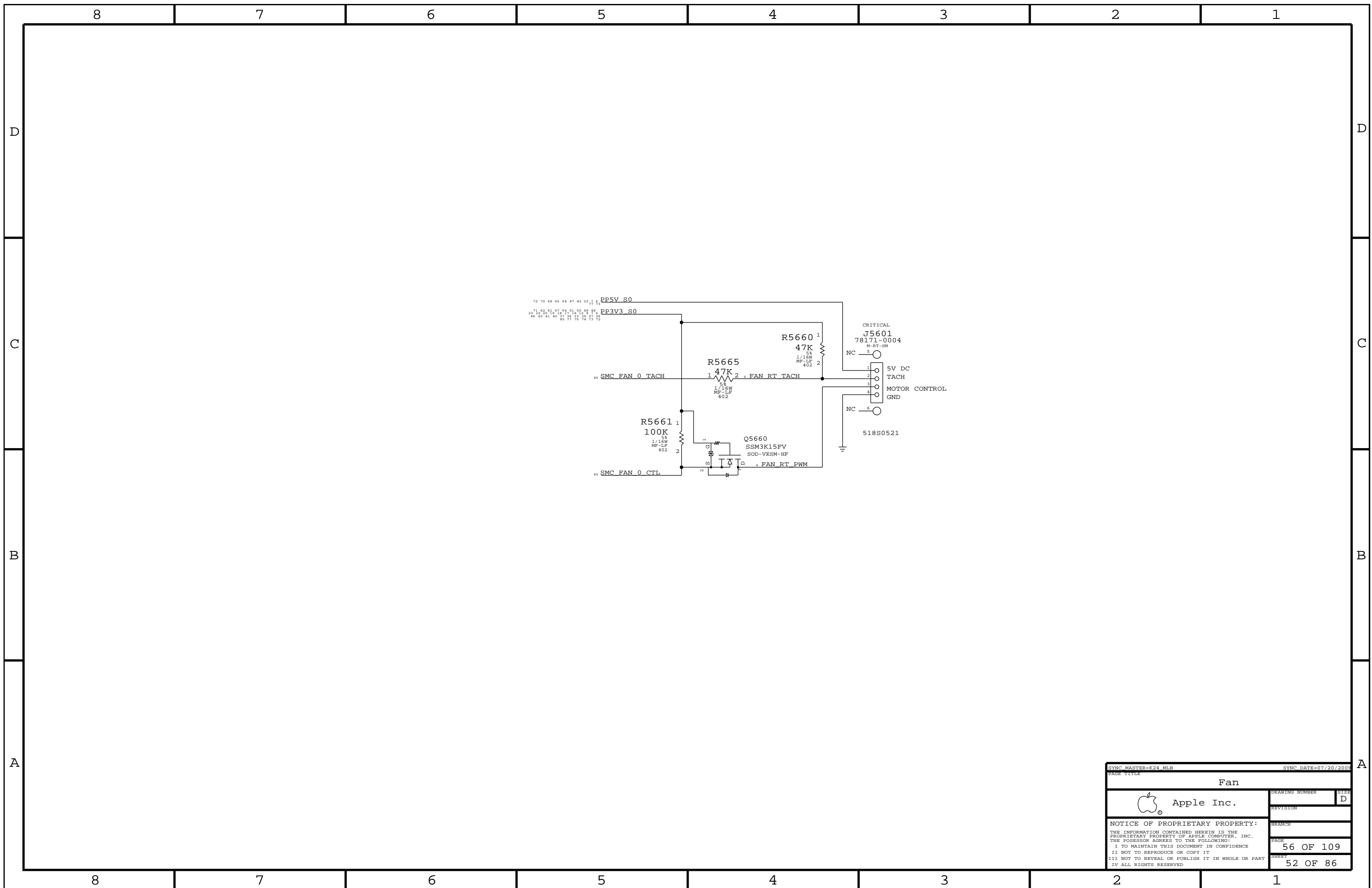
T29 Die



PCH-T29 Proximity/FinStack



SYNC MASTER=LINDA_K901		SYNC DATE=10/22/2011	
PAGE TITLE			
Thermal Sensors			SIZE
Apple Inc.			D
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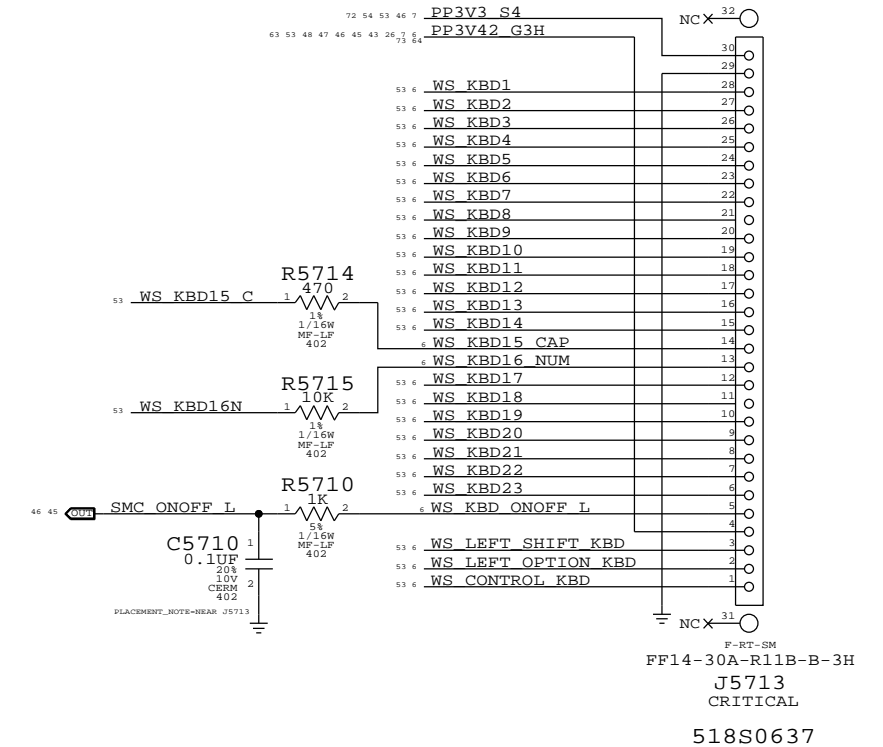
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PAGE TITLE Fan			
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PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

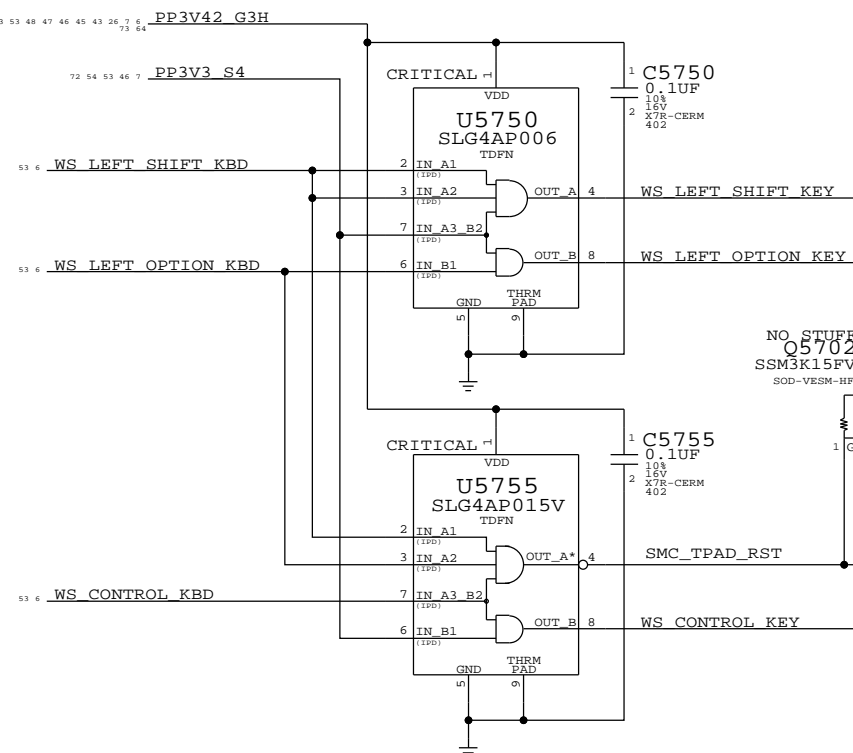
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
	80UA			0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	14MA (MAX)			0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

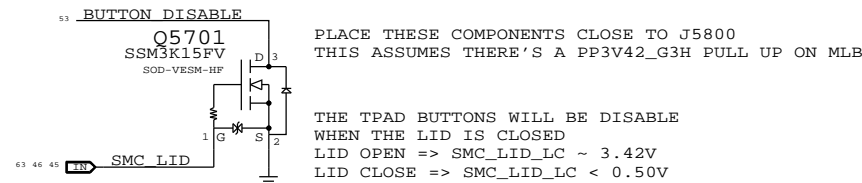


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.



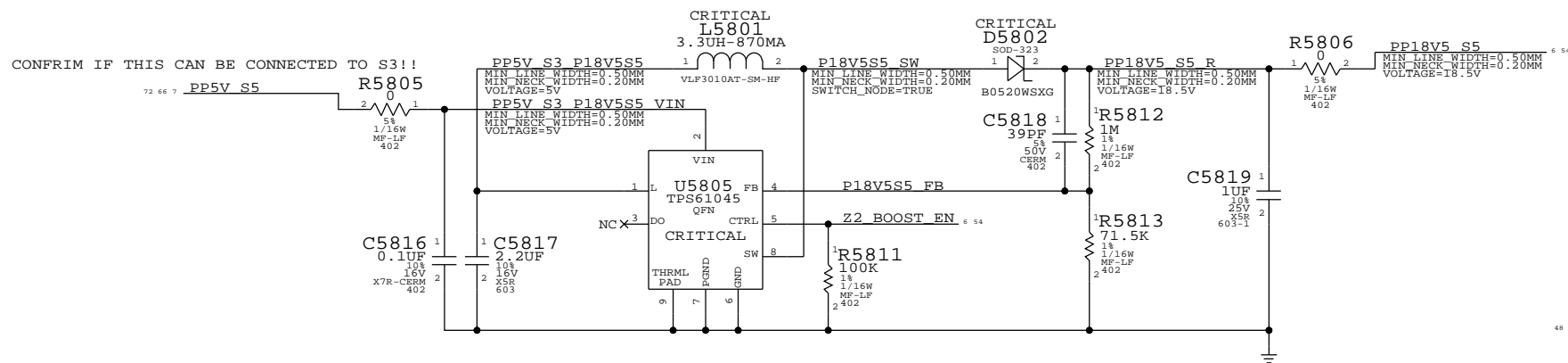
TPAD Buttons Disable



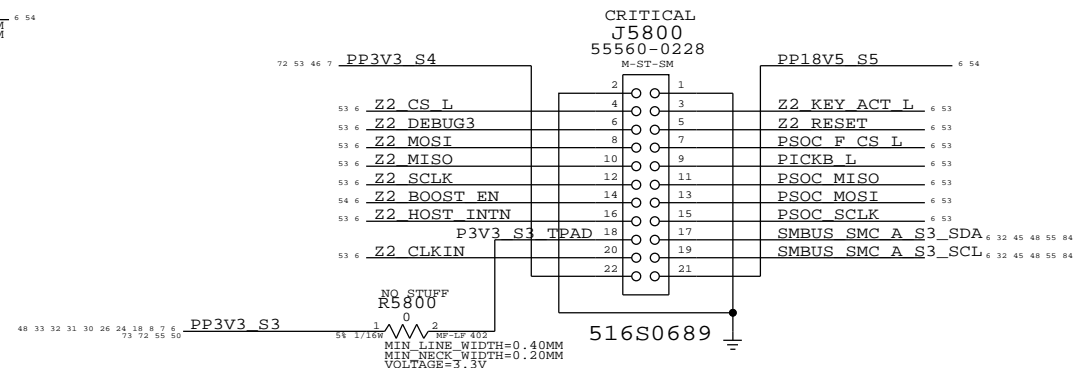
PAGE TITLE		SYNC DATE=07/12/2010	
WELLSPRING 1			
Apple Inc.		DRAWING NUMBER	SIZE
		REVISION	
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BOOSTER +18.5VDC FOR SENSORS

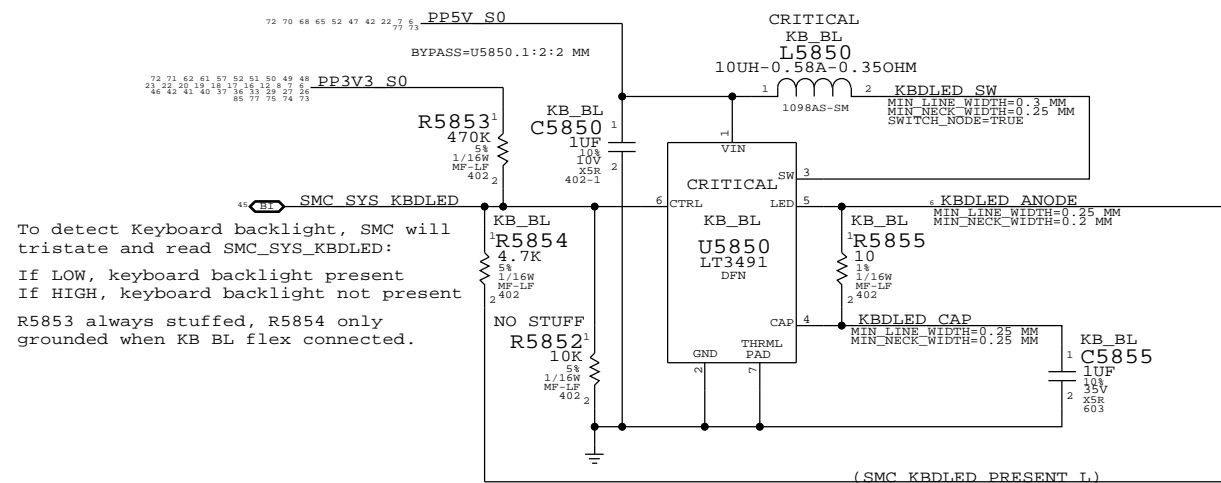
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED



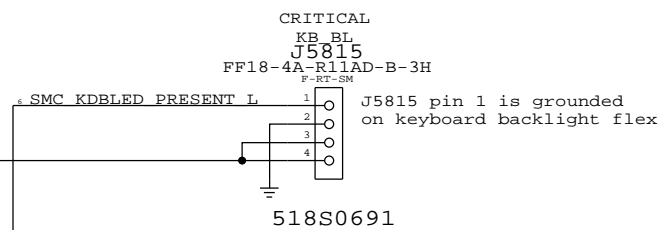
IPD Flex Connector



Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=LINDA K901		SYNC DATE=07/12/2010	
PAGE TITLE WELLSPRING 2			
Apple Inc.		DRAWING NUMBER	SIZE D
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		PAGE	58 OF 109
		SHEET	54 OF 86

D

D

C

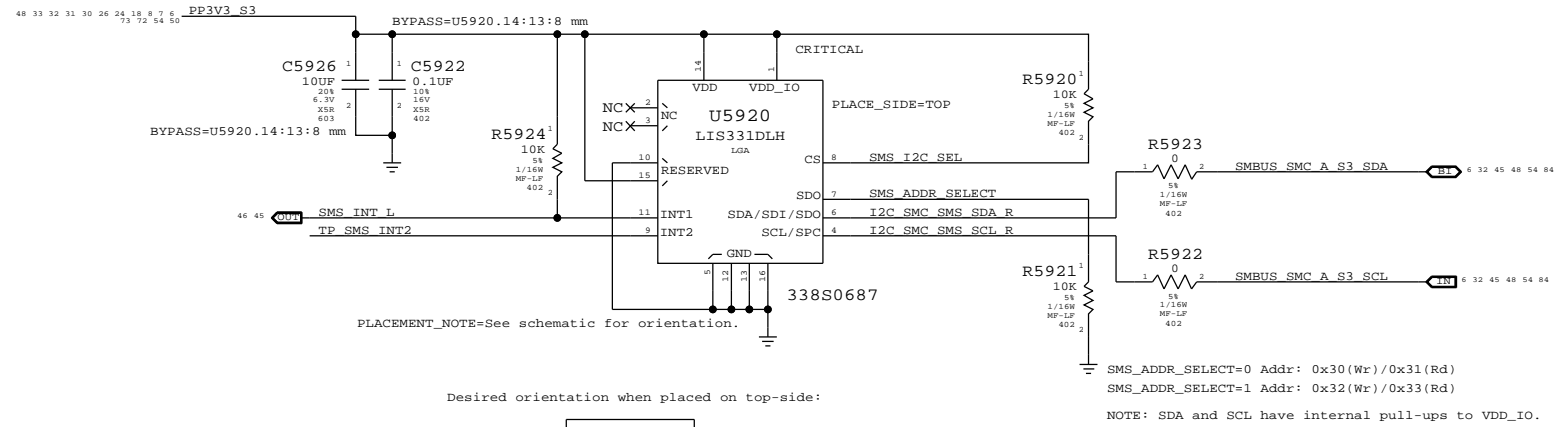
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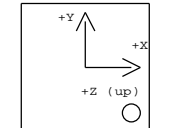
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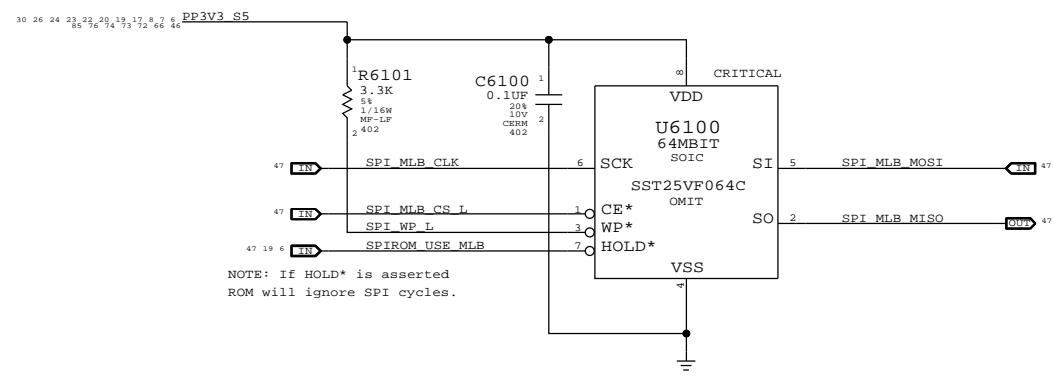


Desired orientation when placed on top-side:

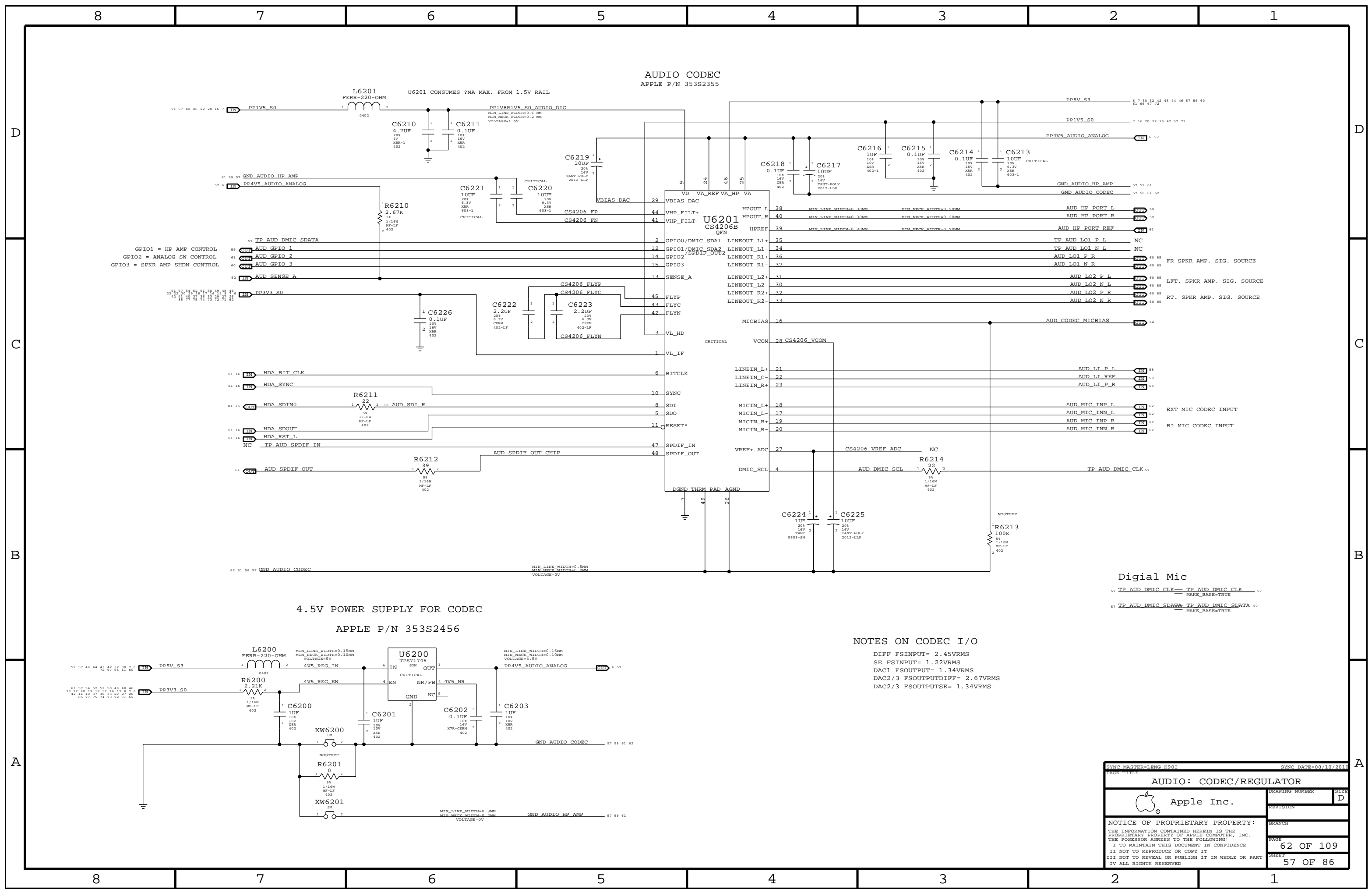


Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=LINDA_K901		SYNC DATE=07/08/2010	
Digital Accelerometer			
Apple Inc.		DRAWING NUMBER	SIZE
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SYNC MASTER=K91_MLB		SYNC DATE=05/15/2011	
PAGE TITLE SPI ROM			
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AUDIO CODEC
APPLE P/N 353S2355

4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456

NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

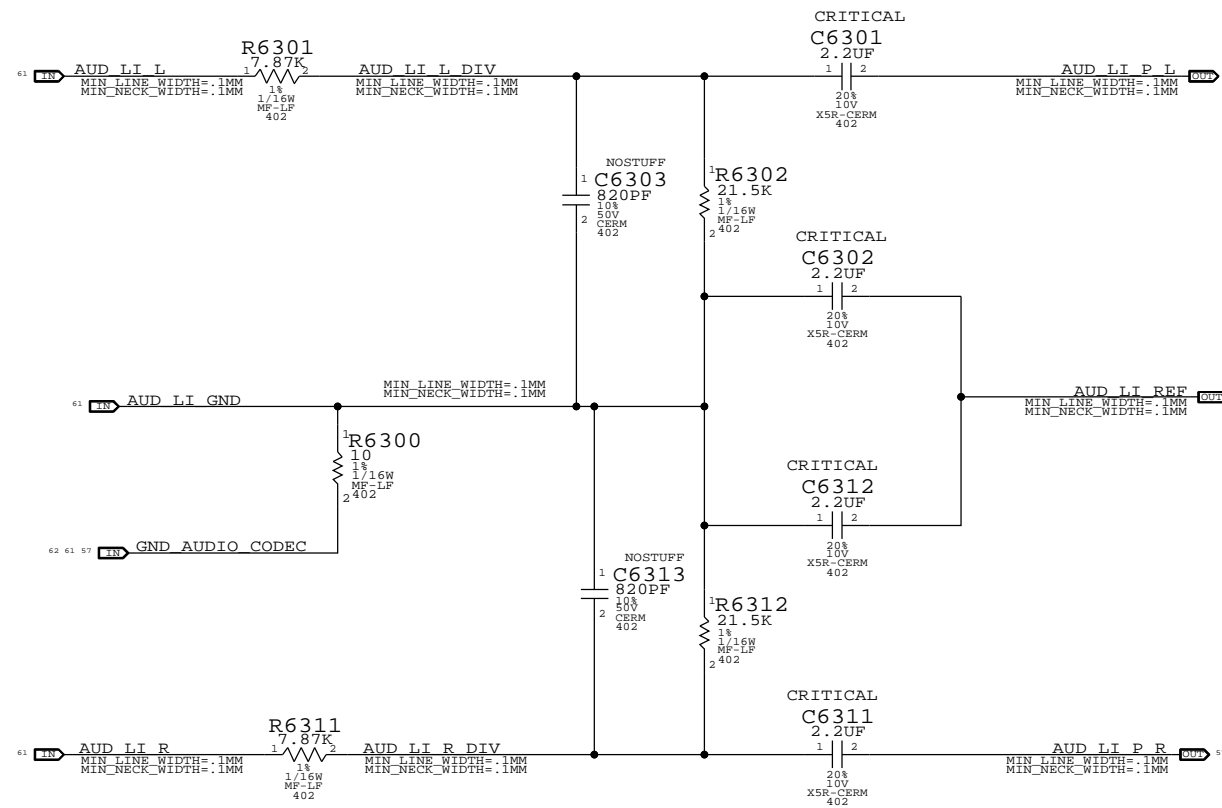
Digital Mic

57 TP AUD DMIC CLK TP AUD DMIC CLK 57
MAKE_BASE=TRUE
57 TP AUD DMIC SDATA TP AUD DMIC SDATA 57
MAKE_BASE=TRUE

SYNC MASTER=LENG K901		SYNC DATE=08/10/2011	
PAGE TITLE			
AUDIO: CODEC/REGULATOR		DRAWING NUMBER	SIZE
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LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
 NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
 FC_HP = 3.6 HZ
 FC_LP = 43KHZ
 VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE		DRAWING NUMBER		SIZE
AUDIO: LINE INPUT FILTER				D
Apple Inc.		REVISION		
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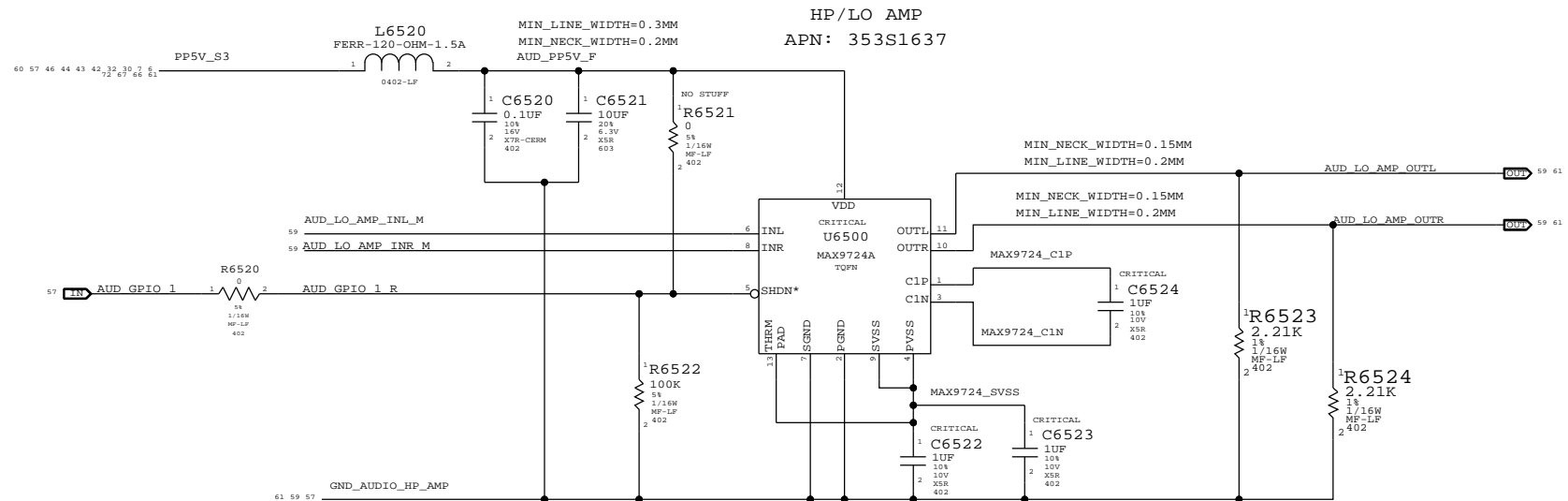
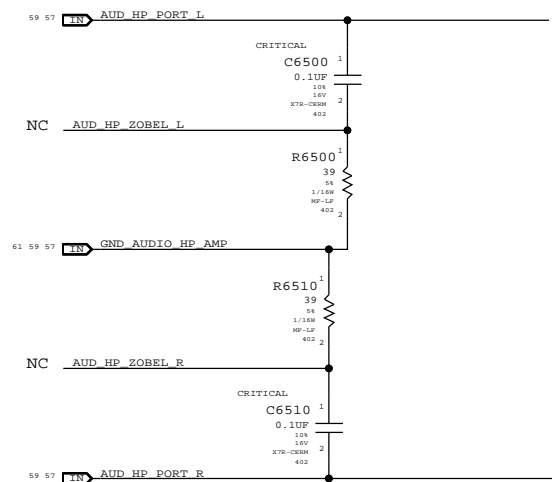
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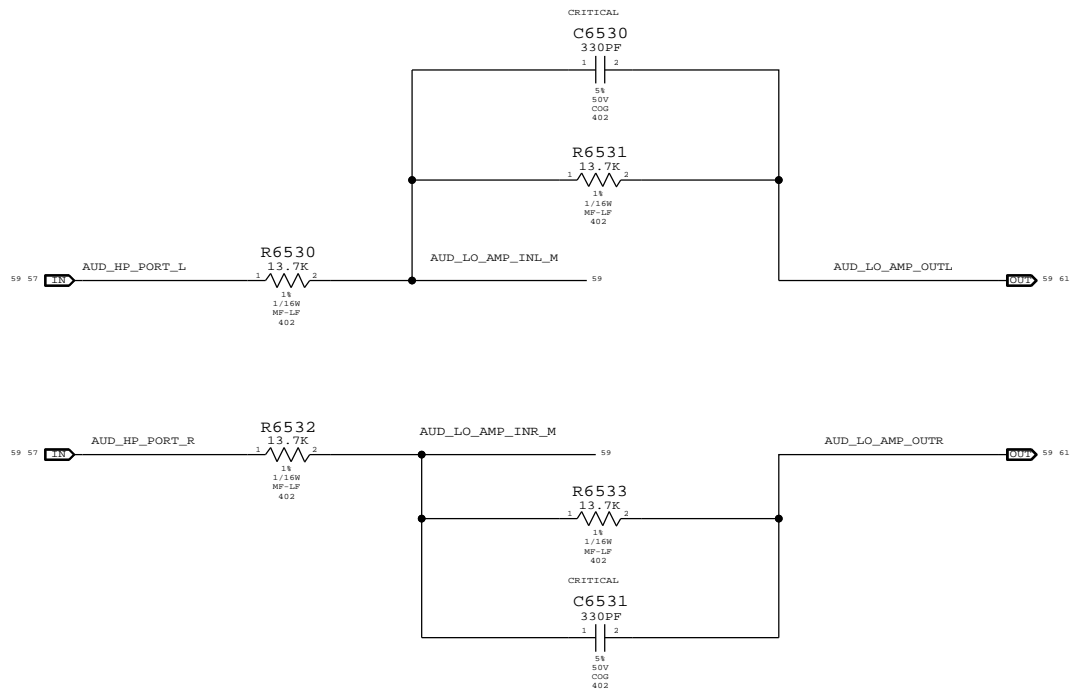
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC MASTER=LENG K901		SYNC DATE=08/10/2011	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
Apple Inc.		DRAWING NUMBER	SIZE
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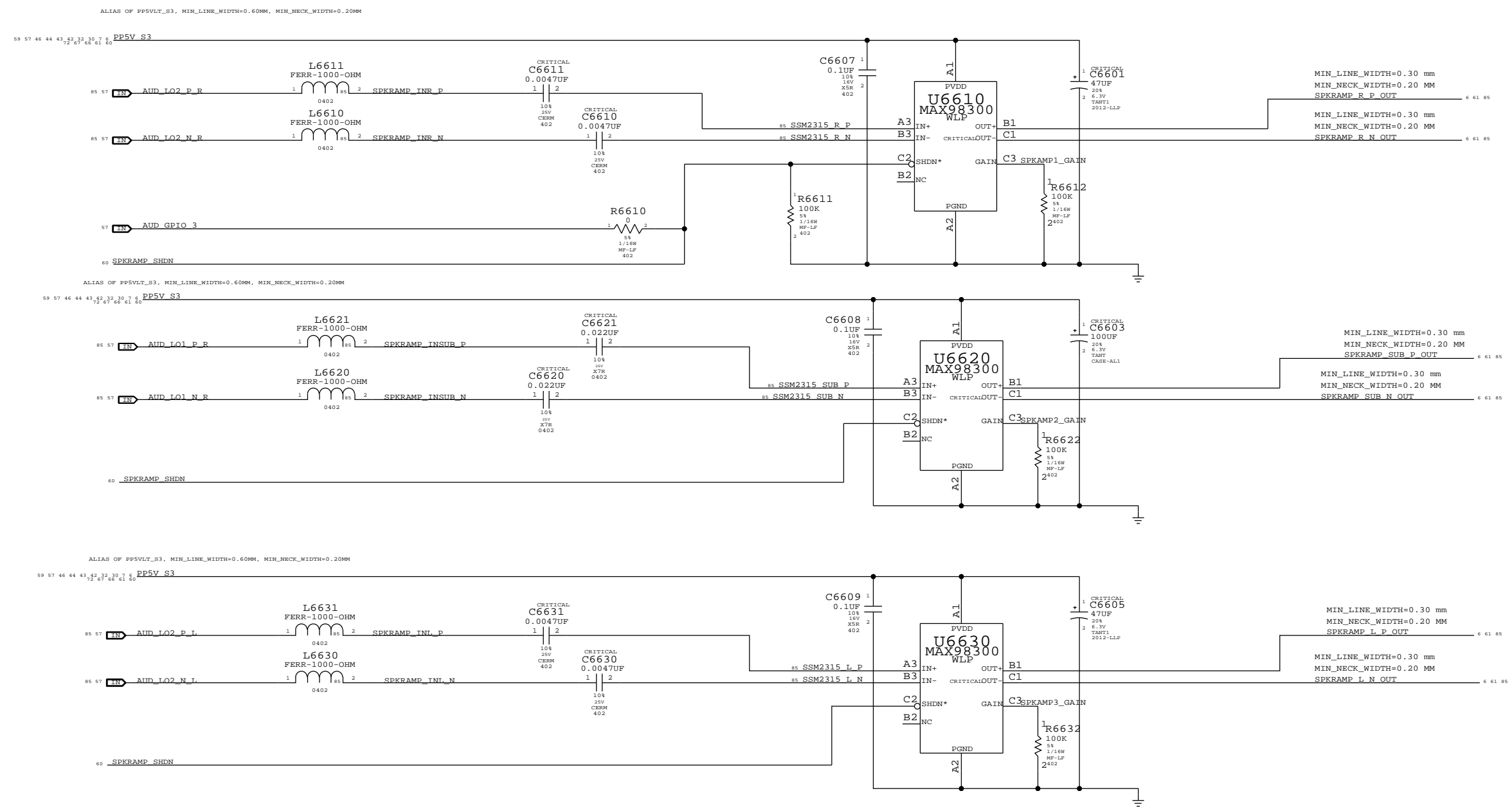
2

1

SATELLITE & SUB TWEETER AMPLIFIER

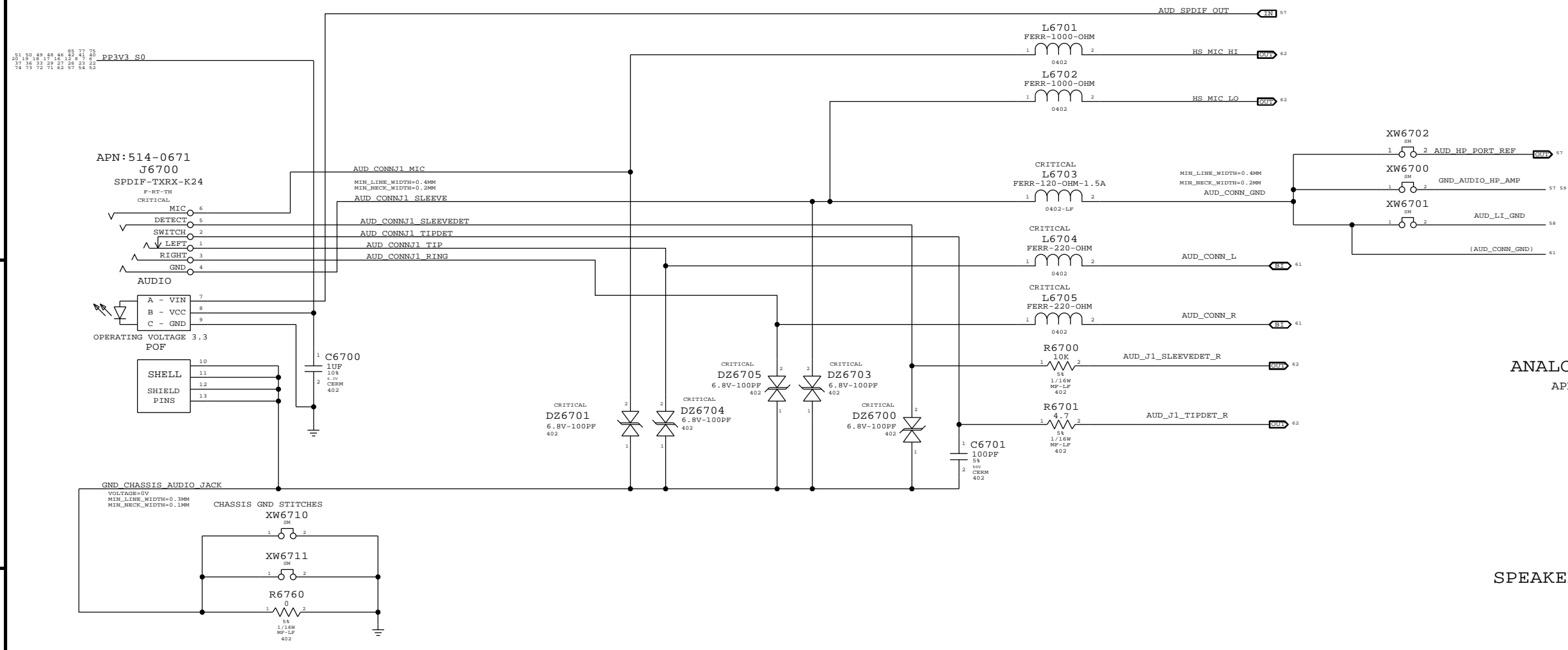
APN: 353S2888

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 3DB

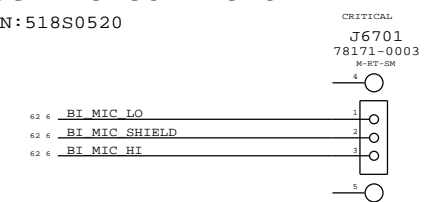


SYNC MASTER=LENG K901		SYNC DATE=08/10/2011	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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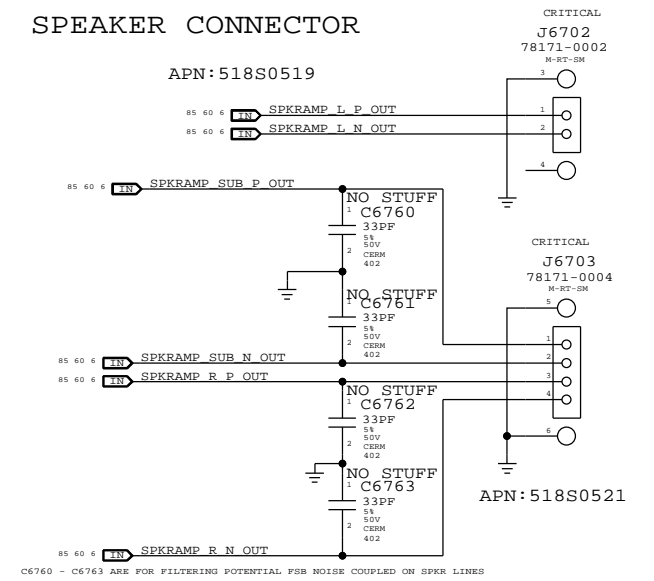
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



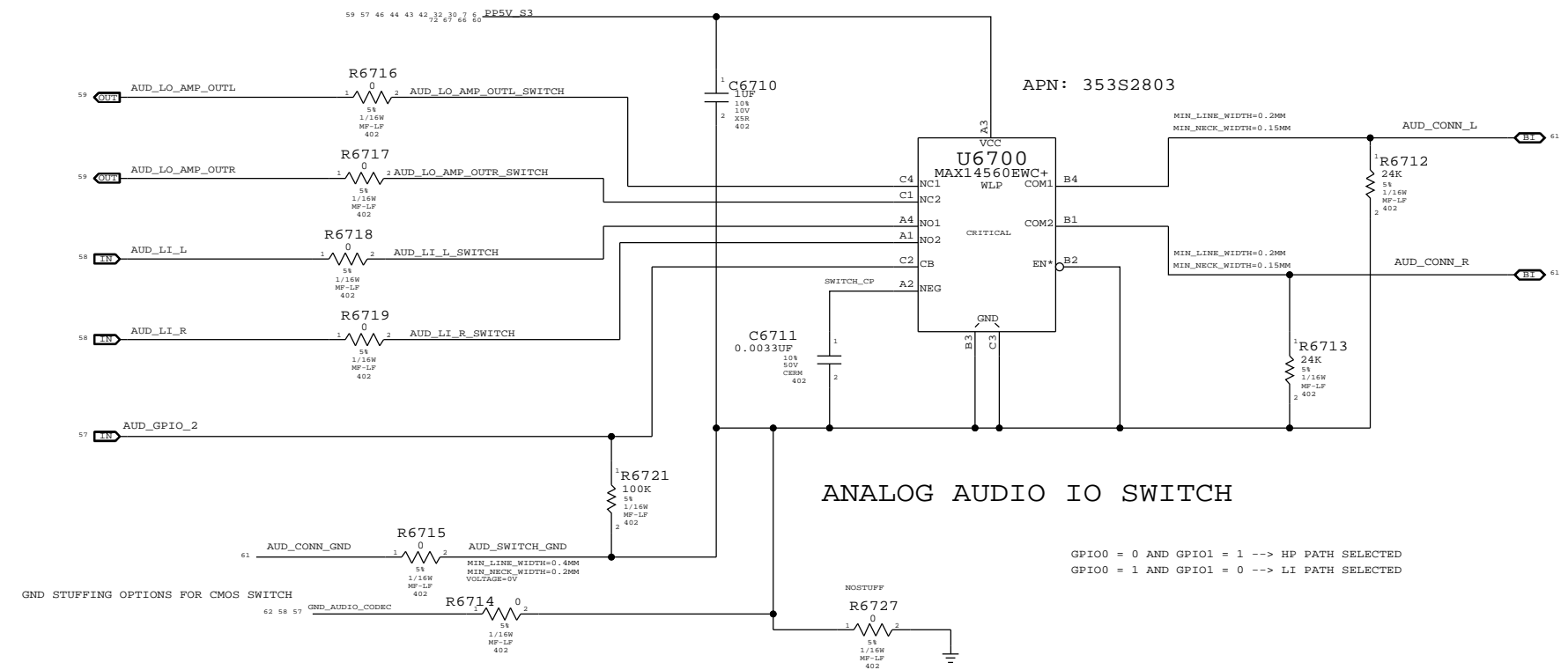
ANALOG MIC CONNECTOR
APN: 518S0520



SPEAKER CONNECTOR



ANALOG AUDIO IO SWITCH



SYNC MASTER=LENG K901		SYNC DATE=08/10/2011	
PAGE TITLE			
AUDIO: JACK			SIZE D
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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_2 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_2 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (3)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

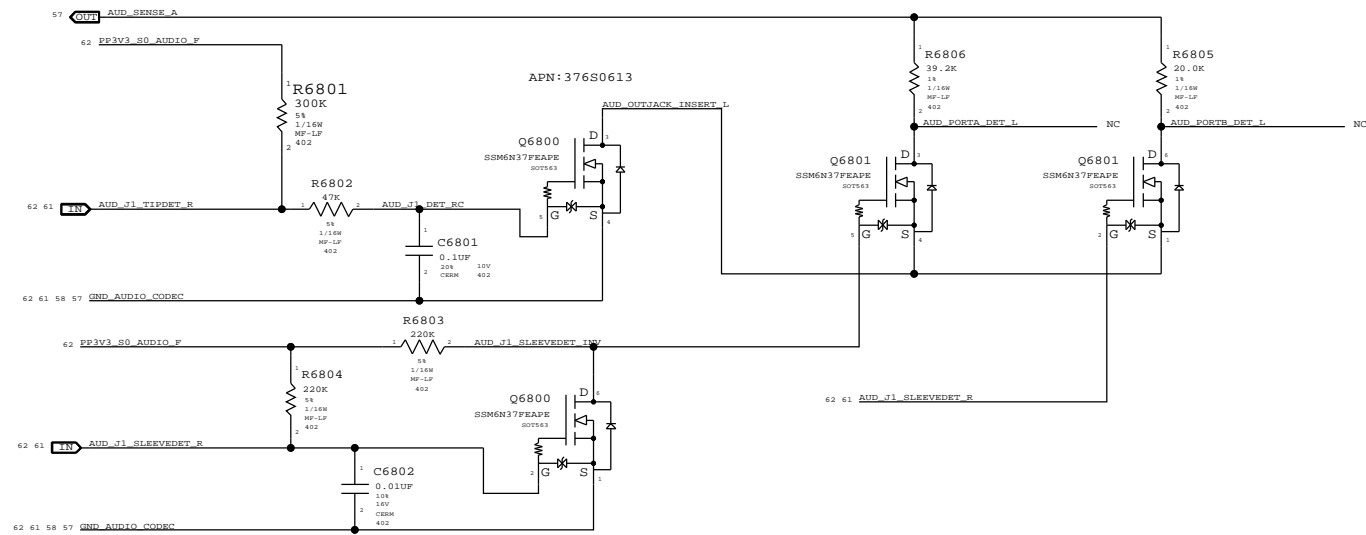
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80A)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SOUTHBRIDGE RESOURCES

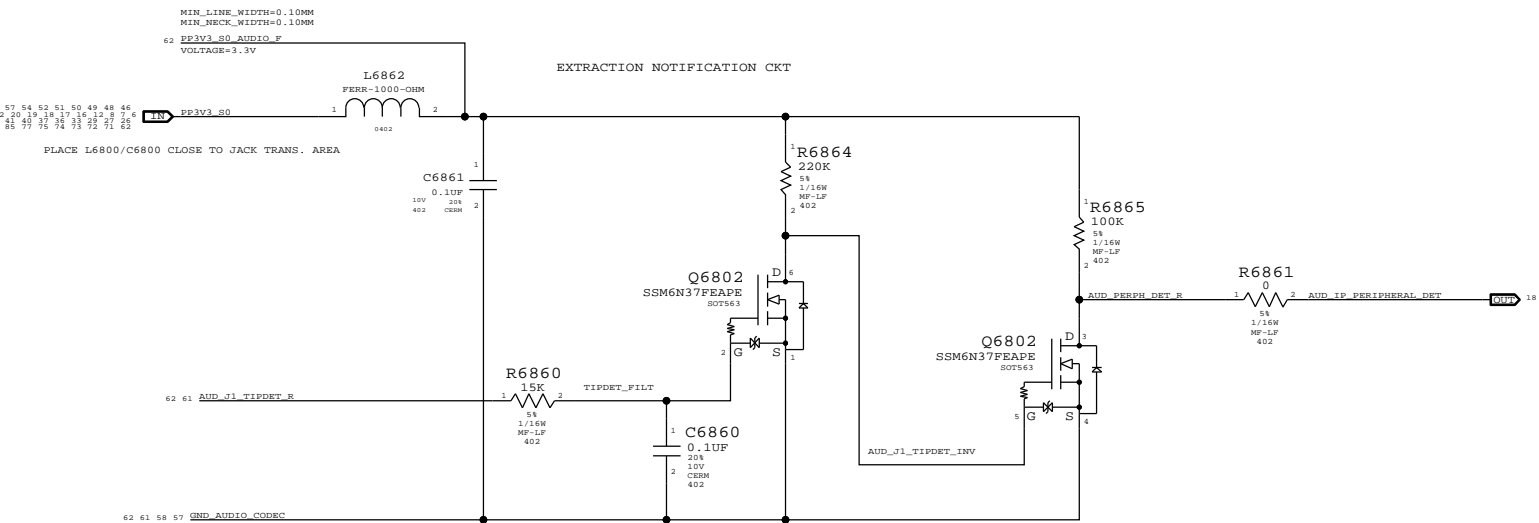
FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	COUGAR_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	COUGAR_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	COUGAR_POINT GPIO3/PIRQH

PORT A DETECT (HEADPHONES)

PORT B DETECT (SPDIF DELEGATE)

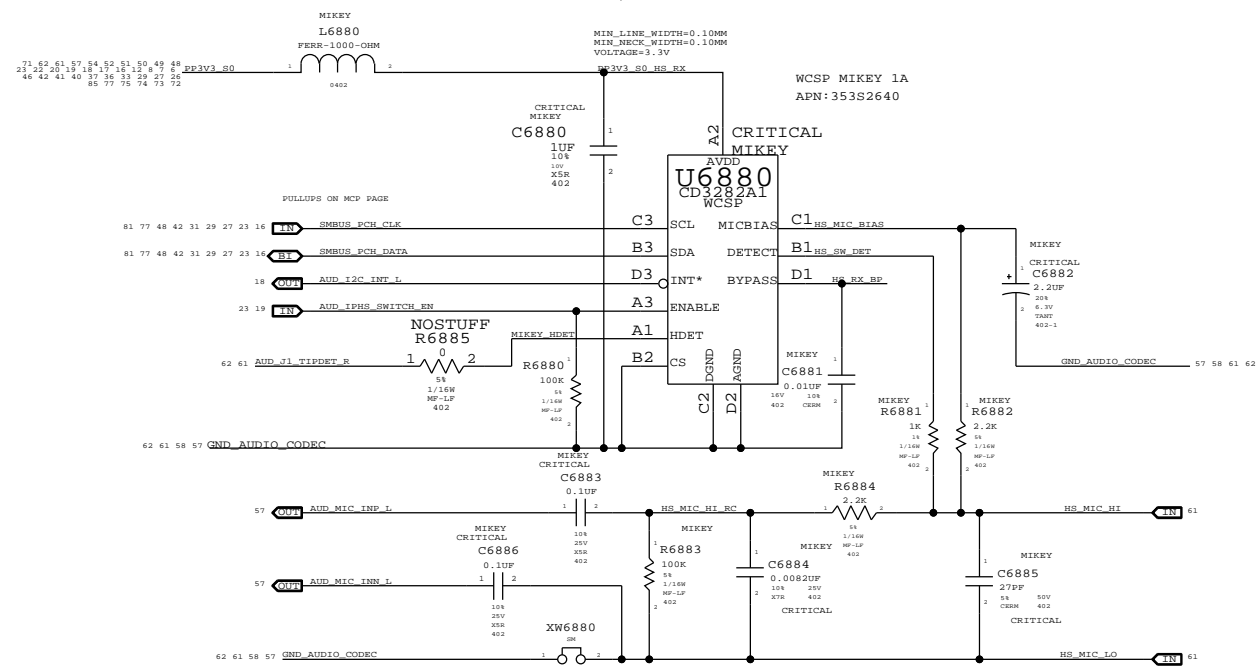


EXTRACTION NOTIFICATION CKT

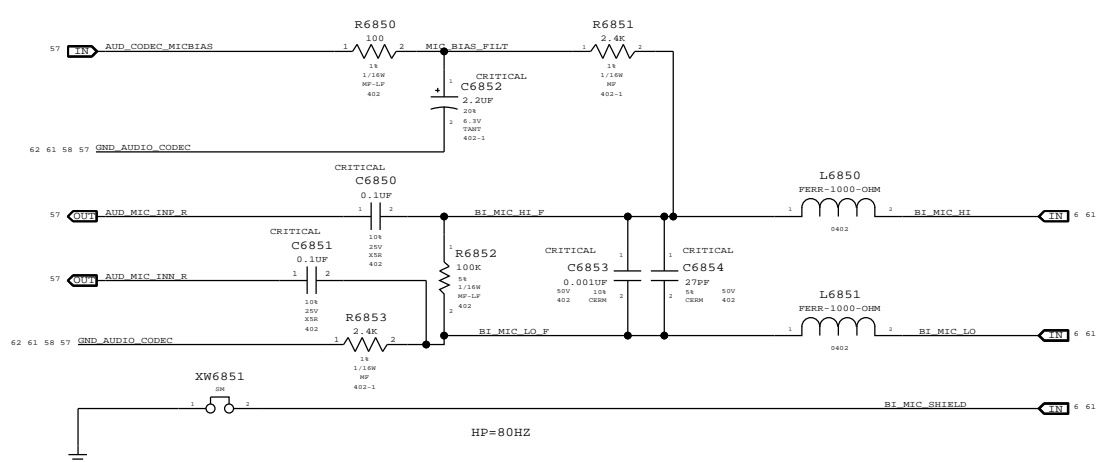


PORT B LEFT (HEADSET MIC)

HP=80HZ, LP=8.82KHZ



PORT B RIGHT (BUILT-IN MIC)



SYNC MASTER=LENG K901 SYNC DATE=08/10/2011

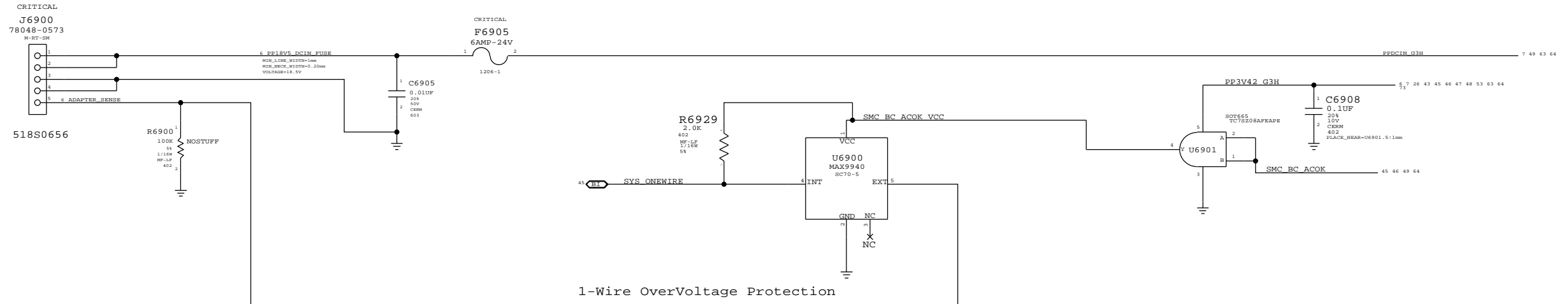
PAGE TITLE: AUDIO: JACK TRANSLATORS

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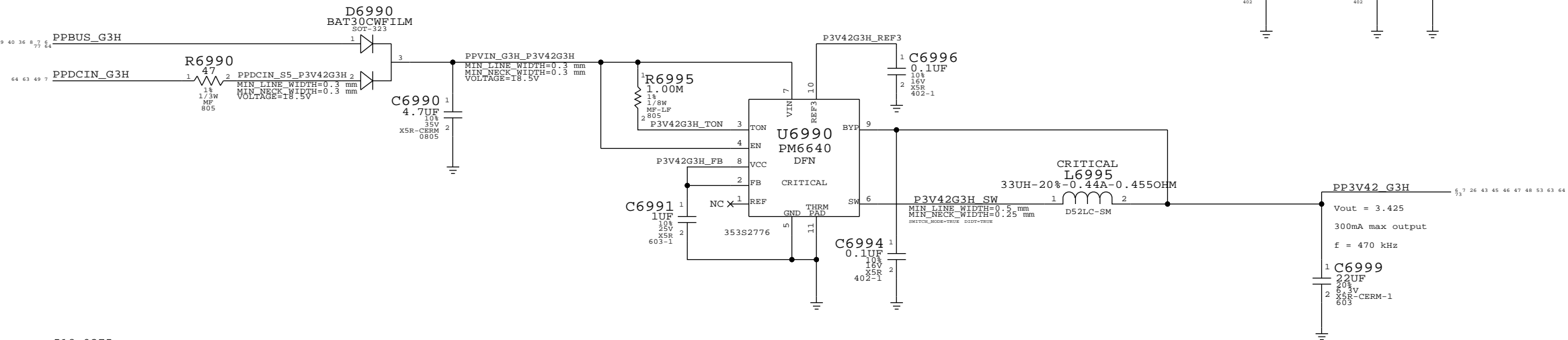
DRAWING NUMBER	SIZE
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MagSafe DC Power Jack

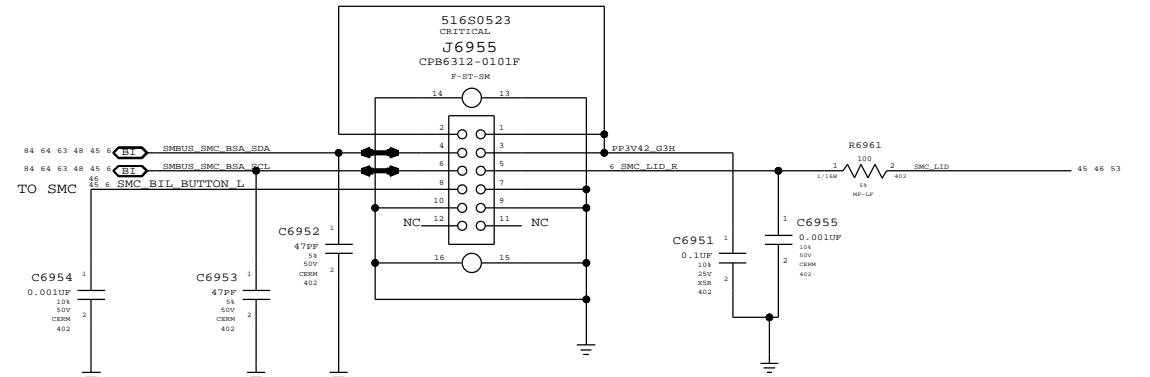


3.425V "G3Hot" Supply

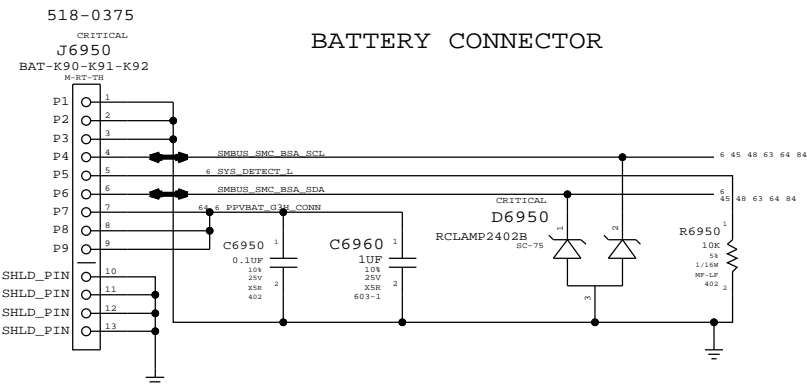
Supply needs to guarantee 3.31V delivered to SMC VRef generator



BIL CONNECTOR

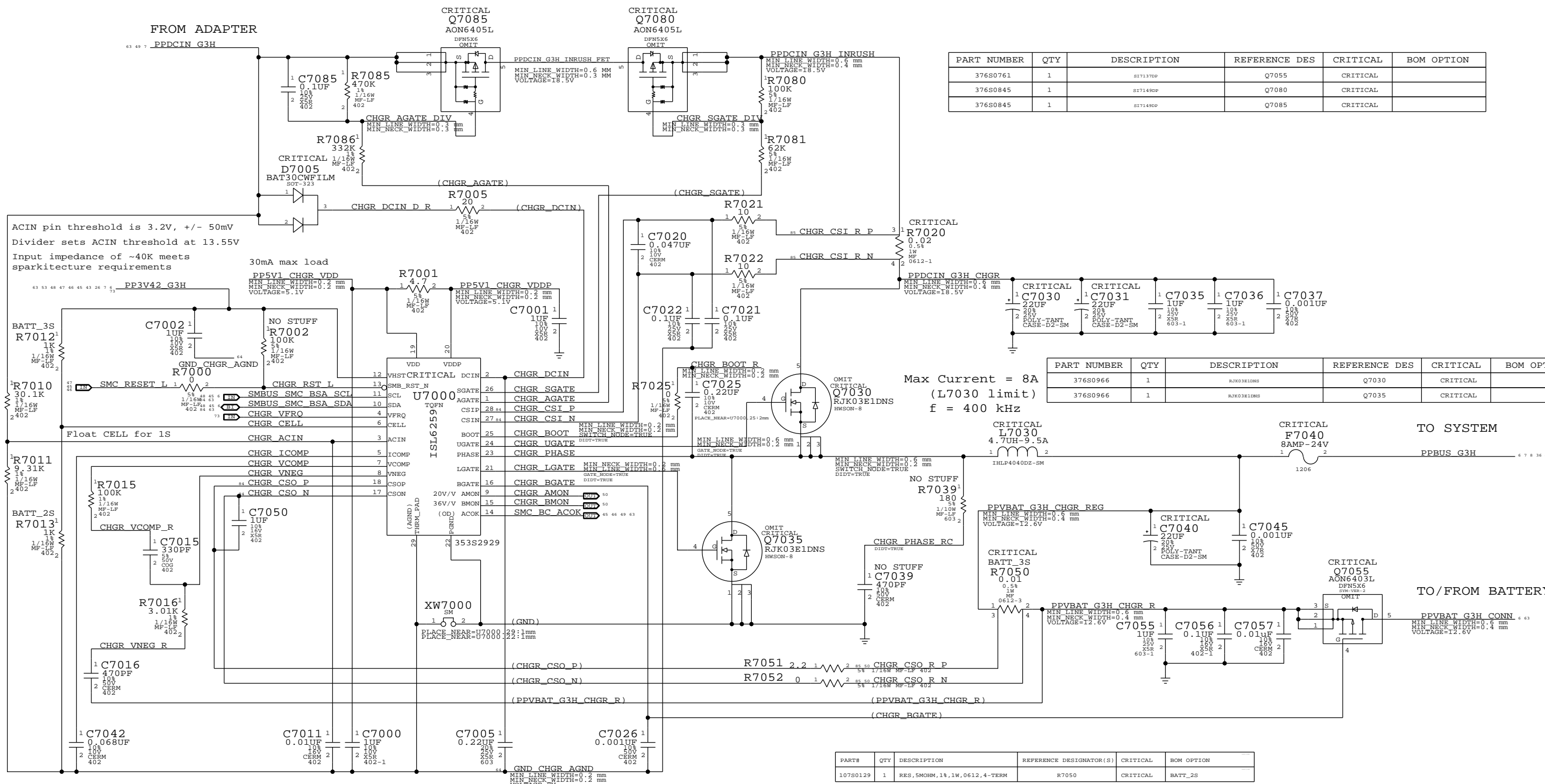


BATTERY CONNECTOR



SYNC MASTER=JACK_K901		SYNC DATE=08/20/2011	
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DC-In & Battery Connectors			
Apple Inc.		DRAWING NUMBER	SIZE
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Inrush Limiter Reverse-Current Protection



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0761	1	S27137DP	Q7055	CRITICAL	
376S0845	1	S27149DP	Q7080	CRITICAL	
376S0845	1	S27149DP	Q7085	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7030	CRITICAL	
376S0966	1	RJK03E1DNS	Q7035	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10780129	1	RES, 5MOHM, 1%, 1W, 0612, 4-TERM	R7050	CRITICAL	BATT_2S

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC MASTER=JACK_K901 SYNC DATE=10/11/2011

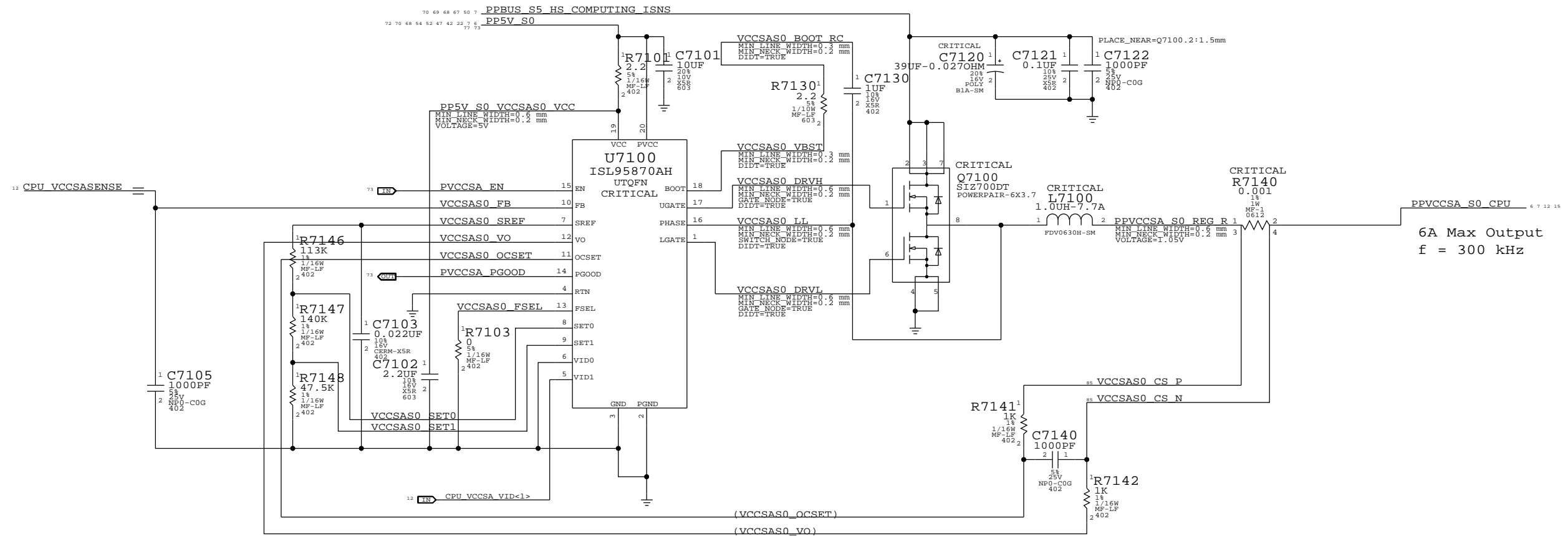
PAGE TITLE: PBus Supply & Battery Charger

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System Agent Power Supply

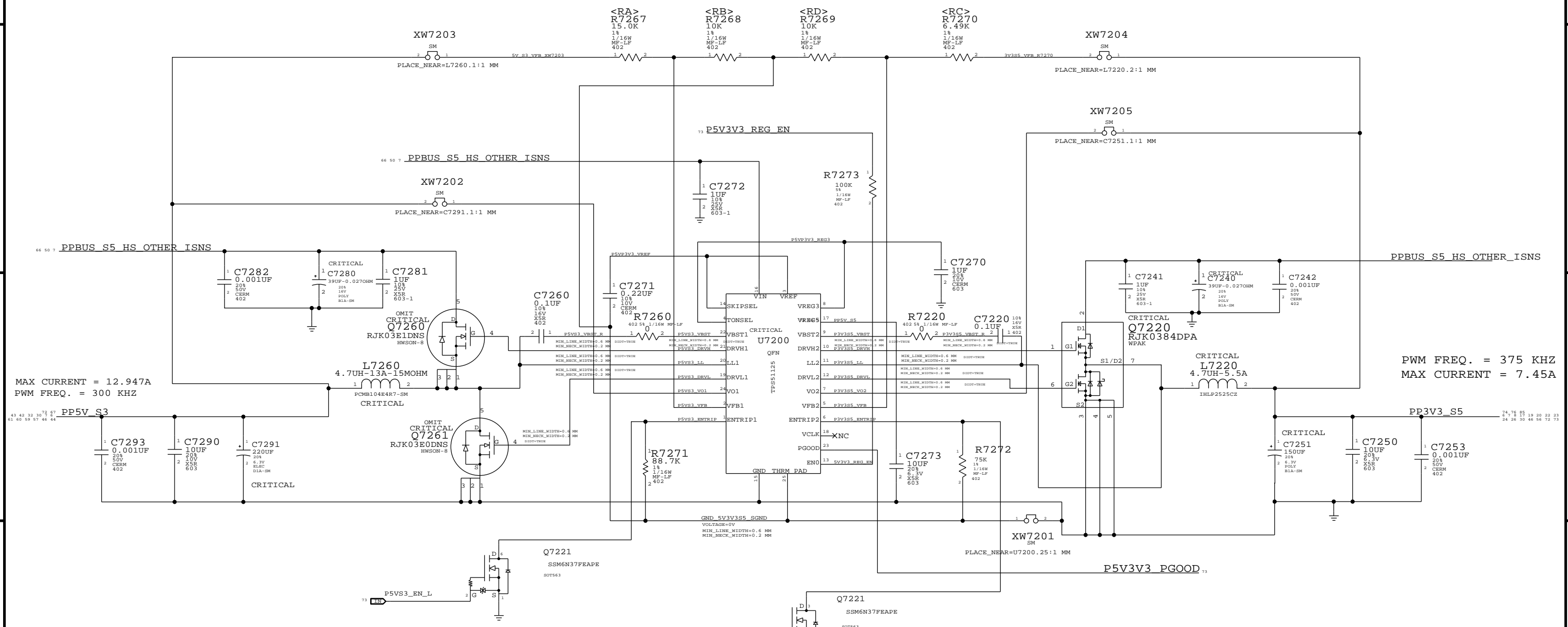


SYNC MASTER=JACK_K901		SYNC DATE=08/19/2010	
System Agent Supply			
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5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * RA / RB) + 2$$

$$V_{OUT} = (2 * RC / RD) + 2$$



MAX CURRENT = 12.947A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.45A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

SYNC MASTER=JACK_K901 SYNC DATE=10/04/2011

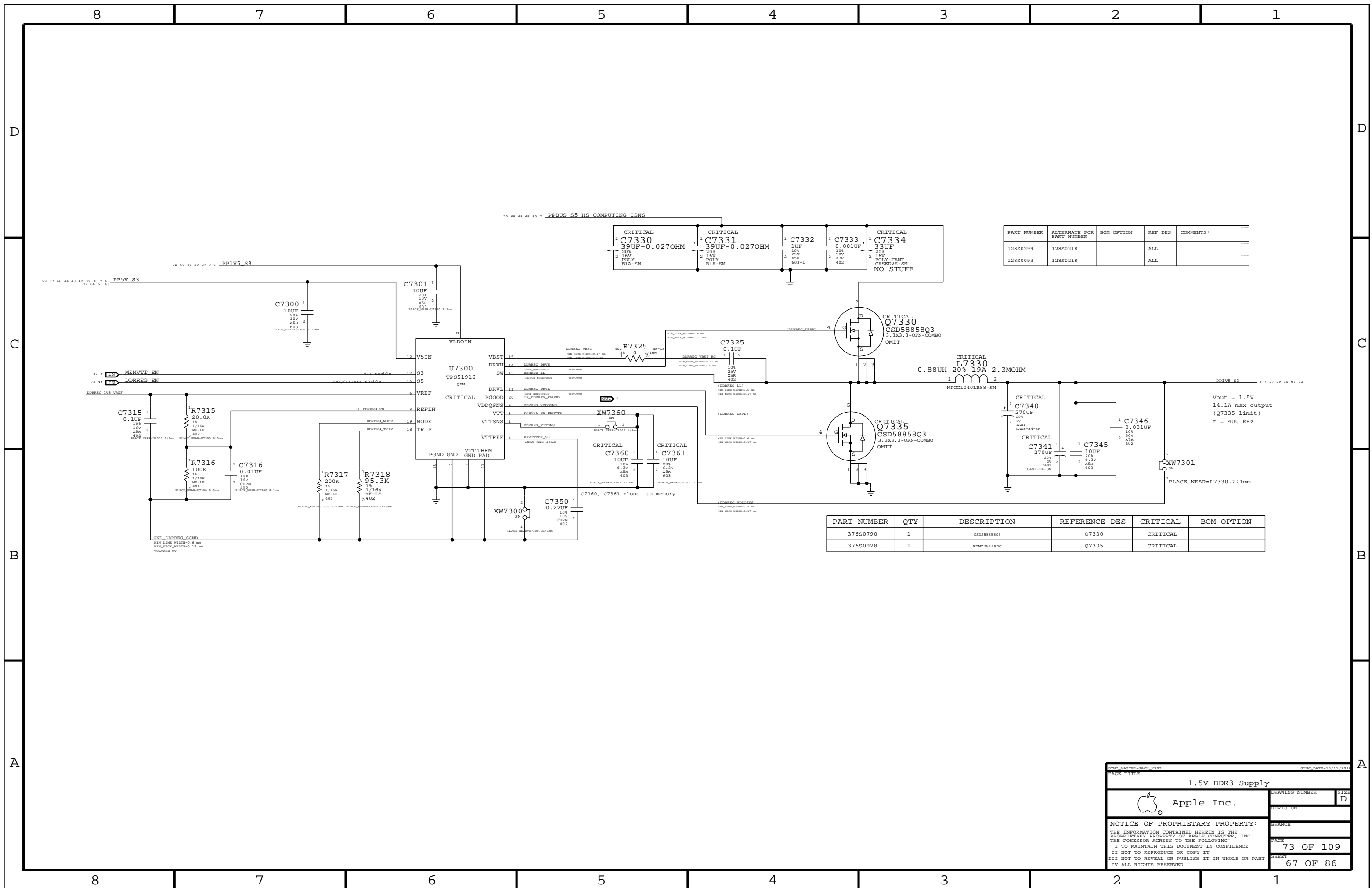
5V/3.3V SUPPLY

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SEPARATED MASTER PG00D FOR BOTH 5V AND 3V3.



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD58858Q3	Q7330	CRITICAL	
376S0928	1	FDMC25148DC	Q7335	CRITICAL	

Vout = 1.5V
14.1A max output
(Q7335 limit)
f = 400 kHz

SYMC MASTER-ACK 4802 SYMC_DATE=10/11/2016

1.5V DDR3 Supply

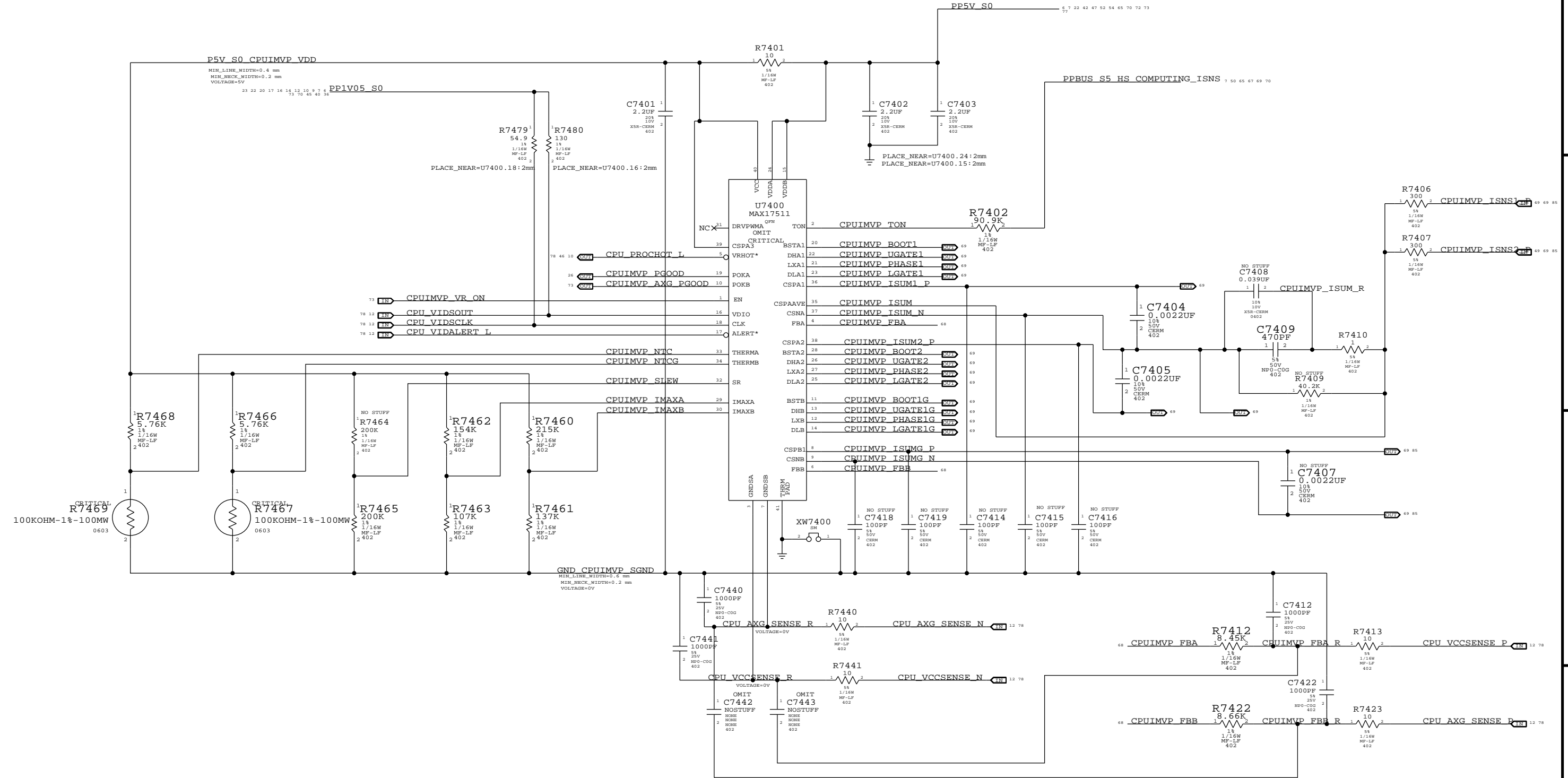
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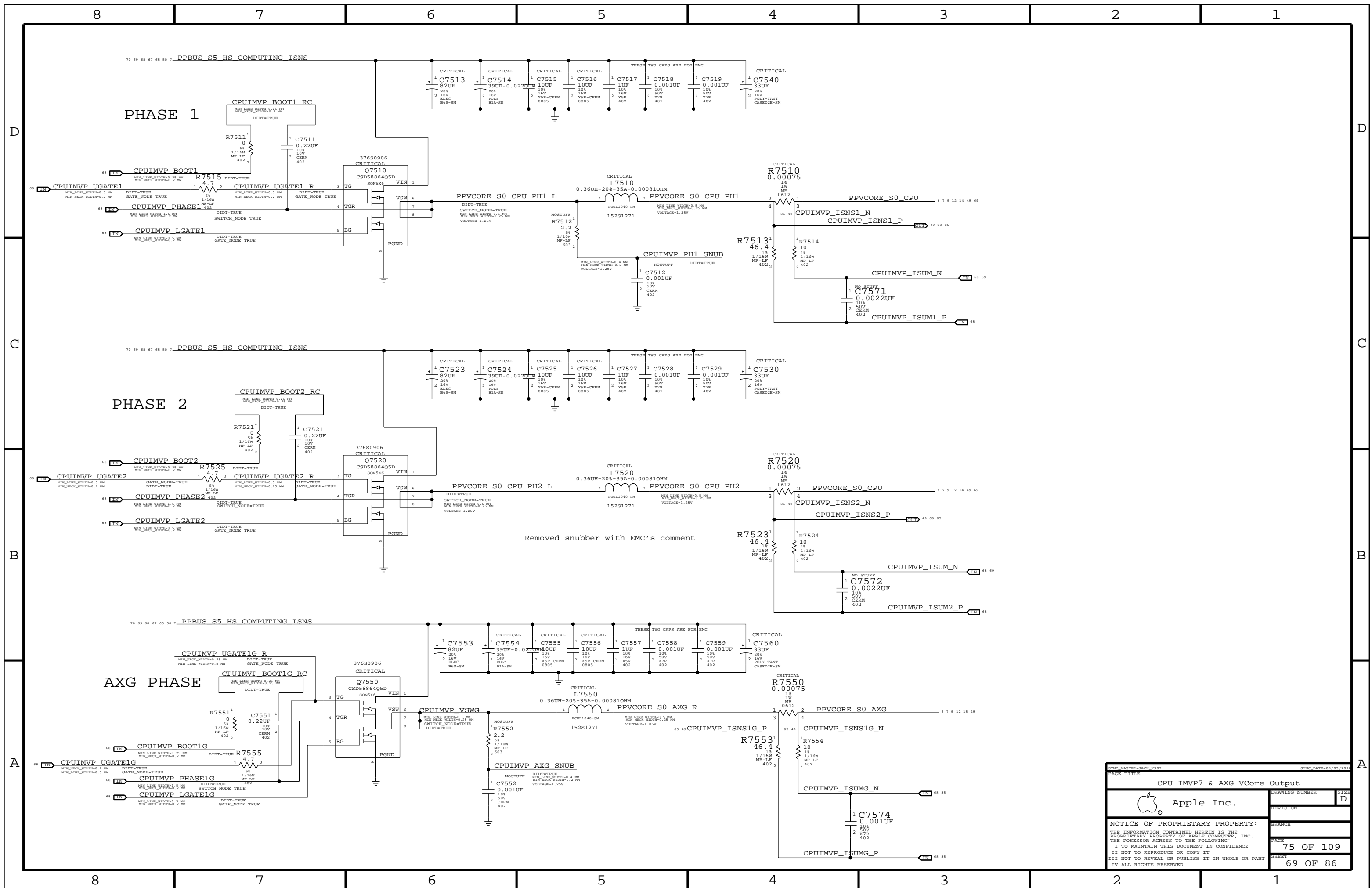
DRAWING NUMBER	SIZE
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PAGE	73 OF 109
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC_MAX15092,3+1PH CPU REG,IMVP7,5XSQPM40	U7400	CRITICAL	

Need symbol to be re-drawn to clean up this page

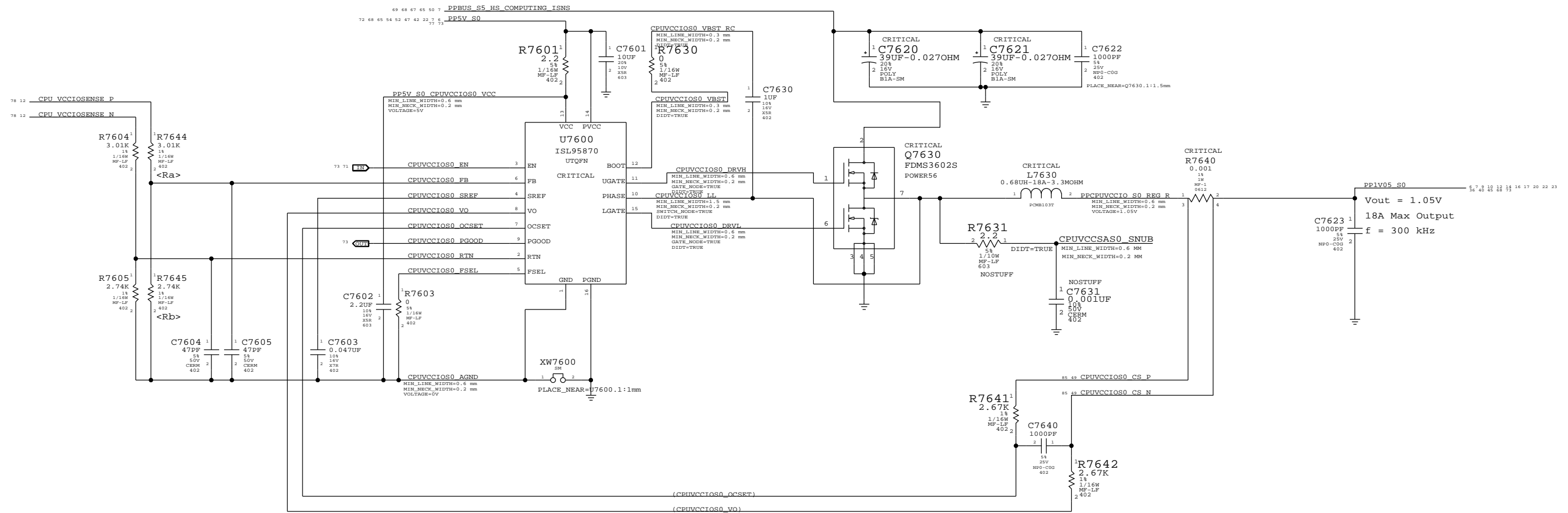


PAGE TITLE		DRAWING NUMBER	
CPU IMVP7 & AXG VCore Regulator		D	
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SYMC MASTER-ACK-2302		SYMC DATE-09/03/2015	
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CPU IMVP7 & AXG VCore Output		DRAWING NUMBER	SIZE
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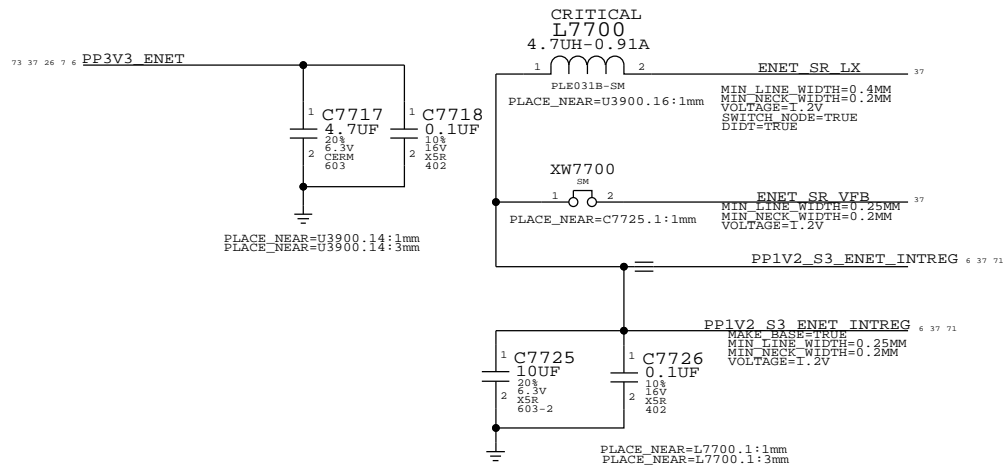
CPU VCCIO (1.05V S0) Regulator



$OCP = R7641 \times 8.5uA / R7640$
 $OCP = 22.695A$
 $Vout = 0.5V * (1 + Ra / Rb)$

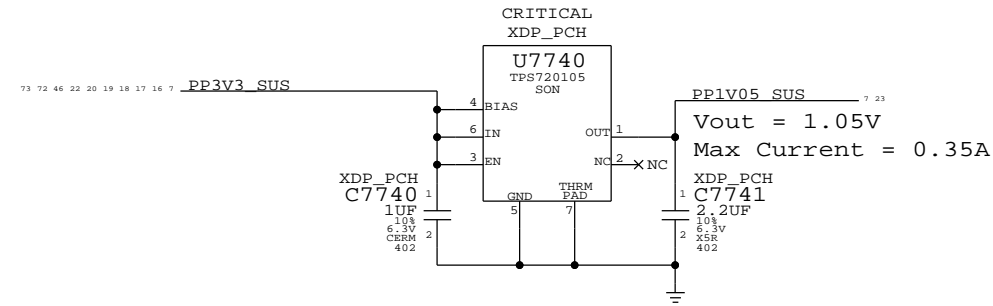
SYNC MASTER=JACK_K901		SYNC DATE=08/19/2011	
PAGE TITLE			
CPUVCCIO (1.05V) Power Supply			
Apple Inc.		DRAWING NUMBER	SIZE
			D
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CAESAR IV 1.2V INT.VR CMPTS



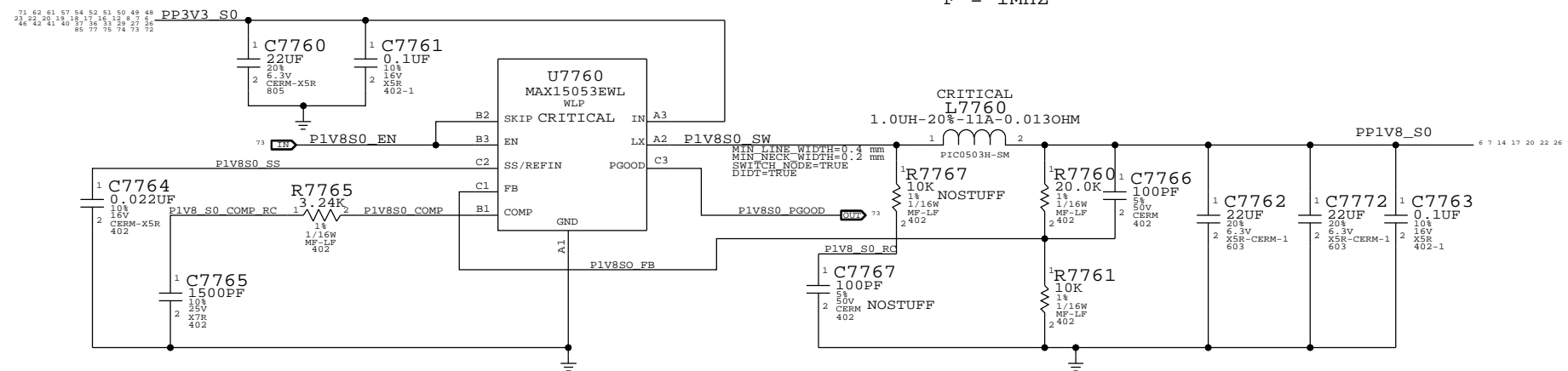
1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5. Pull-ups (3) must be 51 ohms to support XDP (not required in production). 70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



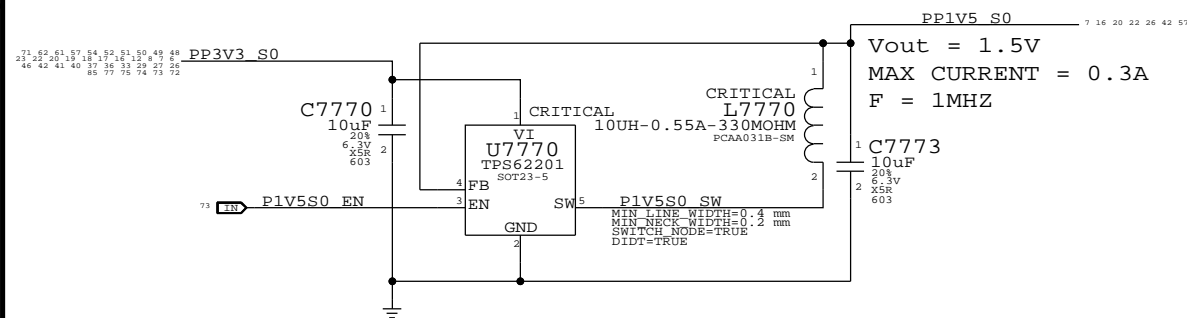
1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



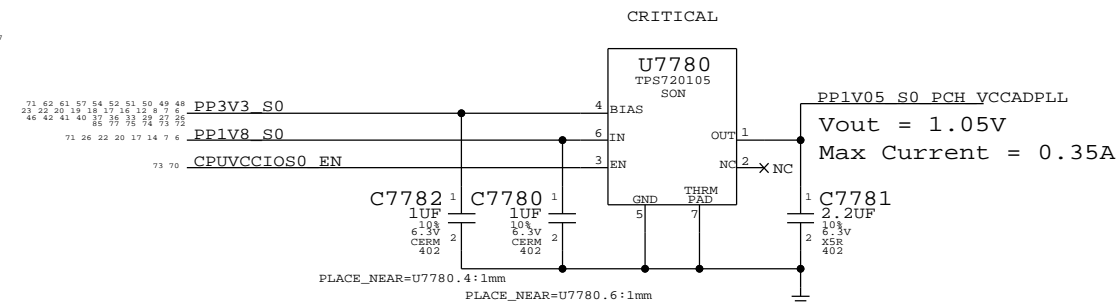
1.5V S0 Switcher

Vout = 1.5V
MAX CURRENT = 0.3A
F = 1MHZ

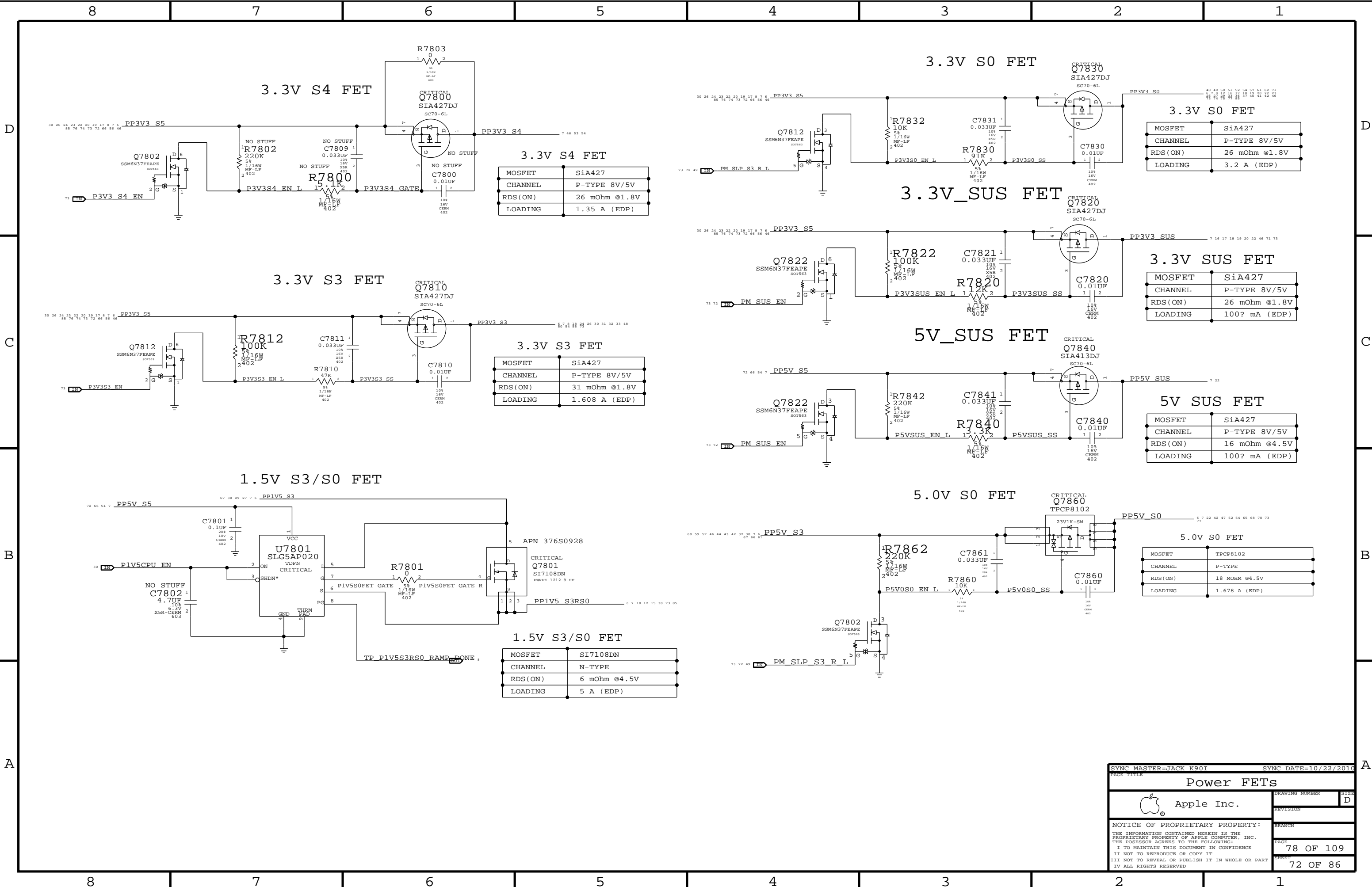


1.05V S0 LDO

Vout = 1.05V
Max Current = 0.35A



SYNC MASTER=JACK_K901		SYNC DATE=08/19/2010	
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Misc Power Supplies		DRAWING NUMBER	SIZE
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3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

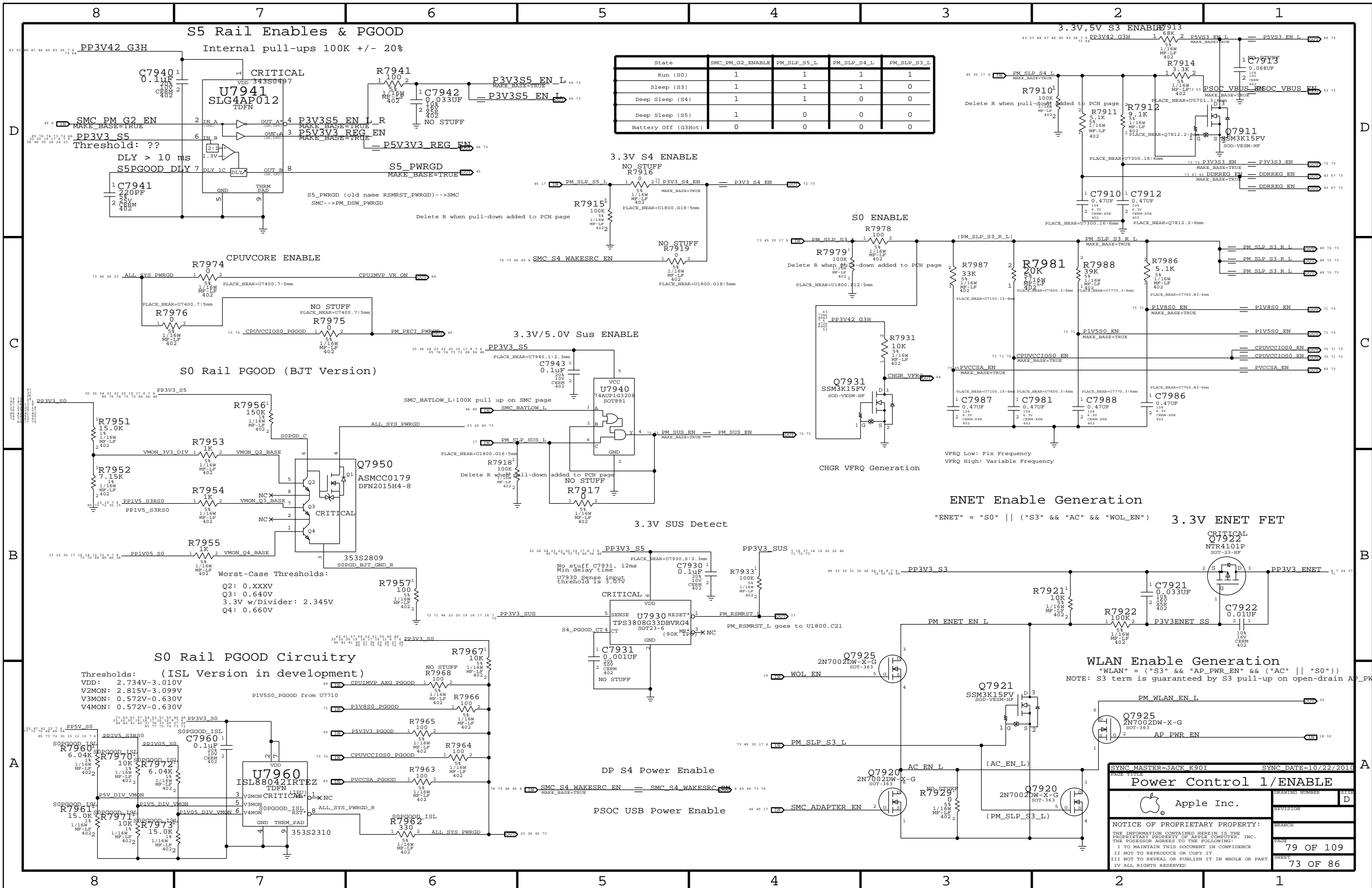
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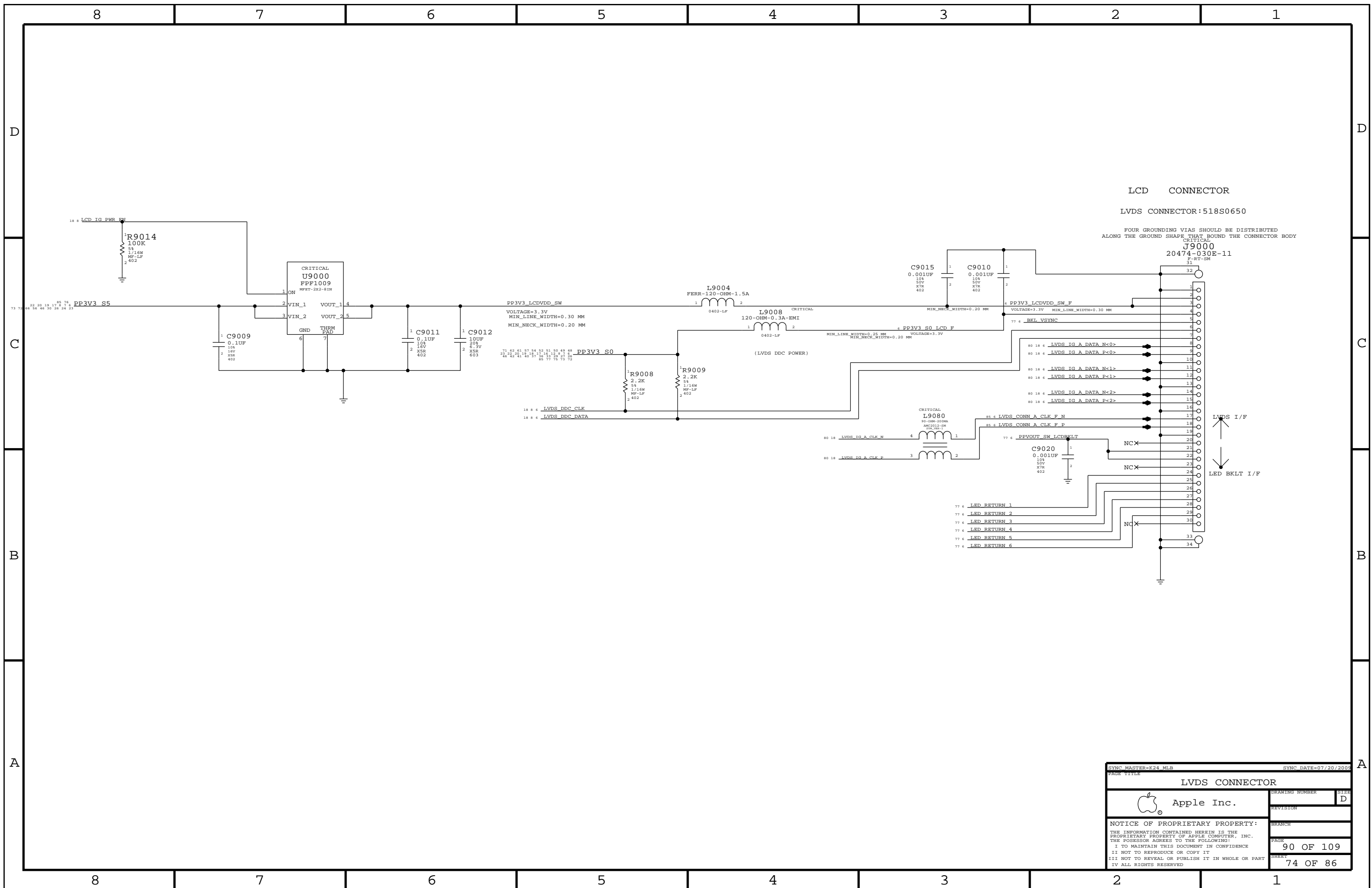
Power FETs

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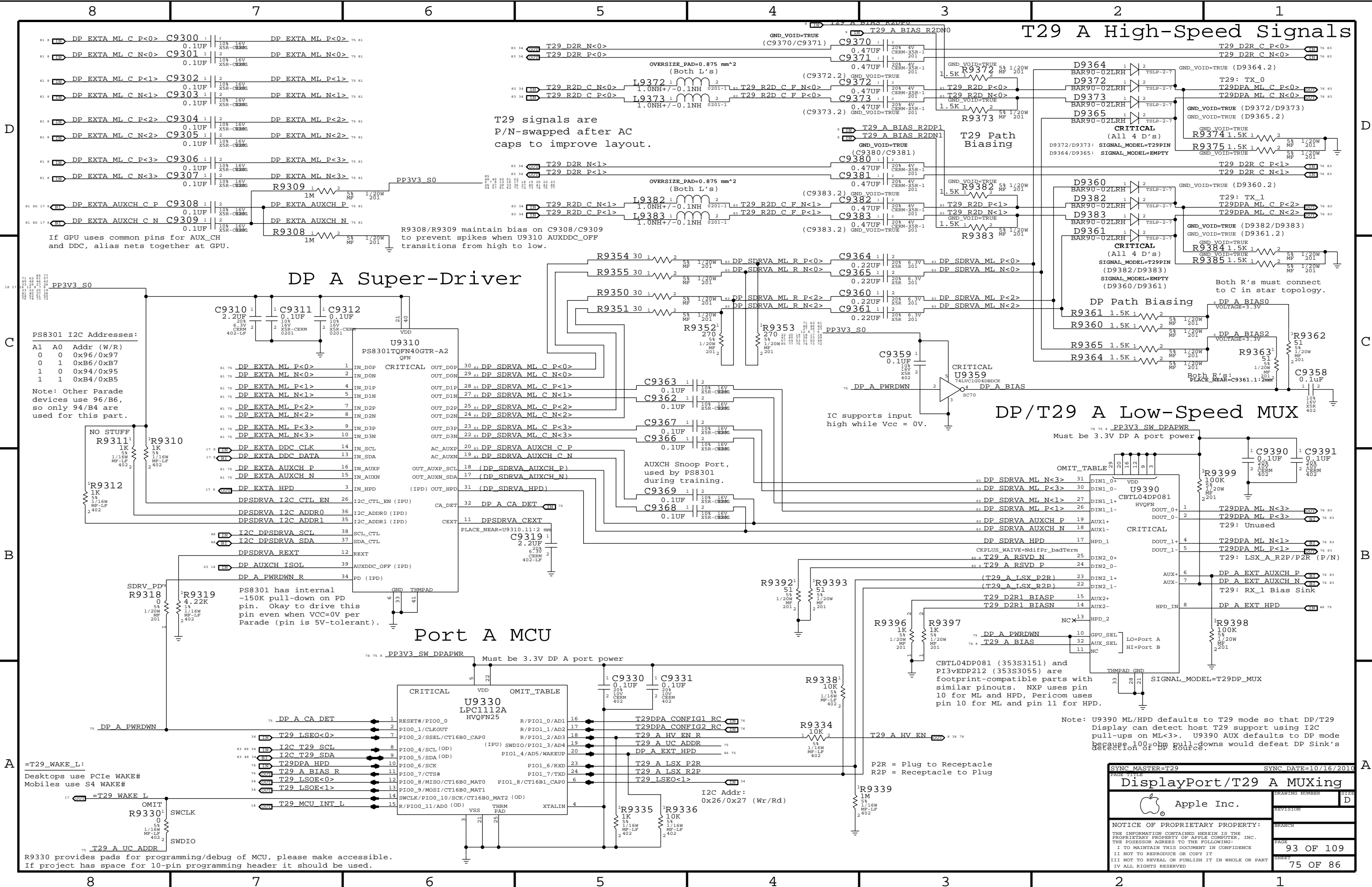
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SYNC MASTER=K24 MLB		SYNC DATE=07/20/2009	
LVDS CONNECTOR			
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T29 A High-Speed Signals

T29 signals are P/N-swapped after AC caps to improve layout.

DP A Super-Driver

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

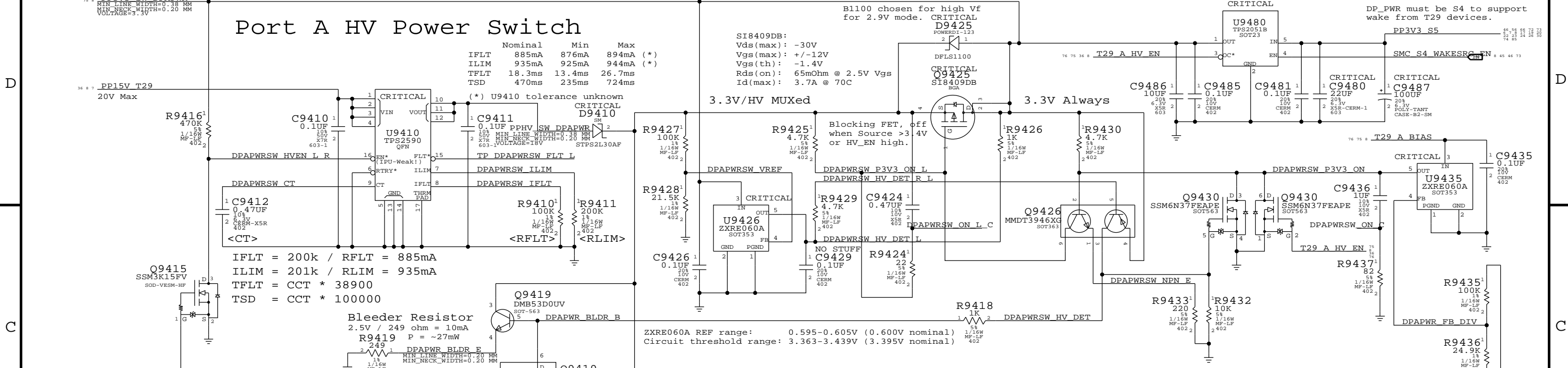
=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

SYNC MASTER=T29		SYNC DATE=10/16/2010	
DisplayPort/T29 A MUXing			
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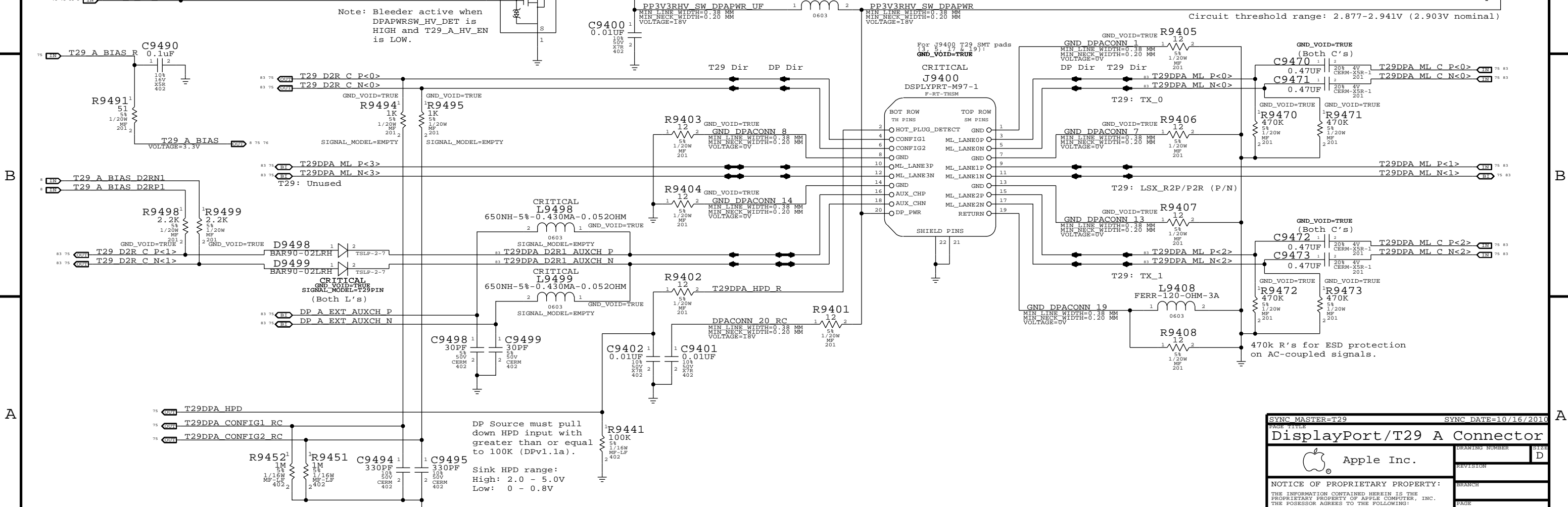
Port A HV Power Switch

3.3V/HV Power MUX

Port A 3.3V Power Switch



DisplayPort/T29 A Connector

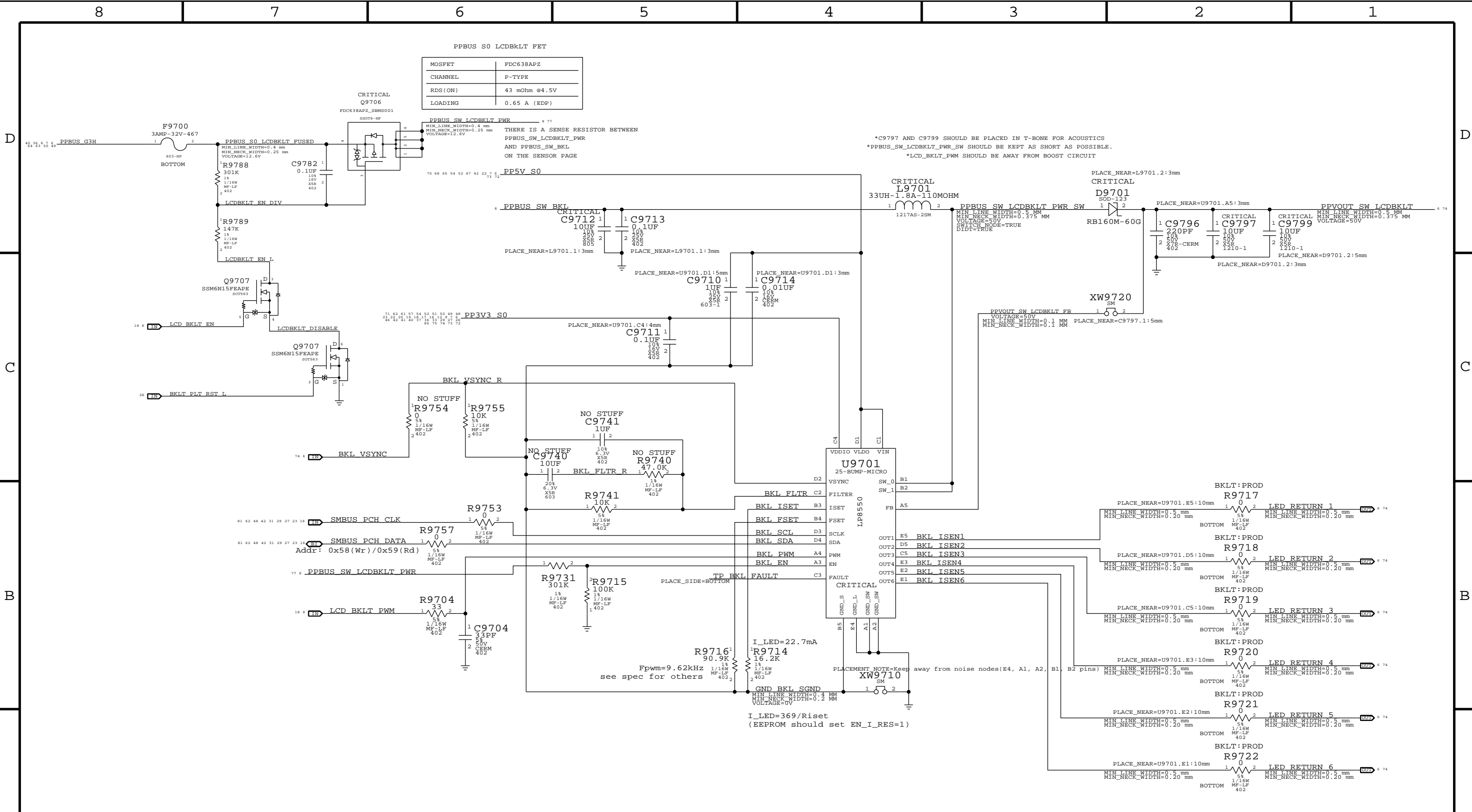


SYNC MASTER=T29		SYNC DATE=10/16/2010	
<h2>DisplayPort/T29 A Connector</h2>			
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PPBUS S0 LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE

*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

PAGE TITLE		SYNC MASTER=VEMURI K901		SYNC DATE=06/25/2010	
LCD Backlight Driver				DRAWING NUMBER	D
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2X_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	20 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

Most CPU signals with impedance requirements are 50-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?	PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?				

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
DMI_S2N	PCIE_85D	PCIE		DMI_S2N P<3:0> 9 17
DMI_S2N	PCIE_85D	PCIE		DMI_S2N N<3:0> 9 17
DMI_N2S	PCIE_85D	PCIE		DMI_N2S P<3:0> 9 17
DMI_N2S	PCIE_85D	PCIE		DMI_N2S N<3:0> 9 17
FDI_DATA	PCIE_85D	PCIE		FDI_DATA P<7:0> 9 17
FDI_DATA	PCIE_85D	PCIE		FDI_DATA N<7:0> 9 17
	CPU_50S	CPU_AGTL		FDI_FSYNC<1..0> 9 17
	CPU_50S	CPU_AGTL		FDI_LSYNC<1..0> 9 17
	CPU_50S	CPU_AGTL		FDI_INT 9 17
	CPU_50S	PCIE		CPU_PRCI 10 19 45
	CPU_50S	CPU_AGTL		PM_SYNC 10 17
	CPU_50S	CPU_AGTL		PM_MEM_PWRGD 10 17 30
	CPU_50S	CPU_ITP		XDP_DBRESET_L 10 23 26
	CPU_50S	CPU_ITP		XDP_CPU_PRDY_L 10 23
	CPU_50S	CPU_ITP		XDP_CPU_PREQ_L 10 23
	CPU_50S	CPU_AGTL		PM_EXT_TS_L<0> 10
	CPU_50S	CPU_AGTL		PM_EXT_TS_L<1> 10
	CPU_SM_RCOMP	CPU_COMP		CPU_SM_RCOMP<0> 10
	CPU_SM_RCOMP	CPU_COMP		CPU_SM_RCOMP<1> 10
	CPU_SM_RCOMP	CPU_COMP		CPU_SM_RCOMP<2> 10
	CPU_50S	CPU_ITP		CPU_CFG<11..0> 9 23
	CPU_50S	CPU_AGTL		CPU_CATERR_L 10
	CPU_50S	CPU_AGTL		CPU_VCCIO_SEE1 12
	CPU_50S	CPU_AGTL		CPU_PROCHOT_L 10 46 68
	CPU_50S	CPU_AGTL		CPU_PWRGD 10 19 23
	PM_THERMTRIP	CPU_8MIL		PM_THERMTRIP_L 10 19
	CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P 10 16
	CLK_PCIE_90D	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N 10 16
	ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P 10 16
	ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N 10 16
	ITPXPDP_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXPDP_CLK100M_P 16 23
	ITPXPDP_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXPDP_CLK100M_N 16 23
	XDP_CPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P 23
	XDP_CPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N 23
	CPU_27P4S	CPU_COMP		EDP_COMP 9
	CPU_27P4S	CPU_COMP		CPU_PEG_COMP 9
	XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI 10 23
	XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO 10 23
	XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS 10 23
	XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK 10 23
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L 10 23
	XDP_BM_L	CPU_50S	CPU_ITP	XDP_BM_L<3..0> 10 23
	XDP_BM_S_L	CPU_50S	CPU_ITP	CPU_CFG<15..12> 9 23
	(FSB_CPUURST_L)	CPU_50S	CPU_ITP	XDP_CPUURST_L 23
	CPU_VCCIO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P 12 68
	CPU_VCCIO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N 12 68
	CPU_VCCIO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P 12 70
	CPU_VCCIO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N 12 70
	CPU_VCCIO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P 12 68
	CPU_VCCIO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N 12 68
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P 12
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N 12
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P 9
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N 9
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P 9
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N 9
	CPU_VIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L 12 68
	CPU_VIDSCCLK	CPU_50S	CPU_COMP	CPU_VIDSCCLK 12 68
	CPU_VIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT 12 68
	PEG_E2D	PCIE_85D	PCIE	PEG_E2D P<15..0> 8
	PEG_E2D	PCIE_85D	PCIE	PEG_E2D N<15..0> 8
	PEG_E2D	PCIE_85D	PCIE	PEG_E2D C P<15..0> 8
	PEG_E2D	PCIE_85D	PCIE	PEG_E2D C N<15..0> 8
	PEG_D2R	PCIE_85D	PCIE	PEG_D2R P<15..0> 8
	PEG_D2R	PCIE_85D	PCIE	PEG_D2R N<15..0> 8
	PEG_D2R	PCIE_85D	PCIE	PEG_D2R C P<15..0> 8
	PEG_D2R	PCIE_85D	PCIE	PEG_D2R C N<15..0> 8

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

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CPU Constraints		DRAWING NUMBER	SIZE
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).
 DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
 DQ to DQS matching per byte lane should be within 0.127mm.
 DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
 CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
 CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
 A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
 DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
 Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from processor ball to SODIMM pad is 88.9mm.
 SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MEM_A_CLK	MEM_37D	MEM_CLK	MEM_A_CLK P<5..0>
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK N<5..0>
MEM_A_CTRL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>
MEM_A_CTRL	MEM_37S	MEM_CTRL	MEM_A_CS L<3..0>
MEM_A_CTRL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BAS L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS L
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE L
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>
MEM_B_CLK	MEM_37D	MEM_CLK	MEM_B_CLK P<5..0>
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK N<5..0>
MEM_B_CTRL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>
MEM_B_CTRL	MEM_37S	MEM_CTRL	MEM_B_CS L<3..0>
MEM_B_CTRL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BAS L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS L
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE L
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS P<0>
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS N<0>
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS P<1>
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS N<1>
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS P<2>
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS N<2>
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS P<3>
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS N<3>
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS P<4>
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS N<4>
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS P<5>
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS N<5>
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS P<6>
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS N<6>
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS P<7>
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS N<7>

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Memory Constraints

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?	SATA	TOP,BOTTOM	=3x_DIELECTRIC	?
SATA_IOMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP IG ML P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP IG ML N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C P	8 17 75 81
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C N	8 17 75 81
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS IG A CLK P	18 74
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS IG A CLK N	18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS IG A DATA P<2..0>	6 18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS IG A DATA N<2..0>	6 18 74
	LVDS_90D	LVDS	NC LVDS IG A DATAP<3>	8 18
	LVDS_90D	LVDS	NC LVDS IG A DATAN<3>	8 18
	LVDS_90D	LVDS	LVDS IG B DATA P<3..0>	8
	LVDS_90D	LVDS	LVDS IG B DATA N<3..0>	8
	LVDS_90D	LVDS	TP LVDS IG B CLKP	6 8 18
	LVDS_90D	LVDS	TP LVDS IG B CLKN	6 8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P	16 42
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA HDD R2D P	6 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA HDD R2D N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P	16 42
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N	16 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA HDD D2R C P	6 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA HDD D2R C N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P	16 42
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N	16 42
SATA_HDD_R2D_RC	SATA_90D	SATA	SATA HDD R2D RC P	42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA HDD R2D RC N	42
SATA_HDD_D2R_RC	SATA_90D	SATA	SATA HDD D2R RC P	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA HDD D2R RC N	42
PCH_SATA_IOMP	SATA_IOMP	SATA_IOMP	PCH SATAIOMP	16
USB_HUB1_UP	USB_85D	USB	USB HUB1 UP P	18 24
USB_HUB1_UP	USB_85D	USB	USB HUB1 UP N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2 UP P	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2 UP N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA P	24 43
USB_EXTA	USB_85D	USB	USB_EXTA N	24 43
USB_EXTB	USB_85D	USB	USB_EXTB P	24 43
USB_EXTB	USB_85D	USB	USB_EXTB N	24 43
USB_EXTC	USB_85D	USB	USB_EXTC P	8 24
USB_EXTC	USB_85D	USB	USB_EXTC N	8 24
USB_EXTD	USB_85D	USB	USB T29A P	8 24
USB_EXTD	USB_85D	USB	USB T29A N	8 24
	USB_85D	USB	T29_A_ESVD P	8 75
	USB_85D	USB	T29_A_ESVD N	8 75
USB_CAMERA	USB_85D	USB	USB_CAMERA P	18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA N	18 32
USB_CAMERA_CONN	USB_85D	USB	USB_CAMERA_CONN P	6 32
USB_CAMERA_CONN	USB_85D	USB	USB_CAMERA_CONN N	6 32
USB_BT	USB_85D	USB	USB_BT P	6 24 32
USB_BT	USB_85D	USB	USB_BT N	6 24 32
USB_TPAD	USB_85D	USB	USB_TPAD P	24 53
USB_TPAD	USB_85D	USB	USB_TPAD N	24 53
USB_IR	USB_85D	USB	USB_IR P	24 44
USB_IR	USB_85D	USB	USB_IR N	24 44
USB_SDCARD	USB_85D	USB	USB_SDCARD P	
USB_SDCARD	USB_85D	USB	USB_SDCARD N	
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT P	
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT N	
PCH_USB_BIAS	PCH_USB_BIAS	PCH_USB_BIAS	PCH USB_BIAS	18
PCH_PCIE_CLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_PCIE_CLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_P	8
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_N	8
PCH_PCIE_CLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_PCIE_CLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_PCIE_CLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_PCIE_CLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
	CLK_PCIE_90D	CLK_PCIE	PCH_CLK33M_PCIEIN	16 26
GFX_CLK_DP1LSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DP1LSS_P	
GFX_CLK_DP1LSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DP1LSS_N	

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PCH Constraints 1			
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LPC Bus Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rules for LPC_50S and CLK_LPC_50S.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rules for LPC and CLK_LPC.

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rule for SMB_50S.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rule for SMB.

HD Audio Interface Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rule for HDA_50S.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rule for HDA.

SOURCE: Calpella Platform Design Guide for Ihex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rule for CLK_SLOW_55S.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rule for CLK_SLOW.

SPI Interface Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rule for SPI_55S.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rule for SPI.

DisplayPort Signal Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rule for DP_85D.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rule for DISPLAYPORT.

PCI-Express Signal Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rules for PCIE_85D and CLK_PCIE_90D.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rules for PCIE and CLK_PCIE.

System Clock Signal Constraints

Table with columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Includes rules for CLK_SLOW_55S and CLK_25M_55S.

Table with columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Includes rules for CLK_SLOW and CLK_25M.

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

Table with columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists various net types such as LPC_AD, LPC_FRAME_L, LPCPLUS RESET_L, LPC_CLK33M, SMBUS_PCH_CLK, HDA_BIT_CLK, SPI_CLK, etc.

Chipset Net Properties

Table with columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists various net types such as DP_EXTA_ML, DP_INT_ML, PCIE_T29_R2D, etc.

Clock Net Properties

Table with columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists various net types such as SYSCLK_CLK32K_RTC, SYSCLK_CLK25M_SB, etc.

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Apple Inc. logo and PCH Constraints 2 header. Includes drawing number, revision, and notice of proprietary property. Page 103 of 109, Sheet 81 of 86.

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	5MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
ENET_50S	ENET_3X	ENET_3X	BCM5764_CLK25M_XTALI	
ENET_50S	ENET_3X	ENET_3X	BCM5764_CLK25M_XTALO	
ENET_50S	ENET_3X	ENET_3X	ENET_RESET_L	33 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38
ENET_CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	33 37
ENET_CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	33 37
ENET_CR_CLK	ENET_50S	ENET_CR_CLK	ENET_CR_CLK	33 37
ENET_CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	33
ENET_CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD	33
ENET_CR_CLK	ENET_50S	ENET_CR_CLK	SDCONN_CLK	33
ENET_CR_CLK	ENET_50S	ENET_CR_CLK	SDCONN_CLK_L	33

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FW_D0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_D0_TPB	FW_110D	FW_TP	NC_FW0_TPB	39 41
FW_D0_TPB	FW_110D	FW_TP	NC_FW0_TBPB	6 39 41
FW_D0_TPB	FW_110D	FW_TP	NC_FW0_TBPN	6 39 41
FW_D1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 41
FW_D1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 41
FW_D1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 41
FW_D1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 41
Port 2 Not Used				

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Ethernet/FW Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?	T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0>	34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0>	34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0>	34
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0>	34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P	34 37 34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N	34 37 34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P	34
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N	34
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0>	34
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0>	34
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0>	34
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0>	34
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P	34 37 34
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N	34 37 34
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P	34
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N	34
DP_T29SRC_ML	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>	
DP_T29SRC_ML	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>	
DP_T29SRC_AUXCH	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P	
DP_T29SRC_AUXCH	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N	
T29_I2C_55S	T29_I2C	T29_I2C	I2C T29_SCL	34 48 75
T29_I2C_55S	T29_I2C	T29_I2C	I2C T29_SDA	34 48 75
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29 SPI CLK	34
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29 SPI MOSI	34
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29 SPI MISO	34
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29 SPI CS_L	34
T29DP_80D	T29DP	T29DP	T29 R2D C P<3..0>	34 75
T29DP_80D	T29DP	T29DP	T29 R2D C N<3..0>	34 75
T29DP_100D	T29DP	T29DP	T29 D2R P<3..0>	34 75
T29DP_100D	T29DP	T29DP	T29 D2R N<3..0>	34 75

Only used on hosts supporting T29 video-in

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
T29_R2D0	T29DP_80D	T29DP	T29 R2D P<0>	75
T29_R2D0	T29DP_80D	T29DP	T29 R2D N<0>	75
T29_R2D1	T29DP_80D	T29DP	T29 R2D P<1>	75
T29_R2D1	T29DP_80D	T29DP	T29 R2D N<1>	75
T29DP_80D	T29DP_80D	T29DP	T29 R2D C F P<1..0>	75
T29DP_80D	T29DP_80D	T29DP	T29 R2D C F N<1..0>	75
T29_D2R0	T29DP_100D	T29DP	T29 D2R C P<0>	75 76
T29_D2R0	T29DP_100D	T29DP	T29 D2R C N<0>	75 76
T29_D2R1	T29DP_100D	T29DP	T29 D2R C P<1>	75 76
T29_D2R1	T29DP_100D	T29DP	T29 D2R C N<1>	75 76
T29DP_100D	T29DP_100D	T29DP	T29DPA D2R1 AUXCH P	76
T29DP_100D	T29DP_100D	T29DP	T29DPA D2R1 AUXCH N	76
T29DP_80D	T29DP_80D	T29DP	DP SDRVA ML C P<3..0>	75
T29DP_80D	T29DP_80D	T29DP	DP SDRVA ML C N<3..0>	75
T29DP_80D	T29DP_80D	T29DP	DP SDRVA ML R P<3..0>	75
T29DP_80D	T29DP_80D	T29DP	DP SDRVA ML R N<3..0>	75
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<2..0:2>	83
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<2..0:2>	83
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML P<3..1:2>	75 83
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<3..1:2>	75
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH P	75
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH N	75
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH C P	75
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH C N	75
T29DP_80D	T29DP_80D	T29DP	T29DPA ML P<3..0>	75 76
T29DP_80D	T29DP_80D	T29DP	T29DPA ML N<3..0>	75 76
T29DP_80D	T29DP_80D	T29DP	T29DPA ML C P<3..0>	75 76
T29DP_80D	T29DP_80D	T29DP	T29DPA ML C N<3..0>	75 76
T29DP_80D	T29DP_80D	T29DP	DP A EXT AUXCH P	75 76
T29DP_80D	T29DP_80D	T29DP	DP A EXT AUXCH N	75 76
T29_R2D2	T29DP_80D	T29DP	T29 R2D P<2>	
T29_R2D2	T29DP_80D	T29DP	T29 R2D N<2>	
T29_R2D3	T29DP_80D	T29DP	T29 R2D P<3>	
T29_R2D3	T29DP_80D	T29DP	T29 R2D N<3>	
T29DP_80D	T29DP_80D	T29DP	T29 R2D C F P<3..2>	
T29DP_80D	T29DP_80D	T29DP	T29 R2D C F N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29 D2R C P<2>	
T29_D2R2	T29DP_100D	T29DP	T29 D2R C N<2>	
T29_D2R3	T29DP_100D	T29DP	T29 D2R C P<3>	
T29_D2R3	T29DP_100D	T29DP	T29 D2R C N<3>	
T29DPB_D2R3_AUXCH	T29DP_100D	T29DP	T29DPB D2R3 AUXCH P	
T29DPB_D2R3_AUXCH	T29DP_100D	T29DP	T29DPB D2R3 AUXCH N	
T29DP_80D	T29DP_80D	T29DP	DP SDRVB ML C P<3..0>	
T29DP_80D	T29DP_80D	T29DP	DP SDRVB ML C N<3..0>	
T29DP_80D	T29DP_80D	T29DP	DP SDRVB ML R P<3..0>	
T29DP_80D	T29DP_80D	T29DP	DP SDRVB ML R N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP SDRVB ML P<2..0:2>	83
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP SDRVB ML N<2..0:2>	83
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP SDRVB ML P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP SDRVB ML N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH N	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH C P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH C N	
T29DPB_D2R3_AUXCH	T29DP_80D	T29DP	T29DPB ML P<3..0>	
T29DPB_D2R3_AUXCH	T29DP_80D	T29DP	T29DPB ML N<3..0>	
T29DPB_D2R3_AUXCH	T29DP_80D	T29DP	T29DPB ML C P<3..0>	
T29DPB_D2R3_AUXCH	T29DP_80D	T29DP	T29DPB ML C N<3..0>	
T29DPB_D2R3_AUXCH	T29DP_80D	T29DP	DP B EXT AUXCH P	
T29DPB_D2R3_AUXCH	T29DP_80D	T29DP	DP B EXT AUXCH N	

Only used on dual-port hosts.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	SIZE
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_500	0300	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_500	0300	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_500	0300	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_500	0300	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_O_S0_SCL	SMB_500	0300	SMBUS_SMC_O_S0_SCL	6 32 45 48 51
SMBUS_SMC_O_S0_SDA	SMB_500	0300	SMBUS_SMC_O_S0_SDA	6 32 45 48 51
SMBUS_SMC_BSA_SCL	SMB_500	0300	SMBUS_SMC_BSA_SCL	6 45 48 53 64
SMBUS_SMC_BSA_SDA	SMB_500	0300	SMBUS_SMC_BSA_SDA	6 45 48 53 64
SMBUS_SMC_MGMT_SCL	SMB_500	0300	SMBUS_SMC_MGMT_SCL	45 48
SMBUS_SMC_MGMT_SDA	SMB_500	0300	SMBUS_SMC_MGMT_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	SIZE
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_L101_550	*	+1:1_DIFFPAIR	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
THERM_L101_550	*	+1:1_DIFFPAIR	+55_OHM_SR	+55_OHM_SR	+55_OHM_SR	+1:1_DIFFPAIR	+1:1_DIFFPAIR
DIFFPAIR	*	+1:1_DIFFPAIR			+1:1_DIFFPAIR	+1:1_DIFFPAIR	+1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	+2:1_SPACING	?
THERM	*	+2:1_SPACING	?
AUDIO	*	+2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	+STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P20M	*	0.20 MM	1000
PWR_P20M	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P20M
MEM_CMD	GND	*	GND_P20M
MEM_CTRL	GND	*	GND_P20M
MEM_DATA	GND	*	GND_P20M
MEM_SQS	GND	*	GND_P20M

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.09 MM	400 MIL	OVERVERRIDE	OVERVERRIDE
MEM_72D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.09 MM	400 MIL	OVERVERRIDE	OVERVERRIDE
MEM_37S	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.09 MM	400 MIL	OVERVERRIDE	OVERVERRIDE
MEM_85D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.09 MM	400 MIL	OVERVERRIDE	OVERVERRIDE
PCIE_85D	OVERVERRIDE	OVERVERRIDE	OVERVERRIDE	0.076 MM	10 MM	OVERVERRIDE	OVERVERRIDE
USB_85D	TOP	OVERVERRIDE	OVERVERRIDE	0.1 MM	500 MIL	OVERVERRIDE	OVERVERRIDE
CPU_27F4S	TOP	OVERVERRIDE	OVERVERRIDE	0.09 MM	400 MIL	OVERVERRIDE	OVERVERRIDE
CLK_PCIE_90D	TOP	OVERVERRIDE	OVERVERRIDE	0.09 MM	400 MIL	OVERVERRIDE	OVERVERRIDE

A Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
ENETCONN_P<3..0>	ENETCONN	ENETCONN_P<3..0>	38
ENETCONN_N<3..0>	ENETCONN	ENETCONN_N<3..0>	38
SATA_Q0D	SATA	SATA_Q0D_D2R_UF_P	6 42
SATA_Q0D	SATA	SATA_Q0D_D2R_UF_N	6 42
SATA_Q0D	SATA	SATA_HDD_D2R_SERV0_OUT_P	42
SATA_Q0D	SATA	SATA_HDD_D2R_SERV0_OUT_N	42
SATA_Q0D	SATA	SATA_HDD_R2D_SERV0_IN_P	42
SATA_Q0D	SATA	SATA_HDD_R2D_SERV0_IN_N	42
SATA_Q0D	SATA	SATA_HDD_D2R_SERV0_IN_P	42
SATA_Q0D	SATA	SATA_HDD_D2R_SERV0_IN_N	42
SATA_Q0D	SATA	SATA_HDD_R2D_SERV0_OUT_P	42
SATA_Q0D	SATA	SATA_HDD_R2D_SERV0_OUT_N	42
THERM_L101_550	THERM	CPUMTHERM_D2_P	51
THERM_L101_550	THERM	CPUMTHERM_D2_N	51
THERM_L101_550	THERM	CPU_THERM_P	9 51
THERM_L101_550	THERM	CPU_THERM_N	9 51
THERM_L101_550	THERM	T29_THERM_P	34 51
THERM_L101_550	THERM	T29_THERM_N	51
THERM_L101_550	THERM	T29THERM_D2_P	51
THERM_L101_550	THERM	T29THERM_D2_N	51
ISNS_HS_COMPUTING_N	ISNS	ISNS_HS_COMPUTING_N	50
ISNS_HS_COMPUTING_P	ISNS	ISNS_HS_COMPUTING_P	50
ISNS_HS_OTHER_N	ISNS	ISNS_HS_OTHER_N	50
ISNS_HS_OTHER_P	ISNS	ISNS_HS_OTHER_P	50
CPUVCCIOS0_CS_N	CPUVCCIOS0	CPUVCCIOS0_CS_N	49 70
CPUVCCIOS0_CS_P	CPUVCCIOS0	CPUVCCIOS0_CS_P	49 70
CPUIMVP_ISNS1_P	CPUIMVP	CPUIMVP_ISNS1_P	49 69 69
CPUIMVP_ISNS1_N	CPUIMVP	CPUIMVP_ISNS1_N	49 69
CPUIMVP_ISNS2_P	CPUIMVP	CPUIMVP_ISNS2_P	49 69 69
CPUIMVP_ISNS2_N	CPUIMVP	CPUIMVP_ISNS2_N	49 69
CPUIMVP_ISNS1G_P	CPUIMVP	CPUIMVP_ISNS1G_P	49 69
CPUIMVP_ISNS1G_N	CPUIMVP	CPUIMVP_ISNS1G_N	49 69
CPUIMVP_ISUM_R_P	CPUIMVP	CPUIMVP_ISUM_R_P	49
CPUIMVP_ISUM_R_N	CPUIMVP	CPUIMVP_ISUM_R_N	49
CPUIMVP_ISUMG_R_P	CPUIMVP	CPUIMVP_ISUMG_R_P	49
CPUIMVP_ISUMG_R_N	CPUIMVP	CPUIMVP_ISUMG_R_N	49
CPUIMVP_ISNS_P	CPUIMVP	CPUIMVP_ISNS_P	49
CPUIMVP_ISNS_N	CPUIMVP	CPUIMVP_ISNS_N	49
VCCSAS0_CS_P	VCCSAS0	VCCSAS0_CS_P	65
VCCSAS0_CS_N	VCCSAS0	VCCSAS0_CS_N	65
CPUIMVP_ISUMG_P	CPUIMVP	CPUIMVP_ISUMG_P	68 69
CPUIMVP_ISUMG_N	CPUIMVP	CPUIMVP_ISUMG_N	68 69
ISNS_CPU_N	ISNS	ISNS_CPU_N	60
ISNS_CPU_P	ISNS	ISNS_CPU_P	60
ISNS_HDD_N	ISNS	ISNS_HDD_N	60
ISNS_HDD_P	ISNS	ISNS_HDD_P	60
ISNS_HDD_R_N	ISNS	ISNS_HDD_R_N	60
ISNS_HDD_R_P	ISNS	ISNS_HDD_R_P	60
ISNS_LACBELT_N	ISNS	ISNS_LACBELT_N	60
ISNS_LACBELT_P	ISNS	ISNS_LACBELT_P	60
ISNS_ODD_N	ISNS	ISNS_ODD_N	60
ISNS_ODD_P	ISNS	ISNS_ODD_P	60
ISNS_ODD_R_N	ISNS	ISNS_ODD_R_N	60
ISNS_ODD_R_P	ISNS	ISNS_ODD_R_P	60
ISNS_P1V8GPU_N	ISNS	ISNS_P1V8GPU_N	60
ISNS_P1V8GPU_P	ISNS	ISNS_P1V8GPU_P	60
ISNS_P1V8GPU_R_N	ISNS	ISNS_P1V8GPU_R_N	60
ISNS_P1V8GPU_R_P	ISNS	ISNS_P1V8GPU_R_P	60
LVDS_CONN_A_CLK_P_N	LVDS	LVDS_CONN_A_CLK_P_N	6 74
LVDS_CONN_A_CLK_P_P	LVDS	LVDS_CONN_A_CLK_P_P	6 74

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N
	1T01_DIFFPAIR		CHGR_CSI_R_P
	1T01_DIFFPAIR		CHGR_CSI_R_N
	1T01_DIFFPAIR		CHGR_CSO_R_P
	1T01_DIFFPAIR		CHGR_CSO_R_N
(HSR_EXTA)	HSR_85D	HSR	USB2_EXTA_MIXED_P
(HSR_EXTA)	HSR_85D	HSR	USB2_EXTA_MIXED_N
(HSR_EXTA)	HSR_85D	HSR	USB2_LT1_P
(HSR_EXTA)	HSR_85D	HSR	USB2_LT1_N
	HSR_85D	HSR	CONN_USB2_ST_P
	HSR_85D	HSR	CONN_USB2_ST_N
	HSR_85D	HSR	USB_LT2_P
	HSR_85D	HSR	USB_LT2_N
	DP_85D	DP_AUXCH_C_P	DP_IG_AUX_CH_C_P
	DP_85D	DP_AUXCH_C_N	DP_IG_AUX_CH_C_N
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_SUB_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_SUB_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_L_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_L_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_R_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SSM2315_R_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_N_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_P_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO1_N_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO1_P_R
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_N_L
AUD_DIFF	1T01_DIFFPAIR	AUDIO	AUD_LO2_P_L
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INL_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INL_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INR_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INR_N
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P
AUD_DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N
	HSR_85D	HSR	USB_TPAD_R_P
	HSR_85D	HSR	USB_TPAD_R_N
	SR_POWER	SR_POWER	PP1V3_85
	SR_POWER	SR_POWER	PP1V3_80
	SR_POWER	SR_POWER	PP1V5_SRS0
	GND	GND	GND

SYNC MASTER=ANNE K90I SYNC DATE=06/08/2011

Project Specific Constraints

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL. OR MM)	ALLEGRO VERSION
TOP, ISL3, ISL4, ISL9, ISL10, ISL11, ISL12, ISL13, ISL14, ISL15, ISL16, ISL17, ISL18, ISL19, ISL20, ISL21, ISL22, ISL23, ISL24, ISL25, ISL26, ISL27, ISL28, ISL29, ISL30, ISL31, ISL32, ISL33, ISL34, ISL35, ISL36, ISL37, ISL38, ISL39, ISL40, ISL41, ISL42, ISL43, ISL44, ISL45, ISL46, ISL47, ISL48, ISL49, ISL50, ISL51, ISL52, ISL53, ISL54, ISL55, ISL56, ISL57, ISL58, ISL59, ISL60, ISL61, ISL62, ISL63, ISL64, ISL65, ISL66, ISL67, ISL68, ISL69, ISL70, ISL71, ISL72, ISL73, ISL74, ISL75, ISL76, ISL77, ISL78, ISL79, ISL80, ISL81, ISL82, ISL83, ISL84, ISL85, ISL86, ISL87, ISL88, ISL89, ISL90, ISL91, ISL92, ISL93, ISL94, ISL95, ISL96, ISL97, ISL98, ISL99, ISL100				NO_TPP, NOA			MM	16.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	+50_OHM_SE	+50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	-DEFAULT	-DEFAULT	10 MM	-DEFAULT	-DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.080 MM	0.080 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	-STANDARD	-STANDARD	-STANDARD
40_OHM_SE	ISL3, ISL4, ISL9	Y	0.126 MM	0.126 MM	-STANDARD	-STANDARD	-STANDARD
40_OHM_SE	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP, BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SE	ISL10	N	0.145 MM	0.1 MM	-STANDARD	-STANDARD	-STANDARD
37_OHM_SE	ISL3, ISL4, ISL9	Y	0.145 MM	0.1 MM	-STANDARD	-STANDARD	-STANDARD
37_OHM_SE	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
274_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.2 MM			
274_OHM_SE	*	Y	0.235 MM	0.2 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
72_OHM_DIFF	ISL3, ISL4, ISL9	Y	0.140 MM	0.140 MM	0.190 MM	0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140 MM	0.140 MM	0.190 MM	0.190 MM	0.190 MM
72_OHM_DIFF	TOP, BOTTOM	Y	0.175 MM	0.175 MM	0.200 MM	0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.1 MM	0.170 MM	0.170 MM	0.170 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.1 MM	0.170 MM	0.170 MM	0.170 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.1 MM	0.190 MM	0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.091 MM	0.091 MM	0.180 MM	0.180 MM	0.180 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.091 MM	0.091 MM	0.180 MM	0.180 MM	0.180 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.111 MM	0.111 MM	0.200 MM	0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.076 MM	0.076 MM	0.250 MM	0.250 MM	0.250 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.076 MM	0.076 MM	0.250 MM	0.250 MM	0.250 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM	0.200 MM	0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.070 MM	0.070 MM	0.330 MM	0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.070 MM	0.070 MM	0.330 MM	0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM	0.250 MM	0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP, BOTTOM	Y	0.145 MM	0.145 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	-STANDARD	-STANDARD	-STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	-STANDARD	-STANDARD	-STANDARD	-STANDARD	-STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM	0.180 MM	0.180 MM	0.180 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM	0.180 MM	0.180 MM	0.180 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM	0.190 MM	0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	-DEFAULT	?
BGA_P1MM	*	-DEFAULT	?
BGA_P2MM	*	-DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	-STANDARD	-STANDARD	-STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF	+85_OHM_DIFF
85_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM	0.125 MM	0.125 MM	0.125 MM
85_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM	0.125 MM	0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF	+90_OHM_DIFF
90_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM	0.125 MM	0.125 MM	0.125 MM
90_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM	0.125 MM	0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF	+100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM	0.125 MM	0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM	0.125 MM	0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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