1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE

Apple Inc.

Jun 23 2009

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Wed Jun 3 11:09:19 2009

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DRAWING NUMBER | SIZE D

REVISION 16.0.0

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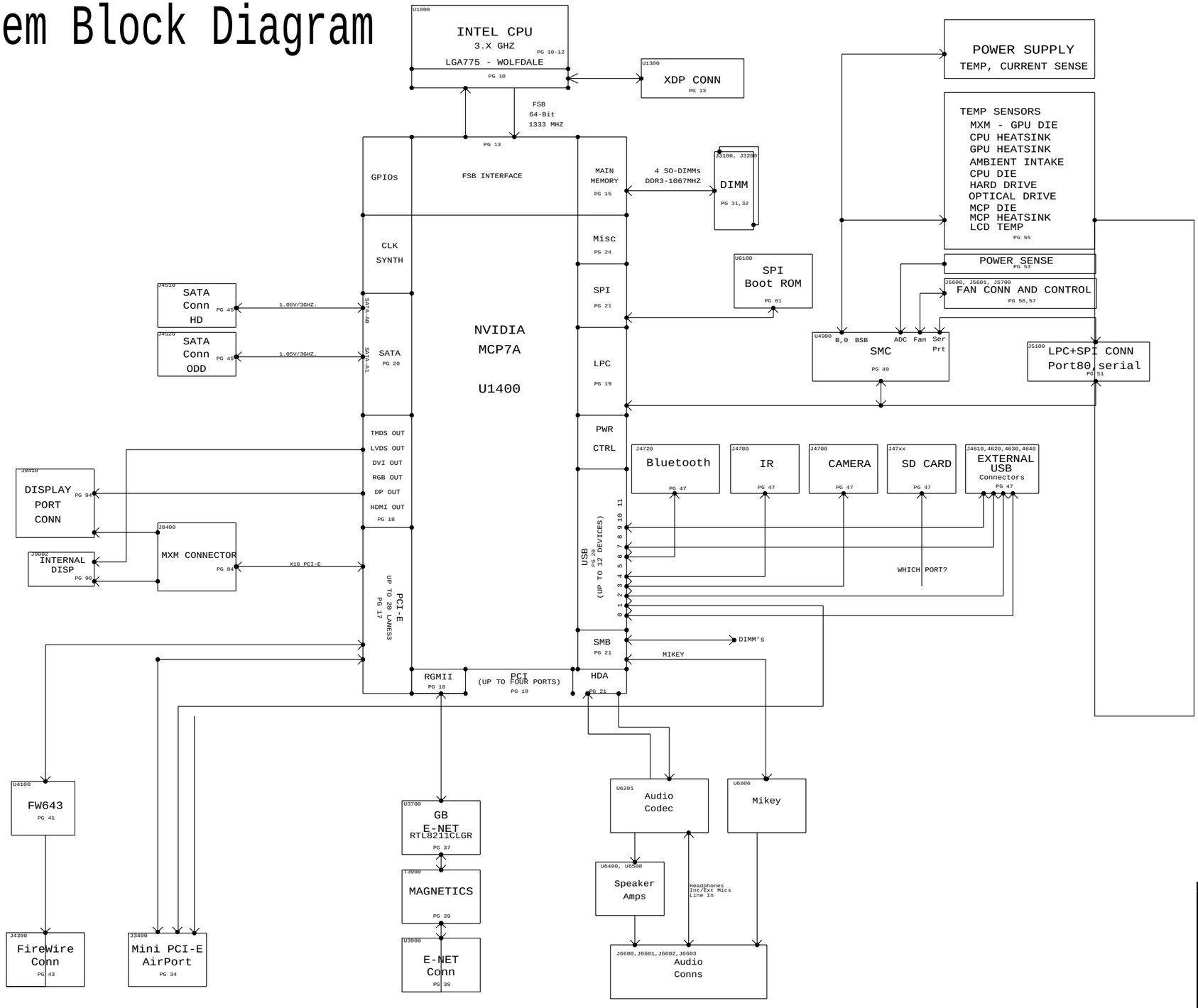
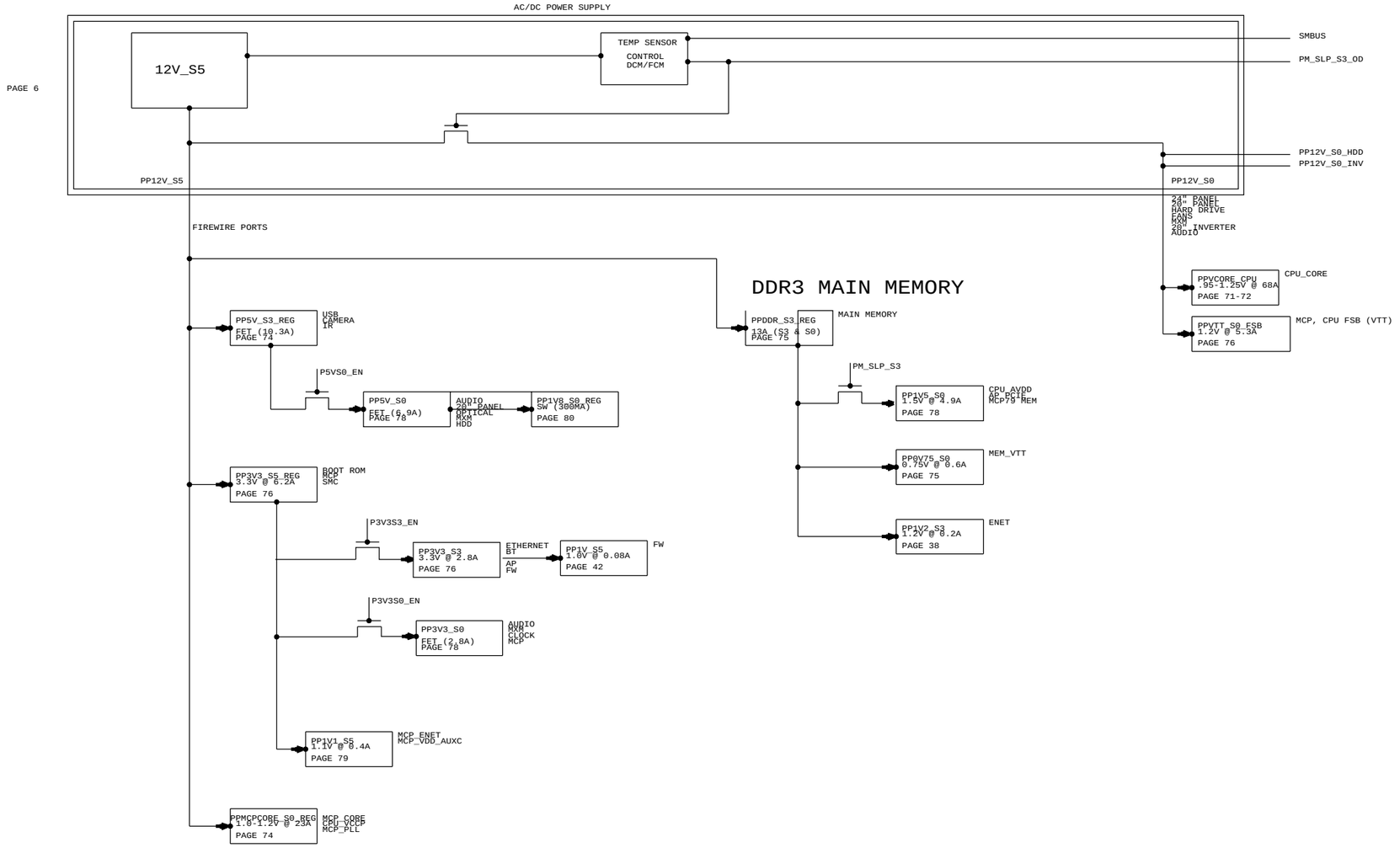
System Block Diagram



PAGE TITLE	System Block Diagram
	Apple Inc.
DRAWING NUMBER	
SIZE	D
REVISION	16.0.0
BRANCH	
PAGE	2 OF 110
SHEET	



PAGE TITLE

Power Block Diagram

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DRAWING NUMBER

SIZE D

REVISION 16.0.0

BRANCH

PAGE 3 OF 110

SHEET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
820-2507	1	PCBF,MLB	MLB1		

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

PAGE TITLE: BOM Configuration

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DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

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PAGE: 4 OF 110

SHEET

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PAGE TITLE

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DRAWING NUMBER

SIZE D

REVISION 16.0.0

BRANCH

PAGE 5 OF 110

SHEET

EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

=SMB_ACDC_SCL
=PP5V_S0_SATA
PP12V_S5
LCD_PWM
=SMB_ACDC_SDA
PP12V_S0
LCD_BKL_ON

C623 10UF 10% 10V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
PM_SLPS3_BUF2_L
Q610 2N7002 SOT23-HF1
C600 0.001UF 10% 50V X7R 402

PP3V3_S3
R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT LED605 GREEN-3.6MCD 2.0X1.25MM-SM

PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:1

PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:2
CORE_VOLTAGES_ON
ALL_SYS_PWRGD_R
Q602 2N7002DW-X-G SOT-363

PP3V3_S0
R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
LED604 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM_GOOD
Q602 2N7002DW-X-G SOT-363

PP3V3_S0
R603 1K 5% 1/16W MF-LF 402
LCD_SHOULD_ON
LED603 GREEN-3.6MCD 2.0X1.25MM-SM SILKSCREEN:4
VIDEO_ON_L
sourced from buffer on csa 90

"S0" RAILS
ONLY ON IN RUN

PPVTT_S0_DDR_LDO
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVTT_S0_VTTCLAMP

PPVCORE_S0_CPU
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_CPU

PPMCPCORE_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.05V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVCORE_S0_MCP
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PLL_UF
=PP1V05_S0_MCP_SATA_DVDD0
=PP1V05_S0_MCP_HDMI_VDD_R

PPVTT_S0_FSB_REG
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PPVTT_S0_CPU
=PPVTT_S0_FSB_CPU
=PPVTT_S0_XDP
=PP1V05_S0_MCP_FSB

PP1V5_S0
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V5_S0_CPU_VCCPLL
=PP1V8R1V5_S0_MCP_MEM
=PP1V5_S0_AUD_DIG
=PP1V5_FWRS0_FWXIO

PP1V8_S0_REG
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3R1V8_S0_MCP_IFP_VDD_R
=PP1V8_S0_PGCMP

PP3V3_S0
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S0_FAN
=PP3V3_S0_MCP
=PP3V3_S0_MCP_VPLL_UF
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_MCP_PLL_UF
=PPSPD_S0_MEM_A
=PPSPD_S0_MEM_B
=PP3V3_S0_VRD
=PP3V3_S0_AUDIO
=PP3V3R1V5_S0_MCP_HDA
=PP3V3_S0_SMBUS
=PP3V3_S0_SMC_LS
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_SMC_MGMT
=PP3V3_S0_DPCONN
=PP3V3_S0_TSENS
=PP3V3_S0_MXM
=PP3V3_S0_XDP
=PP3V3_S0_ODD
=PP3V3_S0_SATALED
=PP3V3_S0_SMC
=PP3V3_S0_PWRCTL
=PP3V3_S0_MCPTHMSNS
=PP3V3_S0_VIDEO
=PP3V3_FW_FWPHY
=PP3V3_FWRS0_FWXIO
=PP3V3_S0_DP

PP5V_S0
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S0_LPCPLUS
=PP5V_S0_AUDIO
=PP5V_S0_SATA
=PP5V_S0_MXM
=PP5V_S0_VRD
=PP5V_S0_DP_AUX_MUX
=PP5V_S0_ISENSE
=PP5V_S0_PWRCTL

PP12V_S0
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S0_FAN
=PP12V_S0_AUDIO_SPKRAMP
=PP12V_S0_VRD
=PPV_S0_MXM_PWR
=PPVIN_S0_PPVTT_FSB
=PP12V_S0_LCD
=PPVIN_S0_MCPCORE

"S3" RAILS
ON IN RUN AND SLEEP

PPDDR_S3_REG
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PPDDR_MEM
MAX_NECK_LENGTH=3 MM
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B
=PP1V5_S3_MEMRESET
=PPDDR_S3_S0FET
=PPDDR_S3_PGCMP

PPVTT_S3_DDR_BUF
MAKE_BASE=TRUE
VOLTAGE=0.75V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 mm
=PPVTT_S3_DDR_BUF

PP3V3_S3
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S3_MINI
=PP3V3_S3_BT
=PP3V3_S3_VREFMRGN
=PP3V3_S3_SDCARD
=PP3V3_S3_MCP_GPIO
=PP3V3_S3_SMC
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_MCPREG

PP5V_S3_REG
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S3_DDRREG
=PP5V_S3_USB
=PP5V_S3_VTTCLAMP
=PP5V_S3_PWRCTL
=PP5V_S3_S0FET
=PP5V_S3_MCPREG
=PP5V_S3_CAMERA
=PP5V_S3_IR
=PP5V_S3_1V8

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP1V1_S5_REG
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V05_S5_MCP_VDD_AUXC
=PP1V1_S5_ENET_FET

PP3V3_S5_REG
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP3V3_S5_MCP
=PP3V3_S5_MCP_GPIO
=PP3V3_S5_SMC
=PP3V3_S5_ROM
=PP3V3_S5_RTC_D
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMBUS_SMC_BSA
=PP3V3_S5_SMCUSBMUX
=PP3V3_S5_MEMRESET
=PP3V3_S5_P1V1S5
=PP3V3_S5_PWRCTL
=PP3V3_S5_S3FET
=PP3V3_S5_S0FET
=PP3V3_S5_ENET_FET

PP5V_S5_LDO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP5V_S5_AVREF

PP12V_S5
MAKE_BASE=TRUE
VOLTAGE=12V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP12V_S5_FW
=PPVIN_S5_DDRREG
=PPVIN_S5_P3V3S5
=PPVIN_S5_P5VS3
=PP12V_S5_REG
=PP12V_S5_PWRCTL

GND RAILS

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
VOLTAGE=0V
NET_SPACING_TYPE=AUDIO
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

PAGE TITLE: Power Conn / Alias

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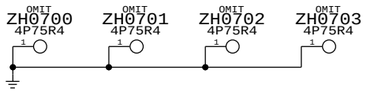
DRAWING NUMBER
SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 6 OF 110
SHEET

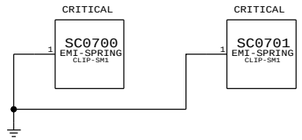
CPU Heatsink

4mm Plated Holes (998-0850)



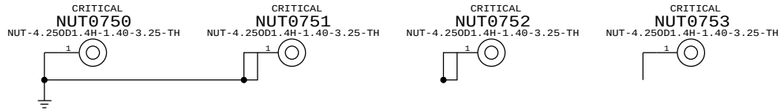
MCP Heatsink

EMC Springs (870-1125)



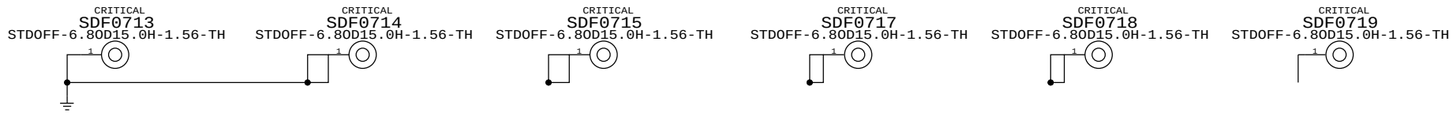
DIMM CONNECTOR NUTS

Nuts (805-9582)



Rear Cover

Standoffs (860-1255)



Backer Plate

Nuts (835-0269)

PAGE TITLE

Holes

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DRAWING NUMBER

SIZE
D

REVISION
16.0.0

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PAGE
7 OF 110

SHEET

NC ON UNUSED ALIASES

18	MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN	MAKE_BASE=TRUE NO_TEST=TRUE
18	MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_MCP_RGB_HSYNC	NC_MCP_RGB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_MCP_RGB_VSYNC	NC_MCP_RGB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<31..15>	NC_PCI_AD<31..15>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_C_BE_L<1..0>	NC_PCI_C_BE_L<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_LPC_DRQ0_L	NC_LPC_DRQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MCP_BUF_SIO_CLK	NC_MCP_BUF_SIO_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_ENET_PWRDWN_L	NC_ENET_PWDWN_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MCP_KBDRSTIN_L	NC_MCP_KBDRSTIN_L	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_MCP_GPIO_18	NC_MCP_GPIO_18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_C_BE_L<3>	NC_PCI_C_BE_L<3>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_CLK0	NC_PCI_CLK0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_GNT0_L	NC_MCP_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTY_L	NC_PCI_INTY_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_PRSNT_L	NC_PCIE_EXCARD_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PE4_CLKREQ_L	NC_PE4_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_MINI_N	NC_USB_MINI_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_MINI_P	NC_USB_MINI_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_EXCARD_N	NC_USB_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_EXCARD_P	NC_USB_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
21	ODD_PWR_EN_L	NC_ODD_PWR_EN_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
17	EXCARD_CLKREQ_L	NC_EXCARD_CLKREQ_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<12..10>	NC_PCI_AD<12..10>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCI_AD<8>	NC_PCI_AD<8>	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CP	NC_PCIE_PE4_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_D2RP	NC_PCIE_PE4_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
17	TP_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
17	PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_TPAD_N	NC_USB_TPAD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_TPAD_P	NC_USB_TPAD_P	MAKE_BASE=TRUE NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

UNUSED MEMORY SIGNALS

15	TP_MEM_A_CLK2P	NC_MEM_A_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_A_CLK5P	NC_MEM_A_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_A_CLK5N	NC_MEM_A_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_B_CLK2P	NC_MEM_B_CLK2P	MAKE_BASE=TRUE NO_TEST=TRUE
15	TP_MEM_B_CLK2N	NC_MEM_B_CLK2N	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_B_CLK5P	NC_MEM_B_CLK5P	MAKE_BASE=TRUE NO_TEST=TRUE
16	TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GMUX JTAG FROM MCP

17	GMUX_JTAG_TCK_L	NC_GMUX_JTAG_TCK_L	MAKE_BASE=TRUE NO_TEST=TRUE
17	GMUX_JTAG_TDO	NC_GMUX_JTAG_TDO	MAKE_BASE=TRUE NO_TEST=TRUE
19	GMUX_JTAG_TDI	NC_GMUX_JTAG_TDI	MAKE_BASE=TRUE NO_TEST=TRUE
19	GMUX_JTAG_TMS	NC_GMUX_JTAG_TMS	MAKE_BASE=TRUE NO_TEST=TRUE

PAGE TITLE: UNUSED SIGNAL ALIAS

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DRAWING NUMBER | SIZE: D

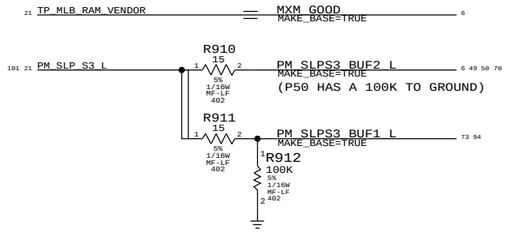
REVISION: 16.0.0

BRANCH

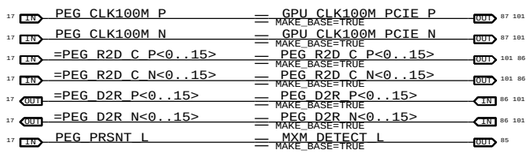
PAGE: 8 OF 110

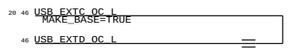
SHEET

SIGNAL ALIAS



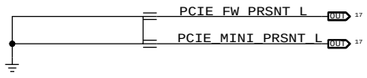
PEG Slot Support





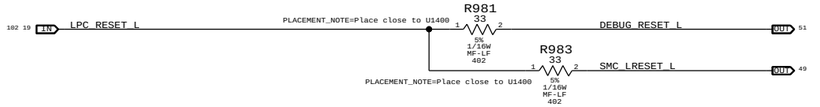
K22/K23 Use one GPIO for both ports 2&3 OC

USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD IT'S OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

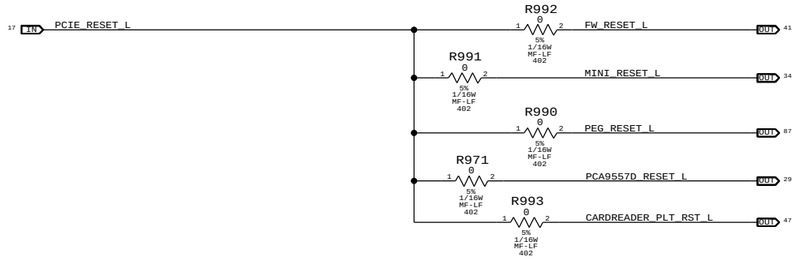


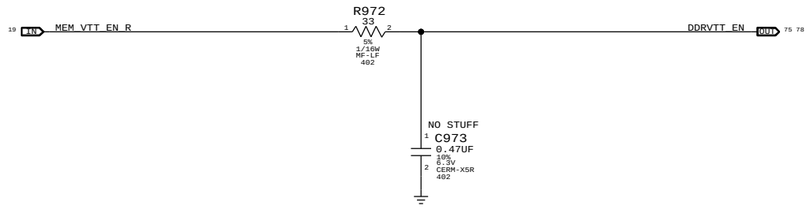
Platform Reset Connections

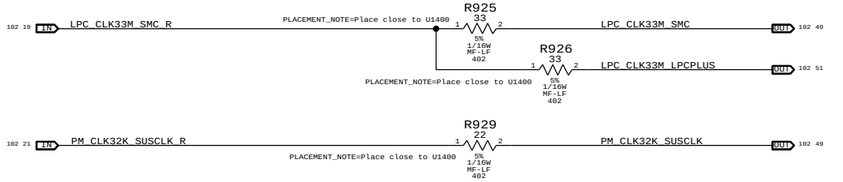
LPC Reset (Unbuffered)



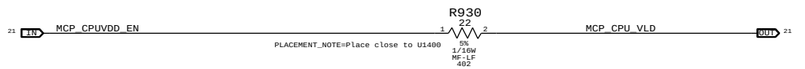
PCIE Reset (Unbuffered)

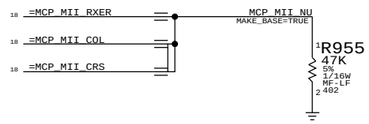






MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP





PAGE TITLE: Signal Aliases

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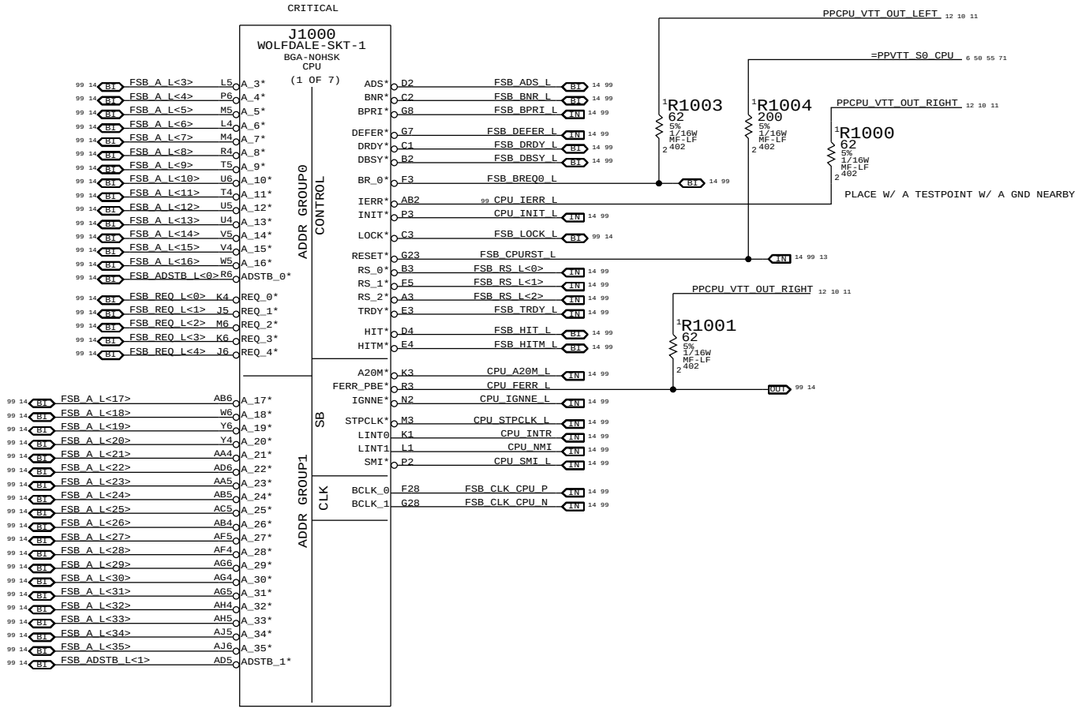
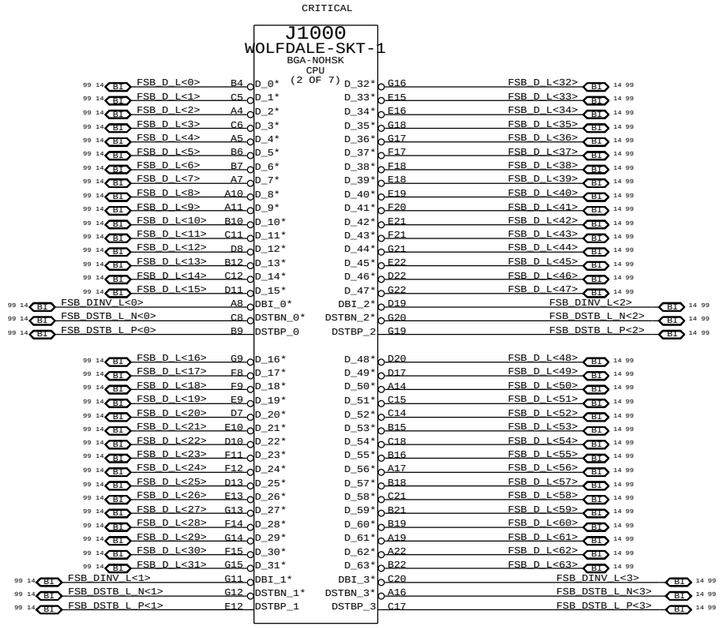
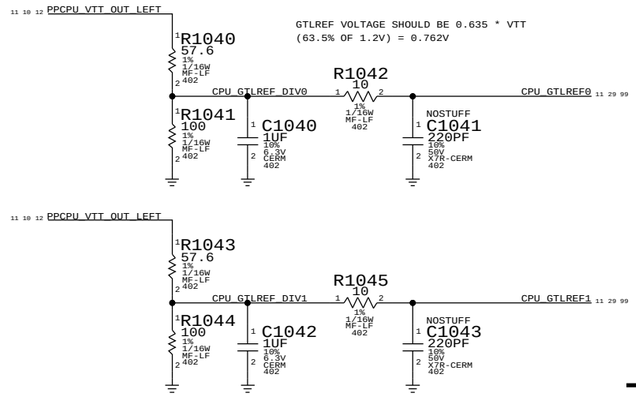
REVISION: 16.0.0
BRANCH:
PAGE: 9 OF 110
SHEET:





CPU GTLREF



PAGE TITLE: CPU FSB

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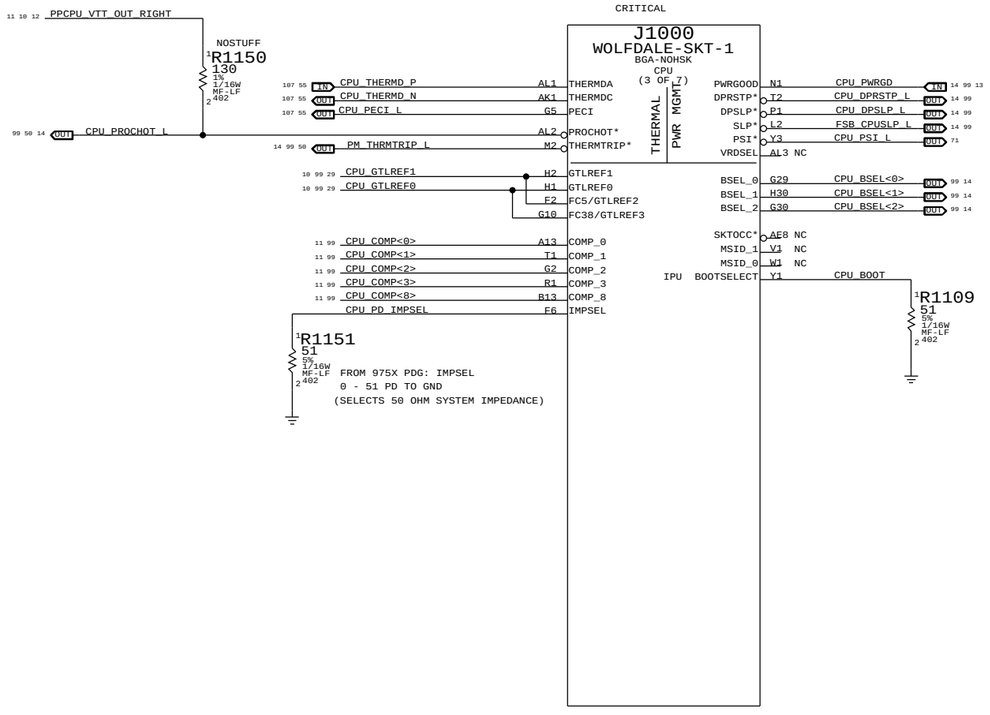
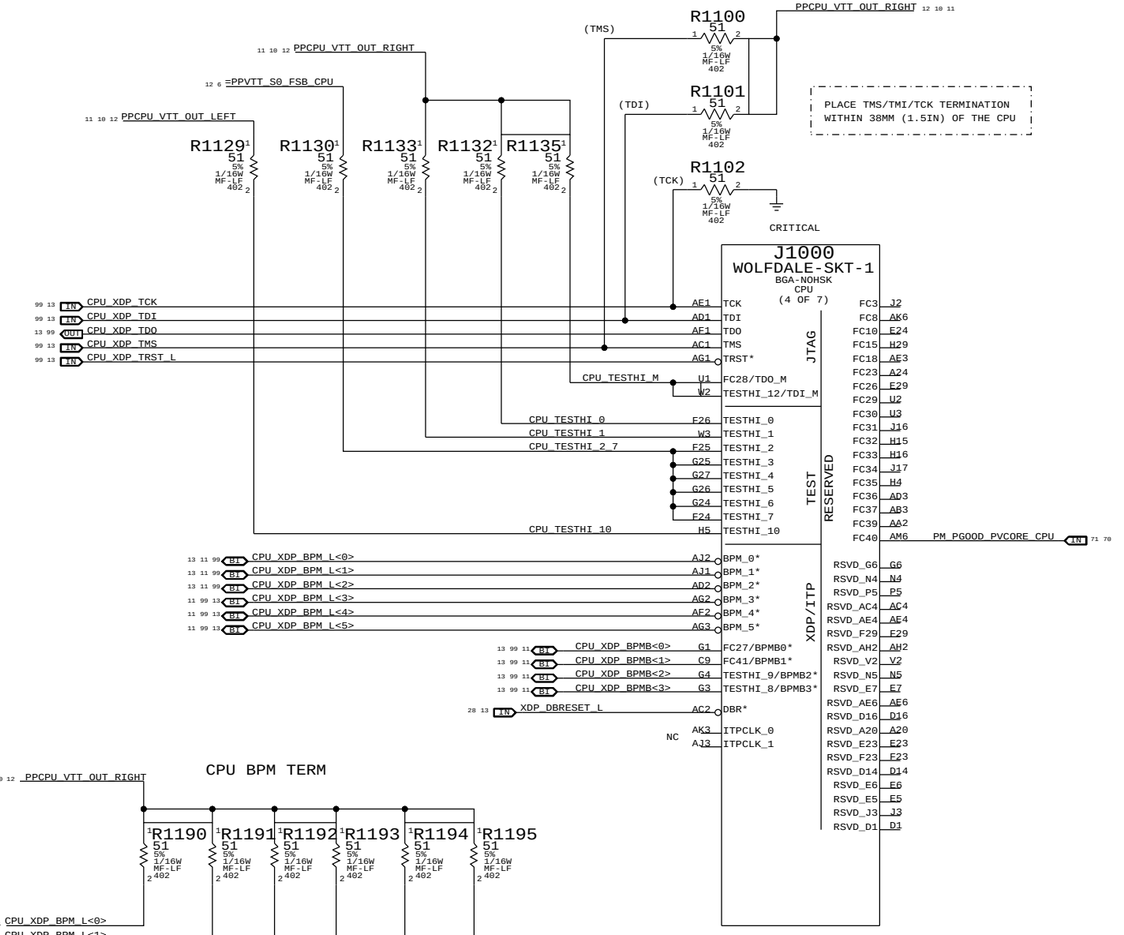
REVISION: 16.0.0

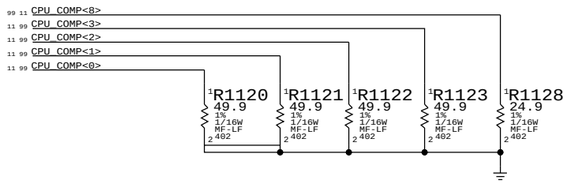
BRANCH

PAGE: 10 OF 110

SHEET







PAGE TITLE
CPU TEST & MISC.

Apple Inc.

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REVISION 16.0.0
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PAGE 11 OF 110
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POWER

THIS IS FOR OLDER CPU SUPPORT
WILL PLACE FILTER BUT NOT CONNECT FOR WOLFDALE

CONROE
~125MA CURRENT

=PPVCORE_S0_CPU

=PPVTT_S0_FSB_CPU
L1210 FERR-120-OHM-0.2A 0603
R1210 0 5% 1/10W MF-LF 603
R1211 0 5% 1/10W MF-LF 603

CPU_VCCIOPLL — VOLTAGE=1.2V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
CPU_VCCA — VOLTAGE=1.2V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM
CPU_VSSA — VOLTAGE=0V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm NET_SPACING_TYPE=PWR MAX_NECK_LENGTH=3 MM

CPU_VCCA_FLT
C1210 22UF 20% 6.3V CERM-X5R 805-3
C1213 10UF 20% 6.3V X5R 603
NOSTUFF C1211 1UF 10% 6.3V CERM 402
NOSTUFF C1212 1UF 10% 6.3V CERM 402

CRITICAL
J1000 WOLFDALE-SKT-1
BGA-NOHSK
CPU
(7 OF 7)

VID PULLUPS WITH VREG

CPU_VID<0>	AM2	VID_0
CPU_VID<1>	AL5	VID_1
CPU_VID<2>	AM3	VID_2
CPU_VID<3>	AL6	VID_3
CPU_VID<4>	AK4	VID_4
CPU_VID<5>	AL4	VID_5
CPU_VID<6>	AM5	VID_6
CPU_VID<7>	AM7	VID_7
CPU_VCCA	A23	VCCA
CPU_VSSA	B23	VSSA
CPU_VCCIOPLL	C23	VCCIOPLL
	D23	VCCPLL
CPU_VCC_SENSE	AN3	VCC_SENSE
CPU_VCC_PKG_SENSE_P	AN5	VCC_MB_REGULATION
CPU_VID_SELECT	AN7	VID_SELECT
TP_CPU_VSS_SENSE	AN4	VSS_SENSE
CPU_VCC_PKG_SENSE_N	AN6	VSS_MB_REGULATION

=PPVTT_S0_FSB_CPU

	A25	VTT_A25
	A26	VTT_A26
	A27	VTT_A27
	A28	VTT_A28
	A29	VTT_A29
	A30	VTT_A30
	B25	VTT_B25
	B26	VTT_B26
	B27	VTT_B27
	B28	VTT_B28
	B29	VTT_B29
	B30	VTT_B30
	C25	VTT_C25
	C26	VTT_C26
	C27	VTT_C27
	C28	VTT_C28
	C29	VTT_C29
	C30	VTT_C30
	D25	VTT_D25
	D26	VTT_D26
	D27	VTT_D27
	D28	VTT_D28
	D29	VTT_D29
	D30	VTT_D30
PPCPU_VTT_OUT_RIGHT	AA1	VTT_OUT_RIGHT
PPCPU_VTT_OUT_LEFT	J1	VTT_OUT_LEFT
TP_VTT_SEL	F27	VTT_SEL

VCCP

	AC8	
	AD23	
	AD24	
	AD25	
	AD26	
	AD27	
	AD28	
	AD29	
	AD30	
	AD8	
	AE11	
	AE12	
	AE14	
	AE15	
	AE18	
	AE19	
	AE21	
	AE22	
	AE23	
	AE9	
	AF11	
	AF12	
	AF14	
	AF15	
	AF18	
	AF19	

VCCP

	J25	
	J26	
	J27	
	J28	
	J29	
	J30	
	J8	
	J9	
	K23	
	K24	
	K25	
	K26	
	K27	
	K28	
	K29	
	K30	
	K8	
	L8	
	M23	
	M24	
	M25	
	M26	
	M27	
	M28	
	M29	
	M30	
	M8	
	N23	
	N24	
	N25	
	N26	
	N27	
	N28	
	N29	
	N30	
	N8	
	P8	
	R8	
	T23	
	T24	
	T25	
	T26	
	T27	
	T28	
	T29	
	T30	
	T8	
	U23	
	U24	
	U25	
	U26	
	U27	
	U28	
	U29	
	U30	
	U8	
	V8	
	W23	
	W24	
	W25	
	W26	
	W27	
	W28	
	Y27	
	Y26	
	Y25	
	Y24	
	Y23	
	W8	
	W30	
	Y8	
	Y30	
	Y29	
	Y28	
	W29	
	AL15	
	AL8	
	AL11	
	AL12	
	AL14	

VCCP

	AF21	
	AF22	
	AF8	
	AF9	
	AG11	
	AG12	
	AG14	
	AG15	
	AG18	
	AG19	
	AG21	
	AG22	
	AG25	
	AG26	
	AG27	
	AG28	
	AG29	
	AG30	
	AG8	
	AG9	
	AH11	
	AH12	
	AH14	
	AH15	
	AH18	
	AH19	
	AH21	
	AH22	
	AH25	
	AH26	
	AH27	
	AH28	
	AH29	
	AH30	
	AH8	
	AH9	
	AJ10	
	AJ11	
	AJ12	
	AJ14	
	AJ15	
	AJ18	
	AJ19	
	AJ21	
	AJ22	
	AJ25	
	AJ26	
	AK8	
	AK9	
	AK11	
	AK12	
	AK14	
	AK15	
	AK18	
	AK19	
	AK21	
	AK22	
	AK25	
	AK26	

VCC PLL DECOUPLING

=PP1V5_S0_CPU_VCCPLL
C1280 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

PPCPU_VTT_OUT_LEFT — PPCPU_VTT_OUT_RIGHT
C1200 0.1UF 20% 10V CERM 402
C1201 0.1UF 20% 10V CERM 402

FSB VTT DECOUPLING

=PPVTT_S0_FSB_CPU
C1226 0.1UF 20% 10V CERM 402
C1234 0.1UF 20% 10V CERM 402
C1235 0.1UF 20% 10V CERM 402
C1236 0.1UF 20% 10V CERM 402
C1237 0.1UF 20% 10V CERM 402
C1238 0.1UF 20% 10V CERM 402

VCCP CORE DECOUPLING

(SEE VREG PAGE)

PPCPU_VTT_OUT_RIGHT
R1200 680 5% 1/10W MF-LF 402
CPU_VID_SELECT

CRITICAL
J1000 WOLFDALE-SKT-1
BGA-NOHSK
CPU
(5 OF 7)

A12	AG17
A15	AG20
A18	AG23
A2	AG24
A21	AG7
A6	AH1
A9	AH10
AA23	AH13
AA24	AH16
AA25	AH17
AA26	AH20
AA27	AH23
AA28	AH24
AA29	AH3
AA3	AH6
AA30	AJ10
AA6	AJ13
AA7	AJ16
AB1	AJ17
AB23	AJ20
AB24	AJ23
AB25	AJ24
AB26	AJ27
AB27	AJ28
AB28	AJ29
AB29	AJ30
AB30	AJ4
AB7	AK10
AC3	AK13
AC6	AK16
AC7	AK17
AD4	AK2
AD7	AK20
AE10	AK23
AE13	AK24
AE16	AK27
AE17	AK28
AE2	AK29
AE20	AK30
AE24	AK5
AE25	AK7
AE26	AL10
AE27	AL13
AE28	AL16
AE29	AL17
AE30	AL20
AE5	AL23
AE7	AL24
AF10	AL27
AF13	AL28
AF16	AM1
AF17	AM10
AF20	AM13
AF23	AM16
AF24	AM17
AF25	AM20
AF26	AM23
AF27	AM24
AF28	AM27
AF29	AM28
AF3	AM4
AF30	AN1
AF6	AN10
AF7	AN13
AG10	AN16
AG13	AN17
AG16	AH7
AL7	AJ7

GND — GND

CRITICAL
J1000 WOLFDALE-SKT-1
BGA-NOHSK
CPU
(6 OF 7)

AN2	H6
AN20	H7
AN23	H8
AN24	H9
AN27	J4
AN28	J7
B1	K2
B11	K5
B14	K7
B17	L23
B20	L24
B24	L25
B5	L26
B8	L27
C10	L28
C13	L29
C16	L3
C19	L30
C22	L6
C24	L7
C4	M1
C7	M7
D12	N3
D15	N6
D18	N7
D21	P23
D24	P24
D3	P25
D5	P26
D6	P27
D9	P28
E11	P29
E14	P30
E17	P4
E2	P7
E20	R2
E25	R23
E26	R24
E27	R25
E28	R26
E8	R27
F10	R28
F13	R29
F16	R30
F19	R5
F22	R7
F4	T3
F7	T6
H10	T7
H11	U7
H12	V23
H13	V24
H14	V25
H17	V26
H18	V27
H19	V28
H20	V29
H21	V3
H22	V30
H23	V6
H24	V7
H25	W4
H26	W7
H27	Y2
H28	Y5
H3	Y7

GND — GND

PAGE TITLE: CPU POWER, GND, DECAPS

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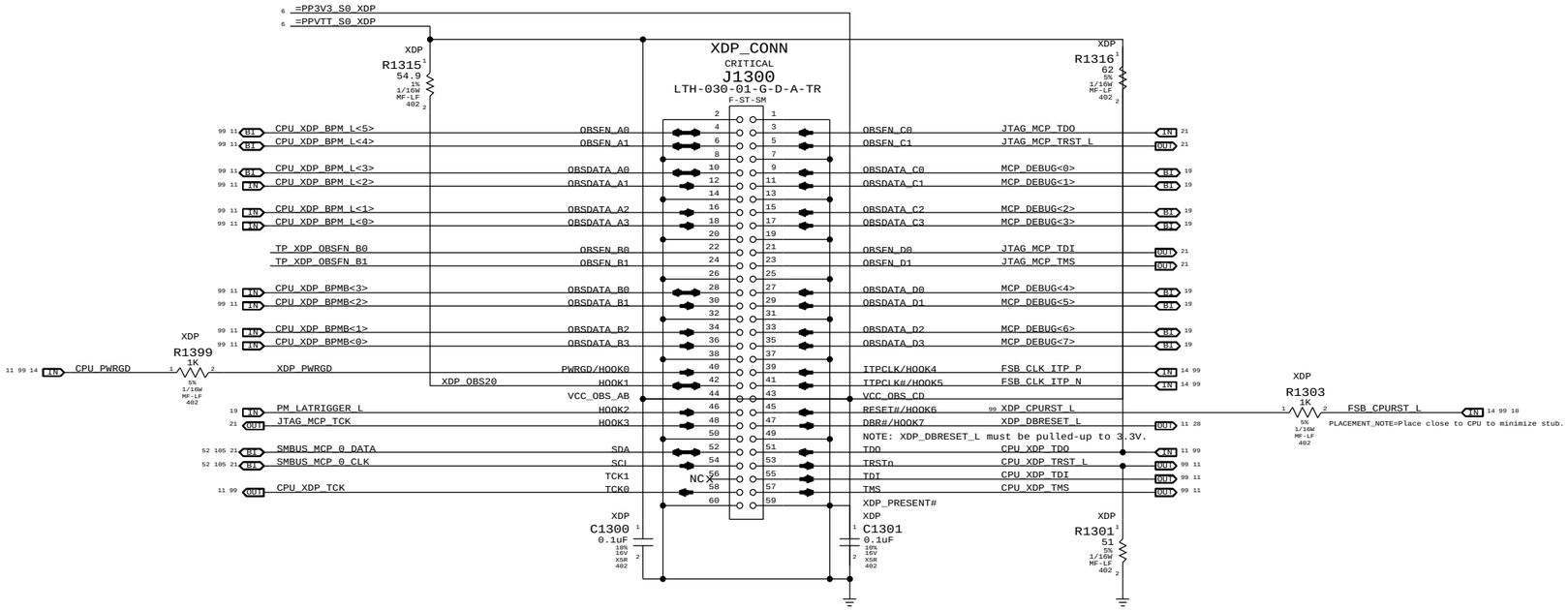
PAGE: 12 OF 110

SHEET

MCP79-specific pinout



PAGE TITLE
eXtended Debug Port (XDP)

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PAGE
13 OF 110

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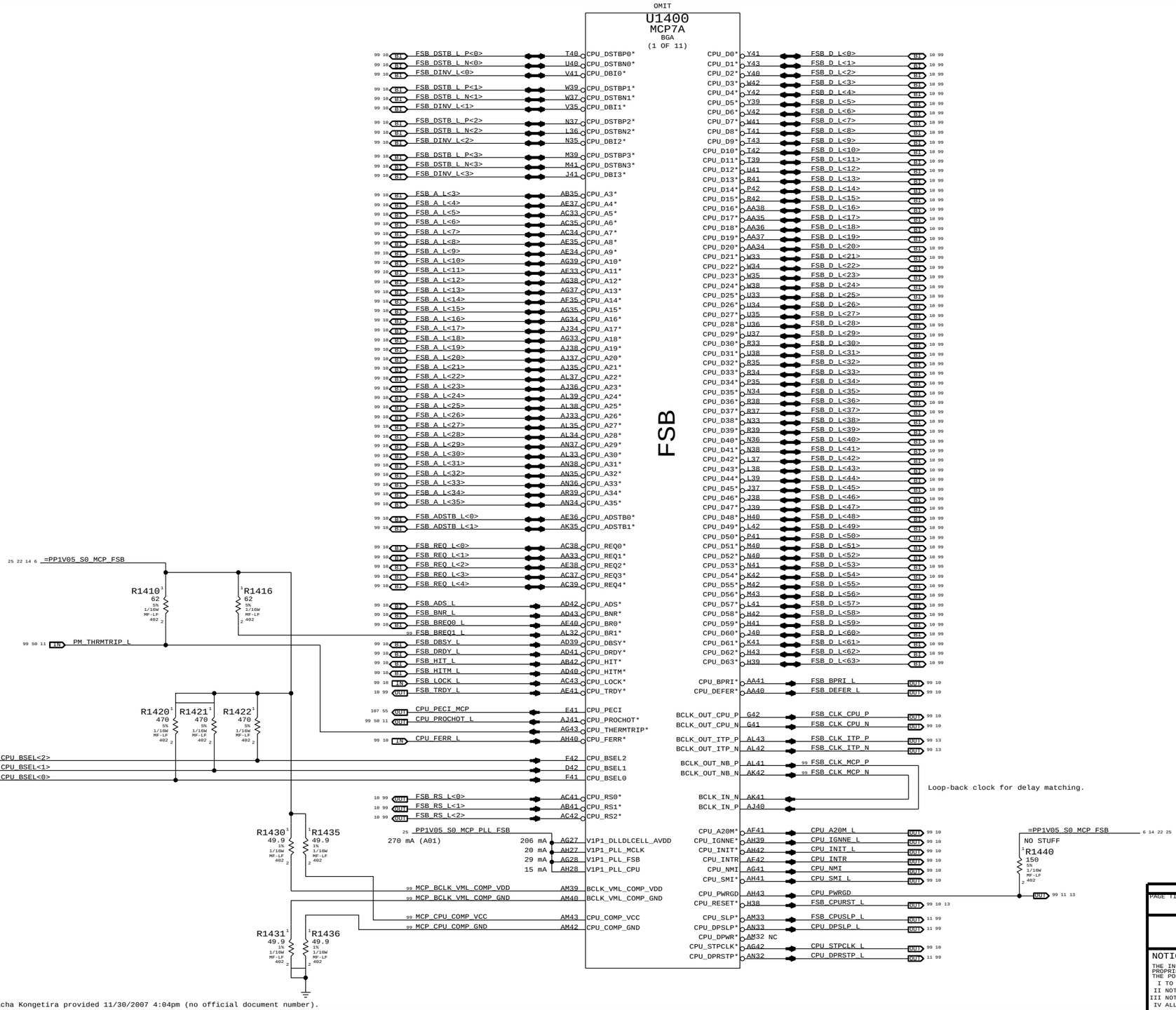

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PAGE TITLE
MCP CPU Interface

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PAGE 14 OF 110
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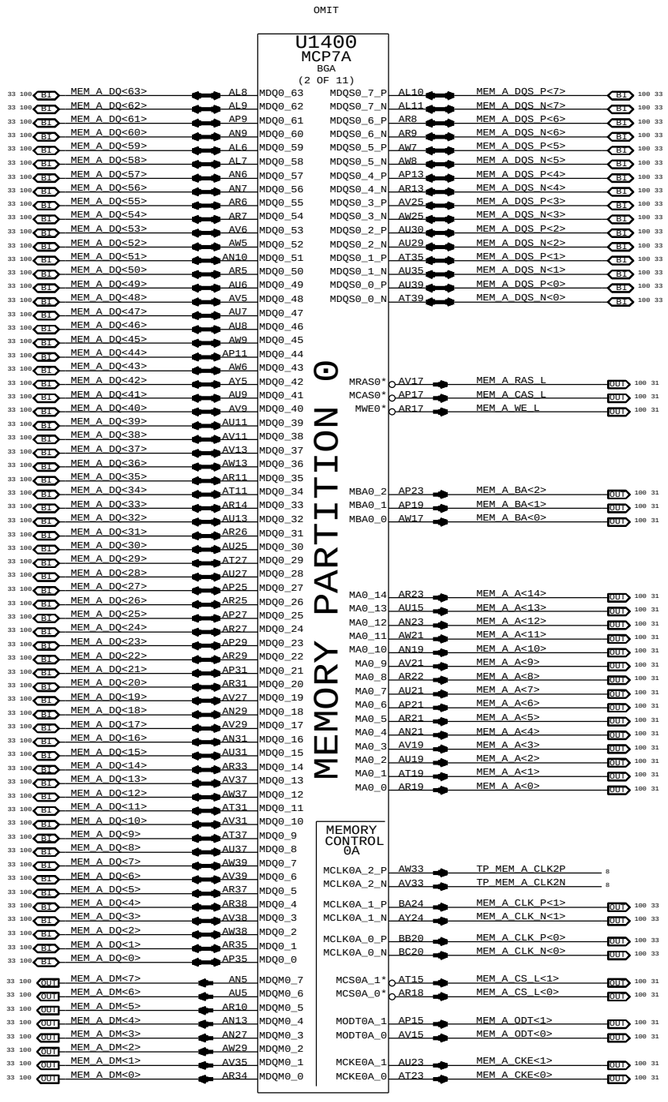

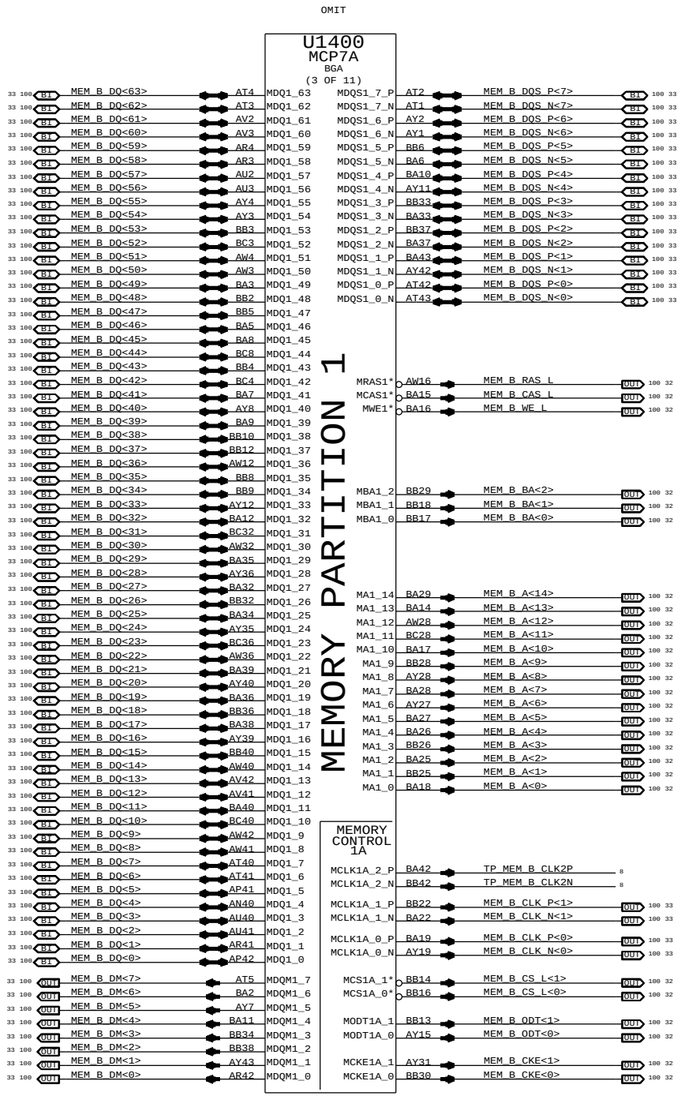

PAGE TITLE
MCP Memory Interface

Apple Inc.

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16.0.0

BRANCH

PAGE
15 OF 110

SHEET

OMIT

U1400
MCP7A
BGA
(4 OF 11)

MEMORY CONTROL 0B

8 TP_MEM_A_CLK5P	AU33	MCLK0B_2_P	
8 TP_MEM_A_CLK5N	AU34	MCLK0B_2_N	
33 100 MEM_A_CLK_P<4>	BB24	MCLK0B_1_P	
33 100 MEM_A_CLK_N<4>	BC24	MCLK0B_1_N	
33 100 MEM_A_CLK_P<3>	BA21	MCLK0B_0_P	
33 100 MEM_A_CLK_N<3>	BB21	MCLK0B_0_N	
31 100 MEM_A_CS_L<2>	AU17	MCS0B_0*	
31 100 MEM_A_CS_L<3>	AR15	MCS0B_1*	
31 100 MEM_A_ODT<2>	AN17	MODT0B_0	
31 100 MEM_A_ODT<3>	AN15	MODT0B_1	
31 100 MEM_A_CKE<2>	AV23	MCKE0B_0	
31 100 MEM_A_CKE<3>	AN25	MCKE0B_1	

MEMORY CONTROL 1B

	BA41	MCLK1B_2_P	8 TP_MEM_B_CLK5P
	BB41	MCLK1B_2_N	8 TP_MEM_B_CLK5N
	AY23	MCLK1B_1_P	100 33 MEM_B_CLK_P<4>
	BA23	MCLK1B_1_N	100 33 MEM_B_CLK_N<4>
	BA20	MCLK1B_0_P	100 33 MEM_B_CLK_P<3>
	AY20	MCLK1B_0_N	100 33 MEM_B_CLK_N<3>
	BC16	MCS1B_0*	100 32 MEM_B_CS_L<2>
	BA13	MCS1B_1*	100 32 MEM_B_CS_L<3>
	AY16	MODT1B_0	100 32 MEM_B_ODT<2>
	BC13	MODT1B_1	100 32 MEM_B_ODT<3>
	BA30	MCKE1B_0	100 32 MEM_B_CKE<2>
	BA31	MCKE1B_1	100 32 MEM_B_CKE<3>

25 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T28	V1P1_PLL_V
12 mA	U28	V1P1_PLL_DP
19 mA	U27	V1P1_PLL_CORE
39 mA	T27	V1P1_PLL_XREF_XS

MRESET0* AY32 — MCP_MEM_RESET_L (OUT 33)
TP or NC for DDR2.

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

R1610 1 40.2 1% 1/16W MF-LF 402 2

R1611 1 40.2 1% 1/16W MF-LF 402 2

109 MCP_MEM_COMP_GND	AM41	MEM_COMP_GND
109 MCP_MEM_COMP_VDD	AN41	MEM_COMP_1P8V

=PP1V8R1V5_S0_MCP_MEM 6 16 25 30
4771 mA (A01, DDR3)

	AA22	
	AP12	
	G30	
	P10	
	T10	
	T6	
	V10	
	V34	
	W5	
	AA39	
	AB22	
	AB7	
	AD22	
	AE20	
	AE24	
	AG24	
	AH35	
	AK7	
	AM28	
	AT25	
	AP30	
	AR36	
	AU10	
	F28	
	BC21	
	AY9	
	BC9	
	D34	
	F24	
	G32	
	H31	
	K7	
	M38	
	M5	
	M6	
	M7	
	M9	
	N39	
	N8	
	P33	
	P34	
	P37	
	P4	
	P40	
	P7	
	R36	
	R40	
	R43	
	R5	
	T18	
	T20	
	AK11	
	T24	
	T26	
GND		

	AM17	
	AN20	
	AN24	
	AT17	
	AP16	
	AN22	
	AP20	
	AP24	
	AV16	
	AR16	
	AR20	
	AM19	
	AR24	
	AW15	
	AP22	
	AP18	
	AU16	
	AN18	
	AU24	
	AT21	
	AY29	
	AV24	
	AM21	
	AU20	
	AU22	
	AW27	
	BC17	
	AV20	
	AY17	
	AY18	
	AM15	
	AU18	
	AY25	
	AM23	
	AV26	
	AW19	
	AW24	
	BC25	
	AL30	
	AM31	
	AM25	
	AM27	
	AM29	
	AN16	
	BC29	
V1P8_MEM_VDDP		

	T33	
	T34	
	T35	
	T37	
	T38	
	T7	
	T9	
	U18	
	U20	
	U22	
GND		

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PAGE TITLE
MCP MEMORY CNTRL & MISC

Apple Inc.

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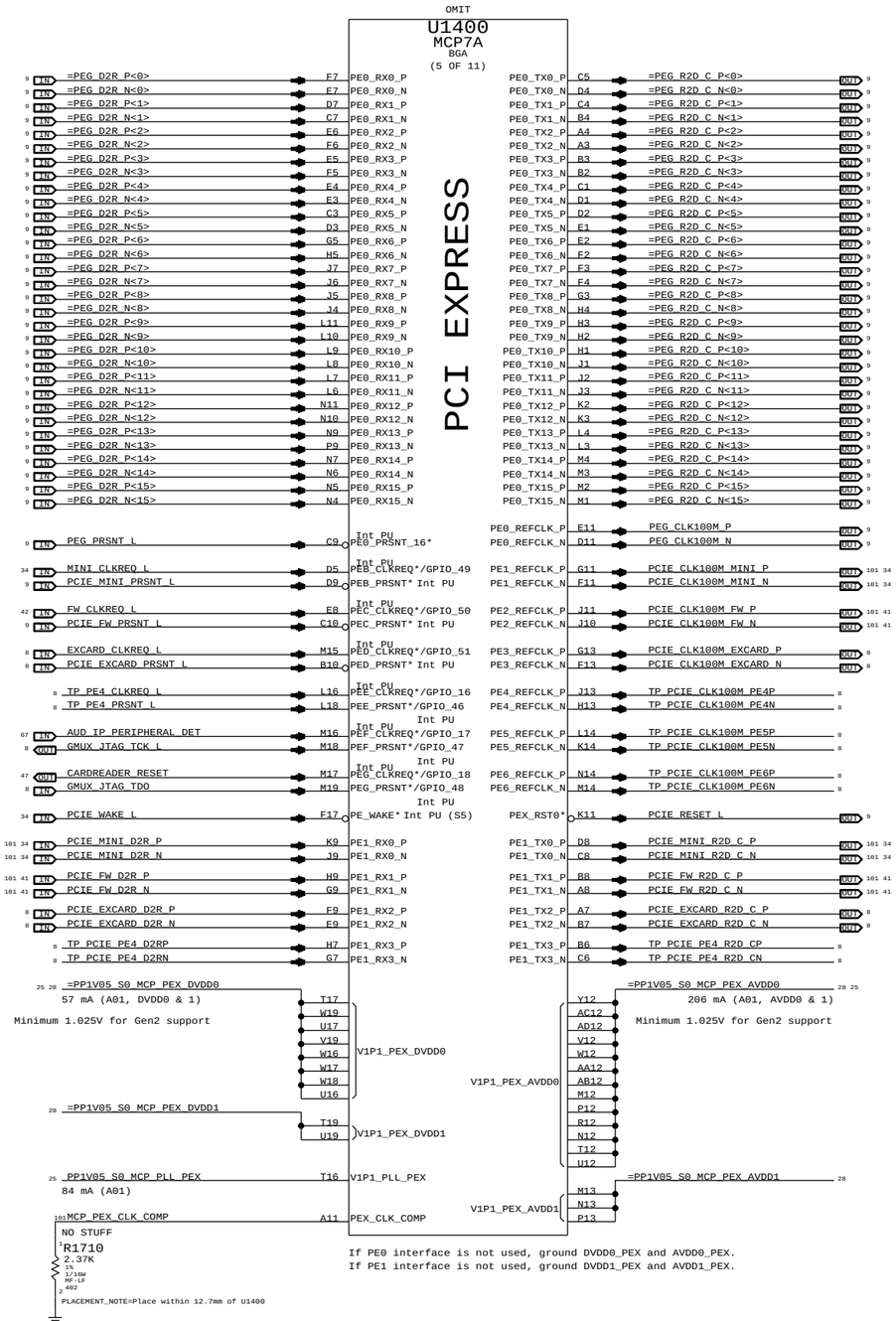
SIZE D
REVISION 16.0.0
BRANCH
PAGE 16 OF 110
SHEET



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PAGE TITLE
MCP PCIe Interfaces

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SIZE D

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16.0.0

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PAGE
17 OF 110

SHEET

OMIT

U1400
MCP7A
BGA
(6 OF 11)

LAN

ENET_RXD<0>	C23	MII_RXD0	
ENET_RXD<1>	B23	MII_RXD1	
ENET_RXD<2>	E24	MII_RXD2	
ENET_RXD<3>	A24	MII_RXD3	
ENET_CLK125M_RXCLK	A23	MII_RXCLK	
ENET_RX_CTRL	C22	MII_RXDV	
=MCP_MII_RXER	F23	MII_RXER/GPIO_36	
=MCP_MII_COL	B26	MII_COL/GPIO_20/MSMB_DATA	
=MCP_MII_CRS	B22	MII_CRS/GPIO_21/MSMB_CLK	
TP_ENET_INTR_L	J22	MII_INTR/GPIO_35	
PP1V05_ENET_MCP_PLL_MAC (5 mA (A01))	T23	V1P1_DUAL_MACPLL	
MCP_MII_COMP_VDD	C27	MII_COMP_VDD	
MCP_MII_COMP_GND	B27	MII_COMP_GND	
	E28	MII_VREF	MCP_MII_VREF
	B24	MII_TXD0	ENET_TXD<0>
	C24	MII_TXD1	ENET_TXD<1>
	C25	MII_TXD2	ENET_TXD<2>
	D25	MII_TXD3	ENET_TXD<3>
	D24	MII_TXCLK	ENET_CLK125M_TXCLK
	C26	MII_TXEN	ENET_TX_CTRL
	D21	MII_MDC	ENET_MDC
	C21	MII_MDIO	ENET_MDIO
	G23	MII_PWRDWN/GPIO_37	TP_ENET_PWRDWN_L
	E23	BUF_25MHZ	MCP_CLK25M_BUF0_R
	J23	MII_RESET*	ENET_RESET_L

=PP3V3_ENET_MCP_RMGT → R1810 49.9 1% 1/16W MF-LF 402 → MII_COMP_VDD

MII_COMP_GND → R1811 49.9 1% 1/16W MF-LF 402 → GND

=PP3V3_S5_MCP_GPIO → R1820 47K 5% 1/16W MF-LF 402 → BI

=PP3V3_S0_MCP_GPIO → R1860 100K 5% 1/16W MF-LF 402 → R1861 100K 5% 1/16W MF-LF 402 → GND

DACS

V3P3_DUAL_RMGT0	J24	=PP3V3_ENET_MCP_RMGT	83 mA (A01)
V3P3_DUAL_RMGT1	K24		
V1P0_DUAL_RMGT_0	U23	=PP1V05_ENET_MCP_RMGT	131 mA (A01)
V1P0_DUAL_RMGT_1	V23		
V3P3_RGBDAC_VDD	J32	PP3V3_S0_MCP_DAC	103 mA / 206 mA (A01)
V3P3_TVDAC_VDD	K32		103 mA
TP_MCP_RGB_DAC_RSET	C39	RGB_DAC_RSET	
TP_MCP_RGB_DAC_VREF	B38	RGB_DAC_VREF	
MCP_TV_DAC_RSET	E36	TV_DAC_RSET	
MCP_TV_DAC_VREF	A35	TV_DAC_VREF	
MCP_CLK27M_XTALIN	C38	XTALIN_TV	
MCP_CLK27M_XTALOUT	D38	XTALOUT_TV	
LPCPLUS_GPIO	E16	GPIO_6/FERR*/IGPU_GPIO6	
DP_IG_CA_DET	B15	GPIO_7/NFERR*/IGPU_GPIO7	
	B39	RGB_DAC_RED	TP_MCP_RGB_RED
	A39	RGB_DAC_GREEN	TP_MCP_RGB_GREEN
	B40	RGB_DAC_BLUE	TP_MCP_RGB_BLUE
	A40	RGB_DAC_HSYNC	TP_MCP_RGB_HSYNC
	A41	RGB_DAC_VSYNC	TP_MCP_RGB_VSYNC
	A36	TV_DAC_RED	CRT_IG_R_C_PR
	B36	TV_DAC_GREEN	CRT_IG_G_Y_Y
	C36	TV_DAC_BLUE	CRT_IG_B_COMP_PB
	D36	TV_DAC_HSYNC/GPIO_44	CRT_IG_HSYNC
	C37	TV_DAC_VSYNC/GPIO_45	CRT_IG_VSYNC

RGB ONLY

TV / Component
C / Pr
Y / Y
Comp / Pb

DDC_CLK0 B31 — MCP_DDC_CLK0
DDC_DATA0 A31 — MCP_DDC_DATA0

FLAT PANEL

LVDS_IG_BKL_PWM	G39	LCD_BKL_CTL/GPIO_57	
LVDS_IG_BKL_ON	E37	LCD_BKL_ON/GPIO_59	
LVDS_IG_PANEL_PWR	F40	LCD_PANEL_PWR/GPIO_58	
=MCP_HDMI_TXC_P	D35	HDMI_TXC_P/ML0_LANE3_P	
=MCP_HDMI_TXC_N	E35	HDMI_TXC_N/ML0_LANE3_N	
=MCP_HDMI_TXD_P<0>	G35	HDMI_TXD0_P/ML0_LANE2_P	
=MCP_HDMI_TXD_N<0>	F35	HDMI_TXD0_N/ML0_LANE2_N	
=MCP_HDMI_TXD_P<1>	F33	HDMI_TXD1_P/ML0_LANE1_P	
=MCP_HDMI_TXD_N<1>	G33	HDMI_TXD1_N/ML0_LANE1_N	
=MCP_HDMI_TXD_P<2>	J33	HDMI_TXD2_P/ML0_LANE0_P	
=MCP_HDMI_TXD_N<2>	H33	HDMI_TXD2_N/ML0_LANE0_N	
DP_IG_AUX_CH_P	D43	DP_AUX_CH0_P	
DP_IG_AUX_CH_N	C43	DP_AUX_CH0_N	
=DVI_HPD_GMUX_INT (See below)	C31	HPLUG_DET2/GPIO_22	
=MCP_HDMI_HPD	E31	HPLUG_DET3	
=PP3V3R1V8_S0_MCP_IFP_VDD (190 mA (A01, 1.8V))	M27	V1P8_IFPA_VDD	
	M26	V1P8_IFPB_VDD	
PP3V3_S0_MCP_VPLL (16 mA (A01))	M28	V3P3_PLL_IFPAB (8 mA)	
	M29	V3P3_PLL_HDMI (8 mA)	
=PP1V05_S0_MCP_HDMI_VDD (95 mA (A01))	T25	V1P1_HDMI_VDD	
MCP_HDMI_RSET	J31	HDMI_RSET	
MCP_HDMI_VPROBE	J30	HDMI_VPROBE	
	C30	DDC_CLK2/GPIO_23	LVDS_IG_DDC_CLK
	B30	DDC_DATA2/GPIO_24	LVDS_IG_DDC_DATA
	D31	DDC_CLK3	=MCP_HDMI_DDC_CLK
	E31	DDC_DATA3	=MCP_HDMI_DDC_DATA
	E32	IFPAB_RSET	MCP_IFPAB_RSET
	G31	IFPAB_VPROBE	MCP_IFPAB_VPROBE
	B35	IFPA_TXC_P	LVDS_IG_A_CLK_P
	C35	IFPA_TXC_N	LVDS_IG_A_CLK_N
	B32	IFPA_TXD0_P	LVDS_IG_A_DATA_P<0>
	A32	IFPA_TXD0_N	LVDS_IG_A_DATA_N<0>
	D32	IFPA_TXD1_P	LVDS_IG_A_DATA_P<1>
	C32	IFPA_TXD1_N	LVDS_IG_A_DATA_N<1>
	D33	IFPA_TXD2_P	LVDS_IG_A_DATA_P<2>
	C33	IFPA_TXD2_N	LVDS_IG_A_DATA_N<2>
	B34	IFPA_TXD3_P	LVDS_IG_A_DATA_P<3>
	C34	IFPA_TXD3_N	LVDS_IG_A_DATA_N<3>
	L31	IFPB_TXC_P	LVDS_IG_B_CLK_P
	K31	IFPB_TXC_N	LVDS_IG_B_CLK_N
	J29	IFPB_TXD4_P	LVDS_IG_B_DATA_P<0>
	H29	IFPB_TXD4_N	LVDS_IG_B_DATA_N<0>
	L29	IFPB_TXD5_P	LVDS_IG_B_DATA_P<1>
	K29	IFPB_TXD5_N	LVDS_IG_B_DATA_N<1>
	L30	IFPB_TXD6_P	LVDS_IG_B_DATA_P<2>
	K30	IFPB_TXD6_N	LVDS_IG_B_DATA_N<2>
	N30	IFPB_TXD7_P	LVDS_IG_B_DATA_P<3>
	M30	IFPB_TXD7_N	LVDS_IG_B_DATA_N<3>

R1850 10K 5% 1/16W MF-LF 402 → GND

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Signal	Interface Mode: TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

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PAGE TITLE
MCP Ethernet & Graphics

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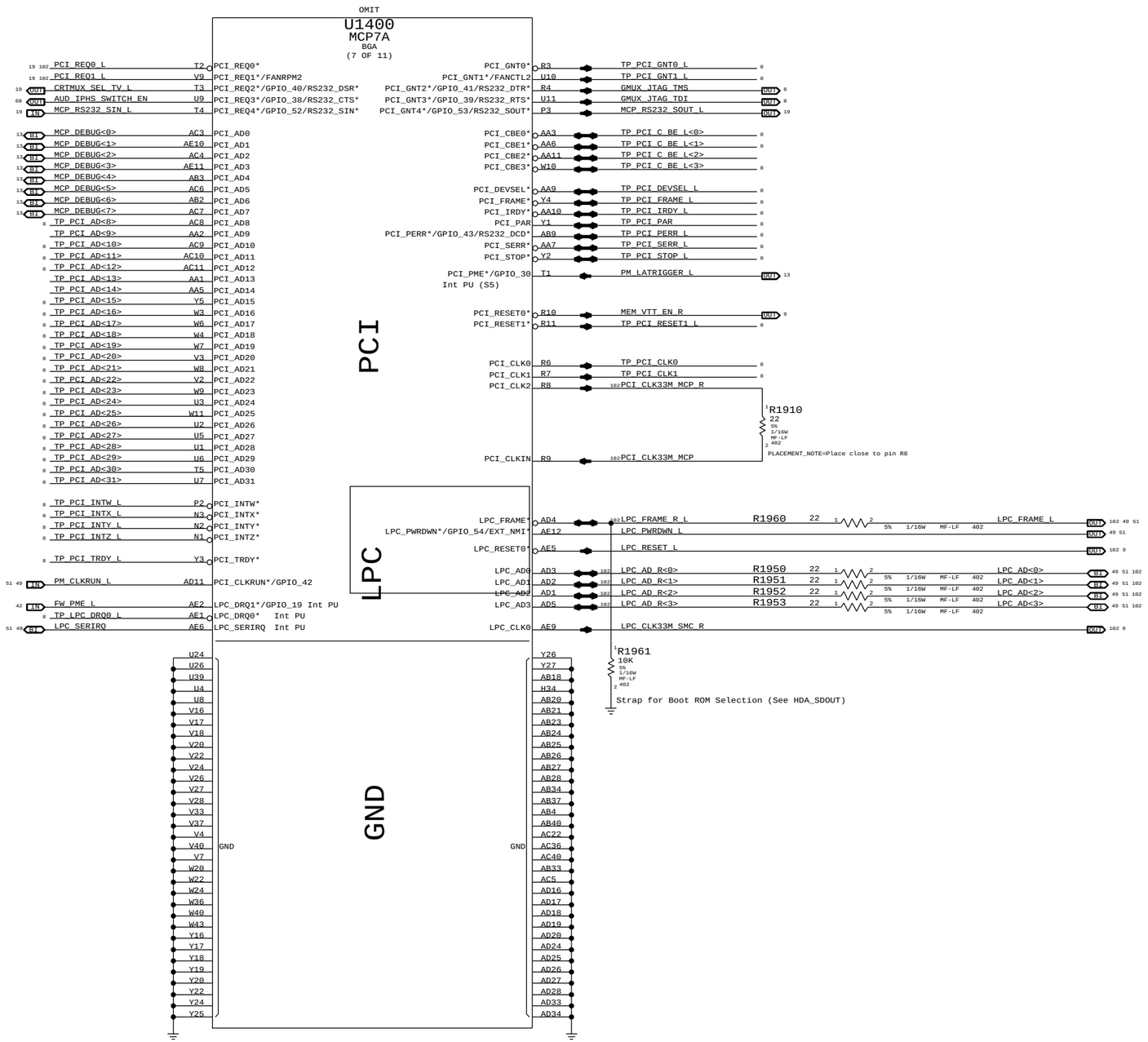
DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 18 OF 110
SHEET



PAGE TITLE	MCP PCI & LPC
	Apple Inc.
DRAWING NUMBER	
SIZE	D
REVISION	16.0.0
BRANCH	
PAGE	19 OF 110
SHEET	

OMIT

U1400
MCP7A
BGA
(8 OF 11)

SATA

45 101 OUT	SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P
45 101 OUT	SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N
101 45 IN	SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N
101 45 IN	SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P
45 101 OUT	SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P
45 101 OUT	SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N
101 45 IN	SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N
101 45 IN	SATA_ODD_D2R_P	AK9	SATA_A1_RX_P
	TP_SATA_C_R2D_CP	AK2	SATA_B0_TX_P
	TP_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N
	TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N
	TP_SATA_C_D2RP	AJ1	SATA_B0_RX_P
	TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P
	TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N
	TP_SATA_D_D2RN	AL4	SATA_B1_RX_N
	TP_SATA_D_D2RP	AK3	SATA_B1_RX_P
	TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P
	TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N
	TP_SATA_E_D2RN	AM2	SATA_C0_RX_N
	TP_SATA_E_D2RP	AM3	SATA_C0_RX_P
	TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P
	TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N
	TP_SATA_F_D2RN	AN3	SATA_C1_RX_N
	TP_SATA_F_D2RP	AN2	SATA_C1_RX_P
45	TP_MCP_SATALED_L	E12	SATA_LED*

25	PP1V05_S0_MCP_PLL_SATA	AE16	V1P1_PLL_SATA
	84 mA (A01)		
28 6	=PP1V05_S0_MCP_SATA_DVDD0	AF19	V1P1_SATA_DVDD0
	43 mA (A01, DVDD0 & 1)	AG16	
	Minimum 1.025V for Gen2 support	AG17	
		AG19	
28	=PP1V05_S0_MCP_SATA_DVDD1	AH17	V1P1_SATA_DVDD1
		AH19	
28	=PP1V05_S0_MCP_SATA_AVDD0	AJ12	V1P1_SATA_AVDD0
	127 mA (A01, AVDD0 & 1)	AN11	
	Minimum 1.025V for Gen2 support	AK12	
		AK13	
		AL12	
		AM11	
		AM12	
		AN12	
		AL13	
28	=PP1V05_S0_MCP_SATA_AVDD1	AN14	V1P1_SATA_AVDD1
		AL14	
		AM13	
		AM14	
101	MCP_SATA_TERMP	AE3	SATA_TERMP

R2010
2.49K
1% 1/16W MF-LF 402

USB

	External A		
USB0_P	C29	USB_EXTA_P	46 102
USB0_N	D29	USB_EXTA_N	46 102
	AirPort (PCIe Mini-Card)		
USB1_P	C28	USB_MINI_P	8
USB1_N	D28	USB_MINI_N	8
	External D		
USB2_P	A28	USB_EXTD_P	46 102
USB2_N	B28	USB_EXTD_N	46 102
	Camera		
USB3_P	F29	USB_CAMERA_P	47 102
USB3_N	G29	USB_CAMERA_N	47 102
	IR		
USB4_P	K27	USB_IR_P	47 102
USB4_N	L27	USB_IR_N	47 102
	Geyser Trackpad/Keyboard		
USB5_P	J26	USB_TPAD_P	8
USB5_N	J27	USB_TPAD_N	8
	Bluetooth		
USB6_P	F27	USB_BT_P	47 102
USB6_N	G27	USB_BT_N	47 102
	External B		
USB7_P	D27	USB_EXTB_P	46 102
USB7_N	E27	USB_EXTB_N	46 102
	ExpressCard		
USB8_P	K25	USB_EXCARD_P	8
USB8_N	L25	USB_EXCARD_N	8
	External C		
USB9_P	H25	USB_EXTC_P	46 102
USB9_N	J25	USB_EXTC_N	46 102
USB10_P	F25	TP_USB_10P	8
USB10_N	G25	TP_USB_10N	8
USB11_P	K23	USB_SDCARD_P	47 102
USB11_N	L23	USB_SDCARD_N	47 102

USB_OC0*/GPIO_25	L21	USB_EXTA_OC_L	46
USB_OC1*/GPIO_26	K21	USB_EXTB_OC_L	46
USB_OC2*/GPIO_27/MGPIO	J21	USB_EXTC_OC_L	46 9
USB_OC3*/GPIO_28/MGPIO	H21	EXCARD_OC_L	

=PP3V3_S5_MCP_GPIO 6 18

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

V3P3_PLL_USB	L28	PP3V3_S0_MCP_PLL_USB	25
		19 mA (A01)	
USB_RBIAS_GND	A27	102 MCP_USB_RBIAS_GND	

R2060 806 1% 1/16W MF-LF 402

	AD35		
	AD37		
	AD38		
	AE22		
	AE24		
	AE39		
	AE4		
	AD6		
	AF16		
	AF17		
	AF18		
	AF20		
	AF22		
	AF26		
GND	AF27		
	AF28		
	AF33		
	AF34		
	AF37		
	AF40		
	AG18		
	AG20		
	AG22		
	AG26		
	AG36		
	AG40		
	AH18		
	AH20		
	AH22		
	AH24		

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

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PAGE: 20 OF 110

SHEET

OMIT

U1400
MCP7A
BGA
(9 OF 11)

HDA

MISC

HDA_SDIN0	G15	HDA_SDATA_IN0	Int PD
TP_MLB_RAM_SIZE	J14	GPIO_2/HDA_SDATA_IN1/PS2_KB_CLK	Int PD
TP_MLB_RAM_VENDOR (MXM_OK for MXM systems)	J15	GPIO_3/HDA_SDATA_IN2/PS2_KB_DATA	Int PD
MCP_HDA_PULLDN_COMP	A15	HDA_PULLDN_COMP	
PP1V05_S0_MCP_PLL_NV 37 mA (A01)	AE18	V1P1_PLL_NV_H	20 mA
	AE17	V1P1_PLL_SP_SPREF	17 mA
=SPI_CS1_R_L_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1	
SMC_ADAPTER_EN	L26	GPIO_12/SUS_STAT*/ACCLMTR_EXT_TRIG	
TP_SB_A20GATE	K13	A20GATE Int PU	
TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN* Int PU	
SMC_WAKE_SCI_L	C19	SIO_PME* Int PU (S5)	
SMC_RUNTIME_SCI_L	C18	EXT_SMI*/GPIO_32 Int PU (S5)	
SM_INTRUDER_L	B20	INTRUDER*	
TP_MCP_LID_L	M25	LID* Int PU (S5)	
PM_BATLOW_L	M24	LLB* Int PU (S5)	
	NC M22	CPU_DPRSLPVR	
PM_PWRBTN_L	C16	PWRBTN* Int PU (S5)	
PM_SYSRST_DEBOUNCE_L	D16	RSTBTN* Int PU	
RTC_RST_L	C20	RTC_RST*	
PM_RSMRST_L	D20	PWRGD_SB	
MCP_PS_PWRGD	E20	PS_PWRGD	
MCP_CPU_VLD	C17	CPU_VLD	
JTAG_MCP_TDI	E19	JTAG_TDI Int PU	
JTAG_MCP_TDO	F19	JTAG_TDO	
JTAG_MCP_TMS	J19	JTAG_TMS Int PU	
JTAG_MCP_TRST_L	J18	JTAG_TRST*	
JTAG_MCP_TCK	G19	JTAG_TCK	
MCP_CLK25M_XTALIN	A16	XTALIN	
MCP_CLK25M_XTALOUT	B16	XTALOUT	
RTC_CLK32K_XTALIN	A19	XTALIN_RTC	
RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC	

=PP3V3R1V5_S0_MCP_HDA	J16	V3P3_DUAL_HDA_0	R2160 8.2K
	K16	V3P3_DUAL_HDA_1	
HDA_SDOUT_R	F15	HDA_SDATA_OUT	R2170 22
HDA_BIT_CLK_R	E15	HDA_BITCLK	R2171 22
HDA_RST_R_L	K15	HDA_RESET*	R2172 22
HDA_SYNC_R	L15	HDA_SYNC	R2173 22
MCP_GPIO_4	K17	GPIO_4/HDA_DOCK_EN*/PS2_MS_CLK	
AUD_I2C_INT_L	L17	GPIO_5/HDA_DOCK_RST*/PS2_MS_DATA	
PM_SLP_S3_L	G17	SLP_S3*	
PM_SLP_RMGT_L	J17	SLP_RMGT*	
PM_SLP_S4_L	H17	SLP_S5*	
MCP_THMDIODE_P	B11	THERM_DIODE_P	
MCP_THMDIODE_N	C11	THERM_DIODE_N	
MCP_VID<0>	L20	GPIO_13/MCP_VID0	
MCP_VID<1>	M20	GPIO_14/MCP_VID1	
MCP_VID<2>	M21	GPIO_15/MCP_VID2	
MCP_SPKR	C13	SPKR	
SMBUS_MCP_0_CLK	L19	SMB_CLK0	
SMBUS_MCP_0_DATA	K19	SMB_DATA0	
SMBUS_MCP_1_CLK	G21	SMB_CLK1/MSMB_CLK	
SMBUS_MCP_1_DATA	F21	SMB_DATA1/MSMB_DATA	
AP_PWR_EN	M23	SMB_ALERT*/GPIO_64	
MEM_EVENT_L	B12	(MGPIO2) FANRPM0/GPIO_60	
ODD_PWR_EN_L	A12	FANCTL0/GPIO_61	
SMC_IG_THROTTLE_L	D12	(MGPIO3) FANRPM1/GPIO_63	
ARB_DETECT	C12	FANCTL1/GPIO_62	
MCP_CPUVDD_EN	D17	CPUVDD_EN	
SPI_CS0_R_L	C14	GPIO_10/SPI_CS0	
SPI_CLK_R	D13	GPIO_11/SPI_CLK	
SPI_MISO	C15	GPIO_8/SPI_DI	
SPI_MOSI_R	B14	GPIO_9/SPI_DO	
PM_CLK32K_SUSCLK_R	B18	SUS_CLK/GPIO_34	
TP_MCP_BUF_SIO_CLK	AE7	BUF_SIO_CLK	
MCP_TEST_MODE_EN	K22	TEST_MODE_EN	
	L22	PKG_TEST	

R2110 49.9 1% 1/16W MF-LF 402 — =PP3V3R1V5_S0_MCP_HDA

R2120 49.9K 1% 1/16W MF-LF 402 — PP3V3_G3_RTC

R2121 49.9K 1% 1/16W MF-LF 402

R2150 10K 5% 1/16W MF-LF 402

R2151 100K 5% 1/16W MF-LF 402

R2163 10K 5% 1/16W MF-LF 402

R2190 1K 1% 1/16W MF-LF 402

=PP3V3_S0_MCP
BOOT_MODE_SAFE
R2180 10K 5% 1/16W MF-LF 402
BOOT_MODE_USER
R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_RST_R_L
HDA_SYNC_R

C2170 10PF 5% 50V CERM 402
C2172 10PF 5% 50V CERM 402
C2171 10PF 5% 50V CERM 402
C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO

R2140 10K 5% 1/16W MF-LF 402
R2141 10K 5% 1/16W MF-LF 402
R2142 10K 5% 1/16W MF-LF 402
R2143 10K 5% 1/16W MF-LF 402

MCP_GPIO_4
AUD_I2C_INT_L
MEM_EVENT_L
SMC_IG_THROTTLE_L

ARB_DETECT
R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO

R2154 100K 5% 1/16W MF-LF 402 — AP_PWR_EN

MCP_VID<0>
MCP_VID<1>
MCP_VID<2>

R2155 22K 5% 1/16W MF-LF 402
R2156 22K 5% 1/16W MF-LF 402
R2157 22K 5% 1/16W MF-LF 402

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PAGE TITLE: MCP HDA & MISC

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DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 21 OF 110
SHEET

OMIT

U1400
MCP7A
BGA
(11 OF 11)

GND: AH26, AH33, AH34, AH37, AH38, AJ39, AJ8, AK10, AK33, AK34, AK37, AK4, AK40, AL36, AL40, AL5, AM10, AM16, AM18, AM20, AM22, AM24, AM26, AM30, AM34, AM35, AM37, AM38, AM5, AM6, AM7, AM9, AP26, AN28, AN30, AN39, AN4, Y7, AP10, AU26, AP14, AU14, AP28, AP32, AP34, AP36, AP37, AP4, AP40, AP7, AW23, AR28, AR32, AR40, AT10, AR12, AT13, AT29, AT33, AT6, AT7, AT9, AY21, AY22, L12, AU12, AU28, AP33, AU32, AR30, AU36, AU38, AU4, G28, F20, AV28, AV32, AV36, AV4, AV7, AW11, G20, AR43, AW43, AY10, AV12, AY30, AY33, AY34, AY37, AY38, AY41

GND: AV40, BA1, BA4, AW31, AY6, L35, BC33, BC37, BC41, AY14, BC5, C2, D10, D14, D15, D18, D19, D22, D23, D26, D30, D37, D6, E13, E17, E21, E25, E29, E33, F12, F16, F32, F8, G10, G12, G14, G16, BC12, G22, G24, AW20, G34, G4, G43, G6, G8, H11, H15, AW35, H23, AN8, G40, J12, J8, K10, K12, K18, K26, K37, K4, K40, K8, AU1, L40, L43, L5, M10, M34, M35, M37, Y28, Y33, Y34, Y35, Y37, Y38, AB17, AB16, AN26, AD7, M11, AA4, AB19, AY13, P11, Y6, T11, V11, Y11, AH16, T22

OMIT

U1400
MCP7A
BGA
(10 OF 11)

=PPVCORE_S0_MCP (25 6)
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

V1P0_CORE_VDD: AA25, AA26, AA27, AA28, AC16, AC17, AC18, AC19, AC20, AC21, AA17, AC23, AC24, AC25, AC26, AC27, AC28, AD21, AD23, W27, V25, AA18, U25, AE19, AE21, AE23, AE25, AE26, AE27, AE28, AE10, AE11, AA19, AH12, AF2, AE21, AF23, AE25, AF3, AF4, AF7, AH23, AF9, AA20, AG10, AG11, AG12, AG21, AG23, AG25, AG3, AG4, AA21, AG6, AG7, AG5, AG8, AG9, AH1, AH10, AH11, W26, AH2, AA23, W28, AH25, Y21, AH21, AH3, AH4, AH5, AH6, AH7, AH9, AA24, W21, W23, Y23, W25, AF12, AA16

=PP1V05_S0_MCP_FSB (6 14 25)
1139 mA
1182 mA (A01)

V1P2_CPU_VTT: R32, P31, AF32, AE32, AH32, AJ32, AK31, AK32, AD32, AL31, AB32, AC32, B41, B42, C40, C41, C42, D39, D40, D41, E38, E39, E40, F37, F38, F39, G36, G37, G38, H35, H37, J34, J35, J36, K33, K34, K35, L32, L33, L34, M31, M32, M33, N31, N32, P32, Y32, AA32, T32, U32, V32, W32

V1P2_CPUCLK_VTT: AG32 — 43 mA

=PP3V3_S0_MCP (6 21 25)
450 mA (A01)

V3P3: AD10, AE8, AB10, AD9, Y10, AB11, AA8, Y9

=PP3V3_S5_MCP (6 25)
16 mA
266 mA (A01)

V3P3_DUAL: G18, H19, J20, K20

V3P3_DUAL_USB: G26, H27, J28, K28 — 250 mA

=PP1V05_S5_MCP_VDD_AUXC (6 25)
105 mA (A01)

V1P0_VDD_AUXC: T21, U21, V21

=PP3V3_G3_RTC (28 21)
10 uA (G3)
80 uA (S0)

V3P3_VBAT: A20

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PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER:
SIZE: D
REVISION: 16.0.0
BRANCH:
PAGE: 22 OF 110
SHEET:

8 7 6 5 4 3 2 1

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PAGE TITLE
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DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
23 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
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DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
24 OF 110

SHEET

MCP Core Power

=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
APPLE: 4X 4.7UF 0402, 4X 1UF 0402, 6X 0.1UF 0402 (23.4 uF)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 1UF 10% 10V X5R 402-1
C2509 1UF 10% 10V X5R 402-1
C2510 1UF 10% 10V X5R 402-1
C2511 1UF 10% 10V X5R 402-1
C2512 1UF 10% 10V X5R 402-1
C2513 1UF 10% 10V X5R 402-1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0,5%,0402	C2574,C2518	IG

MCP PCIE (DVDD) Power

DIFFERENT THAN ON T18
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

PEX_DVDD RAIL SPLIT BASED ON T8 VS. E6. 8 OUT OF 18 BALLS FOR DVDD0 SO 80% OF CAPACITANCE ON DVDD0

NV: 1X 4.7UF 0402, 2X 1UF 0402, 2X 0.1UF 0402 (6.9UF)
K50: 2X 2.2UF 0402, 2X 1UF 0402, (6.4 UF)

=PP1V05_S0_MCP_PEX_DVDD0
C2516 1UF 10% 10V X5R 402-1
C2515 2.2UF 20% 6.3V CERM 402-LF (MXM)
C2517 1UF 10% 10V X5R 402-1 (MXM)
C2518 2.2UF 20% 6.3V CERM 402-LF (MXM)

MCP SATA (DVDD) Power

=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

=PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

=PP1V05_S0_MCP_FSB
1182 mA (A01)

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

=PP3V3_S0_MCP
450 mA (A01)

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF
19 mA (A01)
L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V) 19 mA (A01)
C2555 2.2UF 20% 6.3V CERM 402-LF

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 2x 2.2uF 0402 (2.2 uF)

MCP 3.3V AUX/USB Power

=PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

=PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

MCP 3.3V/1.5V HDA Power

=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

MCP79 Ethernet VRef

=PP3V3_ENET_MCP_RMGT
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF (OUT)
C2591 0.1UF 20% 10V CERM 402

MCP PLL (MAC)

=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 5 mA (A01)
C2595 4.7UF 20% 4V X5R 402
C2596 4.7UF 20% 4V X5R 402

MCP PLL (AVDD_UF)

=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)
L2570 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF (MXM)
C2572 2.2UF 20% 6.3V CERM 402-LF (MXM)
C2573 2.2UF 20% 6.3V CERM 402-LF (MXM)
C2574 2.2UF 20% 6.3V CERM 402-LF (MXM)

PP1V05_S0_MCP_PEX_AVDD (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0
PEX_AVDD RAIL SPLIT BASED ON IG VS. E6. 12 OUT OF 15 BALLS FOR AVDD0 SO 80% OF CAPACITANCE ON AVDD0

L2575 30-OHM-5A 0603

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP1V05_S0_MCP_SATA_AVDD (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 127 mA (A01)
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

MCP PLL (PLL_UF)

=PP1V05_S0_MCP_PLL_UF
562 mA (A01)
L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 270 mA (A01)
C2580 4.7UF 20% 4V X5R 402
C2581 4.7UF 20% 4V X5R 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 84 mA (A01)
C2582 4.7UF 20% 4V X5R 402
C2583 4.7UF 20% 4V X5R 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 84 mA (A01)
C2584 4.7UF 20% 4V X5R 402
C2585 4.7UF 20% 4V X5R 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 87 mA (A01)
C2586 4.7UF 20% 4V X5R 402
C2597 4.7UF 20% 4V X5R 402
C2587 4.7UF 20% 4V X5R 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V) 37 mA (A01)
C2588 4.7UF 20% 4V X5R 402
C2589 4.7UF 20% 4V X5R 402
C2590 2.2UF 20% 6.3V X5R 402

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PAGE TITLE: MCP Standard Decoupling

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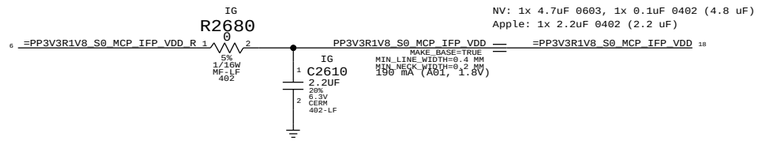
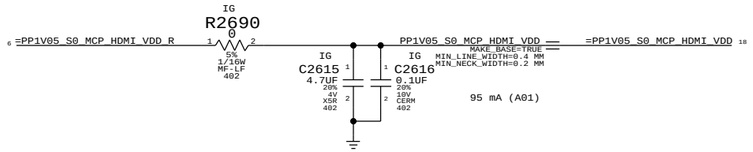
DRAWING NUMBER
SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 25 OF 110
SHEET

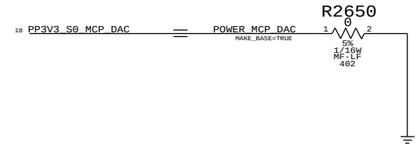
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

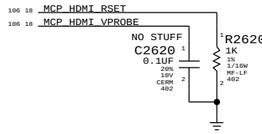


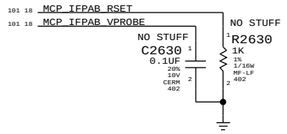
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2610		MXM



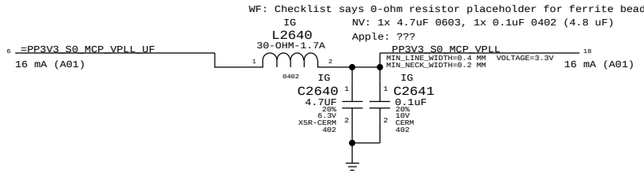
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2616		MXM







WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0,5%,402	C2641		MXM

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PAGE TITLE: MCP Graphics Support

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 26 OF 110

SHEET

8 7 6 5 4 3 2 1

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PAGE TITLE

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Apple Inc.

DRAWING NUMBER

SIZE D

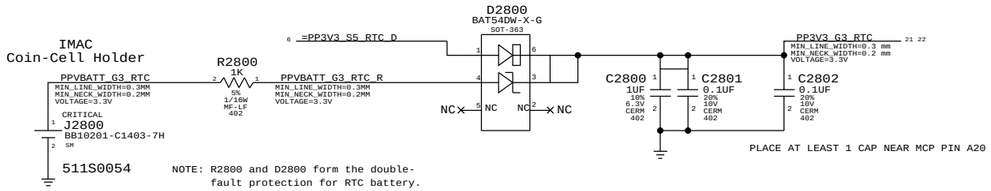
REVISION 16.0.0

BRANCH

PAGE 27 OF 110

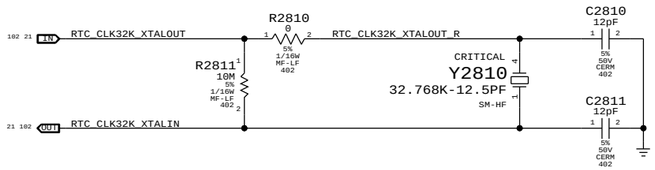
SHEET

RTC Power Sources

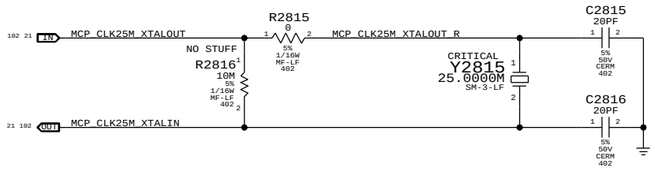


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

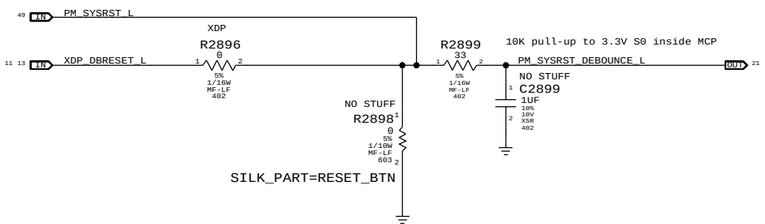
RTC Crystal



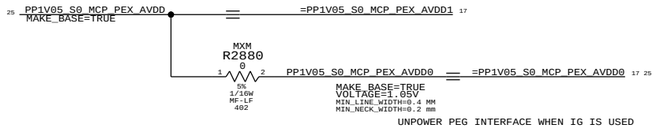
MCP 25MHz Crystal

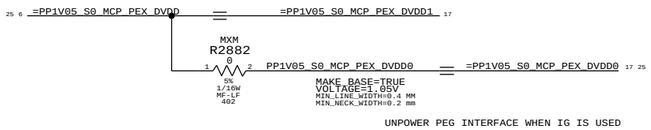


Reset Button

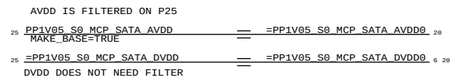


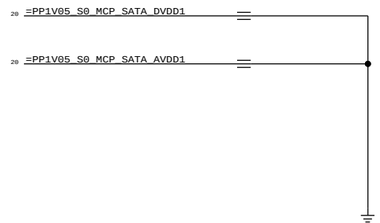
PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN





SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1





PAGE TITLE
SB Misc

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 28 OF 110
SHEET

Page Notes

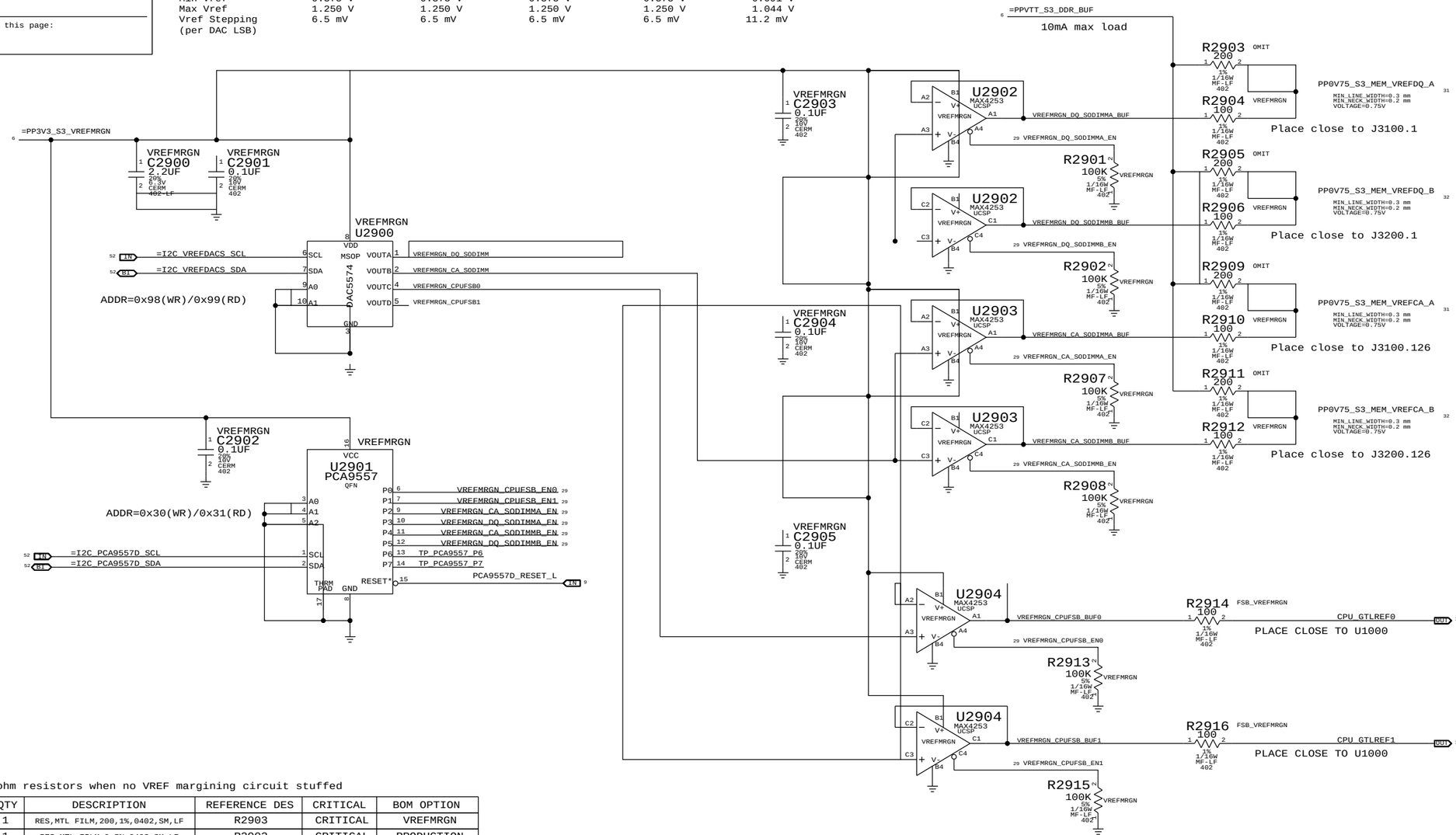
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
PRODUCTION

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2903	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2905	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2909	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	PRODUCTION
114S0149	1	RES,MTL FILM,200,1%,0402,SM,LF	R2911	CRITICAL	VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	PRODUCTION

PAGE TITLE: FSB/DDR3 Vref Margining

Apple Inc.

DRAWING NUMBER — SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 29 OF 110

SHEET

DIMM A (FURTHER FROM MCP)

CAPS TO COUPLE MCP 1V5_S0_MEM

DIMM B (CLOSER TO MCP)

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

C3016 0.1UF 20% 10V CERM 402
C3017 0.1UF 20% 10V CERM 402
C3018 0.1UF 20% 10V CERM 402
C3019 0.1UF 20% 10V CERM 402
C3010 0.1UF 20% 10V CERM 402

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM

C3025 0.1UF 20% 10V CERM 402
C3026 0.1UF 20% 10V CERM 402
C3027 0.1UF 20% 10V CERM 402
C3028 0.1UF 20% 10V CERM 402
C3029 0.1UF 20% 10V CERM 402
C3020 0.1UF 20% 10V CERM 402
C3021 0.1UF 20% 10V CERM 402
C3022 0.1UF 20% 10V CERM 402
C3023 0.1UF 20% 10V CERM 402
C3014 0.1UF 20% 10V CERM 402
C3030 0.1UF 20% 10V CERM 402
C3031 0.1UF 20% 10V CERM 402
C3032 0.1UF 20% 10V CERM 402
C3033 0.1UF 20% 10V CERM 402
C3034 0.1UF 20% 10V CERM 402
C3035 0.1UF 20% 10V CERM 402

EXTRA DECOUPLING CAPS FOR MCP MEM RAIL

30 25 16 6 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C3041 0.1UF 20% 10V CERM 402
C3042 0.1UF 20% 10V CERM 402
C3044 0.1UF 20% 10V CERM 402
C3046 0.1UF 20% 10V CERM 402
C3040 1UF 10% 6.3V CERM 402
C3043 1UF 10% 6.3V CERM 402
C3045 1UF 10% 6.3V CERM 402
C3047 1UF 10% 6.3V CERM 402
C3048 1UF 10% 6.3V CERM 402
C3049 1UF 10% 6.3V CERM 402
C3090 1UF 10% 6.3V CERM 402
C3091 1UF 10% 6.3V CERM 402
C3092 1UF 10% 6.3V CERM 402
C3093 1UF 10% 6.3V CERM 402
C3094 1UF 10% 6.3V CERM 402
C3095 1UF 10% 6.3V CERM 402
C3096 1UF 10% 6.3V CERM 402
C3097 1UF 10% 6.3V CERM 402
C3098 1UF 10% 6.3V CERM 402
C3099 1UF 10% 6.3V CERM 402
C3000 1UF 10% 6.3V CERM 402
C3001 1UF 10% 6.3V CERM 402
C3002 1UF 10% 6.3V CERM 402

16 6 =PP1V8R1V5_S0_MCP_MEM
30 25 4771 mA (A01, DDR3)

C30A0 1UF 10% 6.3V CERM 402
C30A1 1UF 10% 6.3V CERM 402
C30A2 1UF 10% 6.3V CERM 402
C30A3 1UF 10% 6.3V CERM 402
C30A4 1UF 10% 6.3V CERM 402
C30A5 1UF 10% 6.3V CERM 402
C30A6 1UF 10% 6.3V CERM 402
C30A7 1UF 10% 6.3V CERM 402
C30A8 1UF 10% 6.3V CERM 402
C30A9 1UF 10% 6.3V CERM 402
C30AA 1UF 10% 6.3V CERM 402
C30AB 1UF 10% 6.3V CERM 402
C30AC 1UF 10% 6.3V CERM 402
C30AD 1UF 10% 6.3V CERM 402
C30AE 1UF 10% 6.3V CERM 402
C30AF 1UF 10% 6.3V CERM 402
C30B0 1UF 10% 6.3V CERM 402
C30B1 1UF 10% 6.3V CERM 402
C30B2 1UF 10% 6.3V CERM 402
C30B3 1UF 10% 6.3V CERM 402
C30B4 1UF 10% 6.3V CERM 402
C30B5 1UF 10% 6.3V CERM 402
C30B6 1UF 10% 6.3V CERM 402
C30B7 1UF 10% 6.3V CERM 402

25 16 6 =PP1V8R1V5_S0_MCP_MEM
30 4771 mA (A01, DDR3)

C30B8 1UF 10% 6.3V CERM 402
C30B9 1UF 10% 6.3V CERM 402
C30BA 1UF 10% 6.3V CERM 402
C30BB 1UF 10% 6.3V CERM 402
C30BC 1UF 10% 6.3V CERM 402
C30BD 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR

31 107 6 =PP1V5_S3_MEM_A

C3050 10UF 20% 6.3V X5R 603
C3051 10UF 20% 6.3V X5R 603
C3052 1UF 10% 6.3V CERM 402
C3053 1UF 10% 6.3V CERM 402
C3054 1UF 10% 6.3V CERM 402
C3055 1UF 10% 6.3V CERM 402
C3056 1UF 10% 6.3V CERM 402
C3057 1UF 10% 6.3V CERM 402
C3058 1UF 10% 6.3V CERM 402
C3059 1UF 10% 6.3V CERM 402
C3060 1UF 10% 6.3V CERM 402
C3061 1UF 10% 6.3V CERM 402
C3062 1UF 10% 6.3V CERM 402
C3063 1UF 10% 6.3V CERM 402
C3064 1UF 10% 6.3V CERM 402
C3065 1UF 10% 6.3V CERM 402

DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR

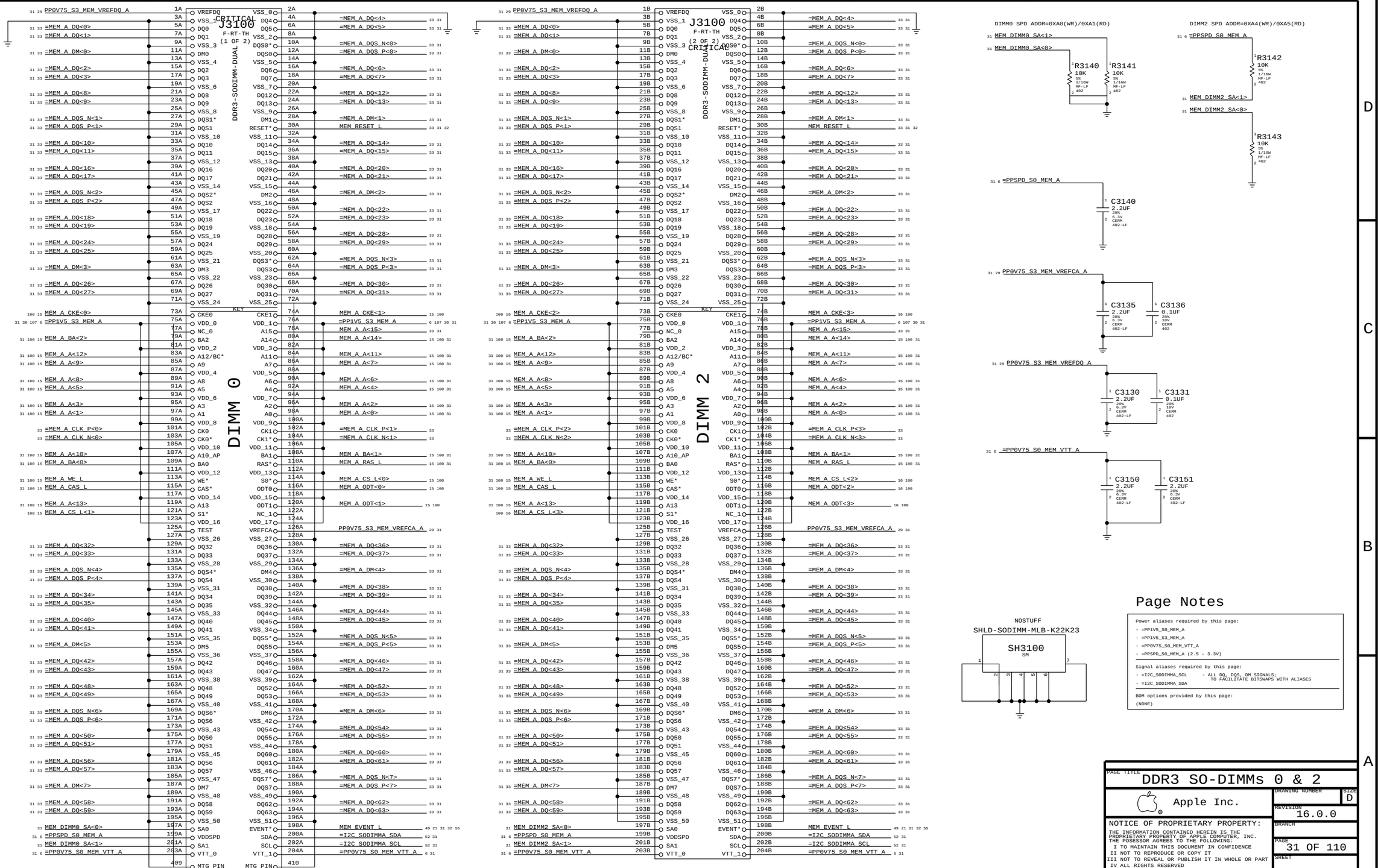
32 107 6 =PP1V5_S3_MEM_B

C3070 10UF 20% 6.3V X5R 603
C3071 10UF 20% 6.3V X5R 603
C3072 1UF 10% 6.3V CERM 402
C3073 1UF 10% 6.3V CERM 402
C3074 1UF 10% 6.3V CERM 402
C3075 1UF 10% 6.3V CERM 402
C3076 1UF 10% 6.3V CERM 402
C3077 1UF 10% 6.3V CERM 402
C3078 1UF 10% 6.3V CERM 402
C3079 1UF 10% 6.3V CERM 402
C3080 1UF 10% 6.3V CERM 402
C3081 1UF 10% 6.3V CERM 402
C3082 1UF 10% 6.3V CERM 402
C3083 1UF 10% 6.3V CERM 402
C3084 1UF 10% 6.3V CERM 402
C3085 1UF 10% 6.3V CERM 402

PAGE TITLE
MEMORY CAPS

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 30 OF 110
SHEET



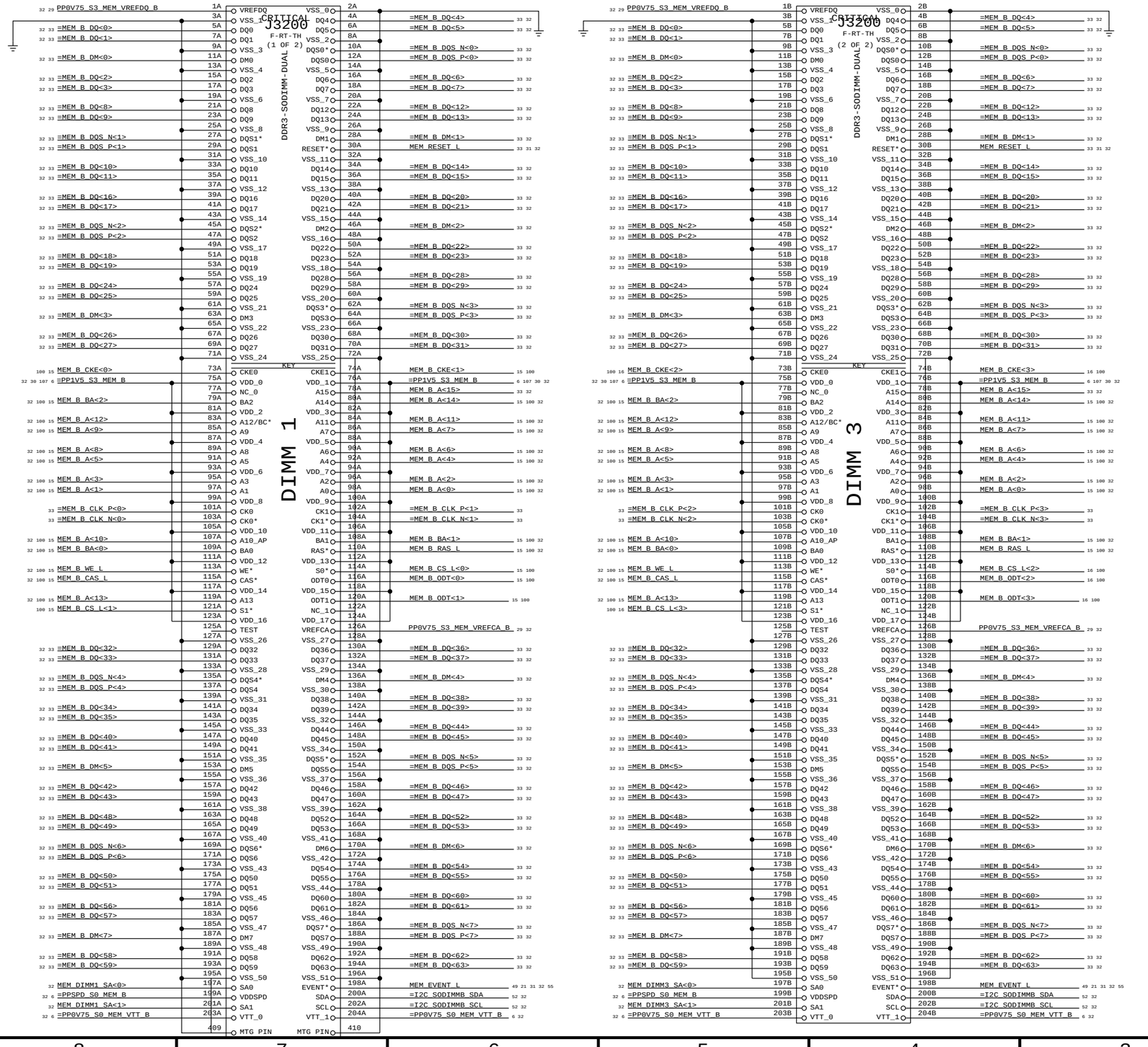
Page Notes

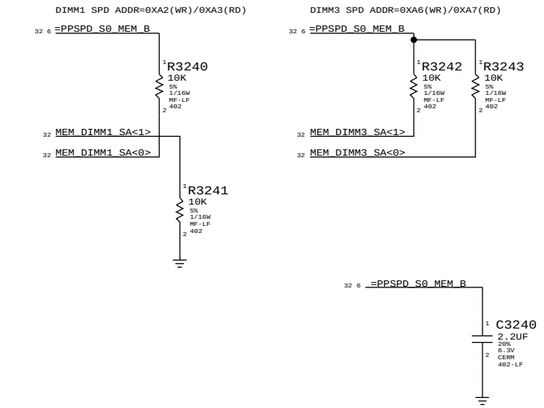
Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

PAGE TITLE	DDR3 SO-DIMMs 0 & 2
	Apple Inc.
DRAWING NUMBER	
SIZE	D
REVISION	16.0.0
BRANCH	
PAGE	31 OF 110
SHEET	





Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:

(NONE)

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

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DRAWING NUMBER

SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 32 OF 110

SHEET

MCP CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	31
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	31
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<0>	31
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	31
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	31
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	31
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	31
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	31
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	31
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	31
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	31

MCP CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	31
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	31
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<1>	31
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	31
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	31
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	31
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	31
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	31
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	31
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	31
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	31

MCP CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	31
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	31
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<2>	31
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	31
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	31
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	31
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	31
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	31
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	31
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	31
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	31

MCP CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	31
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	31
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<3>	31
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	31
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	31
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	31
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	31
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	31
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	31
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	31
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	31

MCP CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	31
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	31
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<4>	31
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	31
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	31
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	31
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	31
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	31
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	31
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	31
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	31

MCP CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	31
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	31
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<5>	31
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	31
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	31
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	31
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	31
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	31
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	31
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	31
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	31

MCP CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	31
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	31
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<6>	31
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	31
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	31
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	31
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	31
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	31
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	31
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	31
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	31

MCP CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	31
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	31
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<7>	31
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	31
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	31
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	31
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	31
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	31
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	31
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	31
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	31

MCP CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	32
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	32
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<0>	32
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	32
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	32
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	32
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	32
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	32
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	32
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	32
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	32

MCP CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	32
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	32
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<1>	32
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	32
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	32
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	32
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	32
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	32
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	32
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	32
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	32

MCP CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	32
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	32
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<2>	32
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	32
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	32
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	32
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	32
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	32
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	32
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	32
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	32

MCP CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	32
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	32
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<3>	32
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	32
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	32
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	32
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	32
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	32
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	32
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	32
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	32

MCP CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	32
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	32
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<4>	32
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	32
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	32
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	32
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	32
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	32
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	32
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	32
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	32

MCP CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	32
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	32
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<5>	32
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	32
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	32
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	32
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	32
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	32
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	32
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	32
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	32

MCP CHANNEL B DQS 6 -> DIMM B DQS 6

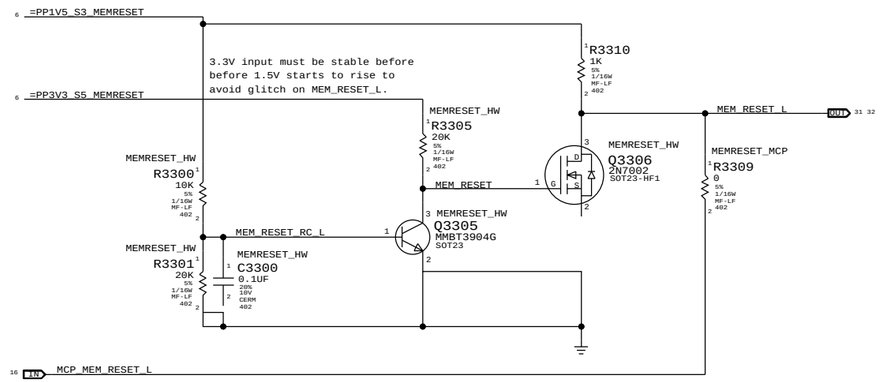
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	32
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	32
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<6>	32
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	32
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	32
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	32
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	32
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	32
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	32
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	32
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	32

MCP CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	32
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	32
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<7>	32
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	32
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	32
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	32
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	32
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	32
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	32
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	32
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	32

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



MCP MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>	31
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>	31
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>	31
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>	31
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>	31
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>	31
MEM_A_CLK_P<4>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>	31
MEM_A_CLK_N<4>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>	31

MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>	32
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>	32
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>	32
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>	32
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>	32
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>	32
MEM_B_CLK_P<4>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>	32
MEM_B_CLK_N<4>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>	32

MCP MEMORY TEST POINT ALIASING

TP_MEM_A_A<15>	MAKE_BASE=TRUE	MEM_A_A<15>	31
TP_MEM_B_A<15>	MAKE_BASE=TRUE	MEM_B_A<15>	32

PAGE TITLE
DDR3 SUPPORT AND BITSWAPS

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SIZE D

REVISION 16.0.0

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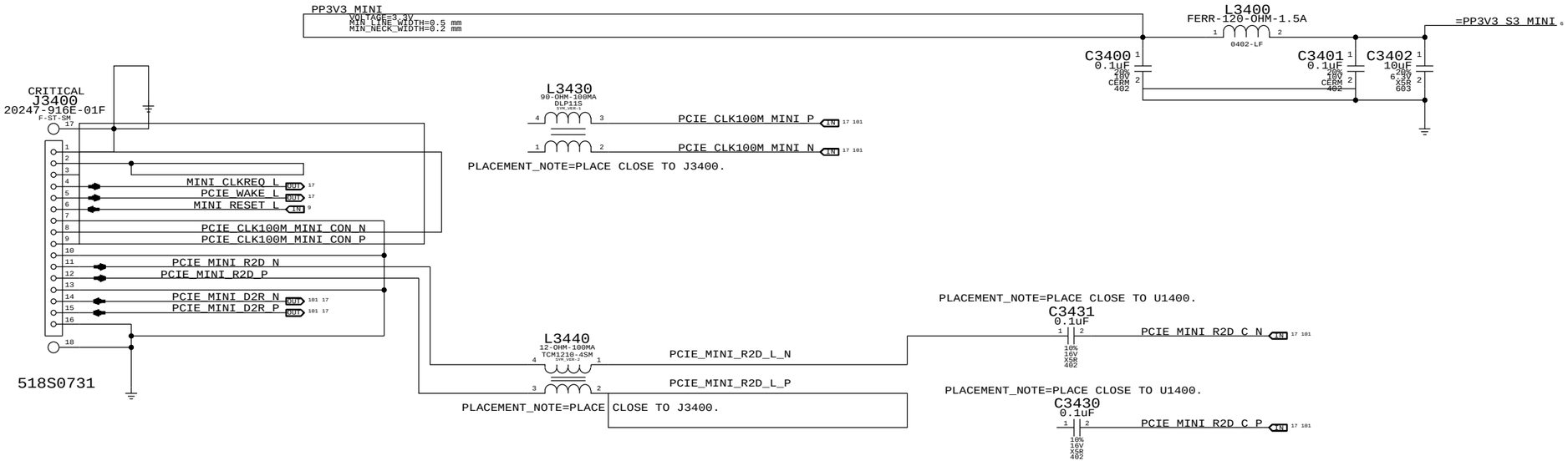
PAGE 33 OF 110

SHEET



PAGE TITLE
PCI-E Wireless Connector

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PAGE 34 OF 110

SHEET

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PAGE TITLE
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SIZE D

REVISION
16.0.0

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PAGE
35 OF 110

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SIZE D

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16.0.0

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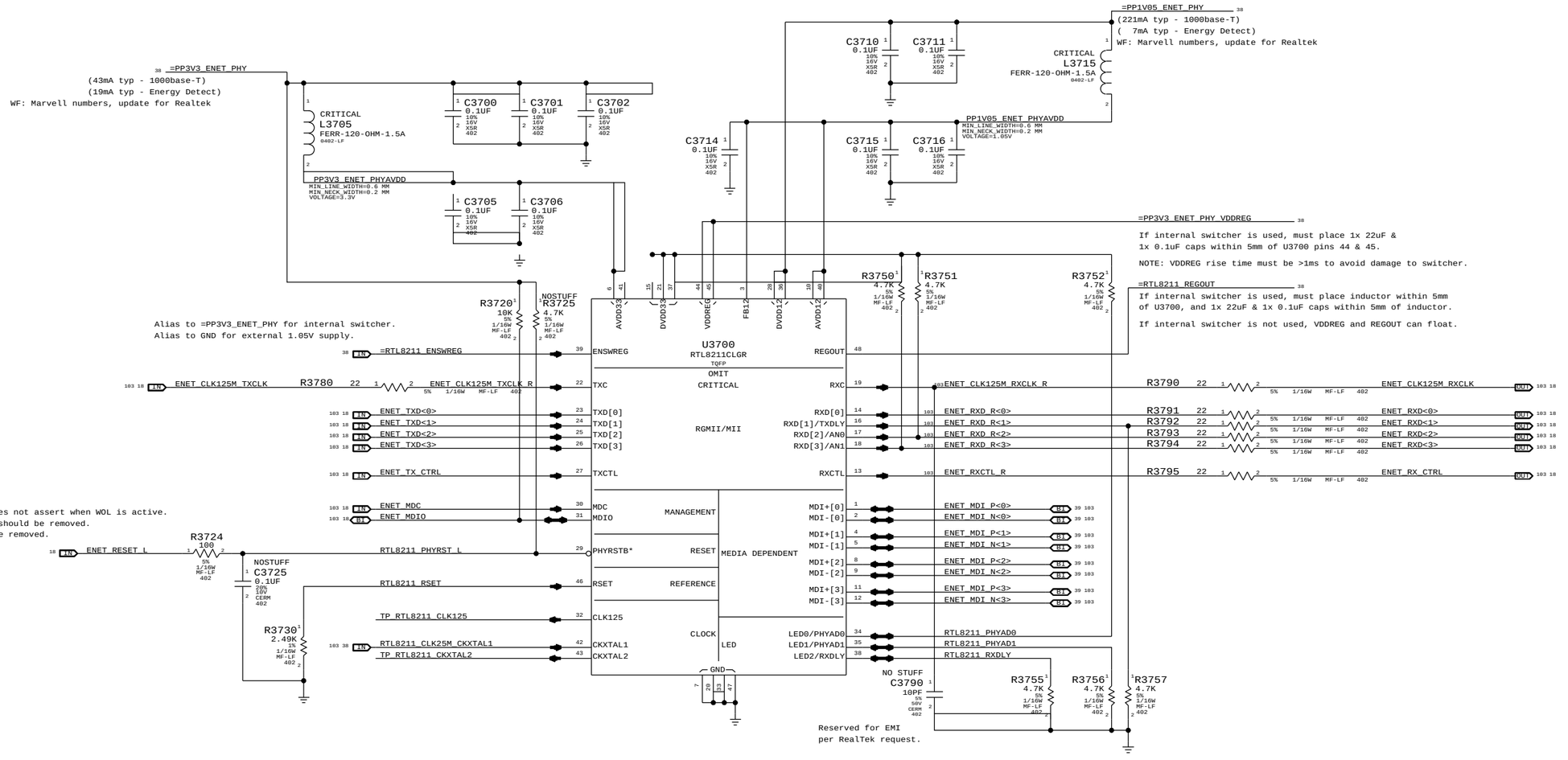
PAGE
36 OF 110

SHEET



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

PAGE TITLE: Ethernet PHY (RTL8211CL)

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DRAWING NUMBER
SIZE D
REVISION 16.0.0
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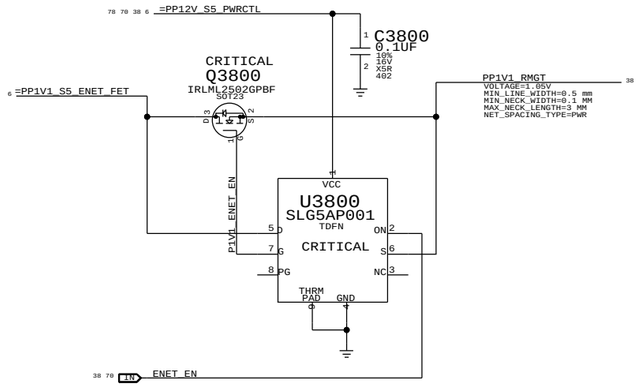
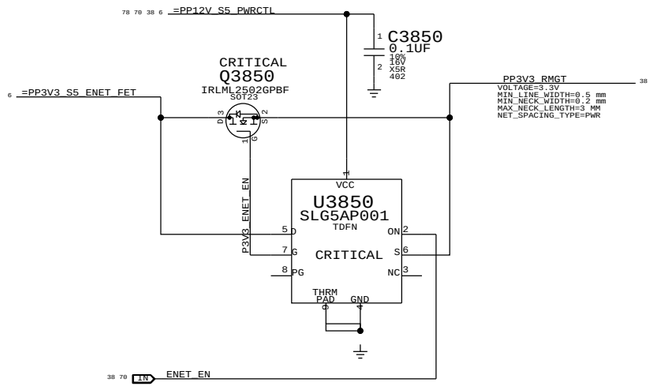
PAGE 37 OF 110
SHEET

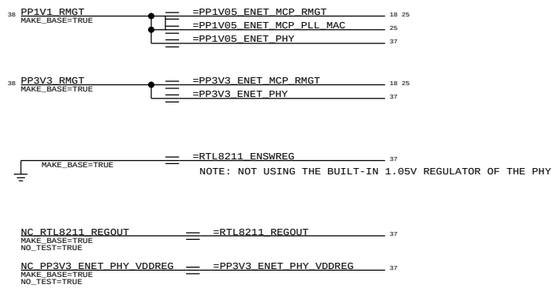
1.1V ENET FET



3.3V ENET FET



ENET ALIASES



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

PAGE TITLE: Ethernet Support

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DRAWING NUMBER

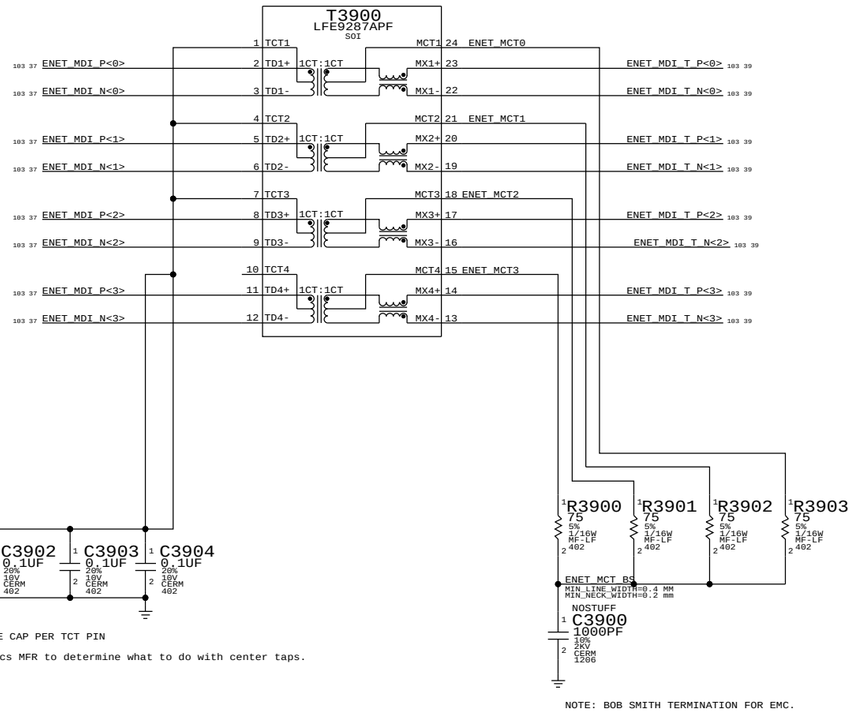
SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 38 OF 110

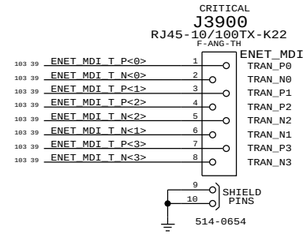
SHEET



PLACE ONE CAP PER TCT PIN

NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.



PAGE TITLE: ETHERNET CONNECTOR

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SIZE: D

REVISION: 16.0.0

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PAGE: 39 OF 110

SHEET

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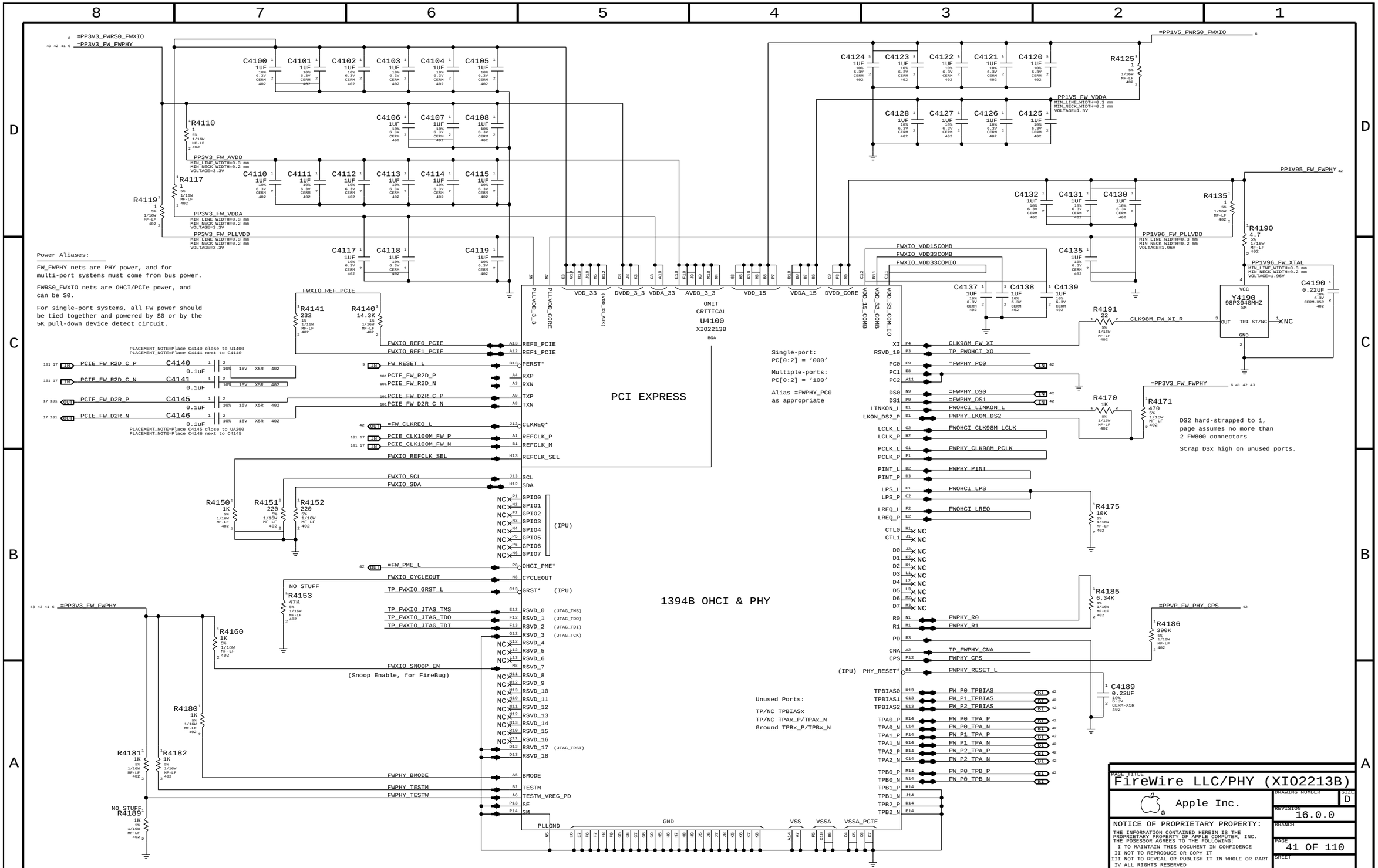
DRAWING NUMBER
SIZE D

REVISION
16.0.0

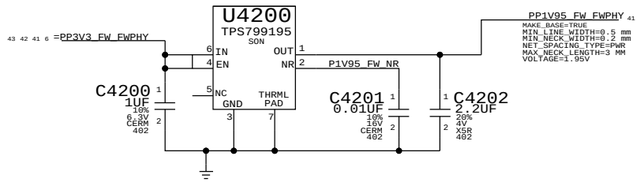
BRANCH

PAGE
40 OF 110

SHEET



1394 PHY 1.95V SUPPLY



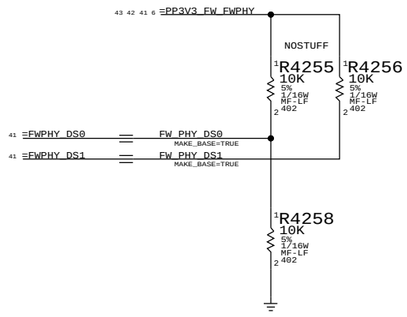
FireWire Aliases For Connectivity

41 =FW_CLKREQ_L = FW_CLKREQ_L 17
MAKE_BASE=TRUE

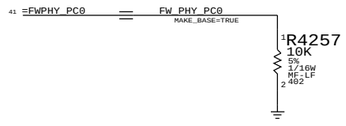
41 =FW_PME_L = FW_PME_L 19
MAKE_BASE=TRUE

41 =PPVP_FW_PHY_CPS = PPVP_FW_PHY_CPS 43
MAKE_BASE=TRUE

1394 PHY STRAPPING OPTIONS



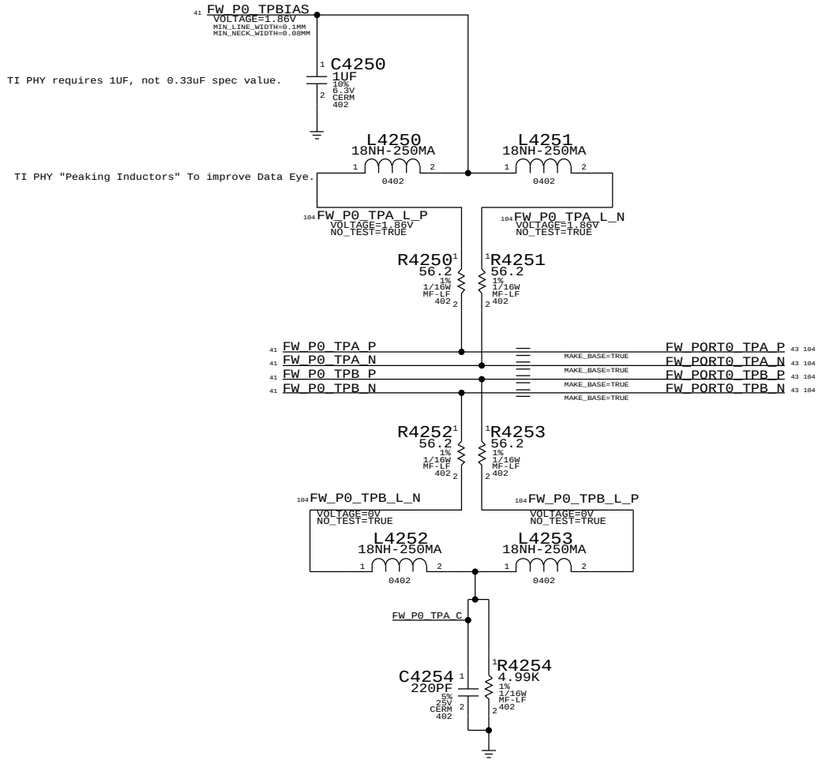
THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.



iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

41 FW_P1_TPBIAS = NC_FW_PORT1_TPBIAS
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P1_TPA_P = NC_FW_PORT1_TPA_P
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P1_TPA_N = NC_FW_PORT1_TPA_N
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P2_TPBIAS = NC_FW_PORT2_TPBIAS
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P2_TPA_P = NC_FW_PORT2_TPA_P
MAKE_BASE=TRUE
NO_TEST=TRUE

41 FW_P2_TPA_N = NC_FW_PORT2_TPA_N
MAKE_BASE=TRUE
NO_TEST=TRUE

PAGE TITLE
FW: 1394B MISC

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SIZE D

REVISION
16.0.0

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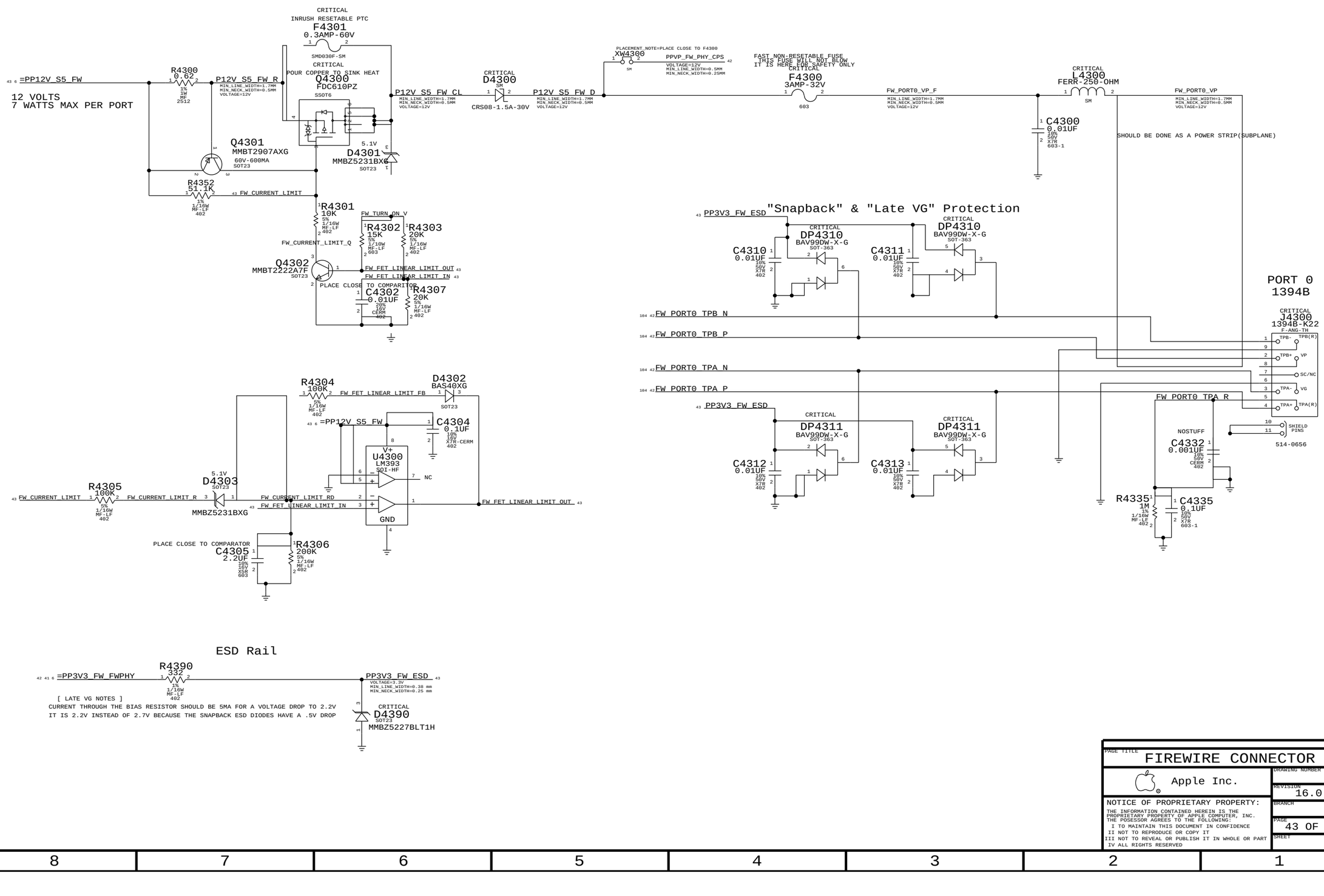
PAGE
42 OF 110

SHEET



PAGE TITLE: FIREWIRE CONNECTOR

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REVISION: 16.0.0

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PAGE: 43 OF 110

SHEET

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REVISION
16.0.0

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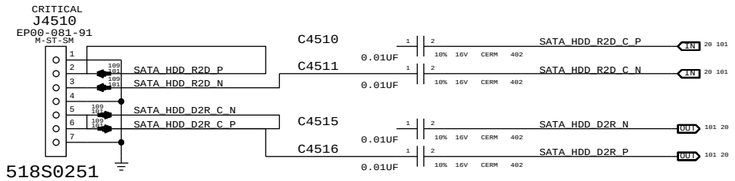
PAGE
44 OF 110

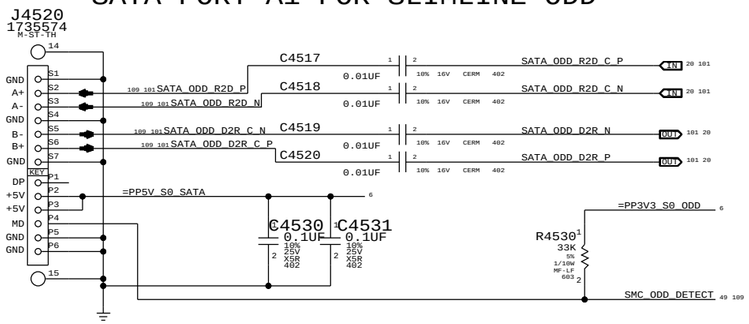
SHEET

SATA PORT A0 FOR HDD

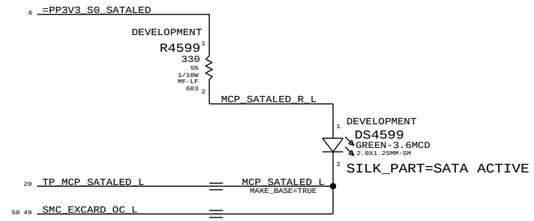


SATA PORT A1 FOR SLIMLINE ODD

518-0361



SATA Activity LED



PAGE TITLE: SATA Connectors

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SIZE: D

REVISION: 16.0.0

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PAGE: 45 OF 110

SHEET

USB/SMC DEBUG MUX

PORT 3

=PP5V_S3_USB
U4601 TPS2060 MSOP
USB_EXTC_OC_L
USB_EXTD_OC_L
R4600 10K 5% 1/16W MF-LF 402
USB_PWR_ENA_L
C4605 0.1UF 20% 10V CERM 402
C4606 150UF 20% 6.3V POLY-TANT CASE-D2-SM NOSTUFF CRITICAL
Q4600 2N7002 SOT23-HF
PM_EN_USB_PWR
C4621 0.1UF 20% 10V CERM 402
C4631 0.1UF 20% 10V CERM 402
=PP3V3_S5_SMCUSBMUX
C4650 0.1UF 20% 10V CERM 402
SMC_RX_L
SMC_TX_L
U4650 PI3USB102ZLE TQFN MOJOMUX
USB_EXTD_P
USB_EXTD_N
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
R4651 0 PRODUCTION 5% 1/10W MF-LF 402
R4652 0 PRODUCTION 5% 1/10W MF-LF 402
USB_D_MUXED_N
USB_D_MUXED_P
L4630 FERR-250-OHM SM CRITICAL
PP5V_USB2_PORT3 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT3_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4630 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4631 120-OHM-90MA DLP0NS CRITICAL
USB_PORT3_N
USB_PORT3_P
J4630 USB-K22 F-ANG-TH CRITICAL
VDD
D-
D+
GND
VBUS
DATA-
DATA+
514-0659
D4630 RCLAMP0502N SLP1210N6 CRITICAL
NC
IO

PORT 2

L4620 FERR-250-OHM SM CRITICAL
PP5V_USB2_PORT2 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT2_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4620 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4621 120-OHM-90MA DLP0NS CRITICAL
USB_EXTC_N
USB_EXTC_P
USB_PORT2_N
USB_PORT2_P
J4620 USB-K22 F-ANG-TH CRITICAL
D4620 RCLAMP0502N SLP1210N6 CRITICAL

PORT 1

U4600 TPS2060 MSOP
=PP5V_S3_USB
USB_EXTA_OC_L
USB_EXTB_OC_L
C4601 0.1UF 20% 10V CERM 402
C4602 150UF 20% 6.3V POLY-TANT CASE-D2-SM NOSTUFF CRITICAL
C4603 0.1UF 20% 10V CERM 402
C4611 0.1UF 20% 10V CERM 402
L4610 FERR-250-OHM SM CRITICAL
PP5V_USB2_PORT1 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT1_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4610 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4611 120-OHM-90MA DLP0NS CRITICAL
USB_EXTB_N
USB_EXTB_P
USB_PORT1_N
USB_PORT1_P
J4610 USB-K22 F-ANG-TH1 CRITICAL
D4610 RCLAMP0502N SLP1210N6 CRITICAL

PORT 0

L4600 FERR-250-OHM SM CRITICAL
PP5V_USB2_PORT0 VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
PP5V_USB2_PORT0_F VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
C4600 0.01UF 20% 16V CERM 402 (PUT CAP ON CONNECTOR SIDE)
L4601 120-OHM-90MA DLP0NS CRITICAL
USB_EXTA_N
USB_EXTA_P
USB_PORT0_N
USB_PORT0_P
J4600 USB-K22 F-ANG-TH1 CRITICAL
D4600 RCLAMP0502N SLP1210N6 CRITICAL

514-0672

PAGE TITLE: EXTERNAL USB CONNECTORS

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SIZE: D
REVISION: 16.0.0
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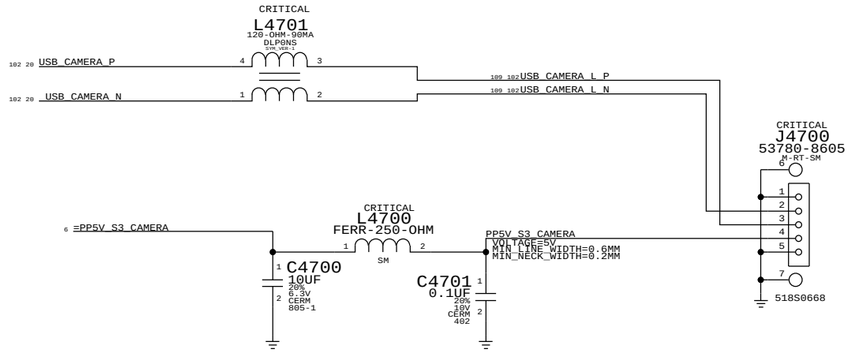
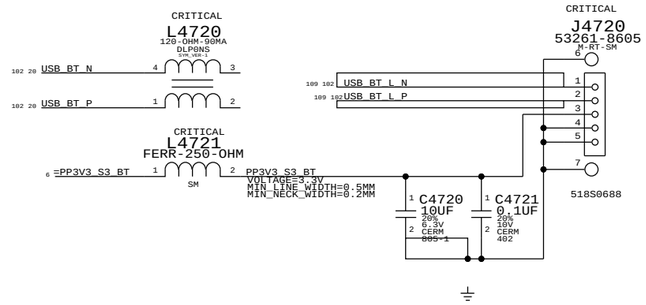
PAGE: 46 OF 110
SHEET

CAMERA CONNECTOR & FILTER

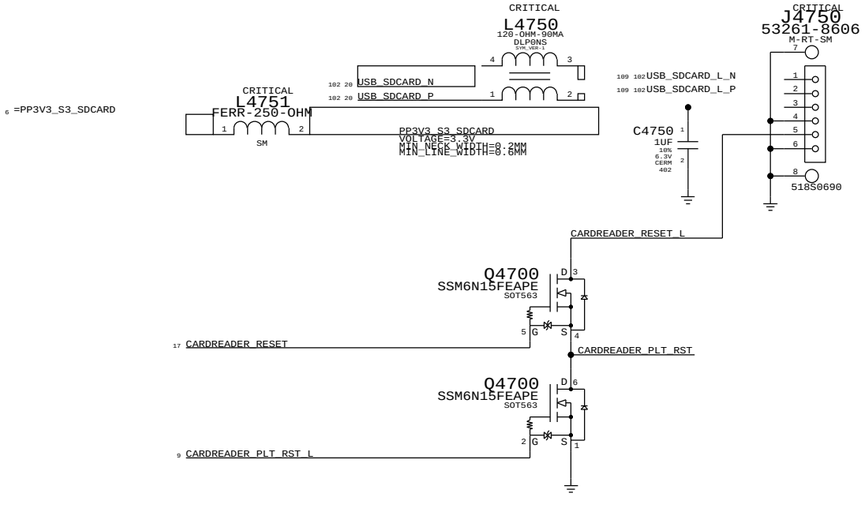


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

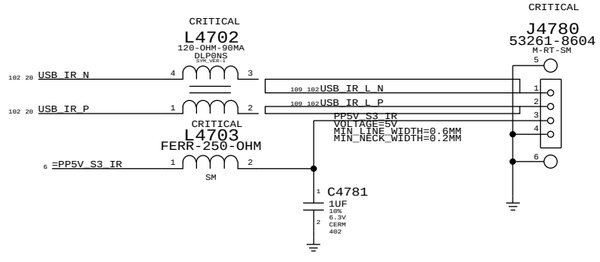
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



IR RECEIVER CONNECTOR



PAGE TITLE
Internal USB Connections

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
47 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

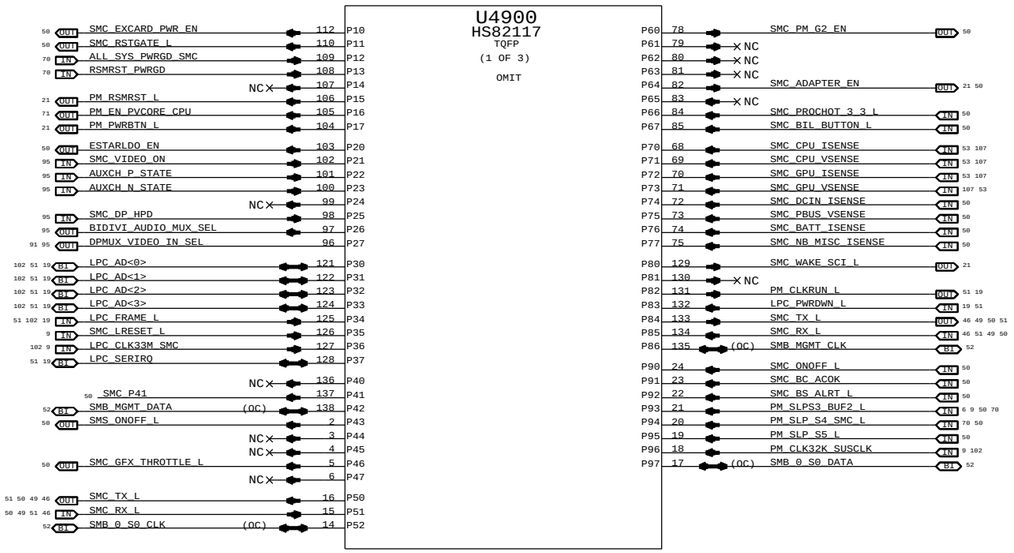
REVISION
16.0.0

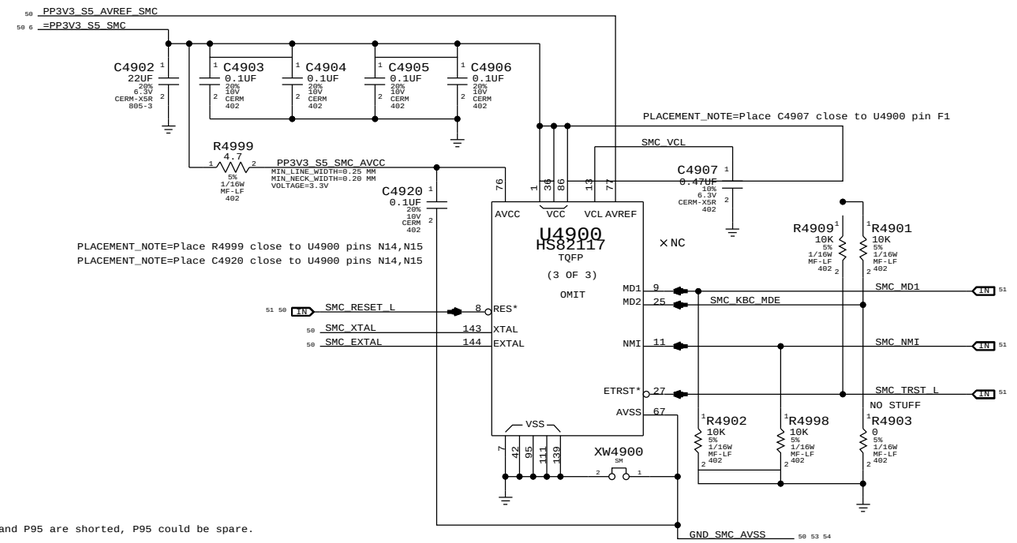
BRANCH

PAGE
48 OF 110

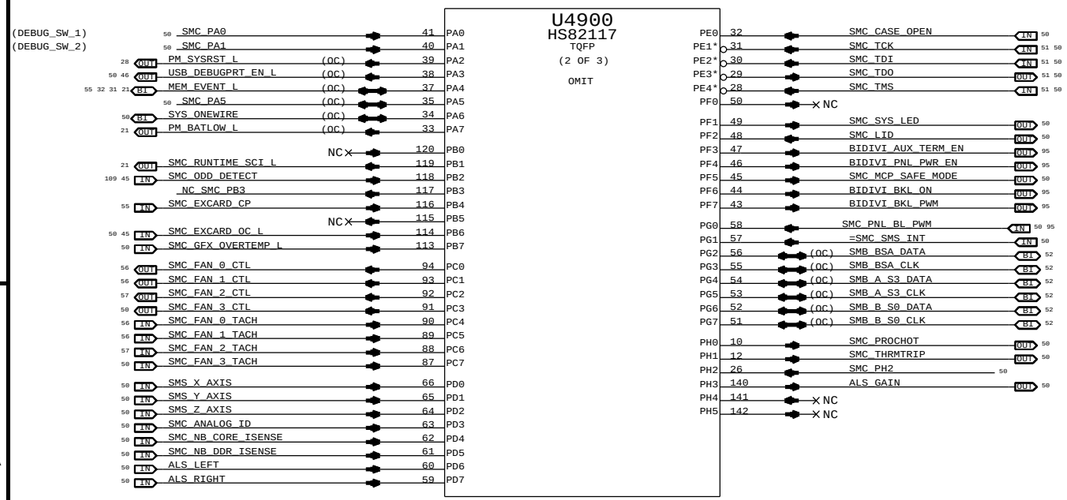
SHEET

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION 16.0.0
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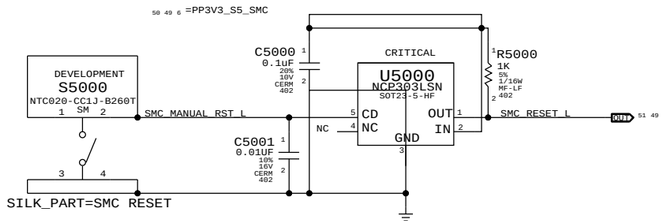
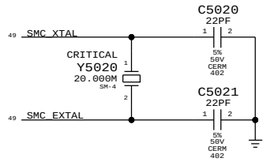
	SHEET

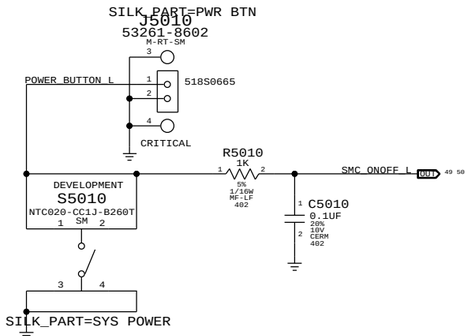
SMC Reset Button / Brownout Detect



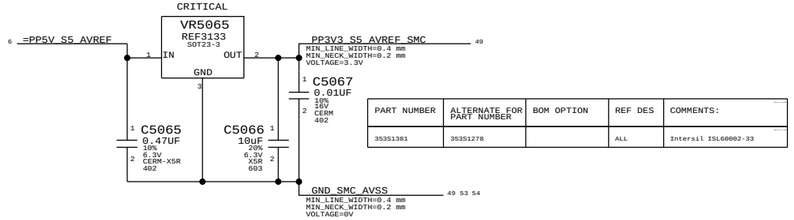
SMC Crystal Circuit



POWER BUTTON

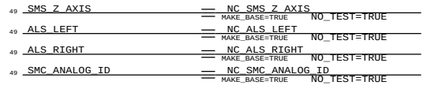


SMC AVREF Supply

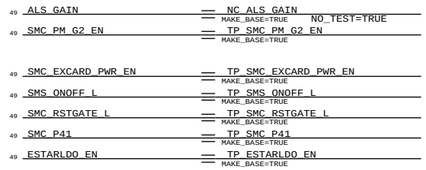


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

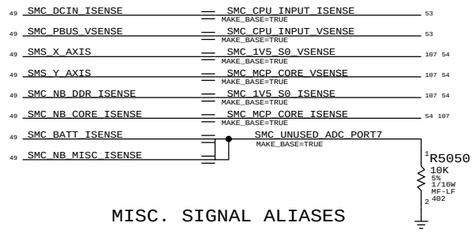
UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS



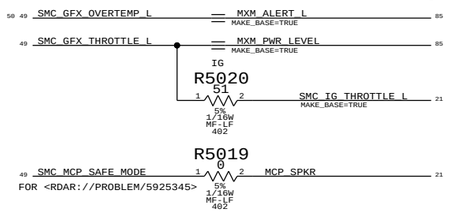
UNUSED TP/NC ALIASES



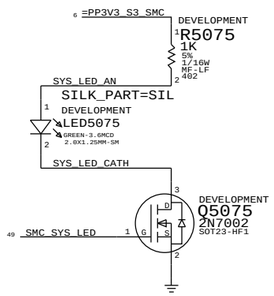
ANALOG SENSORS

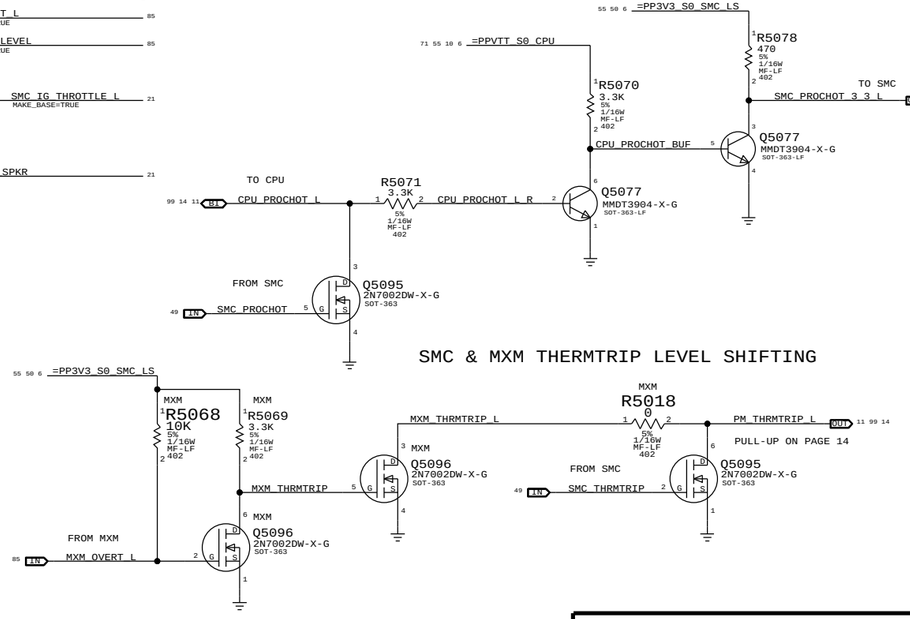


MISC. SIGNAL ALIASES



SIL: FOR DEVELOPMENT USE ONLY



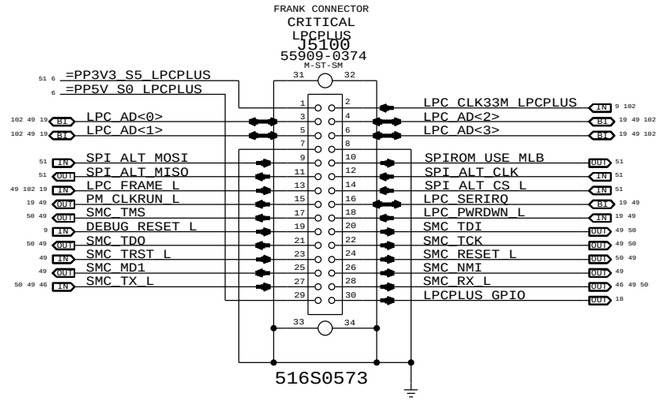


SMC PROCHOT 3.3V LEVEL SHIFTING

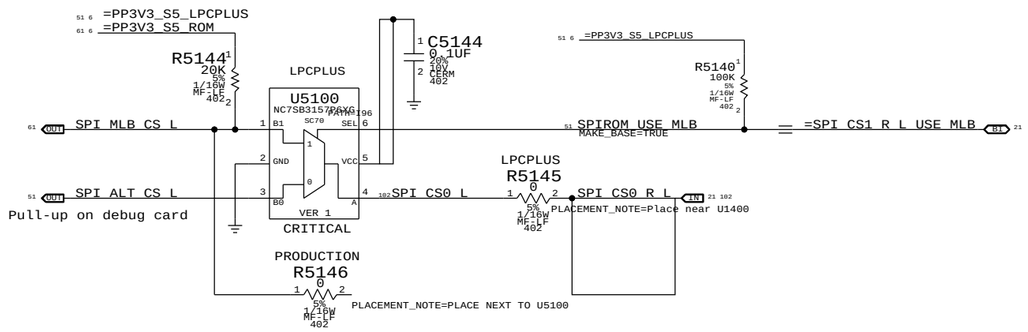
SMC & MXM THERMTRIP LEVEL SHIFTING

PAGE TITLE	SMC Support
	Apple Inc.
DRAWING NUMBER	SIZE D
REVISION	16.0.0
BRANCH	
PAGE	50 OF 110
SHEET	

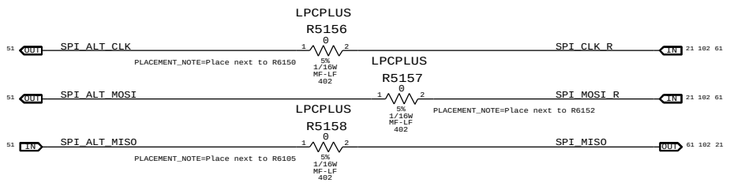
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER
SIZE D

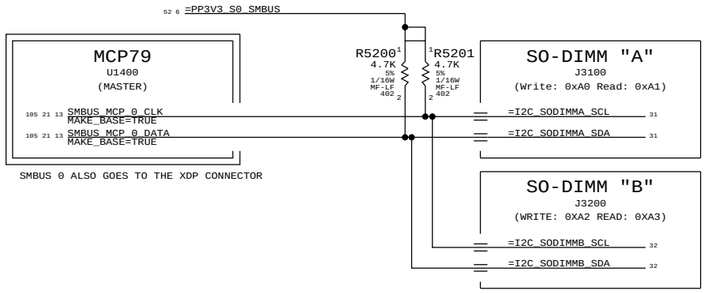
REVISION
16.0.0

BRANCH

PAGE
51 OF 110

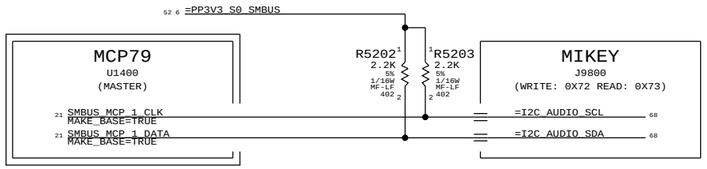
SHEET

MCP79 SMBUS "0" CONNECTIONS

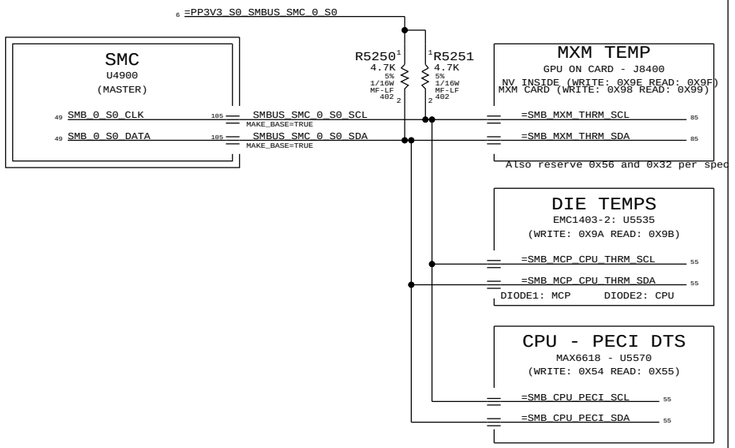


SMBUS 0 ALSO GOES TO THE XDP CONNECTOR

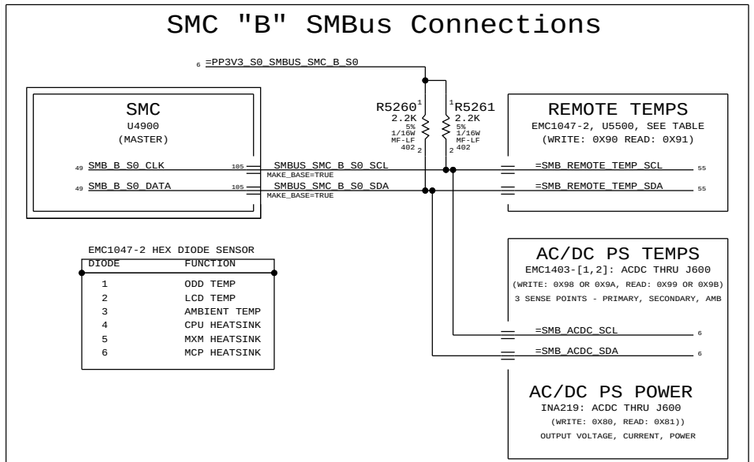
MCP79 SMBUS "1" CONNECTIONS



SMC "0" SMBus Connections

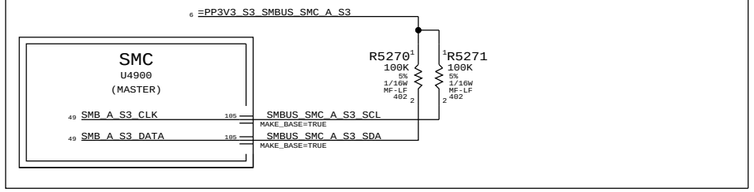


SMC "B" SMBus Connections

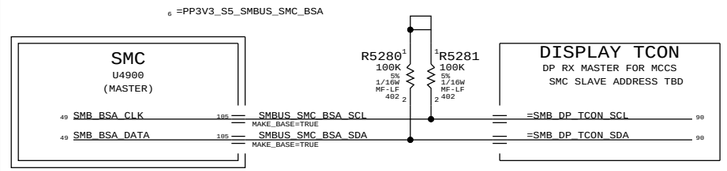


SMC "A" SMBus Connections

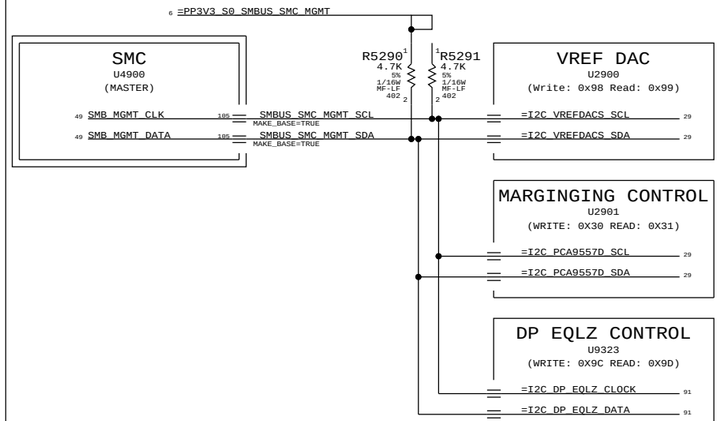
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE



POTENTIAL SMC SLAVE SMBUS CONNECTIONS



SMC "MANAGEMENT" SMBUS CONNECTIONS



PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER | SIZE: D

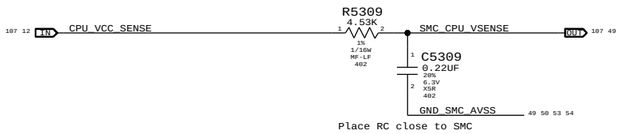
REVISION: 16.0.0

BRANCH

PAGE: 52 OF 110

SHEET

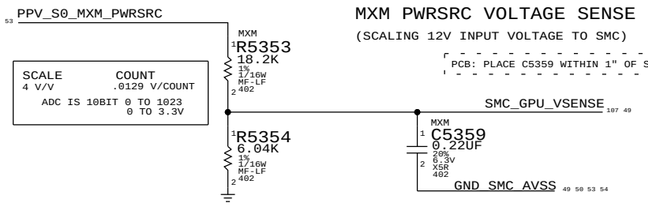
CPU Voltage Sense / Filter



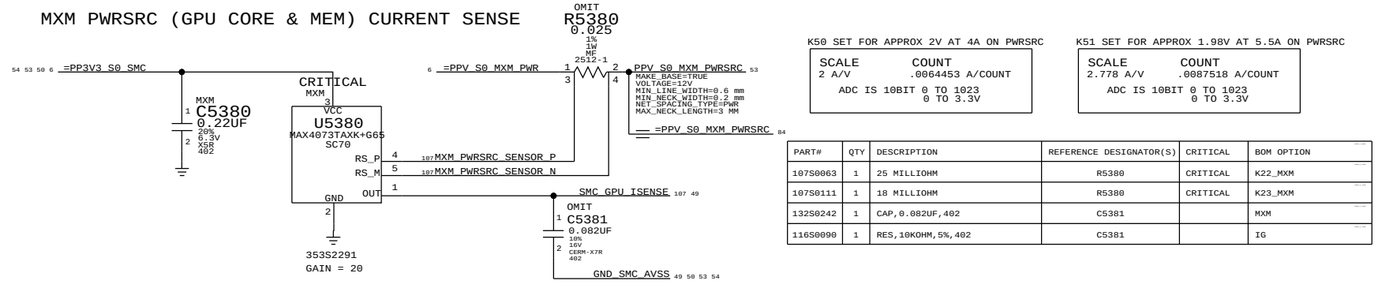
Place RC close to SMC

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K50 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023
0 TO 3.3V

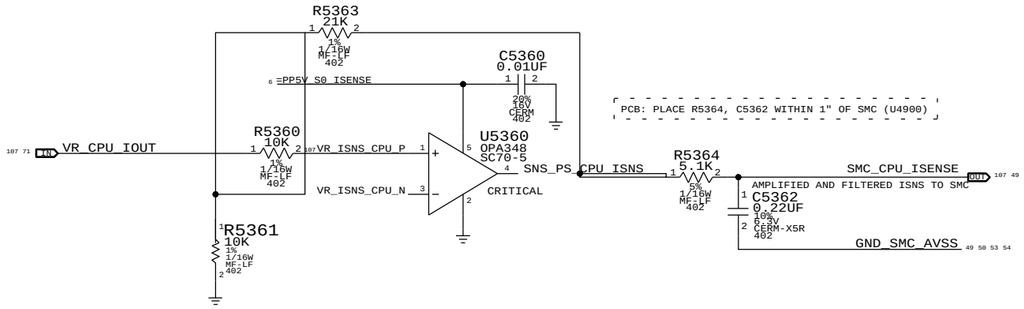
K51 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

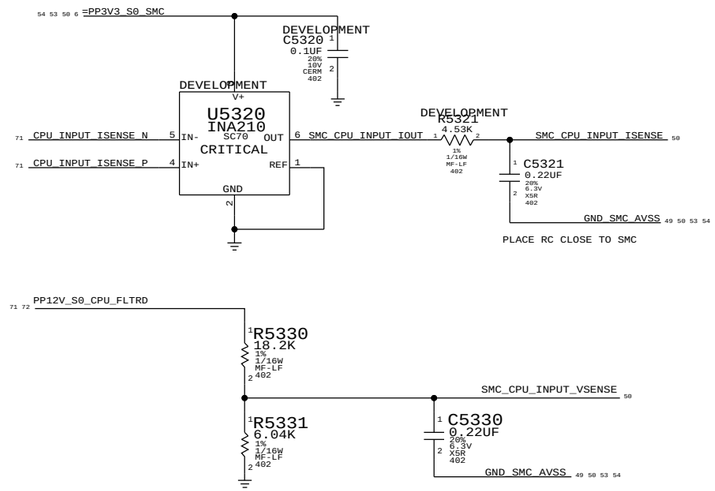
ADC IS 10BIT 0 TO 1023
0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K22_MXM
107S0111	1	18 MILLIOHM	R5380	CRITICAL	K23_MXM
132S0242	1	CAP,0.082UF,402	C5381		MXM
116S0090	1	RES,10KOHM,5%,402	C5381		IG

CPU CURRENT SENSE AMP & FILTER

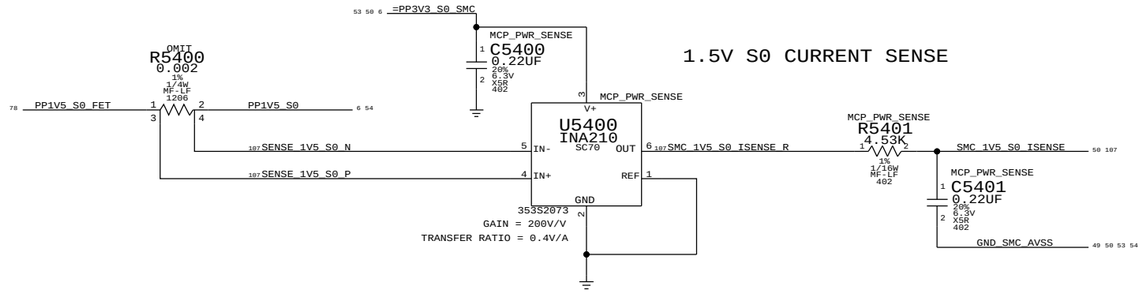


CPU CORE INPUT SIDE CURRENT & VOLTAGE SENSE



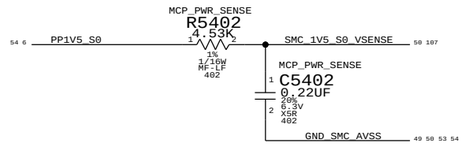
PAGE TITLE	CPU/MXM CURRENT AND VOLTAGE SENSE
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION 16.0.0
	BRANCH
	PAGE 53 OF 110
	SHEET

1.5V S0 CURRENT SENSE

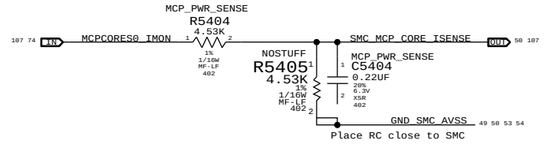


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
104S0018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
101S0414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

1.5V S0 VOLTAGE SENSE

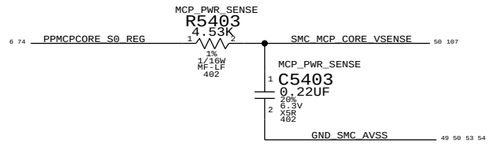


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



PAGE TITLE
MCP CURRENT AND VOLTAGE SENSE

Apple Inc.

DRAWING NUMBER
SIZE D

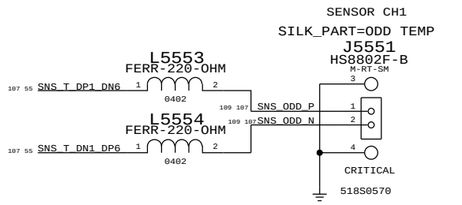
REVISION
16.0.0

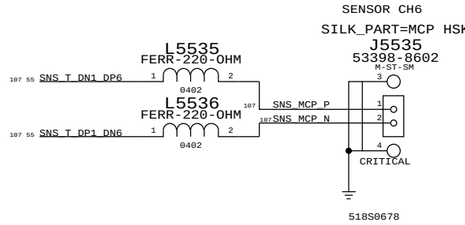
BRANCH

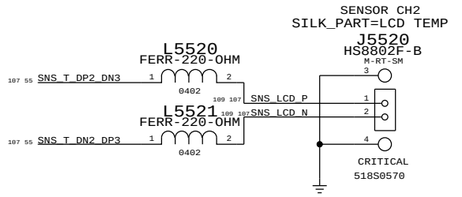
PAGE
54 OF 110

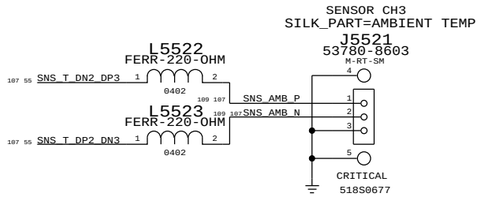
SHEET

REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD

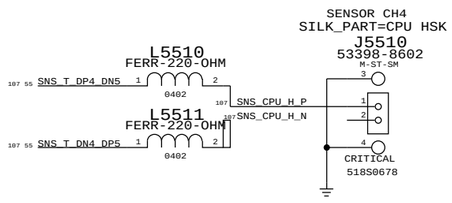


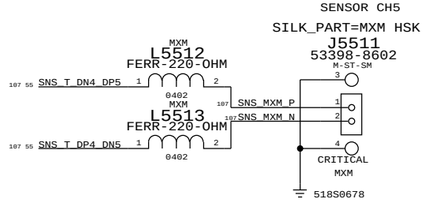




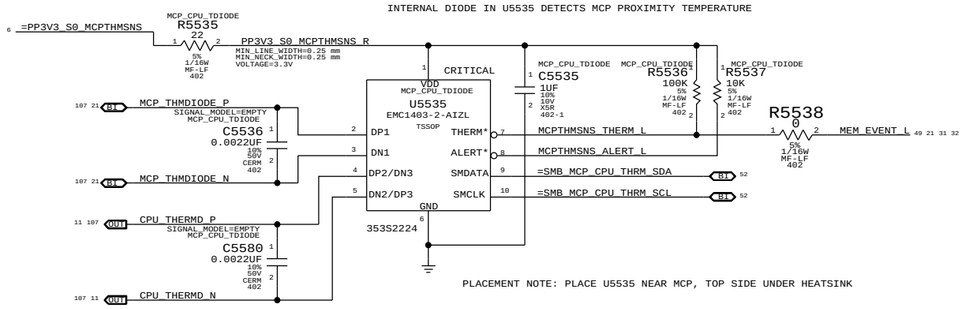


PLACE HSK SENSOR CONN. TOP SIDE NEAR MXM OR CPU

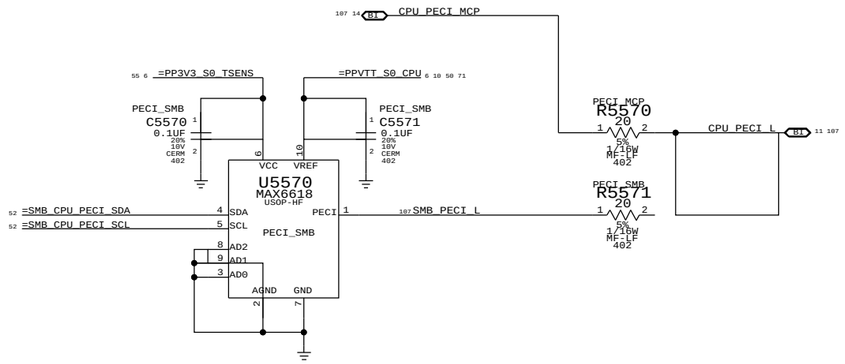




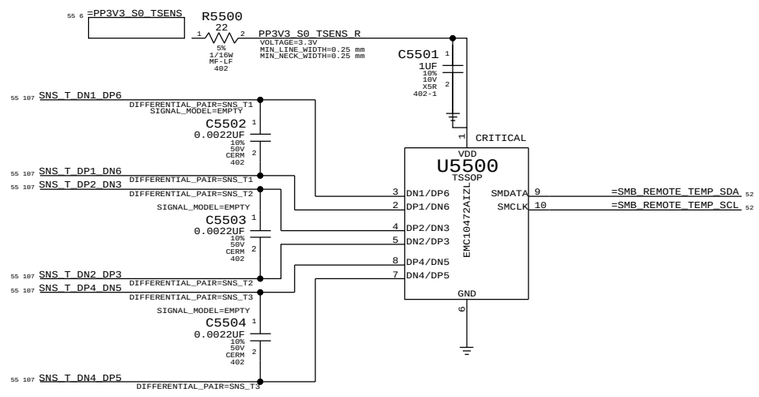
MCP & CPU T-Diode Thermal Sensor



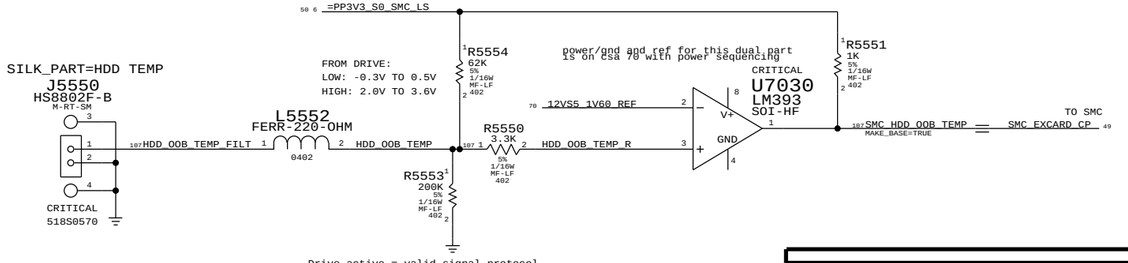
CPU PECI DTS OPTIONS



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



PAGE TITLE	Thermal Sensors
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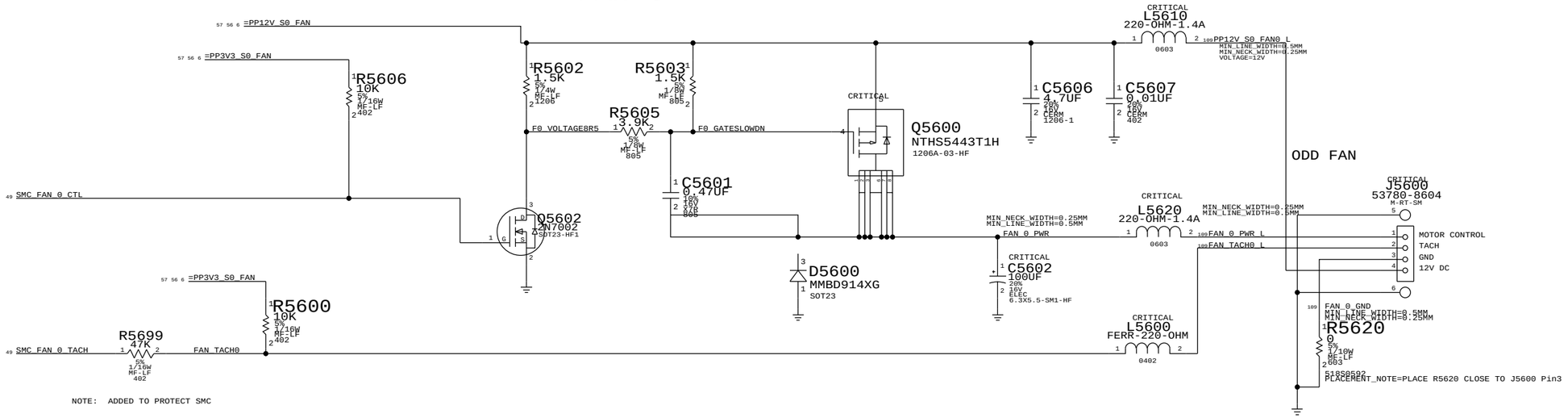
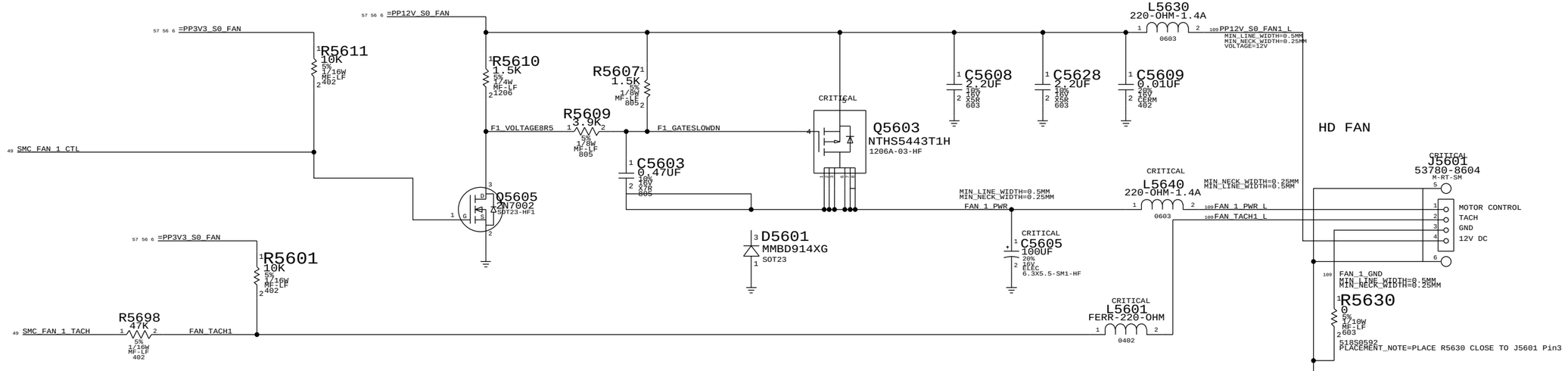
FAN 0



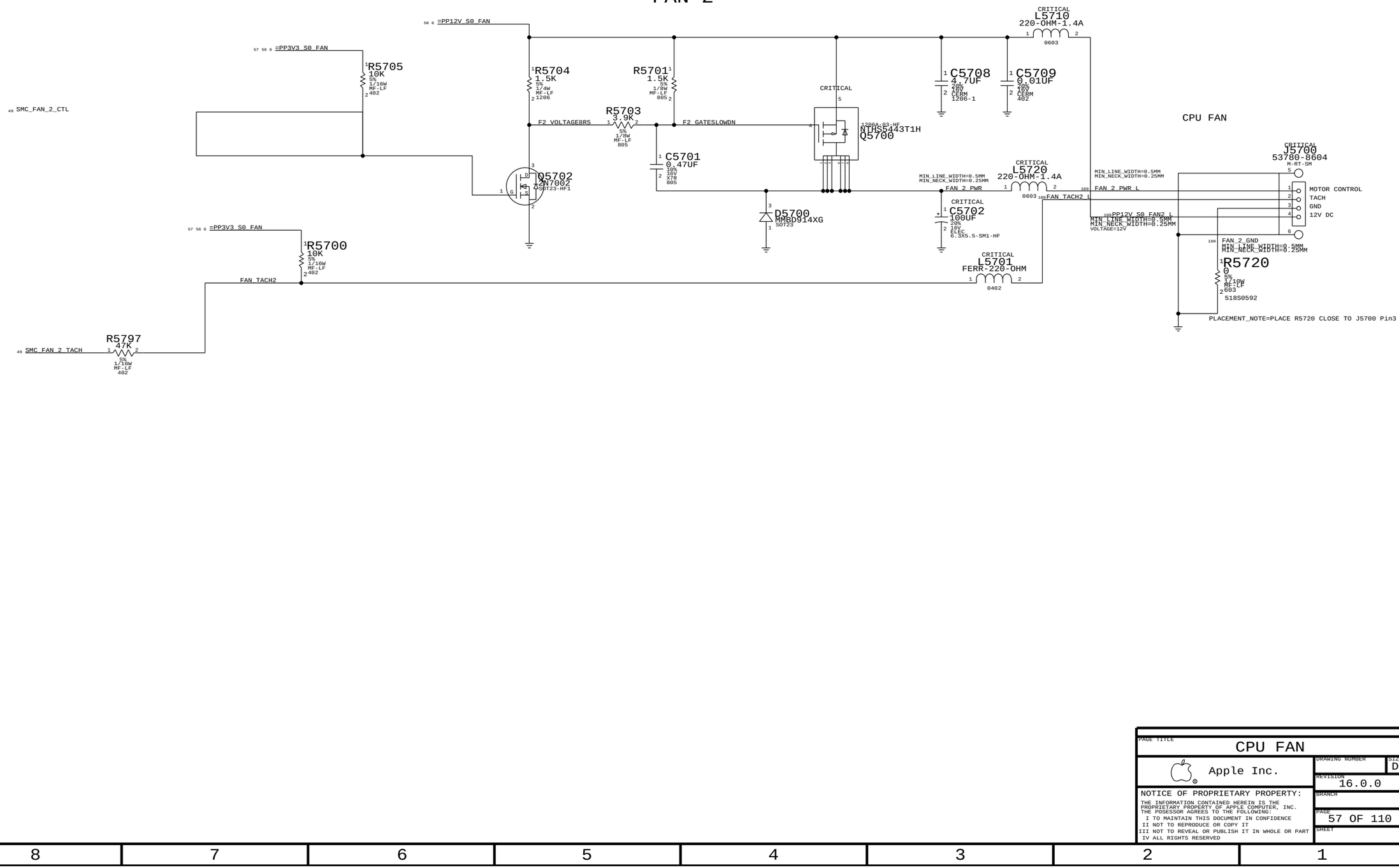
NOTE: ADDED TO PROTECT SMC

FAN 1



PAGE TITLE	HD AND OD FAN
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION 16.0.0
	BRANCH
	PAGE 56 OF 110
	SHEET

FAN 2



PAGE TITLE	CPU FAN
	Apple Inc.
DRAWING NUMBER	SIZE D
REVISION	16.0.0
BRANCH	
PAGE	57 OF 110
SHEET	

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
58 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
59 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
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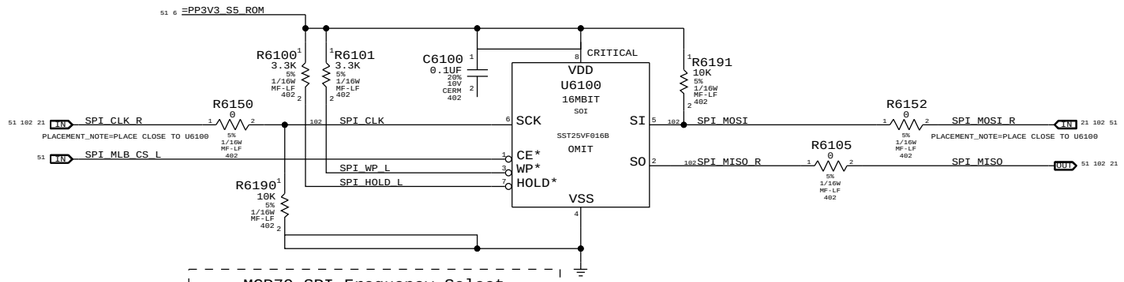
DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
60 OF 110

SHEET



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues ‘READ’ (0x03) commands not ‘READ_FAST’ (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

PAGE TITLE: SPI ROM

Apple Inc.

DRAWING NUMBER

SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 61 OF 110

SHEET

AUDIO CODEC
APPLE P/N 353S2592

=PP1V5_S0_AUD_DIG

C6203 4.7UF 20% 4V X5R 402
C6258 0.47UF 10% 10V X5R 402
C6260 10UF 20% 16V POLY-TANT CASE-B2-SM
C6204 10UF 20% 6.3V X5R 603
C6205 10UF 20% 6.3V X5R 603
C6259 1UF 10% 10V X5R 402-1
C6264 0.47UF 10% 10V X5R 402
C6265 0.47UF 10% 10V X5R 402
C6261 0.47UF 10% 10V X5R 402
C6262 10UF 20% 16V POLY-TANT CASE-B2-SM
C6213 CRITICAL 10UF 20% 6.3V X5R 603

=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG VOLTAGE=4.5V MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM
GND_AUDIO_HP_AMP_L
GND_AUDIO_CODEC

R6255 2.67K 1% 1/16W MF-LF 402

K22 = NC
K23 LOW = S/PDIF IN, HIGH = DP SPDIF

U6201 CS4206ACNZC QFN

		VD	9		
		VA_REF	24		
		VA_HP	46		
		VA	25		
VBIAS_DAC	29	VBIAS_DAC			
CS4206 FP	44	VHP_FILT+	CRITICAL	HPOUT_L	38
CS4206 FN	41	VHP_FILT-		HPOUT_R	40
				HPREF	39
AUD_MUX_CNTRL	95				
AUD_GPIO_1	62	GPIO0/DMIC_SDA1	2	LINEOUT_L1+	35
		GPIO1/DMIC_SDA2/SPDIF_OUT2	12	LINEOUT_L1-	34
AUD_GPIO_2	64 68	GPIO2	14	LINEOUT_R1+	36
AUD_GPIO_3	65 64 68	GPIO3	15	LINEOUT_R1-	37
AUD_SENSE_A	67	SENSE_A	13	LINEOUT_L2+	31
				LINEOUT_L2-	30
				LINEOUT_R2+	32
				LINEOUT_R2-	33
				MICBIAS	16
				VCOM	28
				LINEIN_L+	21
				LINEIN_C-	22
				LINEIN_R+	23
				MICIN_L+	18
				MICIN_L-	17
				MICIN_R+	19
				MICIN_R-	20
				VREF+_ADC	27
				DMIC_SCL	4
		DGND_THRM_PAD_AGND	7 49 26		

HPOUT_L: MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
HPOUT_R: MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
HPREF: MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

AUD_HP_PORT_L
AUD_HP_PORT_R
AUD_HP_PORT_REF
AUD_LO1_P_L
TP_AUD_LO1_N_L NC
AUD_LO1_P_R
TP_AUD_LO1_N_R NC
AUD_LO2_P_L
TP_AUD_LO2_N_L NC
AUD_LO2_P_R
TP_AUD_LO2_N_R NC
AUD_CODEC_MICBIAS
CS4206_VCOM
AUD_LI_P_L
MAKE_BASE=TRUE
AUD_LI_COM
AUD_LI_P_R
AUD_MIC_INP_L
AUD_MIC_INN_L
AUD_MIC_INP_R
AUD_MIC_INN_R
CS4206_VREF_ADC NC
TP_AUD_DMIC_CLK NC

AUD_LI_N_L
AUD_LI_N_R

C6206 2.2UF 20% 6.3V CERM 402-LF
C6208 2.2UF 20% 6.3V CERM 402-LF
CS4206_FLYP
CS4206_FLYC
CS4206_FLYN

HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
AUD_SPDIF_IN_CODEC
AUD_SPDIF_OUT

R6254 22 5% 1/10W MF-LF 402
AUD_SDI_R
R6257 22 5% 1/10W MF-LF 402
AUD_SPDIF_CHIP

R6295 100K 1% 1/10W MF-LF 402
NOSTUFF R6263 0 5% 1/16W MF-LF 402

CRITICAL C6211 1UF 10% 20V TANT CASE-R-HF
CRITICAL C6263 10UF 20% 16V POLY-TANT CASE-B2-SM
NOSTUFF R6267 100K 5% 1/10W MF-LF 402

GND_AUDIO_CODEC
XW6201 SM
GND_AUDIO_HP_AMP_L
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
VOLTAGE=0V

BETTER
R6299 100K 5% 1/16W MF-LF 402
AUD_GPIO_1
EDUCATION
R6298 10K 5% 1/16W MF-LF 402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

HP OUT ZOBEL NETWORK

AUD_HP_PORT_L
AUD_HP_PORT_R
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
C6298 0.1UF 10% 16V X7R-CERM 402
C6297 0.1UF 10% 16V X7R-CERM 402
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
AUD_Z_R NC
AUD_Z_L NC
R6296 39 5% 1/16W MF-LF 402
R6297 39 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.30MM MIN_NECK_WIDTH=0.20MM
GND_AUDIO_HP_AMP_L

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=5V
L6201 FERR-220-OHM 0402
=PP5V_S0_AUDIO
R6201 2.21K 1% 1/10W MF-LF 402
=PP3V3_S0_AUDIO
4V5_REG_IN
4V5_REG_EN

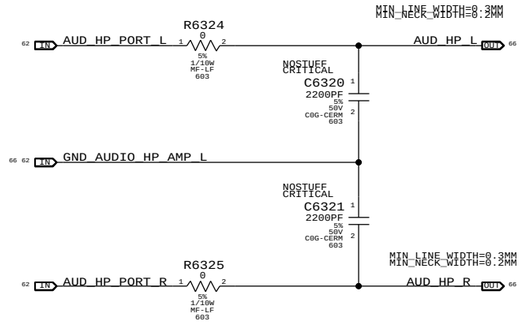
VR6201 TPS71745 SON CRITICAL
IN
EN
GND
NR/FB
NC
OUT
4V5_NR

MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.10MM VOLTAGE=4.5V
PP4V5_AUDIO_ANALOG

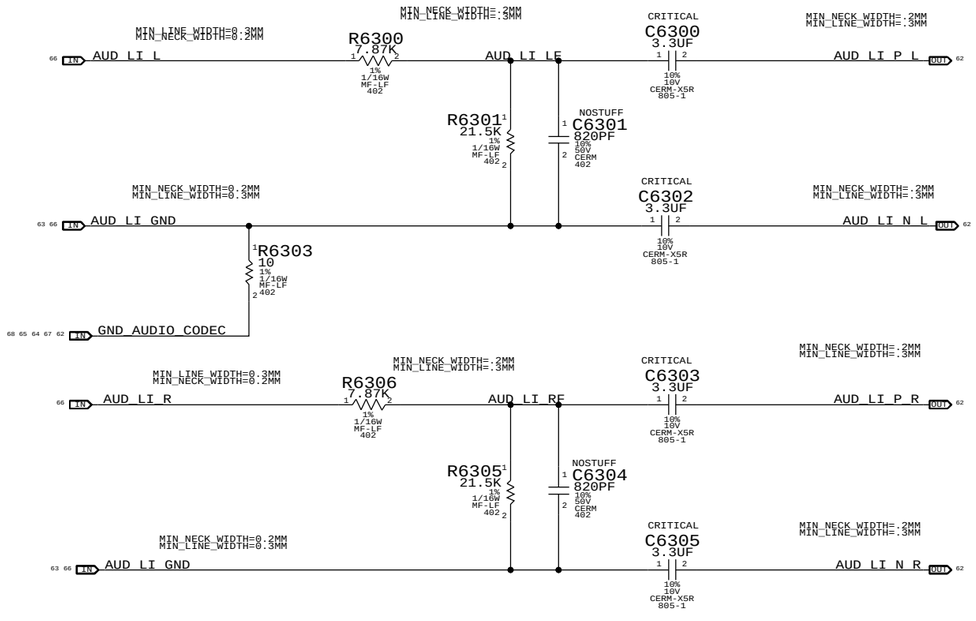
C6201 1UF 10% 10V X5R 402-1
C6202 1UF 10% 10V X5R 402-1
C6266 0.1UF 10% 16V X7R-CERM 402
C6207 1UF 10% 10V X5R 402-1
GND_AUDIO_CODEC

PAGE TITLE	AUDIO: CODEC/REGULATOR
	Apple Inc.
DRAWING NUMBER	
SIZE	D
REVISION	16.0.0
BRANCH	
PAGE	62 OF 110
SHEET	

1ST ORDER DAC FILTER PLACEHOLDER



CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 63 OF 110
SHEET

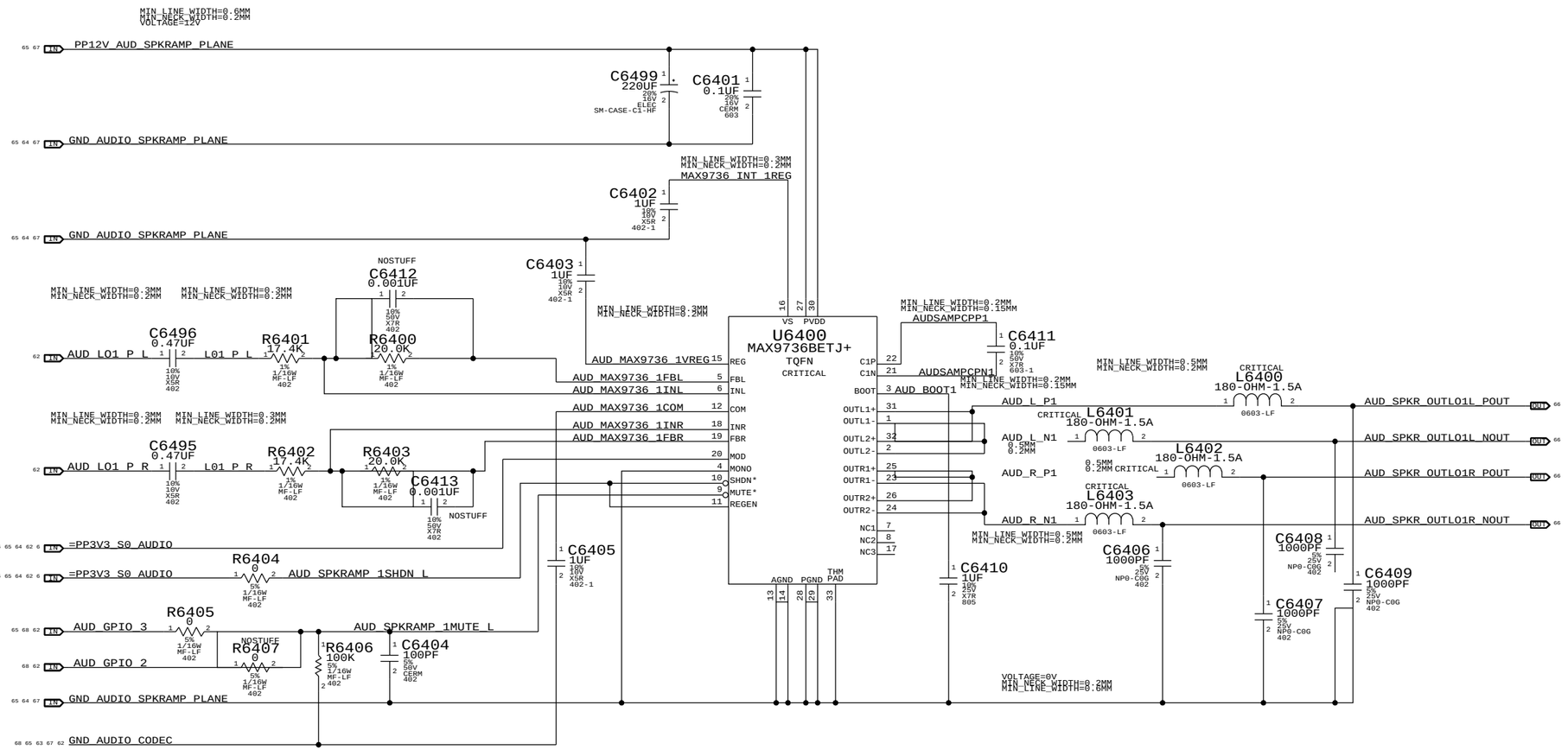
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



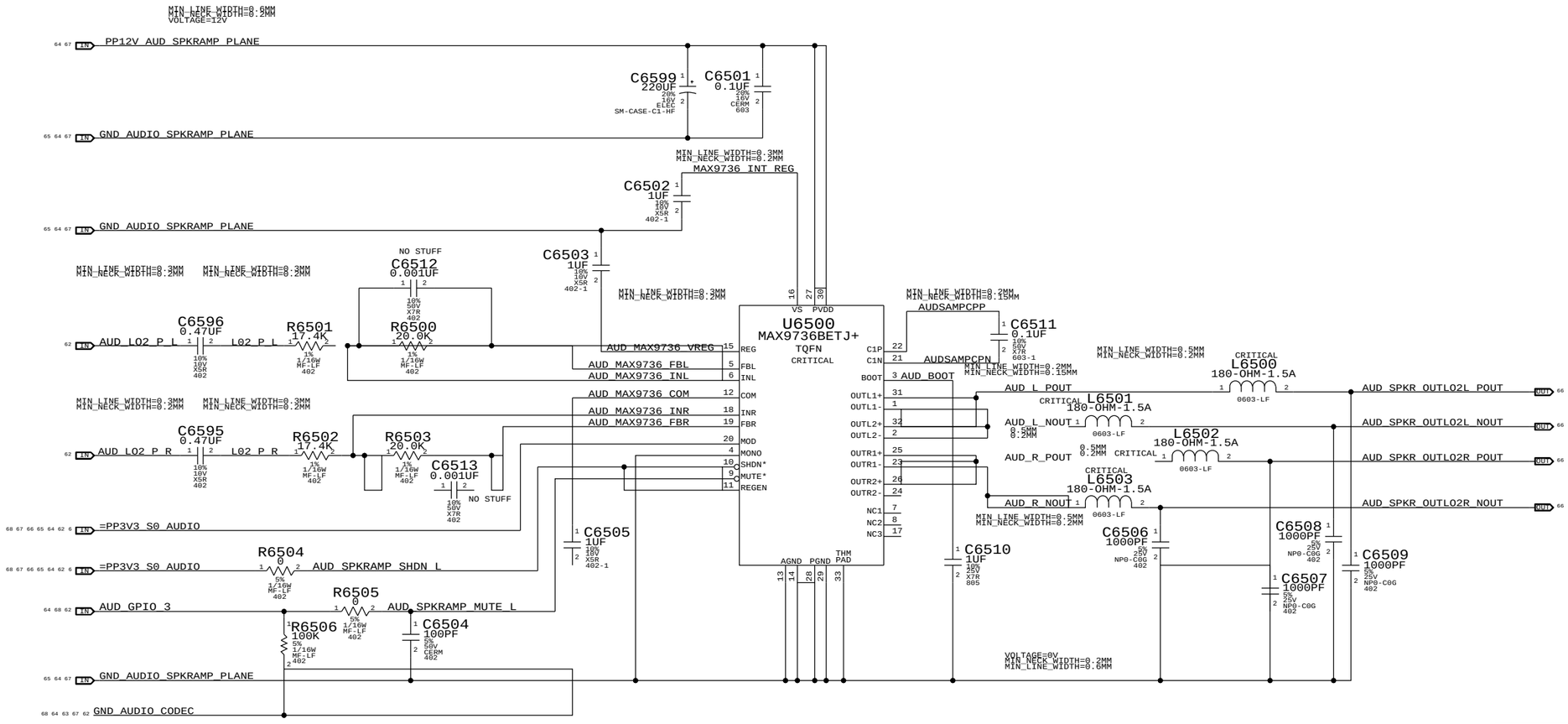
PAGE TITLE	AUDIO: Tweeter Amp 1
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION 16.0.0
	BRANCH
	PAGE 64 OF 110
	SHEET

WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

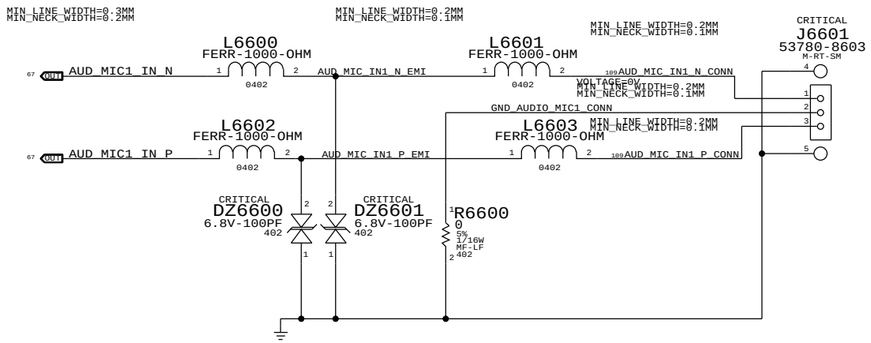
GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

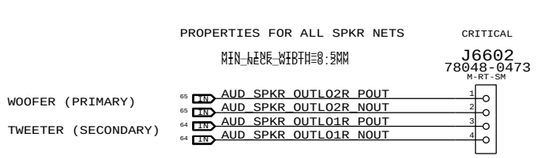


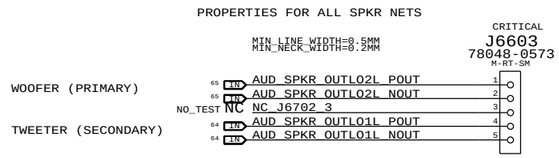
PAGE TITLE	AUDIO: Woofer Amp
	Apple Inc.
DRAWING NUMBER	SIZE D
REVISION	16.0.0
BRANCH	
PAGE	65 OF 110
SHEET	

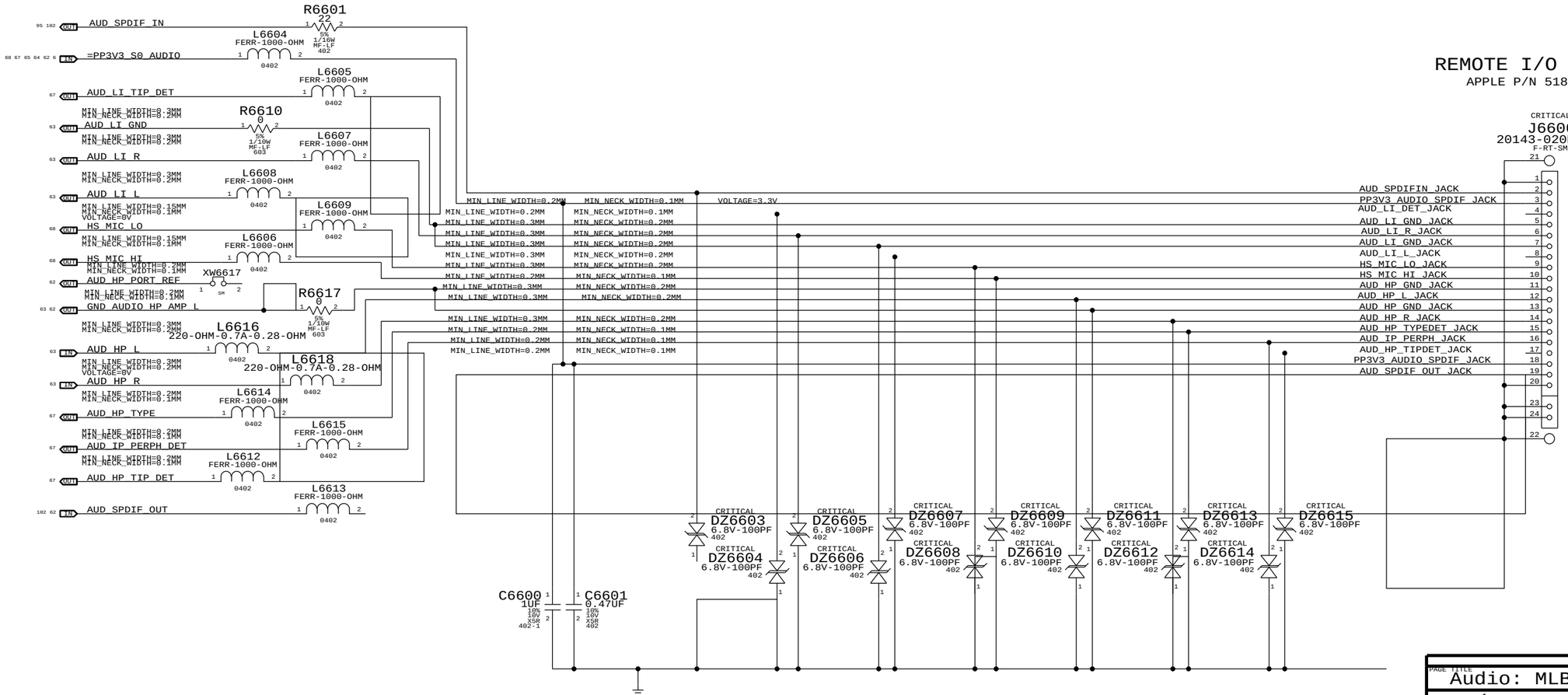
INTERNAL MIC CON
APPLE P/N 518S0677



SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656







REMOTE I/O CONNECTOR
APPLE P/N 518S0723

PAGE TITLE
Audio: MLB to I/O Conn.

Apple Inc.

DRAWING NUMBER
SIZE D

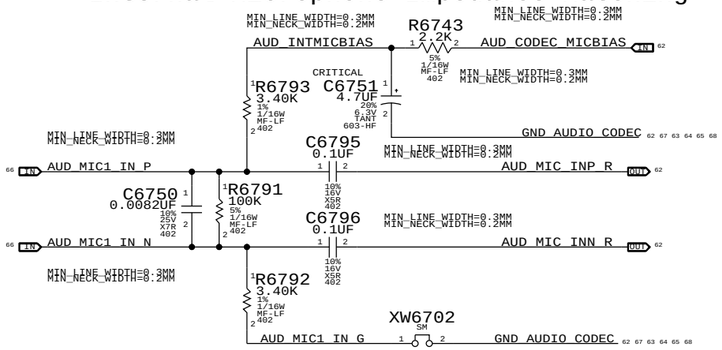
REVISION
16.0.0

BRANCH

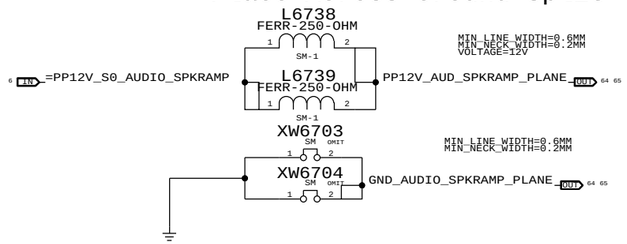
PAGE
66 OF 110

SHEET

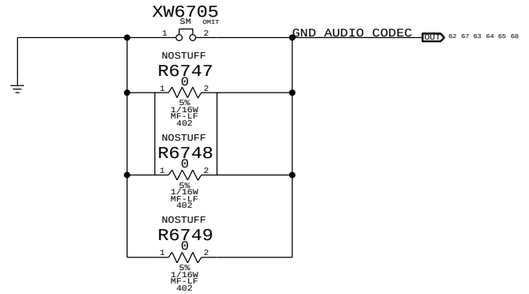
Internal Microphone Impedance Matching



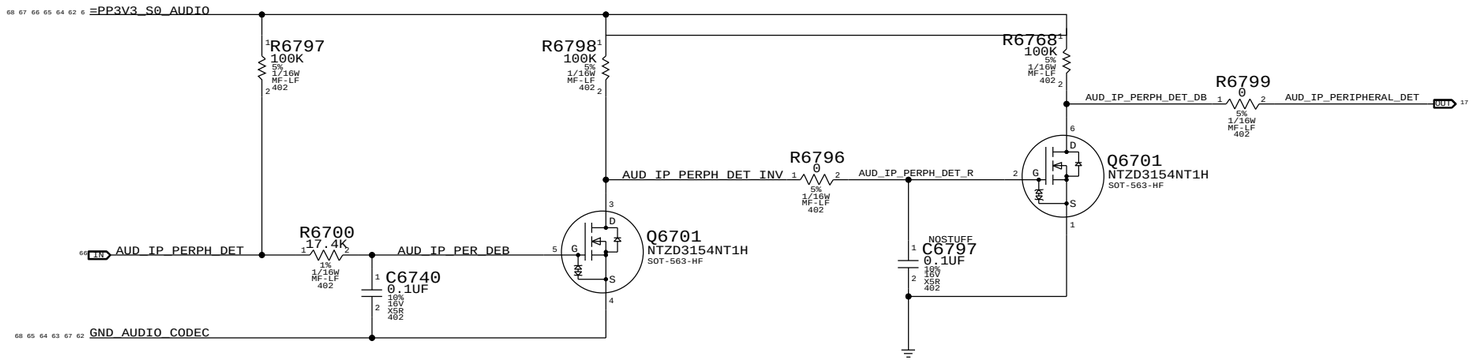
Place Across Ground Split



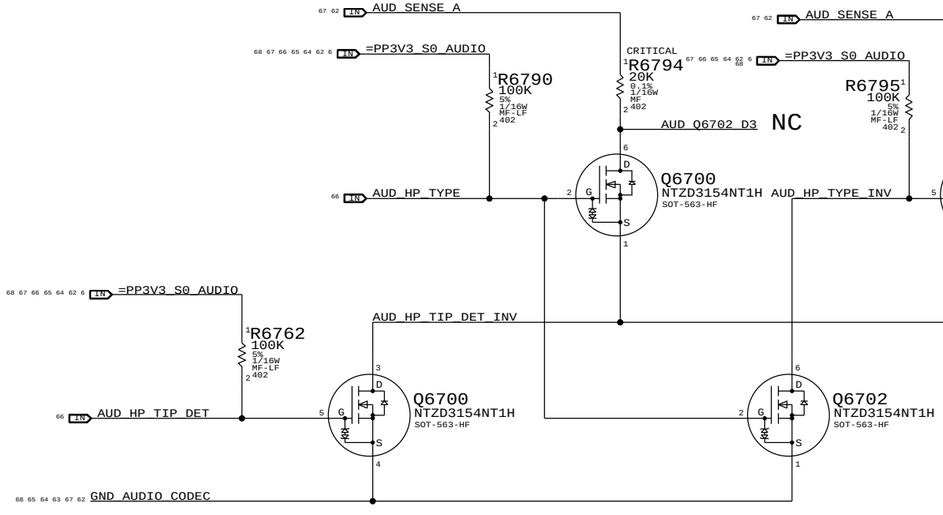
Audio Ground Returns



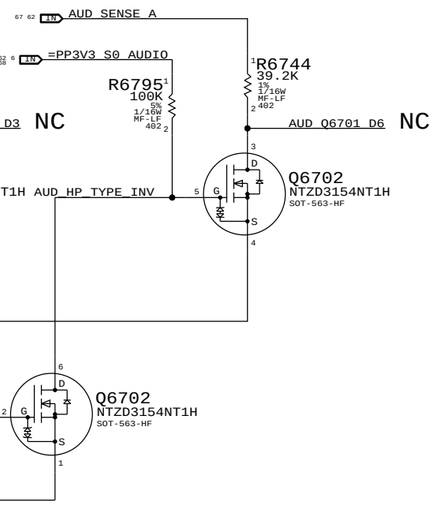
IPHS HS Detect Debounce CKT



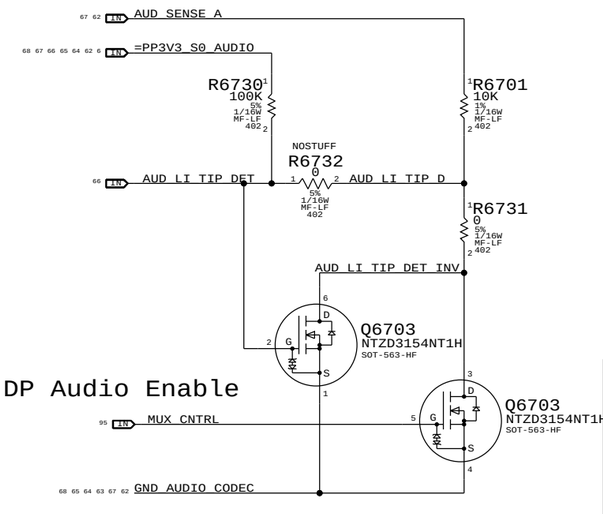
Digital Out



Headphone Out



LI Insert Detect



PAGE TITLE
AUDIO: Detects/Grounding

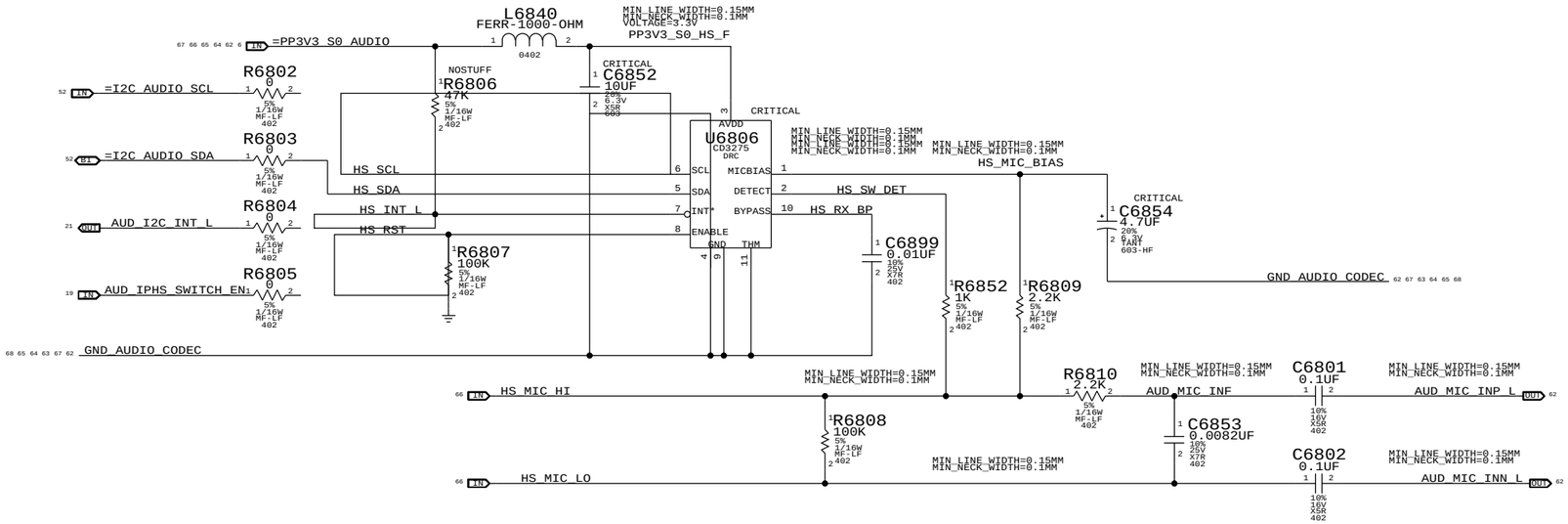
Apple Inc.

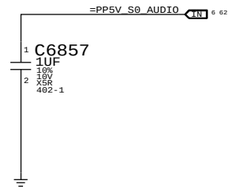
DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 67 OF 110
SHEET

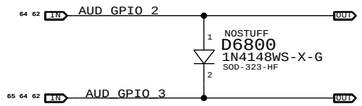
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2256



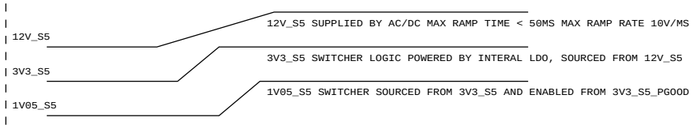




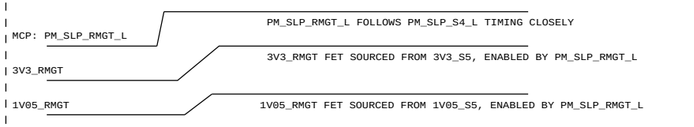
FLP = 8.82 KHZ
FHP = 80 HZ

PAGE TITLE	AUDIO: Mikey
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION 16.0.0
	BRANCH
	PAGE 68 OF 110
	SHEET

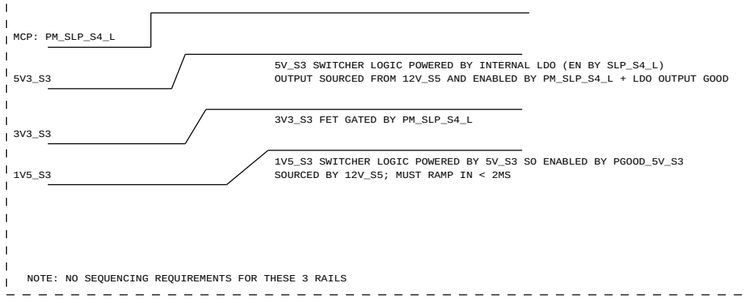
S5 POWER RAIL SEQUENCING



RMGT POWER RAIL SEQUENCING

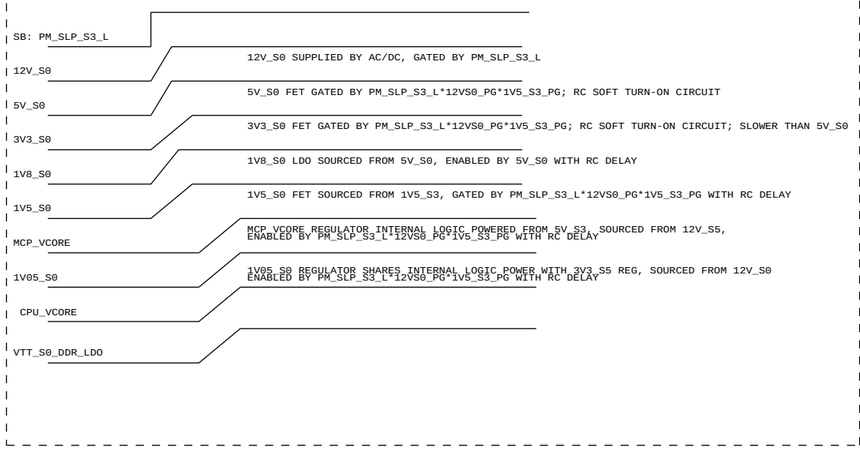


S3 POWER RAIL SEQUENCING

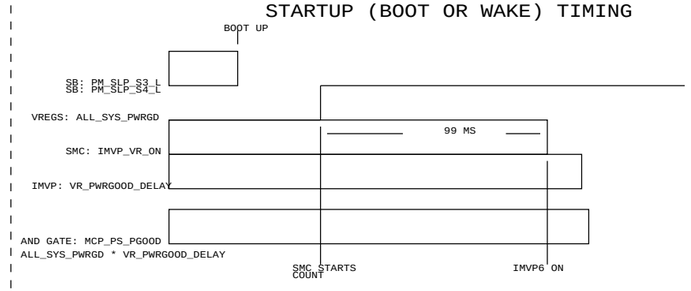


NOTE: NO SEQUENCING REQUIREMENTS FOR THESE 3 RAILS

S0 POWER RAIL SEQUENCING

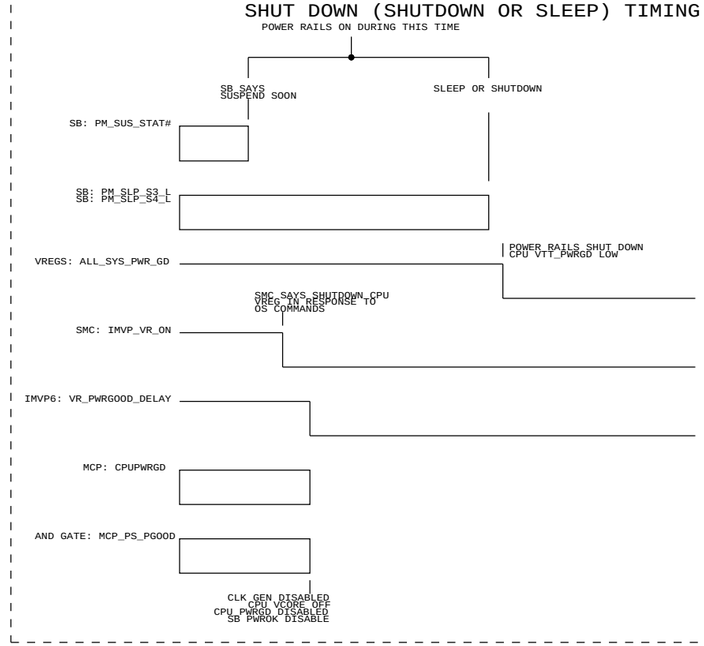


STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



PAGE TITLE
POWER SEQUENCING BLOCK DIAGRAM

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 69 OF 110
SHEET

Power Control Signals
3.3V,5V S3 enable

State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

FROM MCP (6)
PM_SLP_RMGT_L → R7050 0 → ENET_EN
PM_SLP_S4_L (PM_S4_STATE_L) → NOSTUFF R7051 33 (PLACEMENT_NOTE=Place close to U1400)
R7052 33 → P3V3S3_EN (PLACEMENT_NOTE=Place close to U1400) — Enable FET
R7053 33 → 5VREG_EN (PLACEMENT_NOTE=Place close to U1400) — ENABLE REGULATOR
R7054 33 → PM_SLP_S4_SMC_L (PLACEMENT_NOTE=Place close to U1400) — To SMC

=PP5V_S3_PWRCTL → R7072 100K → PGOOD_5V_S3 (MAKE_BASE=TRUE) → =DDRREG_EN — Enable regulator

PGOOD_5V_S3 → PM_EN_USB_PWR — USB Port Switch

MXM POWER SEQUENCE

=PM_MXM_PGOOD_PULLUP → ALL_SYS_PWRGD_R (MAKE_BASE=TRUE) → PM_MXM_EN

MXM CARD INPUT POWER ARE 12V_S0, 3V3_S0, 5V_S0
ALL_SYS_PWRGD ENABLES MXM REGULATORS
PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

=PP3V3_S5_PWRCTL → C7058 0.1UF
R7040 10K (MAKE_BASE=TRUE)
FROM COMPARATOR PGOOD_1V5_S3
FROM COMPARATOR PGOOD_12V_S0
U7059 TC7SZ08AFEAPE SOT665
PM_SLPS3_BUF2_L (PM_SLP_S3_L) → (PM_SLP_S3_L_BUF)
From SMC (6)
PM_SLP_S3_L_AND_S0_RDY
R7085 33 (MAKE_BASE=TRUE, PLACEMENT_NOTE=Place close to U7059) → P5VS0_EN → =P5VS0_EN — Enable FET

R7080 30K, R7081 43K, R7082 10K, R7083 2.2K (5% 1/16W MF-LF 402)
C7080 0.47UF, C7081 0.47UF, C7082 0.47UF, C7083 0.47UF (10% 6.3V CERM-X5R 402)
P3V3S0_EN (MAKE_BASE=TRUE) → =P3V3S0_EN — Enable FET
MCPDDR_EN (MAKE_BASE=TRUE) → =MCPDDR_EN — Enable FET DELAY OF ~15MS FROM PM_SLP_S3_L
CPUVTTS0_EN (MAKE_BASE=TRUE) → =PVTT_S0_EN — Enable regulator DELAY OF ~18MS FROM PM_SLP_S3_L
MCPCORES0_EN (MAKE_BASE=TRUE) → =MCPCORES0_EN — Enable regulator DELAY OF ~16MS FROM PM_SLP_S3_L

1.5V_S3 NEED TO BE ON BEFORE S0 FET ON
12V_S0 NEED TO BE ON BEFORE MCP REG AND 1.05_S0 REG EN

=PP3V3_S5_PWRCTL → R7031 1K → PGOOD_1V1_S5 — 1V05V_S0 DERIVES FROM 3.3V_S5
RSMRST_PWRGD → To SMC (2) — FROM THIS SMC GENERATES PM_RSMRST_L WHICH GOES INTO PGOOD_S8 OF MCP
C7031 0.1UF (10% 16V X5R 402) — DELAY IS ABOUT 200MS

HYSTERESIS NUMBERS CALCULATED BASED ON OUPTPUT PULL UP OF 3.3V

PGOOD Comparators

=PP12V_S5_PWRCTL → R7013 33.2K, R7018 84.5K, C7010 0.1UF
R7014 100K, R7019 10K
PLACE SHORTS CLOSE TO PLANE CUTS

PP12V_S0 → XW7000 (OMIT SM) → R7000 4.99K → 12VS0_PG_CMP1
(9.91V/9.58V; 330MV HYSTERESIS)
(1.30V/1.22V; 80MV HYSTERESIS)
=PPDDR_S3_PGCMP → XW7001 (OMIT SM) → R7001 1.21K → 1V5S3_PG_CMP

USING COMPARTOR INSTEAD OF REGULATOR
PGOOD OUTPUT BECAUSE IF 5V S3 DOES
NOT COME UP, PPDDR REGULATOR HAS
NO INTERNAL POWER TO PULL PGOOD
LOW

U7010 LM393 SOI-HF (CRITICAL)
12VS5_9V00_REF, 12VS5_COMP_REF, 12VS5_1V27_REF, 1V5S3_COMP_REF
R7007 49.9K, R7008 49.9K
PGOOD_12V_S0, PGOOD_1V5_S3

(PULLUPS ARE NEAR LOADS)

=PP12V_S0_VRD
R7022 MXM 100K, R7020 64.9K
(1.67V/1.53V; 132MV HYSTERESIS)
12VS5_1V60_REF
U7030 LM393 SOI-HF (CRITICAL)
R7006 49.9K, C7025 0.1UF
PGOOD_1V8_S0

=PP1V8_S0_PGCMP → XW7002 (OMIT SM) → R7002 2.0K → 1V8S0_PG_CMP
1V8S0_COMP_REF
R7021 10K

S0 RAILS PGOOD

=PP3V3_S5_PWRCTL → R7033 10K
PGOOD_1V8_S0, PGOOD_1V5_S0, PGOOD_5V_S0
=PP3V3_S0_PWRCTL → R7030 10K
PGOOD_MCPCORE_S0, PGOOD_1V05_S0
S0_PWR_CMP_PGOOD, S0_PWR_REG_PGOOD (MAKE_BASE=TRUE)
U7020 TC7SZ08AFEAPE SOT665 → ALL_SYS_PWRGD
R7098 33 → ALL_SYS_PWRGD_SMC
R7099 33 → ALL_SYS_PWRGD_R
C7020 0.1UF (10% 16V CERM 402)

PLACE RESISTORS CLOSE TO U7020

	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

=PP3V3_S5_PWRCTL → C7056 0.1uF
PM_MXM_PGOOD, PM_PGOOD_PVCORE_CPU → U7056 MC74VHC1G08 SOT23-5-HF → MCP_PS_PWRGD

ALL_SYS_PWRGD IS ALSO AN INPUT TO THIS
AND GATE BY THE EARLY TRAY
PM_MXM_PGOOD IS PULLED UP TO IT

PAGE TITLE
PGOOD and Power Sequencing

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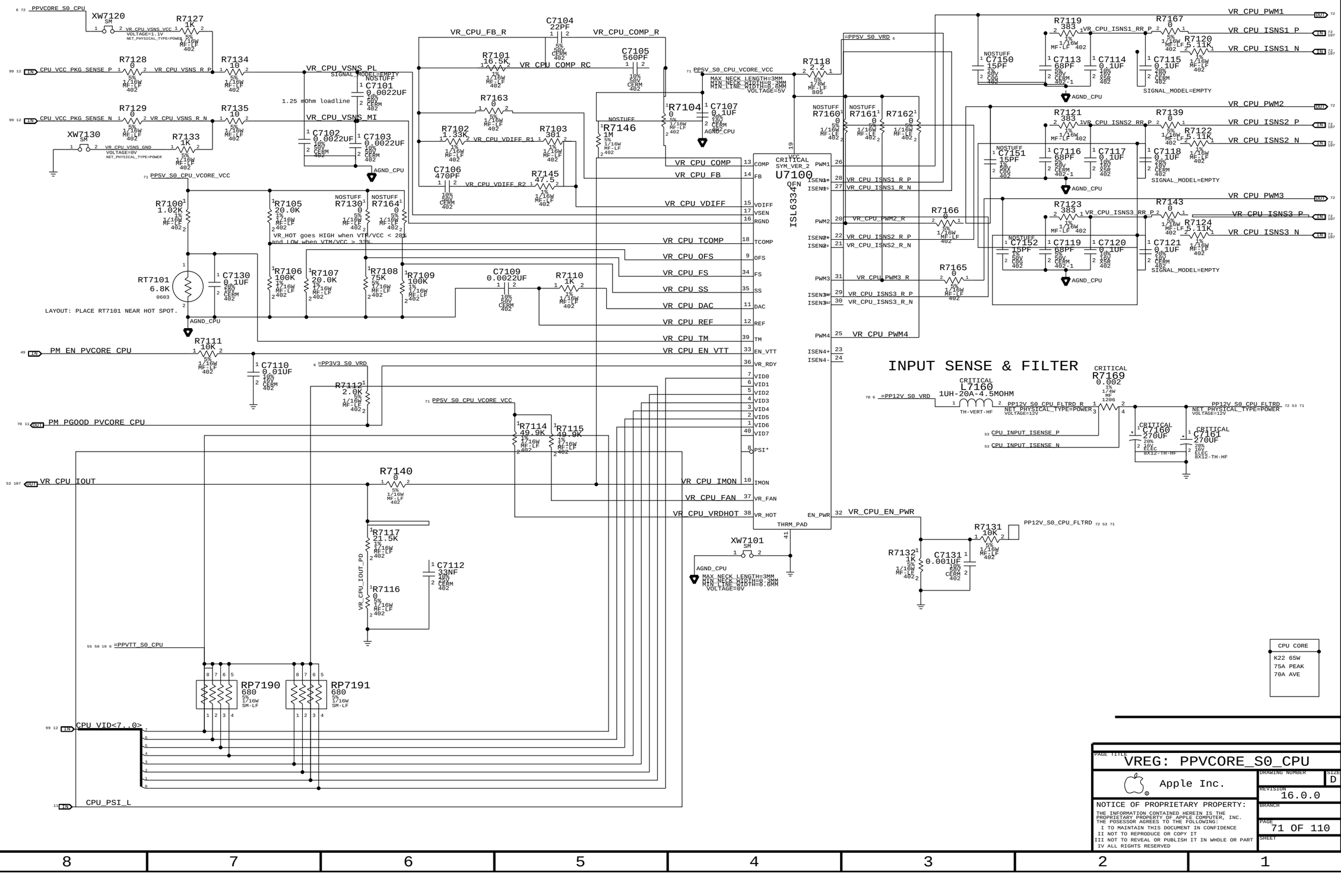
DRAWING NUMBER — SIZE D
REVISION 16.0.0
BRANCH
PAGE 70 OF 110
SHEET



PAGE TITLE: VREG: PPVCORE_S0_CPU

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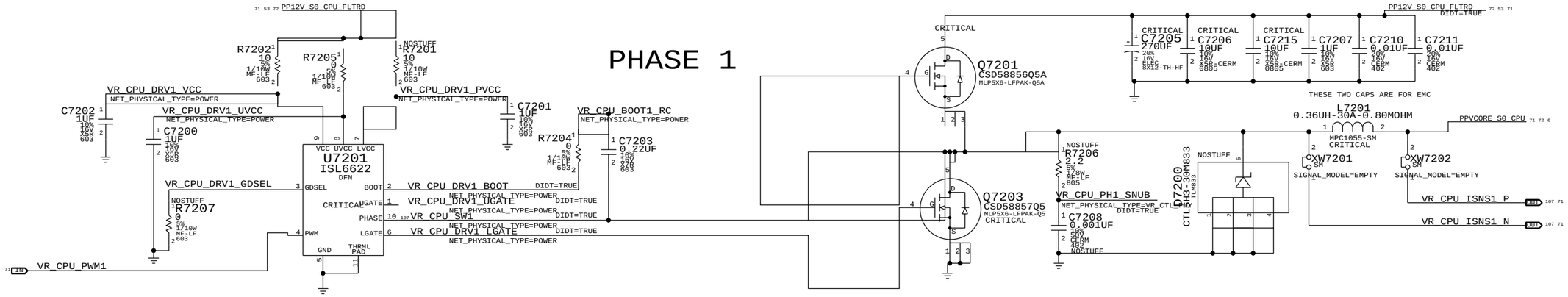
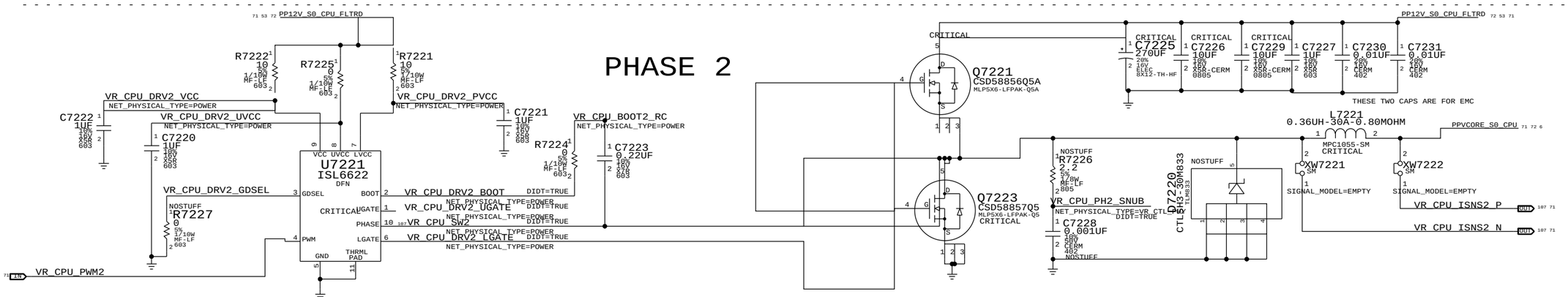
DRAWING NUMBER
SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 71 OF 110
SHEET

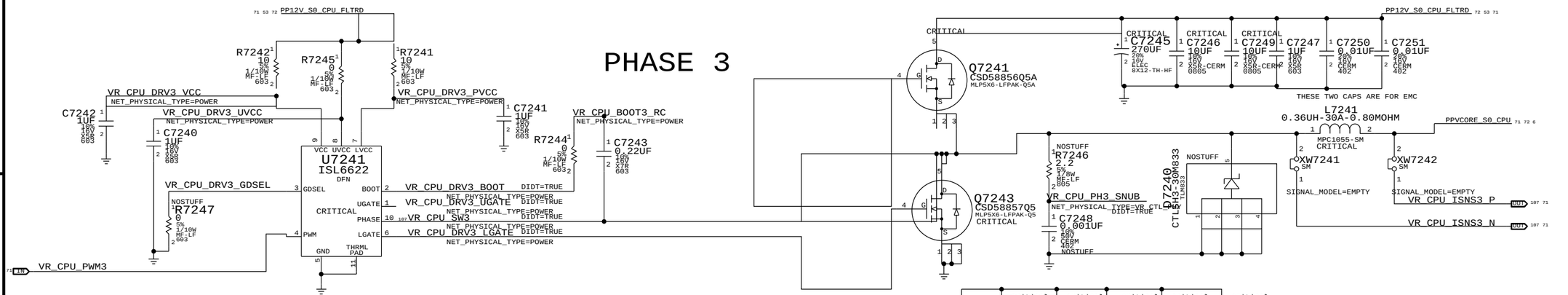
PHASE 1



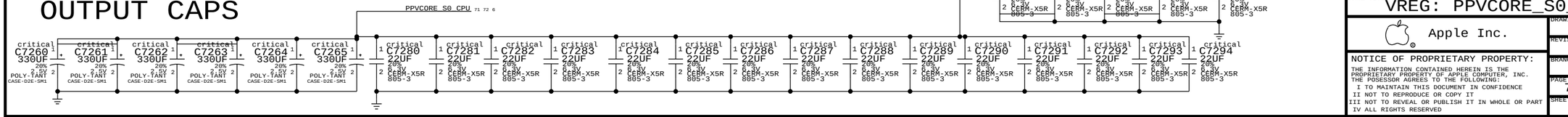
PHASE 2



PHASE 3



OUTPUT CAPS



PAGE TITLE: VREG: PPVCORE_S0_CPU

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DRAWING NUMBER | SIZE D
REVISION: 16.0.0
BRANCH:
PAGE: 72 OF 110
SHEET:

5V S3 REGULATOR

=PPVIN_S5_P5VS3 6 73

C7345 2.2UF 10% 16V X5R 603

C7334 4.7UF 10% 35V X5R-CERM 0805

D7301 B0530WXG SOD-123-HF

CRITICAL
U7300
LTC3851EUD
QFN

INTVCC VIN

OSCILLATED AT APPR. 330KHZ

LTCINTVCC	7	ILIM	
5VS3_FREQ	16	FREQ/PLLFLTR	
5VREG_EN	1	RUN	
5VS3_TK_SS	2	TK/SS	SOFT START TIME 8MS
5VS3_ITH	3	ITH	
LTCMODE	15	MODE/PLLIN	
	17	GND PAD	
	13	TG	
	14	SW	
	12	BOOST	
	9	BG	
	6	SENSE+	
	5	SENSE-	
	4	FB	

R7301 100K 5% 1/10W MF-LF 402

C7331 0.1UF 10% 16V X5R 402

C7316 0.001UF 10% 50V CERM 402

C7303 0.01UF 10% 16V CERM 402

C7306 0.001UF 10% 50V CERM 402

C7307 100PF 5% 50V CERM 402

R7302 24.9K 1% 1/16W MF-LF 402

5VS3_ITH_R

5VS3_TG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE

5VS3_SW
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE

5V_BOOT1
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE

R7324 0 5% 1/10W MF-LF 603

C7326 0.1UF 10% 25V X5R 402

5VS3_BG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
DIDT=TRUE

5VS3_SENSEP

C7315 100PF 5% 50V CERM 402

R7304 0 5% 1/10W MF-LF 402

5VS3_SENSEN

5VS3_FB

C7325 20PF 5% 50V CERM 402

CRITICAL
C7342 270UF 20% 16V ELEC 8X12-TH-HF

C7300 10UF 10% 16V X5R-CERM 0805

C7335 10UF 10% 16V X5R-CERM 0805

C7332 10UF 10% 16V X5R-CERM 0805

EMC: C7353,C7354
PLACE AT Q7330

C7354 0.1UF 10% 25V X5R 402

C7353 0.1UF 10% 25V X5R 402

CRITICAL
Q7330
CSD58856Q5A
MLPS5X6-LFPAK-Q5A

CRITICAL
Q7335
CSD58856Q5A
MLPS5X6-LFPAK-Q5A

SWITCHNODE

PLACE XW CLOSE TO L7320
OMIT
XW7300
5VS3_SENSE

NOSTUFF
C7363 0.0022UF 10% 50V CERM 402

5V_SNUBBER
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.4MM
DIDT=TRUE

R7336 1.5K 1% 1/10W MF-LF 402

R7362 0.499 1% 1/10W MF 603 NOSTUFF

C7317 0.22UF 10% 10V CERM 402

R7307 1.24K 1% 1/10W MF-LF 402

5VS3_SENSEN_R

(5VS3_FB)

CRITICAL
L7320
2.2UH-10A-11.6M-OHM
SM

CRITICAL
D7300
CTLSH3-30M833
TLM833

PLACE XW CLOSE TO L7320
XW7301
SM
OMIT
(5VS3_VOUT)

RA
R7305 43.2K 1% 1/10W MF-LF 402

C7309 100PF 5% 50V CERM 402

RB
R7306 8.06K 1% 1/16W MF-LF 402

EMC: C7304,C7356
PLACE AT L7320.1

C7356 0.1UF 10% 25V X5R 402

C7304 0.1UF 10% 25V X5R 402

5V_S3
K507K51
POWER BUDGET
PEAK=8.86A
AVE=7.3A

PP5V_S3_REG 6 109

C7301 10UF 20% 6.3V CERM 805-1

CRITICAL
C7302 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

CRITICAL
C7305 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7322 10UF 20% 6.3V CERM 805-1

STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE

R7310 10K 5% 1/16W MF-LF 402

PM_SLPS3_BUF1_L

PM_SLPS3_BUF1_R_L

Q7360 MMBT3904G SOT23

5VREG_PS_L

R7311 100K 5% 1/10W MF-LF 402

Q7303 SI2301BDS SM-HF CRITICAL

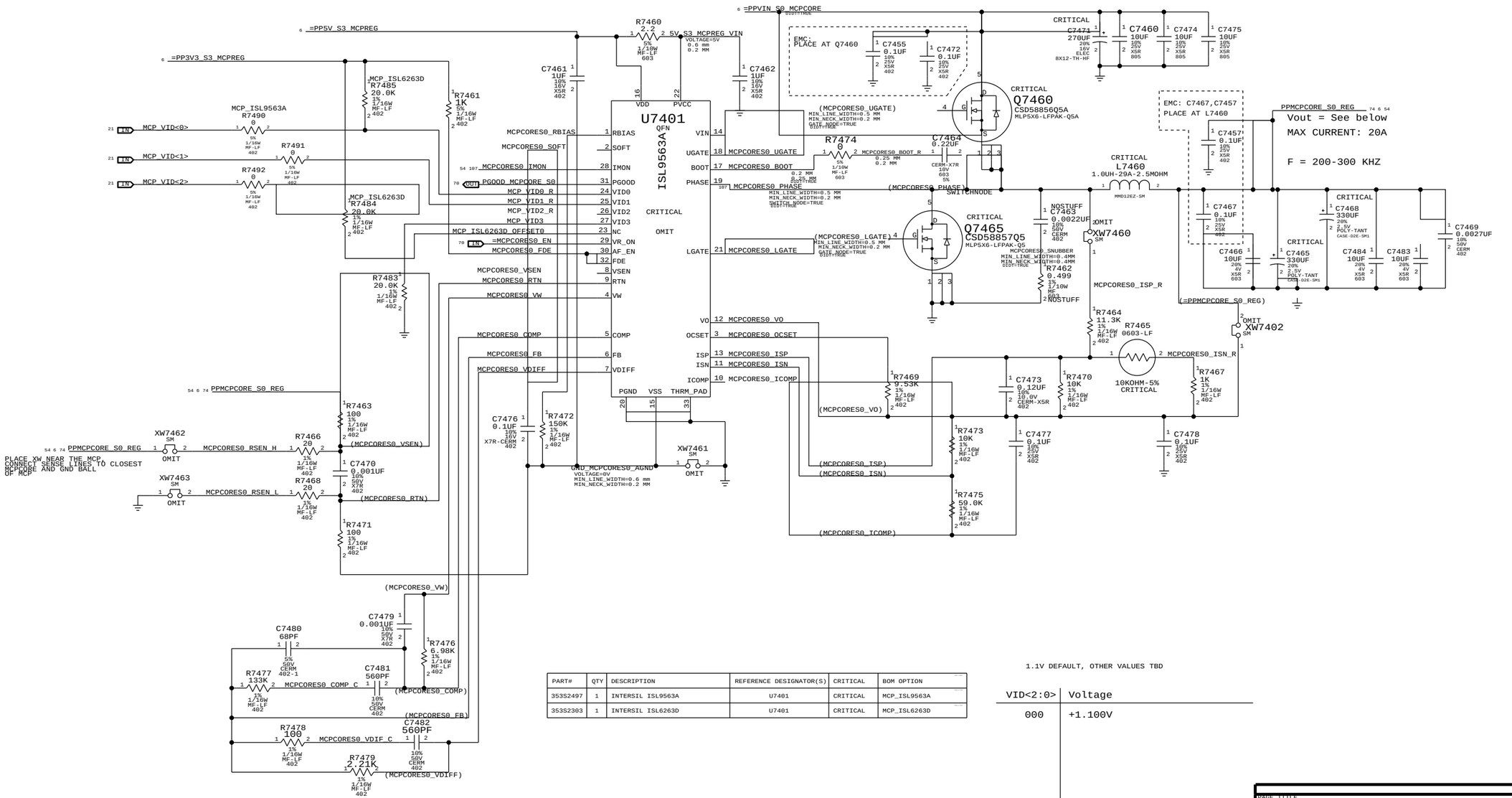
R7312 100K 5% 1/10W MF-LF 402

LTCINTVCC 73

LTCMODE 73

PAGE TITLE	5V_S3 REGULATOR
Apple Inc.	DRAWING NUMBER
SIZE	D
REVISION	16.0.0
BRANCH	
PAGE	73 OF 110
SHEET	

MCP CORE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2497	1	INTERSIL ISL9563A	U7401	CRITICAL	MCP_ISL9563A
353S2303	1	INTERSIL ISL6263D	U7401	CRITICAL	MCP_ISL6263D

1.1V DEFAULT, OTHER VALUES TBD

VID<2:0>	Voltage
000	+1.100V

PAGE TITLE: MCP CORE REGULATOR

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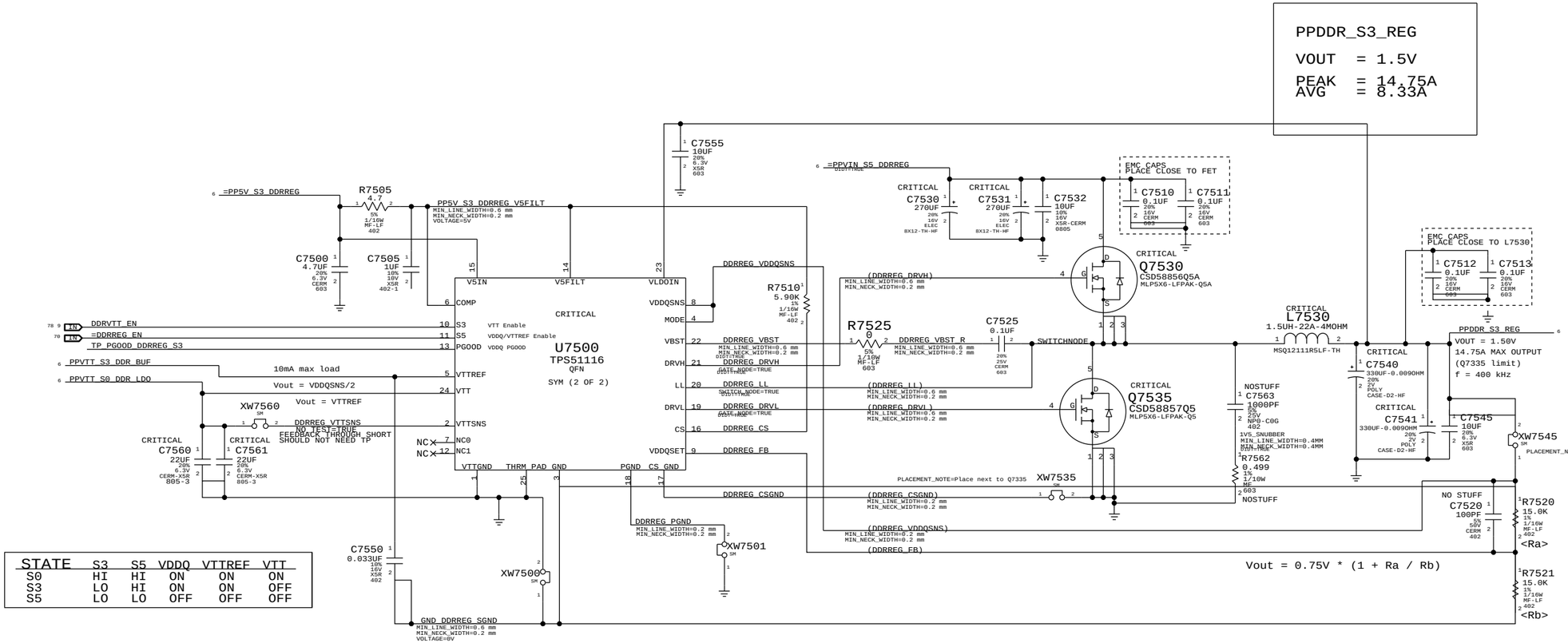
DRAWING NUMBER:
SIZE: D
REVISION: 16.0.0
BRANCH:
PAGE: 74 OF 110
SHEET:

1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 14.75A
AVG = 8.33A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

PAGE TITLE: 1.5V DDR SUPPLY

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DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 75 OF 110

SHEET

FSB VTT AND 3.3V S5 RAILS

INPUT POWER OF 12V_S0

INPUT POWER OF 12V_S5

Vout = 1.212V for Wolfdale
6.7A MAX OUTPUT
(R7614 LIMIT)
f = 200 kHz

Vout = 0.7V * (1 + Ra / Rb)

VTT_FSB_S0
K22/K23
POWER BUDGET
PEAK=5.3A
AVE=2.9A

SEL A3V3 S5
K507/K51
POWER BUDGET
K50 PEAK=4.94A
K50 AVE=2.18A

SELECTS SWITCHING FREQUENCY

EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT. SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

EN1 (PPVTT_S0) CONTROLLED SEPARATELY

PAGE TITLE: FSB VTT/3.3V S5 SUPPLIES

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DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 76 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
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DRAWING NUMBER
SIZE D

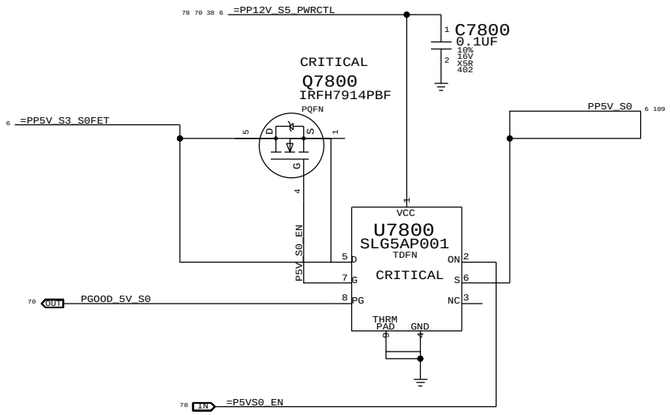
REVISION
16.0.0

BRANCH

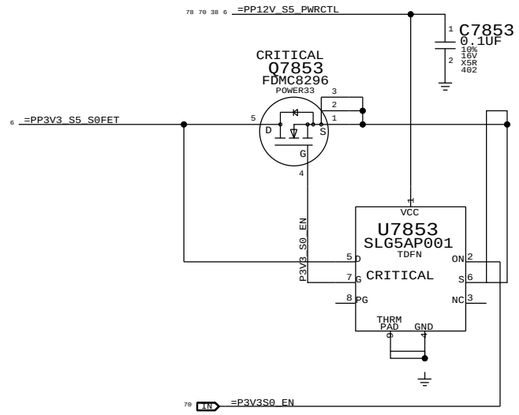
PAGE
77 OF 110

SHEET

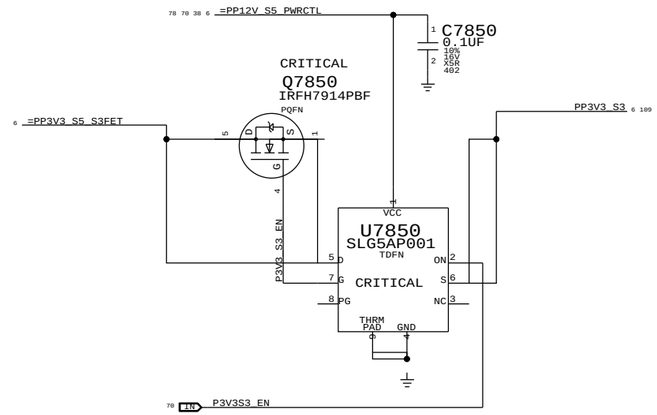
5V S0 FET



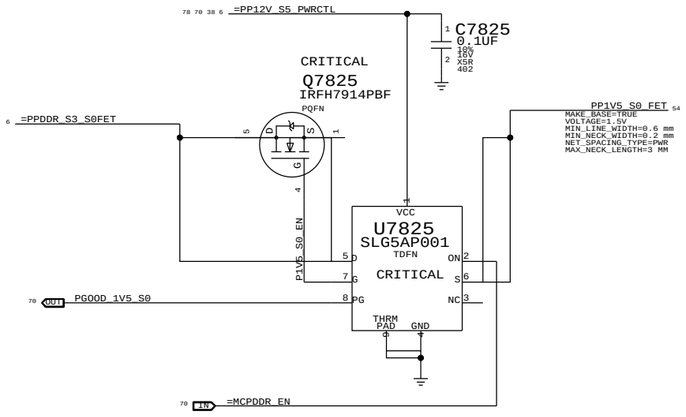
3.3V S0 FET



3.3V S3 FET

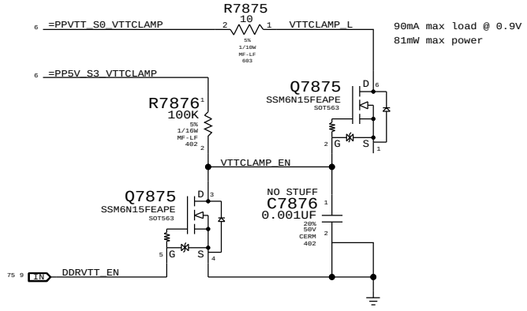


1.5V S0 FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



PAGE TITLE: S3 & S0 FETs

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DRAWING NUMBER | SIZE: D

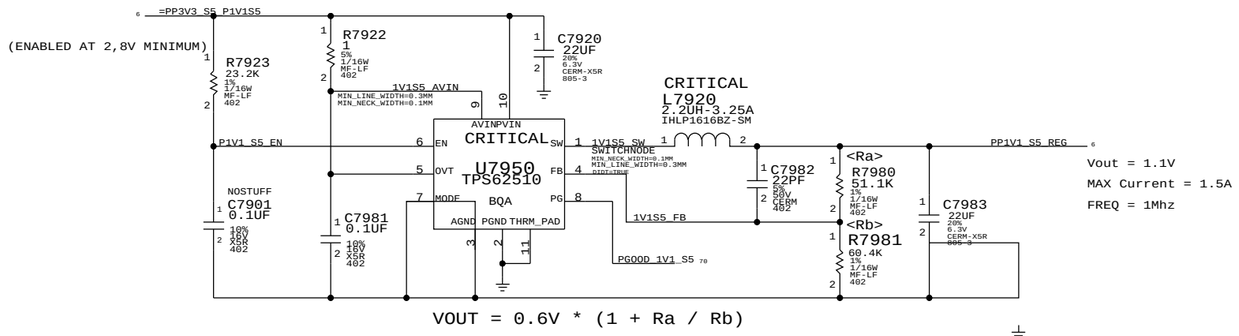
REVISION: 16.0.0

BRANCH

PAGE: 78 OF 110

SHEET

MCP 1.1V_S5 AUXC SUPPLY



PAGE TITLE	1V1 S5 POWER SUPPLY
	Apple Inc.
DRAWING NUMBER	SIZE D
REVISION	16.0.0
BRANCH	
PAGE	79 OF 110
SHEET	

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
80 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
81 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
82 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
83 OF 110

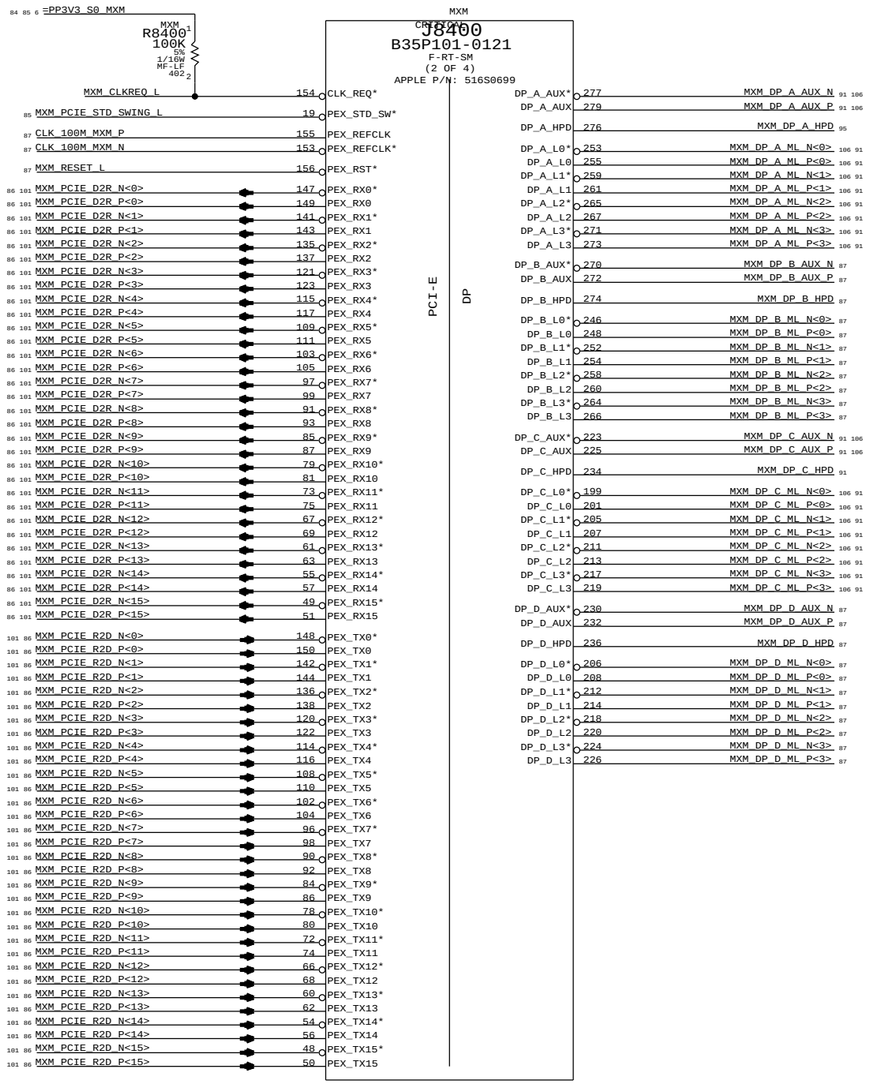
SHEET

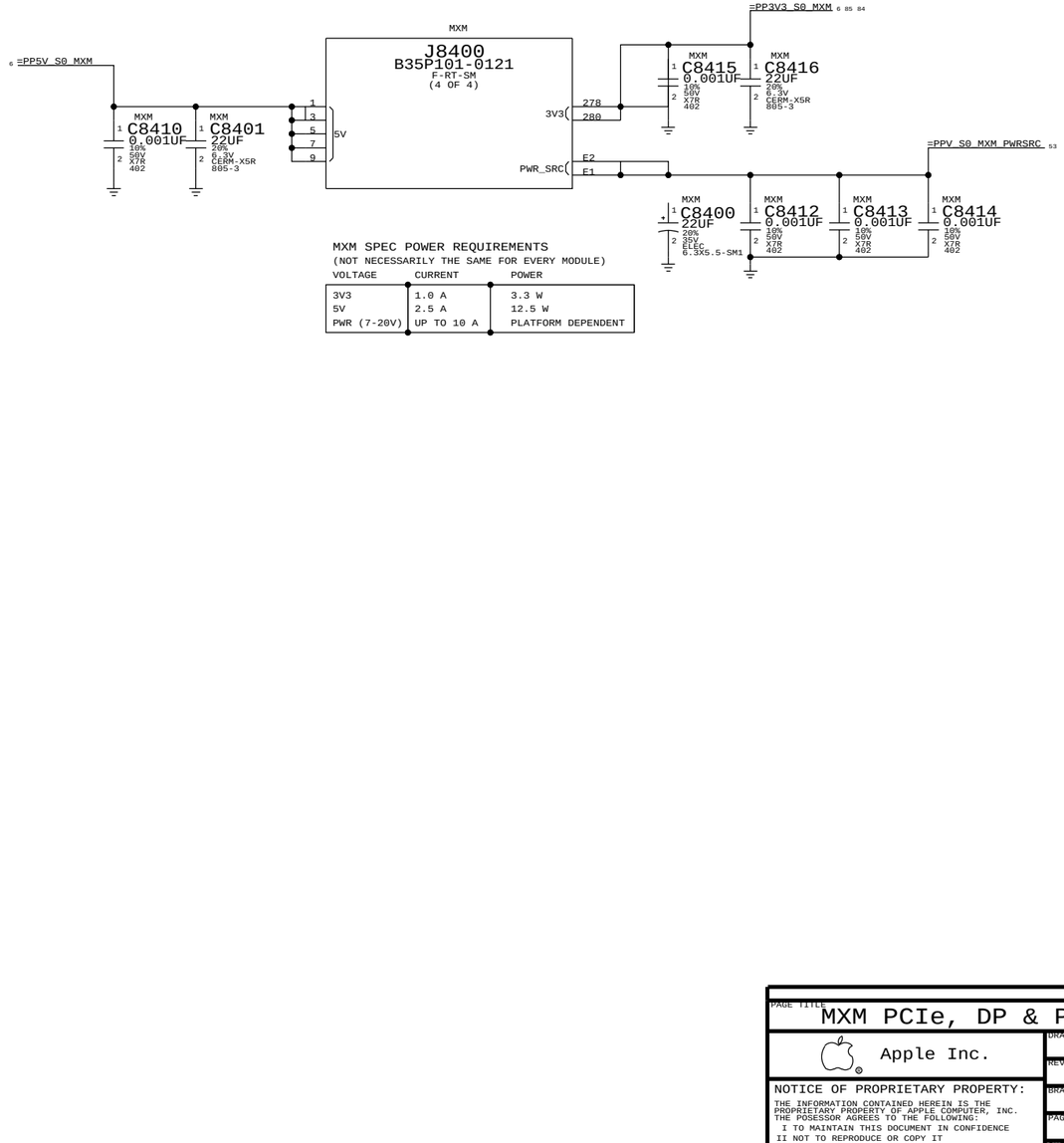
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM





MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

PAGE TITLE: MXM PCIe, DP & Power

Apple Inc.

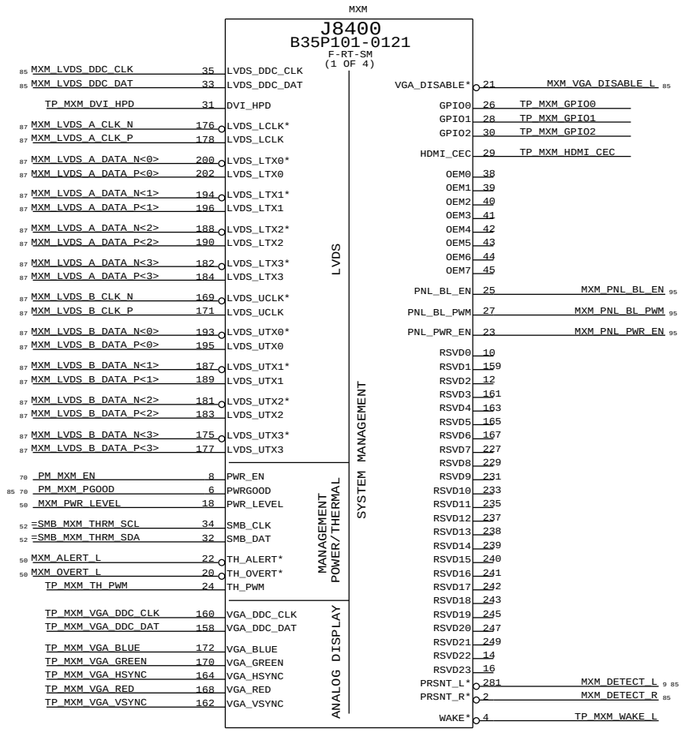
DRAWING NUMBER
SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 84 OF 110
SHEET

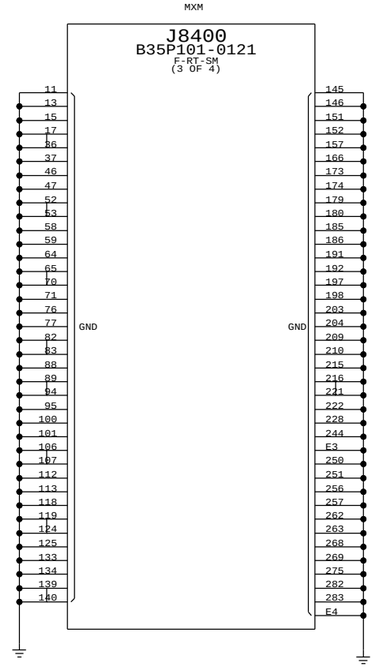
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA
- =SMB_MXM_THRM_CLK
- =PM_MXM_PGOOD_PULLUP

BOM options provided by this page:





PULLUPS & PULLDOWNS AT MXM CONNECTOR

FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

R8510 0 NOSTUFF
MXM_VGA_DISABLE_L
MF-LF 5% 1/16W 402

FLOAT = LOW SWING
GND = HIGH SWING

R8504 0 NOSTUFF
MXM_PCIE_STD_SWING_L
MF-LF 5% 1/16W 402

=PP3V3_S0_MXM

R8500 100K
MXM_DETECT_L
MF-LF 5% 1/16W 402

PULLED TO GROUND ON MXM
WE DON'T USE CARD DETECT

R8501 100K
MXM_DETECT_R
MF-LF 5% 1/16W 402

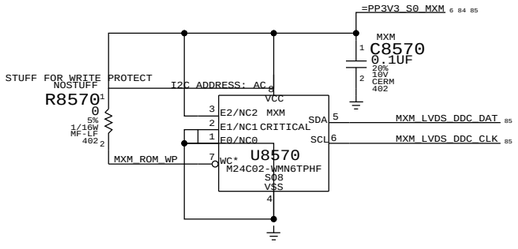
=PM_MXM_PGOOD_PULLUP

SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

R8503 10K
PM_MXM_PGOOD
MF-LF 5% 1/16W 402

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



PAGE TITLE	MXM I/O
Apple Inc.	DRAWING NUMBER
	SIZE D
	REVISION 16.0.0
	BRANCH
	PAGE 85 OF 110
	SHEET

MXM TX CAPS

101 9	IN	PEG_R2D_C_N<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT 101 84
101 9	IN	PEG_R2D_C_P<0>	MXM	C8601	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT 101 84
101 9	IN	PEG_R2D_C_P<1>	MXM	C8602	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	OUT 101 84
101 9	IN	PEG_R2D_C_N<1>	MXM	C8603	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	OUT 101 84
101 9	IN	PEG_R2D_C_N<2>	MXM	C8604	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>	OUT 101 84
101 9	IN	PEG_R2D_C_P<2>	MXM	C8605	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>	OUT 101 84
101 9	IN	PEG_R2D_C_N<3>	MXM	C8606	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	OUT 101 84
101 9	IN	PEG_R2D_C_P<3>	MXM	C8607	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	OUT 101 84
101 9	IN	PEG_R2D_C_N<4>	MXM	C8608	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	OUT 101 84
101 9	IN	PEG_R2D_C_P<4>	MXM	C8609	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	OUT 101 84
101 9	IN	PEG_R2D_C_N<5>	MXM	C8610	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	OUT 101 84
101 9	IN	PEG_R2D_C_P<5>	MXM	C8611	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	OUT 101 84
101 9	IN	PEG_R2D_C_N<6>	MXM	C8612	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>	OUT 101 84
101 9	IN	PEG_R2D_C_P<6>	MXM	C8613	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>	OUT 101 84
101 9	IN	PEG_R2D_C_N<7>	MXM	C8614	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	OUT 101 84
101 9	IN	PEG_R2D_C_P<7>	MXM	C8615	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>	OUT 101 84
101 9	IN	PEG_R2D_C_N<8>	MXM	C8616	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>	OUT 101 84
101 9	IN	PEG_R2D_C_P<8>	MXM	C8617	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>	OUT 101 84
101 9	IN	PEG_R2D_C_N<9>	MXM	C8618	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>	OUT 101 84
101 9	IN	PEG_R2D_C_P<9>	MXM	C8619	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>	OUT 101 84
101 9	IN	PEG_R2D_C_N<10>	MXM	C8620	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>	OUT 101 84
101 9	IN	PEG_R2D_C_P<10>	MXM	C8621	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>	OUT 101 84
101 9	IN	PEG_R2D_C_P<11>	MXM	C8622	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>	OUT 101 84
101 9	IN	PEG_R2D_C_N<11>	MXM	C8623	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>	OUT 101 84
101 9	IN	PEG_R2D_C_N<12>	MXM	C8624	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>	OUT 101 84
101 9	IN	PEG_R2D_C_P<12>	MXM	C8625	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>	OUT 101 84
101 9	IN	PEG_R2D_C_N<13>	MXM	C8626	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>	OUT 101 84
101 9	IN	PEG_R2D_C_P<13>	MXM	C8627	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>	OUT 101 84
101 9	IN	PEG_R2D_C_N<14>	MXM	C8628	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>	OUT 101 84
101 9	IN	PEG_R2D_C_P<14>	MXM	C8629	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>	OUT 101 84
101 9	IN	PEG_R2D_C_N<15>	MXM	C8630	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>	OUT 101 84
101 9	IN	PEG_R2D_C_P<15>	MXM	C8631	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	OUT 101 84

MXM RX CAPS

101 84	IN	MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<0>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<2>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<3>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<3>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<4>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<11>	MXM	C8641	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<4>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<10>	MXM	C8642	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<5>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<10>	MXM	C8643	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<5>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<9>	MXM	C8644	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<6>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<9>	MXM	C8645	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<6>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<7>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<8>	MXM	C8647	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<7>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<8>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<9>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<9>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<5>	MXM	C8652	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<10>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<10>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<13>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<13>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT 101 9
101 84	IN	MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT 101 9

PAGE TITLE

MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION 16.0.0

BRANCH

PAGE 86 OF 110

SHEET

Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MCP Connections

84 CLK_100M_MXM_P ═ GPU_CLK100M_PCIE_P 9 101
MAKE_BASE=TRUE
84 CLK_100M_MXM_N ═ GPU_CLK100M_PCIE_N 9 101
MAKE_BASE=TRUE
84 MXM_RESET_L ═ PEG_RESET_L 9
MAKE_BASE=TRUE

Unused LVDS Interfaces

18 LVDS_IG_A_CLK_P ═ NC_LVDS_IG_A_CLK_P
18 LVDS_IG_A_CLK_N ═ NC_LVDS_IG_A_CLK_N
18 LVDS_IG_A_DATA_P<0> ═ NC_LVDS_IG_A_DATA_P<0>
18 LVDS_IG_A_DATA_N<0> ═ NC_LVDS_IG_A_DATA_N<0>
18 LVDS_IG_A_DATA_P<1> ═ NC_LVDS_IG_A_DATA_P<1>
18 LVDS_IG_A_DATA_N<1> ═ NC_LVDS_IG_A_DATA_N<1>
18 LVDS_IG_A_DATA_P<2> ═ NC_LVDS_IG_A_DATA_P<2>
18 LVDS_IG_A_DATA_N<2> ═ NC_LVDS_IG_A_DATA_N<2>
18 LVDS_IG_A_DATA_P<3> ═ NC_LVDS_IG_A_DATA_P<3>
18 LVDS_IG_A_DATA_N<3> ═ NC_LVDS_IG_A_DATA_N<3>
18 LVDS_IG_B_CLK_P ═ NC_LVDS_IG_B_CLK_P
18 LVDS_IG_B_CLK_N ═ NC_LVDS_IG_B_CLK_N
18 LVDS_IG_B_DATA_P<0> ═ NC_LVDS_IG_B_DATA_P<0>
18 LVDS_IG_B_DATA_N<0> ═ NC_LVDS_IG_B_DATA_N<0>
18 LVDS_IG_B_DATA_P<1> ═ NC_LVDS_IG_B_DATA_P<1>
18 LVDS_IG_B_DATA_N<1> ═ NC_LVDS_IG_B_DATA_N<1>
18 LVDS_IG_B_DATA_P<2> ═ NC_LVDS_IG_B_DATA_P<2>
18 LVDS_IG_B_DATA_N<2> ═ NC_LVDS_IG_B_DATA_N<2>
18 LVDS_IG_B_DATA_P<3> ═ NC_LVDS_IG_B_DATA_P<3>
18 LVDS_IG_B_DATA_N<3> ═ NC_LVDS_IG_B_DATA_N<3>
18 LVDS_IG_DDC_CLK ═ NC_LVDS_IG_DDC_CLK
18 LVDS_IG_DDC_DATA ═ NC_LVDS_IG_DDC_DATA

MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM Interfaces

85 MXM_LVDS_A_CLK_N ═ NC_MXM_LVDS_A_CLK_N
85 MXM_LVDS_A_CLK_P ═ NC_MXM_LVDS_A_CLK_P
85 MXM_LVDS_A_DATA_N<0> ═ NC_MXM_LVDS_A_DATA_N<0>
85 MXM_LVDS_A_DATA_P<0> ═ NC_MXM_LVDS_A_DATA_P<0>
85 MXM_LVDS_A_DATA_N<1> ═ NC_MXM_LVDS_A_DATA_N<1>
85 MXM_LVDS_A_DATA_P<1> ═ NC_MXM_LVDS_A_DATA_P<1>
85 MXM_LVDS_A_DATA_N<2> ═ NC_MXM_LVDS_A_DATA_N<2>
85 MXM_LVDS_A_DATA_P<2> ═ NC_MXM_LVDS_A_DATA_P<2>
85 MXM_LVDS_A_DATA_N<3> ═ NC_MXM_LVDS_A_DATA_N<3>
85 MXM_LVDS_A_DATA_P<3> ═ NC_MXM_LVDS_A_DATA_P<3>
85 MXM_LVDS_B_CLK_N ═ NC_MXM_LVDS_B_CLK_N
85 MXM_LVDS_B_CLK_P ═ NC_MXM_LVDS_B_CLK_P
85 MXM_LVDS_B_DATA_N<0> ═ NC_MXM_LVDS_B_DATA_N<0>
85 MXM_LVDS_B_DATA_P<0> ═ NC_MXM_LVDS_B_DATA_P<0>
85 MXM_LVDS_B_DATA_N<1> ═ NC_MXM_LVDS_B_DATA_N<1>
85 MXM_LVDS_B_DATA_P<1> ═ NC_MXM_LVDS_B_DATA_P<1>
85 MXM_LVDS_B_DATA_N<2> ═ NC_MXM_LVDS_B_DATA_N<2>
85 MXM_LVDS_B_DATA_P<2> ═ NC_MXM_LVDS_B_DATA_P<2>
85 MXM_LVDS_B_DATA_N<3> ═ NC_MXM_LVDS_B_DATA_N<3>
85 MXM_LVDS_B_DATA_P<3> ═ NC_MXM_LVDS_B_DATA_P<3>

MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

84 MXM_DP_B_ML_P<0..3> ═ NC_MXM_DP_B_ML_P<0..3>
84 MXM_DP_B_ML_N<0..3> ═ NC_MXM_DP_B_ML_N<0..3>
84 MXM_DP_B_AUX_P ═ NC_MXM_DP_B_AUX_P
84 MXM_DP_B_AUX_N ═ NC_MXM_DP_B_AUX_N
84 MXM_DP_B_HPD ═ NC_MXM_DP_B_HPD
84 MXM_DP_D_ML_P<0..3> ═ NC_MXM_DP_D_ML_P<0..3>
84 MXM_DP_D_ML_N<0..3> ═ NC_MXM_DP_D_ML_N<0..3>
84 MXM_DP_D_AUX_P ═ NC_MXM_DP_D_AUX_P
84 MXM_DP_D_AUX_N ═ NC_MXM_DP_D_AUX_N
84 MXM_DP_D_HPD ═ NC_MXM_DP_D_HPD

MAKE_BASE=TRUE NO_TEST=TRUE

Unused MCP Interfaces

18 LVDS_IG_BKL_ON ═ NC_LVDS_IG_BKL_ON
18 LVDS_IG_BKL_PWM ═ NC_LVDS_IG_BKL_PWM
18 LVDS_IG_PANEL_PWR ═ NC_LVDS_IG_PANEL_PWR
18 =MCP_HDMI_TXD_P<0..2> ═ NC_MCP_HDMI_TXD_P<0..2>
18 =MCP_HDMI_TXD_N<0..2> ═ NC_MCP_HDMI_TXD_N<0..2>
18 =MCP_HDMI_TXC_P ═ NC_MCP_HDMI_TXC_P
18 =MCP_HDMI_TXC_N ═ NC_MCP_HDMI_TXC_N

MAKE_BASE=TRUE NO_TEST=TRUE

91 90 95 6 =PP3V3_S0_DP

1 R8700 2.7K 5% 1/16W MF-LF 2 402
1 R8701 2.7K 5% 1/16W MF-LF 2 402

MAKE_BASE=TRUE

18 =MCP_HDMI_DDC_CLK ═ DP_IG_DDC_CLK
18 =MCP_HDMI_DDC_DATA ═ DP_IG_DDC_DATA
18 =MCP_HDMI_HPD ═ DP_IG_HPD

MAKE_BASE=TRUE

1 R8710 22K 5% 1/16W MF-LF 2 402

18 DP_IG_AUX_CH_P ═ NC_DP_IG_AUX_CH_P
18 DP_IG_AUX_CH_N ═ NC_DP_IG_AUX_CH_N

MAKE_BASE=TRUE NO_TEST=TRUE

18 DP_IG_CA_DET

1 R8711 1M 5% 1/16W MF-LF 2 402

PAGE TITLE: Display: Aliases
Apple Inc.
DRAWING NUMBER
SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 87 OF 110
SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
88 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
89 OF 110

SHEET

Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

CRITICAL
J9002
20389-Y30E-01
F-RT-SM

NOSTUFF R9050 0 5% 1/16W MF-LF 402
NOSTUFF R9051 0 5% 1/16W MF-LF 402

52 =SMB_DP_TCON_SCL
52 =SMB_DP_TCON_SDA
I2C MASTER ON TCON
I2C_TCON_SCL
I2C_TCON_SDA
106 91 DP_INT_AUXCH_N
106 91 DP_INT_AUXCH_P

106 91 IN DP_INT_LINK_P<0> — C9040 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_P<0>
106 91 IN DP_INT_LINK_N<0> — C9041 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_N<0>
106 91 IN DP_INT_LINK_P<1> — C9042 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_P<1>
106 91 IN DP_INT_LINK_N<1> — C9043 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_N<1>
106 91 IN DP_INT_LINK_P<2> — C9044 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_P<2>
106 91 IN DP_INT_LINK_N<2> — C9045 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_N<2>
106 91 IN DP_INT_LINK_P<3> — C9046 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_P<3>
106 91 IN DP_INT_LINK_N<3> — C9047 0.1uF 10% 16V XSR 402 — 106 DP_INT_LINK_CONN_N<3>

95 SPDIF_DP_AUDIO_OUT
95 90 VIDEO_ON
91 DP_HPD_INT

PANEL POWER CONTROL

6 =PP12V_S0_LCD
MLB_PNL_PWR R9000 100K 5% 1/16W MF-LF 402
LCD_PANEL_PWR_L_DIV
MLB_PNL_PWR R9002 100K 5% 1/16W MF-LF 402
MLB_PNL_PWR R9001 29.4K 1% 1/16W MF-LF 402
MLB_PNL_PWR C9000 0.1UF 10% 50V X7R 603-1
LCD_PANEL_PWR_L_RC
LCD_PANEL_PWR_L
LCD_PNL_PWR R9010 0 5% 1/10W MF-LF 603
MLB_PNL_PWR CRITICAL Q9000 FDC638P_G SM
PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
L9000 FERR-250-OHM SM
C9020 10UF 10% 16V X5R-CERM 0805
C9001 0.001uF 20% 50V CERM 402
PP12V_LCD_CONN
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
6 =PP3V3_S0_VIDEO
C9010 0.001uF 20% 50V CERM 402

PLACE NEAR J9002

NOSTUFF R9071 0 5% 1/10W MF-LF 603
95 LCD_PANEL_PWR
LCD_PANEL_PWR_G
MLB_PNL_PWR
Q9001 2N7002 SOT23-HF1
R9072 0 5% 1/10W MF-LF 603
95 90 VIDEO_ON
MLB_PNL_PWR R9070 100K 5% 1/16W MF-LF 402

91 90 87 95 6 =PP3V3_S0_DP
MLB_PNL_PWR C9011 0.1UF 20% 10V CERM 402

MLB_PNL_PWR U9050 TC7SZ08AFEAPE SOT665
95 90 VIDEO_ON
95 LCD_BKL_ON_MUX
NOSTUFF R9012 1K 5% 1/16W MF-LF 402
LCD_BKL_MLB_EN

95 BACKLIGHT_PWM
R9081 47 5% 1/16W MF-LF 402
LCD_PWM_FILT
CRITICAL L9050 FERR-250-OHM SM
LCD_PWM 6

BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video
Options for GPU or MLB HW controlled backlight enable are included

91 90 87 95 6 =PP3V3_S0_DP
C9005 22UF 20% 6.3V CERM 805

6 OUT VIDEO_ON_L
used by diag LED

91 90 87 95 6 =PP3V3_S0_DP
U9500 74LVC14 TSSOP-HF
95 90 VIDEO_ON

D9000 SOT23 BAT54XG
R9009 19.1K 1% 1/10W MF-LF 402
VIDEO_ON_L_DLY

U9520 74AUP2G14GM SOT886
LCD_BKL_ON_DLY
LCD_PNL_PWR R9011 1K 5% 1/16W MF-LF 402
LCD_BKL_ON OUT 6

buffers are multiple parts, other parts are on csa 95

PAGE TITLE
Display: Int DP Connector

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 90 OF 110
SHEET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0752	1	IC,PS8325,DP MUX,EQ	U9100	CRITICAL	

DisplayPort Equalizer & MUX 2

Note: INT_PD = Internal Pulldown on this pin of >=100 kOhms

U9100 PS8325 QFN — OMIT — CRITICAL

=PP3V3_S0_DP

C9120 0.1UF 20% 10V CERM 402
C9121 0.1UF 20% 10V CERM 402
C9124 0.1UF 20% 10V CERM 402
C9125 0.1UF 20% 10V CERM 402
C9126 0.1UF 20% 10V CERM 402

VDD: 4, 22, 38, 47, 62

From iMac GPU

MXM_DP_C_ML_P<0>	C9140 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_P<0> NO_TEST	IN1_D0P
MXM_DP_C_ML_N<0>	C9141 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_N<0> NO_TEST	IN1_D0N
MXM_DP_C_ML_P<1>	C9142 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_P<1> NO_TEST	IN1_D1P
MXM_DP_C_ML_N<1>	C9143 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_N<1> NO_TEST	IN1_D1N
MXM_DP_C_ML_P<2>	C9144 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_P<2> NO_TEST	IN1_D2P
MXM_DP_C_ML_N<2>	C9145 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_N<2> NO_TEST	IN1_D2N
MXM_DP_C_ML_P<3>	C9146 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_P<3> NO_TEST	IN1_D3P
MXM_DP_C_ML_N<3>	C9147 0.1UF 10% 16V X5R 402	MXM_DP_C_ML_C_N<3> NO_TEST	IN1_D3N

=I2C_DP_EQLZ_DATA → IN1_PEQ/SDA_CTL (68)

From external input via MUX 1

DP_MUX_P<0>	IN2_D0P (14)
DP_MUX_N<0>	IN2_D0N (15)
DP_MUX_P<1>	IN2_D1P (17)
DP_MUX_N<1>	IN2_D1N (18)
DP_MUX_P<2>	IN2_D2P (20)
DP_MUX_N<2>	IN2_D2N (21)
DP_MUX_P<3>	IN2_D3P (23)
DP_MUX_N<3>	IN2_D3N (24)

=I2C_DP_EQLZ_CLOCK → IN2_PEQ/SCL_CTL (67)

=PP3V3_S0_DP

R9121 1K 5% 1/16W MF-LF 402 → DP_EQLZ_MODE0 → MODE0 (64)
R9115 1K 5% 1/16W MF-LF 402 → DP_EQLZ_MODE1 → MODE1 (65)
R9120 1K 5% 1/16W MF-LF 402 → DP_EQLZ_MODE2 → MODE2 (69)

MODE[2..0] = 111 SELECTS I2C CONTROL MODE

R9122 4.99K 1% 1/16W MF-LF 402 → REXT (70)

C9112 4.7UF 20% 6.3V X5R-CERM 402

CEXT (1) — DP_EQLZ_EXTC — see below

=PP3V3_S0_DP

R9180 0 NOSTUFF 5% 1/16W MF-LF 402 → DP_EQLZ_ADDR → SW/I2C_ADDR (66) — INT_PD

TMDS_SCL (34) NC
TMDS_SDA (35) NC

DP_AC_AUXP (30) — DP_EQLZ_AUXCH_P — B1
DP_AC_AUXN (31) — DP_EQLZ_AUXCH_N — B1

From iMac GPU

MXM_DP_C_AUX_P	C9148 0.1UF 10% 16V X5R 402	MXM_DP_C_AUX_C_P	IN1_AUXP_SCL (28)
MXM_DP_C_AUX_N	C9149 0.1UF 10% 16V X5R 402	MXM_DP_C_AUX_C_N	IN1_AUXN_SDA (29)

From external input via MUX 1

DP_MUX_AUXCH_P	IN2_AUXP_SCL (25)
DP_MUX_AUXCH_N	IN2_AUXN_SDA (26)

R9181 1M 5% 1/16W MF-LF 402 → DP_EQLZ_CADET → DP_CADET (56)

INT_PDIN1_CADET (7) NC
INT_PDIN2_CADET (16) NC

From Internal display — DP_HPD_INT → DP_HPD (53) — INT_PD

TMDS_HPD (41) NC — INT_PD

IN1_HPDX (10) — MXM_DP_C_HPD — TO IMAC GPU
IN2_HPDX (19) — DP_MUX_HPD — TO EXTERNAL SOURCE VIA MUX1

TMDS_PC0 (37) NC
TMDS_PC1 (44) NC
PIOINT_PD (71) NC
PDINT_PD (59) NC

GND: 13, 27, 36, 60, 63, 72 — THRM_PAD (73)

DP_D0P (61)	DP_INT_LINK_P<0>
DP_D0N (60)	DP_INT_LINK_N<0>
DP_D1P (58)	DP_INT_LINK_P<1>
DP_D1N (57)	DP_INT_LINK_N<1>
DP_D2P (55)	DP_INT_LINK_P<2>
DP_D2N (54)	DP_INT_LINK_N<2>
DP_D3P (52)	DP_INT_LINK_P<3>
DP_D3N (51)	DP_INT_LINK_N<3>

(NO_TEST) → To Internal display

TMDS_CH0P (43) NC
TMDS_CH0N (42) NC
TMDS_CH1P (46) NC
TMDS_CH1N (45) NC
TMDS_CH2P (48) NC
TMDS_CH2N (47) NC
TMDS_CLKN (39) NC
TMDS_CLKP (40) NC

DP_AC_AUXP (30) — DP_INT_AUXCH_P — B1
DP_AC_AUXN (31) — DP_INT_AUXCH_N — B1

To Internal display

Pulls for AUX_CH from DisplayPort Mux #2

=PP3V3_S0_DP

R9112 100K 1% 1/16W MF-LF 402 → MXM_DP_C_AUX_C_N
R9113 100K 1% 1/16W MF-LF 402 → MXM_DP_C_AUX_C_P

DisplayPort Mux 1 - at External Connector

From iMac GPU

MXM_DP_A_ML_P<0>	C9130 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_P<0> NO_TEST	DIN1_0+ (B4)
MXM_DP_A_ML_N<0>	C9131 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_N<0> NO_TEST	DIN1_0- (A4)
MXM_DP_A_ML_P<1>	C9132 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_P<1> NO_TEST	DIN1_1+ (B5)
MXM_DP_A_ML_N<1>	C9133 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_N<1> NO_TEST	DIN1_1- (A5)
MXM_DP_A_ML_P<2>	C9134 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_P<2> NO_TEST	DIN1_2+ (B6)
MXM_DP_A_ML_N<2>	C9135 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_N<2> NO_TEST	DIN1_2- (A6)
MXM_DP_A_ML_P<3>	C9136 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_P<3> NO_TEST	DIN1_3+ (A8)
MXM_DP_A_ML_N<3>	C9137 0.1UF 10% 16V X5R 402	MXM_DP_A_ML_C_N<3> NO_TEST	DIN1_3- (A9)
MXM_DP_A_AUX_P	C9138 0.1UF 10% 16V X5R 402	MXM_DP_A_AUX_C_P	DAUX1+ (H9)
MXM_DP_A_AUX_N	C9139 0.1UF 10% 16V X5R 402	MXM_DP_A_AUX_C_N	DAUX1- (J9)

=PP3V3_S0_DP → A2, J4 (VDD)

C9322 0.1UF 20% 10V CERM 402
C9323 0.1UF 20% 10V CERM 402

U9120 CBTL06141EE BGA — CRITICAL

DDC_CLK1 (H8)
DDC_DAT1 (J8)
HPD_1 (J2) ← MXM_DP_A_HPD_MUX (95)

From external source to internal display via EQ

DP_MUX_N<3>	NO_TEST	DIN2_0+ (B8)
DP_MUX_P<3>	NO_TEST	DIN2_0- (B9)
DP_MUX_N<2>	NO_TEST	DIN2_1+ (D8)
DP_MUX_P<2>	NO_TEST	DIN2_1- (D9)
DP_MUX_N<1>	NO_TEST	DIN2_2+ (E8)
DP_MUX_P<1>	NO_TEST	DIN2_2- (E9)
DP_MUX_N<0>	NO_TEST	DIN2_3+ (F8)
DP_MUX_P<0>	NO_TEST	DIN2_3- (F9)
DP_MUX_AUXCH_P		DAUX2+ (H6)
DP_MUX_AUXCH_N		DAUX2- (J6)

DDC_CLK2 (H5) NC
DDC_DAT2 (J5) NC

=PP3V3_S0_DP

R9130 10K 5% 1/16W MF-LF 402 NOSTUFF

DP_MUX_HPD → HPD_2 (H3)
DPMUX_VIDEO_IN_SEL → GPU_SEL (A1) — LO=PORT1 HI=PORT2
DPMUX1_ENABLE → XSD* (B7)

DDC_AUX_SEL (C2) — LO=AUX_CH HI=DDC
DP_CA_DET (C2)
TST0 (G2)

GND: B3, C5, G5, H4, H7

DOUT_0+ (B2) — NO_TEST — DP_EXT_LINK_P<0> — B1 (106 94)
DOUT_0- (B1) — NO_TEST — DP_EXT_LINK_N<0> — B1 (106 94)
DOUT_1+ (D2) — NO_TEST — DP_EXT_LINK_P<1> — B1 (106 94)
DOUT_1- (D1) — NO_TEST — DP_EXT_LINK_N<1> — B1 (106 94)
DOUT_2+ (E2) — NO_TEST — DP_EXT_LINK_P<2> — B1 (106 94)
DOUT_2- (E1) — NO_TEST — DP_EXT_LINK_N<2> — B1 (106 94)
DOUT_3+ (F2) — NO_TEST — DP_EXT_LINK_P<3> — B1 (106 94)
DOUT_3- (F1) — NO_TEST — DP_EXT_LINK_N<3> — B1 (106 94)

AUX+ (H2) — DP_EXT_AUXCH_P — B1 (94 106 95)
AUX- (H1) — DP_EXT_AUXCH_N — B1 (94 106 95)

HPDIN (J1) — DP_HPD_EXT_R — R9309 1K 1% 1/16W MF-LF 402 — DP_HPD_EXT — B1 (94 95)

To External display

AC caps for EQ AUX interception

DP_INT_AUXCH_P — NO_TEST — C9190 0.1UF 10% 16V X5R 402 — NO_TEST — DP_EQLZ_AUXCH_P — B1 (91 106)
DP_INT_AUXCH_N — NO_TEST — C9191 0.1UF 10% 16V X5R 402 — NO_TEST — DP_EQLZ_AUXCH_N — B1 (91 106)

PAGE TITLE: Display: BiDiVi Muxes

Apple Inc.

DRAWING NUMBER — SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 91 OF 110
SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE

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Apple Inc.

DRAWING NUMBER

SIZE D

REVISION 16.0.0

BRANCH

PAGE 92 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
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Apple Inc.

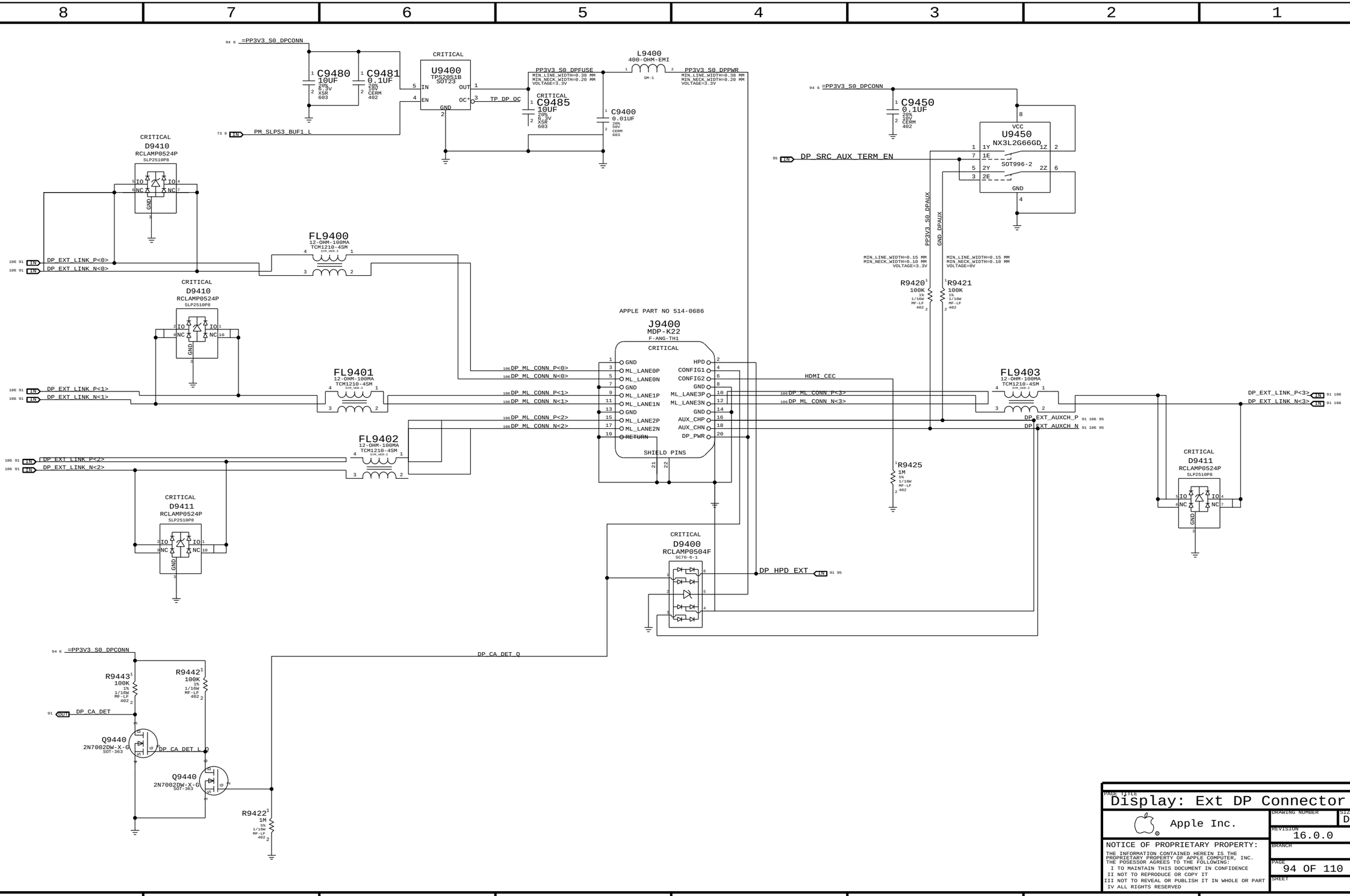
DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
93 OF 110

SHEET



PAGE TITLE
Display: Ext DP Connector

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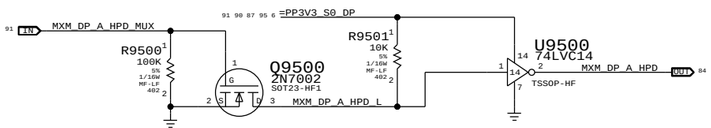
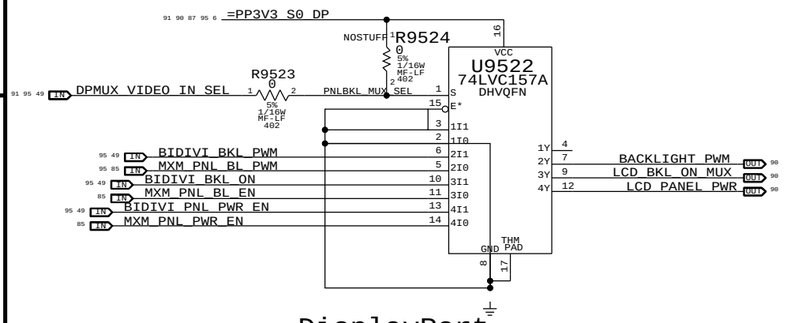
DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 94 OF 110
SHEET

Hot Plug Detect Support

Buffer for 5V tolerance

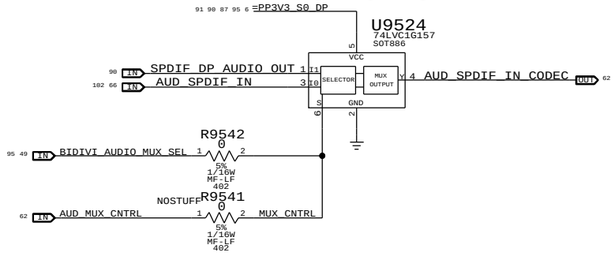


PANEL/BACKLIGHT CONTROL MUX

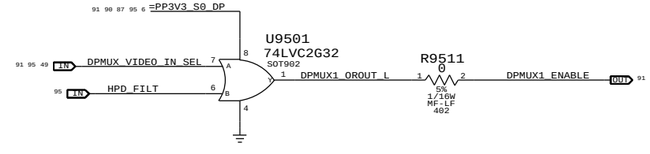


DisplayPort AUDIO MUX

PLACE NEAR U6201

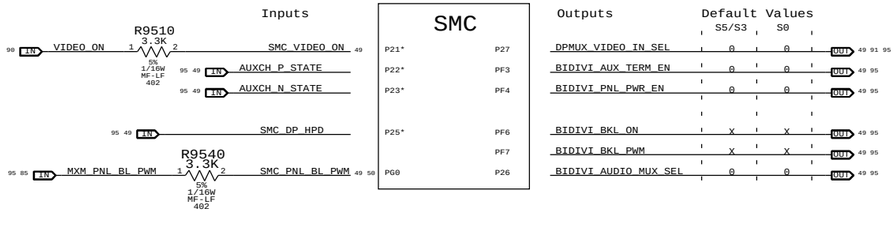


BiDiVi MUX Enable

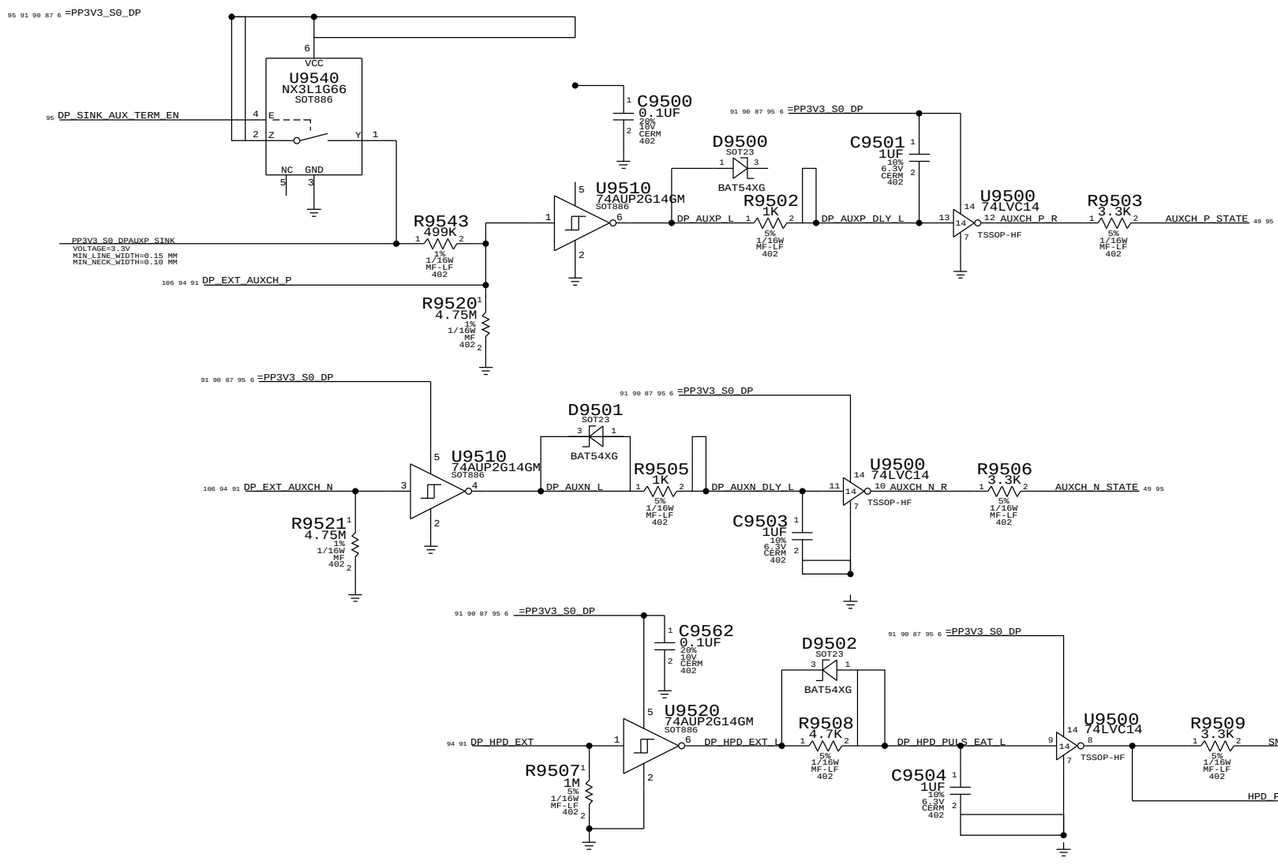


*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

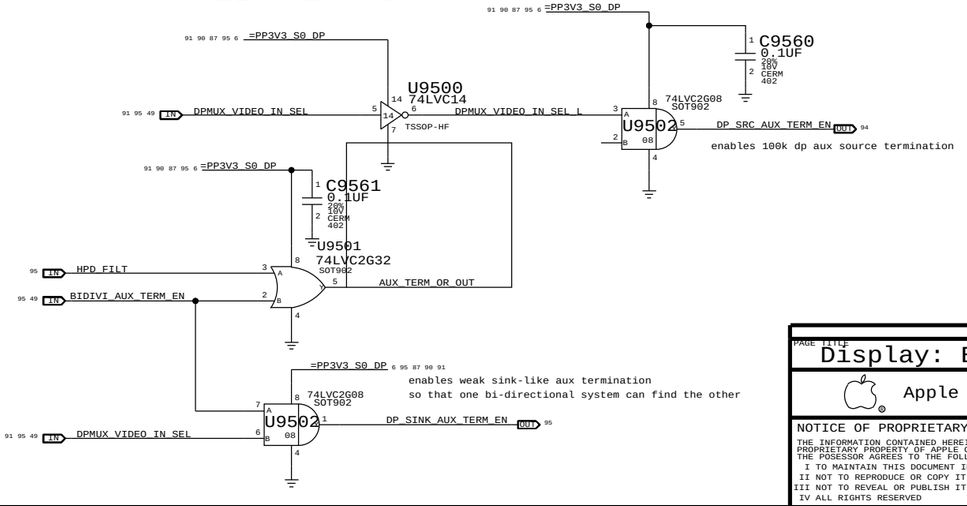
SMC Signals for BiDiVi



External AUX Channel and HPD Buffers & filters



AUX Bias Enable



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DRAWING NUMBER	SIZE D
REVISION	16.0.0
BRANCH	
PAGE	95 OF 110
SHEET	

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DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
96 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
97 OF 110

SHEET

8 7 6 5 4 3 2 1

D C B A

PAGE TITLE
BLANK PAGE

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
99 OF 110

SHEET

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 2x/1x/Async FSB signals with impedance requirements are 50-ohm single-ended.
All 4x FSB signals with impedance requirements are 42-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 90 ps. (Tighther than MCP79)
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommmends each strobe/signal group is routed on the same layer.
Intel Design Guide recommmends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.175 MM	0.175 MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_BMIL	*	0.2 MM	?
CPU_COMP	*	0.6 MM	?
CPU_GTLREF	*	0.6 MM	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	Group 0				
		FSB_42S	FSB_DATA	FSB_D_L<15..0>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
	Group 1				
		FSB_42S	FSB_DATA	FSB_D_L<31..16>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
	Group 2				
		FSB_42S	FSB_DATA	FSB_D_L<47..32>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
	Group 3				
		FSB_42S	FSB_DATA	FSB_D_L<63..48>	10 14
		FSB_42S	FSB_DATA	FSB_DINV_L<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
		FSB_DSTB_42S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB 2X Signals	Group 0				
		FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10 14
		FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
	Group 1				
		FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10 14
		FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
FSB 1X Signals		FSB_50S	FSB_1X	FSB_ADS_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ0_L	10 14
		FSB_50S	FSB_1X	FSB_BREQ1_L	14
		FSB_50S	FSB_1X	FSB_BNR_L	10 14
		FSB_50S	FSB_1X	FSB_BPRI_L	14 10
		FSB_50S	FSB_1X	FSB_DBSY_L	10 14
		FSB_50S	FSB_1X	FSB_DEFER_L	14 10
		FSB_50S	FSB_1X	FSB_DRDY_L	10 14
		FSB_50S	FSB_1X	FSB_HIT_L	10 14
		FSB_50S	FSB_1X	FSB_HITM_L	10 14
		FSB_50S	FSB_1X	FSB_LOCK_L	10 14
		FSB_50S	FSB_1X	FSB_CPURST_L	14 10 13
		FSB_50S	FSB_1X	FSB_RS_L<2..0>	14 10
		FSB_50S	FSB_1X	FSB_TRDY_L	14 10
		CPU_50S	CPU_AGTL	CPU_A20M_L	14 10
		CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	11 14
		CPU_50S	CPU_BMIL	CPU_FERR_L	10 14
		CPU_50S	CPU_AGTL	CPU_IGNNE_L	14 10
		CPU_50S	CPU_AGTL	CPU_INIT_L	14 10
		CPU_50S	CPU_AGTL	CPU_INTR	14 10
		CPU_50S	CPU_AGTL	CPU_NMI	14 10
		CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 14 50
		CPU_50S	CPU_AGTL	CPU_PWRGD	14 11 13
		CPU_50S	CPU_AGTL	CPU_SMI_L	14 10
		CPU_50S	CPU_AGTL	CPU_STPCLK_L	14 10
		CPU_50S	CPU_BMIL	PM_THRMTRIP_L	11 50 14
		CPU_50S	CPU_AGTL	FSB_CPUSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPSLP_L	11 14
		CPU_50S	CPU_AGTL	CPU_DPRSTP_L	11 14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
		MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
		MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	14 10
		CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	14 10
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	14 13
		CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	14 13
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
		CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
		CPU_50S	CPU_AGTL	CPU_IERR_L	10
		CPU_50S	CPU_GTLREF	CPU_GTLREF0	11 29 10
		CPU_50S	CPU_GTLREF	CPU_GTLREF1	11 29 10
		CPU_27P4S	CPU_COMP	CPU_COMP<8>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<3>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<2>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<1>	11
		CPU_27P4S	CPU_COMP	CPU_COMP<0>	11
		CPU_50S	CPU_ITP	CPU_XDP_TDI	13 11
		CPU_50S	CPU_ITP	CPU_XDP_TDO	11 13
		CPU_50S	CPU_ITP	CPU_XDP_TMS	13 11
		CPU_50S	CPU_ITP	CPU_XDP_TCK	13 11
		CPU_50S	CPU_ITP	CPU_XDP_TRST_L	13 11
		CPU_50S	CPU_ITP	CPU_XDP_BPM_L<5..0>	11 13
		CPU_50S	CPU_ITP	CPU_XDP_BPMB<3..0>	11 13
		CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_BMIL	CPU_VID<7..0>	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_P	12 71
		CPU_27P4S	CPU_VCCSENSE	CPU_VCC_PKG_SENSE_N	12 71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_P	71
		CPU_27P4S	CPU_VCCSENSE	VR_CPU_VSNS_R_N	71

PAGE TITLE
CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER
SIZE D

REVISION
16.0.0

BRANCH

PAGE
100 OF 110

SHEET

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 16 31
	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 16 31
	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 31
	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 31
	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<1..0>	15 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<4..3>	16 33
	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<4..3>	16 33
	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 16 32
	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 16 32
	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 32
	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 32
	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 33
	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 33
	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 33

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 33
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 33
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER
SIZE: D
REVISION: 16.0.0
BRANCH
PAGE: 101 OF 110
SHEET

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?
MCP_PEX_COMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	0.2 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 86
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 86
	PCIE_90D	PCIE	PEG_D2R_P<15..0>	86 9
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	86 9
	PCIE_90D	PCIE	MXM_PCIE_R2D_P<15..0>	86 84
	PCIE_90D	PCIE	MXM_PCIE_R2D_N<15..0>	86 84
	PCIE_90D	PCIE	MXM_PCIE_D2R_P<15..0>	84 86
	PCIE_90D	PCIE	MXM_PCIE_D2R_N<15..0>	84 86
PCIE I/O				
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_P	34
	PCIE_90D	PCIE	PCIE_MINI_R2D_L_N	34
	PCIE_90D	PCIE	PCIE_MINI_D2R_P	34 17
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	34 17
	PCIE_90D	PCIE	PCIE_FW_R2D_P	41
	PCIE_90D	PCIE	PCIE_FW_R2D_N	41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 41
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 41
	PCIE_90D	PCIE	PCIE_FW_D2R_P	41 17
	PCIE_90D	PCIE	PCIE_FW_D2R_N	41 17
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	41
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	41
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9 87
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9 87
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 41
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 41
SATA				
	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_HDD_R2D_P	45 109
	SATA_100D	SATA	SATA_HDD_R2D_N	45 109
	SATA_100D	SATA	SATA_HDD_D2R_P	45 20
	SATA_100D	SATA	SATA_HDD_D2R_N	45 20
	SATA_100D	SATA	SATA_HDD_D2R_C_P	45 109
	SATA_100D	SATA	SATA_HDD_D2R_C_N	45 109
	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 45
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 45
	SATA_100D	SATA	SATA_ODD_R2D_P	45 109
	SATA_100D	SATA	SATA_ODD_R2D_N	45 109
	SATA_100D	SATA	SATA_ODD_D2R_P	45 20
	SATA_100D	SATA	SATA_ODD_D2R_N	45 20
	SATA_100D	SATA	SATA_ODD_D2R_C_P	45 109
	SATA_100D	SATA	SATA_ODD_D2R_C_N	45 109
	MCP_SATA	SATA_TERMP	MCP_SATA_TERMP	20
MISC				
	MCP_SATA	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
	MCP_DV_COMP	MCP_PEX_COMP	MCP_IFPAB_RSET	18 26
	MCP_SATA	MCP_PEX_COMP	MCP_IFPAB_VPROBE	18 26
			PM_SLP_S3_L	21 9
			PM_SLP_S4_L	21 70

PAGE TITLE: MCP Constraints 1

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 102 OF 110

SHEET

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_MCP_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
	PCI_55S	PCI	PCI_REQ0_L 19
	PCI_55S	PCI	PCI_REQ1_L 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19
	LPC_55S	LPC	LPC_AD<3..0> 19 49 51
	LPC_55S	LPC	LPC_AD_R<3..0> 19
	LPC_55S	LPC	LPC_FRAME_L 19 49 51
	LPC_55S	LPC	LPC_FRAME_R_L 19
	LPC_55S	LPC	LPC_RESET_L 19 9
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19 9
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 9 49
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 9 51
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R 21 9
	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK 9 49
	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20
	USB_90D	USB	USB_EXTA_P 20 46
	USB_90D	USB	USB_EXTA_N 20 46
	USB_90D	USB	USB_PORT0_P 46
	USB_90D	USB	USB_PORT0_N 46
	USB_90D	USB	USB_EXTB_P 20 46
	USB_90D	USB	USB_EXTB_N 20 46
	USB_90D	USB	USB_PORT1_P 46
	USB_90D	USB	USB_PORT1_N 46
	USB_90D	USB	USB_EXTC_P 20 46
	USB_90D	USB	USB_EXTC_N 20 46
	USB_90D	USB	USB_PORT2_P 46
	USB_90D	USB	USB_PORT2_N 46
	USB_90D	USB	USB_EXTD_P 20 46
	USB_90D	USB	USB_EXTD_N 20 46
	USB_90D	USB	USB_D_MUXED_P 46
	USB_90D	USB	USB_D_MUXED_N 46
	USB_90D	USB	USB_PORT3_P 46
	USB_90D	USB	USB_PORT3_N 46
	USB_90D	USB	USB_CAMERA_P 20 47
	USB_90D	USB	USB_CAMERA_N 20 47
	USB_90D	USB	USB_CAMERA_L_P 47 109
	USB_90D	USB	USB_CAMERA_L_N 47 109
	USB_90D	USB	USB_BT_P 20 47
	USB_90D	USB	USB_BT_N 20 47
	USB_90D	USB	USB_BT_L_P 47 109
	USB_90D	USB	USB_BT_L_N 47 109
	USB_90D	USB	USB_IR_P 20 47
	USB_90D	USB	USB_IR_N 20 47
	USB_90D	USB	USB_IR_L_P 47 109
	USB_90D	USB	USB_IR_L_N 47 109
	USB_90D	USB	USB_SDCARD_P 20 47
	USB_90D	USB	USB_SDCARD_N 20 47
	USB_90D	USB	USB_SDCARD_L_P 47 109
	USB_90D	USB	USB_SDCARD_L_N 47 109
	MCP_50S	SPI	SPI_CLK_R 21 51 61
	MCP_50S	SPI	SPI_CLK 61
	MCP_50S	SPI	SPI_MOSI_R 21 51 61
	MCP_50S	SPI	SPI_MOSI 61
	MCP_50S	SPI	SPI_MISO 51 61 21
	MCP_50S	SPI	SPI_MISO_R 61
	MCP_50S	SPI	SPI_CS0_R_L 21 51
	MCP_50S	SPI	SPI_CS0_L 51
	HDA_55S	HDA	HDA_BIT_CLK 21 62
		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21
	HDA_55S	HDA	HDA_BIT_CLK_R 21
	HDA_55S	HDA	HDA_RST_L 21 62
	HDA_55S	HDA	HDA_RST_R_L 21
	HDA_55S	HDA	HDA_SDOUT 21 62
	HDA_55S	HDA	HDA_SDOUT_R 21
	HDA_55S	HDA	HDA_SYNC 21 62
	HDA_55S	HDA	HDA_SYNC_R 21
	HDA_55S	HDA	HDA_SDIN0 62 21
	HDA_55S	HDA	AUD_SDI_R 62
		HDA	AUD_SPDIF_IN 66 95
		HDA	AUD_SPDIF_OUT 62 66
		HDA	AUD_SPDIF_CHIP 62
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALOUT 21 28
	CLK_MCP_XTAL	XTAL	MCP_CLK25M_XTALIN 28 21
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALOUT 21 28
	CLK_MCP_XTAL	XTAL	RTC_CLK32K_XTALIN 28 21

PAGE TITLE: MCP Constraints 2

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH:

PAGE: 103 OF 110

SHEET:

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP		MCP_MII_COMP_GND	18
ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 38
ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	38 37
ENET_MII_55S	ENET_MII	ENET_MDIO	18 37
ENET_MII_55S	ENET_MII	ENET_MDC	18 37
ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	37 18
ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	37
ENET_MII_55S	ENET_MII	ENET_RXD<0>	37 18
ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	37
ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	37 18
ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	37
ENET_MII_55S	ENET_MII	ENET_RX_CTRL	37 18
ENET_MII_55S	ENET_MII	ENET_RXCTL_R	37
ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 37
ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 37
ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 37
ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 37
ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	37 39
ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	37 39
ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	39
ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	39

PAGE TITLE: Ethernet Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 104 OF 110

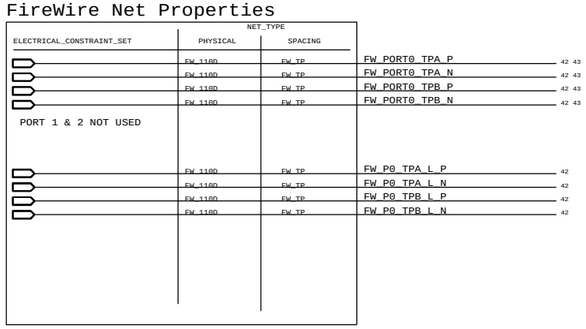
SHEET

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties



PAGE TITLE
FireWire Constraints

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 105 OF 110
SHEET

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	52
	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	52
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	105 52
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	105 52
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	105 52
	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	105 52
	SMB_5SS	SMB	SMBUS_MCP_0_CLK	13 21 52
	SMB_5SS	SMB	SMBUS_MCP_0_DATA	13 21 52

PAGE TITLE
SMC Constraints

Apple Inc.

DRAWING NUMBER
SIZE D
REVISION 16.0.0
BRANCH
PAGE 106 OF 110
SHEET

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	0.08MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	3:1_SPACING
DISPLAYPORT	POWER	*	PWR_P2MM
DISPLAYPORT	GND	*	GND_P2MM

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
ASSINGED IN CONT. MGR.				
	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	94
	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	94
	DP_100D	DISPLAYPORT	DP_INT_LINK_P<3..0>	91 90
	DP_100D	DISPLAYPORT	DP_INT_LINK_N<3..0>	91 90
	DP_100D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0>	90
	DP_100D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0>	90
	DP_100D	DISPLAYPORT	DP_INT_AUXCH_P	91 90
	DP_100D	DISPLAYPORT	DP_INT_AUXCH_N	91 90
	DP_100D	DISPLAYPORT	DP_EXT_LINK_P<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_EXT_LINK_N<3..0>	91 94
	DP_100D	DISPLAYPORT	DP_EXT_AUXCH_P	91 94 95
	DP_100D	DISPLAYPORT	DP_EXT_AUXCH_N	91 94 95
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>	84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>	84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0>	91
	DP_100D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0>	91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_P	84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_N	84 91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_C_P	91
	DP_100D	DISPLAYPORT	MXM_DP_A_AUX_C_N	91
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	84 91
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	84 91
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0>	91
	DP_100D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0>	91
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_P	84 91
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_N	84 91
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_C_P	91
	DP_100D	DISPLAYPORT	MXM_DP_C_AUX_C_N	91
	DP_100D	DISPLAYPORT	DP_EQLZ_P<3..0>	
	DP_100D	DISPLAYPORT	DP_EQLZ_N<3..0>	
	DP_100D	DISPLAYPORT	DP_MUX_P<3..0>	91
	DP_100D	DISPLAYPORT	DP_MUX_N<3..0>	91
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_P	91
	DP_100D	DISPLAYPORT	DP_MUX_AUXCH_N	91
	DP_100D	DISPLAYPORT	DP_EQLZ_AUXCH_P	91
	DP_100D	DISPLAYPORT	DP_EQLZ_AUXCH_N	91
	MCP_DV_COMP		MCP_HDMI_RSET	18 26
	MCP_DV_COMP		MCP_HDMI_VPROBE	18 26

PAGE TITLE: Graphics Constraints

Apple Inc.

DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 107 OF 110

SHEET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
AUDIO	*	*	AUDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D	TOP			0.1 MM	600 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_90D	TOP				500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS	TOP			0.1 MM	500 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP	*			0.25 MM	250 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
		PPDDR_MEM	=PP1V5_S3_MEM_A	6 30 31
		PPDDR_MEM	=PP1V5_S3_MEM_B	6 30 32
		SWITCHNODE	VR_CPU_SW1	72
		SWITCHNODE	VR_CPU_SW2	72
		SWITCHNODE	VR_CPU_SW3	72
		SWITCHNODE	1V8_SW	
		SWITCHNODE	1V1S5_SW	79
		SWITCHNODE	PVTTS0_PHASE	76
		SWITCHNODE	3V3S5_SW	76
		SWITCHNODE	5VS3_SW	73
		SWITCHNODE	MCPCORES0_PHASE	74
	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	55
	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	55
	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	55
	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	55
	THERM_DIFF	THERMAL	CPU_THERMD_P	55 11
	THERM_DIFF	THERMAL	CPU_THERMD_N	11 55
	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	55
	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	55
	THERM_DIFF	THERMAL	MCP_THMDIODE_P	21 55
	THERM_DIFF	THERMAL	MCP_THMDIODE_N	21 55
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_P	53
	THERM_DIFF	THERMAL	MXM_PWRSRC_SENSOR_N	53
	THERM_DIFF	THERMAL	SENSE_1V5_S0_P	54
	THERM_DIFF	THERMAL	SENSE_1V5_S0_N	54
	THERM_DIFF	THERMAL	SNS_LCD_P	55 109
	THERM_DIFF	THERMAL	SNS_LCD_N	55 109
	THERM_DIFF	THERMAL	SNS_ODD_P	55 109
	THERM_DIFF	THERMAL	SNS_ODD_N	55 109
	THERM_DIFF	THERMAL	SNS_CPU_H_P	55
	THERM_DIFF	THERMAL	SNS_CPU_H_N	55
	THERM_DIFF	THERMAL	SNS_MCP_P	55
	THERM_DIFF	THERMAL	SNS_MCP_N	55
	THERM_DIFF	THERMAL	SNS_AMB_P	55 109
	THERM_DIFF	THERMAL	SNS_AMB_N	55 109
	THERM_DIFF	THERMAL	SNS_MXM_P	55
	THERM_DIFF	THERMAL	SNS_MXM_N	55
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	72 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	72 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	72 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	72 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	72 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	72 71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	71
	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	71
1215		THERMAL	SMC_CPU_ISENSE	53 49
1216		THERMAL	VR_CPU_IOUT	71 53
1217		THERMAL	VR_ISNS_CPU_P	53
1218		THERMAL	VR_ISNS_CPU_N	53
1219		THERMAL	SNS_PS_CPU_ISNS	53
1220		THERMAL	SMC_CPU_VSENSE	53 49
1221		THERMAL	CPU_VCC_SENSE	12 53
1222		THERMAL	SMC_GPU_VSENSE	49 53
1223		THERMAL	SMC_GPU_ISENSE	53 49
1224		THERMAL	SMC_1V5_S0_ISENSE	50 54
1225		THERMAL	SMC_1V5_S0_ISENSE_R	54
1226		THERMAL	SMC_1V5_S0_VSENSE	50 54
1227		THERMAL	SMC_MCP_CORE_ISENSE	50 54
1228		THERMAL	SMC_MCP_CORE_VSENSE	50 54
1229		THERMAL	MCPCORES0_IMON	74 54
1230		THERMAL	CPU_PECI_L	11 55
1231		THERMAL	SMB_PECI_L	55
1232		THERMAL	CPU_PECI_MCP	14 55
		THERMAL	HDD_OOB_TEMP_FILT	55
1233		THERMAL	HDD_OOB_TEMP	55
1234		THERMAL	HDD_OOB_TEMP_R	55
1235		THERMAL	SMC_HDD_OOB_TEMP	55

PAGE TITLE
K22/K23 SPECIFIC CONSTRAINTS

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REVISION 16.0.0

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PAGE 108 OF 110

SHEET

K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.300 MM	0.085 MM	=STANDARD		
27P4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	TOP,BOTTOM	Y	0.151 MM	0.085 MM	=STANDARD		
42_OHM_SE	*	Y	0.136 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	*	POWER_WIDTH
VR_CTL_PHY	*	POWER_WIDTH

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI,LPC,SMB,HDA,SPI,RGMII,SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

PAGE TITLE: RULE DEFINITIONS

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DRAWING NUMBER | SIZE: D

REVISION: 16.0.0

BRANCH

PAGE: 109 OF 110

SHEET

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

102 47	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
102 47	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

102 47	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
102 47	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

102 47	IN	USB_BT_L_P	FUNC_TEST=TRUE
102 47	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

102 47	IN	USB_IR_L_P	FUNC_TEST=TRUE
102 47	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

45 101	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
45 101	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
45 101	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
45 101	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
49 45	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

101 45	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
101 45	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
101 45	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
101 45	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

55 107	IN	SNS_LCD_P	FUNC_TEST=TRUE
55 107	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

55 107	IN	SNS_AMB_P	FUNC_TEST=TRUE
55 107	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

55 107	IN	SNS_ODD_P	FUNC_TEST=TRUE
55 107	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

56	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH0_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
56	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

57	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
57	IN	FAN_TACH2_L	FUNC_TEST=TRUE
57	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
57	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

56	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
56	IN	FAN_TACH1_L	FUNC_TEST=TRUE
56	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
56	IN	FAN_1_GND	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

66	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
66	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
66	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

	IN	AUD_SPKR_OUTL02R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL02R_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01R_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01R_N	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

	IN	AUD_SPKR_OUTL02L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL02L_N	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01L_P	FUNC_TEST=TRUE
	IN	AUD_SPKR_OUTL01L_N	FUNC_TEST=TRUE

		GND	16 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
6 78	IN	PP3V3_S3	2 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
6 73	IN	PP5V_S3_REG	2 TP'S	FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
6 78	IN	PP5V_S0		FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

PAGE TITLE
ICT/FCT

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DRAWING NUMBER
SIZE D

REVISION
16.0.0

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PAGE
110 OF 110

SHEET