1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
		546198			

SCHEM,MLB,M82
PVT
11/14/2007

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM,MLB,M82	SCH	CRITICAL	
820-2179	1	PCBF,MLB,M82	PCB	CRITICAL	

DRAWING
TITLE=M82_MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed Nov 14 17:25:50 2007

DIMENSIONS ARE IN MILLIMETERS

XX ±

X.XX ±

X.XXX ±

ANGLES ±

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

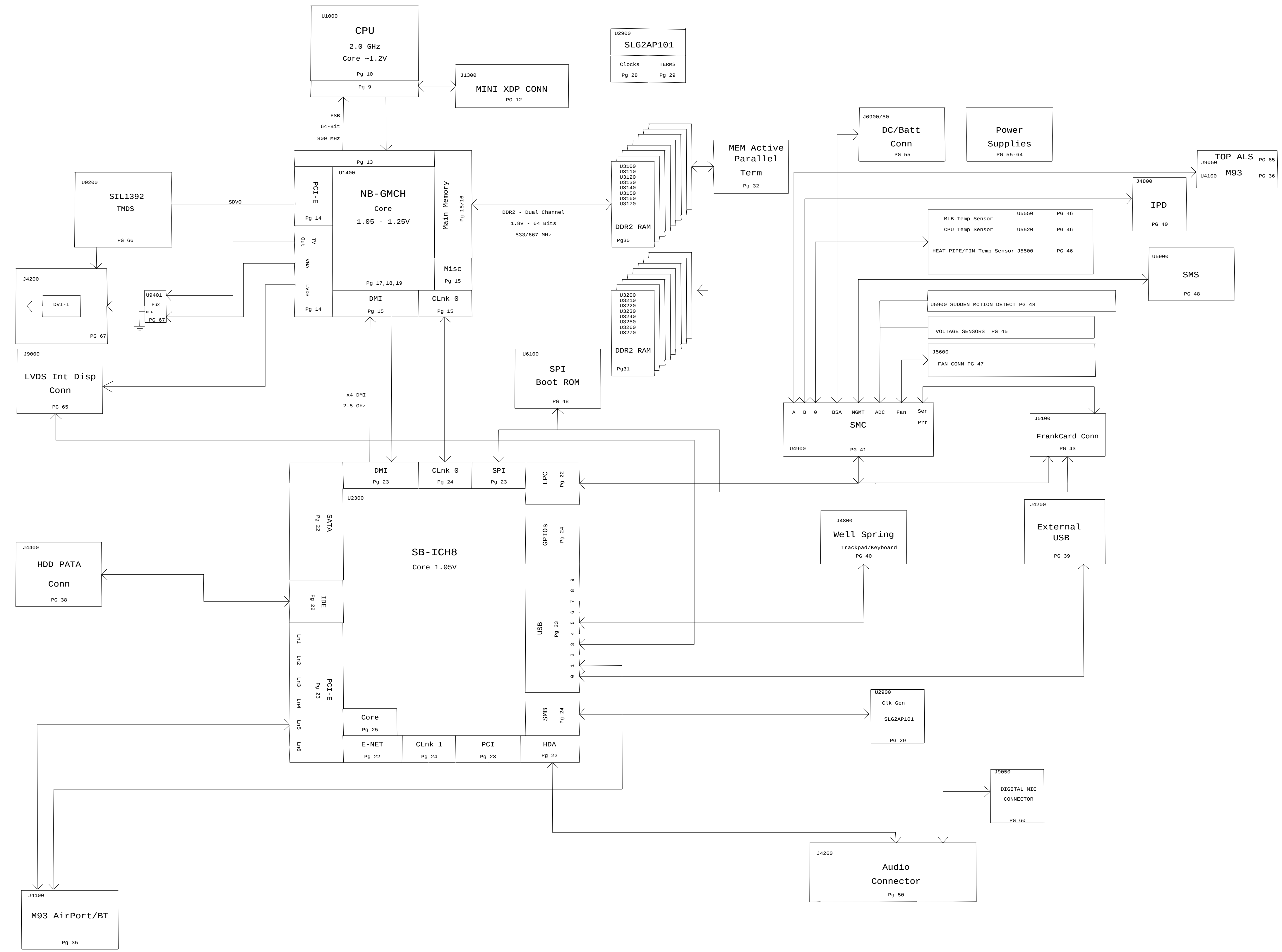
APPLE INC.

TITLE

SCHEM,MLB,M82

DRAWING NUMBER 051-7230

REV. B.0.0



System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

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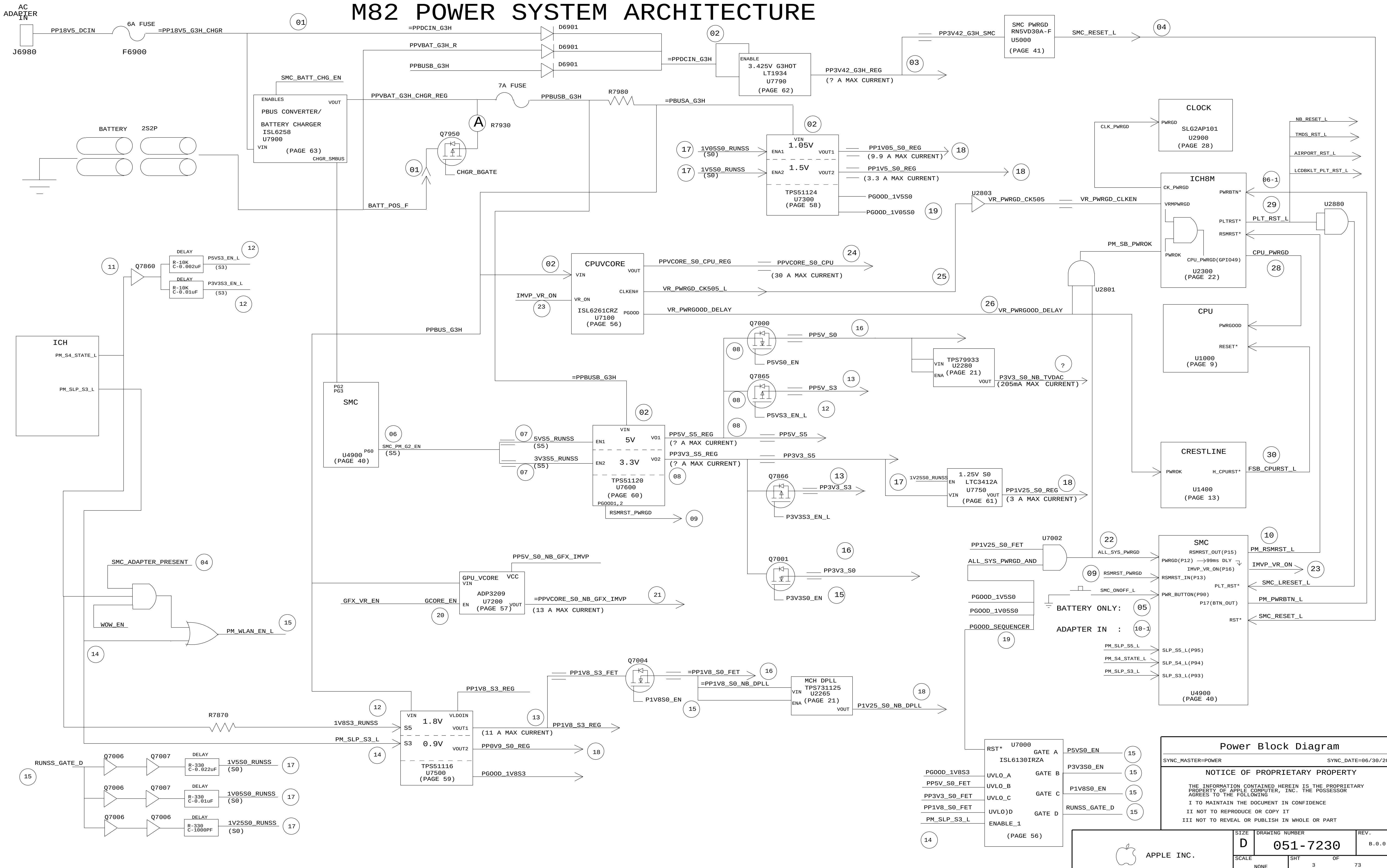
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 2	OF 73

M82 POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=POWER SYNC_DATE=06/30/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 3 OF 73

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7886	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M82	EEE_XSC,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9024	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M82	EEE_YMS,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9133	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M82	EEE_Z80,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9134	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M82	EEE_Z81,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9204	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M82	EEE_ZU5,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9205	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M82	EEE_ZU6,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9206	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M82	EEE_ZU7,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9207	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M82	EEE_ZU8,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9208	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M82	EEE_ZU9,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9209	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M82	EEE_ZUA,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_TY_CAP
630-9210	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M82	EEE_ZUB,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9211	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M82	EEE_ZUC,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_TY_CAP

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XSC]	CRITICAL	EEE_XSC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:YMS]	CRITICAL	EEE_YMS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z80]	CRITICAL	EEE_Z80
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z81]	CRITICAL	EEE_Z81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU5]	CRITICAL	EEE_ZU5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M82_COMMON	ALTERNATE,COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3
M82_COMMON1	ISL6258,BOOTROM_DEVEL,SMC_PRGRM
M82_COMMON2	SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB
M82_COMMON3	
M82_MICRON	DRAM_MICRON,DRAM_SPD_1
M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2
M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF
M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF
M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ
338S0420	1	IC,965GM,CRESTLINE,USFF BGA	U1400	CRITICAL	
338S0421	1	IC,ICH8M,USFF BGA	U2300	CRITICAL	
359S0130	1	LOW POWER CLOCK SYNTHESIZER,SLG2AP101,68PIN	U2900	CRITICAL	
335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH,VWQPN	U6100	CRITICAL	BOOTROM_BLANK_2MB
335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL
341S2112	1	IC,EFI,BOOTROM FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK
341S2173	1	IC,PRGM,SST SST89V54RD,UCNTRLR,M82	U9300	CRITICAL	SST8051_PRGRM
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ
338S0514	1	IC,965GM,CRESTLINE,PRQ,USFF BGA	U1400	CRITICAL	NB_PRQ
338S0515	1	IC,ICH8M,PRQ,USFF BGA	U2300	CRITICAL	SB_PRQ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0044	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE NONE	SHT 4	OF 73

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2144,C2151,C2170	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C2265,C2280,C2600,C2703,C2805,C2900,C7000,C7100,C7101	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2144,C2151,C2170	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C2265,C2280,C2600,C2703,C2805,C2900,C7000,C7100,C7101	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	5	CAP, 1UF, 6.3V, 10%, 0402	C1801,C1802,C2144,C2151,C2170	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C2265,C2280,C2600,C2703,C2805,C2900,C7000,C7100,C7101	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9980,C9981,C9982,C9983,C9984,C9985,C9986,C9987,C9988,C9989	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9990,C9991,C9992,C9993,C9994,C9995,C9996,C9997	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C128[illegible],C1283,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1622,C1624,C4800	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3400,C3401,C3404,C3405,C3410,C3411,C3412,C3414,C3415,C3416	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3420,C3421,C3424,C3425,C3430,C3431,C3434,C3435,C3440,C3441	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3442,C3444,C3445,C3446,C3450,C3451,C3454,C3455	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9980,C9981,C9982,C9983,C9984,C9985,C9986,C9987,C9988,C9989	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9990,C9991,C9992,C9993,C9994,C9995,C9996,C9997	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C128[illegible],C1283,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1622,C1624,C4800	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3400,C3401,C3404,C3405,C3410,C3411,C3412,C3414,C3415,C3416	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3420,C3421,C3424,C3425,C3430,C3431,C3434,C3435,C3440,C3441	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3442,C3444,C3445,C3446,C3450,C3451,C3454,C3455	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9980,C9981,C9982,C9983,C9984,C9985,C9986,C9987,C9988,C9989	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C9990,C9991,C9992,C9993,C9994,C9995,C9996,C9997	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C128[illegible],C1283,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1622,C1624,C4800	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3400,C3401,C3404,C3405,C3410,C3411,C3412,C3414,C3415,C3416	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3420,C3421,C3424,C3425,C3430,C3431,C3434,C3435,C3440,C3441	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3442,C3444,C3445,C3446,C3450,C3451,C3454,C3455	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	9	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	6	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	9	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	6	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	9	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	6	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	[illegible]	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE | SHT 5 OF 73

ICT Test Points

ICT_TEST

These nets have a ICT_TEST property   This indicates a MUSTHAVE requirement for ICT

TRUE PP18V5_DCIN
TRUE BATT_POS
TRUE PP3V3_S5
TRUE PP3V42_G3H
TRUE GND
TRUE PM_SLP_S3_L
TRUE PM_S4_STATE_L
TRUE PM_SLP_S5_L
TRUE SMC_PM_G2_EN
TRUE IMVP_VR_ON
TRUE GFX_VR_EN
TRUE SMC_BATT_CHG_EN
TRUE SMC_ONOFF_L
TRUE ALL_SYS_PWRGD_AND
TRUE PPVBAT_G3H_CHGR_REG
TRUE CPU_PWRGD
TRUE PM_RSMRST_L
TRUE PM_PWRBTN_L
TRUE TP_PCI_RST_L
TRUE PLT_RST_L
TRUE SMC_RESET_L
TRUE PM_SYSRST_L
TRUE PP1V5_S0
TRUE PP1V05_S0
TRUE PP1V8_S0
TRUE PP1V8_S3
TRUE PP0V9_S0
TRUE PP0V9_S3
TRUE PP1V25_S0
TRUE PP5V_S5
TRUE PP5V_S3
TRUE PP5V_S0
TRUE PP3V3_S3
TRUE PP3V3_A_S0
TRUE PP3V3_B_S0
TRUE PPVCORE_S0_CPU
TRUE PPVCORE_S0_NB_GFX
TRUE XDP_TCK
TRUE XDP_TDI
TRUE XDP_TDO
TRUE XDP_TMS
TRUE XDP_TRST_L
TRUE XDP_CPURST_L
TRUE XDP_BPM_L<4>
TRUE XDP_BPM_L<5>
TRUE XDP_DBRESET_L
TRUE XDP_PWRGD
TRUE SPI_A_SCLK_R
TRUE SMC_MANUAL_RST_L
TRUE SMC_TCK
TRUE SMC_TDI
TRUE SMC_TDO
TRUE SMC_TMS
TRUE SMC_TRST_L
TRUE CPU_A20M_L
TRUE CPU_DPRSTP_L
TRUE CPU_DPSLP_L
TRUE CPU_FERR_L
TRUE NB_BSEL<0>
TRUE NB_BSEL<1>
TRUE NB_BSEL<2>
TRUE NB_CFG<16>
TRUE NB_CFG<19>
TRUE NB_CFG<20>

TRUE NB_CFG<3>
TRUE NB_CFG<4>
TRUE NB_CFG<5>
TRUE NB_CFG<6>
TRUE NB_CFG<7>
TRUE NB_CFG<8>
TRUE NB_CFG<9>
TRUE NB_RESET_L
TRUE NB_SB_SYNC_L
TRUE NB_TEST1
TRUE NB_TEST2
TRUE 1V05S0_RUNSS
TRUE 1V05S0_TRIP
TRUE 1V25S0_RUNSS
TRUE 1V51V05S0_V5FILT
TRUE 1V5S0_RUNSS
TRUE 1V5S0_TRIP
TRUE 1V8S3_CS
TRUE 1V8S3_V5FILT
TRUE 1V8S3_VDDQSET
TRUE 3V3S5_CS
TRUE 5V3V3S5_TONSEL
TRUE 5V3V3S5_V5FILT
TRUE 5V3V3S5_VREF
TRUE 5V3V3S5_VREG3
TRUE 5VS5_CS
TRUE 5VS5_VREG
TRUE ADAPTER_SENSE
TRUE AIRPORT_RST_L
TRUE ALL_SYSPWRGD_DLY
TRUE ALL_SYS_PWRGD
TRUE ALL_SYS_PWRGD_AND
TRUE ARB_DETECT_L
TRUE AUD_MIC_CLK
TRUE AUD_MIC_CLK_F
TRUE AUD_MIC_DATA
TRUE AUD_MIC_DATA_F
TRUE BATT_POS
TRUE BATT_POS_F
TRUE BOOTROM_OVR_EN_L
TRUE CHGR_AGATE
TRUE CHGR_AMON
TRUE CHGR_BGATE
TRUE CHGR_BMON
TRUE CHGR_BOOT
TRUE CHGR_CSIN
TRUE CHGR_CSIP
TRUE CHGR_CSON
TRUE CHGR_CSOP
TRUE CHGR_DCIN
TRUE CHGR_LOWCURRENT_GATE
TRUE CHGR_LOWCURRENT_REF
TRUE CHGR_SGATE
TRUE CHGR_SGATE_DIV
TRUE CHGR_VCOMP_R
TRUE CHGR_VDD
TRUE CHGR_VDDP
TRUE CHGR_VNEG
TRUE CHGR_VNEG_R
TRUE CK505_CLK14P3M_TIMER
TRUE CK505_FSA
TRUE CK505_FSB_TEST_MODE
TRUE CK505_FSC
TRUE CK505_PCI3_CLK

TRUE CK505_PCI5_FCTSEL1
TRUE CK505_PCIF0_CLK
TRUE CK505_PCIF1_CLK
TRUE CK505_SRC_CLKREQ6_L
TRUE CK505_USB48_FSA
TRUE CK505_XTAL_OUT
TRUE CLINK_NB_CLK
TRUE CLINK_NB_DATA
TRUE CLINK_NB_RESET_L
TRUE CLK_PWRGD
TRUE CPU_A20M_L
TRUE CPU_BSEL<0>
TRUE CPU_BSEL<1>
TRUE CPU_BSEL<2>
TRUE CPU_COMP<0>
TRUE CPU_COMP<1>
TRUE CPU_COMP<2>
TRUE CPU_COMP<3>
TRUE CPU_DPRSTP_L
TRUE CPU_DPSLP_L
TRUE CPU_FERR_L
TRUE CPU_GTLREF
TRUE CPU_IERR_L
TRUE CPU_IGNNE_L
TRUE CPU_INIT_L
TRUE CPU_INTR
TRUE CPU_NMI
TRUE CPU_PROCHOT_BUF
TRUE CPU_PROCHOT_L
TRUE CPU_PROCHOT_L_R
TRUE CPU_PWRGD
TRUE CPU_SMI_L
TRUE CPU_STPCLK_L
TRUE CPU_THERMD_N
TRUE CPU_THERMD_P
TRUE CPU_THERMTRIP_R
TRUE CPU_VCCSENSE_N
TRUE CPU_VCCSENSE_P
TRUE CPU_VID<6..0>
TRUE CRT_BLUE
TRUE CRT_GREEN
TRUE CRT_HSYNC_LS
TRUE CRT_HSYNC_LS_R
TRUE CRT_HSYNC_R
TRUE CRT_RED
TRUE CRT_TVO_IREF
TRUE CRT_VSYNC_LS
TRUE CRT_VSYNC_LS_R
TRUE CRT_VSYNC_R
TRUE DEBUG_RESET_L
TRUE DLY_OFF_A
TRUE DLY_OFF_B
TRUE DLY_OFF_C
TRUE DLY_OFF_D
TRUE DMI_IRCOMP_R
TRUE DMI_N2S_N<3..0>
TRUE DMI_N2S_P<3..0>
TRUE DMI_S2N_N<3..0>
TRUE DMI_S2N_P<3..0>
TRUE DVI_HOST
TRUE DVI_HOTPLUG_DET
TRUE DVI_HOTPLUG_DET_BUF
TRUE DVI_HOTPLUG_DET_DEL_L
TRUE DVI_HOTPLUG_DET_INT_L

TRUE DVI_HPDET_RC
TRUE EXCARD_OC_L
TRUE EXTAUSB_OC_F_L
TRUE EXTAUSB_OC_L
TRUE EXTBUSB_OC_L
TRUE EXTGPU_LVDS_EN
TRUE EXT_COMPVID_B
TRUE EXT_C_R
TRUE EXT_Y_G
TRUE FAN_RT_PWM
TRUE FAN_RT_TACH
TRUE FRANKCARD_GPIO
TRUE FSB_CLK_CPU_N
TRUE FSB_CLK_CPU_P
TRUE FSB_CLK_NB_N
TRUE FSB_CLK_NB_P
TRUE FSB_CPURST_L
TRUE FWH_MFG_MODE
TRUE GCORE_BST_D
TRUE GCORE_COMP_R
TRUE GCORE_CSFB
TRUE GCORE_FBRTN
TRUE GCORE_LLINE
TRUE GCORE_PMON
TRUE GCORE_PMONFS
TRUE GCORE_PWRGD
TRUE GCORE_RAMP
TRUE GCORE_RPM
TRUE GCORE_RT
TRUE GCORE_ST
TRUE GCORE_SW
TRUE GCORE_SW_R
TRUE GCORE_VARFREQ
TRUE GCORE_VCC
TRUE GCORE_VDC_DIV
TRUE GCORE_VRPM
TRUE GFX_VID<3..0>
TRUE GFX_VR_EN
TRUE GLAN_COMP
TRUE GND_1V51V05S0_SGND
TRUE GND_1V8S3_CSGND
TRUE GND_1V8S3_SGND
TRUE GND_5V3V3S5_SGND
TRUE GND_ALS_F
TRUE GND_CHGR_SGND
TRUE GND_GCORE_PGND
TRUE GND_IMVP6_SGND
TRUE GND_LCDBKLT_GNDA
TRUE GND_P1V2S3_SGND
TRUE GND_SMC_AVSS
TRUE HDA_BIT_CLK
TRUE HDA_BIT_CLK_R
TRUE HDA_DOCK_EN_L
TRUE HDA_RST_L
TRUE HDA_RST_L_R
TRUE HDA_SDIN0
TRUE HDA_SDIN1
TRUE HDA_SDOUT
TRUE HDA_SDOUT_R
TRUE HDA_SYNC
TRUE HDA_SYNC_R
TRUE HDMI_HOST
TRUE I2C_TOP_ALS_SCL_F
TRUE I2C_TOP_ALS_SDA_F

TRUE IDE_IRQ14
TRUE IDE_PDA<2..0>
TRUE IDE_PDCS1_L
TRUE IDE_PDCS3_L
TRUE IDE_PDD<15..0>
TRUE IDE_PDDACK_L
TRUE IDE_PDDREQ
TRUE IDE_PDIORDY
TRUE IDE_PDIOR_L
TRUE IDE_PDIOW_L
TRUE IDE_RESET_BUF_L
TRUE IDE_RESET_L
TRUE IMVP6_BOOT
TRUE IMVP6_BOOT_RC
TRUE IMVP6_COMP_R
TRUE IMVP6_DROOP
TRUE IMVP6_PHASE
TRUE IMVP6_PVCC
TRUE IMVP6_RBIAS
TRUE IMVP6_SOFT
TRUE IMVP6_VDIFF
TRUE IMVP6_VDIFF_RC
TRUE IMVP6_VO_R
TRUE IMVP6_VR_TT
TRUE IMVP6_VSEN_N
TRUE IMVP6_VSEN_P
TRUE IMVP6_VSUM
TRUE IMVP6_VW
TRUE IMVP_DPRSLPVR
TRUE IMVP_VR_ON
TRUE INT_PIRQA_L
TRUE INT_PIRQB_L
TRUE INT_PIRQC_L
TRUE INT_PIRQD_L
TRUE INT_PIRQE_L
TRUE INT_PIRQF_L
TRUE INT_SERIRQ
TRUE LAN_ENERGY_DET
TRUE LAN_PHYPC
TRUE LCDBKLT_ENA
TRUE LCDBKLT_ISET
TRUE LCDBKLT_OVP
TRUE LCDBKLT_PWM_UNBUF
TRUE LCDBKLT_PWREN
TRUE LCDBKLT_RT
TRUE LCDBKLT_RTN<6..1>
TRUE LCDBKLT_RTN_RC<6..1>
TRUE LCDBKLT_SSTCMP
TRUE LCDBKLT_SSTCMP_RC
TRUE LCDBKLT_VREF
TRUE LCDVDD_PWREN_L
TRUE LCDVDD_PWREN_L_R
TRUE LOCAL_CTRL_CLK
TRUE LOCAL_CTRL_DATA
TRUE LPC_AD<3..0>
TRUE LPC_FRAME_L
TRUE LSOC_H
TRUE LSOC_H_R
TRUE LVDS_A_CLK_F_N
TRUE LVDS_A_CLK_F_P
TRUE LVDS_A_CLK_N
TRUE LVDS_A_CLK_P
TRUE LVDS_A_DATA_F_N<2..0>
TRUE LVDS_A_DATA_F_P<2..0>

TRUE LVDS_A_DATA_N<2>
TRUE LVDS_A_DATA_P<2>
TRUE LVDS_DDC_CLK
TRUE LVDS_DDC_DATA
TRUE LVDS_IBG
TRUE LVDS_VDD_EN
TRUE MEM_ODT<3..0>
TRUE MEM_RCOMP
TRUE MEM_RCOMP_L
TRUE MEM_RCOMP_VOH
TRUE MEM_RCOMP_VOL
TRUE NB_BSEL<0>
TRUE NB_BSEL<1>
TRUE NB_BSEL<2>
TRUE NB_CFG<16>
TRUE NB_CFG<19>
TRUE NB_CFG<20>
TRUE NB_CFG<3>
TRUE NB_CFG<4>
TRUE NB_CFG<5>
TRUE NB_CFG<6>
TRUE NB_CFG<7>
TRUE NB_CFG<8>
TRUE NB_CFG<9>
TRUE NB_CLINK_VREF
TRUE NB_CLK100M_DPLLSS_N
TRUE NB_CLK100M_DPLLSS_P
TRUE NB_CLK100M_PCIE_N
TRUE NB_CLK100M_PCIE_P
TRUE NB_CLK96M_DOT_N
TRUE NB_CLK96M_DOT_P
TRUE NB_CLKREQ_L
TRUE NB_FSB_RCOMP
TRUE NB_FSB_SCOMP
TRUE NB_FSB_SCOMP_L
TRUE NB_FSB_SWING
TRUE NB_FSB_VREF
TRUE NB_RESET_L
TRUE NB_SB_SYNC_L
TRUE NB_TEST1
TRUE NB_TEST2
TRUE NB_VCCSM_LF1
TRUE NB_VCCSM_LF2
TRUE NB_VCCSM_LF3
TRUE NB_VCCSM_LF4
TRUE NB_VCCSM_LF5
TRUE NB_VCCSM_LF6
TRUE NB_VCCSM_LF7
TRUE NB_VTTLF_CAP1
TRUE NB_VTTLF_CAP2
TRUE NB_VTTLF_CAP3
TRUE ODD_PWR_EN_L
TRUE ONEWIRE_DCIN_DIV
TRUE ONEWIRE_EN
TRUE ONEWIRE_ESD
TRUE ONEWIRE_OV
TRUE ONEWIRE_PWR_EN_L
TRUE ONEWIRE_PWR_EN_L_DIV
TRUE P1V25S0NBDPLL_FB
TRUE P1V25S0NBDPLL_RF
TRUE P1V25S0_ITH
TRUE P1V25S0_ITH_RC
TRUE P1V25S0_MODE
TRUE P1V25S0_RT

TRUE P1V8S0_EN
TRUE P3V3S0_EN
TRUE P3V3S3_EN_L
TRUE P3V3TVDAC_EN_RC
TRUE P3V3TVDAC_NOISE
TRUE P3V42G3H5_BOOST
TRUE P3V42G3H_SHDN_L
TRUE P3V42G3H_SHDN_L1
TRUE P5VS0_EN
TRUE P5VS3_EN_L
TRUE PBUS_ISENSE_IN_NEG
TRUE PBUS_ISENSE_VREG
TRUE PBUS_S0_SMC_VSENSE
TRUE PBUS_SMC_VSENSE_EN_L
TRUE PCIE_CLK100M_MINI_N
TRUE PCIE_CLK100M_MINI_N_F
TRUE PCIE_CLK100M_MINI_P
TRUE PCIE_CLK100M_MINI_P_F
TRUE PCIE_E_D2R_N
TRUE PCIE_E_D2R_N_F
TRUE PCIE_E_D2R_P
TRUE PCIE_E_D2R_P_F
TRUE PCIE_E_R2D_C_N
TRUE PCIE_E_R2D_C_N_F
TRUE PCIE_E_R2D_C_P
TRUE PCIE_E_R2D_C_P_F
TRUE PCIE_E_R2D_N
TRUE PCIE_E_R2D_P
TRUE PCIE_WAKE_L
TRUE PCI_CLK33M_LPCPLUS
TRUE PCI_CLK33M_SB
TRUE PCI_CLK33M_SMC
TRUE PCI_DEVSEL_L
TRUE PCI_FRAME_L
TRUE PCI_FW_GNT_L
TRUE PCI_FW_REQ_L
TRUE PCI_IRDY_L
TRUE PCI_LOCK_L
TRUE PCI_PERR_L
TRUE PCI_PME_FW_L
TRUE PCI_REQ1_L
TRUE PCI_REQ2_L
TRUE PCI_SERR_L
TRUE PCI_STOP_L
TRUE PCI_TRDY_L
TRUE PEG_COMP
TRUE PEG_D2R_N<1>
TRUE PEG_D2R_P<1>
TRUE PEG_R2D_C_N<3..0>
TRUE PEG_R2D_C_P<3..0>
TRUE PGOOD_1V25S0
TRUE PGOOD_1V8S3
TRUE PLT_RST_BUF_L
TRUE PLT_RST_L
TRUE PM_BATLOW_L
TRUE PM_BMBUSY_L
TRUE PM_CLKRUN_L
TRUE PM_DPRSLPVR
TRUE PM_EXTTS_L<0>
TRUE PM_EXTTS_L<1>
TRUE PM_LAN_ENABLE
TRUE PM_LAN_PWRGD
TRUE PM_LATRIGGER_L
TRUE PM_PWRBTN_L
TRUE PM_RI_L
TRUE PM_RSMRST_L
TRUE PM_S4_STATE_L
TRUE PM_SB_PWROK
TRUE PM_SLP_S3_L
TRUE PM_SLP_S4_LS5V
TRUE PM_SLP_S5_L
TRUE PM_STPCPU_L
TRUE PM_STPPCI_L
TRUE PM_SUS_STAT_L
TRUE PM_SYSRST_L
TRUE PM_THRMTRIP_L
TRUE PM_THRM_L
TRUE PM_WLAN_EN_L
TRUE PM_WLAN_EN_L1
TRUE PM_WLAN_EN_L2
TRUE PM_WLAN_EN_L_SS
TRUE PP0V9_S0
TRUE PP0V9_S3
TRUE PP18V5_DCIN

TRUE PP18V5_DCIN_ONEWIRE
TRUE PP18V5_G3H
TRUE PP18V5_S5_CHGR_SW_R
TRUE PP1V05_S0
TRUE PP1V05_S0_NB_VCCPEG
TRUE PP1V25_S0
TRUE PP1V25_S0M_NB_VCCA_HPLL
TRUE PP1V25_S0_NB_DPLL
TRUE PP1V25_S0_NB_PEGPLL
TRUE PP1V25_S0_NB_PEGPLL_RC
TRUE PP1V25_S0_NB_VCCA_DPLLA
TRUE PP1V25_S0_NB_VCCA_DPLLB
TRUE PP1V5_S0
TRUE PP1V5_S0_NB_QDAC
TRUE PP1V5_S0_NB_VCCD_CRT
TRUE PP1V5_S0_NB_VCCD_QDAC
TRUE PP1V5_S0_SB_VCC1_5_B
TRUE PP1V5_S0_SB_VCCDMIPLL
TRUE PP1V5_S0_SB_VCCDMIPLL_F
TRUE PP1V5_S0_SB_VCCSATAPLL
TRUE PP1V8_S0
TRUE PP1V8_S0_ANALOG_SDVO_F
TRUE PP1V8_S0_ANALOG_TMDS_F
TRUE PP1V8_S0_NB_VCCTXLVDS
TRUE PP1V8_S0_PVCC1_TMDS_F
TRUE PP1V8_S0_PVCC2_TMDS_F
TRUE PP1V8_S0_TMDS_F
TRUE PP1V8_S3
TRUE PP1V8_S3M_NB_VCCSMCK
TRUE PP1V8_S3_NB_VCCSMCK_RC
TRUE PP3V3_A_S0
TRUE PP3V3_B_S0
TRUE PP3V3_LCDVDD_SW
TRUE PP3V3_LCDVDD_SW_F
TRUE PP3V3_S0_ANALOG_SDVO_F
TRUE PP3V3_S0_CK505_VDD48
TRUE PP3V3_S0_CK505_VDDA
TRUE PP3V3_S0_CK505_VDDA_R
TRUE PP3V3_S0_CK505_VDD_CPU_SRC
TRUE PP3V3_S0_CK505_VDD_PCI
TRUE PP3V3_S0_CK505_VDD_REF
TRUE PP3V3_S0_HDCP_F
TRUE PP3V3_S0_IMVP6_3V3
TRUE PP3V3_S0_LCD_F
TRUE PP3V3_S0_NBCORE_FOLLOW_R
TRUE PP3V3_S0_NB_CRTDAC_F
TRUE PP3V3_S0_NB_TVDAC
TRUE PP3V3_S0_NB_TVDAC_F
TRUE PP3V3_S0_NB_TVDAC_FOLLOW
TRUE PP3V3_S0_NB_VCCA_CRTDAC
TRUE PP3V3_S0_NB_VCCA_DAC_BG
TRUE PP3V3_S0_NB_VCCA_TVDACA
TRUE PP3V3_S0_NB_VCCA_TVDACB
TRUE PP3V3_S0_NB_VCCA_TVDACC
TRUE PP3V3_S0_SPVCC_TMDS_F
TRUE PP3V3_S3
TRUE PP3V3_S3_ALS_F
TRUE PP3V3_S3_AP_AUX
TRUE PP3V3_S5_AVREF_SMC
TRUE PP3V3_S5_SMC_AVCC
TRUE PP3V42G3H_SW
TRUE PP3V42_G3H
TRUE PP3V42_G3H_IPD_F
TRUE PP3V42_G3H_SMCUSBMUX_R
TRUE PP5V_S0
TRUE PP5V_S0_DVIPORT
TRUE PP5V_S0_DVIPORT_D
TRUE PP5V_S0_IMVP6_VDD
TRUE PP5V_S0_KBDLED_F
TRUE PP5V_S0_SB_V5REF
TRUE PP5V_S0_TMDS_FUSE
TRUE PP5V_S3
TRUE PP5V_S3_CAMERA_F
TRUE PP5V_S3_TOPCASE_F
TRUE PP5V_S3_USB2_EXTA
TRUE PP5V_S3_USB2_EXTA_F
TRUE PP5V_S5
TRUE PP5V_S5_SB_V5REF_SUS
TRUE PPBUS_G3H
TRUE PPBUS_R_G3H
TRUE PPDCIN_G3H
TRUE PPDCIN_G3H_R
TRUE PPVBATT_G3H_R

TRUE PPVBAT_G3H_CHGR_OUT
TRUE PPVBAT_G3H_CHGR_REG
TRUE PPVBAT_G3H_CHGR_REG_0
TRUE PPVBAT_G3H_CHRGR_REG_0
TRUE PPVCORE_S0_CPU
TRUE PPVCORE_S0_NB_GFX
TRUE PPVDCIN_G3H_PRE
TRUE PPVDCIN_G3H_PRE2
TRUE PPVDCIN_G3H_PRE_0
TRUE PPVDCIN_G3H_PRE_R
TRUE PPVIN_S5_IMVP6_VIN
TRUE PPVOUT_S0_LCDBKLT
TRUE PPVOUT_S0_LCDBKLT_SW
TRUE RSMRST_PWRGD
TRUE RSVD_EXTGPU_LVDS_EN
TRUE RUNSS_GATE_D
TRUE RUNSS_GATE_D_L
TRUE S0PWRGD_1V8_DIV
TRUE S0PWRGD_3V3_DIV
TRUE S0PWRGD_5V_DIV
TRUE S0SEQ_BEGIN
TRUE SATA_B_DET_L
TRUE SB_A20GATE
TRUE SB_CLINK_VREF0
TRUE SB_CLINK_VREF1
TRUE SB_CLK100M_DMI_N
TRUE SB_CLK100M_DMI_P
TRUE SB_CLK14P3M_TIMER
TRUE SB_CLK48M_USBCTLR
TRUE SB_CRT_TVOUT_MUX_L
TRUE SB_GPIO10_CL1
TRUE SB_GPIO18
TRUE SB_GPIO30
TRUE SB_GPIO36
TRUE SB_GPIO40

TRUE SB_INTVRMEN
TRUE SB_LAN100_SLP
TRUE SB_RCIN_L
TRUE SB_RTC_RST_L
TRUE SB_RTC_X1
TRUE SB_RTC_X1_R
TRUE SB_RTC_X2
TRUE SB_SLOAD
TRUE SB_SM_INTRUDER_L
TRUE SB_SPKR
TRUE SDVO_CTRLCLK
TRUE SDVO_CTRLDATA
TRUE SMBUS_SB_ME_SCL
TRUE SMBUS_SB_ME_SDA
TRUE SMBUS_SB_SCL
TRUE SMBUS_SB_SDA
TRUE SMBUS_SMC_0_S0_SCL
TRUE SMBUS_SMC_0_S0_SDA
TRUE SMBUS_SMC_A_S3_SCL
TRUE SMBUS_SMC_A_S3_SDA
TRUE SMBUS_SMC_BSA_SCL
TRUE SMBUS_SMC_BSA_SDA
TRUE SMBUS_SMC_B_S3_SCL
TRUE SMBUS_SMC_B_S3_SDA
TRUE SMBUS_SMC_MGMT_SCL
TRUE SMBUS_SMC_MGMT_SDA
TRUE SMB_AIRPORT_CONN_CLK
TRUE SMB_AIRPORT_CONN_DATA
TRUE SMC_ACIN_VSENSE
TRUE SMC_ADAPTER_EN
TRUE SMC_BATTPACK_STAT
TRUE SMC_BATT_CHG_EN
TRUE SMC_BATT_ISENSE
TRUE SMC_BC_ACOK
TRUE SMC_BC_ACOK_ONEWIRE_R

TRUE SMC_BS_ALRT_L
TRUE SMC_CASE_OPEN
TRUE SMC_DCIN_ISENSE
TRUE SMC_EXTAL
TRUE SMC_FAN_0_CTL
TRUE SMC_FAN_0_TACH
TRUE SMC_GPU_ISENSE
TRUE SMC_GPU_VSENSE
TRUE SMC_KBC_MDE
TRUE SMC_LID
TRUE SMC_LRESET_L
TRUE SMC_MANUAL_RST_L
TRUE SMC_MANUAL_RST_L1
TRUE SMC_MD1
TRUE SMC_NMI
TRUE SMC_ODD_DETECT
TRUE SMC_ONOFF_H
TRUE SMC_ONOFF_L
TRUE SMC_PBUS_ISENSE
TRUE SMC_PBUS_VSENSE
TRUE SMC_PF3
TRUE SMC_PM_G2_EN
TRUE SMC_PROCHOT
TRUE SMC_PROCHOT_3_3_L
TRUE SMC_RESET_L
TRUE SMC_RUNTIME_SCI_L
TRUE SMC_RX_L
TRUE SMC_SMS_INT
TRUE SMC_SUS_CLK
TRUE SMC_SYS_KBDLED
TRUE SMC_SYS_LED
TRUE SMC_TCK
TRUE SMC_TDI
TRUE SMC_TDO
TRUE SMC_THRMTRIP

TRUE SMC_TMS
TRUE SMC_TRST_L
TRUE SMC_TX_L
TRUE SMC_VCL
TRUE SMC_WAKE_SCI_L
TRUE SMC_XTAL
TRUE SMS_MOT_EN
TRUE SMS_ONOFF_L
TRUE SMS_X_AXIS
TRUE SMS_Y_AXIS
TRUE SMS_Z_AXIS
TRUE SPI_A_INT_CLK
TRUE SPI_A_INT_HOLD_L
TRUE SPI_A_INT_SI
TRUE SPI_A_INT_WP_L
TRUE SPI_A_SCLK_R
TRUE SPI_A_SI_R
TRUE SPI_A_SO_R
TRUE SPI_CE_L<0>
TRUE SPI_CE_R_L<0>
TRUE SPI_CE_R_L<1>
TRUE SPI_EXT_A_SCLK_R
TRUE SPI_EXT_A_SI_R
TRUE SPI_EXT_CE_L<0>
TRUE SPI_INT_CE_L<0>
TRUE SPI_SCLK_R
TRUE SPI_SI_R
TRUE SPI_SO
TRUE SST8051_DDC_CLK
TRUE SST8051_DDC_DATA
TRUE SST8051_DDC_EN
TRUE SST8051_DVI_HOTPLUG_DET
TRUE SST8051_EA_L
TRUE SST8051_P25_AUDIO_CONFIG
TRUE SST8051_P34_AUDIO_CONFIG

TRUE SST8051_RST
TRUE SST8051_SW_RESET_L
TRUE SST8051_UPDATE_L
TRUE SST8051_XTAL1
TRUE SST8051_XTAL2
TRUE SUS_CLK_SB
TRUE SYS_ONEWIRE
TRUE SYS_ONEWIRE_BILAT
TRUE THRM_CPU_ALERT_L
TRUE THRM_CPU_DXN
TRUE THRM_CPU_DXP
TRUE THRM_CPU_THM_L
TRUE TMDS_DDC_SCL
TRUE TMDS_DDC_SDA
TRUE TMDS_EXT_RES
TRUE TMDS_EXT_SWING
TRUE TMDS_HTPLG
TRUE TMDS_HTPLG_R
TRUE TMDS_HW_RESET_L
TRUE TMDS_INT_N
TRUE TMDS_INT_P
TRUE TMDS_LINT_L
TRUE TMDS_LSCL
TRUE TMDS_LSDA
TRUE TMDS_SDB_N
TRUE TMDS_SDB_P
TRUE TMDS_SDC_N
TRUE TMDS_SDC_P
TRUE TMDS_SDG_N
TRUE TMDS_SDG_P
TRUE TMDS_SDR_N
TRUE TMDS_SDR_P
TRUE TMDS_SW_RESET_L
TRUE TMDS_TX<2..0>
TRUE TMDS_TXCLK

TRUE TMDS_TX_CLK_N
TRUE TMDS_TX_CLK_P
TRUE TMDS_TX_CONN_CLK_N
TRUE TMDS_TX_CONN_CLK_P
TRUE TMDS_TX_CONN_N<2..0>
TRUE TMDS_TX_CONN_P<2..0>
TRUE TMDS_TX_N<2..0>
TRUE TMDS_TX_P<2..0>
TRUE TV_A_DAC
TRUE TV_B_DAC
TRUE TV_C_DAC
TRUE TV_DCONSEL<1>
TRUE USB2_AIRPORT_N
TRUE USB2_AIRPORT_N_F
TRUE USB2_AIRPORT_P
TRUE USB2_AIRPORT_P_F
TRUE USB2_CAMERA_F_N
TRUE USB2_CAMERA_F_P
TRUE USB2_CAMERA_N
TRUE USB2_CAMERA_P
TRUE USB2_EXTA_F_N
TRUE USB2_EXTA_F_P
TRUE USB2_EXTA_N
TRUE USB2_EXTA_P
TRUE USB2_MUXED_EXTA_N
TRUE USB2_MUXED_EXTA_P
TRUE USB2_WSPRING_N
TRUE USB2_WSPRING_P
TRUE USB_DEBUGPRT_EN_L
TRUE USB_EXTC_OC_L
TRUE USB_EXTD_OC_L
TRUE USB_IR_N
TRUE USB_IR_P
TRUE USB_RBIAS
TRUE VCCCL1_5V

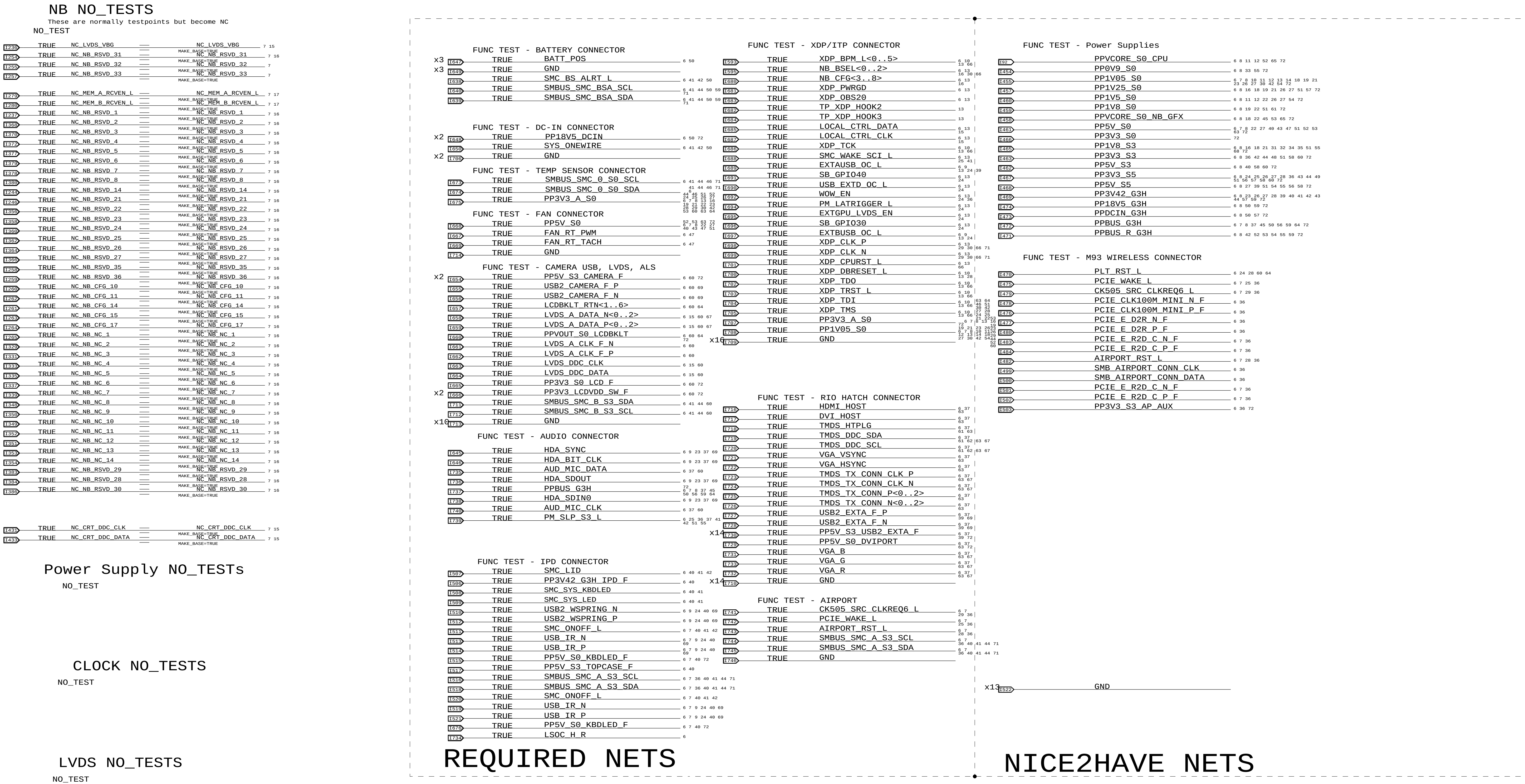
TRUE VGA_B
TRUE VGA_G
TRUE VGA_HSYNC
TRUE VGA_R
TRUE VGA_VSYNC
TRUE VR_PWRGD_CK505
TRUE VR_PWRGD_CK505_L
TRUE VR_PWRGD_DELAY
TRUE WOL_EN
TRUE WOW_EN
TRUE XDP_BPM_L<0>
TRUE XDP_BPM_L<1>
TRUE XDP_BPM_L<2>
TRUE XDP_BPM_L<3>
TRUE XDP_BPM_L<4>
TRUE XDP_BPM_L<5>
TRUE XDP_CLK_N
TRUE XDP_CLK_P
TRUE XDP_CPURST_L
TRUE XDP_DBRESET_L
TRUE XDP_OBS20
TRUE XDP_PWRGD
TRUE XDP_TCK
TRUE XDP_TDI
TRUE XDP_TDO
TRUE XDP_TMS
TRUE XDP_TRST_L

ICT Test Points

APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. 8.0.0
SCALE NONE | SHT 6 OF 73

Functional Test Points



Functional Test and No-Tests

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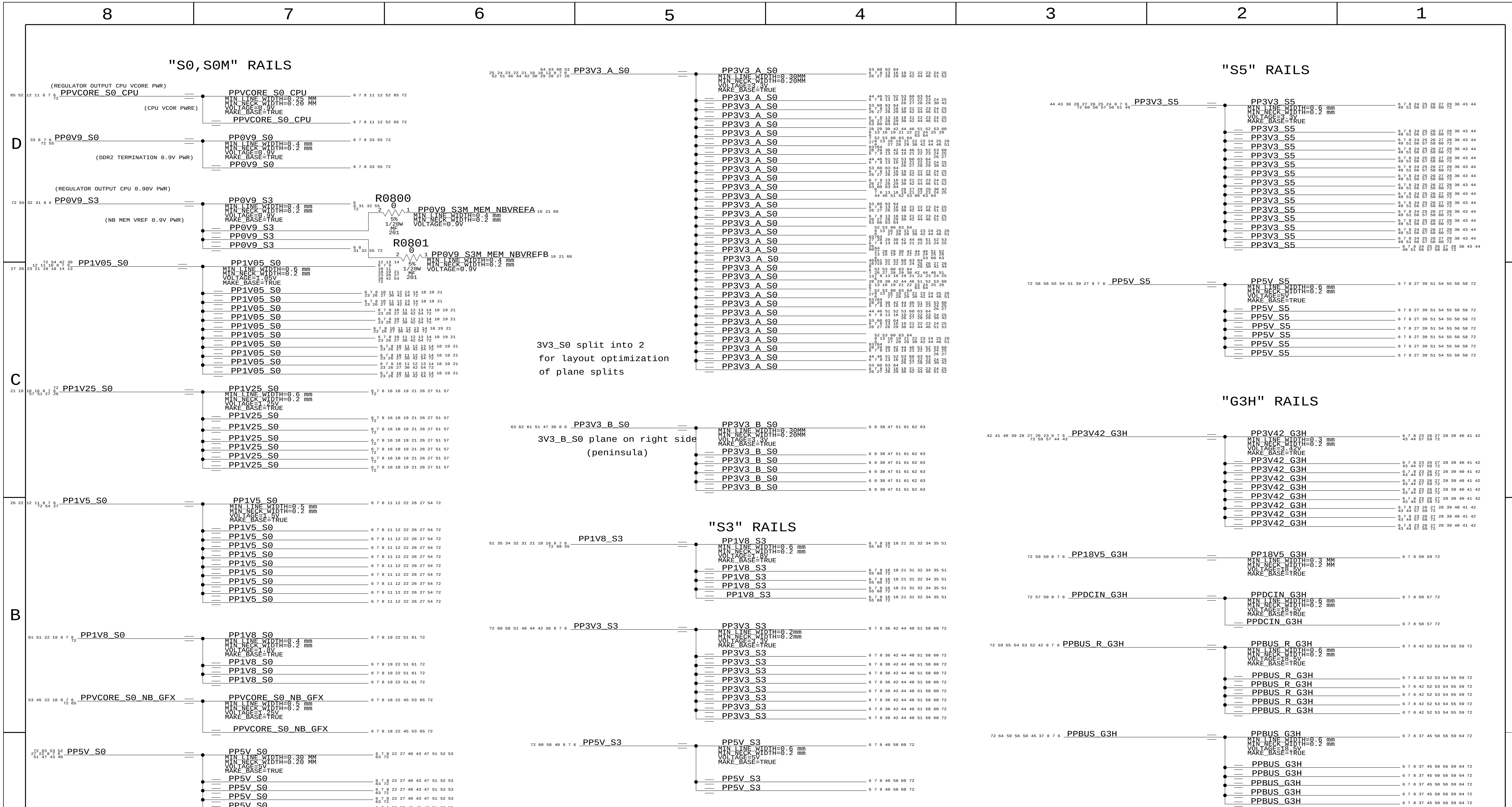
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 7 OF 73	



Power Aliases

SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

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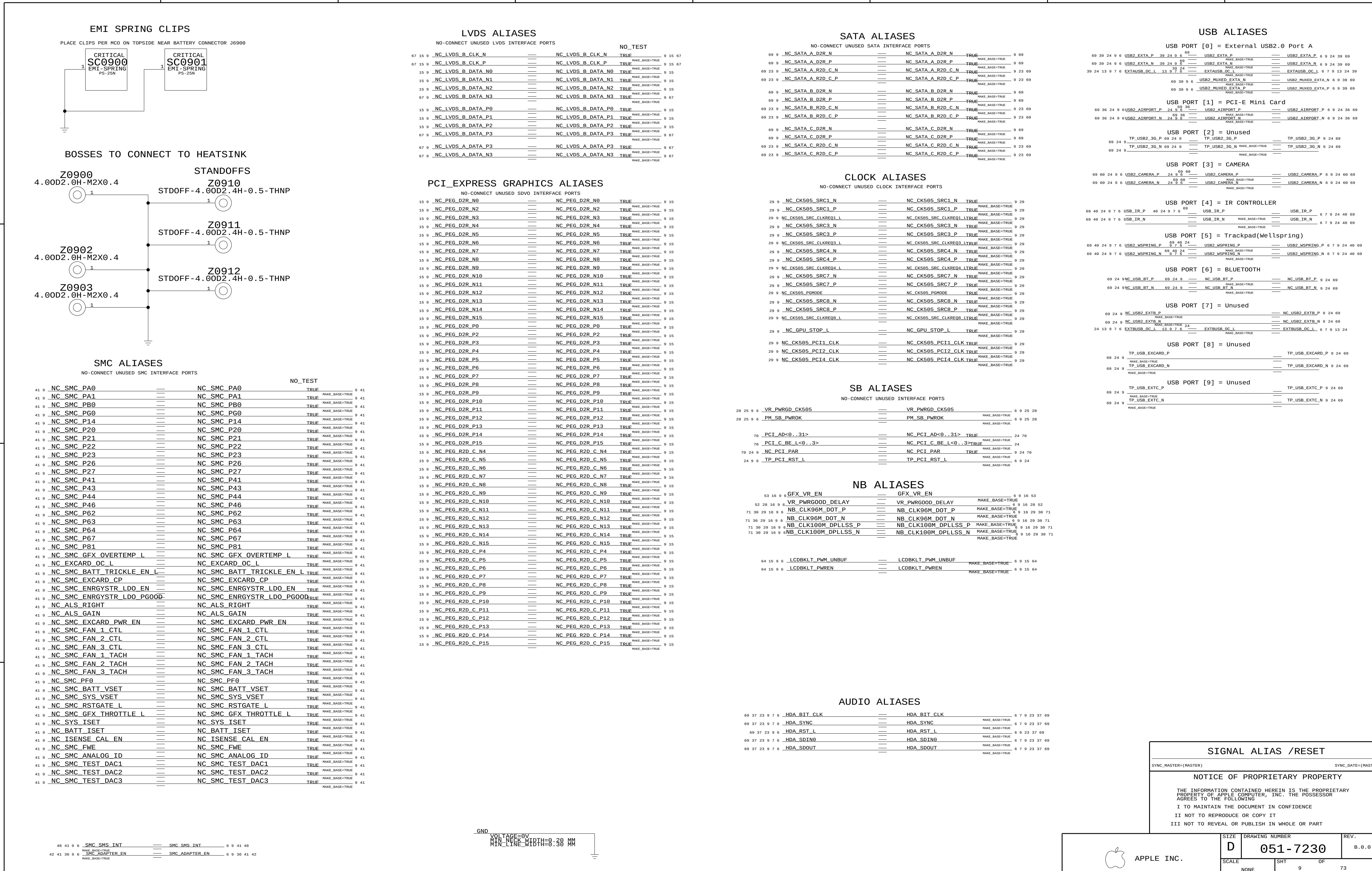
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 8	OF 73



SIGNAL ALIAS /RESET

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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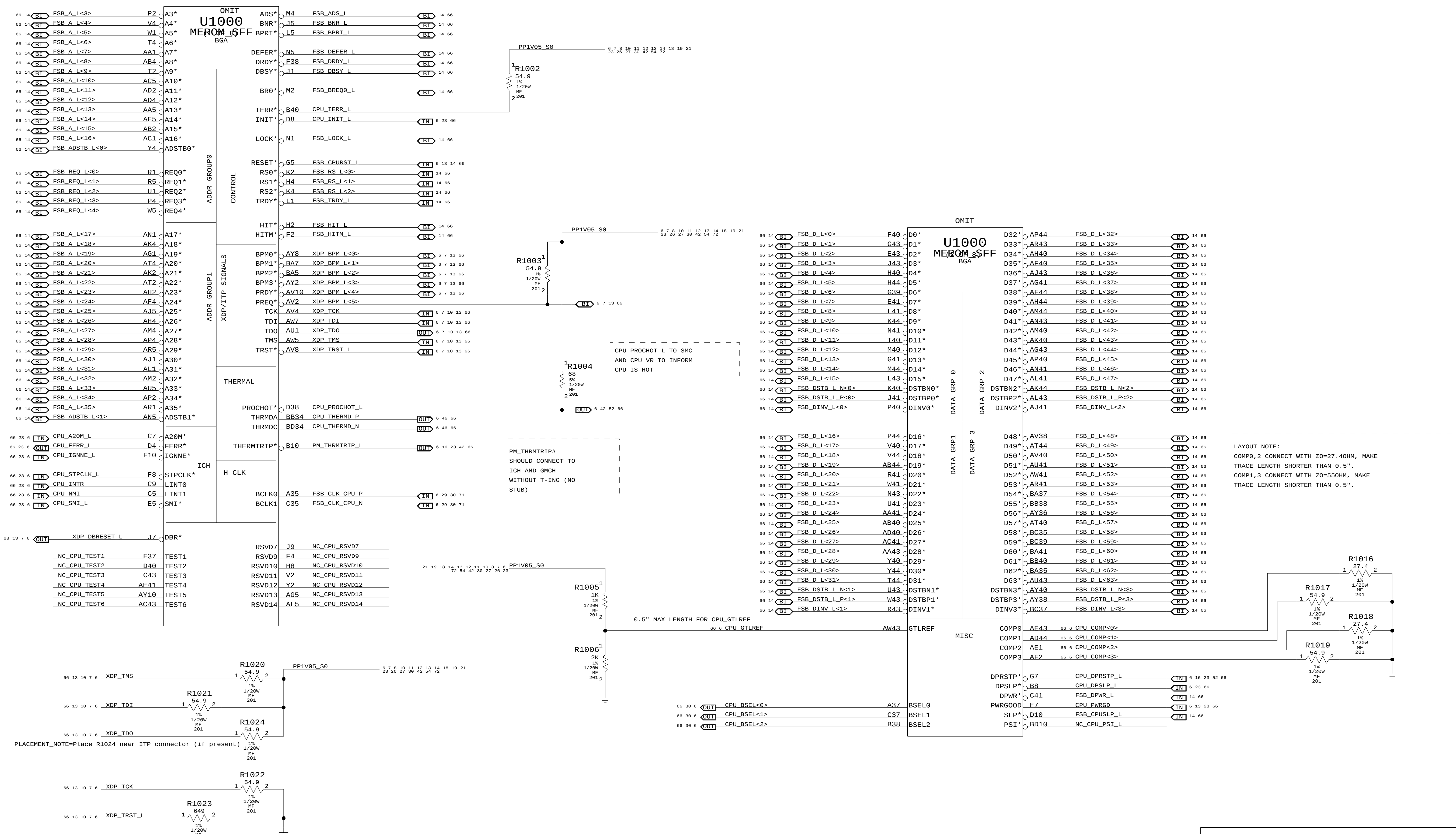
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 9	OF 73



CPU FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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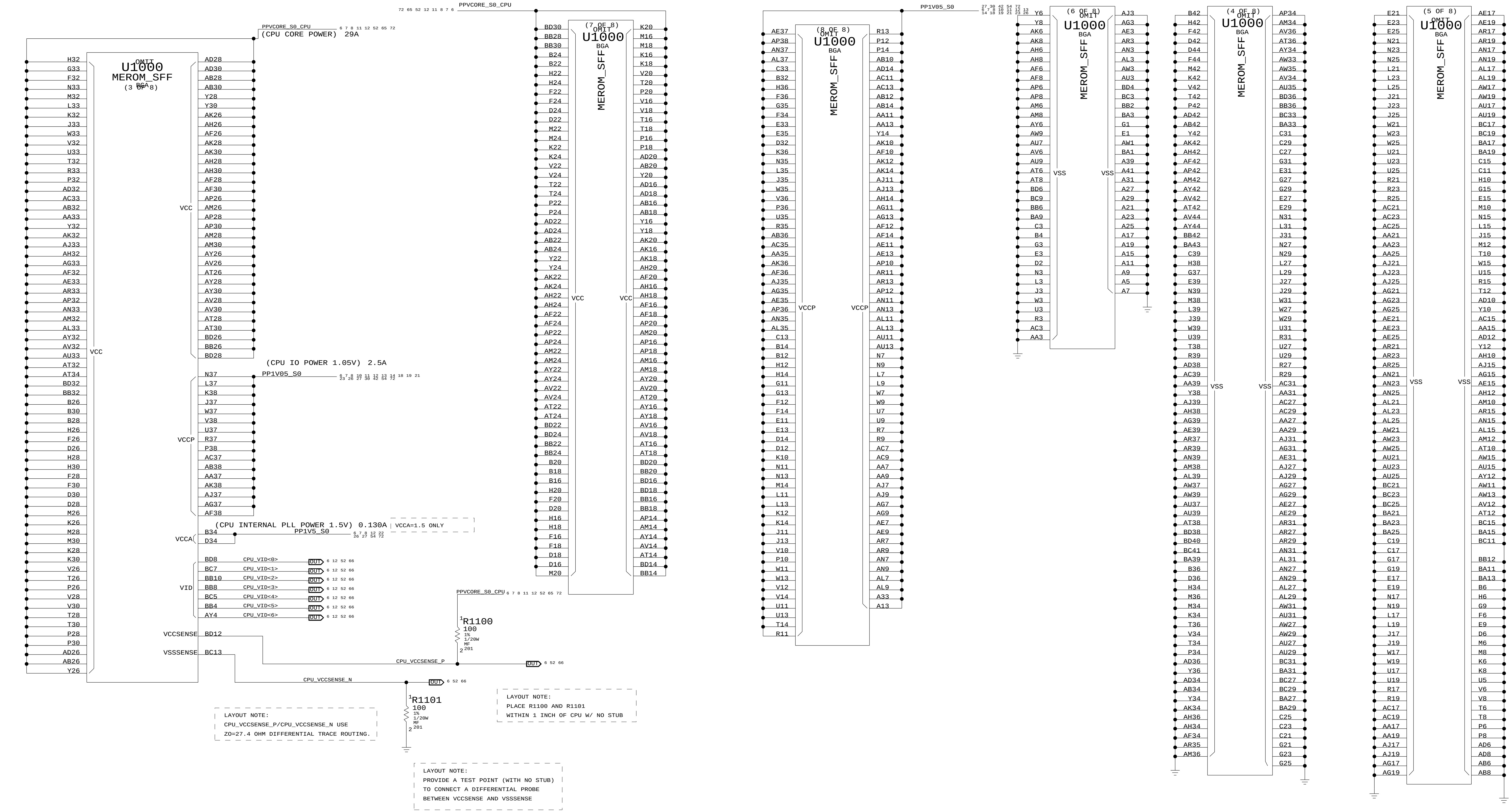
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 10 OF 73	



CPU Power & Ground

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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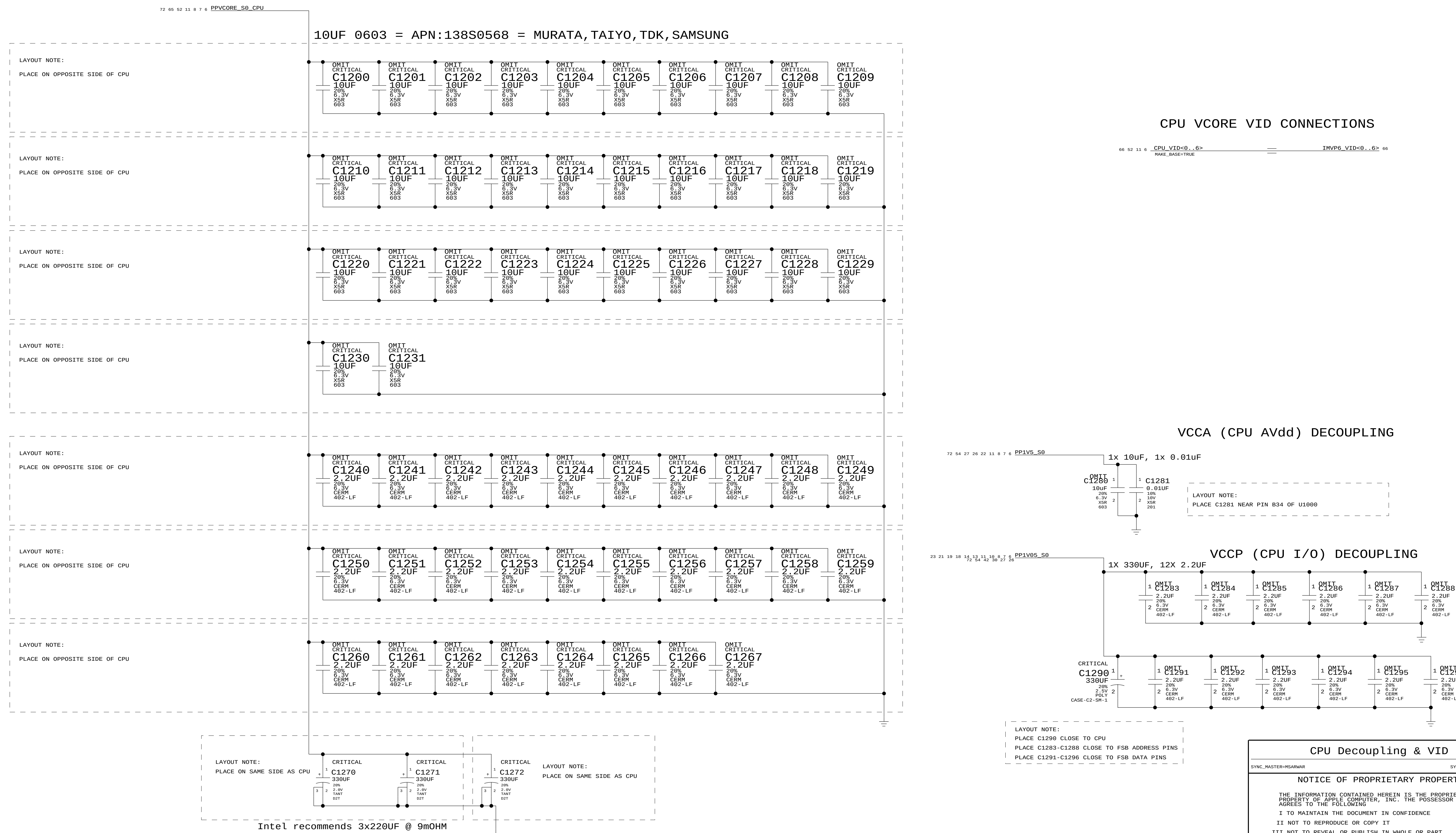
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 11	OF 73

CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 1uF 0402

Intel recommends 32+28 but is evaluating 24+24

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG



CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

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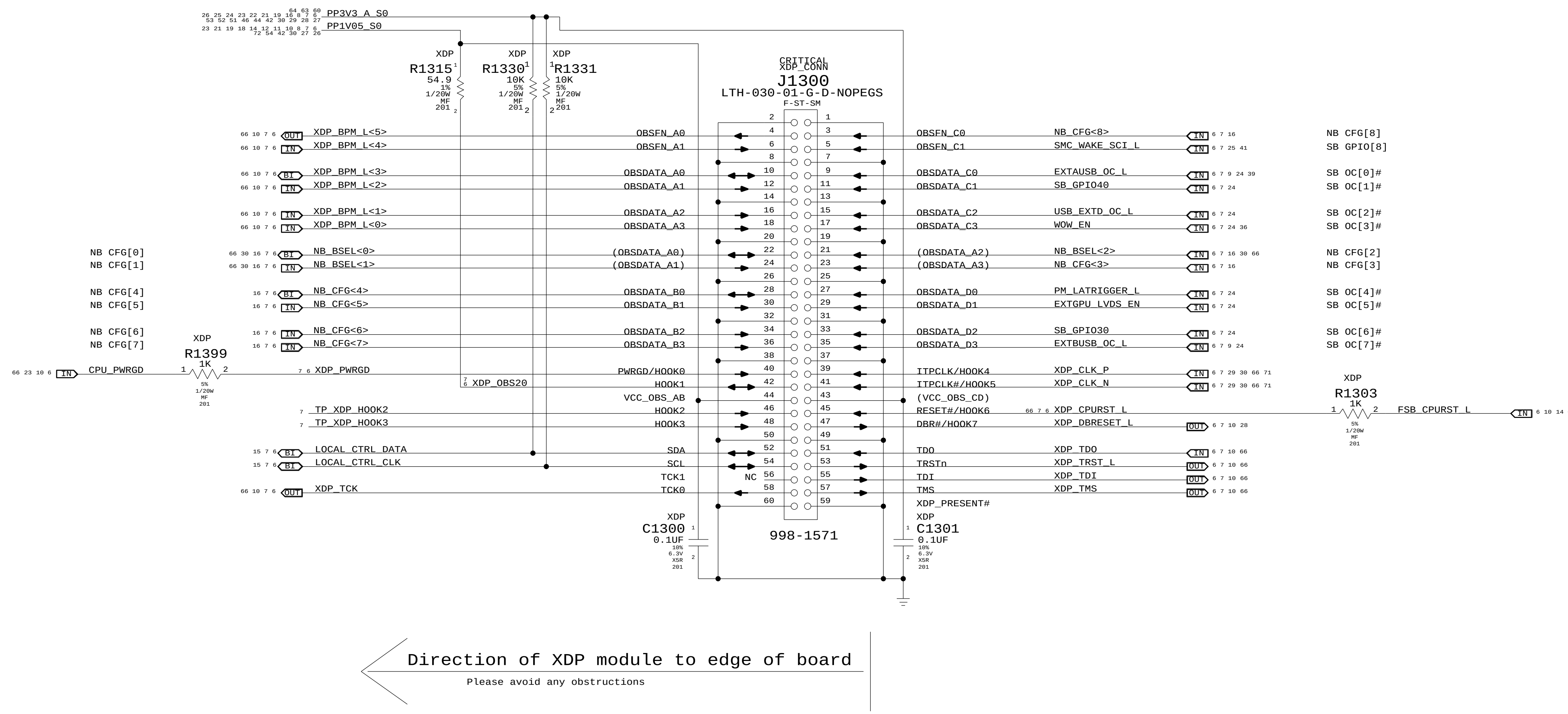
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 12 OF 73	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



eXtended Debug Port (XDP)

SYNC_MASTER=M75 SYNC_DATE=01/24/2007

NOTICE OF PROPRIETARY PROPERTY

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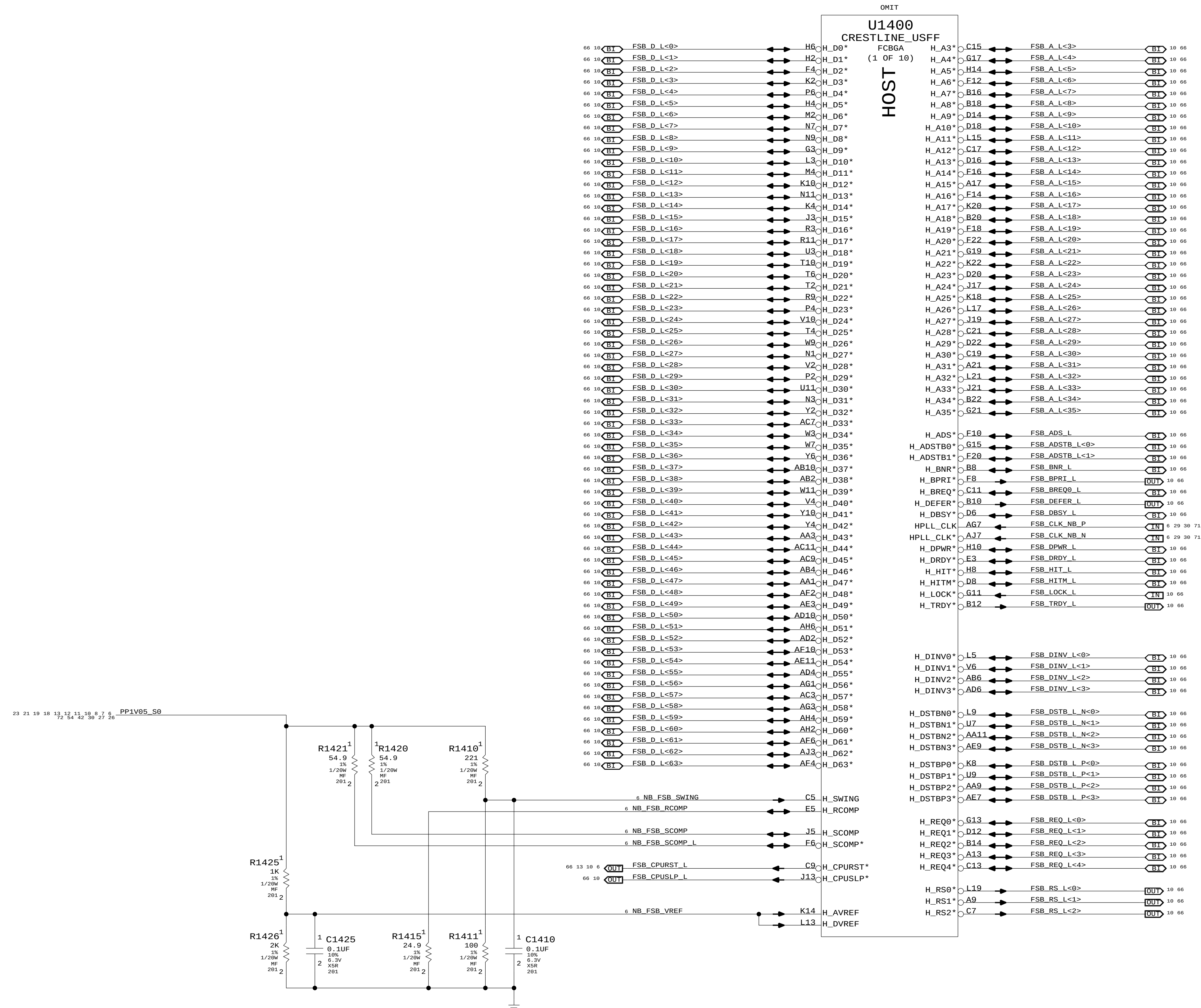
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE | SHT 13 OF 73



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 14 OF 73	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

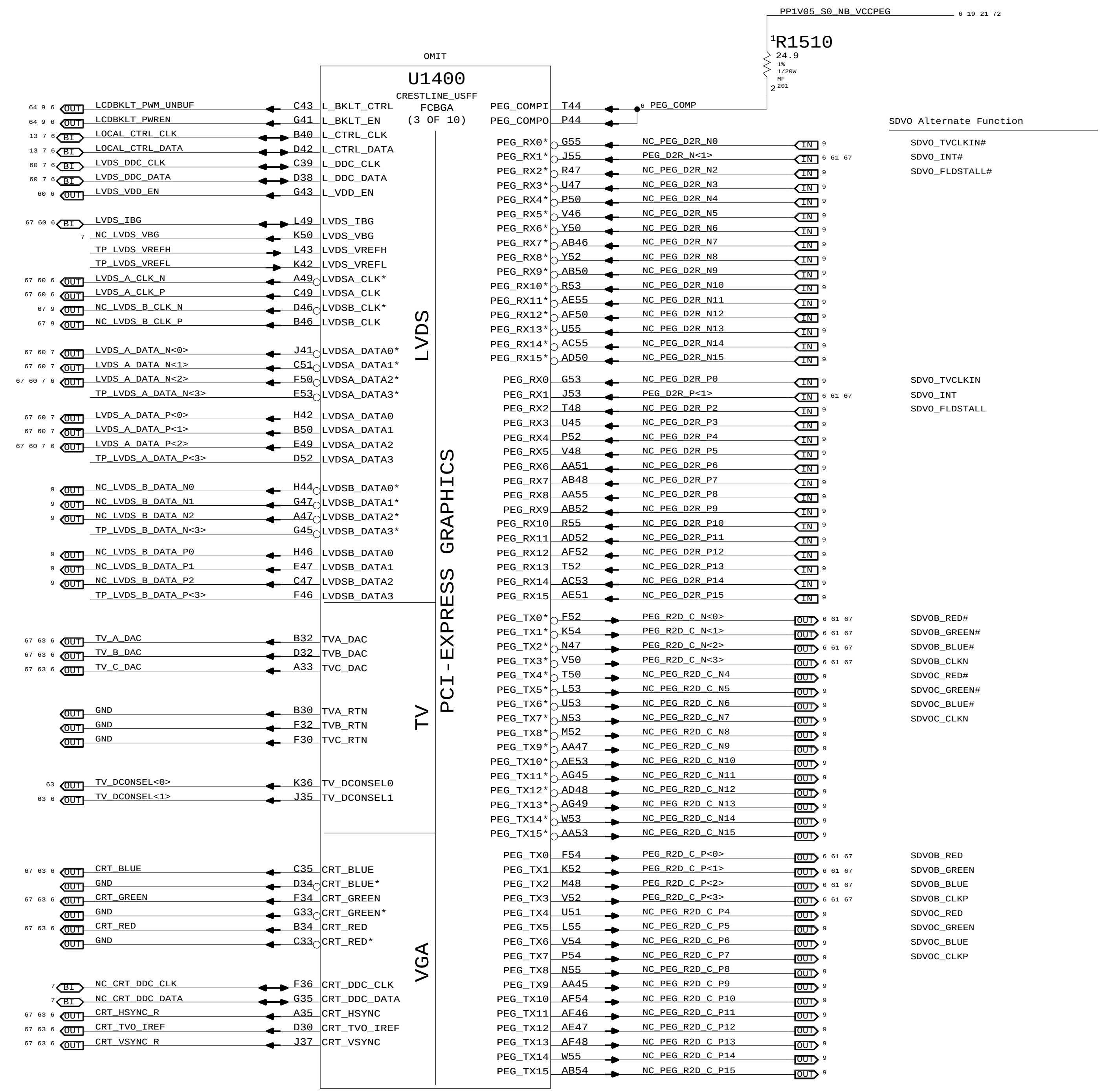
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

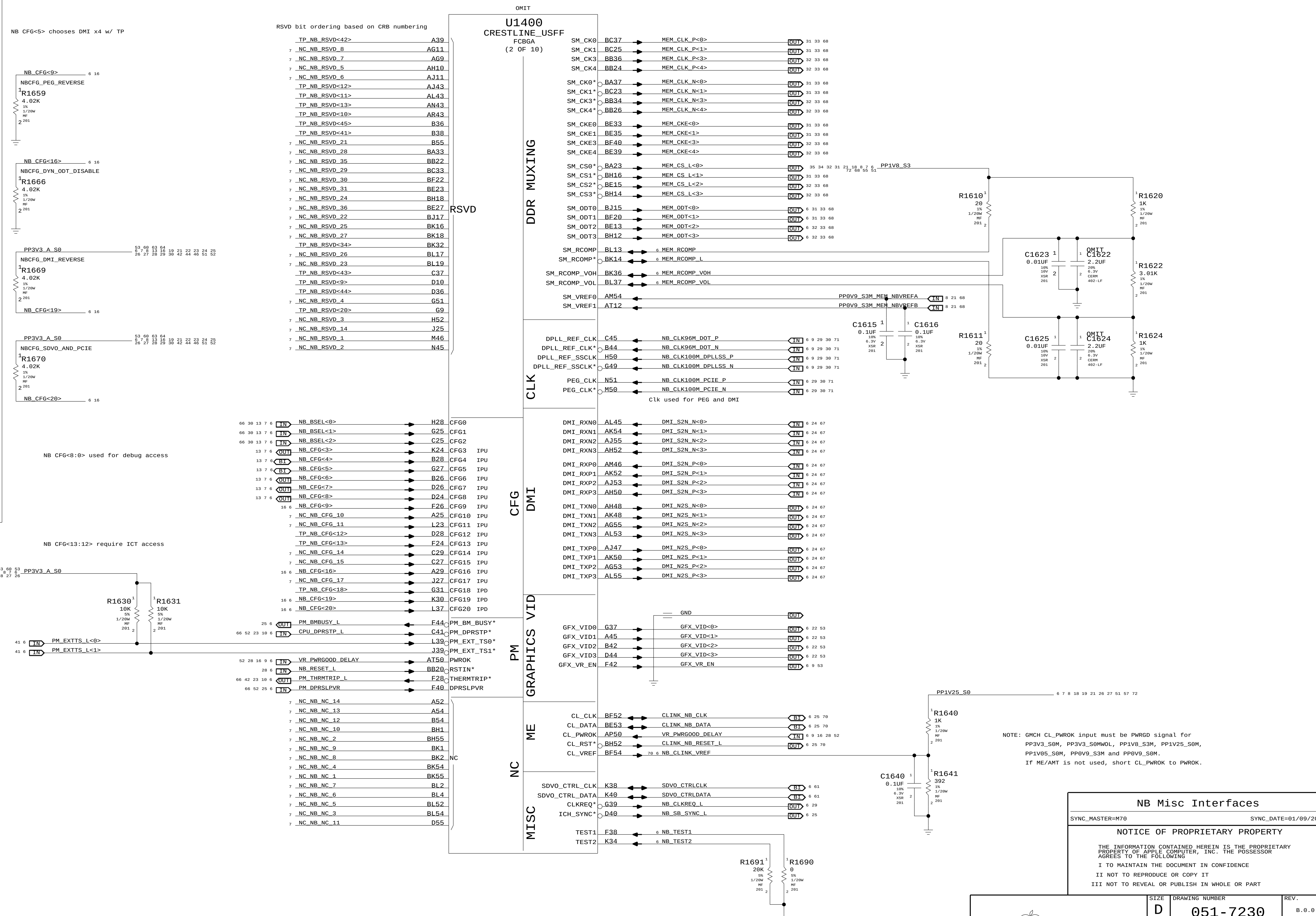
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 15 OF 73

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation



NB Misc Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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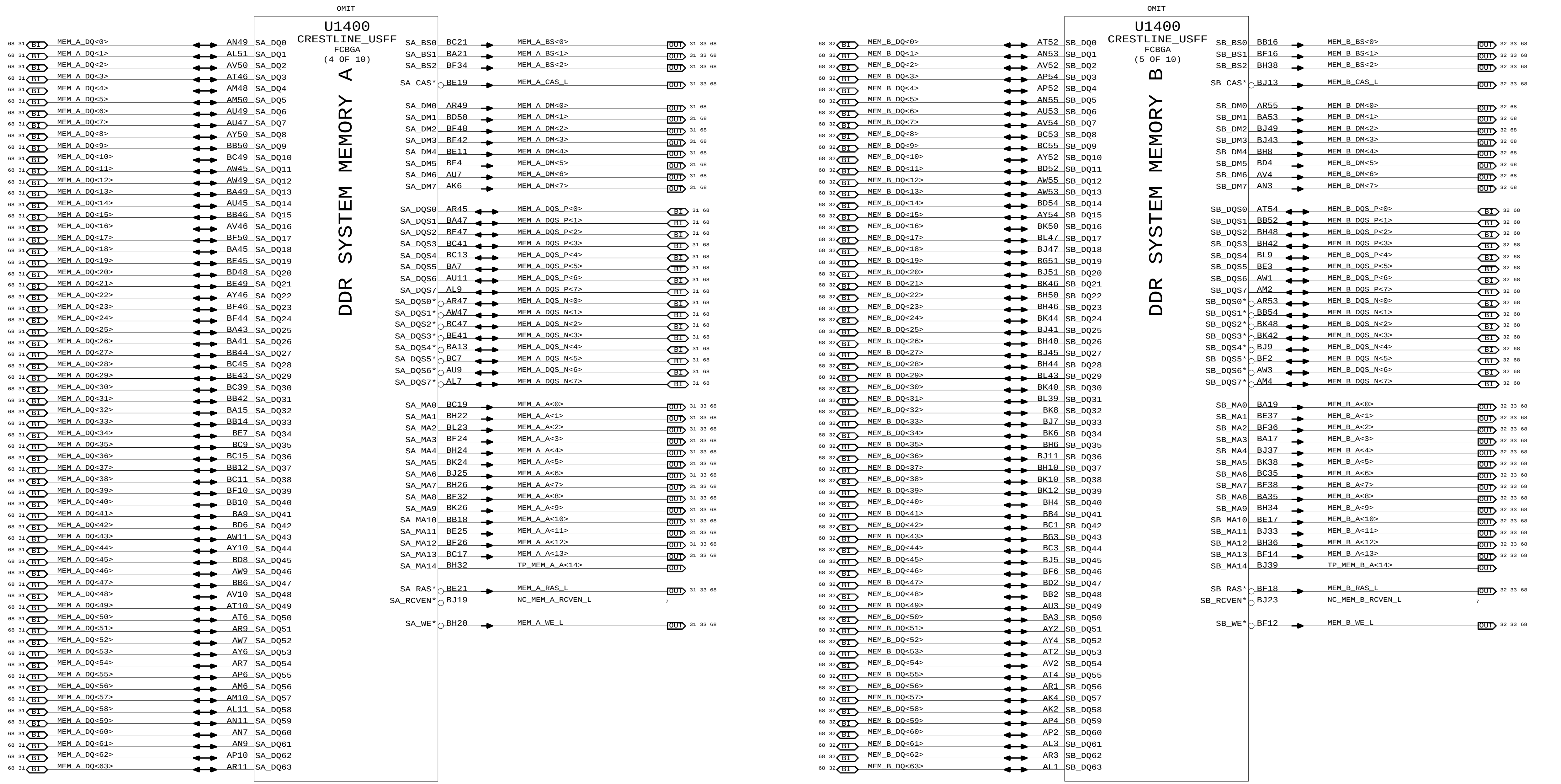
SCALE NONE SHT 16 OF 73



NB DDR2 Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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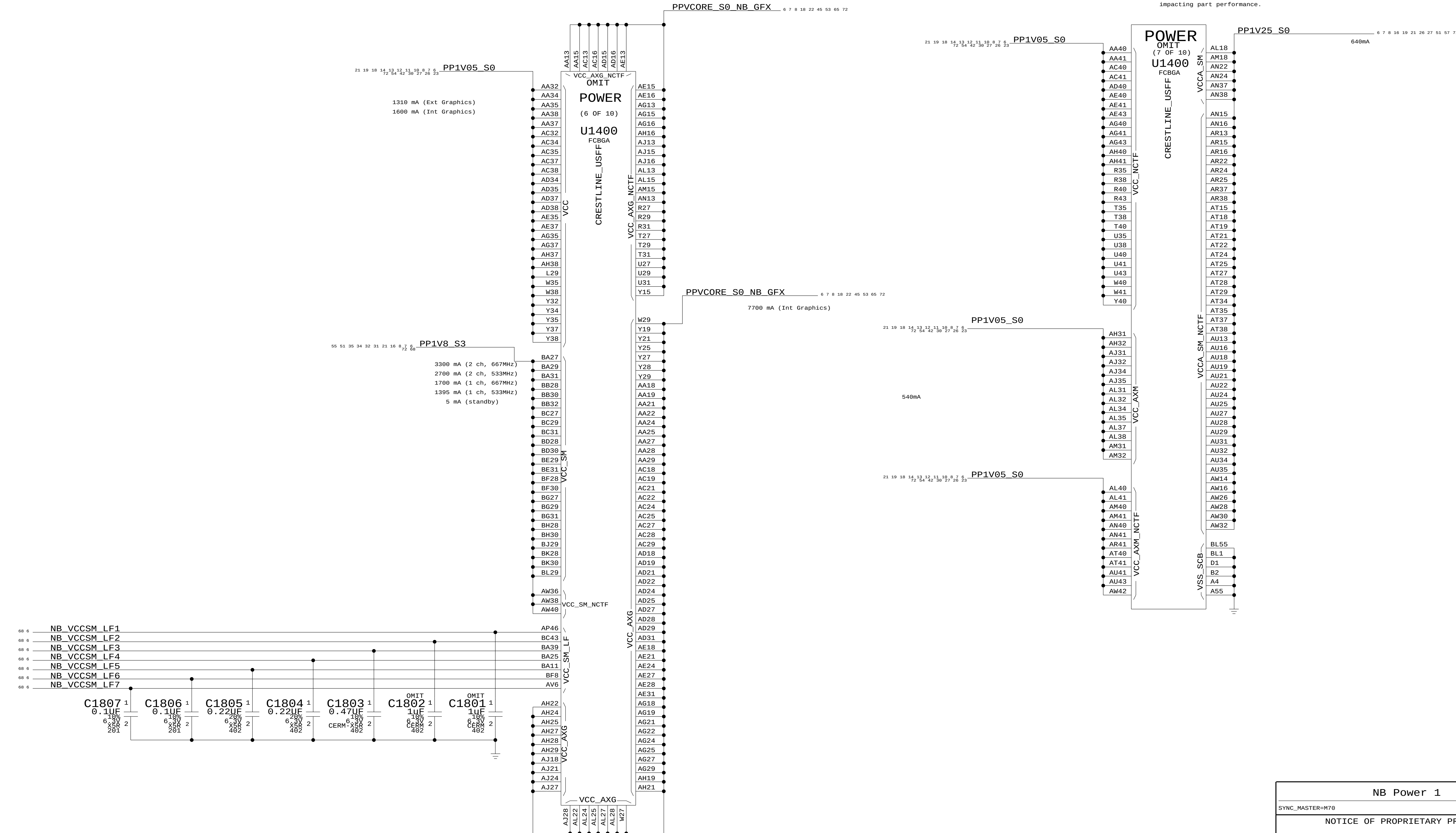
D	051-7230	8.0.0
SCALE NONE	SHT 17	OF 73

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.



Current numbers from Crestline EDS, doc #21749.

NB Power 1

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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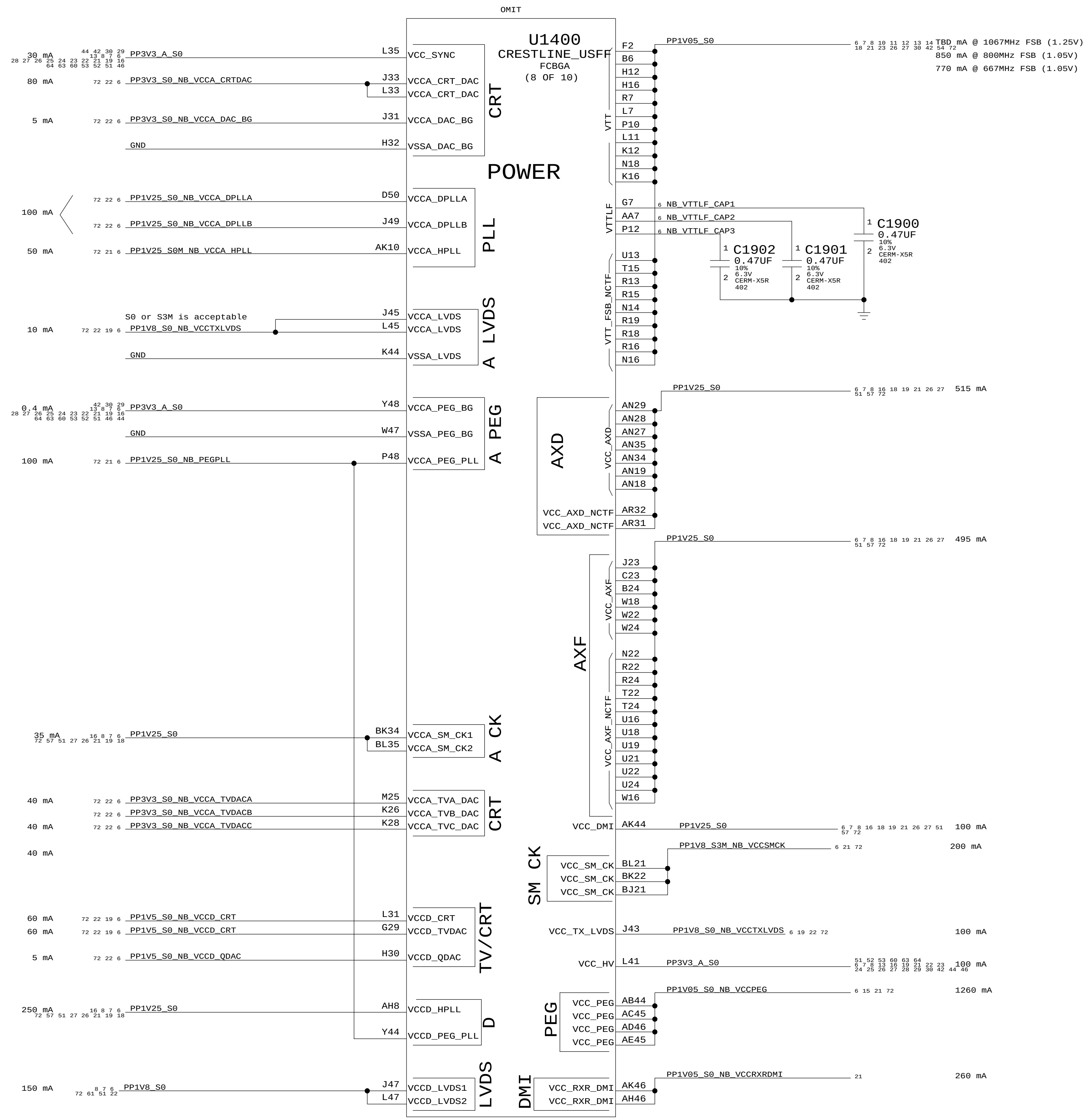
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE	SHT	OF
NONE	18	73



Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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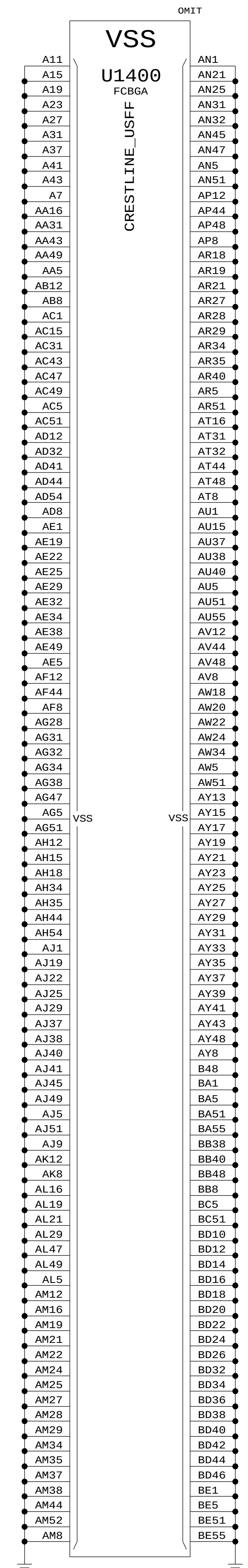
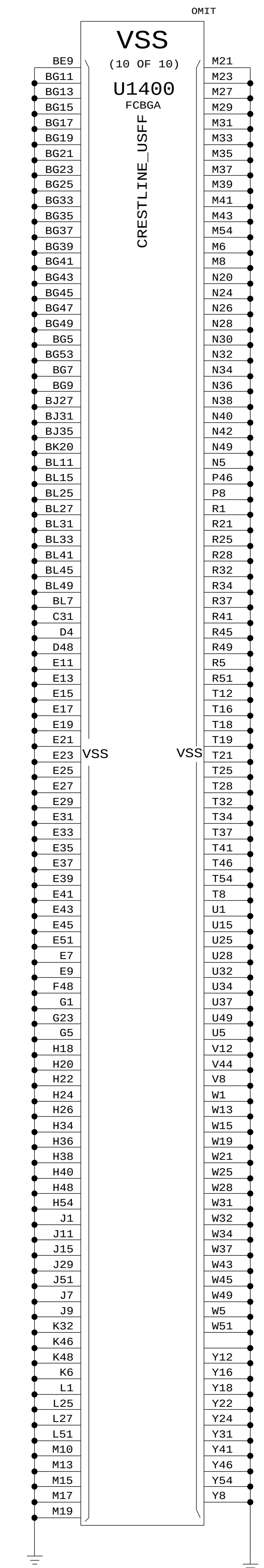
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 19	OF 73



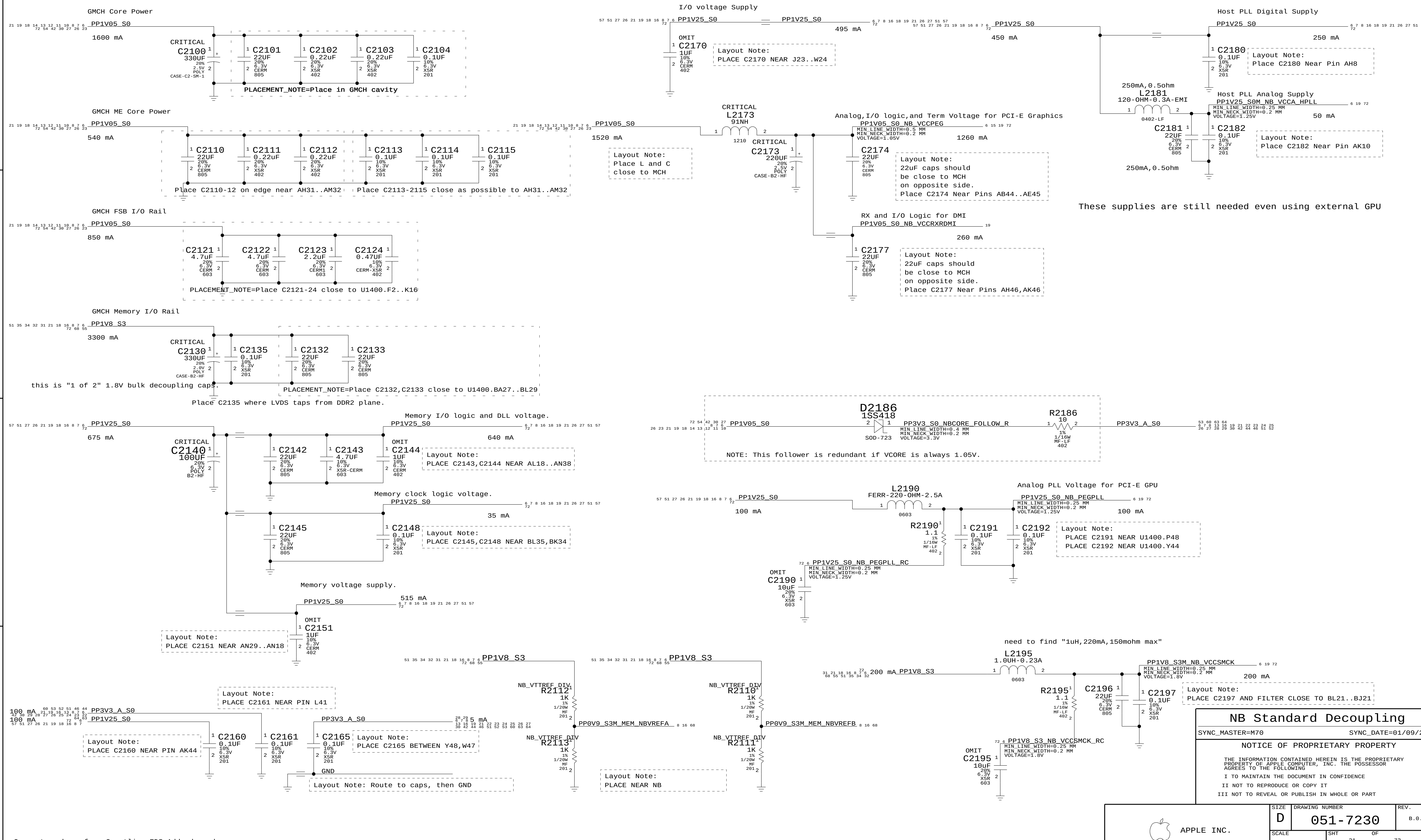


NB Grounds

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 20	OF 73

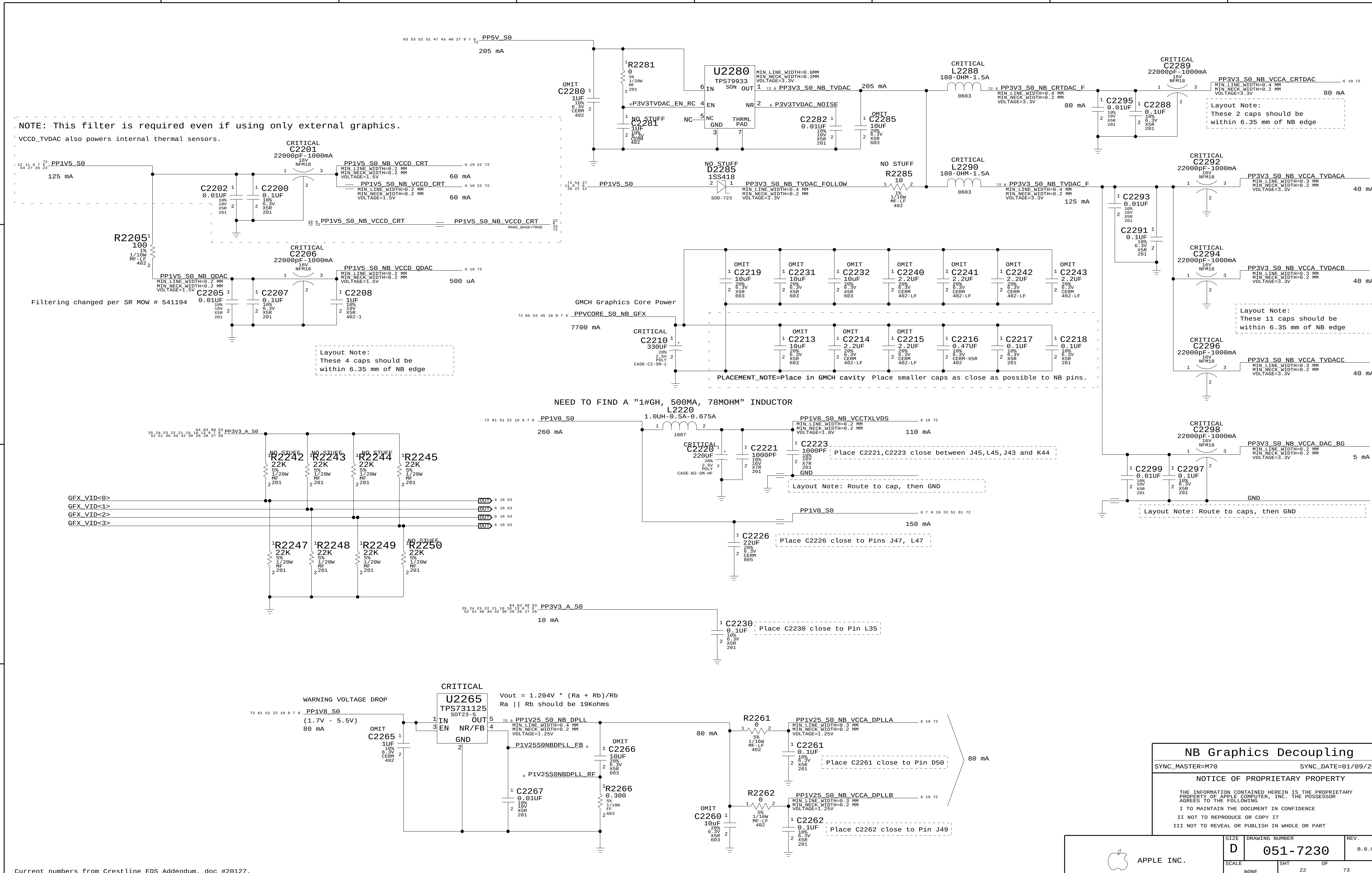


NB Standard Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 21	OF 73



NB Graphics Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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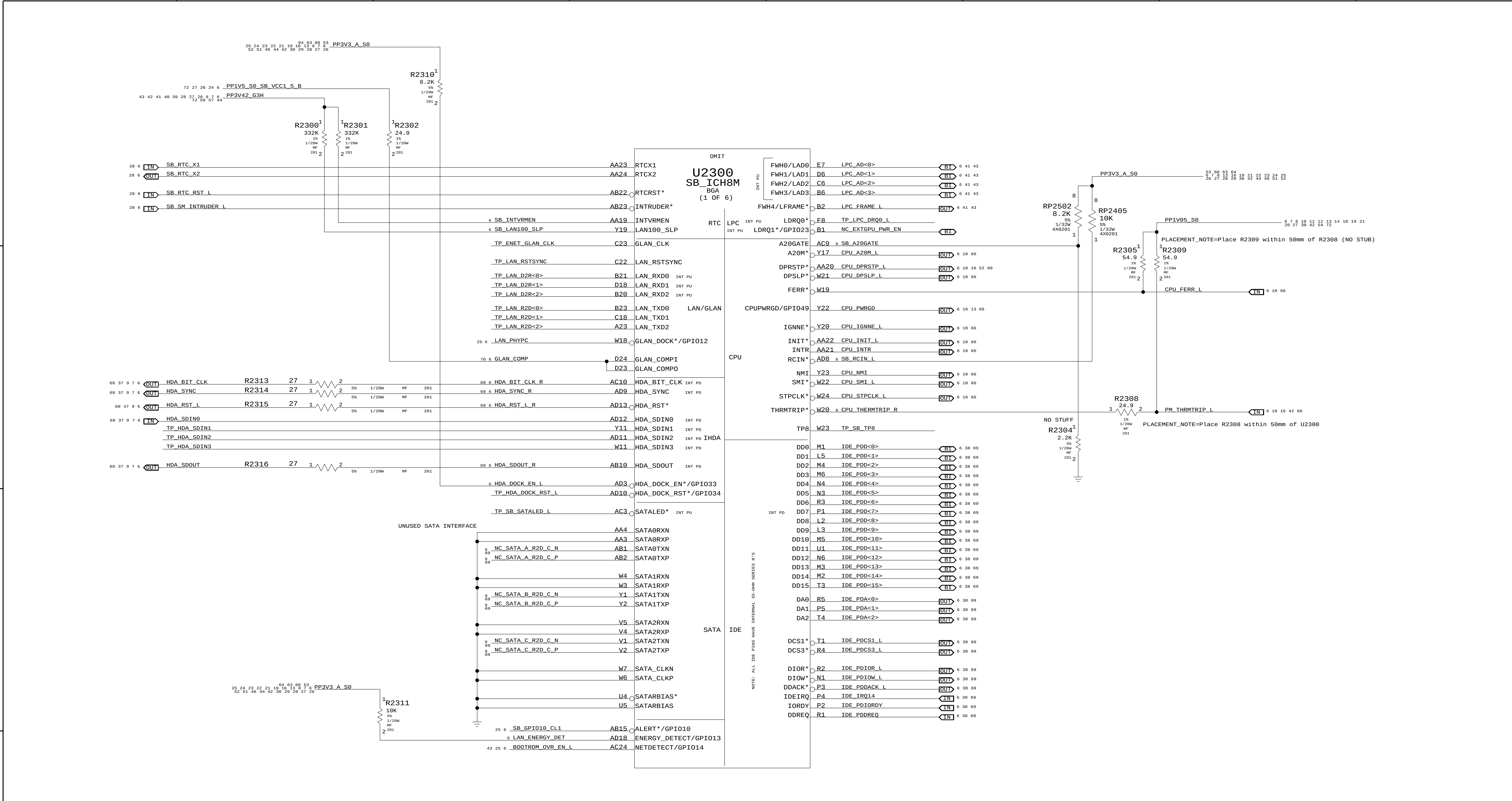
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 22	OF 73



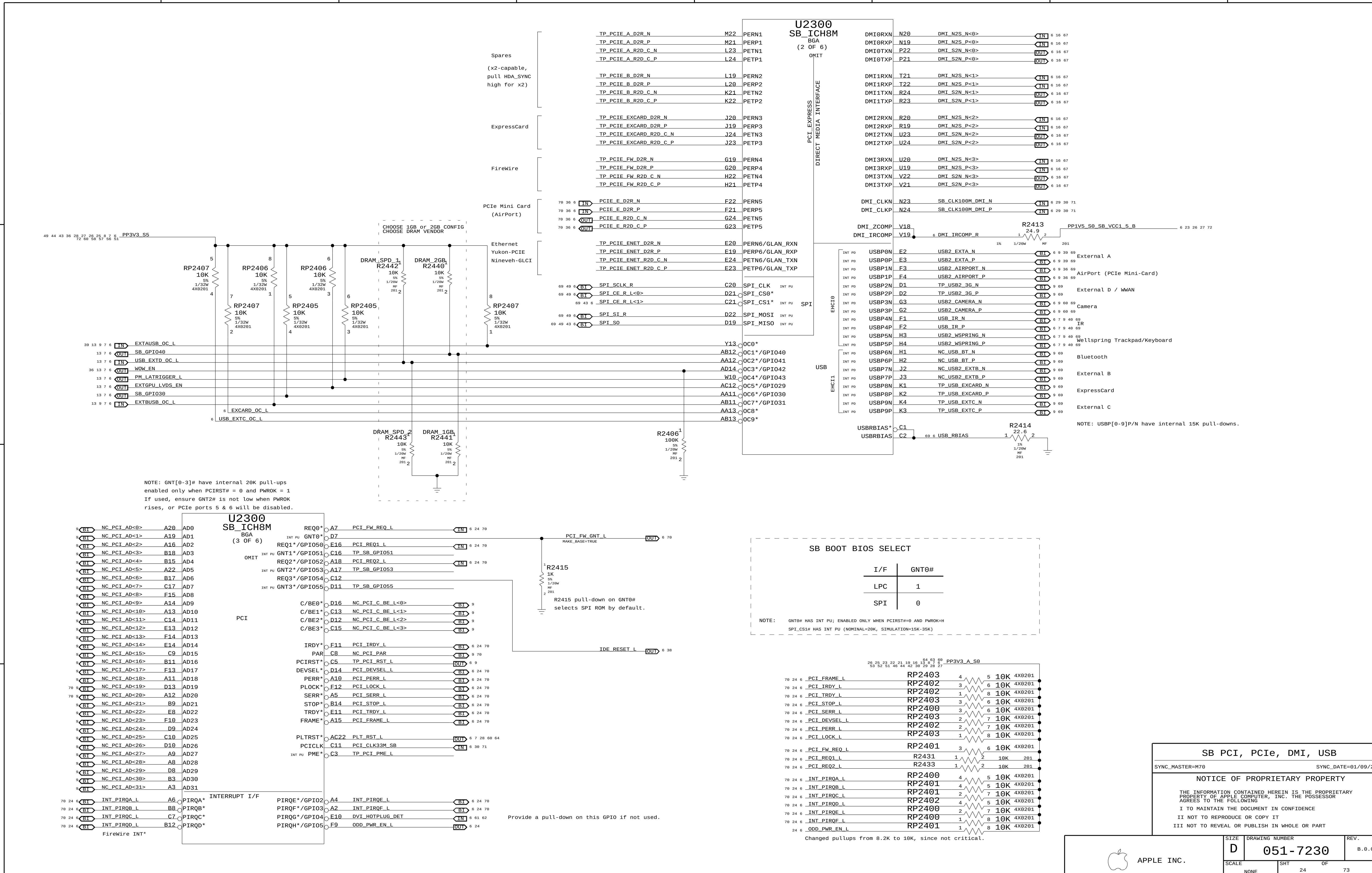
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 23 OF 73	



I/F	GNT0#
LPC	1
SPI	0

SB PCI, PCIe, DMI, USB

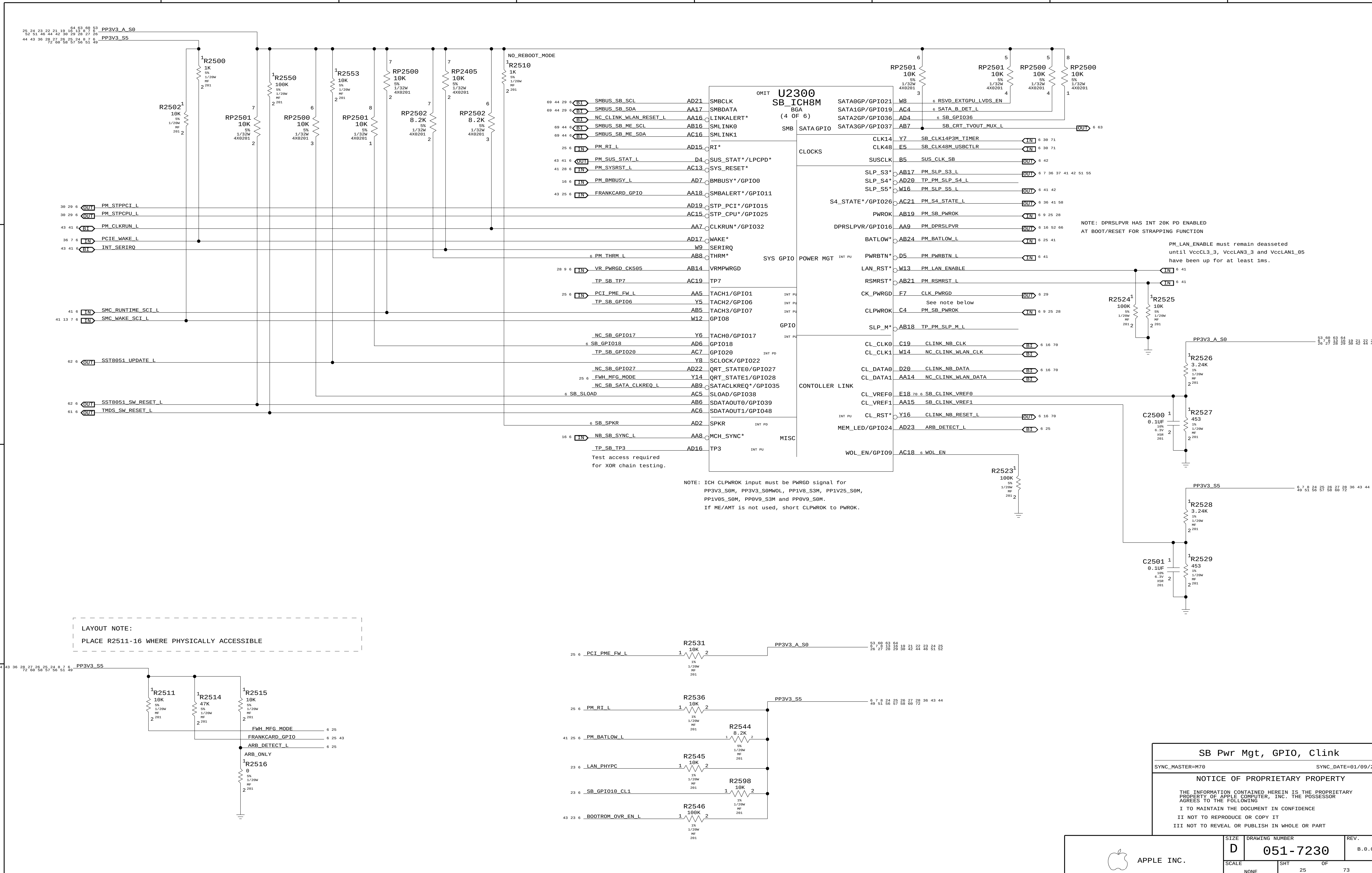
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE D DRAWING NUMBER 051-7230 REV. 8.0.0

SCALE NONE SHT 24 OF 73



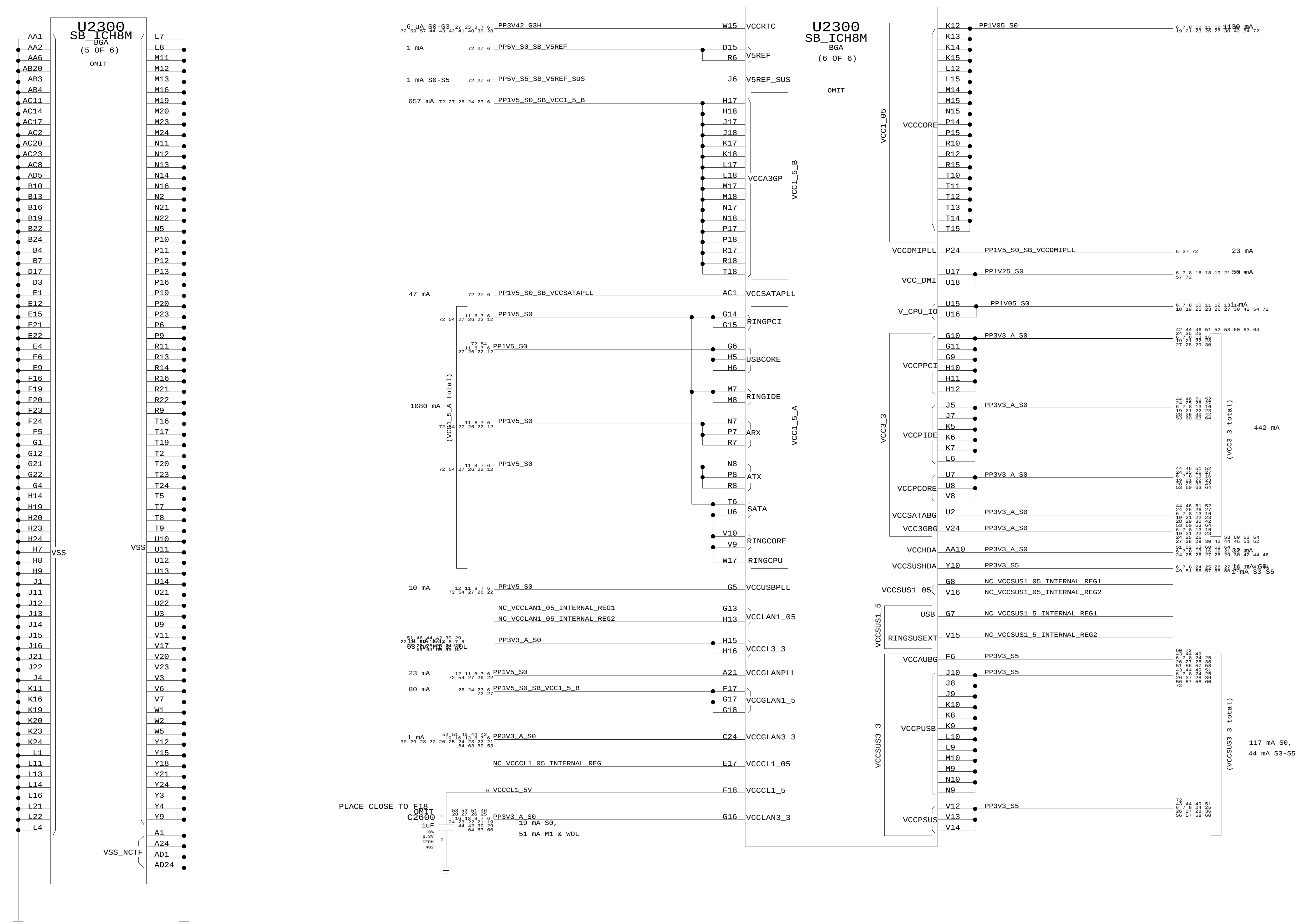
SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE	SHT	OF
NONE	25	73



NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.

Current figures provided assume 1.5V.

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

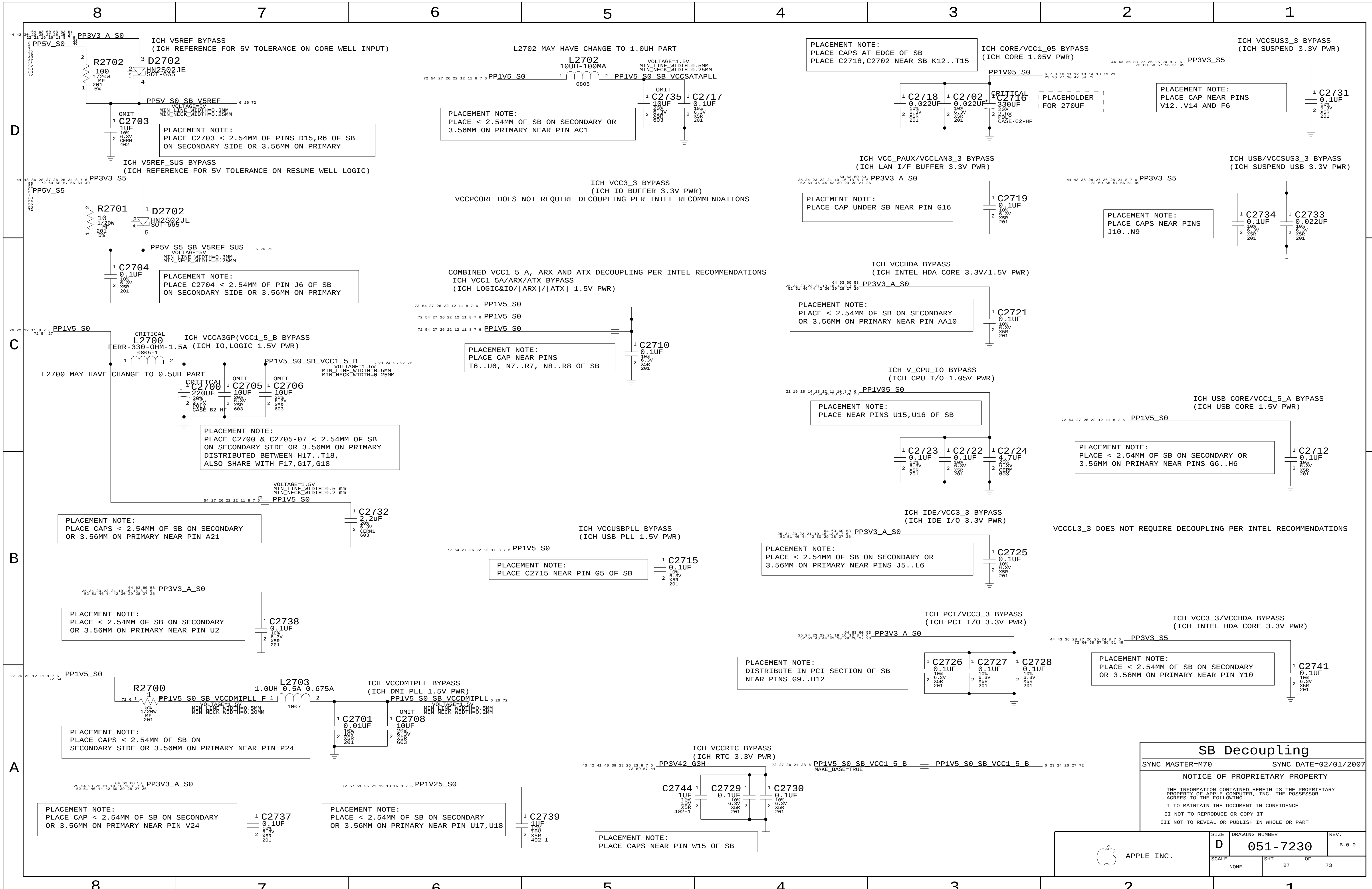
SB Power & Ground

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.	SIZE D	DRAWING NUMBER 051-7230
	REV.	8.0.0
	SCALE NONE	SHT 26 OF 73

www.laptop-schematics.com



SB Decoupling

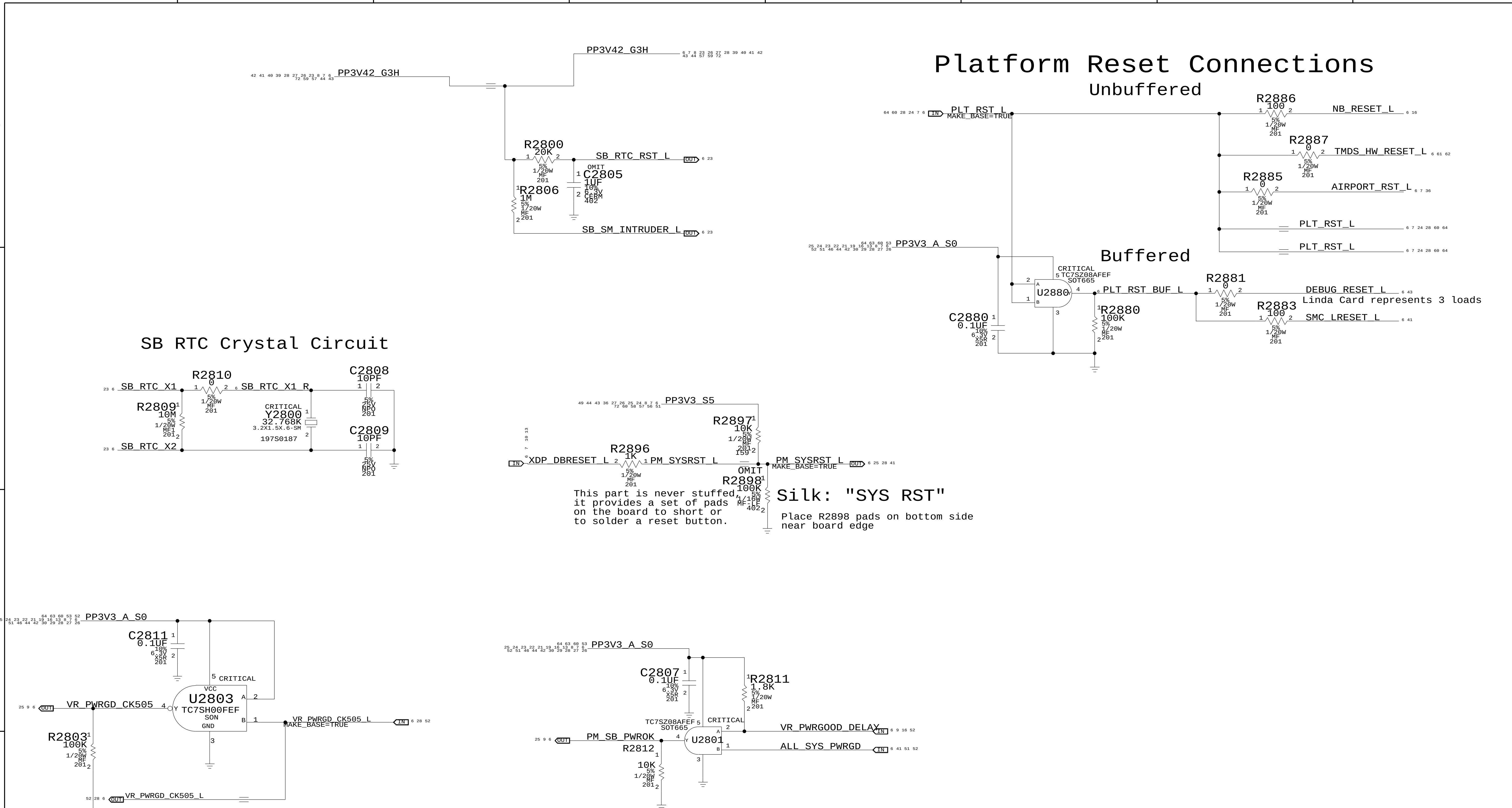
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 27 OF 73



SB Misc

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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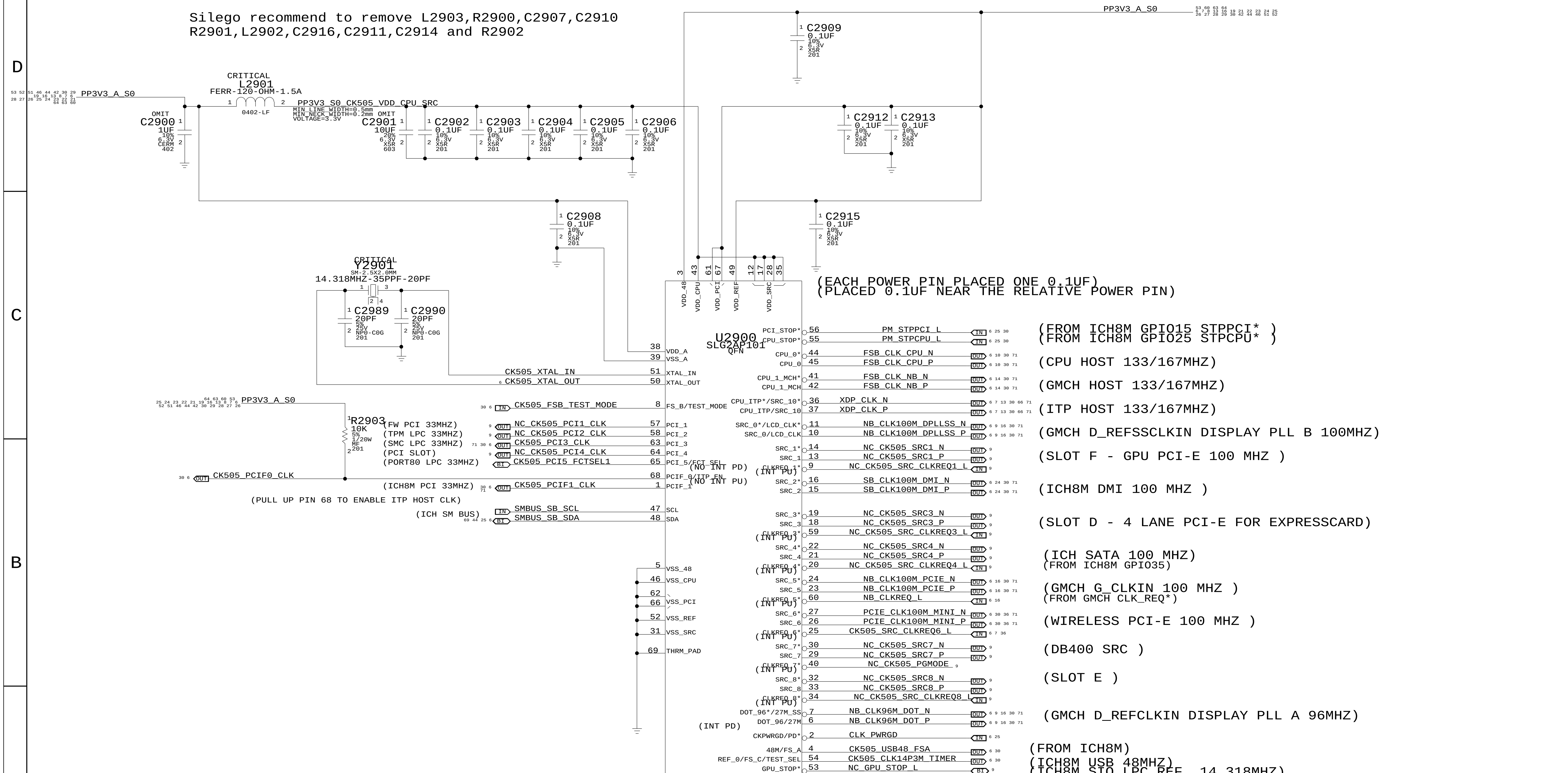
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 28	OF 73



FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

Clock (CK505)

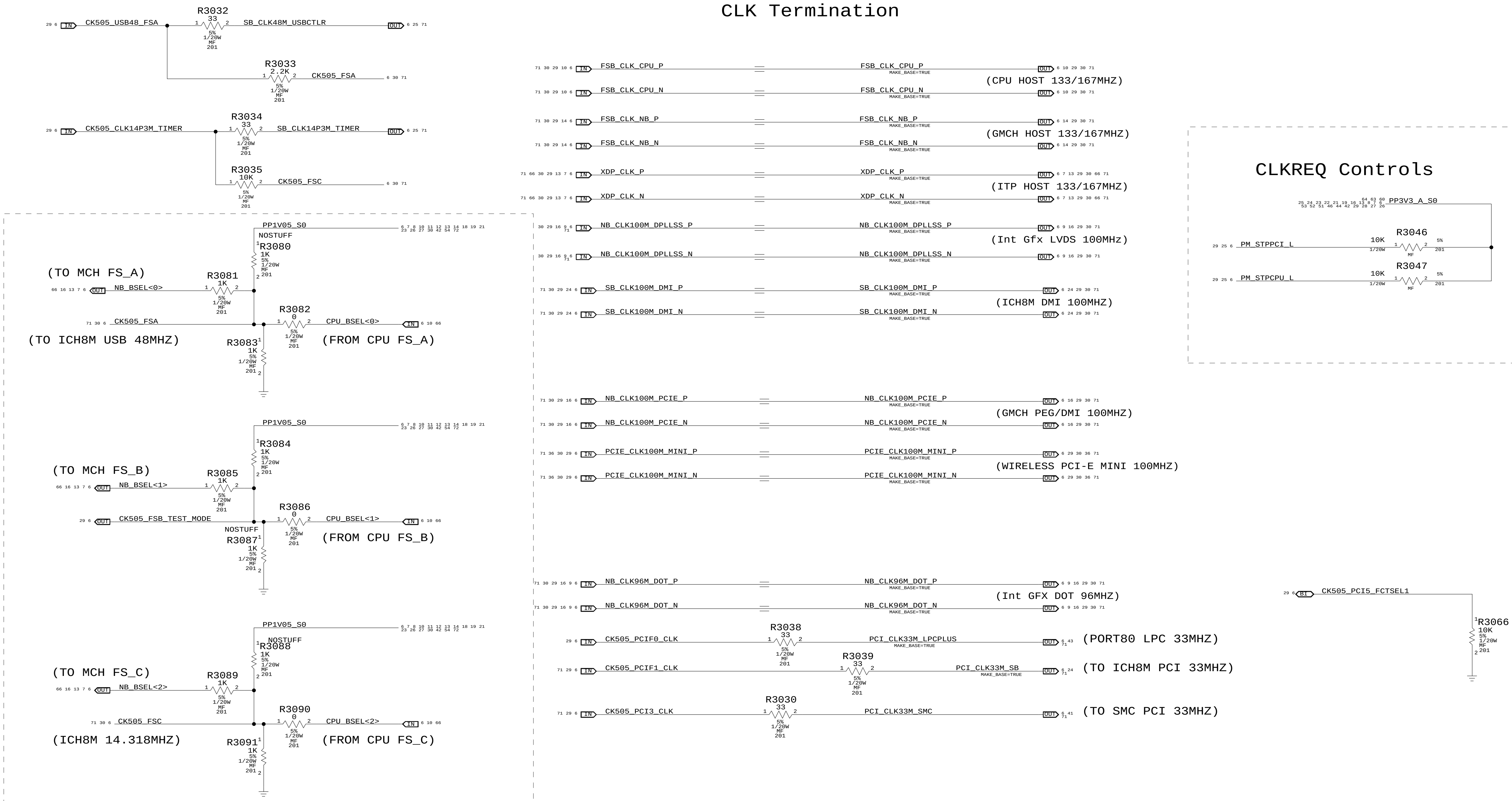
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE: NONE SHT 29 OF 73

CLK Termination



	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
	0	0	1	133M
	0	1	1	166M
*	0	1	0	200M
	1	1	0	400M
	1	1	1	Resrvd
	1	0	1	100M
	1	0	0	333M

NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY

CPU speed is currently set to 200MHz

Clock Termination

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE D DRAWING NUMBER 051-7230 REV. 8.0.0

SCALE NONE SHT 30 OF 73

DDR2 DRAM Channel A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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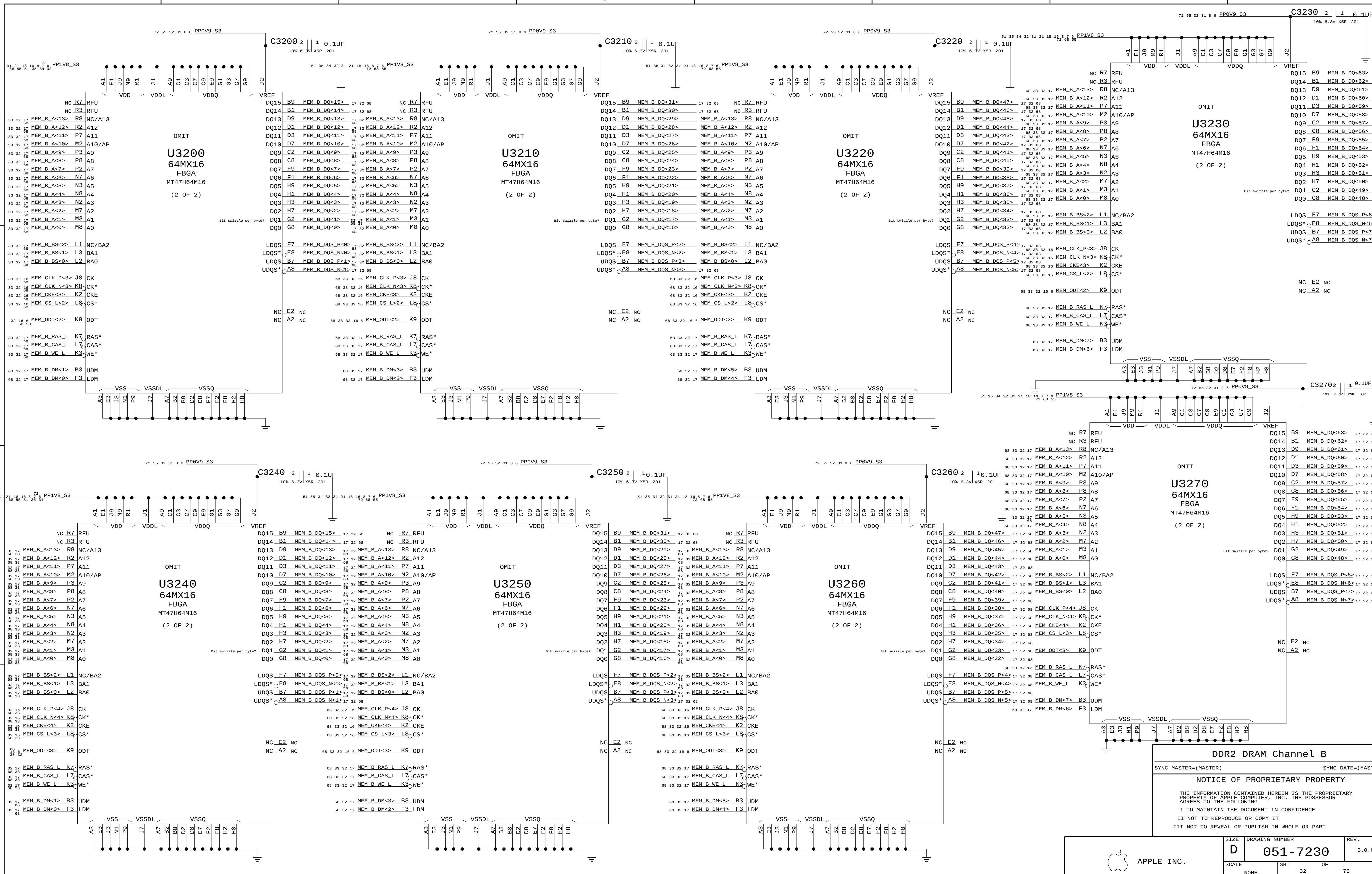
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE	SHT	OF
NONE	31	73



DDR2 DRAM Channel B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

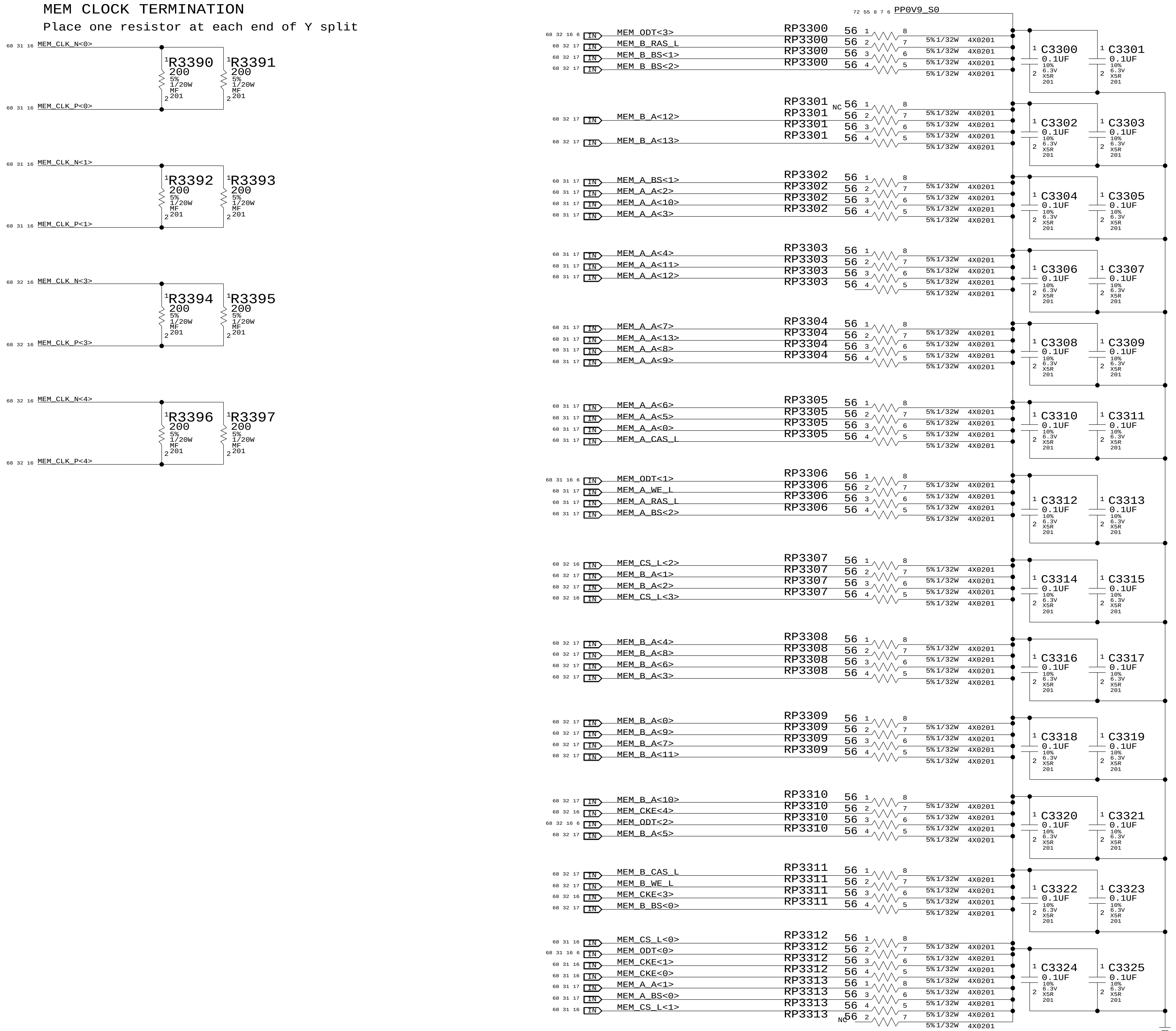
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 32	OF 73

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it

MEM CLOCK TERMINATION

Place one resistor at each end of Y split



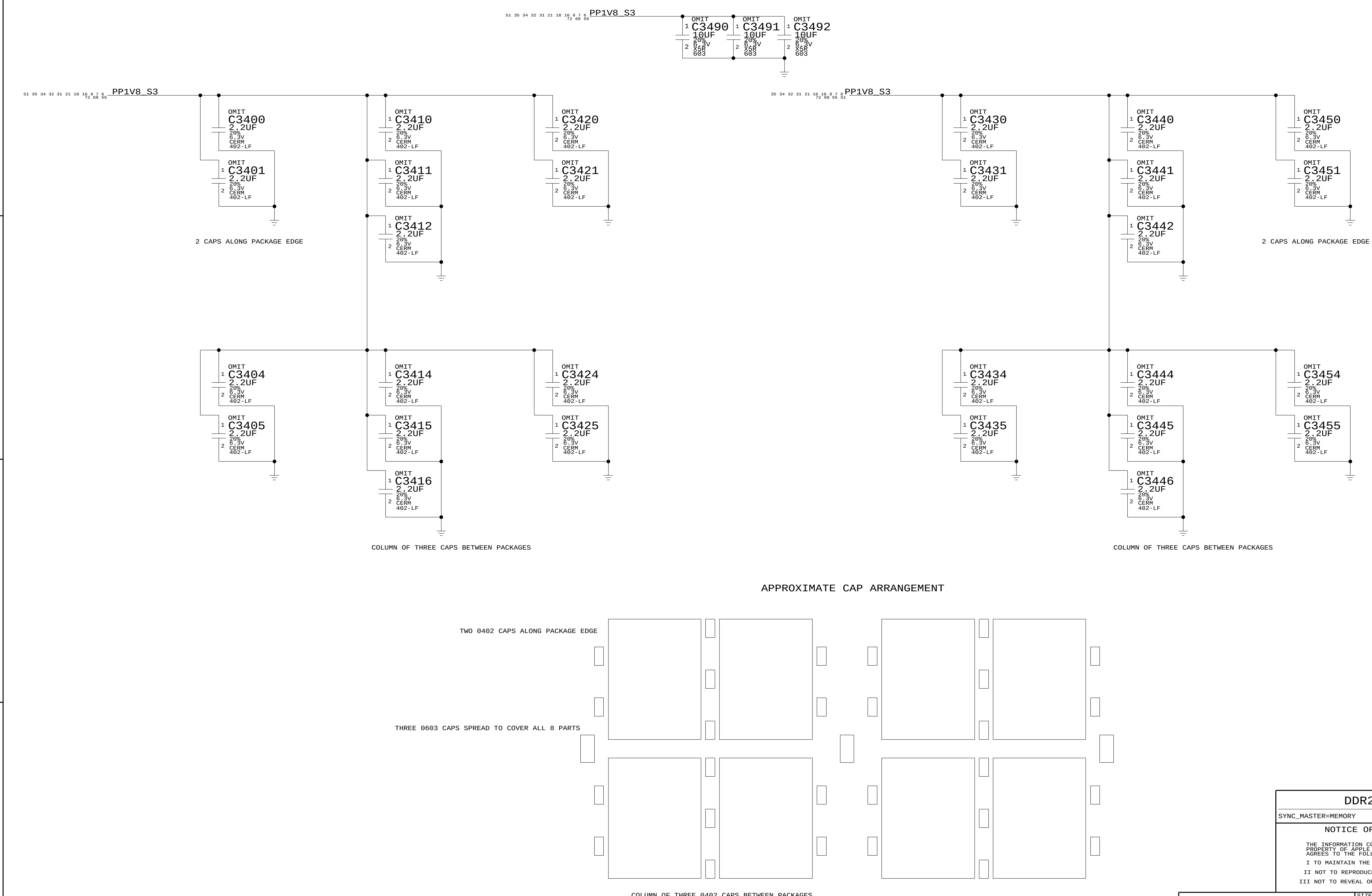
LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED
TO PP0V9_S0_MEM_TERM

Memory Active Termination

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 33	OF 73



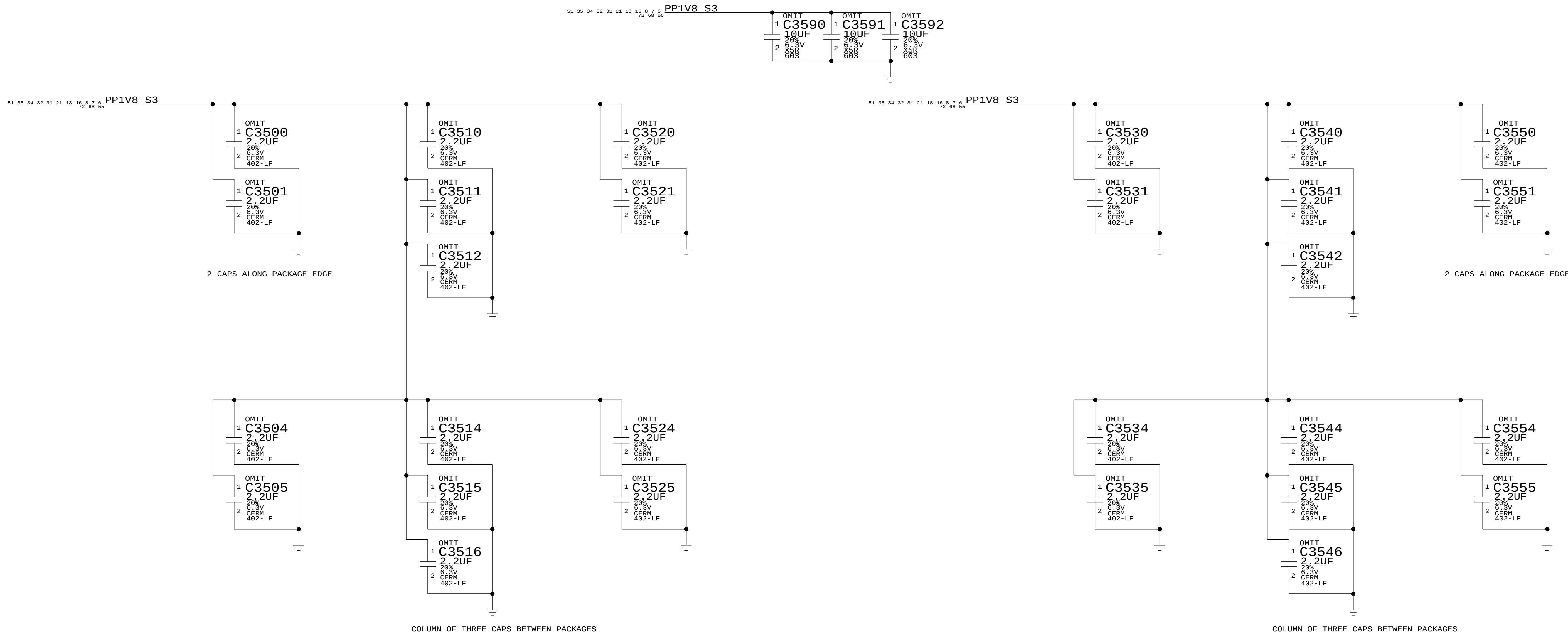
DDR2 BYPASSING 1

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

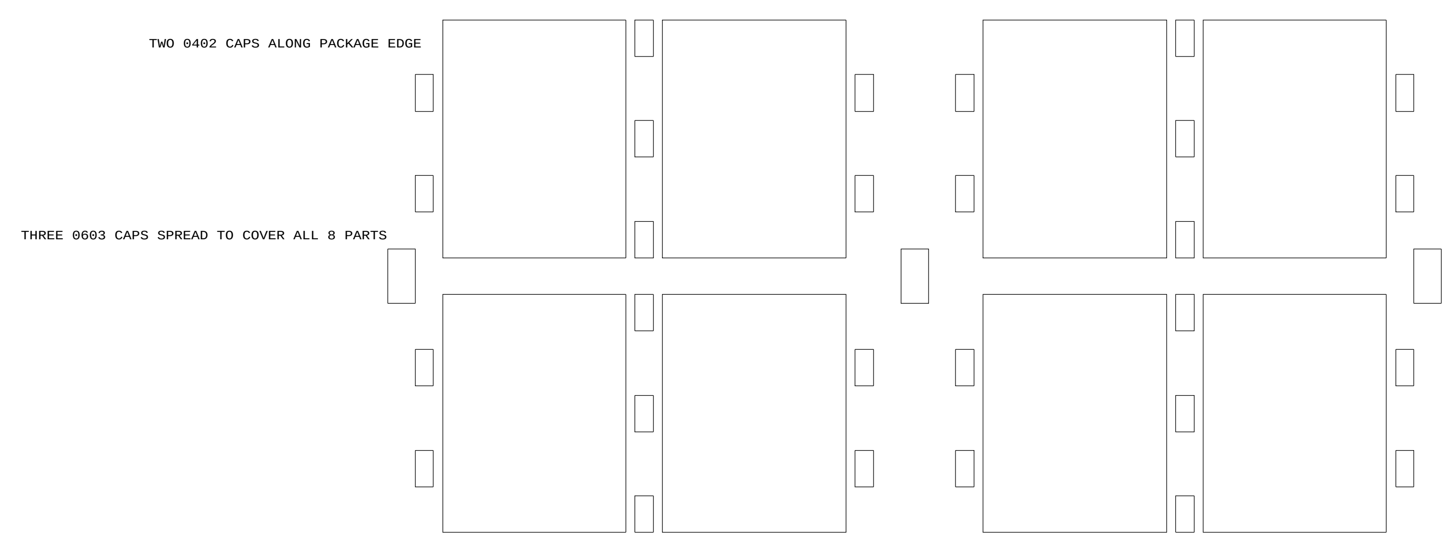
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 34 OF 73



APPROXIMATE CAP ARRANGEMENT



DDR2 BYPASSING 2

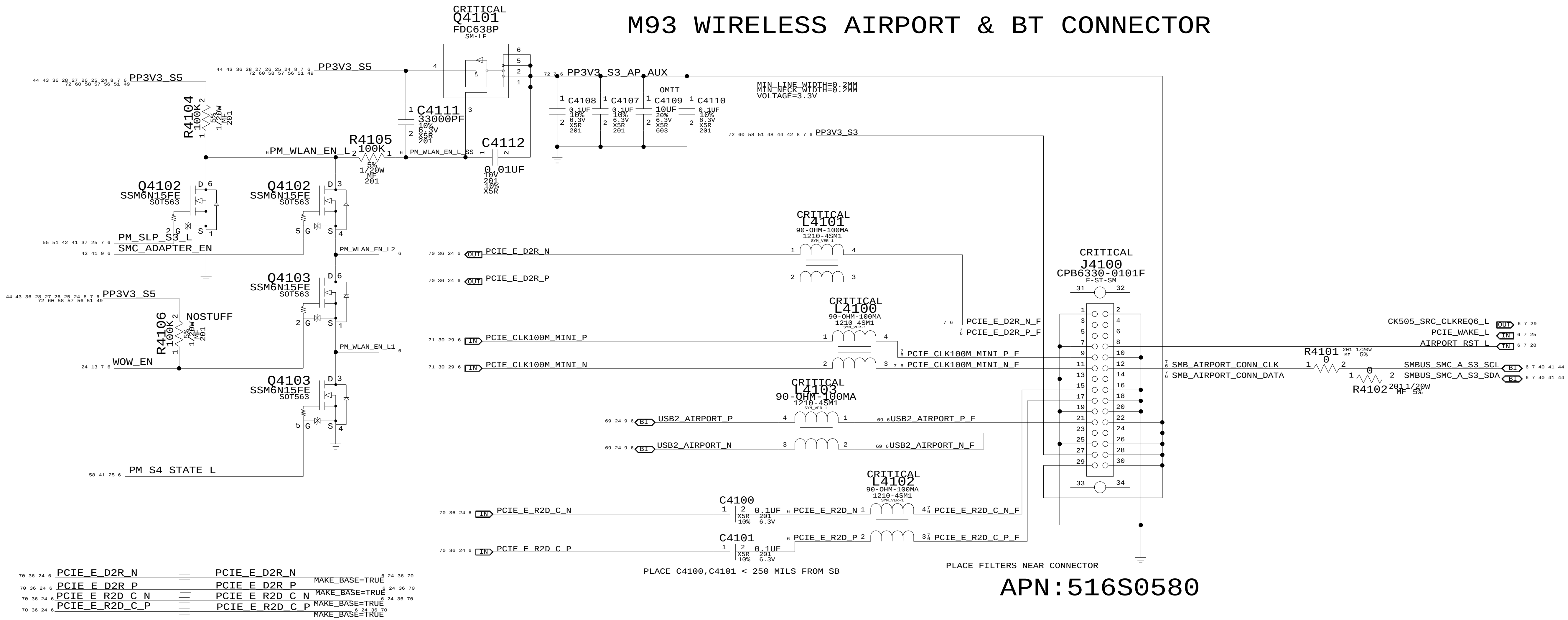
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE | SHT 35 OF 73

M93 WIRELESS AIRPORT & BT CONNECTOR



Wireless M93 Connector

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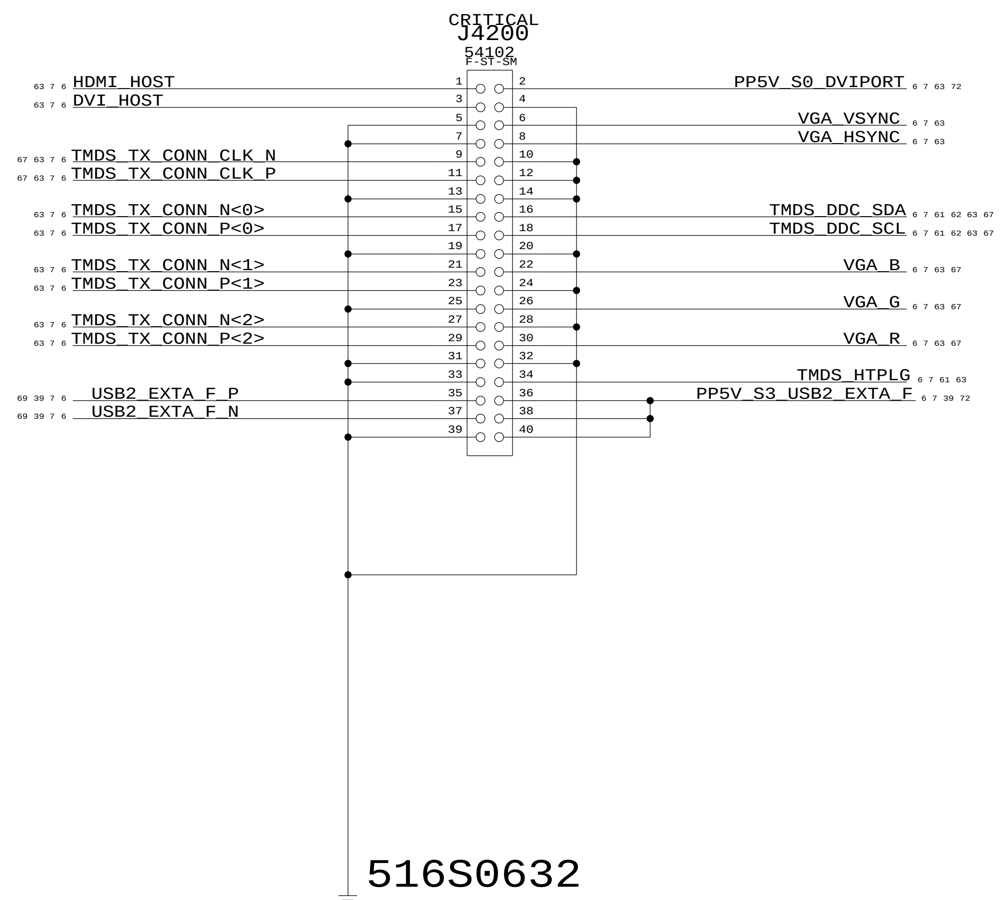
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

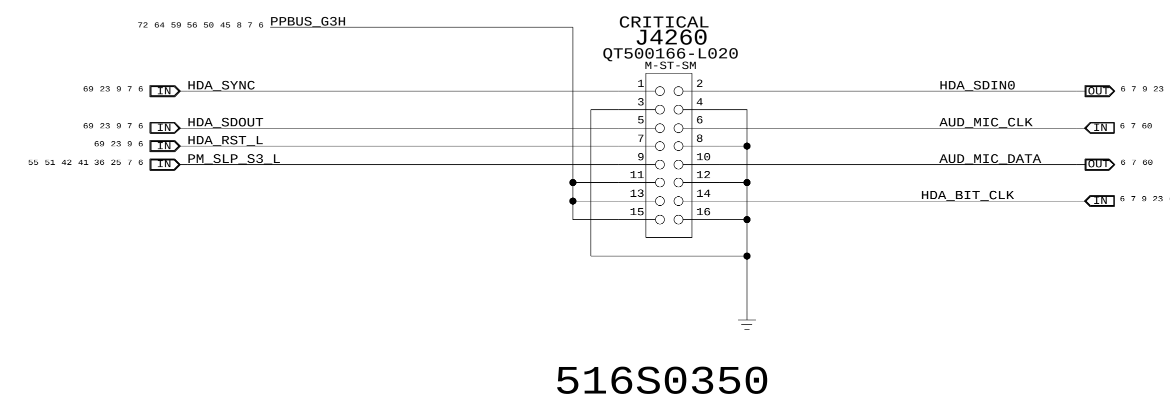
APPLE INC.

SCALE NONE — SHT 36 OF 73

Micro DVI, USB, to RIO Hatch Assembly



Audio Connector



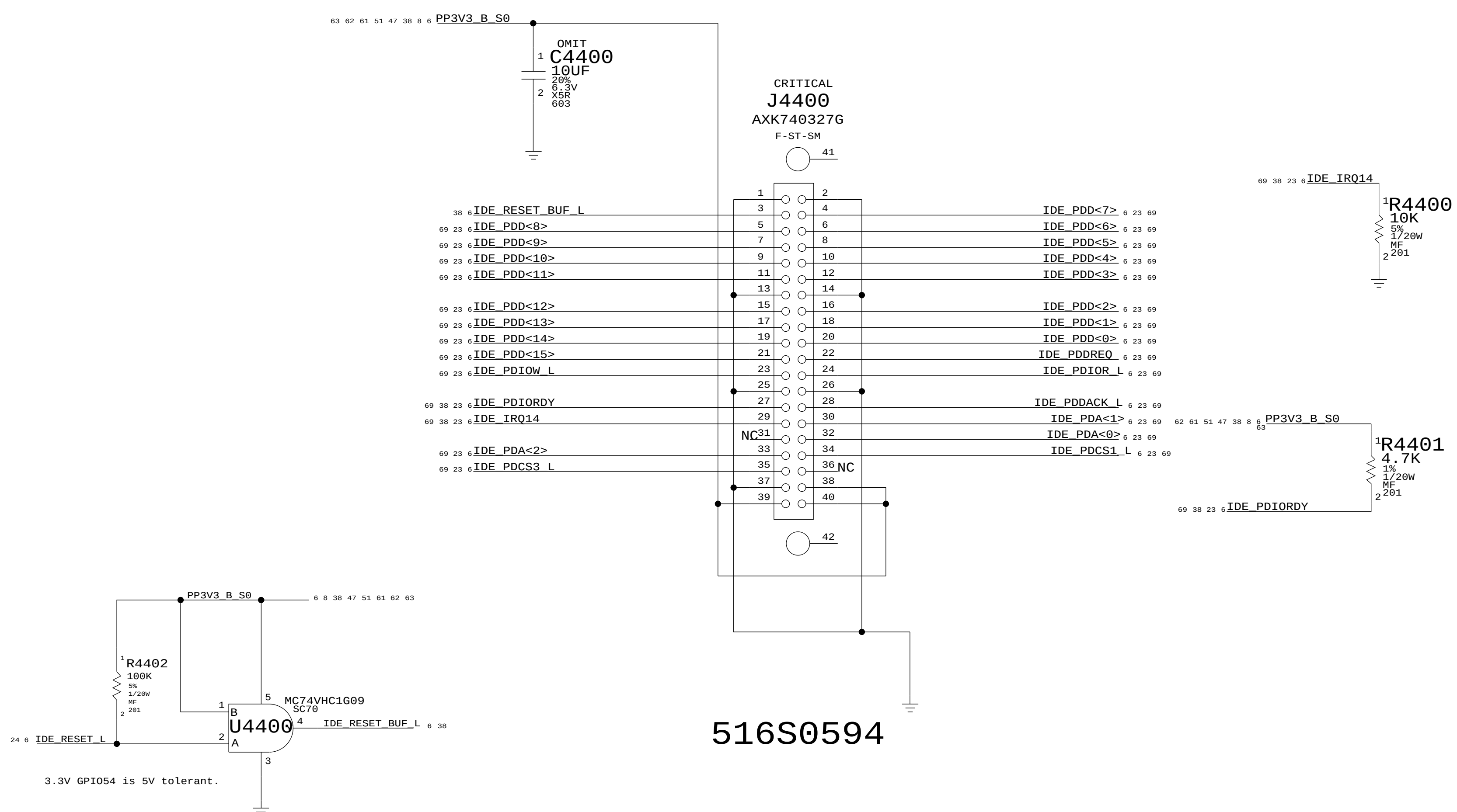
Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

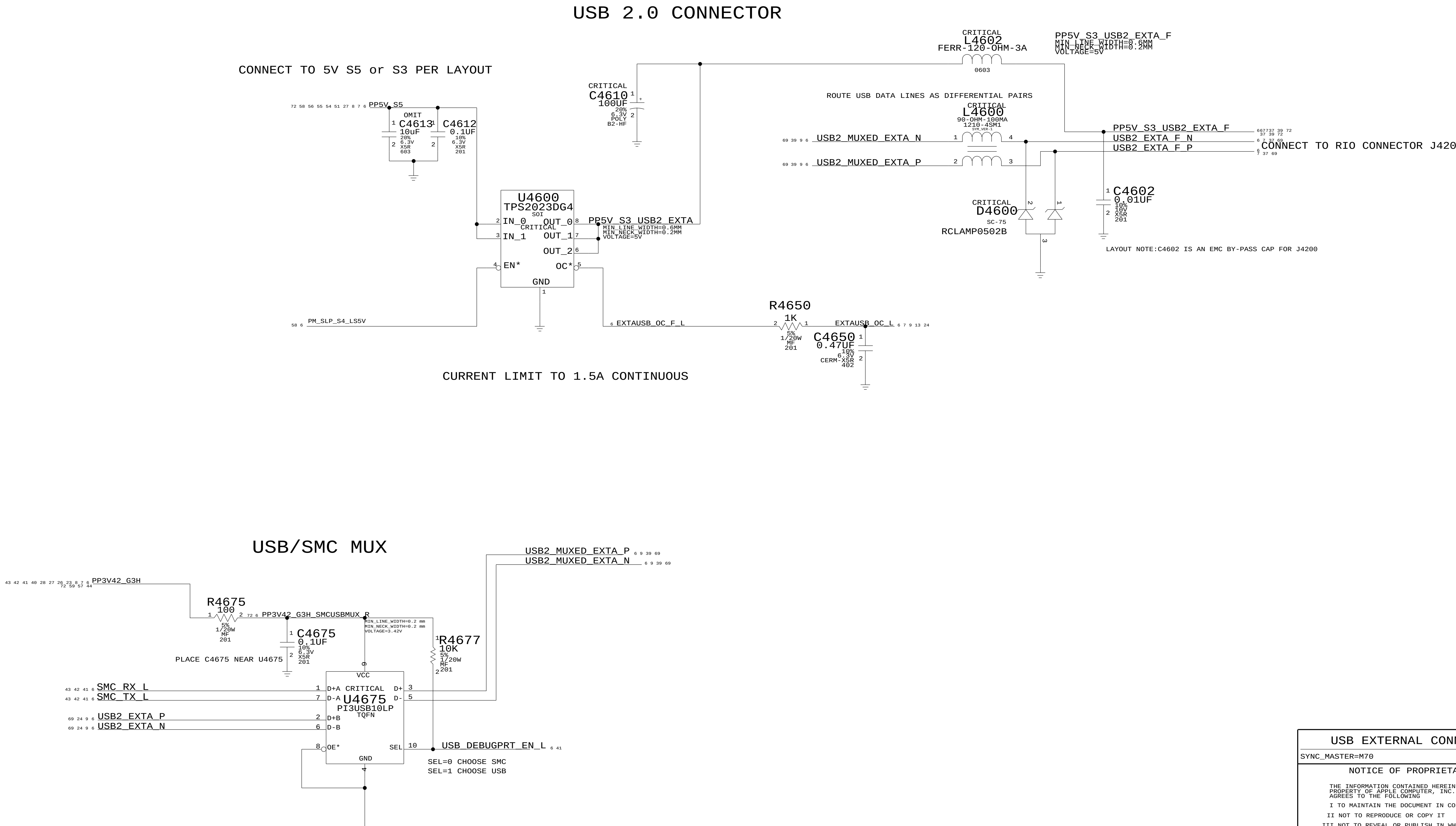
SCALE	SHT	OF
NONE	37	73



PATA HDD CONNECTOR

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 38	OF 73



USB EXTERNAL CONNECTORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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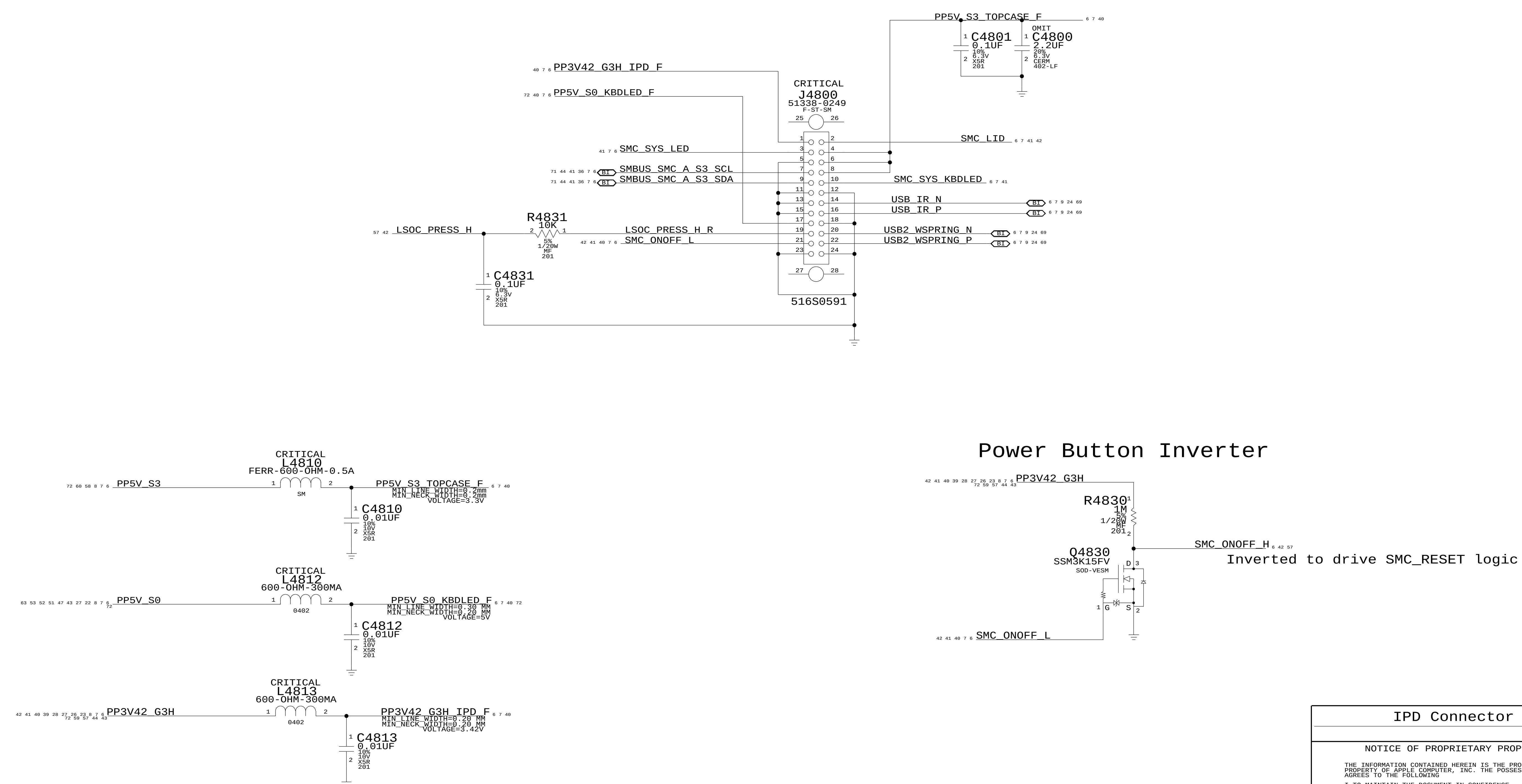
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 39	OF 73

IPD Connector



IPD Connector

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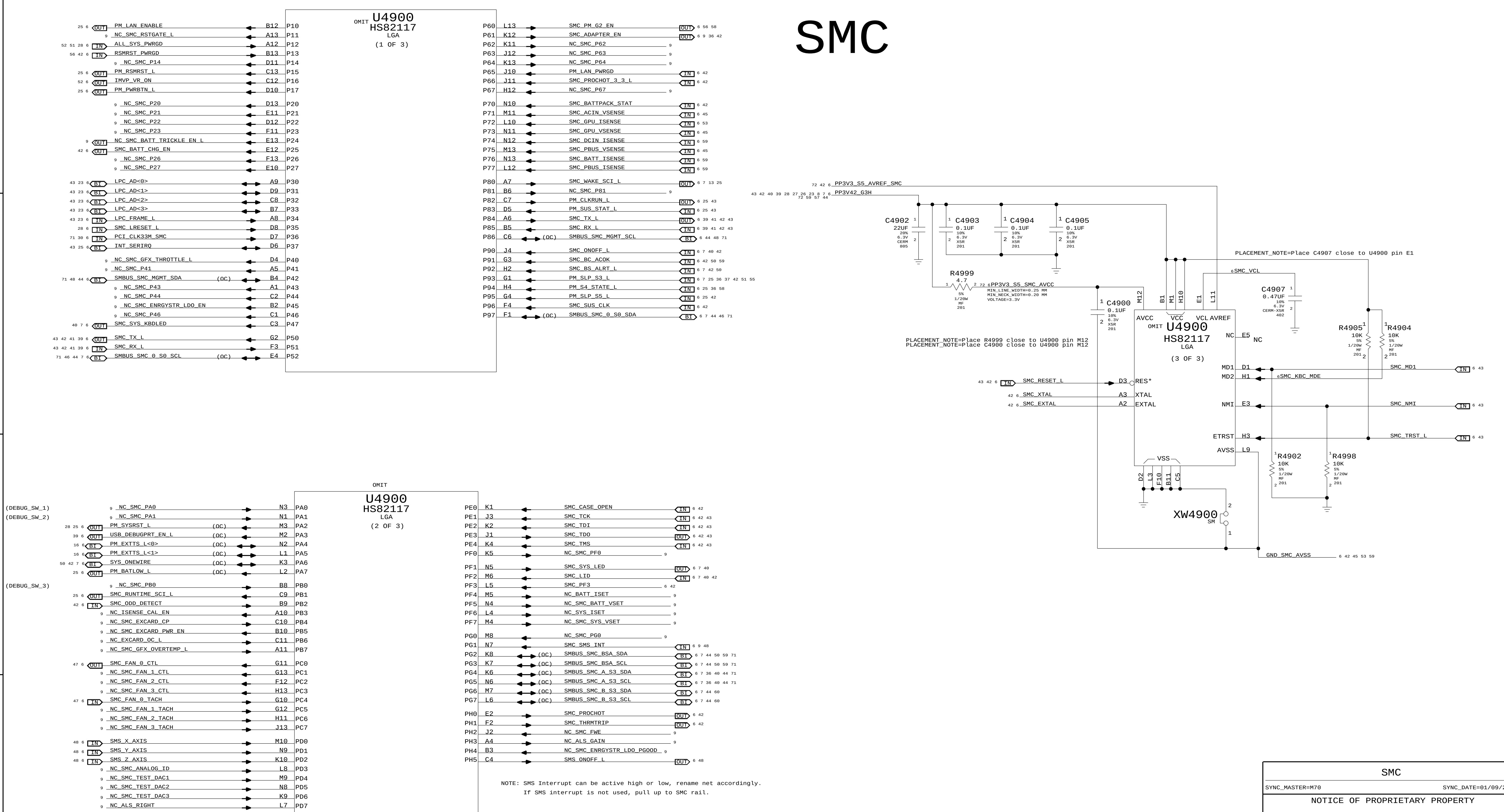
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE: NONE	SHT 40	OF 73

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SMC



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

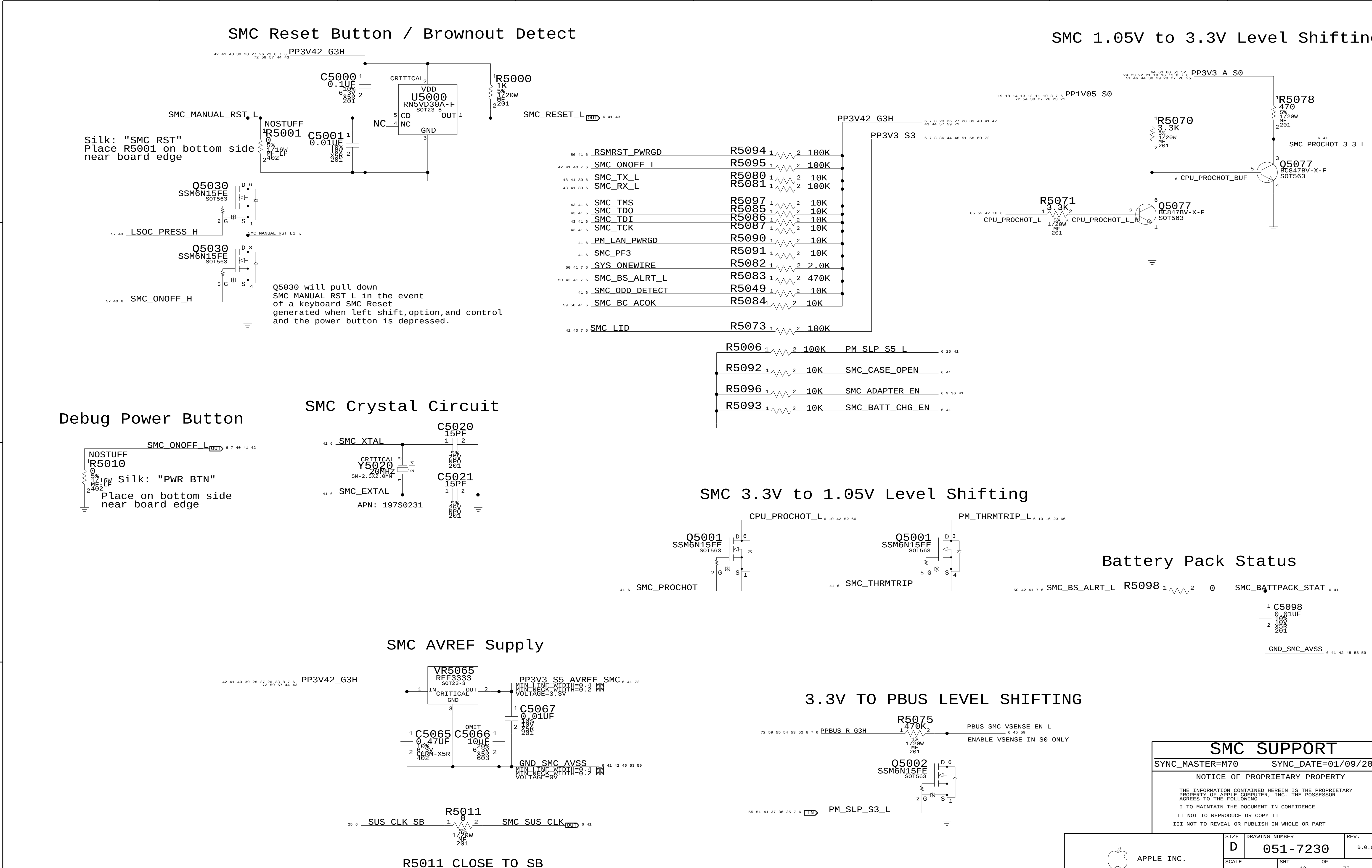
SMC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 41 OF 73	



SMC SUPPORT

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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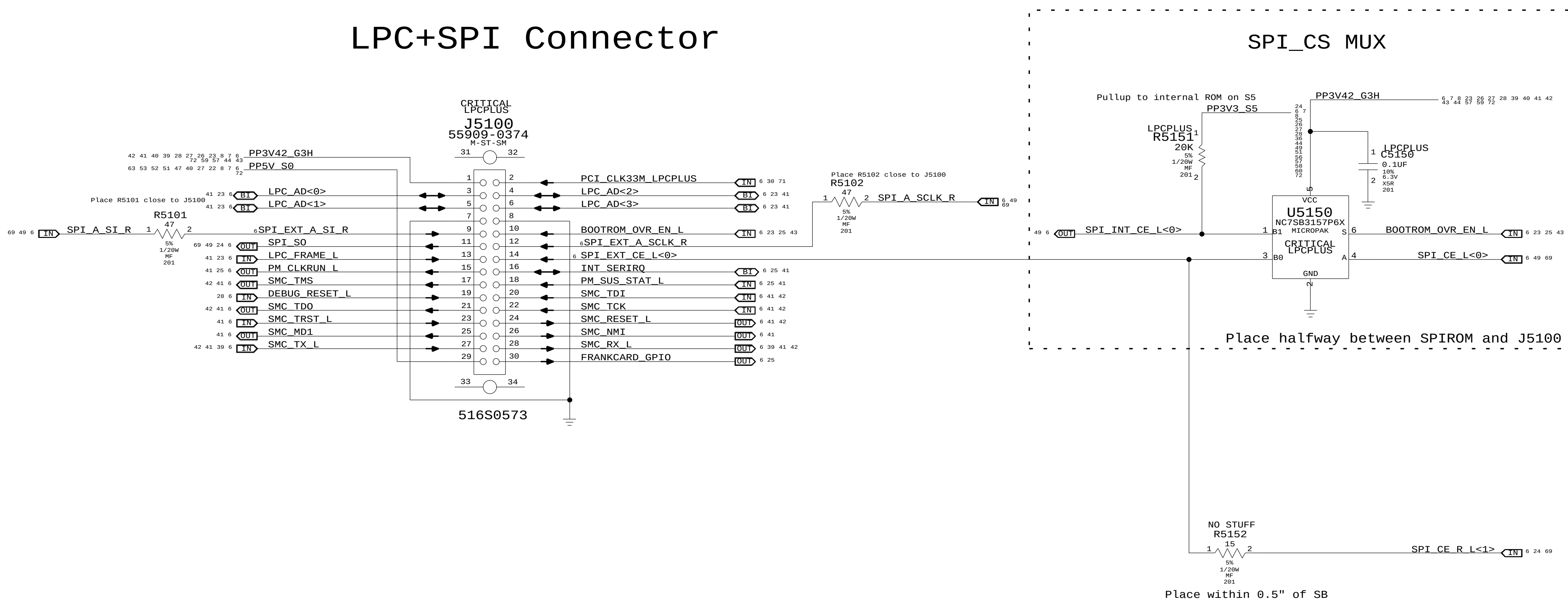
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE	SHT	OF
NONE	42	73



LPC+SPI Debug Connector	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

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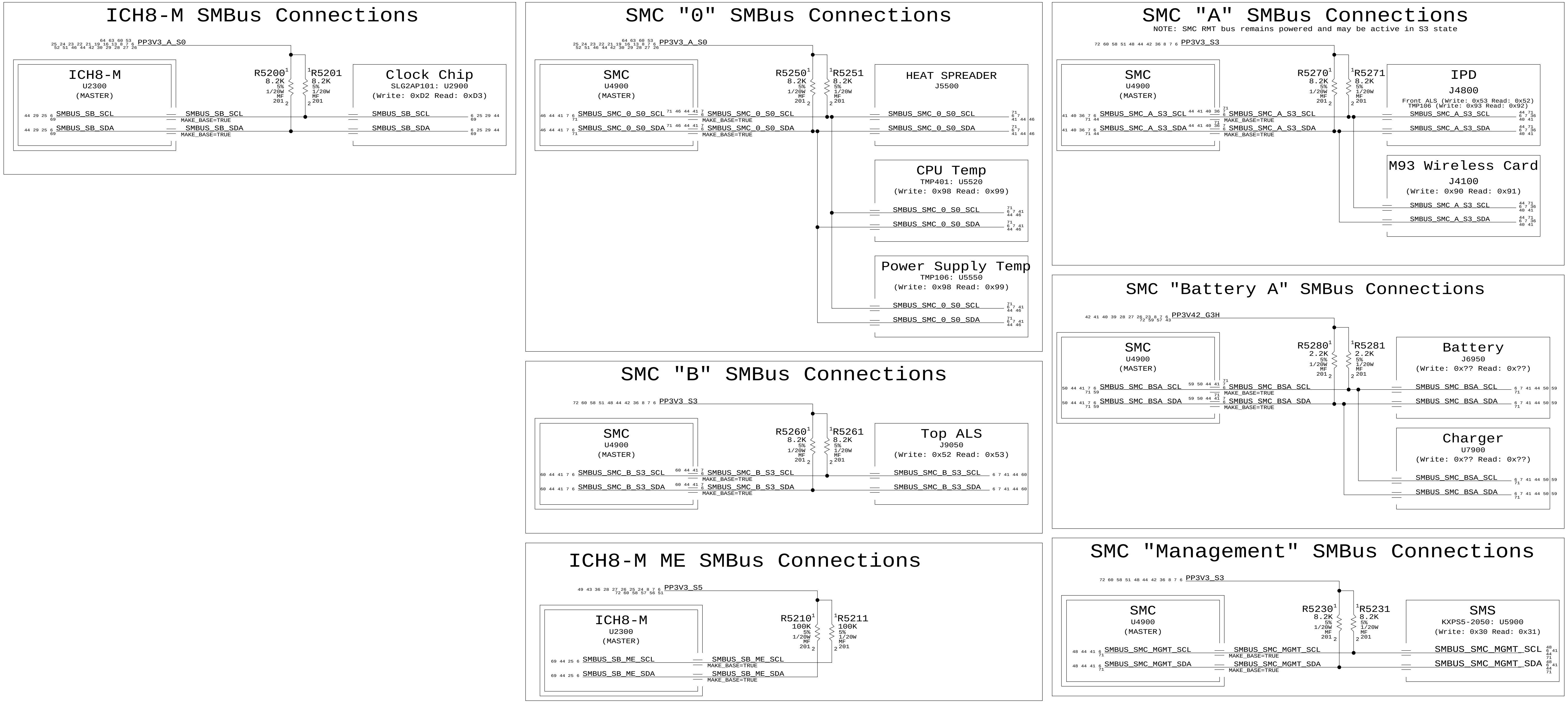
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 43 OF 73	



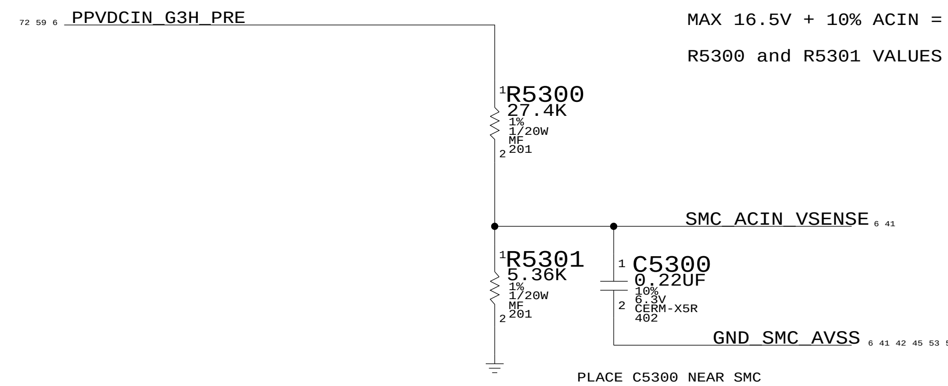
SMBUS CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 44	OF 73

ACIN VOLTAGE SENSE



MAX 16.5V + 10% ACIN = 3.0V SMC_PBUS_VSENSE

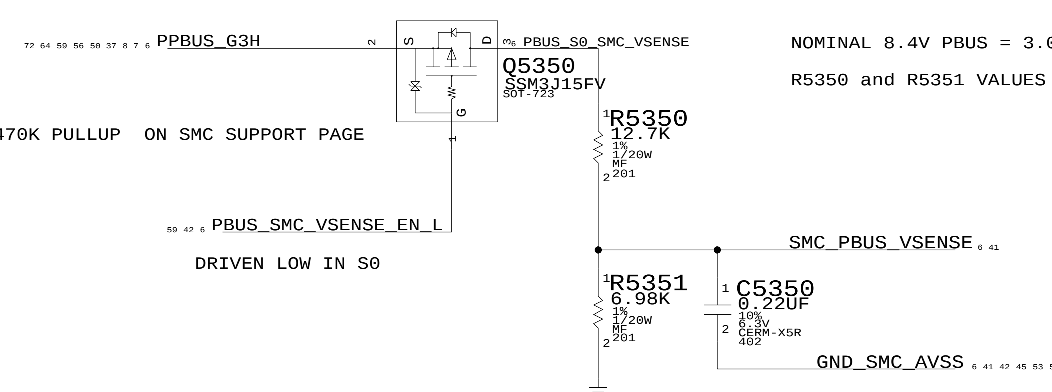
R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

PLACE C5300 NEAR SMC

GPU VOLTAGE SENSE

PLACE R5310.C5310 NEAR SMC

PBUS VOLTAGE SENSE



NOMINAL 8.4V PBUS = 3.0V SMC_PBUS_VSENSE

R5350 and R5351 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

470K PULLUP ON SMC SUPPORT PAGE

DRIVEN LOW IN S0

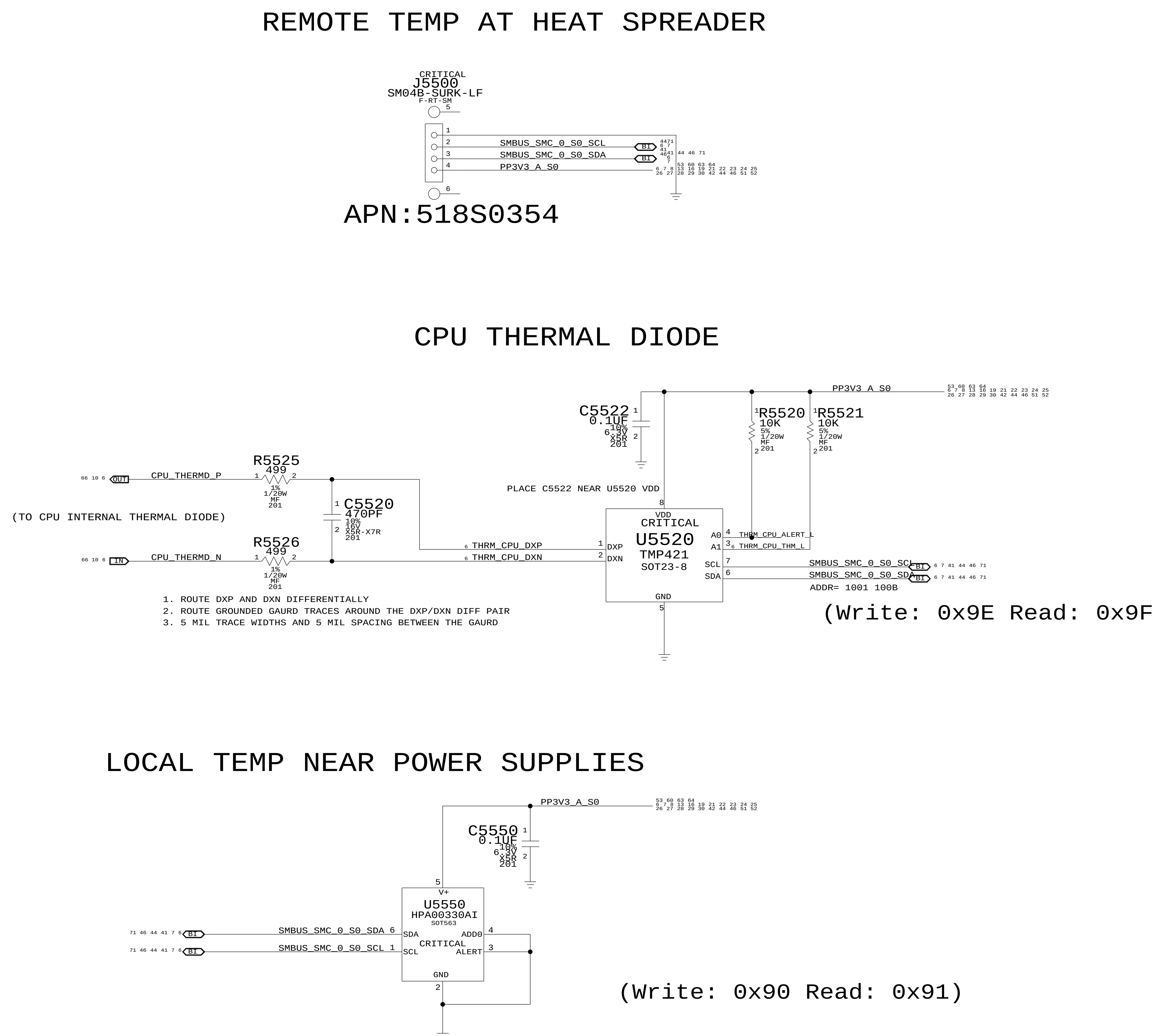
PLACE C5350 NEAR SMC

Voltage Sensors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 45	OF 73



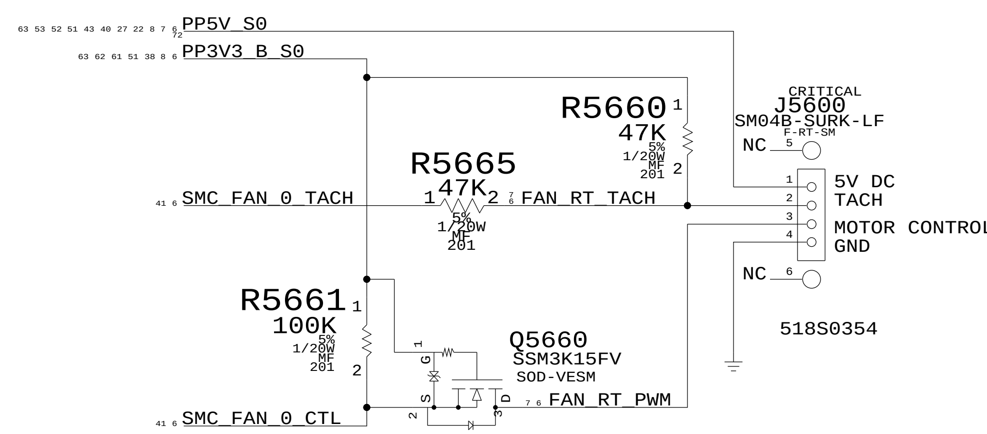
TEMPERATURE SENSORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 46	OF 73

FAN CONNECTOR



Fan	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

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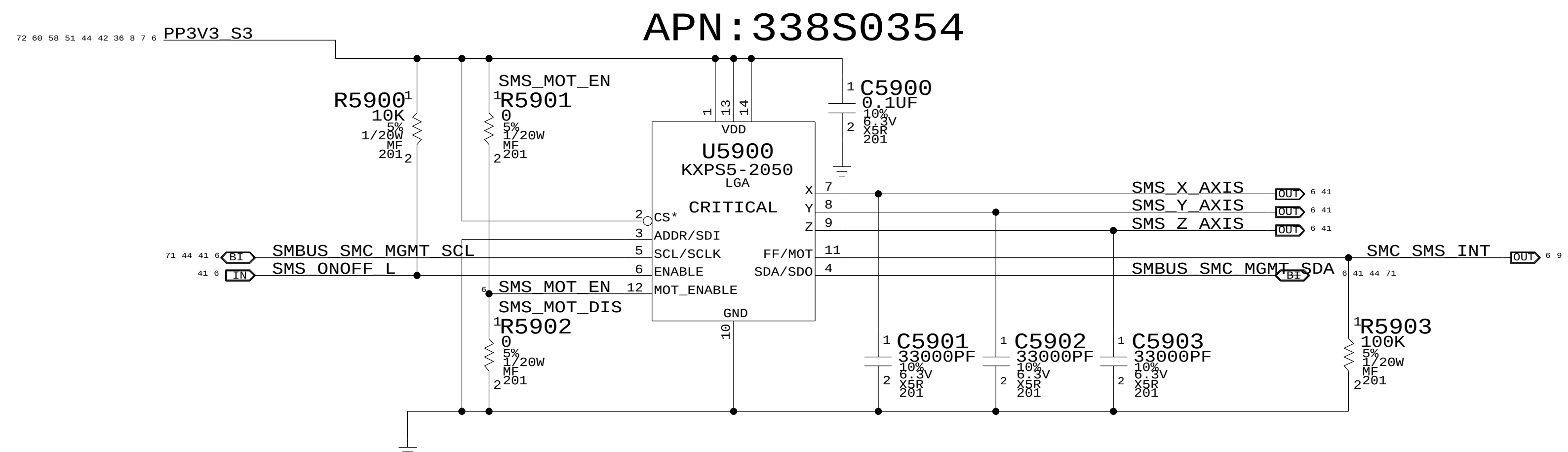
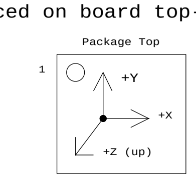
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 47	OF 73



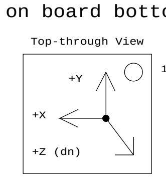
I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



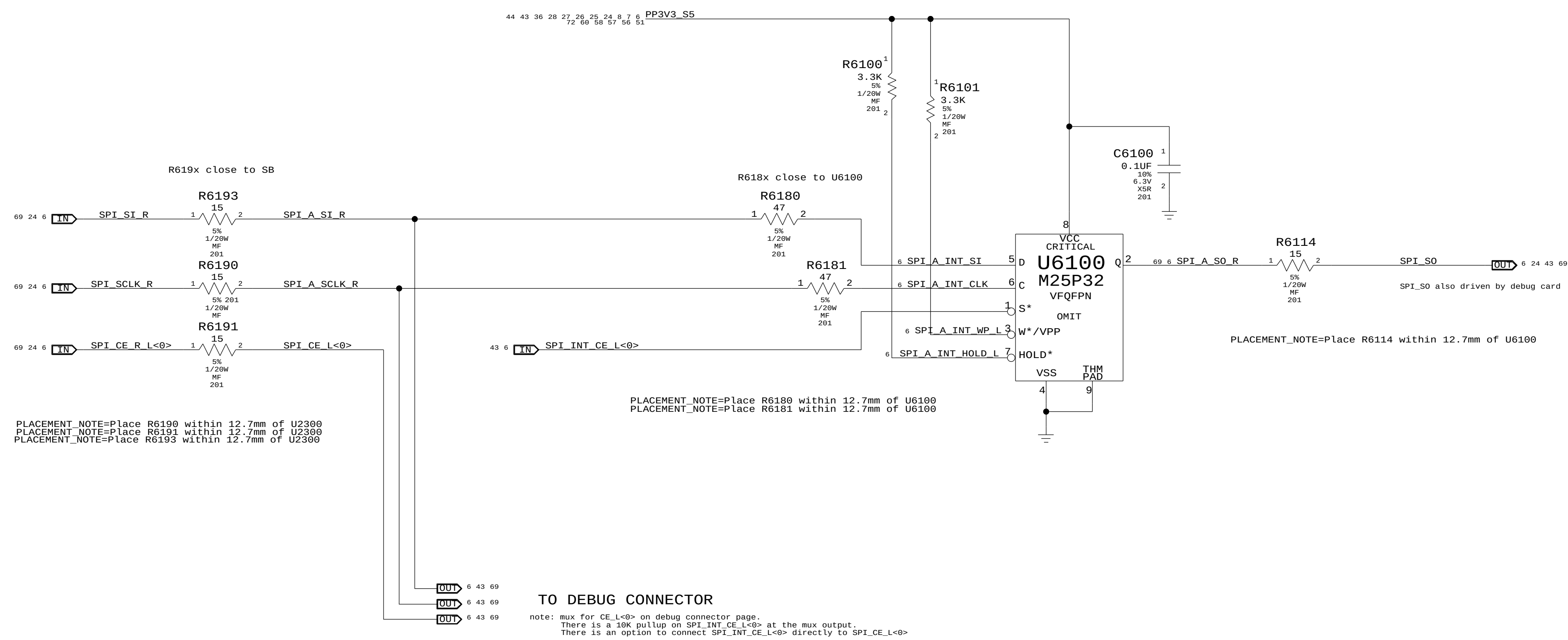
Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE: NONE	SHT 48	OF 73

SPI ROM



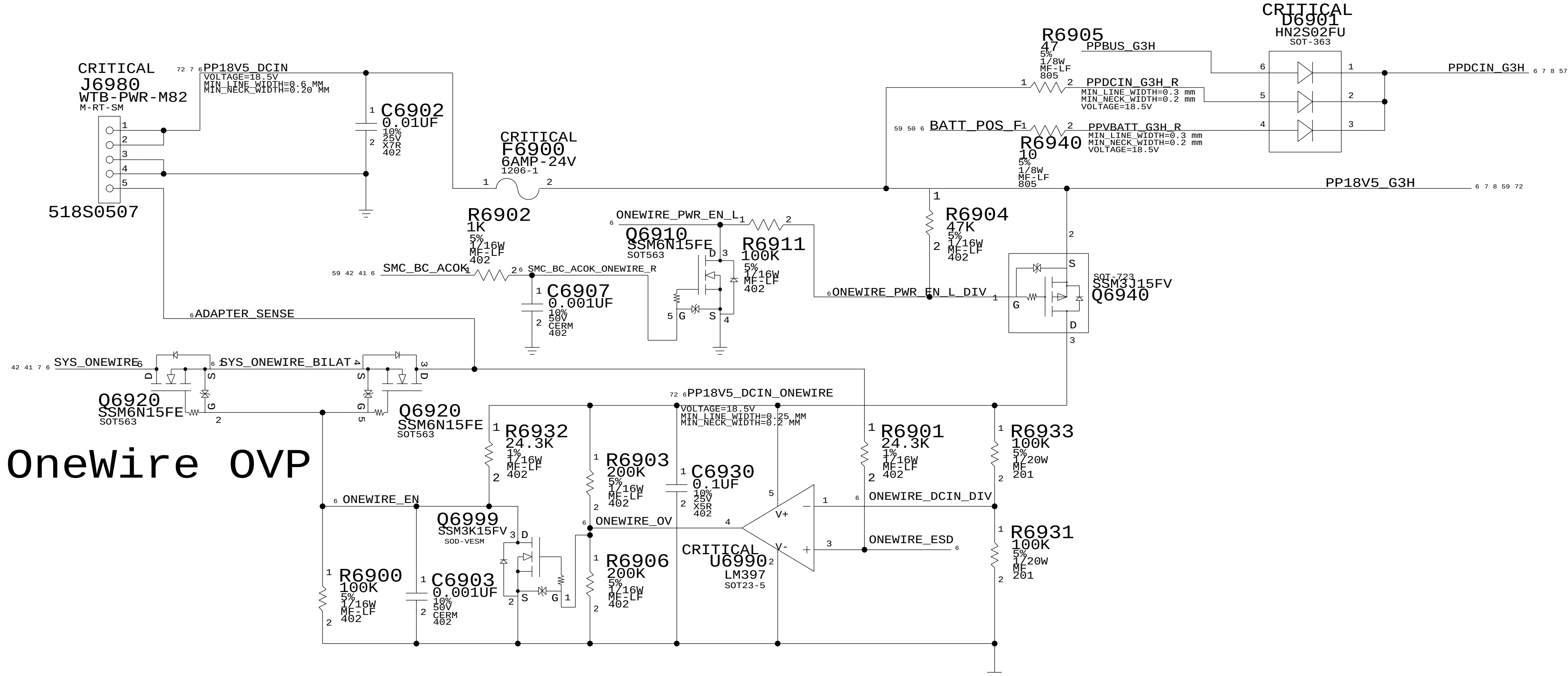
SPI ROMs

SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

NOTICE OF PROPRIETARY PROPERTY

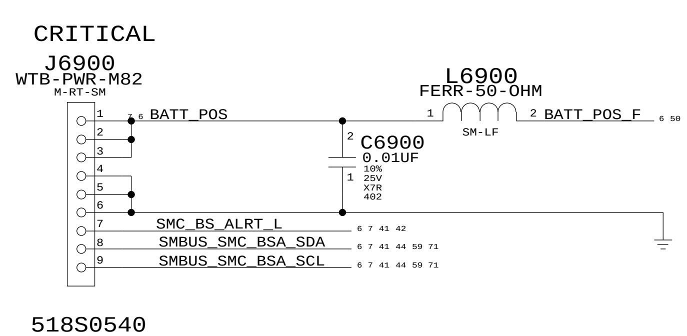
APPLE INC.	SIZE D	DRAWING NUMBER 051-7230	REV. 8.0.0
	SCALE NONE	SHT 49 OF 73	

DC-JACK INTERFACE



OneWire OVP

BATTERY INTERFACE

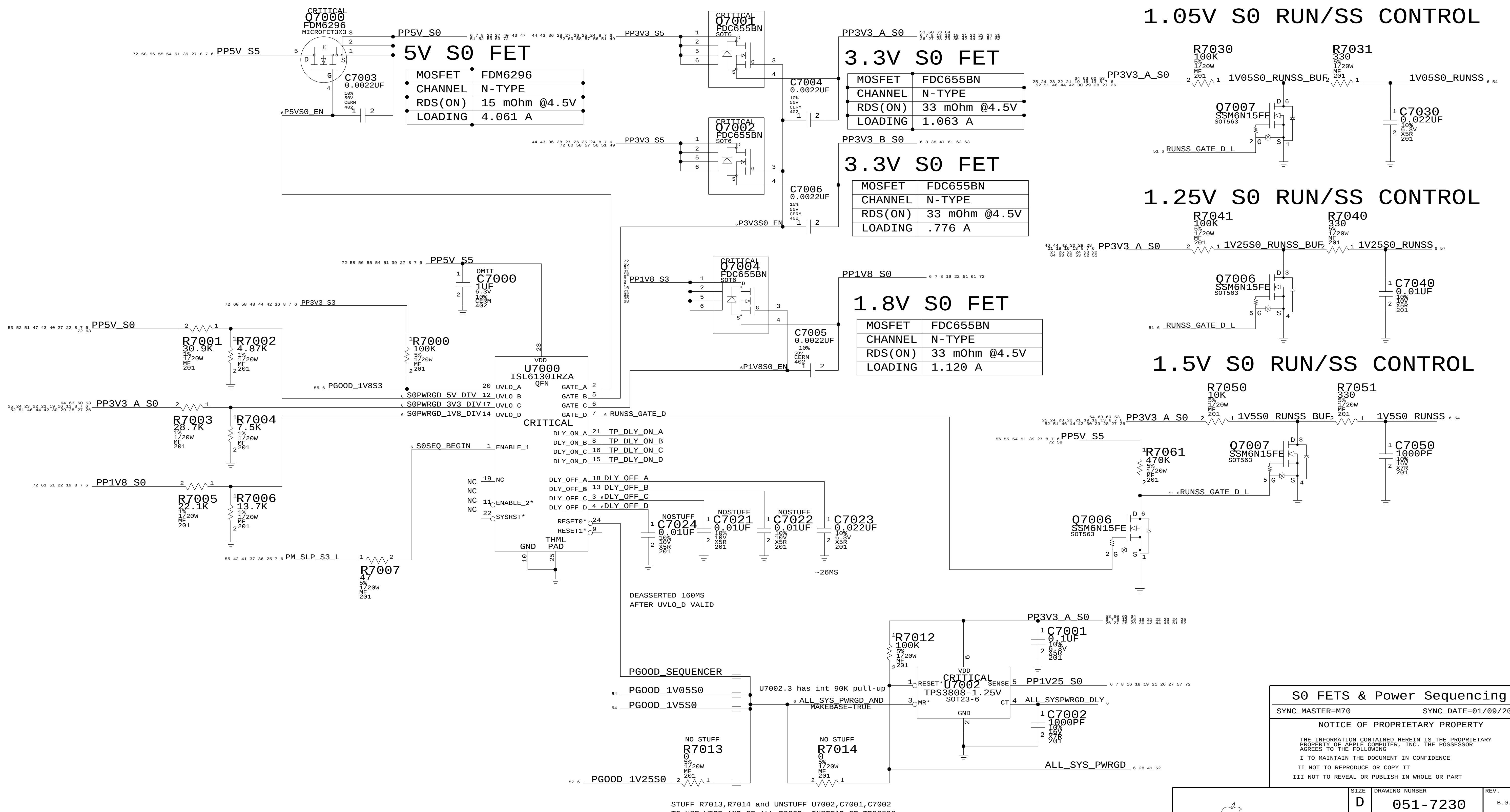


DC-In & Battery Connectors	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 50	OF 73

S0 FETS & POWER SEQUENCING & PGOOD



5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.061 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.063 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	.776 A

1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.120 A

S0 FETS & Power Sequencing

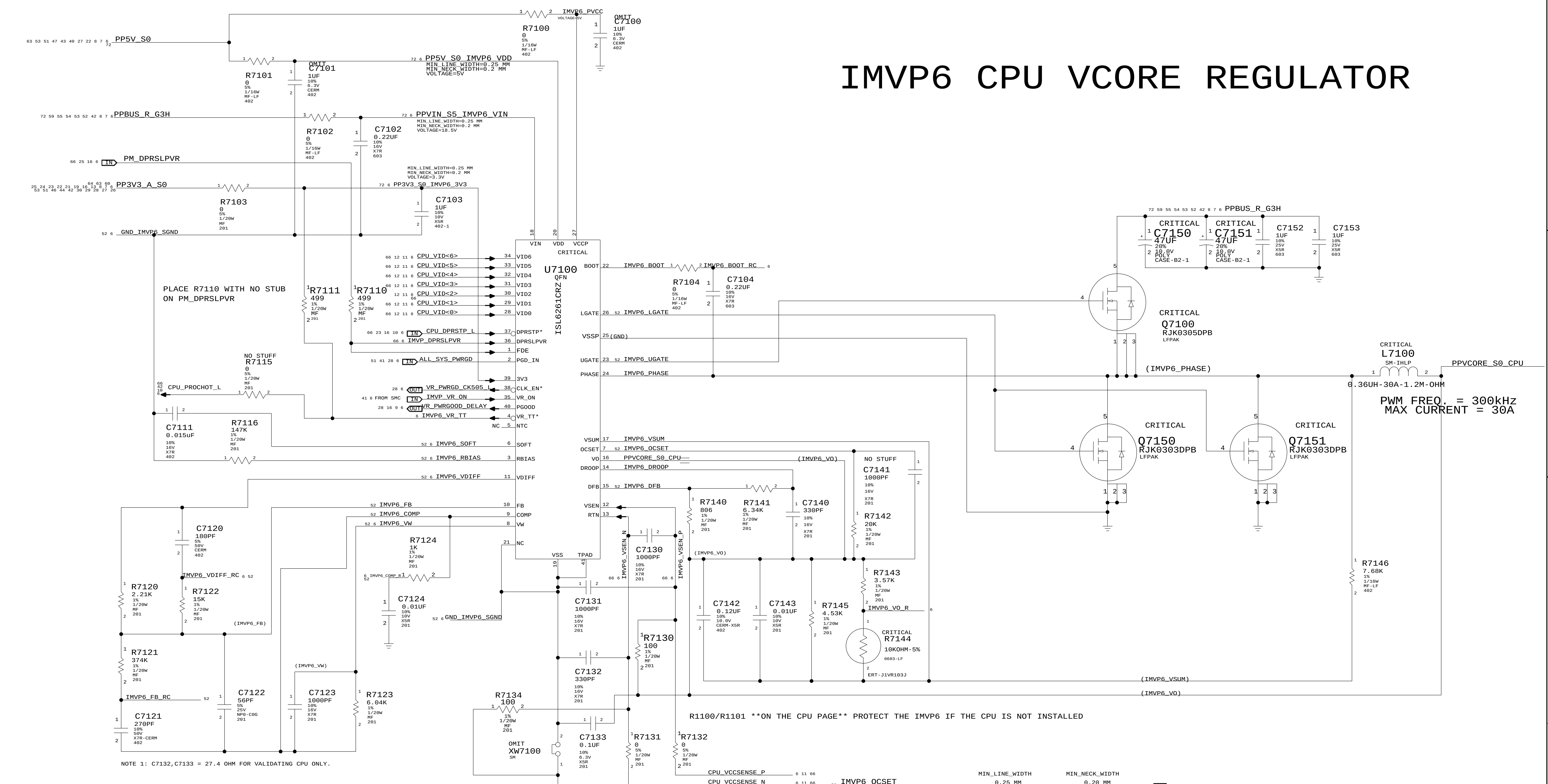
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. 8.0.0

SCALE NONE | SHT 51 OF 73

IMVP6 CPU VCORE REGULATOR



	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
PPVCORE_S0_CPU	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_COMP_RC	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

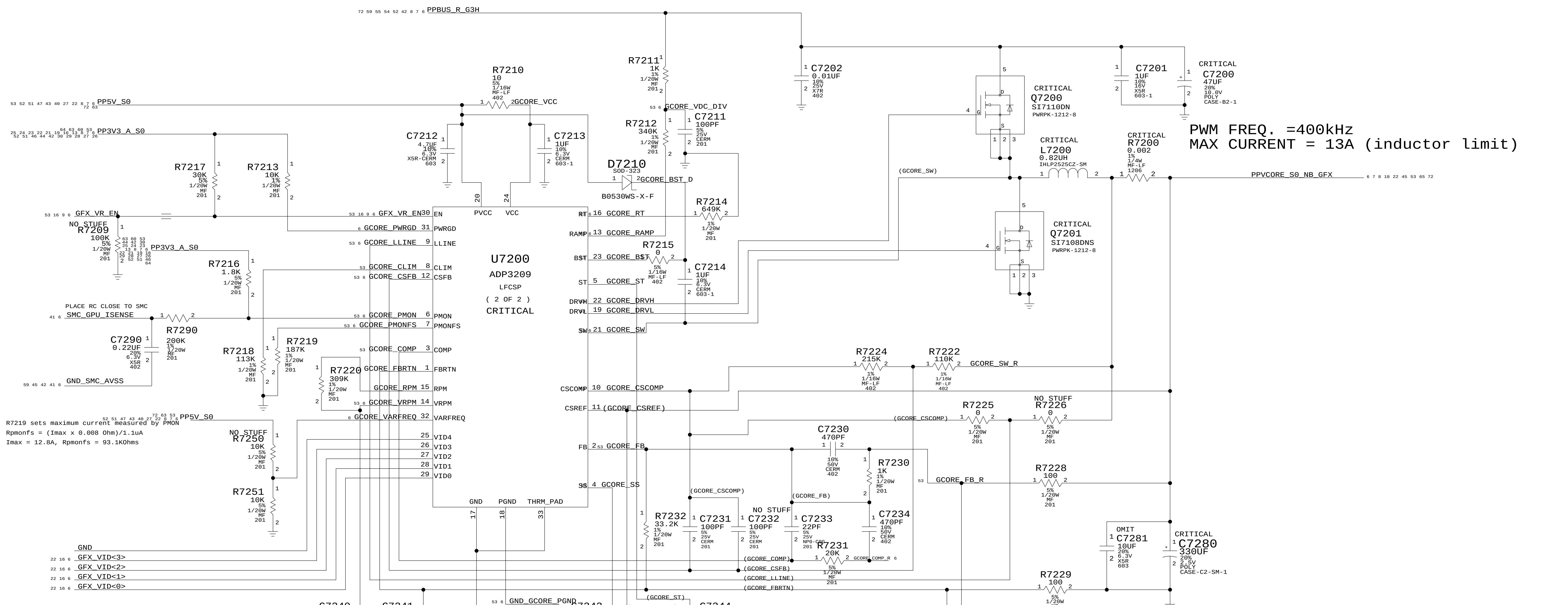
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE D DRAWING NUMBER 051-7230 REV. 8.0.0

SCALE NONE SHT 52 OF 73

RENDER VCORE POWER SUPPLY



NOTE: VID<4> is tied to GND

	4	3	2	1	0	VOLTAGE
VID	0	0	0	0	0	1.250V Each step is 0.025V
VID	0	0	0	0	1	1.225V
VID	0	0	0	1	0	1.200V
VID	0	0	0	1	1	1.175V
VID	0	0	1	0	0	1.150V
VID	0	0	1	0	1	1.125V
VID	0	0	1	1	0	1.100V
VID	0	0	1	1	1	1.075V
VID	0	1	0	0	0	1.050V
VID	0	1	0	0	1	1.025V
VID	0	1	0	1	0	1.000V
VID	0	1	0	1	1	0.975V
VID	0	1	1	0	0	0.950V
VID	0	1	1	0	1	0.925V
VID	0	1	1	1	0	0.900V
VID	0	1	1	1	1	0.875V

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GCORE_SW	0.6 MM	0.20 MM
GCORE_BST	0.3 MM	0.20 MM
GCORE_DRVH	0.6 MM	0.20 MM
GCORE_DRVL	0.6 MM	0.20 MM
GCORE_BST_D	0.3 MM	0.20 MM
GND_GCORE_PGND	0.6 MM	0.20 MM
GCORE_VDC_DIV	0.3 MM	0.20 MM
GCORE_RAMP	0.3 MM	0.20 MM
GCORE_CLIM	0.3 MM	0.20 MM
GCORE_SS	0.3 MM	0.20 MM
GCORE_ST	0.3 MM	0.20 MM
GCORE_SW_R	0.6 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GCORE_CSCOMP	0.3 MM	0.20 MM
GCORE_CSFB	0.3 MM	0.20 MM
GCORE_LLINE	0.3 MM	0.20 MM
GCORE_RT	0.3 MM	0.20 MM
GFX_VR_EN	0.3 MM	0.20 MM
GCORE_COMP	0.3 MM	0.20 MM
GCORE_FB	0.3 MM	0.20 MM
GCORE_FBRTN	0.3 MM	0.20 MM
GCORE_PMON	0.3 MM	0.20 MM
GCORE_PMONFS	0.3 MM	0.20 MM
GCORE_RPM	0.3 MM	0.20 MM
GCORE_VRPM	0.3 MM	0.20 MM
GCORE_FB_R	0.3 MM	0.20 MM

Render VCore Supplies

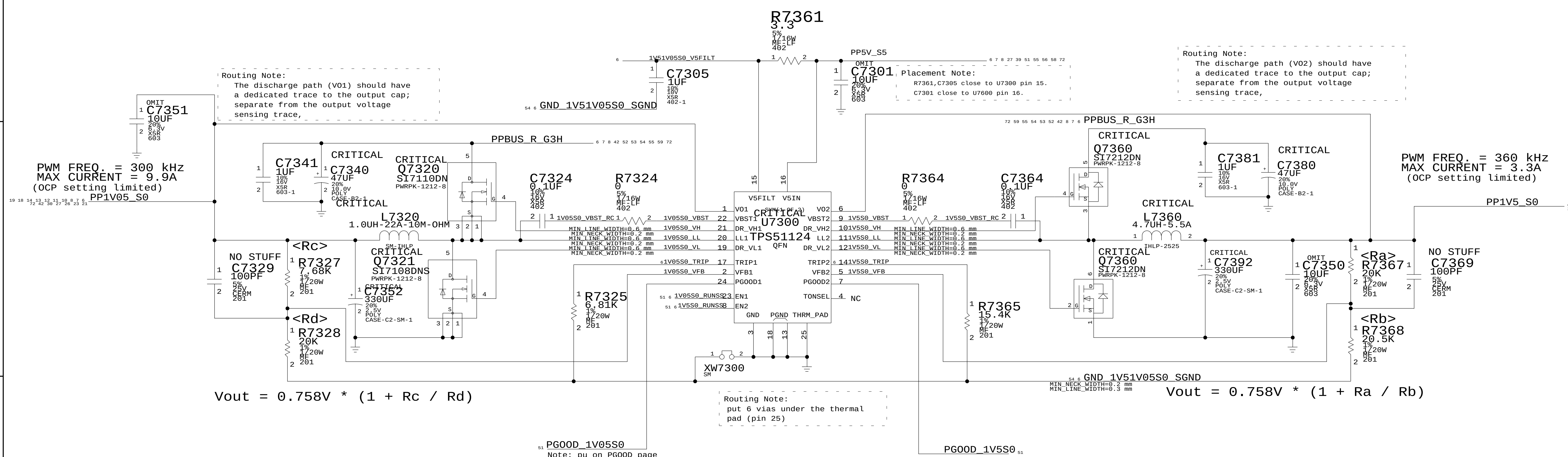
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 53	OF 73

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



1.5V/1.05V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

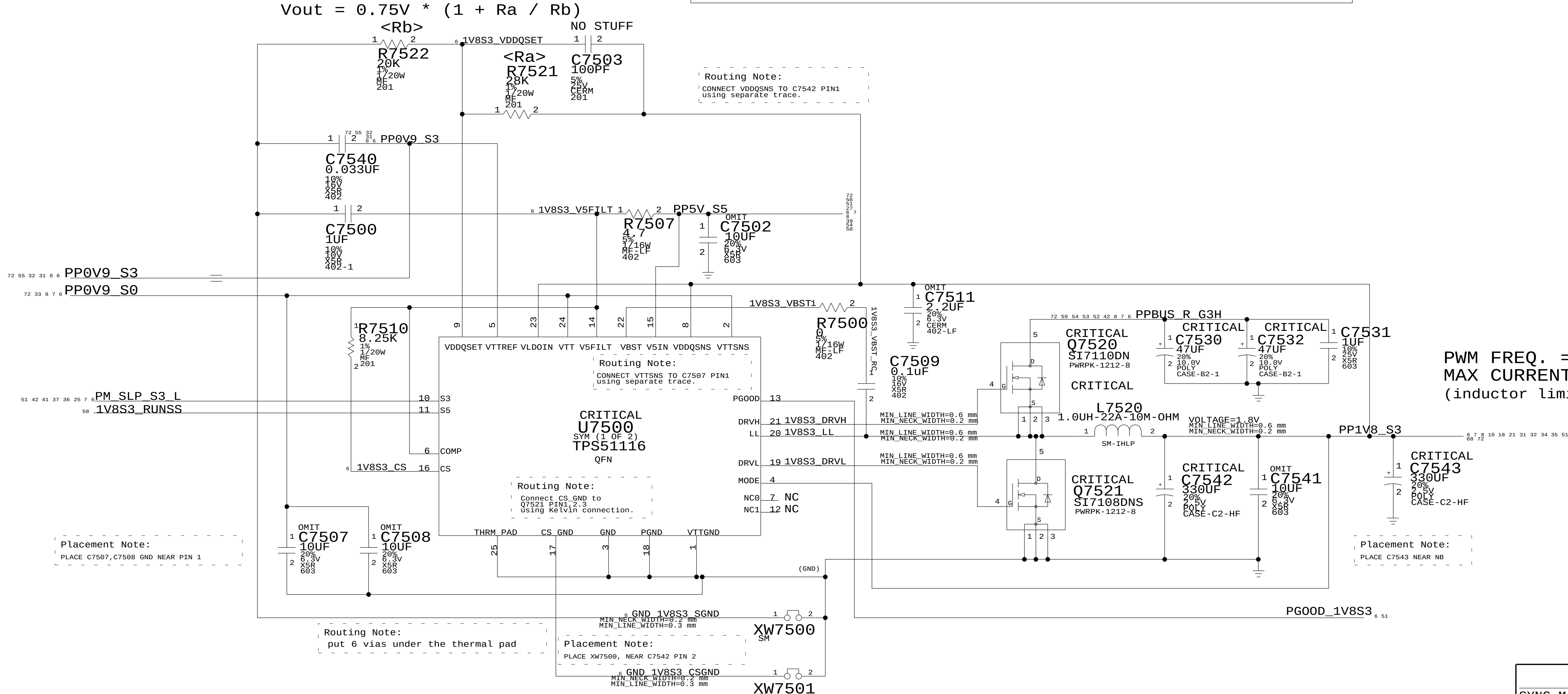
APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. 8.0.0

SCALE NONE | SHT 54 OF 73

1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



1.8V/0.9V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

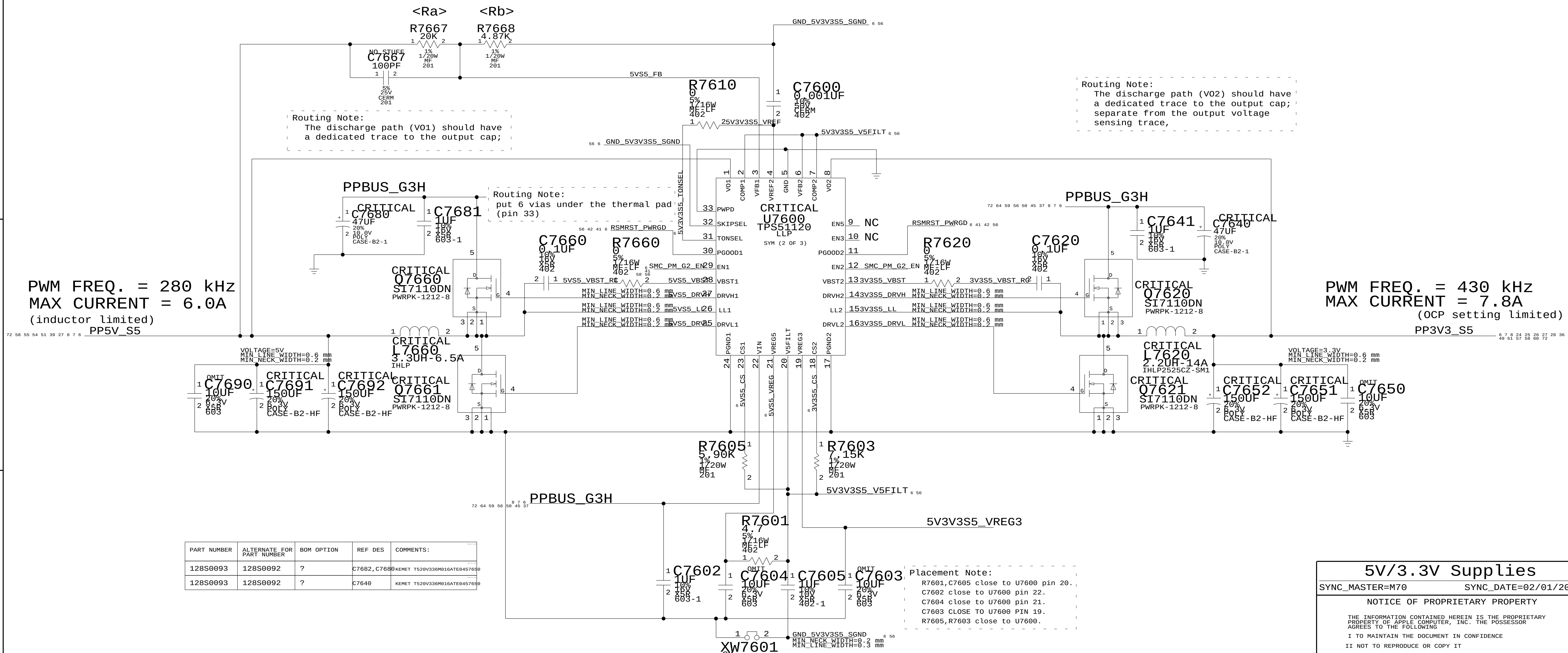
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 55 OF 73

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

Vout = 1V * (1 + Ra / Rb)
5.106V = 1V * (1 + 20K / 4.87K)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7680	KEMET T520V336M016ATE045765
128S0093	128S0092	?	C7640	KEMET T520V336M016ATE045765

5V/3.3V Supplies

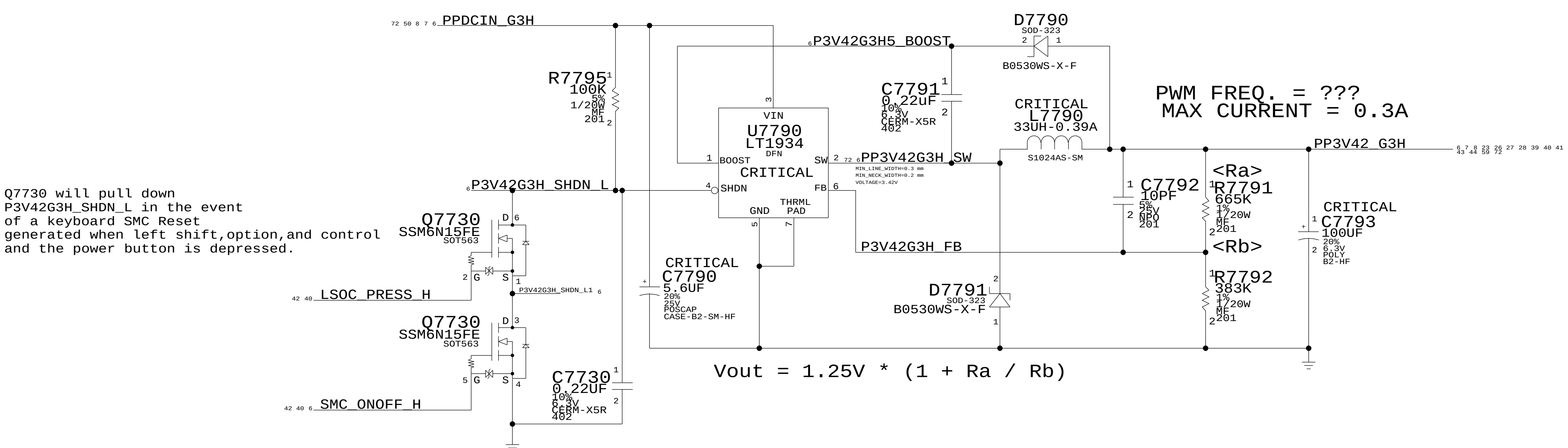
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

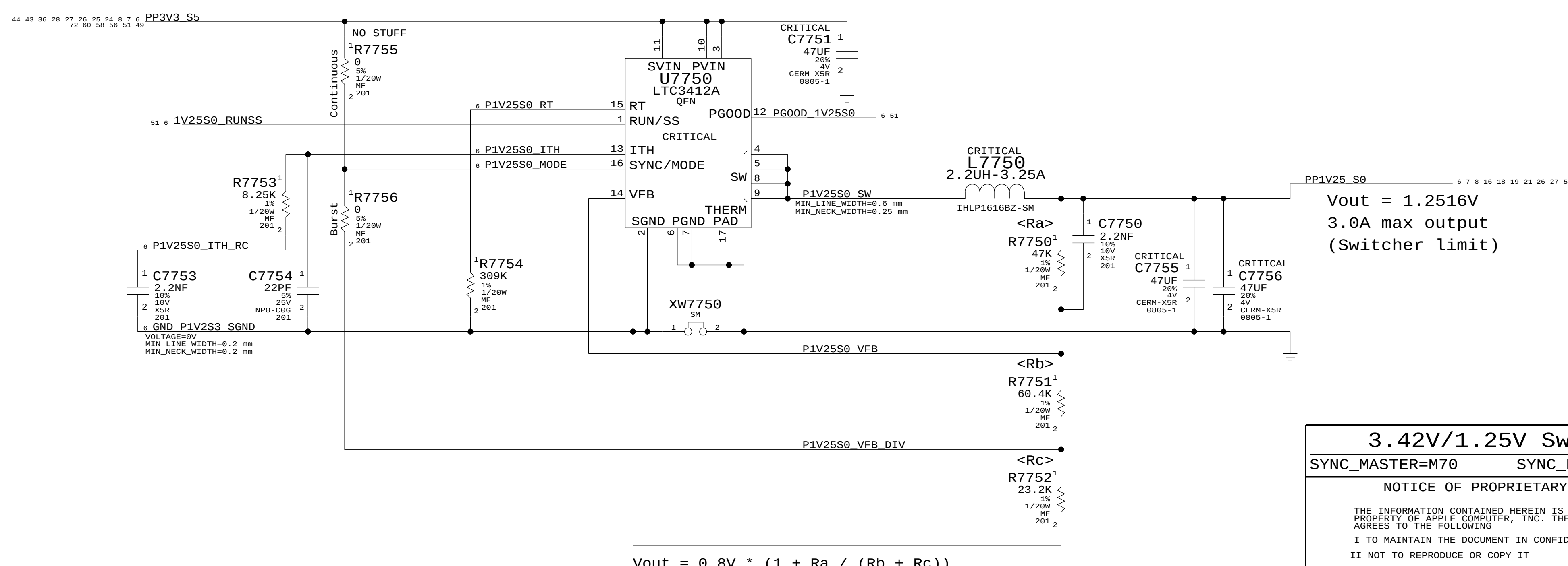
SIZE D DRAWING NUMBER 051-7230 REV. 8.0.0

SCALE NONE SHT 56 OF 73

3.425V G3H SUPPLY



1.25V S0 REGULATOR



3.42V/1.25V Switcher

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

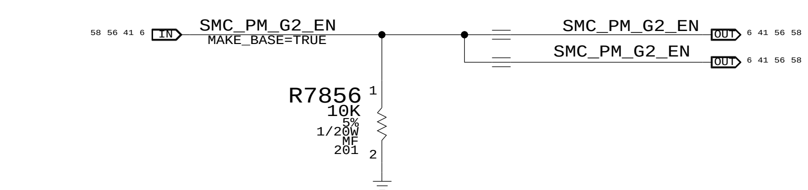
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

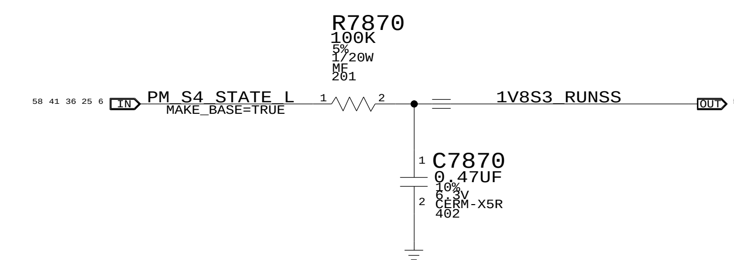
SCALE	SHT	OF
NONE	57	73

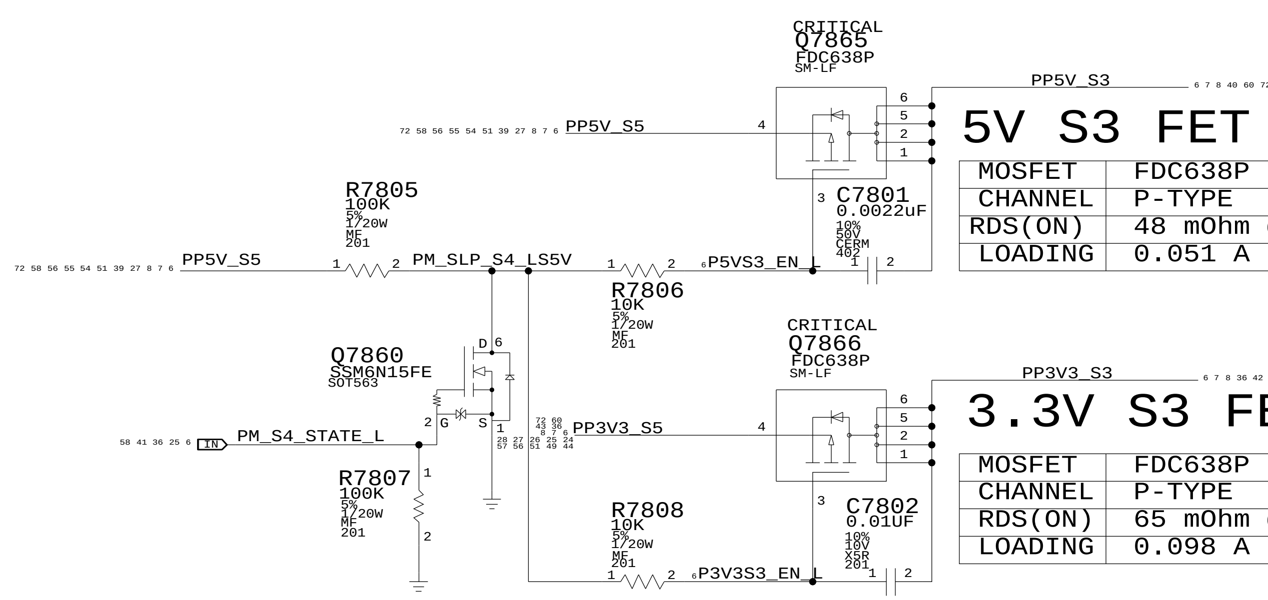
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL



1.8V S3 RUN/SS CONTROL





5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

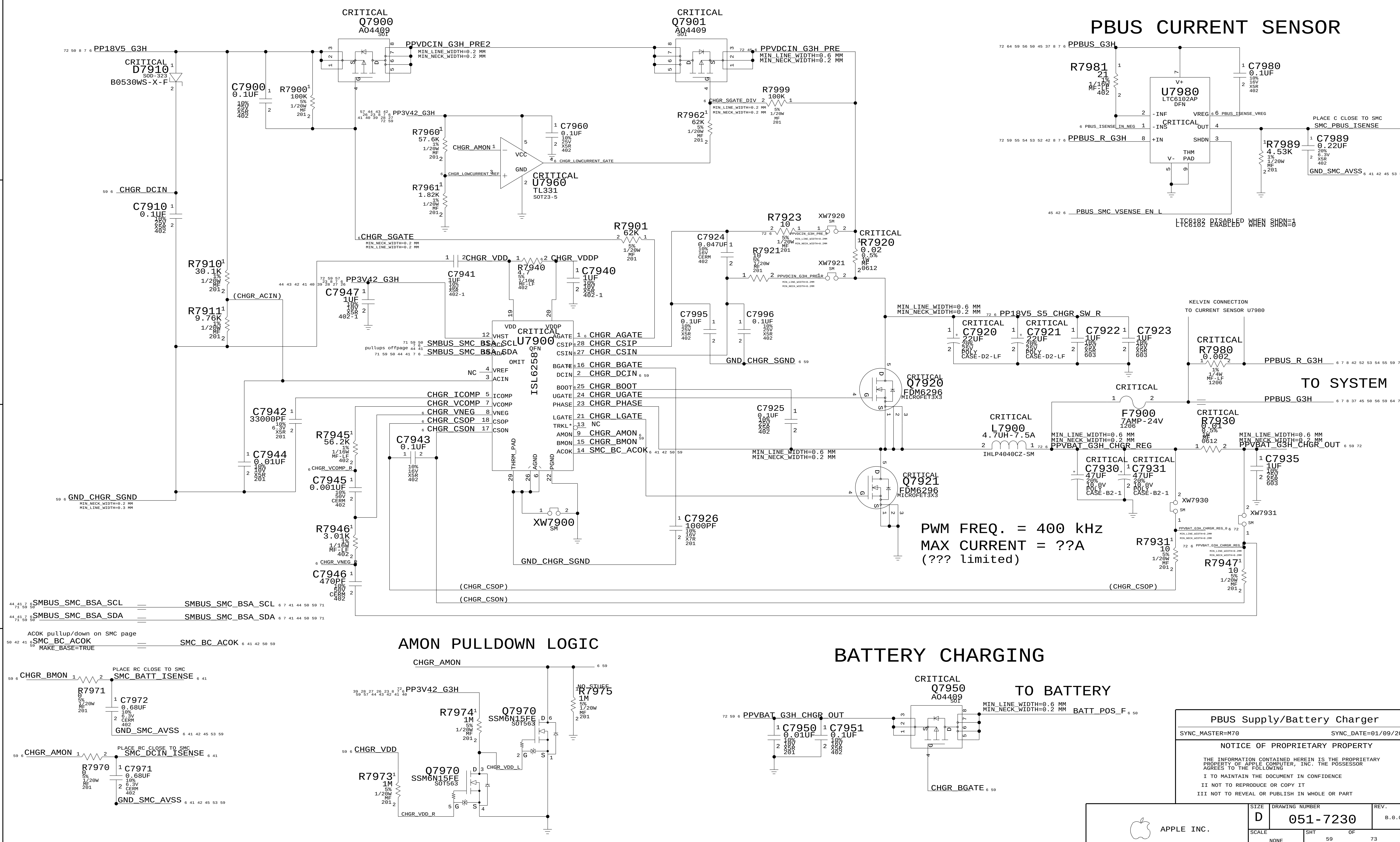
S3 FET & S3/S5 Control

SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE: NONE	SHT 58	OF 73

PBUS SUPPLY / BATTERY CHARGER



PBUS Supply/Battery Charger

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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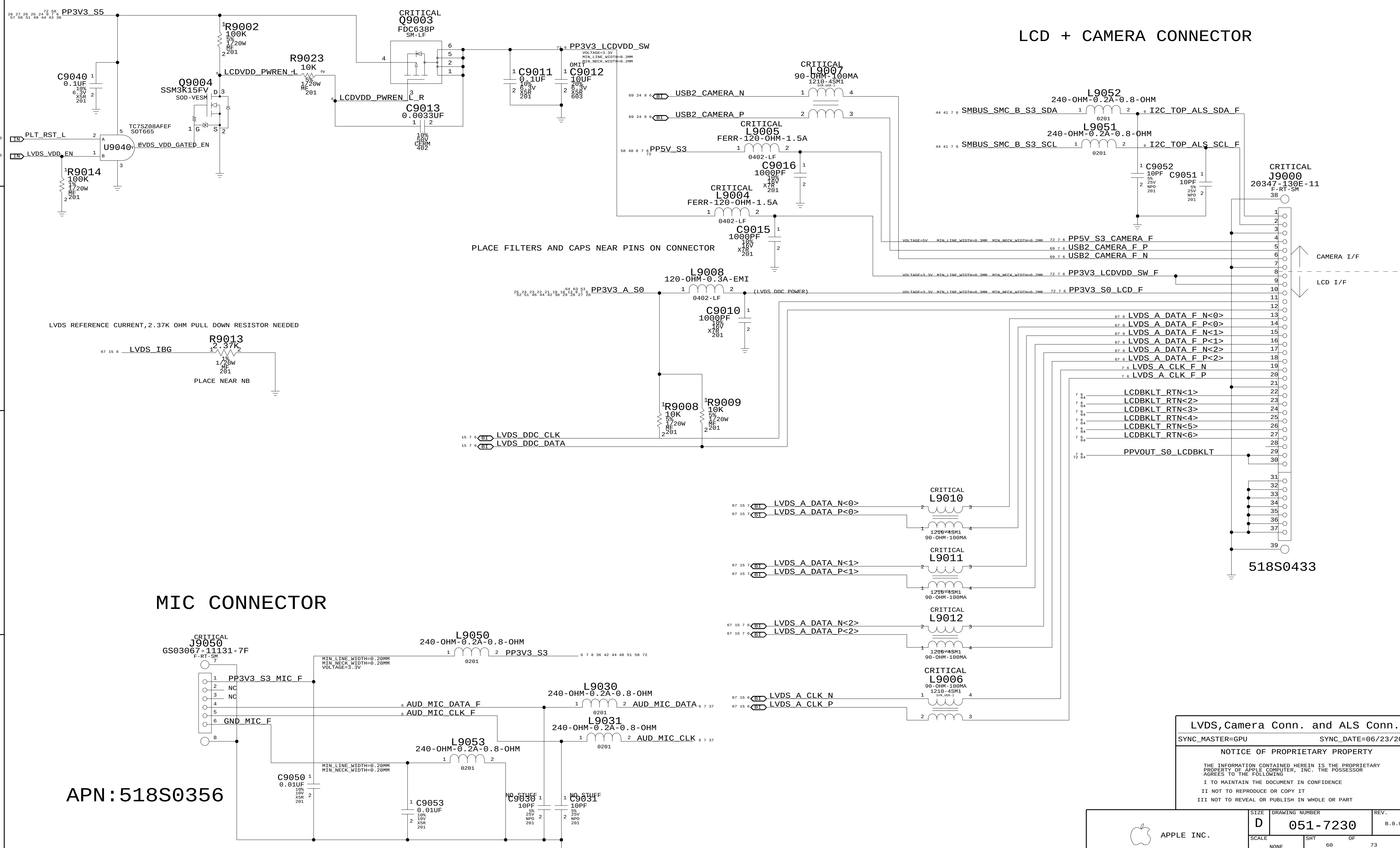
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 59 OF 73	



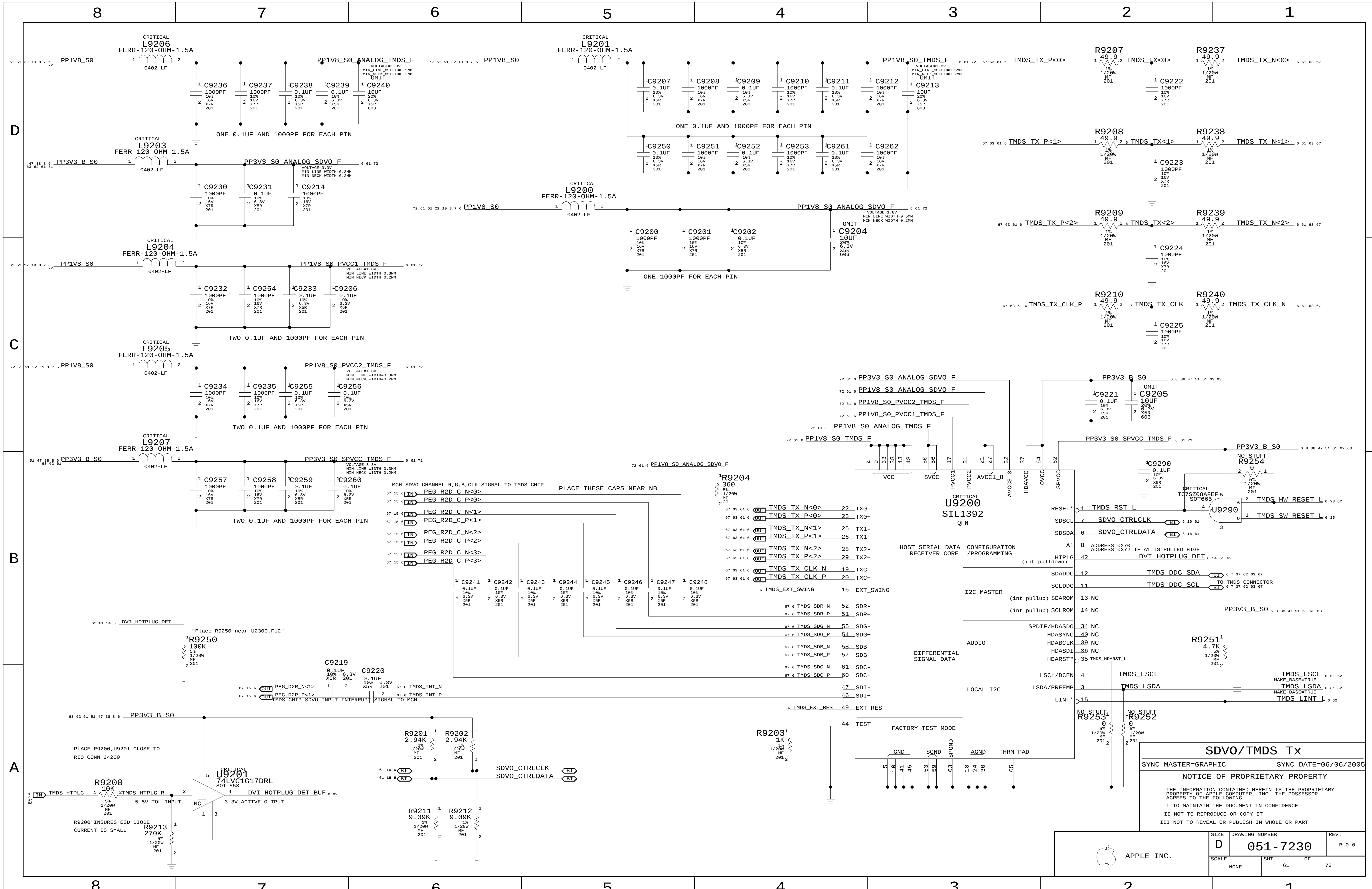
LVDS,Camera Conn. and ALS Conn.

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 60 OF 73



CRITICAL L9206 FERR-120-OHM-1.5A 0402-LF
PP1V8_S0
PP1V8_S0_ANALOG_TMDS_F
C9236 1000PF
C9237 1000PF
C9238 0.1UF
C9239 0.1UF
C9240 10UF OMIT
ONE 0.1UF AND 1000PF FOR EACH PIN
CRITICAL L9203 FERR-120-OHM-1.5A 0402-LF
PP3V3_B_S0
PP3V3_S0_ANALOG_SDVO_F
C9230 1000PF
C9231 0.1UF
C9214 1000PF
CRITICAL L9204 FERR-120-OHM-1.5A 0402-LF
PP1V8_S0_PVCC1_TMDS_F
C9232 1000PF
C9254 1000PF
C9233 0.1UF
C9206 0.1UF
TWO 0.1UF AND 1000PF FOR EACH PIN
CRITICAL L9205 FERR-120-OHM-1.5A 0402-LF
PP1V8_S0_PVCC2_TMDS_F
C9234 1000PF
C9235 1000PF
C9255 0.1UF
C9256 0.1UF
TWO 0.1UF AND 1000PF FOR EACH PIN
CRITICAL L9207 FERR-120-OHM-1.5A 0402-LF
PP3V3_S0_SPVCC_TMDS_F
C9257 1000PF
C9258 1000PF
C9259 0.1UF
C9260 0.1UF
TWO 0.1UF AND 1000PF FOR EACH PIN
CRITICAL L9201 FERR-120-OHM-1.5A 0402-LF
PP1V8_S0_TMDS_F
C9207 0.1UF
C9208 1000PF
C9209 0.1UF
C9210 1000PF
C9211 0.1UF
C9212 1000PF
C9213 10UF OMIT
ONE 0.1UF AND 1000PF FOR EACH PIN
C9250 0.1UF
C9251 1000PF
C9252 0.1UF
C9253 1000PF
C9261 0.1UF
C9262 1000PF
CRITICAL L9200 FERR-120-OHM-1.5A 0402-LF
PP1V8_S0_ANALOG_SDVO_F
C9200 1000PF
C9201 1000PF
C9202 0.1UF
C9204 10UF OMIT
ONE 1000PF FOR EACH PIN
R9207 49.9
R9237 49.9
TMDS_TX_P<0>
TMDS_TX<0>
TMDS_TX_N<0>
C9222 1000PF
R9208 49.9
R9238 49.9
TMDS_TX_P<1>
TMDS_TX<1>
TMDS_TX_N<1>
C9223 1000PF
R9209 49.9
R9239 49.9
TMDS_TX_P<2>
TMDS_TX<2>
TMDS_TX_N<2>
C9224 1000PF
R9210 49.9
R9240 49.9
TMDS_TX_CLK_P
TMDS_TX_CLK
TMDS_TX_CLK_N
C9225 1000PF
PP3V3_B_S0
C9221 0.1UF
C9205 10UF OMIT
MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PLACE THESE CAPS NEAR NB
PEG_R2D_C_N<0>
PEG_R2D_C_P<0>
PEG_R2D_C_N<1>
PEG_R2D_C_P<1>
PEG_R2D_C_N<2>
PEG_R2D_C_P<2>
PEG_R2D_C_N<3>
PEG_R2D_C_P<3>
C9241 C9242 C9243 C9244 C9245 C9246 C9247 C9248 0.1UF
R9204 360
CRITICAL U9200 SIL1392 QFN
HOST SERIAL DATA RECEIVER CORE
CONFIGURATION /PROGRAMMING
I2C MASTER
AUDIO
DIFFERENTIAL SIGNAL DATA
LOCAL I2C
FACTORY TEST MODE
TMDS_RST_L
SDVO_CTRLCLK
SDVO_CTRLDATA
ADDRESS=0X70
ADDRESS=0X72 IF A1 IS PULLED HIGH
DVI_HOTPLUG_DET
TMDS_DDC_SDA
TMDS_DDC_SCL
TO TMDS CONNECTOR
TMDS_LSCL
TMDS_LSDA
TMDS_LINT_L
MAKE_BASE=TRUE
CRITICAL TC7SZ08AFEF SOT665 U9290
TMDS_HW_RESET_L
TMDS_SW_RESET_L
C9290 0.1UF
R9254 0 NO STUFF
R9251 4.7K
R9253 0 NO STUFF
R9252 0 NO STUFF
R9203 1K
"Place R9250 near U2300.F12"
R9250 100K
C9219 0.1UF
C9220 0.1UF
PEG_D2R_N<1>
PEG_D2R_P<1>
TMDS_INT_N
TMDS_INT_P
TMDS CHIP SDVO INPUT INTERRUPT SIGNAL TO MCH
R9201 2.94K
R9202 2.94K
R9211 9.09K
R9212 9.09K
PLACE R9200,U9201 CLOSE TO RIO CONN J4200
R9200 10K
TMDS_HTPLG
TMDS_HTPLG_R
5.5V TOL INPUT
CRITICAL U9201 74LVC1G17DRL SOT-553
DVI_HOTPLUG_DET_BUF
3.3V ACTIVE OUTPUT
R9200 INSURES ESD DIODE CURRENT IS SMALL
R9213 270K
SDVO/TMDS Tx
SYNC_MASTER=GRAPHIC
SYNC_DATE=06/06/2005
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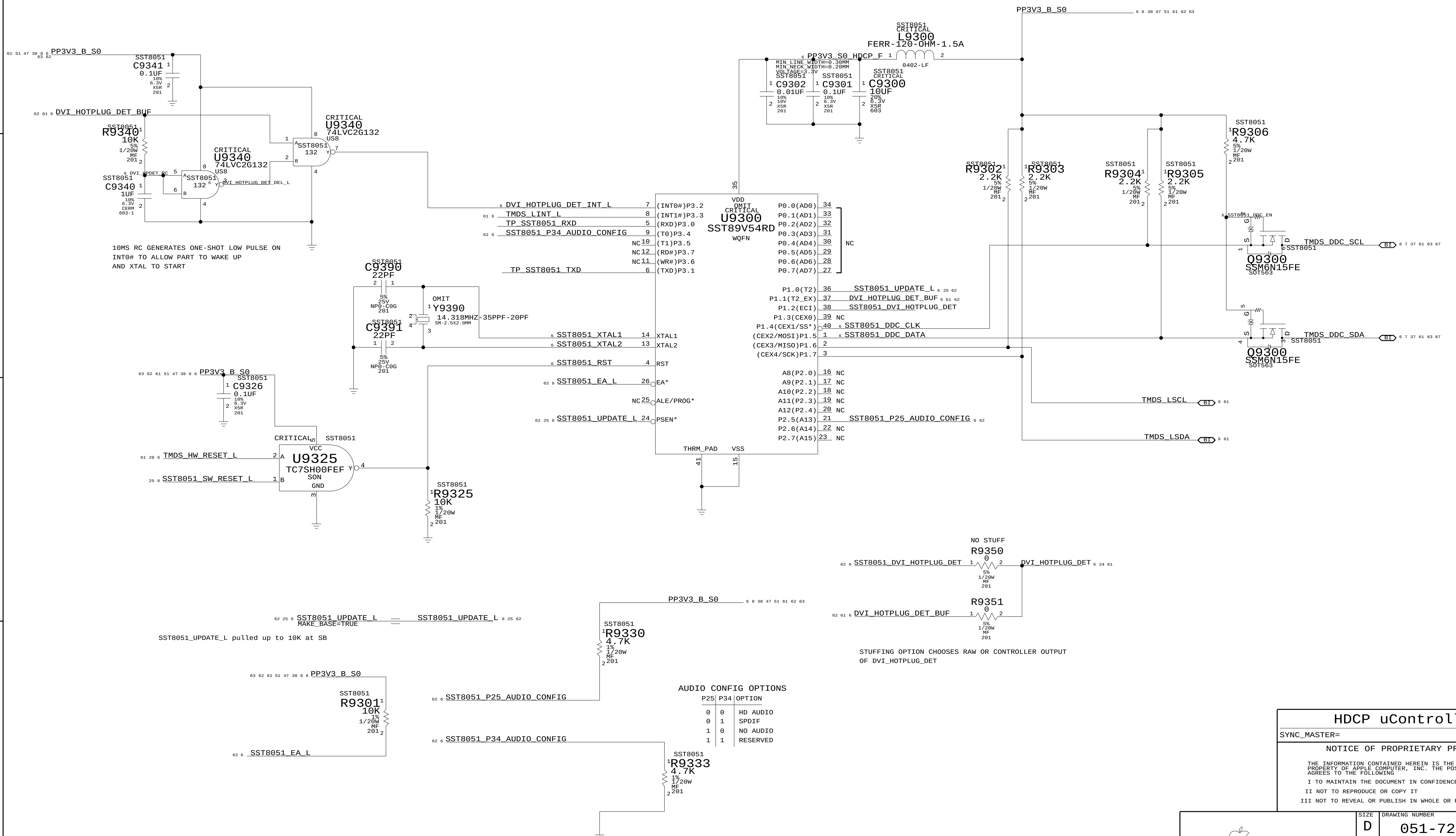
SIZE D
DRAWING NUMBER 051-7230
REV. 8.0.0
SCALE NONE
SHT 61 OF 73

SST8051 microcontroller for HDCP support



10MS RC GENERATES ONE-SHOT LOW PULSE ON
INT0# TO ALLOW PART TO WAKE UP
AND XTAL TO START

SST8051_UPDATE_L pulled up to 10K at SB

STUFFING OPTION CHOOSES RAW OR CONTROLLER OUTPUT
OF DVI_HOTPLUG_DET

AUDIO CONFIG OPTIONS

P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

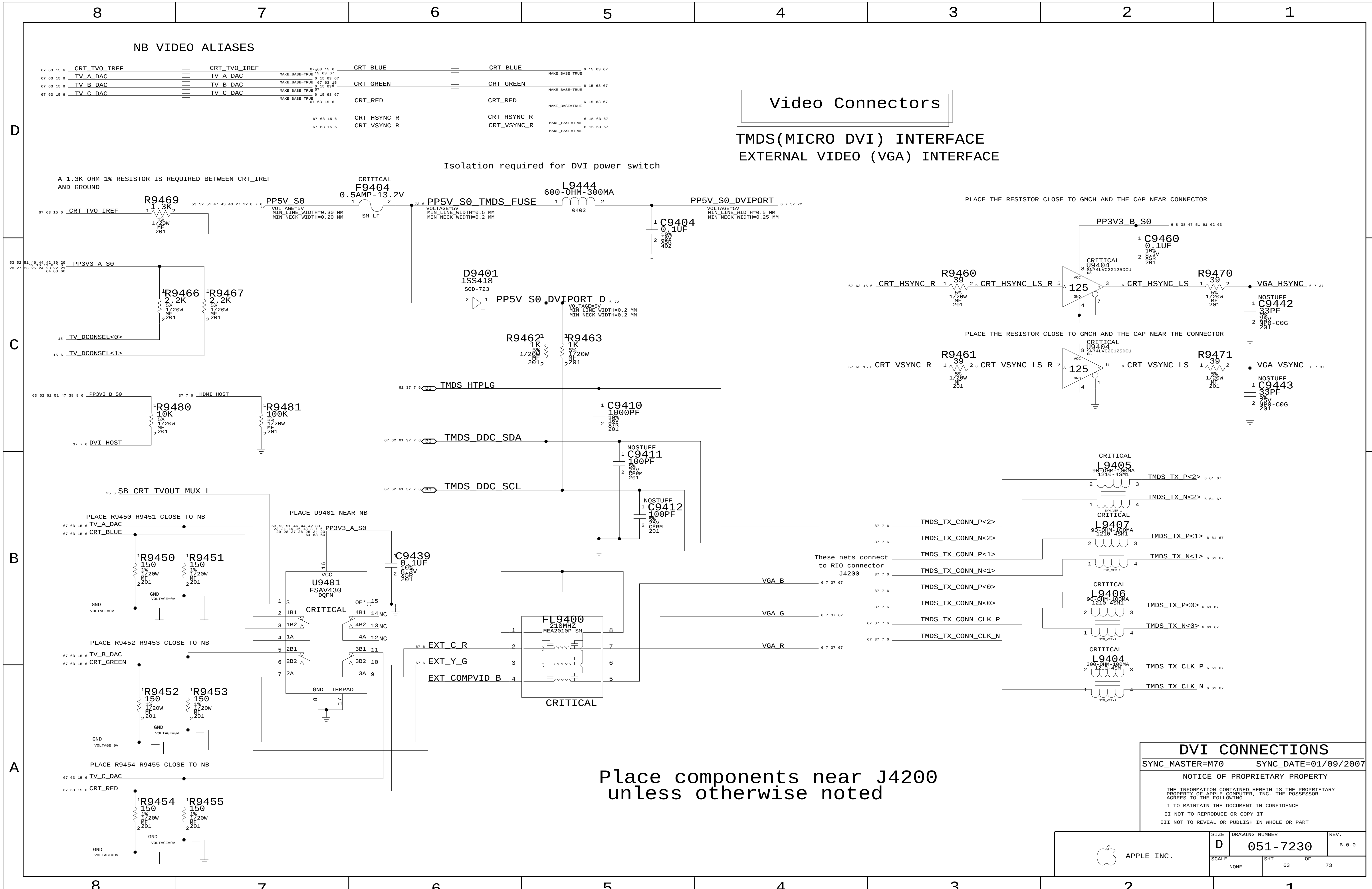
HDCP uController

SYNC_MASTER= SYNC_DATE=

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 62 OF 73


NB VIDEO ALIASES
Video Connectors
TMDS(MICRO DVI) INTERFACE
EXTERNAL VIDEO (VGA) INTERFACE
Isolation required for DVI power switch
A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF
AND GROUND
CRT_TVO_IREF
TV_A_DAC
TV_B_DAC
TV_C_DAC
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_HSYNC_R
CRT_VSYNC_R
MAKE_BASE=TRUE
R9469
1.3K
PP5V_S0
CRITICAL
F9404
0.5AMP-13.2V
SM-LF
PP5V_S0_TMDS_FUSE
L9444
600-OHM-300MA
0402
PP5V_S0_DVIPORT
C9404
0.1UF
VOLTAGE=5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM
PP3V3_A_S0
R9466
2.2K
R9467
2.2K
TV_DCONSEL<0>
TV_DCONSEL<1>
D9401
1SS418
SOD-723
PP5V_S0_DVIPORT_D
R9462
1K
R9463
1K
PP3V3_B_S0
HDMI_HOST
R9480
10K
R9481
100K
DVI_HOST
TMDS_HTPLG
C9410
1000PF
TMDS_DDC_SDA
NOSTUFF
C9411
100PF
TMDS_DDC_SCL
C9412
100PF
SB_CRT_TVOUT_MUX_L
PLACE R9450 R9451 CLOSE TO NB
PLACE U9401 NEAR NB
R9450
150
R9451
150
C9439
0.1UF
U9401
FSAV430
DQFN
CRITICAL
PLACE R9452 R9453 CLOSE TO NB
R9452
150
R9453
150
PLACE R9454 R9455 CLOSE TO NB
R9454
150
R9455
150
EXT_C_R
EXT_Y_G
EXT_COMPVID_B
FL9400
210MHZ
MEA2010P-SM
CRITICAL
VGA_B
VGA_G
VGA_R
These nets connect
to RIO connector
J4200
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR
C9460
0.1UF
U9404
SN74LVC2G125DCU
R9460
39
CRT_HSYNC_LS_R
R9470
39
CRT_HSYNC_LS
VGA_HSYNC
C9442
33PF
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR
R9461
39
CRT_VSYNC_LS_R
R9471
39
CRT_VSYNC_LS
VGA_VSYNC
C9443
33PF
L9405
90-OHM-100MA
1210-4SM1
TMDS_TX_P<2>
TMDS_TX_N<2>
L9407
TMDS_TX_P<1>
TMDS_TX_N<1>
L9406
TMDS_TX_P<0>
TMDS_TX_N<0>
L9404
300-OHM-100MA
1210-4SM
TMDS_CLK_P
TMDS_CLK_N
TMDS_TX_CONN_P<2>
TMDS_TX_CONN_N<2>
TMDS_TX_CONN_P<1>
TMDS_TX_CONN_N<1>
TMDS_TX_CONN_P<0>
TMDS_TX_CONN_N<0>
TMDS_TX_CONN_CLK_P
TMDS_TX_CONN_CLK_N
Place components near J4200
unless otherwise noted
DVI CONNECTIONS
SYNC_MASTER=M70
SYNC_DATE=01/09/2007
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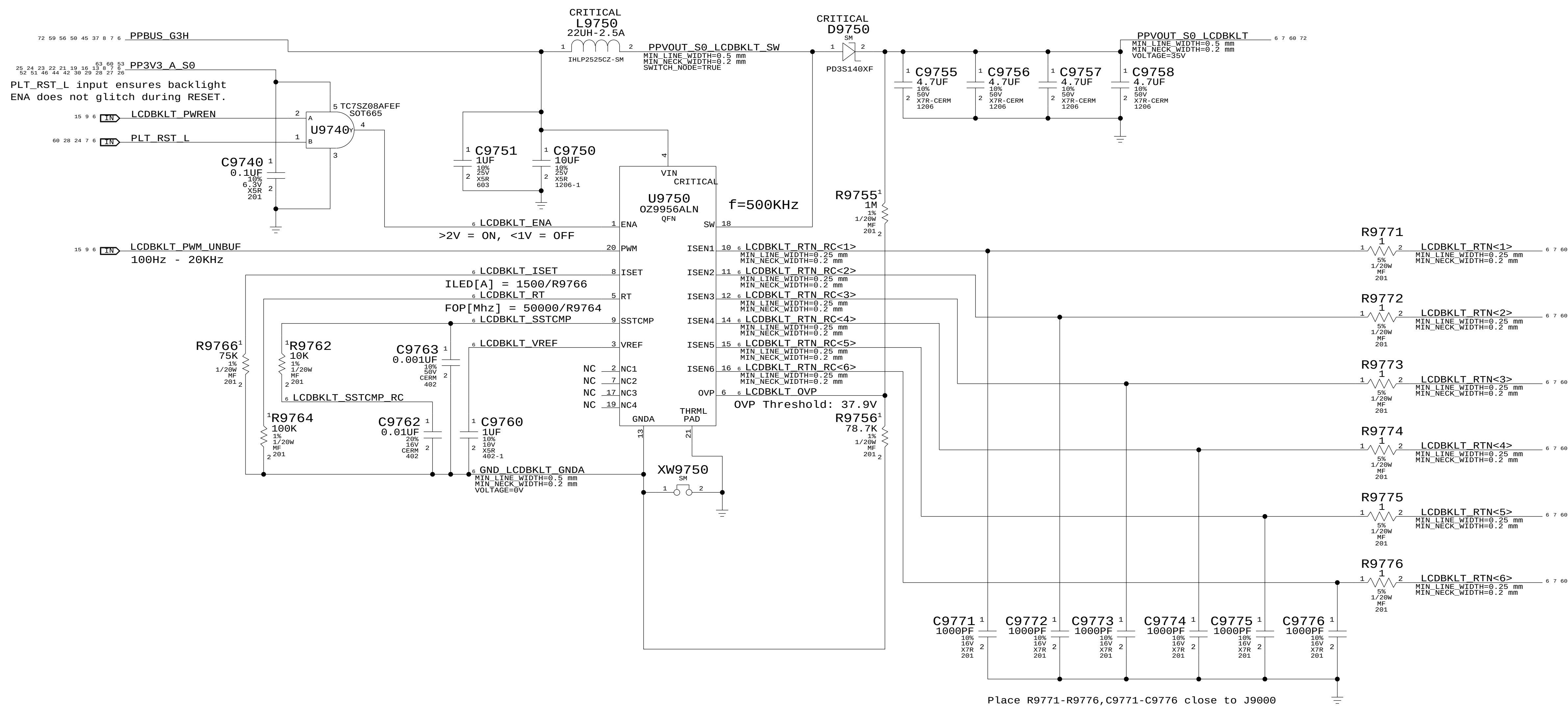
SIZE D
DRAWING NUMBER 051-7230
REV. 8.0.0
SCALE NONE
SHT 63 OF 73

LED Backlight Driver



LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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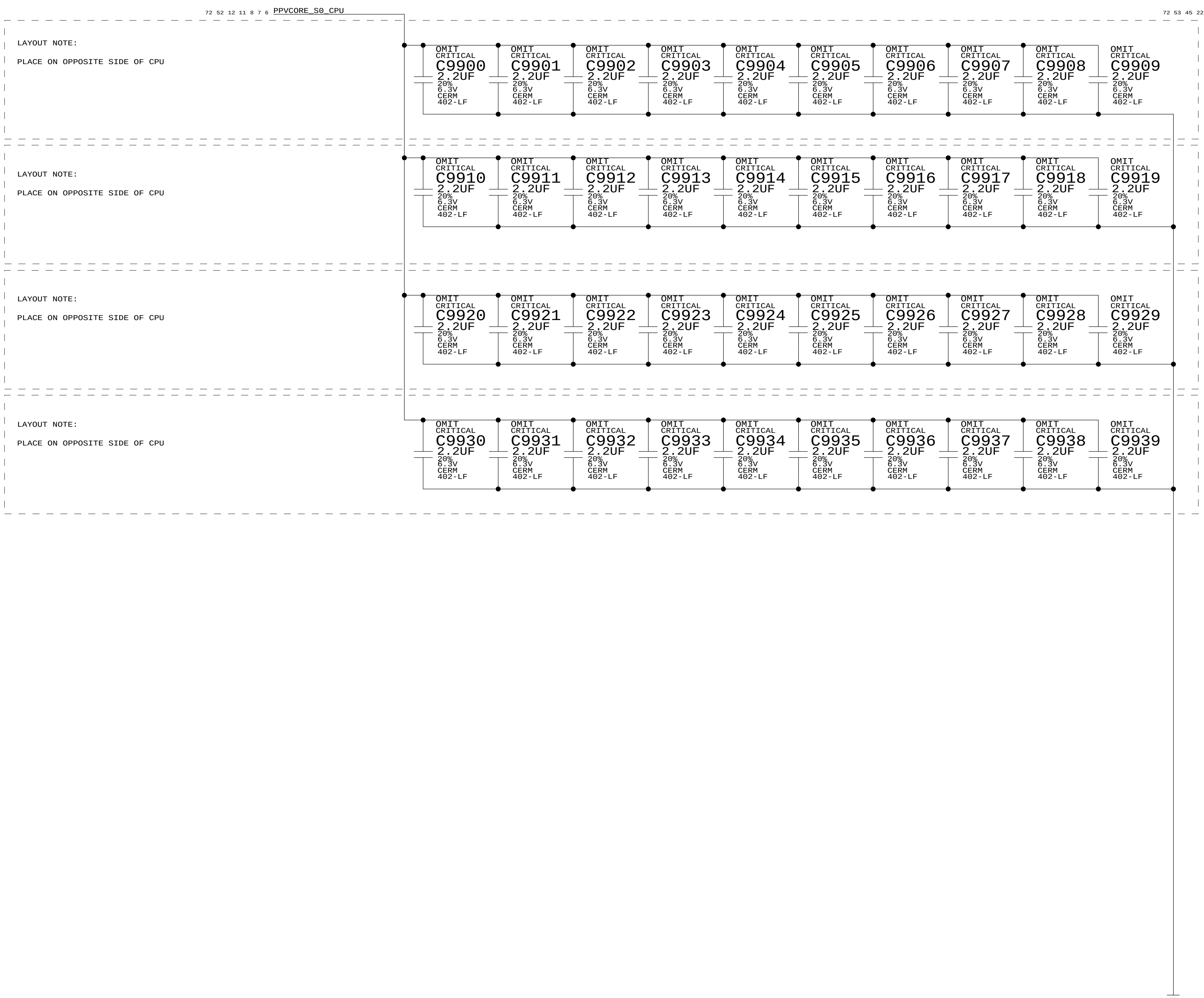
SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 64 OF 73

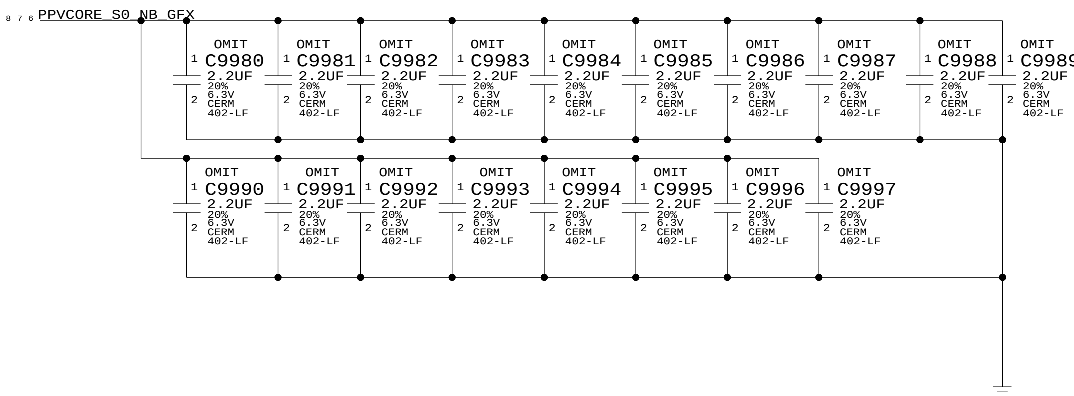
ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402



ADDITIONAL GPU VCORE HF DECOUPLING

18x 1uF 0402



Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 65	OF 73

8	7	6	5	4	3	2	1

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	ISL3,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_4MIL	*	0.100 MM	?
FSB_9MIL	*	0.228 MM	?
FSB_DATA	*	=FSB_4MIL	?
FSB_DATA2DATA	*	=FSB_4MIL	?
FSB_DSTB	*	=FSB_9MIL	?
FSB_DATA2DSTB	*	=FSB_9MIL	?
FSB_ADDR	*	=FSB_4MIL	?
FSB_ADDR2ADDR	*	=FSB_4MIL	?
FSB_ADSTB	*	=FSB_9MIL	?
FSB_ADDR2ADSTB	*	=FSB_9MIL	?
FSB_COMMON	*	=FSB_4MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which
Intel says to route with 7 mil spacing without
specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?
CPU_THERMD	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	6 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	6 10
CPU_FERR_L	CPU_55S		CPU_FERR_L	6 10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	6 10 42 52
CPU_PWRGD	CPU_55S		CPU_PWRGD	6 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	6 10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	6 10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	6 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_SMI_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	6 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	6 10 16 23 42
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	6 16 25 52
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	6 52
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	6 7 13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	6 7 13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	6 7 13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	6 10 16 23 52
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	6 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	6 7 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	6 7 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	6 7 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	6 7 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	6 7 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	6 7 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	6 7 10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 71
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 71
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	6 7 13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	6 11 12 52
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	6 11 52
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	6 11 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	6 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	6 52
	CPU_70D	CPU_THERMD	CPU_THERMD_P	6 10 46
	CPU_70D	CPU_THERMD	CPU_THERMD_N	6 10 46

CPU/FSB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 66	OF 73

8	7	6	5	4	3	2	1

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
PCIE_R2D_2_PCIE_R2D	*	0.228 MM	?
PCIE_D2R_2_PCIE_D2R	*	0.228 MM	?
PCIE_R2D_2_PCIE_D2R	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_N2S_2_DMI_N2S	*	0.228 MM	?
DMI_S2N_2_DMI_S2N	*	0.228 MM	?
DMI_N2S_2_DMI_S2N	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_R2D_2_PCIE_R2D
PCIE_D2R	PCIE_D2R	*	PCIE_D2R_2_PCIE_D2R
PCIE_R2D	PCIE_D2R	*	PCIE_R2D_2_PCIE_D2R

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_N2S_2_DMI_N2S
DMI_S2N	DMI_S2N	*	DMI_S2N_2_DMI_S2N
DMI_N2S	DMI_S2N	*	DMI_N2S_2_DMI_S2N

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	
LVDS2LVDS	*	0.300 MM	?	
TMDS	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC
LVDS	LVDS	*	LVDS2LVDS

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
PEG_R2D	PCIE_100D	PCIE_R2D	PEG_R2D_P<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_N<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_C_P<15..0>	6 15 61
	PCIE_100D	PCIE_R2D	PEG_R2D_C_N<15..0>	6 15 61
PEG_D2R	PCIE_100D	PCIE_D2R	PEG_D2R_P<15..0>	6 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_N<15..0>	6 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_C_P<15..0>	
	PCIE_100D	PCIE_D2R	PEG_D2R_C_N<15..0>	
DMI_N2S	DMI_100D	DMI_N2S	DMI_N2S_P<3..0>	6 16 24
	DMI_100D	DMI_N2S	DMI_N2S_N<3..0>	6 16 24
DMI_S2N	DMI_100D	DMI_S2N	DMI_S2N_P<3..0>	6 16 24
	DMI_100D	DMI_S2N	DMI_S2N_N<3..0>	6 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	6 15 60
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	6 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_P<2..0>	6 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_N<2..0>	6 60
LVDS_A_DATA3	LVDS_100D	LVDS	NC_LVDS_A_DATA_P3	9
LVDS_A_DATA3	LVDS_100D	LVDS	NC_LVDS_A_DATA_N3	9
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_P	9 15
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_N	9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	
LVDS_B_DATA3	LVDS_100D	LVDS	NC_LVDS_B_DATA_P3	9
LVDS_B_DATA3	LVDS_100D	LVDS	NC_LVDS_B_DATA_N3	9
LVDS_IBG		LVDS	LVDS_IBG	6 15 60
CRT_TVO_IREF		CRT	CRT_TVO_IREF	6 15 63
CRT_RED	CRT_50S	CRT	CRT_RED	6 15 63
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	6 15 63
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	6 15 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	6 15 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	6 15 63
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	6 15 63
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	6 15 63
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	6 15 63
EXT_COMPVID_B	CRT_50S	CRT	EXT_COMPVID_B	6 63
EXT_Y_G	CRT_50S	CRT	EXT_Y_G	6 63
EXT_C_R	CRT_50S	CRT	EXT_C_R	6 63
VGA_R	CRT_50S	CRT	VGA_R	6 7 37 63
VGA_G	CRT_50S	CRT	VGA_G	6 7 37 63
VGA_B	CRT_50S	CRT	VGA_B	6 7 37 63
	PCIE_100D	PCIE_R2D	TMDS_SDB_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDB_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CLK_P	6 61 63
	TMDS_100D	TMDS	TMDS_TX_CLK_N	6 61 63
	PCIE_100D	PCIE_D2R	TMDS_INT_P	6 61
	PCIE_100D	PCIE_D2R	TMDS_INT_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_P	6 7 37 63
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_N	6 7 37 63
	TMDS_100D	TMDS	TMDS_CONN_P<3..0>	
	TMDS_100D	TMDS	TMDS_CONN_N<3..0>	
	TMDS_100D	TMDS	TMDS_TX_P<3..0>	6 61 63
	TMDS_100D	TMDS	TMDS_TX_N<3..0>	6 61 63
	SMB_55S	SMB	TMDS_DDC_SCL	6 7 37 61 62 63
	SMB_55S	SMB	TMDS_DDC_SDA	6 7 37 61 62 63

NB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 67	OF 73

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	ISL3,ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_87D	*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	NB_STATIC	*	PWR_P2MM
MEM_CTRL	NB_STATIC	*	PWR_P2MM
MEM_DATA	NB_STATIC	*	PWR_P2MM
MEM_DQS	NB_STATIC	*	PWR_P2MM
MEM_CMD	NB_STATIC	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

	Net	Property	Pages
I93	PP0V9_S3M_MEM_NBVREFB	NET_SPACING_TYPE=NB_STATIC	8 16 21
I95	PP0V9_S3M_MEM_NBVREFA	NET_SPACING_TYPE=NB_STATIC	8 16 21
I94	NB_VCCSM_LF1	NET_SPACING_TYPE=NB_STATIC	6 18
I96	NB_VCCSM_LF2	NET_SPACING_TYPE=NB_STATIC	6 18
I97	NB_VCCSM_LF3	NET_SPACING_TYPE=NB_STATIC	6 18
I98	NB_VCCSM_LF4	NET_SPACING_TYPE=NB_STATIC	6 18
I99	NB_VCCSM_LF5	NET_SPACING_TYPE=NB_STATIC	6 18
I101	NB_VCCSM_LF6	NET_SPACING_TYPE=NB_STATIC	6 18
I103	NB_VCCSM_LF7	NET_SPACING_TYPE=NB_STATIC	6 18
I102	PP1V8_S3	NET_SPACING_TYPE=PP1V8_MEM	6 7 8 16 18 21 31 32 34 35 51 55 72
	GND	NET_SPACING_TYPE=GND	

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	Net	Pages
	MEM_87D	MEM_CLK	MEM_CLK_P<2..0>	16 31 33
	MEM_87D	MEM_CLK	MEM_CLK_N<2..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	6 16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<13..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	17 31
	MEM_87D	MEM_CLK	MEM_CLK_P<5..3>	16 32 33
	MEM_87D	MEM_CLK	MEM_CLK_N<5..3>	16 32 33
	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	6 16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<13..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	17 32

Memory Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE	SHT	OF
NONE	68	73

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	PWR	*	BUS2PWR_GND
USB	GND	*	BUS2PWR_GND

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	6 23 38
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	6 23 38
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	6 23 38
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	6 23 38
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	6 23 38
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	
SATA_A_R2D	SATA_100D	SATA	NC_SATA_A_R2D_C_P	9 23
	SATA_100D	SATA	NC_SATA_A_R2D_C_N	9 23
	SATA_100D	SATA	SATA_A_R2D_P	
	SATA_100D	SATA	SATA_A_R2D_N	
SATA_A_D2R	SATA_100D	GND	NC_SATA_A_D2R_P	9
	SATA_100D	GND	NC_SATA_A_D2R_N	9
	SATA_100D	SATA	SATA_A_D2R_C_P	
	SATA_100D	SATA	SATA_A_D2R_C_N	
SATA_B_R2D	SATA_100D	SATA	NC_SATA_B_R2D_C_P	9 23
	SATA_100D	SATA	NC_SATA_B_R2D_C_N	9 23
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_A_D2R	SATA_100D	GND	NC_SATA_B_D2R_P	9
	SATA_100D	GND	NC_SATA_B_D2R_N	9
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	NC_SATA_C_R2D_C_P	9 23
	SATA_100D	SATA	NC_SATA_C_R2D_C_N	9 23
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_A_D2R	SATA_100D	GND	NC_SATA_C_D2R_P	9
	SATA_100D	GND	NC_SATA_C_D2R_N	9
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIAS	SATA_55S		SATA_RBIAS	
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	6 7 9 23 37
	HDA_55S	HDA	HDA_BIT_CLK_R	6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	6 7 9 23 37
	HDA_55S	HDA	HDA_SYNC_R	6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	6 9 23 37
	HDA_55S	HDA	HDA_RST_L_R	6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	6 7 9 23 37
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	6 7 9 23 37
	HDA_55S	HDA	HDA_SDOUT_R	6 23
USB_EXTA	USB_90D	USB	USB2_EXTA_P	6 9 24 39
	USB_90D	USB	USB2_EXTA_N	6 9 24 39
	USB_90D	USB	USB2_MUXED_EXTA_N	6 9 39
	USB_90D	USB	USB2_MUXED_EXTA_P	6 9 39
USB_MINI	USB_90D	USB	USB2_AIRPORT_P	6 9 24 36
	USB_90D	USB	USB2_AIRPORT_N	6 9 24 36
USB_EXTD	USB_90D	USB	TP_USB2_3G_P	9 24
	USB_90D	USB	TP_USB2_3G_N	9 24
USB_CAMERA	USB_90D	USB	USB2_CAMERA_P	6 9 24 60
	USB_90D	USB	USB2_CAMERA_N	6 9 24 60
USB_BT	USB_90D	USB	NC_USB_BT_P	9 24
	USB_90D	USB	NC_USB_BT_N	9 24
USB_TPAD	USB_90D	USB	USB2_WSPRING_P	6 7 9 24 40
	USB_90D	USB	USB2_WSPRING_N	6 7 9 24 40
USB_IR	USB_90D	USB	USB_IR_P	6 7 9 24 40
	USB_90D	USB	USB_IR_N	6 7 9 24 40
USB_EXTB	USB_90D	USB	NC_USB2_EXTB_P	9 24
	USB_90D	USB	NC_USB2_EXTB_N	9 24
USB_EXCARD	USB_90D	USB	TP_USB_EXCARD_P	9 24
	USB_90D	USB	TP_USB_EXCARD_N	9 24
USB_EXTC	USB_90D	USB	TP_USB_EXTC_P	9 24
	USB_90D	USB	TP_USB_EXTC_N	9 24
	USB_90D	USB	USB2_AIRPORT_P_F	6 36
	USB_90D	USB	USB2_AIRPORT_N_F	6 36
	USB_90D	USB	USB2_CAMERA_F_P	6 7 60
	USB_90D	USB	USB2_CAMERA_F_N	6 7 60
	USB_90D	USB	USB2_EXTA_F_P	6 7 37 39
	USB_90D	USB	USB2_EXTA_F_N	6 7 37 39
			USB2_3G_F_P	
			USB2_3G_F_N	
USB_RBIAS	USB_60S		USB_RBIAS	6 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL	6 25 29 44
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA	6 25 29 44
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL	6 25 44
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA	6 25 44
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	6 24 49
	SPI_55S	SPI	SPI_SCLK	
	SPI_55S	SPI	SPI_A_SCLK_R	6 43 49
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	6 24 49
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	6 43 49
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	6 24 43 49
	SPI_55S	SPI	SPI_A_SO_R	6 49
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	6 24 49
	SPI_55S	SPI	SPI_CE_L<0>	6 43 49
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	6 24 43
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 69	OF 73

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
PCI_AD	PCI_55S	PCI	PCI_AD<18..0>	9
PCI_AD19	PCI_55S	PCI	NC_PCI_AD<19>	9 24
PCI_AD20	PCI_55S	PCI	NC_PCI_AD<20>	9 24
PCI_AD	PCI_55S	PCI	PCI_AD<31..21>	9
PCI_AD	PCI_55S	PCI	NC_PCI_PAR	9 24
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	9
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	6 24
PCI_LOCK_L	PCI_55S	PCI	PCI_LOCK_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	6 24
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	6 24
PCI_FW_REQ_L	PCI_55S	PCI	PCI_FW_REQ_L	6 24
PCI_FW_GNT_L	PCI_55S	PCI	PCI_FW_GNT_L	6 24
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	6 24
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI_REQ2_L	6 24
PCI_GNT2_L	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	6 24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	6 24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	6 24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	6 24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	6 24
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	6 24
PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_P	
	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_N	
PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_P	
	PCIE_100D	PCIE_D2R	PCIE_A_D2R_N	
PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_P	
	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_N	
PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_P	
	PCIE_100D	PCIE_D2R	PCIE_B_D2R_N	
			PCIE_EXCARD_R2D_C_P	
			PCIE_EXCARD_R2D_C_N	
			PCIE_EXCARD_D2R_P	
			PCIE_EXCARD_D2R_N	
			PCIE_FW_R2D_C_P	
			PCIE_FW_R2D_C_N	
			PCIE_FW_D2R_P	
			PCIE_FW_D2R_N	
PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_E_R2D_C_P	6 24 36
	PCIE_100D	PCIE_R2D	PCIE_E_R2D_C_N	6 24 36
PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_E_D2R_P	6 24 36
	PCIE_100D	PCIE_D2R	PCIE_E_D2R_N	6 24 36
			PCIE_ENET_R2D_C_P	
			PCIE_ENET_R2D_C_N	
			PCIE_ENET_D2R_P	
			PCIE_ENET_D2R_N	
GLAN_COMP			GLAN_COMP	6 23
ENET_KBIAS			NINEVEH_KBIAS_P	
ENET_RBIAS			NINEVEH_RBIAS	
(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_P	
	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_N	
(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_P	
	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_N	
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC	
ENET_LAN	LAN_55S	ENET_LAN	LAN_R2D<2..0>	
ENET_LAN	LAN_55S	ENET_LAN	LAN_D2R<2..0>	
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK_R	
	LAN_55S	ENET_CLK	ENET_GLAN_CLK	
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	6 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	6 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	6 16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	6 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	6 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	6 25

SB Constraints (2 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 70	OF 73

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	PWR	*	BUS2PWR_GND
CLK_FSB	GND	*	BUS2PWR_GND
CLK_PCIE	PWR	*	BUS2PWR_GND
CLK_PCIE	GND	*	BUS2PWR_GND
CLK_MED	PWR	*	BUS2PWR_GND
CLK_MED	GND	*	BUS2PWR_GND

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	6 29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	6 29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6 30 43
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	6 24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	6 30 41
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	6 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	6 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	6 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	6 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_P	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_N	
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	6 7 36 40 41 44
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	6 7 36 40 41 44
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	6 7 41 44 46
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	6 7 41 44 46
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	6 7 41 44 50 59
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	6 7 41 44 50 59
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	6 41 44 48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	6 41 44 48

Clock & SMC Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. 8.0.0

SCALE NONE | SHT 71 OF 73

I1	PPBUS_G3H	NET_SPACING_TYPE=PWR	6 7 8 37 45 50 56 59 64
I2	PPBUS_R_G3H	NET_SPACING_TYPE=PWR	6 7 8 42 52 53 54 55 59
I3	PPDCIN_G3H	NET_SPACING_TYPE=PWR	6 7 8 50 57
I4	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR	6 50
I5	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR	6 50
I6	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR	6 59
I7	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR	6 59
I8	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR	6 59
I10	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR	6 59
I9	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR	6 7 8 11 12 52 65
I12	PPVCORE_S0_NB_GFX	NET_SPACING_TYPE=PWR	6 7 8 18 22 45 53 65
I11	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR	6 45 59
I13	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR	6 59
I14	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR	6 59
I16	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR	6 59
I15	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR	6 52
I18	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR	6 7 60 64
I17	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR	6 64
I19	PP0V9_S0	NET_SPACING_TYPE=PWR	6 7 8 33 55
I21	PP0V9_S3	NET_SPACING_TYPE=PWR	6 8 31 32 55
I20	PP1V5_S0	NET_SPACING_TYPE=PWR	6 7 8 11 12 22 26 27 54
I23	PP1V5_S0_NB_QDAC	NET_SPACING_TYPE=PWR	6 22
I100	PP1V5_S0_NB_VCCD_CRT	NET_SPACING_TYPE=PWR	6 19 22
I101	PP1V5_S0_NB_VCCD_QDAC	NET_SPACING_TYPE=PWR	6 19 22
I22	PP1V5_S0_NB_VCCDMIPLL	NET_SPACING_TYPE=PWR	
I24	PP1V5_S0_NB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR	
I25	PP1V5_S0_SB_VCCDMIPLL	NET_SPACING_TYPE=PWR	6 26 27
I26	PP1V5_S0_SB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR	6 27
I28	PP1V5_S0_SB_VCCSATAPLL	NET_SPACING_TYPE=PWR	6 26 27
I27	PP1V5_S0_SB_VCC1_5_B	NET_SPACING_TYPE=PWR	6 23 24 26 27
I30	PP1V8_S0	NET_SPACING_TYPE=PWR	6 7 8 19 22 51 61
I29	PP1V8_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR	6 61
I31	PP1V8_S0_ANALOG_TMDS_F	NET_SPACING_TYPE=PWR	6 61
I33	PP1V8_S0_NB_VCCTXLVDS	NET_SPACING_TYPE=PWR	6 19 22
I32	PP1V8_S0_PVCC1_TMDS_F	NET_SPACING_TYPE=PWR	6 61
I35	PP1V8_S0_PVCC2_TMDS_F	NET_SPACING_TYPE=PWR	6 61
I34	PP1V8_S0_TMDS_F	NET_SPACING_TYPE=PWR	6 61
I36	PP1V8_S3		6 7 8 16 18 21 31 32 34 35 51 55 68
I38	PP1V8_S3M_NB_VCCSMCK	NET_SPACING_TYPE=PWR	6 19 21
I37	PP1V8_S3_NB_VCCSMCK_RC	NET_SPACING_TYPE=PWR	6 21
I39	PP1V05_S0	NET_SPACING_TYPE=PWR	6 7 8 10 11 12 13 14 18 19 21 23 26 27 30 42 54
I41	PP1V05_S0_NB_VCCPEG	NET_SPACING_TYPE=PWR	6 15 19 21
I40	PP1V25_S0	NET_SPACING_TYPE=PWR	6 7 8 16 18 19 21 26 27 51 57
I43	PP1V25_S0M_NB_VCCA_HPLL	NET_SPACING_TYPE=PWR	6 19 21
I42	PP1V25_S0_NB_DPLL	NET_SPACING_TYPE=PWR	6 22
I44	PP1V25_S0_NB_PEGPLL	NET_SPACING_TYPE=PWR	6 19 21
I46	PP1V25_S0_NB_PEGPLL_RC	NET_SPACING_TYPE=PWR	6 21
I45	PP1V25_S0_NB_VCCA_DPLLA	NET_SPACING_TYPE=PWR	6 19 22
I48	PP1V25_S0_NB_VCCA_DPLLB	NET_SPACING_TYPE=PWR	6 19 22
I47	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR	6 60
I49	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR	6 7 60
I50	PP3V3_S0	NET_SPACING_TYPE=PWR	7
I52	PP3V3_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR	6 61
I51	PP3V3_S0_CK505_VDDA	NET_SPACING_TYPE=PWR	6
I54	PP3V3_S0_CK505_VDDA_R	NET_SPACING_TYPE=PWR	6
I53	PP3V3_S0_CK505_VDD_CPU_SRC	NET_SPACING_TYPE=PWR	6 29
I55	PP3V3_S0_CK505_VDD_PCI	NET_SPACING_TYPE=PWR	6
I57	PP3V3_S0_CK505_VDD_REF	NET_SPACING_TYPE=PWR	6
I56	PP3V3_S0_CK505_VDD48	NET_SPACING_TYPE=PWR	6
I59	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR	6 52
I58	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR	6 7 60
I60	PP3V3_S0_NBCORE_FOLLOW_R	NET_SPACING_TYPE=PWR	6 21
I62	PP3V3_S0_NB_CRTDAC_F	NET_SPACING_TYPE=PWR	6 22
I61	PP3V3_S0_NB_TVDAC	NET_SPACING_TYPE=PWR	6 22
I63	PP3V3_S0_NB_TVDAC_F	NET_SPACING_TYPE=PWR	6 22
I65	PP3V3_S0_NB_TVDAC_FOLLOW	NET_SPACING_TYPE=PWR	6 22
I64	PP3V3_S0_NB_VCCA_CRTDAC	NET_SPACING_TYPE=PWR	6 19 22
I67	PP3V3_S0_NB_VCCA_DAC_BG	NET_SPACING_TYPE=PWR	6 19 22
I66	PP3V3_S0_NB_VCCA_TVDACA	NET_SPACING_TYPE=PWR	6 19 22
I68	PP3V3_S0_NB_VCCA_TVDACB	NET_SPACING_TYPE=PWR	6 19 22
I70	PP3V3_S0_NB_VCCA_TVDACC	NET_SPACING_TYPE=PWR	6 19 22
I69	PP3V3_S0_SPVCC_TMDS_F	NET_SPACING_TYPE=PWR	6 61
I72	PP3V3_S3	NET_SPACING_TYPE=PWR	6 7 8 36 42 44 48 51 58 60
I71	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR	6 7 36
I73	PP3V3_S3_TOPCASE_F	NET_SPACING_TYPE=PWR	
I74	PP3V3_S5	NET_SPACING_TYPE=PWR	6 7 8 24 25 26 27 28 36 43 44 49 51 56 57 58 60
I76	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR	6 41 42
I75	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR	6 41
I78	PP3V42G3H_SW	NET_SPACING_TYPE=PWR	6 57
I77	PP3V42_G3H	NET_SPACING_TYPE=PWR	6 7 8 23 26 27 28 39 40 41 42 43 44 57 59
I79	PP3V42_G3H_SMC_F	NET_SPACING_TYPE=PWR	
I81	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR	6 39
I80	PP4V5_AUDIO_ANALOG	NET_SPACING_TYPE=PWR	
I83	PP5V_S0	NET_SPACING_TYPE=PWR	6 7 8 22 27 40 43 47 51 52 53 63
I82	PP5V_S0_AUDIO	NET_SPACING_TYPE=PWR	
I84	PP5V_S0_AUDIO_AMP	NET_SPACING_TYPE=PWR	
I86	PP5V_S0_DVIPORT	NET_SPACING_TYPE=PWR	6 7 37 63
I85	PP5V_S0_DVIPORT_D	NET_SPACING_TYPE=PWR	6 63
I87	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR	6 52
I89	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR	6 7 40
I88	PP5V_S0_SB_V5REF	NET_SPACING_TYPE=PWR	6 26 27
I91	PP5V_S0_TMDS_FUSE	NET_SPACING_TYPE=PWR	6 63
I90	PP5V_S0_3G_F	NET_SPACING_TYPE=PWR	
I92	PP5V_S3	NET_SPACING_TYPE=PWR	6 7 8 40 58 60
I94	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR	6 7 60
I93	PP5V_S3_IR_F	NET_SPACING_TYPE=PWR	
I96	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR	6 39
I95	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR	6 7 37 39
I97	PP5V_S5	NET_SPACING_TYPE=PWR	6 7 8 27 39 51 54 55 56 58
I98	PP5V_S5_SB_V5REF_SUS	NET_SPACING_TYPE=PWR	6 26 27
I99	PP18V5_DCIN	NET_SPACING_TYPE=PWR	6 7 50
I102	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR	6 50
I103	PP18V5_G3H	NET_SPACING_TYPE=PWR	6 7 8 50 59
I104	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR	6 59

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M82 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0

SCALE NONE SHT 72 OF 73

M82 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2,ISL4,ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10,ISL11,ISL13	Y	0.215 MM	0.215 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2,ISL4,ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10,ISL11,ISL13	Y	0.091 MM	0.091 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP,BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

M82 Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 73	OF 73