

SCHEM, MLB, MBP17

05/07/2007

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
?		50265	PVT Release	?	?
				DATE	DATE

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5	BOM Configuration	N/A	N/A
6	Revision History	N/A	N/A
7	Functional / ICT Test	MASTER	MASTER
8	Power Aliases	(MASTER)	(MASTER)
9	Signal Aliases	(T9_MLB)	08/23/2006
10	CPU FSB	T9_NOME	01/25/2007
11	CPU Power & Ground	T9_NOME	01/25/2007
12	CPU Decoupling & VID	M75_MLB	12/07/2006
13	eXtended Debug Port (XDP)	T9_NOME	01/22/2007
14	NB CPU Interface	T9_NOME	01/25/2007
15	NB PEG / Video Interfaces	T9_NOME	03/19/2007
16	NB Misc Interfaces	T9_NOME	01/25/2007
17	NB DDR2 Interfaces	T9_NOME	01/25/2007
18	NB Power 1	T9_NOME	01/25/2007
19	NB Power 2	T9_NOME	01/25/2007
20	NB Grounds	T9_NOME	01/25/2007
21	NB Standard Decoupling	T9_NOME	12/21/2006
22	NB Graphics Decoupling	M75_MLB	03/20/2007
23	SB Enet, Disk, FSB, LPC	T9_NOME	01/25/2007
24	SB PCI, PCIe, DMI, USB	T9_NOME	01/25/2007
25	SB Pwr Mgt, GPIO, Clink	M75_MLB	04/02/2007
26	SB Power & Ground	T9_NOME	01/25/2007
27	SB Decoupling	T9_NOME	01/25/2007
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43	External USB Connector	M75_MLB	12/04/2006
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45	SMC	T9_NOME	12/21/2006

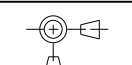

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73	NV G84M GPIO/MIO/Misc	M75_MLB	03/19/2007
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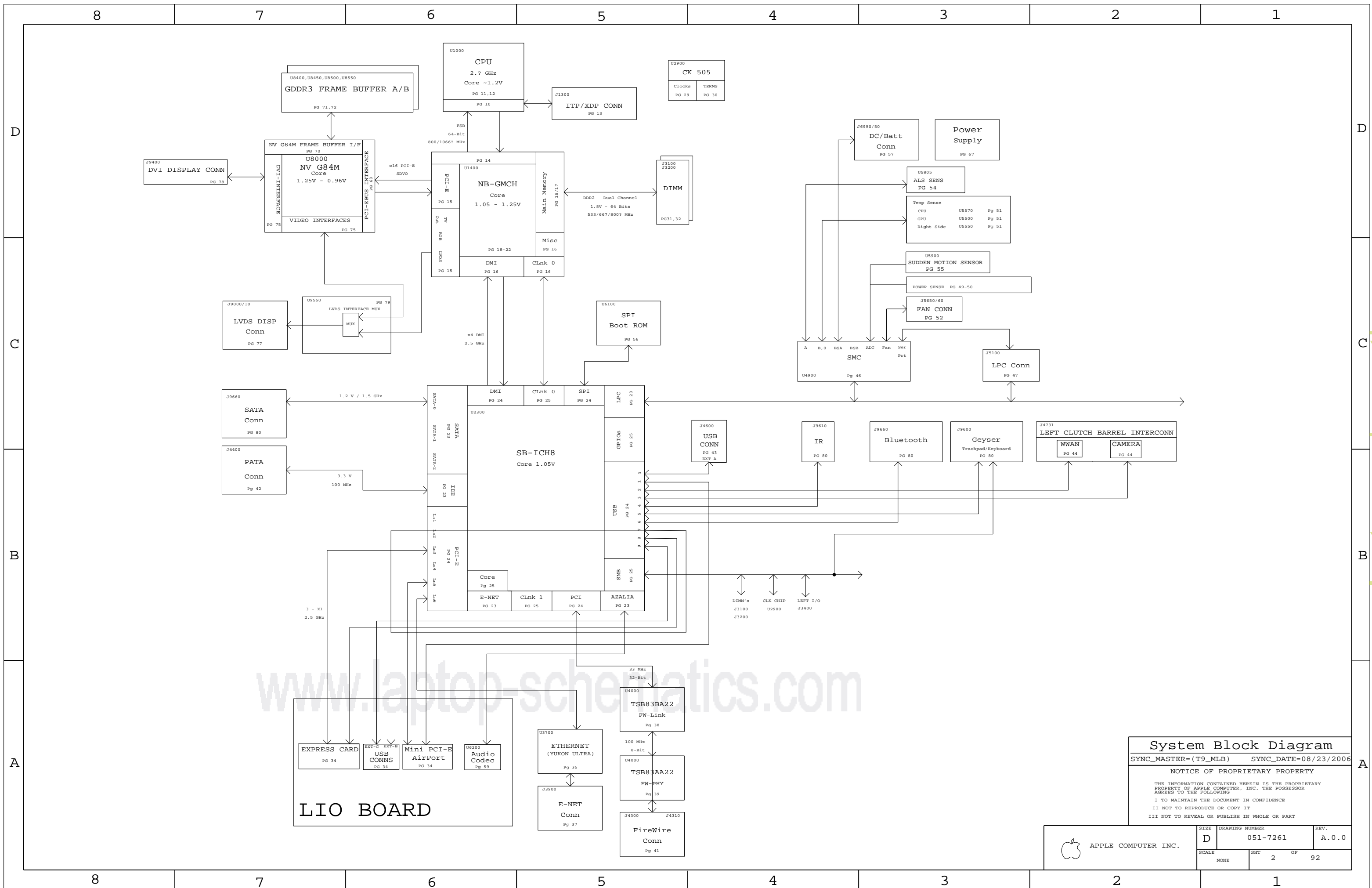
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7261	1	SCHEM, MLB, MBP17	SCH	CRITICAL	
820-2132	1	PCBFB, MLB, MBP17	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon May 7 19:12:36 2007

<p style="text-align: center;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <p style="text-align: center;">  THIRD ANGLE PROJECTION </p>	<p>METRIC</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td>DRAFTER</td> <td>DESIGN CK</td> </tr> <tr> <td>ENG APPD</td> <td>MFG APPD</td> </tr> <tr> <td>QA APPD</td> <td>DESIGNER</td> </tr> <tr> <td>RELEASE</td> <td>SCALE</td> </tr> </table> <p style="text-align: center;">MATERIAL/FINISH NOTED AS APPLICABLE</p> <p style="text-align: center;">SIZE D</p>	DRAFTER	DESIGN CK	ENG APPD	MFG APPD	QA APPD	DESIGNER	RELEASE	SCALE	 <p>Apple Computer Inc.</p> <p style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: small;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="font-size: large; font-weight: bold;">SCHEM, MLB, MBP17</p> <p style="text-align: right;">DRAWING NUMBER 051-7261 REV. A.0.0</p> <p style="text-align: right; font-size: x-small;">SHT 1 OF 92</p>
DRAFTER	DESIGN CK									
ENG APPD	MFG APPD									
QA APPD	DESIGNER									
RELEASE	SCALE									

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System Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

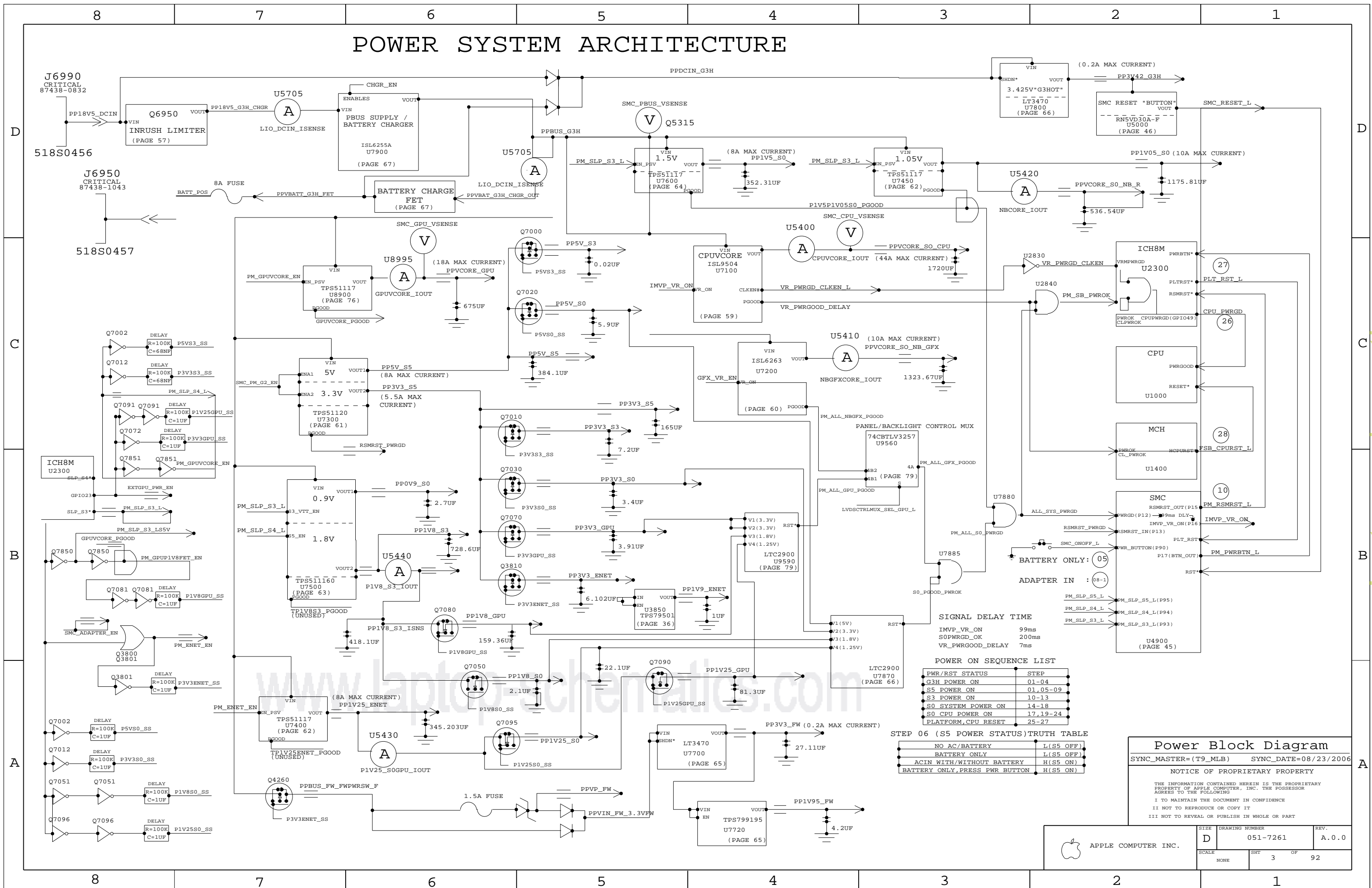
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POWER SYSTEM ARCHITECTURE



SIGNAL DELAY TIME

IMVP_VR_ON	99ms
SOPWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01, 05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17, 19-24
PLATFORM, CPU RESET	25-27

STEP 06 (S5 POWER STATUS) TRUTH TABLE

NO AC/BATTERY	BATTERY ONLY	ACIN WITH/WITHOUT BATTERY	BATTERY ONLY, PRESS PWR BUTTON
L(S5 OFF)	L(S5 OFF)	H(S5 ON)	H(S5 ON)

Power Block Diagram
 SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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M76 BOM Groups

BOM GROUP	BOM OPTIONS
M76_COMMON	COMMON, ALTERNATE, M76_COMMON1, M76_COMMON2, M76_DEBUG, M76_PROGPARTS, ISL6257H
M76_COMMON1	EXTGPU_RST_HW, ISL9504B, LVDS_SEL_RESUME, ONEWIRE_PU, CPU_NTC_A, GPU_XW1
M76_COMMON2	P1V8S3_1V825_GPUFB, SLG2AP101, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN
M76_CTO	INV_SPLIT, INV_17INCH
M76_DEBUG	SMC_DEBUG_NO, XDP, LPCPLUS
M76_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X6P]	CRITICAL	EEE_X6P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XWU]	CRITICAL	EEE_XWU
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XZ6]	CRITICAL	EEE_XZ6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XZ7]	CRITICAL	EEE_XZ7

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0432	1	IC,NB,CRESTLINE,GM,C0,PRQ,965PM	U1400	CRITICAL	
338S0434	1	IC,SB,ICH8M,B1,PRQ,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B

359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,LW PWR CLK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2050	1	IC,SMC,DEVELOPMENT,M76	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG

333S0382	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
337S3465	1	IC,MDC,SR,E1,PRQ,2.4G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	See alt to TR/SiTech magnetism
152S0476	152S0276		ALL	Inductor alternate
138S0603	138S0602		ALL	Make alt to Samsung 22P Ananida caps
353S1681	353S1294		ALL	TI alternate to National
376S0543	376S0466		ALL	See alternate to ellisona 81443
376S0526	376S0451		ALL	Palcohol PRIMER alternate to 087707

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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	8	7	6	5	4	3	2	1	
D	<p>DVT</p> <p>13.1.0: 3/05/07 -- Integrated m75/mlb pages 22,25,28,30-32,50,53-55,72,74,76,78,80-82,84-90,94,95 through: Change 46833 by cerickso@m75_mlb_051-7225_12.5.0_tmp.Ecad on 2007/03/02 09:49:13 Changes since previous major release (12.3.0): - LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882) - NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272) Changes since previous major release (12.2.0): - Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating) - NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109) - Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109) - Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF) - NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines Changes since previous bom release (12.0.0): - GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm) - GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02k, R8432/82, R8532/82 -> 2.21K) - Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927) - GPU Vcore: NO STUFFED all PWRCTL related components (feature not to be supported) - GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V - SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates - Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors) 3/5/07 -- Added GPU Vcore VFB resistor BOM table and GCORE_M76 BOM Option to M76_COMMON BOM group. 3/5/07 -- Removed RX3920-RX3927. 3/5/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435) 3/5/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) 3/5/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.% 13.2.0 3/07/07 -- Integrated m75/mlb pages 25,42,70 through: Change 47192 by cerickso@m75_mlb_051-7225_12.7.0_tmp.Ecad on 2007/03/06 18:36:54 Changes since previous major release (12.6.0): - FireWire Ports: Changed D4260 to PDS540 for higher current capacity - SB GPIOs: Changed R2514 from pulldown to pulldown to correct auto power-on issue (Linda card detect GPIO) 3/07/07 -- Q7080 PPIV8_GPU FET changed for lower Rds on from FDM6296 to RJK0301DPB 13.3.0 3/08/07 -- Removed =PPIV5_S0_NB_VCCD_CRT alias to PPIV5_S0 since VCCD_CRT is GNDed per CRT disable guidelines. 3/08/07 -- Battery charge current limit circuit changes. 3/08/07 -- Changed R9811 from 15.0K to 14.0K. This is so that M57 inverter and split inverter can use same backlight table. 3/08/07 -- Changed R9950 from 220K to NOSTUFF to improve current and voltage asymmetry ratio. 3/08/07 -- Changed BOM option on R9960 511k from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio. 3/08/07 -- Integrated CSA pg. 55 through: Change 47450 by cerickso@m75_mlb_051-7225_12.8.0_tmp.Ecad on 2007/03/08 10:49:26 Changes since previous major release (12.7.0): - Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033 3/08/07 -- Integrated CSA pg. 79 through: Change 47440 by xyang@m75_luo_051-7226_7.9.0_tmp.Ecad on 2007/03/08 10:25:46 Changed Charger PWM limit resistor according to MARC K.'S M70 values 13.4.0 3/12/07 -- Added BOM option P1V8S3_1V825 to M76_COMMON2 BOM group. 3/12/07 -- Modified R7520 and R7521 to use symbols for 0.1% resistors. Removed OMIT BOM option from R7521. Changed BOM options for R7520 to choose between 1.8V or 1.825V 0.1% resistors. 14.0.0 3/14/07 -- Removed BOM option for HDCP as feature is removed. 3/14/07 -- Moved =PPIV8_GPU_P1V8GPFET from PPIV8_S3_ISNS to PPIV8_S3. This is to remove the current sense resistor from the GPU 1.8V path. Cleaned up unused aliases. 3/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms 3/14/07 -- Integrated m75/mlb CSA pages 55 & 78 through: Change 48122 by cerickso@cerickso_m75.Ecad on 2007/03/14 15:27:36 - Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd - Power Control: Corrected alias connections for 5V/3V3 S5 enable signals 14.1.0 3/14/07 -- Moved =PPIV8_S0_P1V8S0FET from PPIV8_S3_ISNS to PPIV8_S3. 14.2.0 3/15/07 -- Changes to low voltage inverter for M76 piezo. 14.5.0 3/19/07 -- Integrated m75/mlb CSA pgs. 28,30-32,50,53-55,80-82,84-88,90,94,95 through: Change 48405 by cerickso@m75_mlb_051-7225_13.3.0_tmp.Ecad on 2007/03/16 12:18:46 Changes since previous major release (13.2.0): - Thermal Sensors: Moved remote sensor U5500 to SMC SMBus A and S3 power rail to clear I2C addr clash 3/19/07 --Integrated t9/mlb_noME CSA pgs. 15 & 38 through: Change 48372 by wferry@wferry_projects.Ecad on 2007/03/16 09:11:01 Quick submit of T9 noME branch. Major release will follow once changes are properly documented in Radar and revision history. Page 15: Sync from main-line (renamed LVDS_VREFx nets). Page 38: Changed Yukon crystal load caps to 18pF per radar://4946795 (really radar://4945362). 3/19/07 -- Added OMIT BOM option to L4731 and L4741. 3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741. 3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5. 3/19/07 -- <rdar://problem/5070179> BOM update: boost circuit open causes MLB & SMM damage (see 5064997) Deleted R7364 and made C7364 0603 size, still 0.1uF (132S0100). Deleted R7420 and R7470 and made C7420 and C7470 0603 size, still 0.1uF (132S0100). Deleted R7525 and made C7525 0805 size, still 0.1uF (132S0201). Deleted R7615 and made C7615 0603 size, still 0.1uF (132S0100). Deleted R8915 and made C8915 0603 size, still 0.1uF (132S0100). 3/19/07 -- Changes to low voltage inverter for M76 piezo. L9950 changed from 152S0527 (15uH, 2.8A, 115mOhm) to 152S0585 (22uH, 2.8A, 129mOhm). 14.6.0 3/19/07 -- Integrated m75/mlb CSA pgs. 55 & 78 through: Change 48590 by cerickso@m75_mlb_051-7225_13.4.0_tmp.Ecad on 2007/03/19 14:26:14 Changes since previous major release (13.3.0): - Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail - Power Control: Added U7858 to level shift PM_G2_EN to 3.42V to 5V 3/19/07 -- Updated SMC A SMBus information for Left I/O Board and Top-Case. 3/19/07 -- Deleted R7324 and made C7324 0603 size, still 0.1uF (132S0100). 14.7.0 3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path. 3/19/07 -- Battery charge current limit circuit changes for max charge current of 4.5A. 3/19/07 -- Integrated m75/mlb CSA pgs. 22 & 78 through: Change 48660 by cerickso@m75_mlb_051-7225_13.5.0_tmp.Ecad on 2007/03/19 20:17:1 Changes since previous major release (13.4.0): - Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3 and EN5) together as part of PM_G2_EN 14.8.0 3/21/07 -- Integrated m75/mlb CSA pgs. 84,85 & 89 through: Change 48885 by cerickso@m75_mlb_051-7225_14.0.0_tmp.Ecad on 2007/03/20 21:27:14 This fab release is for DVT! Changes since previous major release (13.5.0): - GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V, 1.05V, 1.05V, 1.125V) - FB: Changed FB VREF caps to 2x0.0047uF as required by Nvidia PUN 02736-001-v07 (which requests 1x0.01uF) 3/21/07 -- <rdar://problem/4838347> EMC - M76 MLB changes Change BOM option on L4764 to OMIT and added BOM table entry for 0 ohm resistor at L4764. 3/21/07 -- <rdar://problem/5073301> M76: Change GPU Vmin Changed resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.05V, 1.125V, 1.25V) Removed NOSTUFF BOM option from R8924. Changed R8924 to 28K. Changed R8925 to 16.9K. Changed table text notes. 3/22/07 -- Items relating to <rdar://problem/5061583> Task: Current Surge When Insert Battery Without AC Plugged-In 3/22/07 -- Added D7903 for voltage ripple on ISL6257 BOOT and PHASE pins. 3/22/07 -- Added Q7970 for potential battery inrush current. 15.0.0 3/26/07 -- Removed C7930 and R7903 for space reasons. 15.2.0 3/28/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input. 3/28/07 -- Added XW7580 and R7580 for option to tie 1.8V S3 regulator feedback point to input of 1.8V GPU FET. 3/28/07 -- Integrated m75/mlb CSA pg. 87 through Change 49919 by cerickso@cerickso_m75.Ecad on 2007/03/28 14:28:29 Changes since previous fab release (14.0.0): - GPU Straps: Added PCI_DEVID<3..0> pullup straps 15.3.0 3/29/07-- Moved XW7580 to XW0980, and R7580 to R0980. 15.4.0 3/31/97 -- Changed C9950 from 22uF to 10uF for acoustic noise per Flo Kim. 3/31/97 --Added C9951 B2 case size as placeholder for new cap for acoustic noise per Flo Kim.</p>								D
C									C
B									B
A									A

Revision History	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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NONE	6	92	

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Functional Test Points

Fan Connectors

FUNC_TEST	
TRUE PP5V_S0	81 7 27 42 47 48 52
TRUE FAN_LT_PWM	52
TRUE FAN_LT_TACH	52
TRUE FAN_RT_PWM	52
TRUE FAN_RT_TACH	52

LPC+ Debug Connector

FUNC_TEST	
TRUE PP3V42_G3H	8 28 42 45 46 47 48
TRUE PP5V_S0	8 7 27 42 47 48 52
TRUE LPC_AD<0>	23 45 47
TRUE LPC_AD<1>	23 45 47
TRUE LPC_FRAME_L	23 45 47
TRUE PM_CLKRUN_L	25 45 47
TRUE PCI_FW_GNT_L	24 38 47 87
TRUE SMC_TMS	45 46 47
TRUE DEBUG_RESET_L	28 47
TRUE SMC_TRST_L	45 47
TRUE SMC_TDO	45 46 47
TRUE SMC_MD1	45 47
TRUE SMC_TX_L	43 45 46 47
TRUE FWH_INIT_L	47
TRUE PCI_CLK33M_LPCPLUS	30 47 88
TRUE LPC_AD<2>	23 45 47
TRUE LPC_AD<3>	23 45 47
TRUE INT_SERIRQ	25 45 47
TRUE PM_SUS_STAT_L	25 45 46 47
TRUE SMC_TDI	45 46 47
TRUE SMC_TCK	45 46 47
TRUE SMC_RESET_L	45 46 47
TRUE SMC_NMI	45 47
TRUE SMC_RX_L	43 45 46 47
TRUE LINDACARD_GPIO	25 47

Left ALS

FUNC_TEST	
TRUE ALS_GAIN	34 45 54
TRUE LTALS_OUT	34 54
TRUE GND	

Thermal Diode Connectors

FUNC_TEST	
TRUE HSTHMSNS_D_P	51 91
TRUE HSTHMSNS_D_N	51
TRUE RSFSTHMSNS_D_P	51 91
TRUE RSFSTHMSNS_D_N	51
TRUE CEUTHMSNS_D2_P	51 91
TRUE CEUTHMSNS_D2_N	51

System Validation TPs

FUNC_TEST	
TRUE CPU_PWRGD	10 13 23 83
TRUE CPU_DPSLP_L	7 10 23 83
TRUE PM_DPRSPLVR	16 25 59 83
TRUE CPU_DPSLP_L	7 10 23 83
TRUE PM_LAN_ENABLE	25 45
TRUE PCI_RST_L	24 28
TRUE PM_RSMRST_L	25 45
TRUE PM_SB_PWROK	9 25 28
TRUE SB_RTC_RST_L	23 28
TRUE PM_STPCPU_L	25 29 30
TRUE PM_STPPCI_L	25 29 30
TRUE VR_PWRGD_CLKEN	25 28
TRUE VR_PWRGD_DELAY	9 16 28 59
TRUE FSB_CPURST_L	10 13 24 83
TRUE FSB_CPUSLP_L	10 14 83
TRUE FSB_DPWR_L	10 14 83
TRUE NB_SB_SYNC_L	16 25
TRUE PM_BMBUSY_L	16 25

Battery Digital Connector

FUNC_TEST	
TRUE SMC_BS_ALERT_L	45 46 57
TRUE SMBUS_SMC_BSA_SCL	45 48 57 88
TRUE SMBUS_SMC_BSA_SDA	45 48 57 88
TRUE BATT_POS	57 67
TRUE GND	
TRUE GND (HOST_DETECT_L)	

Left I/O Power Connector

FUNC_TEST	
TRUE PP18V5_DCIN	87 Request for 2 test points
TRUE PPBUS_G3H	82 49 Request for 3 test points
TRUE GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST	
TRUE PPVRATT_G3_RTC	28
TRUE GND	

Current Sense Calibration

FUNC_TEST	
TRUE ISENSE_CAL_EN	45 49
TRUE PP5V_S0	7 8 27 42 47 48 52 54 58 59 80
TRUE PPVCORE_S0_NB_GFX	8 18 23 46
TRUE PPVCORE_S0_CPU	8 11 12 49
TRUE PPVCORE_GPU	8 49 69 8
TRUE GND	

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST	
TRUE PP5V_S3_CAMERA_F	44
TRUE USB_CAMERA_F_N	44 91
TRUE USB_CAMERA_F_P	44 91
TRUE PP5V_S3_WWAN_F	44
TRUE USB_WWAN_F_N	44 91
TRUE USB_WWAN_F_P	44 91

Other Func Test Points

FUNC_TEST	
TRUE PM_SYSRST_L	25 28 45
TRUE SMC_ONOFF_L	45 46 80

ICT Test Points

CPU FSB NO_TESTS

MAKE BASE	NO_TEST	
TRUE	FSB_A_L<31..3>	10 14 83
TRUE	FSB_ADS_L	10 14 83
TRUE	FSB_ADSTB_L<1..0>	10 14 83
TRUE	FSB_BNR_L	10 14 83
TRUE	FSB_BREQ0_L	10 14 83
TRUE	FSB_D_L<63..0>	10 14 83
TRUE	FSB_DBSY_L	10 14 83
TRUE	FSB_DINV_L<3..0>	10 14 83
TRUE	FSB_DRDY_L	10 14 83
TRUE	FSB_DSTB_L_N<3..0>	10 14 83
TRUE	FSB_DSTB_L_P<3..0>	10 14 83
TRUE	FSB_HIT_L	10 14 83
TRUE	FSB_HITM_L	10 14 83
TRUE	FSB_LOCK_L	10 14 83
TRUE	FSB_REO_L<4..0>	10 14 83
TRUE	NC_CPU_RSVD5	NC_CPU_RSVD5 7 10

NB NO_TESTS

MAKE BASE	NO_TEST	
TRUE	NC_NB_NC<1..16>	TP_NB_NC<1..16> 16
TRUE	NC_NB_RSVD<26..27>	TP_NB_RSVD<26..27> 16
TRUE	NC_NB_RSVD<24>	TP_NB_RSVD<24> 16

GPU NO_TESTS

NO_TEST	
TRUE LVDS_L_CLK_P	75 79 90
TRUE LVDS_L_DATA_P<0>	75 79 90
TRUE TP_GPU_MIOB_CLKIN	73 74
TRUE TP_GPU_MIOB_CLKOUT_P	73 74
TRUE TP_GPU_MIOB_CTL3	73 74
TRUE NC_GPUVCORE_VFB_PC0	76
TRUE NC_GPUVCORE_VFB_PC1	76

Inverter Connector

FUNC_TEST	
TRUE PPBUS_S0_LCDBKLT_FUSED	82
TRUE GND_CHASSIS_INVERTER	9 44 51 80 82
TRUE PP5V_SW_LCDBKLT	81 82
TRUE LCDBKLT_PWM	81 82
TRUE GND	

IR & Sleep LED Connector

FUNC_TEST	
TRUE PP5V_S3	8 44 46 58 80
TRUE USB_IR_N	24 80 86
TRUE USB_IR_P	24 80 86
TRUE SYS_LED_ANODE	46 80
TRUE GND	

Functional / ICT Test

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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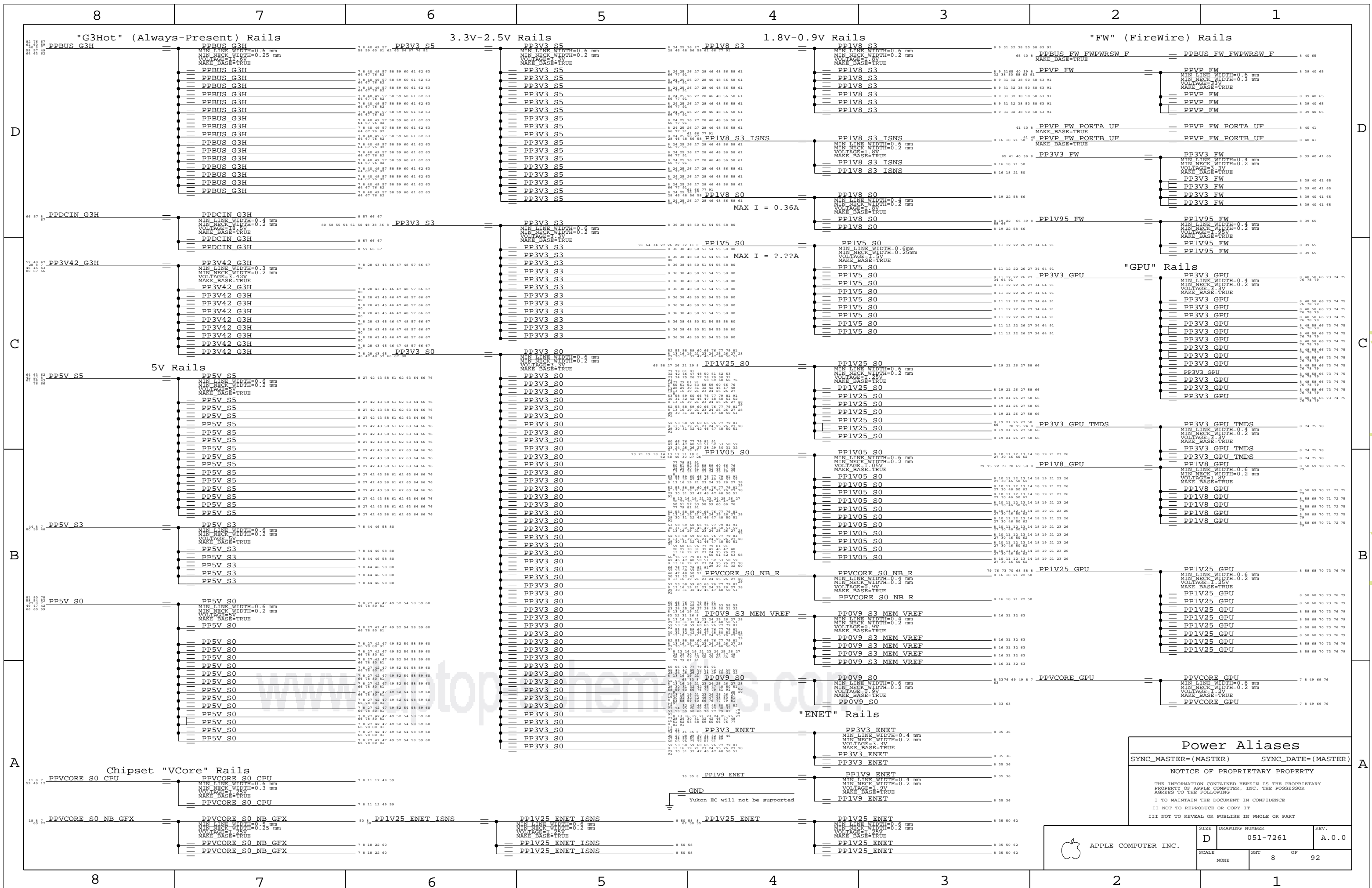
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	SHT 7 OF 92	



Power Aliases

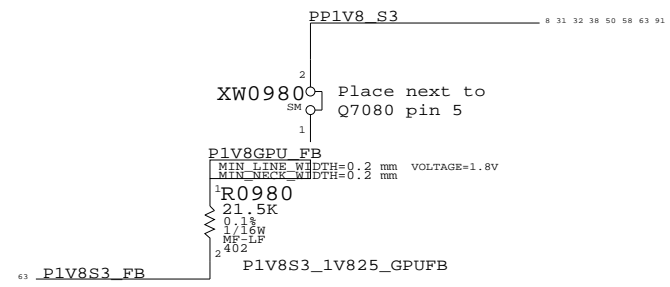
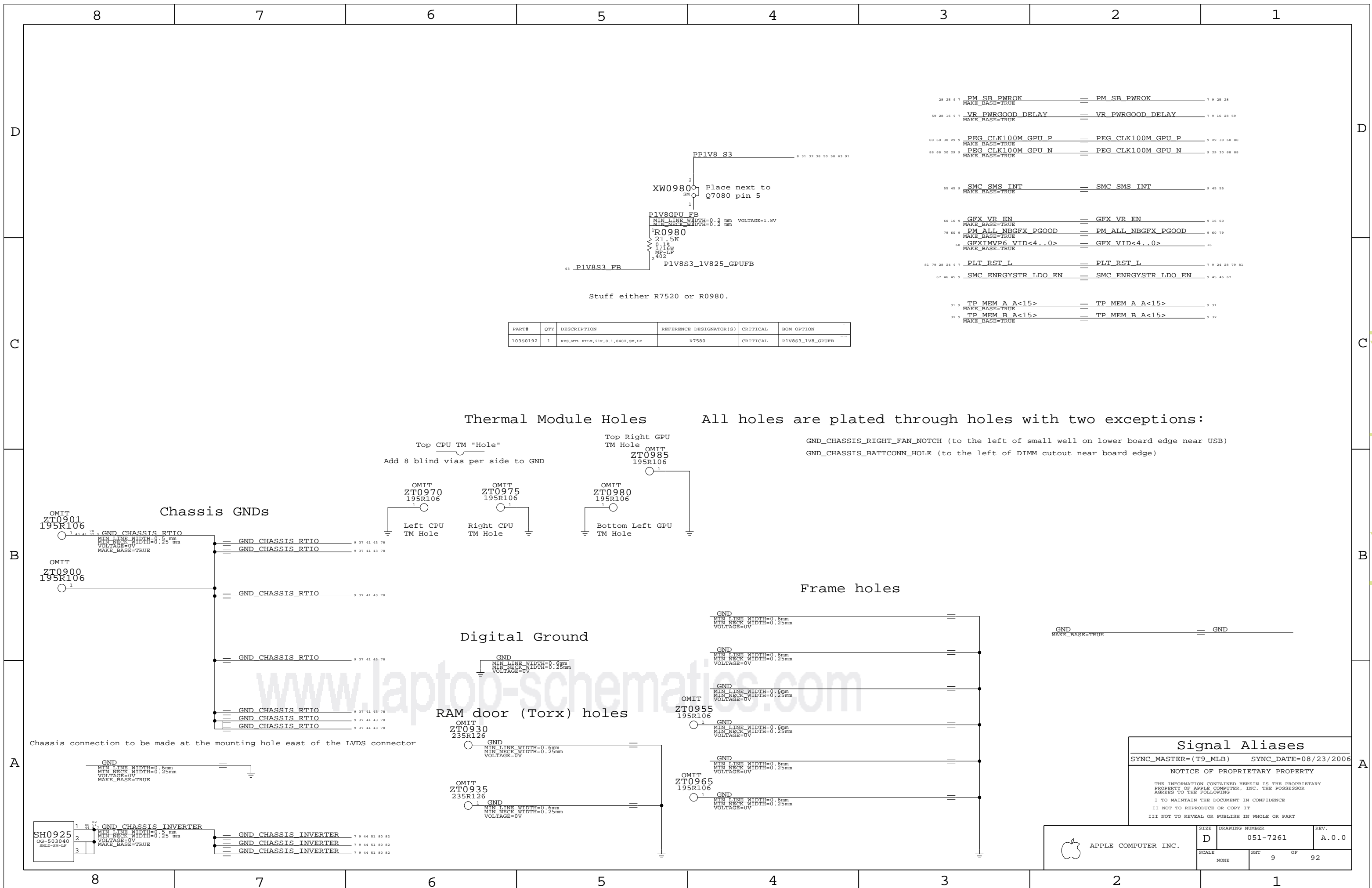
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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			8	92

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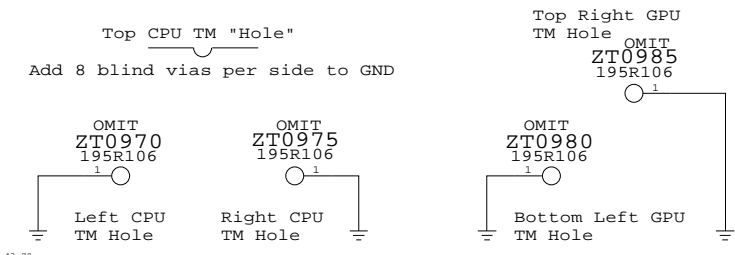
Stuff either R7520 or R0980.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10350192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7580	CRITICAL	P1V8S3_1V8_GPUPB

28 25 9 7	PM_SB_PWROK	==	PM_SB_PWROK	7 9 25 28
	MAKE_BASE=TRUE			
59 28 16 9 7	VR_PWRGOOD_DELAY	==	VR_PWRGOOD_DELAY	7 9 16 28 59
	MAKE_BASE=TRUE			
88 68 30 29 9	PEG_CLK100M_GPU_P	==	PEG_CLK100M_GPU_P	9 29 30 68 88
	MAKE_BASE=TRUE			
88 68 30 29 9	PEG_CLK100M_GPU_N	==	PEG_CLK100M_GPU_N	9 29 30 68 88
	MAKE_BASE=TRUE			
55 45 9	SMC_SMS_INT	==	SMC_SMS_INT	9 45 55
	MAKE_BASE=TRUE			
60 16 9	GFX_VR_EN	==	GFX_VR_EN	9 16 60
	MAKE_BASE=TRUE			
79 60 9	PM_ALL_NBGFX_PGOOD	==	PM_ALL_NBGFX_PGOOD	9 60 79
	MAKE_BASE=TRUE			
60	GFXIMVP6_VID<4..0>	==	GFX_VID<4..0>	16
	MAKE_BASE=TRUE			
81 79 28 24 9 7	PLT_RST_L	==	PLT_RST_L	7 9 24 28 79 81
67 46 45 9	SMC_ENRGYSTR_LDO_EN	==	SMC_ENRGYSTR_LDO_EN	9 45 46 67
31 9	TP_MEM_A_A<15>	==	TP_MEM_A_A<15>	9 31
	MAKE_BASE=TRUE			
32 9	TP_MEM_B_A<15>	==	TP_MEM_B_A<15>	9 32
	MAKE_BASE=TRUE			

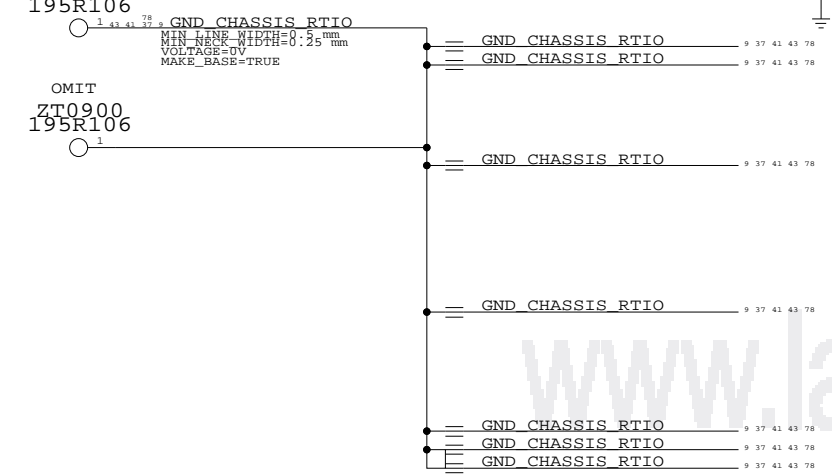
Thermal Module Holes

All holes are plated through holes with two exceptions:

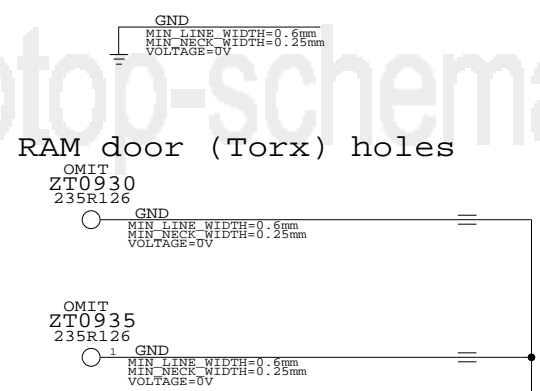


- GND_CHASSIS_RIGHT_FAN_NOTCH (to the left of small well on lower board edge near USB)
- GND_CHASSIS_BATTCONN_HOLE (to the left of DIMM cutout near board edge)

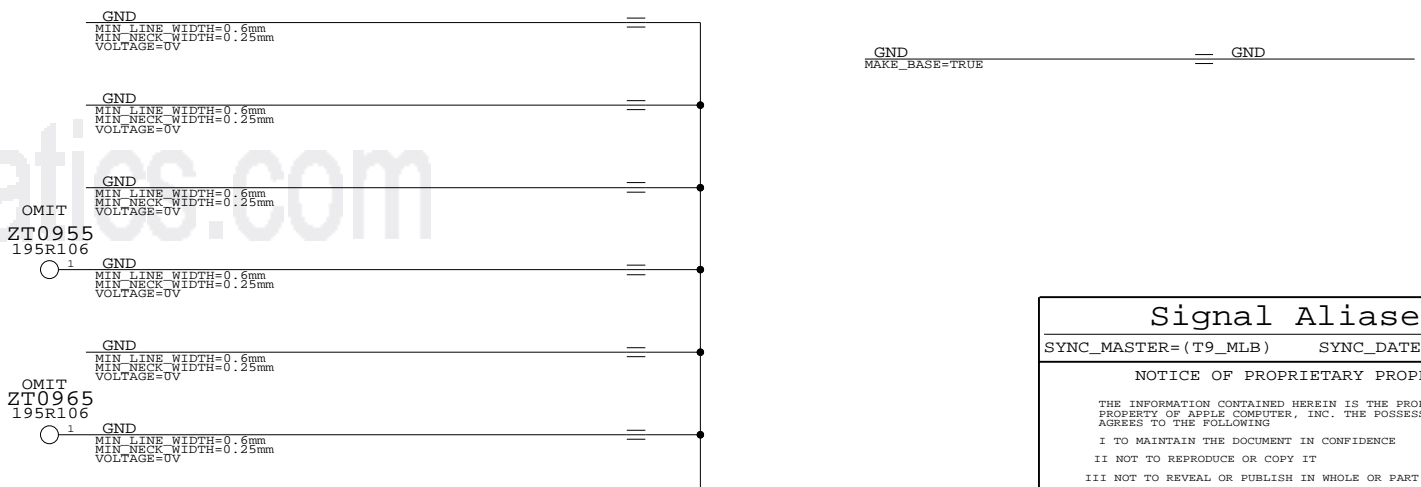
Chassis GNDs



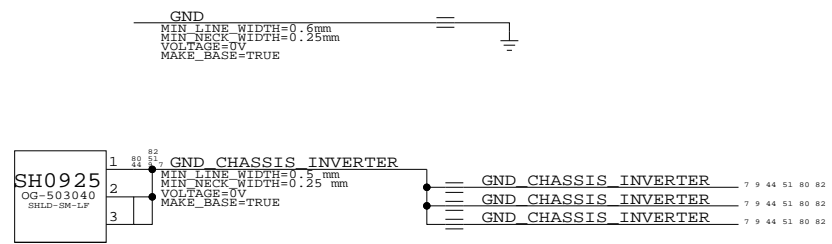
Digital Ground



Frame holes

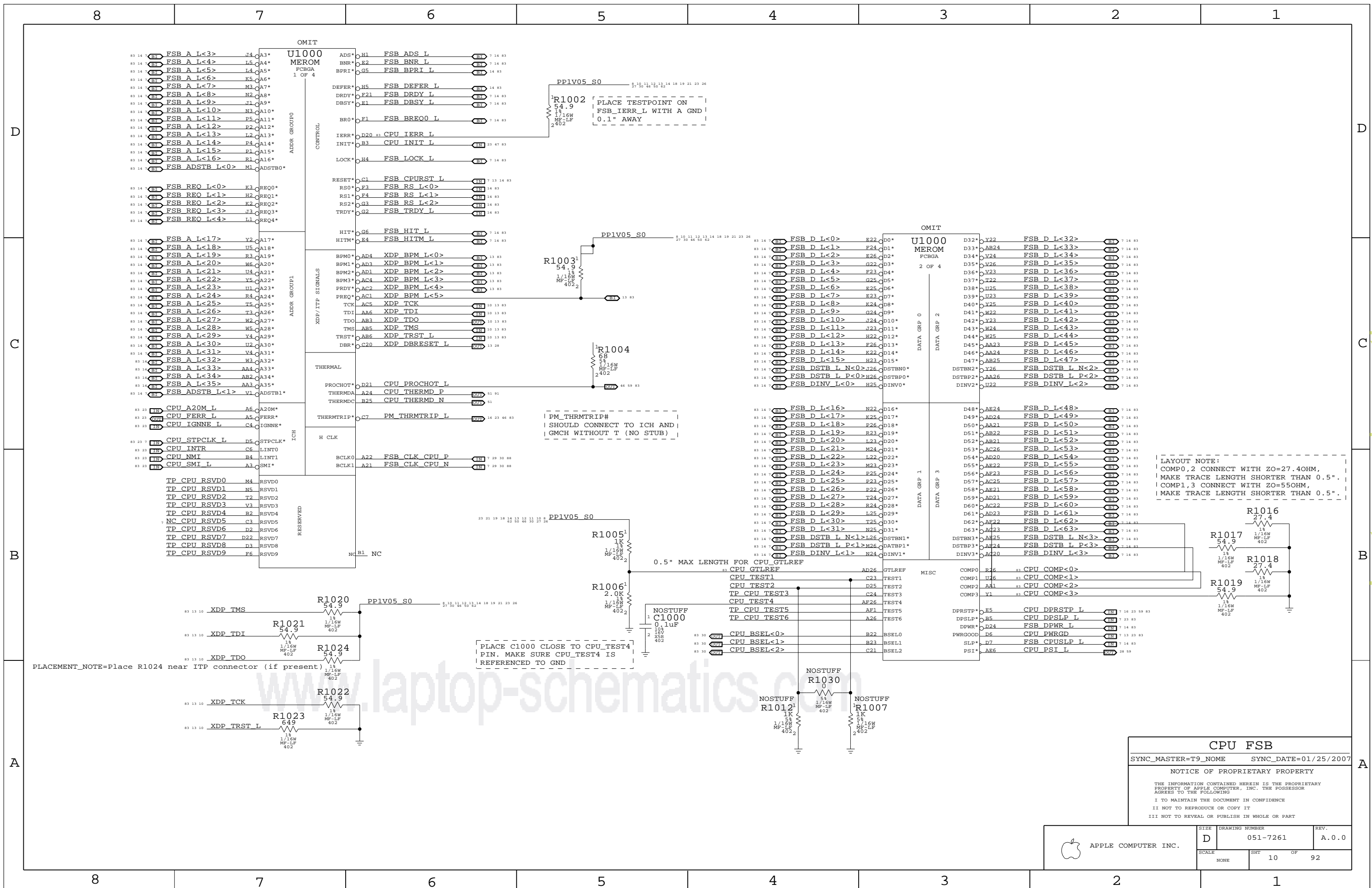


Chassis connection to be made at the mounting hole east of the LVDS connector



Signal Aliases	
SYNC_MASTER=(T9_MLB)	SYNC_DATE=08/23/2006
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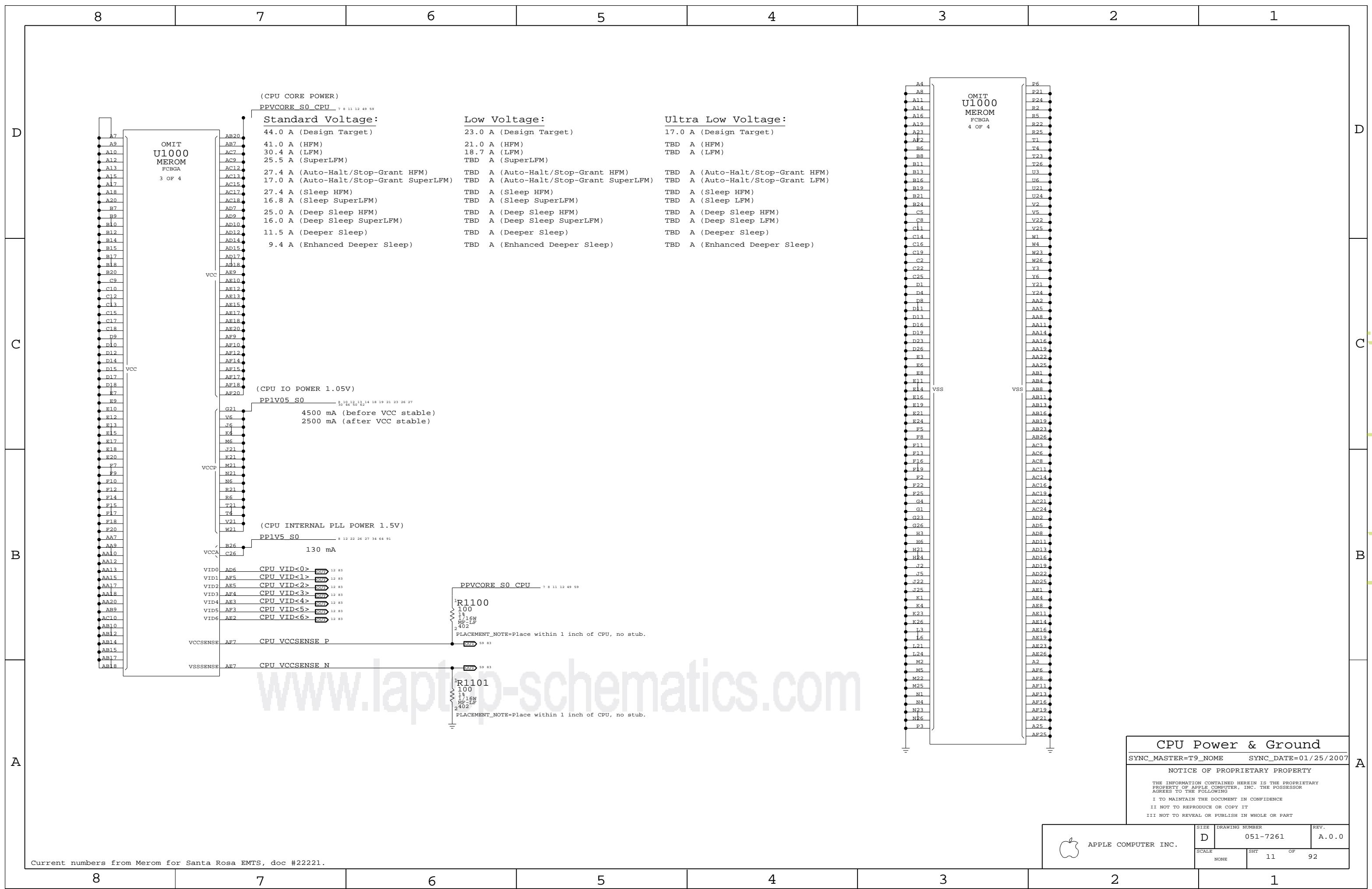
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NONE	9	92	



LAYOUT NOTE:
 COMP0, 2 CONNECT WITH ZO=27.4OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMP1, 3 CONNECT WITH ZO=55OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB
 SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007
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	SCALE NONE	SHEET 10	OF 92



(CPU CORE POWER)
PPVCORE_S0_CPU_7 8 11 12 49 59

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)
PPIV05_S0_50 106 130 132 14 18 19 21 23 26 27

- 4500 mA (before VCC stable)
- 2500 mA (after VCC stable)

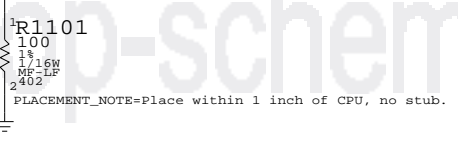
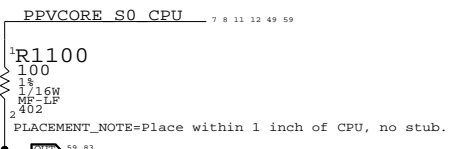
(CPU INTERNAL PLL POWER 1.5V)
PPIV5_S0_8 12 22 26 27 34 64 91

- 130 mA

- VID0 AE6 CPU VID<0>
- VID1 AE5 CPU VID<1>
- VID2 AE5 CPU VID<2>
- VID3 AF4 CPU VID<3>
- VID4 AE3 CPU VID<4>
- VID5 AF3 CPU VID<5>
- VID6 AE2 CPU VID<6>

VCCSENSE AF7 CPU VCCSENSE P

VSSSENSE AE7 CPU VCCSENSE N



CPU Power & Ground
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

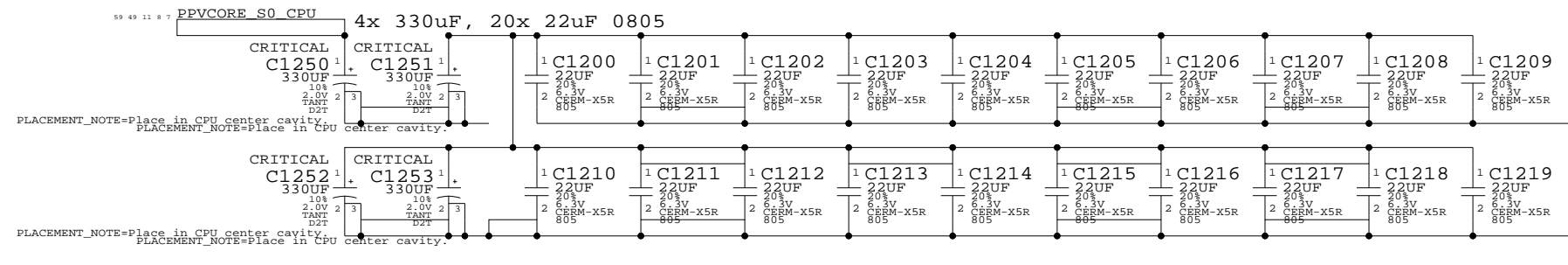
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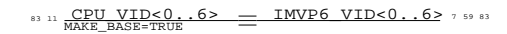
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NONE	11	92	

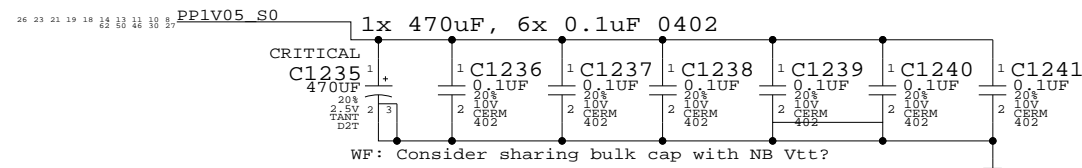
CPU VCORE HF AND BULK DECOUPLING



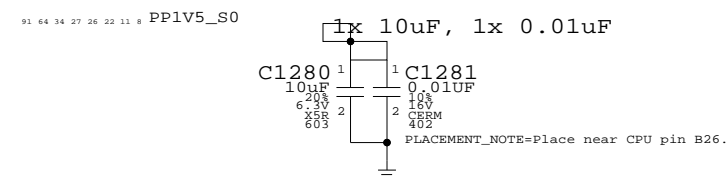
CPU VCORE VID CONNECTIONS



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



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CPU Decoupling & VID

SYNC_MASTER=M75_MLB SYNC_DATE=12/07/2006

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SCALE	SHT		OF
NONE	12		92

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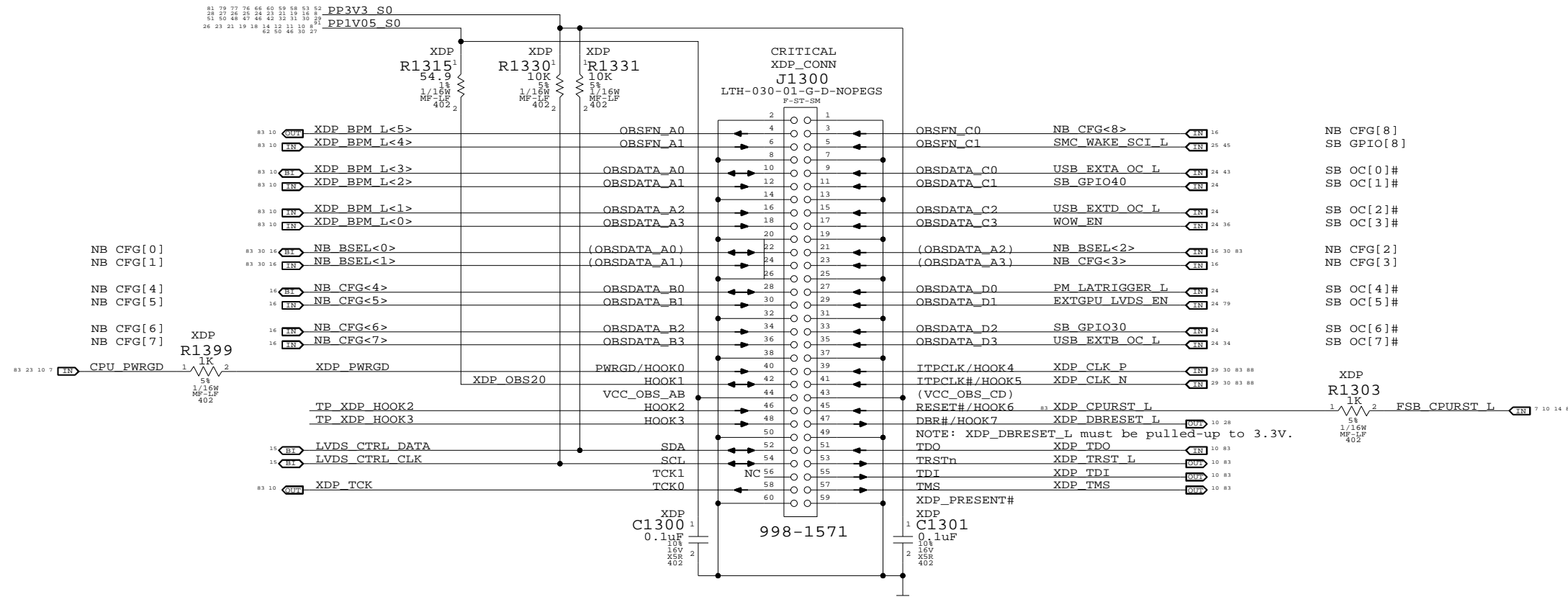
B

A

A

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



← Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

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eXtended Debug Port (XDP)
SYNC_MASTER=T9_NOME SYNC_DATE=01/22/2007

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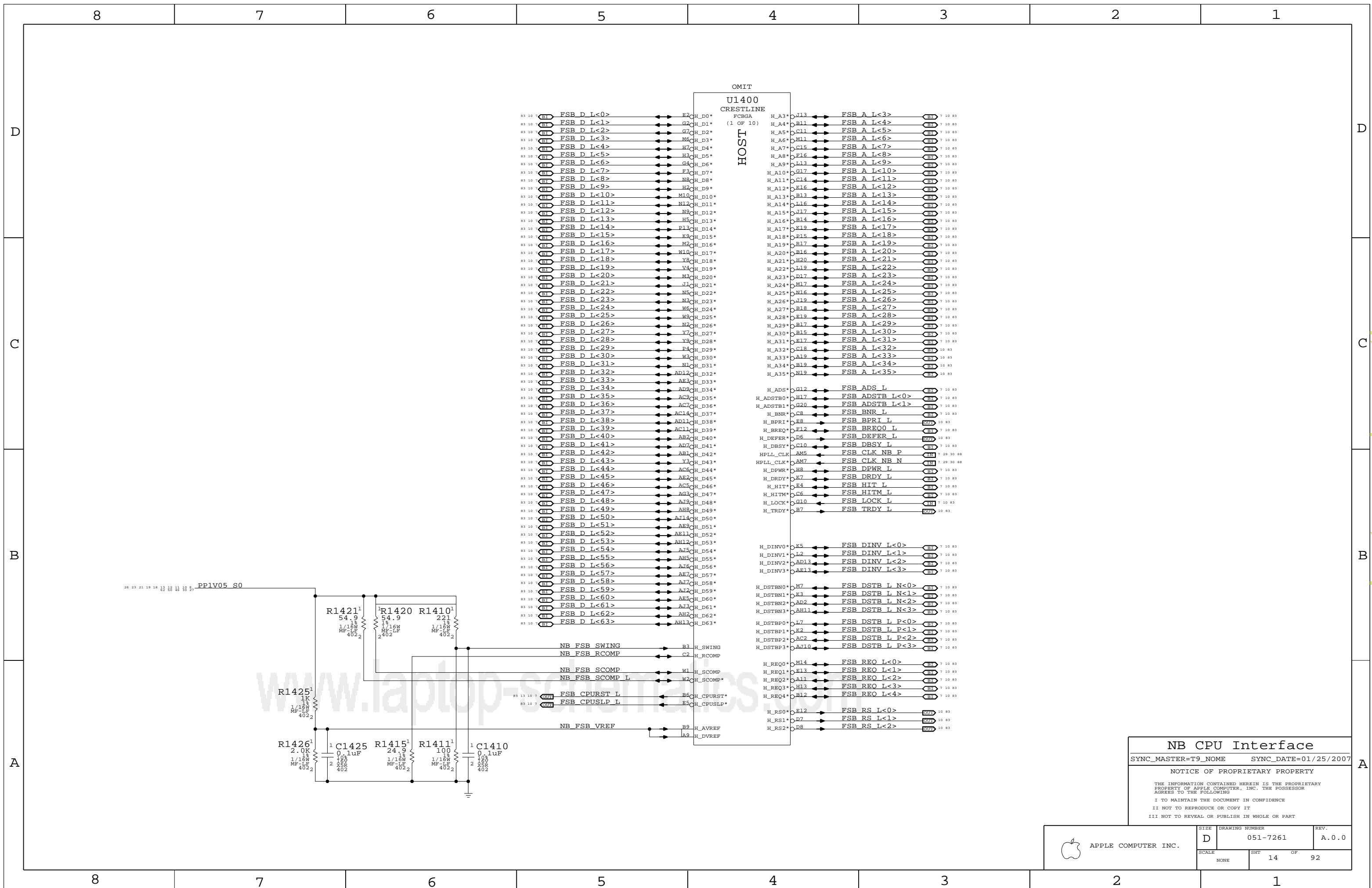
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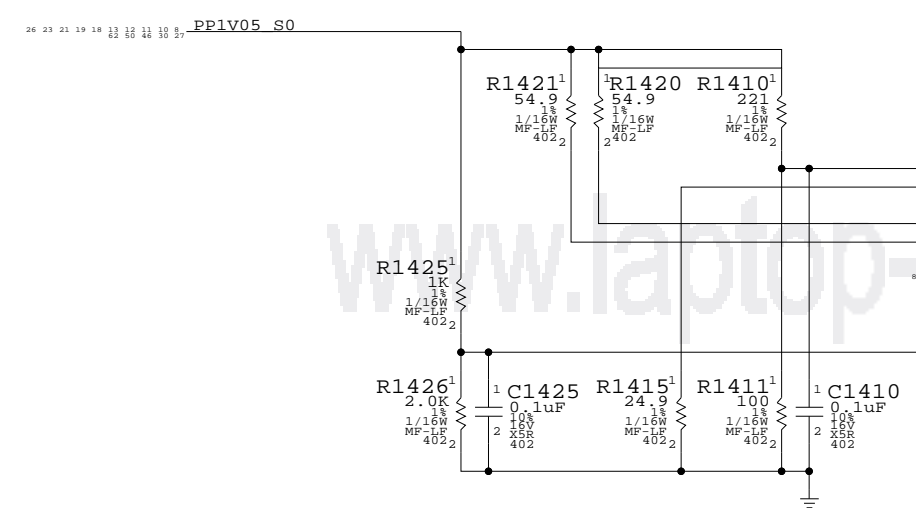
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1



OMIT
U1400
CRESTLINE
(1 OF 10)

Host Pin	Host Label	U1400 Pin	U1400 Label
7 10 83	J13	H_A3*	FSB A L<3>
7 10 83	B11	H_A4*	FSB A L<4>
7 10 83	C11	H_A5*	FSB A L<5>
7 10 83	M11	H_A6*	FSB A L<6>
7 10 83	C15	H_A7*	FSB A L<7>
7 10 83	F16	H_A8*	FSB A L<8>
7 10 83	L13	H_A9*	FSB A L<9>
7 10 83	G17	H_A10*	FSB A L<10>
7 10 83	C14	H_A11*	FSB A L<11>
7 10 83	K16	H_A12*	FSB A L<12>
7 10 83	B13	H_A13*	FSB A L<13>
7 10 83	L16	H_A14*	FSB A L<14>
7 10 83	J17	H_A15*	FSB A L<15>
7 10 83	B14	H_A16*	FSB A L<16>
7 10 83	K19	H_A17*	FSB A L<17>
7 10 83	P15	H_A18*	FSB A L<18>
7 10 83	R17	H_A19*	FSB A L<19>
7 10 83	B16	H_A20*	FSB A L<20>
7 10 83	H20	H_A21*	FSB A L<21>
7 10 83	L19	H_A22*	FSB A L<22>
7 10 83	D17	H_A23*	FSB A L<23>
7 10 83	M17	H_A24*	FSB A L<24>
7 10 83	N16	H_A25*	FSB A L<25>
7 10 83	J19	H_A26*	FSB A L<26>
7 10 83	B18	H_A27*	FSB A L<27>
7 10 83	E19	H_A28*	FSB A L<28>
7 10 83	B17	H_A29*	FSB A L<29>
7 10 83	B15	H_A30*	FSB A L<30>
7 10 83	E17	H_A31*	FSB A L<31>
7 10 83	C18	H_A32*	FSB A L<32>
7 10 83	A19	H_A33*	FSB A L<33>
7 10 83	B19	H_A34*	FSB A L<34>
7 10 83	N19	H_A35*	FSB A L<35>
7 10 83	G12	H_ADS*	FSB ADS L
7 10 83	H17	H_ADSTB0*	FSB ADSTB L<0>
7 10 83	G20	H_ADSTB1*	FSB ADSTB L<1>
7 10 83	C8	H_BNR*	FSB BNR L
7 10 83	E8	H_BPRI*	FSB BPRI L
7 10 83	F12	H_BREQ*	FSB BREQ L
7 10 83	D6	H_DEFER*	FSB DEFER L
7 10 83	C10	H_DBSY*	FSB DBSY L
7 29 30 88	A M5	HPLL_CLK*	FSB CLK NB P
7 29 30 88	A M7	HPLL_CLK*	FSB CLK NB N
7 10 83	H8	H_DPWR*	FSB DPWR L
7 10 83	K7	H_DRDY*	FSB DRDY L
7 10 83	E4	H_HIT*	FSB HIT L
7 10 83	C6	H_HITM*	FSB HITM L
7 10 83	G10	H_LOCK*	FSB LOCK L
7 10 83	B7	H_TRDY*	FSB TRDY L
7 10 83	K5	H_DINV0*	FSB DINV L<0>
7 10 83	L2	H_DINV1*	FSB DINV L<1>
7 10 83	AD13	H_DINV2*	FSB DINV L<2>
7 10 83	AE13	H_DINV3*	FSB DINV L<3>
7 10 83	M7	H_DSTBN0*	FSB DSTB L N<0>
7 10 83	K3	H_DSTBN1*	FSB DSTB L N<1>
7 10 83	AD2	H_DSTBN2*	FSB DSTB L N<2>
7 10 83	AH11	H_DSTBN3*	FSB DSTB L N<3>
7 10 83	L7	H_DSTBP0*	FSB DSTB L P<0>
7 10 83	K2	H_DSTBP1*	FSB DSTB L P<1>
7 10 83	AC2	H_DSTBP2*	FSB DSTB L P<2>
7 10 83	AW10	H_DSTBP3*	FSB DSTB L P<3>
7 10 83	M14	H_REQ0*	FSB REO L<0>
7 10 83	E13	H_REQ1*	FSB REO L<1>
7 10 83	A11	H_REQ2*	FSB REO L<2>
7 10 83	H13	H_REQ3*	FSB REO L<3>
7 10 83	B12	H_REQ4*	FSB REO L<4>
7 10 83	E12	H_RS0*	FSB RS L<0>
7 10 83	D7	H_RS1*	FSB RS L<1>
7 10 83	D8	H_RS2*	FSB RS L<2>



NB CPU Interface
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	14		92

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LVDS Disable

Can leave all signals NC if LVDS is not implemented. Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

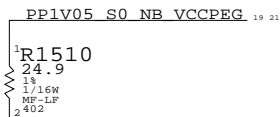
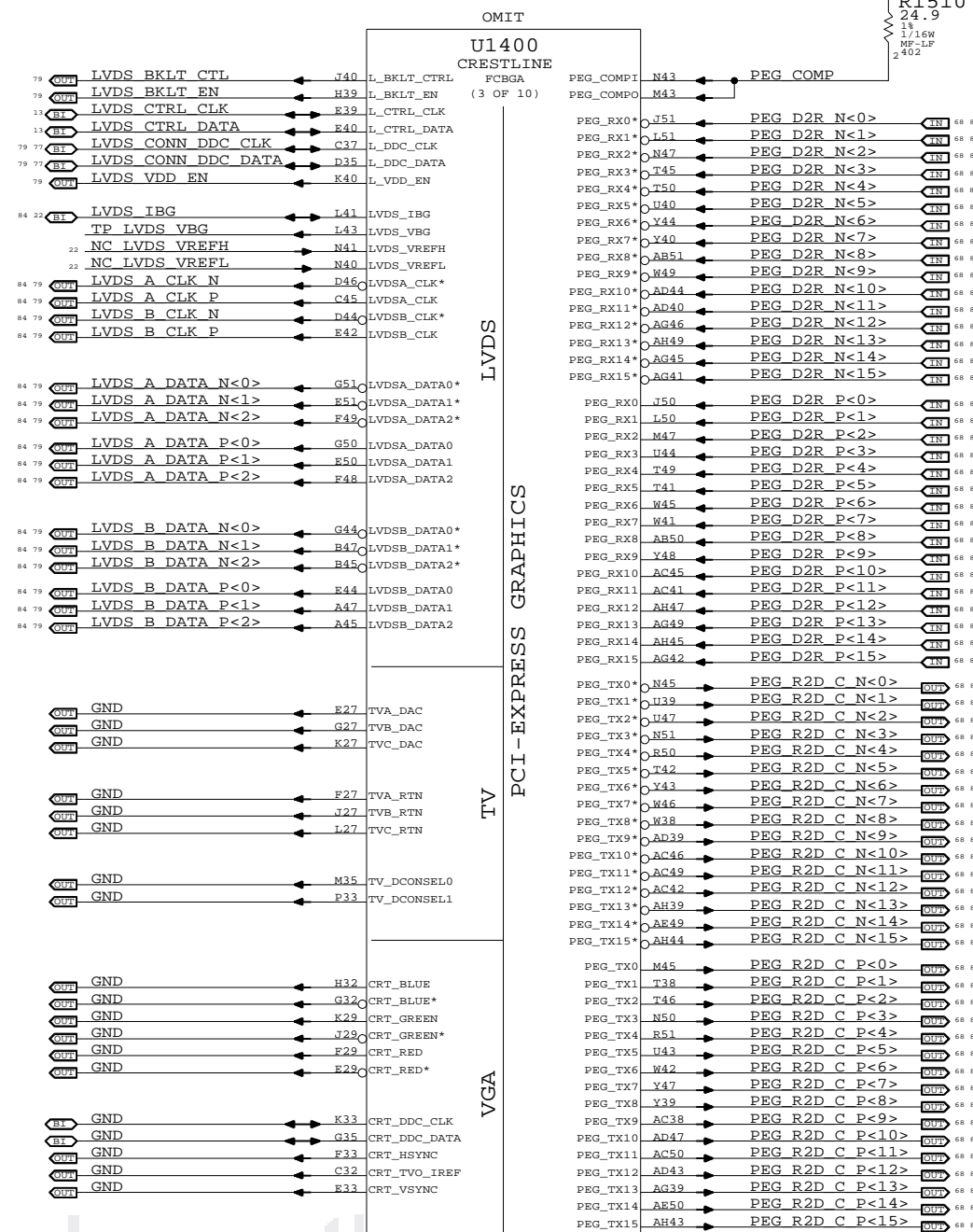
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND. Can tie the following rails to GND: VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC*, L_CTRL*, L_DDC*, SDVO_CTRL* and TV_DCONSELx to GND. Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND. Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore). Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore). Tie VCC_AXG and VCC_AXG_NCTF to GND. Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

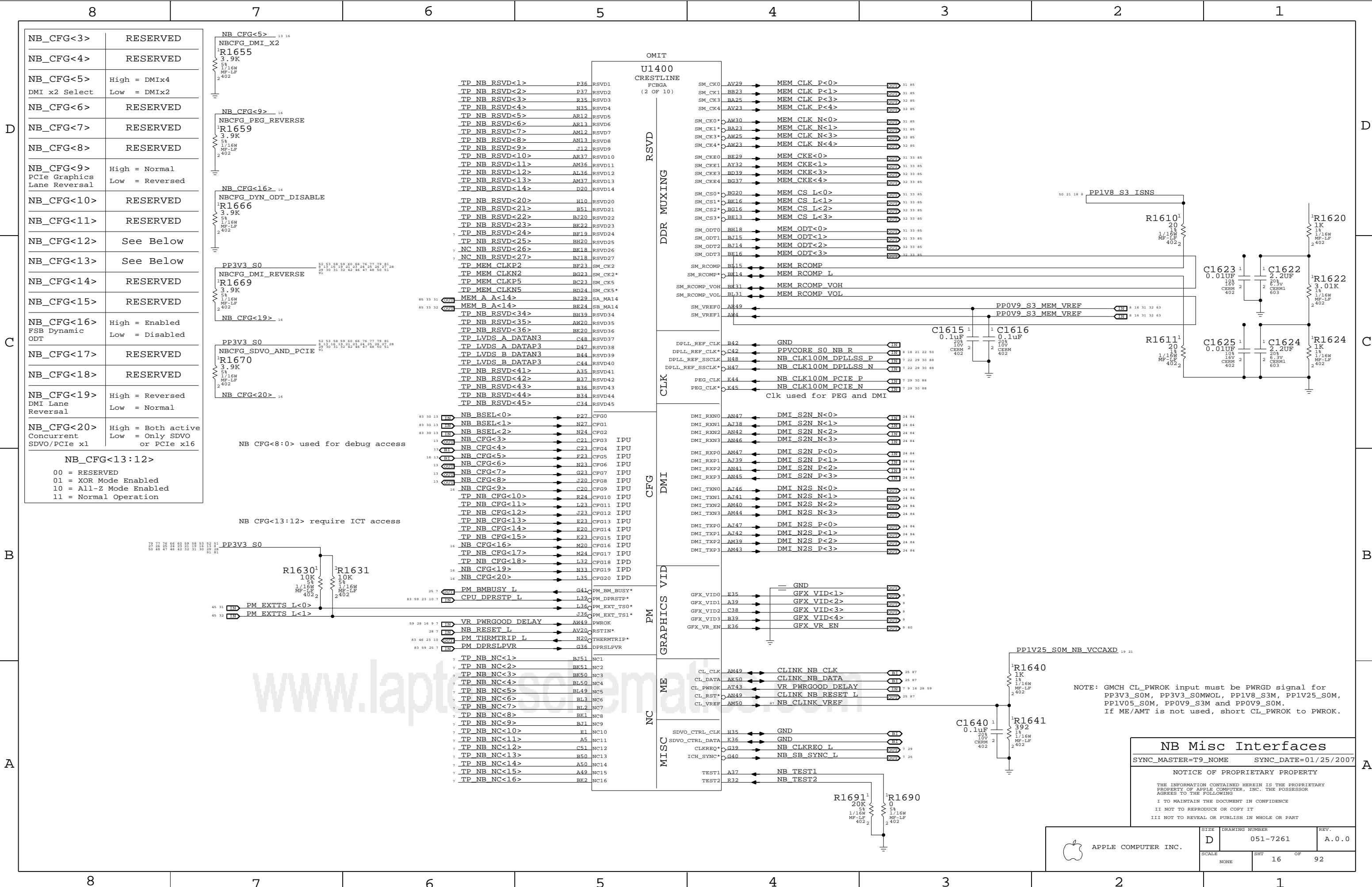
NB PEG / Video Interfaces
SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

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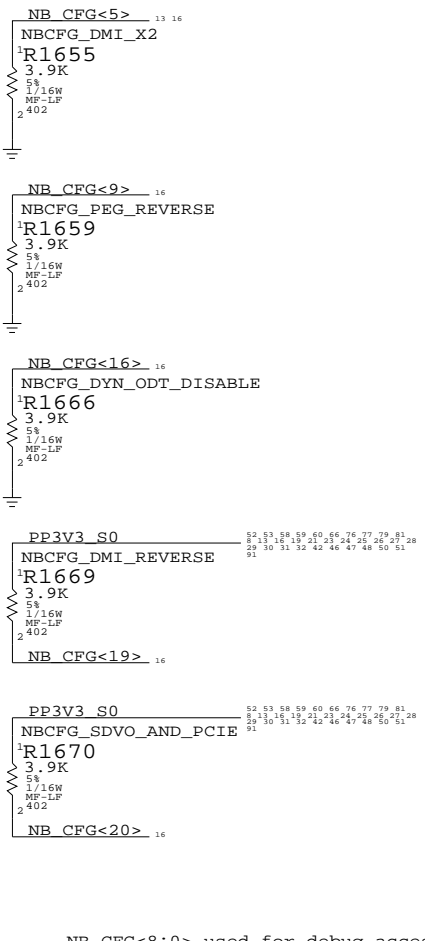
Table with columns: SCALE, DRAWING NUMBER, SHEET, OF, REV. Values: NONE, 051-7261, 15, 92, A.0.0



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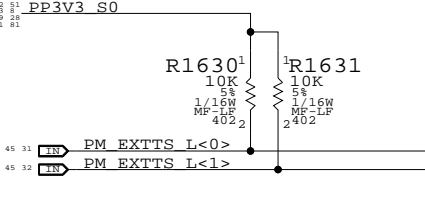
NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent Low = Only SDVO SDVO/PCIe x1 or PCIe x16



NB_CFG<8:0> used for debug access

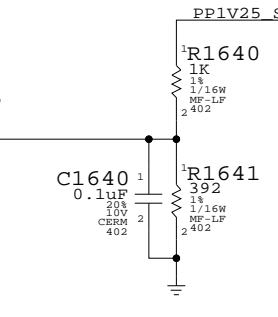
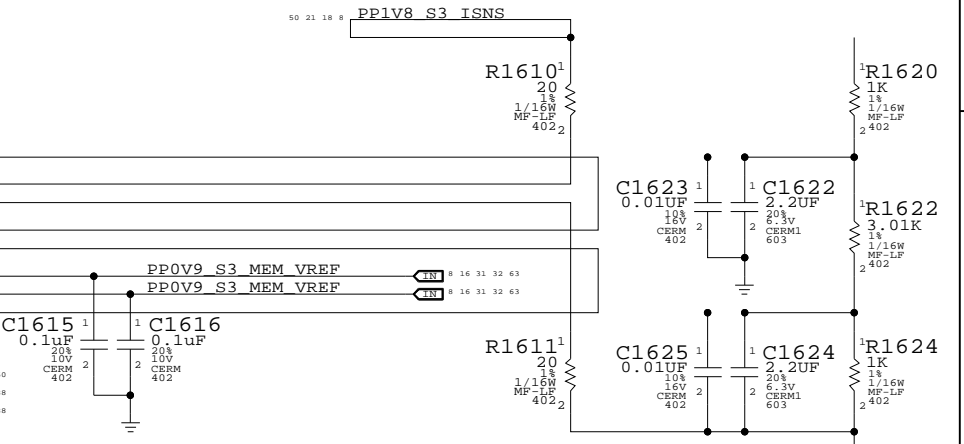
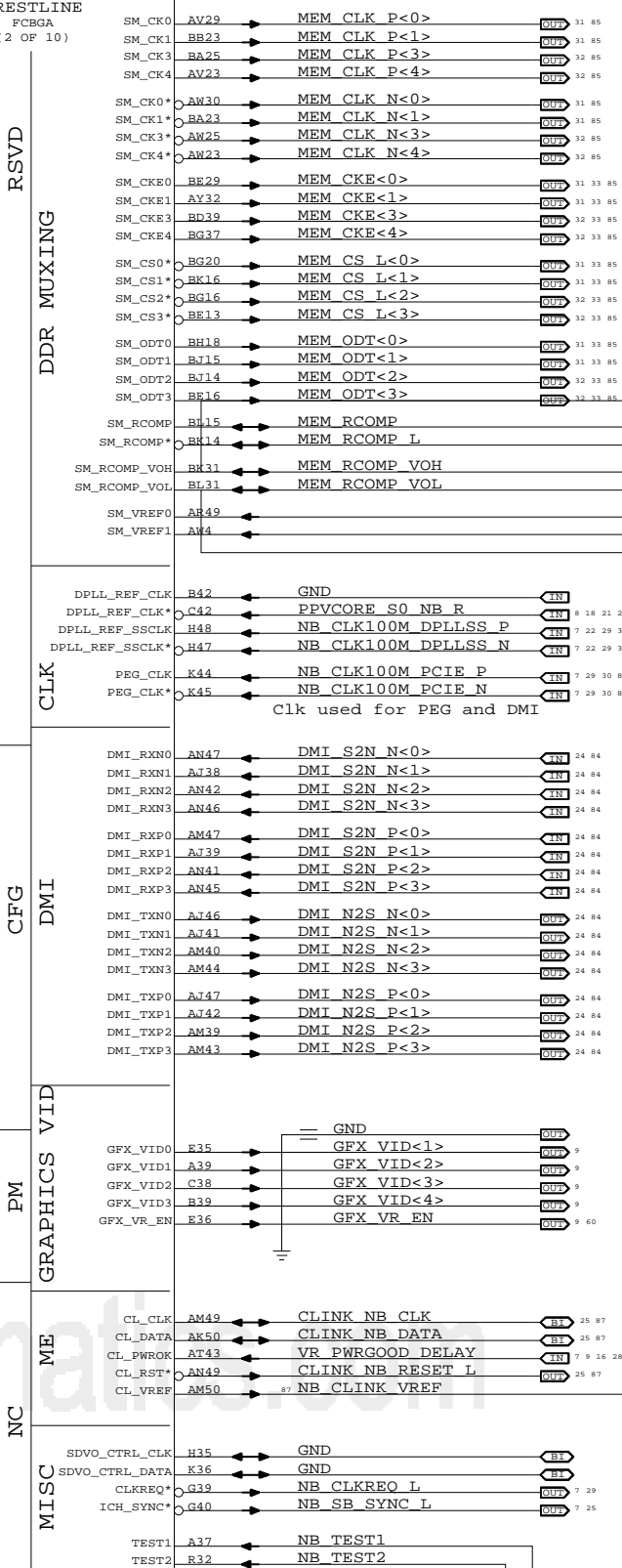
NB_CFG<13:12>
00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<13:12> require ICT access



U1400 CRESTLINE (2 OF 10)

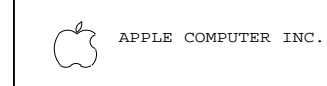
TP NB_RSVD<1>	P36	RSVD1
TP NB_RSVD<2>	P37	RSVD2
TP NB_RSVD<3>	R35	RSVD3
TP NB_RSVD<4>	N35	RSVD4
TP NB_RSVD<5>	AR12	RSVD5
TP NB_RSVD<6>	AR13	RSVD6
TP NB_RSVD<7>	AM12	RSVD7
TP NB_RSVD<8>	AM13	RSVD8
TP NB_RSVD<9>	J12	RSVD9
TP NB_RSVD<10>	AR37	RSVD10
TP NB_RSVD<11>	AM36	RSVD11
TP NB_RSVD<12>	AL36	RSVD12
TP NB_RSVD<13>	AM37	RSVD13
TP NB_RSVD<14>	D20	RSVD14
TP NB_RSVD<20>	H10	RSVD20
TP NB_RSVD<21>	B51	RSVD21
TP NB_RSVD<22>	BK20	RSVD22
TP NB_RSVD<23>	BK22	RSVD23
TP NB_RSVD<24>	BF19	RSVD24
TP NB_RSVD<25>	BH20	RSVD25
NC NB_RSVD<26>	BK18	RSVD26
NC NB_RSVD<27>	BL18	RSVD27
TP MEM_CLKP2	BE23	SM_CK2
TP MEM_CLKN2	EG23	SM_CK2*
TP MEM_CLKP5	BC23	SM_CK5
TP MEM_CLKN5	BD24	SM_CK5*
MEM A A<14>	BT29	SA_MA14
MEM B A<14>	BE24	SB_MA14
TP NB_RSVD<34>	BH39	RSVD34
TP NB_RSVD<35>	AW20	RSVD35
TP NB_RSVD<36>	BK20	RSVD36
TP LVDS A DATAN3	C48	RSVD37
TP LVDS A DATAP3	D47	RSVD38
TP LVDS B DATAN3	B44	RSVD39
TP LVDS B DATAP3	C44	RSVD40
TP NB_RSVD<41>	A35	RSVD41
TP NB_RSVD<42>	B37	RSVD42
TP NB_RSVD<43>	B36	RSVD43
TP NB_RSVD<44>	B34	RSVD44
TP NB_RSVD<45>	C34	RSVD45
NB_BSEL<0>	P27	CFG0
NB_BSEL<1>	N27	CFG1
NB_BSEL<2>	N24	CFG2
NB_CFG<3>	C21	CFG3 IPU
NB_CFG<4>	C23	CFG4 IPU
NB_CFG<5>	F23	CFG5 IPU
NB_CFG<6>	N23	CFG6 IPU
NB_CFG<7>	G23	CFG7 IPU
NB_CFG<8>	J20	CFG8 IPU
NB_CFG<9>	C20	CFG9 IPU
TP NB_CFG<10>	R24	CFG10 IPU
TP NB_CFG<11>	L23	CFG11 IPU
TP NB_CFG<12>	J23	CFG12 IPU
TP NB_CFG<13>	E23	CFG13 IPU
TP NB_CFG<14>	E20	CFG14 IPU
TP NB_CFG<15>	K23	CFG15 IPU
NB_CFG<16>	M20	CFG16 IPU
TP NB_CFG<17>	M24	CFG17 IPU
TP NB_CFG<18>	L32	CFG18 IPD
NB_CFG<19>	N33	CFG19 IPD
NB_CFG<20>	L35	CFG20 IPD
PM_BMBUSY L	G41	PM_BMBUSY*
CPU DPRSTP L	L39	PM_DPRSTP*
	L36	PM_EXT_TSO*
	J36	PM_EXT_TS1*
VR_PWRGOOD DELAY	AW49	PWROK
NB_RESET L	AV20	RSTIN*
PM_THRMTRIP L	N20	THERMTRIP*
PM DPRSLPVR	G36	DPRSLPVR
TP NB_NC<1>	BJ51	NC1
TP NB_NC<2>	BK51	NC2
TP NB_NC<3>	BK50	NC3
TP NB_NC<4>	BL50	NC4
TP NB_NC<5>	BL49	NC5
TP NB_NC<6>	BL3	NC6
TP NB_NC<7>	BL2	NC7
TP NB_NC<8>	BK1	NC8
TP NB_NC<9>	BJ1	NC9
TP NB_NC<10>	E1	NC10
TP NB_NC<11>	A5	NC11
TP NB_NC<12>	C51	NC12
TP NB_NC<13>	B50	NC13
TP NB_NC<14>	A50	NC14
TP NB_NC<15>	A49	NC15
TP NB_NC<16>	BK2	NC16



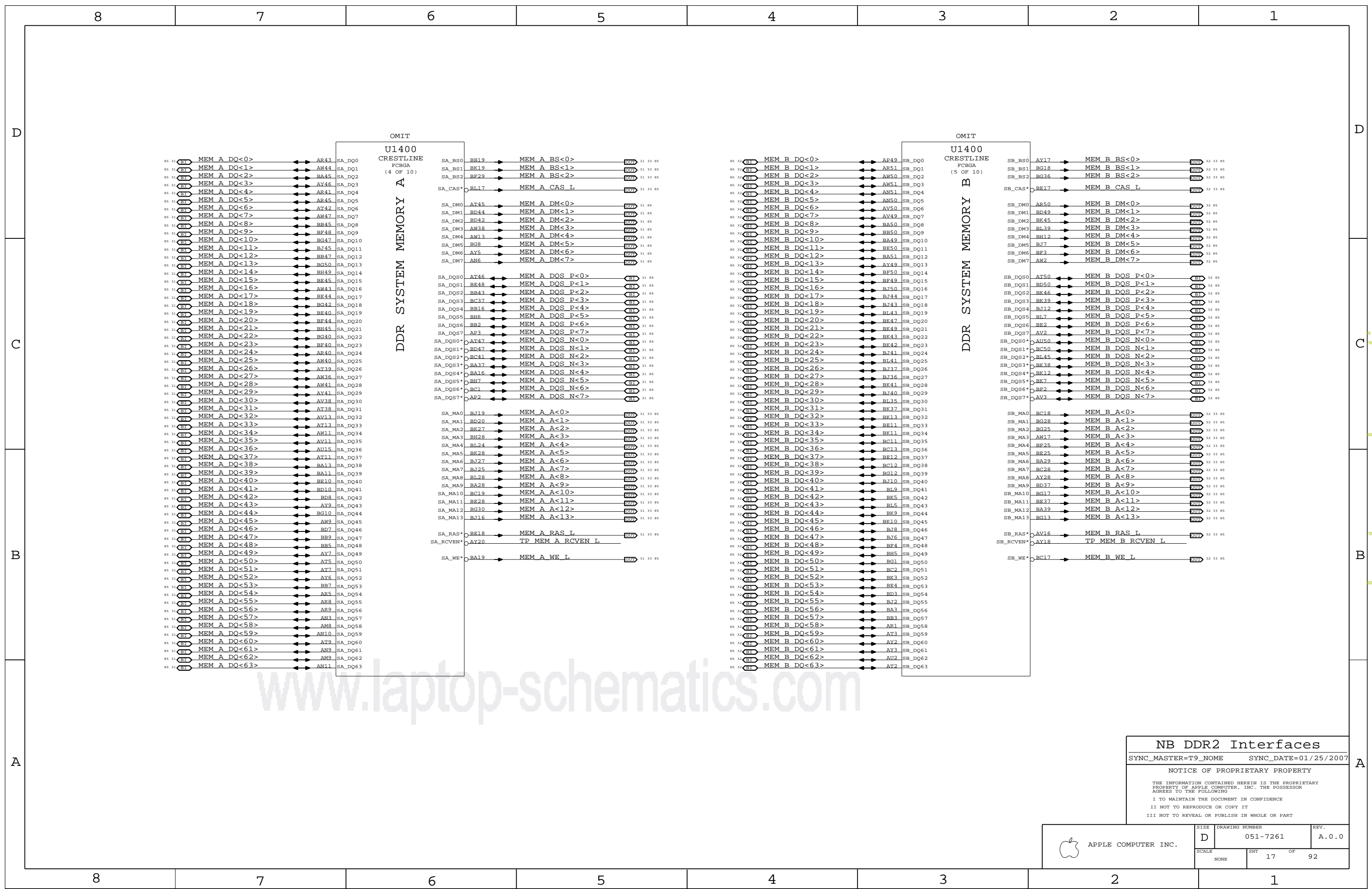
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	
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SCALE	SHT	OF
NONE	16	92



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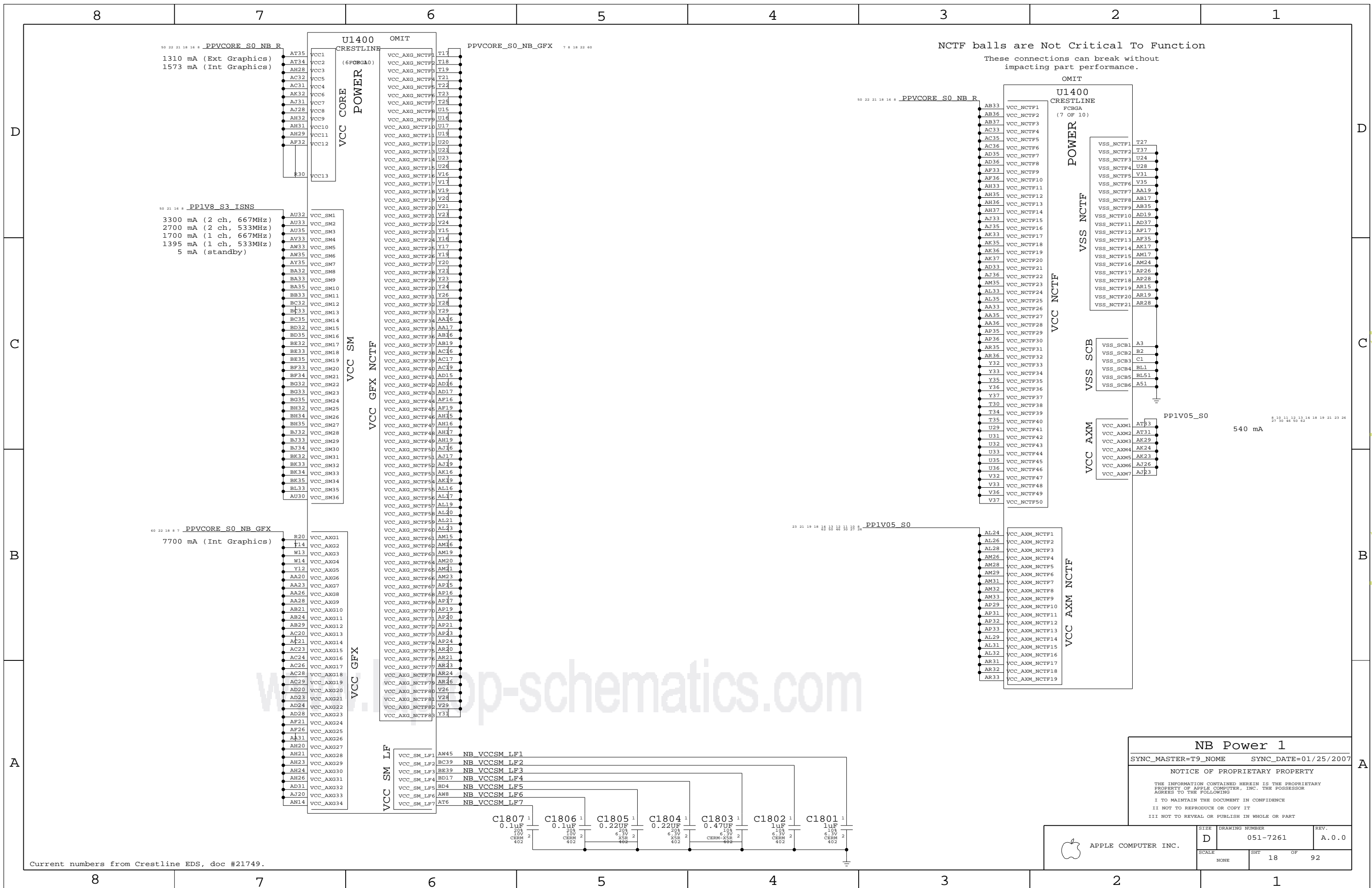


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NB DDR2 Interfaces
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SCALE	SHT	OF	
NONE	17	92	



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.

50 22 21 18 16 8 PPVCORE_S0_NB_R
 1310 mA (Ext Graphics)
 1573 mA (Int Graphics)

50 21 16 8 PP1V8_S3_ISNS
 3300 mA (2 ch, 667MHz)
 2700 mA (2 ch, 533MHz)
 1700 mA (1 ch, 667MHz)
 1395 mA (1 ch, 533MHz)
 5 mA (standby)

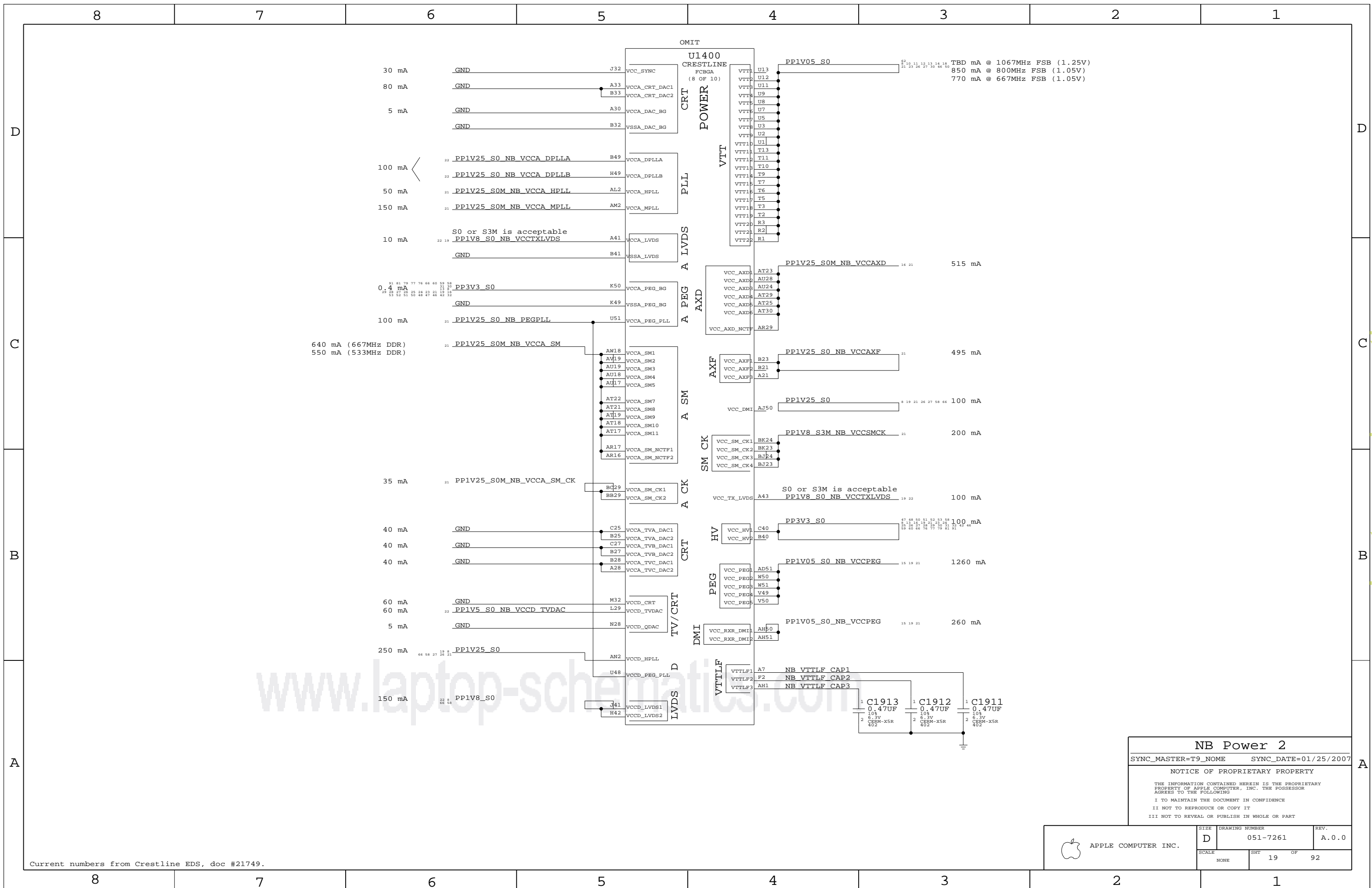
60 22 18 8 7 PPVCORE_S0_NB_GFX
 7700 mA (Int Graphics)

NB Power 1
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	18	92	A.0.0

Current numbers from Crestline EDS, doc #21749.

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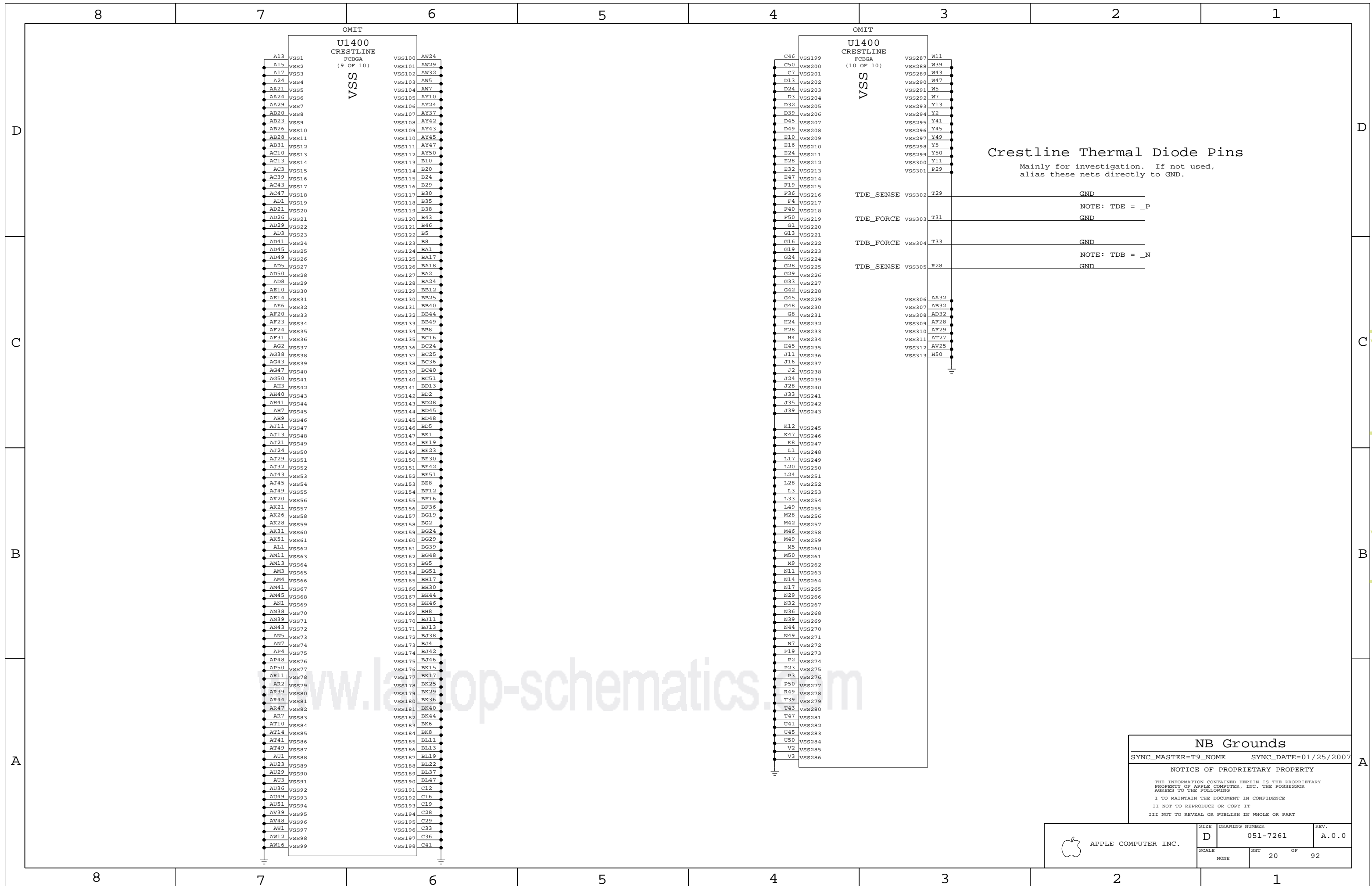


Current numbers from Crestline EDS, doc #21749.

NB Power 2
 SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007
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	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	19		92

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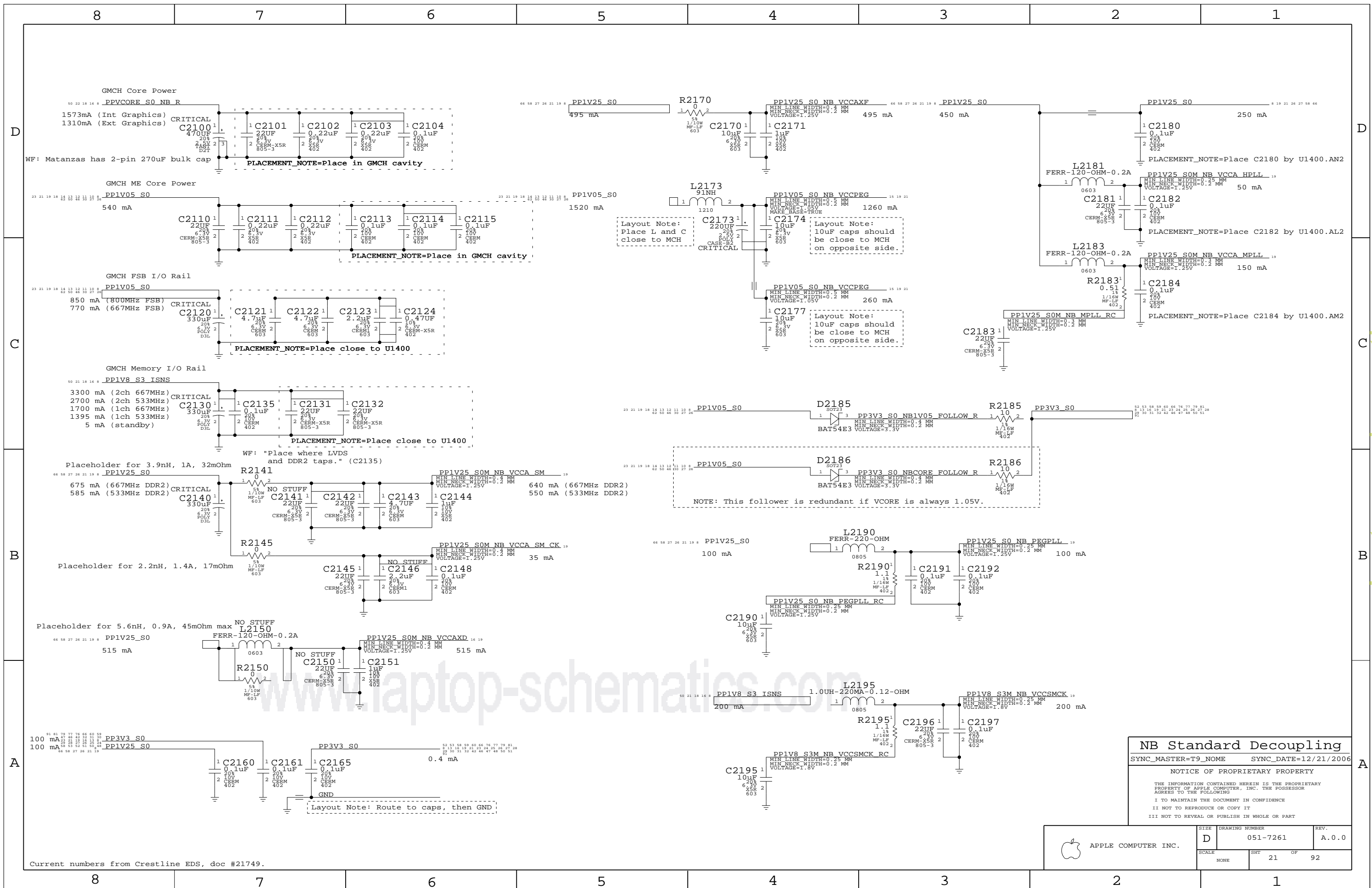
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Crestline Thermal Diode Pins
 Mainly for investigation. If not used,
 alias these nets directly to GND.

NB Grounds
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SCALE	SHT		OF
NONE	20		92

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NB Standard Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=12/21/2006

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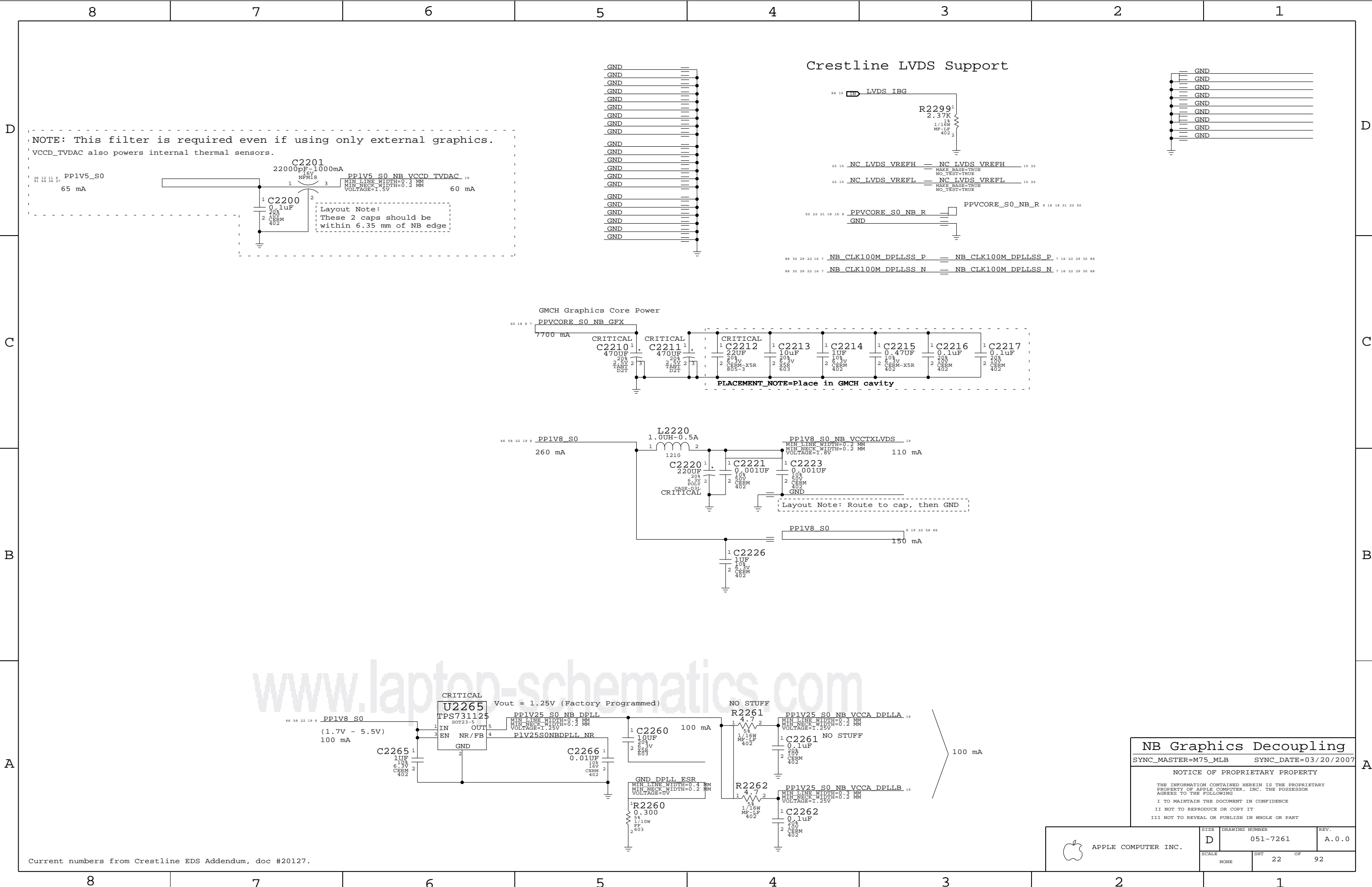
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SCALE NONE	SHEET 21	OF 92	SIZE	DRAWING NUMBER	REV.
			D	051-7261	A.0.0

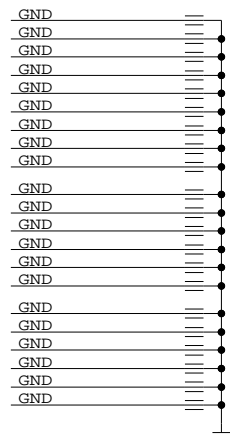
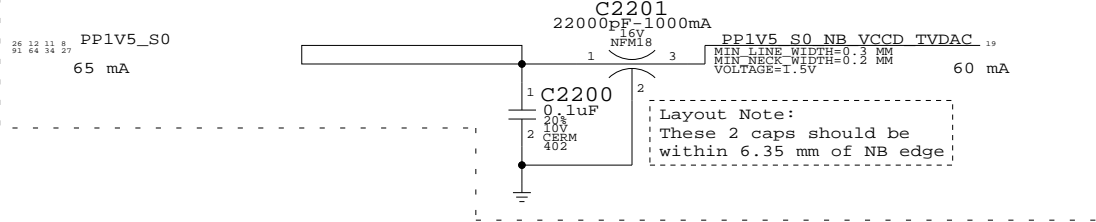


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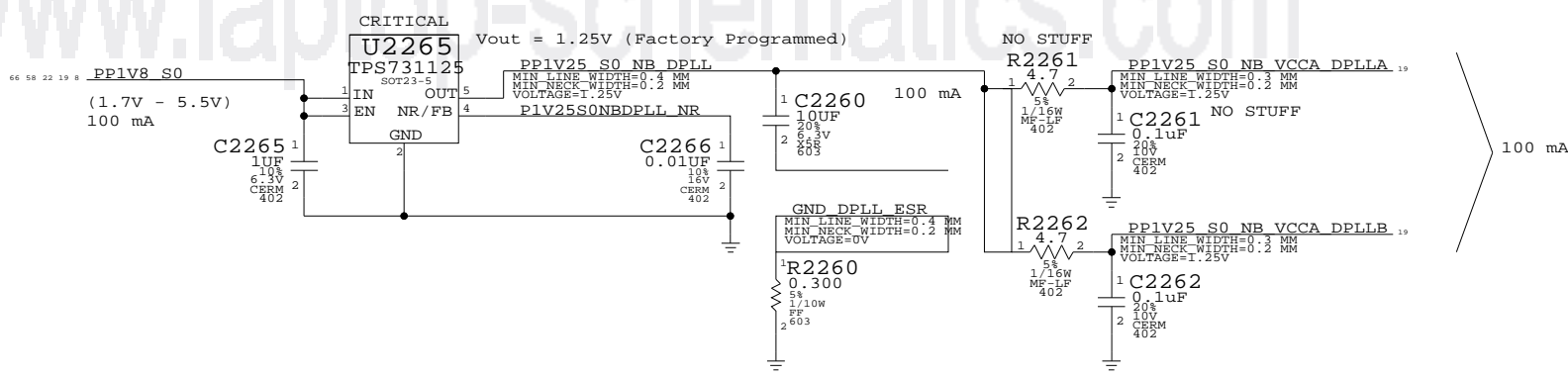
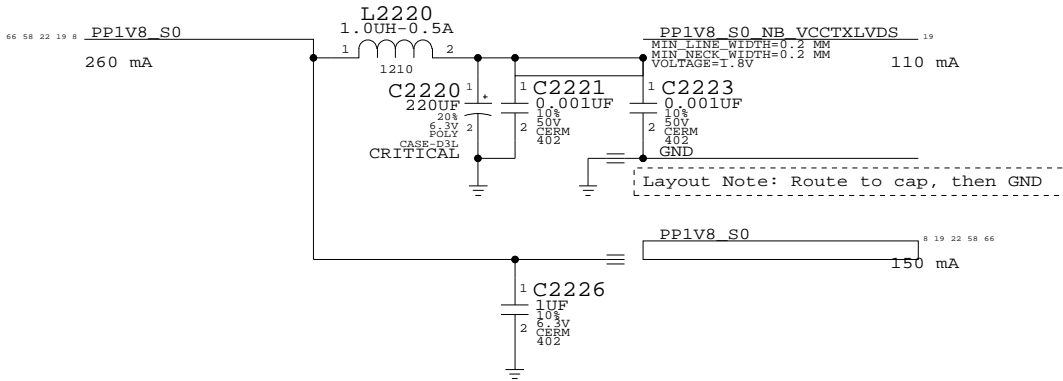
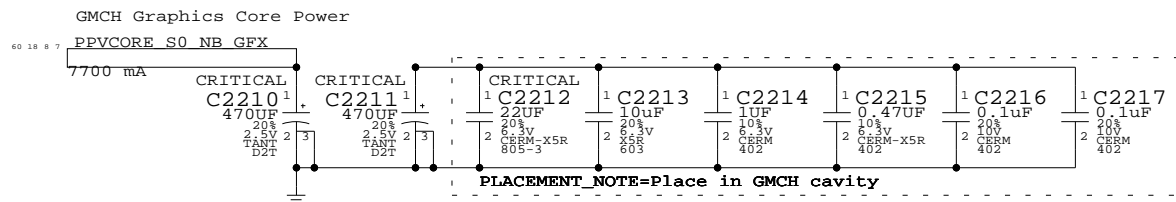
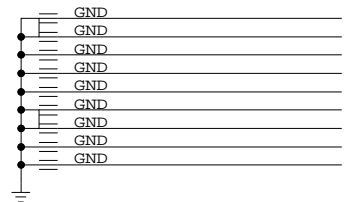
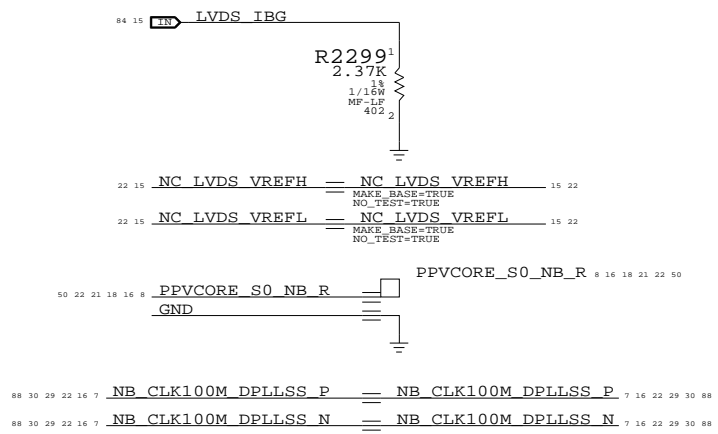
Current numbers from Crestline EDS, doc #21749.



NOTE: This filter is required even if using only external graphics.
 VCCD_TVDAC also powers internal thermal sensors.



Crestline LVDS Support



NB Graphics Decoupling

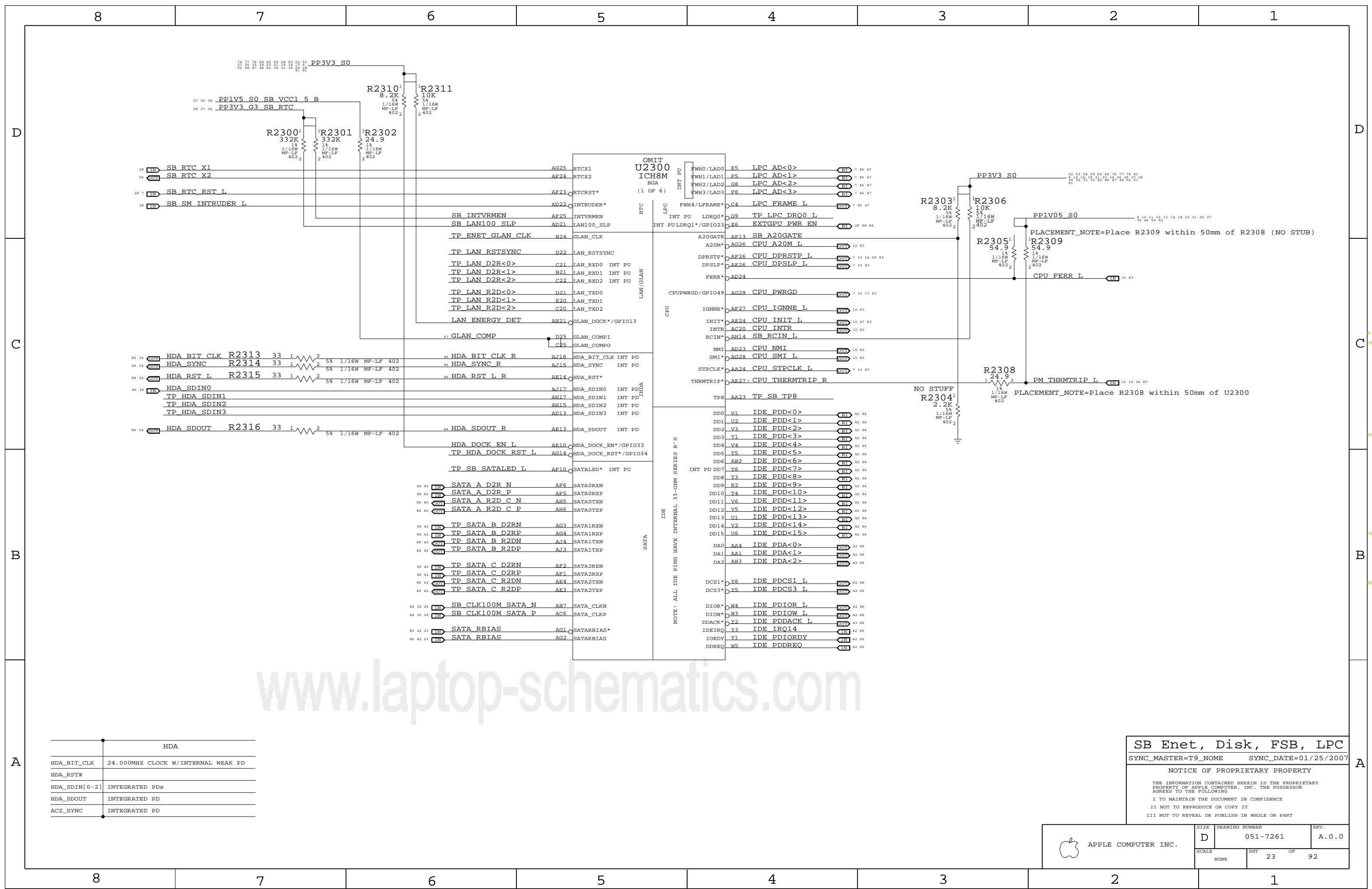
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NONE	22	92	

Current numbers from Crestline EDS Addendum, doc #20127.



SB Enet, Disk, FSB, LPC
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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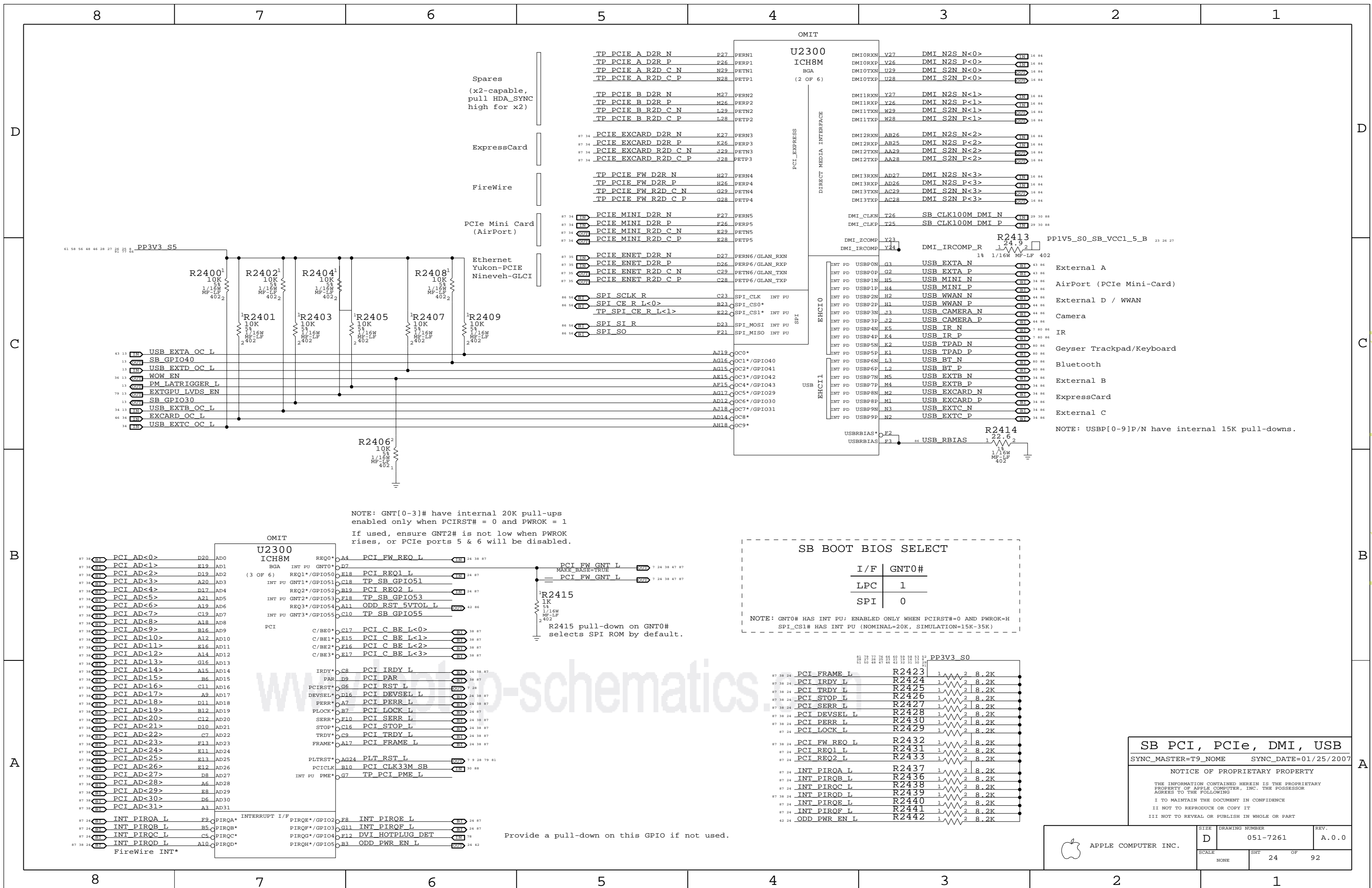
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	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	23	92	



NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

SB BOOT BIOS SELECT	
I/F	GNT0#
LPC	1
SPI	0

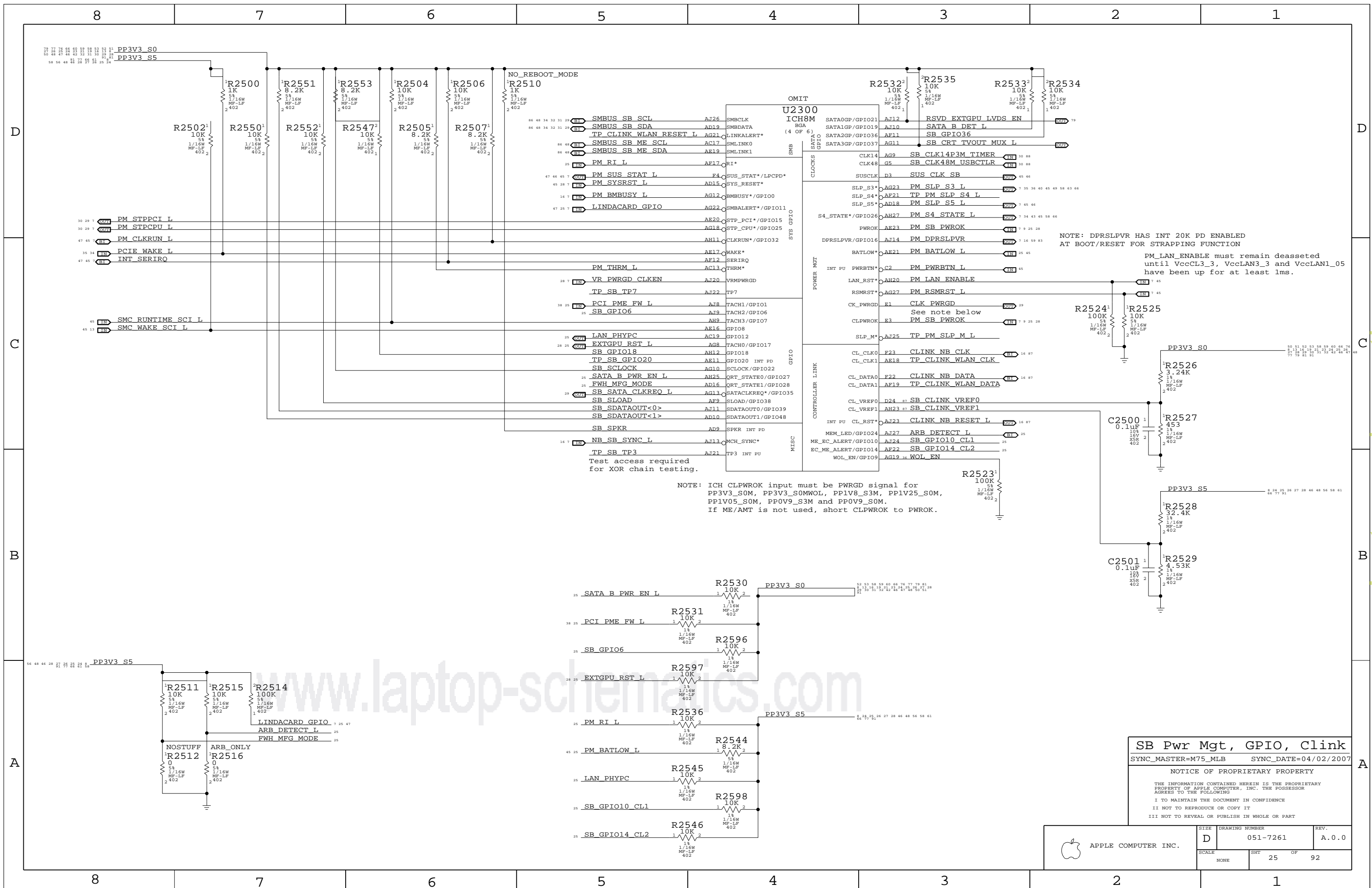
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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SCALE	SHT	OF	
NONE	24	92	

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NO_REBOOT_MODE

U2300 ICH8M BGA (4 OF 6)

86 48 34 32 31 29	SMBUS_SB_SCL	AJ26	SMBCLK
86 48 34 32 31 29	SMBUS_SB_SDA	AD19	SMBDATA
86 48 34 32 31 29	TP_CLINK_WLAN_RESET L	AG21	LINKALERT*
86 48 34 32 31 29	SMBUS_SB_ME_SCL	AC17	SMLINK0
86 48 34 32 31 29	SMBUS_SB_ME_SDA	AE19	SMLINK1
25	PM_RI L	AF17	RI*
47 46 45 7	PM_SUS_STAT L	F4	SUS_STAT*/LPCPD*
45 28 7	PM_SYSRST L	AD15	SYS_RESET*
16 7	PM_BMBUSY L	AG12	BMBUSY*/GPIO0
47 25 7	LINDACARD_GPIO	AG22	SMBALERT*/GPIO11
		AE20	STP_PCI*/GPIO15
		AG18	STP_CPU*/GPIO25
		AH11	CLKRUN*/GPIO32
		AE17	WAKE*
		AF12	SERIRQ
		AC13	THRM*
28 7	VR_PWRGD_CLKEN	AJ20	VRMPWRGD
		AJ22	TP7
38 25	PCI_PME_FW L	AJ8	TACH1/GPIO1
25	SB_GPIO6	AJ9	TACH2/GPIO6
		AH9	TACH3/GPIO7
		AE16	GPIO8
25	LAN_PHYPC	AC19	GPIO12
28 25	EXTGPU_RST L	AG8	TACH0/GPIO17
		AH12	GPIO18
		AE11	GPIO20 INT PD
		AG10	SCLOCK/GPIO22
25	SATA_B_PWR_EN L	AH25	QRT_STATE0/GPIO27
25	FWH_MFG_MODE	AD16	QRT_STATE1/GPIO28
29	SB_SATA_CLKREQ L	AG13	SATACLKREQ*/GPIO35
		AE9	SLOAD/GPIO38
		AJ11	SDATAOUT0/GPIO39
		AD10	SDATAOUT1/GPIO48
		AD9	SPKR INT PD
16 7	NB_SB_SYNC L	AJ13	MCH_SYNC*
		AJ21	TP3 INT PU

Test access required for XOR chain testing.

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasserted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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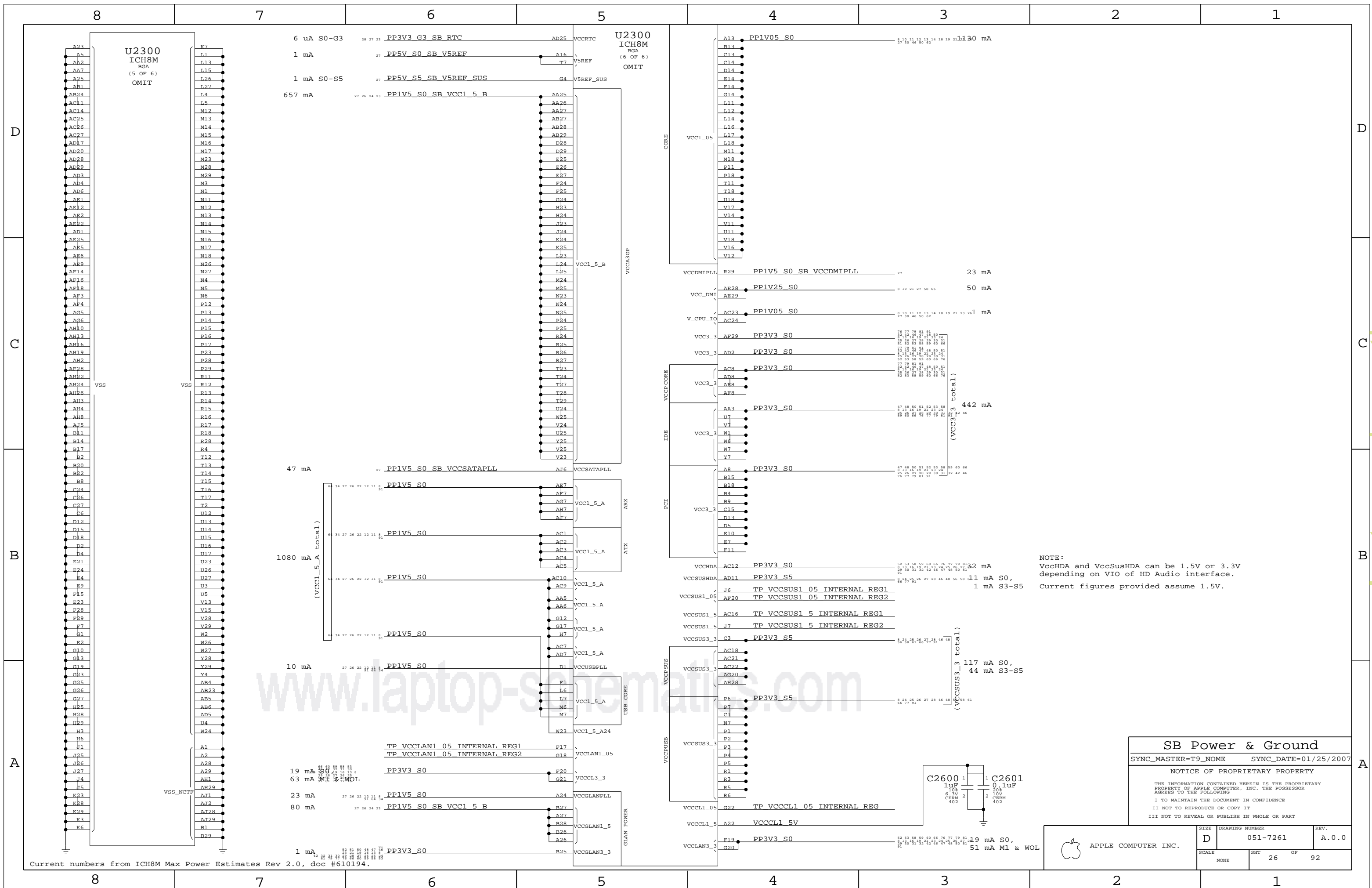
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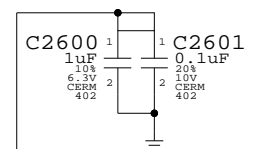
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	92
NONE	25		

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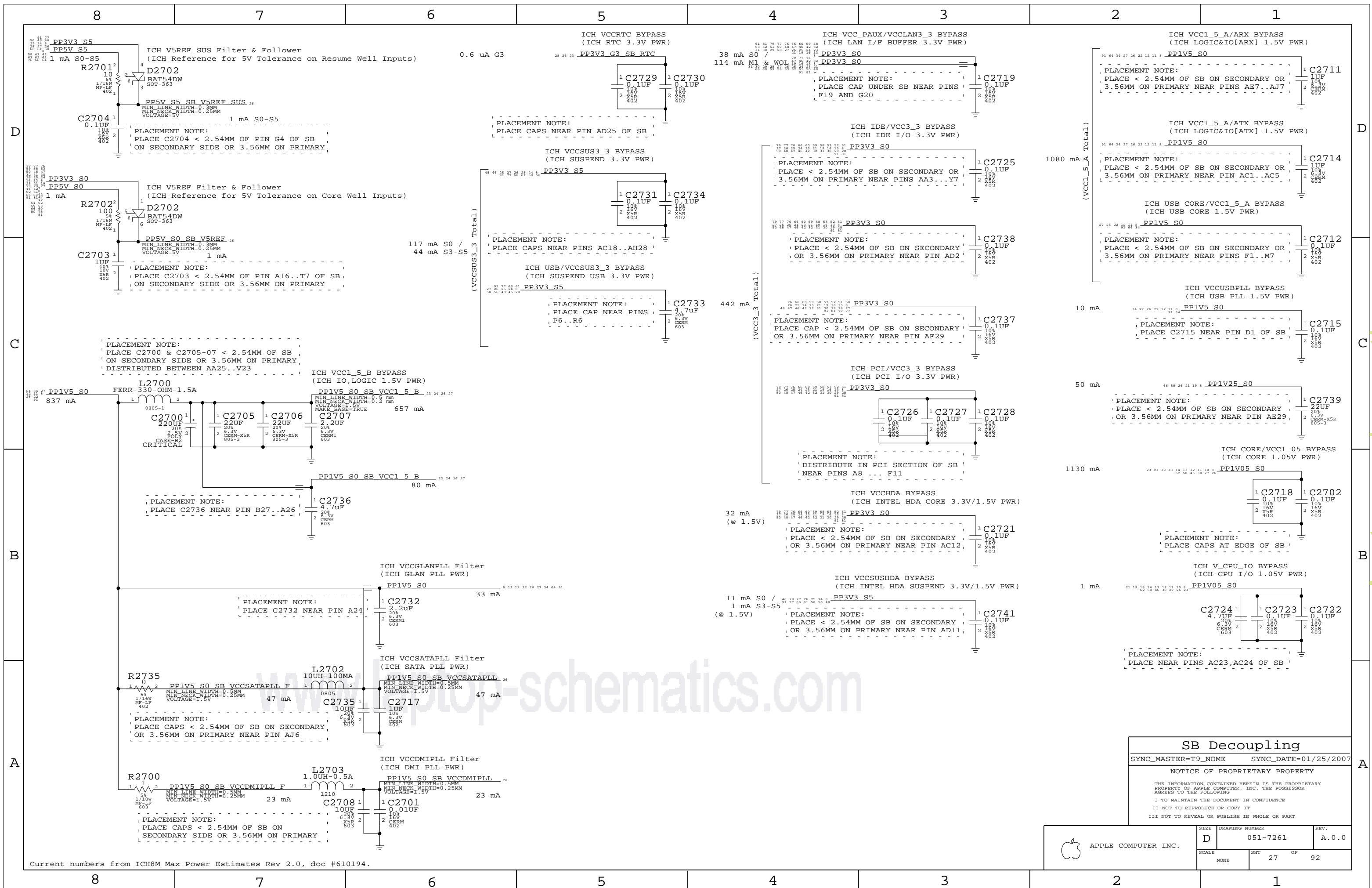


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NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.



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SB Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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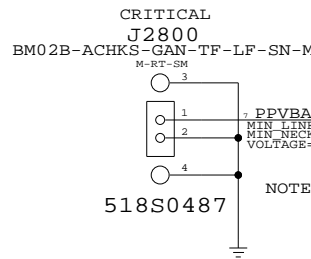
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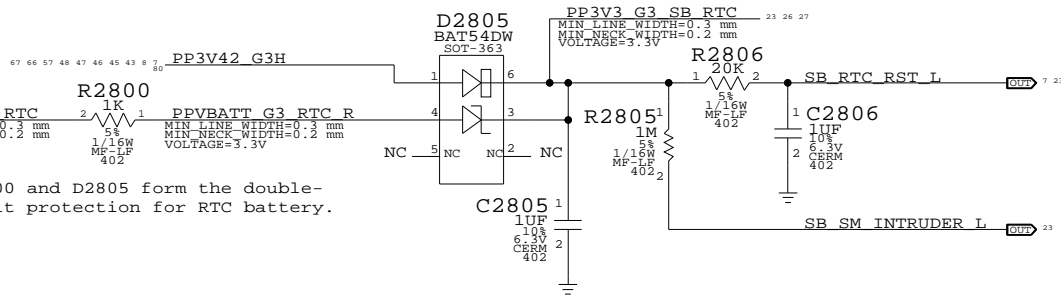
APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	27	92	A.0.0

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

Coin-Cell Connector

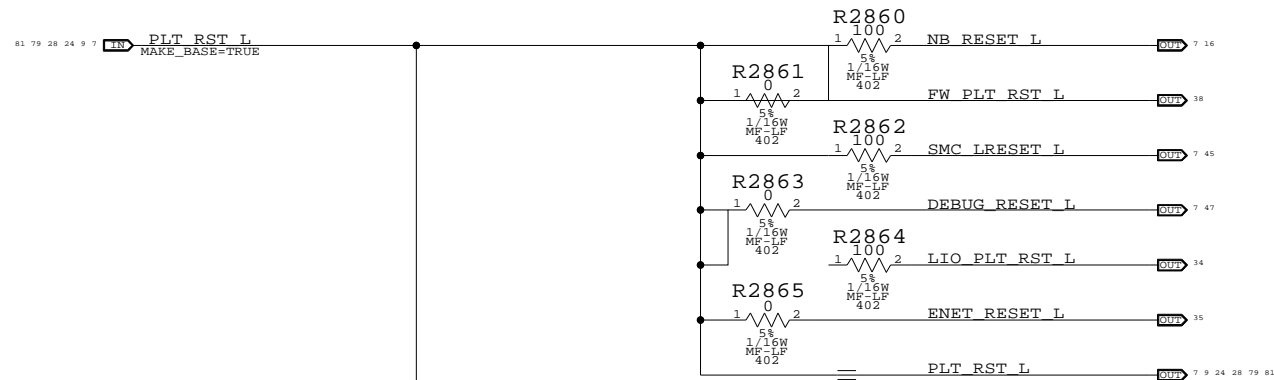


RTC Power Sources

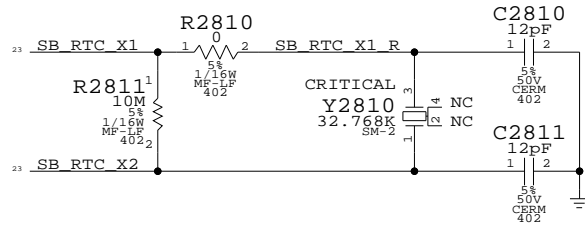


Platform Reset Connections

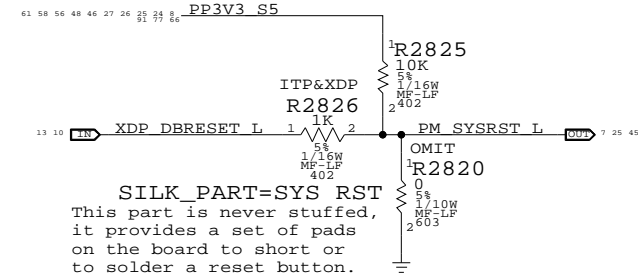
Unbuffered



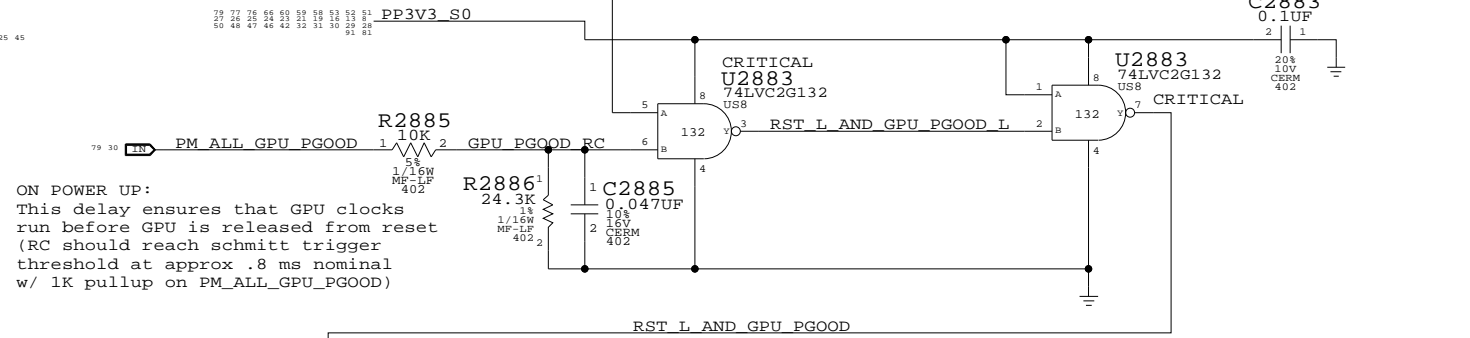
SB RTC Crystal



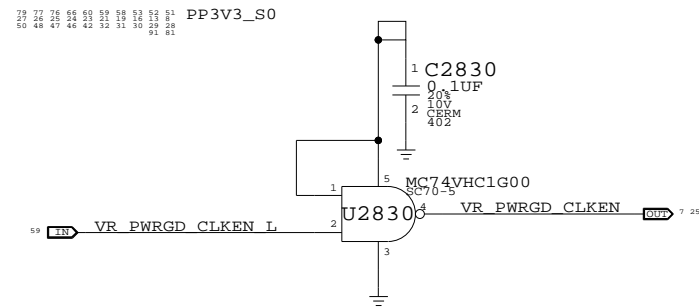
System Reset "Button"



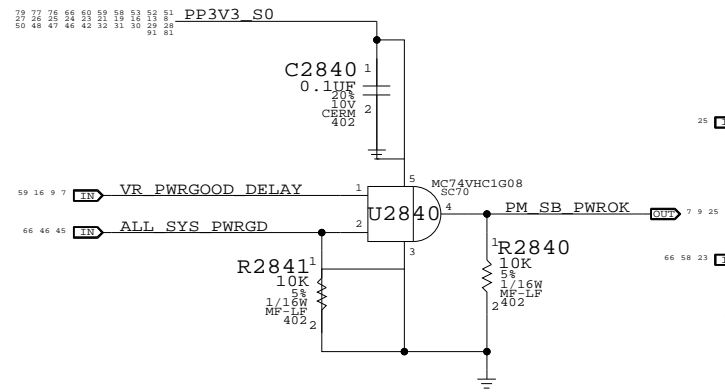
Muxed GFX GPU Reset Support



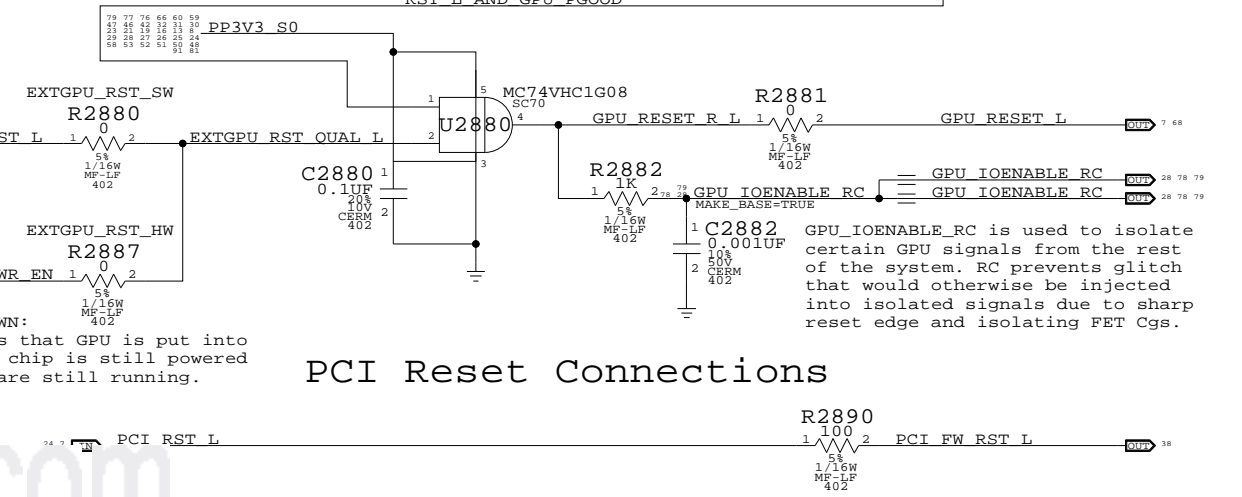
VRMPWRGD Inverter



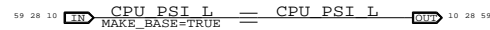
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI



SB Misc

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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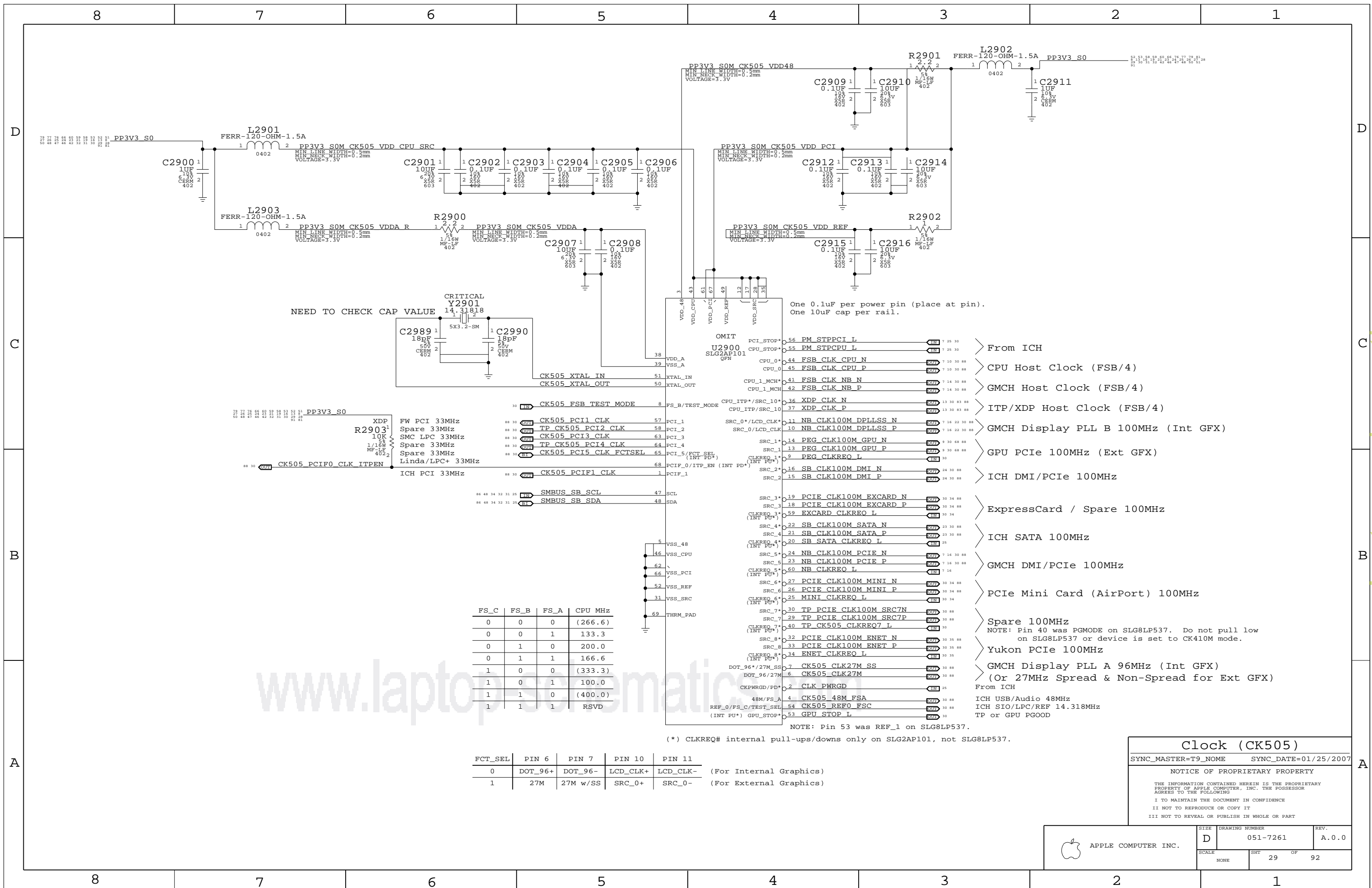
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SCALE	SHT	OF	REV.
NONE	28	92	

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NEED TO CHECK CAP VALUE

One 0.1uF per power pin (place at pin).
One 10uF cap per rail.

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

- From ICH
- CPU Host Clock (FSB/4)
- GMCH Host Clock (FSB/4)
- ITP/XDP Host Clock (FSB/4)
- GMCH Display PLL B 100MHz (Int GFX)
- GPU PCIe 100MHz (Ext GFX)
- ICH DMI/PCIe 100MHz
- ExpressCard / Spare 100MHz
- ICH SATA 100MHz
- GMCH DMI/PCIe 100MHz
- PCIe Mini Card (AirPort) 100MHz
- Spare 100MHz
- NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
- Yukon PCIe 100MHz
- GMCH Display PLL A 96MHz (Int GFX)
- (Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
- ICH SIO/LPC/REF 14.318MHz
- TP or GPU PGOOD

NOTE: Pin 53 was REF_1 on SLG8LP537.

(*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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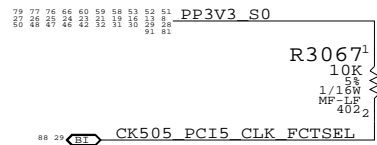
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	29	92	

CLK Termination

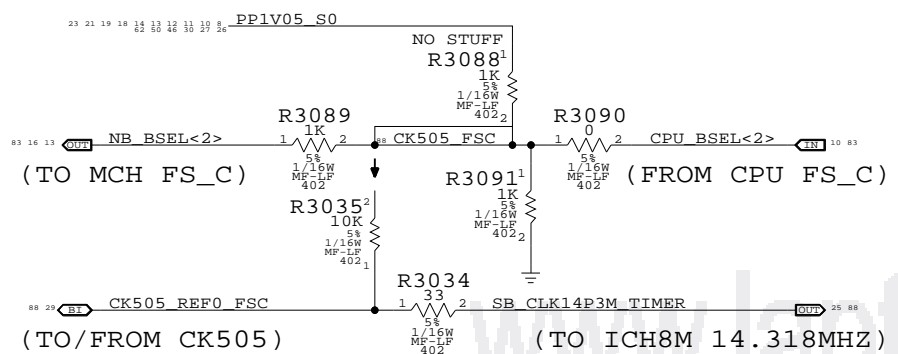
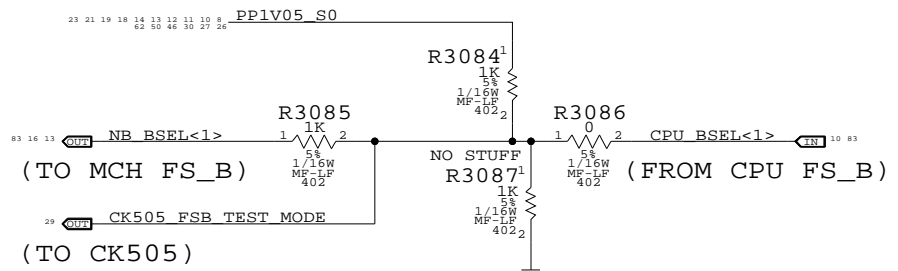
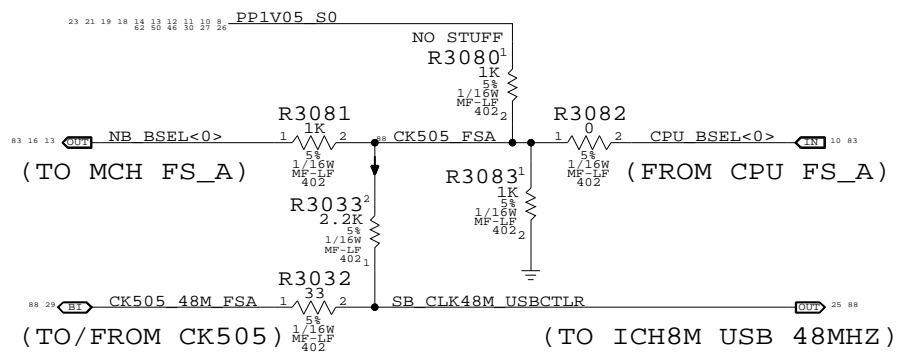
(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)

CK505 Configuration Straps

FCT_SEL (GFX clock select)



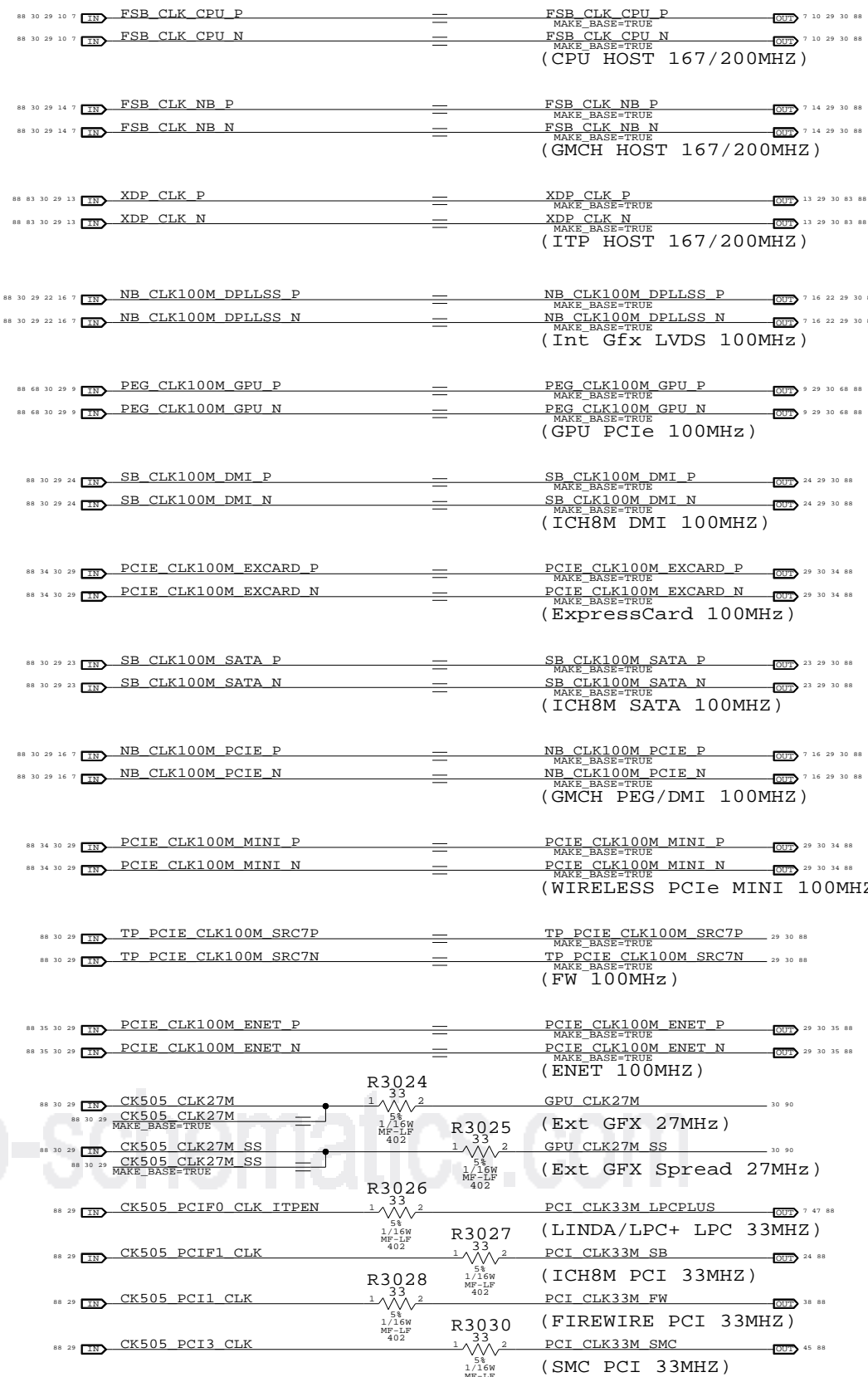
FS_A, FS_B, FS_C (Host clock freq select)



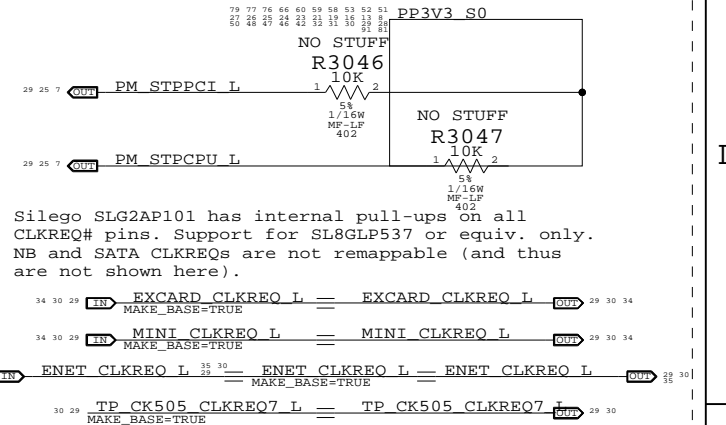
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

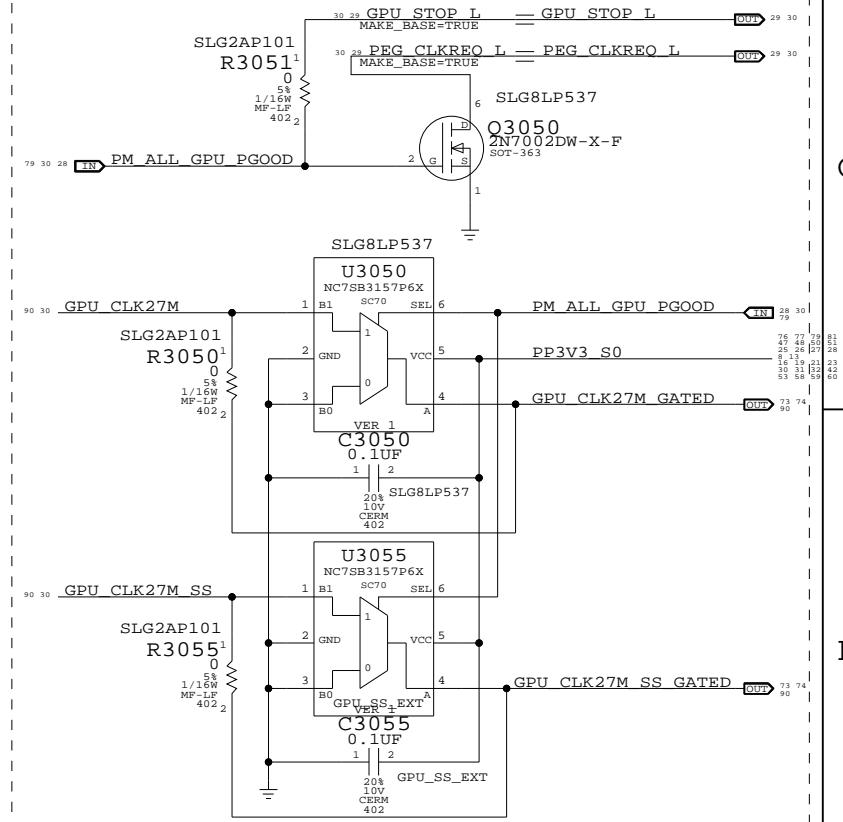
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)



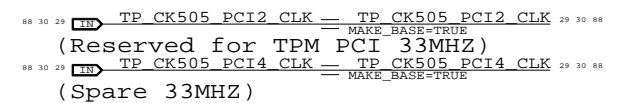
CLKREQ Controls



GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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SCALE	SHT	OF	92
NONE	30		

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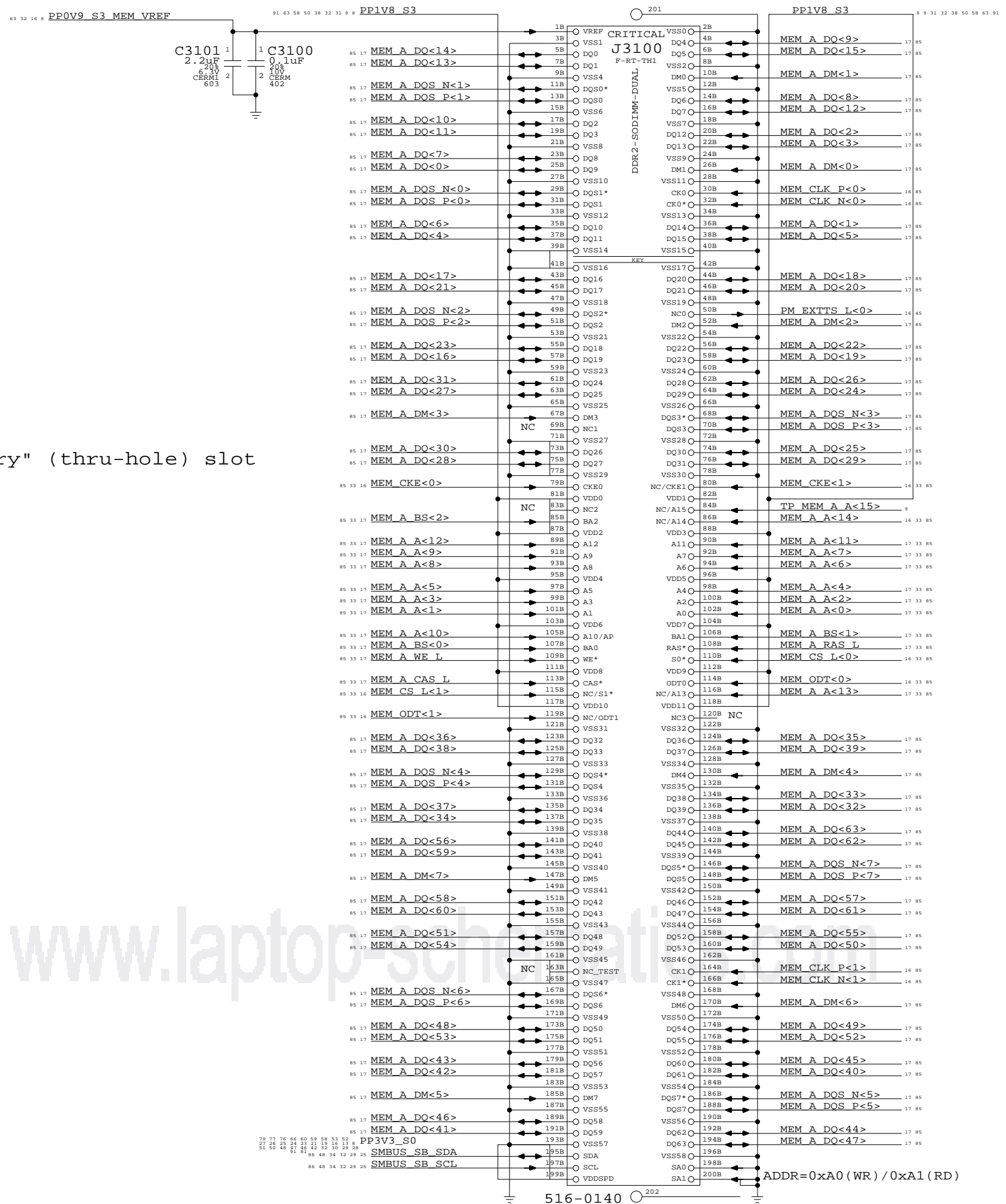
Page Notes

Power aliases required by this page:
 - =PP1V8_S3M_MEM_A
 - =PP0V9_S3M_MEM_DIMMVREFA
 - =PPSPD_S0M_MEM_A (2.5V - 3.3V)

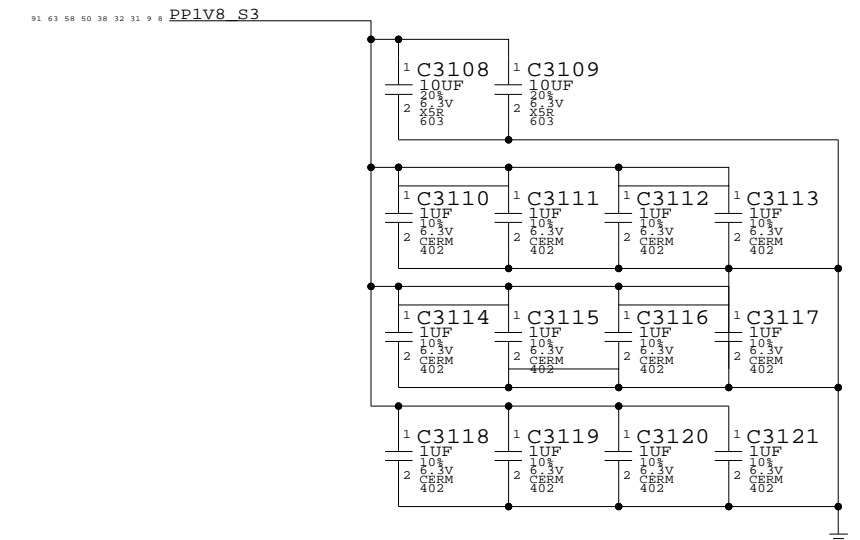
Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

"Factory" (thru-hole) slot



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector A
 SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	31	92	

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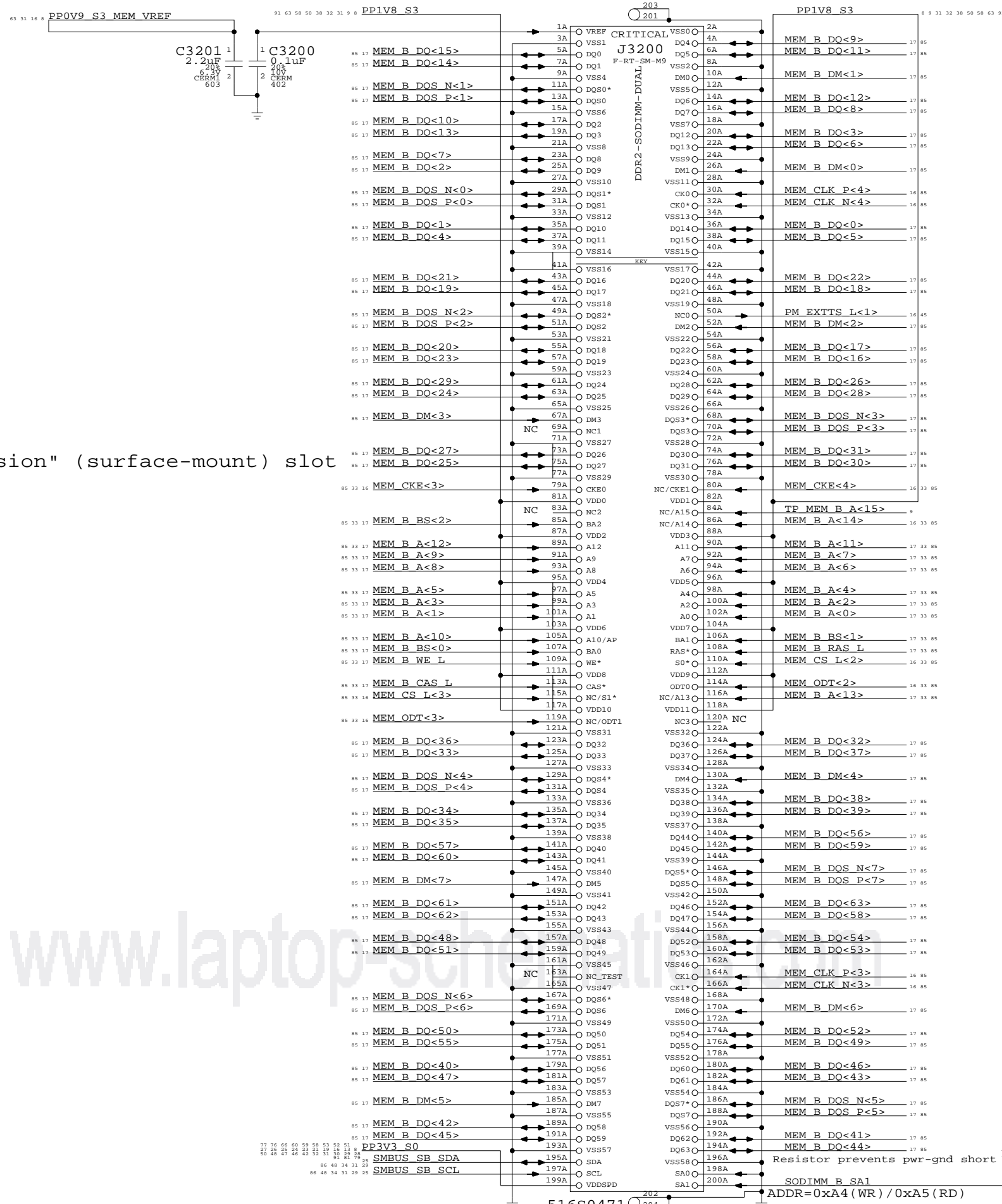
Page Notes

Power aliases required by this page:
 - =PP1V8_S3M_MEM_B
 - =PP0V9_S3M_MEM_DIMMVREFB
 - =PPSPD_S0M_MEM_B (2.5V - 3.3V)

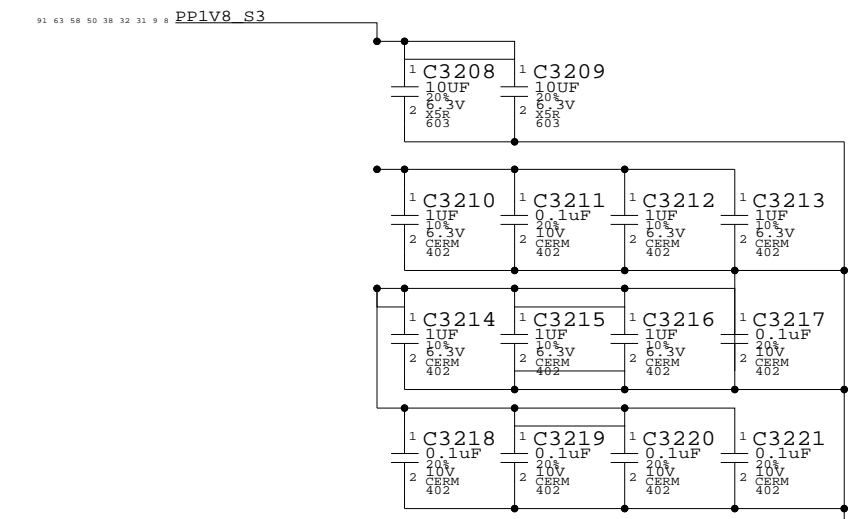
Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

BOM options provided by this page:
 (NONE)

"Expansion" (surface-mount) slot



DDR2 Bypass Caps (For return current)



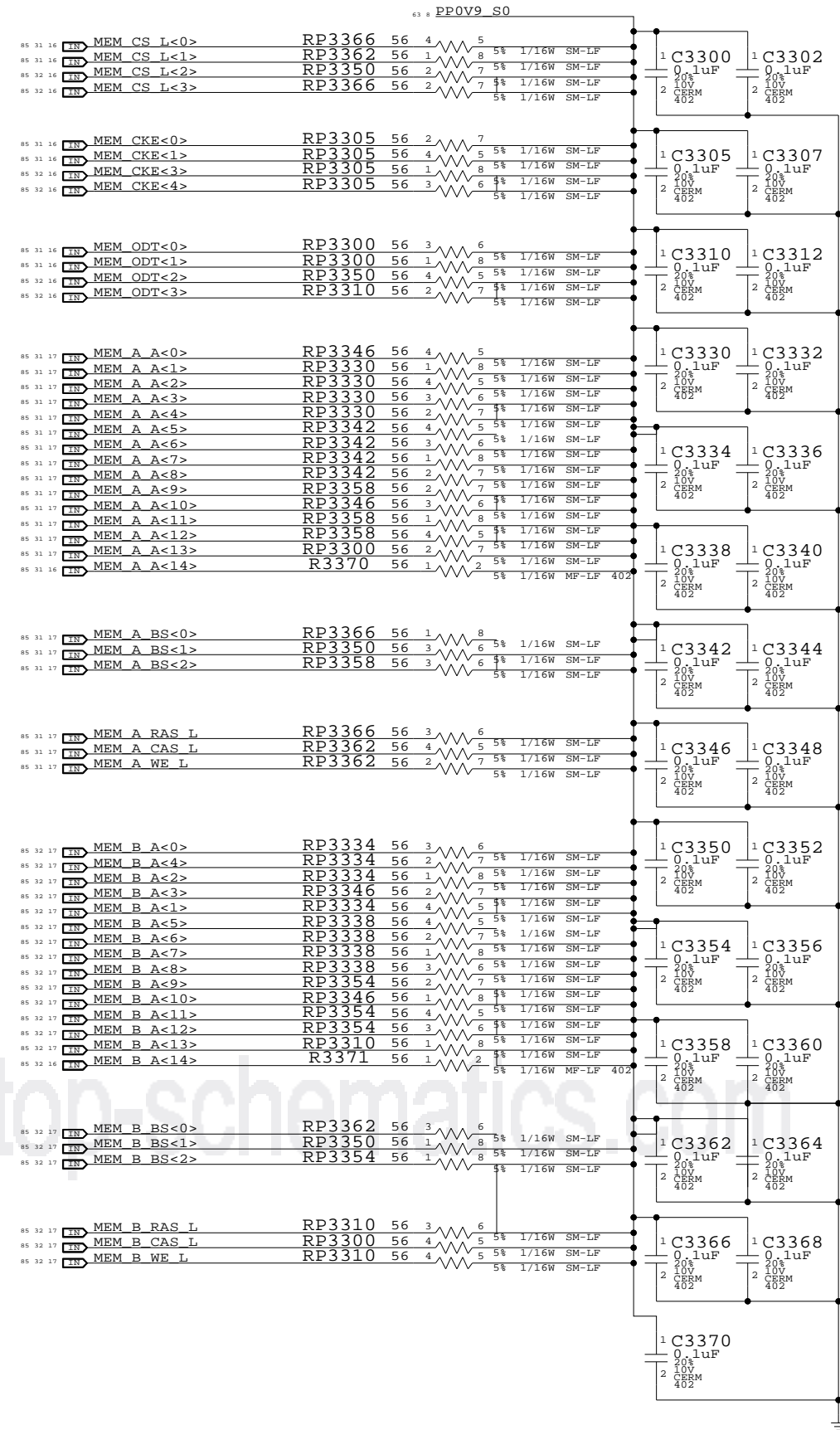
DDR2 SO-DIMM Connector B
 SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	32	92	

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One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector



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Memory Active Termination
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

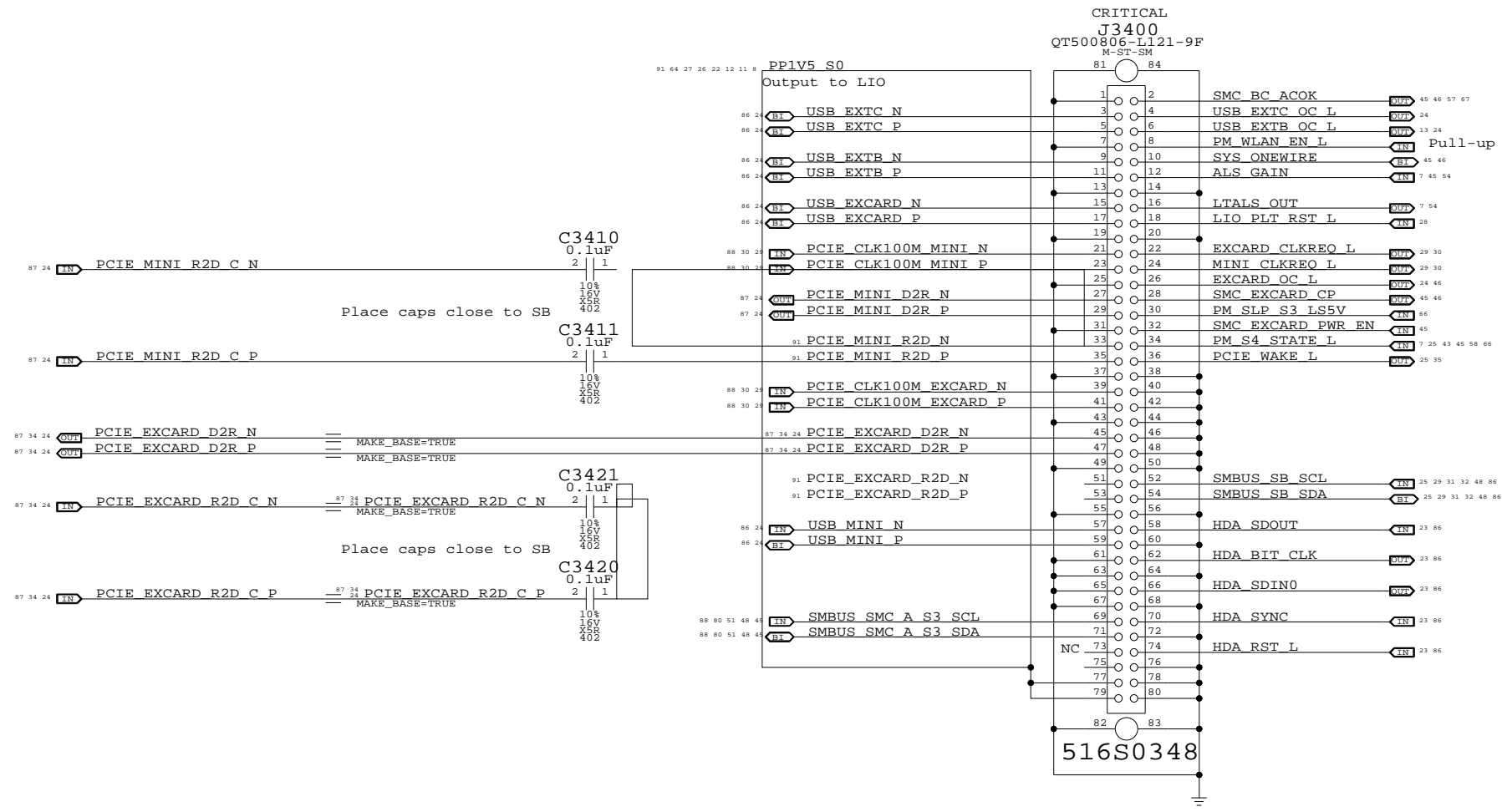
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SCALE	SHT	OF	
NONE	33	92	

Left I/O Board Connector



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Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	34		92

Page Notes

Power aliases required by this page:
 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY

Signal aliases required by this page:
 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBLE (See note by pin)

BOM options provided by this page:
 YUKON_EC - Selects Yukon EC RSET value.
 YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

62 50 # PP1V25_ENET

Yukon EC	Yukon Ultra
No link: 171 mA	No link: 130 mA
10 Mbps: 179 mA	10 Mbps: 130 mA
100 Mbps: 203 mA	100 Mbps: 150 mA
1000 Mbps: 426 mA	1000 Mbps: 290 mA

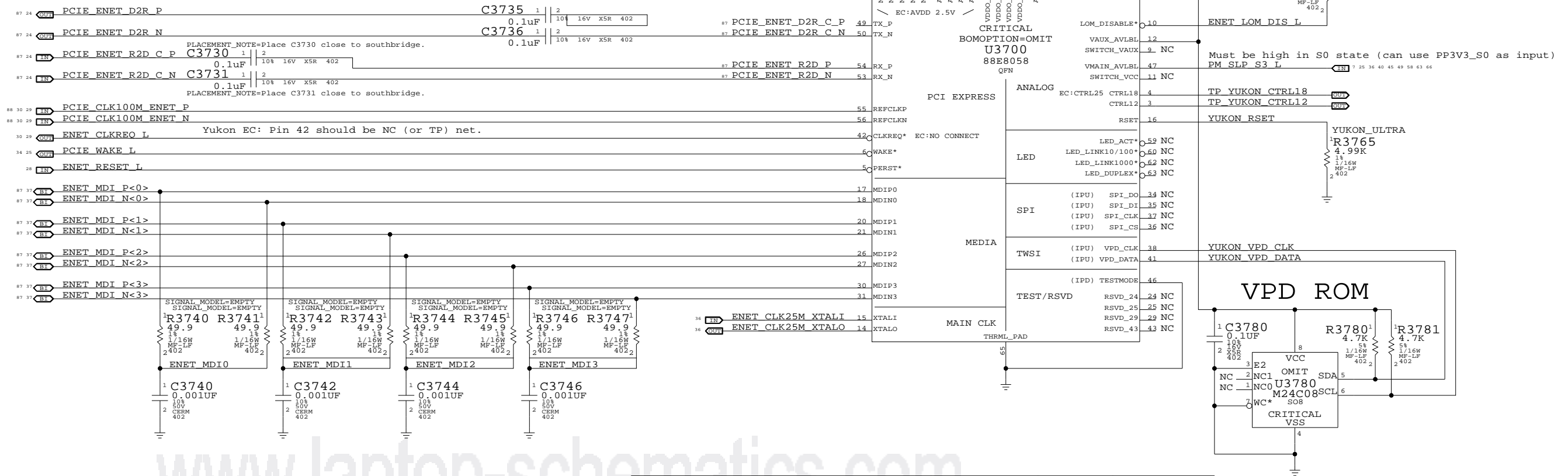
36 # PP3V3_ENET

Yukon EC	Yukon Ultra
No link: 4 mA	No link: 60 mA
10 Mbps: 4 mA	10 Mbps: 70 mA
100 Mbps: 4 mA	100 Mbps: 70 mA
1000 Mbps: 4 mA	1000 Mbps: 80 mA

36 # PP1V9_ENET

Yukon EC (2.5V)	Yukon Ultra (1.8V)
No link: 82 mA	No link: 0 mA
10 Mbps: 108 mA	10 Mbps: 30 mA
100 Mbps: 126 mA	100 Mbps: 40 mA
1000 Mbps: 218 mA	1000 Mbps: 150 mA

GND
 Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:
 - Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
 - Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
 - Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
 - Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

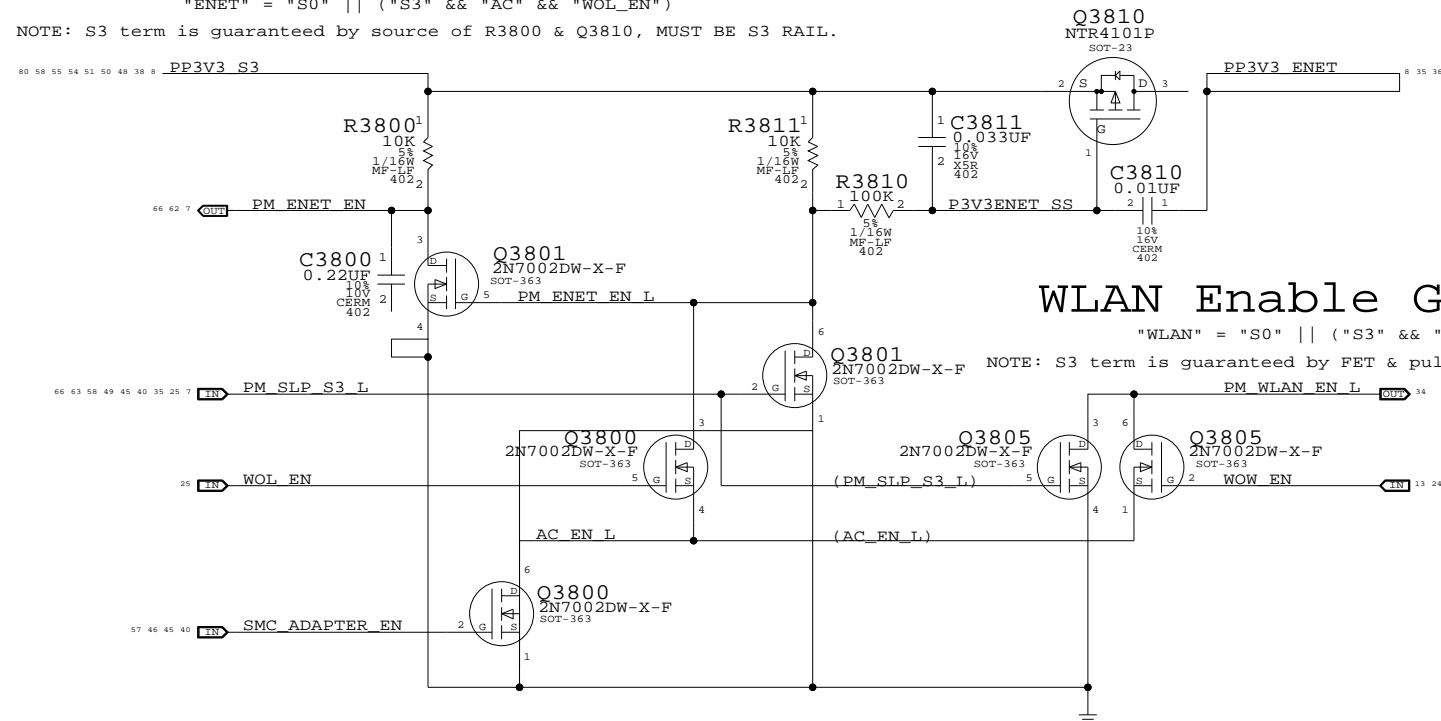
Ethernet (Yukon)
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007
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	D	051-7261	A.0.0
SCALE	SHT	OF	92
NONE		35	

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ENET Enable Generation

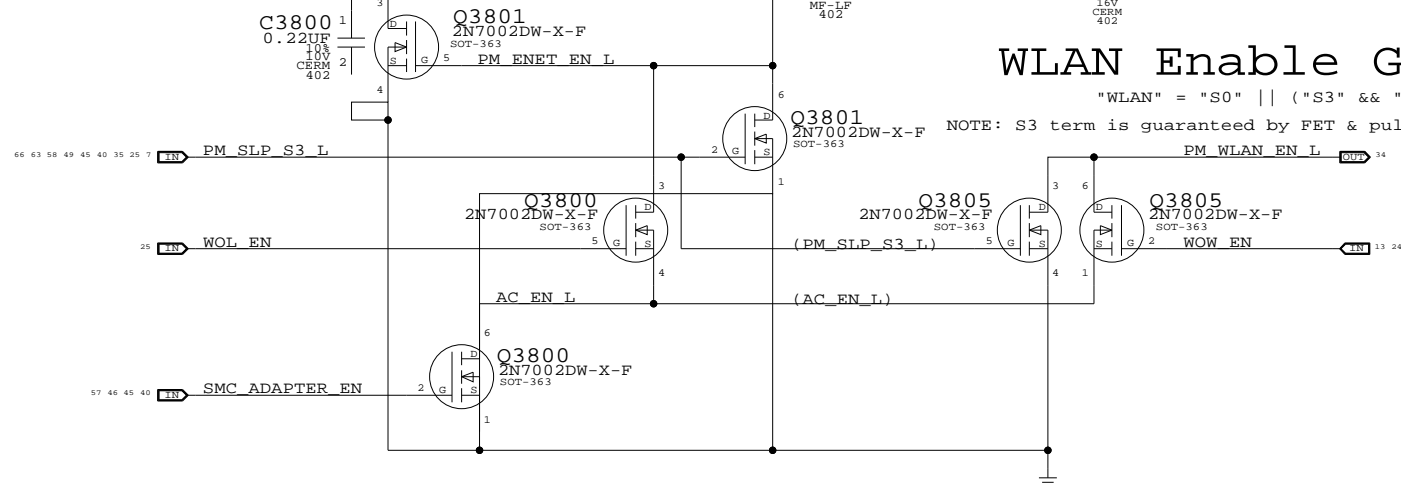
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

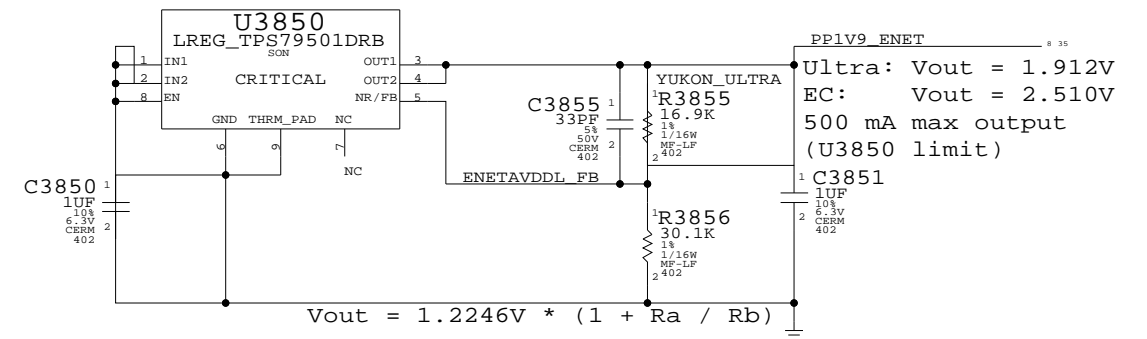
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOL_EN")
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



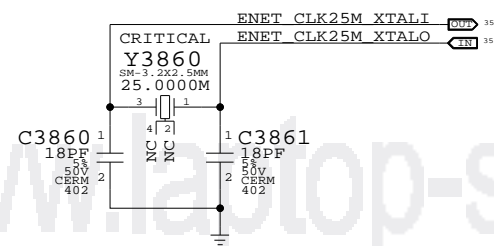
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/19/2007

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	D	051-7261	A.0.0
SCALE	SHT 36 OF 92		
NONE			

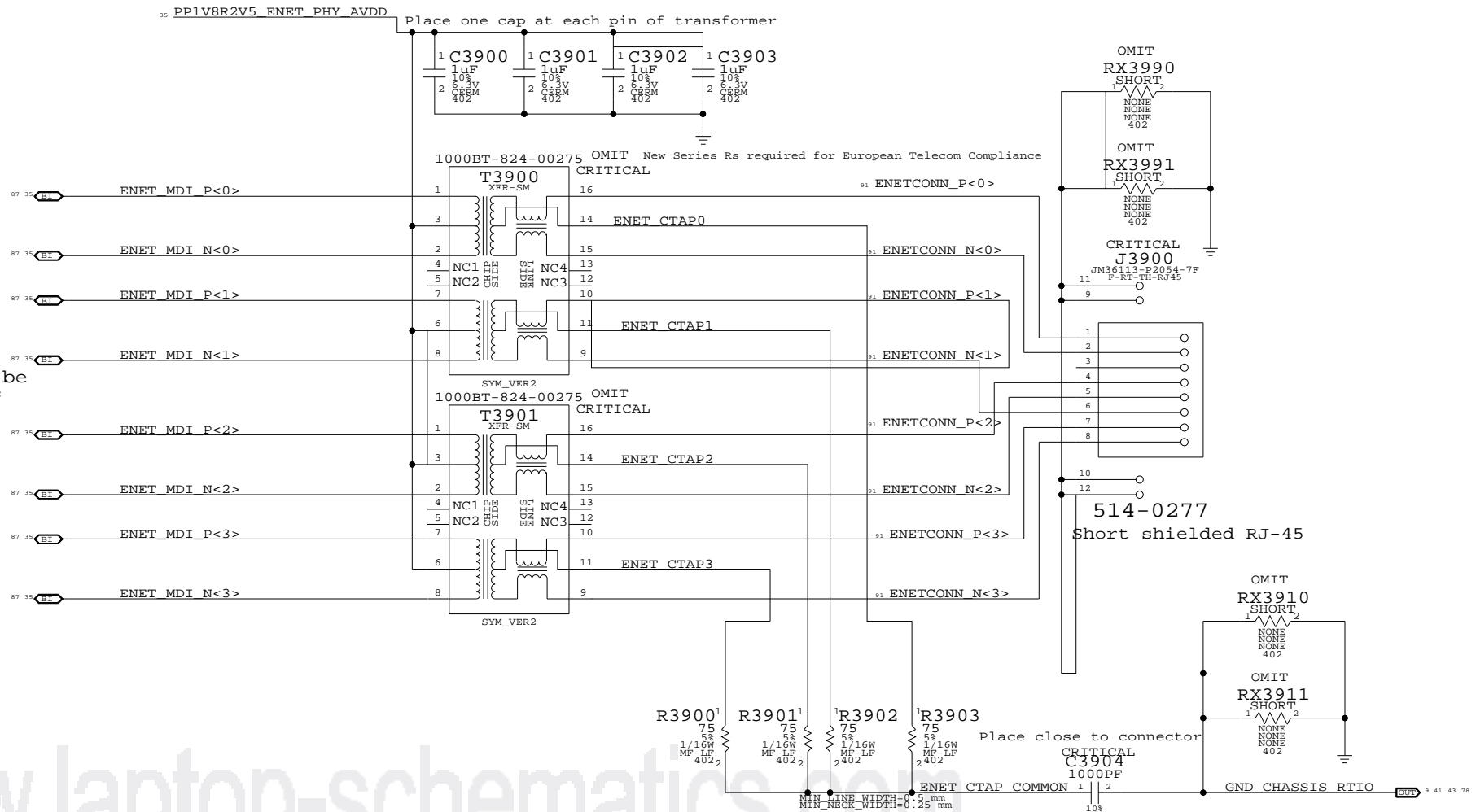
Page Notes

Power aliases required by this page:
 - =GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Transformers should be mirrored on opposite sides of the board



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15780030	2	XPR-SMD,HALF-PORT,100BT,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector
 SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

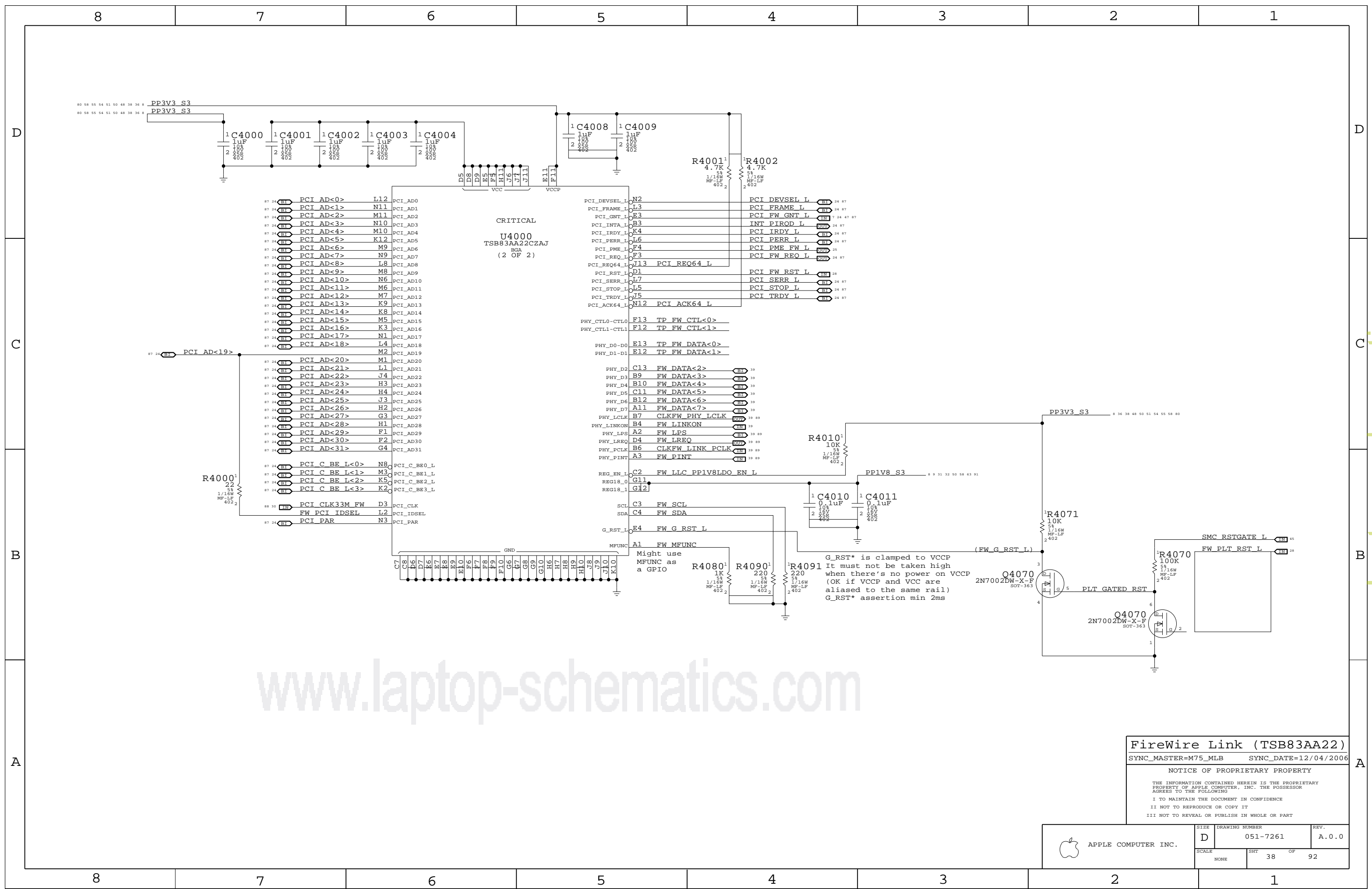
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	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	37	92	

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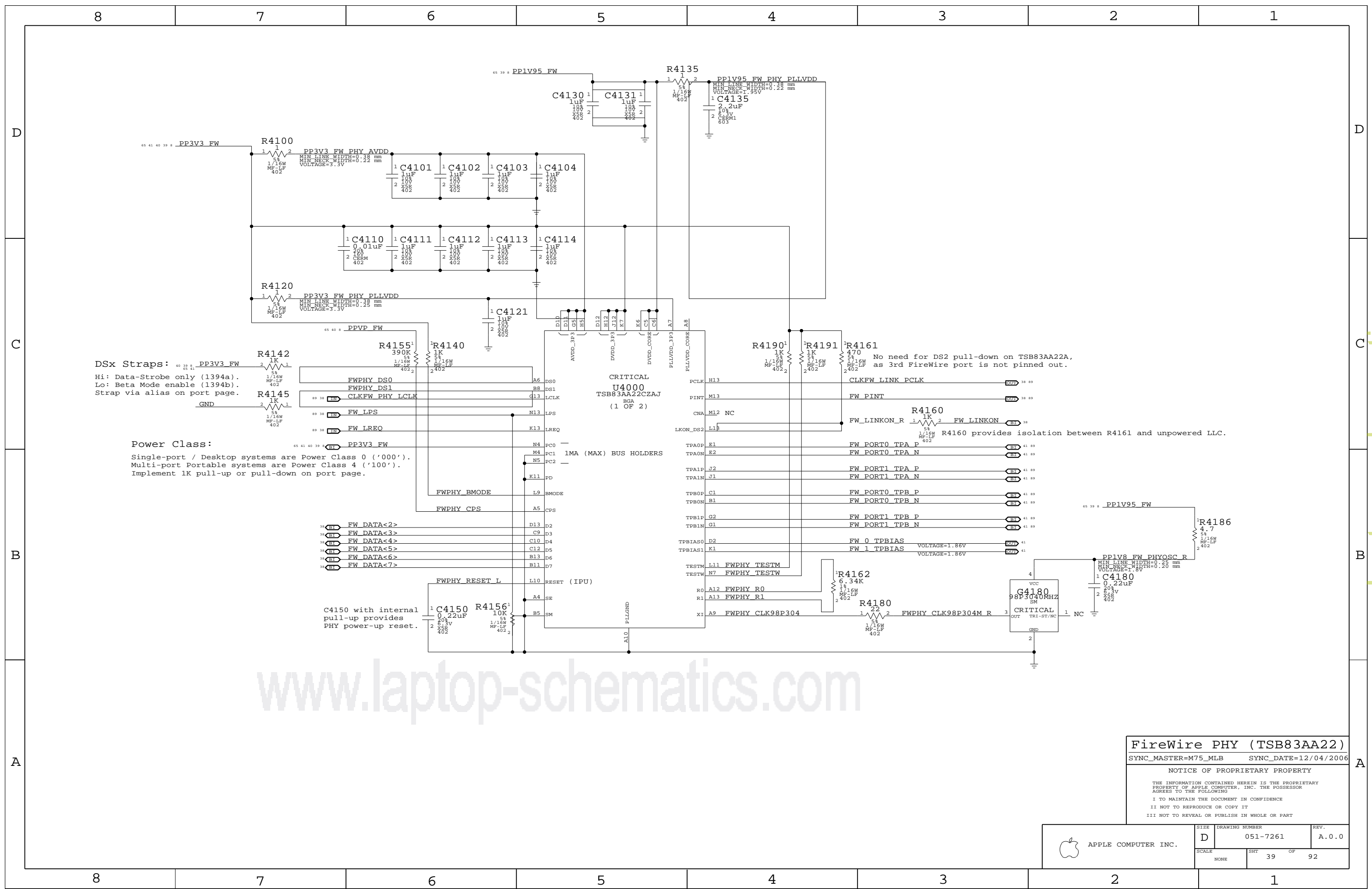
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FireWire Link (TSB83AA22)
 SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT 38 OF 92		
NONE			



8 7 6 5 4 3 2 1

D
C
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A

D
C
B
A

DSx Straps: 40 38 41 PP3V3 FW
 Hi: Data-Strobe only (1394a).
 Lo: Beta Mode enable (1394b).
 Strap via alias on port page.

Power Class:
 Single-port / Desktop systems are Power Class 0 ('000').
 Multi-port Portable systems are Power Class 4 ('100').
 Implement 1K pull-up or pull-down on port page.

No need for DS2 pull-down on TSB83AA22A, as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

C4150 with internal pull-up provides PHY power-up reset.

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FireWire PHY (TSB83AA22)
 SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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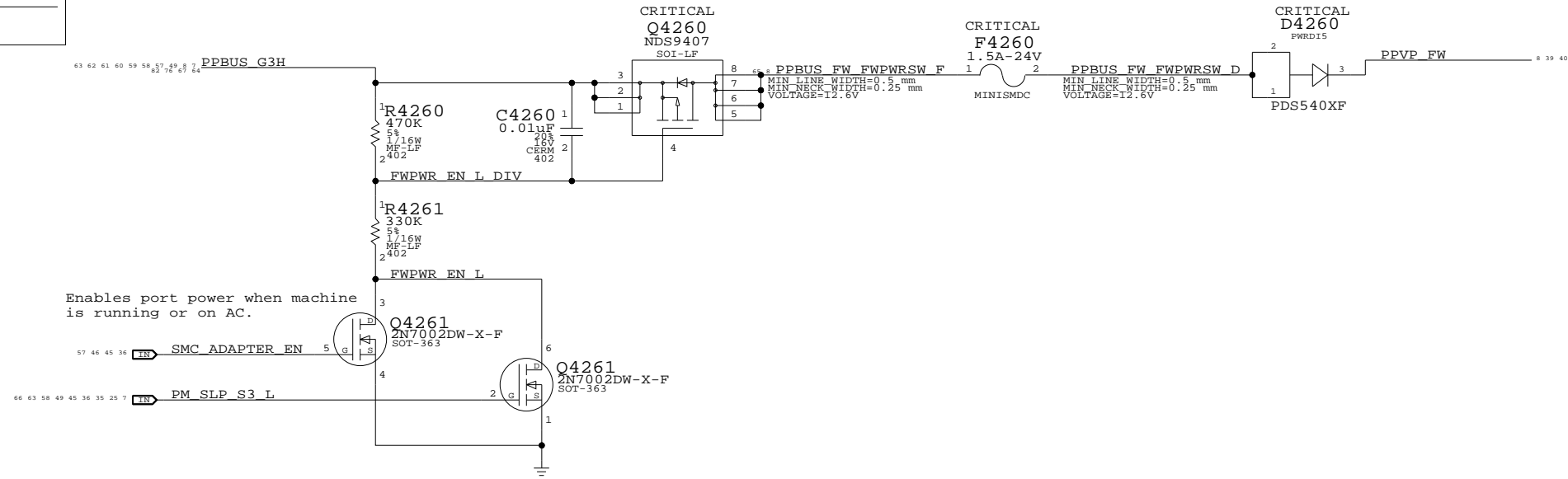
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT 39 OF 92		
NONE			

8 7 6 5 4 3 2 1

Page Notes

- Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)
- Signal aliases required by this page:
(NONE)
- BOM options provided by this page:
- FW_PORT_FAULT_PU

FireWire Port Power Switch

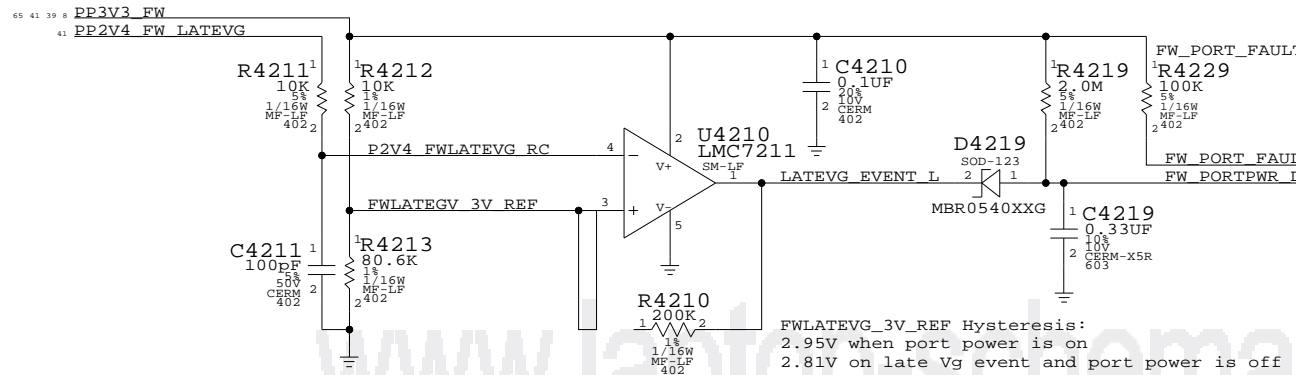


Enables port power when machine is running or on AC.

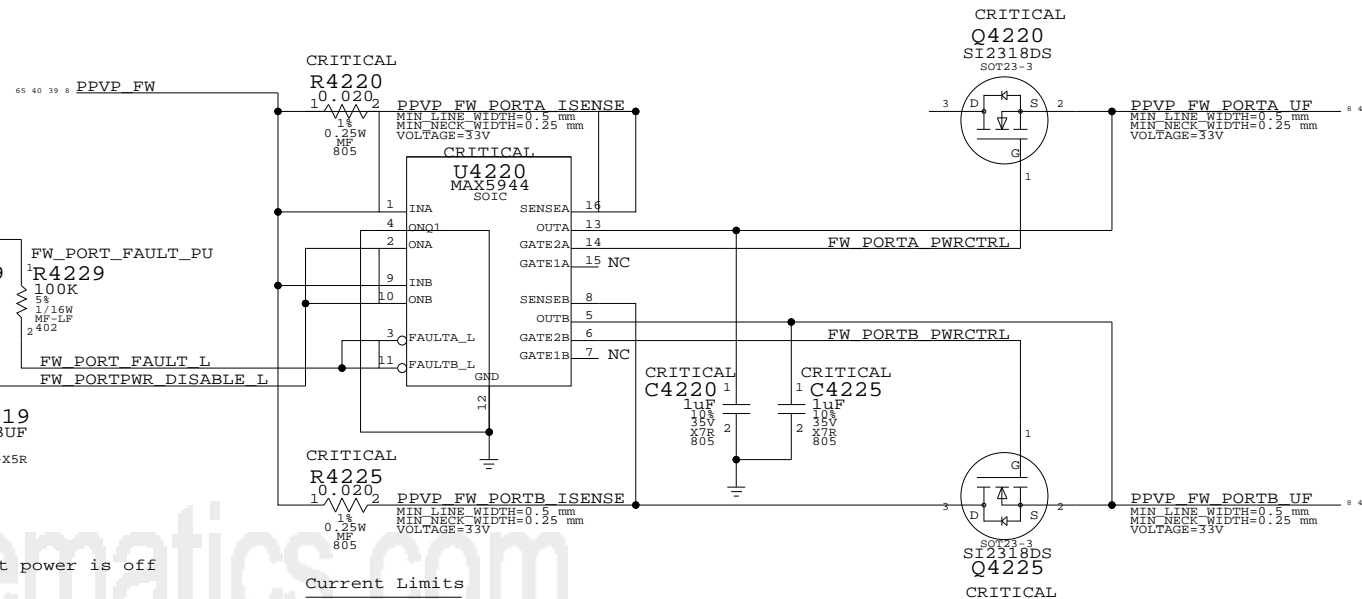
Current Limit/Active Late-VG Protection

R4220 & R4225 PADS SHOULD BE ROUTED DIRECTLY TO MAX5944 SENSEA & SENSEB PINS RESPECTIVELY. SENSEA & SENSEB PINS SHOULD NOT BE PART OF THE MAIN CURRENT PATH

Late-VG Event Detection



FWLATEVG_3V_REF Hysteresis:
2.95V when port power is on
2.81V on late Vg event and port power is off



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M75_MLB SYNC_DATE=03/07/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	40	92	

Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT0
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG
 - =GND_CHASSIS_FW_PORT0L
 - =GND_CHASSIS_FW_PORT0U
 - =GND_CHASSIS_FW_PORT1
 - =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
 (NONE)

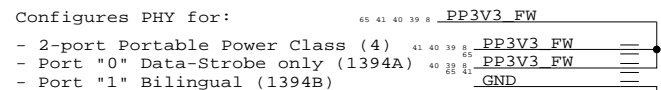
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

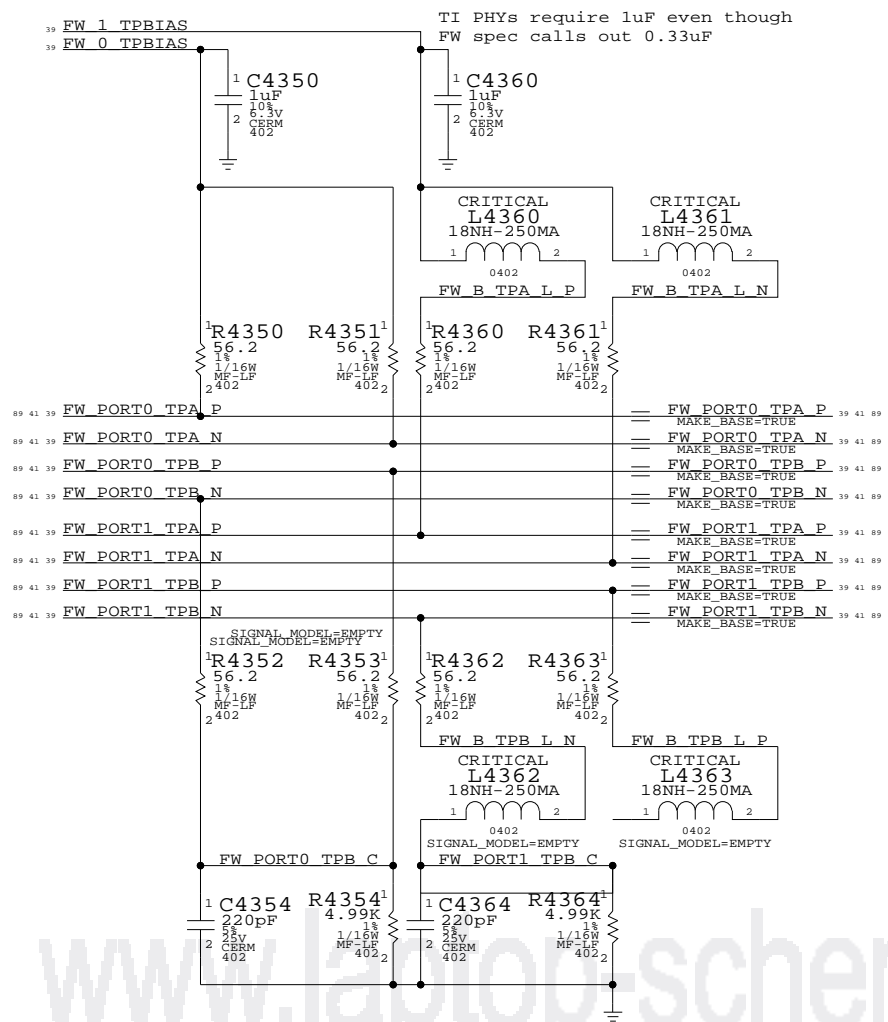
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

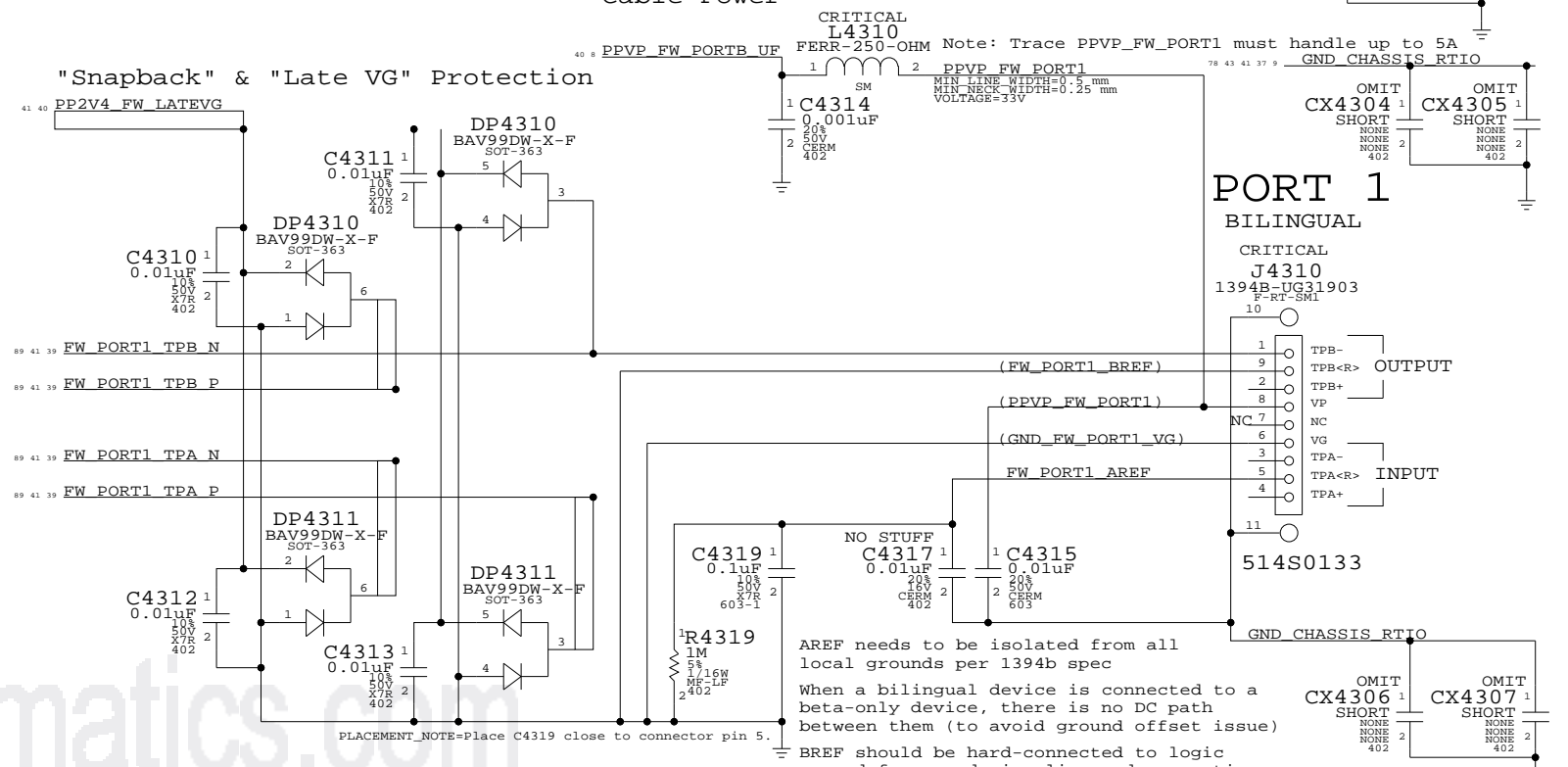
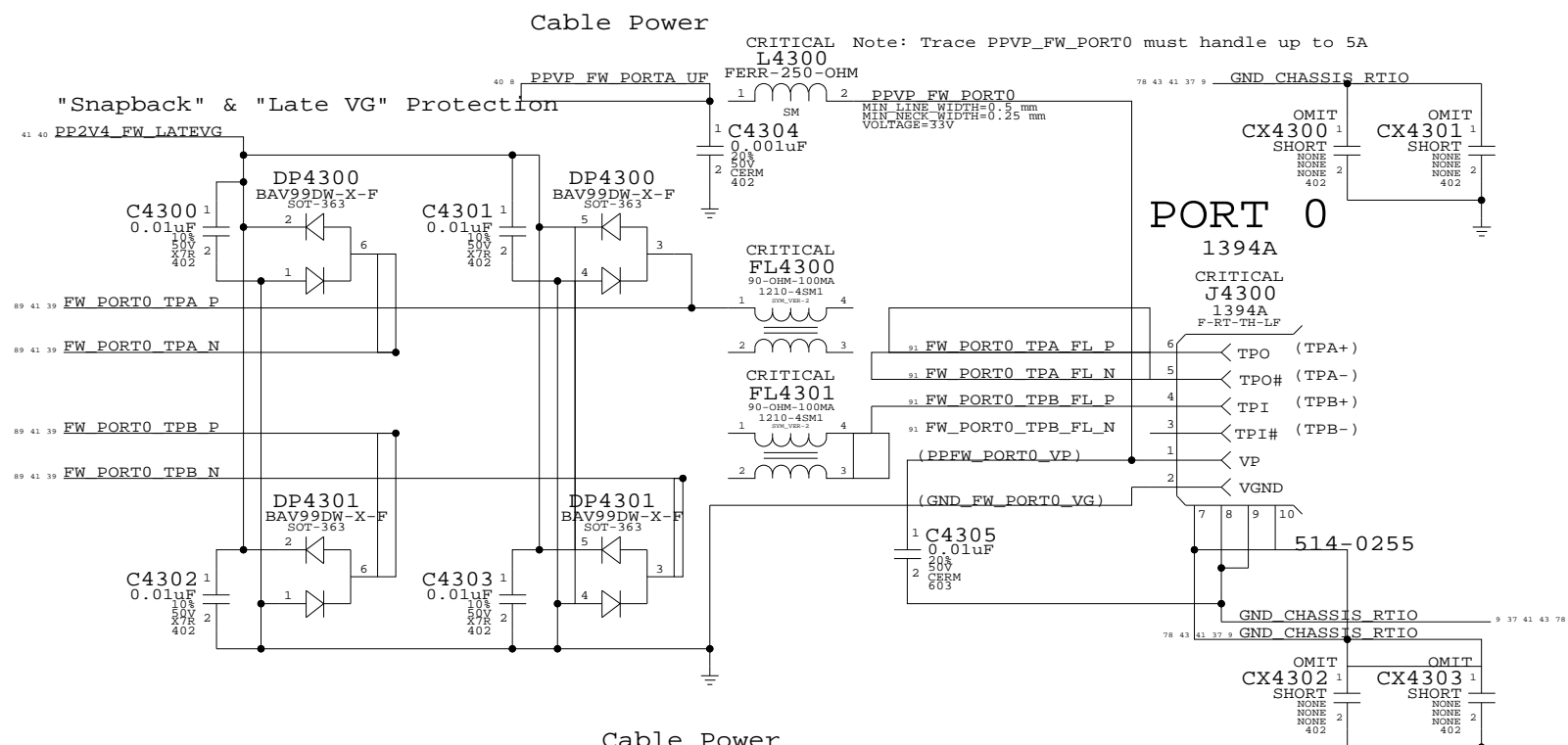
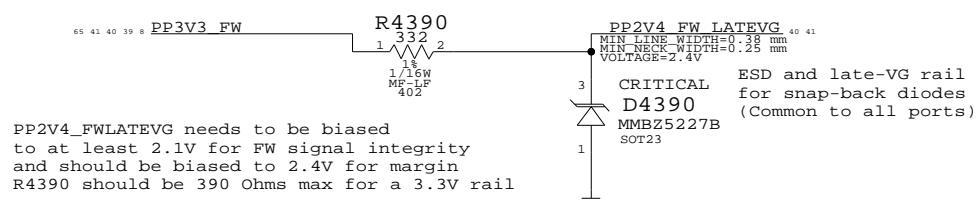


Termination

Place close to FireWire PHY



Late-VG Protection Power



FireWire Ports

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

NOTICE OF PROPRIETARY PROPERTY

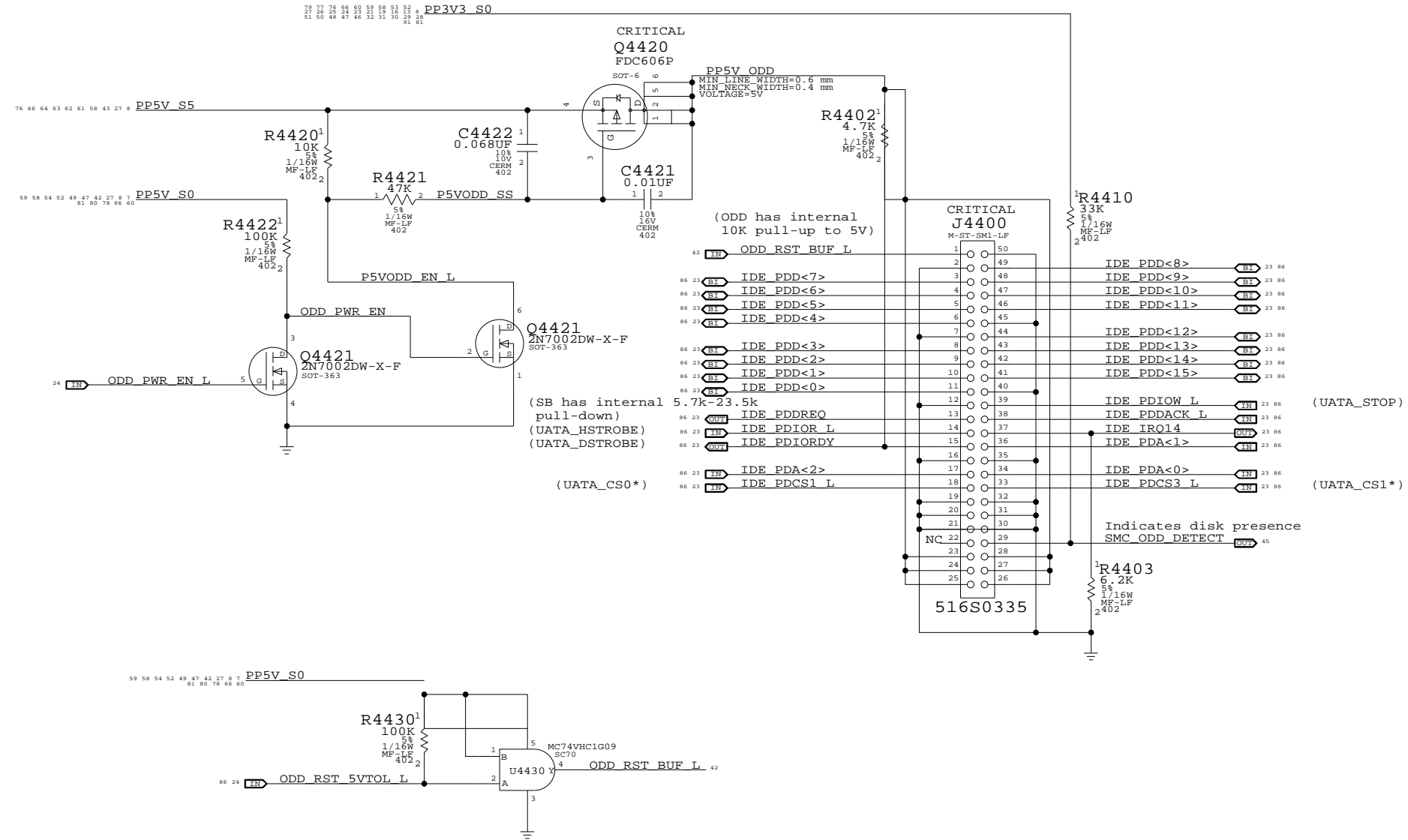
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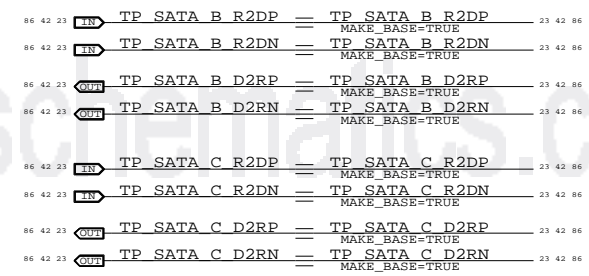
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	41	92	

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IDE (ODD) Connector



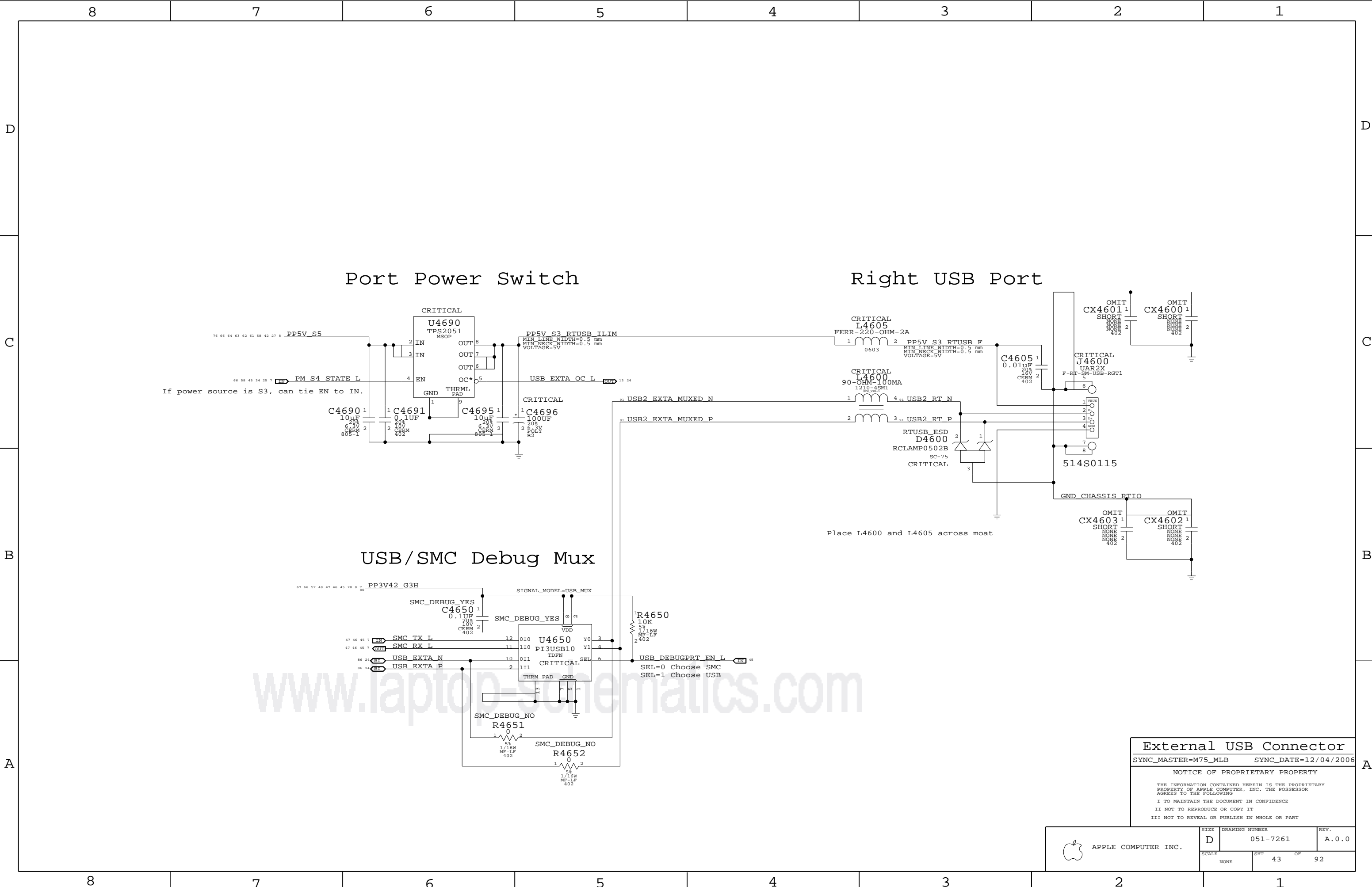
Unused SATA Ports



Placement note:
Place within 12.7mm
from ball of SB

PATA Connector
 SYNC_MASTER=M75_MLB SYNC_DATE=12/07/2006
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	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	42		92



Port Power Switch

Right USB Port

USB/SMC Debug Mux

Place L4600 and L4605 across moat

External USB Connector

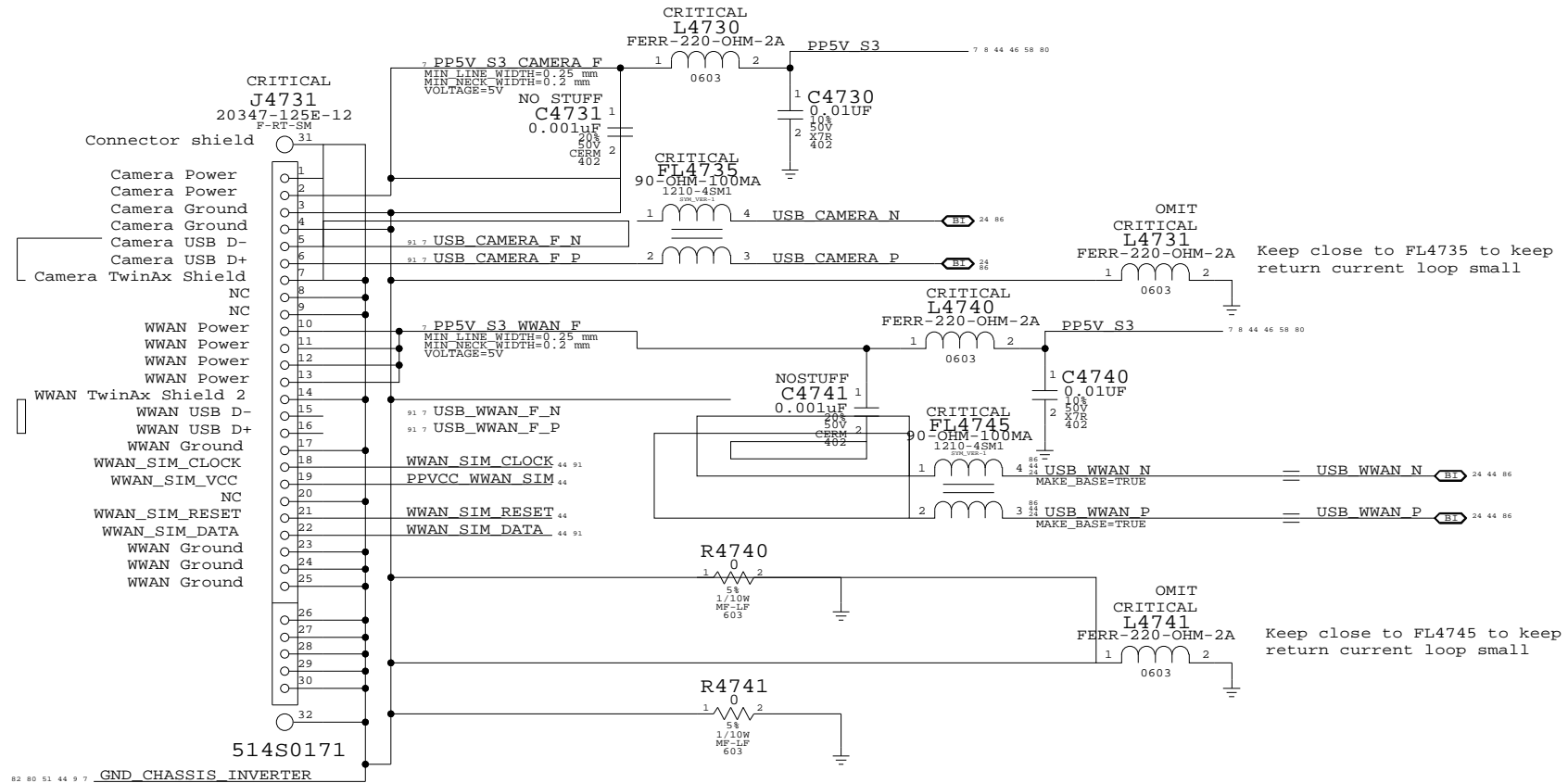
SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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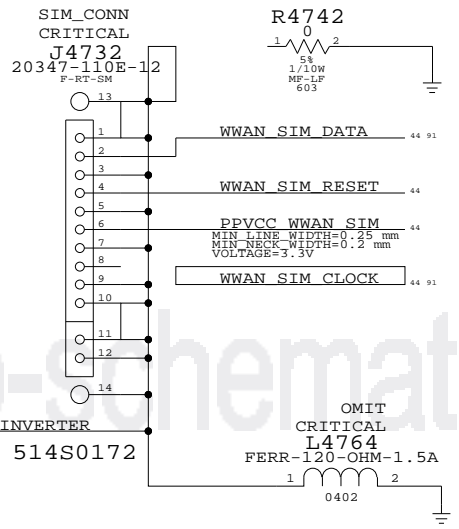
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	43		92

Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES, MF, 1/10W, 0OHM, 5, 0603, SM, LF	L4731, L4741	CRITICAL	
116S0004	1	RES, MF, 1/16W, 0OHM, 5, 0402, SM, LF	L4764	CRITICAL	

SIM Interconnect



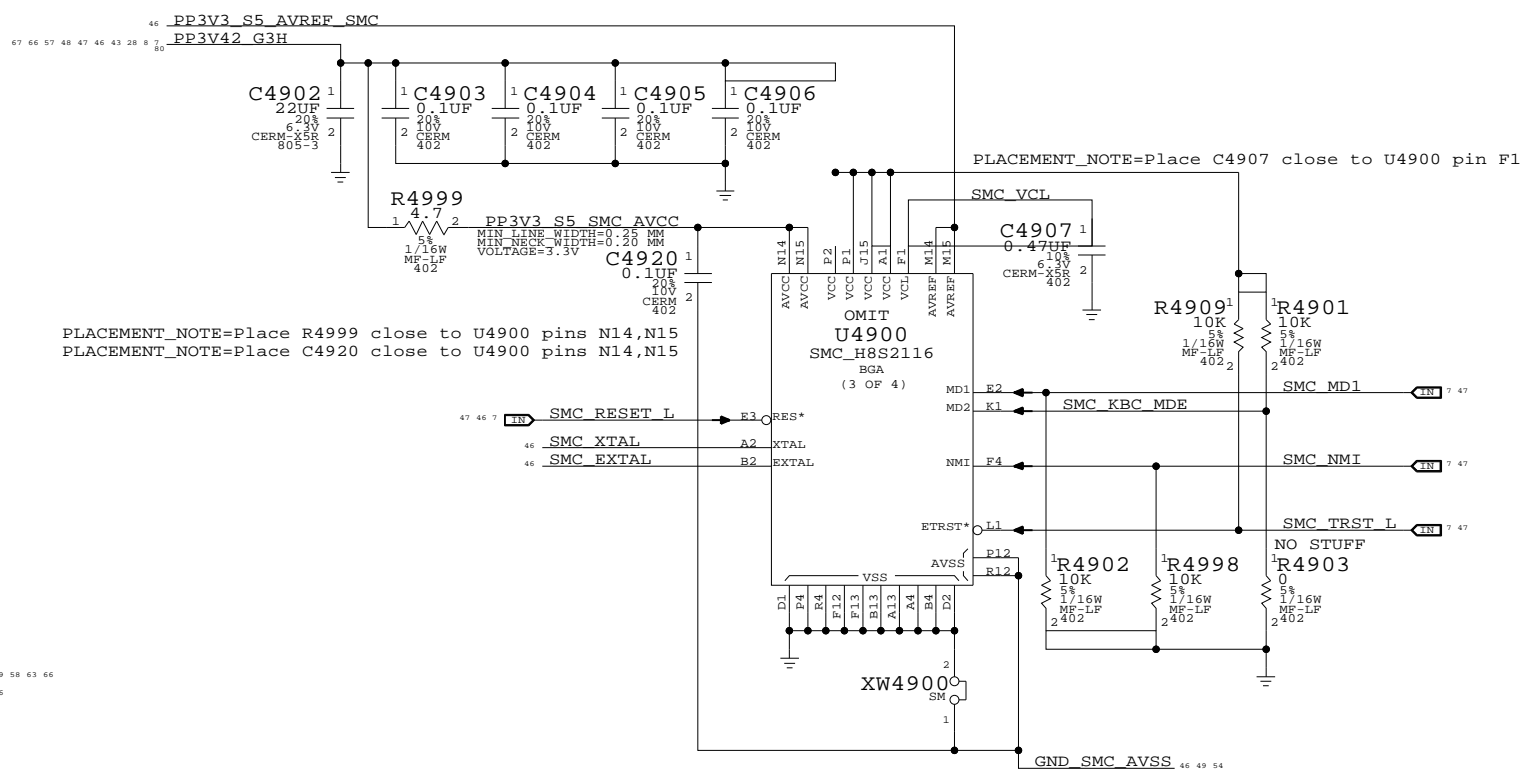
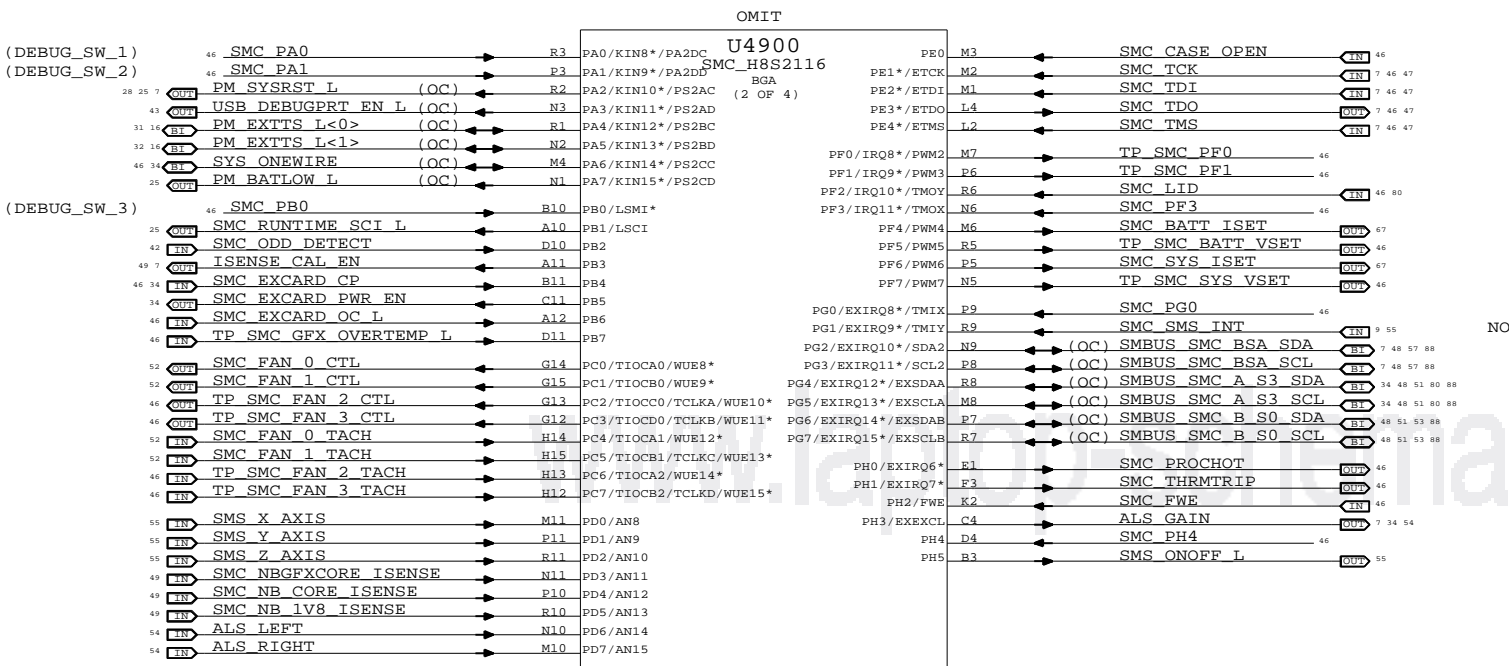
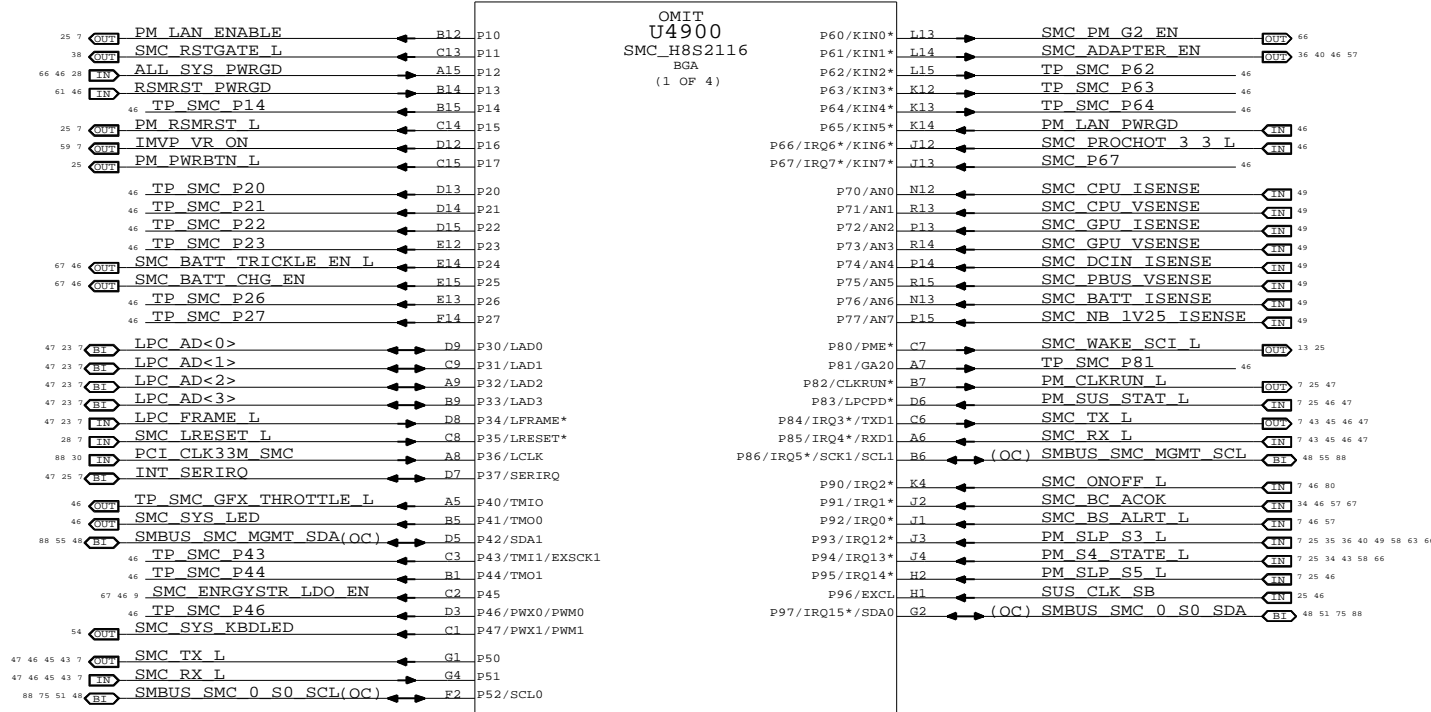
Left Clutch Barrel Interconnect
 SYNC_MASTER=M75_MLB SYNC_DATE=12/21/2006

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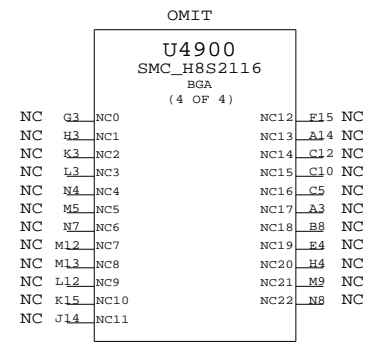
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	44	92	

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



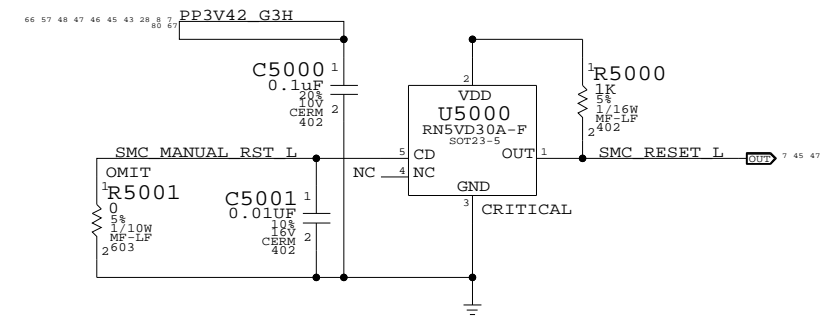
NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



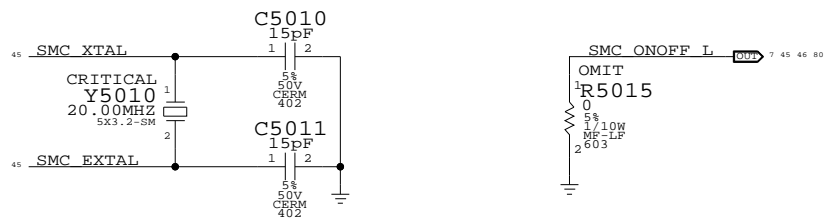
SMC
SYNC_MASTER=T9_NOME SYNC_DATE=12/21/2006
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APPLE COMPUTER INC.
DRAWING NUMBER: 051-7261
SCALE: NONE
SHEET: 45 OF 92
REV: A.0.0

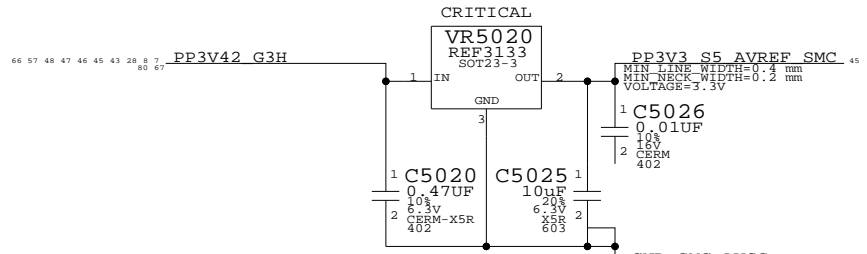
SMC Reset "Button" / Brownout Detect



SMC Crystal Circuit Debug Power "Button"

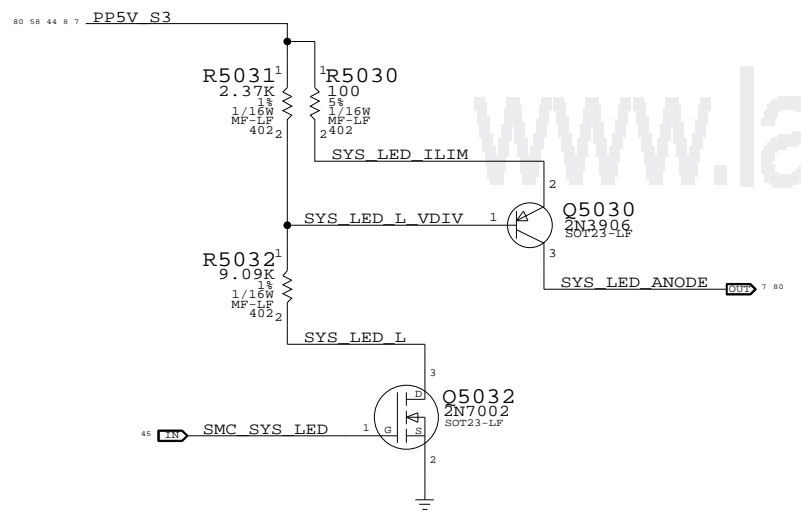


SMC AVREF Supply



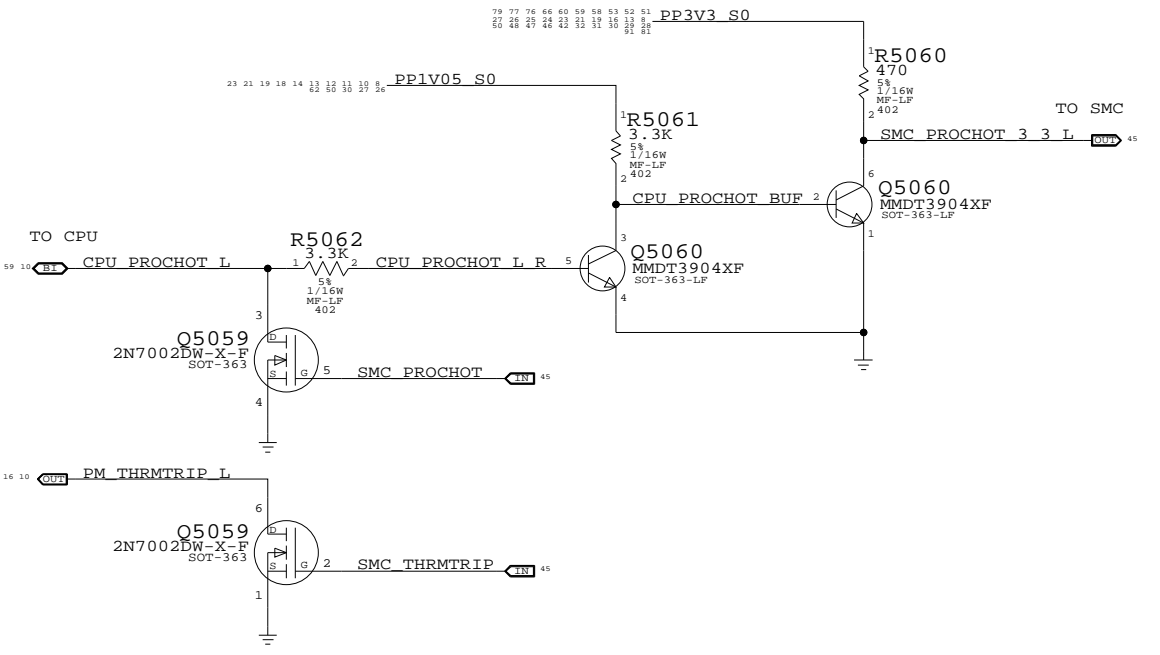
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interail ISL60002-33

System (Sleep) LED Circuit



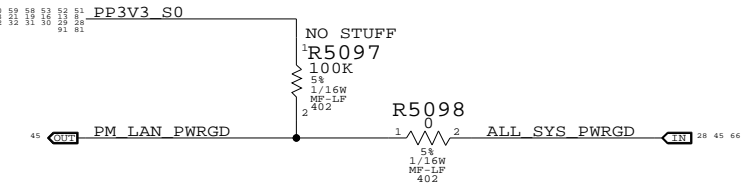
- TP_SMC_FAN_2_CTL == TP_SMC_FAN_2_CTL
- TP_SMC_FAN_2_TACH == TP_SMC_FAN_2_TACH
- TP_SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL
- TP_SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH
- TP_SMC_GFX_OVERTEMP_L == TP_SMC_GFX_OVERTEMP_L
- TP_SMC_GFX_THROTTLE_L == TP_SMC_GFX_THROTTLE_L
- TP_SMC_BATT_VSET == TP_SMC_BATT_VSET
- TP_SMC_SYS_VSET == TP_SMC_SYS_VSET
- TP_SMC_P14 == TP_SMC_P14
- TP_SMC_P20 == TP_SMC_P20
- TP_SMC_P21 == TP_SMC_P21
- TP_SMC_P22 == TP_SMC_P22
- TP_SMC_P23 == TP_SMC_P23
- TP_SMC_P26 == TP_SMC_P26
- TP_SMC_P27 == TP_SMC_P27
- TP_SMC_P43 == TP_SMC_P43
- TP_SMC_P44 == TP_SMC_P44
- TP_SMC_P46 == TP_SMC_P46
- TP_SMC_P62 == TP_SMC_P62
- TP_SMC_P63 == TP_SMC_P63
- TP_SMC_P64 == TP_SMC_P64
- TP_SMC_P81 == TP_SMC_P81
- TP_SMC_PFO == TP_SMC_PFO
- TP_SMC_PF1 == TP_SMC_PF1

SMC FSB to 3.3V Level Shifting

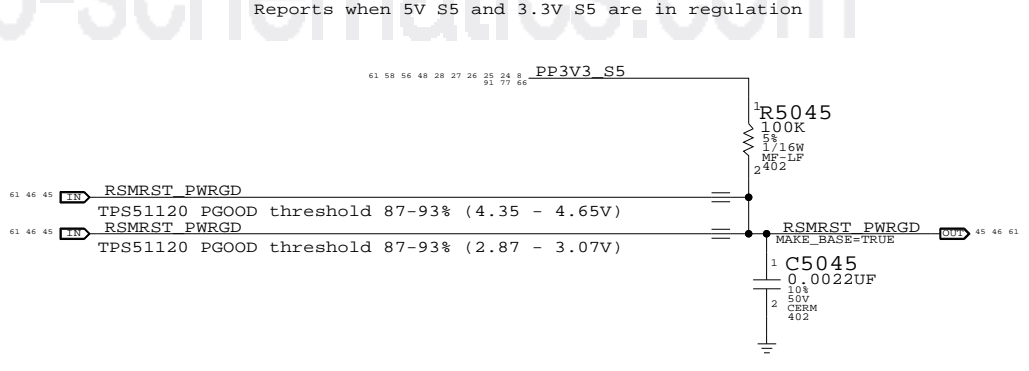


- SMC_EXCARD_OC_L == EXCARD_OC_L
- SUS_CLK_SB == SUS_CLK_SB
- SMC_ENRGYSTR_LDO_EN == SMC_ENRGYSTR_LDO_EN

LAN PWRGD Circuit



S5 Rail PWRGD Circuit

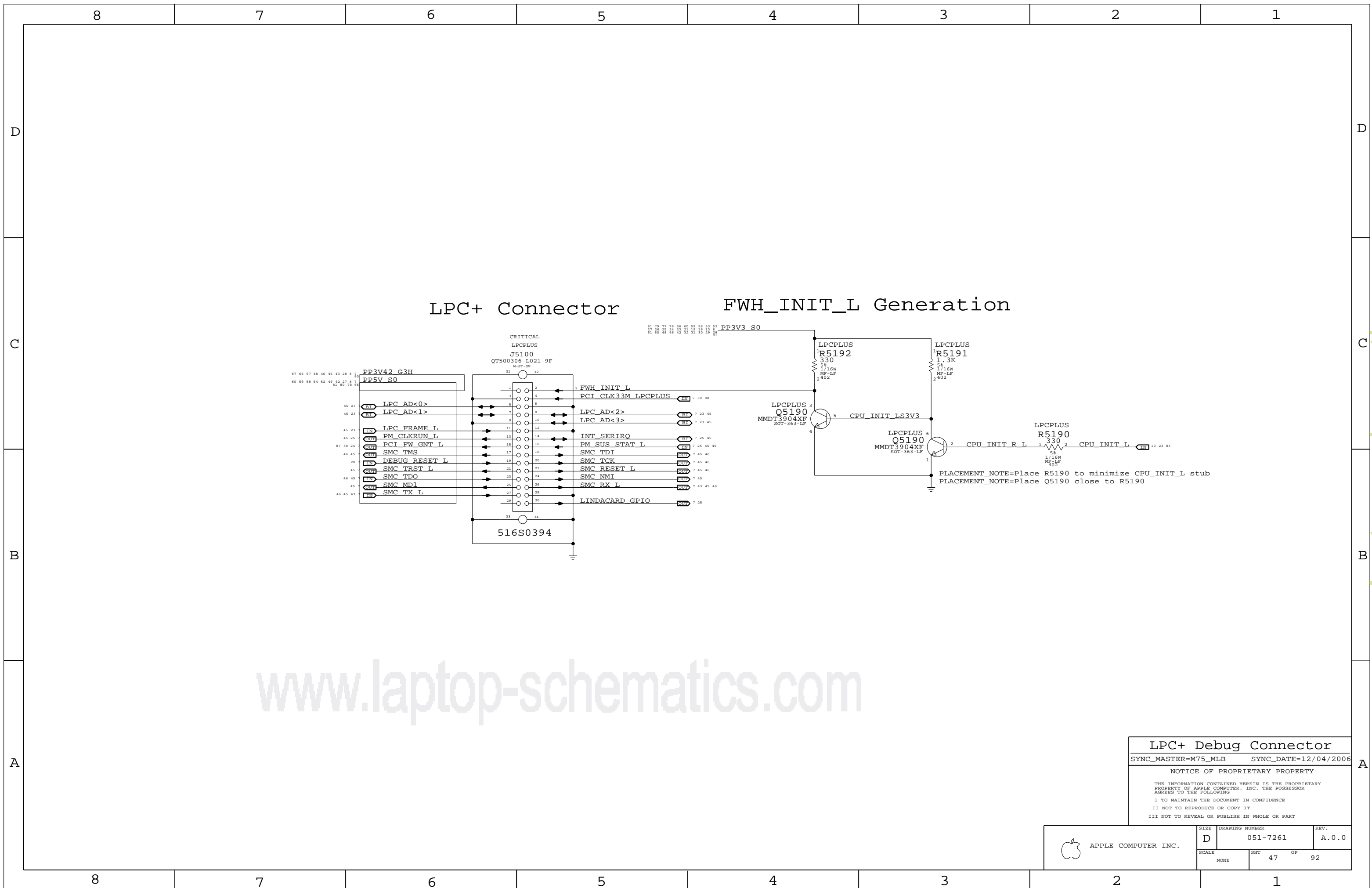


- SMC_PA0 == R5091 100K
- SMC_PA1 == R5092 100K
- SMC_PB0 == R5093 100K
- SMC_ONOFF_L == R5070 10K
- SMC_LID == R5071 100K
- SMC_FWE == R5072 10K
- SMC_TX_L == R5073 10K
- SMC_RX_L == R5074 100K
- SMC_BS_ALRT_L == R5076 100K
- SMC_TMS == R5077 10K
- SMC_TDO == R5078 10K
- SMC_TDI == R5079 10K
- SMC_TCK == R5080 10K
- SMC_P67 == R5094 10K
- SMC_P63 == R5081 10K
- SMC_P60 == R5096 10K
- SMC_PH4 == R5082 10K
- SMC_BATT_TRICKLE_EN_L == R5083 10K
- SMC_BATT_CHG_EN == R5084 10K
- SMC_ADAPTER_EN == R5085 10K
- SMC_CASE_OPEN == R5086 10K
- SMC_BC_ACOK == R5087 470K
- SMC_EXCARD_CP == R5088 10K
- PM_SUS_STAT_L == R5089 100K
- PM_SLP_S5_L == R5090 100K

SMC Support
 SYNC_MASTER=M75_MLB SYNC_DATE=04/25/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	46	92	

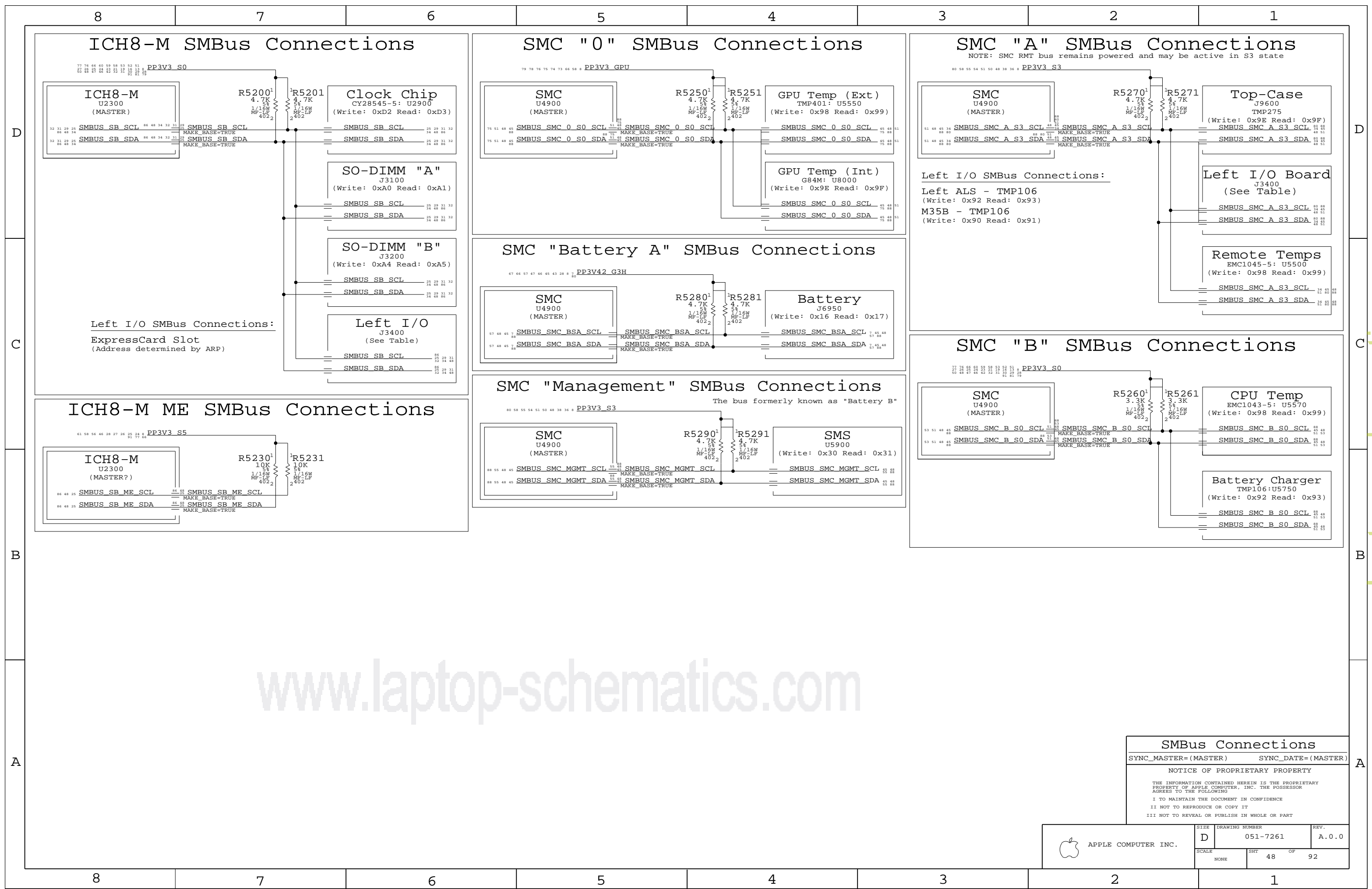


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LPC+ Debug Connector
 SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006
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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	47	92	



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SMBus Connections
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. A.0.0
	SCALE NONE	SHEET 48	OF 92

A

A

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B

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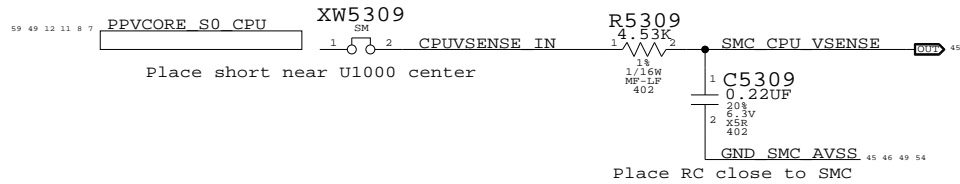
4

3

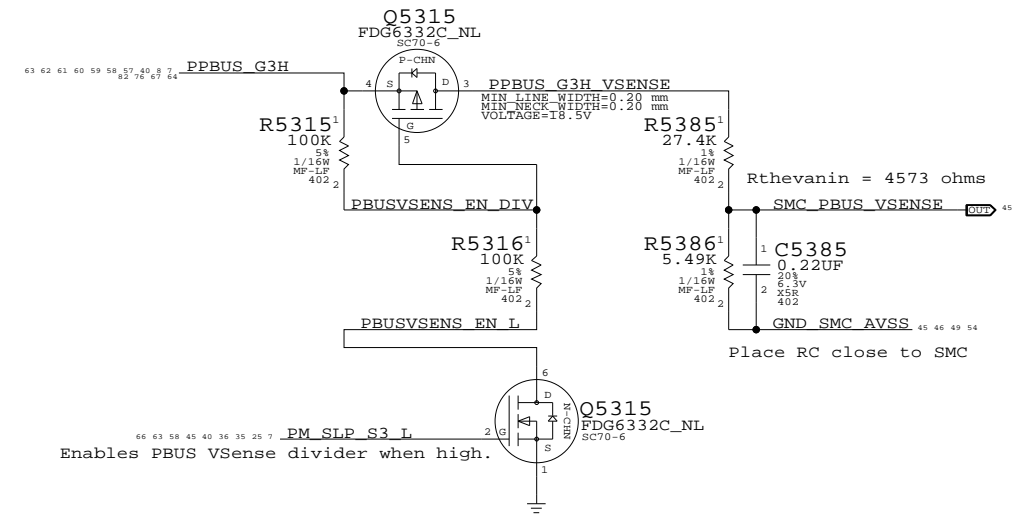
2

1

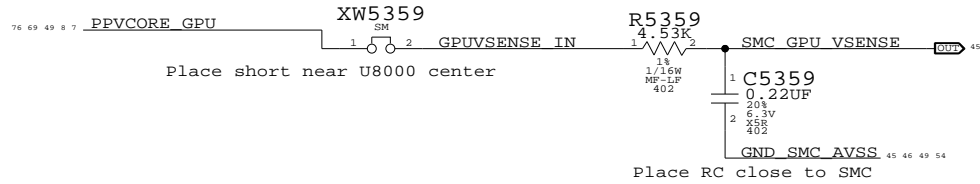
CPU Voltage Sense / Filter



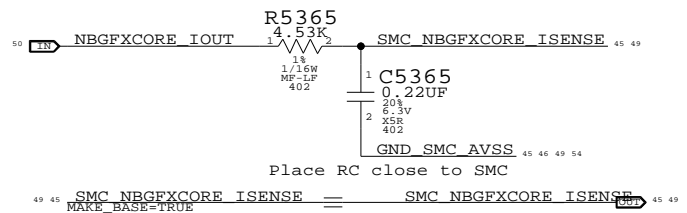
PBUS Voltage Sense & Filter



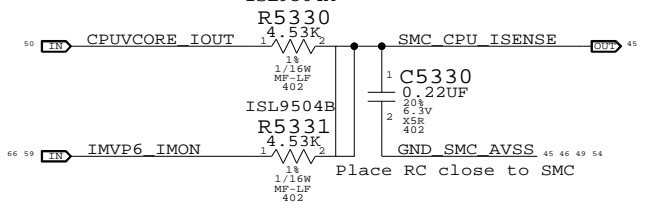
GPU Voltage Sense / Filter



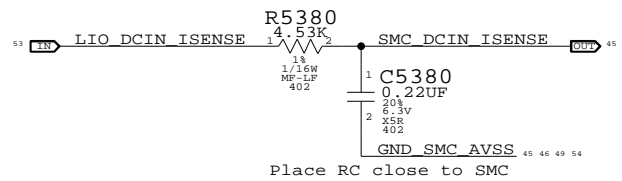
NB GFX Current Sense Filter



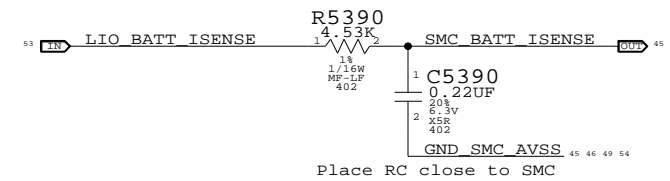
CPU Current Sense Filter



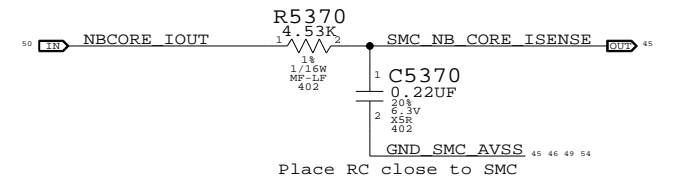
DCIN Current Sense Filter



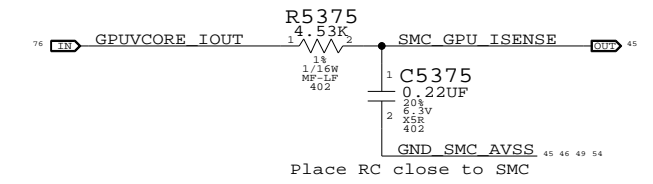
Battery (PBUS) Current Sense Filter



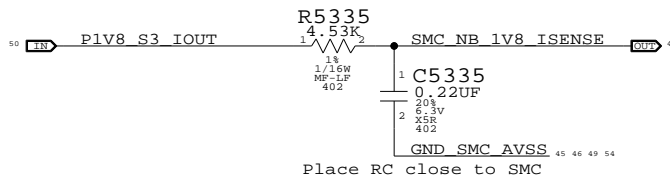
NB Core Current Sense Filter



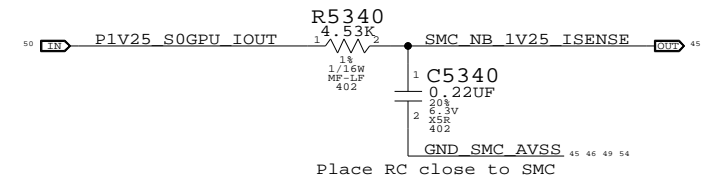
GPU Current Sense Filter



NB 1.8V Current Sense Filter

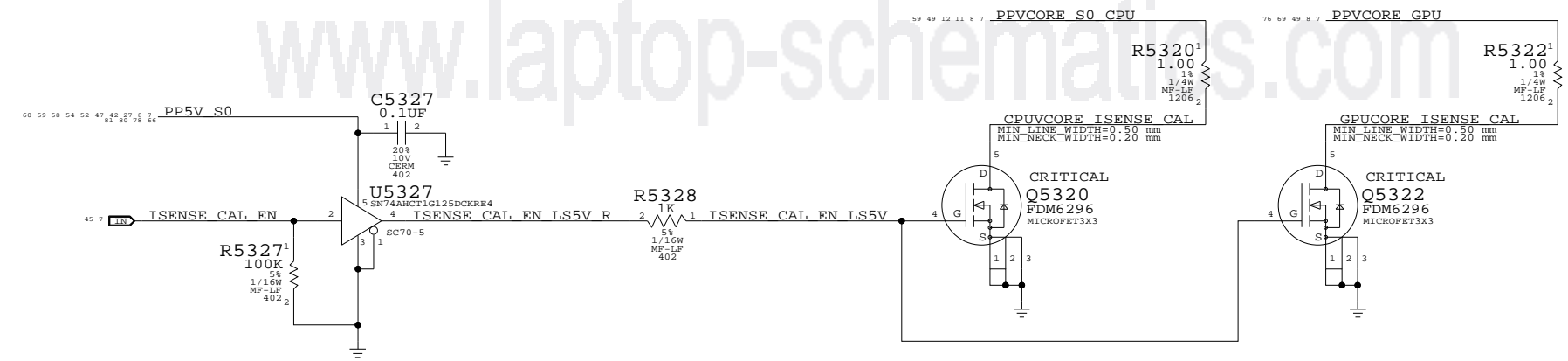


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

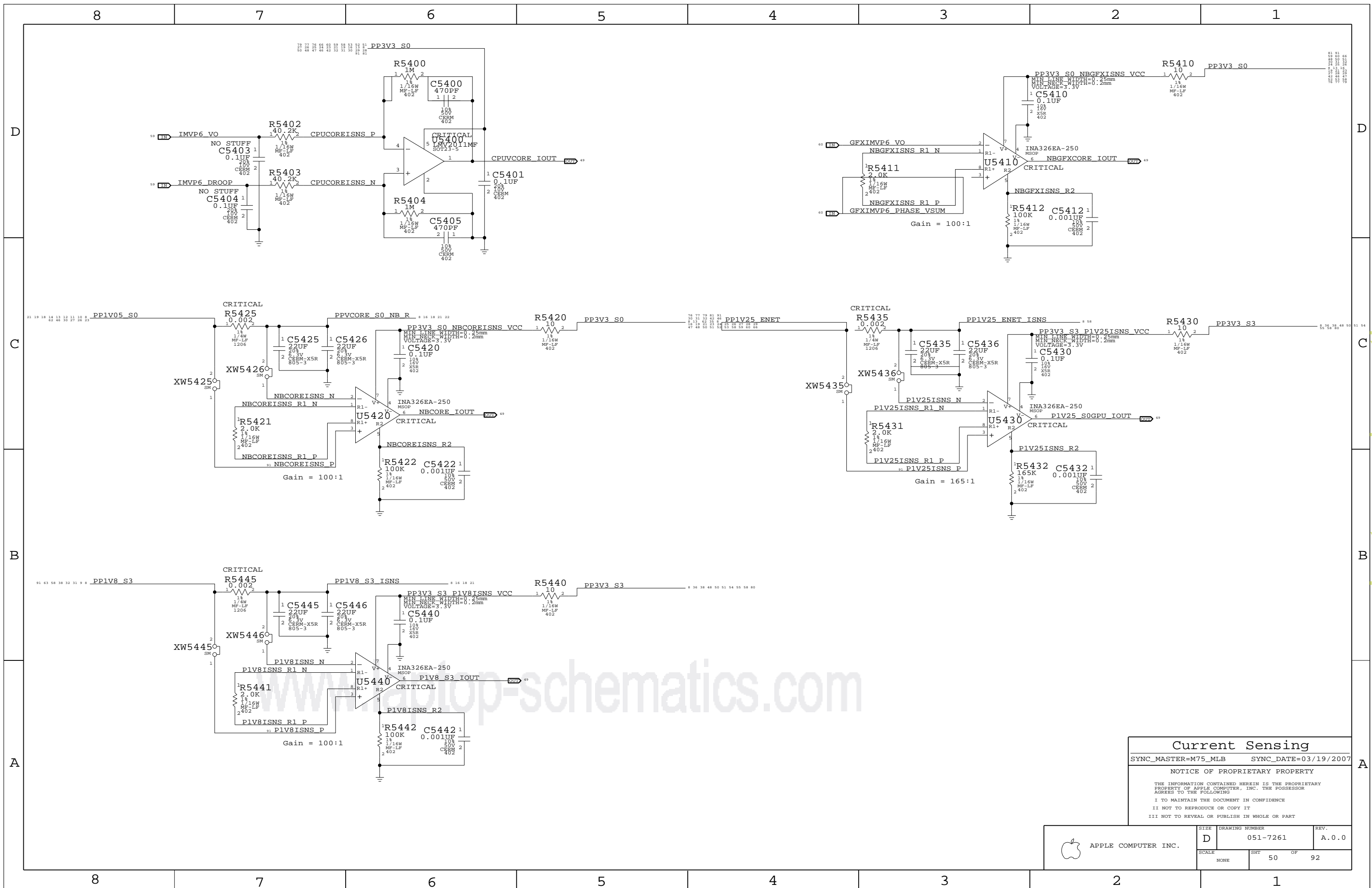
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	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	49	92	

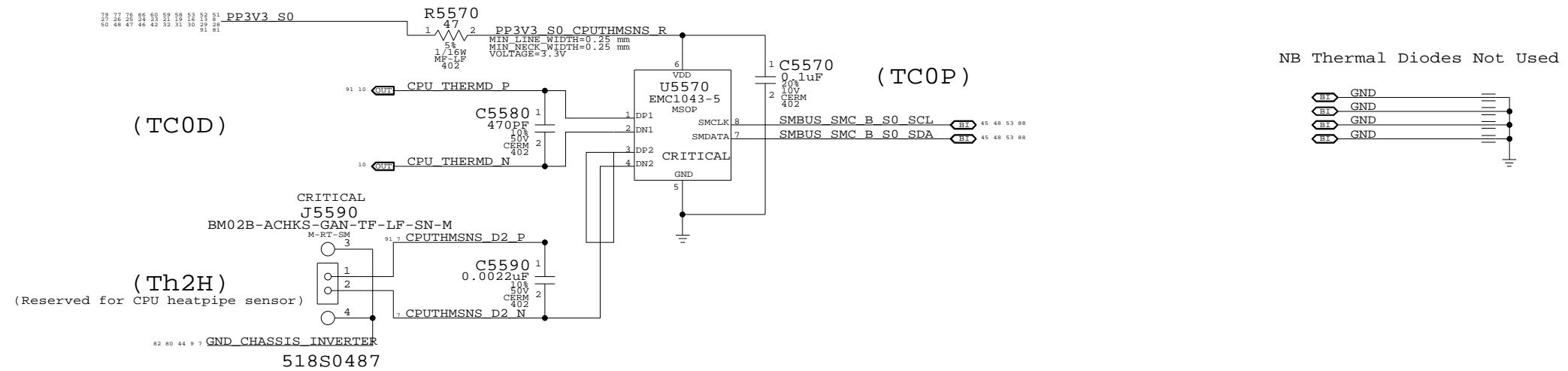


Current Sensing
 SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007
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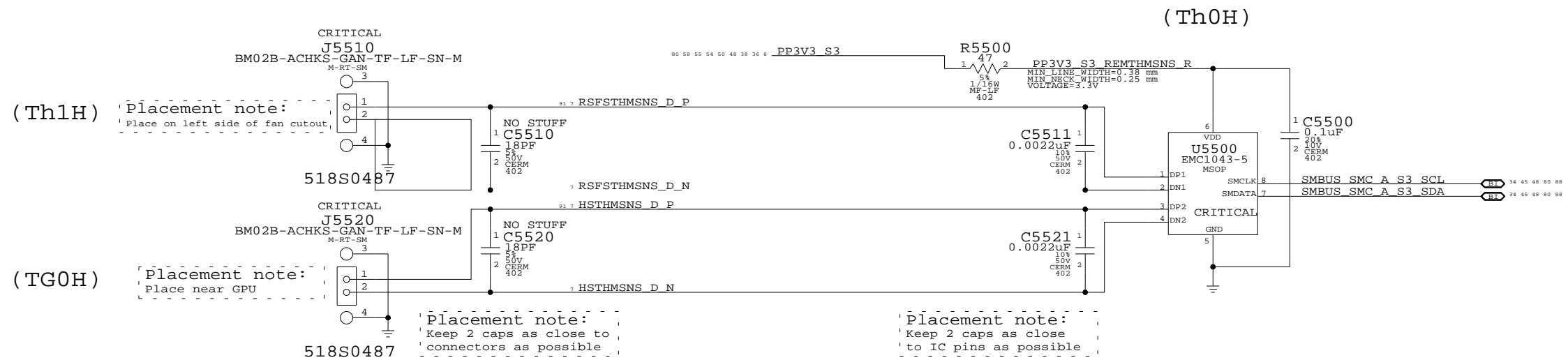
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	50	92	

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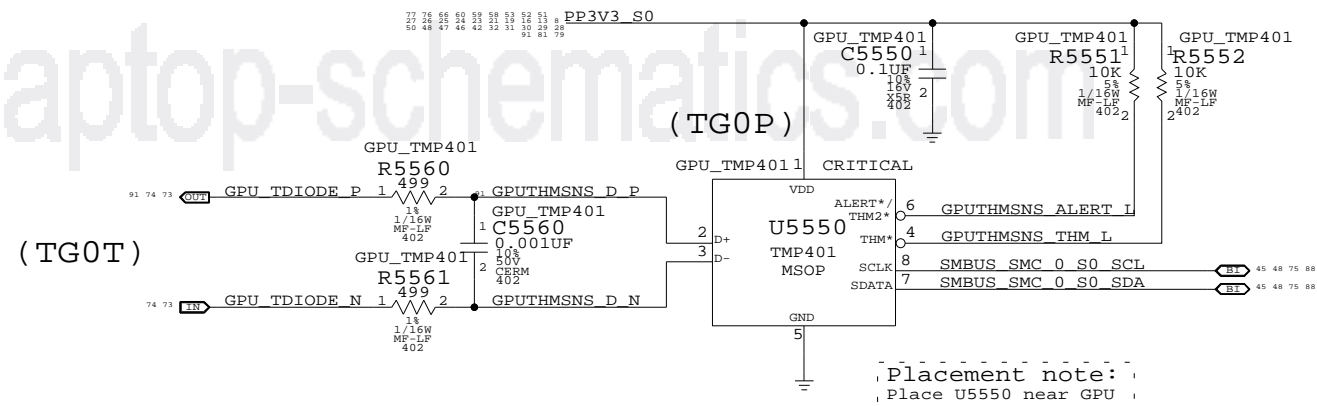
CPU T-Diode Thermal Sensor



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



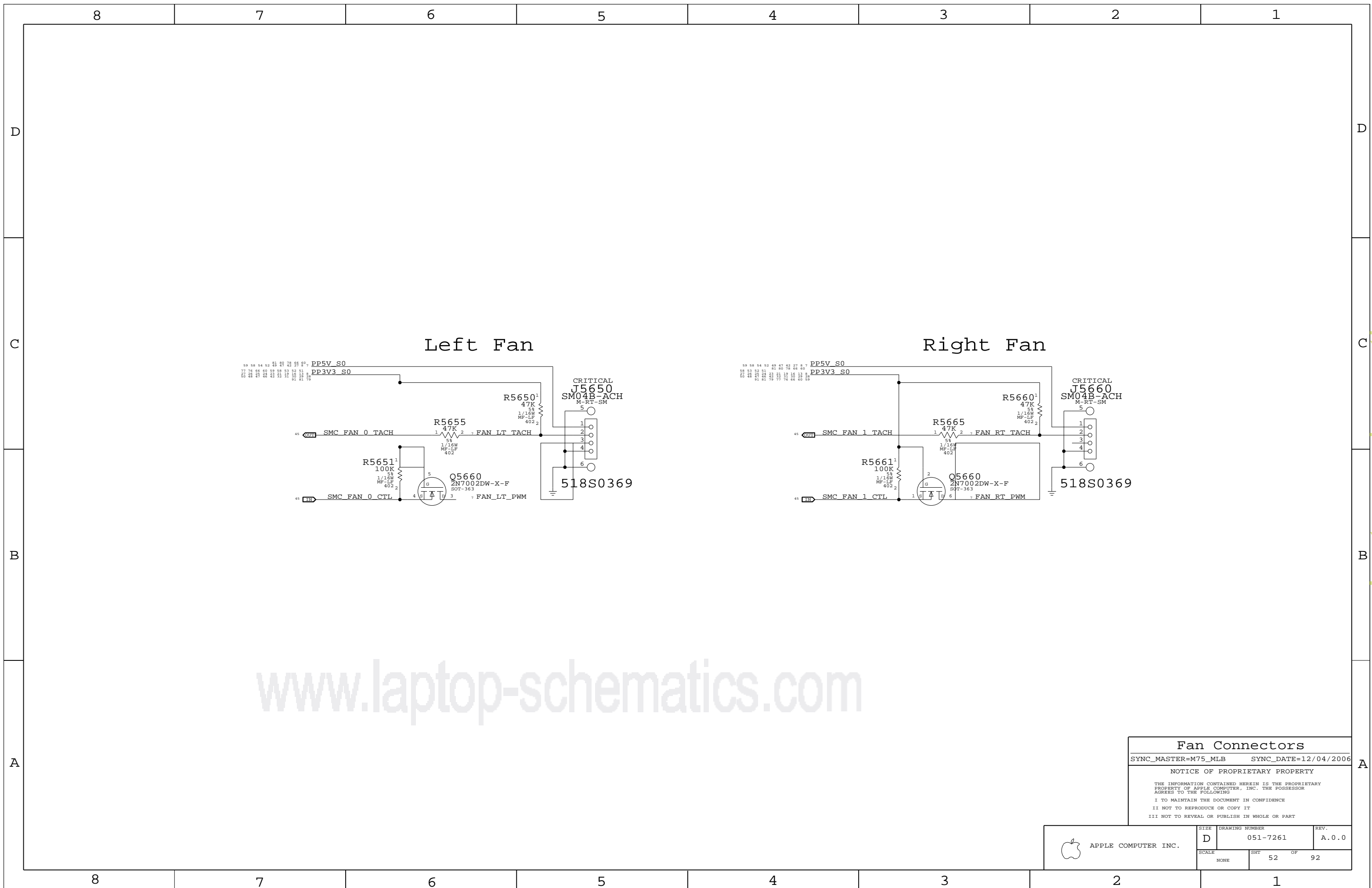
GPU Die Thermal Sensor



Thermal Sensors		
SYNC_MASTER=M75_MLB	SYNC_DATE=03/19/2007	
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SCALE	SHT	OF	
NONE	51	92	

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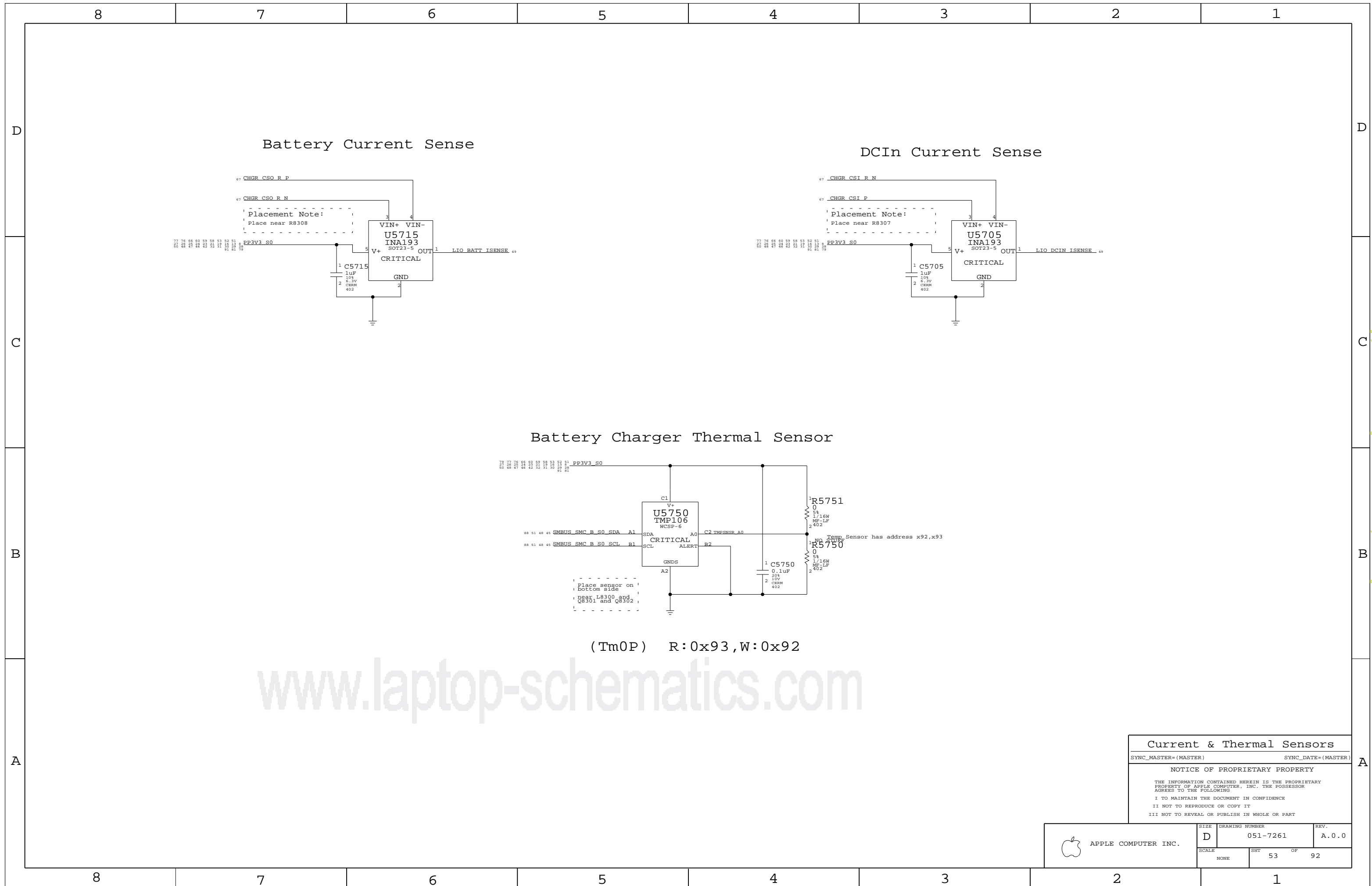


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Fan Connectors
 SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006
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	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	52		92



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Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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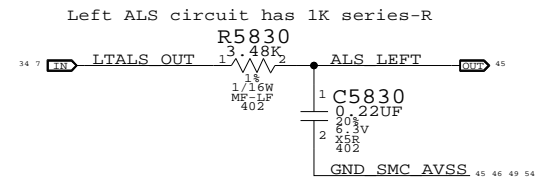
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

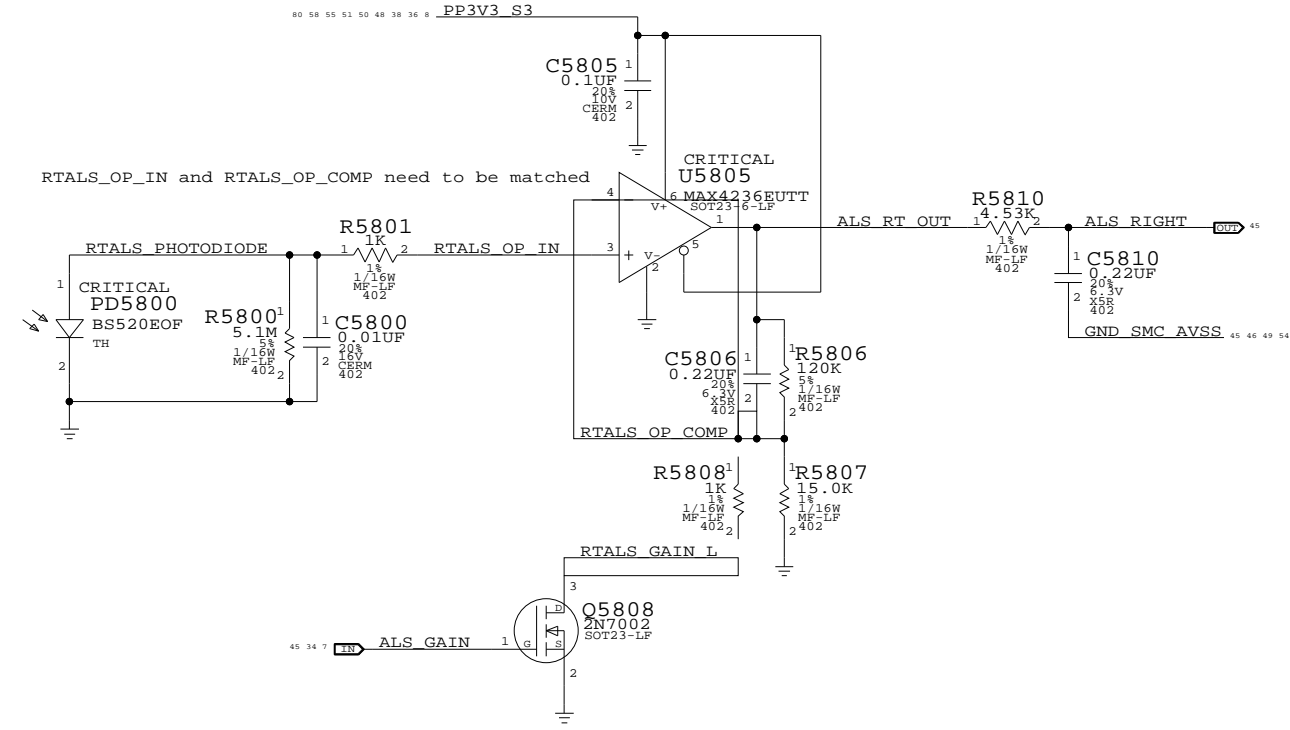
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT		OF
NONE	53		92

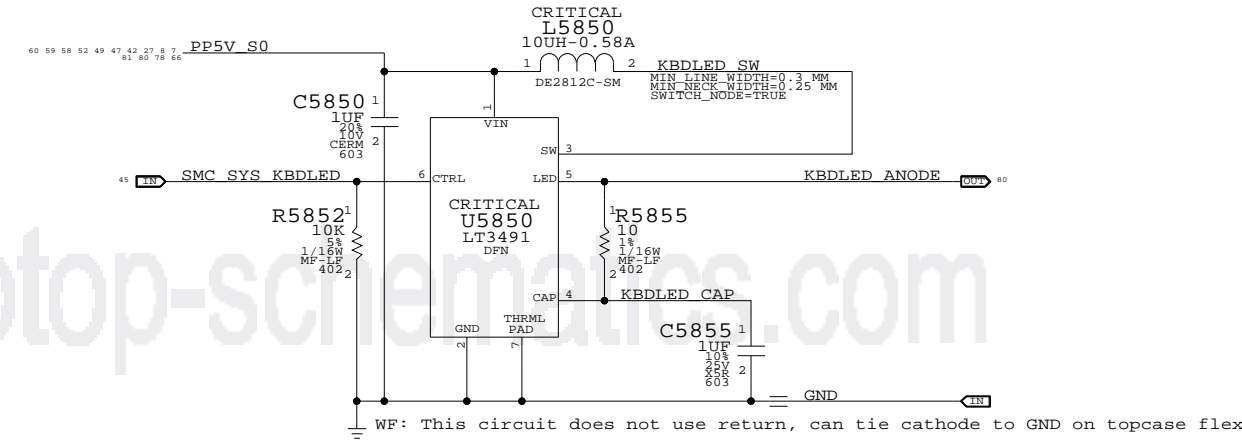
Left ALS Filter



Right ALS Circuit

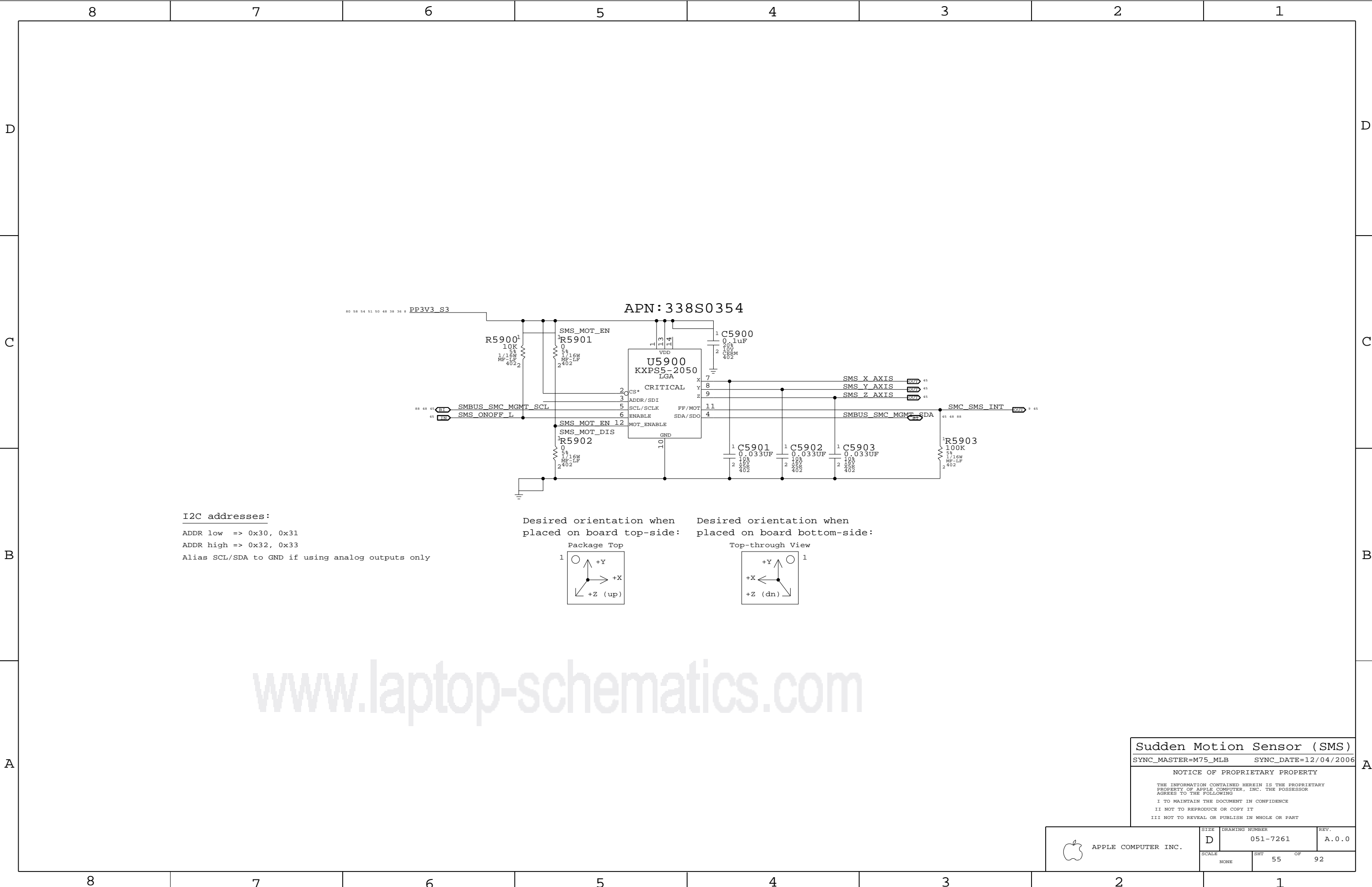


Keyboard LED Driver



ALS Support
 SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	REV.
NONE	54	92	



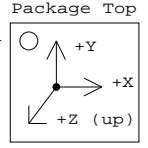
APN: 338S0354

I2C addresses:

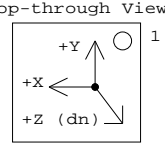
ADDR low => 0x30, 0x31
 ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



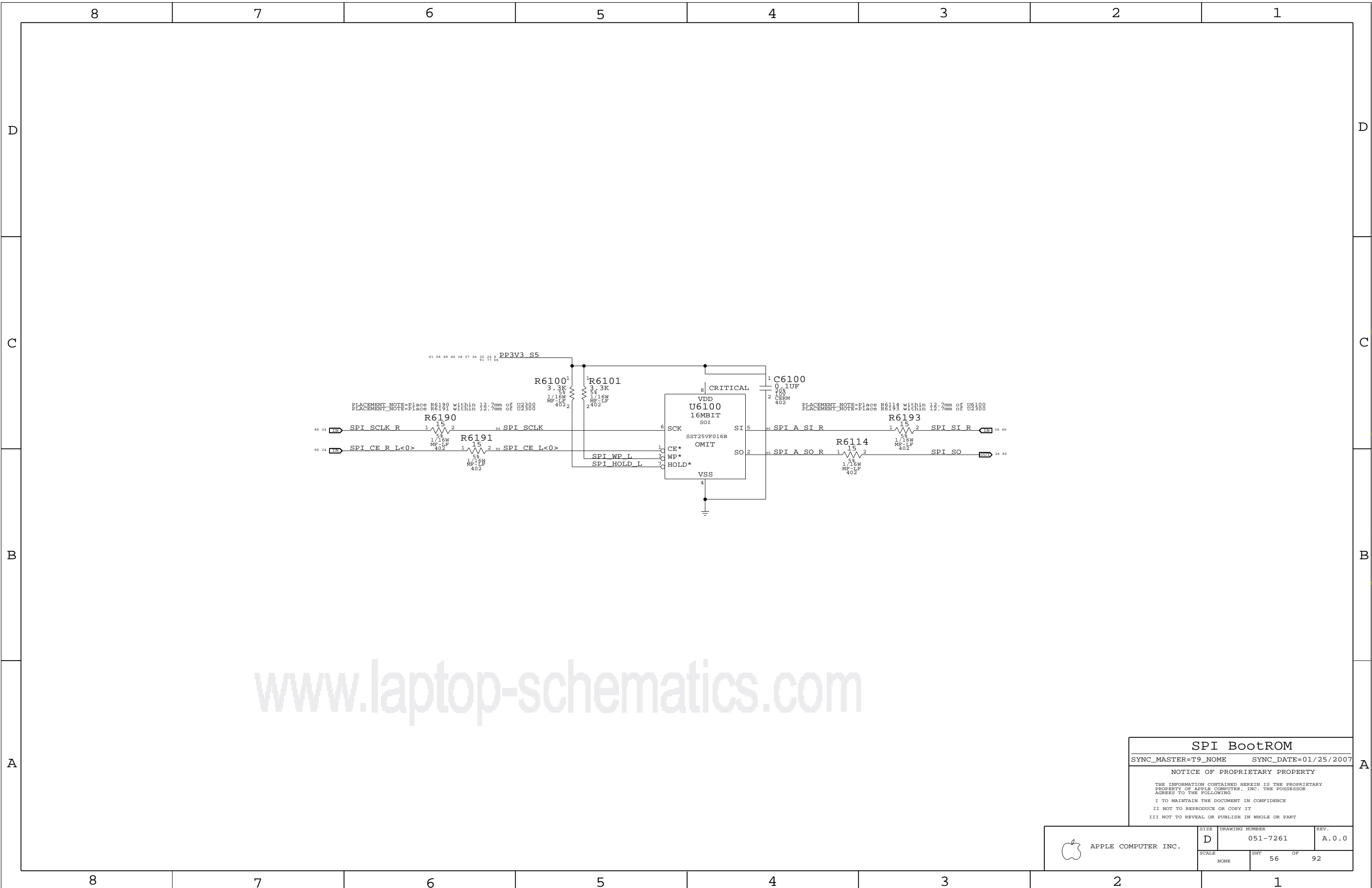
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Sudden Motion Sensor (SMS)
 SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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SCALE	SHT	OF	
NONE	55	92	



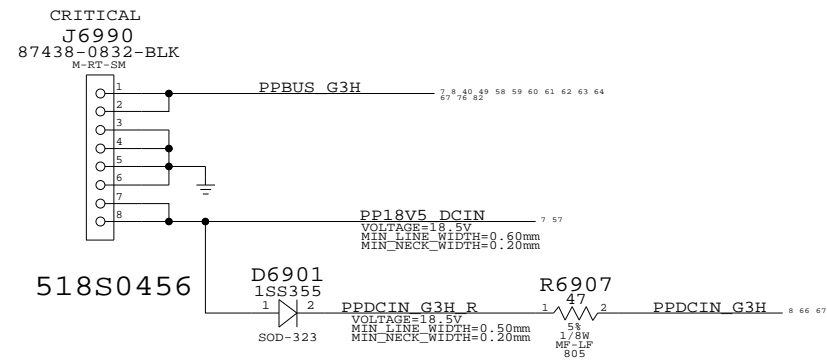
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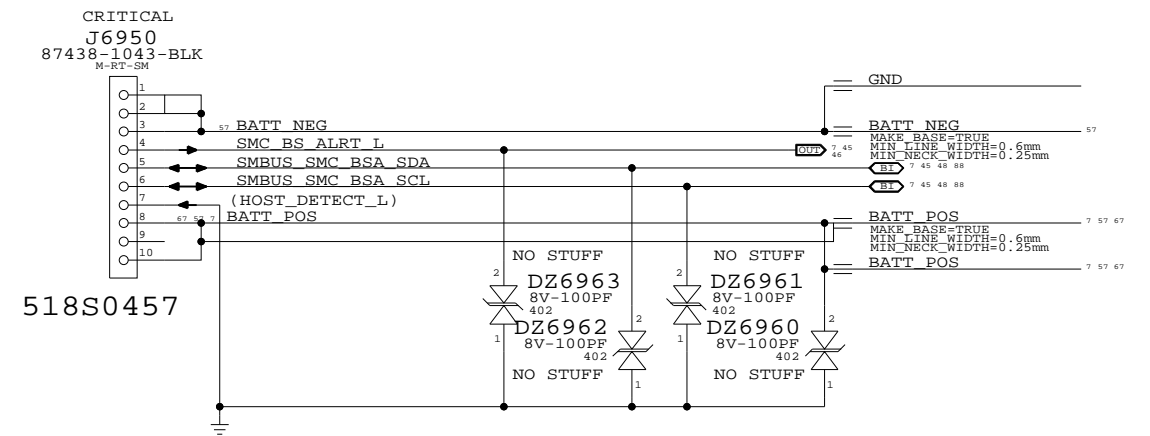
SPI BootROM
 SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007
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	D	051-7261	A.0.0
SCALE	SHT		OF
NONE	56		92

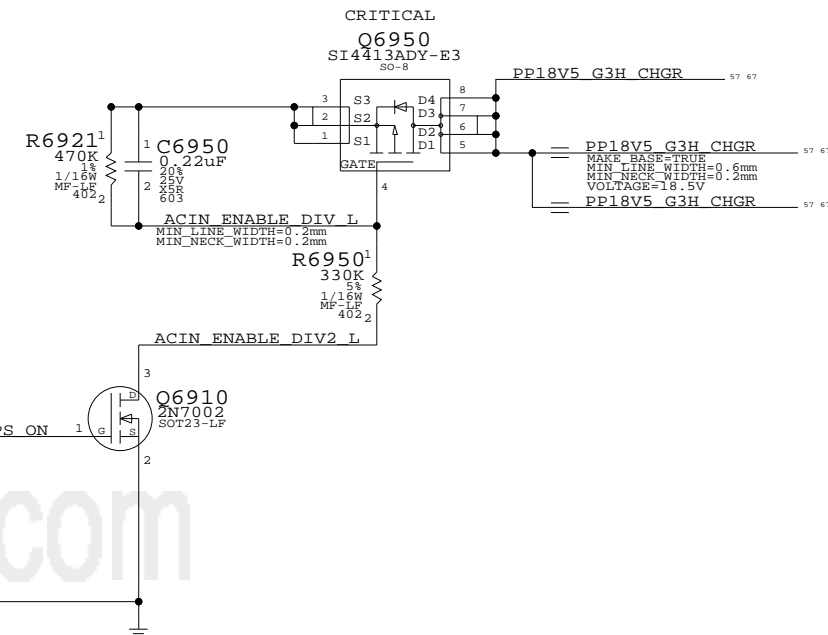
DC-In Connector



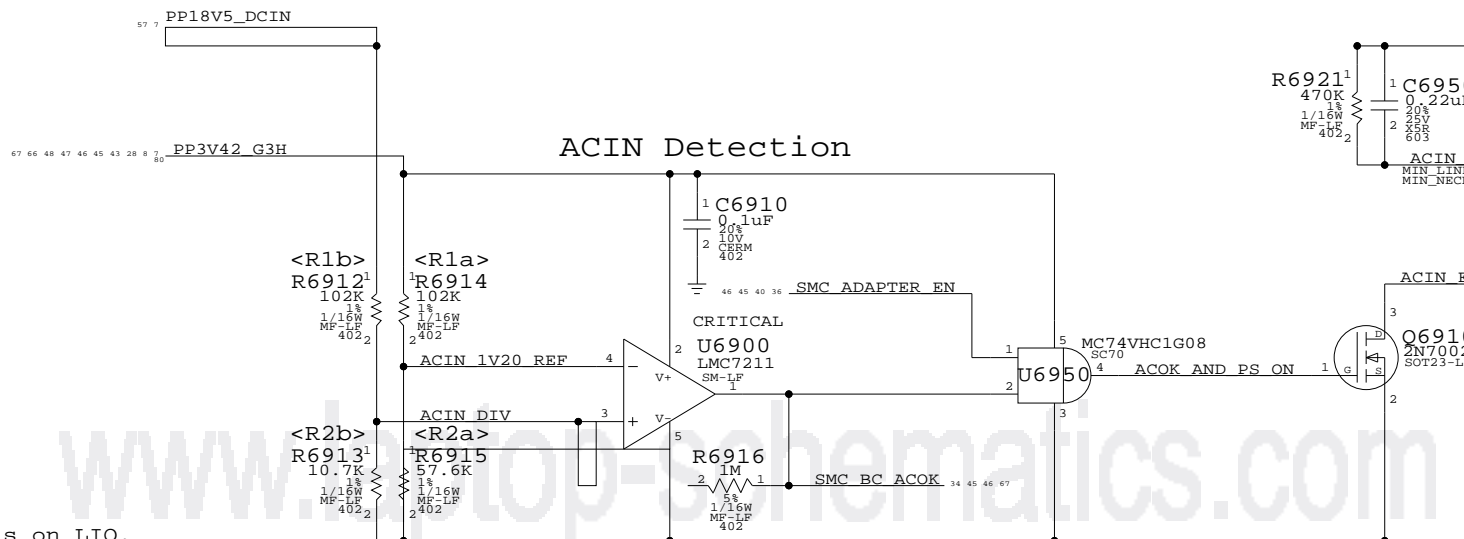
Battery Connector



Inrush Limiter



ACIN Detection



NOTE: R6910 is on LIO.
System must provide 10K-70K impedance to A52 adapter for system load detection.
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

$$V_{ref} = 3.42V * (R2a / (R1a + R2a))$$

$$V_{th} = (V_{ref} / (R2b / (R1b + R2b)))$$

$$V_{ref} = 1.23V$$

$$V_{th} = 13.0V$$

Assuming 1% variance for R6910-R6915 and 3.42V:
Worst case Vth: min:12.47V, max: 13.54V

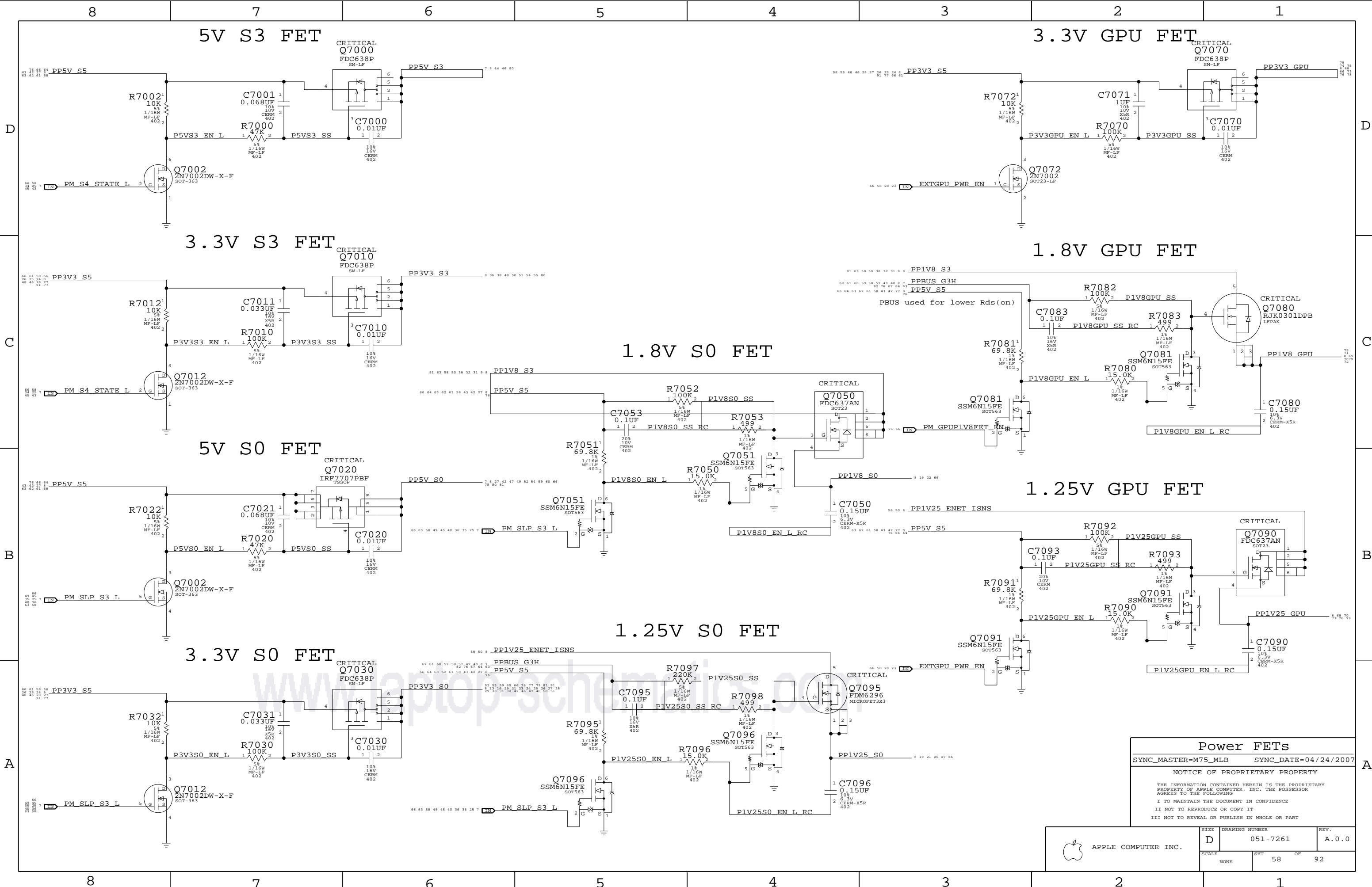
DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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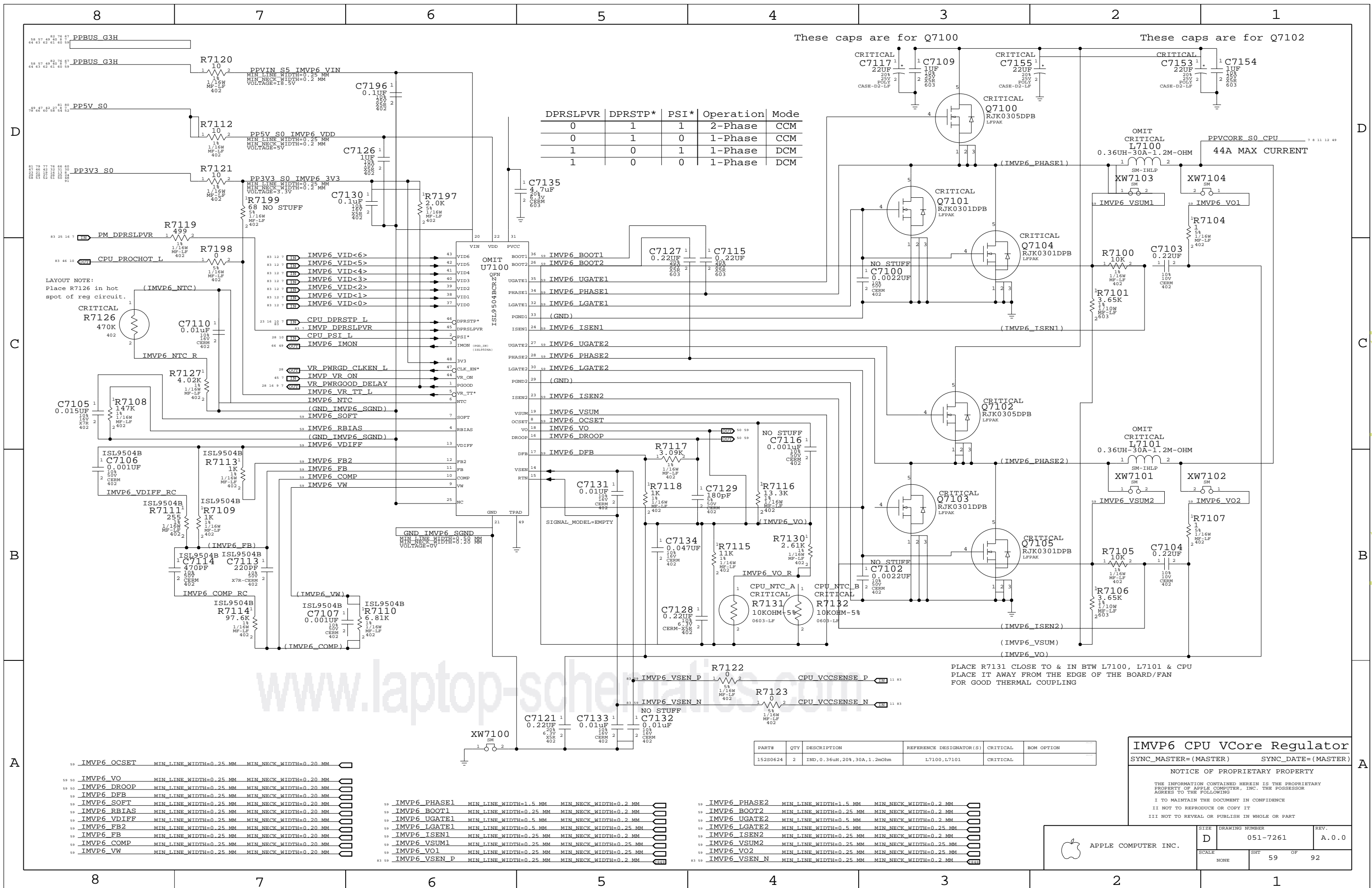
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	57	92	



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Power FETs
 SYNC_MASTER=M75_MLB SYNC_DATE=04/24/2007
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	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	58	92	



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

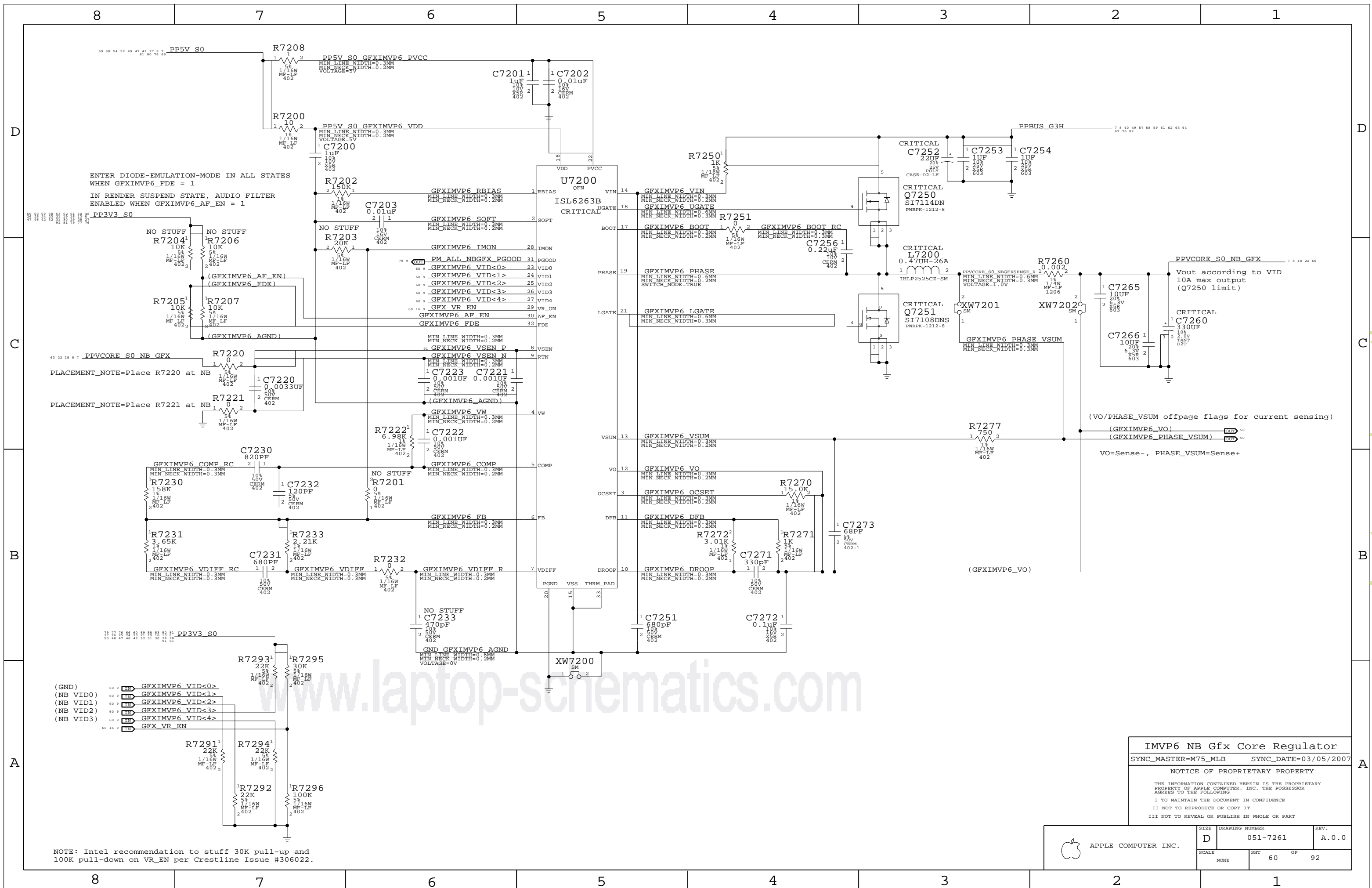
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0624	2	IND, 0.36uH, 20%, 30A, 1.2mOhm	L7100, L7101	CRITICAL	

IMVP6 CPU VCore Regulator
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7261	A.0.0
SCALE	SHEET	OF	
NONE	59	92	

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ENTER DIODE-EMULATION-MODE IN ALL STATES
WHEN GFXIMVP6_FDE = 1
IN RENDER SUSPEND STATE, AUDIO FILTER
ENABLED WHEN GFXIMVP6_AF_EN = 1

PLACEMENT_NOTE=Place R7220 at NB
PLACEMENT_NOTE=Place R7221 at NB

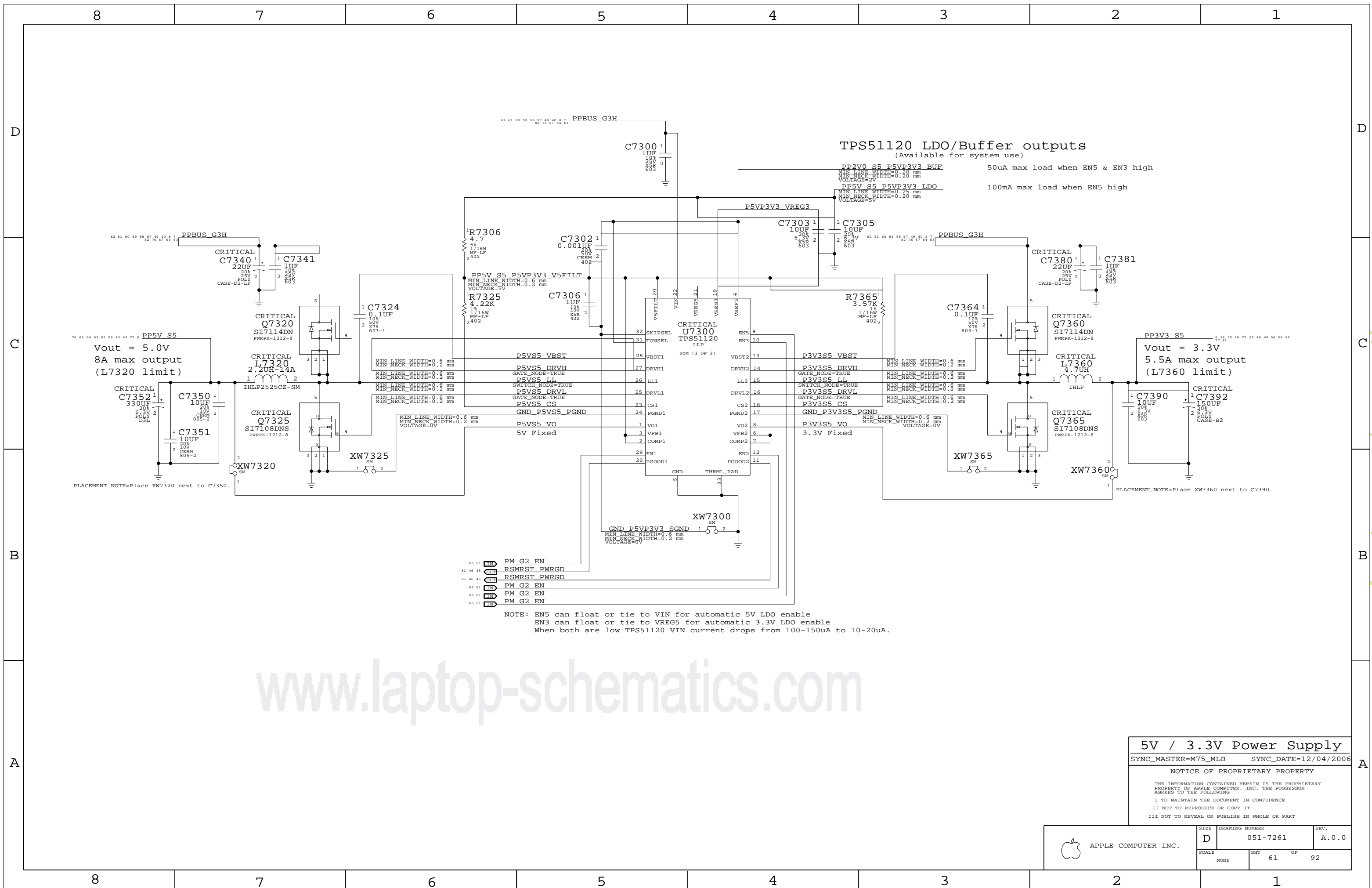
NOTE: Intel recommendation to stuff 30K pull-up and
100K pull-down on VR_EN per Crestline Issue #306022.

IMVP6 NB Gfx Core Regulator
SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	92
NONE	60		

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TPS51120 LDO/Buffer outputs
(Available for system use)

PP2V0 S5 P5VP3V3 BUF 50uA max load when EN5 & EN3 high
MIN_LINE_WIDTH=0.20 mm
MIN_NECK_WIDTH=0.20 mm
VOLTAGE=2V

PP5V S5 P5VP3V3 LDO 100mA max load when EN5 high
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.20 mm
VOLTAGE=5V

Vout = 5.0V
8A max output
(L7320 limit)

Vout = 3.3V
5.5A max output
(L7360 limit)

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

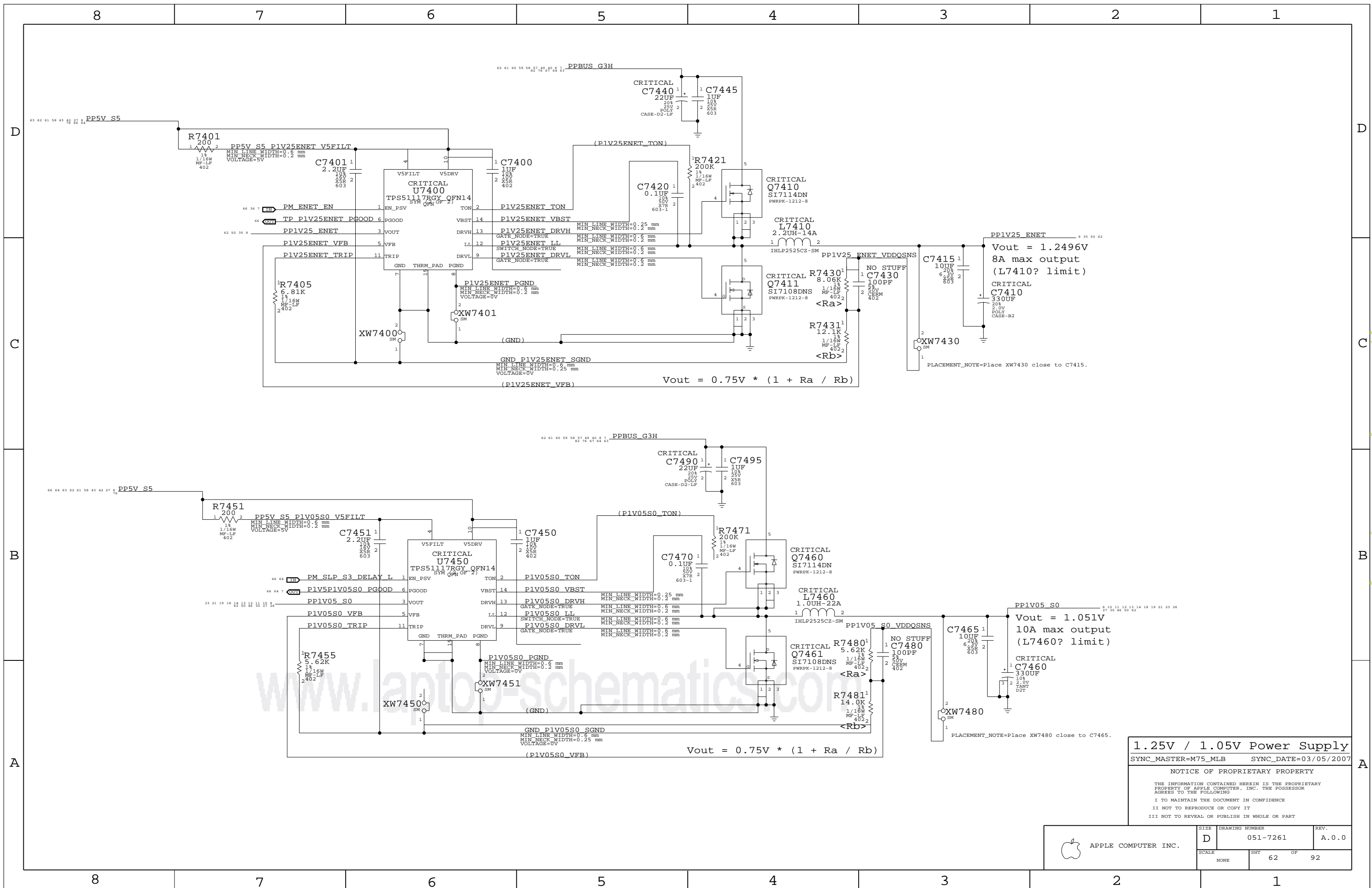
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5V / 3.3V Power Supply
SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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	D	051-7261	A.0.0
SCALE	SHT 61 OF 92		
NONE			

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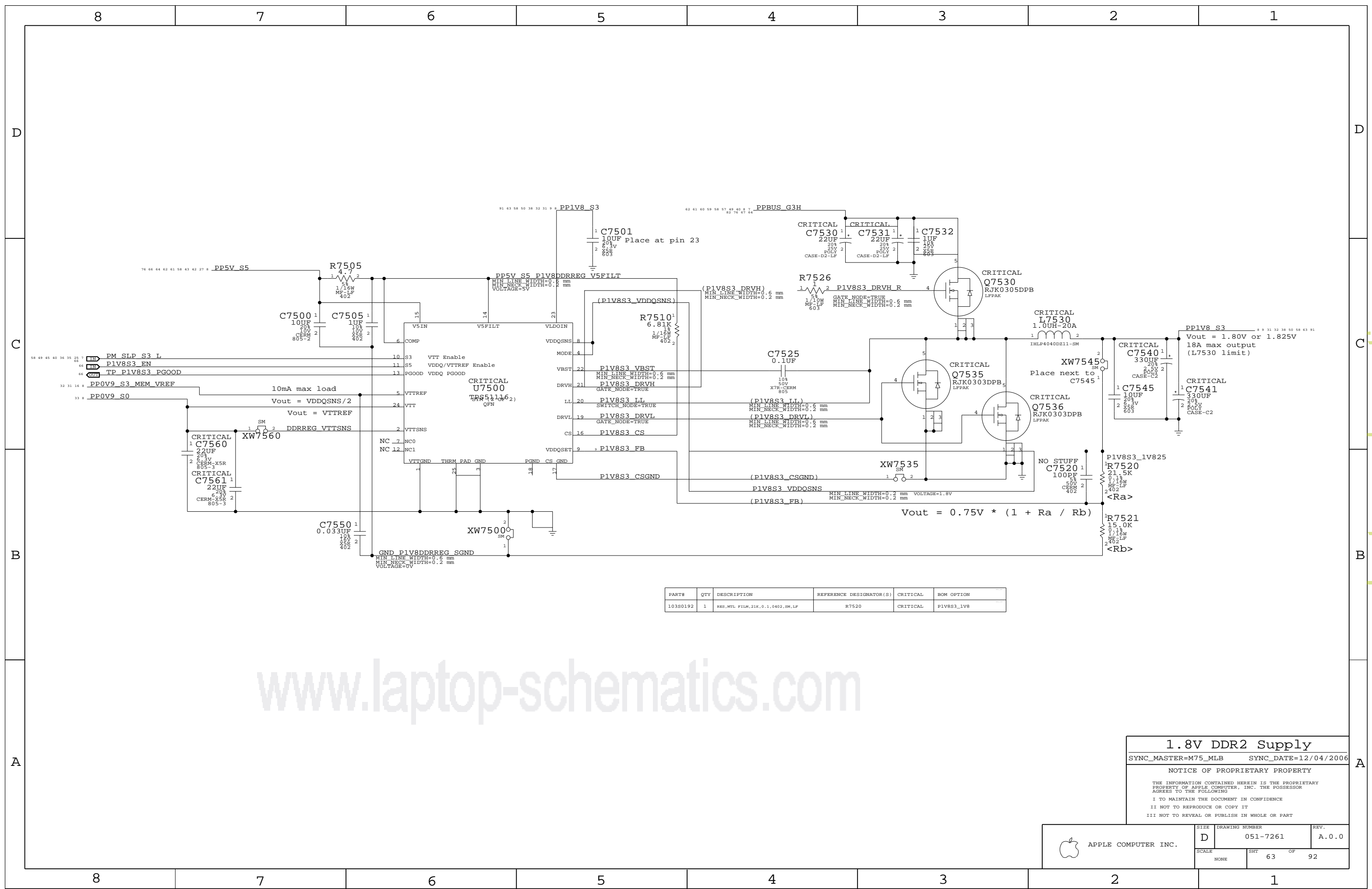


1.25V / 1.05V Power Supply
 SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	92
NONE	62		

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10380192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V8

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1.8V DDR2 Supply
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	D	051-7261	A.0.0
SCALE	NONE	SHT	63 OF 92

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D

D

C

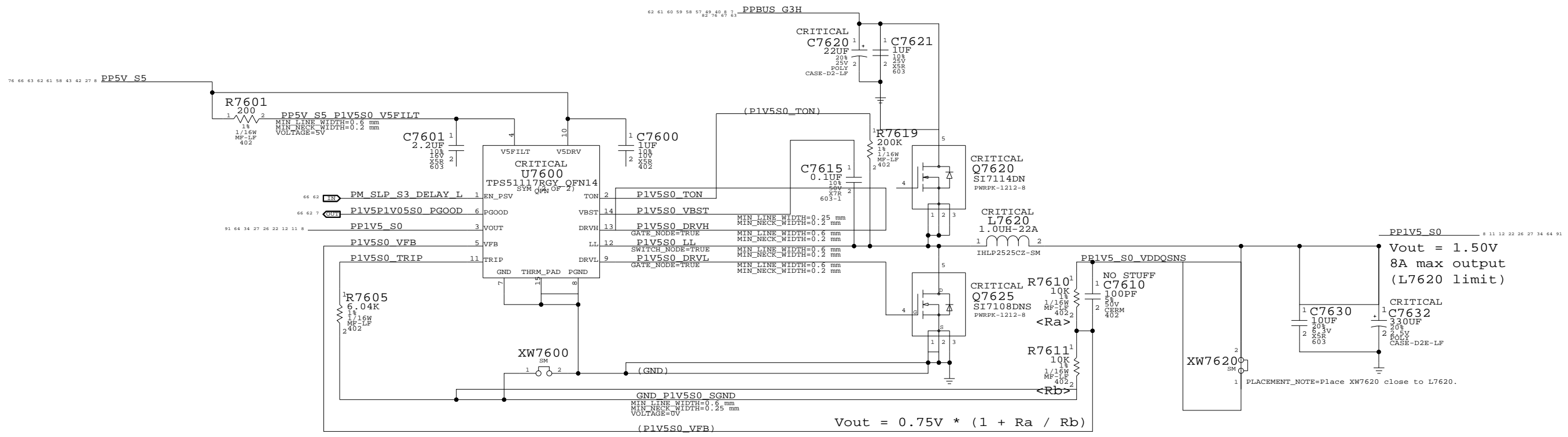
C

B

B

A

A



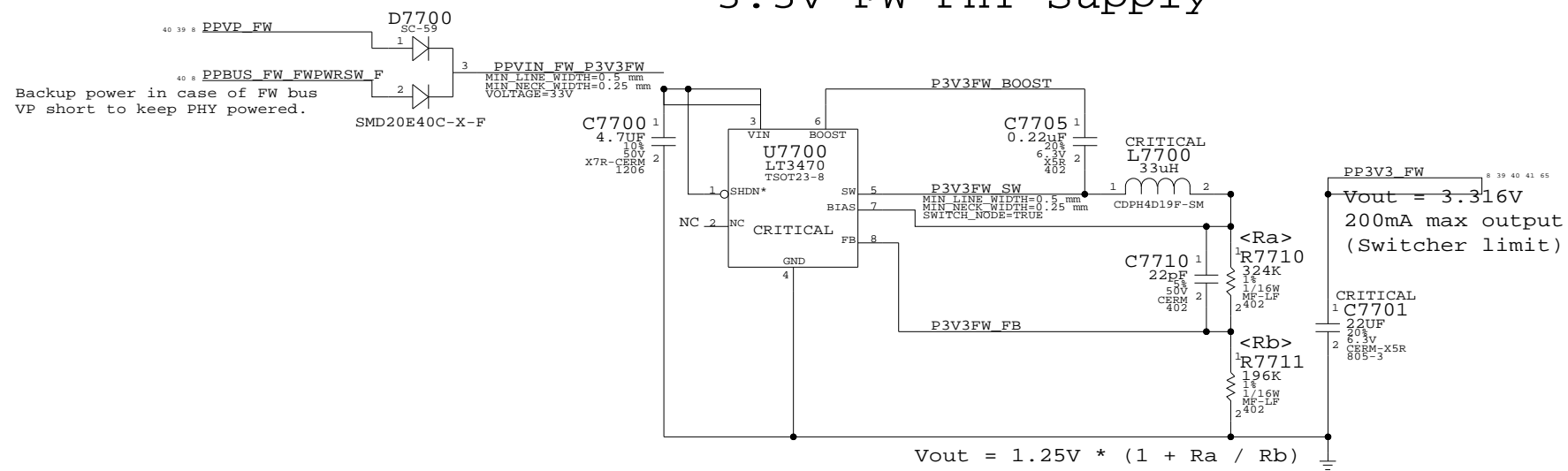
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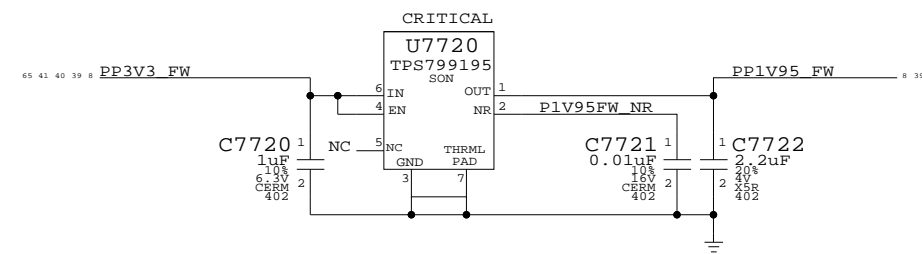
1.5V Power Supply
 SYNC_MASTER=M75_MLB SYNC_DATE=03/05/2007
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	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	64	92	

3.3V FW PHY Supply



1.95V FW PHY Supply



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FW PHY Power Supplies

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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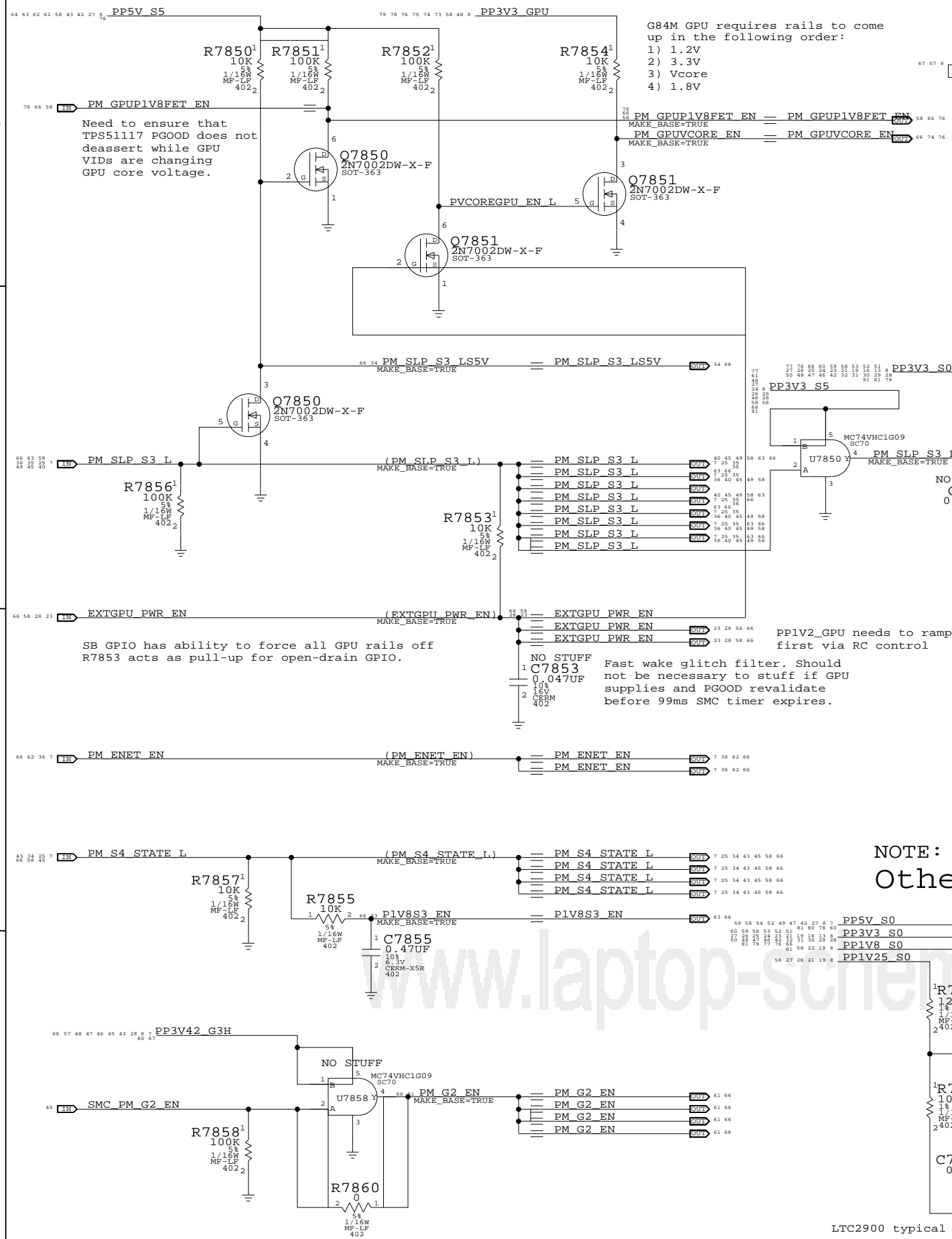
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	65	92	

Power Control Signals

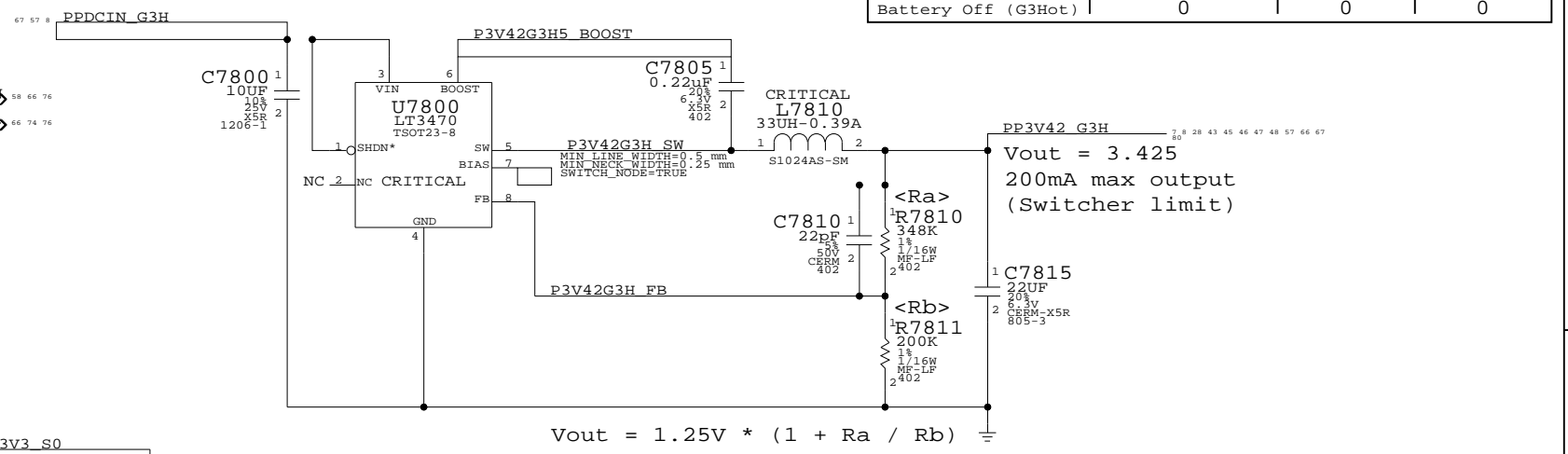


- G84M GPU requires rails to come up in the following order:
- 1) 1.2V
 - 2) 3.3V
 - 3) Vcore
 - 4) 1.8V

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

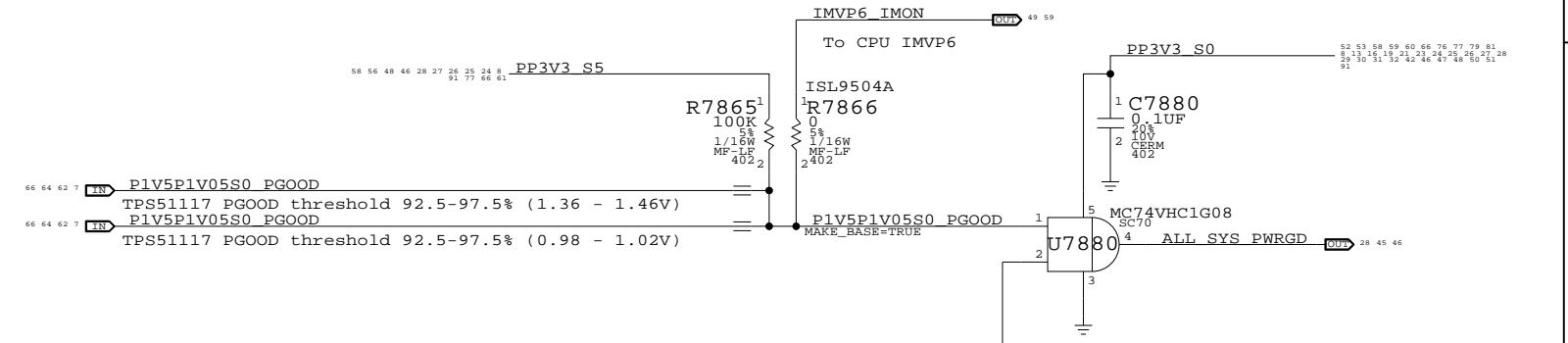


Unused PGOOD Signals

- TP_P1V25ENET_PGOOD = TP_P1V25ENET_PGOOD
- TP_P1V8S3_PGOOD = TP_P1V8S3_PGOOD

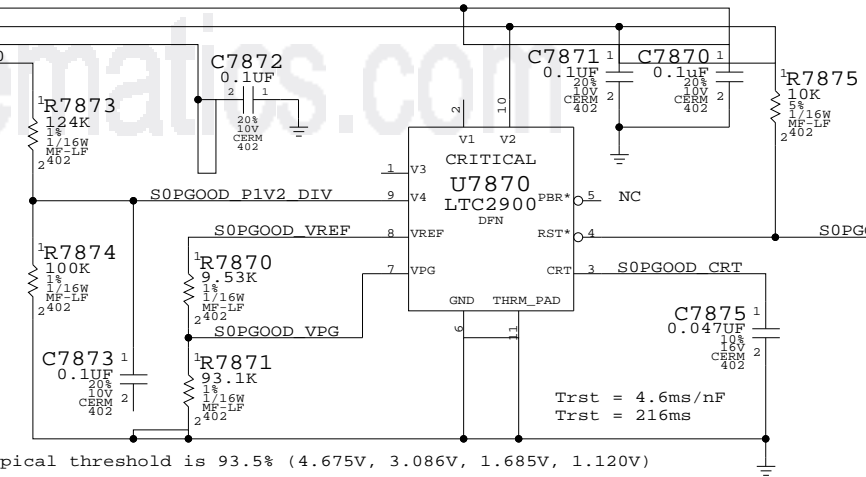
1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



NOTE: 0.9V/2.5V is not checked! Other S0 Rails PWRGD Circuit

Does not include GFX rails



3.425V G3Hot Supply & Power Control

SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

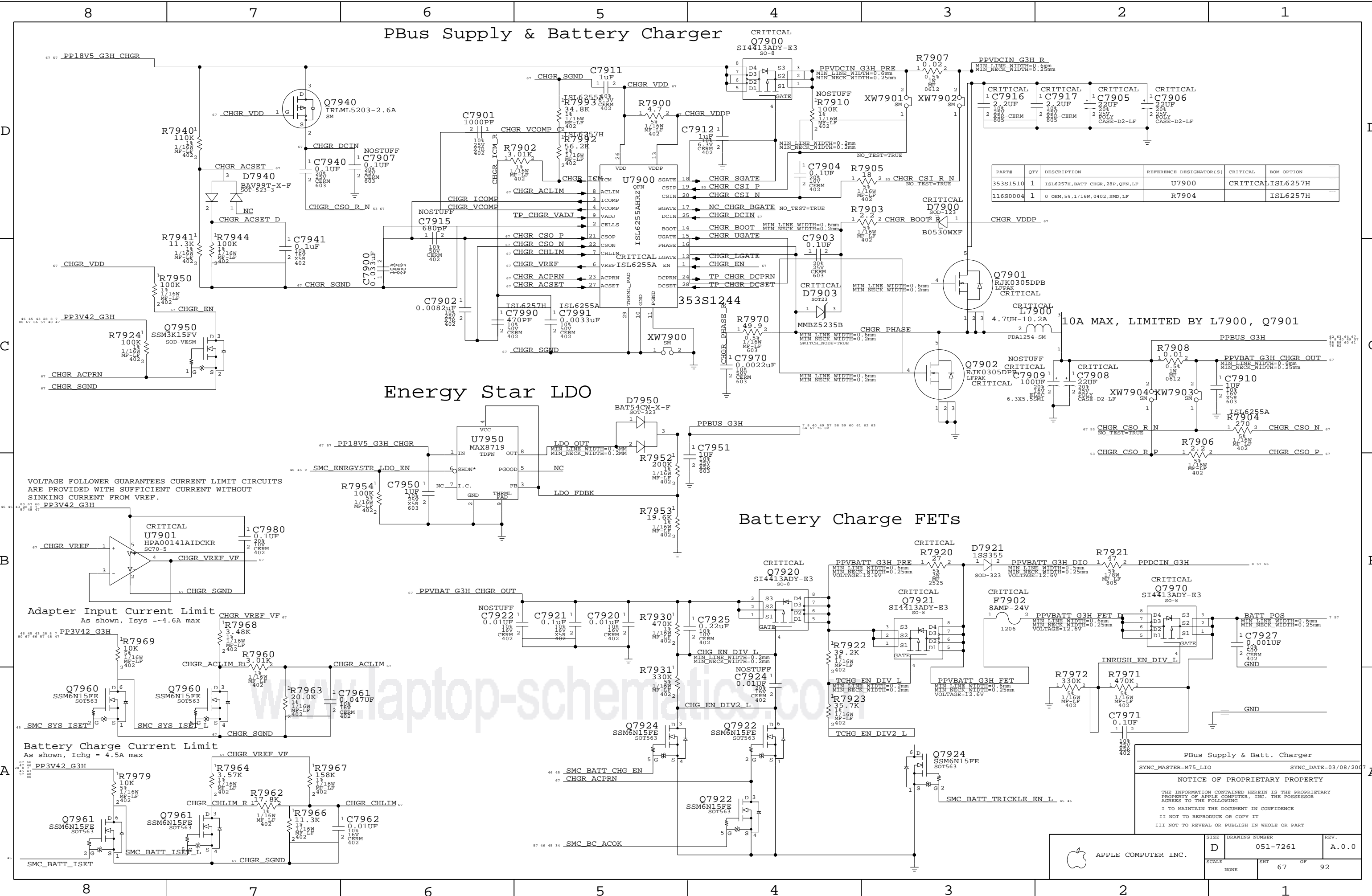
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	66	92	

PBus Supply & Battery Charger



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H, BATT CHGR, 28P, QFN, LF	U7900	CRITICAL	ISL6257H
116S0004	1	0 OHM, 5%, 1/16W, 0402, SMD, LF	R7904		ISL6257H

10A MAX, LIMITED BY L7900, Q7901

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

Adapter Input Current Limit
As shown, Isys = -4.6A max

Battery Charge Current Limit
As shown, Ichg = 4.5A max

Battery Charge FETs

PBus Supply & Batt. Charger
 SYNC_MASTER=M75_LIO SYNC_DATE=03/08/2007

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	D	051-7261	A.0.0
SCALE	SHEET	OF	
NONE	67	92	

Page Notes

Power aliases required by this page:

- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

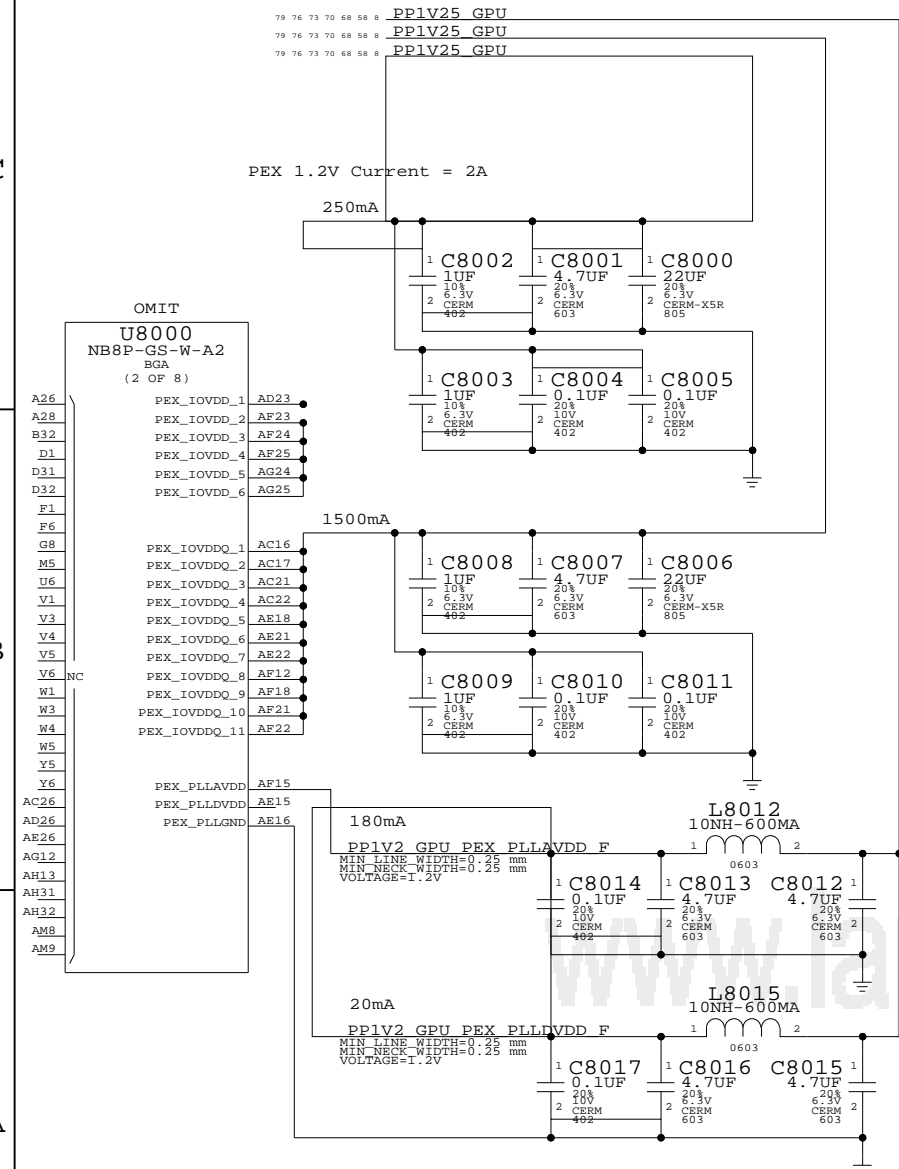
(NONE)

D

C

B

A



OMIT
U8000
NB8P-GS-W-A2
BGA
(1 OF 8)

PCI EXPRESS BUS INTERFACE



OMIT
U8000
NB8P-GS-W-A2
BGA
(1 OF 8)



NV G84M PCI-E
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	68	92	

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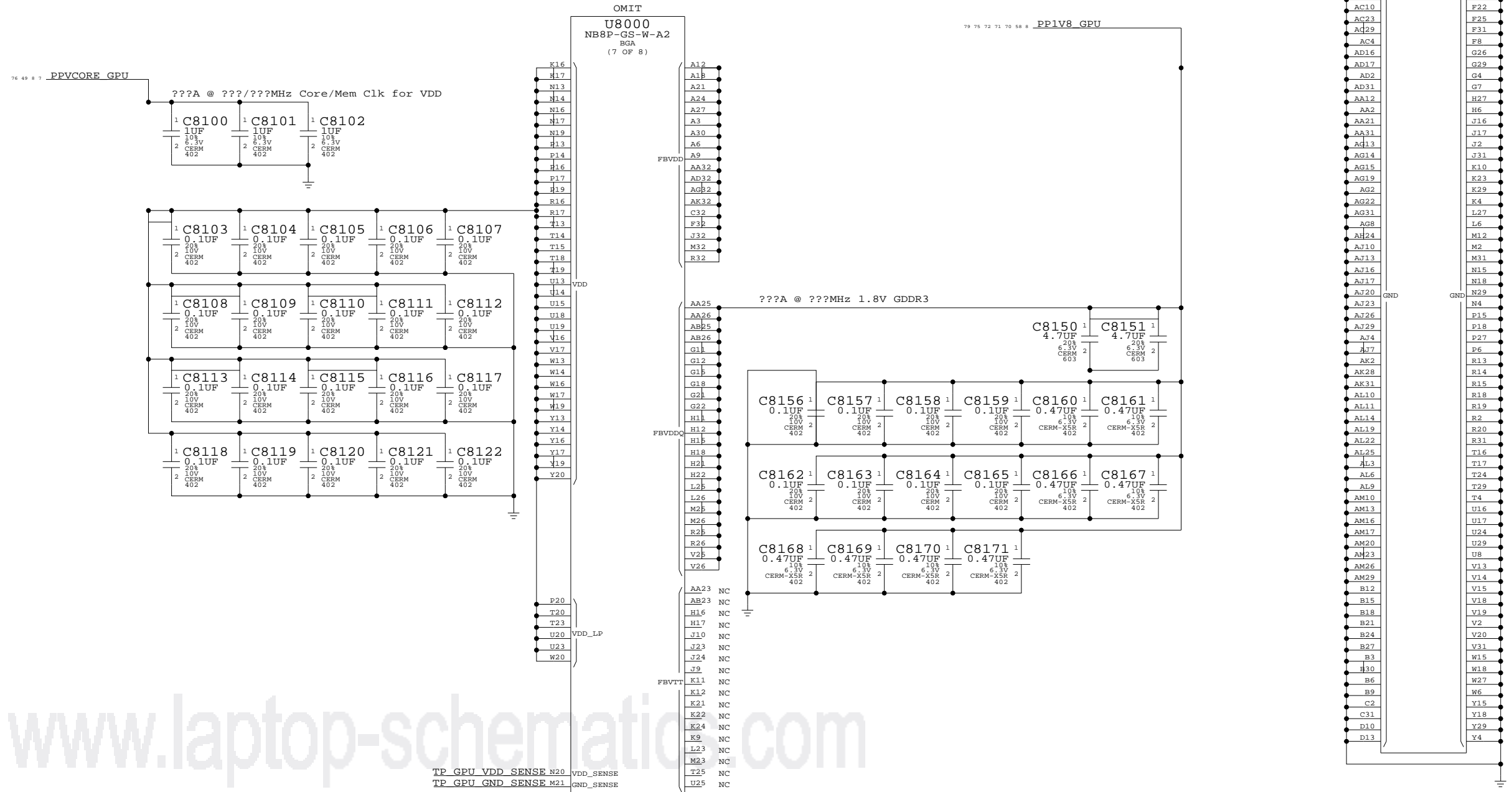
Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V8_GPU_FBVDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	NONE	SHT	69 OF 92

Page Notes

Power aliases required by this page:

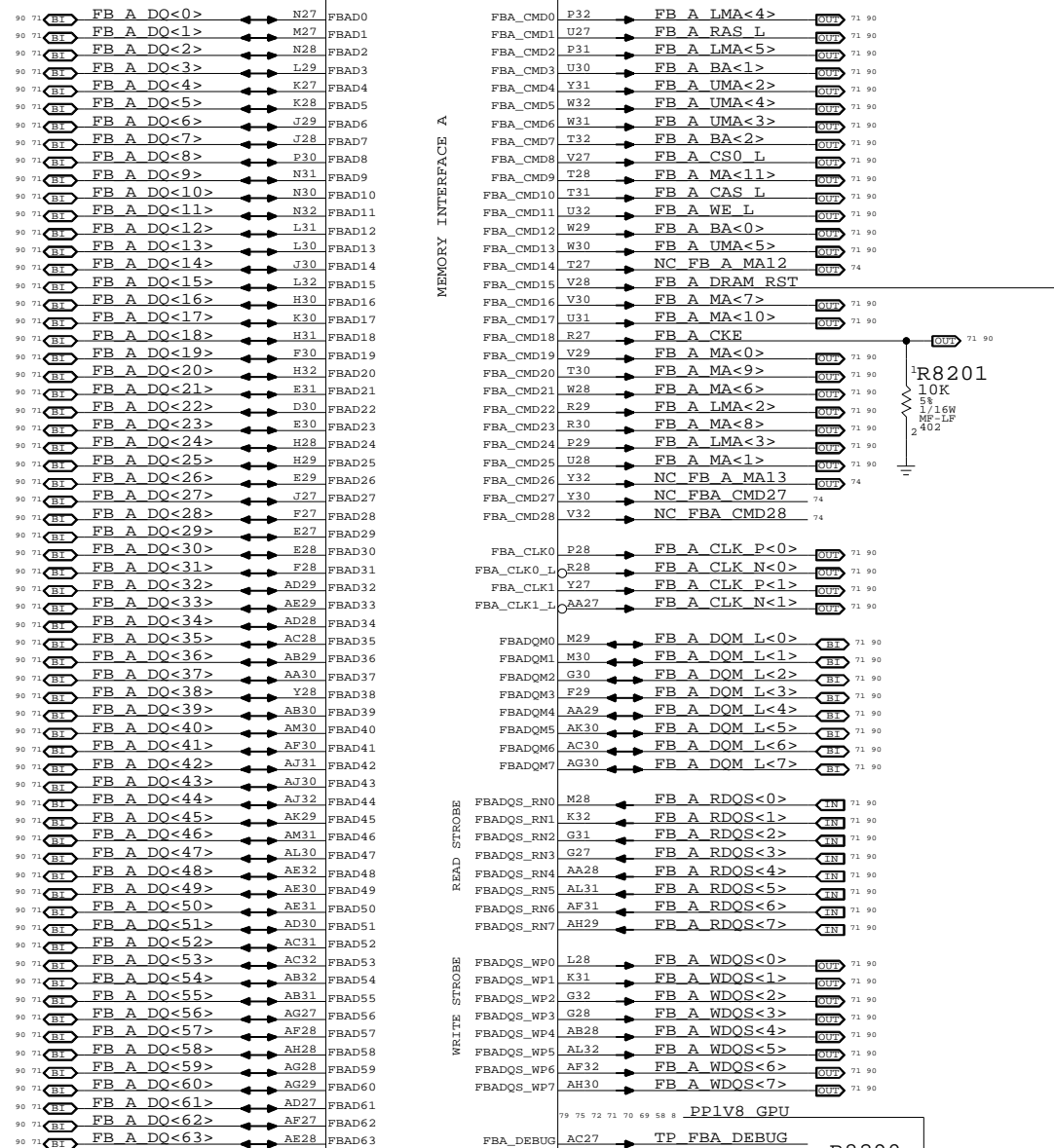
- =PPIV2_GPU_FBPLLAVDD
- =PPIV8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

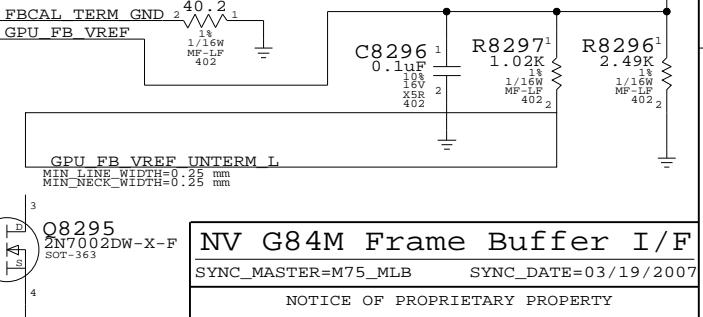
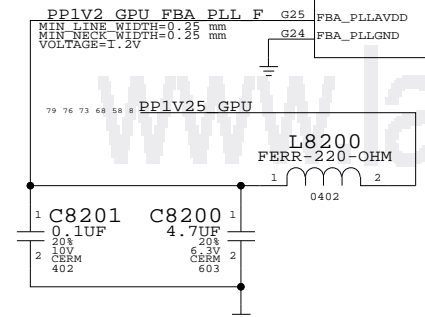
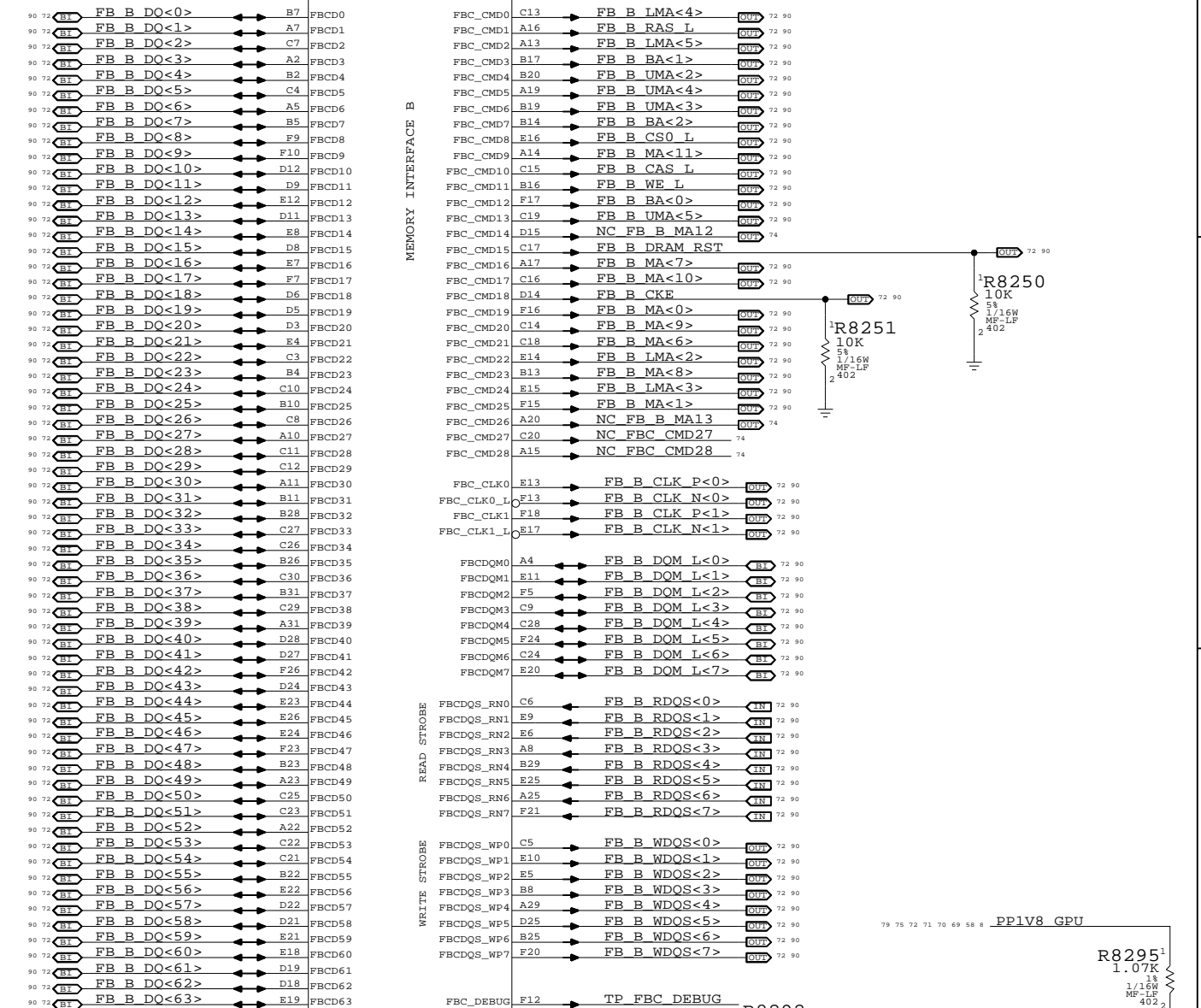
OMIT

U8000
NB8P-GS-W-A2
BGA
(3 OF 8)



OMIT

U8000
NB8P-GS-W-A2
BGA
(4 OF 8)

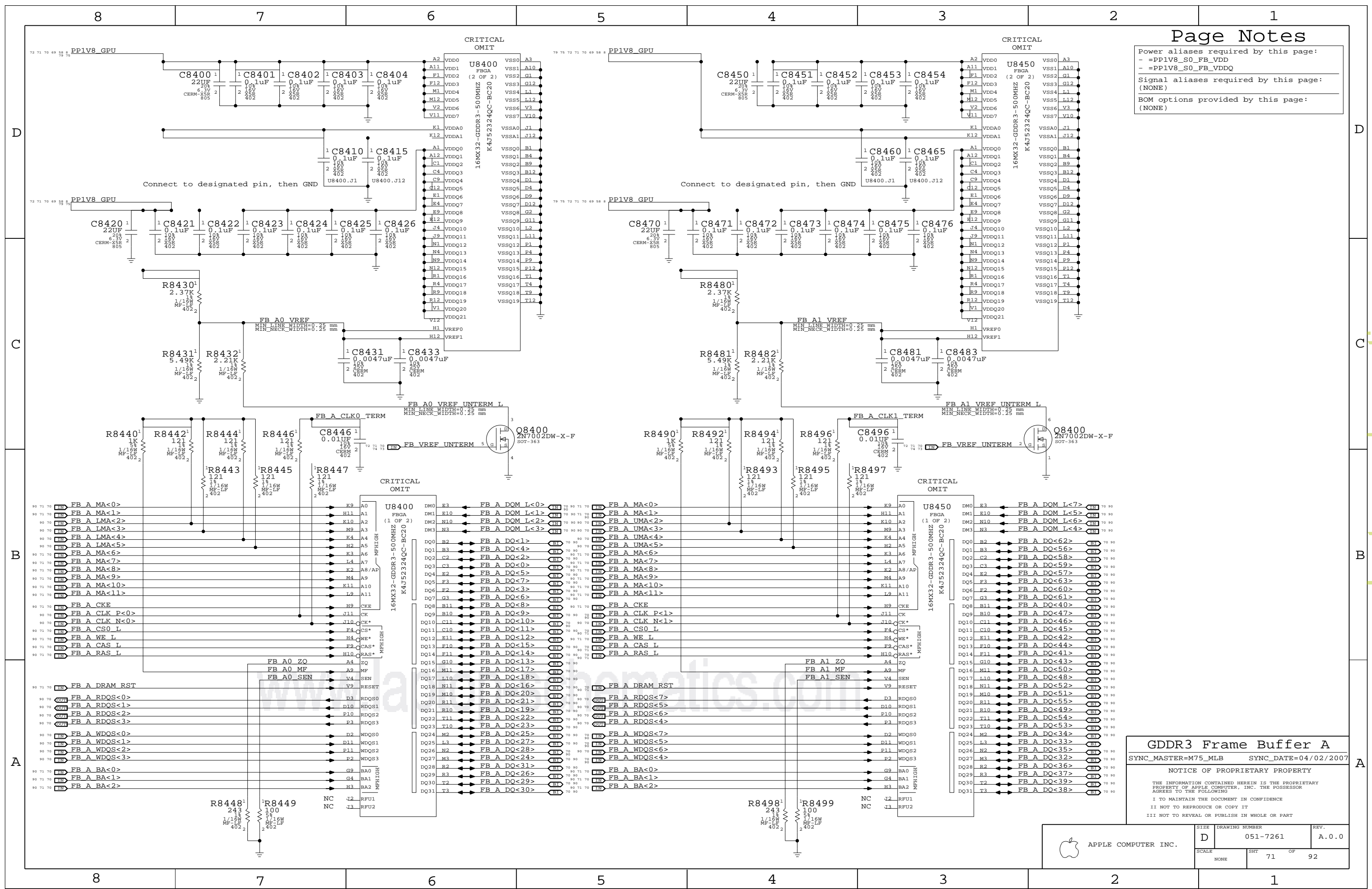


NV G84M Frame Buffer I/F
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	70	92	

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A
SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	71	92	

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Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B
SYNC_MASTER=M75_MLB SYNC_DATE=04/02/2007

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	72	92	

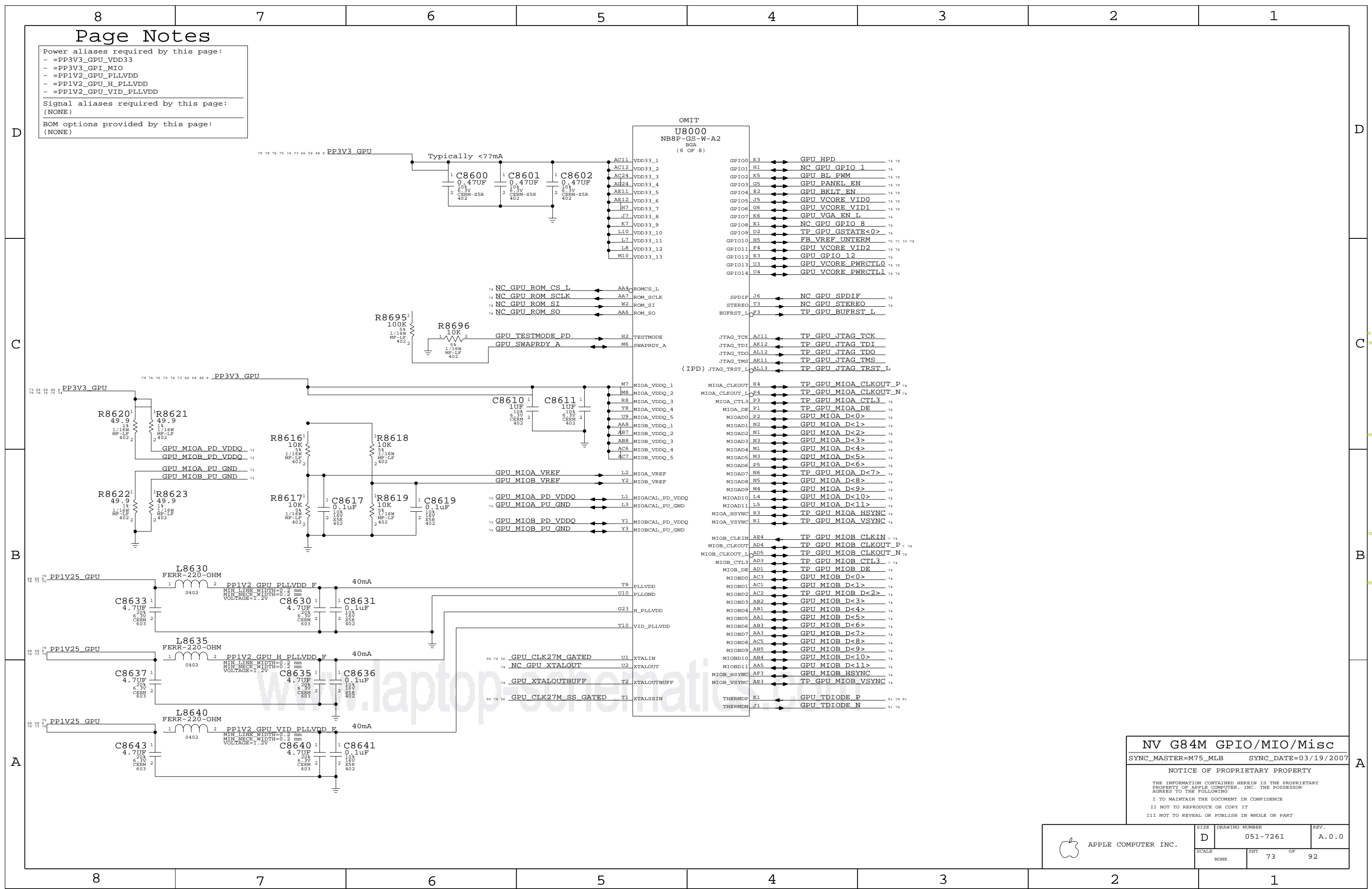
www.laptop-schematics.com

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_VDD33
 - =PP3V3_GPU_MIO
 - =PP1V2_GPU_PLLVDD
 - =PP1V2_GPU_H_PLLVDD
 - =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



NV G84M GPIO/MIO/Misc

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	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	73	92	

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GPIOs

Native Func	GPIOs	Native Func	GPIOs
HPD0	GPU HPD	HPD0	GPU HPD
HPD1	NC GPU GPIO 1	HPD1	NC GPU GPIO 1
LCD0_BL_PWM	GPU BL_PWM	LCD0_BL_PWM	GPU BL_PWM
LCD0_VDD	GPU PANEL_EN	LCD0_VDD	GPU PANEL_EN
LCD0_BL_EN	GPU BKLIT_EN	LCD0_BL_EN	GPU BKLIT_EN
VID0	GPU VCORE VID0	VID0	GPU VCORE VID0
VID1	GPU VCORE VID1	VID1	GPU VCORE VID1
MEM_VID	GPU VGA_EN_L	MEM_VID	GPU VGA_EN_L
THERM	NC GPU GPIO 8	THERM	NC GPU GPIO 8
FAN_PWM	TP GPU GSTATE<0>	FAN_PWM	TP GPU GSTATE<0>
MEM_VREF	FB VREF_UNTERM	MEM_VREF	FB VREF_UNTERM
SLI_SYNC	GPU VCORE VID2	SLI_SYNC	GPU VCORE VID2
AC_DET	GPU GPIO 12	AC_DET	TP GPU GSTATE<1>
PWR_CTL0	GPU VCORE_PWRCTL0	PWR_CTL0	GPU VCORE_PWRCTL0
PWR_CTL1	GPU VCORE_PWRCTL1	PWR_CTL1	GPU VCORE_PWRCTL1

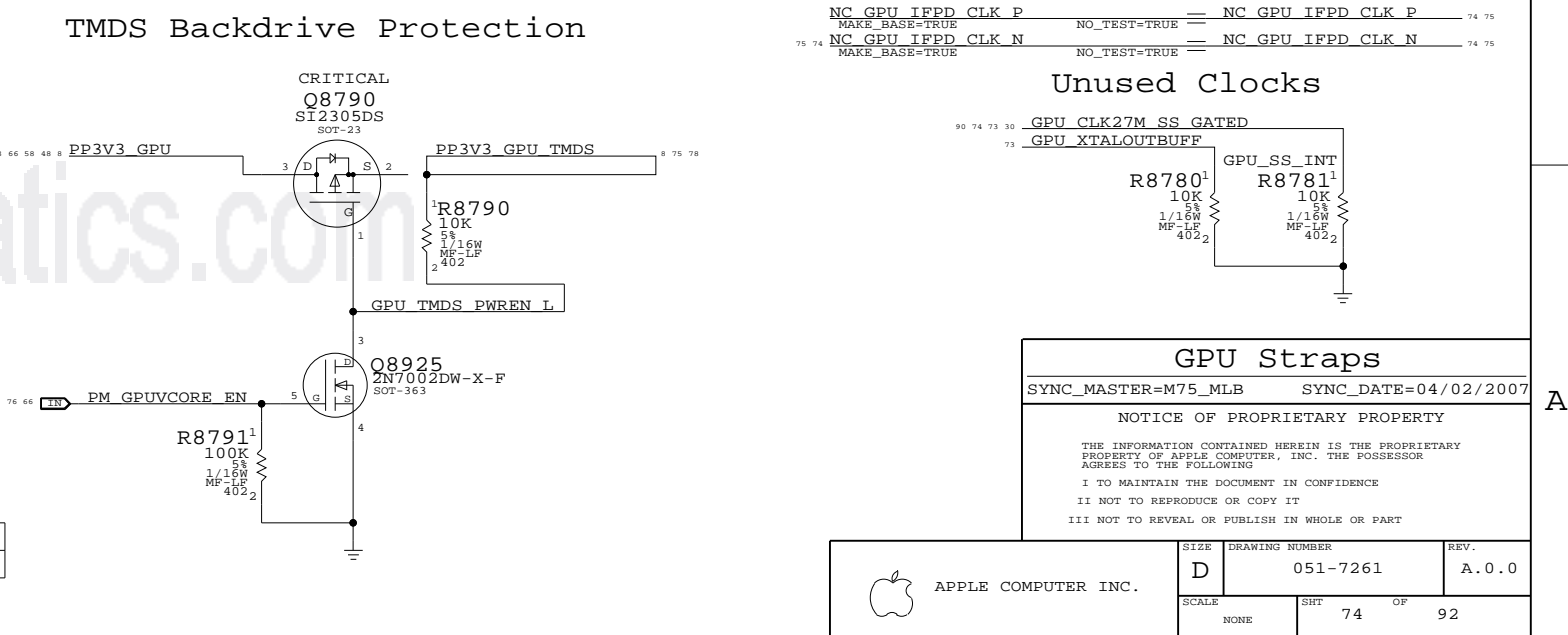
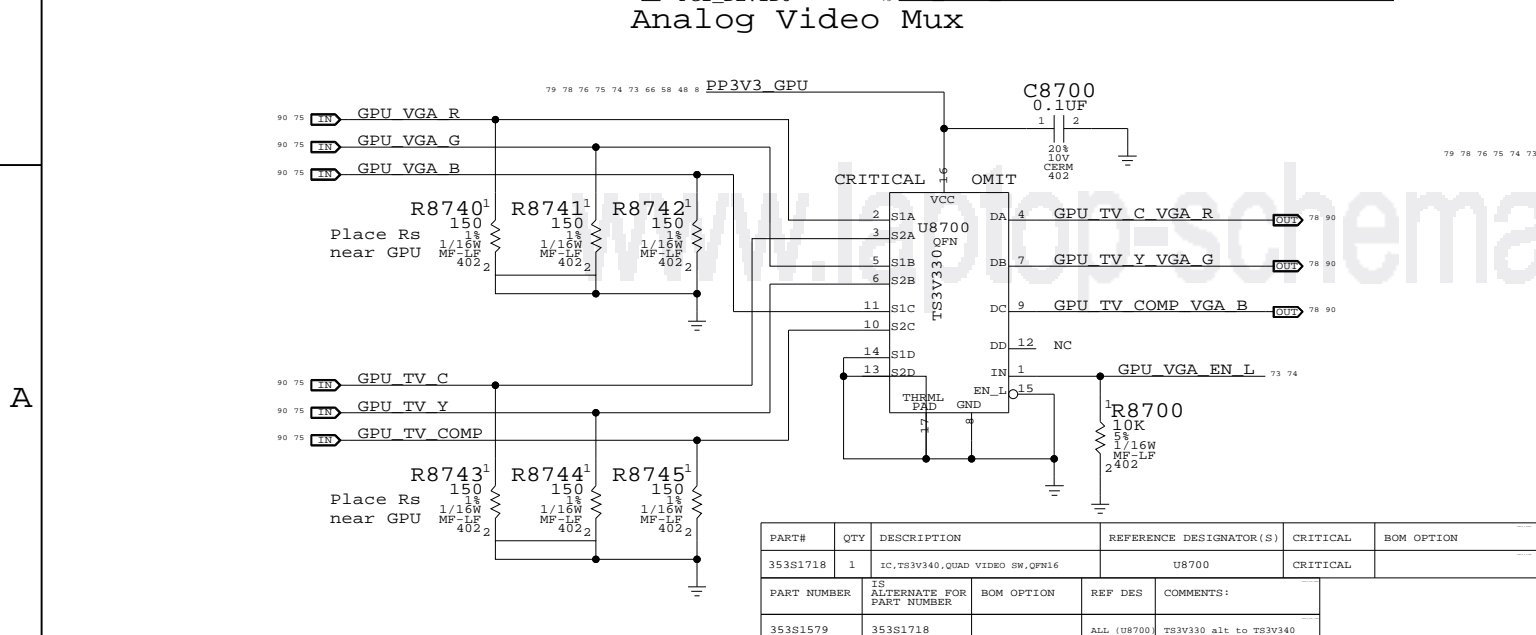
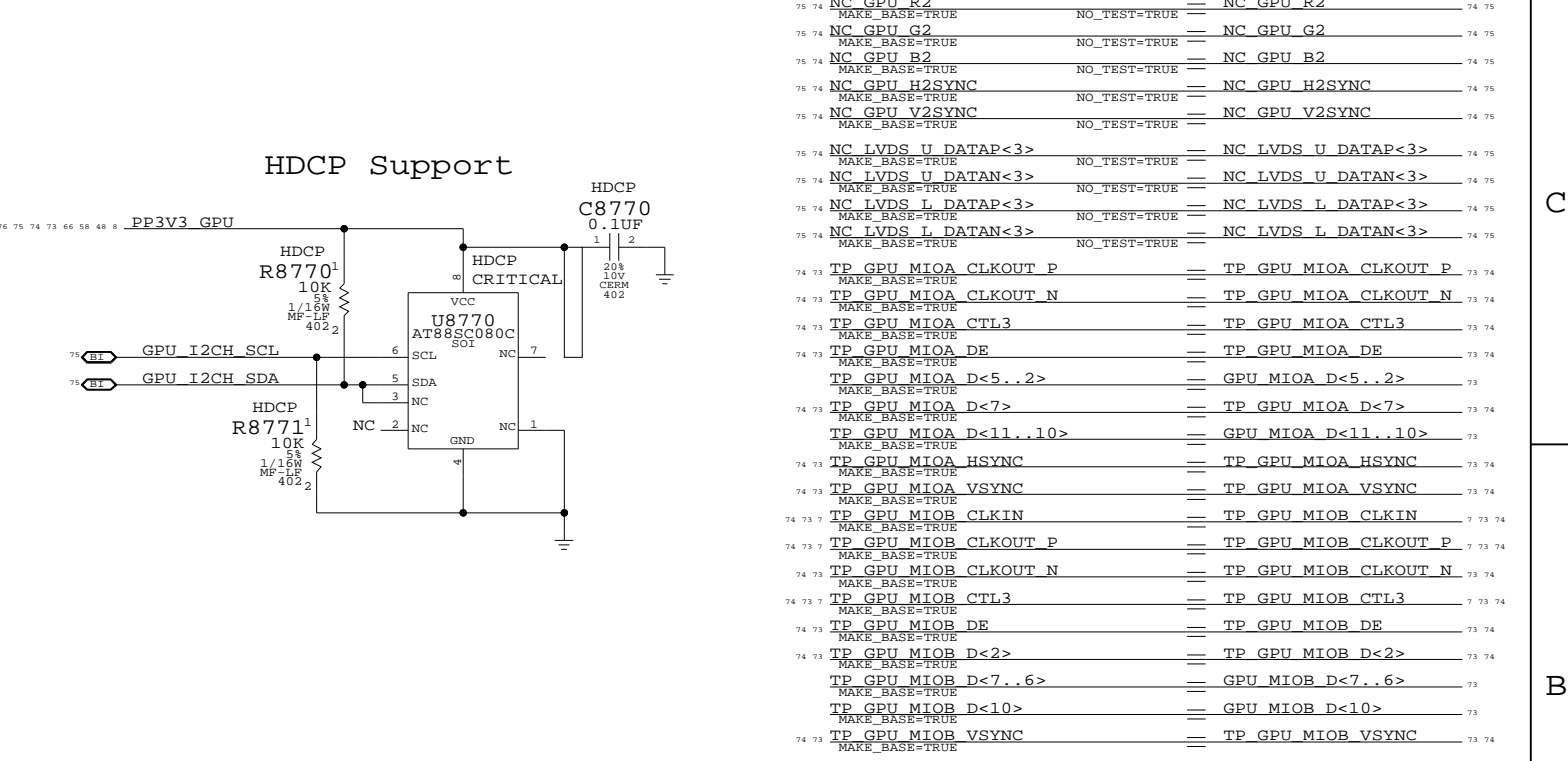
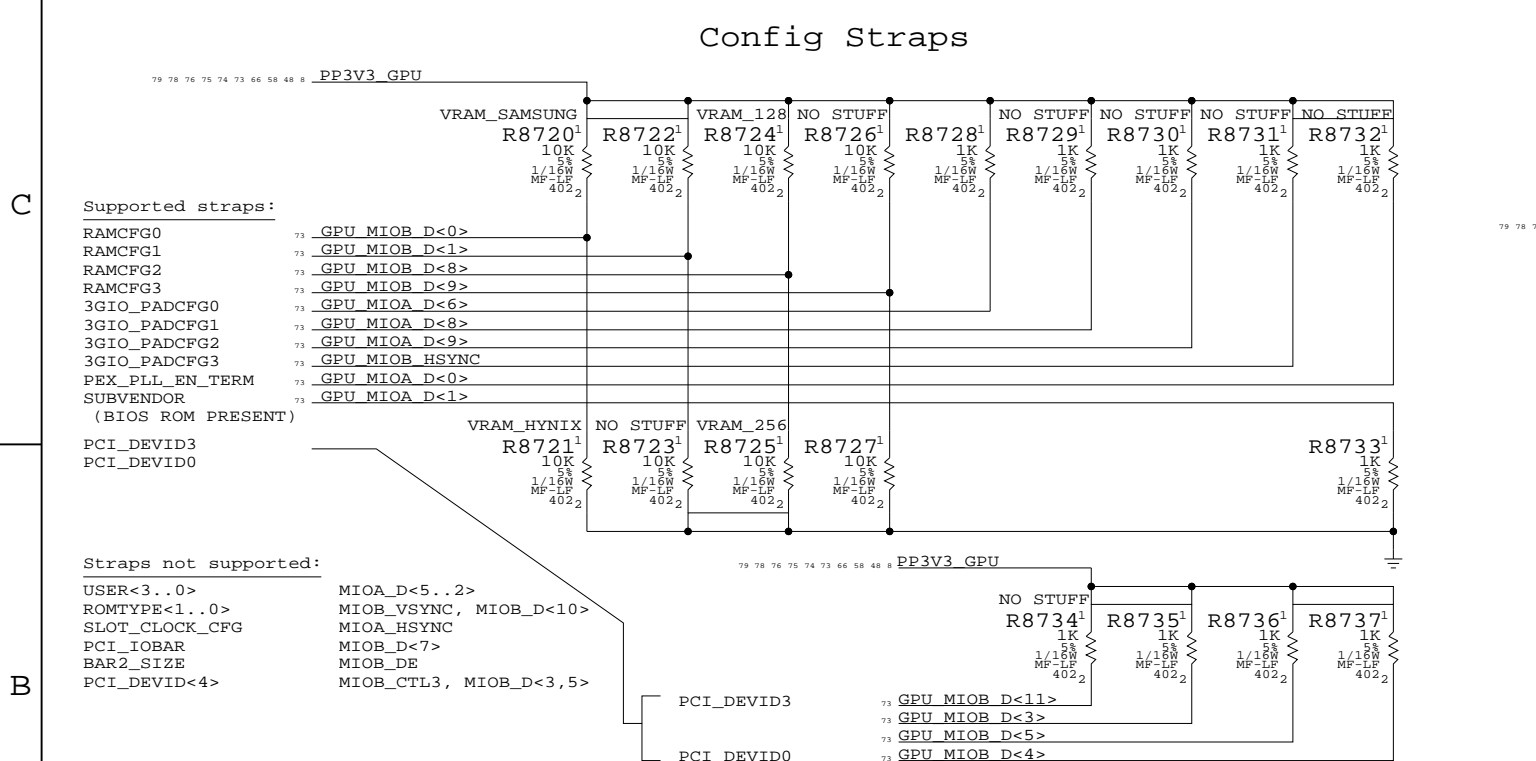
Renamed signals

Renamed signals	Renamed signals	Renamed signals
GPU_CLK27M_GATED	GPU_CLK27M_GATED	GPU_CLK27M_GATED
GPU_CLK27M_SS_GATED	GPU_CLK27M_SS_GATED	GPU_CLK27M_SS_GATED
GPU_TDIODE_P	GPU_TDIODE_P	GPU_TDIODE_P
GPU_TDIODE_N	GPU_TDIODE_N	GPU_TDIODE_N
GPU_DVI_DDC_CLK	GPU_DVI_DDC_CLK	GPU_DVI_DDC_CLK
GPU_DVI_DDC_DATA	GPU_DVI_DDC_DATA	GPU_DVI_DDC_DATA
GPU_PANEL_DDC_CLK	GPU_PANEL_DDC_CLK	GPU_PANEL_DDC_CLK
GPU_PANEL_DDC_DATA	GPU_PANEL_DDC_DATA	GPU_PANEL_DDC_DATA

Unused I2C Buses

Unused I2C Buses	Unused I2C Buses	Unused I2C Buses
NC GPU I2CA_SCL	NC GPU I2CA_SCL	NC GPU I2CA_SCL
NC GPU I2CA_SDA	NC GPU I2CA_SDA	NC GPU I2CA_SDA

I2CS ties into SMBus connection page (I2CS requires pullups even if not used)



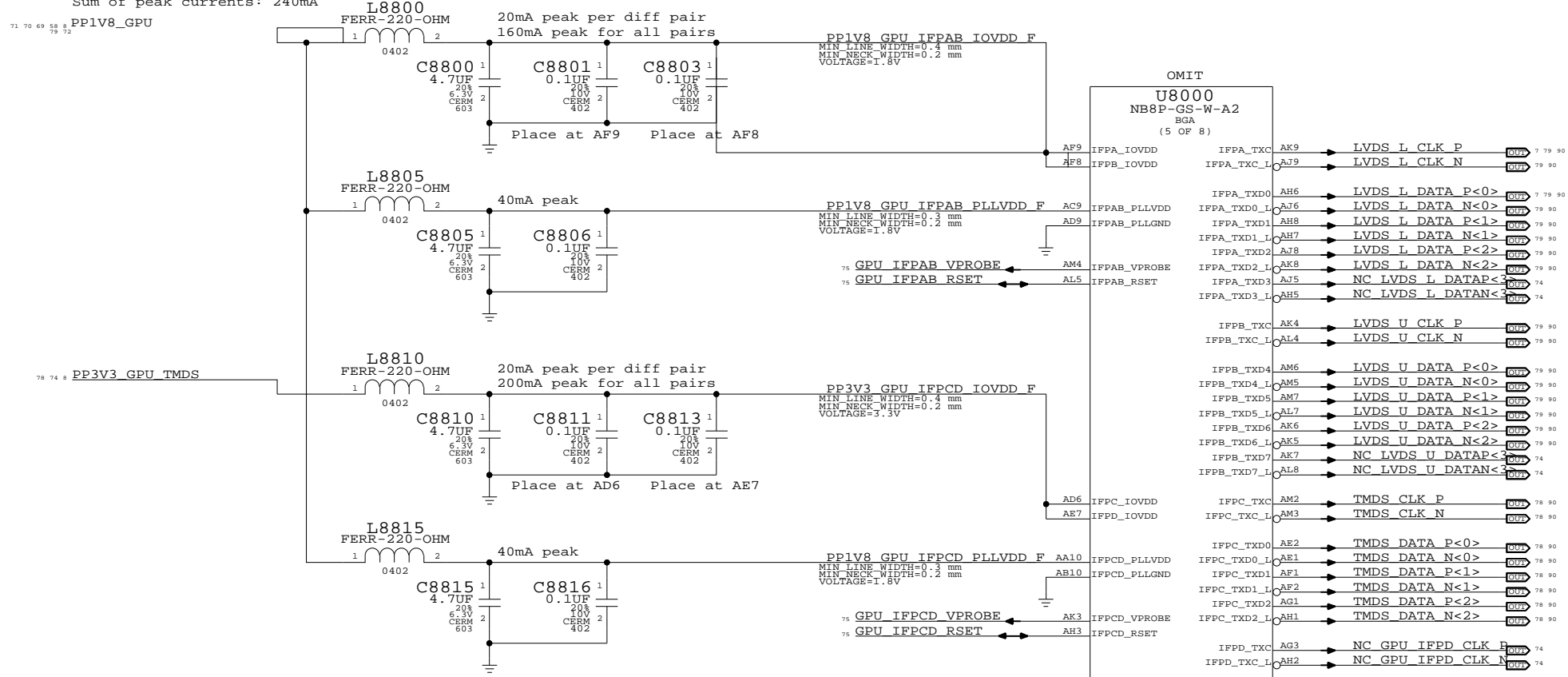
Page Notes

Power aliases required by this page:
 - =PP1V8_GPU_IFPX
 - =PP3V3_GPU_IFPCD_IOVDD
 - =PP3V3_GPU_DAC

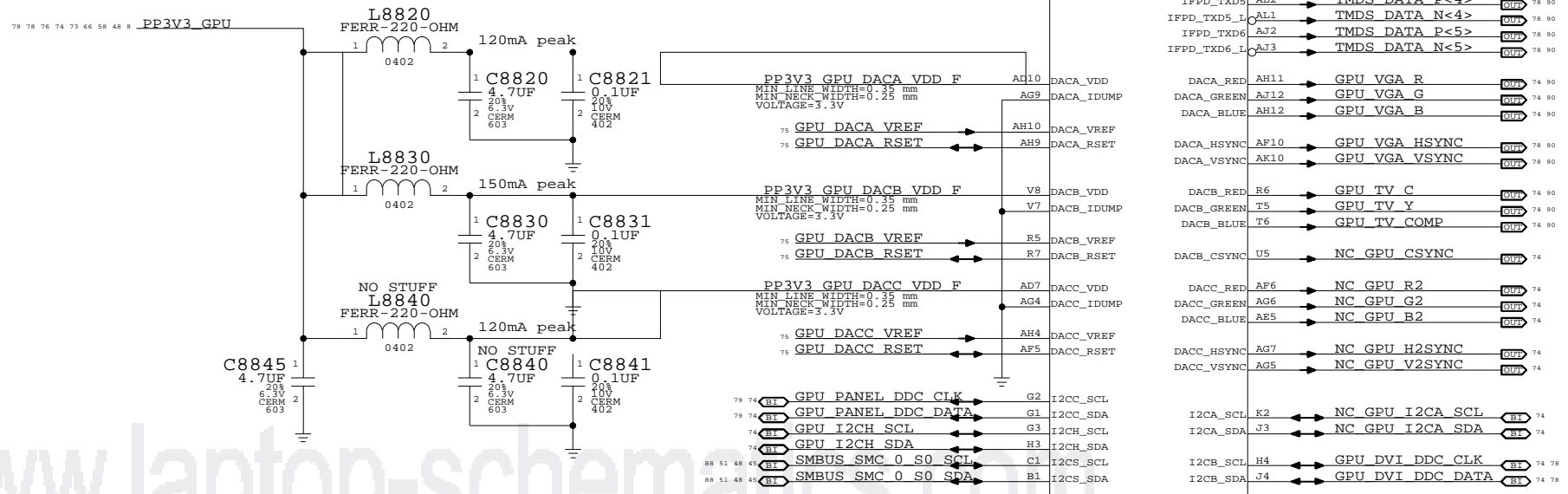
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

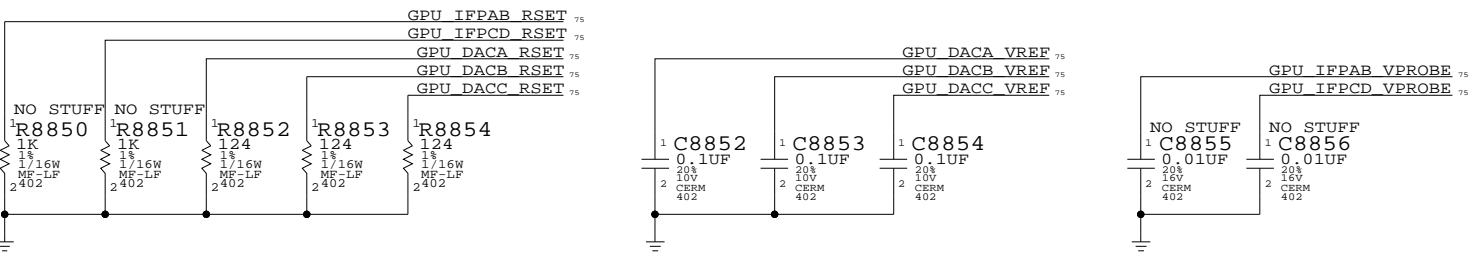
Sum of peak currents: 240mA
 PP1V8_GPU



Sum of peak currents: 390mA
 PP3V3_GPU



I2CS must be pulled up if not used
 I2CS addr fixed at 0x9E,0x9F



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb

NV G84M Video Interfaces
 SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

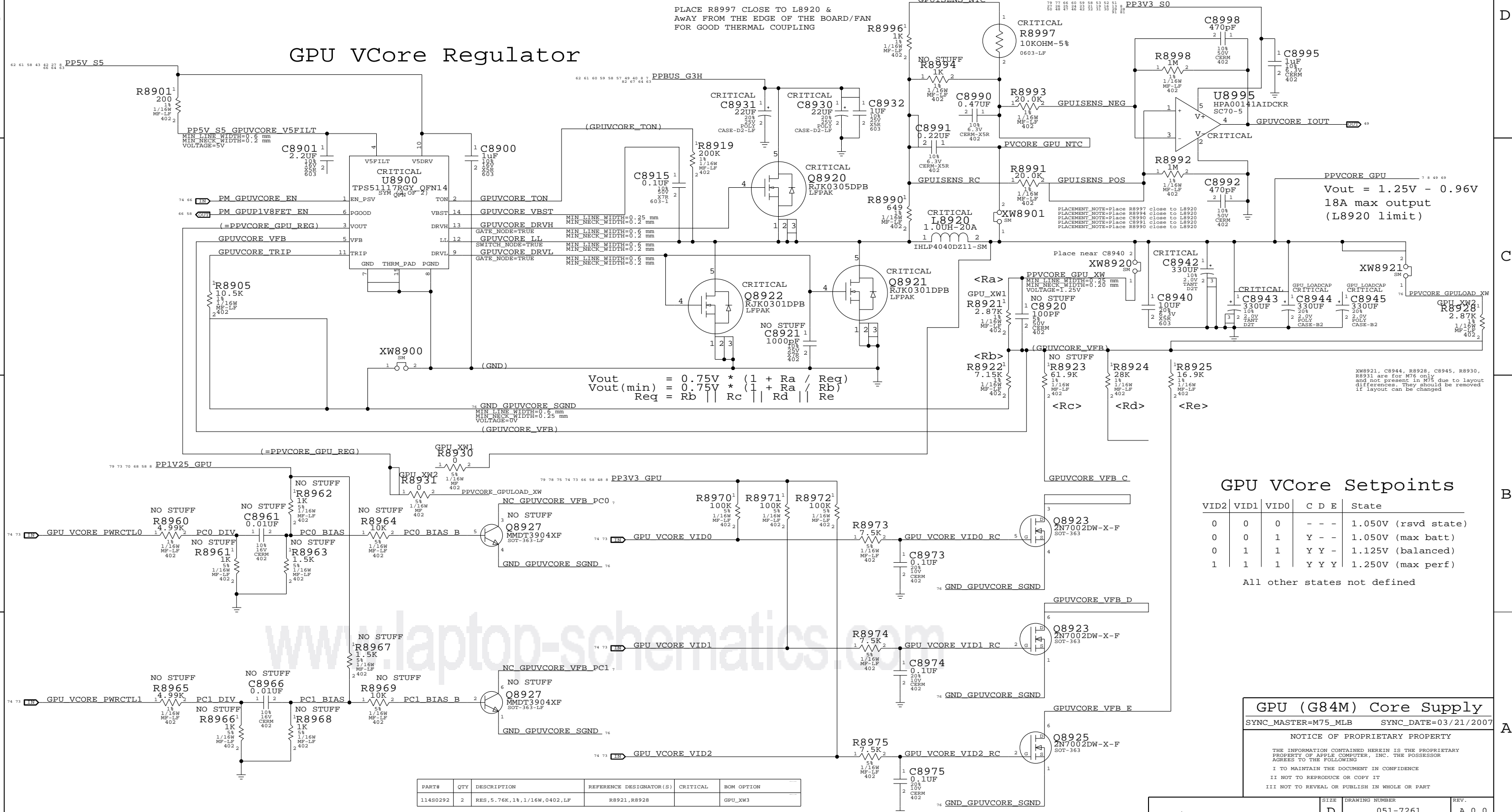
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SCALE	SHT	OF	REV.
NONE	75	92	

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GPU VCore Regulator

GPU VCore Current Sense



PLACE R8997 CLOSE TO L8920 & AWAY FROM THE EDGE OF THE BOARD/FAN FOR GOOD THERMAL COUPLING

$$V_{out} = 0.75V * (1 + R_a / R_{eq})$$

$$V_{out}(\min) = 0.75V * (1 + R_a / R_b)$$

$$R_{eq} = R_b || R_c || R_d || R_e$$

GPU VCore Setpoints

VID2	VID1	VID0	C	D	E	State
0	0	0	-	-	-	1.050V (rsvd state)
0	0	1	Y	-	-	1.050V (max batt)
0	1	1	Y	Y	-	1.125V (balanced)
1	1	1	Y	Y	Y	1.250V (max perf)

All other states not defined

GPU (G84M) Core Supply

SYNC_MASTER=M75_MLB SYNC_DATE=03/21/2007

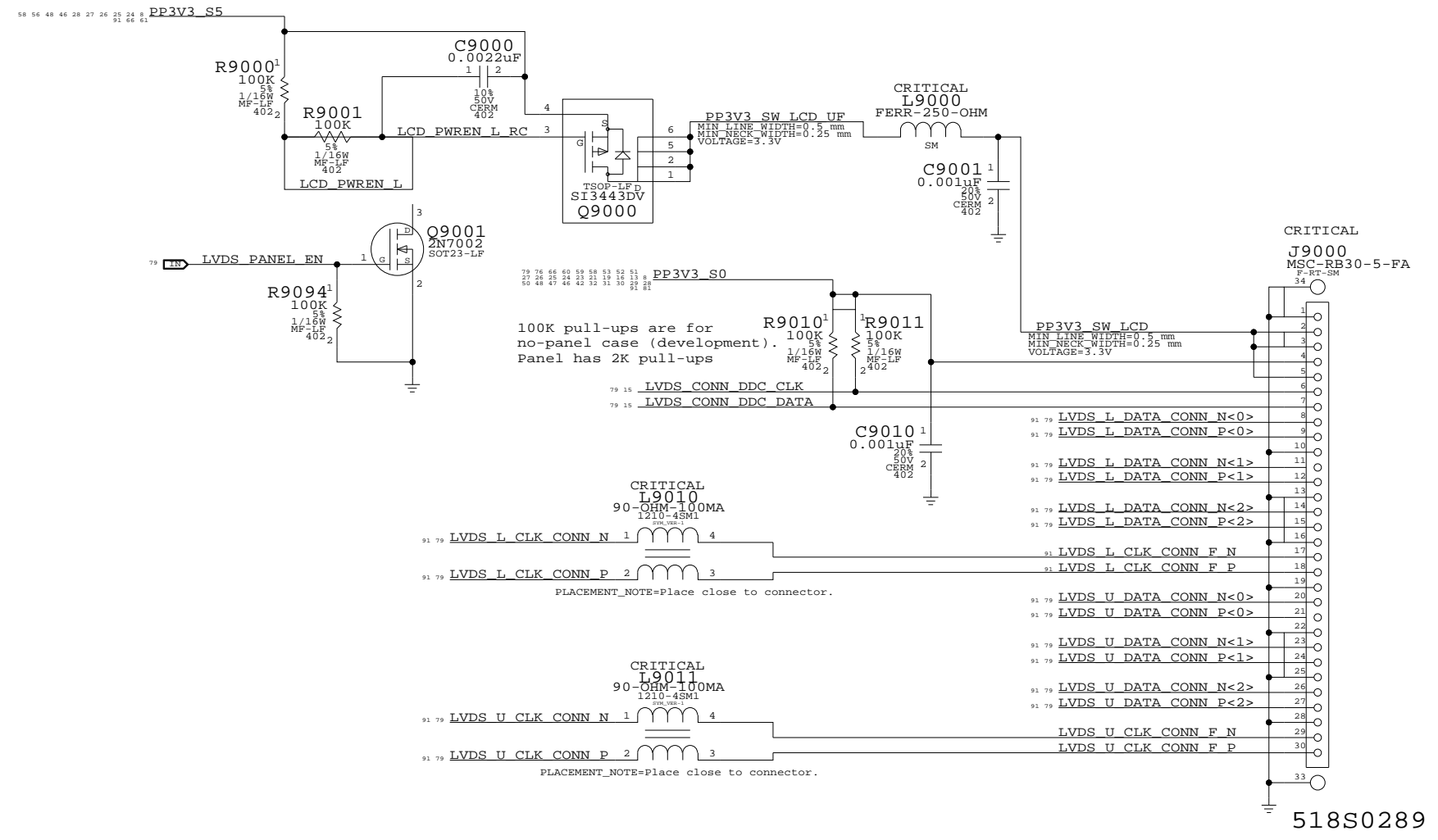
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0292	2	RES, 5.76K, 1%, 1/16W, 0402, LF	R8921, R8928		GPU_XW3

APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-7261	REV.	A.0.0
SCALE	NONE	SHT	76	OF	92

LCD (LVDS) INTERFACE



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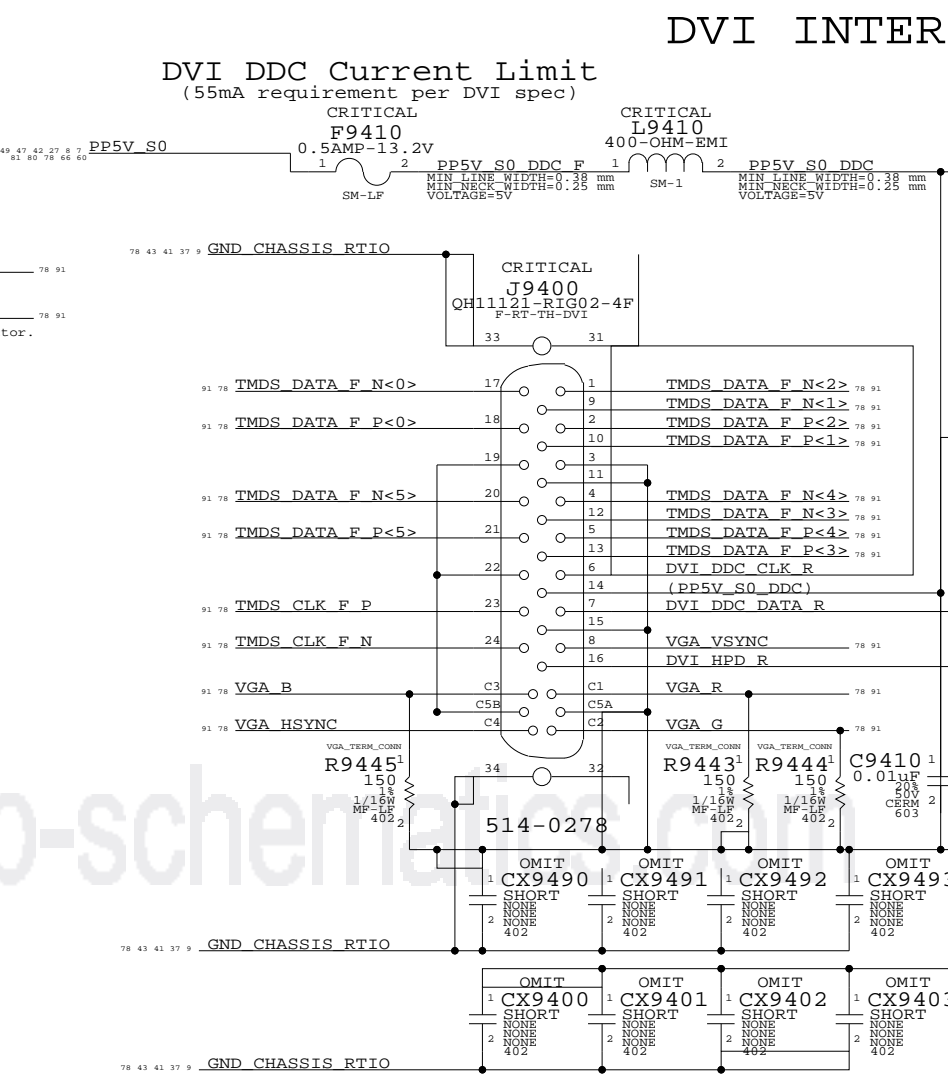
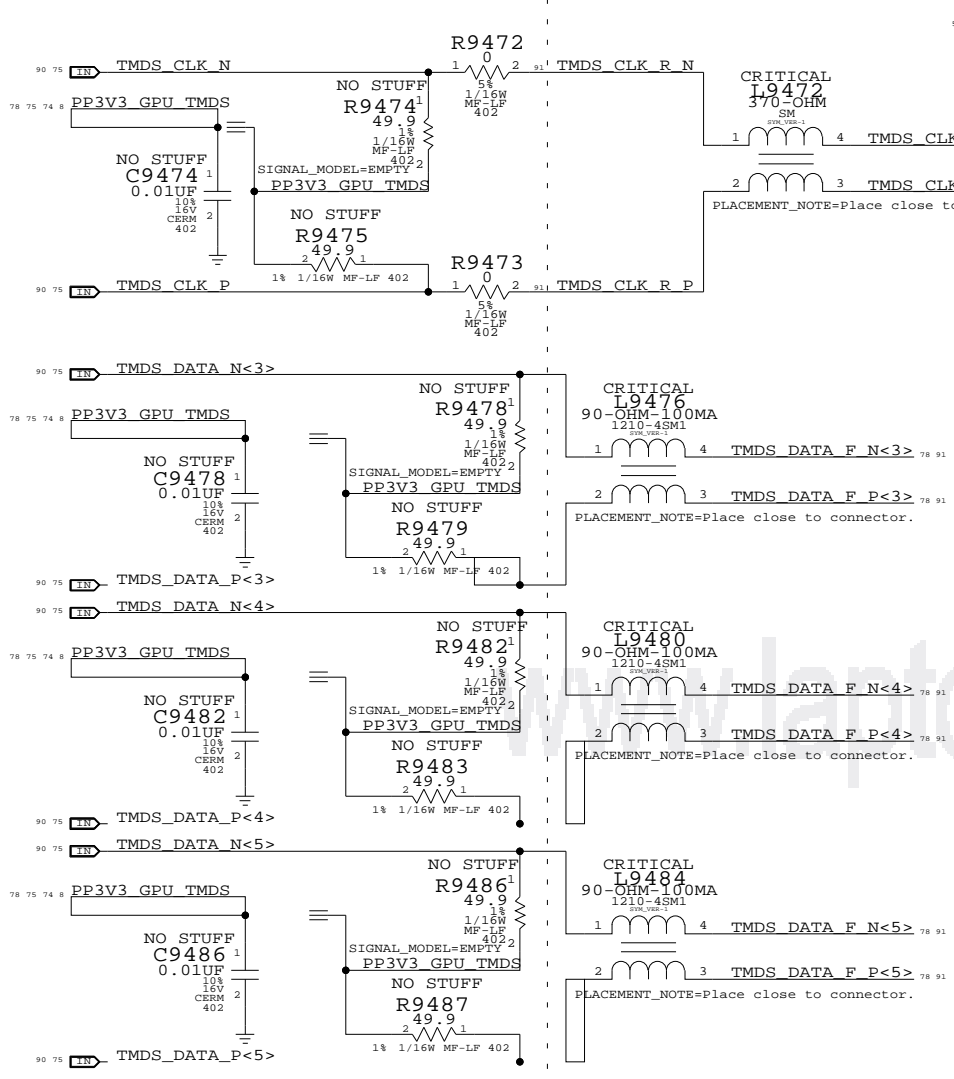
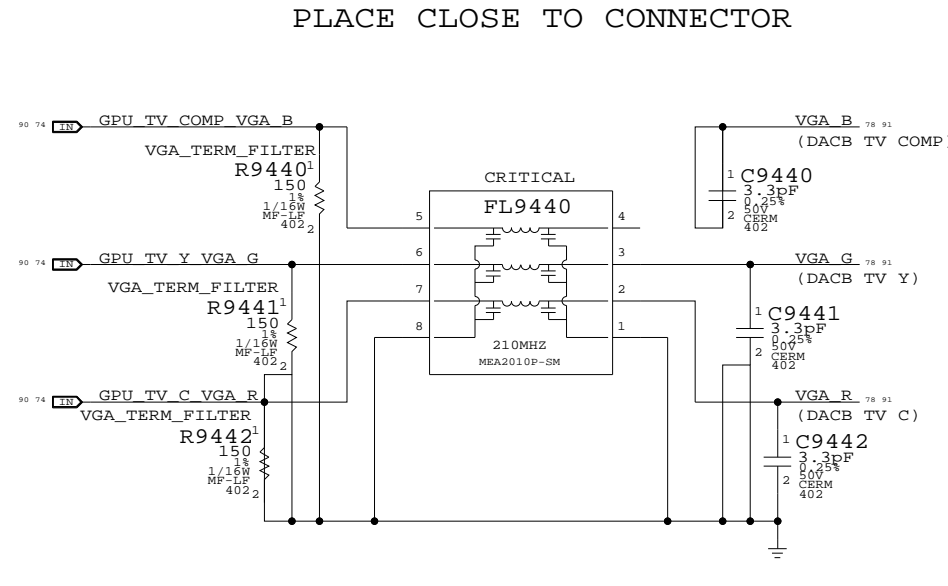
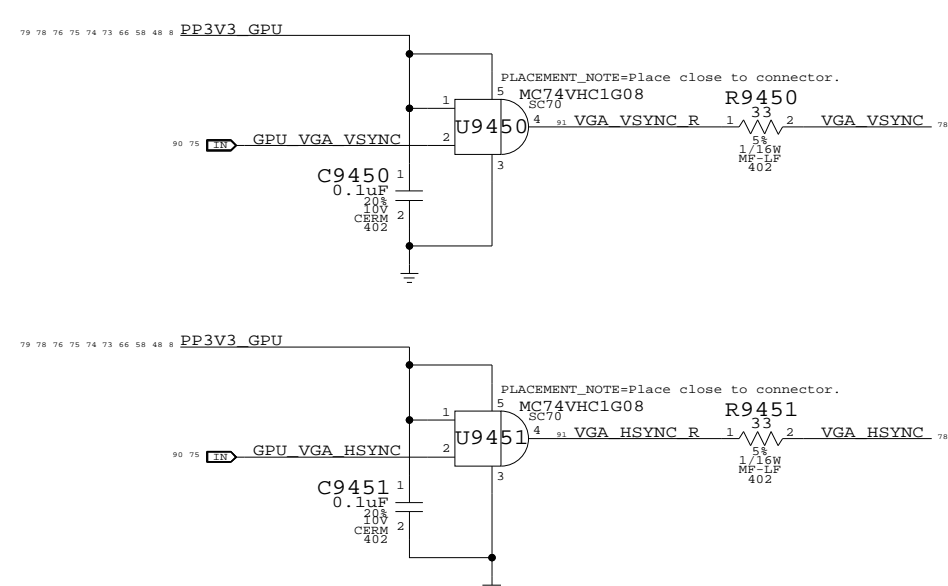
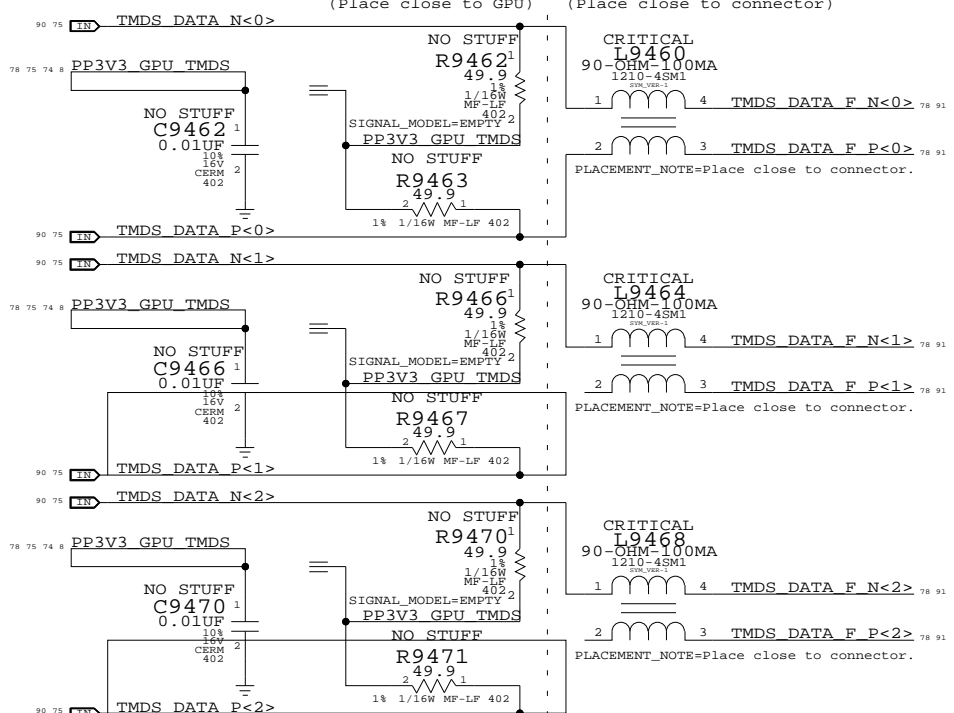
LVDS Display Connector
 SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007
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	SCALE NONE	SHEET 77	OF 92

TMDS Filtering

VGA SYNC Buffers

ANALOG FILTERING PLACE CLOSE TO CONNECTOR



DVI INTERFACE

DVI Display Connector
SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

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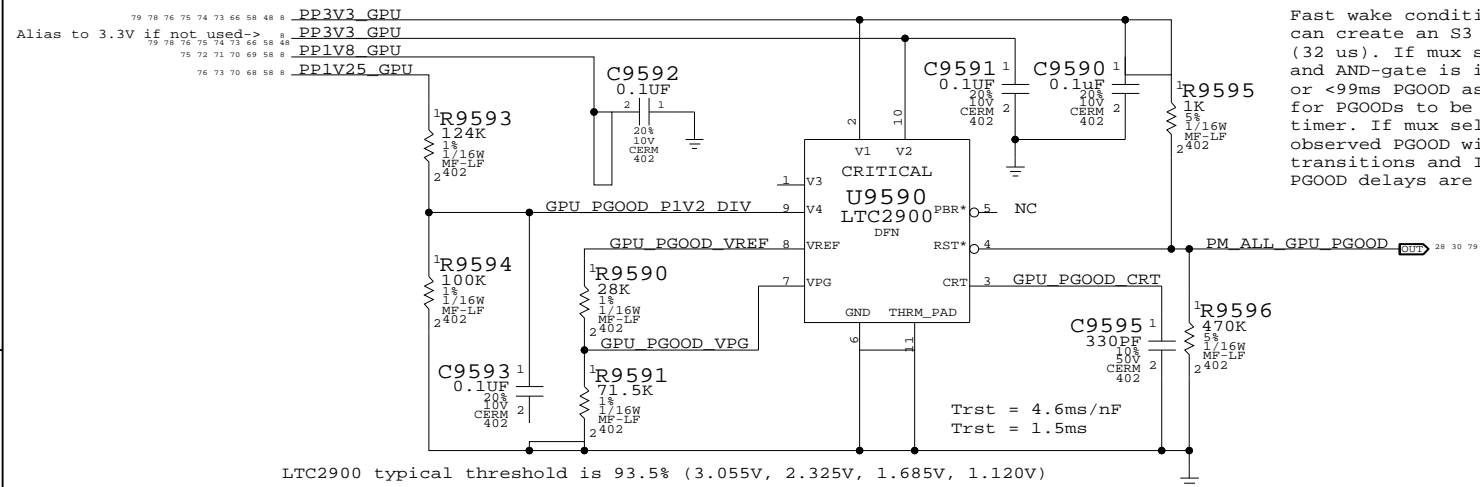
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	78	OF 92

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PGOOD Monitor for GPU Rails

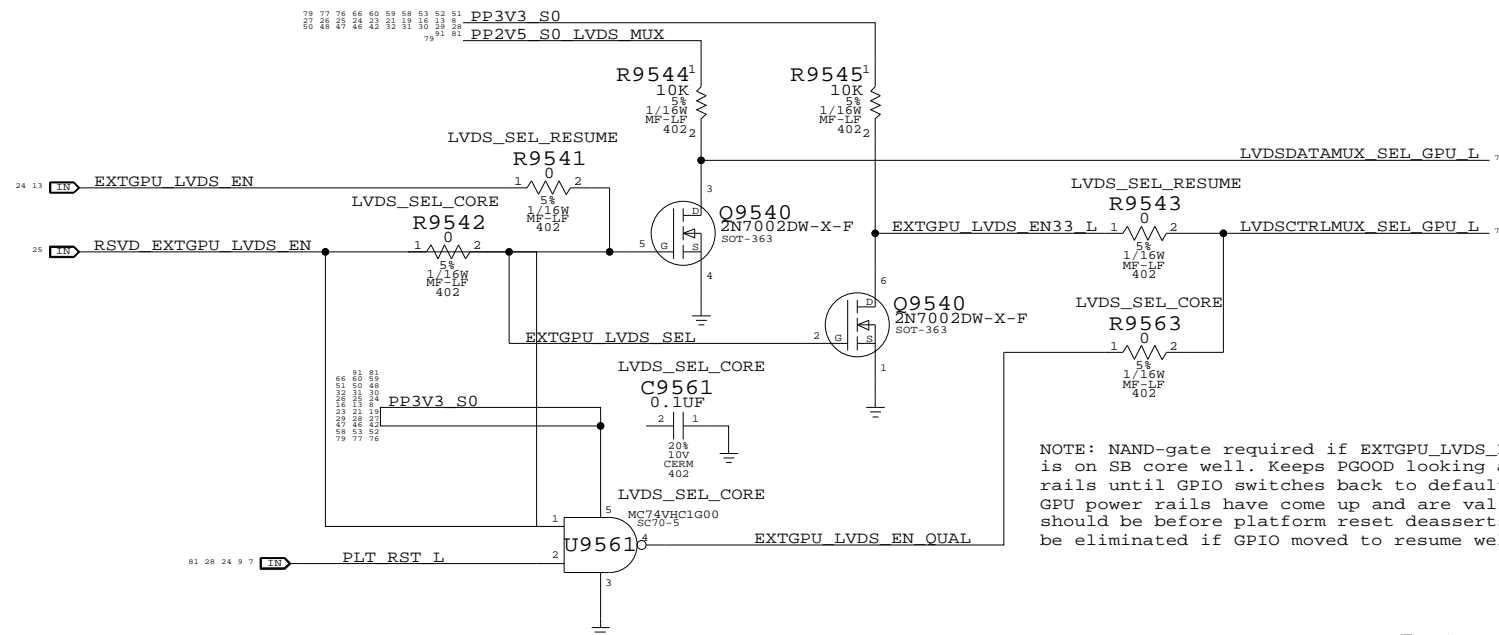
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

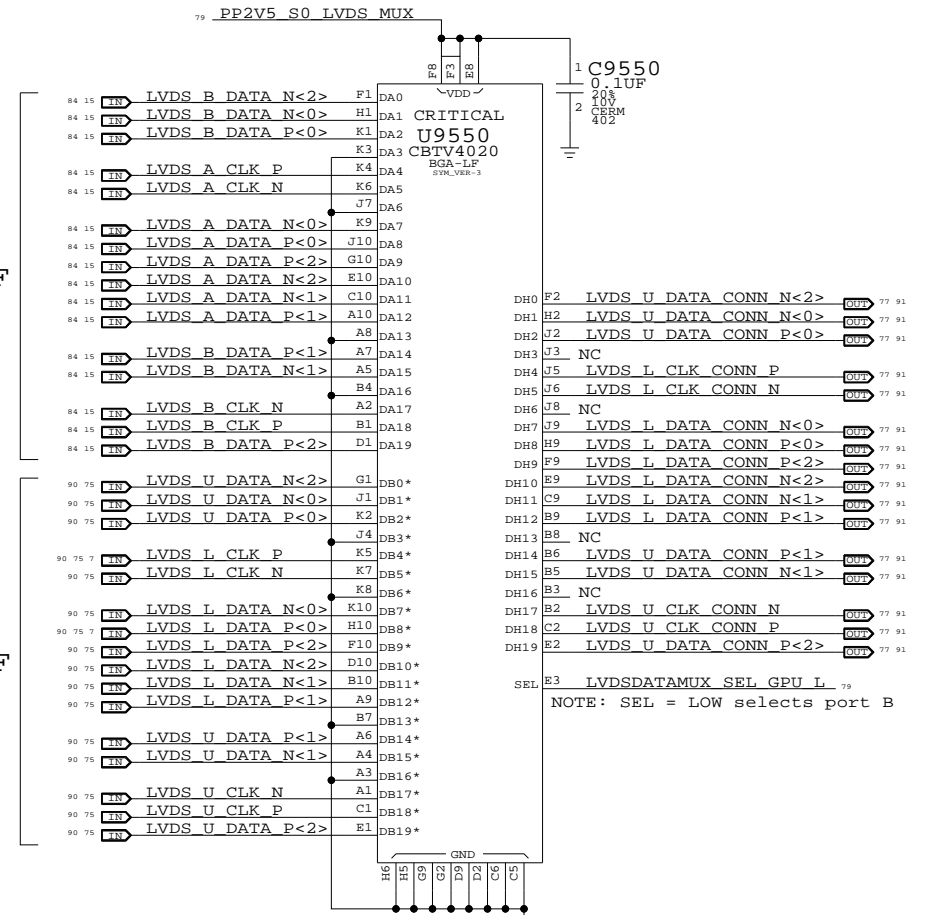
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

Mux Select Conditioning



NOTE: NAND-gate required if EXTGPU_LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

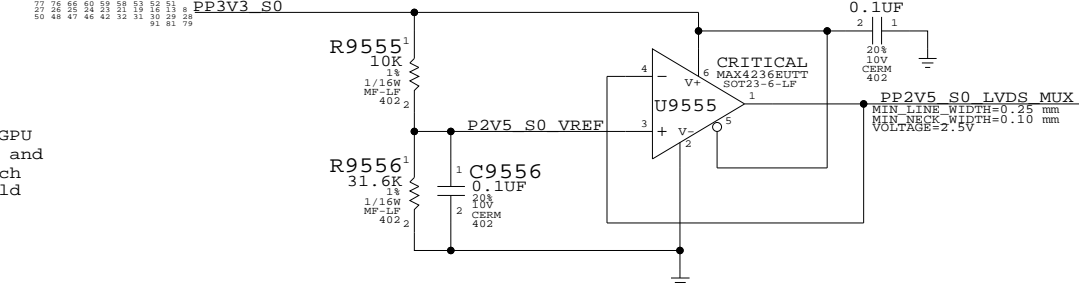
LVDS I/F Mux



NB LVDS I/F

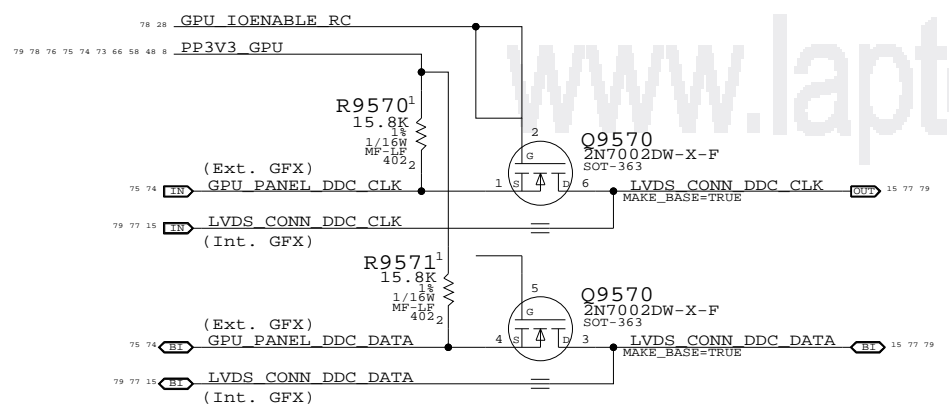
GPU LVDS I/F

LVDS Data Mux Power Supply

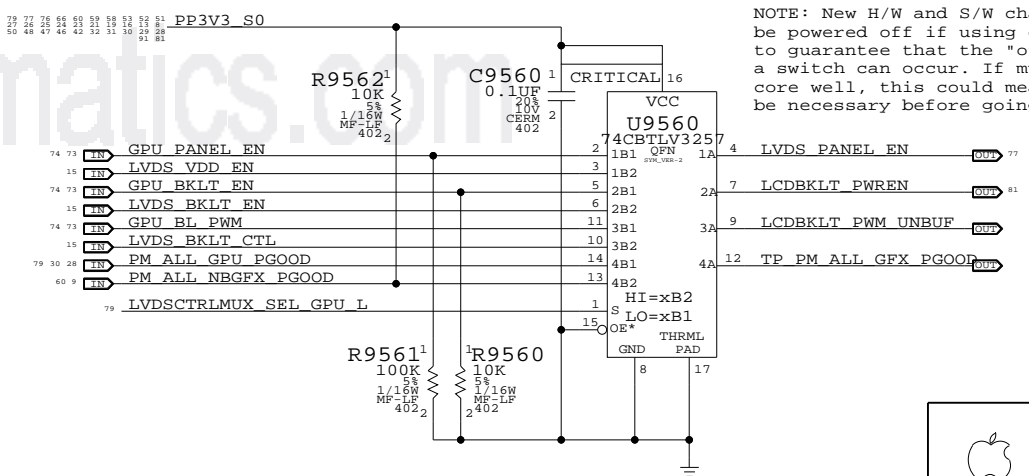


NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

GPU DDC Pass FETs



Panel/Backlight Control Mux



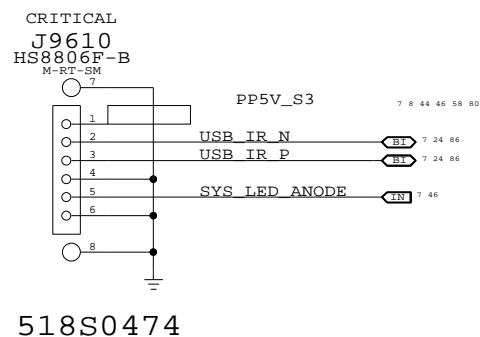
LVDS Interface Mux

SYNC_MASTER=M75_MLB SYNC_DATE=03/19/2007

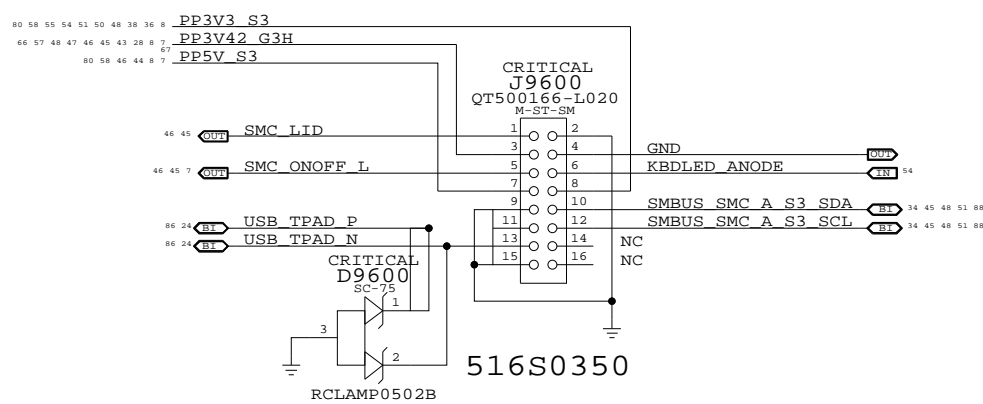
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SCALE	SHT	79	OF 92
NONE			

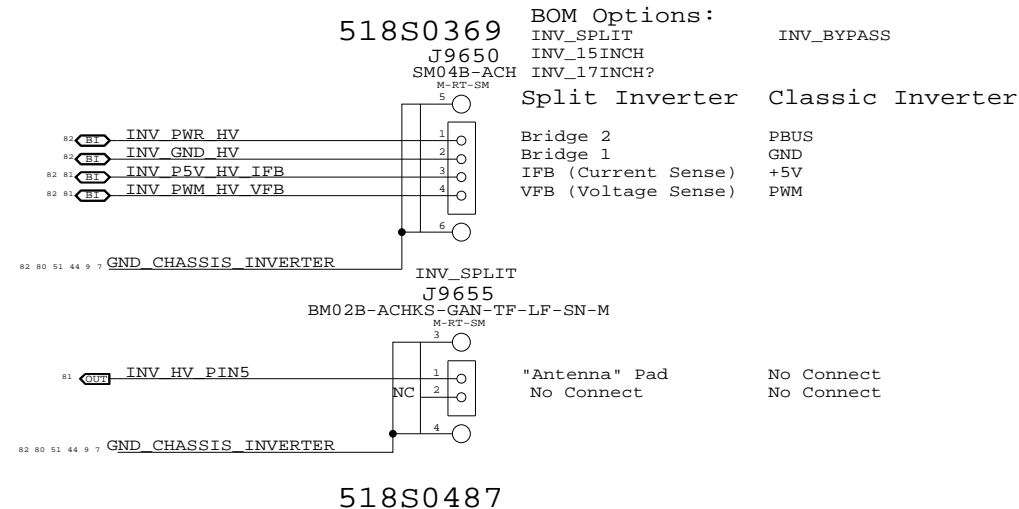
IR & Sleep LED Connector



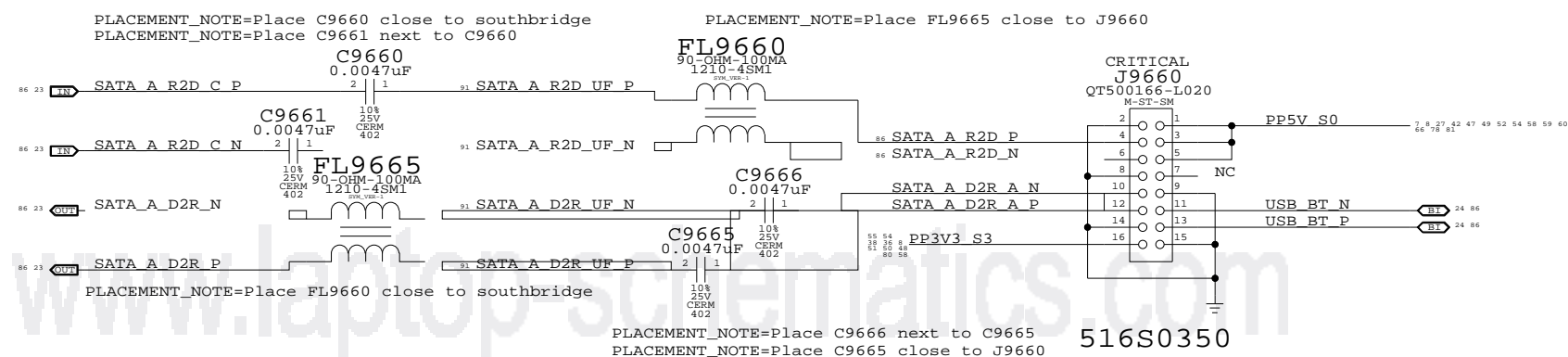
Top-Case Connector



Inverter Connectors



Bluetooth (M13P) & SATA HDD Flex Connector



M76 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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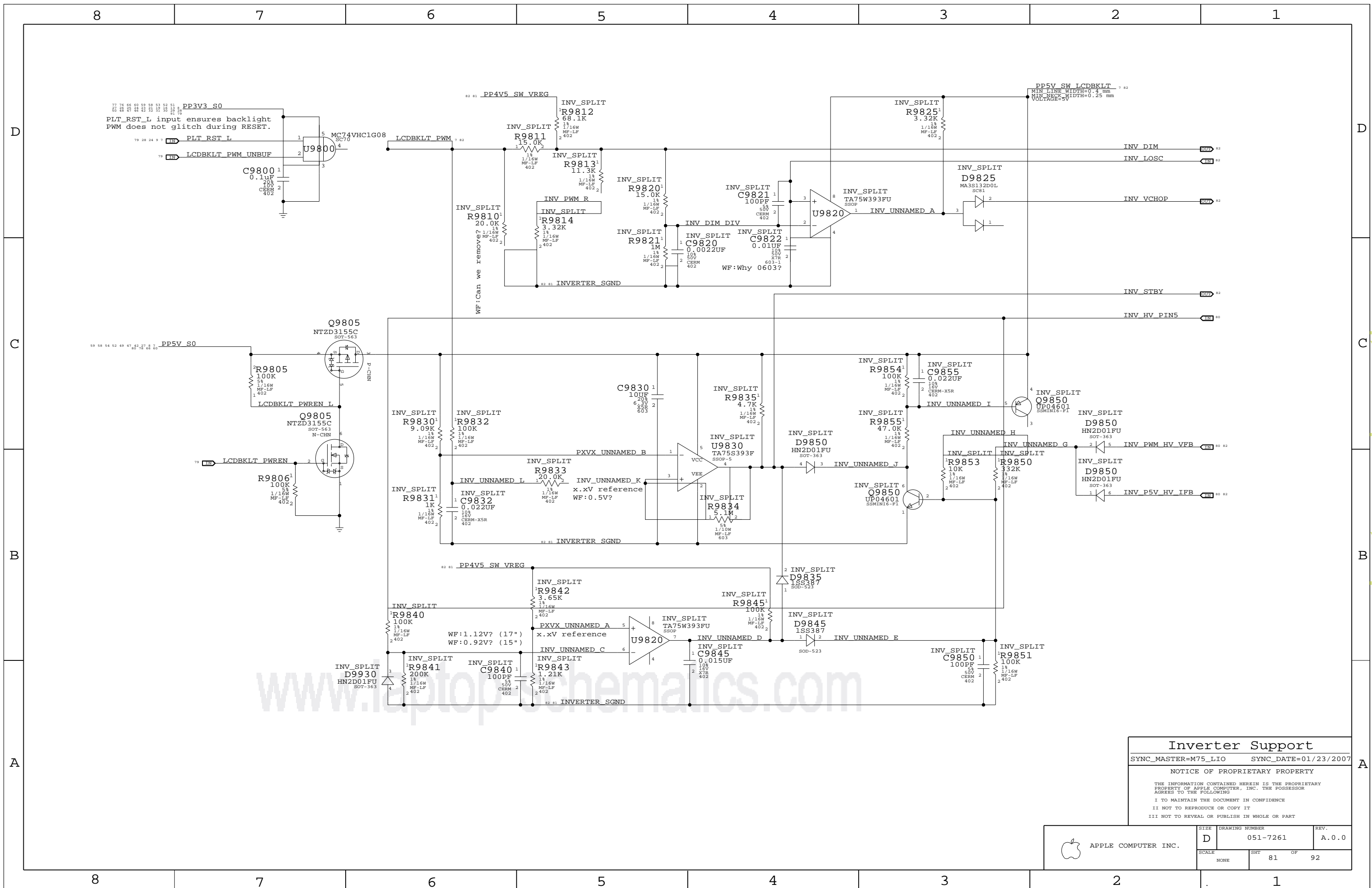
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SCALE	SHT 80 OF 92		
NONE			



Inverter Support

SYNC_MASTER=M75_LIO SYNC_DATE=01/23/2007

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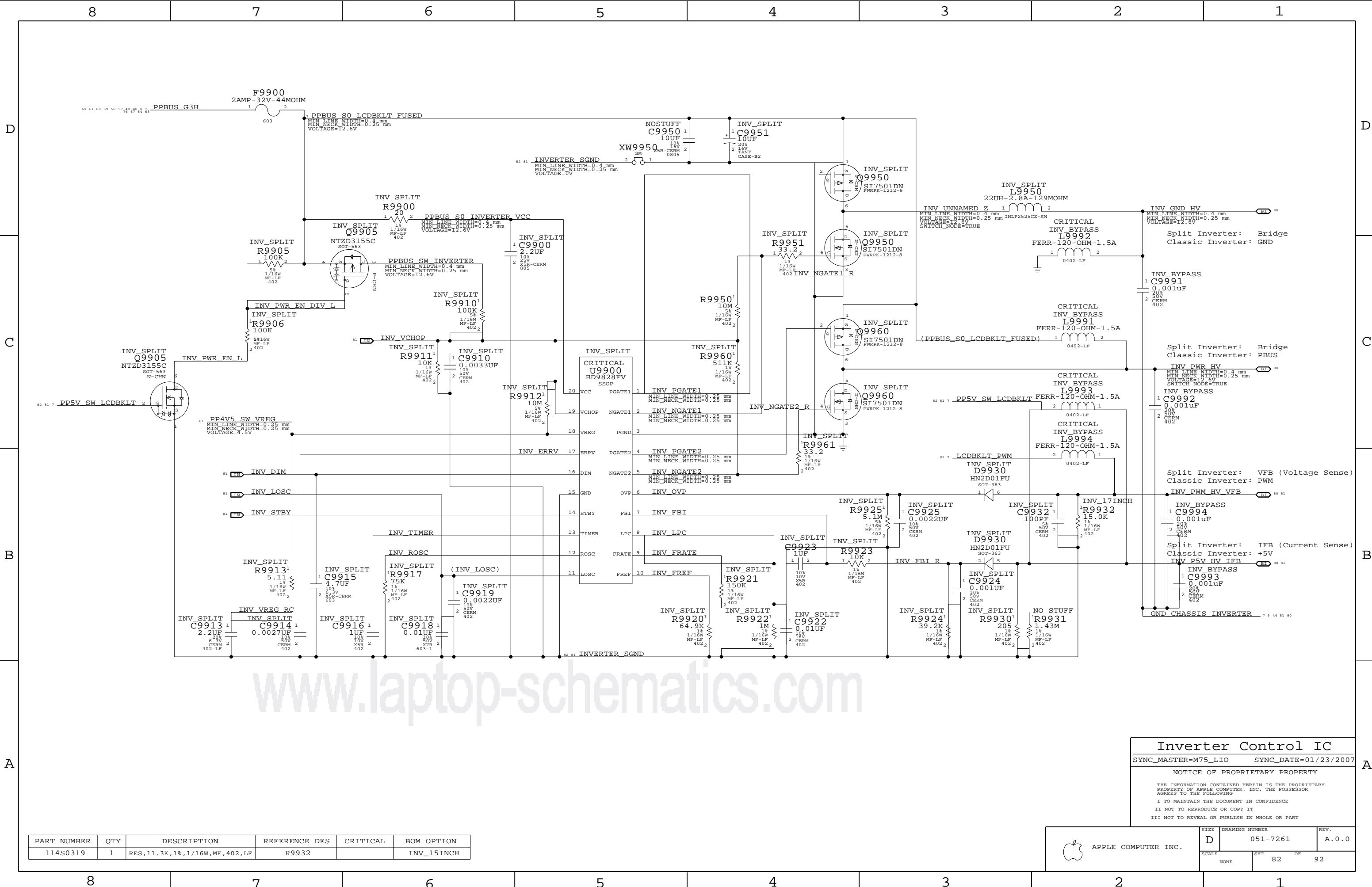
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. A.0.0
	SCALE NONE	SHEET 81	OF 92

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Inverter Control IC

SYNC_MASTER=M75_LIO SYNC_DATE=01/23/2007

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0319	1	RES, 11.3K, 1%, 1/16W, MF, 402, LF	R9932		INV_15INCH

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	92
NONE	82		

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BRQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 59
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FRGM_SB	CPU_55S		CPU INTR	10 23
CPU_FRGM_SB	CPU_55S		CPU NMI	10 23
CPU_FRGM_SB	CPU_55S		CPU A20M L	10 23
CPU_FRGM_SB	CPU_55S		CPU DPSTP L	7 10 23
CPU_FRGM_SB	CPU_55S		CPU IGNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FRGM_SB	CPU_55S		CPU SMI L	10 23
CPU_FRGM_SB	CPU_55S		CPU STPCLK L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TEST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_1000	CLK_FSB_1000	CLK_FSB	XDP CLK P	13 29 30 88
(FSB_CPURST_L)	CLK_FSB_1000	CLK_FSB	XDP CLK N	13 29 30 88
CPU_55S	CPU_55S	CPU_ITP	XDP CPURST L	13
CPU_55S	CPU_2T01		CPU VID<6..0>	11 12
CPU_55S	CPU_2T01		IMVP6 VID<6..0>	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 59
CPU_27P4S	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	59
CPU_27P4S	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	59

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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APPLE COMPUTER INC.

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D	051-7261	A.0.0
SCALE	SHT	OF
NONE	83	92

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
 CRT & TVDAC signal single-ended impedance varies by location:
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.
 - 50-ohm +/- 15% from first to second termination resistor.
 - 55-ohm +/- 15% from second termination resistor to connector.
 CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0>
	PCIE_100D	PCIE	PEG R2D N<15..0>
	PCIE_100D	PCIE	PEG R2D C P<15..0>
	PCIE_100D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0>
	PCIE_100D	PCIE	PEG D2R N<15..0>
	PCIE_100D	PCIE	PEG D2R C P<15..0>
	PCIE_100D	PCIE	PEG D2R C N<15..0>
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>
	DMI_100D	DMI	DMI N2S N<3..0>
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>
	DMI_100D	DMI	DMI S2N N<3..0>
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0>
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0>
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>
LVDS_IBG		LVDS	LVDS IBG
CRT_TVO_IREF		CRT	CRT TVO IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R
TV_A_DAC	CRT_50S	TVDAC	TV A DAC
TV_B_DAC	CRT_50S	TVDAC	TV B DAC
TV_C_DAC	CRT_50S	TVDAC	TV C DAC

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NB Constraints

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	84	92	

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM*-style wildcards!
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM CLK N<2..0>	16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM CLK N<5..3>	16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<4..3>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<3..2>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	17 32

Memory Constraints
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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3 L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDIOW L 23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDACK L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDREO 23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D C P 23 80
SATA_100D	SATA	SATA	SATA_A_R2D C N 23 80
SATA_100D	SATA	SATA	SATA_A_R2D P 80
SATA_100D	SATA	SATA	SATA_A_R2D N 80
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R P 23 80
SATA_100D	SATA	SATA	SATA_A_D2R N 23 80
SATA_100D	SATA	SATA	SATA_A_D2R C P 80
SATA_100D	SATA	SATA	SATA_A_D2R C N 80
SATA_B_R2D	SATA_100D	SATA	TP_SATA_B_R2DP 23 42
SATA_100D	SATA	SATA	TP_SATA_B_R2DN 23 42
SATA_100D	SATA	SATA	SATA_B_R2D P 23 42
SATA_100D	SATA	SATA	SATA_B_R2D N 23 42
SATA_B_D2R	SATA_100D	SATA	TP_SATA_B_D2RP 23 42
SATA_100D	SATA	SATA	TP_SATA_B_D2RN 23 42
SATA_100D	SATA	SATA	SATA_B_D2R C P 23 42
SATA_100D	SATA	SATA	SATA_B_D2R C N 23 42
SATA_C_R2D	SATA_100D	SATA	TP_SATA_C_R2DP 23 42
SATA_100D	SATA	SATA	TP_SATA_C_R2DN 23 42
SATA_100D	SATA	SATA	SATA_C_R2D P 23 42
SATA_100D	SATA	SATA	SATA_C_R2D N 23 42
SATA_C_D2R	SATA_100D	SATA	TP_SATA_C_D2RP 23 42
SATA_100D	SATA	SATA	TP_SATA_C_D2RN 23 42
SATA_100D	SATA	SATA	SATA_C_D2R C P 23 42
SATA_100D	SATA	SATA	SATA_C_D2R C N 23 42
SATA_RBIAS	SATA_55S		SATA_RBIAS 23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 23 34
HDA_55S	HDA	HDA	HDA_BIT_CLK R 23 34
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 23 34
HDA_55S	HDA	HDA	HDA_SYNC R 23 34
HDA_RST_L	HDA_55S	HDA	HDA_RST L 23 34
HDA_55S	HDA	HDA	HDA_RST L R 23 34
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 23 34
HDA_55S	HDA	HDA	HDA_SDIN CODEC 23 34
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 23 34
HDA_55S	HDA	HDA	HDA_SDOUT R 23 34
USB_EXT_A	USB_90D	USB	USB_EXT_A P 24 43
USB_90D	USB	USB	USB_EXT_A N 24 43
USB_90D	USB	USB	USB_EXT_A MUXED P 24 43
USB_90D	USB	USB	USB_EXT_A MUXED N 24 43
USB_MINI	USB_90D	USB	USB_MINI P 24 34
USB_90D	USB	USB	USB_MINI N 24 34
USB_EXT_D	USB_90D	USB	USB_WWAN P 24 44
USB_90D	USB	USB	USB_WWAN N 24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA P 24 44
USB_90D	USB	USB	USB_CAMERA N 24 44
USB_BT	USB_90D	USB	USB_BT P 24 80
USB_90D	USB	USB	USB_BT N 24 80
USB_TPAD	USB_90D	USB	USB_TPAD P 24 80
USB_90D	USB	USB	USB_TPAD N 24 80
USB_IR	USB_90D	USB	USB_IR P 7 24 80
USB_90D	USB	USB	USB_IR N 7 24 80
USB_EXT_B	USB_90D	USB	USB_EXT_B P 24 34
USB_90D	USB	USB	USB_EXT_B N 24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD P 24 34
USB_90D	USB	USB	USB_EXCARD N 24 34
USB_EXTC	USB_90D	USB	USB_EXTC P 24 34
USB_90D	USB	USB	USB_EXTC N 24 34
USB_RBIAS	USB_60S		USB_RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL 25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA 25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA 25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK R 24 56
SPI_55S	SPI	SPI	SPI_SCLK 56
SPI_55S	SPI	SPI	SPI_A_SCLK R 56
SPI_55S	SPI	SPI	SPI_B_SCLK R 56
SPI_SI	SPI_55S	SPI	SPI_SI R 24 56
SPI_55S	SPI	SPI	SPI_SI 56
SPI_55S	SPI	SPI	SPI_A_SI R 56
SPI_55S	SPI	SPI	SPI_B_SI R 56
SPI_SO	SPI_55S	SPI	SPI_SO 24 56
SPI_55S	SPI	SPI	SPI_A_SO R 56
SPI_55S	SPI	SPI	SPI_B_SO R 56
SPI_55S	SPI	SPI	SPI_B_SO R 56
SPI_CE_L0	SPI_55S	SPI	SPI_CE R L<0> 24 56
SPI_55S	SPI	SPI	SPI_CE L<0> 56
SPI_CE_L1	SPI_55S	SPI	SPI_CE R L<1> 56
SPI_55S	SPI	SPI	SPI_CE L<1> 56

SB Constraints (1 of 2)

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	24
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT PIRQD_L	24 38
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L	24
INT_PIRQF_L	PCI_55S	PCI	INT PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C N	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R N	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D P	35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C P	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

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NONE	87	92	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 29 30 88
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 29 30 88
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 88
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 88
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 83 88
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 83 88
CK505_PCIE0	CLK_MED_55S	CLK_MED	CK505_PCIE0_CLK_ITPEN	29 30
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	29 30
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	29 30
CK505_PCIE2	CLK_MED_55S	CLK_MED	TP CK505_PCIE2_CLK	29 30
CK505_PCIE3	CLK_MED_55S	CLK_MED	CK505_PCIE3_CLK	29 30
CK505_PCIE4	CLK_MED_55S	CLK_MED	TP CK505_PCIE4_CLK	29 30
CK505_PCIE5	CLK_MED_55S	CLK_MED	CK505_PCIE5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_CLK27M_SS	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 16 22 29 30 88
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 16 22 29 30 88
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 88 88
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 88 88
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 88
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 88
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 88
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 88
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 88
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 88
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 88
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 88
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 88
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 88
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP_PCIE_CLK100M_SRC7N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 88
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 29 30 88
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 29 30 88
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 29 30 88
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 29 30 88
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 29 30 83 88
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 29 30 83 88
(CK505_PCIE0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCIE2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	30 45
(CK505_PCIE3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTRL	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	7 16 22 29 30 88
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	7 16 22 29 30 88
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_P	9 29 30 88 88
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_GPU_N	9 29 30 88 88
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	24 29 30 88
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	24 29 30 88
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	29 30 34 88
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	29 30 34 88
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	23 29 30 88
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	23 29 30 88
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 29 30 88
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 29 30 88
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29 30 34 88
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29 30 34 88
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	29 30 35 88
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	29 30 35 88

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	34 45 48 51 80
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	34 45 48 51 80
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	45 48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	45 48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	45 48 51 75
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	45 48 51 75
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 45 48 57
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 45 48 57
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	45 48 55
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	45 48 55

Clock & SMC Constraints

SYNC_MASTER=T9_NAME SYNC_DATE=01/25/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	
NONE	88	92	

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
EW_D_CTL	EW_55S	FW	FW LINK<7..0>
EW_D_CTL	EW_55S	FW	FW CTL<1..0>
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW LINK LCLK
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW PHY LCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW LINK PCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW PHY PCLK 38 39
EW_LKON	EW_55S	FW	FW LKON
EW_LKON	EW_55S	FW	FW LKON R
EW_LPS	EW_55S	FW	FW LPS 38 39
EW_LREQ	EW_55S	FW	FW LREQ 38 39
EW_PINT	EW_55S	FW	FW PINT 38 39
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI R
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI
EW_0_TPA	EW_110D	EW_TP	FW PORT0 TPA P 39 41
EW_0_TPA	EW_110D	EW_TP	FW PORT0 TPA N 39 41
EW_0_TPB	EW_110D	EW_TP	FW PORT0 TPB P 39 41
EW_0_TPB	EW_110D	EW_TP	FW PORT0 TPB N 39 41
EW_1_TPA	EW_110D	EW_TP	FW PORT1 TPA P 39 41
EW_1_TPA	EW_110D	EW_TP	FW PORT1 TPA N 39 41
EW_1_TPB	EW_110D	EW_TP	FW PORT1 TPB P 39 41
EW_1_TPB	EW_110D	EW_TP	FW PORT1 TPB N 39 41
Port 2 Not Used			

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FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	A.0.0
SCALE	SHT	OF	REV.
NONE	89	92	

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_A_CLK_P	gDDR3_80D	gDDR3_CLK	FB A CLK P<0>	70 71
FB_B_CLK_P	gDDR3_80D	gDDR3_CLK	FB A CLK N<0>	70 71
FB_A_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A CLK P<1>	70 71
FB_B_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A CLK N<1>	70 71
FB_A_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A MA<1..0>	70 71
FB_B_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A MA<11..6>	70 71
FB_A_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A BA<2..0>	70 71
FB_B_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A RAS L	70 71
FB_A_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A CAS L	70 71
FB_B_CMD	gDDR3_40R50SE	gDDR3_CMD	FB A WE L	70 71
FB_A_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB A CKE	70 71
FB_B_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB A CS0 L	70 71
FB_A_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB A DRAM RST	70 71
FB_B_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB A LMA<5..2>	70 71
FB_A_CMD	gDDR3_50SE	gDDR3_CMD	FB A UMA<5..2>	70 71
FB_B_CMD	gDDR3_50SE	gDDR3_CMD	FB A WDS<0>	70 71
FB_A_WDQS0	gDDR3_50SE	gDDR3_DQS	FB A WDS<1>	70 71
FB_B_WDQS1	gDDR3_50SE	gDDR3_DQS	FB A WDS<2>	70 71
FB_A_WDQS2	gDDR3_50SE	gDDR3_DQS	FB A WDS<3>	70 71
FB_B_WDQS3	gDDR3_50SE	gDDR3_DQS	FB A RDQS<0>	70 71
FB_A_RDQS1	gDDR3_50SE	gDDR3_DQS	FB A RDQS<1>	70 71
FB_B_RDQS2	gDDR3_50SE	gDDR3_DQS	FB A RDQS<2>	70 71
FB_A_RDQS3	gDDR3_50SE	gDDR3_DQS	FB A RDQS<3>	70 71
FB_B_RDQS0	gDDR3_50SE	gDDR3_DQS	FB A DQ<7..0>	70 71
FB_A_DQ_BYTE0	gDDR3_50SE	gDDR3_DATA	FB A DQ<15..8>	70 71
FB_B_DQ_BYTE1	gDDR3_50SE	gDDR3_DATA	FB A DQ<23..16>	70 71
FB_A_DQ_BYTE2	gDDR3_50SE	gDDR3_DATA	FB A DQ<31..24>	70 71
FB_B_DQ_BYTE3	gDDR3_50SE	gDDR3_DATA	FB A DQM L<0>	70 71
FB_A_DQM1	gDDR3_50SE	gDDR3_DATA	FB A DQM L<1>	70 71
FB_B_DQM2	gDDR3_50SE	gDDR3_DATA	FB A DQM L<2>	70 71
FB_A_DQM3	gDDR3_50SE	gDDR3_DATA	FB A WDS<4>	70 71
FB_B_WDQS0	gDDR3_50SE	gDDR3_DQS	FB A WDS<5>	70 71
FB_A_WDQS1	gDDR3_50SE	gDDR3_DQS	FB A WDS<6>	70 71
FB_B_WDQS2	gDDR3_50SE	gDDR3_DQS	FB A WDS<7>	70 71
FB_A_WDQS3	gDDR3_50SE	gDDR3_DQS	FB A RDQS<4>	70 71
FB_B_RDQS0	gDDR3_50SE	gDDR3_DQS	FB A RDQS<5>	70 71
FB_A_RDQS1	gDDR3_50SE	gDDR3_DQS	FB A RDQS<6>	70 71
FB_B_RDQS2	gDDR3_50SE	gDDR3_DQS	FB A RDQS<7>	70 71
FB_A_RDQS3	gDDR3_50SE	gDDR3_DQS	FB A DQ<39..32>	70 71
FB_B_DQ_BYTE0	gDDR3_50SE	gDDR3_DATA	FB A DQ<47..40>	70 71
FB_A_DQ_BYTE1	gDDR3_50SE	gDDR3_DATA	FB A DQ<55..48>	70 71
FB_B_DQ_BYTE2	gDDR3_50SE	gDDR3_DATA	FB A DQ<63..56>	70 71
FB_A_DQ_BYTE3	gDDR3_50SE	gDDR3_DATA	FB A DQM L<4>	70 71
FB_B_DQM1	gDDR3_50SE	gDDR3_DATA	FB A DQM L<5>	70 71
FB_A_DQM2	gDDR3_50SE	gDDR3_DATA	FB A DQM L<6>	70 71
FB_B_DQM3	gDDR3_50SE	gDDR3_DATA	FB A DQM L<7>	70 71

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_C_CLK_P	gDDR3_80D	gDDR3_CLK	FB B CLK P<0>	70 72
FB_D_CLK_P	gDDR3_80D	gDDR3_CLK	FB B CLK N<0>	70 72
FB_C_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B CLK P<1>	70 72
FB_D_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B CLK N<1>	70 72
FB_C_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B MA<1..0>	70 72
FB_D_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B MA<11..6>	70 72
FB_C_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B BA<2..0>	70 72
FB_D_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B RAS L	70 72
FB_C_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B CAS L	70 72
FB_D_CMD	gDDR3_40R50SE	gDDR3_CMD	FB B WE L	70 72
FB_C_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB B CKE	70 72
FB_D_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB B CS0 L	70 72
FB_C_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB B DRAM RST	70 72
FB_D_CMD_PD	gDDR3_40R50SE	gDDR3_CMD	FB B LMA<5..2>	70 72
FB_C_CMD	gDDR3_50SE	gDDR3_CMD	FB B UMA<5..2>	70 72
FB_D_CMD	gDDR3_50SE	gDDR3_CMD	FB B WDS<0>	70 72
FB_C_WDQS0	gDDR3_50SE	gDDR3_DQS	FB B WDS<1>	70 72
FB_D_WDQS1	gDDR3_50SE	gDDR3_DQS	FB B WDS<2>	70 72
FB_C_WDQS2	gDDR3_50SE	gDDR3_DQS	FB B WDS<3>	70 72
FB_D_WDQS3	gDDR3_50SE	gDDR3_DQS	FB B RDQS<0>	70 72
FB_C_RDQS1	gDDR3_50SE	gDDR3_DQS	FB B RDQS<1>	70 72
FB_D_RDQS2	gDDR3_50SE	gDDR3_DQS	FB B RDQS<2>	70 72
FB_C_RDQS3	gDDR3_50SE	gDDR3_DQS	FB B RDQS<3>	70 72
FB_D_RDQS0	gDDR3_50SE	gDDR3_DQS	FB B DQ<7..0>	70 72
FB_C_DQ_BYTE0	gDDR3_50SE	gDDR3_DATA	FB B DQ<15..8>	70 72
FB_D_DQ_BYTE1	gDDR3_50SE	gDDR3_DATA	FB B DQ<23..16>	70 72
FB_C_DQ_BYTE2	gDDR3_50SE	gDDR3_DATA	FB B DQ<31..24>	70 72
FB_D_DQ_BYTE3	gDDR3_50SE	gDDR3_DATA	FB B DQM L<0>	70 72
FB_C_DQM1	gDDR3_50SE	gDDR3_DATA	FB B DQM L<1>	70 72
FB_D_DQM2	gDDR3_50SE	gDDR3_DATA	FB B DQM L<2>	70 72
FB_C_DQM3	gDDR3_50SE	gDDR3_DATA	FB B DQM L<3>	70 72
FB_D_WDQS0	gDDR3_50SE	gDDR3_DQS	FB B WDS<4>	70 72
FB_C_WDQS1	gDDR3_50SE	gDDR3_DQS	FB B WDS<5>	70 72
FB_D_WDQS2	gDDR3_50SE	gDDR3_DQS	FB B WDS<6>	70 72
FB_C_WDQS3	gDDR3_50SE	gDDR3_DQS	FB B WDS<7>	70 72
FB_D_RDQS0	gDDR3_50SE	gDDR3_DQS	FB B RDQS<4>	70 72
FB_C_RDQS1	gDDR3_50SE	gDDR3_DQS	FB B RDQS<5>	70 72
FB_D_RDQS2	gDDR3_50SE	gDDR3_DQS	FB B RDQS<6>	70 72
FB_C_RDQS3	gDDR3_50SE	gDDR3_DQS	FB B RDQS<7>	70 72
FB_D_DQ_BYTE0	gDDR3_50SE	gDDR3_DATA	FB B DQ<39..32>	70 72
FB_C_DQ_BYTE1	gDDR3_50SE	gDDR3_DATA	FB B DQ<47..40>	70 72
FB_D_DQ_BYTE2	gDDR3_50SE	gDDR3_DATA	FB B DQ<55..48>	70 72
FB_C_DQ_BYTE3	gDDR3_50SE	gDDR3_DATA	FB B DQ<63..56>	70 72
FB_D_DQM0	gDDR3_50SE	gDDR3_DATA	FB B DQM L<4>	70 72
FB_C_DQM1	gDDR3_50SE	gDDR3_DATA	FB B DQM L<5>	70 72
FB_D_DQM2	gDDR3_50SE	gDDR3_DATA	FB B DQM L<6>	70 72
FB_C_DQM3	gDDR3_50SE	gDDR3_DATA	FB B DQM L<7>	70 72

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M	30
	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M_GATED	30 73 74
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M_SS	30
	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M_SS_GATED	30 73 74
	LVDS_100D	LVDS	LVDS L CLK P	75 79
	LVDS_100D	LVDS	LVDS L CLK N	75 79
	LVDS_100D	LVDS	LVDS L DATA P<3..0>	75 79
	LVDS_100D	LVDS	LVDS L DATA N<3..0>	75 79
	LVDS_100D	LVDS	LVDS U CLK P	75 79
	LVDS_100D	LVDS	LVDS U CLK N	75 79
	LVDS_100D	LVDS	LVDS U DATA P<3..0>	75 79
	LVDS_100D	LVDS	LVDS U DATA N<3..0>	75 79
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK P	75 78
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK N	75 78
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA P<5..0>	75 78
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA N<5..0>	75 78
VGA_B_TV_C	VGA_50S	VGA	GPU TV C VGA R	74 78
VGA_G_TV_Y	VGA_50S	VGA	GPU TV Y VGA G	74 78
VGA_B_TV_COMP	VGA_50S	VGA	GPU TV COMP VGA B	74 78
	VGA_50S	VGA	GPU VGA R	74 75
	VGA_50S	VGA	GPU VGA G	74 75
	VGA_50S	VGA	GPU VGA B	74 75
	VGA_50S	VGA	GPU TV C	74 75
	VGA_50S	VGA	GPU TV Y	74 75
	VGA_50S	VGA	GPU TV COMP	74 75
VGA_SYNC	VGA_55S	VGA_SYNC	GPU VGA HSYNC	75 78
VGA_SYNC	VGA_55S	VGA_SYNC	GPU VGA VSYNC	75 78

GPU (G84M) Constraints

SYNC_MASTER=M75_MLB SYNC_DATE=01/26/2007

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S_OVERRIDE	*	VERRIDE	VERRIDE	0.100 MM_OVERRIDE	2.54 MM_OVERRIDE	VERRIDE	VERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4, ISL10			0.100 MM	2.54 MM		

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_DIFF_BGA
LVDS_100D	*	100_DIFF_BGA
TMDS_100D	*	100_DIFF_BGA

SIM Card Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WWAN_SIM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
WWAN_SIM	*	=2:1_SPACING	?

M76 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>
	ENET_100D	ENETCONN	ENETCONN_P<3..0>
	ENET_100D	ENETCONN	ENETCONN_N<3..0>
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_P
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_N
(USB_EXT_A)	USB_90D	USB	USB2_RT_P
(USB_EXT_A)	USB_90D	USB	USB2_RT_N
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_P
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_N
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_VSEN_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	NBCOREISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V25ISNS_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THMSNS_D2_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMD_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_THMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	HSTHMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	REMTHMSNS_DX_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	RSFSTHMSNS_D_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_N
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_P<3..0>
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_N<3..0>
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_P
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_N
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_P<3..0>
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_N<3..0>
	TMDS_100D	TMDS	TMDS_CLK_R_P
	TMDS_100D	TMDS	TMDS_CLK_R_N
	TMDS_100D	TMDS	TMDS_CLK_F_P
	TMDS_100D	TMDS	TMDS_CLK_F_N
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC
	PP1V8_MEM		PP1V8_S3
	PP1V8_MEM		PP1V8_S3
	GND		GND
	SB_POWER		PP3V3_S5
	SB_POWER		PP3V3_S0
	SB_POWER		PP1V5_S0
	WWAN_SIM	WWAN_SIM	WWAN_SIM_CLOCK
	WWAN_SIM	WWAN_SIM	WWAN_SIM_DATA
	ENET_POWER		
	FW_POWER		

M76 Specific Constraints

SYNC_MASTER=M76_MLB SYNC_DATE=02/02/2007

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	SHT	OF	
	91	92	

M75/M76 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2, ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL2, ISL11	Y		0.085 MM			0.140 MM
100_DIFF_BGA	TOP, BOTTOM	Y		0.085 MM			0.140 MM

NOTE: 100_DIFF_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs. Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.

M75/M76 Rule Definitions

SYNC_MASTER=M76_MLB SYNC_DATE=02/02/2007

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NONE	92	92	