

SCHEM, MLB, MBP15

05/24/2007

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| REV | ZONE | ECN | DESCRIPTION OF CHANGE | CK APPD DATE | ENG APPD DATE |
|-----|------|-------|-----------------------|-----------------|------------------|
| A | | 50652 | PRODUCTION RELEASED | 05/24/07 | 07 |

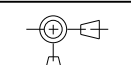
| Page | (.csa) | Contents | Sync | Date |
|------|--------|---------------------------------|------------|------------|
| 1 | 1 | Table of Contents | N/A | N/A |
| 2 | 2 | System Block Diagram | (T9_MLB) | 08/23/2006 |
| 3 | 3 | Power Block Diagram | (T9_MLB) | 08/23/2006 |
| 4 | 4 | Power Block Diagram | N/A | N/A |
| 5 | 5 | BOM Configuration | N/A | N/A |
| 6 | 6 | Revision History | (MASTER) | (MASTER) |
| 7 | 7 | Functional / ICT Test | (MASTER) | (MASTER) |
| 8 | 8 | Power Aliases | (MASTER) | (MASTER) |
| 9 | 9 | Signal Aliases | (T9_MLB) | 08/23/2006 |
| 10 | 10 | CPU FSB | T9_NOME | 03/16/2007 |
| 11 | 11 | CPU Power & Ground | T9_NOME | 03/16/2007 |
| 12 | 12 | CPU Decoupling & VID | M76_MLB | 03/19/2007 |
| 13 | 13 | eXtended Debug Port (XDP) | T9_NOME | 12/12/2006 |
| 14 | 14 | NB CPU Interface | T9_NOME | 03/16/2007 |
| 15 | 15 | NB PEG / Video Interfaces | T9_NOME | 03/16/2007 |
| 16 | 16 | NB Misc Interfaces | T9_NOME | 03/16/2007 |
| 17 | 17 | NB DDR2 Interfaces | T9_NOME | 03/16/2007 |
| 18 | 18 | NB Power 1 | T9_NOME | 03/16/2007 |
| 19 | 19 | NB Power 2 | T9_NOME | 03/16/2007 |
| 20 | 20 | NB Grounds | T9_NOME | 03/16/2007 |
| 21 | 21 | NB Standard Decoupling | T9_NOME | 01/17/2007 |
| 22 | 22 | NB Graphics Decoupling | M76_MLB | 03/12/2007 |
| 23 | 23 | SB Enet, Disk, FSB, LPC | T9_NOME | 03/16/2007 |
| 24 | 24 | SB PCI, PCIE, DMI, USB | T9_NOME | 03/16/2007 |
| 25 | 25 | SB Pwr Mgt, GPIO, Clink | T9_NOME | 03/16/2007 |
| 26 | 26 | SB Power & Ground | T9_NOME | 03/16/2007 |
| 27 | 27 | SB Decoupling | M75_PVT | 05/08/2007 |
| 28 | 28 | SB Misc | (T9_MLB) | 08/24/2006 |
| 29 | 29 | Clock (CK505) | T9_NOME | 03/16/2007 |
| 30 | 30 | Clock Termination | (MASTER) | 08/23/2006 |
| 31 | 31 | DDR2 SO-DIMM Connector A | (M59_SYNC) | 08/24/2006 |
| 32 | 32 | DDR2 SO-DIMM Connector B | (M59_SYNC) | 08/24/2006 |
| 33 | 33 | Memory Active Termination | (T9_NOME) | 11/14/2006 |
| 34 | 34 | Left I/O Board Connector | (M59_SYNC) | 08/24/2006 |
| 35 | 35 | Ethernet (Yukon) | T9_NOME | 03/16/2007 |
| 36 | 36 | Yukon Power Control | T9_NOME | 03/16/2007 |
| 37 | 37 | Ethernet Connector | M76_MLB | 03/19/2007 |
| 38 | 38 | FireWire Link (TSB83AA22) | M76_MLB | 03/19/2007 |
| 39 | 39 | FireWire PHY (TSB83AA22) | M76_MLB | 03/19/2007 |
| 40 | 40 | FireWire Port Power | M76_MLB | 03/19/2007 |
| 41 | 41 | FireWire Ports | M76_MLB | 03/19/2007 |
| 42 | 42 | PATA Connector | (MASTER) | (MASTER) |
| 43 | 43 | External USB Connector | M76_MLB | 03/19/2007 |
| 44 | 44 | Left Clutch Barrel Interconnect | M76_MLB | 03/19/2007 |

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| 45 | 45 | SMC | T9_NOME | 01/17/2007 |
| 46 | 46 | SMC Support | (MASTER) | (MASTER) |
| 47 | 47 | LPC+ Debug Connector | M76_MLB | 03/19/2007 |
| 48 | 48 | SMBus Connections | (MASTER) | (MASTER) |
| 49 | 49 | Current & Voltage Sensing | (MASTER) | (MASTER) |
| 50 | 50 | Current Sensing | (MASTER) | (MASTER) |
| 51 | 51 | Thermal Sensors | (MASTER) | (MASTER) |
| 52 | 52 | Fan Connectors | M76_MLB | 03/19/2007 |
| 53 | 53 | ALS Support | M76_MLB | 03/19/2007 |
| 54 | 54 | Sudden Motion Sensor (SMS) | M76_MLB | 03/19/2007 |
| 55 | 55 | SPI BootROM | T9_NOME | 03/16/2007 |
| 56 | 56 | PBus-In & Battery Connectors | (M59_SYNC) | 09/09/2006 |
| 57 | 57 | Power FETs | M76_MLB | 03/19/2007 |
| 58 | 58 | IMVP6 CPU VCore Regulator | M76_MLB | 01/23/2007 |
| 59 | 59 | IMVP6 NB Gfx Core Regulator | M76_MLB | 03/19/2007 |
| 60 | 60 | 5V / 3.3V Power Supply | M76_MLB | 03/19/2007 |
| 61 | 61 | 1.25V / 1.05V Power Supply | M76_MLB | 03/12/2007 |
| 62 | 62 | 1.8V DDR2 Supply | M76_MLB | 03/19/2007 |
| 63 | 63 | 1.5V Power Supply | M76_MLB | 03/12/2007 |
| 64 | 64 | FW PHY Power Supplies | M76_MLB | 03/19/2007 |
| 65 | 65 | 3.425V G3Hot Supply & Power Control | (MASTER) | (MASTER) |
| 66 | 66 | NV G84M PCI-E | (MASTER) | (MASTER) |
| 67 | 67 | NV G84M Core/FB Power | (MASTER) | (MASTER) |
| 68 | 68 | NV G84M Frame Buffer I/F | (MASTER) | (MASTER) |
| 69 | 69 | GDDR3 Frame Buffer A | (MASTER) | (MASTER) |
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| 71 | 71 | NV G84M GPIO/MIO/Misc | (MASTER) | (MASTER) |
| 72 | 72 | GPU Straps | (MASTER) | (MASTER) |
| 73 | 73 | NV G84M Video Interfaces | (MASTER) | (MASTER) |
| 74 | 74 | GPU (G84M) Core Supply | (MASTER) | (MASTER) |
| 75 | 75 | LVDS Display Connector | (MASTER) | (MASTER) |
| 76 | 76 | DVI Display Connector | (MASTER) | (MASTER) |
| 77 | 77 | LVDS Interface Mux | (MASTER) | (MASTER) |
| 78 | 78 | Project Specific Connectors | (M59_SYNC) | 08/24/2006 |
| 79 | 79 | CPU/FSB Constraints | T9_NOME | 01/17/2007 |
| 80 | 80 | NB Constraints | T9_NOME | 01/17/2007 |
| 81 | 81 | Memory Constraints | T9_NOME | 01/17/2007 |
| 82 | 82 | SB Constraints (1 of 2) | T9_NOME | 01/17/2007 |
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| 84 | 84 | Clock & SMC Constraints | T9_NOME | 01/17/2007 |
| 85 | 85 | FireWire Constraints | T9_NOME | 01/17/2007 |
| 86 | 86 | GPU (G84M) Constraints | (MASTER) | (MASTER) |
| 87 | 87 | Project Specific Constraints | (MASTER) | (MASTER) |
| 88 | 88 | PCB Rule Definitions | (MASTER) | (MASTER) |

Schematic / PCB #'s

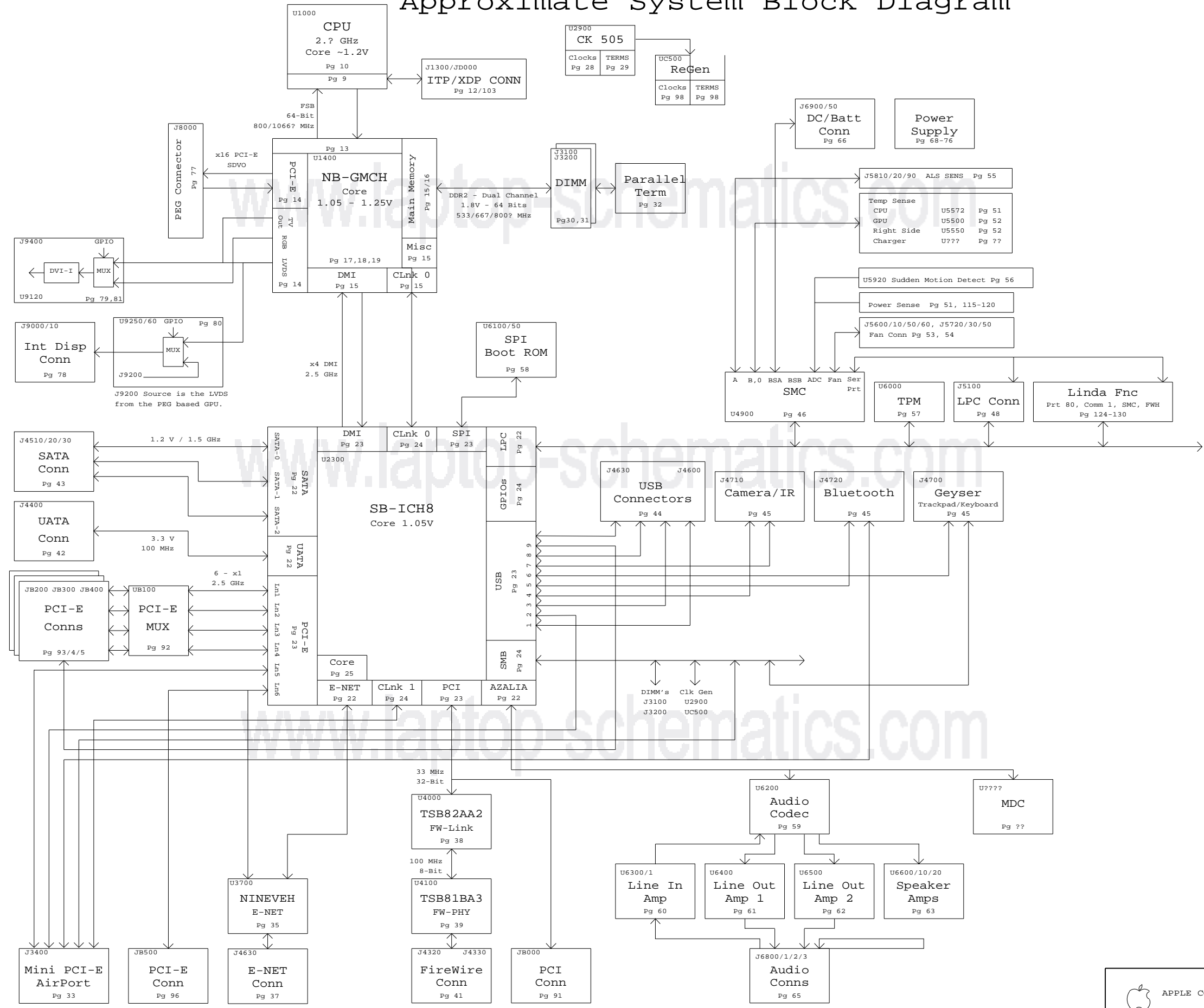
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------|---------------|----------|------------|
| 051-7435 | 1 | SCHEM, MLB, MBP15 | SCH | CRITICAL | |
| 820-2101 | 1 | PCBF, MLB, MBP15 | PCB | CRITICAL | |

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed May 23 18:18:49 2007

| | | | | | |
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| ANGLES : | _____ | | | | |
| DO NOT SCALE DRAWING | | | | TITLE | |
|  THIRD ANGLE PROJECTION | | DRAFTER ENG APPD QA APPD RELEASE | DESIGN CK MFG APPD DESIGNER SCALE | SCHEM, MLB, MBP15 | |
| | | MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D | DRAWING NUMBER | REV. A |
| | | | | 051-7435 | 1 OF 109 |

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Approximate System Block Diagram



System Block Diagram
 SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006
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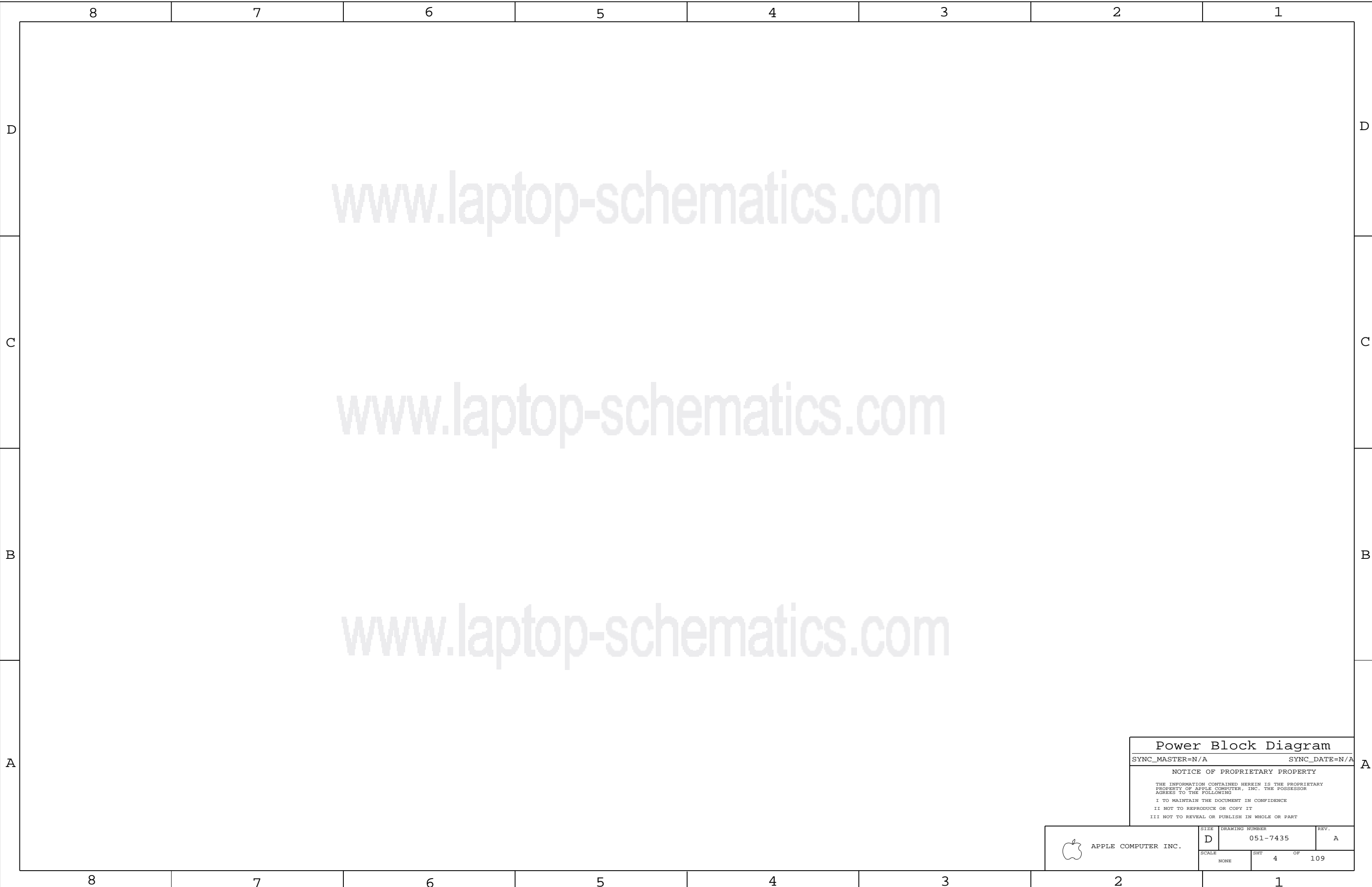
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Power Block Diagram

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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Power Block Diagram

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BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|------------|----------------------------------|---|
| 630-9054 | PCBA, 2.2GHZ, 128VRAM-SAM, MBP15 | M75_COMMON, EEE_YSN, CPU_2_2GHZ, FB_128_SAMSUNG |
| 630-9055 | PCBA, 2.4GHZ, 256VRAM-SAM, MBP15 | M75_COMMON, EEE_YSP, CPU_2_4GHZ, FB_256_SAMSUNG |
| 630-9056 | PCBA, 2.2GHZ, 128VRAM-HY, MBP15 | M75_COMMON, EEE_YSQ, CPU_2_2GHZ, FB_128_HYNIX |
| 630-9057 | PCBA, 2.4GHZ, 256VRAM-HY, MBP15 | M75_COMMON, EEE_YSR, CPU_2_4GHZ, FB_256_HYNIX |

M75 BOM Groups

| BOM GROUP | BOM OPTIONS |
|---------------|---|
| M75_COMMON | ALTERNATE, COMMON, M75_COMMON1, M75_COMMON2, M75_DEBUG, M75_PROGPARTS |
| M75_COMMON1 | EXTGPU_RST_HW, ISL9504B, LVDS_SEL_RESUME, ONEWIRE_PU |
| M75_COMMON2 | P1V8S3_1V825, SLG2AP101, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN |
| M75_DEBUG | SMC_DEBUG_NO, XDP, LPCPLUS |
| M75_PROGPARTS | BOOTROM_PROG, SMC_PROG |

| BOM GROUP | BOM OPTIONS |
|----------------|--|
| FB_128_SAMSUNG | VRAM_128, VRAM_SAMSUNG, VRAM_128_SAMSUNG |
| FB_128_HYNIX | VRAM_128, VRAM_HYNIX, VRAM_128_HYNIX |
| FB_256_SAMSUNG | VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG |
| FB_256_HYNIX | VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX |

Bar Code Labels / EEE #'s

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|----------------------------------|---------------|----------|------------|
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:YSN] | CRITICAL | EEE_YSN |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:YSP] | CRITICAL | EEE_YSP |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:YSQ] | CRITICAL | EEE_YSQ |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:YSR] | CRITICAL | EEE_YSR |

Module Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--|---------------|----------|---------------|
| 337S3464 | 1 | IC, MDC, SR, E1, PRQ, 2.2G, 35W, 800FSB, 4M, BGA | U1000 | CRITICAL | CPU_2_2GHZ |
| 337S3465 | 1 | IC, MDC, SR, E1, PRQ, 2.4G, 35W, 800FSB, 4M, BGA | U1000 | CRITICAL | CPU_2_4GHZ |
| 338S0388 | 1 | IC, GPU, NV G84M, BGA | U8000 | CRITICAL | |
| 338S0432 | 1 | IC, NB, CRESTLINE, GM, CO, PRQ, 965PM | U1400 | CRITICAL | |
| 338S0434 | 1 | IC, SB, ICH8M, B1, PRQ, BGA | U2300 | CRITICAL | |
| 353S1461 | 1 | IC, ISL9504, SYNC REG CTRL, 2PHAS, QFN48, LF | U7100 | CRITICAL | ISL9504A |
| 353S1651 | 1 | IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48 | U7100 | CRITICAL | ISL9504B |
| 359S0127 | 1 | IC, 68 PIN, CK505, LOW POWER CLOCK GENER | U2900 | CRITICAL | SLG8LP537 |
| 359S0130 | 1 | IC, SLG2AP101, 1.5M PWR CLK GEN, CK505, QFN68 | U2900 | CRITICAL | SLG2AP101 |
| 338S0386 | 1 | IC, 88E8058, GIGABIT ENET XCVR, 64P QFN | U3700 | CRITICAL | |
| 338S0274 | 1 | IC, SMC, HSS/2116 | U4900 | CRITICAL | SMC_BLANK |
| 341S2004 | 1 | IC, SMC, DEVELOPMENT, M75 | U4900 | CRITICAL | SMC_PROG |
| 335S0384 | 1 | IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8 | U6100 | CRITICAL | BOOTROM_BLANK |
| 341S2002 | 1 | IC, EFI ROM, DEVELOPMENT, M75 | U6100 | CRITICAL | BOOTROM_PROG |

| | | | | | |
|----------|---|--|----------------------------|----------|------------------|
| 333S0404 | 4 | IC, SGRAM, GDDR3, 8Mx32, 700MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_128_SAMSUNG |
| 333S0409 | 4 | IC, SGRAM, GDDR3, 8Mx32, 700MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_128_HYNIX |
| 333S0382 | 4 | IC, SGRAM, GDDR3, 16Mx32, 700MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_256_SAMSUNG |
| 333S0401 | 4 | IC, SGRAM, GDDR3, 16Mx32, 700MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_256_HYNIX |

| PART NUMBER | IS ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|------------------------------|------------|---------|----------------------------------|
| 157S0011 | 157S0030 | | ALL | See alt to TOK/BI-Tech magnetica |
| 152S0476 | 152S0276 | | ALL | Inductor alternate |
| 353S1681 | 353S1294 | | ALL | TI alt to National |
| 138S0603 | 138S0602 | | ALL | Murata alt to Samsung |

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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| SCALE | DRAWING NUMBER | REV. |
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| NONE | D 051-7435 | A |
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PROTO

See Perforce change notes for updates before Proto Release 12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0: 01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0: 01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0: 01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0: 01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0: 01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMPTIONS and values for ISL9504B
01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0: 01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path
9.4.0: 01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787)
9.5.0: 01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMPTIONS for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3_1V825 BOMPTION to lift voltage at FB memories
10.0.0: 01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMPTIONS to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

EVT_SE

10.1.0: 01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0
01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings
01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes
10.2.0: 01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST
01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes
11.0.0: 01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K)
01/25/07 -- BOM: Updated all Intel APNs to use QS parts
01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03)
12.0.0: 02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup
02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup
02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain
02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain
02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

DVT

12.1.0: 02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)
02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)
02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)
02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates
02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)
12.2.0: 02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)
02/28/07 -- Power Aliases: Moving PP1V8_GPU FET source to PP1V8_S3 rather than PP1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462)
12.3.0: 02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines
12.4.0: 03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)
03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
12.5.0: 03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements
12.6.0: 03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)
03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height
12.7.0: 03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request
03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)
03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage

DVT (cont'd)

12.8.0: 03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0: 03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0: 03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0: 03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0: 03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0: 03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0: 03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0: 03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)
15.0.0: 03/30/07 -- SIL: Changed R5031 to 2.21K and R5032 to 9.53K to raise SIL current approx 15% (lightpipe dimmed by 20%)
03/30/07 -- Power Supply: Changed 1.05V power supply current limit to 10A from 8A (R7455 to 5.62k -- rdar://5095642)
04/03/07 -- Power Supply: Changed numerous 10K Rs to 100K for Energy Star compliance (rdar://5102118)
04/03/07 -- GPU FB: Changed FB clock termination to 242 ohms (2x121) per Nvidia PUN
04/03/07 -- CPU Vcore: Changed R7117,C7134 and R7115,R7130 for calibration improvements (rdar://5085959)
04/03/07 -- Released for DVT (BOM update)
16.0.0: 04/17/07 -- Power Sequencing: NO STUFFED U7858 and stuffed R7860 to allow SMC to drive S5 enable pins directly
04/17/07 -- Released for DVT (As-Built)

Pre-PVT

16.1.0: 04/18/07 -- GPU Misc: Added R8735-37 to implement PCI DEVID 0x407 in hardware
16.2.0: 04/18/07 -- Power FETs: Changed Q7095 to FDM6296 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)
04/18/07 -- Modules: Updated Intel chipset to PRQ parts
16.3.0: 04/20/07 -- Power FETs: Changed R7097 to 220K to maintain EnergyStar compliance with FET gate pulled to PBUS
04/20/07 -- Power FETs: Changed C7095/C7083 to 16V for proper rating of parts tied to PBUS
04/20/07 -- CPU VCore: Changed C7196 to 16V to eliminate a BOM item
17.0.0: 04/20/07 -- No changes. Weekly BOM release.
A.0.0: 04/24/07 -- SB Decoupling: Changed L2700 from 155S0152 to 155S0333 for AVL updates
04/24/07 -- SMC Support: Changed R5031 to 2.37K, R5032 to 9.09K to meet SIL brightness targets
04/24/07 -- Released for Pre-PVT

PVT

A.0.0: 05/08/07 -- SB Decoupling: Changed C2703 to 158S0578 per Intel recommendations (rdar://5185100)
05/08/07 -- GPU Straps: Stuffed R8728 to put GPU PEG I/F into mobile mode (rdar://5188253)
05/24/07 -- Re-released for PVT/production with new part numbers

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Table with columns: DRAWING NUMBER (051-7435), REV. (A), SCALE (NONE), SHEET (6 OF 109)



APPLE COMPUTER INC.

Functional Test Points

ICT Test Points

Fan Connectors

| FUNC_TEST | Pin | Signal |
|-----------|------|-----------------|
| TRUE | 8 52 | =PP5V S0 FAN LT |
| TRUE | 52 | FAN LT PWM |
| TRUE | 52 | FAN LT TACH |
| TRUE | 52 | FAN RT PWM |
| TRUE | 52 | FAN RT TACH |

Battery Digital Connector

| FUNC_TEST | Pin | Signal |
|-----------|----------|-----------------|
| TRUE | 45 46 56 | SMC_BS_ALERT_L |
| TRUE | 48 56 | =SMBUS_BATT_SCL |
| TRUE | 48 56 | =SMBUS_BATT_SDA |
| TRUE | 56 | GND_BATT |

CPU FSB NO_TESTS

| NO_TEST | Pin | Signal |
|---------|----------|--------------------|
| TRUE | 10 14 79 | FSB_A_L<31..3> |
| TRUE | 10 14 79 | FSB_ADS_L |
| TRUE | 10 14 79 | FSB_ADSTB_L<1..0> |
| TRUE | 10 14 79 | FSB_BNR_L |
| TRUE | 10 14 79 | FSB_BREQ0_L |
| TRUE | 10 14 79 | FSB_D_L<63..0> |
| TRUE | 10 14 79 | FSB_DBSY_L |
| TRUE | 10 14 79 | FSB_DINV_L<3..0> |
| TRUE | 10 14 79 | FSB_DRDY_L |
| TRUE | 10 14 79 | FSB_DSTB_L_N<3..0> |
| TRUE | 10 14 79 | FSB_DSTB_L_P<3..0> |
| TRUE | 10 14 79 | FSB_HIT_L |
| TRUE | 10 14 79 | FSB_HITM_L |
| TRUE | 10 14 79 | FSB_LOCK_L |
| TRUE | 10 14 79 | FSB_REQ_L<4..0> |

NB NO_TESTS

| NO_TEST | Pin | Signal |
|---------|-----|-----------------|
| TRUE | 16 | NC_NB_NC<1..16> |
| TRUE | 16 | TP_NB_NC<1..16> |

LPC+ Debug Connector

| FUNC_TEST | Pin | Signal |
|-----------|-------------|--------------------|
| TRUE | 8 47 | =PP3V3_S5_LPCPLUS |
| TRUE | 8 47 | =PP5V_S0_LPCPLUS |
| TRUE | 23 45 47 | LPC_AD<0> |
| TRUE | 23 45 47 | LPC_AD<1> |
| TRUE | 23 45 47 | LPC_FRAME_L |
| TRUE | 25 45 47 | PM_CLKRUN_L |
| TRUE | 24 47 | BOOT_LPC_SPI_L |
| TRUE | 45 46 47 | SMC_TMS |
| TRUE | 28 47 | DEBUG_RESET_L |
| TRUE | 45 47 | SMC_TRST_L |
| TRUE | 45 46 47 | SMC_TDO |
| TRUE | 45 47 | SMC_MD1 |
| TRUE | 43 45 46 47 | SMC_TX_L |
| TRUE | 47 | FWH_INIT_L |
| TRUE | 30 47 84 | PCI_CLK33M_LPCPLUS |
| TRUE | 23 45 47 | LPC_AD<2> |
| TRUE | 23 45 47 | LPC_AD<3> |
| TRUE | 25 45 47 | INT_SERRIO |
| TRUE | 25 45 46 47 | PM_SUS_STAT_L |
| TRUE | 45 46 47 | SMC_TDI |
| TRUE | 45 46 47 | SMC_TCK |
| TRUE | 45 46 47 | SMC_RESET_L |
| TRUE | 45 47 | SMC_NMI |
| TRUE | 43 45 46 47 | SMC_RX_L |
| TRUE | 25 47 | LINDACARD_GPIO |

Left I/O Power Connector

| FUNC_TEST | Pin | Signal |
|-----------|------|---------------------|
| TRUE | 8 56 | =PPBUS_G3H_LIO_CONN |
| TRUE | | GND |

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

| FUNC_TEST | Pin | Signal |
|-----------|-----|----------------|
| TRUE | 28 | PPVBATT_G3_RTC |
| TRUE | | GND |

Current Sense Calibration

| FUNC_TEST | Pin | Signal |
|-----------|---------|------------------------|
| TRUE | 45 49 | ISENSE_CAL_EN |
| TRUE | 8 49 | =PP5V_S0_ISENSECAL |
| TRUE | 8 59 | =PPVCORE_S0_NBGF_X_REG |
| TRUE | 8 49 58 | =PPVCORE_S0_CPU_REG |
| TRUE | 8 49 74 | =PPVCORE_GPU_REG |
| TRUE | | GND |

2 TPs per

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

| FUNC_TEST | Pin | Signal |
|-----------|----------|-----------------|
| TRUE | 8 44 | =PP5V_S3_CAMERA |
| TRUE | 24 44 82 | USB_CAMERA_N |
| TRUE | 24 44 82 | USB_CAMERA_P |
| TRUE | 8 44 | =PP5V_S3_WWAN |
| TRUE | 44 | USB_WWAN_N |
| TRUE | 44 | USB_WWAN_P |

Other Func Test Points

| FUNC_TEST | Pin | Signal |
|-----------|----------|-------------|
| TRUE | 25 28 45 | PM_SYSRST_L |
| TRUE | 45 46 78 | SMC_ONOFF_L |

Left ALS Connector

| FUNC_TEST | Pin | Signal |
|-----------|----------|-----------------|
| TRUE | 8 78 | =PP3V3_S3_LTALS |
| TRUE | 45 53 78 | ALS_GAIN |
| TRUE | 53 78 | LTALS_OUT |
| TRUE | | GND |

Thermal Diode Connectors

| FUNC_TEST | Pin | Signal |
|-----------|-------|----------------|
| TRUE | 51 87 | HSTHMSNS_D_P |
| TRUE | 51 | HSTHMSNS_D_N |
| TRUE | 51 87 | RSFTHMSNS_D_P |
| TRUE | 51 | RSFTHMSNS_D_N |
| TRUE | 51 87 | CPUTHMSNS_D2_P |
| TRUE | 51 | CPUTHMSNS_D2_N |

CPUTHMSNS can not be supported due to layout constraints

System Validation TPs

| FUNC_TEST | Pin | Signal |
|-----------|-------------|------------------|
| TRUE | 10 13 23 79 | CPU_PWRGD |
| TRUE | 7 10 23 79 | CPU_DPSLP_L |
| TRUE | 16 25 58 79 | PM_DPRS_LPVR |
| TRUE | 7 10 23 79 | CPU_DPSLP_L |
| TRUE | 25 45 | PM_LAN_ENABLE |
| TRUE | 24 28 | PCI_RST_L |
| TRUE | 25 45 | PM_RSMRST_L |
| TRUE | 9 25 28 | PM_SB_PWROK |
| TRUE | 23 28 | SB_RTC_RST_L |
| TRUE | 25 29 30 | PM_STPCPU_L |
| TRUE | 25 29 30 | PM_STPPCI_L |
| TRUE | 25 28 | VR_PWRGD_CLKEN |
| TRUE | 9 16 28 58 | VR_PWRGOOD_DELAY |
| TRUE | 10 13 14 79 | FSB_CPURST_L |
| TRUE | 10 14 79 | FSB_CPUSLP_L |
| TRUE | 10 14 79 | FSB_DPWR_L |
| TRUE | 16 25 | NB_SB_SYNC_L |

| FUNC_TEST | Pin | Signal |
|-----------|----------------|---------------------|
| TRUE | 45 58 | IMVP_VR_ON |
| TRUE | 58 79 | IMVP_DPRS_LPVR |
| TRUE | 25 36 40 45 65 | PM_SLP_S3_L |
| TRUE | 25 45 65 | PM_S4_STATE_L |
| TRUE | 25 45 66 | PM_SLP_S5_L |
| TRUE | 36 65 | PM_ENET_EN |
| TRUE | 65 | P1V5P1V05S0_PGOOD |
| TRUE | 10 16 23 58 79 | CPU_DPRSTP_L |
| TRUE | 12 58 79 | IMVP6_VID<6..0> |
| TRUE | 24 28 77 | PLT_RST_L |
| TRUE | 16 28 | NB_RESET_L |
| TRUE | 28 66 | GPU_RESET_L |
| TRUE | 28 45 | SMC_LRESET_L |
| TRUE | 10 23 79 | CPU_STPCLK_L |
| TRUE | 14 30 84 | FSB_CLK_NB_P |
| TRUE | 14 30 84 | FSB_CLK_NB_N |
| TRUE | 16 29 | NB_CLKREQ0_L |
| TRUE | 16 30 84 | NB_CLK100M_PCIE_P |
| TRUE | 16 30 84 | NB_CLK100M_PCIE_N |
| TRUE | 84 | NB_CLK96M_DOT_P |
| TRUE | 84 | NB_CLK96M_DOT_N |
| TRUE | 22 30 84 | NB_CLK100M_DPLLSS_P |
| TRUE | 22 30 84 | NB_CLK100M_DPLLSS_N |
| TRUE | 23 | CPU_THERMTRIP_R |

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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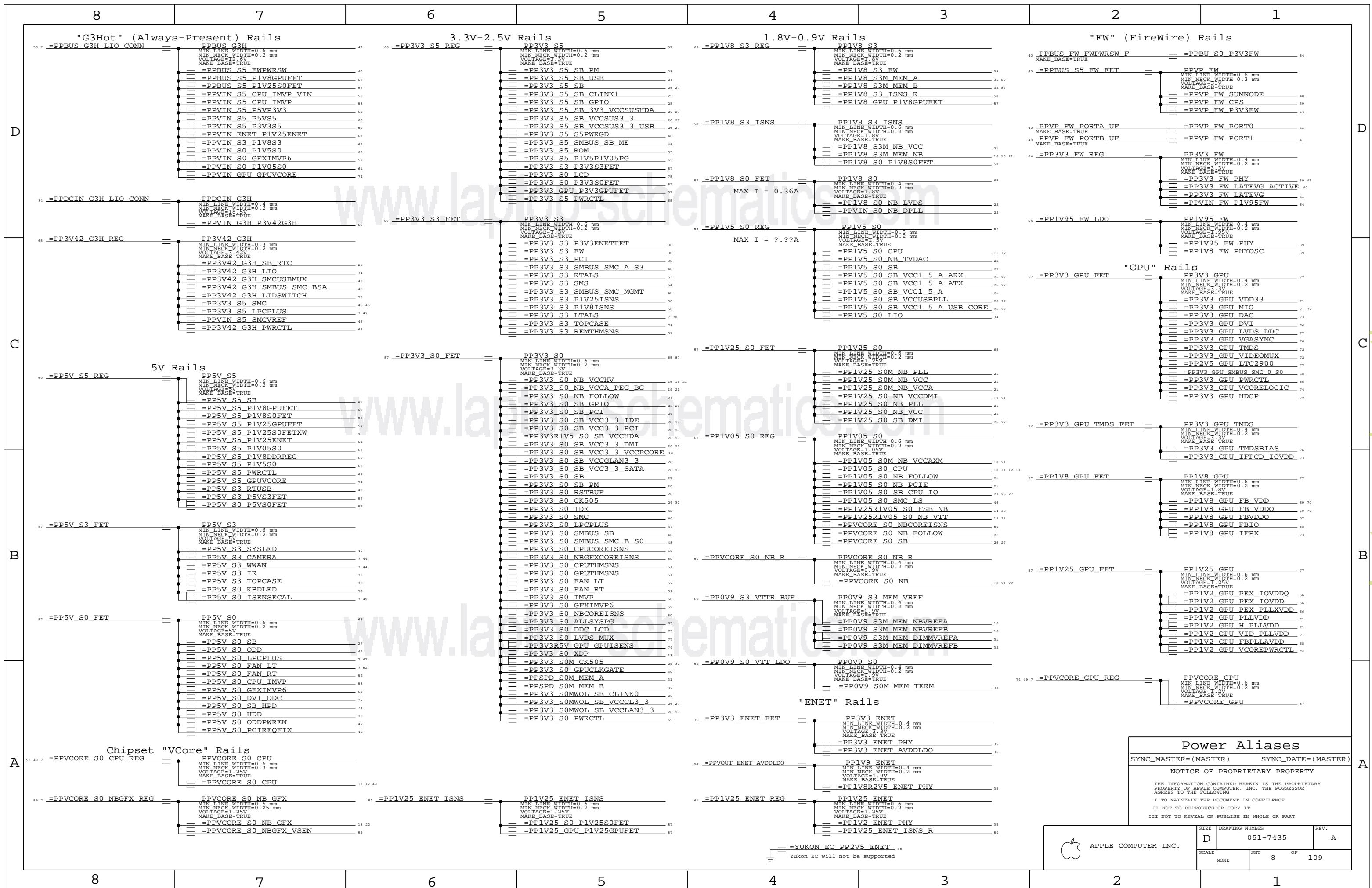
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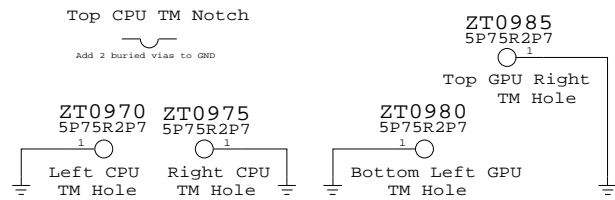
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| NONE | 7 | 109 |

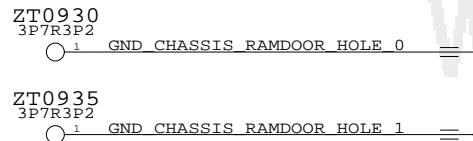


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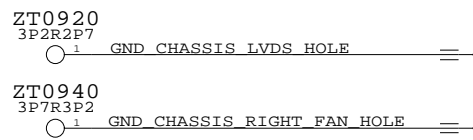
Thermal Module Holes



RAM Door (Torx) Holes

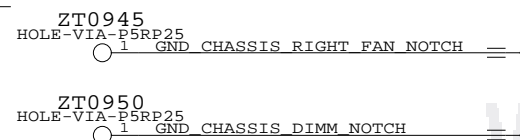


Frame Holes



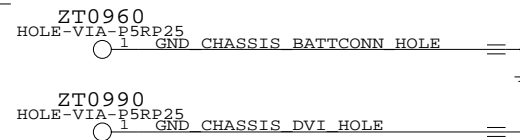
Board Edge Notches

(Can't be PTH)

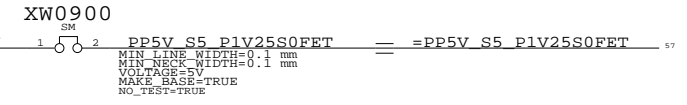
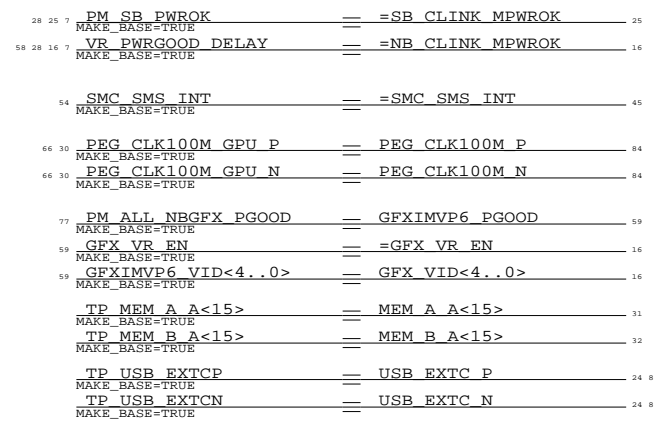
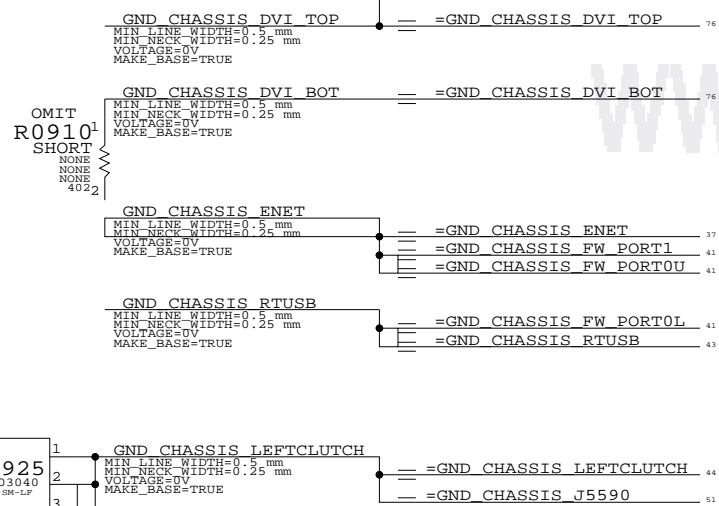


Tooling Holes

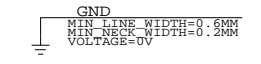
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Chassis GNDs



Digital Ground



Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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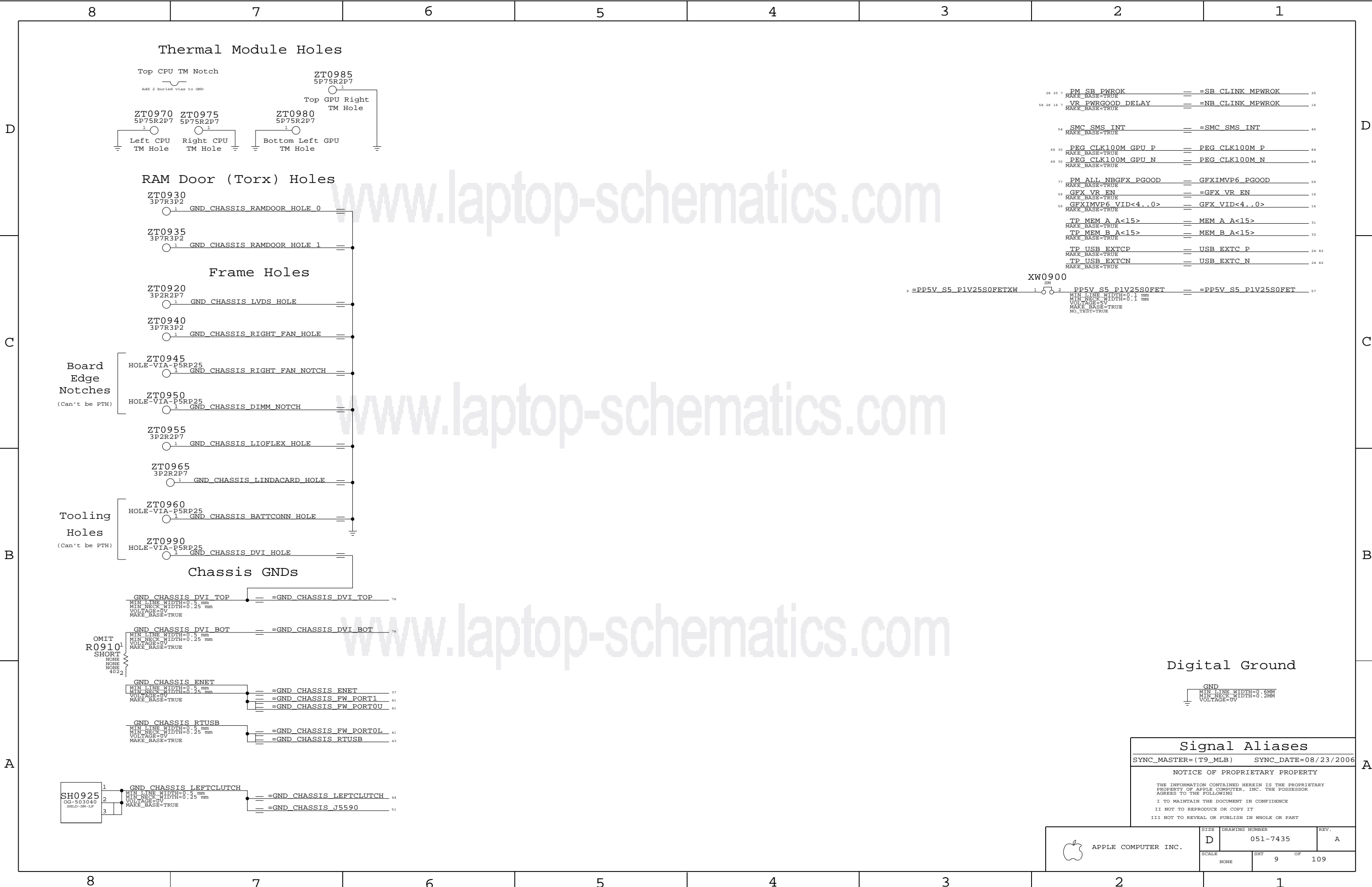
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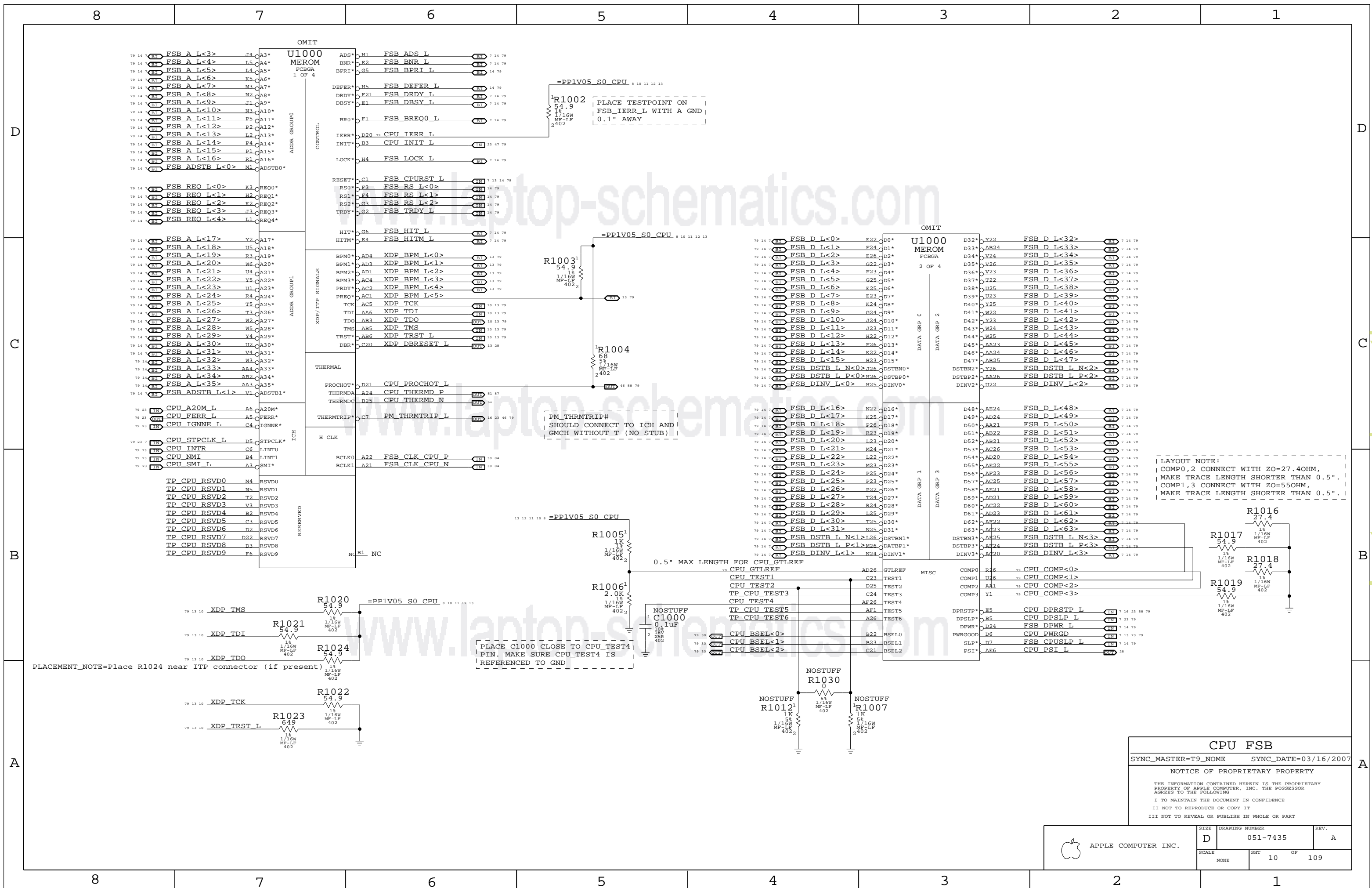
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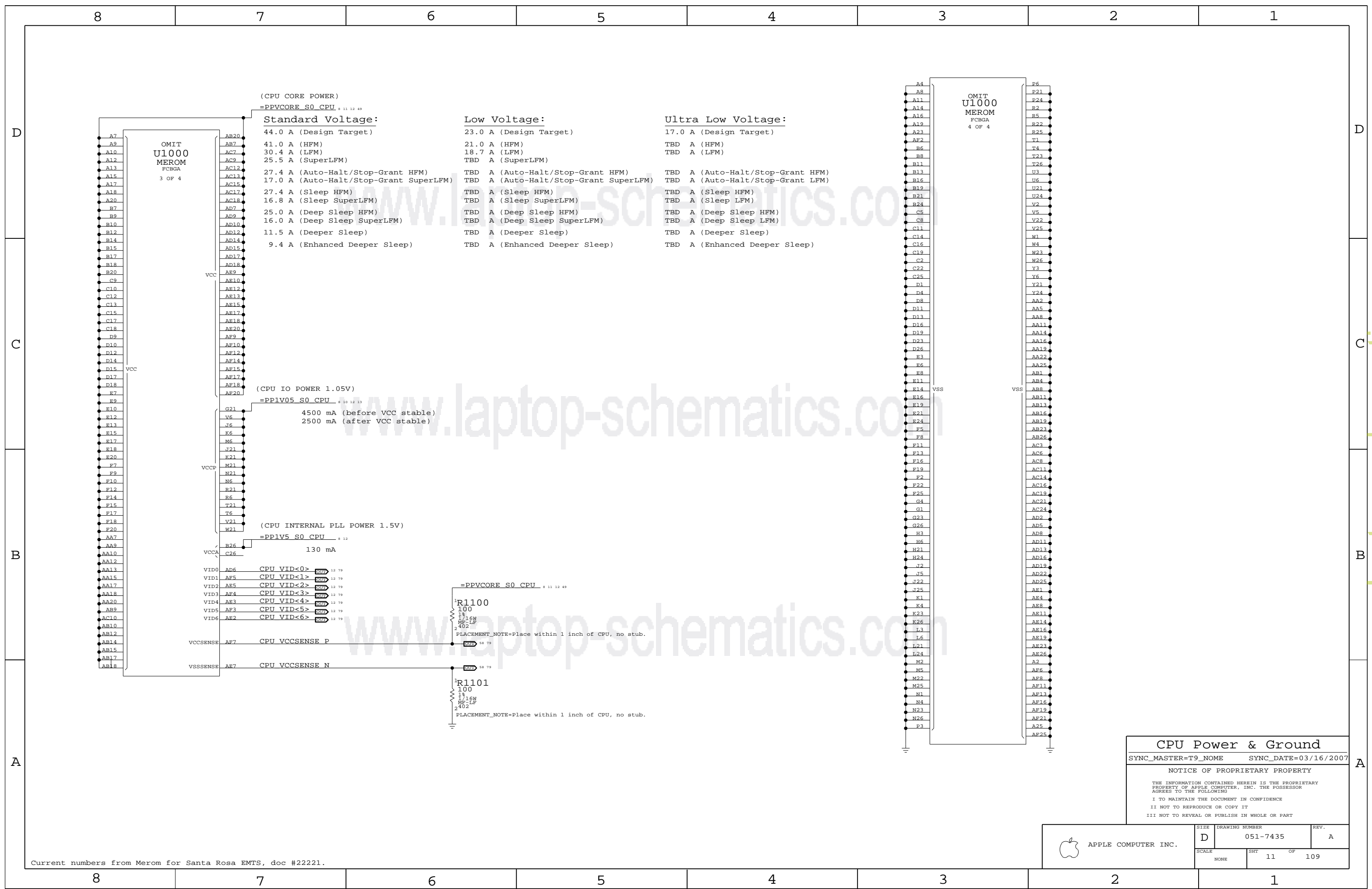
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LAYOUT NOTE:
 COMP0, 2 CONNECT WITH Z0=27.4OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMP1, 3 CONNECT WITH Z0=55OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007
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(CPU CORE POWER)

=PPVCORE_S0_CPU # 11 12 49

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

OMIT
U1000
MEROM
FCBGA
3 OF 4

OMIT
U1000
MEROM
FCBGA
4 OF 4

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU # 10 12 13

- 4500 mA (before VCC stable)
- 2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU # 12

130 mA

- VID0 AD6 CPU VID<0>
- VID1 AE5 CPU VID<1>
- VID2 AE5 CPU VID<2>
- VID3 AF4 CPU VID<3>
- VID4 AE3 CPU VID<4>
- VID5 AF3 CPU VID<5>
- VID6 AE2 CPU VID<6>

VCCSENSE AF7 CPU VCCSENSE P

VSSSENSE AE7 CPU VCCSENSE N

R1100
100
14
1716W
MF-1P
2402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
14
1716W
MF-1P
2402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

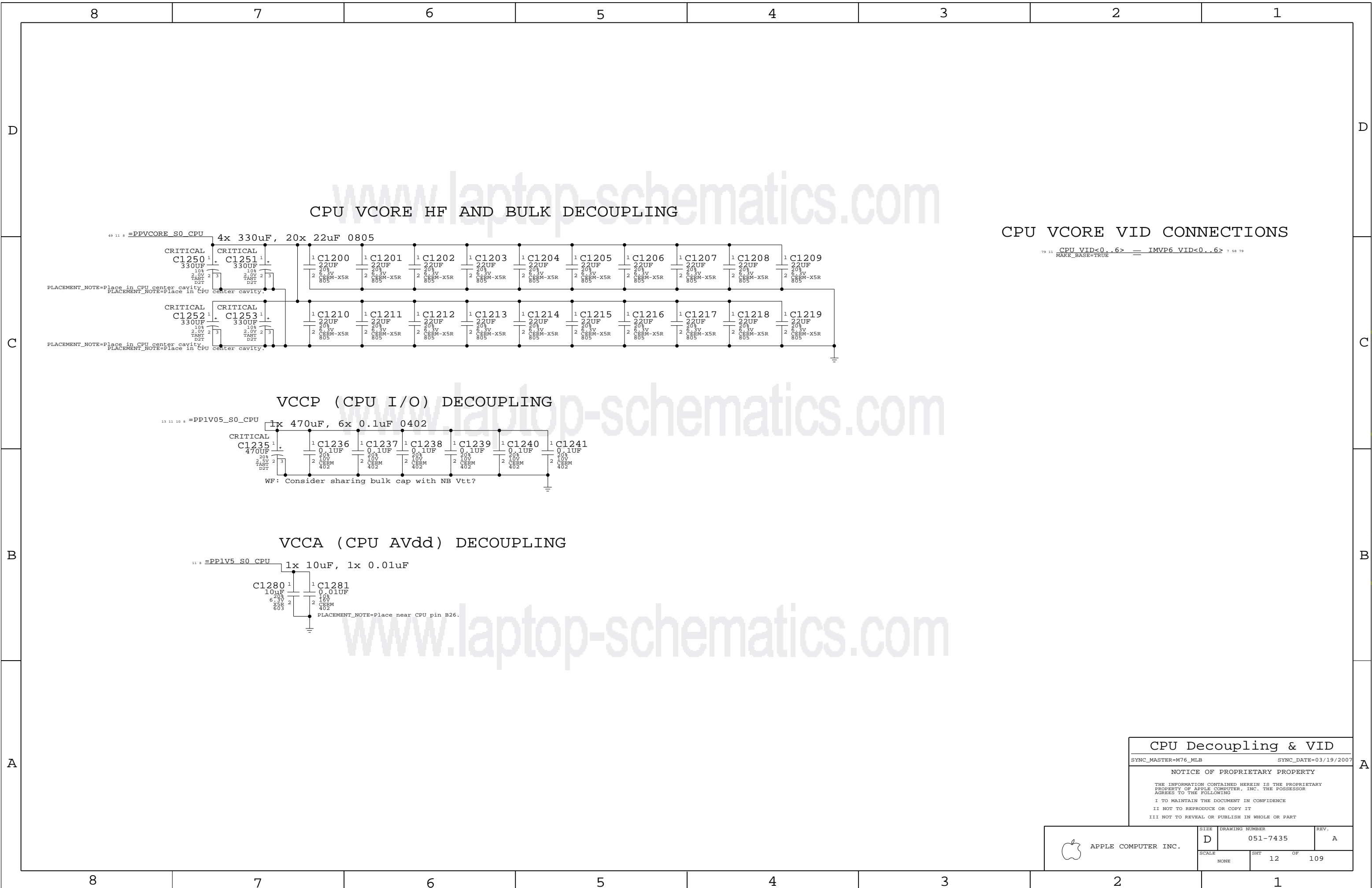
CPU Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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CPU VCORE HF AND BULK DECOUPLING

CPU VCORE VID CONNECTIONS

79 11 CPU VID<0..6> == IMVP6 VID<0..6> 7 18 79
MAKE_BASE=TRUE

VCCP (CPU I/O) DECOUPLING

VCCA (CPU AVdd) DECOUPLING

CPU Decoupling & VID
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007
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| NONE | 12 | | 109 |

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B

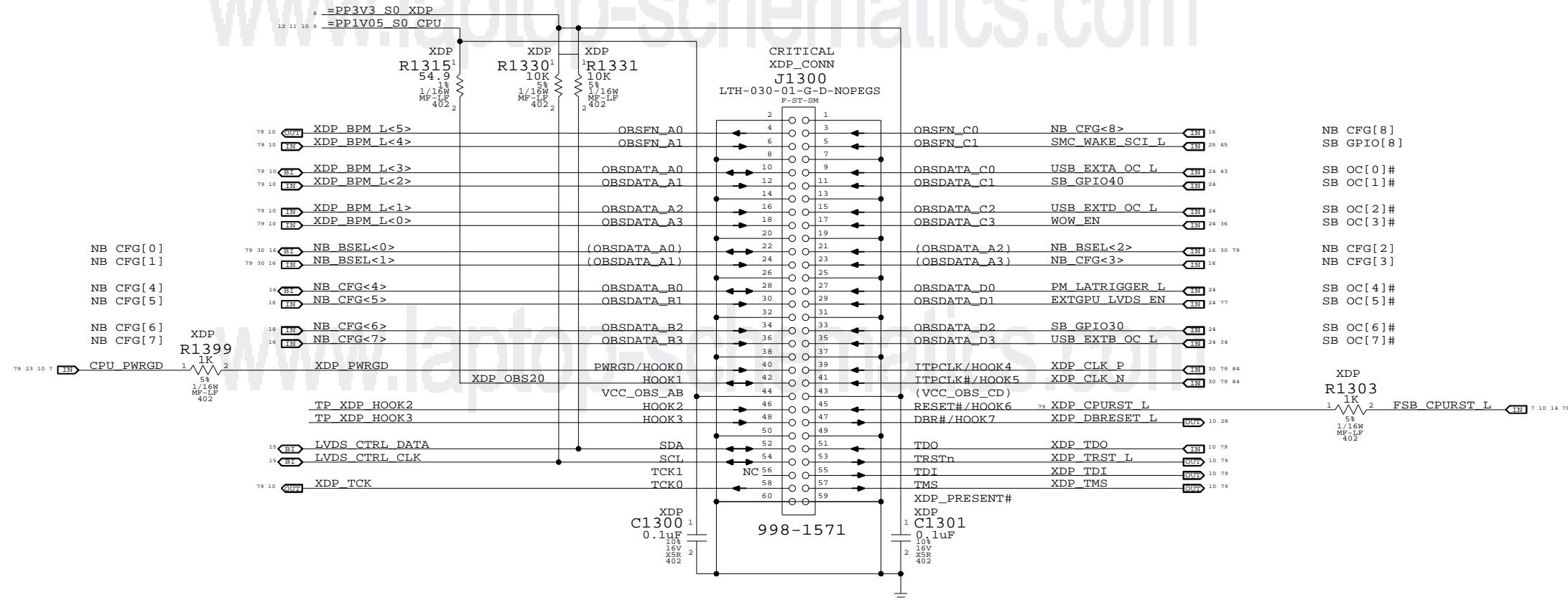
B

A

A

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



← Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)
SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

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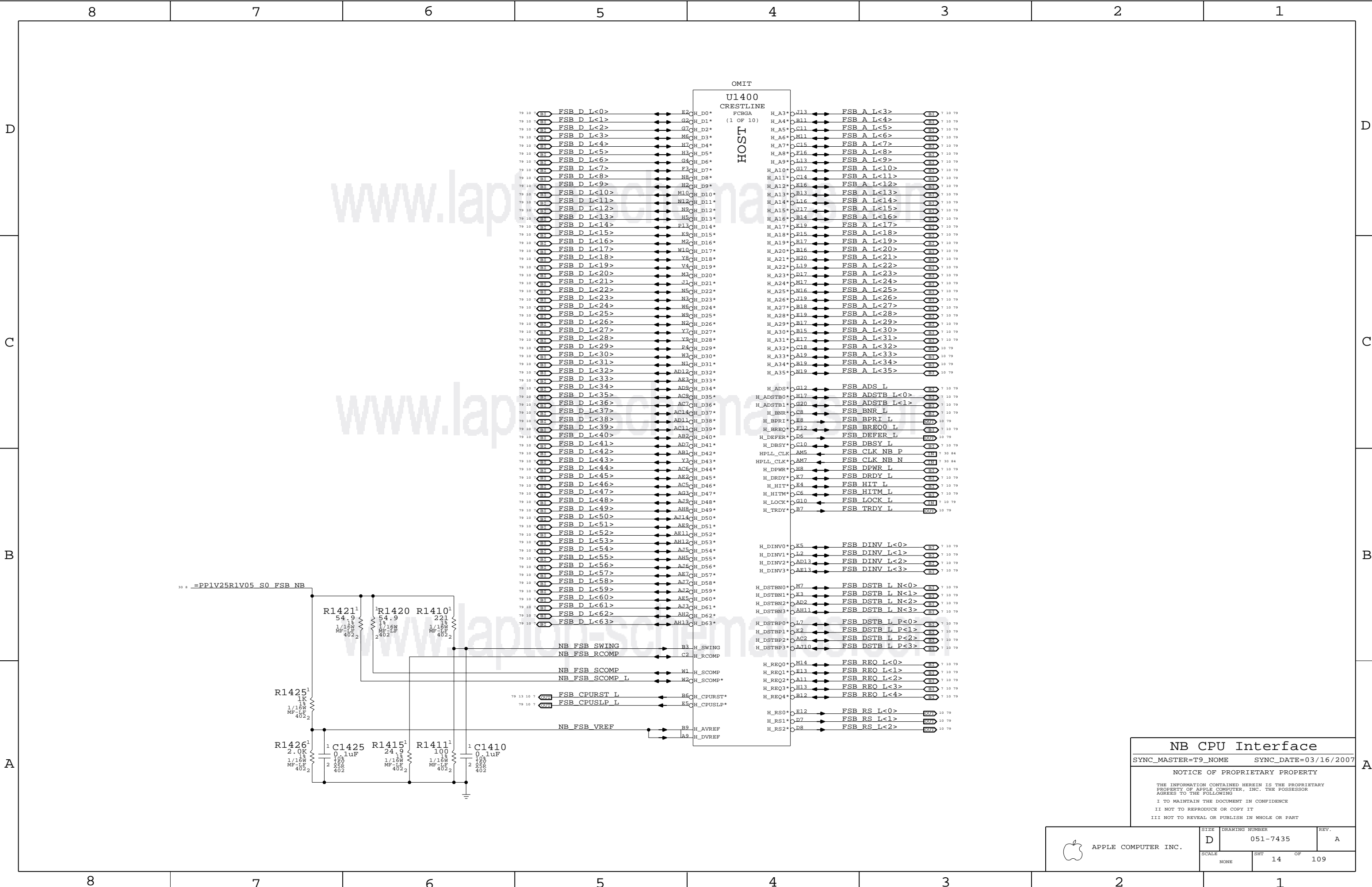
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3

2

1

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NB CPU Interface

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| | D | 051-7435 | A |
| SCALE | SHT | OF | REV. |
| NONE | 14 | 109 | |

LVDS Disable

Can leave all signals NC if LVDS is not implemented. Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

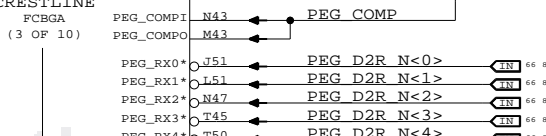
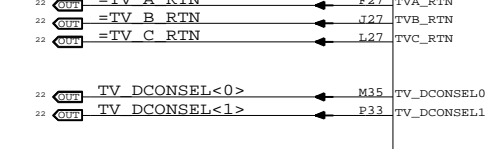
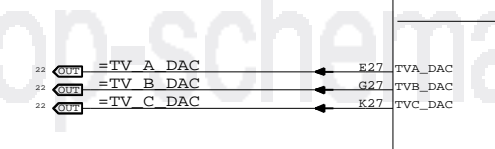
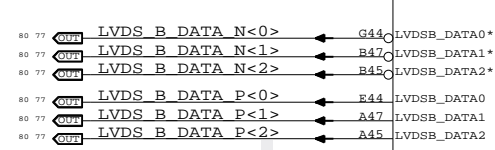
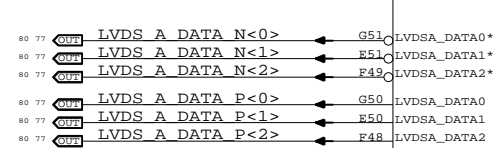
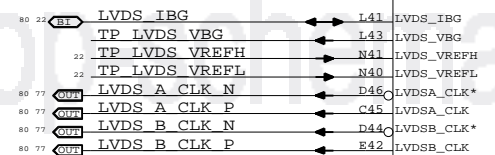
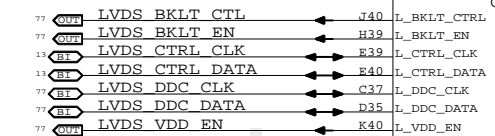
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND. Can tie the following rails to GND: VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND. Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore). Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore). Tie VCC_AXG and VCC_AXG_NCTF to GND. Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLK#
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLK#

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

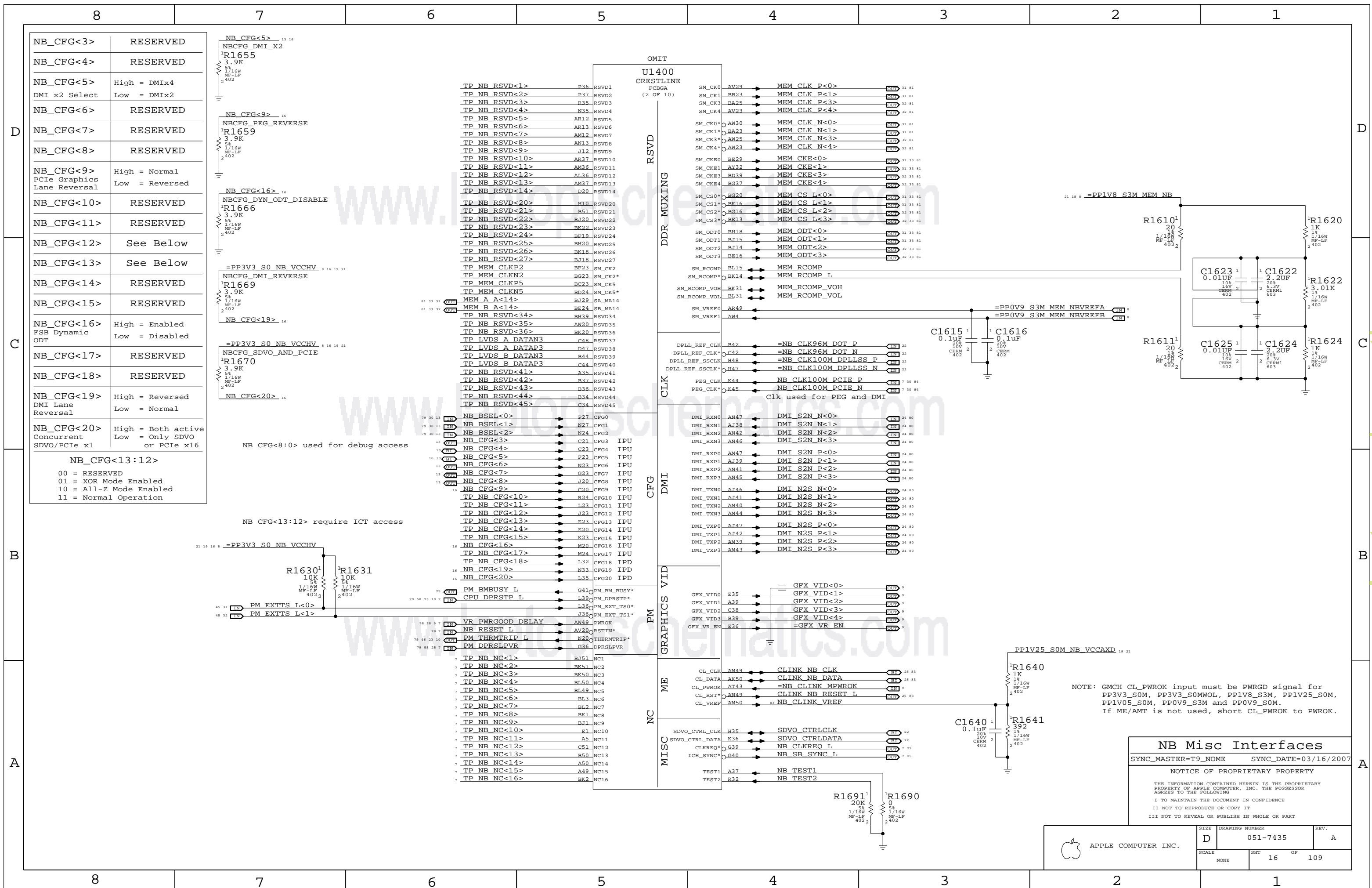
NB PEG / Video Interfaces
SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007

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Table with columns: SIZE (D), DRAWING NUMBER (051-7435), REV. (A), SCALE (NONE), SHEET (15 OF 109)



APPLE COMPUTER INC.



| | |
|------------|---|
| NB_CFG<3> | RESERVED |
| NB_CFG<4> | RESERVED |
| NB_CFG<5> | High = DMIx4 Low = DMIx2 |
| NB_CFG<6> | RESERVED |
| NB_CFG<7> | RESERVED |
| NB_CFG<8> | RESERVED |
| NB_CFG<9> | High = Normal PCIe Graphics Lane Reversal Low = Reversed |
| NB_CFG<10> | RESERVED |
| NB_CFG<11> | RESERVED |
| NB_CFG<12> | See Below |
| NB_CFG<13> | See Below |
| NB_CFG<14> | RESERVED |
| NB_CFG<15> | RESERVED |
| NB_CFG<16> | High = Enabled FSB Dynamic ODT Low = Disabled |
| NB_CFG<17> | RESERVED |
| NB_CFG<18> | RESERVED |
| NB_CFG<19> | High = Reversed DMI Lane Reversal Low = Normal |
| NB_CFG<20> | High = Both active Concurrent Low = Only SDVO SDVO/PCIe x1 or PCIe x16 |

NB_CFG<13:12>

- 00 = RESERVED
- 01 = XOR Mode Enabled
- 10 = All-Z Mode Enabled
- 11 = Normal Operation

NB_CFG<8:0> used for debug access

NB_CFG<13:12> require ICT access

NB Misc Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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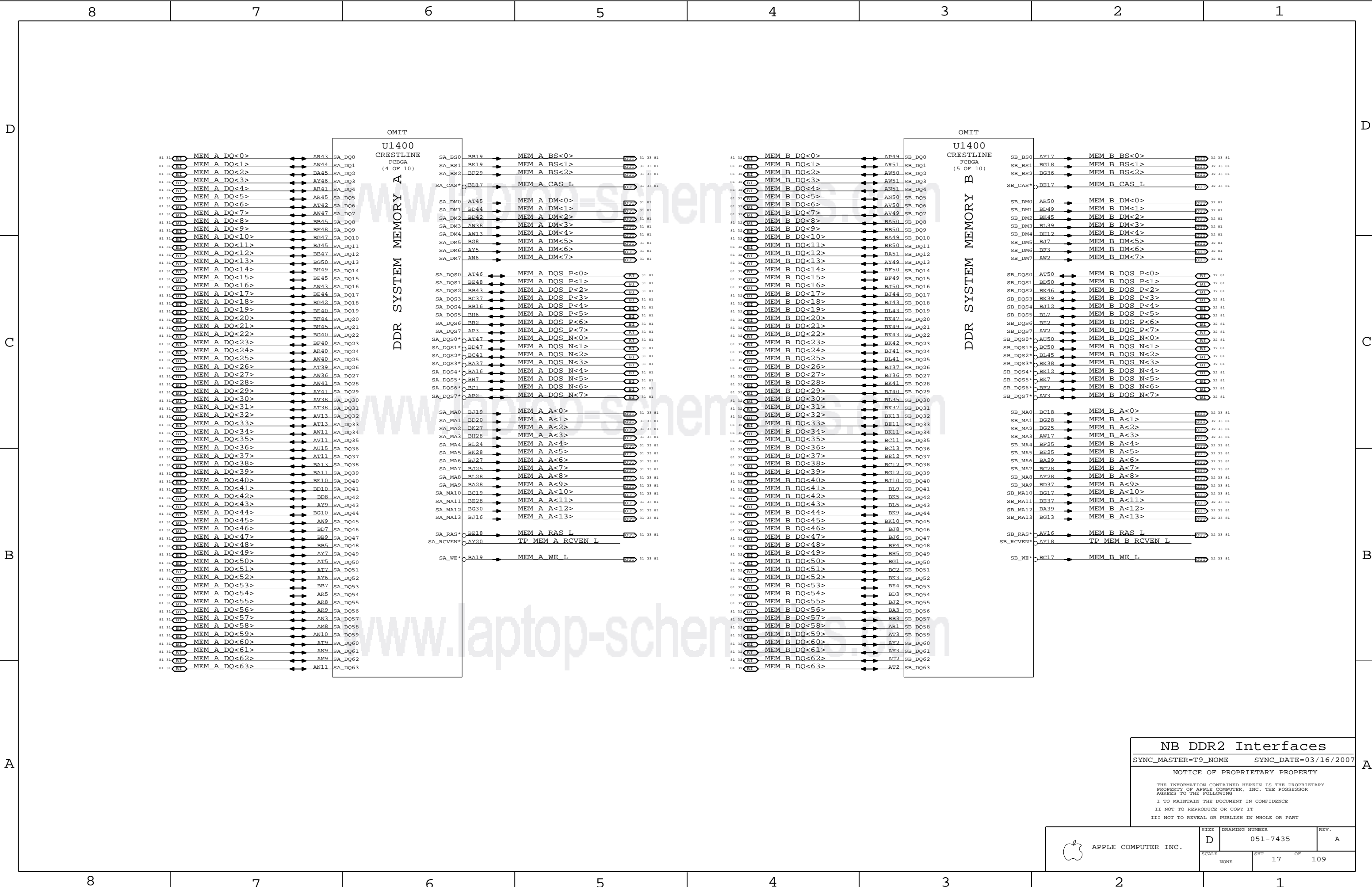
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| SIZE | D | DRAWING NUMBER | 051-7435 | REV. | A |
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NB DDR2 Interfaces
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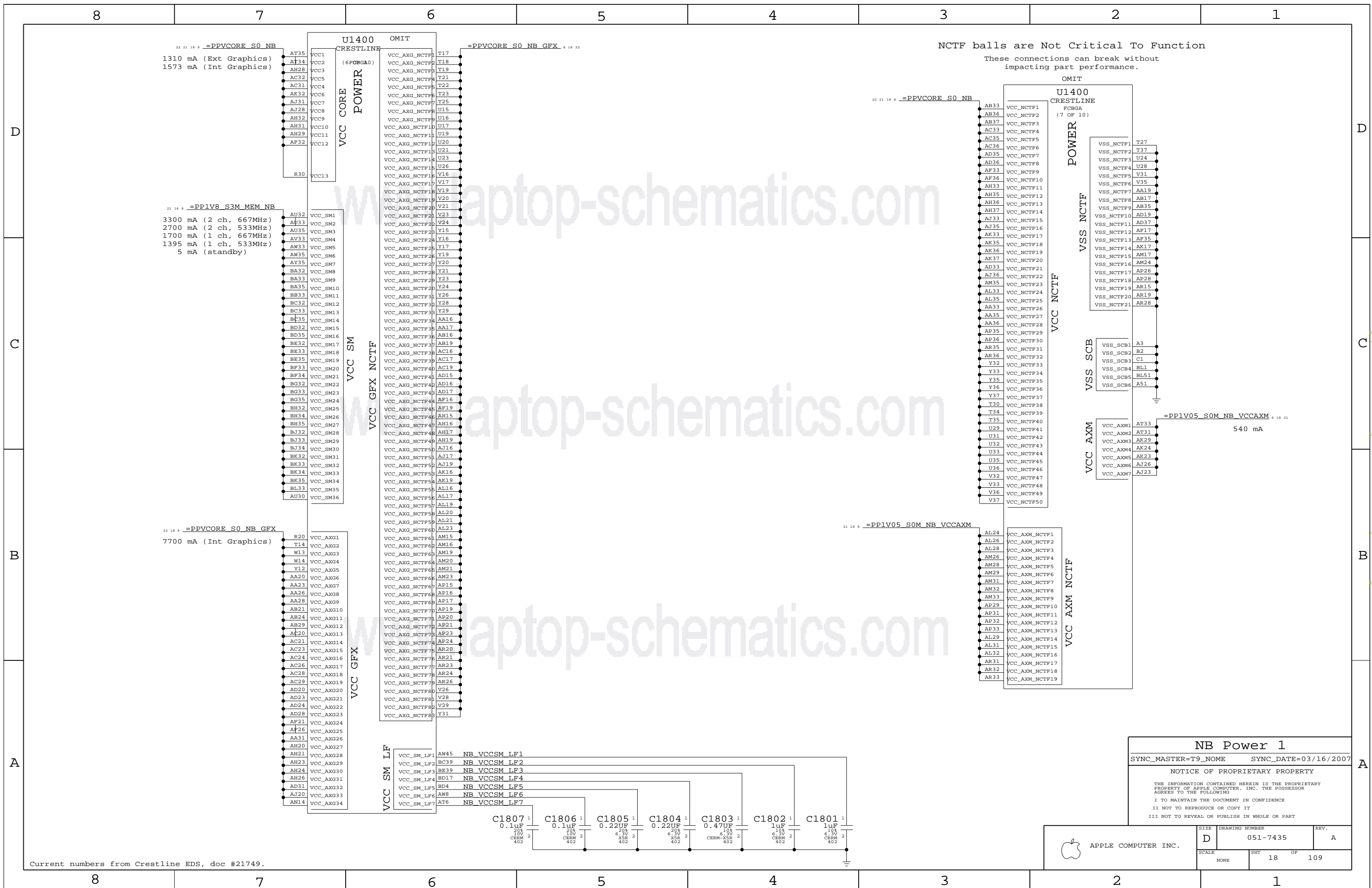
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| | SCALE NONE | SHEET 17 OF 109 | |

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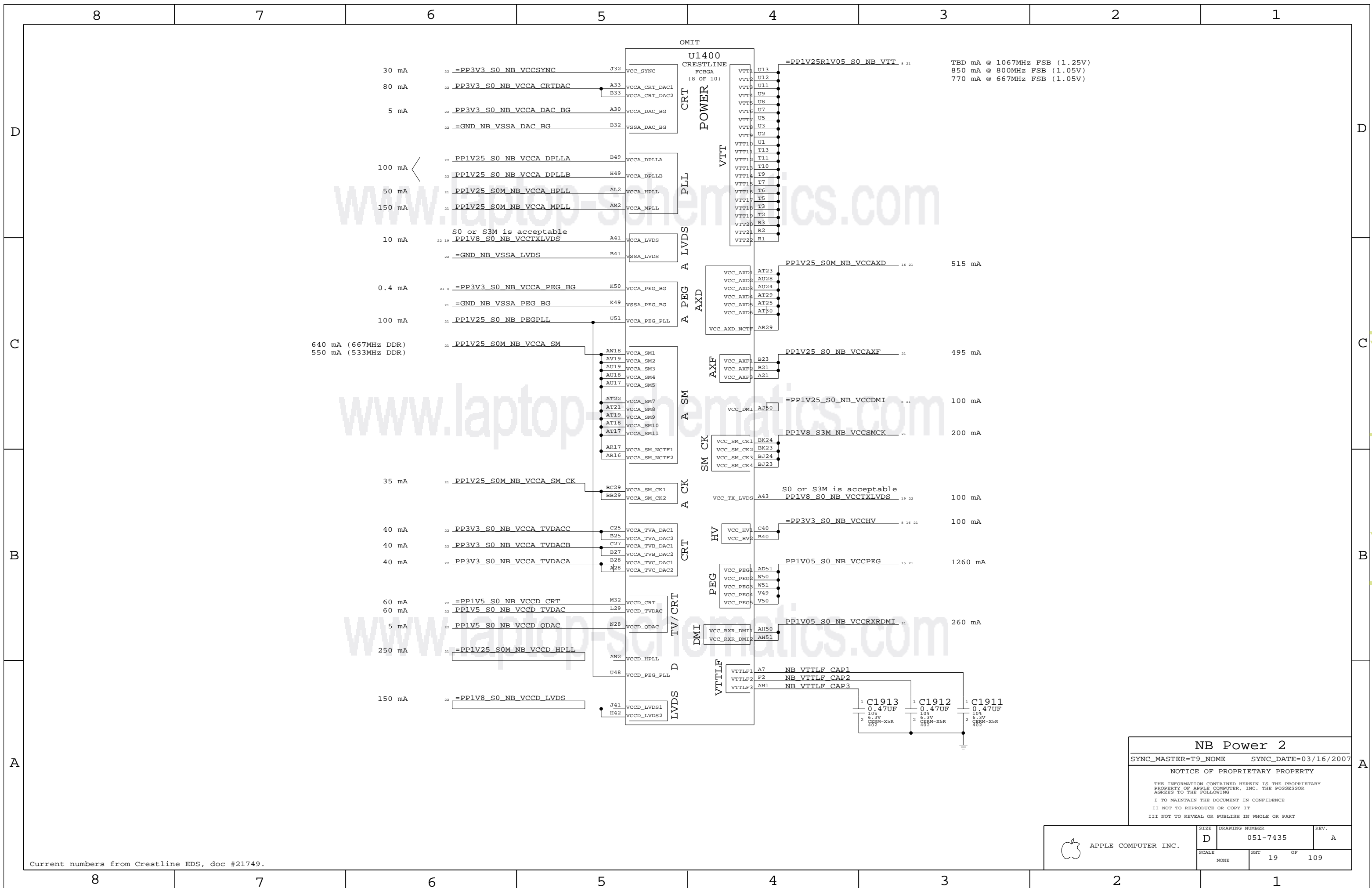


NB Power 1
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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| APPLE COMPUTER INC. | SCALE | SHT | OF | REV. |
| | NONE | 18 | 109 | A |

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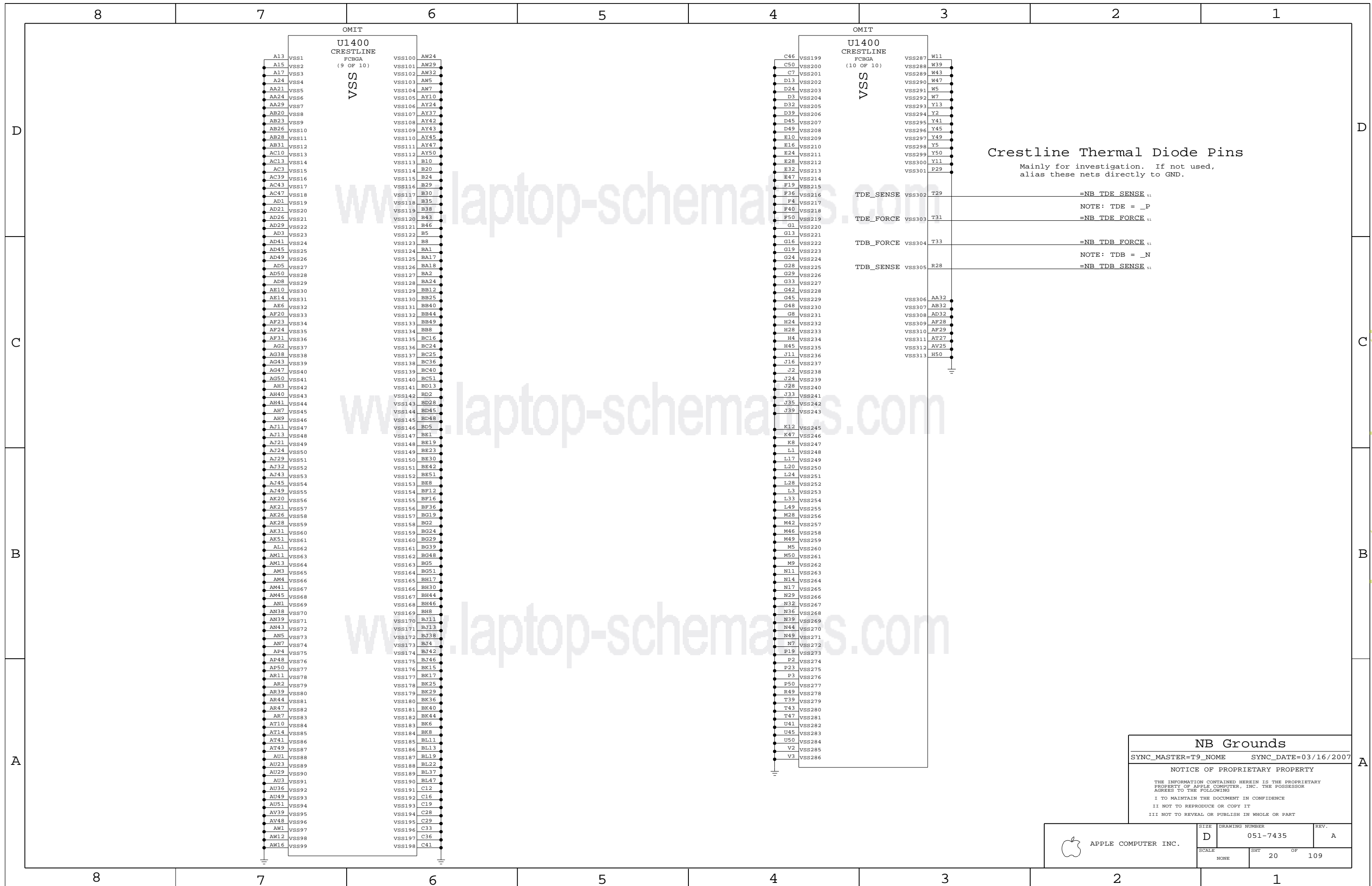


Current numbers from Crestline EDS, doc #21749.

NB Power 2
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007
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| NONE | 19 | 109 | |

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Crestline Thermal Diode Pins
 Mainly for investigation. If not used,
 alias these nets directly to GND.

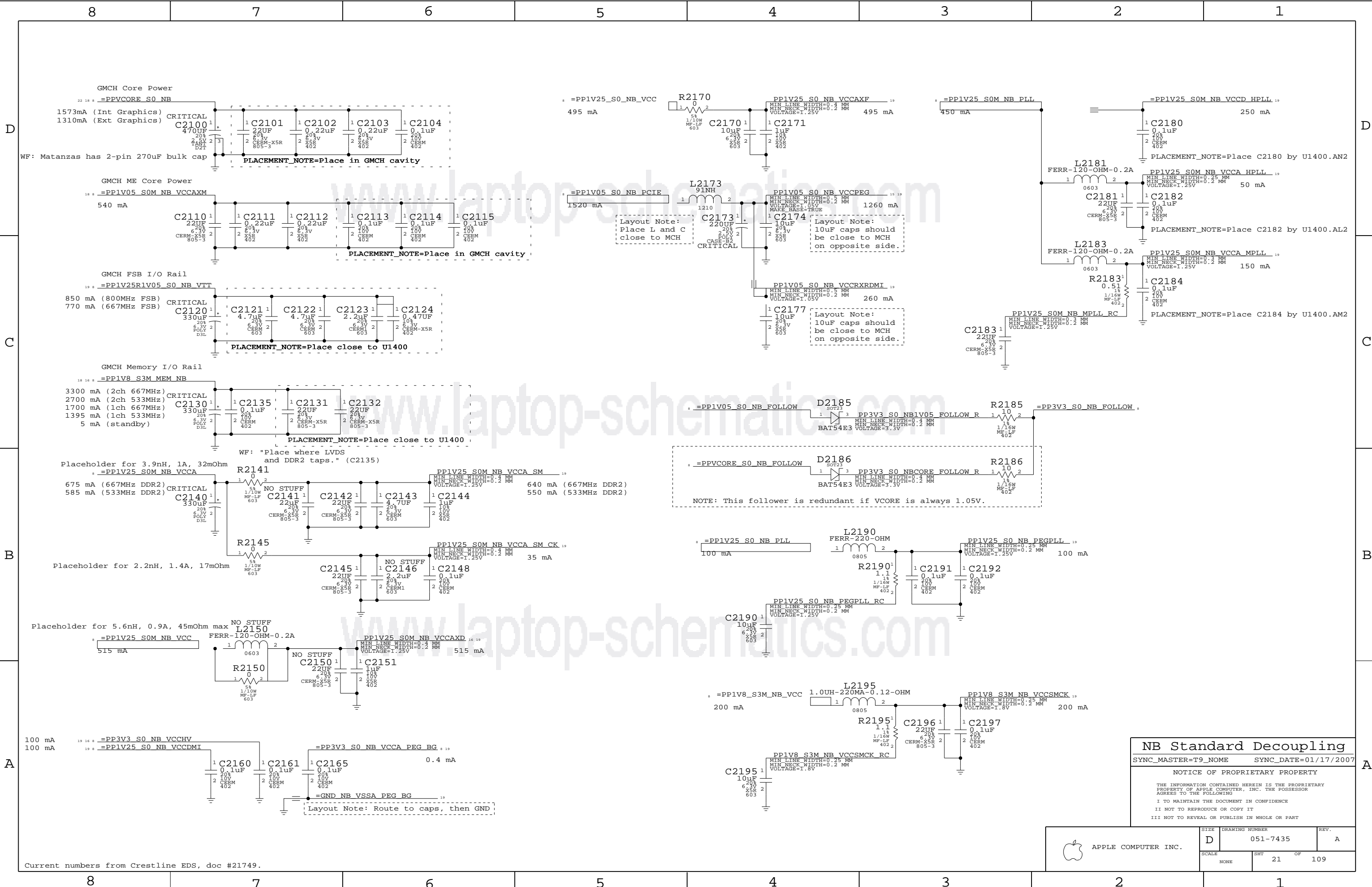
TDE_SENSE VSS302 T29 =NB TDE_SENSE s1
 NOTE: TDE = _P
 TDE_FORCE VSS303 T31 =NB TDE_FORCE s1
 TDB_FORCE VSS304 T33 =NB TDB_FORCE s1
 NOTE: TDB = _N
 TDB_SENSE VSS305 R28 =NB TDB_SENSE s1

NB Grounds
 SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007
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| SCALE | SHT 20 OF 109 | | |
| NONE | | | |

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D

C

B

A

D

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NB Standard Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

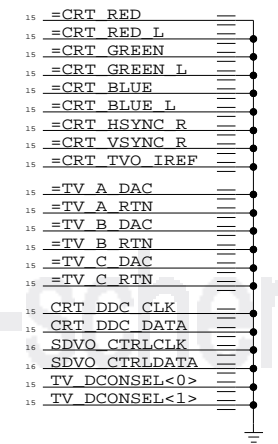
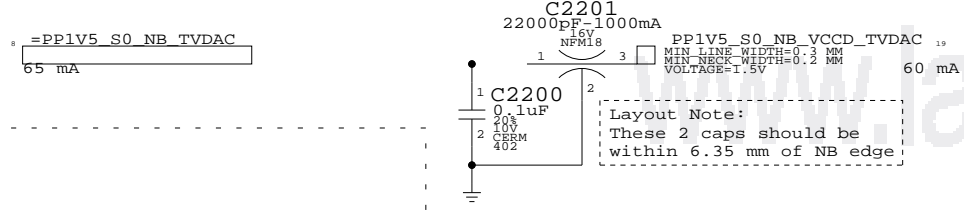
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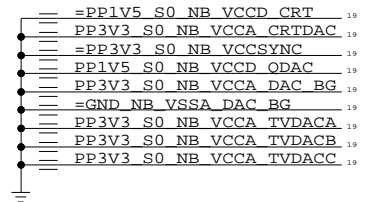
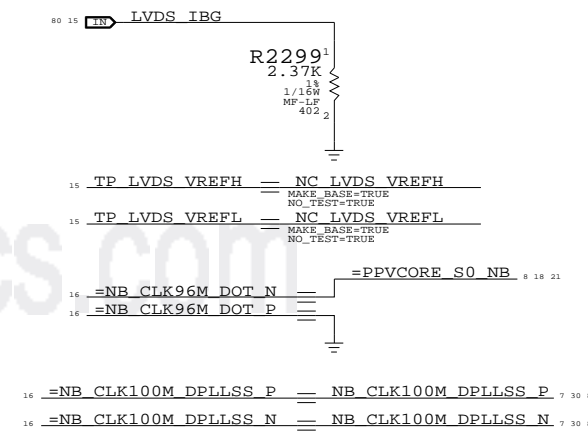
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| SCALE | SHT | OF | REV. |
| NONE | 21 | 109 | |

Current numbers from Crestline EDS, doc #21749.

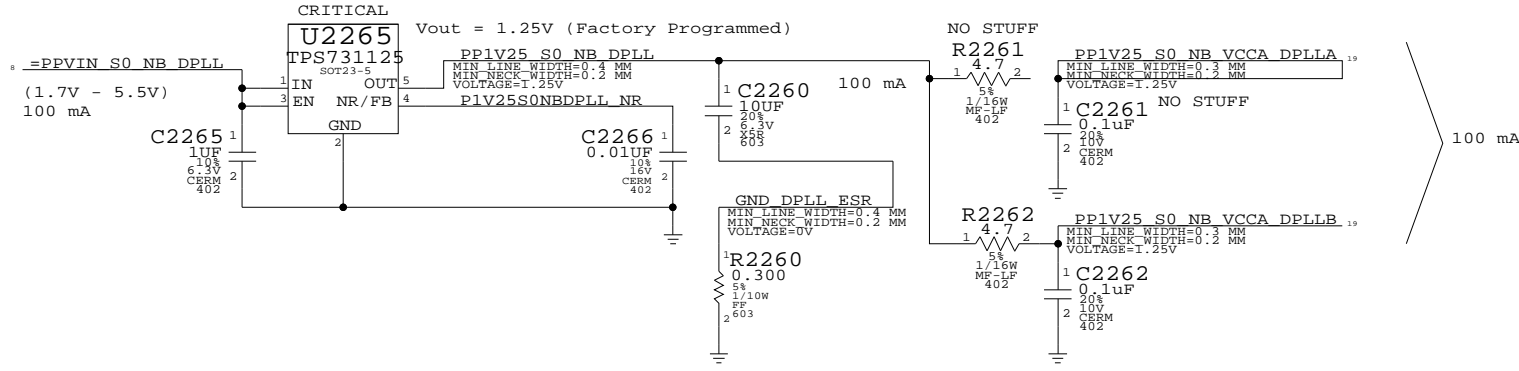
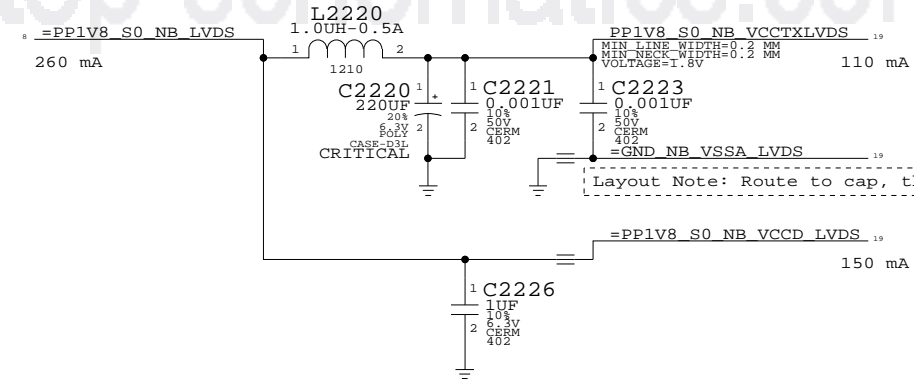
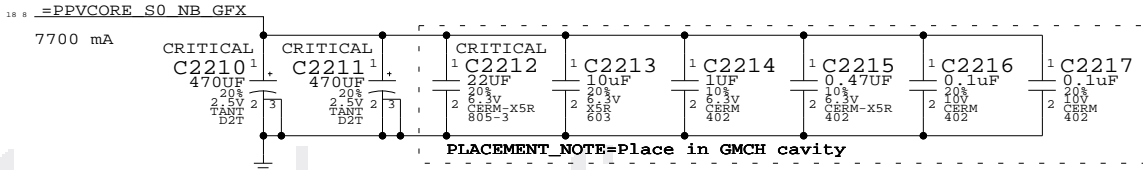
NOTE: This filter is required even if using only external graphics.
 VCCD_TVDAC also powers internal thermal sensors.



Crestline LVDS Support



GMCH Graphics Core Power



NB Graphics Decoupling

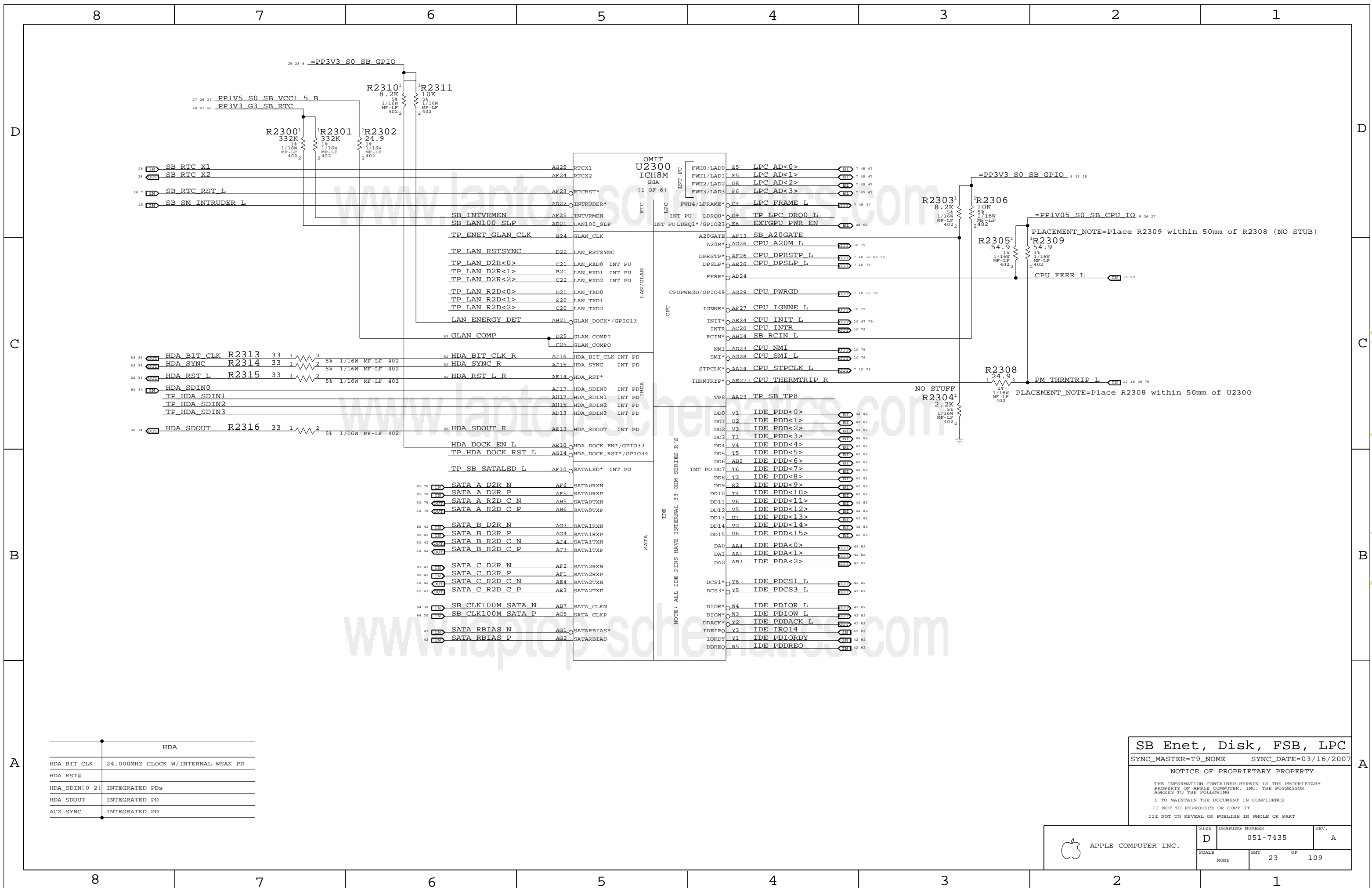
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| NONE | 22 | 109 | |

Current numbers from Crestline EDS Addendum, doc #20127.

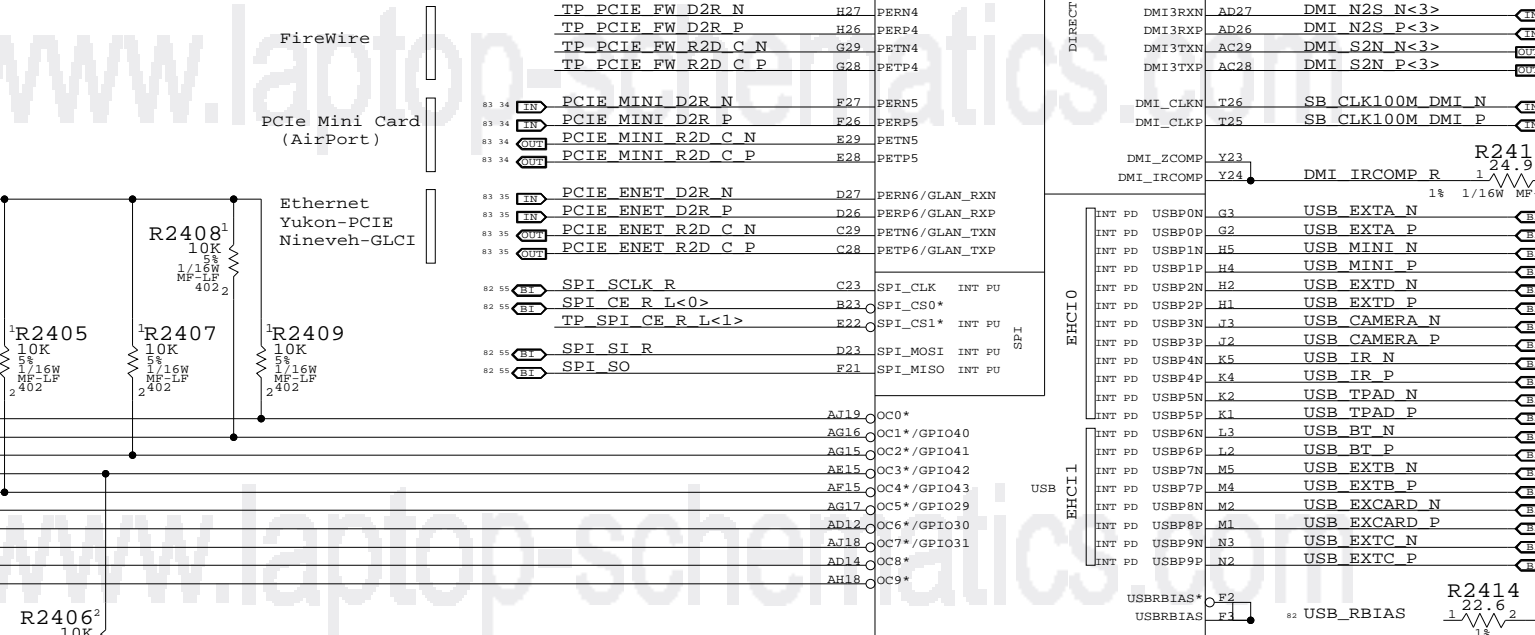
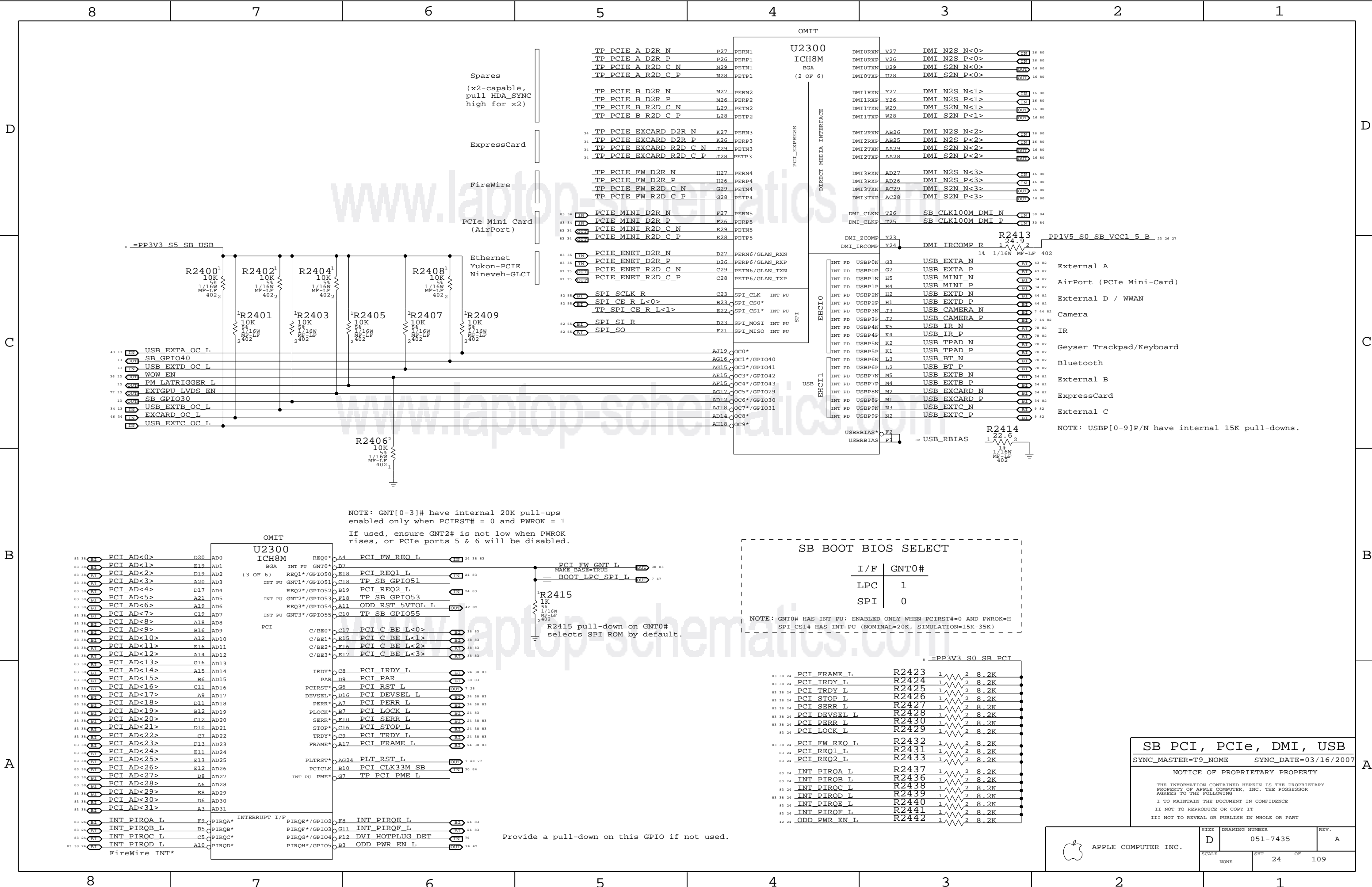


| HDA | |
|---------------|------------------------------------|
| HDA_BIT_CLK | 24.000MHZ CLOCK W/INTERNAL WEAK PD |
| HDA_RST# | |
| HDA_SDIN[0-2] | INTEGRATED PDs |
| HDA_SDOUT | INTEGRATED PD |
| ACZ_SYNC | INTEGRATED PD |

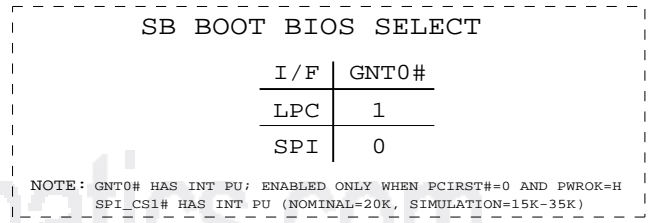
SB Enet, Disk, FSB, LPC
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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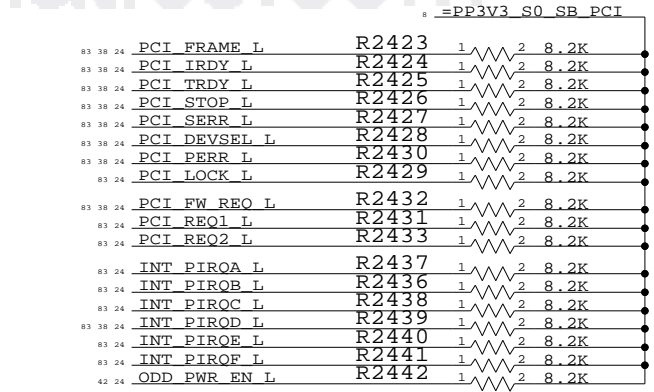
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| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-7435 | REV. A |
| | SCALE NONE | SHEET 23 | OF 109 |



NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.



NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H. SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

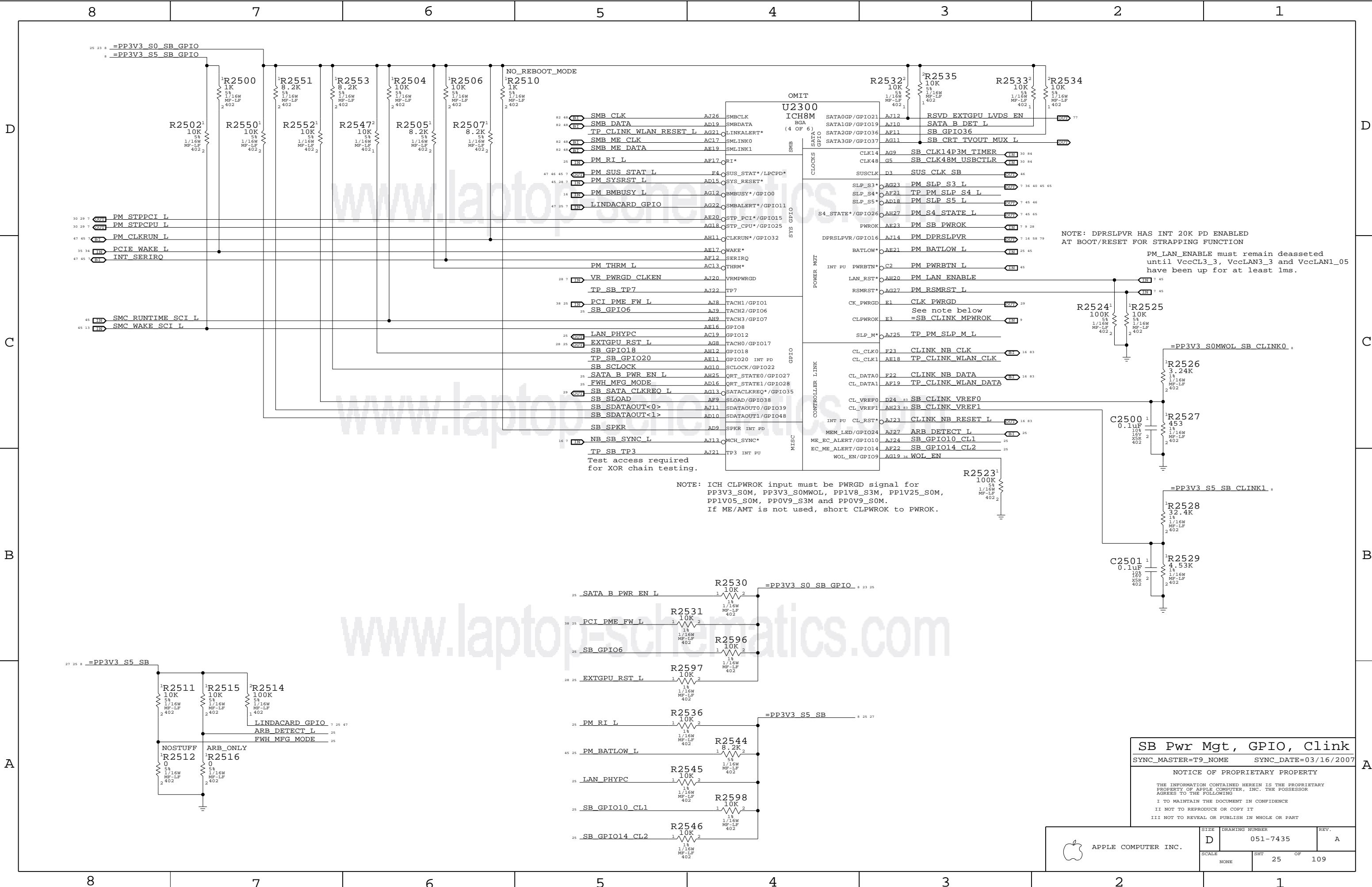


SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007

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| NONE | 24 | | |

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NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasserted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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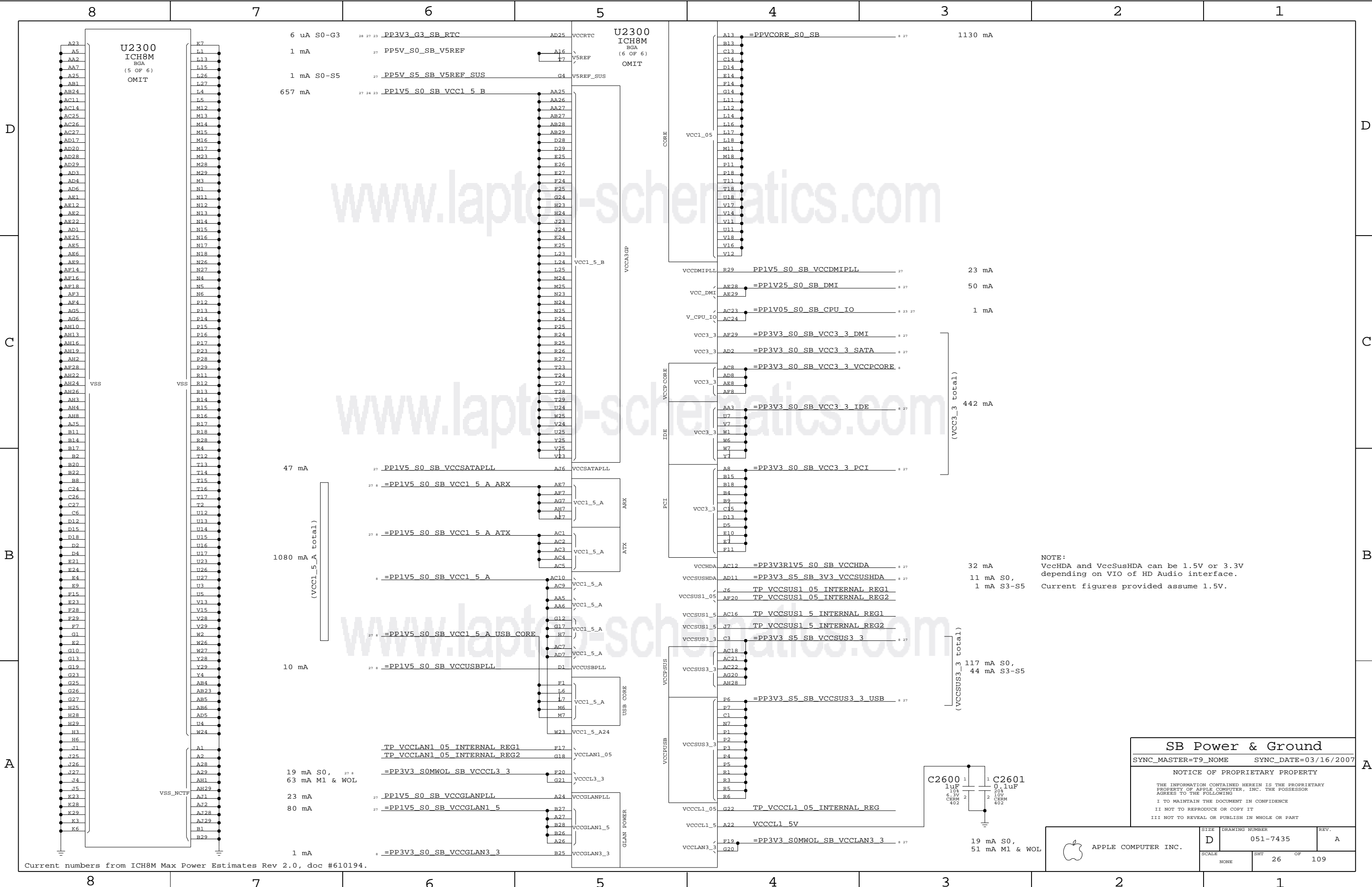
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| NONE | 25 | | |

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SB Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

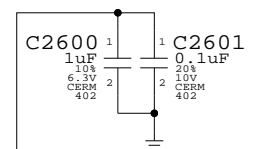
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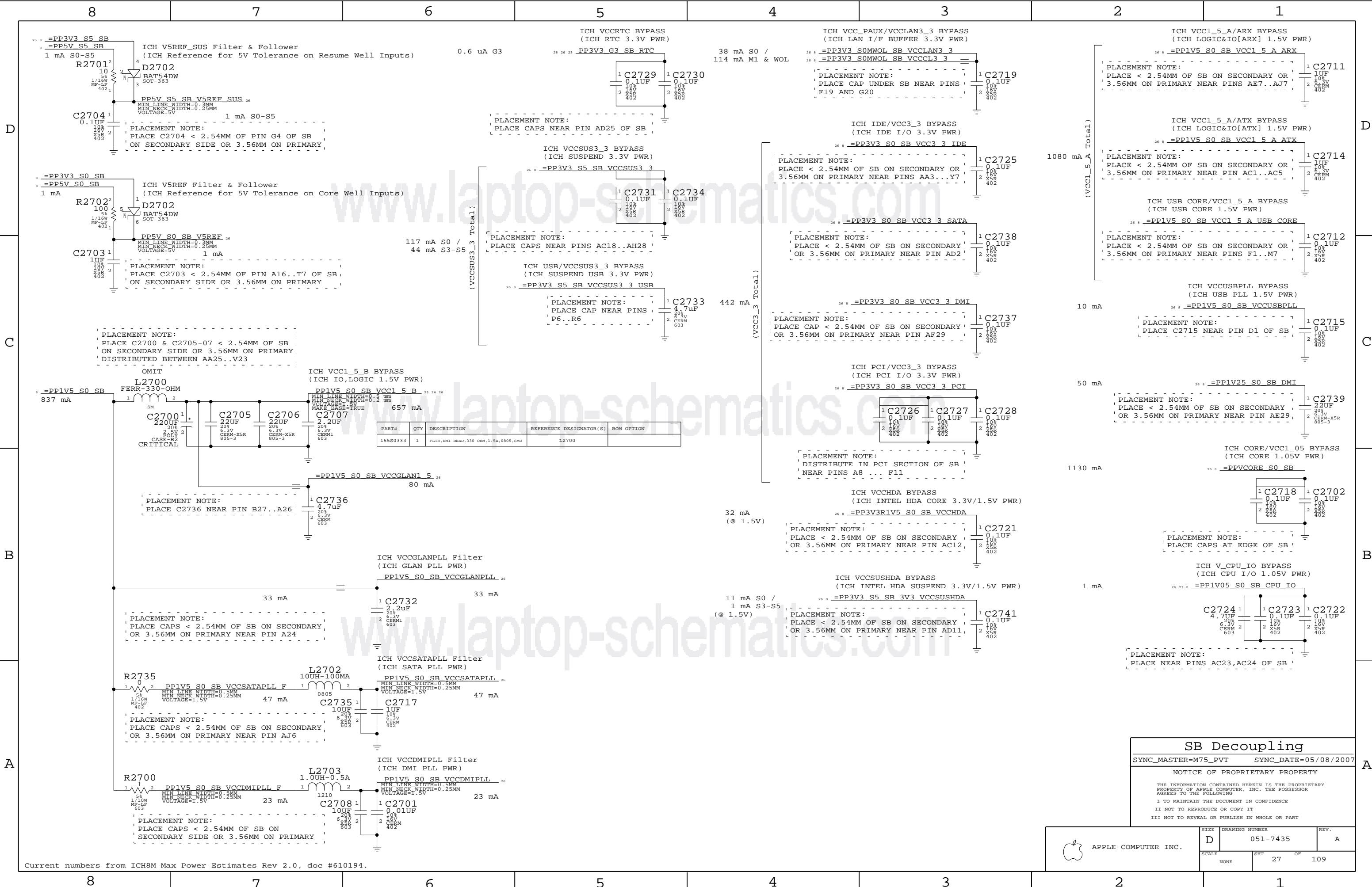
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| D | 051-7435 | A |
| SCALE | SHT | OF |
| NONE | 26 | 109 |



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19 mA S0,
51 mA M1 & WOL



SB Decoupling

SYNC_MASTER=M75_PVT SYNC_DATE=05/08/2007

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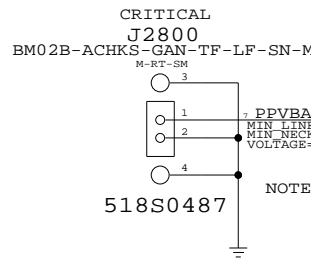
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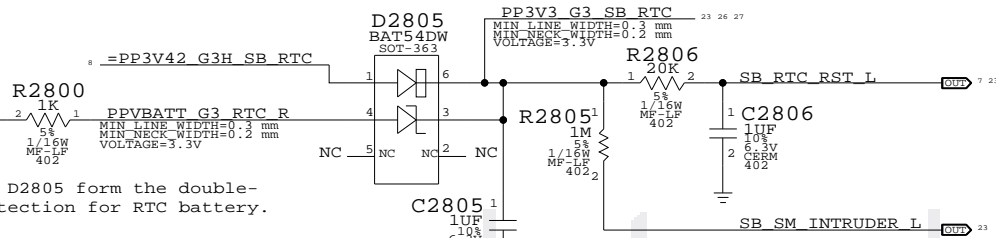
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

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Coin-Cell Connector

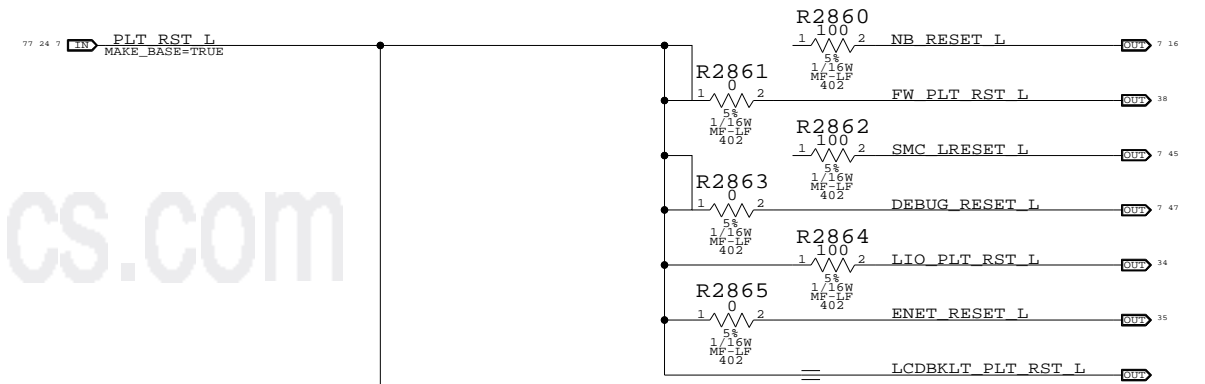


RTC Power Sources

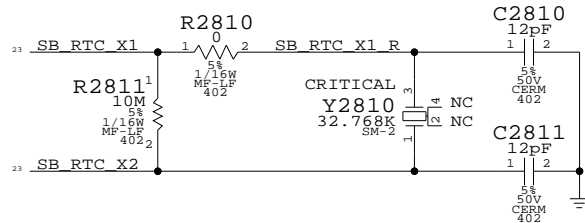


Platform Reset Connections

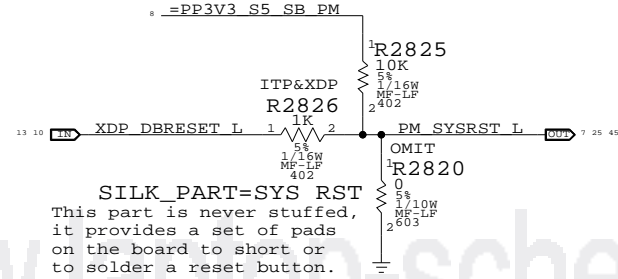
Unbuffered



SB RTC Crystal

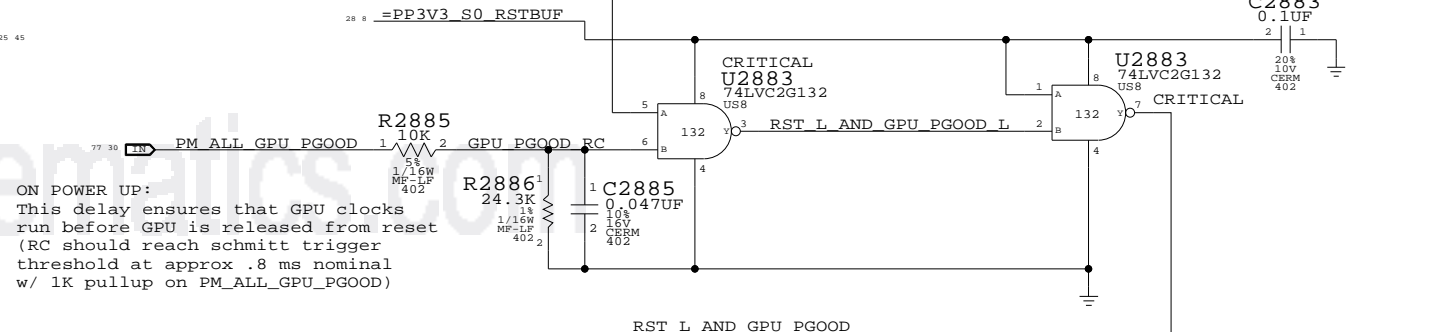


System Reset "Button"



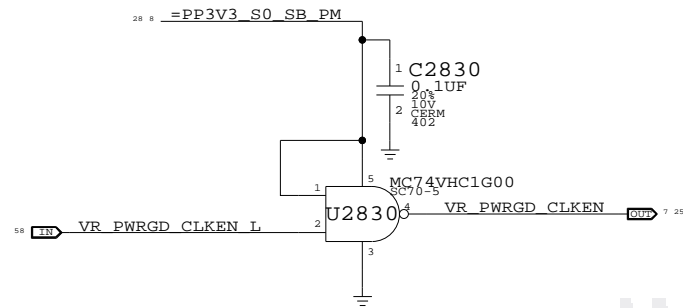
SILK_PART=SYS_RST
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Muxed GFX GPU Reset Support

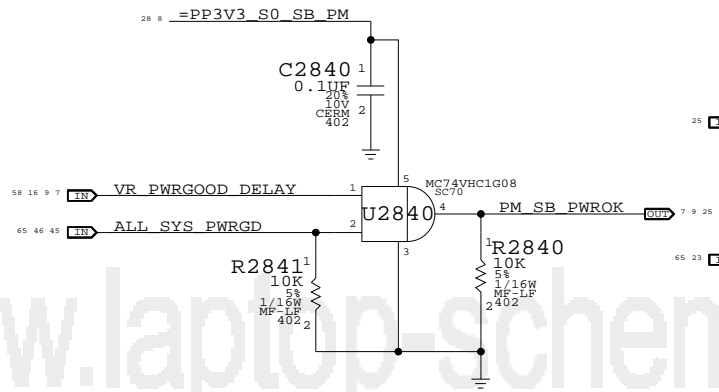


ON POWER UP:
This delay ensures that GPU clocks run before GPU is released from reset (RC should reach schmitt trigger threshold at approx .8 ms nominal w/ 1K pullup on PM_ALL_GPU_PGOOD)

VRMPWRGD Inverter



PWROK Circuit

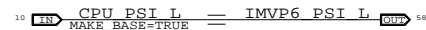


ON POWER DOWN:
This ensures that GPU is put into reset while chip is still powered and clocks are still running.

PCI Reset Connections



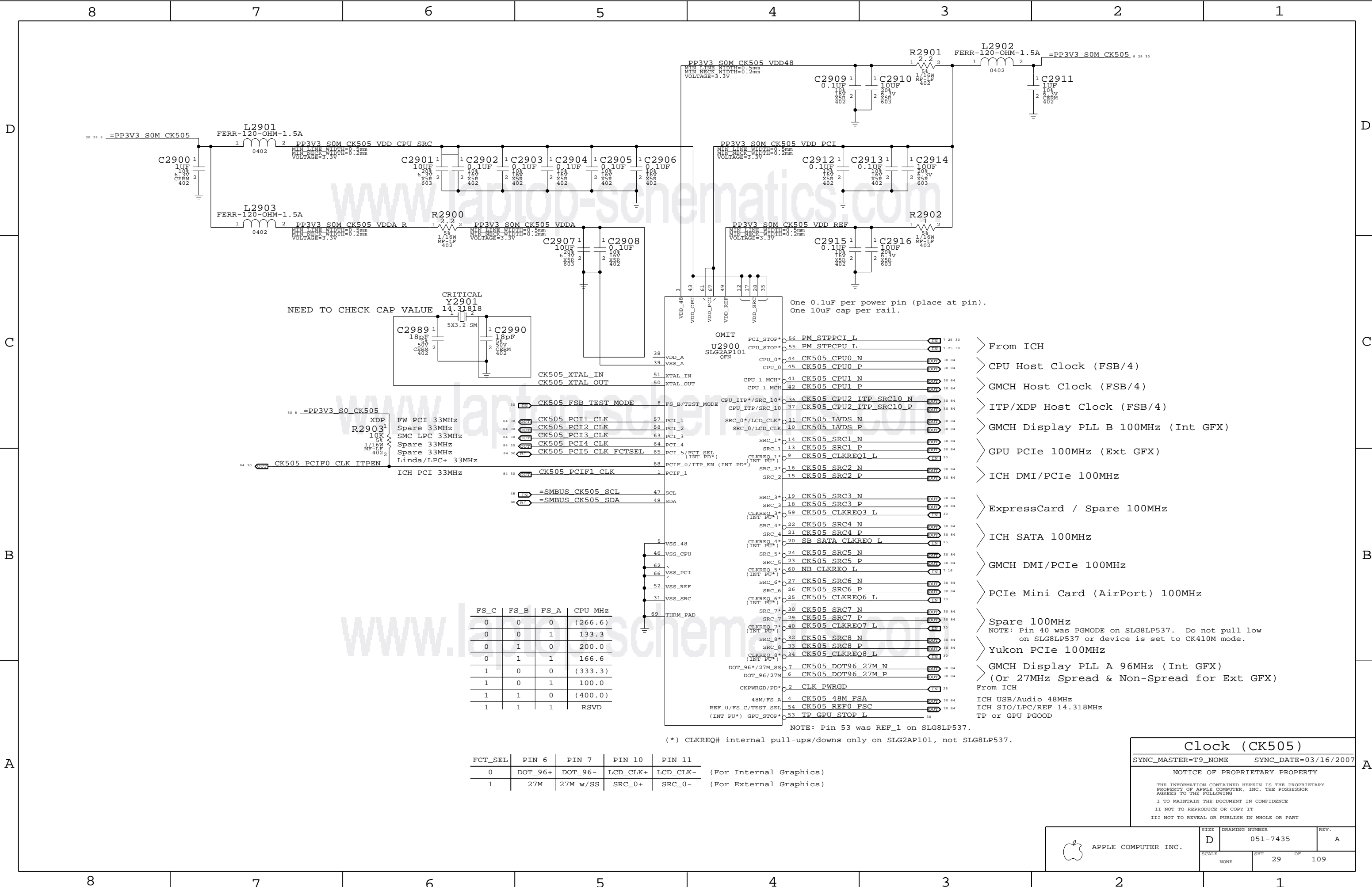
CPU VCore ForcePSI



| SB Misc | | |
|--|----------------------|--|
| SYNC_MASTER=(T9_MLB) | SYNC_DATE=08/24/2006 | |
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NEED TO CHECK CAP VALUE

CRITICAL
Y2901
14.31818

C2989 18pF 50V CERM 402
C2990 18pF 50V CERM 402

One 0.1uF per power pin (place at pin).
One 10uF cap per rail.

| FS_C | FS_B | FS_A | CPU MHz |
|------|------|------|---------|
| 0 | 0 | 0 | (266.6) |
| 0 | 0 | 1 | 133.3 |
| 0 | 1 | 0 | 200.0 |
| 0 | 1 | 1 | 166.6 |
| 1 | 0 | 0 | (333.3) |
| 1 | 0 | 1 | 100.0 |
| 1 | 1 | 0 | (400.0) |
| 1 | 1 | 1 | RSVD |

| FCT_SEL | PIN 6 | PIN 7 | PIN 10 | PIN 11 | |
|---------|---------|----------|----------|----------|-------------------------|
| 0 | DOT_96+ | DOT_96- | LCD_CLK+ | LCD_CLK- | (For Internal Graphics) |
| 1 | 27M | 27M w/SS | SRC_0+ | SRC_0- | (For External Graphics) |

- > From ICH
- > CPU Host Clock (FSB/4)
- > GMCH Host Clock (FSB/4)
- > ITP/XDP Host Clock (FSB/4)
- > GMCH Display PLL B 100MHz (Int GFX)
- > GPU PCIe 100MHz (Ext GFX)
- > ICH DMI/PCIe 100MHz
- > ExpressCard / Spare 100MHz
- > ICH SATA 100MHz
- > GMCH DMI/PCIe 100MHz
- > PCIe Mini Card (AirPort) 100MHz
- > Spare 100MHz
NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
- > Yukon PCIe 100MHz
- > GMCH Display PLL A 96MHz (Int GFX)
(Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- > ICH USB/Audio 48MHz
- > ICH SIO/LPC/REF 14.318MHz
- > TP or GPU PGOOD

NOTE: Pin 53 was REF_1 on SLG8LP537.

(*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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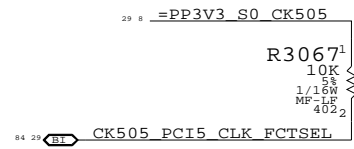
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CLK Termination

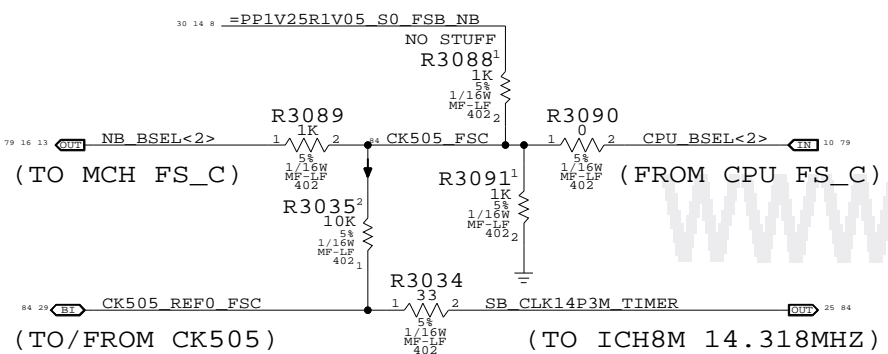
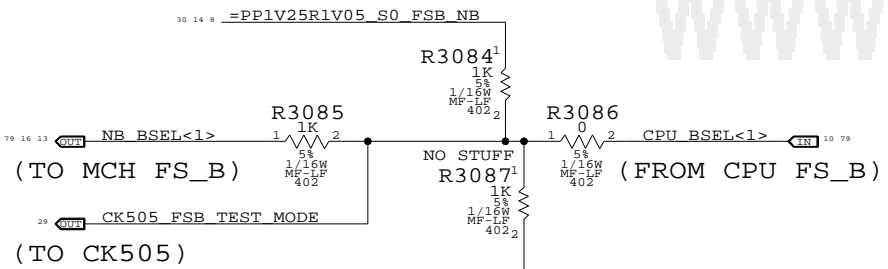
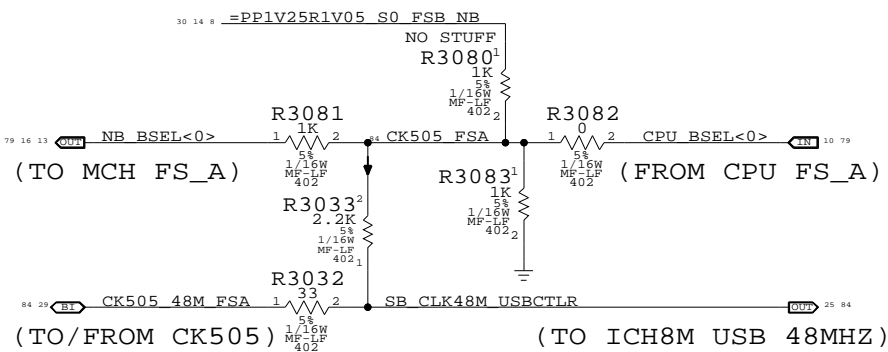
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

CK505 Configuration Straps

FCT_SEL (GFX clock select)



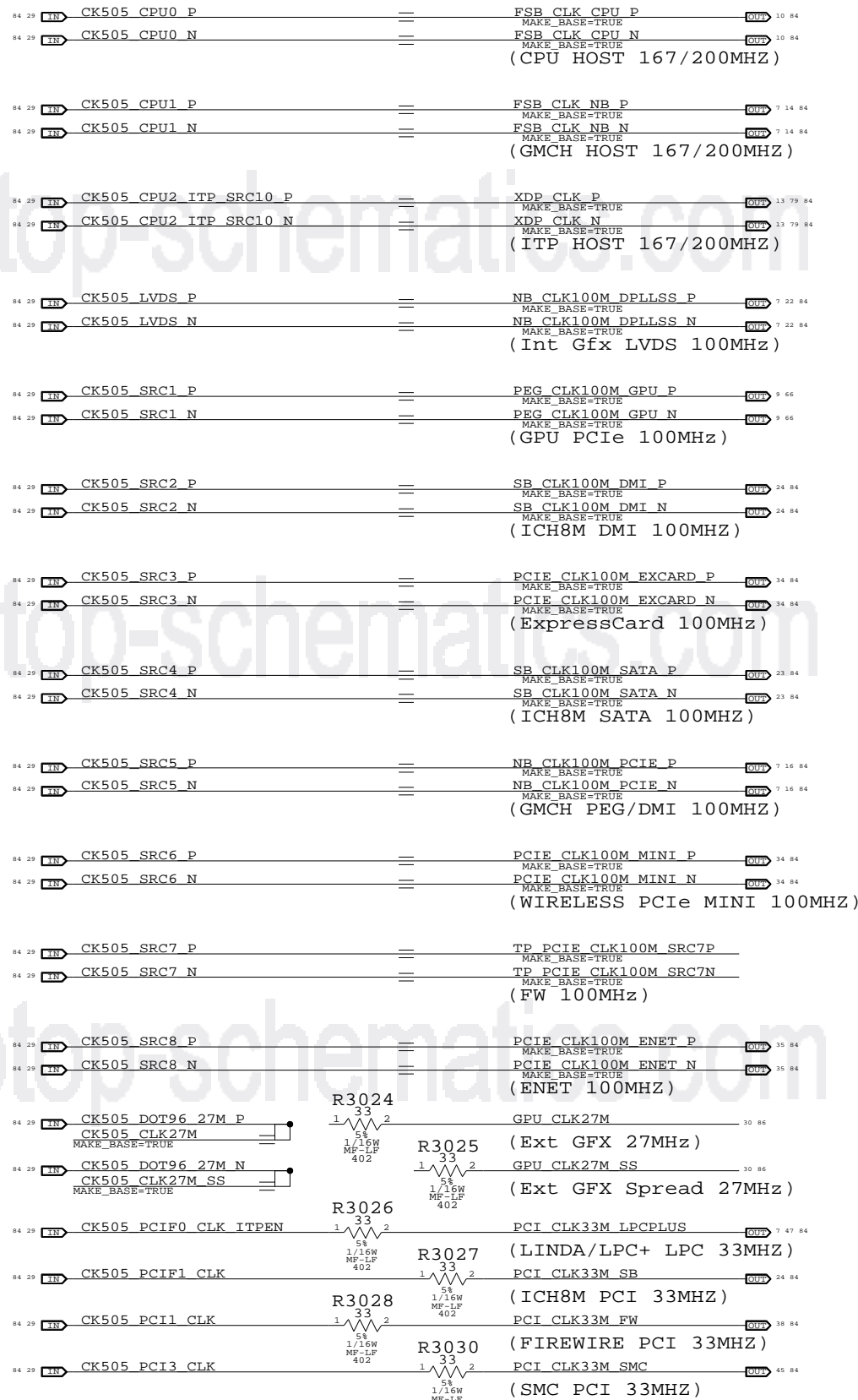
FS_A, FS_B, FS_C (Host clock freq select)



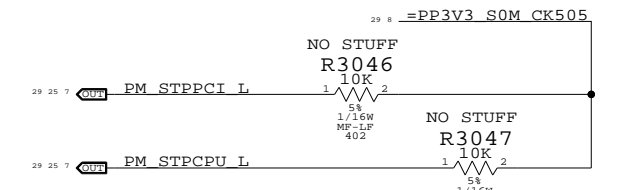
| FS_C | FS_B | FS_A | CPU MHz |
|------|------|------|---------|
| 0 | 0 | 0 | (266.6) |
| 0 | 0 | 1 | 133.3 |
| 0 | 1 | 0 | 200.0 |
| 0 | 1 | 1 | 166.6 |
| 1 | 0 | 0 | (333.3) |
| 1 | 0 | 1 | 100.0 |
| 1 | 1 | 0 | (400.0) |
| 1 | 1 | 1 | RSVD |

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

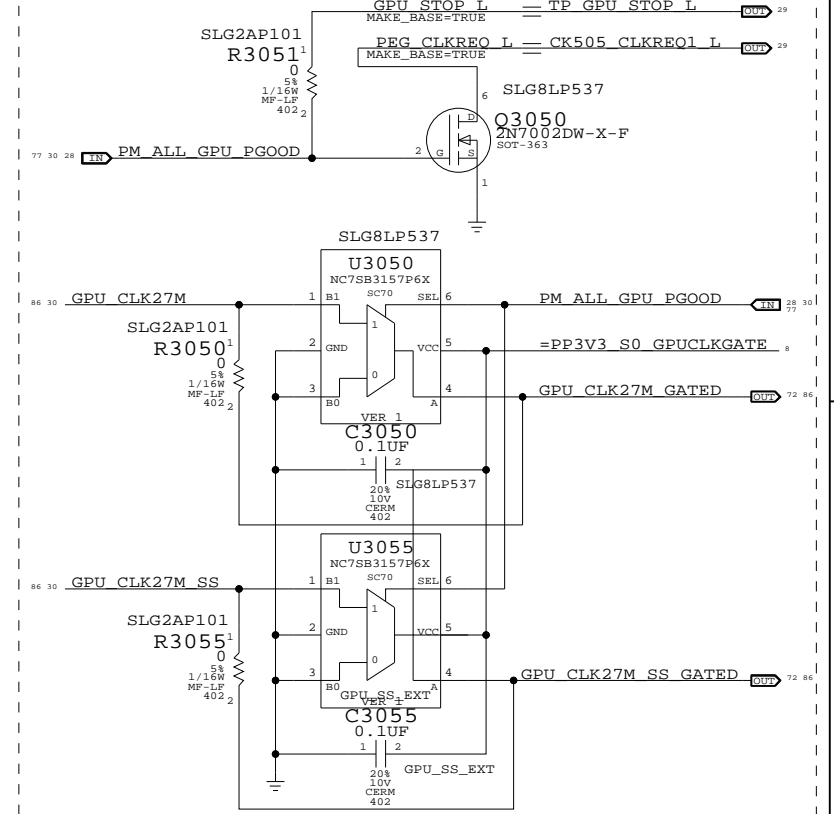


CLKREQ Controls

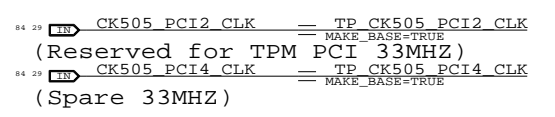


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

GPU Clock Gating



Unused Clocks



Clock Termination
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One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector

=PPOV9 SOM MEM TERM

D

D

C

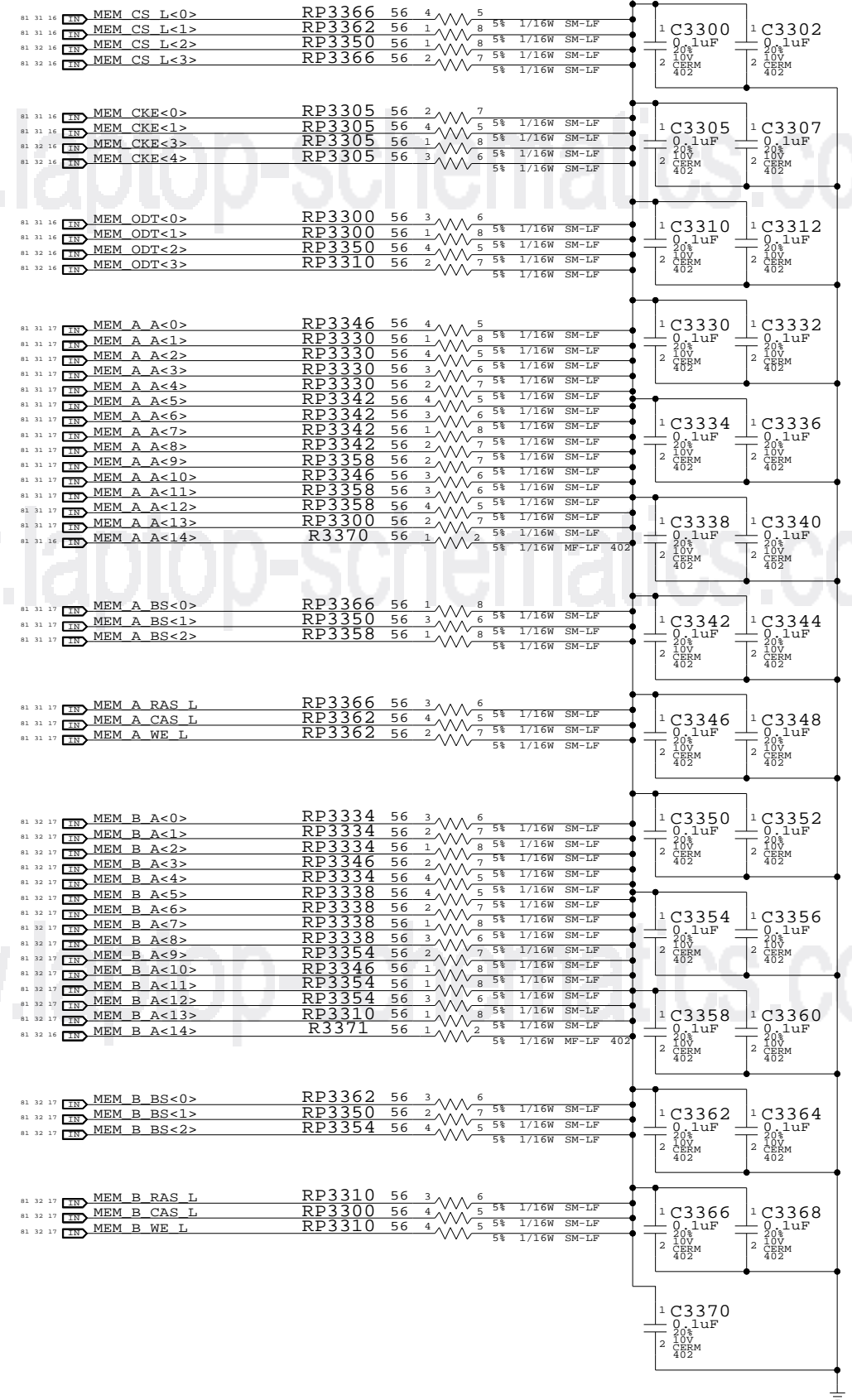
C

B

B

A

A



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

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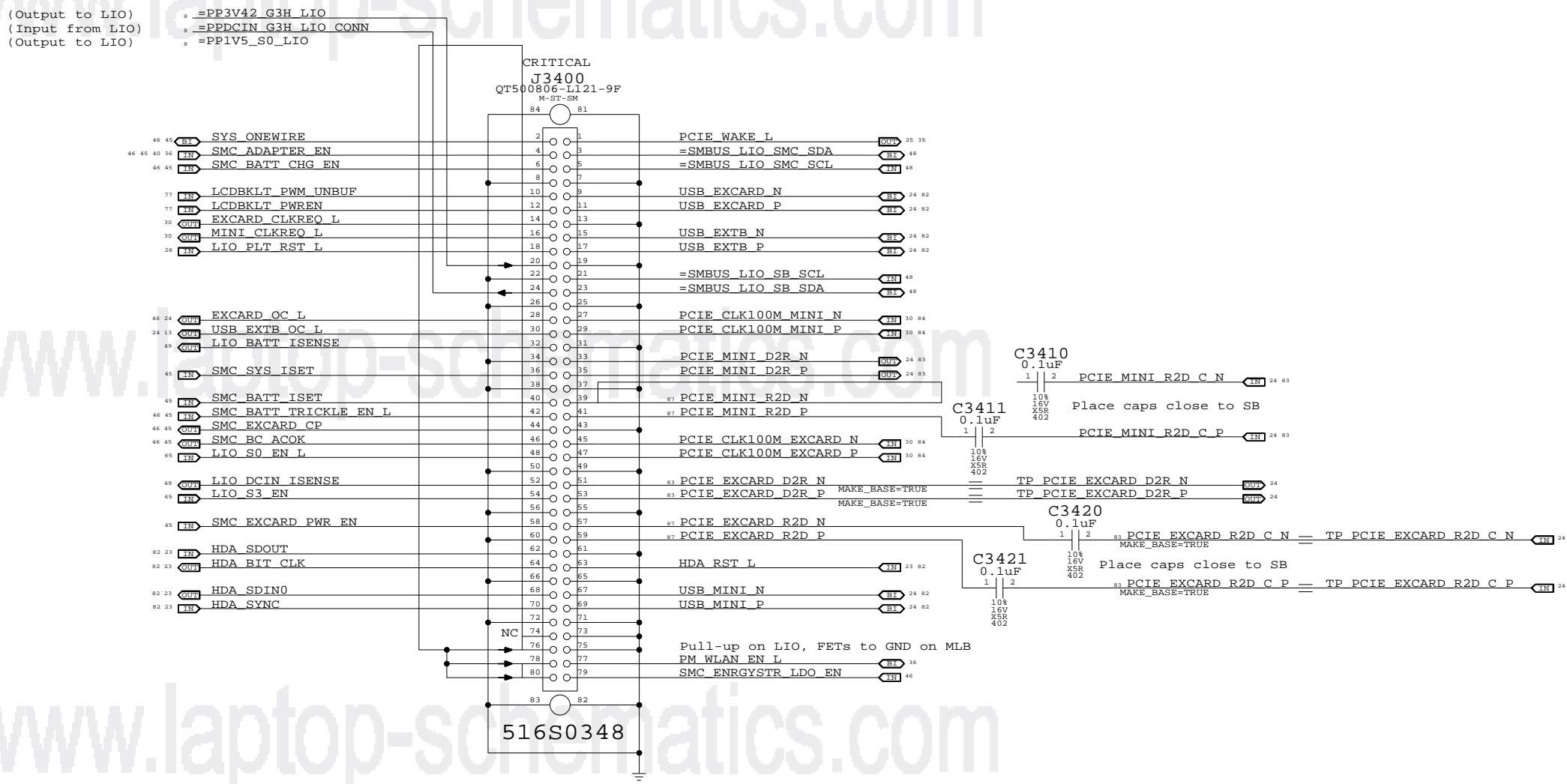
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| SCALE | SHT | OF | |
| NONE | 33 | 109 | |

Left I/O Board Connector

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Left I/O Board Connector
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| NONE | 34 | 109 | |

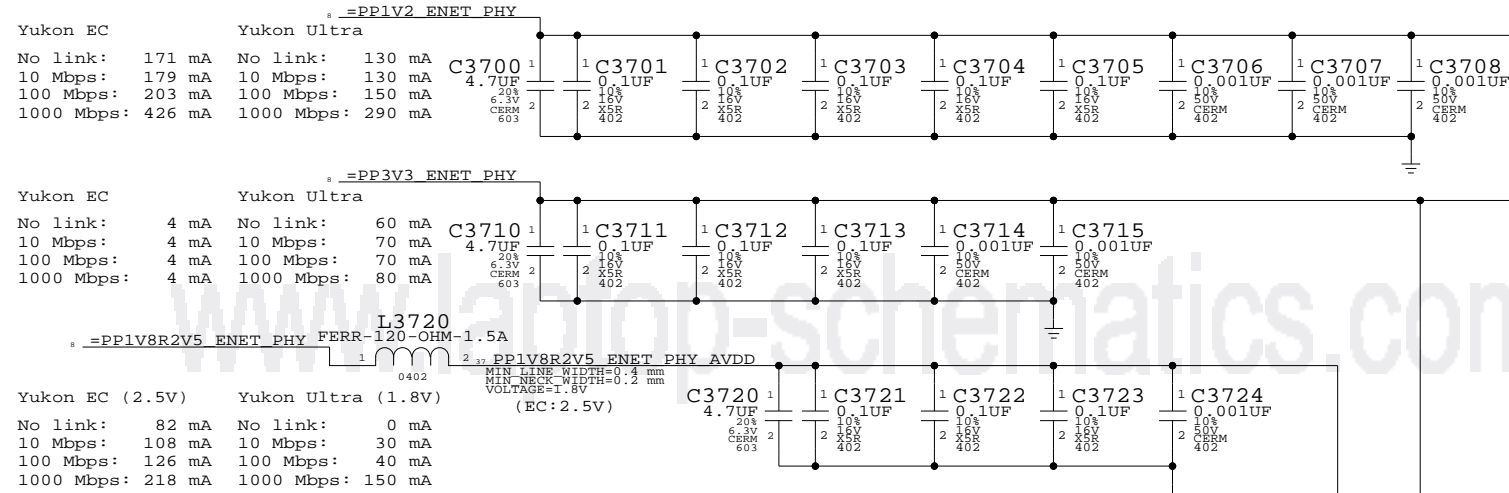
Page Notes

Power aliases required by this page:
 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY

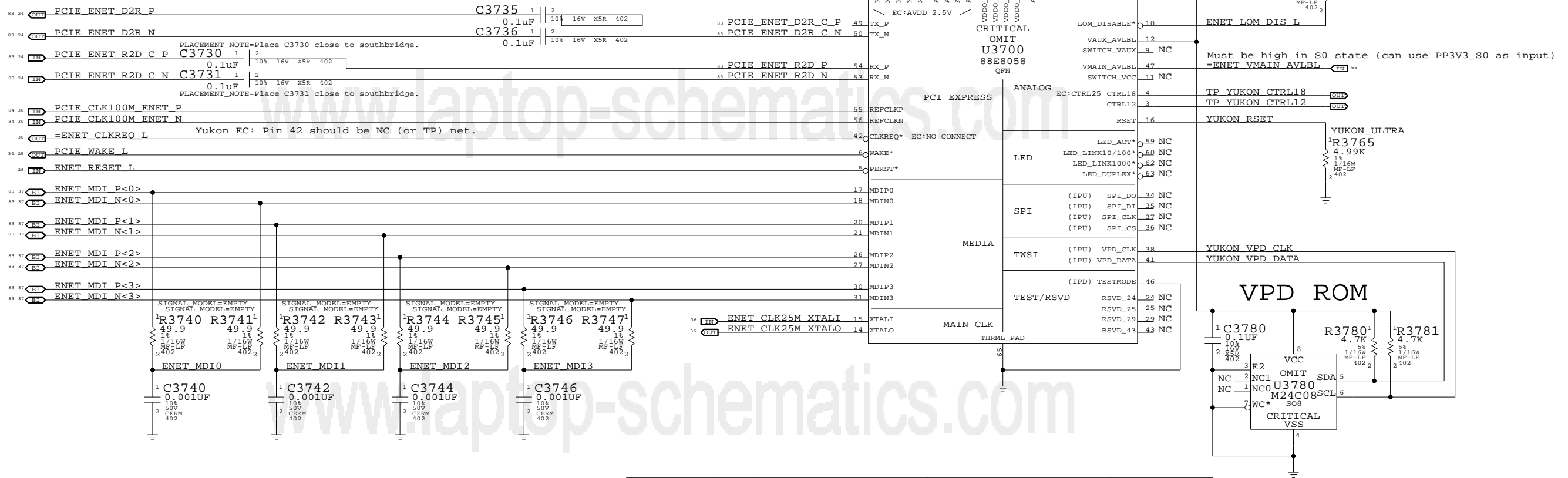
Signal aliases required by this page:
 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBLE (See note by pin)

BOM options provided by this page:
 YUKON_EC - Selects Yukon EC RSET value.
 YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



=YUKON_EC_PP2V5_ENET
 Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
 Yukon Ultra: Alias to GND



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---|---------------|----------|-------------|
| 338S0386 | 1 | IC, 88E8058, GIGABIT ENET XCVR, 64P QFN | U3700 | CRITICAL | YUKON_ULTRA |
| 341S2060 | 1 | IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08 | U3780 | CRITICAL | YUKON_ULTRA |
| 338S0270 | 1 | IC, 88E8053, GIGABIT ENET XCVR, 64P QFN | U3700 | CRITICAL | YUKON_EC |
| 341S1797 | 1 | IC, EEPROM, SERIAL IIC, 8KBIT, S08 | U3780 | CRITICAL | YUKON_EC |
| 114S0285 | 1 | RES, 4.87K, 1%, 1/16W, 0402, LF | R3760 | | YUKON_EC |

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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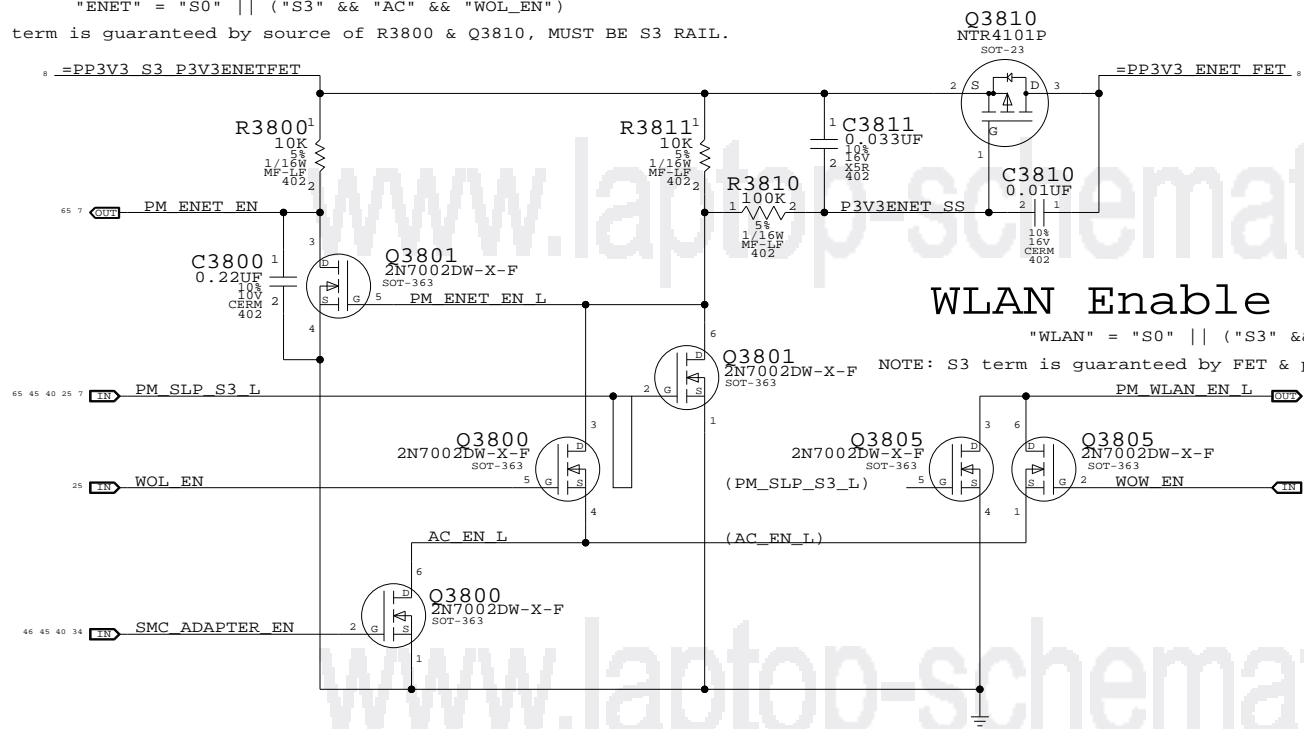
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ENET Enable Generation

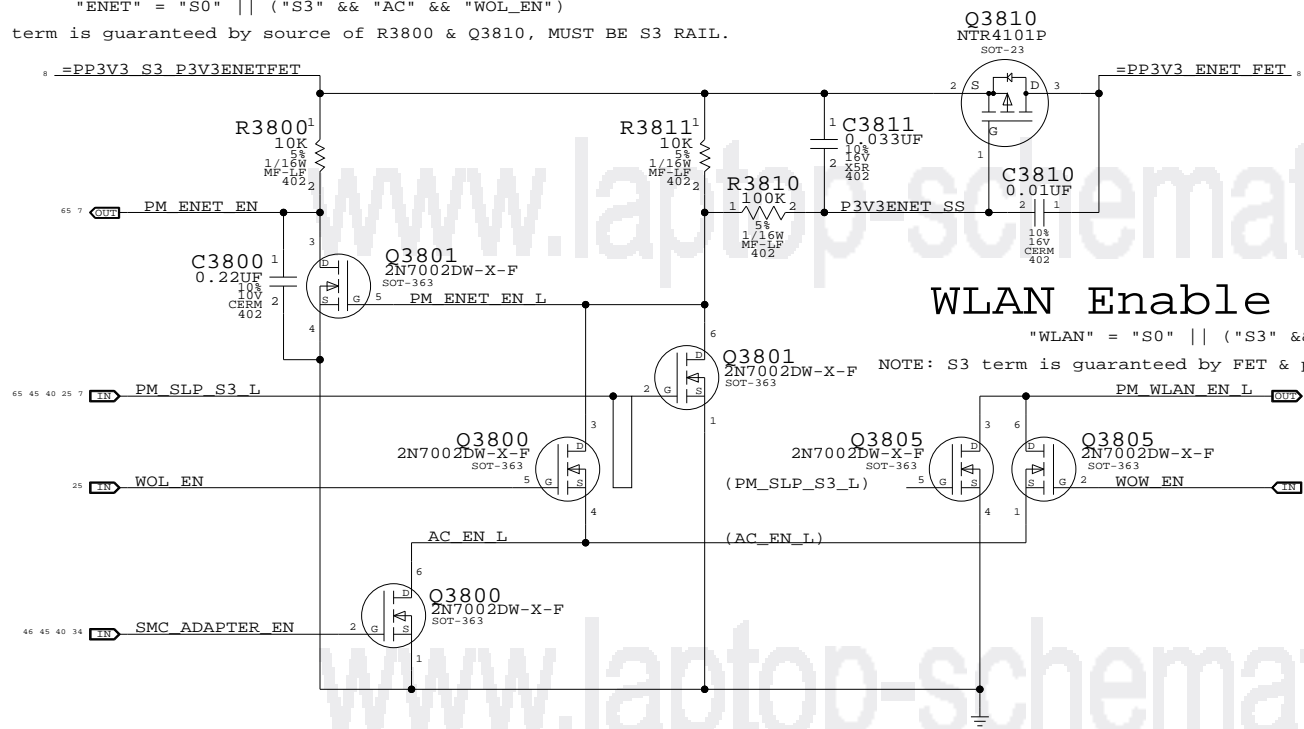
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

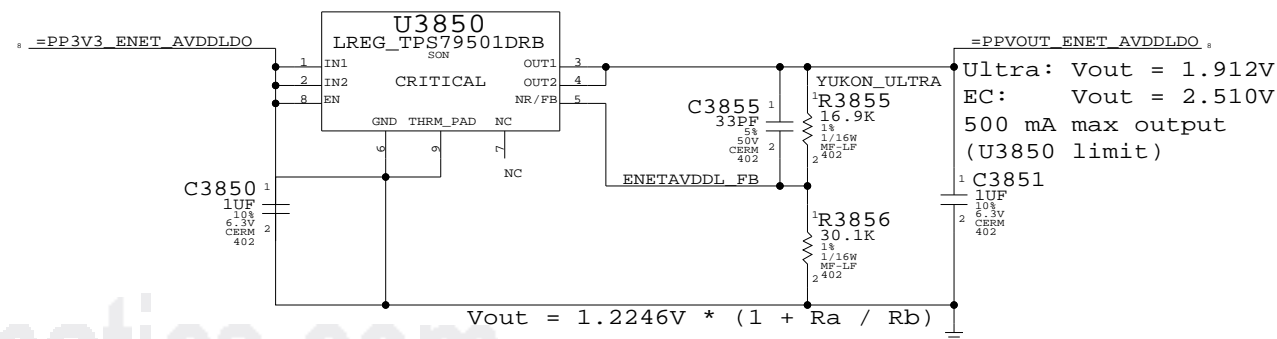
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

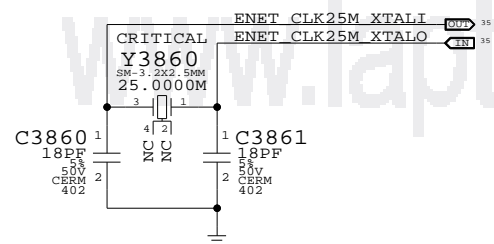


Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



Yukon Crystal



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------------|---------------|----------|------------|
| 114S0363 | 1 | RES,31.6K,1%,1/16W,402,LF | R3855 | | YUKON_EC |

Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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Page Notes

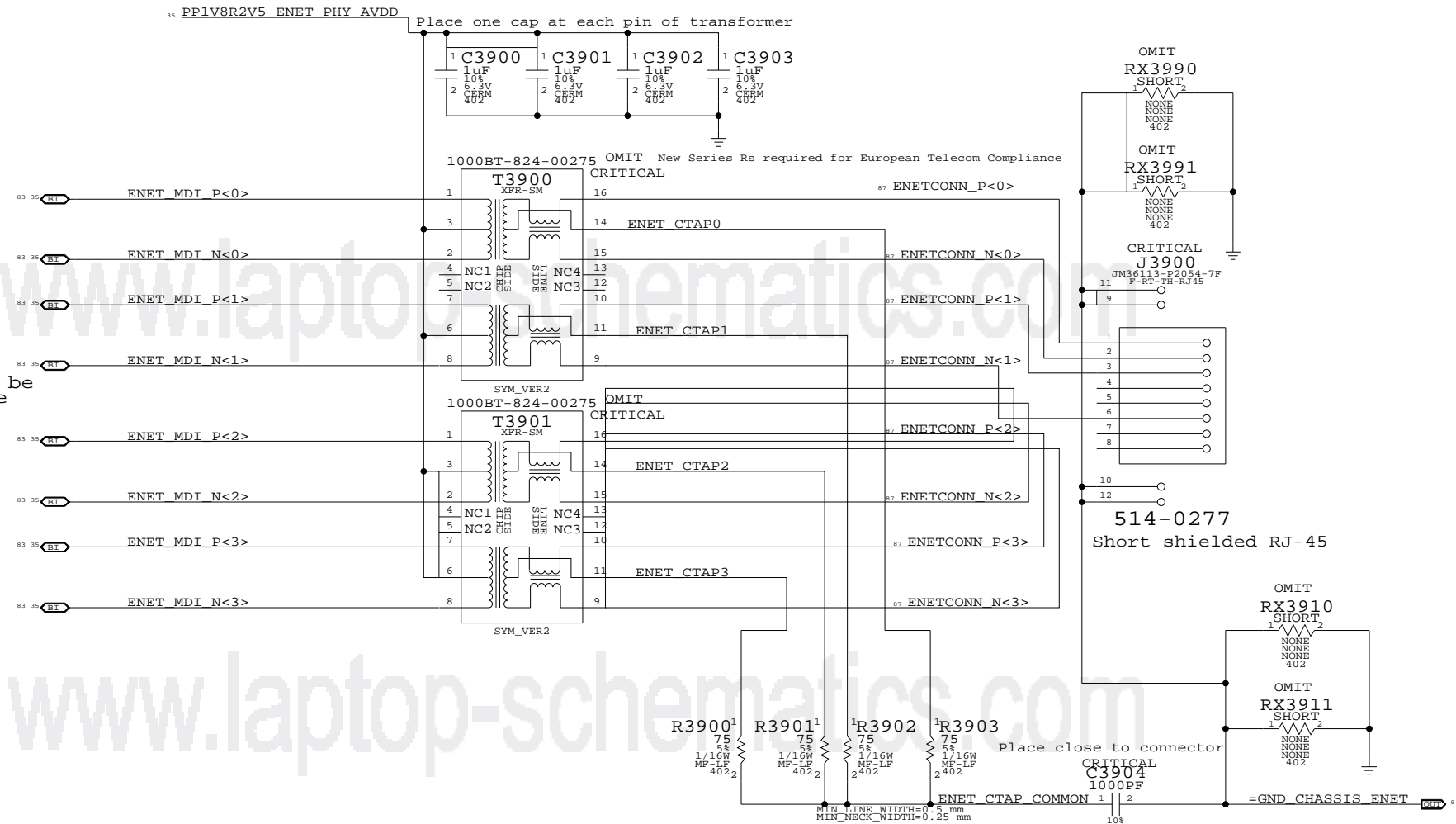
Power aliases required by this page:
 - =GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

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Transformers should be mirrored on opposite sides of the board



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------------|-------------------------|----------|------------|
| 15780030 | 2 | XPRM_ISO_HALF-PORT_1000T_16P_SMD_2MM | T3900, T3901 | CRITICAL | |

Ethernet Connector
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

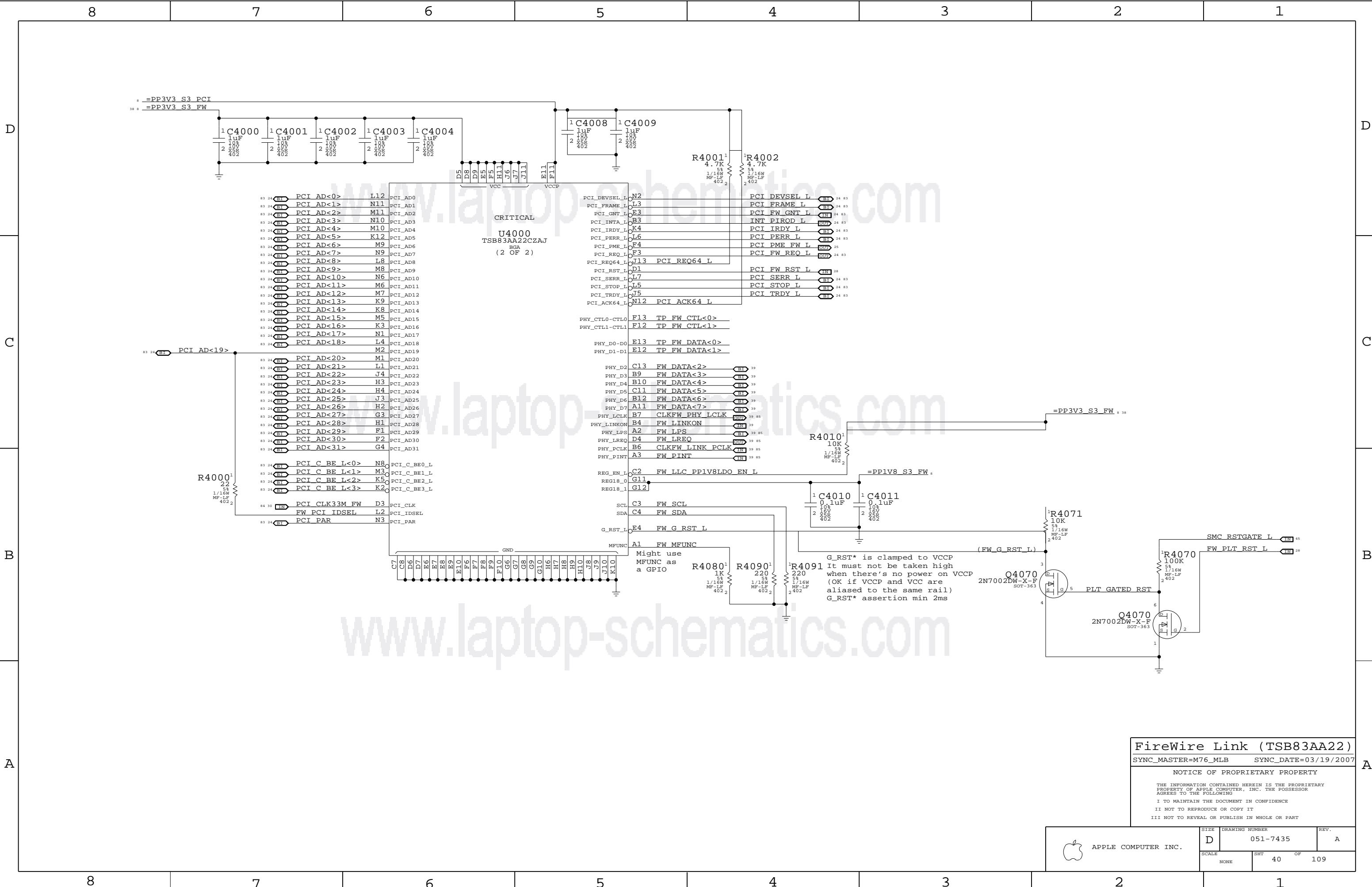
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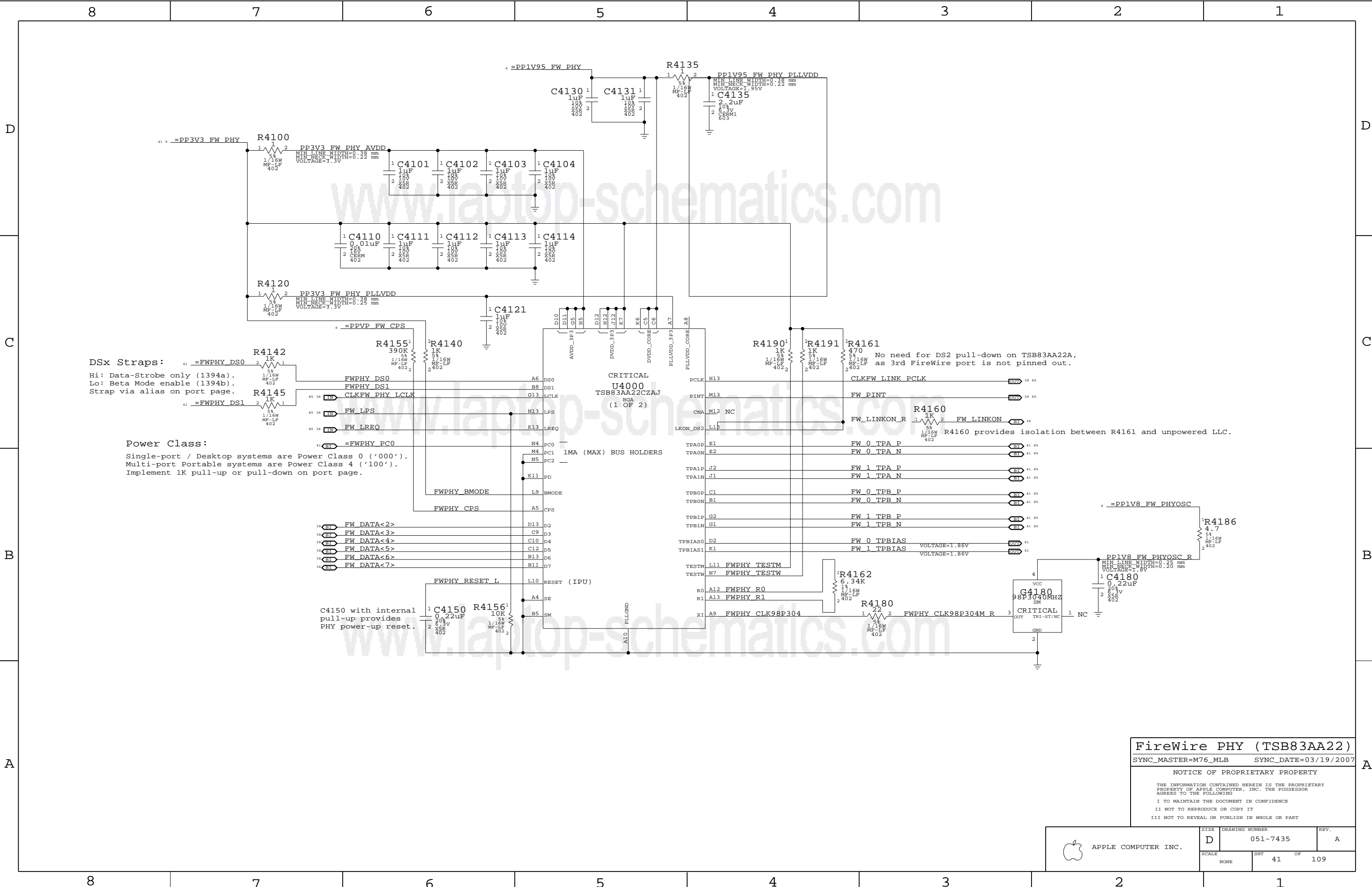
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FireWire Link (TSB83AA22)
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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DSx Straps:
 Hi: Data-Strobe only (1394a).
 Lo: Beta Mode enable (1394b).
 Strap via alias on port page.

Power Class:
 Single-port / Desktop systems are Power Class 0 ('000').
 Multi-port Portable systems are Power Class 4 ('100').
 Implement 1K pull-up or pull-down on port page.

No need for DS2 pull-down on TSB83AA22A,
 as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

FireWire PHY (TSB83AA22)
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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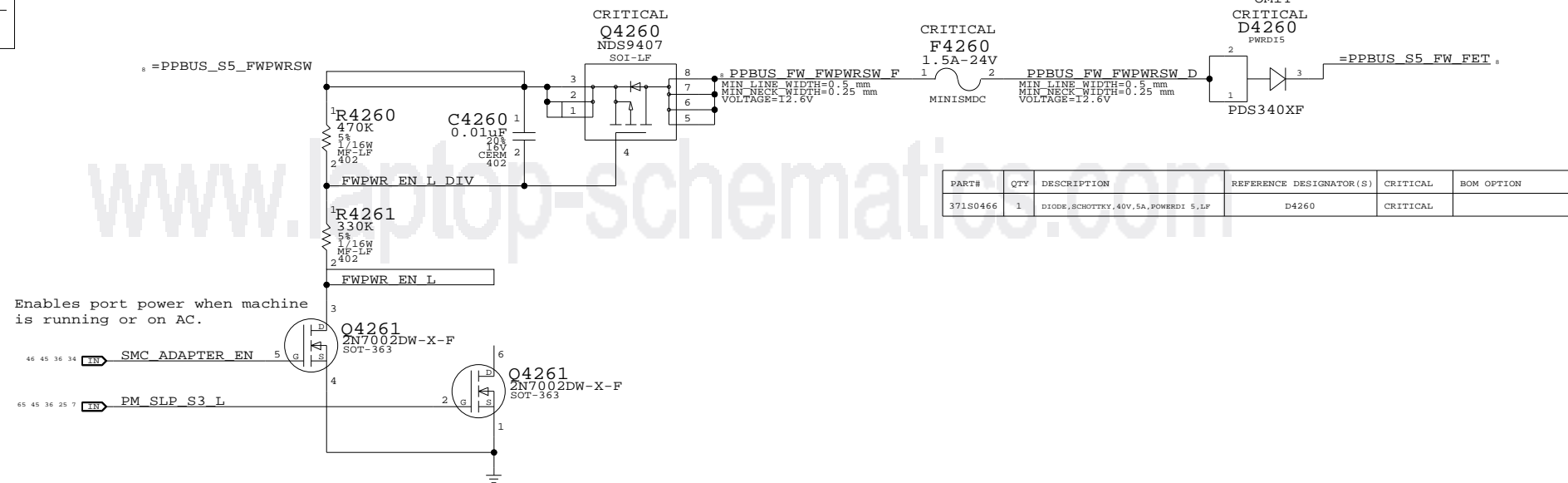
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - FW_PORT_FAULT_PU

FireWire Port Power Switch

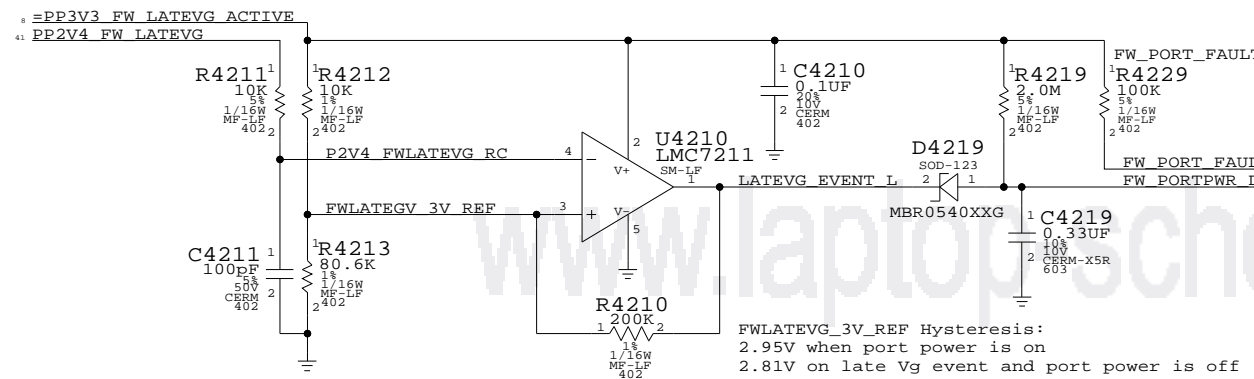


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|------------------------------------|-------------------------|----------|------------|
| 371S0466 | 1 | DIODE,SCHOTTKY,40V,5A,POWERDI 5,LF | D4260 | CRITICAL | |

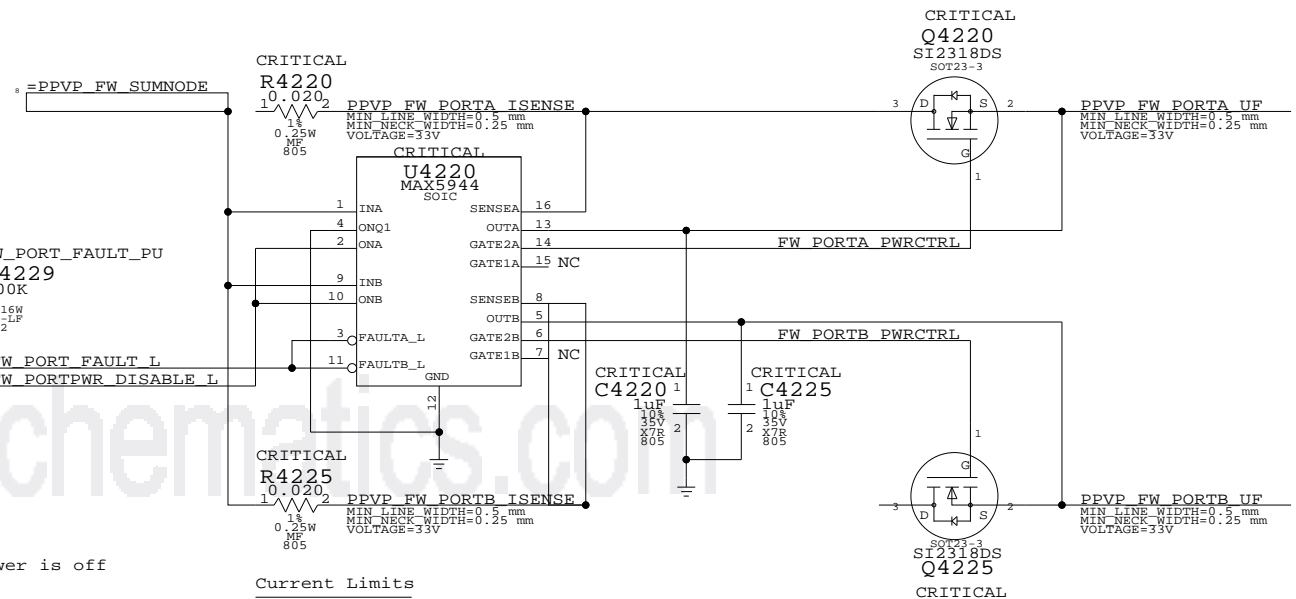
Enables port power when machine is running or on AC.

Current Limit/Active Late-VG Protection

Late-VG Event Detection



FWLATEVG_3V_REF Hysteresis:
 2.95V when port power is on
 2.81V on late Vg event and port power is off



Current Limits
 0.020 ohm => 2.4A
 0.025 ohm => 2A
 0.030 ohm => 1.66A (Ideal)
 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

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Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT0
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG
 - =GND_CHASSIS_FW_PORT0L
 - =GND_CHASSIS_FW_PORT0U
 - =GND_CHASSIS_FW_PORT1
 - =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

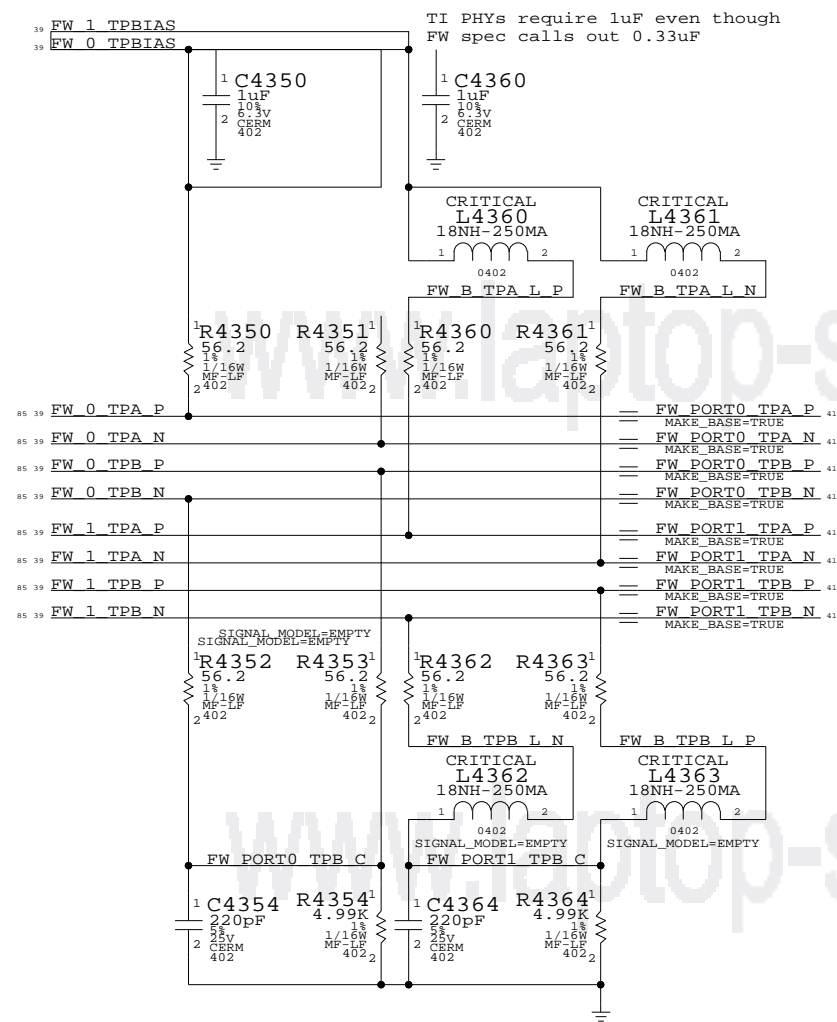
FireWire PHY Config Straps

Configures PHY for:

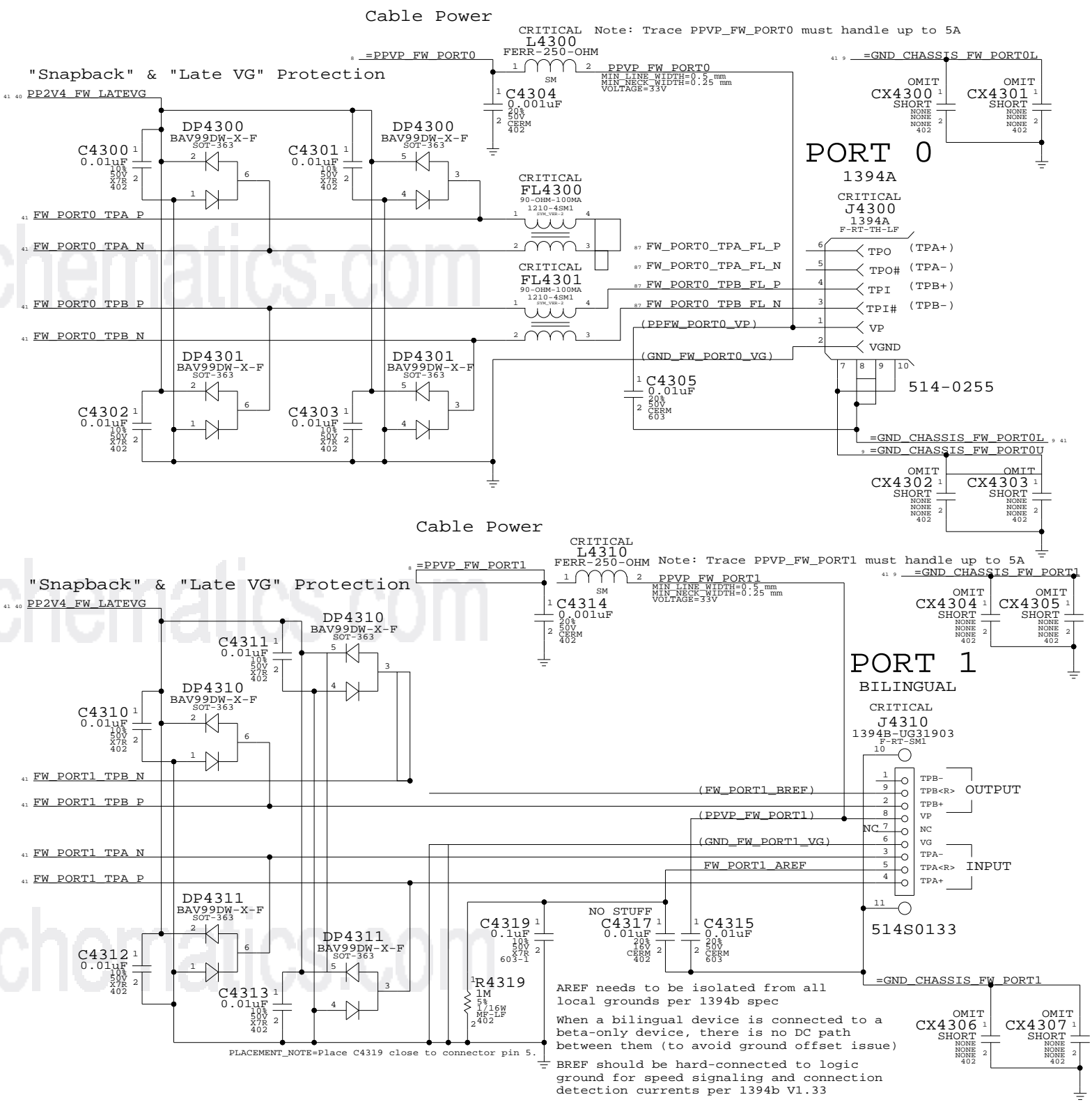
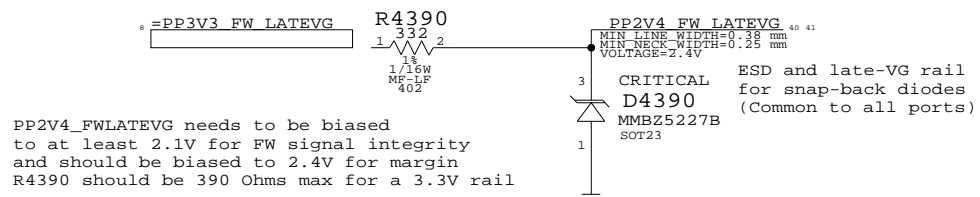
- 2-port Portable Power Class (4) =PP3V3_FW_PHY
- Port "0" Data-Strobe only (1394A) =FWPHY_PC0
- Port "1" Bilingual (1394B) =FWPHY_DS1

Termination

Place close to FireWire PHY



Late-VG Protection Power

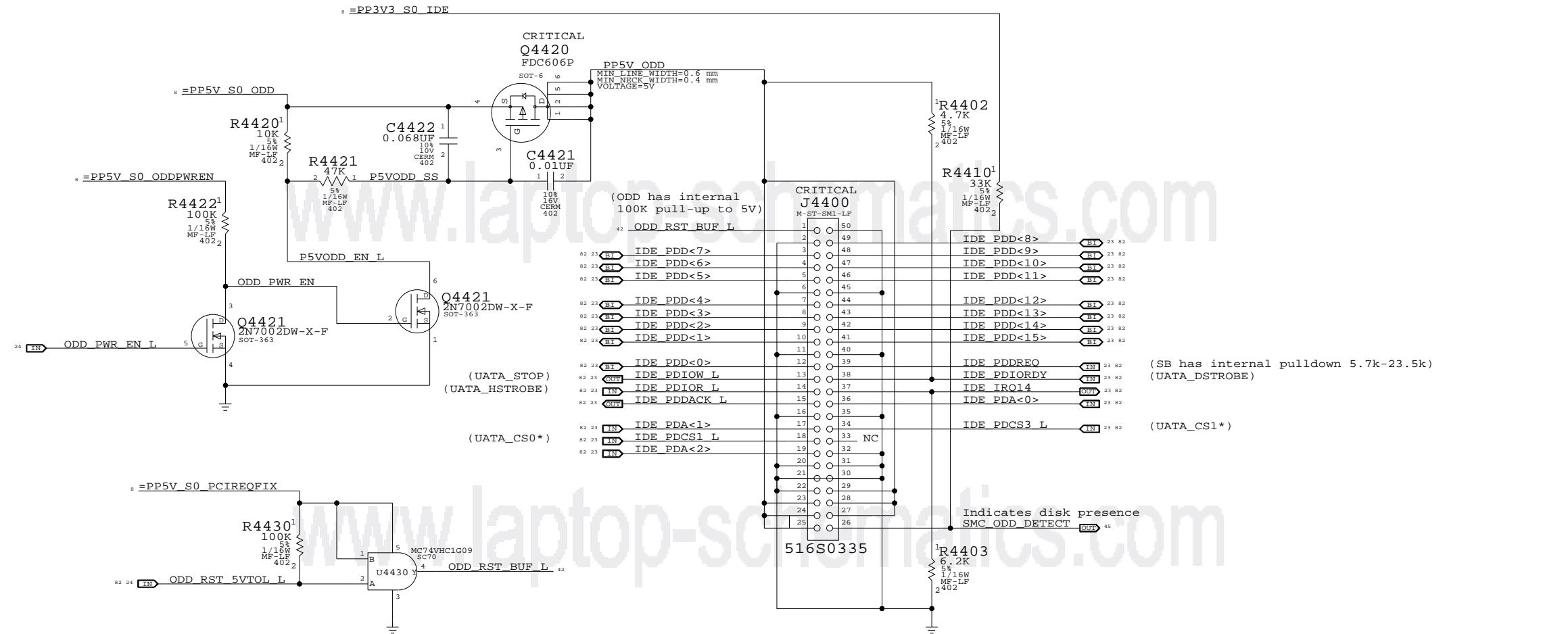


| FireWire Ports | | |
|--|----------------------|--|
| SYNC_MASTER=M76_MLB | SYNC_DATE=03/19/2007 | |
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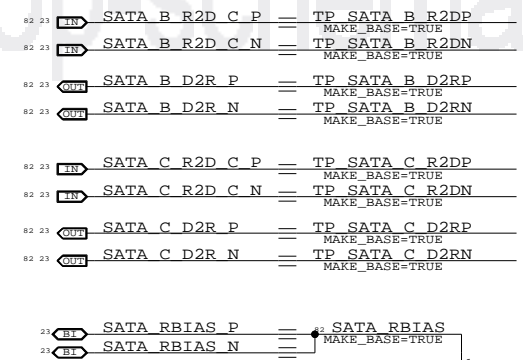
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| | D | 051-7435 | A |
| SCALE | SHT | OF | REV. |
| NONE | 43 | 109 | |

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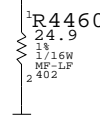
IDE (ODD) Connector



Unused SATA Ports



Placement note:
Place within 12.7mm
from ball of SB

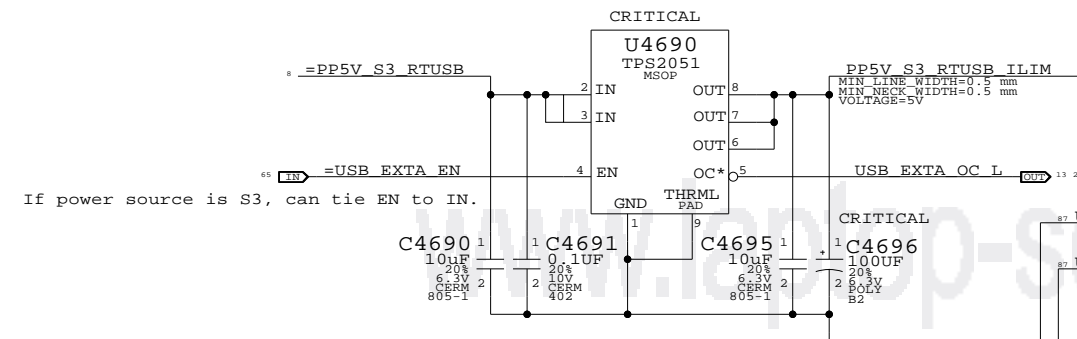


PATA Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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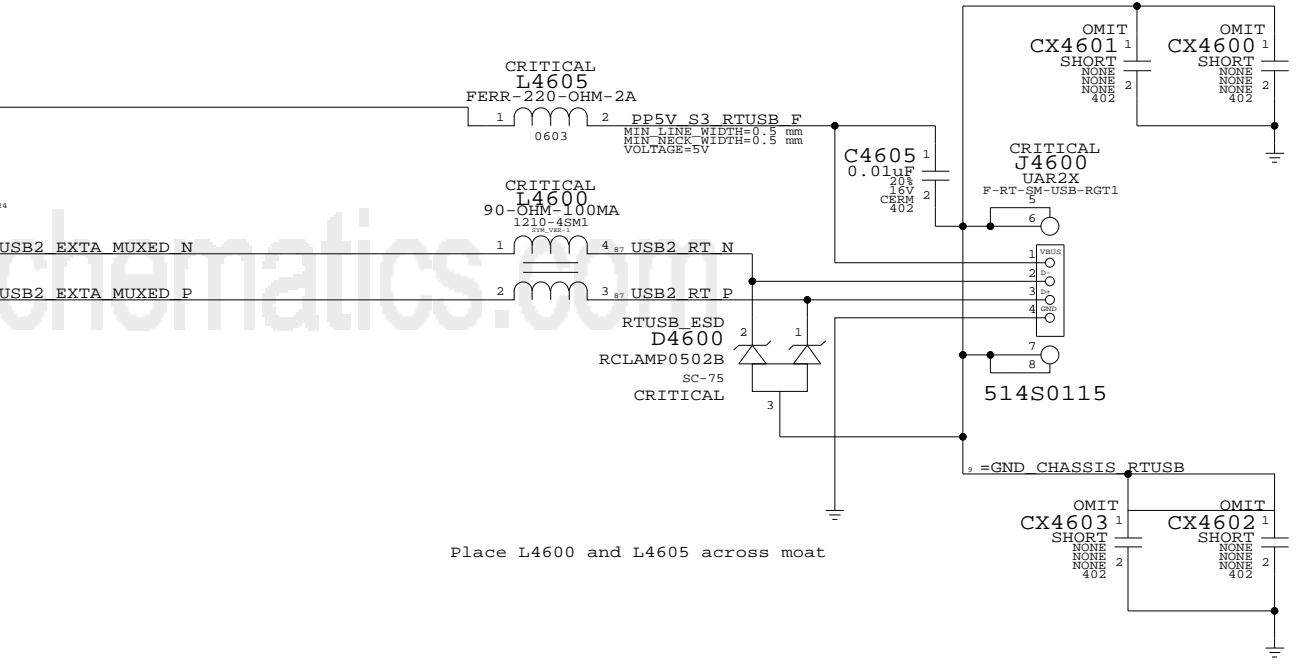
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7435 | A |
| SCALE | SHT | OF | REV. |
| NONE | 44 | 109 | |

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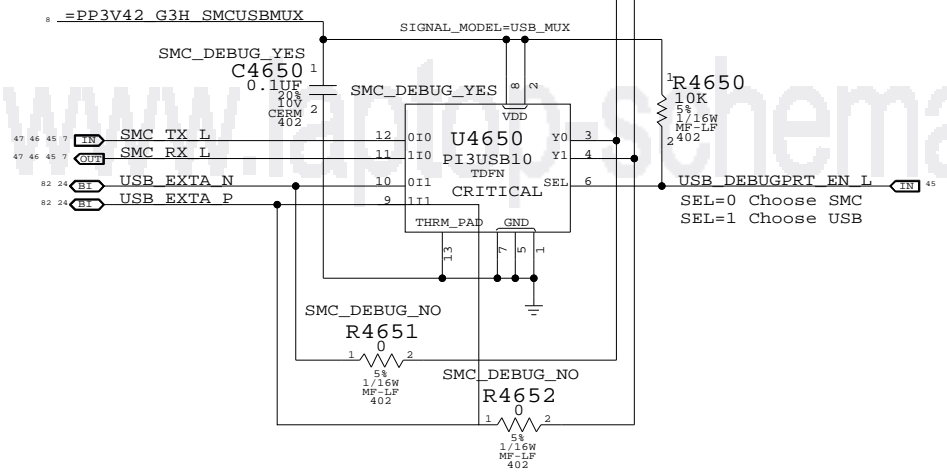
Port Power Switch



Right USB Port



USB/SMC Debug Mux

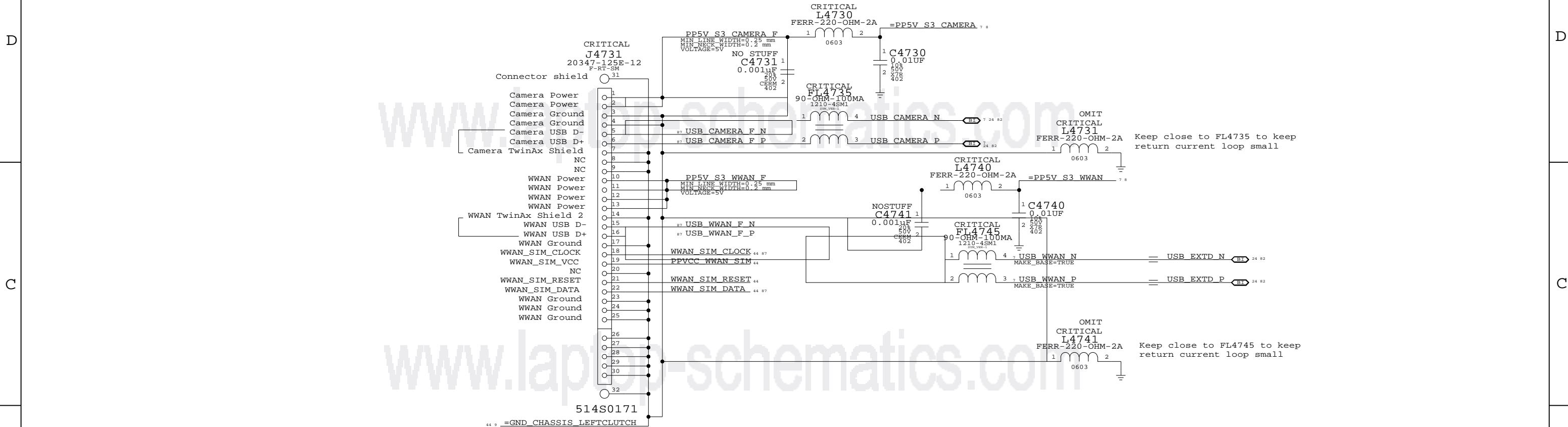


External USB Connector
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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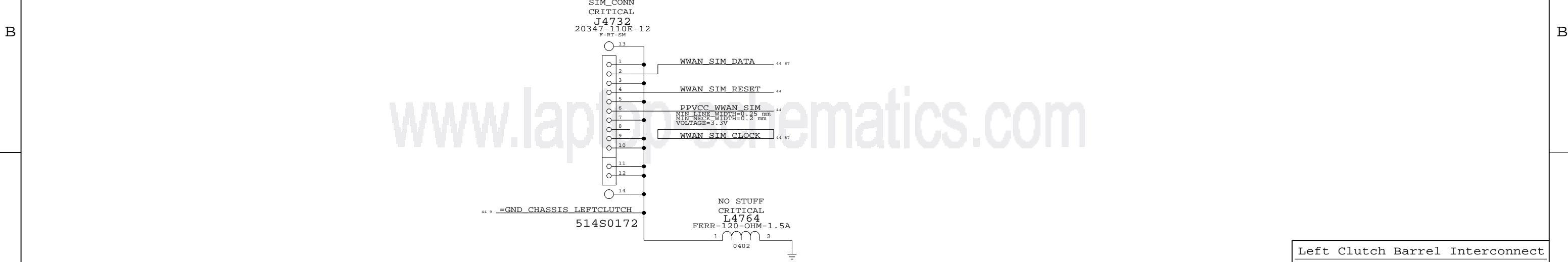
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7435 | A |
| SCALE | SHT | | OF |
| NONE | 46 | | 109 |

Left Clutch Barrel Interconnect



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---------------------------------------|-------------------------|----------|------------|
| 113S0022 | 2 | RES, MF, 1/10W, 00HM, 5, 0603, SM, LF | L4731, L4741 | CRITICAL | |

SIM Interconnect



Left Clutch Barrel Interconnect
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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| SCALE | SHT | OF | REV. |
| NONE | 47 | 109 | |

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

C

B

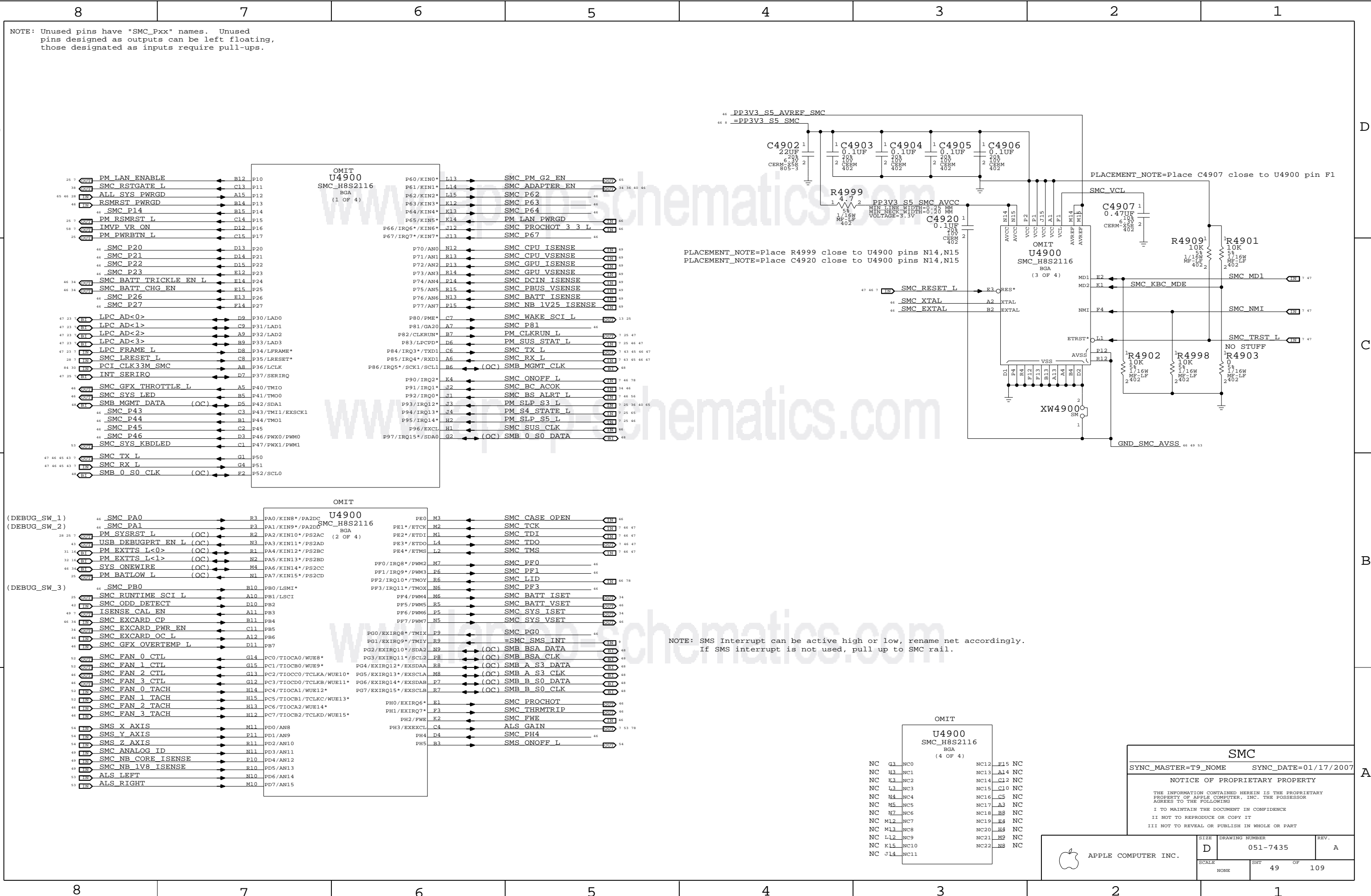
A

D

C

B

A



PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
 PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT_NOTE=Place C4907 close to U4900 pin F1

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
 If SMS interrupt is not used, pull up to SMC rail.

OMIT U4900 SMC_H8S2116 BGA (4 OF 4)

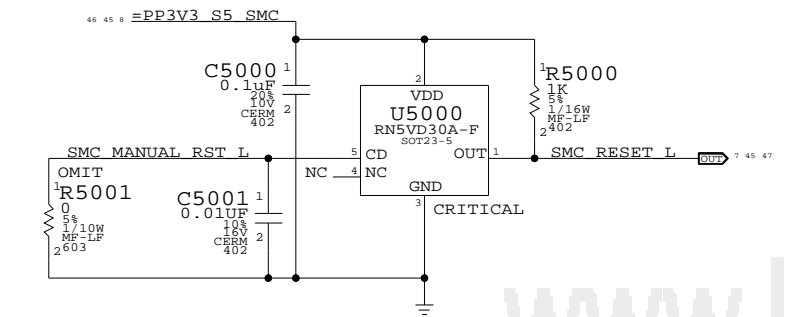
| | | | | |
|-------|------|------|-----|----|
| NC G3 | NC0 | NC12 | E15 | NC |
| NC H3 | NC1 | NC13 | A14 | NC |
| NC K3 | NC2 | NC14 | C12 | NC |
| NC L3 | NC3 | NC15 | C10 | NC |
| NC M3 | NC4 | NC16 | C5 | NC |
| NC N3 | NC5 | NC17 | A3 | NC |
| NC P3 | NC6 | NC18 | BB | NC |
| NC Q3 | NC7 | NC19 | E4 | NC |
| NC R3 | NC8 | NC20 | H4 | NC |
| NC S3 | NC9 | NC21 | M9 | NC |
| NC T3 | NC10 | NC22 | MB | NC |
| NC U3 | NC11 | | | |

SMC
 SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007
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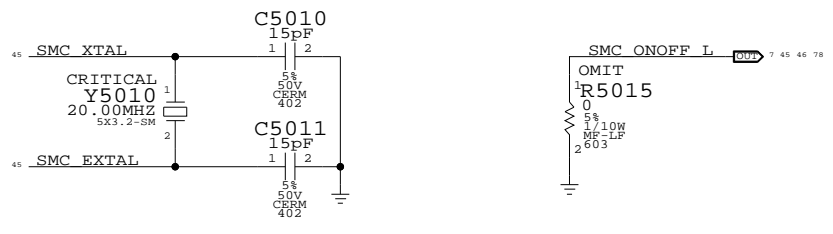
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
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| NONE | 49 | 109 | |

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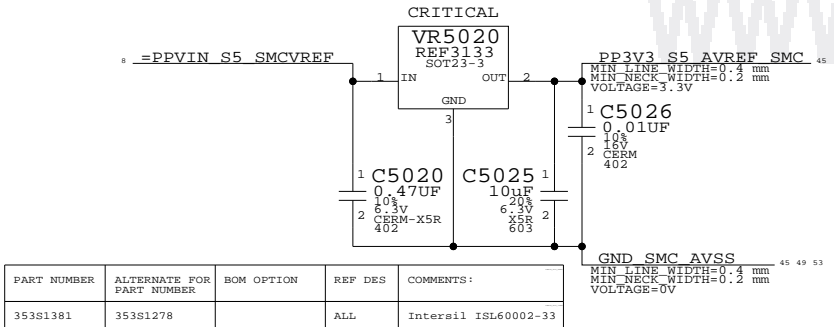
SMC Reset "Button" / Brownout Detect



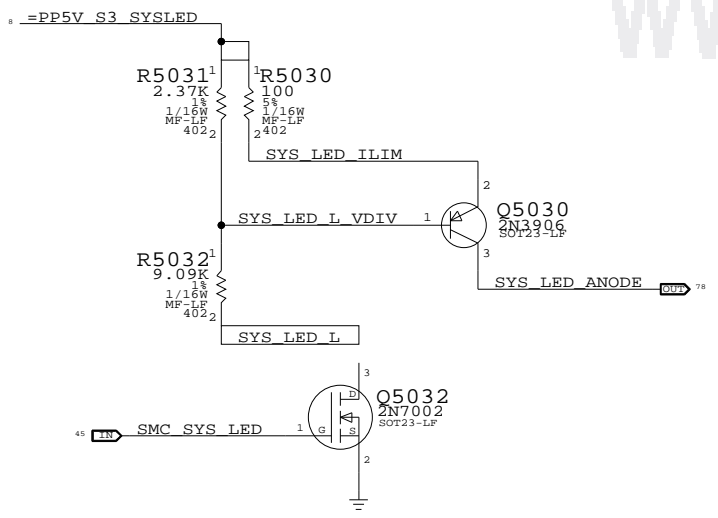
SMC Crystal Circuit Debug Power "Button"



SMC AVREF Supply

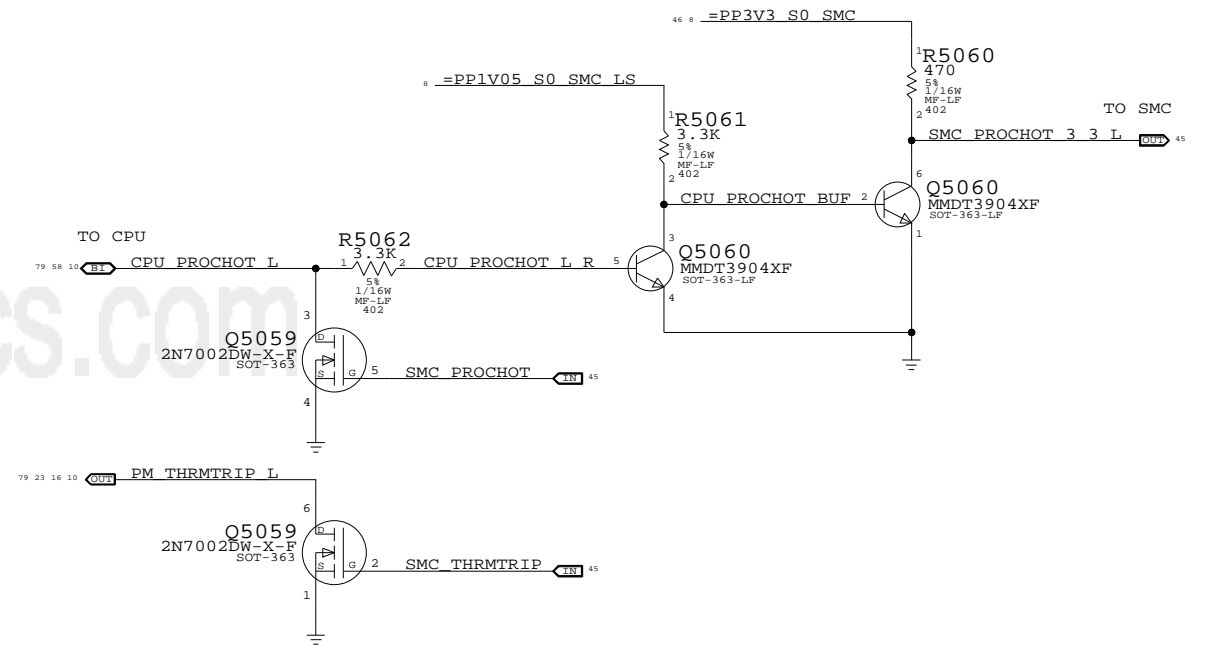


System (Sleep) LED Circuit



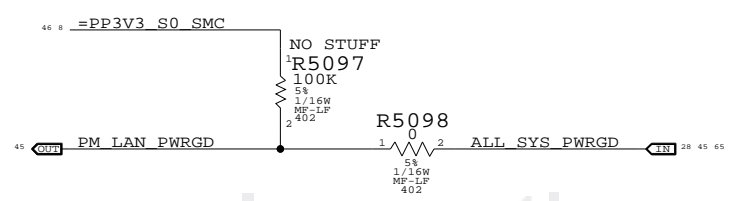
- SMC_FAN_2_CTL == TP_SMC_FAN_2_CTL
- SMC_FAN_2_TACH == TP_SMC_FAN_2_TACH
- SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL
- SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH
- SMC_GFX_OVERTEMP_L == TP_SMC_GFX_OVERTEMP_L
- SMC_GFX_THROTTLE_L == TP_SMC_GFX_THROTTLE_L
- SMC_BATT_VSET == TP_SMC_BATT_VSET
- SMC_SYS_VSET == TP_SMC_SYS_VSET
- SMC_P14 == TP_SMC_P14
- SMC_P20 == TP_SMC_P20
- SMC_P21 == TP_SMC_P21
- SMC_P22 == TP_SMC_P22
- SMC_P23 == TP_SMC_P23
- SMC_P26 == TP_SMC_P26
- SMC_P27 == TP_SMC_P27
- SMC_P43 == TP_SMC_P43
- SMC_P44 == TP_SMC_P44
- SMC_P46 == TP_SMC_P46
- SMC_P62 == TP_SMC_P62
- SMC_P63 == TP_SMC_P63
- SMC_P64 == TP_SMC_P64
- SMC_P81 == TP_SMC_P81
- SMC_PFO == TP_SMC_PFO
- SMC_PF1 == TP_SMC_PF1

SMC FSB to 3.3V Level Shifting

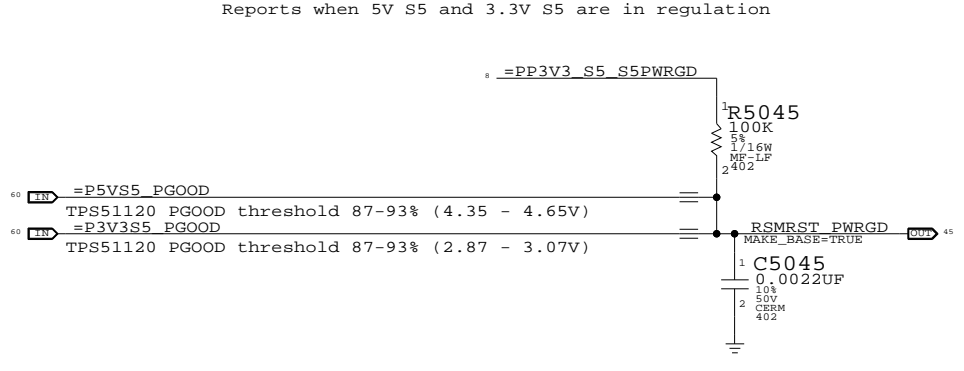


- SMC_EXCARD_OC_L == EXCARD_OC_L
- SMC_SUS_CLK == SUS_CLK_SB
- SMC_P45 == SMC_ENRGYSTR_LDO_EN

LAN PWRGD Circuit



S5 Rail PWRGD Circuit



- SMC_PA0 == R5091 100K
- SMC_PA1 == R5092 100K
- SMC_PB0 == R5093 100K
- SMC_ONOFF_L == R5070 10K
- SMC_LID == R5071 100K
- SMC_FWE == R5072 10K
- SMC_TX_L == R5073 10K
- SMC_RX_L == R5074 10K
- SMC_P67 == R5094 10K
- SMC_P63 == R5081 10K
- SMC_PG0 == R5096 10K
- SMC_PH4 == R5082 10K
- SMC_BATT_TRICKLE_EN_L == R5083 10K
- SMC_BATT_CHG_EN == R5084 10K
- SMC_ADAPTER_EN == R5085 10K
- SMC_CASE_OPEN == R5086 10K
- SMC_BC_ACOK == R5087 470K
- SMC_EXCARD_CP == R5088 10K
- PM_SUS_STAT_L == R5089 100K
- PM_SLP_S5_L == R5090 100K

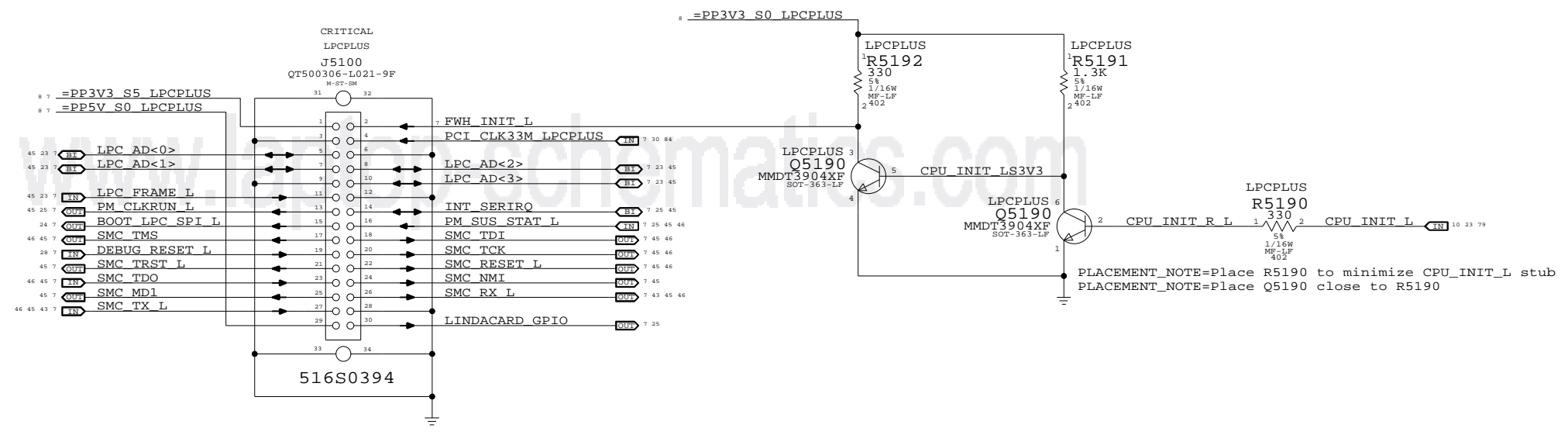
SMC Support
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LPC+ Connector

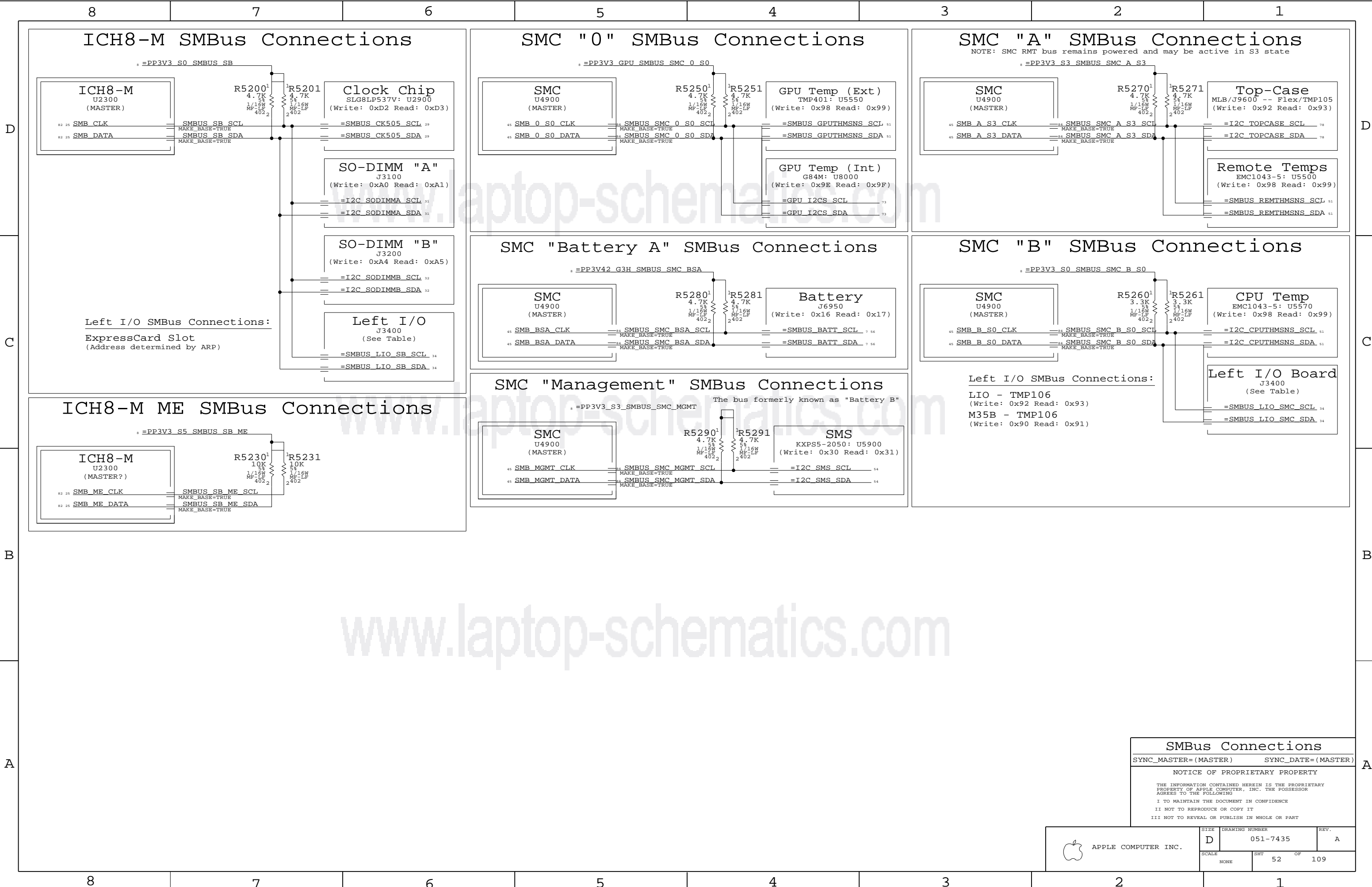
FWH_INIT_L Generation



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LPC+ Debug Connector
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007
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| SCALE | SHT | OF | REV. |
| NONE | 51 | 109 | |



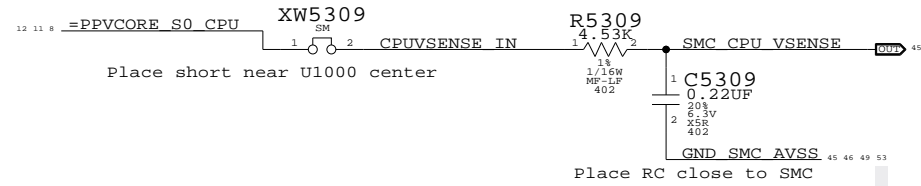
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www.laptop-schematics.com

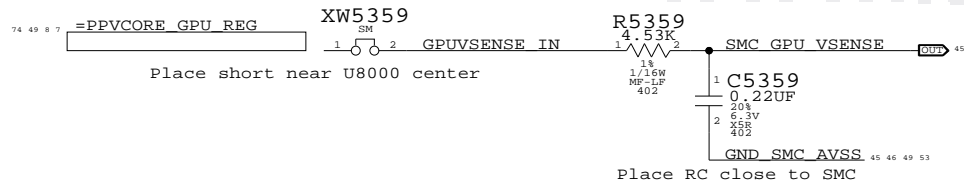
SMBus Connections
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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| | D | 051-7435 | A |
| SCALE | SHT | OF | |
| NONE | 52 | 109 | |

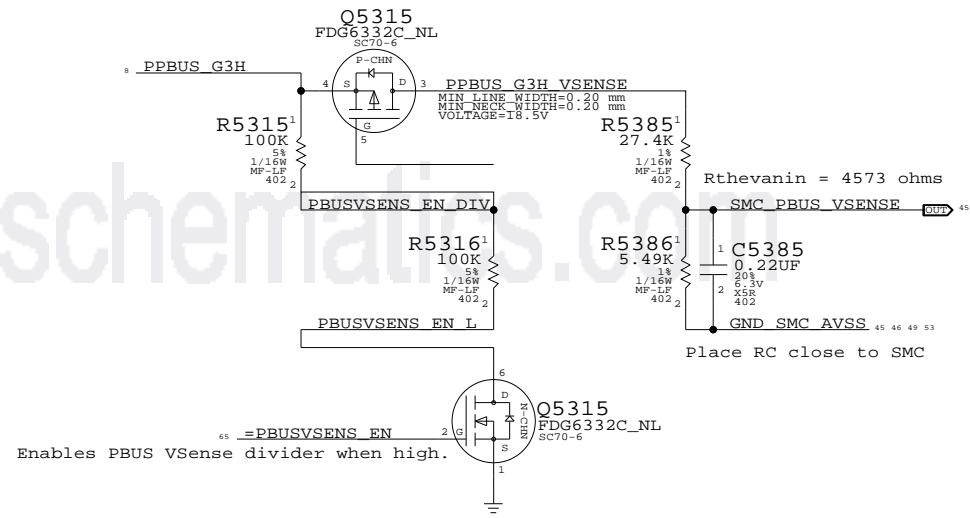
CPU Voltage Sense / Filter



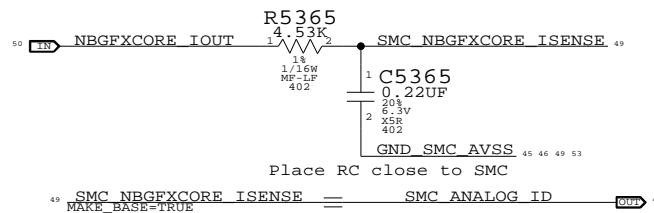
GPU Voltage Sense / Filter



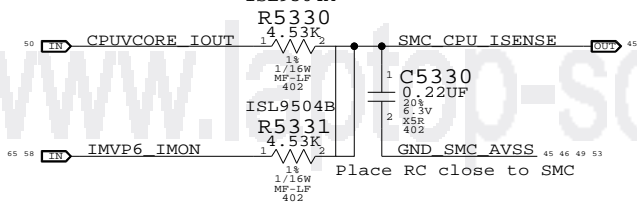
PBUS Voltage Sense & Filter



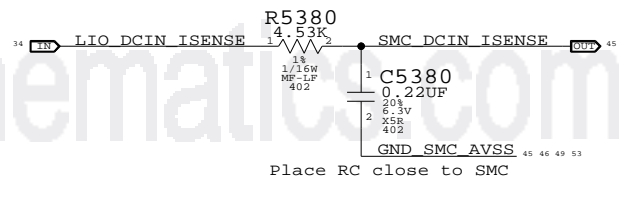
NB GFX Current Sense Filter



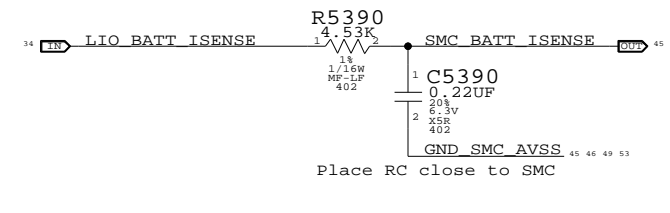
CPU Current Sense Filter



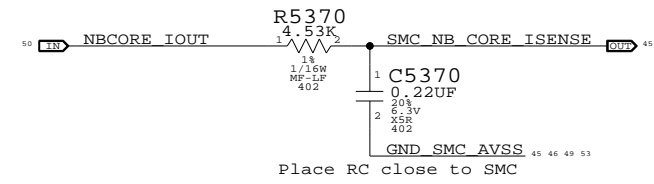
DCIN Current Sense Filter



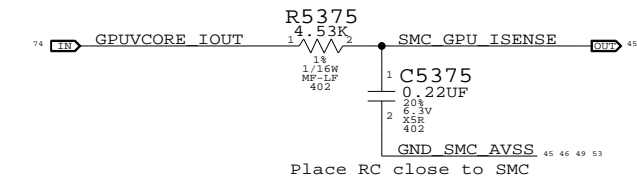
Battery (PBUS) Current Sense Filter



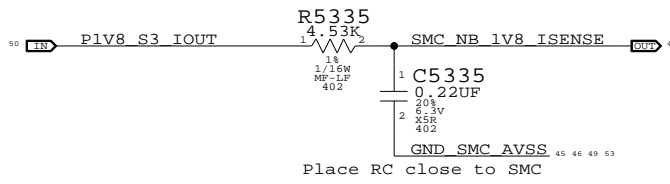
NB Core Current Sense Filter



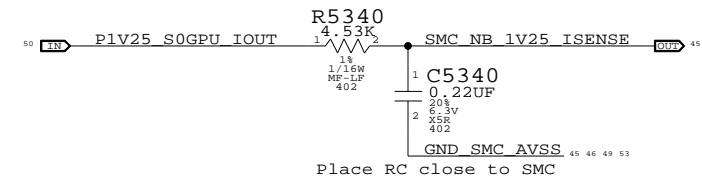
GPU Current Sense Filter



NB 1.8V Current Sense Filter

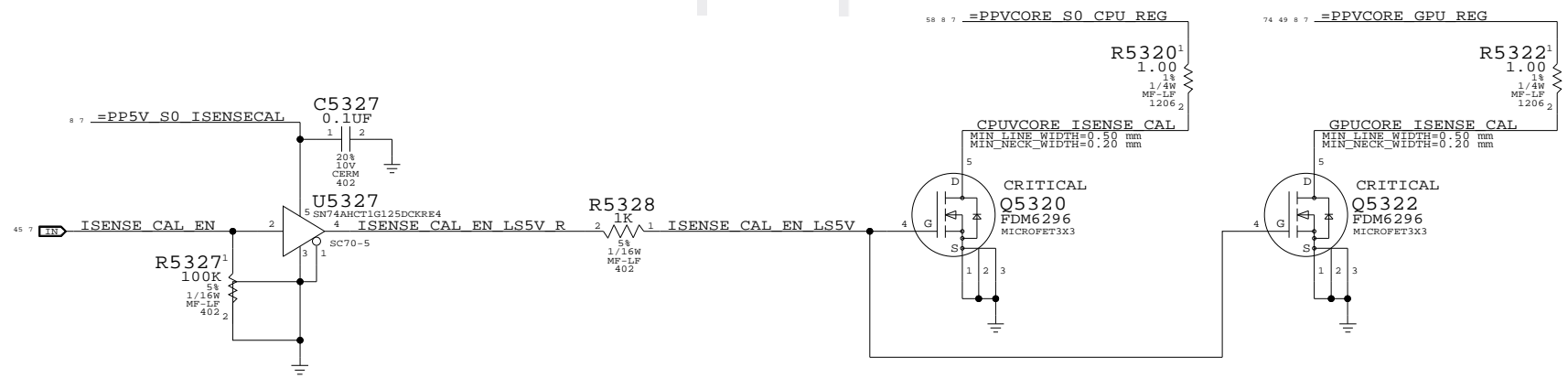


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

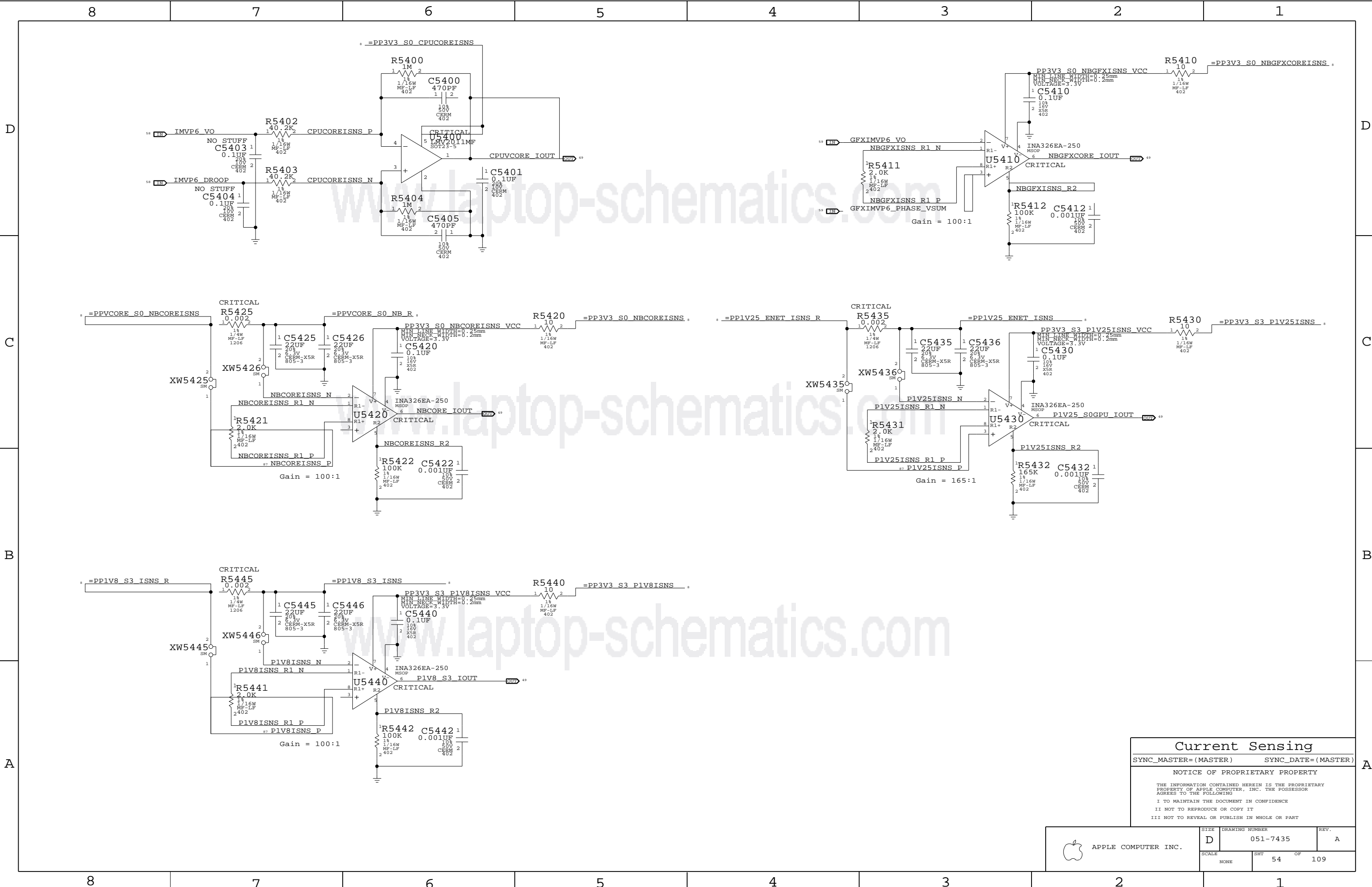


Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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Current Sensing

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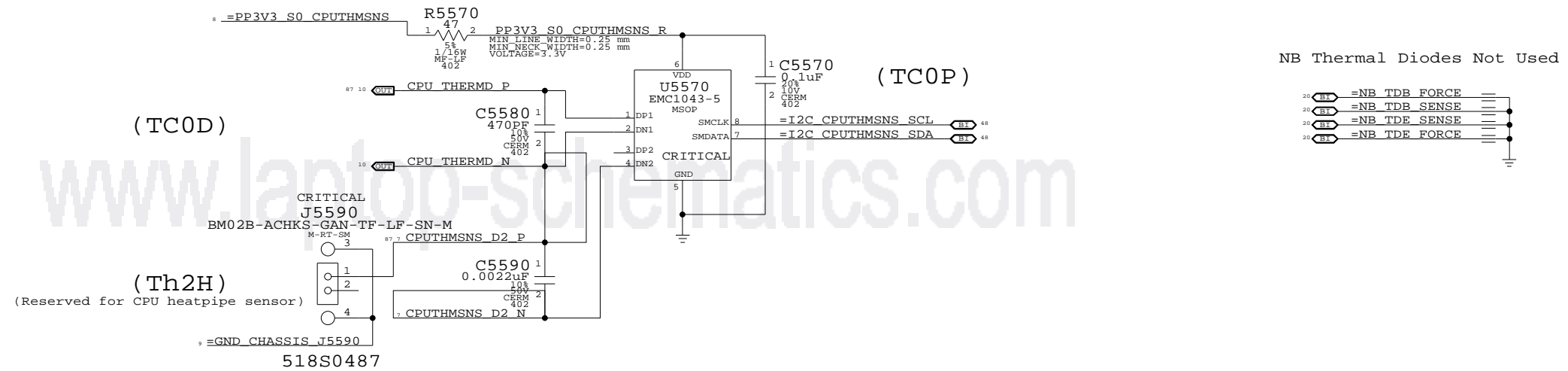
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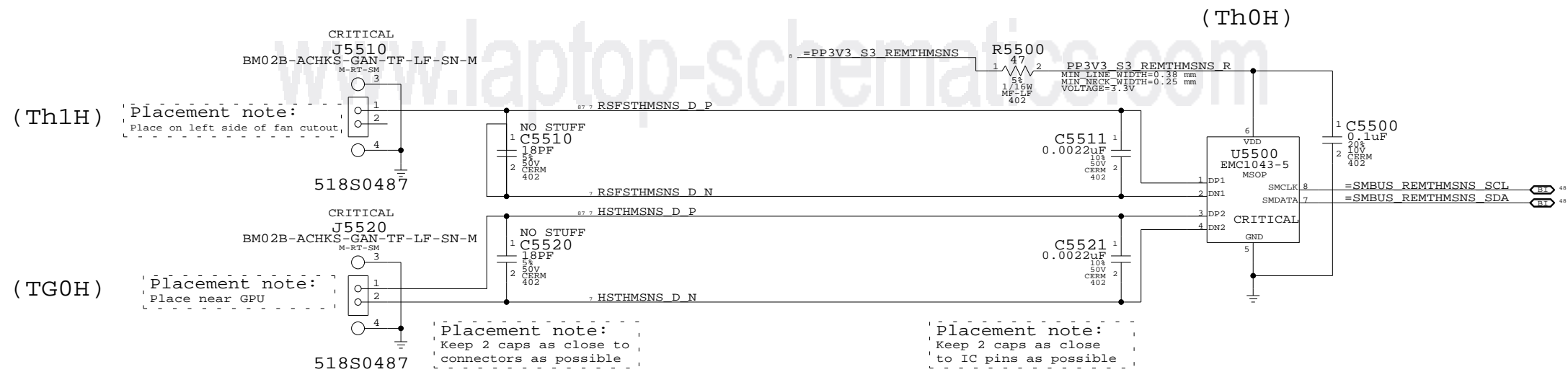
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| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-7435 | REV. A |
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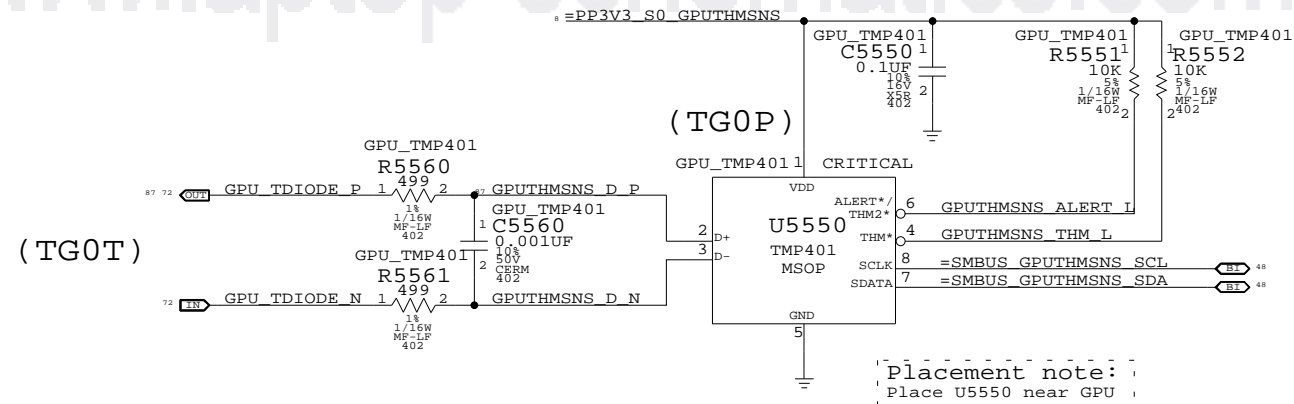
CPU T-Diode Thermal Sensor



GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



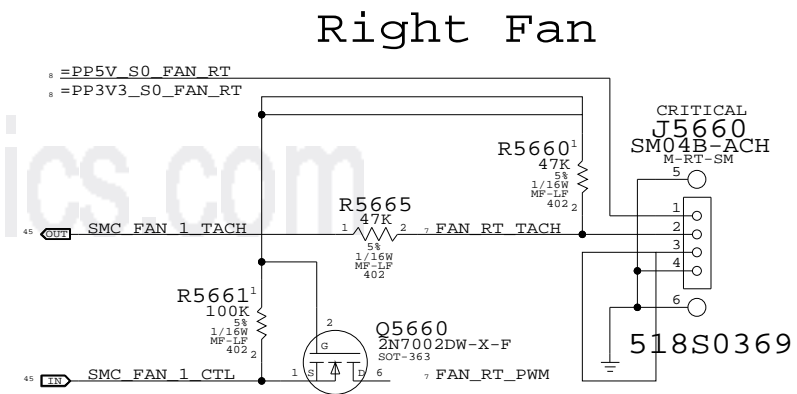
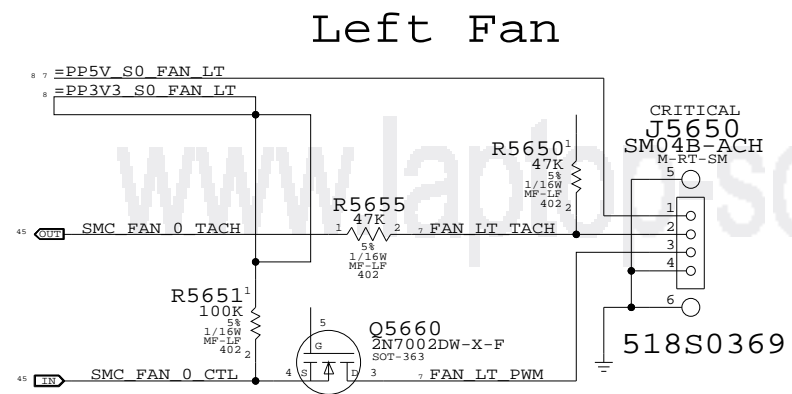
GPU Die Thermal Sensor



| Thermal Sensors | | |
|--|--------------------|--|
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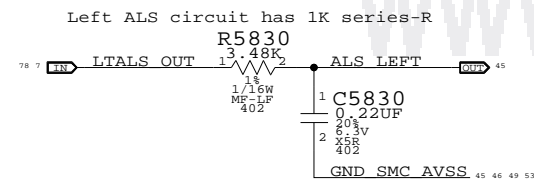
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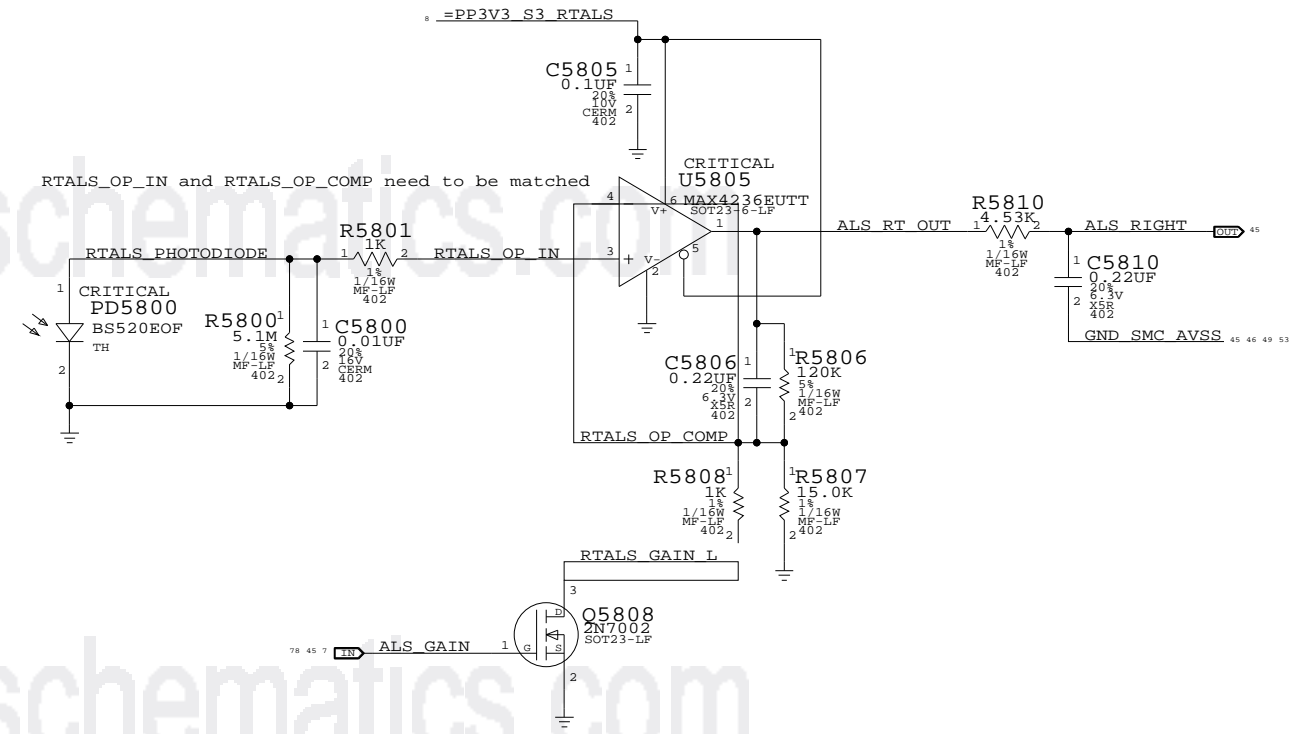
Fan Connectors
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007
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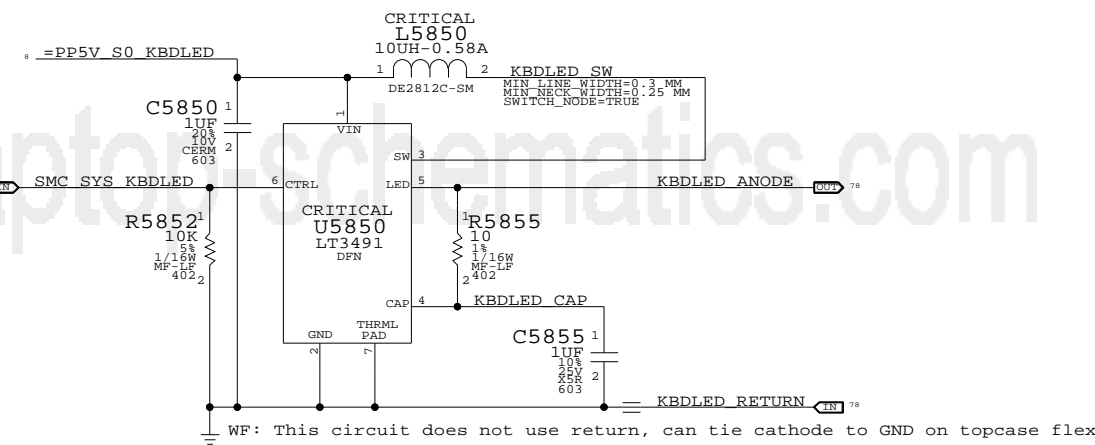
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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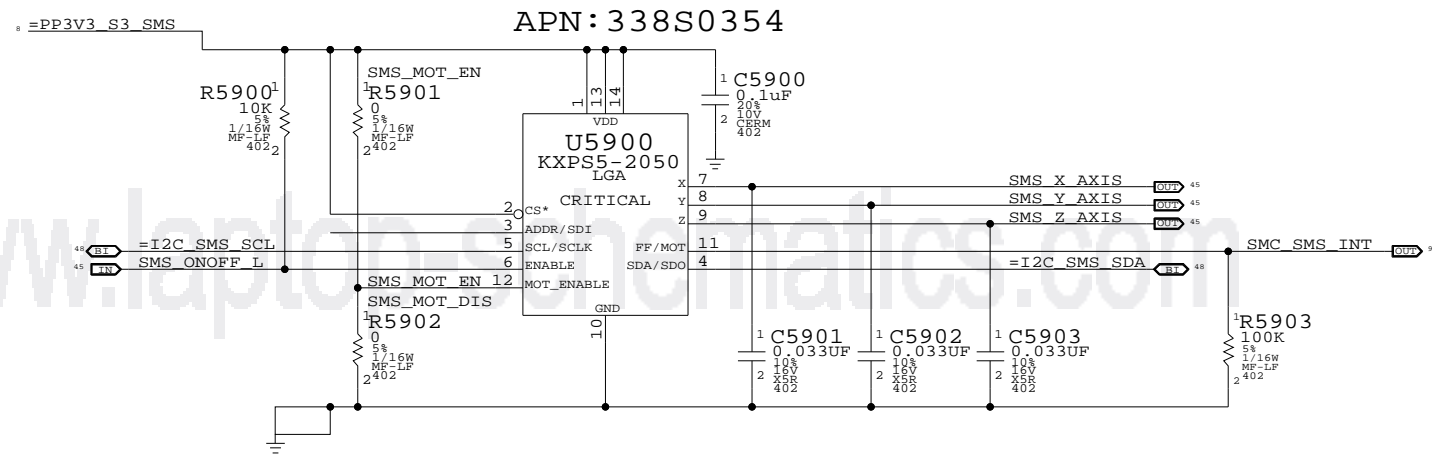
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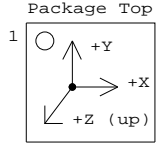


I2C addresses:

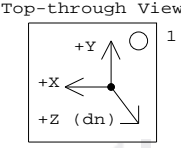
ADDR low => 0x30, 0x31
 ADDR high => 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:

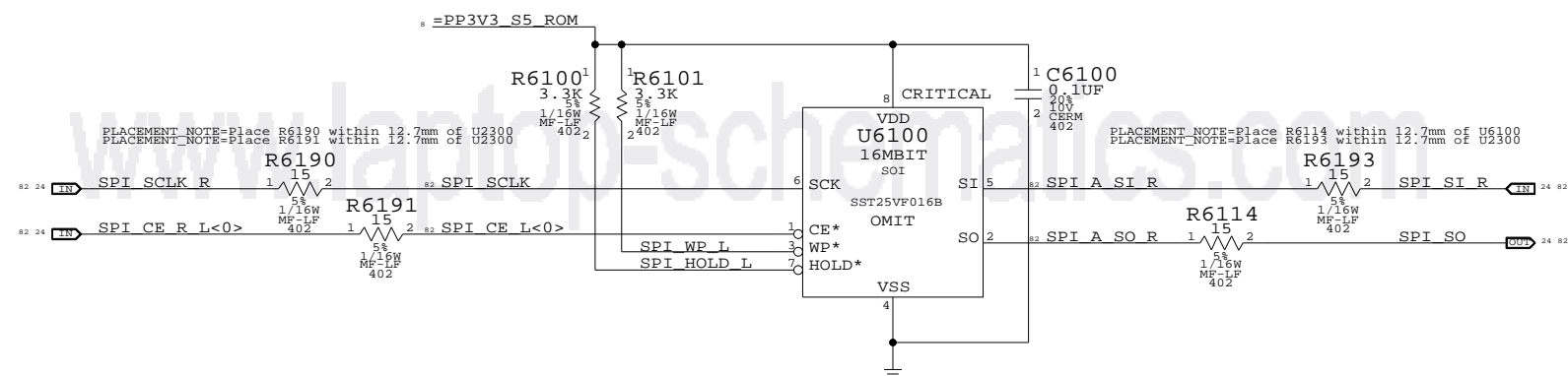


Sudden Motion Sensor (SMS)
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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| SCALE | SHT | | OF |
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SPI BootROM

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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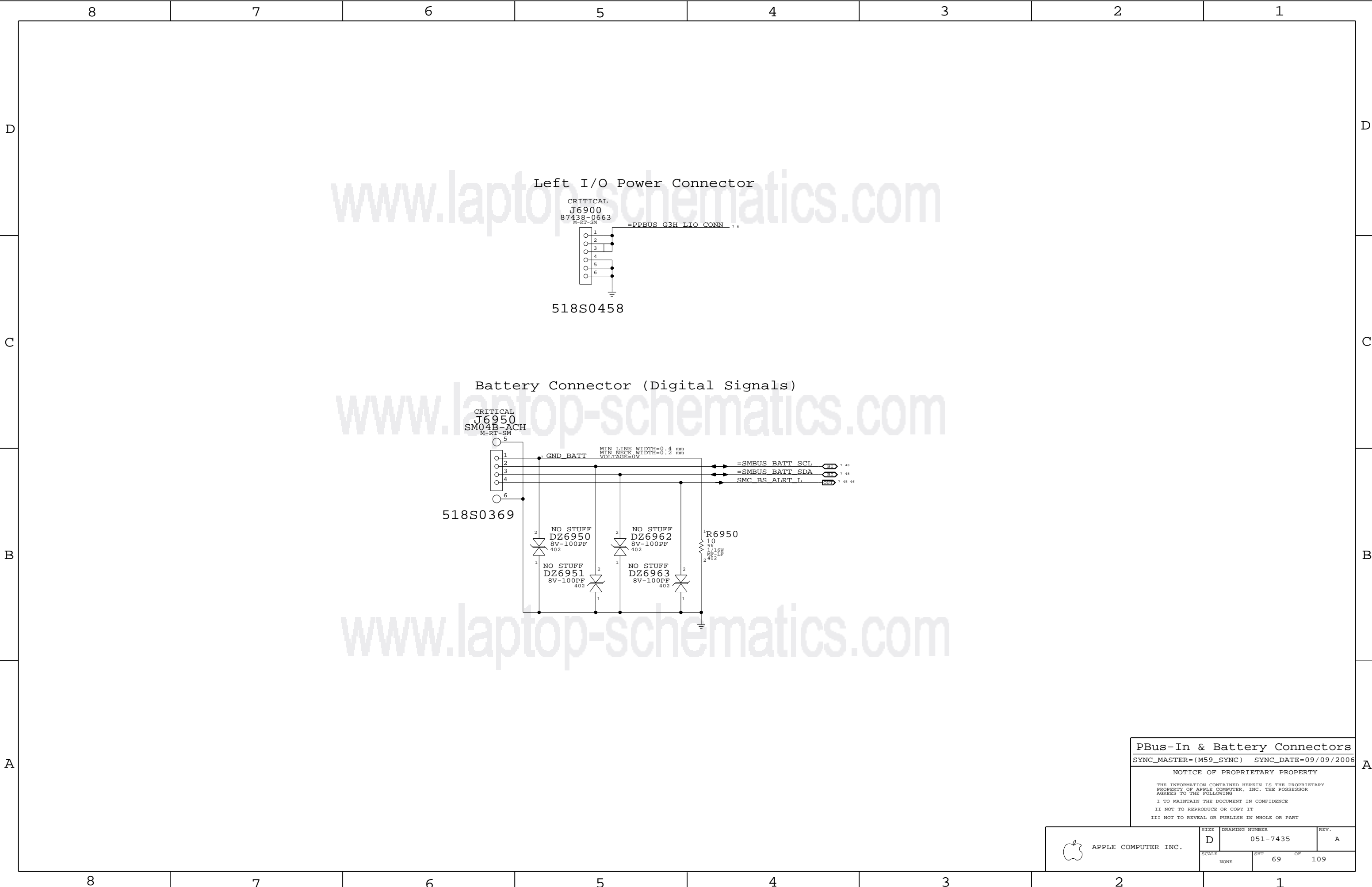
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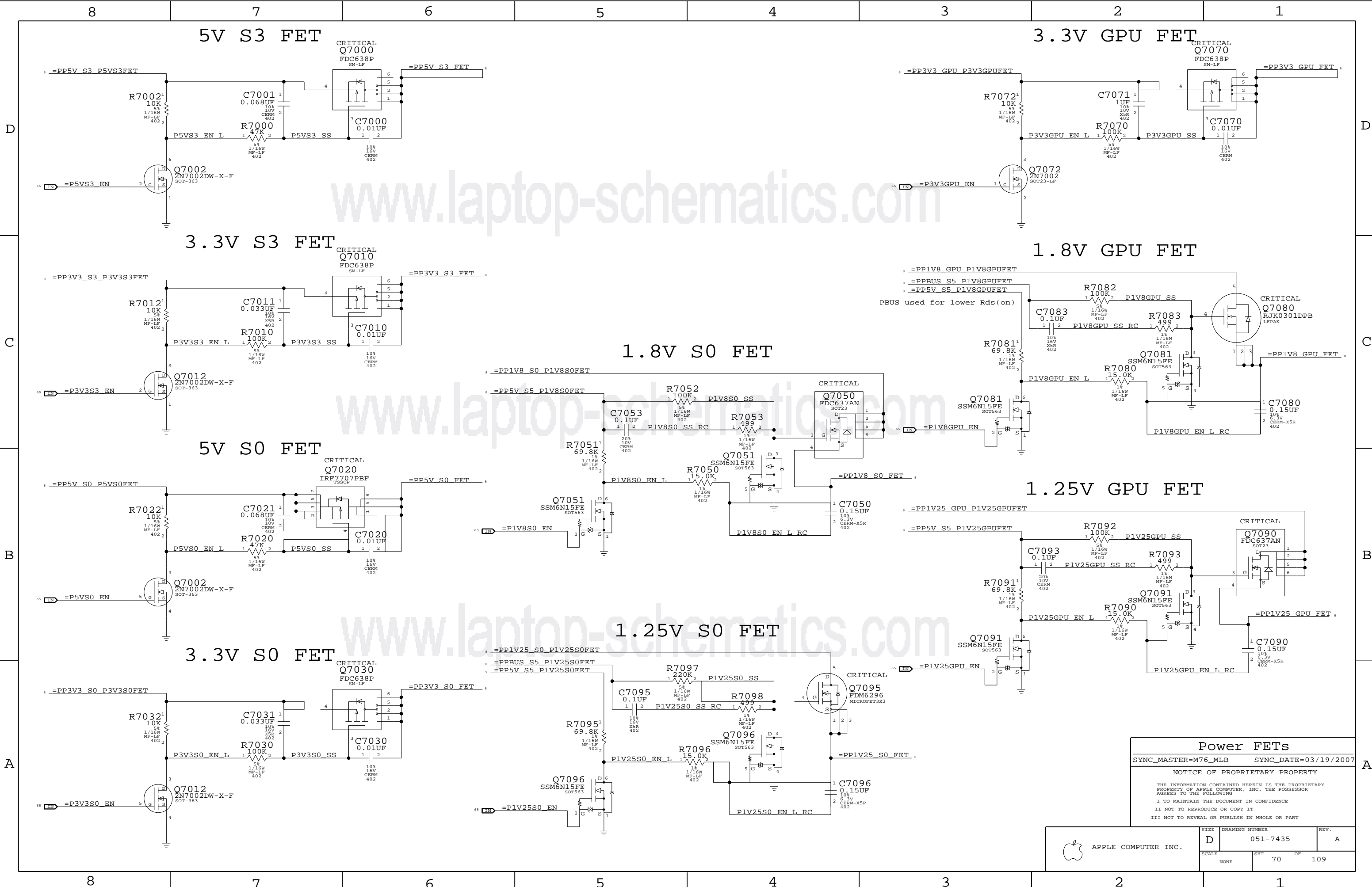
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PBus-In & Battery Connectors
 SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006
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| NONE | 69 | 109 | |



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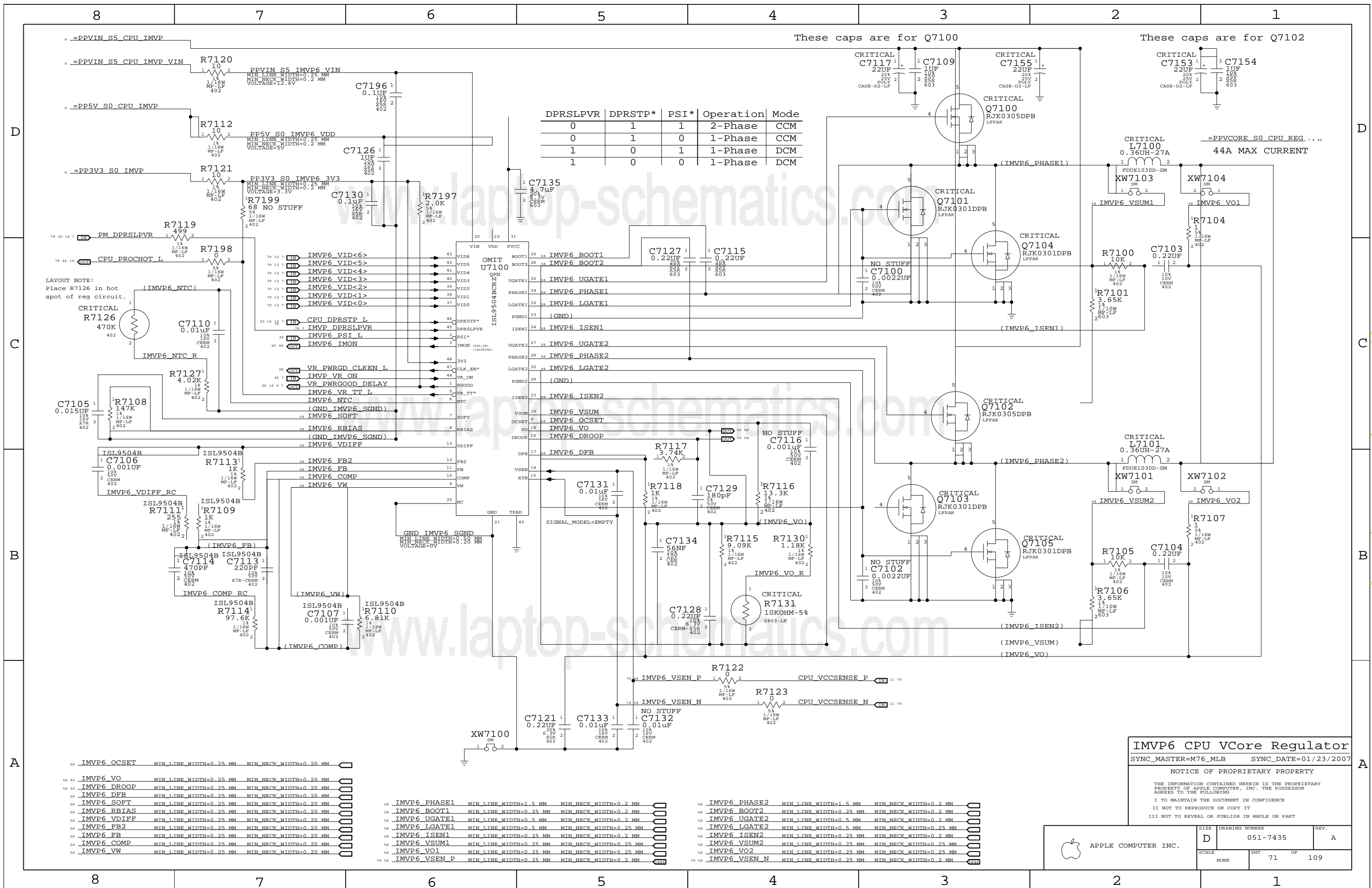
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Power FETs
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| | D | 051-7435 | A |
| SCALE | SHT 70 OF 109 | | |
| NONE | | | |

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| DPRSLPVR | DPRSTP* | PSI* | Operation | Mode |
|----------|---------|------|-----------|------|
| 0 | 1 | 1 | 2-Phase | CCM |
| 0 | 1 | 0 | 1-Phase | CCM |
| 1 | 0 | 1 | 1-Phase | DCM |
| 1 | 0 | 0 | 1-Phase | DCM |

These caps are for Q7100

These caps are for Q7102

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

IMVP6 CPU VCore Regulator

SYNC_MASTER=M76_MLB SYNC_DATE=01/23/2007

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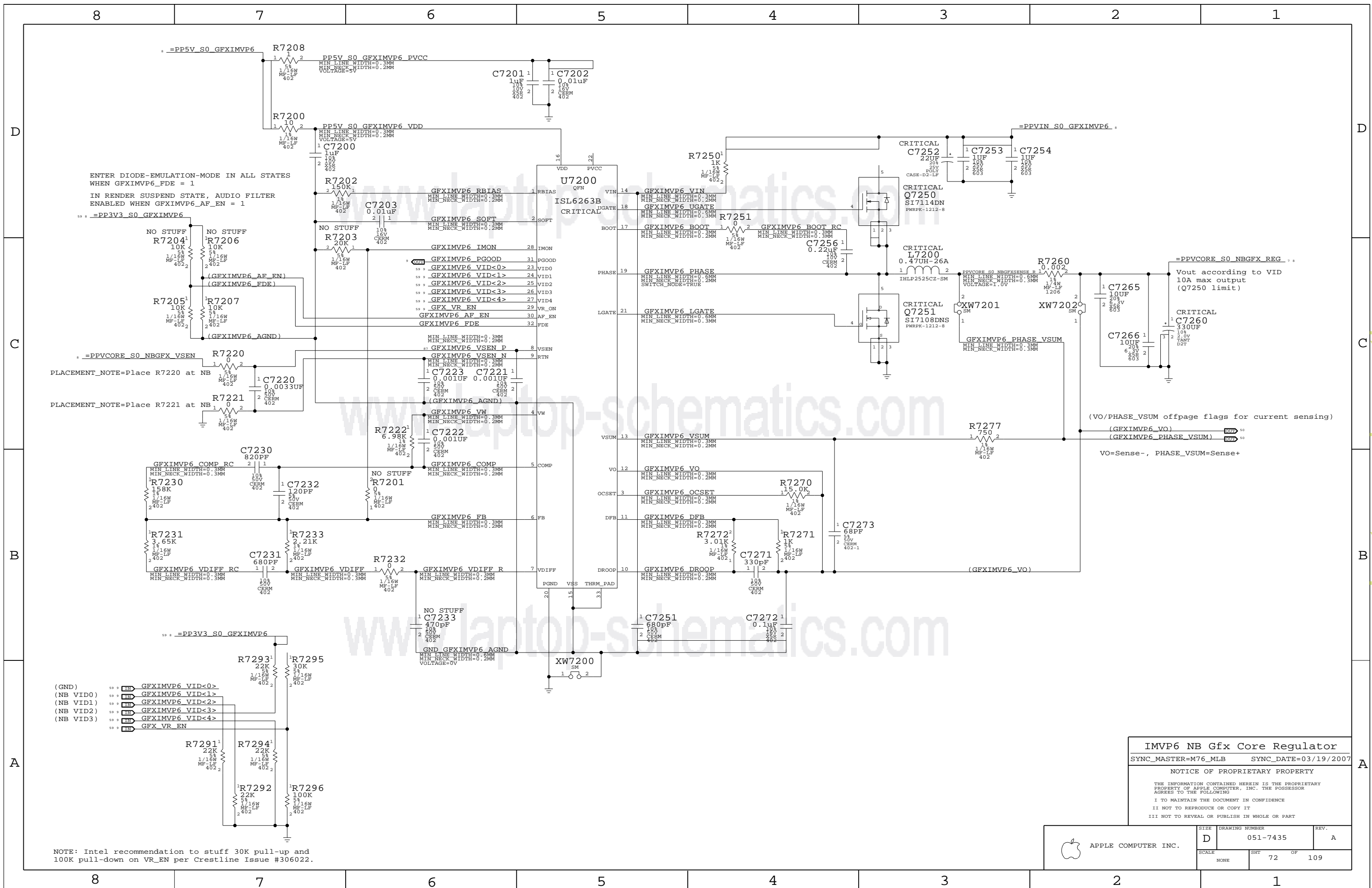
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| SCALE | SHEET | OF | |
| NONE | 71 | OF | 109 |

A

A

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ENTER DIODE-EMULATION-MODE IN ALL STATES
WHEN GFXIMVP6_FDE = 1
IN RENDER SUSPEND STATE, AUDIO FILTER
ENABLED WHEN GFXIMVP6_AF_EN = 1

PLACEMENT_NOTE=Place R7220 at NB
PLACEMENT_NOTE=Place R7221 at NB

(GND)
GFXIMVP6 VID<0>
GFXIMVP6 VID<1>
GFXIMVP6 VID<2>
GFXIMVP6 VID<3>
GFXIMVP6 VID<4>
GFX VR_EN

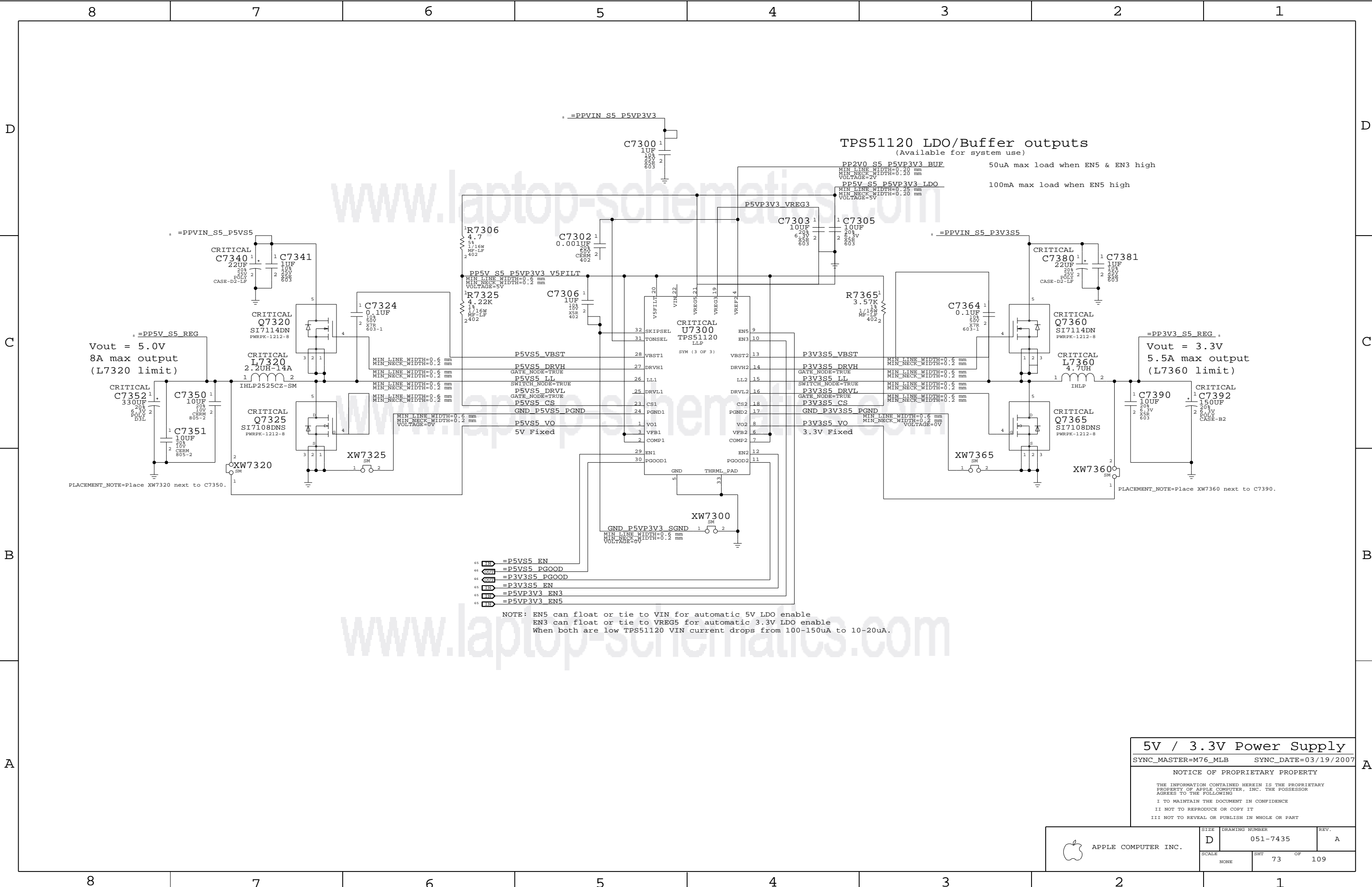
NOTE: Intel recommendation to stuff 30K pull-up and 100K pull-down on VR_EN per Crestline Issue #306022.

IMVP6 NB Gfx Core Regulator
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TPS51120 LDO/Buffer outputs
 (Available for system use)

PP2V0_S5_P5VP3V3_BUF 50uA max load when EN5 & EN3 high
 MIN_LINE_WIDTH=0.20 mm
 MIN_NECK_WIDTH=0.20 mm
 VOLTAGE=2V

PP5V_S5_P5VP3V3_LDO 100mA max load when EN5 high
 MIN_LINE_WIDTH=0.25 mm
 MIN_NECK_WIDTH=0.20 mm
 VOLTAGE=5V

Vout = 5.0V
 8A max output
 (L7320 limit)

Vout = 3.3V
 5.5A max output
 (L7360 limit)

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
 EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
 When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply

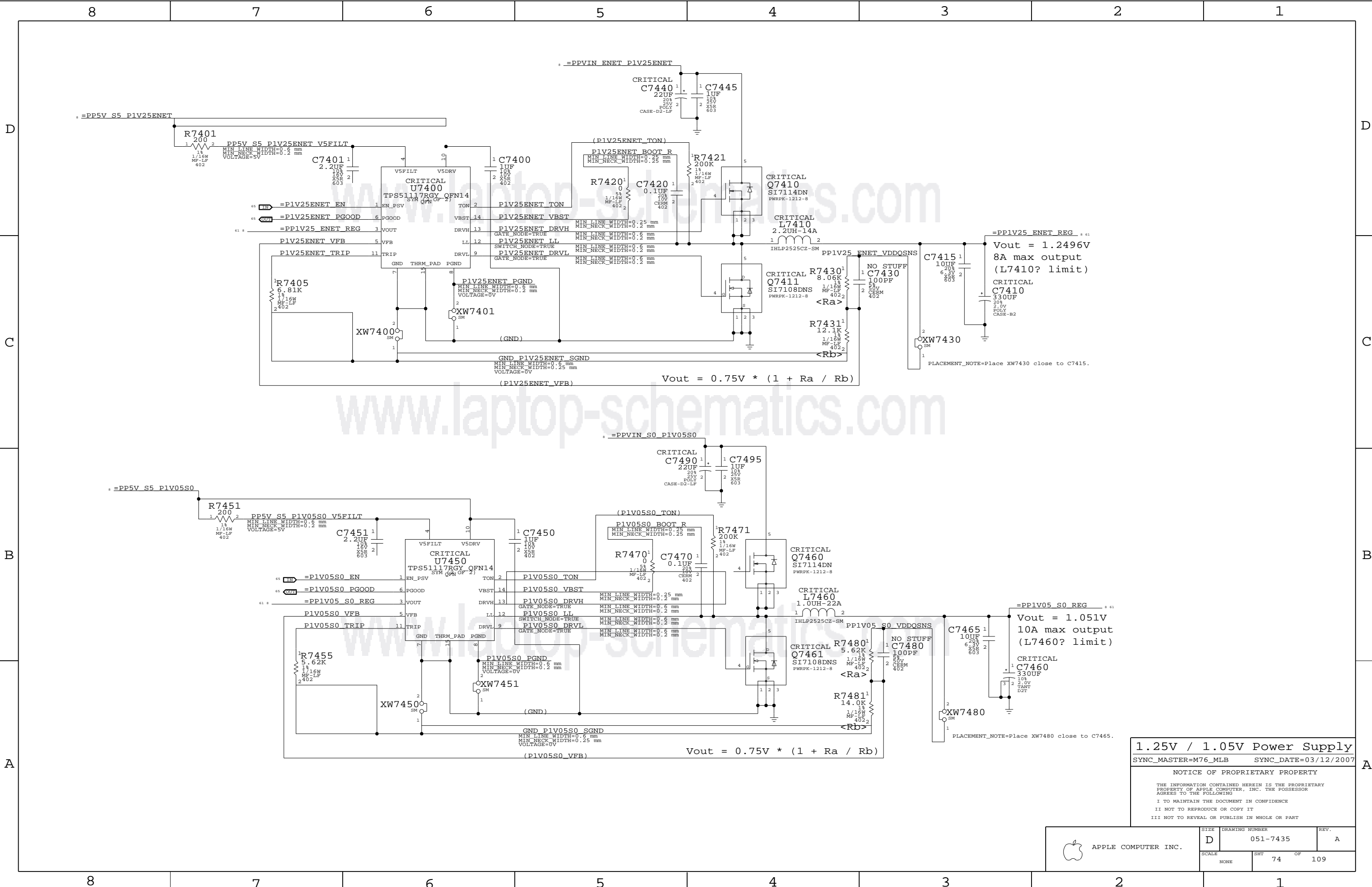
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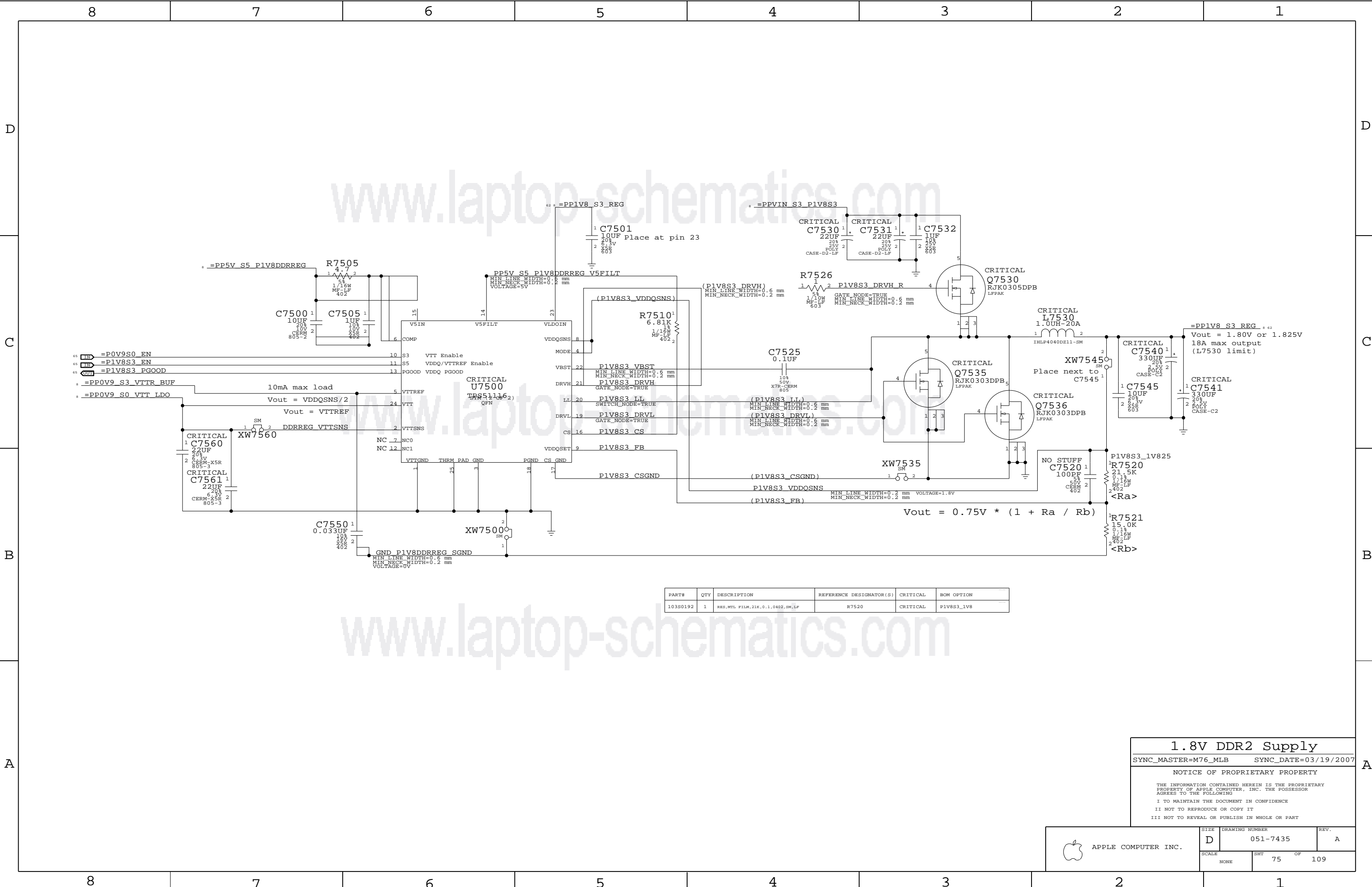


1.25V / 1.05V Power Supply
 SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---------------------------------|-------------------------|----------|------------|
| 10380192 | 1 | RES,MTL FILM,21K,0.1,0402,SM,LF | R7520 | CRITICAL | P1V8S3_1V8 |

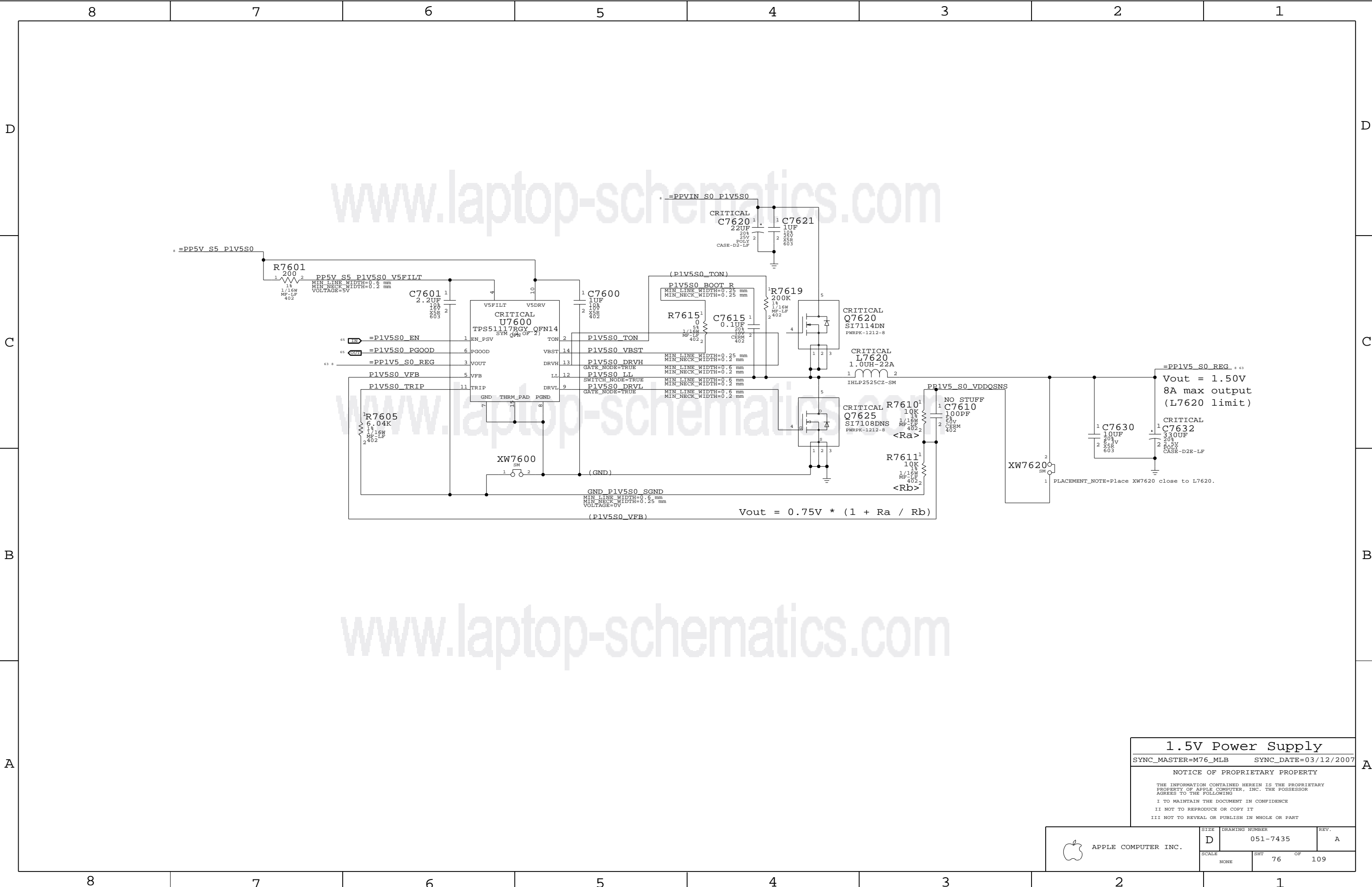
1.8V DDR2 Supply
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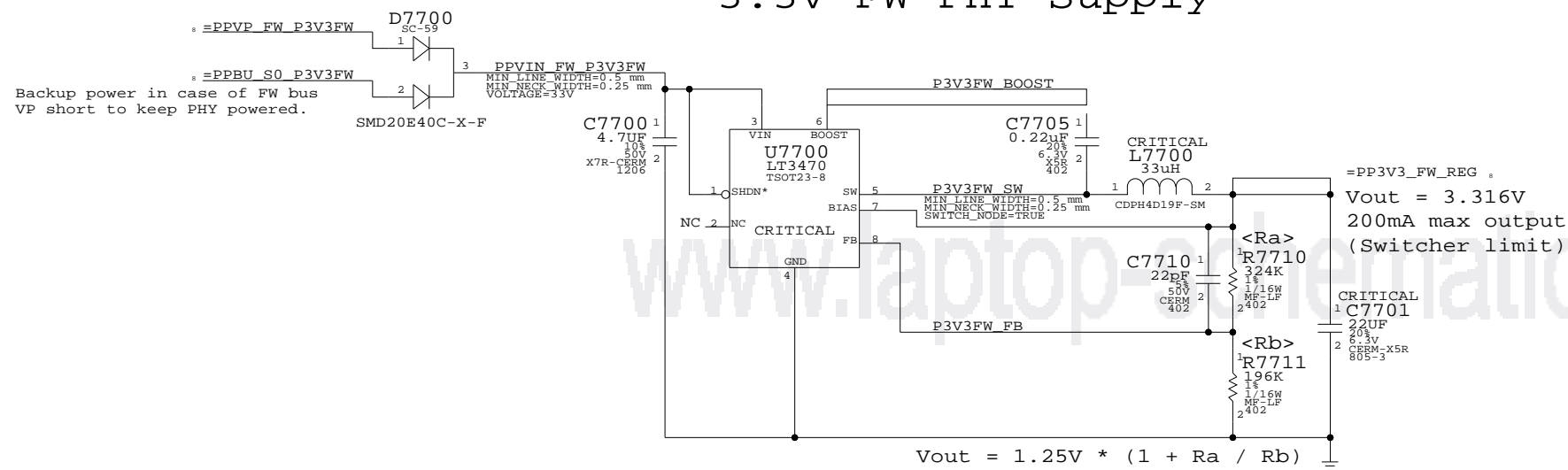
1.5V Power Supply
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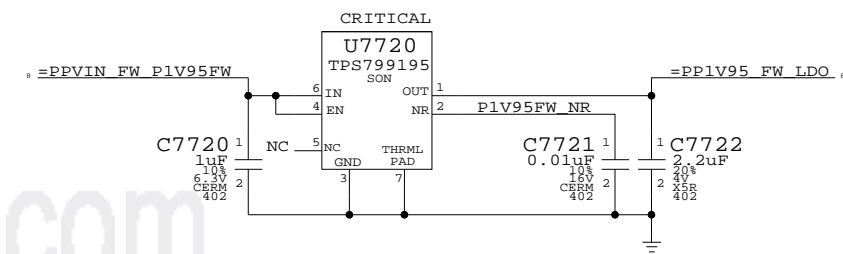
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3.3V FW PHY Supply



1.95V FW PHY Supply



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FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

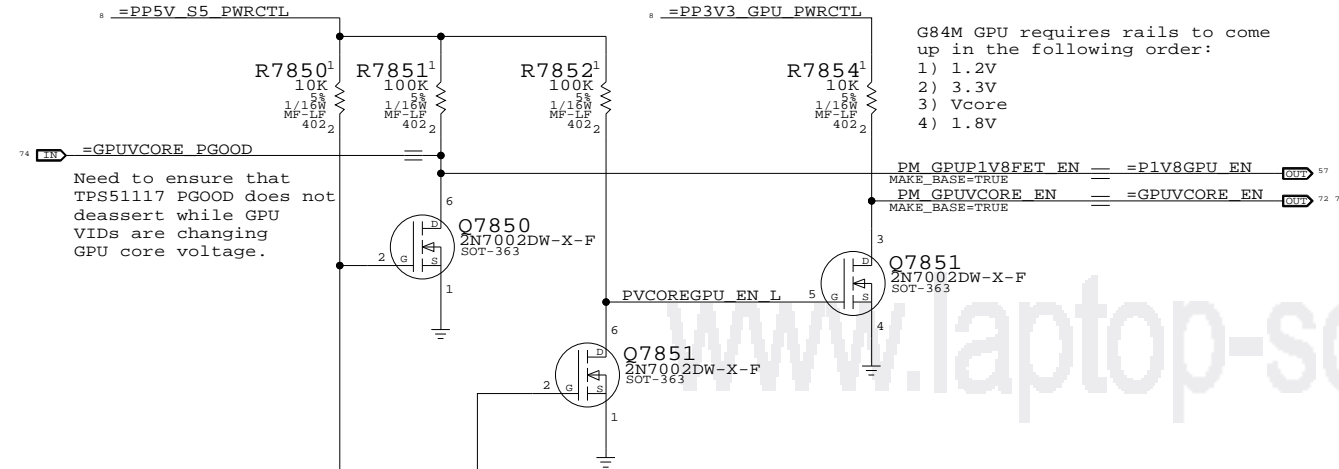
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Power Control Signals



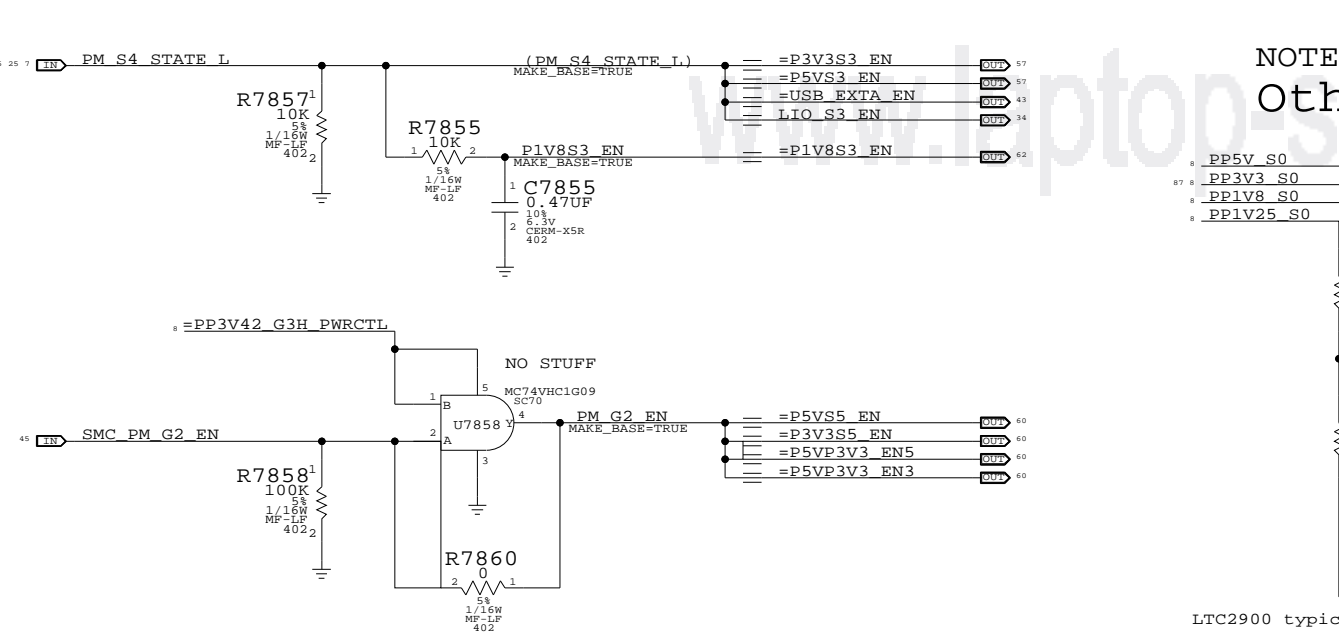
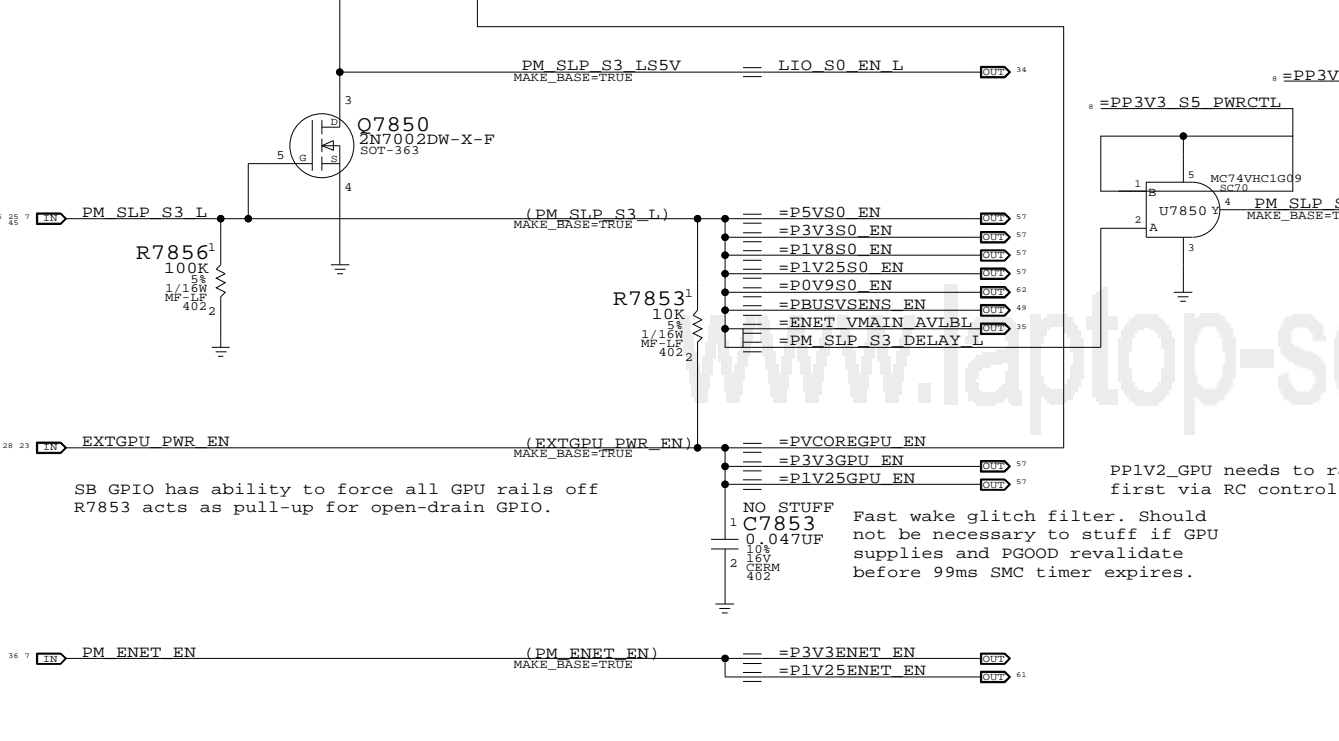
Need to ensure that TPS51117 PGOOD does not deassert while GPU VIDs are changing GPU core voltage.

SB GPIO has ability to force all GPU rails off R7853 acts as pull-up for open-drain GPIO.

G84M GPU requires rails to come up in the following order:
 1) 1.2V
 2) 3.3V
 3) Vcore
 4) 1.8V

Fast wake glitch filter. Should not be necessary to stuff if GPU supplies and PGOOD revalidate before 99ms SMC timer expires.

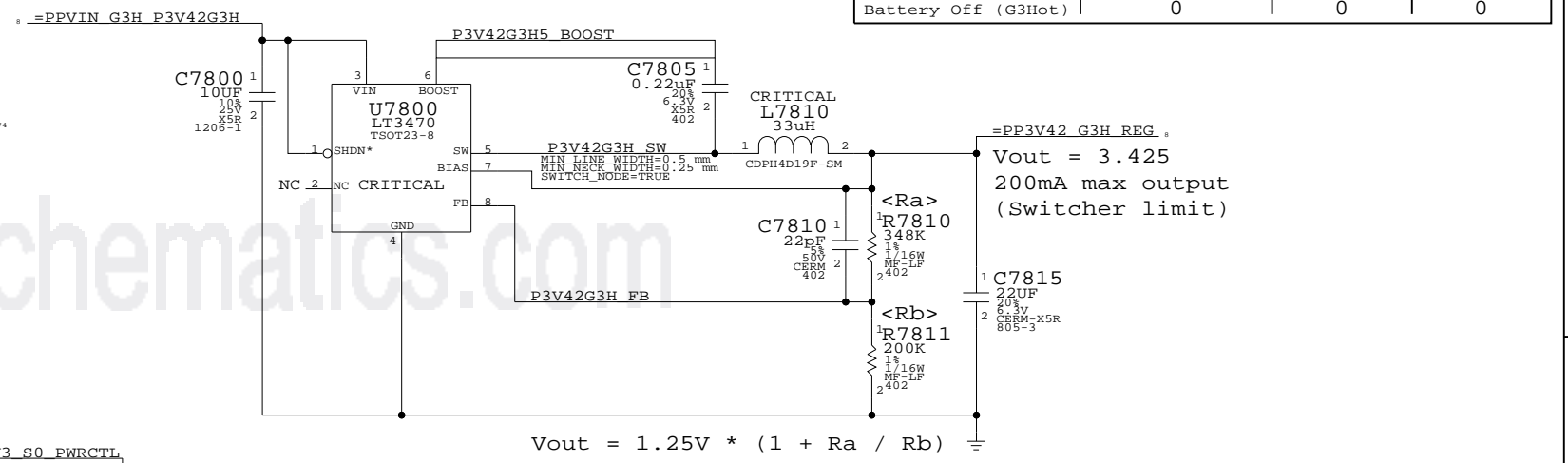
PP1V2_GPU needs to ramp first via RC control



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

| State | SMC_PM_G2_ENABLE | PM_SLP_S4_L | PM_SLP_S3_L |
|---------------------|------------------|-------------|-------------|
| Run (S0) | 1 | 1 | 1 |
| Sleep (S3) | 1 | 1 | 0 |
| Soft-Off (S5) | 1 | 0 | 0 |
| Battery Off (G3Hot) | 0 | 0 | 0 |



Vout = 3.425
 200mA max output
 (Switcher limit)

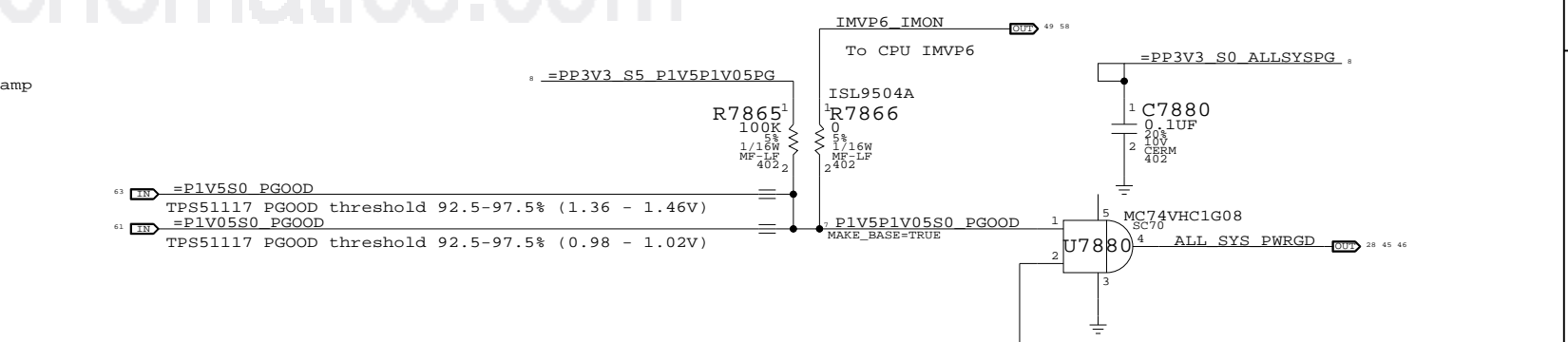
$$V_{out} = 1.25V * (1 + R_a / R_b)$$

Unused PGOOD Signals

- =P1V25ENET_PGOOD == TP_P1V25ENET_PGOOD
- =P1V8S3_PGOOD == TP_P1V8S3_PGOOD

1.5V / 1.05V PWRGD Circuit

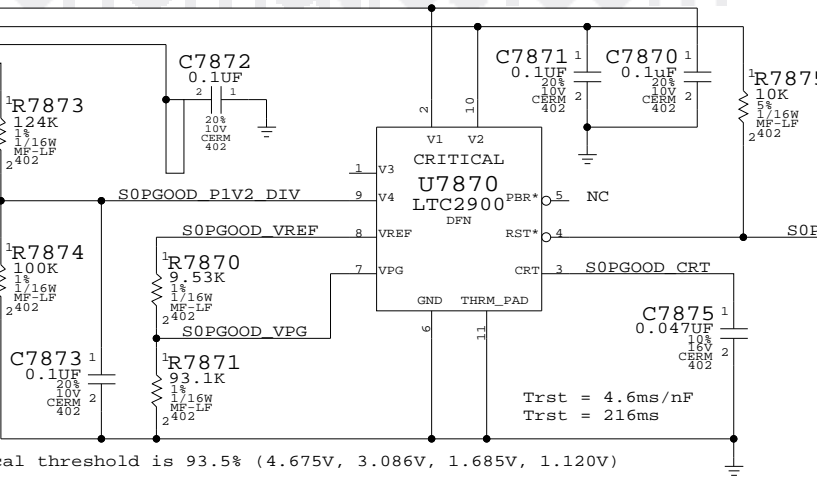
Reports when 1.5V S0 and 1.05V S0 are in regulation



- =P1V5S0_PGOOD
- TPS51117 PGOOD threshold 92.5-97.5% (1.36 - 1.46V)
- =P1V05S0_PGOOD
- TPS51117 PGOOD threshold 92.5-97.5% (0.98 - 1.02V)

NOTE: 0.9V/2.5V is not checked! Other S0 Rails PWRGD Circuit

Does not include GFX rails



LTC2900 typical threshold is 93.5% (4.675V, 3.086V, 1.685V, 1.120V)

3.425V G3Hot Supply & Power Control

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| NONE | 78 | 109 | |

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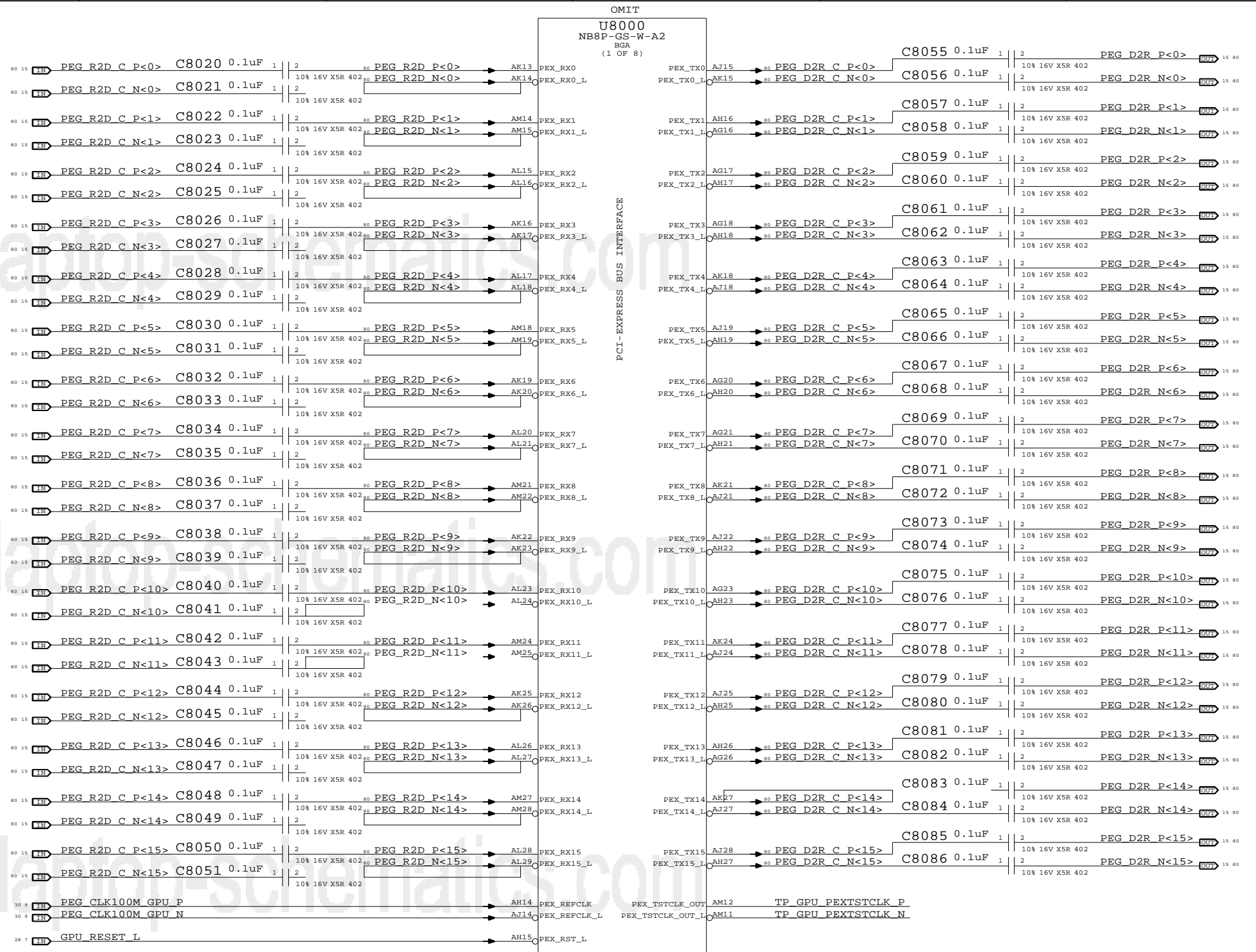
- =PPIV2_GPU_PEX_PLLXVDD
- =PPIV2_GPU_PEX_IOVDDQ
- =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



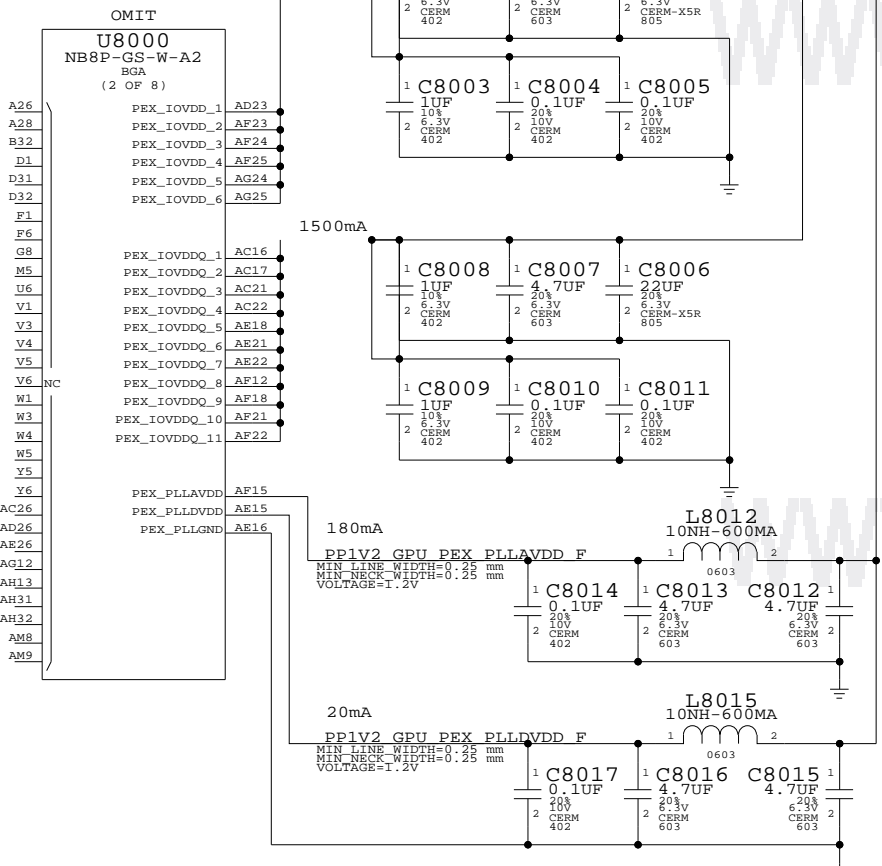
PEX 1.2V Current = 2A

250mA

1500mA

180mA

20mA



NV G84M PCI-E
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Page Notes

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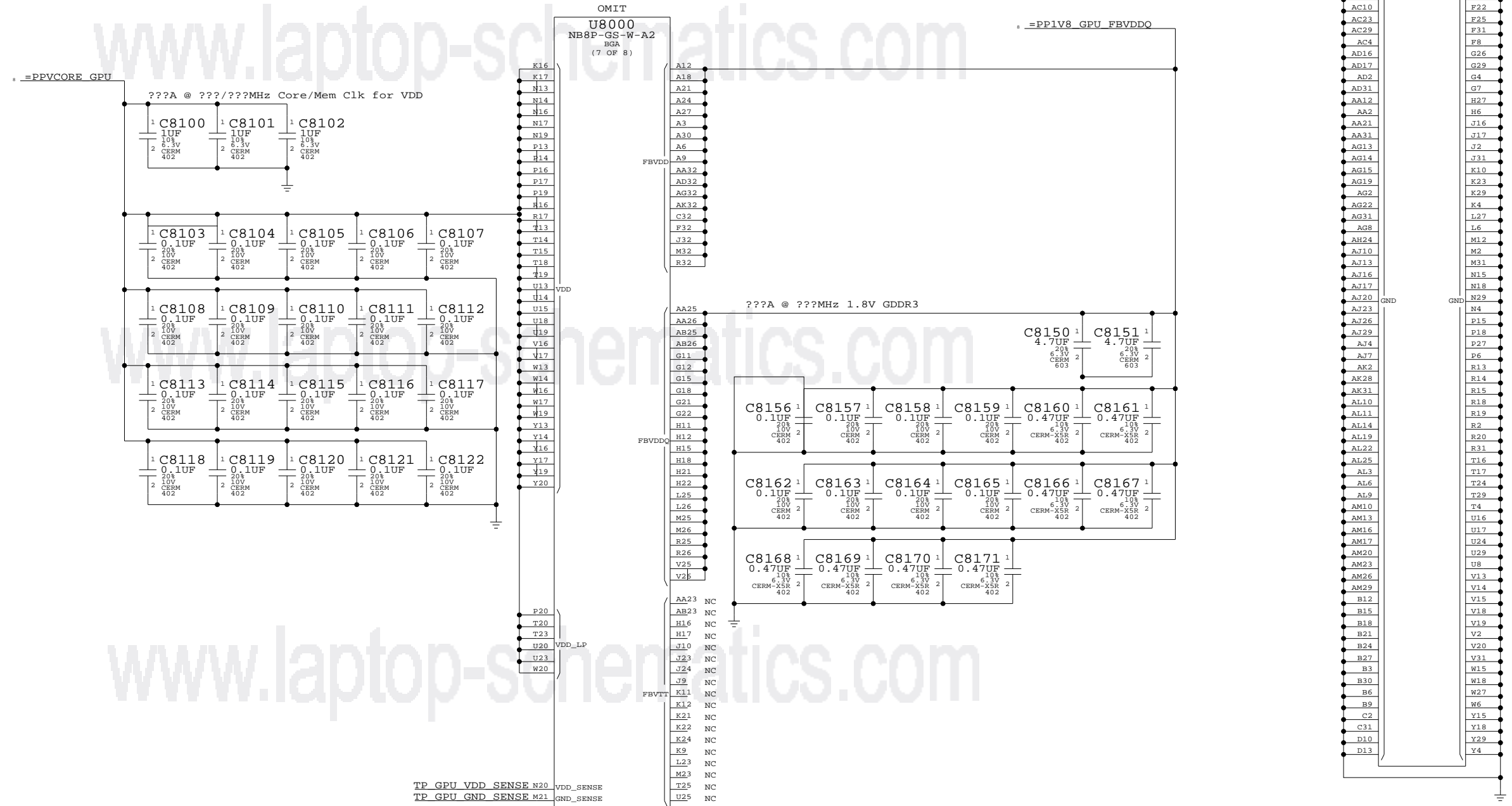
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



NV G84M Core/FB Power
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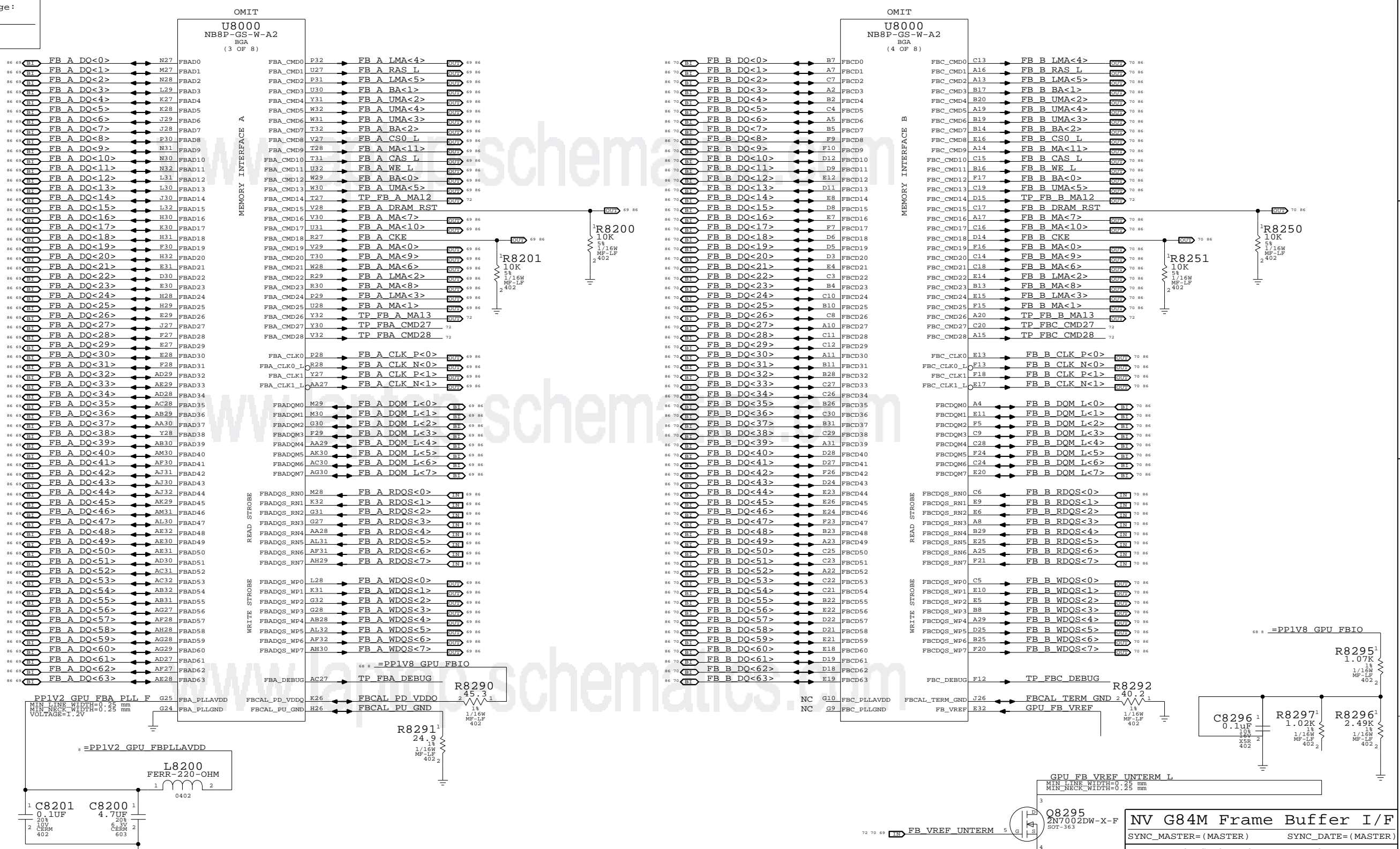
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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



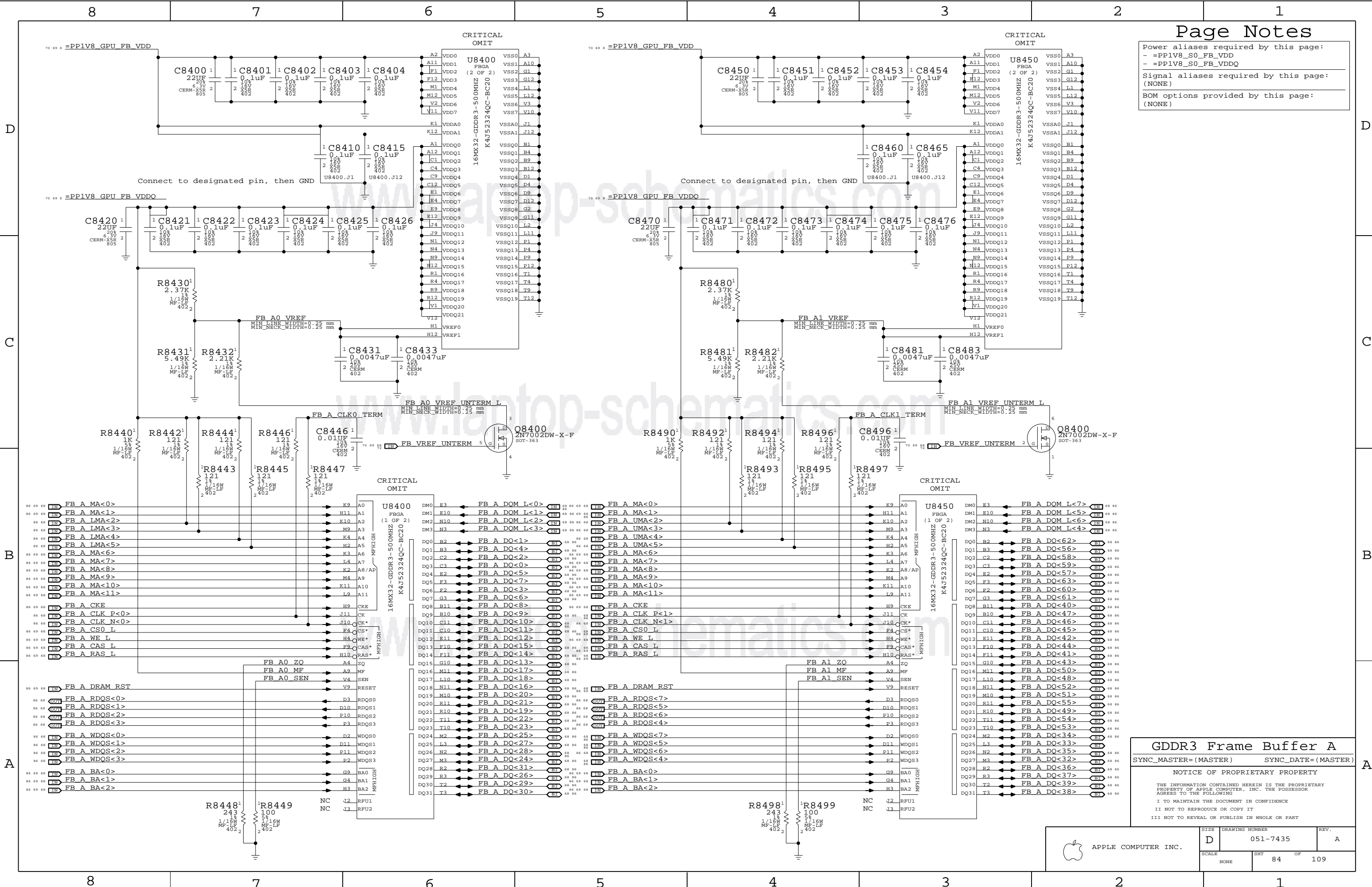
NV G84M Frame Buffer I/F
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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| SCALE | SHT | OF | |
| NONE | 82 | OF | 109 |

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Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
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GDDR3 Frame Buffer A

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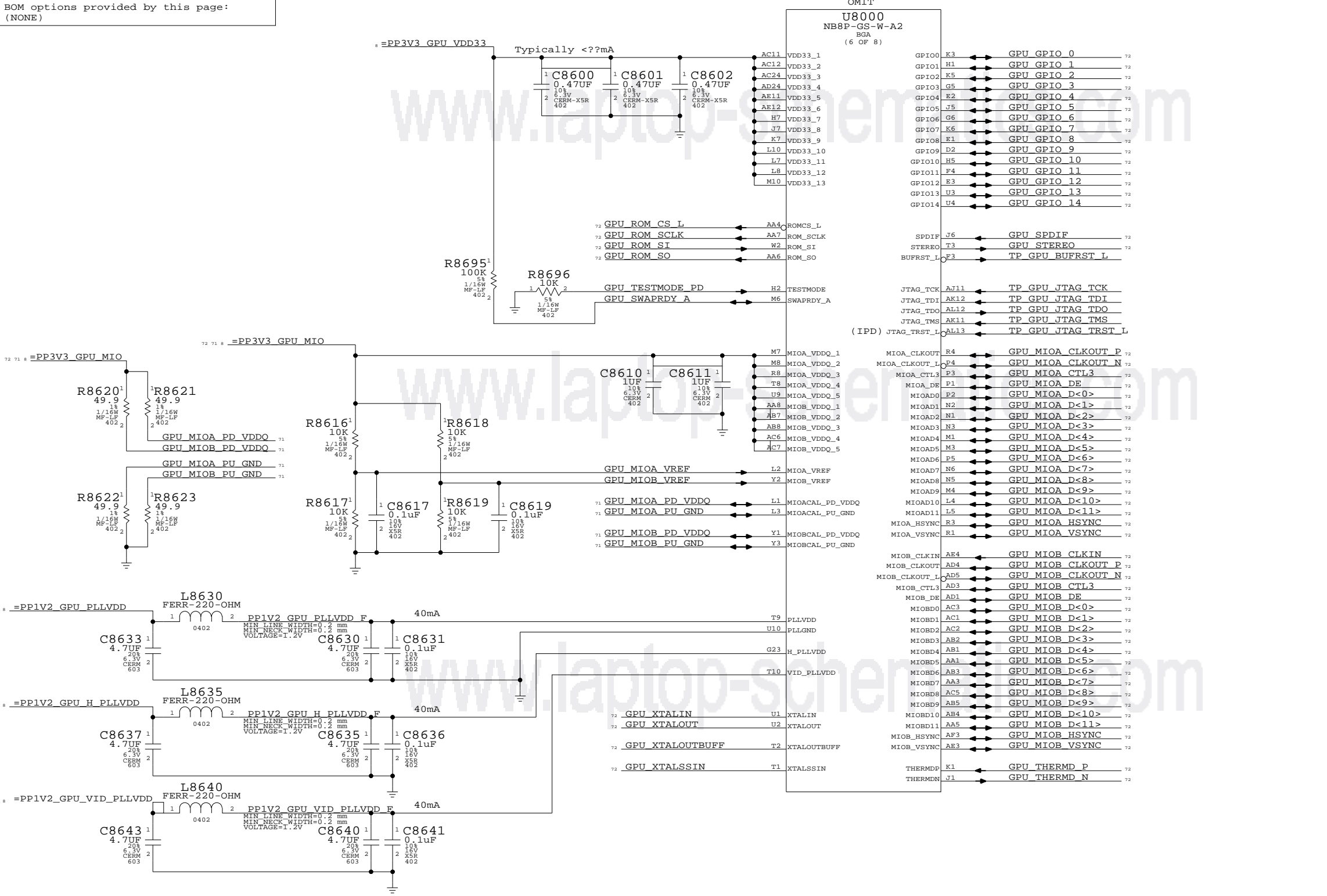
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Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_VDD33
 - =PP3V3_GPU_MIO
 - =PP1V2_GPU_PLLVDD
 - =PP1V2_GPU_H_PLLVDD
 - =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
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BOM options provided by this page:
 (NONE)



NV G84M GPIO/MIO/Misc

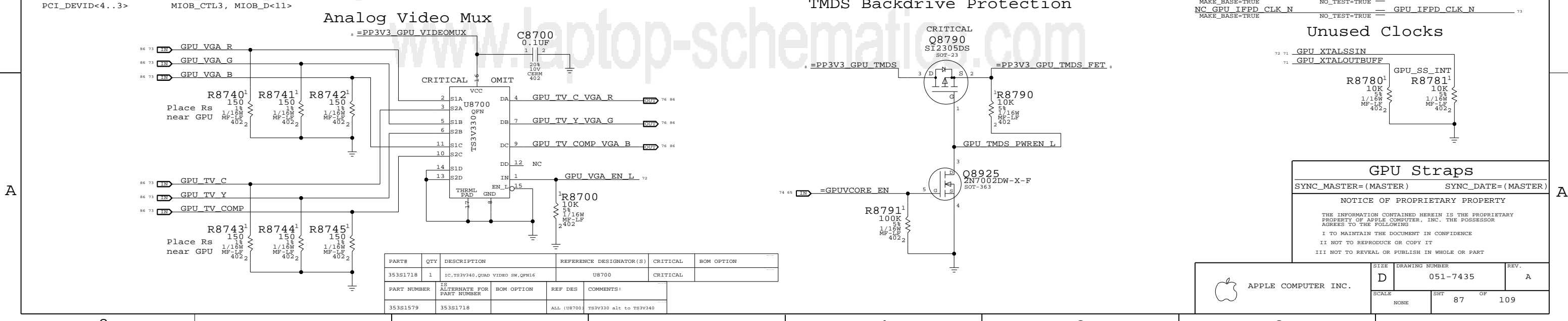
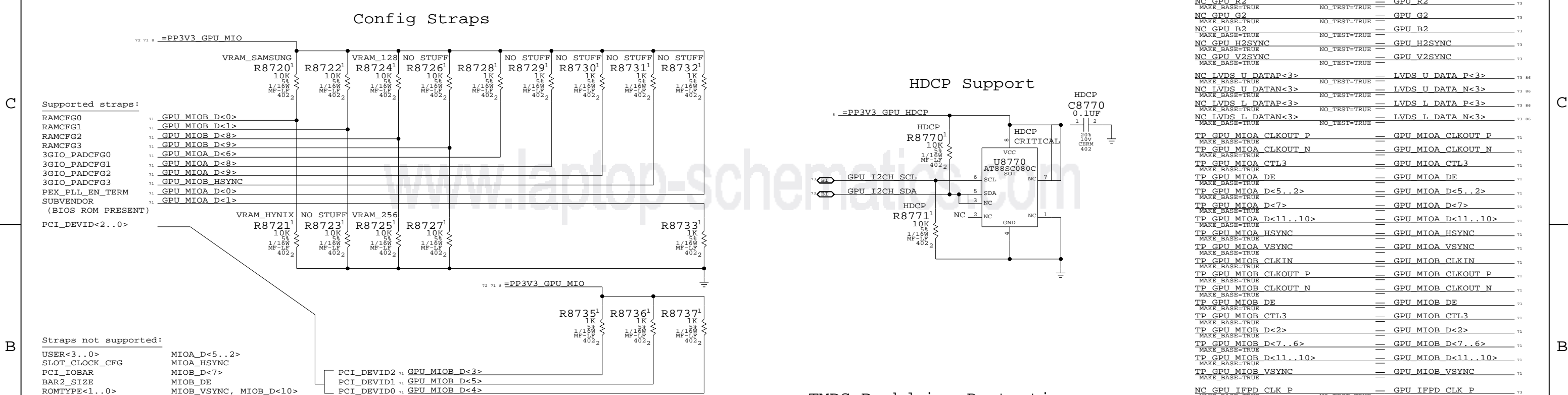
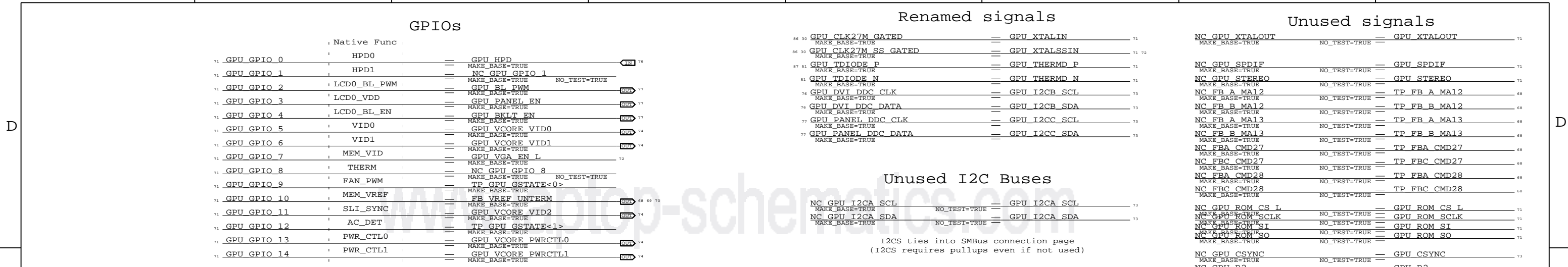
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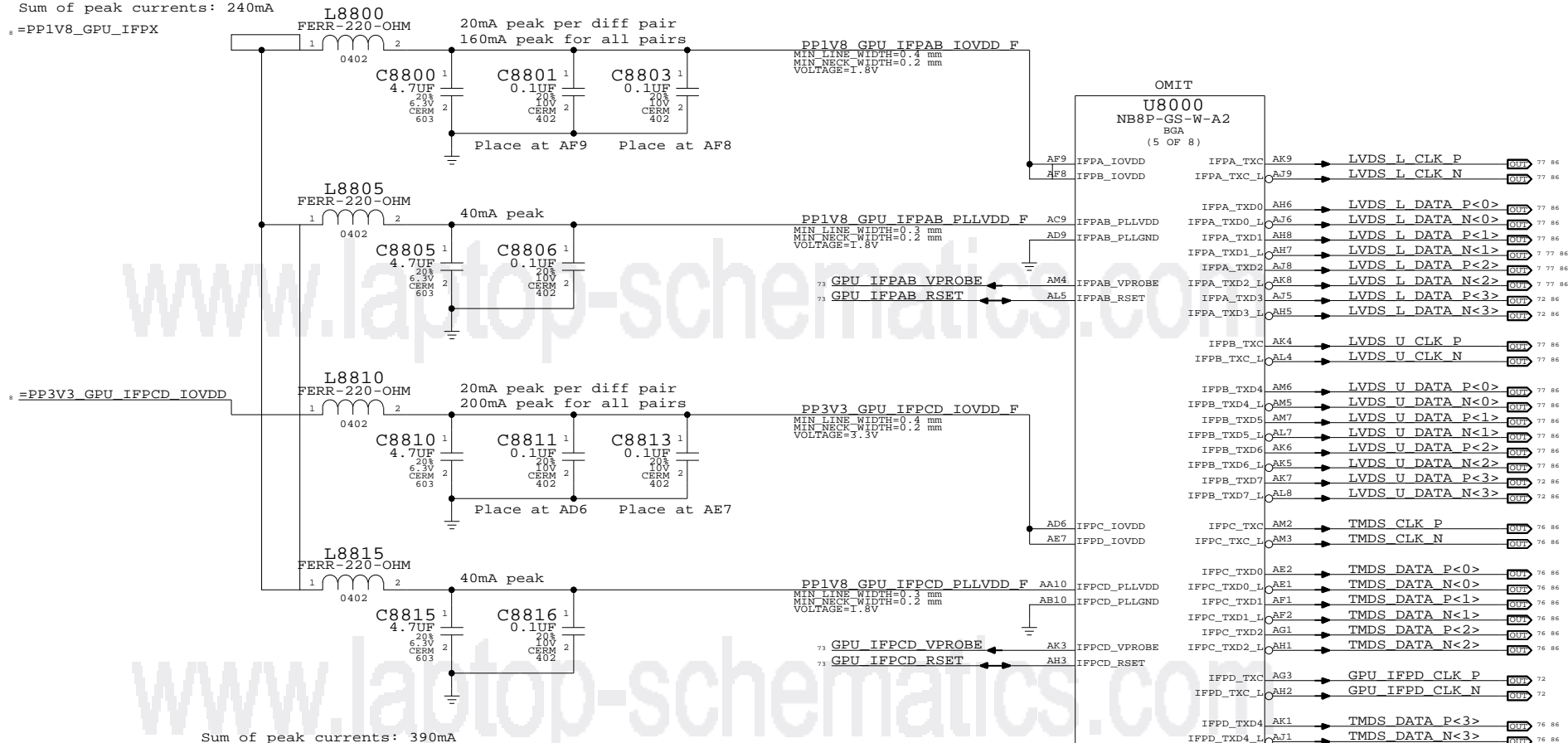
Page Notes

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 - =PP3V3_GPU_IFPCD_IOVDD
 - =PP3V3_GPU_DAC

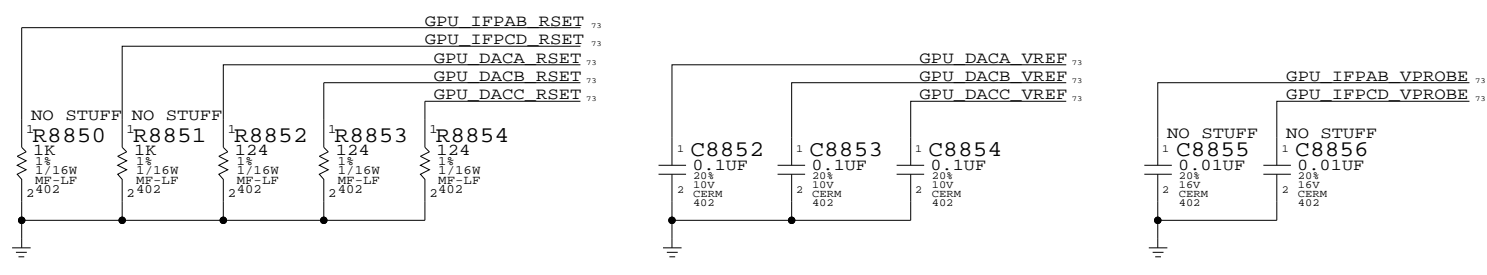
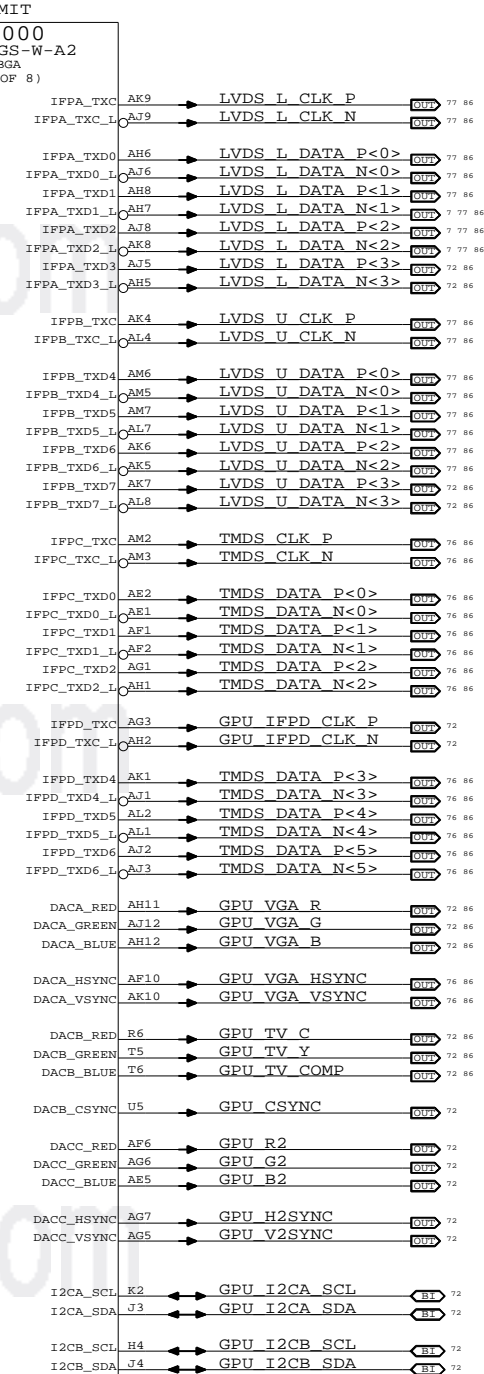
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Sum of peak currents: 240mA
 =PP1V8_GPU_IFPX



| Composite/S-Video | VGA | Component |
|-------------------|-----|-----------|
| C | R | Pr |
| Y | G | Y |
| Comp | B | Pb |



NV G84M Video Interfaces
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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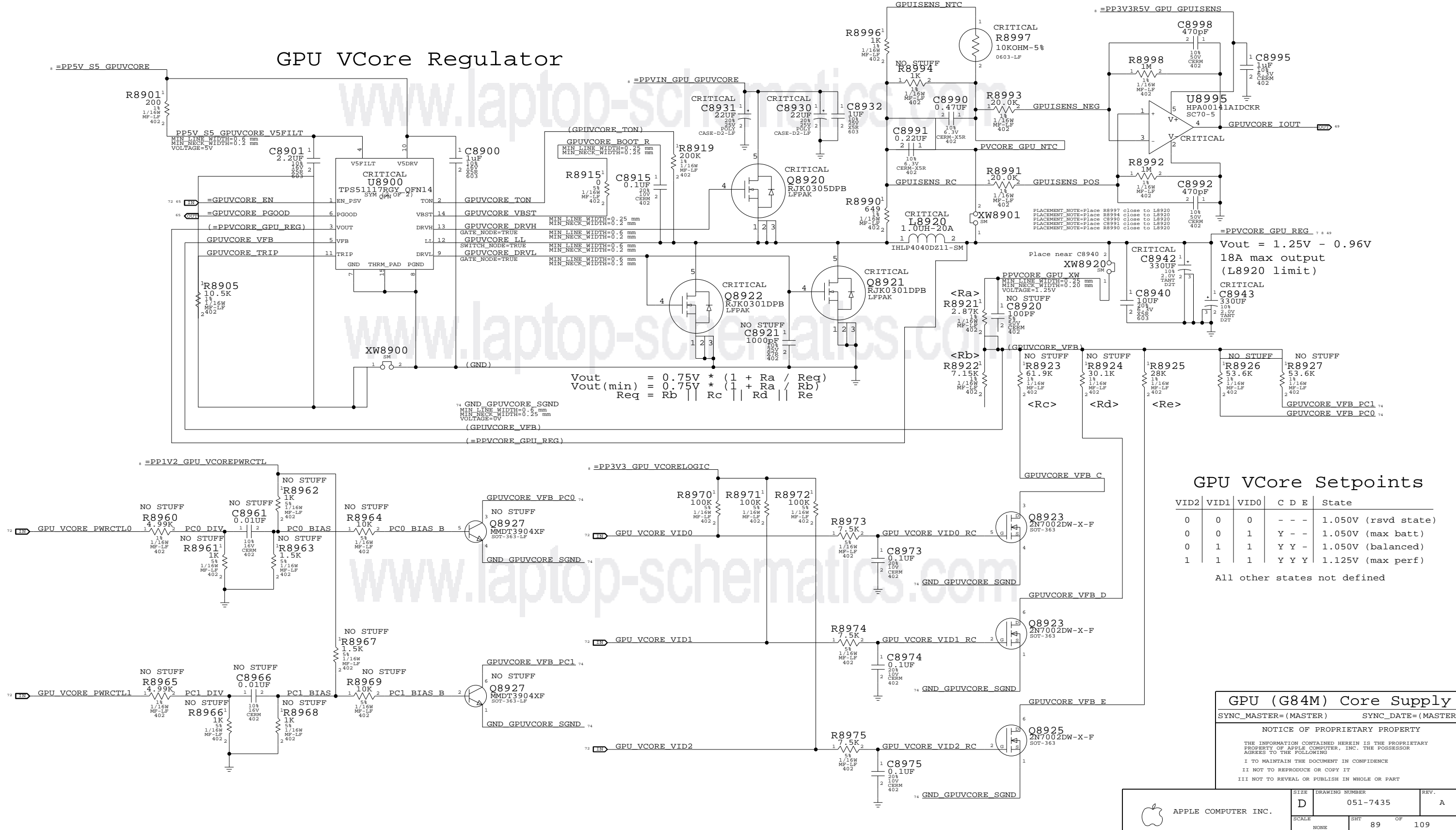
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GPU VCore Regulator

GPU VCore Current Sense



$$V_{out} = 1.25V - 0.96V$$

$$18A \text{ max output (L8920 limit)}$$

$$V_{out}(\min) = 0.75V * (1 + R_a / R_{eq})$$

$$R_{eq} = R_b || R_c || R_d || R_e$$

GPU VCore Setpoints

| VID2 | VID1 | VID0 | C | D | E | State |
|------|------|------|---|---|---|---------------------|
| 0 | 0 | 0 | - | - | - | 1.050V (rsvd state) |
| 0 | 0 | 1 | Y | - | - | 1.050V (max batt) |
| 0 | 1 | 1 | Y | Y | - | 1.050V (balanced) |
| 1 | 1 | 1 | Y | Y | Y | 1.125V (max perf) |

All other states not defined

GPU (G84M) Core Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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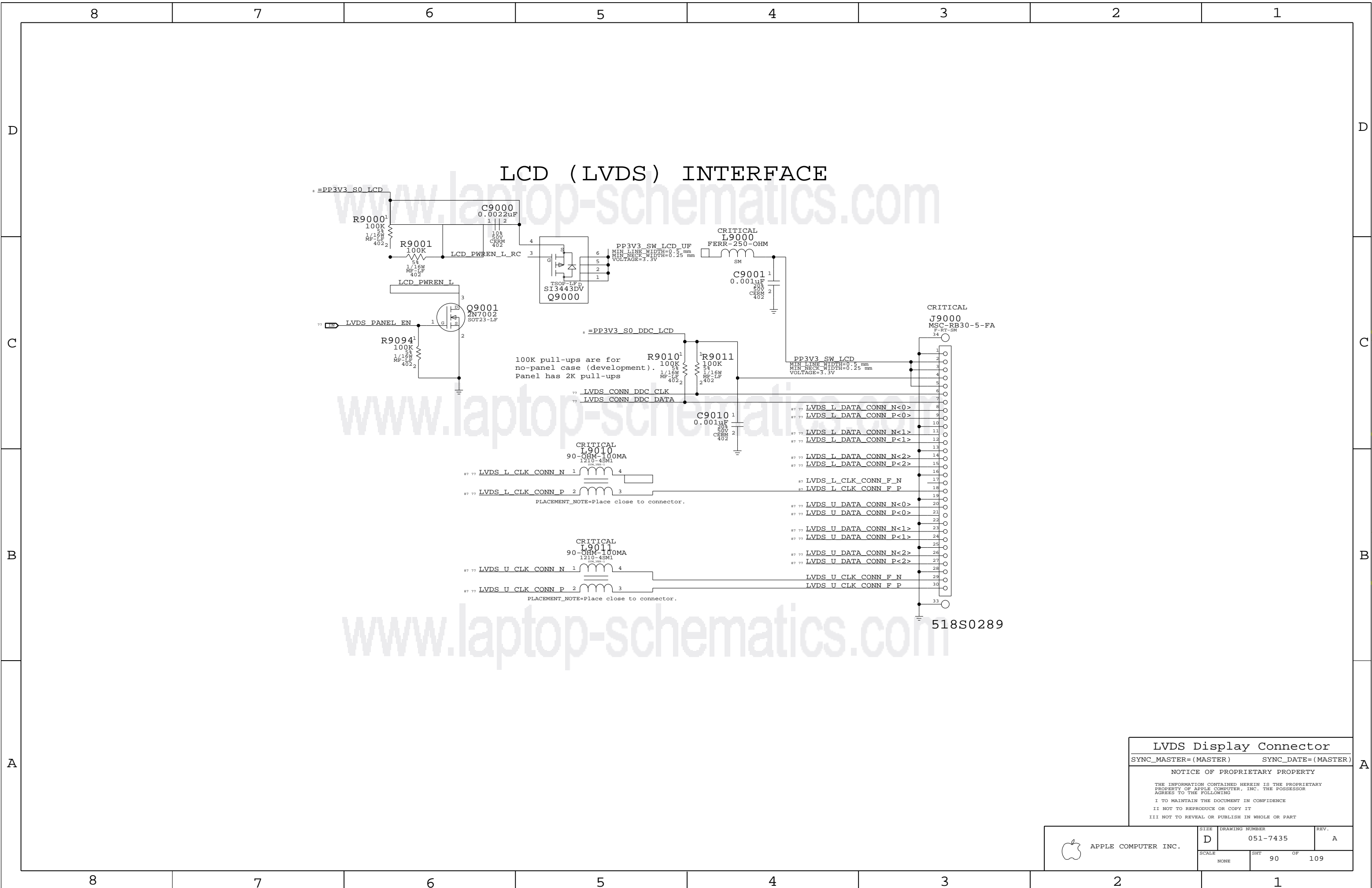
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LVDS Display Connector
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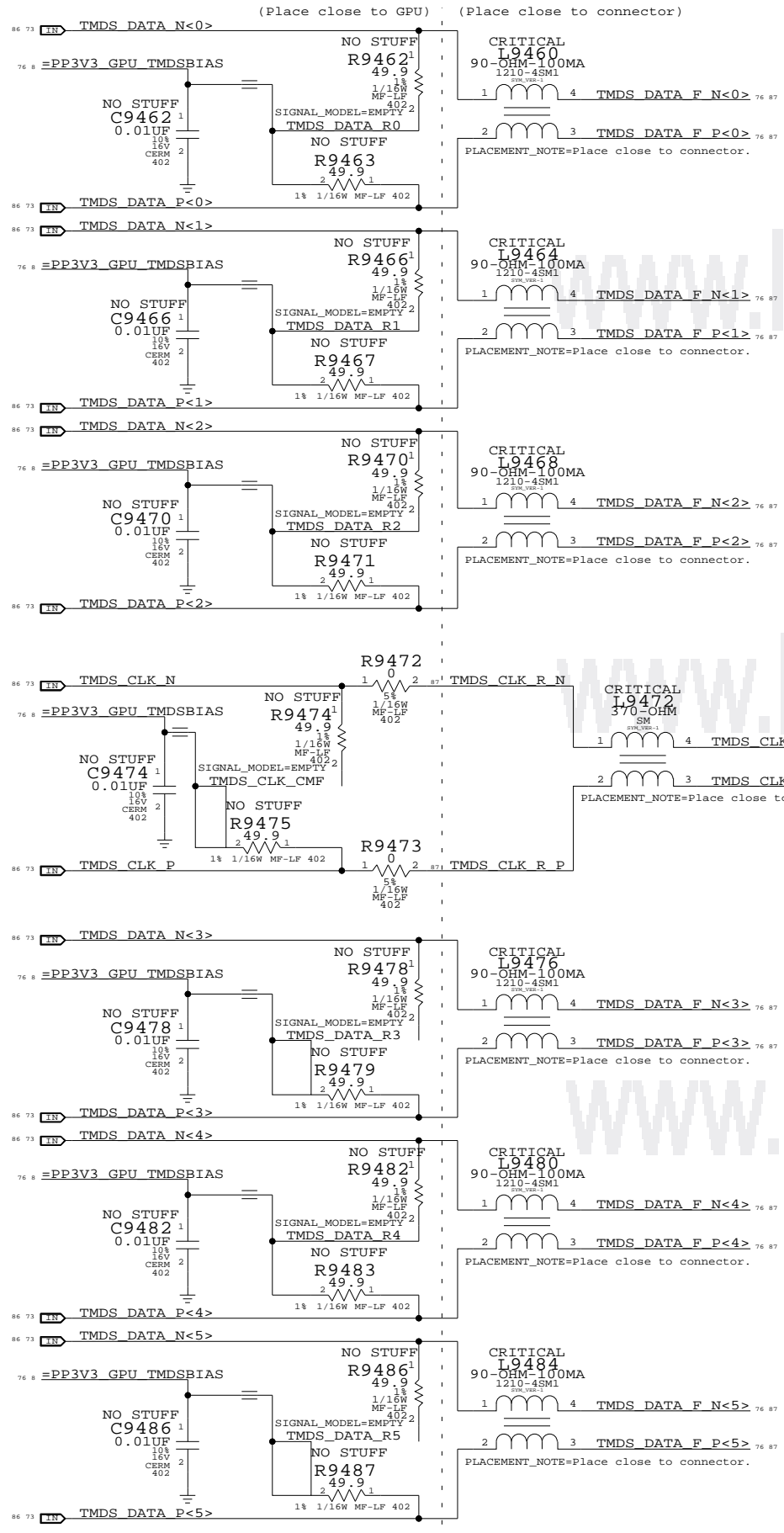
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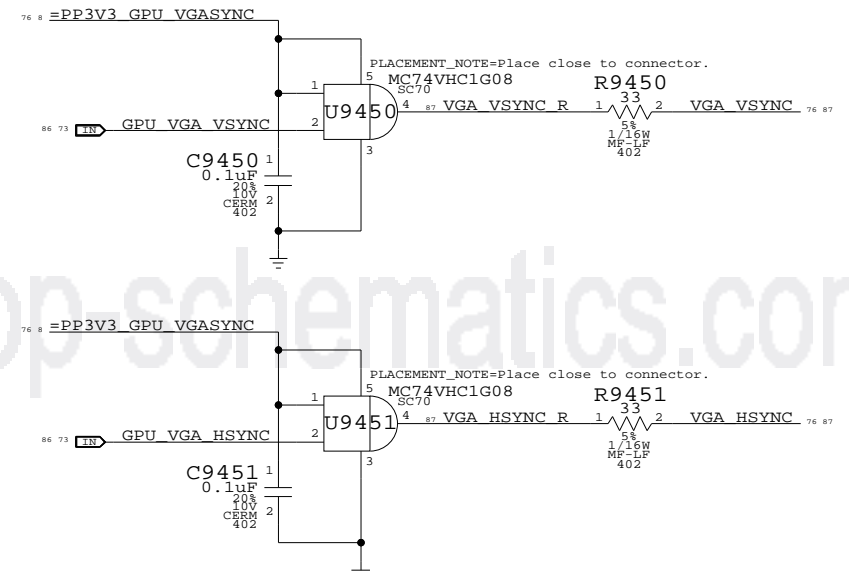
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|---------------------|------------------|----------------------------|-----------|
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| | SCALE NONE | SHIT 90 | OF 109 |

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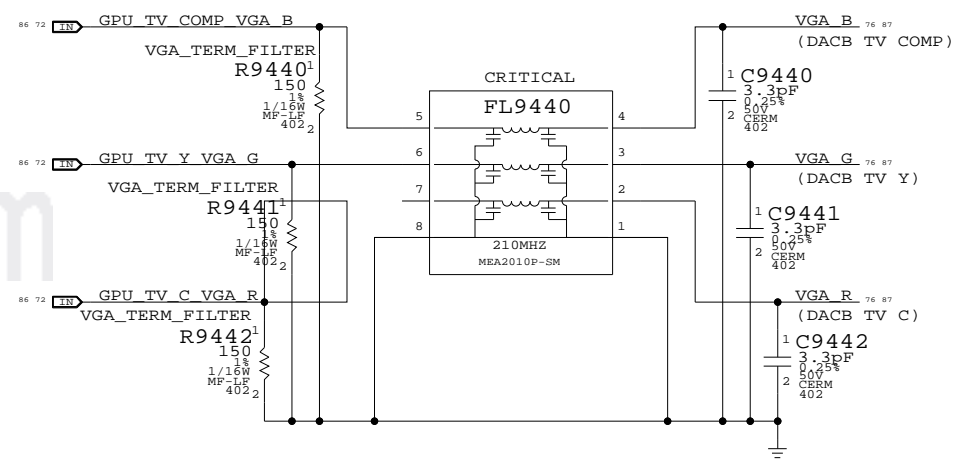
TMDS Filtering



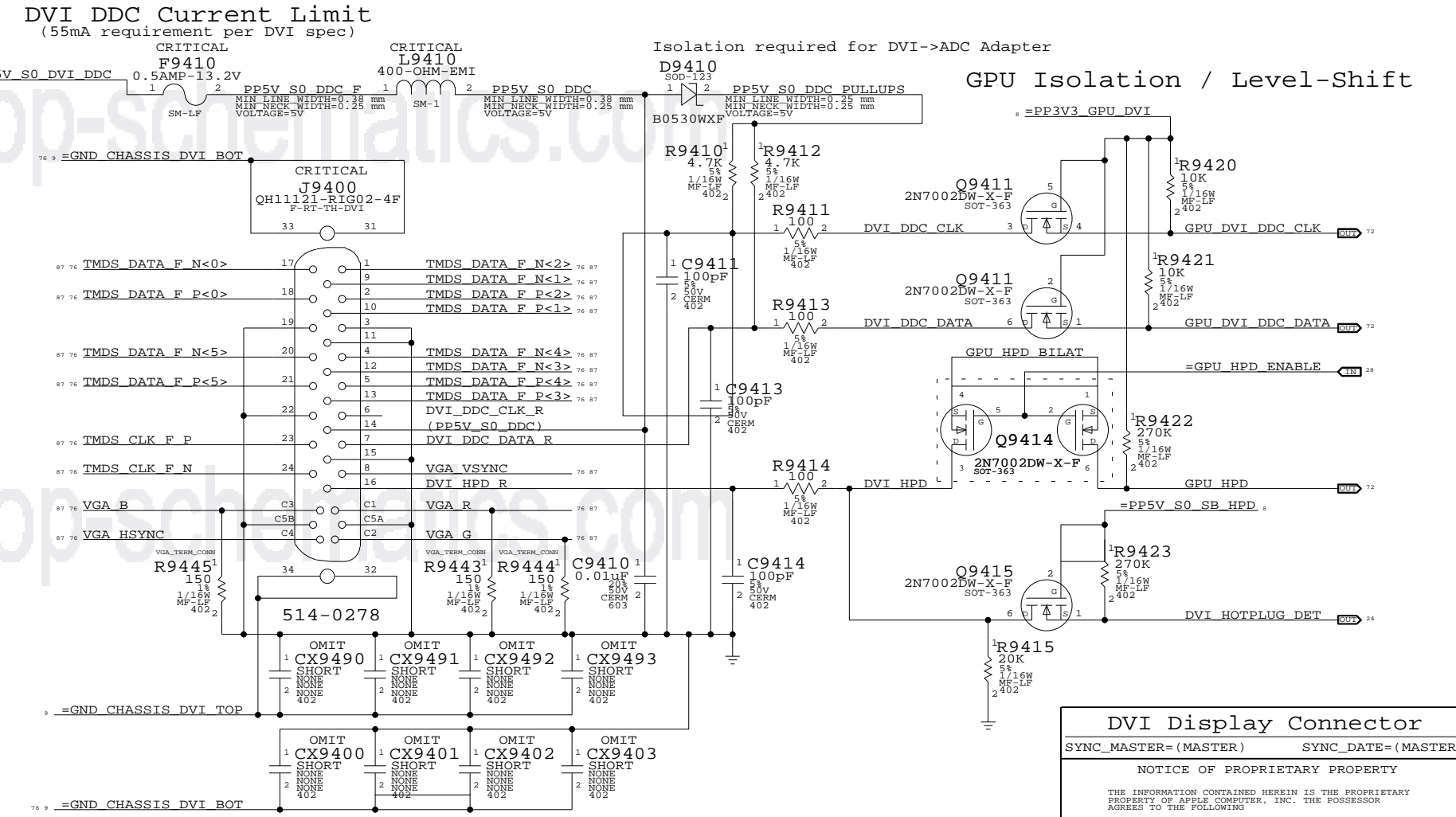
VGA SYNC Buffers



ANALOG FILTERING PLACE CLOSE TO CONNECTOR



DVI INTERFACE

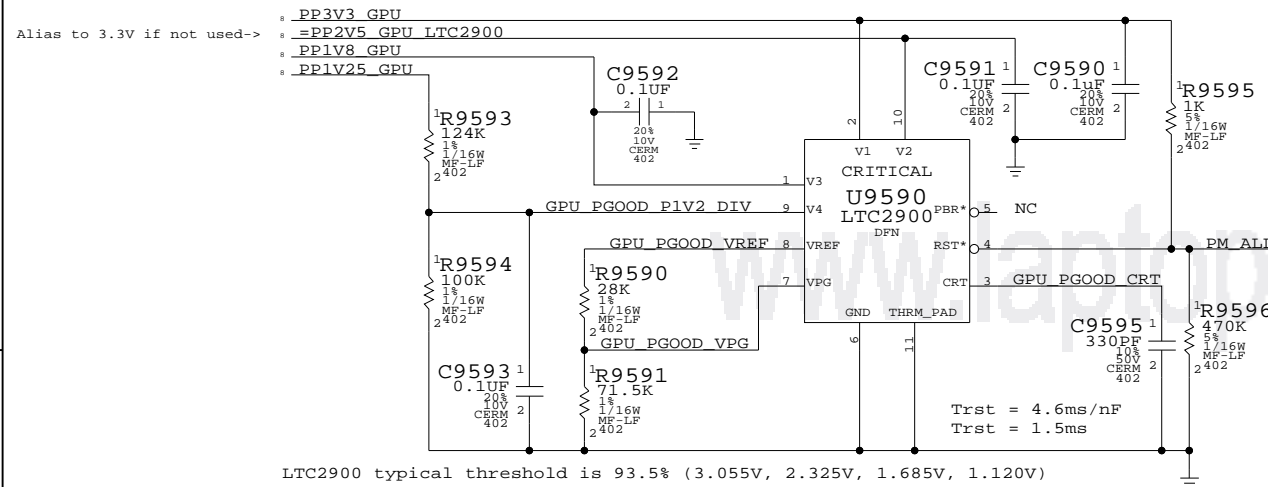


DVI Display Connector
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PGOOD Monitor for GPU Rails

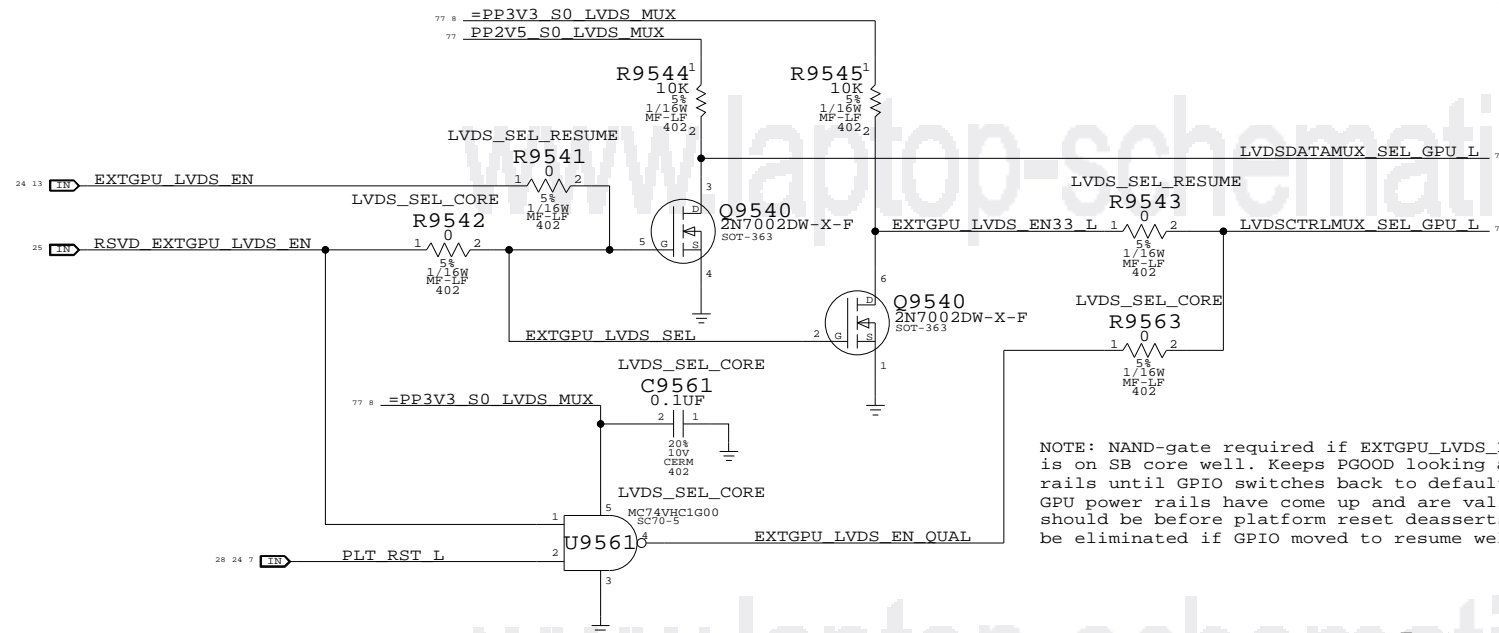
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

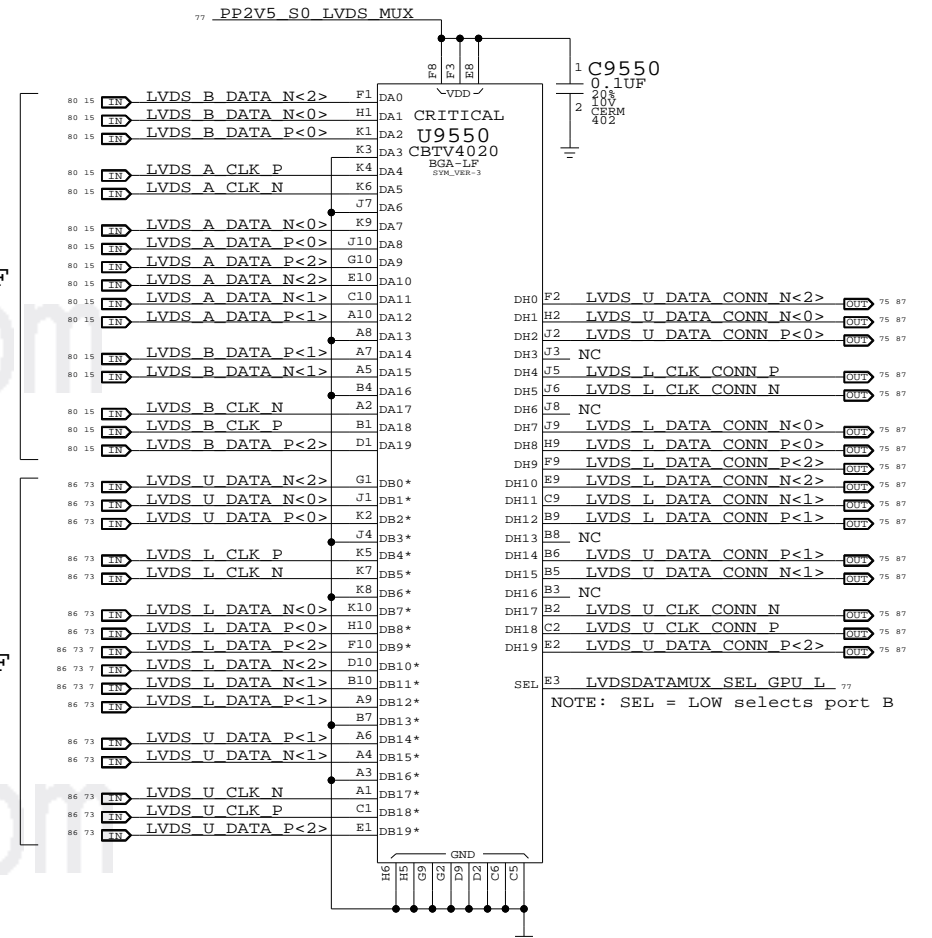
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

Mux Select Conditioning



NOTE: NAND-gate required if EXTGPU_LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

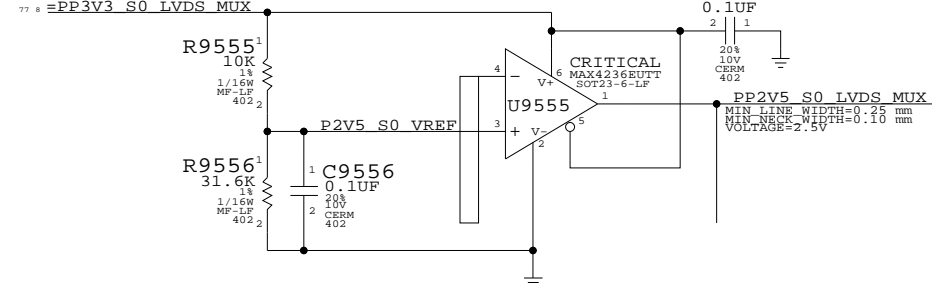
LVDS I/F Mux



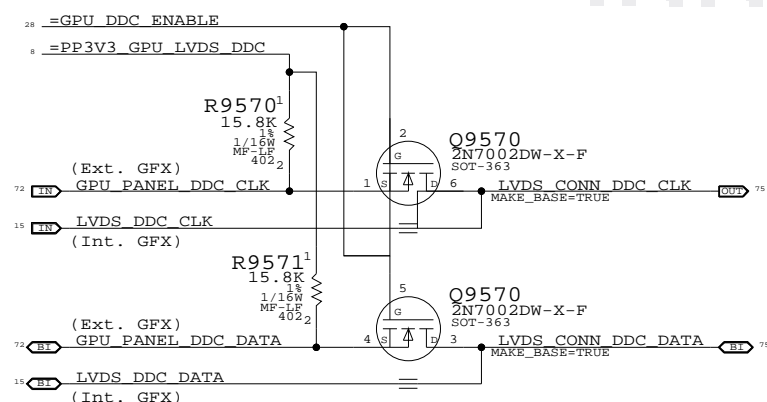
NB LVDS I/F

GPU LVDS I/F

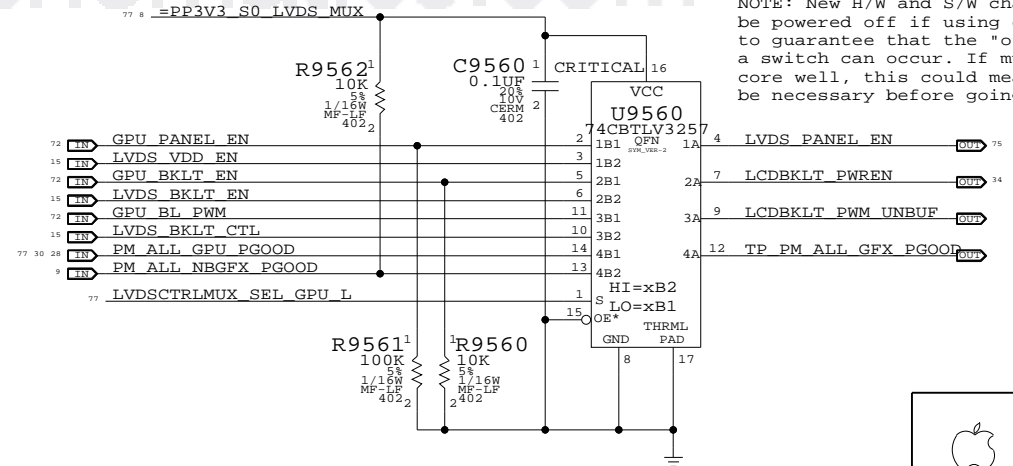
LVDS Data Mux Power Supply



GPU DDC Pass FETs



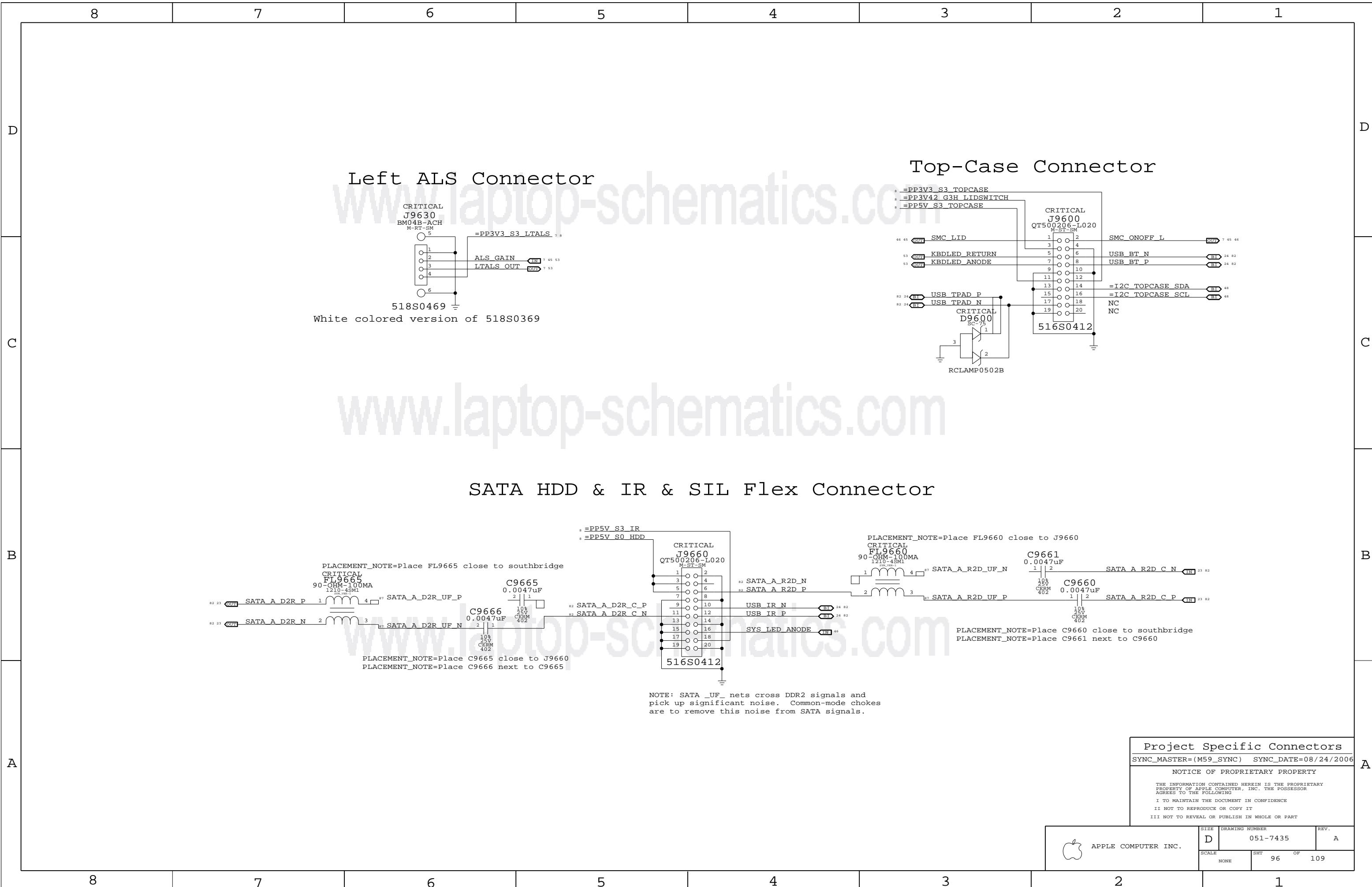
Panel/Backlight Control Mux



NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

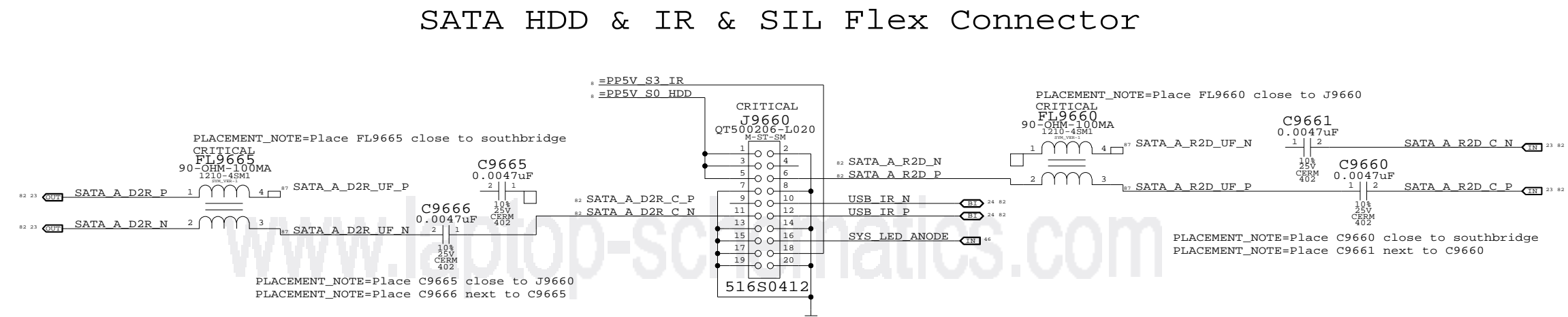
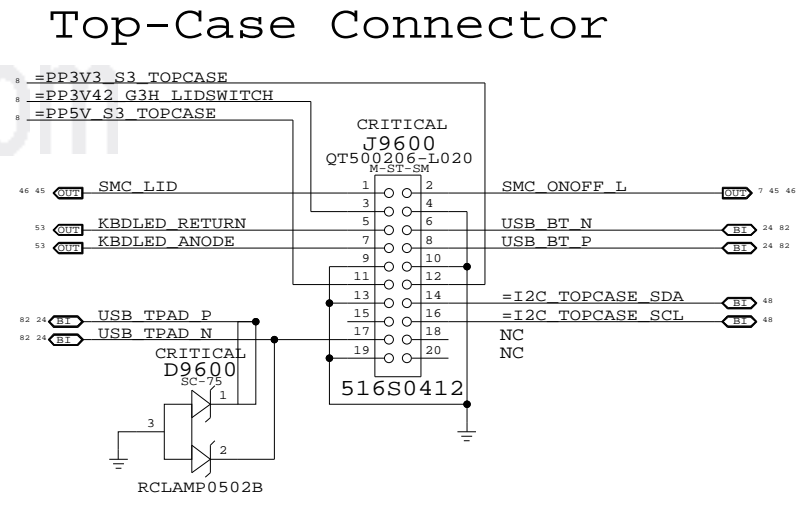
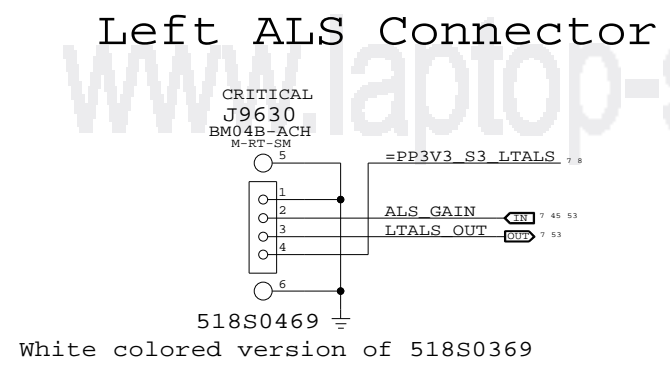
LVDS Interface Mux

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NOTE: SATA_UF_nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

Project Specific Connectors
 SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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| NONE | 96 | 109 | |

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FSB (Front-Side Bus) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FSB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| FSB_DSTB_55S | * | =1:1_DIFFPAIR | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =1:1_DIFFPAIR | =1:1_DIFFPAIR |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FSB_ADDR | * | =3:1_SPACING | ? |
| FSB_ADDR2ADDR | * | =2:1_SPACING | ? |
| FSB_ADSTB | * | =3:1_SPACING | ? |
| FSB_ADDR2ADSTB | * | =3:1_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FSB_DATA | * | =3:1_SPACING | ? |
| FSB_DATA2DATA | * | =2:1_SPACING | ? |
| FSB_DSTB | * | =3:1_SPACING | ? |
| FSB_DATA2DSTB | * | =3:1_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FSB_COMMON | * | =2:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| FSB_ADDR | FSB_ADDR | * | FSB_ADDR2ADDR |
| FSB_ADDR | FSB_ADSTB | * | FSB_ADDR2ADSTB |
| FSB_DATA | FSB_DATA | * | FSB_DATA2DATA |
| FSB_DATA | FSB_DSTB | * | FSB_DATA2DSTB |

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_27P4S | * | Y | =27P4_OHM_SE | =27P4_OHM_SE | =27P4_OHM_SE | 7 MIL | 7 MIL |
| CPU_55S | * | Y | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_2T01 | * | =2:1_SPACING | ? |
| CPU_COMP | * | 25 MIL | ? |
| CPU_GTLREF | * | 25 MIL | ? |
| CPU_ITP | * | =2:1_SPACING | ? |
| CPU_VCCSENSE | * | 25 MIL | ? |

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|--------------|--------------|-----------------|---------------|
| | PHYSICAL | SPACING | | |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB ADS L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB BNR L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB BPRI L | 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB BRQ0 L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB DBSY L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB DEFER L | 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB DPWR L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB DRDY L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB HIT L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB HITM L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB LOCK L | 7 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB RS L<2..0> | 10 14 |
| FSB_COMMON | FSB_55S | FSB_COMMON | FSB TRDY L | 10 14 |
| FSB_CPURST_L | FSB_55S | FSB_COMMON | FSB CPURST L | 7 10 13 14 |
| FSB_DATA_GROUP0 | FSB_55S | FSB_DATA | FSB D L<15..0> | 7 10 14 |
| FSB_DATA_GROUP0 | FSB_55S | FSB_DATA | FSB DINV L<0> | 7 10 14 |
| FSB_DSTB0 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L P<0> | 7 10 14 |
| FSB_DSTB0 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L N<0> | 7 10 14 |
| FSB_DATA_GROUP1 | FSB_55S | FSB_DATA | FSB D L<31..16> | 7 10 14 |
| FSB_DATA_GROUP1 | FSB_55S | FSB_DATA | FSB DINV L<1> | 7 10 14 |
| FSB_DSTB1 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L P<1> | 7 10 14 |
| FSB_DSTB1 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L N<1> | 7 10 14 |
| FSB_DATA_GROUP2 | FSB_55S | FSB_DATA | FSB D L<47..32> | 7 10 14 |
| FSB_DATA_GROUP2 | FSB_55S | FSB_DATA | FSB DINV L<2> | 7 10 14 |
| FSB_DSTB2 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L P<2> | 7 10 14 |
| FSB_DSTB2 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L N<2> | 7 10 14 |
| FSB_DATA_GROUP3 | FSB_55S | FSB_DATA | FSB D L<63..48> | 7 10 14 |
| FSB_DATA_GROUP3 | FSB_55S | FSB_DATA | FSB DINV L<3> | 7 10 14 |
| FSB_DSTB3 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L P<3> | 7 10 14 |
| FSB_DSTB3 | FSB_DSTB_55S | FSB_DSTB | FSB DSTB L N<3> | 7 10 14 |
| FSB_ADDR_GROUP0 | FSB_55S | FSB_ADDR | FSB A L<16..3> | 7 10 14 |
| FSB_ADDR_GROUP0 | FSB_55S | FSB_ADDR | FSB REQ L<4..0> | 7 10 14 |
| FSB_ADSTB0 | FSB_55S | FSB_ADSTB | FSB ADSTB L<0> | 7 10 14 |
| FSB_ADDR_GROUP1 | FSB_55S | FSB_ADDR | FSB A L<35..17> | 7 10 14 |
| FSB_ADSTB1 | FSB_55S | FSB_ADSTB | FSB ADSTB L<1> | 7 10 14 |
| CPU_IERR_L | CPU_55S | | CPU IERR L | 10 |
| CPU_FERR_L | CPU_55S | | CPU FERR L | 10 23 |
| CPU_PROCHOT_L | CPU_55S | CPU_2T01 | CPU PROCHOT L | 10 46 58 |
| CPU_PWRGD | CPU_55S | | CPU PWRGD | 7 10 13 23 |
| CPU_FRGM_SB | CPU_55S | | CPU INTR | 10 23 |
| CPU_FRGM_SB | CPU_55S | | CPU NMI | 10 23 |
| CPU_FRGM_SB | CPU_55S | | CPU A20M L | 10 23 |
| CPU_FRGM_SB | CPU_55S | | CPU DPSLP L | 7 10 23 |
| CPU_FRGM_SB | CPU_55S | | CPU IGNE L | 10 23 |
| CPU_INIT_L | CPU_55S | | CPU INIT L | 10 23 47 |
| CPU_FRGM_SB | CPU_55S | | CPU SMI L | 10 23 |
| CPU_FRGM_SB | CPU_55S | | CPU STPCLK L | 7 10 23 |
| PM_THRMTRIP_L | CPU_55S | CPU_2T01 | PM THRMTRIP L | 10 16 23 46 |
| FSB_CPUSLP_L | CPU_55S | | FSB CPUSLP L | 7 10 14 |
| PM_DPRSLEVR | CPU_55S | CPU_2T01 | PM DPRSLPVR | 7 16 25 58 |
| (See above) | CPU_55S | CPU_2T01 | IMVP DPRSLPVR | 7 8 |
| CPU_BSEL0 | CPU_55S | CPU_2T01 | CPU BSEL<0> | 10 30 |
| (See above) | CPU_55S | CPU_2T01 | NB BSEL<0> | 13 16 30 |
| CPU_BSEL1 | CPU_55S | CPU_2T01 | CPU BSEL<1> | 10 30 |
| (See above) | CPU_55S | CPU_2T01 | NB BSEL<1> | 13 16 30 |
| CPU_BSEL2 | CPU_55S | CPU_2T01 | CPU BSEL<2> | 10 30 |
| (See above) | CPU_55S | CPU_2T01 | NB BSEL<2> | 13 16 30 |
| CPU_DPRSTP_L | CPU_55S | CPU_2T01 | CPU DPRSTP L | 7 10 16 23 58 |
| CPU_GTLREF | CPU_55S | CPU_GTLREF | CPU GTLREF | 10 |
| CPU_COMP | CPU_55S | CPU_COMP | CPU COMP<3> | 10 |
| CPU_COMP | CPU_27P4S | CPU_COMP | CPU COMP<2> | 10 |
| CPU_COMP | CPU_55S | CPU_COMP | CPU COMP<1> | 10 |
| CPU_COMP | CPU_27P4S | CPU_COMP | CPU COMP<0> | 10 |
| XDP_TDI | CPU_55S | CPU_ITP | XDP TDI | 10 13 |
| XDP_TDO | CPU_55S | CPU_ITP | XDP TDO | 10 13 |
| XDP_TMS | CPU_55S | CPU_ITP | XDP TMS | 10 13 |
| XDP_TCK | CPU_55S | CPU_ITP | XDP TCK | 10 13 |
| XDP_TEST_L | CPU_55S | CPU_ITP | XDP TRST L | 10 13 |
| XDP_BPM_L | CPU_55S | CPU_ITP | XDP BPM L<4..0> | 10 13 |
| XDP_BPM_L5 | CPU_55S | CPU_ITP | XDP BPM L<5> | 10 13 |
| CLK_FSB_100D | CLK_FSB | CLK_FSB | XDP CLK P | 13 30 84 |
| CLK_FSB_100D | CLK_FSB | CLK_FSB | XDP CLK N | 13 30 84 |
| (FSB_CPURST_L) | CPU_55S | CPU_ITP | XDP CPURST L | 13 |
| CPU_VID<6..0> | CPU_55S | CPU_2T01 | CPU VID<6..0> | 11 12 |
| CPU_VCCSENSE | CPU_27P4S | CPU_VCCSENSE | CPU VCCSENSE P | 7 12 58 |
| CPU_VCCSENSE | CPU_27P4S | CPU_VCCSENSE | CPU VCCSENSE N | 11 58 |
| CPU_VCCSENSE | CPU_27P4S | CPU_VCCSENSE | IMVP6 VSEN P | 58 |
| CPU_VCCSENSE | CPU_27P4S | CPU_VCCSENSE | IMVP6 VSEN N | 58 |

CPU/FSB Constraints

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| NONE | 100 | 109 |

PCI-Express / DMI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| DMI_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCIE | * | 20 MIL | ? |
| DMI | * | 20 MIL | ? |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| LVDS_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| CRT_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CRT_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| LVDS | * | 20 MIL | ? |
| CRT | * | 25 MIL | ? |
| CRT_2CRT | * | 20 MIL | ? |
| CRT_SYNC | * | 25 MIL | ? |
| CRT_SYNC2SYNC | * | 20 MIL | ? |
| TVDAC | * | 25 MIL | ? |
| TVDAC_2TVDAC | * | 20 MIL | ? |

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CRT | CRT | * | CRT_2CRT |
| CRT_SYNC | CRT_SYNC | * | CRT_SYNC2SYNC |
| TVDAC | TVDAC | * | TVDAC_2TVDAC |

LVDS signals are 100-ohm +/- 20% differential impedance.
 CRT & TVDAC signal single-ended impedance varies by location:
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.
 - 50-ohm +/- 15% from first to second termination resistor.
 - 55-ohm +/- 15% from second termination resistor to connector.
 CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | |
|---------------------------|-----------|----------|---------------------------|
| | PHYSICAL | SPACING | |
| PEG_R2D | PCIE_100D | PCIE | PEG R2D P<15..0> 66 |
| | PCIE_100D | PCIE | PEG R2D N<15..0> 66 |
| | PCIE_100D | PCIE | PEG R2D C P<15..0> 15 66 |
| | PCIE_100D | PCIE | PEG R2D C N<15..0> 15 66 |
| PEG_D2R | PCIE_100D | PCIE | PEG D2R P<15..0> 15 66 |
| | PCIE_100D | PCIE | PEG D2R N<15..0> 15 66 |
| | PCIE_100D | PCIE | PEG D2R C P<15..0> 66 |
| | PCIE_100D | PCIE | PEG D2R C N<15..0> 66 |
| DMI_N2S | DMI_100D | DMI | DMI N2S P<3..0> 16 24 |
| | DMI_100D | DMI | DMI N2S N<3..0> 16 24 |
| DMI_S2N | DMI_100D | DMI | DMI S2N P<3..0> 16 24 |
| | DMI_100D | DMI | DMI S2N N<3..0> 16 24 |
| LVDS_A_CLK | LVDS_100D | LVDS | LVDS A CLK P 15 77 |
| LVDS_A_CLK | LVDS_100D | LVDS | LVDS A CLK N 15 77 |
| LVDS_A_DATA | LVDS_100D | LVDS | LVDS A DATA P<2..0> 15 77 |
| LVDS_A_DATA | LVDS_100D | LVDS | LVDS A DATA N<2..0> 15 77 |
| LVDS_A_DATA3 | LVDS_100D | LVDS | LVDS A DATA P<3> 15 77 |
| LVDS_A_DATA3 | LVDS_100D | LVDS | LVDS A DATA N<3> 15 77 |
| LVDS_B_CLK | LVDS_100D | LVDS | LVDS B CLK P 15 77 |
| LVDS_B_CLK | LVDS_100D | LVDS | LVDS B CLK N 15 77 |
| LVDS_B_DATA | LVDS_100D | LVDS | LVDS B DATA P<2..0> 15 77 |
| LVDS_B_DATA | LVDS_100D | LVDS | LVDS B DATA N<2..0> 15 77 |
| LVDS_B_DATA3 | LVDS_100D | LVDS | LVDS B DATA P<3> 15 77 |
| LVDS_B_DATA3 | LVDS_100D | LVDS | LVDS B DATA N<3> 15 77 |
| LVDS_IBG | | LVDS | LVDS IBG 15 22 |
| CRT_TVO_IREF | | CRT | CRT TVO IREF |
| CRT_RED | CRT_50S | CRT | CRT RED |
| CRT_GREEN | CRT_50S | CRT | CRT GREEN |
| CRT_BLUE | CRT_50S | CRT | CRT BLUE |
| CRT_SYNC | CRT_55S | CRT_SYNC | CRT HSYNC R |
| CRT_SYNC | CRT_55S | CRT_SYNC | CRT VSYNC R |
| TV_A_DAC | CRT_50S | TVDAC | TV A DAC |
| TV_B_DAC | CRT_50S | TVDAC | TV B DAC |
| TV_C_DAC | CRT_50S | TVDAC | TV C DAC |

NB Constraints

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SIZE D DRAWING NUMBER 051-7435 REV. A

SCALE NONE SHEET 101 OF 109

DDR2 Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =STANDARD | =STANDARD |
| MEM_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| MEM_70D | * | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF |
| MEM_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MEM_CLK2MEM | * | =4:1_SPACING | ? |
| MEM_CTRL2CTRL | * | =2:1_SPACING | ? |
| MEM_CTRL2MEM | * | =3:1_SPACING | ? |
| MEM_CMD2CMD | * | =1.5:1_SPACING | ? |
| MEM_CMD2MEM | * | =3:1_SPACING | ? |
| MEM_DATA2DATA | * | =1.5:1_SPACING | ? |
| MEM_DATA2MEM | * | =3:1_SPACING | ? |
| MEM_DQS2MEM | * | =3:1_SPACING | ? |
| MEM_2OTHER | * | 25 MIL | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK | MEM_CLK | * | MEM_CLK2MEM |
| MEM_CLK | MEM_CTRL | * | MEM_CLK2MEM |
| MEM_CLK | MEM_CMD | * | MEM_CLK2MEM |
| MEM_CLK | MEM_DATA | * | MEM_CLK2MEM |
| MEM_CLK | MEM_DQS | * | MEM_CLK2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CMD | MEM_CLK | * | MEM_CMD2MEM |
| MEM_CMD | MEM_CTRL | * | MEM_CMD2MEM |
| MEM_CMD | MEM_CMD | * | MEM_CMD2CMD |
| MEM_CMD | MEM_DATA | * | MEM_CMD2MEM |
| MEM_CMD | MEM_DQS | * | MEM_CMD2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CTRL | MEM_CLK | * | MEM_CTRL2MEM |
| MEM_CTRL | MEM_CTRL | * | MEM_CTRL2CTRL |
| MEM_CTRL | MEM_CMD | * | MEM_CTRL2MEM |
| MEM_CTRL | MEM_DATA | * | MEM_CTRL2MEM |
| MEM_CTRL | MEM_DQS | * | MEM_CTRL2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DATA | MEM_CLK | * | MEM_DATA2MEM |
| MEM_DATA | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DATA | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DATA | MEM_DATA | * | MEM_DATA2DATA |
| MEM_DATA | MEM_DQS | * | MEM_DATA2MEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK | * | * | MEM_2OTHER |
| MEM_CTRL | * | * | MEM_2OTHER |
| MEM_CMD | * | * | MEM_2OTHER |
| MEM_DATA | * | * | MEM_2OTHER |
| MEM_DQS | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQS | MEM_CLK | * | MEM_DQS2MEM |
| MEM_DQS | MEM_CTRL | * | MEM_DQS2MEM |
| MEM_DQS | MEM_CMD | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DATA | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQS | * | MEM_DQS2MEM |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Need to support MEM_*-style wildcards!

Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING | NET_TYPE |
|---------------------------|----------|----------|------------------|
| MEM_A_CLK | MEM_70D | MEM_CLK | MEM CLK P<2..0> |
| MEM_A_CLK | MEM_70D | MEM_CLK | MEM CLK N<2..0> |
| MEM_A_CNTRL | MEM_45S | MEM_CTRL | MEM CKE<1..0> |
| MEM_A_CNTRL | MEM_45S | MEM_CTRL | MEM CS L<1..0> |
| MEM_A_CNTRL | MEM_45S | MEM_CTRL | MEM ODT<1..0> |
| MEM_A_CMD | MEM_55S | MEM_CMD | MEM A A<14..0> |
| MEM_A_CMD | MEM_55S | MEM_CMD | MEM A BS<2..0> |
| MEM_A_CMD | MEM_55S | MEM_CMD | MEM A RAS L |
| MEM_A_CMD | MEM_55S | MEM_CMD | MEM A CAS L |
| MEM_A_CMD | MEM_55S | MEM_CMD | MEM A WE L |
| MEM_A_DQ_BYTE0 | MEM_55S | MEM_DATA | MEM A DQ<7..0> |
| MEM_A_DQ_BYTE1 | MEM_55S | MEM_DATA | MEM A DO<15..8> |
| MEM_A_DQ_BYTE2 | MEM_55S | MEM_DATA | MEM A DO<23..16> |
| MEM_A_DQ_BYTE3 | MEM_55S | MEM_DATA | MEM A DO<31..24> |
| MEM_A_DQ_BYTE4 | MEM_55S | MEM_DATA | MEM A DO<39..32> |
| MEM_A_DQ_BYTE5 | MEM_55S | MEM_DATA | MEM A DO<47..40> |
| MEM_A_DQ_BYTE6 | MEM_55S | MEM_DATA | MEM A DO<55..48> |
| MEM_A_DQ_BYTE7 | MEM_55S | MEM_DATA | MEM A DO<63..56> |
| MEM_A_DM0 | MEM_55S | MEM_DATA | MEM A DM<0> |
| MEM_A_DM1 | MEM_55S | MEM_DATA | MEM A DM<1> |
| MEM_A_DM2 | MEM_55S | MEM_DATA | MEM A DM<2> |
| MEM_A_DM3 | MEM_55S | MEM_DATA | MEM A DM<3> |
| MEM_A_DM4 | MEM_55S | MEM_DATA | MEM A DM<4> |
| MEM_A_DM5 | MEM_55S | MEM_DATA | MEM A DM<5> |
| MEM_A_DM6 | MEM_55S | MEM_DATA | MEM A DM<6> |
| MEM_A_DM7 | MEM_55S | MEM_DATA | MEM A DM<7> |
| MEM_A_DQS0 | MEM_85D | MEM_DQS | MEM A DQS P<0> |
| MEM_A_DQS0 | MEM_85D | MEM_DQS | MEM A DQS N<0> |
| MEM_A_DQS1 | MEM_85D | MEM_DQS | MEM A DQS P<1> |
| MEM_A_DQS1 | MEM_85D | MEM_DQS | MEM A DQS N<1> |
| MEM_A_DQS2 | MEM_85D | MEM_DQS | MEM A DQS P<2> |
| MEM_A_DQS2 | MEM_85D | MEM_DQS | MEM A DQS N<2> |
| MEM_A_DQS3 | MEM_85D | MEM_DQS | MEM A DQS P<3> |
| MEM_A_DQS3 | MEM_85D | MEM_DQS | MEM A DQS N<3> |
| MEM_A_DQS4 | MEM_85D | MEM_DQS | MEM A DQS P<4> |
| MEM_A_DQS4 | MEM_85D | MEM_DQS | MEM A DQS N<4> |
| MEM_A_DQS5 | MEM_85D | MEM_DQS | MEM A DQS P<5> |
| MEM_A_DQS5 | MEM_85D | MEM_DQS | MEM A DQS N<5> |
| MEM_A_DQS6 | MEM_85D | MEM_DQS | MEM A DQS P<6> |
| MEM_A_DQS6 | MEM_85D | MEM_DQS | MEM A DQS N<6> |
| MEM_A_DQS7 | MEM_85D | MEM_DQS | MEM A DQS P<7> |
| MEM_A_DQS7 | MEM_85D | MEM_DQS | MEM A DQS N<7> |
| MEM_B_CLK | MEM_70D | MEM_CLK | MEM CLK P<5..3> |
| MEM_B_CLK | MEM_70D | MEM_CLK | MEM CLK N<5..3> |
| MEM_B_CNTRL | MEM_45S | MEM_CTRL | MEM CKE<4..3> |
| MEM_B_CNTRL | MEM_45S | MEM_CTRL | MEM CS L<3..2> |
| MEM_B_CNTRL | MEM_45S | MEM_CTRL | MEM ODT<3..2> |
| MEM_B_CMD | MEM_55S | MEM_CMD | MEM B A<14..0> |
| MEM_B_CMD | MEM_55S | MEM_CMD | MEM B BS<2..0> |
| MEM_B_CMD | MEM_55S | MEM_CMD | MEM B RAS L |
| MEM_B_CMD | MEM_55S | MEM_CMD | MEM B CAS L |
| MEM_B_CMD | MEM_55S | MEM_CMD | MEM B WE L |
| MEM_B_DQ_BYTE0 | MEM_55S | MEM_DATA | MEM B DQ<7..0> |
| MEM_B_DQ_BYTE1 | MEM_55S | MEM_DATA | MEM B DO<15..8> |
| MEM_B_DQ_BYTE2 | MEM_55S | MEM_DATA | MEM B DO<23..16> |
| MEM_B_DQ_BYTE3 | MEM_55S | MEM_DATA | MEM B DO<31..24> |
| MEM_B_DQ_BYTE4 | MEM_55S | MEM_DATA | MEM B DO<39..32> |
| MEM_B_DQ_BYTE5 | MEM_55S | MEM_DATA | MEM B DO<47..40> |
| MEM_B_DQ_BYTE6 | MEM_55S | MEM_DATA | MEM B DO<55..48> |
| MEM_B_DQ_BYTE7 | MEM_55S | MEM_DATA | MEM B DO<63..56> |
| MEM_B_DM0 | MEM_55S | MEM_DATA | MEM B DM<0> |
| MEM_B_DM1 | MEM_55S | MEM_DATA | MEM B DM<1> |
| MEM_B_DM2 | MEM_55S | MEM_DATA | MEM B DM<2> |
| MEM_B_DM3 | MEM_55S | MEM_DATA | MEM B DM<3> |
| MEM_B_DM4 | MEM_55S | MEM_DATA | MEM B DM<4> |
| MEM_B_DM5 | MEM_55S | MEM_DATA | MEM B DM<5> |
| MEM_B_DM6 | MEM_55S | MEM_DATA | MEM B DM<6> |
| MEM_B_DM7 | MEM_55S | MEM_DATA | MEM B DM<7> |
| MEM_B_DQS0 | MEM_85D | MEM_DQS | MEM B DQS P<0> |
| MEM_B_DQS0 | MEM_85D | MEM_DQS | MEM B DQS N<0> |
| MEM_B_DQS1 | MEM_85D | MEM_DQS | MEM B DQS P<1> |
| MEM_B_DQS1 | MEM_85D | MEM_DQS | MEM B DQS N<1> |
| MEM_B_DQS2 | MEM_85D | MEM_DQS | MEM B DQS P<2> |
| MEM_B_DQS2 | MEM_85D | MEM_DQS | MEM B DQS N<2> |
| MEM_B_DQS3 | MEM_85D | MEM_DQS | MEM B DQS P<3> |
| MEM_B_DQS3 | MEM_85D | MEM_DQS | MEM B DQS N<3> |
| MEM_B_DQS4 | MEM_85D | MEM_DQS | MEM B DQS P<4> |
| MEM_B_DQS4 | MEM_85D | MEM_DQS | MEM B DQS N<4> |
| MEM_B_DQS5 | MEM_85D | MEM_DQS | MEM B DQS P<5> |
| MEM_B_DQS5 | MEM_85D | MEM_DQS | MEM B DQS N<5> |
| MEM_B_DQS6 | MEM_85D | MEM_DQS | MEM B DQS P<6> |
| MEM_B_DQS6 | MEM_85D | MEM_DQS | MEM B DQS N<6> |
| MEM_B_DQS7 | MEM_85D | MEM_DQS | MEM B DQS P<7> |
| MEM_B_DQS7 | MEM_85D | MEM_DQS | MEM B DQS N<7> |

Memory Constraints
 SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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DRAWING NUMBER: 051-7435
 SHEET: 102 OF 109

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Disk Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| IDE_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| SATA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| SATA_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| IDE | * | =1.8:1_SPACING | ? |
| SATA | * | 20 MIL | ? |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| HDA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| HDA | * | =1.8:1_SPACING | ? |

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| USB_60S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| USB_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| USB | * | 20 MIL | ? |
| USB_2CLK | * | 25 MIL | ? |

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB | * | =3:1_SPACING | ? |
| SPI | * | =1.8:1_SPACING | ? |

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | |
|---------------------------|-----------|---------|-------------------------|
| | PHYSICAL | SPACING | |
| IDE_PDD | IDE_55S | IDE | IDE_PDD<15..0> 23 42 |
| IDE_PDA | IDE_55S | IDE | IDE_PDA<2..0> 23 42 |
| IDE_PDCS | IDE_55S | IDE | IDE_PDCS1 L 23 42 |
| IDE_PDCS | IDE_55S | IDE | IDE_PDCS3 L 23 42 |
| IDE_PDIOW | IDE_55S | IDE | IDE_PDIOW L 23 42 |
| IDE_PDIOR | IDE_55S | IDE | IDE_PDIOR L 23 42 |
| IDE_PDDACK | IDE_55S | IDE | IDE_PDDACK L 23 42 |
| IDE_PDDREO | IDE_55S | IDE | IDE_PDDREO 23 42 |
| IDE_PDIORDY | IDE_55S | IDE | IDE_PDIORDY 23 42 |
| IDE_IRQ14 | IDE_55S | IDE | IDE_IRQ14 23 42 |
| IDE_RST_L | IDE_55S | IDE | ODD_RST_5VTOL L 24 42 |
| SATA_A_R2D | SATA_100D | SATA | SATA_A_R2D C P 23 78 |
| SATA_100D | SATA | SATA | SATA_A_R2D C N 23 78 |
| SATA_100D | SATA | SATA | SATA_A_R2D P 78 |
| SATA_100D | SATA | SATA | SATA_A_R2D N 78 |
| SATA_A_D2R | SATA_100D | SATA | SATA_A_D2R P 23 78 |
| SATA_100D | SATA | SATA | SATA_A_D2R N 23 78 |
| SATA_100D | SATA | SATA | SATA_A_D2R C P 78 |
| SATA_100D | SATA | SATA | SATA_A_D2R C N 78 |
| SATA_B_R2D | SATA_100D | SATA | SATA_B_R2D C P 23 42 |
| SATA_100D | SATA | SATA | SATA_B_R2D C N 23 42 |
| SATA_100D | SATA | SATA | SATA_B_R2D P 23 42 |
| SATA_100D | SATA | SATA | SATA_B_R2D N 23 42 |
| SATA_B_D2R | SATA_100D | SATA | SATA_B_D2R P 23 42 |
| SATA_100D | SATA | SATA | SATA_B_D2R N 23 42 |
| SATA_100D | SATA | SATA | SATA_B_D2R C P 23 42 |
| SATA_100D | SATA | SATA | SATA_B_D2R C N 23 42 |
| SATA_C_R2D | SATA_100D | SATA | SATA_C_R2D C P 23 42 |
| SATA_100D | SATA | SATA | SATA_C_R2D C N 23 42 |
| SATA_100D | SATA | SATA | SATA_C_R2D P 23 42 |
| SATA_100D | SATA | SATA | SATA_C_R2D N 23 42 |
| SATA_C_D2R | SATA_100D | SATA | SATA_C_D2R P 23 42 |
| SATA_100D | SATA | SATA | SATA_C_D2R N 23 42 |
| SATA_100D | SATA | SATA | SATA_C_D2R C P 23 42 |
| SATA_100D | SATA | SATA | SATA_C_D2R C N 23 42 |
| SATA_RBIAS | SATA_55S | | SATA_RBIAS 42 |
| HDA_BIT_CLK | HDA_55S | HDA | HDA_BIT_CLK 23 34 |
| HDA_55S | HDA | HDA | HDA_BIT_CLK R 23 34 |
| HDA_SYNC | HDA_55S | HDA | HDA_SYNC 23 34 |
| HDA_55S | HDA | HDA | HDA_SYNC R 23 34 |
| HDA_RST_L | HDA_55S | HDA | HDA_RST_L 23 34 |
| HDA_55S | HDA | HDA | HDA_RST_L R 23 34 |
| HDA_SDIN0 | HDA_55S | HDA | HDA_SDIN0 23 34 |
| HDA_55S | HDA | HDA | HDA_SDIN0 CODEC 23 34 |
| HDA_SDOUT | HDA_55S | HDA | HDA_SDOUT 23 34 |
| HDA_55S | HDA | HDA | HDA_SDOUT R 23 34 |
| USB_EXT_A | USB_90D | USB | USB_EXT_A P 24 43 |
| USB_90D | USB | USB | USB_EXT_A N 24 43 |
| USB_90D | USB | USB | USB_EXT_A MUXED P 24 43 |
| USB_90D | USB | USB | USB_EXT_A MUXED N 24 43 |
| USB_MINI | USB_90D | USB | USB_MINI P 24 34 |
| USB_90D | USB | USB | USB_MINI N 24 34 |
| USB_EXTD | USB_90D | USB | USB_EXTD P 24 44 |
| USB_90D | USB | USB | USB_EXTD N 24 44 |
| USB_CAMERA | USB_90D | USB | USB_CAMERA P 7 24 44 |
| USB_90D | USB | USB | USB_CAMERA N 7 24 44 |
| USB_BT | USB_90D | USB | USB_BT P 24 78 |
| USB_90D | USB | USB | USB_BT N 24 78 |
| USB_TPAD | USB_90D | USB | USB_TPAD P 24 78 |
| USB_90D | USB | USB | USB_TPAD N 24 78 |
| USB_IR | USB_90D | USB | USB_IR P 24 78 |
| USB_90D | USB | USB | USB_IR N 24 78 |
| USB_EXTB | USB_90D | USB | USB_EXTB P 24 34 |
| USB_90D | USB | USB | USB_EXTB N 24 34 |
| USB_EXCARD | USB_90D | USB | USB_EXCARD P 24 34 |
| USB_90D | USB | USB | USB_EXCARD N 24 34 |
| USB_EXTC | USB_90D | USB | USB_EXTC P 9 24 |
| USB_90D | USB | USB | USB_EXTC N 9 24 |
| USB_RBIAS | USB_60S | | USB_RBIAS 24 |
| SMB_SB_SCL | SMB_55S | SMB | SMB_CLK 25 48 |
| SMB_SB_SDA | SMB_55S | SMB | SMB_DATA 25 48 |
| SMB_SB_ME_SCL | SMB_55S | SMB | SMB_ME_CLK 25 48 |
| SMB_SB_ME_SDA | SMB_55S | SMB | SMB_ME_DATA 25 48 |
| SPI_SCLK | SPI_55S | SPI | SPI_SCLK R 24 55 |
| SPI_55S | SPI | SPI | SPI_SCLK 55 |
| SPI_55S | SPI | SPI | SPI_A_SCLK R 55 |
| SPI_55S | SPI | SPI | SPI_B_SCLK R 55 |
| SPI_SI | SPI_55S | SPI | SPI_SI R 24 55 |
| SPI_55S | SPI | SPI | SPI_SI 55 |
| SPI_55S | SPI | SPI | SPI_A_SI R 55 |
| SPI_55S | SPI | SPI | SPI_B_SI R 55 |
| SPI_SO | SPI_55S | SPI | SPI_SO 24 55 |
| SPI_55S | SPI | SPI | SPI_A_SO R 55 |
| SPI_55S | SPI | SPI | SPI_B_SO R 55 |
| SPI_55S | SPI | SPI | SPI_B_SO R 55 |
| SPI_CE_L0 | SPI_55S | SPI | SPI_CE_R_L<0> 24 55 |
| SPI_55S | SPI | SPI | SPI_CE_L<0> 55 |
| SPI_CE_L1 | SPI_55S | SPI | SPI_CE_R_L<1> 24 55 |
| SPI_55S | SPI | SPI | SPI_CE_L<1> 55 |

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7435 | A |
| SCALE | SHT | OF | REV. |
| NONE | 103 | 109 | |

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PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCI | * | =2:1_SPACING | ? |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLINK_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLINK_12MIL | * | =STANDARD | 12 MILS | 5 MILS | 300 MILS | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLINK | * | =1.8:1_SPACING | ? |
| CLINK_VREF | * | 12 MILS | ? |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| ENET_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| ENET_MDI | * | 25 MILS | ? |

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|-------------|------------|---------------------|-------|
| | PHYSICAL | SPACING | | |
| PCI_AD | PCI_55S | PCI | PCI AD<18..0> | 24 38 |
| PCI_AD19 | PCI_55S | PCI | PCI AD<19> | 24 38 |
| PCI_AD20 | PCI_55S | PCI | PCI AD<20> | 24 38 |
| PCI_AD | PCI_55S | PCI | PCI AD<31..21> | 24 38 |
| PCI_AD | PCI_55S | PCI | PCI PAR | 24 38 |
| PCI_C_BE_L | PCI_55S | PCI | PCI C BE L<3..0> | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI IRDY_L | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI DEVSEL_L | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI PERR_L | 24 38 |
| PCI_LOCK_L | PCI_55S | PCI | PCI LOCK_L | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI SERR_L | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI STOP_L | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI TRDY_L | 24 38 |
| PCI_CNTRL | PCI_55S | PCI | PCI FRAME_L | 24 38 |
| PCI_FW_REQ_L | PCI_55S | PCI | PCI FW REQ_L | 24 38 |
| PCI_FW_GNT_L | PCI_55S | PCI | PCI FW GNT_L | 24 38 |
| PCI_REQ1_L | PCI_55S | PCI | PCI REQ1_L | 24 38 |
| PCI_GNT1_L | PCI_55S | PCI | PCI GNT1_L | 24 38 |
| PCI_REQ2_L | PCI_55S | PCI | PCI REQ2_L | 24 38 |
| PCI_GNT2_L | PCI_55S | PCI | PCI GNT2_L | 24 38 |
| INT_PIRQA_L | PCI_55S | PCI | INT PIRQA_L | 24 38 |
| INT_PIRQB_L | PCI_55S | PCI | INT PIRQB_L | 24 38 |
| INT_PIRQC_L | PCI_55S | PCI | INT PIRQC_L | 24 38 |
| INT_PIRQD_L | PCI_55S | PCI | INT PIRQD_L | 24 38 |
| INT_PIRQE_L | PCI_55S | PCI | INT PIRQE_L | 24 38 |
| INT_PIRQF_L | PCI_55S | PCI | INT PIRQF_L | 24 38 |
| PCIE_A_R2D | PCIE_100D | PCIE | PCIE A R2D C P | 24 34 |
| PCIE_A_R2D | PCIE_100D | PCIE | PCIE A R2D C N | 24 34 |
| PCIE_A_D2R | PCIE_100D | PCIE | PCIE A D2R P | 24 34 |
| PCIE_A_D2R | PCIE_100D | PCIE | PCIE A D2R N | 24 34 |
| PCIE_B_R2D | PCIE_100D | PCIE | PCIE B R2D C P | 24 34 |
| PCIE_B_R2D | PCIE_100D | PCIE | PCIE B R2D C N | 24 34 |
| PCIE_B_D2R | PCIE_100D | PCIE | PCIE B D2R P | 24 34 |
| PCIE_B_D2R | PCIE_100D | PCIE | PCIE B D2R N | 24 34 |
| PCIE_EXCARD_R2D | PCIE_100D | PCIE | PCIE EXCARD R2D C P | 24 34 |
| PCIE_EXCARD_R2D | PCIE_100D | PCIE | PCIE EXCARD R2D C N | 24 34 |
| PCIE_EXCARD_D2R | PCIE_100D | PCIE | PCIE EXCARD D2R P | 24 34 |
| PCIE_EXCARD_D2R | PCIE_100D | PCIE | PCIE EXCARD D2R N | 24 34 |
| PCIE_FW_R2D | PCIE_100D | PCIE | PCIE FW R2D C P | 24 34 |
| PCIE_FW_R2D | PCIE_100D | PCIE | PCIE FW R2D C N | 24 34 |
| PCIE_FW_D2R | PCIE_100D | PCIE | PCIE FW D2R P | 24 34 |
| PCIE_FW_D2R | PCIE_100D | PCIE | PCIE FW D2R N | 24 34 |
| PCIE_MINI_R2D | PCIE_100D | PCIE | PCIE MINI R2D C P | 24 34 |
| PCIE_MINI_R2D | PCIE_100D | PCIE | PCIE MINI R2D C N | 24 34 |
| PCIE_MINI_D2R | PCIE_100D | PCIE | PCIE MINI D2R P | 24 34 |
| PCIE_MINI_D2R | PCIE_100D | PCIE | PCIE MINI D2R N | 24 34 |
| GLAN_COMP | | | GLAN COMP | 23 |
| CLINK_NB | CLINK_55S | CLINK | CLINK NB CLK | 16 25 |
| CLINK_NB | CLINK_55S | CLINK | CLINK NB DATA | 16 25 |
| CLINK_NB_RESET_L | CLINK_55S | CLINK | CLINK NB RESET_L | 16 25 |
| CLINK_WLAN | CLINK_55S | CLINK | CLINK WLAN CLK | 16 25 |
| CLINK_WLAN | CLINK_55S | CLINK | CLINK WLAN DATA | 16 25 |
| CLINK_WLAN_RESET_L | CLINK_55S | CLINK | CLINK WLAN RESET_L | 16 25 |
| NB_CLINK_VREF | CLINK_12MIL | CLINK_VREF | NB CLINK VREF | 16 25 |
| SB_CLINK_VREF0 | CLINK_12MIL | CLINK_VREF | SB CLINK VREF0 | 25 |
| SB_CLINK_VREF1 | CLINK_12MIL | CLINK_VREF | SB CLINK VREF1 | 25 |
| PCIE_ENET_R2D | PCIE_100D | PCIE | PCIE ENET R2D C P | 24 35 |
| PCIE_ENET_R2D | PCIE_100D | PCIE | PCIE ENET R2D C N | 24 35 |
| PCIE_ENET_R2D | PCIE_100D | PCIE | PCIE ENET R2D P | 24 35 |
| PCIE_ENET_R2D | PCIE_100D | PCIE | PCIE ENET R2D N | 24 35 |
| PCIE_ENET_D2R | PCIE_100D | PCIE | PCIE ENET D2R P | 24 35 |
| PCIE_ENET_D2R | PCIE_100D | PCIE | PCIE ENET D2R N | 24 35 |
| PCIE_ENET_D2R | PCIE_100D | PCIE | PCIE ENET D2R C P | 24 35 |
| PCIE_ENET_D2R | PCIE_100D | PCIE | PCIE ENET D2R C N | 24 35 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI P<0> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI N<0> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI P<1> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI N<1> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI P<2> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI N<2> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI P<3> | 35 37 |
| ENET_MDI | ENET_100D | ENET_MDI | ENET MDI N<3> | 35 37 |

SB Constraints (2 of 2)

SYNC_MASTER=T9_NAME SYNC_DATE=01/17/2007

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| | D | 051-7435 | A |
| SCALE | SHT | OF | |
| NONE | 104 | 109 | |

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Clock Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_FSB_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| CLK_PCIE_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| CLK_MED_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_SLOW_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_FSB | * | 25 MIL | ? |
| CLK_PCIE | * | 20 MIL | ? |
| CLK_MED | * | 20 MIL | ? |
| CLK_SLOW | * | 10 MIL | ? |

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|---------------|----------|--------------------------------|----------|
| | PHYSICAL | SPACING | | |
| CK505_CPU0 | CLK_FSB_100D | CLK_FSB | CK505_CPU0 P | 29 30 |
| CK505_CPU1 | CLK_FSB_100D | CLK_FSB | CK505_CPU0 N | 29 30 |
| CK505_NB | CLK_FSB_100D | CLK_FSB | CK505_CPU1 P | 29 30 |
| CK505_NB | CLK_FSB_100D | CLK_FSB | CK505_CPU1 N | 29 30 |
| CK505_ITP | CLK_FSB_100D | CLK_FSB | CK505_CPU2 ITP_SRC10 P | 29 30 |
| CK505_ITP | CLK_FSB_100D | CLK_FSB | CK505_CPU2 ITP_SRC10 N | 29 30 |
| CK505_PCIE0 | CLK_MED_55S | CLK_MED | CK505_PCIE0 CLK ITPEN | 29 30 |
| CK505_PCIE1 | CLK_MED_55S | CLK_MED | CK505_PCIE1 CLK | 29 30 |
| CK505_PCIE1 | CLK_MED_55S | CLK_MED | CK505_PCIE1 CLK | 29 30 |
| CK505_PCIE2 | CLK_MED_55S | CLK_MED | CK505_PCIE2 CLK | 29 30 |
| CK505_PCIE3 | CLK_MED_55S | CLK_MED | CK505_PCIE3 CLK | 29 30 |
| CK505_PCIE4 | CLK_MED_55S | CLK_MED | CK505_PCIE4 CLK | 29 30 |
| CK505_PCIE5 | CLK_MED_55S | CLK_MED | CK505_PCIE5 CLK FCTSEL | 29 30 |
| (CPU_BSEL0) | CLK_MED_55S | CLK_MED | CK505_48M_FSA | 29 30 |
| (CPU_BSEL2) | CLK_MED_55S | CLK_MED | CK505_REF0_FSC | 29 30 |
| CK505_DOT96 | CLK_PCIE_100D | CLK_PCIE | CK505_DOT96_27M P | 29 30 |
| CK505_DOT96 | CLK_PCIE_100D | CLK_PCIE | CK505_DOT96_27M N | 29 30 |
| CK505_LVDS | CLK_PCIE_100D | CLK_PCIE | CK505_LVDS P | 29 30 |
| CK505_LVDS | CLK_PCIE_100D | CLK_PCIE | CK505_LVDS N | 29 30 |
| CK505_SRC1 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC1 P | 29 30 |
| CK505_SRC1 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC1 N | 29 30 |
| CK505_SRC2 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC2 P | 29 30 |
| CK505_SRC2 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC2 N | 29 30 |
| CK505_SRC3 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC3 P | 29 30 |
| CK505_SRC3 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC3 N | 29 30 |
| CK505_SRC4 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC4 P | 29 30 |
| CK505_SRC4 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC4 N | 29 30 |
| CK505_SRC5 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC5 P | 29 30 |
| CK505_SRC5 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC5 N | 29 30 |
| CK505_SRC6 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC6 P | 29 30 |
| CK505_SRC6 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC6 N | 29 30 |
| CK505_SRC7 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC7 P | 29 30 |
| CK505_SRC7 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC7 N | 29 30 |
| CK505_SRC8 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC8 P | 29 30 |
| CK505_SRC8 | CLK_PCIE_100D | CLK_PCIE | CK505_SRC8 N | 29 30 |
| (CK505_CPU) | CLK_FSB_100D | CLK_FSB | FSB_CLK_CPU P | 10 30 |
| (CK505_CPU) | CLK_FSB_100D | CLK_FSB | FSB_CLK_CPU N | 10 30 |
| (CK505_NB) | CLK_FSB_100D | CLK_FSB | FSB_CLK_NB P | 7 14 30 |
| (CK505_NB) | CLK_FSB_100D | CLK_FSB | FSB_CLK_NB N | 7 14 30 |
| (CK505_ITP) | CLK_FSB_100D | CLK_FSB | XDP_CLK P | 13 30 79 |
| (CK505_ITP) | CLK_FSB_100D | CLK_FSB | XDP_CLK N | 13 30 79 |
| (CK505_PCIE0) | CLK_MED_55S | CLK_MED | PCI_CLK33M_LPCPLUS | 7 30 47 |
| (CK505_PCIE1) | CLK_MED_55S | CLK_MED | PCI_CLK33M_SB | 24 30 |
| (CK505_PCIE1) | CLK_MED_55S | CLK_MED | PCI_CLK33M_SB | 24 30 |
| (CK505_PCIE2) | CLK_MED_55S | CLK_MED | PCI_CLK33M_TPM | 30 38 |
| (CK505_PCIE3) | CLK_MED_55S | CLK_MED | PCI_CLK33M_SMC | 30 45 |
| (CPU_BSEL0) | CLK_MED_55S | CLK_MED | CK505_PCI4 is project-specific | |
| (CPU_BSEL2) | CLK_MED_55S | CLK_MED | CK505_PCI5 is project-specific | |
| (CPU_BSEL0) | CLK_MED_55S | CLK_MED | SB_CLK48M_USBCTRL | 25 30 |
| (CPU_BSEL2) | CLK_MED_55S | CLK_MED | SB_CLK14P3M_TIMER | 25 30 |
| (CPU_BSEL0) | CLK_MED_55S | CLK_MED | CK505_FSA | 30 |
| (CPU_BSEL2) | CLK_MED_55S | CLK_MED | CK505_FSC | 30 |
| (CK505_DOT96) | CLK_PCIE_100D | CLK_PCIE | NB_CLK96M_DOT P | 7 |
| (CK505_DOT96) | CLK_PCIE_100D | CLK_PCIE | NB_CLK96M_DOT N | 7 |
| (CK505_LVDS) | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_DPLLSS P | 7 22 30 |
| (CK505_LVDS) | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_DPLLSS N | 7 22 30 |
| (CK505_SRC1) | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M P | 9 |
| (CK505_SRC1) | CLK_PCIE_100D | CLK_PCIE | PEG_CLK100M N | 9 |
| (CK505_SRC2) | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_DMI P | 24 30 |
| (CK505_SRC2) | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_DMI N | 24 30 |
| (CK505_SRC3) | CLK_PCIE_100D | CLK_PCIE | PCI_CLK100M_EXCARD P | 30 34 |
| (CK505_SRC3) | CLK_PCIE_100D | CLK_PCIE | PCI_CLK100M_EXCARD N | 30 34 |
| (CK505_SRC4) | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_SATA P | 23 30 |
| (CK505_SRC4) | CLK_PCIE_100D | CLK_PCIE | SB_CLK100M_SATA N | 23 30 |
| (CK505_SRC5) | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_PCIE P | 7 16 30 |
| (CK505_SRC5) | CLK_PCIE_100D | CLK_PCIE | NB_CLK100M_PCIE N | 7 16 30 |
| (CK505_SRC6) | CLK_PCIE_100D | CLK_PCIE | PCI_CLK100M_MINI P | 30 34 |
| (CK505_SRC6) | CLK_PCIE_100D | CLK_PCIE | PCI_CLK100M_MINI N | 30 34 |
| (CK505_SRC7) | CLK_PCIE_100D | CLK_PCIE | CK505_SRC7 is project-specific | |
| (CK505_SRC8) | CLK_PCIE_100D | CLK_PCIE | PCI_CLK100M_ENET P | 30 35 |
| (CK505_SRC8) | CLK_PCIE_100D | CLK_PCIE | PCI_CLK100M_ENET N | 30 35 |

SMC SMBus Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | | |
|---------------------------|----------|---------|--------------------|----|
| | PHYSICAL | SPACING | | |
| SMBUS_SMC_A_S3_SCL | SMB_55S | SMB | SMBUS_SMC_A_S3_SCL | 48 |
| SMBUS_SMC_A_S3_SDA | SMB_55S | SMB | SMBUS_SMC_A_S3_SDA | 48 |
| SMBUS_SMC_B_S0_SCL | SMB_55S | SMB | SMBUS_SMC_B_S0_SCL | 48 |
| SMBUS_SMC_B_S0_SDA | SMB_55S | SMB | SMBUS_SMC_B_S0_SDA | 48 |
| SMBUS_SMC_0_S0_SCL | SMB_55S | SMB | SMBUS_SMC_0_S0_SCL | 48 |
| SMBUS_SMC_0_S0_SDA | SMB_55S | SMB | SMBUS_SMC_0_S0_SDA | 48 |
| SMBUS_SMC_BSA_SCL | SMB_55S | SMB | SMBUS_SMC_BSA_SCL | 48 |
| SMBUS_SMC_BSA_SDA | SMB_55S | SMB | SMBUS_SMC_BSA_SDA | 48 |
| SMBUS_SMC_MGMT_SCL | SMB_55S | SMB | SMBUS_SMC_MGMT_SCL | 48 |
| SMBUS_SMC_MGMT_SDA | SMB_55S | SMB | SMBUS_SMC_MGMT_SDA | 48 |

Clock & SMC Constraints

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| SCALE | SHT | OF | |
| NONE | 105 | 109 | |

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FireWire Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FW_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| FW_110D | * | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FW | * | =2:1_SPACING | ? |
| FW_TP | * | =3:1_SPACING | ? |

FireWire Net Properties


| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | |
|---------------------------|-------------|---------|-----------------------|
| | PHYSICAL | SPACING | |
| EW_D_CTL | EW_55S | FW | FW LINK<7..0> |
| EW_D_CTL | EW_55S | FW | FW CTL<1..0> |
| EW_LCLK | CLK_MED_55S | CLK_MED | CLKFW LINK_LCLK |
| EW_PCLK | CLK_MED_55S | CLK_MED | CLKFW PHY_LCLK 38 39 |
| EW_PCLK | CLK_MED_55S | CLK_MED | CLKFW LINK_PCLK 38 39 |
| EW_PCLK | CLK_MED_55S | CLK_MED | CLKFW PHY_PCLK 38 39 |
| EW_LKON | EW_55S | FW | FW LKON |
| EW_LKON | EW_55S | FW | FW LKON R |
| EW_LPS | EW_55S | FW | FW LPS 38 39 |
| EW_LREQ | EW_55S | FW | FW LREQ 38 39 |
| EW_PINT | EW_55S | FW | FW PINT 38 39 |
| EWPHY_CLK98P304M_XI | CLK_MED_55S | CLK_MED | CLK98P304M FW_XI_R |
| EWPHY_CLK98P304M_XI | CLK_MED_55S | CLK_MED | CLK98P304M FW_XI |
| EW_0_TPA | EW_110D | EW_TP | FW_0 TPA_P 39 41 |
| EW_0_TPA | EW_110D | EW_TP | FW_0 TPA_N 39 41 |
| EW_0_TPB | EW_110D | EW_TP | FW_0 TPB_P 39 41 |
| EW_0_TPB | EW_110D | EW_TP | FW_0 TPB_N 39 41 |
| EW_1_TPA | EW_110D | EW_TP | FW_1 TPA_P 39 41 |
| EW_1_TPA | EW_110D | EW_TP | FW_1 TPA_N 39 41 |
| EW_1_TPB | EW_110D | EW_TP | FW_1 TPB_P 39 41 |
| EW_1_TPB | EW_110D | EW_TP | FW_1 TPB_N 39 41 |
| Port 2 Not Used | | | |

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| FireWire Constraints | | |
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| | D | 051-7435 | A |
| SCALE | SHT | OF | REV. |
| NONE | 106 | 109 | |

GDDR3 Frame Buffer Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| GDDR3_40R50SE | * | =50_OHM_SE | =40_OHM_SE | =50_OHM_SE | 12.7 MM | =STANDARD | =STANDARD |
| GDDR3_50SE | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| GDDR3_80D | * | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GDDR3_CLK | * | =2.5:1_SPACING | ? |
| GDDR3_CMD | * | =2.5:1_SPACING | ? |
| GDDR3_DATA | * | =2.5:1_SPACING | ? |
| GDDR3_DQS | * | =2.5:1_SPACING | ? |

Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| TMDS_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| VGA_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| VGA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| TMDS | * | 20 MIL | ? |
| VGA | * | 20 MIL | ? |
| VGA_SYNC | * | 20 MIL | ? |

GDDR3 FB A/B Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | PROPERTY | VALUE |
|---------------------------|---------------|------------|-----------------|-------|
| | PHYSICAL | SPACING | | |
| FB_A_CLK_P | GDDR3_80D | GDDR3_CLK | FB A CLK P<0> | 68 69 |
| FB_A_CLK_N | GDDR3_80D | GDDR3_CLK | FB A CLK N<0> | 68 69 |
| FB_B_CLK_P | GDDR3_80D | GDDR3_CLK | FB A CLK P<1> | 68 69 |
| FB_B_CLK_N | GDDR3_80D | GDDR3_CLK | FB A CLK N<1> | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A MA<1..0> | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A MA<11..6> | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A BA<2..0> | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A RAS L | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A CAS L | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A WE L | 68 69 |
| FB_AB_CMD_PD | GDDR3_40R50SE | GDDR3_CMD | FB A CKE | 68 69 |
| FB_AB_CMD | GDDR3_40R50SE | GDDR3_CMD | FB A CS0 L | 68 69 |
| FB_AB_CMD_PD | GDDR3_40R50SE | GDDR3_CMD | FB A DRAM RST | 68 69 |
| FB_A_CMD | GDDR3_50SE | GDDR3_CMD | FB A LMA<5..2> | 68 69 |
| FB_B_CMD | GDDR3_50SE | GDDR3_CMD | FB A UMA<5..2> | 68 69 |
| FB_A_WDQS0 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<0> | 68 69 |
| FB_A_WDQS1 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<1> | 68 69 |
| FB_A_WDQS2 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<2> | 68 69 |
| FB_A_WDQS3 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<3> | 68 69 |
| FB_A_RDQS0 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<0> | 68 69 |
| FB_A_RDQS1 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<1> | 68 69 |
| FB_A_RDQS2 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<2> | 68 69 |
| FB_A_RDQS3 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<3> | 68 69 |
| FB_A_DQ_BYTE0 | GDDR3_50SE | GDDR3_DATA | FB A DQ<7..0> | 68 69 |
| FB_A_DQ_BYTE1 | GDDR3_50SE | GDDR3_DATA | FB A DQ<15..8> | 68 69 |
| FB_A_DQ_BYTE2 | GDDR3_50SE | GDDR3_DATA | FB A DQ<23..16> | 68 69 |
| FB_A_DQ_BYTE3 | GDDR3_50SE | GDDR3_DATA | FB A DQ<31..24> | 68 69 |
| FB_A_DQM0 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<0> | 68 69 |
| FB_A_DQM1 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<1> | 68 69 |
| FB_A_DQM2 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<2> | 68 69 |
| FB_A_DQM3 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<3> | 68 69 |
| FB_B_WDQS0 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<4> | 68 69 |
| FB_B_WDQS1 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<5> | 68 69 |
| FB_B_WDQS2 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<6> | 68 69 |
| FB_B_WDQS3 | GDDR3_50SE | GDDR3_DQS | FB A WDQS<7> | 68 69 |
| FB_B_RDQS0 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<4> | 68 69 |
| FB_B_RDQS1 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<5> | 68 69 |
| FB_B_RDQS2 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<6> | 68 69 |
| FB_B_RDQS3 | GDDR3_50SE | GDDR3_DQS | FB A RDQS<7> | 68 69 |
| FB_B_DQ_BYTE0 | GDDR3_50SE | GDDR3_DATA | FB A DQ<39..32> | 68 69 |
| FB_B_DQ_BYTE1 | GDDR3_50SE | GDDR3_DATA | FB A DQ<47..40> | 68 69 |
| FB_B_DQ_BYTE2 | GDDR3_50SE | GDDR3_DATA | FB A DQ<55..48> | 68 69 |
| FB_B_DQ_BYTE3 | GDDR3_50SE | GDDR3_DATA | FB A DQ<63..56> | 68 69 |
| FB_B_DQM0 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<4> | 68 69 |
| FB_B_DQM1 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<5> | 68 69 |
| FB_B_DQM2 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<6> | 68 69 |
| FB_B_DQM3 | GDDR3_50SE | GDDR3_DATA | FB A DQM L<7> | 68 69 |

GDDR3 FB C/D Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | PROPERTY | VALUE |
|---------------------------|---------------|------------|-----------------|-------|
| | PHYSICAL | SPACING | | |
| FB_C_CLK_P | GDDR3_80D | GDDR3_CLK | FB B CLK P<0> | 68 70 |
| FB_C_CLK_N | GDDR3_80D | GDDR3_CLK | FB B CLK N<0> | 68 70 |
| FB_D_CLK_P | GDDR3_80D | GDDR3_CLK | FB B CLK P<1> | 68 70 |
| FB_D_CLK_N | GDDR3_80D | GDDR3_CLK | FB B CLK N<1> | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B MA<1..0> | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B MA<11..6> | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B BA<2..0> | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B RAS L | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B CAS L | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B WE L | 68 70 |
| FB_CD_CMD_PD | GDDR3_40R50SE | GDDR3_CMD | FB B CKE | 68 70 |
| FB_CD_CMD | GDDR3_40R50SE | GDDR3_CMD | FB B CS0 L | 68 70 |
| FB_CD_CMD_PD | GDDR3_40R50SE | GDDR3_CMD | FB B DRAM RST | 68 70 |
| FB_C_CMD | GDDR3_50SE | GDDR3_CMD | FB B LMA<5..2> | 68 70 |
| FB_D_CMD | GDDR3_50SE | GDDR3_CMD | FB B UMA<5..2> | 68 70 |
| FB_C_WDQS0 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<0> | 68 70 |
| FB_C_WDQS1 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<1> | 68 70 |
| FB_C_WDQS2 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<2> | 68 70 |
| FB_C_WDQS3 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<3> | 68 70 |
| FB_C_RDQS0 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<0> | 68 70 |
| FB_C_RDQS1 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<1> | 68 70 |
| FB_C_RDQS2 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<2> | 68 70 |
| FB_C_RDQS3 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<3> | 68 70 |
| FB_C_DQ_BYTE0 | GDDR3_50SE | GDDR3_DATA | FB B DQ<7..0> | 68 70 |
| FB_C_DQ_BYTE1 | GDDR3_50SE | GDDR3_DATA | FB B DQ<15..8> | 68 70 |
| FB_C_DQ_BYTE2 | GDDR3_50SE | GDDR3_DATA | FB B DQ<23..16> | 68 70 |
| FB_C_DQ_BYTE3 | GDDR3_50SE | GDDR3_DATA | FB B DQ<31..24> | 68 70 |
| FB_C_DQM0 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<0> | 68 70 |
| FB_C_DQM1 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<1> | 68 70 |
| FB_C_DQM2 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<2> | 68 70 |
| FB_C_DQM3 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<3> | 68 70 |
| FB_D_WDQS0 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<4> | 68 70 |
| FB_D_WDQS1 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<5> | 68 70 |
| FB_D_WDQS2 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<6> | 68 70 |
| FB_D_WDQS3 | GDDR3_50SE | GDDR3_DQS | FB B WDQS<7> | 68 70 |
| FB_D_RDQS0 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<4> | 68 70 |
| FB_D_RDQS1 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<5> | 68 70 |
| FB_D_RDQS2 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<6> | 68 70 |
| FB_D_RDQS3 | GDDR3_50SE | GDDR3_DQS | FB B RDQS<7> | 68 70 |
| FB_D_DQ_BYTE0 | GDDR3_50SE | GDDR3_DATA | FB B DQ<39..32> | 68 70 |
| FB_D_DQ_BYTE1 | GDDR3_50SE | GDDR3_DATA | FB B DQ<47..40> | 68 70 |
| FB_D_DQ_BYTE2 | GDDR3_50SE | GDDR3_DATA | FB B DQ<55..48> | 68 70 |
| FB_D_DQ_BYTE3 | GDDR3_50SE | GDDR3_DATA | FB B DQ<63..56> | 68 70 |
| FB_D_DQM0 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<4> | 68 70 |
| FB_D_DQM1 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<5> | 68 70 |
| FB_D_DQM2 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<6> | 68 70 |
| FB_D_DQM3 | GDDR3_50SE | GDDR3_DATA | FB B DQM L<7> | 68 70 |

G84M Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | PROPERTY | VALUE |
|---------------------------|--------------|----------|---------------------|----------|
| | PHYSICAL | SPACING | | |
| (CK505_DOT96) | CLK_SLOW_55S | CLK_SLOW | GPU CLK27M | 30 |
| | CLK_SLOW_55S | CLK_SLOW | GPU CLK27M_GATED | 30 72 |
| CK505_CLK27MSS | CLK_SLOW_55S | CLK_SLOW | GPU CLK27M_SS | 30 |
| | CLK_SLOW_55S | CLK_SLOW | GPU CLK27M_SS_GATED | 30 72 |
| | LVDS_100D | LVDS | LVDS L CLK P | 73 77 |
| | LVDS_100D | LVDS | LVDS L CLK N | 73 77 |
| | LVDS_100D | LVDS | LVDS L DATA P<3..0> | 72 73 77 |
| | LVDS_100D | LVDS | LVDS L DATA N<3..0> | 72 73 77 |
| | LVDS_100D | LVDS | LVDS U CLK P | 73 77 |
| | LVDS_100D | LVDS | LVDS U CLK N | 73 77 |
| | LVDS_100D | LVDS | LVDS U DATA P<3..0> | 72 73 77 |
| | LVDS_100D | LVDS | LVDS U DATA N<3..0> | 72 73 77 |
| TMDS_CLK | TMDS_100D | TMDS | TMDS CLK P | 73 76 |
| TMDS_CLK | TMDS_100D | TMDS | TMDS CLK N | 73 76 |
| TMDS_DATA | TMDS_100D | TMDS | TMDS DATA P<5..0> | 73 76 |
| TMDS_DATA | TMDS_100D | TMDS | TMDS DATA N<5..0> | 73 76 |
| VGA_B_TV_C | VGA_50S | VGA | GPU TV_C VGA_R | 72 76 |
| VGA_G_TV_Y | VGA_50S | VGA | GPU TV_Y VGA_G | 72 76 |
| VGA_B_TV_COMP | VGA_50S | VGA | GPU TV_COMP VGA_B | 72 76 |
| | VGA_50S | VGA | GPU VGA_R | 72 73 |
| | VGA_50S | VGA | GPU VGA_G | 72 73 |
| | VGA_50S | VGA | GPU VGA_B | 72 73 |
| | VGA_50S | VGA | GPU TV_C | 72 73 |
| | VGA_50S | VGA | GPU TV_Y | 72 73 |
| | VGA_50S | VGA | GPU TV_COMP | 72 73 |
| VGA_SYNC | VGA_55S | VGA_SYNC | GPU VGA_HSYNC | 73 76 |
| VGA_SYNC | VGA_55S | VGA_SYNC | GPU VGA_VSYNC | 73 76 |

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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| SCALE | SHT | OF | |
| NONE | 107 | 109 | |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SENSE_1T01_55S | * | =1:1_DIFFPAIR | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =1:1_DIFFPAIR | =1:1_DIFFPAIR |
| THERM_1T01_55S | * | =1:1_DIFFPAIR | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =1:1_DIFFPAIR | =1:1_DIFFPAIR |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SENSE | * | =2:1_SPACING | ? |
| THERM | * | =2:1_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| ENETCONN | * | 25 MILS | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND | * | =STANDARD | ? |
| PP1V8_MEM | * | =STANDARD | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND_P2MM | * | 0.20 MM | 1000 |
| PWR_P2MM | * | 0.20 MM | 1000 |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK | GND | * | GND_P2MM |
| MEM_CMD | GND | * | GND_P2MM |
| MEM_CTRL | GND | * | GND_P2MM |
| MEM_DATA | GND | * | GND_P2MM |
| MEM_DQS | GND | * | GND_P2MM |
| MEM_CLK | PP1V8_MEM | * | PWR_P2MM |
| MEM_CMD | PP1V8_MEM | * | PWR_P2MM |
| MEM_CTRL | PP1V8_MEM | * | PWR_P2MM |
| MEM_DATA | PP1V8_MEM | * | PWR_P2MM |
| MEM_DQS | PP1V8_MEM | * | PWR_P2MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CLINK_VREF | GND | * | GND_P2MM |
| CLK_MED | GND | * | GND_P2MM |
| CLK_PCIE | GND | * | GND_P2MM |
| DMI | GND | * | GND_P2MM |
| PCIE | GND | * | GND_P2MM |
| SATA | GND | * | GND_P2MM |
| USB | GND | * | GND_P2MM |
| CLK_PCIE | SB_POWER | * | PWR_P2MM |
| DMI | SB_POWER | * | PWR_P2MM |
| SATA | SB_POWER | * | PWR_P2MM |
| USB | SB_POWER | * | PWR_P2MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| LVDS | GND | * | GND_P2MM |

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|--------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_70D | BOTTOM | | | 0.127 MM | 6.35 MM | | |

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_45S_OVERRIDE | * | VERRIDE | VERRIDE | 0.100 MM_OVERRIDE | 2.54 MM_OVERRIDE | VERRIDE | VERRIDE |
| MEM_70D | ISL10 | | | 0.100 MM | 2.54 MM | | |
| MEM_85D | ISL4, ISL10 | | | 0.100 MM | 2.54 MM | | |

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| LVDS_100D | BGA | 100_DIFF_BGA |
| TMDS_100D | BGA | 100_DIFF_BGA |

SIM Card Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| WWAN_SIM | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| WWAN_SIM | * | =2:1_SPACING | ? |

M75 Specific Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE | | |
|---------------------------|----------------|----------|--------------------------|
| | PHYSICAL | SPACING | |
| (PCIE_EXCARD) | PCIE_100D | PCIE | PCIE_EXCARD_R2D_P |
| (PCIE_EXCARD) | PCIE_100D | PCIE | PCIE_EXCARD_R2D_N |
| (PCIE_MINI) | PCIE_100D | PCIE | PCIE_MINI_R2D_P |
| (PCIE_MINI) | PCIE_100D | PCIE | PCIE_MINI_R2D_N |
| | ENET_100D | ENET_MDI | ENET_MDI_R_P<3..0> |
| | ENET_100D | ENET_MDI | ENET_MDI_R_N<3..0> |
| | ENET_100D | ENETCONN | ENETCONN_P<3..0> |
| | ENET_100D | ENETCONN | ENETCONN_N<3..0> |
| | FW_110D | FW_TP | FW_PORT0_TPA_FL_P |
| | FW_110D | FW_TP | FW_PORT0_TPA_FL_N |
| | FW_110D | FW_TP | FW_PORT0_TPB_FL_P |
| | FW_110D | FW_TP | FW_PORT0_TPB_FL_N |
| (SATA_A_R2D) | SATA_100D | SATA | SATA_A_R2D_UF_P |
| (SATA_A_R2D) | SATA_100D | SATA | SATA_A_R2D_UF_N |
| (SATA_A_D2R) | SATA_100D | SATA | SATA_A_D2R_UF_P |
| (SATA_A_D2R) | SATA_100D | SATA | SATA_A_D2R_UF_N |
| (USB_EXT_A) | USB_90D | USB | USB2_EXT_A_MUXED_P |
| (USB_EXT_A) | USB_90D | USB | USB2_EXT_A_MUXED_N |
| (USB_EXT_A) | USB_90D | USB | USB2_RT_P |
| (USB_EXT_A) | USB_90D | USB | USB2_RT_N |
| (USB_EXT_D) | USB_90D | USB | USB_WWAN_F_P |
| (USB_EXT_D) | USB_90D | USB | USB_WWAN_F_N |
| (USB_CAMERA) | USB_90D | USB | USB_CAMERA_F_P |
| (USB_CAMERA) | USB_90D | USB | USB_CAMERA_F_N |
| SENSE_DIFFPAIR | SENSE_1T01_55S | SENSE | GFXIMVP6_VSEN_P |
| SENSE_DIFFPAIR | SENSE_1T01_55S | SENSE | NBCOREISNS_P |
| SENSE_DIFFPAIR | SENSE_1T01_55S | SENSE | P1V8ISNS_P |
| SENSE_DIFFPAIR | SENSE_1T01_55S | SENSE | P1V25ISNS_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | CPU_THMSNS_D2_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | CPU_THERMD_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | GPU_THMSNS_D_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | GPU_TDIODE_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | HSTHMSNS_D_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | REMTHMSNS_DX_P |
| THERM_DIFFPAIR | THERM_1T01_55S | THERM | RSFSTHMSNS_D_P |
| | LVDS_100D | LVDS | LVDS_L_CLK_CONN_F_P |
| | LVDS_100D | LVDS | LVDS_L_CLK_CONN_F_N |
| | LVDS_100D | LVDS | LVDS_L_CLK_CONN_P |
| | LVDS_100D | LVDS | LVDS_L_CLK_CONN_N |
| | LVDS_100D | LVDS | LVDS_L_DATA_CONN_P<3..0> |
| | LVDS_100D | LVDS | LVDS_L_DATA_CONN_N<3..0> |
| | LVDS_100D | LVDS | LVDS_U_CLK_CONN_P |
| | LVDS_100D | LVDS | LVDS_U_CLK_CONN_N |
| | LVDS_100D | LVDS | LVDS_U_DATA_CONN_P<3..0> |
| | LVDS_100D | LVDS | LVDS_U_DATA_CONN_N<3..0> |
| | TMDS_100D | TMDS | TMDS_CLK_R_P |
| | TMDS_100D | TMDS | TMDS_CLK_R_N |
| | TMDS_100D | TMDS | TMDS_CLK_F_P |
| | TMDS_100D | TMDS | TMDS_CLK_F_N |
| | TMDS_100D | TMDS | TMDS_DATA_F_P<5..0> |
| | TMDS_100D | TMDS | TMDS_DATA_F_N<5..0> |
| (VGA_R_TV_Y) | VGA_50S | VGA | VGA_R |
| (VGA_G_TV_C) | VGA_50S | VGA | VGA_G |
| (VGA_B_TV_COMP) | VGA_50S | VGA | VGA_B |
| (VGA_SYNC) | VGA_55S | VGA_SYNC | VGA_HSYNC_R |
| (VGA_SYNC) | VGA_55S | VGA_SYNC | VGA_VSYNC_R |
| (VGA_SYNC) | VGA_55S | VGA_SYNC | VGA_HSYNC |
| (VGA_SYNC) | VGA_55S | VGA_SYNC | VGA_VSYNC |
| | PP1V8_MEM | | =PP1V8_S3M_MEM_A |
| | PP1V8_MEM | | =PP1V8_S3M_MEM_B |
| | GND | | GND |
| | SB_POWER | | PP3V3_S5 |
| | SB_POWER | | PP3V3_S0 |
| | SB_POWER | | PP1V5_S0 |
| WWAN_SIM | WWAN_SIM | | WWAN_SIM_CLOCK |
| WWAN_SIM | WWAN_SIM | | WWAN_SIM_DATA |

D

C

B

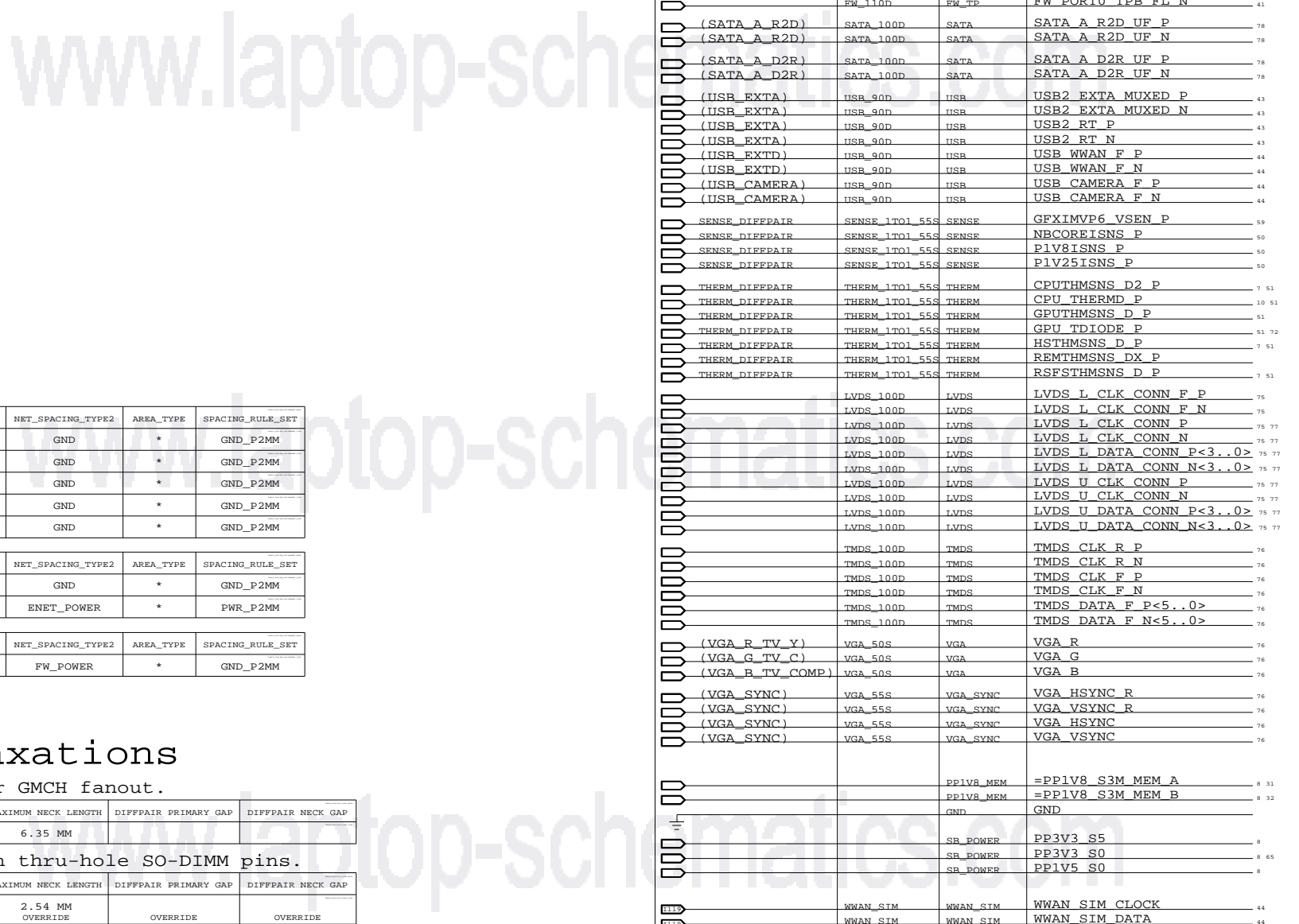
A

D

C

B

A



www.laptop-schematics.com

| Project Specific Constraints | | |
|--|--------------------|--|
| SYNC_MASTER=(MASTER) | SYNC_DATE=(MASTER) | |
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7435 | A |
| SCALE | NONE | SHT | 108 OF 109 |

M75 Board-Specific Spacing & Physical Constraints

| BOARD LAYERS | | | | BOARD AREAS | | | BOARD UNITS (MIL OR MM) | ALLEGRO VERSION |
|---|--|--|--|--------------|--|--|----------------------------|--------------------|
| TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM | | | | NO_TYPE, BGA | | | MM | 15.5.1 |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DEFAULT | * | Y | =55_OHM_SE | =55_OHM_SE | 30 MM | 0 MM | 0 MM |
| STANDARD | * | Y | =DEFAULT | =DEFAULT | 12.7 MM | =DEFAULT | =DEFAULT |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 55_OHM_SE | TOP, BOTTOM | Y | 0.100 MM | 0.100 MM | | | |
| 55_OHM_SE | ISL2, ISL11 | Y | 0.250 MM | 0.076 MM | | | |
| 55_OHM_SE | * | Y | 0.076 MM | 0.076 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 50_OHM_SE | TOP, BOTTOM | Y | 0.125 MM | 0.125 MM | | | |
| 50_OHM_SE | * | Y | 0.090 MM | 0.090 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 45_OHM_SE | TOP, BOTTOM | Y | 0.150 MM | 0.150 MM | | | |
| 45_OHM_SE | * | Y | 0.105 MM | 0.105 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 40_OHM_SE | TOP, BOTTOM | Y | 0.185 MM | 0.185 MM | | | |
| 40_OHM_SE | * | Y | 0.131 MM | 0.131 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 27P4_OHM_SE | TOP, BOTTOM | Y | 0.335 MM | 0.335 MM | | | |
| 27P4_OHM_SE | * | Y | 0.240 MM | 0.240 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 70_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 70_OHM_DIFF | ISL3, ISL4 | Y | 0.149 MM | 0.149 MM | | 0.125 MM | 0.125 MM |
| 70_OHM_DIFF | ISL9, ISL10 | Y | 0.149 MM | 0.149 MM | | 0.125 MM | 0.125 MM |
| 70_OHM_DIFF | ISL2, ISL11 | Y | 0.185 MM | 0.185 MM | | 0.125 MM | 0.125 MM |
| 70_OHM_DIFF | TOP, BOTTOM | Y | 0.185 MM | 0.185 MM | | 0.125 MM | 0.125 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 80_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 80_OHM_DIFF | ISL3, ISL4 | Y | 0.115 MM | 0.115 MM | | 0.125 MM | 0.125 MM |
| 80_OHM_DIFF | ISL9, ISL10 | Y | 0.115 MM | 0.115 MM | | 0.125 MM | 0.125 MM |
| 80_OHM_DIFF | ISL2, ISL11 | Y | 0.140 MM | 0.140 MM | | 0.125 MM | 0.125 MM |
| 80_OHM_DIFF | TOP, BOTTOM | Y | 0.140 MM | 0.140 MM | | 0.125 MM | 0.125 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 85_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 85_OHM_DIFF | ISL3, ISL4 | Y | 0.101 MM | 0.101 MM | | 0.125 MM | 0.125 MM |
| 85_OHM_DIFF | ISL9, ISL10 | Y | 0.101 MM | 0.101 MM | | 0.125 MM | 0.125 MM |
| 85_OHM_DIFF | ISL2, ISL11 | Y | 0.125 MM | 0.125 MM | | 0.125 MM | 0.125 MM |
| 85_OHM_DIFF | TOP, BOTTOM | Y | 0.125 MM | 0.125 MM | | 0.125 MM | 0.125 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 90_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 90_OHM_DIFF | ISL3, ISL4 | Y | 0.102 MM | 0.102 MM | | 0.220 MM | 0.220 MM |
| 90_OHM_DIFF | ISL9, ISL10 | Y | 0.102 MM | 0.102 MM | | 0.220 MM | 0.220 MM |
| 90_OHM_DIFF | ISL2, ISL11 | Y | 0.130 MM | 0.130 MM | | 0.220 MM | 0.220 MM |
| 90_OHM_DIFF | TOP, BOTTOM | Y | 0.130 MM | 0.130 MM | | 0.220 MM | 0.220 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 100_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 100_OHM_DIFF | ISL3, ISL4 | Y | 0.080 MM | 0.080 MM | | 0.200 MM | 0.200 MM |
| 100_OHM_DIFF | ISL9, ISL10 | Y | 0.080 MM | 0.080 MM | | 0.200 MM | 0.200 MM |
| 100_OHM_DIFF | ISL2, ISL11 | Y | 0.099 MM | 0.099 MM | | 0.200 MM | 0.200 MM |
| 100_OHM_DIFF | TOP, BOTTOM | Y | 0.099 MM | 0.099 MM | | 0.200 MM | 0.200 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 110_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 110_OHM_DIFF | ISL3, ISL4 | Y | 0.077 MM | 0.077 MM | | 0.330 MM | 0.330 MM |
| 110_OHM_DIFF | ISL9, ISL10 | Y | 0.077 MM | 0.077 MM | | 0.330 MM | 0.330 MM |
| 110_OHM_DIFF | ISL2, ISL11 | Y | 0.089 MM | 0.089 MM | | 0.330 MM | 0.330 MM |
| 110_OHM_DIFF | TOP, BOTTOM | Y | 0.089 MM | 0.089 MM | | 0.330 MM | 0.330 MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| DEFAULT | * | 0.1 MM | ? |
| STANDARD | * | =DEFAULT | ? |
| BGA_P1MM | * | =DEFAULT | ? |
| BGA_P2MM | * | =DEFAULT | ? |
| BGA_P3MM | * | =DEFAULT | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| 1.5:1_SPACING | * | 0.15 MM | ? |
| 1.8:1_SPACING | * | 0.18 MM | ? |
| 2:1_SPACING | * | 0.2 MM | ? |
| 2.5:1_SPACING | * | 0.25 MM | ? |
| 3:1_SPACING | * | 0.3 MM | ? |
| 4:1_SPACING | * | 0.4 MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| * | * | BGA | BGA_P1MM |
| MEM_CLK | * | BGA | BGA_P2MM |
| CLK_FSB | * | BGA | BGA_P2MM |
| CLK_PCIE | * | BGA | BGA_P2MM |
| CLK_MED | * | BGA | BGA_P2MM |
| CLK_SLOW | * | BGA | BGA_P2MM |
| FSB_DSTB | FSB_DSTB | BGA | BGA_P3MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 1:1_DIFFPAIR | * | Y | =STANDARD | =STANDARD | =STANDARD | 0.1 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 100_DIFF_BGA | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| 100_DIFF_BGA | ISL3, ISL4 | Y | 0.075 MM | 0.075 MM | | 0.125 MM | 0.125 MM |
| 100_DIFF_BGA | ISL9, ISL10 | Y | 0.075 MM | 0.075 MM | | 0.125 MM | 0.125 MM |

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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| SCALE | SHT | OF | |
| NONE | 109 | 109 | |