1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,TRUCKEE,M57

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

8/16/2006

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7164	1	SCHEM,TRUCKEE,M57	SCH	CRITICAL	
820-2059	1	PCBF,TRUCKEE,M57	PCB	CRITICAL	

DRAWING
TITLE=TRUCKEE
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 16 19:10:01 2006

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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TITLE
SCHEM.TRUCKEE,M57

DRAWING NUMBER 051-7164 REV. 03001

SHT 1 OF 87

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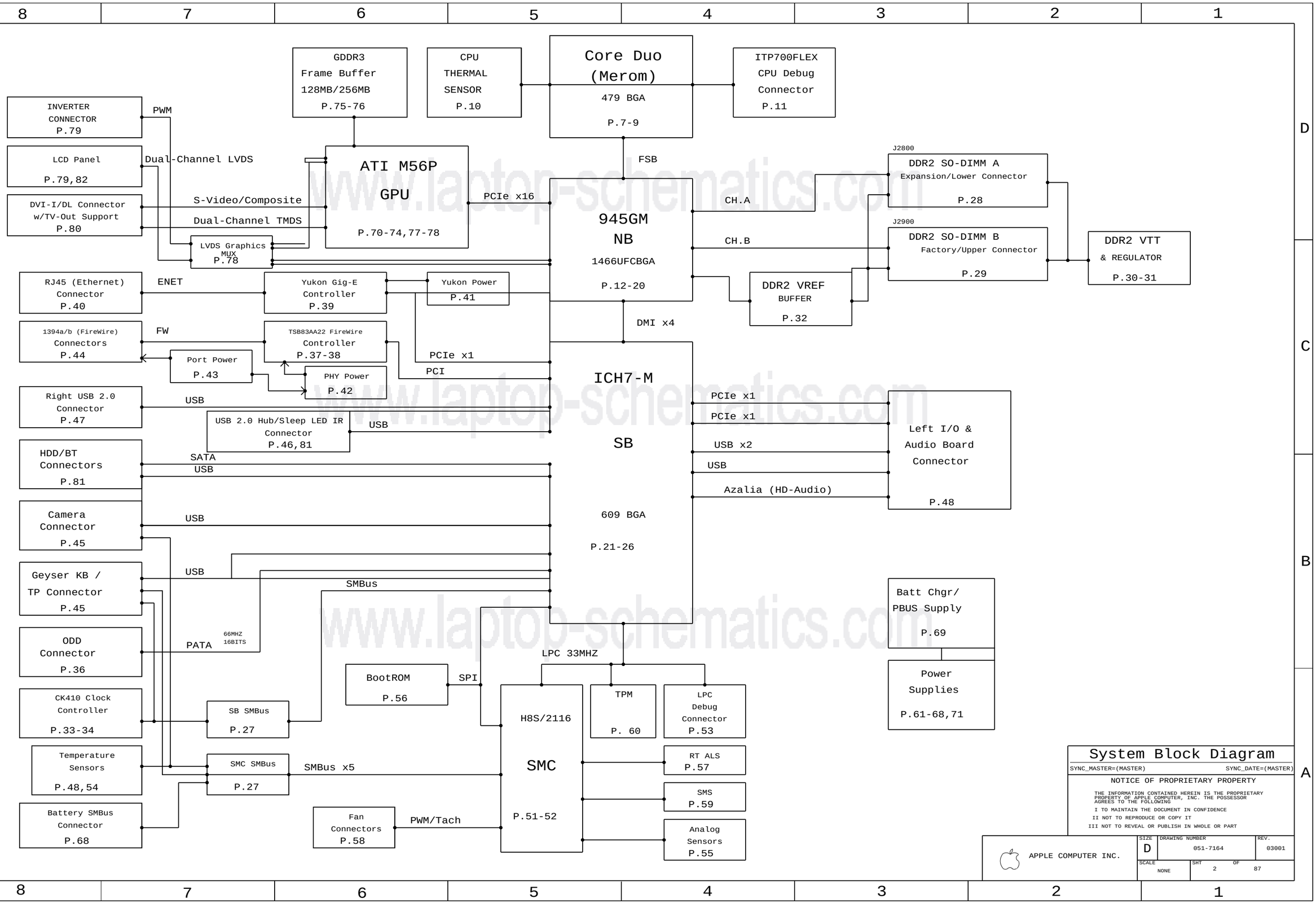

System Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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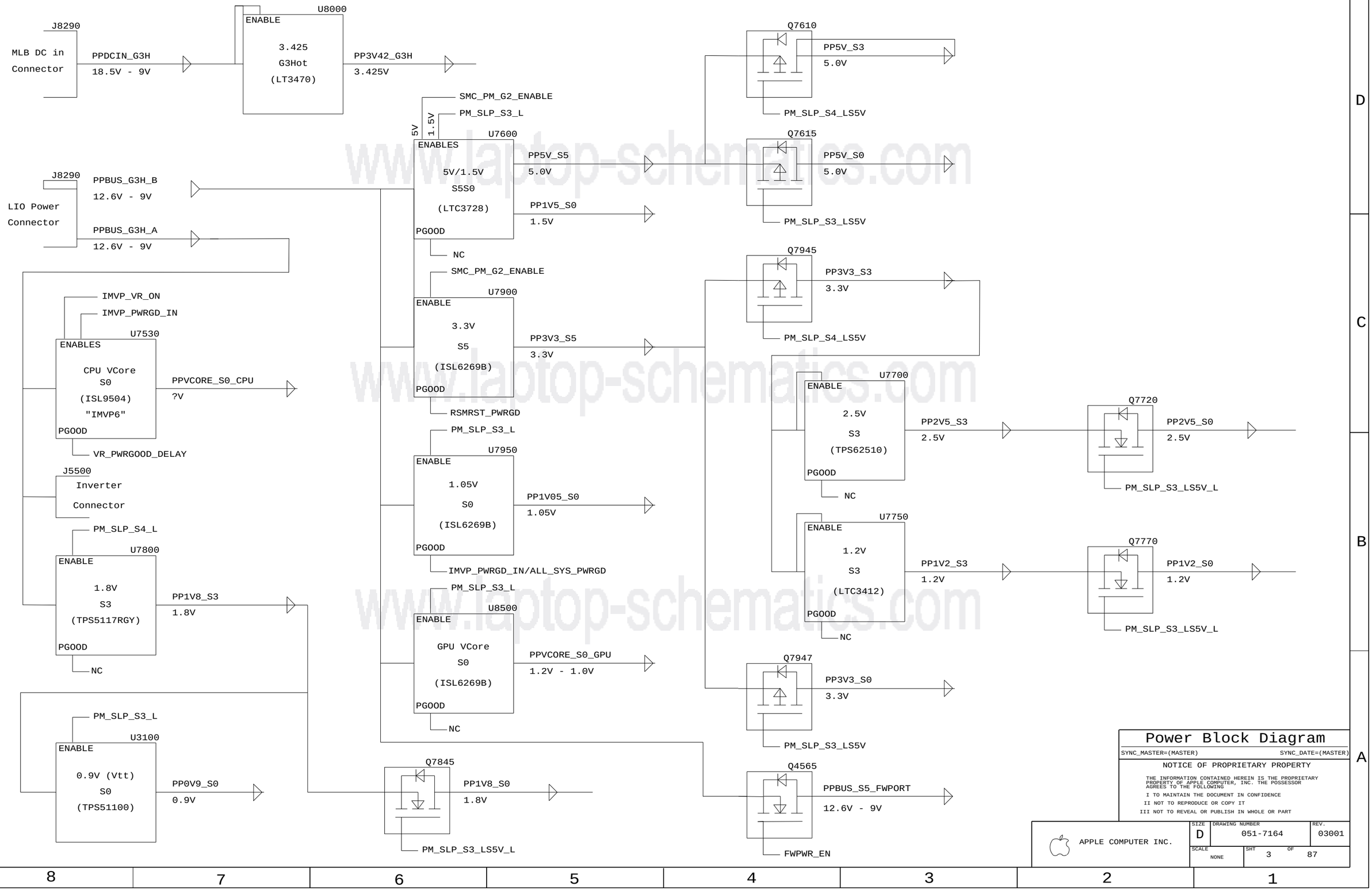
SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	2	87



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Power Block Diagram

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SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 3 OF 87	

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7813	TRUCKEE,2.16GHZ,B2,256VRAM,INF,M57	VRAM_256INF,M57_COMMON,CPU_2_16GHZ_B2,EEE_WJJ
630-7812	TRUCKEE,2.16GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_16GHZ_B2,EEE_WJH

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7815	TRUCKEE,2.33GHZ,B2,256VRAM,INF,M57	VRAM_256INF,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJL
630-7814	TRUCKEE,2.33GHZ,B2,256VRAM,SAM,M57	VRAM_256SAM,M57_COMMON,CPU_2_33GHZ_B2,EEE_WJK

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG
VRAM_128INF	GPU_MEM_NOT_SAM,VRAM_128_INFINEON
VRAM_256INF	GPU_MEM_NOT_SAM,GPU_MEM_256M,VRAM_256_INFINEON

BOM GROUP	BOM OPTIONS
M57_COMMON	ALTERNATE,COMMON,M57_COMMON1,M57_COMMON2,M57_COMMON3,M57_COMMON4,M57_DEBUG,ISL6255A,M57_NO_3G
M57_COMMON1	ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL
M57_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M57_COMMON3	LVDS_PD,FW_PORT_FAULT_PU
M57_COMMON4	BOOTROM_DEVEL,SMC_PRGRM
M57_DEBUG	ITP,ITPCONN,LPCPLUS
M57_TPM	TPM
M57_3G	3G
M57_NO_3G	NO_3G

BAR CODE LABELS / EEE #'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W9J]	CRITICAL	EEE_WJJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W3A]	CRITICAL	EEE_WJH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:W3A]	CRITICAL	EEE_WJK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WDV]	CRITICAL	EEE_WJL

MODULE PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0368	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON

ALTERNATE PARTS

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445		ALL	SI7806ADN for FDM6296
128S0083	128S0073		C2516	1.86 MAX ALT TO 1.9 MAX
128S0093	128S0092		ALL	KEMET IS ALT TO SANYO
128S0094	128S0060		ALL	330UF,2V,9MOHM,D2
128S0095	128S0060		ALL	330UF,2V,6MOHM,D2
128S0081	128S0061		ALL	150UF,6.3V,25MOHM,C2
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504
152S0287	152S0435		ALL	Alternates for Coilcraft MSS5131
157S0030	157S0111		ALL	Alternates for E&E Magnetics, TDK

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1931	1	IC,PRGRM,SMC(NEW),M57	U5800	CRITICAL	SMC_PRGRM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1924	1	IC, BOOTROM, DEVELOPMENT, UNLOCKED ,M57	U6301	CRITICAL	BOOTROM_DEVEL
341S1925	1	IC, BOOTROM, FINAL, LOCKED, M57	U6301	CRITICAL	BOOTROM_FINAL
353S1461	1	IC,ISL9504,SYNC REG CTL,QFN 48	U7530	CRITICAL	
359S0109	1	IC,LOW POWER CLOCK SYNTHESIZER,68PIN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3391	1	IC,MDC,B2,PRQ,2.16GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_16GHZ_B2
337S3393	1	IC,MDC,B2,PRQ,2.33GHZ,34W,667M,4M,479 BGA	U0700	CRITICAL	CPU_2_33GHZ_B2
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	

Extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

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BOM CONFIGURATION

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE	SHT	OF
NONE	4	87

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	61C7
TRUE		P5VS5_RUNSS	62C5 66A6
TRUE		P1V5S0_RUNSS	62C4 66C6
TRUE		P2V5S3_MODE	
TRUE		P2V5S3_SHDNRT	
TRUE		P1V2S3_RT	63B6
TRUE		P1V2S3_RUNSS	41C4 63B7
TRUE		P1V8S3_COMP	
TRUE		P1V8S3_FSET	
TRUE		P3V3S5_COMP	65C6
TRUE		P3V3S5_FSET	65D6
TRUE		P1V05S0_COMP	65A7
TRUE		P1V05S0_FSET	65B7
TRUE		P3V42G3H_FB	66C3
TRUE		GPUVCORE_COMP	71C7
TRUE		GPUVCORE_FSET	71C7
TRUE		GPUBBP_ADJ	71B7

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 87D6
TRUE		FSB_ADS_L	7D6 12C4 87D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 87C6
TRUE		FSB_BNR_L	7D6 12C4 87D6
TRUE		FSB_BREQ0_L	7D6 12C4 87D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 87D6
TRUE		FSB_DBSY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_DRDY_L	7D6 12B4 87D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 87D6
TRUE		FSB_HIT_L	7D6 12B4 87D6
TRUE		FSB_HITM_L	7D6 12B4 87D6
TRUE		FSB_LOCK_L	7D6 12B4 87D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 87D6

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 33B4 34C3 34C5
TRUE	SB_CLK100M_SATA_N	21B6 33B4 34C3 34C5
TRUE	USB_BT_P	6C1 6C2 6C3 22C2 81A4
TRUE	USB_BT_N	6C1 6C2 6C3 22C2 81A4

Misc NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		USB2_CAMERA_P_F	45B5
TRUE		USB2_CAMERA_N_F	45B5
TRUE		TP_FW_CTL<0>	37C3

Power Nets

FUNC_TEST		
TRUE	PP0V9_S0	19D3 34B8 34C4 34C8 35B4 65A2 67D6 67D8
TRUE	PP1V05_S0	19D3 19D4 34C3 34C5 37D3 37D4
TRUE	PP1V2_D3C	68J 78C 78E 79B 80J 80K 11B3 11C5 12A7 12B7 12C2 19C8 19D1 19D2 19D5 19D6
TRUE	PP1V2_S3	5A4 39A8 39D7 63B3 67D6 67D8
TRUE	PP1V5_S0	19C5 19D3 19D2 19D5 19D6 19D7 19D1 19D2 19D4 37C2 37C3 37C4 37C5
TRUE	PP1V5_S0_NB	31C5 32C6 37B2 64A6 64C1 68J 14C2 14B8 19D2 19D3 29D2 29D3 29D6 67B6 67B8
TRUE	PP1V8_S3	64A4 67B6 67B8 72B8 73A5 73A8 73B5 73B8 75D5 75D8 76D5 76D8 82D7
TRUE	PP1V8_D3C	37C6 37D6 13A4 19A6 19A8 19C5 19D7 63D1 68B6 67A6 67A8 67B8 82C6 82D3
TRUE	PP2V5_S0	63C1 67A6 67A8 77A8 77C6 78C8 82D7
TRUE	PP2V5_D3C	
TRUE	PP3V3_S0	
TRUE	PP3V3_S3	
TRUE	PP3V3_S5	65D8 66C5 67C3 67D3 67D5 79D5 24C3 25B6 25C8 25D2 25C7 11B6 22C6 23D8 23A7 23B7 63D1 63D4 67D6 68A1 68B1
TRUE	PP5V_S0	
TRUE	PP5V_S3	5B2 45C3 52B8 62A2 67B1 67B3 81C4 81C6
TRUE	PP5V_S5	60D8 60D6 67B1 67C1 67C3 67D2 67C4 67D4 67D6 68A1 68B1 62B6 62C8 64C8 65B7 65D6 71D7
TRUE	PPBUS_G3H	6A1 41C6 42B8 43B8 65D3 81D4 81D7 81D7 64A6 64D7 65B7 65D6 69C1 71D7 79B7
TRUE	GND	

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TRUE	IMVP_VR_ON	51D7 61C7
TRUE	IMVP_DPRSLPVR	61C7 87C6
TRUE	PM_SLP_S3_L	66C8 27C3 32B3 39C8 42A8 42C8 51C5 55C3 65B8 66A6 66C7
TRUE	PM_SLP_S3BATT	41B5
TRUE	PM_SLP_S4_L	66B8 66C1 6A1 6A2 23C3 41B6 47C7 48C3 51C5 64C8 66A6
TRUE	PM_SLP_S5_L	23C3 51C5 52A2
TRUE	P1V5P1V05S0_PGOOD	61C7 65B8 66B2 66B3 66B5
TRUE	CPU_DPRSTP_L	7B3 21C4 61C7
TRUE	IMVP6_VID<6..0>	9C1 61C7
TRUE	FSB_CLK_CPU_N	7C6 33C4 34D3 34D5
TRUE	FSB_CLK_CPU_P	7C6 33C4 34D3 34D5
TRUE	PLT_RST_L	82A4
TRUE	PLT_RST_L	5C4 6C6 6C7 14B7 22A6 26A4 26B1 26C1 26C3 79A8
TRUE	PEG_RESET_L	26B1 70A5 82A4
TRUE	SMC_LRESET_L	26B1 51C7
TRUE	TPM_LRESET_L	26B1 60B7
TRUE	CPU_STPCLK_L	7C8 21C4 87C6
TRUE	FSB_CLK_NB_P	12A6 33C4 34D3 34D5
TRUE	FSB_CLK_NB_N	12A6 33C4 34D3 34D5
TRUE	CLK_NB_OE_L	14B6 33B4
TRUE	NB_CLK100M_GCLKIN_P	14C4 33B4 34C4 34C5
TRUE	NB_CLK100M_GCLKIN_N	14C4 33B4 34C4 34C5
TRUE	NB_CLK_DREFCLKIN_P	14C4 34B2 34B4
TRUE	NB_CLK_DREFCLKIN_N	14C4 34B2 34B4
TRUE	NB_CLK_DREFSSCLKIN_P	14B4 33B4 34B4 34B5
TRUE	NB_CLK_DREFSSCLKIN_N	14C4 33B4 34B4 34B5
TRUE	CPU_THERMTRIP_R	21C2
TRUE	TP_SB_SUS_CLK	6C6 6C7 23C3

MAC-1 TPs

FUNC_TEST		
TRUE	CPU_PWRGD	7B3 21C4 87C6
TRUE	TP_CPU_CPUSLP_L	21C4
TRUE	PM_DPRSLPVR	14B7 23C3 61C8 87C6
TRUE	CPU_DPSLP_L	7B3 21C4 87C6
TRUE	PM_LAN_ENABLE	23C3 51D7
TRUE	PCI_RST_L	22A6 37C2
TRUE	PM_RSMRST_L	23C1 51D7
TRUE	PM_SB_PWROK	23C3 26A6
TRUE	SB_RTC_RST_L	21D6 26D4
TRUE	PM_STPCPU_L	23C8 33C4
TRUE	PM_STPPCI_L	23C8 33C4
TRUE	VR_PWRGD_CK410	23C5 26B8
TRUE	VR_PWRGOOD_DELAY	14B6 26B5 61C7
TRUE	FSB_CPURST_L	7D6 11B5 12C4 87D6
TRUE	FSB_SLPCPU_L	7A3 12A4
TRUE	FSB_DPWR_L	7B3 12B4 87D6
TRUE	NB_SB_SYNC_L	14B6 22A6
TRUE	PP2V5_S0_GPU_TPVDD	78C7
TRUE	PP2V5_S0_GPU_TXVDDR	78C7
TRUE	PP2V5_S0_GPU_AVDD	78C7
TRUE	PP2V5_S0_GPU_A2VDD	78B7
TRUE	PP2V5_S0_GPU_LPVDD	78B7 66B6 67A2 67B3 67C3 67C5 71D2 79A8 79D3
TRUE	PP2V5_S0_GPU_LVDDR	78B7 26B4 26B6 26B8 26D1 27C3 27D3 29A4 29B4 29C3 29D4
TRUE	PP3V3_S0	29A4 29B4 (=PP3V3_S0_CK410)
TRUE	PP3V3_S0_CK410_VDD48	19C7 19D6 19C6 19C7 19C7 21C3 21D3 22B5 23B3 23D5
TRUE	PP3V3_S0_CK410_VDD_PCI	27B8 27C6 65C2 65C3 65D2 49B5 49C4 49C7 52D3 54B5
TRUE	PP3V3_S0_CK410_VDD_REF	62A6 65B1 65D6 66B1 66B5 82A4 82B3 82C6 82D5
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC	33C5
TRUE	PP3V3_S0_CK410_VDDA	
TRUE	PP3V3_FWPHY	6C3 6C5 6C6 38B5 38D7 42C4 43B8 44A8 44B8
TRUE	PP3V3_FWPHY_AVDD	38D5
TRUE	PP3V3_FWPHY_PLLVDD	38C6
TRUE	PP1V95_FWPHY	6C3 6C5 6C6 38B2 38D5 42C1
TRUE	PP1V95_FWPHY_PLLVDD	38D3
TRUE	PP1V2_S3	5D4 39A8 (=PP1V2_S3_ENET) 39D7 63B3 67D6 67D8
TRUE	PP3V3_S3AC	39A5 39B4 (=PP3V3_S3_ENET) 39B5 39B8 39D6 39D8 42C4 67D1 67D3
TRUE	PP2V5_S3	39D3 63C3 (=PP2V5_S3_ENET) 63D3 63D4 67B6 67B8
TRUE	PP2V5_S3_ENET_AVDD	39D5 40D5

Request for at least 10 GND TPs

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	71A4 78B8 80A1 80B5 81B3 5D3 5D4 25D8 31C5 36D6 53C4 55A8 57B5 60B5 67A1 67B1 67B3
TRUE	FAN_LT_PWM	19D7 21C1 24C3 24D3 25C4 58B6
TRUE	FAN_LT_TACH	58B6
TRUE	FAN_RT_PWM	19D7 62A7 67B6 67C6 67C8 58B3
TRUE	FAN_RT_TACH	58B3

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	66D2 67D3 67D5 68B8 69A8 69B8 69C8 81D4 26D6 27C3 35B7 47B5 51C2 51D3 51D4 53B1 52B5 52B7
TRUE	PP5V_S0	67B3 71A6 78B6 80A1 80B5 81B3 52D7 53C4 66A8 66C8 52B2 66D4 25D8 31C5 36D6 53C4 55A8 57B5 60B5 67A1 67B1 67B3
TRUE	LPC_AD<0>	21D4 51D7 53C4 60C6
TRUE	LPC_AD<1>	21D4 51D7 53C4 60C6
TRUE	LPC_FRAME_L	21C5 51C7 53C4 60C6
TRUE	PM_CLKRUN_L	23C8 51C5 53C4 60C6
TRUE	BOOT_LPC_SPI_L	22B3 51C7 53B4
TRUE	SMC_TMS	51B5 52B2 53B4
TRUE	DEBUG_RST_L	26B1 53B4
TRUE	SMC_TRST_L	51C1 53B4
TRUE	SMC_TDO	51B5 52B2 53B4
TRUE	SMC_MD1	51C1 53B4
TRUE	SMC_TX_L	47B5 51C7 52B2 52B3 53B4
TRUE	FWH_INIT_L	21C4 51D5 52D3 52D5
TRUE	PCI_CLK_PORT80_LPC	34D6 53C5
TRUE	LPC_AD<2>	21D4 51C7 53C5 60C6
TRUE	LPC_AD<3>	21D4 51C7 53C5 60C6
TRUE	INT_SERIRQ	23C8 51C7 53C5 60C6
TRUE	PM_SUS_STAT_L	23C5 51C5 52A2 53B5 60C6
TRUE	SMC_TDI	51B5 52B2 53B5
TRUE	SMC_TCK	51C5 52B2 53B5
TRUE	SMC_RST_L	51C3 52D6 53B5
TRUE	SMC_NMI	51C1 53B5
TRUE	SMC_RX_L	47B5 51C7 52B2 52B3 53B5
TRUE	SV_SET_UP	23B6 23C3 53B5

Resistor Calibration

FUNC_TEST		
TRUE	PP5V_S0_ISENSECAL	67D8 67E8 55A4 65A2 67D6 25C4 25D3 34B8 34C6 19D7 21C1 24C3 24D3 25C4
TRUE	PP1V8_S3	19D1 19D2 19D5 19D6 19D7 19D3 19D4 19D5 19D6
TRUE	PP1V05_S0	9D4 78G 78H 79F 9B7 11B3 11C5 12A7
TRUE	PPVCORE_S0_CPU	8B5 8D7 9D7 55A6 55D7 61D1 67D1 67D3
TRUE	PPVCORE_D3C_GPU	55A5 55C7 67A6 67A8 71B7 71C1 72D8 77A7
TRUE	ISENSE_CAL_EN	51B7 55A8
TRUE	GND	

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TRUE	PP5V_S3	5D4 45C8 52B8 62A2 67B1 67B3 81C4 81C6
TRUE	USB2_CAMERA_N	6D1 6D2 6D3 22C2 45C3
TRUE	USB2_CAMERA_P	6D1 6D2 6D3 22C2 45B3
TP260	PP5V_S3_CAMERA_F	45C5

Inverter Connector

TP270	GND_CHASSIS_INVERTER	5B2 6A6 6A8 45B5 45C5 79A5 79A6
TP270	PPBUS_S0_INVERTER	79B5
TP270	PP5V_INVERTER_SW	79B5
TP270	INVERTER_PWM	79A5
TP270	GND_CHASSIS_INVERTER	5B2 6A6 6A8 45B5 45C5 79A5 79A6

Thermal Sensors

FUNC_TEST		
TH73	HSTHMSNS_DX_P	54C5
TH74	HSTHMSNS_DX_N	54C5
TH72	RSFSTHMSNS_D_P	54D5
TH75	RSFSTHMSNS_D_N	54C5

SMC TPs

FUNC_TEST		
TP277	PM_SYSRST_L	23C5 26C5 51B7
TP276	SMC_ONOFF_L	51C5 52B2 52C6 81C4

Battery Connector

FUNC_TEST		
J190	BATT_POS	68A1 68A2 69B1
J190	BATT_NEG	68B1 68B2
	SMC_BS_ALRT_L	51C5 52B2 68B2
	SMBUS_SMC_BSA_SCL	27C1 27C2 27C3 51B5 68B2
	SMBUS_SMC_BSA_SDA	27C1 27C2 27C3 51B5 68B2

Left I/O Data Connector

FUNC_TEST		
TP191	PP1V5_S0	62A8 62C1 66C5 66D6 66E3 66E6 52A3 24A5 24A6 24A8 24A5 52A4 8B7 9B7 24A3 24A5 24B5 25A6 25B2 25B4 48B6 67C6 67C8
J190	ALS_GAIN	6D5 48C4 51B5
J190	LTALS_OUT	48C3 57C7
J190	ACZ_SDATAIN<0>	21C7 48B3 87B4
J190	ACZ_SDATAOUT	21C7 48B3 87B4
J190	ACZ_BITCLK	21C7 48B3 87B4
J190	ACZ_RST_L	21C7 48B3 87B4
J190	EXCARD_OC_L	6C1 6C3 22C4 22D8 48C3 52B3
J190	LTUSB_OC_L	6D1 6D3 22C4 22D8 48C3
J190	LT2USB_OC_L	6C1 6C3 22C4 22D8 48C3
J190	PM_SLP_S3_LS5V	6A1 6A2 48C3 62B3 66C6 66C7
J190	PM_SLP_S4_L	5C4 6A1 6A2 22C3 47C7 48C3 51C5 66A6 66B8 48C3 51B7
J190	SYS_ONEWIRE	48C3 51B7 52A2
J190	MINI_CLKREQ_L	33B4 34A3 34A4 48C3
J190	SMC_EXCARD_CP	48C3 51B7 52A2
J190	EXCARD_CLKREQ_L	33B4 34A3 34A4 48C3
J190	SMC_EXCARD_PWR_EN	48C3 51B7
J190	LIO_PLT_RESET_L	26C1 48C3
J190	ACZ_SYNC	21C7 48B3 87B4
J190	USB2_LT_N	6D1 6D2 6D3 22C2 48C6
J190	USB2_LT_P	6D1 6D2 6D3 22C2 48C6
J190	USB2_EXCARD_N	6C1 6C2 6C3 22C2 48C6
J190	USB2_EXCARD_P	6C1 6C2 6C3 22C2 48C6
J190	PCIE_EXCARD_R2D_C_N	48B6 50C5 50C6
J190	PCIE_EXCARD_R2D_C_P	48B6 50C5 50C6
J190	PCIE_EXCARD_D2R_N	22D4 48B6 50B3 50B5 50B6
J190	PCIE_EXCARD_D2R_P	22D4 48B6 50C3 50C5 50C6
J190	PCIE_CLK100M_EXCARD_P	33B4 34C3 34C5 48B6
J190	PCIE_CLK100M_EXCARD_N	33B4 34B3 34B5 48B6
J190	USB2_LT2_N	6C1 6C2 6C3 22C2 48C6
J190	USB2_LT2_P	6C1 6C2 6C3 22C2 48C6
J190	PCIE_MINI_R2D_C_N	48C6 50C5 50C6
J190	PCIE_MINI_R2D_C_P	48C6 50C5 50C6
J190	PCIE_MINI_D2R_N	22D4 48C6 50C3 50C5 50C6
J190	PCIE_MINI_D2R_P	22D4 48C6 50C3 50C5 50C6
J190	PCIE_CLK100M_MINI_P	33B4 34D4 34D5 48C6
J190	PCIE_CLK100M_MINI_N	33B4 34D4 34D5 48C6
J190	SMBUS_SB_SCL	46B6 48B3 81C3
J190	SMBUS_SB_SDA	28A6 29A6 33B6 47B6 47C6 47D6
J190	PCIE_WAKE_L	23C8 39C6 48C3
J190	SMC_BC_ACOK	48C3 51C5 52A2 48A8 48B3
J190	SMBUS_SMC_A_S3_SCL	27C3 27C5 27D5 27C6 48B6 51B5
J190	SMBUS_SMC_A_S3_SDA	27B3 27C3 27C5 27C6 48B6 51B5

Left I/O Power Connector

FUNC_TEST		
J190	PP18V5_DCIN	68B8 68C5
J190	PPBUS_G3H	61D7 62D7 64A6 65A6 65C6 67B4 67D4 67D6 68B5 69C1 71D7 79B7
	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NC_CPU_A32_L
NC_CPU_A33_L
NC_CPU_A34_L
NC_CPU_A35_L
NC_CPU_A36_L
NC_CPU_A37_L
NC_CPU_A38_L
NC_CPU_A39_L
NC_CPU_APM0_L
NC_CPU_APM1_L
NC_CPU_EXTBREF
NC_CPU_HFPLL
NC_CPU_SPARE0
NC_CPU_SPARE1
NC_CPU_SPARE2
NC_CPU_SPARE4

NC_MEM_A_A<15..14>
NC_MEM_B_A<15..14>
TP_NB_CFG<4..3>
TP_NB_CFG<6>
TP_NB_CFG<8>
TP_NB_CFG<11..10>
TP_NB_CFG<15..14>
TP_NB_CFG<17>

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12>
TP_SB_SUS_CLK

MEM_A_A<15..14>
MEM_B_A<15..14>
NB_CFG<4..3>
NB_CFG<6>
NB_CFG<8>
NB_CFG<11..10>
NB_CFG<15..14>
NB_CFG<17>
NB_CFG<13..12>
TP_SB_SUS_CLK

Inverter PWM Reset Alias

PLT_RST_L

R0600

ALS_GAIN — 0 — RTALS_GAIN

RTALS_GAIN

NC_ENET_CTRL12
NC_ENET_CTRL25

Ethernet Powr Management Support

ENET_LOWPWR_EN

R0690

SB_GPIO30 — 0 — ENET_LOWPWR_EN

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

FireWire Aliases

PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF

PP3V3_FWPHY
PP1V95_FWPHY

SMC_RSTGATE_L
=FW_PCI_IDSEL
PCI_GNT3_L
PCI_REQ3_L

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P
USB2_RT_N
RTUSB_OC_L

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P
USB_TRACKPAD_N
UNUSED_USB_B_OC_L

USB Port "C" = Left USB 2.0 Port

USB2_LT_P
USB2_LT_N
LTUSB_OC_L

USB Port "D" = Camera

USB2_CAMERA_P
USB2_CAMERA_N
UNUSED_USB_D_OC_L

USB Port "E" = ExpressCard

USB2_EXCARD_P
USB2_EXCARD_N
EXCARD_OC_L

USB Port "F" = USB 1.1 Hub

USB_HUB_P
USB_HUB_N

USB Port "G" = Bluetooth (M13P)

USB_BT_P
USB_BT_N

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P
USB2_LT2_N
LT2USB_OC_L

TP_USB2_3G_P
TP_USB2_3G_N

LVDS Pull Down Aliases

=LVDS_PD_L_CLK_N
=LVDS_PD_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_U_CLK_N
=LVDS_PD_U_CLK_P

LVDS_L_DATA_P<1>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_L_DATA_N<2>
LVDS_L_DATA_P<2>
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_P<2>
LVDS_U_DATA_N<2>
LVDS_U_CLK_N
LVDS_U_CLK_P

Base net is PM_SLP_S3_LS5V

PM_SLP_S4_L

Base net is PM_SLP_S4_L

PM_SLP_S3_LS5V

Chassis connection to be made at the fan cutout near the right ALS. Not stuffed at Proto.

NO STUFF
SH0601 EMI-SPRING 0G-502620M
GND_CHASSIS_FANFRAME
NO STUFF R0601 0 5% 1/10W MF-LF 402

Chassis connection to be made at the mounting hole northwest of the DVI connector. Plated hole.

ZT0600 195R106
GND_CHASSIS_DVI_TOP
C0600 0.01UF 10% 50V X7R 402
GND_CHASSIS_DVI_TOP
GND_CHASSIS_DVI_TOP
GND

Chassis connection to be made on FW shell

ZT0603 HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
NO STUFF R0602 0 5% 1/10W MF-LF 402
GND_CHASSIS_DVI_BOT

ZT0604 HOLE-VIA-P5RP25
GND_CHASSIS_ENET
GND_CHASSIS_ENET
GND_CHASSIS_ENET
GND_CHASSIS_ENET

Chassis connection to be made at the mounting hole southwest of the USB connector. Plated hole.

ZT0601 195R106
GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
C0602 0.01UF 10% 50V X7R 402
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS

SH0600 OG-503040 SHLD-SM-LF
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER
GND_CHASSIS_INVERTER

LEFT CLUTCH BARREL CABLING

Thermal Module Holes

Add one through via per hole to GND or 2 blind vias per side per hole to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Lower Left GPU TM Hole

Frame holes

ZT0612 HOLE-VIA-P5RP25 GND_CHASSIS_LIOFLEX_HOLE
C0612 0.01UF 10% 50V X7R 402
C0613 0.01UF 10% 50V X7R 402

ZT0613 HOLE-VIA-P5RP25 GND_CHASSIS_ODD_HOLE
C0610 0.01UF 10% 50V X7R 402
C0611 0.01UF 10% 50V X7R 402

ZT0611 HOLE-VIA-P5RP25 GND_CHASSIS_BATTCONN_HOLE
GND_CHASSIS_BATTCONN_HOLE
C0619 0.01UF 10% 50V X7R 402
C0614 0.01UF 10% 50V X7R 402

ZT0610 HOLE-VIA-P5RP25 GND_CHASSIS_LNDACARD_HOLE
C0615 0.01UF 10% 50V X7R 402
C0616 0.01UF 10% 50V X7R 402

ZT0614 HOLE-VIA-P5RP25 GND_CHASSIS_LEFT_DIMM_HOLE
C0617 0.01UF 10% 50V X7R 402
C0618 0.01UF 10% 50V X7R 402

Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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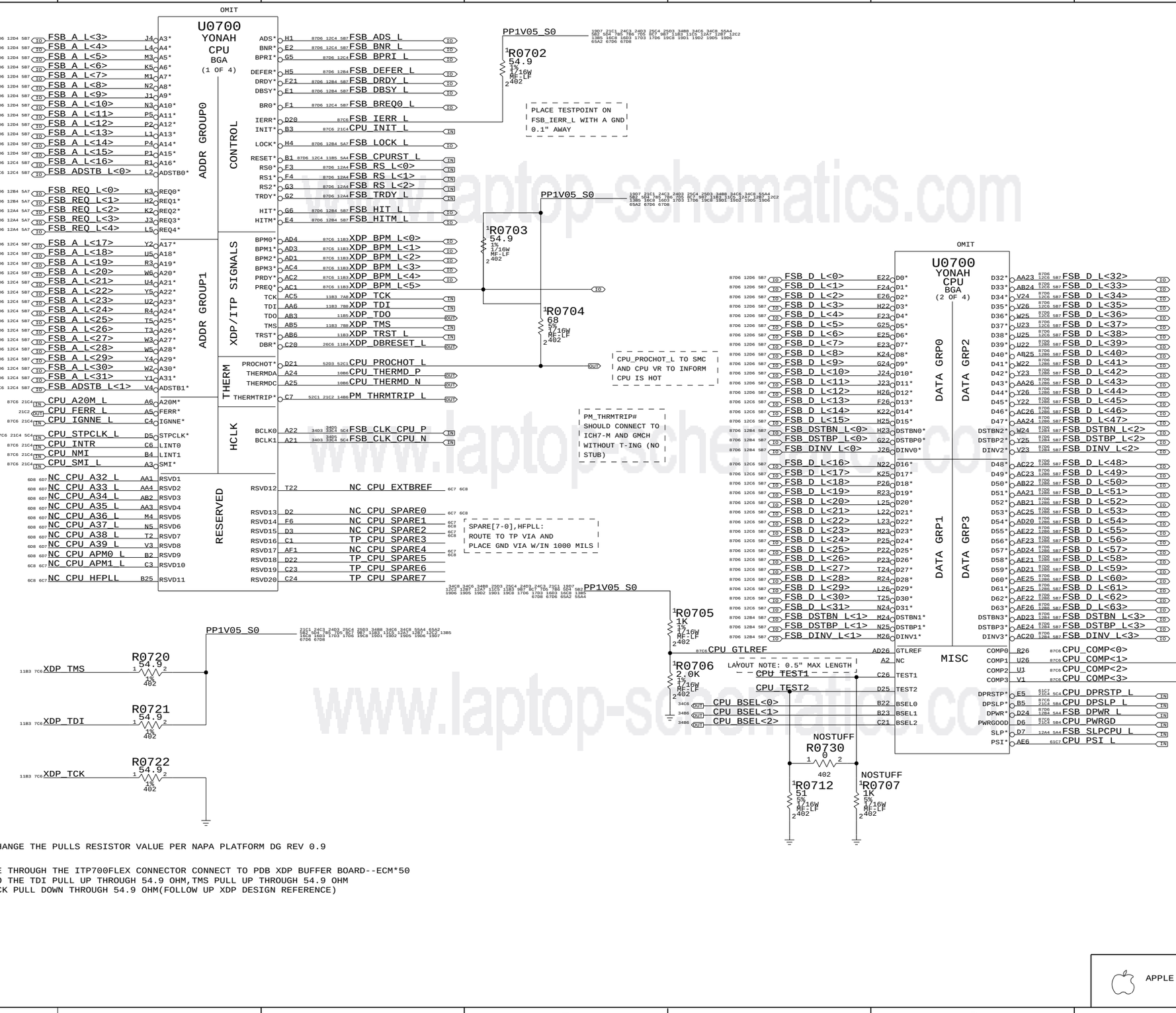

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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PPVCORE_S0_CPU 5B2 8B5 9D7 55A6 55D7 61D1 67D1 67D3
(CPU CORE POWER)

OMIT

U0700 YONAH CPU BGA (3 OF 4)

A7	VCC_1	VCC_68	AB20
A9	VCC_2	VCC_69	AB7
A10	VCC_3	VCC_70	AC7
A12	VCC_4	VCC_71	AC9
A13	VCC_5	VCC_72	AC12
A15	VCC_6	VCC_73	AC13
A17	VCC_7	VCC_74	AC15
A18	VCC_8	VCC_75	AC17
A20	VCC_9	VCC_76	AC18
B7	VCC_10	VCC_77	AD7
B9	VCC_11	VCC_78	AD9
B10	VCC_12	VCC_79	AD10
B12	VCC_13	VCC_80	AD12
B14	VCC_14	VCC_81	AD14
B15	VCC_15	VCC_82	AD15
B17	VCC_16	VCC_83	AD17
B18	VCC_17	VCC_84	AD18
B20	VCC_18	VCC_85	AE9
C9	VCC_19	VCC_86	AE10
C10	VCC_20	VCC_87	AE12
C12	VCC_21	VCC_88	AE13
C13	VCC_22	VCC_89	AE15
C15	VCC_23	VCC_90	AE17
C17	VCC_24	VCC_91	AE18
C18	VCC_25	VCC_92	AE20
D9	VCC_26	VCC_93	AF9
D10	VCC_27	VCC_94	AF10
D12	VCC_28	VCC_95	AF12
D14	VCC_29	VCC_96	AF14
D15	VCC_30	VCC_97	AF15
D17	VCC_31	VCC_98	AF17
D18	VCC_32	VCC_99	AF18
E7	VCC_33	VCC_100	AF20
E9	VCC_34		
E10	VCC_35	VCCP_1	V6
E12	VCC_36	VCCP_2	G21
E13	VCC_37	VCCP_3	J6
E15	VCC_38	VCCP_4	K6
E17	VCC_39	VCCP_5	M6
E18	VCC_40	VCCP_6	J21
E20	VCC_41	VCCP_7	K21
F7	VCC_42	VCCP_8	M21
F9	VCC_43	VCCP_9	N21
F10	VCC_44	VCCP_10	N6
F12	VCC_45	VCCP_11	R21
F14	VCC_46	VCCP_12	R6
F15	VCC_47	VCCP_13	T21
F17	VCC_48	VCCP_14	T6
F18	VCC_49	VCCP_15	V21
F20	VCC_50	VCCP_16	W21
AA7	VCC_51		
AA9	VCC_52		
AA10	VCC_53		
AA12	VCC_54		
AA13	VCC_55		
AA15	VCC_56		
AA17	VCC_57		
AA18	VCC_58		
AA20	VCC_59		
AB9	VCC_60		
AC10	VCC_61		
AB10	VCC_62		
AB12	VCC_63		
AB14	VCC_64		
AB15	VCC_65		
AB17	VCC_66		
AB18	VCC_67		

PP1V05_S0 21C1 24C3 24D3 29C4 35D3 34B8 34C6 34C8 55A4 60A2 5B5 5C4 7B6 7B6 7D6 7D6 9B7 18B3 11C5 12A7 12B7 15C2 13B5 19C8 17D3 17D6 19C8 19D1 19D2 19D5 19D6 19D7 67D5 67D8
(CPU IO POWER 1.05V)

VCCA=1.5 ONLY

PP1V5_S0 67C6 67C8 67C8 66C5 66C6 66C8 4B6 5D1 5D4 9B7 14A3 24A5 24B5 49A8 28B5 26B6 29C2 29D5
(CPU INTERNAL PLL POWER 1.5V)

VCCA	B26		
VID0	AD6	CPU_VID<0>	OUT 9C2 87B6
VID1	AF5	CPU_VID<1>	OUT 9C2 87B6
VID2	AE5	CPU_VID<2>	OUT 9C2 87B6
VID3	AF4	CPU_VID<3>	OUT 9C2 87B6
VID4	AE3	CPU_VID<4>	OUT 9C2 87B6
VID5	AF2	CPU_VID<5>	OUT 9C2 87B6
VID6	AE2	CPU_VID<6>	OUT 9C2 87B6
VCCSENSE	AF7	CPU_VCCSENSE_P	OUT 61B1 87B6
VSSSENSE	AE7	CPU_VCCSENSE_N	OUT 61A1 87B6

VID FOR CPU POWER SUPPLY IF NO USE, NEED PULL-UP OR PULL-DOWN

PPVCORE_S0_CPU 5B2 8D7 9D7 55A6 55D7 61D1 67D1 67D3

R0802 100 1% 1/16W MF-LF 402

R0803 100 1% 1/16W MF-LF 402

LAYOUT NOTE: CONNECT R0803 TO TP_VSSSENSE WITH NO STUB.

LAYOUT NOTE: VCCSENSE AND VSSSENSE LINES SHOULD BE OF EQUAL LENGTH

LAYOUT NOTE: CPU_VCCSENSE_P/CPU_VCCSENSE_N USE ZO=27.4 OHM DIFFERNTIAL TRACE ROUTING.

LAYOUT NOTE: PROVIDE A TEST POINT (WITH NO STUB) TO CONNECT A DIFFERENCTIAL PROBE BETWEEN VCCSENSE AND VSSSENSE AT THE LOCATION WHERE THE TWO 54.9 OHM RESISTORS TERMINATE THE 55 OHM TRANSMISSION LINE

OMIT

U0700 YONAH CPU BGA (4 OF 4)

A4	VSS_1	VSS_82	P6
A8	VSS_2	VSS_83	P21
A11	VSS_3	VSS_84	P24
A14	VSS_4	VSS_85	R2
A16	VSS_5	VSS_86	R5
A19	VSS_6	VSS_87	R22
A23	VSS_7	VSS_88	R25
A26	VSS_8	VSS_89	T1
B6	VSS_9	VSS_90	T4
B8	VSS_10	VSS_91	T23
B11	VSS_11	VSS_92	T26
B13	VSS_12	VSS_93	U3
B16	VSS_13	VSS_94	U6
B19	VSS_14	VSS_95	U21
B21	VSS_15	VSS_96	U24
B24	VSS_16	VSS_97	V2
C5	VSS_17	VSS_98	V5
C8	VSS_18	VSS_99	V22
C11	VSS_19	VSS_100	V25
C14	VSS_20	VSS_101	W1
C16	VSS_21	VSS_102	W4
C19	VSS_22	VSS_103	W23
C2	VSS_23	VSS_104	W26
C22	VSS_24	VSS_105	Y3
C25	VSS_25	VSS_106	Y6
D1	VSS_26	VSS_107	Y21
D4	VSS_27	VSS_108	Y24
D8	VSS_28	VSS_109	AA2
D11	VSS_29	VSS_110	AA5
D13	VSS_30	VSS_111	AA8
D16	VSS_31	VSS_112	AA11
D19	VSS_32	VSS_113	AA14
D23	VSS_33	VSS_114	AA16
D26	VSS_34	VSS_115	AA19
E3	VSS_35	VSS_116	AA22
E6	VSS_36	VSS_117	AA25
E8	VSS_37	VSS_118	AB1
E11	VSS_38	VSS_119	AB4
E14	VSS_39	VSS_120	AB8
E16	VSS_40	VSS_121	AB11
E19	VSS_41	VSS_122	AB13
E21	VSS_42	VSS_123	AB16
E24	VSS_43	VSS_124	AB19
F5	VSS_44	VSS_125	AB23
F8	VSS_45	VSS_126	AB26
F11	VSS_46	VSS_127	AC3
F13	VSS_47	VSS_128	AC6
F16	VSS_48	VSS_129	AC8
F19	VSS_49	VSS_130	AC11
F2	VSS_50	VSS_131	AC14
F22	VSS_51	VSS_132	AC16
F25	VSS_52	VSS_133	AC19
G4	VSS_53	VSS_134	AC21
G1	VSS_54	VSS_135	AC24
G23	VSS_55	VSS_136	AD2
G26	VSS_56	VSS_137	AD5
H3	VSS_57	VSS_138	AD8
H6	VSS_58	VSS_139	AD11
H21	VSS_59	VSS_140	AD13
H24	VSS_60	VSS_141	AD16
J2	VSS_61	VSS_142	AD19
J5	VSS_62	VSS_143	AD22
J22	VSS_63	VSS_144	AD25
J25	VSS_64	VSS_145	AE1
K1	VSS_65	VSS_146	AE4
K4	VSS_66	VSS_147	AE8
K23	VSS_67	VSS_148	AE11
K26	VSS_68	VSS_149	AE14
L3	VSS_69	VSS_150	AE16
L6	VSS_70	VSS_151	AE19
L21	VSS_71	VSS_152	AE23
L24	VSS_72	VSS_153	AE26
M2	VSS_73	VSS_154	AF3
M5	VSS_74	VSS_155	AF6
M22	VSS_75	VSS_156	AF8
M25	VSS_76	VSS_157	AF11
N1	VSS_77	VSS_158	AF13
N4	VSS_78	VSS_159	AF16
N23	VSS_79	VSS_160	AF19
N26	VSS_80	VSS_161	AF21
P3	VSS_81	VSS_162	AF24

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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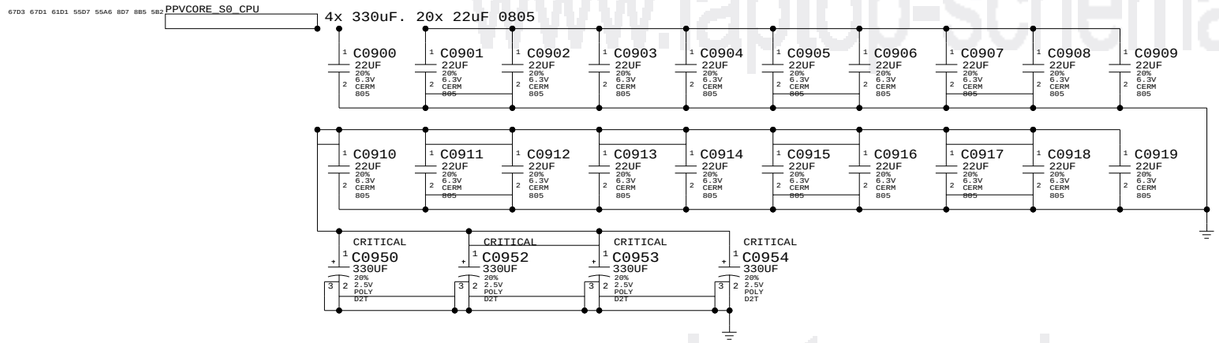
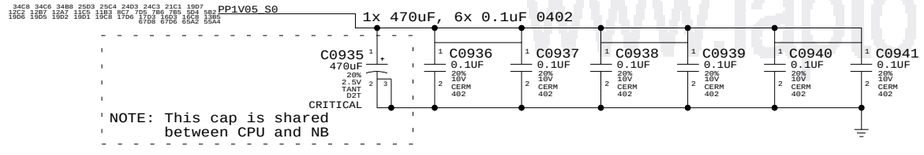
CPU VCORE HF AND BULK DECOUPLING



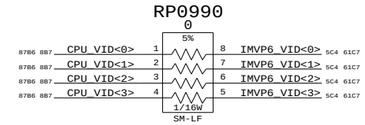
VCCA (CPU AVdd) Decoupling

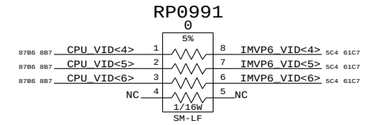
VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production





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CPU Decoupling & VID

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D	051-7164	03001

SCALE	SHT	OF
NONE	9	87

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

67C3 67B3 67A3 66B6 66B5 66B1 65D6 65B3
54B5 26B8 26B6 26B4 25D8 25D5 25C6 25C4 25B8
26D1 26B8 26B6 26B4 25D8 25D5 25C6 25C4 25B8
21C3 20B4 20A4 19C7 19C6 17C6 14D6 14C7 5D4 5A4
25B4 25B3 24D3 24C3 24B5 24B3 23D5 23B3 23B5 23D3
24A5 23A5 23A3 22B6 22B5 22B3 22A5 22A3 22B3 22D3
62A6 61D8 61A5 60D4 60C7 58C7 58C4 57B6 54D4
82D5 82C6 82B3 82A4 79D3 79A8 71D2 67C5

PP3V3_S0

C1002 0.1UF 10% 16V X5R 402

R1006 10K 5% 1/16W MF-LF 402

R1005 10K 5% 1/16W MF-LF 402

R1001 499 1% 1/16W MF-LF 402

R1002 499 1% 1/16W MF-LF 402

C1001 0.001UF 10% 50V CERM 402

7C6 OUT CPU_THERMD_P

7C6 IN CPU_THERMD_N

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

THRM_CPU_DX_P
THRM_CPU_DX_N

U1001
TMP401
MSOP
CRITICAL

VDD
GND
D+
D-
ALERT*/THM2*
THM*
SCLK
SDATA

THRM_ALERT_L
THRM_ALERT

51B5 49B5 27D3 27D2 27D1 SMBUS_SMC_B_S0_SCL TO

51B5 49B5 27D3 27D2 27D1 SMBUS_SMC_B_S0_SDA TO

PLACE U1001 NEAR THE U1200

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CPU MISC1-TEMP SENSOR

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NONE	10	87

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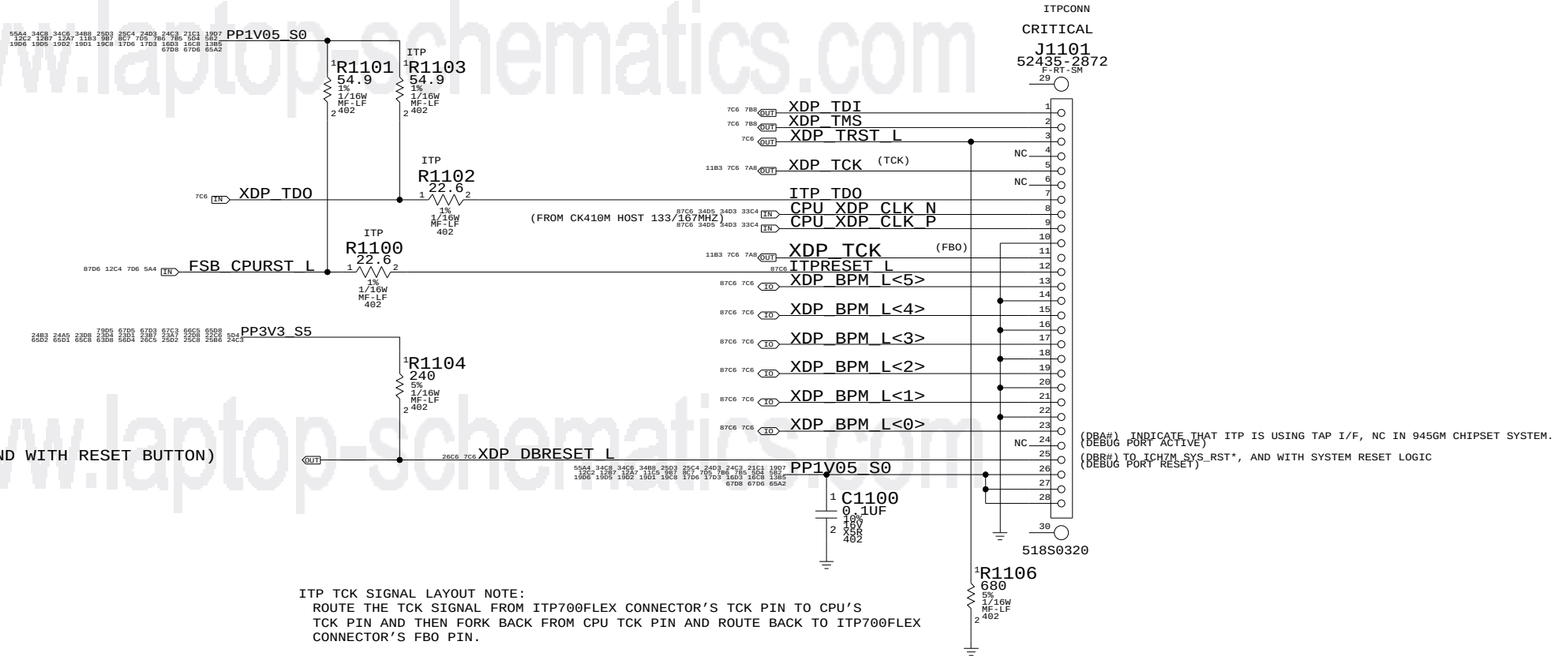
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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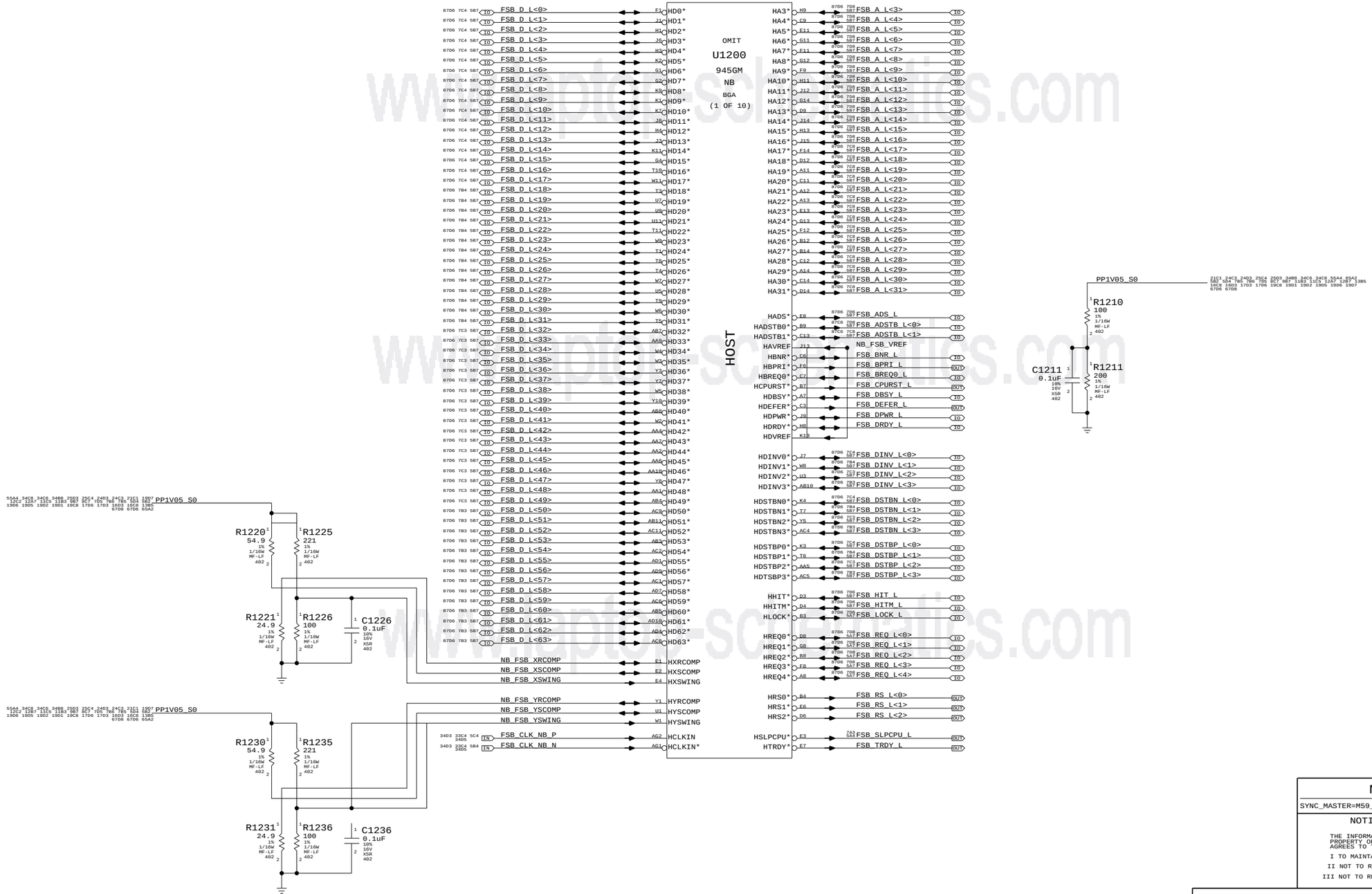

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NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

PP1V5_S0_NB

R1310 24.9 1% 1/16W MF-LF 402

OMIT

U1200
945GM
NB
BGA
(3 OF 10)

LVDS

LVDS_BKLTCTL	D32	L_BKLTCTL	
LVDS_BKLTEN	J30	L_BKLTEN	
TP_LVDS_CLKCTLA	H30	L_CLKCTLA	
TP_LVDS_CLKCTLB	H29	L_CLKCTLB	
LVDS_CONN_DDC_CLK	G26	L_DDC_CLK	
LVDS_CONN_DDC_DATA	G25	L_DDC_DATA	
LVDS_IBG	B38	L_IBG	
TP_LVDS_VBG	C35	L_VBG	
LVDS_VDDEN	F32	L_VDDEN	
GND	C33	L_VREFH	
GND	C32	L_VREFL	
LVDS_A_CLK_N	A33	LA_CLK*	
LVDS_A_CLK_P	A32	LA_CLK	
LVDS_B_CLK_N	E27	LB_CLK*	
LVDS_B_CLK_P	E26	LB_CLK	
LVDS_A_DATA_N<0>	C37	LA_DATA0*	
LVDS_A_DATA_N<1>	B35	LA_DATA1*	
LVDS_A_DATA_N<2>	A37	LA_DATA2*	
LVDS_A_DATA_P<0>	B37	LA_DATA0	
LVDS_A_DATA_P<1>	B34	LA_DATA1	
LVDS_A_DATA_P<2>	A36	LA_DATA2	
LVDS_B_DATA_N<0>	G30	LB_DATA0*	
LVDS_B_DATA_N<1>	D30	LB_DATA1*	
LVDS_B_DATA_N<2>	F29	LB_DATA2*	
LVDS_B_DATA_P<0>	F30	LB_DATA0	
LVDS_B_DATA_P<1>	D29	LB_DATA1	
LVDS_B_DATA_P<2>	F28	LB_DATA2	

TV

PP1V5_S0_NB	A16	TV_DACA_OUT
PP1V5_S0_NB	C18	TV_DACB_OUT
PP1V5_S0_NB	A19	TV_DACC_OUT
PP1V5_S0_NB	J20	TV_IREF
PP1V5_S0_NB	B16	TV_IRTNA
PP1V5_S0_NB	B18	TV_IRTNB
PP1V5_S0_NB	B19	TV_IRTNC

VGA

PP1V05_S0	F23	CRT_BLUE
PP1V05_S0	D23	CRT_BLUE*
PP1V05_S0	C22	CRT_GREEN
PP1V05_S0	B22	CRT_GREEN*
PP1V05_S0	A21	CRT_RED
PP1V05_S0	B21	CRT_RED*
TP_CRT_DDC_CLK	C26	CRT_DDC_CLK
TP_CRT_DDC_DATA	C25	CRT_DDC_DATA
GND	G23	HSYNC
PP1V05_S0	J22	CRT_IREF
GND	H23	CRT_VSYNC

PCI-EXPRESS GRAPHICS

EXP_A_COMPI	D40	PEG_COMP	
EXP_A_COMPO	D38		
EXP_A_RXN0	F34	PEG_D2R_N<0>	
EXP_A_RXN1	G38	PEG_D2R_N<1>	
EXP_A_RXN2	H34	PEG_D2R_N<2>	
EXP_A_RXN3	J38	PEG_D2R_N<3>	
EXP_A_RXN4	L34	PEG_D2R_N<4>	
EXP_A_RXN5	M38	PEG_D2R_N<5>	
EXP_A_RXN6	N34	PEG_D2R_N<6>	
EXP_A_RXN7	P38	PEG_D2R_N<7>	
EXP_A_RXN8	R34	PEG_D2R_N<8>	
EXP_A_RXN9	T38	PEG_D2R_N<9>	
EXP_A_RXN10	V34	PEG_D2R_N<10>	
EXP_A_RXN11	W38	PEG_D2R_N<11>	
EXP_A_RXN12	Y34	PEG_D2R_N<12>	
EXP_A_RXN13	AA38	PEG_D2R_N<13>	
EXP_A_RXN14	AB34	PEG_D2R_N<14>	
EXP_A_RXN15	AC38	PEG_D2R_N<15>	
EXP_A_RXP0	D34	PEG_D2R_P<0>	
EXP_A_RXP1	F38	PEG_D2R_P<1>	
EXP_A_RXP2	G34	PEG_D2R_P<2>	
EXP_A_RXP3	H38	PEG_D2R_P<3>	
EXP_A_RXP4	J34	PEG_D2R_P<4>	
EXP_A_RXP5	L38	PEG_D2R_P<5>	
EXP_A_RXP6	M34	PEG_D2R_P<6>	
EXP_A_RXP7	N38	PEG_D2R_P<7>	
EXP_A_RXP8	P34	PEG_D2R_P<8>	
EXP_A_RXP9	R38	PEG_D2R_P<9>	
EXP_A_RXP10	T34	PEG_D2R_P<10>	
EXP_A_RXP11	V38	PEG_D2R_P<11>	
EXP_A_RXP12	W34	PEG_D2R_P<12>	
EXP_A_RXP13	Y38	PEG_D2R_P<13>	
EXP_A_RXP14	AA34	PEG_D2R_P<14>	
EXP_A_RXP15	AB38	PEG_D2R_P<15>	
EXP_A_TXN0	F36	PEG_R2D_C_N<0>	SDVOB_RED#
EXP_A_TXN1	G40	PEG_R2D_C_N<1>	SDVOB_GREEN#
EXP_A_TXN2	H36	PEG_R2D_C_N<2>	SDVOB_BLUE#
EXP_A_TXN3	J40	PEG_R2D_C_N<3>	SDVOB_CLKN
EXP_A_TXN4	L36	PEG_R2D_C_N<4>	SDVOC_RED#
EXP_A_TXN5	M40	PEG_R2D_C_N<5>	SDVOC_GREEN#
EXP_A_TXN6	N36	PEG_R2D_C_N<6>	SDVOC_BLUE#
EXP_A_TXN7	P40	PEG_R2D_C_N<7>	SDVOC_CLKN
EXP_A_TXN8	R36	PEG_R2D_C_N<8>	
EXP_A_TXN9	T40	PEG_R2D_C_N<9>	
EXP_A_TXN10	V36	PEG_R2D_C_N<10>	
EXP_A_TXN11	W40	PEG_R2D_C_N<11>	
EXP_A_TXN12	Y36	PEG_R2D_C_N<12>	
EXP_A_TXN13	AA40	PEG_R2D_C_N<13>	
EXP_A_TXN14	AB36	PEG_R2D_C_N<14>	
EXP_A_TXN15	AC40	PEG_R2D_C_N<15>	
EXP_A_TXP0	D36	PEG_R2D_C_P<0>	SDVOB_RED
EXP_A_TXP1	F40	PEG_R2D_C_P<1>	SDVOB_GREEN
EXP_A_TXP2	G36	PEG_R2D_C_P<2>	SDVOB_BLUE
EXP_A_TXP3	H40	PEG_R2D_C_P<3>	SDVOB_CLKP
EXP_A_TXP4	J36	PEG_R2D_C_P<4>	SDVOC_RED
EXP_A_TXP5	L40	PEG_R2D_C_P<5>	SDVOC_GREEN
EXP_A_TXP6	M36	PEG_R2D_C_P<6>	SDVOC_BLUE
EXP_A_TXP7	N40	PEG_R2D_C_P<7>	SDVOC_CLKP
EXP_A_TXP8	P36	PEG_R2D_C_P<8>	
EXP_A_TXP9	R40	PEG_R2D_C_P<9>	
EXP_A_TXP10	T36	PEG_R2D_C_P<10>	
EXP_A_TXP11	V40	PEG_R2D_C_P<11>	
EXP_A_TXP12	W36	PEG_R2D_C_P<12>	
EXP_A_TXP13	Y40	PEG_R2D_C_P<13>	
EXP_A_TXP14	AA36	PEG_R2D_C_P<14>	
EXP_A_TXP15	AB40	PEG_R2D_C_P<15>	

SDVO Alternate Function

SDVO_TVCLKIN#	
SDVO_INT#	
SDVO_FLDSTALL#	
SDVO_TVCLKIN	
SDVO_INT	
SDVO_FLDSTALL	

NB PEG / Video Interfaces

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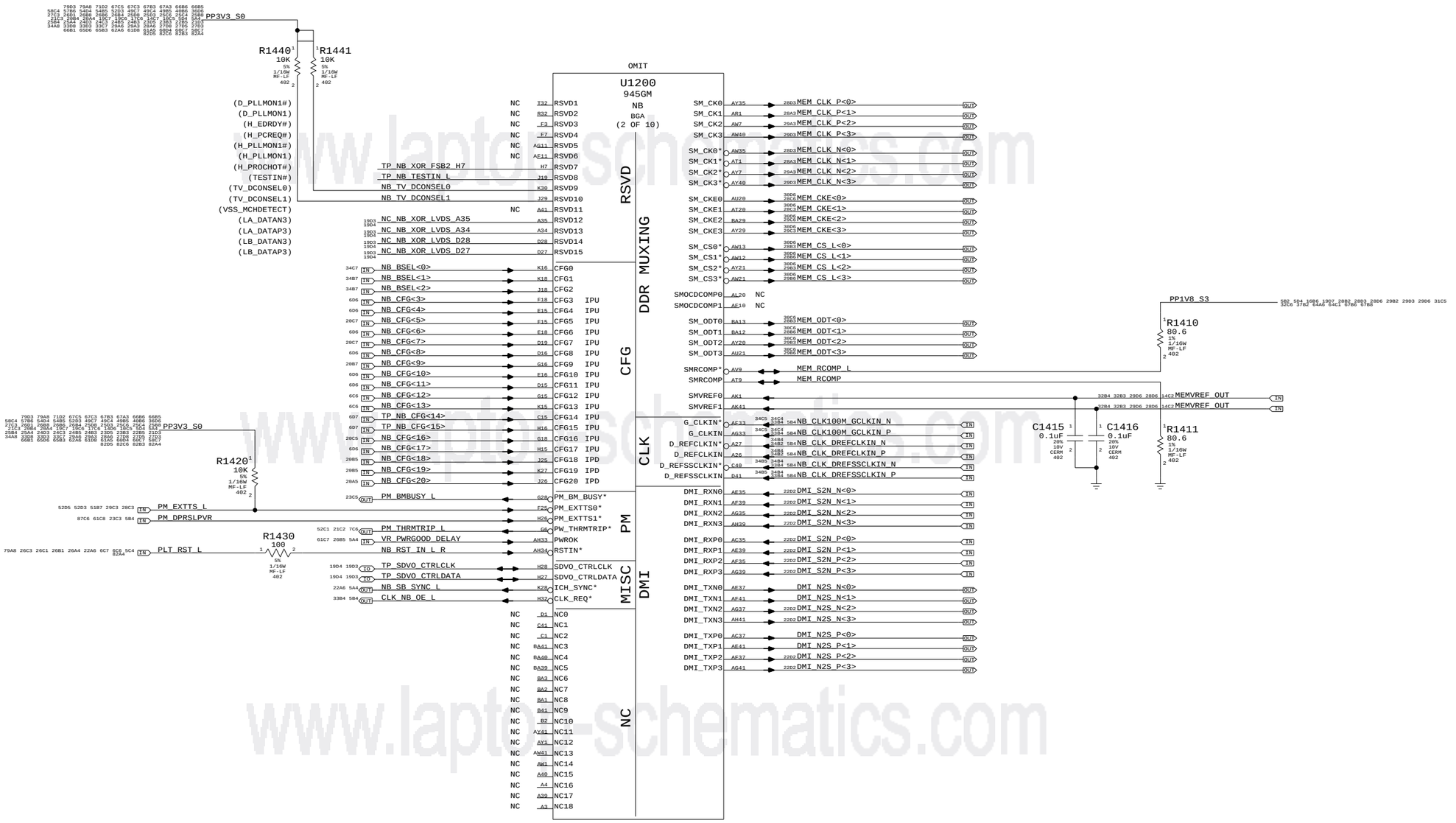

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NB Misc Interfaces

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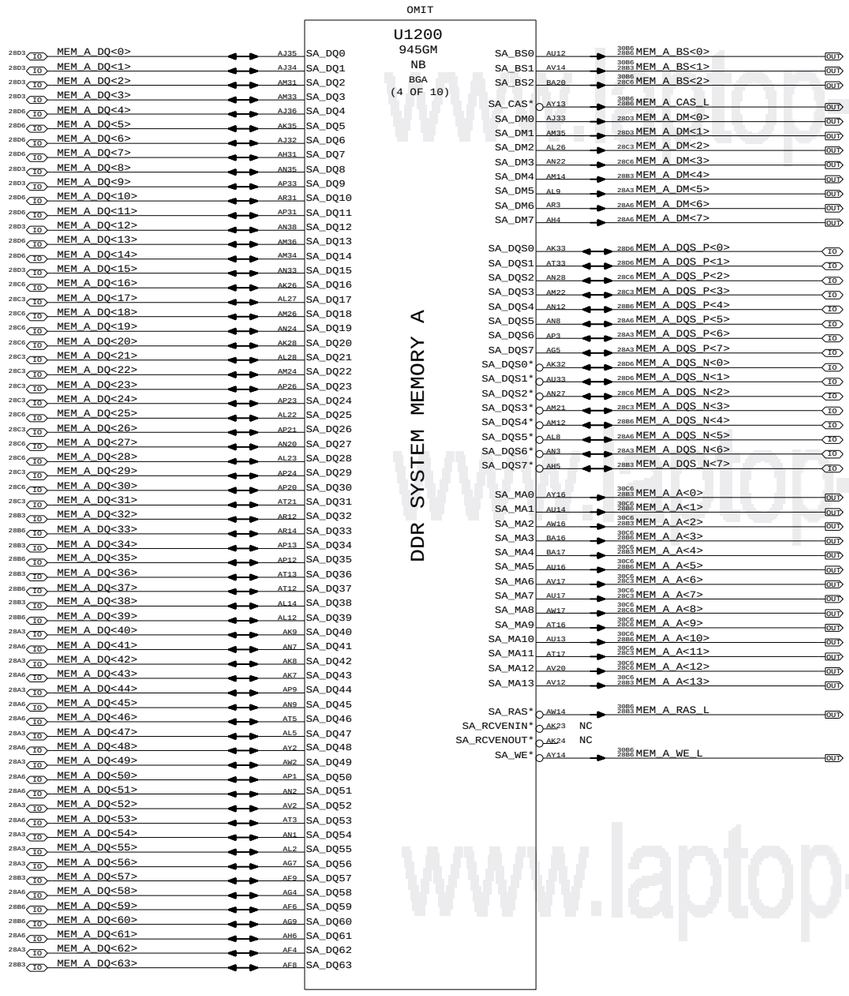

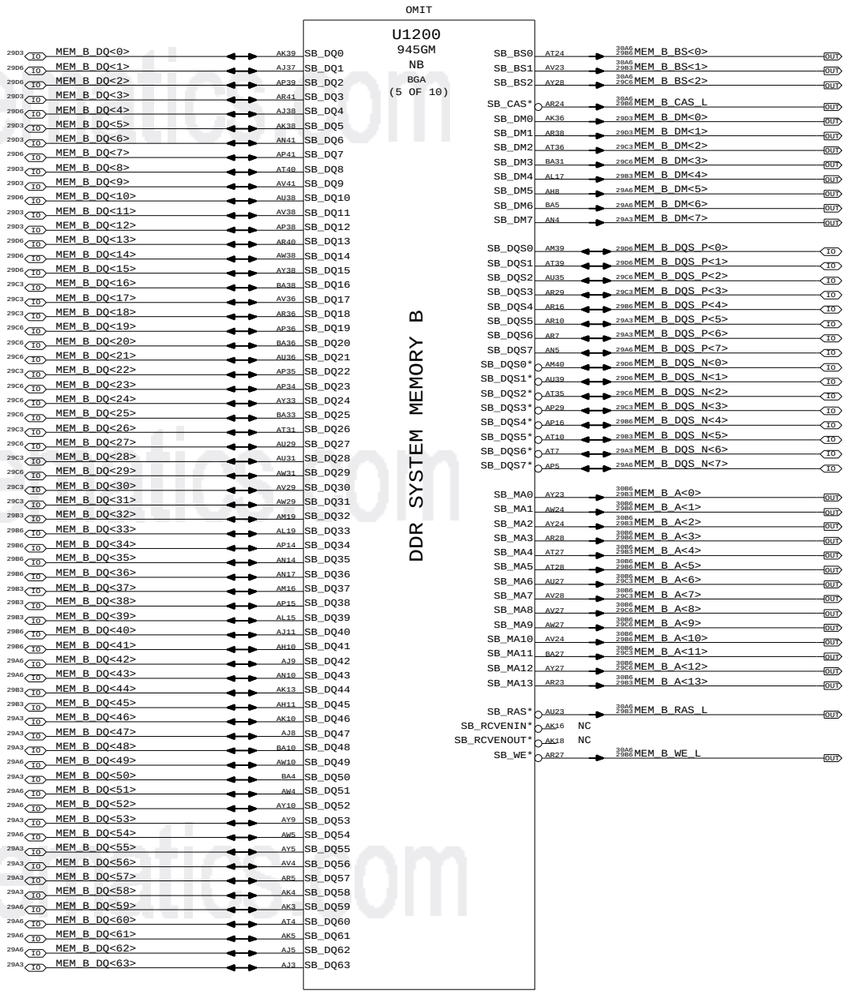

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NB DDR2 Interfaces

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NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

PP1V05_S0

1.05V or 1.5V

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.05V, Internal Graphics: 5500mA Max

U1200
945GM
NB
BGA
(6 OF 10)
OMIT
VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47UF 10% 6.3V CERM-X5R 402
C1613 0.47UF 10% 6.3V CERM-X5R 402

C1615 0.47UF 10% 6.3V CERM-X5R 402
Layout Note: Place near pin BA23

PP1V8_S3

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note: Place in cavity

C1610 0.47UF 10% 6.3V CERM-X5R 402
Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 0.47UF 10% 6.3V CERM-X5R 402
C1611 0.47UF 10% 6.3V CERM-X5R 402

PP1V05_S0

U1200
945GM
NB
BGA
(7 OF 10)
OMIT
NCTF

AD27	VCC_NCTF0	VSS_NCTF0	AE27
AC27	VCC_NCTF1	VSS_NCTF1	AE26
AB27	VCC_NCTF2	VSS_NCTF2	AE25
AA27	VCC_NCTF3	VSS_NCTF3	AE24
Y27	VCC_NCTF4	VSS_NCTF4	AE23
W27	VCC_NCTF5	VSS_NCTF5	AE22
V27	VCC_NCTF6	VSS_NCTF6	AE21
U27	VCC_NCTF7	VSS_NCTF7	AE20
T27	VCC_NCTF8	VSS_NCTF8	AE19
R27	VCC_NCTF9	VSS_NCTF9	AE18
AD26	VCC_NCTF10	VSS_NCTF10	AC17
AC26	VCC_NCTF11	VSS_NCTF11	Y17
AB26	VCC_NCTF12	VSS_NCTF12	U17
AA26	VCC_NCTF13		
Y26	VCC_NCTF14		
W26	VCC_NCTF15		
V26	VCC_NCTF16		
U26	VCC_NCTF17		
T26	VCC_NCTF18		
R26	VCC_NCTF19		
AD25	VCC_NCTF20		
AC25	VCC_NCTF21		
AB25	VCC_NCTF22		
AA25	VCC_NCTF23		
Y25	VCC_NCTF24		
W25	VCC_NCTF25		
V25	VCC_NCTF26		
U25	VCC_NCTF27		
T25	VCC_NCTF28		
R25	VCC_NCTF29		
AD24	VCC_NCTF30		
AC24	VCC_NCTF31		
AB24	VCC_NCTF32		
AA24	VCC_NCTF33		
Y24	VCC_NCTF34		
W24	VCC_NCTF35		
V24	VCC_NCTF36		
U24	VCC_NCTF37		
T24	VCC_NCTF38		
R24	VCC_NCTF39		
AD23	VCC_NCTF40		
Y23	VCC_NCTF41		
U23	VCC_NCTF42		
T23	VCC_NCTF43		
R23	VCC_NCTF44		
AD22	VCC_NCTF45		
V22	VCC_NCTF46		
U22	VCC_NCTF47		
T22	VCC_NCTF48		
R22	VCC_NCTF49		
AD21	VCC_NCTF50		
V21	VCC_NCTF51		
U21	VCC_NCTF52		
T21	VCC_NCTF53		
R21	VCC_NCTF54		
AD20	VCC_NCTF55		
V20	VCC_NCTF56		
U20	VCC_NCTF57		
T20	VCC_NCTF58		
R20	VCC_NCTF59		
AD19	VCC_NCTF60		
V19	VCC_NCTF61		
U19	VCC_NCTF62		
T19	VCC_NCTF63		
AD18	VCC_NCTF64		
AC18	VCC_NCTF65		
AB18	VCC_NCTF66		
AA18	VCC_NCTF67		
Y18	VCC_NCTF68		
W18	VCC_NCTF69		
V18	VCC_NCTF70		
U18	VCC_NCTF71		
T18	VCC_NCTF72		

PP1V5_S0_NB

		VCCAUX_NCTF0	AG27
		VCCAUX_NCTF1	AF27
		VCCAUX_NCTF2	AG26
		VCCAUX_NCTF3	AF26
		VCCAUX_NCTF4	AG25
		VCCAUX_NCTF5	AF25
		VCCAUX_NCTF6	AG24
		VCCAUX_NCTF7	AF24
		VCCAUX_NCTF8	AG23
		VCCAUX_NCTF9	AF23
		VCCAUX_NCTF10	AG22
		VCCAUX_NCTF11	AF22
		VCCAUX_NCTF12	AG21
		VCCAUX_NCTF13	AF21
		VCCAUX_NCTF14	AG20
		VCCAUX_NCTF15	AF20
		VCCAUX_NCTF16	AG19
		VCCAUX_NCTF17	AF19
		VCCAUX_NCTF18	R19
		VCCAUX_NCTF19	AG18
		VCCAUX_NCTF20	AF18
		VCCAUX_NCTF21	R18
		VCCAUX_NCTF22	AG17
		VCCAUX_NCTF23	AF17
		VCCAUX_NCTF24	AE17
		VCCAUX_NCTF25	AD17
		VCCAUX_NCTF26	AB17
		VCCAUX_NCTF27	AA17
		VCCAUX_NCTF28	W17
		VCCAUX_NCTF29	V17
		VCCAUX_NCTF30	T17
		VCCAUX_NCTF31	R17
		VCCAUX_NCTF32	AG16
		VCCAUX_NCTF33	AF16
		VCCAUX_NCTF34	AE16
		VCCAUX_NCTF35	AD16
		VCCAUX_NCTF36	AC16
		VCCAUX_NCTF37	AB16
		VCCAUX_NCTF38	AA16
		VCCAUX_NCTF39	Y16
		VCCAUX_NCTF40	W16
		VCCAUX_NCTF41	V16
		VCCAUX_NCTF42	U16
		VCCAUX_NCTF43	T16
		VCCAUX_NCTF44	R16
		VCCAUX_NCTF45	AG15
		VCCAUX_NCTF46	AF15
		VCCAUX_NCTF47	AE15
		VCCAUX_NCTF48	AD15
		VCCAUX_NCTF49	AC15
		VCCAUX_NCTF50	AB15
		VCCAUX_NCTF51	AA15
		VCCAUX_NCTF52	Y15
		VCCAUX_NCTF53	W15
		VCCAUX_NCTF54	V15
		VCCAUX_NCTF55	U15
		VCCAUX_NCTF56	T15
		VCCAUX_NCTF57	R15

NB Power 1

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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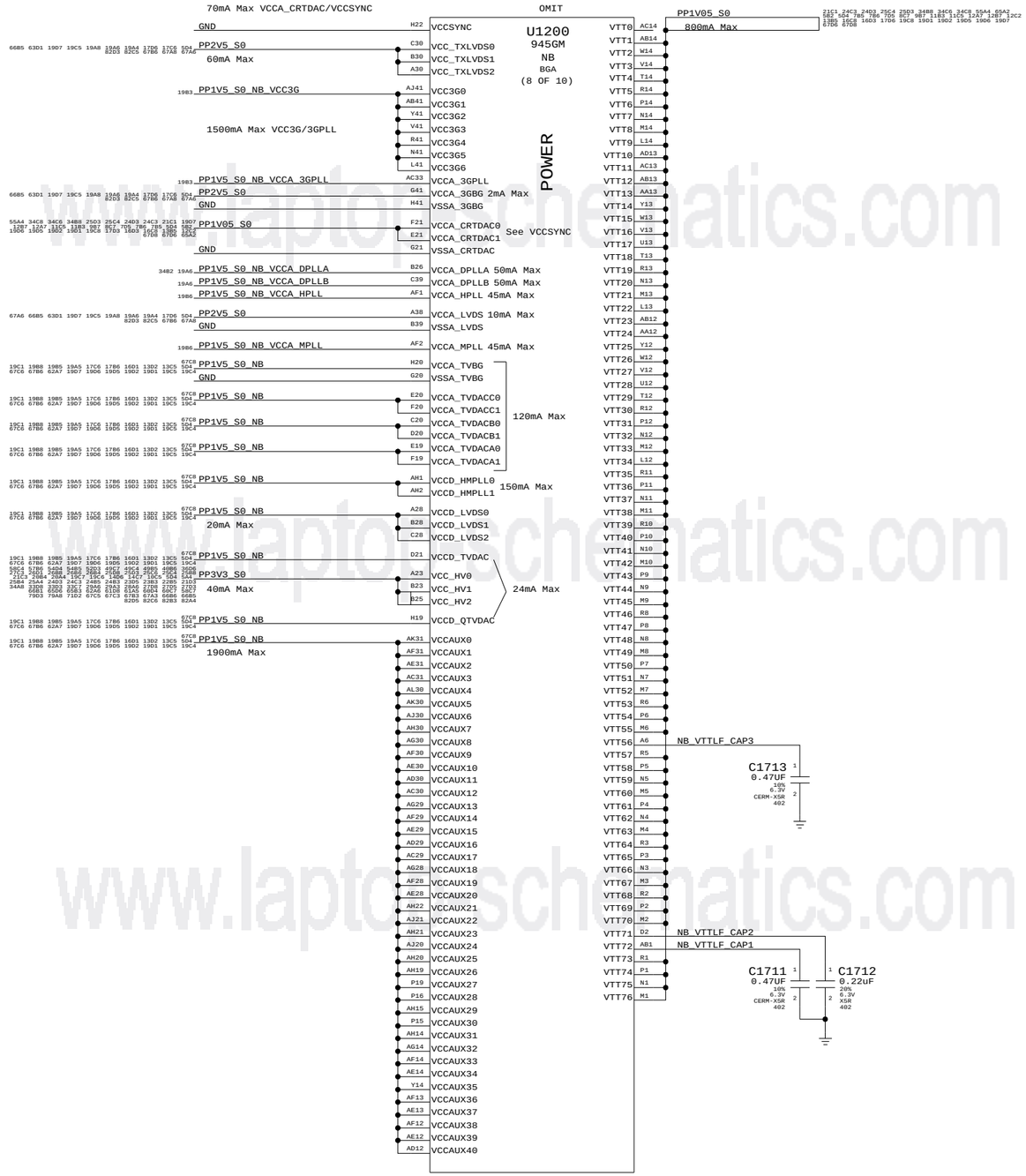
D	051-7164	03001

SCALE	SHT	OF
NONE	16	87



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NB Power 2

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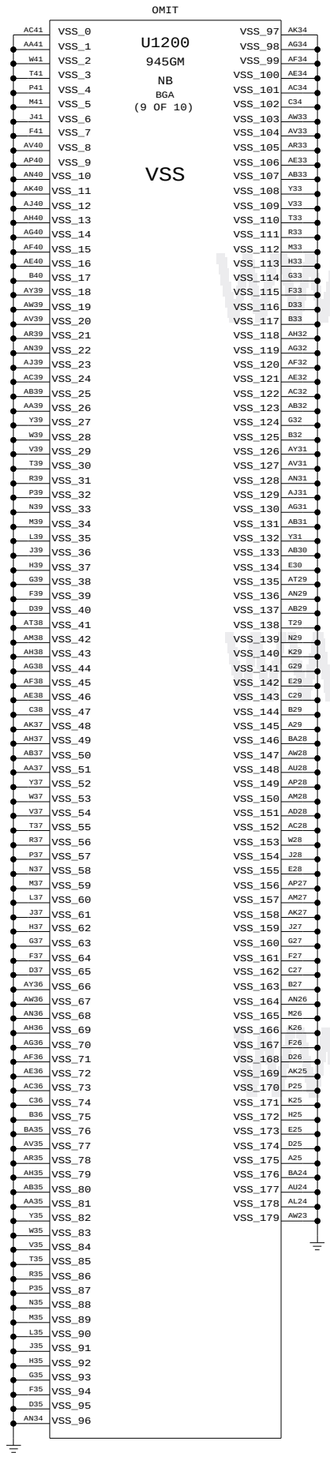
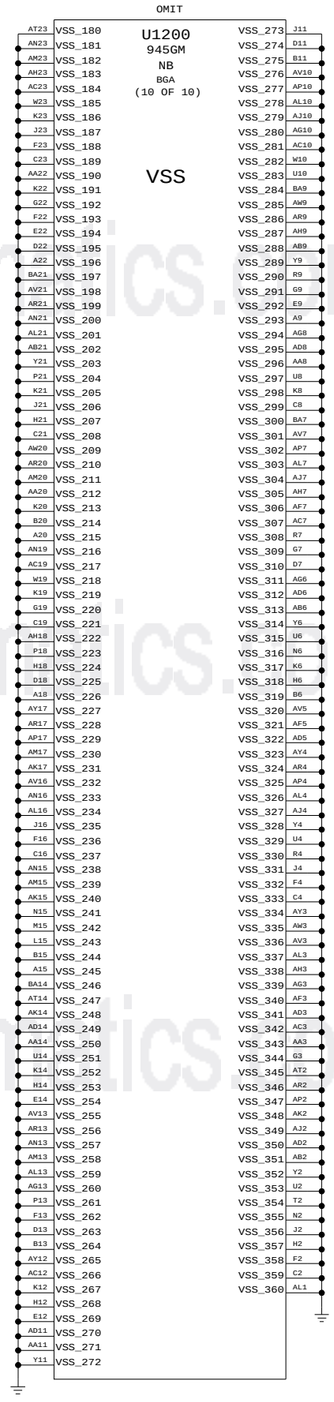
D	051-7164	03001
SCALE: NONE	SHT 17 OF 87	





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NB Grounds

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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SCALE: NONE	SHT 18 OF 87	

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?
PP1V05_S0
PP1V05_S0
PP1V05_S0
PP1V05_S0

3674mA Max
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB

3200mA Max
PP1V8_S3

132mA Max
GND
PP2V5_S0
PP2V5_S0

40mA Max?
PP3V3_S0
PP3V3_S0

1500mA Max
800mA Max
7mA Max
10mA Max?
7mA Max
1500mA Max
100mA Max
24mA Max
150mA Max
190mA Max
3200mA Max
70mA Max
7mA Max
60mA Max
2mA Max
7mA Max
40mA Max

PP1V05_S0
PP1V05_S0
PP1V05_S0
PP1V05_S0
PP1V05_S0
PP1V05_S0
GND
GND

TP_CRT_DDC_CLK
TP_CRT_DDC_DATA

PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB
PP1V5_S0_NB

TP_LVDS_CLKCTLA
TP_LVDS_CLKCTLB
NC_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK
TP_SDVO_CTRLDATA

LVDS IBG
R1990 1.5K 1% 1/16W MF-LF 402
GND
GND

PP1V5_S0_NB

(MCH CRTDAC ANALOG 2.5V PWR)
PP1V05_S0
GND

(MCH H/V SYNC 2.5V PWR)
GND

(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB

(MCH TV OUT CHANNEL A 3.3V PWR)
PP1V5_S0_NB

(MCH TV OUT CHANNEL B 3.3V PWR)
PP1V5_S0_NB

(MCH TV OUT CHANNEL C 3.3V PWR)
PP1V5_S0_NB

(MCH TV DAC BAND GAP 3.3V PWR)
PP1V5_S0_NB
GND

PP1V5_S0 1500mA Max

GMCH CORE PWR 1.05V BYPASS
CRITICAL
C1900 470uF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

PP1V05_S0 800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

PP3V3_S0 40mA Max

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)
(SHARE C0940 470UF)
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

PP2V5_S0 2mA Max

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)
C1916 0.1uF 20% 10V CERM 402

PP1V5_S0_NB 1900mA Max

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
C1918 0.1uF 20% 10V CERM 402

PP1V5_S0_NB 100mA Max

L1934 FERR-120-OHM-0.2A 0603
C1934 22UF 20% 6.3V CERM 805
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

L1936 FERR-120-OHM-0.2A 0603
C1936 22UF 20% 6.3V CERM 805
C1937 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

1500mA Max

PP1V5_S0_NB

L1970 91nH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY CASE-B2
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

1500mA Max

L1975 1.0UH-220MA-0.12-OHM 0805
R1975 0 5% 1/16W MF-LF 402
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GND
Layout Note: Route to caps, then GND

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
Layout Note: 3GPLL 10uF cap should be placed in cavity

PP2V5_S0 1.05A Max

CRITICAL
U1900 TPS73115 SOT23-5
IN OUT EN NR/FB GND
TPS73115_NR
C1950 1uF 10% 6.3V CERM 402

PP1V5_S0_NB_DPLL
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603

NO STUFF
R1953 0 5% 1/16W MF-LF 402
R1954 0 5% 1/16W MF-LF 402
NO STUFF
C1953 0.1uF 20% 10V CERM 402
C1954 0.1uF 20% 10V CERM 402

GMCH VCCA_DPLLA FILTER
(CRT/TVOUT PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLA
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
50MA MAX

GMCH VCCA_DPLLB FILTER
(LVDS PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLB
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
50MA MAX

MCH VCC_TXLVDS BYPASS
(MCH LVDS TRANSMITTER 2.5V PWR)
PP2V5_S0
60MA MAX
C1990 4.7UF 20% 6.3V CERM 603
C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)
PP1V5_S0_NB
20MA MAX
C1992 10uF 20% 6.3V X5R 603
C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS
(MCH LVDS ANALOG 2.5V PWR)
PP2V5_S0
10MA MAX
C1994 0.01UF 20% 16V CERM 402
C1995 0.1uF 20% 10V CERM 402
GND
Layout Note: Route to caps, then GND

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NB (GM) Decoupling

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

PP3V3_S0
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

PP3V3_S0
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

PP3V3_S0
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

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SCALE	SHT	OF
NONE	20	87

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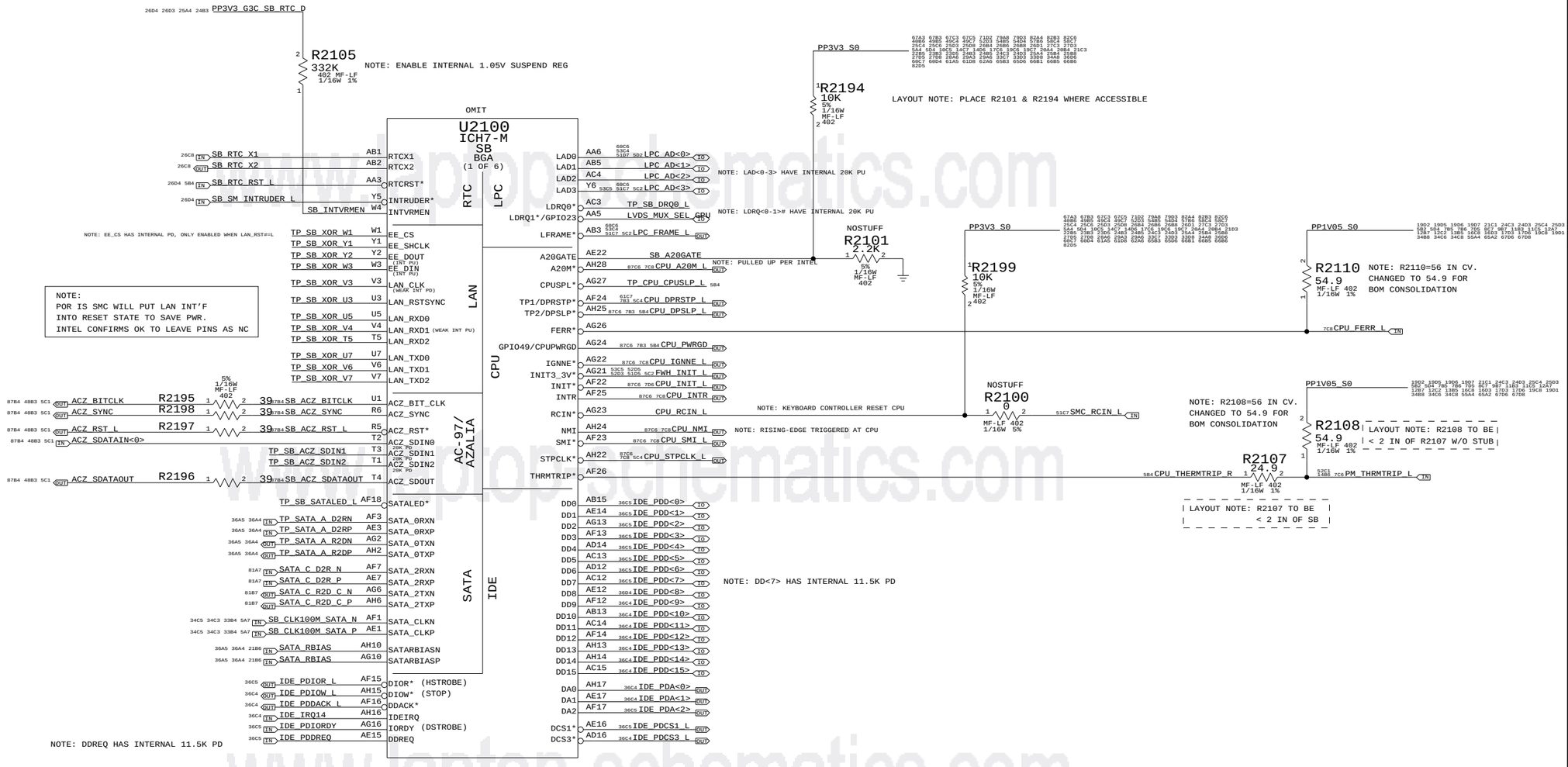

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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NONE	21	87

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PP3V3_S5

R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402 (USB_C_OC_PU)
R2255 10K 5% 1/16W MF-LF 402 (USB_D_OC_PU)
R2251 10K 5% 1/16W MF-LF 402 (USB_E_OC_PU)
R2223 10K 5% 1/16W MF-LF 402
R2222 10K 5% 1/16W MF-LF 402 (USB_G_OC_PU)
R2226 10K 5% 1/16W MF-LF 402

RTUSB_OC_L
UNUSED_USB_B_OC_L
LTUSB_OC_L
UNUSED_USB_D_OC_L
EXCARD_OC_L
SB_GPIO29
SB_GPIO30
LT2USB_OC_L

PP3V3_S5

R2205 10K MF-LF 1/16W 402 5%
NOSTUFF R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%

SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO

OMIT

U2100
ICH7-M
SB
BGA
(3 OF 6)

PCI-EXP

PCIE_A_D2R_N	F26	PERN1
PCIE_A_D2R_P	F25	PERP1
PCIE_A_R2D_C_N	E28	PETN1
PCIE_A_R2D_C_P	E27	PETP1
PCIE_MINI_D2R_N	H26	PERN2
PCIE_MINI_D2R_P	H25	PERP2
PCIE_B_R2D_C_N	G28	PETN2
PCIE_B_R2D_C_P	G27	PETP2
PCIE_EXCARD_D2R_N	K26	PERN3
PCIE_EXCARD_D2R_P	K25	PERP3
PCIE_C_R2D_C_N	J28	PETN3
PCIE_C_R2D_C_P	J27	PETP3
TP_PCIE_D_D2RN	M26	PERN4
TP_PCIE_D_D2RP	M25	PERP4
TP_PCIE_D_R2DN	L28	PETN4
TP_PCIE_D_R2DP	L27	PETP4
TP_PCIE_E_D2RN	P26	PERN5
TP_PCIE_E_D2RP	P25	PERP5
TP_PCIE_E_R2DN	N28	PETN5
TP_PCIE_E_R2DP	N27	PETP5
TP_PCIE_F_D2RN	T25	PERN6
TP_PCIE_F_D2RP	T24	PERP6
TP_PCIE_F_R2DN	R28	PETN6
TP_PCIE_F_R2DP	R27	PETP6

SPI

	R2	SPI_CLK (INT PD)
	P6	SPI_CS*
	P1	SPI_ARB (INT PD)
	P5	SPI_MOSI
	P2	SPI_MISO

USB

RTUSB_OC_L	D3	OC0*
UNUSED_USB_B_OC_L	C4	OC1*
LTUSB_OC_L	D5	OC2*
UNUSED_USB_D_OC_L	D4	OC3*
EXCARD_OC_L	E5	OC4*
SB_GPIO29	C3	OC5*/GPIO29
SB_GPIO30	A2	OC6*/GPIO30
LT2USB_OC_L	B3	OC7*/GPIO31

DMI

DMI0RXN	V26	DMI_N2S_N<0>
DMI0RXP	V25	DMI_N2S_P<0>
DMI0TXN	U28	DMI_S2N_N<0>
DMI0TXP	U27	DMI_S2N_P<0>
DMI1RXN	Y26	DMI_N2S_N<1>
DMI1RXP	Y25	DMI_N2S_P<1>
DMI1TXN	W28	DMI_S2N_N<1>
DMI1TXP	W27	DMI_S2N_P<1>
DMI2RXN	AB26	DMI_N2S_N<2>
DMI2RXP	AB25	DMI_N2S_P<2>
DMI2TXN	AA28	DMI_S2N_N<2>
DMI2TXP	AA27	DMI_S2N_P<2>
DMI3RXN	AD25	DMI_N2S_N<3>
DMI3RXP	AD24	DMI_N2S_P<3>
DMI3TXN	AC28	DMI_S2N_N<3>
DMI3TXP	AC27	DMI_S2N_P<3>
DMI_CLKN	AE28	SB_CLK100M_DMI_N
DMI_CLKP	AE27	SB_CLK100M_DMI_P
DMI_ZCOMP	C25	
DMI_IRCOMP	D25	DMI_IRCOMP_R

R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB

USBP0N F1 — USB2_RT_N — EXTERNAL 0
USBP0P F2 — USB2_RT_P
USBP1N G4 — USB_TRACKPAD_N — TRACKPAD (GEYSER)
USBP1P G3 — USB_TRACKPAD_P
USBP2N H1 — USB2_LT_N — EXTERNAL 1
USBP2P H2 — USB2_LT_P
USBP3N J4 — USB2_CAMERA_N — CAMERA
USBP3P J3 — USB2_CAMERA_P
USBP4N K1 — USB2_EXCARD_N — EXTERNAL 2
USBP4P K2 — USB2_EXCARD_P
USBP5N L4 — USB_HUB_N — IR
USBP5P L5 — USB_HUB_P
USBP6N M1 — USB_BT_N — BLUETOOTH
USBP6P M2 — USB_BT_P
USBP7N N4 — USB2_LT2_N
USBP7P N3 — USB2_LT2_P

NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD

USBRBIAS* D2
USBRBIAS D1 — USB_RBIAS_PN
R2204 22.6 1% 1/16W MF-LF 402
VOLTAGE=0V
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB

OMIT

U2100
ICH7-M
SB
BGA
(2 OF 6)

PCI

PCI_AD<0>	E18	AD0
PCI_AD<1>	C18	AD1
PCI_AD<2>	A16	AD2
PCI_AD<3>	F18	AD3
PCI_AD<4>	E16	AD4
PCI_AD<5>	A18	AD5
PCI_AD<6>	E17	AD6
PCI_AD<7>	A17	AD7
PCI_AD<8>	A15	AD8
PCI_AD<9>	C14	AD9
PCI_AD<10>	E14	AD10
PCI_AD<11>	D14	AD11
PCI_AD<12>	B12	AD12
PCI_AD<13>	C13	AD13
PCI_AD<14>	G15	AD14
PCI_AD<15>	G13	AD15
PCI_AD<16>	E12	AD16
PCI_AD<17>	C11	AD17
PCI_AD<18>	D11	AD18
PCI_AD<19>	A11	AD19
PCI_AD<20>	A10	AD20
PCI_AD<21>	F11	AD21
PCI_AD<22>	F10	AD22
PCI_AD<23>	E9	AD23
PCI_AD<24>	D9	AD24
PCI_AD<25>	B9	AD25
PCI_AD<26>	A8	AD26
PCI_AD<27>	A6	AD27
PCI_AD<28>	C7	AD28
PCI_AD<29>	B6	AD29
PCI_AD<30>	E6	AD30
PCI_AD<31>	D6	AD31
PCI_FRAME_L	F16	FRAME*
C/BE0*	B15	PCI_C_BE_L<0>
C/BE1*	C12	PCI_C_BE_L<1>
C/BE2*	D12	PCI_C_BE_L<2>
C/BE3*	C15	PCI_C_BE_L<3>
IRDY*	A7	PCI_IRDY_L
PAR	E10	PCI_PAR
PCICLK	A9	PCI_CLK_SB
DEVSEL*	A12	PCI_DEVSEL_L
PERR*	C9	PCI_PERR_L
PLOCK*	E11	PCI_LOCK_L
SERR*	B10	PCI_SERR_L
STOP*	F15	PCI_STOP_L
TRDY*	F14	PCI_TRDY_L
PLTRST*	C26	PLT_RST_L
PCIRST*	B18	PCI_RST_L
(INT 20K PU) PME*	B19	TP_PCI_PME_L

INT I/F

INT_PIRQA_L	A3	PIRQA*
INT_PIRQB_L	B4	PIRQB*
INT_PIRQC_L	C5	PIRQC*
INT_PIRQD_L	B5	PIRQD*
	G8	GPIO2/PIRQE* — SB_GPIO2
	F7	GPIO3/PIRQF* — SB_GPIO3
	F8	GPIO4/PIRQG* — SB_DVI_HPD
	G7	GPIO5/PIRQH* — ODD_PWR_EN_L

MISC

TP_SB_XOR_AE5	AE5	RSVD0
TP_SB_XOR_AD5	AD5	RSVD1
TP_SB_XOR_AG4	AG4	RSVD2
TP_SB_XOR_AH4	AH4	RSVD3
TP_SB_XOR_AD9	AD9	RSVD4
	AE9	RSVD5 — TP_SB_XOR_AE9
	AG8	RSVD6 — TP_SB_XOR_AG8
	AH8	RSVD7 — TP_SB_XOR_AH8
	F21	RSVD8 — TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
	AH20	MCH_SYNC* — NB_SB_SYNC_L

NOTE: CHANGE SYMBOL TO RSVD[1-9]

NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H

	D7	GNT0* — TP_PCI_GNT0_L
	C16	GNT1* — TP_PCI_GNT1_L
	D16	GNT2* — TP_PCI_GNT2_L
	C17	GNT3* — PCI_GNT3_L
	E7	REQ0* — PCI_REQ0_L
	E13	REQ1* — PCI_REQ1_L
	D17	REQ2* — PCI_REQ2_L
	F13	REQ3* — PCI_GNT3_L
	A13	REQ4*/GPIO22 — SB_CRT_TVOUT_MUX (NOTE: FWH_WP_L NOT USED)
	A14	GNT4*/GPIO48 — TP_PCI_GNT4_L
	C8	GPIO1/REQ5*
	D8	GPIO17/GNT5* — BOOT_LPC_SPI_L

PP3V3_S0

R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402

PCI_PME_FW_L

R2211 1K 5% 1/16W MF-LF 402

BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IE SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)

SB BOOT BIOS SELECT

STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT) 11	UNSTUFF	UNSTUFF
PCI 10	UNSTUFF	STUFF
SPI 01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

PP3V3_S0

PP3V3_S5

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

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SMBUS_SB_SCL → C22 SMBCLK
SMBUS_SB_SDA → B22 SMBDATA
SMB_LINK_ALERT_L → A26 LINKALERT*
SMLINK<0> → B25 SMLINK0
SMLINK<1> → A25 SMLINK1
NOT USED
PM_RI_L → A28 RI*
SB_SPKR → A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L → A27 SUS_STAT*
PM_SYSRST_L → A22 SYS_RST*
PM_BMBUSY_L → AB18 GPIO0/BM_BUSY*
SMB_ALERT_L → B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L → AC20 GPIO18/STPPCI*
PM_STPCPU_L → AF21 GPIO20/STPCPU*
SB_GPIO26 → A21 GPIO26
BIOS_REC → B21 GPIO27
FWH_MFG_MODE → E23 GPIO28
PM_CLKRUN_L → AG18 GPIO32/CLKRUN*
GPU_D3COLD_RESET_L → AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L → U2 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L → F20 WAKE*
INT_SERIRQ → AH21 SERIRQ
PM_THRM_L → AF20 THRM*
VR_PWRGD_CK410 → AD22 VRMPWRGD
TP_SB_GPIO6 → AC21 GPIO6
SMC_RUNTIME_SCI_L → AC18 GPIO7
SMC_EXTSMI_L → E21 GPIO8

SMB

CLKS

SYS GPIO

PWR MNGT

GPIO

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

AF19 SB_GPIO21 100 R2302
AH18 SB_GPIO19 100 R2303
AH19
AE19 SB_GPIO37 100 R2305
SATA_C_DET_L

CLK14 AC1 SB_CLK14P3M_TIMER
CLK48 B2 SB_CLK48M_USBCTLR
SUSCLK C20 TP_SB_SUS_CLK
SLP_S3* B24 PM_SLP_S3_L
SLP_S4* D23 PM_SLP_S4_L
SLP_S5* F22 PM_SLP_S5_L
PWROK AA4 PM_SB_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
PWRBTN* (INT 20K PU) C23 PM_PWRBTN_L
LAN_RST* C19 PM_LAN_ENABLE
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4

GPIO9 E20 SMS_INT_L
GPIO10 A20 SMC_SB_NMI
DEF=GPI GPIO12 F19 LAN_ENERGY_DET
GPIO13 E19
DEF=GPI GPIO14 R4 IDE_RESET_L
GPIO15 E22 SV_SET_UP
GPIO24 R3 CRB_SV_DET
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 SB_CLK100M_SATA_OE_L
GPIO36 AD20 SB_GPUVCORE_DISABLE_L
DEF=GPI GPIO39 AE20 SATA_C_PWR_EN_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

PM_BATLOW_L
PM_RSMRST_L
R2399 100K 5% 1/16W 402 MF-LF
SMC_WAKE_SCI_L

PP3V3_S5

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

PP3V3_S5

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE
BIOS_REC

PP3V3_S0

R2388 10K 5% 1/16W MF-LF 402

SATA_C_PWR_EN_L

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SB: 3 OF 4

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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NONE	23	87

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VSS

A4			AD3
A23			AD4
N24			AD7
P24			AD8
R18			AD15
U14			AD19
V27			AD23
AA24			AE2
AB27			AE4
AD11			AE8
B1			AE11
D10			AE13
F4			AE18
G18			AE21
J1			B8
L24			B11
M17			B14
N14			B17
N17			B20
N18			B26
N25			B28
N26			C2
P3			C6
P4			C27
P12			D13
P13			D18
P14			D21
P15			D24
P16			E1
P17			E2
P27			E4
P28			E8
R1			E15
R11			F3
R12			F5
R13			F12
R14			F27
R15			F28
R16			G1
R17			G2
T6			G5
T12			G6
T13			G9
T14			G14
T15			G21
T16			G24
T17			G25
U4			G26
U12			H3
U13			H4
U15			H5
U16			H24
U17			H27
U24			H28
U25			J2
U26			J5
V2			J24
V13			J25
V15			J26
V24			K24
V28			K27
W6			K28
W24			L13
W25			L15
W26			L25
Y3			L26
Y24			M3
Y27			M4
Y28			M5
AA1			M12
AA25			M13
AA26			M14
AB4			M15
AB6			M16
AB11			M24
AB14			M27
AB16			M28
AB19			N1
AB21			N2
AB24			N5
AB28			N6
AC2			N11
AC5			N12
AC9			N13
AC11			N15
AD1			N16
AE24			AG11
AE25			AG14
AF2			AG17
AF4			AG20
AF8			AG25
AF11			AH1
AF27			AH3
AF28			AH7
AG1			AH12
AG3			AH23
AG7			AH27

0 0

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25D7 PP5V_S0_SB_V5REF	G10		L11
	AD17	V5REF	L12
25C7 PP5V_S5_SB_V5REF_SUS	F6	V5REF_SUS	L14
			L16
25B6 22C1 PP1V5_S0_SB_VCC1_5_B	AA22		L17
	AA23		L18
	AB22		M11
	AB23		M18
	AC23		P11
	AC24		P18
	AC25		T11
	AC26		T18
	AD26		U11
	AD27		U18
	AD28		V11
	D26		V12
	D27		V14
	D28		V16
	E24		V17
	E25		V18
	E26		
	F23		V5
	F24		V1
	G22		W2
	G23	VCCA3GP	W7
	H22	VCC1_5_B	
	H23		U6
	J22		R7
	J23		
	K22		AE23
	K23		AE26
	L22		AH26
	L23		
	M22		AA7
	M23		AB12
	N22		AB20
	N23		AC16
	P22		AD13
	P23		AD18
	R22		AG12
	R23		AG15
	R24		AG19
	R25		
	R26		A5
	T22		B13
	T23		B16
	T26		B7
	T27		C10
	T28		D15
	U22		F9
	U23		G11
	V22		G12
	V23		G16
	W22		
	W23		W5
	Y22		
	Y23		P7
25B6 22C1 PP3V3_S0	B27	VCC3_3	A24
	AG28	VCCDMIPLL	C24
25A5 PP1V5_S0_SB_VCCDMIPLL			D19
			D22
25B6 25B2 25A8 24B5 24A5 24A3 9B7 8B7 5D4 5D1 PP1V5_S0	AB7		G19
	AC6		
	AC7		K3
	AD6	ARX	K4
	AE6	VCC1_5_A	K5
	AF5		K6
	AF6		L1
	AG5		L2
	AH5		L3
			L6
67C8 67C6 66C6 62C1 62A8 48B6 25D6 25C8 25C6 25C2 PP1V5_S0	AD2	VCCSATAPLL	L7
			M6
52D3 49C7 49C4 49B5 48B6 36D6 34A8 33D8 33D3 25C8 PP3V3_S0	AH11	VCC3_3	M7
			N7
67C8 67C6 66C6 62C1 62A8 48B6 25D6 25C8 25C6 25C2 PP1V5_S0	AB10		
	AB9		AB17
	AC10		AC17
	AD10	ATX	T7
	AE10	VCC1_5_A	F17
	AF10		G17
	AF9		
	AG9		AB8
	AH9		AC8
24B3 23D8 23D4 21D1 23B7 22A7 22D9 22C6 11B5 5D4 PP3V3_S5	E3	VCCSUS3_3	K7
6SD2 6SD1 5SC8 63D8 5GD4 24C5 25D2 25C8 25B6 24C3			C28
	C1	VCCUSBPLL	G20
25B6 25B2 25A8 24B5 24A5 24A3 9B7 8B7 5D4 5D1 PP1V5_S0			
67C8 67C6 66C5 62C1 62A8 48B6 25D6 25C8 25C6 25C2			A1
VOLTAGE GENERATED INTERNALLY	AA2		H6
SO NO CONNECT HERE	Y7	VCCLAN1_5	H7
		CHANGE SYMBOL TO 1.05	J6
			J7

CORE
VCC1_05

VCC_PAUX
VCCLAN_3_3

IDE
VCC3_3

PCI
VCC3_3

USB
VCCSUS3_3

USB CORE
VCC1_5_A

PP1V05_S0
PP3V3_S0
PP3V3_S5
PP1V5_S0
PP3V3_G3C_SB_RTC_D

VCCRTC

VCCSUS1_5
CHANGE SYMBOL TO 1.05

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

VCC3_3/VCCHDA
VCCSUS3_3/VCCSUSHDA
V_CPU_IO

SB: 4 OF 4

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)

PP1V5_S0

C2511 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG5

PP3V3_S0

R2502 100 1/16W MF-LF 402 5%

D2502 BAT54DW SOT-363

PP5V_S0

ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)

PP5V_S0_SB_V5REF 24D5
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM

C2503 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)

PP1V5_S0

C2517 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AD2

PP3V3_S5

R2501 10 1/16W MF-LF 402 5%

D2502 BAT54DW SOT-363

ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)

PP5V_S5_SB_V5REF_SUS 24D5
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM

C2504 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)

PP3V3_S0

C2513 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AH11

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)

PP1V5_S0

C2514 1UF 10% 6.3V CERM 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AG9

PP1V5_S0

L2500 100-OHM-EMI SM-3

ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)

PP1V5_S0_SB_VCC1_5_B 22C1 24D5
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C2500 220UF 20% 2V POLY CASE-B2
C2505 0.1UF 10% 16V X5R 402
C2506 0.1UF 10% 16V X5R 402
C2507 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY NEAR PINS D28, T28, AD28

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)

PP3V3_S5

C2520 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)

PP1V5_S0

C2515 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)

PP3V3_S0

C2509 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB

PP1V5_S0

R2500 1 1/10W 5% MF-LF 603

PP1V5_S0_SB_VCCDMIPLL_F
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

L2507 0.28-OHM 1206

ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)

PP1V5_S0_SB_VCCDMIPLL 24B5
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C2501 0.01UF 10% 16V CERM 402
C2508 10UF 20% 6.3V X5R 603

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)

PP1V05_S0

C2518 0.1UF 10% 16V X5R 402
C2502 1UF 10% 6.3V CERM 402
C2516 330UF 20% 2.5V POLY CASE-C2

PLACEHOLDER FOR 270UF

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)

PP3V3_S5

C2531 0.1UF 10% 16V X5R 402
C2534 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS NEAR PINS A24 ... G19 AND P7 OF SB

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)

PP3V3_S0

C2519 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V1, V5, W2, OR W7

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)

PP3V3_S5

C2533 0.1UF 10% 16V X5R 402
C2532 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS NEAR PINS K3 ... N7 OF SB

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)

PP3V3_S0

C2521 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN U6

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)

PP1V05_S0

PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB

C2523 0.1UF 10% 16V X5R 402
C2522 0.1UF 10% 16V X5R 402
C2524 4.7UF 20% 6.3V CERM 603

ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)

PP1V5_S0

C2510 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS NEAR PINS AB8 AND AC8 OF SB

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)

PP1V5_S0

C2512 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS A1 ... J7

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)

PP3V3_S0

C2525 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS AA7 ... AG19

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)

PP3V3_S0

C2526 0.1UF 10% 16V X5R 402
C2527 0.1UF 10% 16V X5R 402
C2528 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB NEAR PINS A5 ... G16

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)

PP3V3_G3C_SB_RTC_D

C2530 0.1UF 10% 16V X5R 402
C2529 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB

SB: 4 OF 4

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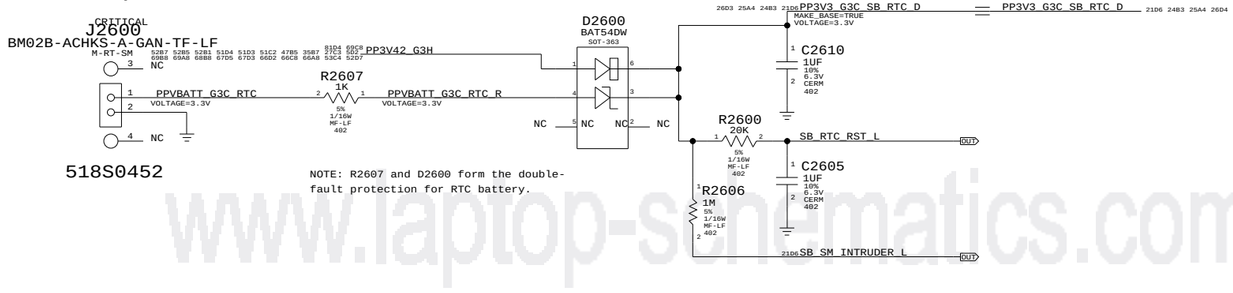
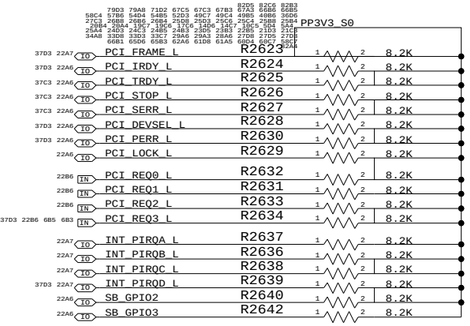
D	051-7164	03001
SCALE: NONE	SHT 25 OF 87	

RTC Battery Connector



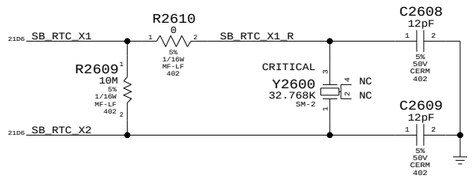
518S0452

NOTE: R2607 and D2600 form the double-fault protection for RTC battery.

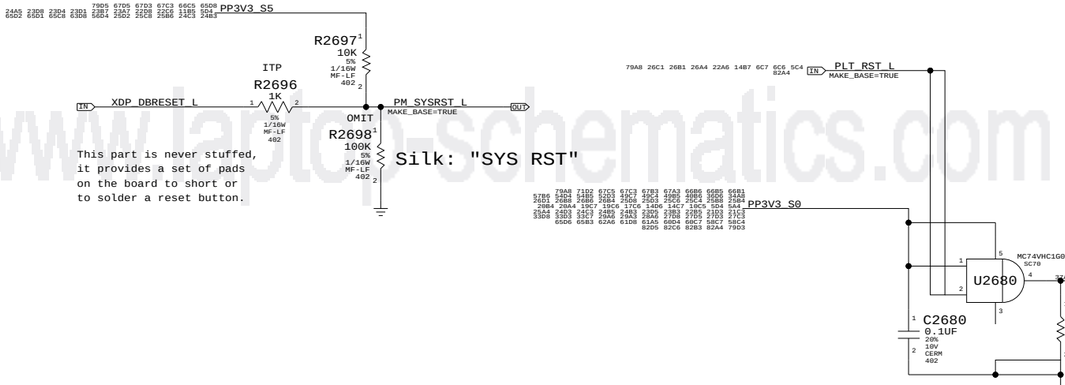


Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit

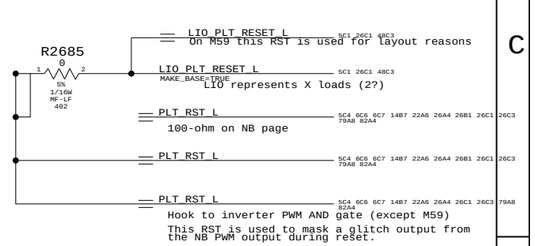


Platform Reset Connections



This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Unbuffered



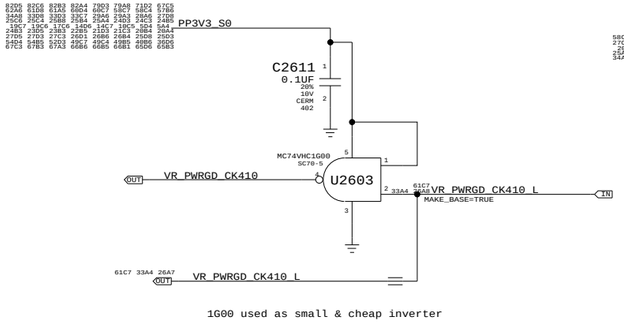
Hook to inverter PWM AND gate (except M59)

This RST is used to mask a glitch output from the NB PWM output during reset.

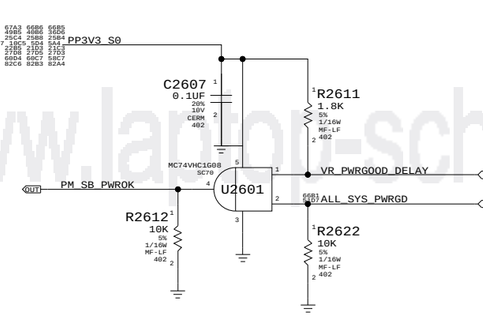
Buffered

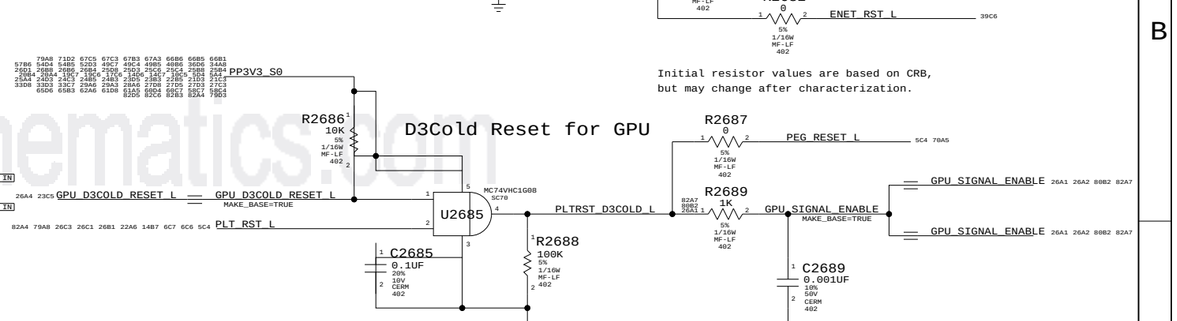
Linda Card represents 3 loads

Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter





SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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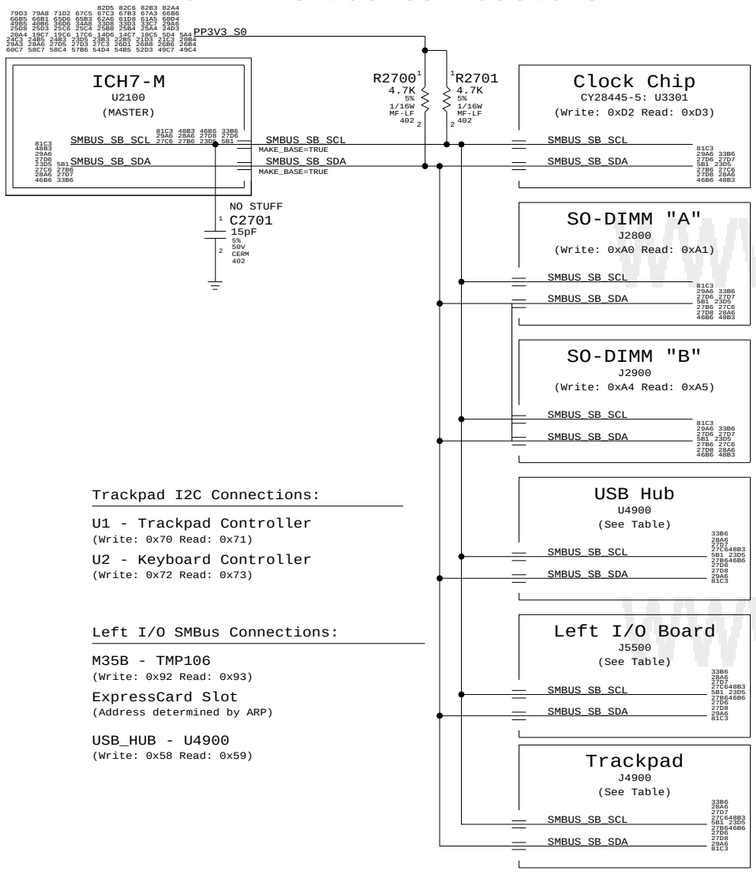
ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

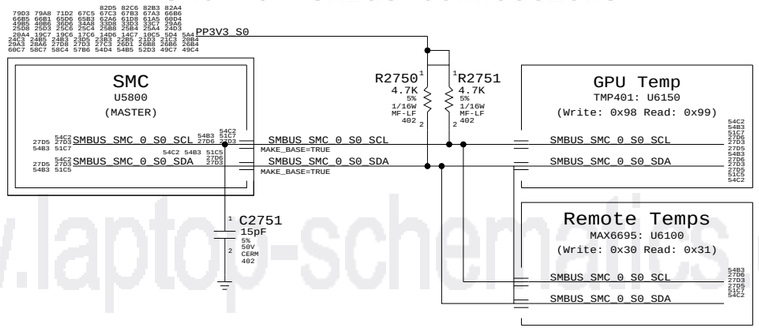
Left I/O SMBus Connections:

M35B - TMP106
(Write: 0x92 Read: 0x93)

ExpressCard Slot
(Address determined by ARP)

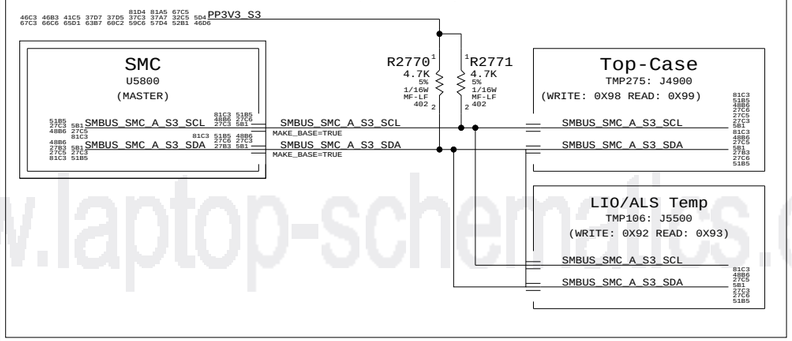
USB_HUB - U4900
(Write: 0x58 Read: 0x59)

SMC "0" SMBus Connections

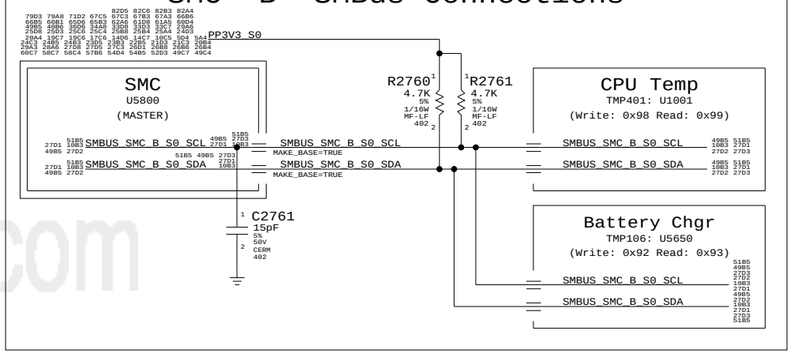


SMC "A" SMBus Connections

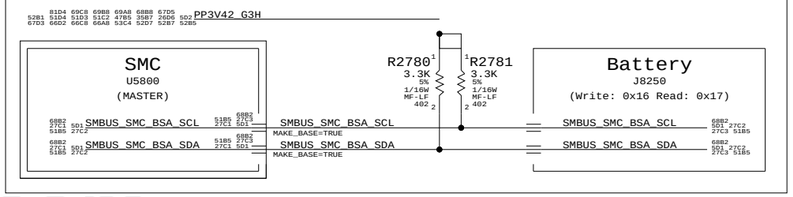
NOTE: SMC RMT bus remains powered and may be active in S3 state



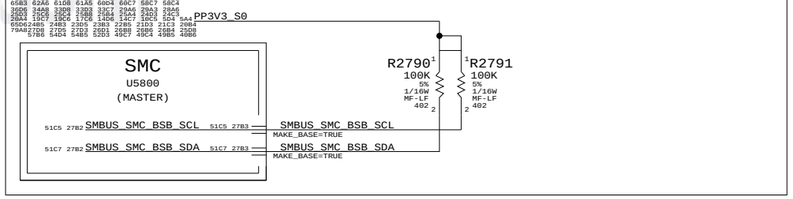
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



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M57 SMBUS CONNECTIONS

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SCALE	SHT	OF
NONE	27	87

Page Notes

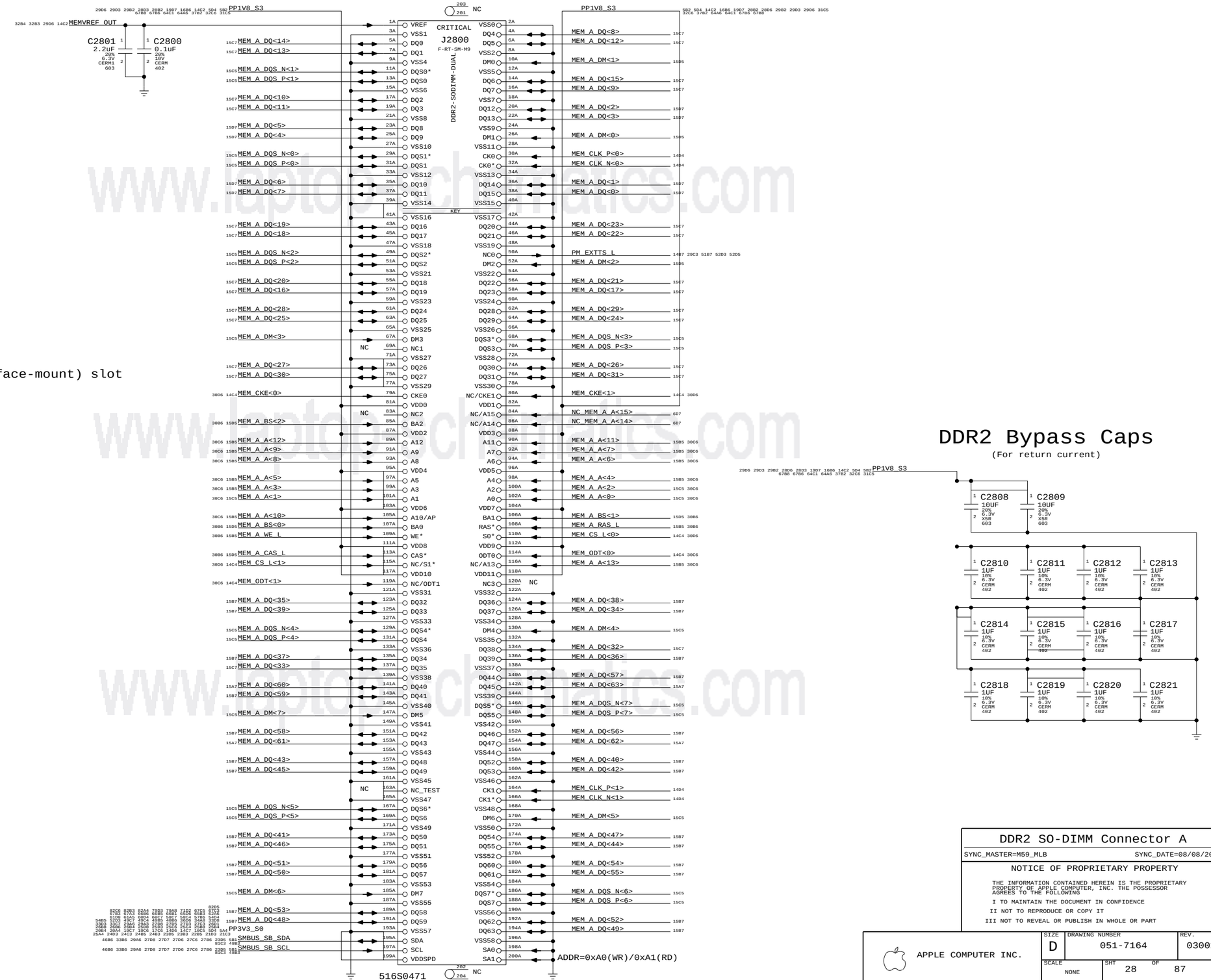
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot



DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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SCALE: NONE	SHT 28 OF 87	

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Page Notes

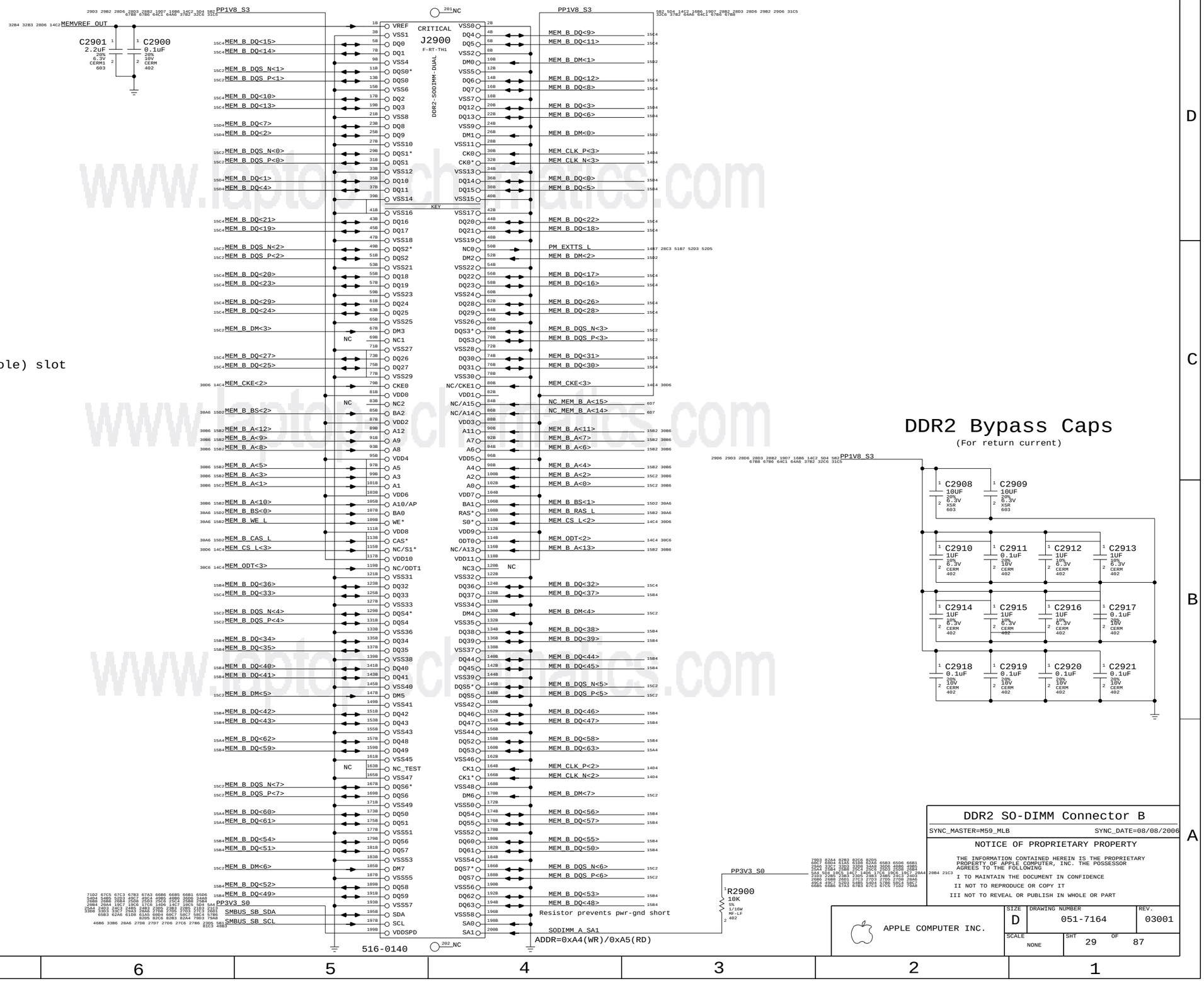
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Factory" (thru-hole) slot



DDR2 Bypass Caps

(For return current)

PP3V3_S0
R2900 10K 5% 1/16W MF-LF 402

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DDR2 SO-DIMM Connector B			
SYNC_MASTER=M59_MLB	SYNC_DATE=08/08/2006		
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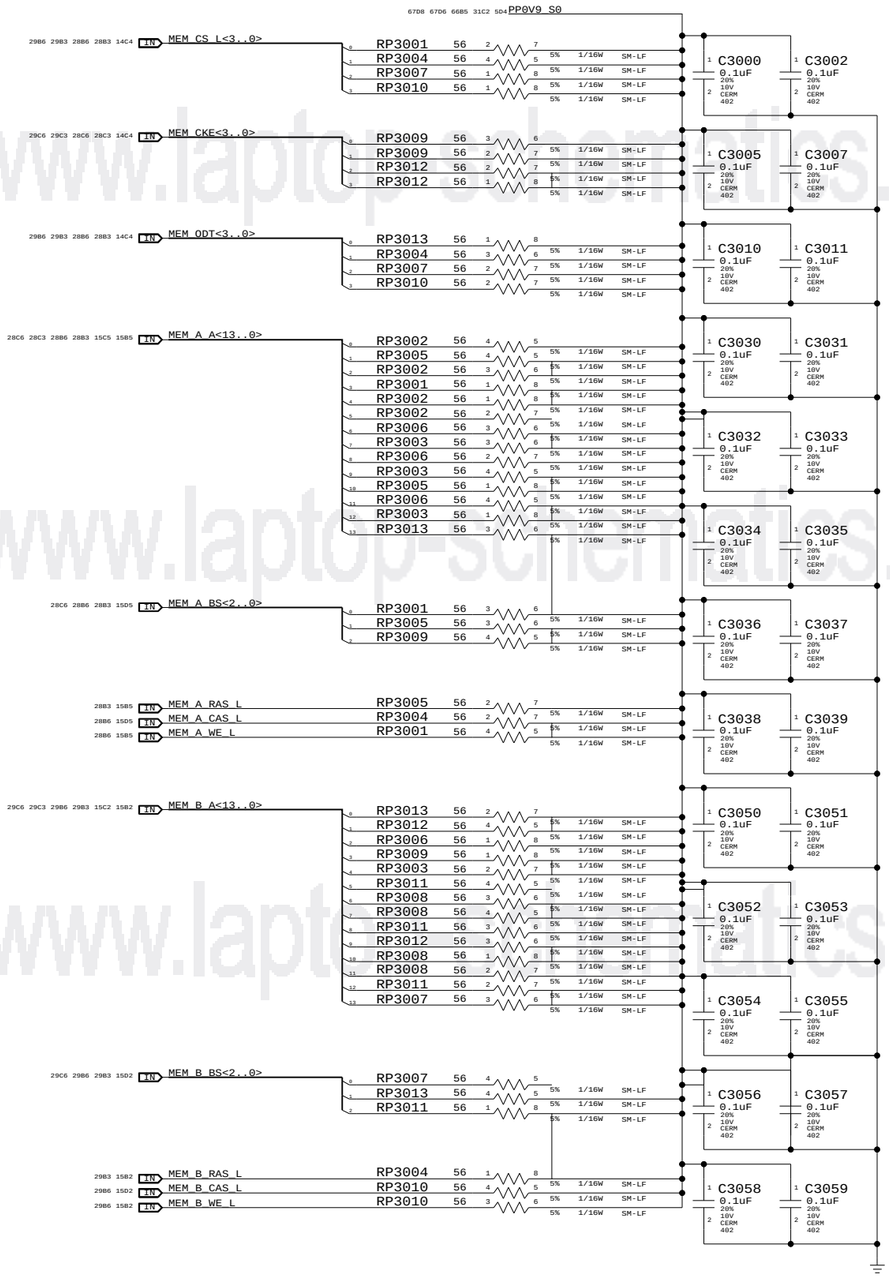
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7164	REV. 03001
	SCALE NONE	SHT 29 OF 87	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



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Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE NONE SHT 30 OF 87

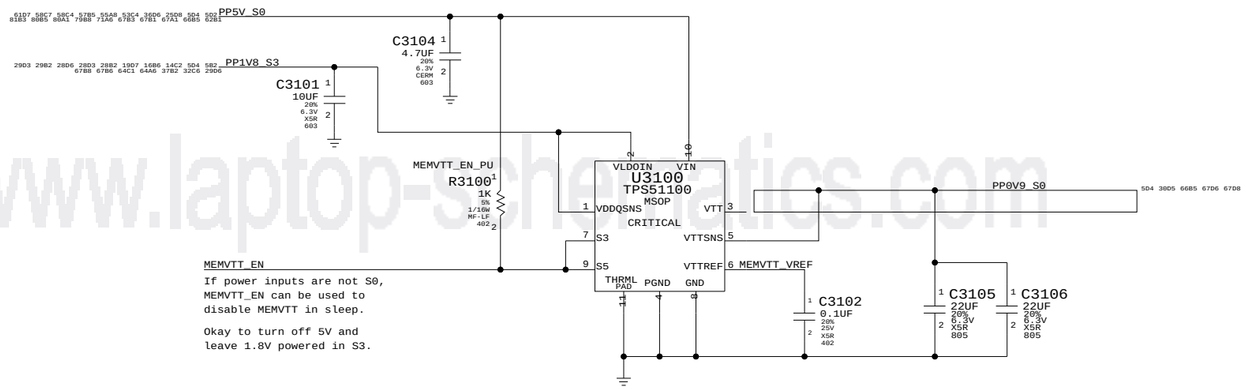
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



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Memory Vtt Supply

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SCALE: NONE SHT 31 OF 87

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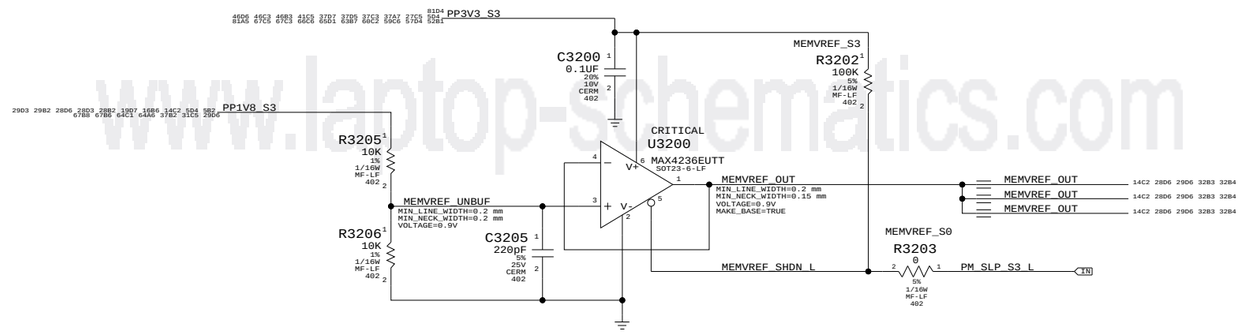

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DDR2 VRef

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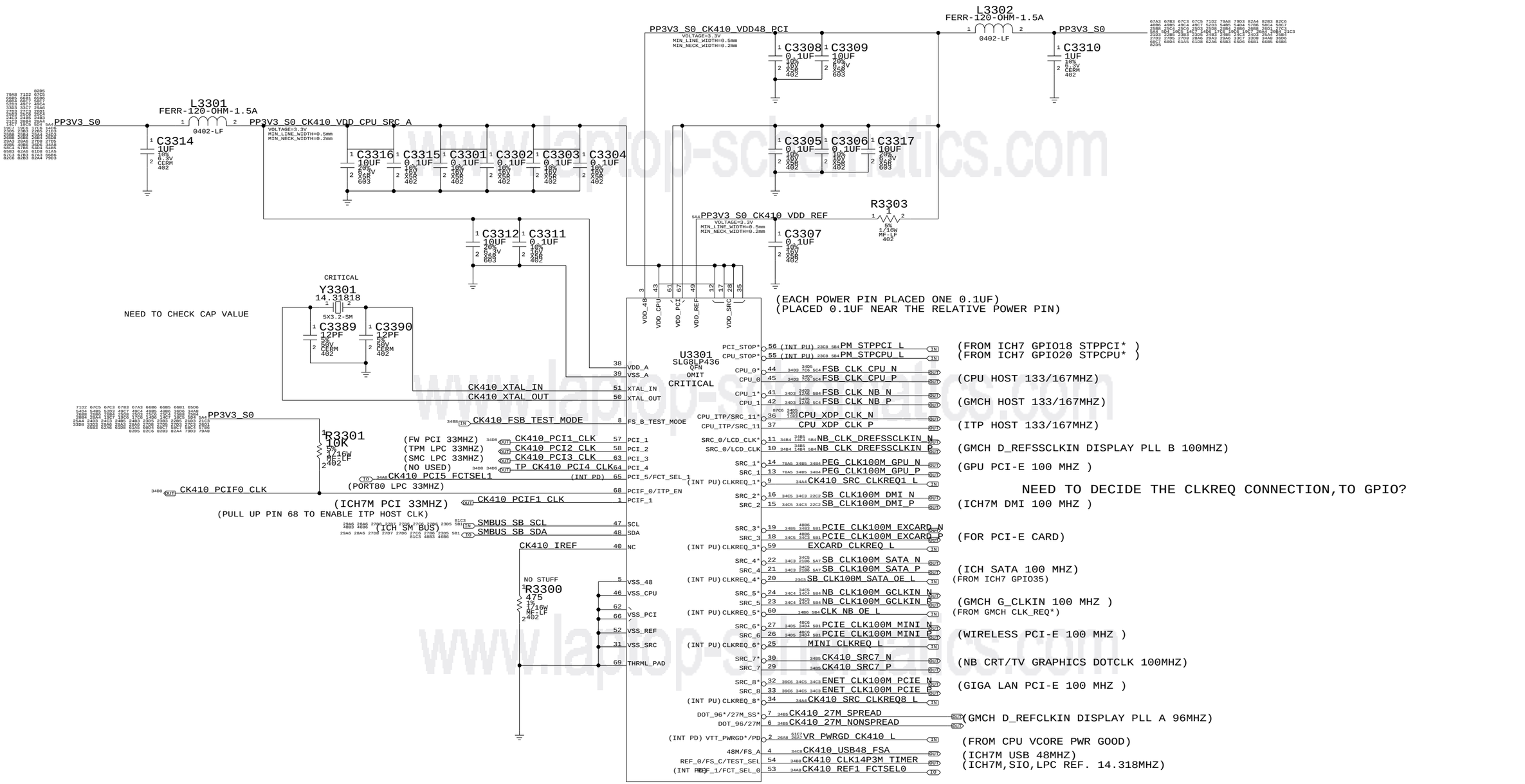
SCALE: NONE

SHT 32 OF 87



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

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D	051-7164	03001
SCALE: NONE	SHT 33 OF 87	

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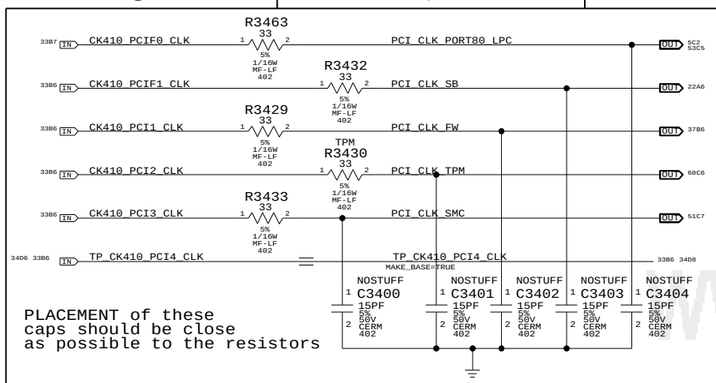
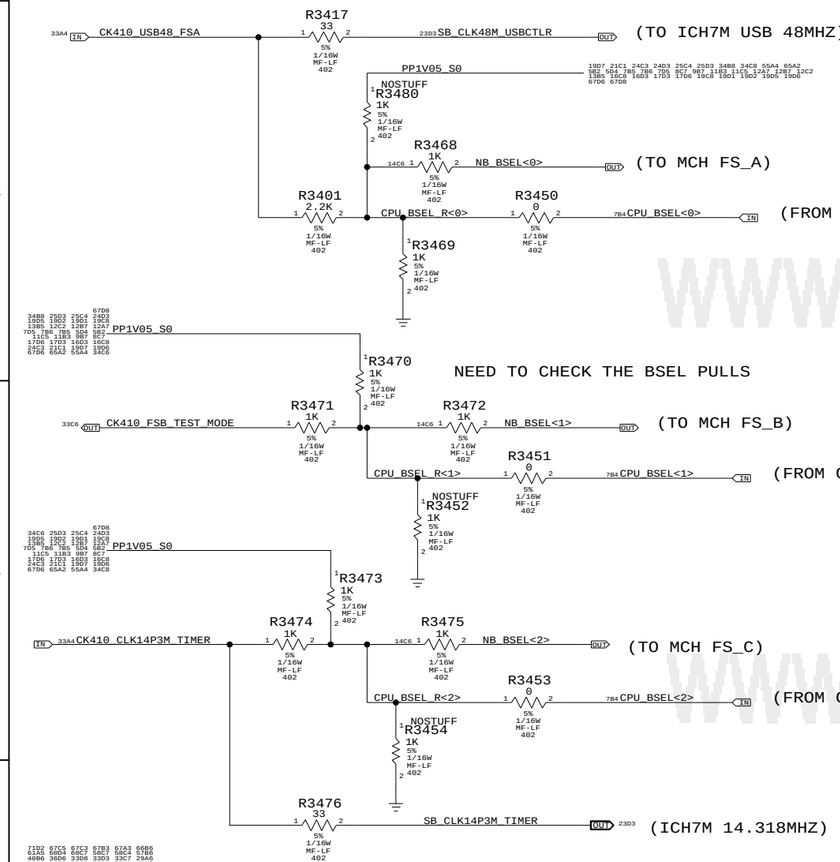
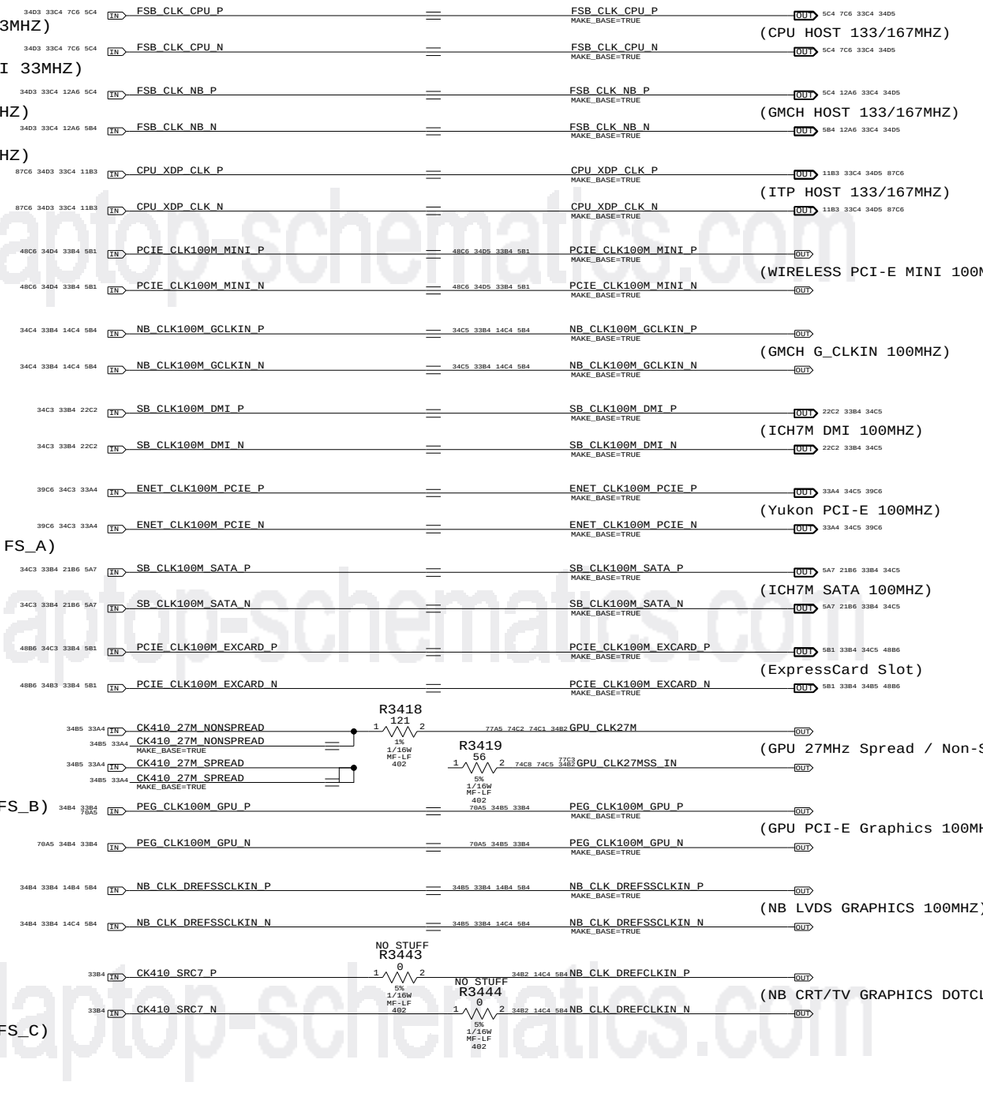


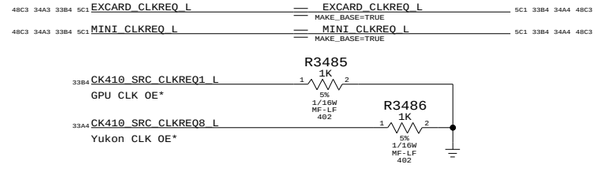


NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED





Clock Termination

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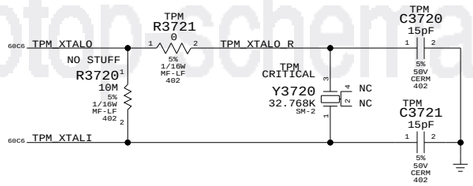
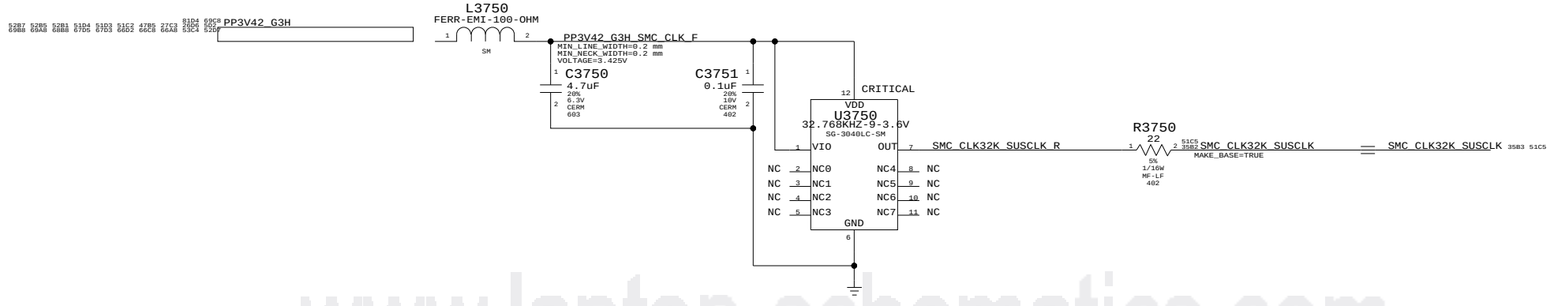
TPM Crystal Circuit



SMC G3Hot Oscillator



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Mobile Clocking

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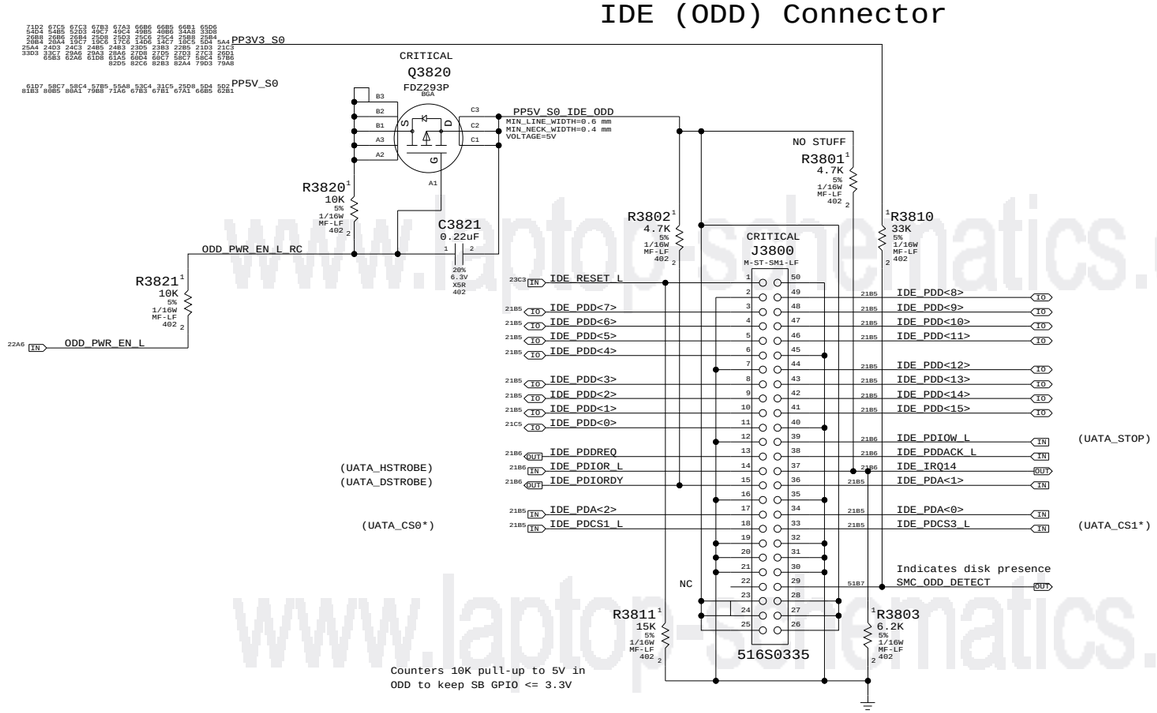
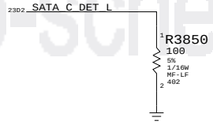
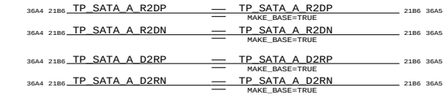
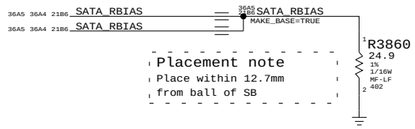
SCALE: NONE	SHT 35 OF 87	

IDE (ODD) Connector









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PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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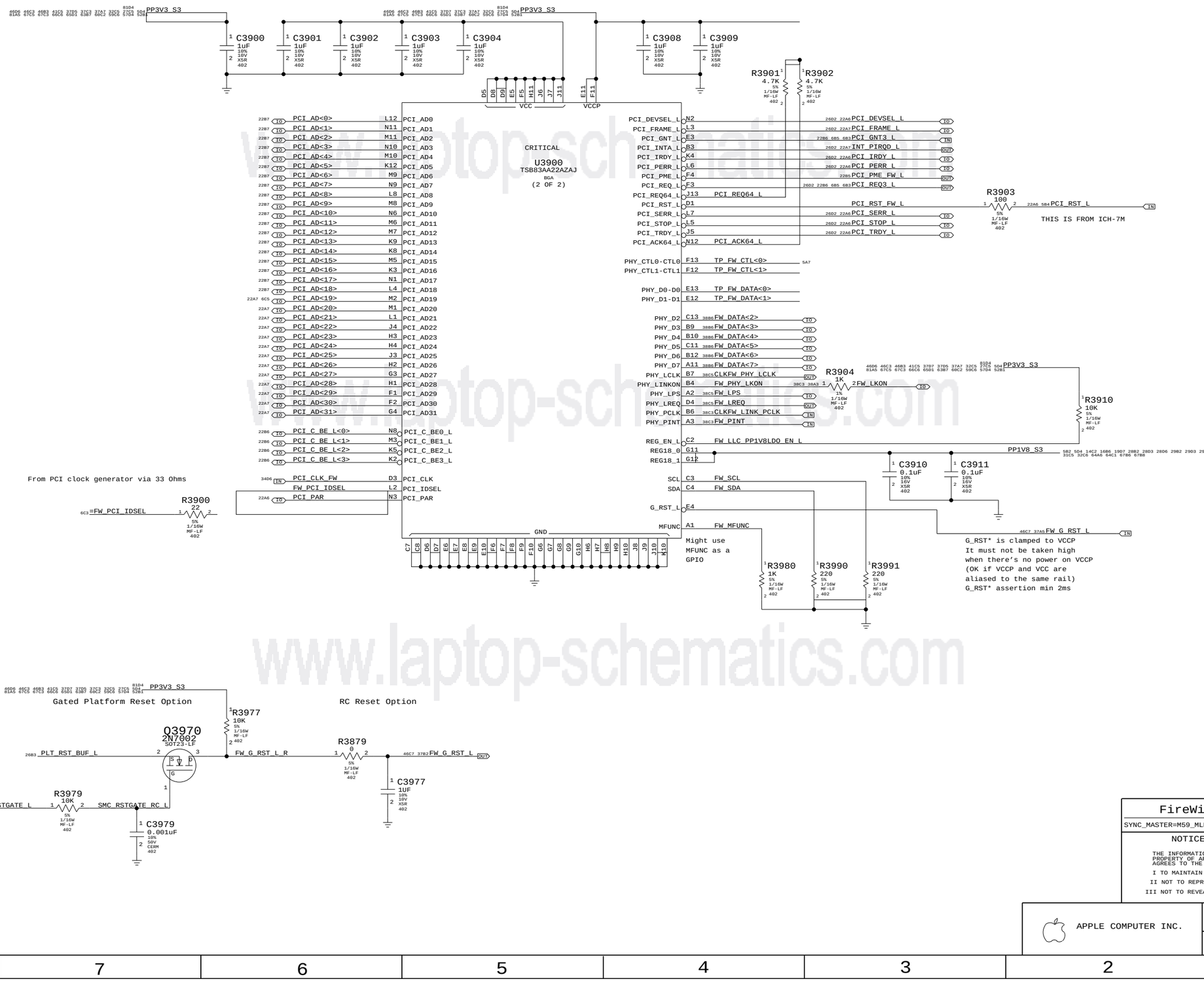
D	051-7164	03001

SCALE	SHT	OF
NONE	36	87



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FireWire Link (TSB83AA22)

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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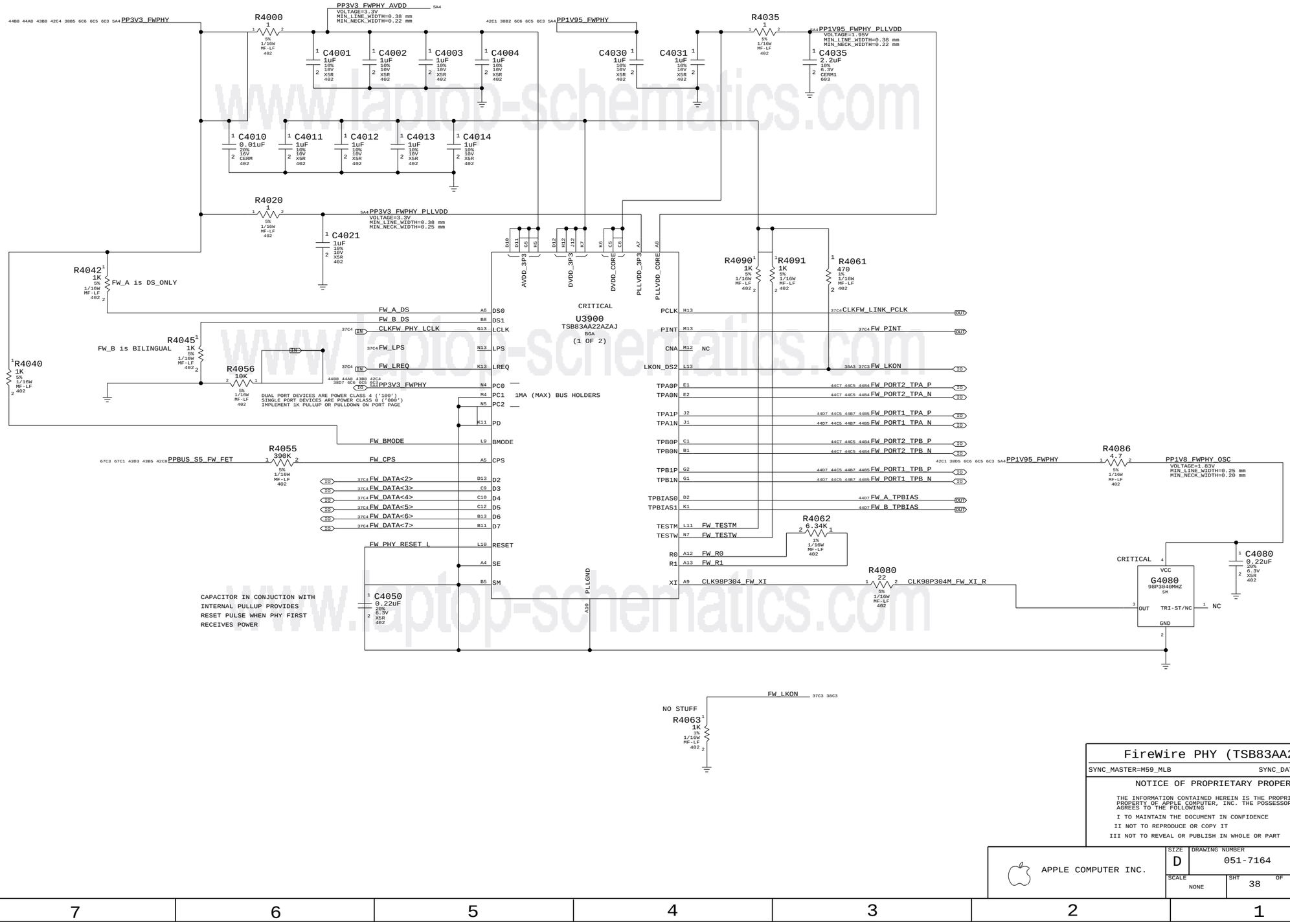
SCALE: NONE	SHT 37 OF 87	



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PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402-LF

PP2V5_S3

PLACE C4107 NEAR U4101 AVDD

PP3V3_S3AC

PP1V2_S3

PLACE C4110 AND C4111 WITHIN 12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF X5R 10% 16V 402
C4113 0.1UF X5R 16V 10% 402

PLACE C4113 AND C4112 WITHIN 12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

OMIT CRITICAL U4101 88E8053 QFN

VDD7 VDD6 VDD5 VDD4 VDD3 VDD2 VDD1 VDD0
VDDO_TTL4 VDDO_TTL3 VDDO_TTL2 VDDO_TTL1 VDDO_TTL0
AVDD AVDDL6 AVDDL5 AVDDL4 AVDDL3 AVDDL2 AVDDL1 AVDDL0 VDD25

ENET_LOM_DIS_L
PM_SLP_S3_L

ANALOG
LOM_DISABLE*
VAUX_AVLBL
VMAIN_AVLBL
SWITCH_VCC
SWITCH_VAUX
HSDACP
HSDACN

OPTIONAL EXTERNAL LDO
NC_ENET_CTRL25
NC_ENET_CTRL12
CTRL25
CTRL12

ENET_RSET
RSET

R4102 4.87K 1% 1/16W MF-LF 402

NO PULL-UP NEEDED

LED
LED_ACT*
LED_LINK10/100*
LED_LINK1000*
LINK*

TEST
TSTPT
TESTMODE

PCI EXPRESS
TX_P
TX_N
RX_P
RX_N
REFCLKP
REFCLKN
WAKE*
PERST*

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

MEDIA
MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

TWSI
VPD_CLK
VPD_DATA

ENET_VPD_CLK
ENET_VPD_DATA

TEST
PU_VDDO_TTL0
PU_VDDO_TTL1

ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 80S3

SPI
SPI_DI
SPI_DO
SPI_CLK
SPI_CS

INTERNAL PULL-UP

MAIN CLK
XTALI
XTALO

CRITICAL
ENET_XTALI
ENET_XTALO
Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD

R4106 R4105 R4104 R4103 R4120 R4119 R4118 R4117
49.9 1% 1/16W MF-LF 402

ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V

C4116 C4115 C4117 C4118 0.001UF 10% 50V CERM 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

PLACE RESISTORS CLOSE TO U4101

R4101 4.7K 5% 1/16W MF-LF 402
Q4100 2N7002 SOT23-LF
R4132 100K 5% 1/16W MF-LF 402
ENET_LOWPWR_EN

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT CRITICAL
U4102 M24C08 SO8
VCC E2 NC1 NC0 WC* VSS SDA SCL

R4122 10K 5% 1/16W MF-LF 402
R4123 10K 5% 1/16W MF-LF 402

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4126 C4127 C4128 C4129 C4130 C4131 0.001UF C4132 0.001UF C4133 0.001UF C4134 0.001UF
10% 16V X5R 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4135 C4136 C4137 0.1UF C4138 0.001UF C4139 0.001UF
10% 16V X5R 402
10% 50V CERM 402

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ETHERNET CONTROLLER

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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D	051-7164	03001
SCALE: NONE	SHT 39 OF 87	

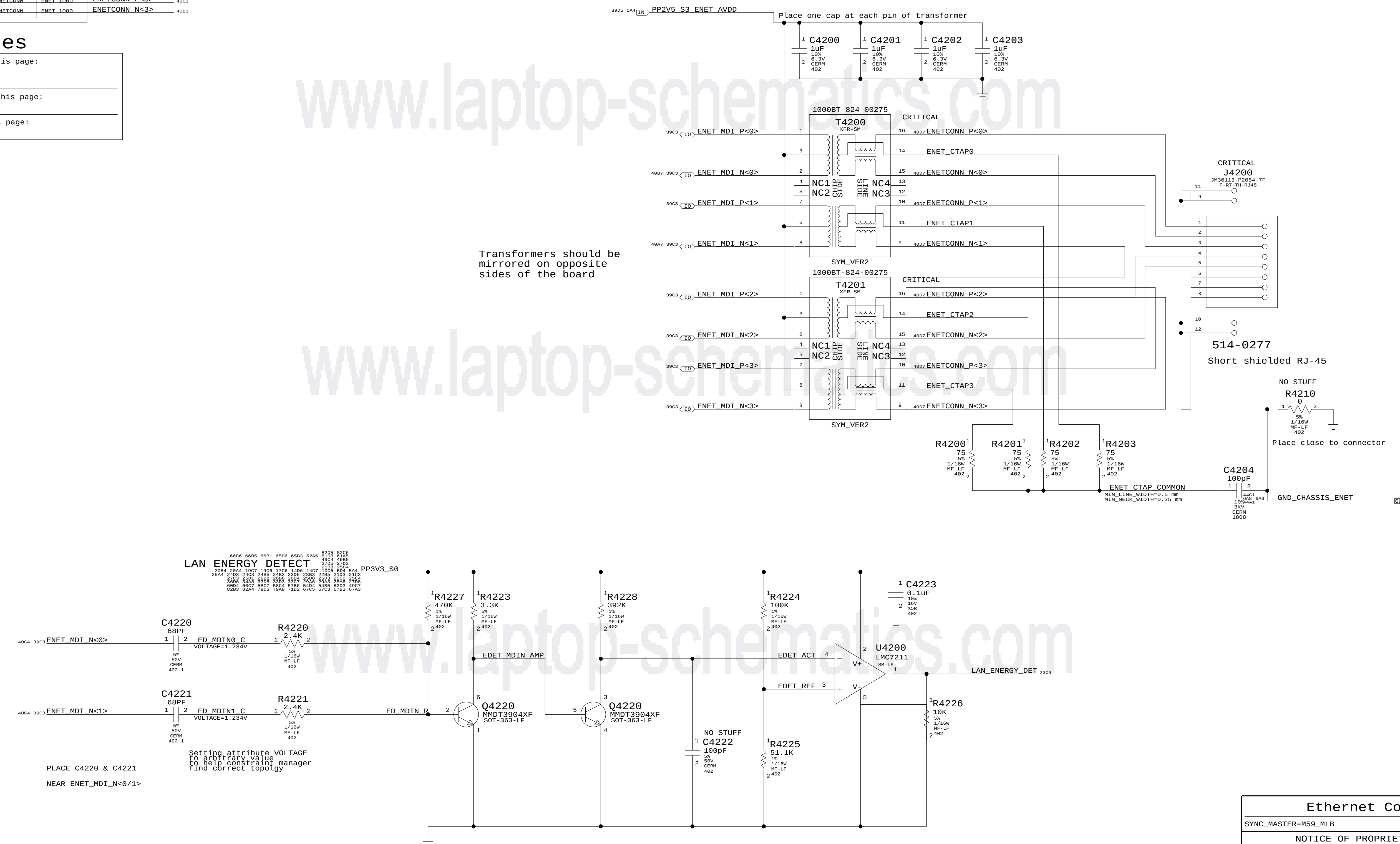
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>	40D3
	ENETCONN	ENET_100D	ENETCONN_N<0>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<1>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<2>	40C3
	ENETCONN	ENET_100D	ENETCONN_P<3>	40C3
	ENETCONN	ENET_100D	ENETCONN_N<3>	40B3

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PP2V5_S3_ENET_AVDD
Place one cap at each pin of transformer
C4200 1uF 10% 6.3V CERM 402
C4201 1uF 10% 6.3V CERM 402
C4202 1uF 10% 6.3V CERM 402
C4203 1uF 10% 6.3V CERM 402
1000BT-824-00275
CRITICAL
T4200 XFR-SM
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENETCONN_P<0>
ENET_CTAP0
ENETCONN_N<0>
ENETCONN_P<1>
ENET_CTAP1
ENETCONN_N<1>
SYM_VER2
T4201 XFR-SM
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
ENETCONN_P<2>
ENET_CTAP2
ENETCONN_N<2>
ENETCONN_P<3>
ENET_CTAP3
ENETCONN_N<3>
Transformers should be mirrored on opposite sides of the board
CRITICAL
J4200
JM36113-P2054-7F
F-RT-TH-RJ45
514-0277
Short shielded RJ-45
NO STUFF
R4210 0 5% 1/16W MF-LF 402
Place close to connector
R4200 75 5% 1/16W MF-LF 402
R4201 75 5% 1/16W MF-LF 402
R4202 75 5% 1/16W MF-LF 402
R4203 75 5% 1/16W MF-LF 402
ENET_CTAP_COMMON
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
C4204 100pF 10% 3KV CERM 1808
GND_CHASSIS_ENET
LAN ENERGY DETECT
PP3V3_S0
R4227 470K 1% 1/16W MF-LF 402
R4223 3.3K 5% 1/16W MF-LF 402
R4228 392K 1% 1/16W MF-LF 402
R4224 100K 1% 1/16W MF-LF 402
C4223 0.1uF 10% 16V X5R 402
C4220 68PF 5% 50V CERM 402-1
ENET_MDI_N<0>
ED_MDIN0_C
VOLTAGE=1.234V
R4220 2.4K 5% 1/16W MF-LF 402
EDET_MDIN_AMP
EDET_ACT
EDET_REF
U4200 LMC7211 SM-LF
LAN_ENERGY_DET
C4221 68PF 5% 50V CERM 402-1
ENET_MDI_N<1>
ED_MDIN1_C
VOLTAGE=1.234V
R4221 2.4K 5% 1/16W MF-LF 402
ED_MDIN_R
Q4220 MMDT3904XF SOT-363-LF
Q4220 MMDT3904XF SOT-363-LF
NO STUFF
C4222 100pF 5% 50V CERM 402
R4225 51.1K 1% 1/16W MF-LF 402
R4226 10K 5% 1/16W MF-LF 402
Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy
PLACE C4220 & C4221
NEAR ENET_MDI_N<0/1>

Ethernet Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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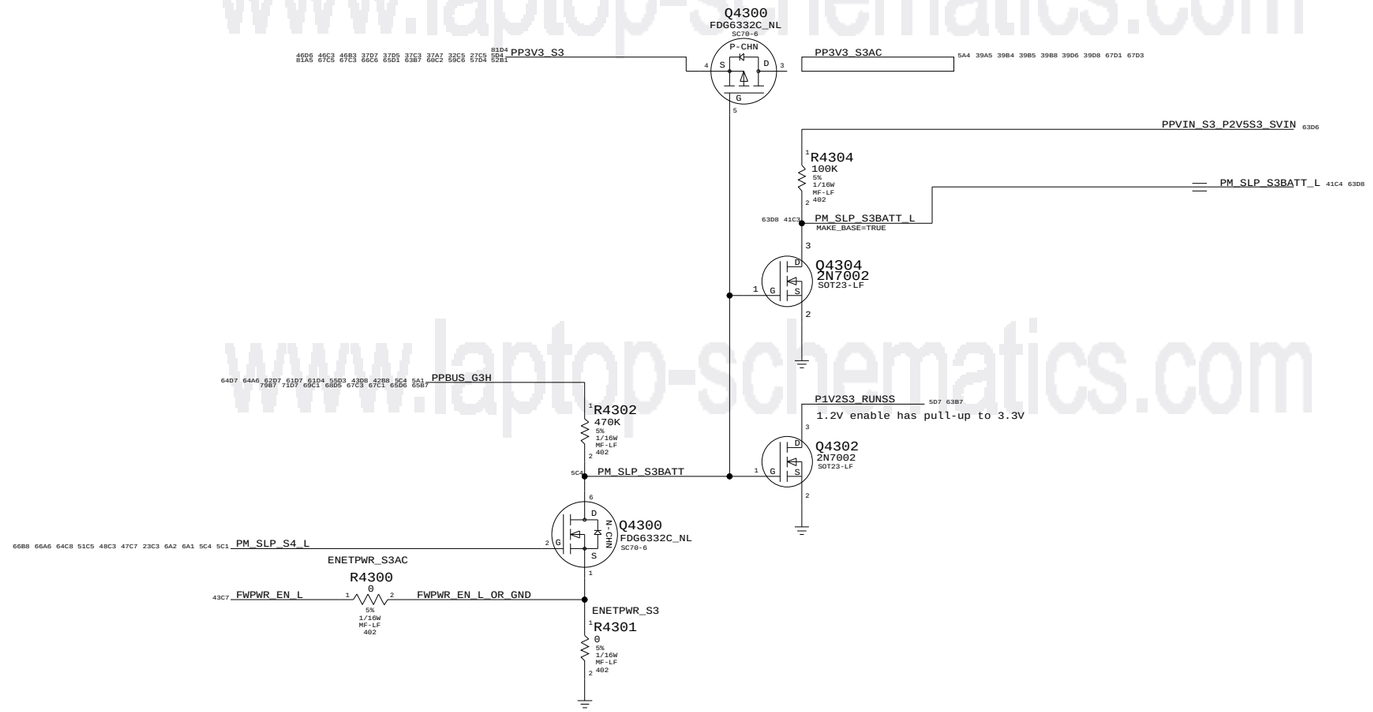
SCALE NONE	SHT 40 OF 87	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

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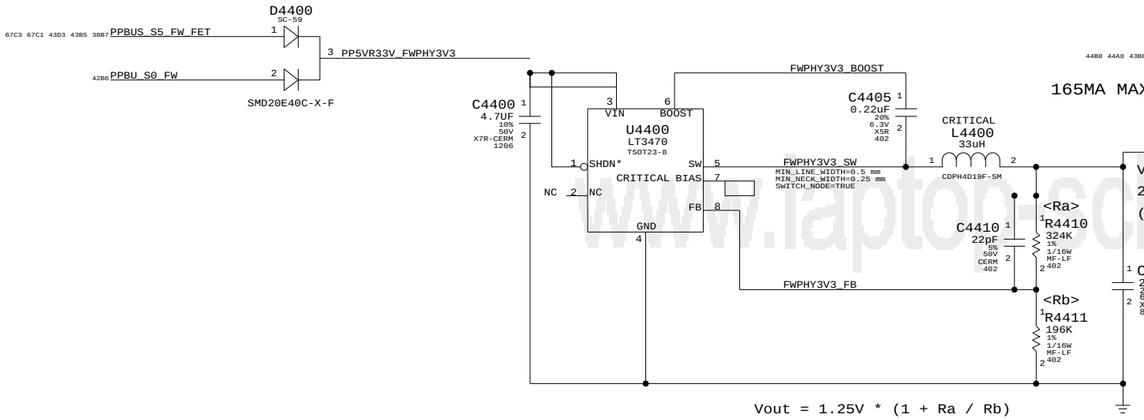
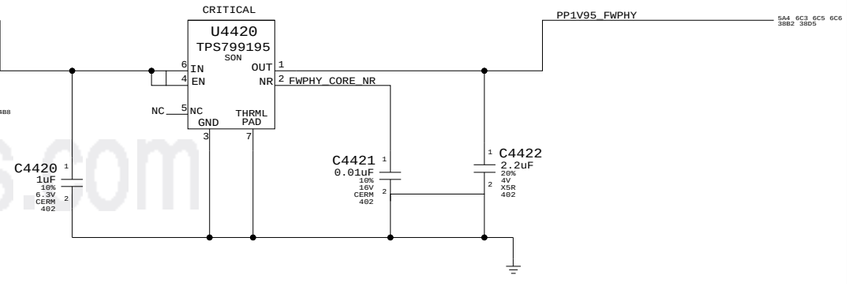
3.3V Supply for FWPHY



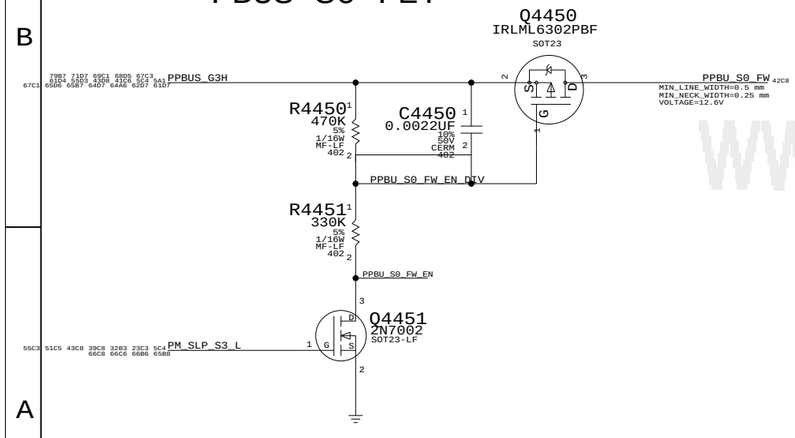
165MA MAX LOAD

1.95V Supply for FW PHY



Vout = 1.25V * (1 + Ra / Rb)

PBUS S0 FET



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FW PHY Power Supply

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D	051-7164	03001
SCALE: NONE	SHT 42 OF 87	

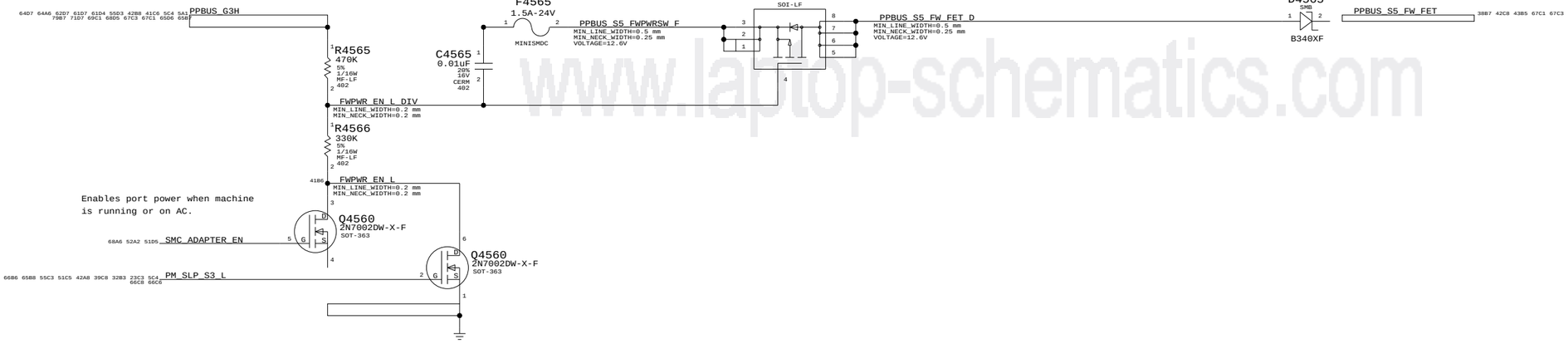
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

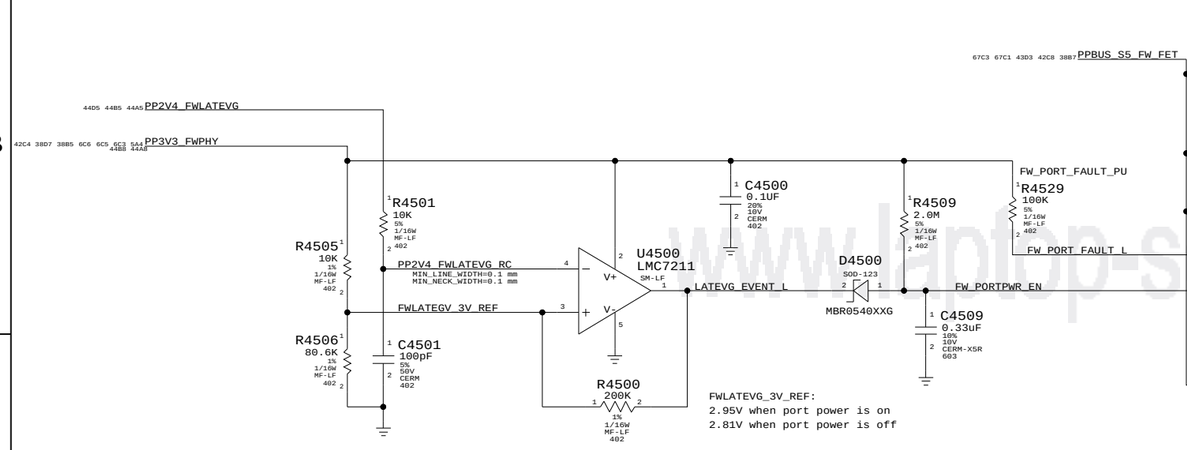
Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

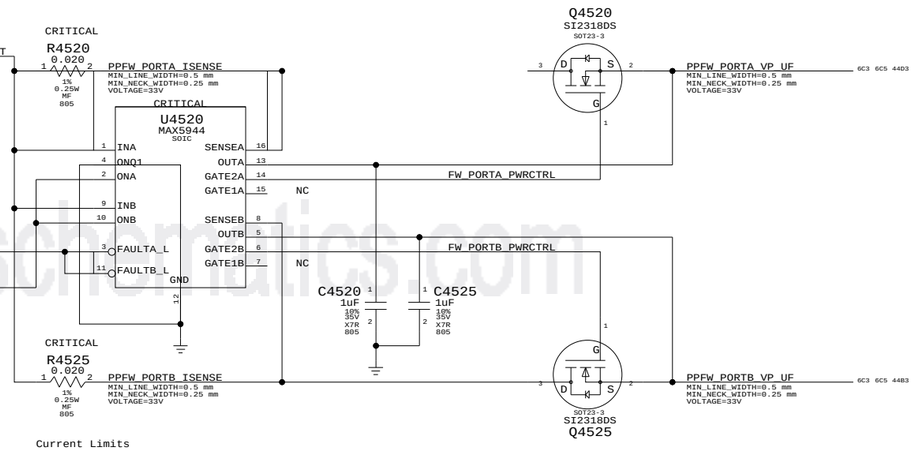
Port Power Switch



Late-VG Event Detection



Current Limit/Active Late-VG Protection



Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

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FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	38B3 44B5 44B7 44C5
	FW	FW_110D	FW_PORT1_TPA_N	38B3 44B5 44B7 44C5
BY	FW	FW_110D	FW_PORT1_TPB_P	38B3 44B5 44B7 44C5
	FW	FW_110D	FW_PORT1_TPB_N	38B3 44B5 44B7 44C5
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPA_FL_N	44B2
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_P	44B2
	FW	FW_110D	FW_PORT2_TPB_FL_N	44B2

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

Place close to FireWire PHY

38B3 FW_B_TPBIAS
38B3 FW_A_TPBIAS

C4650 1uF 10% 6.3V CERM 402 — VOLTAGE=1.234V

C4660 1uF 10% 6.3V CERM 402 — VOLTAGE=1.234V

TI PHYs require 1uF even though FW spec calls out 0.33uF

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topolgy

OMIT L4660 0 5% 1/16W MF-LF 402 — FW_B_TPA_L_P VOLTAGE=1.234V

OMIT L4661 0 5% 1/16W MF-LF 402 — FW_B_TPA_L_N VOLTAGE=1.234V

R4650 56.2 1% 1/16W MF-LF 402
R4651 56.2 1% 1/16W MF-LF 402
R4660 56.2 1% 1/16W MF-LF 402
R4661 56.2 1% 1/16W MF-LF 402

44C5 44B4 38B3 FW_PORT2_TPA_P — FW_PORT2_TPA_P 38B3 44B4 44C7 MAKE_BASE=TRUE
44C5 44B4 38B3 FW_PORT2_TPA_N — FW_PORT2_TPA_N 38B3 44B4 44C7 MAKE_BASE=TRUE
44C5 44B4 38B3 FW_PORT2_TPB_P — FW_PORT2_TPB_P 38B3 44B4 44C7 MAKE_BASE=TRUE
44C5 44B4 38B3 FW_PORT2_TPB_N — FW_PORT2_TPB_N 38B3 44B4 44C7 MAKE_BASE=TRUE
44D7 44C5 44B5 38B3 FW_PORT1_TPA_P — FW_PORT1_TPA_P 38B3 44B7 44C5 44D7 MAKE_BASE=TRUE
44D7 44C5 44B5 38B3 FW_PORT1_TPA_N — FW_PORT1_TPA_N 38B3 44B7 44C5 44D7 MAKE_BASE=TRUE
44D7 44C5 44B5 38B3 FW_PORT1_TPB_P — FW_PORT1_TPB_P 38B3 44B7 44C5 44D7 MAKE_BASE=TRUE
44D7 44C5 44B5 38B3 FW_PORT1_TPB_N — FW_PORT1_TPB_N 38B3 44B7 44C5 44D7 43B8 44D5 44A5 MAKE_BASE=TRUE

R4652 56.2 1% 1/16W MF-LF 402
R4653 56.2 1% 1/16W MF-LF 402
R4662 56.2 1% 1/16W MF-LF 402
R4663 56.2 1% 1/16W MF-LF 402

FW_B_TPB_L_N VOLTAGE=1.234V — FW_B_TPB_L_P VOLTAGE=1.234V

OMIT L4662 0 5% 1/16W MF-LF 402 — OMIT L4663 0 5% 1/16W MF-LF 402

FW_PORT2_TPB_C VOLTAGE=1.234V — FW_PORT1_TPB_C VOLTAGE=1.234V

C4654 220pF 5% 25V CERM 402
R4654 4.99K 1% 1/16W MF-LF 402
C4664 220pF 5% 25V CERM 402
R4664 4.99K 1% 1/16W MF-LF 402

Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

44B8 44A8 43B8 42C4 38D7 38B5 6C6 6C5 6C3 5A4 PP3V3_FWPHY

38D7 38B5 6C6 6C5 6C3 5A4 44B8 44A8 43B8 42C4 PP3V3_FWPHY — PP3V3_FWPHY

Late-VG Protection Power

44B8 43B8 42C4 38D7 38B5 6C6 6C5 6C3 5A4 PP3V3_FWPHY

R4690 332 1% 1/16W MF-LF 402

PP2V4_FWLATEVG MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.4V — 43B8 44B5 44D5

C4691 0.01UF 10% 50V X7R 402

CRITICAL D4690 MMBZ5227B SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail

Cable Power

43B2 6C5 6C3 PPFW_PORTA_VP_UF — L4620 FERR-250-OHM SM — PPFW_PORT1_VP MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4624 0.001uF 20% 50V CERM 402

Note:Trace PPFW_PORT1_VP should handle up to 5A

"Snapback" & "Late VG" Protection

44B5 44A5 43B8 PP2V4_FWLATEVG

DP4620 BAV99DW-X-F SOT-363
C4621 0.01uF 10% 50V X7R 402
DP4620 BAV99DW-X-F SOT-363
C4620 0.01uF 10% 50V X7R 402

44D7 44B7 44B5 38B3 FW_PORT1_TPB_N
44D7 44B7 44B5 38B3 FW_PORT1_TPB_P
44D7 44B7 44B5 38B3 FW_PORT1_TPA_N
44D7 44B7 44B5 38B3 FW_PORT1_TPA_P

DP4621 BAV99DW-X-F SOT-363
C4622 0.01uF 10% 50V X7R 402
DP4621 BAV99DW-X-F SOT-363
C4623 0.01uF 10% 50V X7R 402

C4629 0.1uF 10% 50V X7R 603-1 — Place C4629 close to pin 5 of connector

R4629 1M 5% 1/16W MF-LF 402

PORT 1 BILINGUAL

CRITICAL J4620 1394B-UG31903 F-RT-SM1

(FW_PORT1_BREF)
(PPFW_PORT1_VP)
(GND_FW_PORT1_VG)
FW_PORT1_AREF

TPB- TPB<R> TPB+ VP NC VG TPA- TPA<R> TPA+ — OUTPUT / INPUT

514S0133

C4625 0.01uF 20% 50V CERM 603
NO STUFF C4627 0.01uF 20% 16V CERM 402
C4626 0.01uF 20% 16V CERM 402

GND_CHASSIS_ENET 6A6 6A8 40B2 44A1

Cable Power

43A2 6C5 6C3 PPFW_PORTB_VP_UF — L4630 FERR-250-OHM SM — PPFW_PORT2_VP MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=33V

C4634 0.001uF 20% 50V CERM 402

"Snapback" & "Late VG" Protection

PP2V4_FWLATEVG

DP4630 BAV99DW-X-F SOT-363
C4630 0.01uF 10% 50V X7R 402
DP4630 BAV99DW-X-F SOT-363
C4631 0.01uF 10% 50V X7R 402

44C7 44C5 38B5 FW_PORT2_TPA_P
44C7 44C5 38B5 FW_PORT2_TPA_N
44C7 44C5 38B5 FW_PORT2_TPB_P
44C7 44C5 38B5 FW_PORT2_TPB_N

FL4630 1210-45R1 90-OHM-100MA
FL4631 1210-45R1 90-OHM-100MA

DP4631 BAV99DW-X-F SOT-363
C4632 0.01uF 10% 50V X7R 402
DP4631 BAV99DW-X-F SOT-363
C4633 0.01uF 10% 50V X7R 402

44D7 FW_PORT2_TPA_FL_P
44D7 FW_PORT2_TPA_FL_N
44D7 FW_PORT2_TPB_FL_P
44D7 FW_PORT2_TPB_FL_N
(PPFW_PORT2_VP)
(GND_FW_PORT2_VG)

PORT 2 1394A

CRITICAL J4630 1394A F-RT-TH-LF

TPO (TPA+) TPO# (TPA-) TPI (TPB+) TPI# (TPB-) VP VGND

514-0255

C4635 0.01uF 20% 50V CERM 603
C4636 0.01uF 20% 16V CERM 402

GND_CHASSIS_USB 47B2 6A6 6A8 44A3
GND_CHASSIS_ENET 44C1 6A6 6A8 40B2

R4699 0 5% 1/16W MF-LF 402 — GND_CHASSIS_USB 6A6 6A8 44A1 47B2

FireWire Ports

SYNC_MASTER=M59_MLB SYNC_DATE=06/27/2006

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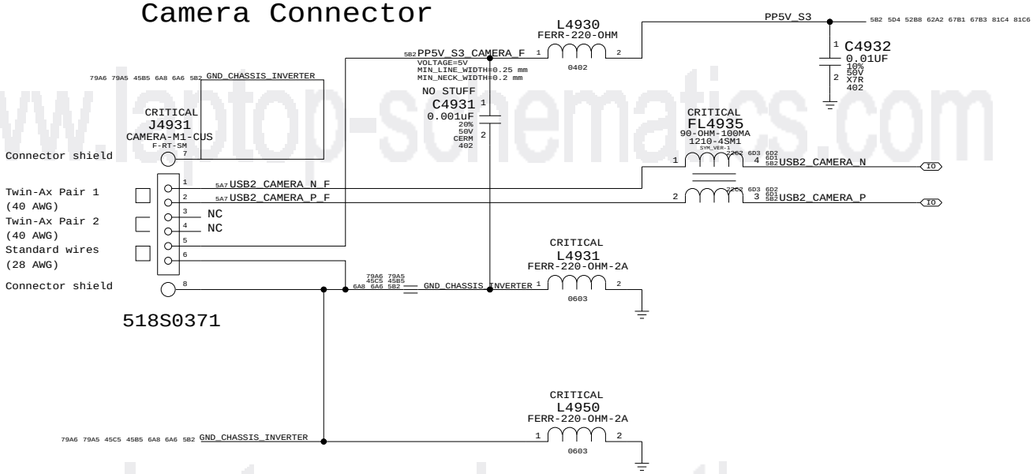
D	051-7164	03001
SCALE: NONE	SHT 44 OF 87	

Camera Connector



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Camera Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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SCALE: NONE

SHT 45 OF 87

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PP1V8_USB_HUB_INTERNAL_VDD18
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

PP1V8_USB_HUB_INTERNAL_VDD18PLL
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

C5000 0.1UF 20% 10V CERM 402
C5005 0.1UF 20% 10V CERM 402
C5012 4.7UF 20% 6.3V CERM 603
C5008 0.1UF 20% 10V CERM 402
C5010 4.7UF 20% 6.3V CERM 603

PP3V3_S3

C5003 0.1UF 20% 10V CERM 402
C5004 0.1UF 20% 10V CERM 402
C5011 4.7UF 20% 6.3V CERM 603
C5007 0.1UF 20% 10V CERM 402
C5014 4.7UF 20% 6.3V CERM 603
C5006 0.1UF 20% 10V CERM 402
C5013 4.7UF 20% 6.3V CERM 603

R5005 0 5% 1/16W MF-LF 402
FW_G_RST_L

VDDA33 VDDA33PLL VDD33CK 28 18 VDD18 VDD18PLL

CRITICAL
U5000 QFN
USB2502 2-PORT USB2.0 MISC

REG_EN High = internal 1.8V

TEST
ATEST/REG_EN
SELF_PWR
RESET*
CLKIN_EN
XTAL1/CLKIN
XTAL2
SDA/SMBDATA
SCL/SMBCLK/CFG_SEL0
CFG_SEL1
SERIAL PORT
VSS
THRML PAD

USBDP1 USB_IR_P
USBDN1 USB_IR_N
USBDP2 TP_USB2_3G_P
USBDN2 TP_USB2_3G_N
PRTPWR TP_USB_HUB_ENUM
PRTPWR_POL PP3V3_S3
GR1/NON_REM0 NC
GR2/NON_REM1 NC
OCS* NC
RBIAS USB_HUB_RBIAS
VBUS_DET PP3V3_S3
USBDP0 USB_HUB_P
USBDN0 USB_HUB_N

Test point should be on TOP side.
PRTPWR_POL High = PRTPWR goes high whenever USB HUB is enumerated
R4912 should be placed as close as possible to U4900.36 and isolated by 0.9mm from other signals.

R5012 12K 1% 1/16W MF-LF 402

R5001 1M 1% 1/16W MF-LF 402

Y5000 CRITICAL SM-2 24.000MHZ-12PF-60PPM
197S0162

C5001 12PF 5% 50V CERM 402
C5002 12PF 5% 50V CERM 402

USB_HUB_XTAL_OUT_R
R5006 0 5% 1/16W MF-LF 402
USB_HUB_XTAL_IN
USB_HUB_XTAL_OUT

SMBUS_SB_SDA
SMBUS_SB_SCL

311S0279

NO_3G
R5004 0 5% 1/16W MF-LF 402
USB_HUB_P
USB_HUB_N
USB_IR_P
USB_IR_N

NO_3G
R5003 0 5% 1/16W MF-LF 402

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Internal USB Hub

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT 46 OF 87	

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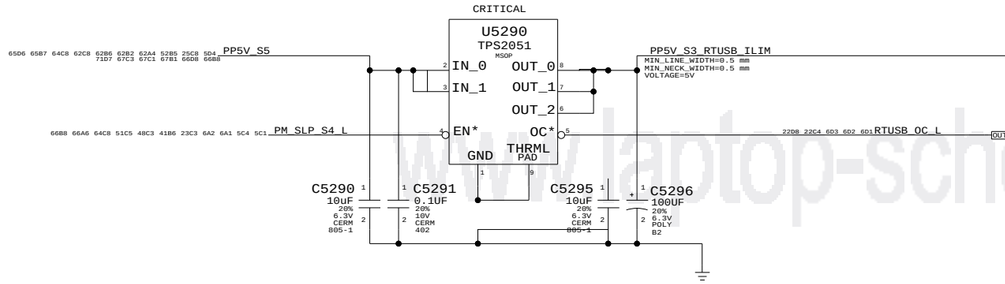
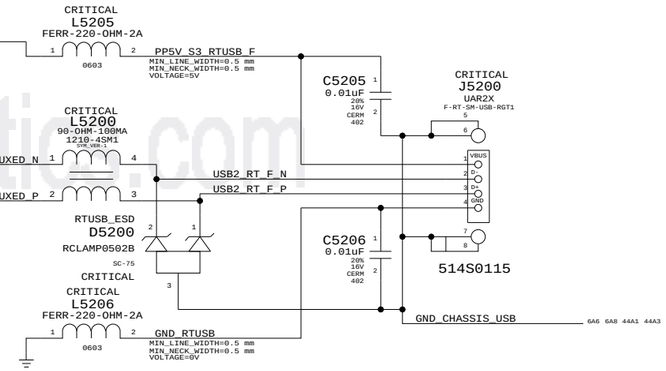
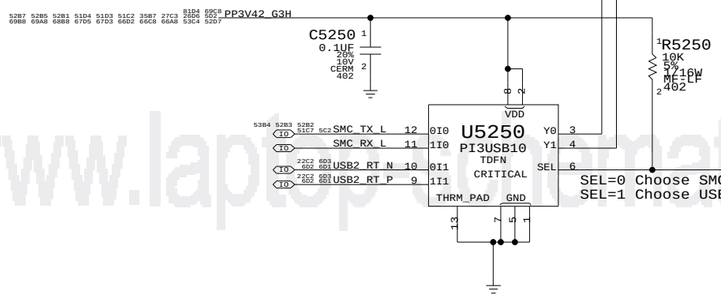
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

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External USB Connector

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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Left I/O Board Connector

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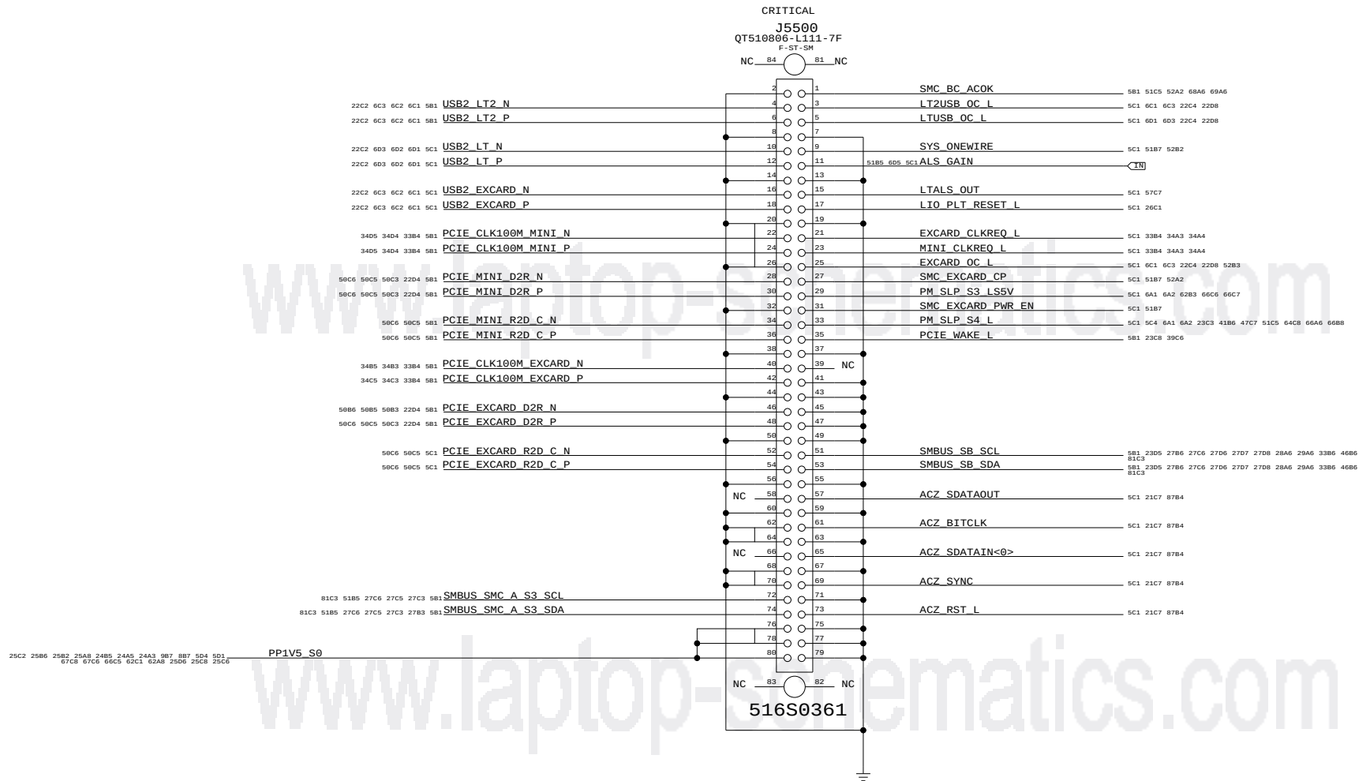

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Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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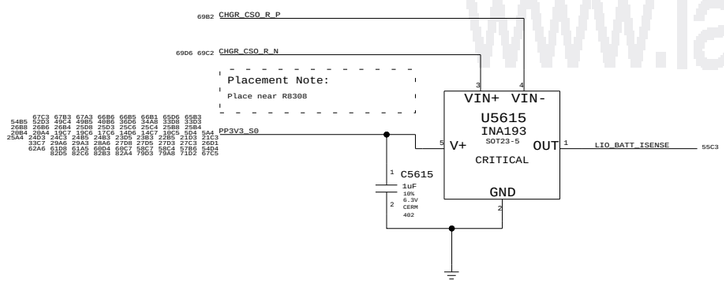
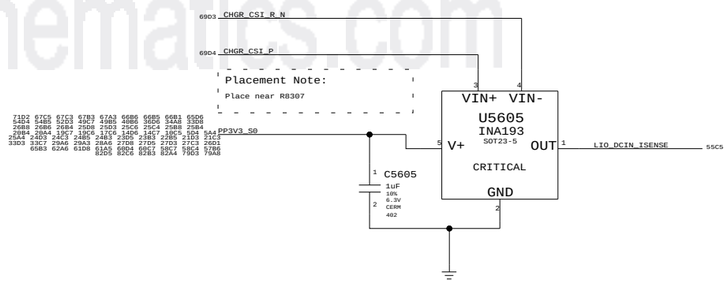
D	051-7164	03001

SCALE	SHT	OF
NONE	48	87

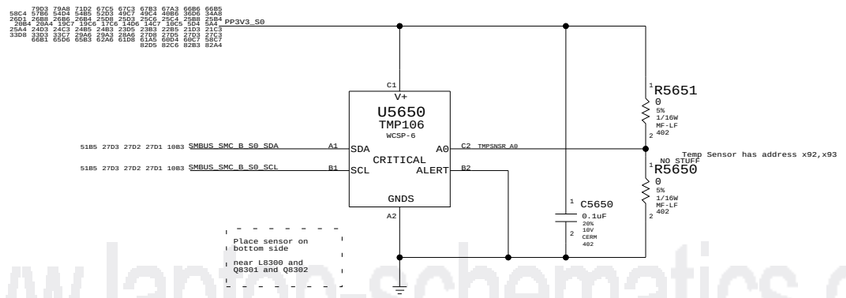
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



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Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT 49 OF 87	

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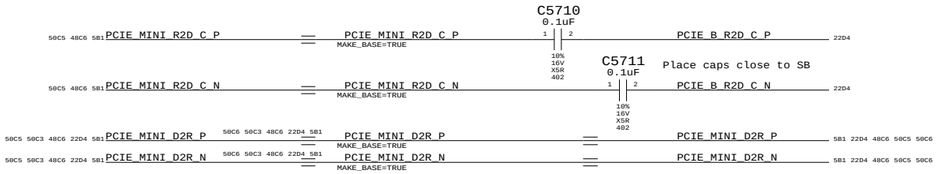
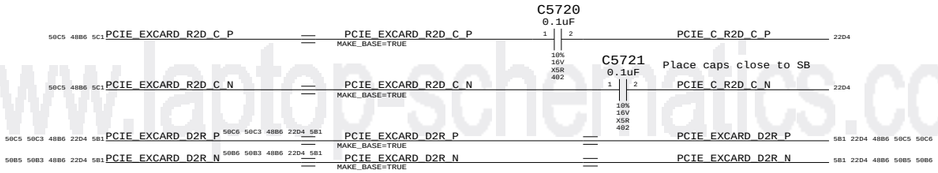
PCI-E x1 Port "A" = Ethernet (Yukon)

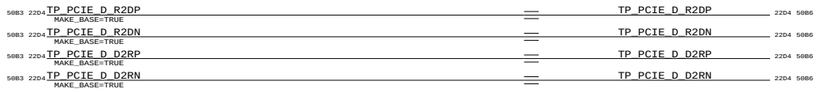
PCI-E x1 Port "B" = PCI-E Mini Card



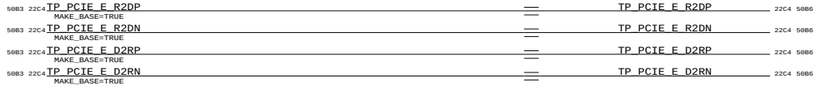
PCI-E x1 Port "C" = ExpressCard



PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused

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PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT 50 OF 87	

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE_XXX_IS_THE_PORT_NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13		SMC_PM_G2_EN
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14		SMC_ADAPTER_EN
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15		SPI_ARB
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12		SPI_SCLK
SMC_SB_NMI	B15	P14	P64/KIN4*	K13		SPI_SI
PM_RSMRST_L	C14	P15	P65/KIN5*	K14		SPI_SO
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12		SMC_PROCHOT_3_3_L
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13		FWH_INIT_L
TP_SMC_P20	D13	P20	P70/AN0	N12		SMC_CPU_ISENSE
TP_SMC_P21	D14	P21	P71/AN1	R13		SMC_CPU_VSENSE
TP_SMC_P22	D15	P22	P72/AN2	P13		SMC_GPU_ISENSE
TP_SMC_P23	E12	P23	P73/AN3	R14		SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14		SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15		SMC_PBUS_VSENSE
TP_SMC_P26	E13	P26	P76/AN6	N13		SMC_BATT_ISENSE
TP_SMC_P27	F14	P27	P77/AN7	P15		SMC_P1V5S0_NB_ISENSE
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7		SMC_WAKE_SCI_L
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7		SMC_TPM_GPIO
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7		PM_CLKRUN_L
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6		PM_SUS_STAT_L
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6		SC_TX_L
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6		SC_RX_L
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6		SMBUS_SMC_BSB_SCL
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4		SMC_ONOFF_L
TP_SMC_XDP_TMS	A5	P40/TMI0	P91/IRQ1*	J2		SMC_BC_ACOK
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1		SMC_BS_ALRT_L
SMBUS_SMC_BSB_SDA	D5	P42/SDA1	P93/IRQ12*	J3		PM_SLP_S3_L
SMC_TPM_PP	C3	P43/TMI1/EXSCKX1	P94/IRQ13*	J4		PM_SLP_S4_L
TP_SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2		PM_SLP_S5_L
TP_SMC_XDP_TCK	C2	P45	P96/EXCL	H1		SMC_CLK32K_SUSCLK
TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2		SMBUS_SMC_0_S0_SDA
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
SMC_TX_L	G1	P50				
SMC_RX_L	G4	P51				
SMBUS_SMC_0_S0_SCL	F2	P52/SCL0				

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3		SMC_CASE_OPEN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2		SMC_TCK
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1		SMC_TDI
SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4		SMC_TDO
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2		SMC_TMS
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		TP_SMC_PF0
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		TP_SMC_PF1
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6		SMC_LID
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6		SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6		SMC_BATT_ISET
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5		TP_SMC_BATT_VSET
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5		SMC_SYS_ISET
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5		TP_SMC_SYS_VSET
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9		SPI_CE_L
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9		SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9		SMBUS_SMC_BSA_SDA
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8		SMBUS_SMC_BSA_SCL
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8		SMBUS_SMC_A_S3_SDA
TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8		SMBUS_SMC_A_S3_SCL
TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7		SMBUS_SMC_B_S0_SDA
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7		SMBUS_SMC_B_S0_SCL
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1		SMC_PROCHOT
TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3		SMC_THRMTRIP
TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2		SMC_FWE
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4		ALS_GAIN
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4		SMS_INT_L
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3		SMS_ONOFF_L
TP_SMC_ANALOG_ID	N11	PD3/AN11				
SMC_P1V05S0_ISENSE	P10	PD4/AN12				
SMC_MEM_ISENSE	R10	PD5/AN13				
ALS_LEFT	N10	PD6/AN14				
ALS_RIGHT	M10	PD7/AN15				

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 10% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

PP3V42_G3H
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
PP3V42_G3H

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

AVCC	N14	VCC	P1
AVCC	N15	VCC	J15
VCC	P2	VCC	A1
VCC	F1	AVREF	M14
AVREF	M15		
SMC_RST_L	E3	RES*	
SMC_XTAL	A2	XTAL	
SMC_EXTAL	B2	EXTAL	
MD1	F2		
MD2	K1		
NMI	F4		
ETRST*	L1		
AVSS	P12		
AVSS	R12		
VSS	D1		
VSS	F4		
VSS	R4		
VSS	F12		
VSS	F13		
VSS	B13		
VSS	A13		
VSS	A4		
VSS	B4		
VSS	D2		

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
KBC_MDE
SMC_MD1
SMC_NMI
SMC_TRST_L
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800
SM
GND_SMC_AVSS

SMC

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SCALE: NONE

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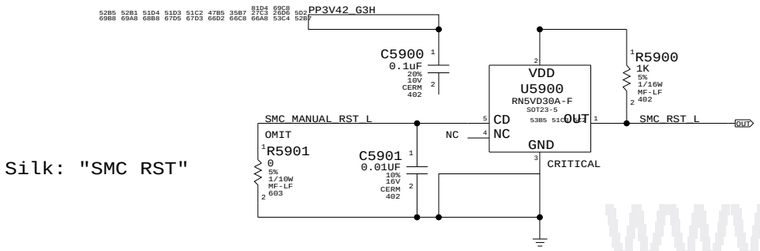
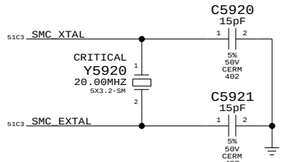
SMC Reset Button / Brownout Detect

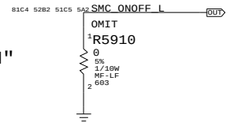


Silk: "SMC RST"

SMC Crystal Circuit

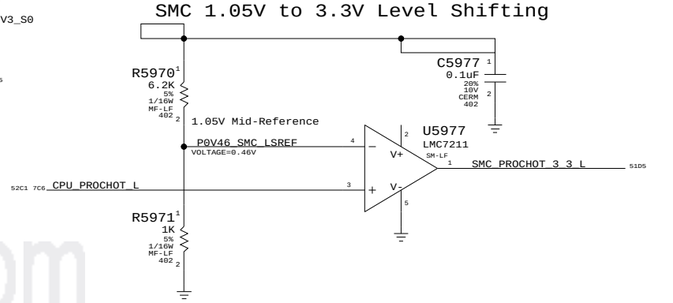


Debug Power Button

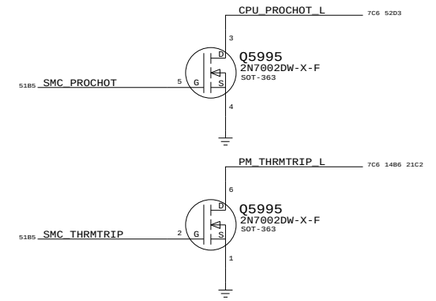


Silk: "PWR BTN"

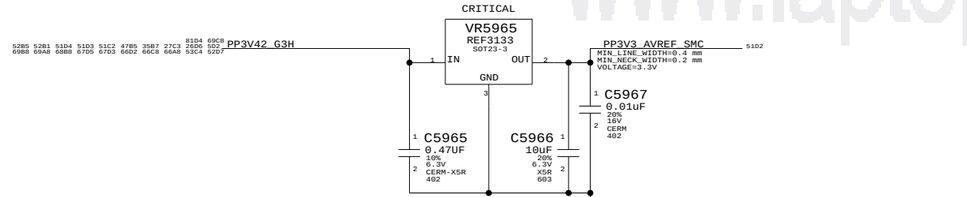
SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting

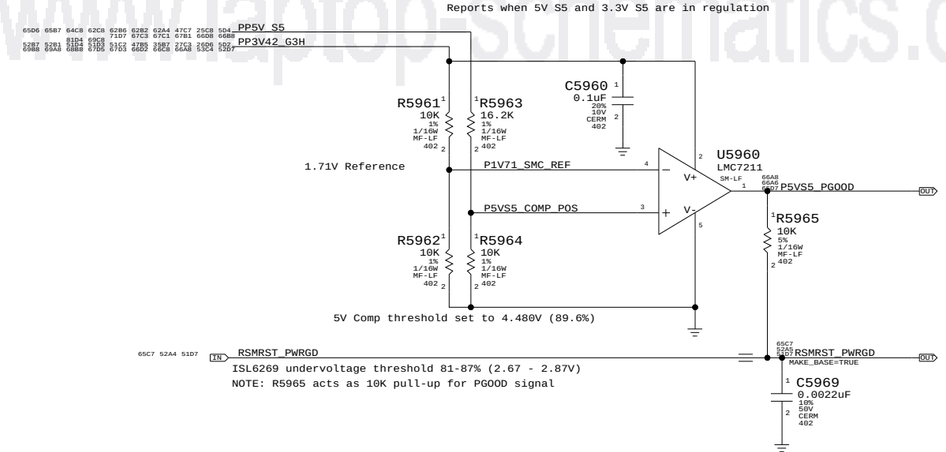


SMC AVREF Supply

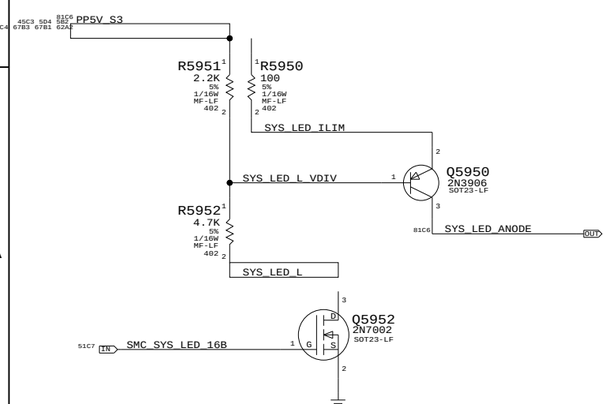


SMC PWRGD Circuit

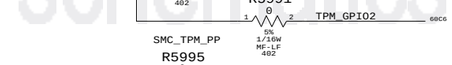
Reports when 5V S5 and 3.3V S5 are in regulation



System (Sleep) LED Circuit



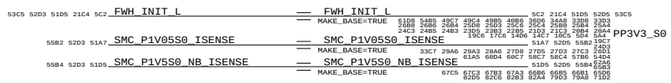
SMC_TPM_GPIO1



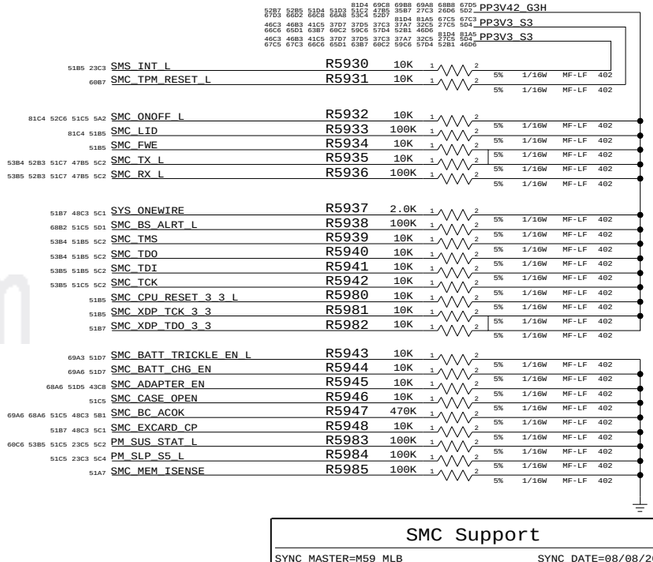
SMC_TPM_GPIO2

SMC_TPM_PP

PP3V3_S0



PP3V3_S3



SMC Support

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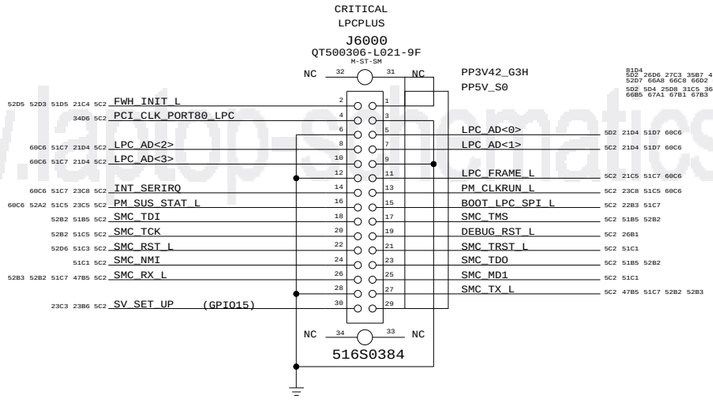

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LPC+ Debug Connector

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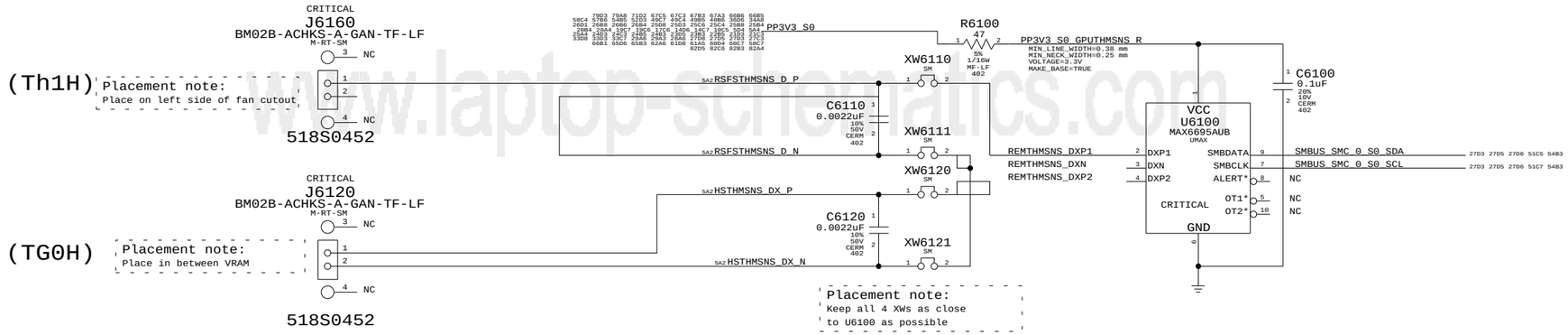
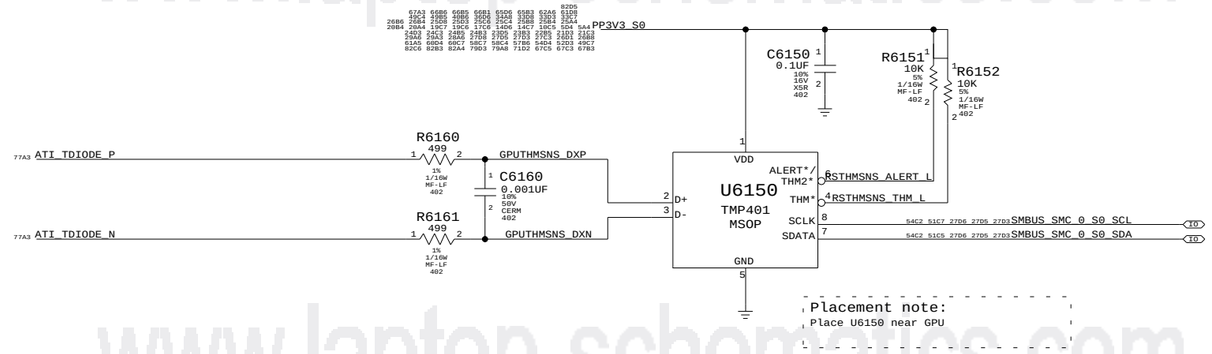
GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



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Thermal Sensors

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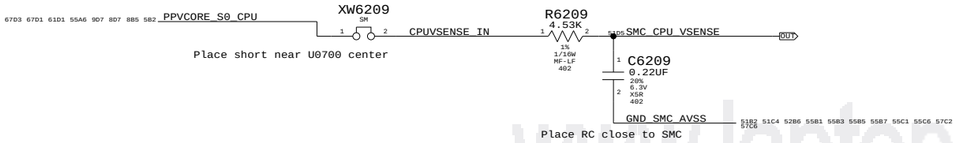
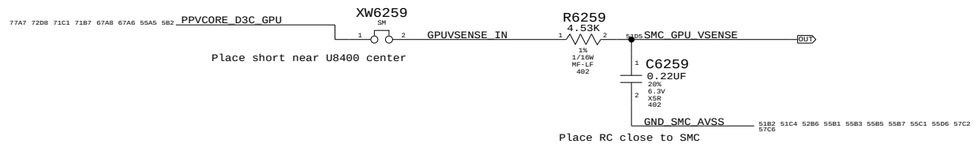
SCALE	SHT	OF
NONE	54	87

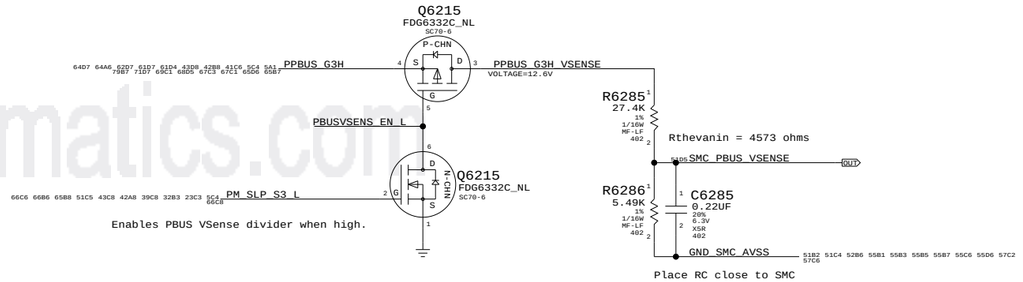
CPU Voltage Sense / Filter



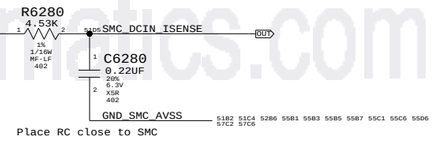
GPU Voltage Sense / Filter



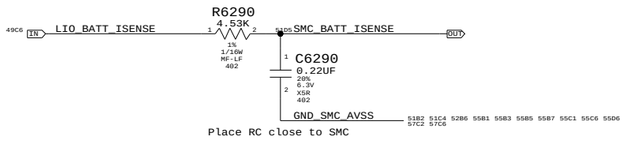
PBUS Voltage Sense Enable & Filter



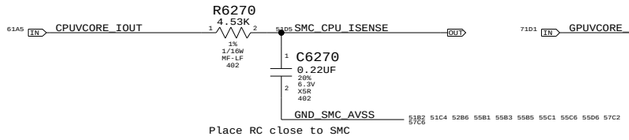
DCIN Current Sense Filter



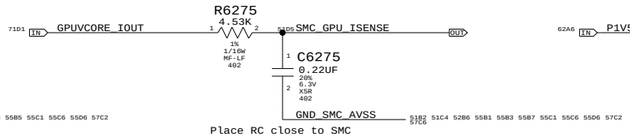
Battery Current Sense Filter



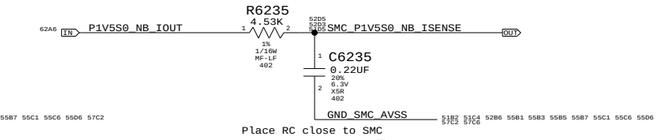
CPU Current Sense Filter



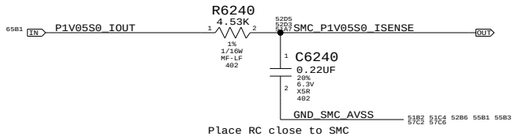
GPU Current Sense Filter



1.5V S0 (NB) Current Sense Filter

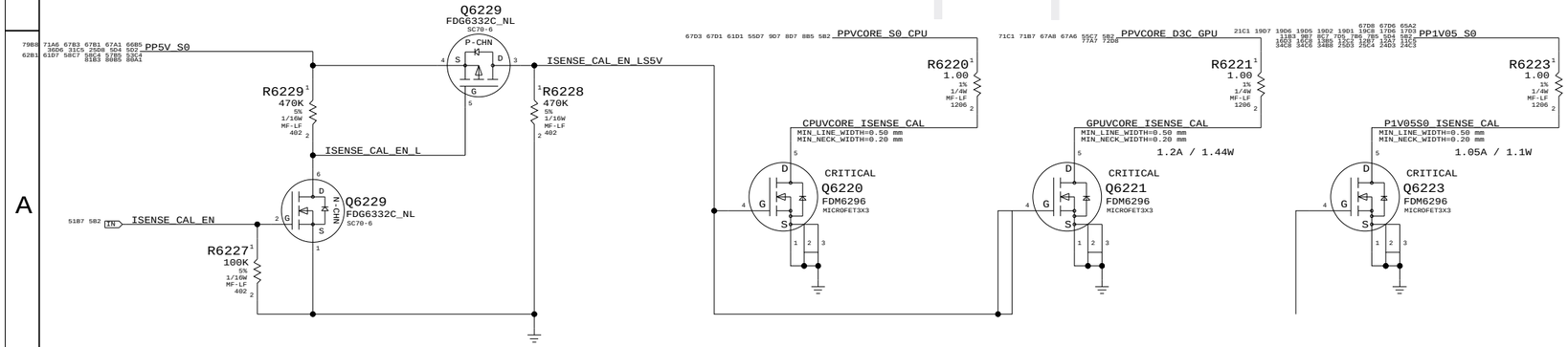


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



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Current & Voltage Sensing		
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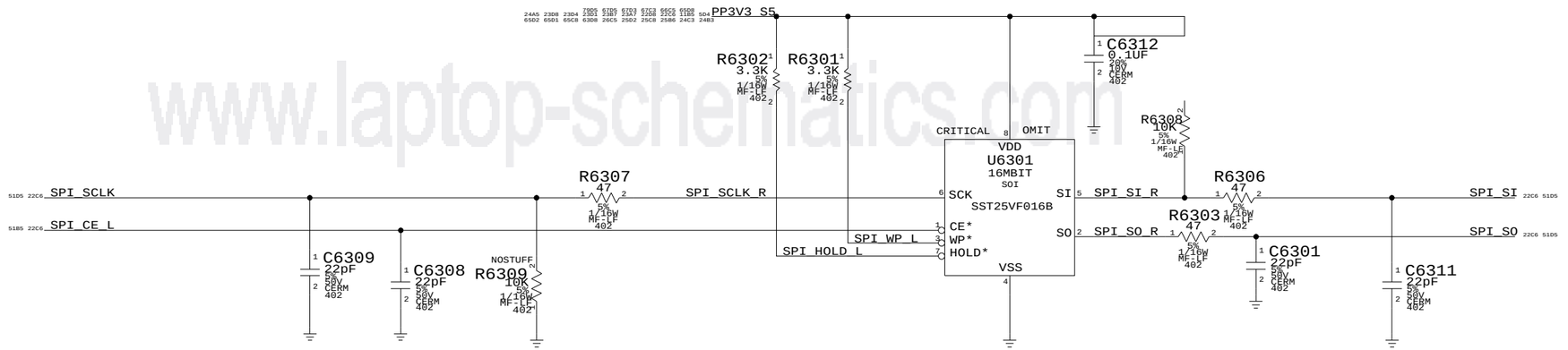
	SCALE: NONE	SHT 55 OF 87	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

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SPI BOOTROM

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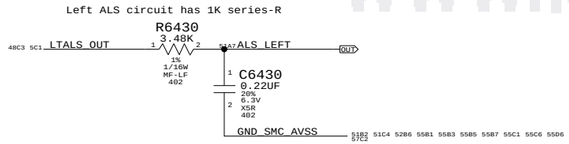
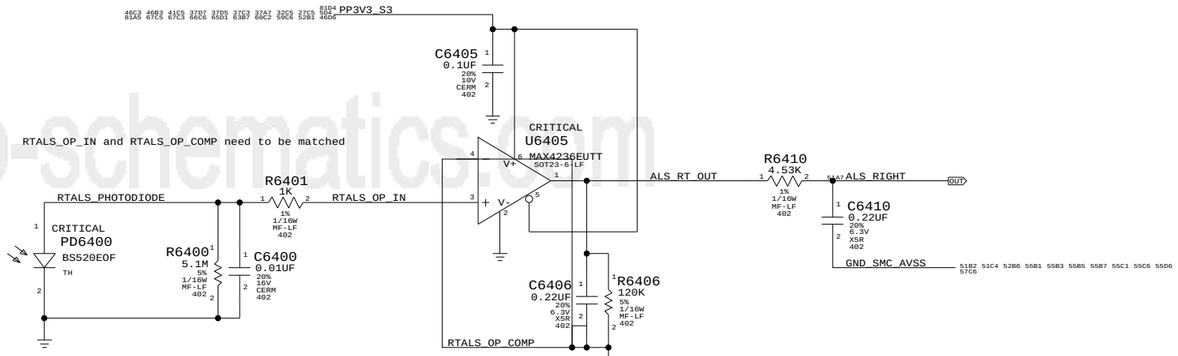
D	051-7164	03001

SCALE	SHT	OF
NONE	56	87

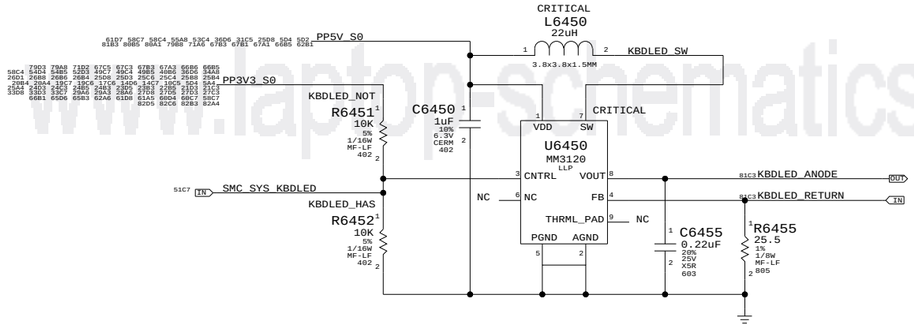
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



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ALS Support

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SCALE	SHT	OF
NONE	57	87

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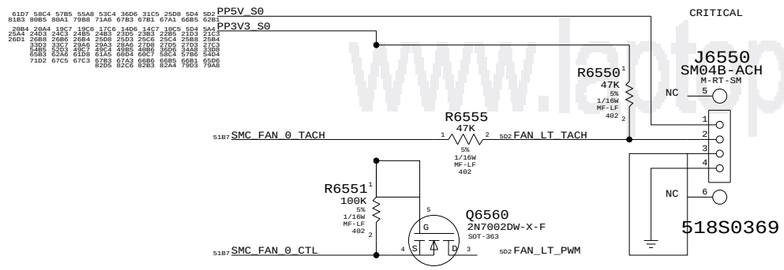
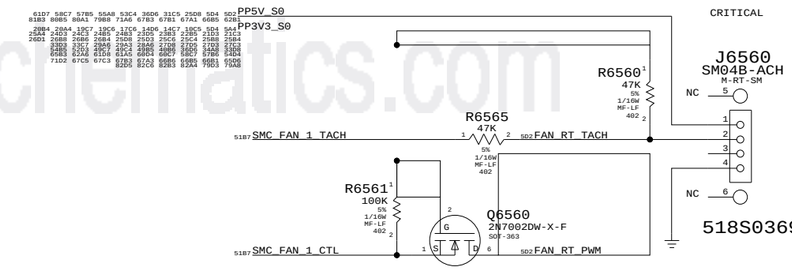
Left Fan



Right Fan



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Fan Connectors

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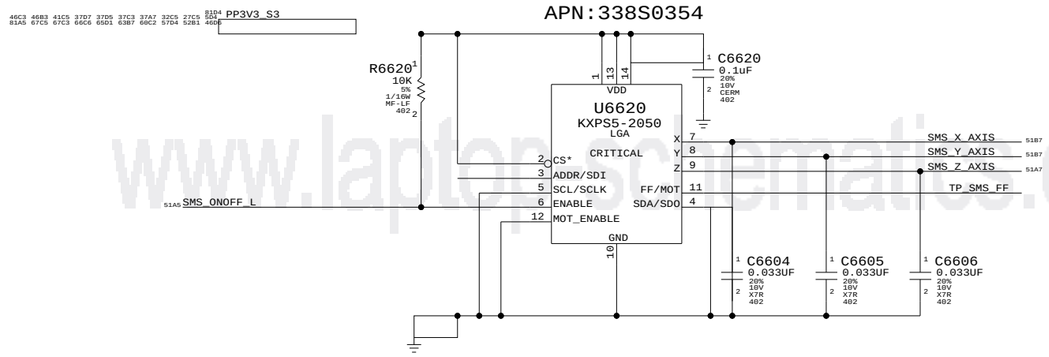
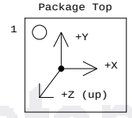
APN:338S0354



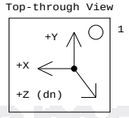
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M59 placement: Bottom-side

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Sudden Motion Sensor (SMS)

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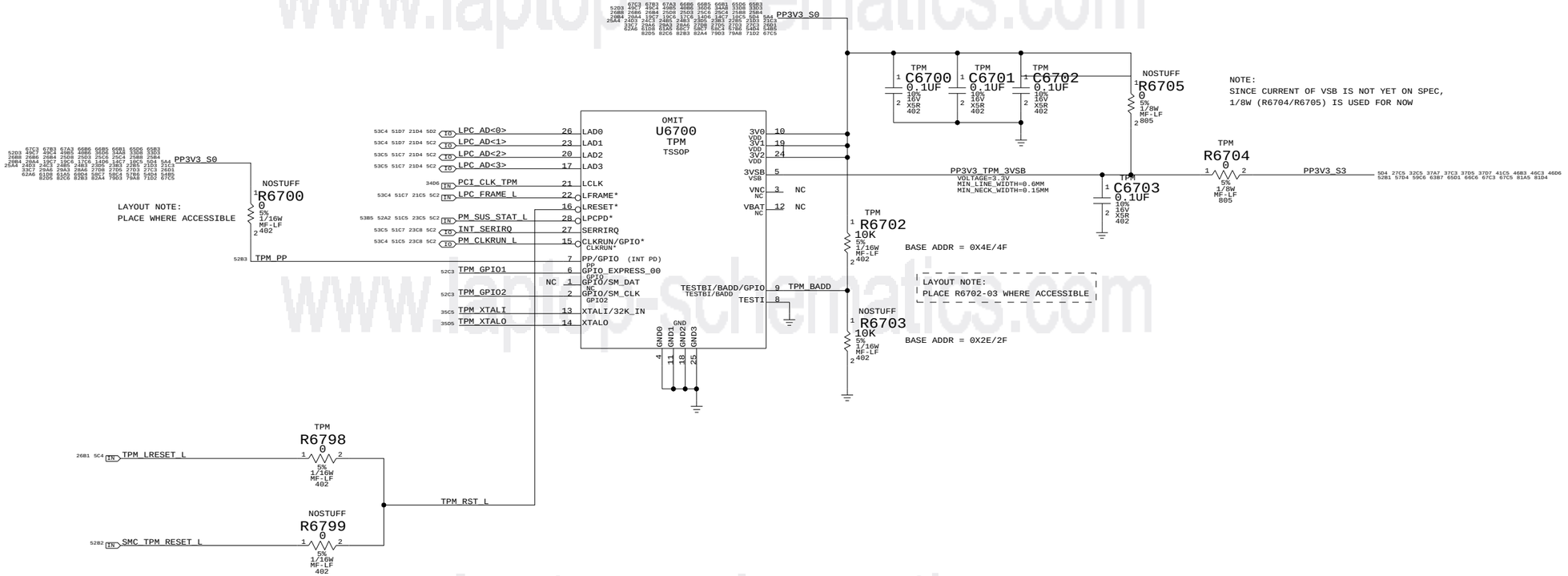

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TPM

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SCALE	SHT	OF
NONE	60	87

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DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

CPU VCore Current Sense

IMVP6 CPU VCore Regulator

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SCALE: NONE	SHT 61 OF 87	

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PPBUS_G3H

CRITICAL C7640 33uF 20% 16V POLY CASED2E-SM
C7641 1uF 10% 16V X5R 603
R7600 10 5% 1/16W MF-LF 402
CRITICAL C7680 33uF 20% 16V POLY CASED2E-SM
C7681 1uF 10% 16V X5R 603

R7623 4.02K 1% 1/16W MF-LF 402
C7623 0.1uF 10% 16V X5R 402
C7620 0.1uF 10% 16V X5R 402
R7620 4.53K 1% 1/16W MF-LF 402
R7629 23.7K 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

62B3 62D3 PP5V_S5_P5VP1V5_INTVCC
CRITICAL D7624 SOD-323 CMDSH-3
P5VS5_BOOST_RC
R7624 0 5% 1/16W MF-LF 402

PPVIN_S5_P5VP1V5_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12V
C7600 1uF 10% 16V X5R 603
R7630 1M 5% 1/16W MF-LF 402
R7670 1M 5% 1/16W MF-LF 402

CRITICAL Q7620 FDM6296 MICROFET3X3
C7624 0.1uF 20% 10V CERM 402
CRITICAL L7620 2.0UH SM-IHLP

PP5V_S5 Vout = 4.98V 11.5A max output (Q7621 limit)

CRITICAL C7652 150uF 20% 6.3V POLY CASE-C3
C7650 22UF 20% 6.3V CERM 805
C7651 22UF 20% 6.3V CERM 805

CRITICAL Q7621 FDM6296 MICROFET3X3
NO STUFF C7621 1000pF 10% 25V X7R 402

P5VS5_TG
P5VS5_BOOST
P5VS5_SW
P5VS5_BG
P5VS5_SNS_P
P5VS5_SNS_N
P5VS5_VOSNS
P5VS5_ITH
P5VS5_RUNSS

VIN
CRITICAL U7600 LTC3728LXC QFN

26	TG1	TG2	14
25	BOOST1	BOOST2	17
24	SW1	SW2	15
23	BG1	BG2	18
NC	PLLIN	PLLFLTR	2
30	SENSE1+	SENSE2+	12
29	SENSE1-	SENSE2-	11
1	VOSENSE1	VOSENSE2	9
5	ITH1	ITH2	8
28	RUN_SS1	RUN_SS2	13
4	FCB	3_3VOUT	7
21	EXTVCC	PGOOD	27
		INTVCC	20
		NC1	10
		NC2	16
		NC3	29
		NC4	32

SGND THRML_PAD PGND

P1V5S0_TG
P1V5S0_BOOST
P1V5S0_SW
P1V5S0_BG
62B3 P5VP1V5_FSEL
P1V5S0_SNS_R_P
P1V5S0_SNS_R_N
P1V5S0_VOSNS
P1V5S0_ITH
P1V5S0_RUNSS
NC

C7622 0.001uF 10% 50V CERM 402
C7626 47pF 5% 50V CERM 402
C7625 470pF 10% 50V CERM 402
P5VS5_ITH_RC
R7625 33K 5% 1/16W MF-LF 402
C7630 0.1uF 20% 10V CERM 402
C7607 0.01uF 10% 16V CERM 402
XW7600 SM

C7662 0.001uF 10% 50V CERM 402
C7665 470pF 5% 50V CERM 402
C7666 100pF 5% 50V CERM 402
P1V5S0_ITH_RC
C7670 0.1uF 20% 10V CERM 402
R7665 10K 1% 1/16W MF-LF 402

<Ra>
R7627 52.3K 1% 1/16W MF-LF 402
C7627 47PF 5% 50V CERM 402
<Rb>
R7628 10K 1% 1/16W MF-LF 402
NO STUFF C7628 1000pF 10% 25V X7R 402
GND_P5VP1V5_SGND VOLTAGE=0V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

TP_P5V_P1V5_PGOOD 66C1 66C2

Vout = 0.8V * (1 + Ra / Rb)

Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.

PP5V_S5_P5VP1V5_INTVCC 62D3 62D6
VOLTAGE=5V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm

P5VP1V5_SKIP
R7606 0 5% 1/16W MF-LF 402
P5VP1V5_FCB
P5VP1V5_CONT
R7607 0 5% 1/16W MF-LF 402
C7605 1uF 10% 6.3V CERM 402
C7601 4.7uF 20% 6.3V CERM 603
R7603 30K 5% 1/16W MF-LF 402
C7602 1uF 10% 6.3V CERM 402
R7604 10K 5% 1/16W MF-LF 402
C7604 0.01uF 10% 16V CERM 402

5V S0 FET

PP5V_S5
CRITICAL Q7660 FDM6296 MICROFET3X3
R7664 0 5% 1/16W MF-LF 402
C7664 0.1uF 20% 10V CERM 402
NO STUFF C7661 1000pF 10% 25V X7R 402
CRITICAL Q7661 IRF7832Z SO-8

R7660 3.65K 1% 1/16W MF-LF 402
C7660 0.1uF 10% 16V X5R 402
C7663 0.1uF 10% 16V X5R 402
R7663 909 1% 1/16W MF-LF 402
R7669 1.21K 1% 1/16W MF-LF 402
CRITICAL L7660 2.2uH-14A IHLP2525CZ-SM

PP1V5_S0 Vout = 1.49V 8A max output (L7660 & Q7660 limit)

C7690 22UF 20% 6.3V CERM 805
C7691 22UF 20% 6.3V CERM 805
CRITICAL C7692 330UF 20% 2.5V POLY CASE-D2E-LF

<Ra>
C7667 470pF 10% 50V CERM 402
R7667 34.0K 1% 1/16W MF-LF 402
<Rb>
NO STUFF C7668 1000pF 10% 25V X7R 402
R7668 39.2K 1% 1/16W MF-LF 402

5V S3 FET

PP5V_S5
CRITICAL Q7610 FDC638P SM-LF
PP5V_S3
C7610 0.0022uF 10% 50V CERM 402
R7610 100K 5% 1/16W MF-LF 402
PM_SLP_S4_LS5V
P5VS3_EN_L_RC

5V S0 FET

PP5V_S5
CRITICAL Q7615 IRF7707PBF TSSOP
R7615 100K 5% 1/16W MF-LF 402
PM_SLP_S3_LS5V
P5VS0_EN_L_RC
C7615 0.0022uF 10% 50V CERM 402
C7616 22UF 20% 6.3V CERM 805
C7617 22UF 20% 6.3V CERM 805
PP5V_S0

PP1V5_S0
R7675 0.002 1% 1/4W MF-LF 1206
PP1V5_S0_NB
C7672 22UF 20% 6.3V CERM 805
C7671 22UF 20% 6.3V CERM 805
C7675 0.1UF 10% 16V X5R 402
R7671 10 1% 1/16W MF-LF 402
Placement Note: PLACE C7675 NEAR U7670 PIN 7
PP3V3_S0
NB1V5_ISENSE_R1_N
NB1V5_ISENSE_R1_P
R7672 2.0K 1% 1/16W MF-LF 402
CRITICAL U7670 INA326EA-250 MSOP
P1V5S0_NB_IOUT
NB1V5_ISENSE_R2
R7674 100K 1% 1/16W MF-LF 402
C7674 0.001UF 10% 50V CERM 402

1	V+	R1-	2
7		R1+	3
4	V-	R2	5
6			

5V / 1.5V Power Supply

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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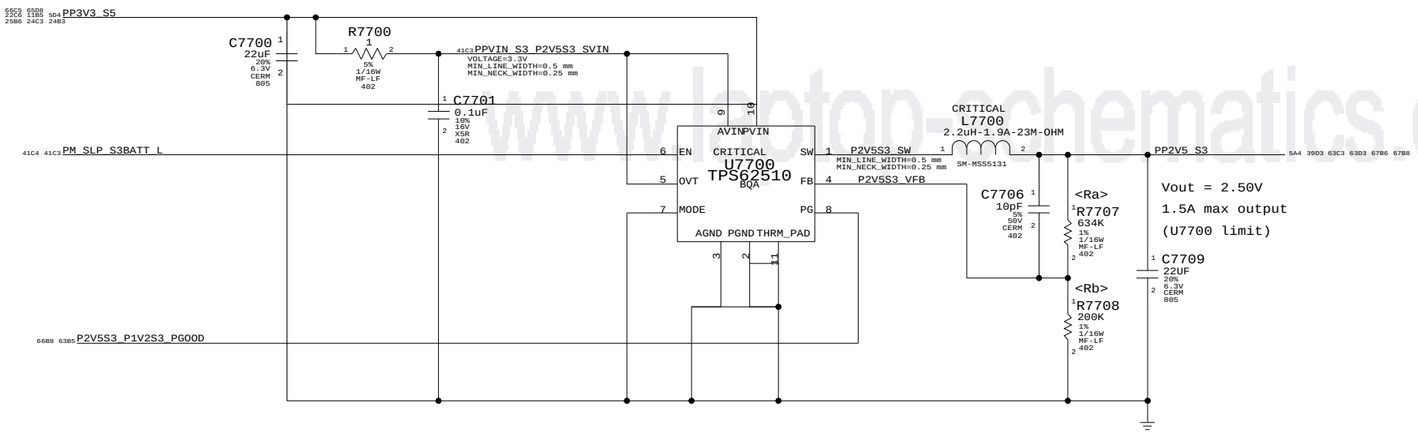
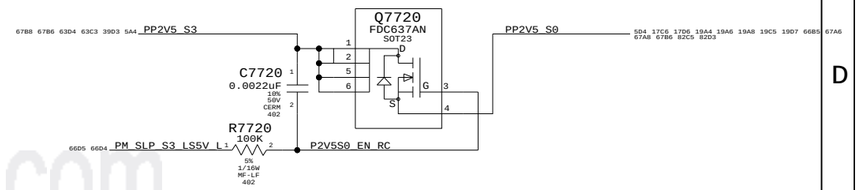
SCALE: NONE	SHT 62 OF 87	

2.5V S3 Regulator

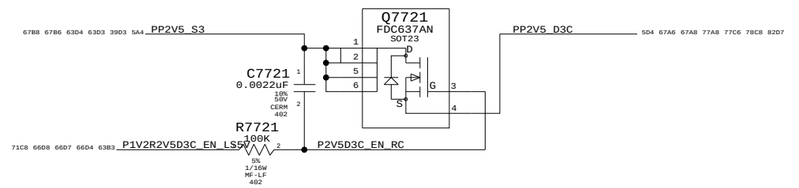


Vout = 0.6V * (1 + Ra / Rb)

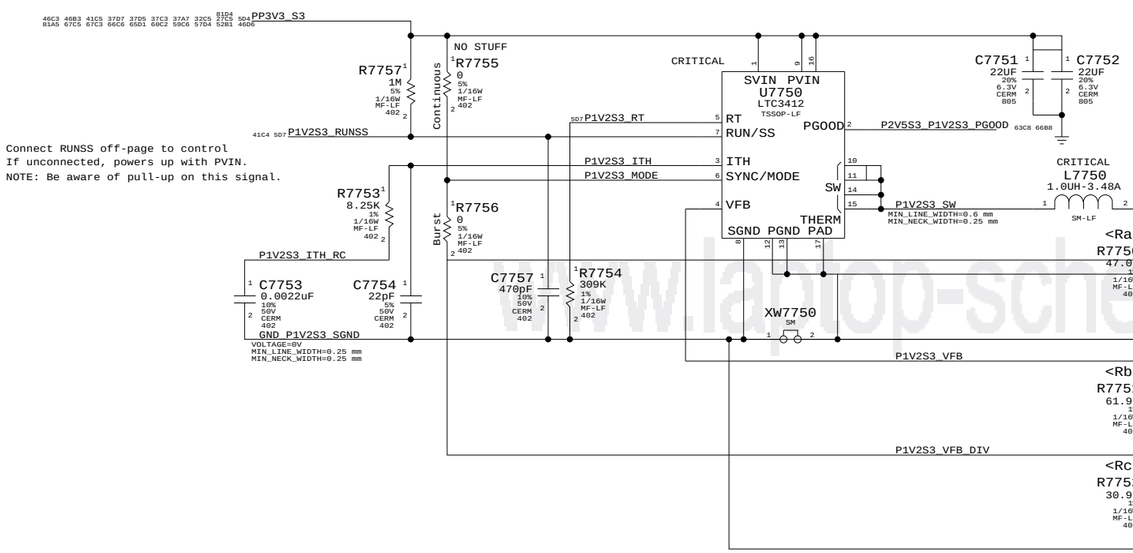
2.5V S0 FET



2.5V D3Cold FET

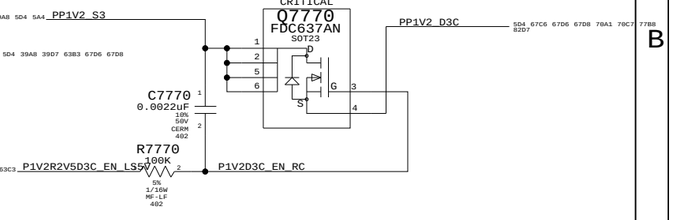


1.2V S3 Regulator



Vout = 0.8V * (1 + Ra / (Rb + Rc))

1.2V D3Cold FET



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2.5V & 1.2V Regulators

SYNC_MASTER=M59_MLB SYNC_DATE=08/08/2006

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SCALE: NONE	SHT 63 OF 87	

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PPBUS_G3H

PP5V_S5

C7800 1UF 10% 6.3V CERM 402

R7801 10 1% 1/10W MF-LF 402

C7801 4.7UF 20% 6.3V CERM 603

P1V8S3_V5FILT
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C7802 1uF 10% 16V X5R 603

C7830 33uF 20% 16V POLY CASED2E-SM

C7831 1uF 10% 16V X5R 603

C7832 1uF 10% 16V X5R 603

PM_SLP_S4_L

U7800
TPS51117RGY_QFN14
QFN

4	V5FILT	DRVH	13
10	V5DRV	DRVL	9
1	EN_PSV	LL	12
2	TON	VOUT	3
11	TRIP	PGOOD	6
14	VBST		
5	VFB		
THRM_PAD	GND	PGND	
15	7	8	

CRITICAL

P1V8S3_TON
P1V8S3_TRIP
P1V8S3_VBST

R7803 182K 1% 1/10W MF-LF 402

C7803 0.1UF 10% 16V X5R 402

R7804 12.1K 1% 1/16W MF-LF 402

P1V8S3_FB

P1V8S3_DRVH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

CRITICAL
Q7820
RJK0305DPB
LFPAK

P1V8S3_LL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

CRITICAL
L7820
1.2UH
FDA1055

P1V8S3_DRVL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

CRITICAL
Q7822
RJK0303DPB
LFPAK

CRITICAL
Q7821
RJK0303DPB
LFPAK

<Ra>
R7821 21K 1% 1/16W MF-LF 402

<Rb>
R7822 15K 5% 1/16W MF-LF 402

C7820 47PF 5% 50V CERM 402

(P1V8S3_FB)

C7842 330UF 20% 2.5V POLY CASE-D2E-LF

C7841 22UF 20% 6.3V CERM 805

C7843 330UF 20% 2.5V POLY CASE-D2E-LF

PP1V8_S3
Vout = 1.825V
18A max output
(L7820 limit)

Vout = 0.75V * (1 + Ra / Rb)

TP_P1V8S3_PGOOD

1.8V D3Cold FET

CRITICAL
Q7845
FDM6296
MICROFET3X3

PP1V8_S3
PPBUS_G3H
PP1V8_D3C

R7846 470K 5% 1/16W MF-LF 402

C7845 0.0022uF 10% 50V CERM 402

R7845 0 5% 1/16W MF-LF 402

P1V8D3C_EN
P1V8D3C_EN_RC

C7846 22UF 20% 6.3V CERM 805

C7847 22UF 20% 6.3V CERM 805

1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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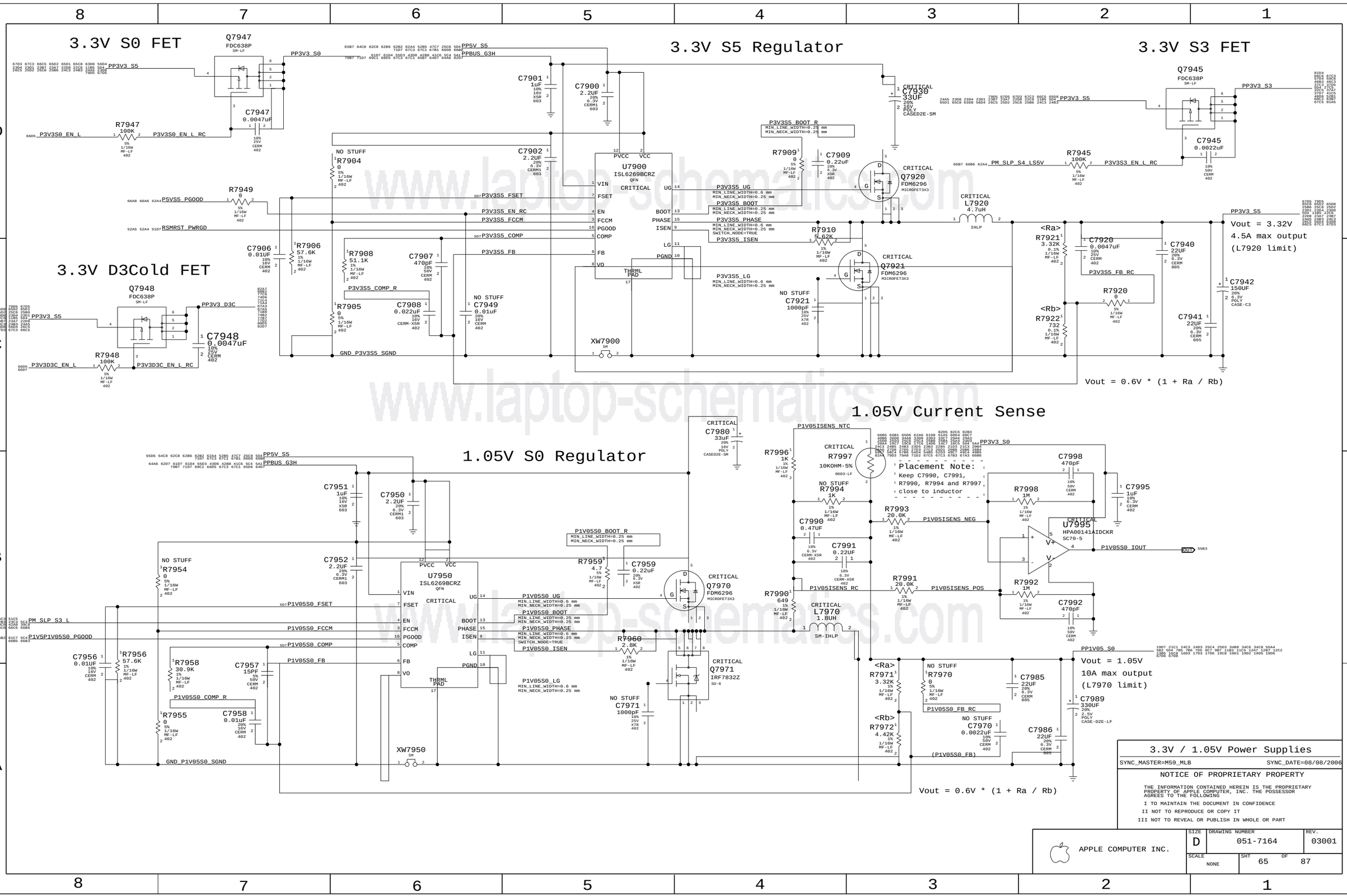
NONE	64	87



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Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

PP5V_S5

R8050 10K 5% 1/16W MF-LF 402

R8051 10K 5% 1/16W MF-LF 402

R8052 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

R8068 10K 5% 1/16W MF-LF 402

R8069 10K 5% 1/16W MF-LF 402

P1V2R2V5D3C_EN_LS5V (IN)

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V (MAKE_BASE=TRUE)

P3V3D3C_EN_L (MAKE_BASE=TRUE)

P1V8D3C_EN (MAKE_BASE=TRUE)

Q8055 2N7002DW-X-F SOT-363

Q8056 2N7002DW-X-F SOT-363

1.8V Enable has pull-up to PBUS

Q8050 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE)

P3V3S0_EN_L (MAKE_BASE=TRUE)

Q8058 2N7002DW-X-F SOT-363

Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE)

PM_SLP_S3_LS5V

PM_SLP_S3_LS5V

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363

R8054 100K 5% 1/16W MF-LF 402

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

PM_SLP_S3_L (IN)

R8056 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE

PP3V3_S3

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PM_SLP_S3_L

PP3V3_S0

C8081 0.1uF 20% 10V CERM 402

R8053 10K 5% 1/16W MF-LF 402

R8081 10K 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (IN)

P2V5S3_P1V2S3_PGOOD

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

NO STUFF R8060 0 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD MAKE_BASE=TRUE

PM_SLP_S3_L_GPUVCORE_EN

MC74VHC1G08 SC70

U8081

SB_GPUVCORE_DISABLE_L MAKE_BASE=TRUE

GPUVCORE_EN MAKE_BASE=TRUE

GPUVCORE_EN

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

PP5V_S5

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE)

PM_SLP_S4_LS5V

PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L (IN)

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) MAKE_BASE=TRUE

PM_SLP_S4_L

PM_SLP_S4_L

PM_SLP_S4_L

PP3V42_G3H

P5VS5_PGOOD (IN)

(P5VS5_PGOOD) MAKE_BASE=TRUE

P5VS5_PGOOD

P5VS5_RUNSS

5V Enable has pull-up to PBUS

R8059 470K 5% 1/16W MF-LF 402

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN (IN)

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

C8000 10UF 10% 25V X5R 1206-1

U8000 LT3470 TSOT23-8

VIN BOOST SHDN* SW BIAS NC NC CRITICAL FB GND

P3V42G3H5_BOOST

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

P3V42G3H_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE

P3V42G3H_FB

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402

<Rb> R8011 200K 1% 1/16W MF-LF 402

PP3V42_G3H

Vout = 3.425

200mA max output

(Switcher limit)

C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5

PP1V5_S0

R8061 27.4K 1% 1/16W MF-LF 402

R8063 4.99K 1% 1/16W MF-LF 402

0.89V Reference

P1V0_P1V5PG_REF

P1V5S0_COMP_POS

R8062 10K 1% 1/16W MF-LF 402

R8064 10K 1% 1/16W MF-LF 402

C8060 0.1uF 20% 10V CERM 402

U8060 LMC7211 SM-LF

P1V5S0_PGOOD

R8065 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5P1V05S0_PGOOD (OUT)

P1V5P1V05S0_PGOOD (IN)

P1V5P1V05S0_PGOOD MAKE_BASE=TRUE

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)

NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD — TP_P5V_P1V5_PGOOD MAKE_BASE=TRUE

TP_P1V8S3_PGOOD — TP_P1V8S3_PGOOD MAKE_BASE=TRUE

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

PP3V3_S0

PP5V_S0

PP2V5_S0

PP0V9_S0

R8074 68.1K 1% 1/16W MF-LF 402

R8072 365K 1% 1/16W MF-LF 402

R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

R8076 10K 5% 1/16W MF-LF 402

U8070 LTC2903 TSOT-23

V1 V2 V3 V4 RST* GND

CRITICAL

S0PGOOD_5V_DIV

S0PGOOD_2V5_DIV

S0PGOOD_0V9_DIV

S0PGOOD_PWROK

R8075 100K 1% 1/16W MF-LF 402

C8075 0.1UF 20% 10V CERM 402

R8073 100K 1% 1/16W MF-LF 402

C8073 0.1UF 20% 10V CERM 402

R8071 100K 1% 1/16W MF-LF 402

C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

PP3V3_S0

MC74VHC1G08 SC70

U8080

ALL_SYS_PWRGD (OUT)

PGOOD_MUXED_S0_OR_S0D3C

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0
PP1V05_S0
PP1V2_S3
PP1V2_D3C
PP1V5_S0
PP1V5_S0_NB
PP1V8_S3
PP1V8_D3C
PP2V5_S3
PP2V5_S0
PP2V5_D3C
PPVCORE_D3C_GPU
PPDCIN_G3H
GND
PP3V42_G3H
PP3V3_S5
PP3V3_S3
PP3V3_S0
PP3V3_D3C
PP3V3_S3AC
PPNBB_S0_GPU
PPBB_S0_GPU
PPVCORE_S0_CPU
PPBUS_G3H
PPBUS_S5_FW_FET
PP5V_S5
PP5V_S3
PP5V_S0

Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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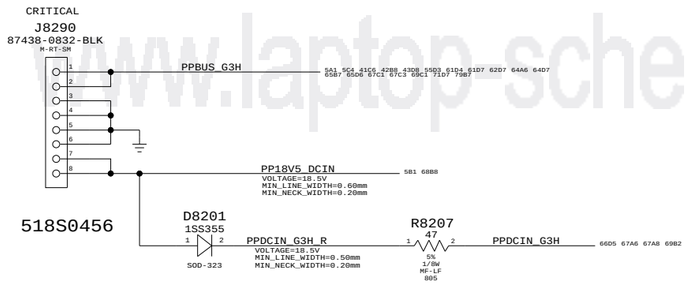
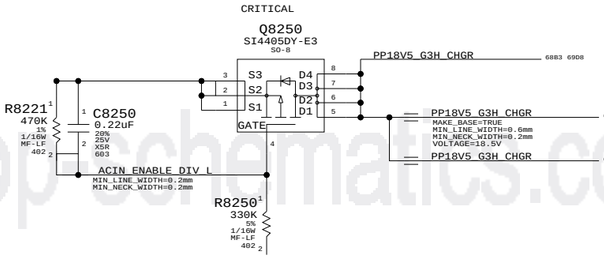
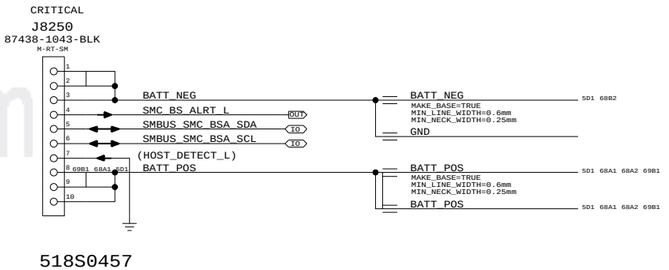
DC-In Connector



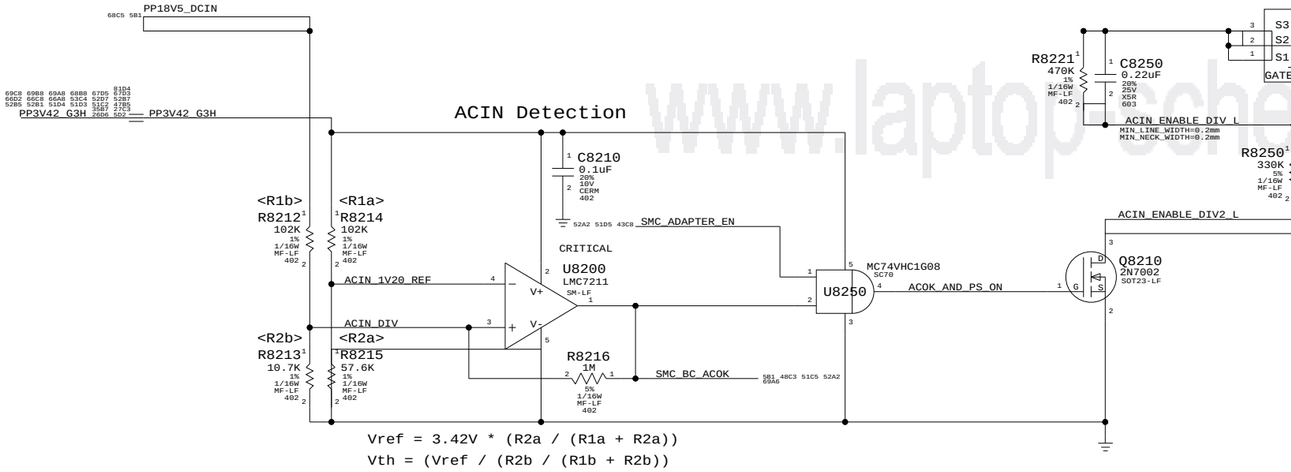
Inrush Limiter



Battery Connector



ACIN Detection



DC-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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PBus Supply & Battery Charger

Battery Charge FET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H,BATT CHGR,28P,QFN,LF	U8300	CRITICAL	ISL6257H
116S0004	1	0 OHM,5%,1/16W,0402,SMD,LF	R8304		ISL6257H

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

Adapter Input Current Limit

As shown, Isys =~4.6A max

Battery Charge Current Limit

As shown, Icng = 3.9A max

10A MAX, LIMITED BY L8300, Q8301

PBus Supply & Batt. Charger

SYNC_MASTER=MS9_LIO SYNC_DATE=08/08/2006

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SIZE D | DRAWING NUMBER 051-7164 | REV. 03001

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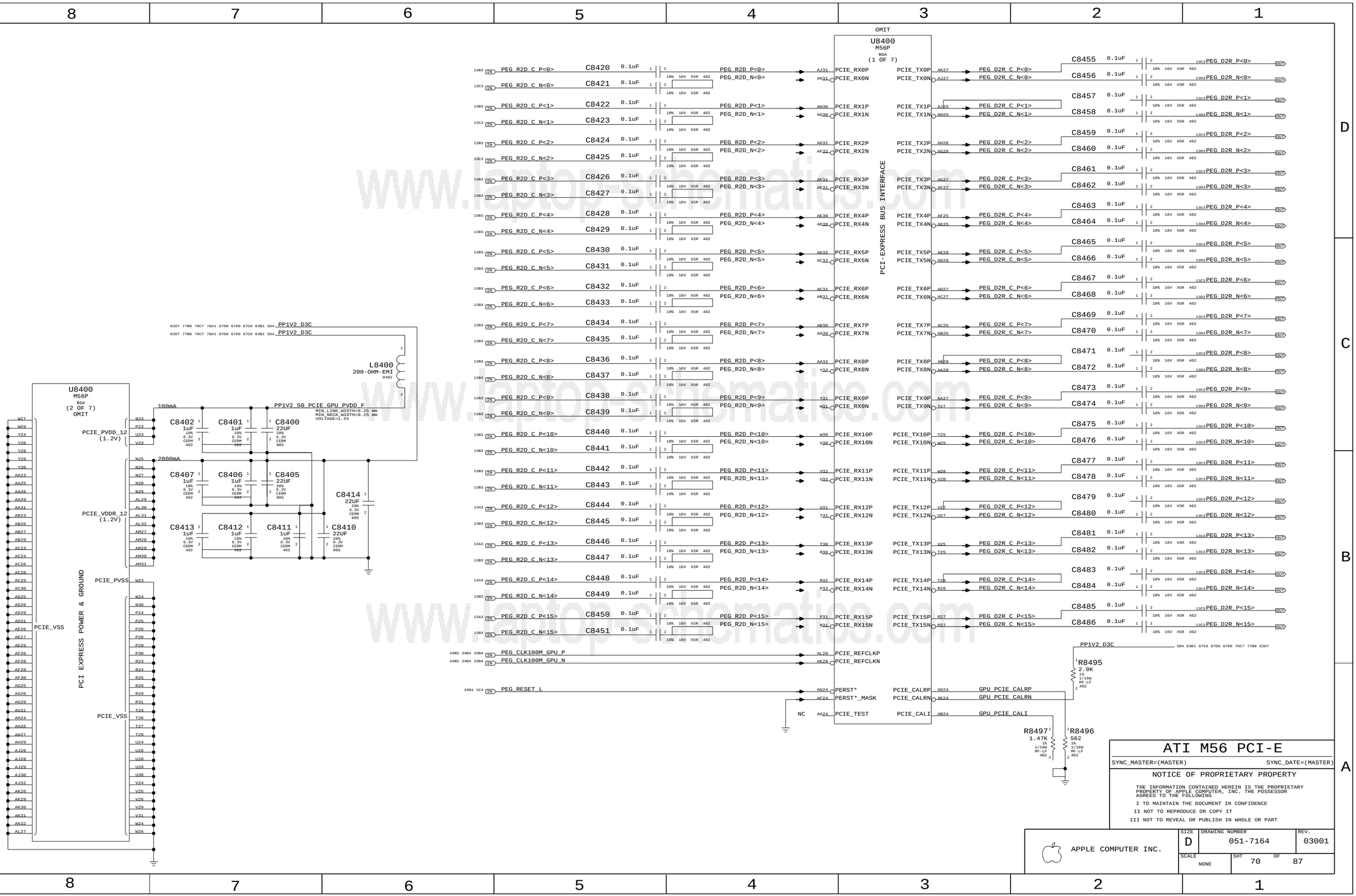

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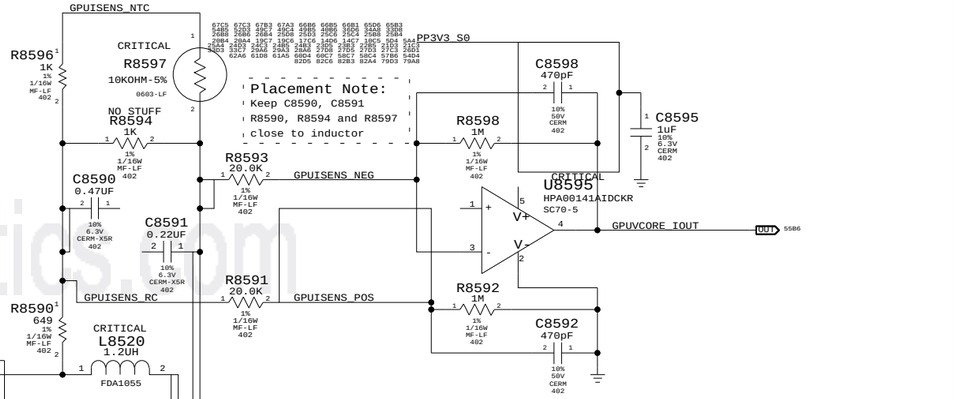
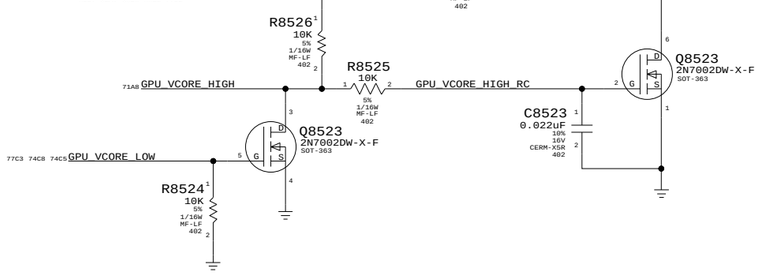
GPU VCore Current Sense



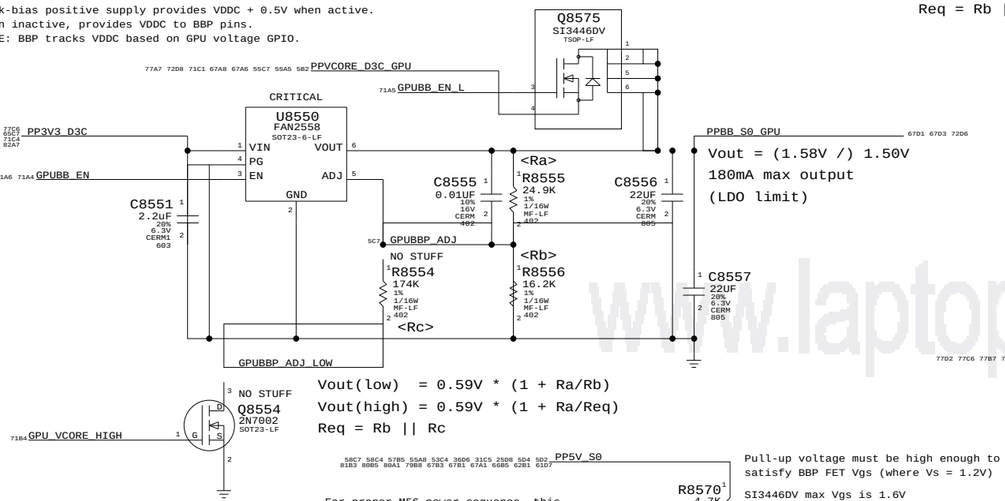
GPU VCore Supply

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

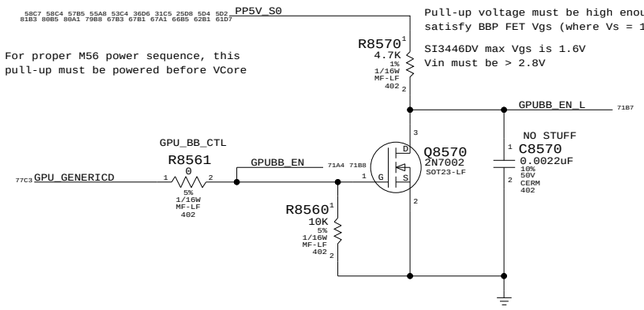


Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

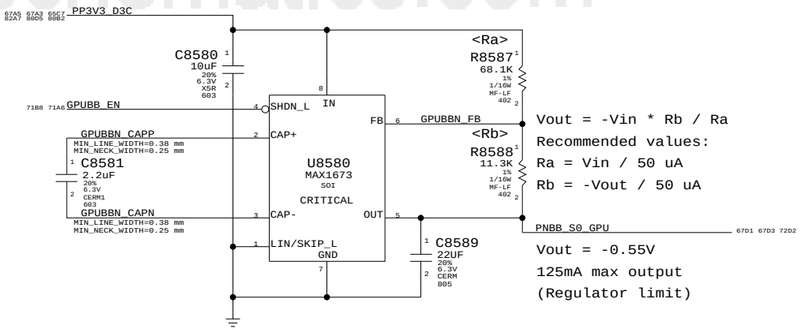


Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PPBB_S0_GPU
100mA (Preliminary)
C8690 22UF 20% 6.3V CERM 805
C8691 1uF 10% 6.3V CERM 402
C8692 0.1uF 10% 16V XSR 402

U8400
M56P
BGA
(7 OF 7)
OMIT
MEMORY & CORE POWER / GROUND

BBP
BBN

C8697 0.1uF 10% 16V XSR 402
C8696 1uF 10% 6.3V CERM 402
C8695 22UF 20% 6.3V CERM 805
100mA (Preliminary)
PNBB_S0_GPU

PPVCORE_D3C_GPU
14.2A @ 445/452MHz Core/Mem Clk for VDDC+VDDCI
C8600 22UF 20% 6.3V CERM 805
C8601 22UF 20% 6.3V CERM 805
C8604 C8605 C8606 C8607 C8608 C8609 C8610 1uF 10% 6.3V CERM 402
C8611 C8612 C8613 C8614 C8615 C8616 1uF 10% 6.3V CERM 402
R8630 0 5% 1/10W MF-LF 603

VDDC (1.0V/1.2V)

PPVCORE_S0_GPU_VDDCI
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
C8630 22UF 20% 6.3V CERM 805
C8631 C8632 C8633 C8634 1uF 10% 6.3V CERM 402

VDDCI (1.0V/1.2V)

PP1V8_D3C
2.0A @ 500MHz 1.8V GDDR3
C8650 C8651 C8652 C8653 22UF 20% 6.3V CERM 805
C8655 C8656 C8657 C8658 C8659 C8660 C8661 C8662 C8663 C8664 C8665 C8666 C8667 C8668 C8669 C8670 C8671 C8672 C8673 C8674 C8675 C8676 C8677 C8678 C8679 C8680 C8681 C8682 C8683 1uF 10% 6.3V CERM 402

VDDR1 (1.8V/2.0V)

VSS

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ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
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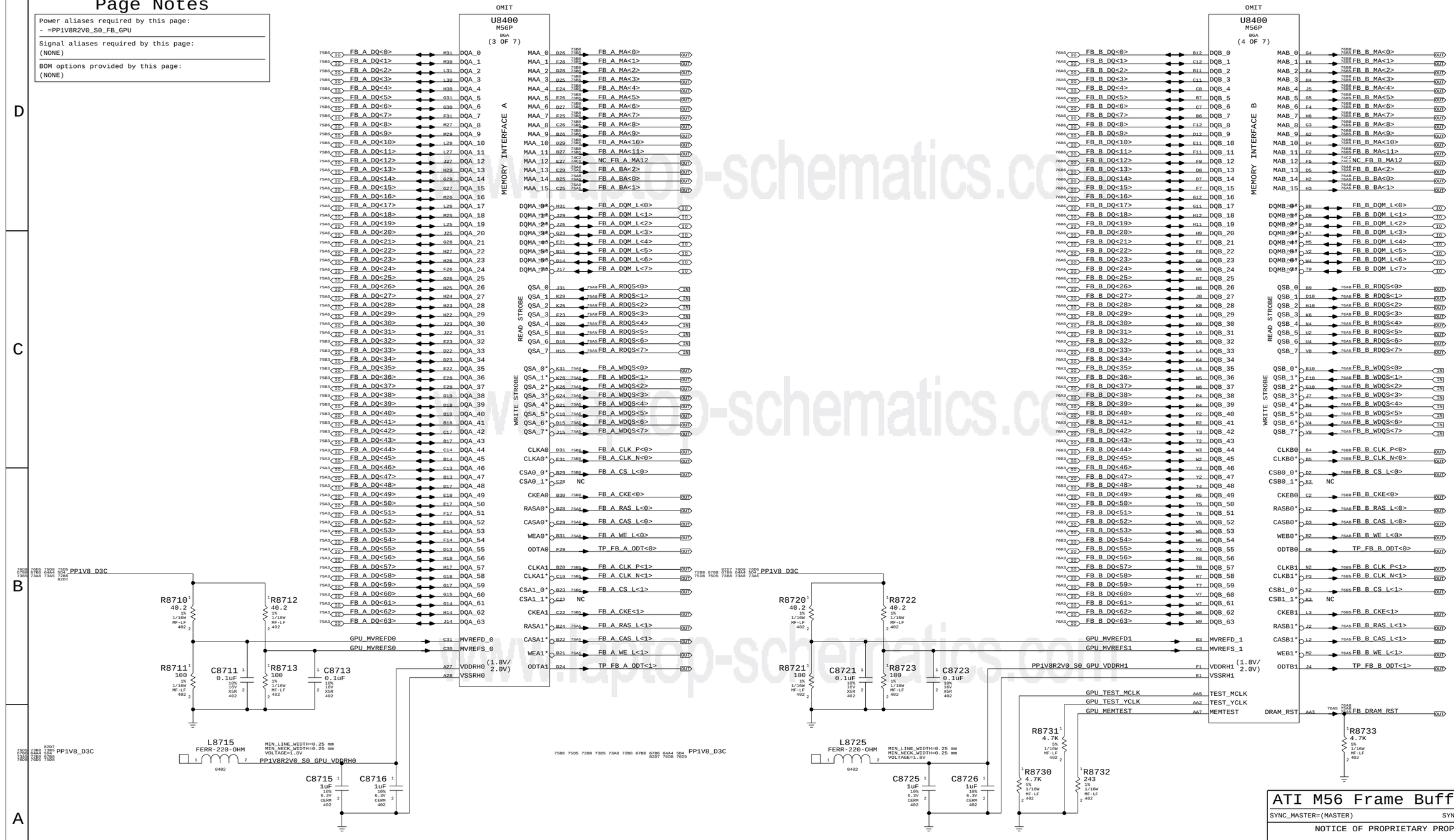
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



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ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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ROMCFGID[3..0]

0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

77D2 77C6 77B7 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8800 10K 5% 1/16W MF-LF 402
R8802 NO STUFF 10K 5% 1/16W MF-LF 402
R8804 NO STUFF 10K 5% 1/16W MF-LF 402
R8806 NO STUFF 10K 5% 1/16W MF-LF 402
R8809 NO STUFF 10K 5% 1/16W MF-LF 402
R8812 GPU_MEM_256M 10K 5% 1/16W MF-LF 402
R8824 GPU_MEM_256M 10K 5% 1/16W MF-LF 402

R8801 GPU_DEEPMH_EN 10K 5% 1/16W MF-LF 402
R8803 NO STUFF 10K 5% 1/16W MF-LF 402
R8805 10K 5% 1/16W MF-LF 402
R8808 NO STUFF 10K 5% 1/16W MF-LF 402
R8813 GPU_MEM_64M 10K 5% 1/16W MF-LF 402
R8811 NO STUFF 10K 5% 1/16W MF-LF 402
R8827 GPU_MEM_NOT_SAM 10K 5% 1/16W MF-LF 402

		Serial ROM	TestBus	Misc	Straps
77D3	GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
77D3	GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
77D3	GPU_GPIO_2		TESTIN[2]		Reserved
77D3	GPU_GPIO_3		TESTIN[3]		Reserved
77D3	GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
77D3	GPU_GPIO_5		TESTIN[5]		Reserved
77D3	GPU_GPIO_6		TESTIN[6]		Reserved
82A4 77D3 74C5	GPU_BLON	ENA_BL	TESTIN[7]		
77D3	GPU_GPIO_8	ROMSO	TESTWR		Reserved
77C3	GPU_GPIO_9	IPD	ROMSI		ROMIDCFG[3]
77C3 74C5	TP_GPU_GPIO_10		ROMSCK	TESTOUT[8]	
77C3	GPU_GPIO_11	IPD		TESTOUT[9]	ROMIDCFG[0]
77C3	GPU_GPIO_12	IPD		TESTOUT[10]	ROMIDCFG[1]
77C3	GPU_GPIO_13	IPD		TESTOUT[11]	ROMIDCFG[2]
77C3 74C5	NC_GPU_GPIO_14			TESTIN[8]	
77C3 74C5 71B4	GPU_VCORE_LOW			TESTIN[9] PWRCNTL	
77C3 74C5 34B4 34B2	GPU_CLK27MSS_IN			SS_IN	
77C3 74C5	NC_GPU_GPIO_17			Thm Mon Int	

GPU_BLON — MAKE_BASE=TRUE — 74C8 77D3 82A4

TP_GPU_GPIO_10 — MAKE_BASE=TRUE — 74C8 77C3

Required for debug access
Required for debug access
Required for debug access
Required for debug access

NC_GPU_GPIO_14 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3
GPU_VCORE_LOW — MAKE_BASE=TRUE — 71B4 74C8 77C3
GPU_CLK27MSS_IN — MAKE_BASE=TRUE — 34B2 34B4 74C8 77C3
NC_GPU_GPIO_17 — MAKE_BASE=TRUE NO_TEST=TRUE — 74C8 77C3

77D5 74B7 NC_GPU_GPIO_18 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_18 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_19 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_19 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_20 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_20 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_21 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_21 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_22 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_22 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_23 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_23 — 74B8 77D5
77D5 74B6 GPU_MEM_256M — 77D5 74B8 GPU_MEM_256M MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_25 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_25 — 74B8 77D5
77D5 74B7 NC_GPU_GPIO_26 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_26 — 74B8 77D5
77D5 74B6 GPU_MEMID — 77D5 74B8 GPU_MEMID MAKE_BASE=TRUE
77D5 74B7 NC_GPU_GPIO_28 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_28 — 74B8 77D5
77C5 74B7 NC_GPU_GPIO_29 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_29 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_30 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_30 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_31 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_31 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_32 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_32 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_33 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_33 — 74B8 77C5
77C5 74B7 NC_GPU_GPIO_34 — MAKE_BASE=TRUE NO_TEST=TRUE — NC_GPU_GPIO_34 — 74B8 77C5

Renamed signals

77A5 74C1 34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_CLK27M — 34B2 34B4 74C2 77A5

Unused signals

77A5 74C1	NC_GPU_XTALOUT	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_XTALOUT 74C2 77A5
77A3 74C1	NC_ATI_ROMCS_L	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_ATI_ROMCS_L 74C2 77A3
74C1 73D5	NC_FB_A_MA12	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_FB_A_MA12 73D5 74C2
74C1 73D1	NC_FB_B_MA12	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_FB_B_MA12 73D1 74C2
77C3 74C1	NC_GPU_GENERICA	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_GENERICA 74C2 77C3
77C3 74C1	NC_GPU_GENERICB	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_GENERICB 74C2 77C3
77C3 74C1	NC_GPU_GENERICC	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_GENERICC 74C2 77C3
78C3 74C1	NC_GPU_VGA_R	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_VGA_R 74C2 78C3
78C3 74C1	NC_GPU_VGA_G	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_VGA_G 74C2 78C3
78C3 74C1	NC_GPU_VGA_B	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_VGA_B 74C2 78C3
78B3 74C1	TP_GPU_VGA_HSYNC	MAKE_BASE=TRUE		TP_GPU_VGA_HSYNC 74C2 78B3
78B3 74C1	TP_GPU_VGA_VSYNC	MAKE_BASE=TRUE		TP_GPU_VGA_VSYNC 74C2 78B3
78B3 74C1	NC_GPU_TV_Y	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_TV_Y 74C2 78B3
78B3 74B1	NC_GPU_TV_C	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_TV_C 74B2 78B3
78B3 74B1	NC_GPU_TV_COMP	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_GPU_TV_COMP 74B2 78B3
78B3 74B1	NC_LVDS_U_DATAP<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_LVDS_U_DATAP<3> 74B2 78B3
78B3 74B1	NC_LVDS_U_DATAN<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_LVDS_U_DATAN<3> 74B2 78B3
78A3 74B1	NC_LVDS_L_DATAP<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_LVDS_L_DATAP<3> 74B2 78A3
78A3 74B1	NC_LVDS_L_DATAN<3>	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_LVDS_L_DATAN<3> 74B2 78A3
77C3 74B1	NC_ATI_DVPCLK	MAKE_BASE=TRUE	NO_TEST=TRUE	NC_ATI_DVPCLK 74B2 77C3
77C3 77B3	NC_ATI_DVPCNTL<2..0>	MAKE_BASE=TRUE	NO_TEST=TRUE	ATI_DVPCNTL<2..0>
77B3	NC_ATI_DVPDATA<15..0>	MAKE_BASE=TRUE	NO_TEST=TRUE	ATI_DVPDATA<15..0>

Required for debug access

77B3 77A3 TP_ATI_DVPDATA<23..16> — MAKE_BASE=TRUE — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

77D2 77C6 77B7 74D6 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 PP3V3_D3C

R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402

78A3 GPU_DDC_B_CLK
78A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

Connect to designated pin, then GND

CRITICAL OMIT

U8900 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

U8950 FBGA (1 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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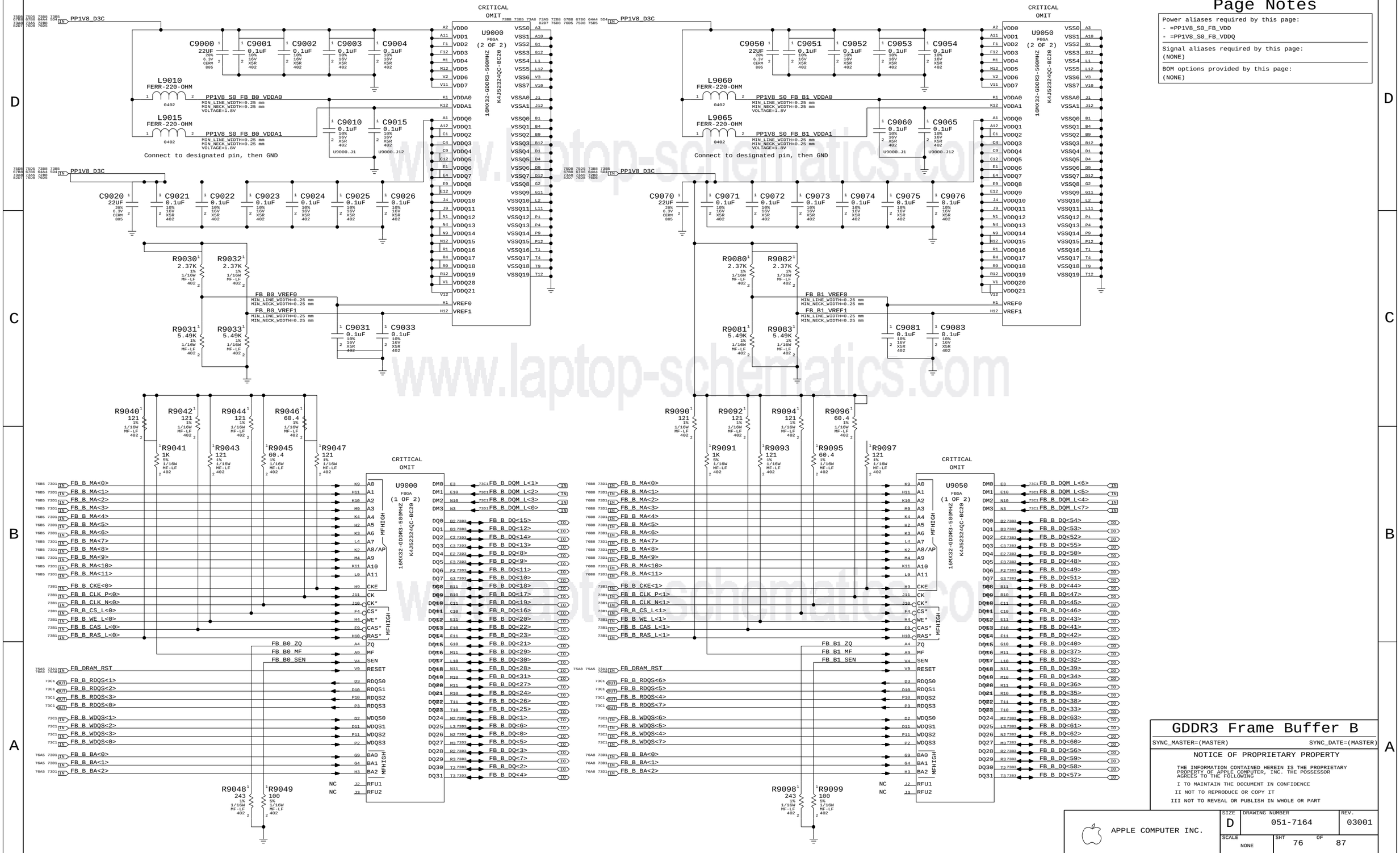

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7164	03001

SCALE	SHT	OF
NONE	76	87

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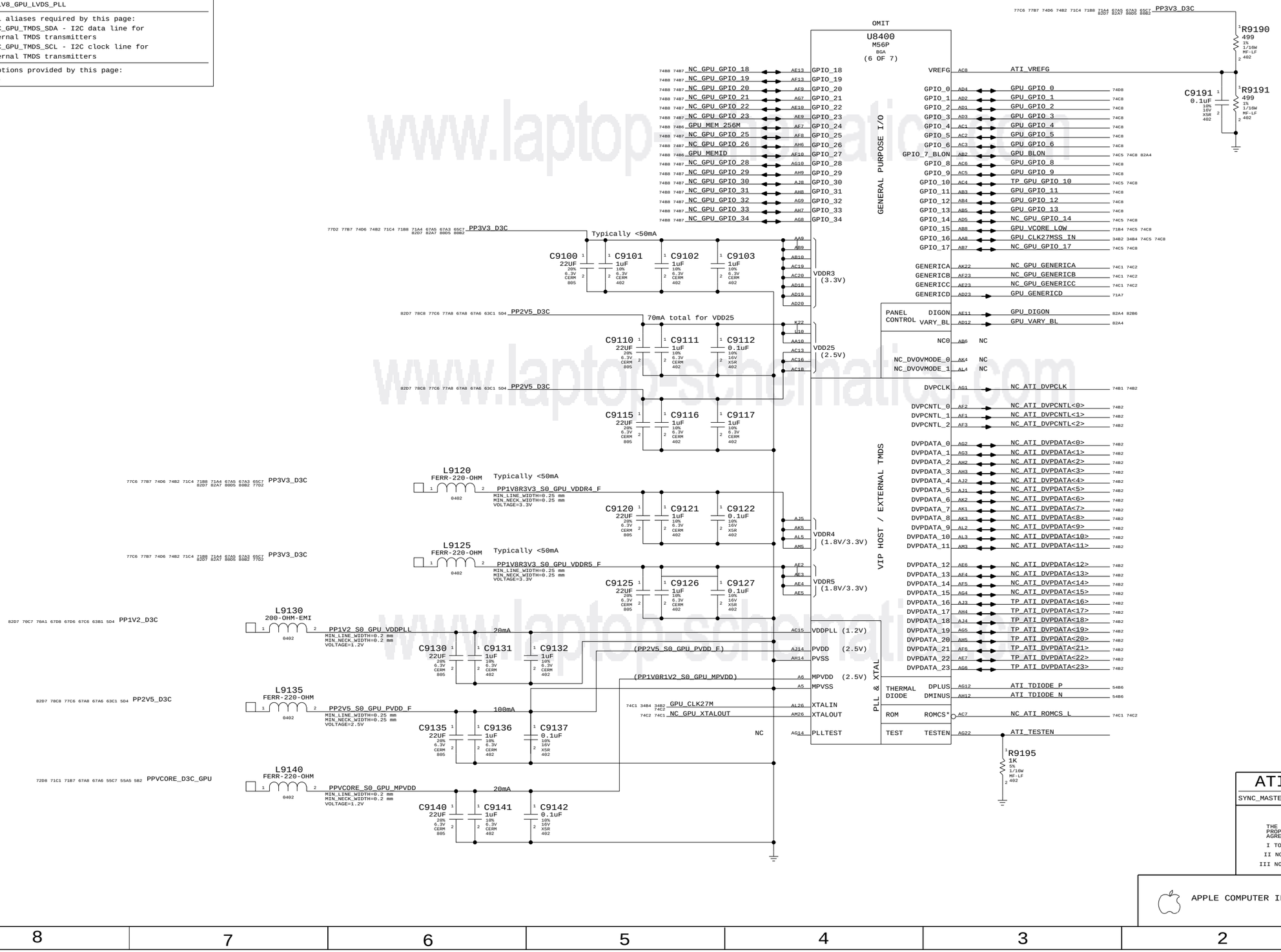
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



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ATI M56 GPIO/DVO/Misc		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

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Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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PP2V5_D3C
Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
20mA peak
C9300 22UF 20% 6.3V CERM 805
C9301 1uF 10% 6.3V CERM 402
C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V
150mA peak
C9305 22UF 20% 6.3V CERM 805
C9306 1uF 10% 6.3V CERM 402
C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V
65mA peak
C9310 22UF 20% 6.3V CERM 805
C9311 1uF 10% 6.3V CERM 402
C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
20mA peak
C9315 22UF 20% 6.3V CERM 805
C9316 1uF 10% 6.3V CERM 402
C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V
130mA peak
C9320 22UF 20% 6.3V CERM 805
C9321 1uF 10% 6.3V CERM 402
C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
20mA peak
C9325 22UF 20% 6.3V CERM 805
C9326 1uF 10% 6.3V CERM 402
C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
20mA peak
C9330 22UF 20% 6.3V CERM 805
C9331 1uF 10% 6.3V CERM 402
C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V
200mA peak
C9340 22UF 20% 6.3V CERM 805
C9345 22UF 20% 6.3V CERM 805
C9341 1uF 10% 6.3V CERM 402
C9342 0.1uF 10% 16V X5R 402
C9346 0.1uF 10% 16V X5R 402
C9347 0.1uF 10% 16V X5R 402

ATI_RSET — 78A8
ATI_R2SET — 78B5

R9350 499 1% 1/10W MF-LF 402
R9351 715 1% 1/10W MF-LF 402

OMIT

U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR
- AL25 AVDD (2.5V)
- AM25 AVDD (2.5V)
- AJ24 AVSS
- AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- AL22 RSET
- AL16 A2VDD (2.5V)
- AM16 A2VDD (2.5V)
- AL17 A2VSS
- AM17 A2VSS
- AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- AK14 R2SET
- AE19 LPVDD (2.5V)
- AE18 LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
- AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

DAC (CRT)
- AK24 R
- AM24 G
- AL24 B
- AJ23 HSYNC
- AJ22 VSYNC

DAC2 (TV/CRT2)
- AK15 R2
- AM15 G2
- AL15 B2
- AF15 H2SYNC
- AG15 V2SYNC
- AJ15 Y
- AJ13 C
- AH15 COMP

LVDS
- AJ21 TXCLK_UP
- AK21 TXCLK_UN
- AG18 TXOUT_U0P
- AH18 TXOUT_U0N
- AK20 TXOUT_U1P
- AJ20 TXOUT_U1N
- AG20 TXOUT_U2P
- AH20 TXOUT_U2N
- AH21 TXOUT_U3P
- AG21 TXOUT_U3N
- AM18 TXCLK_LP
- AL18 TXCLK_LN
- AL19 TXOUT_L0P
- AK19 TXOUT_L0N
- AM20 TXOUT_L1P
- AL20 TXOUT_L1N
- AM21 TXOUT_L2P
- AL21 TXOUT_L2N
- AJ18 TXOUT_L3P
- AK18 TXOUT_L3N

MONITOR IDENTIFICATION
- AH23 DDC1CLK
- AH22 DDC1DATA
- AG13 DDC2CLK
- AH13 DDC2DATA
- AE12 DDC3CLK
- AE12 DDC3DATA
- AE11 HPD1 — GPU_HPD — 80A2

TMDS
- AM9 TXCP — TMDS_CLK_P
- AL9 TXCM — TMDS_CLK_N
- AL10 TX0P — TMDS_DATA_P<0>
- AK10 TX0M — TMDS_DATA_N<0>
- AM11 TX1P — TMDS_DATA_P<1>
- AL11 TX1M — TMDS_DATA_N<1>
- AM12 TX2P — TMDS_DATA_P<2>
- AL12 TX2M — TMDS_DATA_N<2>
- AJ9 TX3P — TMDS_DATA_P<3>
- AK9 TX3M — TMDS_DATA_N<3>
- AJ11 TX4P — TMDS_DATA_P<4>
- AK11 TX4M — TMDS_DATA_N<4>
- AJ12 TX5P — TMDS_DATA_P<5>
- AK12 TX5M — TMDS_DATA_N<5>

R — NC_GPU_VGA_R
G — NC_GPU_VGA_G
B — NC_GPU_VGA_B
HSYNC — TP_GPU_VGA_HSYNC
VSYNC — TP_GPU_VGA_VSYNC

R2 — GPU_R2
G2 — GPU_G2
B2 — GPU_B2
H2SYNC — GPU_H2SYNC
V2SYNC — GPU_V2SYNC
Y — NC_GPU_TV_Y
C — NC_GPU_TV_C
COMP — NC_GPU_TV_COMP

LVDS
- TXCLK_UP — LVDS_U_CLK_P
- TXCLK_UN — LVDS_U_CLK_N
- TXOUT_U0P — LVDS_U_DATA_P<0>
- TXOUT_U0N — LVDS_U_DATA_N<0>
- TXOUT_U1P — LVDS_U_DATA_P<1>
- TXOUT_U1N — LVDS_U_DATA_N<1>
- TXOUT_U2P — LVDS_U_DATA_P<2>
- TXOUT_U2N — LVDS_U_DATA_N<2>
- TXOUT_U3P — NC_LVDS_U_DATAP<3>
- TXOUT_U3N — NC_LVDS_U_DATAN<3>
- TXCLK_LP — LVDS_L_CLK_P
- TXCLK_LN — LVDS_L_CLK_N
- TXOUT_L0P — LVDS_L_DATA_P<0>
- TXOUT_L0N — LVDS_L_DATA_N<0>
- TXOUT_L1P — LVDS_L_DATA_P<1>
- TXOUT_L1N — LVDS_L_DATA_N<1>
- TXOUT_L2P — LVDS_L_DATA_P<2>
- TXOUT_L2N — LVDS_L_DATA_N<2>
- TXOUT_L3P — NC_LVDS_L_DATAP<3>
- TXOUT_L3N — NC_LVDS_L_DATAN<3>

MONITOR IDENTIFICATION
- DDC1CLK — GPU_DDC_A_CLK
- DDC1DATA — GPU_DDC_A_DATA
- DDC2CLK — GPU_DDC_B_CLK
- DDC2DATA — GPU_DDC_B_DATA
- DDC3CLK — GPU_DDC_C_CLK
- DDC3DATA — GPU_DDC_C_DATA

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7164	03001

SCALE: NONE SHT 78 OF 87

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	78B3 80C3
	VGA	VGA	GPU_G2	78B3 80C3
	VGA	VGA	GPU_B2	78B3 80C3
	LVDS	LVDS	LVDS_U_CLK_P	6A1 6A2 78B3 82B8 82C3
	LVDS	LVDS	LVDS_U_CLK_N	6A1 6A2 78B3 82B8 82C3
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	6A1 6B1 6B2 78B3 82B3 82C3 82C8
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	6A1 6B1 6B2 78B3 82C3 82C8
	LVDS	LVDS	LVDS_L_CLK_P	6B1 6B2 78A3 82C3 82C8
	LVDS	LVDS	LVDS_L_CLK_N	6B1 6B2 78A3 82C3 82D8
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	6B1 6B2 78A3 82C3 82D8
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	6B1 6B2 78A3 82C3 82D8
	LVDS	LVDS	LVDS_U_CLK_CONN_P	79B2 82C1
	LVDS	LVDS	LVDS_U_CLK_CONN_N	79B2 82C1
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	79B2 79C2 82C1 82D1
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	79C2 82C1 82D1
	LVDS	LVDS	LVDS_L_CLK_CONN_P	79C2 82C1
	LVDS	LVDS	LVDS_L_CLK_CONN_N	79C2 82C1
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	79C2 82C1
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	79C2 82C1
	TMDS	TMDS	TMDS_CLK_P	78C3 80B8 87B4
	TMDS	TMDS	TMDS_CLK_N	78C3 80C8 87B4
	TMDS	TMDS	TMDS_DATA_P<5..3>	78C3 80A8 80B8 87A4
	TMDS	TMDS	TMDS_DATA_N<5..3>	78C3 80A8 80B8 87A4
	TMDS	TMDS	TMDS_DATA_P<2..0>	78C3 80C8 80D8 87A4
	TMDS	TMDS	TMDS_DATA_N<2..0>	78C3 80C8 80D8 87A4

PP3V3_S5

R9400 100K 5% 1/10W MF-LF 402

C9400 0.0022uF 10% 50V CERM 402

R9401 100K 5% 1/16W MF-LF 402

LCD_PWREN_L_RC

LCD_PWREN_L

Q9400 SI3443DV TSOP-LF

PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

L9400 FERR-250-OHM SM

C9401 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

Q9401 2N7002 SOT23-LF

LVDS_PANEL_EN

R9494 100K 5% 1/16W MF-LF 402

PP3V3_S0

100K pull-ups are for no-panel case (development). Panel has 2K pull-ups

R9410 100K 5% 1/16W MF-LF 402

R9411 100K 5% 1/16W MF-LF 402

LVDS_CONN_DDC_CLK

LVDS_CONN_DDC_DATA

C9410 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM

GND_CHASSIS_LVDS

C9420 0.001uF 20% 50V CERM 402

PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V

NC

LVDS_L_DATA_CONN_N<0>
LVDS_L_DATA_CONN_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_CONN_N
LVDS_L_CLK_CONN_P
LVDS_U_DATA_CONN_N<0>
LVDS_U_DATA_CONN_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_CONN_N
LVDS_U_CLK_CONN_P

C9421 0.001uF 20% 50V CERM 402

GND_CHASSIS_LVDS

518S0289

INVERTER INTERFACE

PPBUS_G3H

CRITICAL
L9450 FERR-220-OHM-2A 0603

PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V

C9450 0.001uF 20% 50V CERM 402

PP5V_S0

Q9450 FDG6332C_NL SC70-6 P-CHN

R9450 100K 5% 1/16W MF-LF 402

PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

L9452 400-OHM-EMI SM-1

C9451 10UF 20% 6.3V X5R 603

FP_PWR_EN_L

Q9450 FDG6332C_NL SC70-6 N-CHN

INVERTER_BKLTON

R9489 100K 5% 1/16W MF-LF 402

CRITICAL
J9450 SM04B-ACH M-RT-SM

NC

PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

C9452 0.001uF 20% 50V CERM 402

L9454 400-OHM-EMI SM-1

INVERTER_PWM

GND_CHASSIS_INVERTER

518S0369

C9454 0.001uF 20% 50V CERM 402

CRITICAL
L9455 FERR-220-OHM-2A 0603

GND_CHASSIS_INVERTER

PP3V3_S0

PLT_RST_L

U9453 MC74VHC1G08 SC70

INVERTER_PWM_UNBUF

INVERTER_PWM_F

INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL

C9453 0.1uF 20% 10V CERM 402

www.laptop-schematics.com

Internal Display Connectors

SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7164	03001
SCALE: NONE	SHT 79 OF 87	

TMDS Filtering

Place termination components close to GPU, common mode chokes near connector.

TMDS_DATA_N<0> — TMDS_DATA_RL<0> (VOLTAGE=0V, NO_TEST=TRUE) — R9762 182 1% 1/16W MF-LF 402 — L9743 47nH 0402 — TMDS_DATA_P<0>

TMDS_DATA_N<1> — TMDS_DATA_RL<1> (VOLTAGE=0V, NO_TEST=TRUE) — R9766 182 1% 1/16W MF-LF 402 — L9744 47nH 0402 — TMDS_DATA_P<1>

TMDS_DATA_N<2> — TMDS_DATA_RL<2> (VOLTAGE=0V, NO_TEST=TRUE) — R9770 182 1% 1/16W MF-LF 402 — L9745 47nH 0402 — TMDS_DATA_P<2>

TMDS_CLK_N — R9772 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_N (80D3)

TMDS_CLK_N — R9774 182 1% 1/16W MF-LF 402 — TMDS_CLK_P

TMDS_CLK_P — R9773 0 5% 1/16W MF-LF 402 → TMDS_CLK_R_P (80D1)

TMDS_DATA_N<3> — TMDS_DATA_RL<3> (VOLTAGE=0V, NO_TEST=TRUE) — R9778 182 1% 1/16W MF-LF 402 — L9746 47nH 0402 — TMDS_DATA_P<3>

TMDS_DATA_N<4> — TMDS_DATA_RL<4> (VOLTAGE=0V, NO_TEST=TRUE) — R9782 182 1% 1/16W MF-LF 402 — L9747 47nH 0402 — TMDS_DATA_P<4>

TMDS_DATA_N<5> — TMDS_DATA_RL<5> (VOLTAGE=0V, NO_TEST=TRUE) — R9786 182 1% 1/16W MF-LF 402 — L9748 47nH 0402 — TMDS_DATA_P<5>

CRITICAL L9700 90-OHM-100MA 1210-4SM1 (SYM_VER-1): TMDS_DATA_F_N<0> (80B5 80D1 87A4) / TMDS_DATA_F_P<0> (80B5 80D1 87A4)

CRITICAL L9701 90-OHM-100MA 1210-4SM1 (SYM_VER-1): TMDS_DATA_F_N<1> (80B3 80D1 87A4) / TMDS_DATA_F_P<1> (80B3 80D1 87A4)

CRITICAL L9702 90-OHM-100MA 1210-4SM1 (SYM_VER-1): TMDS_DATA_F_N<2> (80B3 80D1 87A4) / TMDS_DATA_F_P<2> (80B3 80D1 87A4)

CRITICAL L9706 370-OHM SM (SYM_VER-1): TMDS_CLK_F_N (80A5 80D1 87A4) / TMDS_CLK_F_P (81B3 80A1 79B8 71A6 67B3 67B1 67A1 80B5 80D1 87A4 25D8 5D4 5D2 66B5 62B1 61D7 58C7 58C4 57B5 55A8 53C4 36D6 31C6) → PP5V_S0

CRITICAL L9703 90-OHM-100MA 1210-4SM1 (SYM_VER-1): TMDS_DATA_F_N<3> (80B3 80D1 87A4) / TMDS_DATA_F_P<3> (80B3 80D1 87A4)

CRITICAL L9704 90-OHM-100MA 1210-4SM1 (SYM_VER-1): TMDS_DATA_F_N<4> (80B3 80D1 87A4) / TMDS_DATA_F_P<4> (80B3 80D1 87A4)

CRITICAL L9705 90-OHM-100MA 1210-4SM1 (SYM_VER-1): TMDS_DATA_F_N<5> (80B5 80D1 87A4) / TMDS_DATA_F_P<5> (80B5 80D1 87A4)

VGA SYNC BUFFERS

PP3V3_D3C (77C6 77B7 74D6 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 77D2)

GPU_V2SYNC (78B3) → U9750 MC74VHC1G08 SC70 → VGA_VSYNC_R → R9750 33 5% 1/16W MF-LF 402 → VGA_VSYNC (80A3)

C9750 0.1uF 20% 10V CERM 402

PLACE U9750 & U9751 CLOSE TO DVI CONNECTOR

PP3V3_D3C (77C6 77B7 74D6 74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 80B2 77D2)

GPU_H2SYNC (78B3) → U9751 MC74VHC1G08 SC70 → VGA_HSYNC_R → R9751 33 5% 1/16W MF-LF 402 → VGA_HSYNC (80A5)

C9751 0.1uF 20% 10V CERM 402

DVI INTERFACE

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0 → PP5V_S0_DDC_F (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm) → L9710 400-OHM-EMI SM-1 → PP5V_S0_DDC (VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL J9700 QH11121-RIG02-4F F-RT-TH-DVI

GND_CHASSIS_DVI_BOT (80A2 6B8 6B6 6A6)	33	31	
TMDS_DATA_F_N<0> (87A4 80D6 80D1)	17	1	TMDS_DATA_F_N<2> (80C6 80D1 87A4)
	9		TMDS_DATA_F_N<1> (80C6 80D1 87A4)
TMDS_DATA_F_P<0> (87A4 80D6 80D1)	18	2	TMDS_DATA_F_P<2> (80C6 80D1 87A4)
	10		TMDS_DATA_F_P<1> (80C6 80D1 87A4)
	19	3	
		11	
TMDS_DATA_F_N<5> (87A4 80D1 80A6)	20	4	TMDS_DATA_F_N<4> (80A6 80D1 87A4)
		12	TMDS_DATA_F_N<3> (80B6 80D1 87A4)
TMDS_DATA_F_P<5> (87A4 80D1 80A6)	21	5	TMDS_DATA_F_P<4> (80A6 80D1 87A4)
		13	TMDS_DATA_F_P<3> (80B6 80D1 87A4)
	22	6	DVI_DDC_CLK_R
		14	(PP5V_S0_DDC)
TMDS_CLK_F_P (87A4 80D1 80B6)	23	7	DVI_DDC_DATA_R
		15	
TMDS_CLK_F_N (87A4 80D1 80C6)	24	8	VGA_VSYNC (80D3)
		16	DVI_HPD_R
VGA_B (80C1)	C3	C1	VGA_R (80C1)
	C5B	C5A	
VGA_HSYNC (80C3)	C4	C2	VGA_G (80C1)
GND_CHASSIS_DVI_TOP (80A3 6B8 6B6)	34	32	

514-0278

PLACE NEAR C5A & C5B

R9730 0 5% 1/16W MF-LF 402

R9731 0 5% 1/16W MF-LF 402 → GND_CHASSIS_DVI_TOP (6B6 6B8 80A5)

PLACE NEAR 3, 11 & 19

C9710 0.01uF 20% 50V CERM 603

C9711 100pF 5% 50V CERM 402

C9713 100pF 5% 50V CERM 402

C9714 100pF 5% 50V CERM 402

Isolation required for DVI power switch

D9710 SOD-123 B0530WXF

R9710 4.7K 5% 1/16W MF-LF 402

R9712 4.7K 5% 1/16W MF-LF 402

PP5V_S0_DDC_PULLUPS (VOLTAGE=5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)

R9724 0 5% 1/16W MF-LF 402: GPU_HPD_R (80A1) → GPU_HPD (78A5)

3V LEVEL SHIFTERS

PP3V3_D3C (74B2 71C4 71B8 71A4 67A5 67A3 65C7 82D7 82A7 80D5 77D2 77C6 77B7 74D6)

R9711 100 5% 1/16W MF-LF 402: DVI_DDC_CLK → GPU_DDC_A_CLK (78A3)

R9713 100 5% 1/16W MF-LF 402: DVI_DDC_DATA → GPU_DDC_A_DATA (78A3)

GPU_SIGNAL_ENABLE (26A2 82A7)

R9714 100 5% 1/16W MF-LF 402: DVI_HPD → GPU_HPD_BILAT

Q9711 2N7002DW-X-F SOT-363 (G/D/S)

R9720 10K 5% 1/16W MF-LF 402

R9721 10K 5% 1/16W MF-LF 402

Q9714 2N7002DW-X-F SOT-363 (G/D/S)

R9722 270K 5% 1/16W MF-LF 402: GPU_HPD_R (80A3 81B3 67A1 67B1 67B3 57B5 58C4 58C7 55A8 53C4 36D6 31C5 66B5 62B1 61D7 58C7 58C4 57B5 55A8 53C4 36D6 31C6 71A6 79B8 80B5)

PP5V_S0

R9723 270K 5% 1/16W MF-LF 402

Q9715 2N7002DW-X-F SOT-363 (G/D/S)

SB_DVI_HPD (80A1 22A8) — MAKE_BASE=TRUE — SB_DVI_HPD (22A6 80A1)

R9715 20K 5% 1/16W MF-LF 402

GND_CHASSIS_DVI_BOT (6A6 6B6 6B8 80B5)

GND

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

CRITICAL FL9740 LCFILTER SM-220MHZ-LF: GPU_B2 (79D7 78B3) (DAC2 Comp) → VGA_B (80A5)

R9740 75 1% 1/16W MF-LF 402

C9740 3.3pF 0.25% 50V CERM 402

CRITICAL FL9741 LCFILTER SM-220MHZ-LF: GPU_G2 (79D7 78B3) (DAC2 Y) → VGA_G (80A3)

R9741 75 1% 1/16W MF-LF 402

C9741 3.3pF 0.25% 50V CERM 402

CRITICAL FL9742 LCFILTER SM-220MHZ-LF: GPU_R2 (79D7 78B3) (DAC2 C) → VGA_R (80A3)

R9742 75 1% 1/16W MF-LF 402

C9742 3.3pF 0.25% 50V CERM 402

External Display Connector		
SYNC_MASTER=M57_MLB_MG	SYNC_DATE=08/08/2006	

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	D	051-7164	03001
	SCALE: NONE	SHT 80 OF 87	

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL		
TMDS	TMDS	TMDS_CLK_R_P	80B7	
TMDS	TMDS	TMDS_CLK_R_N	80C7	
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	80B5	80B6 87A4
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	80A5	80C6 87A4
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>	80A6	80B3 80B5 80B6 80C6 80D6 87A4
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>	80A6	80B3 80B5 80B6 80C6 80D6 87A4

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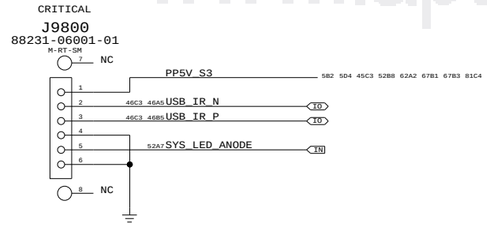
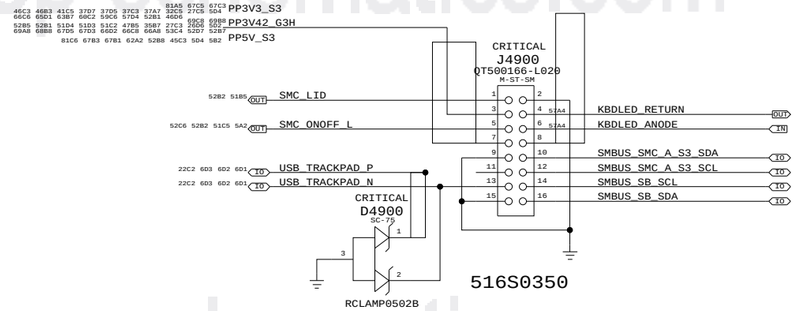
IR & Sleep LED Connector



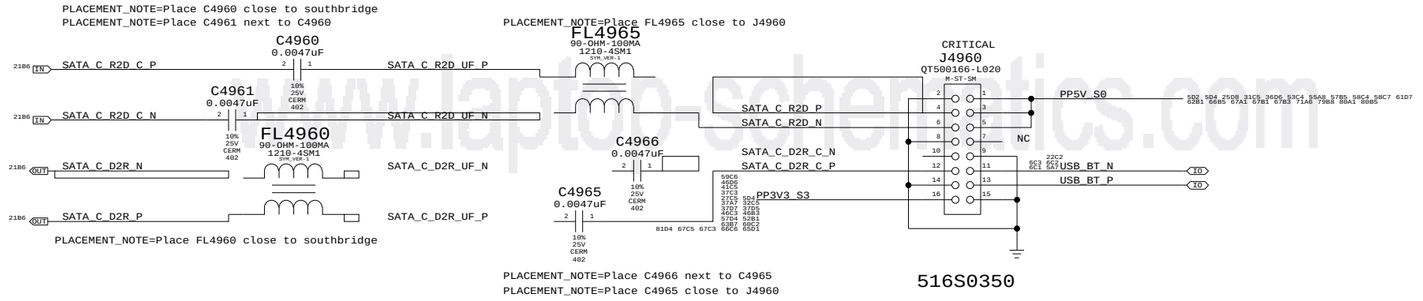
518S0474

Top-Case Connector



516S0350

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M57 SPECIFIC CONNECTORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS_L_DATA_P<0>
LVDS_L_DATA_N<0>
LVDS_L_CLK_N
LVDS_L_CLK_P
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_L_CLK_P
=LVDS_PD_L_CLK_N
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
=LVDS_PD_U_CLK_P
=LVDS_PD_U_CLK_N

LVDS_PD RP9900 8.2K
LVDS_PD RP9900 8.2K
LVDS_PD RP9900 8.2K
LVDS_PD RP9901 8.2K
LVDS_PD RP9901 8.2K
LVDS_PD RP9901 8.2K
LVDS_PD RP9902 8.2K
LVDS_PD RP9902 8.2K
LVDS_PD RP9902 8.2K
LVDS_PD RP9903 8.2K
LVDS_PD RP9903 8.2K
LVDS_PD RP9903 8.2K

5% 1/16W SM-LF

PGOOD Monitor for GPU Rails

PP3V3_D3C
PP2V5_D3C
PP1V8_D3C
PP1V2_D3C

R9994 124K 1% 1/16W MF-LF 402
R9992 237K 1% 1/16W MF-LF 402
R9990 365K 1% 1/16W MF-LF 402
R9997 10K 5% 1/16W MF-LF 402

C9990 0.1UF 20% 10V CERM 402
C9991 0.1UF 20% 10V CERM 402

PP3V3_S0

U9990 LTC2903 TSOT-23 CRITICAL
V1 V2 V3 V4 RST* GND

D3CPGOOD_2V5_DIV
D3CPGOOD_1V8_DIV
D3CPGOOD_1V2_DIV
D3CPGOOD_PWROK

R9995 100K 1% 1/16W MF-LF 402
R9993 100K 1% 1/16W MF-LF 402
R9991 100K 1% 1/16W MF-LF 402
C9995 0.1UF 20% 10V CERM 402
C9993 0.1UF 20% 10V CERM 402
C9992 0.1UF 20% 10V CERM 402
R9996 470K 5% 1/16W MF-LF 402

U9991 MC74VHC1G08 SC70
S0PGOOD_PWROK
S0D3CPGOOD_PWROK

LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

PP3V3_S0
PP2V5_S0

C9985 0.1UF 20% 10V CERM 402
C9980 0.1UF 20% 10V CERM 402

U9985 MC74VHC1G08 SC70
GPU_DIGON
LVDS_MUX_SEL_GPU
GPU_DIGON_AND_SELECTED

U9980 SN74LVC1G132 SC70-5 CRITICAL

R9980 10K 5% 1/16W MF-LF 402
PP3V3_LCD_SW
PANEL_PWR_ON
R9981 13.3K 1% 1/16W MF-LF 402

Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU DDC Pass FETs

GPU_SIGNAL_ENABLE
PP3V3_D3C

R9970 15.8K 1% 1/16W MF-LF 402
R9971 15.8K 1% 1/16W MF-LF 402

Q9970 2N7002DW-X-F SOT-363

GPU_DDC_C_CLK
GPU_DDC_C_DATA
LVDS_CONN_DDC_CLK
LVDS_CONN_DDC_DATA
MAKE_BASE=TRUE

LVDS I/F Mux

PP2V5_S0

C9950 0.1UF 20% 10V CERM 402

U9950 CBTV4020 BGA-LF CRITICAL
VDD GND

NB LVDS I/F

LVDS_B_DATA_N<2>
LVDS_B_DATA_N<0>
LVDS_B_DATA_P<0>
LVDS_A_CLK_P
LVDS_A_CLK_N
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
LVDS_A_DATA_P<2>
LVDS_A_DATA_N<2>
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
LVDS_B_DATA_P<1>
LVDS_B_DATA_N<1>
LVDS_B_CLK_N
LVDS_B_CLK_P
LVDS_B_DATA_P<2>

GPU LVDS I/F

LVDS_U_DATA_N<2>
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_L_CLK_P
LVDS_L_CLK_N
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_P<2>
LVDS_L_DATA_N<2>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<1>
LVDS_U_CLK_N
LVDS_U_CLK_P
LVDS_U_DATA_P<2>

DH0 LVDS_U_DATA_CONN_N<2>
DH1 LVDS_U_DATA_CONN_N<0>
DH2 LVDS_U_DATA_CONN_P<0>
DH3 NC
DH4 LVDS_L_CLK_CONN_P
DH5 LVDS_L_CLK_CONN_N
DH6 NC
DH7 LVDS_L_DATA_CONN_N<0>
DH8 LVDS_L_DATA_CONN_P<0>
DH9 LVDS_L_DATA_CONN_P<2>
DH10 LVDS_L_DATA_CONN_N<2>
DH11 LVDS_L_DATA_CONN_N<1>
DH12 LVDS_L_DATA_CONN_P<1>
DH13 NC
DH14 LVDS_U_DATA_CONN_P<1>
DH15 LVDS_U_DATA_CONN_N<1>
DH16 NC
DH17 LVDS_U_CLK_CONN_N
DH18 LVDS_U_CLK_CONN_P
DH19 LVDS_U_DATA_CONN_P<2>

SEL LVDS_MUX_SEL_GPU_L

NOTE: SEL = LOW selects port B

Panel/Backlight Control Mux

PP3V3_S0

C9960 0.1UF 20% 10V CERM 402

U9960 74CBTLV3257 QFN SYM_VER-2 CRITICAL
VCC GND THRML PAD

LVDS_VDDEN
GPU_DIGON
LVDS_BKLTEN
GPU_BLON
LVDS_BKLTCTL
GPU_VARY_BL
S0PGOOD_PWROK
S0D3CPGOOD_PWROK
LVDS_MUX_SEL_GPU_MUXED

1B1 1B2 2B1 2B2 3B1 3B2 4B1 4B2 S OE*

1A LVDS_PANEL_EN
2A INVERTER_BKLTON
3A INVERTER_PWM_UNBUF
4A PGOOD_MUXED_S0_OR_S0D3C

NOTE: S = HIGH selects xB2

PP3V3_S0
C9961 0.1UF 20% 10V CERM 402

PLT_RST_L
LVDS_MUX_SEL_GPU

U9961 MC74VHC1G08 SC70

R9961 100K 5% 1/16W MF-LF 402
R9960 10K 5% 1/16W MF-LF 402

NO STUFF
R9962 0 5% 1/16W MF-LF 402

LVDS_MUX_SEL_GPU
LVDS_MUX_SEL_GPU
MAKE_BASE=TRUE
LVDS_MUX_SEL_GPU

NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU

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LVDS Interface Pull-downs
SYNC_MASTER=M57_MLB_MG SYNC_DATE=08/08/2006

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NONE	83	87

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3SS_TO_5SS	*	Y	=3S_OHM_SE	=5S_OHM_SE	=3S_5S_OHM_SE	=STANDARD	=STANDARD
FB_4QS	*	Y	=4Q_OHM_SE	=4Q_OHM_SE	=4Q_OHM_SE	=STANDARD	=STANDARD
FB_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

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More System Constraints

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D	051-7164	03001

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M9 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

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M9 Spacing & Physical Constraints

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5B7 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5A4 7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5B7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5A7 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5A4 7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5B7 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5B7 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5B7 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5A7 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5B7 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5B4 7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	5B4 7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	5C4 7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5B4 14B7 23C3 61C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5C4 61C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 33C4 34D3 34D5
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 33C4 34D3 34D5
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 87B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 61B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 61A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	61A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	61A3

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 48B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 48B3
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 48B3

TMDS	TMDS	TMDS_CLK_P	78C3 79C7 80B8
TMDS	TMDS	TMDS_CLK_N	78C3 79C7 80C8
TMDS	TMDS	TMDS_DATA_P<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_N<5..3>	78C3 79C7 80A8 80B8
TMDS	TMDS	TMDS_DATA_P<2..0>	78C3 79C7 80C8 80D8
TMDS	TMDS	TMDS_DATA_N<2..0>	78C3 79C7 80C8 80D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	80A5 80C6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	80A6 80B3 80B5 80B6 80D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	80B3 80B5 80C6 80D1 80D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	80B3 80B5 80C6 80D1 80D6

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