

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESC
A		625211	PRODUCTION RELEASED 08/29/08 ?

M97 MLB SCHEMATIC

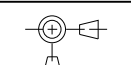
REFERENCED FROM T18
08/27/2008

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13	eXtended Debug Port (XDP)	T18_MLB 12/12/2007	48	WELLSPRING 2	YUAN_MA 05/09/2008			
14	MCP CPU Interface	T18_MLB 04/04/2008	49	SMS	YUNMU 06/26/2008			
15	MCP Memory Interface	T18_MLB 04/04/2008	50	SPI ROM	CHANGZHANG 05/02/2008			
16	MCP Memory Misc	T18_MLB 04/04/2008	51	AUDIO: CODEC	AUDIO 07/01/2008			
17	MCP PCIe Interfaces	T18_MLB 04/04/2008	52	AUDIO: MIKEY	AUDIO 07/03/2008			
18	MCP Ethernet & Graphics	T18_MLB 04/04/2008	53	AUDIO: SPEAKER AMP	AUDIO 07/01/2008			
19	MCP PCI & LPC	T18_MLB 04/04/2008	54	AUDIO: JACK	AUDIO 07/01/2008			
20	MCP SATA & USB	T18_MLB 04/04/2008	55	AUDIO: JACK TRANSLATORS	AUDIO 07/01/2008			
21	MCP HDA & MISC	T18_MLB 06/26/2008	56	DC-In & Battery Connectors	JACK 09/13/2008			
22	MCP Power & Ground	T18_MLB 04/04/2008	57	PBUS Supply/Battery Charger	RAYMOND 01/31/2008			
23	MCP79 A01 Silicon Support	T18_MLB 03/08/2008	58	5V/3.3V SUPPLY	RAYMOND 02/08/2008			
24	MCP Standard Decoupling	T18_MLB 04/04/2008	59	1.5V/0.75V DDR3 SUPPLY	RAYMOND 01/31/2008			
25	MCP Graphics Support	T18_MLB 12/12/2007	60	IMVP6 CPU VCore Regulator	RAYMOND 01/31/2008			
26	SB Misc	RAYMOND 04/05/2008	61	MCP VCore Regulator	RAYMOND 01/31/2008			
27	FSB/DDR3 Vref Margining	BEN 03/31/2008	62	CPU VTT(1.05V) SUPPLY	RAYMOND 02/08/2008			
28	DDR3 SO-DIMM Connector A	BEN 06/30/2008	63	MISC POWER SUPPLIES	RAYMOND 01/23/2008			
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30	DDR3 Support	T18_MLB 04/04/2008	65	POWER FETS	YUAN_MA 04/04/2008			
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32	VENICE CONNECTOR	YITE 03/13/2008	67	DISPLAYPORT SUPPORT	AMASON 04/18/2008			
33	Ethernet PHY (RTL8211CL)	SUMA 05/23/2008	68	DisplayPort Connector	AMASON 06/30/2008			
34	Ethernet & AirPort Support	SUMA 07/01/2008	69	LCD BACKLIGHT DRIVER	YITE 08/12/2008			
35	ETHERNET CONNECTOR	SUMA 04/04/2008	70	LCD Backlight Support	YITE 06/30/2008			

PVT BUILD

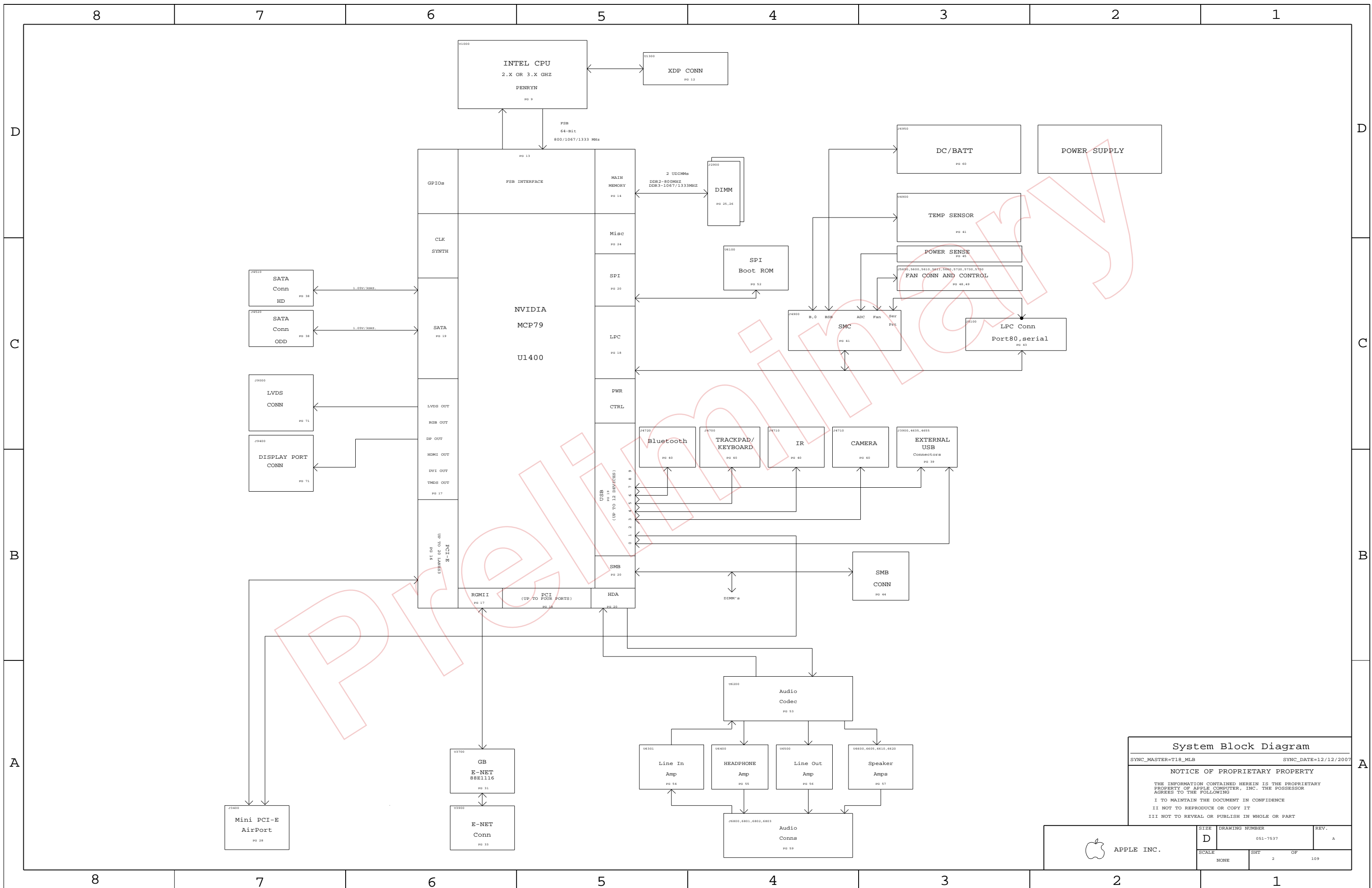
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7537	1	SCHEM,MLB,M97	SCH	CRITICAL	
820-2327	1	PCBF,MLB,M97	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
XX ± _____		DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX ± _____		ENG APPD	MFG APPD		
X.XXX ± _____		QA APPD	DESIGNER		
ANGLES ± _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				051-7537	
				REV. A	
				SHT 1 OF 109	

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System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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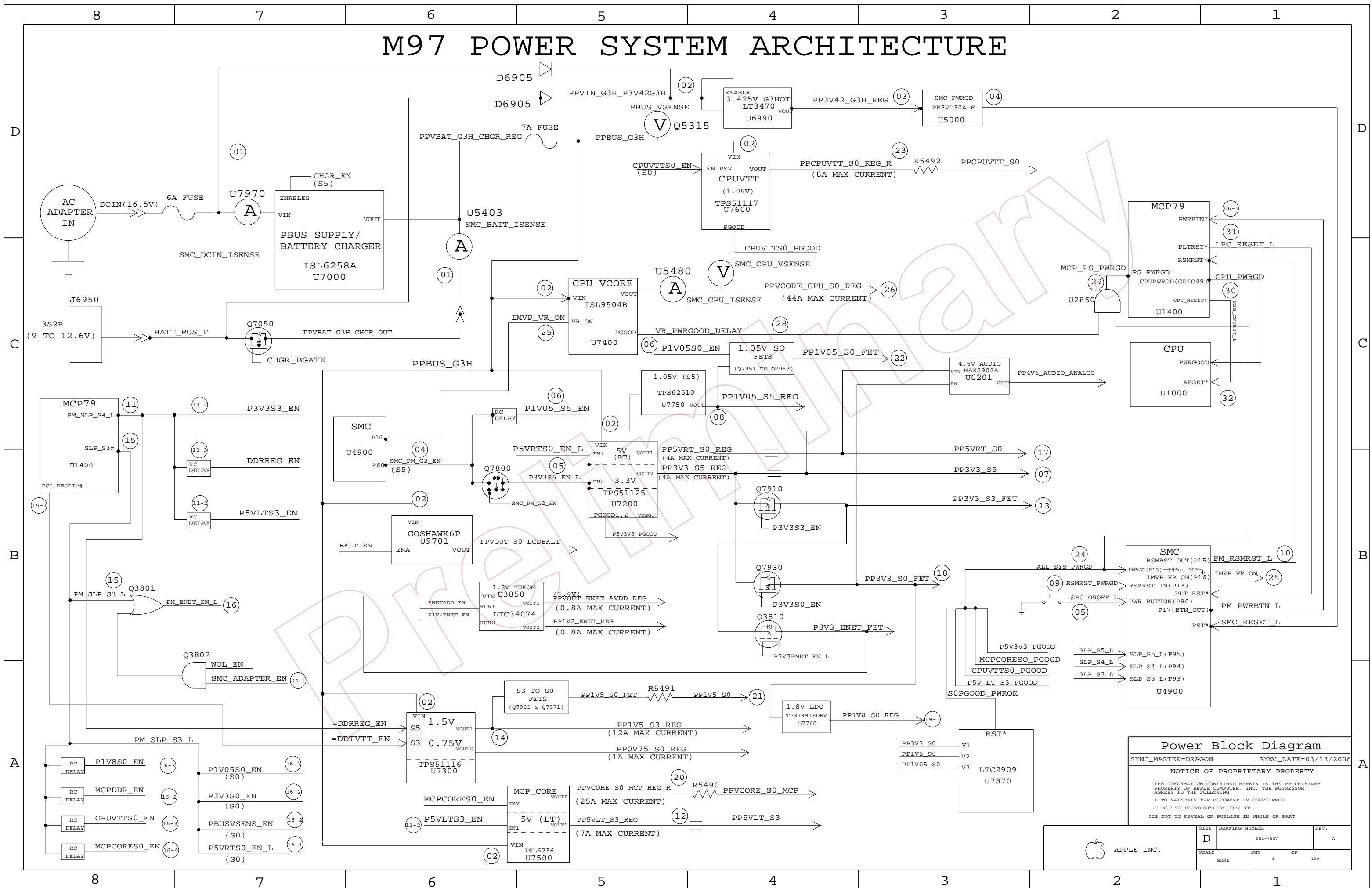
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHEET 2	OF 109

M97 POWER SYSTEM ARCHITECTURE



Power Block Diagram
 SYNC_MASTER=DRAGON SYNC_DATE=03/13/2008
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	D	051-7537	A
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9554	PCBA,MLB,BETTER,M97	M97_COMMON,CPU_2_0GHZ,EEE_2KA
630-9314	PCBA,MLB,BEST,M97	M97_COMMON,CPU_2_4GHZ,EEE_1DJ

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2K9]	CRITICAL	EEE_2K9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2KA]	CRITICAL	EEE_2KA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:1DJ]	CRITICAL	EEE_1DJ

BOM Groups

BOM GROUP	BOM OPTIONS
M97_COMMON	COMMON,ALTERNATE,M97_MCP,M97_MISC,M97_DEBUG_PVT,M97_PROGPARTS
M97_MCP	MCP_B02,MCP_PROD,MEMRESET_HW,MEMRESET_MCP,BOOT_MODE_USER,MCPSEQ_SMC,MCP_CS1_NO
M97_MISC	ONEWIRE_PU,BKLT_PLL_NOT,DP_ESD,ENG_BMON,MIKEY
M97_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
M97_DEBUG_ENG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TFAD_DEBUG
M97_DEBUG_PVT	SMC_DEBUG_YES,XDP,LPCPLUS,NO_VREFMRGN
M97_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3622	1	PDC,QJGL,QS,2.0,25W,1066,MO,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ_QS
337S3624	1	PDC,QDYD,QS,2.26,25W,1066,MO,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ_QS
337S3625	1	PDC,QDVJ,QS,2.4,25W,1066,MO,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ_QS
337S3646	1	PDC,SLGRK,FRQ,2.0,25W,1066,MO,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3653	1	PDC,SLBU,FRQ,2.26,25W,1066,MO,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLBN,FRQ,2.4,25W,1066,MO,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0540	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01	U1400	CRITICAL	MCP_A01
338S0591	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01P	U1400	CRITICAL	MCP_A01P
338S0603	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01Q	U1400	CRITICAL	MCP_A01Q
338S0600	1	IC,GMCP,MCP79,35X35MM,BGA1437,B01	U1400	CRITICAL	MCP_B01
338S0635	1	IC,GMCP,MCP79,35X35MM,BGA1437,B02	U1400	CRITICAL	MCP_B02
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER,48P,TOFP	U3700	CRITICAL	

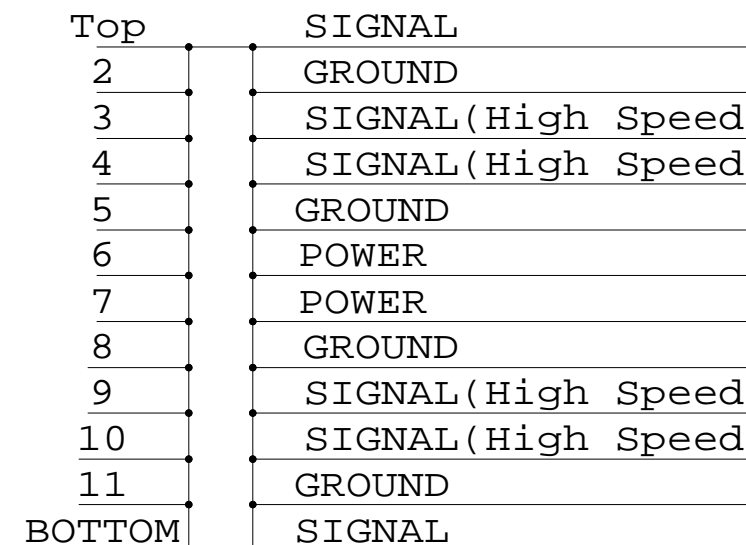
Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0563	1	IC,SMC,H88/2117,9X9MM,TLP,HP	U4900	CRITICAL	SMC_BLANK
341S2287	1	IC,SMC,M97	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SP1,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2285	1	IC,PRGRM,EFI,BOOTROM,UNLOCK,M97	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLP,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2348	1	IC,WELLSPRING CONTROLLER,M97	U5701	CRITICAL	WELLSPRING_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYTEC AS ALTERNATE
152S0796	152S0685		ALL	CYTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
514-0612	514-0607		ALL	FOXLINK AS ALTERNATE
514-0613	514-0608		ALL	FOXLINK AS ALTERNATE

M97 BOARD STACK-UP



BOM Configuration
 SYNC_MASTER=M97_MLB
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHEET 4	OF 109

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Revision History

Preliminary

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SYNC_MASTER=M97_MLB

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NONE	5	109	

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

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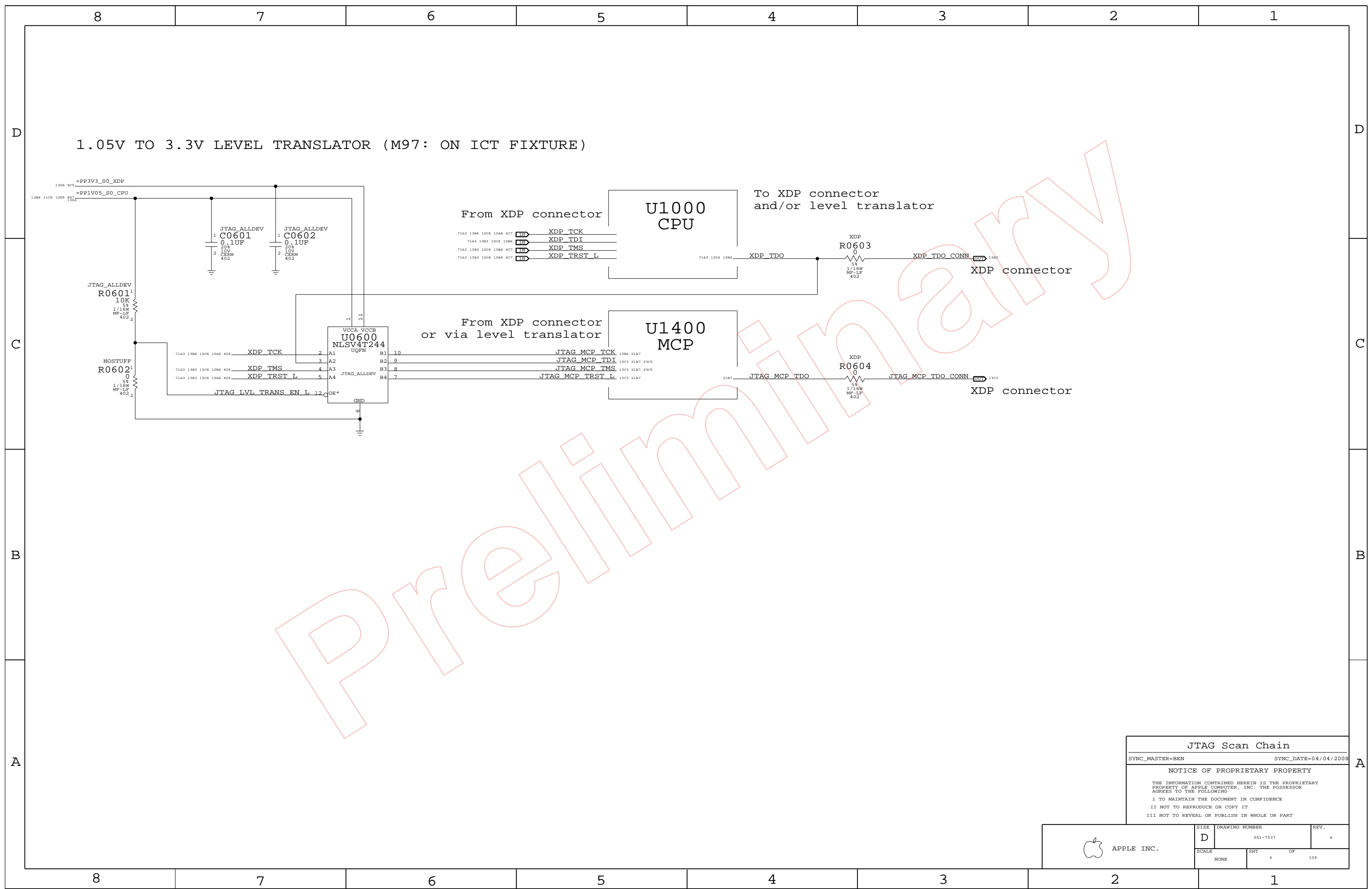
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JTAG Scan Chain

SYNC_MASTER=BEN SYNC_DATE=04/04/2008

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SCALE	SHT	OF	109
NONE	6		

Functional Test Points

8 7 6 5 4 3 2 1

Fan Connectors

8180	TRUE	PP5VRT_S0	(NEED 3 TP)	703 805
8181	TRUE	FAN_RT_PWM		4684
8182	TRUE	FAN_RT_TACH		4604

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

8231	TRUE	MIC_HI_CONN		5481 5402
8232	TRUE	MIC_LO_CONN		5481 5402
8233	TRUE	MIC_SHLD_CONN		5402 5546

SPEAKER FUNC_TEST

8240	TRUE	SPKRAMP_L_N_OUT		53A2 54C2
8241	TRUE	SPKRAMP_L_P_OUT		53B2 54C2
8242	TRUE	SPKRAMP_R_N_OUT		53C3 54C2
8243	TRUE	SPKRAMP_R_P_OUT		53B3 54C2
8244	TRUE	SPKRAMP_SUB_N_OUT		53B2 54C2
8245	TRUE	SPKRAMP_SUB_P_OUT		53B2 54C2

THERMAL FUNC_TEST

8260	TRUE	MCPTHMSNS_D2_P		4585 7703
8261	TRUE	MCPTHMSNS_D2_N		4585 7703

LVDS FUNC_TEST

8250	TRUE	PP3V3_LCDVDD_SW_F		703 6602
8251	TRUE	PP3V3_S0_LCD_F		6603
8252	TRUE	PPVOUT_S0_LCDBKLT		703 6802 6983 69C1
8253	TRUE	LVDS_IG_DDC_CLK		18A3 6605
8254	TRUE	LVDS_IG_DDC_DATA		18A3 6605
8255	TRUE	LVDS_IG_A_DATA_N<0>		18A3 6605
8256	TRUE	LVDS_IG_A_DATA_P<0>		18B3 6602 73B3
8257	TRUE	LVDS_IG_A_DATA_N<1>		18B3 6602 73B3
8258	TRUE	LVDS_IG_A_DATA_P<1>		18B3 6602 73B3
8259	TRUE	LVDS_IG_A_DATA_N<2>		18B3 6602 73B3
8260	TRUE	LVDS_IG_A_DATA_P<2>		18B3 6602 73B3
8261	TRUE	LVDS_IG_A_CLK_F_N		66B2 73B3
8262	TRUE	LVDS_IG_A_CLK_F_P		66B2 73B3
8263	TRUE	LED_RETURN_1		66B3 69C1
8264	TRUE	LED_RETURN_2		66B3 69B1
8265	TRUE	LED_RETURN_3		66B3 69B1
8266	TRUE	LED_RETURN_4		66B3 69B1
8267	TRUE	LED_RETURN_5		66B3 69B1
8268	TRUE	LED_RETURN_6		66B3 69B1

(NEED TO ADD 5 GND TP)

SATA ODD CONN

8240	TRUE	PP5V_SW_ODD	(NEED 4 TP)	703 3603
8241	TRUE	SMC_ODD_DETECT		36B7 39B8
8242	TRUE	SATA_ODD_D2R_C_P		36B5 73A3
8243	TRUE	SATA_ODD_D2R_C_N		36B5 73A3
8244	TRUE	SATA_ODD_R2D_P		36B5 73A3
8245	TRUE	SATA_ODD_R2D_N		705 36B5 73A3

(NEED TO ADD 4 GND TP)

DC POWER CONN

8230	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP)	5606
8231	TRUE	ADAPTER_SENSE		5607

(NEED TO ADD 4 GND TP)

BATT POWER CONN

8230	TRUE	PPVBAT_G3H_CONN_F	(NEED 3 TP)	56A8
8231	TRUE	GND_BATT_CONN	(NEED 3 TP)	56A8
8232	TRUE	SMBUS_SMC_BSA_SCL		7A7 4205 76D3
8233	TRUE	SMBUS_SMC_BSA_SCL		7A7 4205 76D3
8234	TRUE	SMC_BS_ALERT_L		39C5 40B2 56A8

BATT SIGNAL CONN

8230	TRUE	PP3V42_G3H	(NEED 3 TP)	785 703 805
8231	TRUE	SMBUS_SMC_BSA_SCL		7A7 4205 76D3
8232	TRUE	SMBUS_SMC_BSA_SCL		7A7 4205 76D3
8233	TRUE	SMC_BIL_BUTTON_DB_L		56A5

(NEED TO ADD 3 GND TP)

FRONT FLEX CONN

8180	TRUE	PP3V42_G3H_LIDSWITCH_R		38B6
8181	TRUE	PP5V_S3_IR_R		38B6
8182	TRUE	IR_RX_OUT		38A4 38C4
8183	TRUE	SMC_LID_R		38B6
8184	TRUE	SYS_LED_ANODE_R		38B6

(NEED TO ADD 2 GND TP)

RIGHT CLUTCH CONN

8180	TRUE	PP5V_S3_BT_CAMERA_F		31A7
8181	TRUE	PCIE_MINI_D2R_P		1786 3107 73D3
8182	TRUE	PCIE_MINI_D2R_N		1786 3107 73D3
8183	TRUE	PCIE_MINI_R2D_P		3107 73D3
8184	TRUE	PCIE_MINI_R2D_N		3107 73D3
8185	TRUE	PCIE_CLK100M_MINI_CONN_P		3108 73D3
8186	TRUE	PCIE_CLK100M_MINI_CONN_N		3108 73D3
8187	TRUE	USB_CAMERA_CONN_P		31B7 74C3
8188	TRUE	USB_CAMERA_CONN_N		31B7 74C3
8189	TRUE	PP5V_WLAN		703 3105
8190	TRUE	PCIE_WAKE_L		1786 3105 3107
8191	TRUE	SMBUS_SMC_A_S3_SCL		785 4202 76D3
8192	TRUE	SMBUS_SMC_A_S3_SDA		785 4202 76D3
8193	TRUE	CONN_USB2_BT_P		31B7 74B3
8194	TRUE	CONN_USB2_BT_N		31B7 74B3
8195	TRUE	MINI_CLKREQ_O_L		3107
8196	TRUE	MINI_RESET_CONN_L		31A7

(NEED TO ADD 3 GND TP)

SATA HDD CONN

8240	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP)	703 36A7
8241	TRUE	SATA_HDD_R2D_P		36A7 73A3
8242	TRUE	SATA_HDD_R2D_N		36A7 73A3
8243	TRUE	SATA_HDD_D2R_C_P		36A7 73A3
8244	TRUE	SATA_HDD_D2R_C_N		36A7 73A3
8245	TRUE	SATA_ODD_R2D_N		707 36B5 73A3

(NEED TO ADD 4 GND TP)

IPD_FLEX_CONN

8230	TRUE	PP3V3_S3_LDO		703 48B4 48C3
8231	TRUE	PP18V5_S3		703 48C1 48D3
8232	TRUE	TPAD_GND_F		48B4 48C3 48C4 48C7
8233	TRUE	Z2_CS_L		4708 4803
8234	TRUE	Z2_DEBUG3		4708 4803
8235	TRUE	Z2_MOSI		4708 4803
8236	TRUE	Z2_MISO		4708 4803
8237	TRUE	Z2_SCLK		4708 4803
8238	TRUE	Z2_BOOST_EN		4803 4805
8239	TRUE	Z2_HOST_INTN		4708 4803
8240	TRUE	Z2_BOOT_CFG1		4708 4803
8241	TRUE	Z2_CLKIN		4708 4803
8242	TRUE	Z2_KEY_ACT_L		4708 4801
8243	TRUE	Z2_RESET		4708 4801
8244	TRUE	PSOC_MISO		4708 4803
8245	TRUE	PSOC_MOSI		4708 4801
8246	TRUE	PSOC_SCLK		4708 4801
8247	TRUE	SMBUS_SMC_A_S3_SDA		705 4202 76D3
8248	TRUE	SMBUS_SMC_A_S3_SCL		705 4202 76D3
8249	TRUE	PSOC_F_CS_L		4708 4801
8250	TRUE	PICKB_L		4708 4801

KEYBOARD CONN

8230	TRUE	PP3V3_S3		703 803
8231	TRUE	PP3V42_G3H		7A7 703 801
8232	TRUE	WS_KBD1		4706 4702
8233	TRUE	WS_KBD2		4706 4702
8234	TRUE	WS_KBD3		4706 4702
8235	TRUE	WS_KBD4		4706 4702
8236	TRUE	WS_KBD5		4706 4702
8237	TRUE	WS_KBD6		4706 4702
8238	TRUE	WS_KBD7		4706 4702
8239	TRUE	WS_KBD8		4706 4702
8240	TRUE	WS_KBD9		4706 4702
8241	TRUE	WS_KBD10		4706 4702
8242	TRUE	WS_KBD11		4702 4706
8243	TRUE	WS_KBD12		4702 4706
8244	TRUE	WS_KBD13		4702 4706
8245	TRUE	WS_KBD14		4702 4706
8246	TRUE	WS_KBD15_CAP		4702
8247	TRUE	WS_KBD16_NUM		4702
8248	TRUE	WS_KBD17		4702 4706
8249	TRUE	WS_KBD18		4702 4707
8250	TRUE	WS_KBD19		4702 4707
8251	TRUE	WS_KBD20		4702 4707
8252	TRUE	WS_KBD21		4702 4707
8253	TRUE	WS_KBD22		4702 4707
8254	TRUE	WS_KBD23		4702 4707
8255	TRUE	WS_KBD_ONOFF_L		4702
8256	TRUE	WS_LEFT_SHIFT_KBD		47B3 47B5 47C2
8257	TRUE	WS_LEFT_OPTION_KBD		47B3 47B5 47C2
8258	TRUE	WS_CONTROL_KBD		47B3 47B5 47C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

8230	TRUE	KBDLED_ANODE		48A6
------	------	--------------	--	------

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

8230	TRUE	PPVCORE_S0_CPU		807
8231	TRUE	PPCPUVT_S0		807
8232	TRUE	PPVCORE_S0_MCP		807
8233	TRUE	PP0V75_S0		807
8234	TRUE	PP1V05_S0		807
8235	TRUE	PP1V5_S0		807
8236	TRUE	PP1V8_S0		807
8237	TRUE	PP5VRT_S0		807
8238	TRUE	PP3V3_S0		805
8239	TRUE	PP1V5_S3		803
8240	TRUE	PP3V3_S3		785 803
8241	TRUE	PP5VLT_S3		803
8242	TRUE	PP1V1R1V05_S5		883
8243	TRUE	PP3V3_S5		883
8244	TRUE	PP3V42_G3H		7A7 785 801
8245	TRUE	PPBUS_G3H		801
8246	TRUE	PP3V3_ENET_PHY		881
8247	TRUE	PP1V2R1V05_ENET		881
8248	TRUE	PP3V3_G3_RTC		2108 22A5 26D4
8249	TRUE	PP5V_WLAN		705 3105
8250	TRUE	PP5V_SW_ODD		787 36D3
8251	TRUE	PP5V_S0_HDD_FLT		705 36A7
8252	TRUE	PP3V3_S5_AVREF_SMC		3904 40B6
8253	TRUE	PP18V5_S3		705 48C1 48D3
8254	TRUE	PP3V3_S3_LDO		705 48B4 48C3
8255	TRUE	PP3V3_LCDVDD_SW_F		707 66C2
8256	TRUE	PPVOUT_S0_LCDBKLT		707 68B2 69B3 69C1
8257	TRUE	BKL_VREF_4V9		69A8 69B6 69C4 69C8
8258	TRUE	PP4V6_AUDIO_ANALOG		51A3 51D3 52D6
8259	TRUE	SMC_PM_G2_EN		39D5 64D8
8260	TRUE	PM_SLP_S4_L		2103 3905 40A2 64C8
8261	TRUE	PM_SLP_S3_L		2103 34B7 3905 41A5 64D5 68D8

(NEED TO ADD 4 GND TP)

FUNC TEST

SYNC_MASTER=M97_MLB

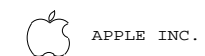
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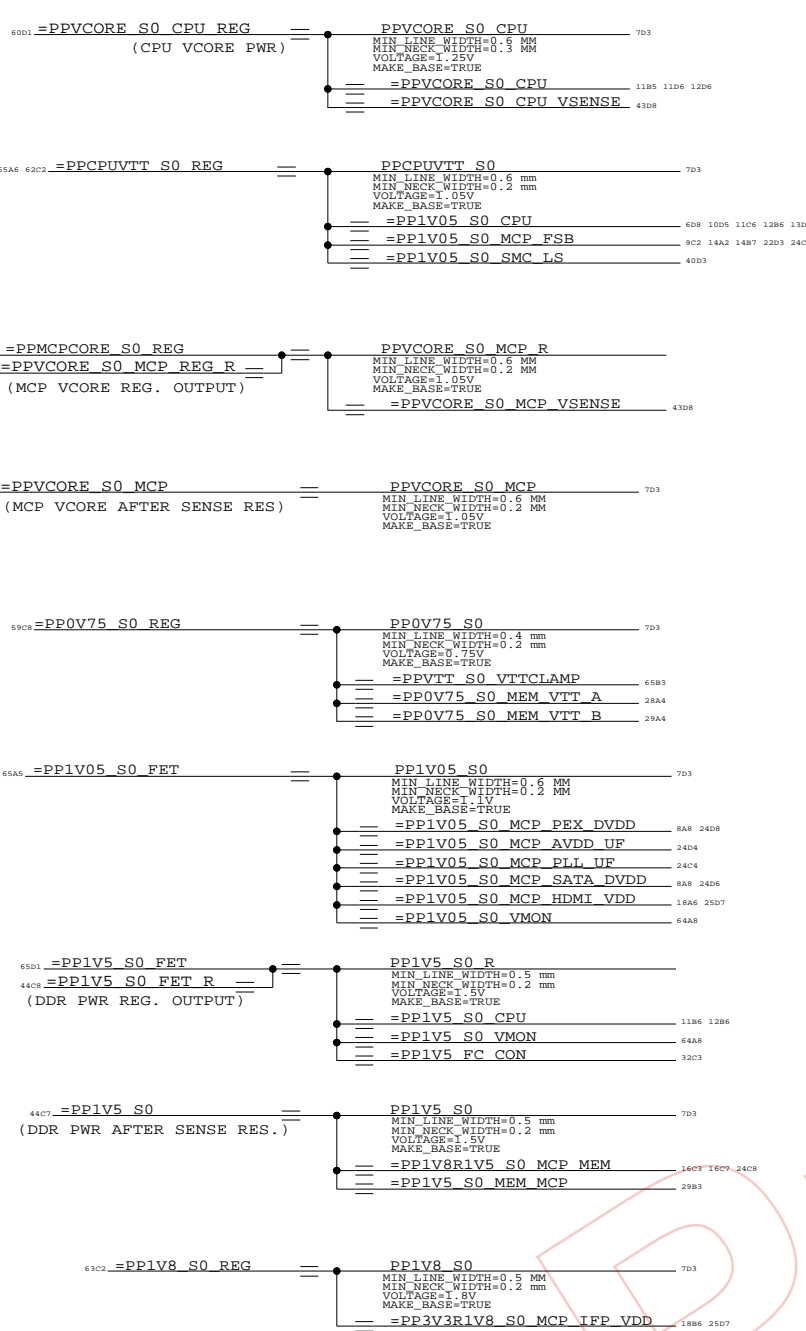
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



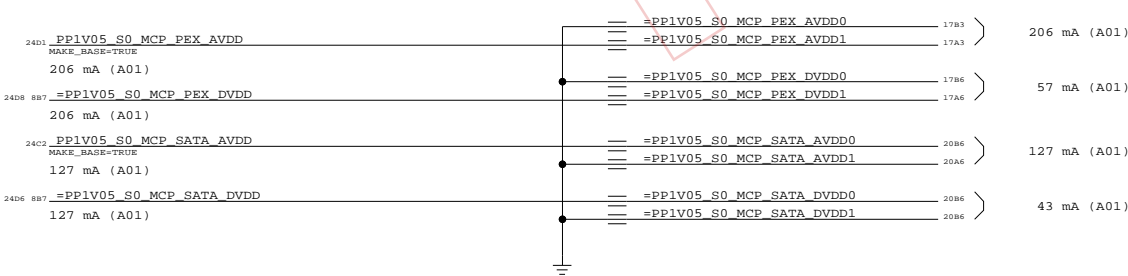
SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	7	109

8 7 6 5 4 3 2 1

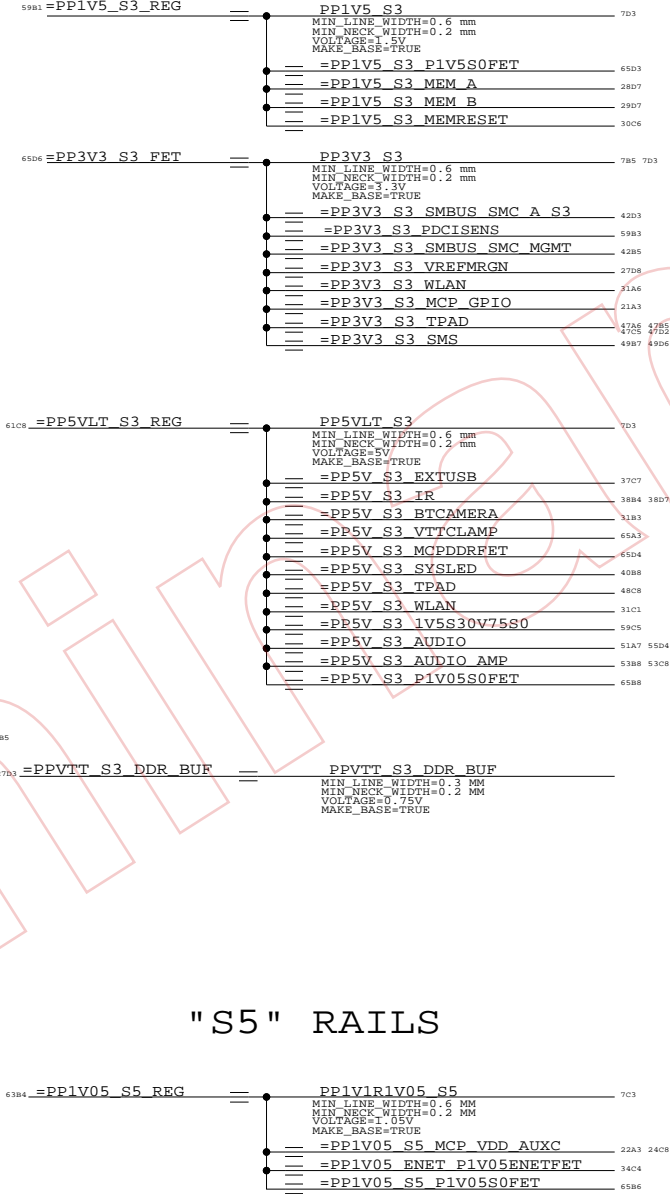
"S0,S0M" RAILS



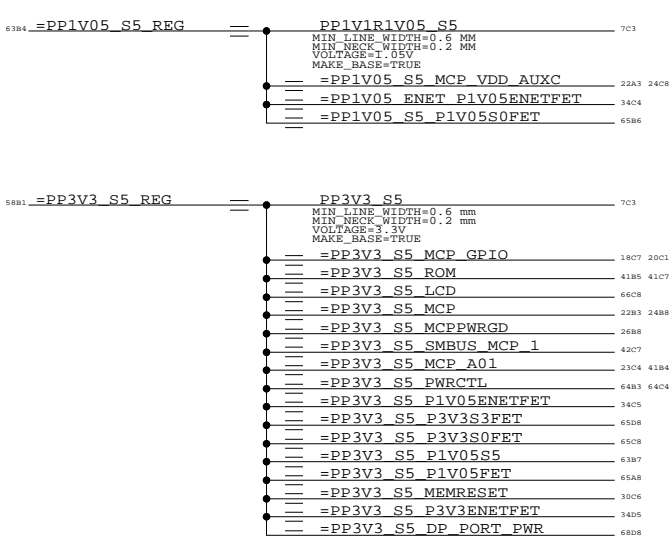
PEX & SATA AVDD/DVDD aliases



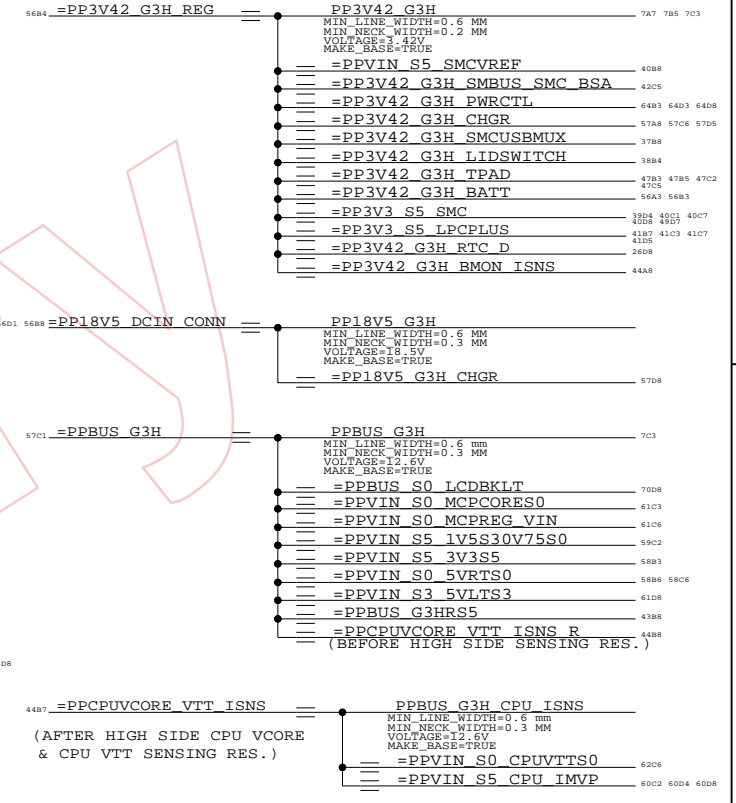
"S3" RAILS



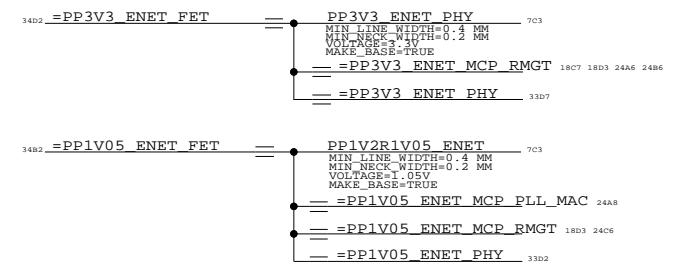
"S5" RAILS



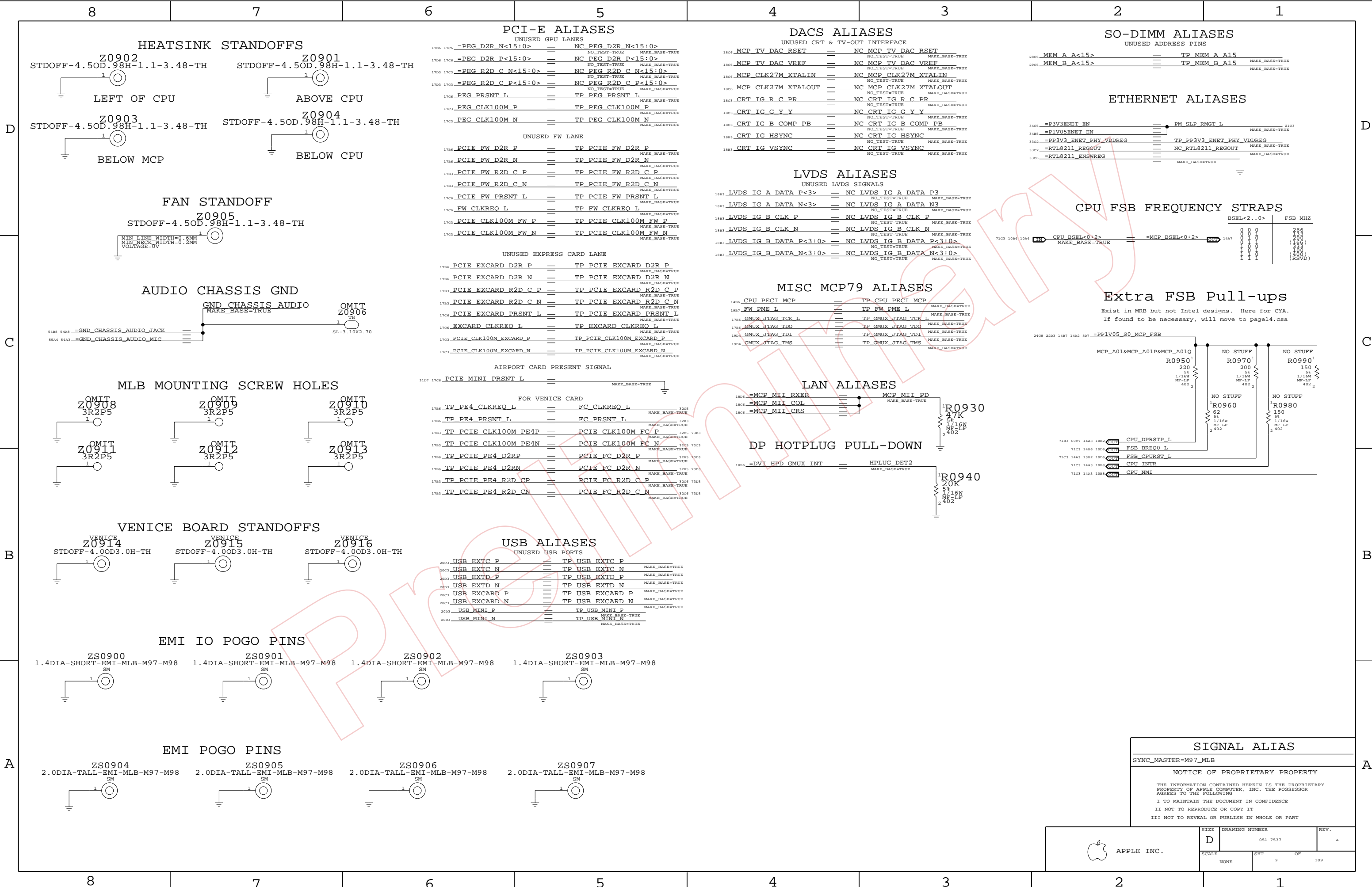
"G3H" RAILS



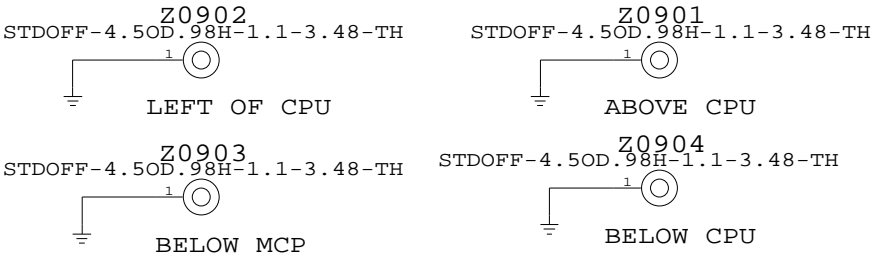
"ENET" RAILS



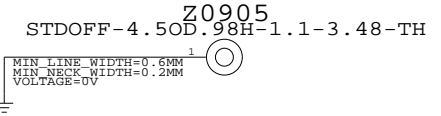
Power Aliases		
SYNC_MASTER=BEN		
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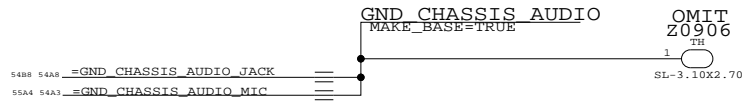
HEATSINK STANDOFFS



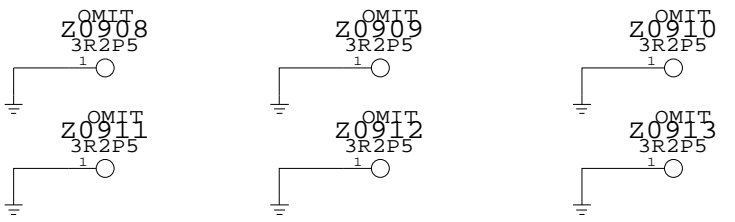
FAN STANDOFF



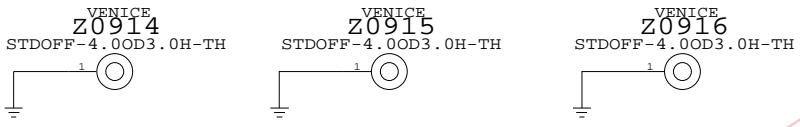
AUDIO CHASSIS GND



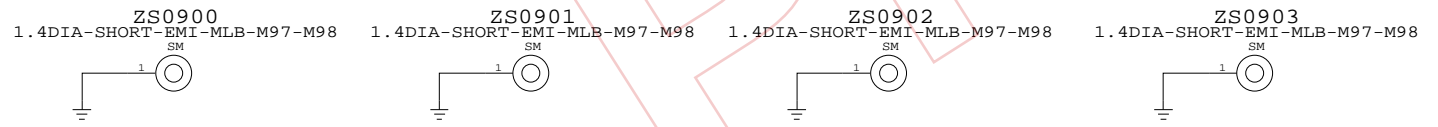
MLB MOUNTING SCREW HOLES



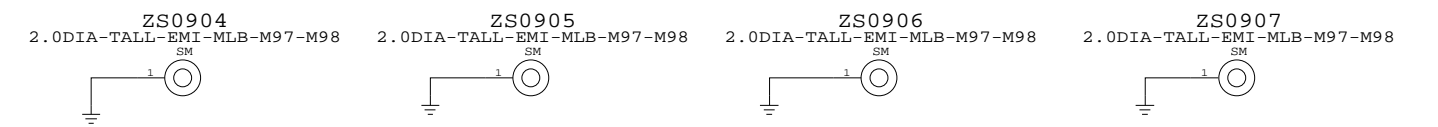
VENICE BOARD STANDOFFS



EMI IO POGO PINS



EMI POGO PINS



PCI-E ALIASES

UNUSED GPU LANES

1706 =PEG D2R N<15:0> == NC PEG D2R N<15:0>

1706 =PEG D2R P<15:0> == NC PEG D2R P<15:0>

1703 =PEG R2D C N<15:0> == NC PEG R2D C N<15:0>

1703 =PEG R2D C P<15:0> == NC PEG R2D C P<15:0>

1706 PEG PRSNT L == TP PEG PRSNT L

1703 PEG CLK100M P == TP PEG CLK100M P

1703 PEG CLK100M N == TP PEG CLK100M N

UNUSED FW LANE

1786 PCIE FW D2R P == TP PCIE FW D2R P

1786 PCIE FW D2R N == TP PCIE FW D2R N

1783 PCIE FW R2D C P == TP PCIE FW R2D C P

1783 PCIE FW R2D C N == TP PCIE FW R2D C N

1706 PCIE FW PRSNT L == TP PCIE FW PRSNT L

1706 FW CLKREQ L == TP FW CLKREQ L

1703 PCIE CLK100M FW P == TP PCIE CLK100M FW P

1703 PCIE CLK100M FW N == TP PCIE CLK100M FW N

UNUSED EXPRESS CARD LANE

1784 PCIE EXCARD D2R P == TP PCIE EXCARD D2R P

1784 PCIE EXCARD D2R N == TP PCIE EXCARD D2R N

1783 PCIE EXCARD R2D C P == TP PCIE EXCARD R2D C P

1783 PCIE EXCARD R2D C N == TP PCIE EXCARD R2D C N

1706 PCIE EXCARD PRSNT L == TP PCIE EXCARD PRSNT L

1706 EXCARD CLKREQ L == TP EXCARD CLKREQ L

1703 PCIE CLK100M EXCARD P == TP PCIE CLK100M EXCARD P

1703 PCIE CLK100M EXCARD N == TP PCIE CLK100M EXCARD N

AIRPORT CARD PRESENT SIGNAL

3107 1706 PCIE MINI PRSNT L == MAKE_BASE=TRUE

FOR VENICE CARD

1786 TP PE4 CLKREQ L == FC CLKREQ L

1786 TP PE4 PRSNT L == FC PRSNT L

1783 TP PCIE CLK100M PE4P == PCIE CLK100M FC P

1783 TP PCIE CLK100M PE4N == PCIE CLK100M FC N

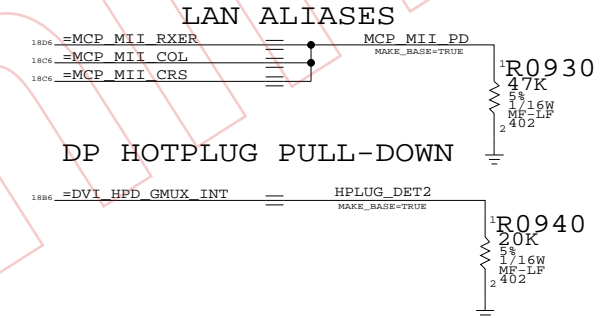
1786 TP PCIE PE4 D2RP == PCIE FC D2R P

1786 TP PCIE PE4 D2RN == PCIE FC D2R N

1783 TP PCIE PE4 R2D CP == PCIE FC R2D C P

1783 TP PCIE PE4 R2D CN == PCIE FC R2D C N

LAN ALIASES



USB ALIASES

UNUSED USB PORTS

2003 USB EXTC P == TP USB EXTC P

2003 USB EXTC N == TP USB EXTC N

2003 USB EXTD P == TP USB EXTD P

2003 USB EXTD N == TP USB EXTD N

2003 USB EXCARD P == TP USB EXCARD P

2003 USB EXCARD N == TP USB EXCARD N

2003 USB MINI P == TP USB MINI P

2003 USB MINI N == TP USB MINI N

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

1806 MCP TV DAC RSET == NC MCP TV DAC RSET

1806 MCP TV DAC VREF == NC MCP TV DAC VREF

1806 MCP CLK27M XTALIN == NC MCP CLK27M XTALIN

1806 MCP CLK27M XTALOUT == NC MCP CLK27M XTALOUT

1803 CRT IG R C PR == NC CRT IG R C PR

1803 CRT IG G Y Y == NC CRT IG G Y Y

1803 CRT IG B COMP PB == NC CRT IG B COMP PB

1883 CRT IG HSYNC == NC CRT IG HSYNC

1883 CRT IG VSYNC == NC CRT IG VSYNC

LVDS ALIASES

UNUSED LVDS SIGNALS

1883 LVDS IG A DATA P<3> == NC LVDS IG A DATA P3

1883 LVDS IG A DATA N<3> == NC LVDS IG A DATA N3

1883 LVDS IG B CLK P == NC LVDS IG B CLK P

1883 LVDS IG B CLK N == NC LVDS IG B CLK N

1883 LVDS IG B DATA P<3:0> == NC LVDS IG B DATA P<3:0>

1883 LVDS IG B DATA N<3:0> == NC LVDS IG B DATA N<3:0>

MISC MCP79 ALIASES

1486 CPU PECl MCP == TP CPU PECl MCP

1987 FW PME L == TP FW PME L

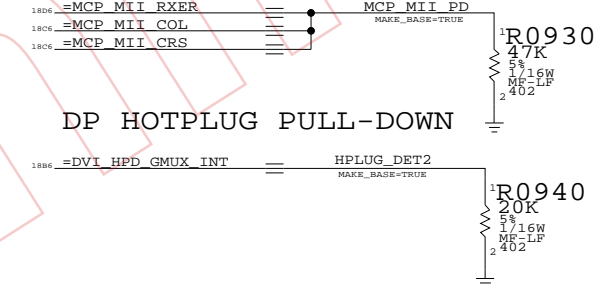
1786 GMUX JTAG TCK L == TP GMUX JTAG TCK L

1786 GMUX JTAG TDO == TP GMUX JTAG TDO

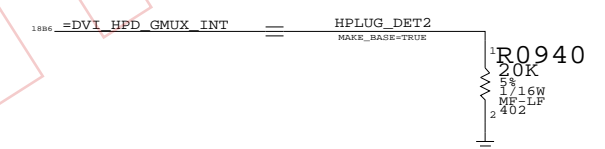
1904 GMUX JTAG TDI == TP GMUX JTAG TDI

1904 GMUX JTAG TMS == TP GMUX JTAG TMS

LAN ALIASES



DP HOTPLUG PULL-DOWN



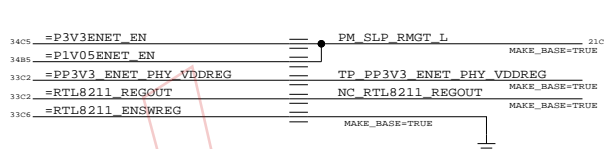
SO-DIMM ALIASES

UNUSED ADDRESS PINS

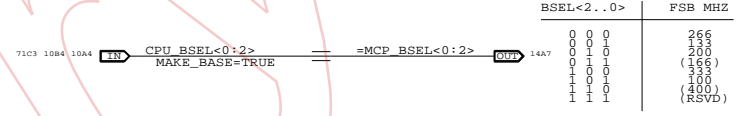
2805 MEM A A<15> == TP MEM A A15

2905 MEM B A<15> == TP MEM B A15

ETHERNET ALIASES

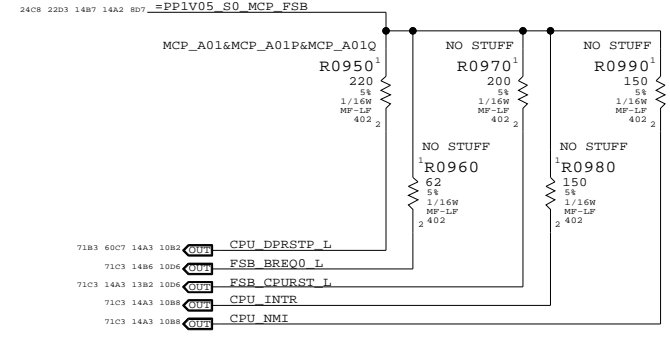


CPU FSB FREQUENCY STRAPS



Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa



SIGNAL ALIAS

SYNC_MASTER=M97_MLB

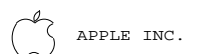
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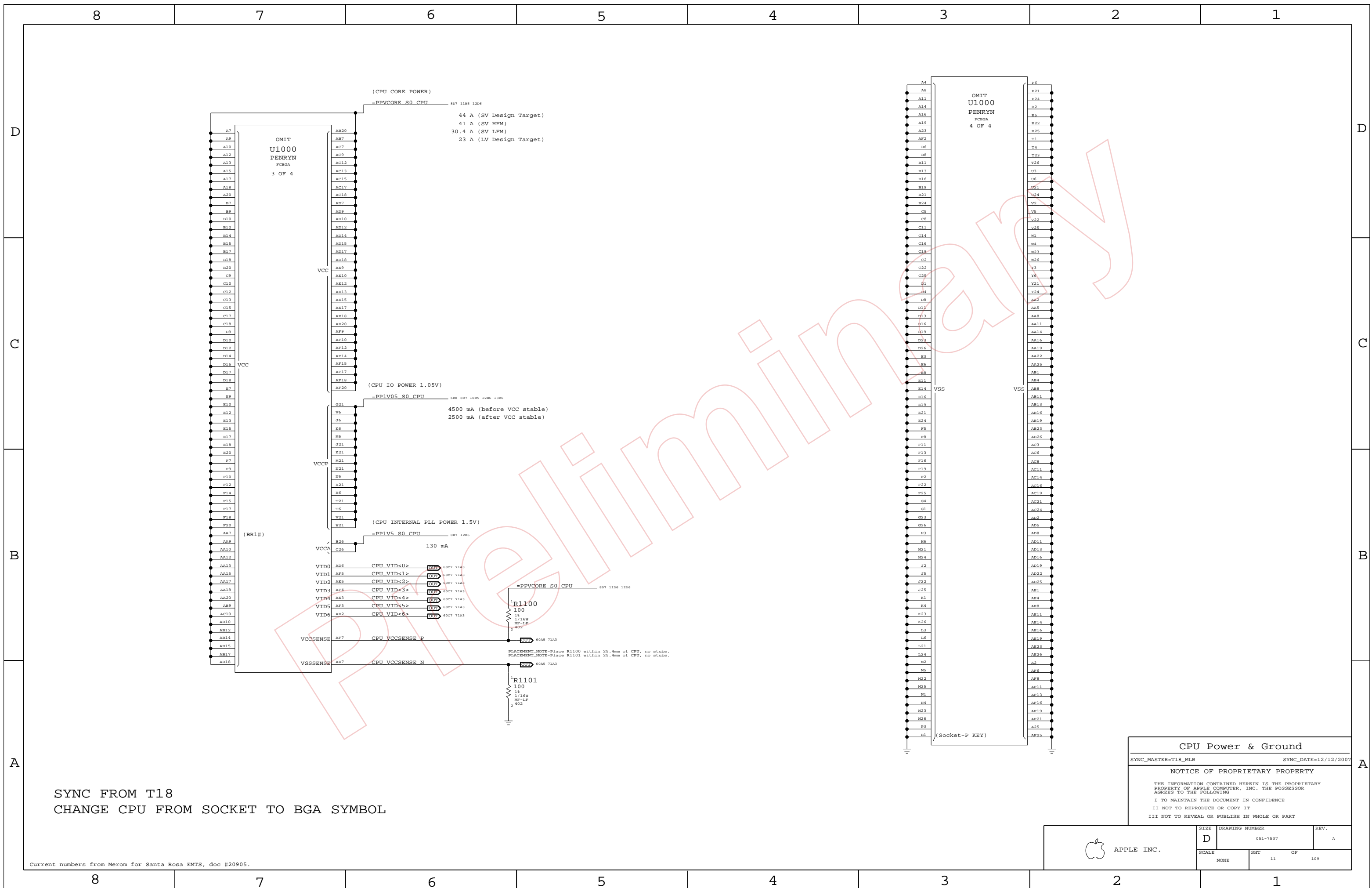
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D	051-7537	A
SCALE	SHT	OF
NONE	9	109



SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

NOTICE OF PROPRIETARY PROPERTY

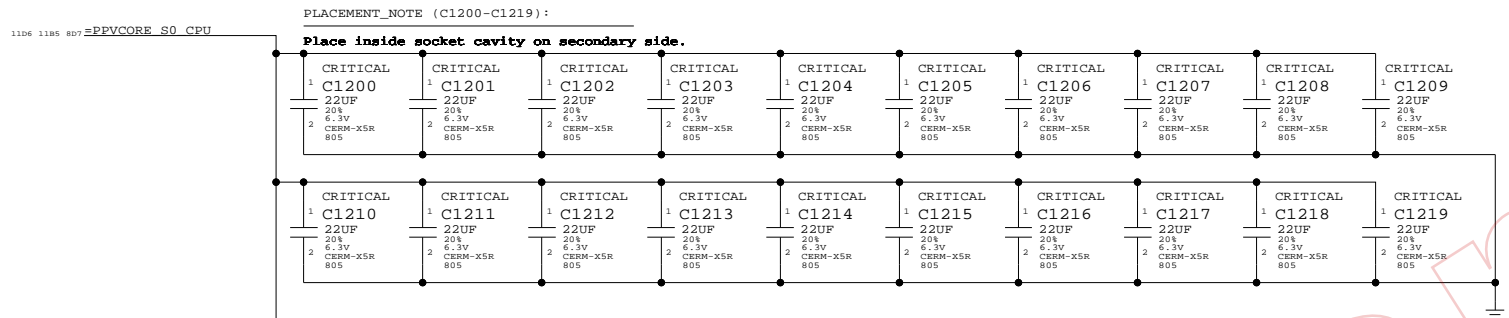
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	SCALE NONE	SHEET 11	OF 109

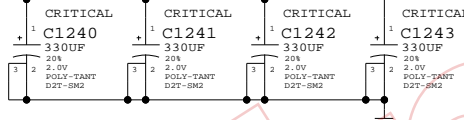
CPU VCore HF and Bulk Decoupling

4X 330UF, 20X 22UF 0805



PLACEMENT_NOTE (C1240-C1243):

Place on secondary side.

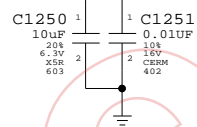


VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF

1186 807=PP1V5_S0_CPU

PLACEMENT_NOTE=Place C1281 near CPU pin B26.

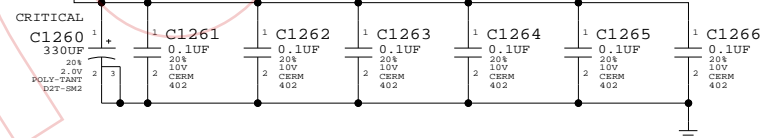


VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402

1106 1106 1005 807 608=PP1V05_S0_CPU

PLACEMENT_NOTE=Place C1260 between CPU & NB.

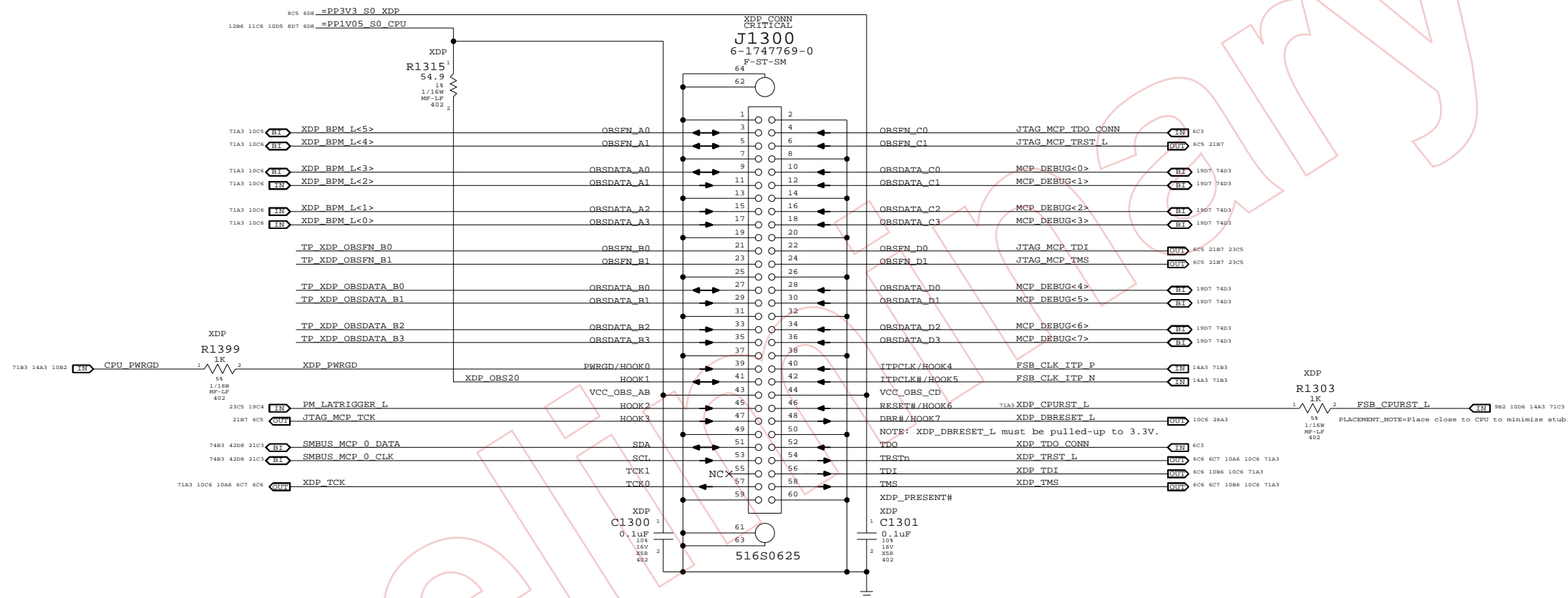


SYNC FROM T18
 REMOVE NO STUFF CAPS C1220 TO C1231
 REMOVE C1244 & C1245
 CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

CPU Decoupling		
SYNC_MASTER=RAYMOND	SYNC_DATE=03/31/2008	
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	D	051-7537	A
SCALE	SHT	OF	109
NONE	12		

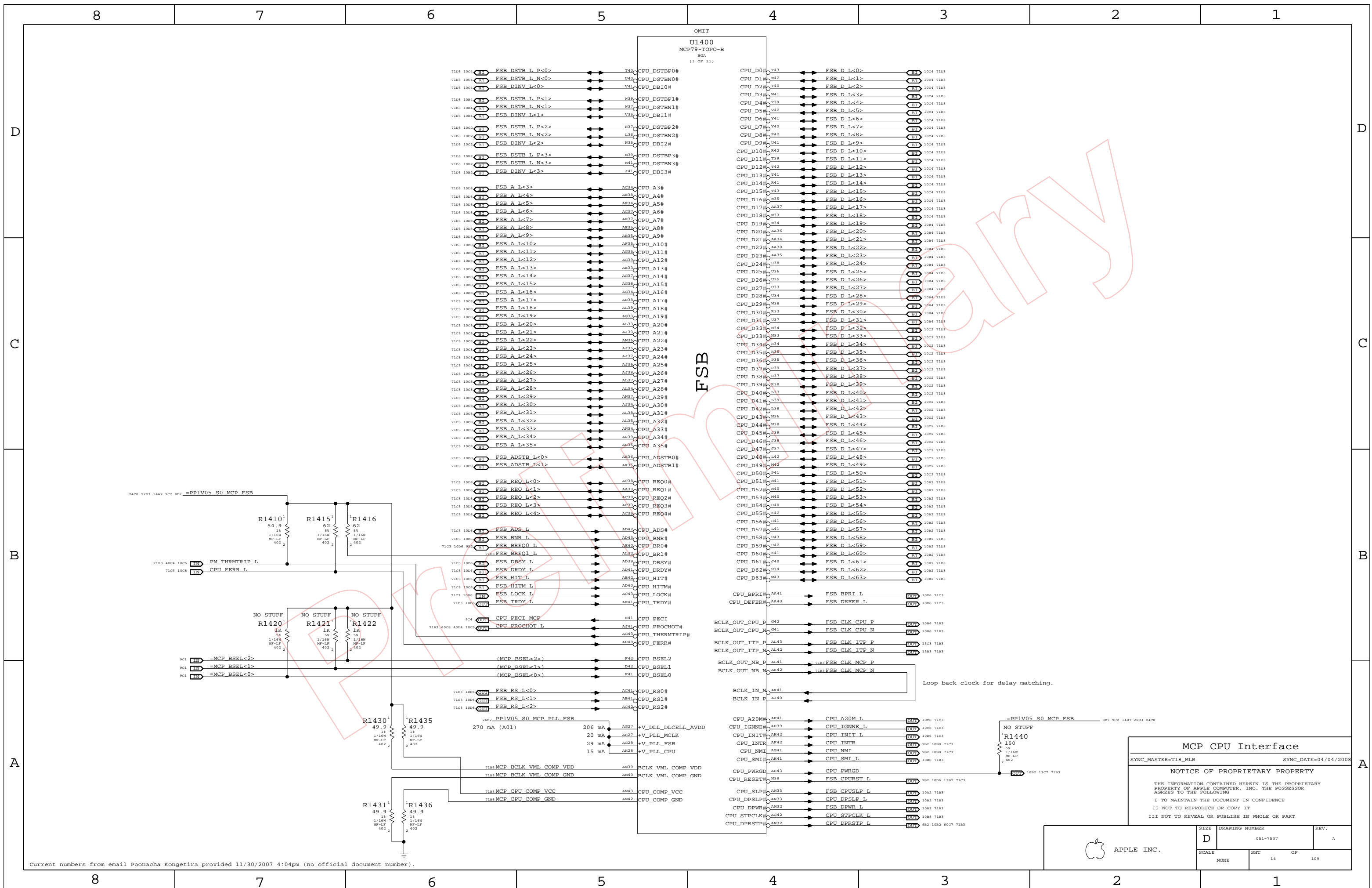
MCP79-specific pinout



SYNC FROM T18
 CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
 RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
 RENAME XDP_TDO TO XDP_TDO_CONN

eXtended Debug Port (XDP)
 SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007
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	SCALE NONE	SHEETS 13	OF 109



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MCP CPU Interface

SYNC_MASTER=TI8_MLB SYNC_DATE=04/04/2008

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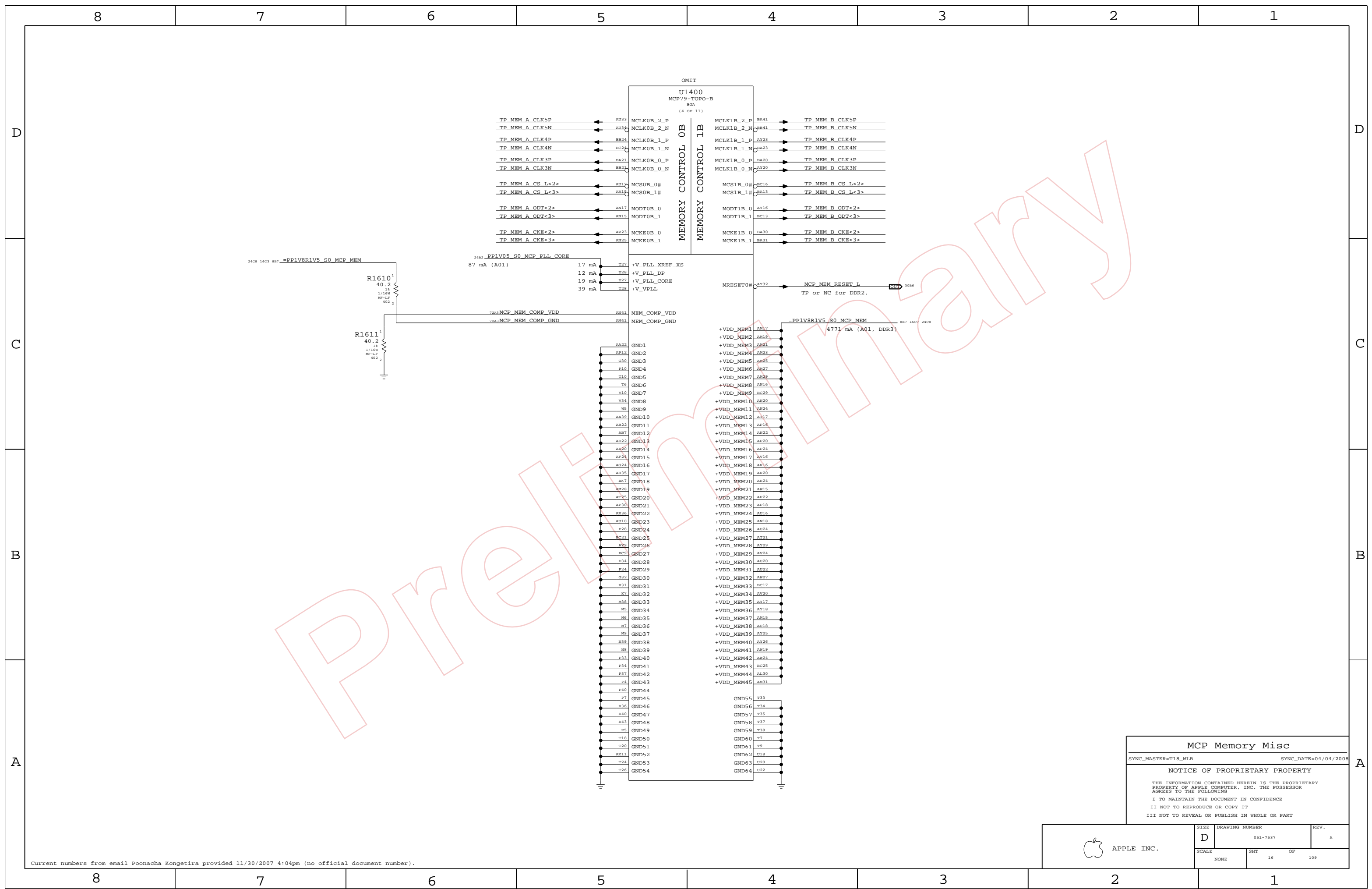
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	SCALE NONE	SHEET 14	OF 109



D
C
B
A

D
C
B
A

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

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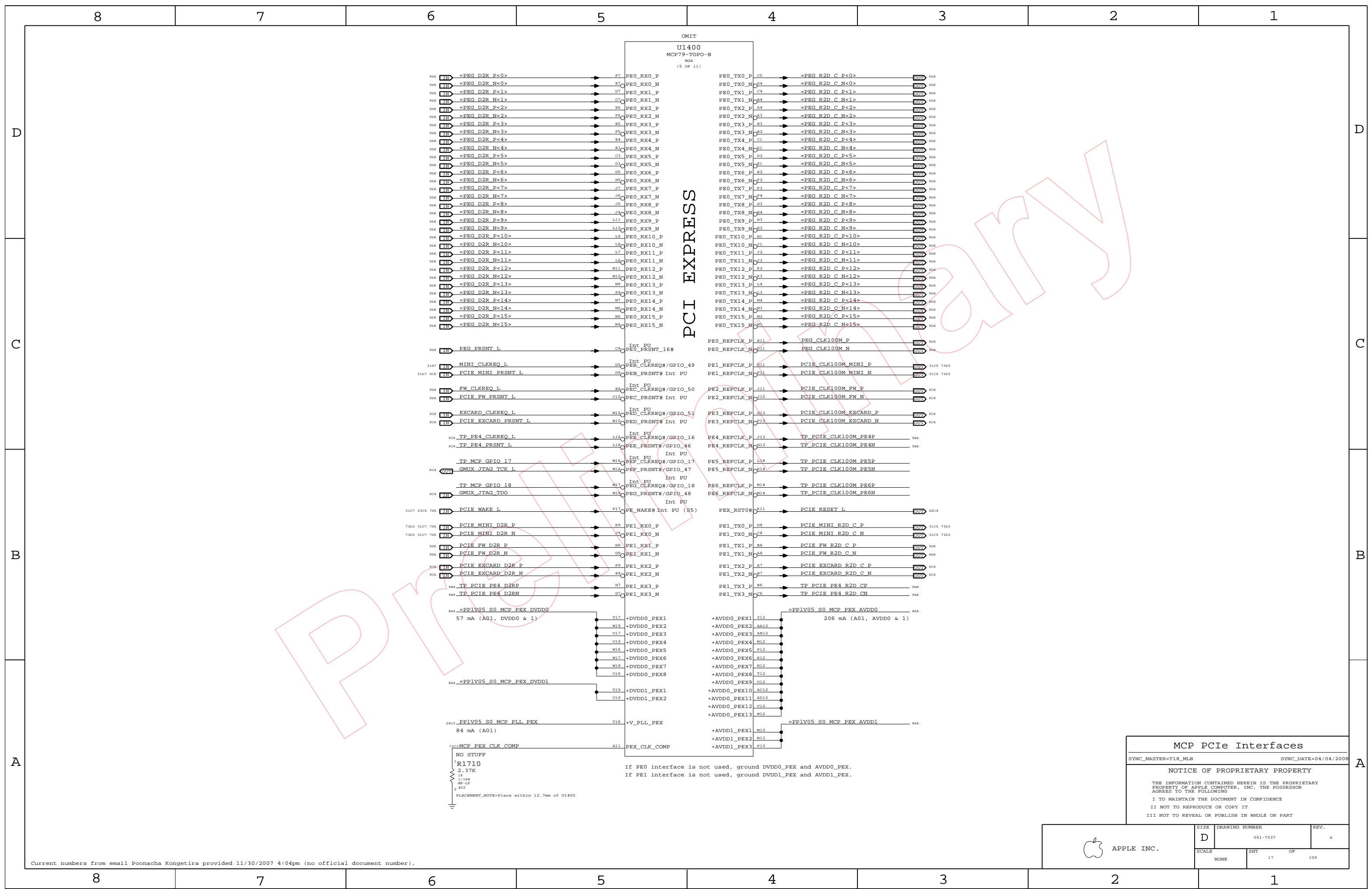
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PCI EXPRESS

MCP PCIe Interfaces

SYNC_MASTER=TI8_MLB SYNC_DATE=04/04/2008

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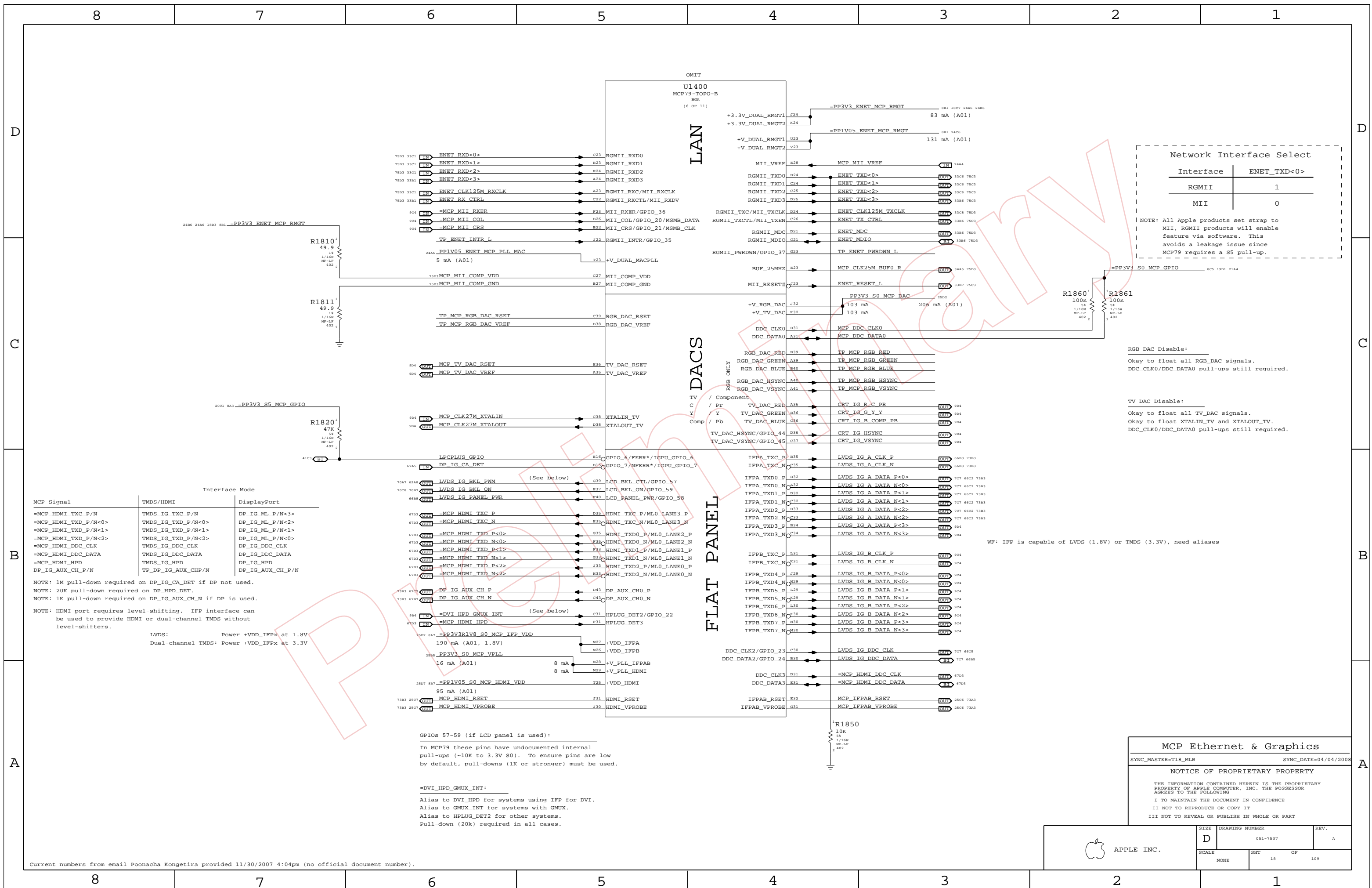
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	SCALE NONE	SHEET 17	OF 109

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Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
 Okay to float all TV_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
 NOTE: 20K pull-down required on DP_HPD_DET.
 NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IPFX at 1.8V
 Dual-channel TMDS: Power +VDD_IPFX at 3.3V

GPIOs 57-59 (if LCD panel is used):
 In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
 Alias to DVI_HPD for systems using IFP for DVI.
 Alias to GMUX_INT for systems with GMUX.
 Alias to HPLUG_DET2 for other systems.
 Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

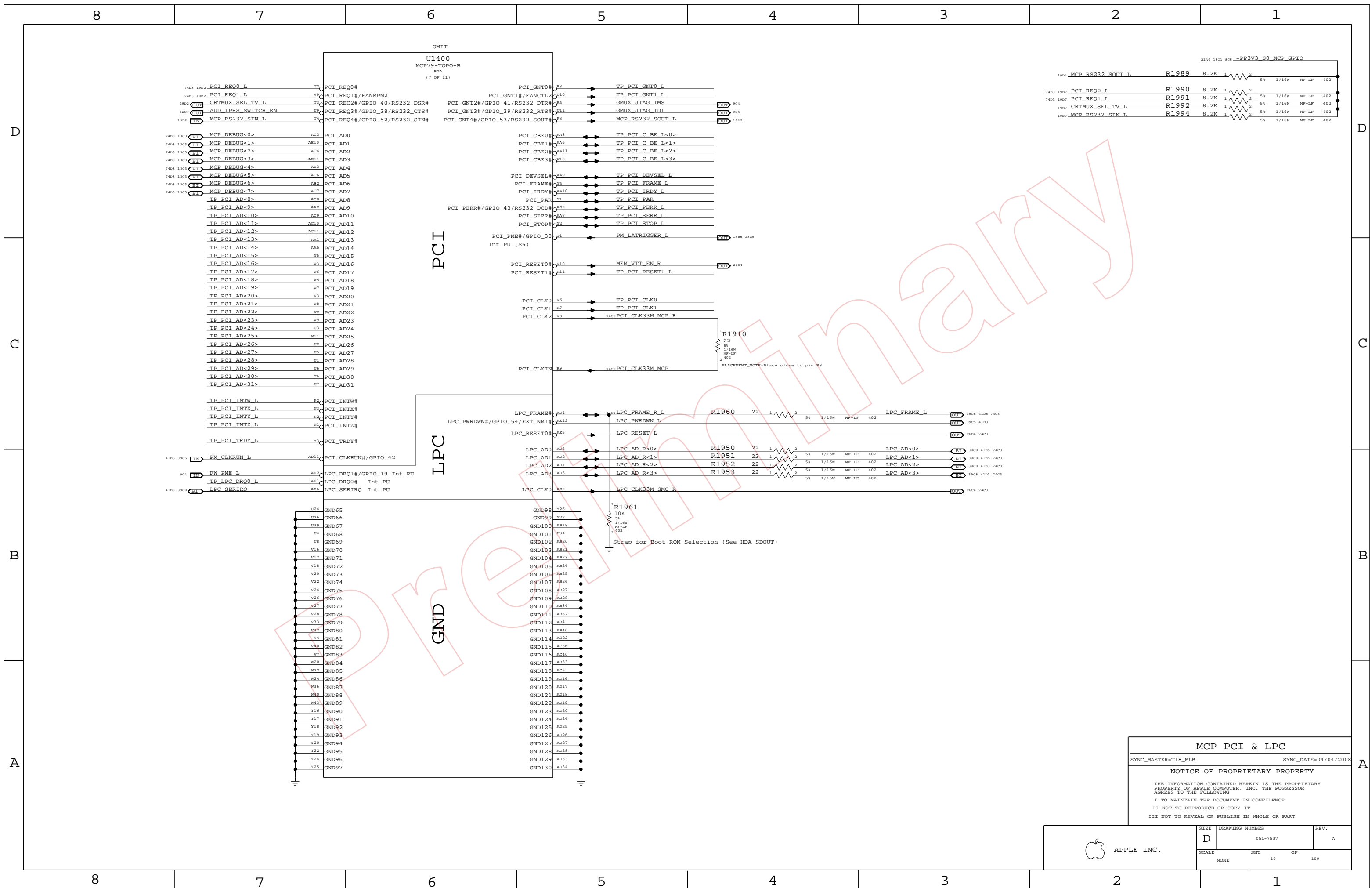
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SCALE	SHT	OF
NONE	18	109



MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

NOTICE OF PROPRIETARY PROPERTY

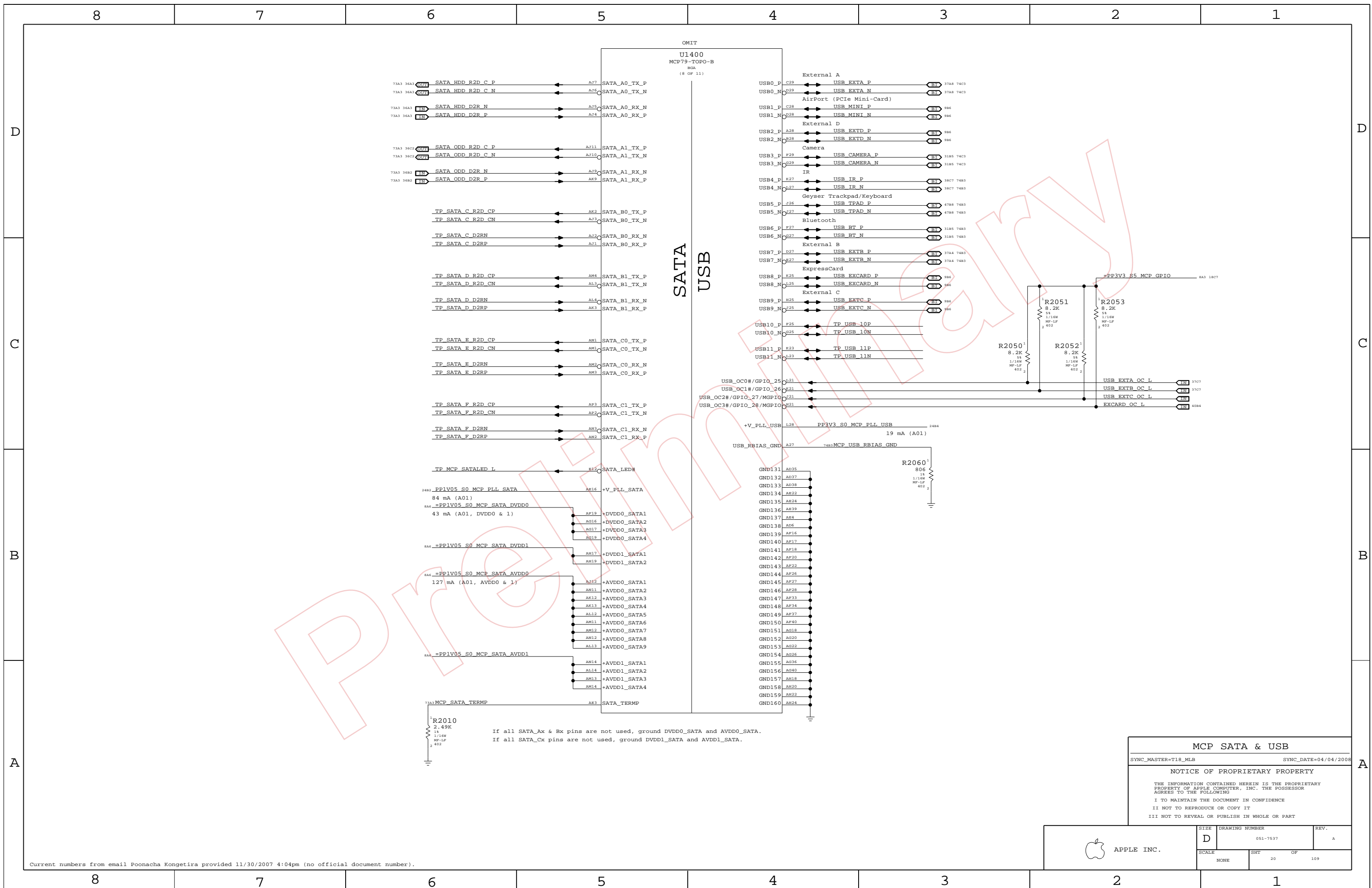
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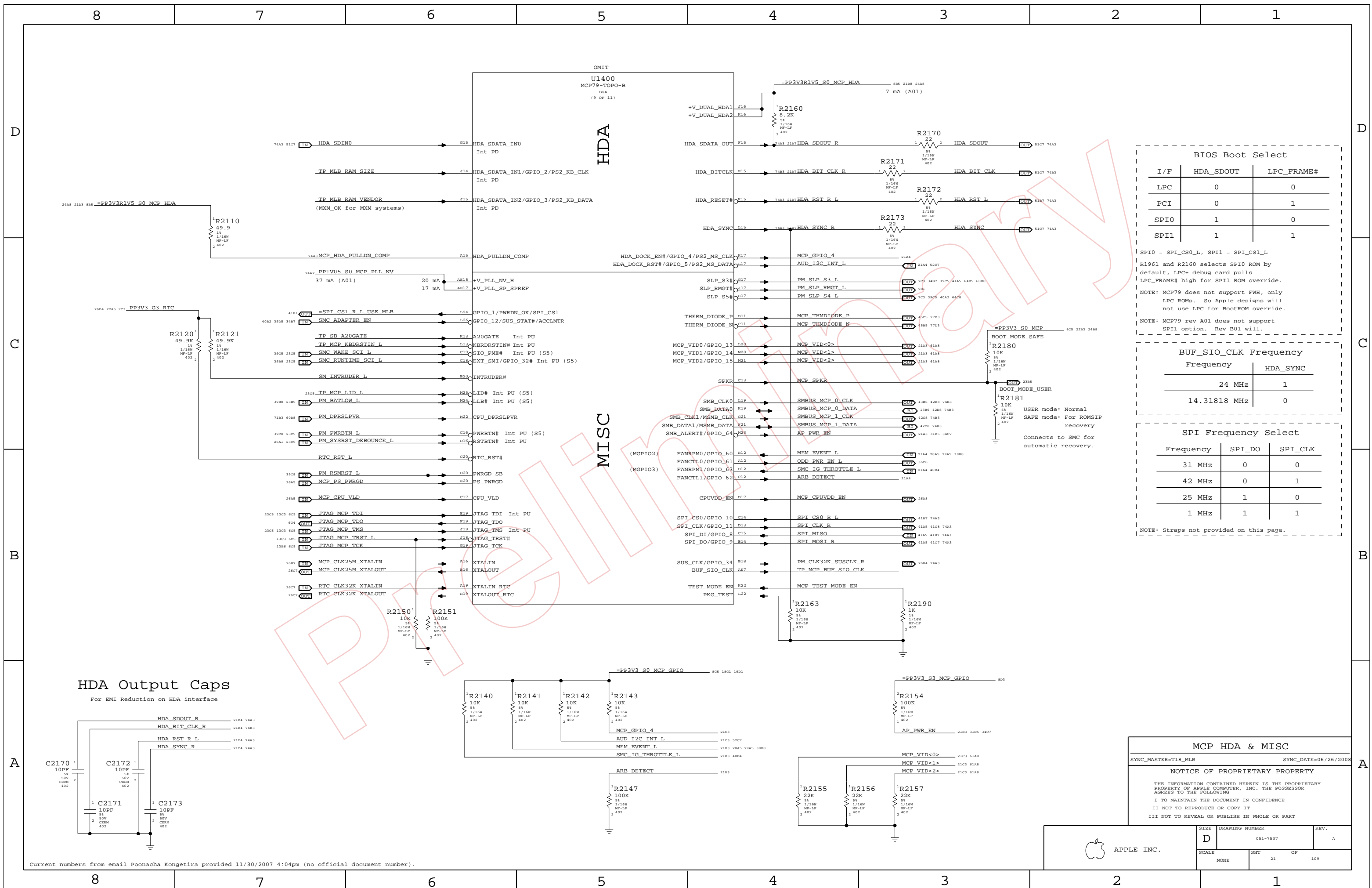
APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHEET 19	OF 109



If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
 If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB
 SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	20		



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
 NOTE: MCP79 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

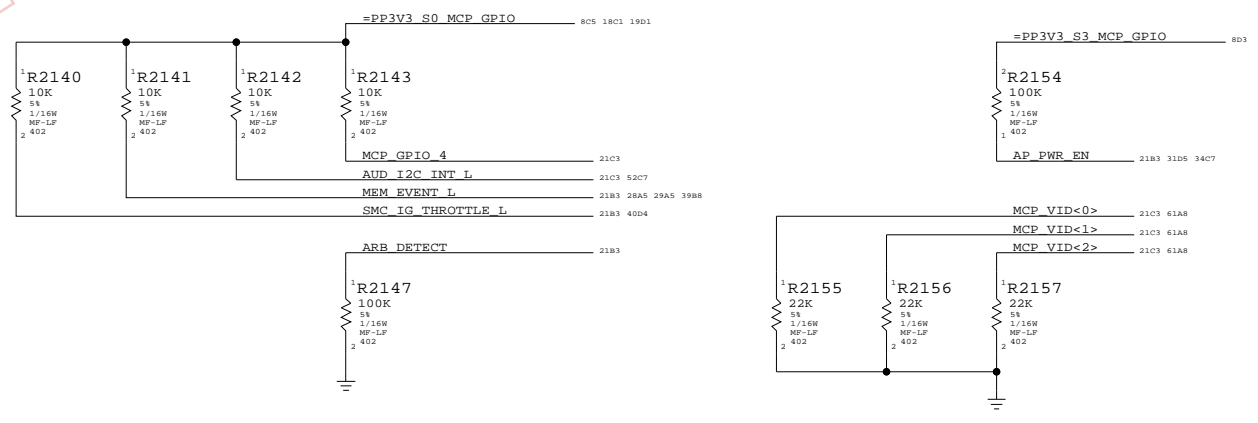
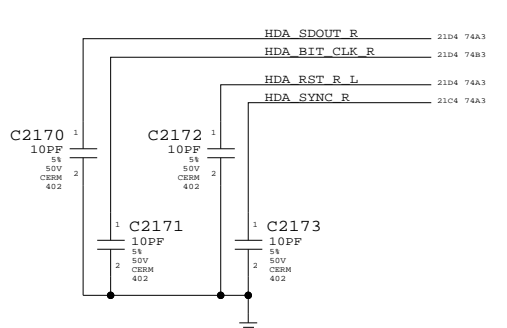
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

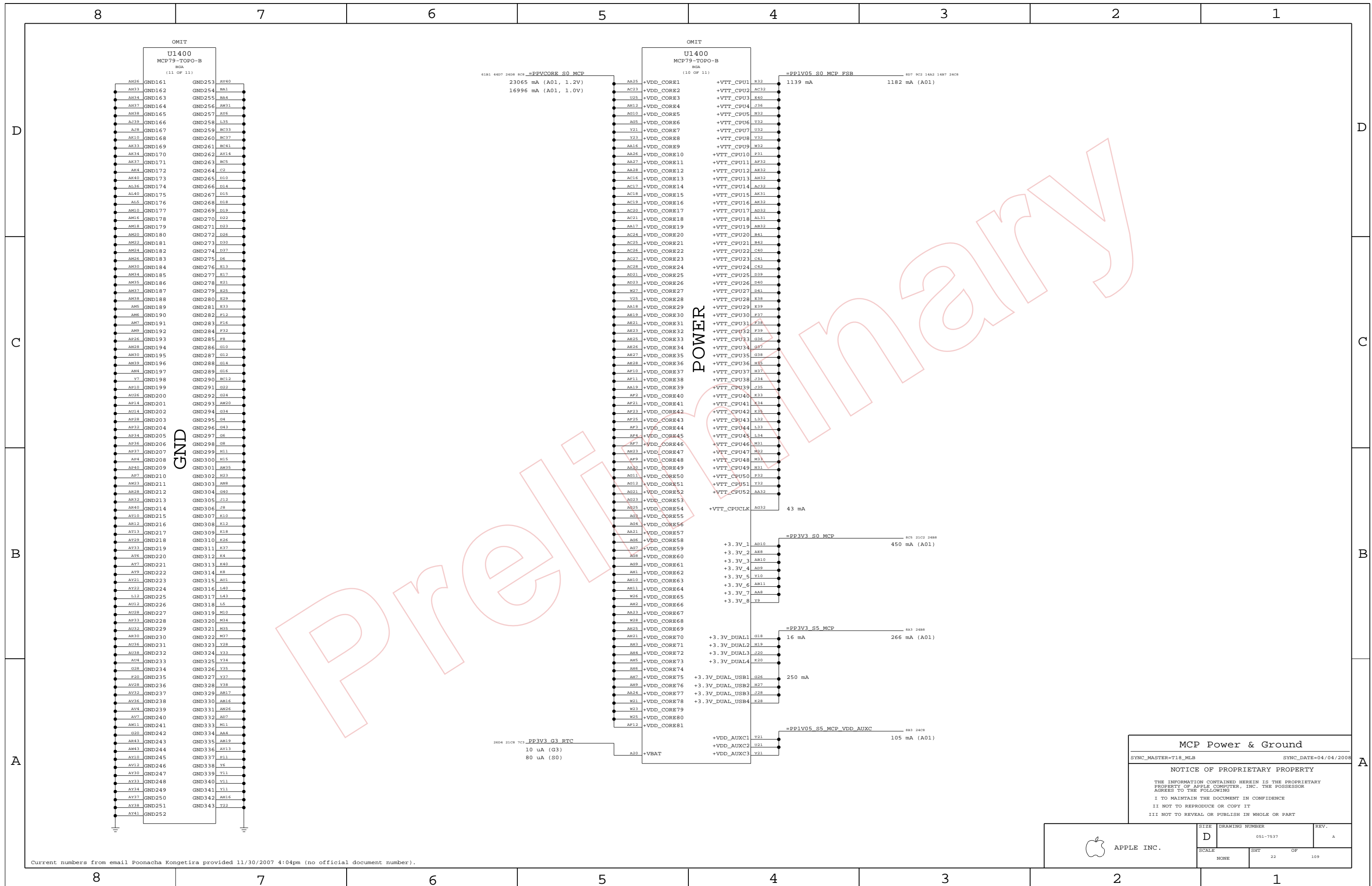
HDA Output Caps
 For EMI Reduction on HDA interface



MCP HDA & MISC
 SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008
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APPLE INC.
 DRAWING NUMBER: 051-7537
 SCALE: NONE
 SHEET: 21 OF 109
 REV: A

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



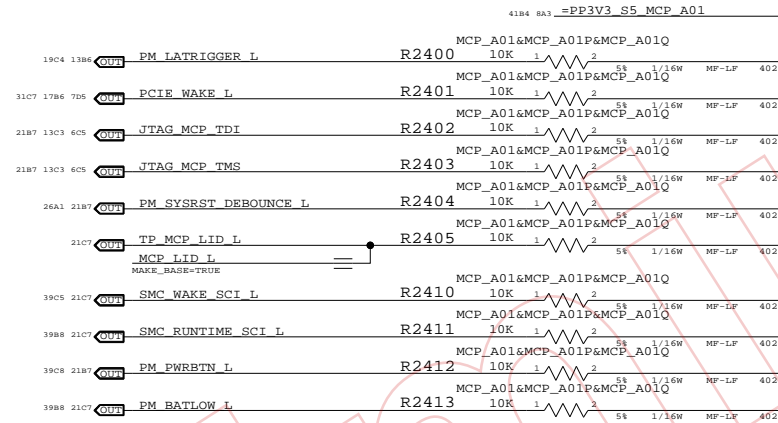
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground
 SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008
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	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	22		

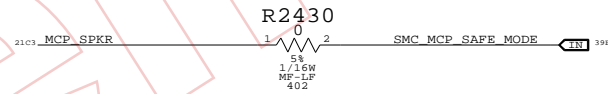
3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345



PRELIMINARY

MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/08/2008

NOTICE OF PROPRIETARY PROPERTY

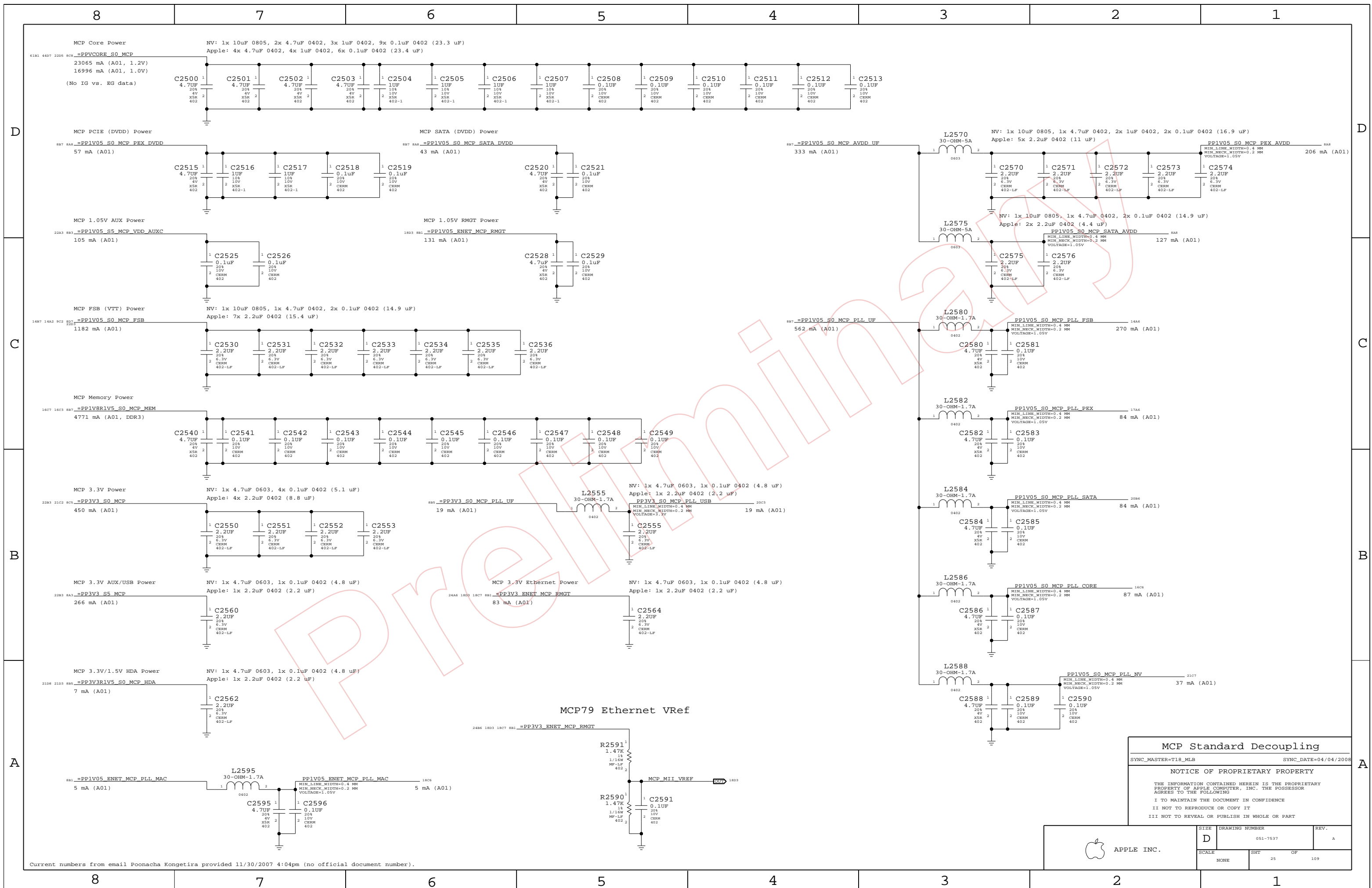
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	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	
NONE	24	109	



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling
 SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	
NONE	25	109	

8

7

6

5

4

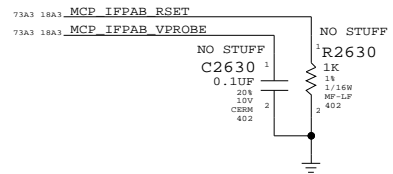
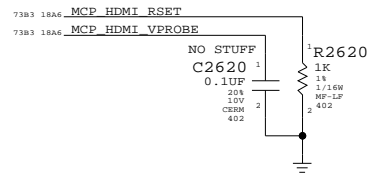
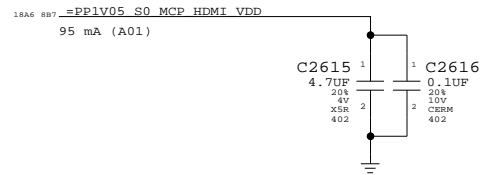
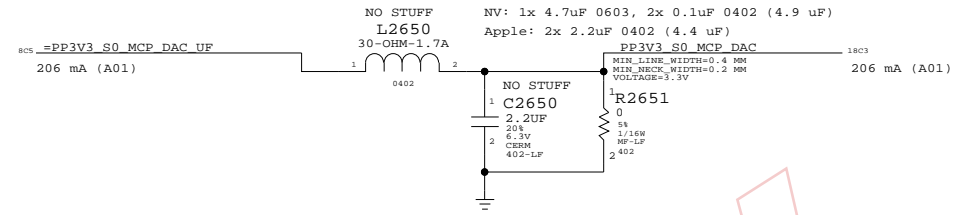
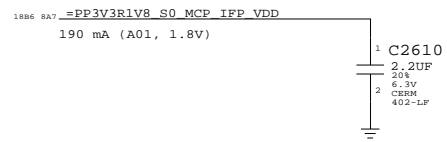
3

2

1

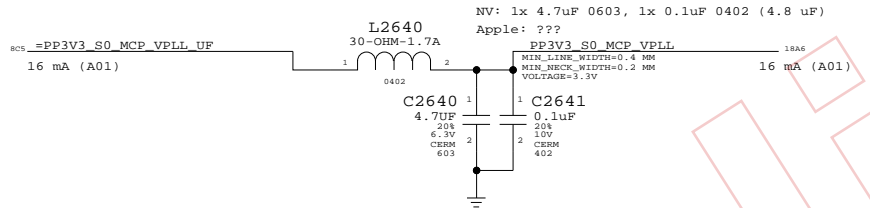
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



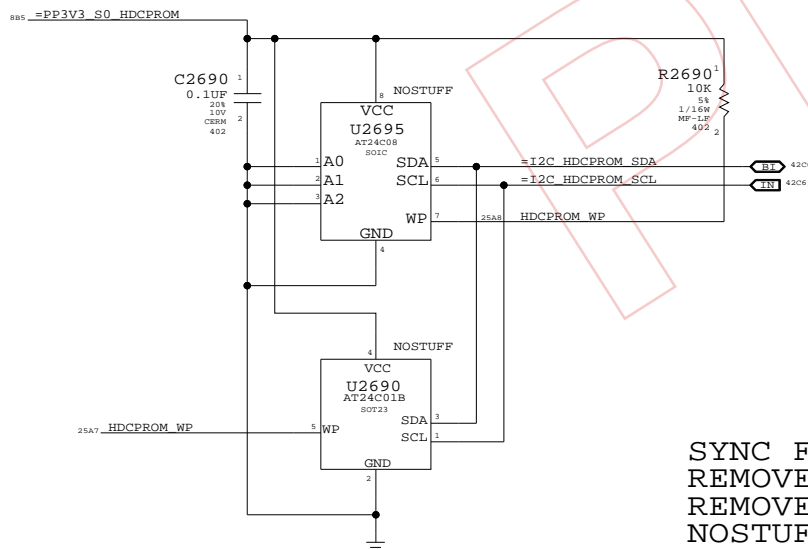
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???



HDCP ROM

WF: Open question on which package option(s) nVidia can support.



SYNC FROM T18
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
 NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
 CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

8

7

6

5

4

3

2

1

D

C

B

A

D

C

B

A

MCP Graphics Support

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

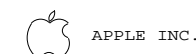
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APPLE INC.

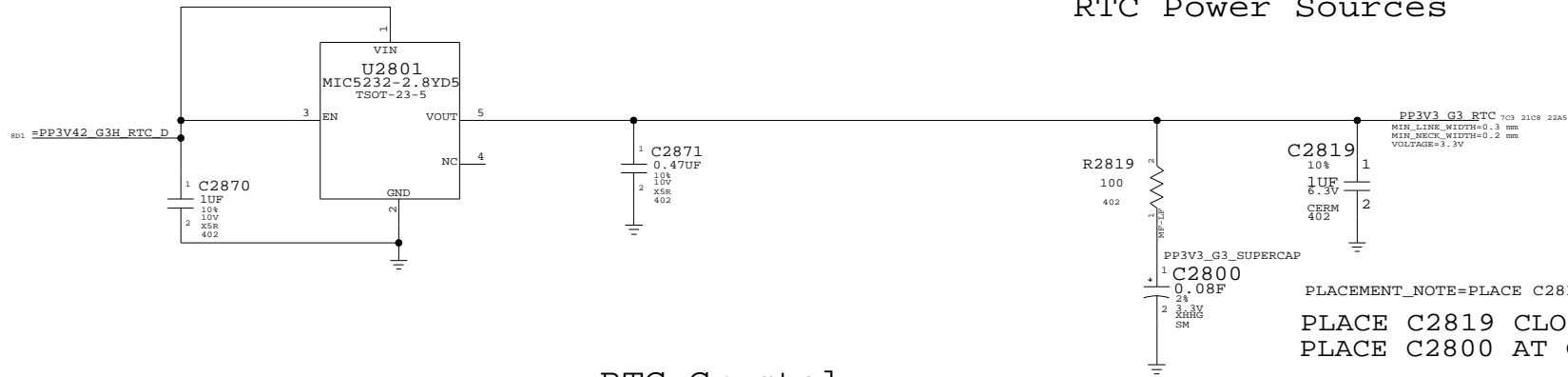
SIZE DRAWING NUMBER REV.

D 051-7537 A

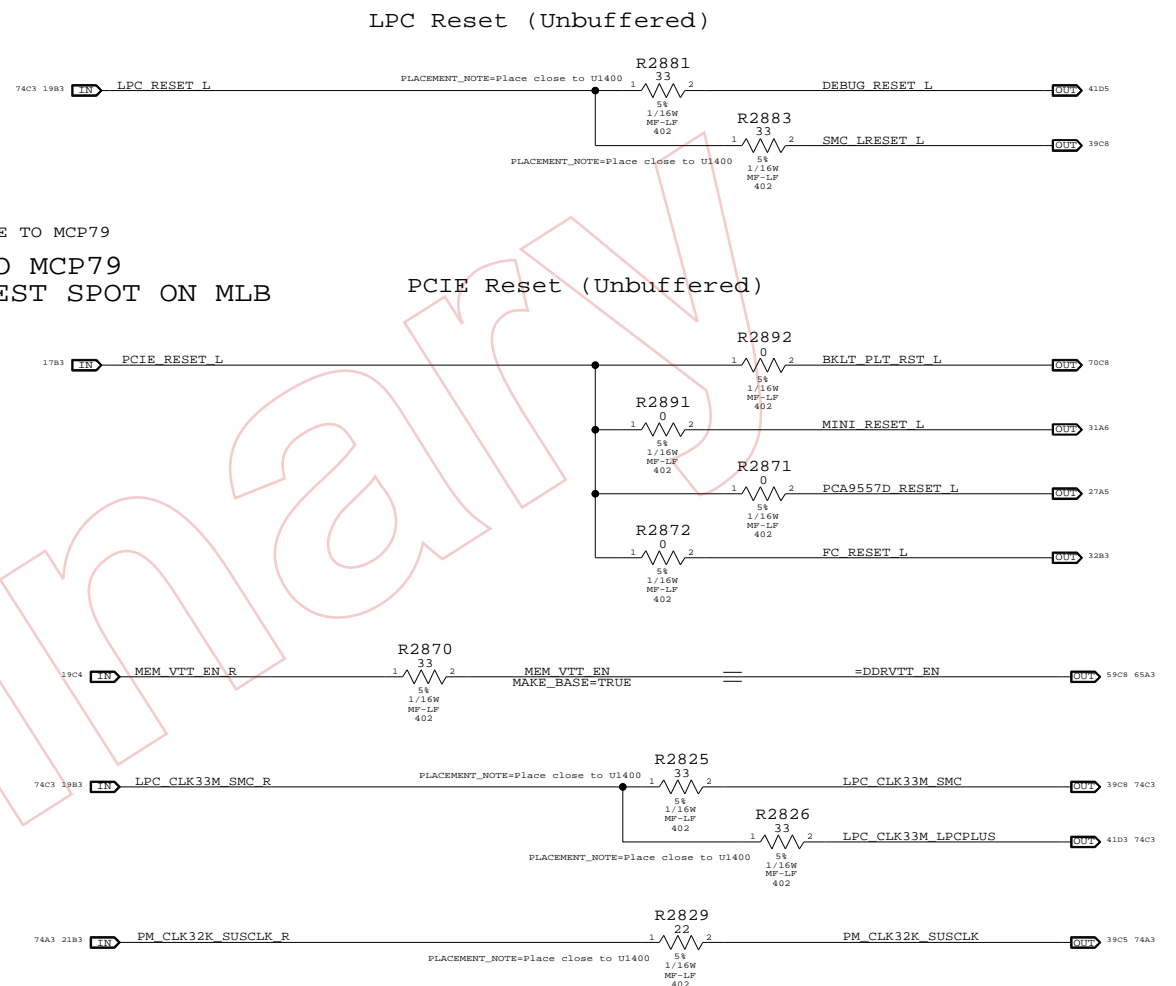
SCALE SHEET OF 109

NONE 26

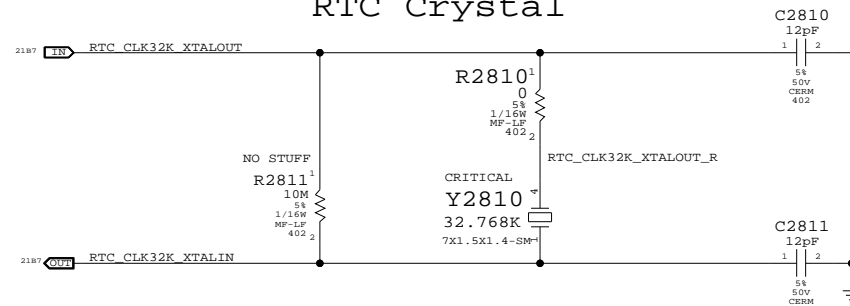
RTC Power Sources



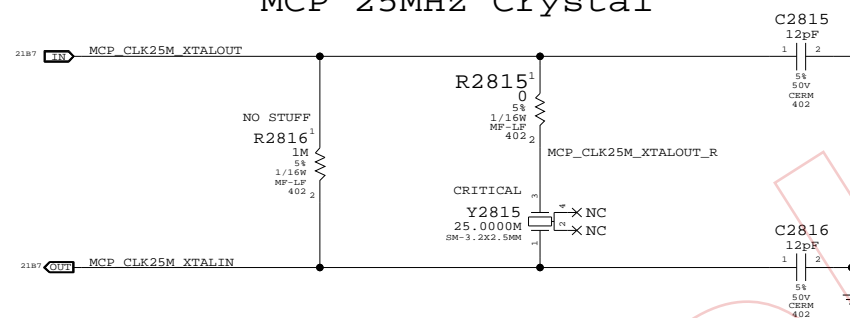
Platform Reset Connections



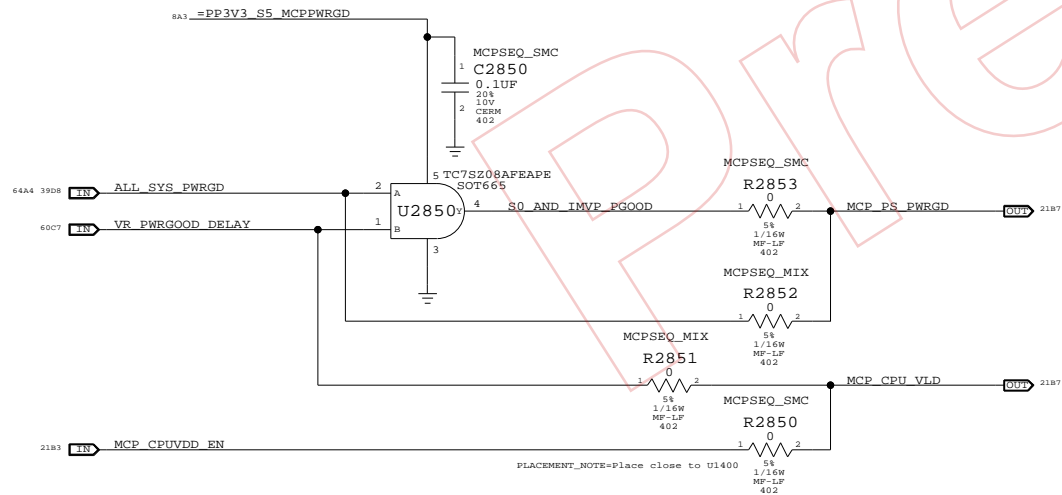
RTC Crystal



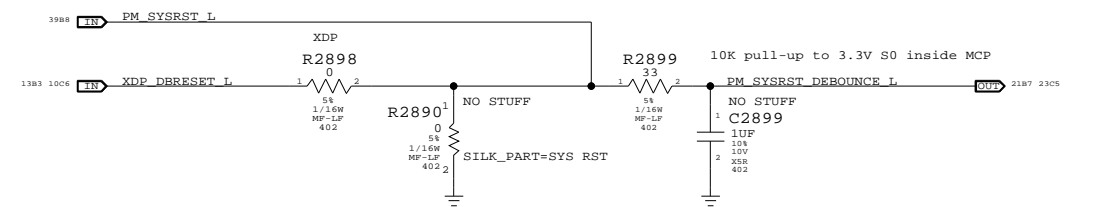
MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



Reset Button



SB Misc

SYNC_MASTER=RAYMOND SYNC_DATE=04/05/2008

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SYNC FROM T18
 CHANGE RESET BUTTON TO RESET PADS
 REMOVE UNUSED PCIE RESET SIGNALS
 REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
 CHANGE RTC COIN CELL TO LDO & SUPERCAP
 ALIAS MEM_VTT_EN TO =DDRVTT_EN
 CHANGE Y2810 AND U2850 TO SMALLER PARTS

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	28		

Page Notes

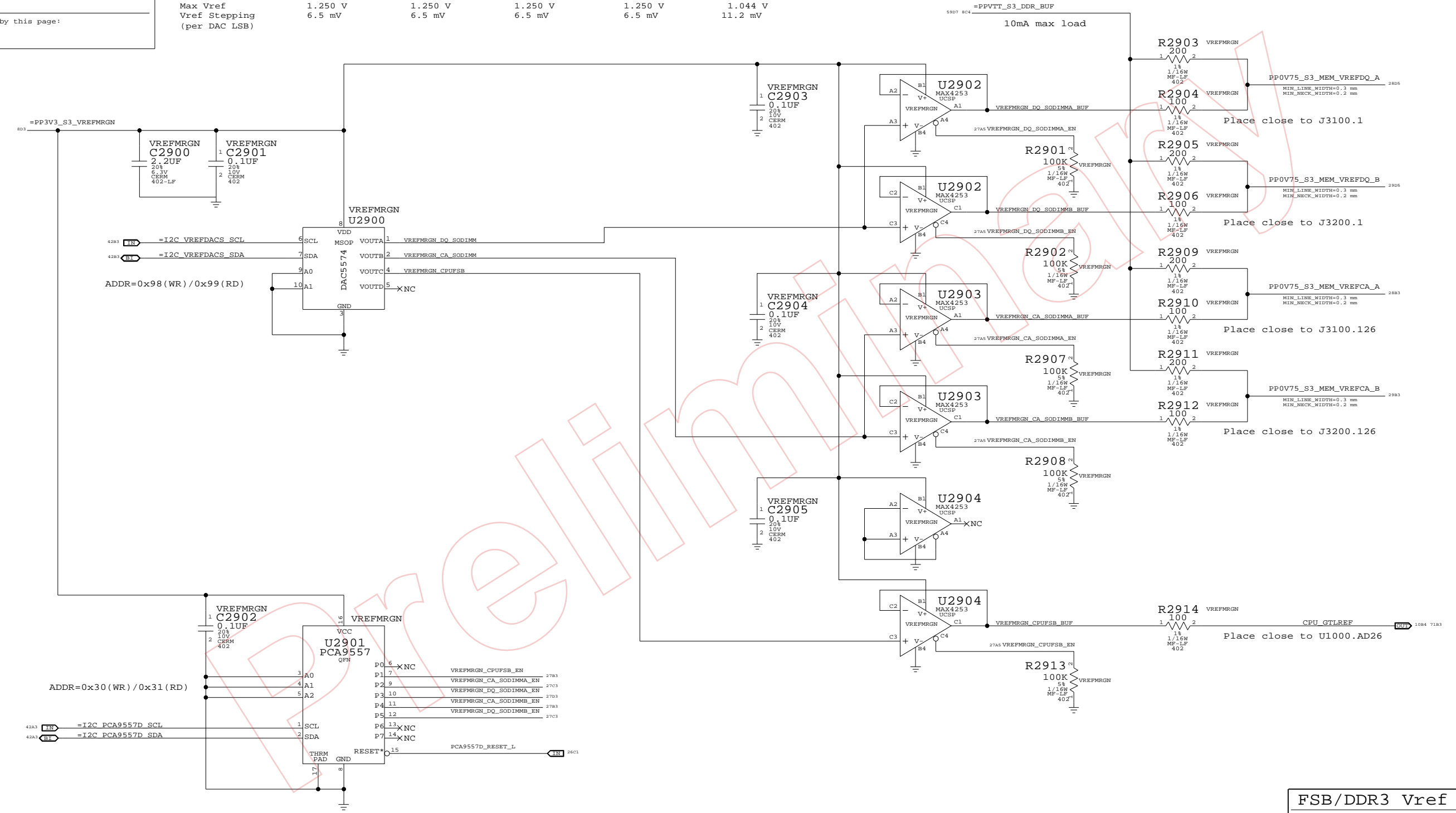
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN
 NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	29	109

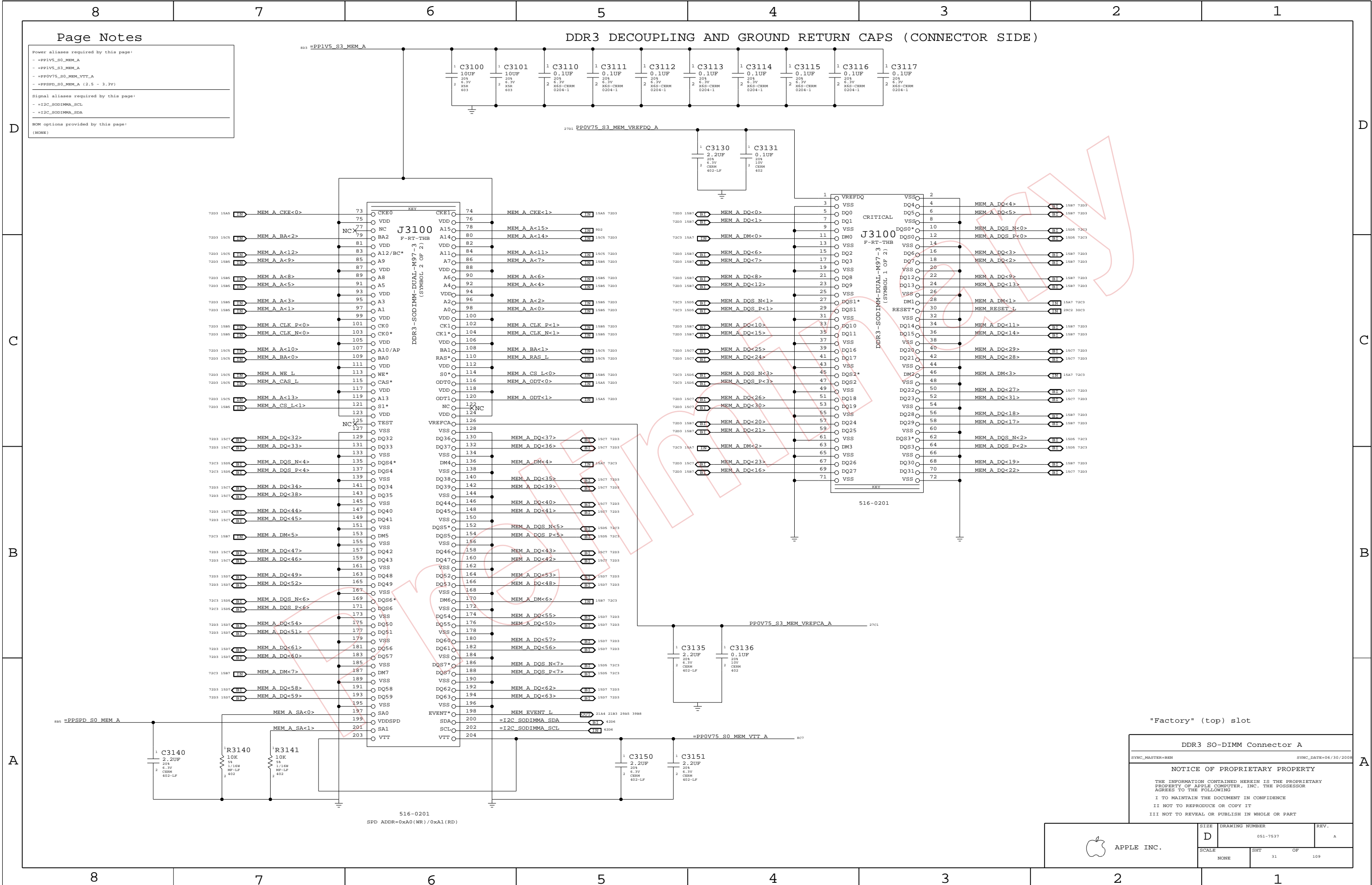
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_A
 - =PP1V5_S3_MEM_A
 - =PP0V75_S0_MEM_VTT_A
 - =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BN SYNC_DATE=06/30/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	NONE	SHT	OF
		31	109

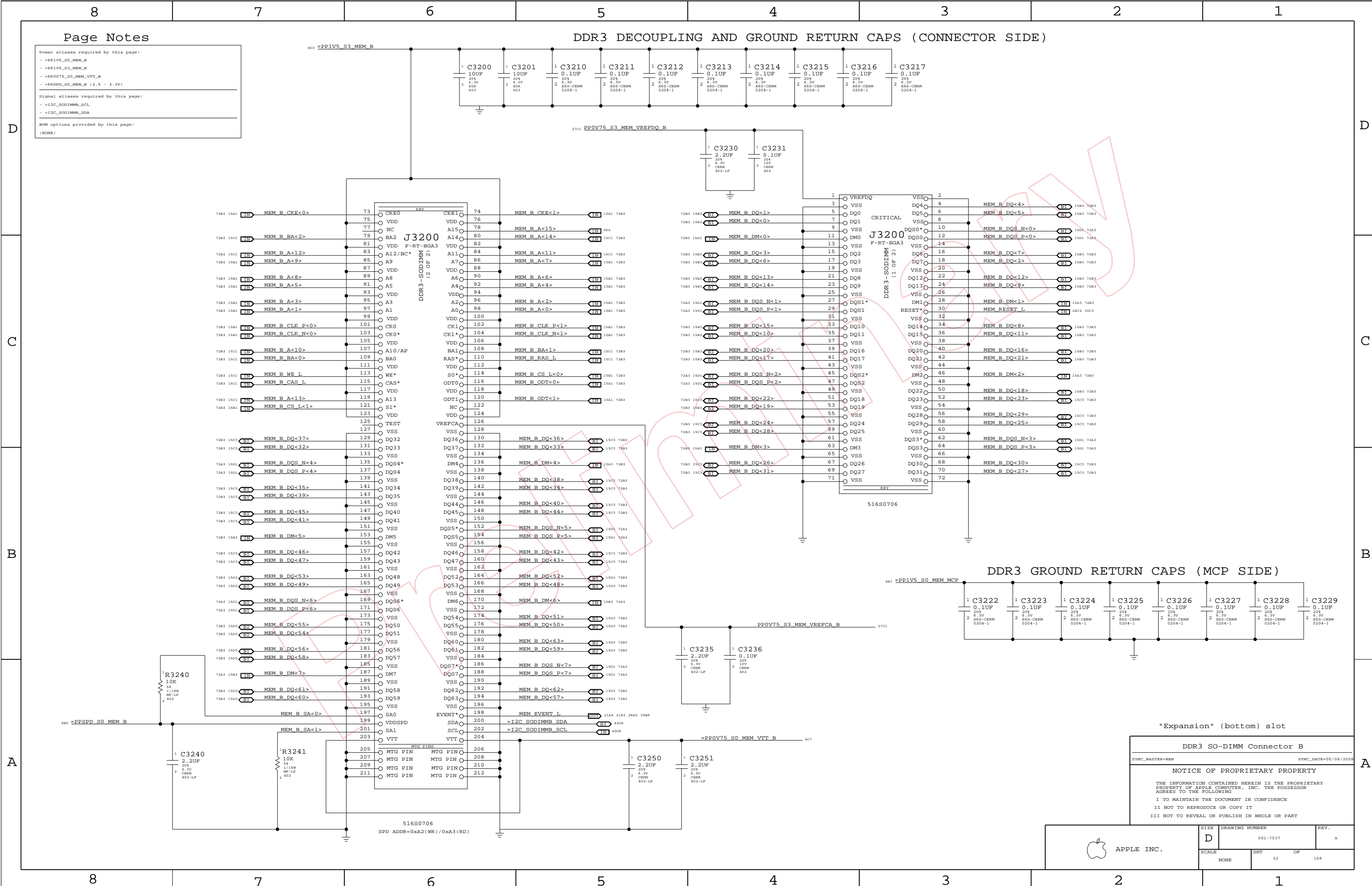
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_B
 - =PP1V5_S3_MEM_B
 - =PP0V75_S0_MEM_VTT_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)

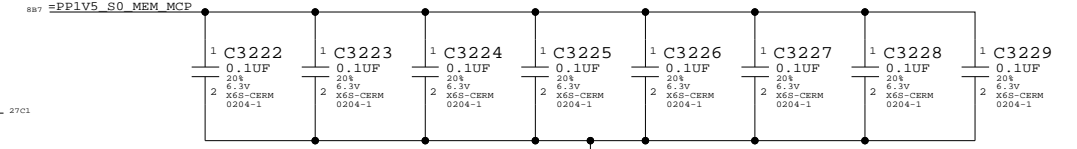
Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

BOM options provided by this page:
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)

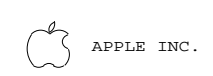


"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B
 SYNC_MASTER=BNB SYNC_DATE=05/09/2008

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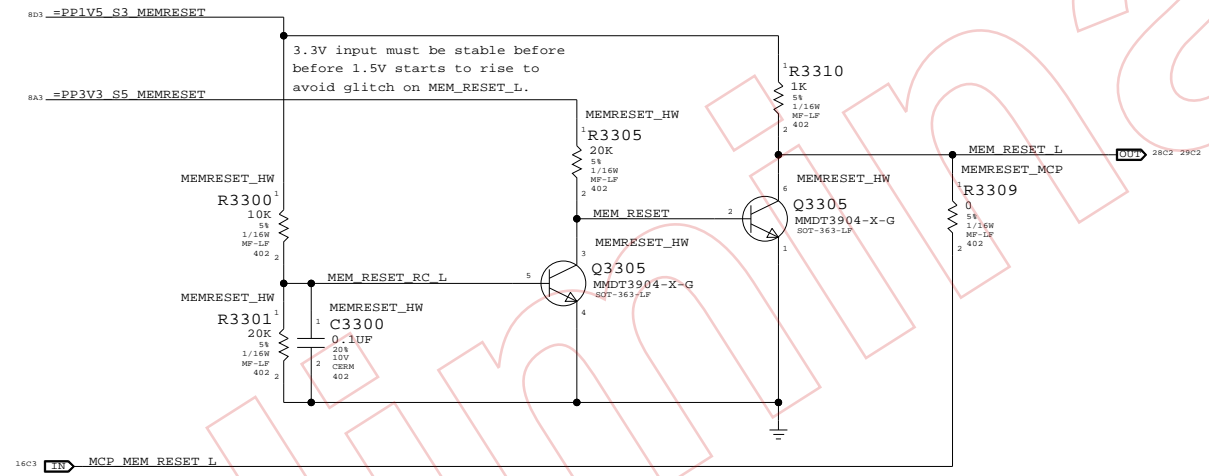


SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	32	109

516S0706
 SPD_ADDR=0xA2 (WR) / 0xA3 (RD)

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



Pre-release

DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

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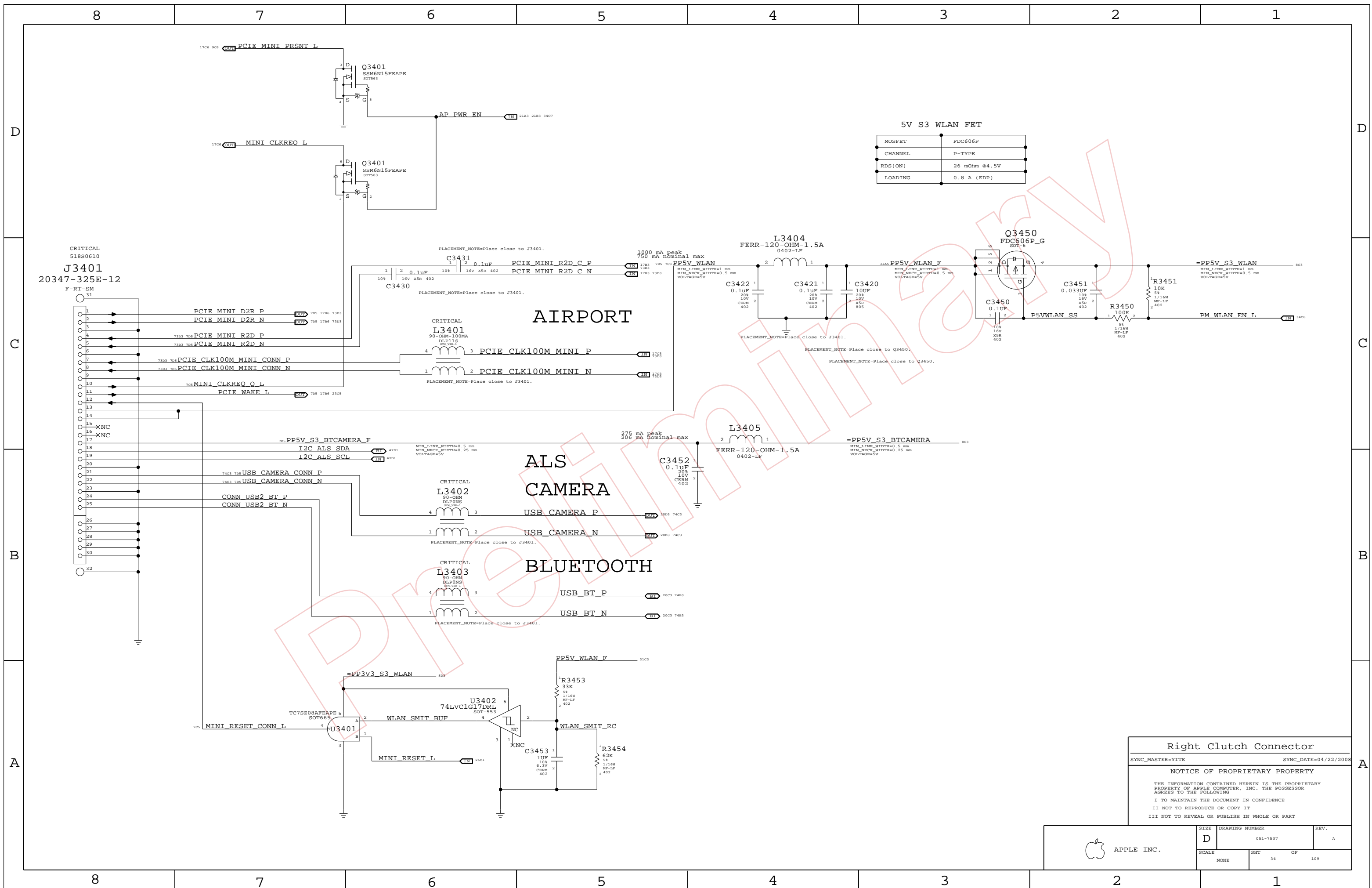
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	33		



5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS (ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

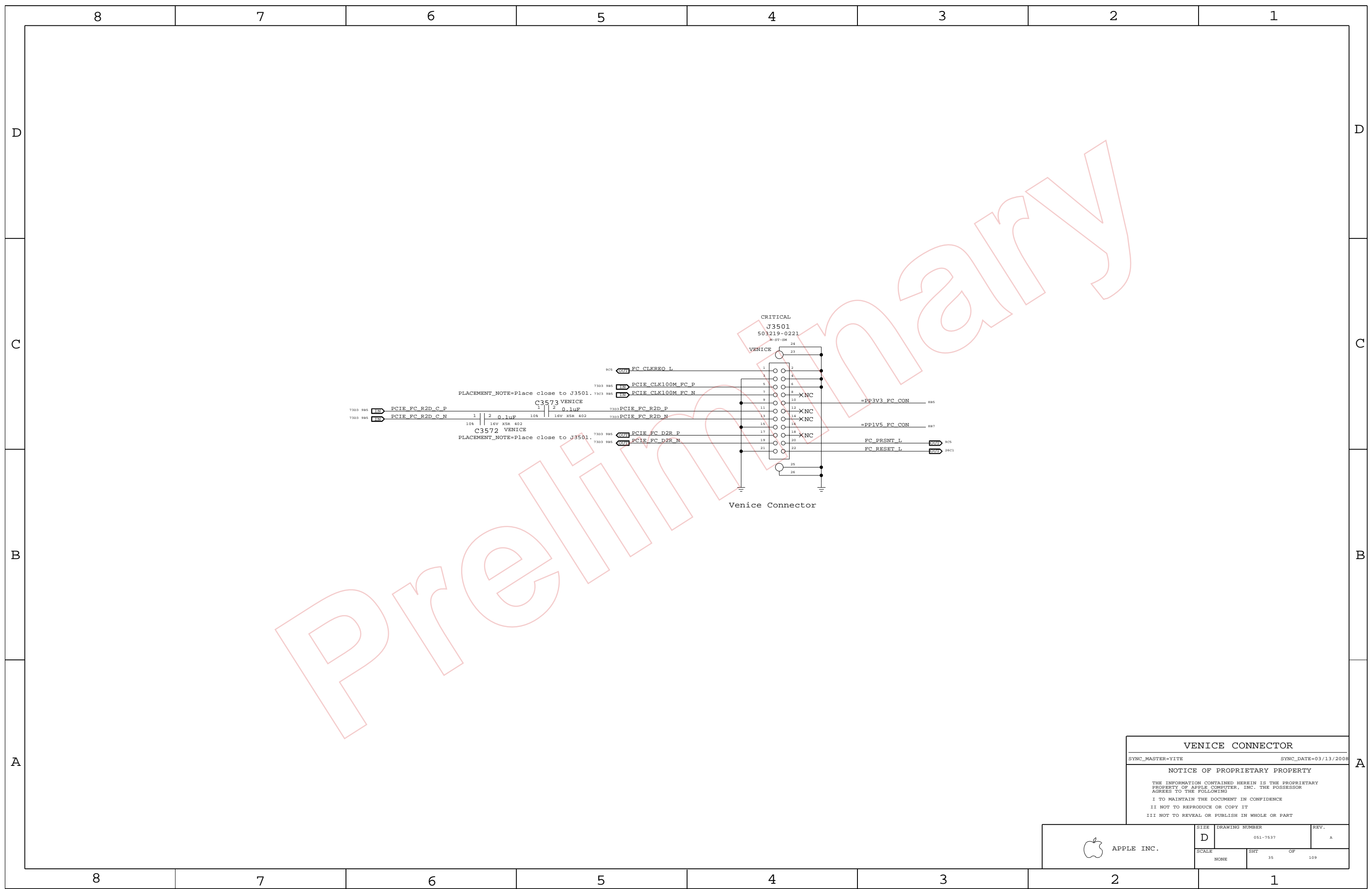
AIRPORT

ALS CAMERA

BLUETOOTH

Right Clutch Connector
 SYNC_MASTER=YITE SYNC_DATE=04/22/2008
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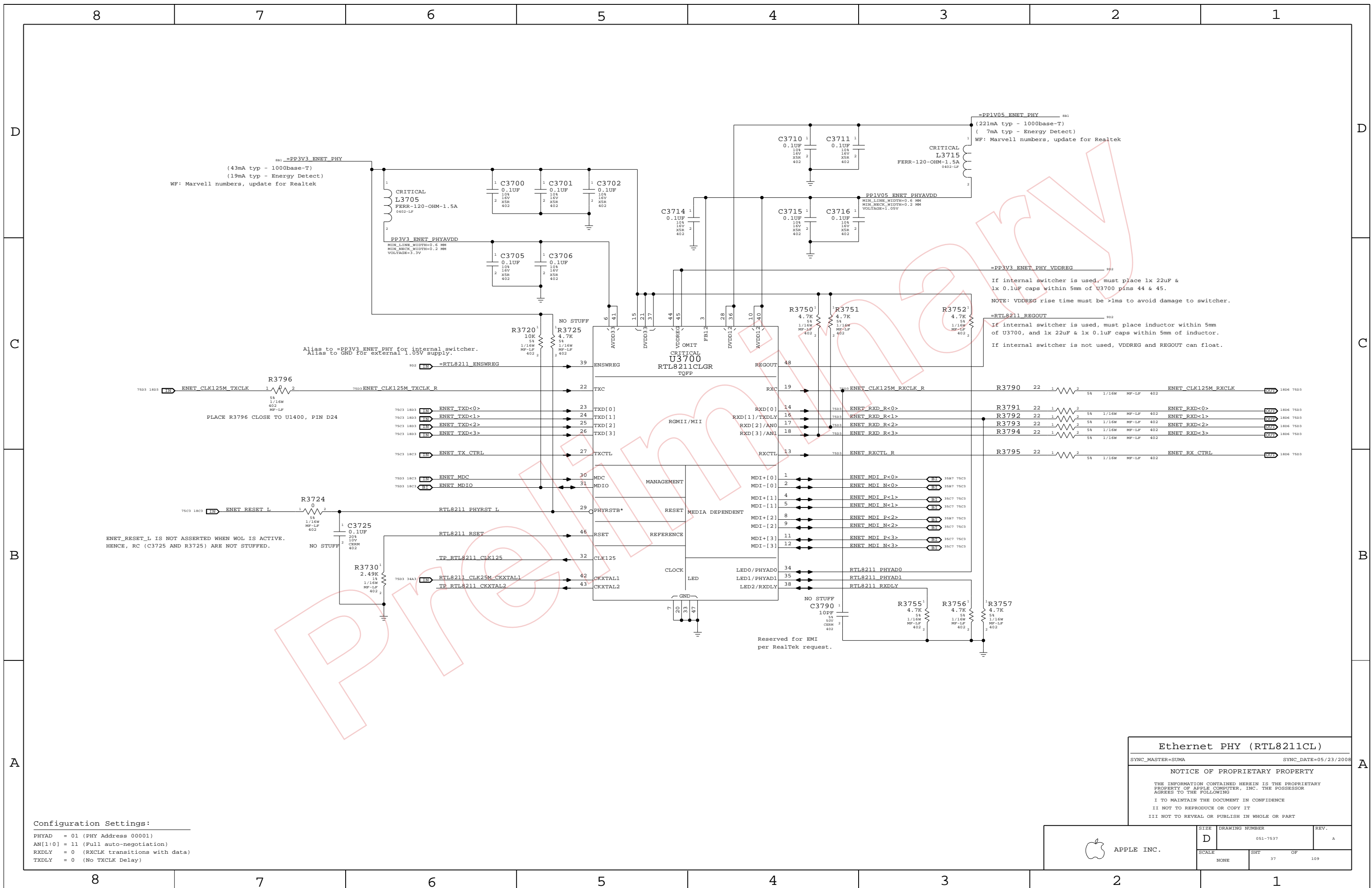
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	REV.
NONE	34	109	



Preliminary

VENICE CONNECTOR
 SYNC_MASTER=YITE SYNC_DATE=03/13/2008
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	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	
NONE	35	109	



881: =PP3V3_ENET_PHY
 (43mA typ - 1000base-T)
 (19mA typ - Energy Detect)
 WF: Marvell numbers, update for Realtek

Alias to =PP3V3_ENET_PHY for internal switcher.
 Alias to GND for external 1.05V supply.

PLACE R3796 CLOSE TO U1400, PIN D24

ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.
 HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.

If internal switcher is used, must place 1x 22uF &
 1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
 NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

If internal switcher is used, must place inductor within 5mm
 of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
 If internal switcher is not used, VDDREG and REGOUT can float.

Reserved for EMI
 per Realtek request.

Ethernet PHY (RTL8211CL)
 SYNC_MASTER=SUMA SYNC_DATE=05/23/2008
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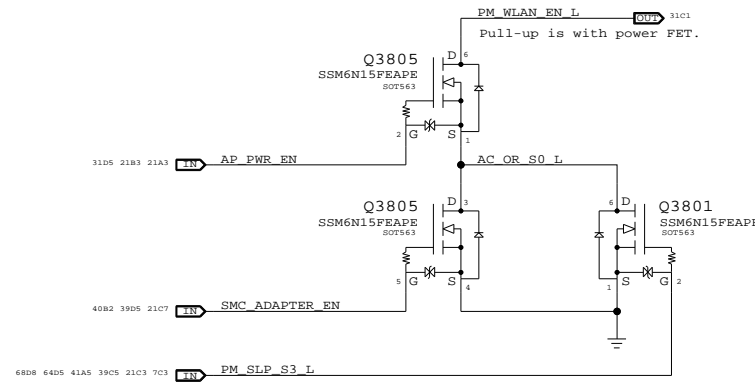
Configuration Settings:
 PHYAD = 01 (PHY Address 00001)
 AN[1:0] = 11 (Full auto-negotiation)
 RXDLY = 0 (RXCLK transitions with data)
 TXDLY = 0 (No TXCLK Delay)

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	37		

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

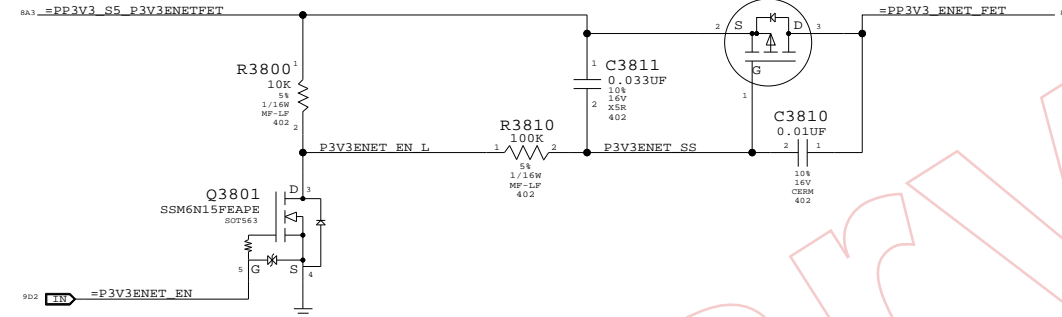
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

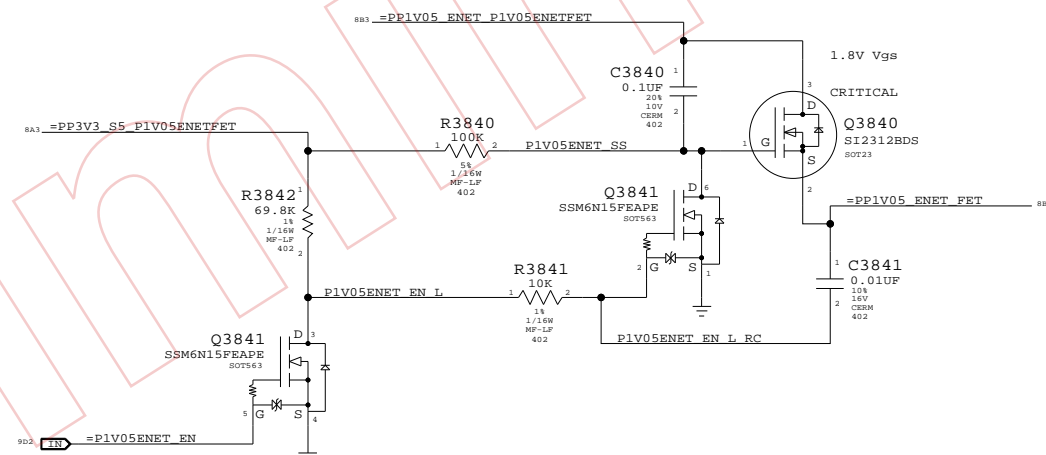
@ 2.5V Vgs:
 Rds(on) = 90mOhm max
 I(max) = 1.7A (85C)

CRITICAL
 Q3810
 NTR4101P
 SOT-23-NP



MOBILE:
 Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

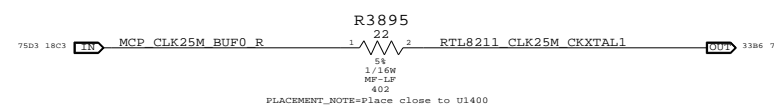
1.05V ENET FET



Non-ARB:
 Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
 Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

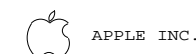


Ethernet & AirPort Support

SYNC_MASTER=SUMA SYNC_DATE=07/01/2008

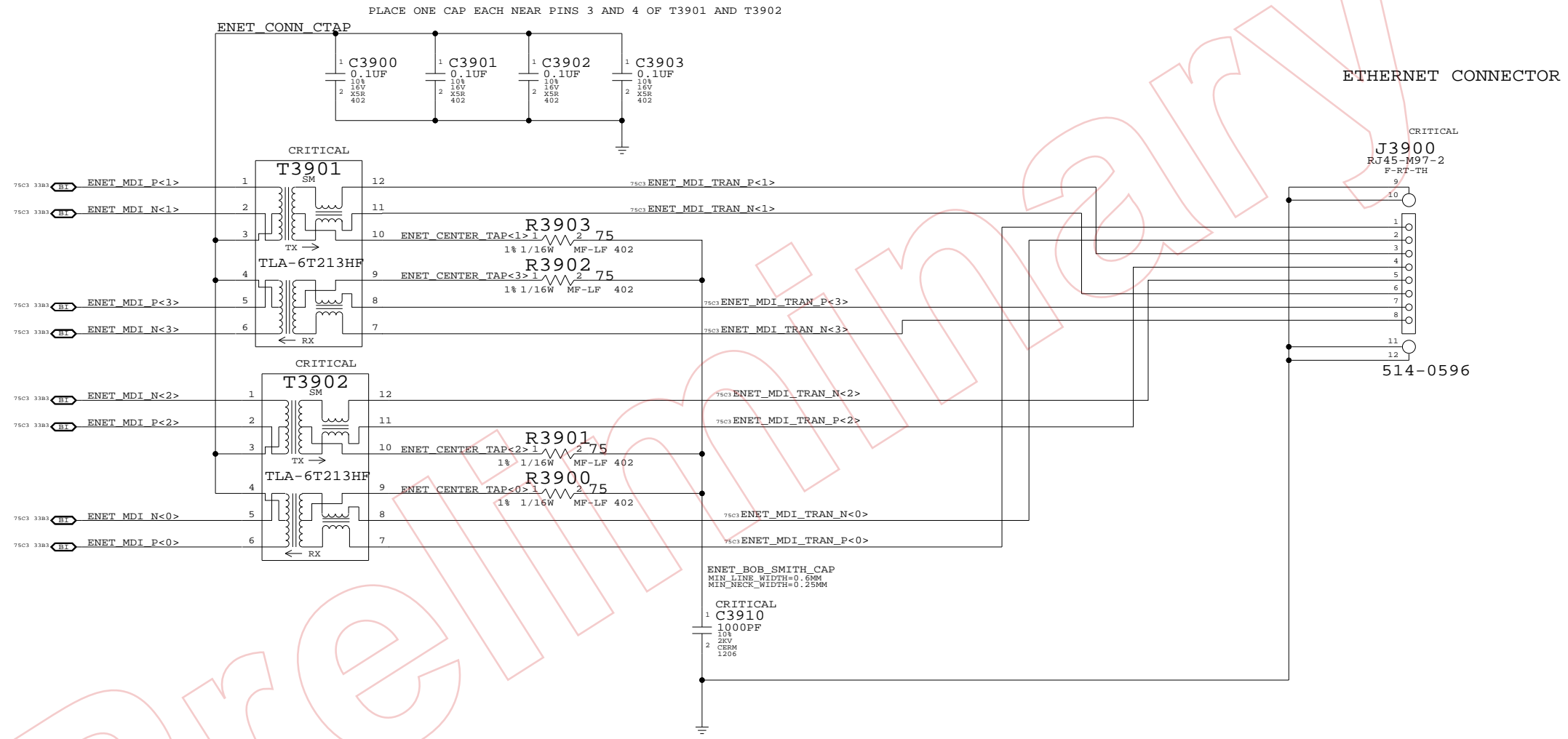
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	38	109



ETHERNET CONNECTOR

SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

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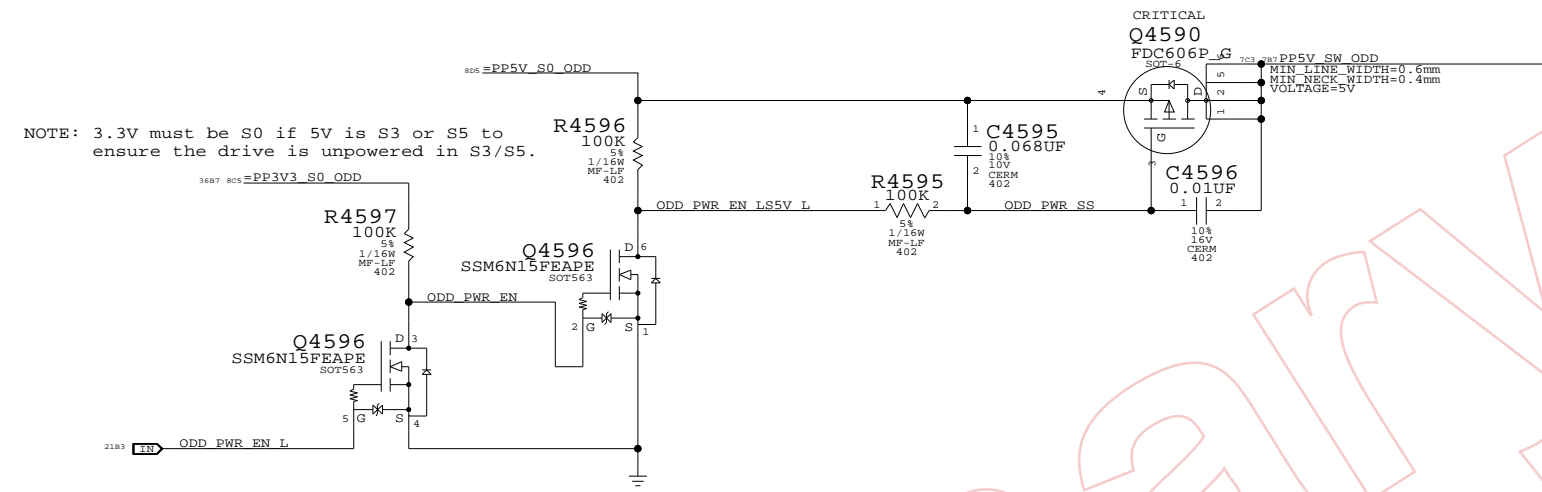
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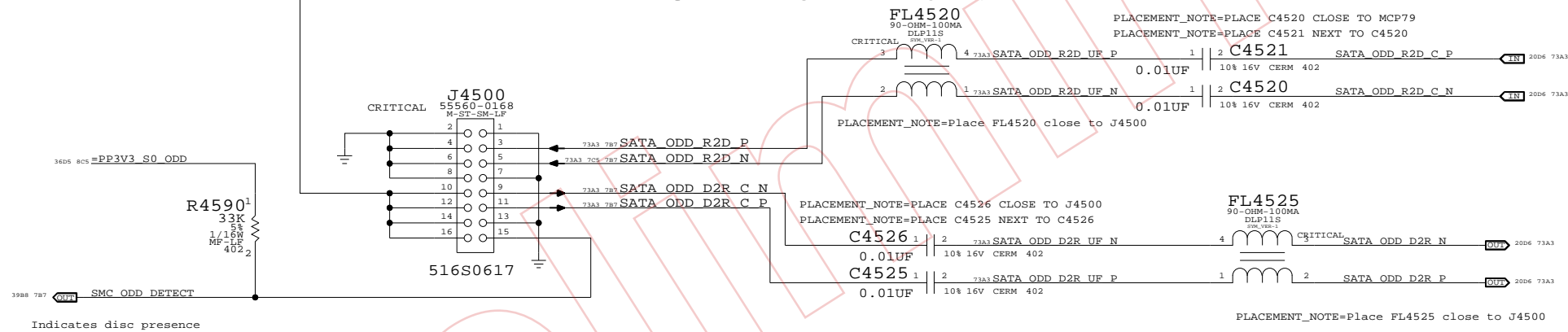
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT		OF
NONE	39		109

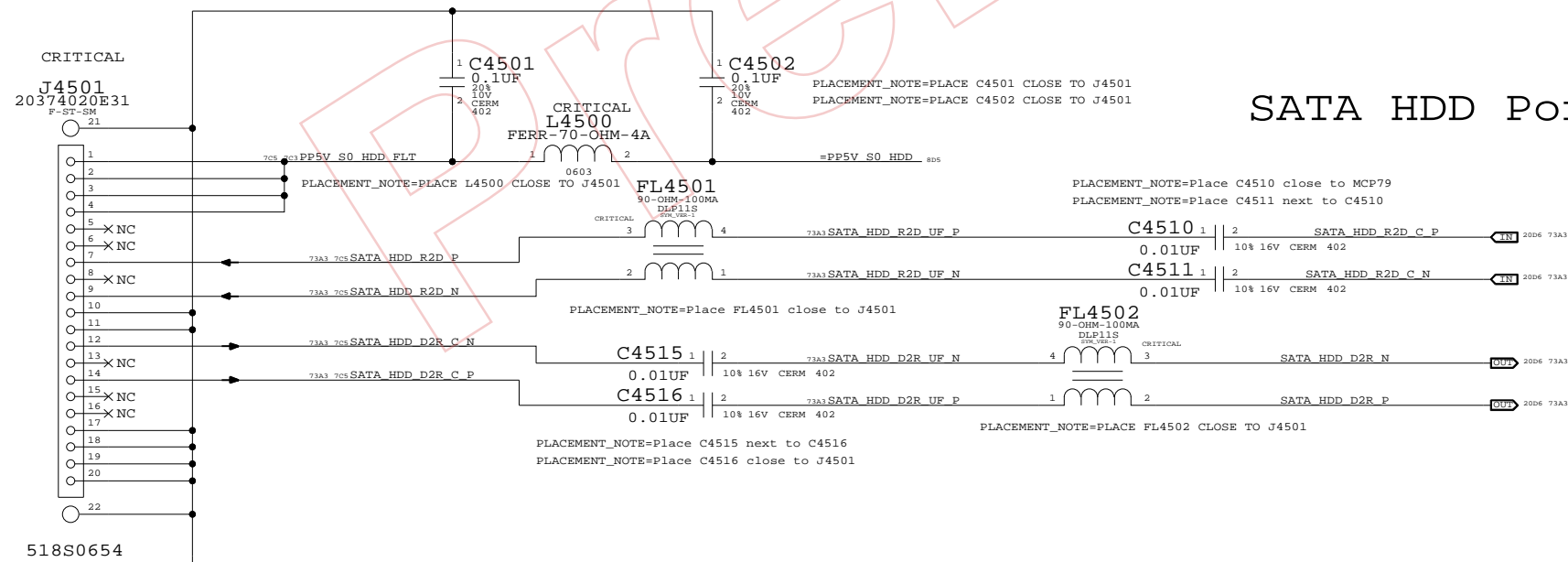
ODD Power Control



SATA ODD Port

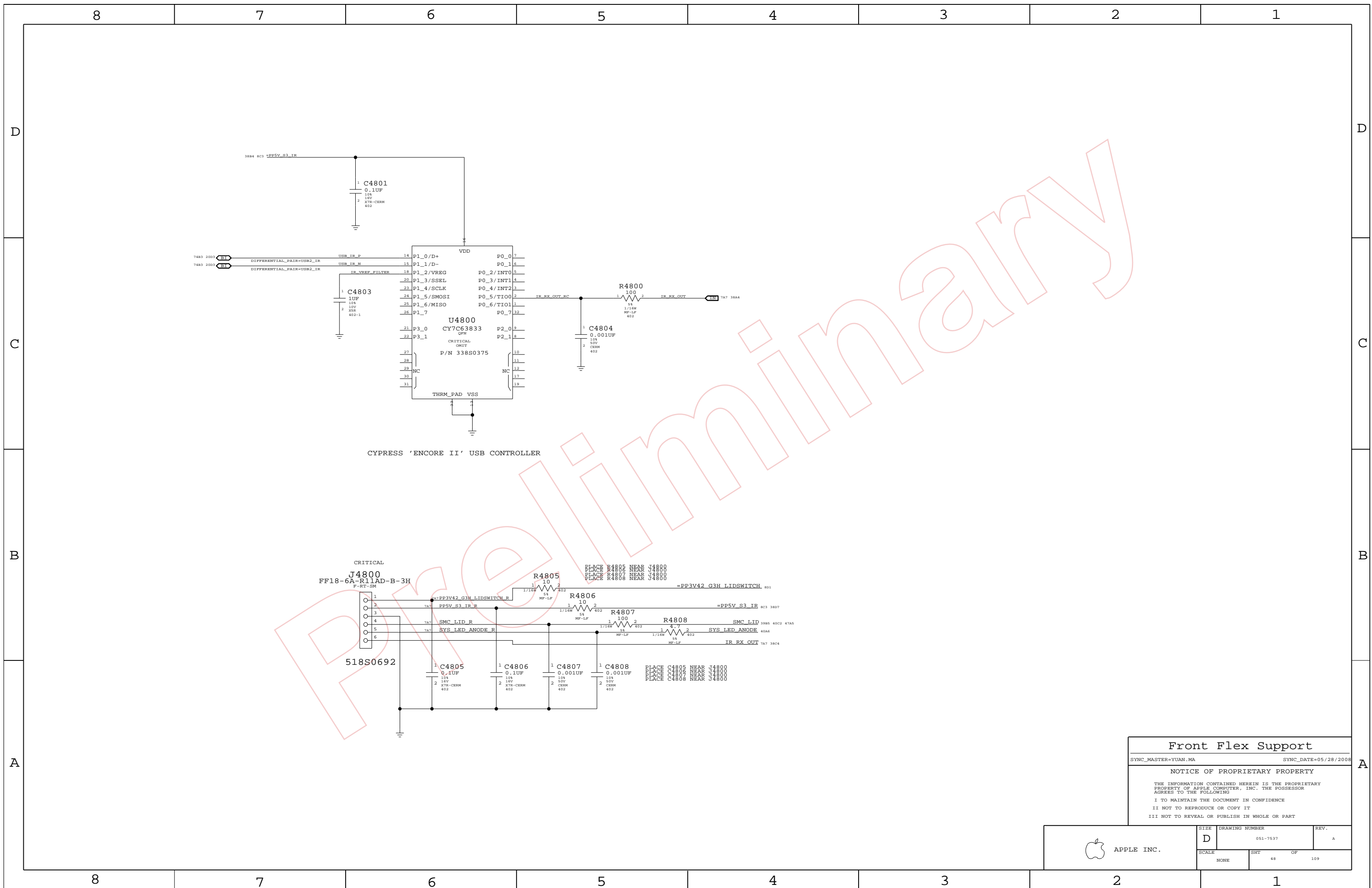


SATA HDD Port

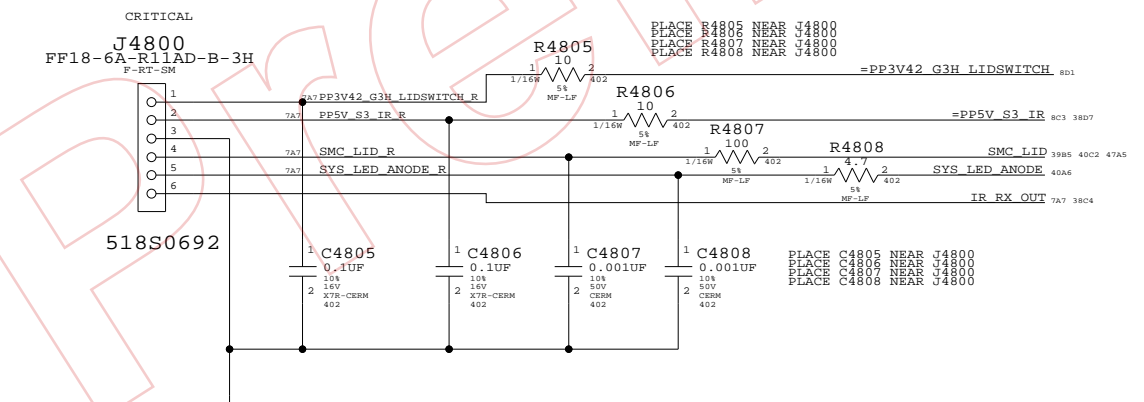


SATA Connectors
 SYNC_MASTER=CHANGZHANG SYNC_DATE=04/14/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	45		



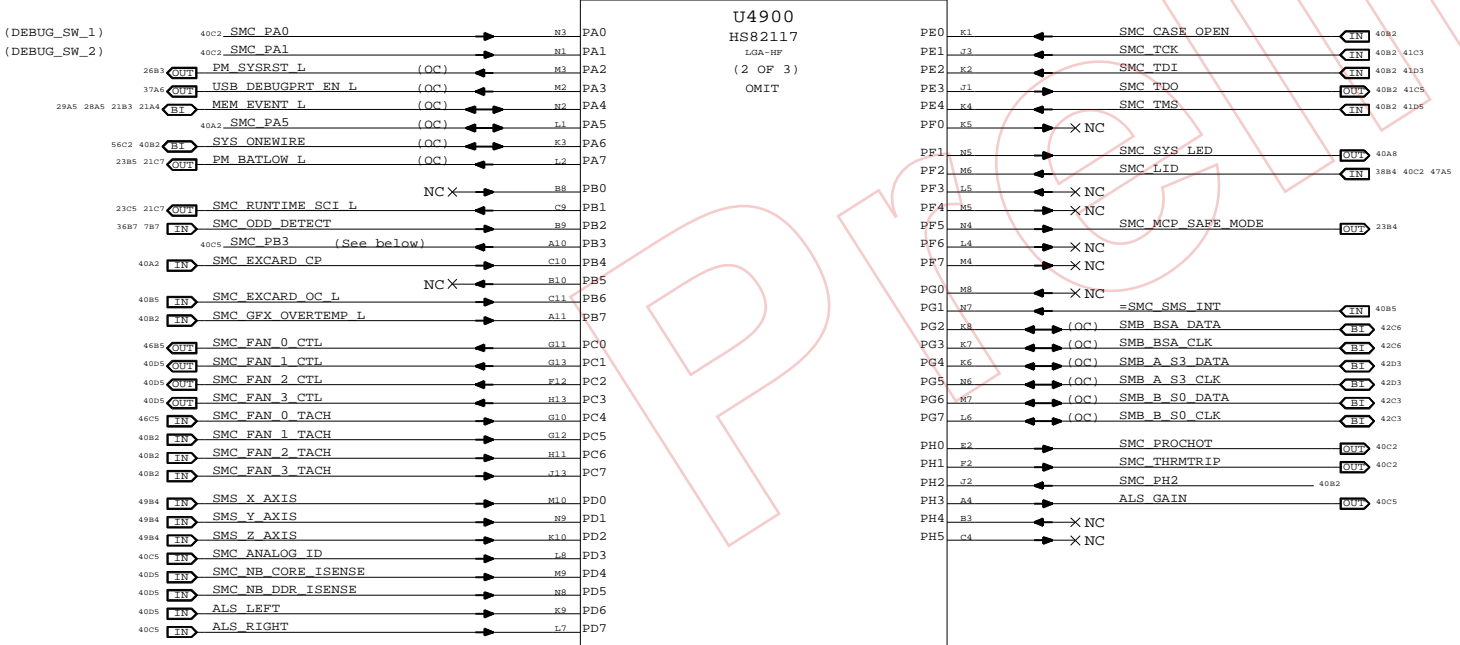
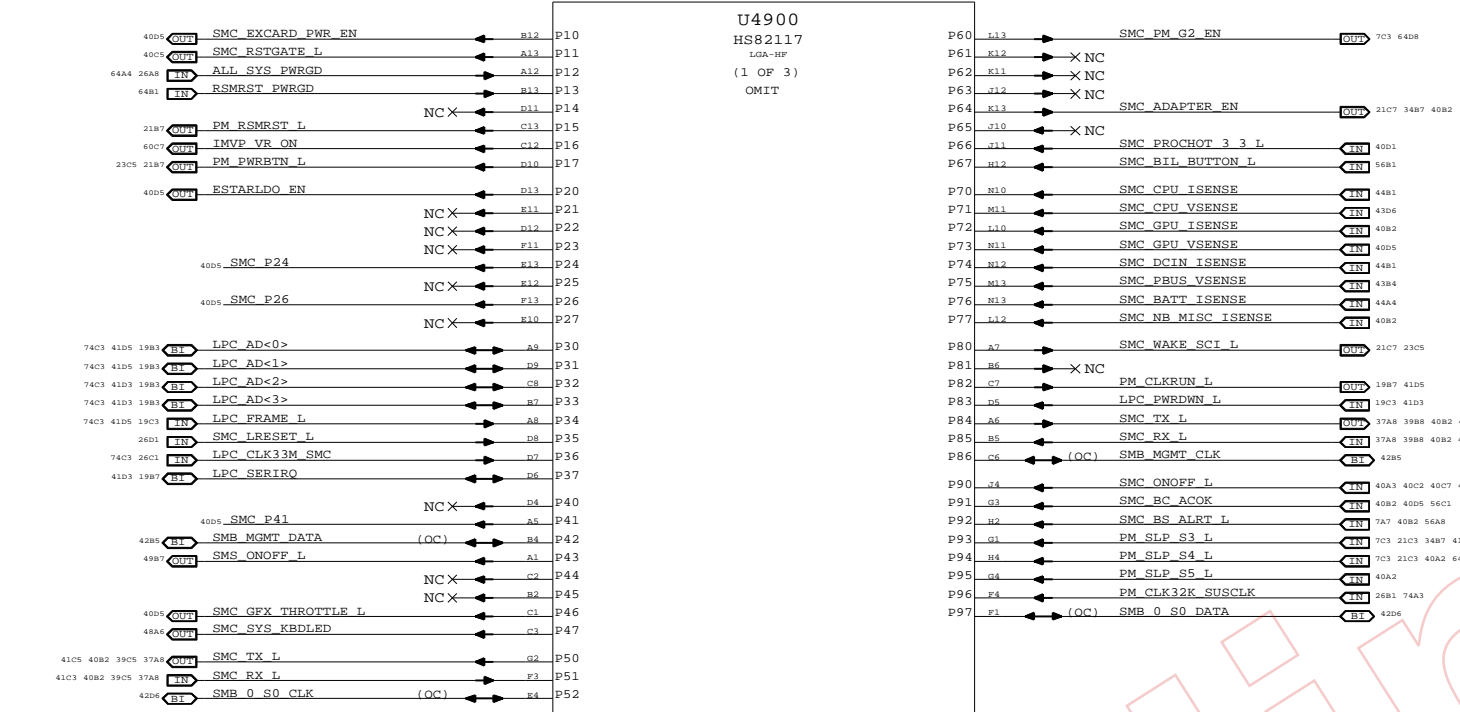
CYPRESS 'ENCORE II' USB CONTROLLER



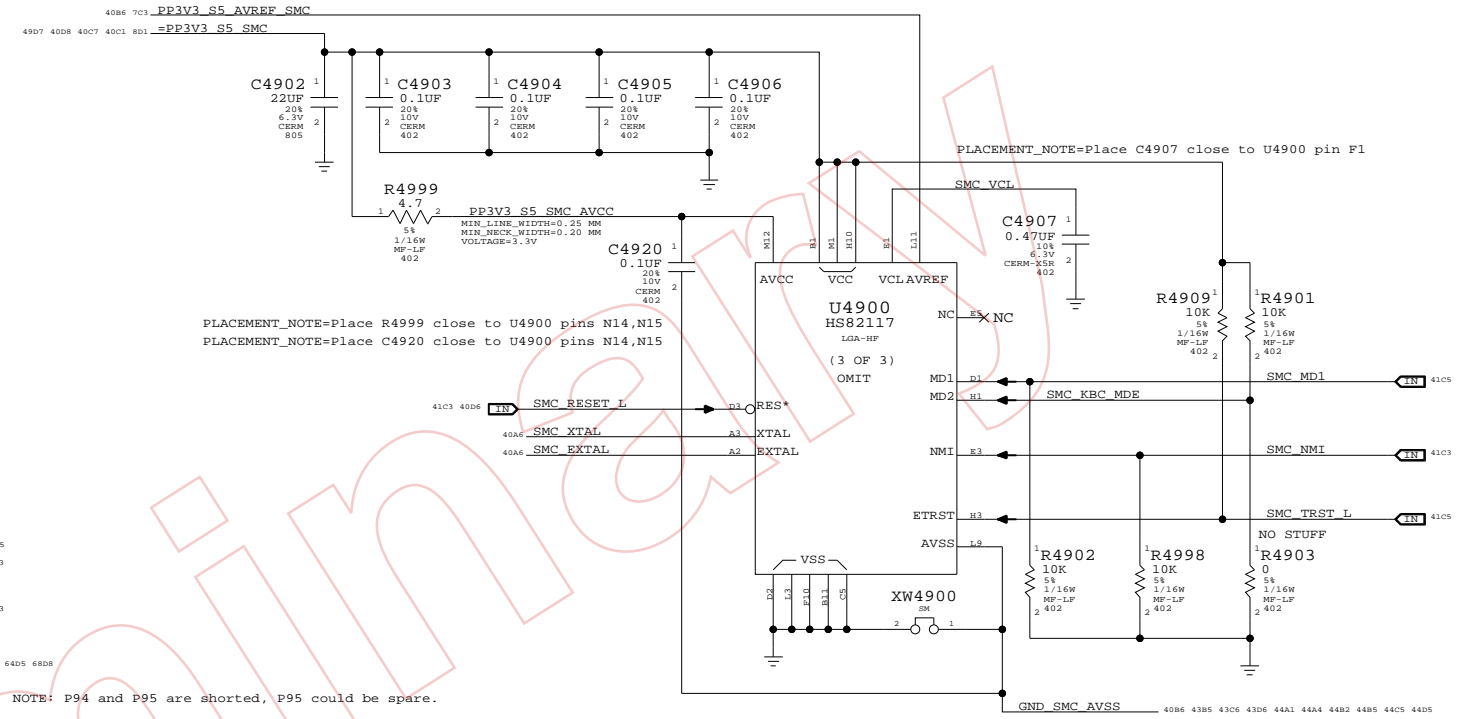
Front Flex Support
 SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	REV.
NONE	48	109	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



SMC

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

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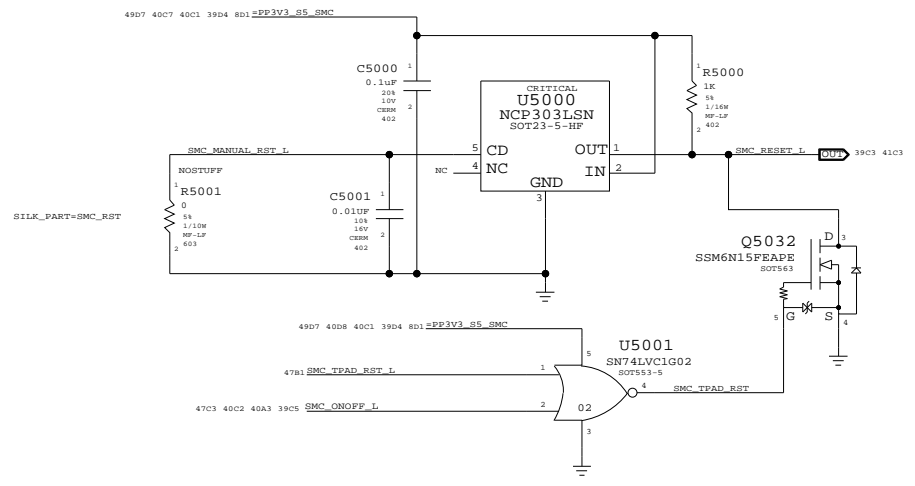
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

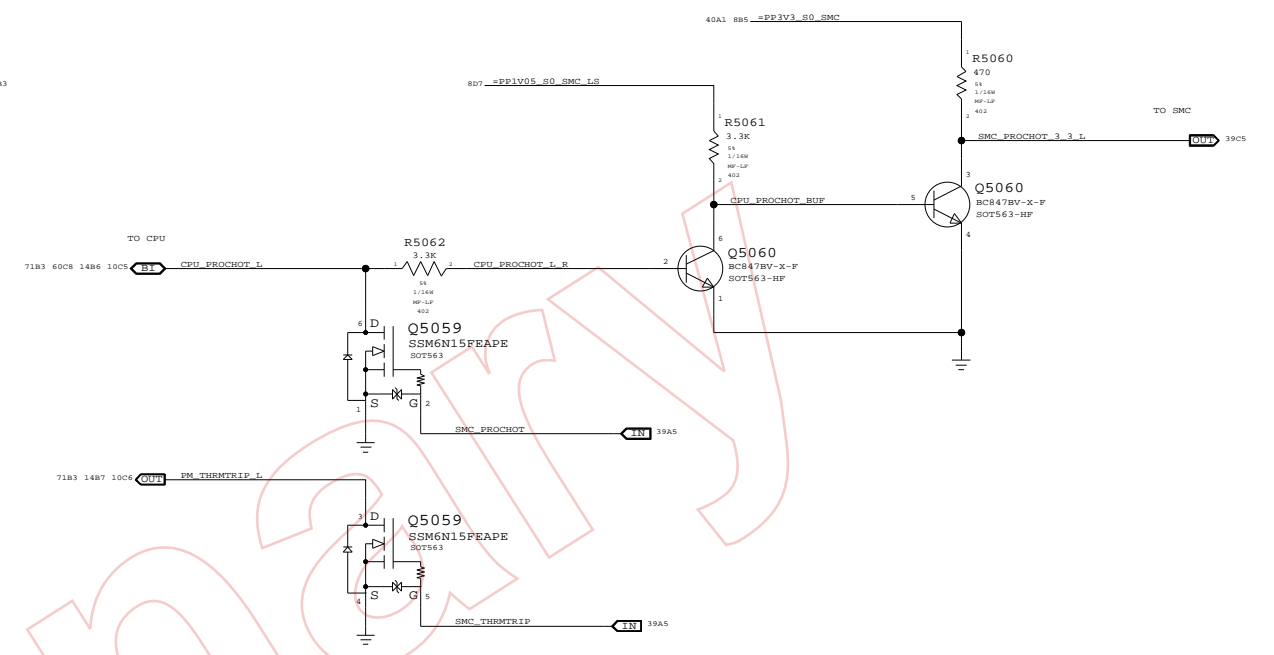
APPLE INC.		SCALE	DRAWING NUMBER	REV.
NONE		D	051-7537	A
		SHT	OF	
		49	109	

SMC Reset "Button" / Brownout Detect

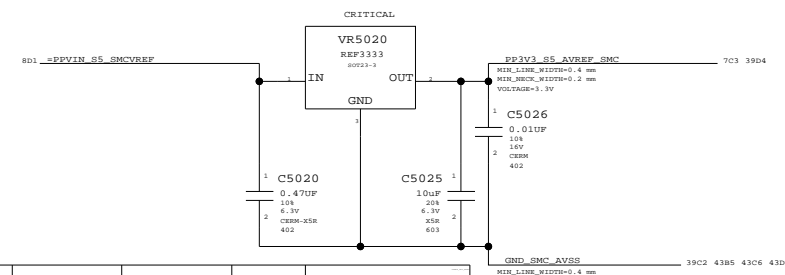


39A8	SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE	
39A8	SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	
39A8	SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
39B8	SMC_GPU_THROTTLE_L	SMC_IG_THROTTLE_L	MAKE_BASE=TRUE	21A4 21B3
39C8	ESTARLDO_EN	NC_ESTARLDO_EN	MAKE_BASE=TRUE	
56C1 40B2 39C5	SMC_BC_ACOK	=CHGR_ACOK	MAKE_BASE=TRUE	57B5
39C8	SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
39C8	SMC_P26	SMC_RMON_MUX_SEL	MAKE_BASE=TRUE	44A5
39C8	SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
39A8	SMC_NB_CORE_ISENSE	SMC_MCP_CORE_ISENSE	MAKE_BASE=TRUE	44D5
39A8	SMC_NB_DDR_ISENSE	SMC_MCP_DDR_ISENSE	MAKE_BASE=TRUE	44C5
39A8	ALS_LEFT	SMC_CPU_FSB_ISENSE	MAKE_BASE=TRUE	44B5
39C5	SMC_GPU_VSENSE	SMC_MCP_VSENSE	MAKE_BASE=TRUE	43D6
39D8	SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
39D8	SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
39B8	SMC_PB3	NC_SMC_PB3	MAKE_BASE=TRUE	
39A5	ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	
39A8	SMC_ANALOG_ID	NC_SMC_ANALOG_ID	MAKE_BASE=TRUE	
39A8	ALS_RIGHT	NC_ALS_RIGHT	MAKE_BASE=TRUE	

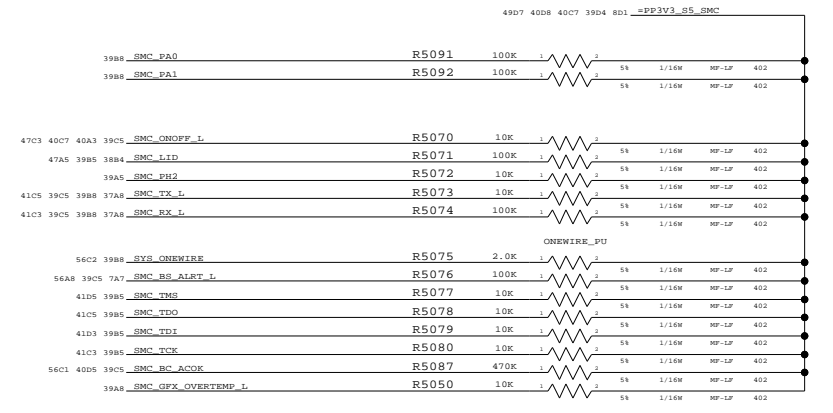
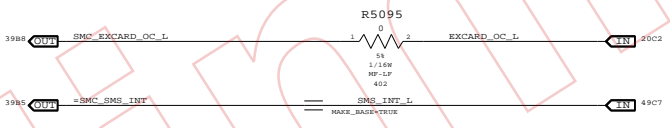
SMC FSB to 3.3V Level Shifting



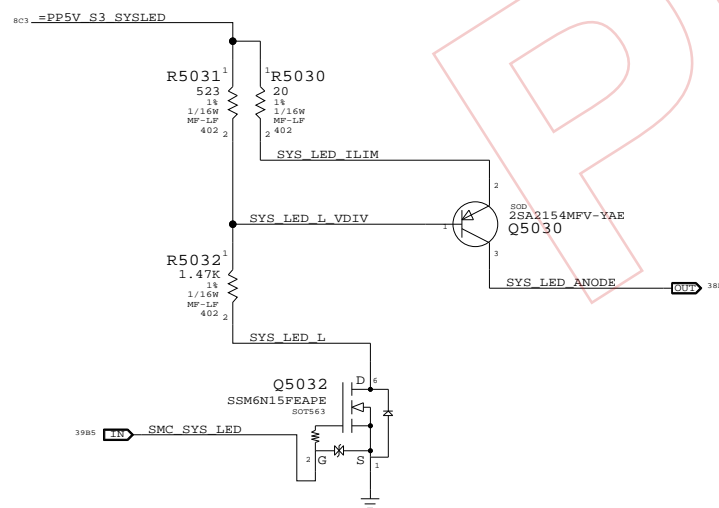
SMC AVREF Supply



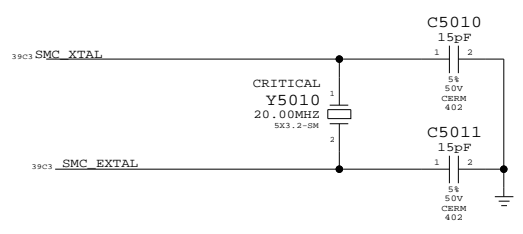
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interim ISL60002-33



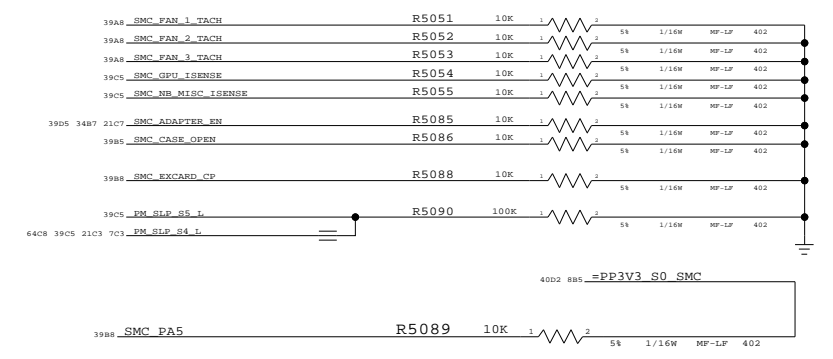
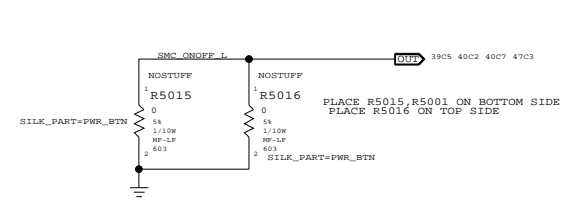
System (Sleep) LED Circuit



SMC Crystal Circuit



Debug Power "Button"

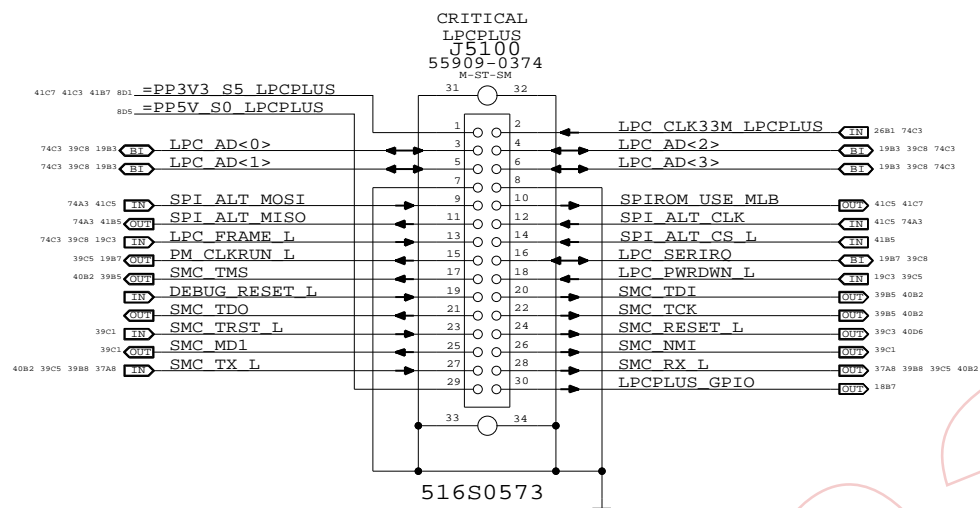


SMC Support
 SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

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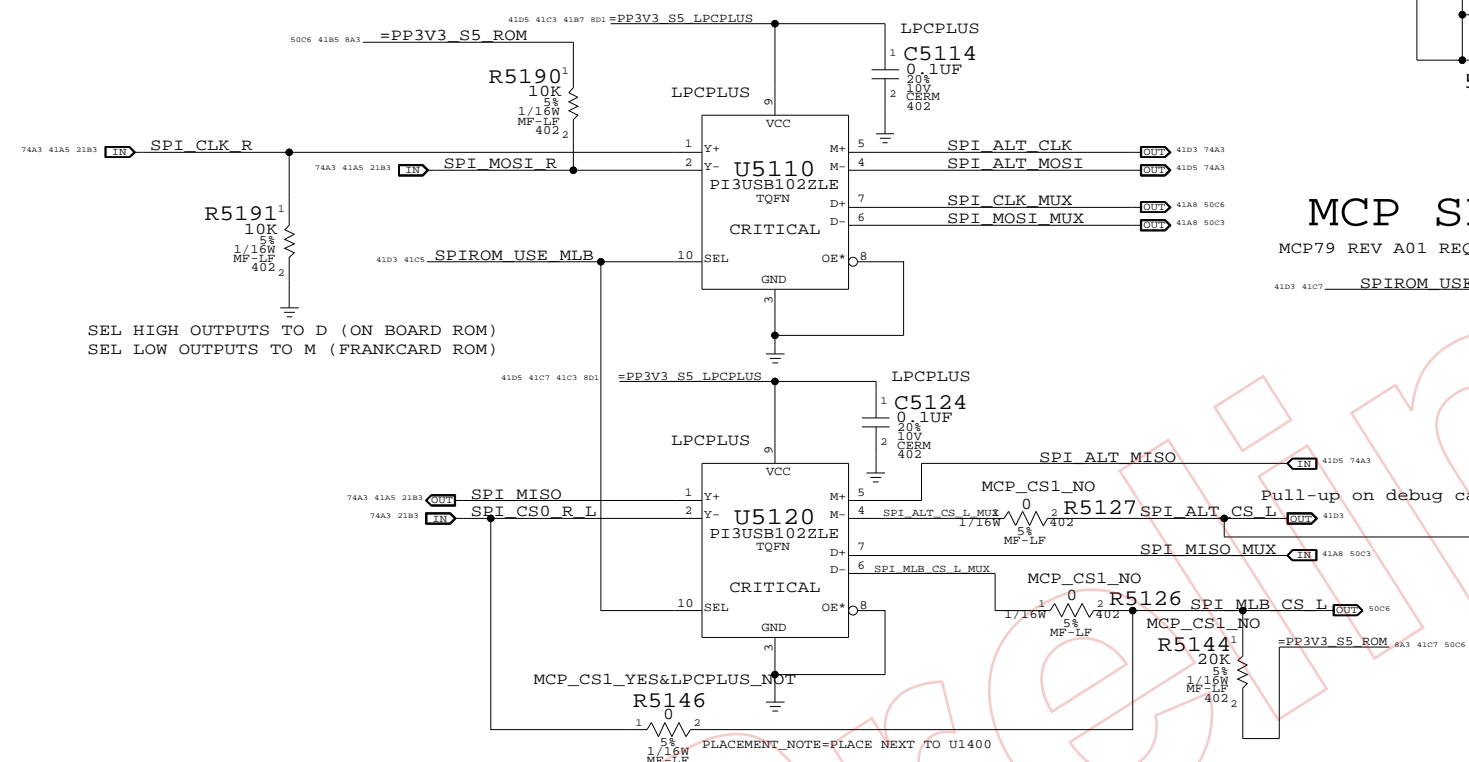
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	NONE	SHT	50 OF 109

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

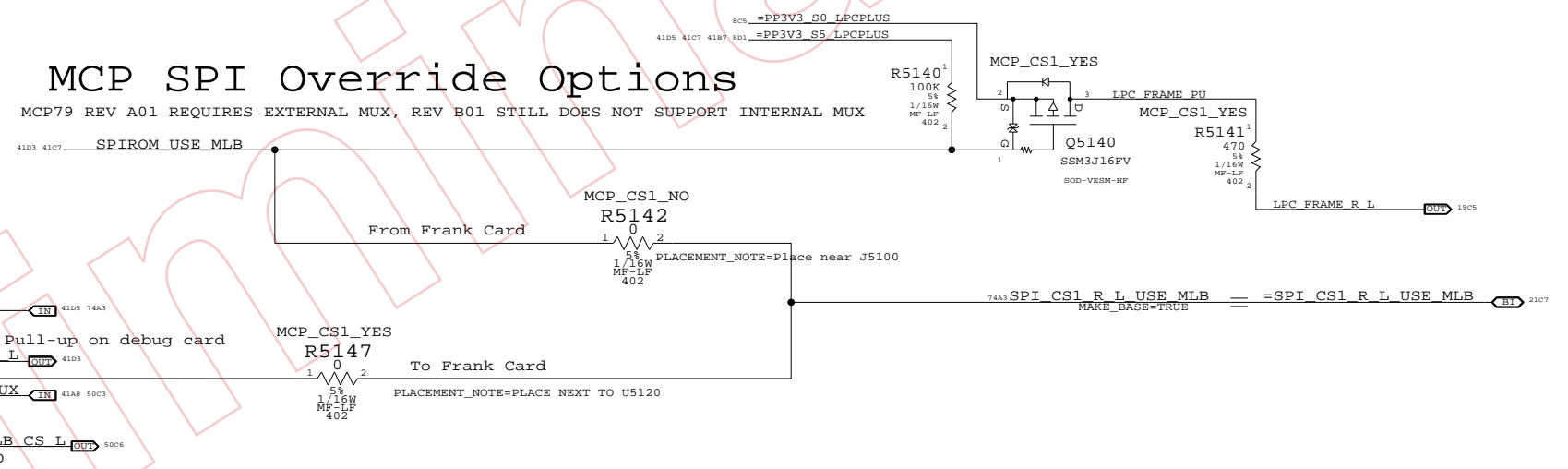


MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

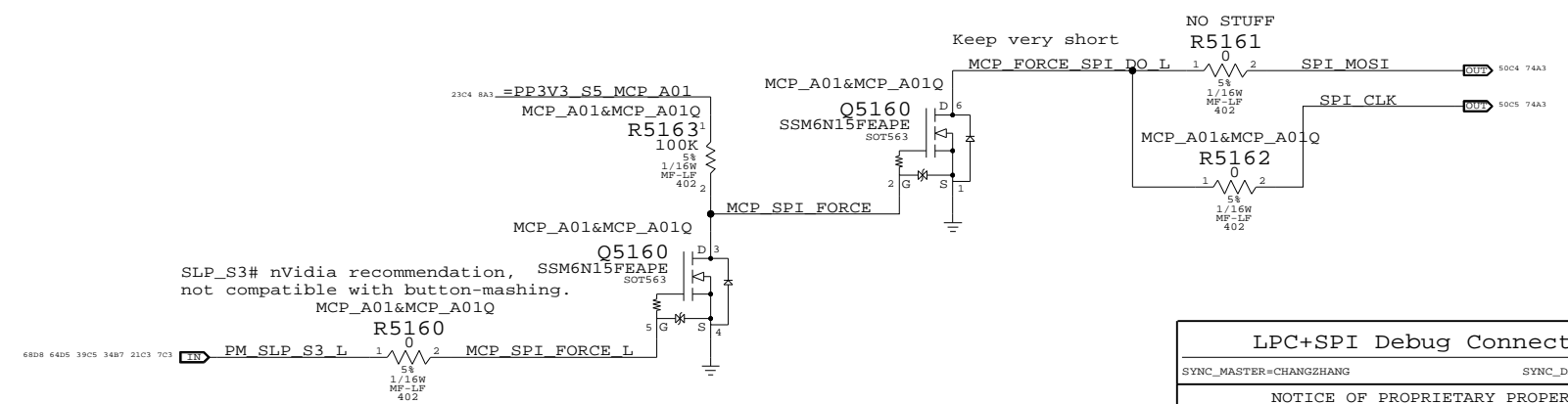
MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

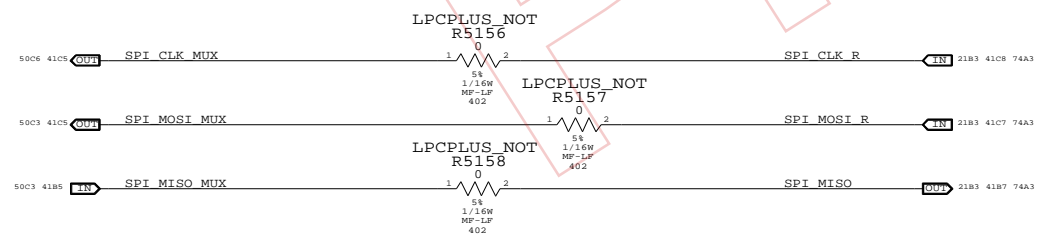


SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED. NOT NEEDED FOR B01 OR LATER.



SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

NOTICE OF PROPRIETARY PROPERTY

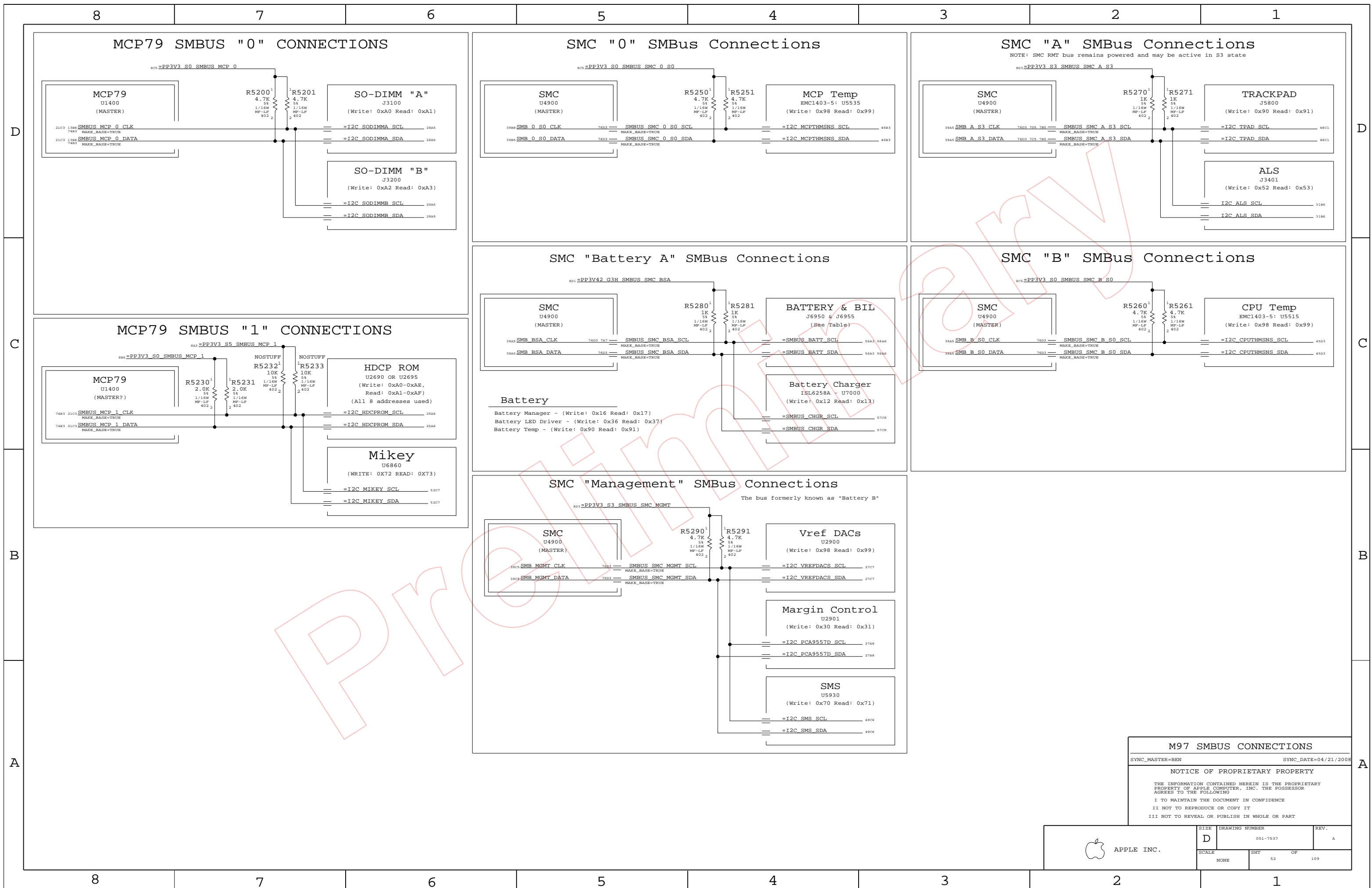
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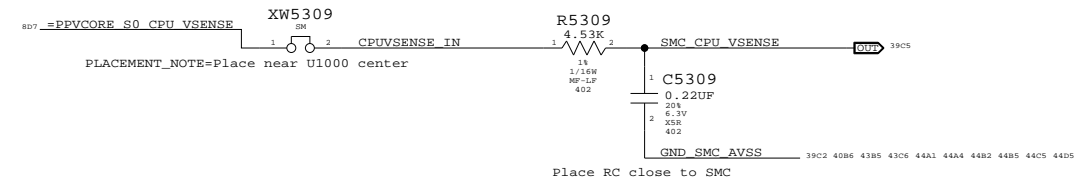
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	51		



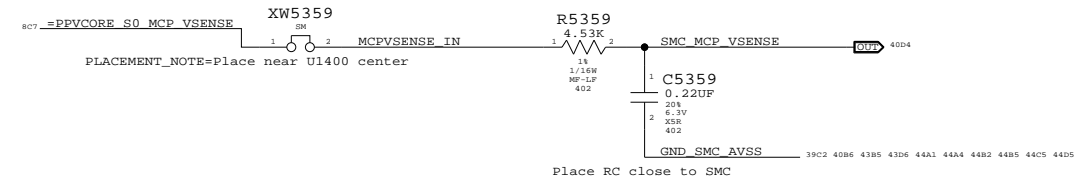
M97 SMBUS CONNECTIONS
 SYNC_MASTER=BEN SYNC_DATE=04/21/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	52		

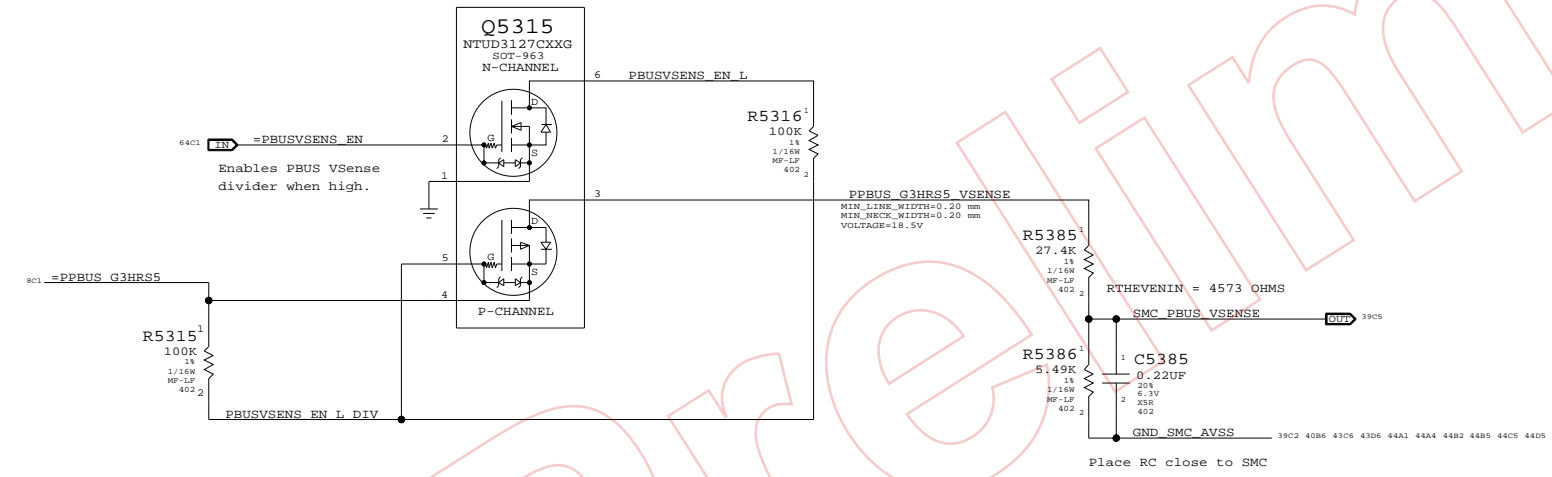
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



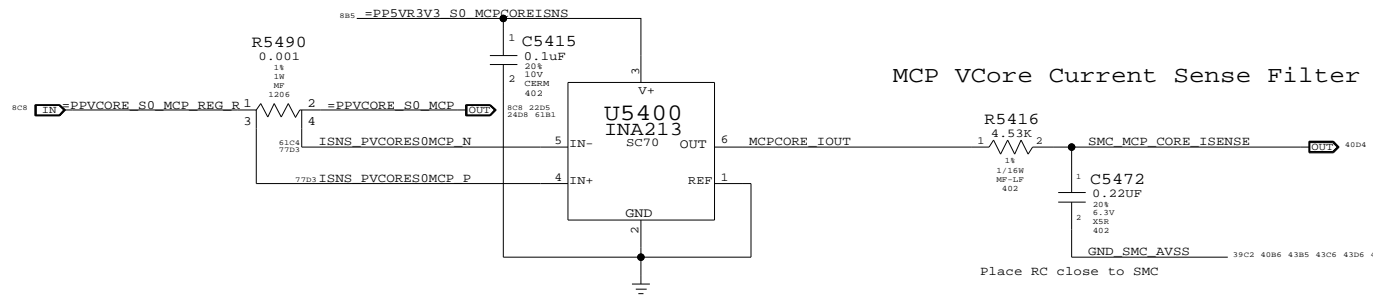
PBUS VOLTAGE SENSE ENABLE & FILTER



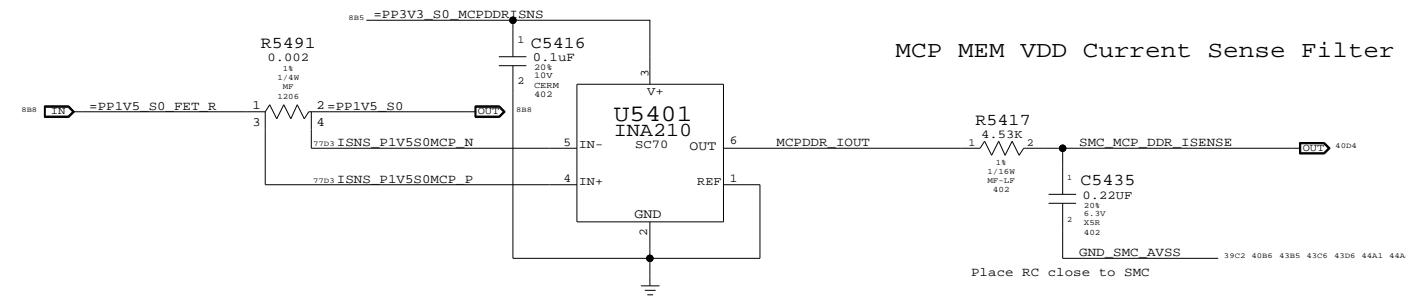
VOLTAGE SENSING
 SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	53		

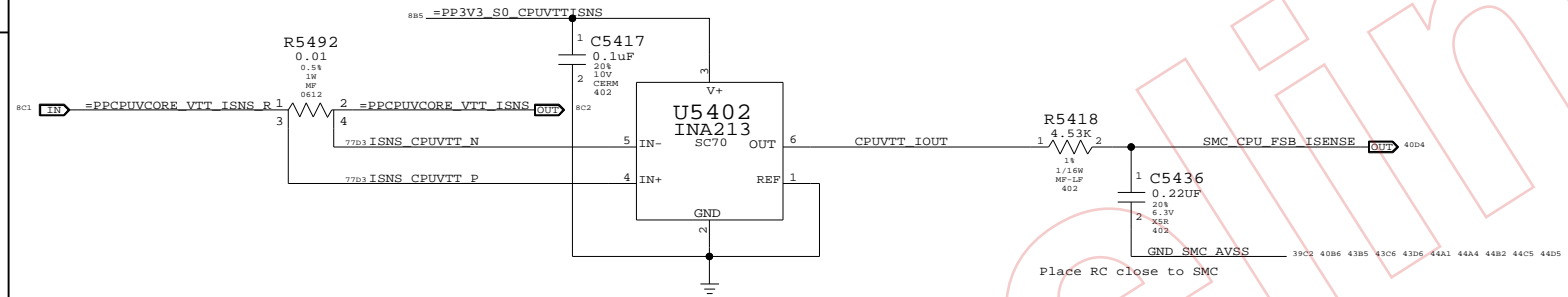
MCP VCore Current Sense



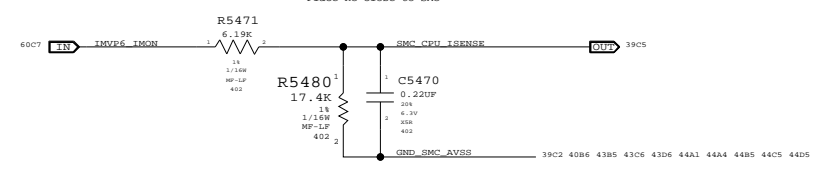
MCP MEM VDD Current Sense



CPU 1.05V AND CPU VCore HIGH SIDE CURRENT SENSE

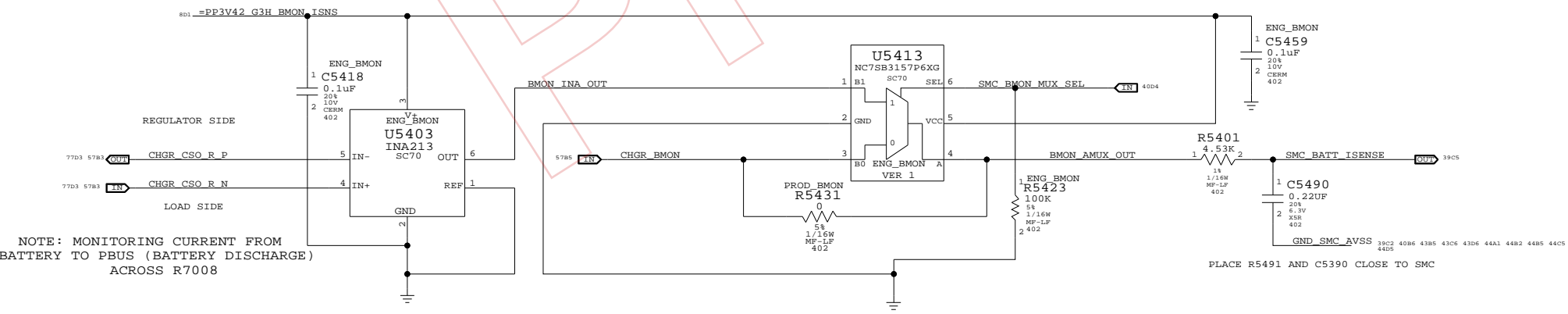


CPU VCore Load Side Current Sense / Filter

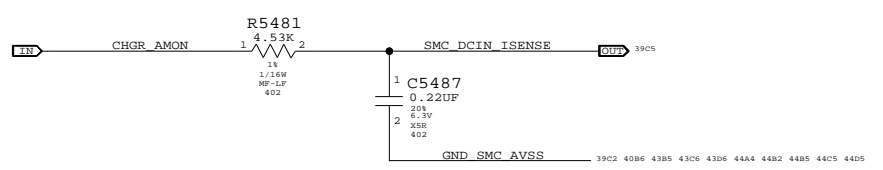


BMON CURRENT SENSE

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)



DC-IN (AMON) CURRENT SENSE



Current Sensing		
SYNC_MASTER=YUNWU	SYNC_DATE=04/07/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	54		

8

7

6

5

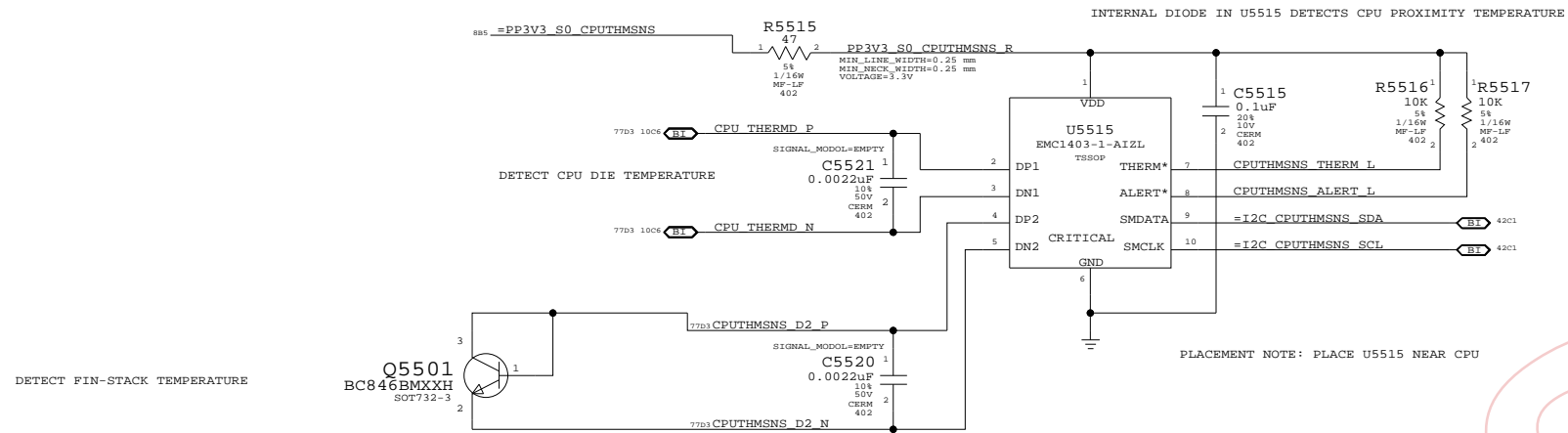
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3

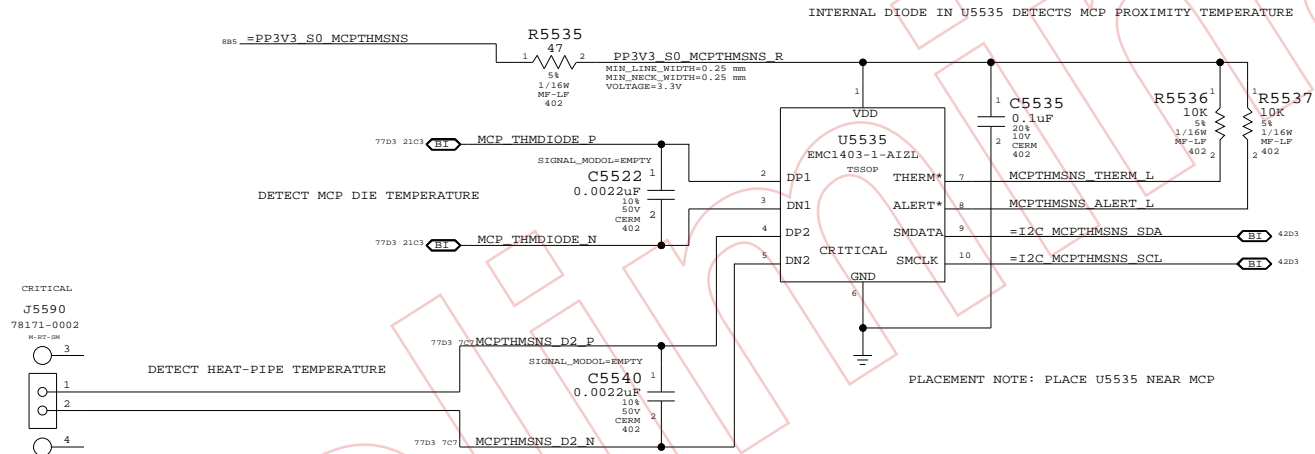
2

1

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

Thermal Sensors

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

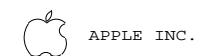
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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	55	109

8

7

6

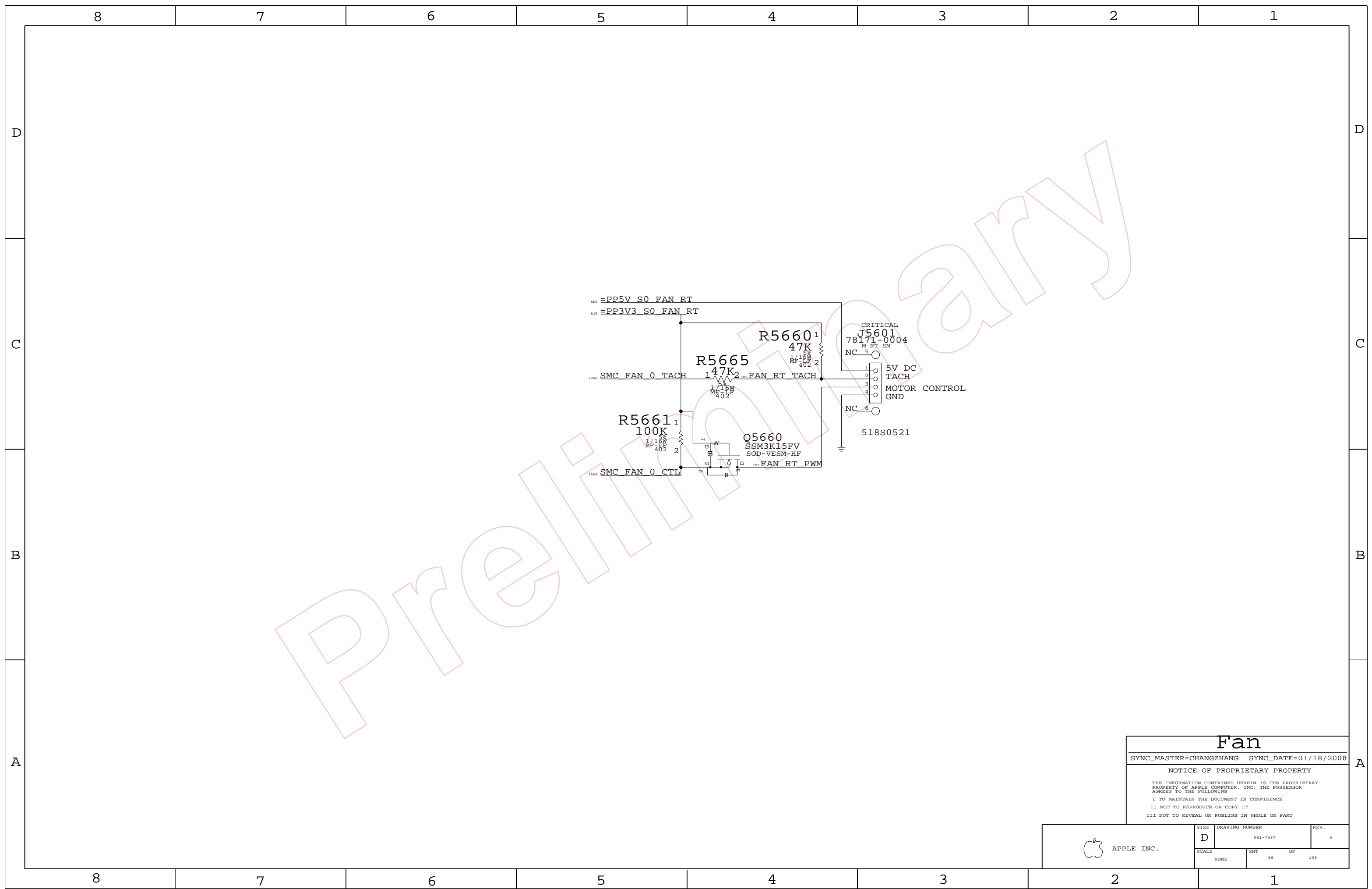
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4

3

2

1



Preliminary

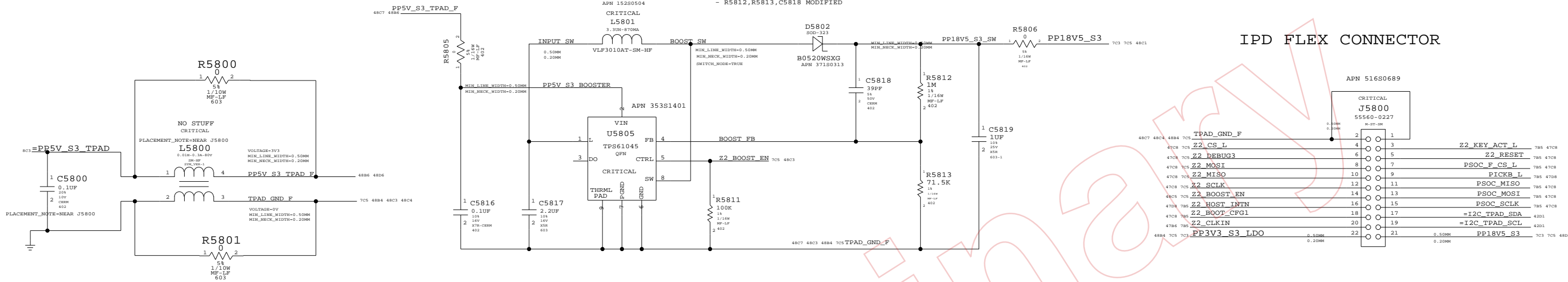
Fan

SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008
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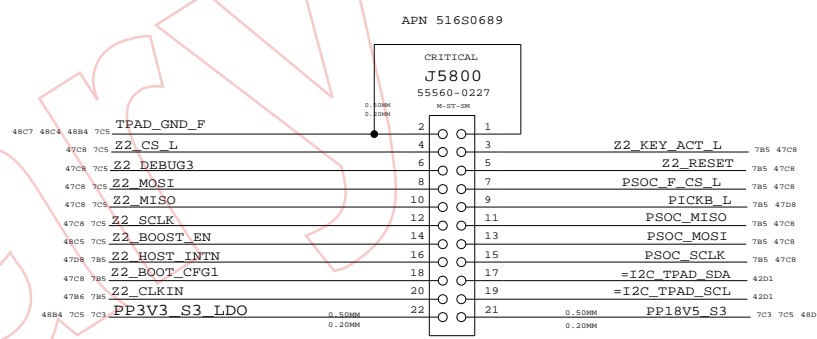
APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHIT 56	OF 109

BOOSTER +18.5VDC FOR SENSORS

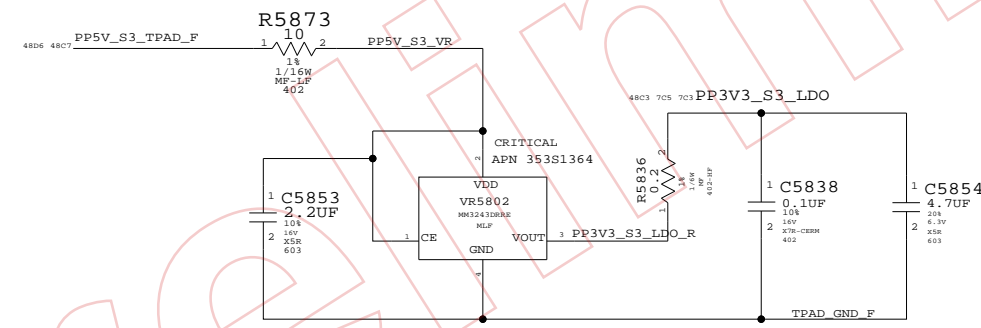
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812, R5813, C5818 MODIFIED



IPD FLEX CONNECTOR

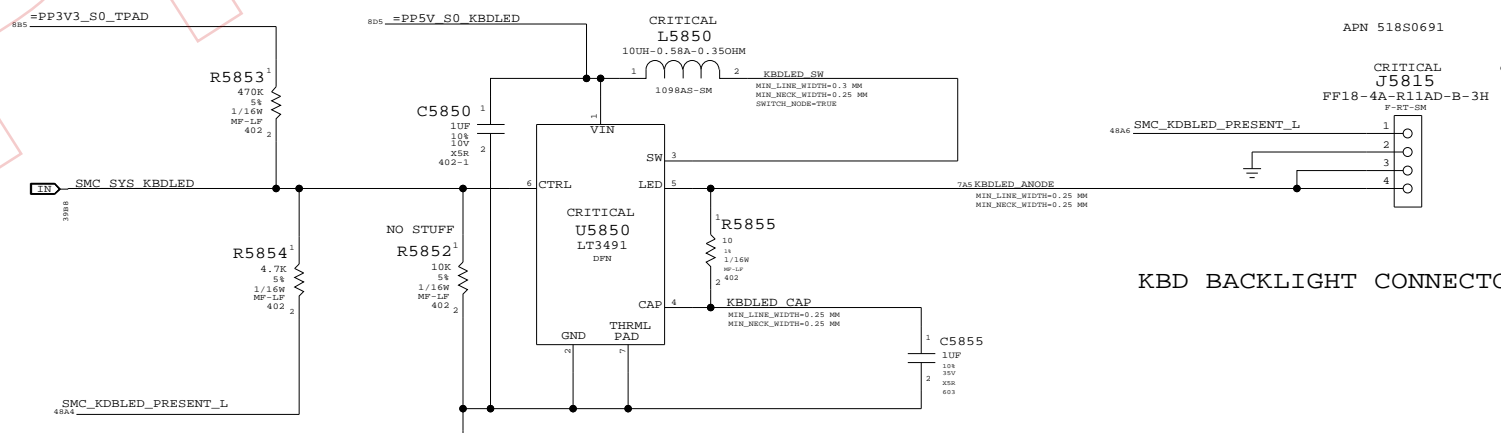


3V3 LDO FOR IPD

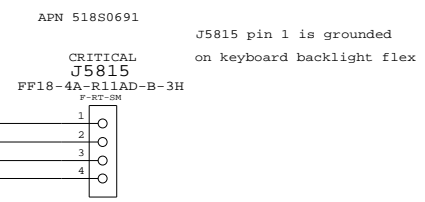


KEYBOARD BACKLIGHT DRIVING AND DETECTION

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
 LOW = keyboard backlight present
 HIGH = keyboard backlight not present
 BOM OPTION: KBDLED_YES
 TURNED ON FOR BEST MLB CONFIG
 R5853 ALWAYS PRESENT



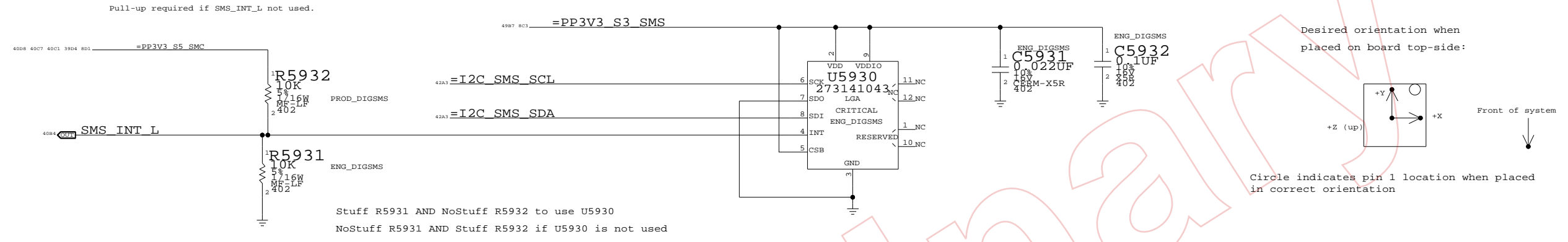
KBD BACKLIGHT CONNECTOR



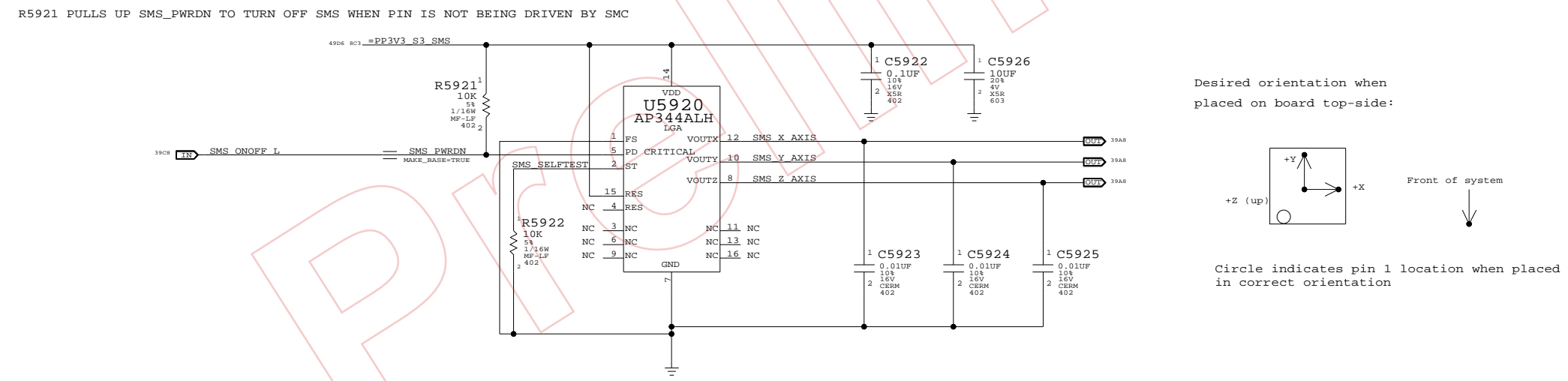
WELLSPRING 2
 SYNC_MASTER=YUAN.MA SYNC_DATE=05/09/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	58		

Digital SMS



Analog SMS



SMS

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

NOTICE OF PROPRIETARY PROPERTY

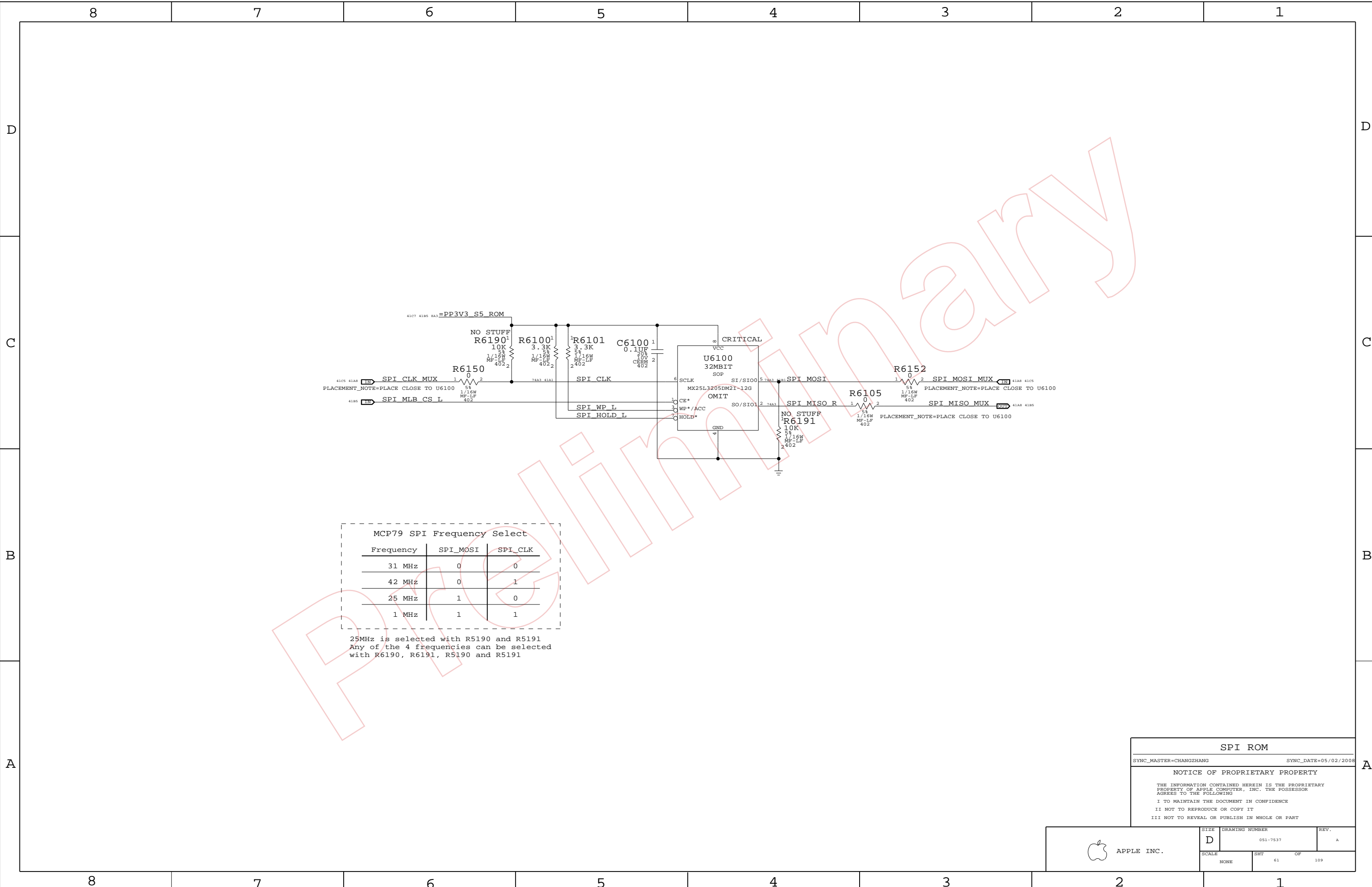
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	59		



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
 Any of the 4 frequencies can be selected
 with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

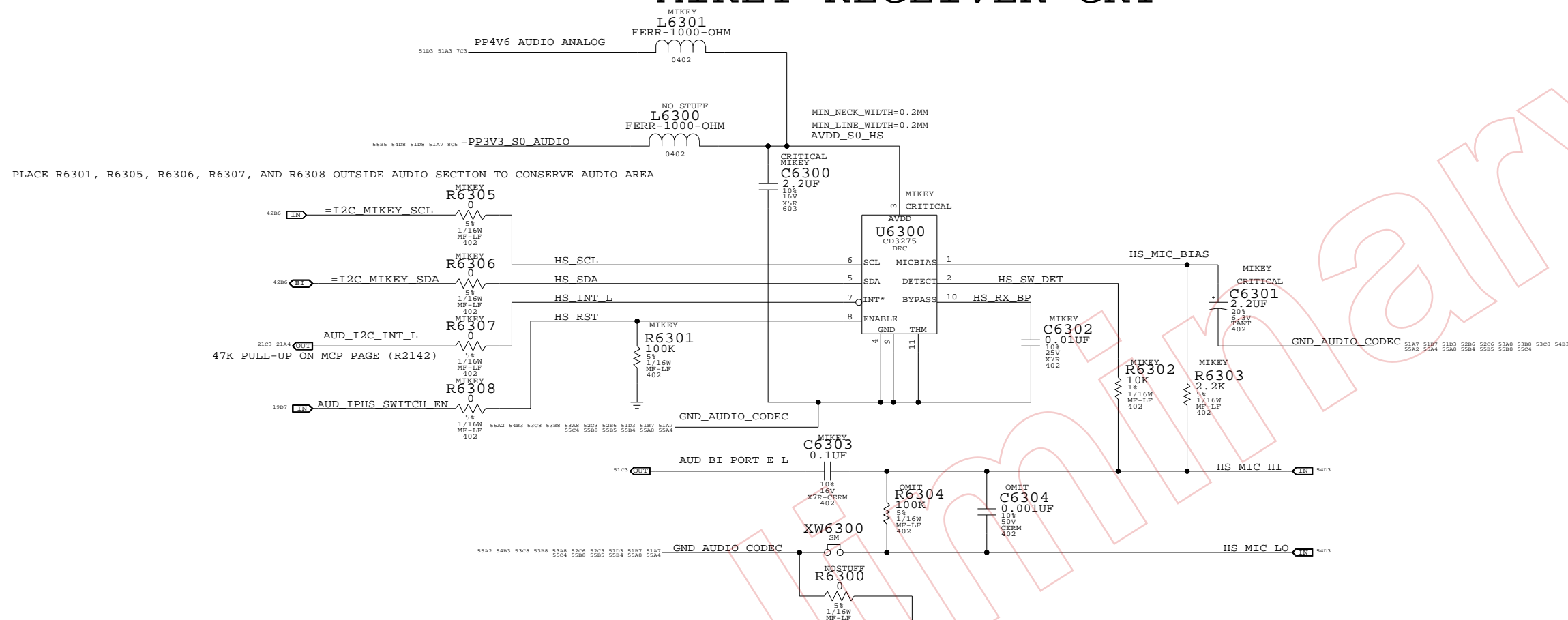
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	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	61		

MIKEY RECEIVER CKT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	100PF 50V 10% 0402 CAPACITOR	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

AUDIO: MIKEY

SYNC_MASTER=AUDIO SYNC_DATE=07/03/2008

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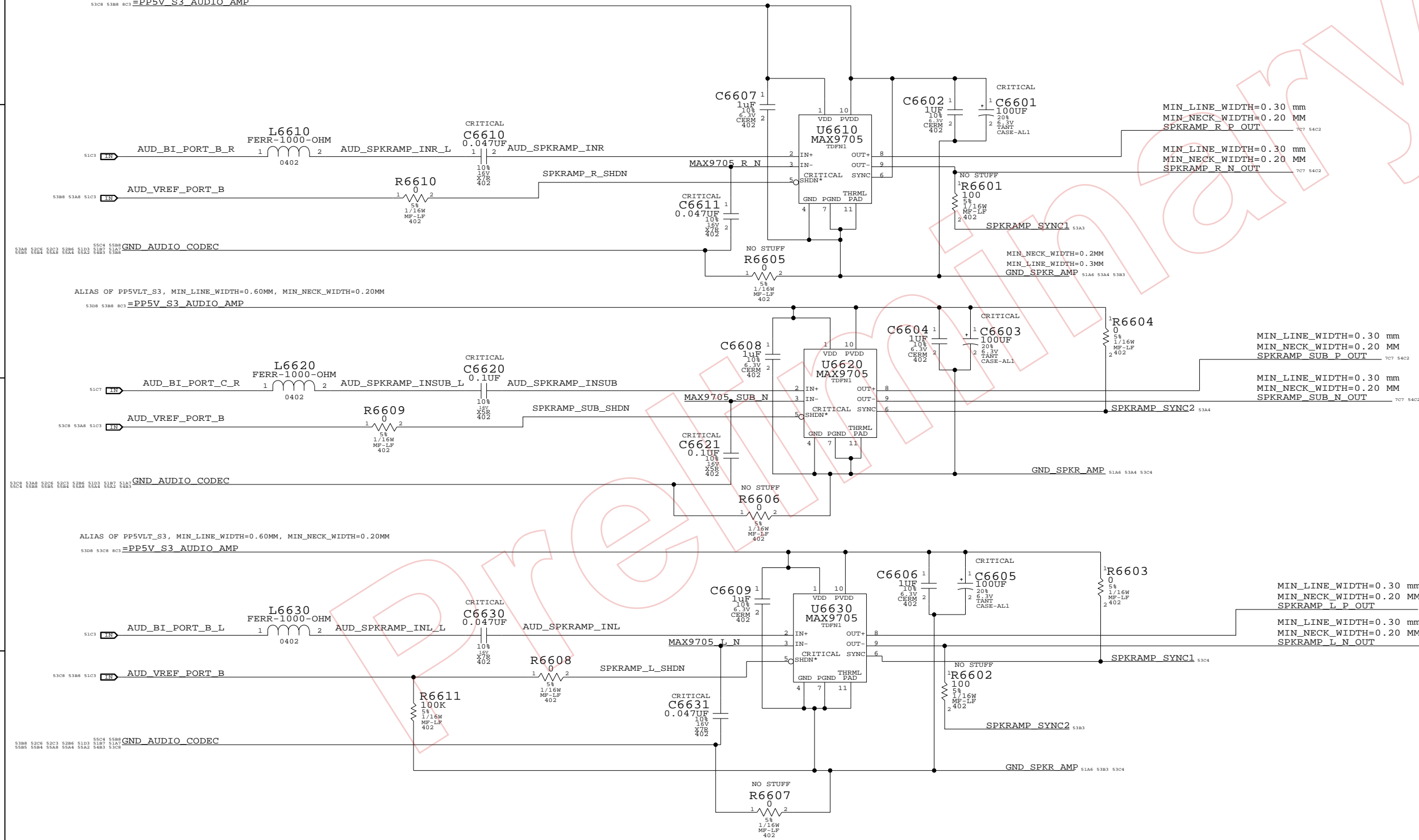


SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	63	109

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 12DB

ALIAS OF PP5VLT_S3, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM
 VOLTAGE=5V
 5308 5388 RC1=PP5V_S3_AUDIO_AMP



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	66		

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR
APN: 518S0520

SPEAKER CONNECTOR
APN: 518S0519

APN: 518S0521

MIC EMI FILTER

AUDIO: JACK

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

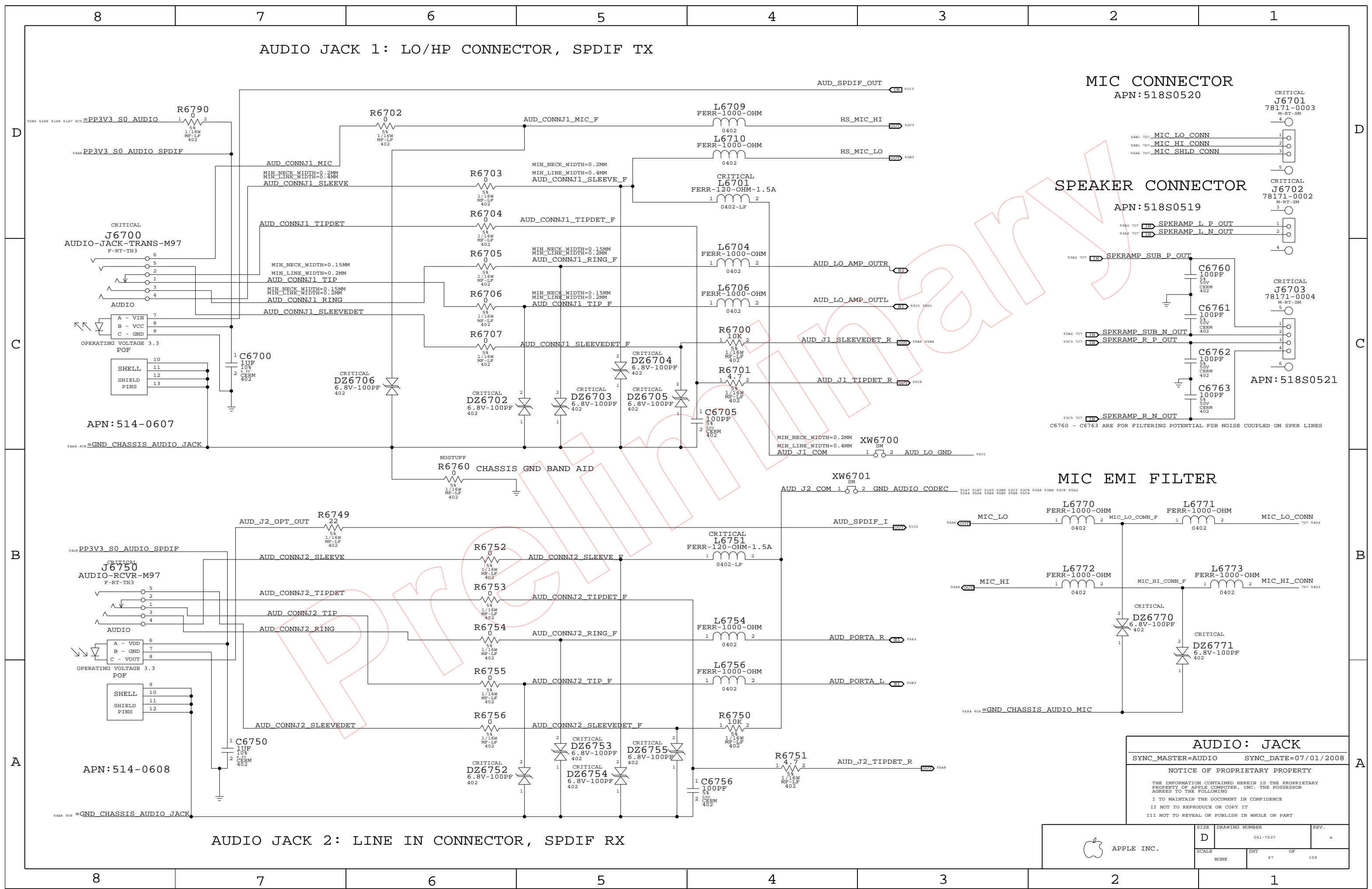
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	67	109



8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

A

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

8 7 6 5 4 3 2 1

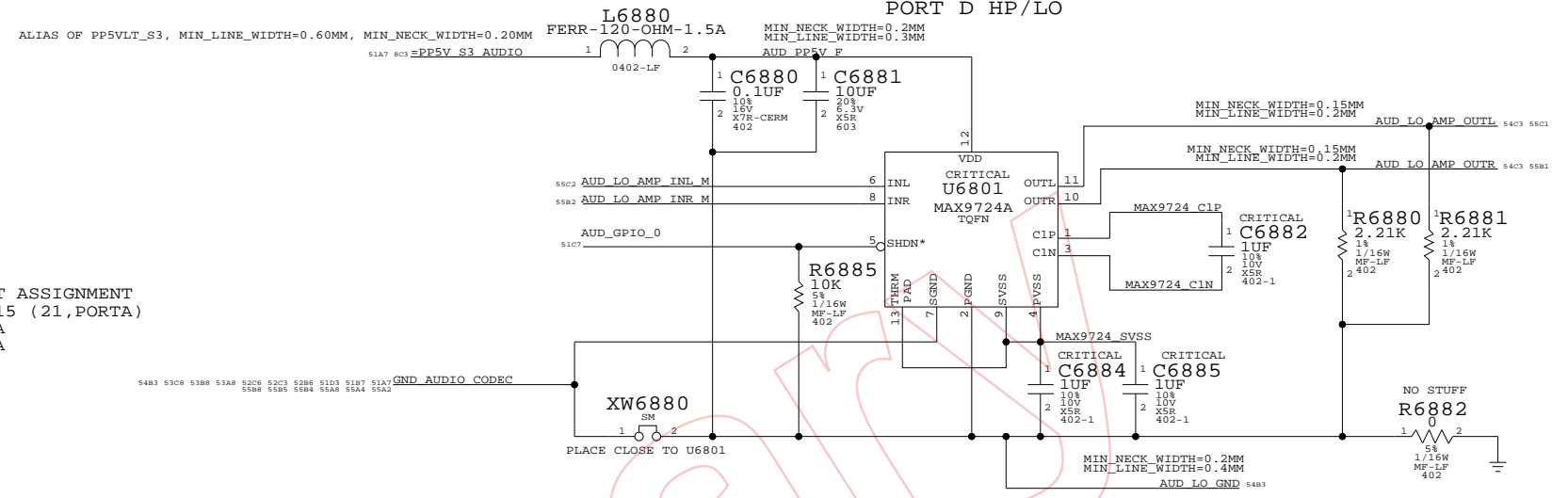
HP/LO AMP
APN:353S1637
PORT D HP/LO

CODEC OUTPUT SIGNAL PATHS

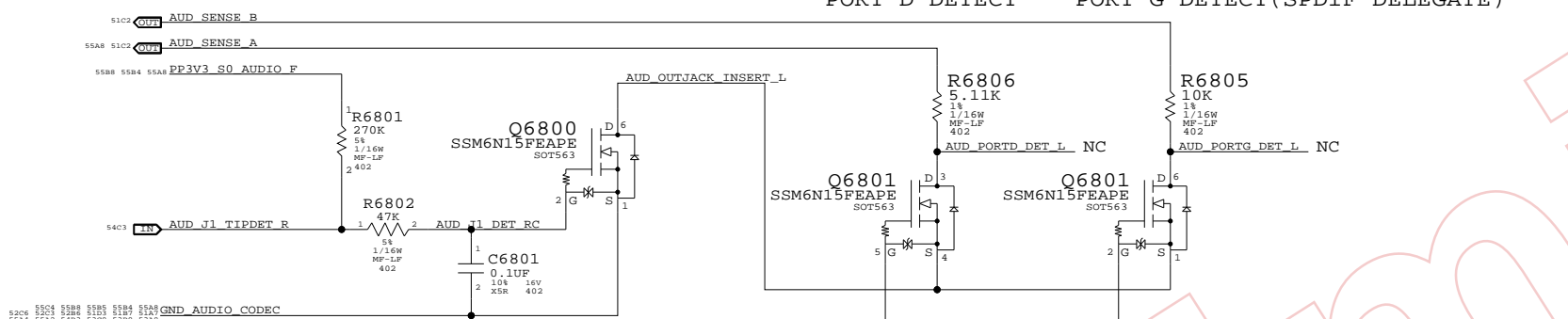
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0C (12)	0X02 (2)	0X14 (20,PORTD)	GPIO 0	0X14 (20,PORTD)
SAT SPKRS	0X0D (13)	0X03 (3)	0X18 (24,PORTB)	VREF_B(100%)	N/A
SUB SPKR	0X0F (15)	0X05 (5)	0X1A (26,PORTC)	VREF_B(100%)	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X16 (22, PORTG)

CODEC INPUT SIGNAL PATHS

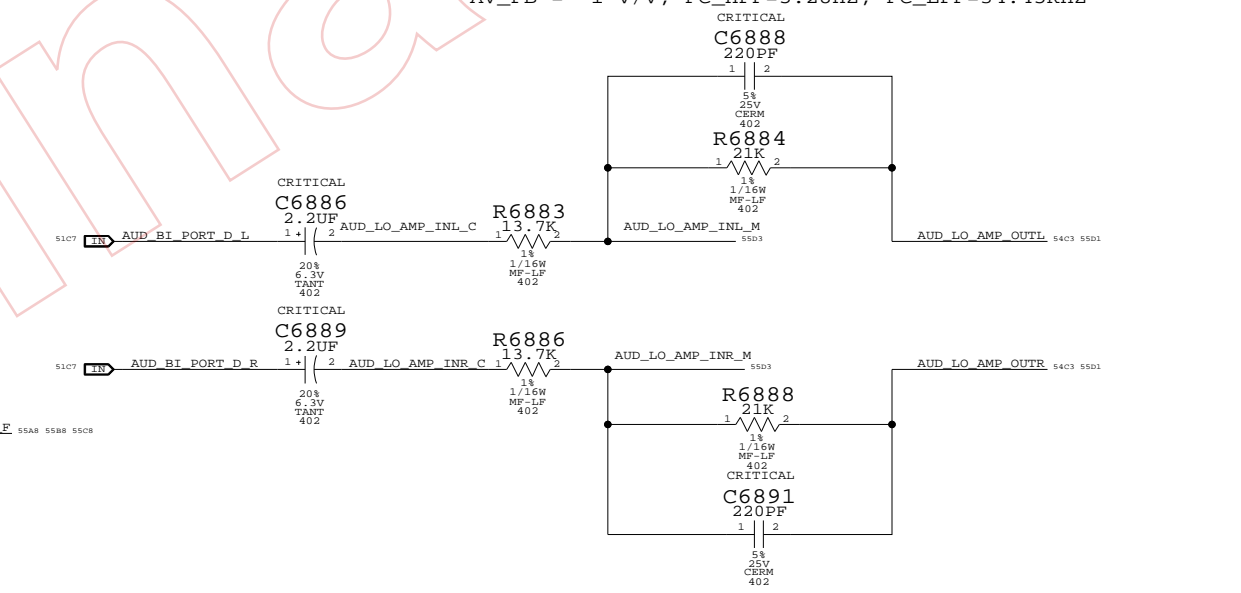
FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X15 (21,PORTA)	N/A	0X15 (21,PORTA)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X19 (25,PORTF)	VREF_F (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A



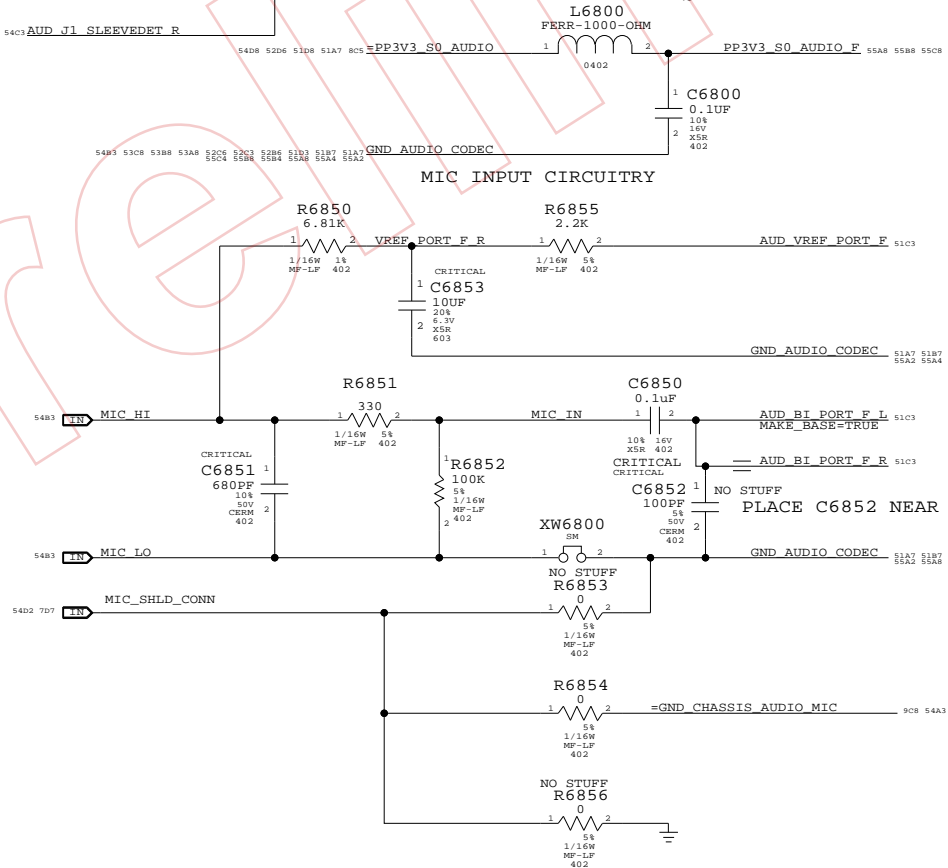
PORT D DETECT PORT G DETECT (SPDIF DELEGATE)



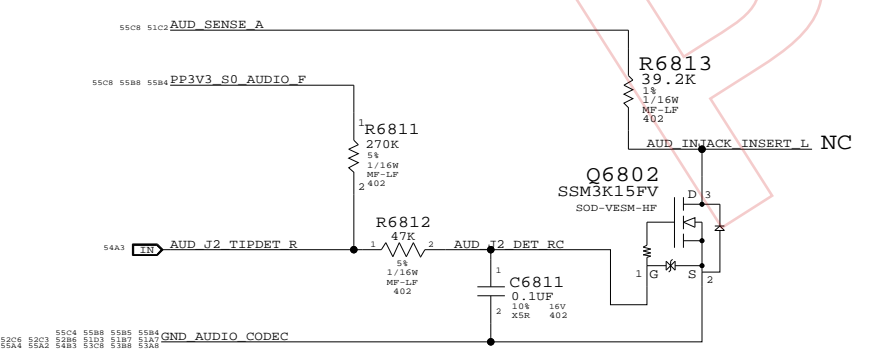
MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1 V/V, FC_HPF=5.28HZ, FC_LPF=34.45KHZ



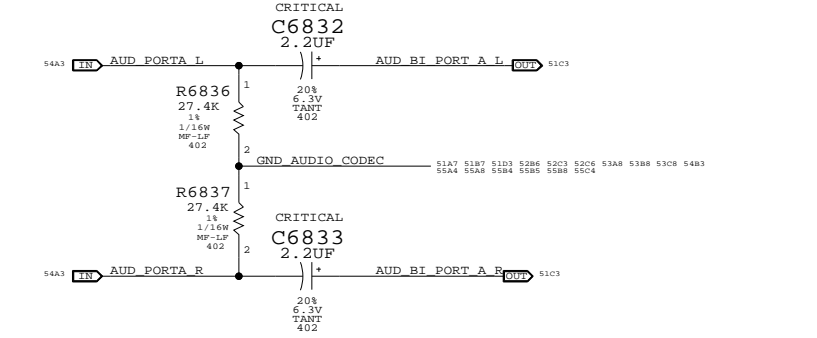
MIC INPUT CIRCUITRY



LINE-IN (PORT A) DETECT



PORT A LI



AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

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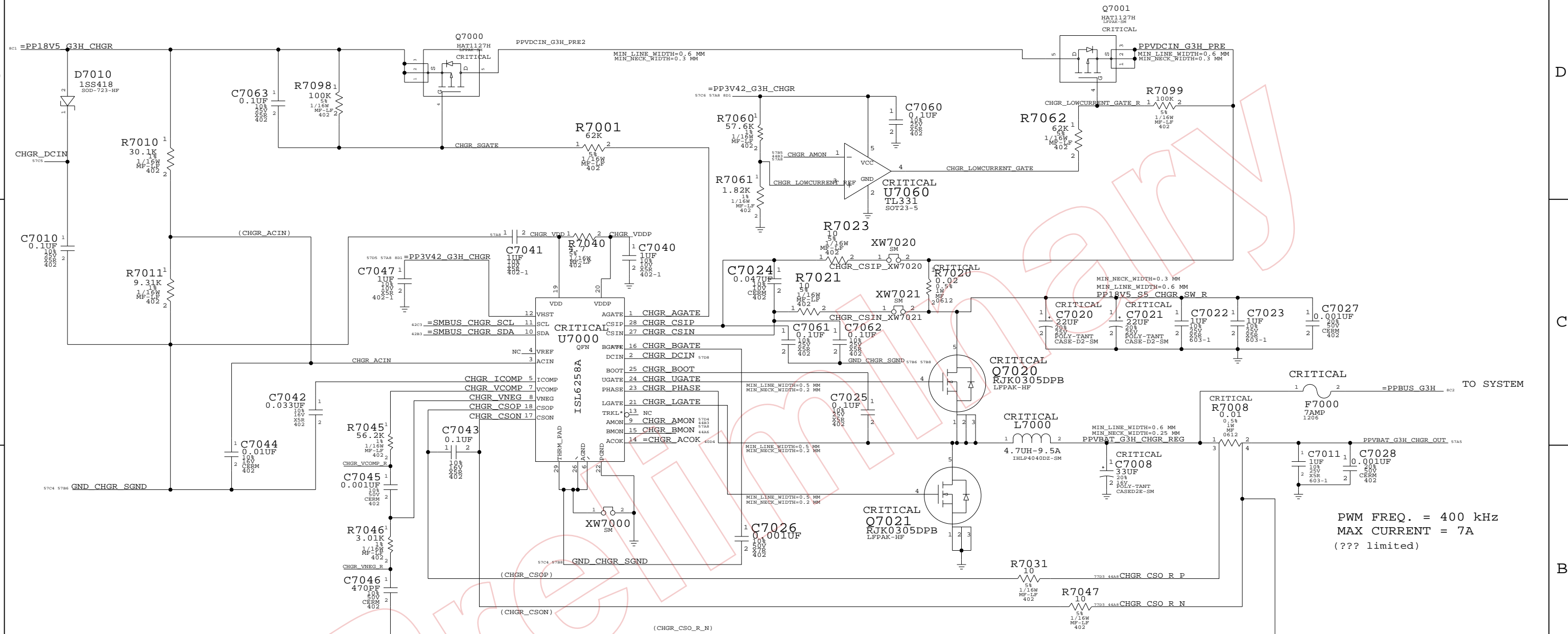
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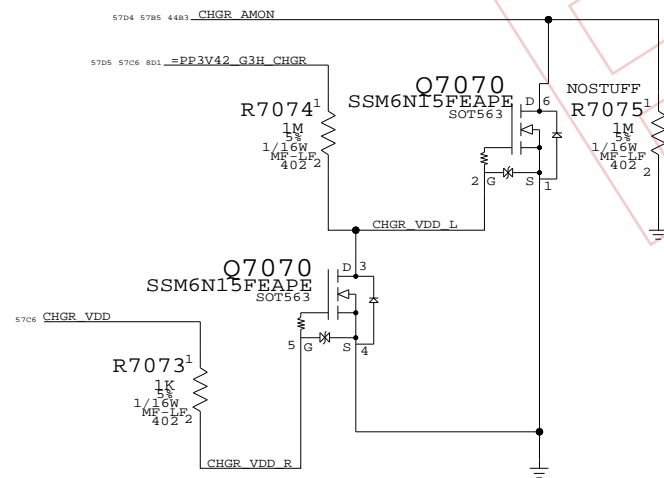
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	68		

PBUS SUPPLY / BATTERY CHARGER

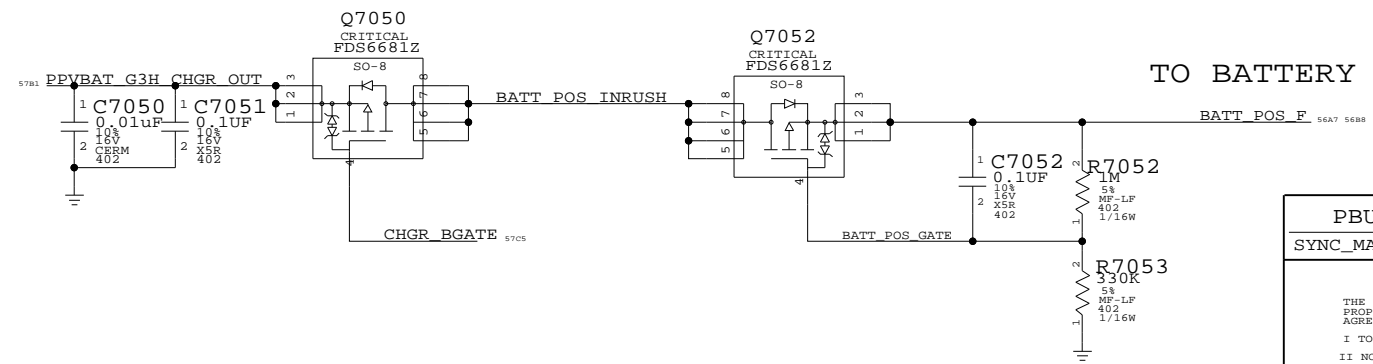


PWM FREQ. = 400 kHz
MAX CURRENT = 7A
(??? limited)

AMON PULLDOWN LOGIC



BATTERY INRUSH FETS



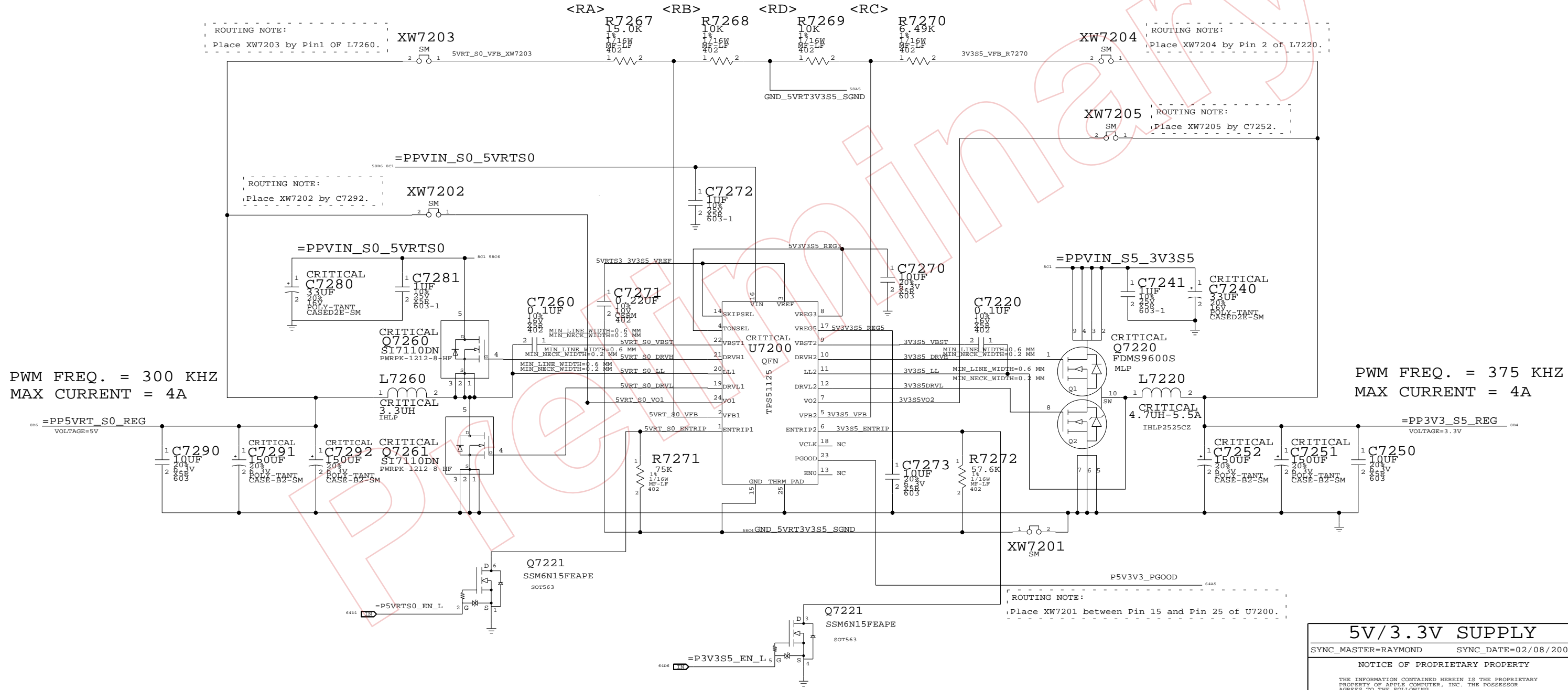
PBUS Supply/Battery Charger
 SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	70		

5V_RT/3.3V POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

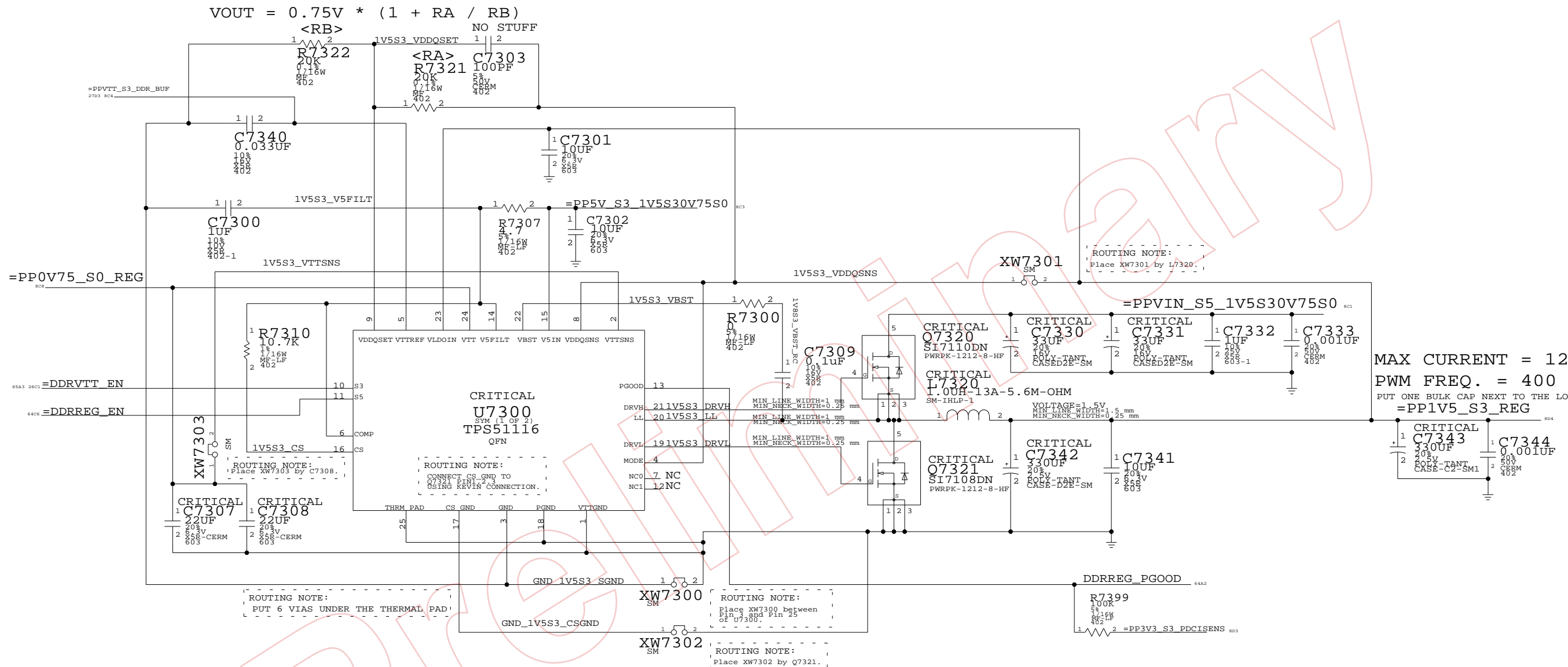
PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

SEPARATED MASTER PGOOD FOR BOTH 5V AND 3V3.

5V/3.3V SUPPLY	
SYNC_MASTER=RAYMOND	SYNC_DATE=02/08/2008
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	72		

1.5V/0.75V (DDR3) POWER SUPPLY



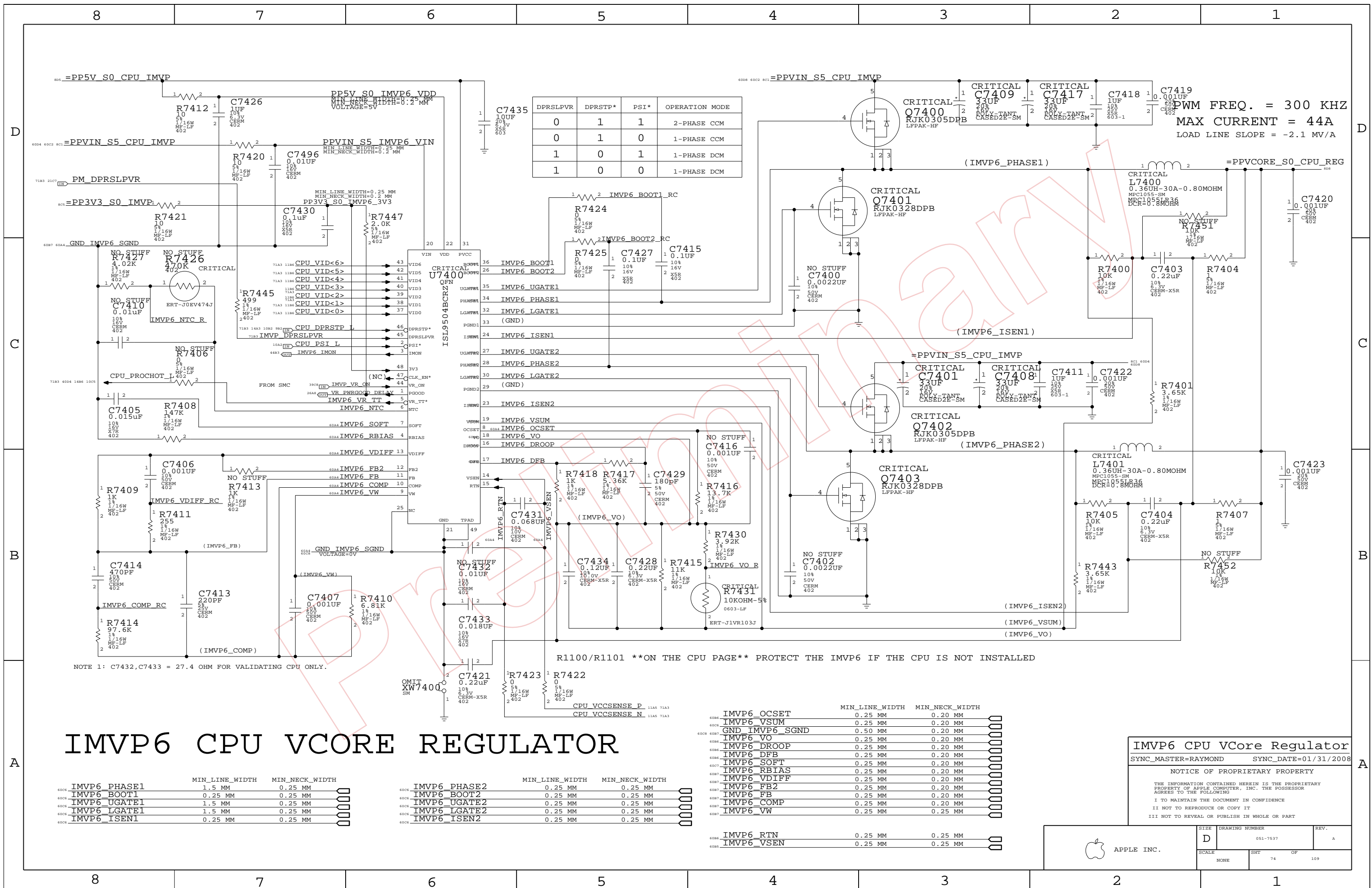
MAX CURRENT = 12A
 PWM FREQ. = 400 KHZ
 PUT ONE BULK CAP NEXT TO THE LOAD
 =PP1V5_S3_REG

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

1.5V/0.75V DDR3 SUPPLY
 SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	73	109



DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PWM FREQ. = 300 KHZ
 MAX CURRENT = 44A
 LOAD LINE SLOPE = -2.1 MV/A

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCore Regulator

MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM 0.25 MM
IMVP6_BOOT1	0.25 MM 0.25 MM
IMVP6_UGATE1	1.5 MM 0.25 MM
IMVP6_LGATE1	1.5 MM 0.25 MM
IMVP6_ISEN1	0.25 MM 0.25 MM

MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM 0.25 MM
IMVP6_BOOT2	0.25 MM 0.25 MM
IMVP6_UGATE2	0.25 MM 0.25 MM
IMVP6_LGATE2	0.25 MM 0.25 MM
IMVP6_ISEN2	0.25 MM 0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

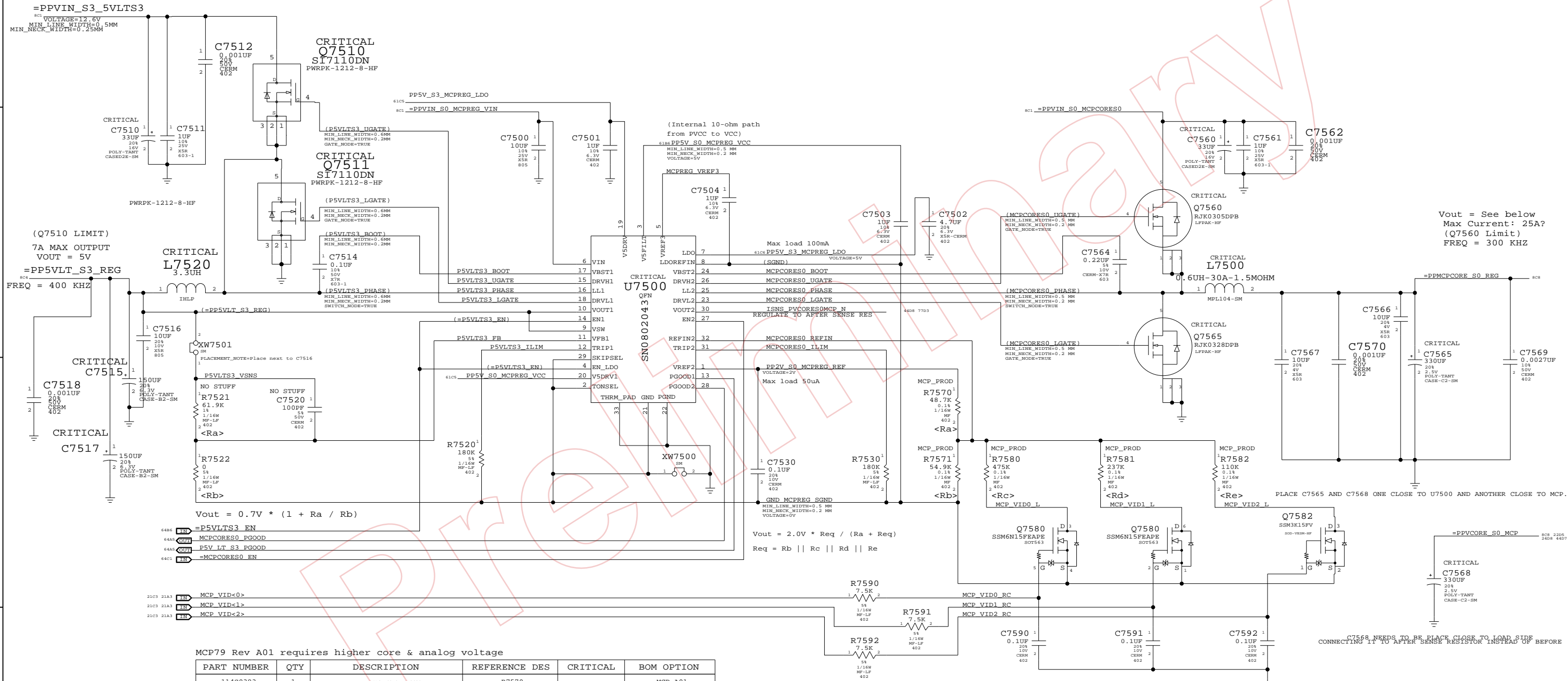
IMVP6 CPU VCore Regulator
 SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

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	D	051-7537	A
SCALE	SHEET	OF	
NONE	74	109	

NOTE 1: C7432,C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

MCP VCORE / 5V_S3 LEFT REGULATOR



(Q7510 LIMIT)
7A MAX OUTPUT
VOUT = 5V
FREQ = 400 KHZ

Vout = See below
Max Current: 25A?
(Q7560 Limit)
FREQ = 300 KHZ

$$V_{out} = 0.7V * (1 + R_a / R_b)$$

$$V_{out} = 2.0V * Req / (Ra + Req)$$

$$Req = R_b || R_c || R_d || R_e$$

- 6486 EN1 = P5VLT3_EN
- 6485 PG2 = MCPCORES0_PGOOD
- 6484 PG1 = P5V LT S3_PGOOD
- 6481 EN2 = MCPCORES0_EN
- 21C3 21A3 EN3 = MCP_VID<0>
- 21C3 21A3 EN4 = MCP_VID<1>
- 21C3 21A3 EN5 = MCP_VID<2>

MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0383	1	RES.MTL.FILM,1/16W,49.9K,1,0402,SMD,LP	R7570		MCP_A01
114S0401	1	RES.MTL.FILM,1/16W,76.7K,1,0402,SMD,LP	R7571		MCP_A01
114S0484	1	RES.MTL.FILM,1/16W,549K,1,0402,SMD,LP	R7580		MCP_A01
114S0454	1	RES.MTL.FILM,1/16W,274K,1,0402,SMD,LP	R7581		MCP_A01
114S0423	1	RES.MTL.FILM,1/16W,133K,1,0402,SMD,LP	R7582		MCP_A01
114S0373	1	RES.MTL.FILM,1/16W,40.2K,1,0402,SMD,LP	R7570		MCP_A01P&MCP_A01Q
114S0404	1	RES.MTL.FILM,1/16W,84.5K,1,0402,SMD,LP	R7571		MCP_A01P&MCP_A01Q
114S0458	1	RES.MTL.FILM,1/16W,301K,1,0402,SMD,LP	R7580		MCP_A01P&MCP_A01Q
114S0447	1	RES.MTL.FILM,1/16W,237K,1,0402,SMD,LP	R7581		MCP_A01P&MCP_A01Q
114S0411	1	RES.MTL.FILM,1/16W,100K,1,0402,SMD,LP	R7582		MCP_A01P&MCP_A01Q

Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:
 Added C7568 bulk cap on output.
 Tied TON to REF.
 Changed Q7510 to 376S0674.
 C7500 changed to 138S0638.
 L7560 changed from T18 MLB inductor to 152S0782.
 Changed Q7565 to 376S0637.
 Changed R7514 to 280K, R7564 to 180K.

MCP VCORE REGULATOR

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

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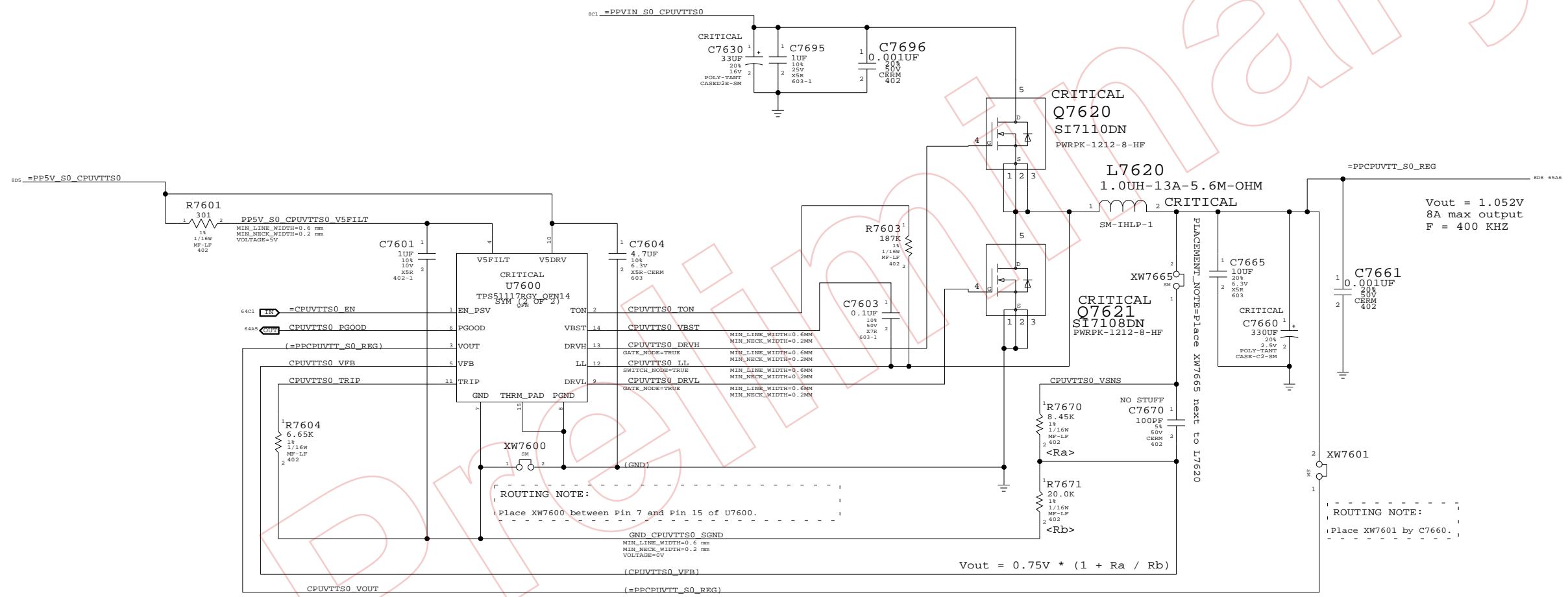
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APPLE INC.

SIZE: D DRAWING NUMBER: 051-7537 REV: A

SCALE: NONE SHEET: 75 OF: 109

CPUVTT POWER SUPPLY



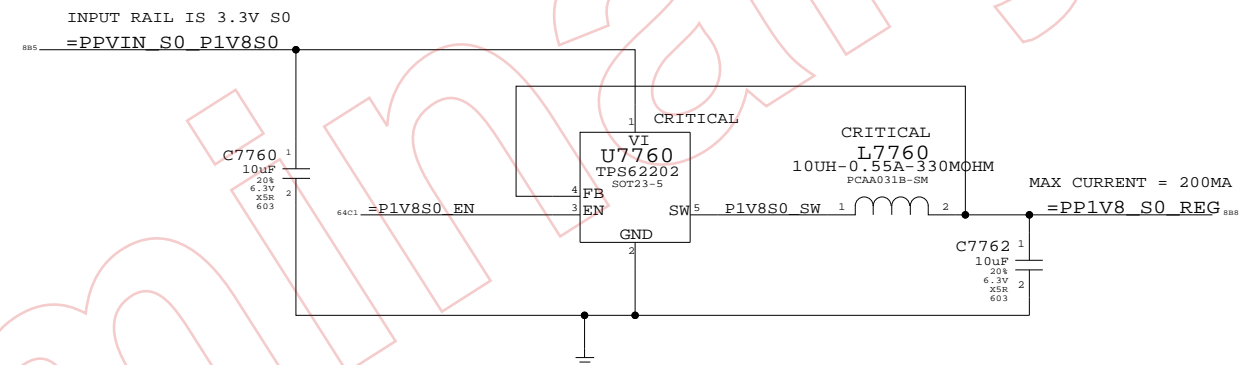
ROUTING NOTE:
Place XW7600 between Pin 7 and Pin 15 of U7600.

ROUTING NOTE:
Place XW7601 by C7660.

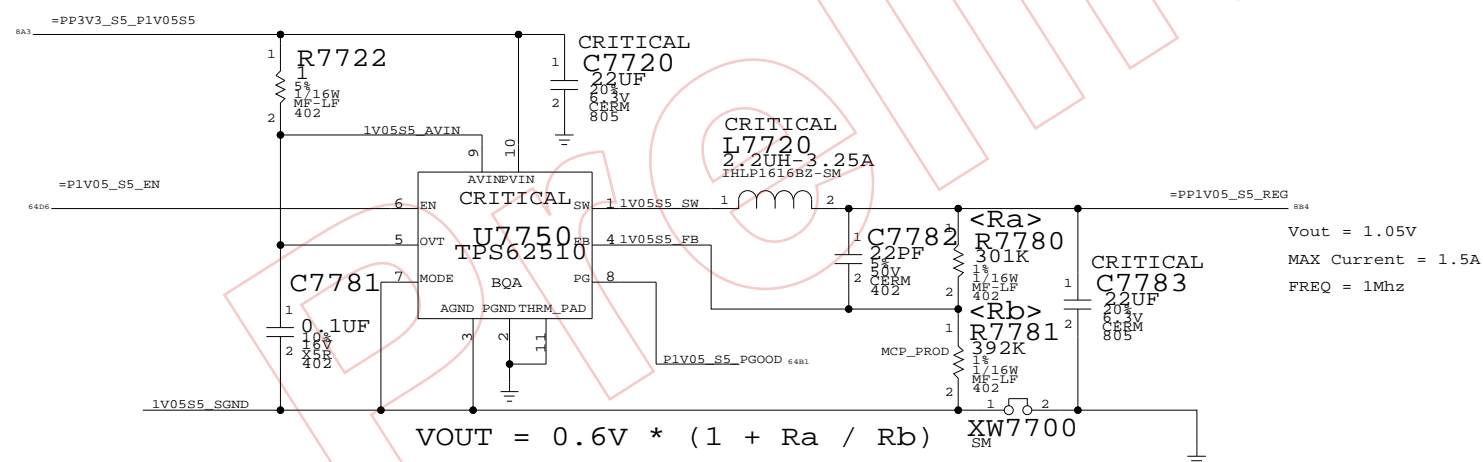
CPU VTT(1.05V) SUPPLY
 SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	76		

1.8V S0 SWITCHER



MCP 1.05V_S5 AUXC SUPPLY



MCP79 Rev A01 requires higher voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781		MCP_A01&MCP_A01P&MCP_A01Q

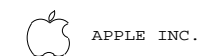
VOUT = 1.102V

MISC POWER SUPPLIES

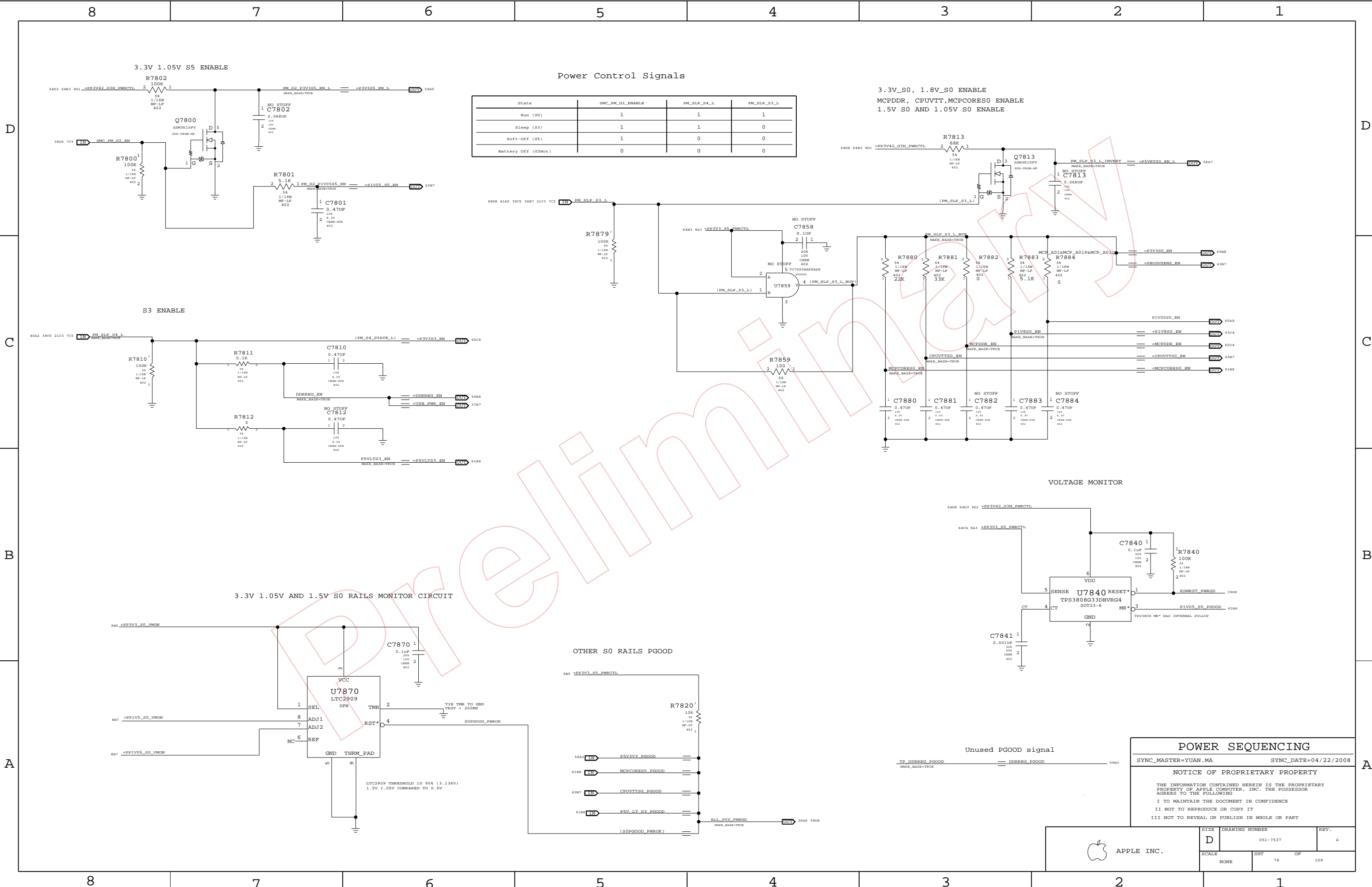
SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	77	109



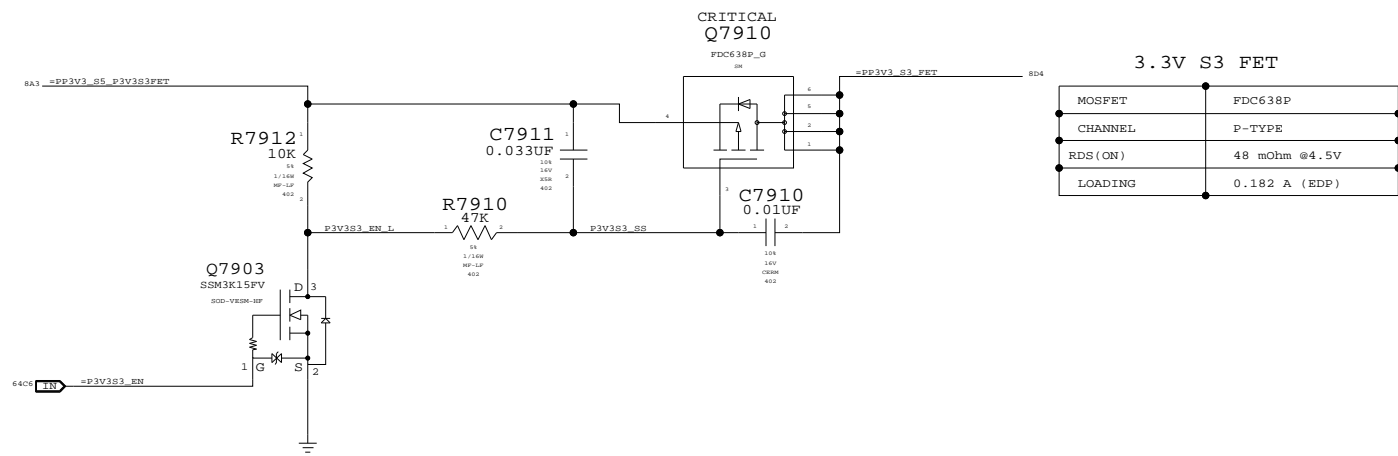
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

POWER SEQUENCING
 SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

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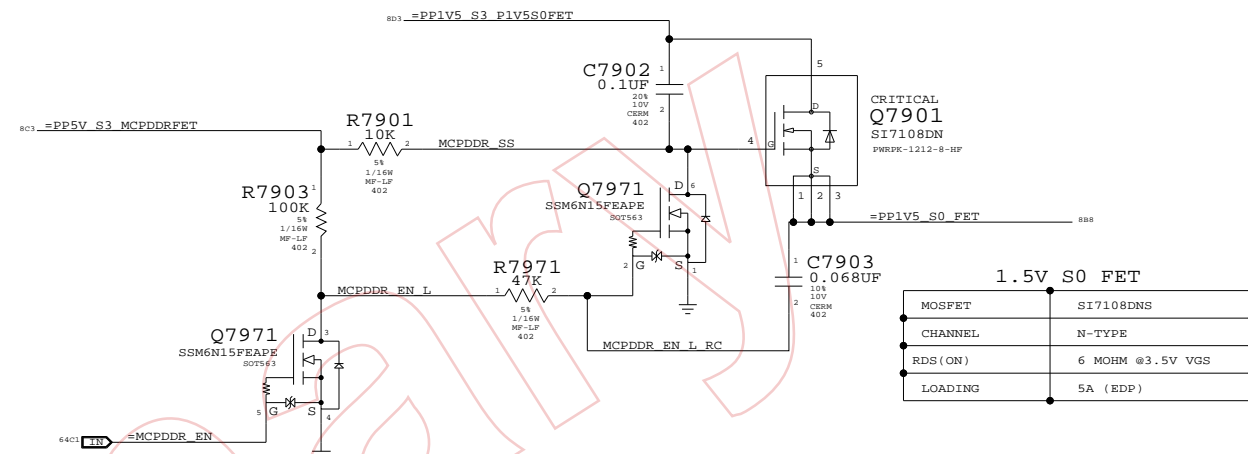
3.3V S3 FET



3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

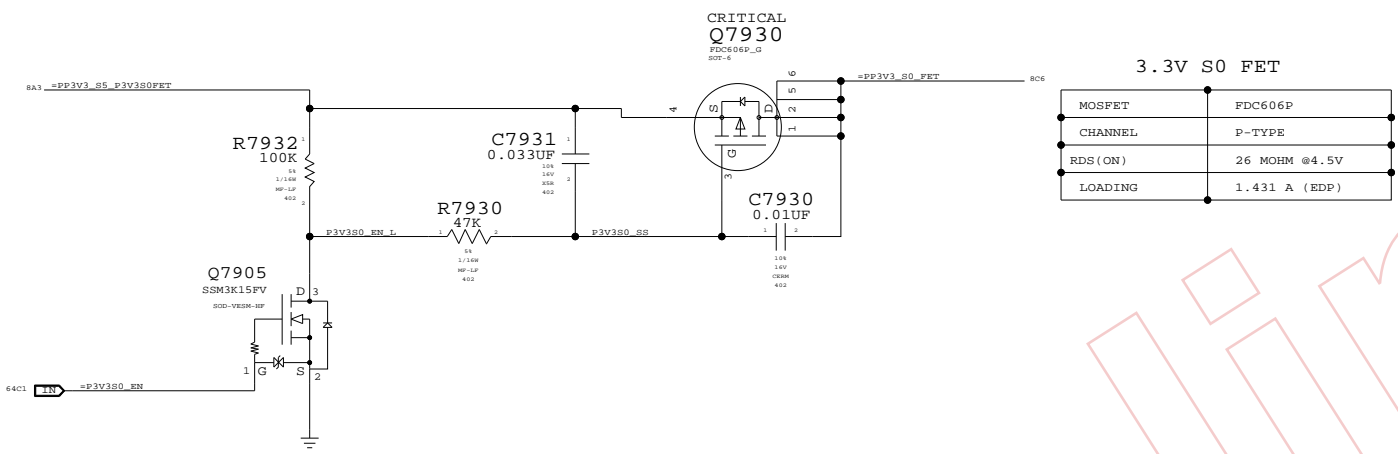
1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

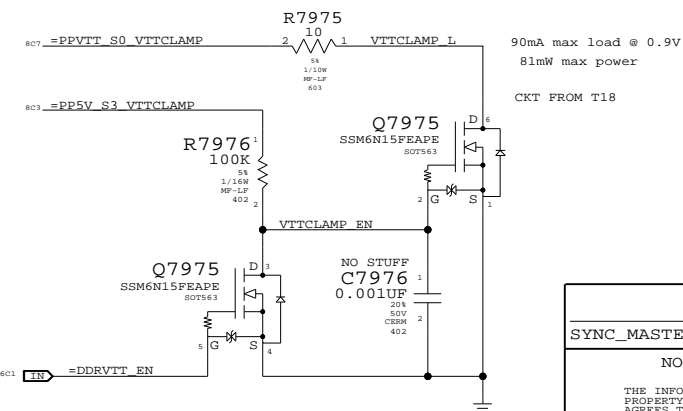
3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

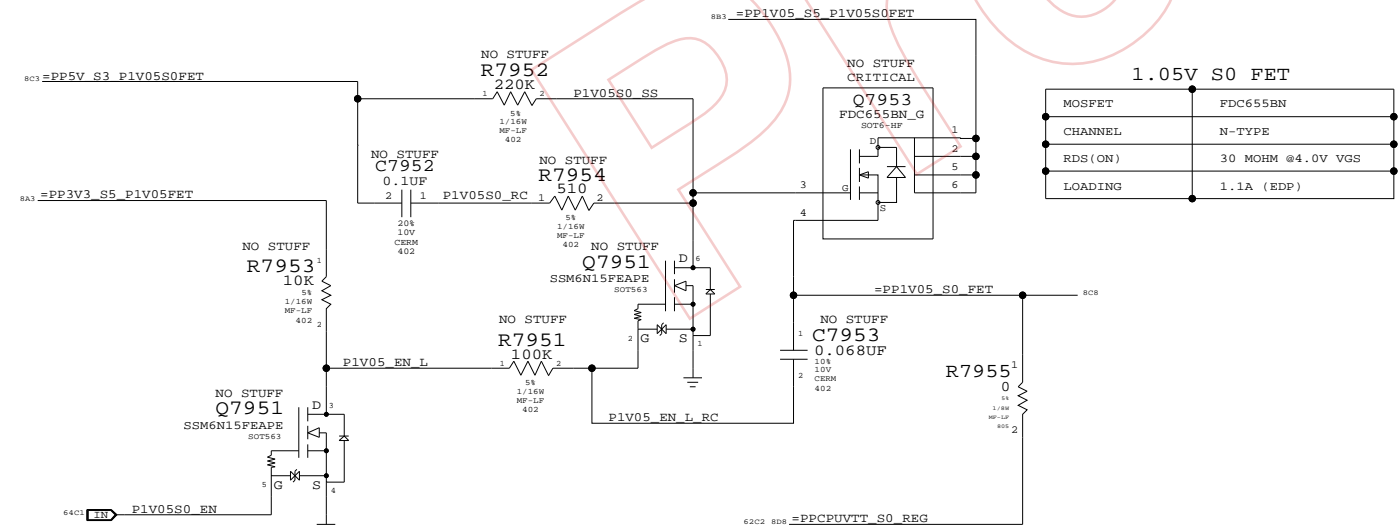
MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS
 SYNC_MASTER=YUAN.MA SYNC_DATE=04/04/2008
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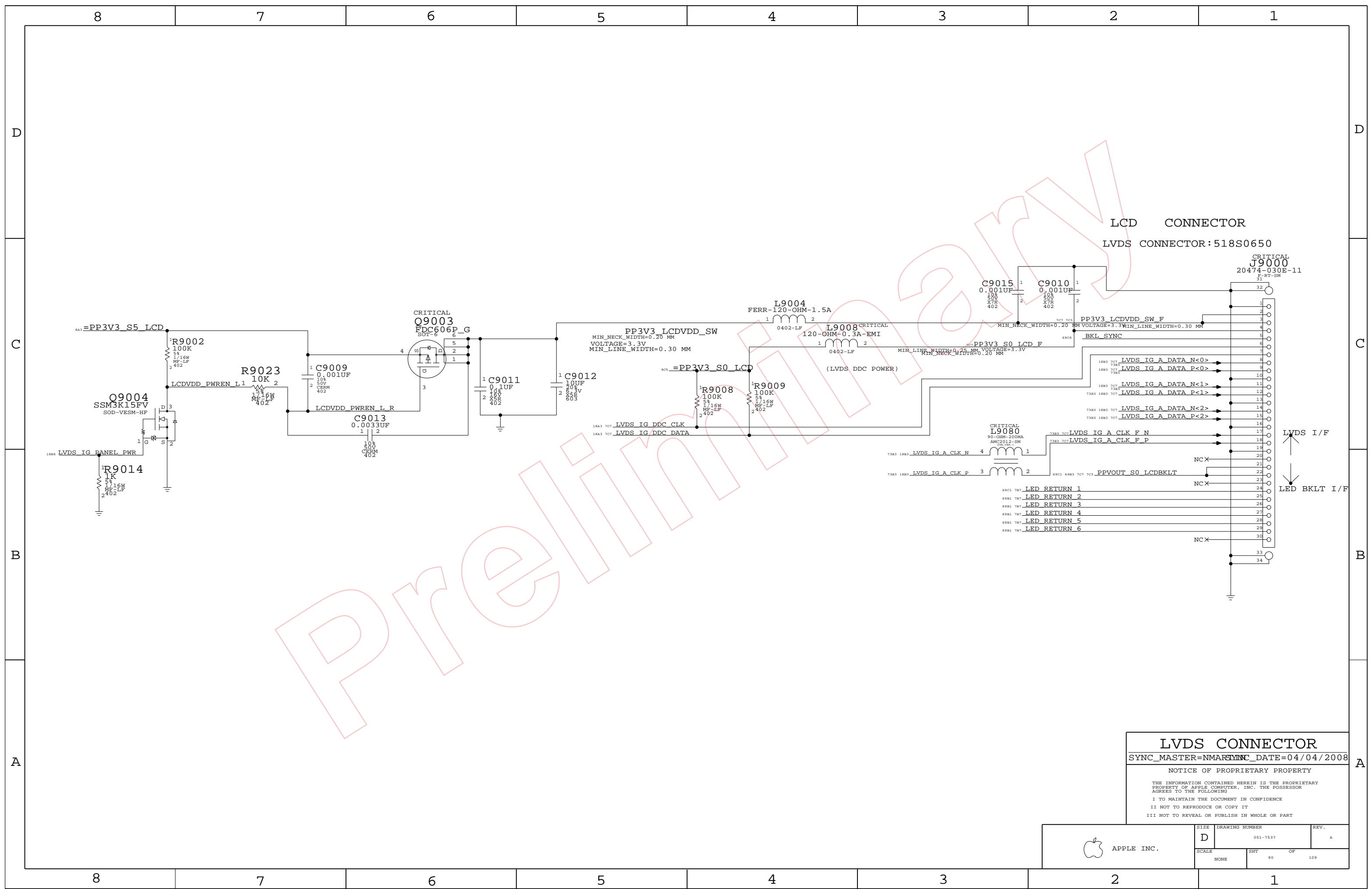
1.05V S0 FET



1.05V S0 FET	
MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	30 MOHM @4.0V VGS
LOADING	1.1A (EDP)

D
C
B
A

D
C
B
A



LCD CONNECTOR
LVDS CONNECTOR: 518S0650

CRITICAL
J9000
20474-030E-11
F-K2-SM

LVDS I/F
LED BKL T I/F

LVDS CONNECTOR
SYNC_MASTER=NMARSYNC_DATE=04/04/2008

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	D	051-7537	A
SCALE	SHT	OF	109
NONE	90		

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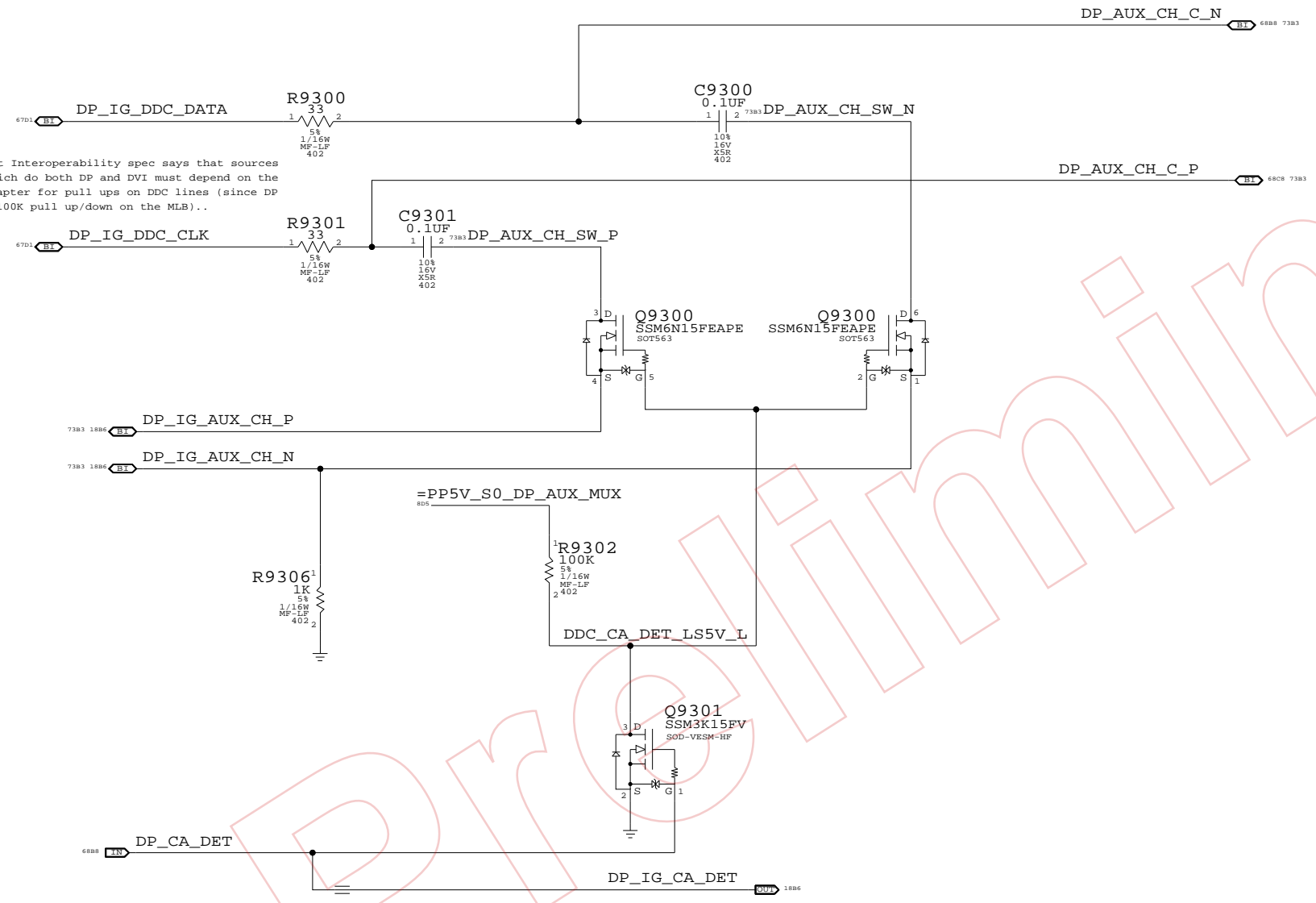
3

2

1

1886	=MCP_HDMI_TXC_P	DP_ML_P<3>	68C8_7383
1886	=MCP_HDMI_TXC_N	DP_ML_N<3>	MAKE_BASE=TRUE 68C8_7383
1886	=MCP_HDMI_TXD_P<0>	DP_ML_P<2>	MAKE_BASE=TRUE 68C1_7383
1886	=MCP_HDMI_TXD_N<0>	DP_ML_N<2>	MAKE_BASE=TRUE 68A1_7383
1886	=MCP_HDMI_TXD_P<1>	DP_ML_P<1>	MAKE_BASE=TRUE 68C1_7383
1886	=MCP_HDMI_TXD_N<1>	DP_ML_N<1>	MAKE_BASE=TRUE 68C1_7383
1886	=MCP_HDMI_TXD_P<2>	DP_ML_P<0>	MAKE_BASE=TRUE 68C1_7383
1886	=MCP_HDMI_TXD_N<2>	DP_ML_N<0>	MAKE_BASE=TRUE 68C1_7383
1886	=MCP_HDMI_HPD	DP_HPD	MAKE_BASE=TRUE 68A8
18A1	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	67C8
18A1	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BASE=TRUE 67C8

Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)...



DISPLAYPORT SUPPORT
 SYNC_MASTER=AMASON SYNC_DATE=04/18/2008
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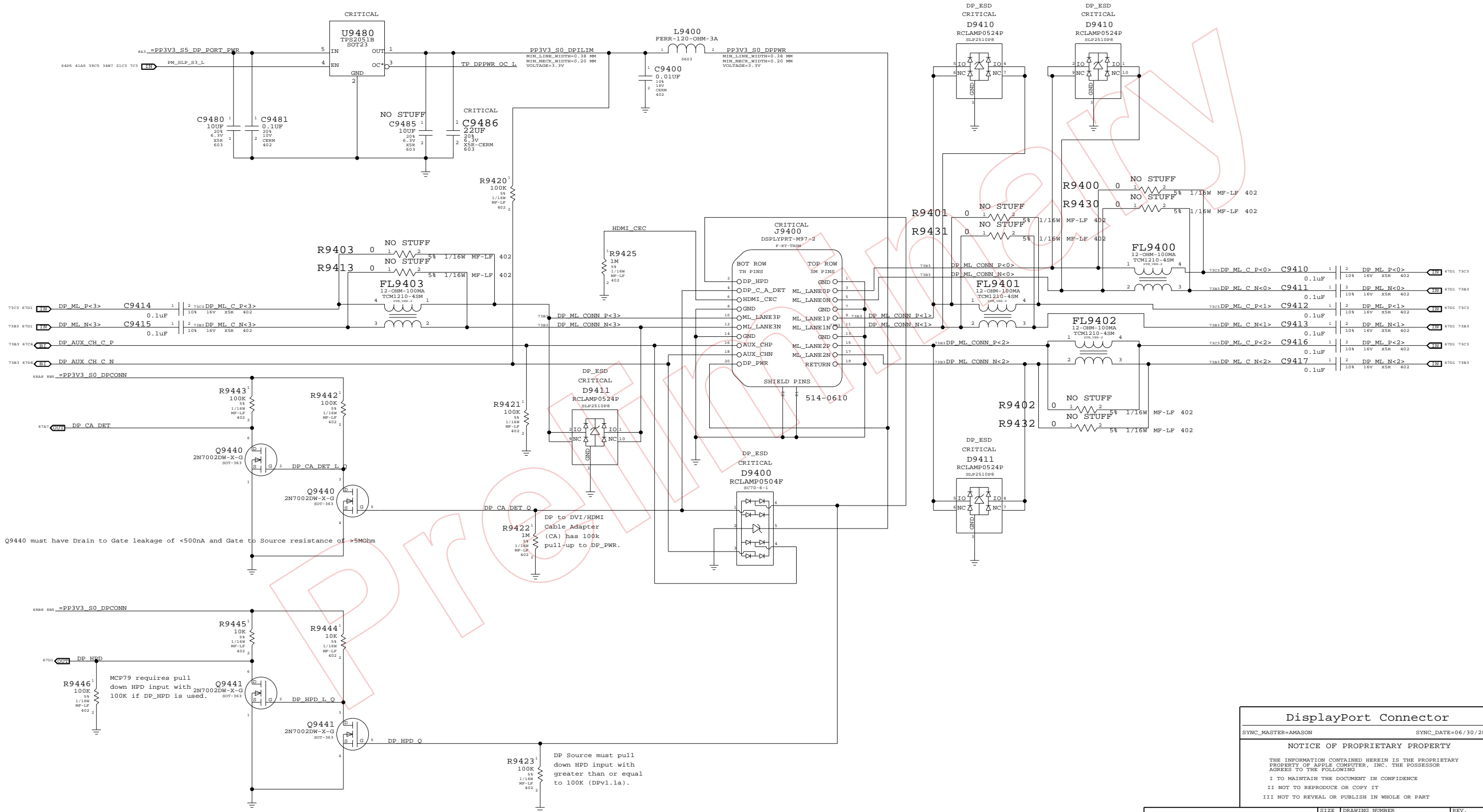
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2

1

Port Power Switch

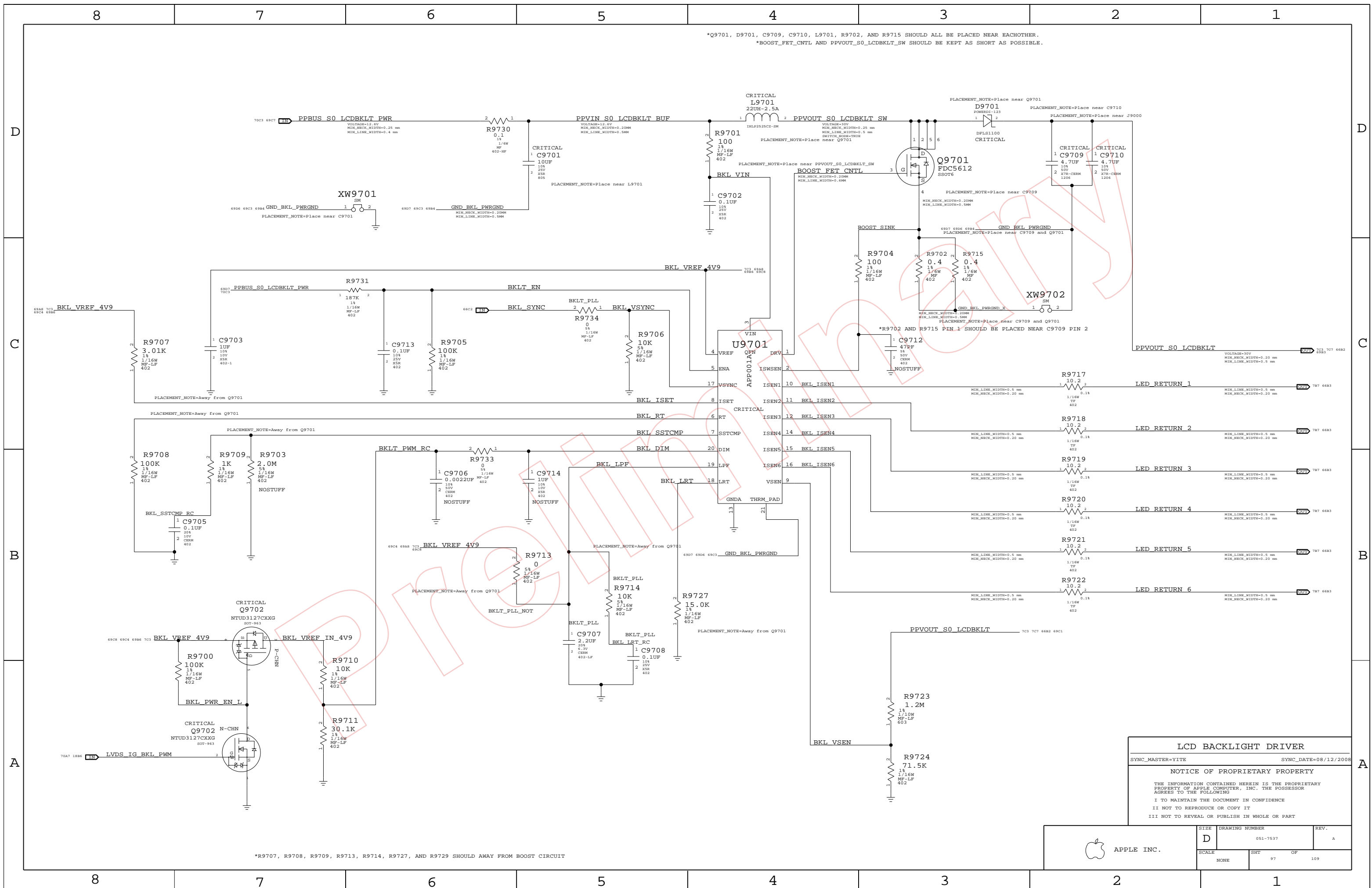


Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MΩm

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

DisplayPort Connector
 SYNC_MASTER=AMASON SYNC_DATE=06/30/2008
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SCALE	SHT	OF	109
NONE	94		

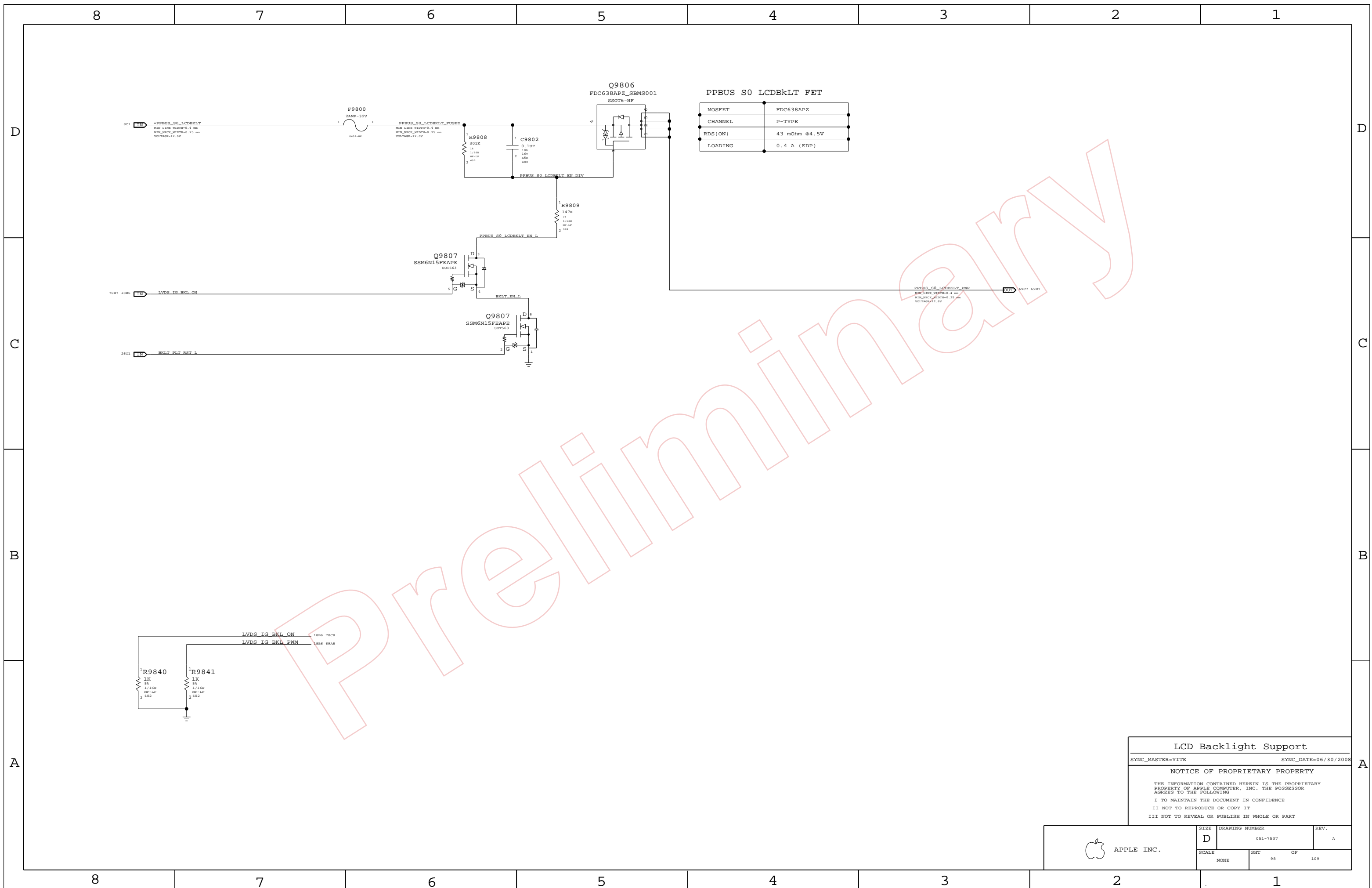


*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
 *BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

LCD BACKLIGHT DRIVER
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE	SHT	OF	109
NONE	97		



LCD Backlight Support

SYNC_MASTER=VITE SYNC_DATE=06/30/2008

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	SCALE NONE	SHT 98	OF 109

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
FSB_DATA_GROUP0	FSB_50S	FSB_DATA		FSB D L<15..0> 1004 1403
FSB_DATA_GROUP0	FSB_50S	FSB_DATA		FSB DINV L<0> 1004 1406
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L P<0> 1004 1406
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L N<0> 1004 1406
FSB_DATA_GROUP1	FSB_50S	FSB_DATA		FSB D L<31..16> 1084 1004 1403 1403
FSB_DATA_GROUP1	FSB_50S	FSB_DATA		FSB DINV L<1> 1084 1406
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L P<1> 1084 1406
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L N<1> 1084 1406
FSB_DATA_GROUP2	FSB_50S	FSB_DATA		FSB D L<47..32> 1002 1483 1403
FSB_DATA_GROUP2	FSB_50S	FSB_DATA		FSB DINV L<2> 1002 1406
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L P<2> 1002 1406
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L N<2> 1002 1406
FSB_DATA_GROUP3	FSB_50S	FSB_DATA		FSB D L<63..48> 1082 1002 1483
FSB_DATA_GROUP3	FSB_50S	FSB_DATA		FSB DINV L<3> 1082 1406
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L P<3> 1082 1406
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB		FSB DSTB L N<3> 1082 1406
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR		FSB A L<16..3> 1008 1406 1406
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR		FSB REQ L<4..0> 1008 1486
FSB_ADSTB0	FSB_50S	FSB_ADSTB		FSB ADSTB L<0> 1008 1486
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR		FSB A L<35..17> 1008 1486 1406
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR		FSB ADSTB L<1> 1008 1486
FSB_1X	FSB_50S	FSB_1X		FSB ADS L 1006 1486
FSB_BREQ0_1	FSB_50S	FSB_1X		FSB BREQ0 L 982 1006 1486
FSB_BREQ1_1	FSB_50S	FSB_1X		FSB BREQ1 L 1486
FSB_1X	FSB_50S	FSB_1X		FSB BNR L 1006 1486
FSB_1X	FSB_50S	FSB_1X		FSB BPR1 L 1006 1483
FSB_1X	FSB_50S	FSB_1X		FSB DBSY L 1006 1486
FSB_1X	FSB_50S	FSB_1X		FSB DEFER L 1006 1483
FSB_1X	FSB_50S	FSB_1X		FSB DRDY L 1006 1486
FSB_1X	FSB_50S	FSB_1X		FSB HIT L 1006 1486
FSB_1X	FSB_50S	FSB_1X		FSB HITM L 1006 1486
FSB_1X	FSB_50S	FSB_1X		FSB LOCK L 1006 1486
FSB_CPURST_L	FSB_50S	FSB_1X		FSB CPURST L 982 1006 1382 1443
FSB_1X	FSB_50S	FSB_1X		FSB BS L<2..0> 1006 1446
FSB_1X	FSB_50S	FSB_1X		FSB TRDY L 1006 1486
CPU_ASYNC	CPU_50S	CPU_AGTL		CPU A20M L 1008 1443
CPU_BSEL	CPU_50S	CPU_AGTL		CPU BSEL<2..0> 902 1044 1084
CPU_FERR_L	CPU_50S	CPU_BMT		CPU FERR L 1008 1487
CPU_ASYNC	CPU_50S	CPU_AGTL		CPU IGARNE L 1008 1443
CPU_INIT_L	CPU_50S	CPU_AGTL		CPU INIT L 1006 1443
CPU_ASYNC_R	CPU_50S	CPU_AGTL		CPU INTR 982 1088 1443
CPU_ASYNC_R	CPU_50S	CPU_AGTL		CPU NMI 982 1088 1443
CPU_PROCHOT_L	CPU_50S	CPU_AGTL		CPU PROCHOT L 1005 1486 4004 6008
CPU_PWRGD	CPU_50S	CPU_AGTL		CPU_PWRGD 1082 1307 1443
CPU_ASYNC	CPU_50S	CPU_AGTL		CPU SMI L 1088 1443
CPU_ASYNC	CPU_50S	CPU_AGTL		CPU STPECLK L 1088 1443
PM_THERMTRIP_L	CPU_50S	CPU_BMT		PM_THERMTRIP L 1006 1487 4004
FSB_CPURST_L	CPU_50S	CPU_AGTL		FSB CPURST L 1082 1443
CPU_PDRSR	CPU_50S	CPU_AGTL		CPU_DPSLP L 1082 1443
CPU_DPRSTP_L	CPU_50S	CPU_AGTL		CPU DPRSTP L 982 1082 1443 6007
CPU_ASYNC	CPU_50S	CPU_AGTL		FSB DPWR L 1082 1443
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP		MCP BCLK VML COMP VDD 1446
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP		MCP BCLK VML COMP GND 1446
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP		MCP CPU COMP VCC 1446
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP		MCP CPU COMP GND 1446
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB		FSB CLK CPU P 1086 1483
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB		FSB CLK CPU N 1086 1483
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB		FSB CLK ITP P 1303 1443
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB		FSB CLK ITP N 1383 1443
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB		FSB CLK MCP P 1444
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB		FSB CLK MCP N 1444
CPU_IERR_L	CPU_50S			CPU_IERR L 1006
PM_DPSLPVPR	CPU_50S	CPU_AGTL		PM_DPSLPVPR 2107 6008
(See above)	CPU_50S	CPU_AGTL		IMVP6 DPSLPVPR 6007
CPU_GTLREF	CPU_50S	CPU_GTLREF		CPU_GTLREF 1084 2781
CPU_COMP	CPU_50S	CPU_COMP		CPU_COMP<3> 1083
CPU_COMP	CPU_27P4S	CPU_COMP		CPU_COMP<2> 1083
CPU_COMP	CPU_50S	CPU_COMP		CPU_COMP<1> 1083
CPU_COMP	CPU_27P4S	CPU_COMP		CPU_COMP<0> 1083
XDP_TDI	CPU_50S	CPU_ITP		XDP_TDI 606 1086 1006 1383
XDP_TDO	CPU_50S	CPU_ITP		XDP_TDO 604 1086 1006
XDP_TMS	CPU_50S	CPU_ITP		XDP_TMS 606 607 1086 1006 1383
XDP_TCK	CPU_50S	CPU_ITP		XDP_TCK 606 607 1086 1006 1386
XDP_TRST_L	CPU_50S	CPU_ITP		XDP_TRST L 606 607 1086 1006 1386
XDP_BPM_1	CPU_50S	CPU_ITP		XDP BPM L<4..0> 1006 1306
XDP_BPM_15	CPU_50S	CPU_ITP		XDP BPM L<5> 1005 1306
(FSB_CPURST_L)	CPU_50S	CPU_ITP		XDP_CPURST L 1384
	CPU_50S	CPU_BMT		CPU VID<6..0> 1186 6007
	CPU_50S	CPU_BMT		IMVP6 VID<6..0> 1186 6007
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_VCCSENSE P 1145 6045
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE		CPU_VCCSENSE N 1145 6045
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE		IMVP6_VSEN P
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE		IMVP6_VSEN N

CPU/FSB Constraints

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	SHT	OF	
	100	109	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
MEM_A_CLK	MEM_70D_VDD	MEM_CLK		MEM_A_CLK P<5..0> 1585 2805 2807
MEM_A_CLK	MEM_70D_VDD	MEM_CLK		MEM_A_CLK N<5..0> 1585 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL		MEM_A_CKE<3..0> 15A5 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL		MEM_A_CS L<3..0> 1585 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL		MEM_A_ODT<3..0> 15A5 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM_A A<14..0> 1585 1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM_A BA<2..0> 1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM_A RAS L 1505 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM_A CAS L 1505 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD		MEM_A WE L 1505 2807
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA		MEM_A DQ<7..0> 1587 2802 2804 2802 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA		MEM_A DQ<15..8> 1587 2802 2804
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA		MEM_A DQ<23..16> 1587 1507 2802 2804 2802 2804
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA		MEM_A DQ<31..24> 1507 2802 2804
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA		MEM_A DQ<39..32> 1507 2805 2807
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA		MEM_A DQ<47..40> 1507 2805 2807
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA		MEM_A DQ<55..48> 1507 2805 2807
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA		MEM_A DQ<63..56> 1507 2805 2807
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA		MEM_A DM<0> 15A7 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA		MEM_A DM<1> 15A7 2802
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA		MEM_A DM<2> 15A7 2804
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA		MEM_A DM<3> 15A7 2802
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA		MEM_A DM<4> 15A7 2805
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA		MEM_A DM<5> 1587 2807
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA		MEM_A DM<6> 1587 2805
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA		MEM_A DM<7> 1587 28A7
MEM_A_DQS0	MEM_70D	MEM_DQS		MEM_A DQS P<0> 1505 2802
MEM_A_DQS0	MEM_70D	MEM_DQS		MEM_A DQS N<0> 1505 2802
MEM_A_DQS1	MEM_70D	MEM_DQS		MEM_A DQS P<1> 1505 2804
MEM_A_DQS1	MEM_70D	MEM_DQS		MEM_A DQS N<1> 1505 2804
MEM_A_DQS2	MEM_70D	MEM_DQS		MEM_A DQS P<2> 1505 2802
MEM_A_DQS2	MEM_70D	MEM_DQS		MEM_A DQS N<2> 1505 2802
MEM_A_DQS3	MEM_70D	MEM_DQS		MEM_A DQS P<3> 1505 2804
MEM_A_DQS3	MEM_70D	MEM_DQS		MEM_A DQS N<3> 1505 2804
MEM_A_DQS4	MEM_70D	MEM_DQS		MEM_A DQS P<4> 1505 2807
MEM_A_DQS4	MEM_70D	MEM_DQS		MEM_A DQS N<4> 1505 2807
MEM_A_DQS5	MEM_70D	MEM_DQS		MEM_A DQS P<5> 1505 2805
MEM_A_DQS5	MEM_70D	MEM_DQS		MEM_A DQS N<5> 1505 2805
MEM_A_DQS6	MEM_70D	MEM_DQS		MEM_A DQS P<6> 1505 2807
MEM_A_DQS6	MEM_70D	MEM_DQS		MEM_A DQS N<6> 1505 2807
MEM_A_DQS7	MEM_70D	MEM_DQS		MEM_A DQS P<7> 1505 28A5
MEM_A_DQS7	MEM_70D	MEM_DQS		MEM_A DQS N<7> 1505 28A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK		MEM_B_CLK P<5..0> 1581 2905 2907
MEM_B_CLK	MEM_70D_VDD	MEM_CLK		MEM_B_CLK N<5..0> 1581 2905 2907
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL		MEM_B_CKE<3..0> 15A1 2905 2907
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL		MEM_B_CS L<3..0> 1581 2905 2907
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL		MEM_B_ODT<3..0> 15A1 2905
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM_B A<14..0> 1581 1501 2905 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM_B BA<2..0> 1501 2905 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM_B RAS L 1501 2905
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM_B CAS L 1501 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD		MEM_B WE L 1501 2907
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA		MEM_B DQ<7..0> 1583 2902 2904 2902 2904
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA		MEM_B DQ<15..8> 1583 2902 2904
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA		MEM_B DQ<23..16> 1583 1503 2902 2904
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA		MEM_B DQ<31..24> 1503 2902 2904 2902 2904
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA		MEM_B DQ<39..32> 1503 2905 2907
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA		MEM_B DQ<47..40> 1503 2905 2907
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA		MEM_B DQ<55..48> 1503 2905 2907
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA		MEM_B DQ<63..56> 1503 29A5 29A7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA		MEM_B DM<0> 15A3 2904
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA		MEM_B DM<1> 15A3 2902
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA		MEM_B DM<2> 15A3 2902
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA		MEM_B DM<3> 15A3 2904
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA		MEM_B DM<4> 15A3 2905
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA		MEM_B DM<5> 1583 2907
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA		MEM_B DM<6> 1583 2905
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA		MEM_B DM<7> 1583 29A7
MEM_B_DQS0	MEM_70D	MEM_DQS		MEM_B DQS P<0> 1501 2902
MEM_B_DQS0	MEM_70D	MEM_DQS		MEM_B DQS N<0> 1501 2902
MEM_B_DQS1	MEM_70D	MEM_DQS		MEM_B DQS P<1> 1501 2904
MEM_B_DQS1	MEM_70D	MEM_DQS		MEM_B DQS N<1> 1501 2904
MEM_B_DQS2	MEM_70D	MEM_DQS		MEM_B DQS P<2> 1501 2904
MEM_B_DQS2	MEM_70D	MEM_DQS		MEM_B DQS N<2> 1501 2904
MEM_B_DQS3	MEM_70D	MEM_DQS		MEM_B DQS P<3> 1501 2902
MEM_B_DQS3	MEM_70D	MEM_DQS		MEM_B DQS N<3> 1501 2902
MEM_B_DQS4	MEM_70D	MEM_DQS		MEM_B DQS P<4> 1501 2907
MEM_B_DQS4	MEM_70D	MEM_DQS		MEM_B DQS N<4> 1501 2907
MEM_B_DQS5	MEM_70D	MEM_DQS		MEM_B DQS P<5> 1501 2905
MEM_B_DQS5	MEM_70D	MEM_DQS		MEM_B DQS N<5> 1501 2905
MEM_B_DQS6	MEM_70D	MEM_DQS		MEM_B DQS P<6> 1501 2907
MEM_B_DQS6	MEM_70D	MEM_DQS		MEM_B DQS N<6> 1501 2907
MEM_B_DQS7	MEM_70D	MEM_DQS		MEM_B DQS P<7> 1501 29A5
MEM_B_DQS7	MEM_70D	MEM_DQS		MEM_B DQS N<7> 1501 29A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP		MCP_MEM_COMP_VDD 1606
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP		MCP_MEM_COMP_GND 1606

Memory Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

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	D	051-7537	A
SCALE	SHT	OF	
NONE	101	109	

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	*	=3X_DIELECTRIC	?
CLK_PCI_E	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4X_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_E	PCI_E_90D	PCI_E	PCI_E MINI R2D P	706 3107
	PCI_E_90D	PCI_E	PCI_E MINI R2D N	706 3107
	PCI_E_90D	PCI_E	PCI_E MINI R2D C P	1783 3105
	PCI_E_90D	PCI_E	PCI_E MINI R2D C N	1783 3105
	PCI_E_90D	PCI_E	PCI_E MINI D2R P	706 1786 3107
	PCI_E_90D	PCI_E	PCI_E MINI D2R N	706 1786 3107
	PCI_E_90D	PCI_E	PCI_E FC R2D P	3205
	PCI_E_90D	PCI_E	PCI_E FC R2D N	3205
	PCI_E_90D	PCI_E	PCI_E FC R2D C P	986 3206
	PCI_E_90D	PCI_E	PCI_E FC R2D C N	986 3206
	PCI_E_90D	PCI_E	PCI_E FC D2R P	986 3285
	PCI_E_90D	PCI_E	PCI_E FC D2R N	986 3285
MCP_PEX	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI P	1703 3105
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI N	1703 3105
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI CONN P	706 3108
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI CONN N	706 3108
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M FC P	986 3205
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M FC N	986 3205
MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6	
TMDS	DP_100D	DISPLAYPORT	TMDS IG TXC P	
	DP_100D	DISPLAYPORT	TMDS IG TXC N	
	DP_100D	DISPLAYPORT	TMDS IG TXD P<2..0>	
	DP_100D	DISPLAYPORT	TMDS IG TXD N<2..0>	
	DP_100D	DISPLAYPORT	DP ML P<3..0>	6701 68C1 68C8
	DP_100D	DISPLAYPORT	DP ML C P<3..0>	68C2 68C7
	DP_100D	DISPLAYPORT	DP ML N<3..0>	6701 68A1 68C1 68C8
	DP_100D	DISPLAYPORT	DP ML C N<3..0>	68B2 68C2 68C7
	DP_100D	DISPLAYPORT	DP IG AUX CH P	1886 6707
	DP_100D	DISPLAYPORT	DP IG AUX CH N	1886 6787
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	6706
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	6705
DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	6704 6808	
DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	6704 6888	
MCP_HDMI	MCP_DV_COMP	MCP_HDMI_RSET	18A6 25C7	
MCP_HDMI	MCP_DV_COMP	MCP_HDMI_VPROBE	18A6 25C7	
LVDS	LVDS	LVDS IG A CLK P	18B3 66B3	
LVDS	LVDS	LVDS IG A CLK F P	707 66B2	
LVDS	LVDS	LVDS IG A CLK N	18B3 66B3	
LVDS	LVDS	LVDS IG A CLK F N	707 66B2	
LVDS	LVDS	LVDS IG A DATA P<2..0>	707 18B3 66C2	
LVDS	LVDS	LVDS IG A DATA N<2..0>	707 18B3 66C2	
DP	DISPLAYPORT	DP ML CONN P<3..0>	68C3 68C4 68C5	
DP	DISPLAYPORT	DP ML CONN N<3..0>	68B3 68C3 68C4 68C5	
MCP_IFFAB	MCP_DV_COMP	MCP_IFFAB_RSET	18A3 2506	
MCP_IFFAB	MCP_DV_COMP	MCP_IFFAB_VPROBE	18A3 2506	
SATA	SATA	SATA HDD R2D C P	2006 36A3	
SATA	SATA	SATA HDD R2D C N	2006 36A3	
SATA	SATA	SATA HDD R2D P	705 36A7	
SATA	SATA	SATA HDD R2D N	705 36A7	
SATA	SATA	SATA HDD R2D UF P	36A5	
SATA	SATA	SATA HDD R2D UF N	36A5	
SATA	SATA	SATA HDD D2R P	2006 36A3	
SATA	SATA	SATA HDD D2R N	2006 36A3	
SATA	SATA	SATA HDD D2R C P	705 36A7	
SATA	SATA	SATA HDD D2R C N	705 36A7	
SATA	SATA	SATA HDD D2R UF P	36A5	
SATA	SATA	SATA HDD D2R UF N	36A5	
SATA	SATA	SATA ODD R2D C P	2006 36C2	
SATA	SATA	SATA ODD R2D C N	2006 36C2	
SATA	SATA	SATA ODD R2D P	787 36B5	
SATA	SATA	SATA ODD R2D N	787 705 36B5	
SATA	SATA	SATA ODD R2D UF P	36C4	
SATA	SATA	SATA ODD R2D UF N	36C4	
SATA	SATA	SATA ODD D2R P	2006 36B2	
SATA	SATA	SATA ODD D2R N	2006 36B2	
SATA	SATA	SATA ODD D2R C P	787 36B5	
SATA	SATA	SATA ODD D2R C N	787 36B5	
SATA	SATA	SATA ODD D2R UF P	36B4	
SATA	SATA	SATA ODD D2R UF N	36B4	
MCP_SATA	SATA_TERM	MCP_SATA_TERM	20A6	

MCP Constraints 1
 SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	102	109

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HDA Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING	
MCP_DEBUG	PCI_55S	PCI		MCP_DEBUG<7..0> 1303 1907
PCI_AD	PCI_55S	PCI		PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI		PCI_AD<24>
PCI_AD	PCI_55S	PCI		PCI_AD<31..25>
PCI_AD	PCI_55S	PCI		PCI_PAR
PCI_C_BE_L	PCI_55S	PCI		PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI		PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI		PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI		PCI_PERR_L
PCI_CNTL	PCI_55S	PCI		PCI_SERR_L
PCI_CNTL	PCI_55S	PCI		PCI_STOP_L
PCI_CNTL	PCI_55S	PCI		PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI		PCI_FRAME_L
PCI_BE00_I	PCI_55S	PCI		PCI_BE00_I 1902 1907
PCI_GNT0_L	PCI_55S	PCI		PCI_GNT0_L
PCI_BE01_I	PCI_55S	PCI		PCI_BE01_I 1902 1907
PCI_GNT1_L	PCI_55S	PCI		PCI_GNT1_L
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_L
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_L
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_L
PCI_INTX_I	PCI_55S	PCI		PCI_INTX_L
PCI_CLK33M_MCP_R	CLK_PCI_55S	CLK_PCI		PCI_CLK33M_MCP_R 1905
PCI_CLK33M_MCP	CLK_PCI_55S	CLK_PCI		PCI_CLK33M_MCP 1905
LPC_AD	LPC_55S	LPC		LPC_AD<3..0>
LPC_FRAME_L	LPC_55S	LPC		LPC_FRAME_L 1983 3908 41D3 41D5
LPC_RESET_L	LPC_55S	LPC		LPC_RESET_L 1983 3908 41D5
LPC_RESET_L	LPC_55S	LPC		LPC_RESET_L 1983 2604
LPC_CLK33M_SMC_R	CLK_LPC_55S	CLK_LPC		LPC_CLK33M_SMC_R 1983 2604
LPC_CLK33M_SMC	CLK_LPC_55S	CLK_LPC		LPC_CLK33M_SMC 2601 3908
LPC_CLK33M_LPCPLUS	CLK_LPC_55S	CLK_LPC		LPC_CLK33M_LPCPLUS 2681 41D3
USB_EXTN_P	USB_90D	USB		USB_EXTN_P 2003 37A8
USB_EXTN_N	USB_90D	USB		USB_EXTN_N 2003 37A8
USB_EXTN_MUXED_P	USB_90D	USB		USB_EXTN_MUXED_P 3704
USB_EXTN_MUXED_N	USB_90D	USB		USB_EXTN_MUXED_N 3704
CONN_USB_EXTN_P	USB_90D	USB		CONN_USB_EXTN_P 3703
CONN_USB_EXTN_N	USB_90D	USB		CONN_USB_EXTN_N 3703
USB_CAMERA_P	USB_90D	USB		USB_CAMERA_P 2003 3185
USB_CAMERA_N	USB_90D	USB		USB_CAMERA_N 2003 3185
USB_CAMERA_CONN_P	USB_90D	USB		USB_CAMERA_CONN_P 705 3187
USB_CAMERA_CONN_N	USB_90D	USB		USB_CAMERA_CONN_N 705 3187
USB_BT_P	USB_90D	USB		USB_BT_P 2003 3188
USB_BT_N	USB_90D	USB		USB_BT_N 2003 3188
CONN_USB2_BT_P	USB_90D	USB		CONN_USB2_BT_P 705 3187
CONN_USB2_BT_N	USB_90D	USB		CONN_USB2_BT_N 705 3187
USB_TPAD_P	USB_90D	USB		USB_TPAD_P 2003 4788
USB_TPAD_N	USB_90D	USB		USB_TPAD_N 2003 4788
USB_TPAD_R_P	USB_90D	USB		USB_TPAD_R_P 4787
USB_TPAD_R_N	USB_90D	USB		USB_TPAD_R_N 4787
USB_IR_P	USB_90D	USB		USB_IR_P 2003 3807
USB_IR_N	USB_90D	USB		USB_IR_N 2003 3807
USB_EXTB_P	USB_90D	USB		USB_EXTB_P 2003 37A4
USB_EXTB_N	USB_90D	USB		USB_EXTB_N 2003 37A4
CONN_USB_EXTB_P	USB_90D	USB		CONN_USB_EXTB_P 37A3
CONN_USB_EXTB_N	USB_90D	USB		CONN_USB_EXTB_N 37A3
MCP_USB_BIAS	MCP_USB_BIAS			MCP_USB_BIAS_GND 2084
SMBUS_MCP_0_CLK	SMB_55S	SMB		SMBUS_MCP_0_CLK 1386 21C3 42D8
SMBUS_MCP_0_DATA	SMB_55S	SMB		SMBUS_MCP_0_DATA 1386 21C3 42D8
SMBUS_MCP_1_CLK	SMB_55S	SMB		SMBUS_MCP_1_CLK 21C3 42C8
SMBUS_MCP_1_DATA	SMB_55S	SMB		SMBUS_MCP_1_DATA 21C3 42C8
HDA_BIT_CLK	HDA_55S	HDA		HDA_BIT_CLK 2102 5107
HDA_BIT_CLK_R	HDA_55S	HDA		HDA_BIT_CLK_R 21A7 21D4
HDA_SYNC	HDA_55S	HDA		HDA_SYNC 2102 5107
HDA_SYNC_R	HDA_55S	HDA		HDA_SYNC_R 21A7 21D4
HDA_RST_I	HDA_55S	HDA		HDA_RST_I 21A7 21D4
HDA_RST_L	HDA_55S	HDA		HDA_RST_L 2102 5107
HDA_SDIN	HDA_55S	HDA		HDA_SDIN 2107 5107
HDA_SDIN_CODEC	HDA_55S	HDA		HDA_SDIN_CODEC 2102 5107
HDA_SDOUT	HDA_55S	HDA		HDA_SDOUT 21A7 21D4
HDA_SDOUT_R	HDA_55S	HDA		HDA_SDOUT_R 21A7 21D4
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP			MCP_HDA_PULLDN_COMP 2107
PM_CLK32K_SUSCLK_R	CLK_SLOW_55S	CLK_SLOW		PM_CLK32K_SUSCLK_R 2183 2684
PM_CLK32K_SUSCLK	CLK_SLOW_55S	CLK_SLOW		PM_CLK32K_SUSCLK 2681 3905
SPI_CLK_R	SPI_55S	SPI		SPI_CLK_R 2183 41A5 41C8
SPI_CLK	SPI_55S	SPI		SPI_CLK 41A1 5005
SPI_ALT_CLK	SPI_55S	SPI		SPI_ALT_CLK 4105 41D3
SPI_MOSI_R	SPI_55S	SPI		SPI_MOSI_R 2183 41A5 41C7
SPI_MOSI	SPI_55S	SPI		SPI_MOSI 41A1 5004
SPI_MISO	SPI_55S	SPI		SPI_MISO 2183 41A5 41B7
SPI_MISO_R	SPI_55S	SPI		SPI_MISO_R 5004
SPI_ALT_MISO	SPI_55S	SPI		SPI_ALT_MISO 4185 41D5
SPI_CS0_R_L	SPI_55S	SPI		SPI_CS0_R_L 2183 41B7
SPI_CS0_L	SPI_55S	SPI		SPI_CS0_L
SPI_CS1_R_L	SPI_55S	SPI		SPI_CS1_R_L
SPI_CS1_R_L_USE_MLB	SPI_55S	SPI		SPI_CS1_R_L_USE_MLB 4182

MCP Constraints 2

SYNC_MASTER=T18_MLB SYNC_DATE=12/14/2007

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		MCP MII COMP VDD	MCP MII COMP GND	MCP CLK25M BUF0 R	RTL8211 CLK25M CKXTAL1
	PHYSICAL	SPACING				
MCP_MII_COMP	MCP_MII_COMP					
MCP_MII_COMP	MCP_MII_COMP					
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK				
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK				
ENET_INTR_L	ENET_MII_55S	ENET_MII				
ENET_INTR_L	ENET_MII_55S	ENET_MII				
ENET_MDIO	ENET_MII_55S	ENET_MII				
ENET_MDIO	ENET_MII_55S	ENET_MII				
ENET_MDC	ENET_MII_55S	ENET_MII				
ENET_MDC	ENET_MII_55S	ENET_MII				
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII				
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII				
ENET_CLK125M_RXCLK_R	ENET_MII_55S	ENET_MII				
ENET_CLK125M_RXCLK_R	ENET_MII_55S	ENET_MII				
ENET_RXD_R<3..0>	ENET_MII_55S	ENET_MII				
ENET_RXD_R<3..0>	ENET_MII_55S	ENET_MII				
ENET_RXD<0>	ENET_MII_55S	ENET_MII				
ENET_RXD<0>	ENET_MII_55S	ENET_MII				
ENET_RXD<3..3>	ENET_MII_55S	ENET_MII				
ENET_RXD<3..3>	ENET_MII_55S	ENET_MII				
ENET_RX_CTRL	ENET_MII_55S	ENET_MII				
ENET_RX_CTRL	ENET_MII_55S	ENET_MII				
ENET_RXCTL_R	ENET_MII_55S	ENET_MII				
ENET_RXCTL_R	ENET_MII_55S	ENET_MII				
ENET_CLK125M_TXCLK_R	ENET_MII_55S	ENET_MII				
ENET_CLK125M_TXCLK_R	ENET_MII_55S	ENET_MII				
ENET_TXD<0>	ENET_MII_55S	ENET_MII				
ENET_TXD<0>	ENET_MII_55S	ENET_MII				
ENET_TXD<3..3>	ENET_MII_55S	ENET_MII				
ENET_TXD<3..3>	ENET_MII_55S	ENET_MII				
ENET_TX_CTRL	ENET_MII_55S	ENET_MII				
ENET_TX_CTRL	ENET_MII_55S	ENET_MII				
ENET_RESET_L	ENET_MII_55S	ENET_MII				
ENET_RESET_L	ENET_MII_55S	ENET_MII				
ENET_MDI_P<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_P<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_N<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_N<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_TRAN_P<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_TRAN_P<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_TRAN_N<3..0>	ENET_MDI_100D	ENET_MDI				
ENET_MDI_TRAN_N<3..0>	ENET_MDI_100D	ENET_MDI				

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Ethernet Constraints	
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NONE		104	109

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 55G	SMB	SMBUS_SMC_A_S3_SCL	785 7D5 42D2
SMBUS_SMC_A_S3_SDA	SMB 55G	SMB	SMBUS_SMC_A_S3_SDA	785 7C5 42D2
SMBUS_SMC_B_S0_SCL	SMB 55G	SMB	SMBUS_SMC_B_S0_SCL	42C2
SMBUS_SMC_B_S0_SDA	SMB 55G	SMB	SMBUS_SMC_B_S0_SDA	42D2
SMBUS_SMC_O_S0_SCL	SMB 55G	SMB	SMBUS_SMC_O_S0_SCL	42D5
SMBUS_SMC_O_S0_SDA	SMB 55G	SMB	SMBUS_SMC_O_S0_SDA	42D5
SMBUS_SMC_BSA_SCL	SMB 55G	SMB	SMBUS_SMC_BSA_SCL	7A7 42C5
SMBUS_SMC_BSA_SDA	SMB 55G	SMB	SMBUS_SMC_BSA_SDA	42C5
SMBUS_SMC_MGMT_SCL	SMB 55G	SMB	SMBUS_SMC_MGMT_SCL	42B5
SMBUS_SMC_MGMT_SDA	SMB 55G	SMB	SMBUS_SMC_MGMT_SDA	42B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	
			CHGR_CSI_N	
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	
			CHGR_CSO_N	

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

M97 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DIFFPAIR	CHGR_CSO_R_P		44A8	5783
DIFFPAIR	CHGR_CSO_R_N		44A8	5783
DIFFPAIR	CPUTHMSNS_D2_P		4505	
DIFFPAIR	CPUTHMSNS_D2_N		4505	
DIFFPAIR	CPU_THERMD_P		10C6	4505
DIFFPAIR	CPU_THERMD_N		10C6	4505
DIFFPAIR	ISNS_CPUVTT_P		44B7	
DIFFPAIR	ISNS_CPUVTT_N		44B7	
DIFFPAIR	ISNS_P1VSS0MCP_P		44C7	
DIFFPAIR	ISNS_P1VSS0MCP_N		44C7	
DIFFPAIR	ISNS_PVCORES0MCP_P		44D8	
DIFFPAIR	ISNS_PVCORES0MCP_N		44D8	61C4
DIFFPAIR	MCP_THMSNS_D2_P		7C7	45B5
DIFFPAIR	MCP_THMSNS_D2_N		7C7	45B5
DIFFPAIR	MCP_THMDIODE_P		21C3	45C5
DIFFPAIR	MCP_THMDIODE_N		21C3	45B5

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M97 SPECIAL CONSTRAINTS

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M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA_P1MM				MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM				
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM				
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM				
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
27F4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM				
27F4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM	
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM	
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM	
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM	
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM	
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM	
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

M97 RULE DEFINITIONS

SYNC_MASTER=M97_MLB

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