

# SANTANA - M51 MLB

DVT -- 06/29/06

| REV | ZONE | ECN    | DESCRIPTION OF CHANGE | CK APPD  | ENG APPD |
|-----|------|--------|-----------------------|----------|----------|
| 21  |      | 446951 | ENGINEERING RELEASED  |          |          |
|     |      |        |                       | DATE     | DATE     |
|     |      |        |                       | 06/29/06 | 06/22/04 |

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| PDF | CSA | CONTENTS                  | MASTER            | DATE       |
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| 8   | 8   | CPU 2 OF 2-PWR/GND        | M50_HENRY         | 06/29/2006 |
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| PDF | CSA | CONTENTS                  | MASTER            | DATE       |
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## Schematic / PCB #'s

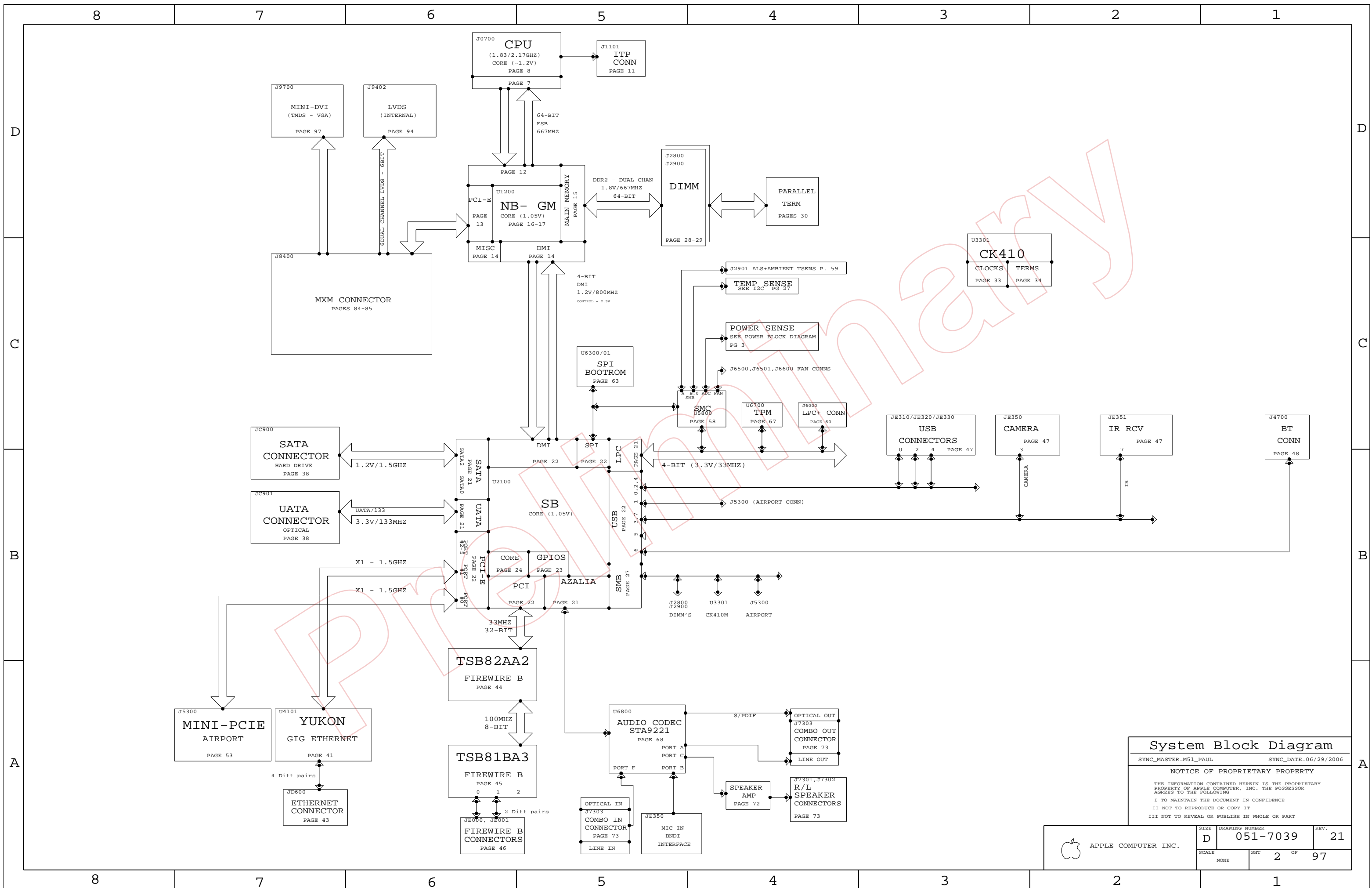
| PART#    | QTY | DESCRIPTION          | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------------|-------------------------|----------|------------|
| 051-7039 | 1   | PCB, SCHEM, MLB, M51 | SCH1                    |          |            |
| 820-1984 | 1   | PCB, FAB, MLB, M51   | MLB1                    |          |            |



|                               |  |                                     |           |   |                |
|-------------------------------|--|-------------------------------------|-----------|---|----------------|
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| x.xx : _____                  |  | ENG APPD                            | MFG APPD  |   |                |
| x.xxx : _____                 |  | QA APPD                             | DESIGNER  |   |                |
| ANGLES : _____                |  | RELEASE                             | SCALE     |   |                |
| DO NOT SCALE DRAWING          |  | NONE                                |           | TITLE   |                |
| THIRD ANGLE PROJECTION        |  | MATERIAL/FINISH NOTED AS APPLICABLE |           | SIZE D  | DRAWING NUMBER |
|                               |  |                                     |           | 820-1984  | REV. 21        |
|                               |  |                                     |           | SHT 1 OF 97   |                |

D  
C  
B  
A

D  
C  
B  
A



### System Block Diagram

SYNC\_MASTER=M51\_PAUL SYNC\_DATE=06/29/2006

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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | OF             |      |
| NONE                | 2    | 97             |      |



Production BOM

| BOM NUMBER | BOM NAME             | BOM OPTIONS                              |
|------------|----------------------|--|
| 630-7512   | PCBA,MLB,2.33GHz,M51 | M51_COMMON,M51_BEST,EEE_V4K              |
| 630-7595   | PCBA,MLB,2.16GHz,M51 | M51_COMMON,M51_BETTER,EEE_VMD,PRODUCTION |

Development BOM

| BOM NUMBER | BOM NAME        | BOM OPTIONS     |
|------------|-----------------|-----------------|
| 603-8960   | PCBA,DEVBOM,M51 | M51_DEVELOPMENT |

BOMOPTION Groups

| BOM GROUP       | BOM OPTIONS  |
|-----------------|--|
| M51_COMMON      | COMMON,M51_COMMON1,M51_COMMON2,ALTERNATE                               |
| M51_COMMON1     | CPU_TSSENS_EXT,GPU_TSSENS_INT,GPU_TSSENS_EXT,MXM_ROM,NBCFG_PEG_REVERSE |
| M51_COMMON2     | SB_SYSRST_4_PVT,ITP,MEROM,AMB_TSSENS,CPU_PWR_SENSE,MXM_PWR_SENSE       |
| M51_DEVELOPMENT | DEVELOPMENT,M51_DEV1   |
| M51_DEV1        | CPU_TSSENS_INT,SYS_PWR_SENSE   |

MEROM BOM OPTION DUE TO PAGE 76 SHARING W/ M50

BarCode Label / EEE #'s

| PART NUMBER | QTY | DESCRIPTION              | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--------------------------|---------------|----------|------------|
| 825-6447    | 1   | BAR CODE LABEL, MLB, M51 | [EEE:VMD]     | CRITICAL | EEE_VMD    |
| 825-6447    | 1   | BAR CODE LABEL, MLB, M51 | [EEE:V4K]     | CRITICAL | EEE_V4K    |

Module Parts

| PART NUMBER | QTY | DESCRIPTION                             | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---|---------------|----------|------------|
| 511S0025    | 1   | IC,CPU-SKT,479BGA                       | J0700         | CRITICAL |            |
| 338S0328    | 1   | IC,945PM,NORTHBRIDGE                    | U1200         | CRITICAL |            |
| 343S0385    | 1   | IC,SB,652BGA                            | U2100         | CRITICAL |            |
| 359S0101    | 1   | IC,CY28445-5,CLK GEN,68PIN QFN          | U3301         | CRITICAL |            |
| 338S0270    | 1   | IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO | U4101         | CRITICAL |            |
| 341S1797    | 1   | IC,ENET LAN ROM                         | U4102         | CRITICAL |            |
| 341S1789    | 1   | IC,TPM,TSSOP,28P                        | U6700         | CRITICAL | TPM        |
| 353S1465    | 1   | IC,CPU VREG,IMVP,TWO PHASE,SCREENED     | U7500         | CRITICAL |            |
| 341S1892    | 1   | IC,2K I2C EEPROM,MXM,M51                | U8570         | CRITICAL | MXM_ROM    |

| PART NUMBER | QTY | DESCRIPTION         | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------|---------------|----------|------------|
| 341T0019    | 1   | IC,EFI BOOT ROM,M51 | U6301         | CRITICAL |            |
| 341T0020    | 1   | IC,SMC,M51          | U5800         | CRITICAL |            |
| 337S3292    | 1   | MEROM 2.3GHZ, M51   | CPU           | CRITICAL | M51_BEST   |
| 337S3293    | 1   | MEROM 2.16GHZ, M51  | CPU           | CRITICAL | M51_BETTER |

Misc. Parts

| PART NUMBER | QTY | DESCRIPTION                 | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-----------------------------|---------------|----------|------------|
| 742-0048    | 1   | BAT,COIN,3V,220MAH,CR2032   | BT2600        | CRITICAL | NOSTUFF    |
| 820-2038    | 1   | IO ALIGNMENT BOARD, M51     | PCB2          | CRITICAL |            |
| 946-0743    | 1   | IO ALIGNMENT BOARD ADHESIVE | ADH1          | CRITICAL |            |

BATTERY IS INSTALLED AT FATP

FOR DVT, TRYING AN EVEN BRIGHTER LED ON 2.16GHZ CONFIG

| PART NUMBER | QTY | DESCRIPTION                | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|----------------------------|---------------|----------|------------|
| 378S0199    | 1   | LED,WHITE,DUAL,2500MCD,SMD | LED5950       | CRITICAL | M51_BETTER |
| 378S0193    | 1   | LED,WHITE,740MCD,LF,3X2MM  | LED5950       | CRITICAL | M51_BEST   |

Alternate Parts

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:           |
|-------------|---------------------------|------------|---------|---------------------|
| 126S0086    | 126S0078                  |            | ALL     | Sanyo alt for Nich. |
| 126S0099    | 126S0073                  |            | ALL     | Sanyo alt for Nich. |
| 126S0068    | 126S0088                  |            | ALL     | Sanyo alt for Nich. |
| 124-0361    | 124-0339                  |            | ALL     | SANYO ALT           |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:            |
|-------------|---------------------------|------------|---------|----------------------|
| 378S0141    | 378S0140                  |            | ALL     | GREEN LED ALT.       |
| 359S0117    | 359S0101                  |            | U3301   | SILEGO CK410 CLOCK   |
| 353S1461    | 353S1465                  |            | U7500   | CPU VREG NEW REV     |
| 740S0044    | 740S0028                  |            | F9710   | DVI DDC (LITTLEFUSE) |
| 516S0511    | 516S0460                  |            | J8400   | MXM CONN SPEEDTECH   |

SENSOR STUFFING OPTIONS

MUST STUFF WHEN SYS\_PWR\_SENSE IS NOT STUFFED (I.E. WHEN DEVELOPMENT BOM IS NOT STUFFED)

| PART#    | QTY | DESCRIPTION         | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|---------------------|-------------------------|------------|
| 102S0699 | 1   | RES,0-OHM,2010      | R7650                   | PRODUCTION |
| 116S0090 | 1   | RES,10K-OHM,54,0402 | C7650                   | PRODUCTION |
| 116S0090 | 1   | RES,10K-OHM,54,0402 | C7650                   | PRODUCTION |

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN MXM\_PWR\_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

| PART#    | QTY | DESCRIPTION         | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|---------------------|-------------------------|------------|
| 107S0070 | 1   | RES,0-OHM,2512      | R8450                   | NOSTUFF    |
| 116S0090 | 1   | RES,10K-OHM,54,0402 | C8458                   | NOSTUFF    |
| 116S0090 | 1   | RES,10K-OHM,54,0402 | C8459                   | NOSTUFF    |

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

MUST STUFF WHEN CPU\_PWR\_SENSE IS NOT STUFFED (IF THIS MOVES TO DEV BOM)

| PART#    | QTY | DESCRIPTION         | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|---------------------|-------------------------|------------|
| 116S0090 | 1   | RES,10K-OHM,54,0402 | C7602                   | NOSTUFF    |
| 116S0090 | 1   | RES,10K-OHM,54,0402 | C7612                   | NOSTUFF    |

PULL-DOWNS FOR UNUSED PINS WHEN DEVELOPMENT SENSORS ARE GONE

BOM Config

SYNC\_MASTER=M51\_DAVE SYNC\_DATE=(MASTER)

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|                     | NONE  | D 051-7039     | 21   |
|                     | SHT   | OF             |      |
|                     | 4     | 97             |      |

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1

LAYOUT: PLACE CLOSE TO DESTINATION  
\* OPPOSITE END FROM CLOCK BUFFER

FSB SIGNALS

34 21 SB\_CLK100M\_SATA\_P PP6C4 OMIT P4MM  
34 21 SB\_CLK100M\_SATA\_N PP6C5 OMIT P4MM

34 21 SB\_CLK14P3M\_TIMER PP6D9 OMIT P4MM  
34 23 SB\_CLK48M\_USBCTLR PP6E0 OMIT P4MM

34 22 PCI\_CLK\_SB PP6D0 OMIT P4MM  
44 34 PCI\_CLK\_FW PP626 OMIT P4MM  
58 34 PCI\_CLK\_SMC PP627 OMIT P4MM

LAYOUT NOTE: PLACE NEAR SOUTHBRIDGE

38 21 IDE\_PDIO\_L PP6C6 OMIT P4MM  
38 21 IDE\_PDIO\_RY PP6C7 OMIT P4MM  
38 21 IDE\_PDD<9> PP6C8 OMIT P4MM

54 22 PCIE\_B\_D2R\_P PP600 OMIT P4MM  
54 22 PCIE\_B\_D2R\_N PP601 OMIT P4MM  
22 14 DMI\_N2S\_P<0> PP6D3 OMIT P4MM  
22 14 DMI\_N2S\_N<0> PP6D4 OMIT P4MM

67 60 58 21 5 LPC\_FRAME\_L PP6D8 OMIT P4MM  
63 58 22 SPI\_S0 PP612 OMIT P4MM  
63 58 22 SPI\_S1 PP613 OMIT P4MM

ALL I2C BUSSES (PLACE IN ACCESSIBLE LOCATION TOP SIDE)

27 SMBUS\_SB\_SCL PP604 OMIT P4MM  
27 SMBUS\_SB\_SDA PP605 OMIT P4MM

27 SMBUS\_SMC\_A\_S3\_SCL PP610 OMIT P4MM  
27 SMBUS\_SMC\_A\_S3\_SDA PP611 OMIT P4MM

12 11 7 FSB\_CPURST\_L PP621 OMIT P4MM

LAYOUT NOTE: PLACE NEAR NORTHBRIDGE

75 26 14 5 VR\_PWRGOOD\_DELAY PP665 OMIT P4MM  
14 NB\_RST\_IN\_L\_R PP666 OMIT P4MM

22 14 DMI\_S2N\_N<0> PP673 OMIT P4MM  
22 14 DMI\_S2N\_P<0> PP674 OMIT P4MM  
19 14 MEM\_VREF\_NB\_0 PP6E1 OMIT P4MM  
19 14 MEM\_VREF\_NB\_1 PP675 OMIT P4MM

14 NB\_CFG<17> I473 NC\_NB\_CFG<17> MAKE\_BASE=TRUE  
14 NB\_CFG<15> I474 NC\_NB\_CFG<15> MAKE\_BASE=TRUE  
14 NB\_CFG<14> I475 NC\_NB\_CFG<14> MAKE\_BASE=TRUE  
14 NB\_CFG<13> I476 NC\_NB\_CFG<13> MAKE\_BASE=TRUE  
14 NB\_CFG<12> I477 NC\_NB\_CFG<12> MAKE\_BASE=TRUE  
14 NB\_CFG<11> I478 NC\_NB\_CFG<11> MAKE\_BASE=TRUE  
14 NB\_CFG<10> I479 NC\_NB\_CFG<10> MAKE\_BASE=TRUE  
14 NB\_CFG<8> I480 NC\_NB\_CFG<8> MAKE\_BASE=TRUE  
14 NB\_CFG<6> I482 NC\_NB\_CFG<6> MAKE\_BASE=TRUE  
14 NB\_CFG<4> I483 NC\_NB\_CFG<4> MAKE\_BASE=TRUE  
14 NB\_CFG<3> I484 NC\_NB\_CFG<3> MAKE\_BASE=TRUE

22 PCI\_GNT3\_L I513 TP\_PCI\_GNT3\_L MAKE\_BASE=TRUE

SPARE USB PORT  
22 USB\_F\_N TP\_USB\_F\_N MAKE\_BASE=TRUE  
22 USB\_F\_P TP\_USB\_F\_P MAKE\_BASE=TRUE

INVERTER DOES NOT USE THIS SIGNAL  
19 LVDS\_BKLTEN TP\_LVDS\_BKLTEN MAKE\_BASE=TRUE

64 NC\_AUD\_BI\_PORT\_G\_L NO\_TEST=TRUE  
64 NC\_AUD\_VREF\_PORT\_C NO\_TEST=TRUE  
64 NC\_AUD\_VREF\_PORT\_D NO\_TEST=TRUE  
64 NC\_SMC\_BATT\_CHG\_EN NO\_TEST=TRUE  
64 NC\_SMC\_BATT\_ISET NO\_TEST=TRUE  
64 NC\_SMC\_BATT\_TRICKLE\_EN\_L NO\_TEST=TRUE  
64 NC\_SMC\_BATT\_VSET NO\_TEST=TRUE  
64 NC\_SMC\_P20 NO\_TEST=TRUE  
64 NC\_SMC\_P21 NO\_TEST=TRUE  
64 NC\_SMC\_P22 NO\_TEST=TRUE  
64 NC\_SMC\_P23 NO\_TEST=TRUE  
64 NC\_SMC\_P26 NO\_TEST=TRUE  
64 NC\_SMC\_P27 NO\_TEST=TRUE  
64 NC\_SMC\_SYS\_ISET NO\_TEST=TRUE  
64 NC\_SMC\_SYS\_VSET NO\_TEST=TRUE  
64 NC\_SMS\_X\_AXIS NO\_TEST=TRUE  
64 NC\_SMS\_Y\_AXIS NO\_TEST=TRUE  
64 NC\_SMS\_Z\_AXIS NO\_TEST=TRUE

64 13 PEG\_R2D\_C\_N<0> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<0> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<1> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<1> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<2> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<2> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<3> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<3> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<4> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<4> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<5> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<5> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<6> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<6> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<7> NO\_TEST=TRUE  
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64 13 PEG\_R2D\_C\_N<8> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<8> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<9> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<9> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<10> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<10> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<11> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<11> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<12> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<12> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<13> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<13> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<14> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<14> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_N<15> NO\_TEST=TRUE  
64 13 PEG\_R2D\_C\_P<15> NO\_TEST=TRUE

73 NC\_J7302\_3 NO\_TEST=TRUE  
73 NC\_J7302\_6 NO\_TEST=TRUE  
68 NC\_AUD\_BI\_PORT\_E\_L NO\_TEST=TRUE  
68 NC\_AUD\_BI\_PORT\_E\_R NO\_TEST=TRUE  
68 NC\_SMC\_MEM\_ISENSE NO\_TEST=TRUE  
68 NC\_AUD\_BI\_PORT\_H\_L NO\_TEST=TRUE  
68 NC\_AUD\_BI\_PORT\_H\_R NO\_TEST=TRUE  
68 NC\_AUD\_VREF\_PORT\_B NO\_TEST=TRUE

29 TP\_MEM\_B\_A<15> NO\_TEST=TRUE  
29 TP\_MEM\_B\_A<14> NO\_TEST=TRUE

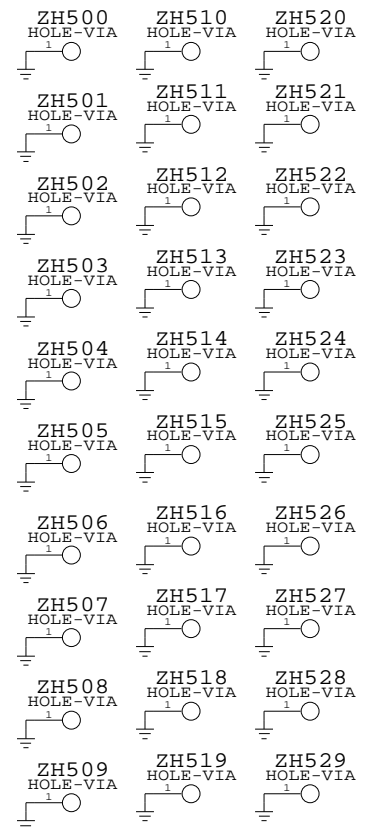
64 13 PEG\_R2D\_N<0> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<0> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<1> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<1> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<2> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<2> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<3> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<3> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<4> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<4> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<5> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<5> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<6> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<6> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<7> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<7> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<8> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<8> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<9> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<9> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<10> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<10> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<11> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<11> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<12> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<12> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<13> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<13> NO\_TEST=TRUE  
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64 13 PEG\_R2D\_P<14> NO\_TEST=TRUE  
64 13 PEG\_R2D\_N<15> NO\_TEST=TRUE  
64 13 PEG\_R2D\_P<15> NO\_TEST=TRUE

76 75 3 PPVOCORE\_CPU FUNC\_TEST=TRUE  
80 79 78 77 76 66 65 26 6 5 83 PP3V3\_S5 FUNC\_TEST=TRUE  
83 78 1 PP2V5\_S5 FUNC\_TEST=TRUE  
79 1 PP1V8\_S3 FUNC\_TEST=TRUE  
80 3 PP1V2\_S3 FUNC\_TEST=TRUE  
80 3 PP1V5\_S0 FUNC\_TEST=TRUE  
80 34 3 PP1V05\_S0 FUNC\_TEST=TRUE  
83 82 80 79 78 77 75 59 5 3 PP5V\_S5 FUNC\_TEST=TRUE  
97 83 75 59 3 PP5V\_S0 FUNC\_TEST=TRUE  
83 82 80 79 78 77 75 59 5 3 PP5V\_S5 FUNC\_TEST=TRUE  
80 79 78 77 76 66 65 26 6 5 83 PP3V3\_S5 FUNC\_TEST=TRUE  
84 83 76 41 27 26 10 6 3 PP3V3\_S0 FUNC\_TEST=TRUE  
83 1 PP24V\_S0 FUNC\_TEST=TRUE

11 7 XDP\_BPM\_L<3> FUNC\_TEST=TRUE  
11 7 XDP\_BPM\_L<2> FUNC\_TEST=TRUE  
11 7 XDP\_BPM\_L<1> FUNC\_TEST=TRUE  
11 7 XDP\_BPM\_L<0> FUNC\_TEST=TRUE  
26 11 7 XDP\_DRRSTBT\_L FUNC\_TEST=TRUE  
26 5 SW\_RST\_BTN\_L FUNC\_TEST=TRUE  
59 5 POWER\_BUTTON\_L FUNC\_TEST=TRUE  
67 60 58 21 LPC\_AD<0> FUNC\_TEST=TRUE  
67 60 58 21 LPC\_AD<1> FUNC\_TEST=TRUE  
67 60 58 21 LPC\_AD<2> FUNC\_TEST=TRUE  
67 60 58 21 LPC\_AD<3> FUNC\_TEST=TRUE  
67 60 58 21 LPC\_FRAME\_L FUNC\_TEST=TRUE  
67 60 58 21 PM\_CLKRUN\_L FUNC\_TEST=TRUE  
60 58 22 BOOT\_LPC\_SPI\_L FUNC\_TEST=TRUE  
60 6 DEBUG\_RST\_L FUNC\_TEST=TRUE  
60 59 21 FWH\_INIT\_L FUNC\_TEST=TRUE  
60 34 PCI\_CLK\_PORT80 FUNC\_TEST=TRUE  
67 60 58 23 INT\_SERIRQ FUNC\_TEST=TRUE  
67 60 58 23 PM\_SUS\_STAT\_L FUNC\_TEST=TRUE  
60 58 SMC\_MD1 FUNC\_TEST=TRUE  
60 58 SMC\_RST\_L FUNC\_TEST=TRUE  
60 58 SMC\_NMI FUNC\_TEST=TRUE  
60 23 SV\_SETUP\_FUNC\_TEST=TRUE  
76 58 ISENSE\_CAL\_EN FUNC\_TEST=TRUE  
94 85 INV\_ENABLE\_BL FUNC\_TEST=TRUE  
94 LCD\_PWM FUNC\_TEST=TRUE  
75 8 CPU\_VID<0> FUNC\_TEST=TRUE  
75 8 CPU\_VID<1> FUNC\_TEST=TRUE  
75 8 CPU\_VID<2> FUNC\_TEST=TRUE  
75 8 CPU\_VID<3> FUNC\_TEST=TRUE  
75 8 CPU\_VID<4> FUNC\_TEST=TRUE  
75 8 CPU\_VID<5> FUNC\_TEST=TRUE  
75 8 CPU\_VID<6> FUNC\_TEST=TRUE  
75 21 4 PM\_DPRS\_L\_PVR FUNC\_TEST=TRUE  
75 21 4 CPU\_DPRST\_L\_FUNC\_TEST=TRUE  
75 21 7 VR\_PWRGOOD\_DELAY\_FUNC\_TEST=TRUE  
76 26 14 5 VR\_PWRGD\_CK410\_FUNC\_TEST=TRUE  
84 77 58 26 ALL\_SYS\_PWRGD\_FUNC\_TEST=TRUE  
77 58 23 PM\_SLP\_S4\_L\_FUNC\_TEST=TRUE  
80 79 77 58 23 PM\_SLP\_S3\_L\_FUNC\_TEST=TRUE

60 59 58 SMC\_TCK FUNC\_TEST=TRUE  
60 59 58 SMC\_TDI FUNC\_TEST=TRUE  
60 59 58 SMC\_TDO FUNC\_TEST=TRUE  
60 59 58 SMC\_TMS FUNC\_TEST=TRUE  
60 58 SMC\_TRST\_L FUNC\_TEST=TRUE  
60 59 58 SMC\_TX\_L FUNC\_TEST=TRUE  
60 59 58 SMC\_RX\_L FUNC\_TEST=TRUE  
58 SMC\_MANUAL\_RST\_L FUNC\_TEST=TRUE  
11 XDP\_TCK FUNC\_TEST=TRUE  
11 XDP\_TDI FUNC\_TEST=TRUE  
11 XDP\_TDO FUNC\_TEST=TRUE  
11 XDP\_TMS FUNC\_TEST=TRUE  
11 XDP\_TRST\_L FUNC\_TEST=TRUE  
59 5 POWER\_BUTTON\_L FUNC\_TEST=TRUE  
26 5 SW\_RST\_BTN\_L FUNC\_TEST=TRUE  
16 NB\_TSENS\_HS\_DXP FUNC\_TEST=TRUE  
16 NB\_TSENS\_HS\_DYN\_FUNC\_TEST=TRUE  
34 11 CPU\_XDP\_CLK\_N\_FUNC\_TEST=TRUE  
34 11 CPU\_XDP\_CLK\_P\_FUNC\_TEST=TRUE  
11 ITPRESET\_L FUNC\_TEST=TRUE  
11 XDP\_BPM\_L<5> FUNC\_TEST=TRUE  
11 XDP\_BPM\_L<4> FUNC\_TEST=TRUE

MISC GROUND VIAS



FUNC TEST 1 OF 2

SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

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APPLE COMPUTER INC. DRAWING NUMBER 051-7039 REV. 21 SCALE NONE SHIT 5 OF 97

8

7

6

5

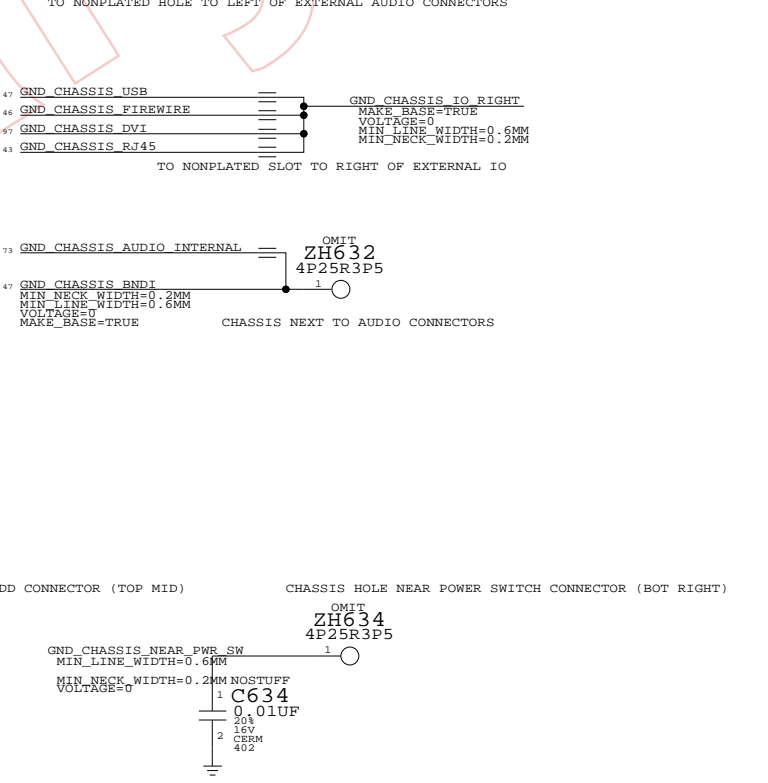
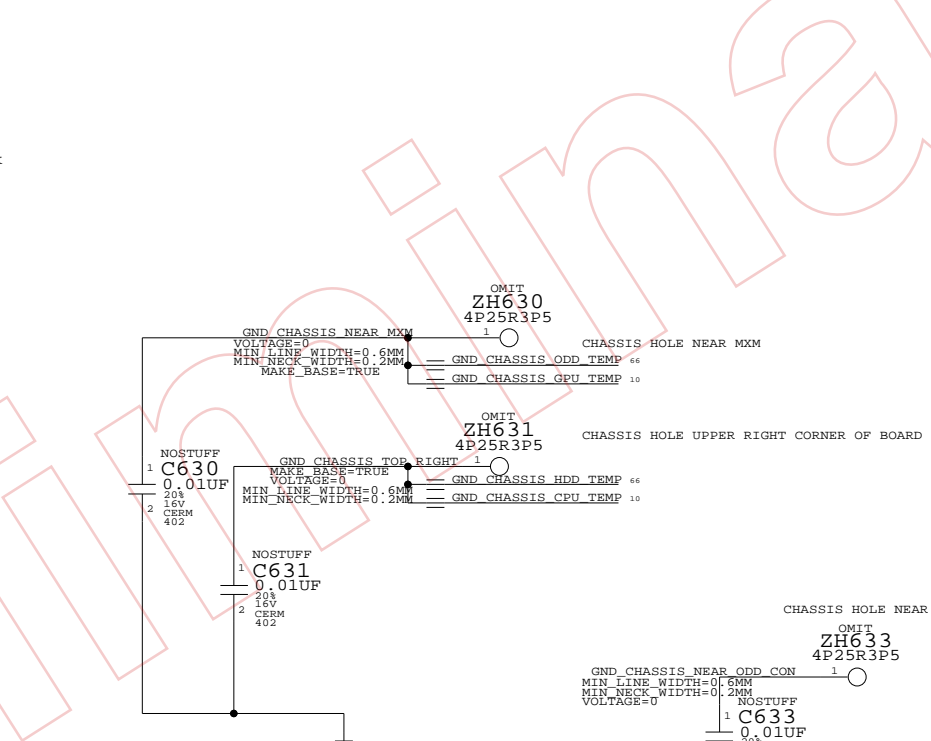
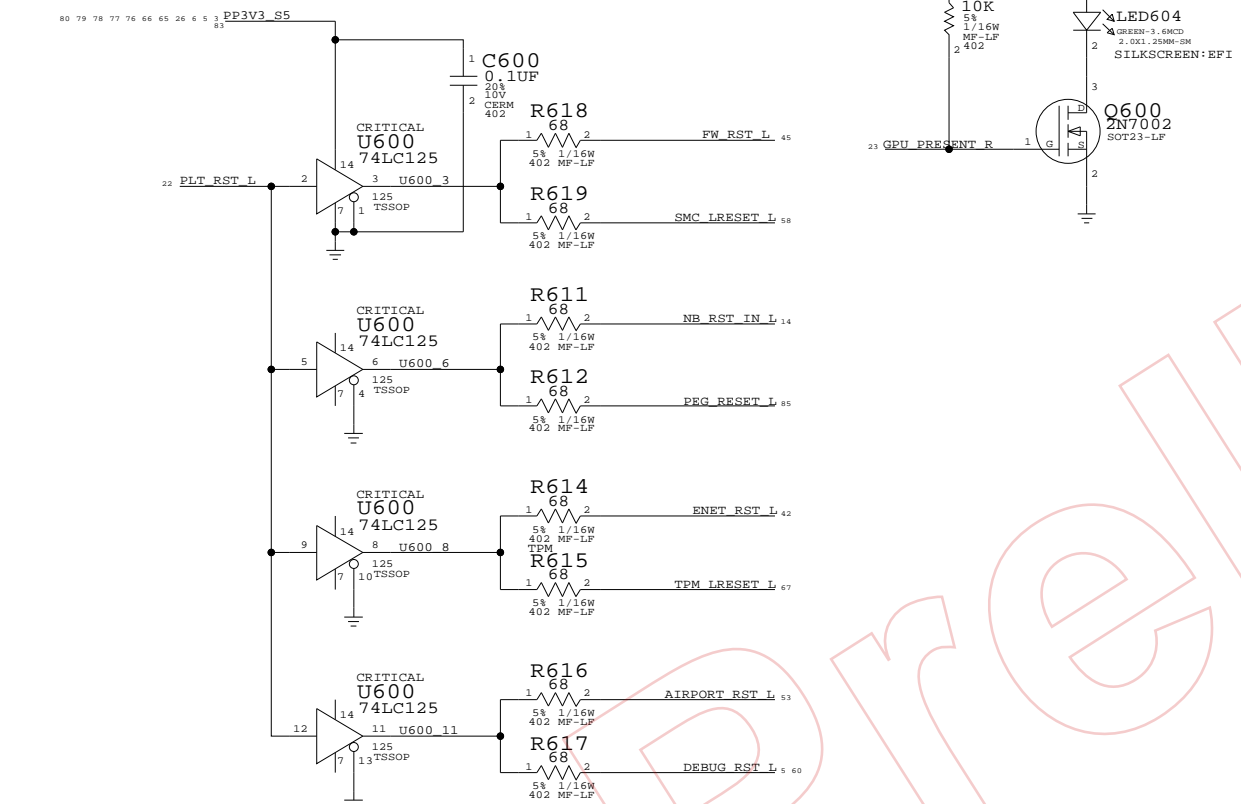
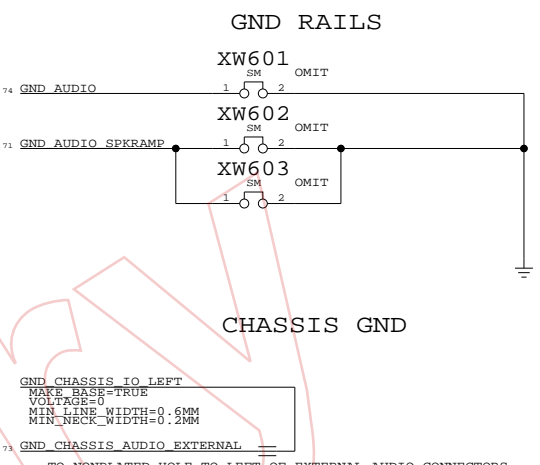
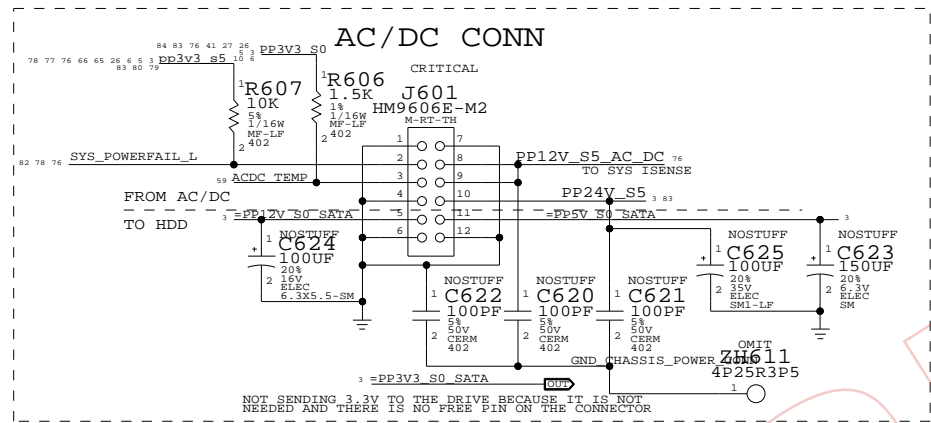
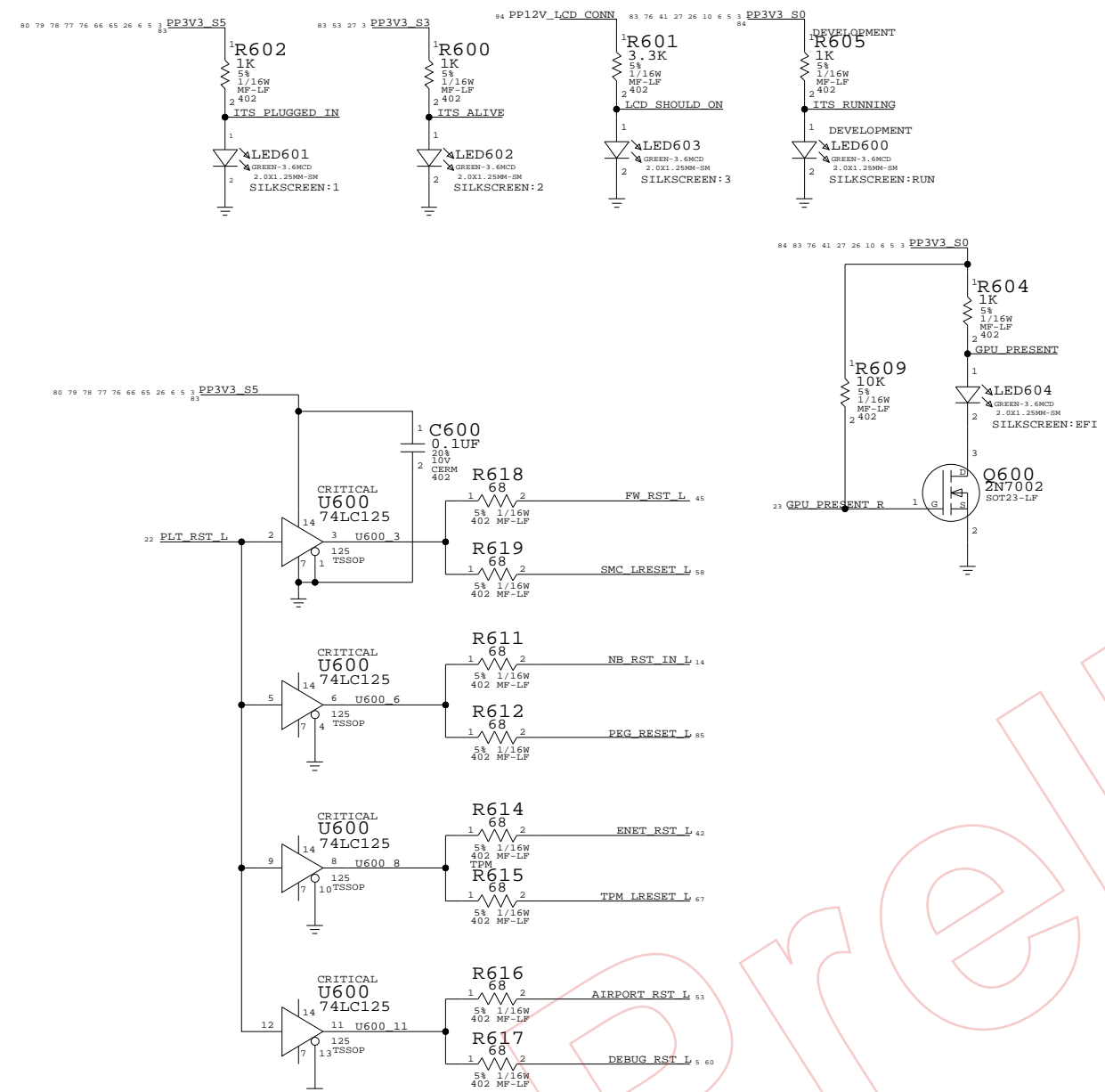
4

3

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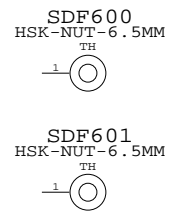
1

SYSTEM STATUS



HEATSINK BACKER PLATE STANDOFFS

LOCATED NORTH OF CPU



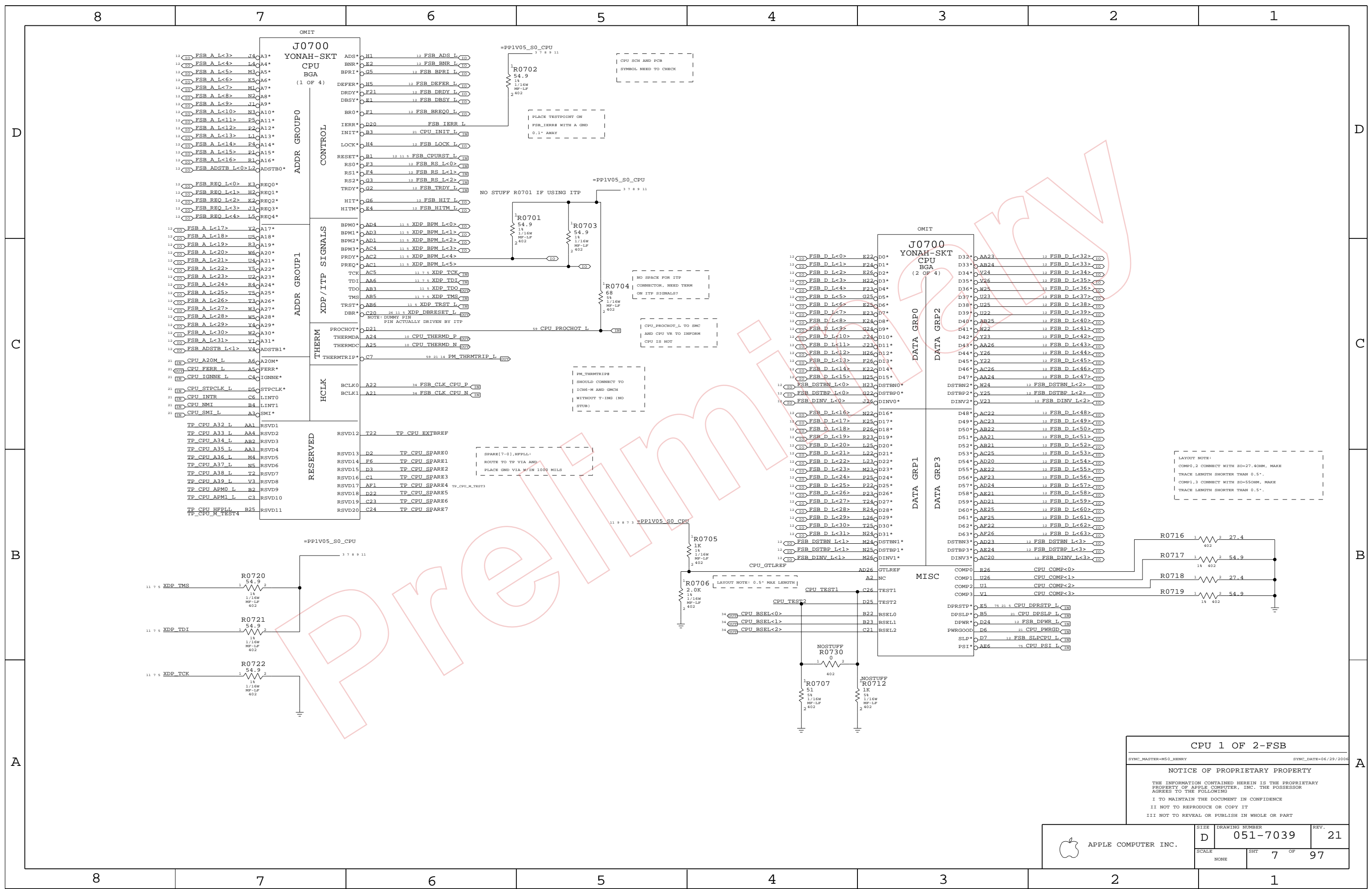
POWER CONN / MISC

SYNC\_MASTER=M51\_PAUL SYNC\_DATE=06/29/2006

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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 6 OF           | 97   |
| NONE                |      |                |      |



**CPU 1 OF 2-FSB**

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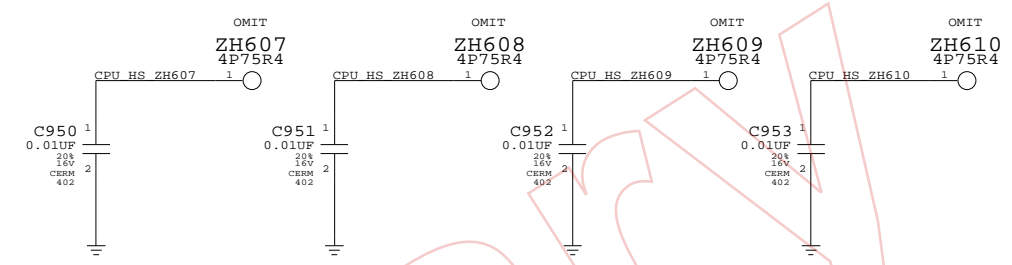
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

|                     |                  |                                   |                   |
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|                     | SCALE<br>NONE    | SHEET<br>7 OF 97                  |                   |



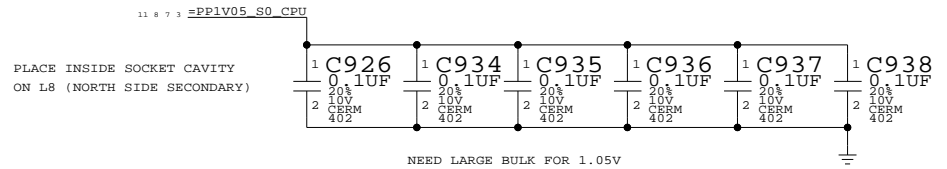


### CPU HEATSINK MOUNTING HOLES



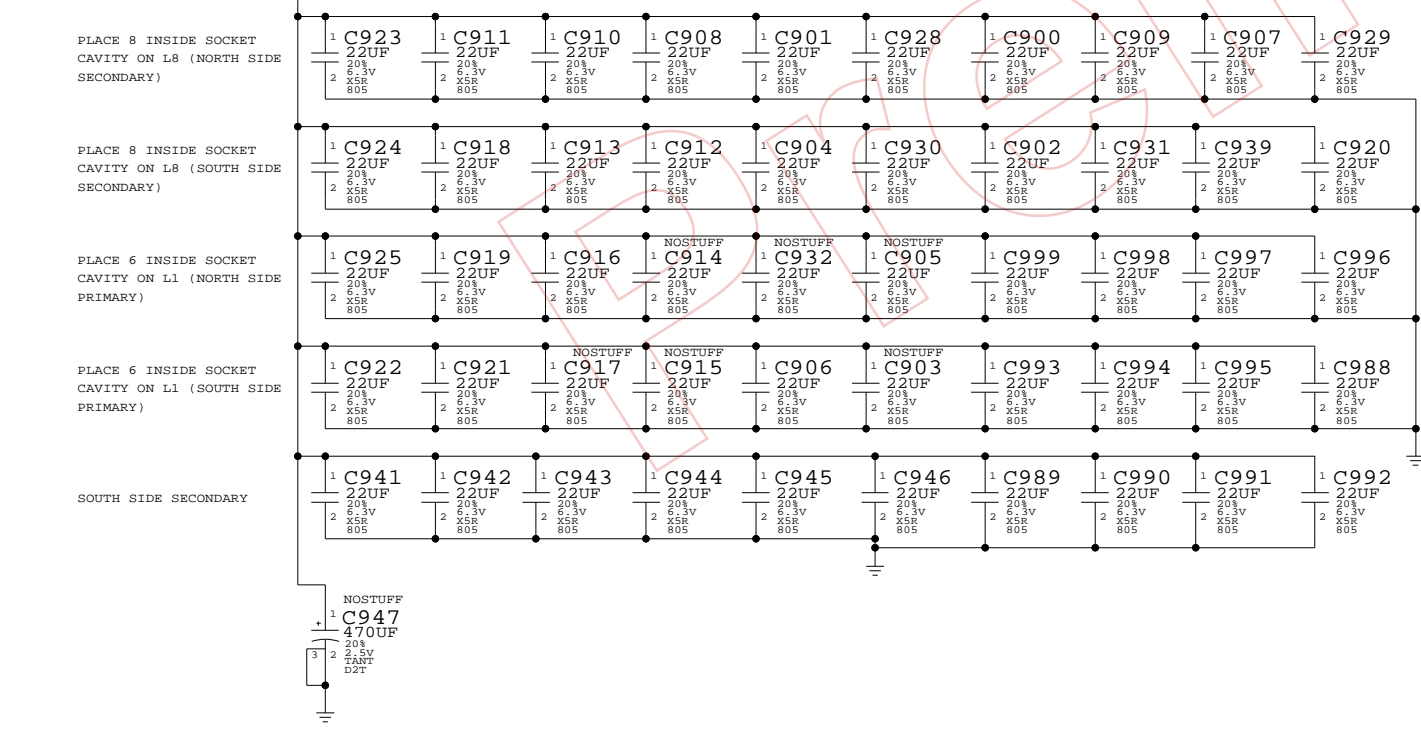
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

### VCCP CORE DECOUPLING



### VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



CPU DECAPS & VID<>

SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

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| SCALE               | SHT  | OF             | REV. |
| NONE                | 9    | 97             |      |

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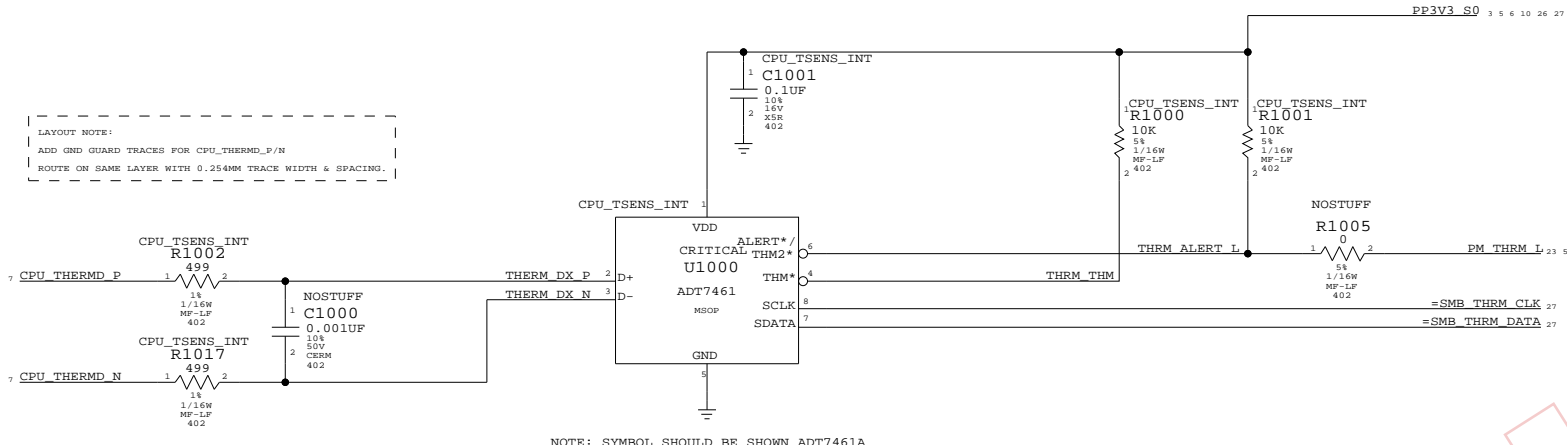
C

B

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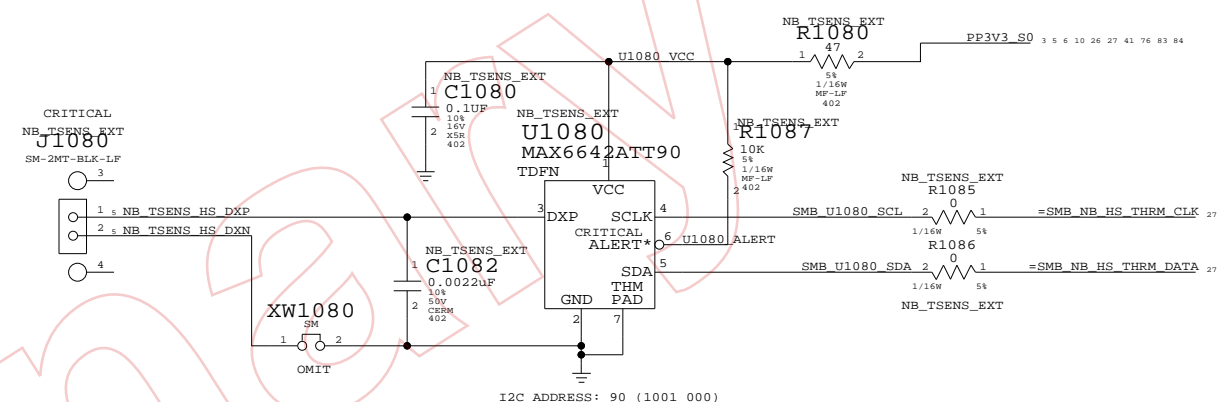
CPU INTERNAL DIODE THERMAL SENSOR

NOTE:  
IF CPU T DIODE TO BE READ IN OFF STATE,  
THEN THIS SHOULD BE S5



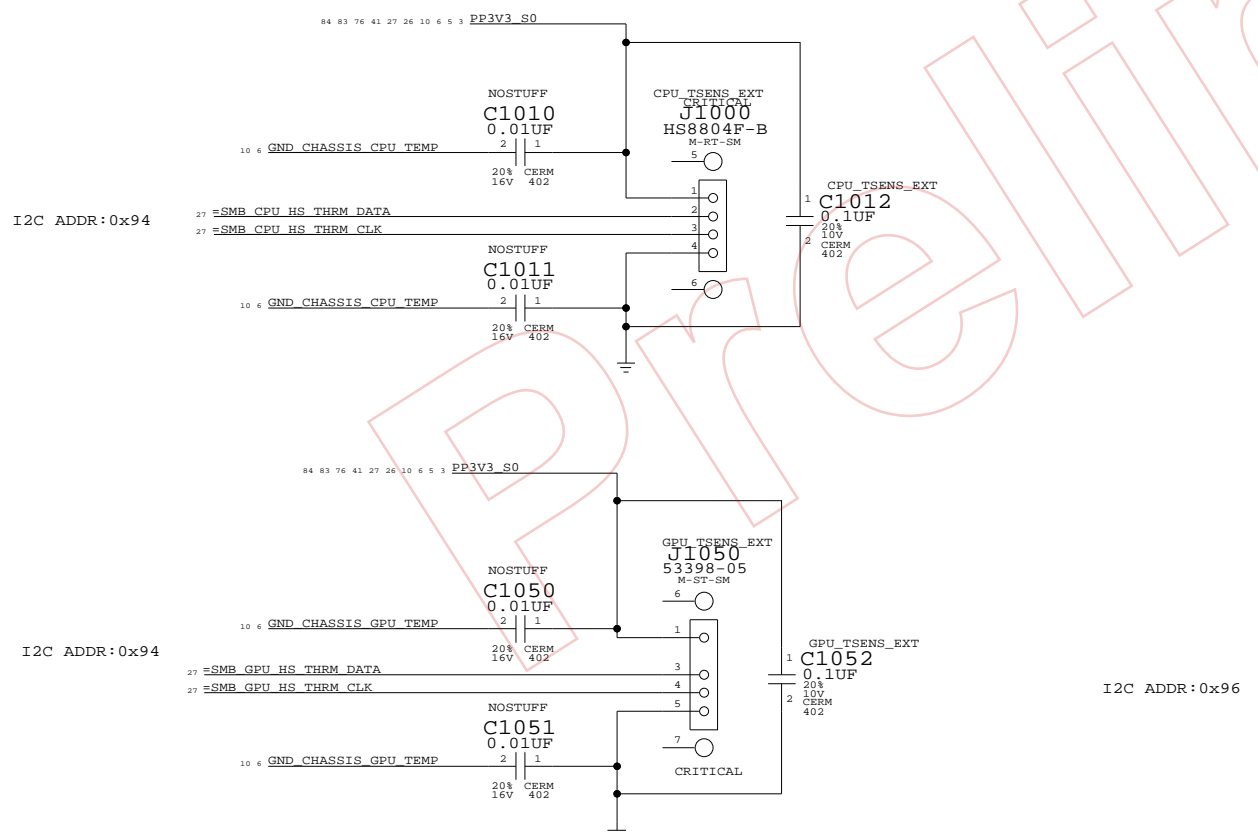
NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

NB HEATSINK TEMPERATURE SENSE

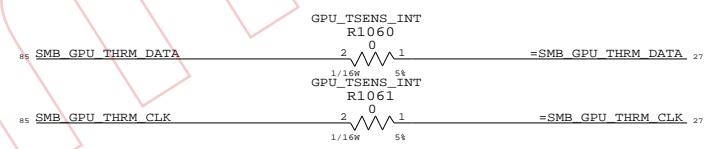


I2C ADDRESS: 90 (1001 000)

CPU AND GPU REMOTE HEATSINK THERMAL SENSORS

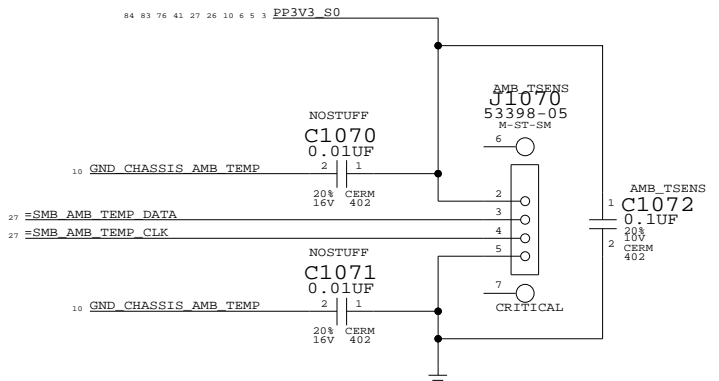


MXM CARD TEMPERATURE SENSOR  
(GPU INTERNAL DIODE)



NOTE: I2C ADDR:98(1001 100) ON NVIDIA CARD  
MAY NOT BE CONSISTENT WITH OTHER CARDS

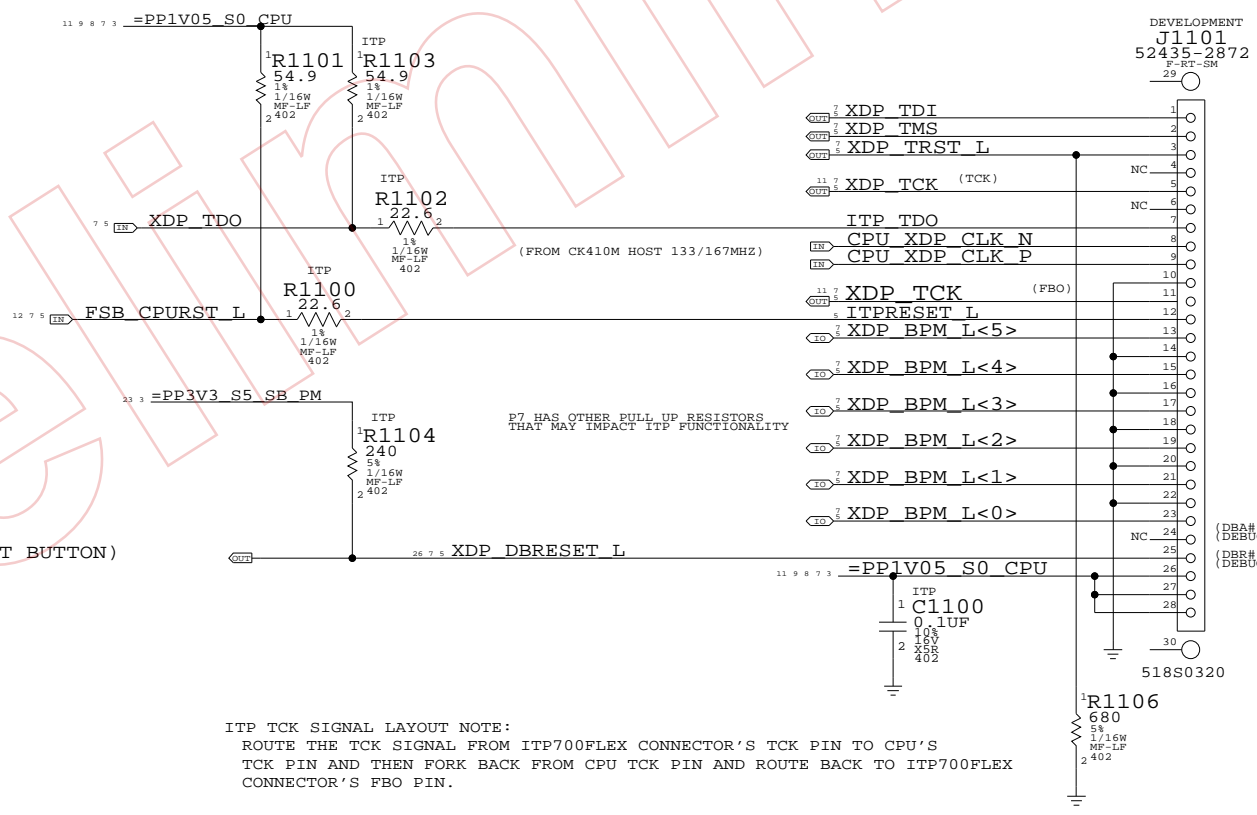
AMBIENT TEMPERATURE (CPU FAN INTAKE) SENSOR



| ASIC TEMP SENSORS    |                |          |          |
|----------------------|----------------|----------|----------|
| SYNC_MASTER=M51_DAVE | DRAWING NUMBER |          | REV.     |
|                      | D              | 051-7039 | 21       |
| SCALE                |                | SHT      | 10 OF 97 |
| NONE                 |                |          |          |

APPLE COMPUTER INC.

### CPU ITP700FLEX DEBUG SUPPORT



DEVELOPMENT  
 J1101  
 52435-2872  
 P-ST-SM  
 29

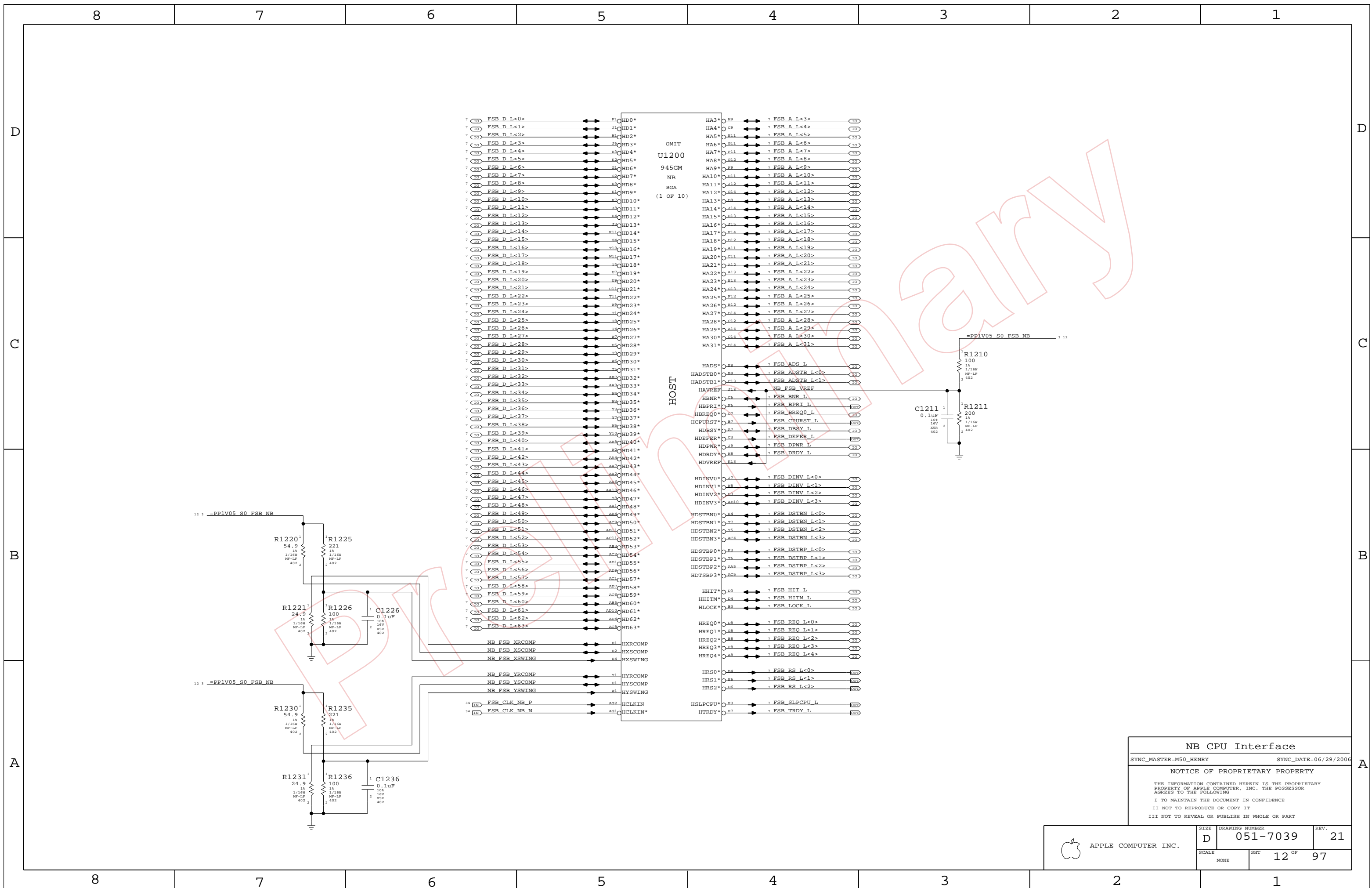
(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.  
 (DEBUG PORT ACTIVE)  
 (DBA#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
 (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:  
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
 CONNECTOR'S FBO PIN.

(AND WITH RESET BUTTON)

**CPU ITP700FLEX DEBUG**  
 SYNC\_MASTER=M50\_HENRY SYNC\_DATE=06/29/2006  
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| NONE                |      |                |      |



**NB CPU Interface**

SYNC\_MASTER=M50\_HENRY      SYNC\_DATE=06/29/2006

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| SCALE               | SHT  | 12 OF          | 97   |
| NONE                |      |                |      |

**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented  
 Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
 VCCD\_LVDS must remain powered with proper decoupling.  
 Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**

Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC

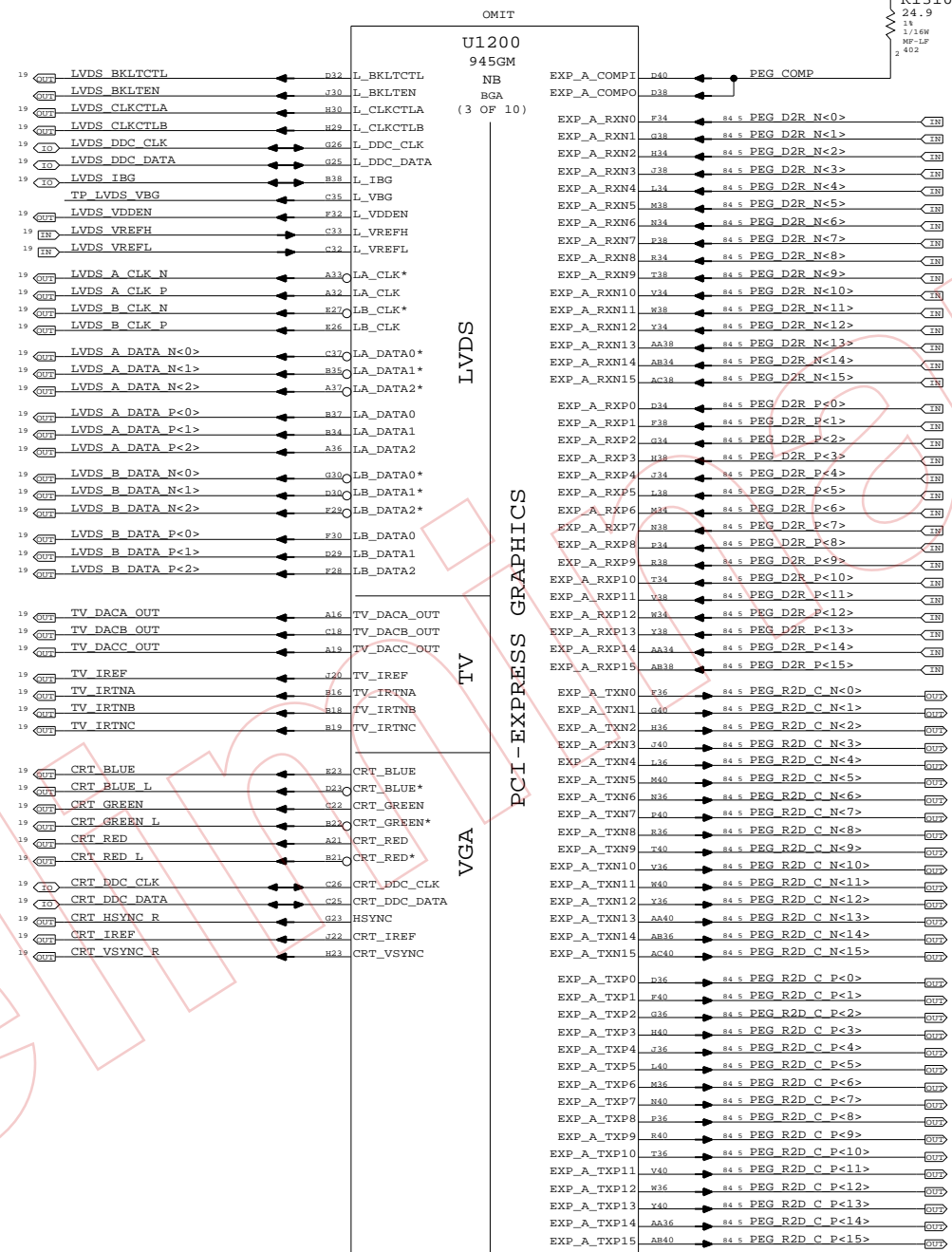
Unused DAC outputs must remain powered, but can omit  
 filtering components. Unused DAC outputs should  
 connect to GND through 75-ohm resistors.

**TV-Out Disable**

Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
 Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
 VCCA\_TVVBG to 1.5V power rail. Tie VSSA\_TVVBG to GND.

**CRT Disable**

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
 HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
 rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.



**SDVO Alternate Function**

SDVO\_TVCLKIN#  
 SDVO\_INT#  
 SDVO\_FLDSTALL#

SDVO\_TVCLKIN  
 SDVO\_INT  
 SDVO\_FLDSTALL

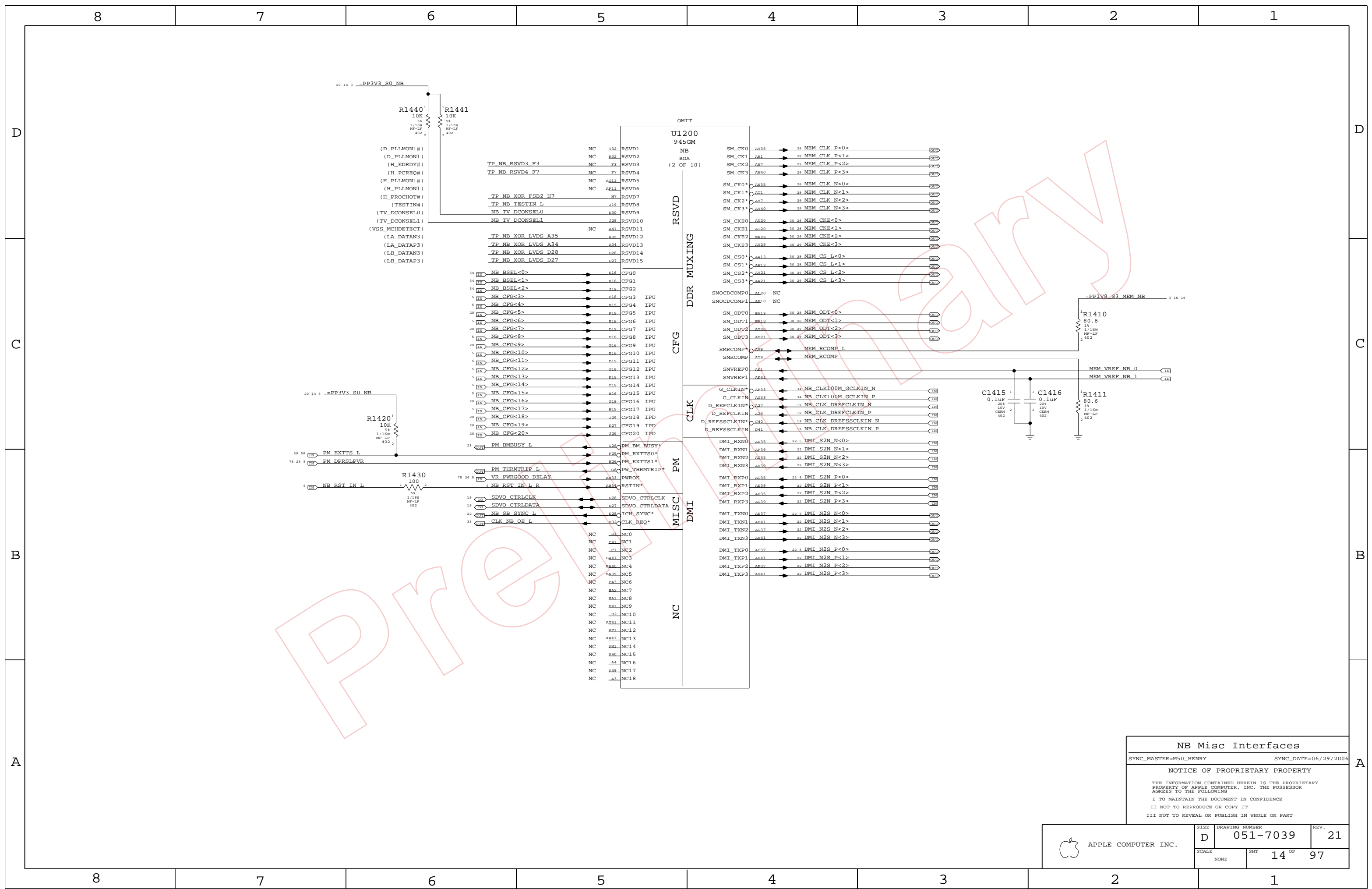
SDVOB\_RED#  
 SDVOB\_GREEN#  
 SDVOB\_BLUE#  
 SDVOB\_CLKN  
 SDVOC\_RED#  
 SDVOC\_GREEN#  
 SDVOC\_BLUE#  
 SDVOC\_CLKN

SDVOB\_RED  
 SDVOB\_GREEN  
 SDVOB\_BLUE  
 SDVOB\_CLKP  
 SDVOC\_RED  
 SDVOC\_GREEN  
 SDVOC\_BLUE  
 SDVOC\_CLKP

Preview

|   |                      |
|---|----------------------|
| <b>NB PEG / Video Interfaces</b>  |                      |
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| NONE                |      |                |      |



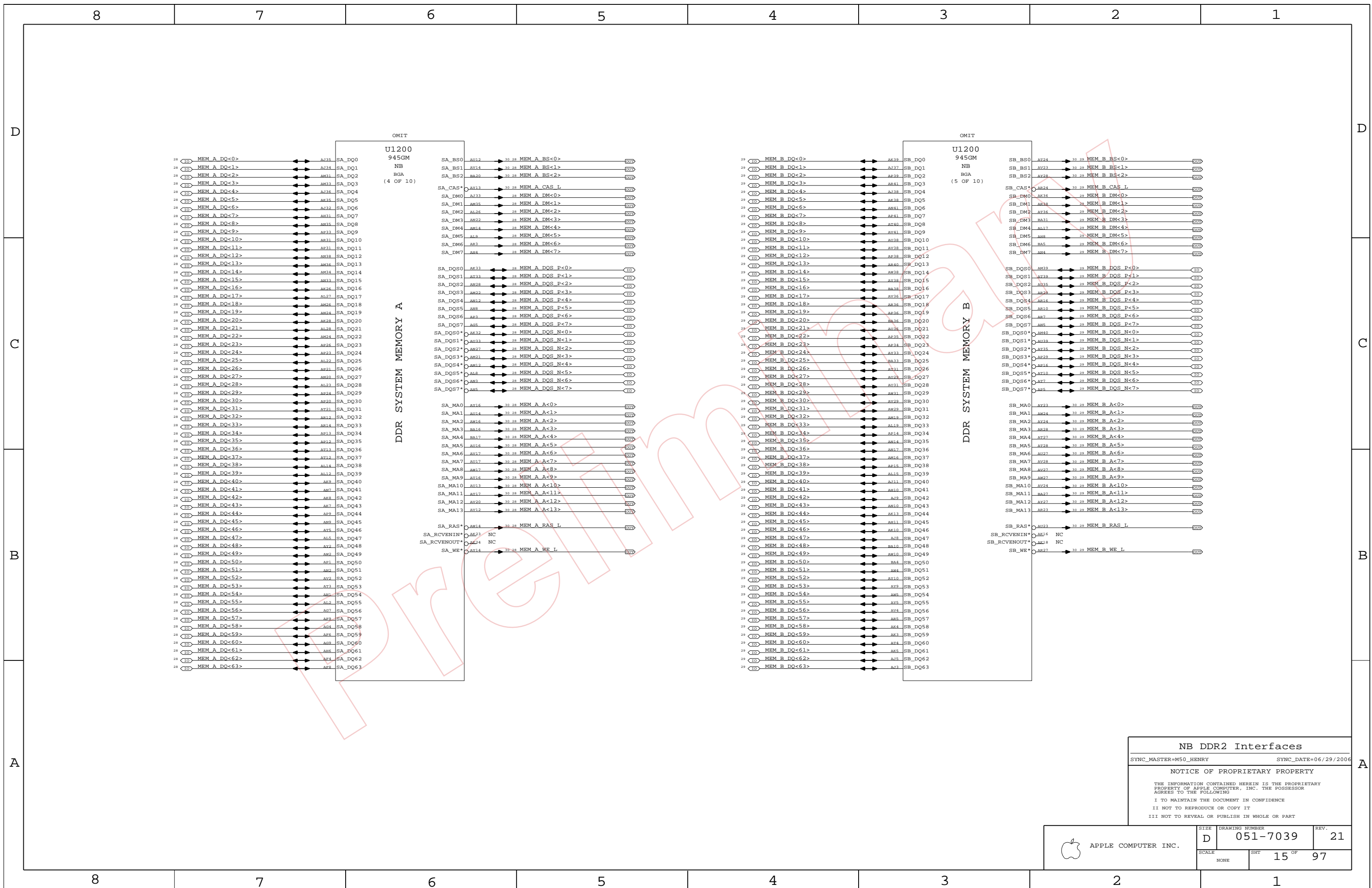
**NB Misc Interfaces**

SYNC\_MASTER=M50\_HENRY SYNC\_DATE=06/29/2006

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| SCALE               | SHT  | 14 OF 97       |      |
| NONE                |      |                |      |



**NB DDR2 Interfaces**

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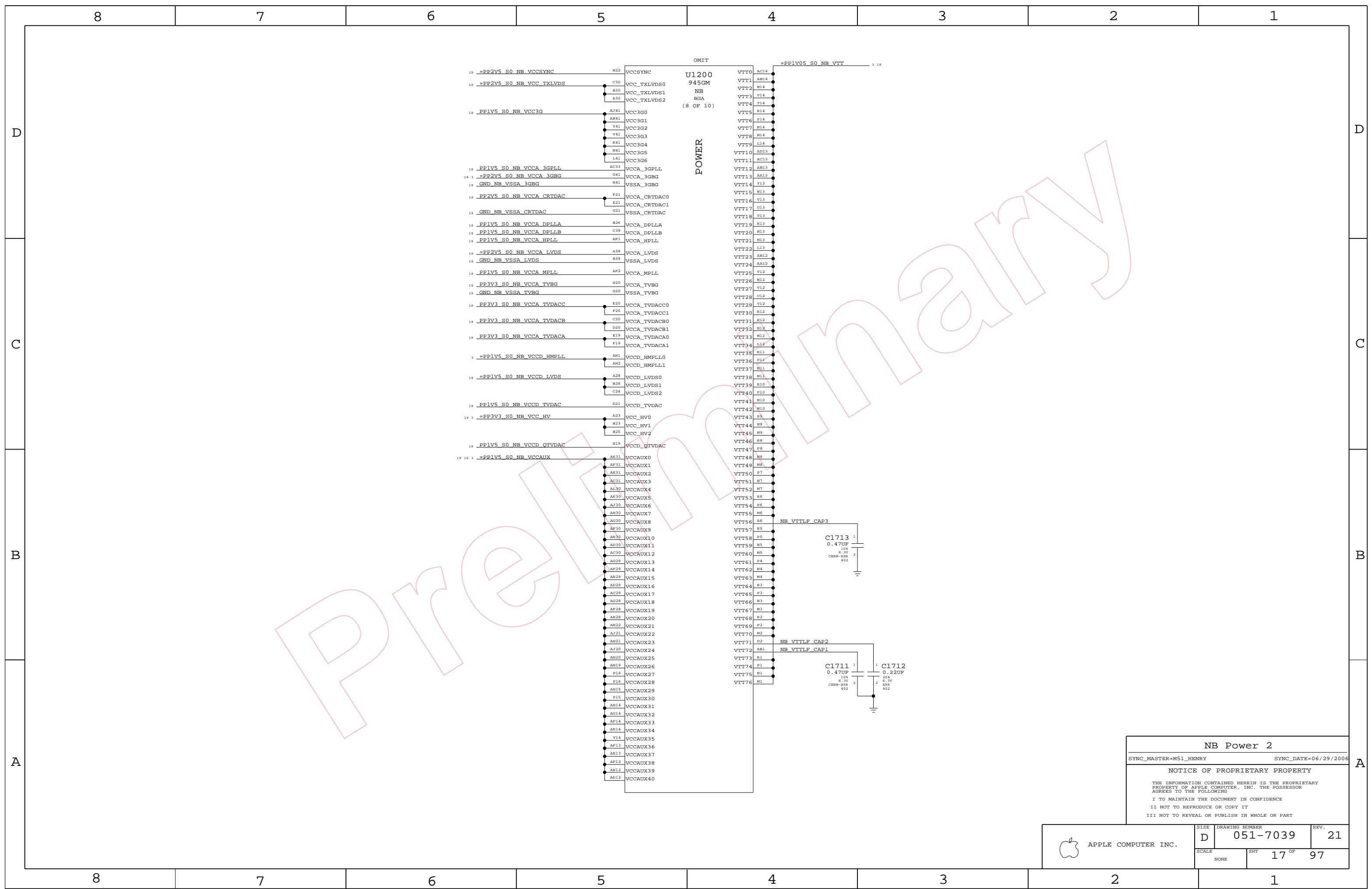
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|                     | SCALE<br>NONE    | SHEET<br>15 OF 97                 |                   |



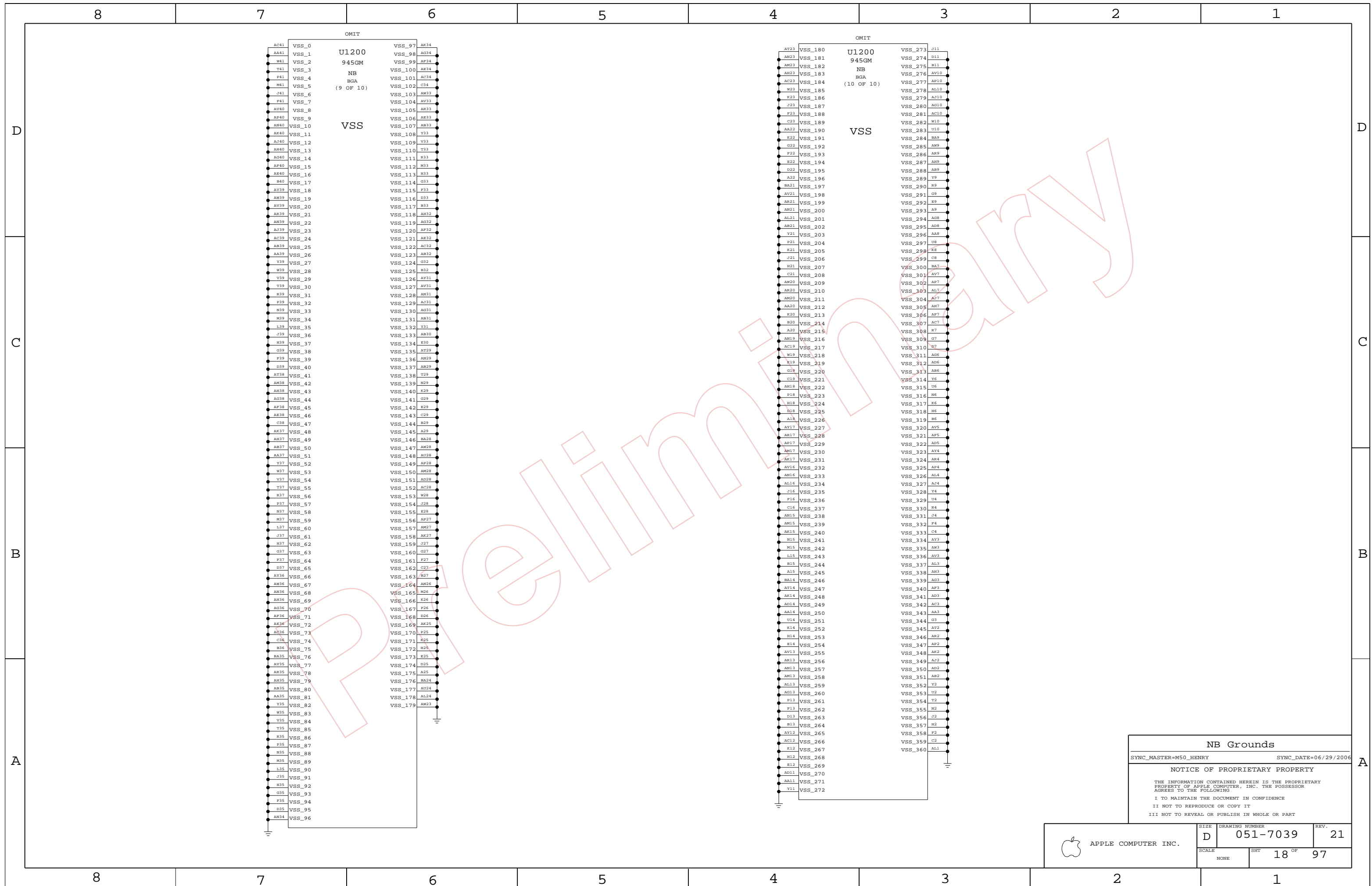




NB Power 2  
 SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

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| SCALE               | NONE | SHT            | 17 OF 97 |



**NB Grounds**

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|                     | SCALE<br>NONE    | SHT<br><b>18</b> OF <b>97</b>     |                   |

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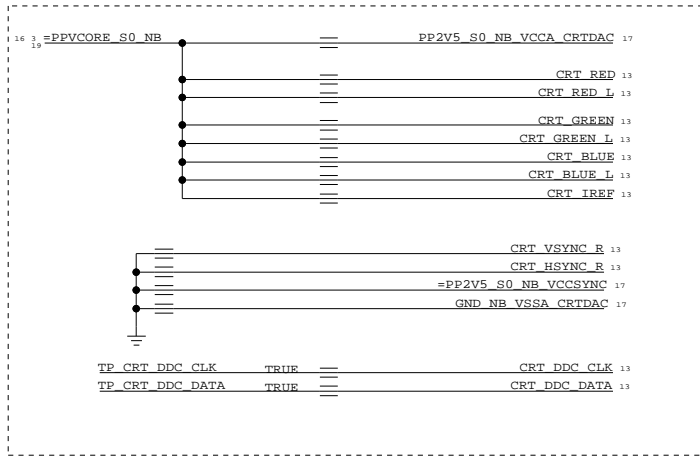
B

B

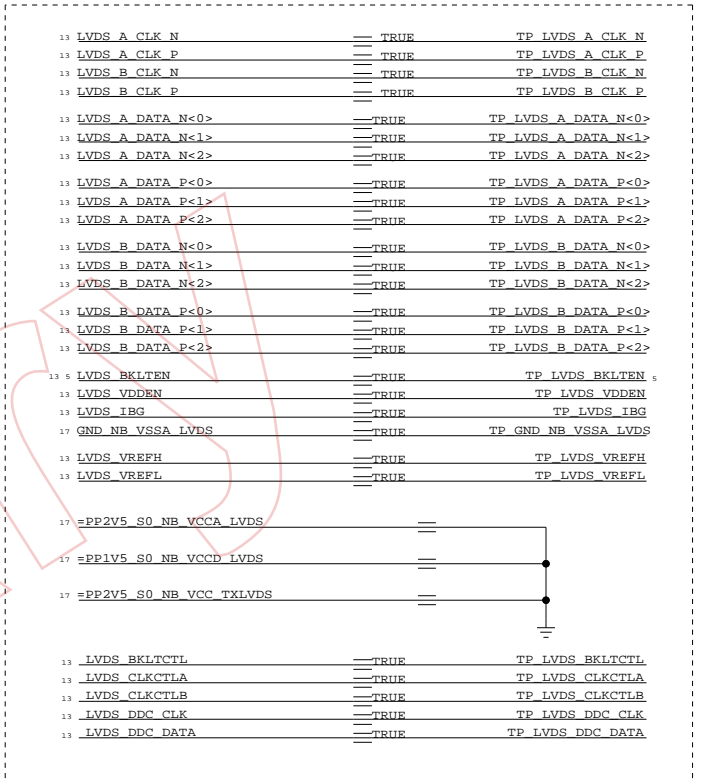
A

A

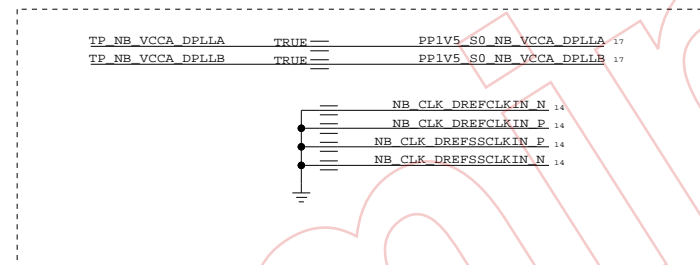
### TVOUT DISABLE



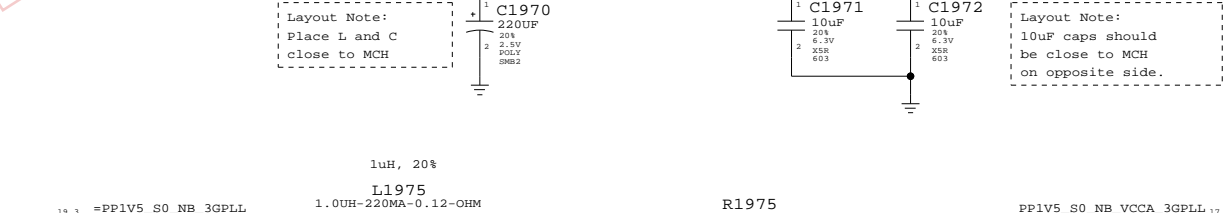
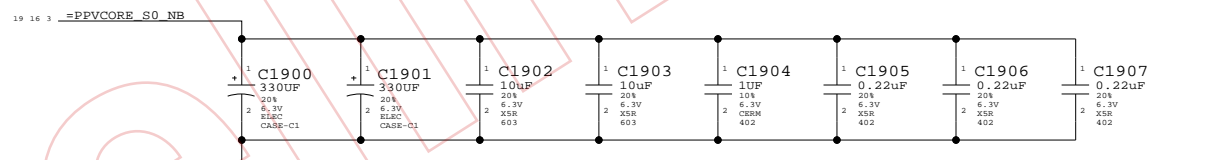
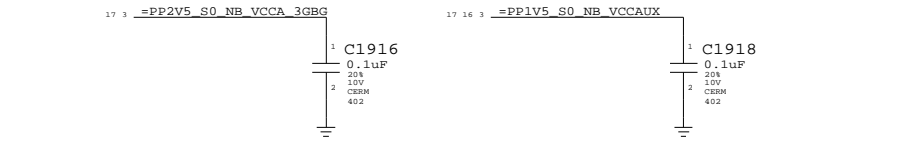
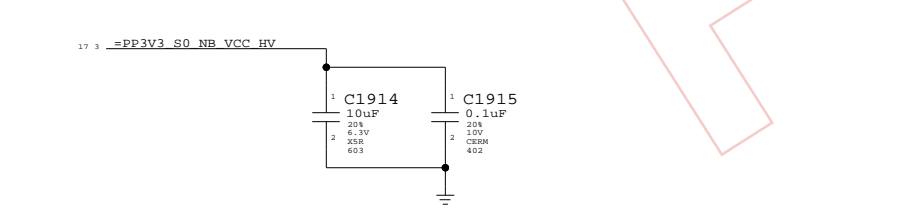
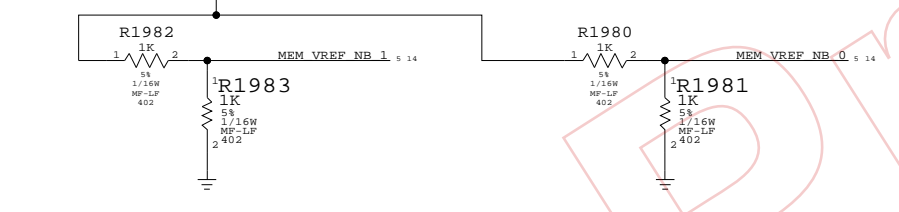
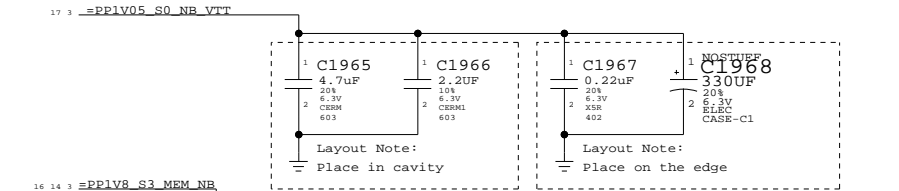
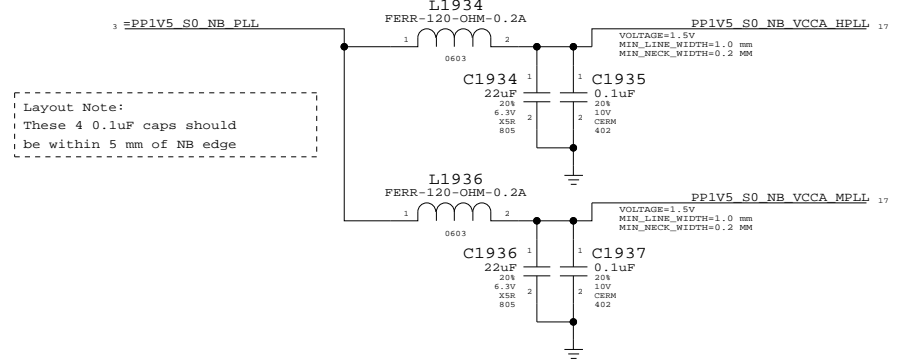
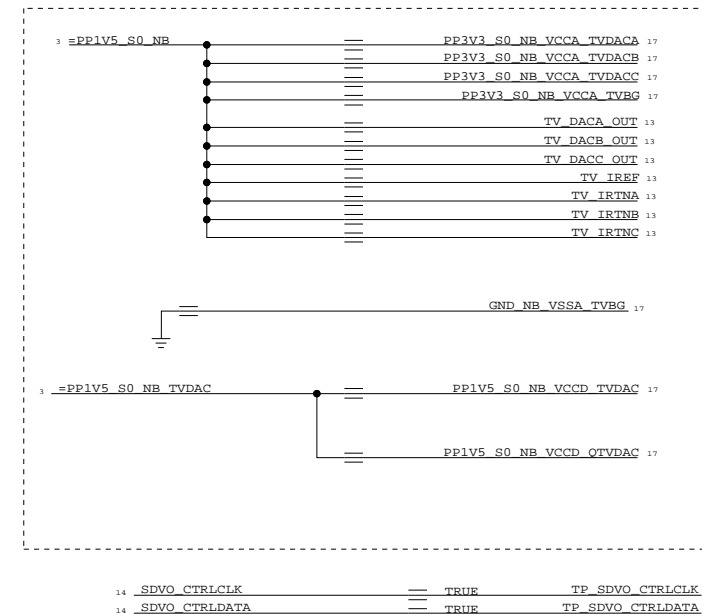
### LVDS DISABLE



### DISPLAY DISABLE

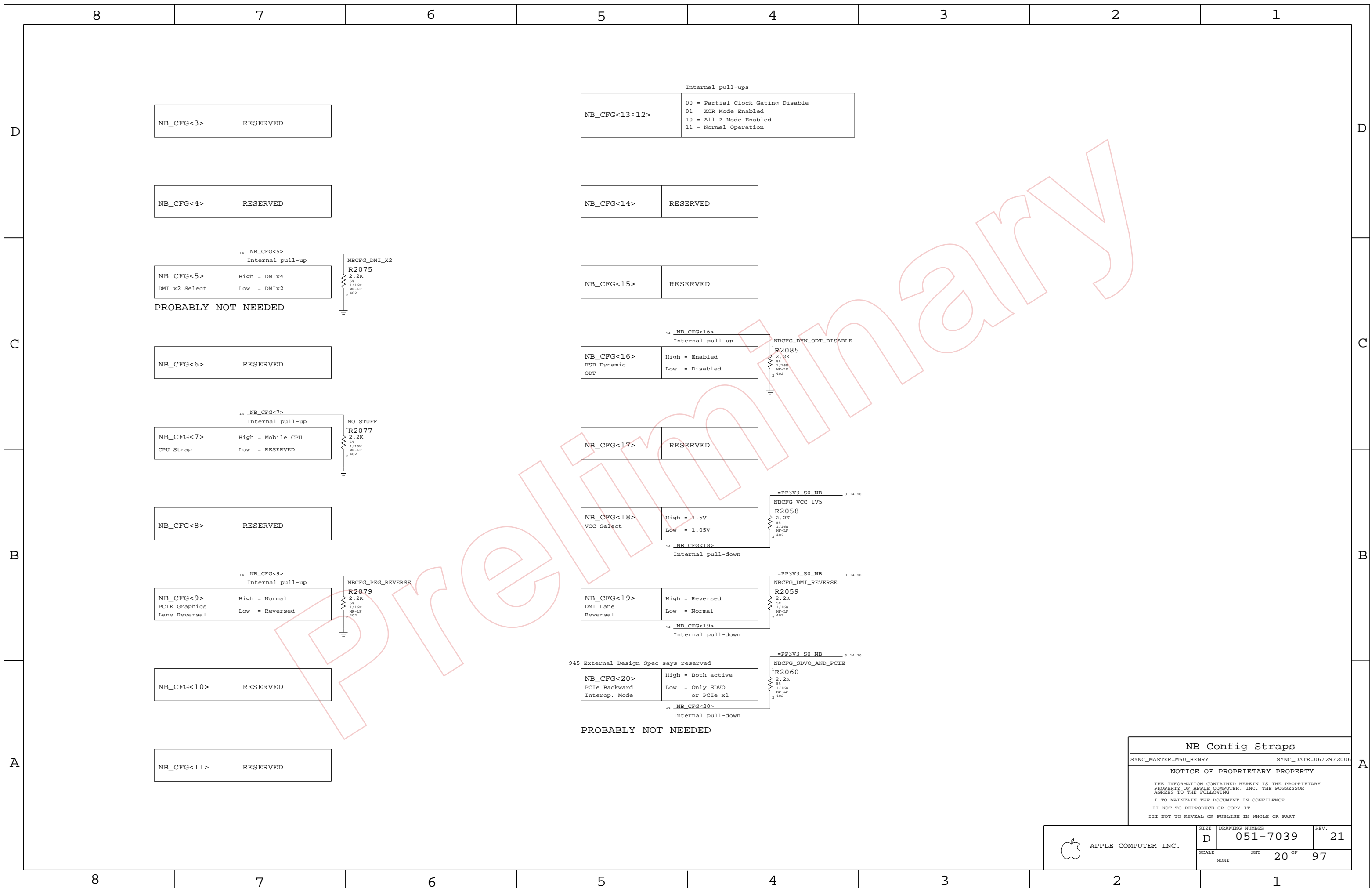


### TVOUT DISABLE



**NB (GM) Decoupling**  
 SYNC\_MASTER=M51\_DAVE SYNC\_DATE=(MASTER)  
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 19 OF          | 97   |
| NONE                |      |                |      |



**NB Config Straps**

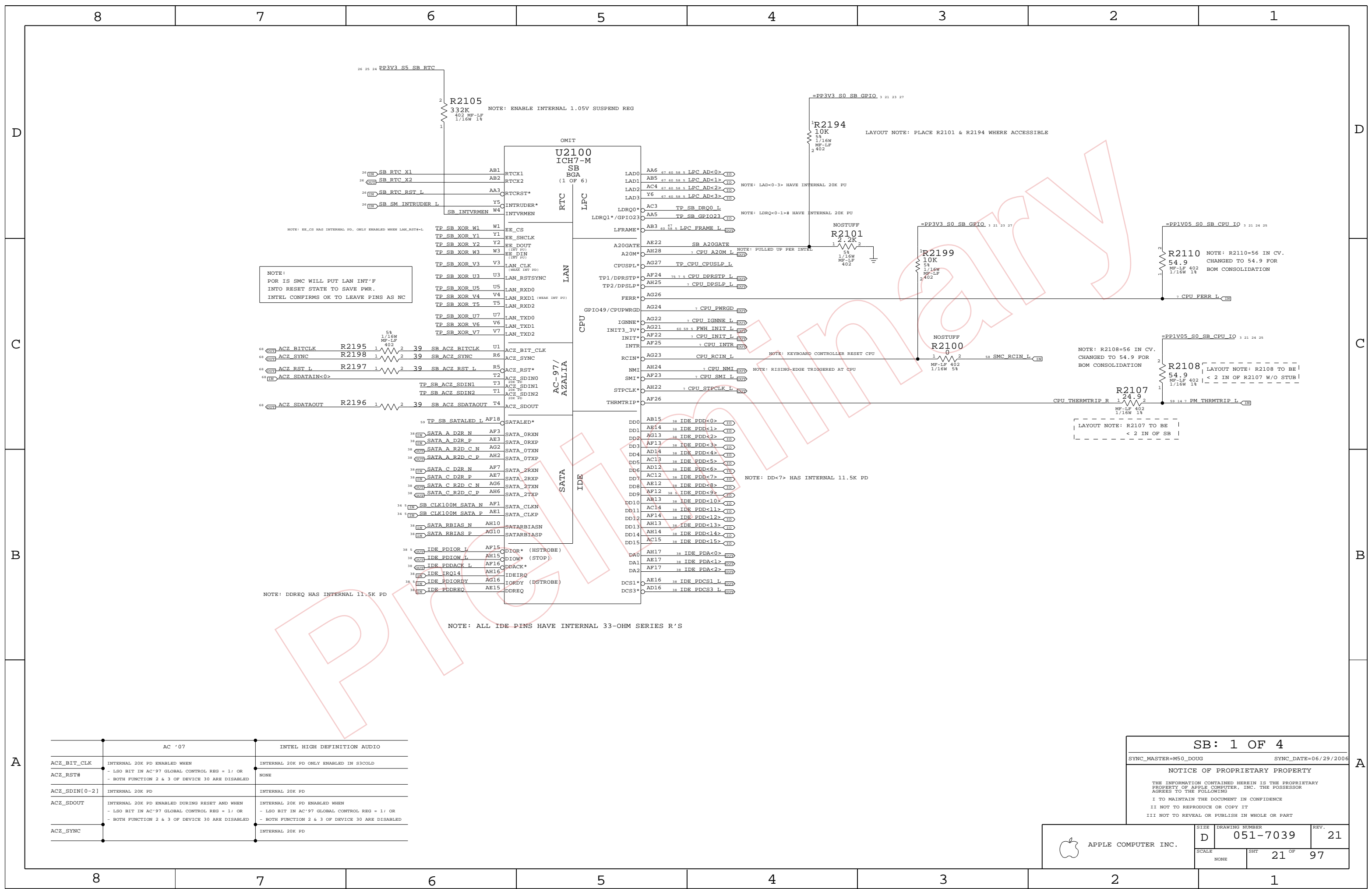
SYNC\_MASTER=M50\_HENRY      SYNC\_DATE=06/29/2006

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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | OF             |      |
| NONE                | 20   | 97             |      |



NOTE:  
 POR IS SMC WILL PUT LAN INT'F  
 INTO RESET STATE TO SAVE PWR.  
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

| AC '07        | INTEL HIGH DEFINITION AUDIO   |
|---------------|---|
| ACZ_BIT_CLK   | INTERNAL 20K PD ENABLED WHEN<br>- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR<br>INTERNAL 20K PD ONLY ENABLED IN S3COLD                           |
| ACZ_RST#      | NONE  |
| ACZ_SDIN[0-2] | INTERNAL 20K PD   |
| ACZ_SDOUT     | INTERNAL 20K PD ENABLED DURING RESET AND WHEN<br>- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR<br>- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED |
| ACZ_SYNC      | INTERNAL 20K PD   |

**SB: 1 OF 4**

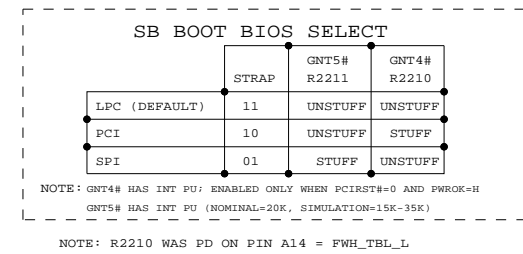
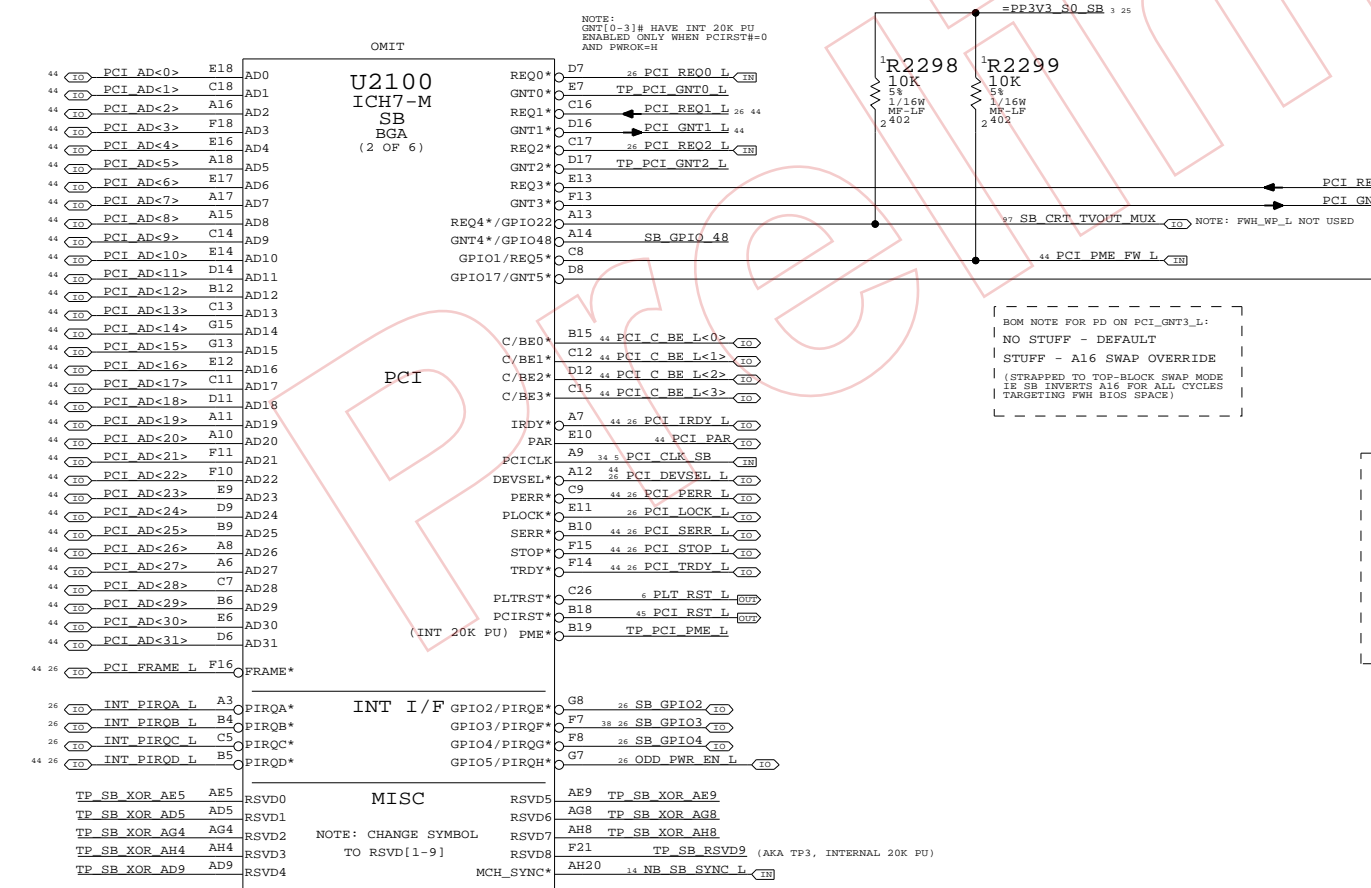
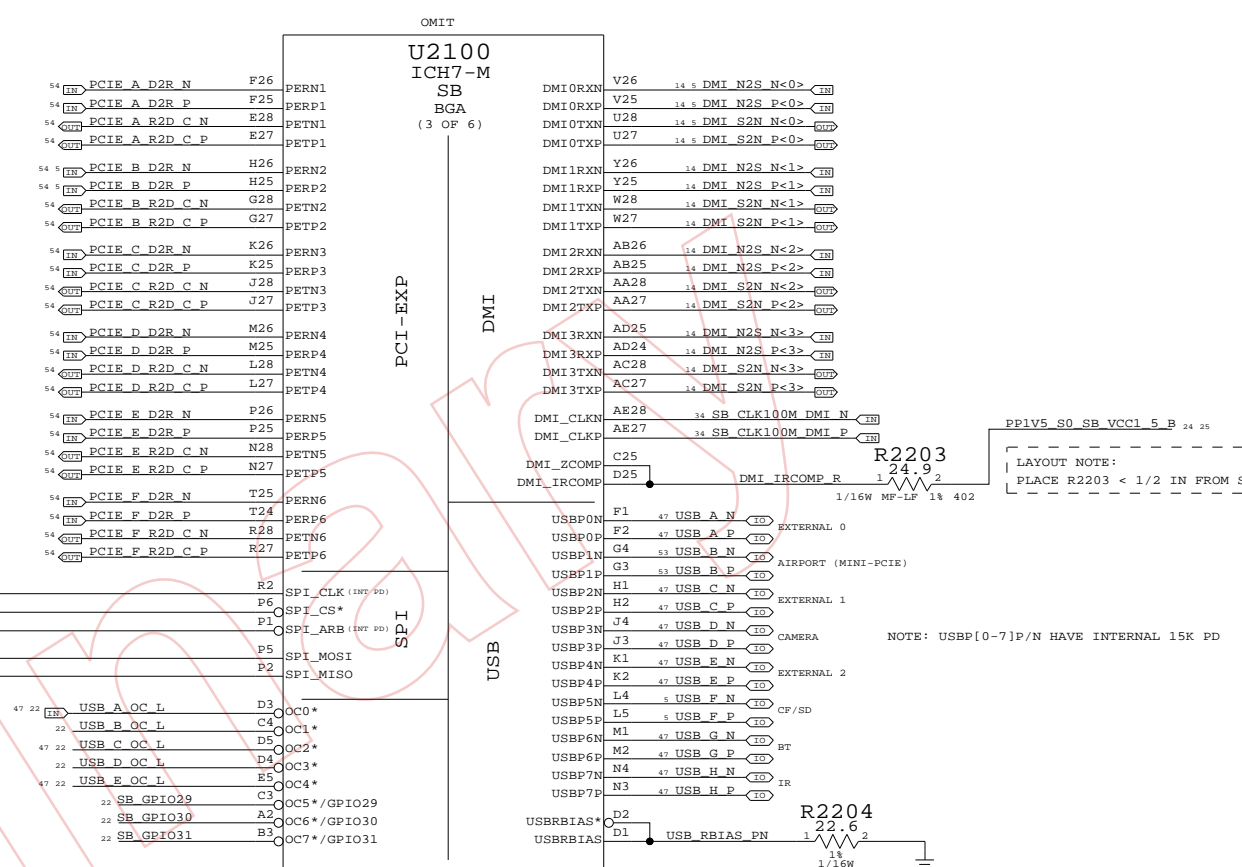
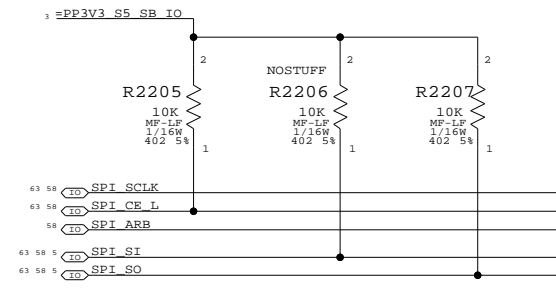
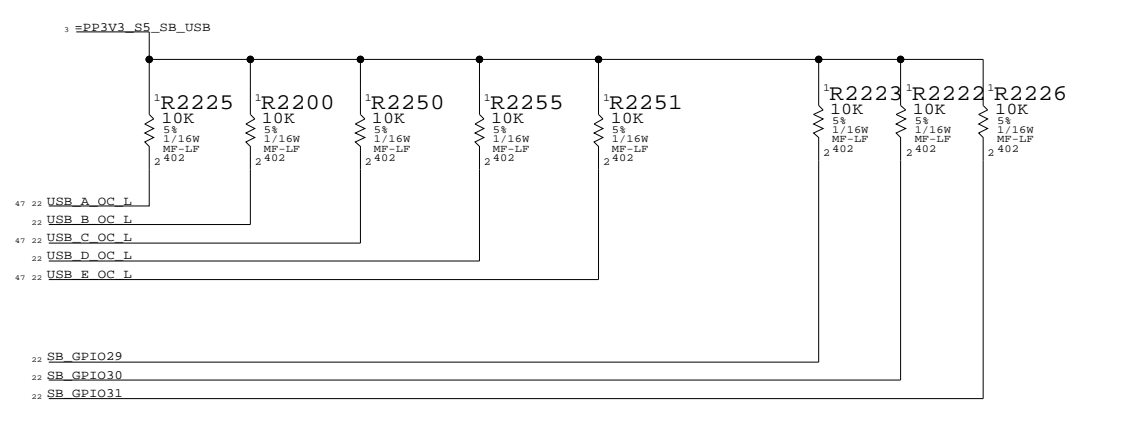
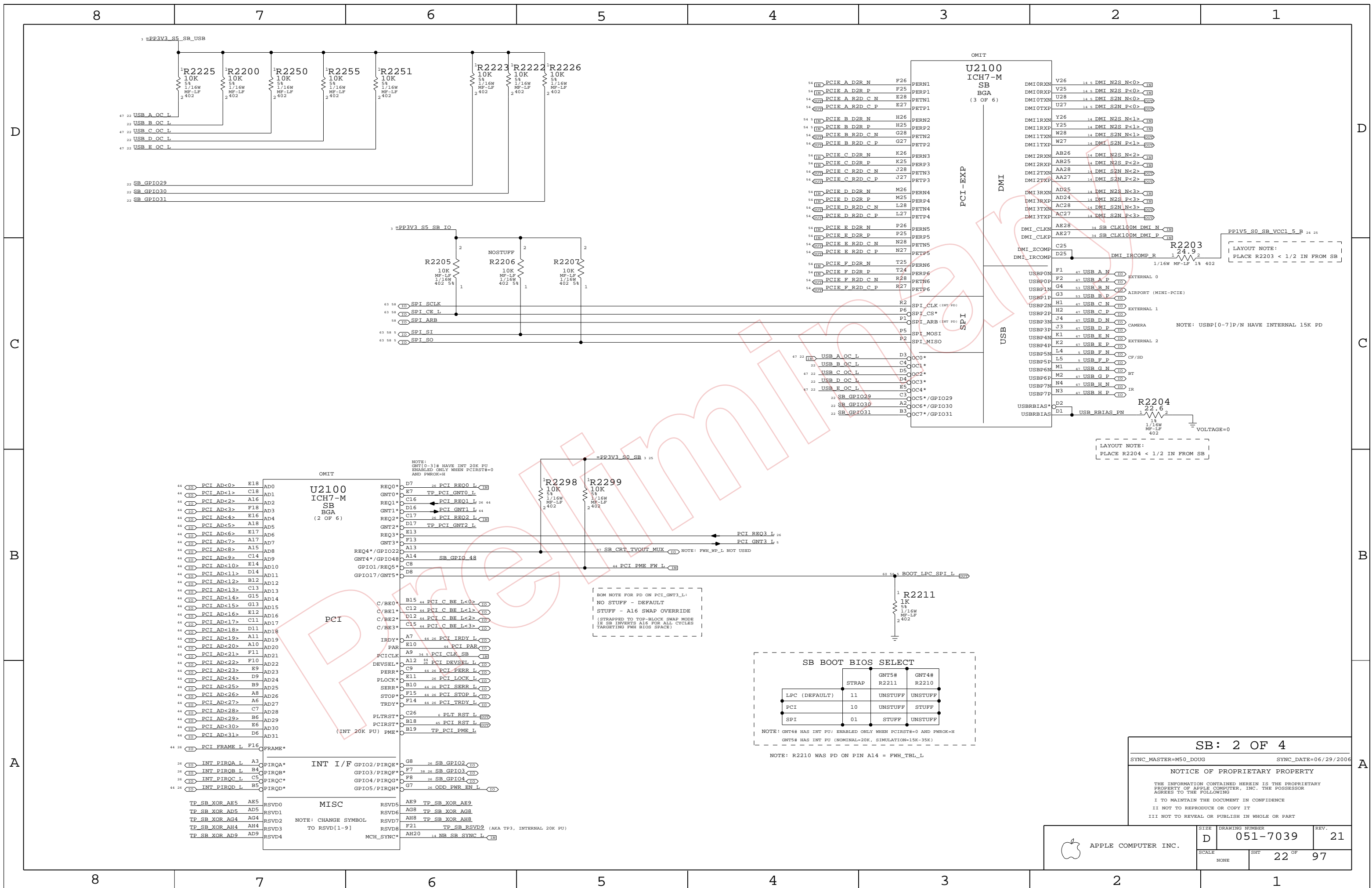
SYNC\_MASTER=M50\_DOUG      SYNC\_DATE=06/29/2006

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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 21 OF 97       |      |
| NONE                |      |                |      |



SB: 2 OF 4

SYNC\_MASTER=M50\_D0UG SYNC\_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

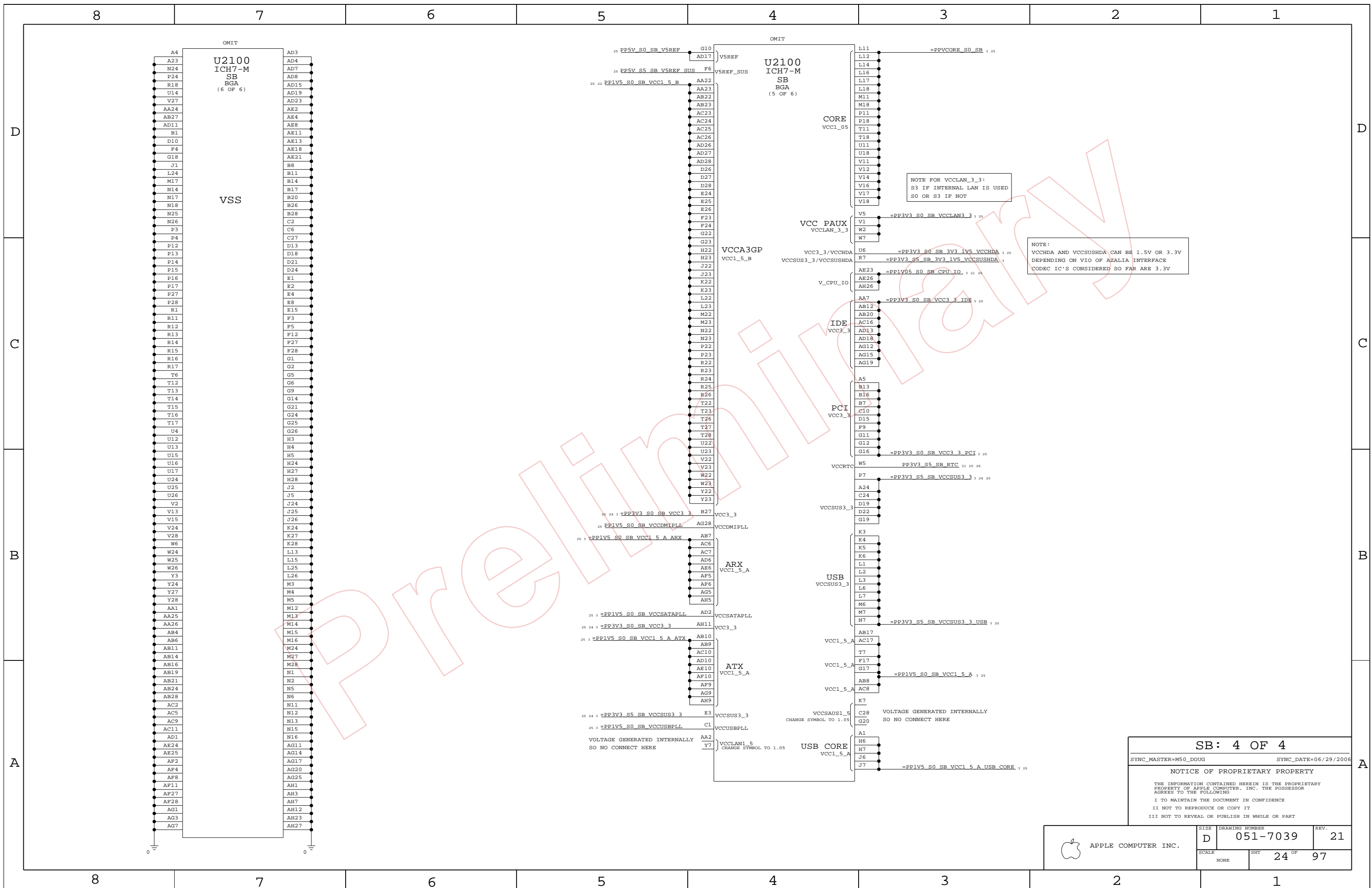
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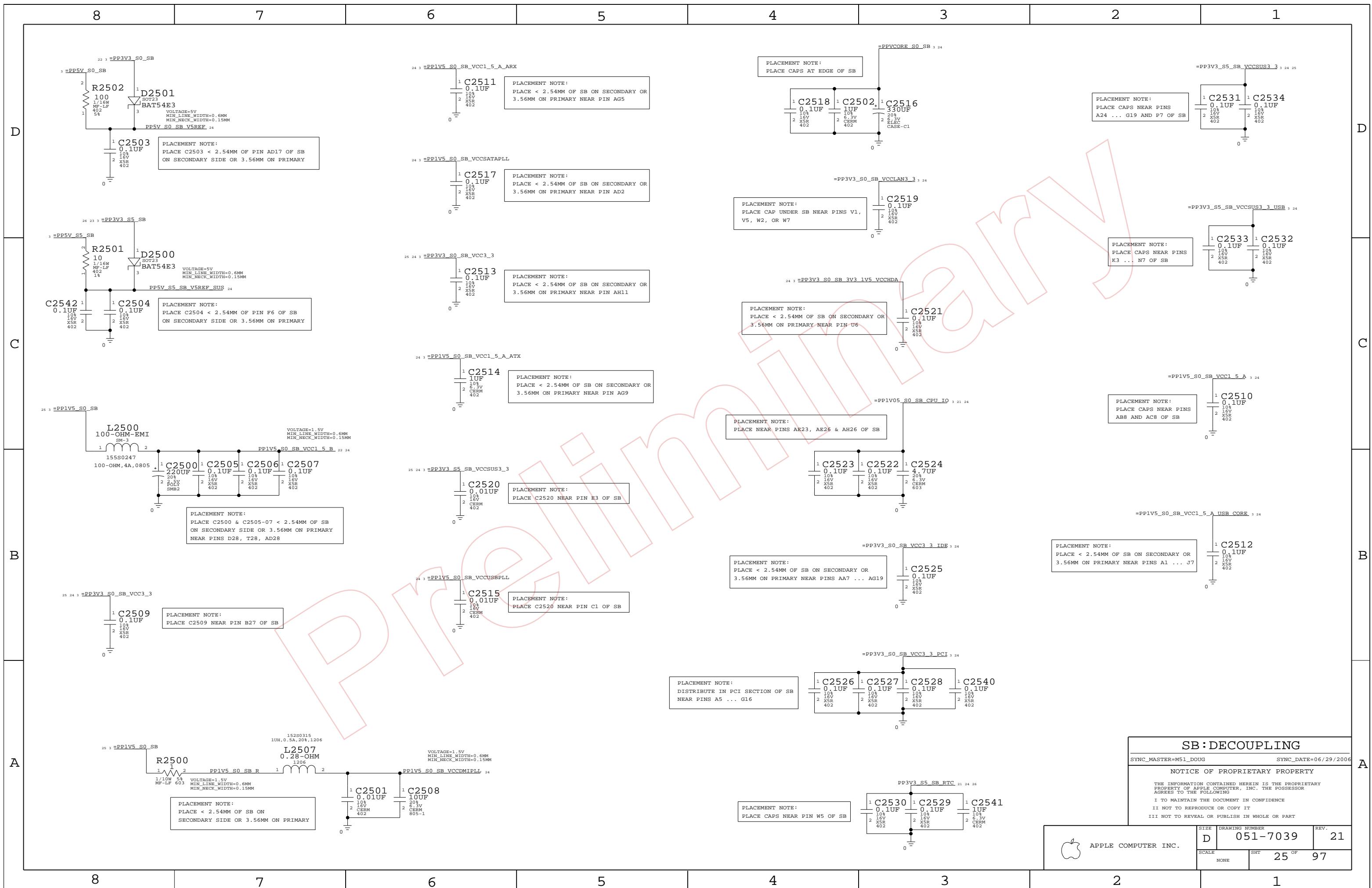
NOTE FOR VCCLAN\_3\_3:  
S3 IF INTERNAL LAN IS USED  
S0 OR S3 IF NOT

NOTE:  
VCCCHDA AND VCCSUS3\_3 CAN BE 1.5V OR 3.3V  
DEPENDING ON VIO OF AZALIA INTERFACE  
CODIC IC'S CONSIDERED SO FAR ARE 3.3V

|  |                      |
|--|----------------------|
| <b>SB: 4 OF 4</b>  |                      |
| SYNC_MASTER=M50_D0UG   | SYNC_DATE=06/29/2006 |
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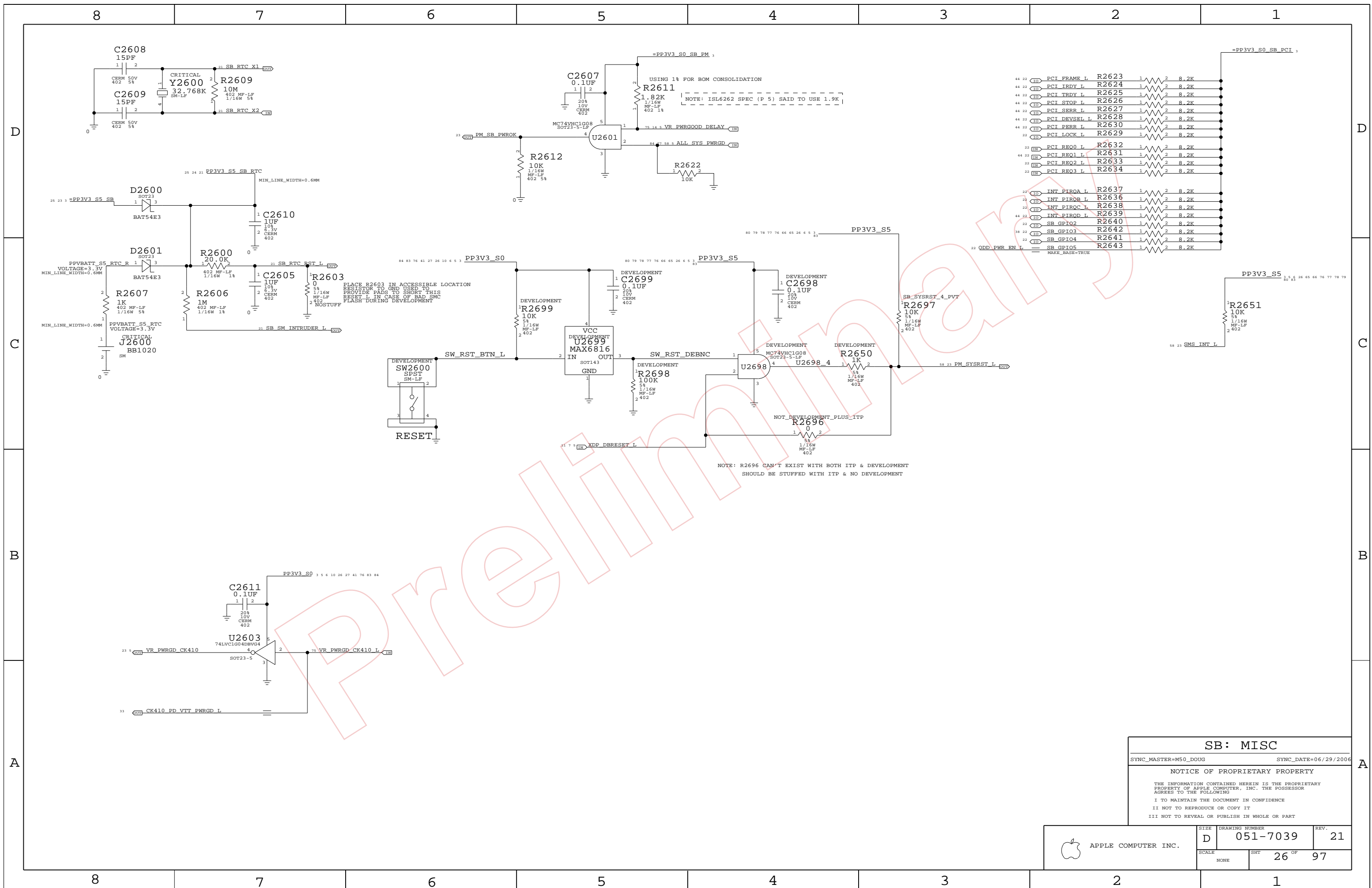
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 24 OF 97       |      |
| NONE                |      |                |      |





**SB: DECOUPLING**  
 SYNC\_MASTER=M51\_D0UG SYNC\_DATE=06/29/2006  
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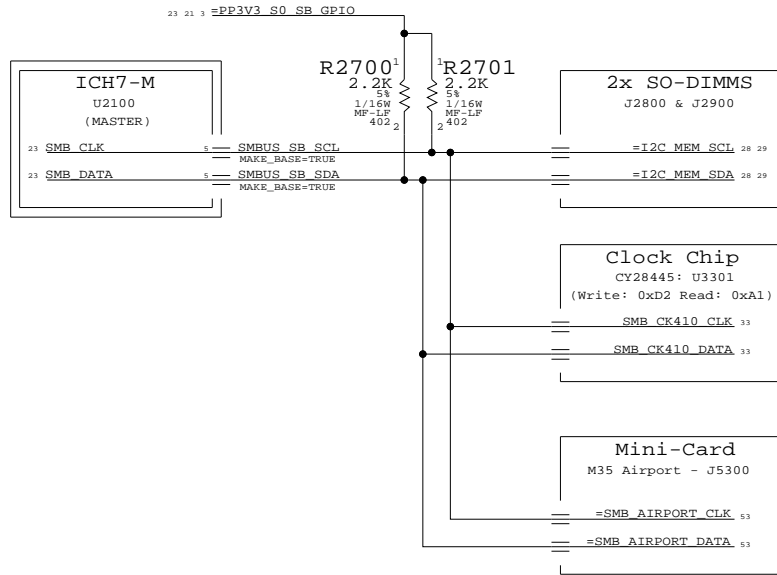
|                     |      |                |      |
|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 25 OF          | 97   |
| NONE                |      |                |      |



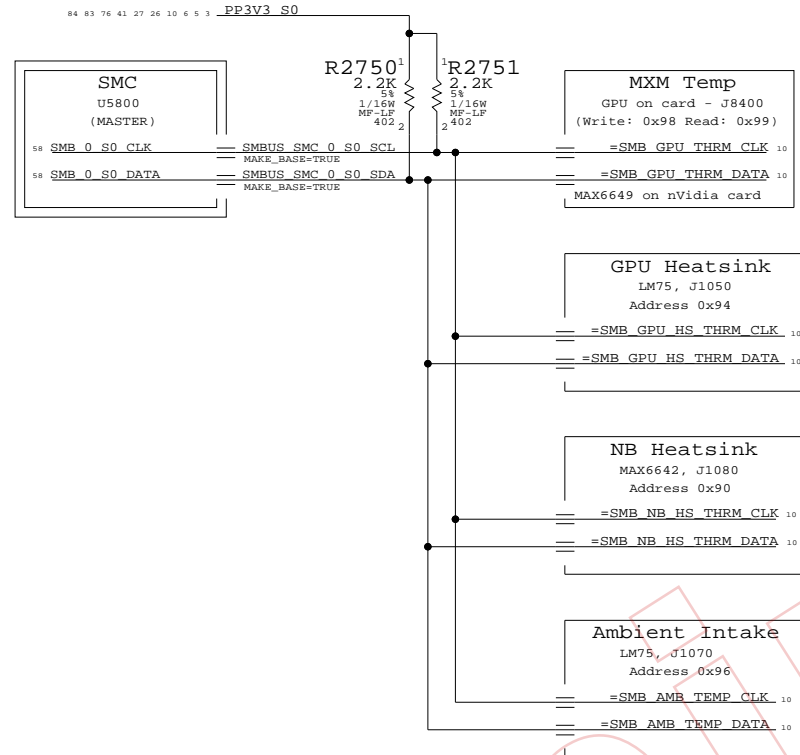
**SB: MISC**  
 SYNC\_MASTER=M50\_DOUG SYNC\_DATE=06/29/2006  
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|                     |      |                |      |
|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 26 OF          | 97   |
| NONE                |      |                |      |

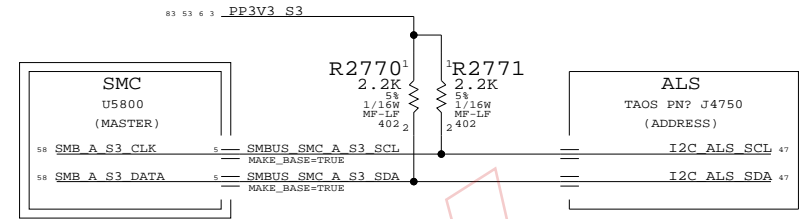
### ICH7-M SMBus Connections



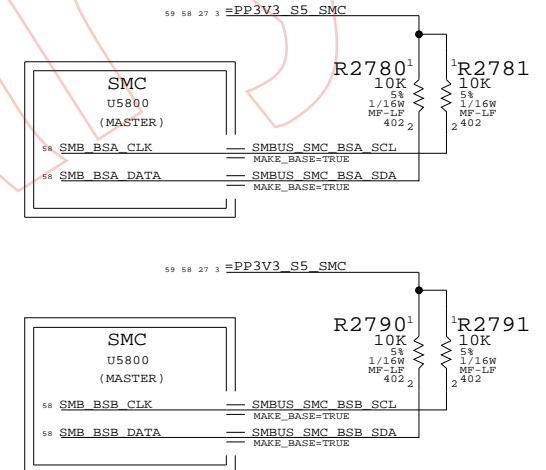
### SMC "0" SMBus Connections



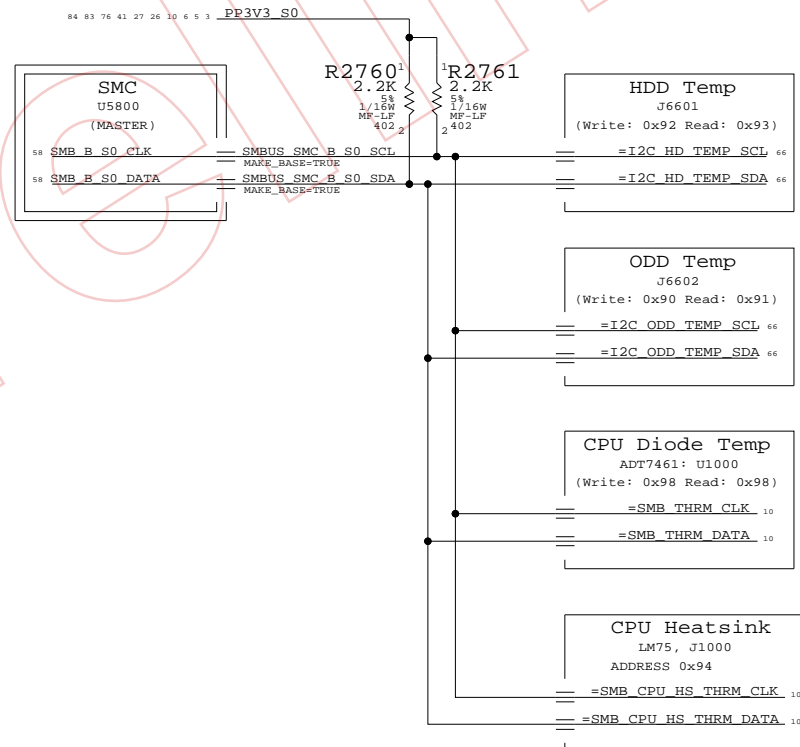
### SMC "A" SMBus Connections



### Unused SMC "Battery A/B" SMBus



### SMC "B" SMBus Connections



### M51 SMBus Connections

SYNC\_MASTER=M51\_DAVE SYNC\_DATE=(MASTER)

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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 27 OF 97       |      |
| NONE                |      |                |      |

# Page Notes

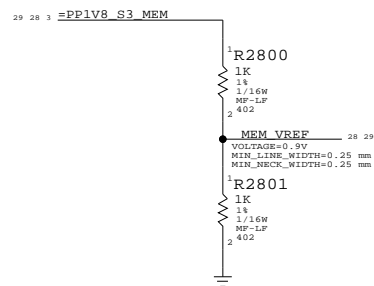
Power aliases required by this page:  
 - =PP1V8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

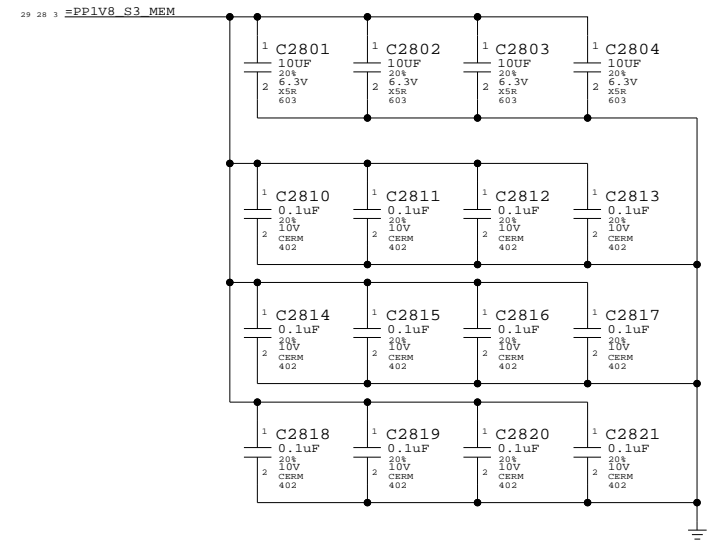
## DDR2 VRef

One 0.1uF per connector



## DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A  
 SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 28 OF          | 97   |
| NONE                |      |                |      |

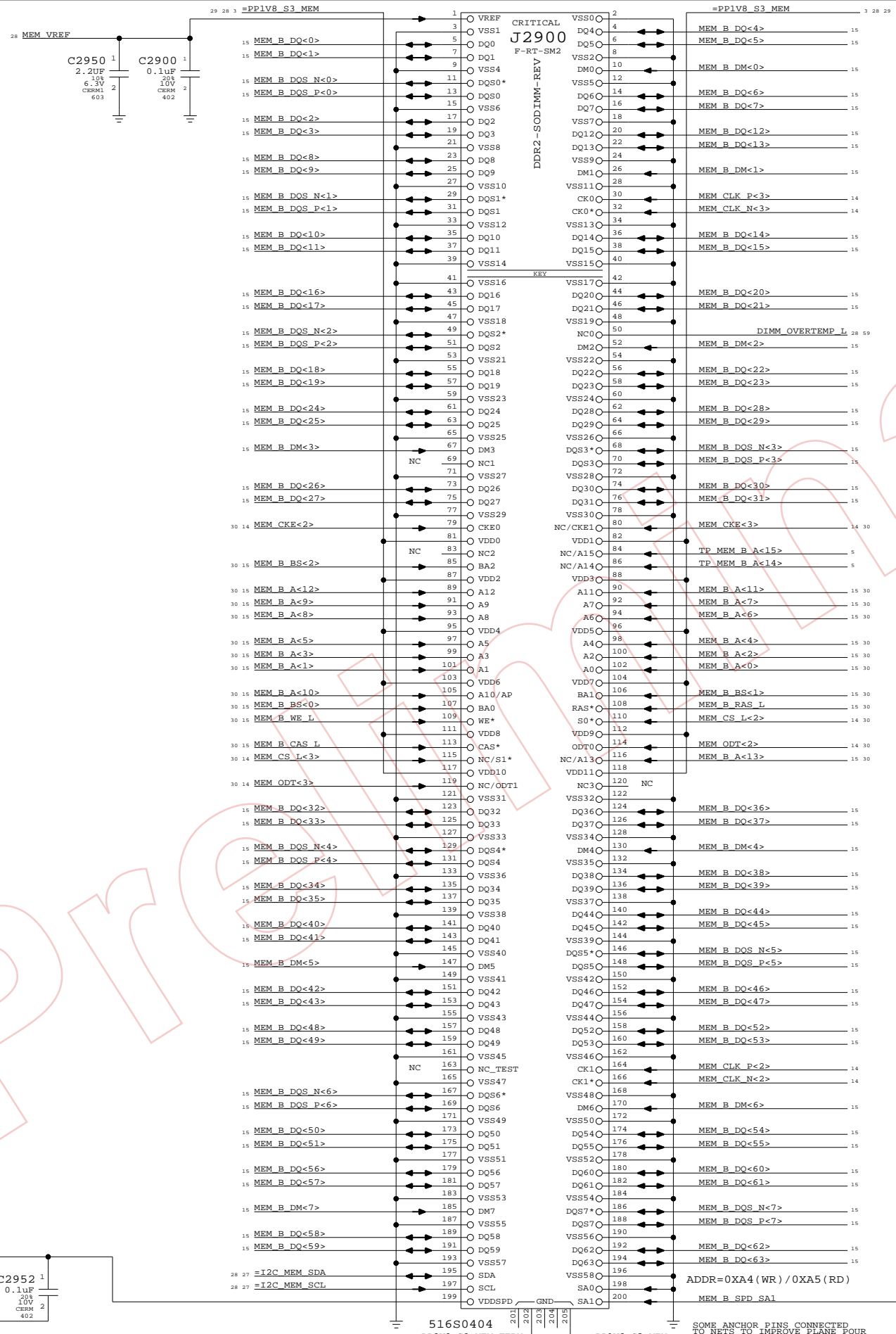
# Page Notes

Power aliases required by this page:  
 - =PP1V8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

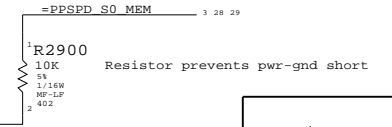
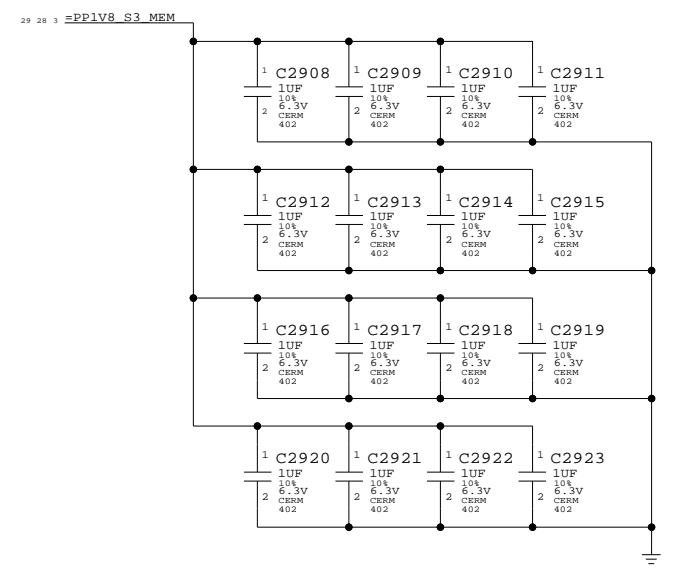
Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

NOTE: This page does not supply VREF.  
 The reference voltage must be provided by another page.



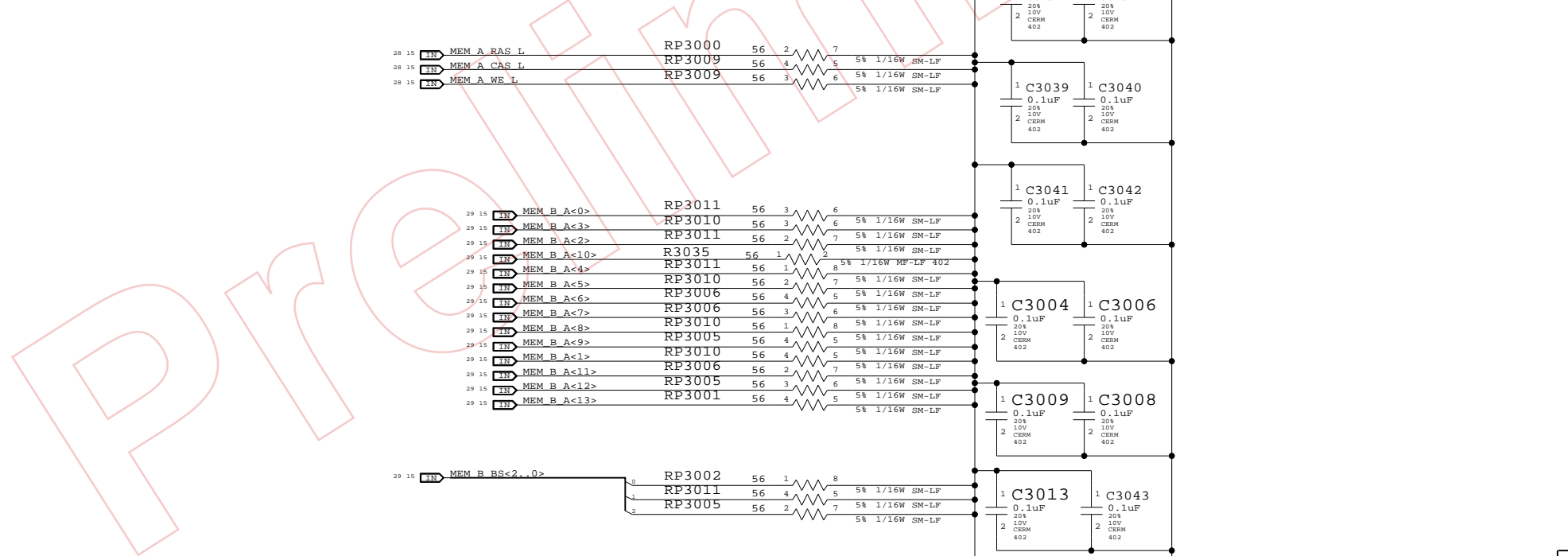
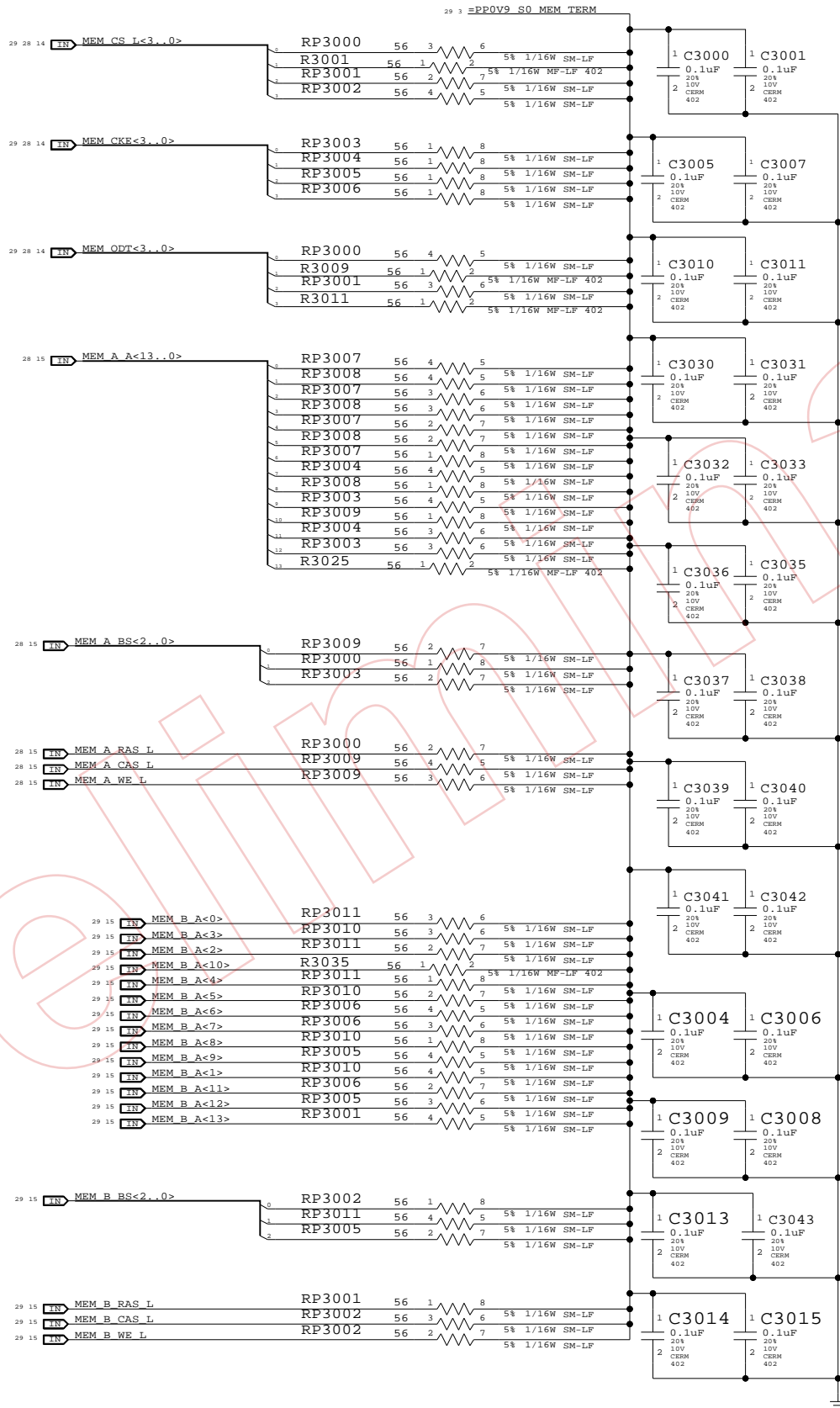
## DDR2 Bypass Caps (For return current)



| DDR2 SO-DIMM Connector B  |                      |
|---|----------------------|
| SYNC_MASTER=M51_HENRY   | SYNC_DATE=06/29/2006 |
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|---------------------|------|----------------|------|
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 29 OF          | 97   |
| NONE                |      |                |      |

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it



**Memory Active Termination**

---

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|---------------------|------------------|-----------------------------------|-------------------|
| APPLE COMPUTER INC. | SIZE<br><b>D</b> | DRAWING NUMBER<br><b>051-7039</b> | REV.<br><b>21</b> |
|                     | SCALE<br>NONE    | SHT<br>30 OF                      | 97                |

Page Notes

Power aliases required by this page:  
 - =PP5V\_S0\_MEMVTT  
 - =PP1V8\_S0\_MEMVTT  
 - =PP0V9\_S0\_MEMVTT\_LDO

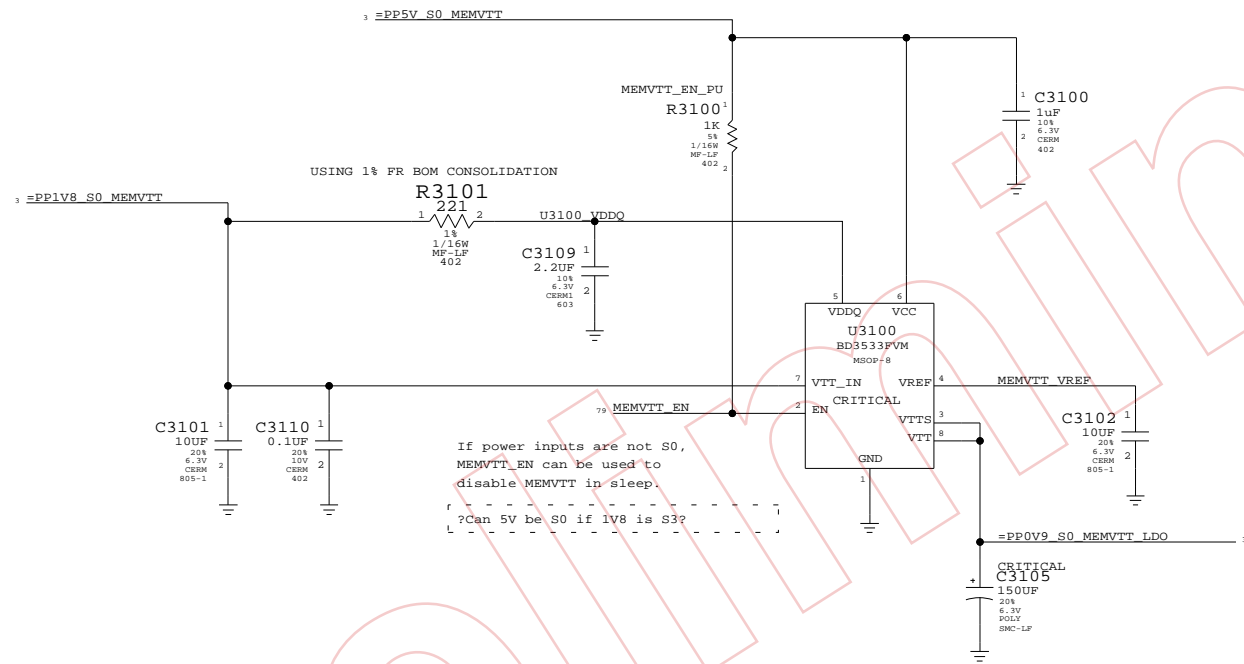
---

Signal aliases required by this page:  
 (NONE)

---

BOM options provided by this page:  
 (NONE)

DDR2 Vtt Regulator



Pre-Announcement

**Memory Vtt Supply**

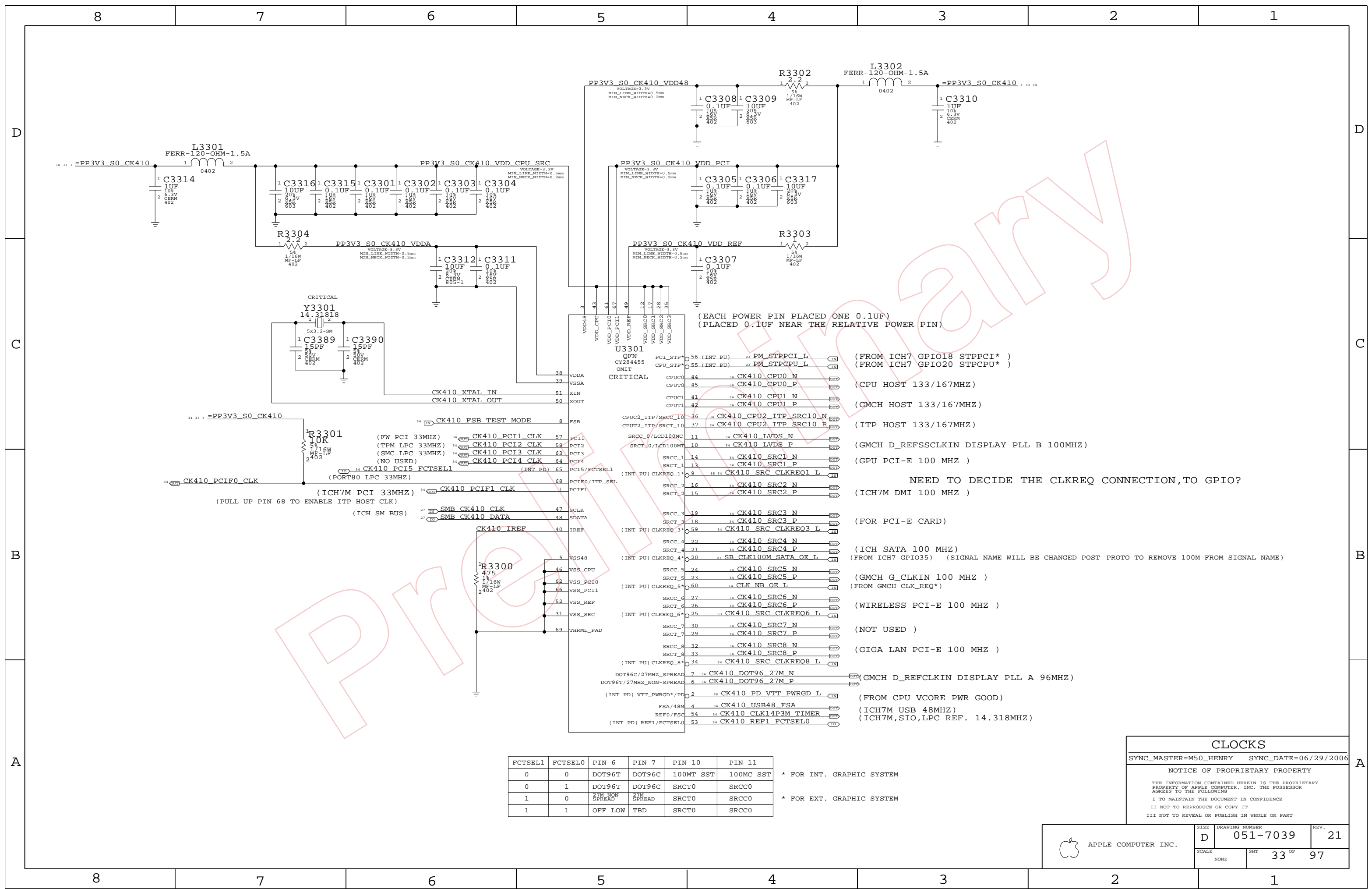
SYNC\_MASTER=M50\_HENRY      SYNC\_DATE=06/29/2006

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|---------------------|------------------|-----------------------------------|-------------------|
| APPLE COMPUTER INC. | SIZE<br><b>D</b> | DRAWING NUMBER<br><b>051-7039</b> | REV.<br><b>21</b> |
|                     | SCALE<br>NONE    | SHT<br>31 OF 97                   |                   |



(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI\* )  
(FROM ICH7 GPIO20 STPCPU\* )

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ )

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ )

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)

(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G\_CLKIN 100 MHZ )  
(FROM GMCH CLK\_REQ\*)

(WIRELESS PCI-E 100 MHZ )

(NOT USED )

(GIGA LAN PCI-E 100 MHZ )

(GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

| FCTSEL1 | FCTSEL0 | PIN 6          | PIN 7      | PIN 10    | PIN 11    |
|---------|---------|----------------|------------|-----------|-----------|
| 0       | 0       | DOT96T         | DOT96C     | 100MT_SST | 100MC_SST |
| 0       | 1       | DOT96T         | DOT96C     | SRCT0     | SRCC0     |
| 1       | 0       | 27M NON SPREAD | 27M SPREAD | SRCT0     | SRCC0     |
| 1       | 1       | OFF LOW        | TBD        | SRCT0     | SRCC0     |

\* FOR INT. GRAPHIC SYSTEM

\* FOR EXT. GRAPHIC SYSTEM

**CLOCKS**

SYNC\_MASTER=M50\_HENRY    SYNC\_DATE=06/29/2006

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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 33 OF 97       |      |
| NONE                |      |                |      |



D

D

C

C

B

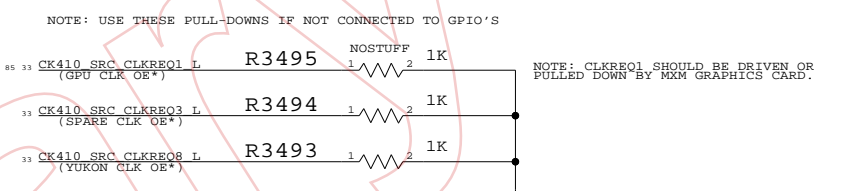
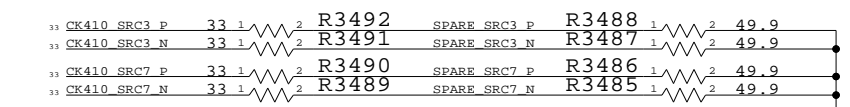
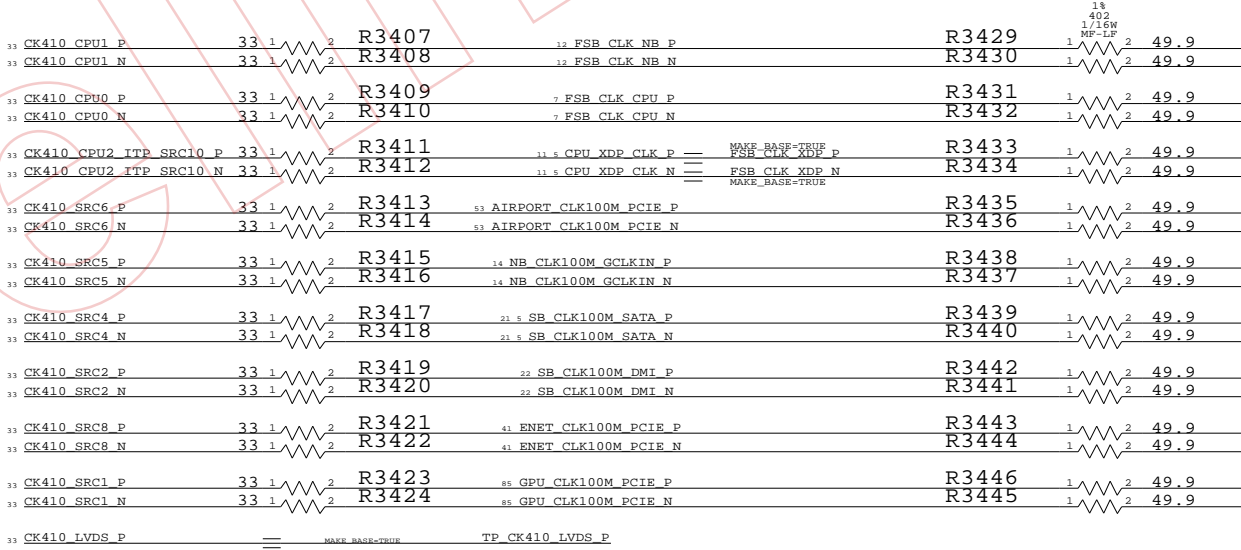
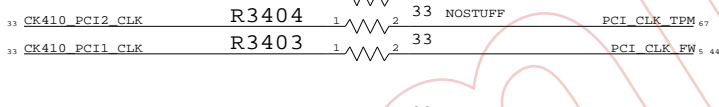
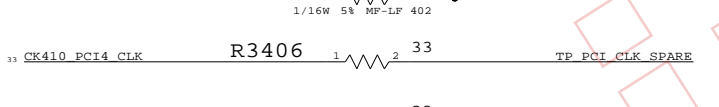
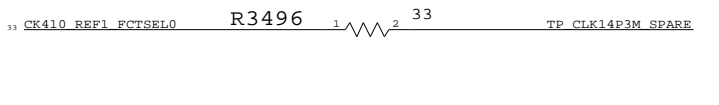
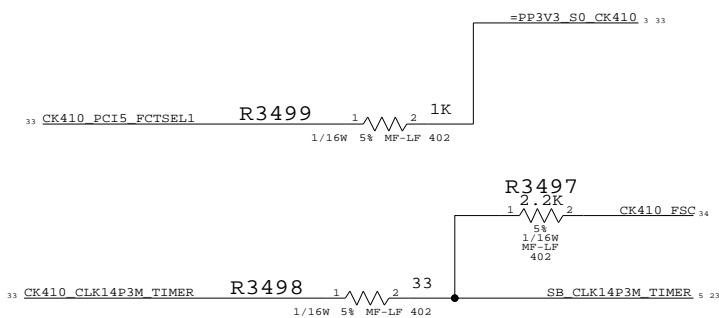
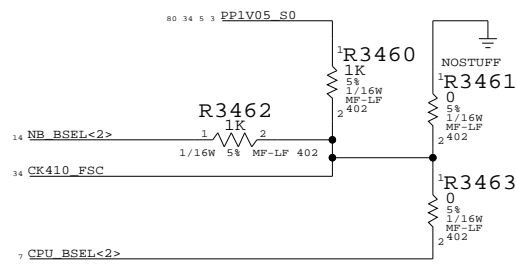
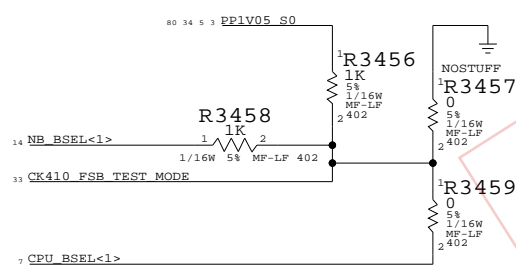
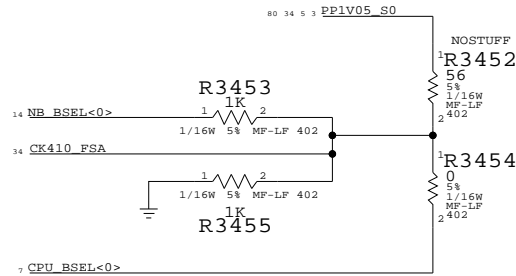
B

A

A

FSB FREQUENCY SELECT:

|                            | STUFF                            | NO STUFF                         |
|----------------------------|----------------------------------|----------------------------------|
| CPU DRIVEN                 | R3452<br>R3453<br>R3454<br>R3455 | R3456<br>R3457<br>R3458<br>R3459 |
| 533MHZ<br>(133MHZ CPU CLK) | R3452<br>R3453<br>R3454<br>R3455 | R3456<br>R3457<br>R3458<br>R3459 |
| 667MHZ<br>(166MHZ CPU CLK) | R3452<br>R3453<br>R3454<br>R3455 | R3456<br>R3457<br>R3458<br>R3459 |



NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

NOTE: CLKREQ1 SHOULD BE DRIVEN OR PULLED DOWN BY MMX GRAPHICS CARD.

CLOCKS: TERMINATIONS

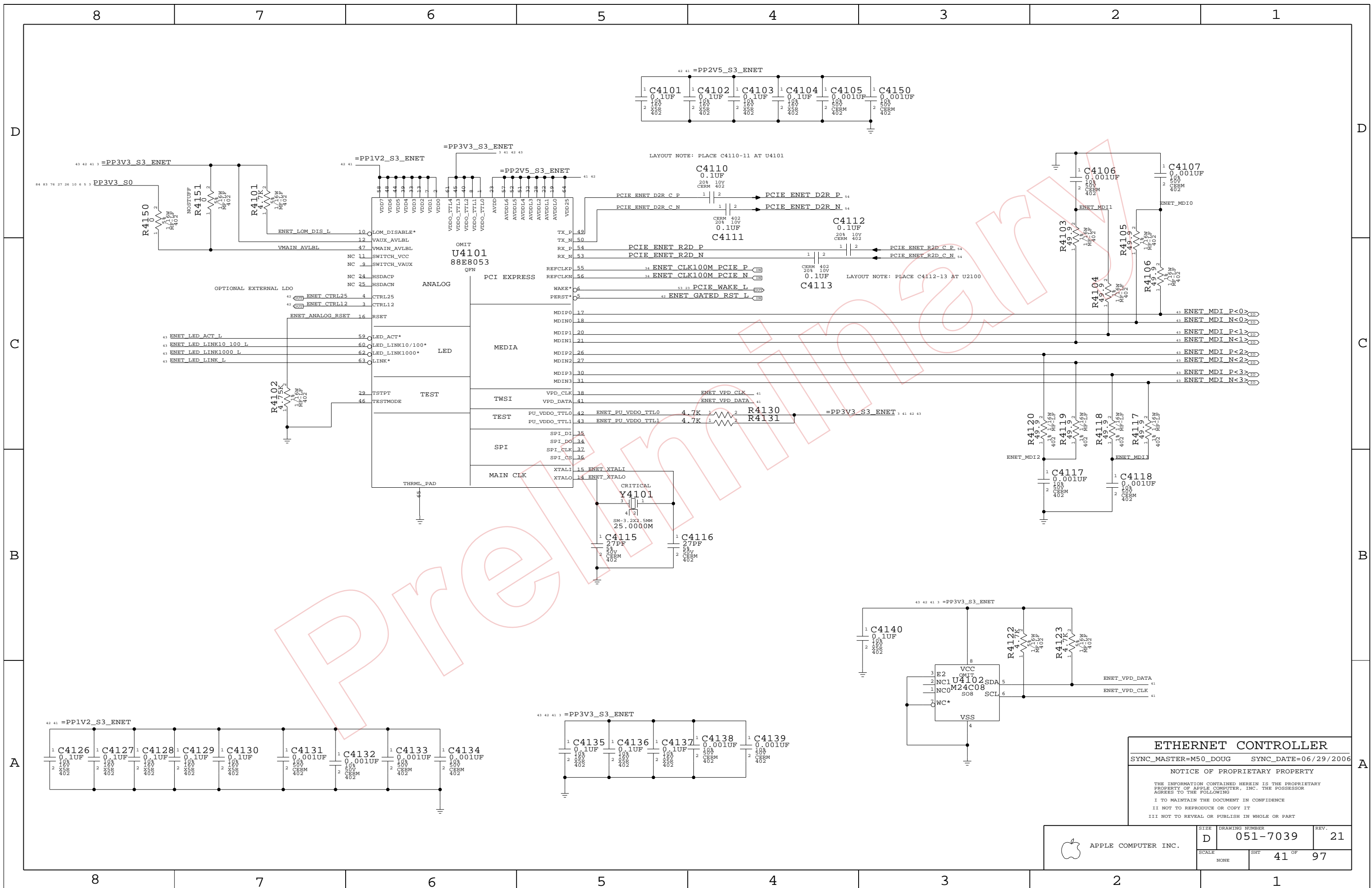
SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

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|                     |      |                |          |
|---------------------|------|----------------|----------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV.     |
|                     | D    | 051-7039       | 21       |
| SCALE               | NONE | SHT            | 34 OF 97 |





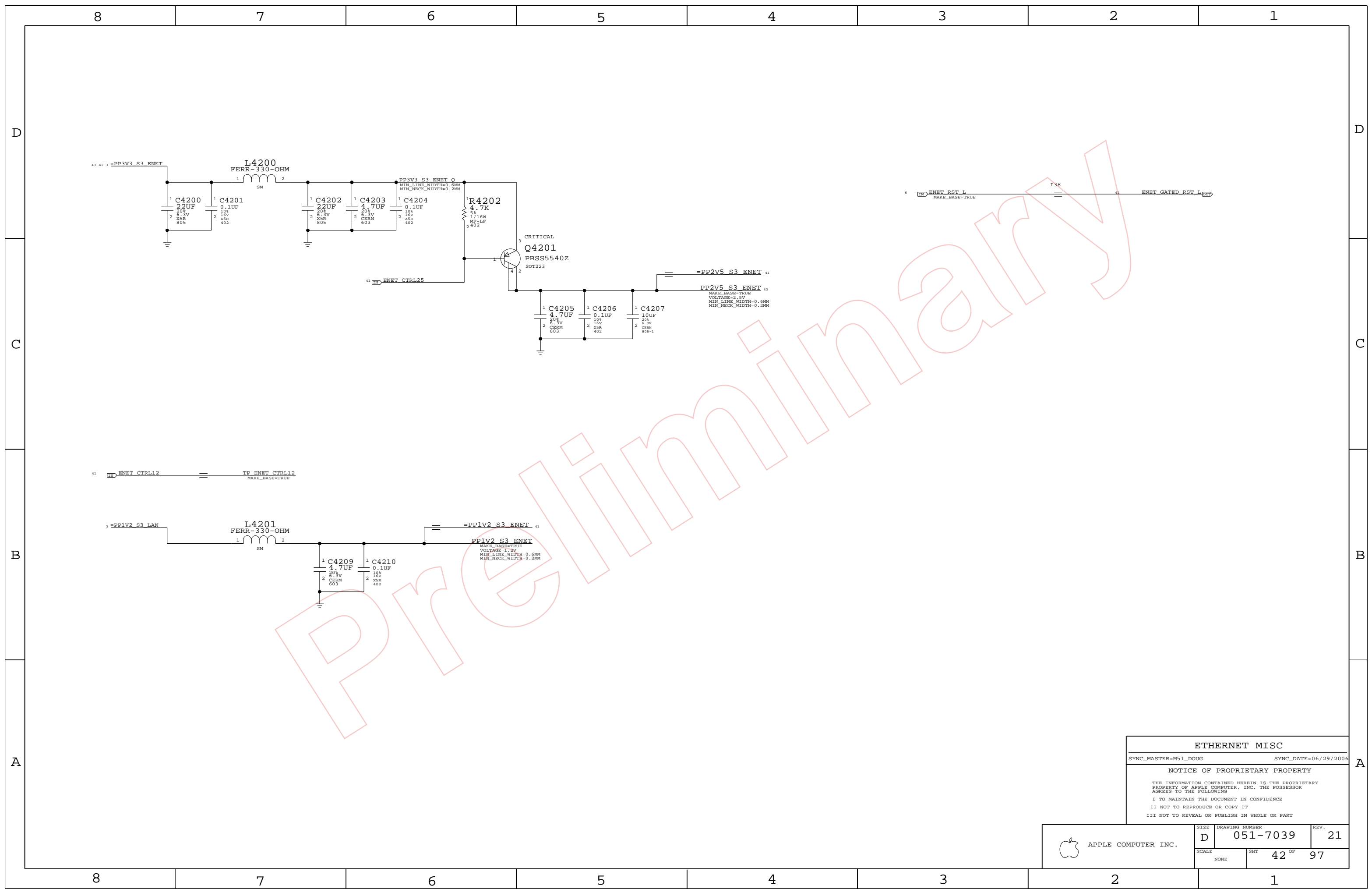
**ETHERNET CONTROLLER**

SYNC\_MASTER=M50\_DOUG SYNC\_DATE=06/29/2006

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| APPLE COMPUTER INC. | SIZE<br><b>D</b> | DRAWING NUMBER<br><b>051-7039</b> | REV.<br><b>21</b> |
|                     | SCALE<br>NONE    | SHEET<br><b>41</b> OF <b>97</b>   |                   |



**ETHERNET MISC**

SYNC\_MASTER=M51\_DOUG      SYNC\_DATE=06/29/2006

**NOTICE OF PROPRIETARY PROPERTY**

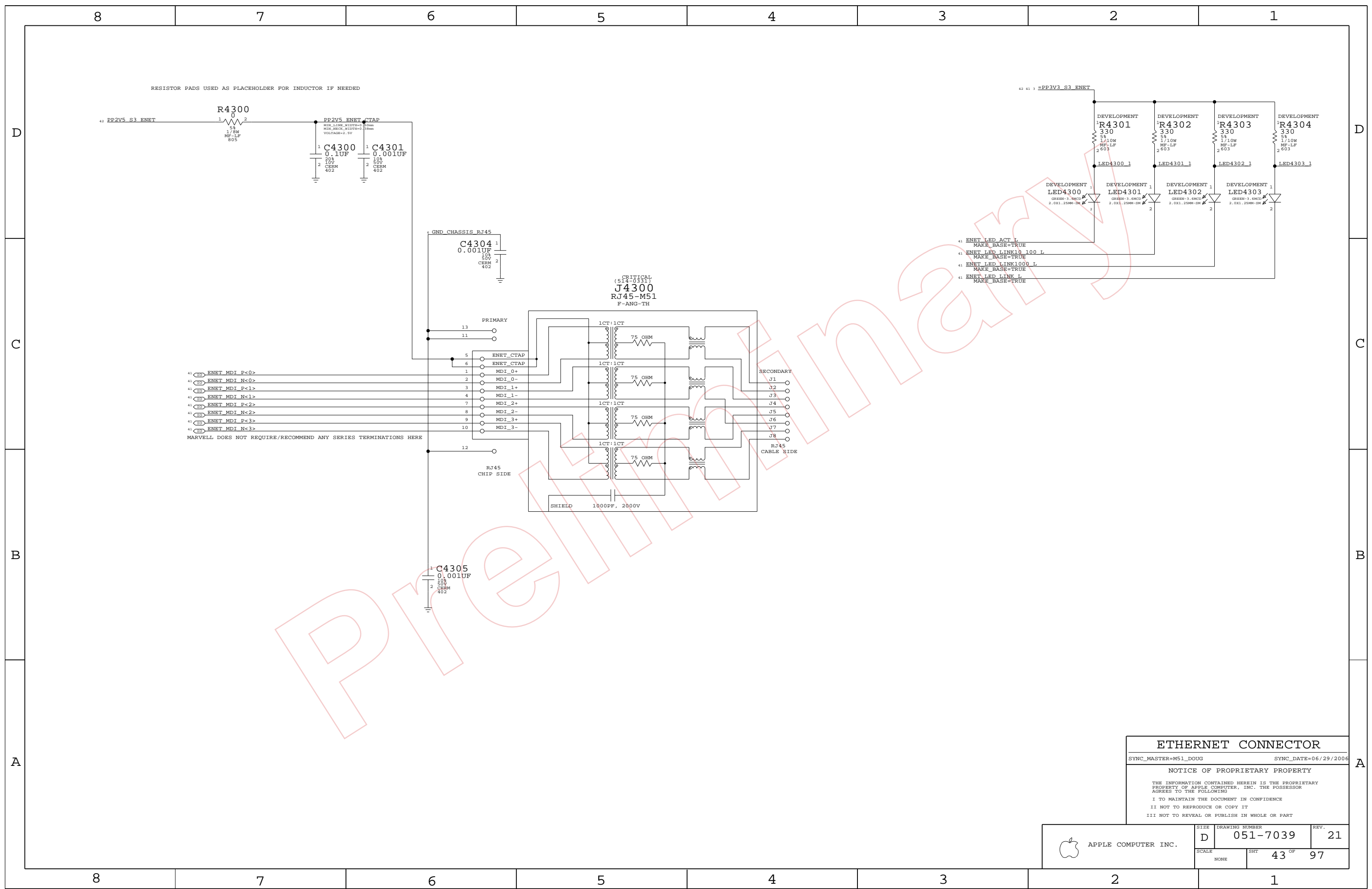
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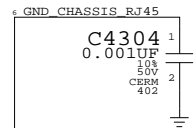
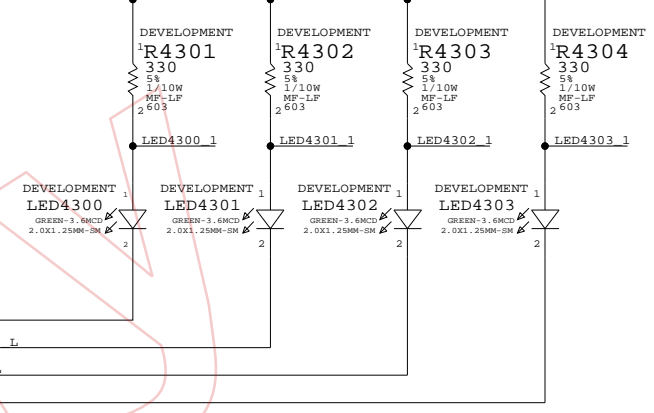
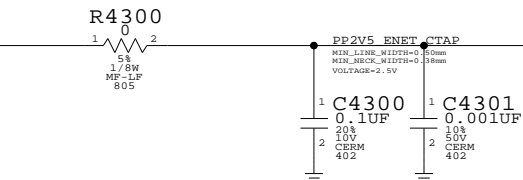
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|---------------------|------------------|-----------------------------------|-------------------|
| APPLE COMPUTER INC. | SIZE<br><b>D</b> | DRAWING NUMBER<br><b>051-7039</b> | REV.<br><b>21</b> |
|                     | SCALE<br>NONE    | SHIT<br><b>42</b> OF <b>97</b>    |                   |

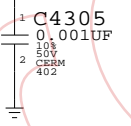
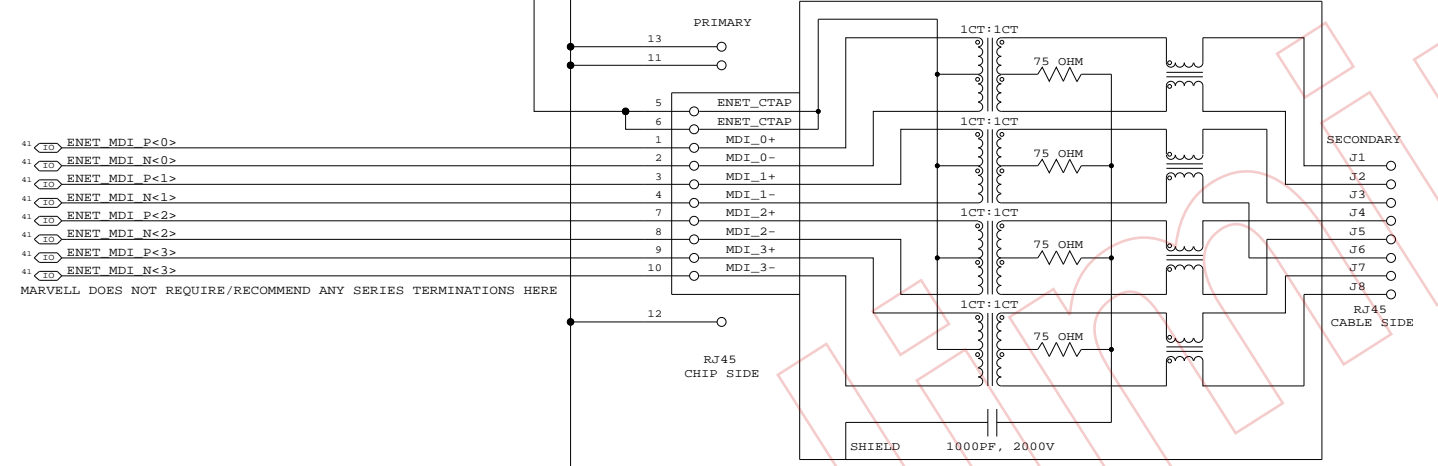


RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED

42 41 3 PP3V3\_S3\_ENET



CRITICAL  
(514-0331)  
J4300  
RJ45-M51  
F-ANG-TH



**ETHERNET CONNECTOR**

SYNC\_MASTER=M51\_DOUG SYNC\_DATE=06/29/2006

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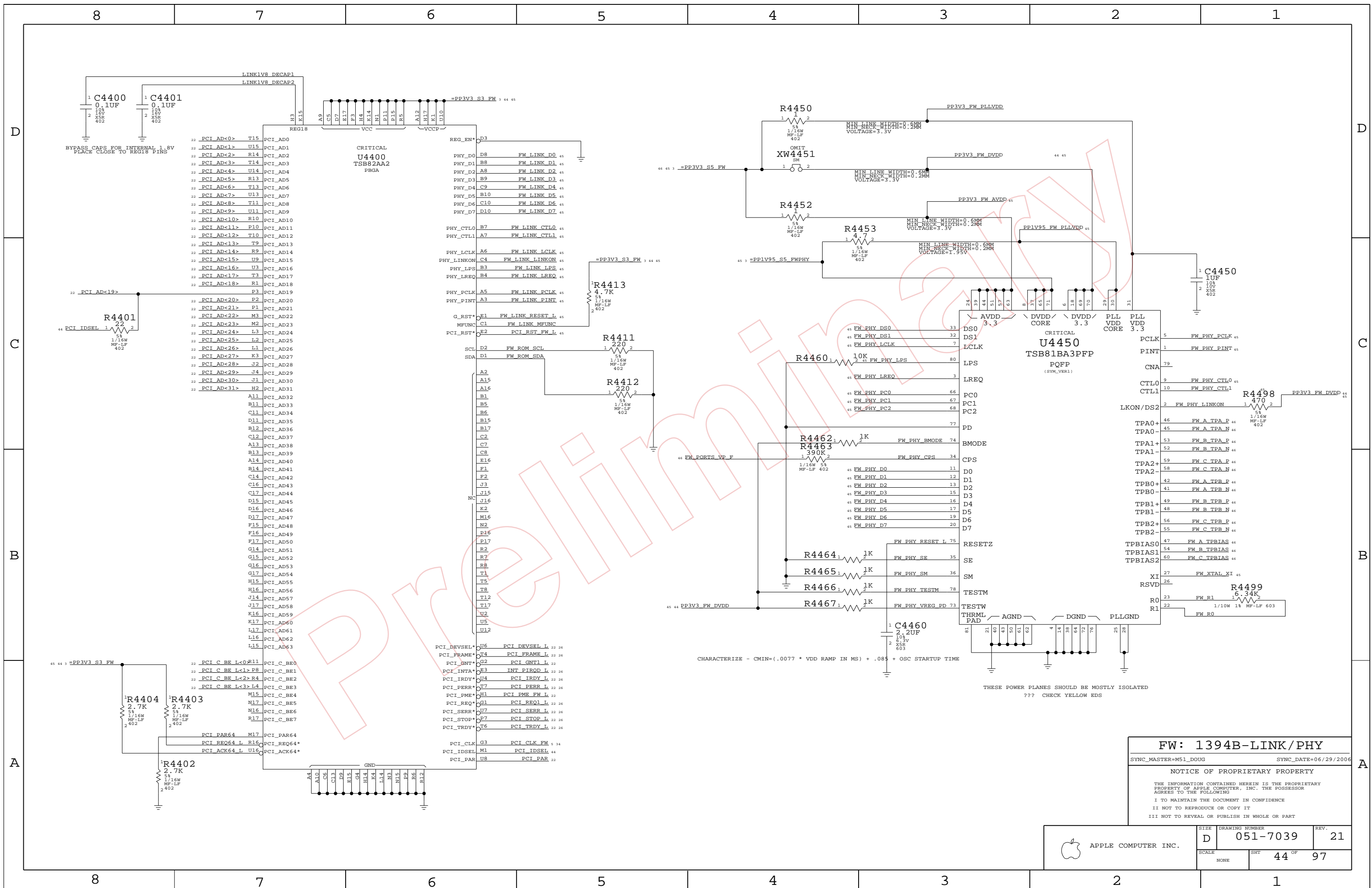
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 43 OF 97       |      |
| NONE                |      |                |      |

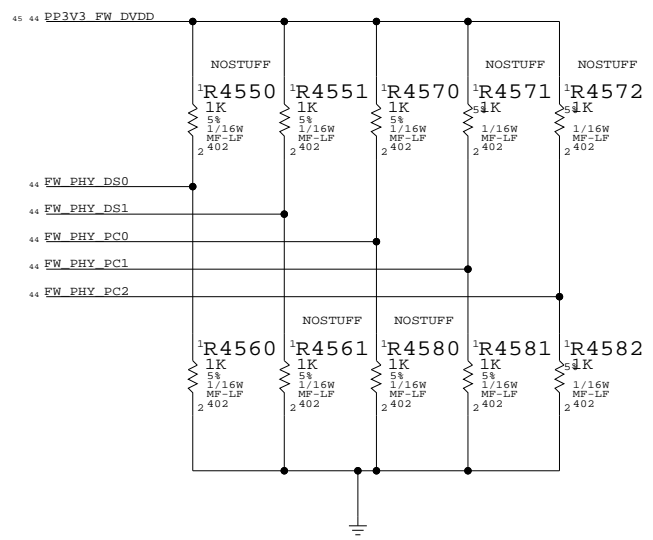


**FW: 1394B-LINK/PHY**  
 SYNC\_MASTER=M51\_D0UG SYNC\_DATE=06/29/2006

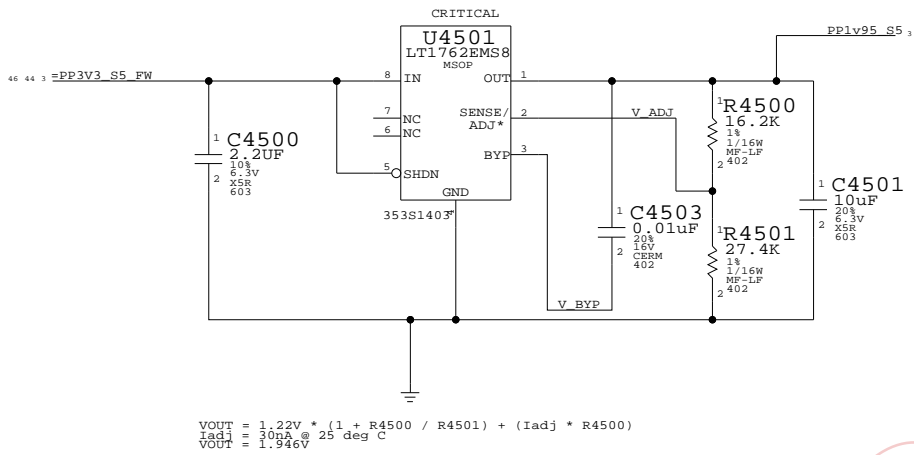
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|                     | SCALE<br>NONE    | SHEET<br><b>44</b> OF <b>97</b>   |                   |

1394 PHY DATA/STROBE AND POWER CLASS OPTIONS



1394 PHY 1.95V REGULATOR



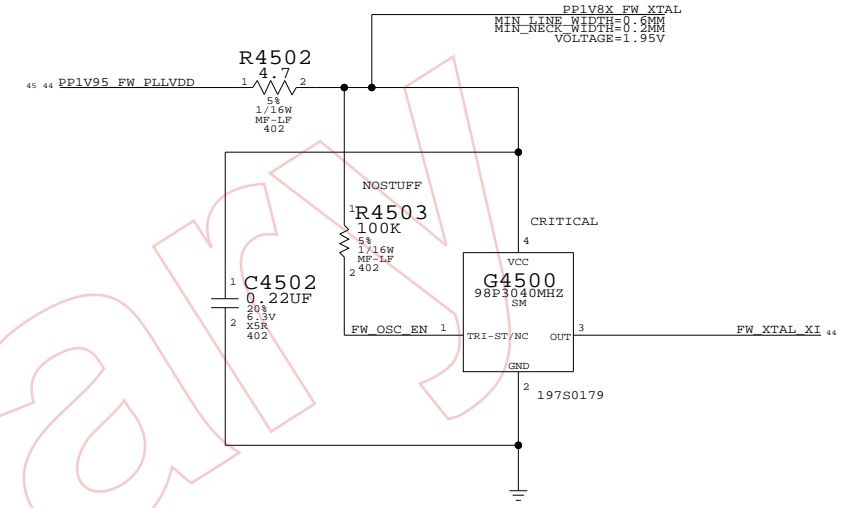
$$V_{OUT} = 1.22V * (1 + R4500 / R4501) + (I_{adj} * R4500)$$

$$I_{adj} = 30\mu A @ 25 \text{ deg C}$$

$$V_{OUT} = 1.946V$$

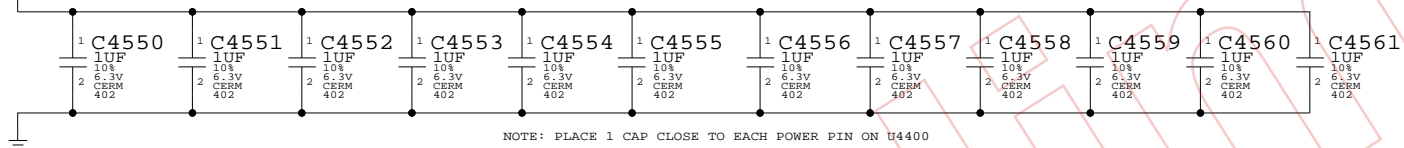
1394 PHY CRYSTAL OSCILLATOR

FIXME!!! CHARACTERIZE TO SEE IF THIS BRINGS US CLOSE ENOUGH TO 1.8V - 4.7 CHOSEN FOR BOM CONSOLIDATION



PP3V3\_S3\_FW

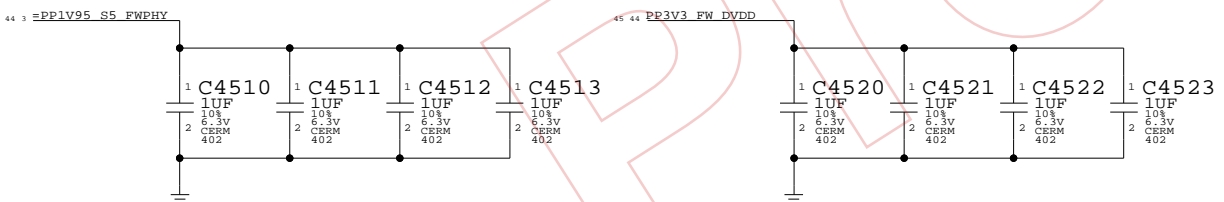
LINK DECOUPLING



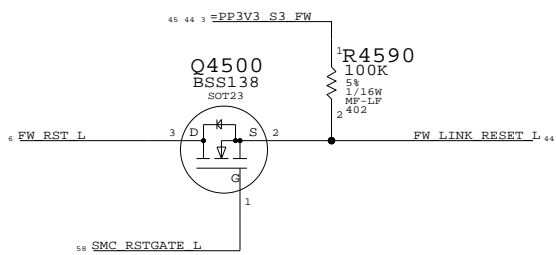
NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4400

- FW\_LINK\_D0 MAKE\_BASE=TRUE == FW\_PHY\_D0
- FW\_LINK\_D1 MAKE\_BASE=TRUE == FW\_PHY\_D1
- FW\_LINK\_D2 MAKE\_BASE=TRUE == FW\_PHY\_D2
- FW\_LINK\_D3 MAKE\_BASE=TRUE == FW\_PHY\_D3
- FW\_LINK\_D4 MAKE\_BASE=TRUE == FW\_PHY\_D4
- FW\_LINK\_D5 MAKE\_BASE=TRUE == FW\_PHY\_D5
- FW\_LINK\_D6 MAKE\_BASE=TRUE == FW\_PHY\_D6
- FW\_LINK\_D7 MAKE\_BASE=TRUE == FW\_PHY\_D7
- FW\_LINK\_CTL0 MAKE\_BASE=TRUE == FW\_PHY\_CTL0
- FW\_LINK\_CTL1 MAKE\_BASE=TRUE == FW\_PHY\_CTL1
- FW\_LINK\_LCLK MAKE\_BASE=TRUE == FW\_PHY\_LCLK
- FW\_LINK\_LPS MAKE\_BASE=TRUE == FW\_PHY\_LPS
- FW\_LINK\_LREQ MAKE\_BASE=TRUE == FW\_PHY\_LREQ
- FW\_LINK\_PCLK MAKE\_BASE=TRUE == FW\_PHY\_PCLK
- FW\_LINK\_LINKON MAKE\_BASE=TRUE == FW\_PHY\_LINKON
- FW\_LINK\_PINT MAKE\_BASE=TRUE == FW\_PHY\_PINT

PHY DECOUPLING



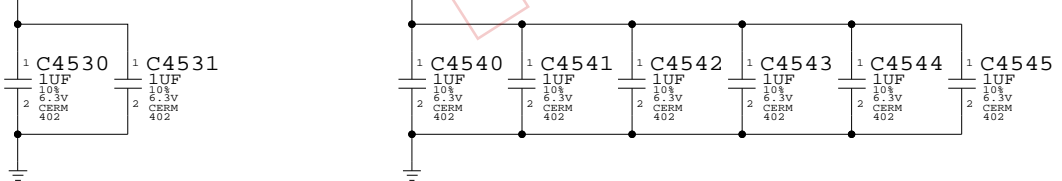
1394 LINK POWER ON RESET AND PCI RESET



NOTE: 1% FOR BOM CONSOLIDATION (APPLIED TO M50)  
NOTE: R SHOULD BE CHOSEN TO PREVENT OVERSHOOT

PPIV95\_FW\_PLLVDD

PP3V3\_FW\_AVDD



NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4450

**FW: 1394B MISC**

SYNC\_MASTER=M51\_DOUG SYNC\_DATE=06/29/2006

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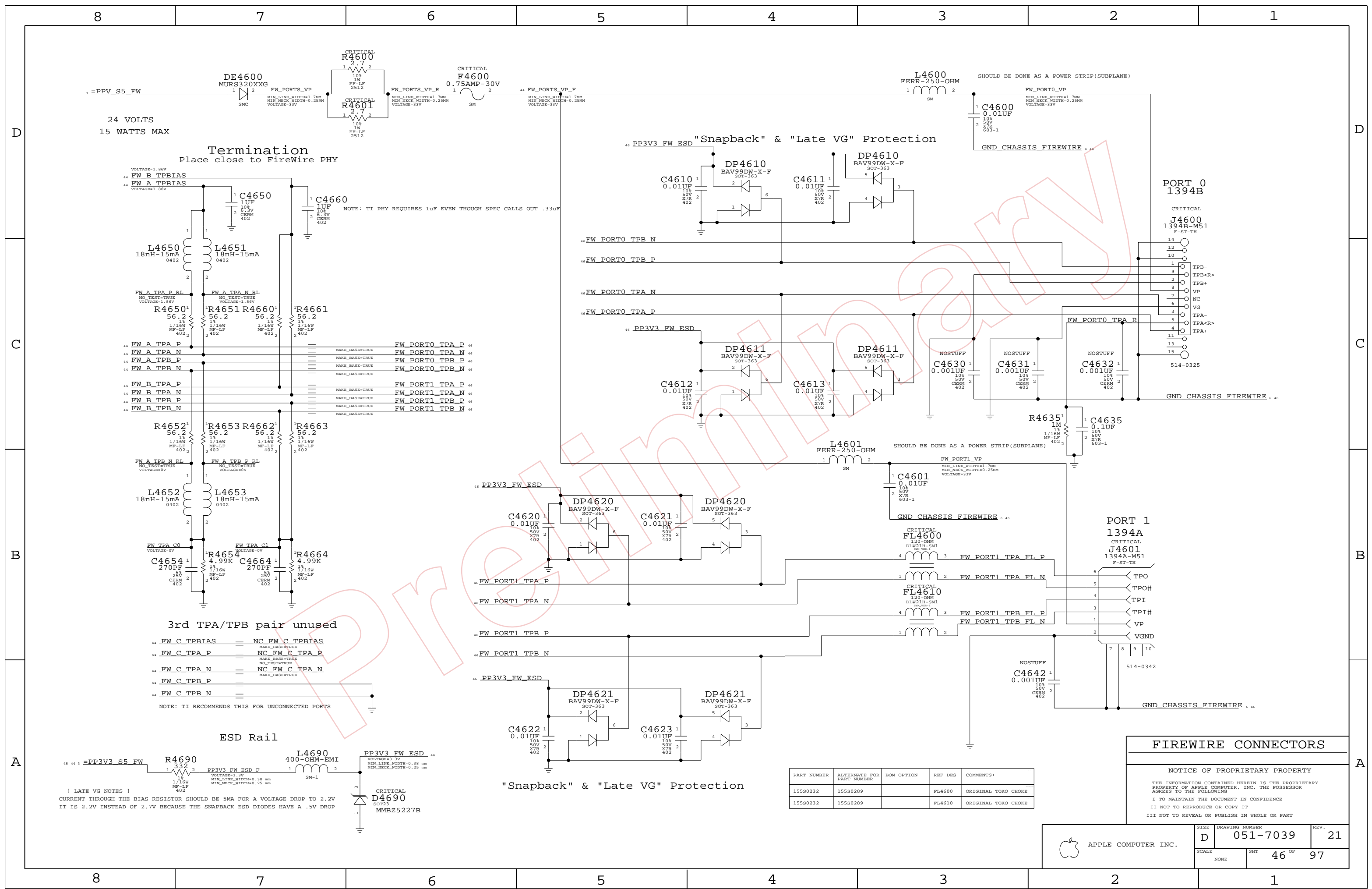
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 45 OF          | 97   |
| NONE                |      |                |      |



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS            |
|-------------|---------------------------|------------|---------|---------------------|
| 15580232    | 15580289                  |            | FL4600  | ORIGINAL TOKO CHOKE |
| 15580232    | 15580289                  |            | FL4610  | ORIGINAL TOKO CHOKE |

**FIREWIRE CONNECTORS**

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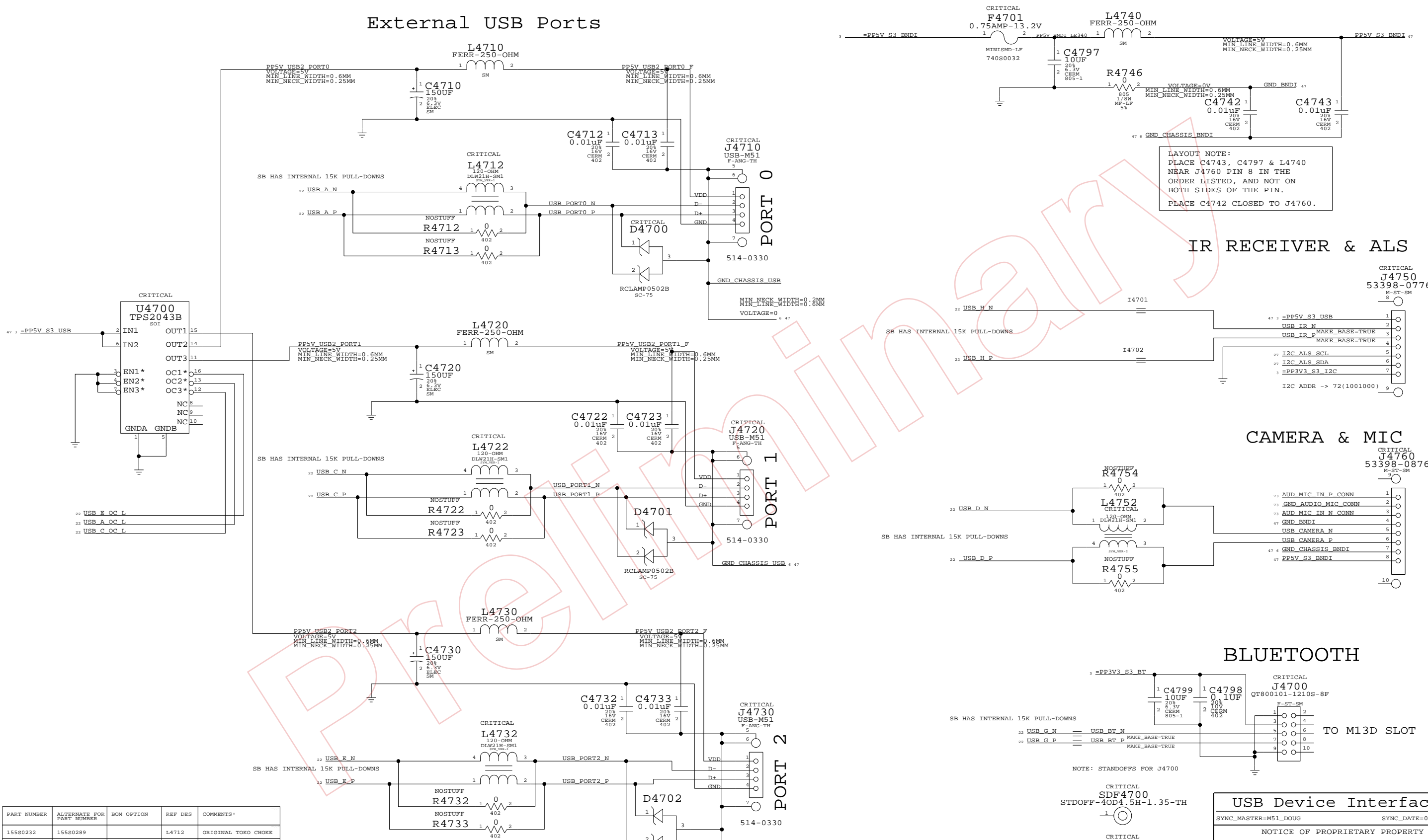
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 46 OF          | 97   |
| NONE                |      |                |      |

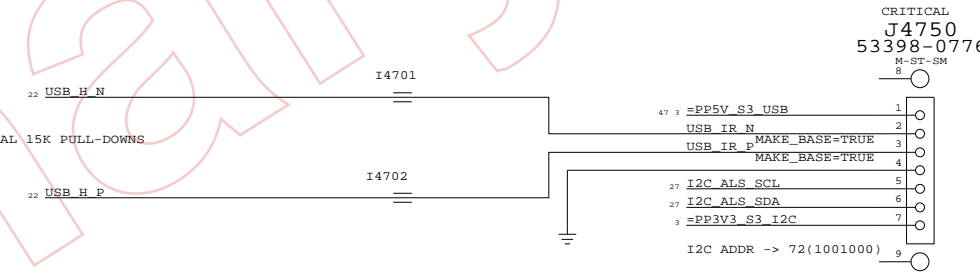


# External USB Ports

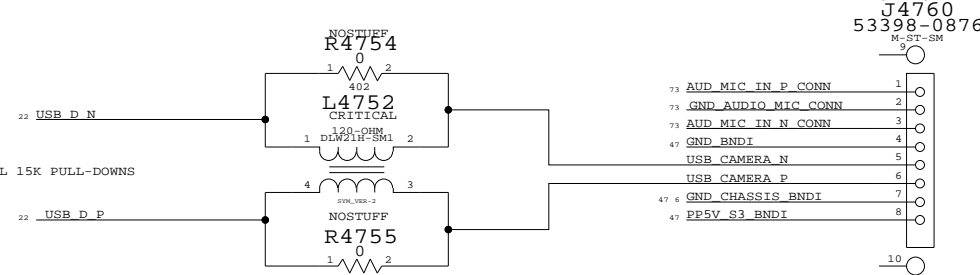


LAYOUT NOTE:  
PLACE C4743, C4797 & L4740  
NEAR J4760 PIN 8 IN THE  
ORDER LISTED, AND NOT ON  
BOTH SIDES OF THE PIN.  
PLACE C4742 CLOSED TO J4760.

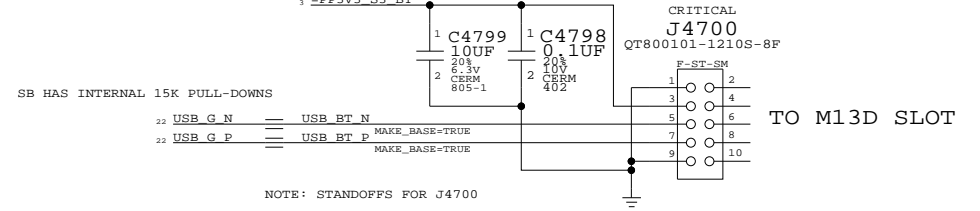
## IR RECEIVER & ALS



## CAMERA & MIC



## BLUETOOTH



| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:           |
|-------------|---------------------------|------------|---------|---------------------|
| 155S0232    | 155S0289                  |            | L4712   | ORIGINAL TOKO CHOKE |
| 155S0232    | 155S0289                  |            | L4722   | ORIGINAL TOKO CHOKE |
| 155S0232    | 155S0289                  |            | L4732   | ORIGINAL TOKO CHOKE |
| 155S0232    | 155S0289                  |            | L4752   | ORIGINAL TOKO CHOKE |

USB Device Interfaces

SYNC\_MASTER=M51\_D0UG SYNC\_DATE=06/29/2006

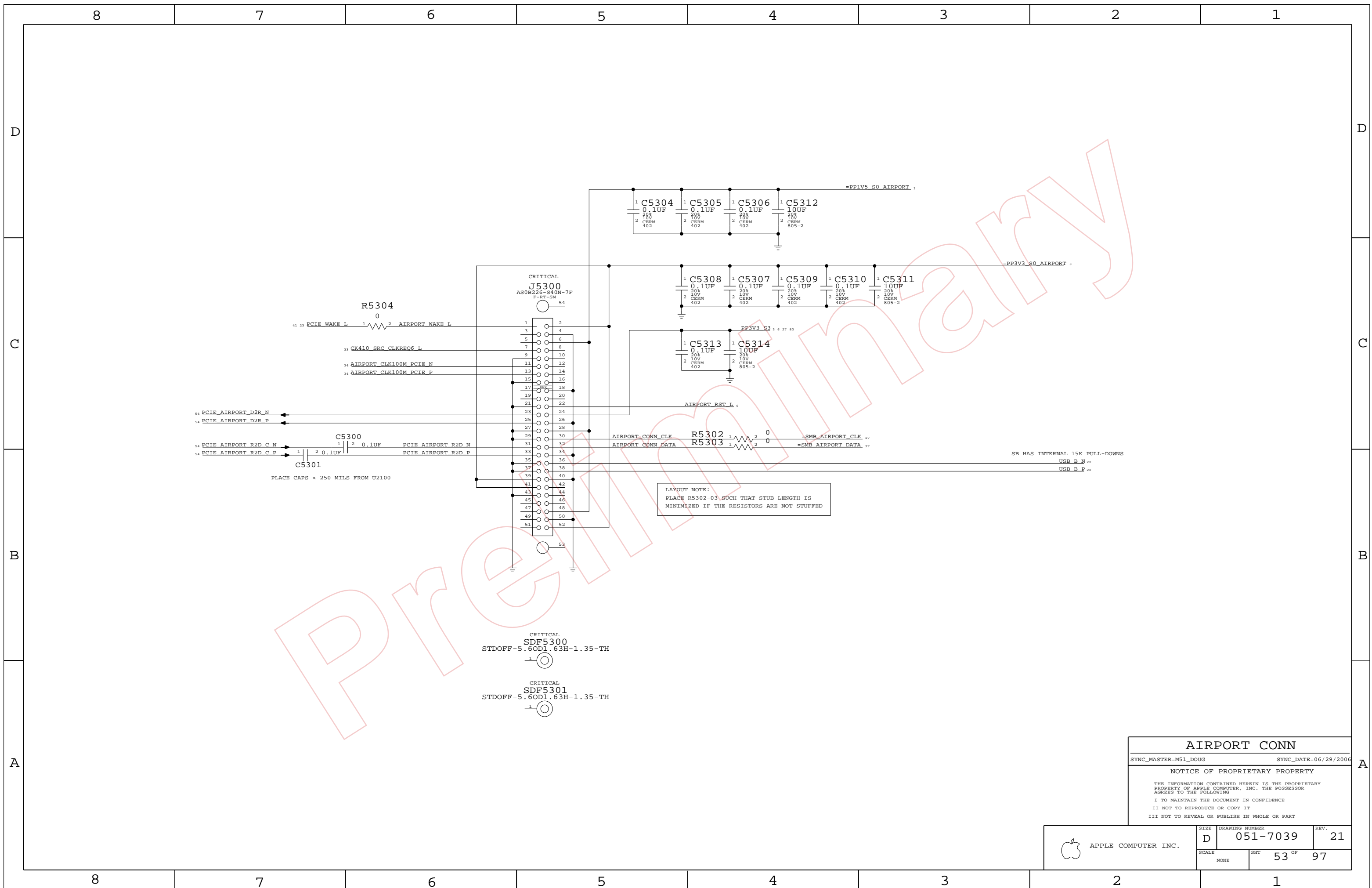
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PROTOTYPE

LAYOUT NOTE:  
 PLACE R5302-03 SUCH THAT STUB LENGTH IS  
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

SB HAS INTERNAL 15K PULL-DOWNS  
 USB\_B\_N 22  
 USB\_B\_P 22

CRITICAL  
 SDF5300  
 STDOFF-5.60D1.63H-1.35-TH

CRITICAL  
 SDF5301  
 STDOFF-5.60D1.63H-1.35-TH

**AIRPORT CONN**

SYNC\_MASTER=M51\_DOUG      SYNC\_DATE=06/29/2006

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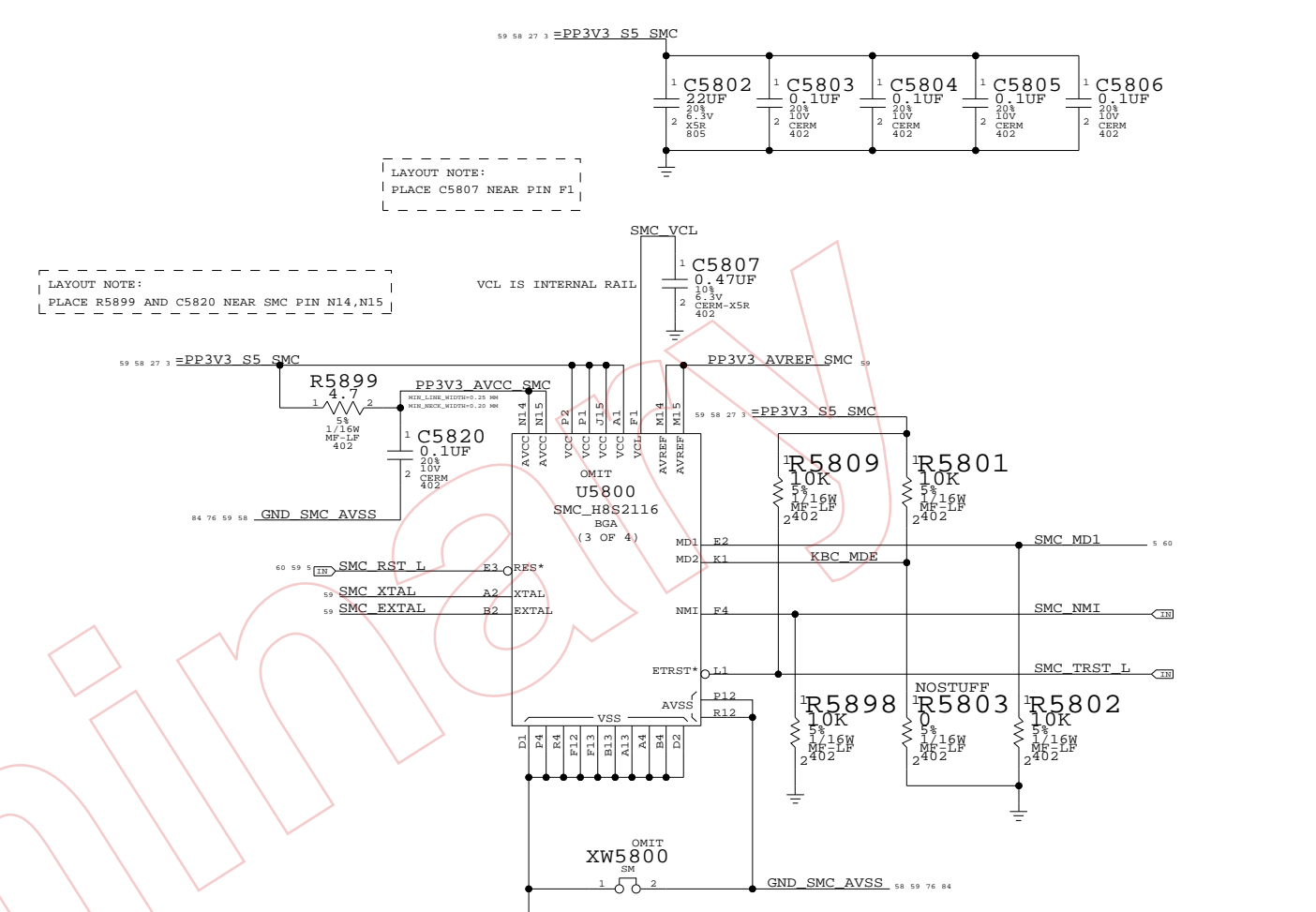
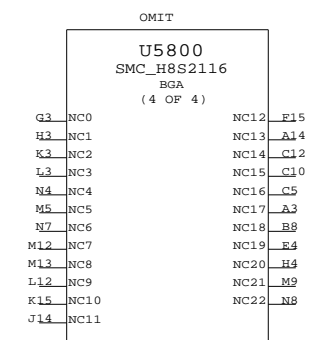
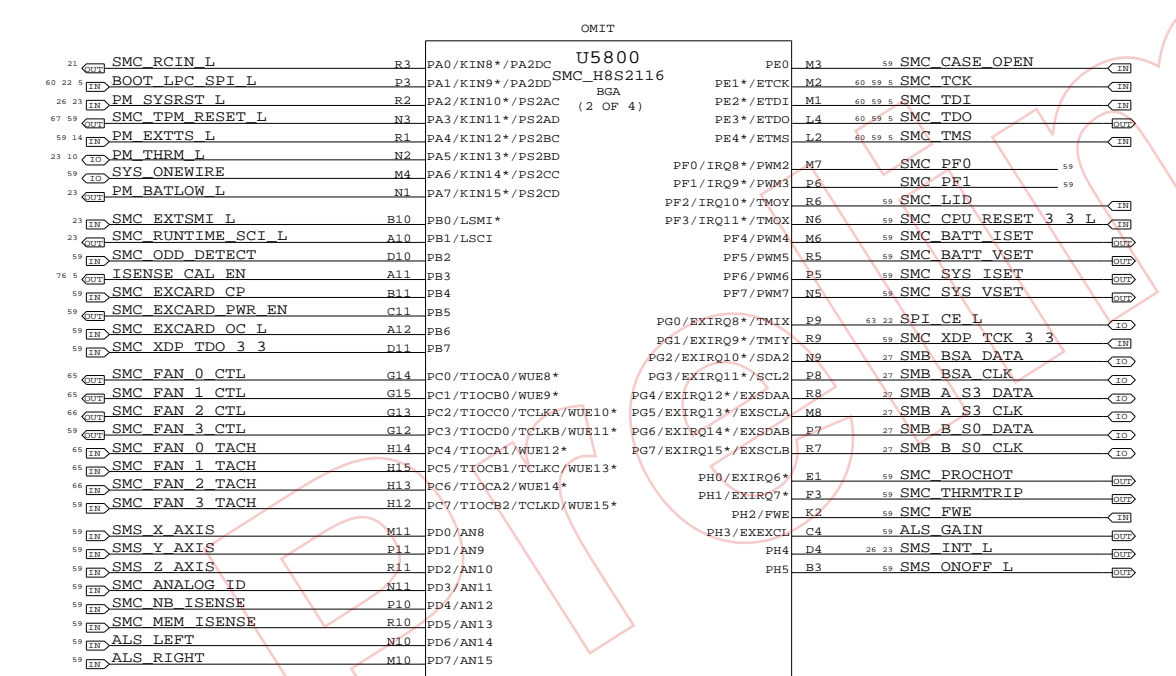
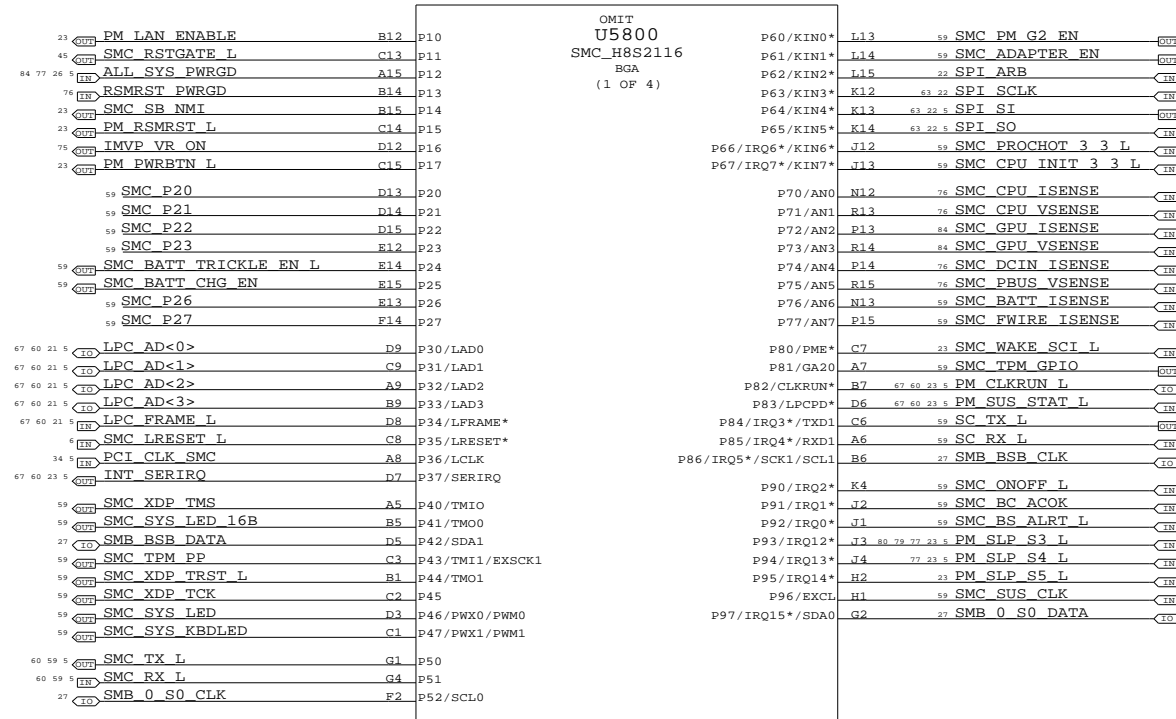
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|                     | SCALE<br>NONE    | SHT<br>53 OF                      | 97                |



UNUSED PINS HAVE THE FORMAT SMC\_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



**SMC**

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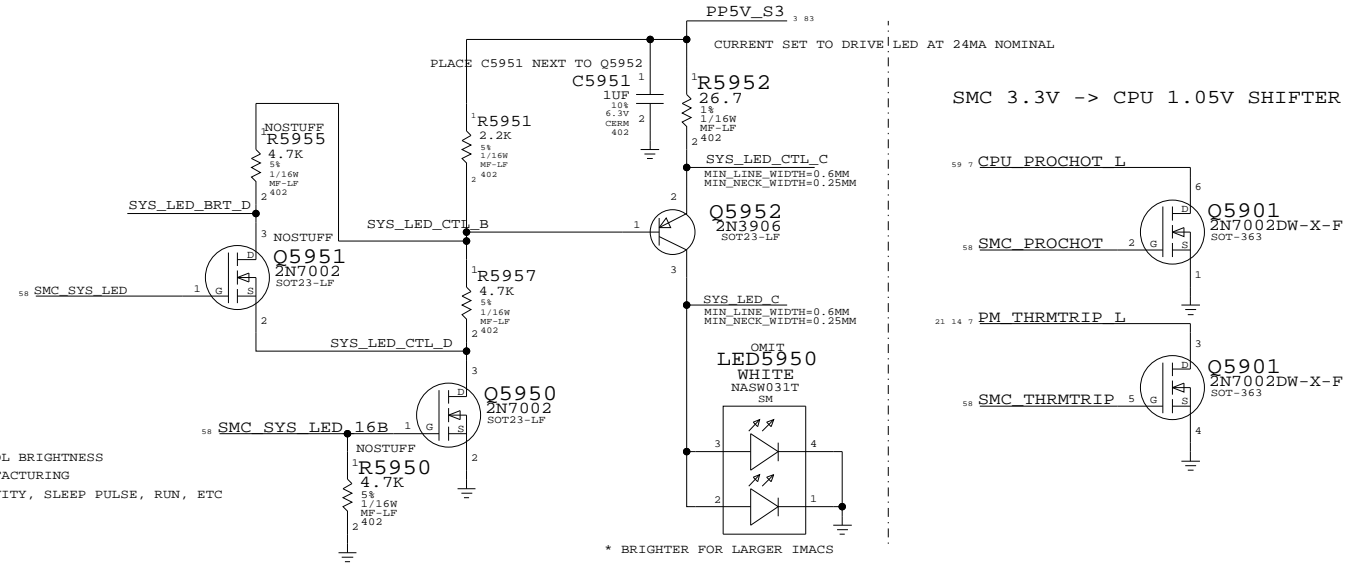
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|-------|----------------|----------|------|
|       | DRAWING NUMBER |          | REV. |
|       | D              | 051-7039 | 21   |
| SCALE |                | SHT      | OF   |
| NONE  |                | 58       | 97   |

D

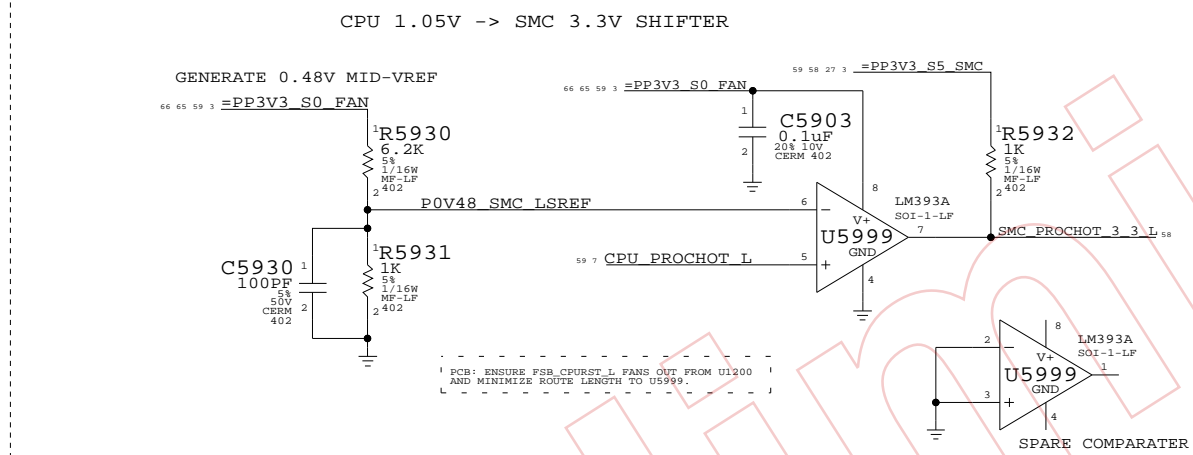
D

**WHITE SYSLED**  
 SMC\_SYS\_LED - PWM, S/W VARIED TO CONTROL BRIGHTNESS  
 ACROSS LARGE VOLUME MANUFACTURING  
 SMC\_SYS\_LED\_16B - PWM, NORMAL LED ACTIVITY, SLEEP PULSE, RUN, ETC



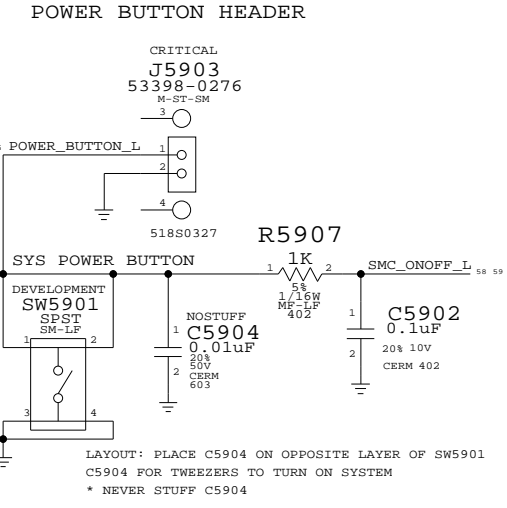
C

C



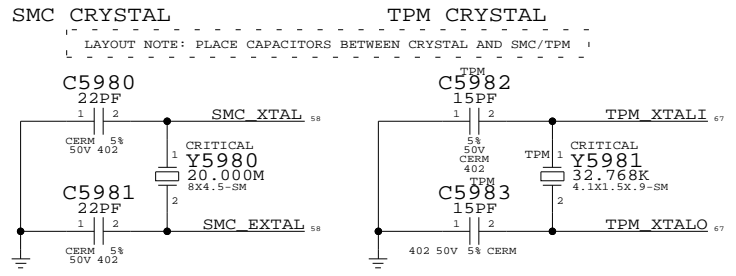
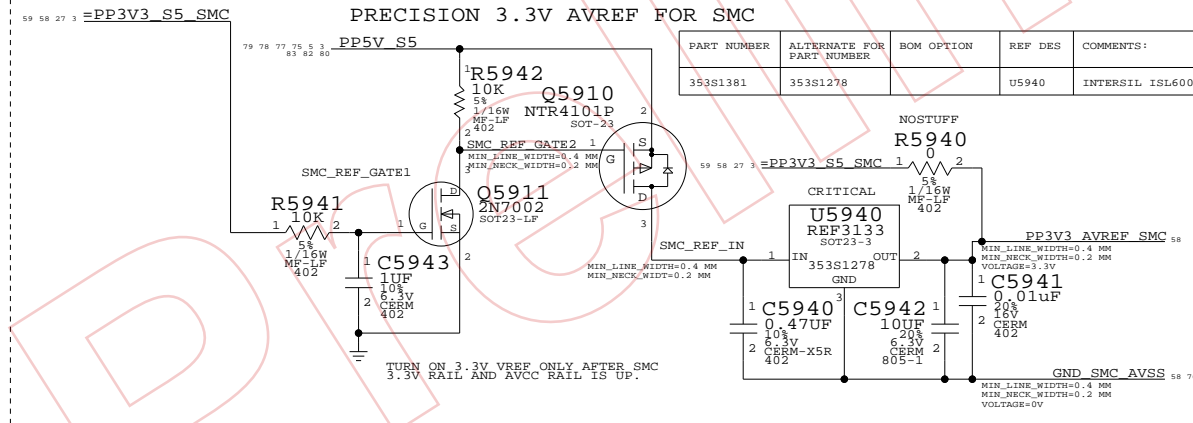
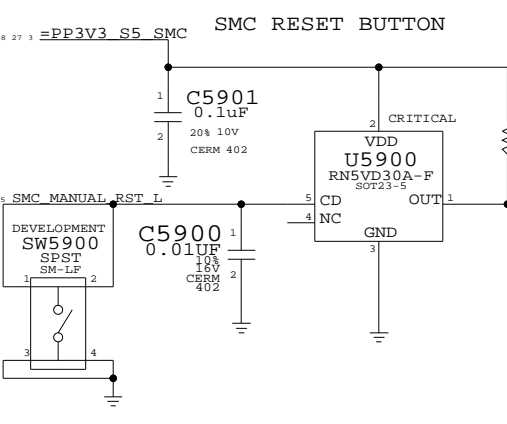
B

B



A

A



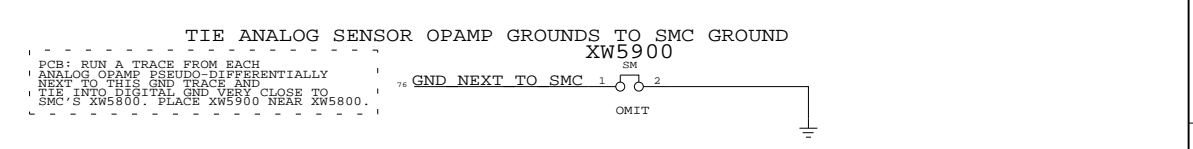
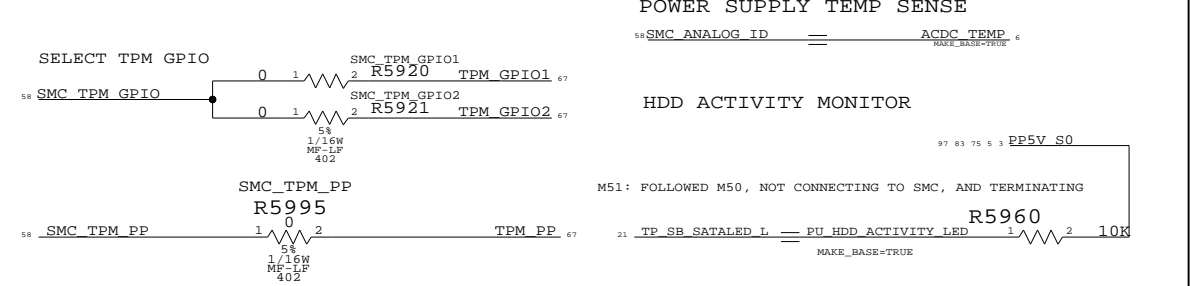
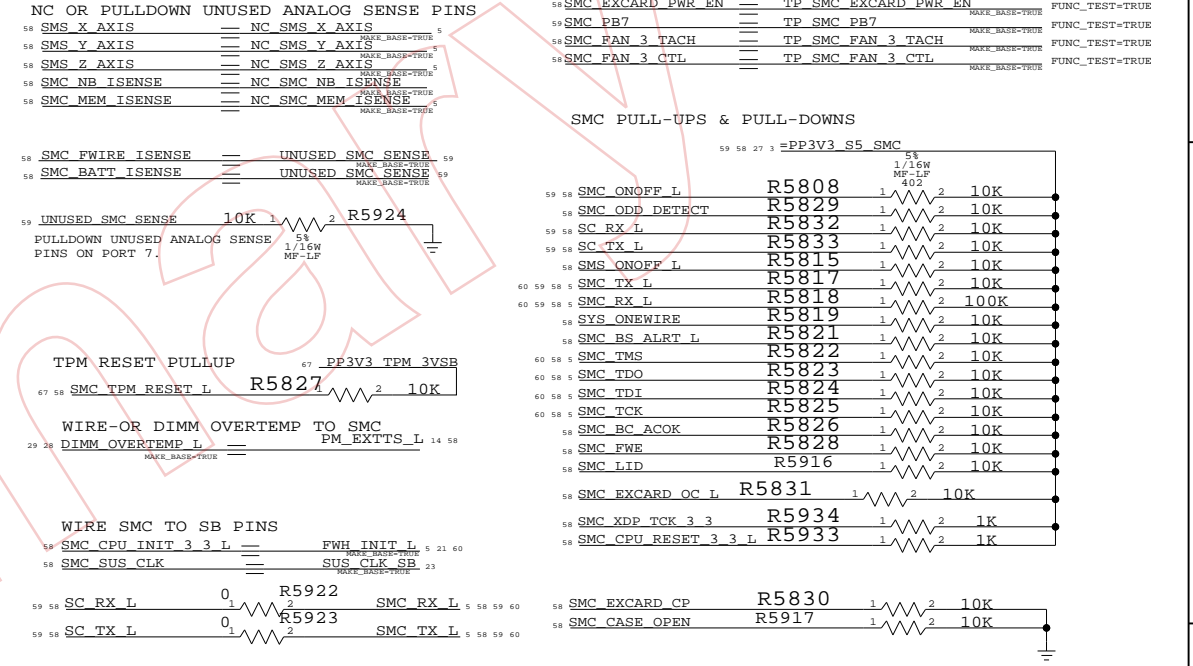
**SMC ALIASES, PULLUPS, AND TESTPOINTS**

**NO-CONNECT UNUSED PINS**

|                       |                          |
|-----------------------|--------------------------|
| SMC P20               | NC SMC P20               |
| SMC P21               | NC SMC P21               |
| SMC P22               | NC SMC P22               |
| SMC P23               | NC SMC P23               |
| SMC P26               | NC SMC P26               |
| SMC P27               | NC SMC P27               |
| SMC BATT ISET         | NC SMC BATT ISET         |
| SMC BATT VSET         | NC SMC BATT VSET         |
| SMC SYS ISET          | NC SMC SYS ISET          |
| SMC SYS VSET          | NC SMC SYS VSET          |
| SMC BATT TRICKLE EN L | NC SMC BATT TRICKLE EN L |
| SMC BATT CHG EN       | NC SMC BATT CHG EN       |
| ALS_GAIN              | NC ALS_GAIN              |

**DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS**

|                   |                      |
|-------------------|----------------------|
| SMC SYS_KBDLED    | TP SMC SYS_KBDLED    |
| SMC PF0           | TP SMC PF0           |
| SMC PM_G2_EN      | TP SMC PM_G2_EN      |
| SMC_ADAPTER_EN    | TP SMC_ADAPTER_EN    |
| ALS_LEFT          | TP ALS_LEFT          |
| ALS_RIGHT         | TP ALS_RIGHT         |
| SMC PF1           | TP SMC PF1           |
| SMC_XDP_TCK       | TP SMC_XDP_TCK       |
| SMC_XDP_TRST_L    | TP SMC_XDP_TRST_L    |
| SMC_PB7           | TP SMC_PB7           |
| SMC_EXCARD_PWR_EN | TP SMC_EXCARD_PWR_EN |
| SMC_PB7           | TP SMC_PB7           |
| SMC_FAN_3_TACH    | TP SMC_FAN_3_TACH    |
| SMC_FAN_3_CTL     | TP SMC_FAN_3_CTL     |



**M51 SPECIFIC: GPU MONITORING SIGNALS**

|                 |      |                |
|-----------------|------|----------------|
| SMC_XDP_TMS     | I327 | MXM_AC_BATT_L  |
| SMC_XDP_TDO_3_3 | I328 | GPU_OVERTEMP_L |

**SMC & TPM SUPPORT**

SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

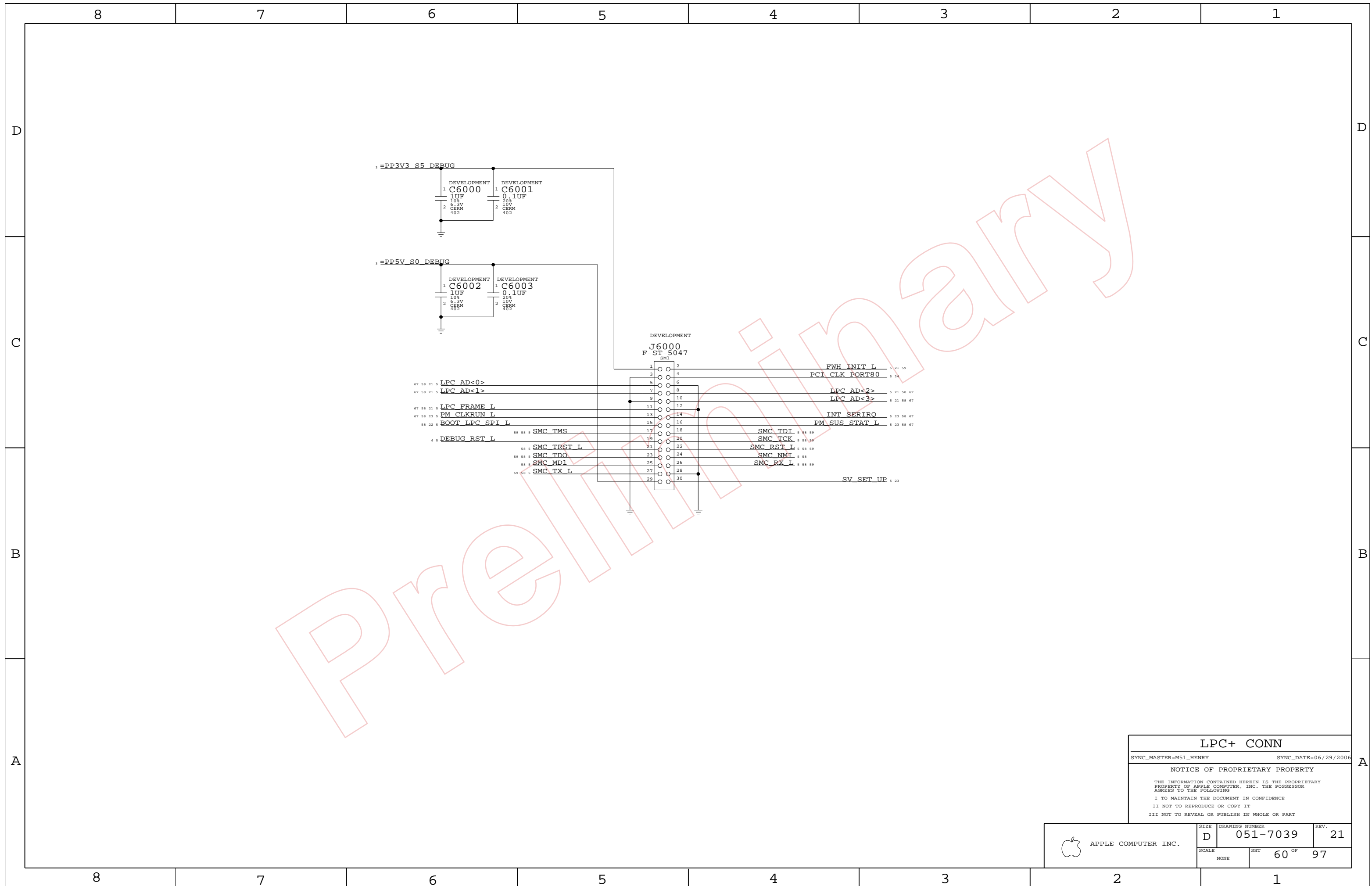
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Pre-release

**LPC+ CONN**

SYNC\_MASTER=M51\_HENRY      SYNC\_DATE=06/29/2006

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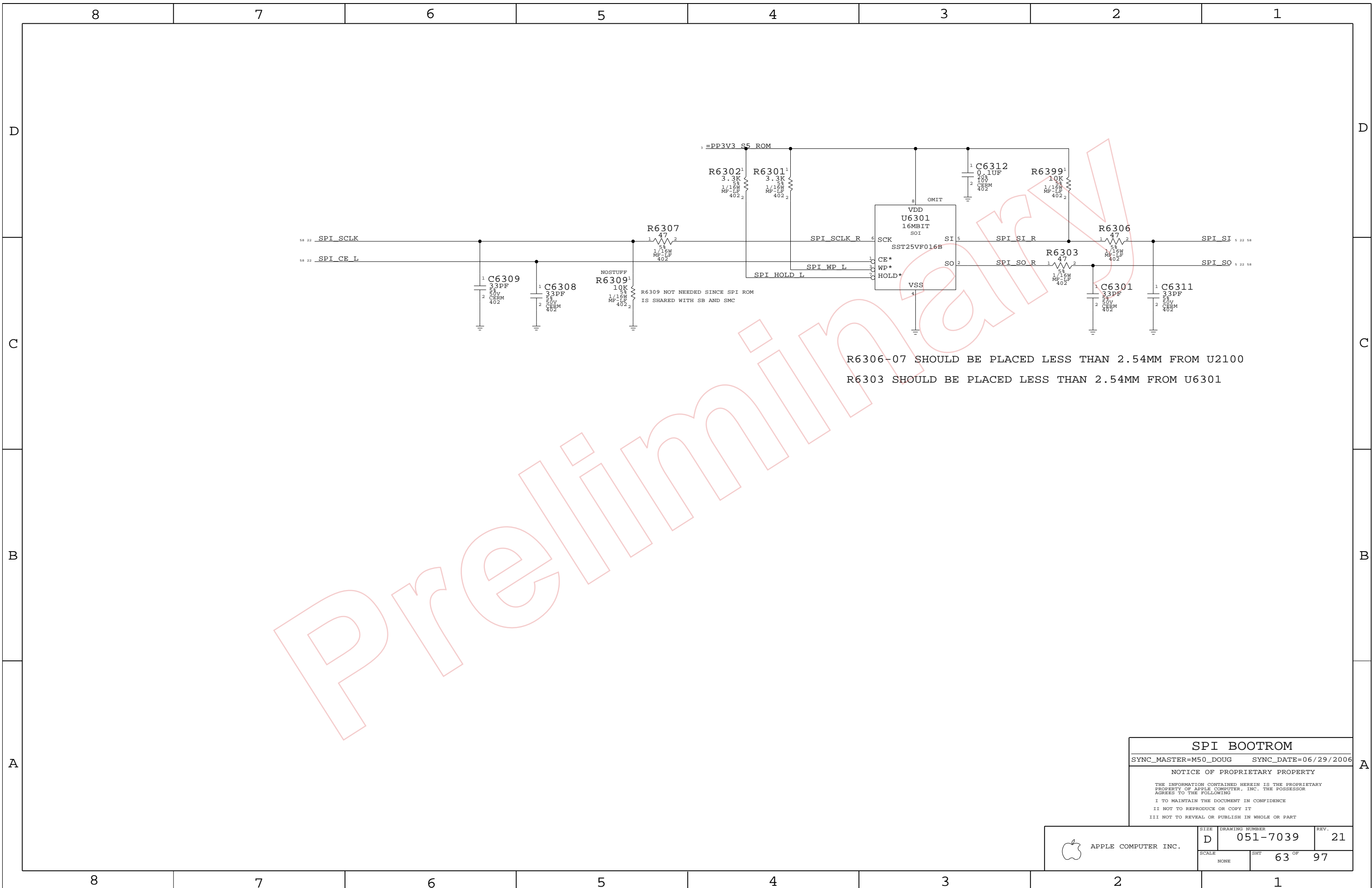
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|                     | SCALE | NONE | SHT            | 60 OF    | 97   |    |



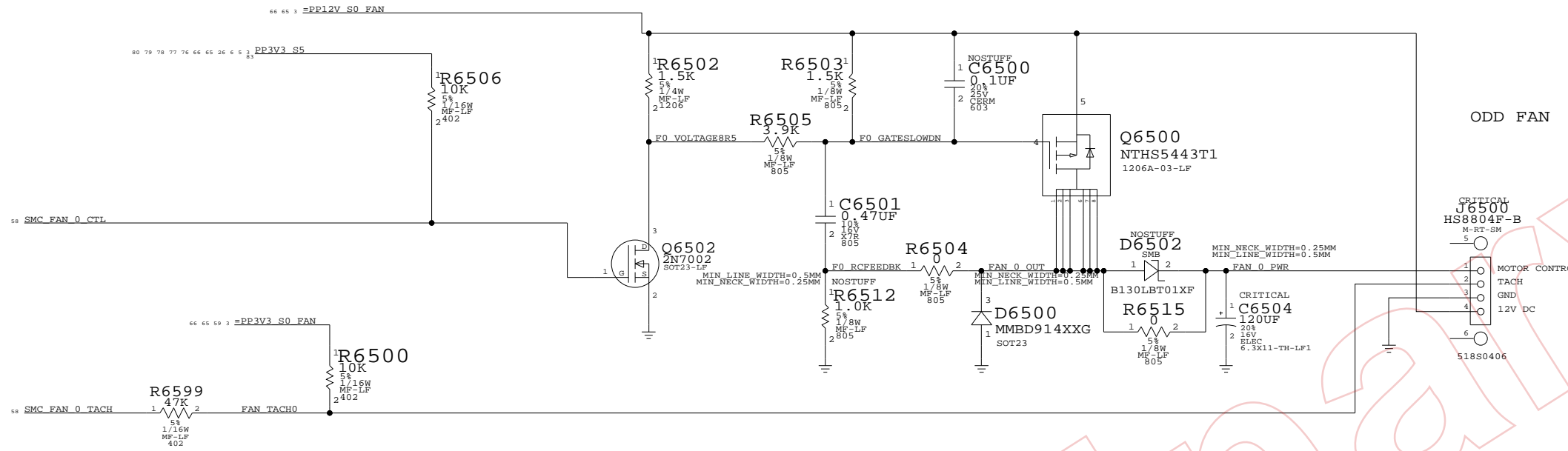
R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100  
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

**SPI BOOTROM**  
 SYNC\_MASTER=M50\_DOUG    SYNC\_DATE=06/29/2006

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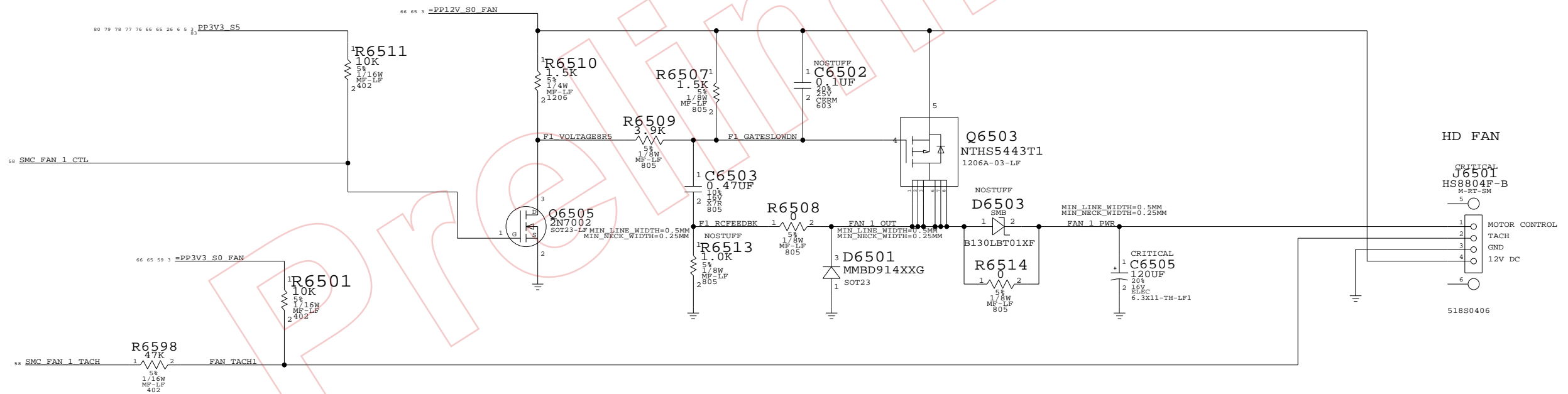
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|                     | D        | 051-7039       | 21   |
| SCALE               | SHT      |                |      |
| NONE                | 63 OF 97 |                |      |

### FAN 0



NOTE: ADDED TO PROTECT SMC

### FAN 1



**HD AND OD FAN**

SYNC\_MASTER=M51\_HENRY      SYNC\_DATE=06/29/2006

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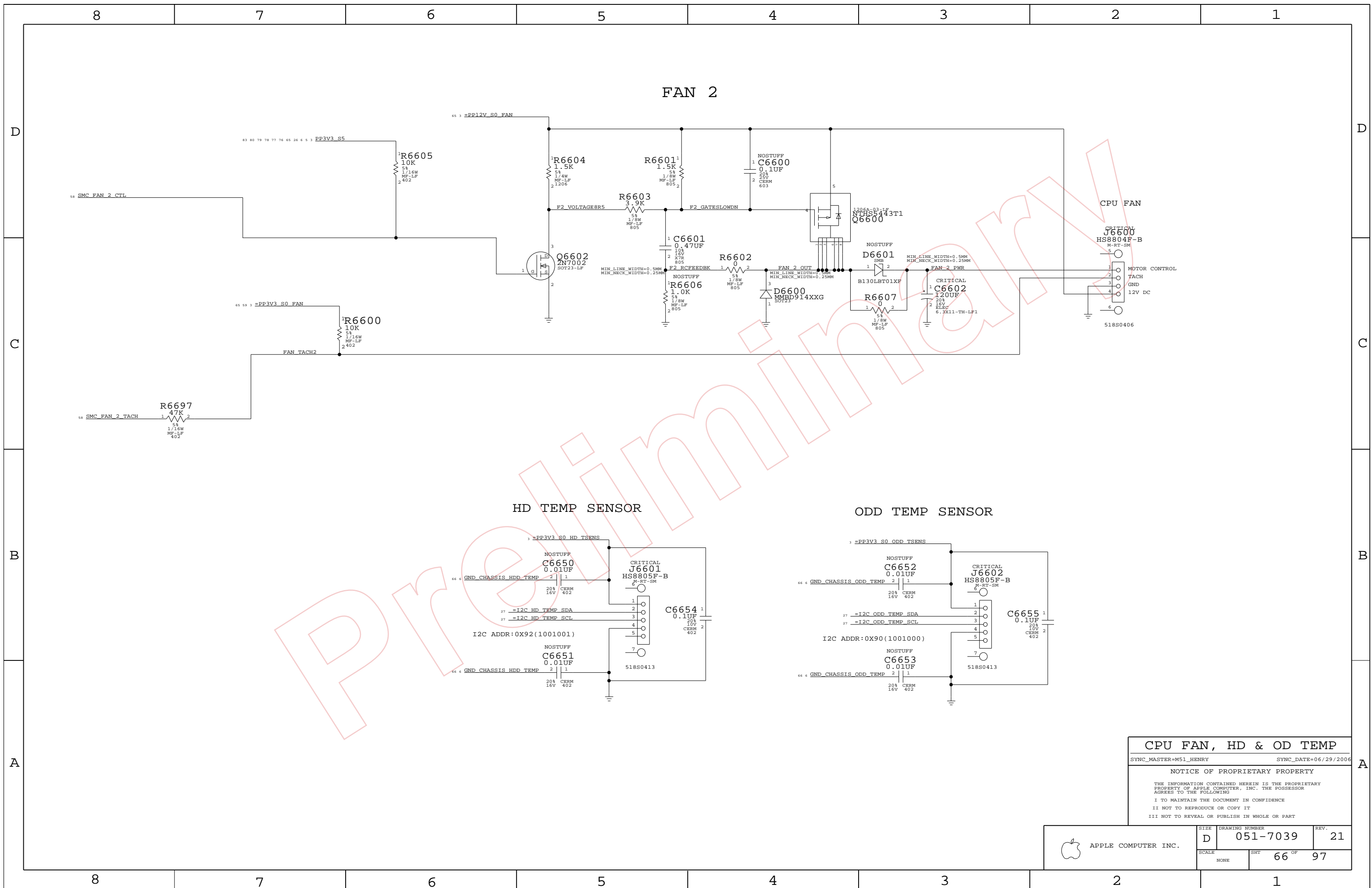
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 65 OF 97       |      |
| NONE                |      |                |      |





**CPU FAN, HD & OD TEMP**

SYNC\_MASTER=M51\_HENRY SYNC\_DATE=06/29/2006

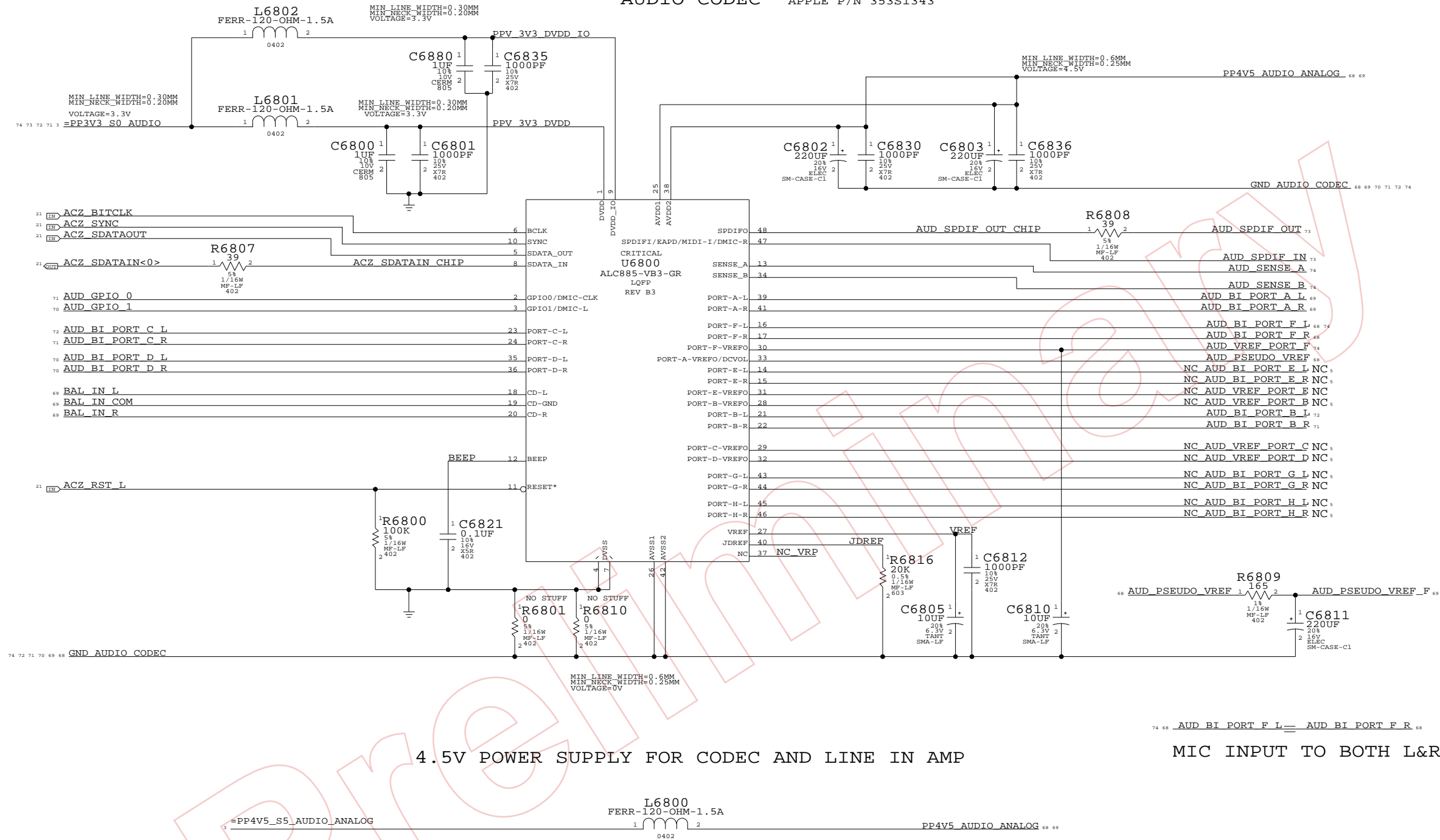
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|                     | D    | 051-7039       | 21   |
| SCALE               |      | SHT            | OF   |
| NONE                |      | 66             | 97   |



AUDIO CODEC APPLE P/N 353S1343



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

MIC INPUT TO BOTH L&R

**AUDIO: CODEC**  
 SYNC\_MASTER=AUDIO SYNC\_DATE=06/29/2006  
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 68 OF 97       |      |
| NONE                |      |                |      |

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5

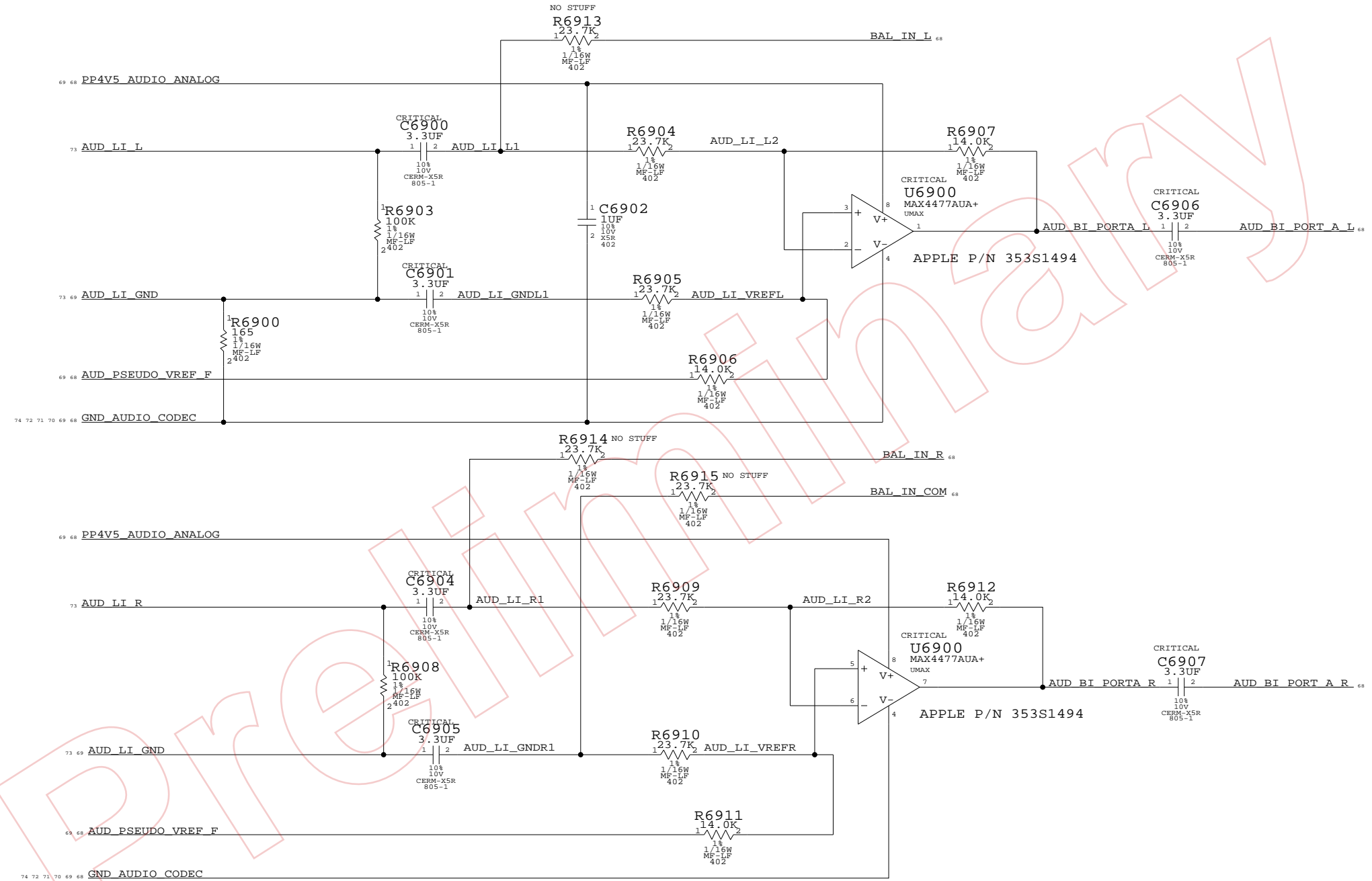
4

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1

LINE IN PSEUDO-DIFFERENTIAL AMP  
AV= 0.59



AUDIO: LINE INPUT AMP

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| SCALE               | SHT  | 69 OF 97       |      |
| NONE                |      |                |      |

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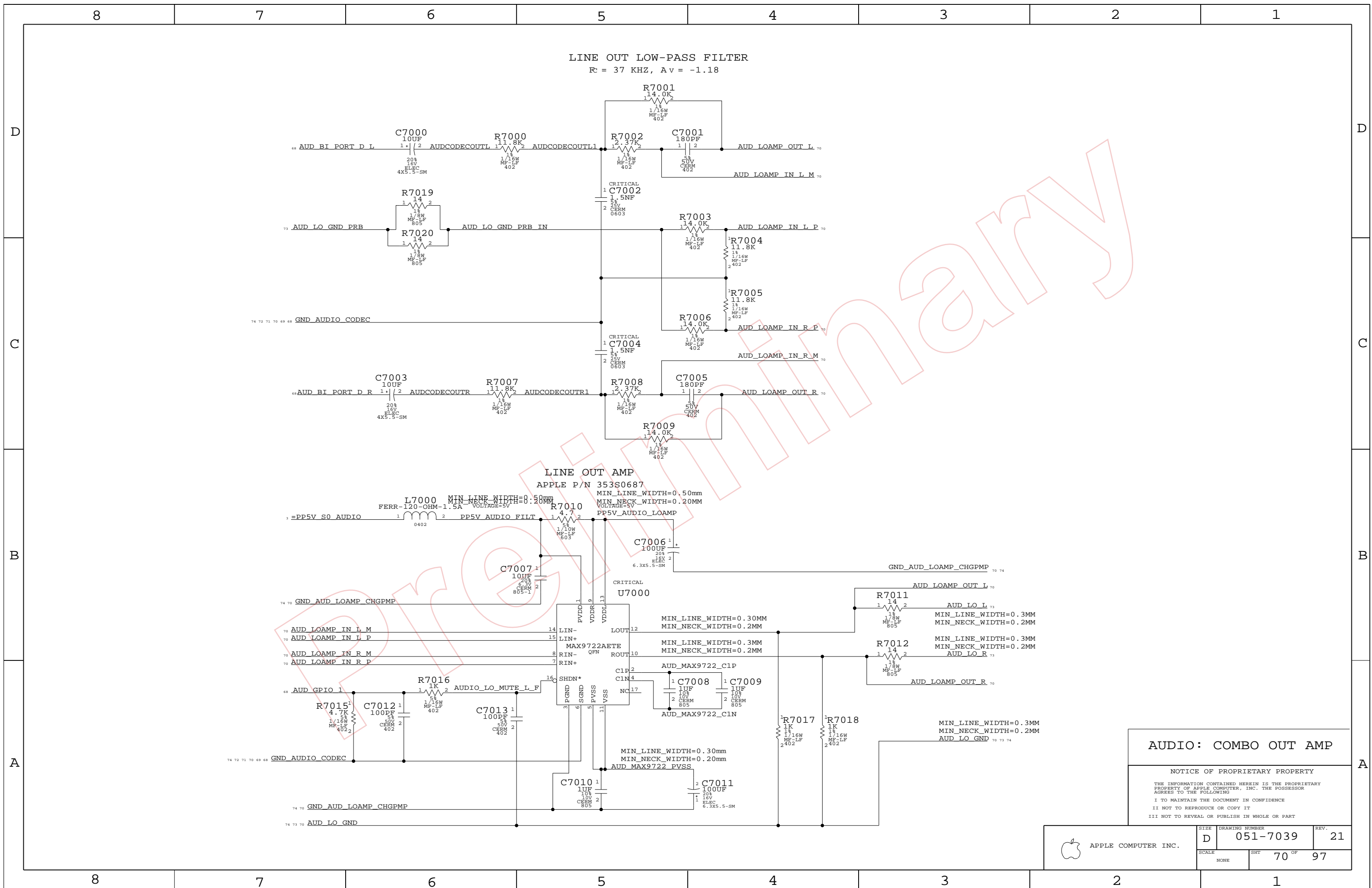
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|                     |      |                |      |
|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 70 OF          | 97   |
| NONE                |      |                |      |

8 7 6 5 4 3 2 1

DRAWS NO POWER DURING S5  
ONLY ON S5 RAIL TO AID ROUTING

NET SPACING TYPE=AUDIO  
MIN LINE WIDTH=0.5MM  
MIN NECK WIDTH=0.2MM  
VOLTAGE=12V  
PP12V\_AUD\_SPKRAMP\_PLANE  
SPEAKER AMP  
APPLE P/N 353S1156

NET SPACING TYPE=AUDIO  
MIN LINE WIDTH=0.5MM  
MIN NECK WIDTH=0.2MM  
VOLTAGE=12V  
=PP12V S5 AUDIO SPKRAMP

R7170  
0.005  
1/4W  
MF-LF  
1206

NET SPACING TYPE=AUDIO  
MIN LINE WIDTH=0.5MM  
MIN NECK WIDTH=0.2MM  
VOLTAGE=12V  
12V S5 SPKRAMP

L7122  
FERR-250-OHM  
SM-1

L7100  
FERR-250-OHM  
SM-1

C7117  
470UF  
20V  
X7R  
10X10-SM

C7100  
470UF  
20V  
X7R  
10X10-SM

C7101  
10UF  
10V  
CERN  
1210

C7118  
0.1UF  
20V  
CERN  
603

71 GND AUDIO SPKRAMP PLANE

L7105  
1000-OHM-200MA  
0603

C7104  
0.47UF  
10V  
X7R  
805

68 AUD BI PORT C R

C7115  
100PF  
50V  
CERN  
402

L7106  
1000-OHM-200MA  
0603

C7105  
0.47UF  
10V  
X7R  
805

74 72 71 70 69 68 GND AUDIO CODEC

L7107  
1000-OHM-200MA  
0603

C7106  
0.47UF  
10V  
X7R  
805

AUD SAMP INL N

AUD SAMP INL P

AUD SAMP INR P

AUD SAMP INR N

AUD SAMP G1

AUD SAMP G2

AUD SAMP FS1

AUD SAMP FS2

AUD SAMP SHDN L

AUD MAX9714 VREG

SPKRAMP SS

AGND PAD

PGND

SS

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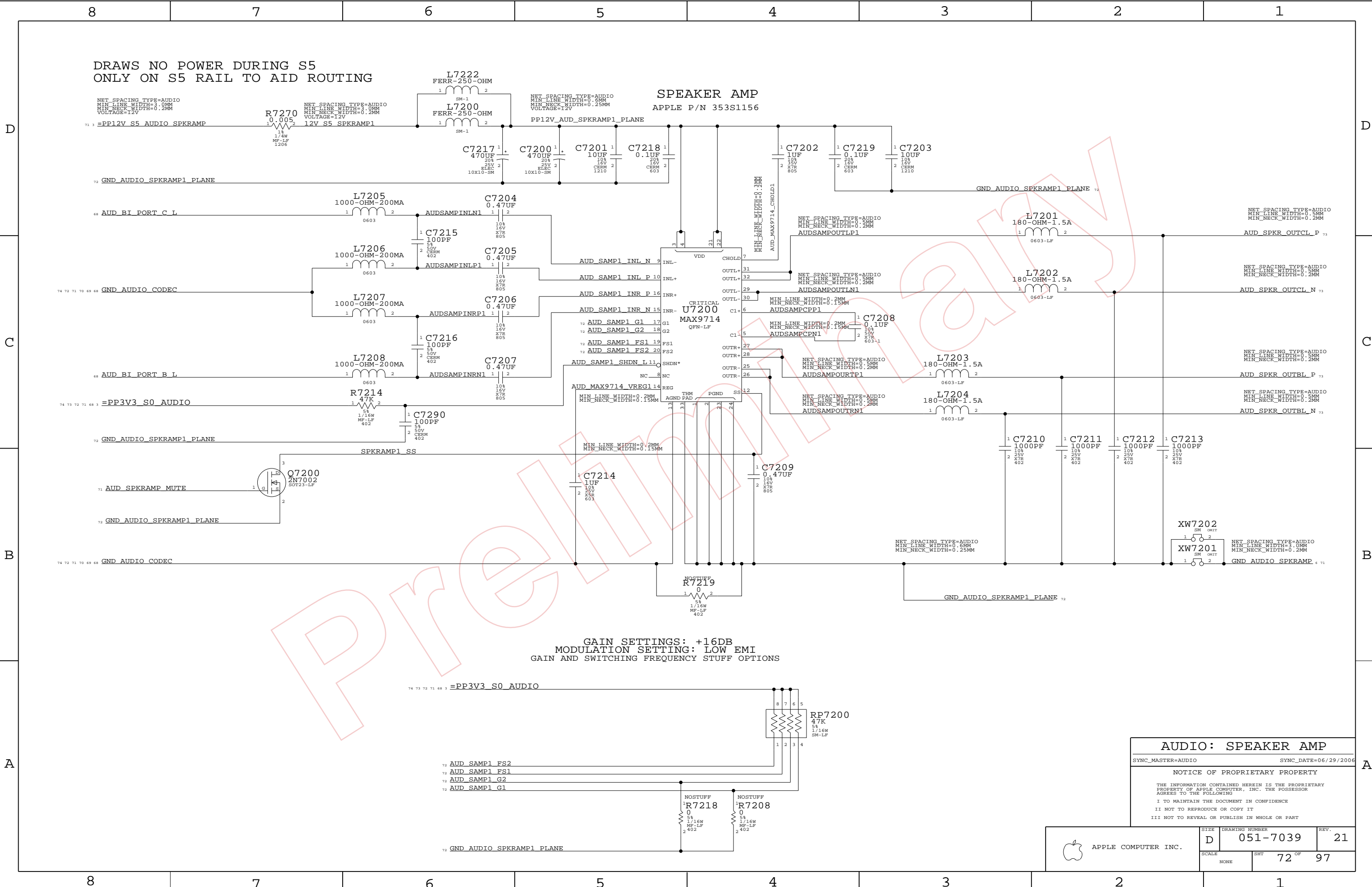
OUTL+

OUTL-

OUTL+

DRWS NO POWER DURING S5  
ONLY ON S5 RAIL TO AID ROUTING

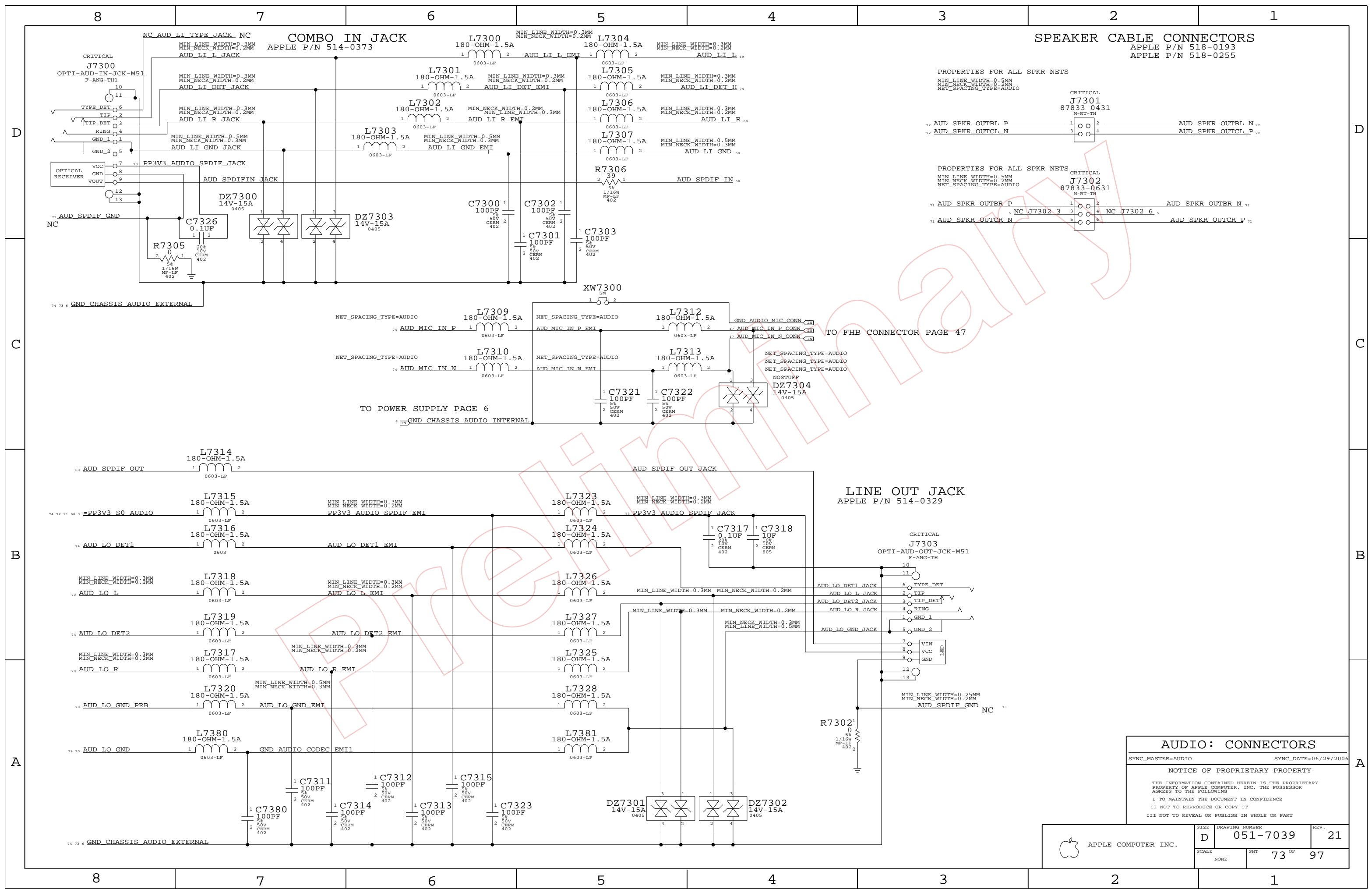
**SPEAKER AMP**  
APPLE P/N 353S1156



GAIN SETTINGS: +16DB  
MODULATION SETTING: LOW EMI  
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

**AUDIO: SPEAKER AMP**  
SYNC\_MASTER=AUDIO SYNC\_DATE=06/29/2006  
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 72 OF 97       |      |
| NONE                |      |                |      |



**AUDIO: CONNECTORS**  
 SYNC\_MASTER=AUDIO SYNC\_DATE=06/29/2006  
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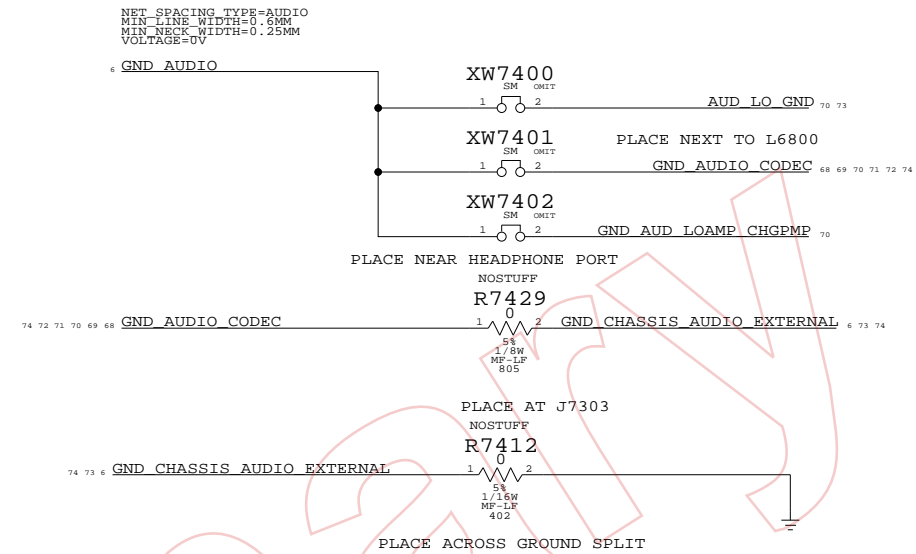
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
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| SCALE               | SHT  | 73 OF 97       |      |
| NONE                |      |                |      |



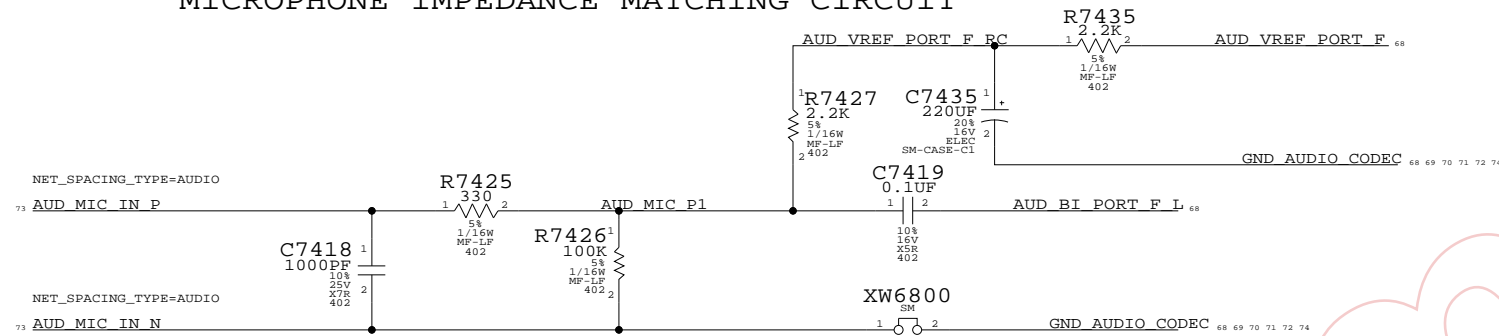
| CODEC OUTPUT SIGNAL PATHS |        |                 |             |              |
|---------------------------|--------|-----------------|-------------|--------------|
| FUNCTION                  | VOLUME | DAC             | PIN COMPLEX | MUTE CONTROL |
| LINE OUT                  | 0X0C   | 0X02            | 0X14 (D)    | GPIO 1       |
| SPKR AMP                  | 0X0D   | 0X03            | 0X18 (B)    | GPIO 0       |
| SPKR AMP1                 | 0X0F   | 0X05            | 0X1A (C)    | GPIO 0       |
| SPDIFOUT                  |        | CONVERTER=0X06  | PIN=0X1E    |              |
|                           |        | DETECT DELEGATE | PIN 0X16H   |              |

| CODEC INPUT SIGNAL PATHS |                |       |          |      |
|--------------------------|----------------|-------|----------|------|
| FUNCTION                 | ADC            | MIXER | PORT     | VREF |
| MIC INPUT                | 0X07           | 0X24  | 0X19 (F) | 80%  |
| LINE INPUT               | 0X08           | 0X23  | 0X15 (A) | 50%  |
| SPDIFIN                  | CONVERTER=0X0A |       | PIN=0X1F |      |

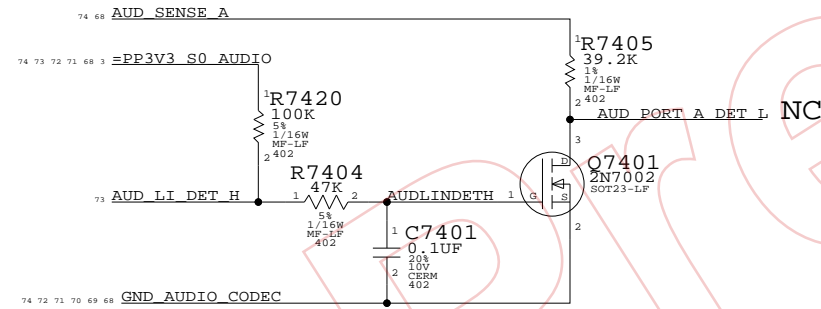
### AUDIO GROUND RETURNS



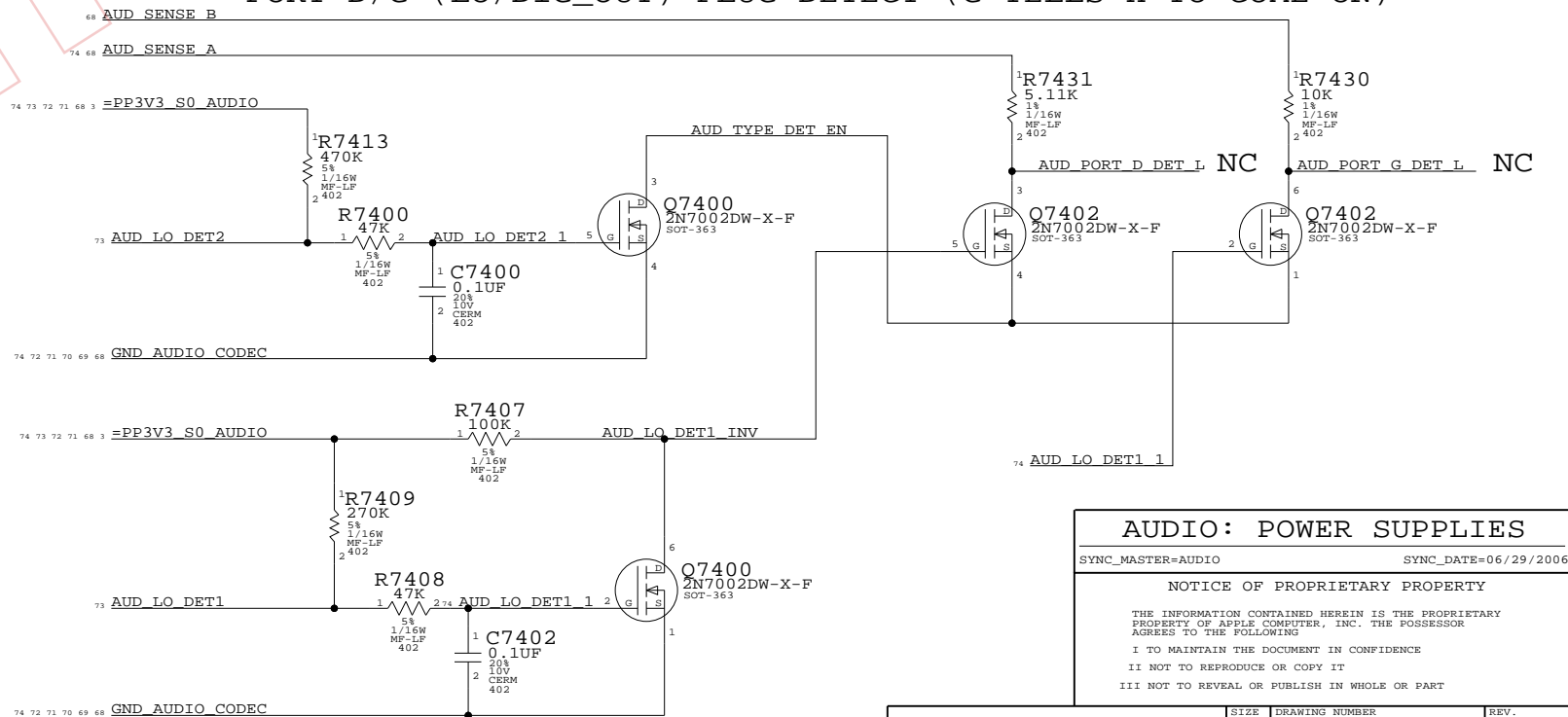
### MICROPHONE IMPEDANCE MATCHING CIRCUIT



### PORT A (LI) PLUG DETECT



### PORT D/G (LO/DIG\_OUT) PLUG DETECT (G TELLS H TO COME ON)



### AUDIO: POWER SUPPLIES

SYNC\_MASTER=AUDIO SYNC\_DATE=06/29/2006

#### NOTICE OF PROPRIETARY PROPERTY

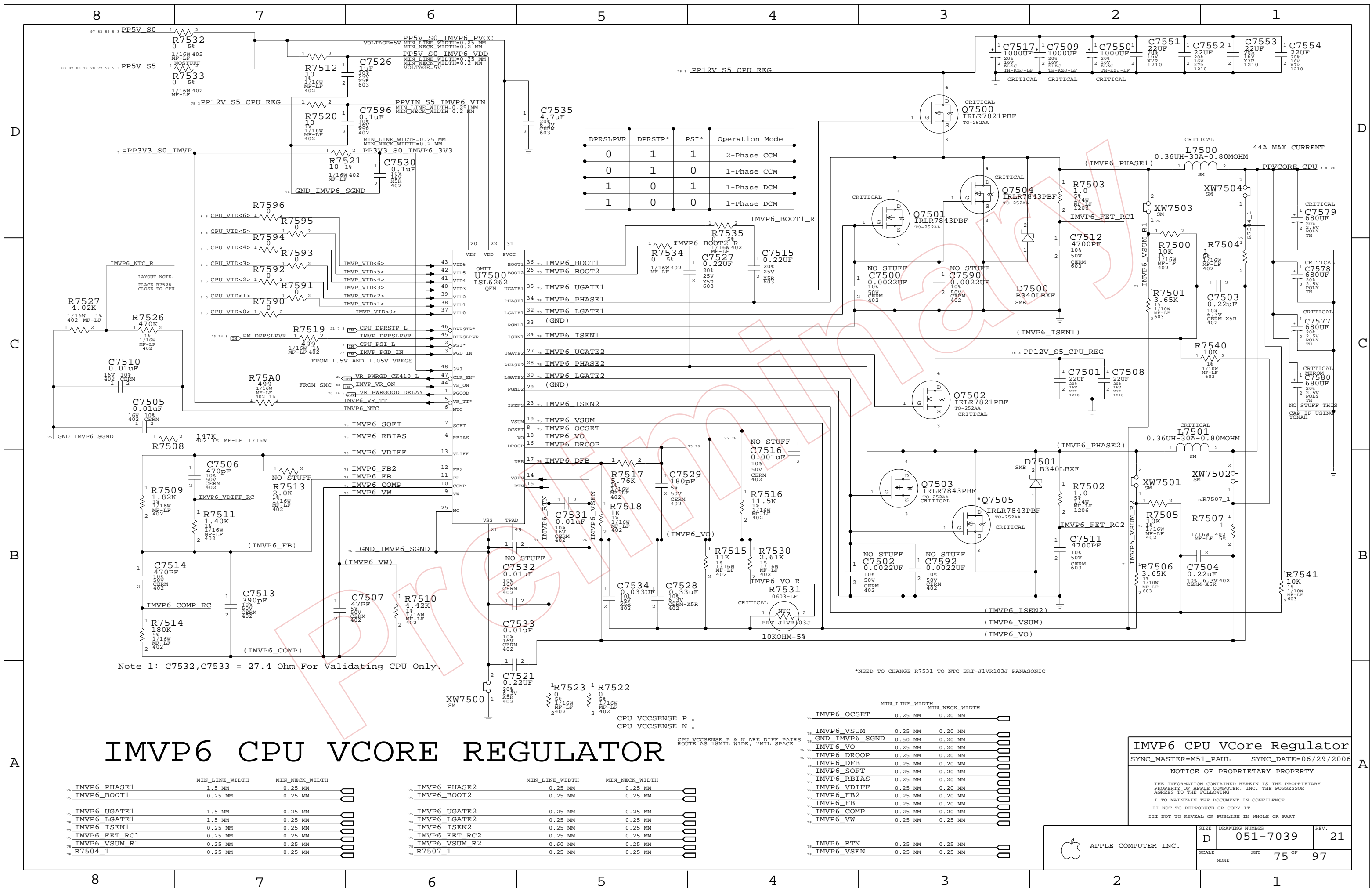
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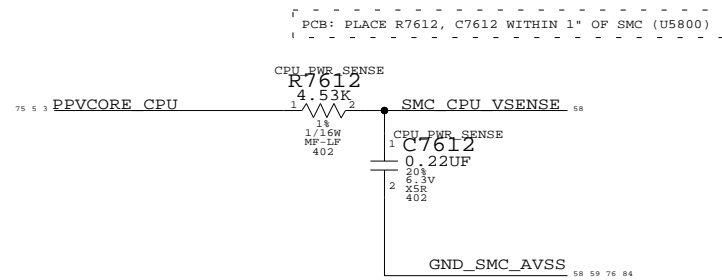
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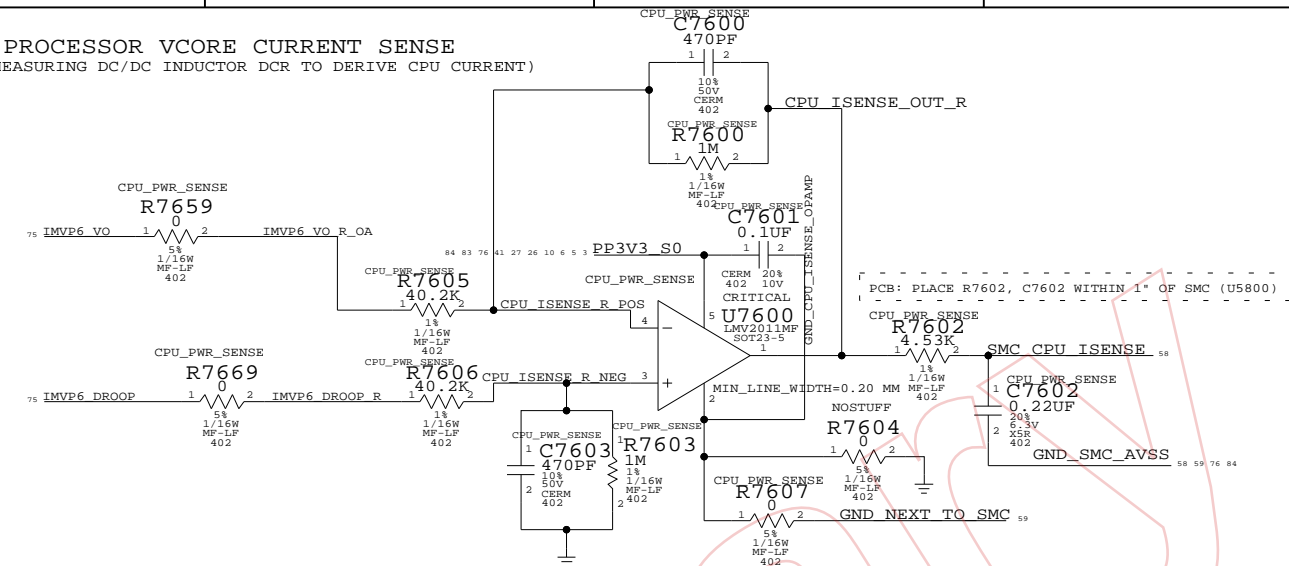
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|---------------------|------|----------------|------|
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 74 OF 97       |      |
| NONE                |      |                |      |



PROCESSOR VCORE SENSE

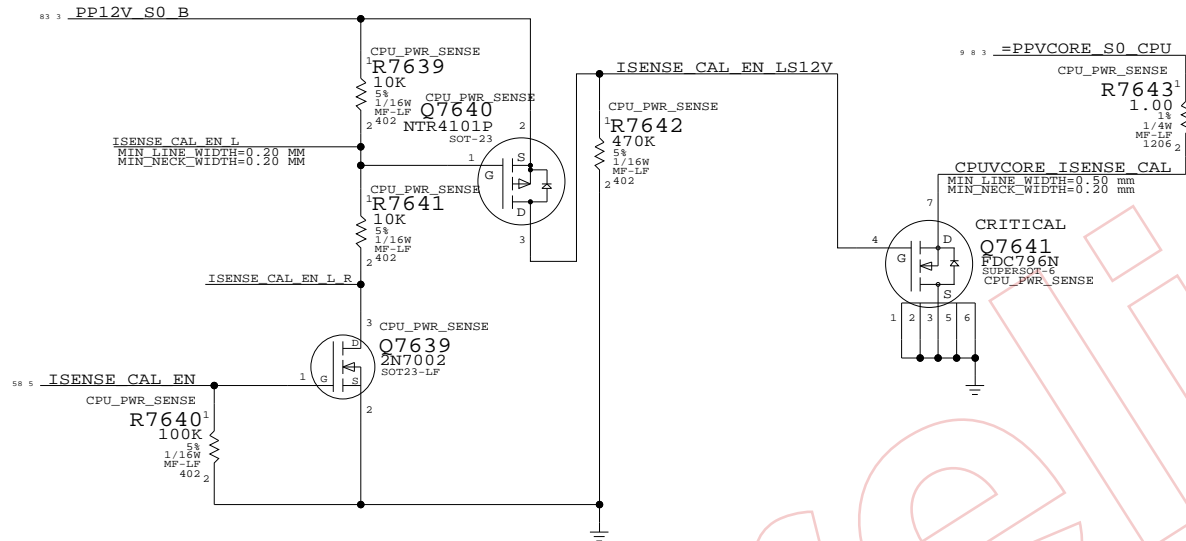


PROCESSOR VCORE CURRENT SENSE  
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

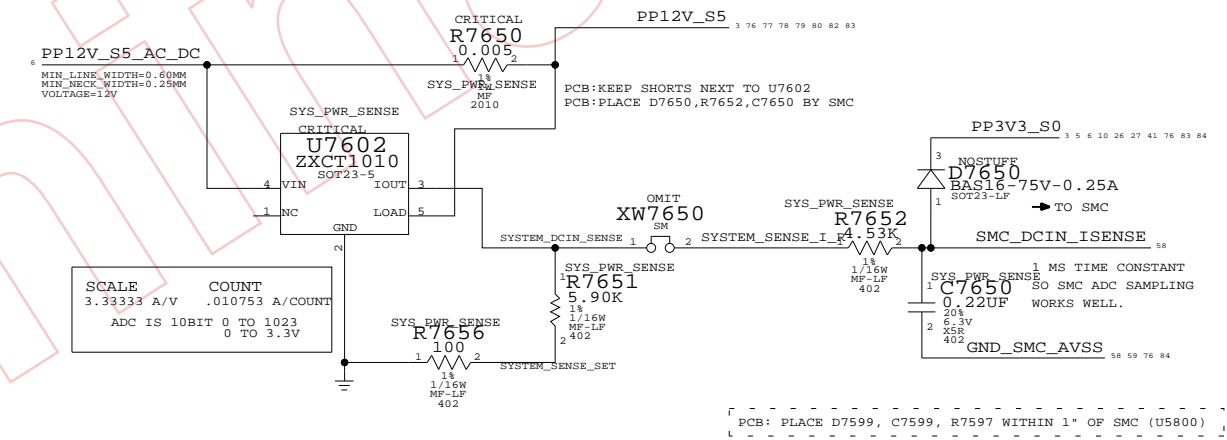


CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

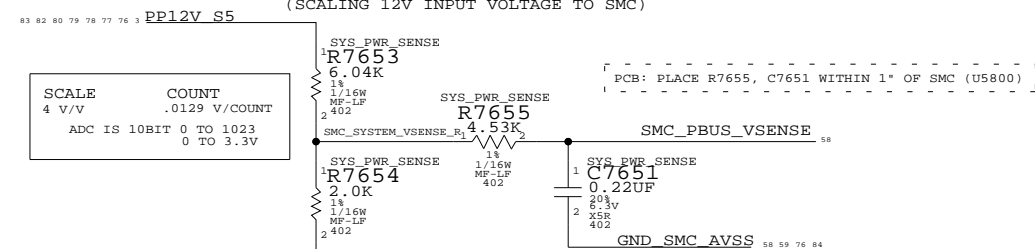


SYSTEM CURRENT SENSE



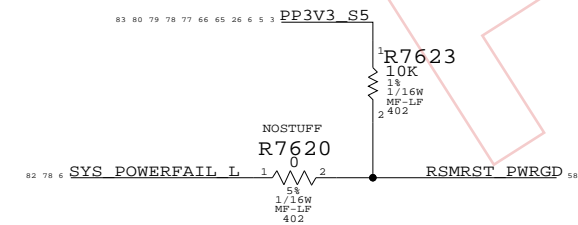
| SCALE                  | COUNT            |
|------------------------|------------------|
| 3.33333 A/V            | 0.010753 A/COUNT |
| ADC IS 10BIT 0 TO 1023 | 0 TO 3.3V        |

SYSTEM VOLTAGE SENSE  
(SCALING 12V INPUT VOLTAGE TO SMC)



| SCALE                  | COUNT         |
|------------------------|---------------|
| 4 V/V                  | 0.129 V/COUNT |
| ADC IS 10BIT 0 TO 1023 | 0 TO 3.3V     |

SMC PWRGD PULLUP



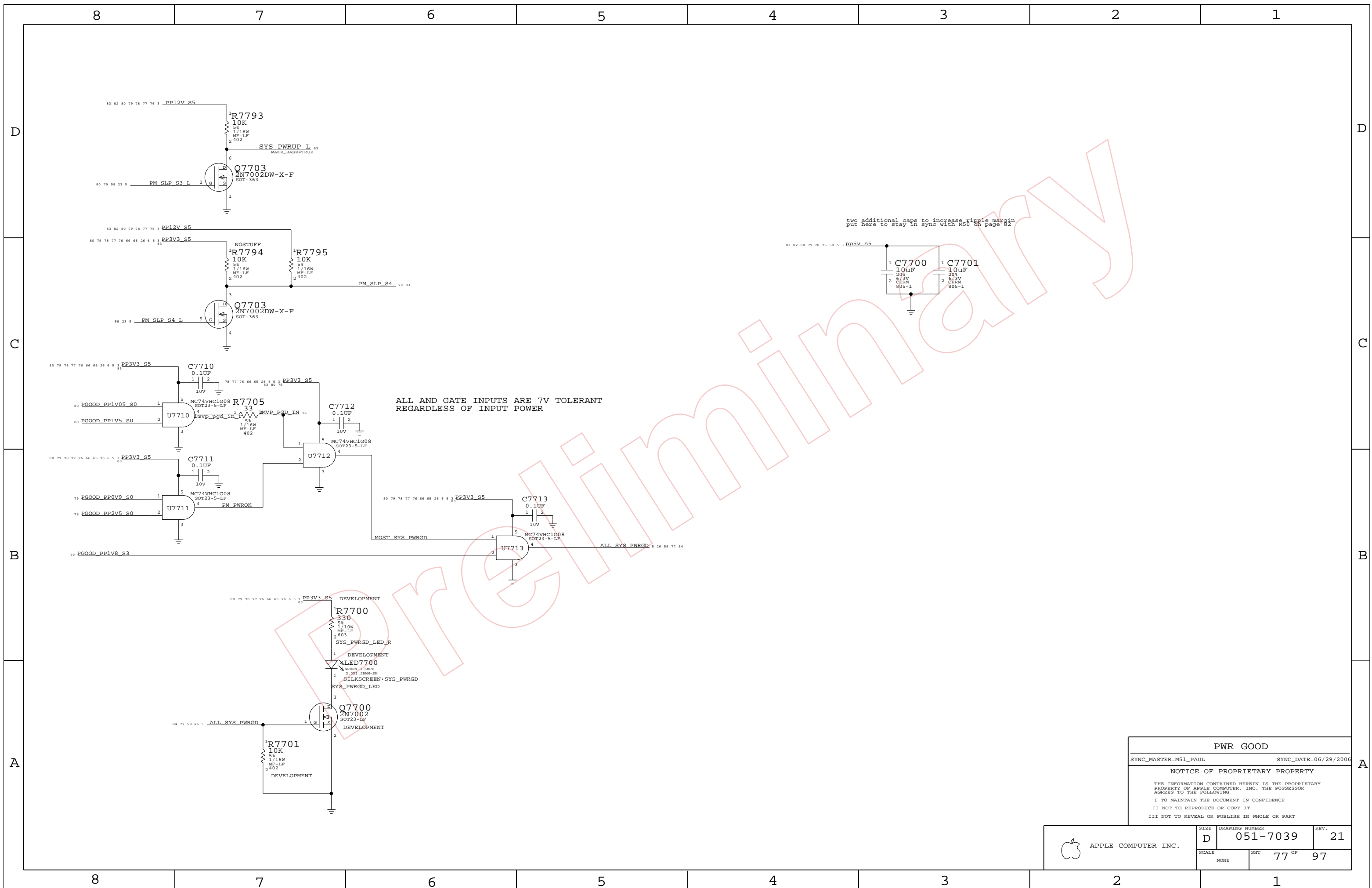
CPU & SYSTEM SENSE

SYNC\_MASTER=M51\_DAVE SYNC\_DATE=(MASTER)

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| SCALE               | SHT  | 76 OF          | 97   |
| NONE                |      |                |      |



ALL AND GATE INPUTS ARE 7V TOLERANT  
REGARDLESS OF INPUT POWER

two additional caps to increase ripple margin  
put here to stay in sync with M50 on page 82

|  |                      |
|--|----------------------|
| PWR GOOD   |                      |
| SYNC_MASTER=M51_PAUL   | SYNC_DATE=06/29/2006 |
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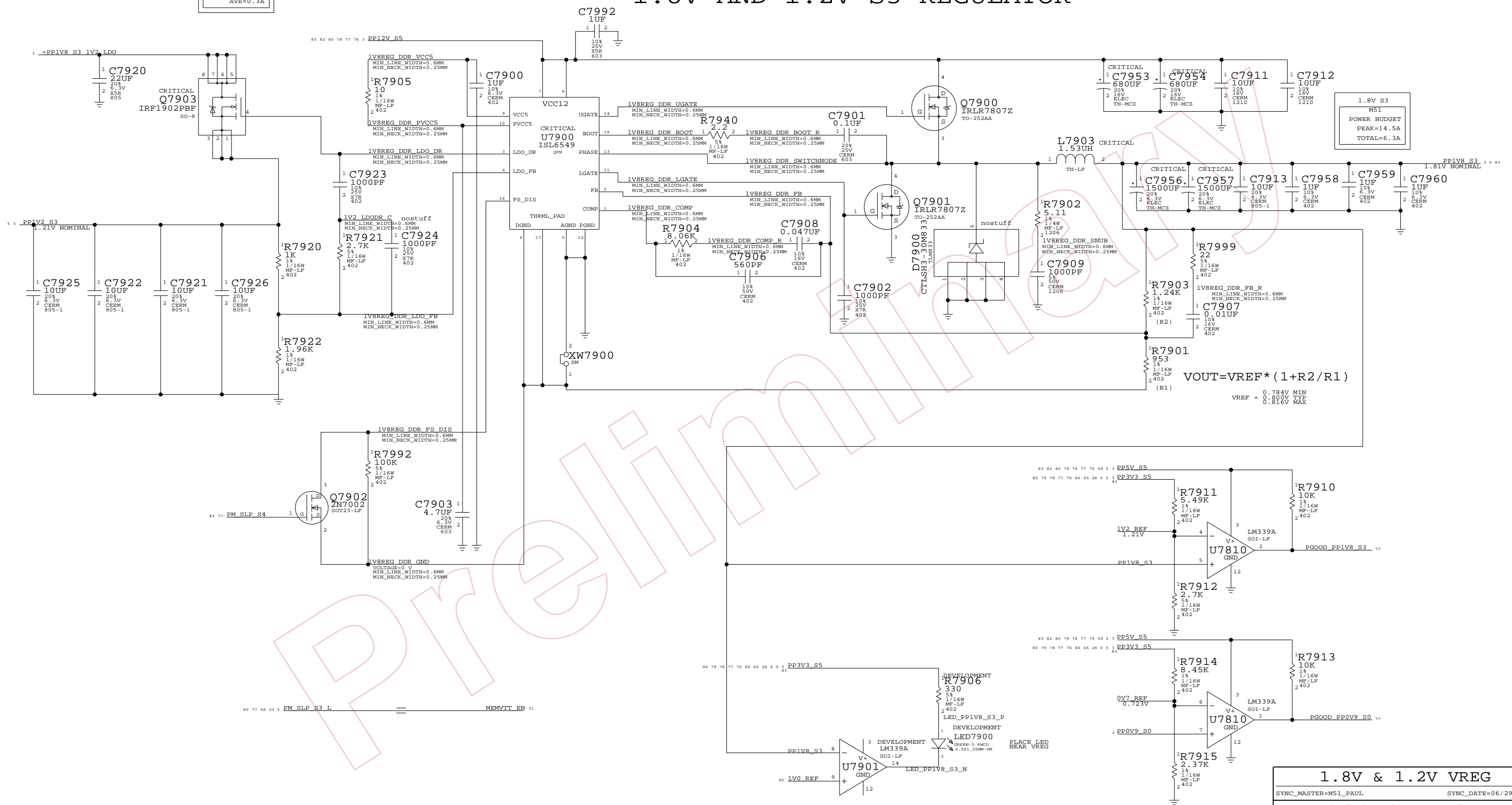
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|---------------------|------|----------------|------|
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 77 OF          | 97   |
| NONE                |      |                |      |



# 1.8V AND 1.2V S3 REGULATOR

1.2V S3  
POWER BUDGET  
PEAK=0.4A  
AVE=0.3A

1.8V S3  
M51  
POWER BUDGET  
PEAK=14.5A  
TOTAL=6.3A

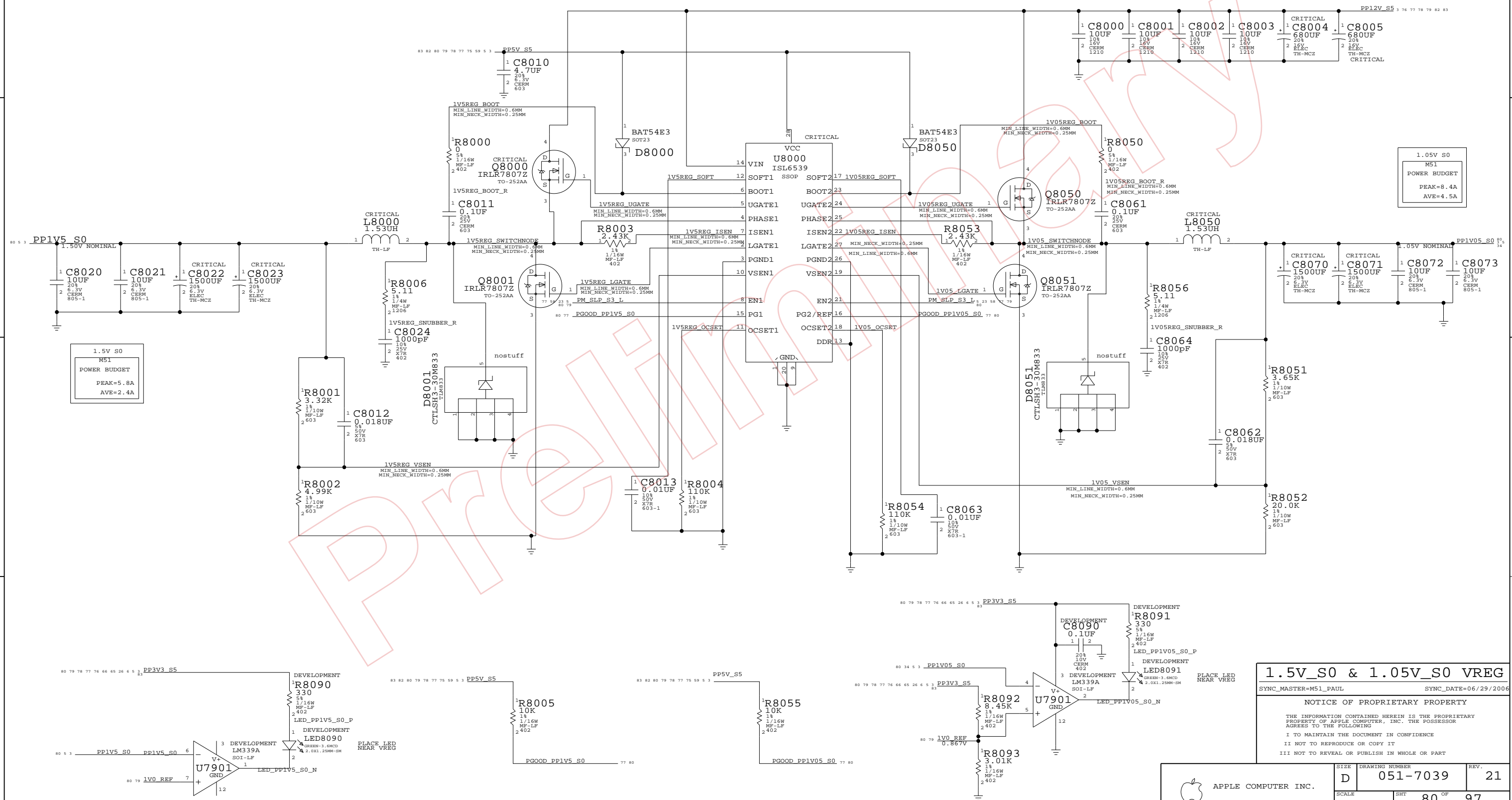


1.8V & 1.2V VREG  
SYNC\_MASTER=M51\_PAUL  
SYNC\_DATE=06/29/2006

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| SCALE               | SHT  | 79 OF          | 97   |
| NONE                |      |                |      |

# 1.5V S0 AND 1.05V S0 RAILS



## 1.5V\_S0 & 1.05V\_S0 VREG

SYNC\_MASTER=M51\_PAUL SYNC\_DATE=06/29/2006

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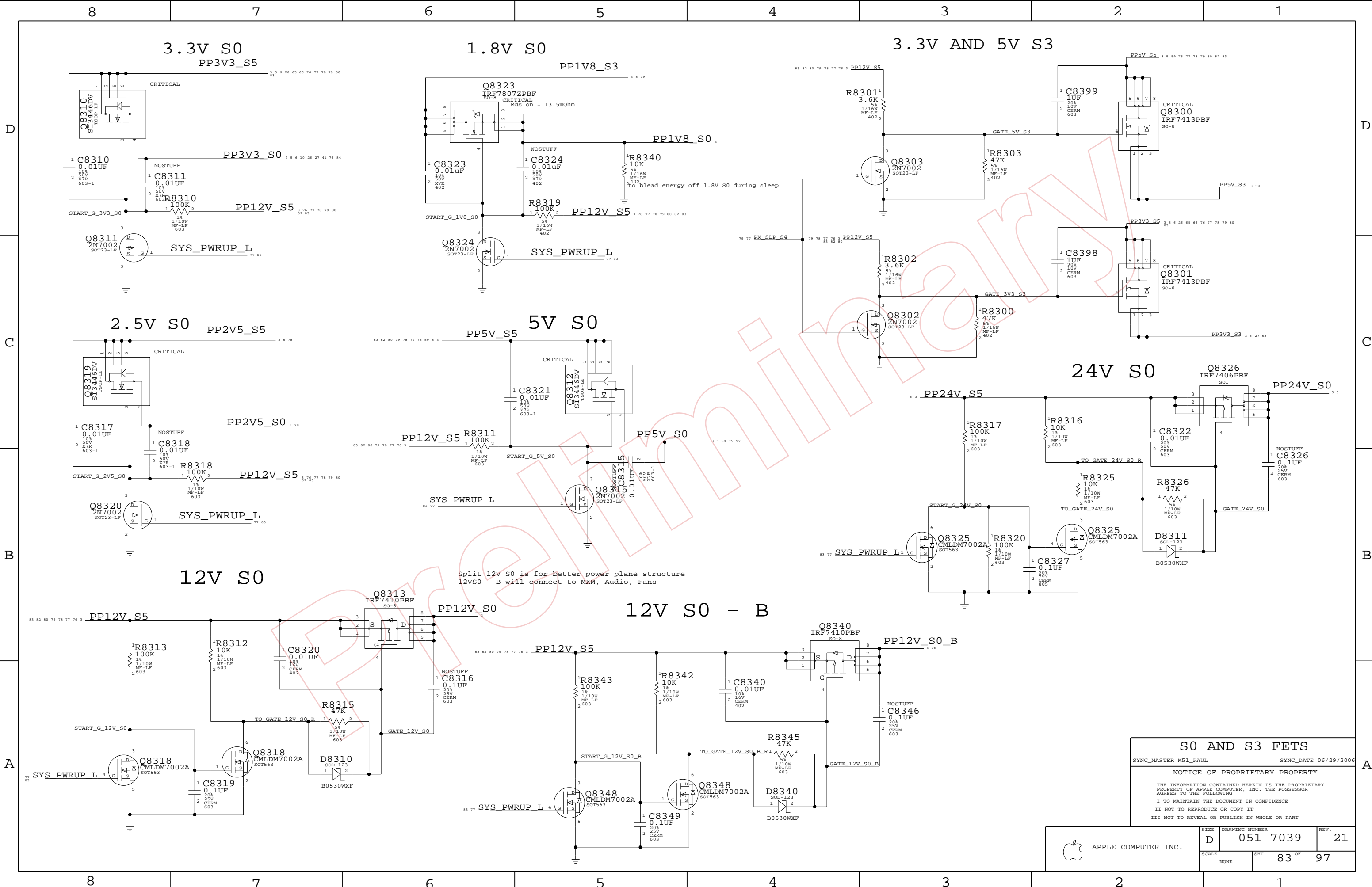
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| SCALE               | SHT  | 80 OF          | 97   |
| NONE                |      |                |      |







Split 12V S0 is for better power plane structure  
 12VS0 - B will connect to MXM, Audio, Fans

**S0 AND S3 FETS**  
 SYNC\_MASTER=M51\_PAUL SYNC\_DATE=06/29/2006  
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|                     | D    | 051-7039       | 21   |
| SCALE               | SHT  | 83 OF          | 97   |
| NONE                |      |                |      |



# Page Notes

Power aliases required by this page:  
 - =PP3V3\_S0\_MXM  
 - =PP2V5\_S0\_MXM

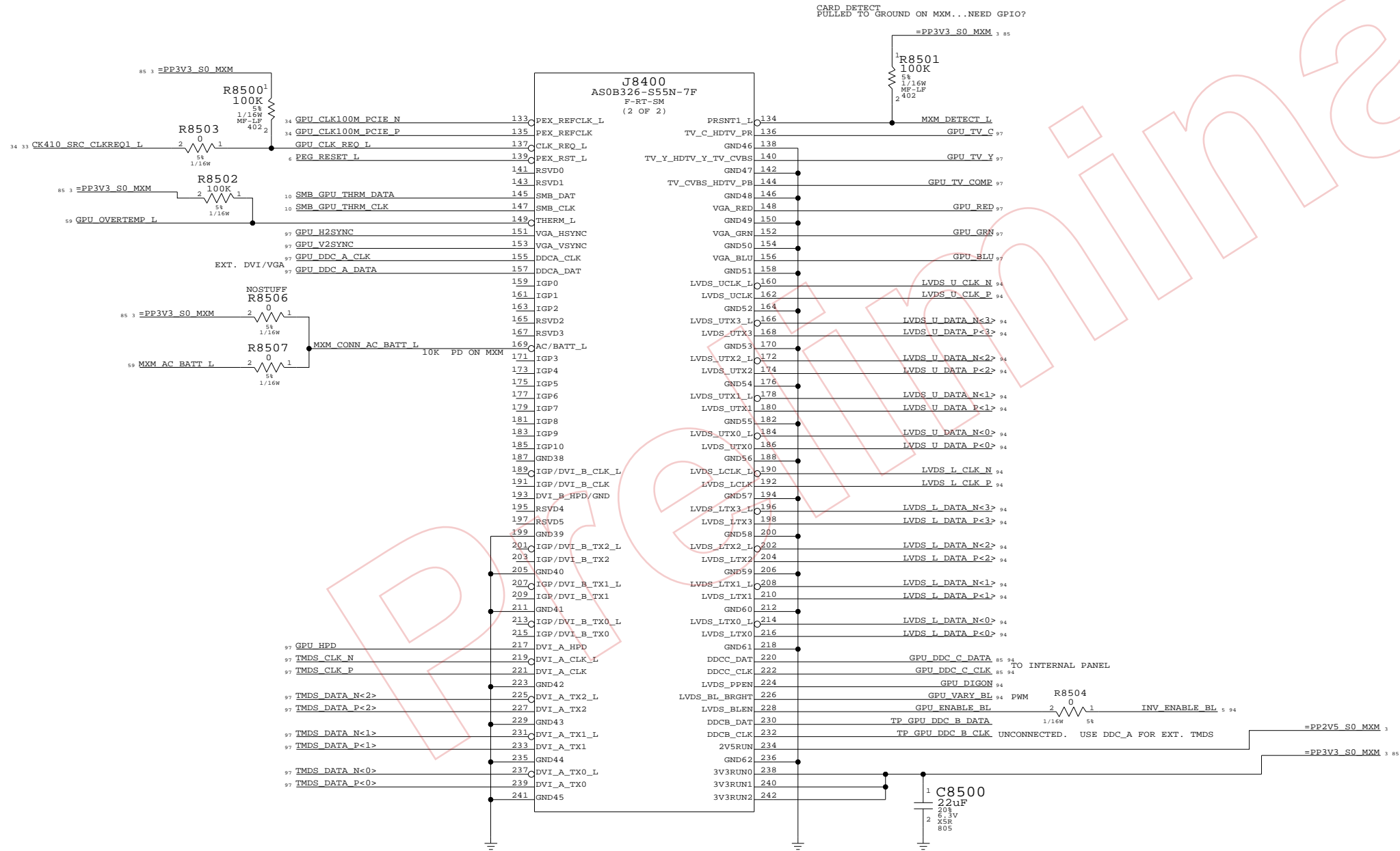
Signal aliases required by this page:  
 - =SMB\_GPU\_THRM\_DATA  
 - =SMB\_GPU\_THRM\_CLK

BOM options provided by this page:  
 (NONE)

## MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

| VOLTAGE   | CURRENT   | POWER              |
|-----------|-----------|--------------------|
| 3V3       | 1.5 A     | 4.95 W             |
| 5V        | 0.5 A     | 2.5 W              |
| 2V5       | 0.5 A     | 1.25 W             |
| 1V8       | 3.5 A     | 6.3 W              |
| PWR (12V) | UP TO 4 A | PLATFORM DEPENDENT |



**MXM I/O**  
 SYNC\_MASTER=M51\_DAVE SYNC\_DATE=(MASTER)

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| SCALE               | SHT  | 85 OF          | 97   |
| NONE                |      |                |      |

# Page Notes

Power aliases required by this page:  
 - =PP12V\_LCD  
 - =PP24V\_INVERTER  
 - =PP3V3\_S0\_VIDEO

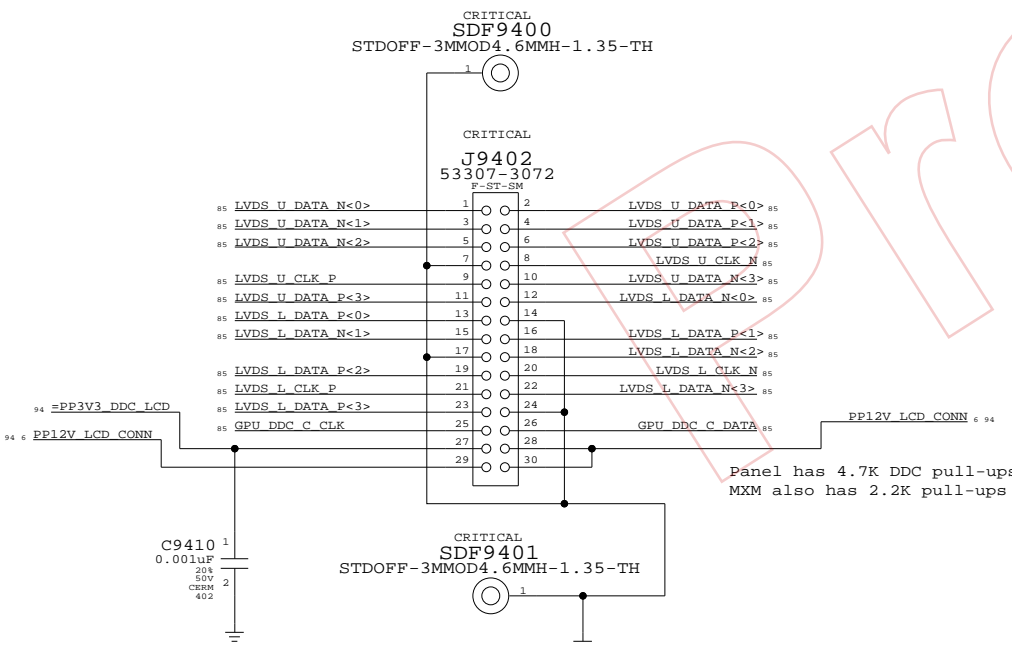
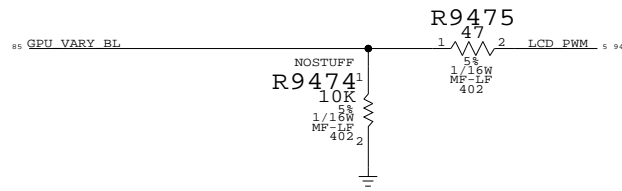
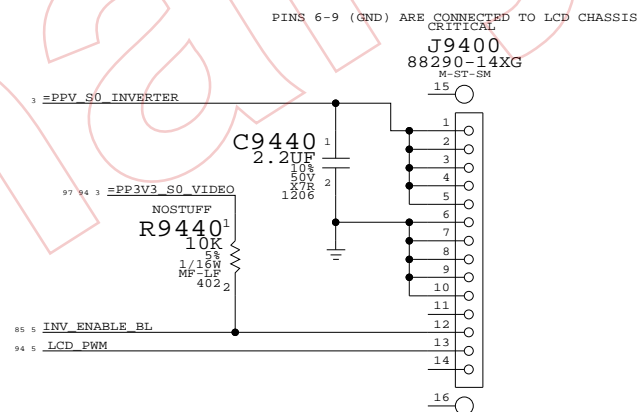
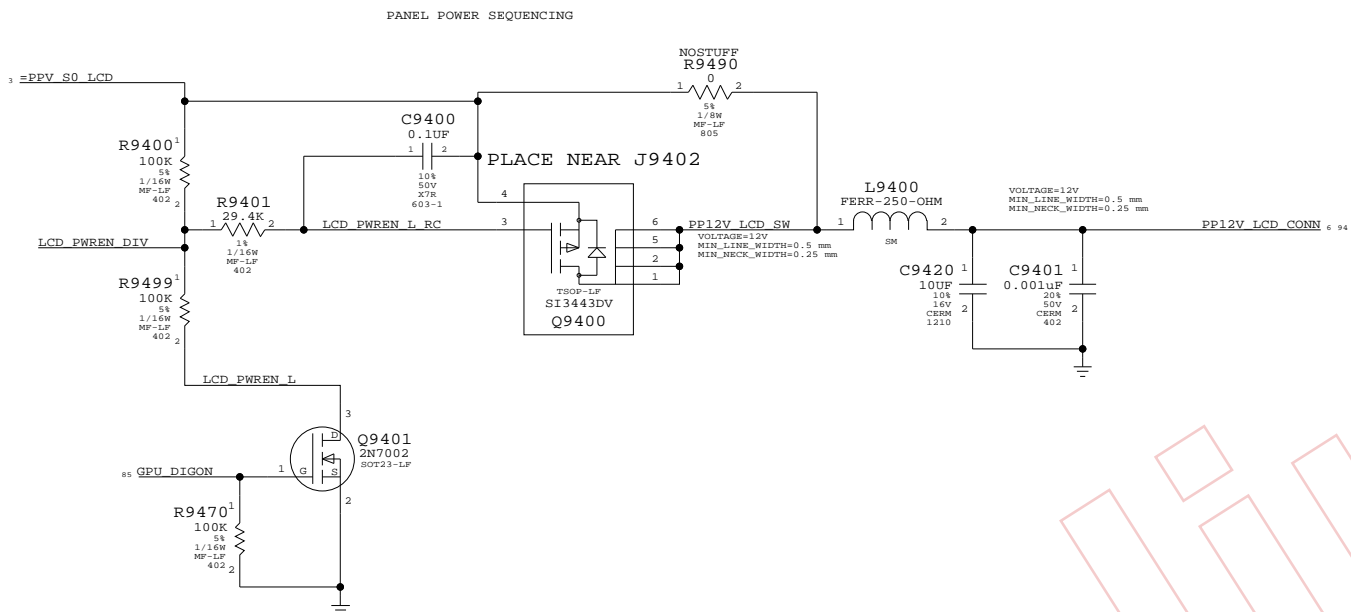
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

97 94 3 =PP3V3\_S0\_VIDEO =PP3V3\_DDC\_LCD 94

## LCD (LVDS) INTERFACE

## INVERTER INTERFACE



**Internal Display Conns**

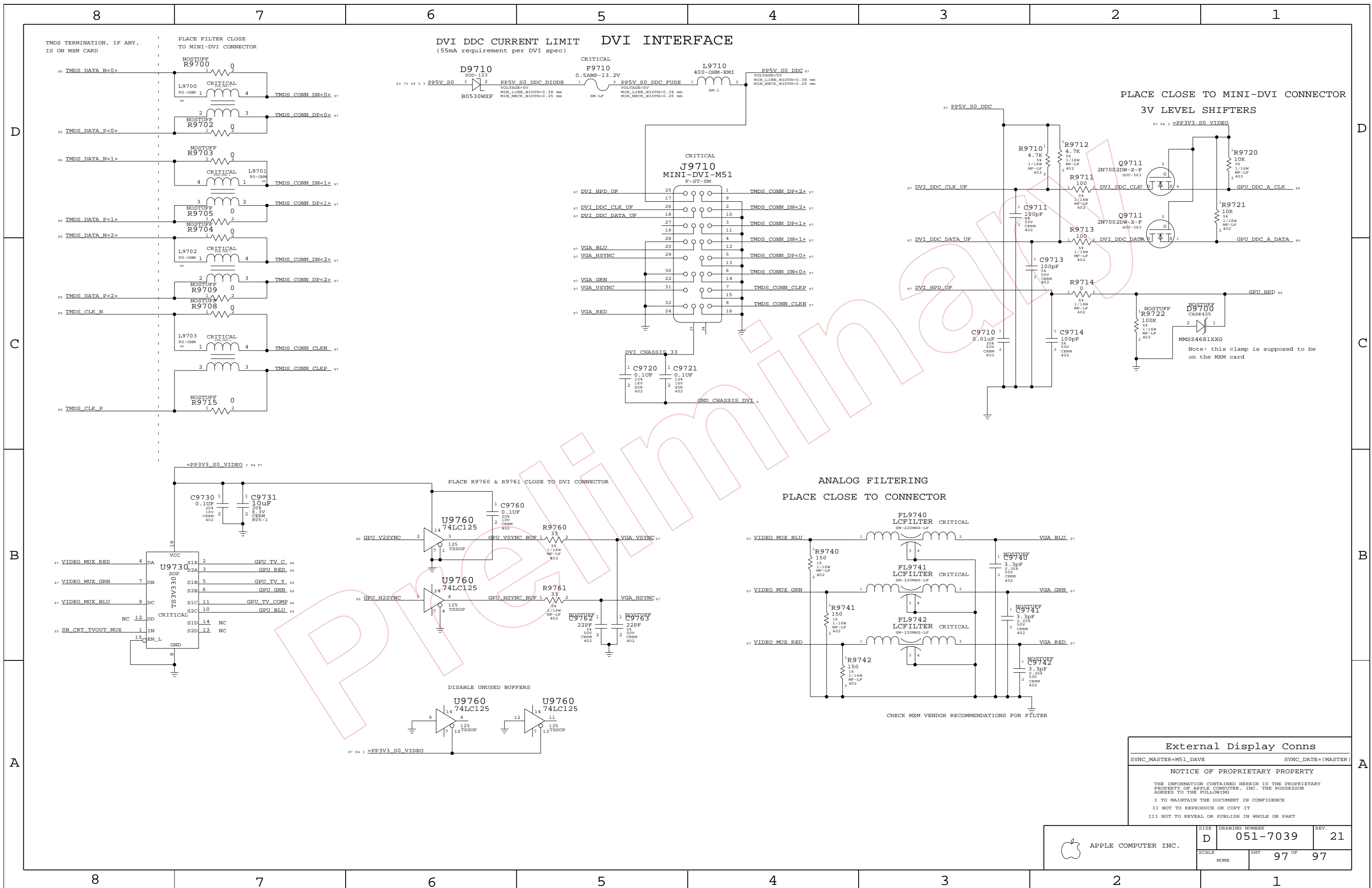
SYNC\_MASTER=M51\_DAVE SYNC\_DATE=(MASTER)

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TMDS TERMINATION, IF ANY, IS ON MXM CARD

PLACE FILTER CLOSE TO MINI-DVI CONNECTOR

**DVI DDC CURRENT LIMIT DVI INTERFACE**  
(55mA requirement per DVI spec)

**PLACE CLOSE TO MINI-DVI CONNECTOR**  
**3V LEVEL SHIFTERS**

**ANALOG FILTERING**  
**PLACE CLOSE TO CONNECTOR**

**External Display Conns**

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