

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
01		279015	ENGINEERING RELEASED		
				DATE	DATE
				06/06/03	?

Q59 MLB CONFIG A,B,C

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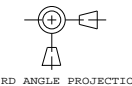

POWER RAIL DEFINITIONS

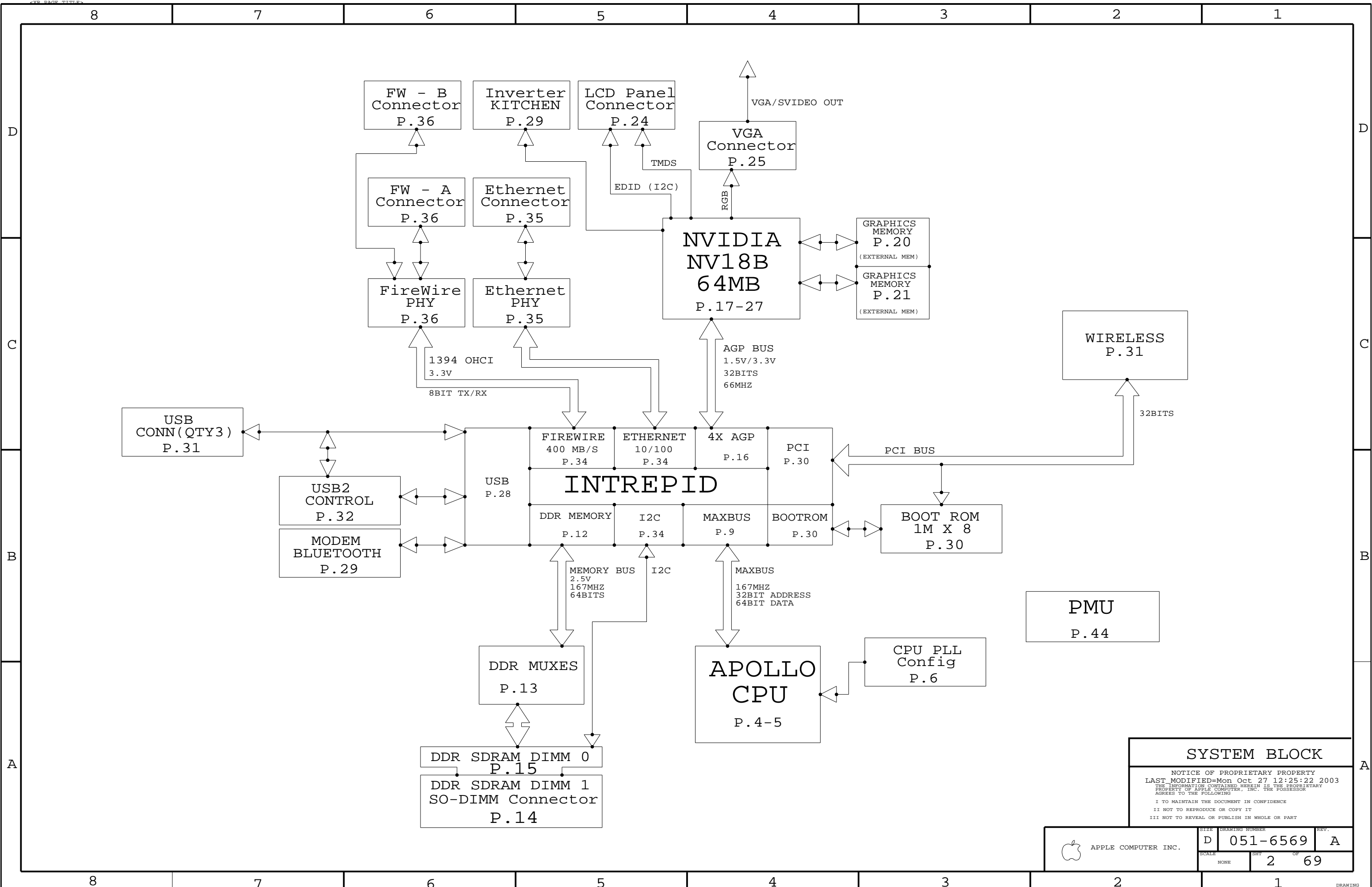
	RUN	SLEEP	SHUTDOWN
+2_5V_MAIN	ON	ON	OFF
+3V_MAIN	ON	ON	OFF
+5V_MAIN	ON	ON	OFF
+5V_SLEEP	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12V_SLEEP	ON	OFF	OFF
FW_PWR	ON	ON	OFF
+1.8V_SLEEP	ON	OFF	OFF
+MAXBUS_SLEEP	ON	OFF	OFF

SCHEMATIC AND PCB SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6569	1	SCHEM,MLB,Q59	SCH1	CRITICAL	
820-1599	1	PCB,MLB,IMACG4.A,B,C	PCB1	CRITICAL	
825-2029	1	LBL,SER #,BARCODE	PCB1		
056-1158	1	DESIGN GUIDE,MCO,IMACG4	PCB1	CRITICAL	
057-0085	1	DFM,PNLZN DWG,MLB,Q59	PCB1	CRITICAL	
630-XXXX	1	630-XXXX,PCBA,H,Q59,EEE XXX	HYNIX		OMIT
630-XXXX	1	630-XXXX,PCBA,S,Q59,EEE XXX	SAMSUNG		OMIT

PCB,UL RECOGNIZED, MIN.130 DEG. C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94. PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, TEMPERATURE RATING AND FLAME RATING.

DIMENSIONS ARE IN MILLIMETERS XX : _____ X.XX : _____ X.XXX : _____ ANGLES : _____ DO NOT SCALE DRAWING  THIRD ANGLE PROJECTION	METRIC		 Apple Computer Inc.																	
	<table border="1"> <tr> <td>DRAPPER</td> <td>/</td> <td>DESIGN CR</td> <td>/</td> </tr> <tr> <td>ENG APPD</td> <td>/</td> <td>MRG APPD</td> <td>/</td> </tr> <tr> <td>QA APPD</td> <td>/</td> <td>DESIGNER</td> <td>/</td> </tr> <tr> <td>RELEASE</td> <td>/</td> <td>SCALE</td> <td>NONE</td> </tr> </table>	DRAPPER	/	DESIGN CR	/	ENG APPD	/	MRG APPD	/	QA APPD	/	DESIGNER	/	RELEASE	/	SCALE	NONE	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
	DRAPPER	/	DESIGN CR	/																
	ENG APPD	/	MRG APPD	/																
QA APPD	/	DESIGNER	/																	
RELEASE	/	SCALE	NONE																	
MATERIAL/FINISH NOTED AS APPLICABLE		TITLE SCHEM,MLB,Q59,ABC																		
DRAWING NUMBER 051-6569		REV. A																		

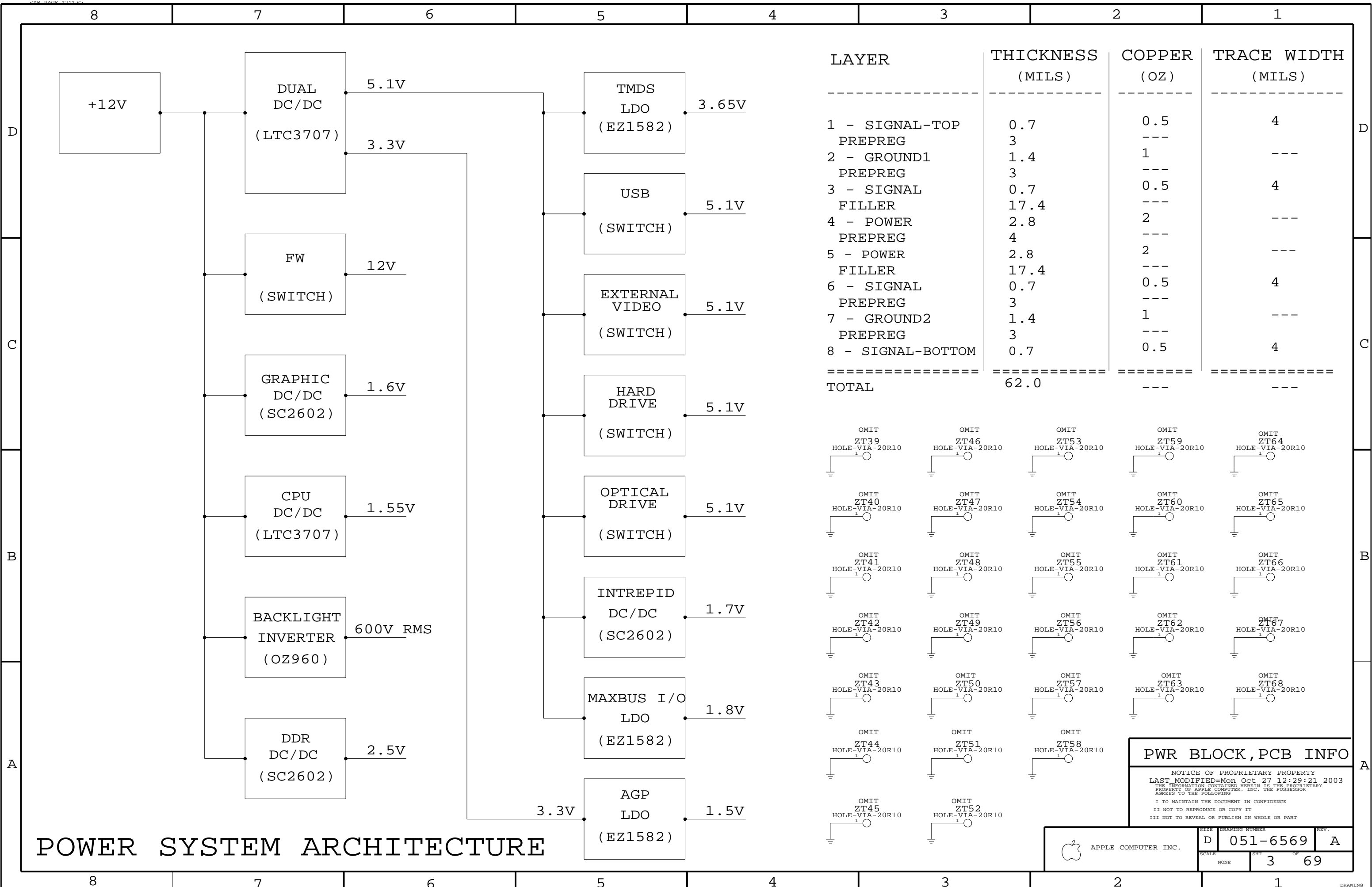


SYSTEM BLOCK

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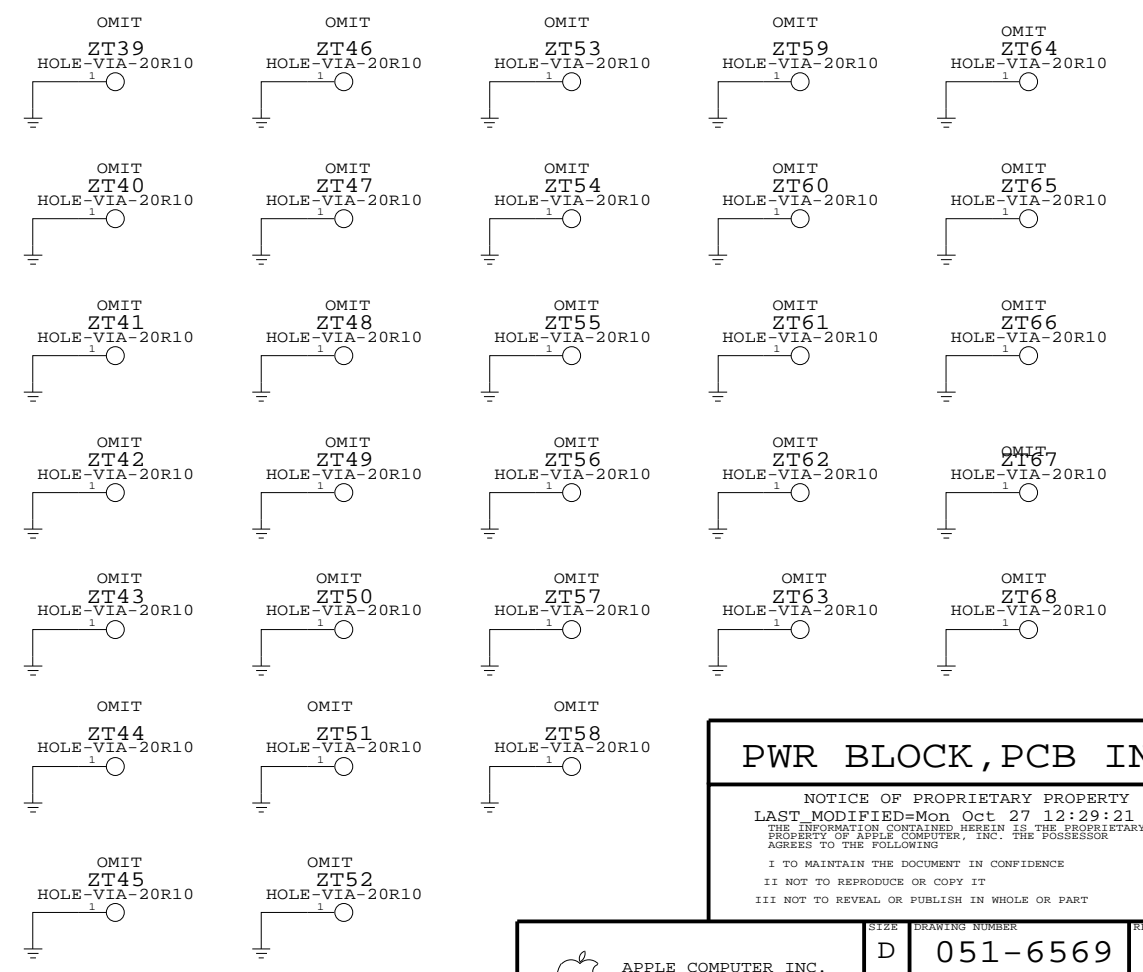
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	NONE	051-6569	A
		SCALE	SHT OF
		NONE	2 OF 69



POWER SYSTEM ARCHITECTURE

LAYER	THICKNESS (MILS)	COPPER (OZ)	TRACE WIDTH (MILS)
1 - SIGNAL-TOP	0.7	0.5	4
PREPREG	3	---	---
2 - GROUND1	1.4	1	---
PREPREG	3	---	---
3 - SIGNAL	0.7	0.5	4
FILLER	17.4	---	---
4 - POWER	2.8	2	---
PREPREG	4	---	---
5 - POWER	2.8	2	---
FILLER	17.4	---	---
6 - SIGNAL	0.7	0.5	4
PREPREG	3	---	---
7 - GROUND2	1.4	1	---
PREPREG	3	---	---
8 - SIGNAL-BOTTOM	0.7	0.5	4
=====	=====	=====	=====
TOTAL	62.0	---	---



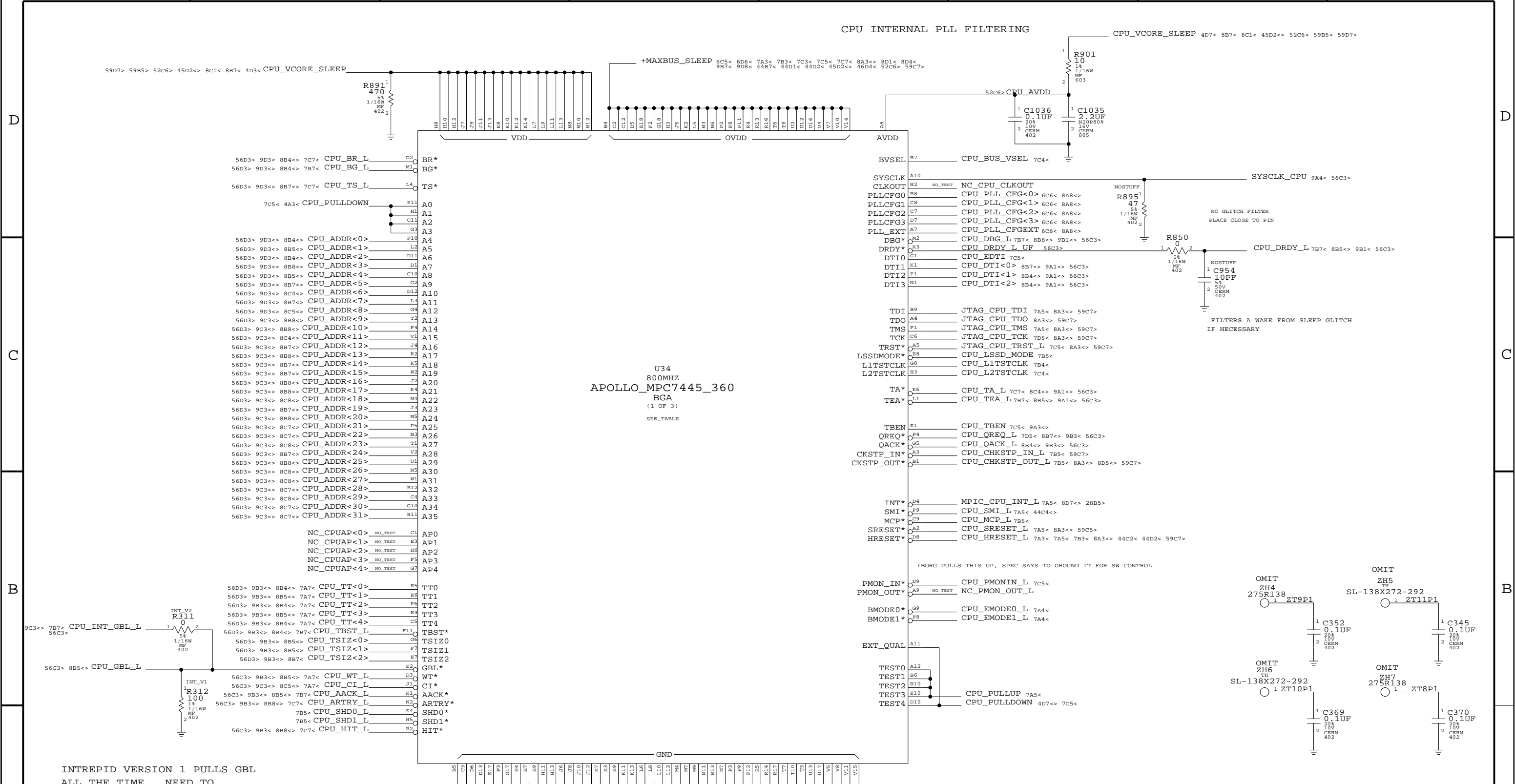
PWR BLOCK, PCB INFO

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NONE		3	69

CPU INTERNAL PLL FILTERING



U34
800MHZ
APOLLO MPC7445_360
BGA
(1 OF 3)
SEE_TABLE

INTREPID VERSION 1 PULLS GBL
ALL THE TIME. NEED TO
CUT THE TRACE AND YANK
DOWN HARD FOR SNOOPING.
FIXED IN INTREPID VERSION 2.

CPU MECHANICAL PARTS SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
875-1475	1	PAD, THERMAL, CPU, U34	U341	?	
870-1113	1	HEAT SINK, CPU, Q26, U34	U342	?	DEV
870-1114	1	CLIP, HEAT SINK, CPU, Q26, U34	U343	?	DEV
412-0042	1	SCREW, MACH, 3MM W, 8MM L, U34	U344	?	DEV
835-0251	1	NUT, 3MM, U34	U345	?	DEV

MPC7450 MAXBUS

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	D	051-6569	A
SCALE	SHT	OF	
NONE	4	69	

APOLLO_MPC7445_360

NC_CPUCRUD<0>	NO_TEST	F18	NC_F18
NC_CPUCRUD<1>	NO_TEST	F17	NC_F17
NC_CPUCRUD<2>	NO_TEST	F19	NC_F19
NC_CPUCRUD<3>	NO_TEST	H19	NC_H19
NC_CPUCRUD<4>	NO_TEST	H18	NC_H18
NC_CPUCRUD<5>	NO_TEST	H17	NC_H17
NC_CPUCRUD<6>	NO_TEST	H16	NC_H16
NC_CPUCRUD<7>	NO_TEST	E19	NC_E19
NC_CPUCRUD<8>	NO_TEST	D18	NC_D18
NC_CPUCRUD<9>	NO_TEST	F16	NC_F16
NC_CPUCRUD<10>	NO_TEST	G16	NC_G16
NC_CPUCRUD<11>	NO_TEST	D19	NC_D19
NC_CPUCRUD<12>	NO_TEST	F15	NC_F15
NC_CPUCRUD<13>	NO_TEST	G19	NC_G19
NC_CPUCRUD<14>	NO_TEST	E16	NC_E16
NC_CPUCRUD<15>	NO_TEST	D17	NC_D17
NC_CPUCRUD<16>	NO_TEST	D16	NC_D16

U34
800MHZ
BGA
(3 OF 3)

NC_CPUCRUD<17>	NO_TEST	P15	NC_P15
NC_CPUCRUD<18>	NO_TEST	L15	NC_L15
NC_CPUCRUD<19>	NO_TEST	N15	NC_N15
NC_CPUCRUD<20>	NO_TEST	P18	NC_P18
NC_CPUCRUD<21>	NO_TEST	N14	NC_N14
NC_CPUCRUD<22>	NO_TEST	M14	NC_M14
NC_CPUCRUD<23>	NO_TEST	M17	NC_M17
NC_CPUCRUD<24>	NO_TEST	N13	NC_N13
NC_CPUCRUD<25>	NO_TEST	N16	NC_N16
NC_CPUCRUD<26>	NO_TEST	M19	NC_M19
NC_CPUCRUD<27>	NO_TEST	M16	NC_M16
NC_CPUCRUD<28>	NO_TEST	P19	NC_P19
NC_CPUCRUD<29>	NO_TEST	N17	NC_N17
NC_CPUCRUD<30>	NO_TEST	M15	NC_M15
NC_CPUCRUD<31>	NO_TEST	L17	NC_L17
NC_CPUCRUD<32>	NO_TEST	L14	NC_L14
NC_CPUCRUD<33>	NO_TEST	K15	NC_K15
NC_CPUCRUD<34>	NO_TEST	J14	NC_J14
NC_CPUCRUD<35>	NO_TEST	J18	NC_J18
NC_CPUCRUD<36>	NO_TEST	J19	NC_J19
NC_CPUCRUD<37>	NO_TEST	J15	NC_J15
NC_CPUCRUD<38>	NO_TEST	K19	NC_K19
NC_CPUCRUD<39>	NO_TEST	J16	NC_J16
NC_CPUCRUD<40>	NO_TEST	H15	NC_H15
NC_CPUCRUD<41>	NO_TEST	L16	NC_L16
NC_CPUCRUD<42>	NO_TEST	P16	NC_P16
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NC_CPUCRUD<49>	NO_TEST	C19	NC_C19
NC_CPUCRUD<50>	NO_TEST	D15	NC_D15
NC_CPUCRUD<51>	NO_TEST	G15	NC_G15
NC_CPUCRUD<52>	NO_TEST	C18	NC_C18
NC_CPUCRUD<53>	NO_TEST	A16	NC_A16
NC_CPUCRUD<54>	NO_TEST	B19	NC_B19
NC_CPUCRUD<55>	NO_TEST	A19	NC_A19
NC_CPUCRUD<56>	NO_TEST	D14	NC_D14
NC_CPUCRUD<57>	NO_TEST	E15	NC_E15
NC_CPUCRUD<58>	NO_TEST	B15	NC_B15
NC_CPUCRUD<59>	NO_TEST	B17	NC_B17
NC_CPUCRUD<60>	NO_TEST	C17	NC_C17
NC_CPUCRUD<61>	NO_TEST	C16	NC_C16
NC_CPUCRUD<62>	NO_TEST	G13	NC_G13
NC_CPUCRUD<63>	NO_TEST	E14	NC_E14
NC_CPUCRUD<64>	NO_TEST	H14	NC_H14
NC_CPUCRUD<65>	NO_TEST	G14	NC_G14
NC_CPUCRUD<66>	NO_TEST	C15	NC_C15
NC_CPUCRUD<67>	NO_TEST	A17	NC_A17
NC_CPUCRUD<68>	NO_TEST	G12	NC_G12
NC_CPUCRUD<69>	NO_TEST	F14	NC_F14
NC_CPUCRUD<70>	NO_TEST	F13	NC_F13
NC_CPUCRUD<71>	NO_TEST	E13	NC_E13
NC_CPUCRUD<72>	NO_TEST	B16	NC_B16
NC_CPUCRUD<73>	NO_TEST	A15	NC_A15
NC_CPUCRUD<74>	NO_TEST	C14	NC_C14
NC_CPUCRUD<75>	NO_TEST	A18	NC_A18
NC_CPUCRUD<76>	NO_TEST	A13	NC_A13
NC_CPUCRUD<77>	NO_TEST	F12	NC_F12
NC_CPUCRUD<78>	NO_TEST	A14	NC_A14
NC_CPUCRUD<79>	NO_TEST	G11	NC_G11
NC_CPUCRUD<80>	NO_TEST	C13	NC_C13

NC_CPUCRUD<81>	NO_TEST	N12	NC_N12
NC_CPUCRUD<82>	NO_TEST	N18	NC_N18
NC_CPUCRUD<83>	NO_TEST	K17	NC_K17
NC_CPUCRUD<84>	NO_TEST	N19	NC_N19
NC_CPUCRUD<85>	NO_TEST	B18	NC_B18
NC_CPUCRUD<86>	NO_TEST	E12	NC_E12
NC_CPUCRUD<87>	NO_TEST	B13	NC_B13
NC_CPUCRUD<88>	NO_TEST	B14	NC_B14
NC_CPUCRUD<89>	NO_TEST	A6	NC_A6

APOLLO_MPC7445_360

56D3> 9D1<> 8C4<>	CPU_DATA<0>	R15	D0
56D3> 9D1<> 8C7<>	CPU_DATA<1>	M15	D1
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56D3> 9D1<> 8C5<>	CPU_DATA<3>	V16	D3
56D3> 9D1<> 8C7<>	CPU_DATA<4>	M16	D4
56D3> 9D1<> 8C8<>	CPU_DATA<5>	T15	D5
56D3> 9D1<> 8C4<>	CPU_DATA<6>	U15	D6
56D3> 9D1<> 8C8<>	CPU_DATA<7>	F14	D7
56D3> 9D1<> 8C5<>	CPU_DATA<8>	V13	D8
56D3> 9D1<> 8C4<>	CPU_DATA<9>	M13	D9
56D3> 9D1<> 8C7<>	CPU_DATA<10>	T13	D10
56D3> 9D1<> 8C5<>	CPU_DATA<11>	F13	D11
56D3> 9D1<> 8C5<>	CPU_DATA<12>	U14	D12
56D3> 9D1<> 8C7<>	CPU_DATA<13>	M14	D13
56D3> 9D1<> 8C8<>	CPU_DATA<14>	R12	D14
56D3> 9D1<> 8C5<>	CPU_DATA<15>	T12	D15
56D3> 9C1<> 8C4<>	CPU_DATA<16>	M12	D16
56D3> 9C1<> 8C7<>	CPU_DATA<17>	V12	D17
56D3> 9C1<> 8C4<>	CPU_DATA<18>	N11	D18
56D3> 9C1<> 8C4<>	CPU_DATA<19>	M10	D19
56D3> 9C1<> 8C4<>	CPU_DATA<20>	R11	D20
56D3> 9C1<> 8C8<>	CPU_DATA<21>	U11	D21
56D3> 9C1<> 8C7<>	CPU_DATA<22>	M11	D22
56D3> 9C1<> 8C8<>	CPU_DATA<23>	T11	D23
56D3> 9C1<> 8D4<>	CPU_DATA<24>	R10	D24
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56D3> 9C1<> 8B7<>	CPU_DATA<34>	T5	D34
56D3> 9C1<> 8B7<>	CPU_DATA<35>	U5	D35
56D3> 9C1<> 8A7<>	CPU_DATA<36>	M7	D36
56D3> 9C1<> 8D5<>	CPU_DATA<37>	R6	D37
56D3> 9C1<> 8D5<>	CPU_DATA<38>	F7	D38
56D3> 9C1<> 8D5<>	CPU_DATA<39>	V6	D39
56D3> 9C1<> 8D7<>	CPU_DATA<40>	F17	D40
56D3> 9C1<> 8C4<>	CPU_DATA<41>	R19	D41
56D3> 9B1<> 8C5<>	CPU_DATA<42>	V18	D42
56D3> 9B1<> 8C4<>	CPU_DATA<43>	R18	D43
56D3> 9B1<> 8C8<>	CPU_DATA<44>	V19	D44
56D3> 9B1<> 8C7<>	CPU_DATA<45>	T19	D45
56D3> 9B1<> 8C4<>	CPU_DATA<46>	U19	D46
56D3> 9B1<> 8C7<>	CPU_DATA<47>	M19	D47
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56D3> 9D8< 9B1<>	8C8<>	M18	D50
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56D3> 9C8< 9B1<>	8C5<>	T18	D52
56D3> 9C8< 9B1<>	8C7<>	T17	D53
56D3> 9C8< 9B1<>	8D7<>	M3	D54
56D3> 9C8< 9B1<>	8C5<>	V17	D55
56D3> 9B1<>	8D8<>	U4	D56
56D3> 9D5< 9B1<>	8D5<>	U8	D57
56D3> 9D5< 9B1<>	8D4<>	U7	D58
56D3> 9D5< 9B1<>	8D8<>	R7	D59
56D3> 9D5< 9B1<>	8D8<>	P6	D60
56D3> 9C5< 9B1<>	8D4<>	R8	D61
56D3> 9C5< 9B1<>	8D4<>	M8	D62
56D3> 9C5< 9B1<>	8D5<>	T8	D63

U34
800MHZ
BGA
(2 OF 3)

NC_CPUDP<0>	NO_TEST	T3	DP0
NC_CPUDP<1>	NO_TEST	M4	DP1
NC_CPUDP<2>	NO_TEST	T4	DP2
NC_CPUDP<3>	NO_TEST	M9	DP3
NC_CPUDP<4>	NO_TEST	M6	DP4
NC_CPUDP<5>	NO_TEST	V3	DP5
NC_CPUDP<6>	NO_TEST	N8	DP6
NC_CPUDP<7>	NO_TEST	M6	DP7

MPC7450 - 2

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SCALE	SHEET		OF
NONE	5		69

BOMOPTIONS FOR UPPER-SET OF RESISTORS

1200@133&1500@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167

667@133&833@167&733@133&917@167&800@133&1000@167&1067@133&1333@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&1867@133&2333@167&2133@133&2667@167

800@133&1000@167&867@133&1083@167&1067@133&1333@167&1200@133&1500@167&1733@133&2167@167&1867@133&2333@167&2133@133&2667@167

667@133&833@167&933@133&1167@167&1200@133&1500@167&1333@133&1667@167&1600@133&2000@167

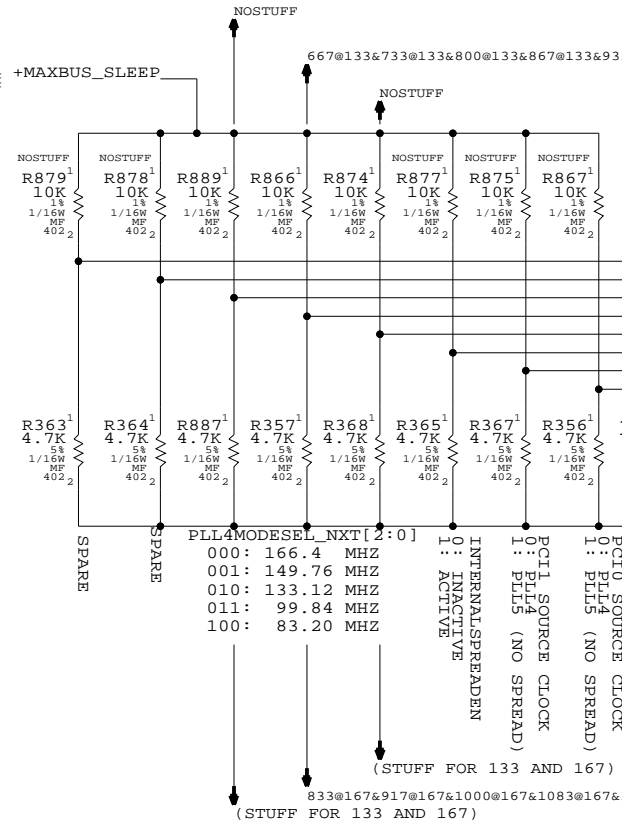
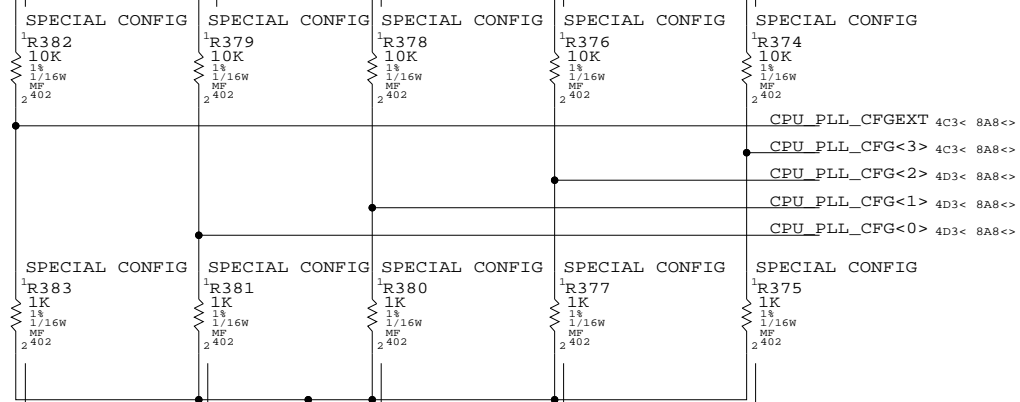
667@133&833@167&733@133&917@167&800@133&1000@167&867@133&1083@167&1000@133&1250@167&1200@133&1500@167&1467@133&1833@167&1600@133&2000@167&1733@133&2167@167&2000@133&2500@167&2133@133&2667@167

+MAXBUS_SLEEP 4D5< 6C5< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3<> 8D1< 8D4< 9B7< 9D8<
44B7< 44D1< 44D2< 45D2<> 46D4< 52C6> 59C7>

8D1< 8A3<> 7C7< 7C5< 7C3< 7B3< 7A3< 6D8< 4D5<
46D4< 45D2<> 44D1< 44B7< 9D8< 9B7< 8D4<

CPU FREQUENCY CONFIGURATION
(SUPPORTED CPU & BUS SPEEDS)

MULTIPLIER (BUS-TO-CORE)	CORE FREQUENCY (AT BUS FREQUENCY)		CPU_PLL_CFG
	167MHZ	133MHZ	E 0123 HEX
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
9.0X	1500	1200	1 0111 17
10.0X	1667	1333	1 1010 1A
11.0X	1833	1467	1 1001 19
12.0X	2000	1600	1 1011 1B
13.0X	2167	1733	1 0101 15
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D



44B8< CPU_PLL_STOP

933@133&1167@167&1067@133&1333@167&1333@133&1667@167&1867@133&2333@167
 733@133&917@167&800@133&1000@167&867@133&1083@167&1000@133&1250@167&1067@133&1333@167&1467@133&1833@167&1733@133&2167@167&1867@133&2333@167&2000@133&2500@167&2133@133&2667@167
 667@133&833@167&733@133&917@167&933@133&1167@167&1000@133&1250@167&1333@133&1667@167&1467@133&1833@167&1600@133&2000@167&2000@133&2500@167
 867@133&1083@167&933@133&1167@167&1000@133&1250@167&1200@133&1500@167&1733@133&2167@167&2000@133&2500@167
 667@133&833@167&733@133&917@167&800@133&1000@167&867@133&1083@167&933@133&1167@167&1000@133&1250@167&1067@133&1333@167

CPU SPEED & BUS RATIO SUPPORT
 THE CONFIGURATION RESISTORS BELOW ARE SELF CONFIGURING
 WHEN THE ENGINEER SELECTS THE APPROPRIATE CPU AND
 BUS SPEED BOM OPTION, THE APPROPRIATE RESISTORS ARE
 AUTOMATICALLY SELECTED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S2799	1	IC, APOLLO6, S1COH, 1.0GHZ, 1.5V+30/-130MV, 28W, 85C	U34	CRITICAL	1000@167
337S2801	1	IC, APOLLO6, S1COH, 1.25GHZ, 1.57V+70/-70MV, 35W, 85C	U34	CRITICAL	1250@167

CPU BUS RATIO BITS

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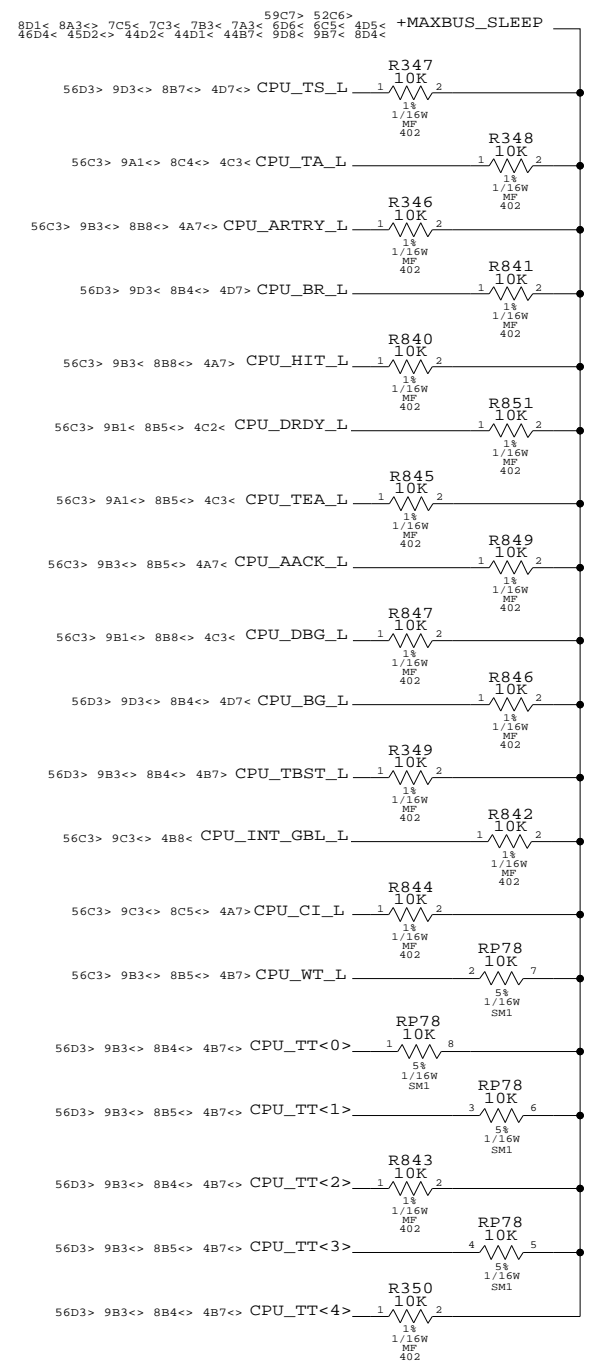
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SCALE		SHT	OF
NONE		6	69

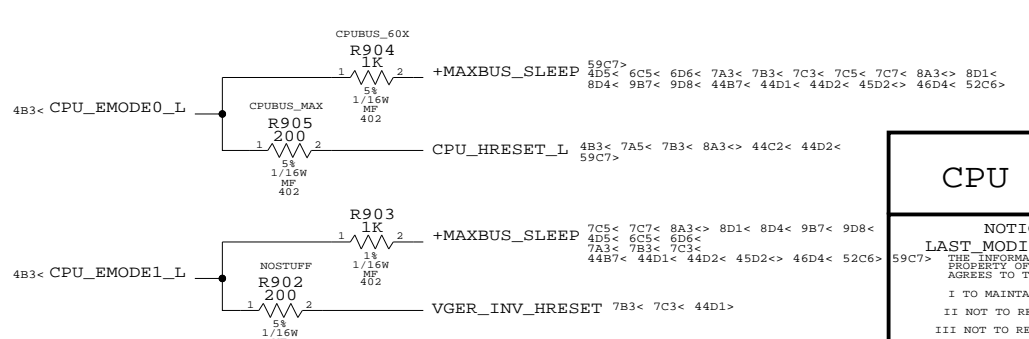
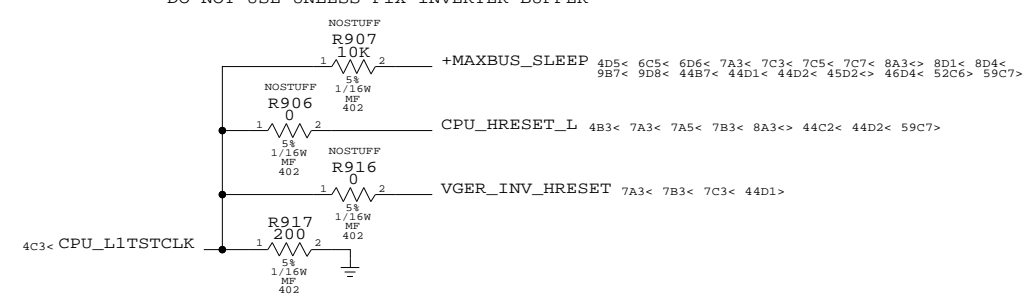
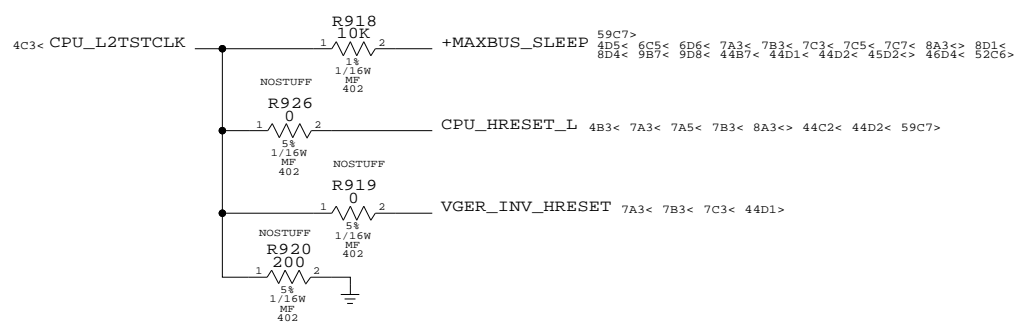
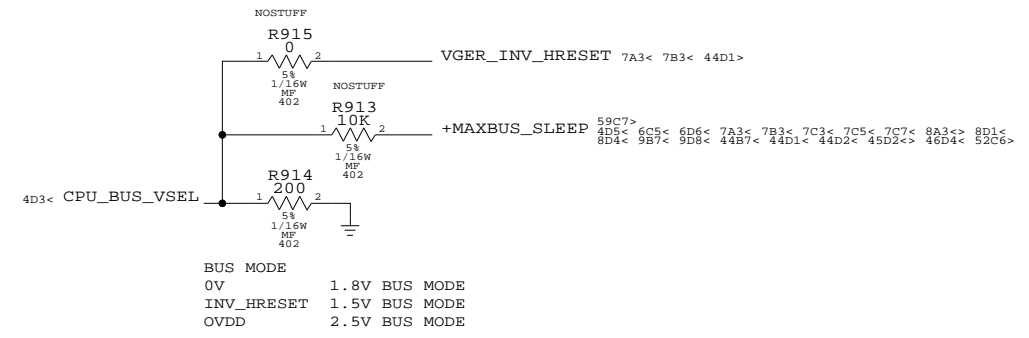
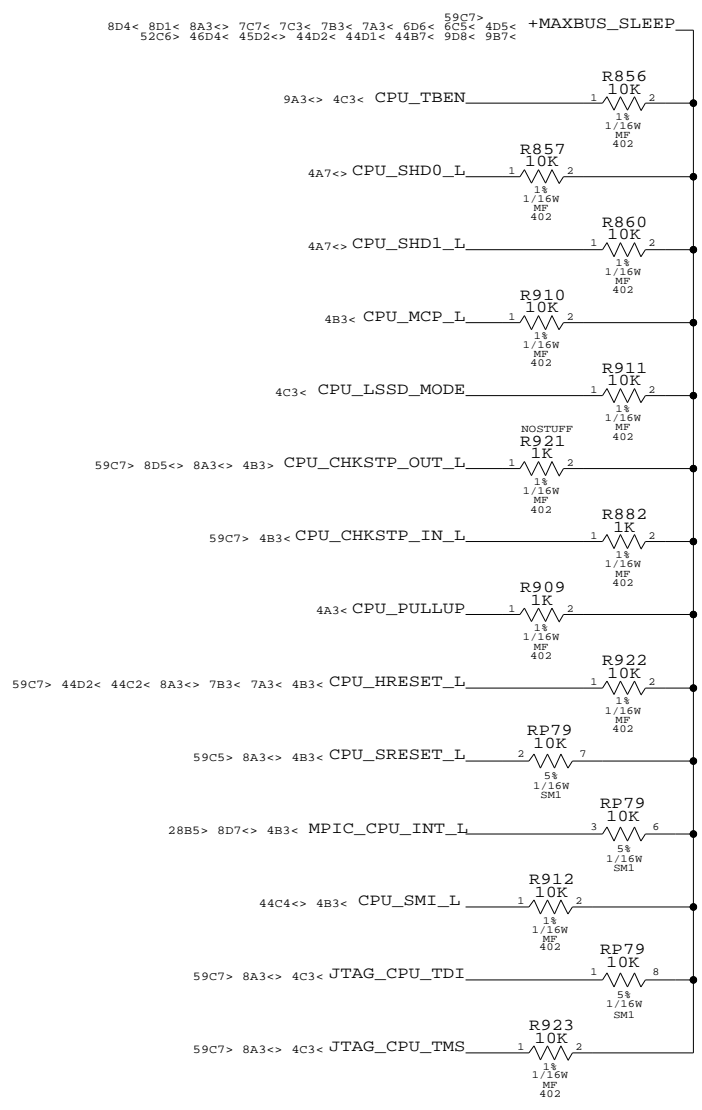
BMODE <0> <1>	MSSCR0 <16:17>	Sys Bus	Vger ID	Addr Drve
L L	1 1	???	01	yes unavail
L !hr	1 0	Max	01	yes unavail
L hr	1 1	???	00	yes unavail
L H	1 0	Max	00	yes unavail
!hr L	0 1	MB+	01	yes unavail
!hr !hr	0 0	60x	01	yes unavail
!hr hr	0 1	MB+	00	yes unavail
!hr H	0 0	60x	00	yes unavail
hr L	1 1	???	01	norm unavail
hr !hr	1 0	Max	01	norm
hr hr	1 1	???	00	norm unavail
HR H	1 0	MAX	00	NORM <- DEFAULT
H L	0 1	MB+	01	norm unavail
H !hr	0 0	60x	01	norm
H hr	0 1	MB+	00	norm unavail
H H	0 0	60x	00	norm

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L	HIGH	60X BUS MODE
CPU_BUS_VSEL	CPU_HRESET_L	MAX BUS MODE
	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE
CPU_L3_VSEL	CPU_HRESET_L or L3_OVDD	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_H	1.5V INTERFACE

MAXBUS PULL-UPS



MPC7450 PULL-UPS



CPU CONFIG OPTIONS

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SCALE: NONE SHEET: 7 OF 69

DRAWING NUMBER: D 051-6569 REV: A

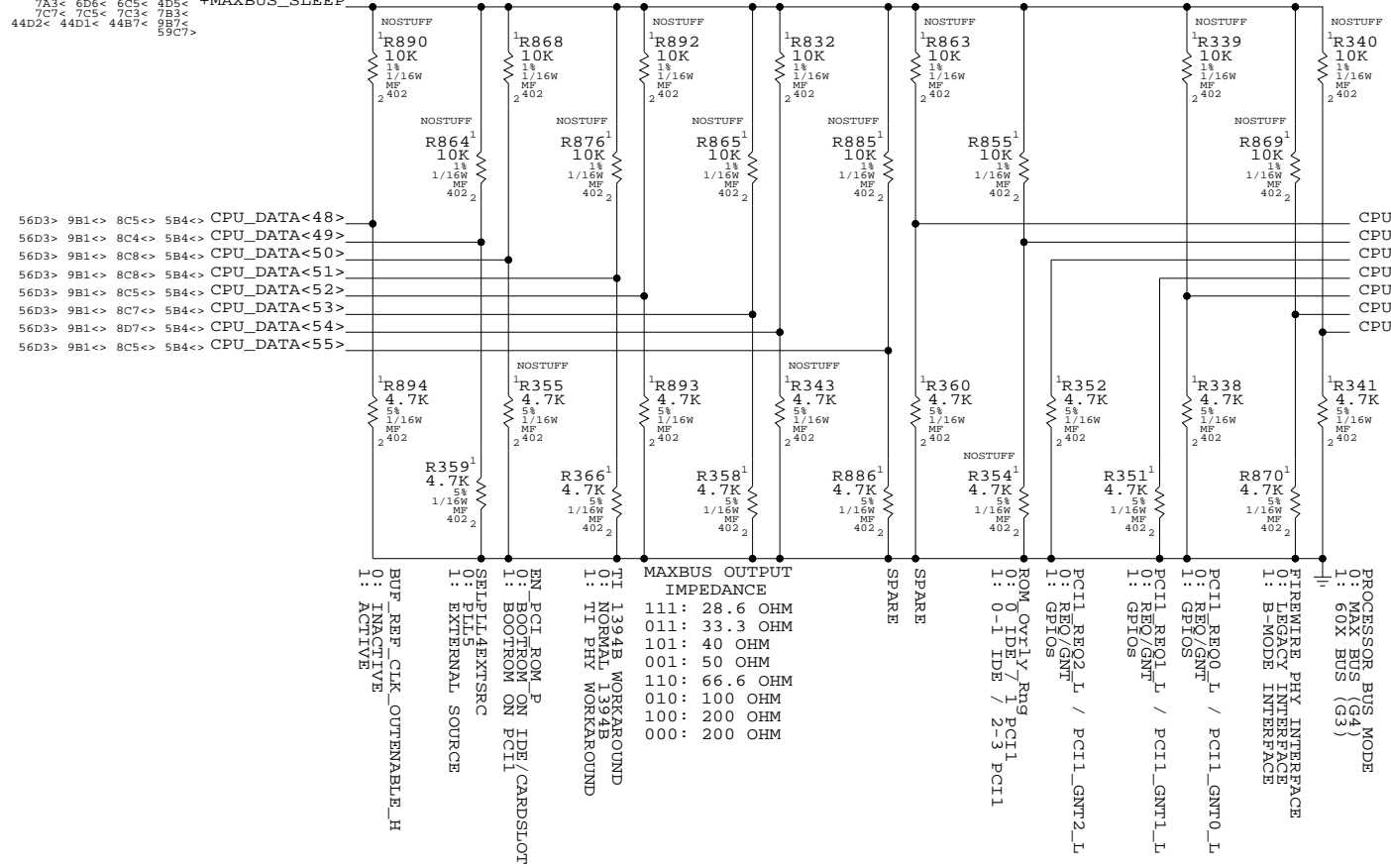
INTREPID BOOT STRAPS

INTREPID V1.1 IS 133MHZ ONLY

52D3> 30D5< 28D6<> 16D6< +1_5V_INTREPID_PLL

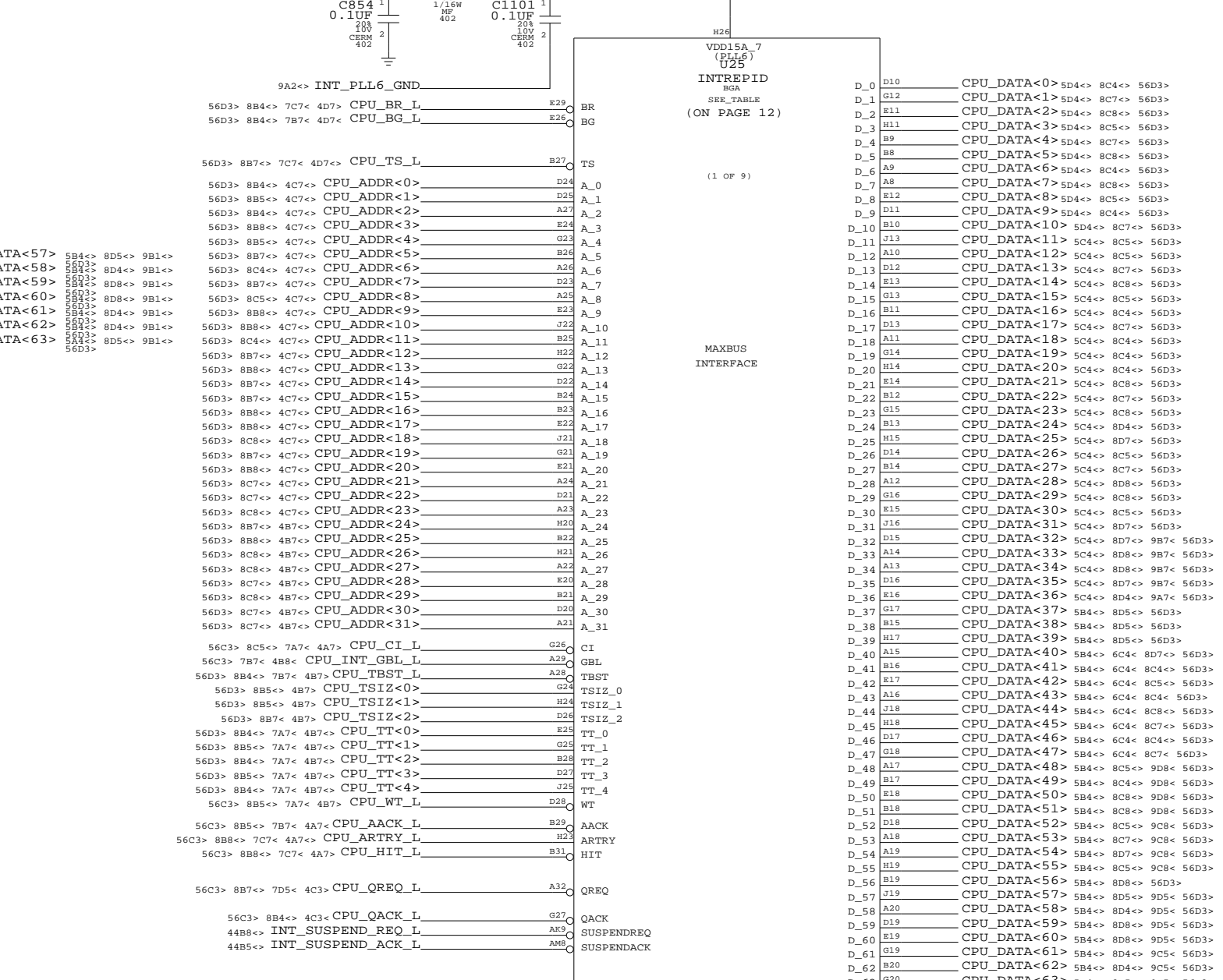
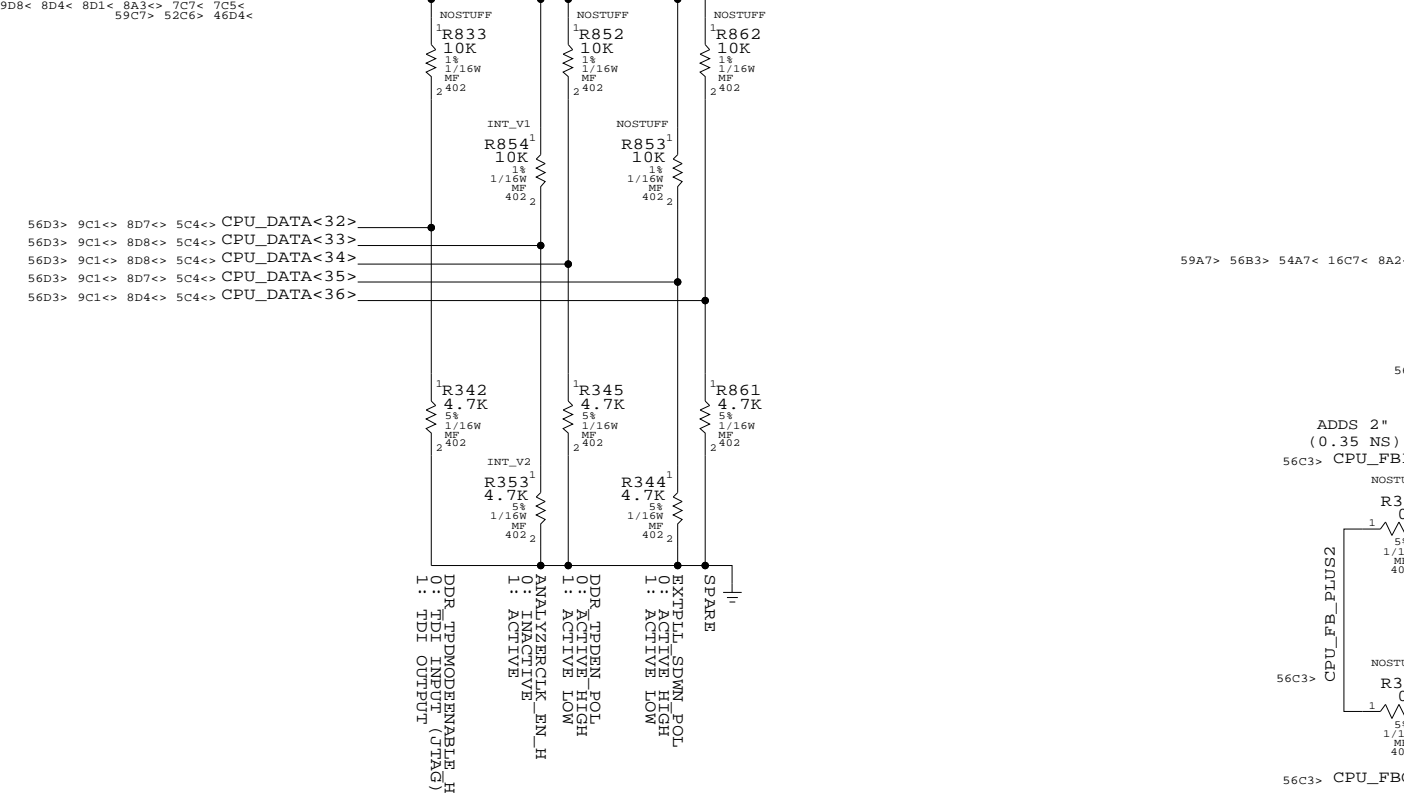
52C6> 46D4< 45D2<>
8D4< 8D1< 8A3<>
7A3< 6D6< 6C5< 4D5<
7C7< 7C5< 7C3< 7B3<
44D2< 44D1< 44B7< 5B7<
5C7>

BITS 48 - 63

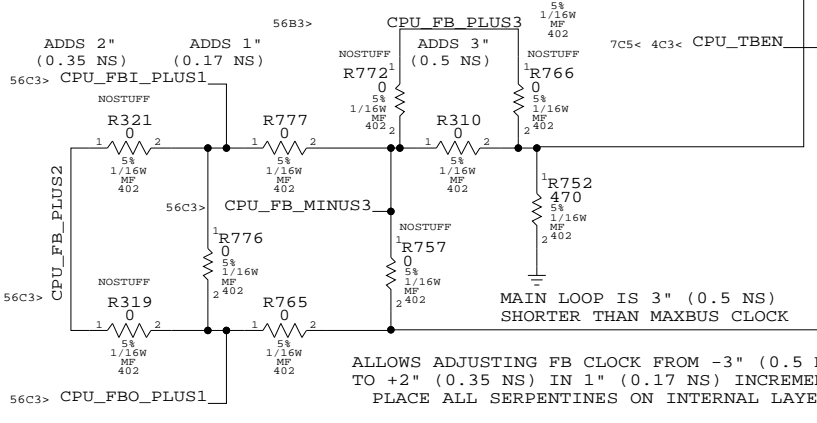


45D2<> 44D2< 44D1< 44B7<
7C3< 7B3< 7A3< 6D6< 6C5< 4D5<
9D8< 8D4< 8D1< 8A3<> 7C7< 7C5<
5C7> 52C6> 46D4<

BITS 32 - 39



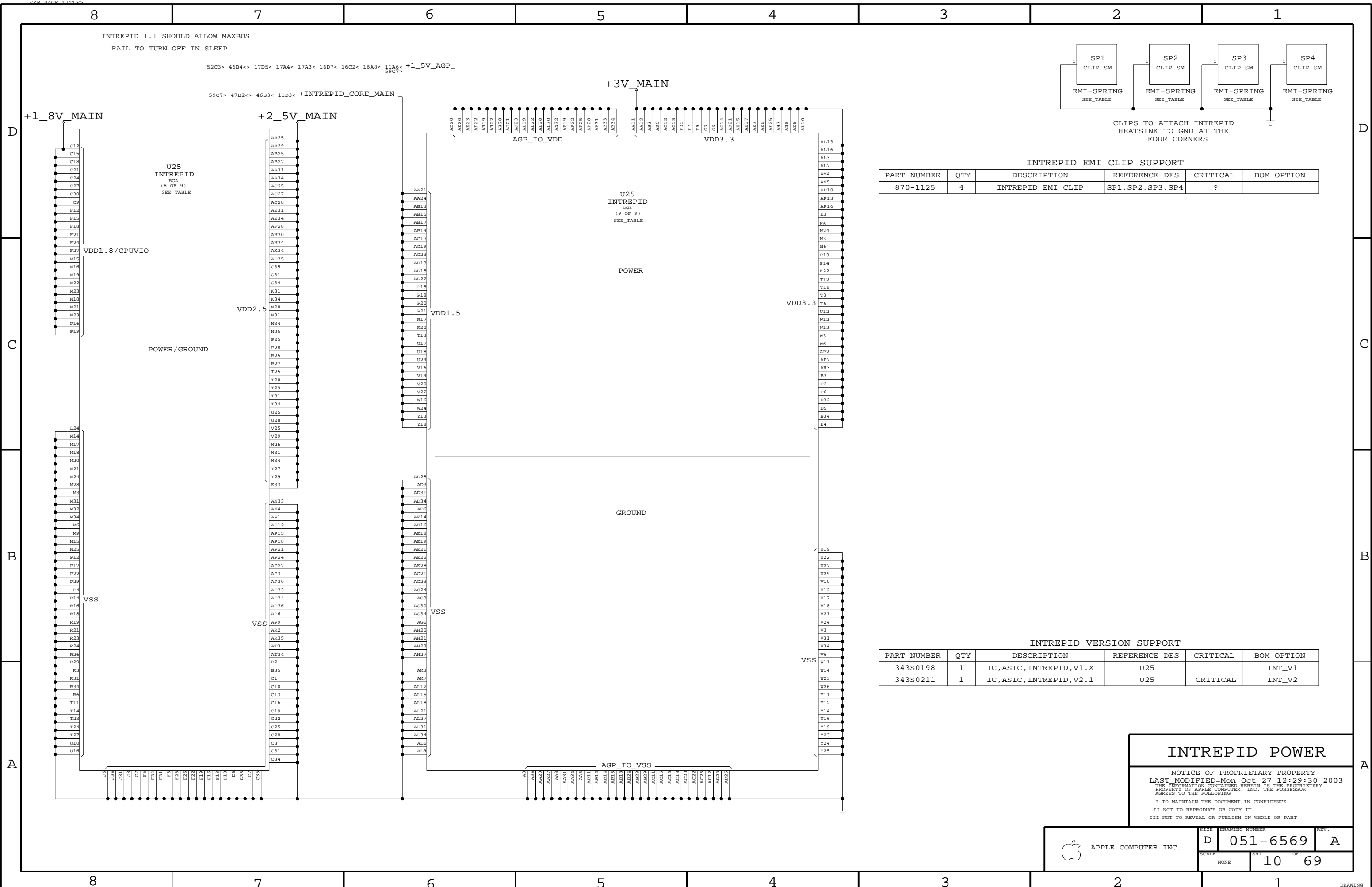
59A7> 56B3> 54A7< 16C7< 8A2< INT_ANALYZER_CLK



ALLOWS ADJUSTING FB CLOCK FROM -3" (0.5 NS) TO +2" (0.35 NS) IN 1" (0.17 NS) INCREMENTS PLACE ALL SERPENTINES ON INTERNAL LAYER

INTREPID MAX
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF, PART NUMBER. Values: D, 051-6569, A, NONE, 9, 69.



INTREPID EMI CLIP SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1125	4	INTREPID EMI CLIP	SP1,SP2,SP3,SP4	?	

INTREPID VERSION SUPPORT

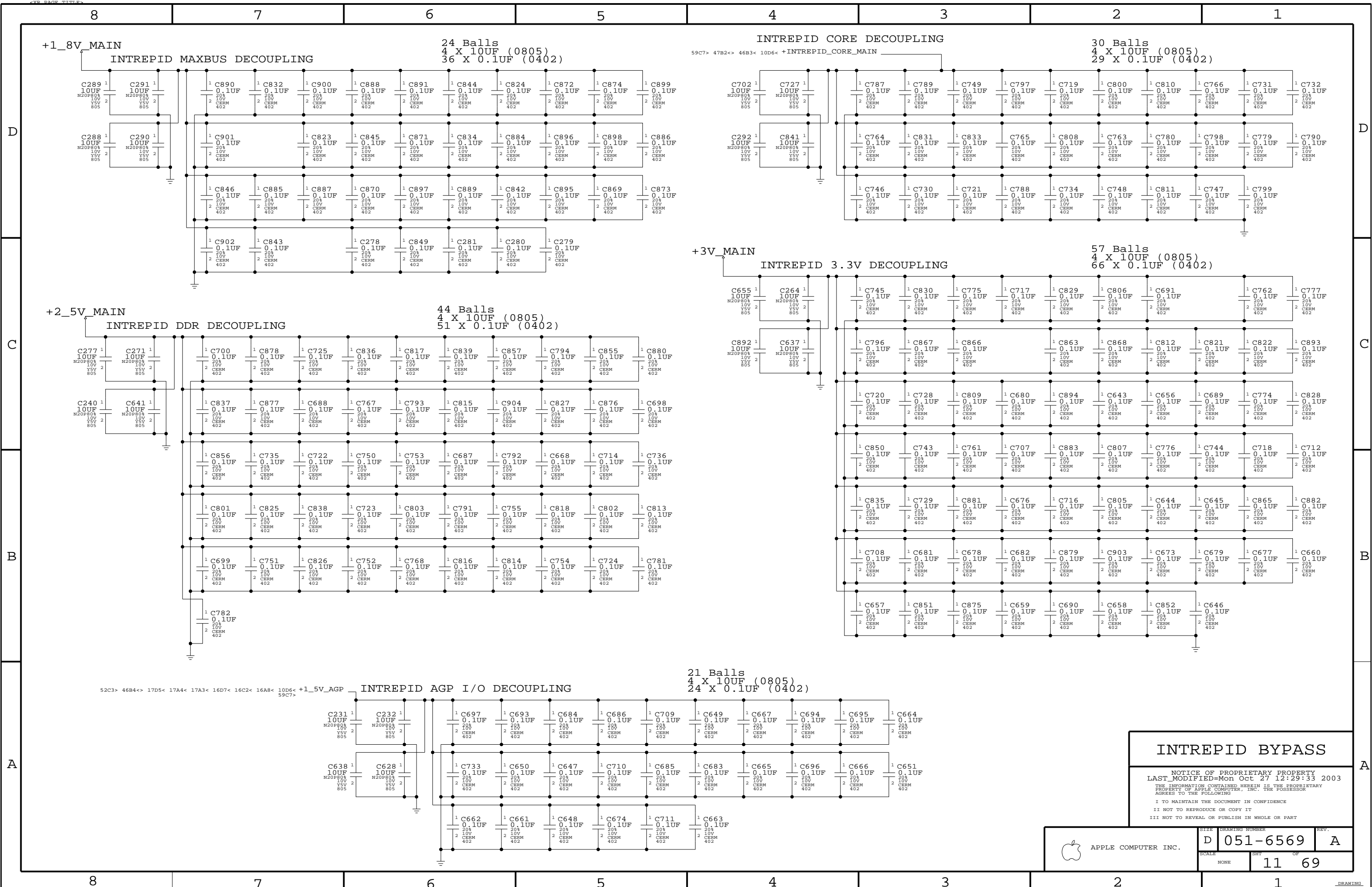
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0198	1	IC,ASIC,INTREPID,V1.X	U25		INT_V1
343S0211	1	IC,ASIC,INTREPID,V2.1	U25	CRITICAL	INT_V2

INTREPID POWER

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SCALE		SHT	OF
		10	69



INTREPID BYPASS

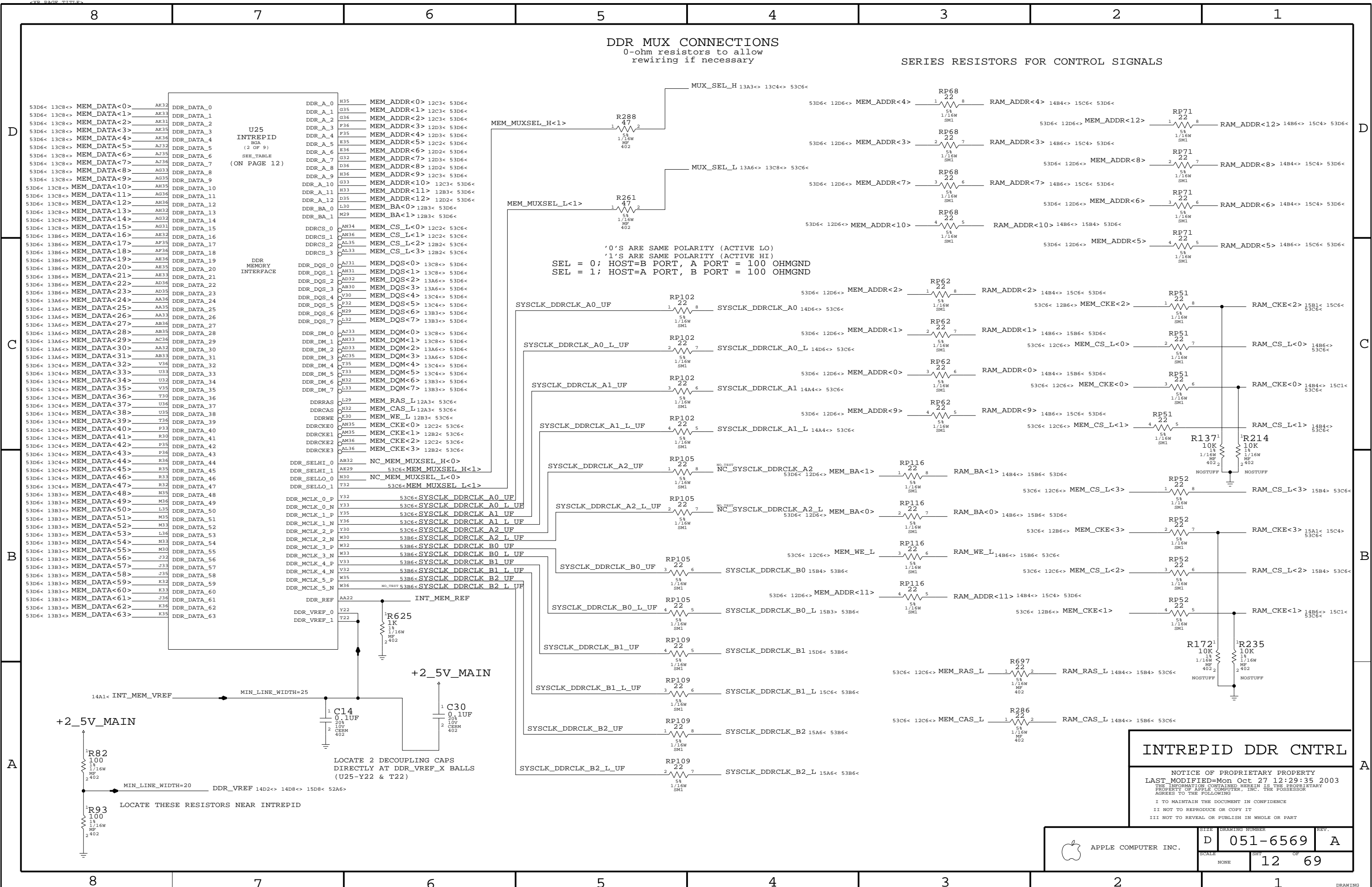
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APPLE COMPUTER INC.	SIZE DRAWING NUMBER REV. D 051-6569 A
	SCALE SHEET OF NONE 11 69

DDR MUX CONNECTIONS
0-ohm resistors to allow
rewiring if necessary

SERIES RESISTORS FOR CONTROL SIGNALS



D

C

B

A

D

C

B

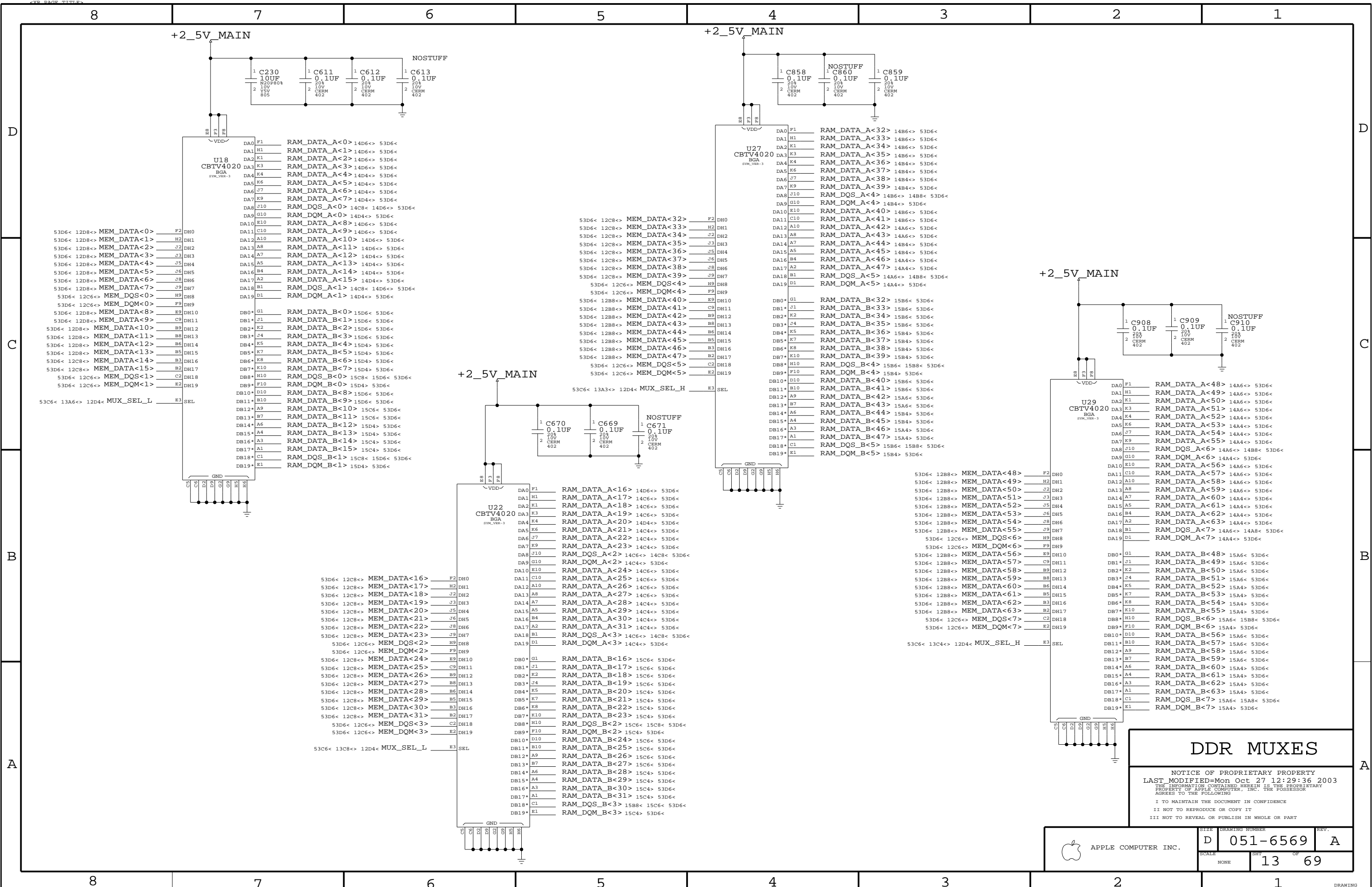
A

MEM_DATA<n>	MEM_ADDR<n>	MEM_CS_L<n>	MEM_CKE<n>	MEM_WE_L	MEM_RAS_L	MEM_CAS_L
53D6< 13C8<> MEM_DATA<0>	AK32	DDR_DATA_0	DDR_A_0	H35	MEM_ADDR<0>	12C3< 53D6<
53D6< 13C8<> MEM_DATA<1>	AK33	DDR_DATA_1	DDR_A_1	G35	MEM_ADDR<1>	12C3< 53D6<
53D6< 13C8<> MEM_DATA<2>	AK31	DDR_DATA_2	DDR_A_2	G36	MEM_ADDR<2>	12C3< 53D6<
53D6< 13C8<> MEM_DATA<3>	AK35	DDR_DATA_3	DDR_A_3	F36	MEM_ADDR<3>	12D3< 53D6<
53D6< 13C8<> MEM_DATA<4>	AK36	DDR_DATA_4	DDR_A_4	F35	MEM_ADDR<4>	12D3< 53D6<
53D6< 13C8<> MEM_DATA<5>	AJ32	DDR_DATA_5	DDR_A_5	E35	MEM_ADDR<5>	12C2< 53D6<
53D6< 13C8<> MEM_DATA<6>	AJ35	DDR_DATA_6	DDR_A_6	E36	MEM_ADDR<6>	12D2< 53D6<
53D6< 13C8<> MEM_DATA<7>	AJ36	DDR_DATA_7	DDR_A_7	G32	MEM_ADDR<7>	12D3< 53D6<
53D6< 13C8<> MEM_DATA<8>	AG33	DDR_DATA_8	DDR_A_8	D36	MEM_ADDR<8>	12D2< 53D6<
53D6< 13C8<> MEM_DATA<9>	AG35	DDR_DATA_9	DDR_A_9	H36	MEM_ADDR<9>	12C3< 53D6<
53D6< 13C8<> MEM_DATA<10>	AH35	DDR_DATA_10	DDR_A_10	G33	MEM_ADDR<10>	12C3< 53D6<
53D6< 13C8<> MEM_DATA<11>	AG36	DDR_DATA_11	DDR_A_11	H33	MEM_ADDR<11>	12B3< 53D6<
53D6< 13C8<> MEM_DATA<12>	AH36	DDR_DATA_12	DDR_A_12	D35	MEM_ADDR<12>	12D2< 53D6<
53D6< 13C8<> MEM_DATA<13>	AH32	DDR_DATA_13	DDR_BA_0	L30	MEM_BA<0>	12B3< 53D6<
53D6< 13C8<> MEM_DATA<14>	AG32	DDR_DATA_14	DDR_BA_1	M29	MEM_BA<1>	12B3< 53D6<
53D6< 13C8<> MEM_DATA<15>	AG31	DDR_DATA_15	DDRCRS_0	AN34	MEM_CS_L<0>	12C2< 53C6<
53D6< 13B6<> MEM_DATA<16>	AE32	DDR_DATA_16	DDRCRS_1	AN36	MEM_CS_L<1>	12C2< 53C6<
53D6< 13B6<> MEM_DATA<17>	AF35	DDR_DATA_17	DDRCRS_2	AL35	MEM_CS_L<2>	12B2< 53C6<
53D6< 13B6<> MEM_DATA<18>	AF36	DDR_DATA_18	DDRCRS_3	AL33	MEM_CS_L<3>	12B2< 53C6<
53D6< 13B6<> MEM_DATA<19>	AE36	DDR_DATA_19	DDR_DQS_0	AJ31	MEM_DQS<0>	13C8<> 53D6<
53D6< 13B6<> MEM_DATA<20>	AE35	DDR_DATA_20	DDR_DQS_1	AH31	MEM_DQS<1>	13C8<> 53D6<
53D6< 13B6<> MEM_DATA<21>	AE33	DDR_DATA_21	DDR_DQS_2	AD32	MEM_DQS<2>	13A6<> 53D6<
53D6< 13B6<> MEM_DATA<22>	AD36	DDR_DATA_22	DDR_DQS_3	AB30	MEM_DQS<3>	13A6<> 53D6<
53D6< 13B6<> MEM_DATA<23>	AD35	DDR_DATA_23	DDR_DQS_4	F30	MEM_DQS<4>	13A6<> 53D6<
53D6< 13A6<> MEM_DATA<24>	AA36	DDR_DATA_24	DDR_DQS_5	F32	MEM_DQS<5>	13C4<> 53D6<
53D6< 13A6<> MEM_DATA<25>	AA35	DDR_DATA_25	DDR_DQS_6	W29	MEM_DQS<6>	13B3<> 53D6<
53D6< 13A6<> MEM_DATA<26>	AA33	DDR_DATA_26	DDR_DQS_7	L32	MEM_DQS<7>	13B3<> 53D6<
53D6< 13A6<> MEM_DATA<27>	AB36	DDR_DATA_27	DDR_DM_0	AJ33	MEM_DQM<0>	13C8<> 53D6<
53D6< 13A6<> MEM_DATA<28>	AB35	DDR_DATA_28	DDR_DM_1	AH33	MEM_DQM<1>	13C8<> 53D6<
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53D6< 13A6<> MEM_DATA<30>	AA32	DDR_DATA_30	DDR_DM_3	AC35	MEM_DQM<3>	13A6<> 53D6<
53D6< 13A6<> MEM_DATA<31>	AB33	DDR_DATA_31	DDR_DM_4	F35	MEM_DQM<4>	13C4<> 53D6<
53D6< 13C4<> MEM_DATA<32>	V36	DDR_DATA_32	DDR_DM_5	F33	MEM_DQM<5>	13C4<> 53D6<
53D6< 13C4<> MEM_DATA<33>	U33	DDR_DATA_33	DDR_DM_6	N32	MEM_DQM<6>	13B3<> 53D6<
53D6< 13C4<> MEM_DATA<34>	U32	DDR_DATA_34	DDR_DM_7	L33	MEM_DQM<7>	13B3<> 53D6<
53D6< 13C4<> MEM_DATA<35>	V35	DDR_DATA_35	DDRRAS	L29	MEM_RAS_L	12A3< 53C6<
53D6< 13C4<> MEM_DATA<36>	T30	DDR_DATA_36	DDRCAS	H32	MEM_CAS_L	12A3< 53C6<
53D6< 13C4<> MEM_DATA<37>	U36	DDR_DATA_37	DDRWE	E30	MEM_WE_L	12B3< 53C6<
53D6< 13C4<> MEM_DATA<38>	U35	DDR_DATA_38	DDRCKE0	AN35	MEM_CKE<0>	12C2< 53C6<
53D6< 13C4<> MEM_DATA<39>	T36	DDR_DATA_39	DDRCKE1	AM35	MEM_CKE<1>	12B2< 53C6<
53D6< 13C4<> MEM_DATA<40>	R30	DDR_DATA_40	DDRCKE2	AM36	MEM_CKE<2>	12C2< 53C6<
53D6< 13C4<> MEM_DATA<41>	P33	DDR_DATA_41	DDRCKE3	AL36	MEM_CKE<3>	12B2< 53C6<
53D6< 13C4<> MEM_DATA<42>	P35	DDR_DATA_42	DDR_SELHI_0	AB32	NC_MEM_MUXSEL_H<0>	
53D6< 13C4<> MEM_DATA<43>	P36	DDR_DATA_43	DDR_SELHI_1	R36	53C6<MEM_MUXSEL_H<1>	
53D6< 13C4<> MEM_DATA<44>	R35	DDR_DATA_44	DDR_SELLO_0	AE29	53C6<MEM_MUXSEL_L<0>	
53D6< 13C4<> MEM_DATA<45>	R33	DDR_DATA_45	DDR_SELLO_1	N30	NC_MEM_MUXSEL_L<1>	
53D6< 13C4<> MEM_DATA<46>	R32	DDR_DATA_46	DDR_MCLK_0_P	Y32	53C6<SYSCLK_DDRCLK_A0_UF	
53D6< 13B3<> MEM_DATA<47>	N35	DDR_DATA_47	DDR_MCLK_0_N	Y33	53C6<SYSCLK_DDRCLK_A0_L_UF	
53D6< 13B3<> MEM_DATA<48>	M36	DDR_DATA_48	DDR_MCLK_1_P	Y35	53C6<SYSCLK_DDRCLK_A1_UF	
53D6< 13B3<> MEM_DATA<49>	M35	DDR_DATA_49	DDR_MCLK_1_N	Y36	53C6<SYSCLK_DDRCLK_A1_L_UF	
53D6< 13B3<> MEM_DATA<50>	L35	DDR_DATA_50	DDR_MCLK_2_P	Y30	53C6<SYSCLK_DDRCLK_A2_UF	
53D6< 13B3<> MEM_DATA<51>	L36	DDR_DATA_51	DDR_MCLK_2_N	W30	53B6<SYSCLK_DDRCLK_A2_L_UF	
53D6< 13B3<> MEM_DATA<52>	M33	DDR_DATA_52	DDR_MCLK_3_P	W32	53B6<SYSCLK_DDRCLK_B0_UF	
53D6< 13B3<> MEM_DATA<53>	M30	DDR_DATA_53	DDR_MCLK_3_N	W33	53B6<SYSCLK_DDRCLK_B0_L_UF	
53D6< 13B3<> MEM_DATA<54>	J32	DDR_DATA_54	DDR_MCLK_4_P	V33	53B6<SYSCLK_DDRCLK_B1_UF	
53D6< 13B3<> MEM_DATA<55>	J33	DDR_DATA_55	DDR_MCLK_4_N	V32	53B6<SYSCLK_DDRCLK_B1_L_UF	
53D6< 13B3<> MEM_DATA<56>	J35	DDR_DATA_56	DDR_MCLK_5_P	W35	53B6<SYSCLK_DDRCLK_B2_UF	
53D6< 13B3<> MEM_DATA<57>	K32	DDR_DATA_57	DDR_MCLK_5_N	W36	53B6<SYSCLK_DDRCLK_B2_L_UF	
53D6< 13B3<> MEM_DATA<58>	K33	DDR_DATA_58	DDR_REF	AA22	INT_MEM_REF	
53D6< 13B3<> MEM_DATA<59>	K36	DDR_DATA_59	DDR_VREF_0	Y22		
53D6< 13B3<> MEM_DATA<60>	K35	DDR_DATA_60	DDR_VREF_1	T22		
53D6< 13B3<> MEM_DATA<61>		DDR_DATA_61				
53D6< 13B3<> MEM_DATA<62>		DDR_DATA_62				
53D6< 13B3<> MEM_DATA<63>		DDR_DATA_63				

INTREPID DDR CNTRL

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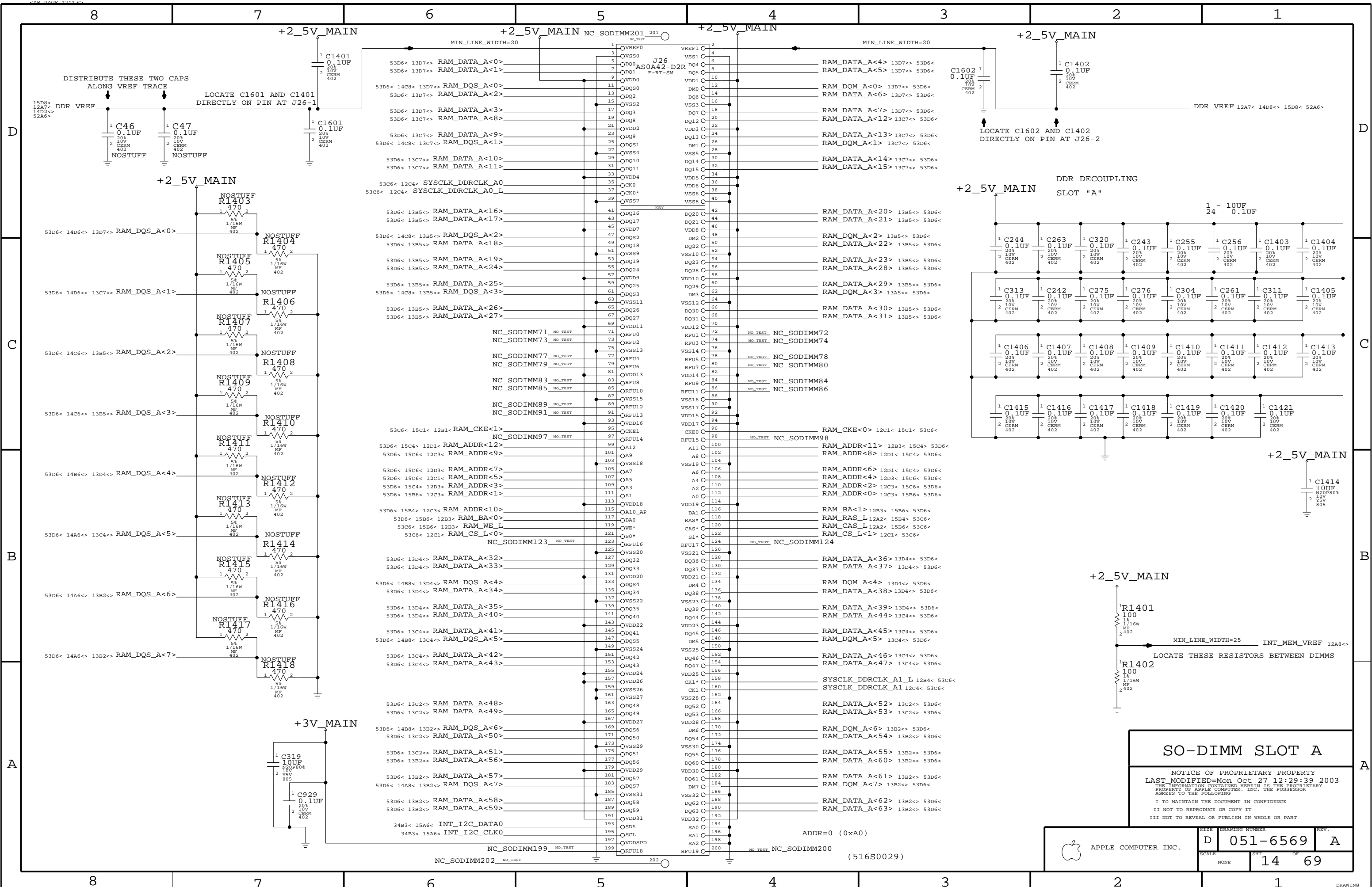
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DDR MUXES

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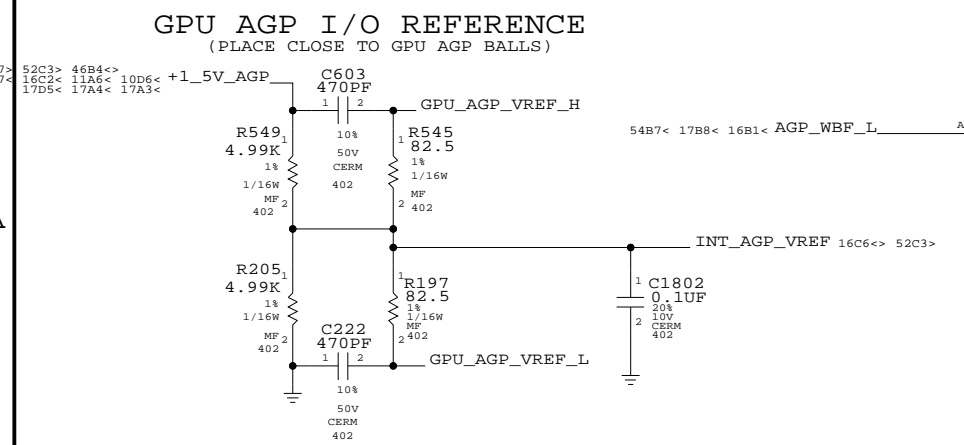
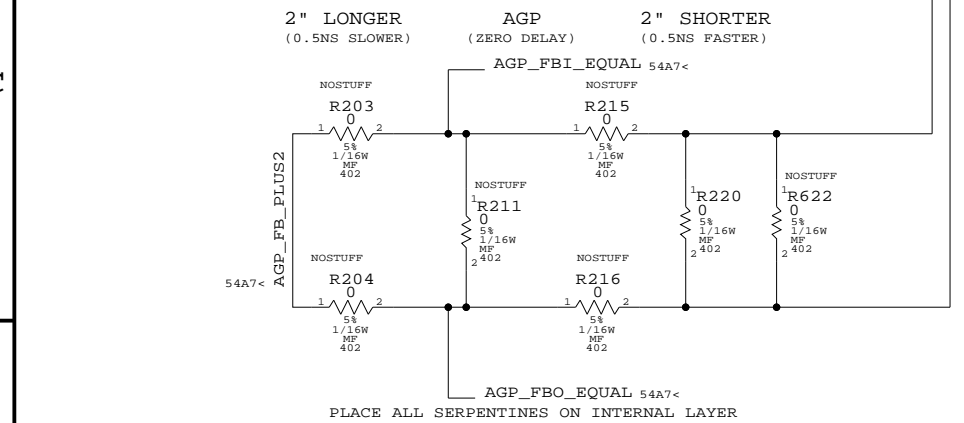
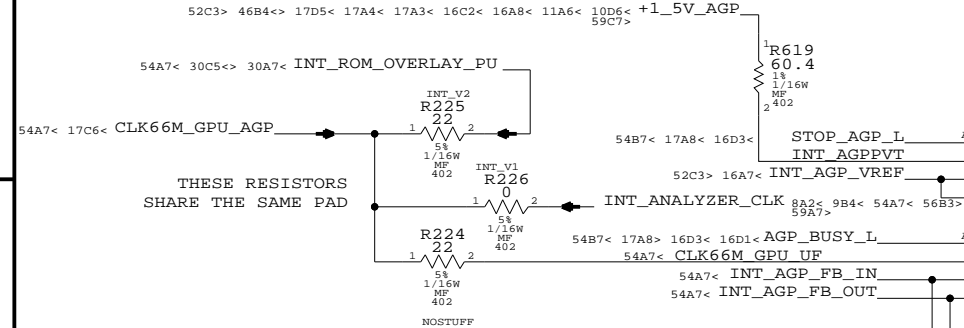
SO-DIMM SLOT A

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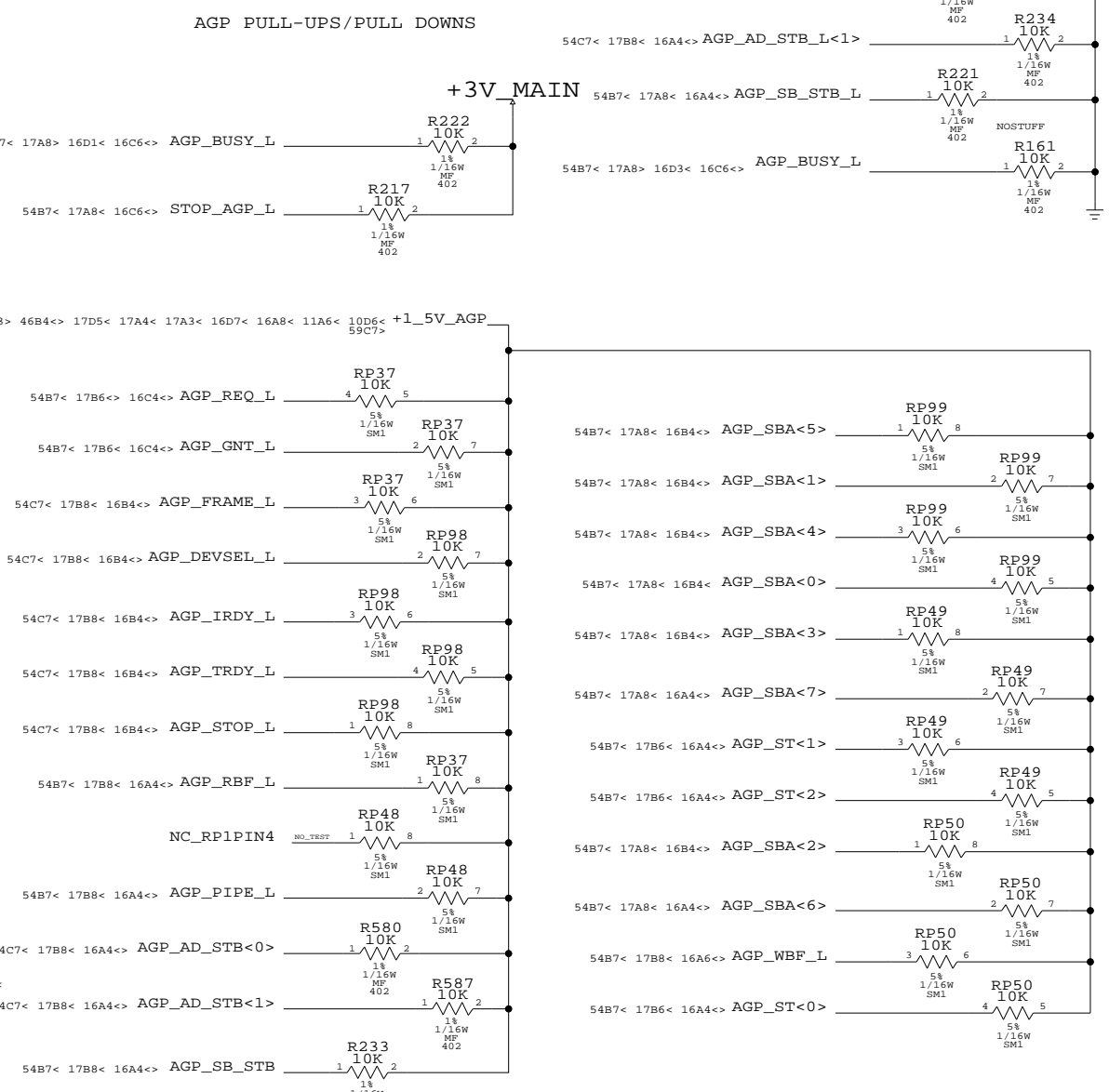
APPLE COMPUTER INC.	DRAWING NUMBER D 051-6569	REV. A
	SCALE NONE	SHEET 14

INTREPID AGP CLK IS 1.5V OUT
NEED 3.3V SWING FOR VIDEO CHIPS
VERSION 1 WORKAROUND IS LA CLOCK
VERSION 2 WORKAROUND IS UNUSED PIN



U25 INTREPID (3 OF 9) (ON PAGE 12)

AGPREQ	AT33	AGP_REQ_L	16C3< 17B6<	54B7<
AGPGNT	AM29	AGP_GNT_L	16C3< 17B6<	54B7<
AGPAD0	AR19	AGP_AD<0>	17D8< 54C7<	
AGPAD1	AM19	AGP_AD<1>	17D8< 54C7<	
AGPAD2	AT20	AGP_AD<2>	17D8< 54C7<	
AGPAD3	AR20	AGP_AD<3>	17D8< 54C7<	
AGPAD4	AT21	AGP_AD<4>	17D8< 54C7<	
AGPAD5	AN20	AGP_AD<5>	17D8< 54C7<	
AGPAD6	AR21	AGP_AD<6>	17D8< 54C7<	
AGPAD7	AN21	AGP_AD<7>	17D8< 54C7<	
AGPAD8	AM21	AGP_AD<8>	17D8< 54C7<	
AGPAD9	AT22	AGP_AD<9>	17D8< 54C7<	
AGPAD10	AR22	AGP_AD<10>	17D8< 54C7<	
AGPAD11	AN22	AGP_AD<11>	17D8< 54C7<	
AGPAD12	AM22	AGP_AD<12>	17D8< 54C7<	
AGPAD13	AT23	AGP_AD<13>	17D8< 54C7<	
AGPAD14	AR23	AGP_AD<14>	17D8< 54C7<	
AGPAD15	AL24	AGP_AD<15>	17C8< 54C7<	
AGPAD16	AM23	AGP_AD<16>	17C8< 54C7<	
AGPAD17	AR24	AGP_AD<17>	17C8< 54C7<	
AGPAD18	AT25	AGP_AD<18>	17C8< 54C7<	
AGPAD19	AM24	AGP_AD<19>	17C8< 54C7<	
AGPAD20	AN24	AGP_AD<20>	17C8< 54C7<	
AGPAD21	AL25	AGP_AD<21>	17C8< 54C7<	
AGPAD22	AT24	AGP_AD<22>	17C8< 54C7<	
AGPAD23	AR26	AGP_AD<23>	17C8< 54C7<	
AGPAD24	AT26	AGP_AD<24>	17C8< 54C7<	
AGPAD25	AM25	AGP_AD<25>	17C8< 54C7<	
AGPAD26	AN26	AGP_AD<26>	17C8< 54C7<	
AGPAD27	AM26	AGP_AD<27>	17C8< 54C7<	
AGPAD28	AR27	AGP_AD<28>	17C8< 54C7<	
AGPAD29	AT27	AGP_AD<29>	17C8< 54C7<	
AGPAD30	AN28	AGP_AD<30>	17C8< 54C7<	
AGPAD31	AL27	AGP_AD<31>	17C8< 54C7<	
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AGPCBE_1	AT23	AGP_CBE<1>	17C8< 54C7<	
AGPCBE_2	AN24	AGP_CBE<2>	17C8< 54C7<	
AGPCBE_3	AL25	AGP_CBE<3>	17C8< 54C7<	
AGPPAR	AT29	AGP_PAR	17B8< 54B7<	
AGPFRAME	AN28	AGP_FRAME_L	16C3< 17B8<	54C7<
AGPTRDY	AR29	AGP_TRDY_L	16B3< 17B8<	54C7<
AGPIRDY	AT28	AGP_IRDY_L	16C3< 17B8<	54C7<
AGPSTOP	AM28	AGP_STOP_L	16B3< 17B8<	54C7<
AGPDEVSEL	AM27	AGP_DEVSEL_L	16C3< 17B8<	54C7<
AGP_SBA0	AT32	AGP_SBA<0>	16C1< 17A8<	54B7<
AGP_SBA1	AR32	AGP_SBA<1>	16C1< 17A8<	54B7<
AGP_SBA2	AM31	AGP_SBA<2>	16B1< 17A8<	54B7<
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AGP_SBA5	AT31	AGP_SBA<5>	16C1< 17A8<	54B7<
AGP_SBA6	AM30	AGP_SBA<6>	16B1< 17A8<	54B7<
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AGP_SB_STB_N	AN25	AGP_SB_STB_L	16D1< 17A8<	54B7<
AGP_ST0	AN29	AGP_ST<0>	16B1< 17B6<	54B7<
AGP_ST1	AT30	AGP_ST<1>	16B1< 17B6<	54B7<
AGP_ST2	AR30	AGP_ST<2>	16B1< 17B6<	54B7<
AGP_AD_STB0_P	AK20	AGP_AD_STB<0>	16B3< 17B8<	54C7<
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AGP_AD_STB1_N	AK22	AGP_AD_STB_L<1>	16D1< 17B8<	54C7<
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AGPRBF	AK24	AGP_RBF_L	16B3< 17B8<	54B7<

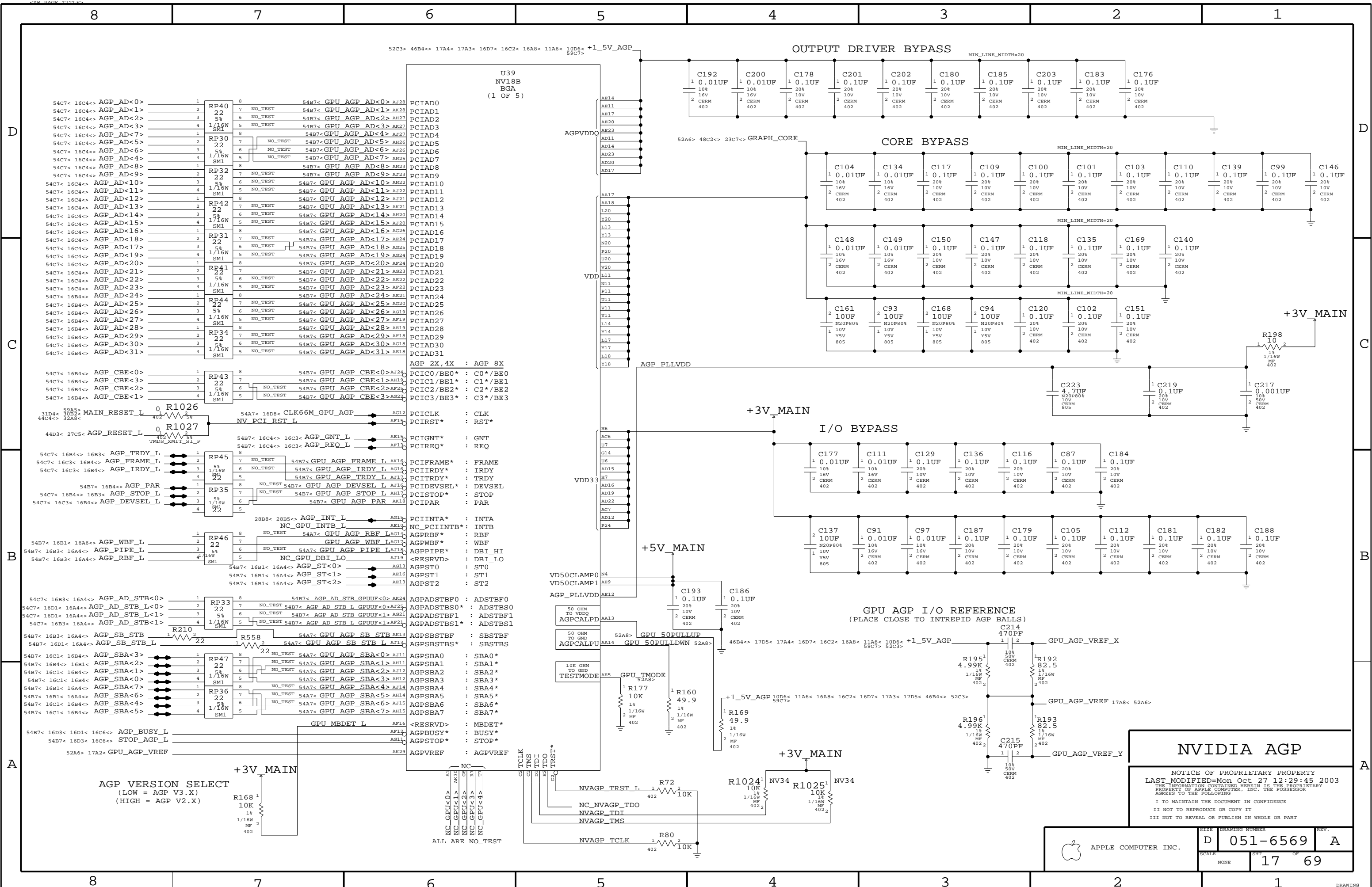


INTREPID AGP

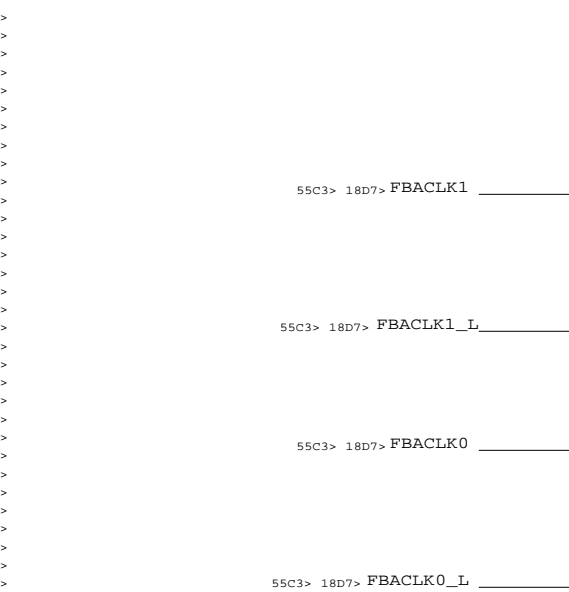
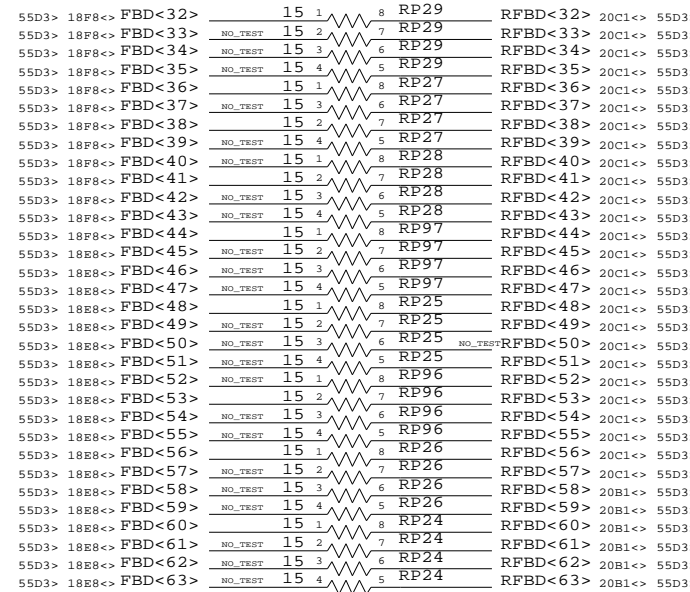
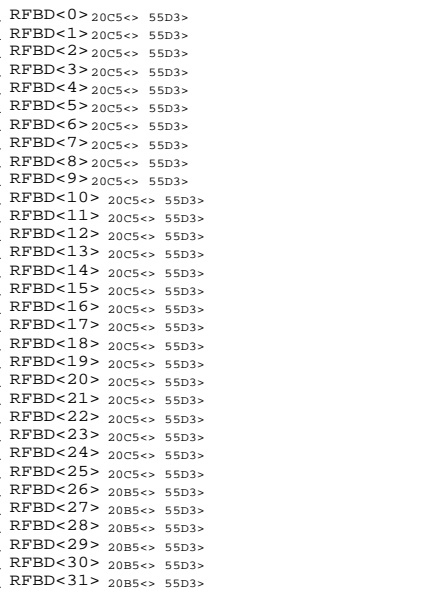
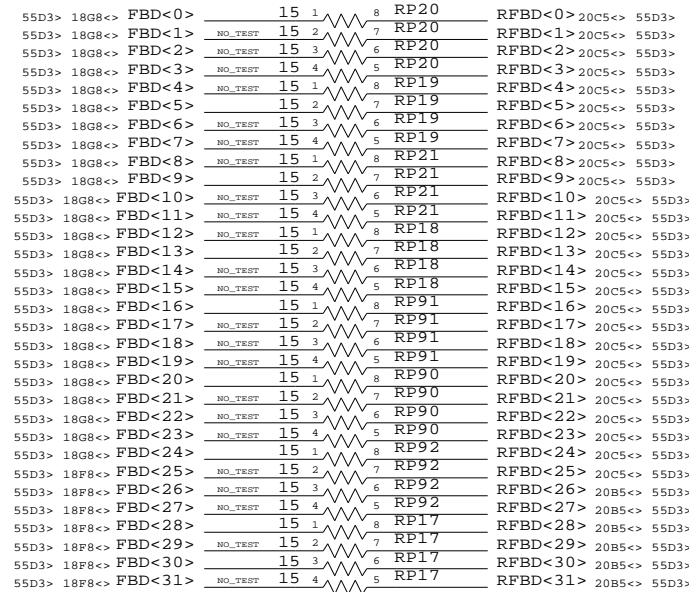
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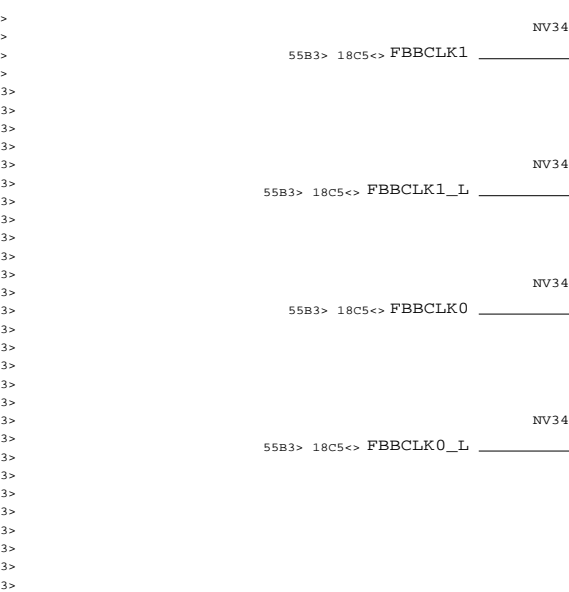
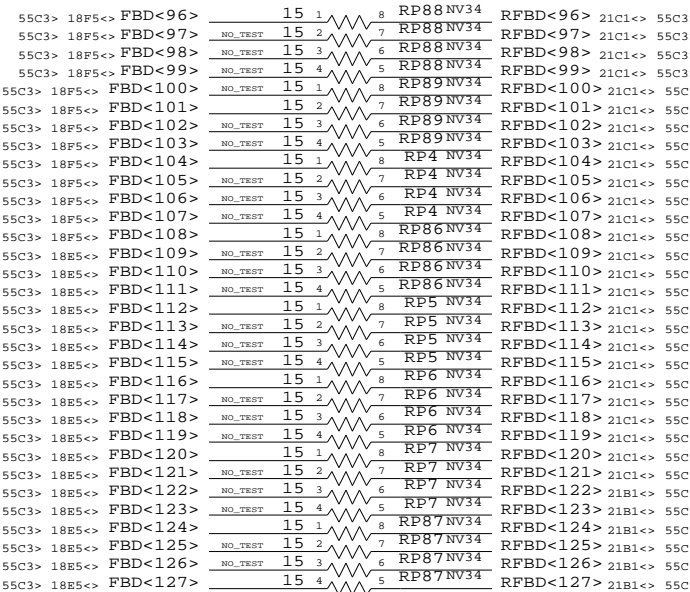
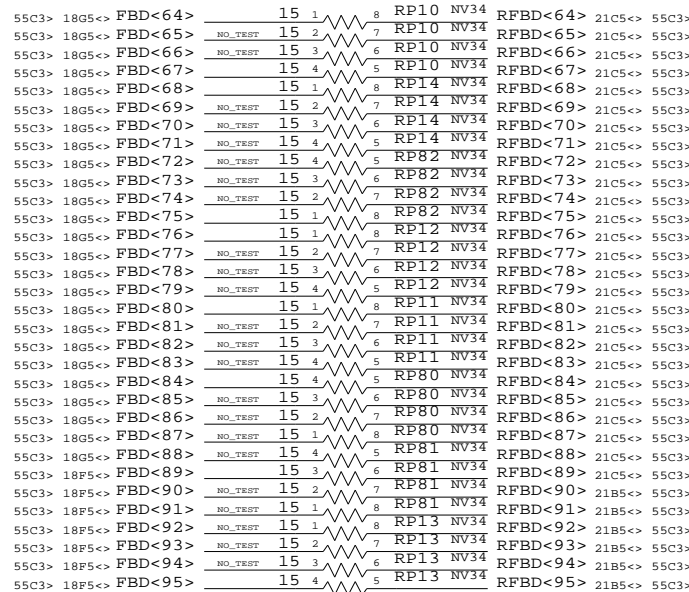
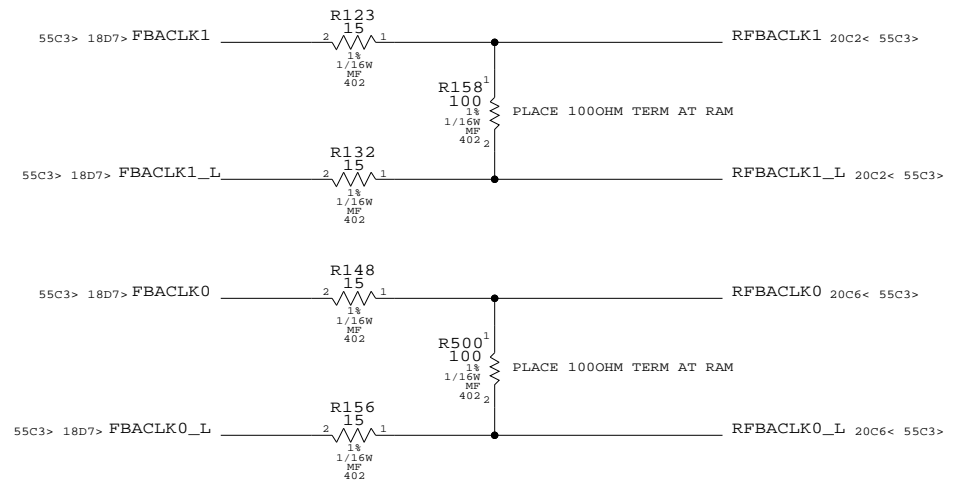
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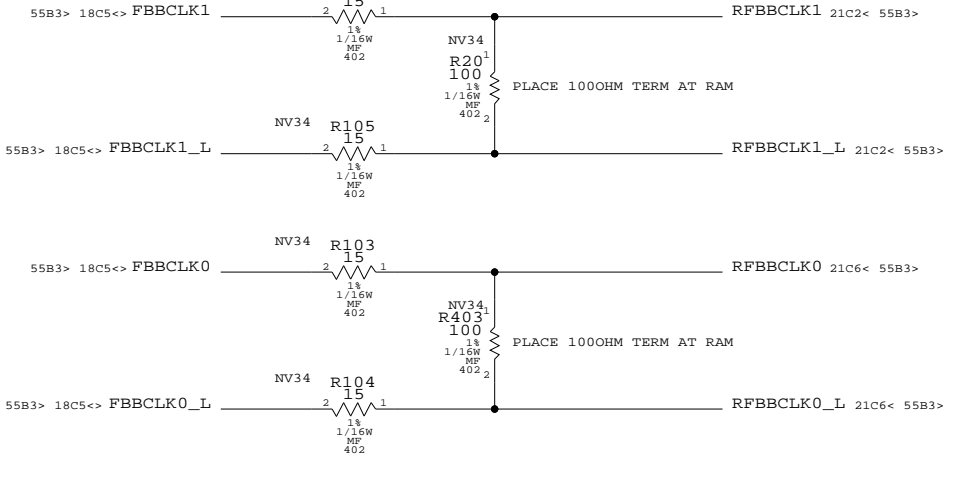
PLACE R'S BETWEEN GPU & MEMORY



PLACE R'S CLOSE TO GPU



PLACE R'S CLOSE TO GPU

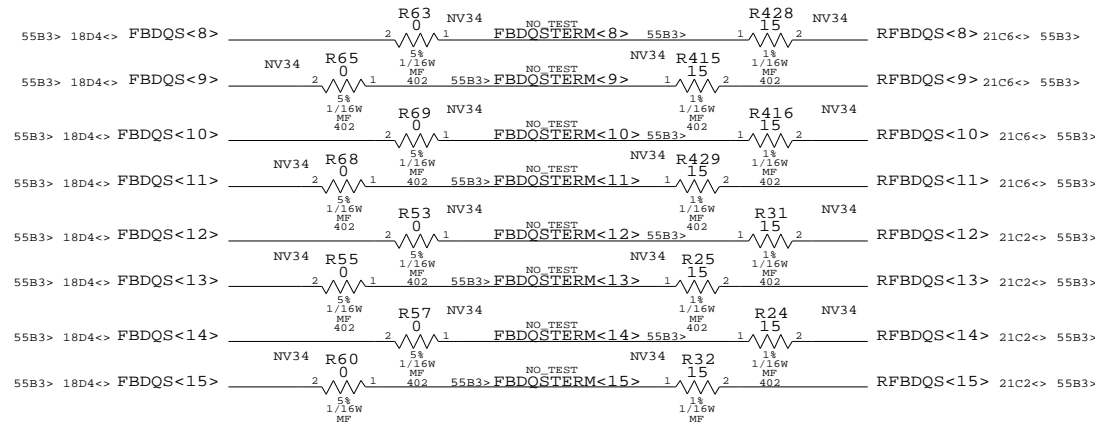
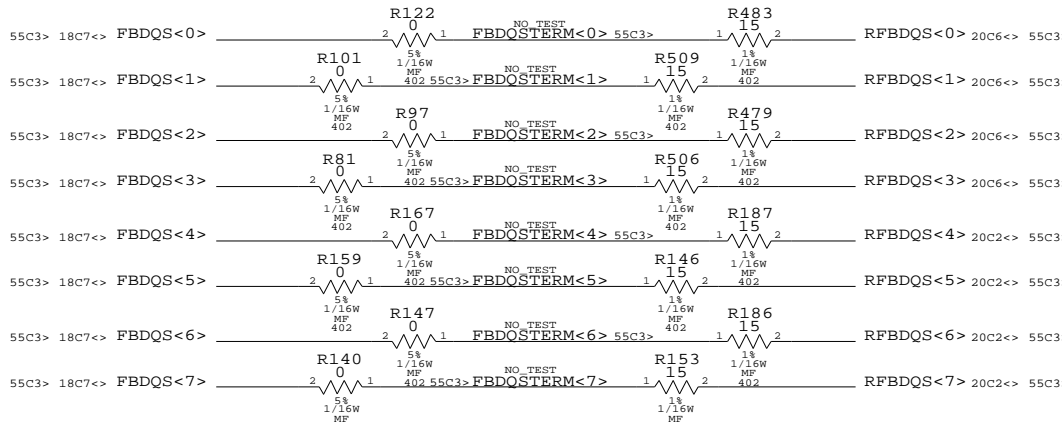


PLACE THESE R CLOSE TO GPU

PLACE THESE R CLOSE TO SGRAM

PLACE THESE R CLOSE TO GPU

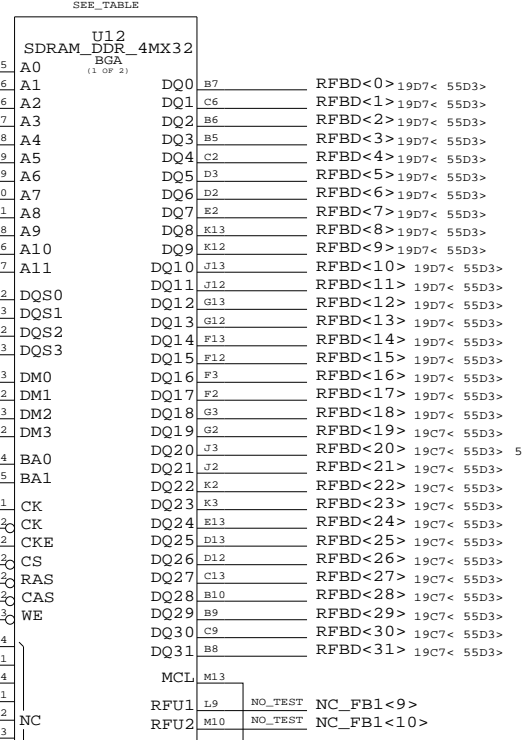
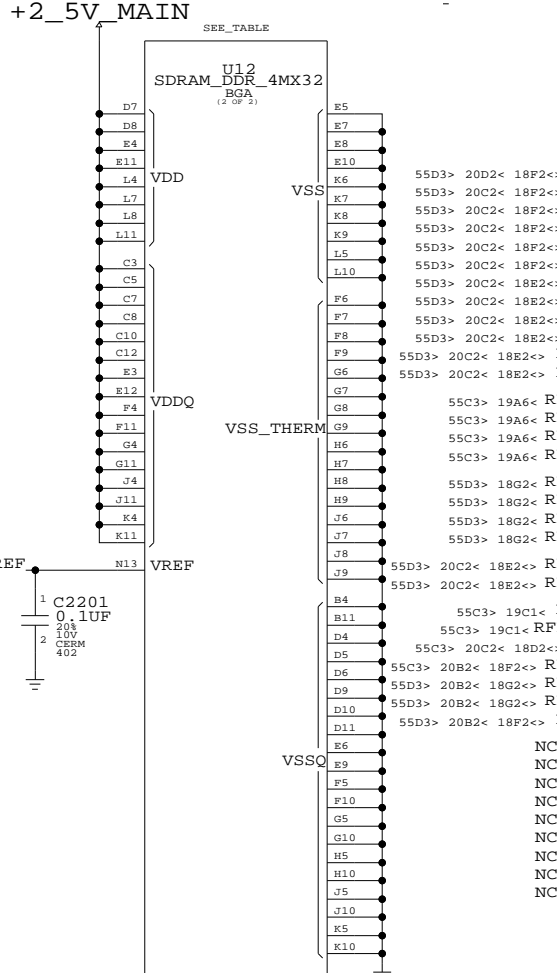
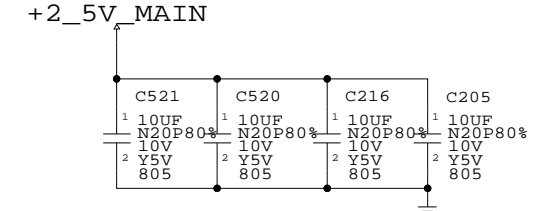
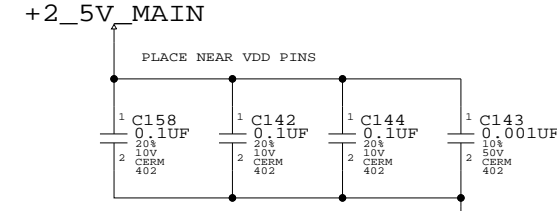
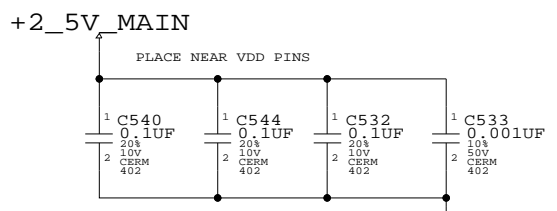
PLACE THESE R CLOSE TO SGRAM



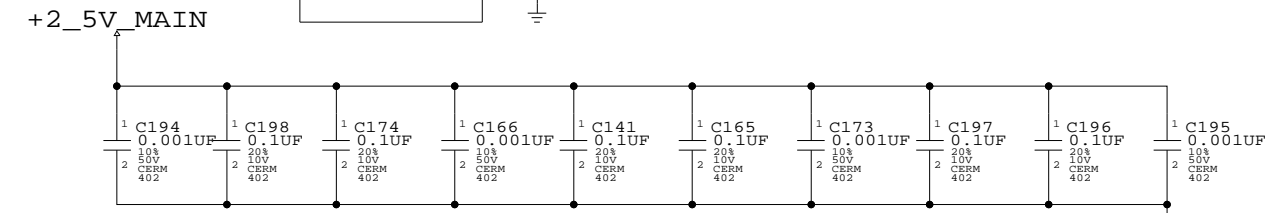
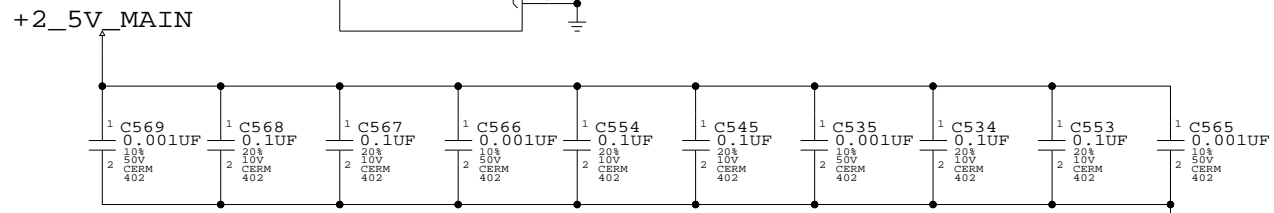
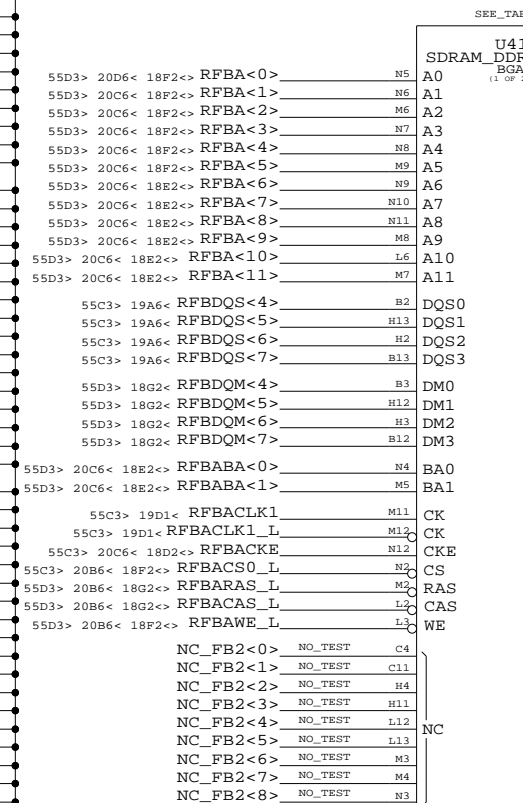
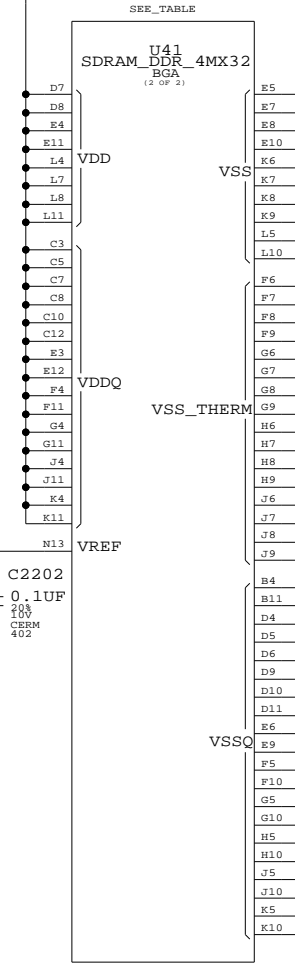
FB TERMINATION

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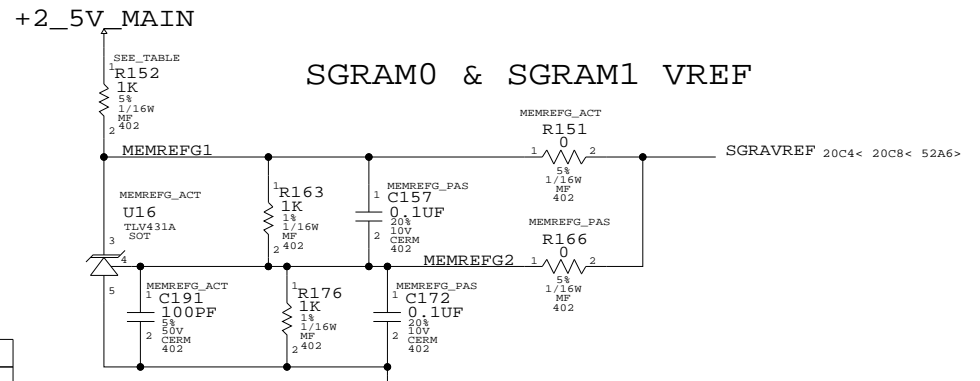


SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM, 4MX32, DDR, 275MHZ	U12, U41	CRITICAL	SAMSUNG_275_32M
333S0250	2	SDRAM, 4MX32, DDR, 275MHZ	U12, U41	CRITICAL	HYNIX_275_32M
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U12, U41	CRITICAL	SAMSUNG_300_32M
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U12, U41	CRITICAL	HYNIX_300_32M

SGRAM0 & SGRAM1 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R152	CRITICAL	MEMREFG_ACT
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R152		MEMREFG_PAS



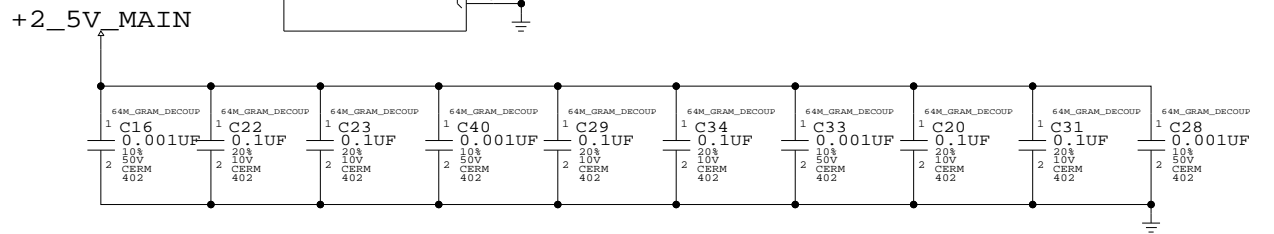
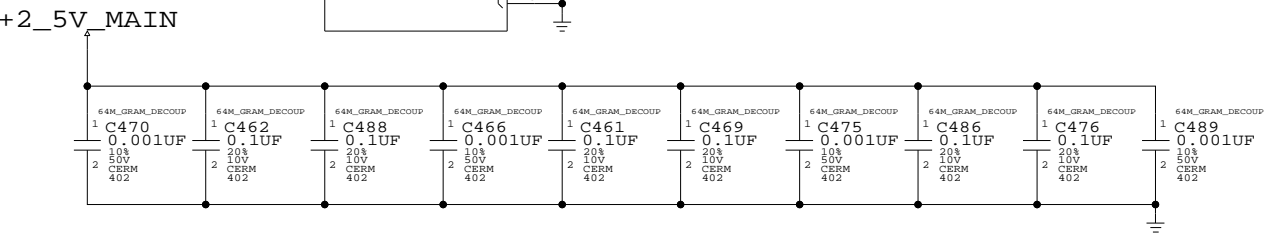
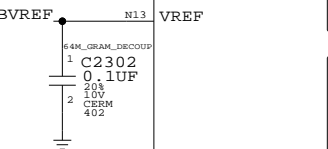
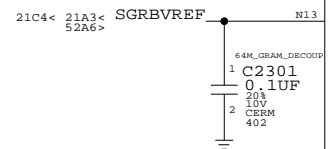
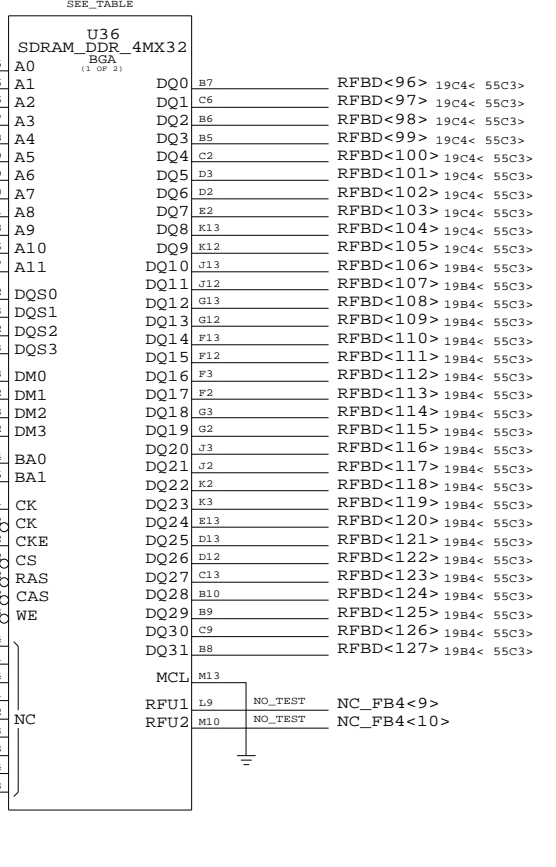
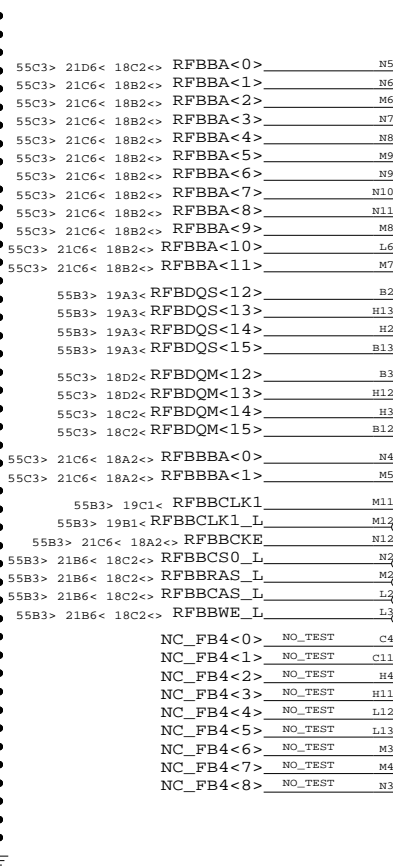
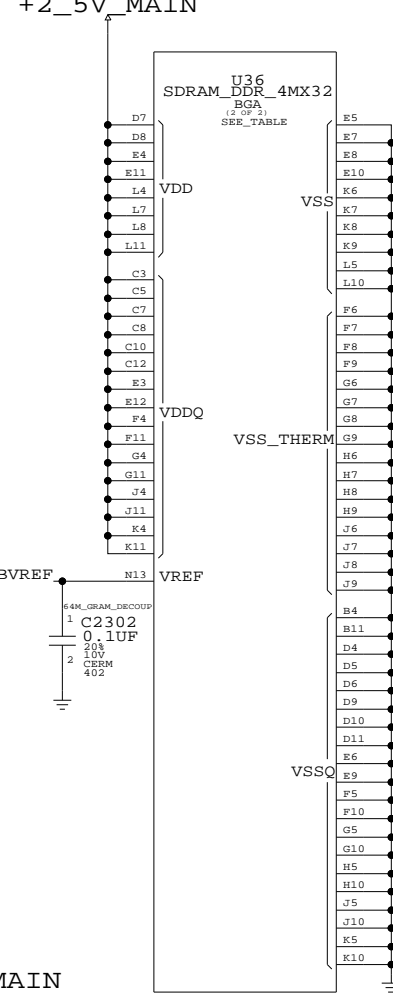
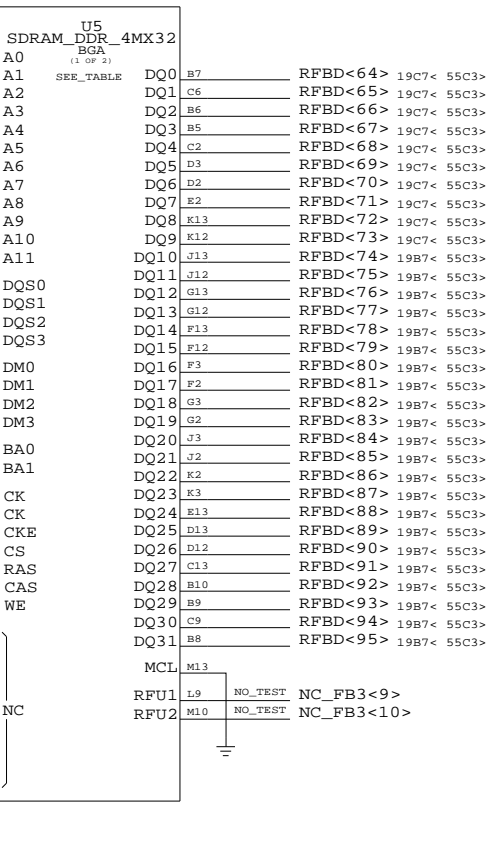
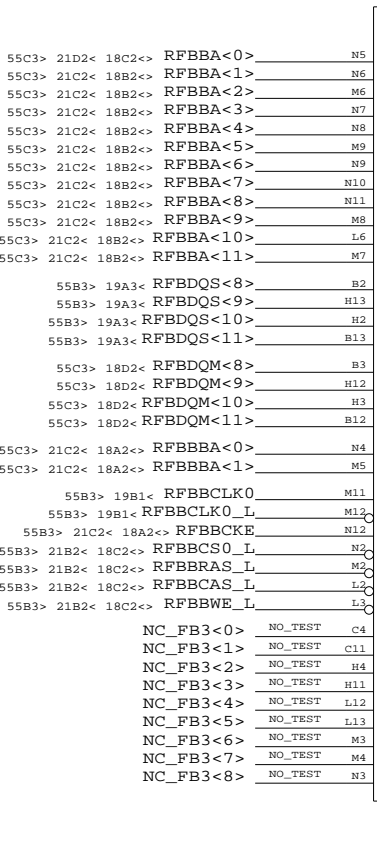
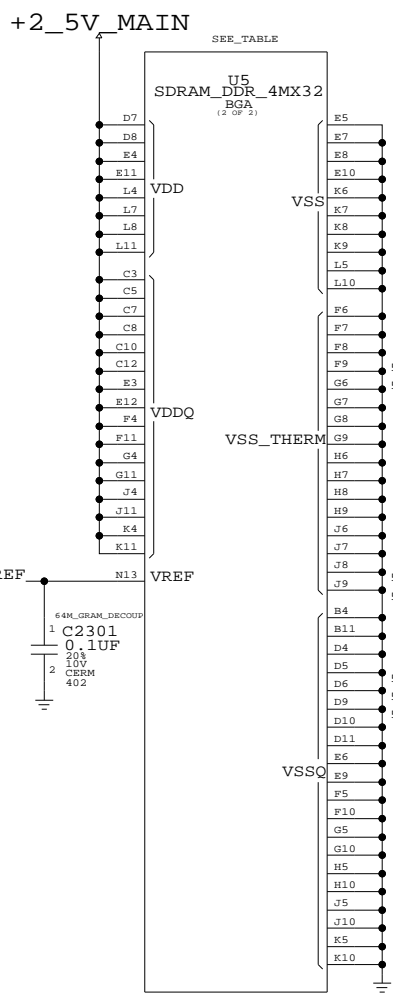
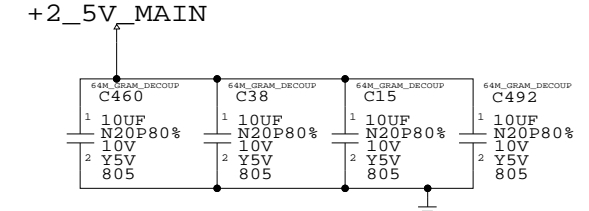
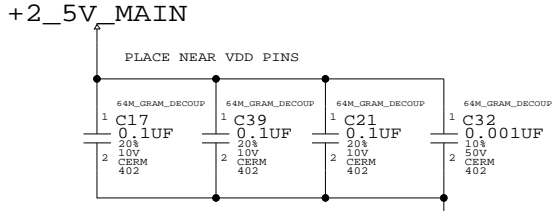
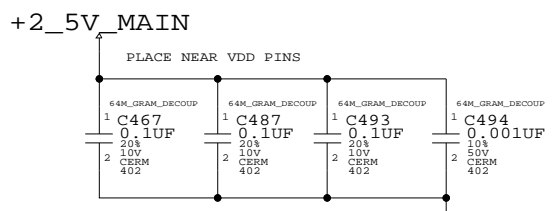
SGRAM0 & SGRAM1

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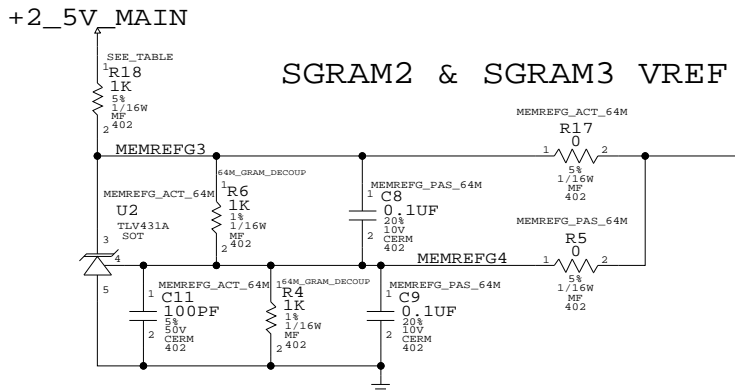


SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0249	2	SDRAM, 4MX32, DDR, 275MHZ	U5,U36	CRITICAL	SAMSUNG_275_64M
333S0250	2	SDRAM, 4MX32, DDR, 275MHZ	U5,U36	CRITICAL	HYNIX_275_64M
333S0251	2	SDRAM, 4MX32, DDR, 300MHZ	U5,U36	CRITICAL	SAMSUNG_300_64M
333S0252	2	SDRAM, 4MX32, DDR, 300MHZ	U5,U36	CRITICAL	HYNIX_300_64M

SGRAM2 & SGRAM3 DDR MEMORY REFERENCE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S1103	1	RES, 1K-OHM, 5%, 1/16W, 0402	R18	CRITICAL	MEMREFG_ACT_64M
116S1000	1	RES, 0-OHM, 5%, 1/16W, 0402	R18		MEMREFG_PAS_64M

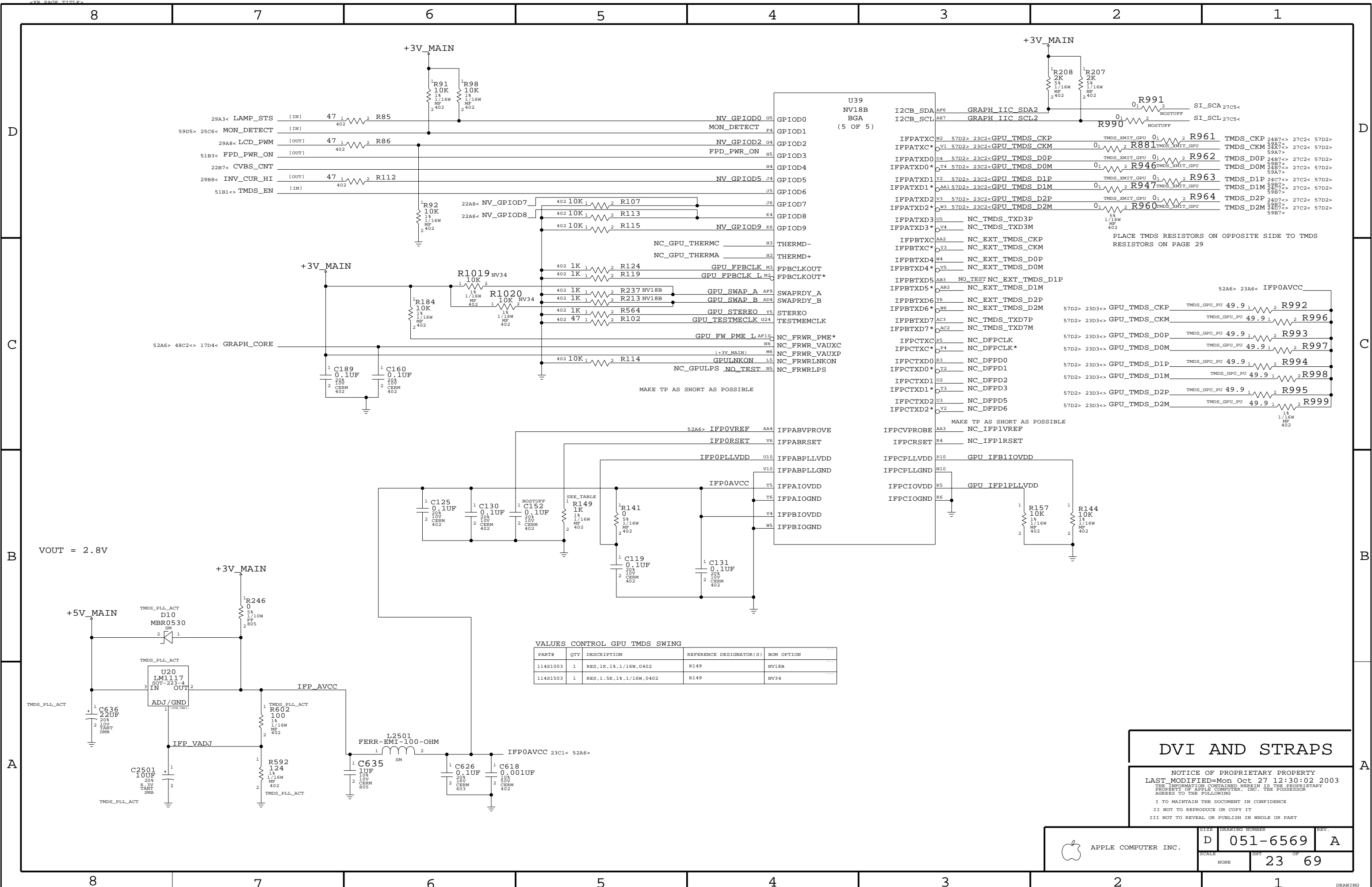


SGRAM2 & SGRAM3

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SCALE	SHT	OF
NONE	21	69



VALUES CONTROL GPU TMS SWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481003	1	RES,1K,1%,1/16W,0402	R149	NV18B
11481503	1	RES,1.5K,1%,1/16W,0402	R149	NV34

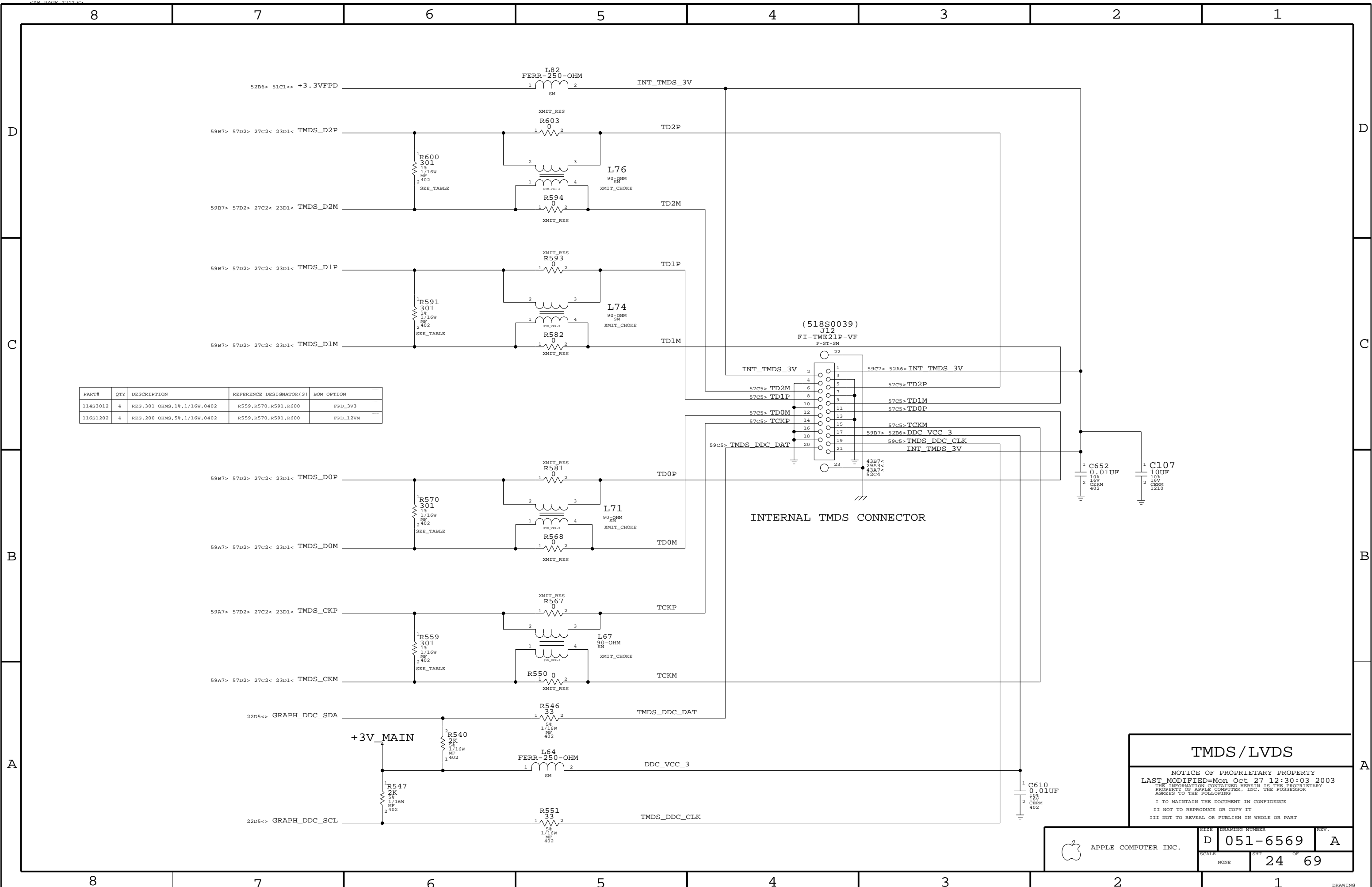
DVI AND STRAPS

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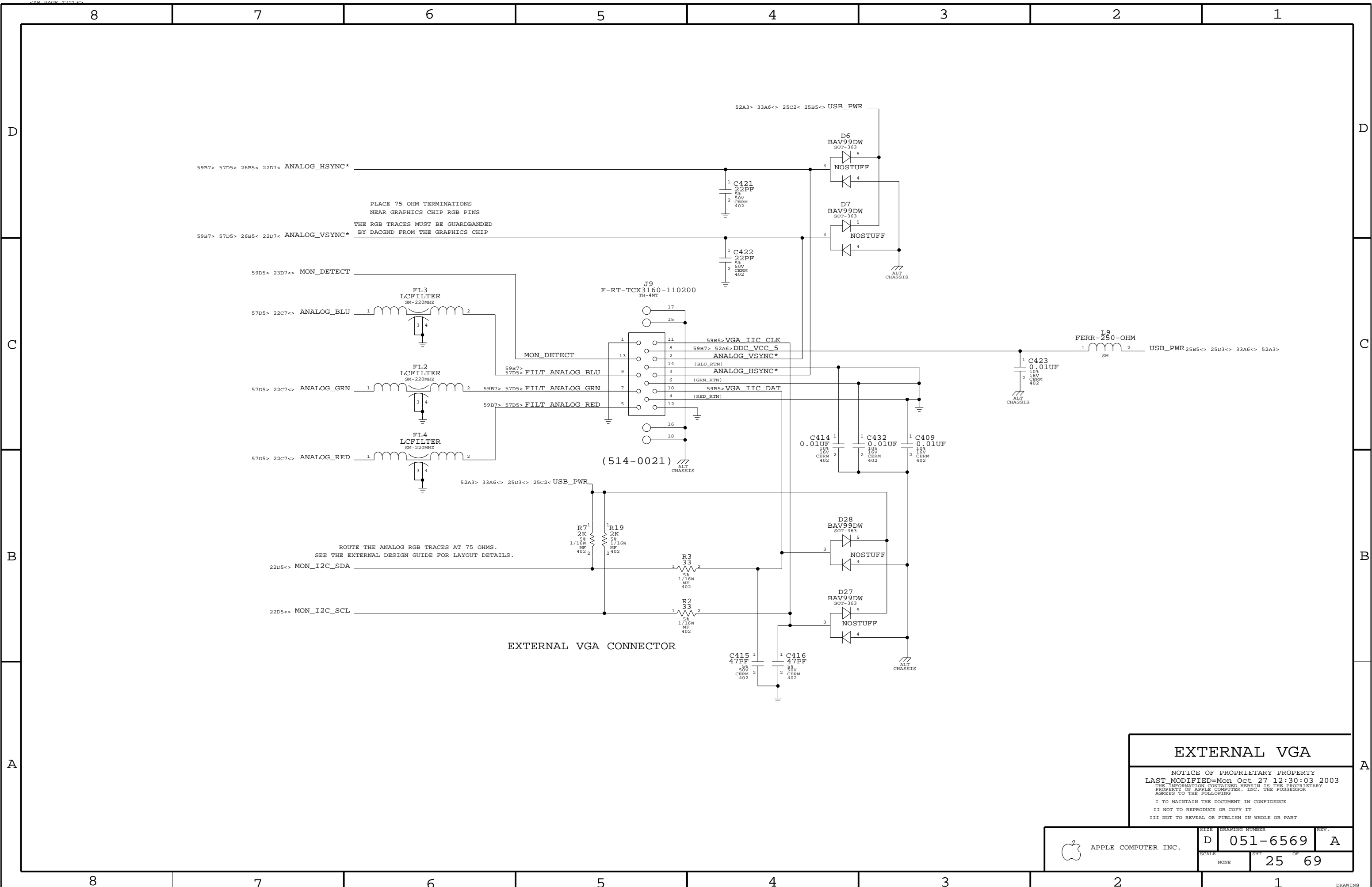


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483012	4	RES,301 OHMS,1%,1/16W,0402	R559,R570,R591,R600	FPD_3V3
11681202	4	RES,200 OHMS,5%,1/16W,0402	R559,R570,R591,R600	FPD_12VM

TMDS/LVDS

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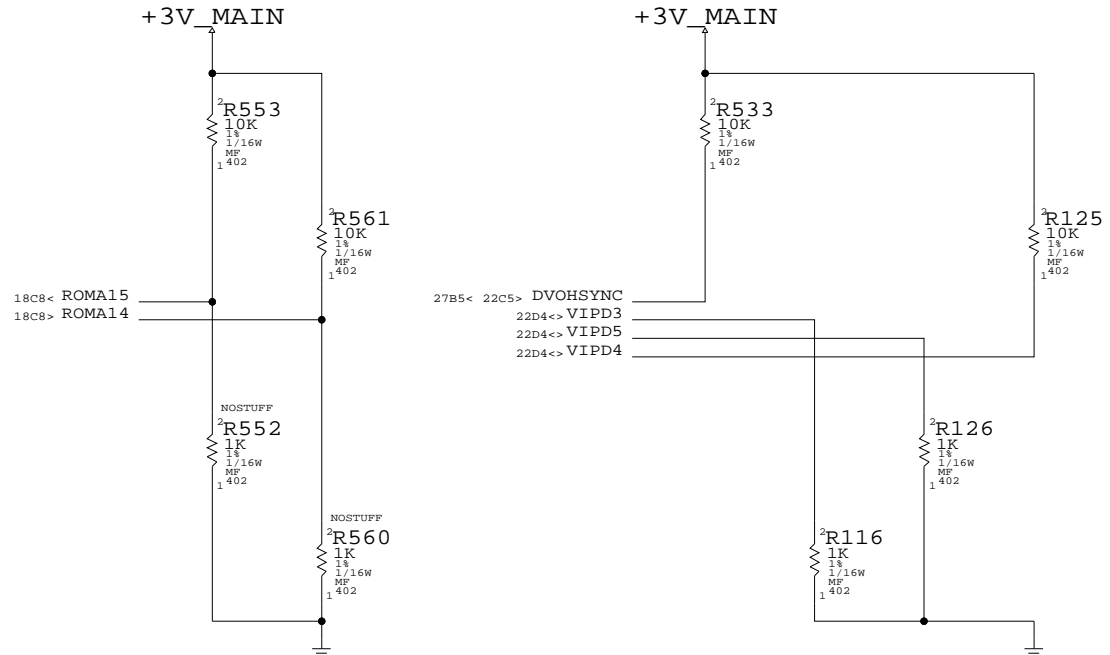


EXTERNAL VGA

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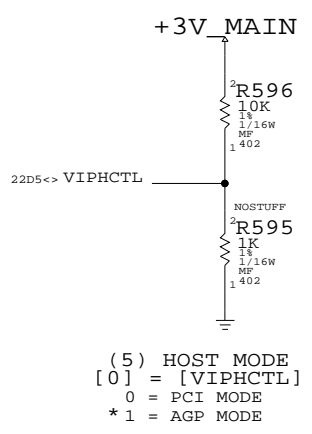
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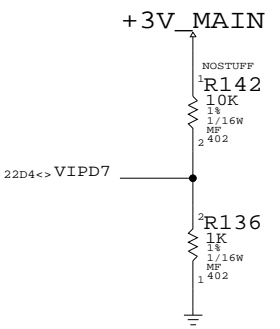


(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
 [1..0] = [ROMA15,ROMA14]
 00 = PARALLEL
 01 = SERIAL AT25F
 10 = SERIAL SST45VF
 * 11 = SERIAL FUTURE

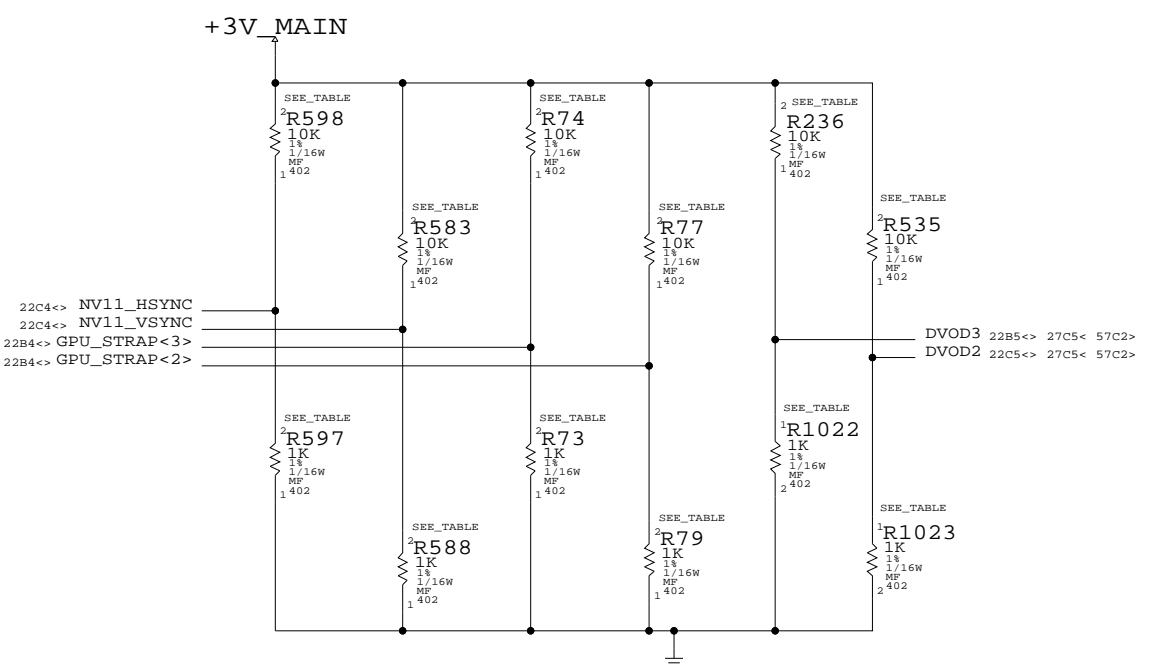
(3) PCI DEVICE ID
 [3..0] = [DVOHSYNC, VIPD3, VIPD5, VIPD4]
 0010 = 0X112 GEFORCE2 GO
 0011 = 0X113 QUADRO2 GO
 0100 = 0X114 NV17M
 0000 = 0X110 GEFORCE2GO MX (NV11B)
 * 1001 = NV18B, NV31, NV34



(5) HOST MODE
 [0] = [VIPHCTL]
 0 = PCI MODE
 * 1 = AGP MODE



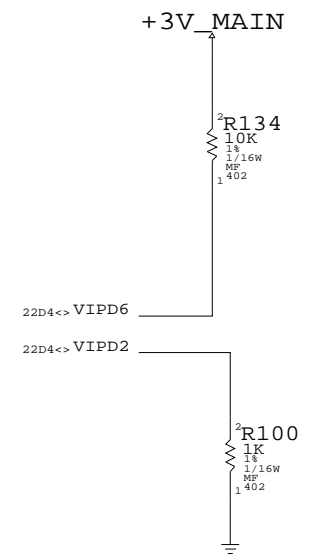
(6) AGP SIDEBAND
 [0] = [VIPD7]
 * 0 = ENABLE AGP SIDEBAND
 1 = DISABLE AGP SIDEBAND



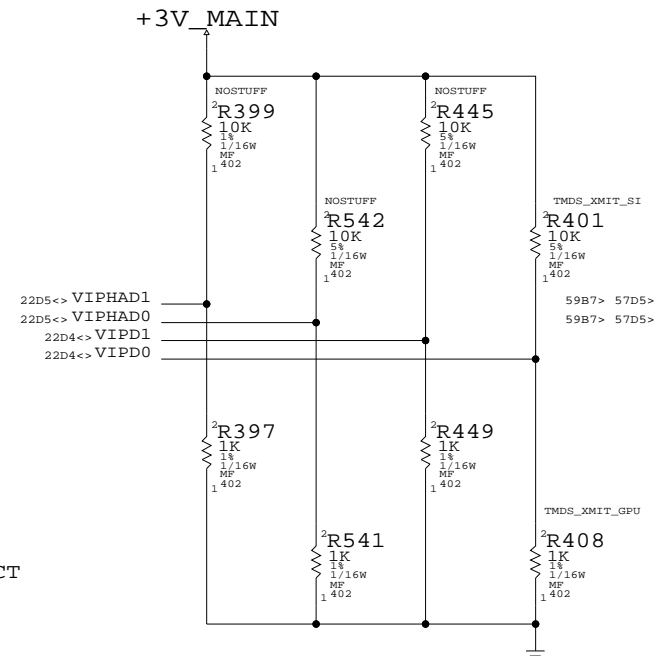
(8) FRAME BUFFER MEMORY TYPE
 [3..0] = [NV11_HSYNC, NV11_VSYNC, GPU_STRAP<3>, GPU_STRAP<2>]
 1111 = 222MHZ
 1101 = 275MHZ SAMSUNG
 1100 = 275MHZ HYNIX

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S1004	5	RES,10KOHM,1%,0402	R598,R583,R77,R236,R535		SAMSUNG_NV18B_270
114S1003	1	RES,1KOHM,1%,0402	R73		SAMSUNG_NV18B_270
114S1004	4	RES,10KOHM,1%,0402	R598,R583,R236,R535		HYNIX_NV18B_270
114S1003	2	RES,1KOHM,1%,0402	R73,R79		HYNIX_NV18B_270

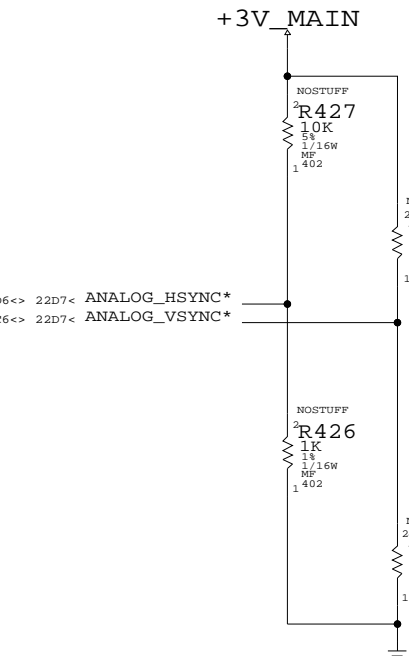
114S1004	5	RES,10KOHM,1%,0402	R598,R583,R535	R74,R77	SAMSUNG_NV34_270
114S1003	1	RES,1KOHM,1%,0402	R1022		SAMSUNG_NV34_270
114S1004	4	RES,10KOHM,1%,0402	R583,R74,R77,R535		HYNIX_NV34_270
114S1003	2	RES,1KOHM,1%,0402	R597,R1022		HYNIX_NV34_270



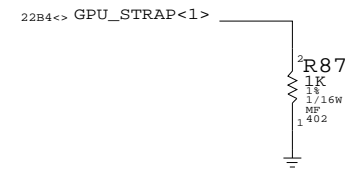
(2) CRYSTAL FREQUENCY SELECT
 [1..0] = [VIPD6, VIPD2]
 00 = 13.5MHZ
 01 = 14.38MHZ
 * 10 = 27MHZ
 11 = {UNDEFINED}



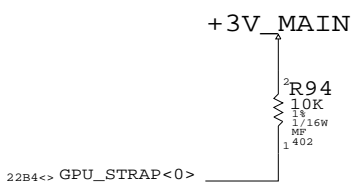
(4) USER DEFINED STRAPS
 [3..0] = [VIPHAD1, VIPHAD0, VIPD1, VIPD0]
 THESE BITS ARE UNDEFINED BUT THEY MUST BE KEPT LOW DURING RESET



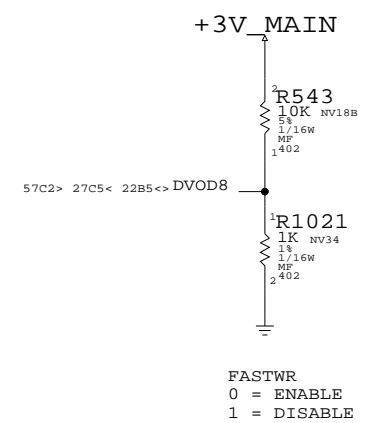
(7) TV MODE
 [1..0] = [ANALOG_HSYNC*, ANALOG_VSYNC*]
 00 = SECAM
 01 = NTSC
 10 = PAL
 * 11 = DISABLED
 (THESE RESISTORS ARE ALL NOSTUFF)



(9) SUB-VENDOR
 [0] = [GPU_STRAP<1>]
 0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
 1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)



(10) PCI ADDRESS BUS
 [0] = [GPU_STRAP<0>]
 0 = REVERSED
 * 1 = NORMAL



FASTWR
 0 = ENABLE
 1 = DISABLE

NVIDIA STRAPS 1

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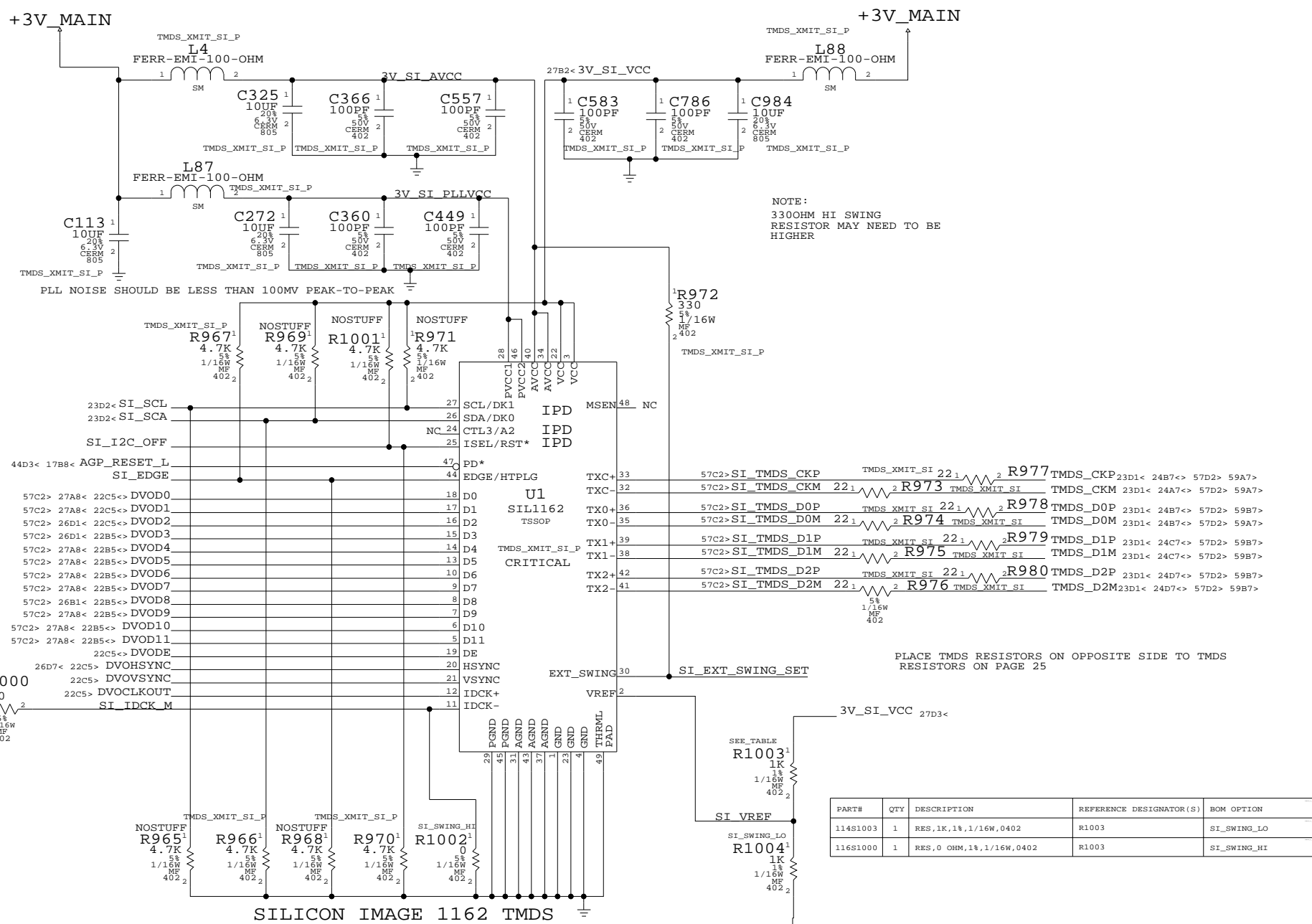
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	D	051-6569	A
SCALE	SHT	OF	
NONE	26	69	

D

C

B

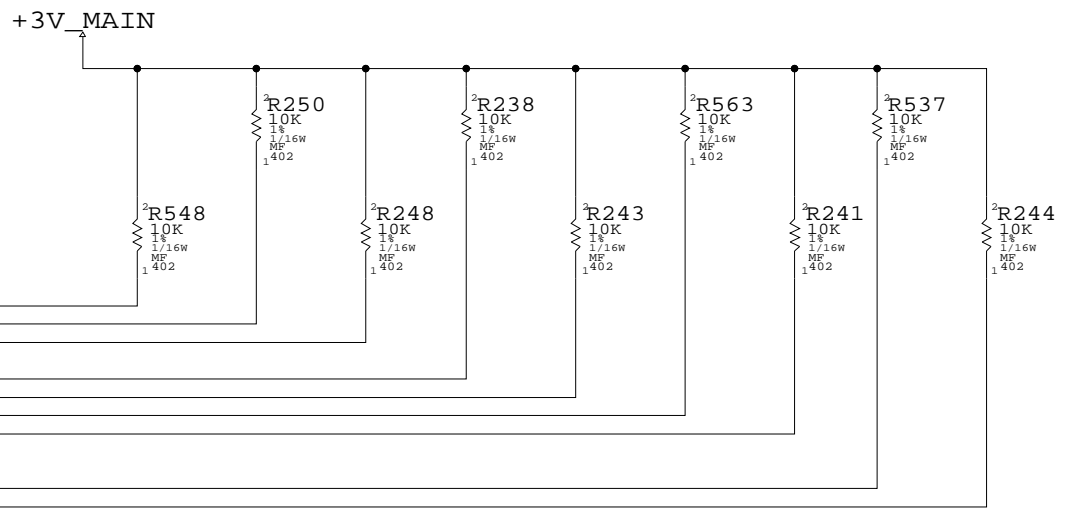
A



NOTE:
330OHM HI SWING
RESISTOR MAY NEED TO BE
HIGHER

PLACE TMD5 RESISTORS ON OPPOSITE SIDE TO TMD5
RESISTORS ON PAGE 25

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11481003	1	RES,1K,1%,1/16W,0402	R1003	SI_SWING_LO
11681000	1	RES,0 OHM,1%,1/16W,0402	R1003	SI_SWING_HI



UNDEFINED RESET CONFIGURATION STRAPS

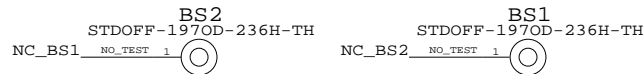
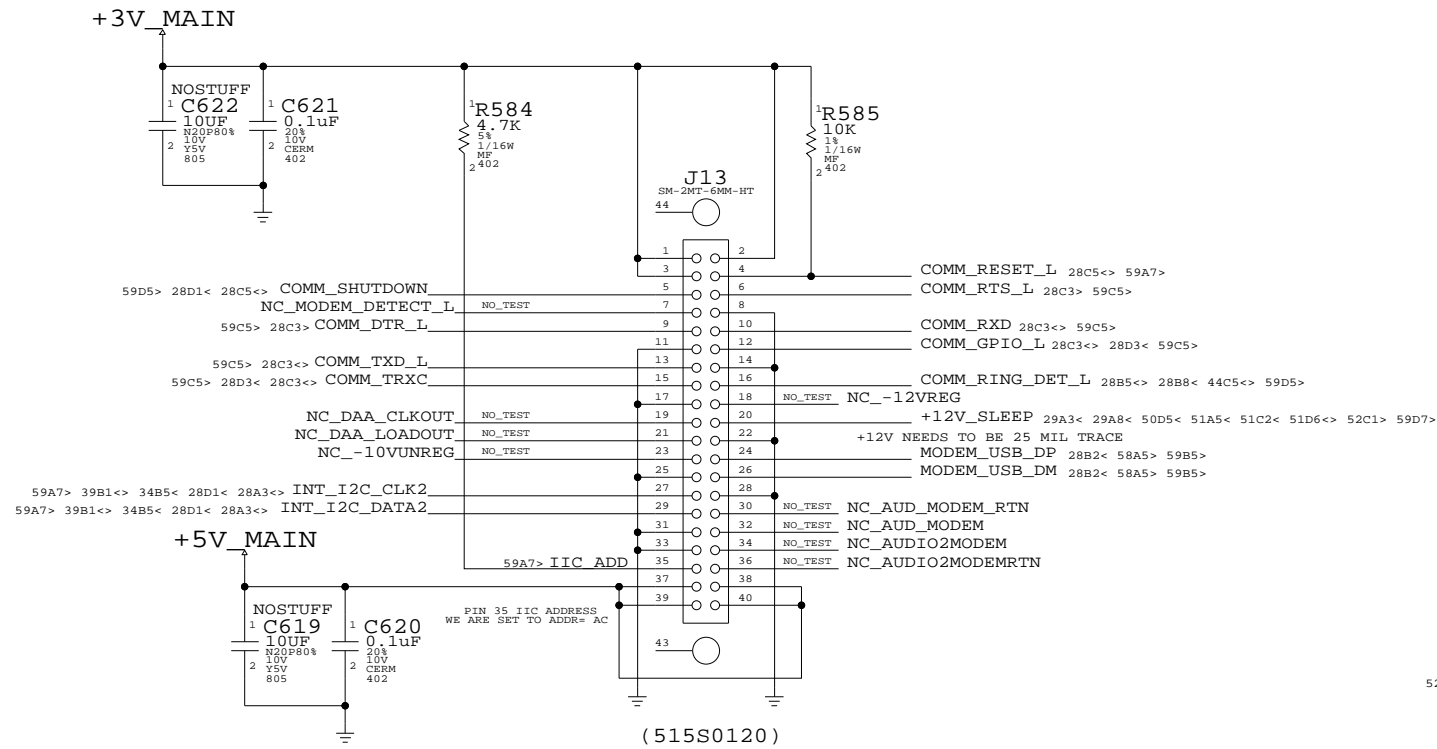
NVIDIA STRAPS 2

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SCALE	SHT		OF
NONE	27		69

MODEM BOARD CONNECTOR

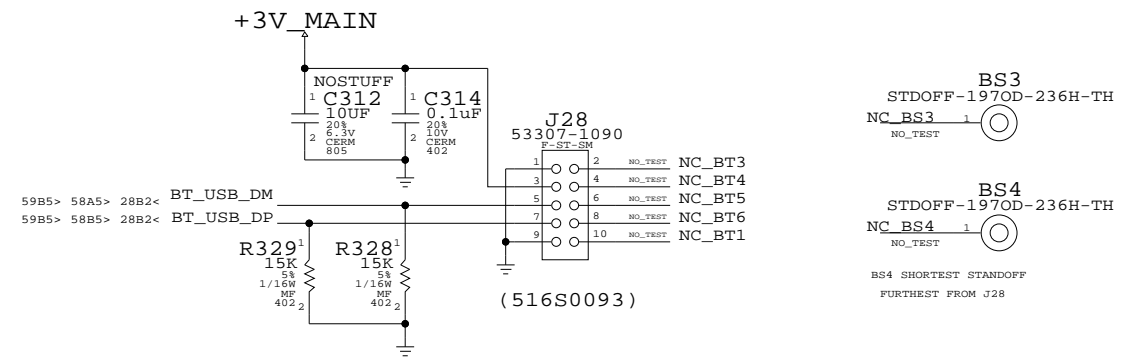
(DASH II)



MODEM STANDOFF SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1034	2	STDOFF-19709-236H-TH	BS1, BS2		

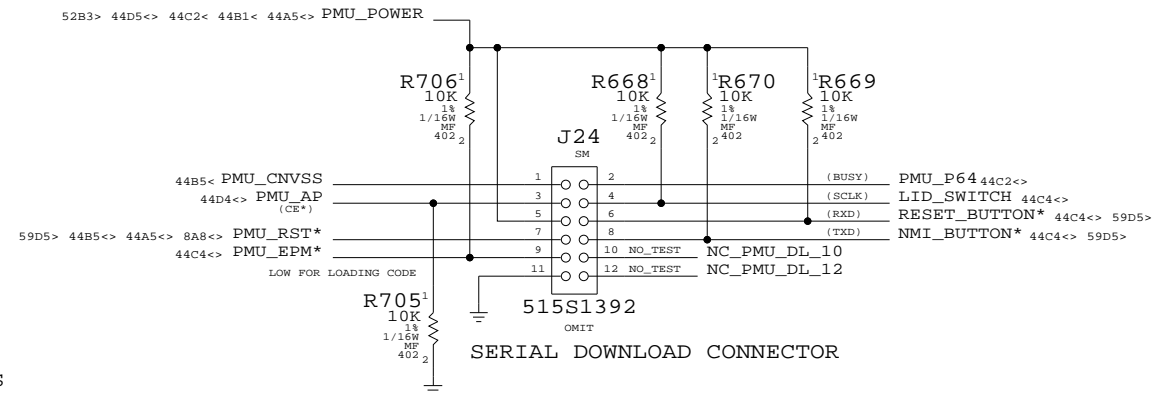
BLUETOOTH CONNECTOR



BLUETOOTH CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-0170	1	STDOFF, BLUETOOTH, SHORT	BS4		
860-0171	1	STDOFF, BLUETOOTH, LONG	BS3		

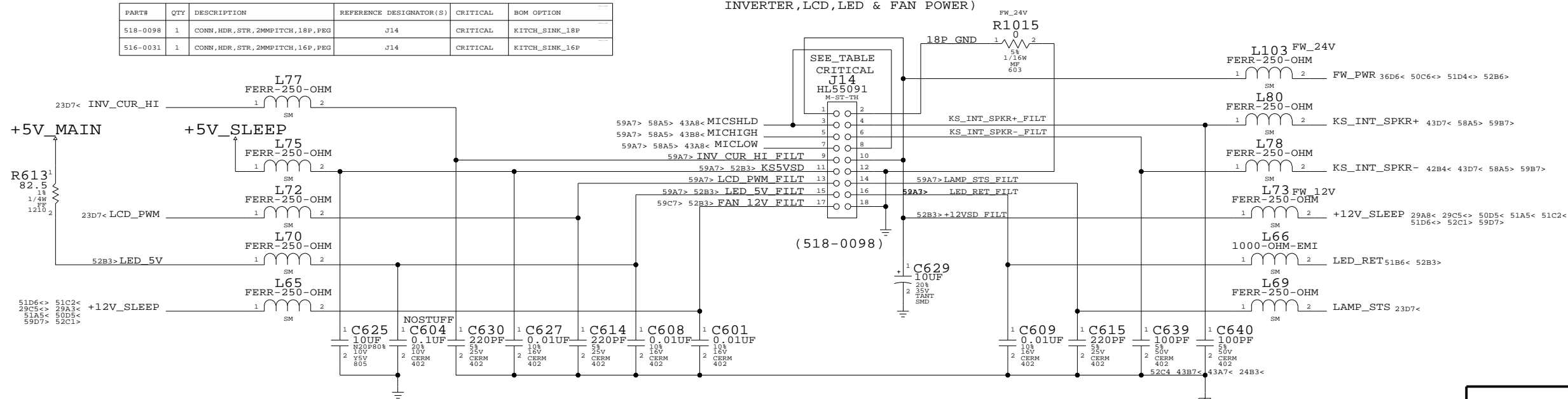
SERIAL DOWNLOAD INTERFACE



SERIAL DOWNLOAD CONNECTOR

'KITCHEN SINK' CONNECTOR
(MICROPHONE, INTERNAL SPEAKER CONNECTIONS
INVERTER, LCD, LED & FAN POWER)

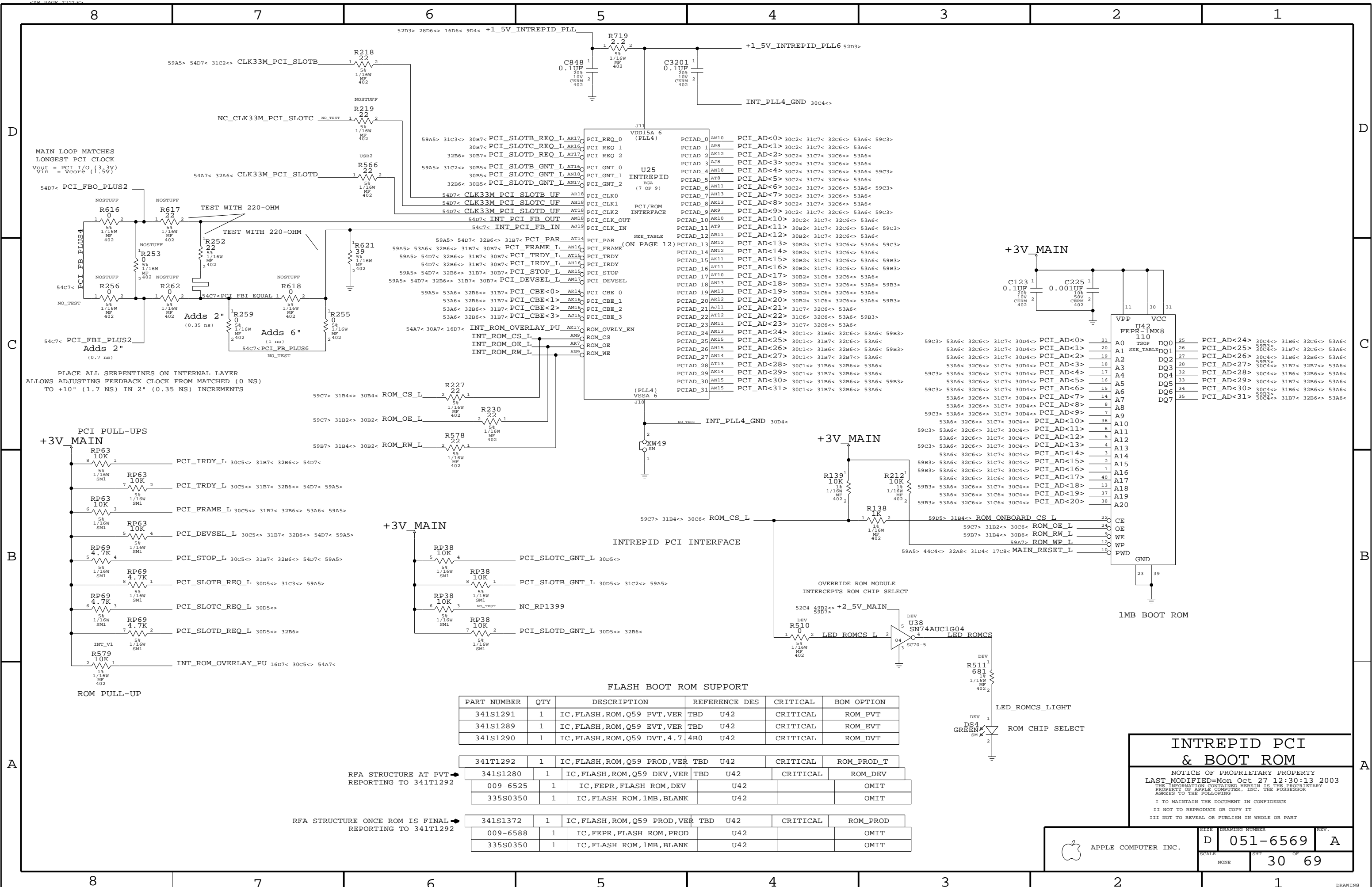
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0098	1	CONN, HDR, STR, 2MMPITCH, 18P, PEG	J14	CRITICAL	KITCH_SINK_18P
516-0031	1	CONN, HDR, STR, 2MMPITCH, 16P, PEG	J14	CRITICAL	KITCH_SINK_16P



MODEM, BLUETOOTH,
KITCHEN SINK
& SERIAL DOWNLOAD

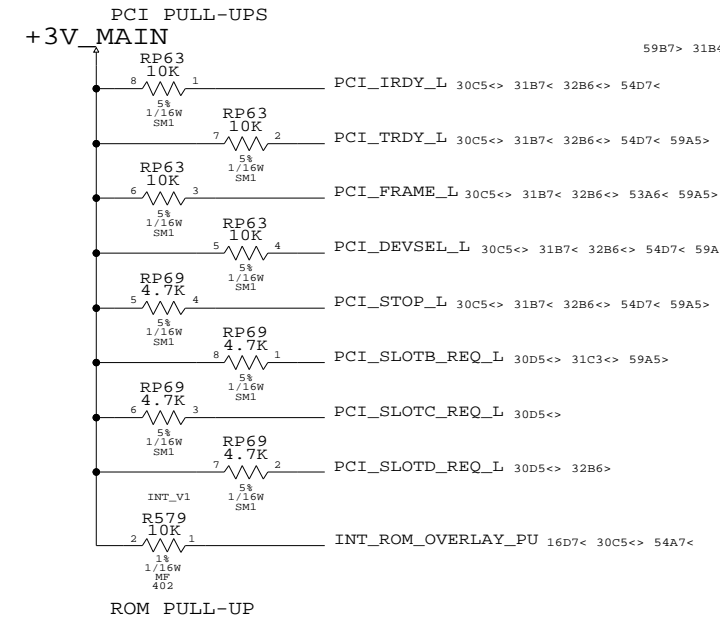
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NONE	29	69	



MAIN LOOP MATCHES
LONGEST PCI CLOCK
V_{out} = PCI I/O (3.3V)
V_{in} = V_{core} (1.5V)

PLACE ALL SERPENTINES ON INTERNAL LAYER
ALLOWS ADJUSTING FEEDBACK CLOCK FROM MATCHED (0 NS)
TO +10" (1.7 NS) IN 2" (0.35 NS) INCREMENTS



FLASH BOOT ROM SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1291	1	IC, FLASH, ROM, Q59 PVT, VER	TBD U42	CRITICAL	ROM_PVT
341S1289	1	IC, FLASH, ROM, Q59 EVT, VER	TBD U42	CRITICAL	ROM_EVT
341S1290	1	IC, FLASH, ROM, Q59 DVT, 4.7	4B0 U42	CRITICAL	ROM_DVT

RFA STRUCTURE AT PVT
REPORTING TO 341T1292

RFA STRUCTURE ONCE ROM IS FINAL
REPORTING TO 341T1292

341T1292	1	IC, FLASH, ROM, Q59 PROD, VER	TBD U42	CRITICAL	ROM_PROD_T
341S1280	1	IC, FLASH, ROM, Q59 DEV, VER	TBD U42	CRITICAL	ROM_DEV
009-6525	1	IC, FEPR, FLASH ROM, DEV	U42		OMIT
335S0350	1	IC, FLASH ROM, 1MB, BLANK	U42		OMIT
341S1372	1	IC, FLASH, ROM, Q59 PROD, VER	TBD U42	CRITICAL	ROM_PROD
009-6588	1	IC, FEPR, FLASH ROM, PROD	U42		OMIT
335S0350	1	IC, FLASH ROM, 1MB, BLANK	U42		OMIT

INTREPID PCI & BOOT ROM

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NONE	30	69	

D

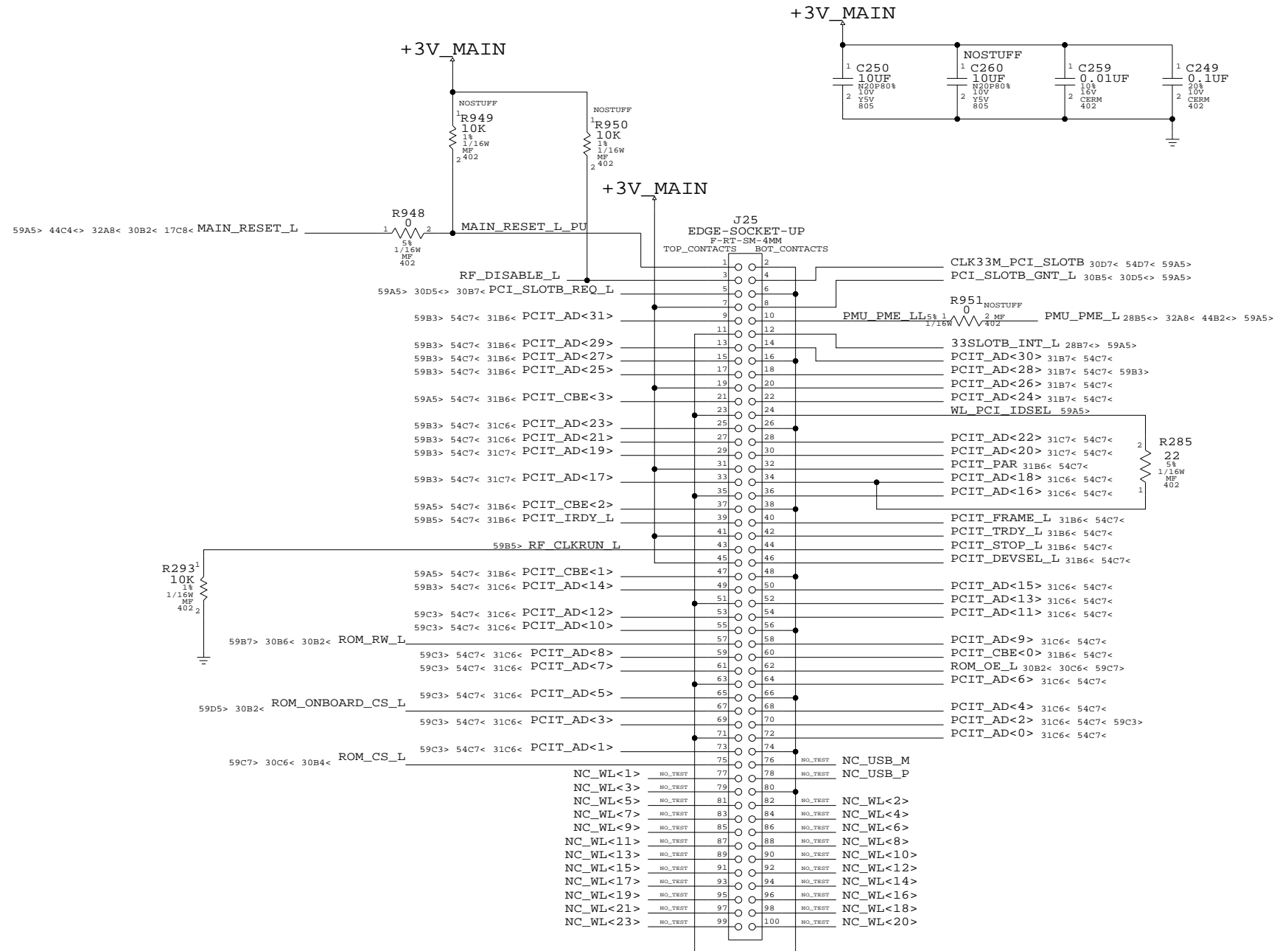
C

B

A

PLACE RP'S NEAR WIRELESS CONNECTOR

59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<0>	1	RP77	8	PCIT_AD<0>	31B2<>	54C7<
53A6< 32C6<> 30D4<> 30C2< PCI_AD<1>	2	RP73	7	NO_TEST	PCIT_AD<1>	31B3<> 54C7< 59C3>
53A6< 32C6<> 30D4<> 30C2< PCI_AD<2>	3	RP75	6	NO_TEST	PCIT_AD<2>	31B2<> 54C7< 59C3>
53A6< 32C6<> 30D4<> 30C2< PCI_AD<3>	4	RP75	5	NO_TEST	PCIT_AD<3>	31B3<> 54C7< 59C3>
59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<4>	1	RP75	8	PCIT_AD<4>	31B2<>	54C7<
53A6< 32C6<> 30D4<> 30C2< PCI_AD<5>	2	RP75	7	NO_TEST	PCIT_AD<5>	31B3<> 54C7< 59C3>
59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<6>	3	RP75	6	NO_TEST	PCIT_AD<6>	31B2<> 54C7<
53A6< 32C6<> 30D4<> 30C2< PCI_AD<7>	4	RP75	5	NO_TEST	PCIT_AD<7>	31B3<> 54C7< 59C3>
53A6< 32C6<> 30D4<> 30C2< PCI_AD<8>	1	RP73	8	PCIT_AD<8>	31B3<>	54C7< 59C3>
59C3> 53A6< 32C6<> 30D4<> 30C2< PCI_AD<9>	2	RP73	7	NO_TEST	PCIT_AD<9>	31B2<> 54C7<
53A6< 32C6<> 30C4<> 30C2< PCI_AD<10>	3	RP73	6	NO_TEST	PCIT_AD<10>	31B3<> 54C7< 59C3>
59C3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<11>	4	RP73	5	NO_TEST	PCIT_AD<11>	31B2<> 54C7<
53A6< 32C6<> 30C4<> 30B2< PCI_AD<12>	1	RP72	8	PCIT_AD<12>	31B3<>	54C7< 59C3>
59C3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<13>	2	RP72	7	NO_TEST	PCIT_AD<13>	31B2<> 54C7<
53A6< 32C6<> 30C4<> 30B2< PCI_AD<14>	3	RP72	6	NO_TEST	PCIT_AD<14>	31C3<> 54C7< 59B3>
59B3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<15>	4	RP72	5	NO_TEST	PCIT_AD<15>	31C2<> 54C7<
59B3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<16>	1	RP59	8	PCIT_AD<16>	31C2<>	54C7<
59B3> 54C7< 31C3<> PCIT_AD<17>	2	RP59	7	NO_TEST	PCIT_AD<17>	30B2< 30C4<> 32C6<> 53A6<
59B3> 53A6< 32C6<> 30C4<> 30B2< PCI_AD<18>	3	RP59	6	NO_TEST	PCIT_AD<18>	31C2<> 54C7<
59B3> 54C7< 31C3<> PCIT_AD<19>	4	RP59	5	NO_TEST	PCIT_AD<19>	30B2< 30C4<> 32C6<> 53A6<
53A6< 32C6<> 30C4<> PCI_AD<23>	1	RP58	8	PCIT_AD<23>	31C3<>	54C7< 59B3>
53A6< 32C6<> 30C4<> PCI_AD<21>	2	RP58	7	NO_TEST	PCIT_AD<21>	31C3<> 54C7< 59B3>
54C7< 31C2<> PCIT_AD<22>	3	RP58	6	NO_TEST	PCIT_AD<22>	30C4<> 32C6<> 53A6< 59B3>
54C7< 31C2<> PCIT_AD<20>	4	RP58	5	NO_TEST	PCIT_AD<20>	30B2< 30C4<> 32C6<> 53A6< 59B3>
53A6< 32B7<> 30C4<> 30C1<> PCI_AD<27>	1	RP56	8	PCIT_AD<27>	31C3<>	54C7< 59B3>
53A6< 32C6<> 30C4<> 30C1<> PCI_AD<25>	2	RP56	7	NO_TEST	PCIT_AD<25>	31C3<> 54C7< 59B3>
54C7< 31C2<> PCIT_AD<26>	3	RP56	6	NO_TEST	PCIT_AD<26>	30C1<> 30C4<> 32B6<> 53A6< 59B3>
54C7< 31C2<> PCIT_AD<24>	4	RP56	5	NO_TEST	PCIT_AD<24>	30C1<> 30C4<> 32C6<> 53A6< 59B3>
59B3> 54C7< 31C2<> PCIT_AD<28>	1	RP54	8	PCIT_AD<28>	30C1<>	30C4<> 32B6<> 53A6<
54C7< 31C2<> PCIT_AD<30>	2	RP54	7	NO_TEST	PCIT_AD<30>	30C1<> 30C4<> 32B6<> 53A6< 59B3>
53A6< 32B6<> 30C4<> 30C1<> PCI_AD<31>	3	RP61	6	NO_TEST	PCIT_AD<31>	31C3<> 54C7< 59B3>
53A6< 32B6<> 30C4<> 30C1<> PCI_AD<29>	4	RP61	5	NO_TEST	PCIT_AD<29>	31C3<> 54C7< 59B3>
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_FRAME_L	1	RP61	8	PCIT_PAR	31C2<>	54C7<
59A5> 53A6< 32B6<> 30C5<> 30B7< PCI_TRDY_L	2	RP61	7	NO_TEST	PCIT_FRAME_L	31C2<> 54C7<
54D7< 32B6<> 30C5<> 30B7< PCI_IRDY_L	3	RP61	6	NO_TEST	PCIT_TRDY_L	31C2<> 54C7<
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_STOP_L	4	RP61	5	NO_TEST	PCIT_IRDY_L	31C3<> 54C7< 59B5>
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_DEVSEL_L	1	RP67	8	PCIT_STOP_L	31C2<>	54C7<
59A5> 54D7< 32B6<> 30C5<> 30B7< PCI_CBE<1>	2	RP67	7	NO_TEST	PCIT_DEVSEL_L	31C2<> 54C7<
53A6< 32B6<> 30C5<> PCI_CBE<1>	3	RP67	6	NO_TEST	PCIT_CBE<1>	31C3<> 54C7< 59A5>
59A5> 53A6< 32B6<> 30C5<> PCI_CBE<0>	4	RP67	5	NO_TEST	PCIT_CBE<0>	31B2<> 54C7<
53A6< 32B6<> 30C5<> PCI_CBE<2>	1	RP64	8	PCIT_CBE<2>	31C3<>	54C7< 59A5>
53A6< 32B6<> 30C5<> PCI_CBE<3>	2	RP64	7	NO_TEST	PCIT_CBE<3>	31C3<> 54C7< 59A5>
NC_PCIR0	NO_TEST	3	5	NO_TEST	NC_PCITR0	
NC_PCIR1	NO_TEST	4	5	NO_TEST	NC_PCITR1	



(516S0046)

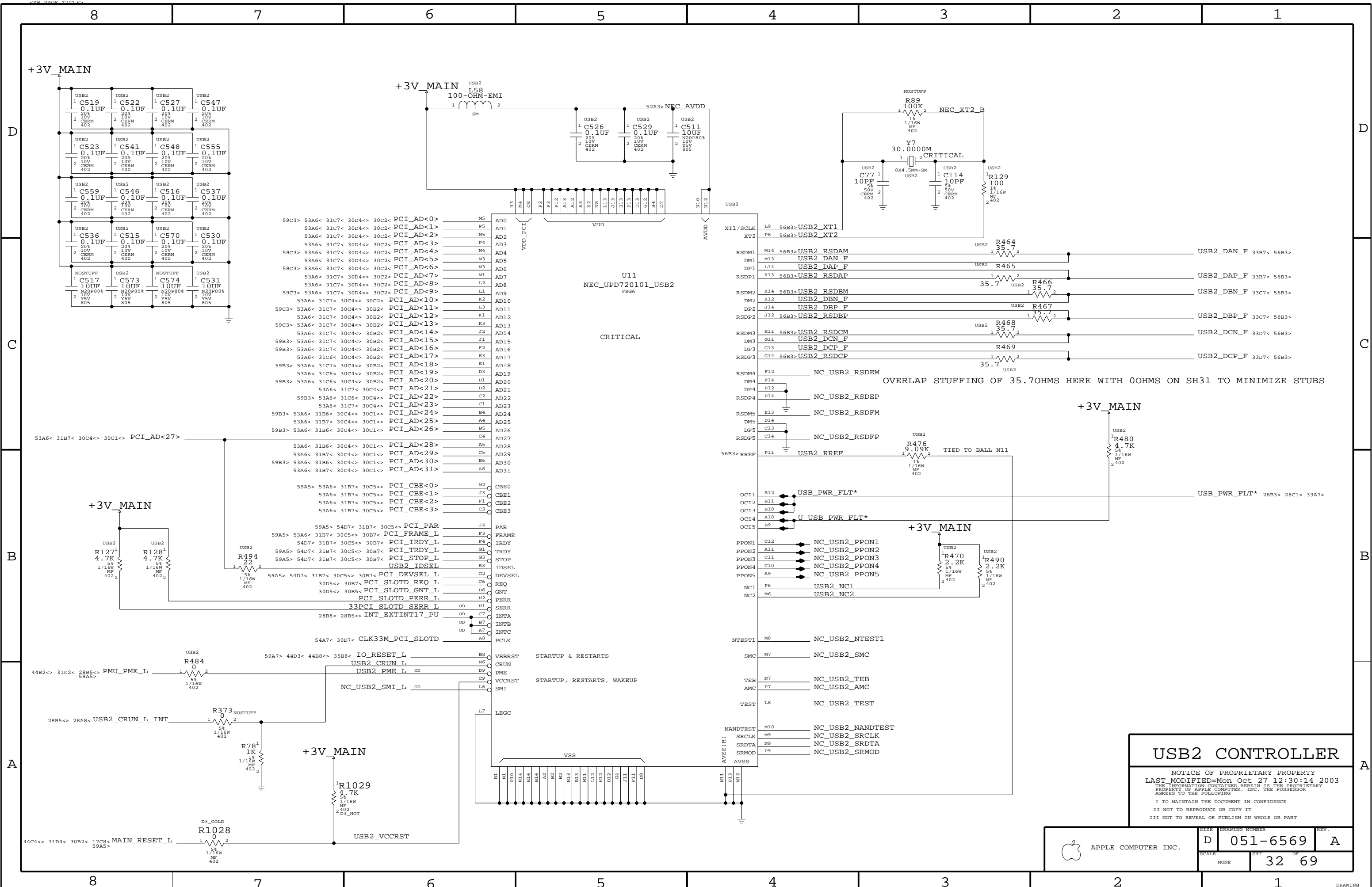
WIRELESS CARD MOUNTING HARDWARE SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
815-7245	1	WIRELESS CARD GUIDE, J25	J251		
452-0411	2	NUT, HEX, M2 X 1.5H, J25	J252, J253		
452-0412	2	SCREW, M2 X 0.4 X 6.0 L, J25	J254, J255		

WIRELESS PCI

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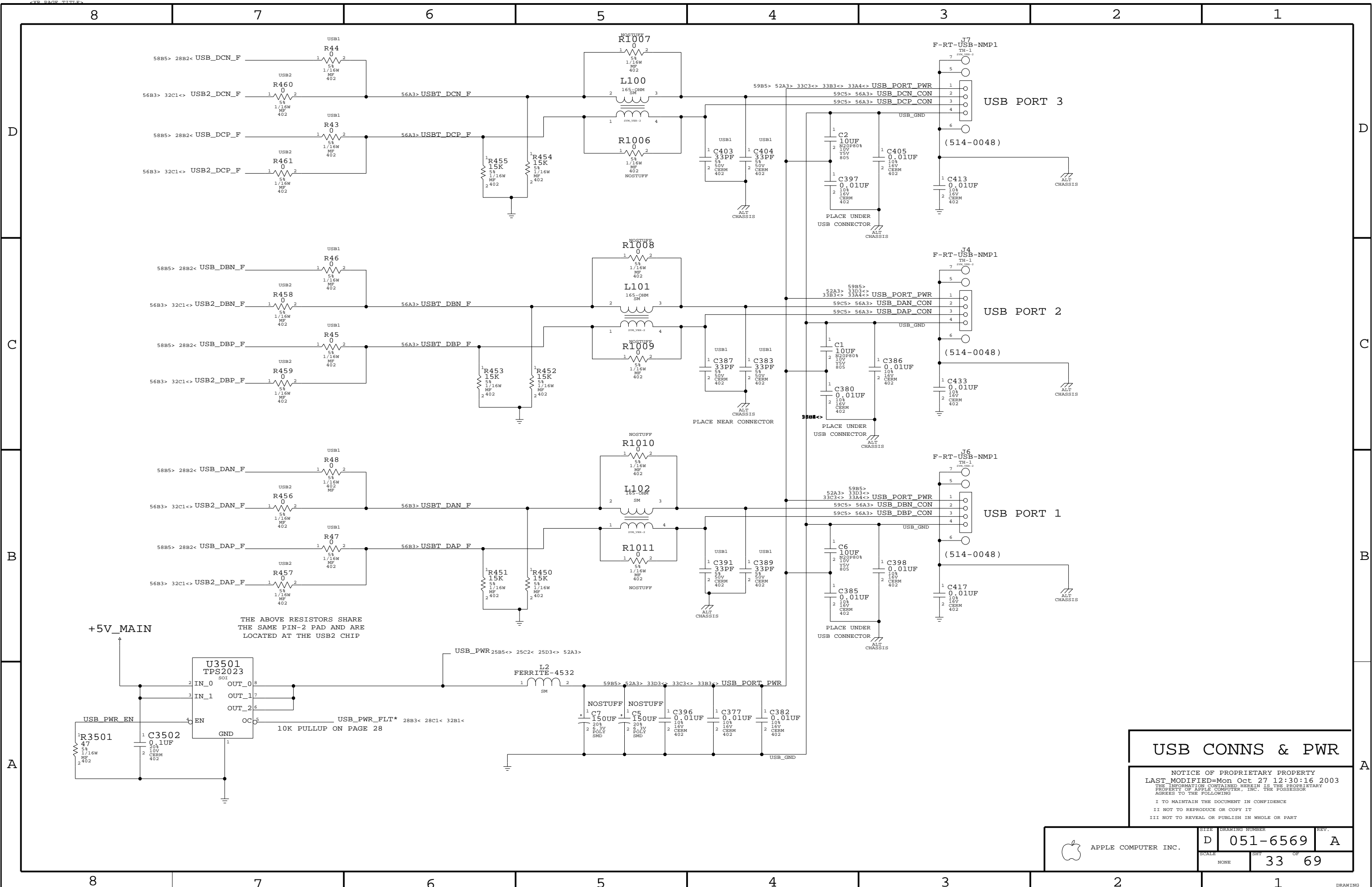
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SCALE		SHT	OF
NONE		31	69



USB2 CONTROLLER

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	SCALE: NONE SHEET: 32 OF 69



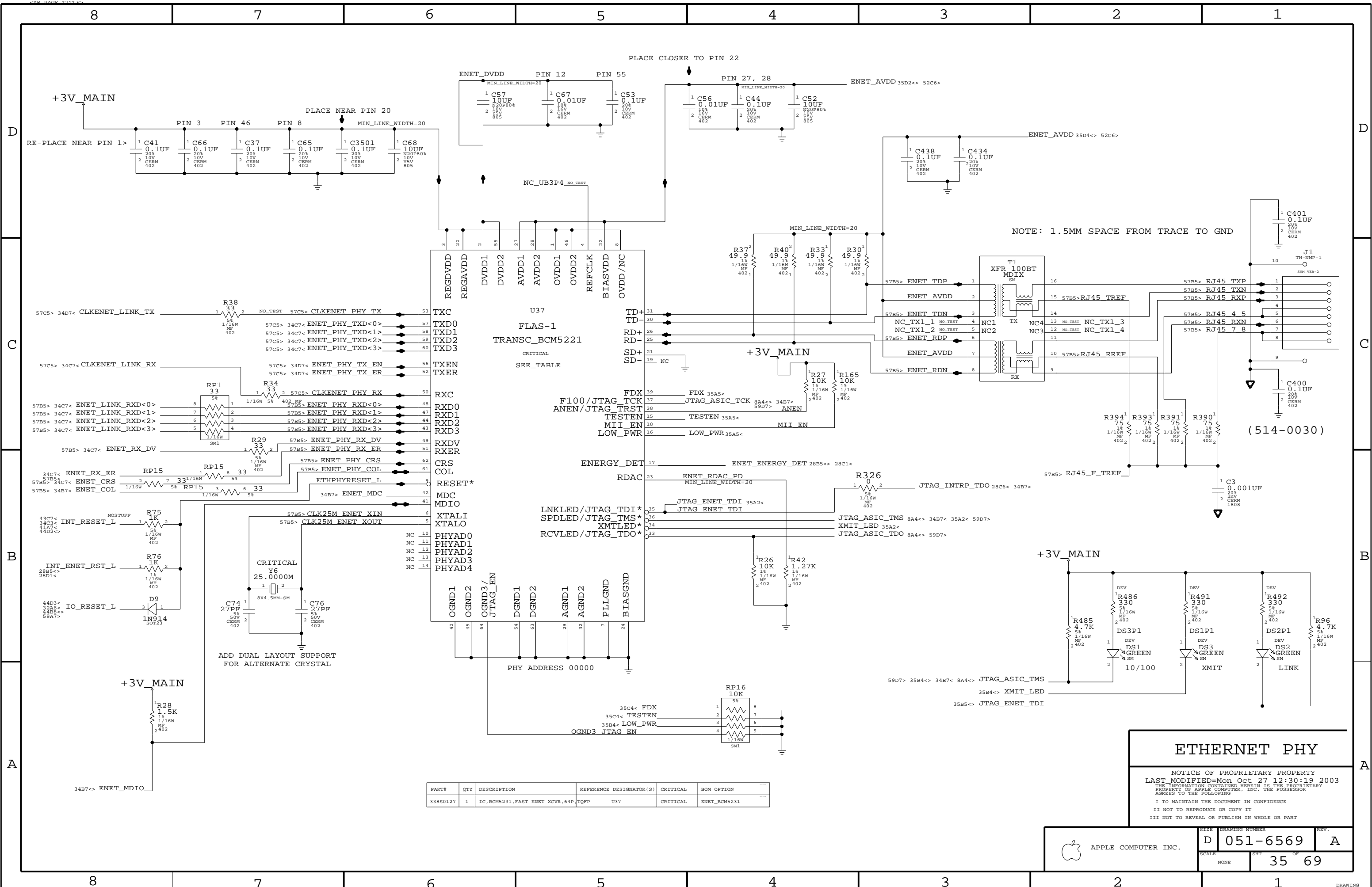
THE ABOVE RESISTORS SHARE THE SAME PIN-2 PAD AND ARE LOCATED AT THE USB2 CHIP

USB CONNS & PWR

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SCALE	SHT		OF
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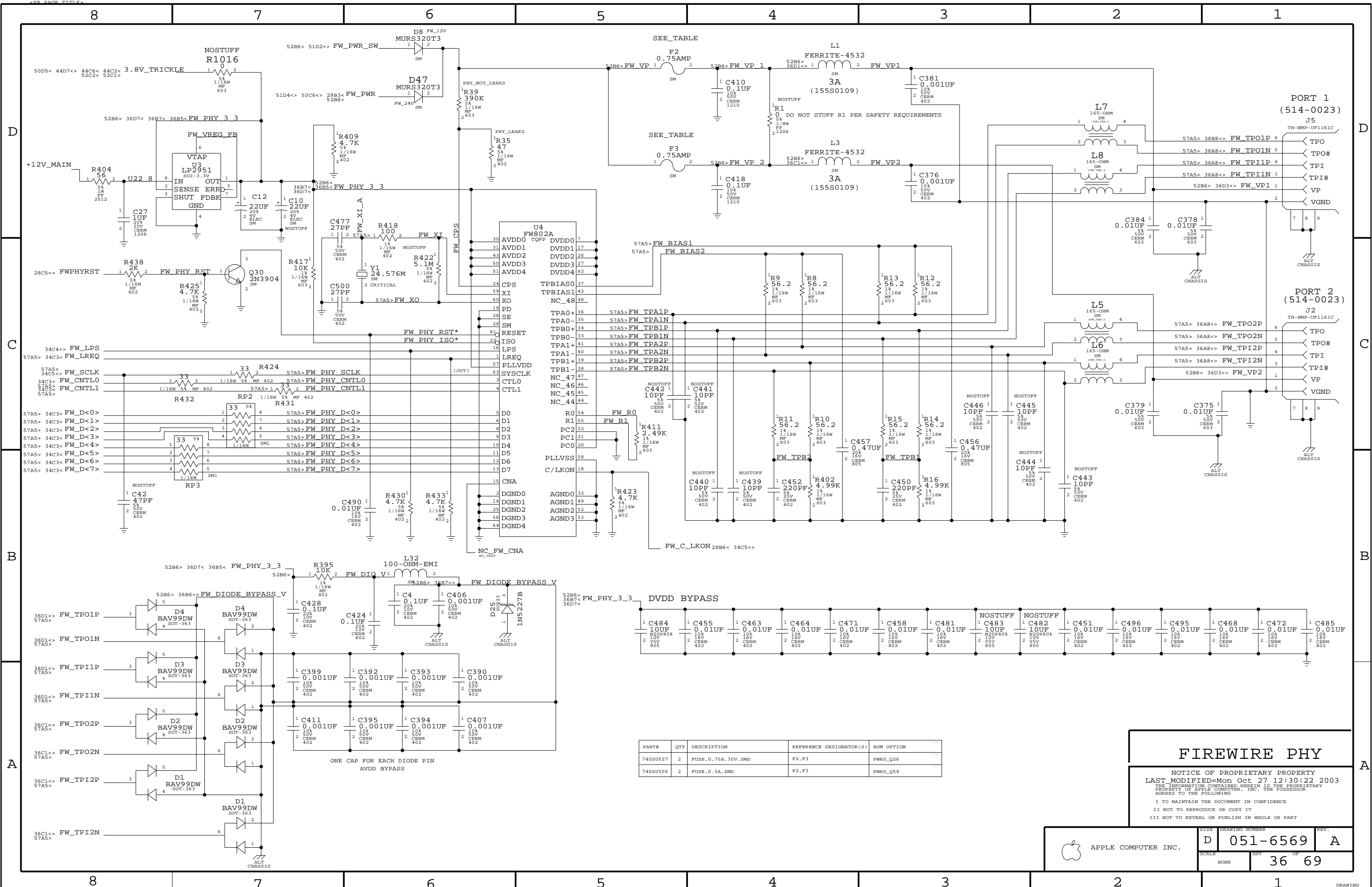


ETHERNET PHY

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	SCALE: NONE SHEET: 35 OF 69



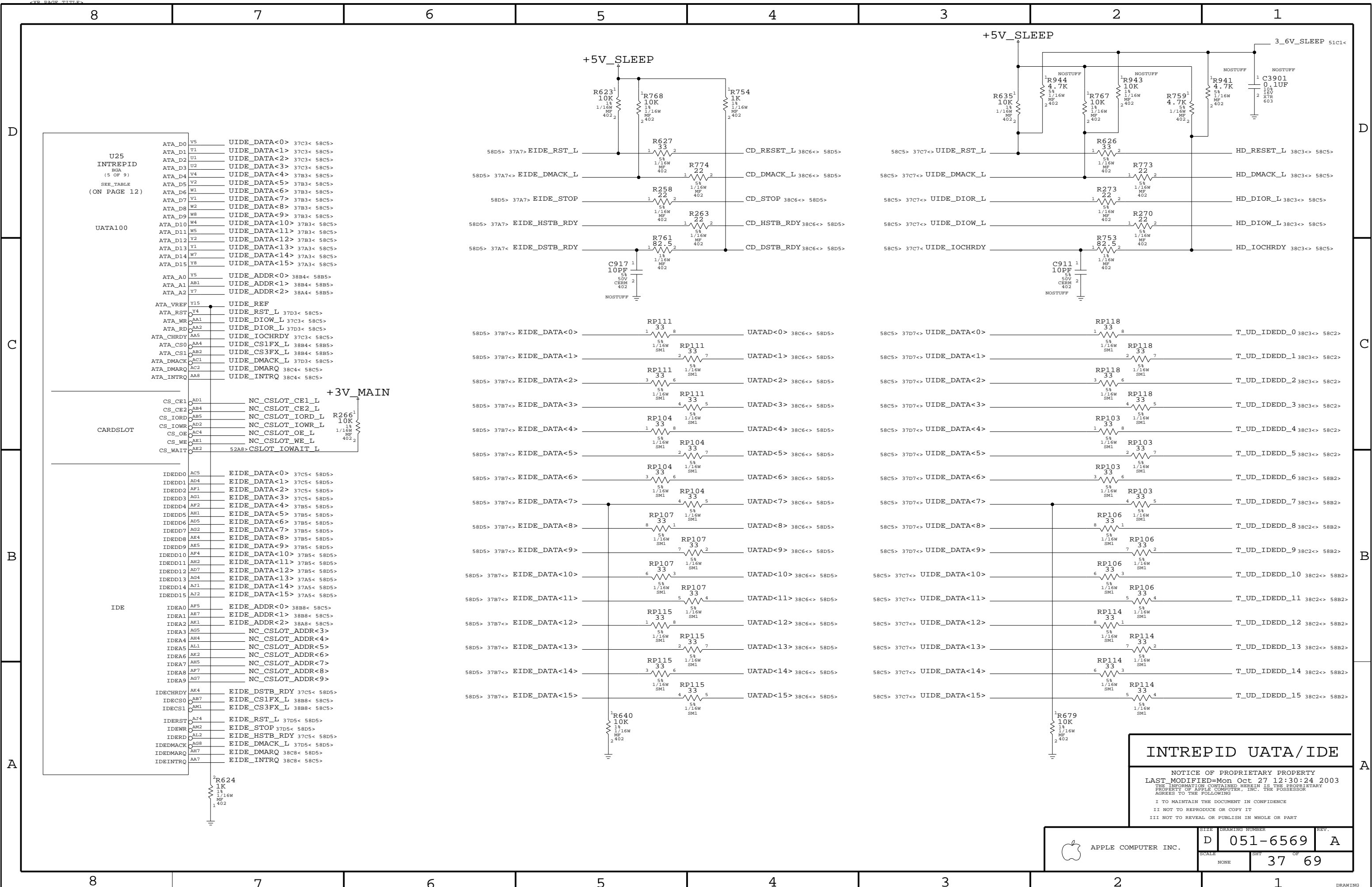
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
740S0527	2	FUSE, 0.75A, 30V, SMD	F2, F3	PWRS_Q26
740S0506	2	FUSE, 0.5A, SMD	F2, F3	PWRS_Q59

FIREWIRE PHY

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	NONE	D 051-6569	A
		SHT	OF
		36	69



INTREPID UATA/IDE

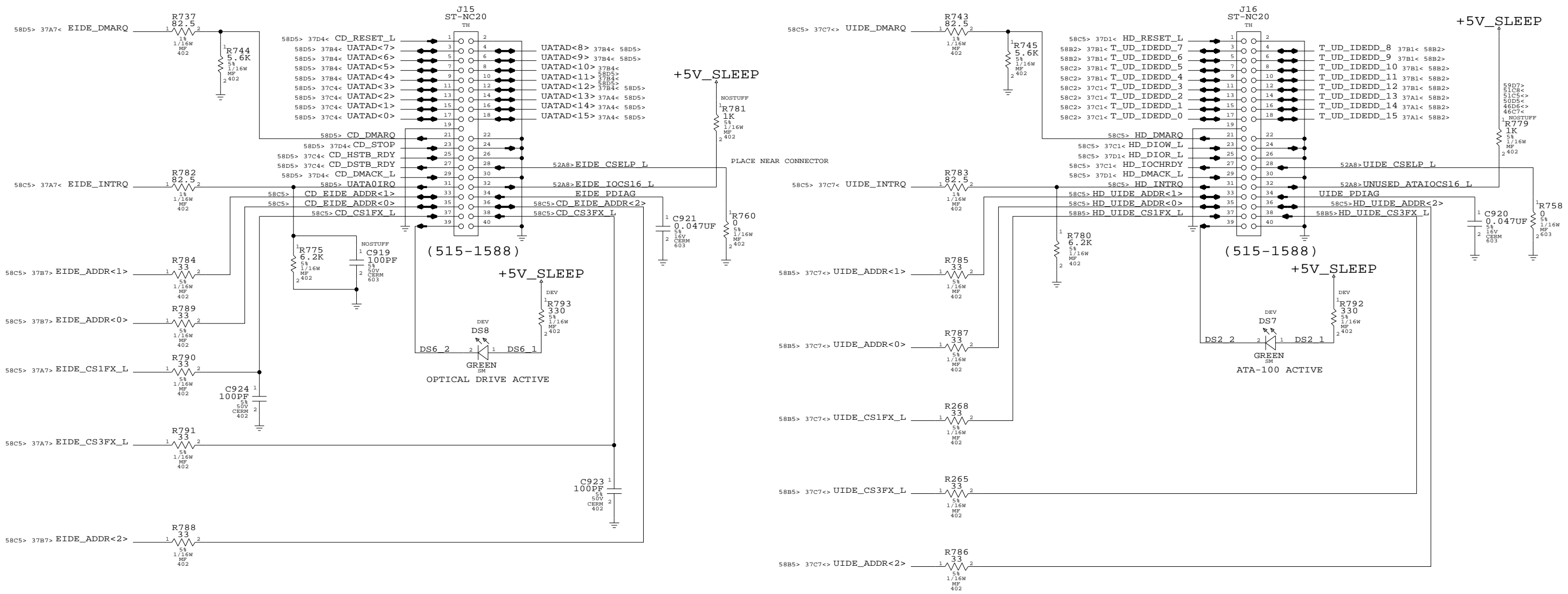
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	SCALE	37	OF 69

OPTICAL DRIVE INTERFACE

ATA-100 INTERFACE

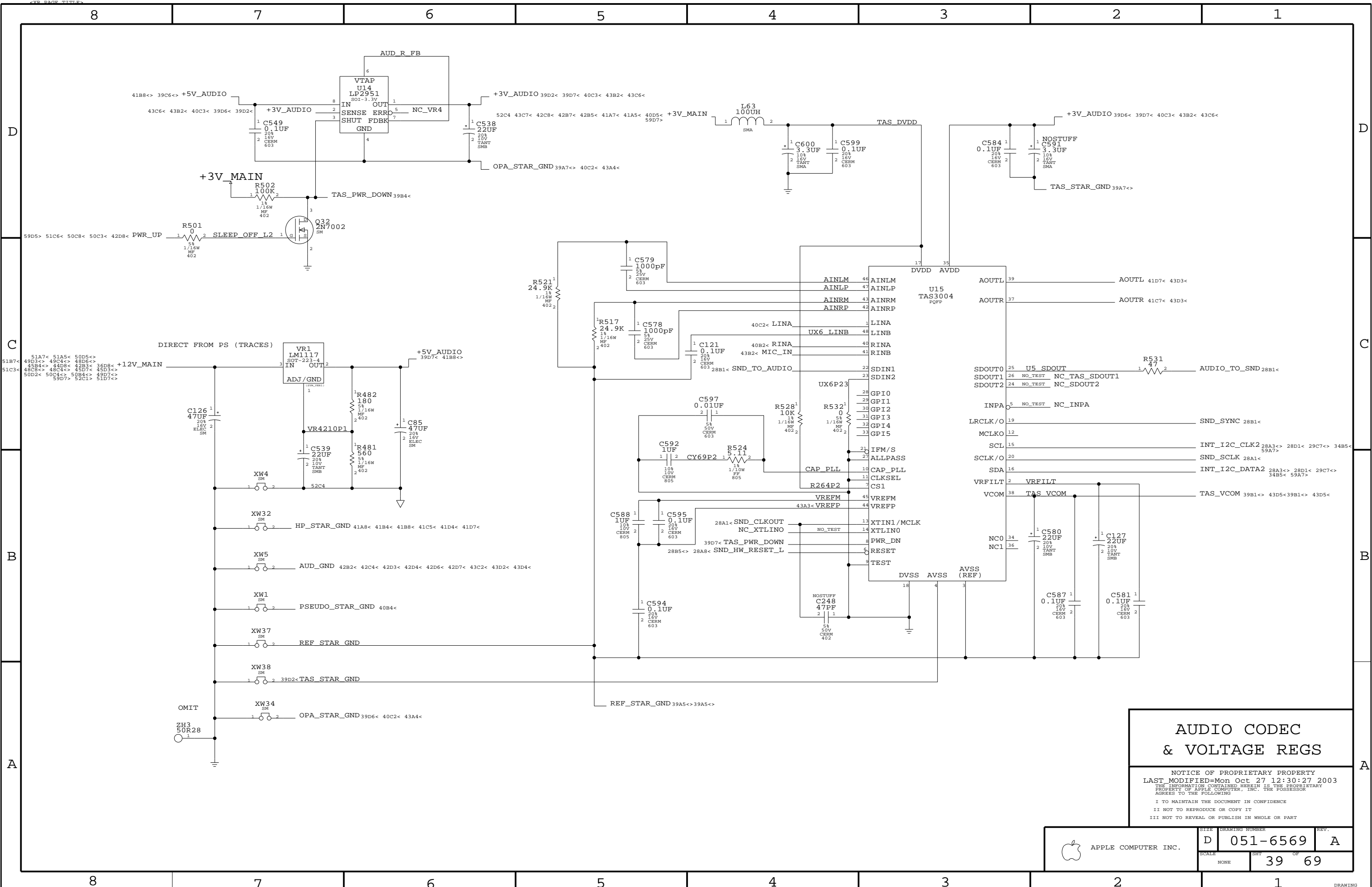


CD/HD CONS

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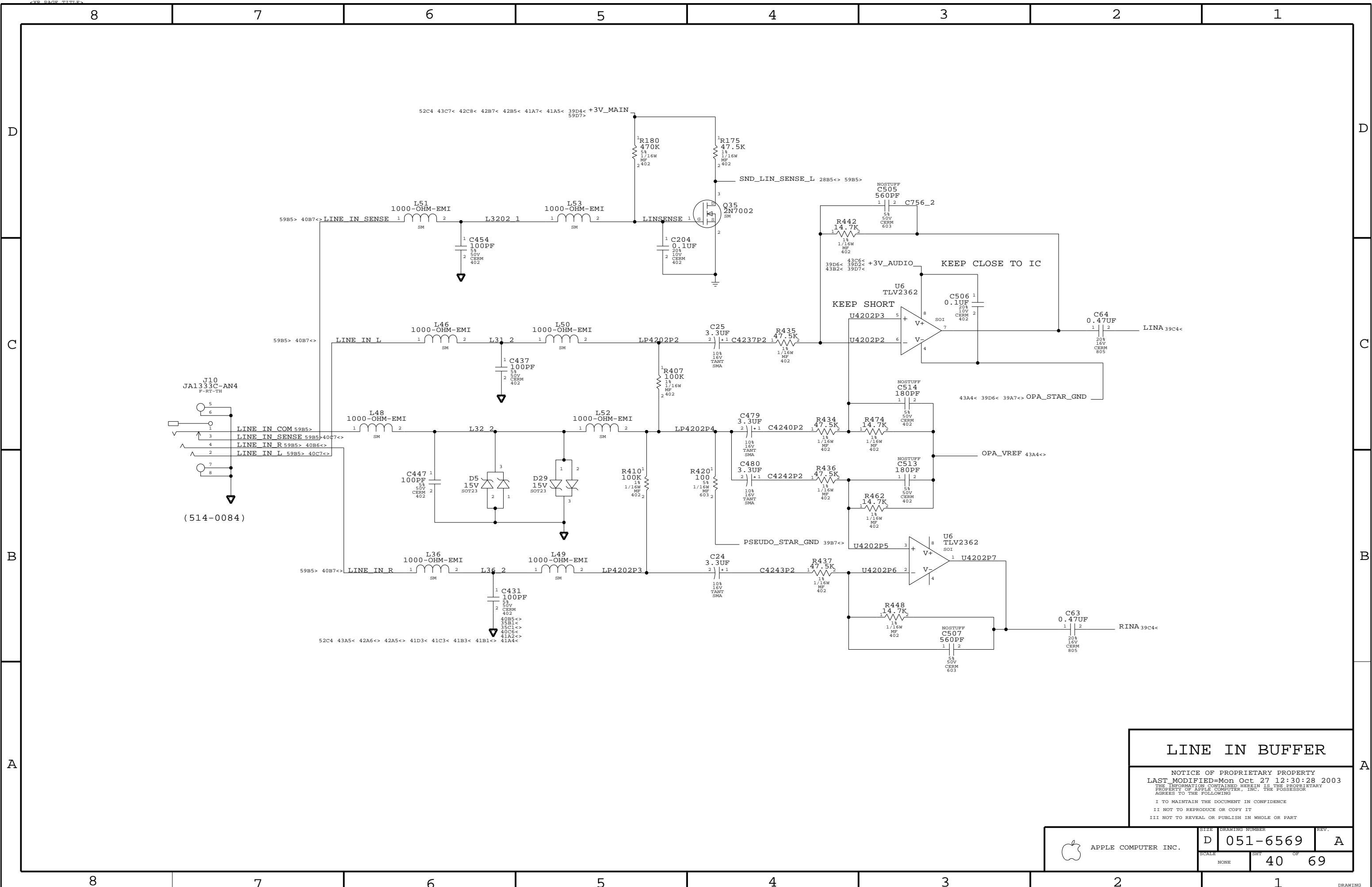
APPLE COMPUTER INC.	SIZE: D SCALE: NONE	DRAWING NUMBER: 051-6569	REV.: A
	SHEETS: 38 OF 69		



AUDIO CODEC & VOLTAGE REGS

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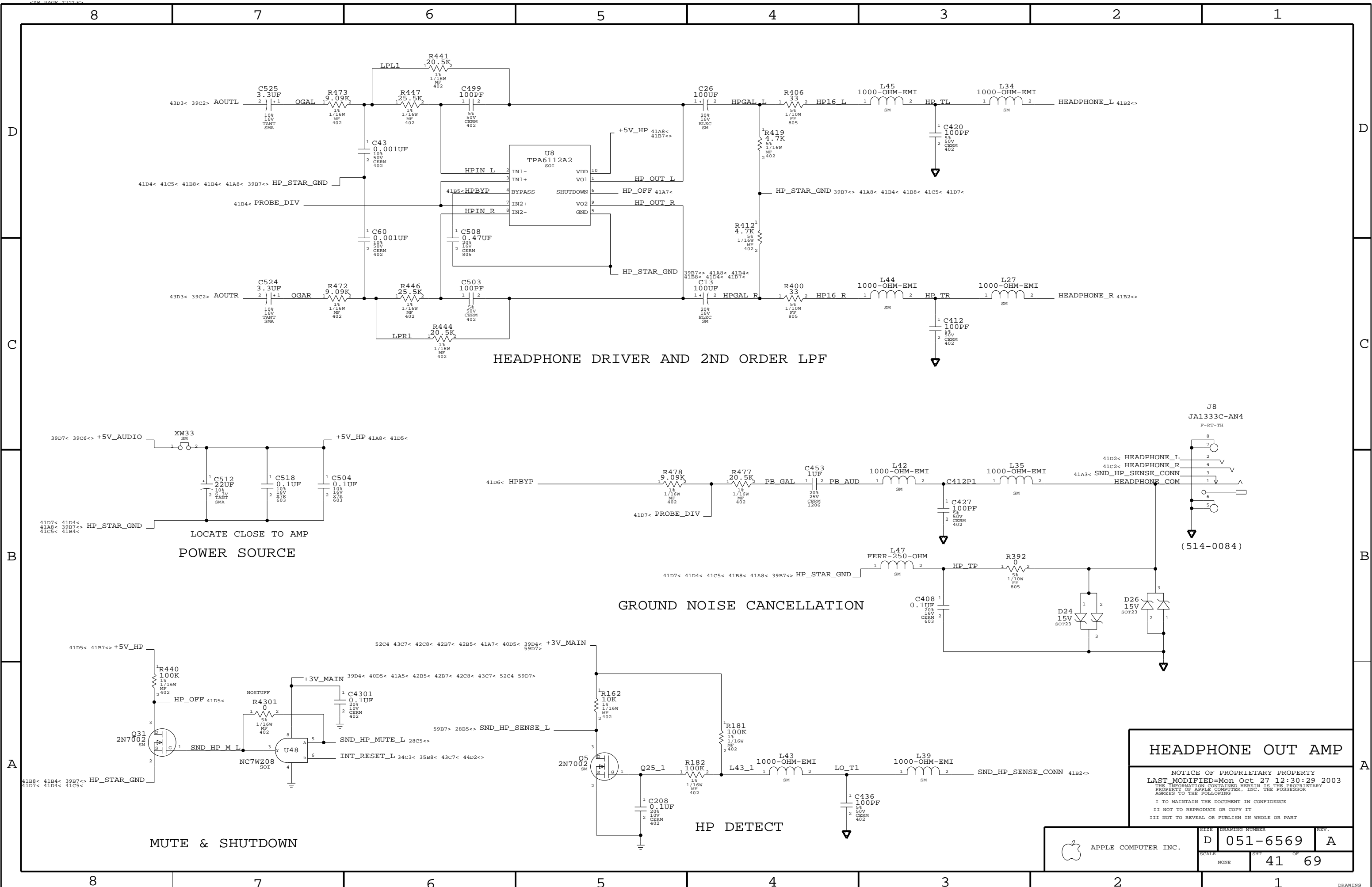
APPLE COMPUTER INC.	SIZE: DRAWING NUMBER: REV. D 051-6569 A
	SCALE: SHEET OF NONE 39 OF 69



LINE IN BUFFER

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	SHEETS: 40 OF 69		



HEADPHONE DRIVER AND 2ND ORDER LPF

LOCATE CLOSE TO AMP
POWER SOURCE

GROUND NOISE CANCELLATION

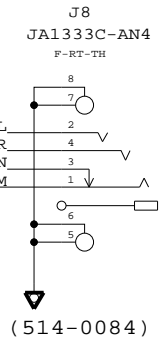
HP DETECT

MUTE & SHUTDOWN

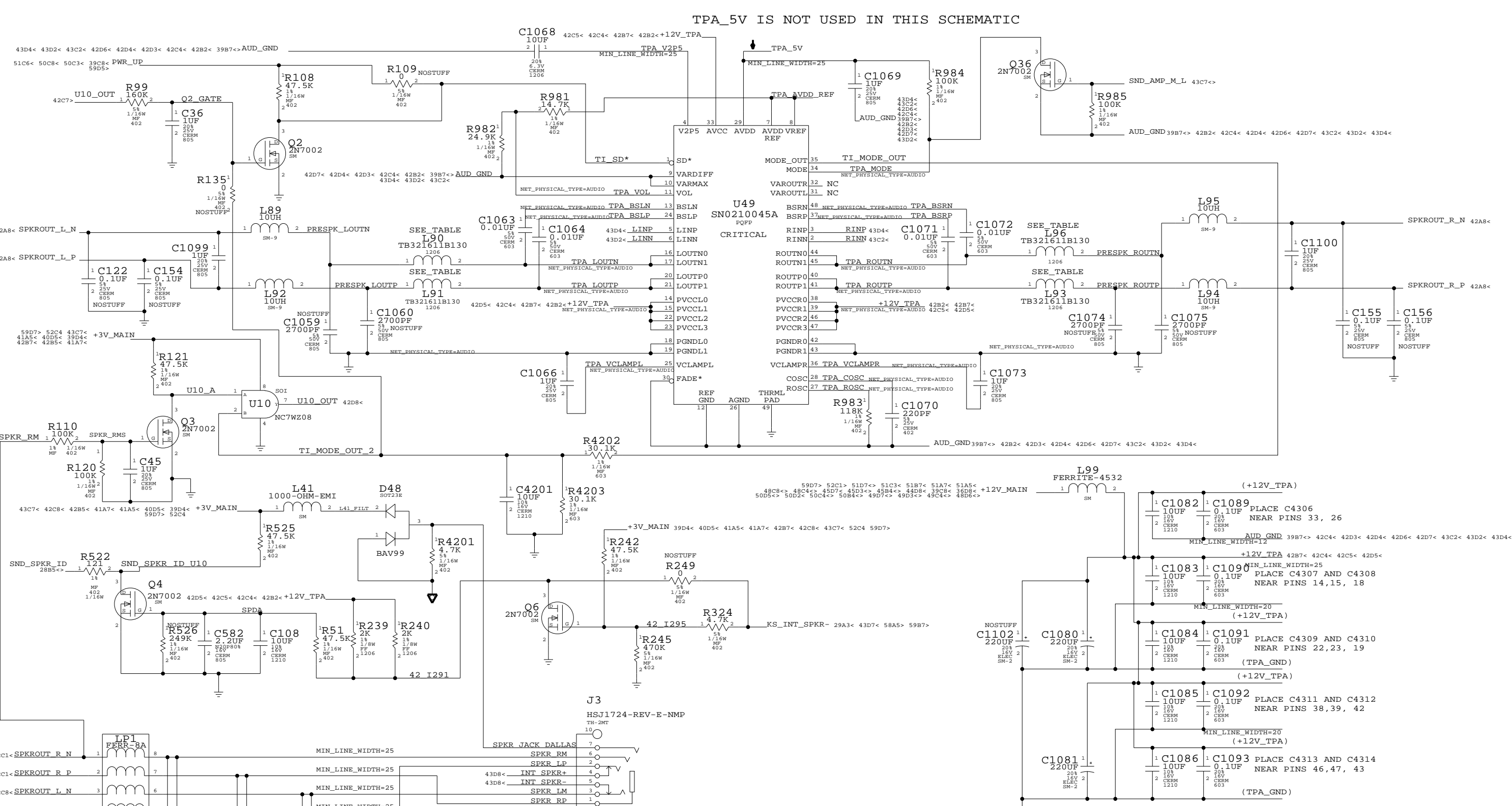
HEADPHONE OUT AMP

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		41	69



(514-0084)



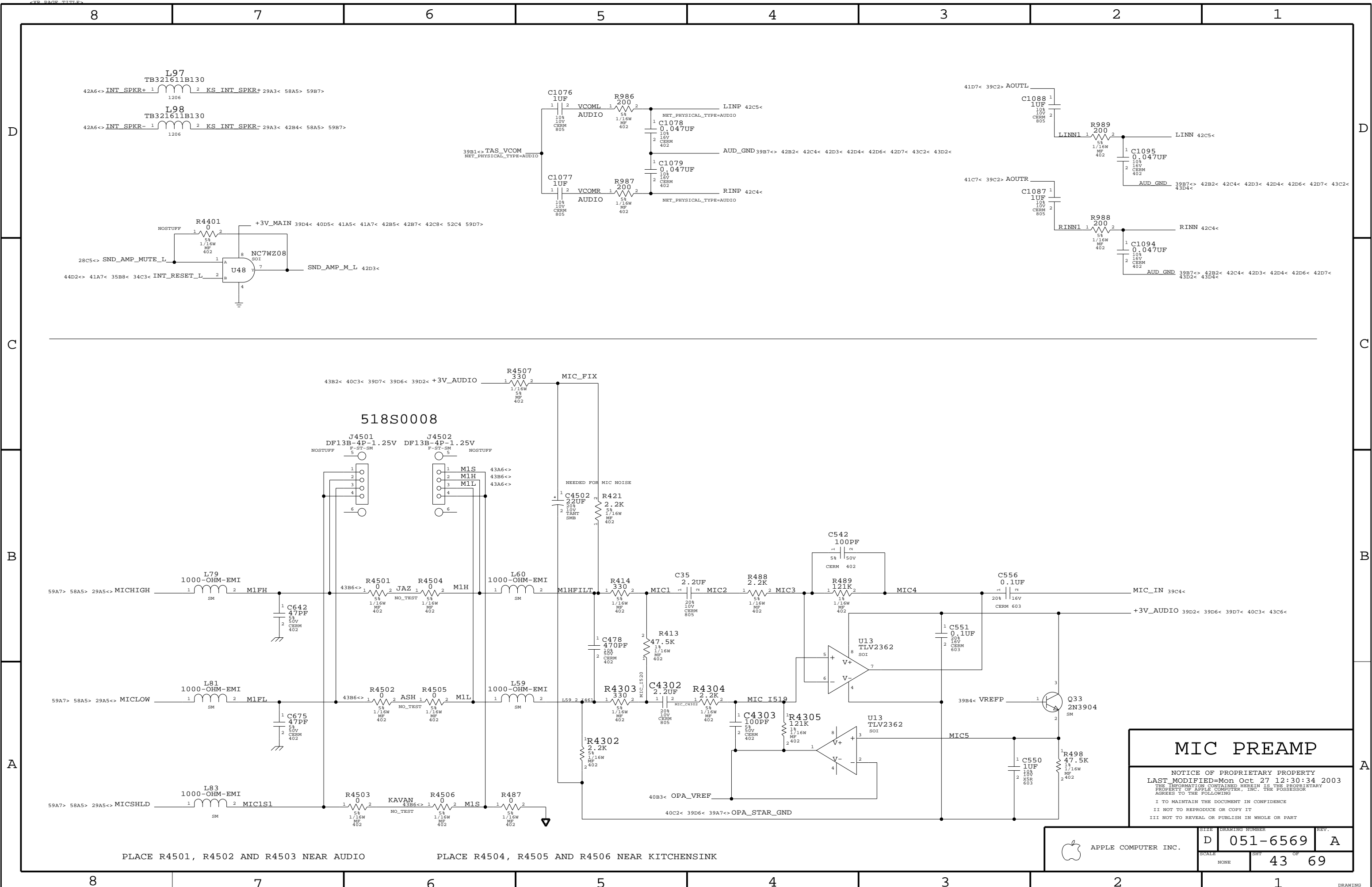
SPEAKER AMP

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
101S8000	4	0 OHM, 5%, 1/8W, RES-1206	L90, L91, L93, L96	

PREVIOUS PART NUMBER FOR L90, L91, L93, L96 IS 155S0148

SCALE	D	DRAWING NUMBER	REV.
NONE	42	051-6569	A
		SHEET	OF
		42	69



MIC PREAMP

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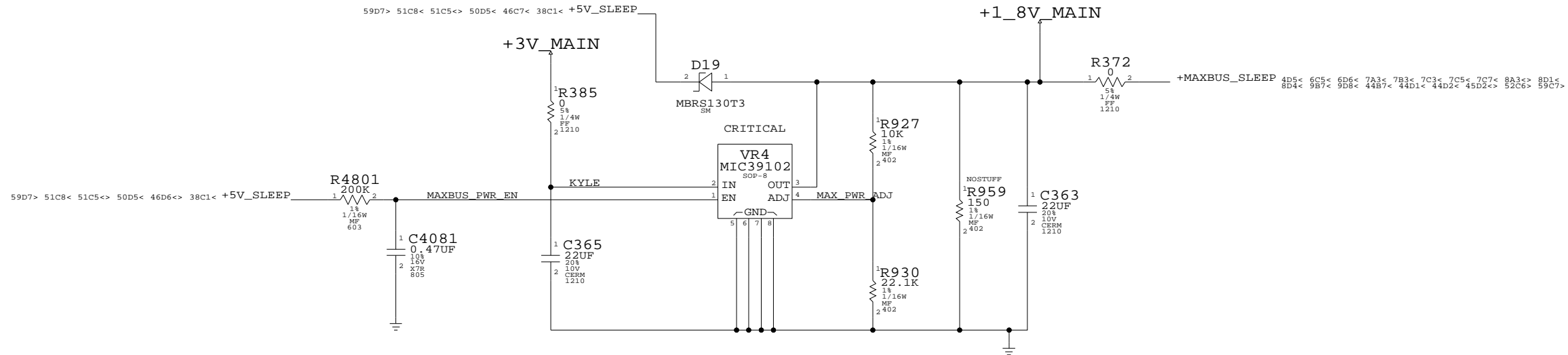
PLACE R4501, R4502 AND R4503 NEAR AUDIO

PLACE R4504, R4505 AND R4506 NEAR KITCHENSINK

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	SCALE	43	OF 69

INTREPID MAXBUS & CPU OVDD POWER CONVERTER
(OFF DURING SLEEP)

+MAXBUS_SLEEP 1.8V, +/-2%, .606W

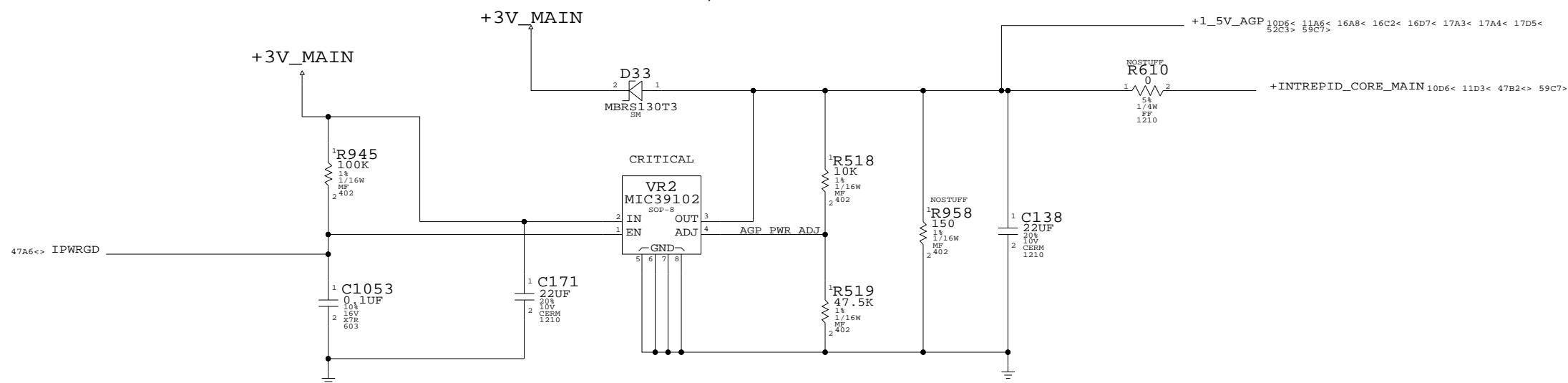


MAXBUS I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES, FF, 47.5K-OHM, 1%	R930		MAXIO_1'50V
114S3014	1	RES, FF, 30.1K-OHM, 1%	R930		MAXIO_1'65V
114S2674	1	RES, FF, 26.7K-OHM, 1%	R930		MAXIO_1'70V
114S2214	1	RES, FF, 22.1K-OHM, 1%	R930		MAXIO_1'80V

+1_5V_AGP 1.5V, +/-5%, .6W

AGP I/O POWER CONVERTER



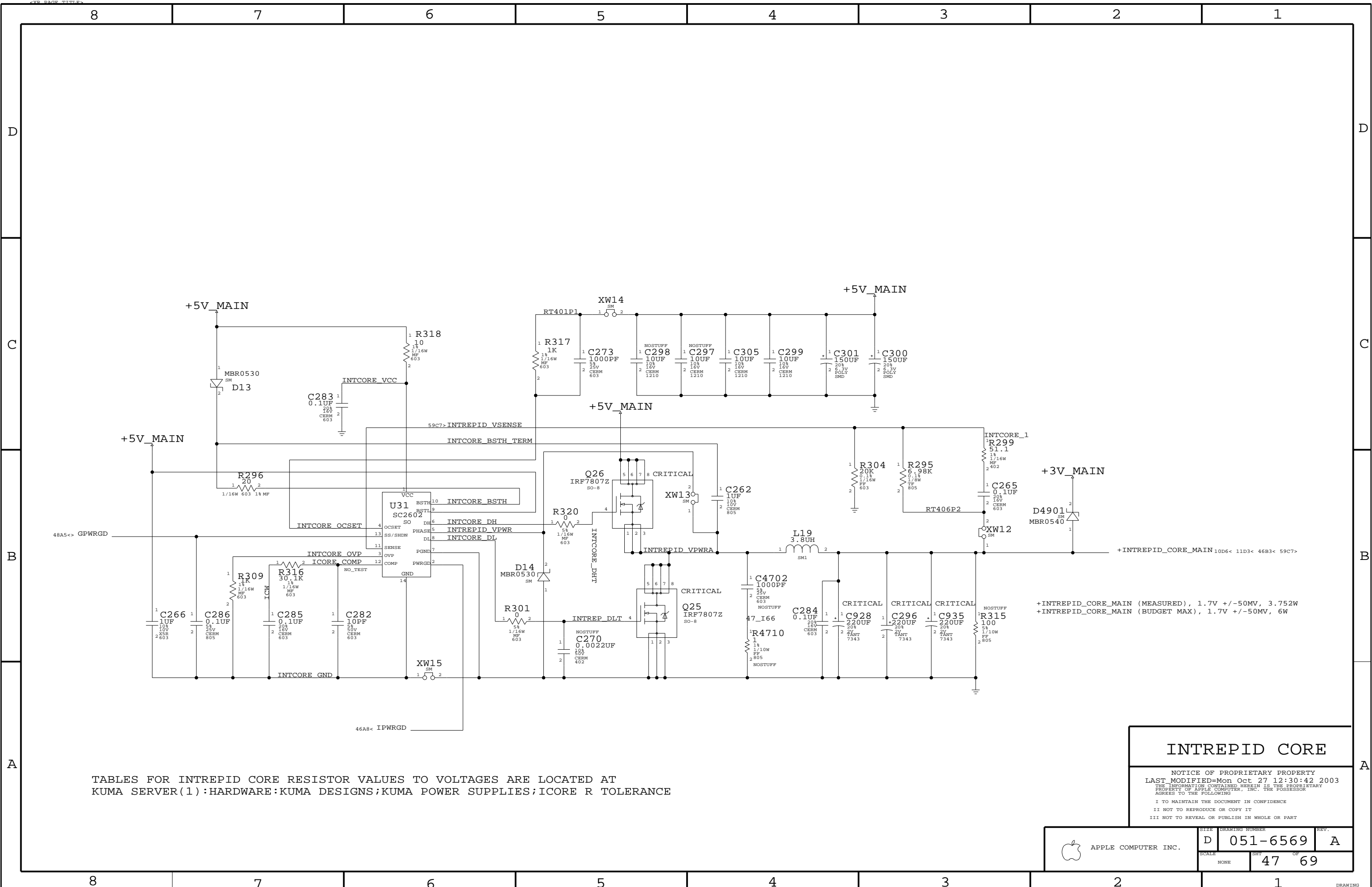
AGP I/O SUPPLY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S4754	1	RES, FF, 47.5K-OHM, 1%	R519		AGPIO_1'50V
114S3014	1	RES, FF, 30.1K-OHM, 1%	R519		AGPIO_1'65V
114S2674	1	RES, FF, 26.7K-OHM, 1%	R519		AGPIO_1'70V
114S2214	1	RES, FF, 22.1K-OHM, 1%	R519		AGPIO_1'80V

CPU & AGP VREGS

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NONE		46 OF 69	



TABLES FOR INTREPID CORE RESISTOR VALUES TO VOLTAGES ARE LOCATED AT
 KUMA SERVER(1):HARDWARE:KUMA DESIGNS;KUMA POWER SUPPLIES;ICORE R TOLERANCE

INTREPID CORE

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SCALE	SHEET		OF
NONE	47		69

D

D

C

C

B

B

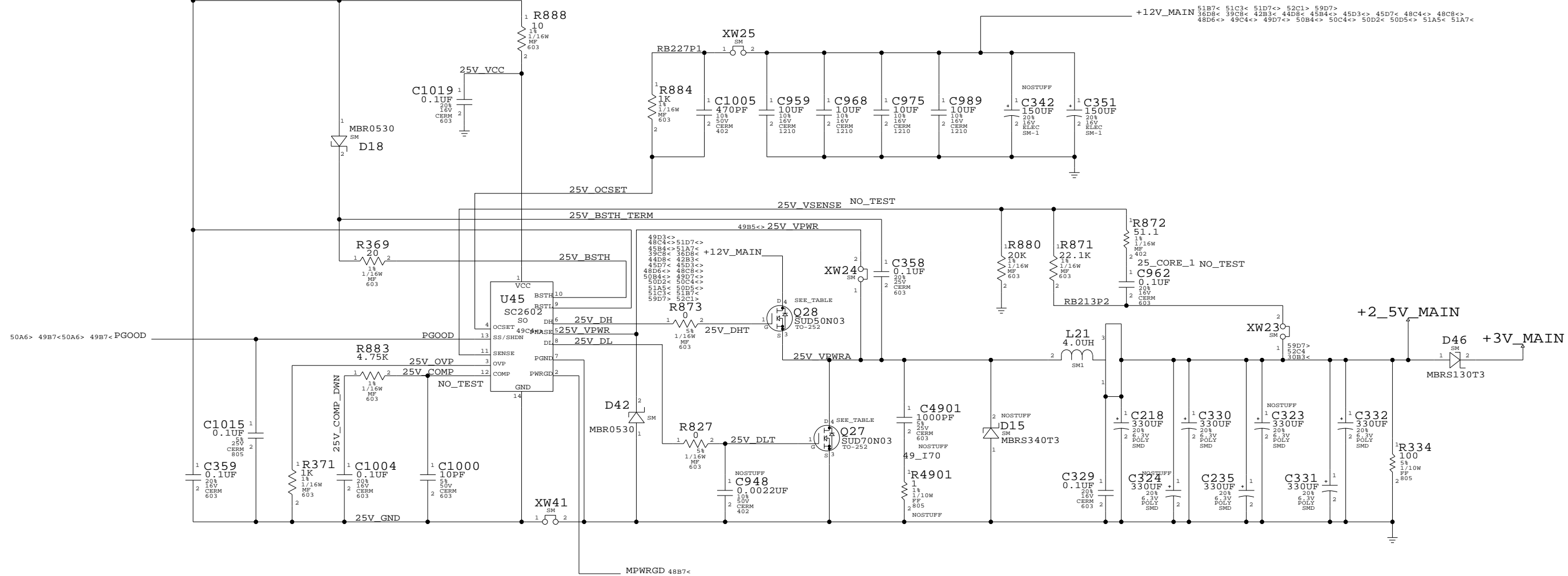
A

A

59D7> 52C1> 51D7<> 51C3< 51B7< 51A7< 51A5< +12V_MAIN
48C4<> 45D7< 45D3<> 45B4<> 44D8< 42B3< 39C8< 36D8< +12V_MAIN
50D5<> 50D2< 50C4<> 50B4<> 49D3<> 49C4<> 48D6<> 48C8<>

MAIN MEMORY DDR AND FRAME BUFFER POWER CONVERTER (2.50VDC)

+12V_MAIN 51B7< 51C3< 51D7<> 52C1> 59D7>
36D8< 39C8< 42B3< 44D8< 45B4<> 45D3<> 45D7< 48C4<> 48C8<>
48D8<> 49C4<> 49D7<> 50B4<> 50C4<> 50D2< 50D5<> 51A5< 51A7<



+2.5V_MAIN, 1.61V +/-50MV, 12.908W

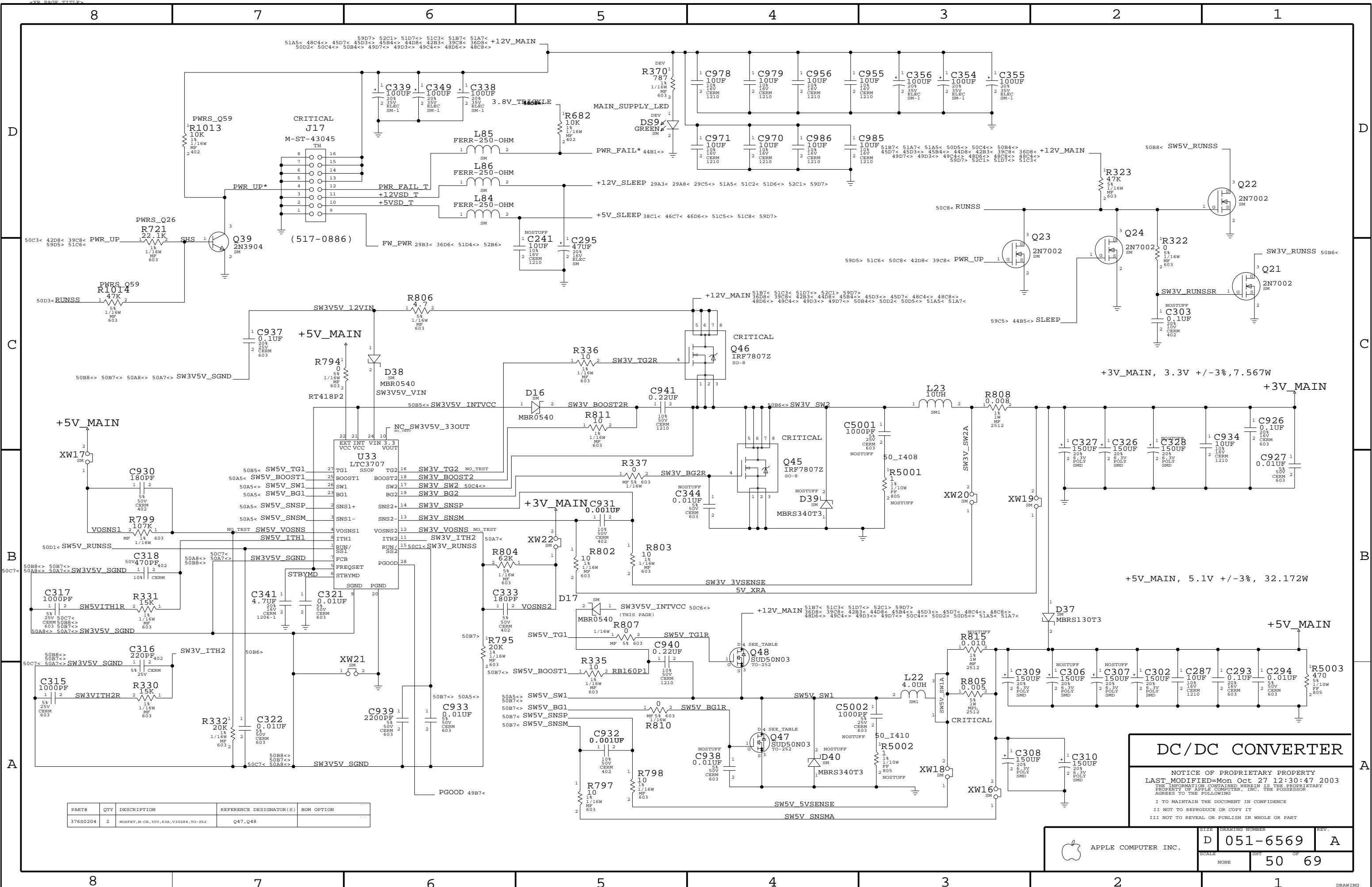
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0204	1	MOSFET, N-CH, 30V, 63A, V30284, TO-252	Q28	
376S0207	1	MOSFET, N-CH, 30V, 70A, V30289, TO-252	Q27	

MEMORY PS

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NONE		49	69



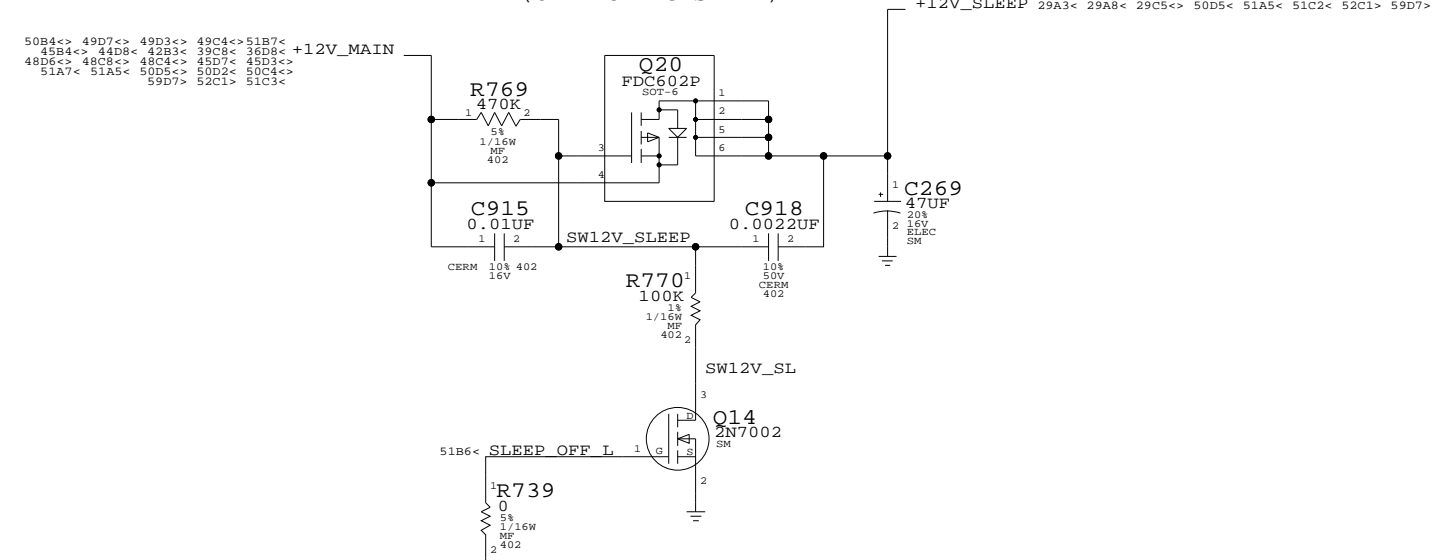
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
37650204	2	MOSFET, N-CH, 30V, 63A, V30204, TO-252	Q47, Q48	

DC/DC CONVERTER

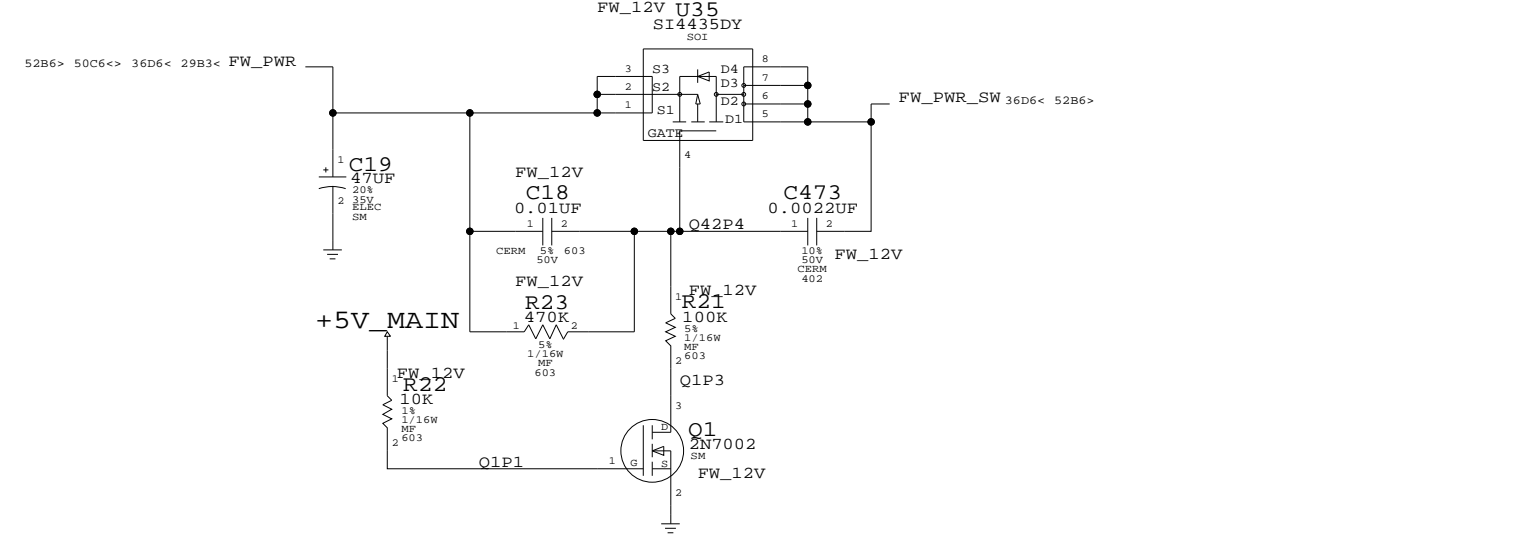
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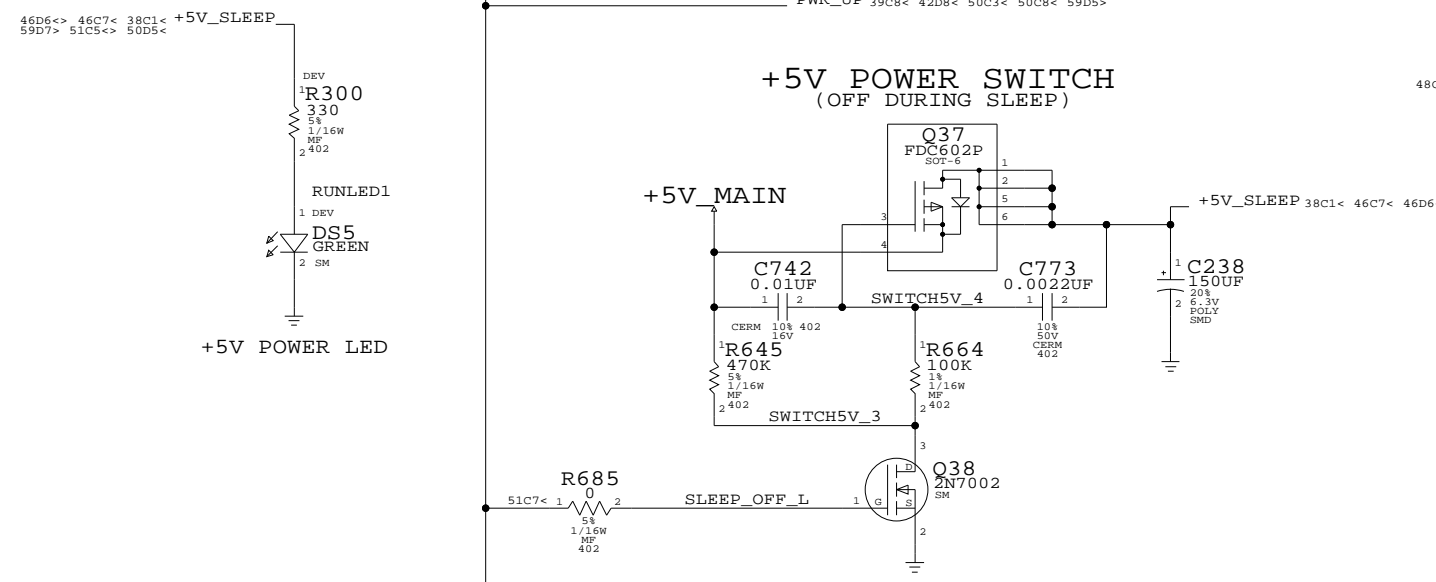
+12V MAIN POWER SWITCH (OFF DURING SLEEP)



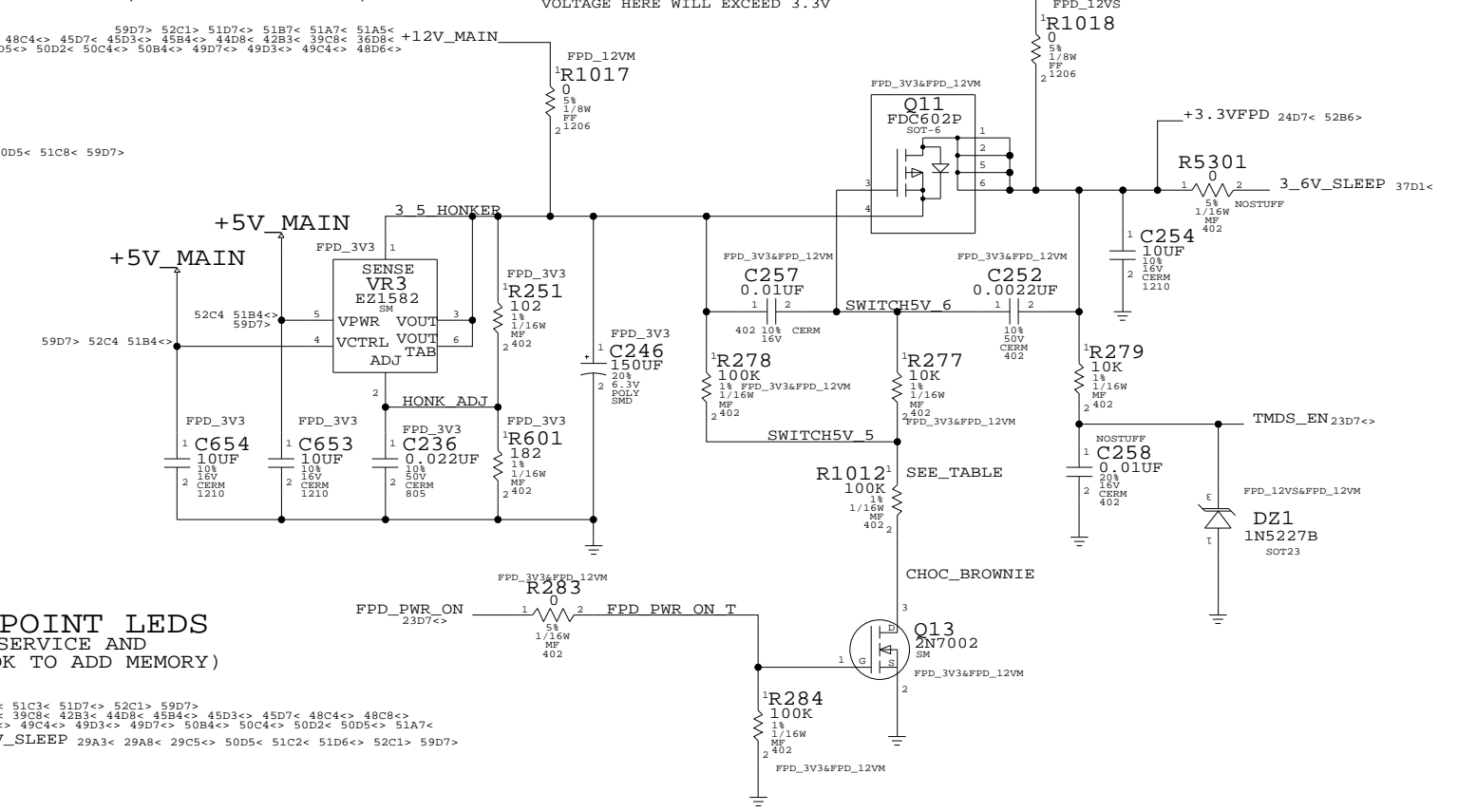
FIREWIRE POWER SWITCH EVALUATE CIRCUIT FOR SURGE PROTECTION FOR Q59C



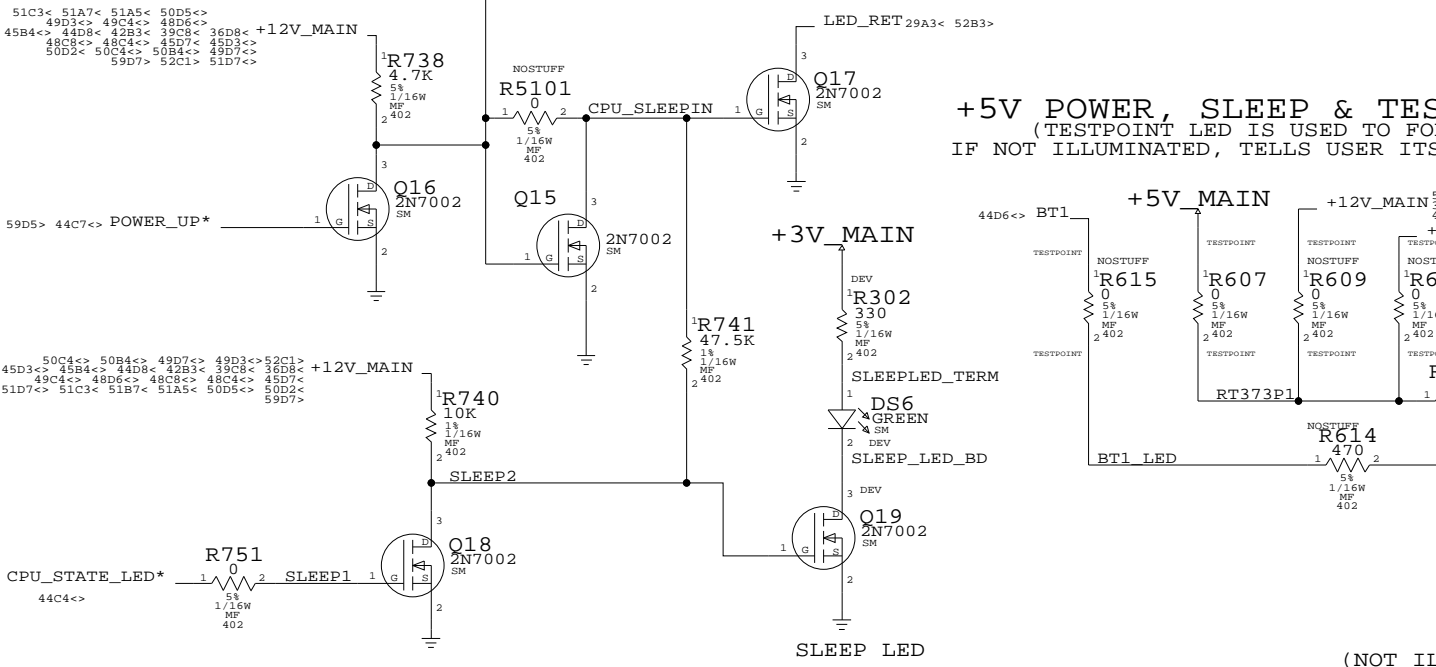
+5V POWER SWITCH (OFF DURING SLEEP)



TMDS POWER CONVERTER & SWITCH (OFF DURING SLEEP)



+5V POWER, SLEEP & TESTPOINT LEDS (TESTPOINT LED IS USED TO FOR SERVICE AND IF NOT ILLUMINATED, TELLS USER ITS OK TO ADD MEMORY)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1005	1	RES,100K OHM,1%,1/16W,0402,SMD	R1012	FPD_12VM
116S1000	1	RES,0 OHM,5%,1/16W,0402,SMD	R1012	FPD_3V3

+5V/+12V, AUDIO FW & TMDS PWR

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NONE	51	69	

CPU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+MAXBUS_SLEEP	10	1.8	20
CPU_AVDD	10	1.85	20
CPU_VCORE_SLEEP	10	1.85	20

4D5< 6C5< 6D6< 7A3< 7B3< 7C3< 7C5< 7C7< 8A3< 8D1< 8D4< 9B7< 9D8< 44B7<
 44D1< 44D2< 45D2< 46D4< 59C7>
 4D3< 4D7< 8B7< 8C1< 45D2< 59B5> 59D7>

ETHERNET POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
ENET_AVDD	10	2.5	20

59D7>
 59D7> 49B2<> 30B3<
 43C7< 42C8< 42B7< 42B5< 41A7< 41A5< 40D5< 39D4<
 59D7>
 59D7> 51B4<>

FIREWIRE POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
FW_DIO_V	10	3.3	20
FW_DIODE_BYPASS_V	10	3.3	20
FW_PWR	10	24	20
FW_PWR_SW	10	24	20
FW_PHY_3_3	10	3.3	20
FW_VGND	10	0	20
FW_VP	10	1.2	20
FW_VP1	10	1.2	20
FW_VP2	10	1.2	20
FW_VP_1	10	1.2	20
FW_VP_2	10	1.2	20

35D2<> 35D4<>
 39B7<>
 41B3< 41B1<> 41A4< 41A2<> 40C6< 40B6< 40B5<> 35C1<> 35B1<
 43A5< 42B6<> 42A5<> 41D3< 41C3<
 36B6<> 36B2< 36A7<> 33D4< 33C4< 32C2< 31B4< 29C3< 29B3<>
 36C1< 36C1<> 36B6<
 43B7< 43A7< 29A3< 24B5<

GRAPHICS POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3.3VFPD	10	3.6	20
DAC2VDD	10	3.3	20
DACVDD	10	3.3	20
DDC_VCC_3	10	3.3	20
DDC_VCC_5	10	5	20
DDR_VREF	10	1.25	20
IFP0AVCC	10	3.8	20
IFP0VREF	10	3.8	20
INT_TMDS_3V	10	3.6	20
GPU_AGP_VREF	10	0.75	20
GPU_FB_VREF	10	1.25	20
GRAPH_CORE	10	1.6	20
NVPLLVDD	10	3.3	20
SGRAVREF	10	1.25	20
SGRBVREF	10	1.25	20

36B6<
 36B6<> 36B7<>
 29B3< 36D6< 50C6<> 51D4<>
 36D6< 51D2<>
 36B5< 36B7< 36D7<
 36D5<
 36D1<> 36D3<>
 36C1<> 36D3<>
 36D4<
 36D4<
 24D7< 51C1<>
 22C5<
 22C4<
 24B3<> 59B7>
 25C4< 59B7>
 12A7< 14D2<> 14D8<> 15D8<
 23A6< 23C1<
 23B4<>
 24C3<> 59C7>
 17A2< 17A8<
 18C8<
 17D4< 23C7<> 48C2<>
 22D5<
 20A3< 20C4< 20C8<
 21A3< 21C4< 21C8<

17B5<> GPU_50PULLUP	1.5	
17A5<> GPU_50PULLDOWN	0	
17A5< GPU_TMODE	0	
22B2< 22A5< GPU_XTALSSIN	0	
22D4< VIPCLK	0	
37B7< CSL0T_IOWAIT_L	3.3	
38C6<> EIDE_CSELP_L	0	
38C6<> EIDE_IOCS16_L	5	
38C2<> UIIDE_CSELP_L	0	
38C2<> UNUSED_ATAI0CS16_L	5	

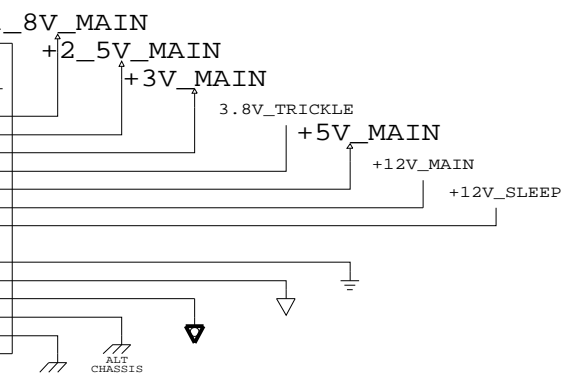
INTREPID POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_5V_INTREPID_PLL	10	1.5	20
+1_5V_INTREPID_PLL1	10	1.5	20
+1_5V_INTREPID_PLL2	10	1.5	20
+1_5V_INTREPID_PLL3	10	1.5	20
+1_5V_INTREPID_PLL4	10	1.5	20
+1_5V_INTREPID_PLL5	10	1.5	20
+1_5V_INTREPID_PLL6	10	1.5	20
+1_5V_INTREPID_PLL7	10	1.5	20
+1_5V_INTREPID_PLL8	10	1.5	20
+1_5V_AGP	10	1.5	20
INT_AGP_VREF	10	0.75	20

9D4< 16D6< 28D6<> 30D5<
 28C4<
 28D4<
 28D4<
 28D4<
 16D5<
 30D4<
 9D2<
 28D4<
 10D6< 11A6< 16A8< 16C2< 16D7< 17A3< 17A4< 17D5< 46B4<> 59C7>
 16A7< 16C6<>

MAIN POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+1_8V_MAIN	10	1.8	20
+2_5V_MAIN	10	2.5	20
+3V_MAIN	10	3.3	20
3.8V_TRICKLE	10	3.8	20
+5V_MAIN	10	5	20
+12V_MAIN	10	12	20
+12V_SLEEP	10	12	20
GND	10	0	20
AGND	10	0	20
ANALOGGND	10	0	20
ALTCHGND	10	0	20
CHGND	10	0	20



PMU POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
3.8VH_TRICKLE	10	3.8	20
PMU_AVCC	10	3.5	20
PMU_POWER	10	3.5	20

44C1< 44D7<>
 44B5< 44D4<> 59C5>
 29C3<> 44A5<> 44B1< 44C2< 44D5<>

SYSTEM POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+12VSD_FILT	10	12	20
FAN_12V_FILT	10	12	20
KSSVSD	10	5	20
LED_5V	10	5	20
LED_5V_FILT	10	5	20
LED_RET	10	0	20
LED_RET_FILT	10	0	20

29A5<>
 29A5<> 59C7>
 29A5<> 59A7>
 29A8<
 29A5<> 59A7>
 29A3< 51B6<
 29A5<> 59A7>

USB POWER CONSTRAINT TABLE

SIG_NAME	MIN_NECK_WIDTH	VOLTAGE	MIN_LINE_WIDTH
+3V_INTREPID_USB	10	3.3	20
NEC_AVDD	10	3.3	20
USB_GND	10	0	20
USB_PORT_PWR	10	5	20
USB_PWR	10	5	20

28C4<
 32D5<
 33A4<> 33B3<> 33C3<>
 33B2<> 33B3<> 25D3<> 33A6<>

POWER CONSTRAINTS

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NONE	52	69	

D

D

C

C

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B

A

A

SIG_NAME	RATSNEST_SCHEDULE	RELATIVE_PROPAGATION_DELAY	MIN_NECK_WIDTH	MAX_EXPOSED_LENGTH	NO_TEST	FUNC_TEST	PULSE_PARAM
13C4<> 13B6<> 13B3<> 13A6<> 12D8<> 12C8<> 12B8<> MEM_DATA<0..63>	MEM_GROUP0:G:L:S:0:150	8 L:S::1300	3				167 MHZ
13D4<> 13C7<> 13C4<> 13C2<> 13B5<> 13B2<> RAM_DATA_A<0..63>	RAM_GROUP0_A:G:L:S:0:180	8 L:S::1800	3				167 MHZ
14C4<> 14B6<> 14B4<> 14A6<> 14A4<> 13D7<> RAM_DATA_B<0..63>	RAM_GROUP0_B:G:L:S:0:180	2 L:S::2400	3				167 MHZ
13B2<> 13A5<> 15D6<> 13A2<> 15A6<> 15B4<> 15B6<> 15C4<> 15C6<> 15D4<>	MEM_GROUP0:G:L:S:0:180	3 L:S::1300	3				167 MHZ
13C8<> 13C4<> 13B3<> 13A6<> 12C6<> MEM_DQS<0..7>	RAM_GROUP0_A:G:L:S:0:180	3 L:S::1700	3				167 MHZ
14A6<> 13D7<> 13D4<> 13C7<> 13C4<> 13B5<> 13B2<> RAM_DQS_A<0..7>	RAM_GROUP0_B:G:L:S:0:180	2 L:S::2400	3				167 MHZ
13C7<> 13C4<> 13B7<> 13B4<> 13B2<> 13A5<> RAM_DQS_B<0..7>	MEM_GROUP0:G:L:S:0:180	3 L:S::1300	3				167 MHZ
15D6<> 15C8<> 15C6<> 15D4<> 15B6<> 15B4<> 15A6<> MEM_DQM<0..7>	RAM_GROUP0_A:G:L:S:0:180	3 L:S::1800	3				167 MHZ
13D7<> 13D4<> 13C7<> 13C4<> 13B5<> 13B2<> 13A5<> RAM_DQM_A<0..7>	RAM_GROUP0_B:G:L:S:0:180	2 L:S::2400	3				167 MHZ
13C7<> 13C4<> 13B7<> 13B4<> 13B2<> 13A5<> RAM_DQM_B<0..7>							
12D6<> 12D3<> 12D2<> 12C3<> 12C2<> 12B3<> MEM_ADDR<0..12>	MEM_ADDR:G:L:S:0:200	3 L:S::600					
15B4> 14B6<> 14B4> 12D3<> 12D1<> 12C3<> 12C1<> 12B3<> RAM_ADDR<0..12>	RAM_ADDR:G:L:S:0:1300	4 L:S::3500	200				
15C6<> 15C4<> 15B6<> 15B4<> 15A6<> 12D6<> 12B3<> MEM_BA<0..1>	MEM_ADDR:G:L:S:0:1300	3 L:S::600					
15B6<> 14B6<> 14B4> 12B3<> RAM_BA<0..1>	RAM_ADDR:G:L:S:0:1300	4 L:S::4000	200				
12C6<> 12C2<> 12B2<> MEM_CS_L<0..3>	MEM_ADDR:G:L:S:0:200	3 L:S::600	10 MIL SPACING				
14B6<> 14B4> 12C1<> RAM_CS_L<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3 L:S:2000:3500	10 MIL SPACING				
15B4> 12B1<> RAM_CS_L<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2 L:S:2000:3500	10 MIL SPACING				
12C6<> 12A3<> MEM_RAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3 L:S::600 MIL					
12C6<> 12A3<> MEM_CAS_L	MEM_ADDR:G:L:S:0 MIL:200 MIL	3 L:S::600 MIL					
12C6<> 12B3<> MEM_WE_L	MEM_ADDR:G:L:S:0 MIL:280 MIL	3 L:S::600 MIL					
15B6<> 14B4> 12A2<> RAM_CAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4 L:S::4000 MIL	200				
15B4> 14B4> 12A2<> RAM_RAS_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4 L:S::4000 MIL	200				
15B6<> 14B6> 12B3<> RAM_WE_L	RAM_ADDR:G:L:S:0 MIL:2000 MIL	4 L:S::4000 MIL	200				
12C6<> 12C2<> 12B2<> MEM_CKE<0..3>	MEM_ADDR:G:L:S:0:200	3 L:S::600	10 MIL SPACING				
15C1<> 14B6<> 14B4> 12C1<> 12B1<> RAM_CKE<0..1>	RAM_CS_GROUP0:G:L:S:0:400	3 L:S::2500	10 MIL SPACING				
15C6<> 15C4> 15B1<> 15A1<> 12C1<> 12B1<> RAM_CKE<2..3>	RAM_CS_GROUP1:G:L:S:0:350	2 L:S::2500	10 MIL SPACING				
12B6<> MEM_MUXSEL_H<0..1>		3 L:S::1000					
12B6<> MEM_MUXSEL_L<0..1>		3 L:S::1000					167 MHZ
13C4<> 13A3<> 12D4<> MUX_SEL_H		4 L:S::2000 MIL	200				167 MHZ
13C8<> 13A6<> 12D4<> MUX_SEL_L		4 L:S::2000 MIL	200				167 MHZ
12B6<> SYSCLK_DDRCLK_A0_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A0_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
14D6<> 12C4<> SYSCLK_DDRCLK_A0	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
14D6<> 12C4<> SYSCLK_DDRCLK_A0_L	SYSCLK_DDRCLKA0:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_A1_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A1_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
14A4<> 12C4<> SYSCLK_DDRCLK_A1	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
14A4<> 12B4<> SYSCLK_DDRCLK_A1_L	SYSCLK_DDRCLKA1:G:L:S:0 MIL:100 MIL	3 L:S::2600 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_A2_L		3 L:S::750 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B0_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B0_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
15B4> 12B4<> SYSCLK_DDRCLK_B0	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
12B4<> 15B3> SYSCLK_DDRCLK_B0_L	SYSCLK_DDRCLKB0:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_B1_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B1_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
15D6<> 12A4<> SYSCLK_DDRCLK_B1	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
15C6<> 12A4<> SYSCLK_DDRCLK_B1_L	SYSCLK_DDRCLKB1:G:L:S:0 MIL:100 MIL	3 L:S::3200 MIL	200	8 MIL SPACING			167 MHZ
12B6<> SYSCLK_DDRCLK_B2_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
12B6<> SYSCLK_DDRCLK_B2_L_UF		I:S:500 MIL:850 MIL	8 MIL SPACING	270			167 MHZ
15A6<> 12A4<> SYSCLK_DDRCLK_B2	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
15A6<> 12A4<> SYSCLK_DDRCLK_B2_L	SYSCLK_DDRCLKB2:G:L:S:0 MIL:100 MIL	3 L:S::3500 MIL	200	8 MIL SPACING			167 MHZ
28A6< INT_REF_CLK_IN_PD		8 L:S::2500 MIL	10 MIL SPACING	270			66.56 MHZ
31C6< 31B7< 31B6< 30D4<> 30C4<> 30C2<> 30C1<> 30B2<> PCI_AD<31..0>	MIN_DAISSY_CHAIN	6 L:S:6000:8000	500				33 MHZ
59C3> 59B3> 32B6<> 32B4<> 32B2<> 32B0<> PCI_CBE<3..0>	MIN_DAISSY_CHAIN	6 L:S:6000:8000	500				33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_FRAME_L	MIN_DAISSY_CHAIN	L:S:6000 MIL:8000 MIL	500				33 MHZ

DIGITAL SIGNAL CONSTRAINTS

SIGNAL CONSTRAINTS

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	D	051-6569	A
SCALE	SHT		OF
NONE	53		69

D

D

C

C

B

B

A

A

SIG_NAME	RATSNEST_SCHEDULE	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	DIFFERENTIAL_PAIR	FUNC_TEST	PULSE_PARAM
32B6<> 31B7< 30C5<> 30B7< PCI_IRDY_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_TRDY_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_DEVSEL_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> 30B7< PCI_STOP_L	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
59A5> 32B6<> 31B7< 30C5<> PCI_PAR	MIN DAISY_CHAIN	16	S:6000	MIL:8000	M200					33 MHZ
30D5<> CLK33M_PCI_SLOTB_UF			B:S:600	MIL:10D0	M200		450			33 MHZ
30D5<> CLK33M_PCI_SLOTC_UF			B:S:600	MIL:12D0	M200		450			33 MHZ
30D5<> CLK33M_PCI_SLOTD_UF			B:S:600	MIL:10D0	M200		450			33 MHZ
59A5> 31C2<> 30D7< CLK33M_PCI_SLOTB			I:S:3000	MIL:4000	M200	10 MIL SPACING	450			33 MHZ
30C5<> INT_PCI_FB_OUT			4	L:S::1000	MIL 200		450			33 MHZ
30D8< PCI_FBO_PLUS2			4	L:S::200	MIL 200		450			33 MHZ
30C8< PCI_FB_PLUS4			I4:S:1900	MIL:2000	MIL		450			33 MHZ
30C8< PCI_FBI_PLUS2			I4:S:1900	MIL:2000	M200		450			33 MHZ
30C7< PCI_FBI_EQUAL			I4:S:2000	MIL:3000	M200		450			33 MHZ
30C7< PCI_FB_PLUS6			I4:S:5900	MIL:6000	MIL		450			33 MHZ
30C5< INT_PCI_FB_IN			4	L:S::1080	MIL 200		450			33 MHZ
31C6< 31C3<> 31C2<> 31B7< 31B6< 31B3<> 31B2<> PCIT_AD<31..0>			3	L:S::1000						33 MHZ
59A5> 31C3<> 31B6< 31B2<> PCIT_CBE<31..0>			3	L:S::1000						33 MHZ
31C2<> 31B6< PCIT_FRAME_L			3	L:S::1000	MIL					33 MHZ
59B5> 31C3<> 31B6< PCIT_IRDY_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_TRDY_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_DEVSEL_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_STOP_L			3	L:S::1000	MIL					33 MHZ
31C2<> 31B6< PCIT_PAR			3	L:S::1000	MIL					33 MHZ
17D8< 17C8< 16C4<> AGP_AD<0..15>	AGP_GROUP0:G:L:S:0:280	5	L:S:4500							266 MHZ
17C8< 16B4<> AGP_CBE<0..1>	AGP_GROUP0:G:L:S:0:330	5	L:S:4500							266 MHZ
17B8< 16B3< 16A4<> AGP_AD_STB<0>	AGP_GROUP0:G:L:S:0 MIL:330	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP0			133 MHZ
17B8< 16D1< 16A4<> AGP_AD_STB_L<0>	AGP_GROUP0:G:L:S:0 MIL:330	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP0			133 MHZ
17C8< 16C4<> 16B4<> AGP_AD<16..31>	AGP_GROUP0:G:L:S:0:280	5	L:S:4500							266 MHZ
17C8< 16B4<> AGP_CBE<2..3>	AGP_GROUP0:G:L:S:0:280	5	L:S:4500							266 MHZ
17B8< 16B3< 16A4<> AGP_AD_STB<1>	AGP_GROUP0:G:L:S:0 MIL:280	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP1			133 MHZ
17B8< 16D1< 16A4<> AGP_AD_STB_L<1>	AGP_GROUP0:G:L:S:0 MIL:330	MIL	L:S:4400	MIL 200	8 MIL SPACING	500	AGP_ADSTBDP1			133 MHZ
17B8< 16C3< 16B4<> AGP_FRAME_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16C3< 16B4<> AGP_IRDY_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_TRDY_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16C3< 16B4<> AGP_DEVSEL_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_STOP_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B4<> 16B3< AGP_PAR			I:S:4000	MIL:4500	MIL					66 MHZ
17A8< 16C1< 16B4<> 16B4<> 16B1< 16A4<> AGP_SBA<0..7>			5	L:S:4000:4500						AGP_SBSTBB
17B8< 16B3< 16A4<> AGP_SB_STB	AGP_GROUP99:G:L:S:0 MIL:200	MIL	L:S:4500	MIL						AGP_SBSTBB
17A8< 16D1< 16A4<> AGP_SB_STB_L	AGP_GROUP99:G:L:S:0 MIL:200	MIL	L:S:4500	MIL						AGP_SBSTBB
17B6< 16B1< 16A4<> AGP_ST<0..2>			5	L:S:4500:5000						
17B8< 16B3< 16A4<> AGP_PIPE_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B8< 16B3< 16A4<> AGP_RBF_L			I:S:4000	MIL:4500	MIL					66 MHZ
17B6<> 16C4<> 16C3< AGP_REQ_L			I:S:4500	MIL:5000	MIL					66 MHZ
17B6< 16C4<> 16C3< AGP_GNT_L			I:S:4500	MIL:5000	MIL					66 MHZ
17B8< 16B1< 16A6<> AGP_WBF_L			I:S:4000	MIL:4500	MIL					66 MHZ
17A8> 16D3< 16D1< 16C6<> AGP_BUSY_L			I:S:4500	MIL:5000	MIL					66 MHZ
17A8< 16D3< 16C6<> STOP_AGP_L			I:S:4500	MIL:5000	MIL					66 MHZ
17D7<> 17D6<> 17C6<> GPU_AGP_AD<0..15>	GPU_AGP_GROUP0:G:L:S:0:1003		L:S:600							266 MHZ
17C6<> GPU_AGP_CBE<0..1>	GPU_AGP_GROUP0:G:L:S:0:1003		L:S:600							266 MHZ
AGP_AD_STB_GPU_AGP<0>	GPU_AGP_STB0:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP0			133 MHZ
AGP_AD_STB_L_GPU_AGP<0>	GPU_AGP_STB0:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP0			133 MHZ
17C6<> GPU_AGP_AD<16..31>	GPU_AGP_GROUP1:G:L:S:0:1003		L:S:600							266 MHZ
17C6<> GPU_AGP_CBE<2..3>	GPU_AGP_GROUP1:G:L:S:0:1003		L:S:600							266 MHZ
AGP_AD_STB_GPU_AGP<1>	GPU_AGP_STB1:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP1			133 MHZ
AGP_AD_STB_L_GPU_AGP<1>	GPU_AGP_STB1:G:L:S:0 MIL:50	MIL	L:S:800	MIL	8 MIL SPACING	500	GPU_ADSTBDP1			133 MHZ
17B6<> GPU_AGP_FRAME_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_IRDY_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_TRDY_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_DEVSEL_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_STOP_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_PAR			I:S:300	MIL:600	MIL					66 MHZ
17A6<> GPU_AGP_SBA<0..7>			3	L:S:300:600						GPU_SBSTBB
17B6<> GPU_AGP_SB_STB	GPU_AGP_SBSTB:G:L:S:0 MIL:150	MIL	I:S:300	MIL:600	MIL					GPU_SBSTBB
17A6<> GPU_AGP_SB_STB_L	GPU_AGP_SBSTB:G:L:S:0 MIL:150	MIL	I:S:300	MIL:600	MIL					GPU_SBSTBB
17B6<> GPU_AGP_PIPE_L			I:S:300	MIL:600	MIL					66 MHZ
17B6<> GPU_AGP_RBF_L			I:S:300	MIL:600	MIL					66 MHZ
16C6<> CLK66M_GPU_UF			I:S:1000	MIL:1100	MIL	10 MIL SPACING	250			66 MHZ
17C6< 16D8< CLK66M_GPU_AGP			I4:S:3700	MIL:3900	M200	10 MIL SPACING	250			66 MHZ
16C6<> INT_AGP_FB_OUT			I4:S:1400	MIL:1500	M200		250			66 MHZ
16B7< AGP_FBO_EQUAL			B:S:900	MIL:10B0	M200		250			66 MHZ
16B8< AGP_FB_PLUS2			I4:S:1900	MIL:2000	MIL		250			66 MHZ
16C7< AGP_FBI_EQUAL			4	L:S::200	MIL 200		250			66 MHZ
16C6< INT_AGP_FB_IN			4	L:S::1200	MIL 200		250			66 MHZ
30C5<> 30A7< 16D7< INT_ROM_OVERLAY_PU			I:S:600	MIL:800	MIL	10 MIL SPACING	250			66 MHZ
59A7> 56B3> 16C7< 9B4< 8A2< INT_ANALYZER_CLK			3	L:S::2800	MIL	8 MIL SPACING	250			166 MHZ
32A6< 30D7< CLK33M_PCI_SLOTD			I4:S:3000	MIL:3500	M200	8 MIL SPACING	250			33 MHZ

SIGNAL CONSTRAINTS

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	NONE	D 051-6569	A
	SCALE	SHT	OF
		54	69

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX EXPOSED LENGTH	PULSE PARAM	RATSNEST_SCHEDULE
	FBD<0..63>	GPU_FBDDATA_A:G:L:S:0:225		L:S::800				300 MHZ	18E8<> 18F8<> 18G8<> 19C5< 19C8< 19D5< 19D8<
	RFBD<0..63>	RAM_FBDDATA_A:G:L:S:0:300		L:S::1000				300 MHZ	19C4< 19C7< 19D4< 19D7< 20B1<> 20B5<> 20C1<> 20C5<>
	FBDQM<0..7>	GPU_FBDQM_A:G:L:S:0:200		L:S::800				300 MHZ	18D8< 18G3<
	RFBDQM<0..7>	RAM_FBDQM_A:G:L:S:0:200		L:S::1000				300 MHZ	18G2< 20C2< 20C6<
	FBA<0..12>	GPU_FBADDR_A:G:L:S:0:200		L:S::700				300 MHZ	18C8< 18D8< 18E3< 18F3<
	RFBA<0..12>	RAM_FBADDR_A:G:L:S:0:330		L:S::2400	2350			300 MHZ	18E2<> 18F2<> 20C2< 20C6< 20D2< 20D6<
	FBABA<0..1>	GPU_FBADDR_A:G:L:S:0:200		L:S::600				300 MHZ	18C8<> 18E3<
	RFBABA<0..1>	RAM_FBADDR_A:G:L:S:0:330		L:S::2400	50			300 MHZ	18E2<> 20C2< 20C6<
	FBARAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18G3<
	FBACAS_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18G3<
	FBARE_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18F3<
	FBACSO_L	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL						300 MHZ	18C8< 18F3<
	FBACKE	GPU_FBCNTL_A:G:L:S:0 MIL:200 MTS::400 MIL			100			300 MHZ	18D3< 18D7<>
	RFBARAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18G2<> 20B2< 20B6<
	RFBACAS_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18G2<> 20B2< 20B6<
	RFBAWE_L	RAM_FBCNTL_A:G:L:S:0 MIL:500 MTS::2700 MIL			50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACSO_L	RAM_FBCNTL_A:G:L:S:0 MIL:350 MTS::2700 MIL			50			300 MHZ	18F2<> 20B2< 20B6<
	RFBACKE	RAM_FBCNTL_A:G:L:S:0 MIL:500 MTS::2700 MIL			50			300 MHZ	18D2<> 20C2< 20C6<
	FBDQS<0..7>	GPU_FBDQS_A:G:L:S:0:100		L:S::350				300 MHZ	18C7< 19A8<
	FBDOSTERM<0..7>	FB_DQSTERM_A:G:L:S:0:50		L:S::1500		10 MIL SPACING		300 MHZ	19A7<
	RFBDQS<0..7>	RAM_FBDQS_A:G:L:S:0:55		L:S::150		10 MIL SPACING		300 MHZ	19A6< 20C2<> 20C6<>
	FBACLK0	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19C3<
	FBACLK0_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19C3<
	FBACLK1	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19D3<
	FBACLK1_L	GPU_FBCLK_A:G:L:S:0 MIL:50 MIL:S::150 MIL					200	300 MHZ	18D7< 19D3<
	RFBACLK1	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL:S::2500 MIL					200	300 MHZ	19D1< 20C2<
	RFBACLK1_L	RAM_FBCLK_A:G:L:S:0 MIL:80 MIL:S::2500 MIL					200	300 MHZ	19D1< 20C2<
	RFBACLK0	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL:S::2500 MIL					200	300 MHZ	19C1< 20C6<
	RFBACLK0_L	RAM_FBCLK_A:G:L:S:0 MIL:70 MIL:S::2500 MIL					200	300 MHZ	19C1< 20C6<
	FBD<64..127>	GPU_FBDDATA_B:G:L:S:0:225		L:S::800				300 MHZ	18E5<> 18F5<> 18G5<> 19B5< 19B8< 19C5< 19C8<
	RFBD<64..127>	RAM_FBDDATA_B:G:L:S:0:325		L:S::1000				300 MHZ	19B4< 19B7< 19C4< 19C7< 21B1<> 21B5<> 21C1<> 21C5<>
	FBDQM<8..15>	GPU_FBDQM_B:G:L:S:0:120		L:S::800				300 MHZ	18C3< 18D3< 18D5<
	RFBDQM<8..15>	RAM_FBDQM_B:G:L:S:0:120		L:S::1000				300 MHZ	18C2< 18D2< 21C2< 21C6<
	FBBAA<0..12>	GPU_FBADDR_B:G:L:S:0:220		L:S::600				300 MHZ	18A3< 18B3< 18C3< 18C5<> 18D5<>
	RFBBAA<0..12>	RAM_FBADDR_B:G:L:S:0:370		L:S::2400	50			300 MHZ	18B2<> 18C2<> 21C2< 21C6< 21D2< 21D6<
	FBBBA<0..1>	GPU_FBADDR_B:G:L:S:0:220		L:S::600				300 MHZ	18A3< 18C5<>
	RFBBBA<0..1>	RAM_FBADDR_B:G:L:S:0:370		L:S::2400	50			300 MHZ	18A2<> 21C2< 21C6<
	FBBRAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBRAS_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBWE_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBWE_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18D4<>
	FBBCSO_L	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL						300 MHZ	18C3< 18C4<>
	FBBCKE	GPU_FBCNTL_B:G:L:S:0 MIL:120 MTS::400 MIL			100			300 MHZ	18A3< 18C4<>
	RFBBRAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBRAS_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBWE_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCSO_L	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18C2<> 21B2< 21B6<
	RFBBCKE	RAM_FBCNTL_B:G:L:S:0 MIL:2000 MTS::3500 MIL			3550			300 MHZ	18A2<> 21C2< 21C6<
	FBDQS<8..15>	GPU_FBDQS_B:G:L:S:0:190		L:S::350				300 MHZ	18D4<> 19A5<
	FBDOSTERM<8..15>	FB_FBDQSTERM_B:G:L:S:0:60		L:S::1500		10 MIL SPACING		300 MHZ	19A4<
	RFBDQS<8..15>	RAM_FBDQS_B:G:L:S:0:59		L:S::150		10 MIL SPACING		300 MHZ	19A3< 21C2<> 21C6<>
	FBBCLK0	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19B3<
	FBBCLK0_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19B3<
	FBBCLK1	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19C3<
	FBBCLK1_L	GPU_FBCLK_B:G:L:S:0 MIL:50 MIL L:S::150 MIL					200	300 MHZ	18C5<> 19B3<
	RFBBCLK1	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19C1< 21C2<
	RFBBCLK1_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19B1< 21C2<
	RFBBCLK0	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19B1< 21C6<
	RFBBCLK0_L	RAM_FBCLK_B:G:L:S:0 MIL:90 MIL L:S::2500 MIL					200	300 MHZ	19B1< 21C6<

SIGNAL CONSTRAINTS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6569	A
SCALE	SHEET		OF
NONE	55		69

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MIN_LENGTH	PROPAGATION_DELAY	MIN_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	MAX_EXPOSED_LENGTH	
MAXBUS	CPU_ADDR<0..31>	CPU_ADDR_GROUP:G:L:S:0	1500	250				166 MHZ		4B7<> 4C7<> 8B4<> 8B5<> 8B7<> 8B8<> 8C4<> 8C5<> 8C7<> 8C8<>
	CPU_DATA<0..63>	CPU_DATA_GROUP:G:L:S:0	1500	1550				166 MHZ		8C3<> 9D3<> 9D5<> 9D8<>
	CPU BR L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		5A4<> 5B4<> 5C4<> 5D4<> 6C4< 8C4<> 8C4< 8C5<> 8C7<> 8C7< 8C8<>
	CPU BG L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		8D4<> 8D5<> 8D7<> 8D8<> 9A7< 9B1<> 9B7< 9C1<> 9C5< 9C8< 9D1<>
	CPU TS L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4D7<> 7C7< 8B4<> 9D3<>
	CPU TT<0..4>	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4D7<> 7C7< 8B7<> 9D3<>
	CPU TBST L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4B7<> 7A7< 8B4<> 8B5<> 9B3<>
	CPU TSIZ<0..2>	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4B7<> 7B7< 8B4<> 9B3<>
	CPU ARTRY L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4B7<> 8B5<> 8B7< 9B3<>
	CPU AACK L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4A7<> 7C7< 8B8<> 9B3<>
	CPU GBL L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4A7< 7B7< 8B5<> 9B3<>
	CPU INT_GBL L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4B8<> 8B5<>
	CPU CI L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4B8< 7B7< 9C3<>
	CPU HIT L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4A7<> 7A7< 8C5<> 9C3<>
	CPU DBG L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4A7<> 7C7< 8B8<> 9B3<>
	CPU DRDY L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C3< 7B7< 8B8<> 9B1<>
	CPU WT L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C2< 7B7< 8B5<> 9B1<>
	CPU DRDY L UP	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4B7<> 7A7< 8B5<> 9B3<>
	CPU DTI<0..2>	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C3<>
	CPU TA L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C3< 8B4<> 8B7<> 9A1<>
	CPU TEA L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C3< 7C7< 8C4<> 9A1<>
	CPU OREQ L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C3< 7B7< 8B5<> 9A1<>
	CPU OACK L	CPU_CNTL_GROUP:G:L:S:0	1500	250	10 MIL SPACING			166 MHZ		4C3<> 7D5< 8B7<> 9B3<>
	SYSCLK_CPU UP			150		10 MIL SPACING		166 MHZ	315	4C3< 8B4<> 9B3<>
	SYSCLK_CPU			2200	200	10 MIL SPACING		166 MHZ	315	9A3<>
	INT_CPU_FB_OUT			1000	200			166 MHZ	315	4D2< 9A4<
	CPU_FBO_PLUS1			200	200			166 MHZ	315	9B3<>
	CPU_FBI_PLUS1			1400	1500	200		166 MHZ	315	9A5<
	CPU_FB_MINUS3			900	1000	200		166 MHZ	315	9A5<
	INT_CPU_FB_IN			1000	200			166 MHZ	315	9A4<
	CPU_FB_PLUS2			900	1000			166 MHZ	315	9B3<
	CPU_FB_PLUS3			2900	3000			166 MHZ	315	9A5<
	INT_ANALYZER_CLK			300				166 MHZ		9A4<
	SYSCLK_LA			2000				166 MHZ		8A2< 9B4< 16C7< 54A7< 59A7>
	INT_CLOCK_OUT			3000				166 MHZ		8A2< 8D8<>
USB2_XT1			1000	100	10 MIL SPACING		30 MHZ		DIFFERENTIAL_PAIR	
USB2_XT2_B			1000	100	10 MIL SPACING		30 MHZ		32C4<	
USB2_XT2			100	100	10 MIL SPACING		30 MHZ		32C4<>	
USB2_RREF			100						32B4<>	
USB2_RSDAM	USB2_RSDA:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ		32C4<>	
USB2_RSDAP	USB2_RSDA:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ		32C4<>	
USB2_RSDBM	USB2_RSDB:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ		32C4<>	
USB2_RSDBP	USB2_RSDB:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ		32C4<>	
USB2_RSDCM	USB2_RSDB:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ		32C4<>	
USB2_RSDCP	USB2_RSDB:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ		32C4<>	
USB2_DAN_F	USB2_DMA:G:L:S:0	0.04MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_DMA_DP	MIN DAISY_CHAIN	
USB2_DAP_F	USB2_DMA:G:L:S:0	0.04MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_DMA_DP	MIN DAISY_CHAIN	
USB2_DBN_F	USB2_DMB:G:L:S:0	0.04MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_DMB_DP	MIN DAISY_CHAIN	
USB2_DBP_F	USB2_DMB:G:L:S:0	0.04MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_DMB_DP	MIN DAISY_CHAIN	
USB2_DCN_F	USB2_DMC:G:L:S:0	0.04MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_DMC_DP	MIN DAISY_CHAIN	
USB2_DCP_F	USB2_DMC:G:L:S:0	0.04MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_DMC_DP	MIN DAISY_CHAIN	
USBT_DAN_F	USB2_DMAT:G:L:S:0	0.04MIL	30	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMAT_DP	MIN DAISY_CHAIN	
USBT_DAP_F	USB2_DMAT:G:L:S:0	0.04MIL	30	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMAT_DP	MIN DAISY_CHAIN	
USBT_DBN_F	USB2_DMBT:G:L:S:0	0.04MIL	30	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMBT_DP	MIN DAISY_CHAIN	
USBT_DBP_F	USB2_DMBT:G:L:S:0	0.04MIL	30	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMBT_DP	MIN DAISY_CHAIN	
USBT_DCN_F	USB2_DMCT:G:L:S:0	0.04MIL	30	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMCT_DP	MIN DAISY_CHAIN	
USBT_DCP_F	USB2_DMCT:G:L:S:0	0.04MIL	30	2000	8 MIL SPACING	3.5	480 MHZ	USB2_DMCT_DP	MIN DAISY_CHAIN	
USB_DAN_CON	USB2_CONA:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_CONA_DP	MIN DAISY_CHAIN	
USB_DAP_CON	USB2_CONA:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_CONA_DP	MIN DAISY_CHAIN	
USB_DBN_CON	USB2_CONB:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_CONB_DP	MIN DAISY_CHAIN	
USB_DBP_CON	USB2_CONB:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_CONB_DP	MIN DAISY_CHAIN	
USB_DCN_CON	USB2_CONC:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_CONC_DP	MIN DAISY_CHAIN	
USB_DCP_CON	USB2_CONC:G:L:S:0	0.02MIL	30	500	8 MIL SPACING	3.5	480 MHZ	USB2_CONC_DP	MIN DAISY_CHAIN	

SIGNAL CONSTRAINTS

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	D	051-6569	A
SCALE	SHT		OF
NONE	56		69

DIGITAL SIGNALS

DIGITAL SIGNALS

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM
NEW	VSYNC*	3		L:S::1000 MIL			22C5<>
STUFF	ANALOG VSYNC*	4		L:S::3500 MIL			22D7< 25C6> 26B5< 59B7>
HERE	HSYNC*	3		L:S::1000 MIL			22C5<>
	ANALOG HSYNC*	5		L:S::3500 MIL			22D7< 25D6> 26B5< 59B7>
	ANALOG BLU	4		L:S::4000 MIL	10 MIL SPACING	5.8	22C7<> 25C6<
	ANALOG GRN	4		L:S::4000 MIL	10 MIL SPACING	5.8	22C7<> 25C6<
	ANALOG RED	4		L:S::4000 MIL	10 MIL SPACING	5.8	22C7<> 25C6<
	FILT ANALOG RED	2		L:S::500 MIL	10 MIL SPACING	5.8	25C5< 59B7>
	FILT ANALOG GRN	2		L:S::500 MIL	10 MIL SPACING	5.8	25C5< 59B7>
	FILT ANALOG BLU	2		L:S::500 MIL	10 MIL SPACING	5.8	25C5< 59B7>
	DAC2RSET			L:S::1000 MIL	10 MIL SPACING		22C5<>
	DAC2VREF			L:S::1000 MIL	10 MIL SPACING		22C5<>
	NV11 XTALIN	4		L:S::1000 MIL	8 MIL SPACING		22B4<>
	NV11 XTALOUT	4		L:S::1000 MIL	8 MIL SPACING		22B4<>
	TCKP			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_CLK 24C4<>
	TCKM			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_CLK 24C3<>
	TD0P			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_D0 24C3<>
	TD0M			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_D0 24C4<>
	TD1P			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_D1 24C4<>
	TD1M			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_D1 24C3<>
	TD2P			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_D2 24C3<>
	TD2M			TMDSFILT:G:L:S:02MIL:110 MIL	110	8 MIL SPACING	TMDSFILT_D2 24C4<>
	ENET LINK TX EN	4		L:S::1000 MIL			25 MHZ 34D6<>
	ENET LINK TX ER	4		L:S::1000 MIL			25 MHZ 34D6<>
	ENET LINK TXD<0..3>	4		L:S::1000 MIL			25 MHZ 34C6<>
	ENET PHY TX EN	4		L:S::5600 MIL			25 MHZ 34D7< 35C6<
	ENET PHY TX ER	4		L:S::5600 MIL			25 MHZ 34D7< 35C6<
	ENET PHY TXD<0..3>	4		L:S:4600:5600			25 MHZ 34C7< 35C6>
	CLKENET LINK TX	4		L:S:4600 MIL:5600 MIL			25 MHZ 34D7< 35C8<
	CLKENET PHY TX	4		L:S::1000 MIL			25 MHZ 35C6<>
	CLKENET LINK RX	4		L:S:4600 MIL:5600 MIL			25 MHZ 34C7< 35C8<
	CLKENET PHY RX	4		L:S::1000 MIL			25 MHZ 35C6<>
	ENET PHY RXD<0..3>	4		L:S::1000 MIL			25 MHZ 35B6<> 35C6<>
	ENET PHY RX DV	4		L:S::1000 MIL			25 MHZ 35B6<>
	ENET PHY RX ER	4		L:S::1000 MIL			25 MHZ 35B6<>
	ENET PHY CRS	4		L:S::1000 MIL			25 MHZ 35B6<>
	ENET PHY COL	4		L:S::1000 MIL			25 MHZ 35B6<>
	ENET LINK RXD<0..3>	4		L:S:4600:5600			25 MHZ 34C7< 35B8< 35C8<
	ENET CRS	4		L:S:4600 MIL:5600 MIL			25 MHZ 34C7< 35B8<
	ENET COL	4		L:S:4600 MIL:5600 MIL			25 MHZ 34B7< 35B8<
	ENET RX DV	4		L:S:4600 MIL:5600 MIL			25 MHZ 34C7< 35B8<
	ENET RX ER	4		L:S:4600 MIL:5600 MIL			25 MHZ 34C7< 35B8<
	CLK25M ENET XIN	3		L:S::1000 MIL	8 MIL SPACING		25 MHZ 35B6<
	CLK25M ENET XOUT	3		L:S::1000 MIL	8 MIL SPACING		25 MHZ 35B6<>
	ENET TDP			ETHTD:G:L:S:0 MBL:70 MIB::4000 MIL:50	10 MIL SPACING	ETH TXD	100 MHZ 35C3<>
	ENET TDN			ETHTD:G:L:S:0 MBL:70 MIB::4000 MIL:50	10 MIL SPACING	ETH TXD	100 MHZ 35C3<>
	ENET RDP			ETHRD:G:L:S:0 MBL:70 MIB::4000 MIL:50	10 MIL SPACING	ETH RXD	100 MHZ 35C3<>
	ENET RDN			ETHRD:G:L:S:0 MBL:70 MIB::4000 MIL:50	10 MIL SPACING	ETH RXD	100 MHZ 35C3<>
	RJ45 TXP			RJTXD:G:L:S:0 MBL:70 MIB::750 MIL	2KV ISO	RJ45_TXD	100 MHZ 35C1<>
	RJ45 TXN			RJTXD:G:L:S:0 MBL:70 MIB::750 MIL	2KV ISO	RJ45_TXD	100 MHZ 35C1<>
	RJ45 RXP			RJRXD:G:L:S:0 MBL:70 MIB::750 MIL	2KV ISO	RJ45_RXD	100 MHZ 35C1<>
	RJ45 RXN			RJRXD:G:L:S:0 MBL:70 MIB::750 MIL	2KV ISO	RJ45_RXD	100 MHZ 35C1<>
	RJ45 TREF				2KV ISO		35C2<>
	RJ45 RREF				2KV ISO		35C2<>
	RJ45 4 5				2KV ISO		35C1<>
	RJ45 7 8				2KV ISO		35C1<>
	RJ45 F TREF				2KV ISO		35B2<
	FW LINK DATA<0..7>	4		L:S::1000 MIL			34C4<>
	FW LINK CNTL<0..1>	4		L:S::1000 MIL			49.152 MHZ 34C4<>
	FW LINK LREQ	4		L:S::1000 MIL			49.152 MHZ 34C4<>
	FW SCLK	4		L:S:3500 MIL:4500 MIL			49.152 MHZ 34C5<> 36C8<
	FW D<0..7>	4		L:S:3700 MIL:4700 MIL			49.152 MHZ 34C3< 36C8<
	FW CNTL0	4		L:S:3700 MIL:4700 MIL			49.152 MHZ 34C3< 36C8<
	FW CNTL1	4		L:S:3700 MIL:4700 MIL			49.152 MHZ 34C3< 36C8<
	FW LREQ	4		L:S:3700 MIL:4700 MIL			49.152 MHZ 34C3< 36C8<
	FW PHY SCLK	4		L:S:500 MIL			49.152 MHZ 36C7<>
	FW PHY CNTL0	4		L:S:1000 MIL			49.152 MHZ 36C7<>
	FW PHY CNTL1	4		L:S:1000 MIL			49.152 MHZ 36C7<>
	FW PHY D<0..7>	4		L:S:1000 MIL			49.152 MHZ 36B7<> 36C7<>
	FW XT	3		L:S:1000 MIL	8 MIL SPACING		24.576 MHZ 36C6<
	FW XO	3		L:S:1000 MIL	8 MIL SPACING		24.576 MHZ 36C6<>
	FW BIAS1						36C5<>
	FW BIAS2						36C5<>
	FW TPA1P			FWTPA1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPA1	400 MHZ 36C5<>
	FW TPA1N			FWTPA1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPA1	400 MHZ 36C5<>
	FW TPB1P			FWTPB1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPB1	400 MHZ 36C5<>
	FW TPB1N			FWTPB1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPB1	400 MHZ 36C5<>
	FW TPA2P			FWTPA2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPA2	400 MHZ 36C5<>
	FW TPA2N			FWTPA2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPA2	400 MHZ 36C5<>
	FW TPB2P			FWTPB2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPB2	400 MHZ 36C5<>
	FW TPB2N			FWTPB2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPB2	400 MHZ 36C5<>
	FW TPO1P			FWTPO1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPO1	400 MHZ 36A8<> 36D1<>
	FW TPO1N			FWTPO1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPO1	400 MHZ 36A8<> 36D1<>
	FW TPL1P			FWTPL1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPL1	400 MHZ 36A8<> 36D1<>
	FW TPL1N			FWTPL1:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPL1	400 MHZ 36A8<> 36D1<>
	FW TPO2P			FWTPO2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPO2	400 MHZ 36A8<> 36C1<>
	FW TPO2N			FWTPO2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPO2	400 MHZ 36A8<> 36C1<>
	FW TPL2P			FWTPL2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPL2	400 MHZ 36A8<> 36C1<>
	FW TPL2N			FWTPL2:G:L:S:0 MIL:50.358H:1220 MFD00		FW TPL2	400 MHZ 36A8<> 36C1<>

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM
NEW	TMDS CKP	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_CLK 23D1< 24B7<> 27C2< 59A7>
STUFF	TMDS CKM	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_CLK 23D1< 24A7<> 27C2< 59A7>
HERE	TMDS D0P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_D0 23D1< 24B7<> 27C2< 59A7>
	TMDS D0M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_D0 23D1< 24B7<> 27C2< 59A7>
	TMDS D1P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_D1 23D1< 24C7<> 27C2< 59B7>
	TMDS D1M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_D1 23D1< 24C7<> 27C2< 59B7>
	TMDS D2P	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_D2 23D1< 24D7<> 27C2< 59B7>
	TMDS D2M	TMDS:G:L:S:0 MIL:120 MIL	3	70	8 MIL SPACING		TMDS_D2 23D1< 24D7<> 27C2< 59B7>
	GPU TMDS CKP	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_CLK 23C2< 23D3<>
	GPU TMDS CKM	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_CLK 23C2< 23D3<>
	GPU TMDS D0P	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_D0 23C2< 23D3<>
	GPU TMDS D0M	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_D0 23C2< 23D3<>
	GPU TMDS D1P	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_D1 23C2< 23D3<>
	GPU TMDS D1M	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_D1 23C2< 23D3<>
	GPU TMDS D2P	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_D2 23C2< 23D3<>
	GPU TMDS D2M	GTMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		G_TMDS_D2 23C2< 23D3<>
	SI TMDS CKP	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_CLK 27C3<>
	SI TMDS CKM	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_CLK 27C3<>
	SI TMDS D0P	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_D0 27C3<>
	SI TMDS D0M	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_D0 27C3<>
	SI TMDS D1P	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_D1 27C3<>
	SI TMDS D1M	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_D1 27C3<>
	SI TMDS D2P	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_D2 27C3<>
	SI TMDS D2M	STMSD:G:L:S:0 MIL:120 MIL	3	50	8 MIL SPACING		S_TMDS_D2 27C3<>
	DVOD0	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22C5<> 27A8< 27C5<
	DVOD1	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22C5<> 27A8< 27C5<
	DVOD2	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22C5<> 26D1< 27C5<
	DVOD3	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 26D1< 27C5<
	DVOD4	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27C5<
	DVOD5	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27C5<
	DVOD6	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27C5<
	DVOD7	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27C5<
	DVOD8	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 26B1< 27C5<
	DVOD9	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27C5<
	DVOD10	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27B5<
	DVOD11	TMDS_XMIT:G:L:S:0 MIL:400 MIL		200			165MHZ 22B5<> 27A8< 27B5<

SIGNAL CONSTRAINTS

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APPLE COMPUTER INC.

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SCALE NONE SHEET 57 OF 69

DIGITAL SIGNALS (CONT'D)

GROUP	SIG_NAME	RELATIVE_PROPAGATION_DELAY	MAX_VIAS	PROPAGATION_DELAY	STUB_LENGTH	NET_SPACING_TYPE	MAX_EXPOSED_LENGTH	PULSE_PARAM		
CD DRIVE BUS	EIDE_RST_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 37D5<	
	EIDE_DMACK_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7<> 37D5<	
	EIDE_STOP			L:S:5500 MIL				33 MHZ	37A7> 37D5<	
	EIDE_HSTB_RDY			L:S:5500 MIL				33 MHZ	37A7> 37C5<	
	EIDE_DSTB_RDY			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 37C5<	
	EIDE_DATA<0..15>			L:S:3500:5500				33 MHZ	37A5< 37B5< 37B7<> 37C5<	
	CD_RESET_L			L:S:1000 MIL				33 MHZ	37D4< 38C6<>	
	CD_DMACK_L			L:S:4000 MIL				33 MHZ	37D4< 38C6<>	
	CD_STOP			L:S:5000 MIL				33 MHZ	37D4< 38C6<>	
	CD_HSTB_RDY			L:S:5000 MIL				33 MHZ	37C4< 38C6<>	
	CD_DSTB_RDY			L:S:1000 MIL				33 MHZ	37C4< 38C6<>	
	UATAD<0..15>			L:S:1000				33 MHZ	37A4< 37B4< 37C4< 38C6<>	
	CD_DMARQ			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_DMARQ			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<	
	UATAOIRO			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_INTRO			L:S:3500 MIL:5500 MIL				33 MHZ	37A7< 38C8<	
	CD_EIDE_ADDR<0..2>			L:S:1000				33 MHZ	38C6<>	
	EIDE_ADDR<0..2>			L:S:3500:5500				33 MHZ	37B7> 38A8< 38B8<	
	CD_CS1FX_L			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_CS1FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<	
	CD_CS3FX_L			L:S:1000 MIL				33 MHZ	38C6<>	
	EIDE_CS3FX_L			L:S:3500 MIL:5500 MIL				33 MHZ	37A7> 38B8<	
	HD DRIVE BUS	UIDE_RST_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DMACK_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DIOR_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C7<> 37D3<
		UIDE_DIOW_L	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C3< 37C7<>
		UIDE_IOCHRDY	HD_DATA:G:L:S:0		L:S:100 MIL:6000 MIL				100 MHZ	37C3< 37C7<>
		UIDE_DATA<0..15>	HD_DATA:G:L:S:0		L:S:100:6000				100 MHZ	37C3< 37C7<
		HD_RESET_L			L:S:1000 MIL				100 MHZ	37A3< 37B3< 37C3< 37C7<> 37D7<>
		HD_DMACK_L			L:S:1000 MIL				100 MHZ	37D1< 38C3<>
HD_DIOR_L				L:S:5500 MIL				100 MHZ	37D1< 38C3<>	
HD_DIOW_L				L:S:55000 MIL				100 MHZ	37C1< 38C3<>	
HD_IOCHRDY				L:S:1000 MIL				100 MHZ	37C1< 38C3<>	
HD_DMARQ				L:S:1000 MIL				100 MHZ	38C3<>	
UIDE_DMARQ		HD_DATA:G:L:S:0		L:S:5500 MIL:6000 MIL				100 MHZ	37C7<> 38C4<	
HD_INTRO				L:S:1000 MIL				100 MHZ	38C3<>	
UIDE_INTRO		HD_DATA:G:L:S:0		L:S:5500 MIL:6000 MIL				100 MHZ	37C7< 38C4<	
HD_UIDE_ADDR<0..2>				L:S:1000				100 MHZ	38C2<> 38C3<>	
UIDE_ADDR<0..2>		HD_DATA:G:L:S:0		L:S:100:6000				100 MHZ	37C7<> 38A4< 38B4<	
HD_UIDE_CS1FX_L				L:S:6000 MIL				100 MHZ	38C3<>	
UIDE_CS1FX_L		HD_DATA:G:L:S:0		L:S:5500 MIL				100 MHZ	37C7<> 38B4<	
HD_UIDE_CS3FX_L				L:S:6000 MIL				100 MHZ	38C2<>	
UIDE_CS3FX_L		HD_DATA:G:L:S:0		L:S:5500 MIL				100 MHZ	37C7<> 38B4<	
CLK_18M_INT_XOUT				L:S:1000 100		8 MIL SPACING		18.432 MHZ	58B5>	
CLK_18M_INT_XOUT				L:S:1000 100		8 MIL SPACING		18.432 MHZ	58B5>	
CLK_18M_INT_XOUT				L:S:200 50		8 MIL SPACING		18.432 MHZ	58B5>	
USB_DAP		USBA:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DAN		USBA:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DAP_F		USBA_F:G:L:S:0		MIL:500 MIL	100				28B2< 33B7<	
USB_DAN_F		USBA_F:G:L:S:0		MIL:500 MIL	100				28B2< 33B7<	
USB_DBP		USBB:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DBN		USBB:G:L:S:0		MIL:500 MIL					28A3< 28B3<>	
USB_DBP_F	USBB_F:G:L:S:0		MIL:500 MIL	100				28B2< 33C7<		
USB_DBN_F	USBB_F:G:L:S:0		MIL:500 MIL	100				28B2< 33C7<		
USB_DCP	USBC:G:L:S:0		MIL:500 MIL					28A3< 28B3<>		
USB_DCN	USBC:G:L:S:0		MIL:500 MIL					28A3< 28B3<>		
USB_DCP_F	USBC_F:G:L:S:0		MIL:500 MIL	100				28B2< 33D7<		
USB_DCN_F	USBC_F:G:L:S:0		MIL:500 MIL	100				28B2< 33D7<		
USB_DEP	USBE:G:L:S:0		MIL:500 MIL					28B3<>		
USB_DEN	USBE:G:L:S:0		MIL:500 MIL					28B3<>		
BT_USB_DP	USBE_F:G:L:S:0		MIL:500 MIL	100				28B2< 29D3<> 59B5>		
BT_USB_DM	USBE_F:G:L:S:0		MIL:500 MIL	100				28B2< 29D3<> 59B5>		
USB_DFP	USBF:G:L:S:0		MIL:500 MIL					28B3<>		
USB_DFN	USBF:G:L:S:0		MIL:500 MIL					28B3<>		
MODEM_USB_DP	USBF_F:G:L:S:0		MIL:500 MIL	100				28B2< 29C5<> 59B5>		
MODEM_USB_DM	USBF_F:G:L:S:0		MIL:500 MIL	100				28B2< 29C5<> 59B5>		
PMU_XO			L:S:1000 MDD		8 MIL SPACING		10 MHZ	44B5<		
PMU_XI			L:S:1000 MDD		8 MIL SPACING		10 MHZ	44B5<		
PMU_XT			L:S:300 MDD		8 MIL SPACING		10 MHZ	44A6<		
PMU_CLKOUT			L:S:1000 MDD		8 MIL SPACING		32.768 MHZ	44B4<>		
PMU_CLKIN			L:S:1000 MDD		8 MIL SPACING		32.768 MHZ	44B4<>		
PMU_CLKT			L:S:300 MDD		8 MIL SPACING		32.768 MHZ	44B2<>		
MICSHLD					10 MIL SPACING			29A5<> 43A8< 59A7>		
MICHIGH					10 MIL SPACING			29A5<> 43B8< 59A7>		
MICLOW					10 MIL SPACING			29A5<> 43A8< 59A7>		
KS_INT_SPKR+					10 MIL SPACING			29A3< 43D7< 59B7>		
KS_INT_SPKR-					10 MIL SPACING			29A3< 42B4< 43D7< 59B7>		

SIG_NAME	PROPAGATION_DELAY	REFERENCE_PARAM
T_UD_IDEDD_0	L:S:1000 MIL	100 MHZ 37C1< 38C3<>
T_UD_IDEDD_1	L:S:1000 MIL	100 MHZ 37C1< 38C3<>
T_UD_IDEDD_2	L:S:1000 MIL	100 MHZ 37C1< 38C3<>
T_UD_IDEDD_3	L:S:1000 MIL	100 MHZ 37C1< 38C3<>
T_UD_IDEDD_4	L:S:1000 MIL	100 MHZ 37B1< 38C3<>
T_UD_IDEDD_5	L:S:1000 MIL	100 MHZ 37B1< 38C3<>
T_UD_IDEDD_6	L:S:1000 MIL	100 MHZ 37B1< 38C3<>
T_UD_IDEDD_7	L:S:1000 MIL	100 MHZ 37B1< 38C3<>
T_UD_IDEDD_8	L:S:1000 MIL	100 MHZ 37B1< 38C2<>
T_UD_IDEDD_9	L:S:1000 MIL	100 MHZ 37B1< 38C2<>
T_UD_IDEDD_10	L:S:1000 MIL	100 MHZ 37B1< 38C2<>
T_UD_IDEDD_11	L:S:1000 MIL	100 MHZ 37B1< 38C2<>
T_UD_IDEDD_12	L:S:1000 MIL	100 MHZ 37B1< 38C2<>
T_UD_IDEDD_13	L:S:1000 MIL	100 MHZ 37A1< 38C2<>
T_UD_IDEDD_14	L:S:1000 MIL	100 MHZ 37A1< 38C2<>
T_UD_IDEDD_15	L:S:1000 MIL	100 MHZ 37A1< 38C2<>

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	D	051-6569	A
SCALE	SHT	OF	
NONE	58	69	

FUNC_TEST

FUNC_TEST

FUNC_TEST

D

D

C

C

B

B

A

A

52c4	+1_8V_MAIN	52c4
51b7< 51a7< 51a5< 50d5<	+12V_MAIN	51c3< 51d7<
45d7< 45d3< 45b4< 44d8<	+12V_SLEEP	50b4< 50c4<
49d7< 49d3< 49c4< 48b6<	+12V_SLEEPA	36d2< 36d4<
51d6< 51c2< 51a5< 50d5<	+5V_MAIN	29a8< 29a3<
	+5V_SLEEP	52c1< 52c1<
51c8< 51c5< 50d5< 46d6<	+2_5V_MAIN	52c4 51b4<
52c4 49b2< 30b3<	+3V_MAIN	52c4 46c7< 38c1<
42c8< 42b7< 42b5< 41a7<	CPU_VCORE_SLEEP	52c4 49b2< 30b3<
59b5> 52c6> 45d2< 8c1<	JTAG_ASIC_TCK	40d5< 39d4< 41a5<
35c4< 34b7< 8a4<	JTAG_ASIC_TDI	52c4 43c7<
34b7< 28c6< 8a4<	JTAG_ASIC_TDO	8c1< 8b7< 4d7< 4d3<
35b4< 8a4<	JTAG_ASIC_TMS	35c4< 34b7< 8a4<
35b4< 35a2< 34b7< 8a4<	JTAG_ASIC_TRST_L	34b7< 28c6< 8a4<
34b7< 8a4<	INT_TMDS_3V	35b4< 8a4<
52a6> 24c3<	+1_5V_AGP	35b4< 35a2< 34b7< 8a4<
17a4< 17a3< 16d7< 16c2<	FAN_12V_FILT	34b7< 8a4<
11a6< 10d6< 17d5<	+INTREPID_CORE_MAIN	52a6> 24c3<
52c3> 46b4< 17d5<	INTREPID_VSENSE	17a4< 17a3< 16d7< 16c2<
52b3> 29a5<	OVDD_ADJ	52c3> 46b4< 17d5<
47b2< 46b3< 11d3< 10d6<	CPU_CHKSTP_OUT_L	52b3> 29a5<
47c6<	CPU_CHKSTP_IN_L	47b2< 46b3< 11d3< 10d6<
8d5< 8a3< 7b5< 4b3<	CPU_HRESET_L	47c6<
7b5< 4b3<	JTAG_CPU_TCK	8d5< 8a3< 7b5< 4b3<
44d2< 44c2< 8a3< 7b3<	JTAG_CPU_TDI	7b5< 4b3<
8a3< 7d5< 4c3<	JTAG_CPU_TDO	44d2< 44c2< 8a3< 7b3<
8a3< 7a5< 4c3<	JTAG_CPU_TMS	8a3< 7d5< 4c3<
8a3< 4c3<	JTAG_CPU_TRST_L	8a3< 7a5< 4c3<
8a3< 7c5< 4c3<	+MAXBUS_SLEEP	8a3< 4c3<
8d1< 8a3< 7c7< 7c5< 7c3<	ROM_CS_L	8a3< 7c5< 4c3<
52c6> 46d4< 45d2< 44d2<	ROM_OE_L	8d1< 8a3< 7c7< 7c5< 7c3<
44d1< 44b7< 9d8< 9b7< 8d4<	ROM_RW_L	52c6> 46d4< 45d2< 44d2<
31b4< 30c6< 30b4<	DDC_VCC_3	44d1< 44b7< 9d8< 9b7< 8d4<
31b2< 30c6< 30b2<	DDC_VCC_5	31b4< 30c6< 30b4<
31b4< 30b6< 30b2<	SND_HP_SENSE_L	31b2< 30c6< 30b2<
52b6> 24b3<	ANALOG_HSYNC*	31b4< 30b6< 30b2<
52a6> 25c4<	ANALOG_VSYNC*	52b6> 24b3<
41a5< 28b5<	FILT_ANALOG_BLU	52a6> 25c4<
57d5> 26b5< 25d6< 22d7<	FILT_ANALOG_RED	41a5< 28b5<
57d5> 26b5< 25c6< 22d7<	FILT_ANALOG_GRN	57d5> 26b5< 25d6< 22d7<
57d5> 25c5<	GND	57d5> 26b5< 25c6< 22d7<
57d5> 25c5<	KS_INT_SPKR+	57d5> 25c5<
57d5> 25c5<	KS_INT_SPKR-	57d5> 25c5<
58a5> 43d7< 29a3<	TMDS_D2P	58a5> 43d7< 29a3<
58a5> 43d7< 42b4< 29a3<	TMDS_D2M	58a5> 43d7< 29a3<
57d2> 27c2< 24d7< 23d1<	TMDS_D1P	57d2> 27c2< 24d7< 23d1<
57d2> 27c2< 24d7< 23d1<	TMDS_D1M	57d2> 27c2< 24d7< 23d1<
57d2> 27c2< 24c7< 23d1<	TMDS_D0P	57d2> 27c2< 24d7< 23d1<
57d2> 27c2< 24b7< 23d1<	TMDS_D0M	57d2> 27c2< 24c7< 23d1<
57d2> 27c2< 24b7< 23d1<	TMDS_CKP	57d2> 27c2< 24b7< 23d1<
57d2> 27c2< 24a7< 23d1<	TMDS_CKM	57d2> 27c2< 24b7< 23d1<
29a5<	INV_CUR_HI_FILT	57d2> 27c2< 24a7< 23d1<
44d3< 44b8< 35b8< 32a6<	IO_RESET_L	29a5<
52b3> 29a5<	KS5VSD	44d3< 44b8< 35b8< 32a6<
39b1< 34b5< 29c7< 28d1<	INT_I2C_CLK2	52b3> 29a5<
39b1< 34b5< 29c7< 28d1<	INT_I2C_DATA2	39b1< 34b5< 29c7< 28d1<
56b3> 54a7< 16c7< 9b4< 8a2<	INT_ANALYZER_CLK	56b3> 54a7< 16c7< 9b4< 8a2<
29a5<	LAMP_STS_FILT	56b3> 54a7< 16c7< 9b4< 8a2<
29a5<	LCD_PWM_FILT	29a5<
29a5<	LED_5V_FILT	29a5<
52b3> 29a5<	LED_RET_FILT	52b3> 29a5<
52a3> 29a5<	MICSHLD	52b3> 29a5<
58a5> 43a8< 29a5<	MICHIGH	52a3> 29a5<
58a5> 43b8< 29a5<	MICLOW	58a5> 43a8< 29a5<
58a5> 43a8< 29a5<	COMM_RESET_L	58a5> 43b8< 29a5<
29d5< 28c5<	IIC_ADD	58a5> 43a8< 29a5<
29c6< 28c5<	ROM_WP_L	29d5< 28c5<
30b2<		29c6< 28c5<

29d7< 28d1< 28c5<	COMM_SHUTDOWN	29d7< 28d1< 28c5<
25c6< 23d7<	MON_DETECT	25c6< 23d7<
45c8< 45c7<	FLO_KNOWS_BEST	45c8< 45c7<
44c4< 29b2<	NMI_BUTTON*	44c4< 29b2<
59d5> 44c5< 44b1< 8a8<	PWR_SWITCH*	59d5> 44c5< 44b1< 8a8<
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	NC_RF_DISABLE_L	
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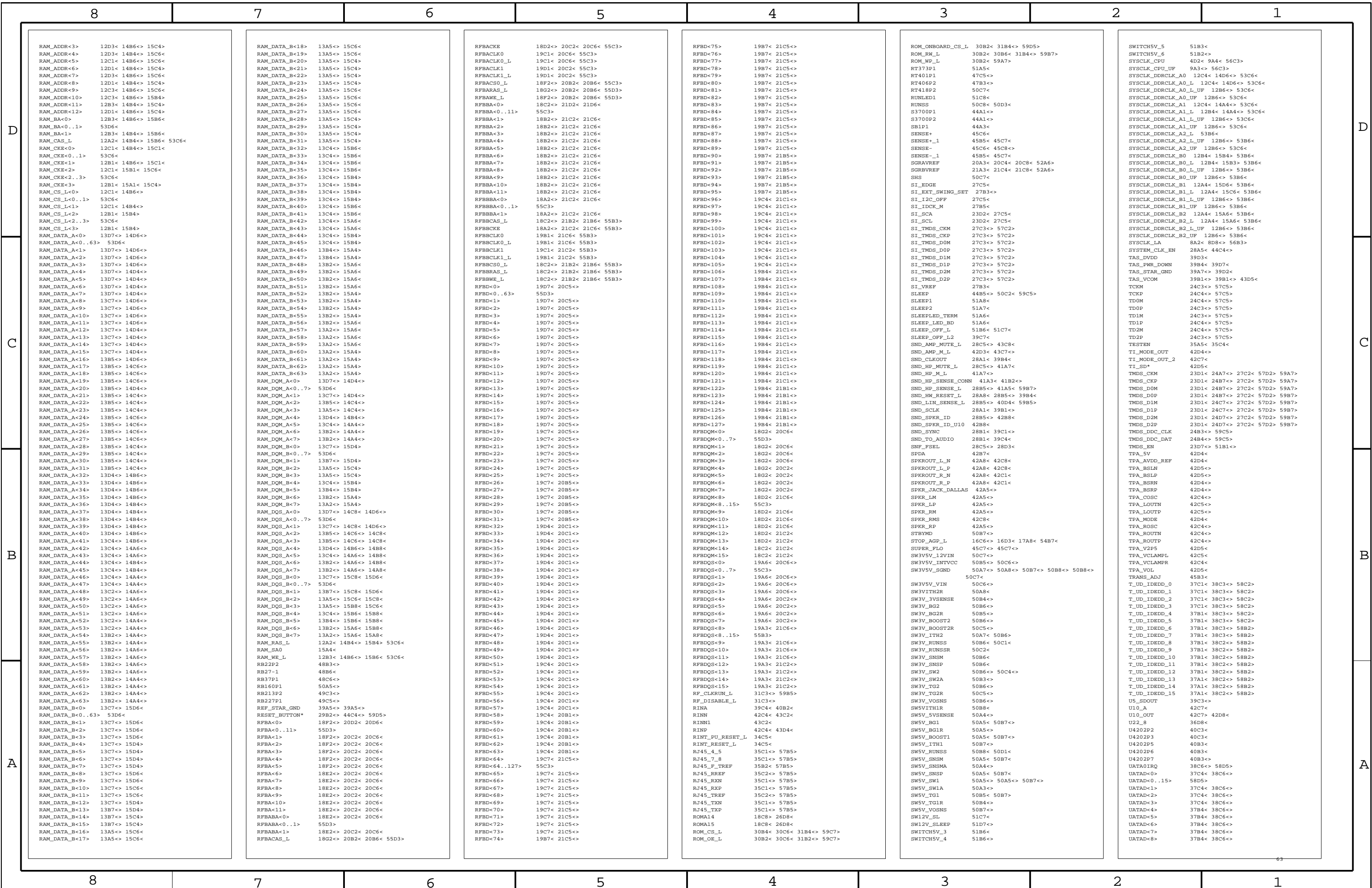
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CONSTRAINT TABLES

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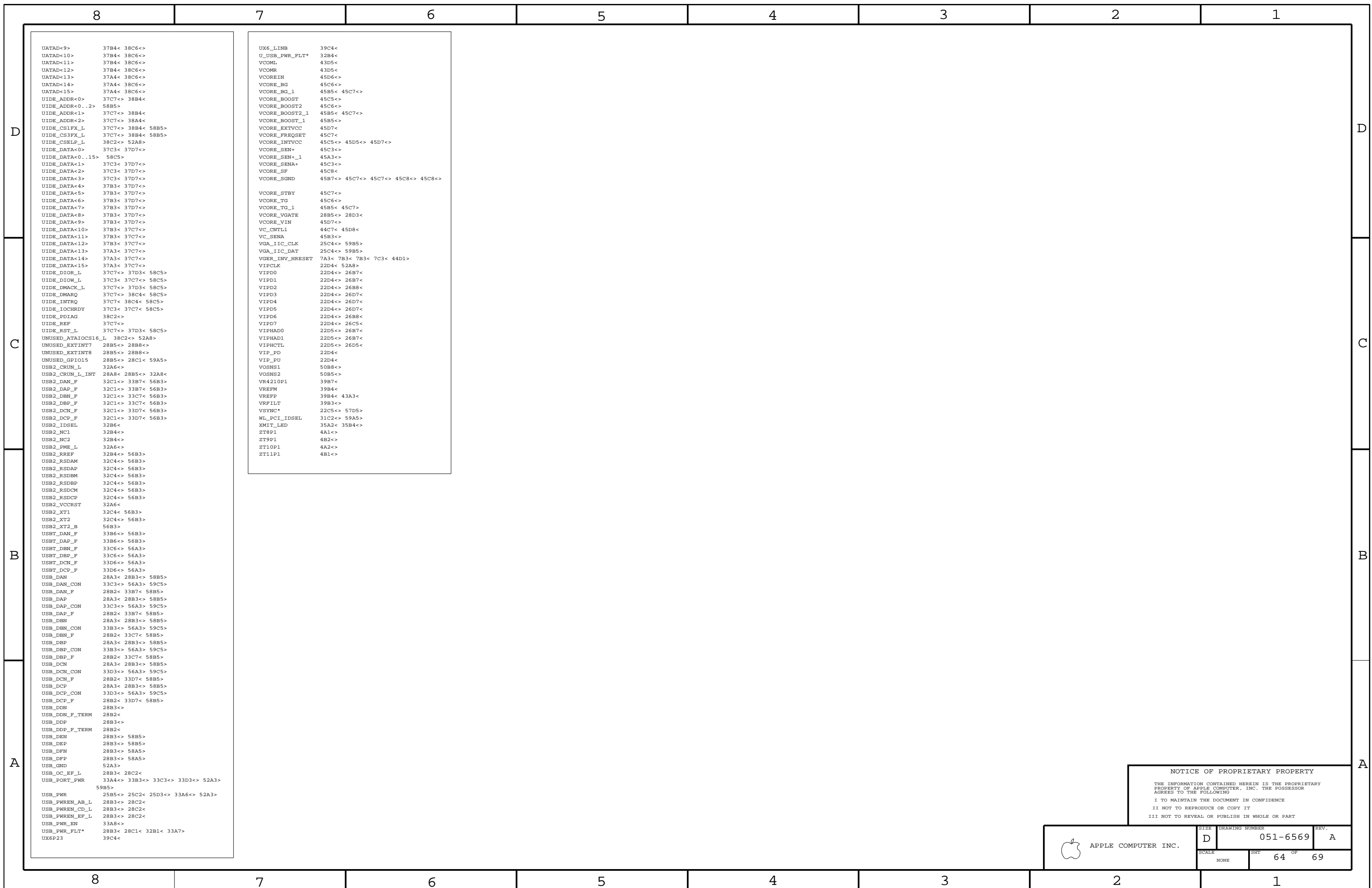
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	BS4 PCR_STANDOFF 29D1	C107 CAP 24B2	C219 CAP 17C2	C336 CAP_P 45C2	C454 CAP 40C6	C575 CAP 48C3		
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	C98 CAP 18H6	C206 CAP 22C2	C325 CAP 27D4	C442 CAP 36C5	C563 CAP 48B6	C677 CAP 11B1		
	C99 CAP 17D1	C207 CAP 22C7	C326 CAP_P 50B2	C443 CAP 36B2	C564 CAP 48C2	C678 CAP 11B3		
	C100 CAP 17D3	C208 CAP 41A5	C327 CAP_P 50B2	C444 CAP 36B2	C565 CAP 20B5	C679 CAP 11B1		
	C101 CAP 17D2	C209 CAP 22B6	C328 CAP_P 50B2	C445 CAP 36C3	C566 CAP 20B7	C680 CAP 11C3		
	C102 CAP 17C2	C210 CAP 22D6	C329 CAP 49B3	C446 CAP 36C3	C567 CAP 20B7	C681 CAP 11B3		
	C103 CAP 17D2	C211 CAP 22D6	C330 CAP_P 49B2	C447 CAP 40B6	C568 CAP 20B8	C682 CAP 11B3		
		C212 CAP 22D6	C331 CAP_P 49B2	C449 CAP 27D4	C569 CAP 20B8	C683 CAP 11A4		
		C213 CAP 22D6	C332 CAP_P 49B2	C450 CAP 36B3	C570 CAP 32C8			

	8	7	6	5	4	3	2	1
D	C685 CAP 11A5 C686 CAP 11A5 C687 CAP 11B6 C688 CAP 11C7 C689 CAP 11C1 C690 CAP 11B2 C691 CAP 11C2 C692 CAP 28D6 C693 CAP 11A6 C694 CAP 11A4 C695 CAP 11A4 C696 CAP 11A4 C697 CAP 11A6 C698 CAP 11C5 C699 CAP 11B7 C700 CAP 11C7 C701 CAP 44B2 C702 CAP 11D4 C703 CAP 28D6 C704 CAP 28D5 C705 CAP 44A6 C706 CAP 44A6 C707 CAP 11B3 C708 CAP 11B3 C709 CAP 11A5 C710 CAP 11A5 C711 CAP 11A5 C712 CAP 11B1 C713 CAP 28D5 C714 CAP 11B5 C715 CAP 44B2 C716 CAP 11B2 C717 CAP 11C3 C718 CAP 11B1 C719 CAP 11D2 C720 CAP 11C3 C721 CAP 11D3 C722 CAP 11B7 C723 CAP 11B6 C724 CAP 11B5 C725 CAP 11C7 C726 CAP 15D3 C727 CAP 11D4 C728 CAP 11C3 C729 CAP 11B3 C730 CAP 11D3 C731 CAP 11D1 C732 CAP 11D1 C733 CAP 11A6 C734 CAP 11D2 C735 CAP 11B7 C736 CAP 11B5 C741 CAP 15D3 C742 CAP 51C6 C743 CAP 11B3 C744 CAP 11B1 C745 CAP 11C3 C746 CAP 11D3 C747 CAP 11D1 C748 CAP 11D2 C749 CAP 11D3 C750 CAP 11B6 C751 CAP 11B7 C752 CAP 11B6 C753 CAP 11B6 C754 CAP 11B5 C755 CAP 11B6 C759 CAP 44D5 C760 CAP 16D6 C761 CAP 11B3 C762 CAP 11C1 C763 CAP 11D2 C764 CAP 11D3 C765 CAP 11D3 C766 CAP 11D1 C767 CAP 11C6 C768 CAP 11B6 C773 CAP 51C6 C774 CAP 11C1 C775 CAP 11C3 C776 CAP 11B2 C777 CAP 11C1 C778 CAP 22B6 C779 CAP 11D1 C780 CAP 11D2 C781 CAP 11B5 C782 CAP 11B7 C783 CAP 44D5 C784 CAP 28A6 C785 CAP 28C3 C786 CAP 27D3 C787 CAP 11D3 C788 CAP 11D3 C789 CAP 11D3 C790 CAP 11D1 C791 CAP 11B6 C792 CAP 11B6 C793 CAP 11C6 C794 CAP 11C5 C795 CAP 28C3 C796 CAP 11C3 C797 CAP 11D3 C798 CAP 11D1 C799 CAP 11D1 C800 CAP 11D2 C801 CAP 11B7 C802 CAP 11B5 C803 CAP 11B6 C805 CAP 11B2 C806 CAP 11C2	C807 CAP 11B2 C808 CAP 11D2 C809 CAP 11C3 C810 CAP 11D2 C811 CAP 11D2 C812 CAP 11C2 C813 CAP 11B5 C814 CAP 11B6 C815 CAP 11C6 C816 CAP 11B6 C817 CAP 11C6 C818 CAP 11B5 C819 CAP 15D3 C820 CAP 28C3 C821 CAP 11C1 C822 CAP 11C1 C823 CAP 11D7 C824 CAP 11D6 C825 CAP 11B7 C826 CAP 11B7 C827 CAP 11C5 C828 CAP 11C1 C829 CAP 11C2 C830 CAP 11C3 C831 CAP 11D3 C832 CAP 11D7 C833 CAP 11D3 C834 CAP 4C2 C835 CAP 11B3 C836 CAP 11C6 C837 CAP 11C7 C838 CAP 8D4 C839 CAP 11C6 C840 CAP 45B2 C841 CAP 11D4 C842 CAP 11D6 C843 CAP 11C7 C844 CAP 11D6 C845 CAP 11D6 C846 CAP 11D7 C848 CAP 30D5 C849 CAP 11C6 C850 CAP 11B3 C851 CAP 11B3 C852 CAP 11B2 C854 CAP 9D3 C855 CAP 11C5 C856 CAP 11B7 C857 CAP 11C6 C858 CAP 13D4 C859 CAP 13D3 C860 CAP 13D4 C861 CAP 44A1 C862 CAP 44B7 C863 CAP 11C2 C864 CAP 15D2 C865 CAP 11B1 C866 CAP 11C3 C867 CAP 11C3 C868 CAP 11C2 C869 CAP 11D5 C870 CAP 11D6 C871 CAP 11D6 C872 CAP 11D5 C873 CAP 11D5 C874 CAP 11D5 C875 CAP 11B3 C876 CAP 11C5 C877 CAP 11C7 C878 CAP 11C7 C879 CAP 11B6 C880 CAP 11C5 C881 CAP 11B3 C882 CAP 11B1 C883 CAP 11B2 C884 CAP 11D6 C885 CAP 11D7 C886 CAP 11D5 C887 CAP 11D7 C888 CAP 45C2 C889 CAP 11D6 C890 CAP 11D7 C891 CAP 11D6 C892 CAP 11C4 C893 CAP 11C1 C894 CAP 11C2 C895 CAP 11D5 C896 CAP 11D5 C897 CAP 11D6 C898 CAP 11D5 C899 CAP 11D5 C900 CAP 11D7 C901 CAP 11D3 C902 CAP 11C7 C903 CAP 11B2 C904 CAP 11C6 C908 CAP 13C2 C909 CAP 13C2 C910 CAP 13C1 C911 CAP 37C2 C914 CAP 15D2 C915 CAP 51D7 C917 CAP 37C5 C918 CAP 51D6 C919 CAP 11D2 C920 CAP 38C1 C921 CAP 38C5 C922 CAP 15D2 C923 CAP 38B5 C924 CAP 38B7	C925 CAP 15D3 C926 CAP 50C1 C927 CAP 50B1 C928 CAP_P 47B4 C929 CAP 14A7 C930 CAP 50B8 C931 CAP 50B5 C932 CAP 50A5 C933 CAP 50A6 C934 CAP 50B1 C935 CAP_P 47B3 C936 CAP 15D3 C937 CAP 50C7 C938 CAP 50A4 C939 CAP 50A6 C940 CAP 50A5 C941 CAP 50C5 C943 CAP 15A3 C944 CAP 45D3 C945 CAP 15A2 C947 CAP_P 45C1 C948 CAP 49B4 C949 CAP 45C5 C950 CAP 45D4 C951 CAP 45D4 C952 CAP 45D4 C953 CAP 45D4 C954 CAP 4C2 C955 CAP 50D3 C956 CAP 50D4 C957 CAP_P 45B1 C958 CAP 8D4 C959 CAP 49C4 C960 CAP 45B2 C961 CAP 8C2 C962 CAP 49C3 C963 CAP 45D4 C964 CAP 45D4 C965 CAP 45D4 C966 CAP 45D4 C967 CAP 8C1 C968 CAP 49C4 C969 CAP 8D4 C970 CAP 50D4 C971 CAP 50D4 C972 CAP 8D2 C973 CAP 8D1 C974 CAP 8D1 C975 CAP 49C4 C976 CAP 8C1 C977 CAP 8D1 C978 CAP 50D4 C979 CAP 50D4 C980 CAP 8D2 C981 CAP 8D2 C982 CAP 8D2 C983 CAP 8D3 C984 CAP 27D3 C985 CAP 50D3 C986 CAP 50D4 C987 CAP 8D2 C988 CAP 8D3 C989 CAP 49C3 C990 CAP 8D1 C991 CAP 8D1 C992 CAP 8D3 C993 CAP 8D1 C994 CAP 8C2 C995 CAP 8D2 C996 CAP 8A7 C997 CAP 8A6 C998 CAP 8D2 C999 CAP 8D1 C1000 CAP 49B6 C1001 CAP 8A6 C1002 CAP 8A7 C1003 CAP 8D1 C1004 CAP 49B6 C1005 CAP 49C4 C1006 CAP 45C2 C1007 CAP 8C2 C1008 CAP 8B6 C1009 CAP 8A7 C1010 CAP 8B6 C1011 CAP 8B6 C1012 CAP 8A7 C1013 CAP 8D2 C1014 CAP 8D2 C1015 CAP 49B7 C1016 CAP 8C1 C1017 CAP 8A6 C1018 CAP 8A6 C1019 CAP 49C6 C1020 CAP 8C1 C1021 CAP 8C1 C1022 CAP 8B7 C1023 CAP 8A6 C1024 CAP 8A6 C1025 CAP 8B6 C1026 CAP 8D2 C1027 CAP 8B7 C1028 CAP 8A6 C1029 CAP 45B4 C1030 CAP 45B2 C1031 CAP 8A6 C1032 CAP 8C2 C1033 CAP 8C1 C1034 CAP 45B2 C1035 CAP 4D3 C1036 CAP 4D3	C1037 CAP 8C1 C1038 CAP 45B4 C1039 CAP 45C5 C1040 CAP 8C2 C1041 CAP 8D3 C1042 CAP 8C1 C1043 CAP 8D2 C1044 CAP 45D7 C1045 CAP 45B7 C1046 CAP 45C1 C1047 CAP 45D5 C1048 CAP 45C2 C1049 CAP 45B7 C1050 CAP 45C7 C1051 CAP 45B6 C1052 CAP 45C8 C1053 CAP 46A7 C1054 CAP 8B2 C1055 CAP 8B2 C1056 CAP 8B1 C1057 CAP 8B1 C1058 CAP 8B1 C1059 CAP 42C7 C1060 CAP 42C6 C1061 CAP 42A8 C1062 CAP 42A7 C1063 CAP 42C6 C1064 CAP 42C6 C1065 CAP 42A7 C1066 CAP 42C6 C1067 CAP 42A6 C1068 CAP 42D6 C1069 CAP 42D4 C1070 CAP 42C4 C1071 CAP 42C4 C1072 CAP 42C3 C1073 CAP 42C3 C1074 CAP 42C3 C1075 CAP 42C2 C1076 CAP 43D5 C1077 CAP 43D5 C1078 CAP 43D5 C1079 CAP 43D5 C1080 CAP_P 42B3 C1081 CAP_P 42A3 C1082 CAP 42B2 C1083 CAP 42B2 C1084 CAP 42B2 C1085 CAP 42B2 C1086 CAP 42A2 C1087 CAP 43D2 C1088 CAP 43D2 C1089 CAP 42B2 C1090 CAP 42B2 C1091 CAP 42B2 C1092 CAP 42B2 C1093 CAP 42A2 C1094 CAP 43C2 C1095 CAP 43D2 C1096 CAP 8A7 C1097 CAP 8A7 C1098 CAP 8B5 C1099 CAP 42C7 C1100 CAP 42C2 C1101 CAP 9D3 C1102 CAP_P 42B3 C1103 CAP 22B5 C1104 CAP 14D7 C11402 CAP 14D2 C11403 CAP 14C1 C11404 CAP 14C1 C11405 CAP 14C1 C11406 CAP 14C3 C11407 CAP 14C2 C11408 CAP 14C2 C11409 CAP 14C2 C11410 CAP 14C2 C11411 CAP 14C1 C11412 CAP 14C1 C11413 CAP 14C1 C11414 CAP 14B1 C11415 CAP 14C3 C11416 CAP 14C2 C11417 CAP 14C2 C11418 CAP 14C2 C11419 CAP 14C2 C11420 CAP 14C1 C11421 CAP 14C1 C1501 CAP 15D7 C1502 CAP 15D1 C1503 CAP 15D1 C1504 CAP 15D3 C1505 CAP 15D3 C1506 CAP 15D3 C1507 CAP 15D2 C1508 CAP 15D2 C1509 CAP 15D2 C1510 CAP 15D1 C1511 CAP 15D1 C1512 CAP 15D1 C1513 CAP 15D1 C1514 CAP 15C3 C1515 CAP 15C3 C1601 CAP 14D7 C1602 CAP 14D3 C1702 CAP 15D7 C1801 CAP 16D5 C1802 CAP 16A7 C1901 CAP 8A7 C1902 CAP 8A6	C1903 CAP 8A6 C1904 CAP 8A6 C1910 CAP 8A6 C1911 CAP 8C2 C1912 CAP 8C1 C1913 CAP 8C1 C1914 CAP 8C1 C2201 CAP 20C8 C2202 CAP 20C4 C2301 CAP 21C8 C2302 CAP 21C4 C2501 CAP_P 23A8 C3001 CAP 28C5 C3002 CAP 28D5 C3003 CAP 28D5 C3004 CAP 28D4 C3005 CAP 28D4 C3201 CAP 30D4 C3501 CAP 35D6 C3502 CAP 33A8 C3901 CAP 37D1 C4081 CAP 46C7 C4201 CAP 42B6 C4261 CAP 42A7 C4262 CAP 42A7 C4265 CAP 42A7 C4267 CAP 42A6 C4301 CAP 41A6 C4302 CAP 43A5 C4303 CAP 43A4 C4502 CAP_P 43B5 C4504 CAP 45B3 C4509 CAP 45C4 C4701 CAP 45B6 C4702 CAP 47B4 C4801 CAP 48B4 C4901 CAP 49B4 C5001 CAP 50C3 C5002 CAP 50A3 D1 DIODE_DUAL_6P 36A7 D2 DIODE_DUAL_6P 36A7 D3 DIODE_DUAL_6P 36A7 D4 DIODE_DUAL_6P 36B7 D5 ZENER_MMBZ15VDLT1 40B6 D6 DIODE_DUAL_6P 25D4 D7 DIODE_DUAL_6P 25D4 D8 DIODE 36D6 D9 DIODE 35B8 D10 DIODE_SCHOT 23B8 D11 DIODE_SCHOT 44D7 D12 DIODE_SCHOT 44D7 D13 DIODE_SCHOT 47C7 D14 DIODE_SCHOT 47B5 D15 DIODE_SCHOT 49B3 D16 DIODE_SCHOT 50C5 D17 DIODE_SCHOT 50B5 D18 DIODE_SCHOT 49C6 D19 DIODE_SCHOT 46D6 D20 DIODE_SCHOT 45D5 D21 DIODE_SCHOT 45B5 D22 DIODE_SCHOT_3P 42A6 D23 ZENER_MMBZ15VDLT1 41B2 D24 ZENER_MMBZ15VDLT1 41B2 D25 ZENER 36B6 D26 ZENER_MMBZ15VDLT1 41B2 D27 DIODE_DUAL_6P 25B4 D28 DIODE_DUAL_6P 25B4 D29 ZENER_MMBZ15VDLT1 40B5 D30 DIODE_SCHOT 48C5 D31 DIODE_SCHOT 48B3 D32 DIODE_SCHOT 48B5 D33 DIODE_SCHOT 46B6 D34 DIODE_SCHOT 48B2 D35 DIODE_SCHOT 44D6 D36 DIODE_SCHOT 44D6 D37 DIODE_SCHOT 50B2 D38 DIODE_SCHOT 50C6 D39 DIODE_SCHOT 50B4 D40 DIODE_SCHOT 50A4 D41 DIODE_SCHOT 45C4 D42 DIODE_SCHOT 49B5 D43 DIODE_SCHOT 45B4 D44 DIODE_SCHOT 45D2 D45 DIODE_SCHOT 45D6 D46 DIODE_SCHOT 49B1 D47 DIODE 36D6 D48 DIODE_DUAL_SWI 42B6 D4901 DIODE_SCHOT 47B2 DS1 LED 35A2 DS2 LED 35A1 DS3 LED 35A1 DS4 LED 30A3 DS5 LED 51C8 DS6 LED 51A6 DS7 LED 38B2 DS8 LED 38B6 DS9 LED 50D5 DS10 LED 51A4 D21 ZENER 51B1 F2 FUSE 36D5 F3 FUSE 36D5 FL2 FILTER_IC 25C6 FL3 FILTER_IC 25C6 FL4 FILTER_IC 25B6 J1 CON_RJ45 35C1 J2 CON_FWVERT_SKT 36C1 J3 CON_F8RT_S_TH1 42B5 J4 CON_F4RT_USB_UPRIGHT 33C3 J5 CON_FWVERT_SKT 36D1 J6 CON_F4RT_USB_UPRIGHT 33B3 J7 CON_F4RT_USB_UPRIGHT 33D3	J8 CON_F4RT_S4MT_TH1 41C1 J9 CON_F14RT_D4MT_TH1 25C5 J10 CON_F4RT_S4MT_TH1 40C7 J11 CON_F184ST_DDRDIMM 15D5 J12 CON_F21ST_D2MT_SM 24C4 J13 CON_M40SM_635 29D6 J14 CON_M18ST_D_TH 29B5 J15 CON_M40ST_NC20 38D6 J16 CON_M40ST_NC20 38D2 J17 CON_M16ST_MICROFIT 50D7 J18 CON_M45T_LCK 34B4 J19 CON_37SM_MTOR 8C4 J20 CON_38SM_MTOR 8D7 J21 CON_M35T_LCK 45C8 J22 CON_F20SM_KX 8A4 J23 CON_F15T_S2MT_SM 28B7 J24 CON_M12ST_SM 29B3 J25 CON_F100RT_LP_SM 31D3 J26 CON_F200RT_DDRDIMM_SM2 14D5 J27 CON_F15T_S2MT_SM 8B1 J28 CON_F10ST_D_SMA 29D2 J30 CON_38SM_MTOR 8D4 J31 CON_38SM_MTOR 8C7 J32 CON_F12RT_S2MT_SM 8A8 J4501 CON_F45T_S2MT_SM 43B6 J4502 CON_F45T_S2MT_SM 43B6 JA21 TP 51A5 L1 IND 36D4 L2 IND 33A5 L3 IND 36D4 L4 IND 27D5 L5 FILTER_4P 36C2 L6 FILTER_4P 36C2 L7 FILTER_4P 36D2 L8 FILTER_4P 36D2 L9 IND 25C2 L12 IND 48B3 L13 IND 22D7 L16 IND 28C3 L19 IND 47B4 L20 IND 45C3 L21 IND_3P 49B3 L22 IND_3P 50A3 L23 IND 50C3 L24 IND 45B3 L26 IND 42A6 L27 IND 41C3 L32 IND 36B6 L33 IND 22B7 L34 IND 41D3 L35 IND 41B3 L36 IND 40B6 L39 IND 41A3 L40 IND 42A5 L41 IND 42B7 L42 IND 41B3 L43 IND 41A4 L44 IND 41C3 L45 IND 41D3 L46 IND 40C6 L47 IND 41B3 L48 IND 40C6 L49 IND 40B5 L50 IND 40C5 L51 IND 40D6 L52 IND 40C5 L53 IND 40D5 L56 IND 44A1 L57 IND 44A1 L58 IND 32D6 L59 IND 43A5 L60 IND 43B5 L63 IND 39D4 L64 IND 24A5 L65 IND 29A7 L66 IND 29A3 L67 FILTER_4P 24B5 L68 IND 22D2 L69 IND 29A3 L70 IND 29A7 L71 FILTER_4P 24B5 L72 IND 29A7 L73 IND 29A3 L74 FILTER_4P 24C5 L75 IND 29A7 L76 FILTER_4P 24D5 L77 IND 29B7 L78 IND 29A3 L79 IND 43B7 L80 IND 29B3 L81 IND 43A7 L82 IND 24D5 L83 IND 43A7 L84 IND 50D6 L85 IND 50D6 L86 IND 50D6 L87 IND 27D5 L88 IND 27D2 L89 IND 42D7 L90 IND 42C6 L91 IND 42C6 L92 IND 42C7 L93 IND 42C3 L94 IND 42C2 L95 IND 42D2 L96 IND 42C3 L97 IND 43D7 L98 IND 43D7 L99 IND 42B3 L100 FILTER_4P 33D5	A	
A	8	7	6	5	4	3	2	1
B								
C								
D								

	8	7	6	5	4	3	2	1
D	L101 FILTER_4P 33C5 L102 FILTER_4P 33B5 L103 IND 29B3 L2401 IND 22C7 L2501 IND 23A6 LP1 LPAK4P 42A8 Q1 TRA_2N7002 51C3 Q2 TRA_2N7002 42D7 Q3 TRA_2N7002 42C7 Q4 TRA_2N7002 42B8 Q5 TRA_2N7002 41A5 Q6 TRA_2N7002 42B6 Q7 TRA_SUD70N03 48B4 Q8 TRA_SUD50N03 48B4 Q9 TRA_SUD50N03 48C4 Q10 TRA_2N7002 22B7 Q11 TRA_FDC602P 51C2 Q12 TRA_2N3904 44D7 Q13 TRA_2N7002 51B2 Q14 TRA_2N7002 51C7 Q15 TRA_2N7002 51A7 Q16 TRA_2N7002 51A7 Q17 TRA_2N7002 51B6 Q18 TRA_2N7002 51A7 Q19 TRA_2N7002 51A6 Q20 TRA_FDC602P 51D7 Q21 TRA_2N7002 50C1 Q22 TRA_2N7002 50D1 Q23 TRA_2N7002 50C2 Q24 TRA_2N7002 50C2 Q25 TRA_IRF7807Z 47B5 Q26 TRA_IRF7807Z 47B5 Q27 TRA_SUD70N03 49B4 Q28 TRA_SUD50N03 49B4 Q29 TRA_2N7002 45D8 Q30 TRA_2N3904 36C7 Q31 TRA_2N7002 41A8 Q32 TRA_2N7002 39C7 Q33 TRA_2N3904 43A2 Q34 TRA_SUD70N03 48B4 Q35 TRA_2N7002 40D4 Q36 TRA_2N7002 42D3 Q37 TRA_FDC602P 51C6 Q38 TRA_2N7002 51B6 Q39 TRA_2N3904 50C7 Q40 TRA_SUD70N03 45C4 Q41 TRA_2N7002 15B2 Q42 TRA_2N7002 15C2 Q43 TRA_SUD70N03 45C4 Q44 TRA_SUD50N03 45C4 Q45 TRA_IRF7807Z 50B4 Q46 TRA_IRF7807Z 50C4 Q47 TRA_SUD50N03 50A4 Q48 TRA_SUD50N03 50A4 Q49 TRA_SUD70N03 45B4 Q50 TRA_SUD50N03 45B4 Q51 TRA_SUD70N03 45B4 Q52 TRA_2N7002 15B2 Q53 TRA_2N7002 15A2 Q54 TRA_2N7002 15B2	R51 RES 42B7 R52 RES 18C5 R53 RES 19A4 R54 RES 18D3 R55 RES 19A4 R56 RES 18D2 R57 RES 19A4 R58 RES 18D3 R59 RES 18C2 R60 RES 19A4 R61 RES 18A3 R62 RES 18A2 R63 RES 19A4 R64 RES 18D3 R65 RES 19A4 R66 RES 18D2 R67 RES 18D2 R68 RES 19A4 R69 RES 19A4 R70 RES 18D3 R71 RES 18D6 R72 RES 17A5 R73 RES 26C2 R74 RES 26D2 R75 RES 35B8 R76 RES 19A6 R77 RES 26D2 R78 RES 32A7 R79 RES 26C2 R80 RES 17A5 R81 RES 19A7 R82 RES 12A8 R83 RES 18A5 R84 RES 18D2 R85 RES 23D6 R86 RES 23D6 R87 RES 26B3 R88 RES 18A5 R89 RES 32D3 R90 RES 18D3 R91 RES 23D6 R92 RES 23D6 R93 RES 12A8 R94 RES 26A3 R95 RES 18A5 R96 RES 35B1 R97 RES 19A7 R98 RES 23D6 R99 RES 42D8 R100 RES 26A8 R101 RES 19A7 R102 RES 23C5 R103 RES 19B2 R104 RES 19B2 R105 RES 19C2 R106 RES 19C2 R107 RES 23D5 R108 RES 42D7 R109 RES 42D6 R110 RES 42C8 R111 RES 18D2 R112 RES 23D6 R113 RES 23D5 R114 RES 23C5 R115 RES 23C5 R116 RES 26C6 R117 RES 18D3 R118 RES 22D3 R119 RES 23C5 R120 RES 42B8 R121 RES 42D8 R122 RES 19A7 R123 RES 19D2 R124 RES 23C5 R125 RES 26D5 R126 RES 26C6 R127 RES 32B8 R128 RES 32B8 R129 RES 32D3 R130 RES 18D2 R131 RES 18D3 R132 RES 19D2 R133 RES 22D3 R134 RES 26B8 R135 RES 42D7 R136 RES 26C5 R137 RES 12B1 R138 RES 30B3 R139 RES 30B4 R140 RES 19A7 R141 RES 23B5 R142 RES 26C5 R143 RES 18G2 R144 RES 23B2 R145 RES 22D3 R146 RES 19A7 R147 RES 35C4 R148 RES 19C2 R149 RES 23B5 R150 RES 48C5 R151 RES 20A4 R152 RES 20A5 R153 RES 19A7 R154 RES 18D3 R155 RES 18G2 R156 RES 19C2 R157 RES 23B3 R158 RES 19D2 R159 RES 19A7 R160 RES 17A5	R161 RES 16D1 R162 RES 41A5 R163 RES 20A4 R164 RES 18D3 R165 RES 35C4 R166 RES 20A4 R167 RES 19A7 R168 RES 17A7 R169 RES 17A4 R170 RES 22B5 R171 RES 22B6 R172 RES 12A1 R173 RES 22C7 R174 RES 22C6 R175 RES 40D4 R176 RES 20A4 R177 RES 17A5 R178 RES 22C7 R179 RES 22C6 R180 RES 40D5 R181 RES 41A4 R182 RES 41A4 R183 RES 22C3 R184 RES 23C6 R185 RES 22B6 R186 RES 19A6 R187 RES 19A6 R188 RES 22B2 R191 RES 22B6 R192 RES 17A2 R193 RES 17A2 R194 RES 22B6 R195 RES 17A3 R196 RES 17A3 R197 RES 16A7 R198 RES 17C1 R199 RES 22D6 R200 RES 47B3 R203 RES 16C8 R204 RES 16B8 R205 RES 16A8 R206 RES 22D6 R207 RES 23D2 R208 RES 23D2 R210 RES 17B7 R211 RES 16C7 R212 RES 30B3 R213 RES 23C5 R214 RES 12B1 R215 RES 29D3 R216 RES 16B7 R217 RES 50B8 R218 RES 30D6 R219 RES 30D6 R220 RES 16C7 R221 RES 16D1 R222 RES 16D3 R223 RES 16D1 R224 RES 16C7 R225 RES 9D5 R226 RES 16C7 R227 RES 30C6 R228 RES 28C7 R230 RES 30C6 R231 RES 28C8 R232 RES 28C6 R233 RES 16D1 R234 RES 16D1 R235 RES 12A1 R236 RES 26D2 R237 RES 23C5 R238 RES 27A6 R239 RES 42B7 R240 RES 42B6 R241 RES 27A5 R242 RES 42B5 R243 RES 27A6 R244 RES 27A5 R245 RES 42B5 R246 RES 23B7 R247 RES 28A2 R248 RES 27A7 R249 RES 42B5 R250 RES 27A7 R251 RES 51B3 R252 RES 30C7 R253 RES 30C8 R254 RES 34B4 R255 RES 30C7 R256 RES 30C8 R257 RES 50D5 R258 RES 37D5 R259 RES 30C7 R261 RES 12D5 R262 RES 30C8 R263 RES 37D4 R264 RES 28D1 R265 RES 38B4 R266 RES 37C6 R267 RES 28B1 R268 RES 38B4 R269 RES 34C4 R270 RES 37D2 R271 RES 28B3 R272 RES 28B3 R273 RES 37D2 R274 RES 28C7 R275 RES 34C4 R276 RES 28C8 R277 RES 51B2	R278 RES 51B3 R279 RES 51B2 R280 RES 44D8 R281 RES 44D7 R282 RES 44D7 R283 RES 51B3 R284 RES 51A3 R285 RES 31C1 R286 RES 12A3 R287 RES 44D5 R288 RES 12D5 R289 RES 28C8 R290 RES 44D8 R291 RES 28C7 R292 RES 28C7 R293 RES 31C5 R294 RES 28C1 R295 RES 47B3 R296 RES 47B7 R297 RES 44D6 R298 RES 44B1 R299 RES 47B3 R300 RES 51C8 R301 RES 47B5 R302 RES 51A6 R303 RES 34D7 R304 RES 47B3 R305 RES 28A2 R306 RES 28B8 R307 RES 34D7 R308 RES 8B1 R309 RES 47B7 R310 RES 9A4 R311 RES 4B8 R312 RES 4A8 R313 RES 8A2 R314 RES 8B2 R315 RES 47B3 R316 RES 47B7 R317 RES 47C5 R318 RES 47C6 R319 RES 9A5 R320 RES 47B5 R321 RES 9A5 R322 RES 50C2 R323 RES 50D2 R324 RES 42B5 R326 RES 35B3 R328 RES 29D3 R329 RES 29D3 R330 RES 50A8 R331 RES 50B8 R332 RES 50A7 R333 RES 28A2 R334 RES 49B1 R335 RES 50A5 R336 RES 50C5 R337 RES 50B5 R338 RES 9C5 R339 RES 9D5 R340 RES 9D5 R341 RES 9C5 R342 RES 9A7 R343 RES 9C6 R344 RES 9A7 R345 RES 9A7 R346 RES 7C7 R347 RES 7C7 R348 RES 7C7 R349 RES 7B7 R350 RES 33D7 R351 RES 9C5 R352 RES 9C6 R353 RES 9A7 R354 RES 9C6 R355 RES 9C7 R356 RES 6C4 R357 RES 6C4 R358 RES 9C6 R359 RES 9C7 R360 RES 9C6 R361 RES 45B3 R362 RES 45B3 R363 RES 6C5 R364 RES 6C5 R365 RES 6C4 R366 RES 9C7 R367 RES 6C4 R368 RES 6C4 R369 RES 49C6 R370 RES 50D5 R371 RES 49B6 R372 RES 46D4 R373 RES 32A7 R374 RES 6C6 R375 RES 6C6 R376 RES 6C7 R377 RES 6C7 R378 RES 6C7 R379 RES 6C8 R380 RES 6C7 R381 RES 6C8 R382 RES 6C8 R383 RES 6C8 R384 RES 45C5 R385 RES 46D6 R386 RES 45B5 R387 RES 45B5 R388 RES 45B6 R389 RES 45B6	R390 RES 35C1 R391 RES 35C2 R392 RES 41B3 R393 RES 35C2 R394 RES 35C2 R395 RES 36B7 R396 RES 28A2 R397 RES 26A7 R398 RES 28A2 R399 RES 26B7 R400 RES 41C4 R401 RES 26B6 R402 RES 36B4 R403 RES 19B2 R404 RES 36D8 R405 RES 15C2 R406 RES 41D4 R407 RES 40C5 R408 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