

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M42B MLB NO_LDO SCHEMATIC

3/22/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
07		355269	ENGINEERING RELEASED	12/10/04	?

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38	38	FIREWIRE CONTROLLER	ES	ENET	08/30/2005
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40	40	CONNECTOR MISC	ES	ENET	11/16/2005
41	41	IR CONTROLLER	ES	ENET	11/09/2005
42	42		ES	ENET	11/01/2005
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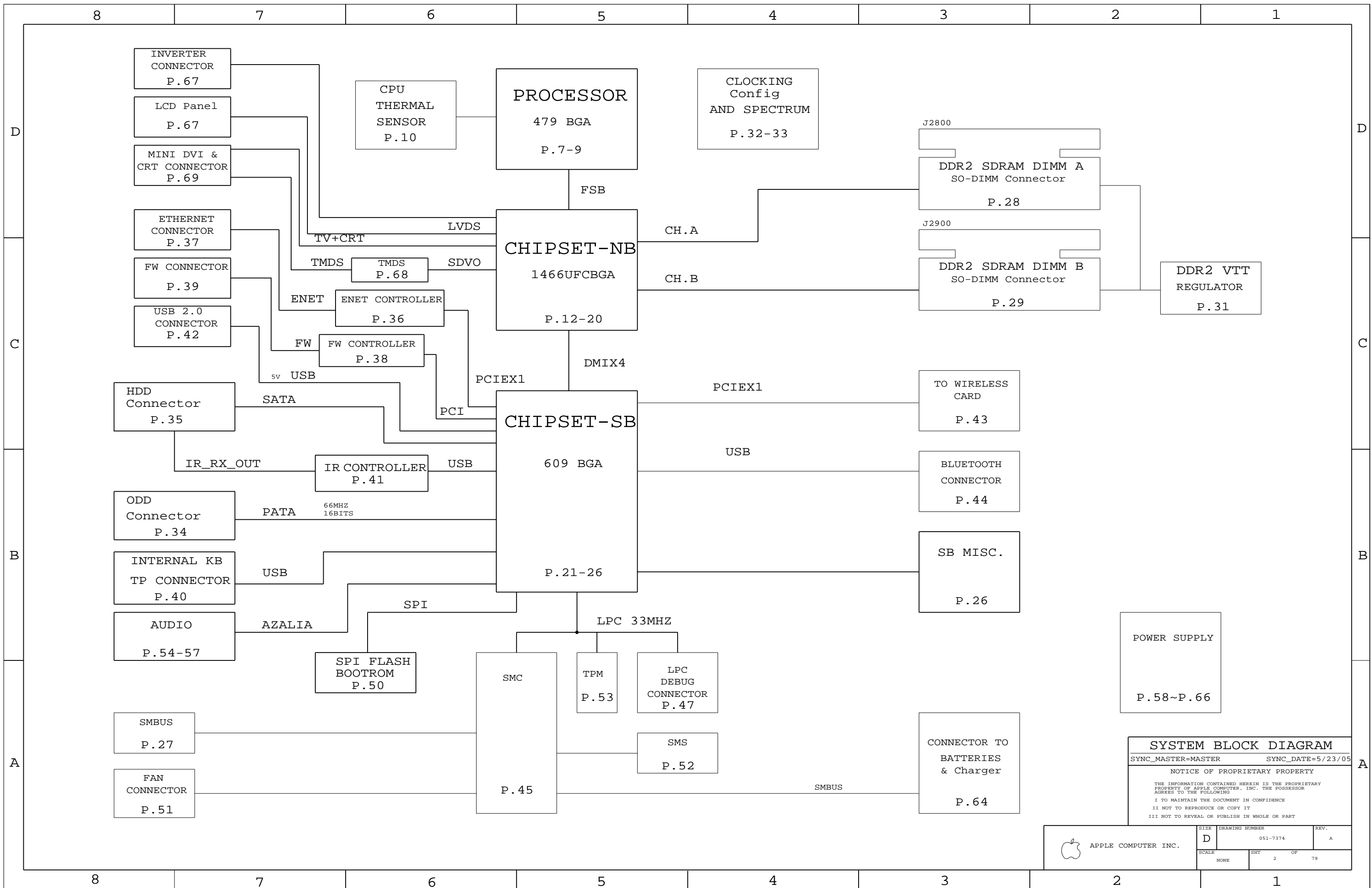


EE DRIS:
 RX-RAYMOND XU
 DK-DINESH KUMAR
 RC-RAY CHANG
 MK-MARC KLINGELHOFER
 LT-LAWRENCE TAN
 LD-LINDA DUNN

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7374	1	SCHEM, M42B, MLB NO_LDO	SCH	
820-1889	1	PCBF, M42, MLB NO_LDO	PCB	

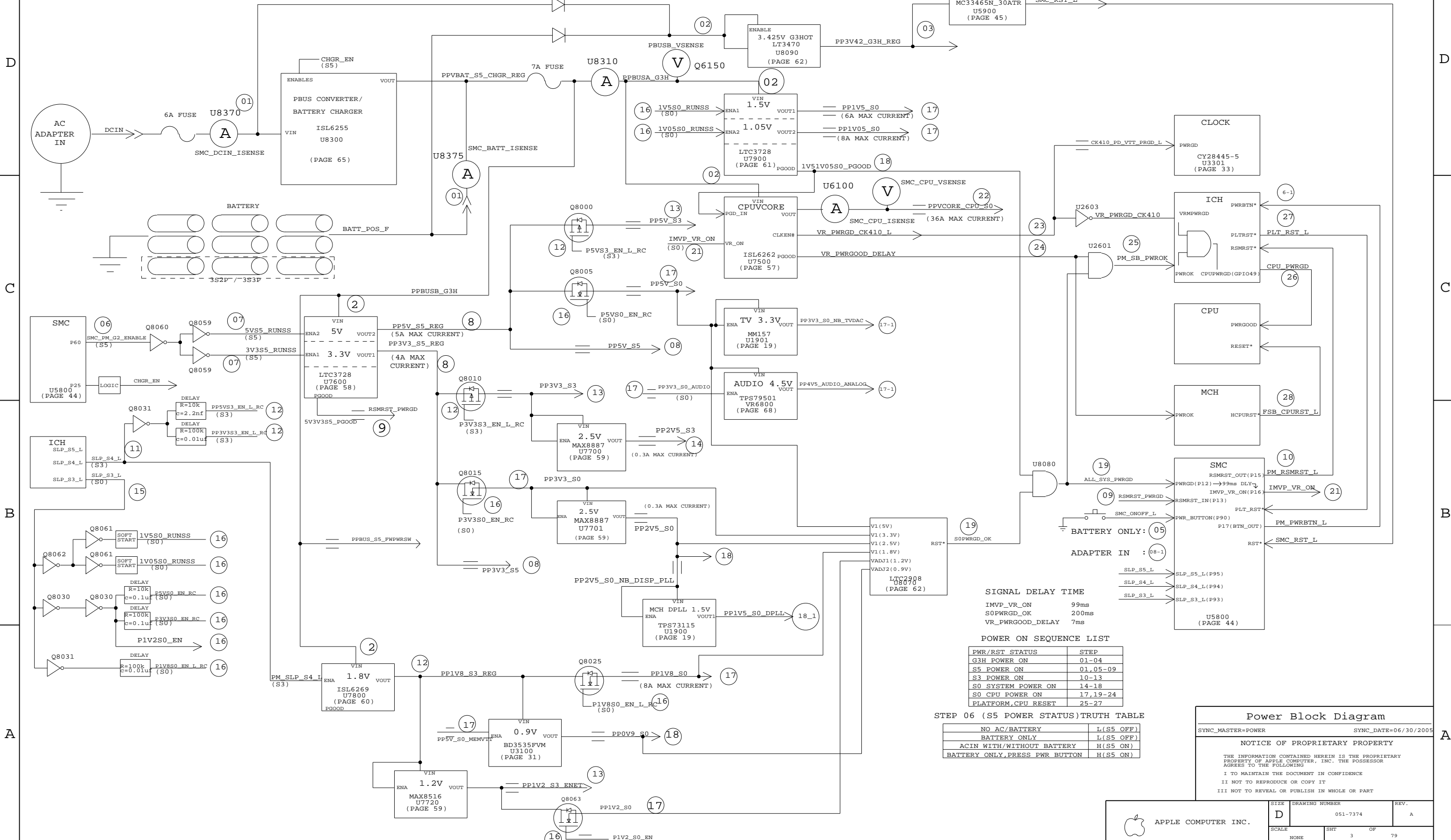
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XX : _____		DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____		ENG APPD	MFG APPD		
X.XXX : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER
				051-7374	REV. A
				SHT 1 OF 79	



SYSTEM BLOCK DIAGRAM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	2		

M42A POWER SYSTEM ARCHITECTURE



SIGNAL DELAY TIME

IMVP_VR_ON	99ms
SOPWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

POWER ON SEQUENCE LIST

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

STEP 06 (S5 POWER STATUS) TRUTH TABLE

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY,PRESS PWR BUTTON	H(S5 ON)

Power Block Diagram

SYNC_MASTER=POWER SYNC_DATE=06/30/2005

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	v	v	v	v	v	v
5V3V3S3_CONT						
5V3V3S3_SKIP	v	v	v	v	v	v
ACCEL_KIONIX			v	v	v	
ACCEL_ST	v	v				v
INVERTER_BUF	v	v	v	v	v	v
INVERTER_UNBUF						
ITP						
LEMENU	v	v	v	v	v	v
MEMVIT_EN_PU	v	v	v	v	v	v
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	v	v	v	v	v	v
USB_D_OC_PU	v	v	v	v	v	v
USB_E_OC_PU	v	v	v	v	v	v
GOOD	v			v		
BETTER		v			v	
BEST			v			v
M42A_PGM	v	v	v	v	v	v
ONEWIRE_PULLUP	v	v	v	v	v	v
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	v	v	v	v	v	v
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	v	v	v	v	v	v
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	v	v	v	v	v	v
3V3_IND_3MM						
NORMAL	v	v		v	v	
FANCY			v			v
STANDOFF	v	v	v	v	v	v
FET_FDN6296	v	v	v	v	v	v
FET_STL8NH3LL						
GOOD-ST	v					
BETTER-ST		v				
BEST-KIONIX			v			
GOOD-KIONIX				v		
BETTER-KIONIX					v	
BEST-ST						v
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	v	v	v	v	v	v
M42						
M42A	v	v	v	v	v	v

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

MLB STACKUP		
LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT		
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3450	1	IC, MEMOM, CPU L2 1.83GHZ, 479 PGA	U0700	GOOD
337S3389	1	IC, MEMOM, CPU 2.0GHZ, 479 PGA	U0700	BETTER
337S3391	1	IC, MEMOM, CPU 2.16GHZ, 479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC, FW32306, 1394A LINK, BGA, 129P	U4400	LEMENU
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	LEMENU
359S0109	1	IC, SLOBLP436, CLOCK GEN, 68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S2131	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, 802CE	U6301	M42A_PGM
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, 808	U4102	M42A_PGM
341S2133	1	IC, SMC, 176P BGA, MS8/2116	U5800	M42A_PGM
341S1890	1	IC, PSOC-W/USB, 56P, MFP, CY8C24794	U5100	M42A_PGM

341S2132 FOR M42B LOCKED BOOTROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:YCT	CRITICAL	BEST-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:YCS	CRITICAL	BETTER-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:YCR	CRITICAL	GOOD-KIONIX

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	4		

Functional Test Points

Power Supply NO_TESTs

NO_TEST		
IMVP6_RBIAS	58A4	58B7
IMVP6_COMP	58A4	58B7
5VS5_RUNSS	5984	63C7
1V5S0_RUNSS	62B5	63B7
1V8S3_COMP	6186	
1V8S3_FSET	61C6	
TRUE 3V3S5_COMP		
TRUE 3V3S5_FSET		
TRUE 1V05S0_COMP		
TRUE 1V05S0_FSET		
TRUE P3V42G3H_FB	63D2	

CLOCK NO_TESTS

NO_TEST		
TRUE CK410_CPU0_N	32C4	33D5
TRUE CK410_CPU0_P	32C4	33D5
TRUE CK410_CPU1_N	32C4	33D5
TRUE CK410_CPU1_P	32C4	33D5
TRUE CK410_CPU2_ITP_SRC10_N	32C4	33D5
TRUE CK410_CPU2_ITP_SRC10_P	32C4	33D5
TRUE CK410_DOT96_27M_N	32A4	33B5
TRUE CK410_DOT96_27M_P	32A4	33B5
TRUE CK410_LVDS_N	32B4	33A5
TRUE CK410_LVDS_P	32B4	33A5
TRUE CK410_PCI4_CLK_SPN		
TRUE CK410_PCI4_CLK	32B6	33D6
TRUE CK410_SRC1_N_SPN	6B3	
TRUE CK410_SRC1_P_SPN	6B3	
TRUE CK410_SRC2_N	32B4	33C5
TRUE CK410_SRC2_P	32B4	33C5
TRUE CK410_SRC3_N_SPN	6B3	
TRUE CK410_SRC3_P_SPN	6B3	
TRUE CK410_SRC4_N	32B4	33B5
TRUE CK410_SRC4_P	32B4	33B5
TRUE CK410_SRC5_N	32B4	33C5
TRUE CK410_SRC5_P	32B4	33C5
TRUE CK410_SRC6_N	32B4	33C5
TRUE CK410_SRC6_P	32B4	33C5
TRUE CK410_SRC7_N_SPN	6B3	
TRUE CK410_SRC7_P_SPN	6B3	
TRUE CK410_SRC8_N	32A4	33C5
TRUE CK410_SRC8_P	32A4	33C5
TRUE CK410_SRC_CLKREQ01_L_SPN	6B3	
TRUE CK410_SRC_CLKREQ03_L_SPN	6B3	
TRUE CK410_SRC_CLKREQ08_L	32A4	33A5

FIREWARE NO_TESTS

NO_TEST		
TRUE FW_B_TPA_N_SPN	6D1	
TRUE FW_B_TPA_P_SPN	6D1	
TRUE FW_B_TPBIAS_SPN	6D1	
TRUE FW_B_TPB_N_SPN	6D1	
TRUE FW_B_TPB_P_SPN	6D1	
TRUE FW_C_TPA_N_SPN	6D1	
TRUE FW_C_TPA_P_SPN	6D1	
TRUE FW_C_TPBIAS_SPN	6D1	
TRUE FW_C_TPB_N_SPN	6D1	
TRUE FW_C_TPB_P_SPN	6D1	

LVDS NO_TESTS

NO_TEST		
TRUE LVDS_B_CLK_N_SPN	6D5	
TRUE LVDS_B_CLK_P_SPN	6D5	
TRUE LVDS_B_DATA_N0_SPN	6D5	
TRUE LVDS_B_DATA_N1_SPN	6D5	
TRUE LVDS_B_DATA_N2_SPN	6D5	
TRUE LVDS_B_DATA_P1_SPN	6D5	
TRUE LVDS_B_DATA_P2_SPN	6D5	

ETHERNET NO_TESTS

NO_TEST		
TRUE ENET_MDI_TRAN_P<2>	37B5	
TRUE ENET_MDI_TRAN_N<2>	37B5	
TRUE ENET_MDI_TRAN_P<3>	37B5	

NO_TEST		
TRUE SMC_FAN_3_TACH	45B8	46C3
TRUE ALS_LEFT	45A8	46C3

Fan Connectors

FUNC_TEST		
TRUE =PP5V_S0_FAN_RT	51C4	64D3
TRUE FAN_RT_PWM	51B3	
TRUE FAN_RT_TACH	51C3	
TRUE =PP3V3_S0_FAN_RT	51C4	64A6
TRUE SMC_FAN_1_CTL	45B8	51B4
TRUE SMC_FAN_1_TACH	45B8	51C4

LPC+ Debug Connector

FUNC_TEST		
TRUE =PP3V42_G3H_LPCPLUS	47C6	64D1
TRUE =PP5V_S0_LPCPLUS	47C6	64D3
TRUE LPC_AD<0>	31D4	45D8 47C5 53C6
TRUE LPC_AD<1>	31D4	45D8 47C5 53C6
TRUE LPC_FRAME_L	31C5	45C8 47C5 53C6
TRUE PM_CLKRUN_L	23C8	38A5 45D6 47C6
TRUE BOOT_LPC_SPI_L	31C5	
TRUE SMC_TMS	45B5	46C6 47C6
TRUE DEBUG_RST_L	36B1	47C6
TRUE SMC_TRST_L	45C1	47C6
TRUE SMC_TDO	45C5	46C6 47B6
TRUE SMC_MD1	45C2	47B6
TRUE SMC_TX_L	45C8	46B2 46C6 47B6
TRUE FWH_INIT_L	5B2	21C4 47C5
TRUE PCI_CLK_PORT80_LPC	33D6	47C5
TRUE LPC_AD<2>	31D4	45D8 47C5 53C6
TRUE LPC_AD<3>	31D4	45D8 47C5 53C6
TRUE INT_SERIRO	33C8	45C8 47C5 53C6
TRUE PM_SUS_STAT_L	23C5	45D5 46D3 47C5
TRUE SMC_TDI	45C5	46C6 47C5
TRUE SMC_TCK	45C5	46C6 47C5
TRUE SMC_RST_L	45C1	46D7 47C5
TRUE SMC_NMI	45C1	47B5
TRUE SMC_RX_L	45C8	46B2 46C6 47B5
TRUE SV_SET_UP	23B6	23C3 47B5

Other Func Test Points

FUNC_TEST		
TRUE =PP1V05_S0_REG	62B1	64D8
SMBus FUNC_TEST		
TRUE SMBUS_SMC_MLB_SCL	37C5	
TRUE SMBUS_SMC_MLB_SDA	37B5	
FIREWIRE FUNC_TEST		
TRUE PPFW_SWITCH	39D4	
SLEEP_LED_FUNC_TEST		
TRUE SYS_LED_ANODE	35C5	46A3
SMC FUNC_TEST		
TRUE SMC_LID	40C4	45B5 46C5 65A8
TRUE SMC_MANUAL_RST_L	46D8	
TRUE SMC_CPU_VSENSE	45D5	48B1
Power Supply FUNC_TEST		
TRUE ALL_SYS_PWRGD	26A5	45D8 63B1
TRUE PPVCORE_CPU_S0	64D7	
TRUE PP1V05_S0	64D7	
TRUE PP1V5_S0	64C7	
TRUE PP1V8_S0	64C7	
TRUE PP2V5_S0	64B7	
TRUE PP3V3_S0	64B7	
TRUE PP5V_S0	64D4	
TRUE PP1V2_S3	64C4	
TRUE PP1V8_S3	64C4	
TRUE PP2V5_S3	64C4	
TRUE PP3V3_S3	64B4	
TRUE PP5V_S3	64B4	
TRUE PP3V3_S5	64A4	
TRUE PP5V_S5	64A4	
TRUE PP3V42_G3H	64D3	
TRUE PPBUS_A_G3H		
TRUE PPBUS_B_G3H		
TRUE PP18V5_G3H	64C1	
TRUE PP0V9_S0	64C1	

Battery Digital Connector

FUNC_TEST		
TRUE SMC_BS_ALRT_L	45C5	46C6 65A2
TRUE SMBUS_BATT_SCL_F	65B6	
TRUE SMBUS_BATT_SDA_F	65A6	
TRUE BATT_IN		
TRUE BATT_POS	65A6	
TRUE BATT_NEG	65A6	

Audio FUNC_TEST

FUNC_TEST		
TRUE PP5V_S0_AUDIO_PWR		
TRUE PP5V_S0_AUDIO		
TRUE GND_AUDIO_PWR	64B2	
TRUE GND_AUDIO_CODEC	64B2	
TRUE ACZ_SDATAIN<0>	21C7	54D7
TRUE ACZ_SDATAOUT	21C7	54D7
TRUE ACZ_BITCLK	21C7	54D7
TRUE ACZ_RST_L	21C7	54C7 57C3
TRUE ACZ_SYNC	21C7	54D7

Battery FUNC_TEST

FUNC_TEST		
TRUE SMC_BATT_ISET	45B5	66B7
TRUE SMC_BATT_CHG_EN	45D8	46B6 66A4
TRUE SMC_BC_ACOK	45C5	46B6 65C3
TRUE SMC_PS_ON	39C6	45D5 46B3
TRUE SMC_BATT_TRICKLE_EN_L	45D8	46B6 66A3
TRUE SYS_ONEWIRE	45B8	46D6 65C8

USB FUNC_TEST

FUNC_TEST		
TRUE TP_USBP_E	6C2	
TRUE TP_USBN_E	6C2	
TRUE TP_USBP_F		
TRUE TP_USBN_F		

DC-JACK FUNC_TEST

FUNC_TEST		
TRUE ACIN_ENABLE_GATE	65C3	

Battery charger FUNC_TEST

FUNC_TEST		
TRUE PPVBAT_G3H_CHGR_OUT	66B5	66C2

INVERTER CONNECTOR FUNC_TEST

FUNC_TEST		
TRUE PPBUS_ALL_INV_CONN	67D3	
TRUE INV_GND	67D3	
TRUE PP5V_INV_F	67D3	
TRUE INV_BKLIGHT_PWM_L	67D3	



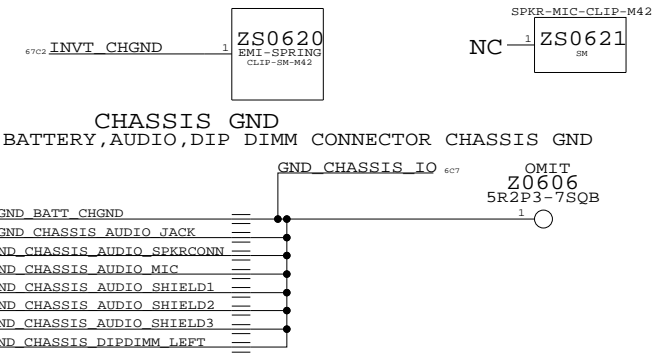
FUNC TEST 1 OF 2

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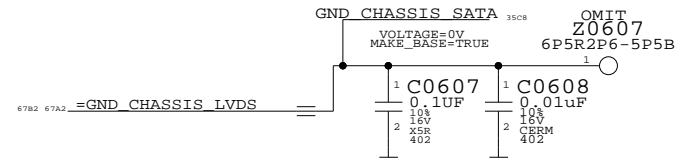
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	NONE	5	79	A

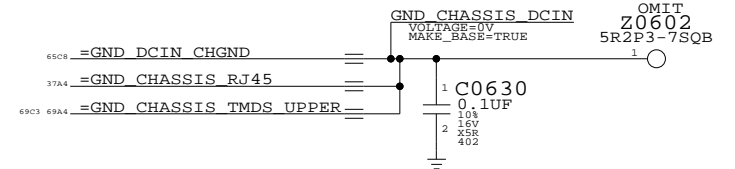
(EMI PAD FOR INVERTER CONNECTOR)



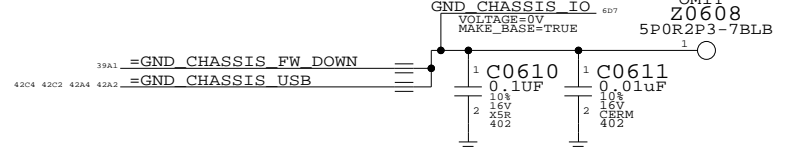
SATA, LVDS CONNECTOR CHASSIS GND



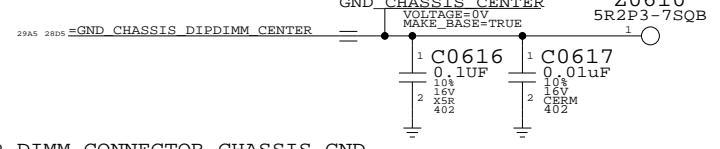
DCIN CONNECTOR CHASSIS GND



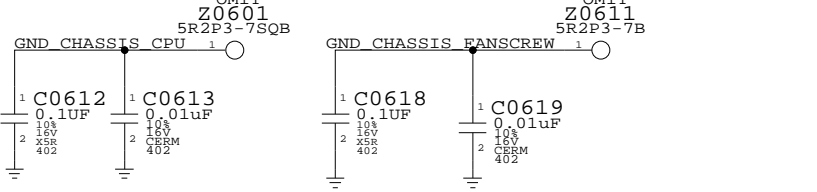
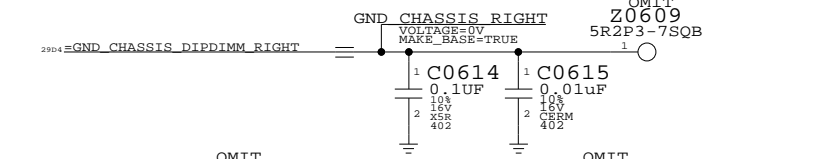
I/O CONNECTOR CHASSIS GND



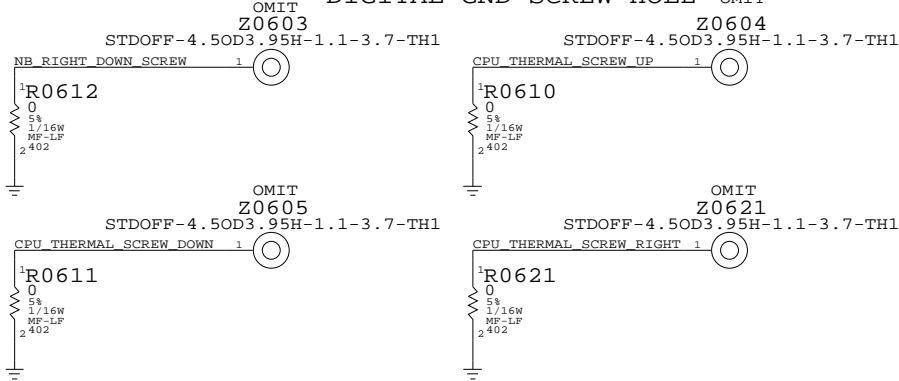
DIP DIMM CONNECTOR CHASSIS GND



DIP DIMM CONNECTOR CHASSIS GND



DIGITAL GND SCREW HOLE



LVDS ALIASES

Table mapping LVDS interface ports (e.g., LVDS B CLK N) to their respective SPN and MAKE_BASE-TRUE values.

PCI EXPRESS GRAPHICS ALIASES

Table mapping PCI Express graphics interface ports (e.g., PEG D2R N<0>) to their respective SPN and MAKE_BASE-TRUE values.

NB CFG ALIASES

Table mapping NB CFG interface ports (e.g., NB_CFG<3>) to their respective TP_NB_CFG and MAKE_BASE-TRUE values.

FIREWIRE ALIASES

Table mapping FireWire interface ports (e.g., FW_B_TPBias) to their respective SPN and MAKE_BASE-TRUE values.

SATA ALIASES

Table mapping SATA interface ports (e.g., SATA A D2R N) to their respective SPN and MAKE_BASE-TRUE values.

PCI_EXP ALIASES

Table mapping PCI Express interface ports (e.g., PCIE C D2R N) to their respective SPN and MAKE_BASE-TRUE values.

CLOCK ALIASES

Table mapping clock interface ports (e.g., CK410_SRC1_N) to their respective SPN and MAKE_BASE-TRUE values.

SB ALIASES

Table mapping SB interface ports (e.g., SUS_CLK_SB) to their respective SPN and MAKE_BASE-TRUE values.

SO-DIMM ALIASES

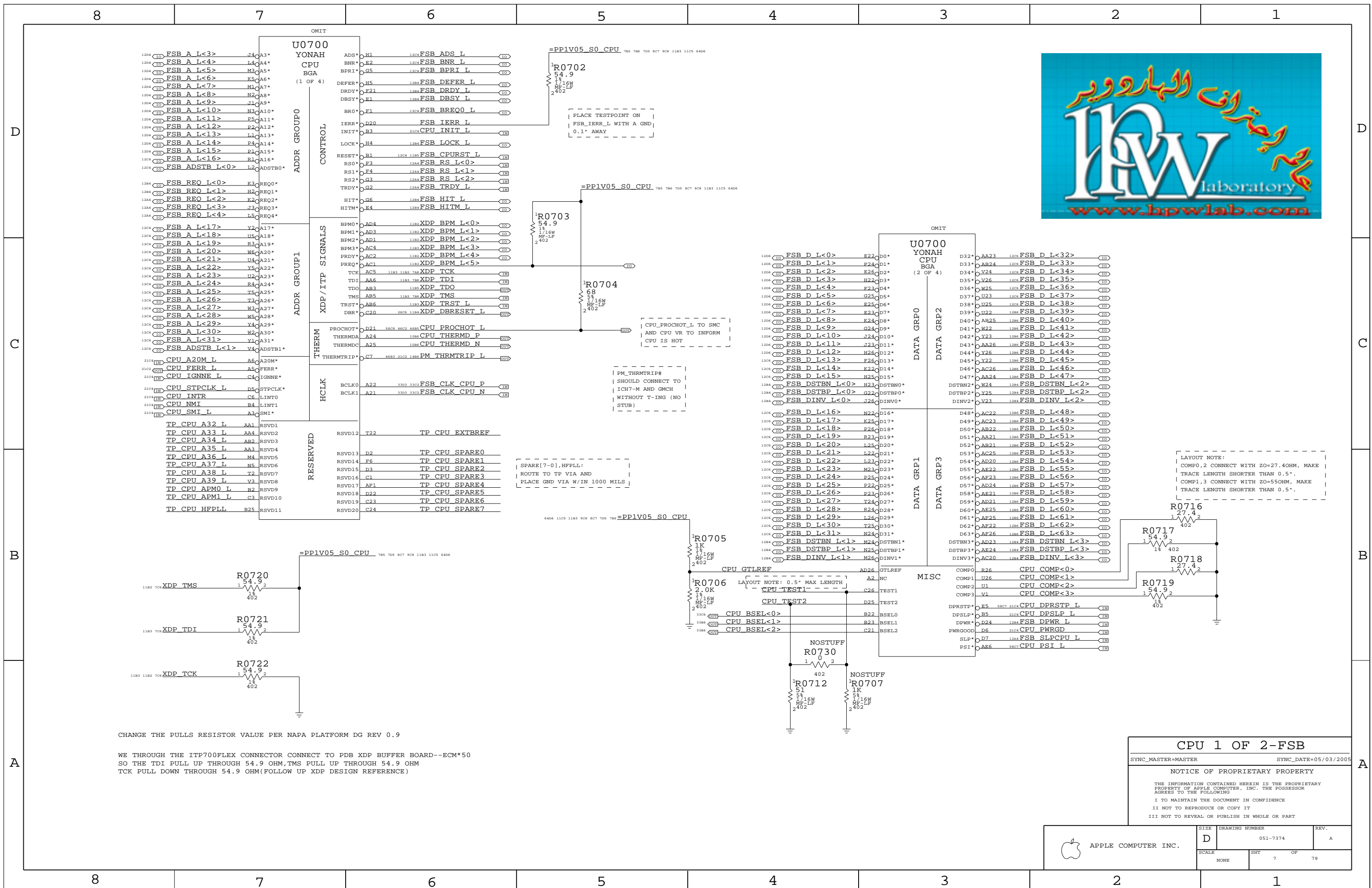
Table mapping SO-DIMM address interface ports (e.g., MEM A A<15>) to their respective SPN and MAKE_BASE-TRUE values.

Ethernet ALIASES

Table mapping Ethernet interface ports (e.g., ENET_CTRL12) to their respective SPN and MAKE_BASE-TRUE values.

Table with columns: PART#, QTY, DESCRIPTION, REFERENCE DESIGNATOR(S), BOM OPTION. Lists components like thermal standoffs.

SIGNAL ALIAS /RESET
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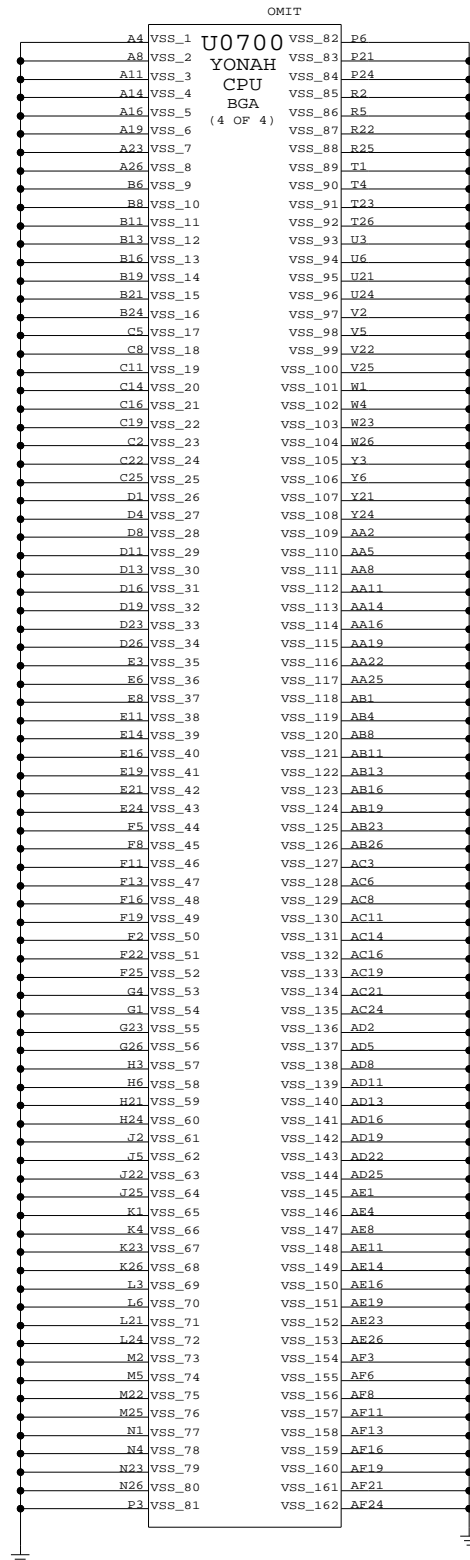
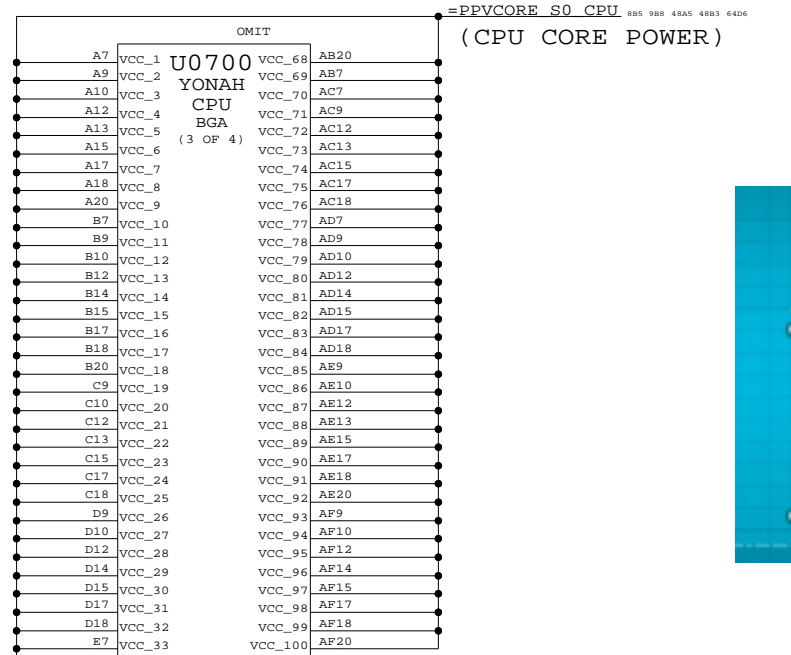
LAYOUT NOTE:
 COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50 SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB
 SYNC_MASTER=MASTER SYNC_DATE=05/03/2005
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	7		



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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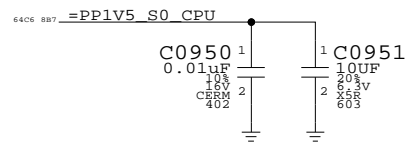
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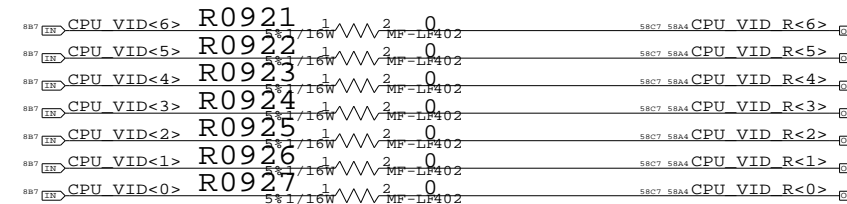
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT 8 OF 79		

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

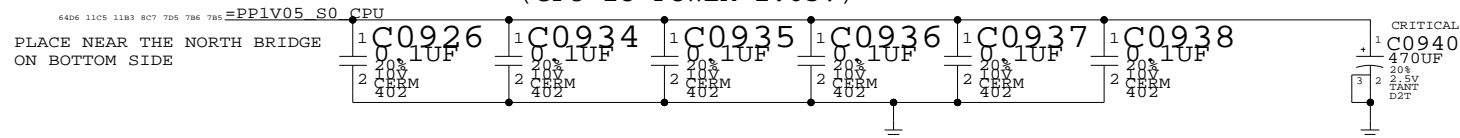
CPU CORE VID<> SETTINGS



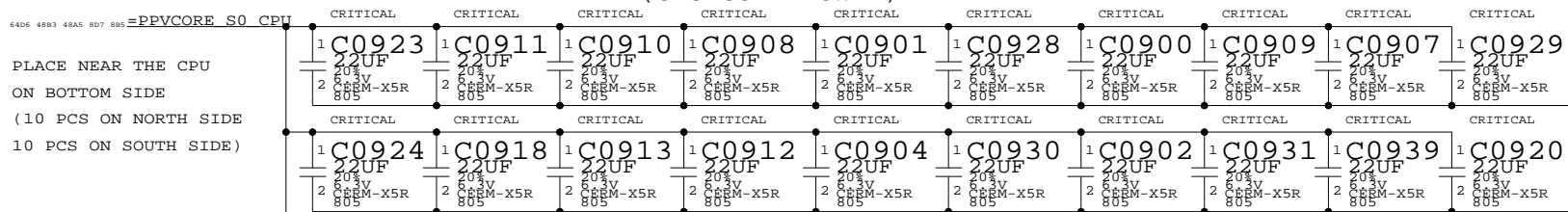
R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU, GMCH FSB BUS 1.05V



VCC CORE DECOUPLING
(CPU CORE POWER)



IF WE USE LOW ESL CAP, THEN WE CAN USE 20 PCS 22UF CAP

	MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625	1.30
	VCCLFM	TBD	TBD
SINGLE CORE SV CPU	VCCHFM	1.1625	1.30
	VCCLFM	TBD	TBD
DUAL CORE LV CPU	VCCHFM	1.0	1.1625
	VCCLFM	TBD	TBD
ULV CPU	VCCHFM	TBD	TBD
	VCCLFM	TBD	TBD

UNIT: V

- # ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
- # TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE (VCORE VOLTAGE)!
- # REFER TO YONAH PROCESSOR EMTS REV 1.0
- # VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
- # VCCLFM: VCORE AT LOWEST FREQUENCY MODE

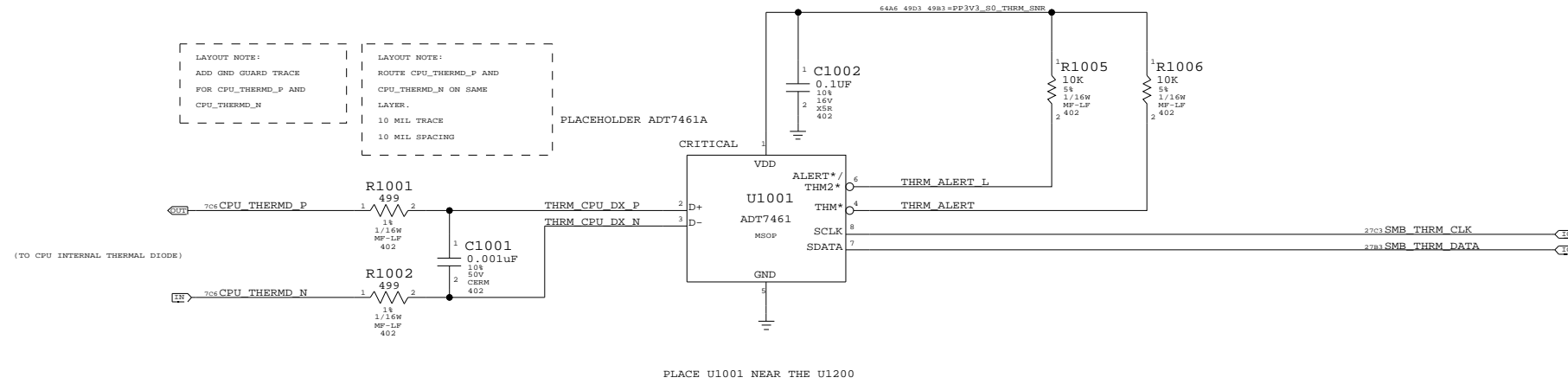
CPU DECAPS & VID<>

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SCALE	NONE	SHT	9 OF 79

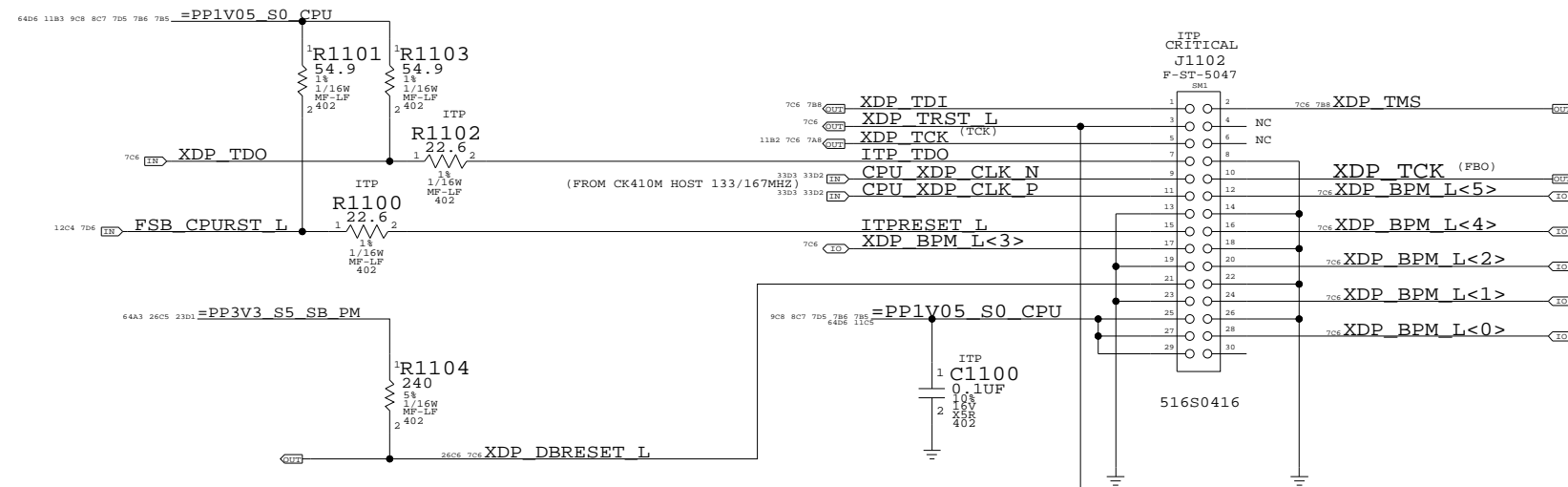
CPU ZONE THERMAL SENSOR



CPU MISC1-TEMP SENSOR	
SYNC_MASTER=ENET	SYNC_DATE=08/19/2005
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	10		

CPU ITP700FLEX DEBUG SUPPORT



(AND WITH RESET BUTTON)

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
 (DEBUG PORT ACTIVE)
 (DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
 (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
 CONNECTOR'S FBO PIN.



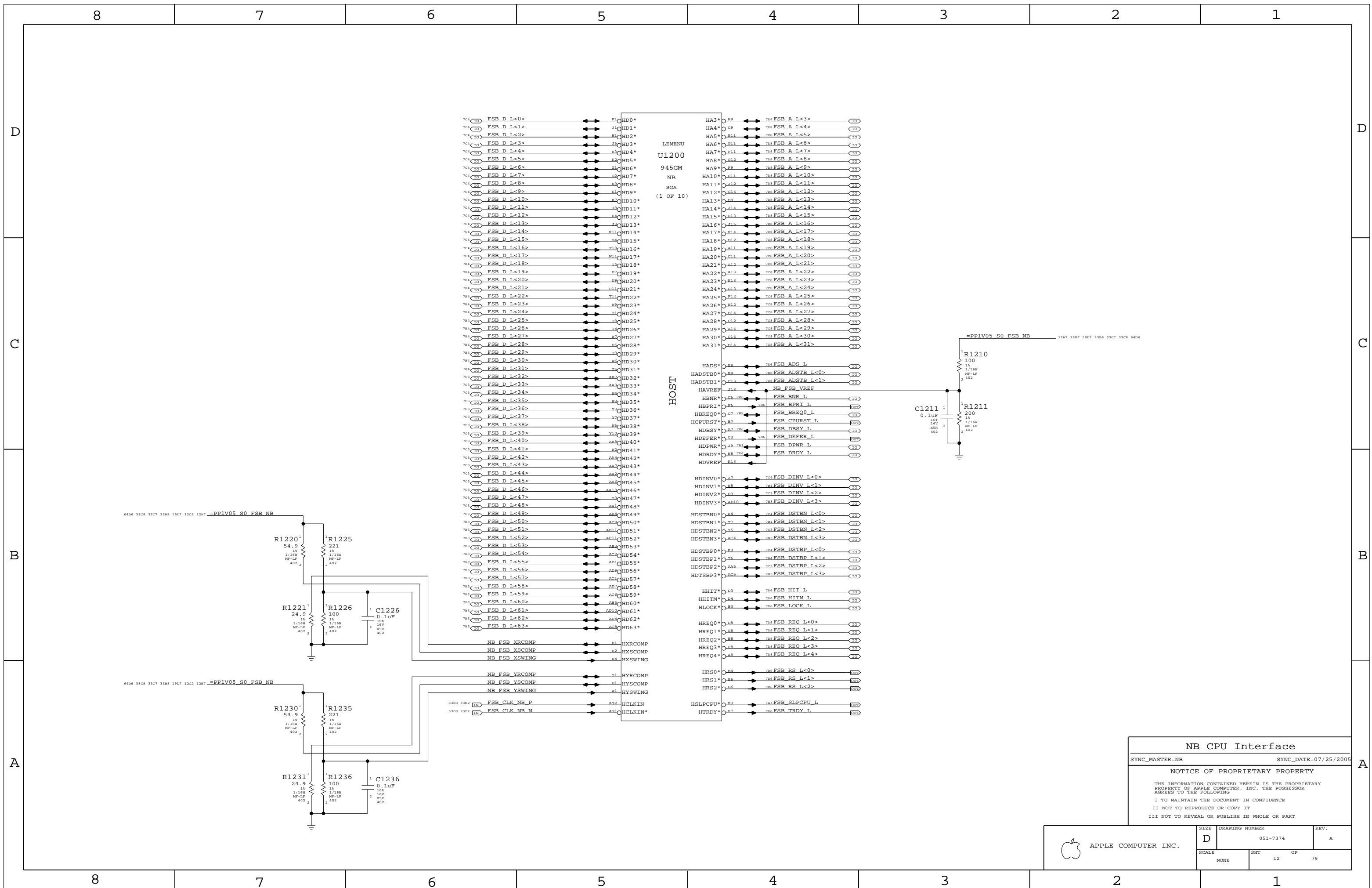
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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SCALE	SHT	OF	REV.
NONE	11	79	



NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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	SCALE NONE	SHEET 12	OF 79

LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

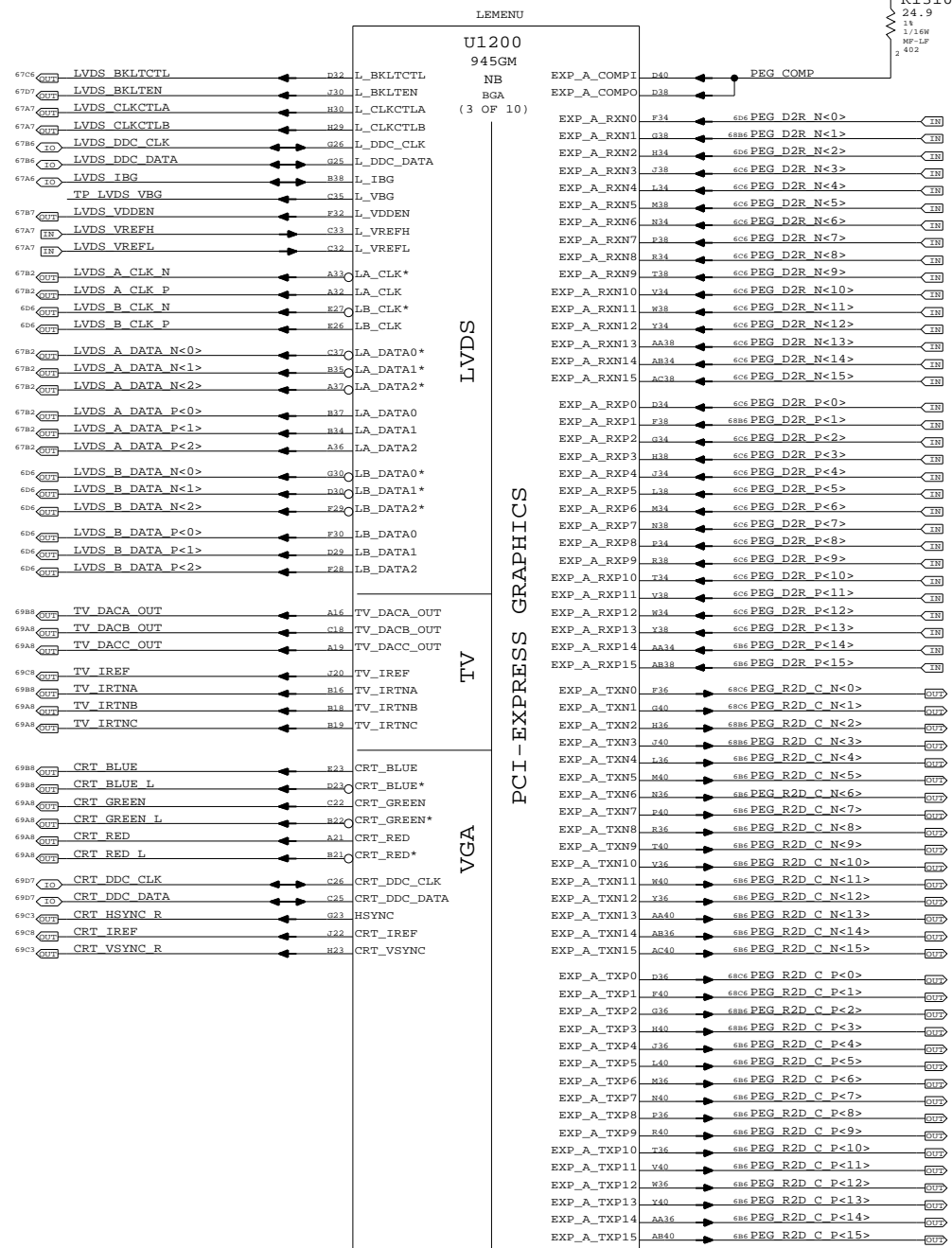
Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

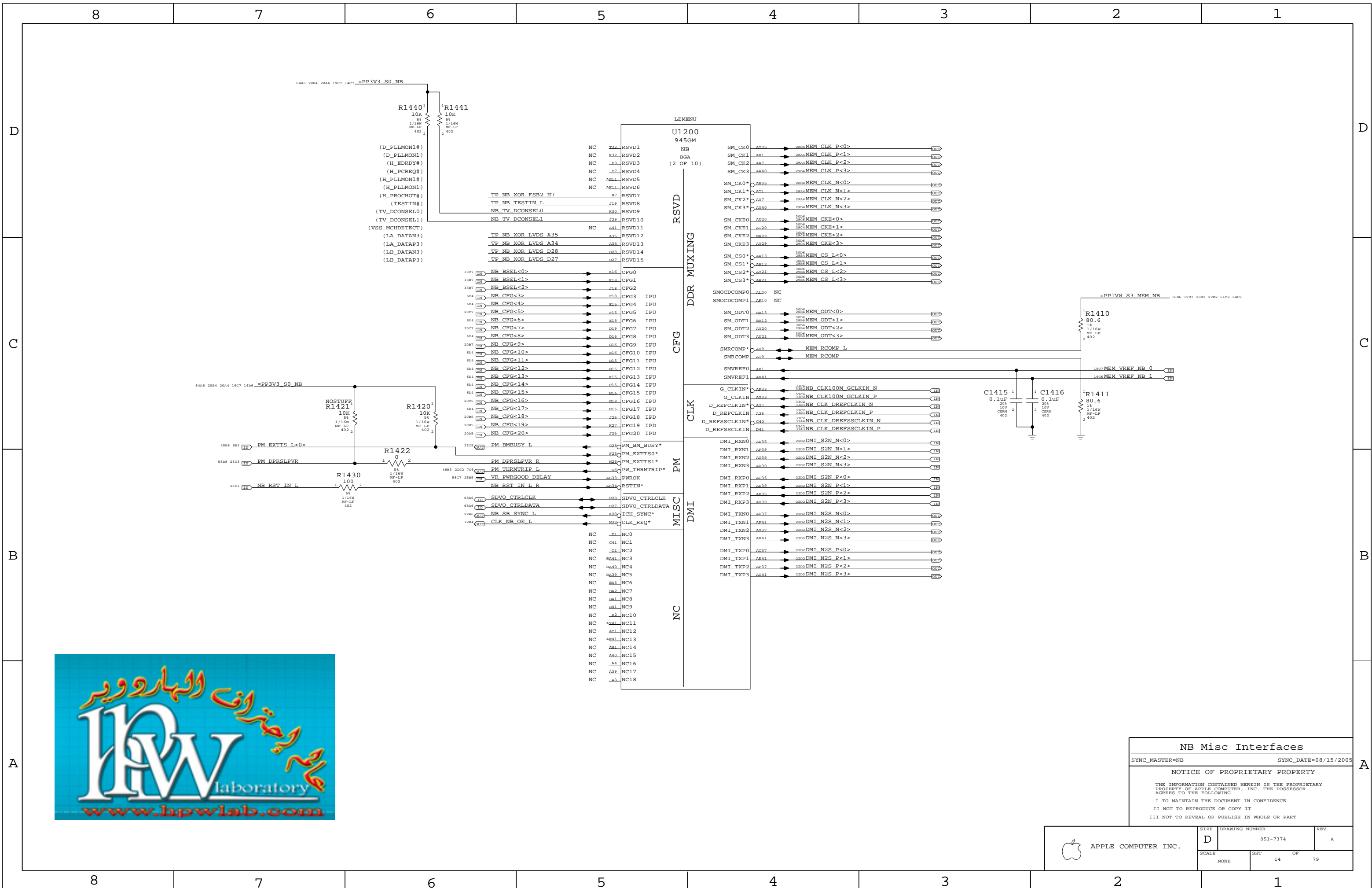
NB PEG / Video Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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SCALE	SHT	OF	79
NONE	13		



NB Misc Interfaces

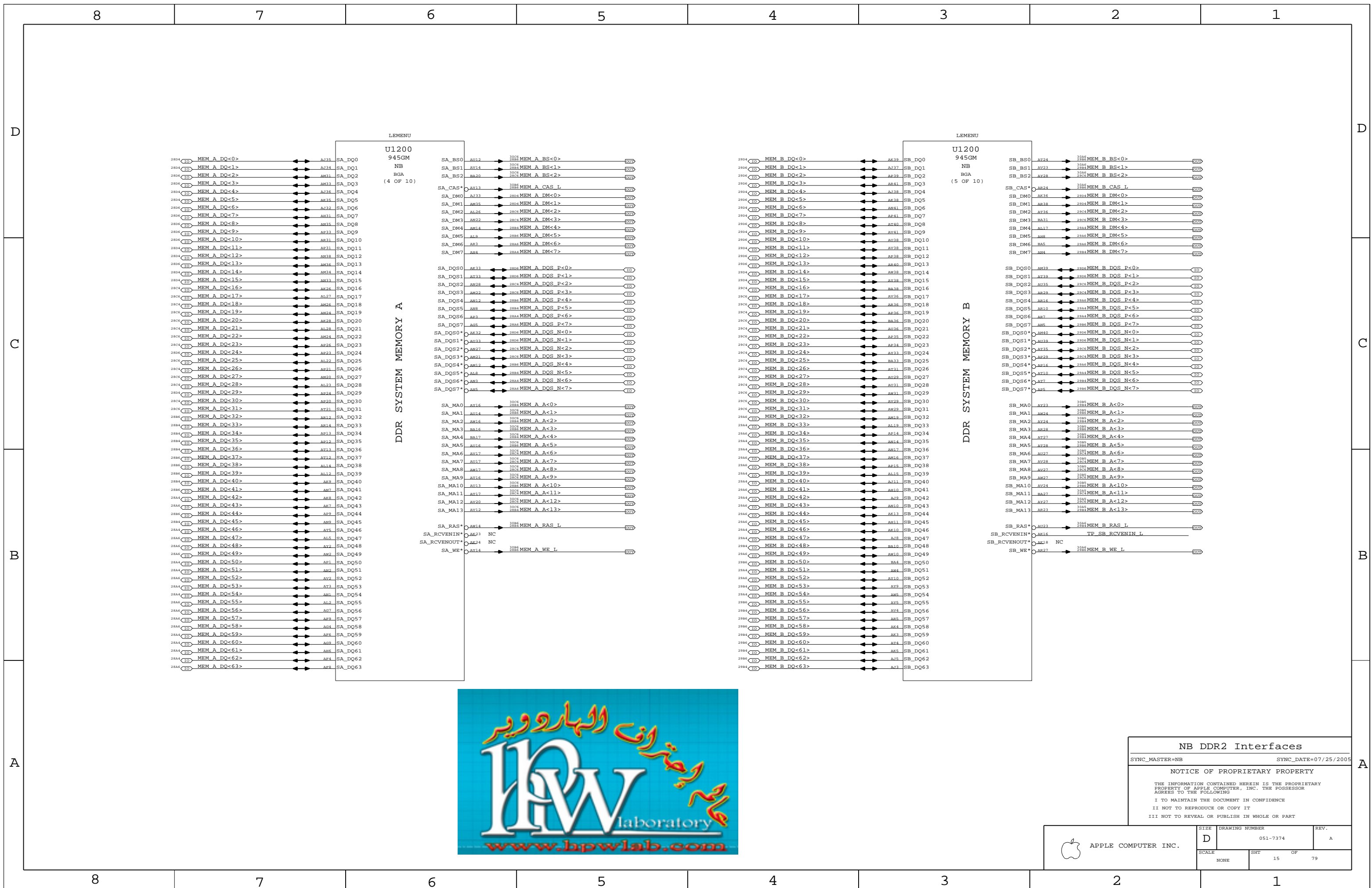
SYNC_MASTER=NB SYNC_DATE=08/15/2005

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	SCALE NONE	SHEET 14	OF 79



NB DDR2 Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

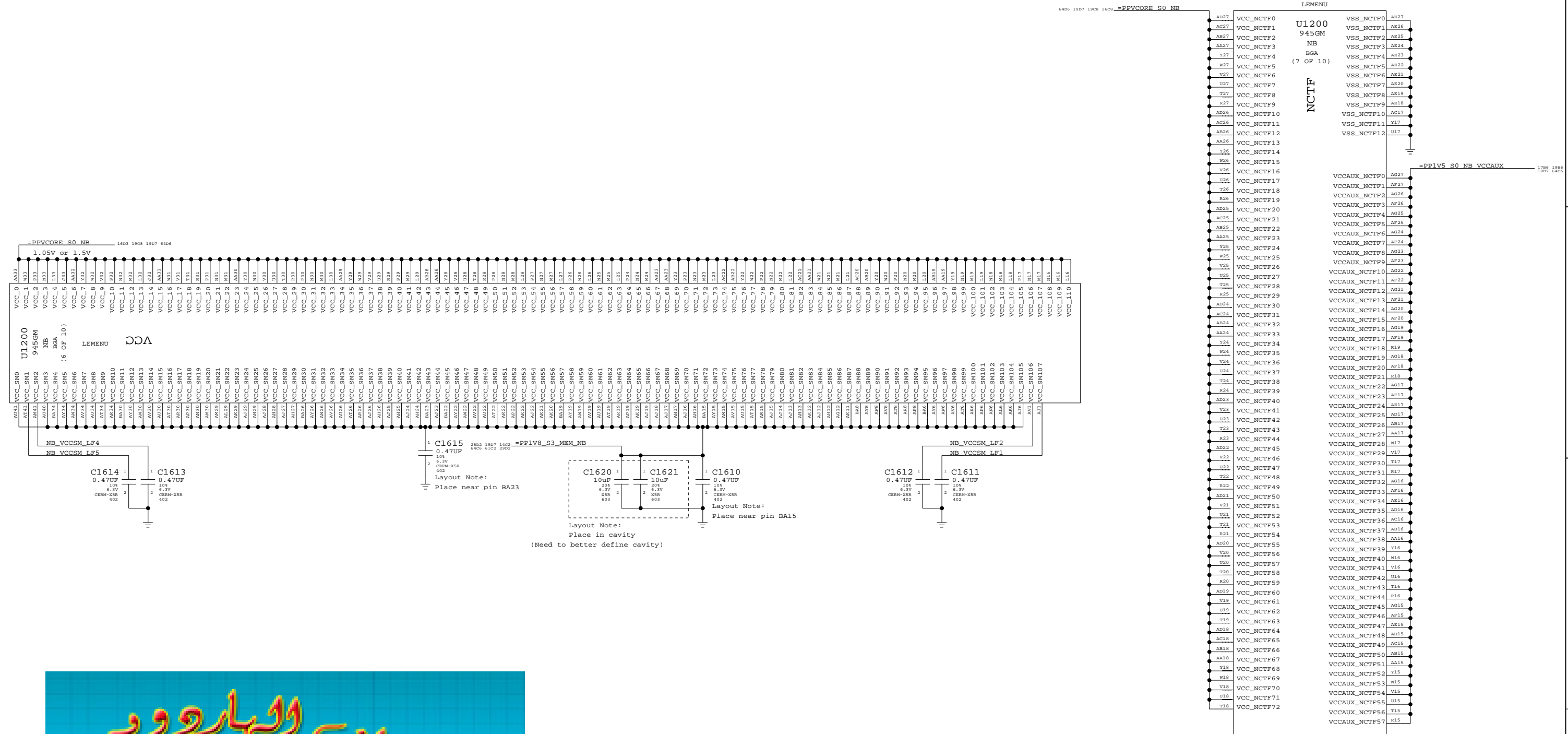
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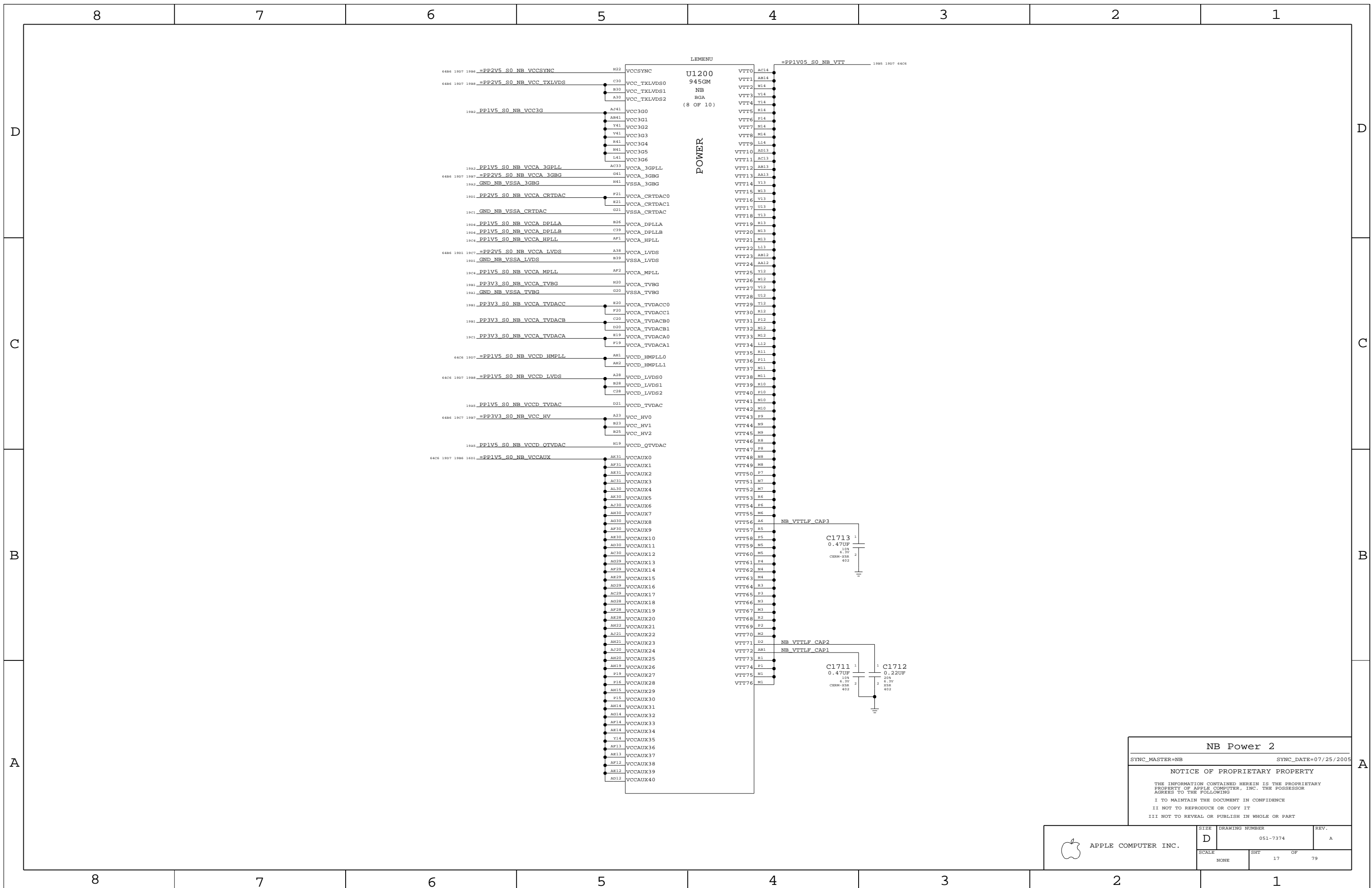
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 15	OF 79

NCTF balls are Not Critical To Function
These connections can break without impacting part performance.



NB Power 1
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SCALE	SHT	OF	REV.
NONE	16	79	



NB Power 2

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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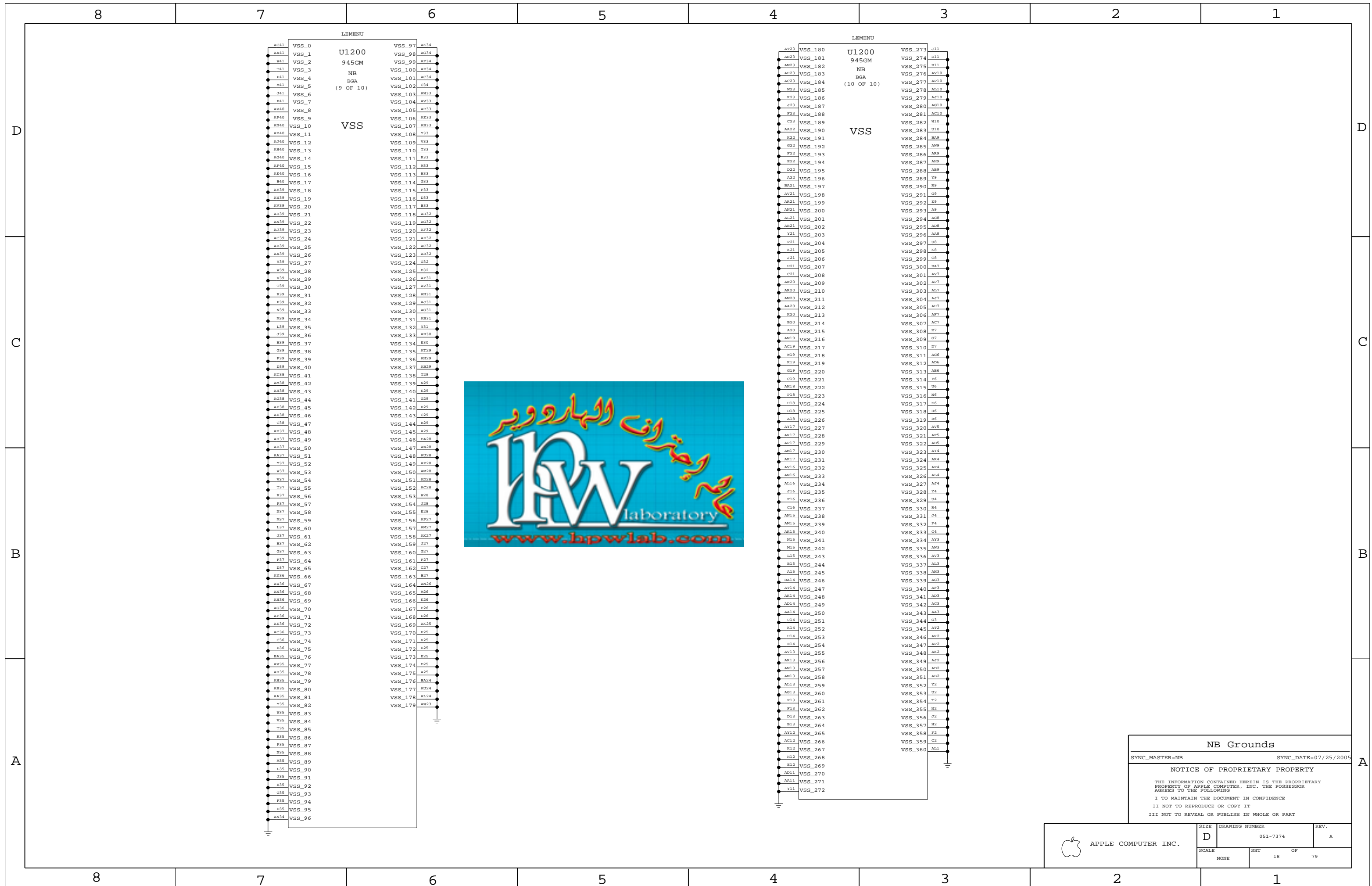
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	SCALE NONE	SHEETS 17 OF 79	



NB Grounds

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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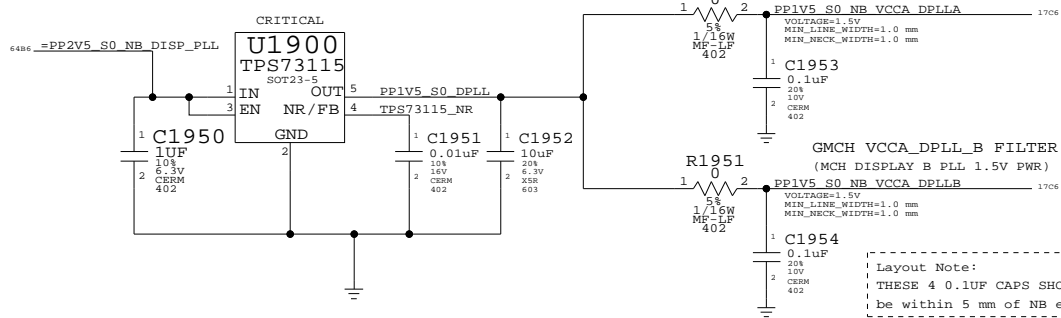
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 18	OF 79

Power Interface

These are the power signals that leave the NB "block"

PP1V05_S0_FSB_NB	1287	1287	1202	3388	3307	3308	6406
PPVCORE_S0_NB	1608	1603	1908	6406			
PP1V05_S0_NB	1901	6406					
PP1V05_S0_NB_VTT	1703	1985	6406				
PP1V5_S0_NB	1901	6406					
PP1V5_S0_NB_PCIE	1302	6406					
PP1V5_S0_NB_PLL	1908	6406					
PP1V5_S0_NB_TVDAC	1988	6406					
PP1V5_S0_NB_VCCD_HMPLL	1706	1988	6406				
PP1V5_S0_NB_VCCD_LVDS	1706	1988	6406				
PP1V5_S0_NB_VCCAUX	1601	1786	1986	6406			
PP1V8_S3_MEM_NB	1402	1686	2802	2902	6102	6406	
PP2V5_S0_NB_CRTDAC	1904	6486					
PP2V5_S0_NB_VCCSYNC	1706	1986	6486				
PP2V5_S0_NB_VCC_TXLVDS	1706	1988	6486				
PP2V5_S0_NB_VCCA_3GBG	1706	1987	6486				
PP2V5_S0_NB_VCCA_LVDS	1706	1901	6486				
PP3V3_S0_NB	1407	1406	20A4	2084	6084	6486	
PP3V3_S0_NB_VCC_HV	1706	1987	6486				
PP5V_S0_NB_TVDAC	1904	6403					

MCH DISPLAY PLL POWER LDO

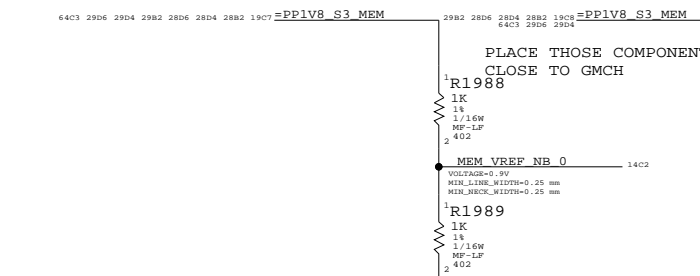


MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)

GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)



GMCH CORE PWR 1.05V BYPASS
THIS 470UF FOR GMCH CORE 1.05V

GMCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

MCH VCCSYNC BYPASS
(MCH H/V SYNC 2.5V PWR)

MCH VTT BYPASS
(MCH FSB 1.05V PWR) (SHARE C0940 470UF)

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

GMCH VCCD_TV DAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)

GMCH VCCD_QTV DAC FILTER
(MCH TVDAC DIGITAL QUIET 1.5V PWR)

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSI0&IO PWR 1.5V)

GMCH VCCD_TV DAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)

GMCH VCCD_QTV DAC FILTER
(MCH TVDAC DIGITAL QUIET 1.5V PWR)

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)

Layout Note:
This 0.1uF cap should be within 5 mm of NB edge

Layout Note: Route to caps, then GND

Layout Note:
THESE 4 0.1uF CAPS SHOULD be within 5 mm of NB edge

Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

Layout Note:
These 8 caps should be within 6.35 mm of NB edge

Layout Note:
Place L and C close to MCH

Layout Note:
Place in cavity

Layout Note:
10uF caps should be close to MCH on opposite side.

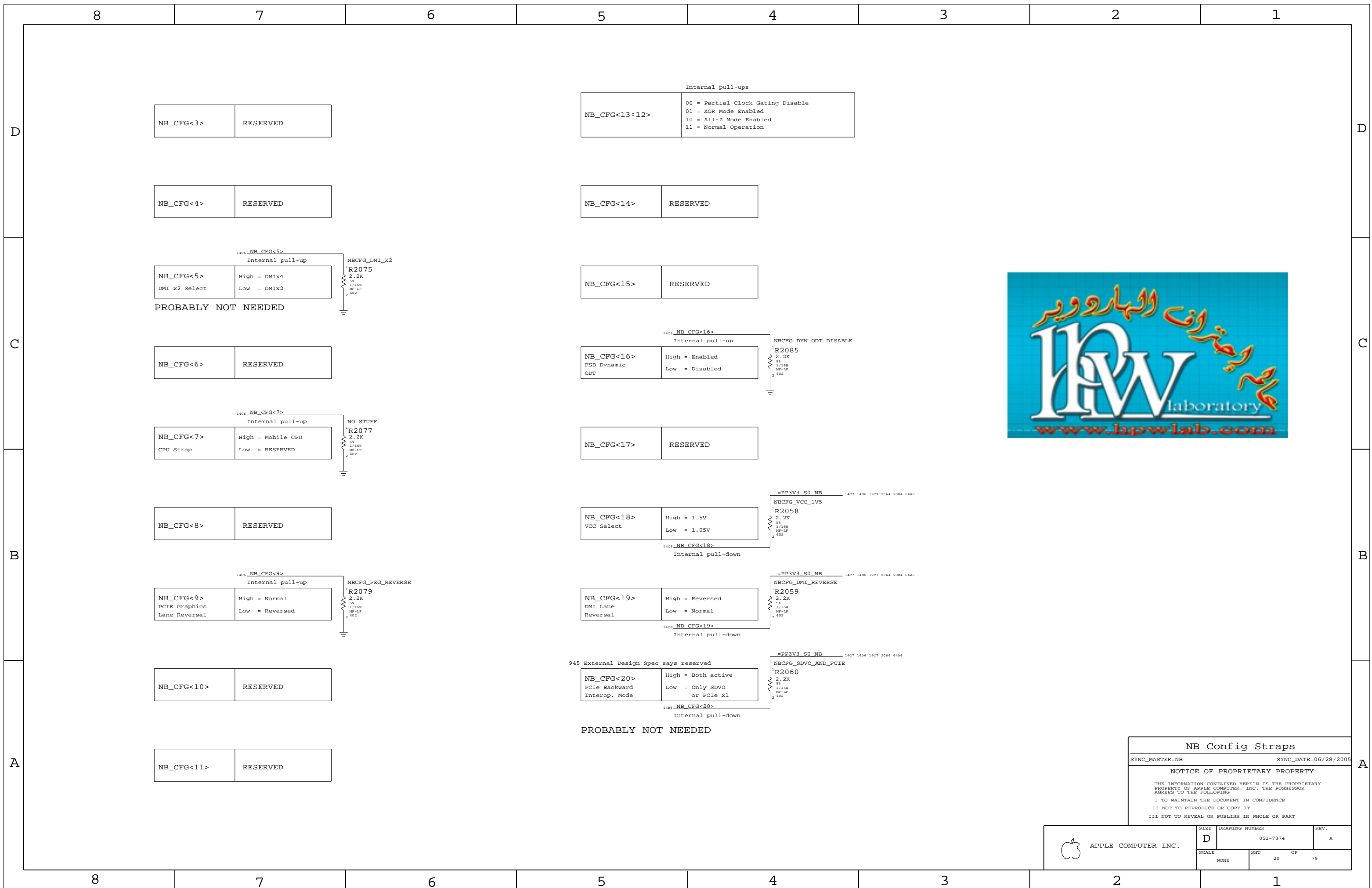
Layout Note:
These 4 caps should be within 6.35 mm of NB edge

Layout Note:
3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

NB (GM) Decoupling		
SYNC_MASTER=NB		SYNC_DATE=06/22/2005
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	19		



NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<13:12>	Internal pull-ups 00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	---

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

1406 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
PROBABLY NOT NEEDED	

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

1406 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled

1406 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
NO STUFF	

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

1406 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V

1406 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

1406 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved	
1486 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED



NB Config Straps

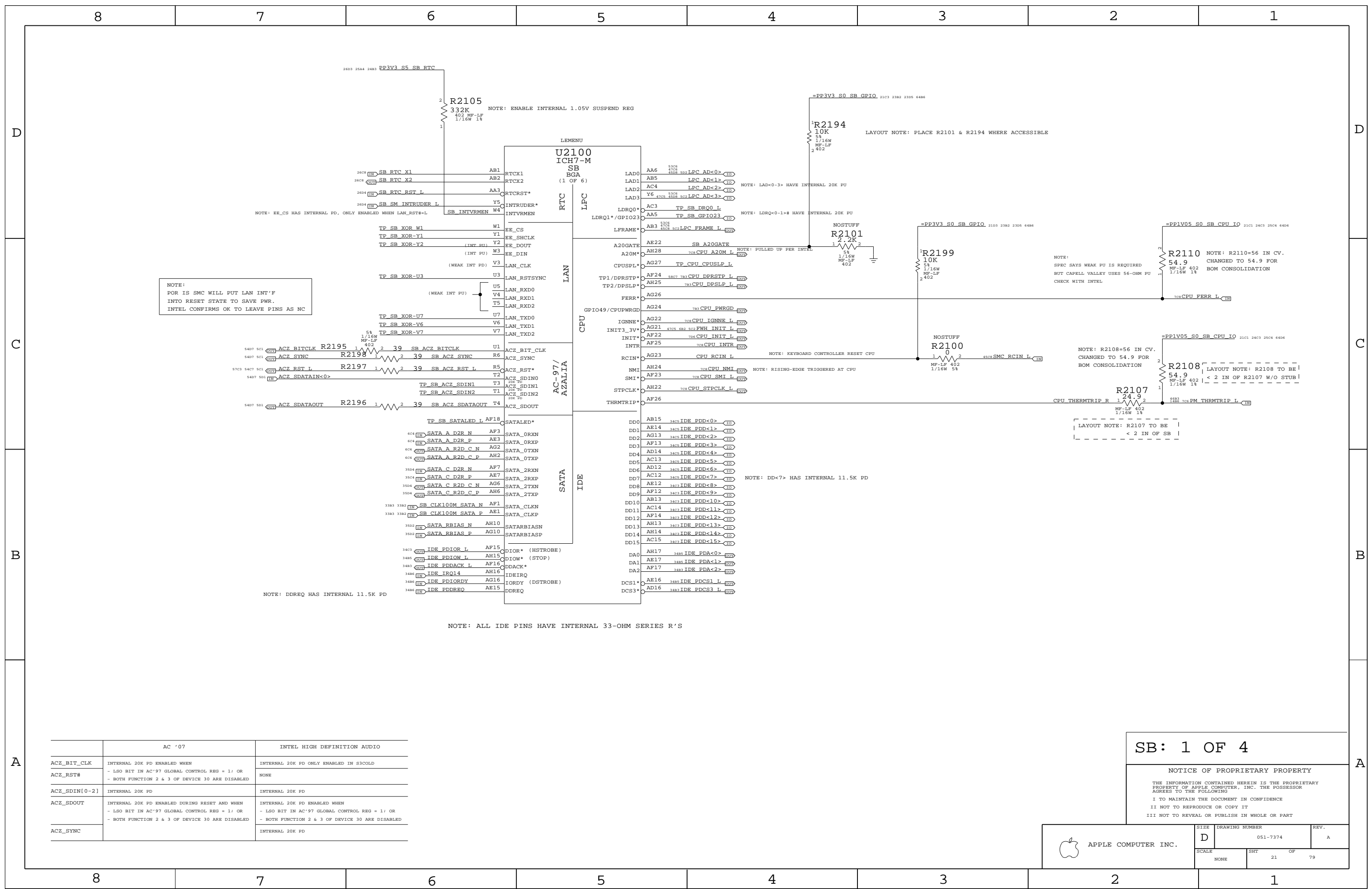
SYNC_MASTER=NB SYNC_DATE=06/28/2005

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	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	20	79	



NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: ER_CS HAS INTERNAL PD, ONLY ENABLED WHEN LAN_RST# = L

NOTE: LAD<0-3> HAVE INTERNAL 20K PU

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: PULLED UP PER INTEL

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: RISING-EDGE TRIGGERED AT CPU

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE:
SPEC SAYS WEAK PU IS REQUIRED
BUT CAPELL VALLEY USES 56-OHM PU
CHECK WITH INTEL

NOTE: R2108=56 IN CV.
CHANGED TO 54.9 FOR
BOM CONSOLIDATION

LAYOUT NOTE: R2107 TO BE
< 2 IN OF SB

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

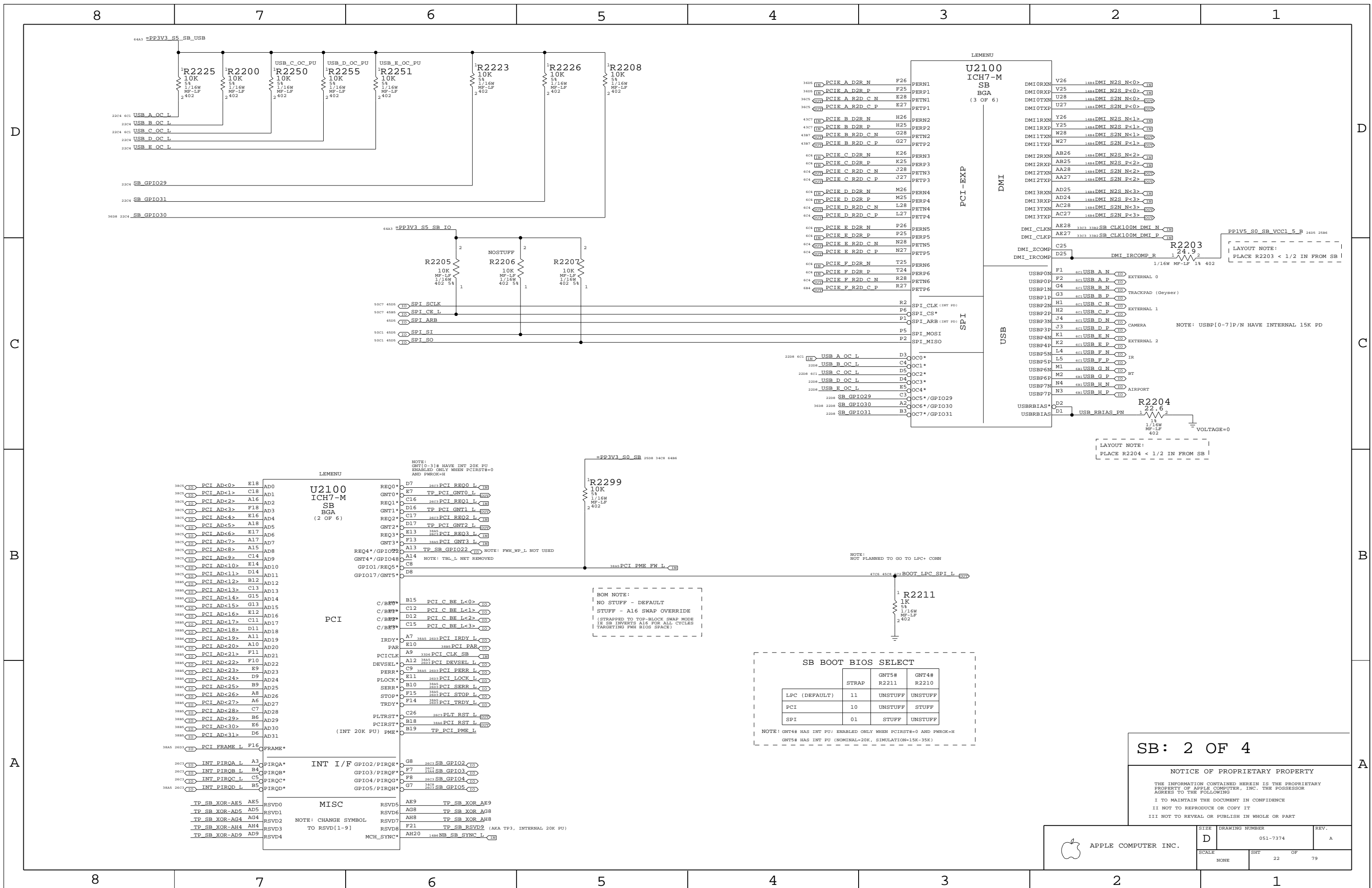
	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD	INTERNAL 20K PD

SB: 1 OF 4

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SCALE	NONE	SHT	21 OF 79



SB: 2 OF 4

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 22	OF 79

SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

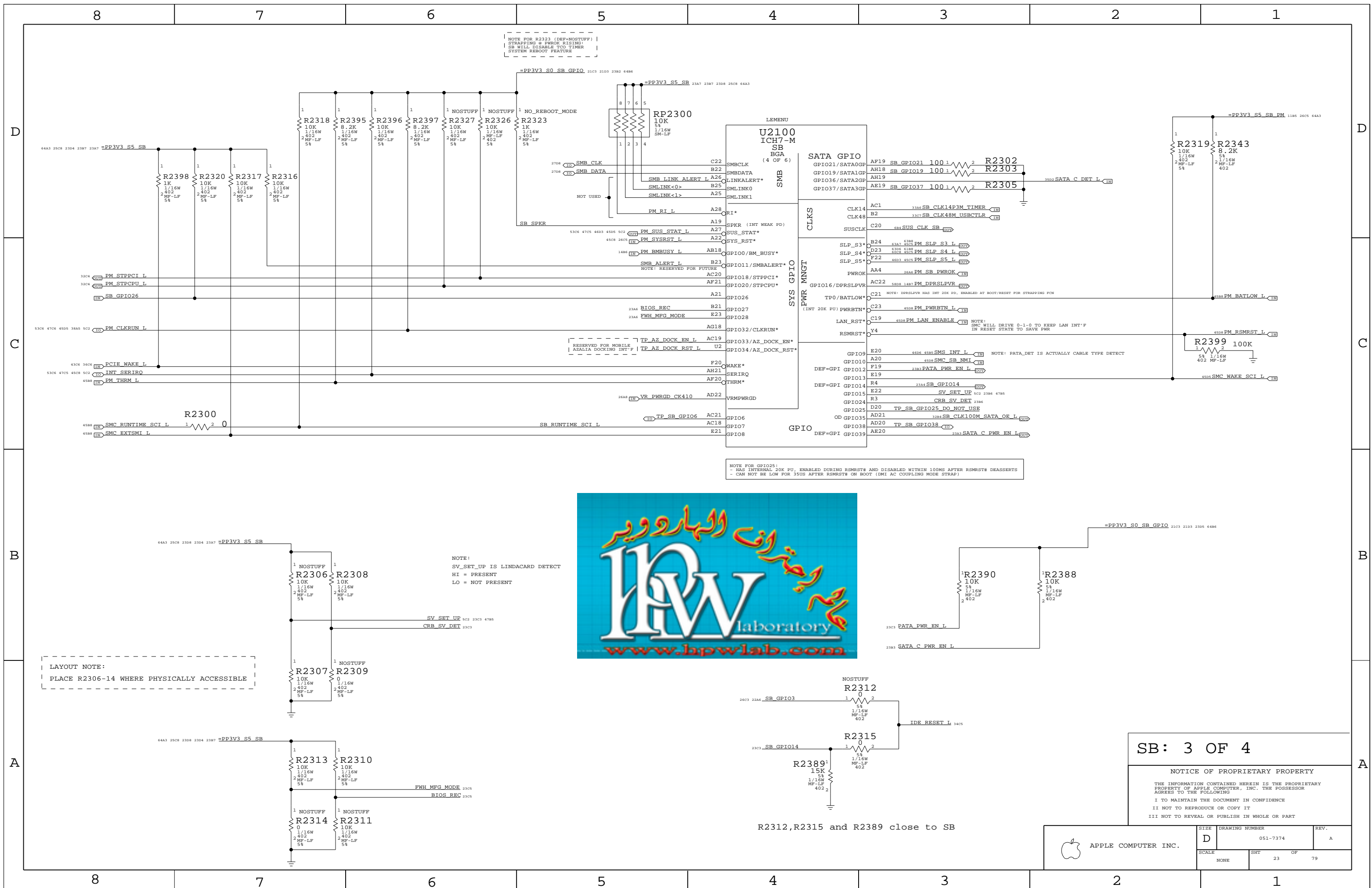
NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST#0 AND FWROK#H
 GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

BOM NOTE:
 NO STUFF - DEFAULT
 STUFF - A16 SWAP OVERRIDE
 (STRAPPED TO TOP-BLOCK SWAP MODE
 IF SB INVERTS A16 FOR ALL CYCLES
 (TARGETING FWB BIOS SPACE))

NOTE: CHANGE SYMBOL
 TO RSV[1-9]

INT I/F	GPIO2/PIRQ*	GPIO3/PIRQ*	GPIO4/PIRQ*	GPIO5/PIRQ*
INT_PIRQA_L	A3	F7	F8	G7
INT_PIROB_L	B4	F7	F8	G7
INT_PIROC_L	C5	F7	F8	G7
INT_PIROD_L	B5	F7	F8	G7

MISC	RSVD5	RSVD6	RSVD7	RSVD8	RSVD4
TP_SB_XOR-AE5	AE5	AG8	F21	AH20	
TP_SB_XOR-AD5	AD5	AG8	F21	AH20	
TP_SB_XOR-AG4	AG4	AG8	F21	AH20	
TP_SB_XOR-AH4	AH4	AG8	F21	AH20	
TP_SB_XOR-AD9	AD9	AG8	F21	AH20	



NOTE FOR R2323 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

NOTE FOR GPIO25:
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (EMI AC COUPLING MODE STRAP)



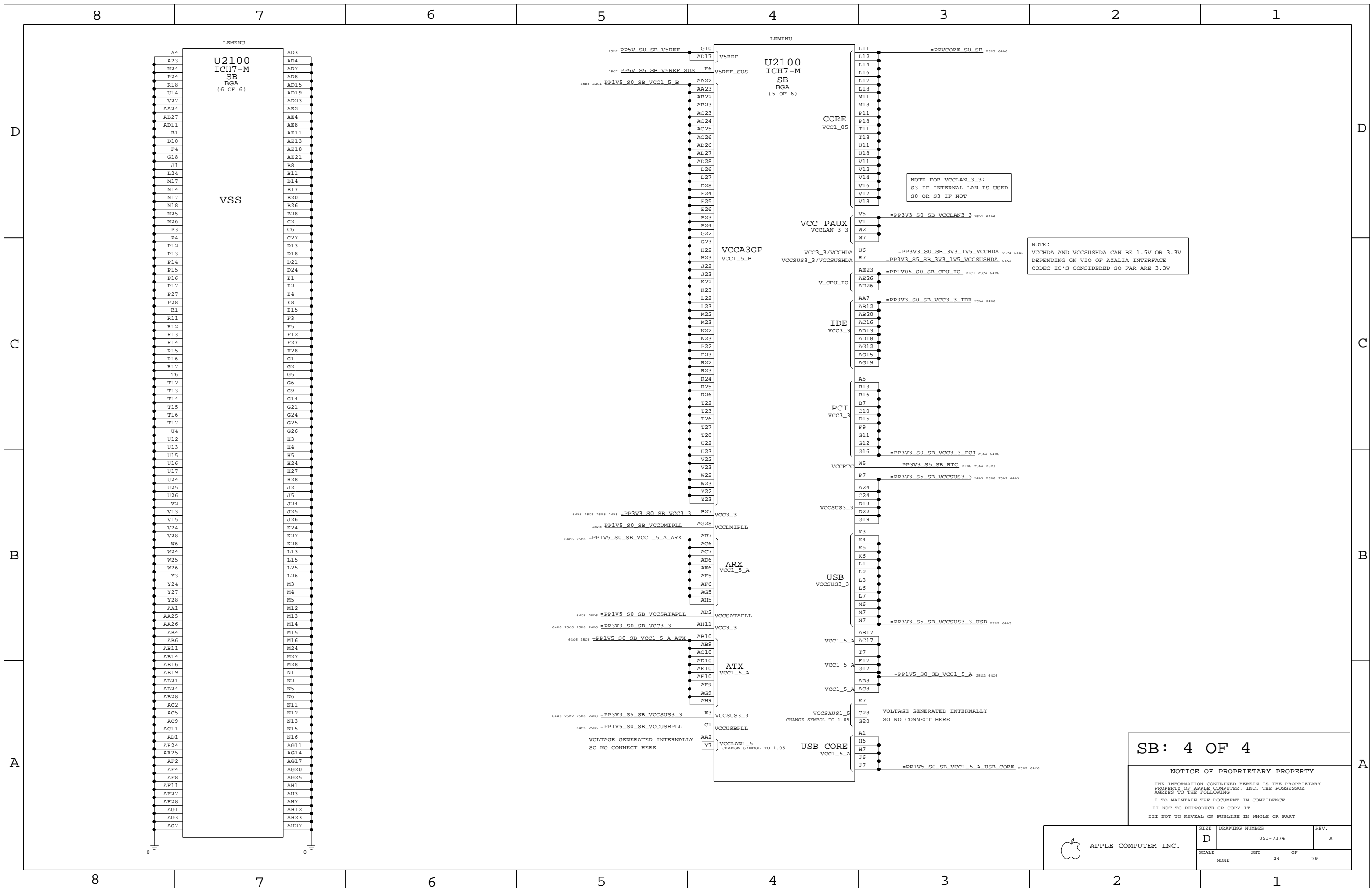
LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

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	D	051-7374	A
SCALE	SHT	OF	79
NONE	23		

R2312, R2315 and R2389 close to SB



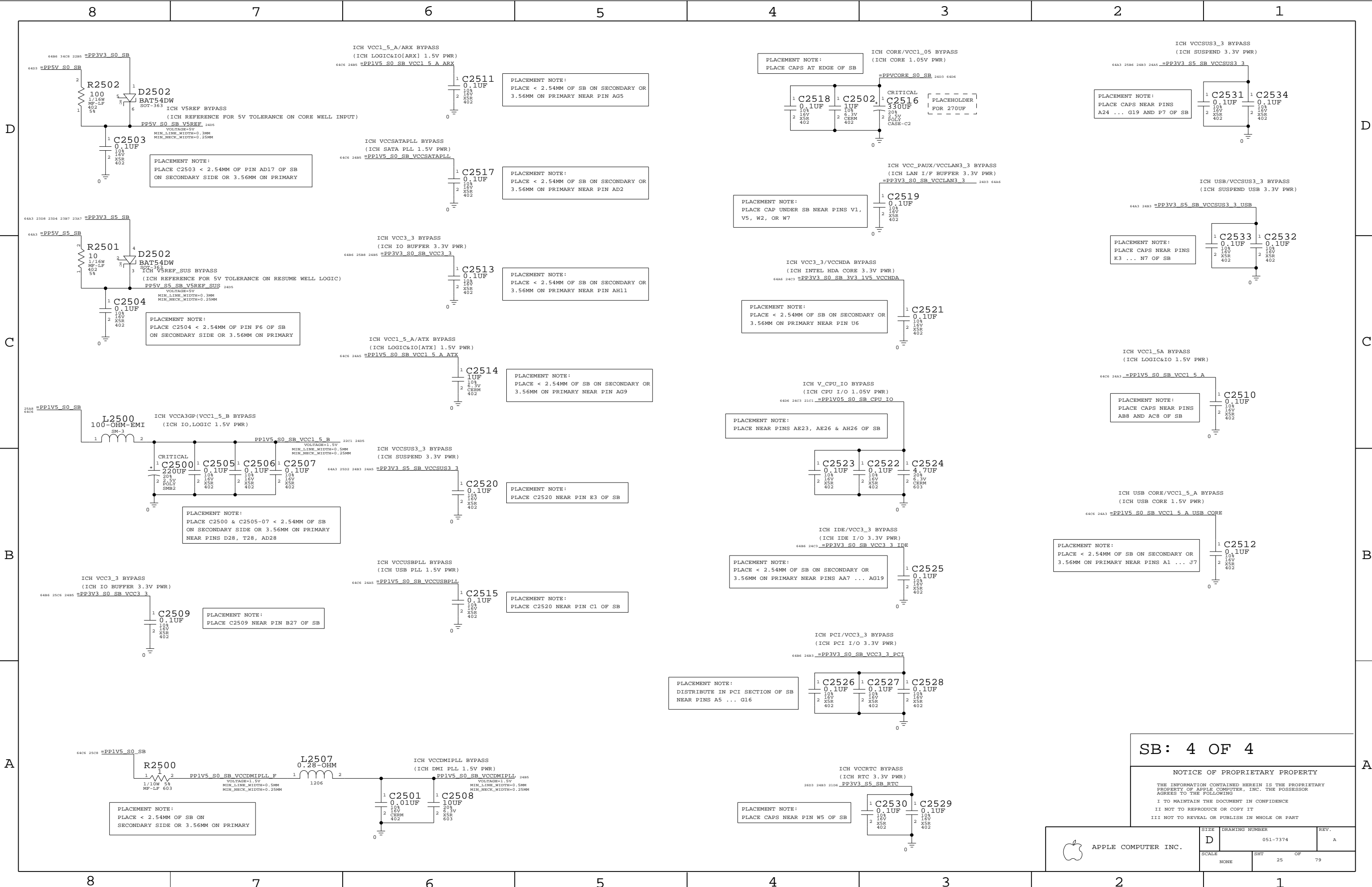
NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCCHDA AND VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

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	D	051-7374	A
SCALE	SHT	OF	
NONE	24	79	



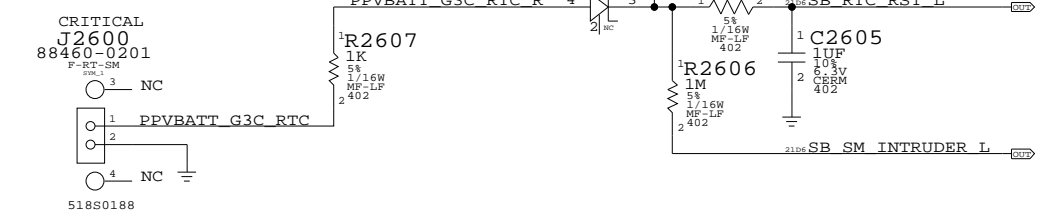
SB: 4 OF 4

NOTICE OF PROPRIETARY PROPERTY

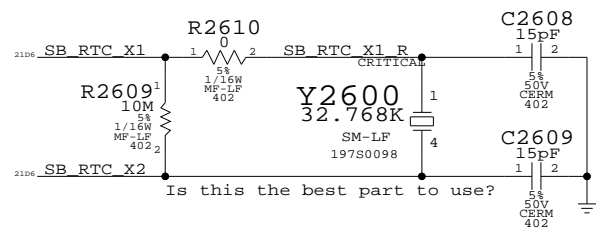
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	25		

RTC Battery Connector



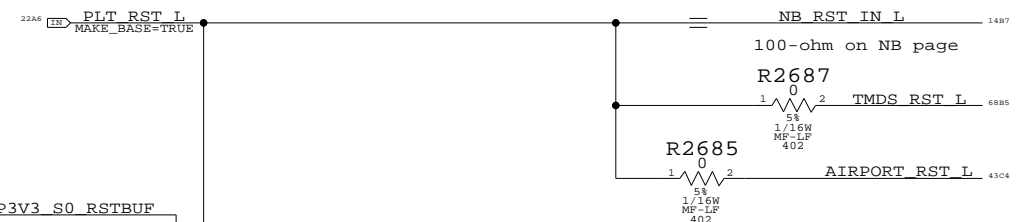
SB RTC Crystal Circuit



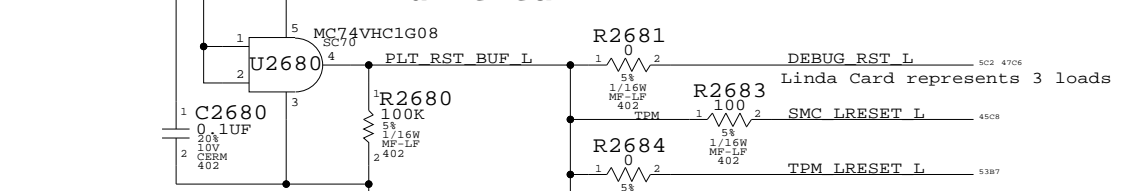
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.
Silk: "SYS RST"

Platform Reset Connections

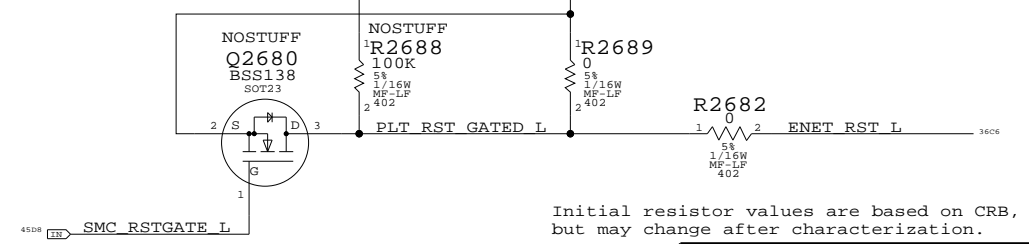
Unbuffered



Buffered



Gated



SB Misc

SYNC_MASTER=NB SYNC_DATE=07/26/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	26		

8

7

6

5

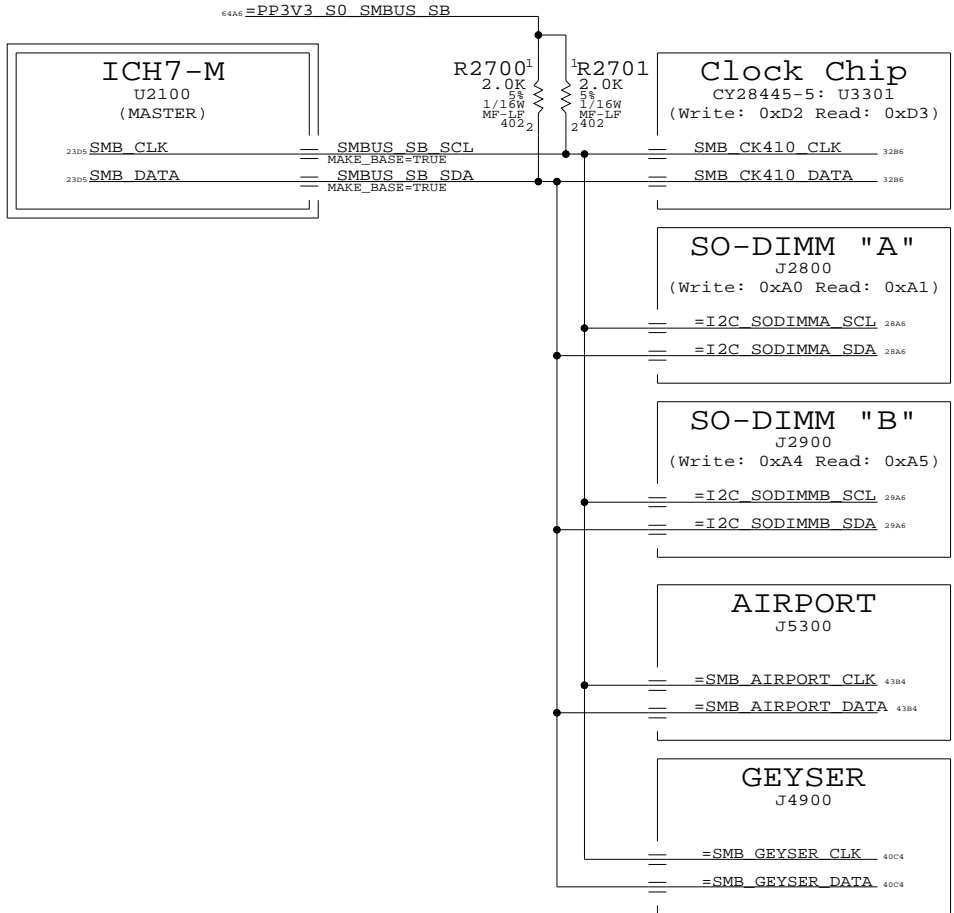
4

3

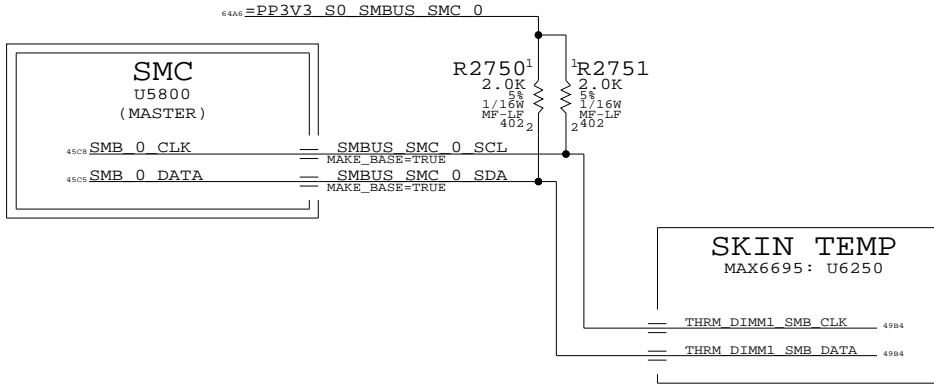
2

1

ICH7-M SMBus Connections

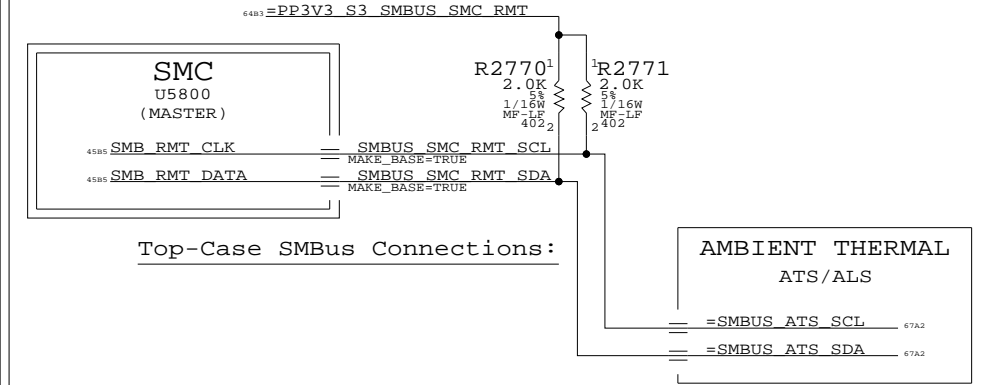


SMC "0" SMBus Connections

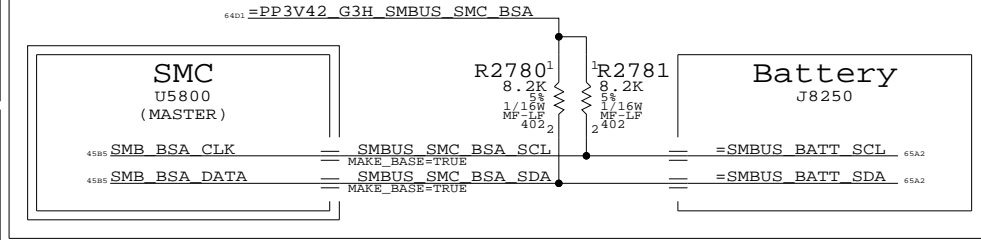


SMC "RMT" SMBus Connections

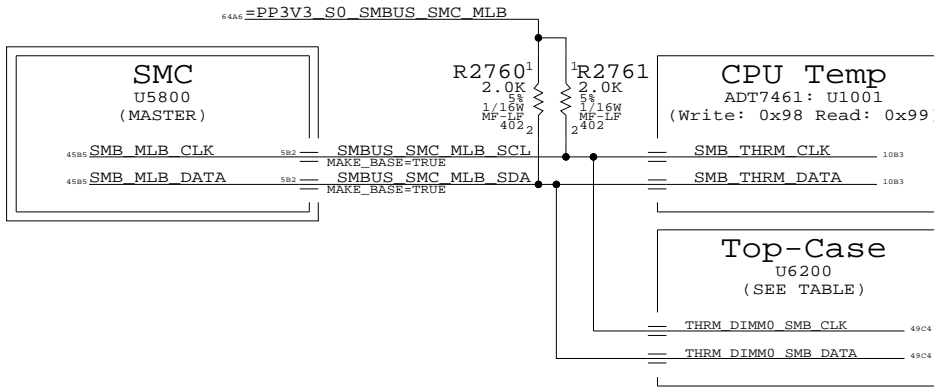
NOTE: SMC RMT bus remains powered and may be active in S3 state



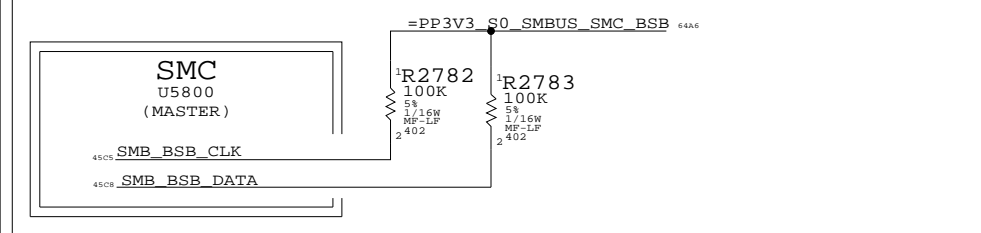
SMC "Battery A" SMBus Connections



SMC "MLB" SMBus Connections



SMC "Battery B" SMBus Connections



M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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	D	051-7374	A
SCALE	SHT	OF	79
NONE	27		

8

7

6

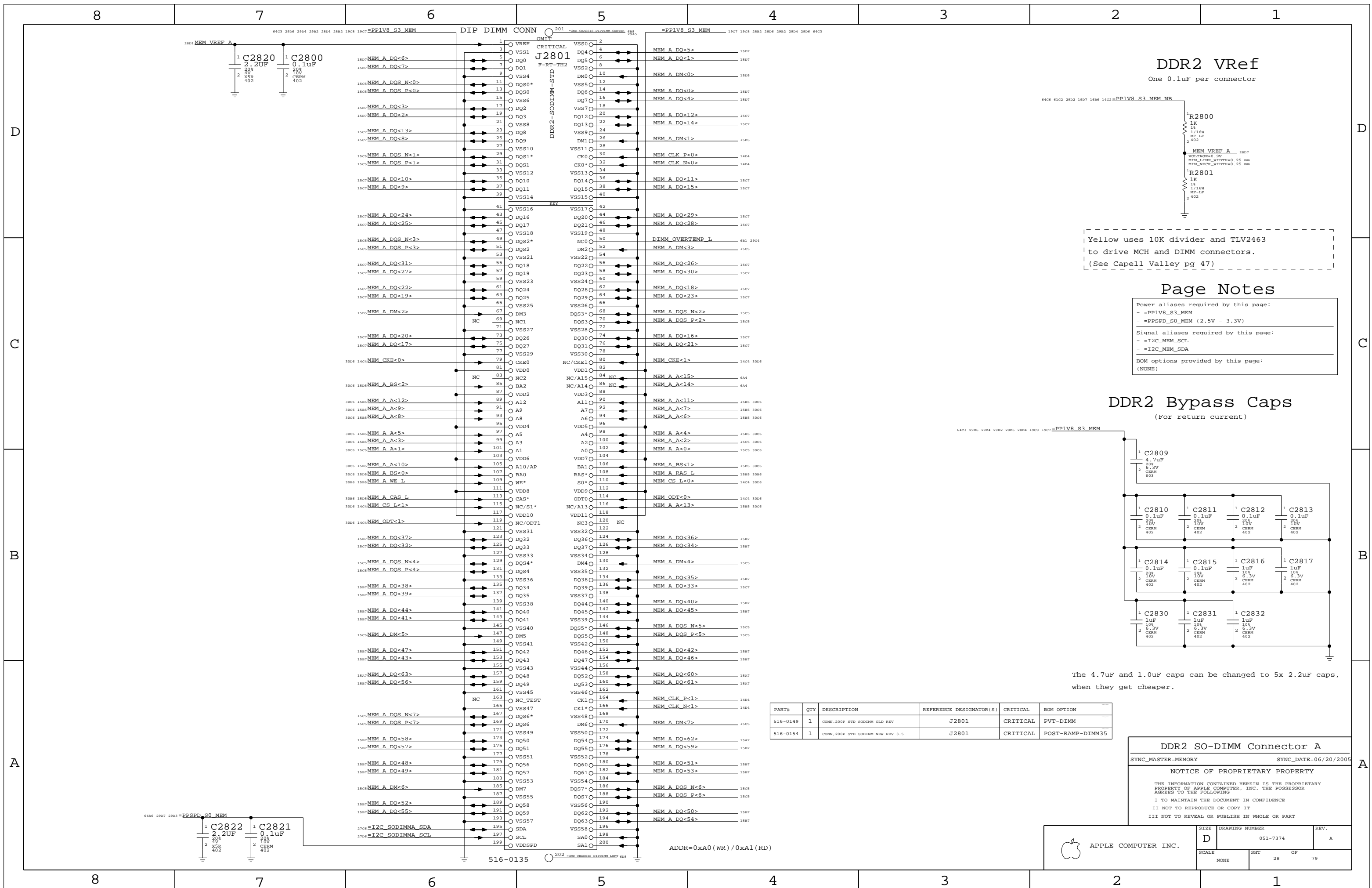
5

4

3

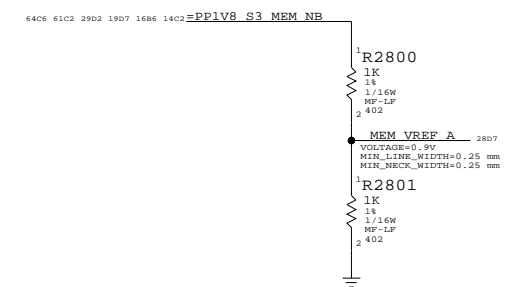
2

1



DDR2 VRef

One 0.1uF per connector



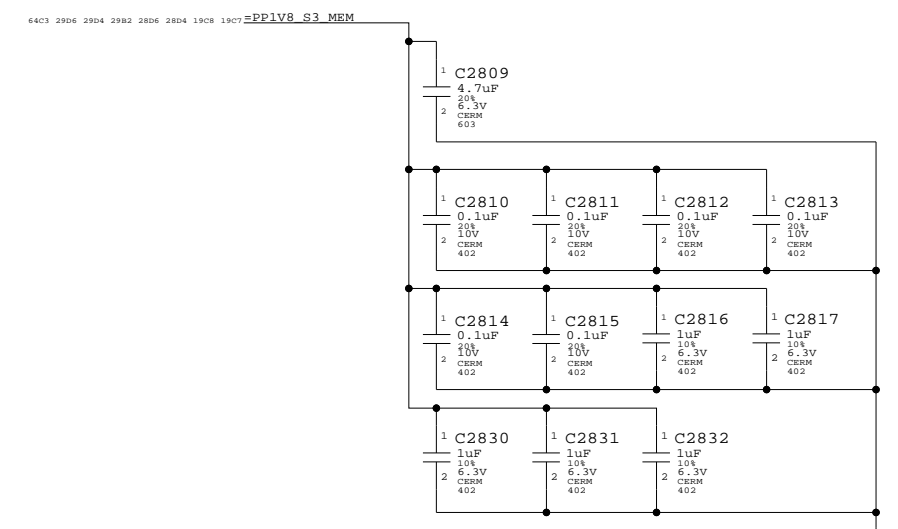
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

Page Notes

- Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA
- BOM options provided by this page:
 - (NONE)

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector A

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

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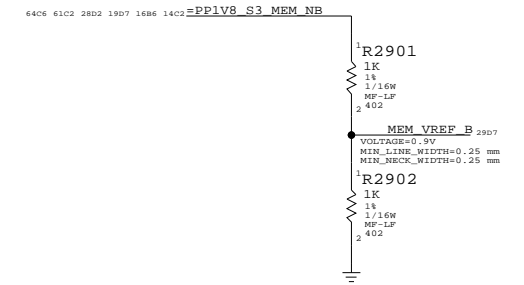
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	28		

ADDR=0xA0 (WR) / 0xA1 (RD)

DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector



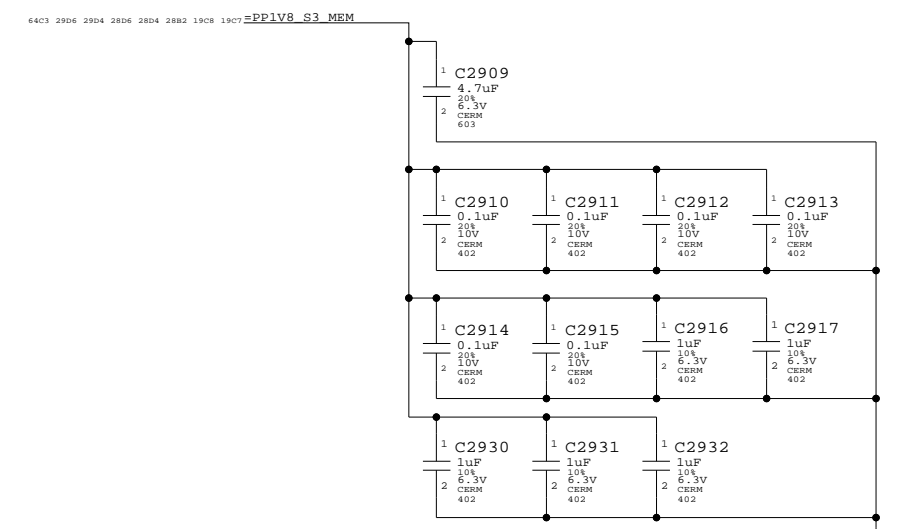
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

Page Notes

- Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
 - Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA
 - BOM options provided by this page:
 - (NONE)
- NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0145	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 1.5	J2901	CRITICAL	POST-RAMP-DIMM35

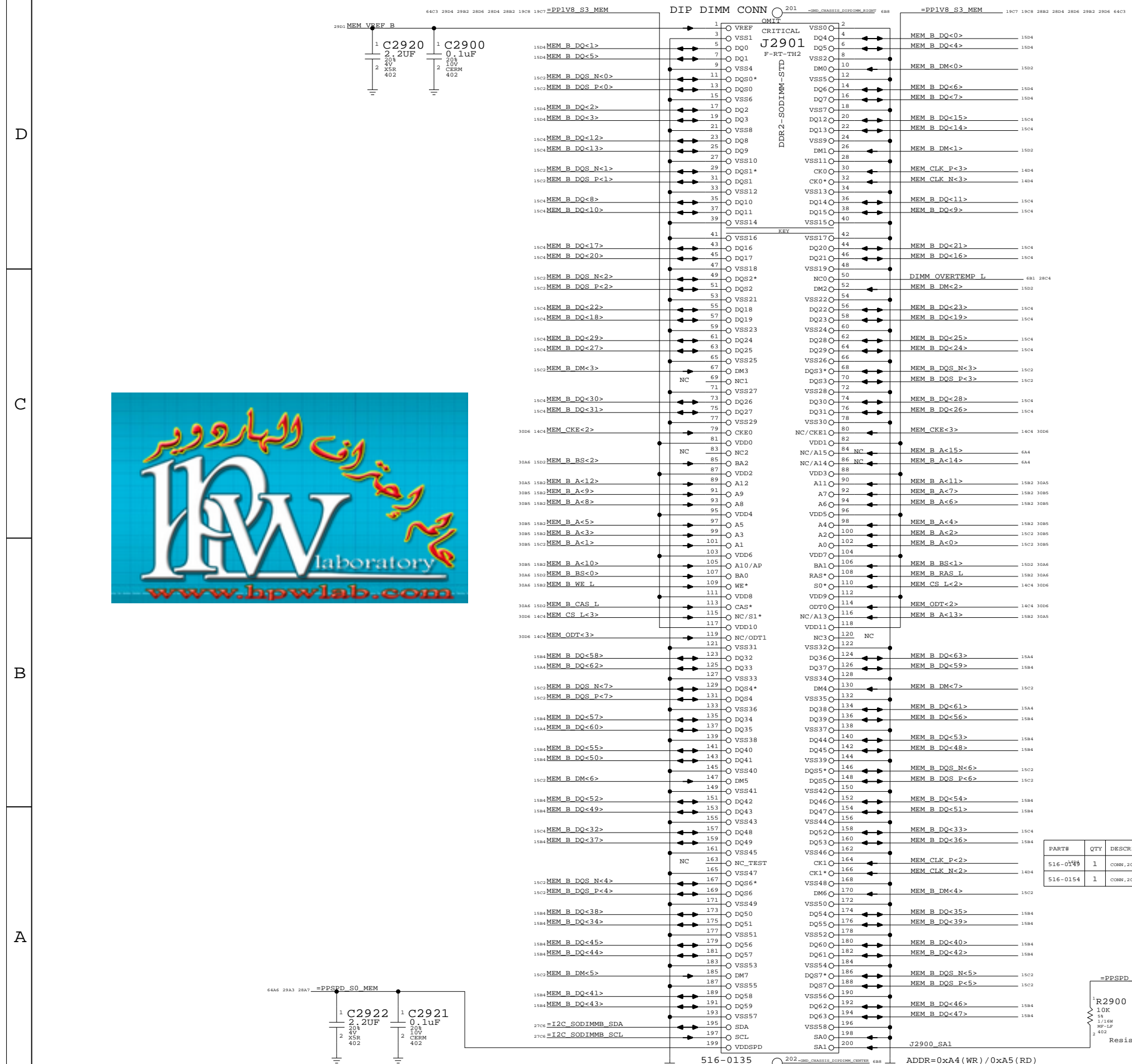
DDR2 SO-DIMM Connector B

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

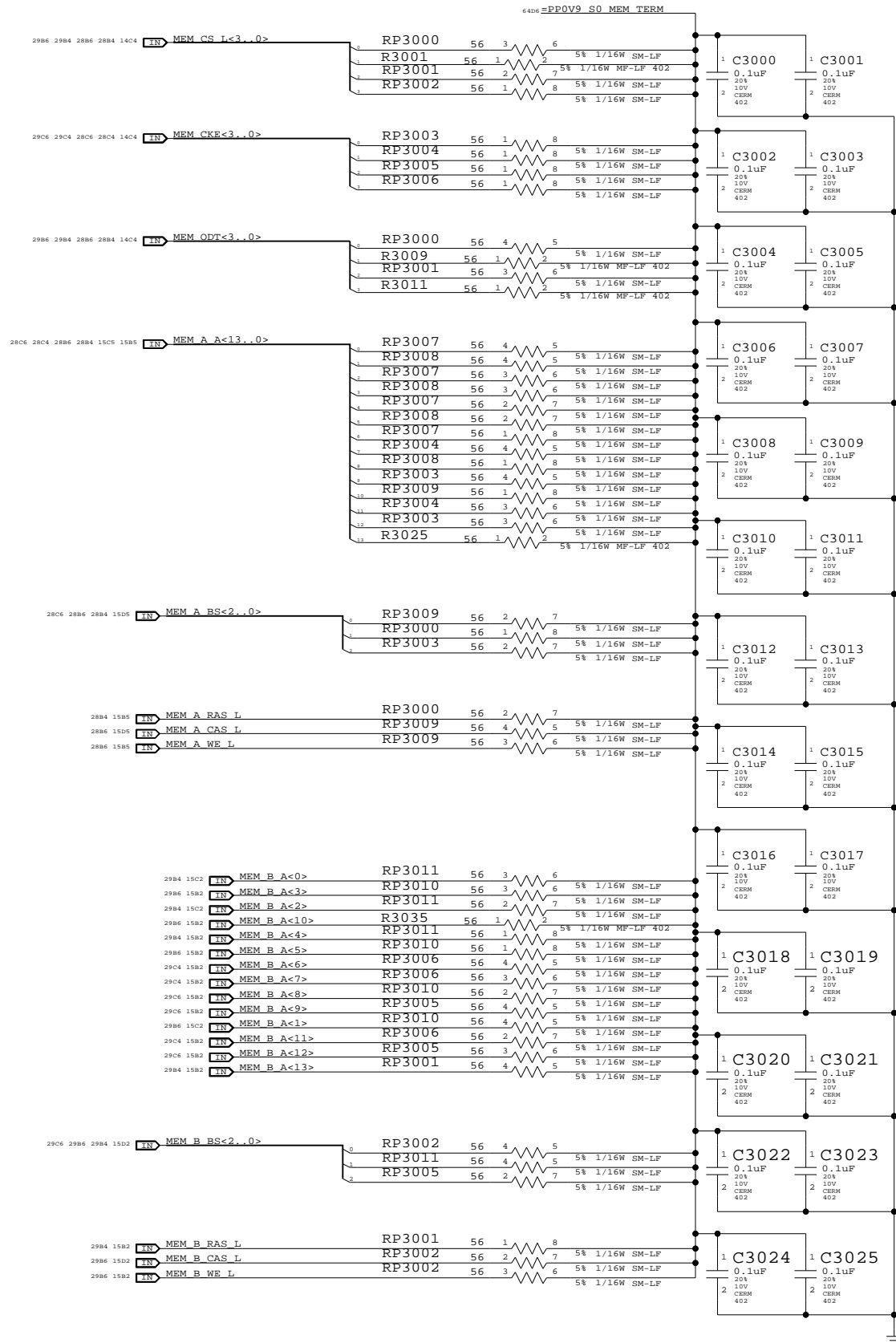
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	29		



One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

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	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	30	79	

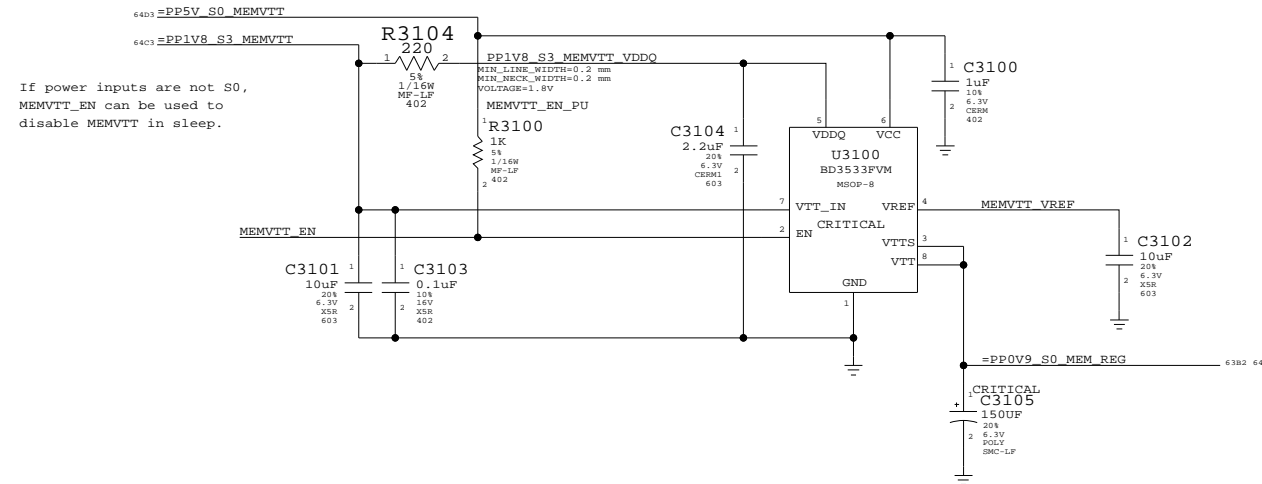
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

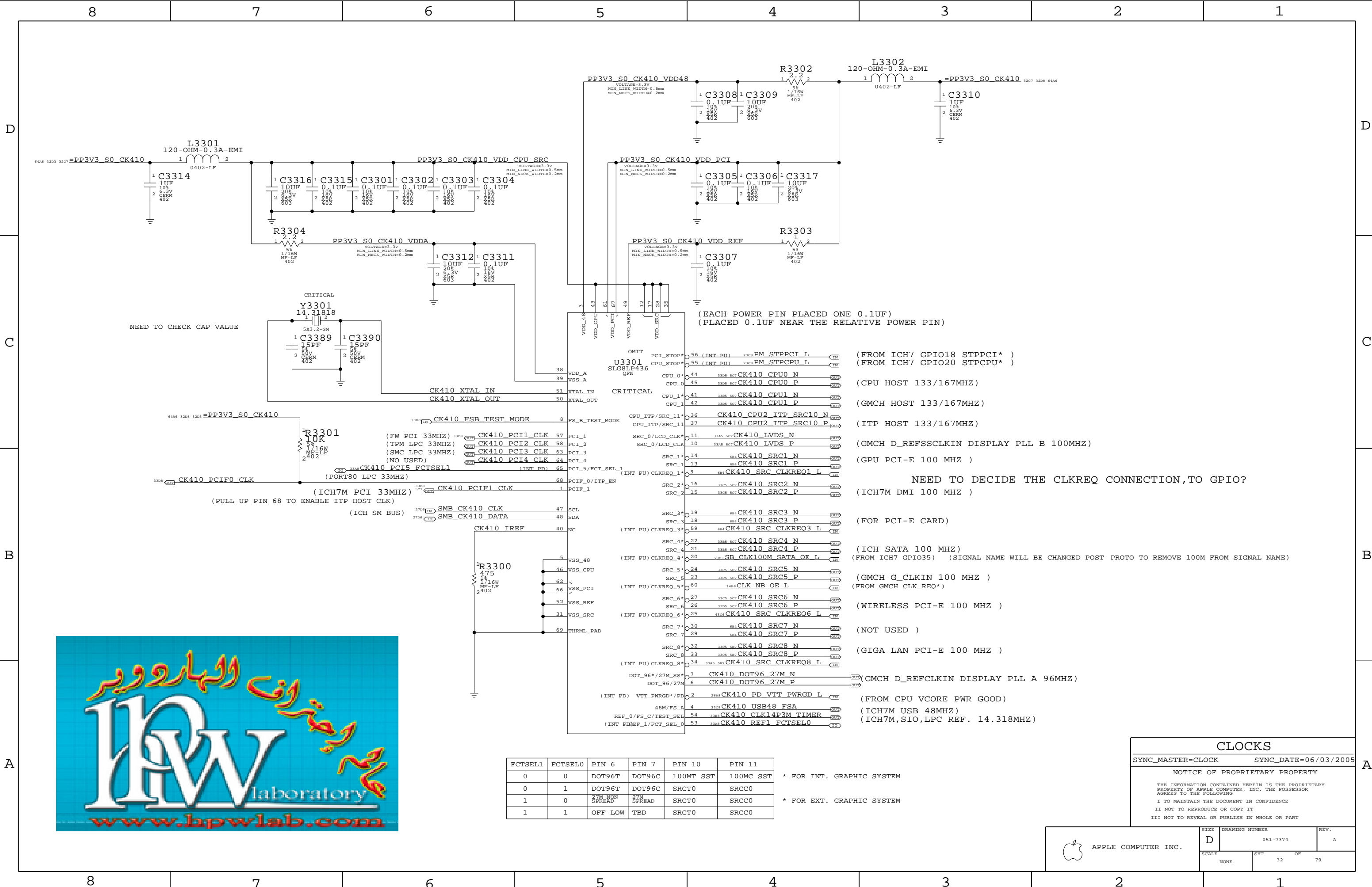
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	31	79	



NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?
(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)
(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G_CLKIN 100 MHZ)
(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)
(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSELO	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM



CLOCKS

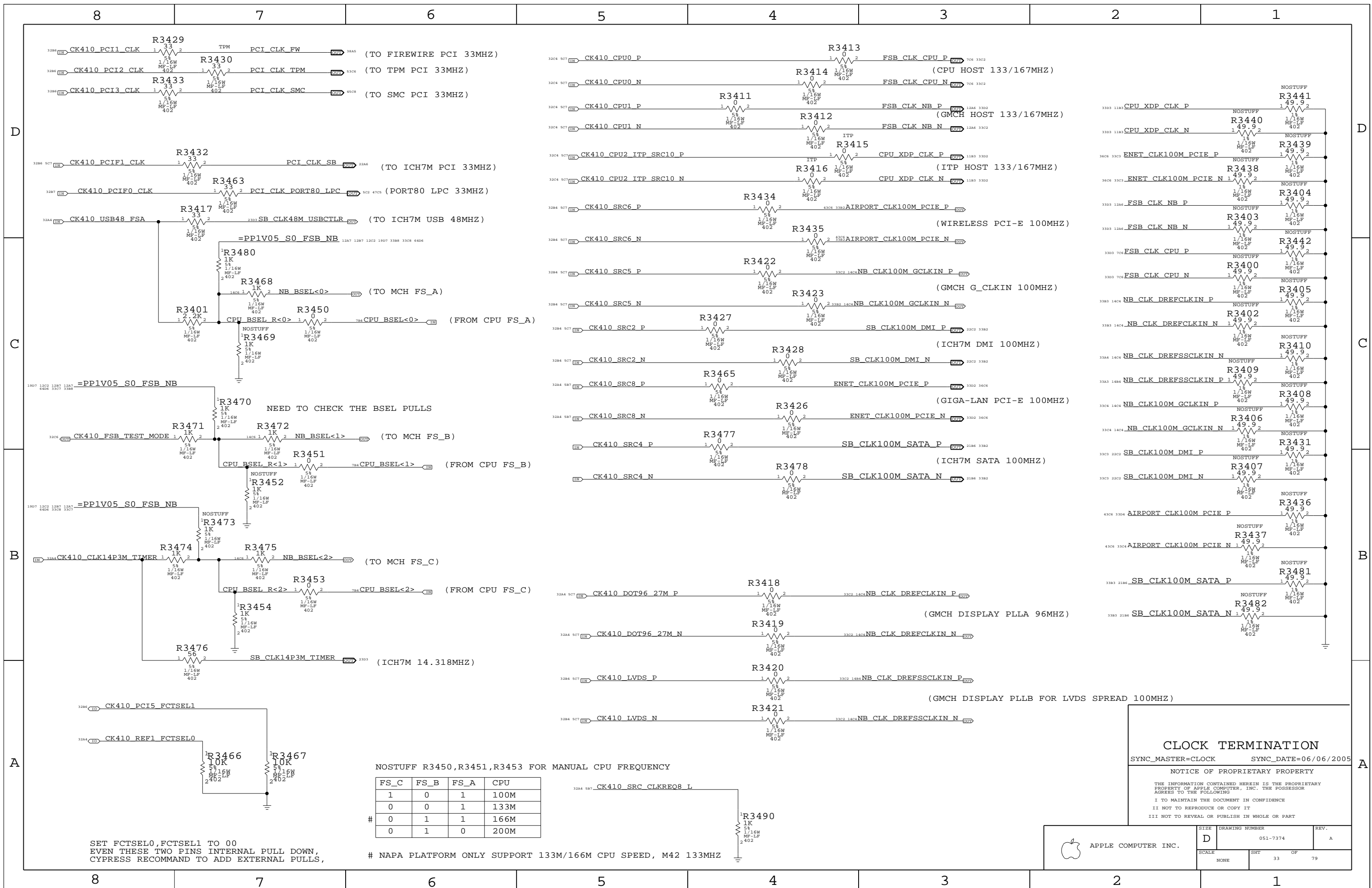
SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

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	D	051-7374	A
SCALE	SHT	OF	79
NONE		32	



NOSTUFF R3450, R3451, R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M

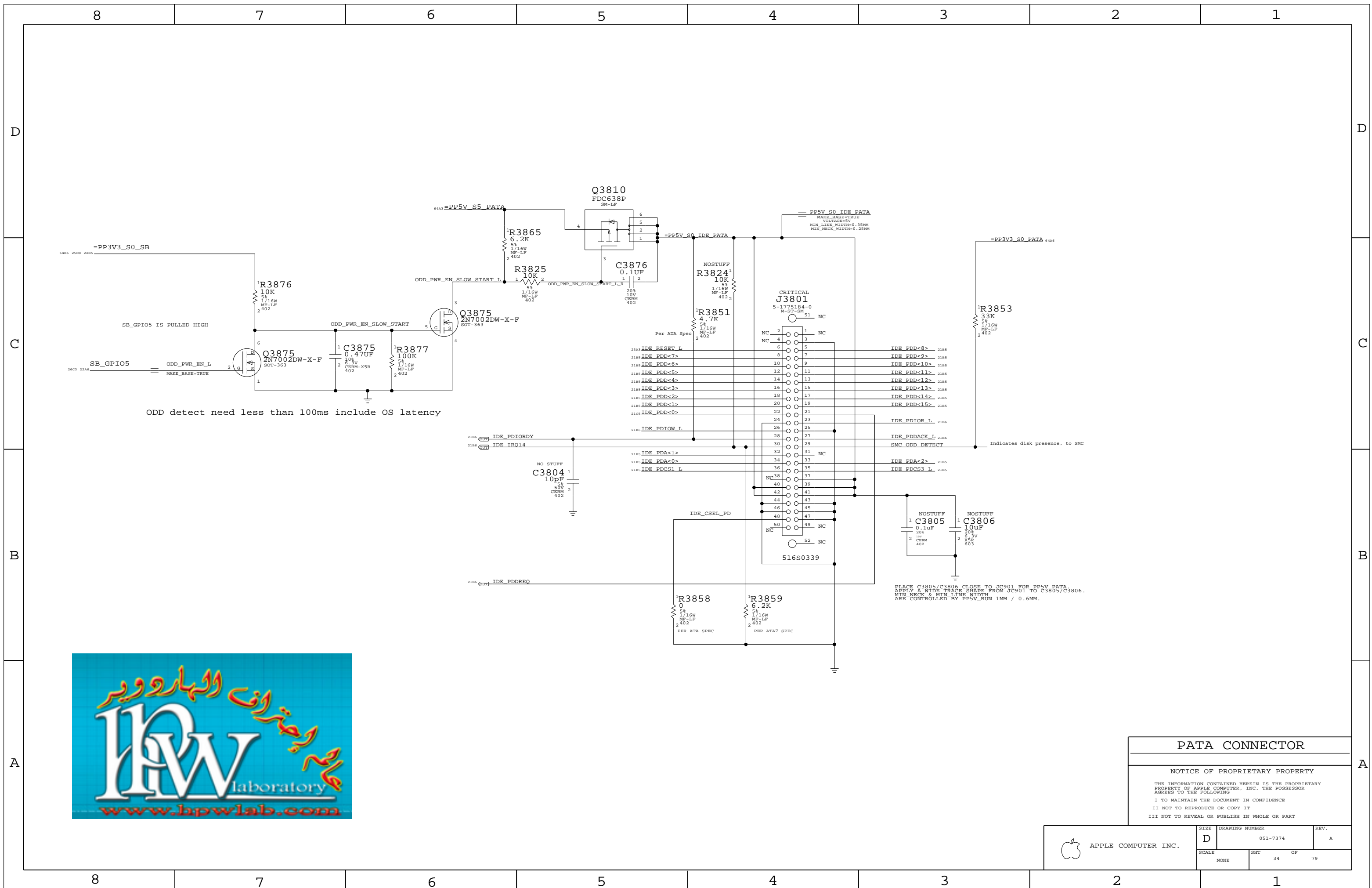
NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ

SET FCTSEL0, FCTSEL1 TO 00
EVEN THESE TWO PINS INTERNAL PULL DOWN,
CYPRESS RECOMMAND TO ADD EXTERNAL PULLS,

CLOCK TERMINATION
SYNC_MASTER=CLOCK SYNC_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 33	OF 79



PATA CONNECTOR

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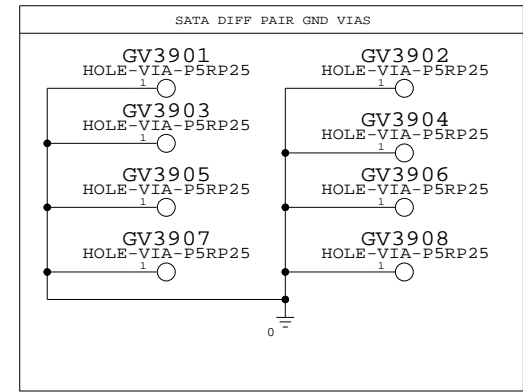
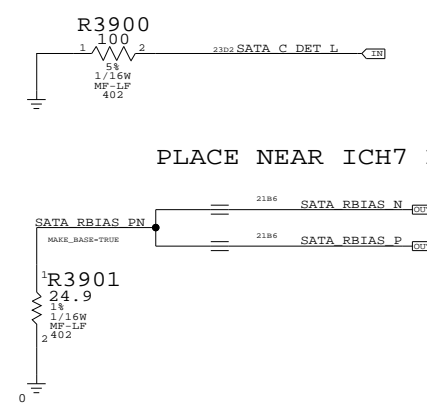
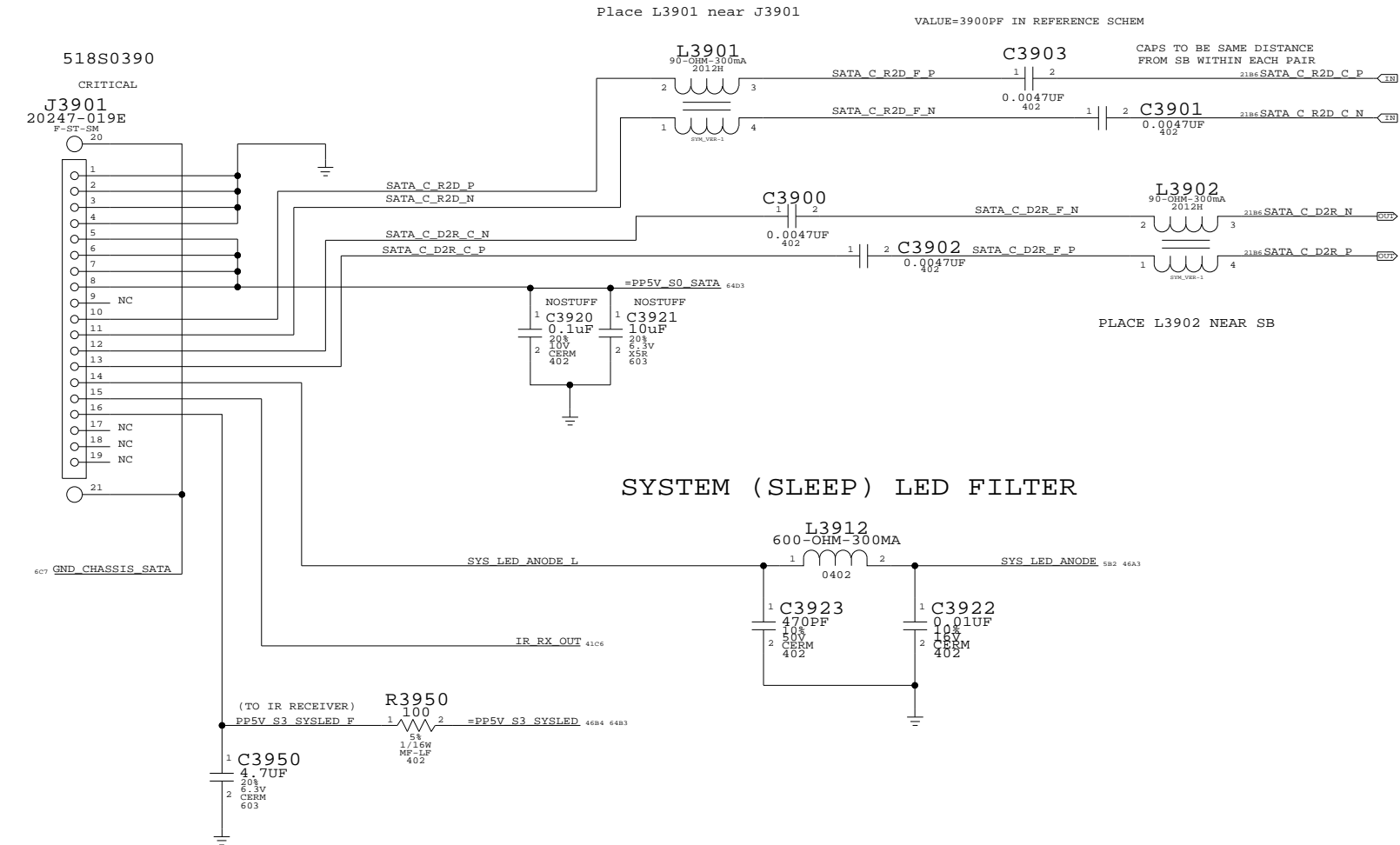
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 34	OF 79

SATA CONNECTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	J3901.L3902	KEEP MAG. LAYER IN BOM

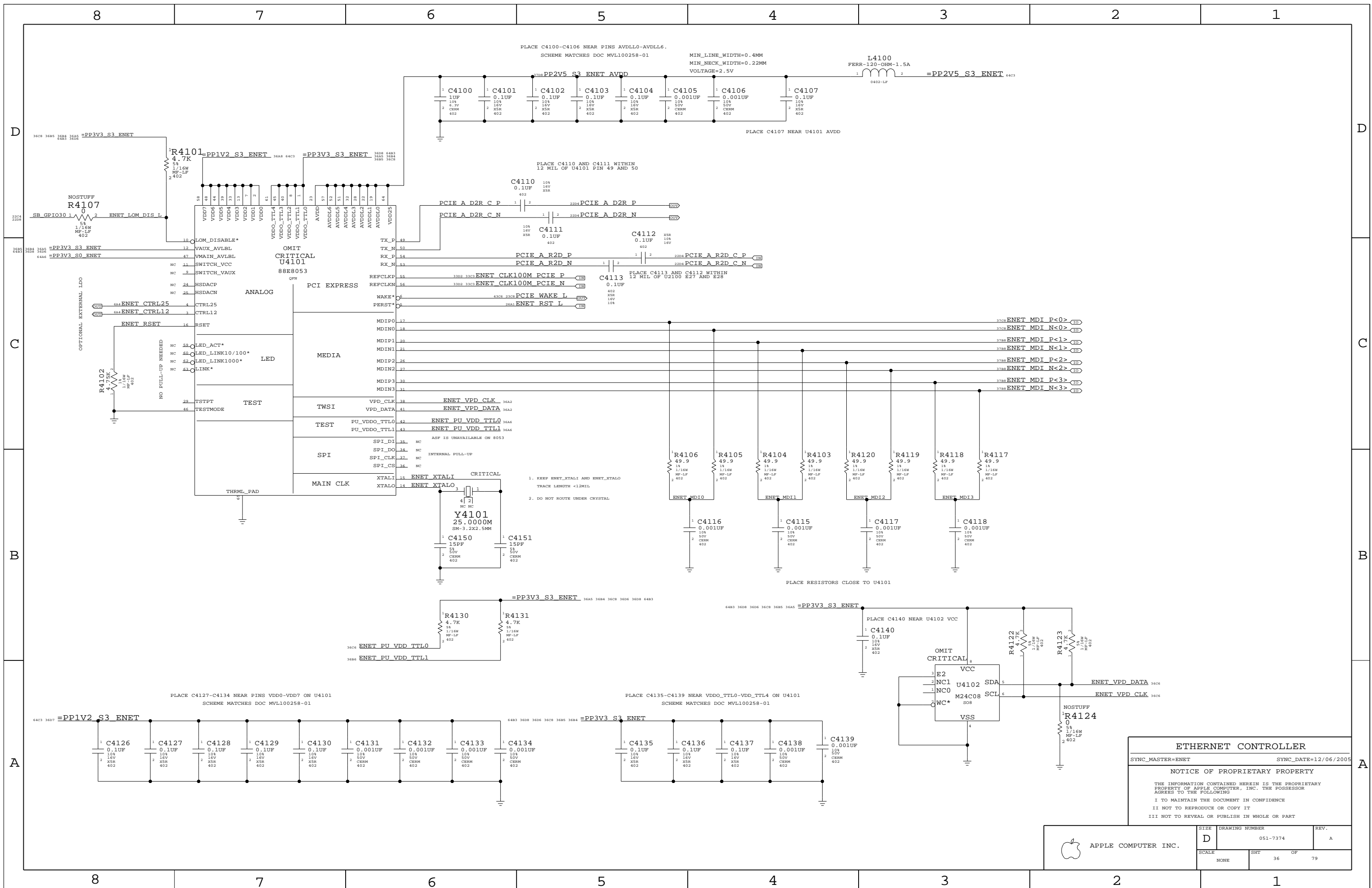
SATA CONNECTOR

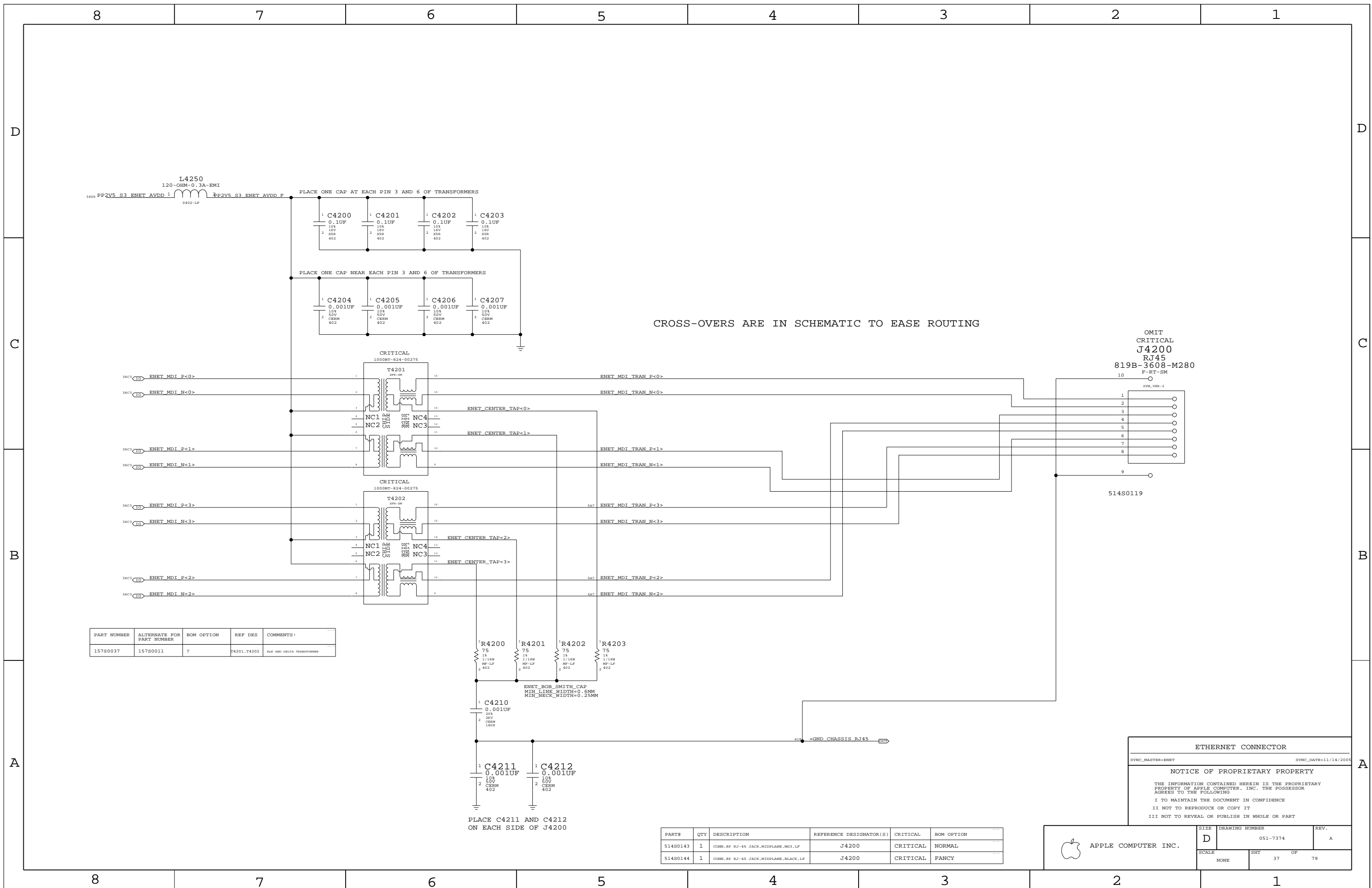
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	35		





L4250
120-OHM-0.3A-EMI
3605 PP2V5_S3_ENET_AVDD 1 0402-LF 3 PP2V5_S3_ENET_AVDD_F

PLACE ONE CAP AT EACH PIN 3 AND 6 OF TRANSFORMERS

1 C4200 0.1UF 10% 10V XSR 402
1 C4201 0.1UF 10% 10V XSR 402
1 C4202 0.1UF 10% 10V XSR 402
1 C4203 0.1UF 10% 10V XSR 402

PLACE ONE CAP NEAR EACH PIN 3 AND 6 OF TRANSFORMERS

1 C4204 0.001UF 10% 50V CERM 402
1 C4205 0.001UF 10% 50V CERM 402
1 C4206 0.001UF 10% 50V CERM 402
1 C4207 0.001UF 10% 50V CERM 402

CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING

OMIT CRITICAL
J4200
RJ45
819B-3608-M280
F-RT-SM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
157S0037	157S0011	?	R4201, T4202	SEE AND DELTA TRANSFORMER

1 R4200 75 1% 1/16W NP-LF 402
1 R4201 75 1% 1/16W NP-LF 402
1 R4202 75 1% 1/16W NP-LF 402
1 R4203 75 1% 1/16W NP-LF 402

1 C4210 0.001UF 20% 20V CERM 1808

1 C4211 0.001UF 10% 50V CERM 402
1 C4212 0.001UF 10% 50V CERM 402

PLACE C4211 AND C4212 ON EACH SIDE OF J4200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN, SP RJ-45 JACK, MIDPLANE, M3, LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN, SP RJ-45 JACK, MIDPLANE, BLACK, LF	J4200	CRITICAL	FANCY

ETHERNET CONNECTOR
SYNC_MASTER=ENET SYNC_DATE=11/14/2005
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APPLE COMPUTER INC.

SIZE D	DRAWING NUMBER 051-7374	REV. A
SCALE NONE	SHT 37	OF 79

PAGE NOTES

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PCO - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

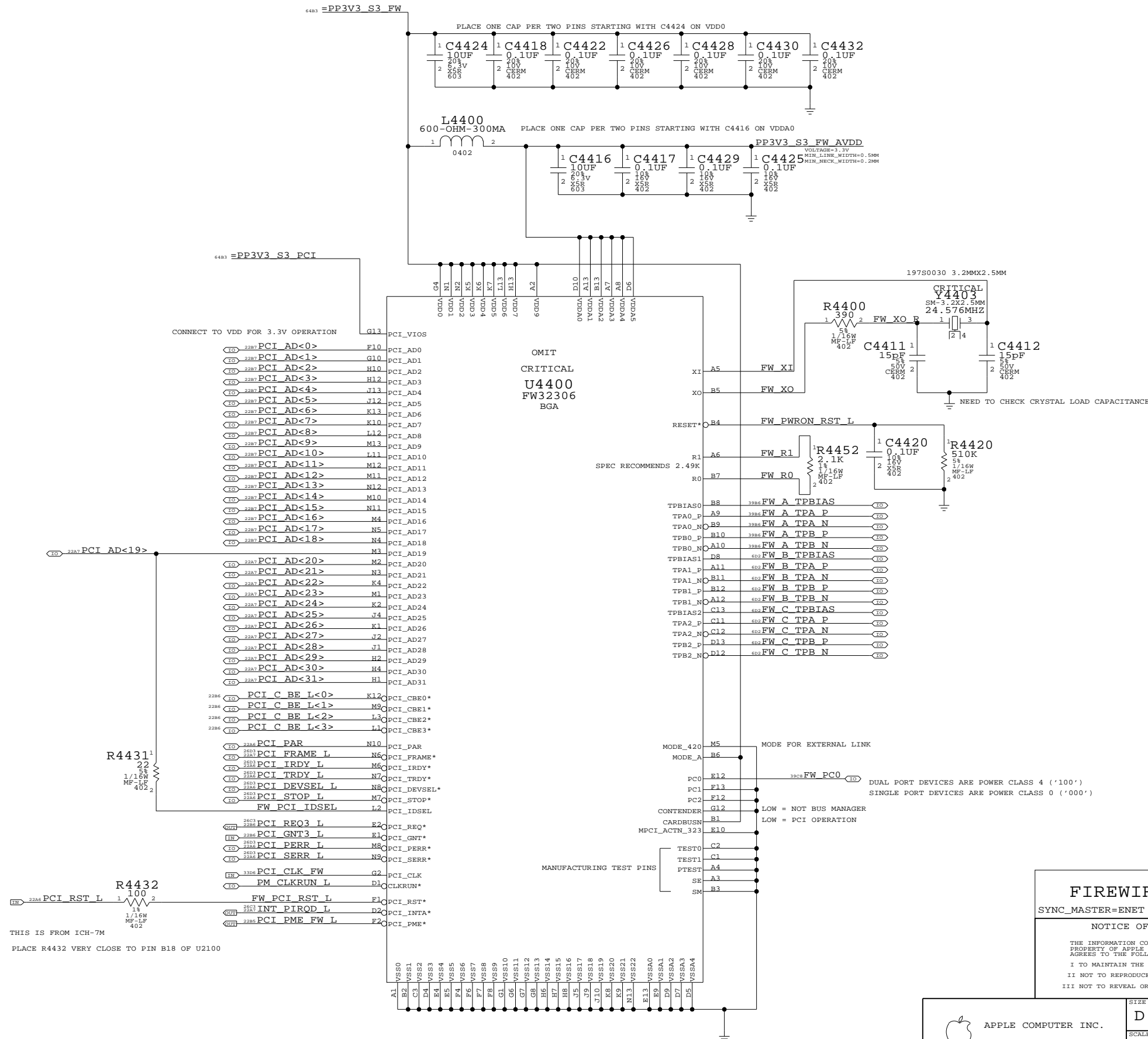
OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ3/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRINGS OUT PCO CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP



FIREWIRE CONTROLLER
SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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Table with columns: SCALE, SHEET, OF, REV. A. Values: NONE, 38, 79, A.

Page Notes

INPUT:
 =PPBUS_S5 - PORT POWER
 =PP3V3_S5_FW - DIGITAL POWER
 =GND_CHASSIS_FW_PORT0 - CHASSIS GROUND
 =FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:
 FW_TP0A_P/N, FW_TP0B_P/N, FW_TPBIA50 - FIREWIRE DIFF PAIRS

OUTPUT:
 FW_PCO - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

PAGE HISTORY

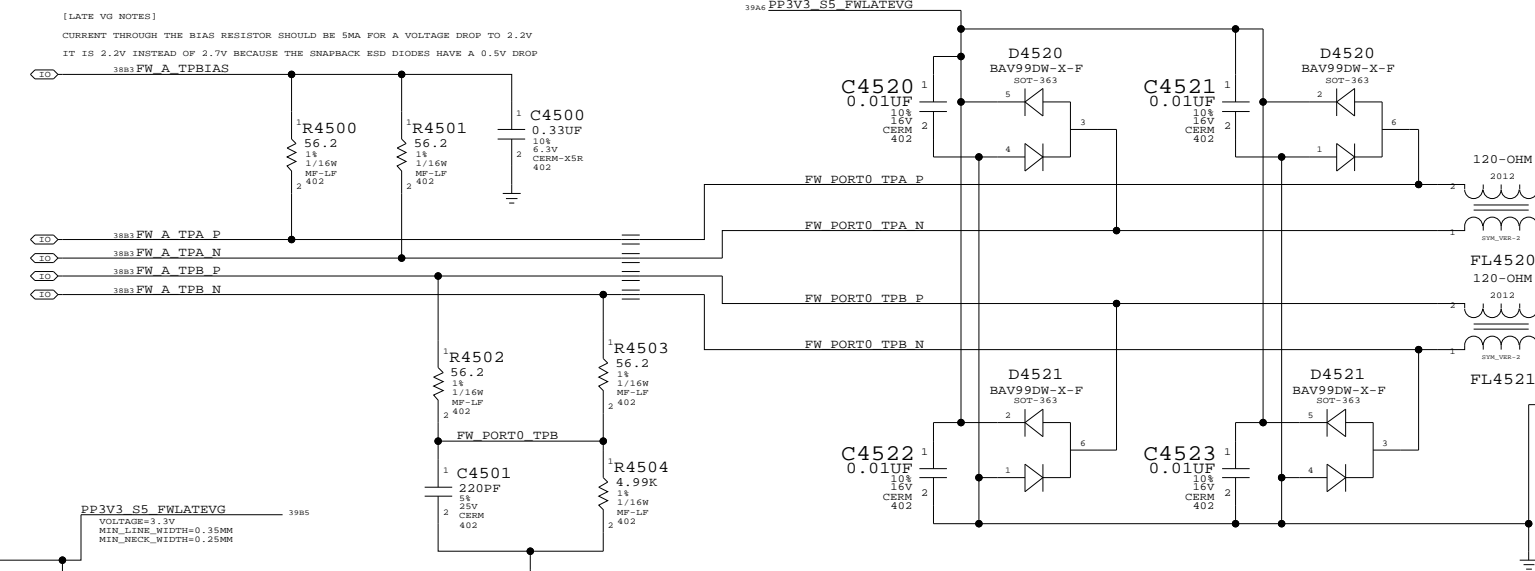
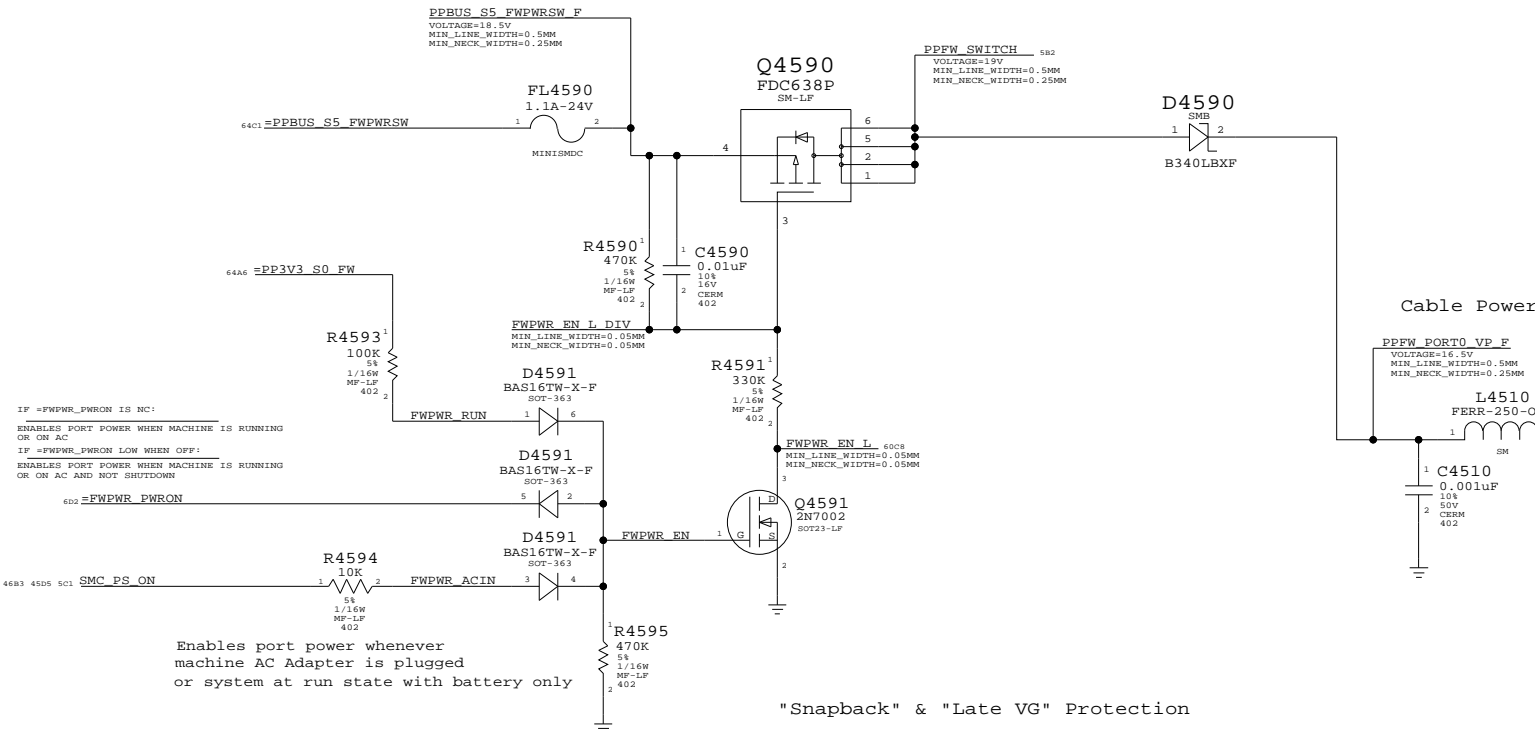
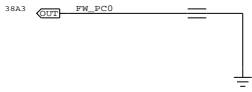
5/19/05 - INITIAL REVISION
 6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
 6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
 6/22/05 - CONNECTED FW_PCO FOR SINGLE PORT
 7/26/05 - UPDATED LATE-VG POWER HALL CIRCUIT FROM M1
 7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
 7/26/05 - SWITCHED TO 514-0124 FOR FIRE-PROTD CONNECTOR
 7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
 7/26/05 - CHANGED FL4590 TO 1.1A VERSION
 7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
 7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
 FireWire Design Guide (FWDG 0.6, 5/14/03)

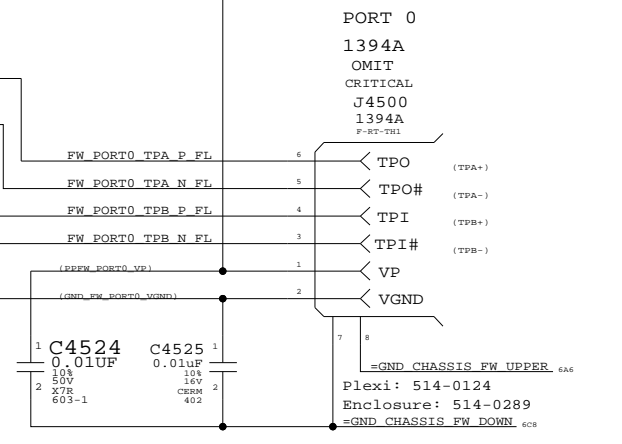
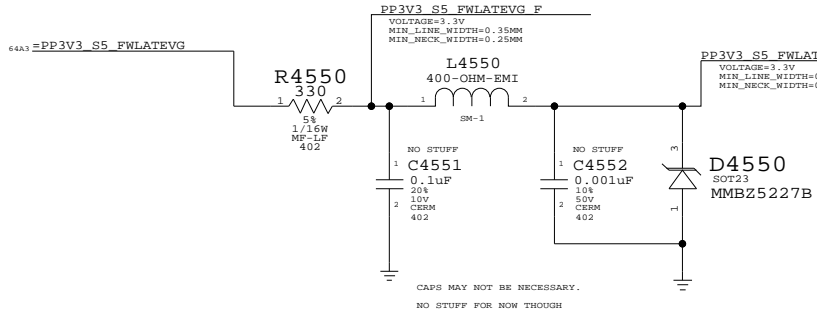


PORT POWER CLASS

0 FOR SINGLE PORT
 1 FOR DUAL PORT



LATE-VG PROTECTION POWER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN, 6P 1394A RCPT, MIDLANE, M33, LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN, 6P 1394A RCPT, MIDLANE, BLACK, LF	J4500	CRITICAL	FANCY

FIREWIRE PORT

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

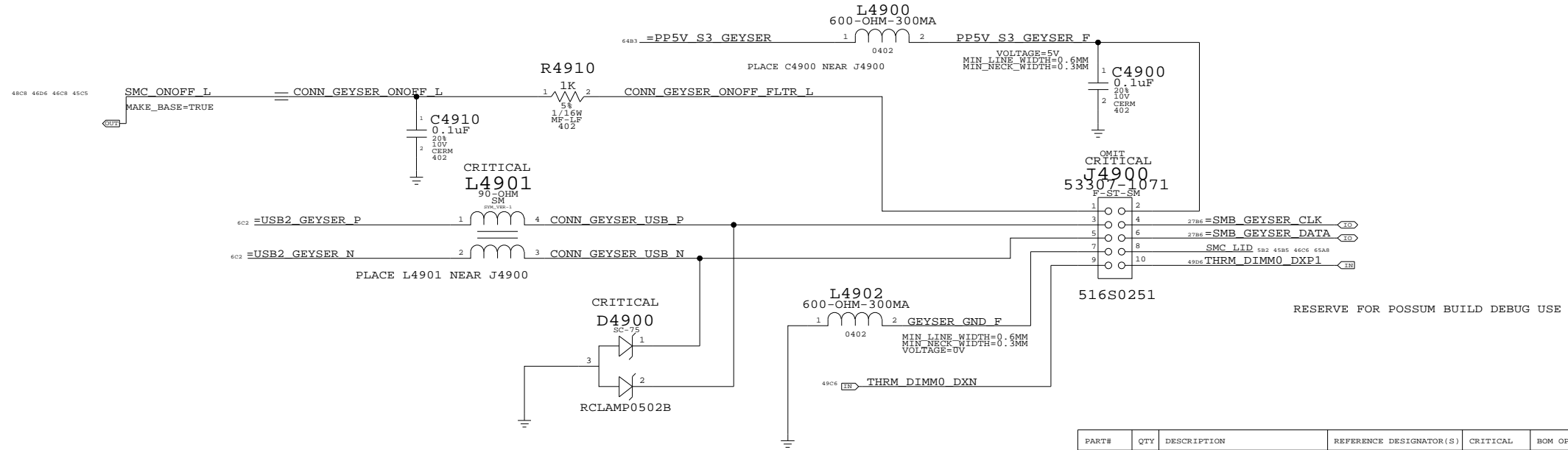
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	D	051-7374	A
SCALE	SHT	OF	79
NONE	39		

GEYSER AND DIMMO REMOTE TEMP SENSORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY



CONNECTOR MISC
 SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	40	79	

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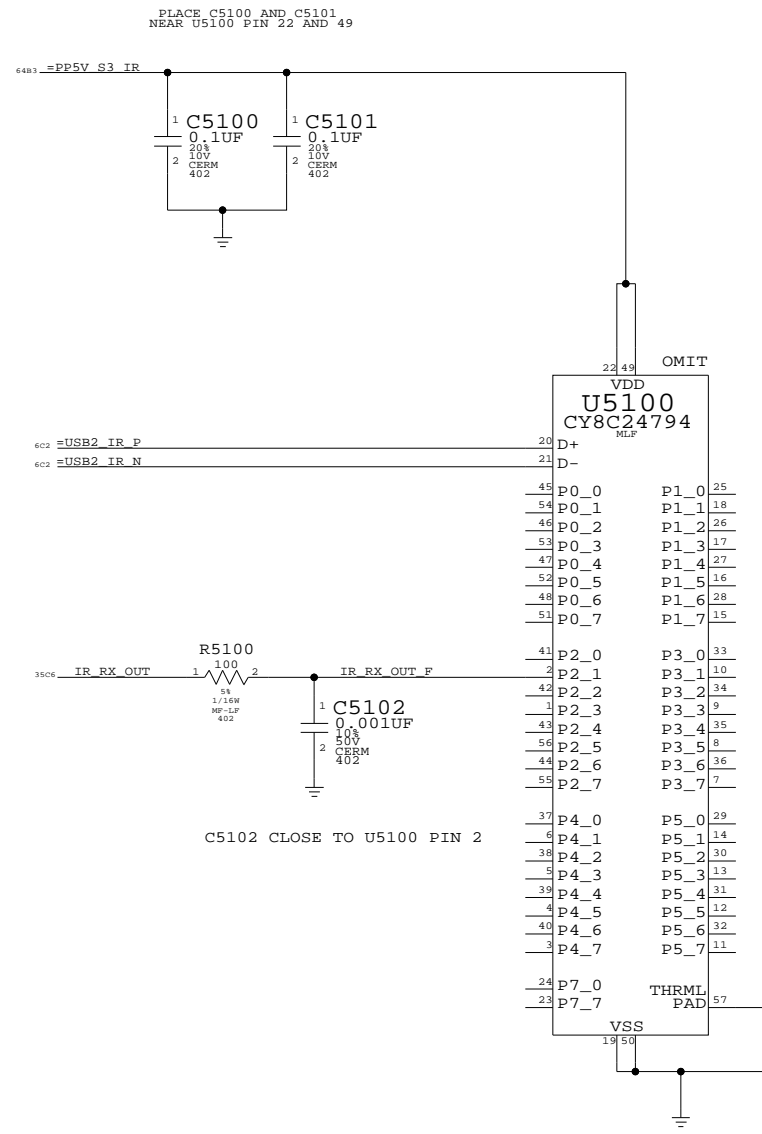
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8 7 6 5 4 3 2 1



8 7 6 5 4 3 2 1

IR CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=11/09/2005

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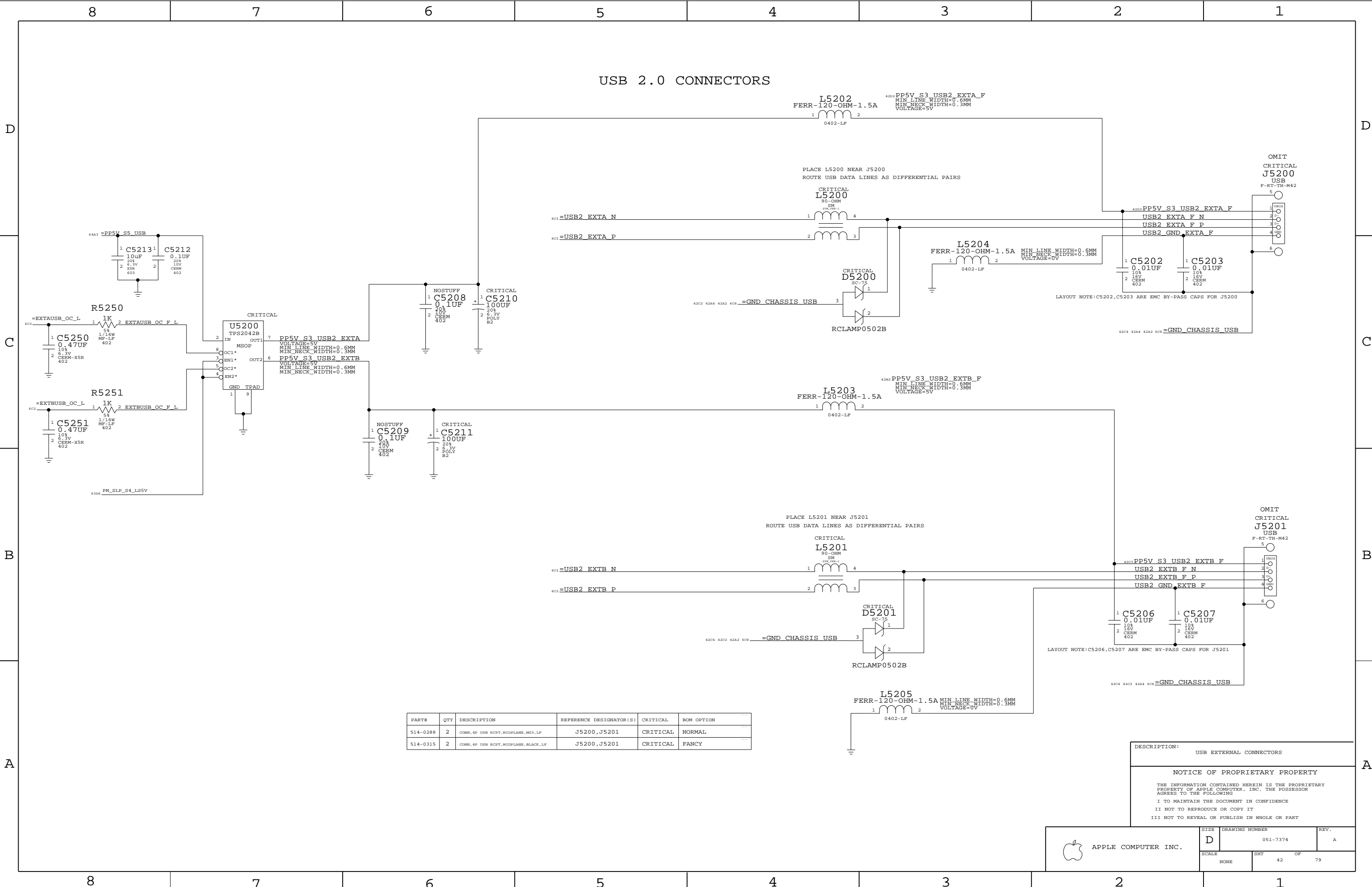
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT		OF
NONE	41		79

USB 2.0 CONNECTORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN, 4P USB RCPT, MIDPLANE, W3, LF	J5200, J5201	CRITICAL	NORMAL
514-0315	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J5200, J5201	CRITICAL	FANCY

DESCRIPTION: USB EXTERNAL CONNECTORS

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	42	79	

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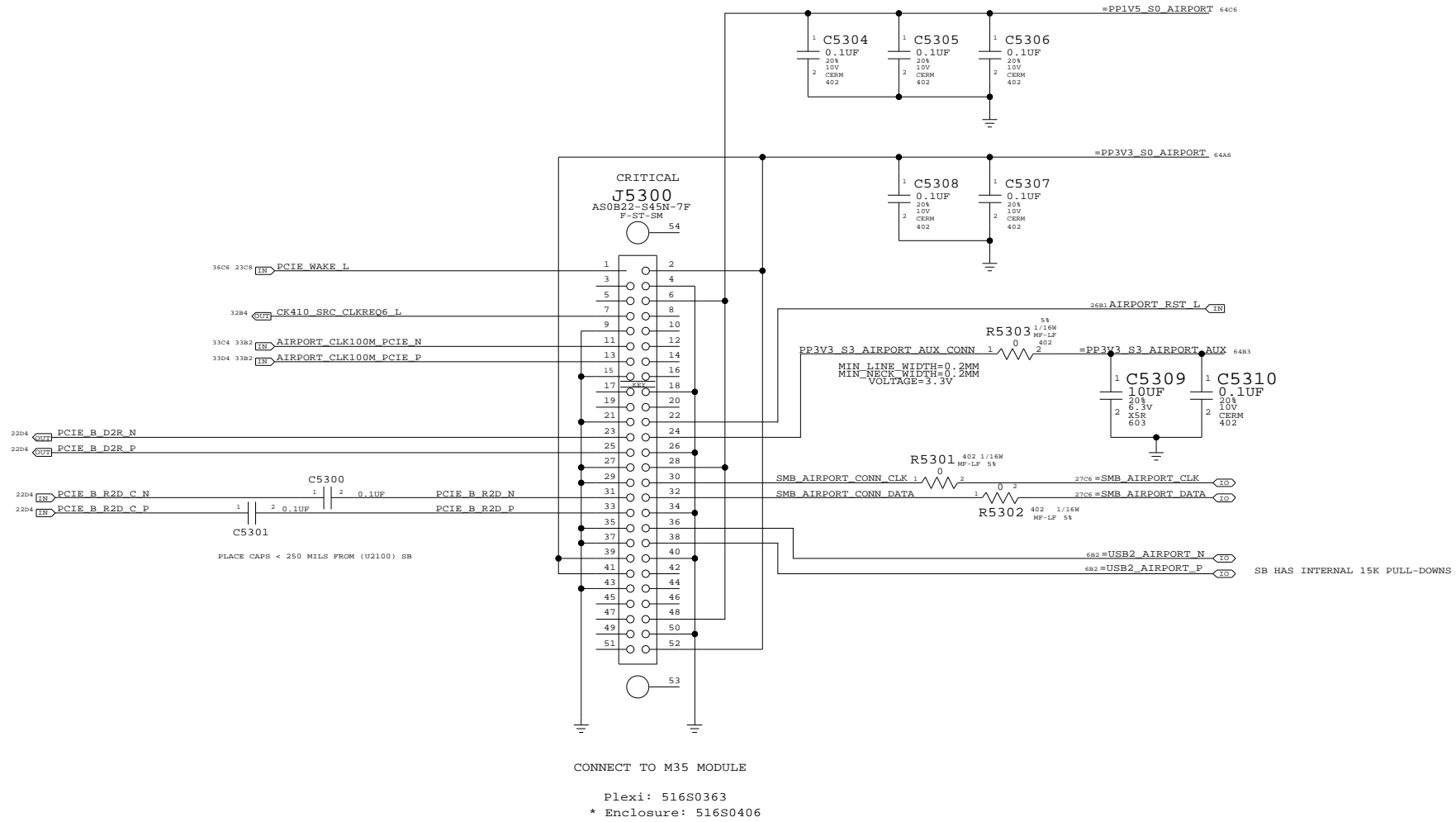
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AIRPORT CONN

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 43	OF 79

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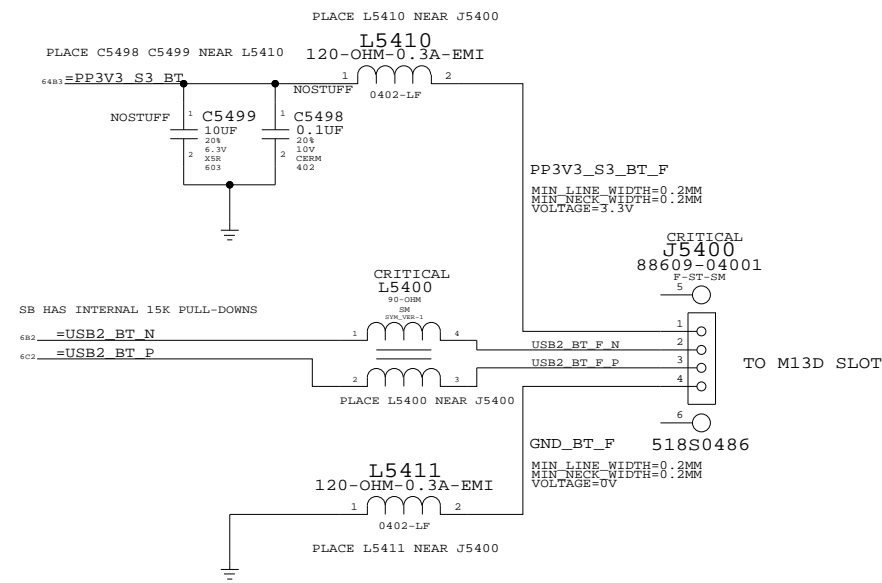
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BLUETOOTH INTERFACE


NOTICE OF PROPRIETARY PROPERTY

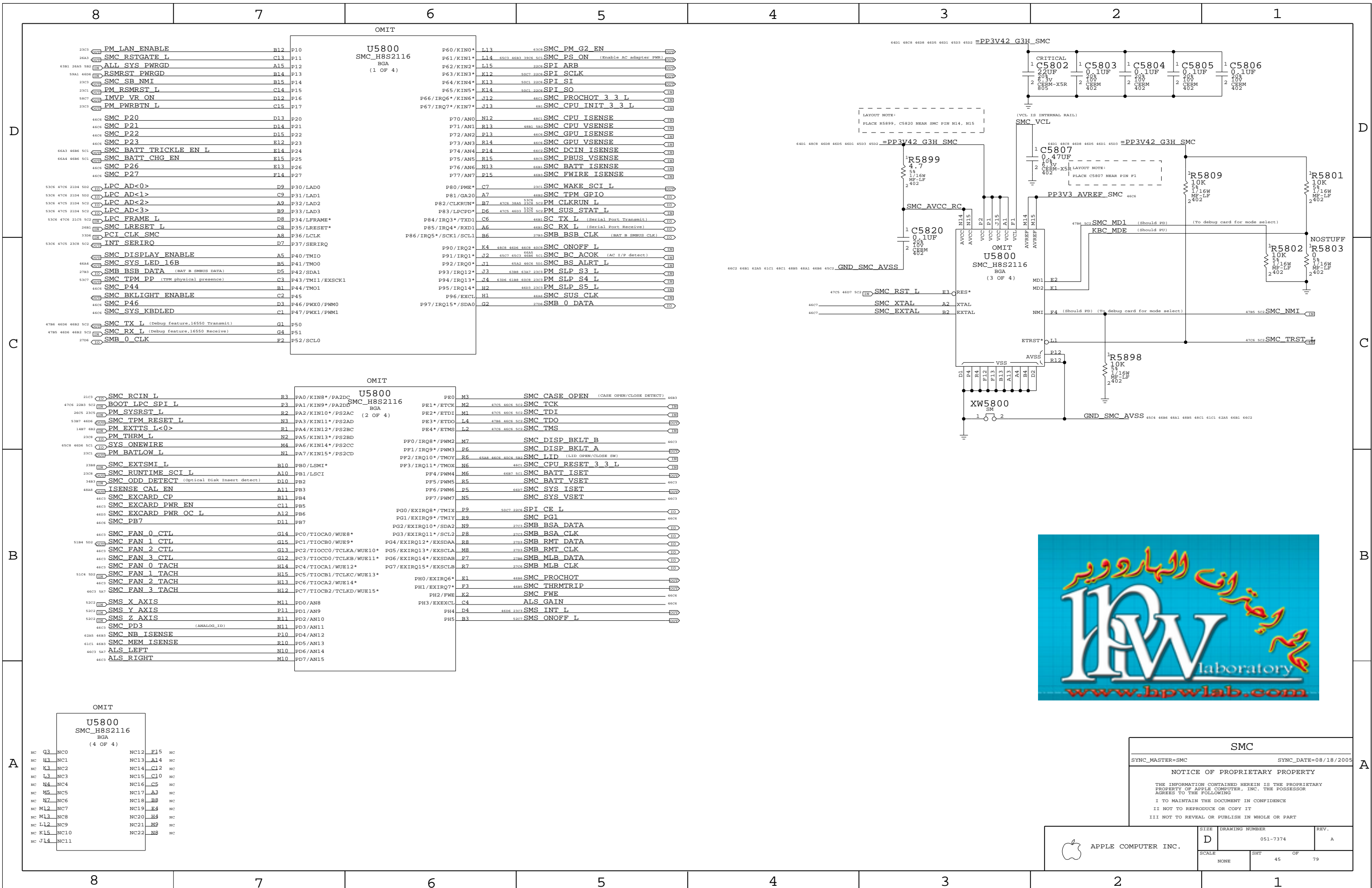
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	
NONE	44	79	



SMC

SYNC_MASTER=SMC SYNC_DATE=08/18/2005

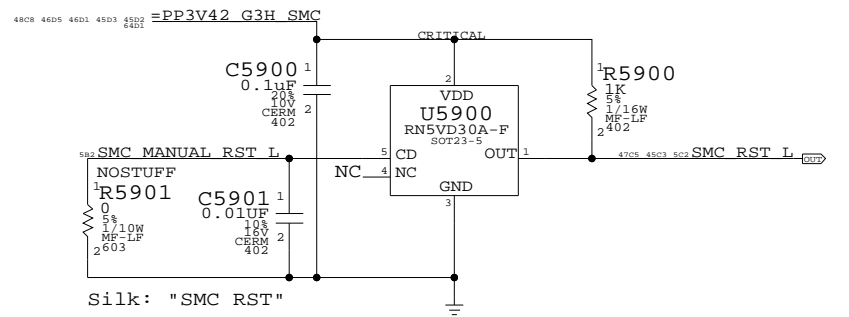
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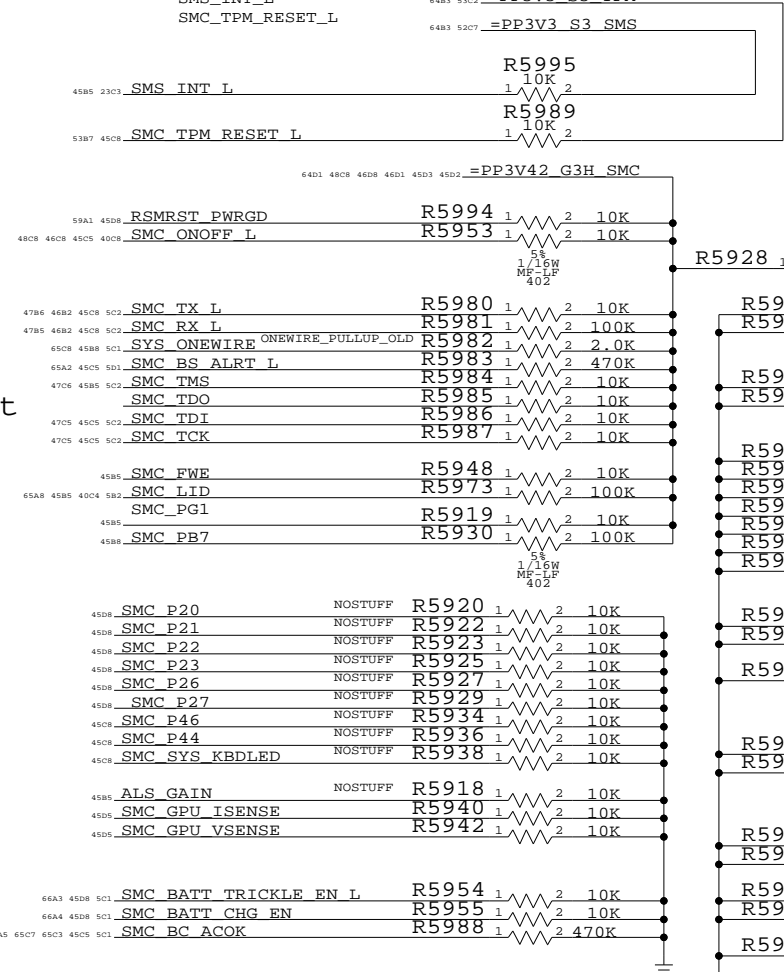
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 45	OF 79

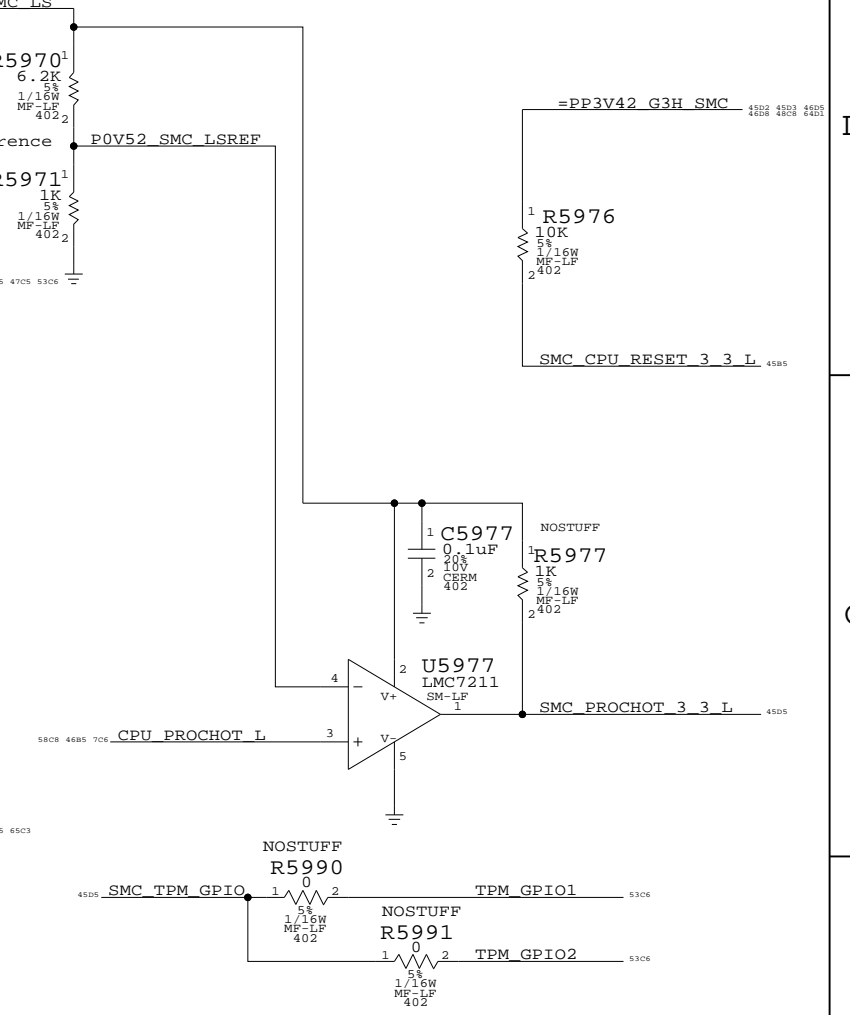
SMC Reset Button / Brownout Detect



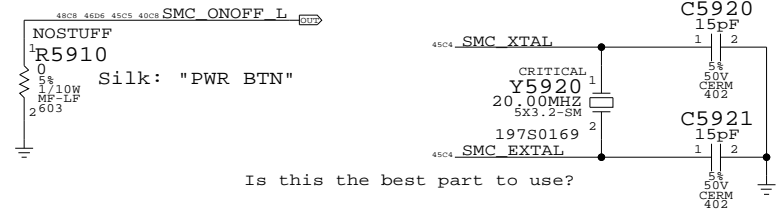
THESE NEED TO BE PULLED TO THE PROPER RAIL:



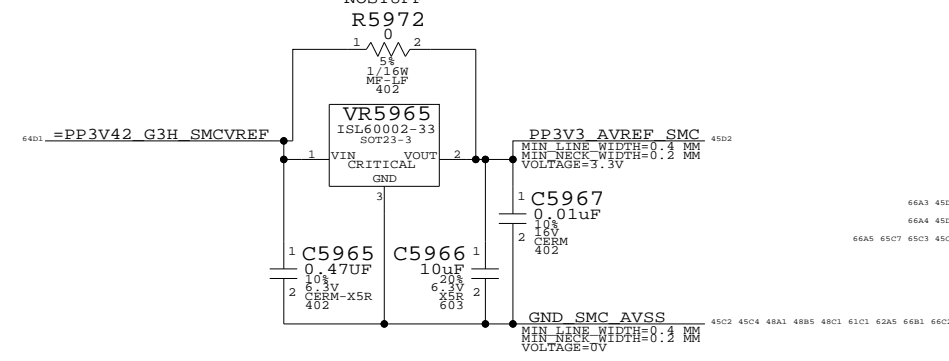
SMC 1.05V to 3.3V Level Shifting



Debug Power Button SMC Crystal Circuit

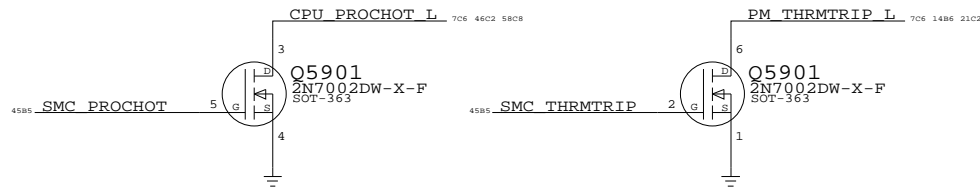


SMC AVREF Supply

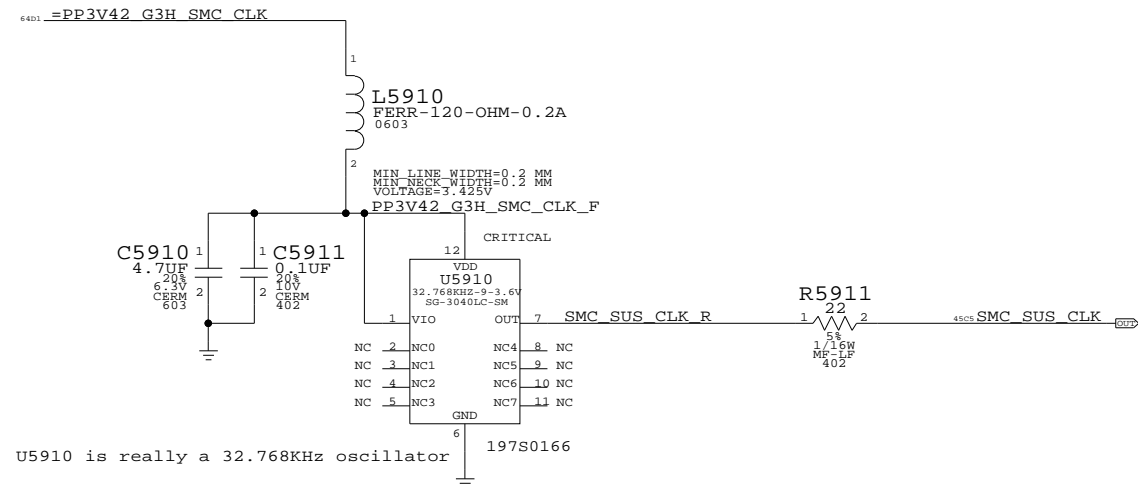


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

SMC 3.3V to 1.05V Level Shifting

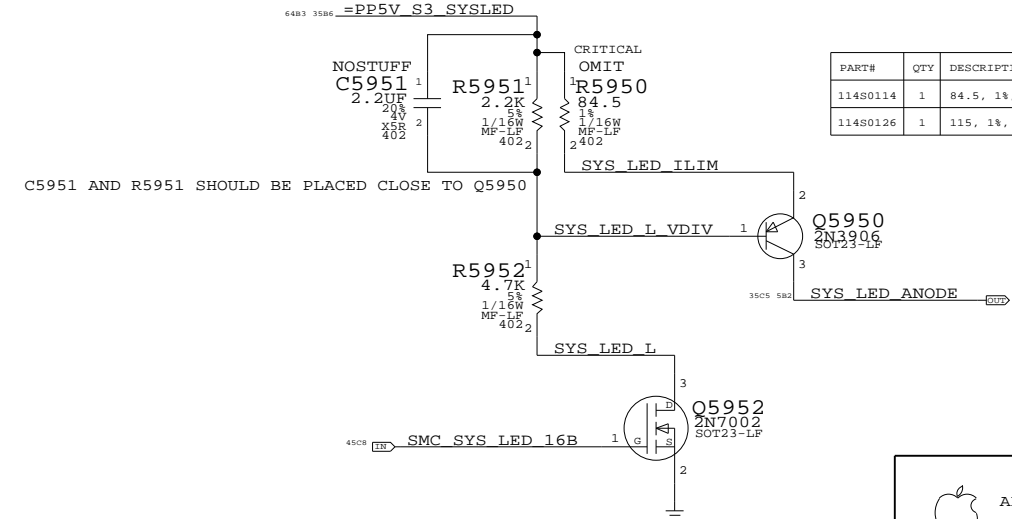


SMC G3HOT OSCILLATOR



U5910 is really a 32.768KHz oscillator

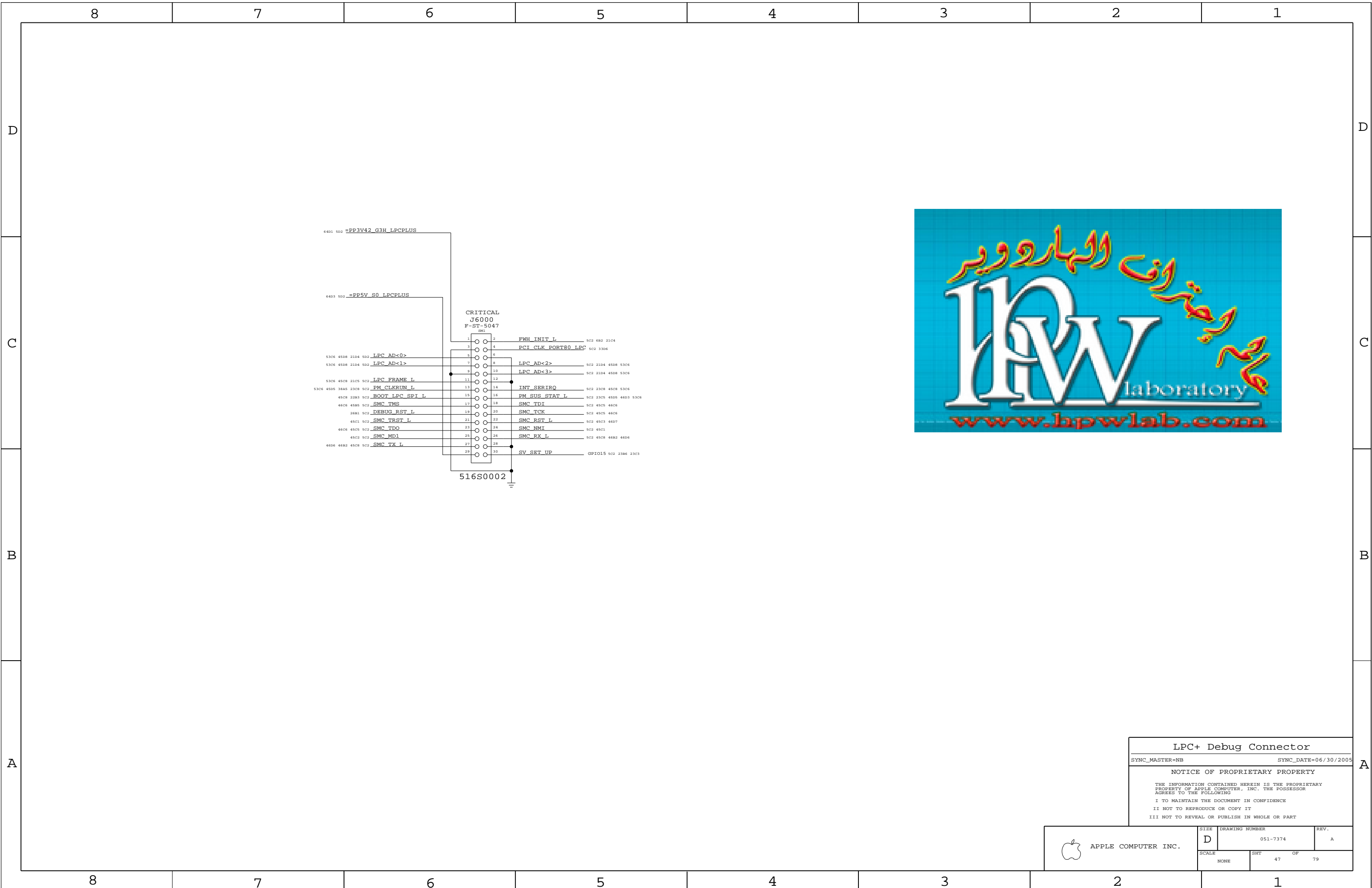
System (Sleep) LED Circuit



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT
 SYNC_MASTER=SMC SYNC_DATE=08/23/2005
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	SCALE NONE	SHEET 46	OF 79



LPC+ Debug Connector

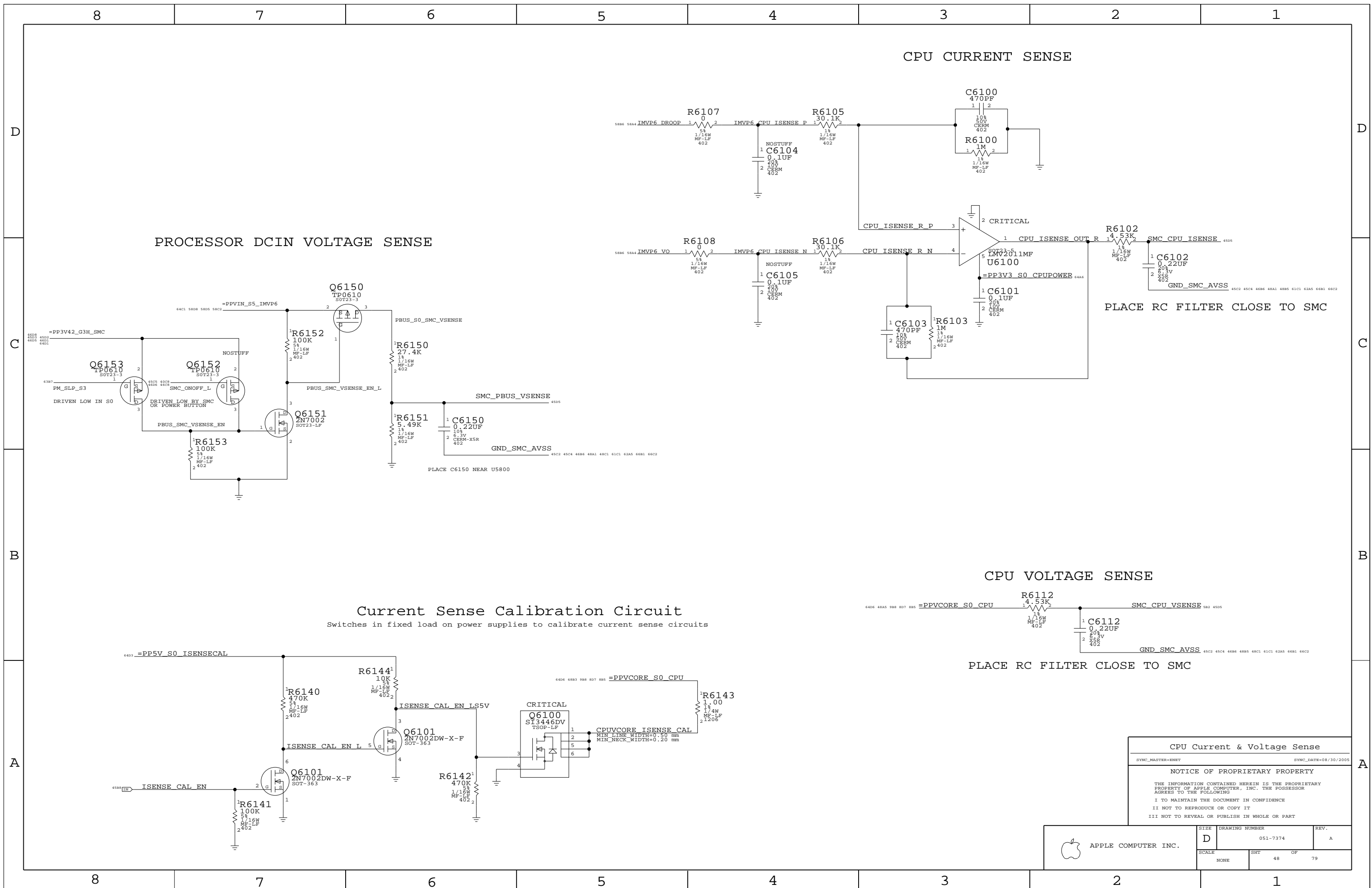
SYNC_MASTER=NB SYNC_DATE=06/30/2005

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	SCALE NONE	SHEET 47	OF 79



PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

CPU VOLTAGE SENSE

Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits

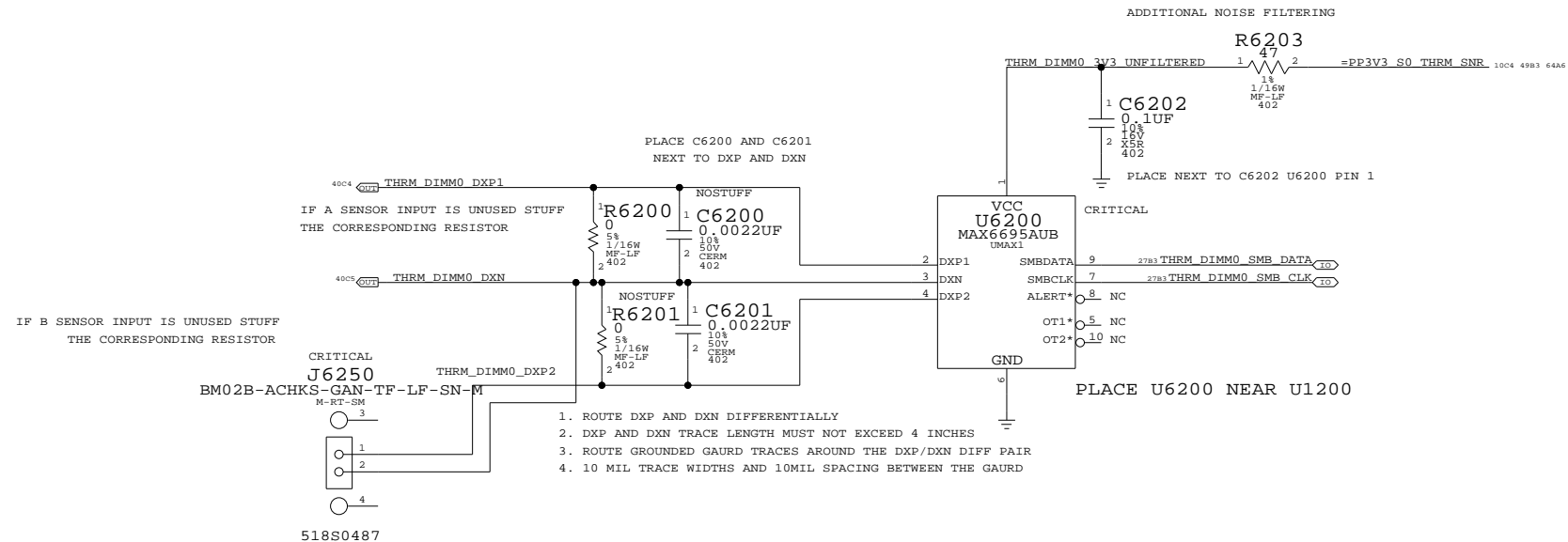
PLACE RC FILTER CLOSE TO SMC

PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense
 SYNC_MASTER=EMBT SYNC_DATE=08/30/2005
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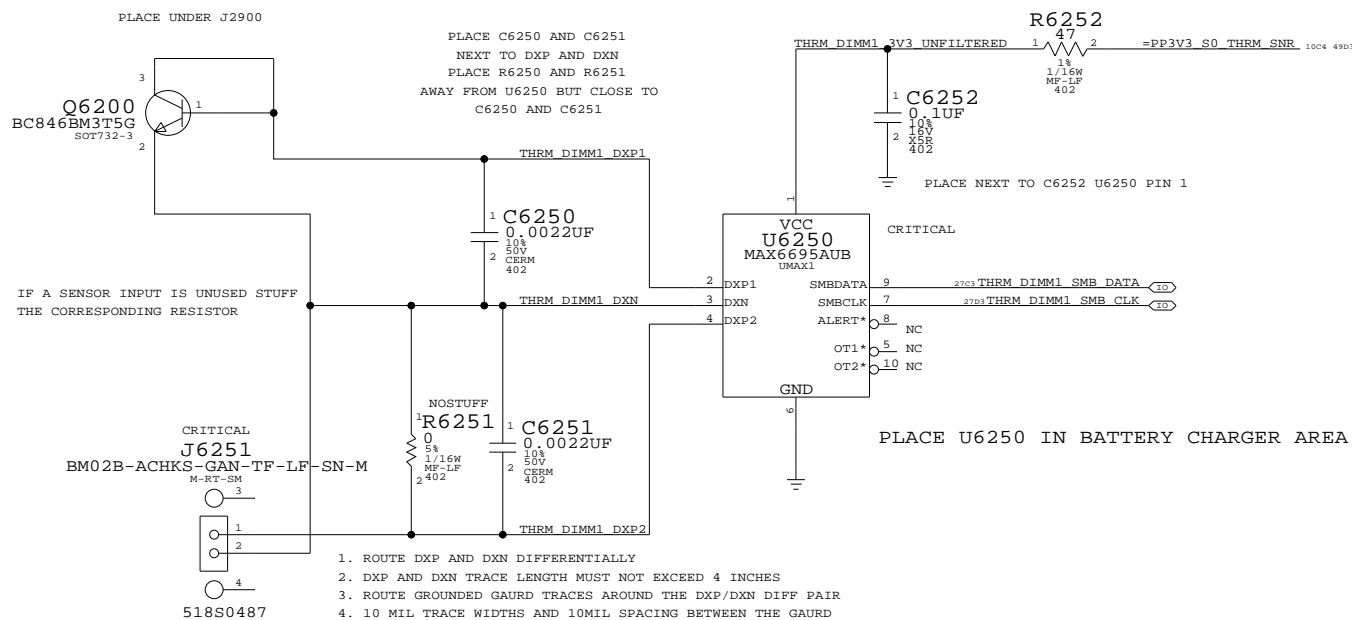
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	48		

DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452 AND THEN 518S0487
 AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

DIMM1 TEMPERATURE ZONE

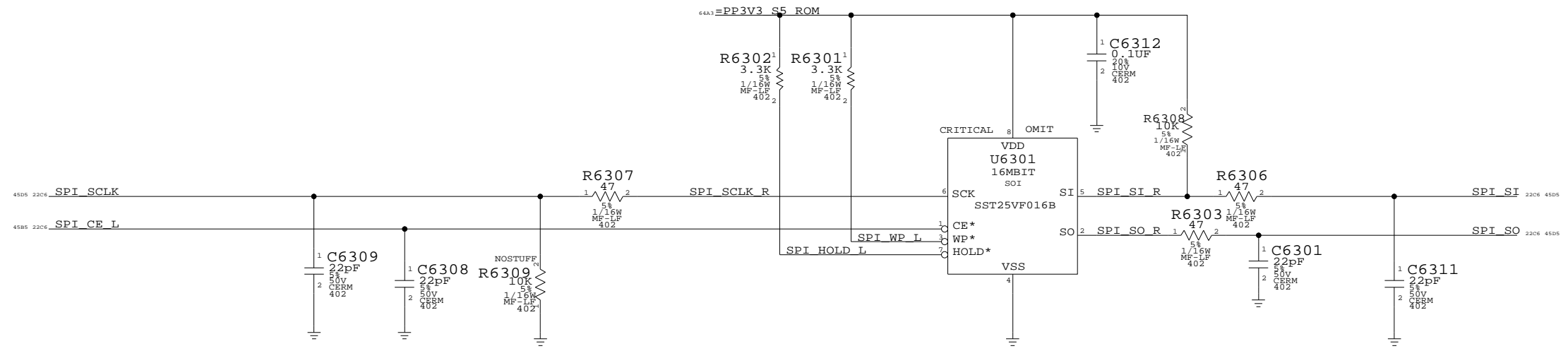


NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452 AND 518S0487
 AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.



TEMPERATURE SENSE		
SYNC_MASTER=ENET	SYNC_DATE=11/09/2005	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	49		



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
 R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM



SPI BOOTROM

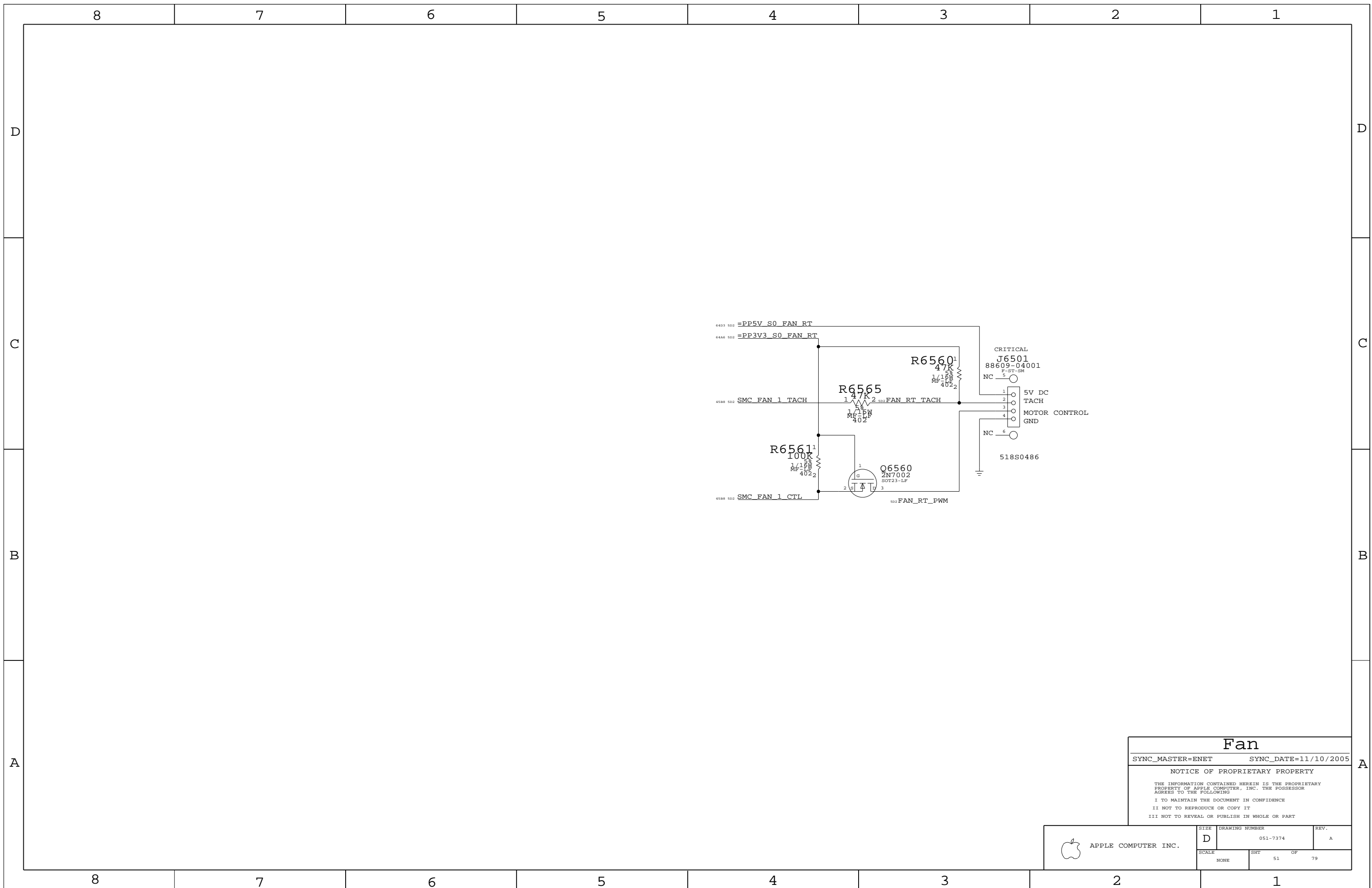
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 50	OF 79



Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

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	SCALE NONE	SHIT 51	OF 79

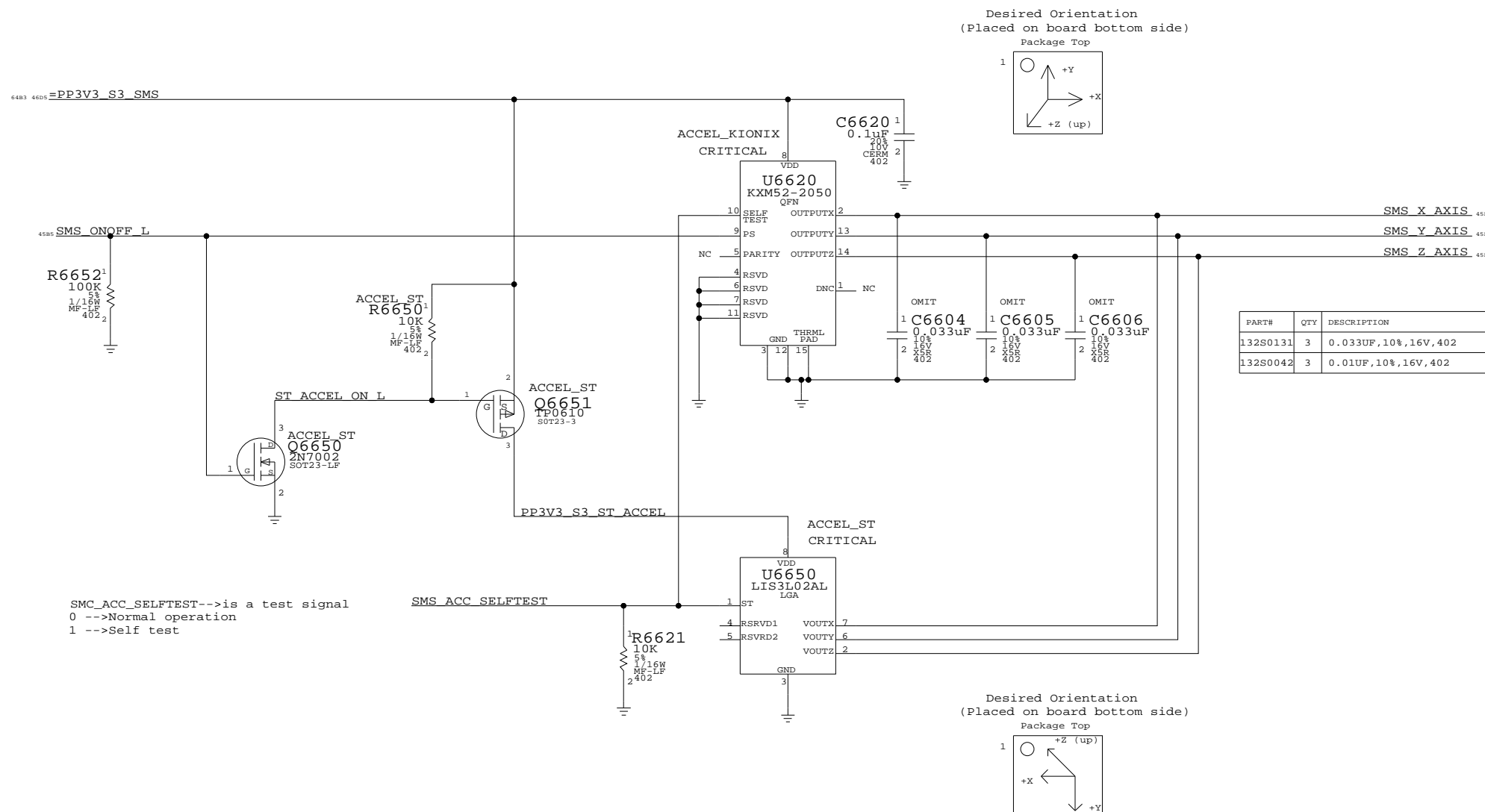
PAGE NOTES

INPUT
 =PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
 SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT
 SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
 7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
 7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
 7/26/2005 -



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMC_ACC_SELFTEST-->is a test signal
 0 -->Normal operation
 1 -->Self test

SMS

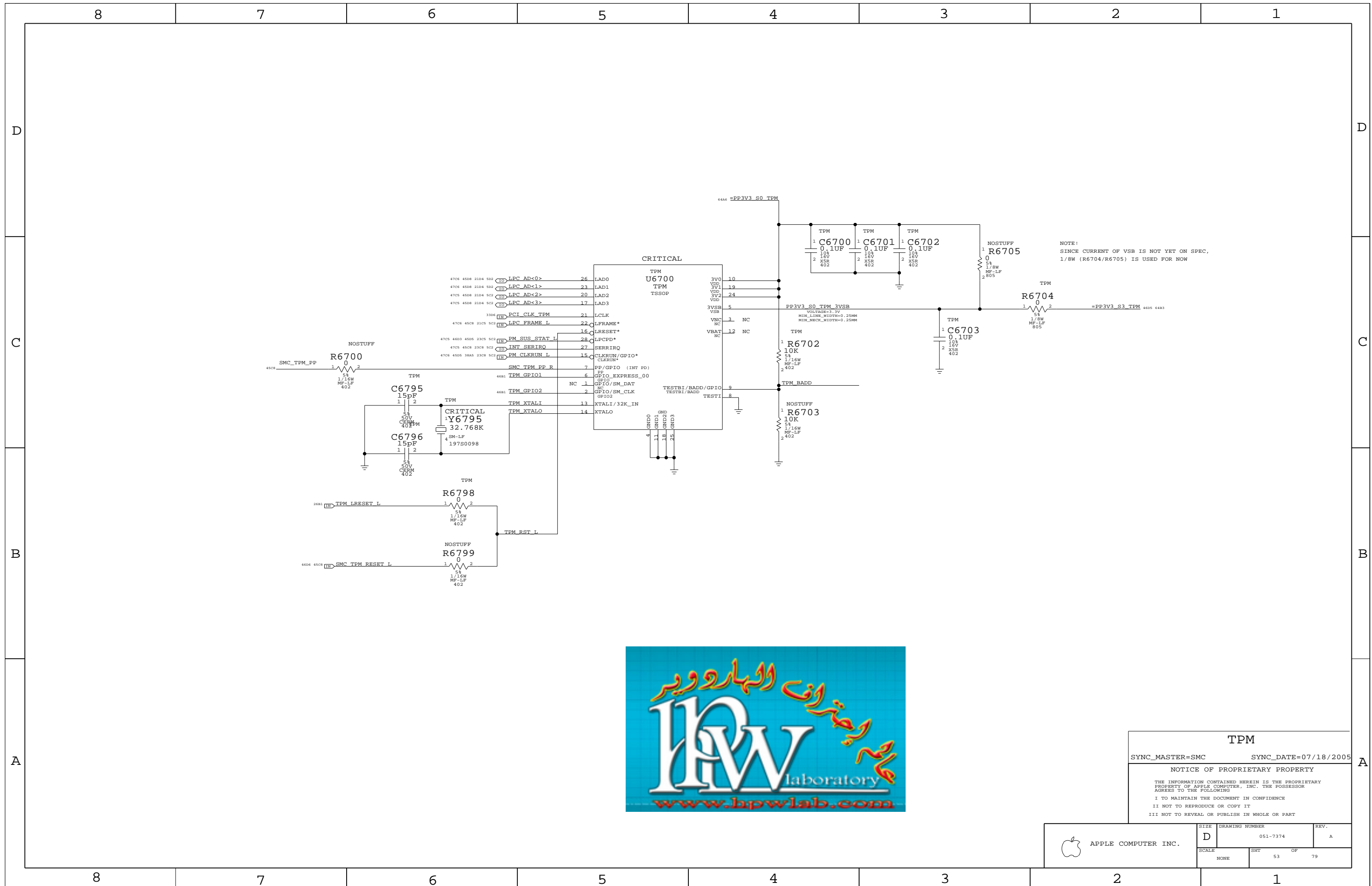
SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	52	79	



NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

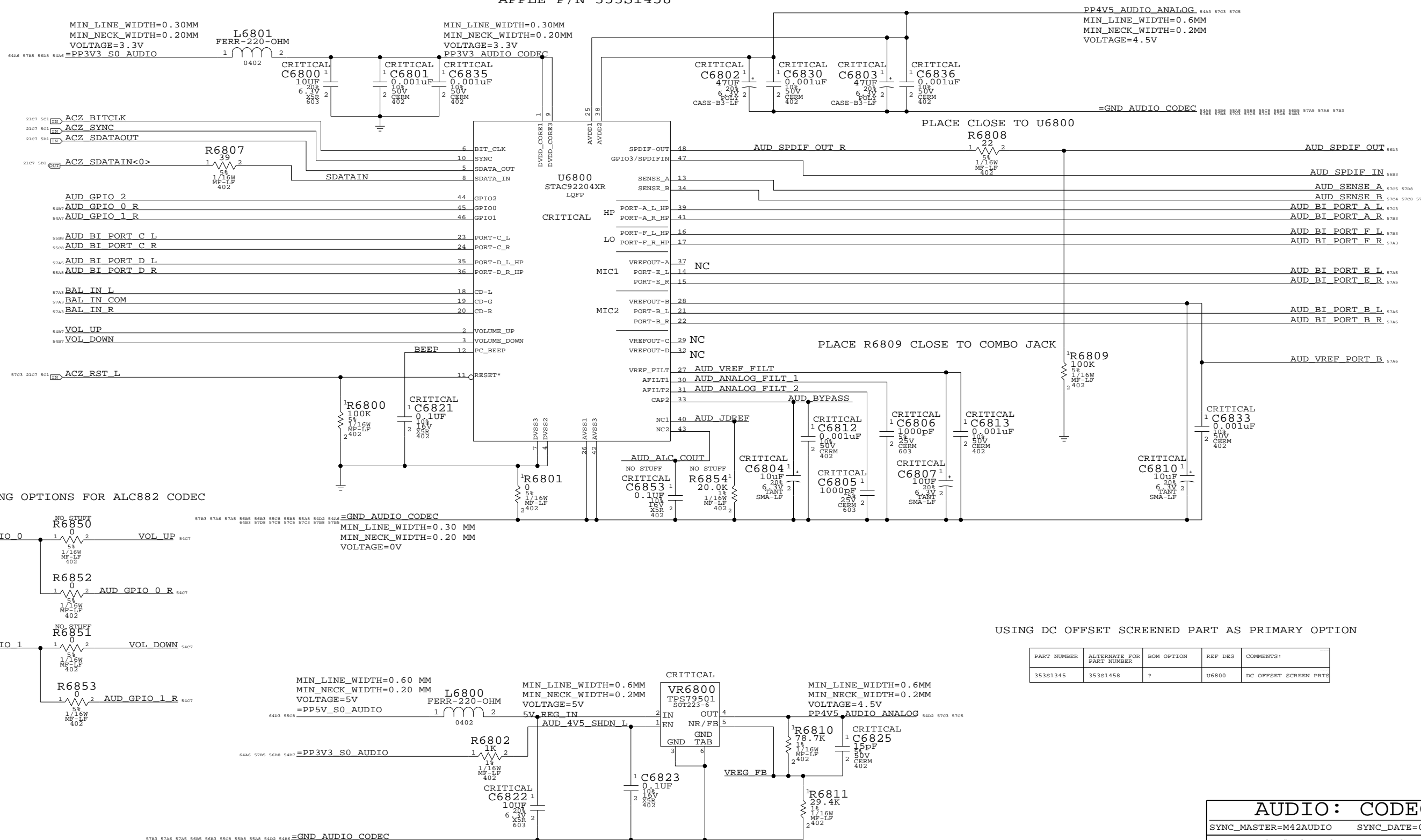


TPM
 SYNC_MASTER=SMC SYNC_DATE=07/18/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	53		

AUDIO CODEC

APPLE P/N 353S1458



STUFFING OPTIONS FOR ALC882 CODEC

USING DC OFFSET SCREENED PART AS PRIMARY OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1345	353S1458	?	U6800	DC OFFSET SCREEN PRTS

4.5V POWER SUPPLY FOR CODEC

AUDIO: CODEC

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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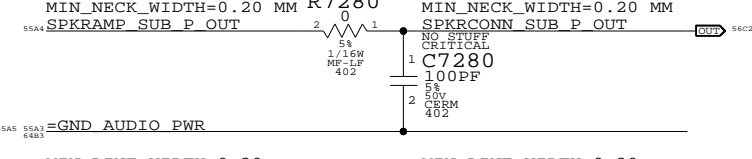
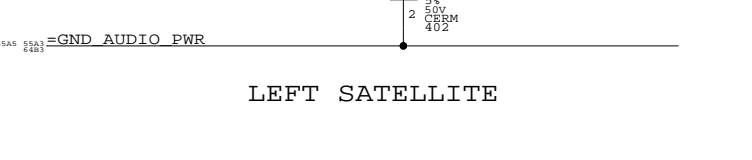
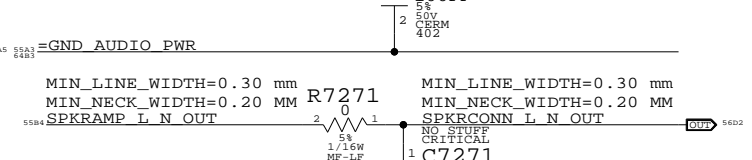
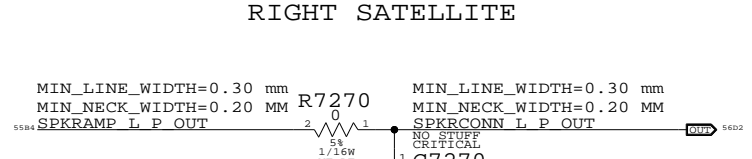
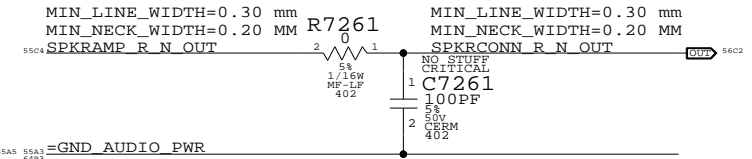
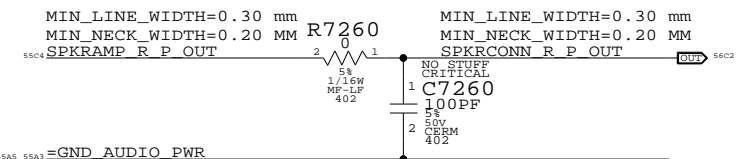
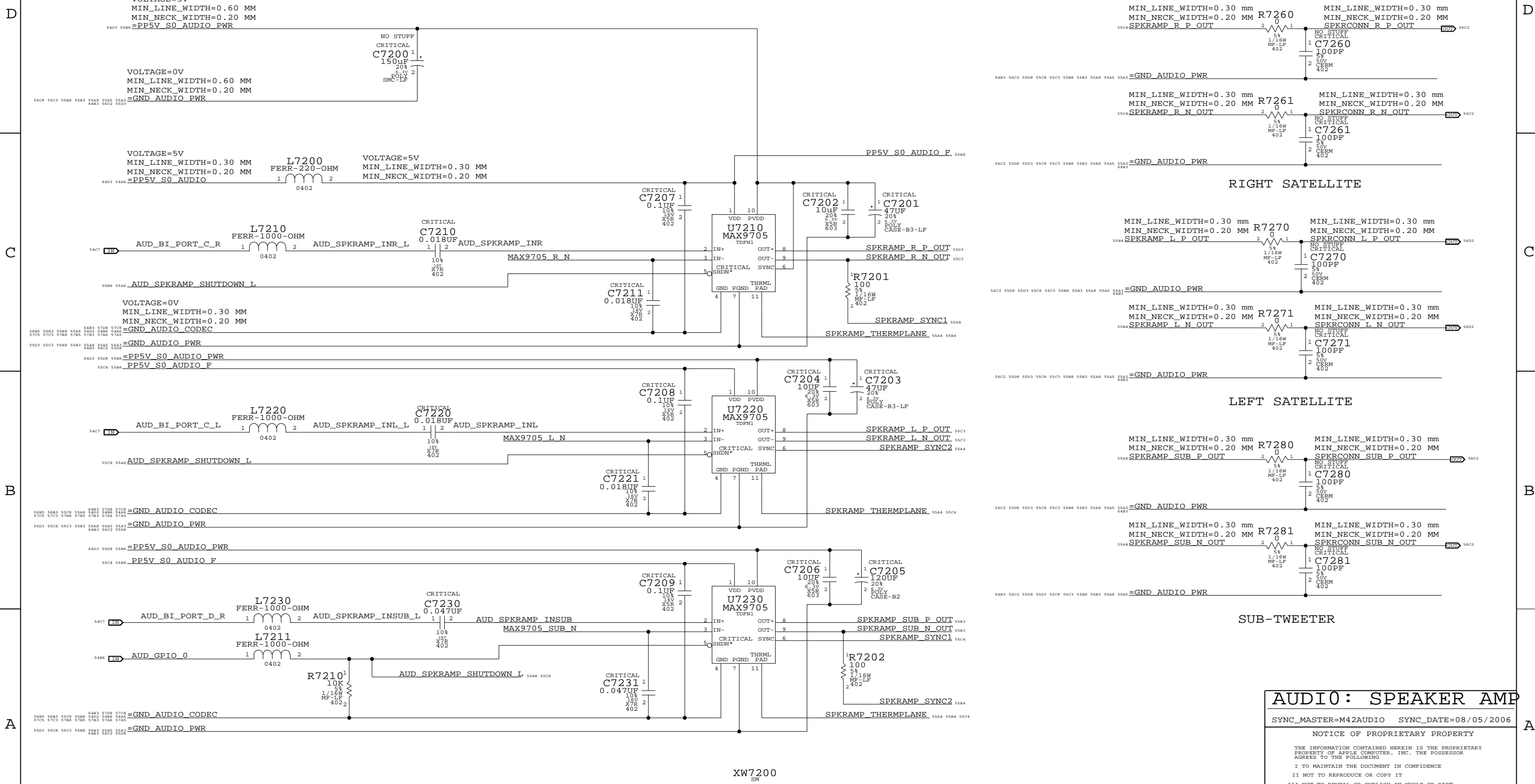
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	54		

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz
 SUB 169 Hz < FC < 282 Hz

SPEAKER OUTPUT EMI FILTERS



AUDIO: SPEAKER AMP
 SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	55	79	

XW7200

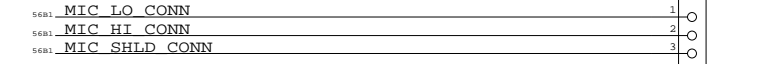
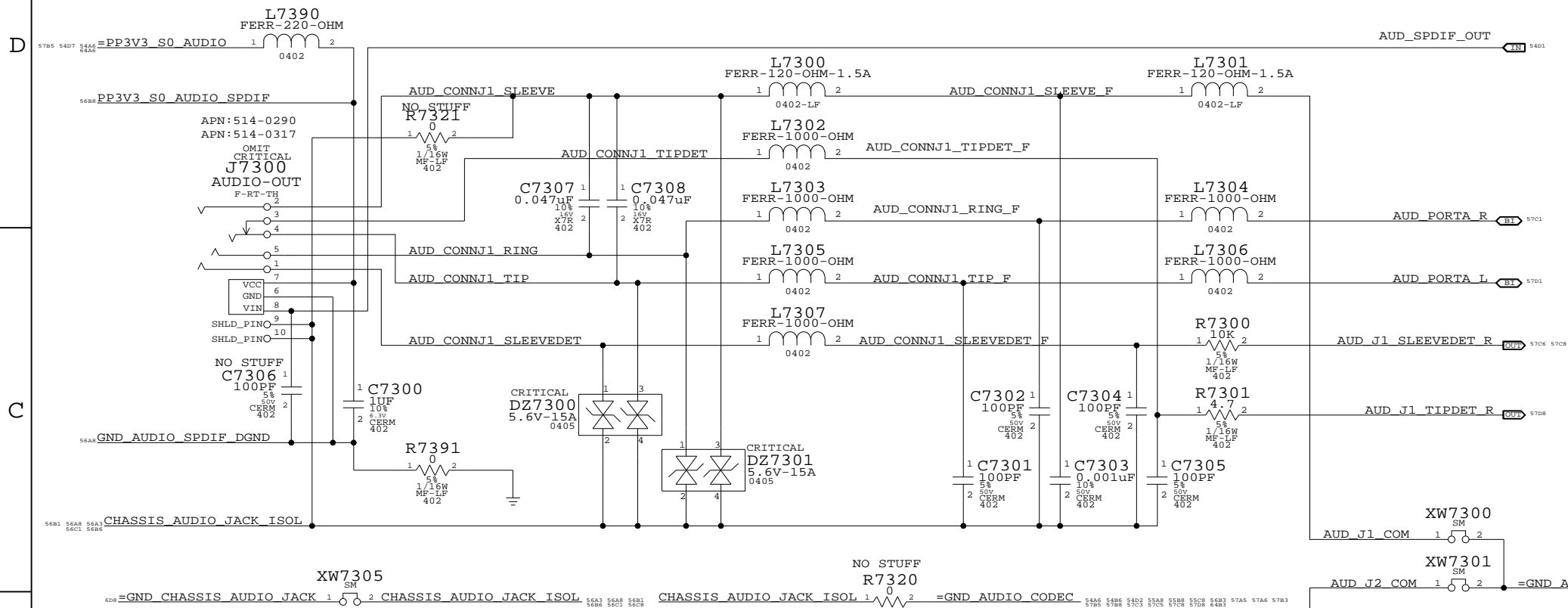
6483 56C2 55D8 55D3 55C8 55C3 55B8 55B3 55A8 55A3 55A1 =GND_AUDIO_PWR 1 2 SPKRAMP_THERMPLANE 55A4 55B4 55C4

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0491	518S0332	?	J7302	IMPROVED TWO PIN CONNECTOR

MIC CONNECTOR
APN:514S0392

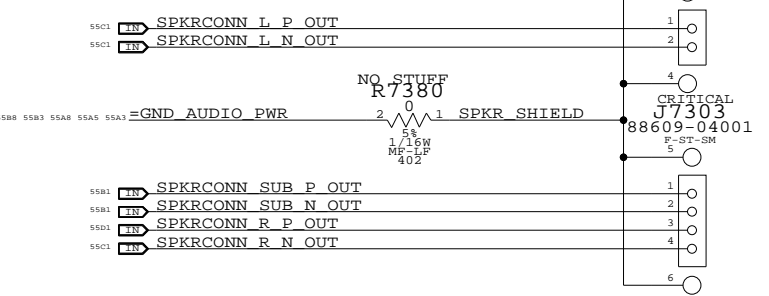
CRITICAL
J7301
48227-0301
M-RT-SM1
4

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

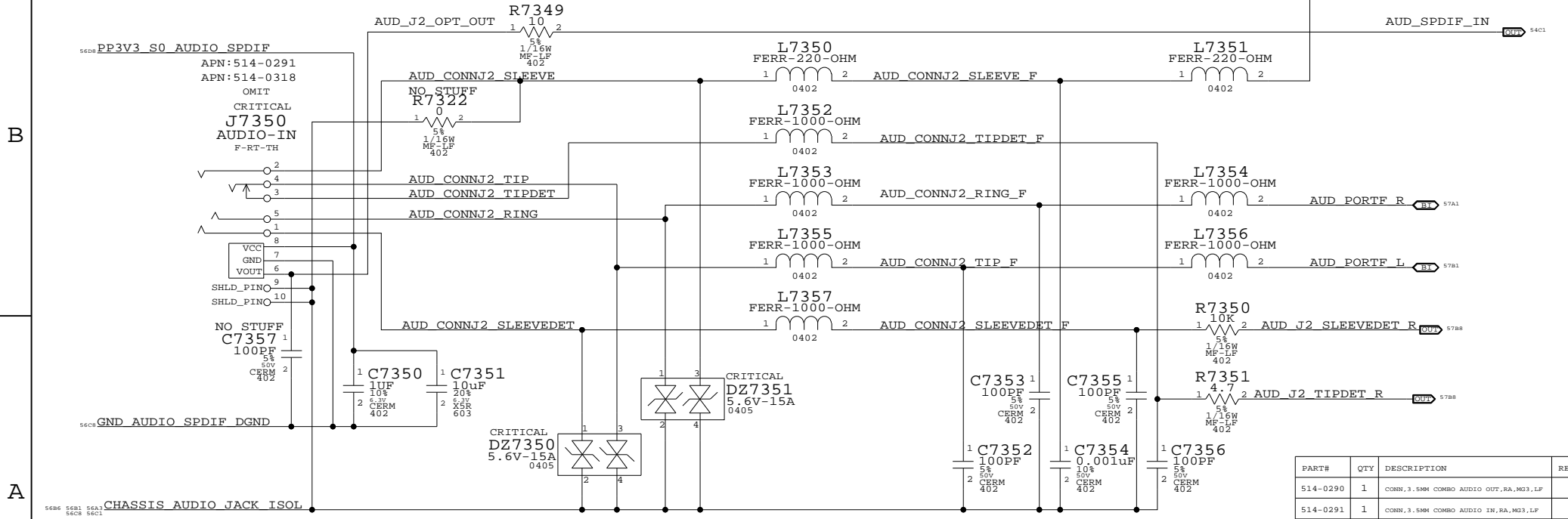
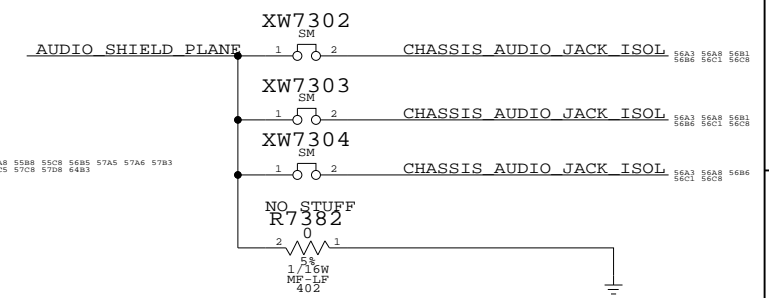


SPEAKER CONNECTOR
APN:518S0332

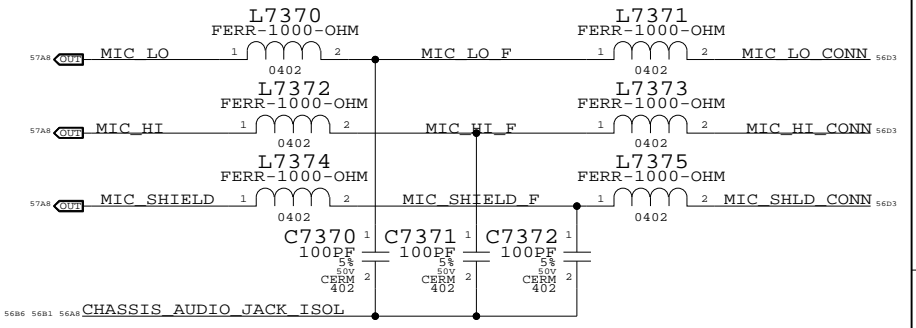
CRITICAL
J7302
88611-02001
F-ST-SM
3



REPLACE 518S0334 WITH 518S0486
AUDIO SHIELD FILL



MIC EMI FILTER



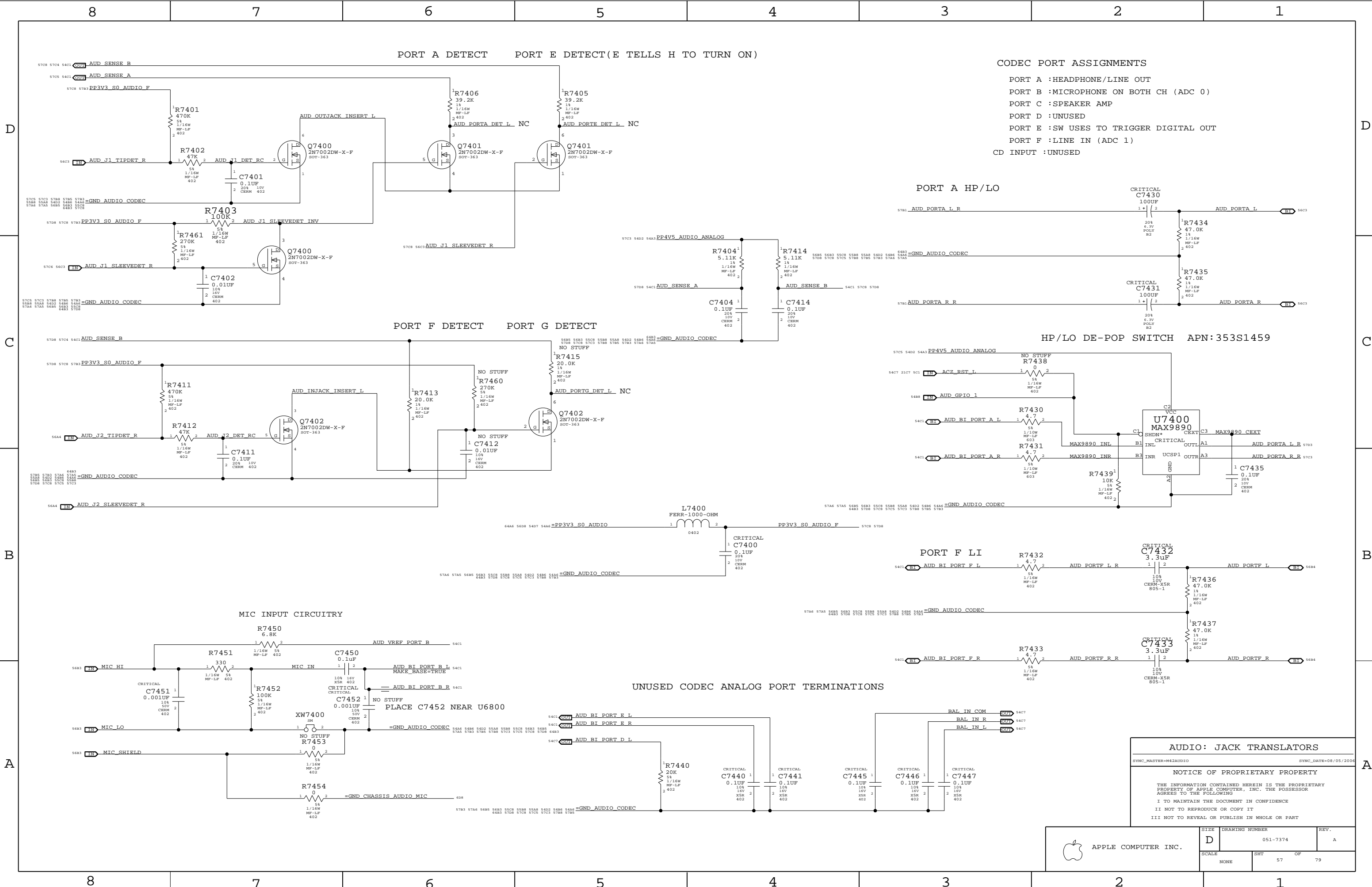
AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN, 3.5MM COMBO AUDIO OUT, RA, MG3, LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J7300	CRITICAL	FANCY
514-0318	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J7350	CRITICAL	FANCY

AUDIO: JACK
SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006
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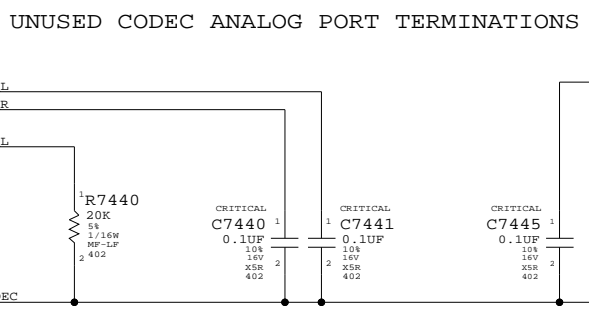
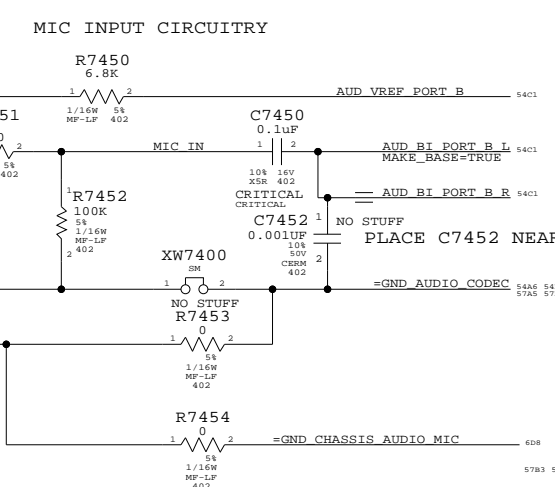
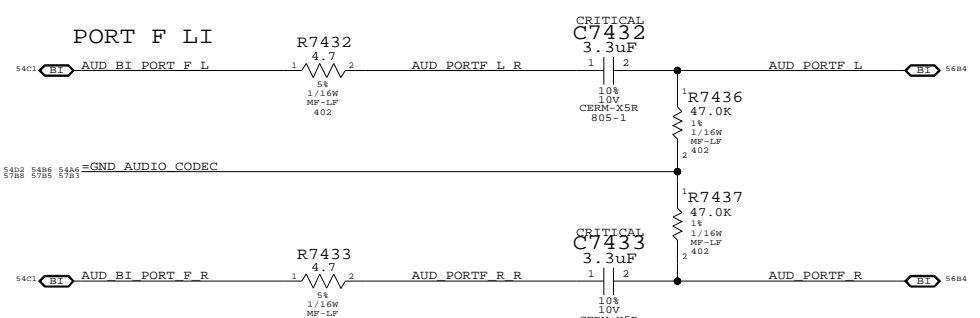
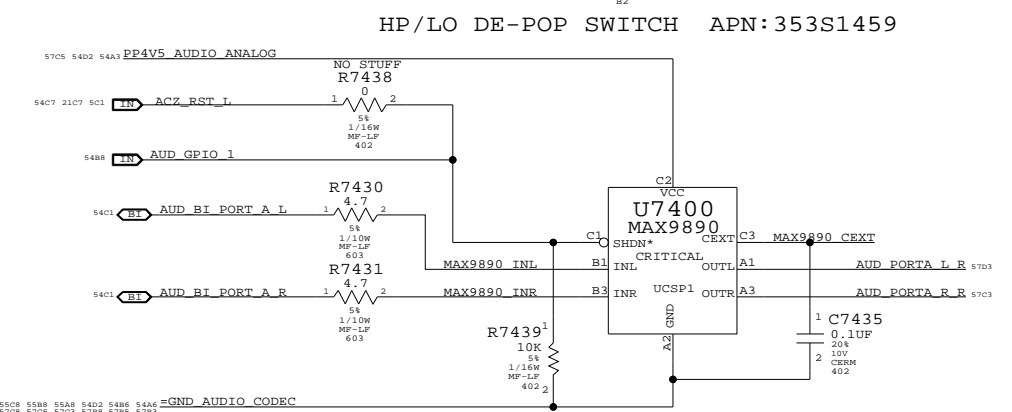
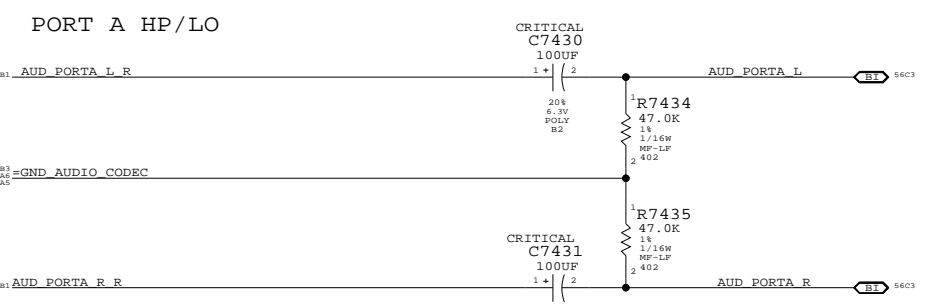
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7374	A
SCALE	SHT	OF
NONE	56	79



CODEC PORT ASSIGNMENTS

PORT A : HEADPHONE/LINE OUT
 PORT B : MICROPHONE ON BOTH CH (ADC 0)
 PORT C : SPEAKER AMP
 PORT D : UNUSED
 PORT E : SW USES TO TRIGGER DIGITAL OUT
 PORT F : LINE IN (ADC 1)
 CD INPUT : UNUSED



AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

NOTICE OF PROPRIETARY PROPERTY

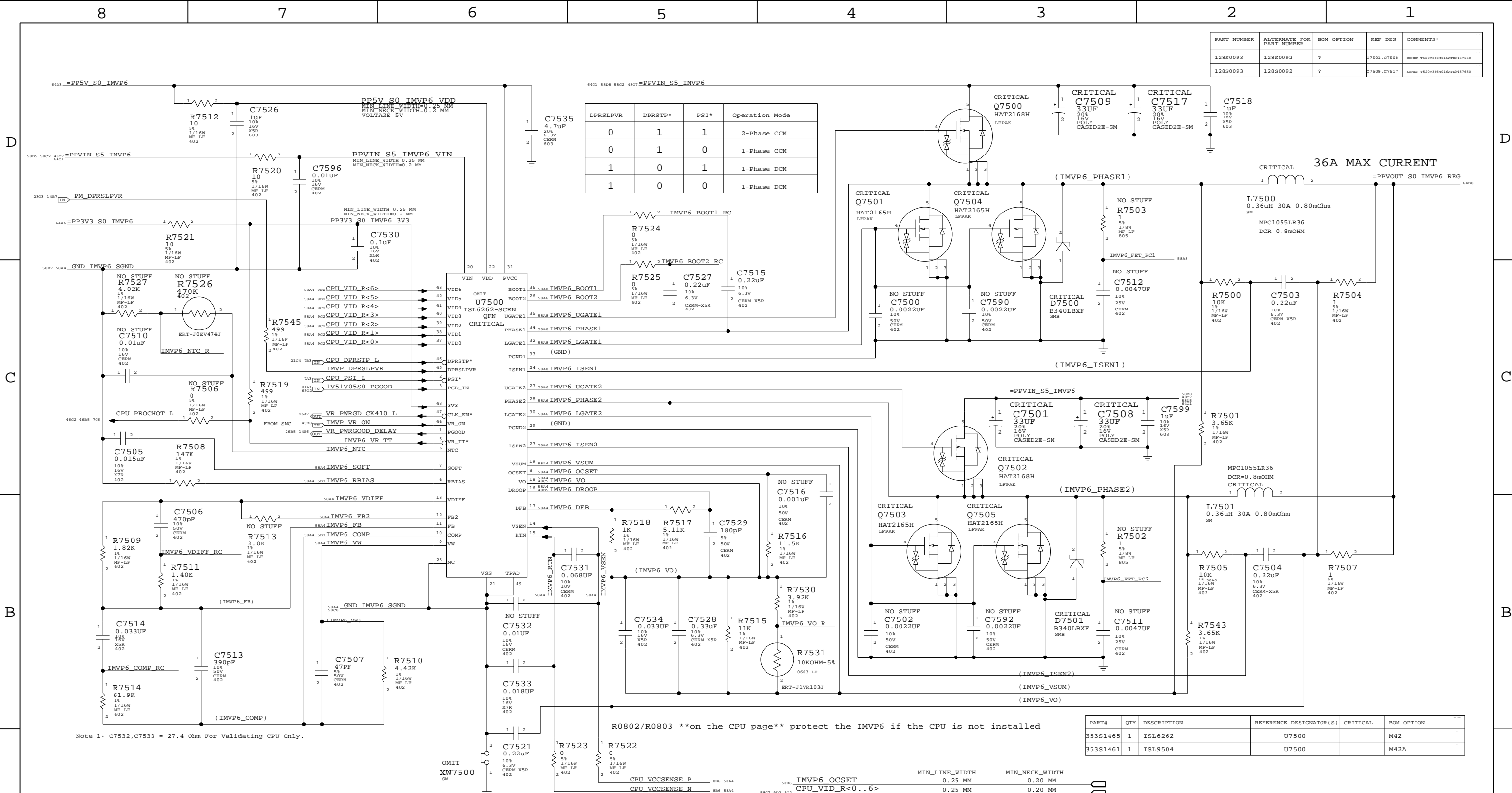
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	57	79	A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7501_C7508	RENET T520V3300016ATE0457650
128S0093	128S0092	?	C7509_C7517	RENET T520V3300016ATE0457650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM



Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

IMVP6 CPU VCore Regulator

MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM 0.25 MM
IMVP6_BOOT1	0.25 MM 0.25 MM
IMVP6_UGATE1	1.5 MM 0.25 MM
IMVP6_LGATE1	1.5 MM 0.25 MM
IMVP6_ISEN1	0.25 MM 0.25 MM
IMVP6_FET_RC1	0.25 MM 0.25 MM
IMVP6_VSUM_R1	0.25 MM 0.25 MM
IMVP6_VO_R1	0.25 MM 0.25 MM

MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM 0.25 MM
IMVP6_BOOT2	0.25 MM 0.25 MM
IMVP6_UGATE2	0.25 MM 0.25 MM
IMVP6_LGATE2	0.25 MM 0.25 MM
IMVP6_ISEN2	0.25 MM 0.25 MM
IMVP6_FET_RC2	0.25 MM 0.25 MM
IMVP6_VSUM_R2	0.25 MM 0.25 MM
IMVP6_VO_R2	0.25 MM 0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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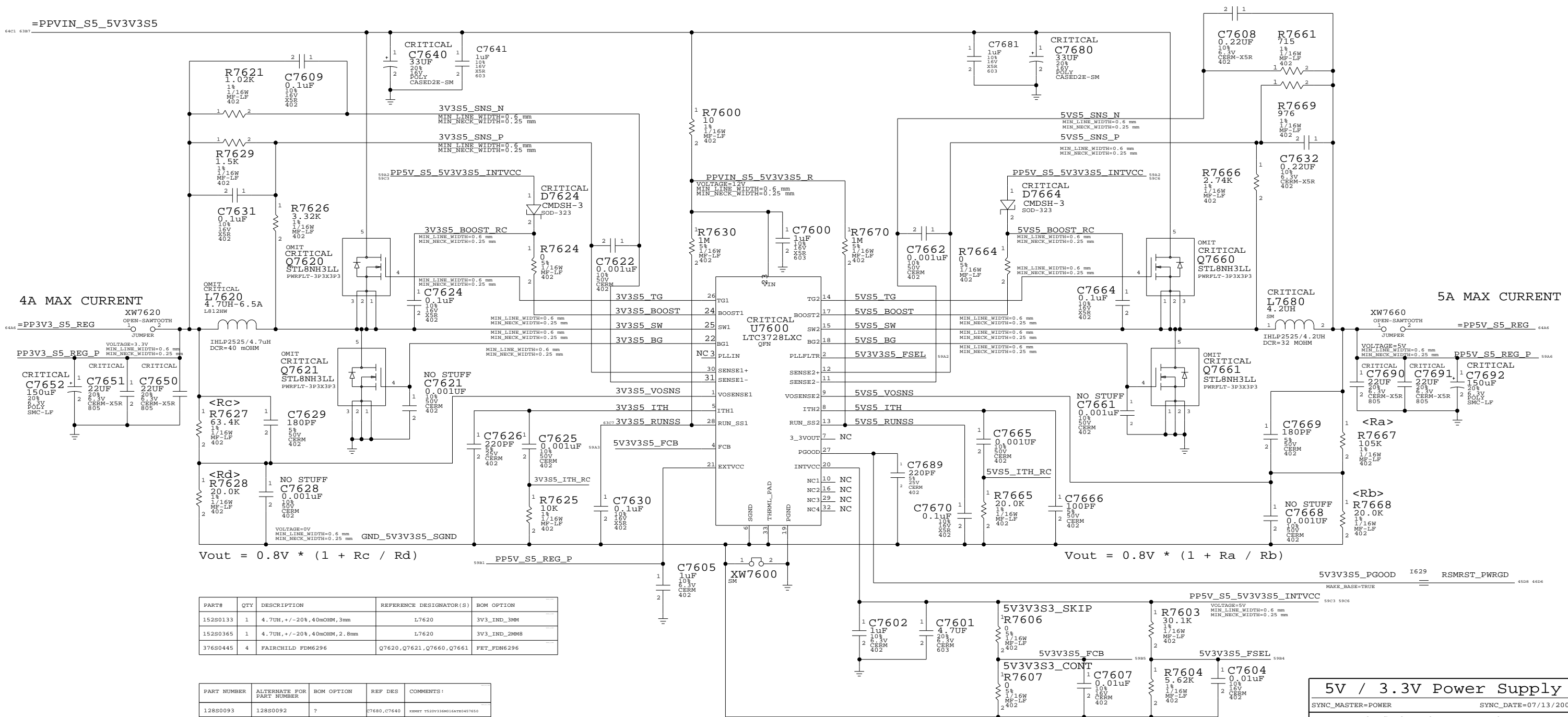
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	58		

5V / 3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0133	1	4.7UH, +/-20%, 40mOHM, 3mm	L7620	3V3_IND_3MM
152S0365	1	4.7UH, +/-20%, 40mOHM, 2.8mm	L7620	3V3_IND_2MM8
376S0445	4	FAIRCHILD FDM6296	Q7620, Q7621, Q7660, Q7661	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7680, C7640	RENET VS20V33M016ATE0487650
376S0448	376S0445	?	Q7620, Q7621	VISHAY SI7806ADN
376S0448	376S0445	?	Q7660, Q7661	VISHAY SI7806ADN

5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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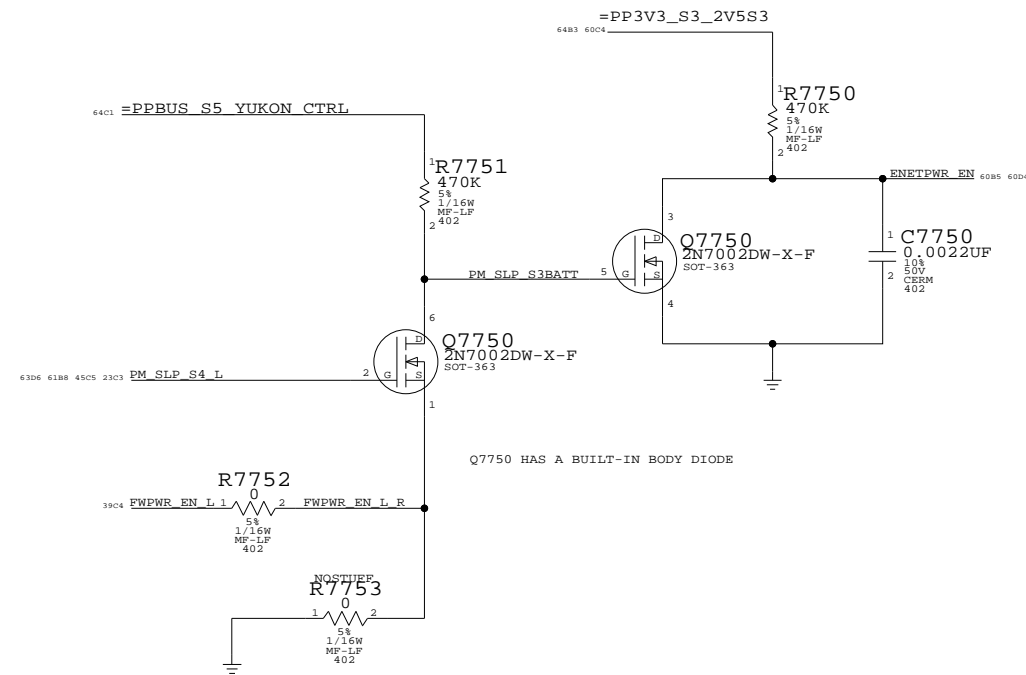
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	59		

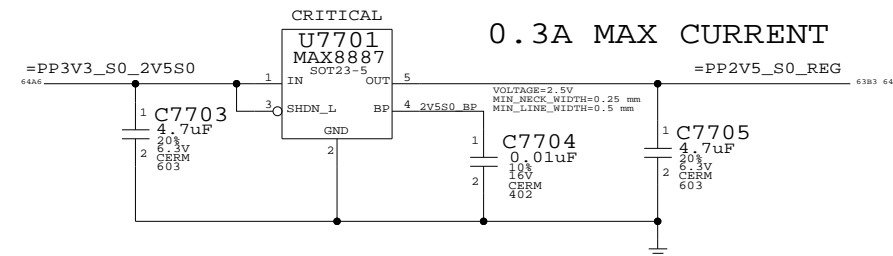
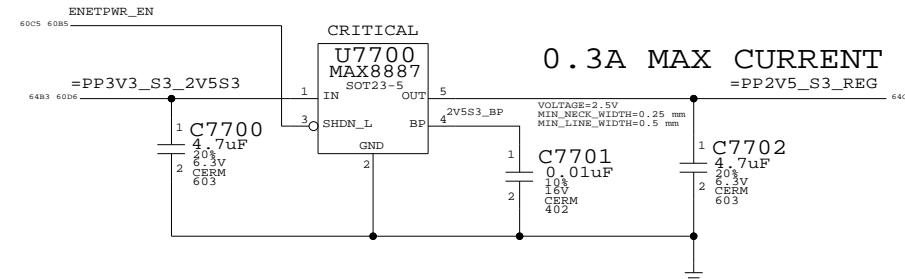
YUKON POWER CONTROL



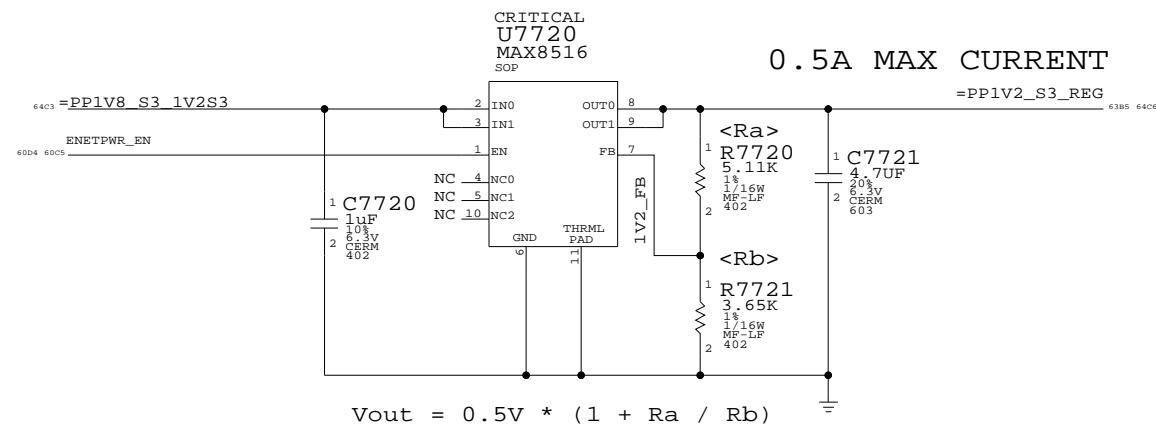
NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 S0	~S0 ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L

2.5V REGULATORS



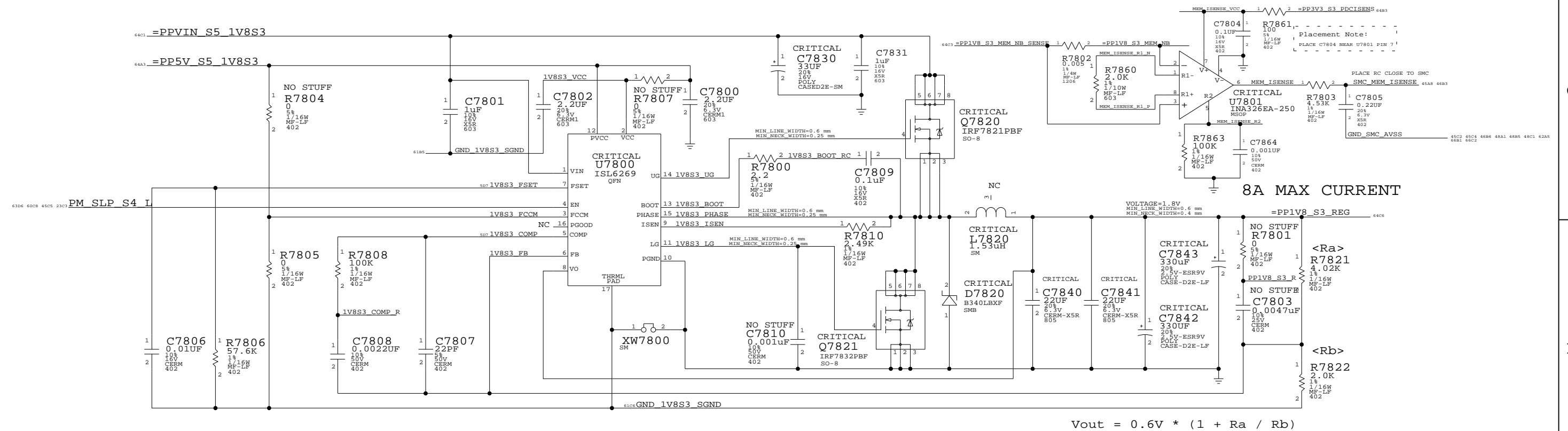
1.2V REGULATOR



2.5V/1.2V Regulator
 SYNC_MASTER=ENET SYNC_DATE=12/06/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	REV.
NONE	60	79	

1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	ERRY 0520V330M16AT00457450

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842, C7843	PANASONIC EEP5X0D3311R
128S0095	128S0060	?	C7842, C7843	PANASONIC EEP5X0D3311K



1.8V Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

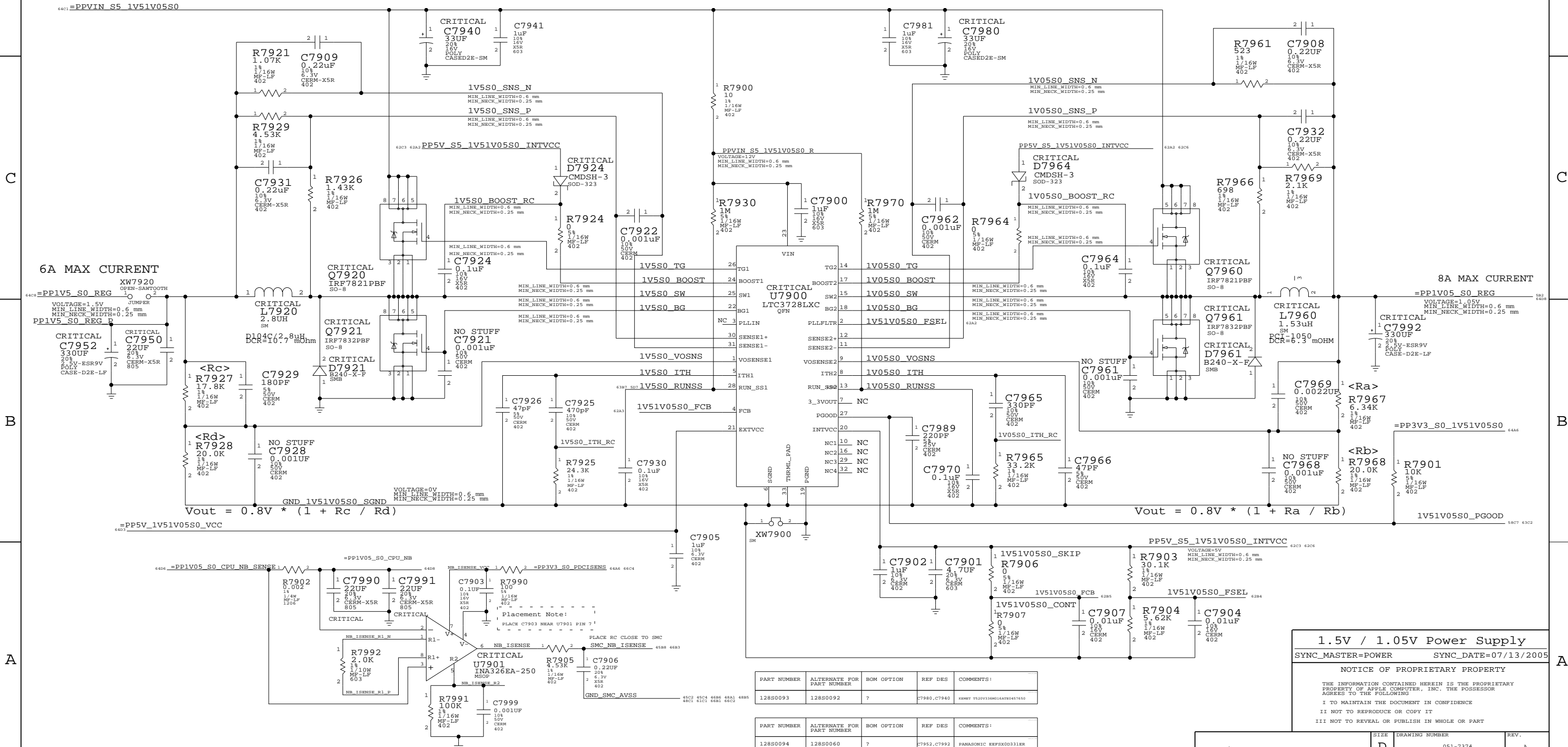
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	61		

1.5V/1.05V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7980, C7940	RENT 7520V3H001A480457450
128S0094	128S0060	?	C7952, C7992	PANASONIC EEPX003311E
128S0095	128S0060	?	C7952, C7992	PANASONIC EEPX003311E

1.5V / 1.05V Power Supply
 SYNC_MASTER=POWER SYNC_DATE=07/13/2005
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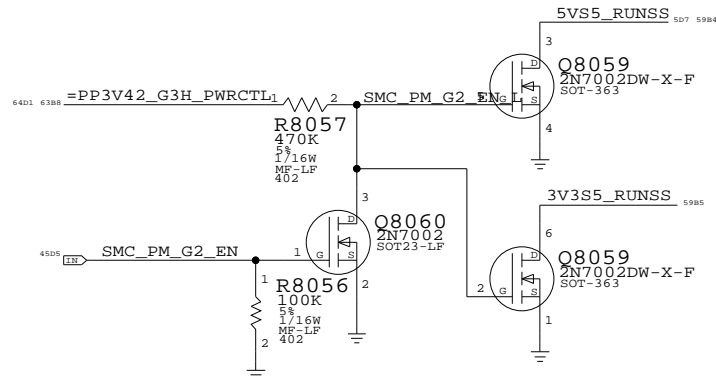
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	62		

POWER CONTROL SIGNALS

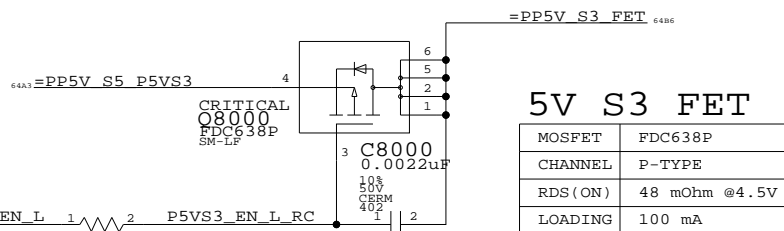
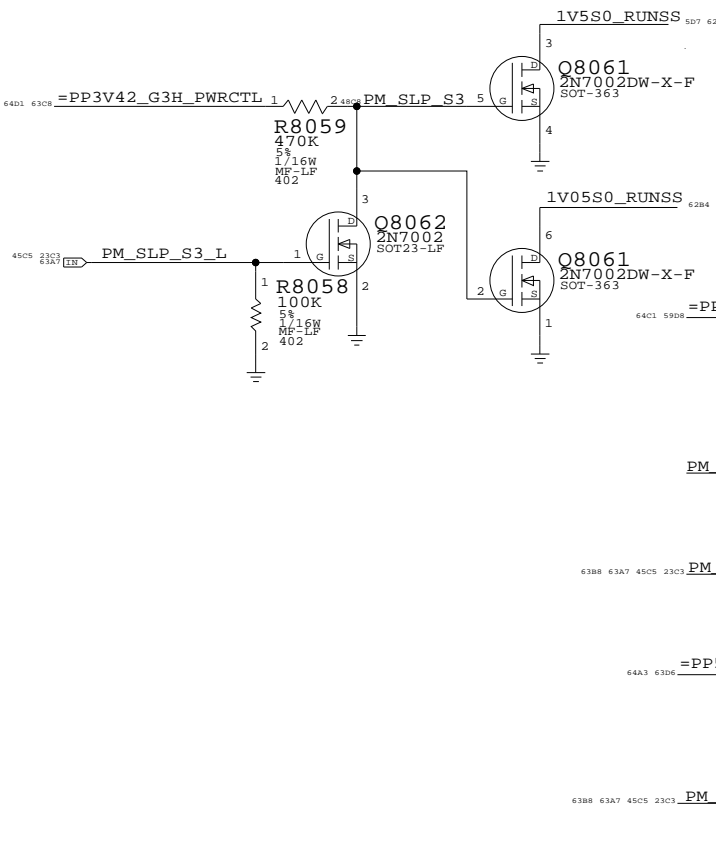
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

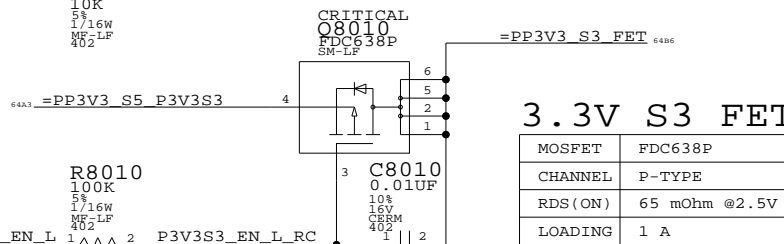
5V/3.3V S5 RUN/SS CONTROL



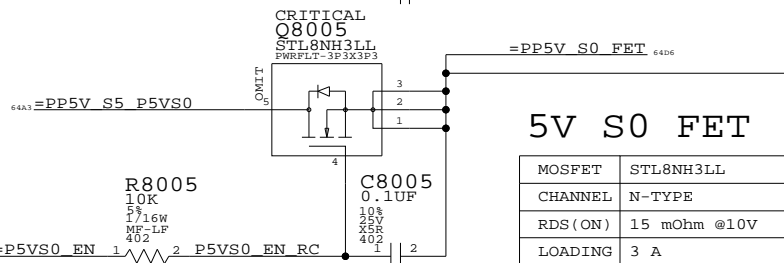
1.5V/1.05V S0 RUN/SS CONTROL



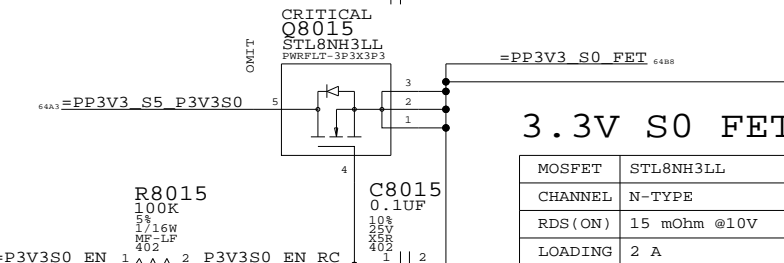
5V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA



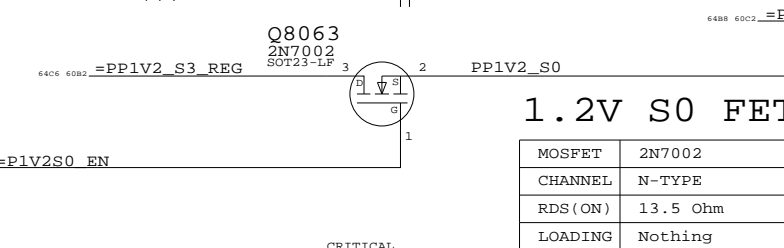
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A



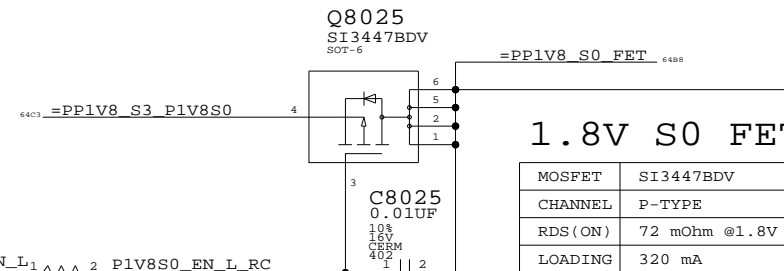
5V S0 FET	
MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A



3.3V S0 FET	
MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A



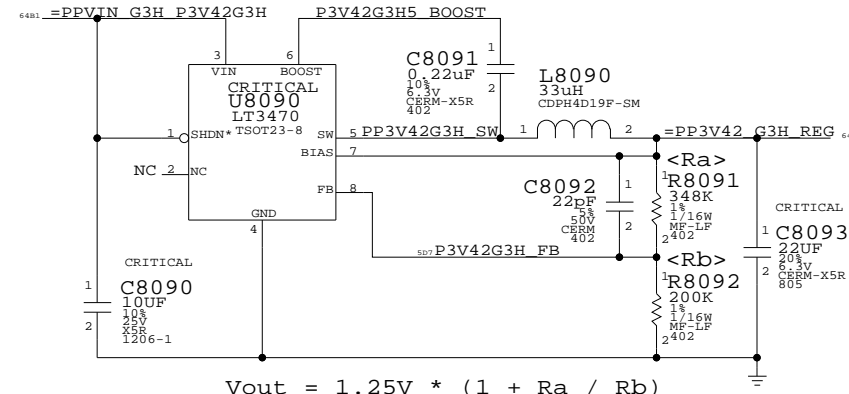
1.2V S0 FET	
MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing



1.8V S0 FET	
MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

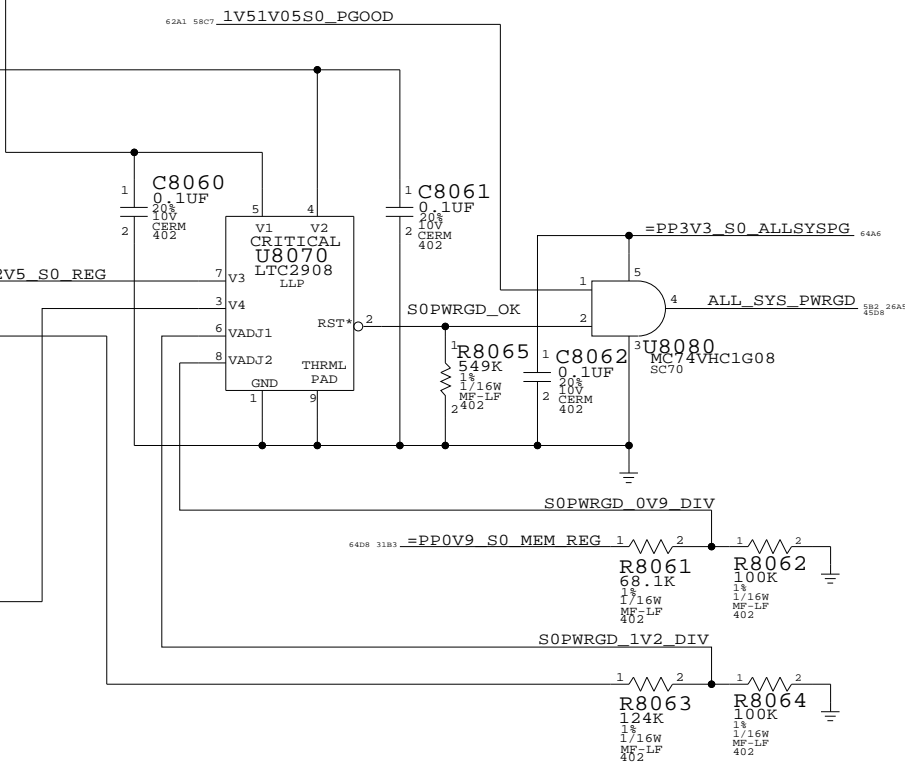
3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



$$V_{out} = 1.25V * (1 + R_a / R_b)$$

ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005, Q8015	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005, Q8015	VISHAY SI7806ADN

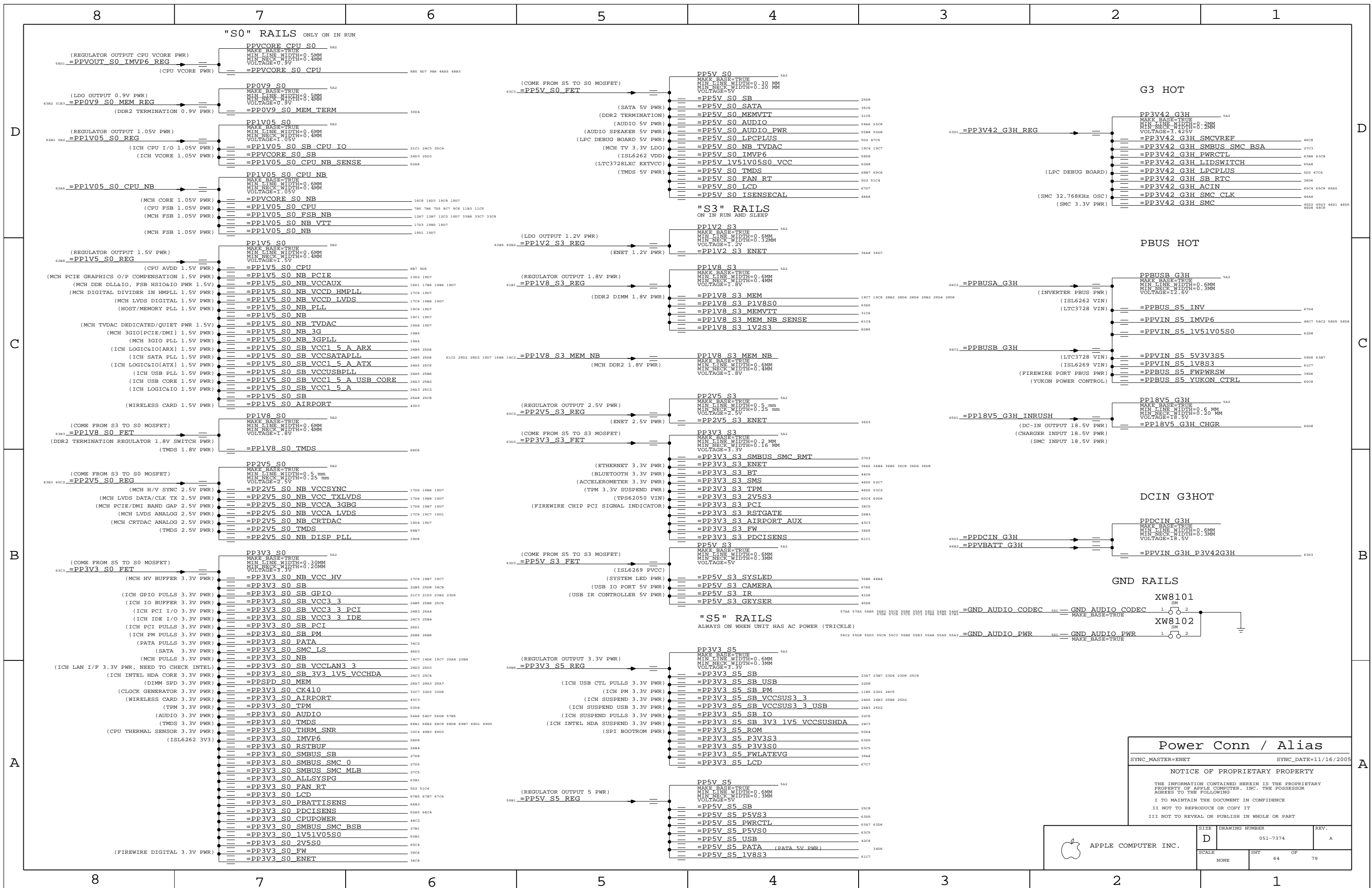
S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	63		



Power Conn / Alias

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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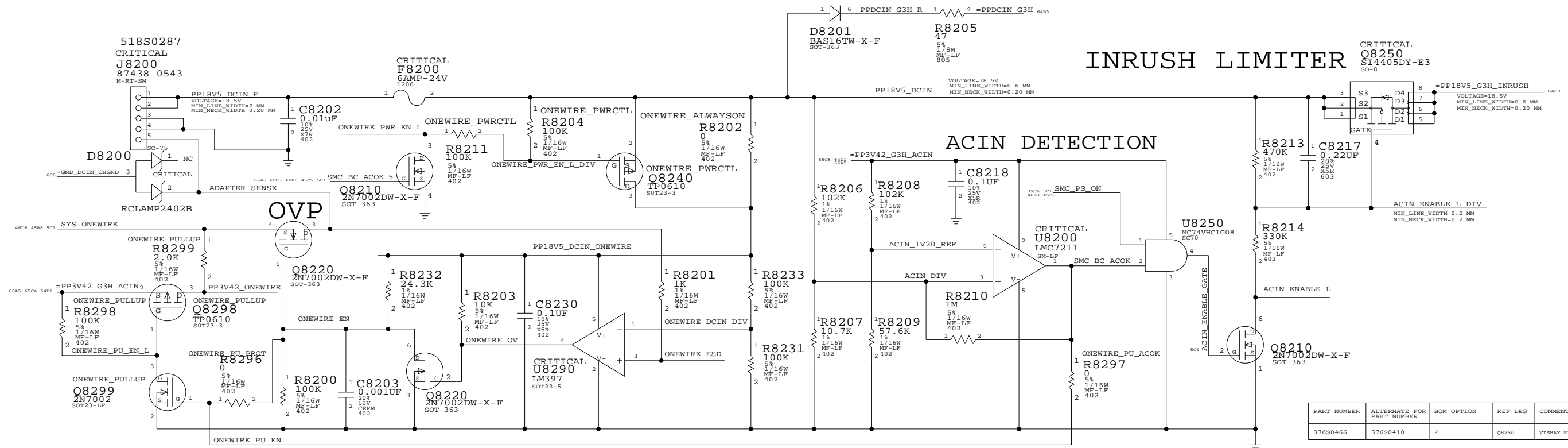
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	DRAWING NUMBER		REV.
	D 051-7374		A
SCALE		SHT	OF
NONE		64	79

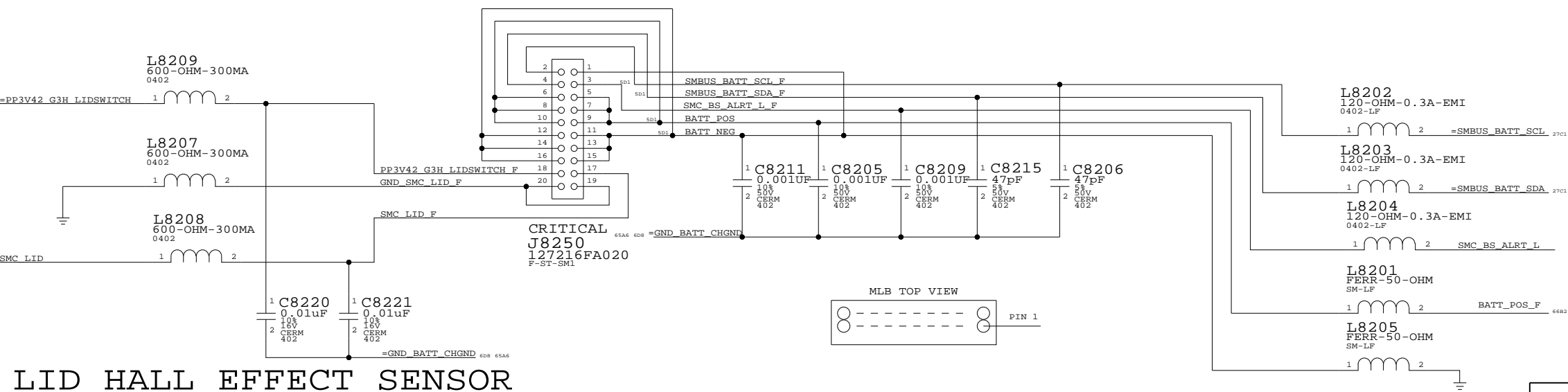
DC-JACK INTERFACE

INRUSH LIMITER

ACIN DETECTION



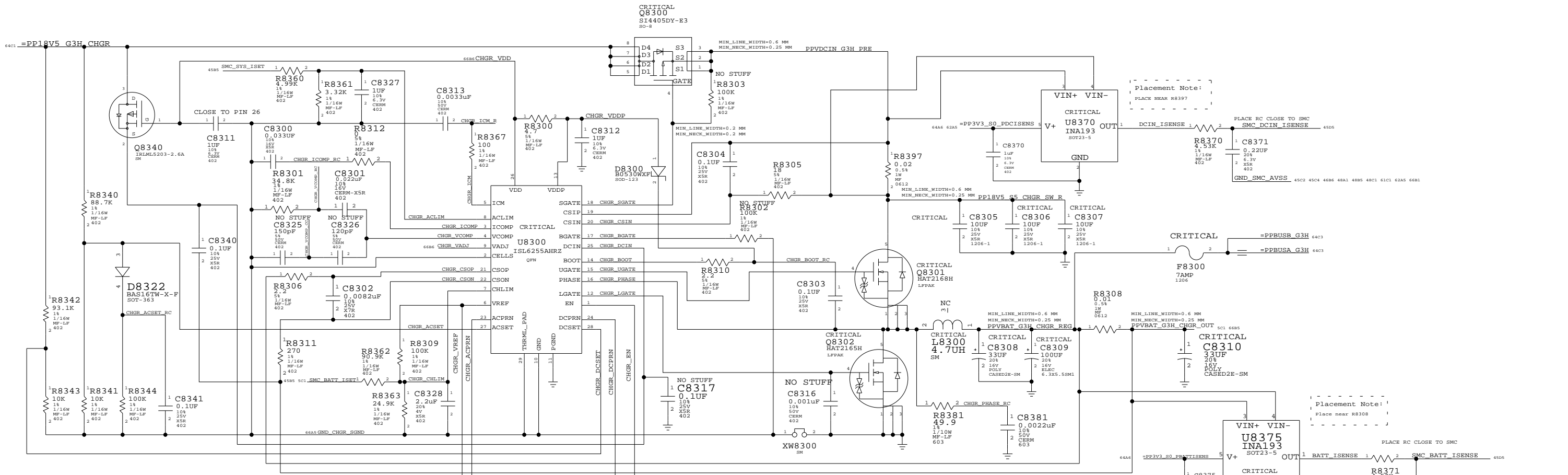
BATTERY INTERFACE



LID HALL EFFECT SENSOR

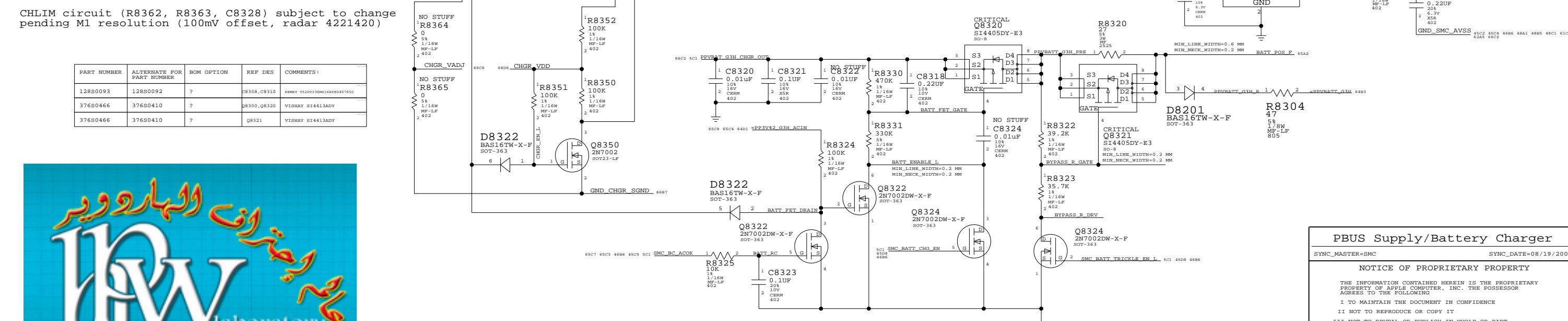
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	65		

PBUS SUPPLY / BATTERY CHARGER



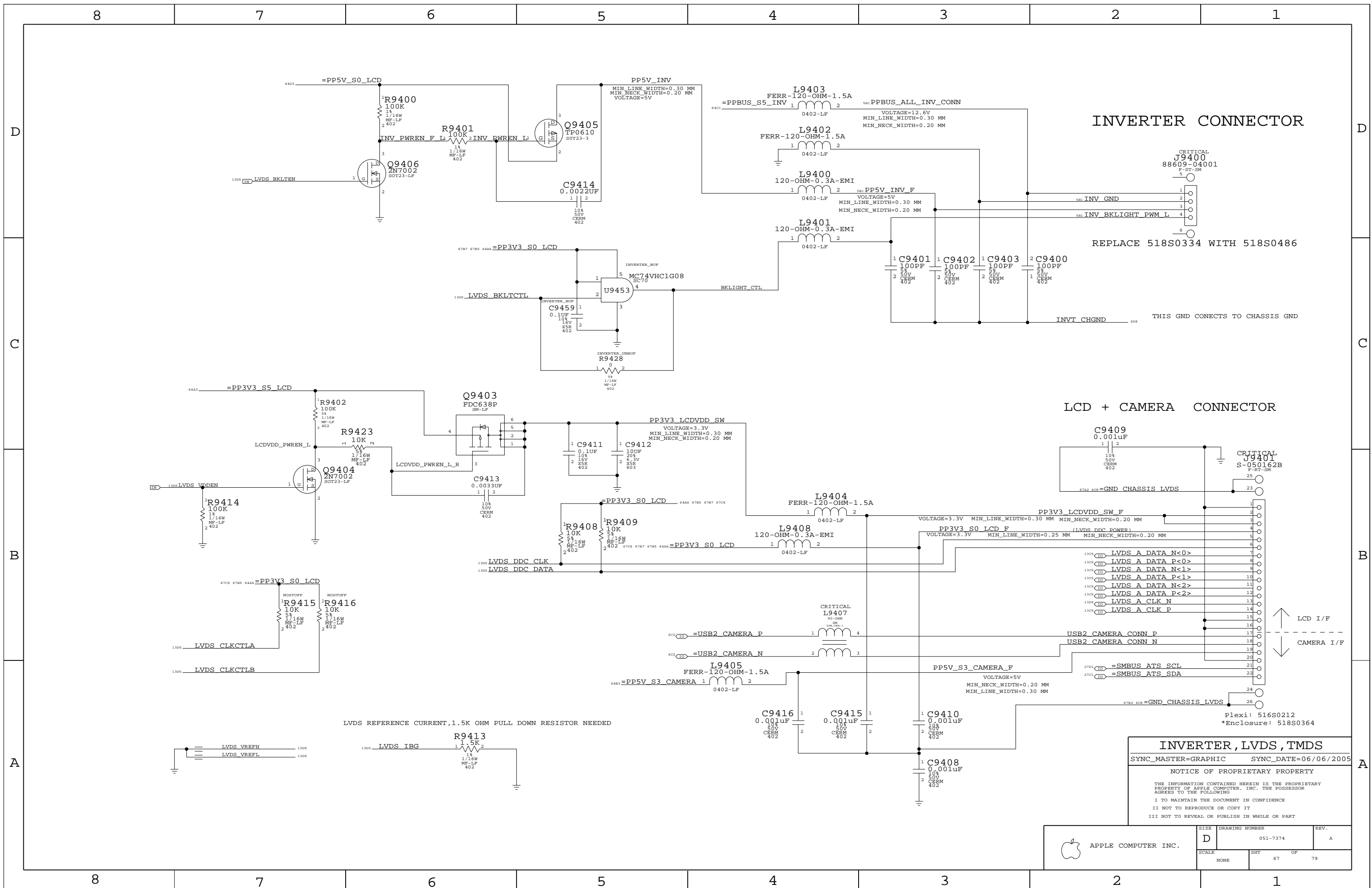
CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mV offset, radar 4221420)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS 1
128S0093	128S0092	?	C8308, C8310	KEMET T520V33M018AT00457650
376S0466	376S0410	?	Q8300, Q8320	VISHAY S14413ADY
376S0466	376S0410	?	Q8321	VISHAY S14413ADY



PBUS Supply/Battery Charger
 SYNC_MASTER=SMC SYNC_DATE=08/19/2005
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 66	OF 79



INVERTER CONNECTOR

CRITICAL
J9400
88609-04001
F-ST-SM

REPLACE 518S0334 WITH 518S0486

THIS GND CONNECTS TO CHASSIS GND

LCD + CAMERA CONNECTOR

CRITICAL
J9401
S-050162B
F-RT-SM

LVDS A DATA N<0>
LVDS A DATA P<0>
LVDS A DATA N<1>
LVDS A DATA P<1>
LVDS A DATA N<2>
LVDS A DATA P<2>
LVDS A CLK N
LVDS A CLK P

USB2 CAMERA CONN P
USB2 CAMERA CONN N

=SMBUS_ATS_SCL
=SMBUS_ATS_SDA

Plexi: 516S0212
*Enclosure: 518S0364

INVERTER, LVDS, TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

NOTICE OF PROPRIETARY PROPERTY

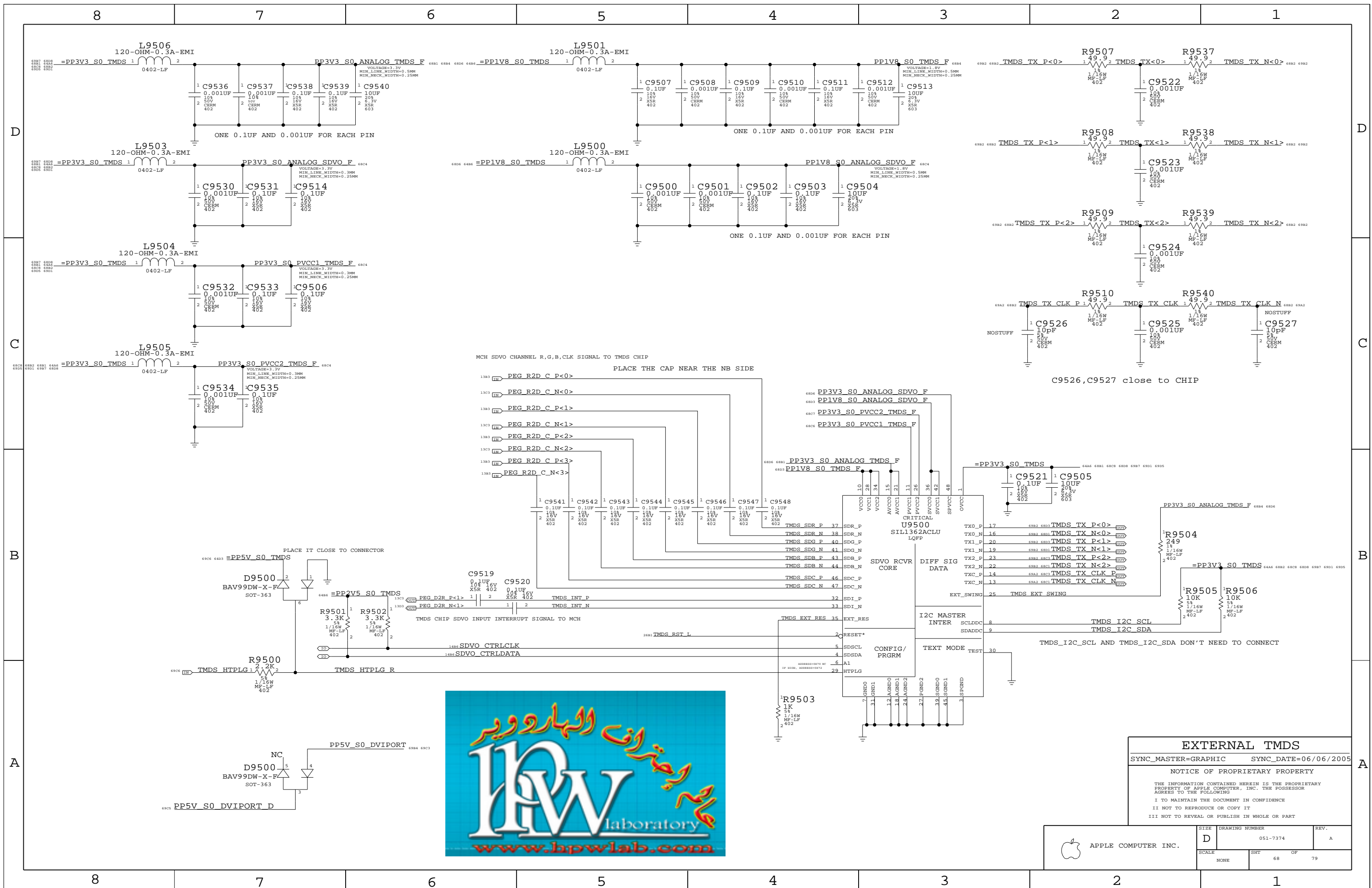
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	67		



EXTERNAL TMSD

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7374	REV. A
	SCALE NONE	SHEET 68	OF 79

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
15580227	15580164	?	REF: 15580164	KEEP MAG LAYER IN BOX

Video Connectors

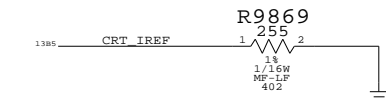
EXTERNAL VIDEO (VGA) INTERFACE

TMDS(MINI DVI) INTERFACE

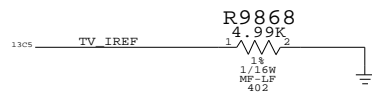
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

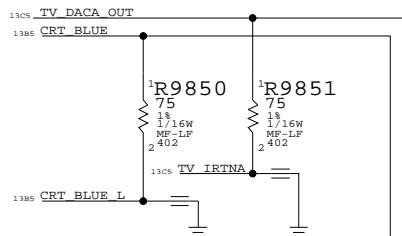
A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND



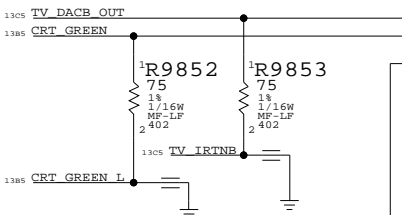
TV REFERENCE CURRENT, USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS



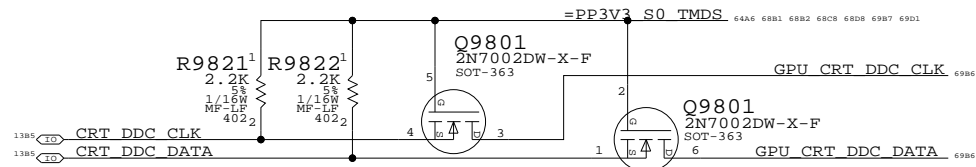
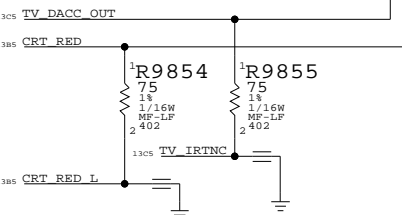
PLACE THE RESISTOR CLOSE TO GMCH



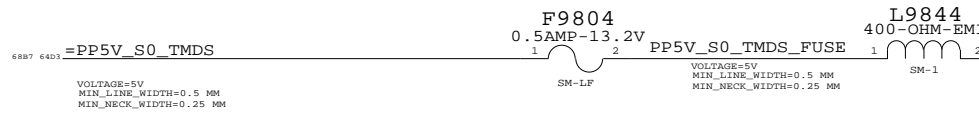
PLACE THE RESISTOR CLOSE TO GMCH



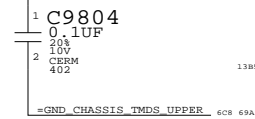
PLACE THE RESISTOR CLOSE TO GMCH



Isolation required for DVI power switch

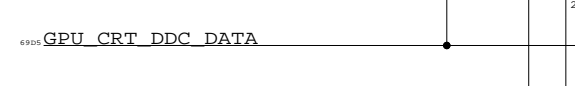
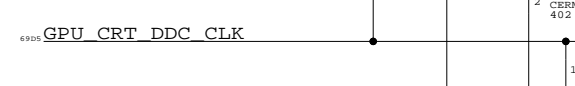
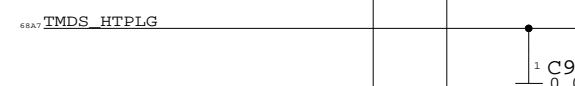


VOLTAGE=5V
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.25 MM

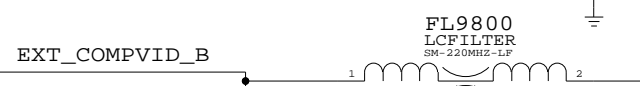
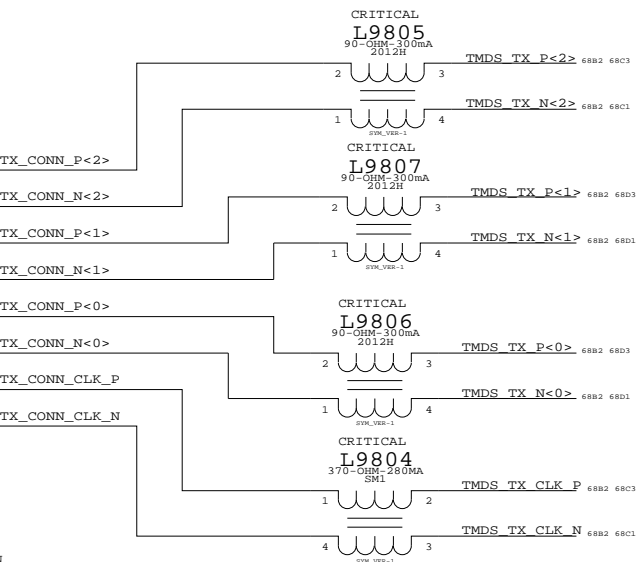
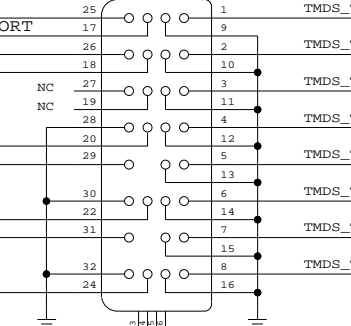


PP5V_S0_DVIPOINT_D

DVI power DIODE on page 95 (D9500)



OMIT CRITICAL J9801 MINI-DVI RT-TH



MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN, 32P MINI-DVI RCTP, RA, MG3, LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN, 32P MINI-DVI RCTP, RA, BLACK, LF	J9801	CRITICAL	FANCY

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7374	A
SCALE	SHT	OF	79
NONE	69		

	8	7	6	5	4	3	2	1
D	Title: Basenet Report	5V55_SW - @mlb_noldo_lib.MLB_NOLDO	5V55_SW - @mlb_noldo_lib.MLB_NOLDO	59B4	=PP1V05_S0_NB -	19D1 19D7 64C6	=PP2V5_S0_NB_VCCSYN -	17D6 19B6 19D7 64B6
	Design: mlb_noldo	5V55_TG - @mlb_noldo_lib.MLB_NOLDO	5V55_TG - @mlb_noldo_lib.MLB_NOLDO	59C4	@mlb_noldo_lib.MLB_NOLDO		@mlb_noldo_lib.MLB_NOLDO	@mlb_noldo_lib.MLB_NOLDO
	Date: Mar 22 15:44:50 2007	5V55_VOSNS - @mlb_noldo_lib.MLB_NOLDO	5V55_VOSNS - @mlb_noldo_lib.MLB_NOLDO	59B4	=PP1V05_S0_CPU_NB -	62A6 64D8	=PP2V5_S0_NB_VCCA_LVDS -	17C6 19C7 19D1 64B6
	Base nets and synonyms for mlb_noldo_lib.MLB_NOLDO(@mlb_noldo_lib.mlb_noldo(sch_1))	5V_REG_IN - @mlb_noldo_lib.MLB_NOLDO	5V_REG_IN - @mlb_noldo_lib.MLB_NOLDO	54A5	@mlb_noldo_lib.MLB_NOLDO		@mlb_noldo_lib.MLB_NOLDO	@mlb_noldo_lib.MLB_NOLDO
	Base Signal Synonyms Location([Zone][dir])	=EXTBUSB_OC_L - @mlb_noldo_lib.MLB_NOLDO	=EXTBUSB_OC_L - @mlb_noldo_lib.MLB_NOLDO	6C2 42C8	@mlb_noldo_lib.MLB_NOLDO		@mlb_noldo_lib.MLB_NOLDO	@mlb_noldo_lib.MLB_NOLDO
	LV2_FB - @mlb_noldo_lib.MLB_NOLDO	60A3	60A3		@mlb_noldo_lib.MLB_NOLDO		@mlb_noldo_lib.MLB_NOLDO	@mlb_noldo_lib.MLB_NOLDO
	LV05S0_BG - @mlb_noldo_lib.MLB_NOLDO	62B4	62B4		USB_C_OC_L - @mlb_noldo_lib.MLB_NOLDO	62A8 64D6	=PP3V3_S0_FAN_RT - @mlb_noldo_lib.MLB_NOLDO	17D6 19B7 19D7 64B6
	LV05S0_BOOST - @mlb_noldo_lib.MLB_NOLDO	62B4	62B4		EXTBUSB_OC_L - @mlb_noldo_lib.MLB_NOLDO		62B4 64B6	19D6 64B6
	LV05S0_BOOST_RC - @mlb_noldo_lib.MLB_NOLDO	62C3	62C3		=PP1V05_S0_SB_CPU_IO - @mlb_noldo_lib.MLB_NOLDO	21C1 21C1 24C3 25C4 64D6	=PP3V3_S0_ENET - @mlb_noldo_lib.MLB_NOLDO	36C8 64A6
	LV05S0_BOOST_RC - @mlb_noldo_lib.MLB_NOLDO	62C3	62C3		=PPVCORE_S0_SB - @mlb_noldo_lib.MLB_NOLDO	24D3 25D3 64D6	=PP3V3_S0_FW - @mlb_noldo_lib.MLB_NOLDO	39C6 64A6
C	LV05S0_COMP - @mlb_noldo_lib.MLB_NOLDO	5D7	5D7		PP1V05_S0 - @mlb_noldo_lib.MLB_NOLDO	5B2 64D7	=PP3V3_S0_2V5S0 - @mlb_noldo_lib.MLB_NOLDO	60C4 64A6
	LV05S0_FSET - @mlb_noldo_lib.MLB_NOLDO	5D7	5D7		=PPVCORE_S0_SB - @mlb_noldo_lib.MLB_NOLDO	24D3 25D3 64D6	=PP3V3_S0_1V51V05S0 - @mlb_noldo_lib.MLB_NOLDO	62B1 64A6
	LV05S0_ITH - @mlb_noldo_lib.MLB_NOLDO	62B4	62B4		PP1V05_S0_CPU_NB_SENSE - @mlb_noldo_lib.MLB_NOLDO	21C1 21C1 24C3 25C4 64D6	=PP3V3_S0_SMBUS_SMC_BSB - @mlb_noldo_lib.MLB_NOLDO	27B1 64A6
	LV05S0_ITH_RC - @mlb_noldo_lib.MLB_NOLDO	62B3	62B3		PP1V05_S0_CPU_NB_SENSE - @mlb_noldo_lib.MLB_NOLDO	62A8 64D6	=PP3V3_S0_RSTBUF - @mlb_noldo_lib.MLB_NOLDO	26B4 64A6
	LV05S0_ITH_RC - @mlb_noldo_lib.MLB_NOLDO	62B3	62B3		PP1V05_S0_NB - @mlb_noldo_lib.MLB_NOLDO	19C1 19D7 64C6	=PP3V3_S0_SMBUS_SB - @mlb_noldo_lib.MLB_NOLDO	27D8 64A6
	LV05S0_RUNSS - @mlb_noldo_lib.MLB_NOLDO	62B4 63B7	62B4 63B7		@mlb_noldo_lib.MLB_NOLDO	13D2 19D7 64C6	=PP3V3_S0_SMBUS_SMC_0 - @mlb_noldo_lib.MLB_NOLDO	27D5 64A6
	LV05S0_SNS_N - @mlb_noldo_lib.MLB_NOLDO	62C3	62C3		PP1V5_S0_AIRPORT - @mlb_noldo_lib.MLB_NOLDO	43D3 64C6	=PP3V3_S0_SMBUS_SMC_MLB - @mlb_noldo_lib.MLB_NOLDO	27C5 64A6
	LV05S0_SNS_P - @mlb_noldo_lib.MLB_NOLDO	62C3	62C3		@mlb_noldo_lib.MLB_NOLDO		=PP3V3_S0_SMBUS_SMC_MLB - @mlb_noldo_lib.MLB_NOLDO	27C5 64A6
	LV05S0_SW - @mlb_noldo_lib.MLB_NOLDO	62B4	62B4		PP1V5_S0_SB_VCCSATAPLL - @mlb_noldo_lib.MLB_NOLDO	24B5 25D6 64C6	=PP3V3_S0_ALL5VSPG - @mlb_noldo_lib.MLB_NOLDO	63B1 64A6
	LV05S0_TG - @mlb_noldo_lib.MLB_NOLDO	62C4	62C4		PP1V5_S0_SB_VCC1_5_A_ATX - @mlb_noldo_lib.MLB_NOLDO	24A5 25C6 64C6	=PP3V3_S0_LCD - @mlb_noldo_lib.MLB_NOLDO	64A6 67B5 67B5 67B7 67C6
B	LV05S0_VOSNS - @mlb_noldo_lib.MLB_NOLDO	62B4	62B4		PP1V5_S0_SB_VCCUSBPLL - @mlb_noldo_lib.MLB_NOLDO	24A5 25B6 64C6	=PP3V3_S0_PBAATTISENS - @mlb_noldo_lib.MLB_NOLDO	64A6 66B3
	LV550_BG - @mlb_noldo_lib.MLB_NOLDO	62B5	62B5		@mlb_noldo_lib.MLB_NOLDO		=PP3V3_S0_PDCISENS - @mlb_noldo_lib.MLB_NOLDO	62A5 64A6 66C4
	LV550_BOOST - @mlb_noldo_lib.MLB_NOLDO	62B5	62B5		PP1V5_S0_SB_VCC1_5_A_USB_CORE - @mlb_noldo_lib.MLB_NOLDO	24A3 25B2 64C6	=PP3V3_S0_SMBUS_SMC_MLB - @mlb_noldo_lib.MLB_NOLDO	48C2 64A6
	LV550_BOOST_RC - @mlb_noldo_lib.MLB_NOLDO	62C6	62C6		PP1V5_S0_SB_VCC1_5_A - @mlb_noldo_lib.MLB_NOLDO	24A3 25C2 64C6	=PP3V3_S0_CPUPOWER - @mlb_noldo_lib.MLB_NOLDO	22B5 25D8 34C8 64B6
	LV550_ITH - @mlb_noldo_lib.MLB_NOLDO	62B5	62B5		PP1V5_S0_SB - @mlb_noldo_lib.MLB_NOLDO	25A8 25C8 64C6	=PP3V3_S0_SB - @mlb_noldo_lib.MLB_NOLDO	21C3 21D3 23B2 23D5 64B6
	LV550_ITH_RC - @mlb_noldo_lib.MLB_NOLDO	62B5	62B5		@mlb_noldo_lib.MLB_NOLDO		@mlb_noldo_lib.MLB_NOLDO	@mlb_noldo_lib.MLB_NOLDO
	LV550_RUNSS - @mlb_noldo_lib.MLB_NOLDO	5D7 62B5 63B7	5D7 62B5 63B7		PP1V5_S0_NB_VCCCAUX - @mlb_noldo_lib.MLB_NOLDO	16D1 17B6 19B6 19D7 64C6	=PP3V3_S0_SB_GPIO - @mlb_noldo_lib.MLB_NOLDO	24B5 24B5 25B8 25C6 64B6
	LV550_SNS_N - @mlb_noldo_lib.MLB_NOLDO	62C6	62C6		PP1V5_S0_NB_VCCD_HMPLL - @mlb_noldo_lib.MLB_NOLDO	17C6 19D7 64C6	=PP3V3_S0_SB_VCC3_3 - @mlb_noldo_lib.MLB_NOLDO	24B3 25A4 64B6
	LV550_SNS_P - @mlb_noldo_lib.MLB_NOLDO	62C6	62C6		PP1V5_S0_NB_VCCD_LVDS - @mlb_noldo_lib.MLB_NOLDO	17C6 19B8 19D7 64C6	=PP3V3_S0_SB_VCC3_3_PCIE - @mlb_noldo_lib.MLB_NOLDO	24C3 25B4 64B6
	LV550_SW - @mlb_noldo_lib.MLB_NOLDO	62B5	62B5		PP1V5_S0_NB_PLL - @mlb_noldo_lib.MLB_NOLDO	19C6 19D7 64C6	=PP3V3_S0_SB_VCC3_3_TDE - @mlb_noldo_lib.MLB_NOLDO	26D1 64B6
A	LV550_TG - @mlb_noldo_lib.MLB_NOLDO	62C5	62C5		PP1V5_S0_NB_TVDCAC - @mlb_noldo_lib.MLB_NOLDO	19A8 19D7 64C6	=PP3V3_S0_SB_PCI - @mlb_noldo_lib.MLB_NOLDO	26M6 26B8 64B6
	LV550_VOSNS - @mlb_noldo_lib.MLB_NOLDO	62B5	62B5		PP1V5_S0_NB_3G - @mlb_noldo_lib.MLB_NOLDO	19B5 64C6	=PP3V3_S0_SB_PM - @mlb_noldo_lib.MLB_NOLDO	34C2 64A6
	LV8S3_BOOT - @mlb_noldo_lib.MLB_NOLDO	61B5	61B5		PP1V5_S0_NB_3GPLL - @mlb_noldo_lib.MLB_NOLDO	19A5 64C6	=PP3V3_S0_PATA - @mlb_noldo_lib.MLB_NOLDO	46D3 64A6
	LV8S3_BOOT_RC - @mlb_noldo_lib.MLB_NOLDO	61C4	61C4		PP1V5_S0_SB_VCC1_5_A_ARX - @mlb_noldo_lib.MLB_NOLDO	24B5 25D6 64C6	=PP3V3_S0_SMC_LS - @mlb_noldo_lib.MLB_NOLDO	14C7 14D6 19C7 20A4 20B4
	LV8S3_COMP - @mlb_noldo_lib.MLB_NOLDO	5D7 61B6	5D7 61B6		PP1V5_S0_NB - @mlb_noldo_lib.MLB_NOLDO	8B7 9D8 64C6	@mlb_noldo_lib.MLB_NOLDO	20B4 64A6
	LV8S3_COMP_R - @mlb_noldo_lib.MLB_NOLDO	61B6	61B6		PP1V5_S0_REG - @mlb_noldo_lib.MLB_NOLDO	62B8 64C8	=PP3V3_S0_SB_VCCLAN3_3 - @mlb_noldo_lib.MLB_NOLDO	24D3 25D3 64A6
	LV8S3_FB - @mlb_noldo_lib.MLB_NOLDO	61B6	61B6		PP1V5_S0 - @mlb_noldo_lib.MLB_NOLDO	5B2 64C7	=PP3V3_S0_SB_3V3_1V5_VCCCHA - @mlb_noldo_lib.MLB_NOLDO	24C3 25C4 64A6
	LV8S3_FCCM - @mlb_noldo_lib.MLB_NOLDO	61B6	61B6		PP1V5_S0_SB_VCCUSBPLL - @mlb_noldo_lib.MLB_NOLDO	24A5 25B6 64C6	@mlb_noldo_lib.MLB_NOLDO	28A7 29A3 29A7 64A6
	LV8S3_FSET - @mlb_noldo_lib.MLB_NOLDO	5D7 61C6	5D7 61C6		@mlb_noldo_lib.MLB_NOLDO		=PPSPD_S0_MEM - @mlb_noldo_lib.MLB_NOLDO	32C7 32D3 32D8 64A6
	LV8S3_ISET - @mlb_noldo_lib.MLB_NOLDO	61B5	61B5		PP1V5_S0_CPU - @mlb_noldo_lib.MLB_NOLDO	24A3 25B2 64C6	=PP3V3_S0_CK410 - @mlb_noldo_lib.MLB_NOLDO	43C3 64A6
LV8S3_LG - @mlb_noldo_lib.MLB_NOLDO	61B5	61B5		PP1V5_S0_CPU - @mlb_noldo_lib.MLB_NOLDO	24A5 25C6 64C6	=PP3V3_S0_AIRPORT - @mlb_noldo_lib.MLB_NOLDO	53D4 64A6	

	8	7	6	5	4	3	2	1
D		-USB2_EXTA_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 42C5					
		USB2_EXTA_N - @mlb_nolddo.lib.MLB_NOLDO	6C2					
	USB_A_OC_L	=USB2_EXTA_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 42C5					
		USB_A_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C4 22D8					
		=EXTAUSB_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C2 42C8					
		EXTAUSB_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		=EXTAUSB_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C2 42C8					
	USB_A_P	USB_A_P - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
		=USB2_EXTA_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 42C5					
		USB2_EXTA_P - @mlb_nolddo.lib.MLB_NOLDO	6C2					
C		=USB2_EXTA_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 42C5					
	USB_B_N	USB_B_N - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
		=USB2_GEYSER_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 40C7					
		USB2_GEYSER_N - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		=USB2_GEYSER_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 40C7					
	USB_B_OC_L	@mlb_nolddo.lib.MLB_NOLDO	22C4 22D8					
		USB_B_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
	USB_B_P	USB_B_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 40C7					
		=USB2_GEYSER_P - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		USB2_GEYSER_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 40C7					
B		@mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
	USB_C_N	USB_C_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 42B5					
		=USB2_EXTB_N - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		USB2_EXTB_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 42B5					
		=USB2_EXTB_N - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
	USB_C_P	USB_C_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 42B5					
		=USB2_EXTB_P - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		USB2_EXTB_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 42B5					
		=USB2_EXTB_P - @mlb_nolddo.lib.MLB_NOLDO	22C4 22D8					
	USB_D_OC_L	USB_D_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
A		TP_USBN_E - @mlb_nolddo.lib.MLB_NOLDO	5C1 6C2					
	USB_E_N	USB_E_N - @mlb_nolddo.lib.MLB_NOLDO	22C4 22D8					
		USB_E_OC_L - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
	USB_E_P	USB_E_P - @mlb_nolddo.lib.MLB_NOLDO	5C1 6C2					
		TP_USBP_E - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
	USB_F_N	USB_F_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 41C6					
		=USB2_IR_N - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		USB_IR_N - @mlb_nolddo.lib.MLB_NOLDO	6C2 41C6					
		=USB2_IR_N - @mlb_nolddo.lib.MLB_NOLDO	6C1 22C2					
	USB_F_P	USB_F_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 41C6					
B		@mlb_nolddo.lib.MLB_NOLDO	6C2					
		=USB2_IR_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 41C6					
		USB_IR_P - @mlb_nolddo.lib.MLB_NOLDO	6C2					
		=USB2_IR_P - @mlb_nolddo.lib.MLB_NOLDO	6B1 22C2					
	USB_G_N	USB_G_N - @mlb_nolddo.lib.MLB_NOLDO	6B2 44C6					
		=USB2_BT_N - @mlb_nolddo.lib.MLB_NOLDO	6B2					
		USB_BT_N - @mlb_nolddo.lib.MLB_NOLDO	6B2 44C6					
		=USB2_BT_N - @mlb_nolddo.lib.MLB_NOLDO	6B1 22C2					
	USB_G_P	USB_G_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 44C6					
		=USB2_BT_P - @mlb_nolddo.lib.MLB_NOLDO	6C2 44C6					
A		USB_BT_P - @mlb_nolddo.lib.MLB_NOLDO	6C2					
	USB_RBIAS_PN	@mlb_nolddo.lib.MLB_NOLDO	22C2					
		USB_RBIAS_PN - @mlb_nolddo.lib.MLB_NOLDO	69B4					
	VGA_B	VGA_B - @mlb_nolddo.lib.MLB_NOLDO	69B4					
	VGA_G	VGA_G - @mlb_nolddo.lib.MLB_NOLDO	69B4 69C1					
	VGA_HSYNC	VGA_HSYNC - @mlb_nolddo.lib.MLB_NOLDO	69A4					
	VGA_R	VGA_R - @mlb_nolddo.lib.MLB_NOLDO	69B4 69C1					
	VGA_VSYNC	VGA_VSYNC - @mlb_nolddo.lib.MLB_NOLDO	54B7 54C7					
	VOL_DOWN	VOL_DOWN - @mlb_nolddo.lib.MLB_NOLDO	54B7 54C7					
	VOL_UP	VOL_UP - @mlb_nolddo.lib.MLB_NOLDO	54A4					
A		VREG_FB - @mlb_nolddo.lib.MLB_NOLDO	23C5 26A8					
	VR_PWRGD_CK410	VR_PWRGD_CK410 - @mlb_nolddo.lib.MLB_NOLDO	14B6 26B5 58C7					
	VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B2					
	XDP_BPM_L<0>	XDP_BPM_L<0> - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B2					
	XDP_BPM_L<1>	XDP_BPM_L<1> - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B2					
	XDP_BPM_L<2>	XDP_BPM_L<2> - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B2					
	XDP_BPM_L<3>	XDP_BPM_L<3> - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B3					
	XDP_BPM_L<4>	XDP_BPM_L<4> - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B2					
	XDP_BPM_L<5>	XDP_BPM_L<5> - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B2					
	XDP_DBRESET_L	XDP_DBRESET_L - @mlb_nolddo.lib.MLB_NOLDO	7A8 7C6 11B2 11B3					
XDP_TCK	XDP_TCK - @mlb_nolddo.lib.MLB_NOLDO	7B8 7C6 11B3						
XDP_TDI	XDP_TDI - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B5						
XDP_TDO	XDP_TDO - @mlb_nolddo.lib.MLB_NOLDO	7B8 7C6 11B2						
XDP_TMS	XDP_TMS - @mlb_nolddo.lib.MLB_NOLDO	7C6 11B3						
XDP_TRST_L	XDP_TRST_L - @mlb_nolddo.lib.MLB_NOLDO							



