

M60 - PVT

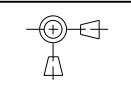
08/01/06

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
			DATE	DATE	DATE
D		452633	PRODUCTION RELEASED	08/01/06	06/22/04

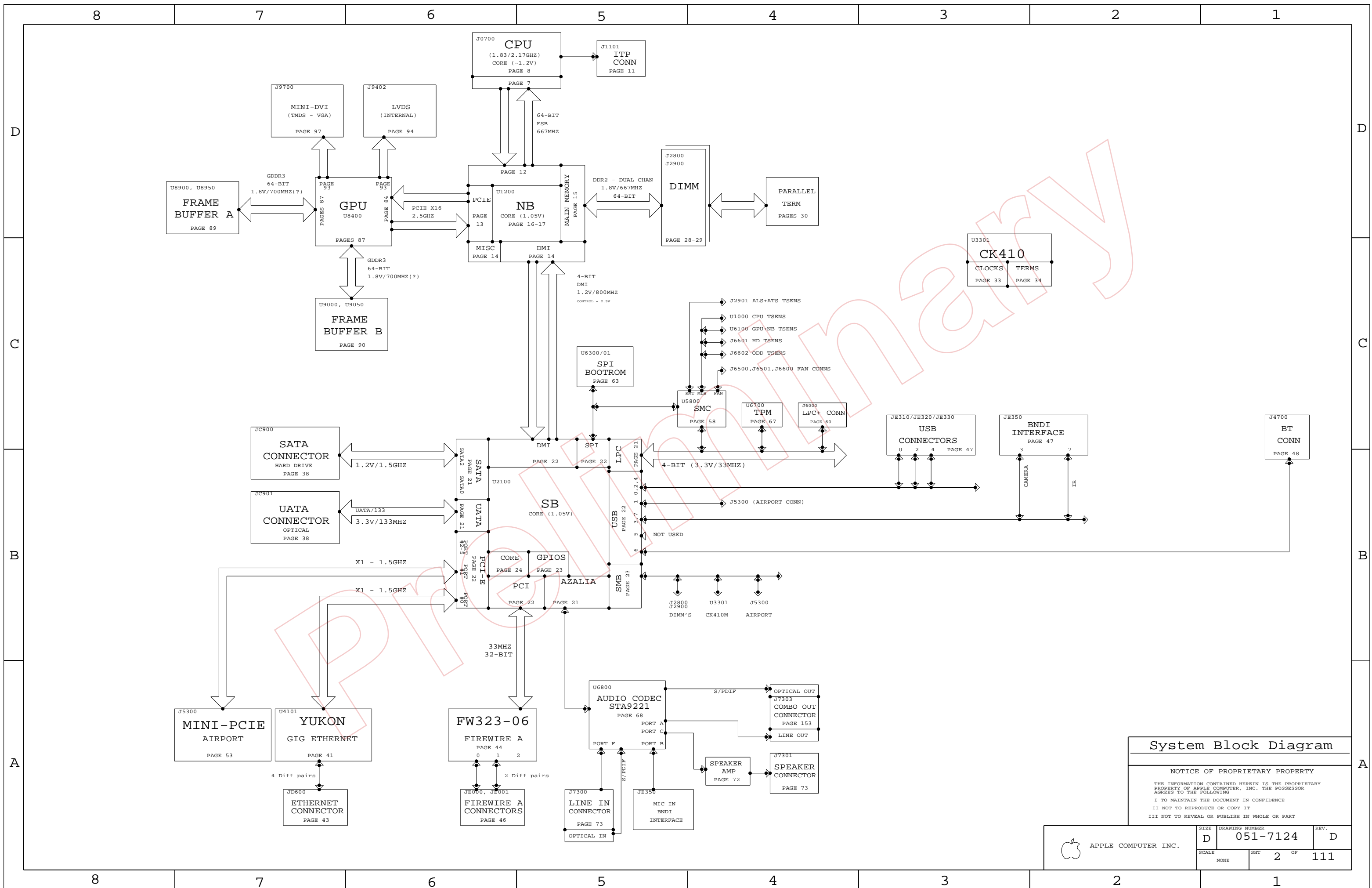
PAGE	PDF	CIRCUIT	
1	JD	1	TABLE OF CONTENTS
2	JD	2	SYSTEM BLOCK DIAGRAM
3	MY	3	POWER BLOCK DIAGRAM
4	JD	4	TABLE ITEMS & REVISION HISTORY
5	JD	5	FUNC TEST
6	MY	6	POWER CONNECTOR / POWER ALIAS
7	JD	7	CPU - BUS INTERFACE
8	JD	8	CPU - PWR & GND
9	JD	9	CPU - DECAPS
10	JD	10	CPU - THERMAL SENSOR
11	JD	11	CPU - ITP CONN
12	JH	12	NB - CPU INTERFACE
13	JH	13	NB - VIDEO INTERFACE
14	JH	14	NB - MISC INTERFACES
15	JH	15	NB - DDR2 INTERFACE
16	JH	16	NB - POWER 1
17	JH	17	NB - POWER 2
18	JH	18	NB - GROUNDS
19	JH	19	NB - DECAPS
20	JH	20	NB - CONFIG STRAPS
21	JD	21	SB - RTC, LAN, AUDIO, ATA, CPU, LPC
22	JD	22	SB - PCIE, SPI, USB, DMI, PCI
23	JD	23	SB - SMB, GPIO, PM, CLKS
24	JD	24	SB - POWERS AND GROUNDS
25	JD	25	SB - DECAPS
26	JD	26	SB - MISC
27	JD	27	SB - SMB BUS CONNECTIONS
28	JD	28	DDR2 - SO-DIMM CONN A
29	JD	29	DDR2 - SO-DIMM CONN B (REVERSED)
30	JD	30	DDR2 - TERMINATION
31	MY	31	DDR2 - VTT SUPPLY
33	JD	32	CLOCKS - GENERATOR
34	JD	33	CLOCKS - TERMINATIONS
38	JD	34	ATA (SATA AND IDE) CONN'S
41	JD	35	LAN - YUKON'S PCIE INTERFACE
42	JD	36	LAN - YUKON'S PWR, MISC
43	JD	37	LAN - CONN
44	JD	38	FIREWIRE - FW323-06
45	JD	39	FIREWIRE - DECAPS
46	JD	40	FIREWIRE - CONN'S
47	JD	41	USB - CONN'S
53	JD	42	PCI-E - AIRPORT MINI-PCIE CONN
54	JD	43	PCI-E - UNUSED PORTS

PAGE	PDF	CIRCUIT	
57	MY	44	VR - "S5" 3.3V AND 2.5V
58	MY	45	SMC - H8S2116
59	MY	46	SMC - SMB BUSSES, MISC
60	MY	47	SMC - LPC+ CONN
61	MY	48	SMC - GPU/NB THERMAL SENSOR
63	MY	49	SMC - SPI BOOTROM
65	MY	50	SMC - FANS
66	MY	51	SMC - FANS
67	JD	52	SMC - TPM
TG		68	AUDIO - CODEC, VREG, MIC BIAS
TG		72	AUDIO - INTERNAL SPEAKER AMP
TG		73	AUDIO - I/O CONN'S, EMC
TG		74	AUDIO - DETECT TRANSLATORS
75	MY	57	VR - CPU CORE
76	MY	58	VR - CPU I-V SENSE CKT
77	MY	59	VR - "S3" 1.2V & "S0" 1.2V
78	MY	60	VR - "S0" 1.8V
79	MY	61	VR - "S3" 1.8V
80	MY	62	VR - "S0" 1.5V
81	MY	63	VR - "S0" 1.05V
82	MY	64	VR - "S5" 5V AND "S0" 4.5V
83	MY	65	VR - FETS FOR REMAINING RAILS
84	JH	66	GPU - M56 PCI-E
85	JH	67	GPU - VCORE SUPPLY
86	JH	68	GPU - M56 CORE PWR
87	JH	69	GPU - M56 FRAME BUFFER
88	JH	70	GPU - MISC
89	JH	71	GPU - GDDR SDRAM A
90	JH	72	GPU - GDDR SDRAM B
91	JH	73	GPU - M56 GPIO, DVO, MISC
92	JH	74	GPU - M56 CLOCKS
93	JH	75	GPU - M56 VIDEO INTERFACES
94	JH	76	GPU - INTERNAL DISPLAY CONN'S
95	JH	77	GPU - TP'S
96	JH	78	GPU - TMDS, INVERTER, EXT VGA
97	JH	79	GPU - EXTERNAL DISPLAY CONN'S

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7124	REV. D
				SHT 1 OF 111	

D
C
B
A

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A



System Block Diagram

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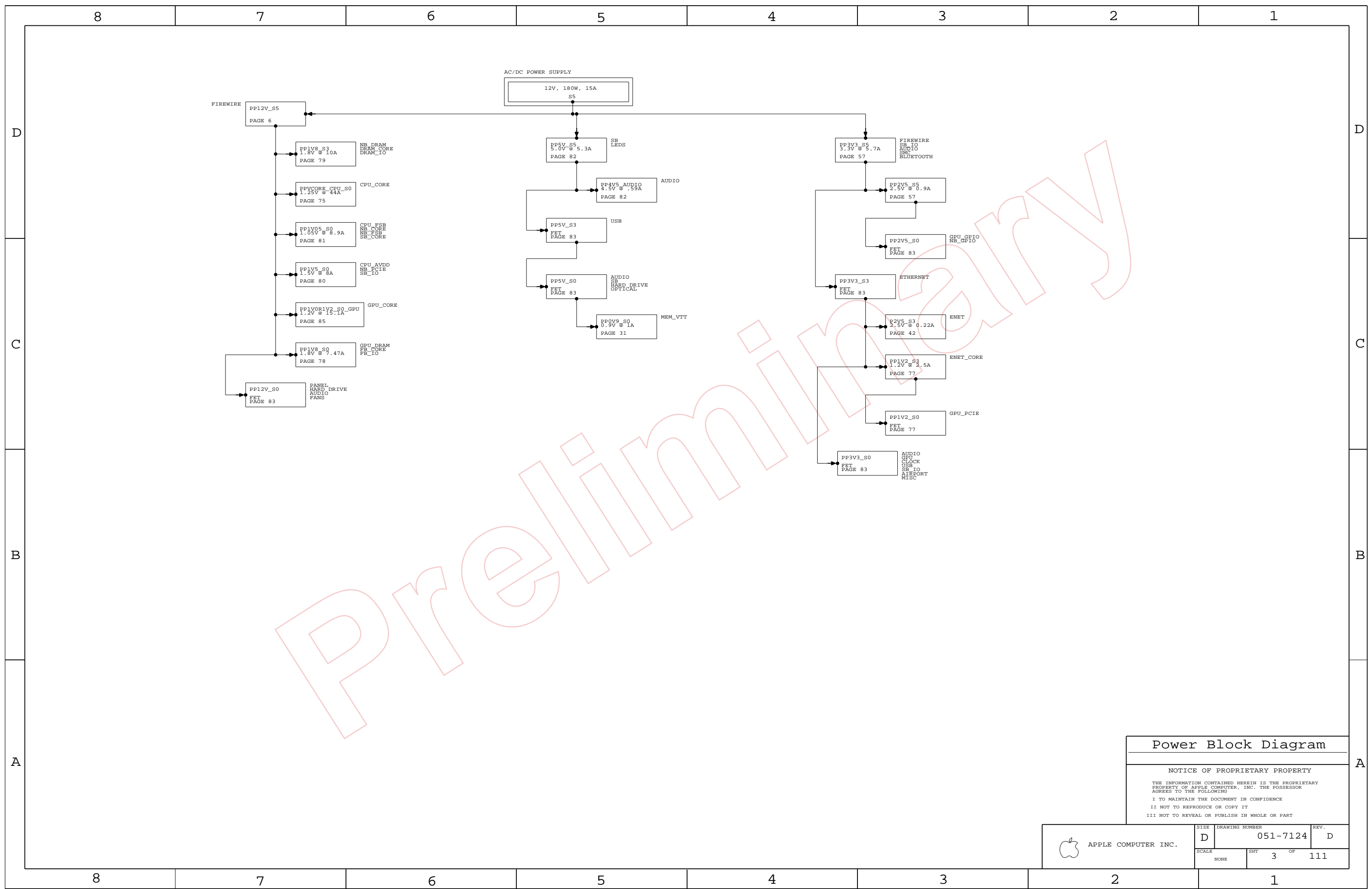
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	SCALE NONE	SHEET 2 OF 111	



Preliminary

Power Block Diagram

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SCALE	SHT	OF	REV.
NONE	3	111	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
338S0345	1	IC,ATI,M56D,GRAFIXCTLR,880BGA,LF	U8400	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382)	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1235	1	IC,CPU VREG,1MVP,TWO PHASE	U7500	CRITICAL	
152S0138	2	IND,PWR,SMD,3.3OH,20%,6A,30MHZ,LF,MD	L5703,L8203	CRITICAL	
128S0078	2	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518	CRITICAL	
825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
155S0289	7	EMI CHOKE	FLR011,FLR021,FL4610,FL4620,L4712,L4722,L4732	CRITICAL	

(341S1904 - DEV)
(341S1905 - PVT)
(335S0384 - BLNK)
(341S1903 - PROG)
(338S0274 - BLNK)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7124	1	PCB,SCHEM,MLB,M60	SCH1		20_INCH_LCD
820-2031	1	PCB,FAB,MLB,M60	MLB1		20_INCH_LCD
341T0036	1	EPI ROM,M60	U6301	CRITICAL	20_INCH_LCD
341T0035	1	IC,SMC,M60	U5800	CRITICAL	20_INCH_LCD
338S0315	1	IC,ATI,M56LP,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
114S0264	1	3.01K,1%,1/16W,402,MP-LF	R8522		GPU_VCORE_1P2V
337S3390	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU
337S3392	1	2.33GHZ MEROM	CPU	CRITICAL	2P33_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SDRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SDRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SDRAM,GDDR3,16MX32,600MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		C940,C1900,C1901,C1968	SANYO W6CE330FS 330UF 6.3V LF
128S0080	128S0078		C7517,C7518	SANYO 166VP330M 330UF 16V SMD LF
124-0338	124-0333			CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
124-0361	124-0339		C7807	SANYO
353S1321	353S1105		U7910	LM339
338S0344	338S0345		U8400	M56 B26 P - DIFF P/N
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504
378S0141	378S0140		LED01,LED02,LED03	LED
138S0598	138S0512			SAMSUNG

Preliminary

Table Items


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SCALE	SHT	OF	REV.
NONE	4	111	

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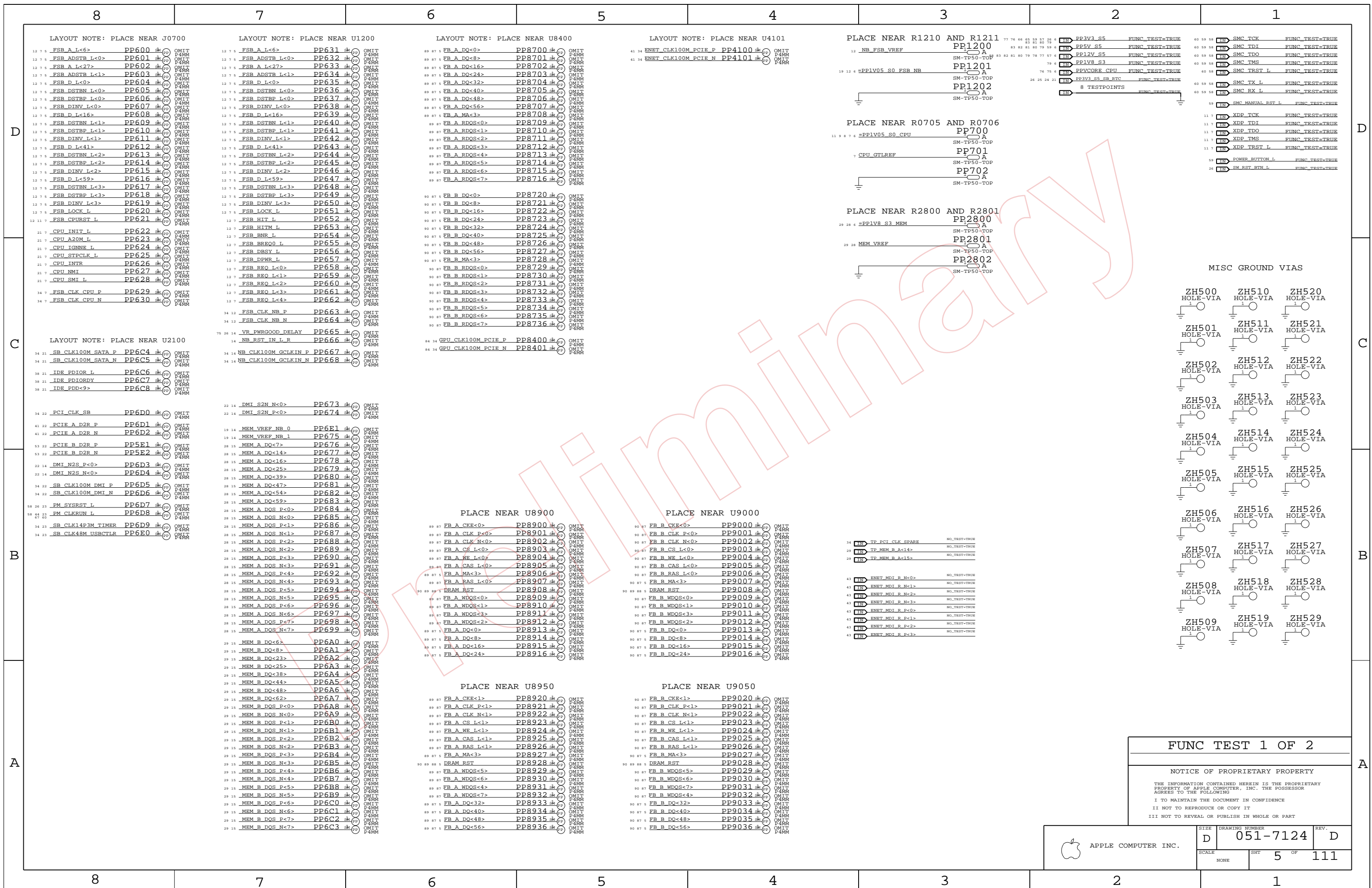
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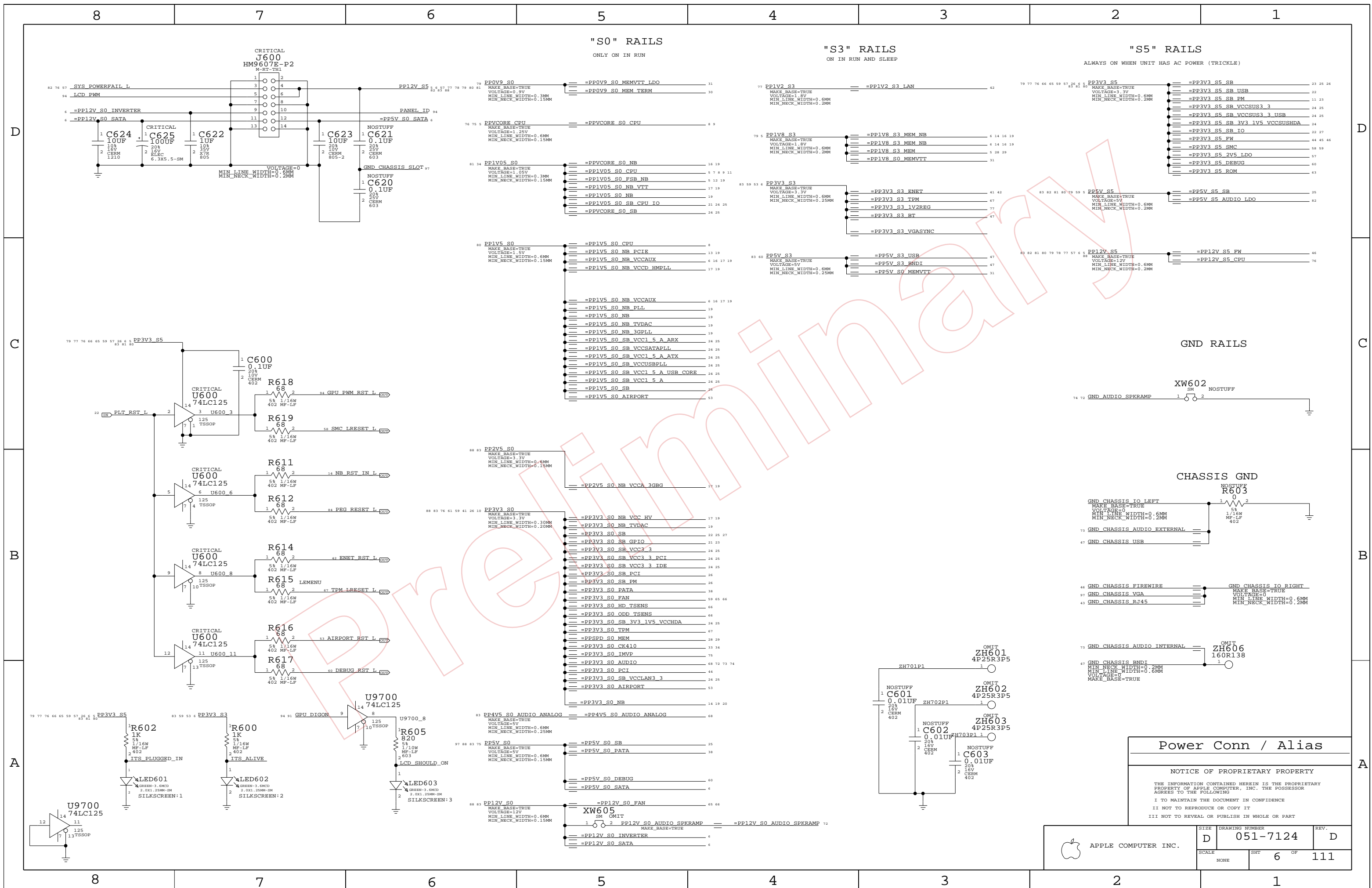


FUNC TEST 1 OF 2

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SCALE	SHEET	OF	
NONE	5	111	



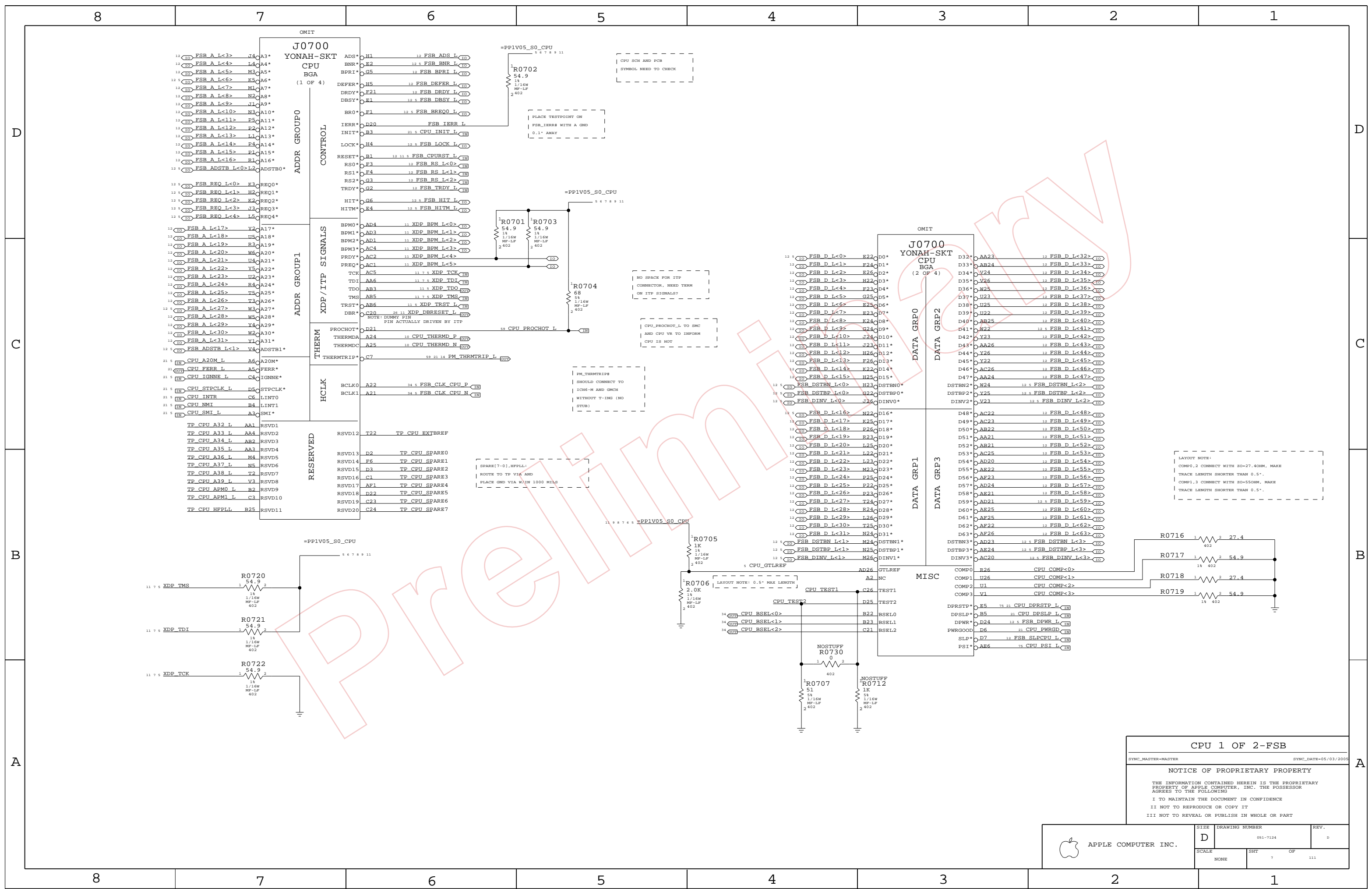
Power Conn / Alias

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	SCALE NONE	SHEET 6	OF 111



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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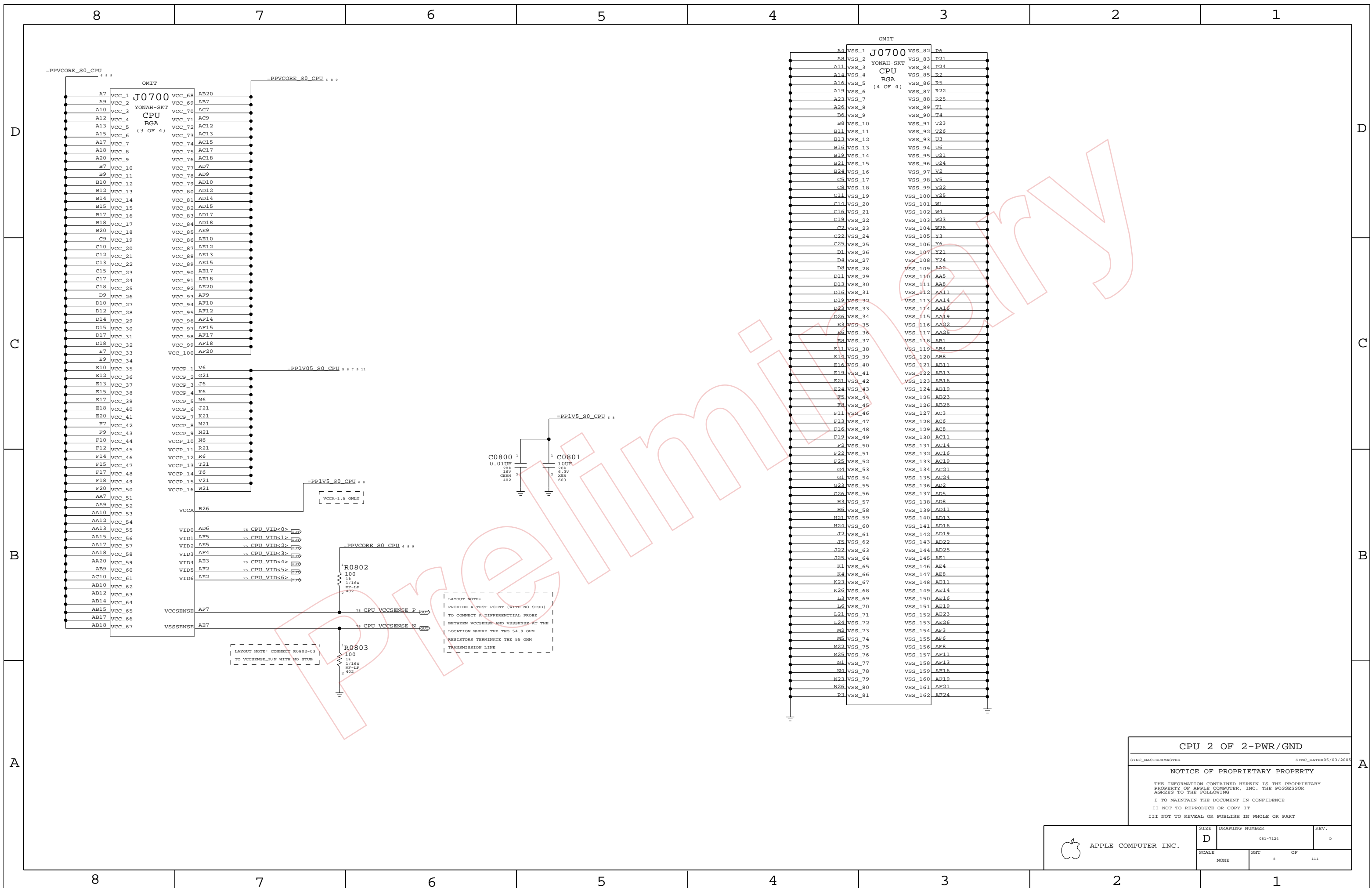
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET 7	OF 111



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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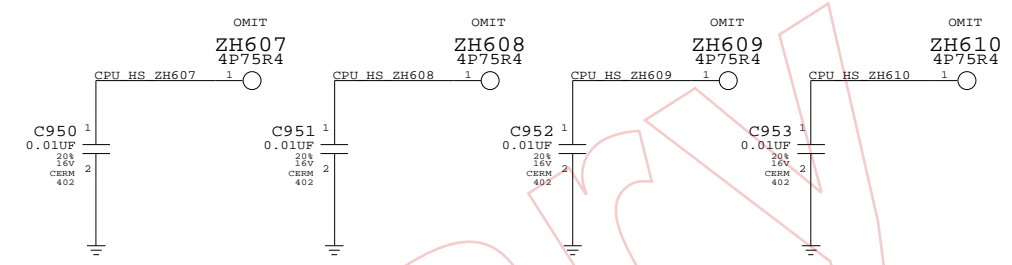
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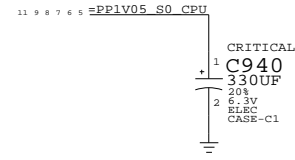
D

CPU HEATSINK MOUNTING HOLES

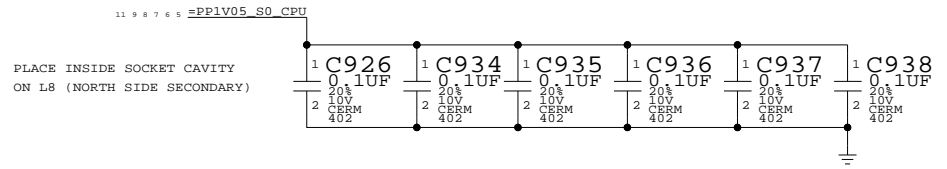


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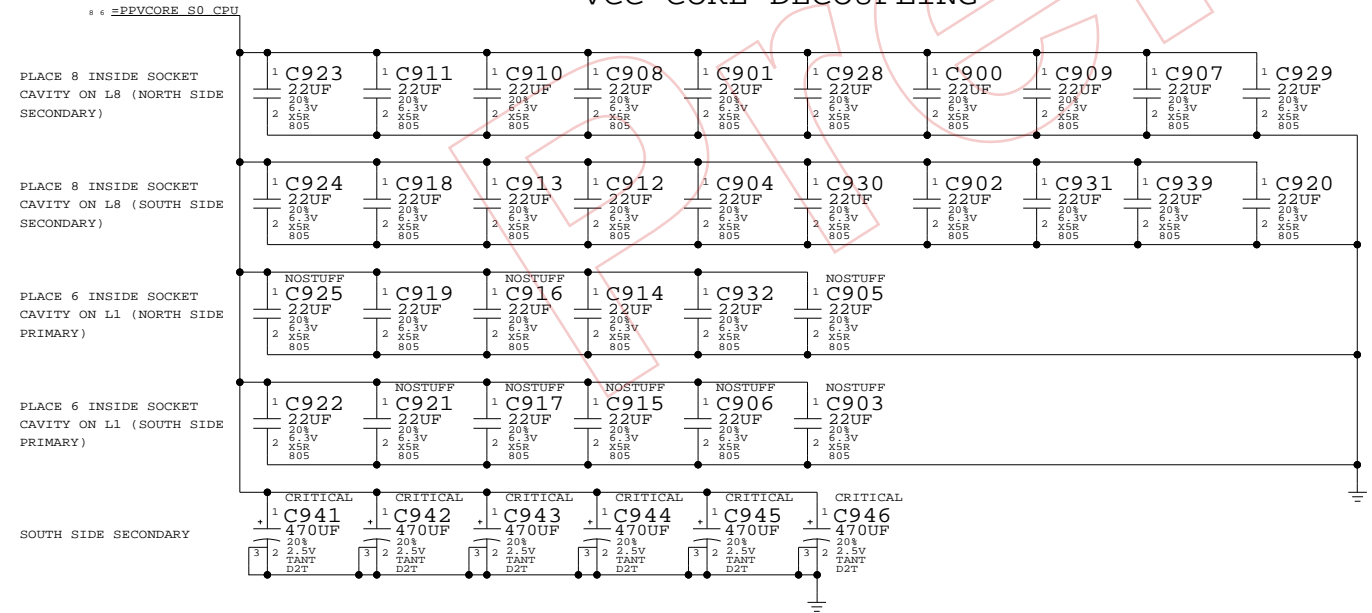
VCCP CORE DECOUPLING



B

B

VCC CORE DECOUPLING



A

A

CPU DECAPS & VID<>

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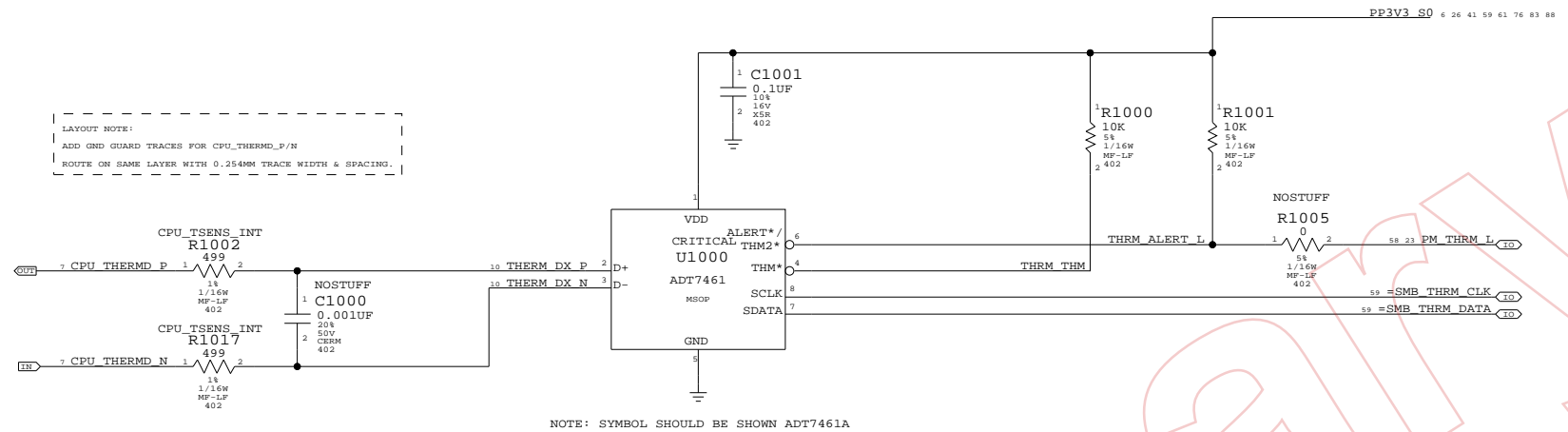
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NONE	9	111	

CPU THERMAL SENSOR

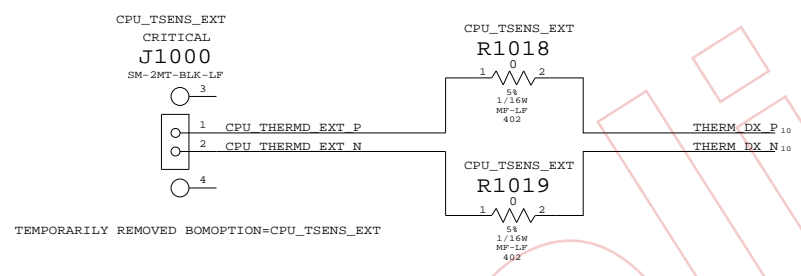
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

CPU TEMP SENSOR

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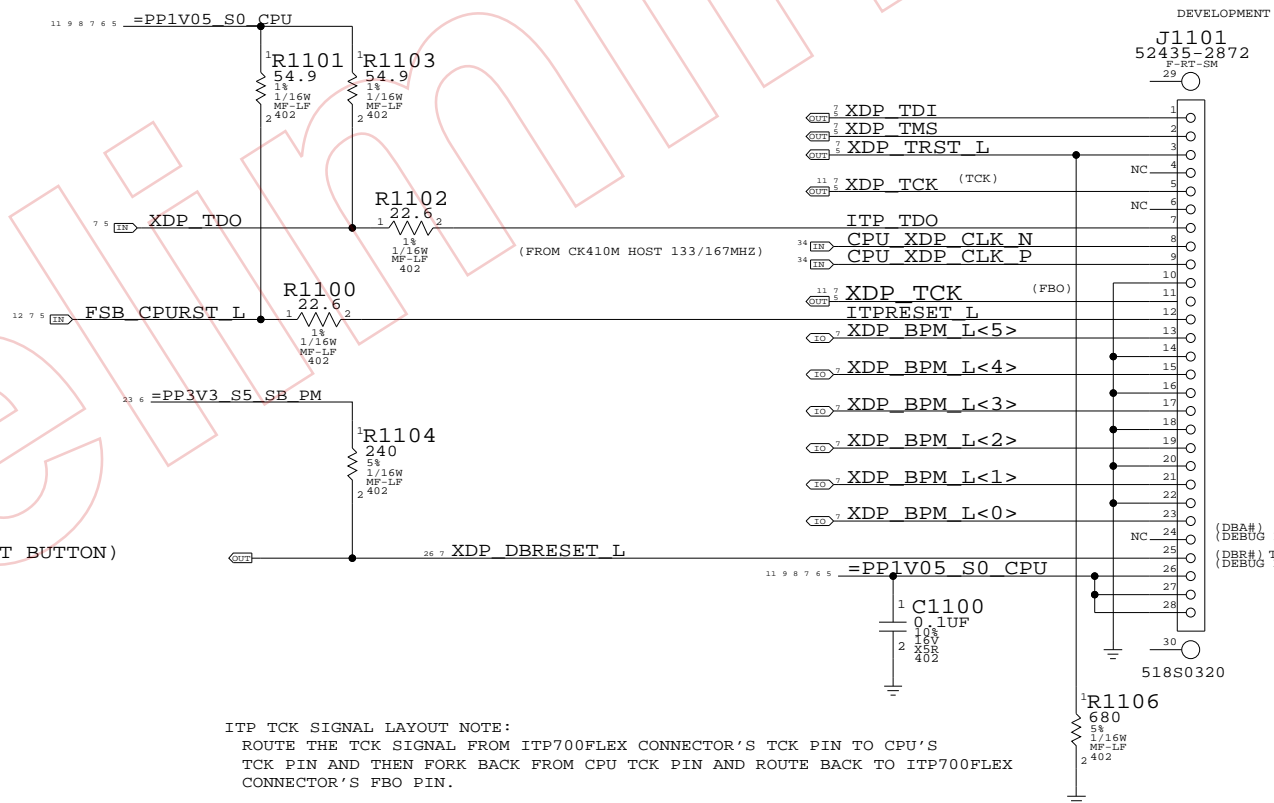
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SCALE	SHT	OF	REV.
NONE	10	111	

CPU ITP700FLEX DEBUG SUPPORT

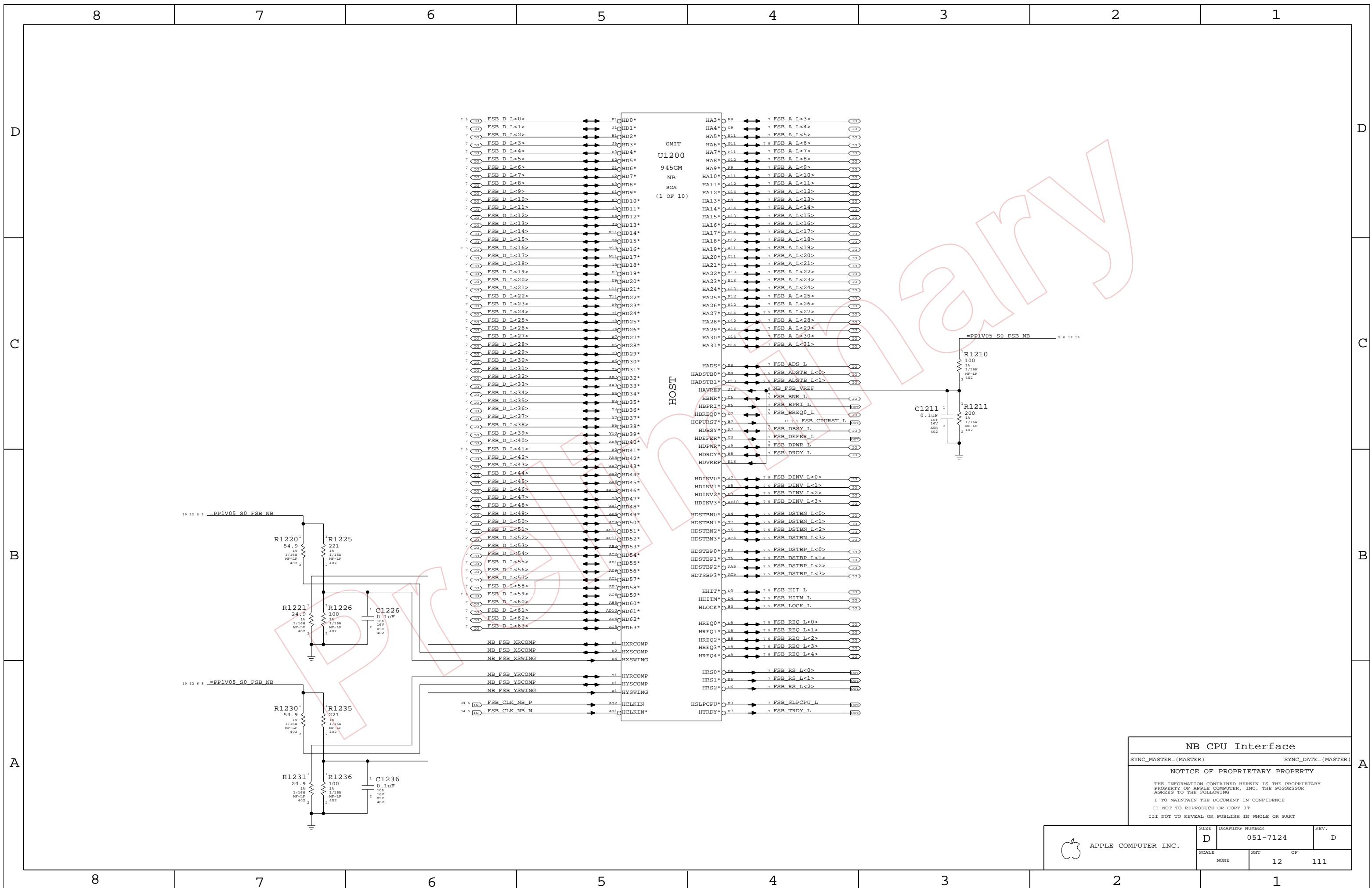


ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
 CONNECTOR'S FBO PIN.

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
 (DEBUG PORT ACTIVE)
 (DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
 (DEBUG PORT RESET)

CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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SCALE	SHT	OF	REV.
NONE	11	111	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
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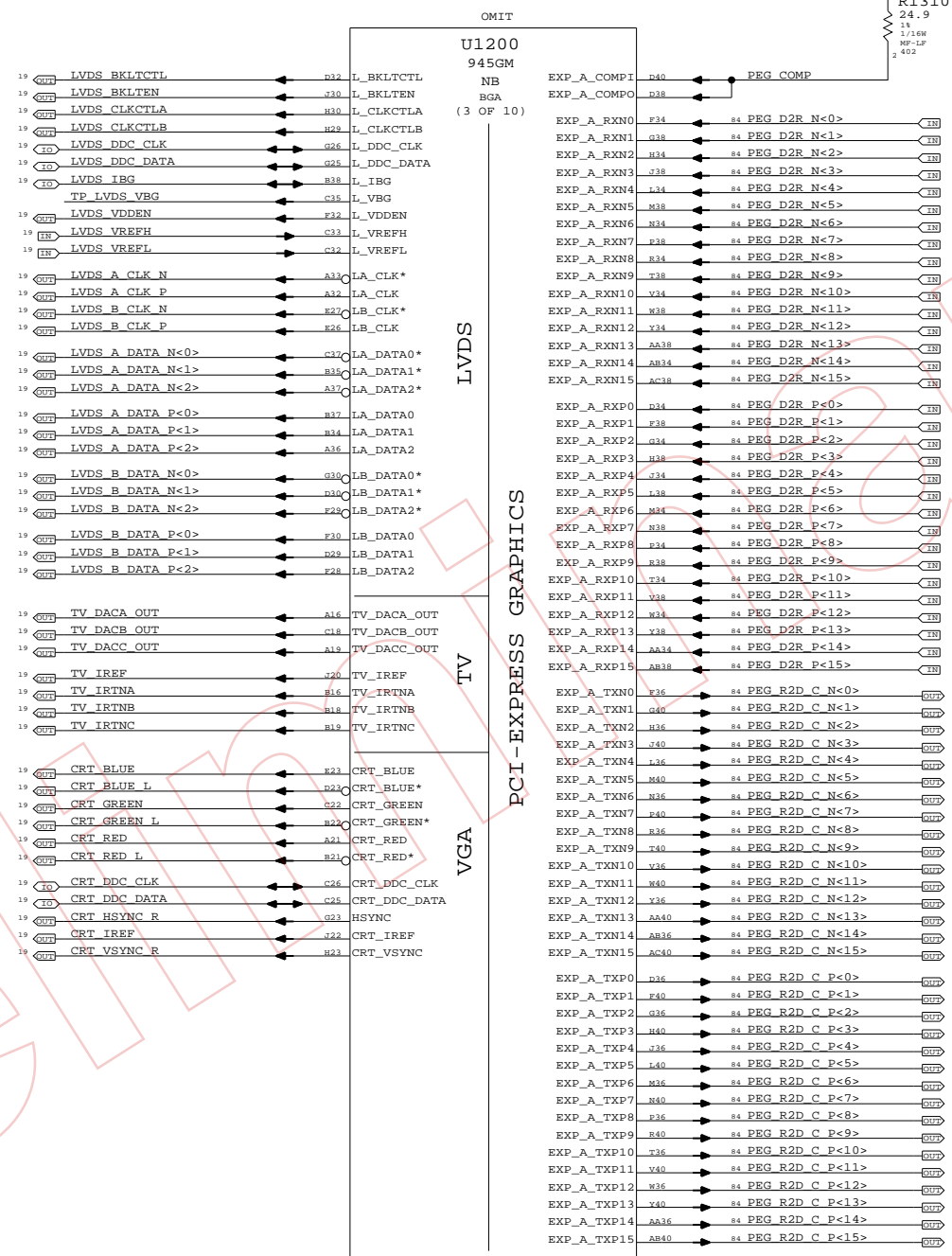
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

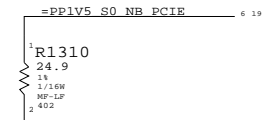


SDVO Alternate Function
 SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

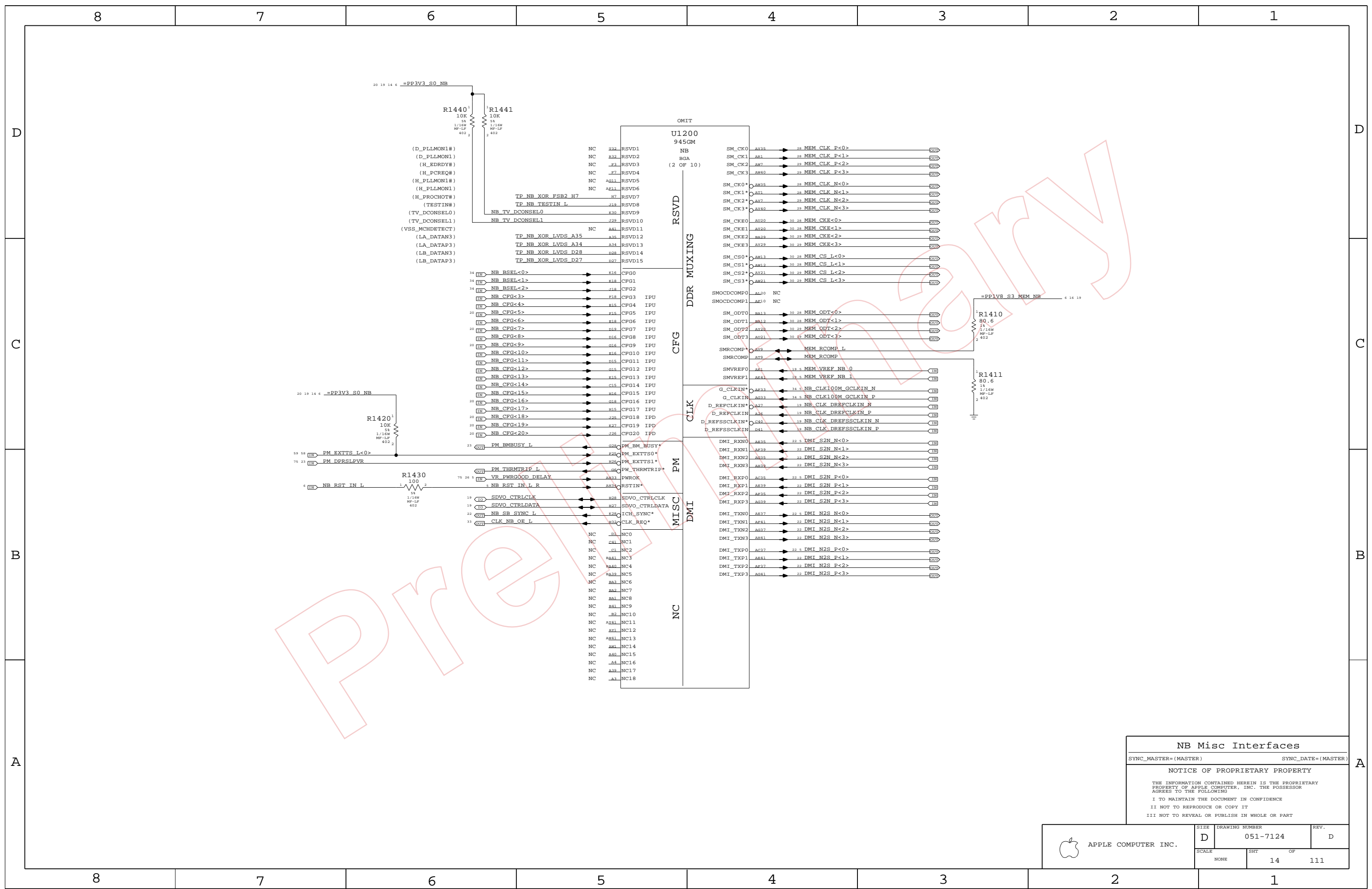
SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP



Pre

NB PEG / Video Interfaces
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	13	111	



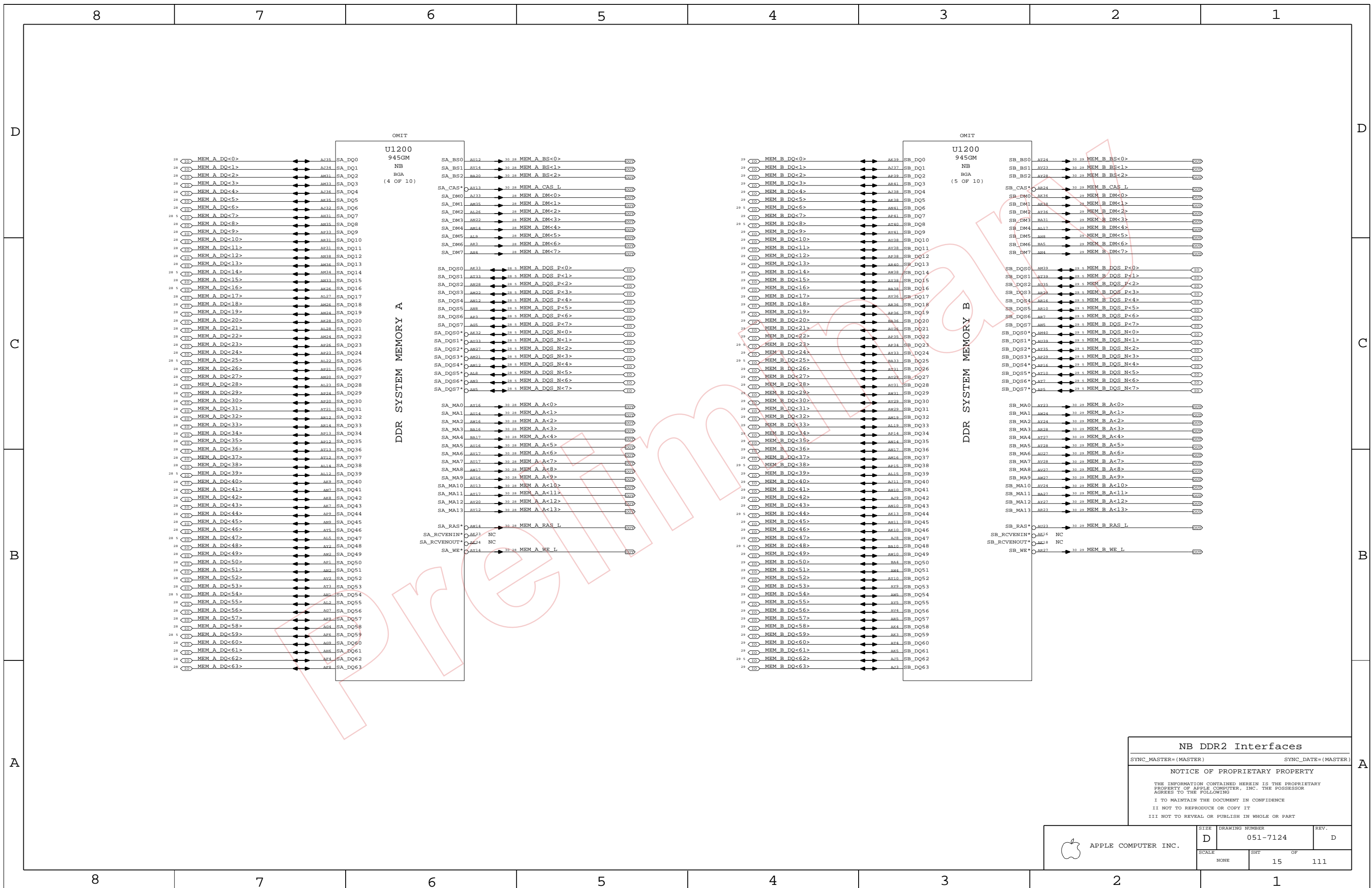
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	14	111	



NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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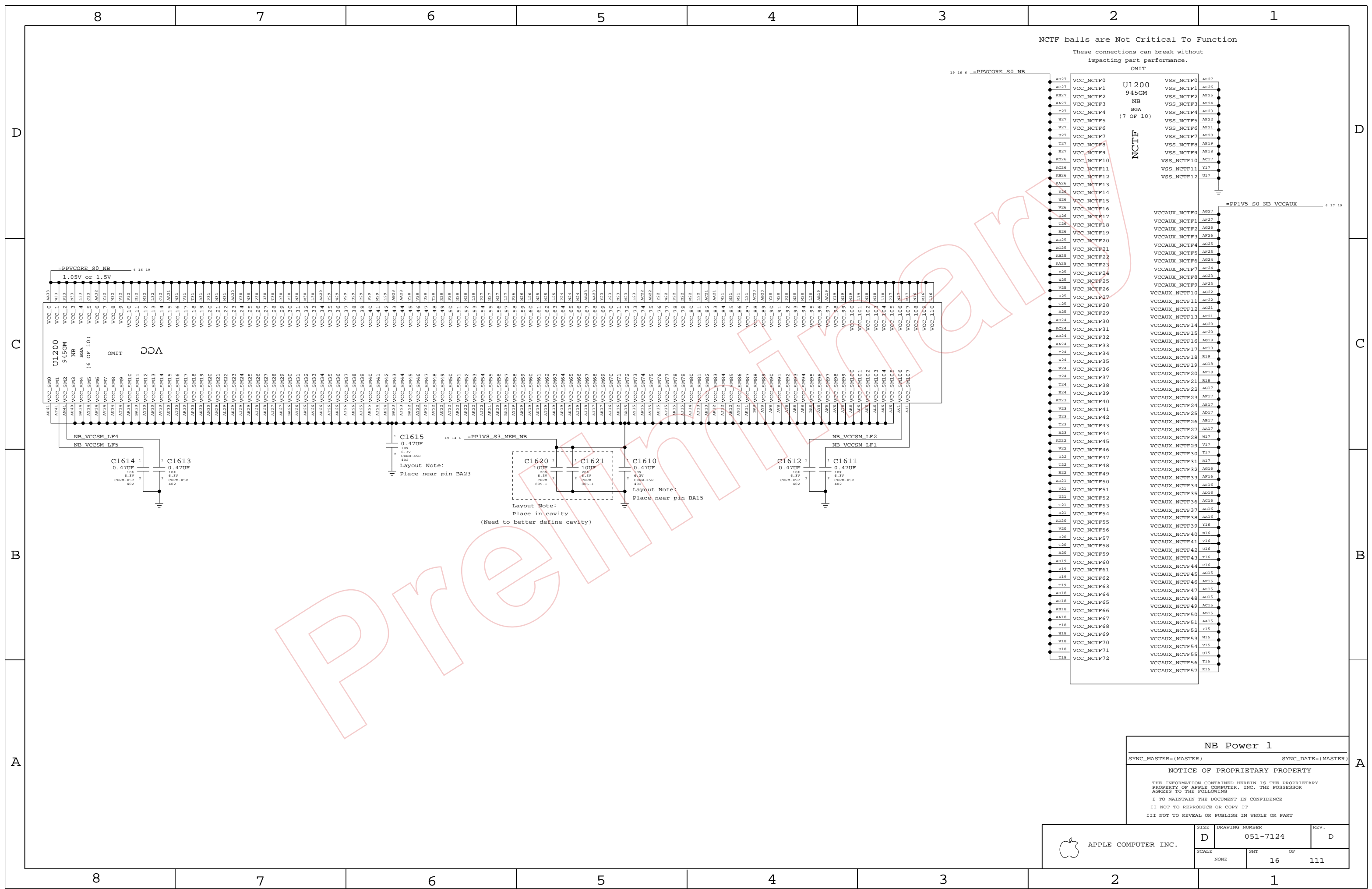
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SCALE	SHT	OF	
NONE	15	111	



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200 945GM NB BGA (7 OF 10)
 VCC
 OMIT

U1200 945GM NB BGA (7 OF 10)
 NCTF

VCCAUX_NCTF0 AG27
 VCCAUX_NCTF1 AF27
 VCCAUX_NCTF2 AG26
 VCCAUX_NCTF3 AF26
 VCCAUX_NCTF4 AG25
 VCCAUX_NCTF5 AF25
 VCCAUX_NCTF6 AG24
 VCCAUX_NCTF7 AF24
 VCCAUX_NCTF8 AG23
 VCCAUX_NCTF9 AF23
 VCCAUX_NCTF10 AG22
 VCCAUX_NCTF11 AF22
 VCCAUX_NCTF12 AG21
 VCCAUX_NCTF13 AF21
 VCCAUX_NCTF14 AG20
 VCCAUX_NCTF15 AF20
 VCCAUX_NCTF16 AG19
 VCCAUX_NCTF17 AF19
 VCCAUX_NCTF18 R19
 VCCAUX_NCTF19 AG18
 VCCAUX_NCTF20 AF18
 VCCAUX_NCTF21 R18
 VCCAUX_NCTF22 AG17
 VCCAUX_NCTF23 AF17
 VCCAUX_NCTF24 AE17
 VCCAUX_NCTF25 AD17
 VCCAUX_NCTF26 AB17
 VCCAUX_NCTF27 AA17
 VCCAUX_NCTF28 V17
 VCCAUX_NCTF29 T17
 VCCAUX_NCTF30 R17
 VCCAUX_NCTF31 AG16
 VCCAUX_NCTF32 AF16
 VCCAUX_NCTF33 AE16
 VCCAUX_NCTF34 AD16
 VCCAUX_NCTF35 AB16
 VCCAUX_NCTF36 AC16
 VCCAUX_NCTF37 AB16
 VCCAUX_NCTF38 AA16
 VCCAUX_NCTF39 Y16
 VCCAUX_NCTF40 W16
 VCCAUX_NCTF41 V16
 VCCAUX_NCTF42 U16
 VCCAUX_NCTF43 T16
 VCCAUX_NCTF44 R16
 VCCAUX_NCTF45 AG15
 VCCAUX_NCTF46 AF15
 VCCAUX_NCTF47 AE15
 VCCAUX_NCTF48 AD15
 VCCAUX_NCTF49 AC15
 VCCAUX_NCTF50 AB15
 VCCAUX_NCTF51 AA15
 VCCAUX_NCTF52 Y15
 VCCAUX_NCTF53 W15
 VCCAUX_NCTF54 V15
 VCCAUX_NCTF55 U15
 VCCAUX_NCTF56 T15
 VCCAUX_NCTF57 R15

C1614 0.47UF 6.3V CERM-XSR 402

C1613 0.47UF 6.3V CERM-XSR 402

C1615 0.47UF 6.3V CERM-XSR 402
 Layout Note:
 Place near pin BA23

C1620 10UF 6.3V CERM 805-1

C1621 10UF 6.3V CERM 805-1

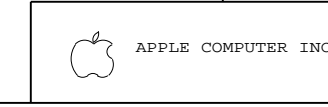
C1610 0.47UF 6.3V CERM-XSR 402
 Layout Note:
 Place near pin BA15

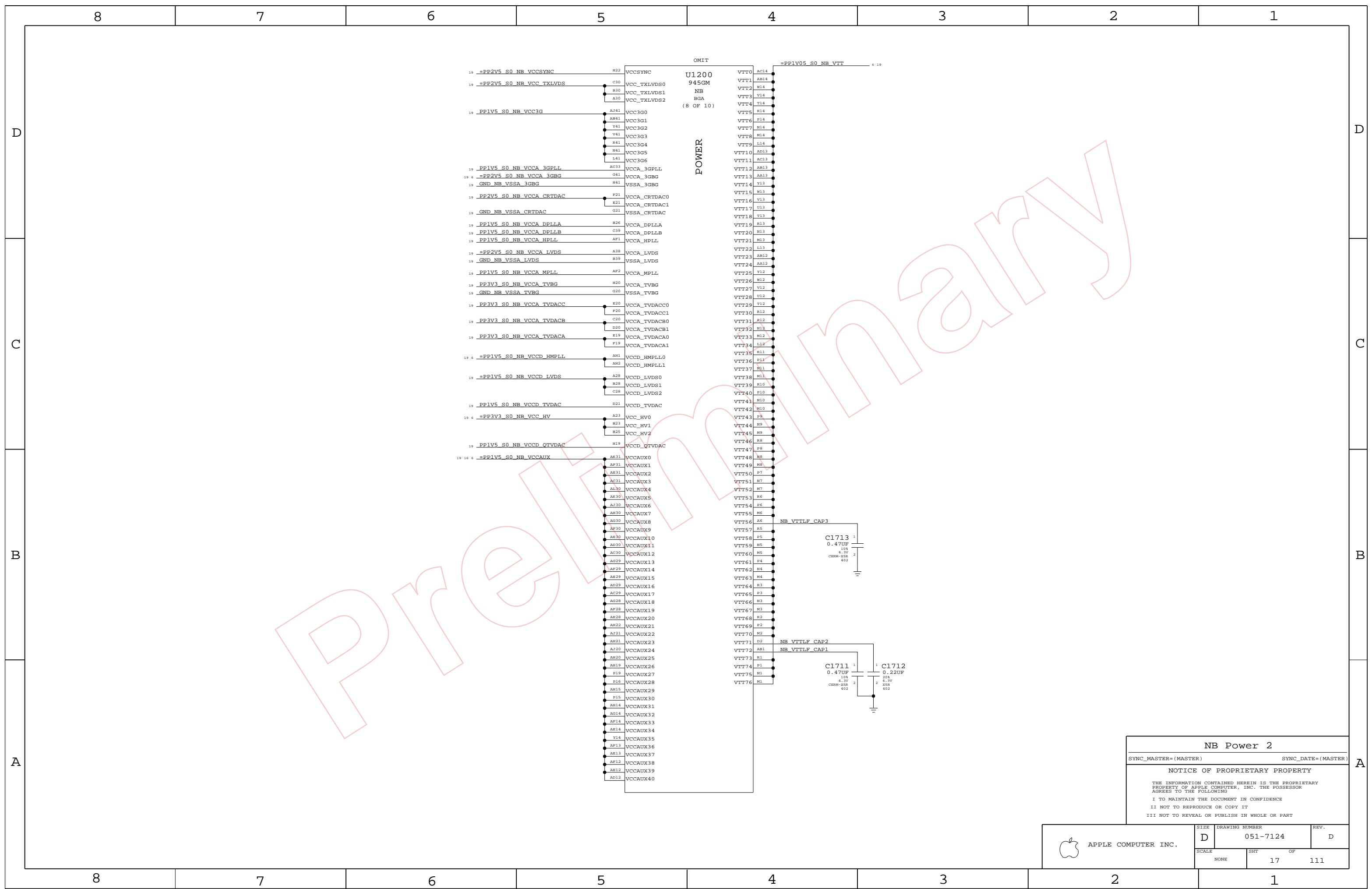
C1612 0.47UF 6.3V CERM-XSR 402

C1611 0.47UF 6.3V CERM-XSR 402

NB Power 1
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	DRAWING NUMBER		REV.
	D	051-7124	
NONE	SHT	OF	
	16	111	





Pre-release

NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

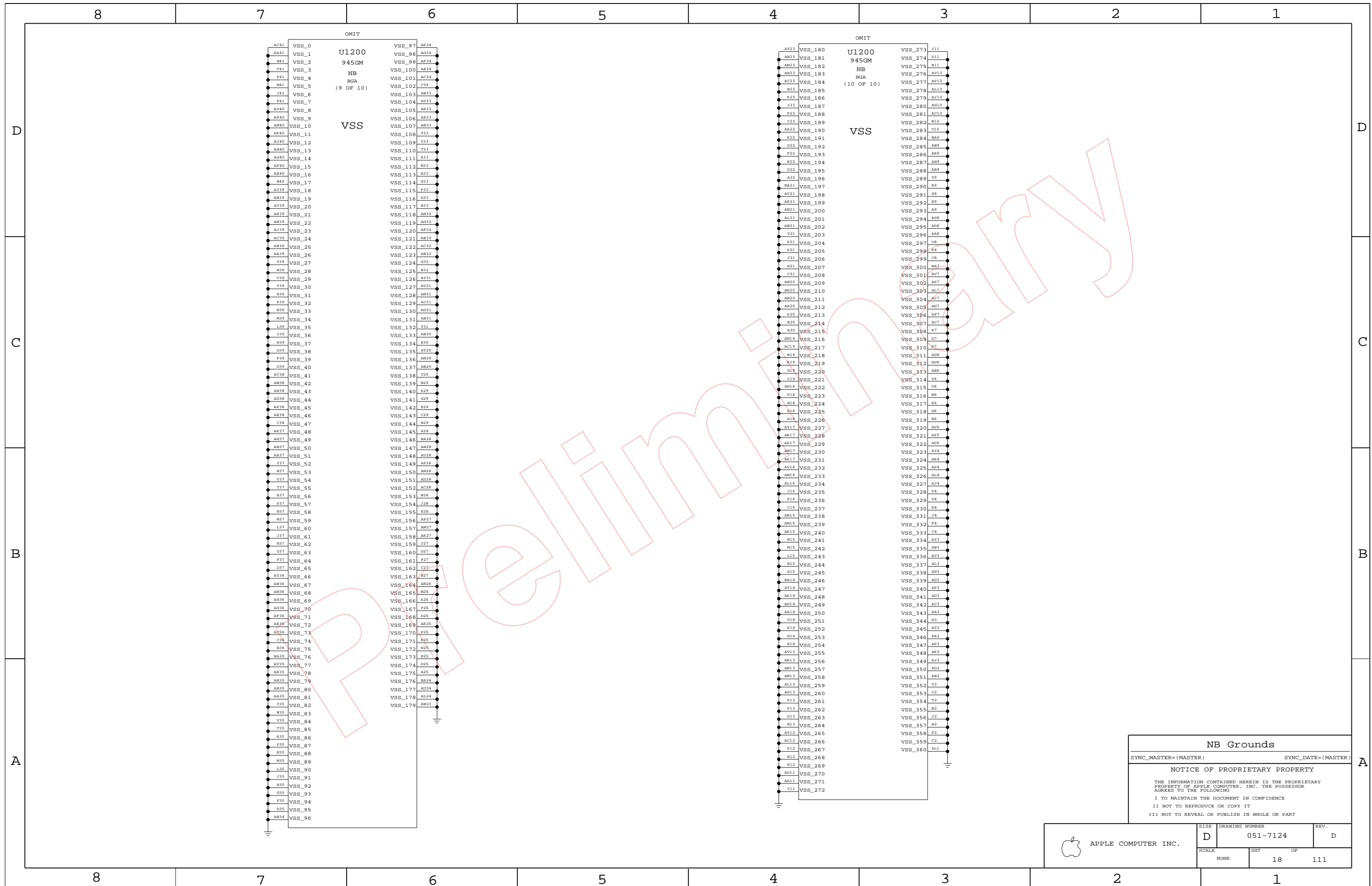
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHT 17	OF 111



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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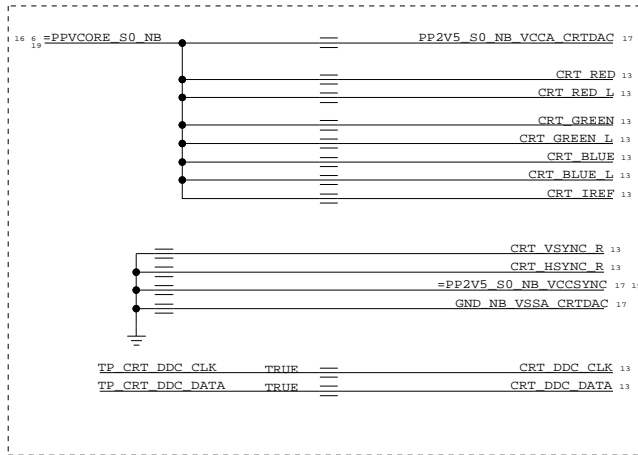
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET 18	OF 111

Power Interface

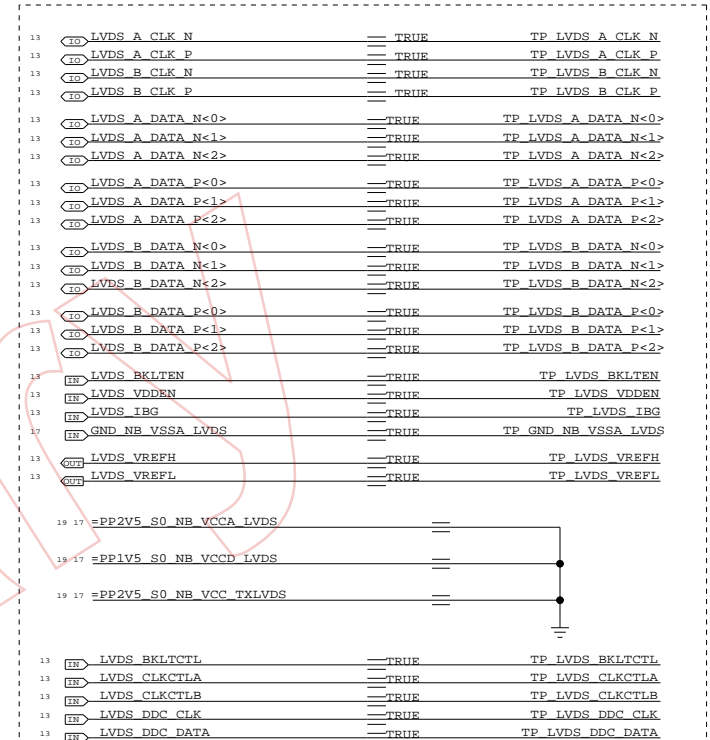
These are the power signals that leave the NB "block"

IN	=PP1V05_S0_FSB_NB	5 6 12
IN	=PPVCORE_S0_NB	6 16 19
IN	=PP1V05_S0_NB	6
IN	=PP1V05_S0_NB_VTT	6 17 19
IN	=PP1V5_S0_NB	6 19
IN	=PP1V5_S0_NB_PCIE	6 13
IN	=PP1V5_S0_NB_PLL	6 19
IN	=PP1V5_S0_NB_TVDAC	6 19
IN	=PP1V5_S0_NB_VCCD_HMPLL	6 19
IN	=PP1V5_S0_NB_VCCD_LVDS	17 19
IN	=PP1V5_S0_NB_VCCAUX	6 16 17 19
IN	=PP1V8_S3_MEM_NB	6 14 16 19
IN	=PP2V5_S0_NB_VCCSYNCR	17 19
IN	=PP2V5_S0_NB_VCC_TXLVDS	17 19
IN	=PP2V5_S0_NB_VCCA_3GBG	6 17 19
IN	=PP2V5_S0_NB_VCCA_LVDS	17 19
IN	=PP3V3_S0_NB	6 14 20
IN	=PP3V3_S0_NB_TVDAC	6
IN	=PP3V3_S0_NB_VCC_HV	6 17 19

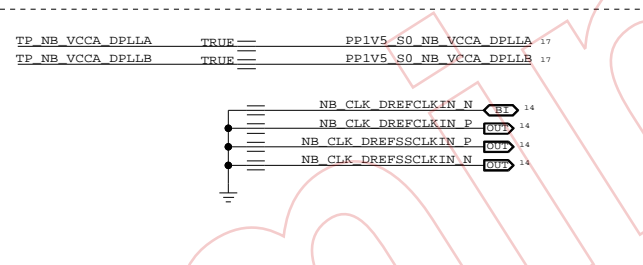
TVOUT DISABLE



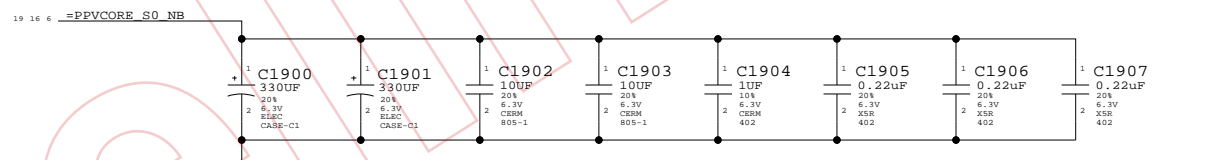
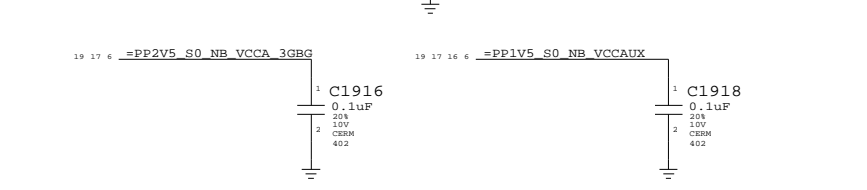
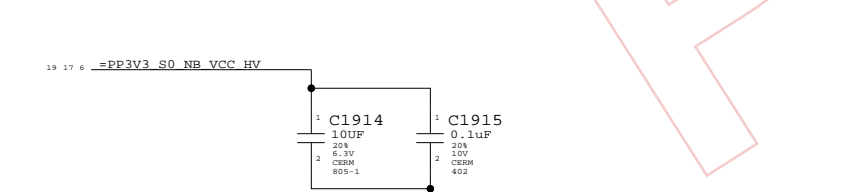
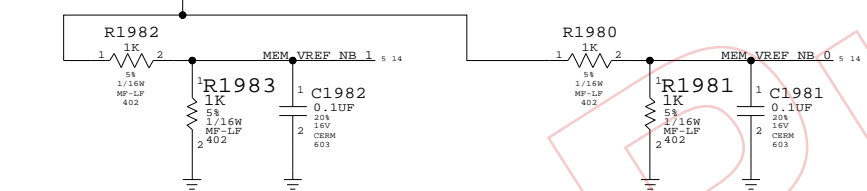
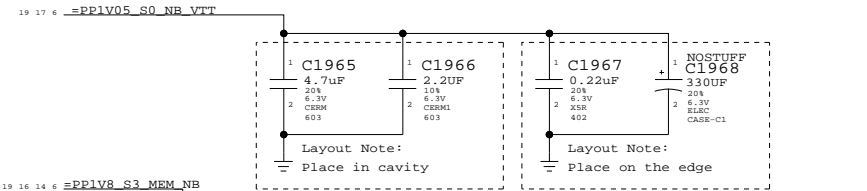
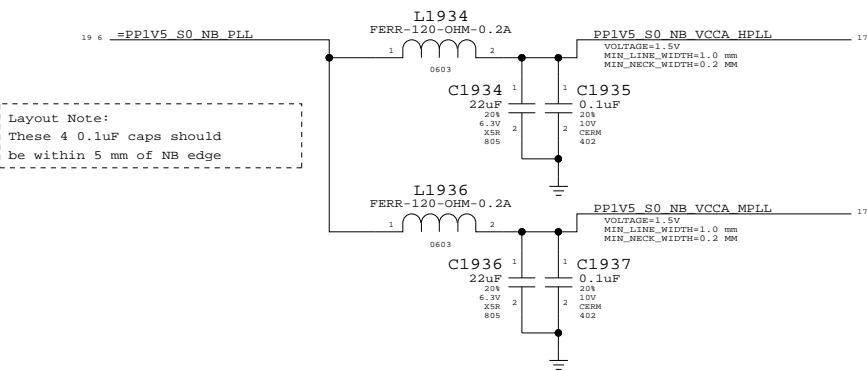
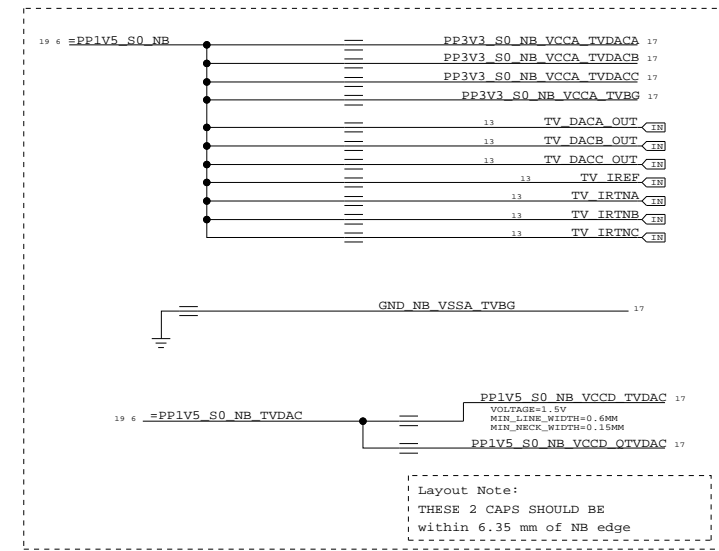
LVDS DISABLE



DISPLAY DISABLE

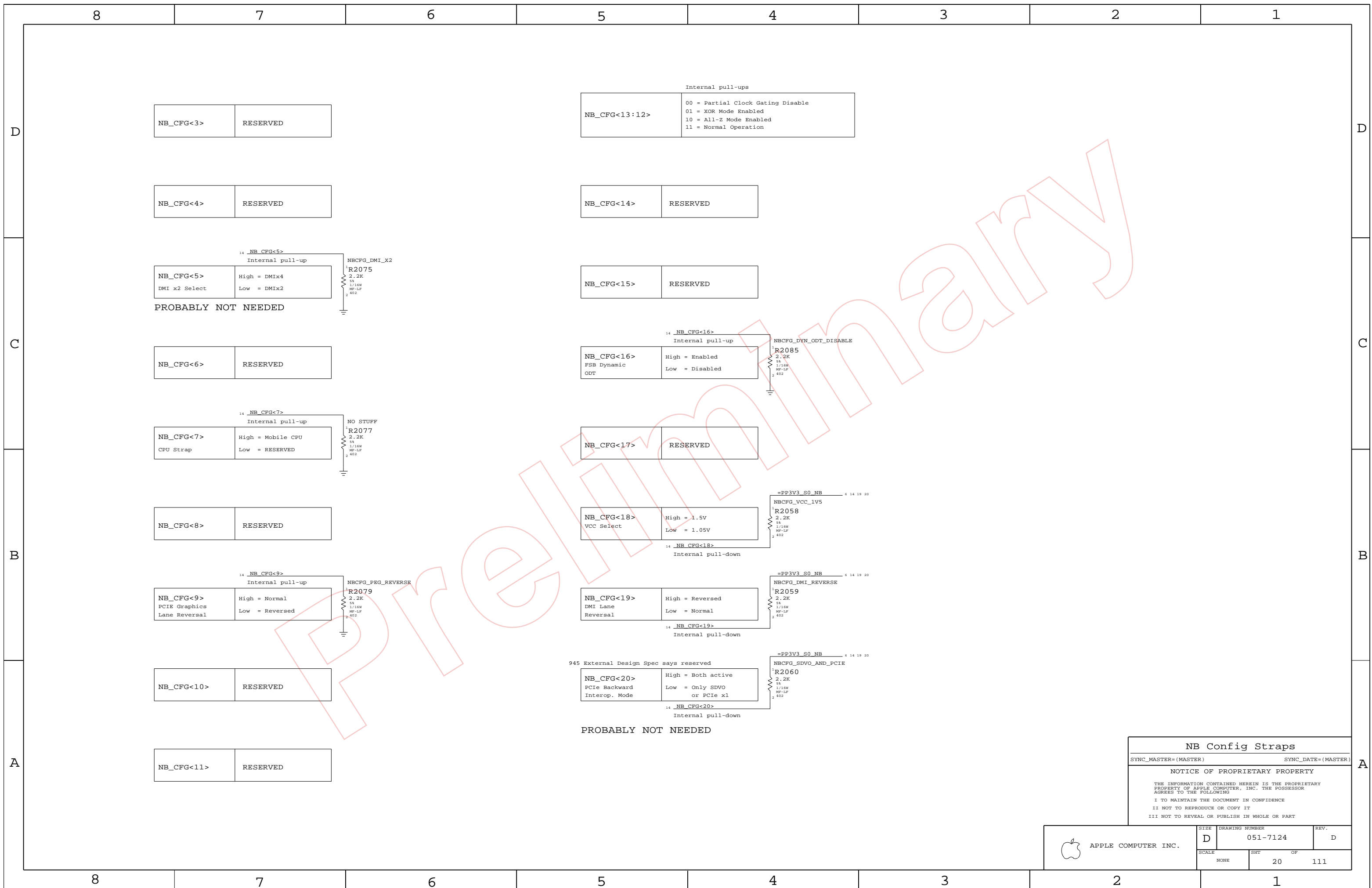


TVOUT DISABLE



NB (GM) Decoupling
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7124	D
SCALE	SHT	OF	
NONE	19	111	



NB Config Straps

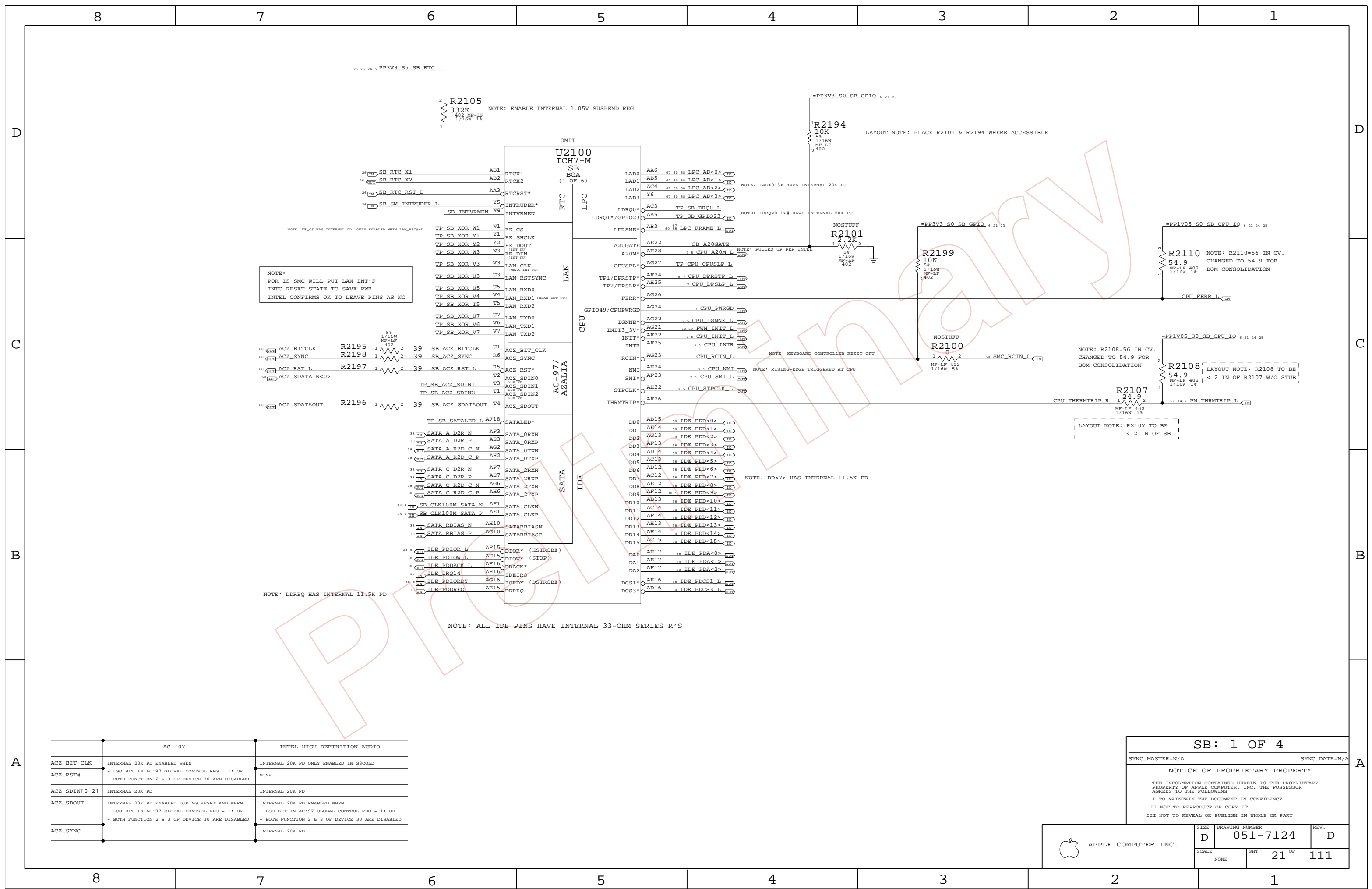
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	D
SCALE	SHT	OF	
NONE	20	111	



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

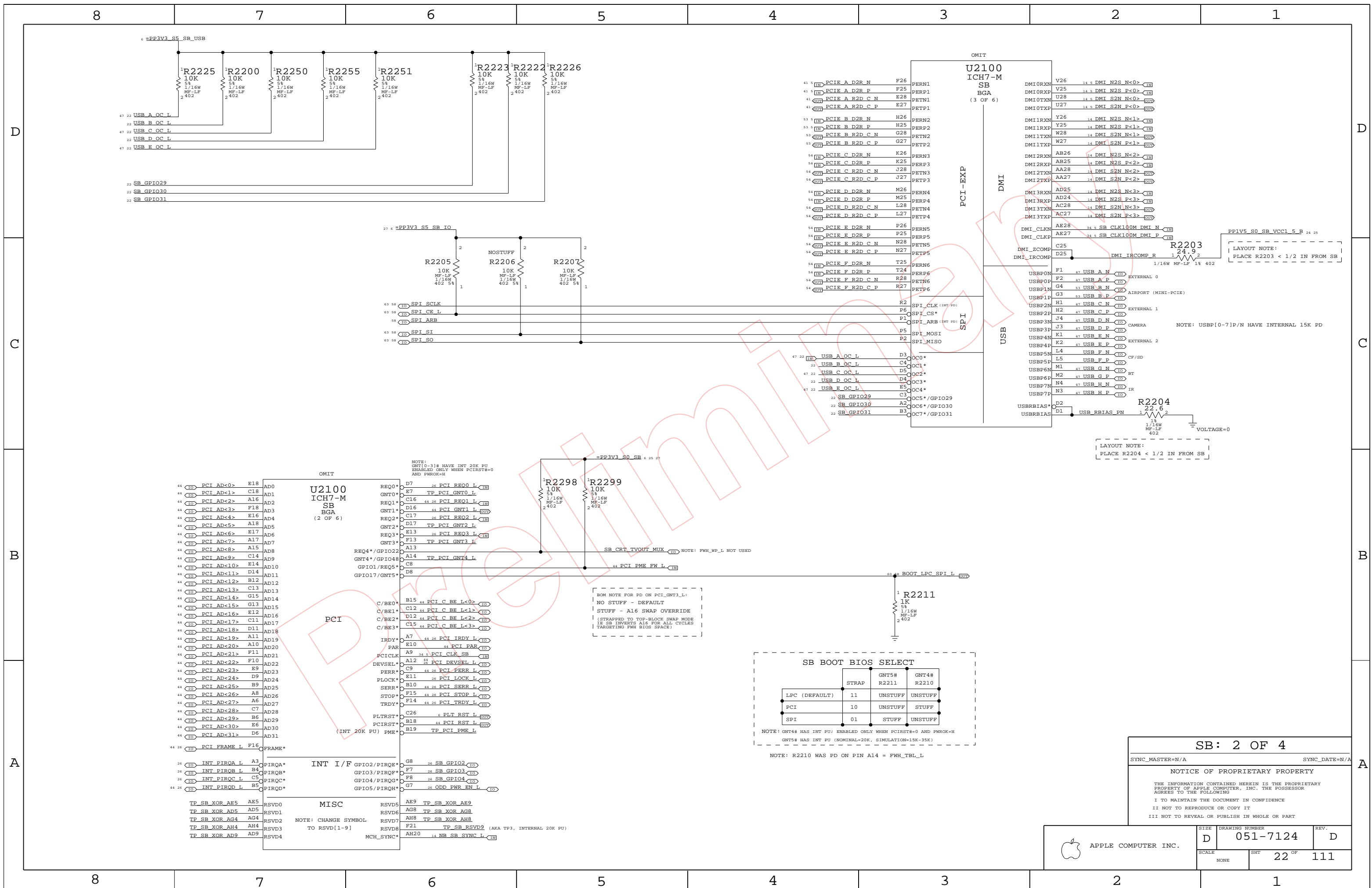
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NOTICE OF PROPRIETARY PROPERTY

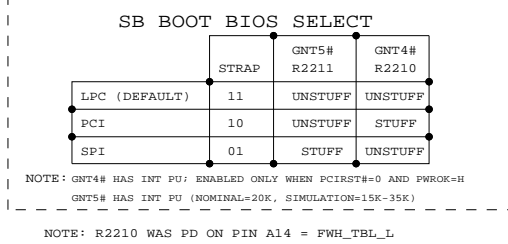
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	D	051-7124	D
SCALE	SHT	21 OF	111
NONE			



BOM NOTE FOR PD ON PCI_GNT3_L:
 NO STUFF - DEFAULT
 STUFF - A16 SWAP OVERRIDE
 (STRAPPED TO TOP-BLOCK SWAP MODE
 IF SB INVERTS A16 FOR ALL CYCLES
 TARGETING FWB BIOS SPACE)

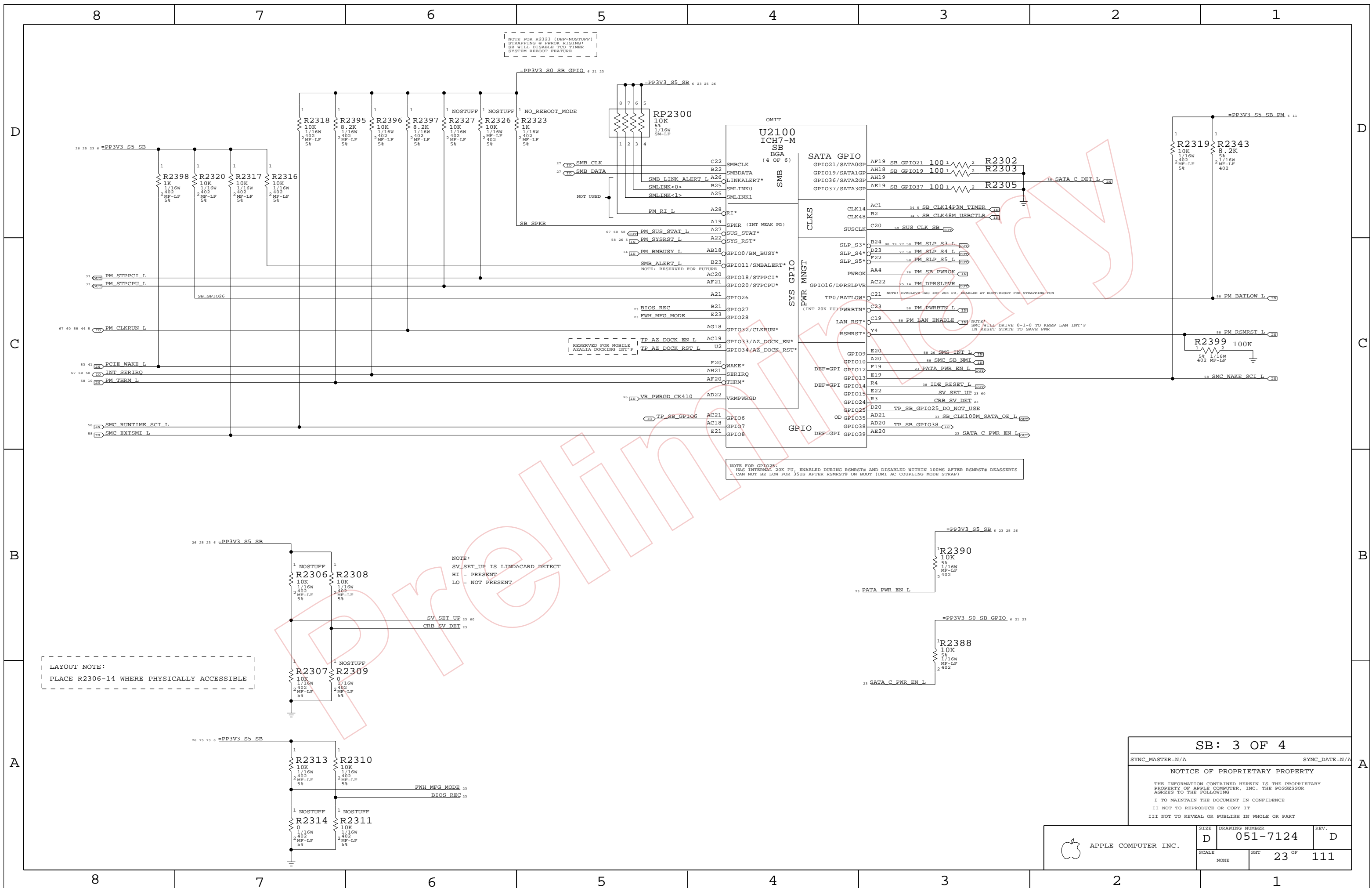


SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7124	D
SCALE	SHT	22 OF	111
NONE			



NOTE FOR R2323 (DEF-NOSTUFF)
STRAPPING & PWROK RISING:
SB WILL DISABLE TOO TIMER
SYSTEM REBOOT FEATURE

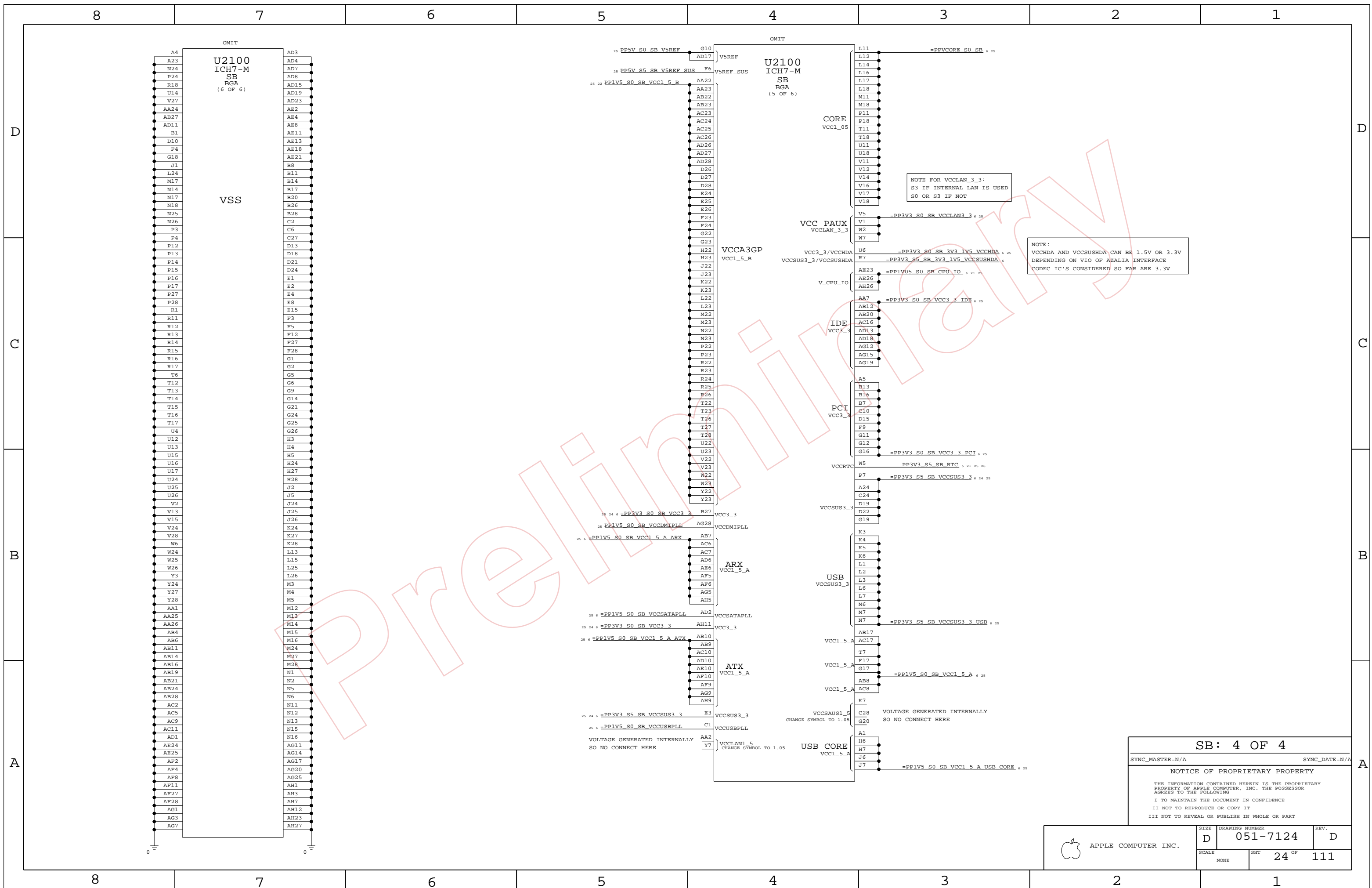
NOTE FOR GPIO25:
* HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
* CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (EMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SB: 3 OF 4
SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7124	D
SCALE	NONE	SHT	23 OF 111



SB: 4 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

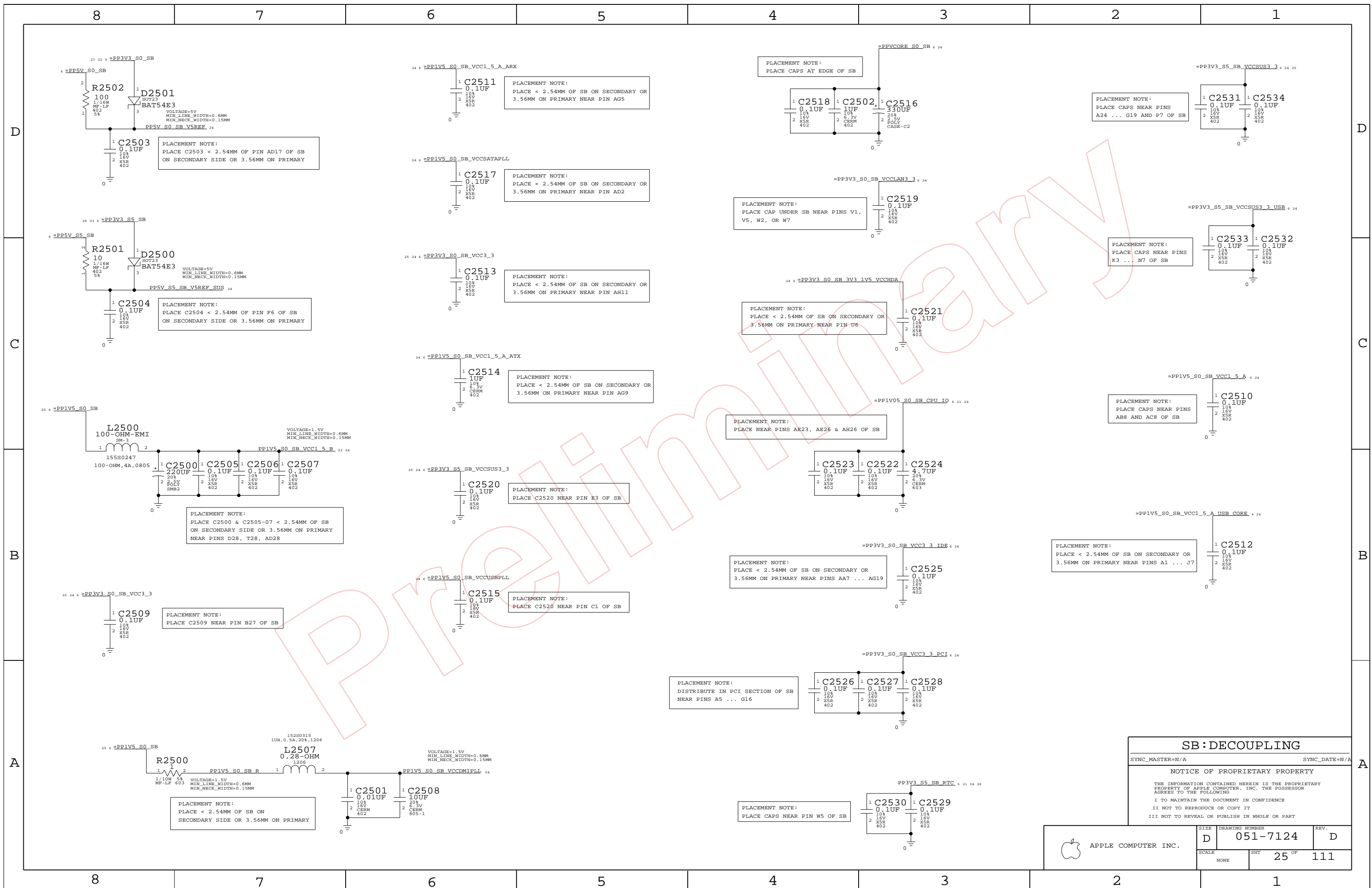
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	REV.	
NONE	24 OF 111		



SB: DECOUPLING

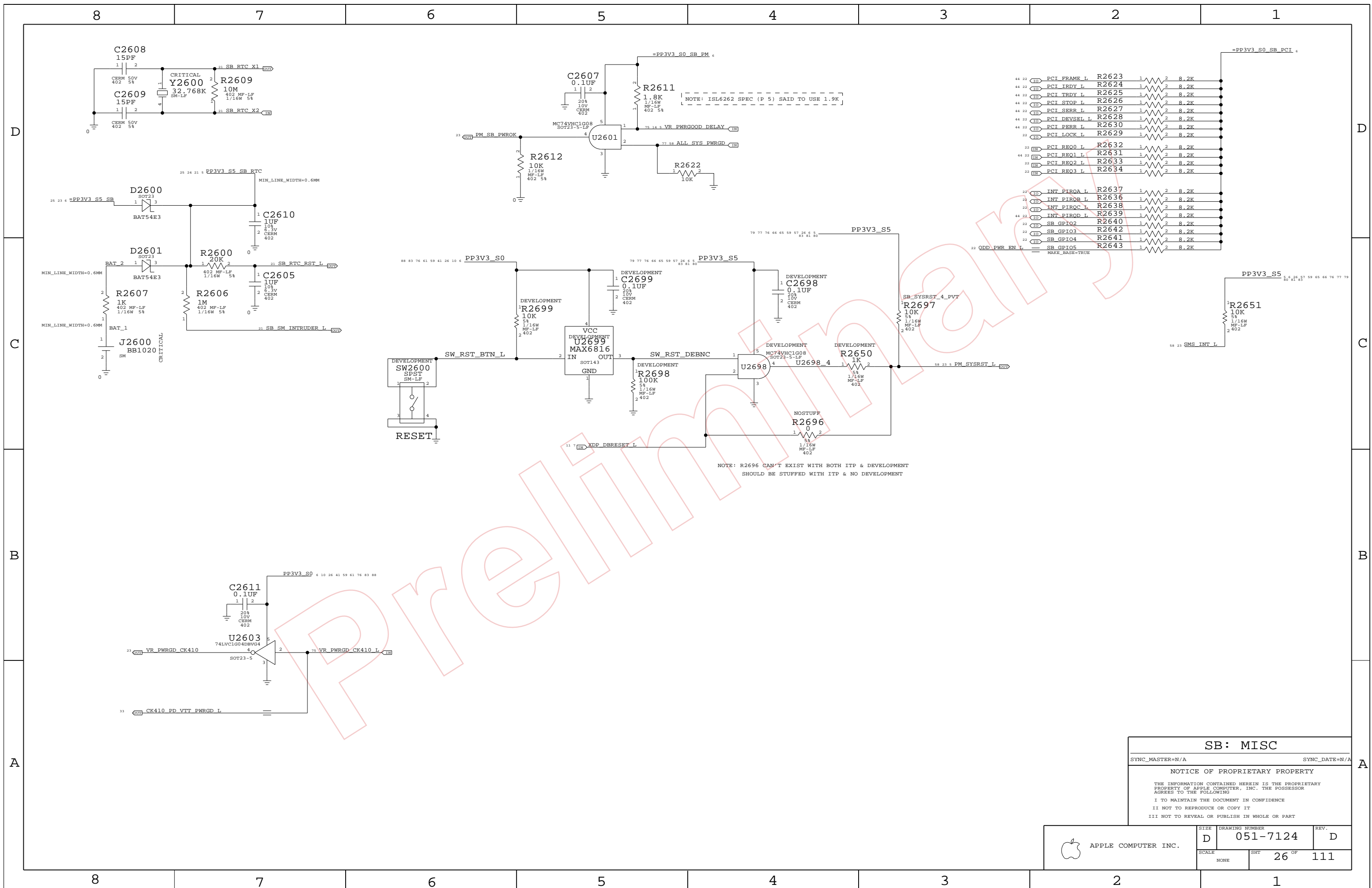
SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7124	D
SCALE	SHT	25 OF	111
NONE			



SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

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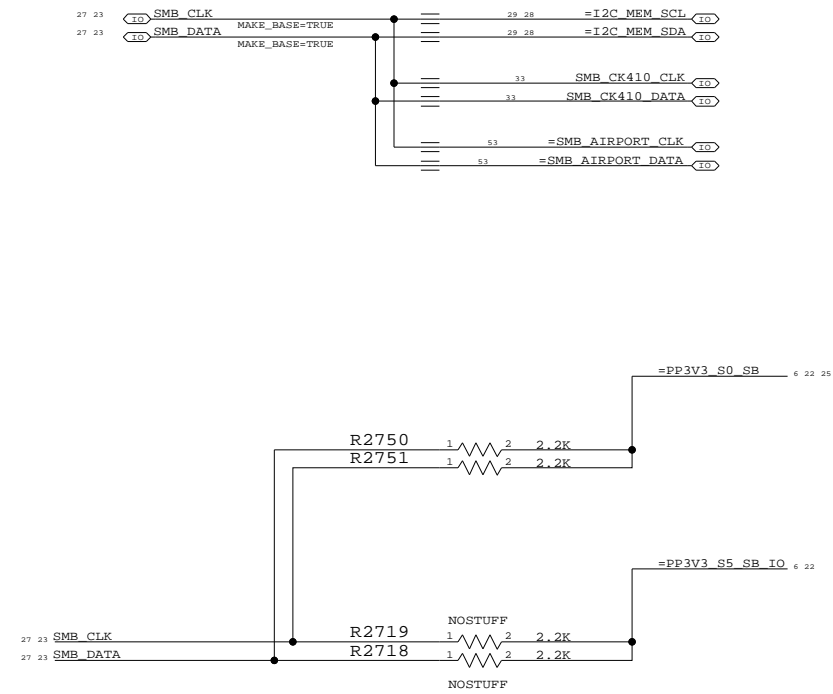
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	26 OF	111
NONE			

SB I2C BUSSES



Preliminary


SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	27 OF 111	
NONE			

Page Notes

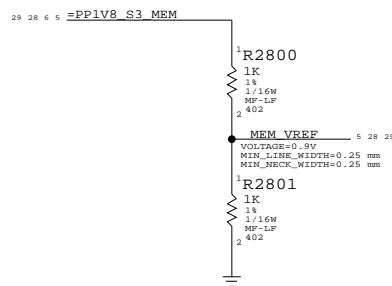
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector



Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

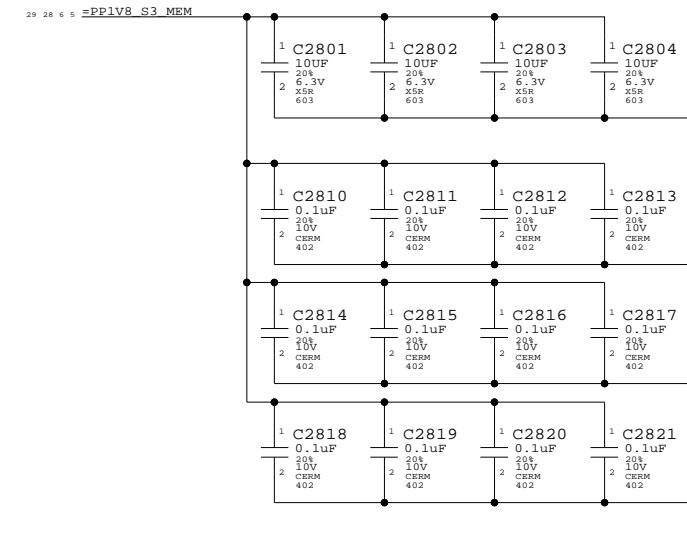
PR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0503	1	DDR2 SODIMM STD	J2800	CRITICAL	

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	D
SCALE	SHT	OF	
NONE	28	111	

Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

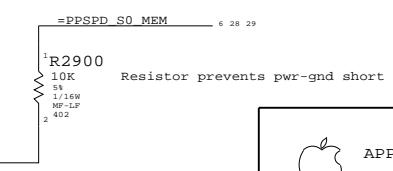
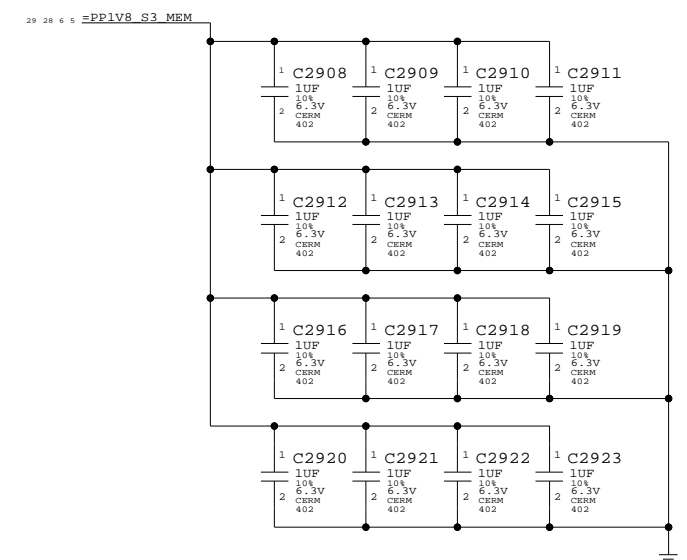
NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0504	1	DDR2 SODIMM REV	J2900	CRITICAL	



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	29	111	

8

7

6

5

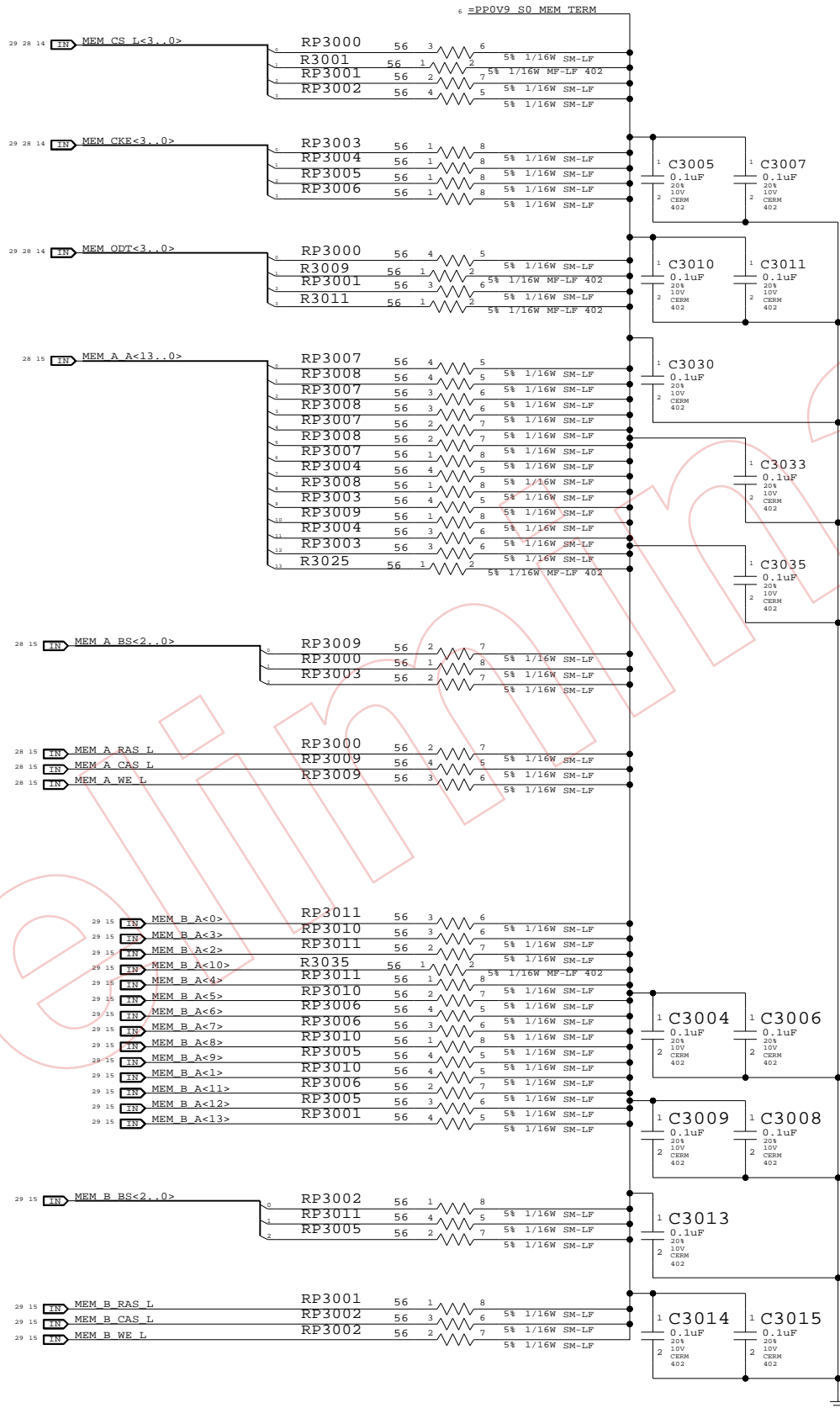
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	D
SCALE	SHT	OF
NONE	30	111

8

7

6

5

4

3

2

1

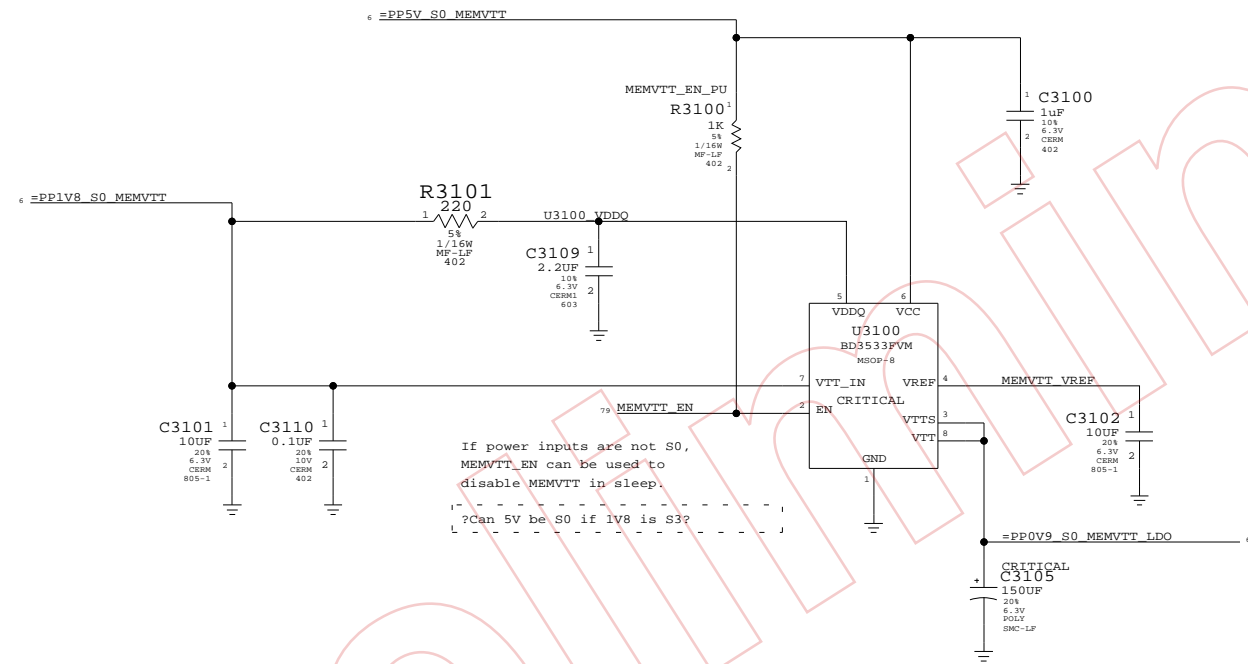
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



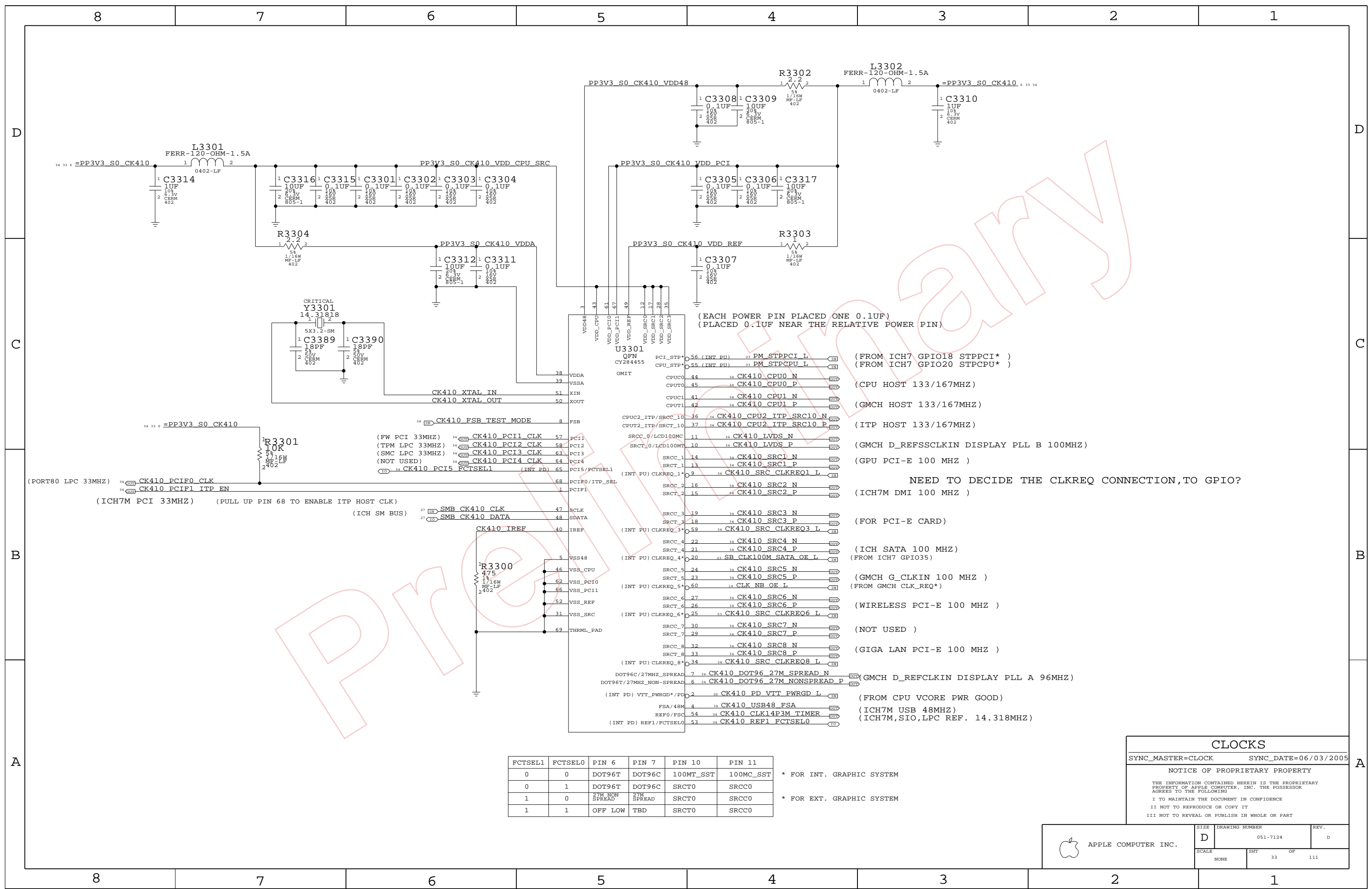
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	REV.
NONE	31	111	



- (FROM ICH7 GPIO18 STPPCI*)
- (FROM ICH7 GPIO20 STPCPU*)
- (CPU HOST 133/167MHZ)
- (GMCH HOST 133/167MHZ)
- (ITP HOST 133/167MHZ)
- (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- (GPU PCI-E 100 MHZ)
- NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?
- (ICH7M DMI 100 MHZ)
- (FOR PCI-E CARD)
- (ICH SATA 100 MHZ)
- (FROM ICH7 GPIO35)
- (GMCH G_CLKIN 100 MHZ)
- (FROM GMCH CLK_REQ*)
- (WIRELESS PCI-E 100 MHZ)
- (NOT USED)
- (GIGA LAN PCI-E 100 MHZ)
- (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- (FROM CPU VCORE PWR GOOD)
- (ICH7M USB 48MHZ)
- (ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
 * FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

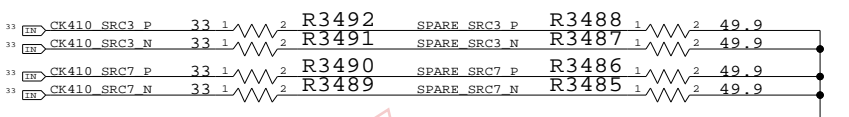
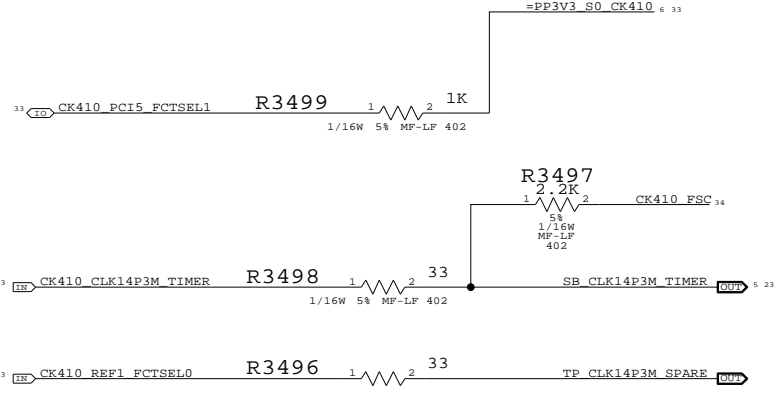
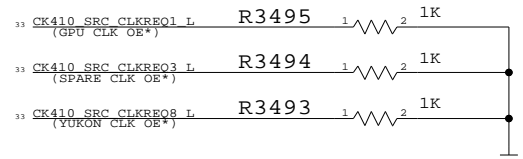
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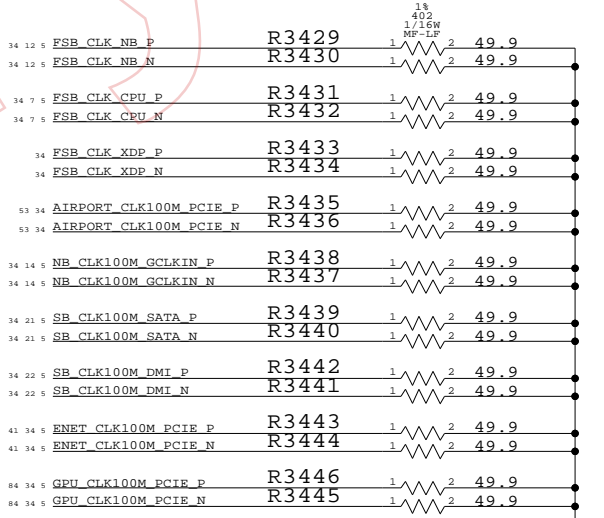
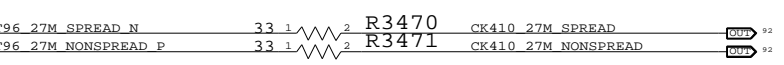
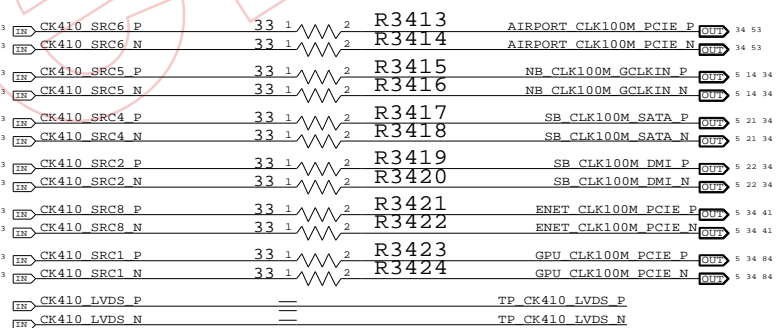
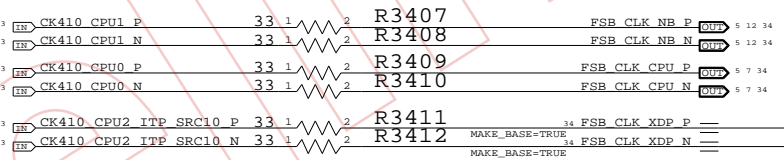
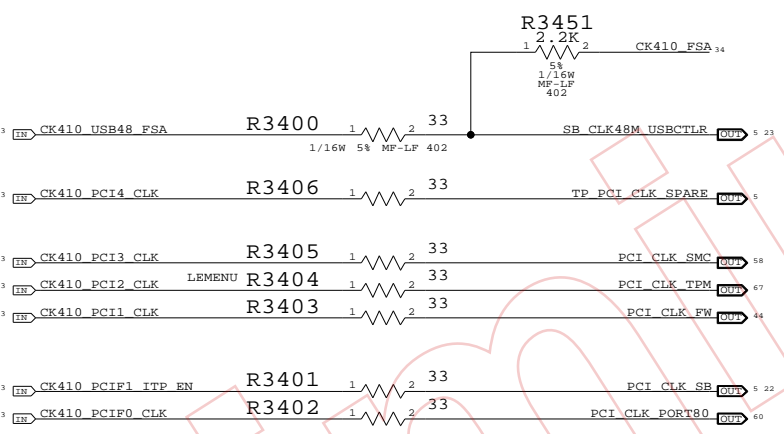
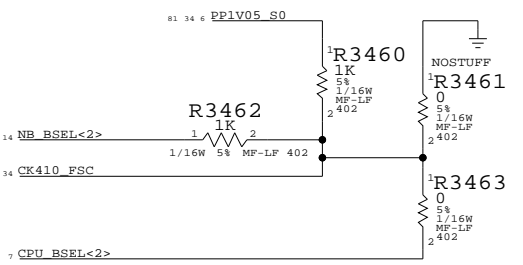
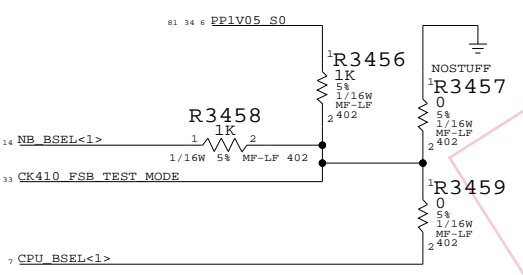
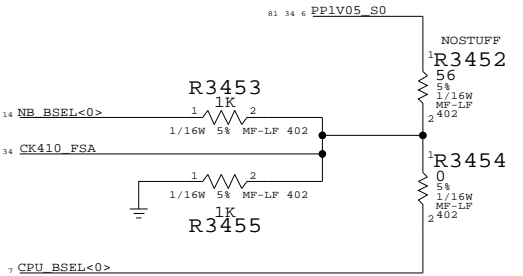
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	REV.
NONE	33	111	

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3452 R3453 R3454 R3455	R3457 R3456 R3459 R3460
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3457 R3456 R3459 R3460
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3457 R3456 R3459 R3460



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

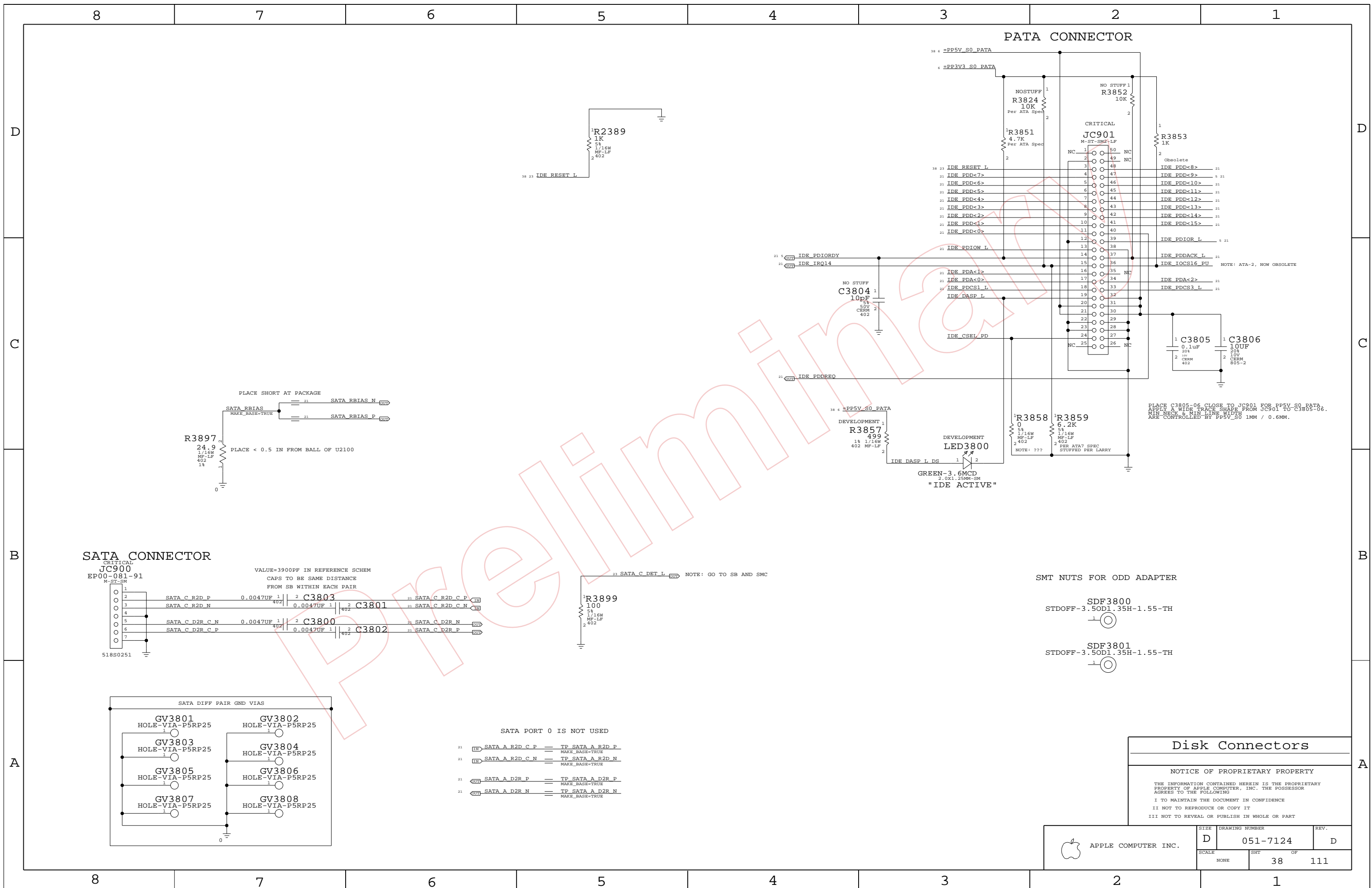
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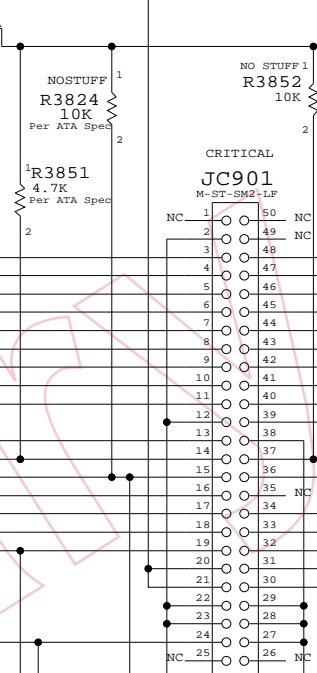
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	REV.
NONE	34	111	



PATA CONNECTOR

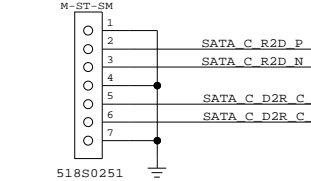
CRITICAL
JC901
M-ST-SM2-LF



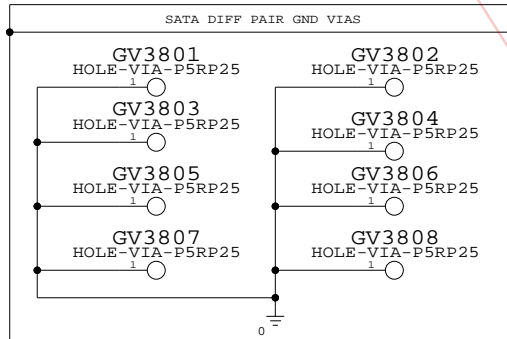
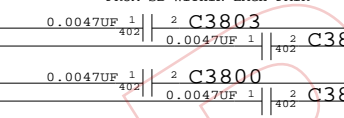
PLACE C3805-06 CLOSE TO JC901 FOR PP5V_S0_PATA.
APPLY A WIDE TRACE SHAPE FROM JC901 TO C3805-06.
WIN NECK & MIN LINE WIDTHS ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.

SATA CONNECTOR

CRITICAL
JC900
EP00-081-91
M-ST-SM



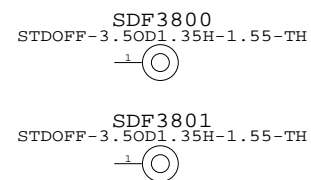
VALUE=3900PF IN REFERENCE SCHEM
CAPS TO BE SAME DISTANCE
FROM SB WITHIN EACH PAIR



SATA PORT 0 IS NOT USED

IN	SATA A R2D C P	TP_SATA A R2D P
		MAKE_BASE=TRUE
IN	SATA A R2D C N	TP_SATA A R2D N
		MAKE_BASE=TRUE
OUT	SATA A D2R P	TP_SATA A D2R P
		MAKE_BASE=TRUE
OUT	SATA A D2R N	TP_SATA A D2R N
		MAKE_BASE=TRUE

SMT NUTS FOR ODD ADAPTER

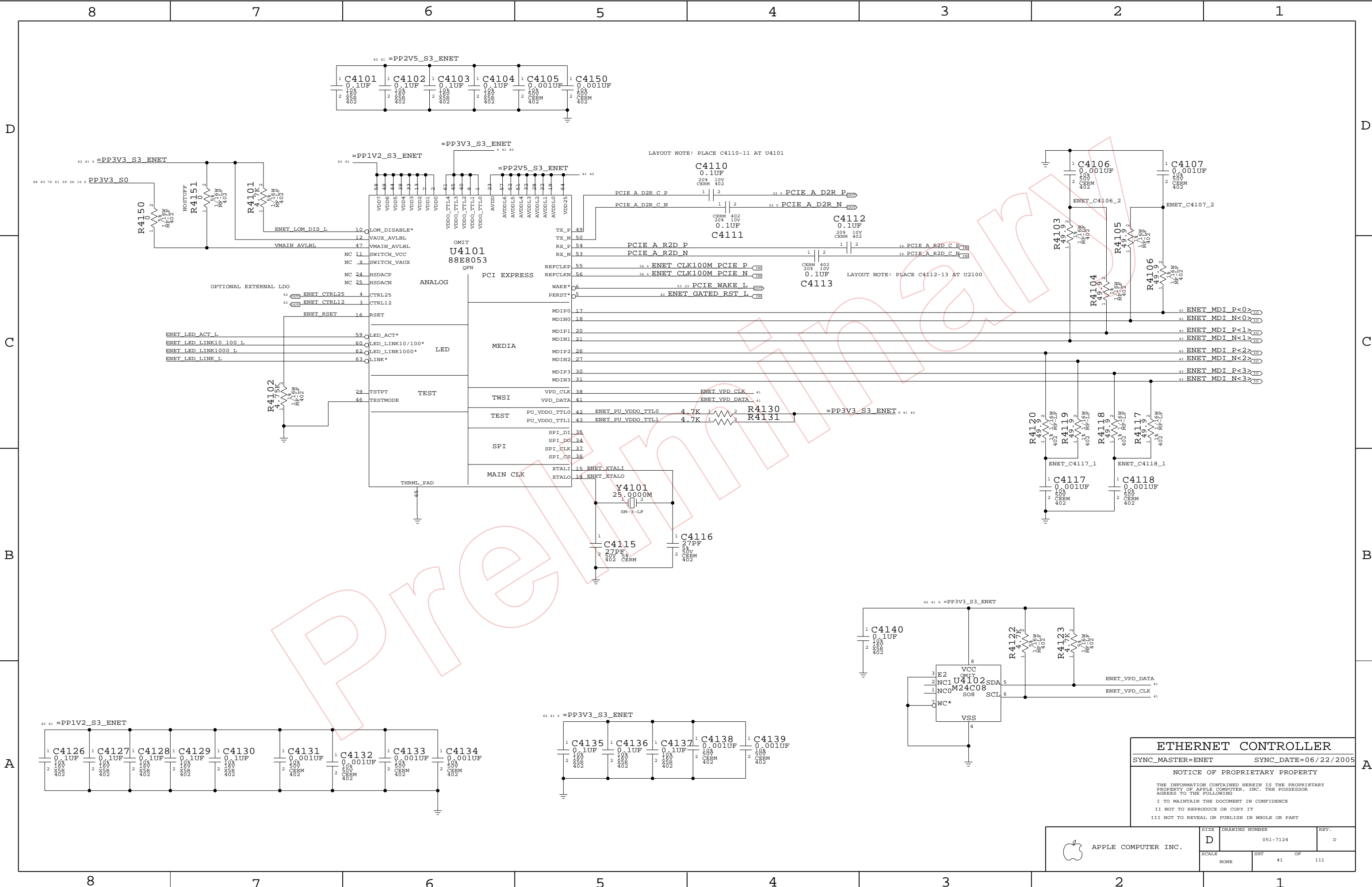


Disk Connectors

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	38	111	



PROTOTYPE

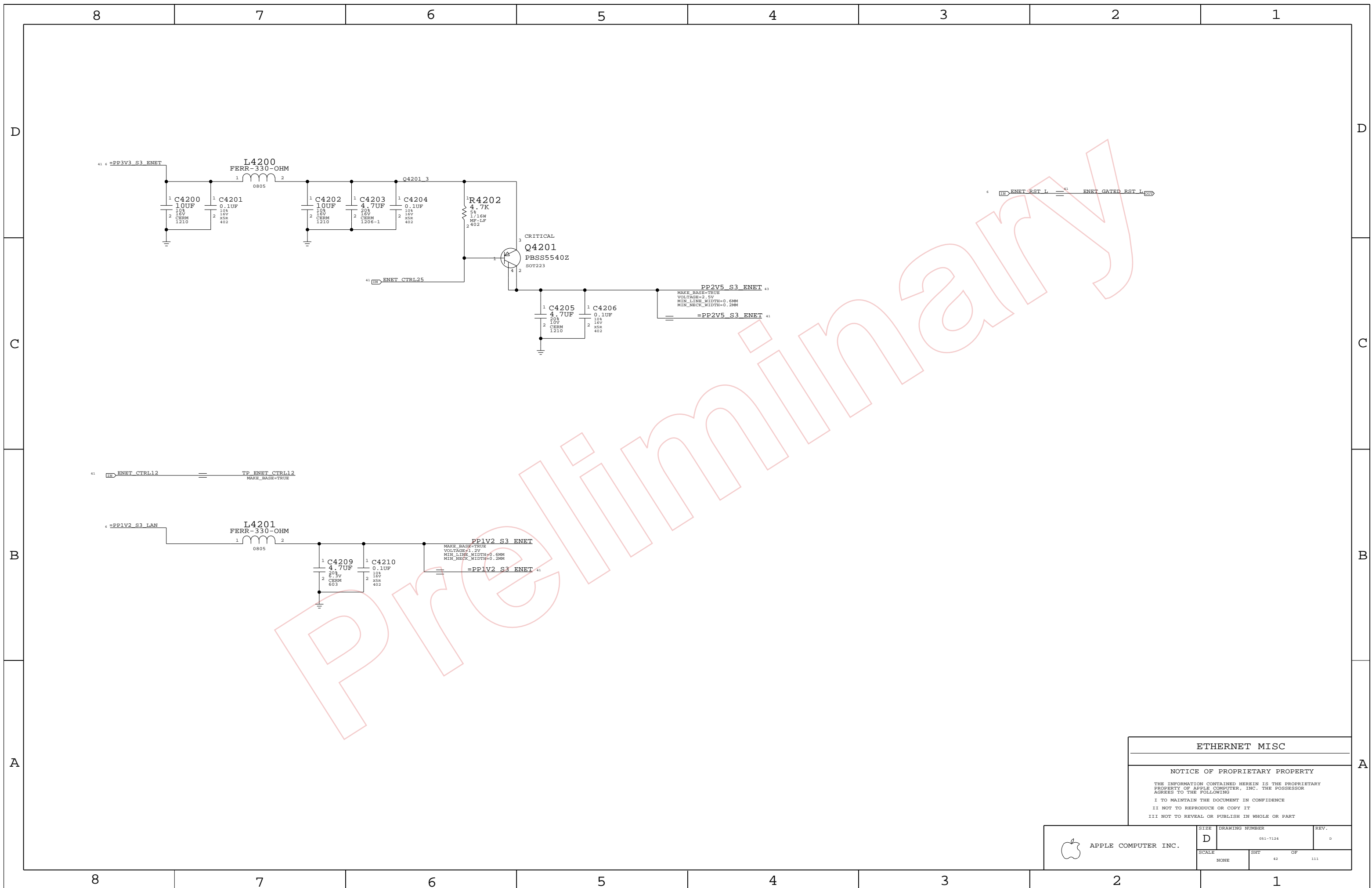
ETHERNET CONTROLLER
 SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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	D	051-7124	D
SCALE	SHT	OF	111
NONE	41	111	



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

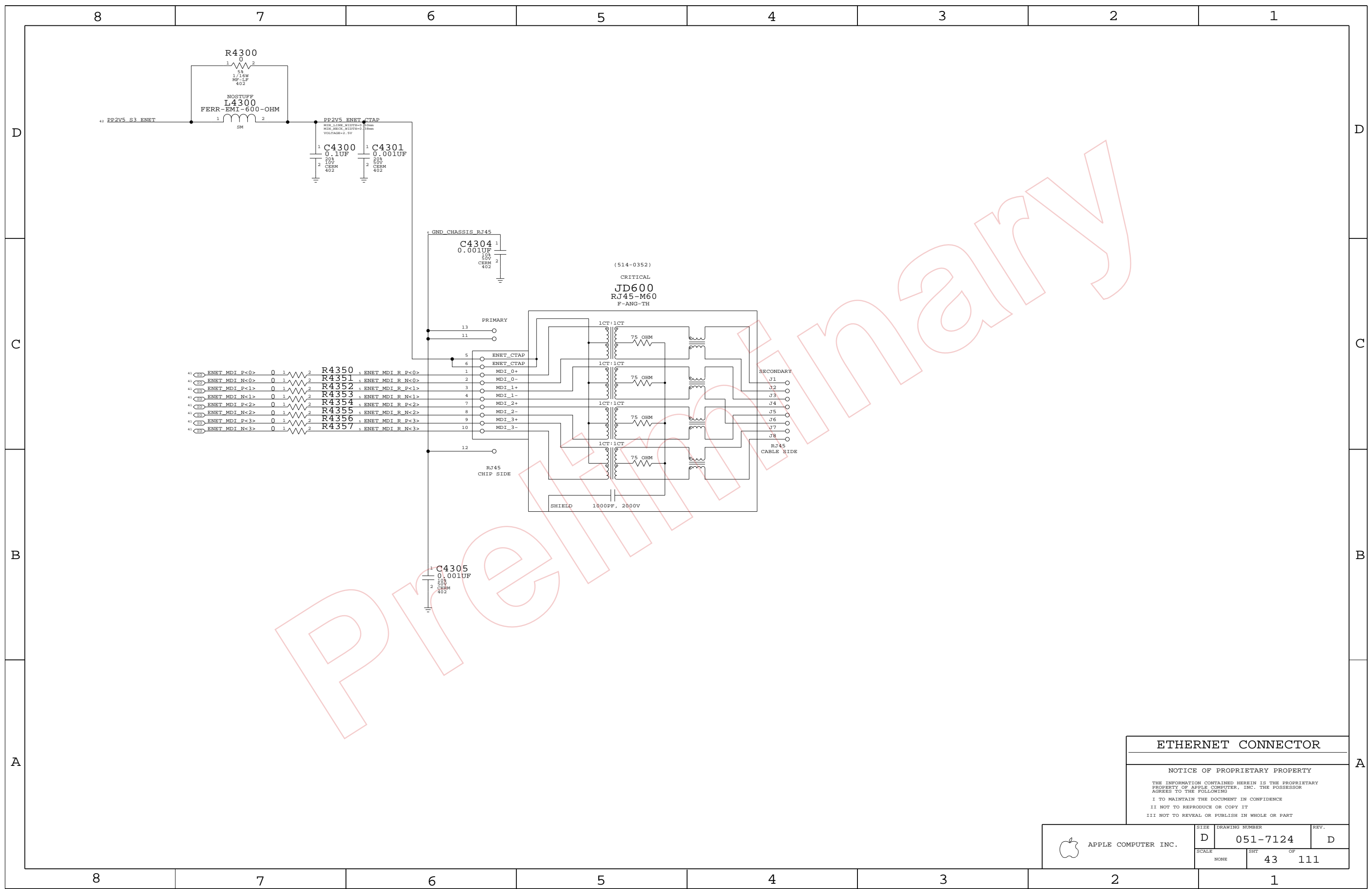
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET 42	OF 111

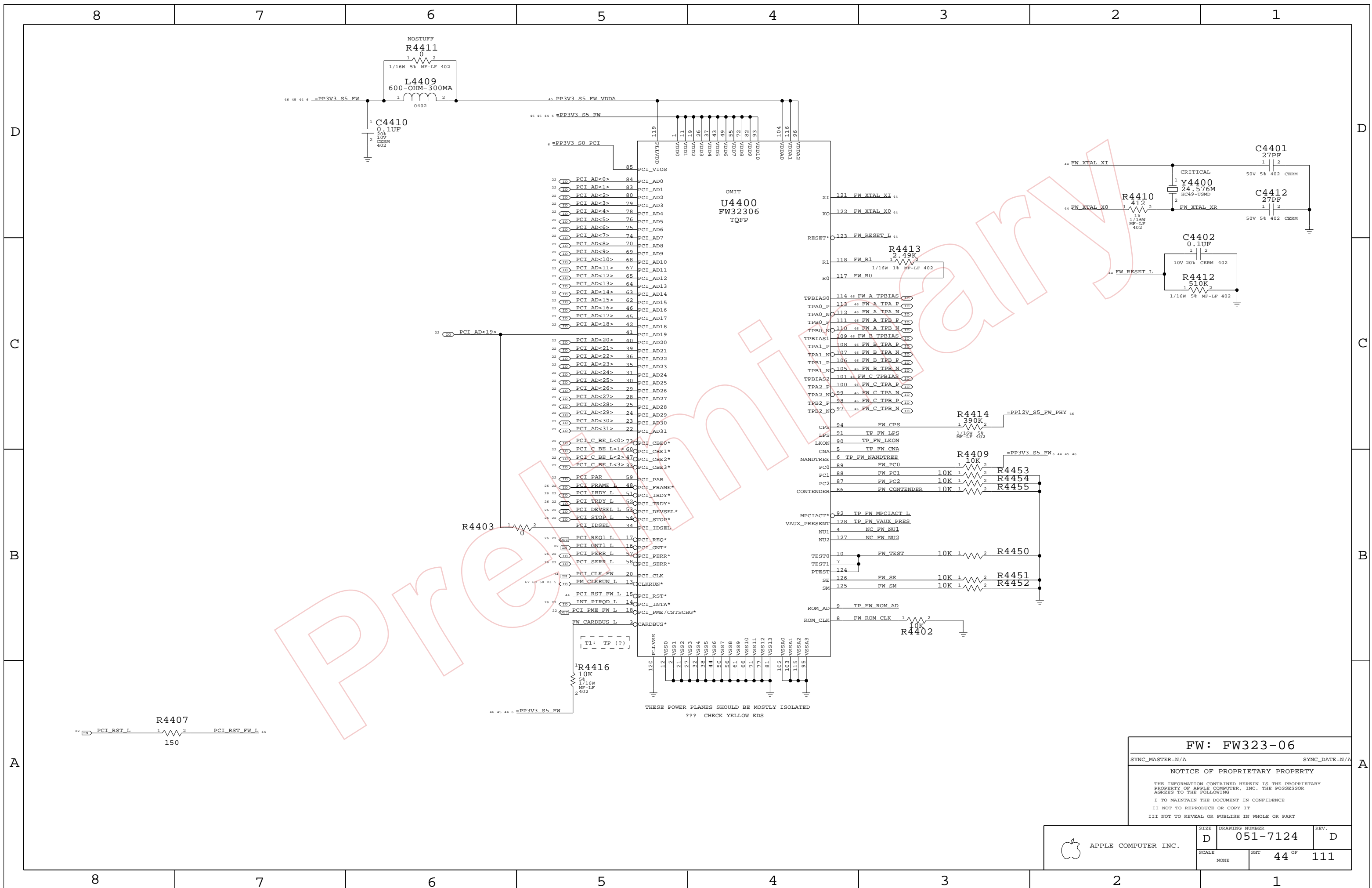


ETHERNET CONNECTOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT OF		
NONE	43 OF 111		



FW: FW323-06

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

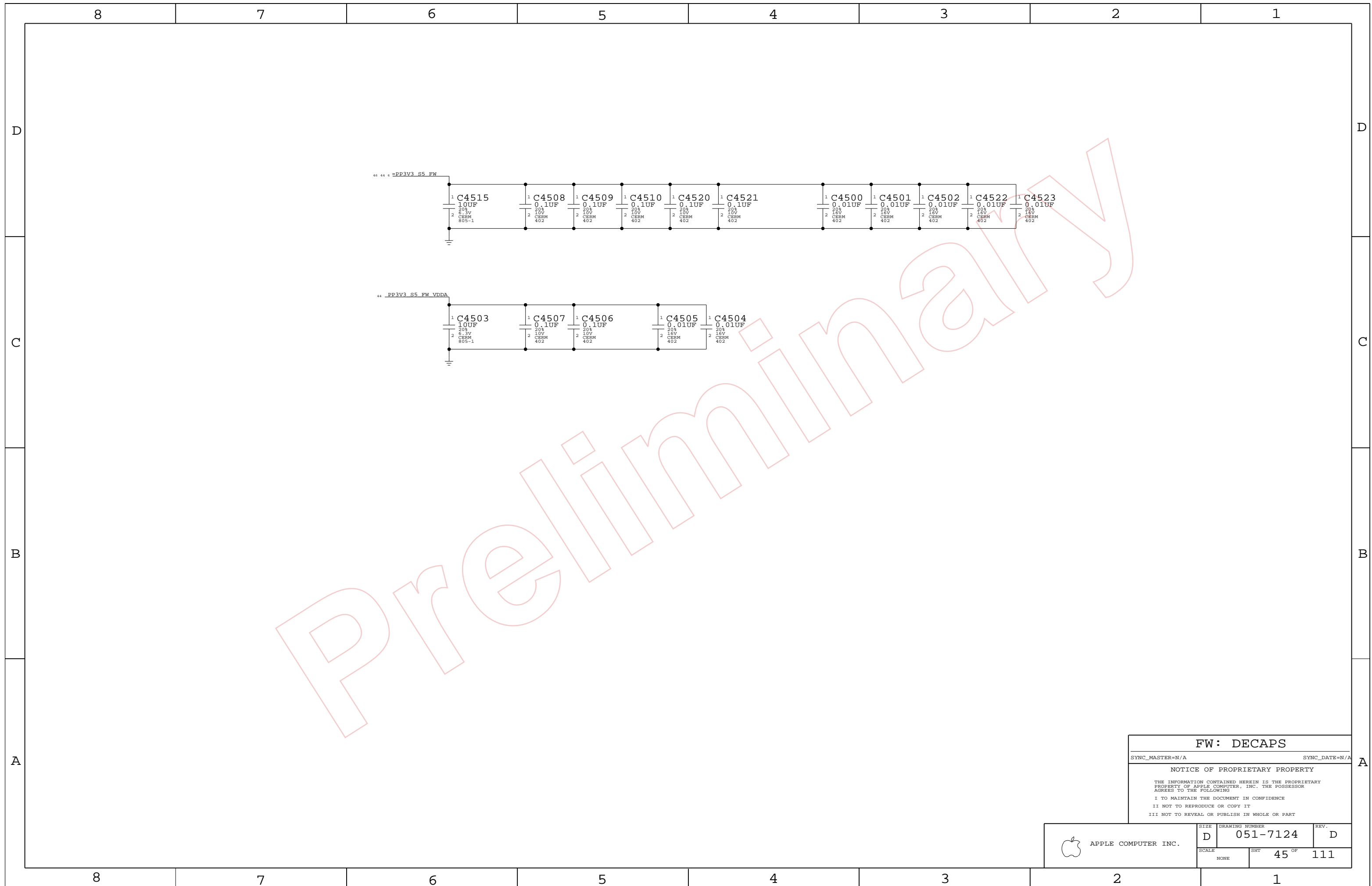
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	44 OF	111
NONE			



Preliminary

FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

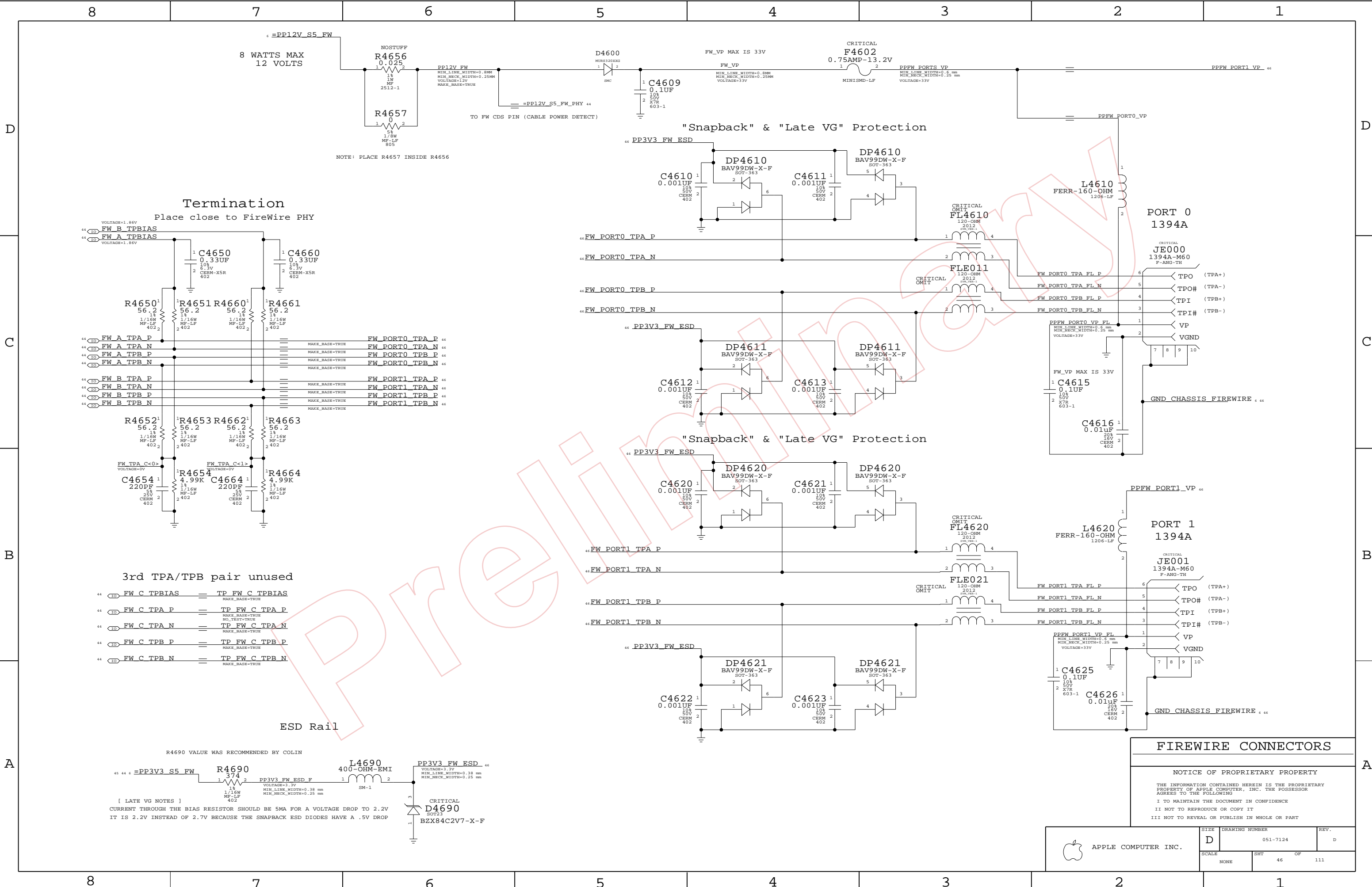
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	REV.
NONE	45	111	



FIREWIRE CONNECTORS

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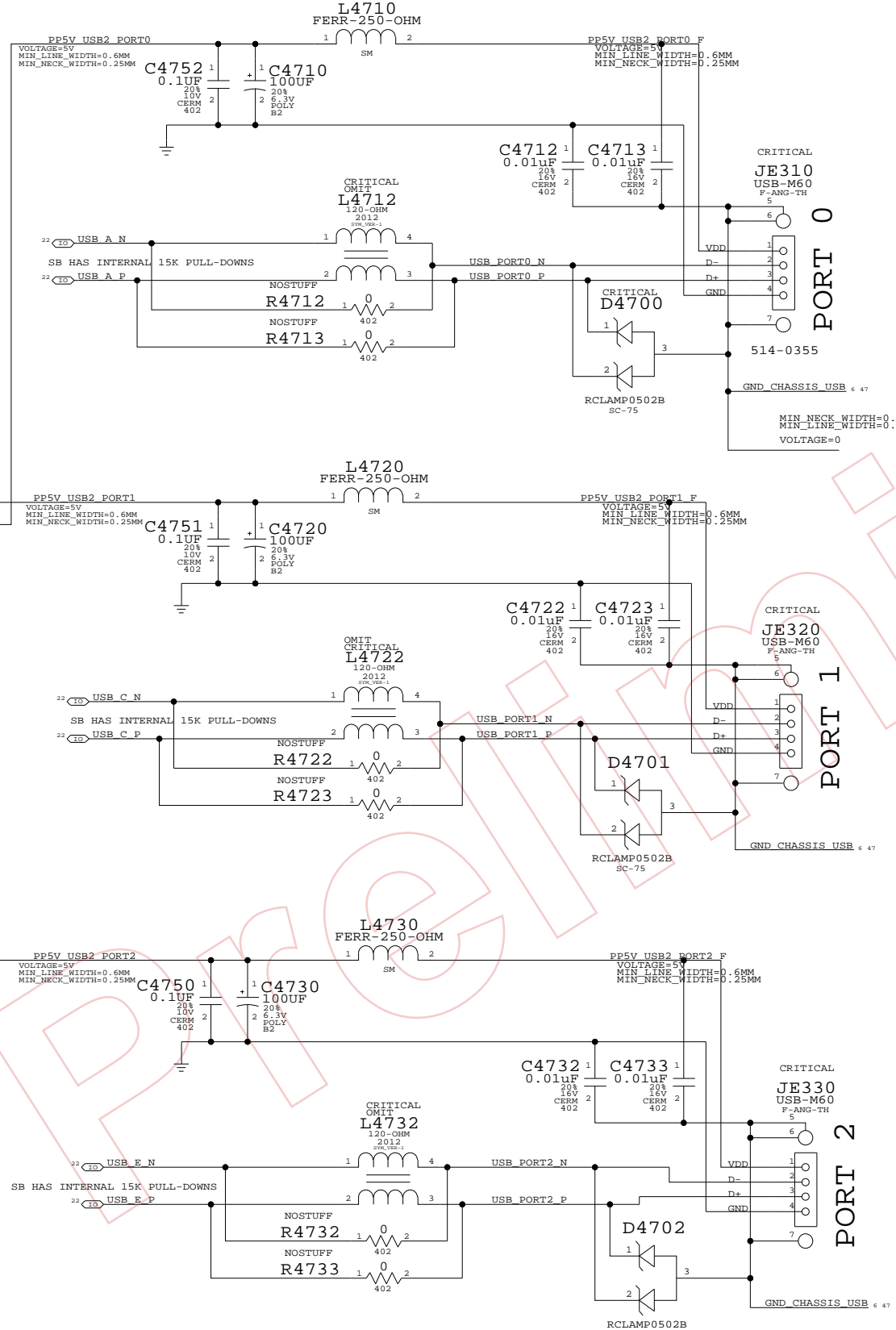
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

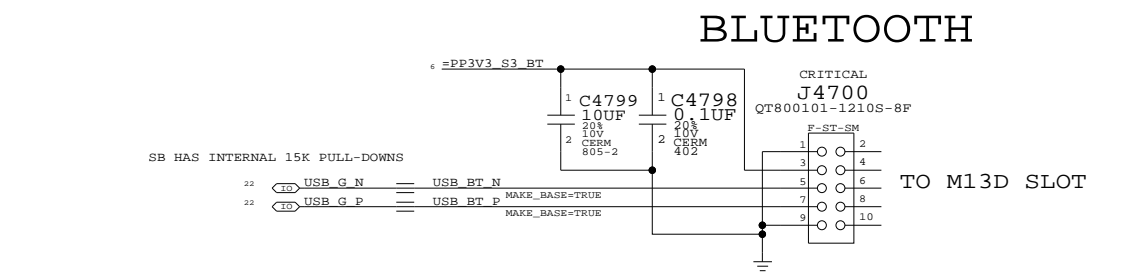
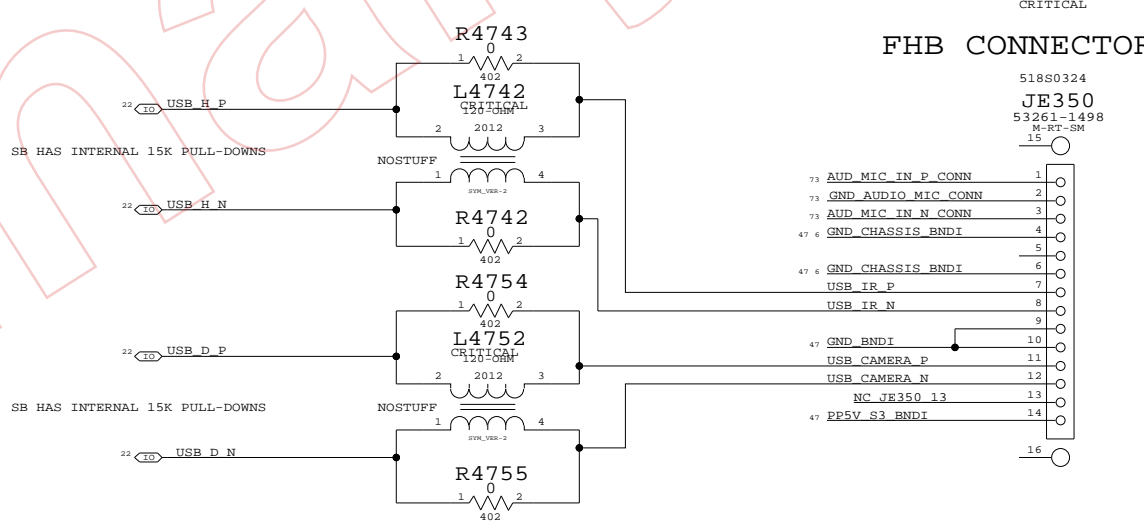
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET 46	OF 111

External USB Ports



LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE350.



NOTE: STANDOFFS FOR J4700
SDF4700
STDOFF-40D4.5H-1.35-TH
SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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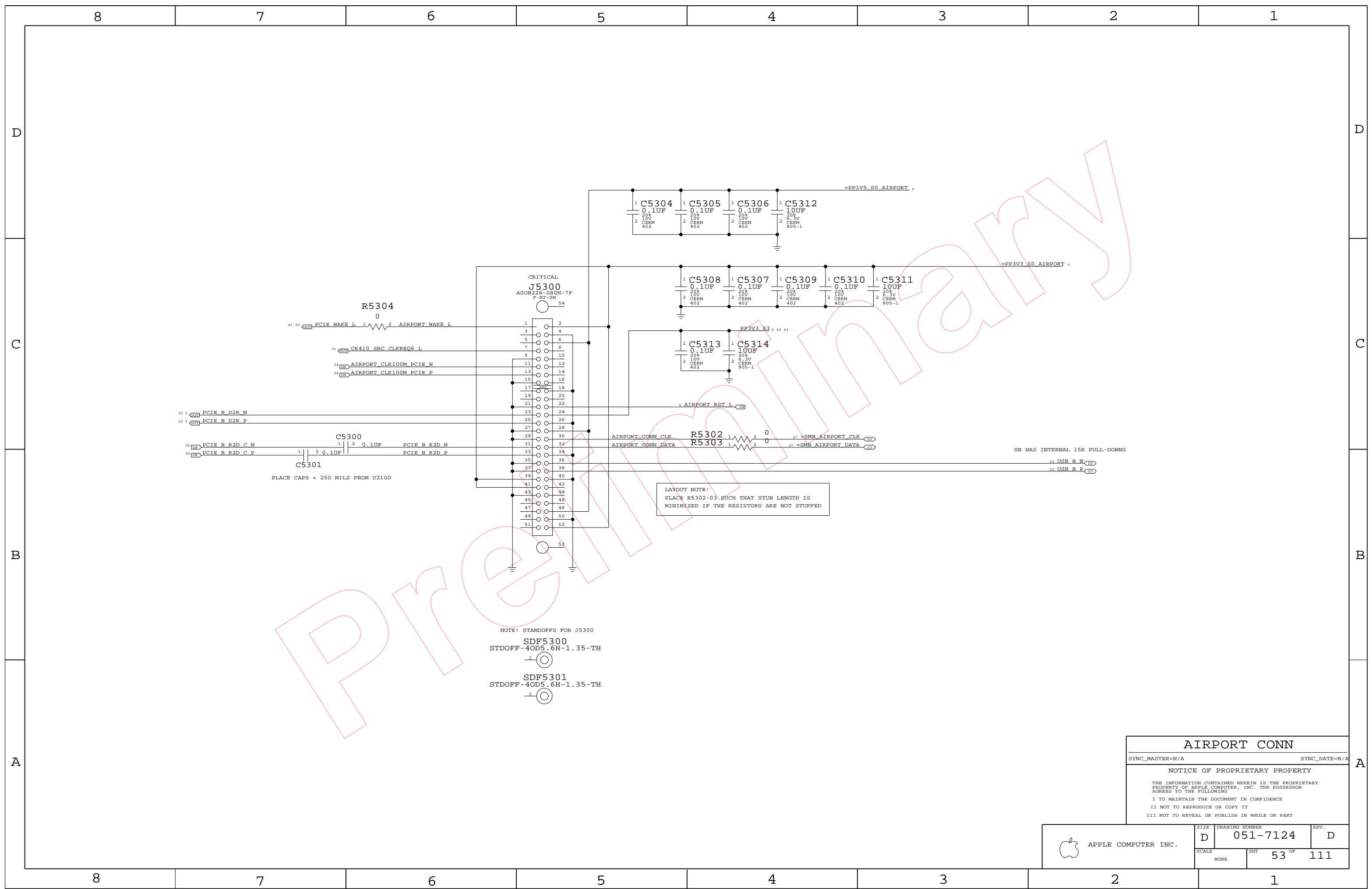
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0355	3	USB RECEPTACLE, 4P, RIBLESS	JE310, JE320, JE330	CRITICAL	20_INCH_LCD

APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	47	111	D



AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET 53 OF 111	

8

7

6

5

4

3

2

1

D

D

C


C


B


B


A


A


22  PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE


22  PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE


22  PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE


22  PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE


22  PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE


22  PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE


22  PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE


22  PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE


22  PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE


22  PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE


22  PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22  PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22  PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22  PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22  PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22  PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

Preliminary

8

7

6

5

4

3

2

1

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A


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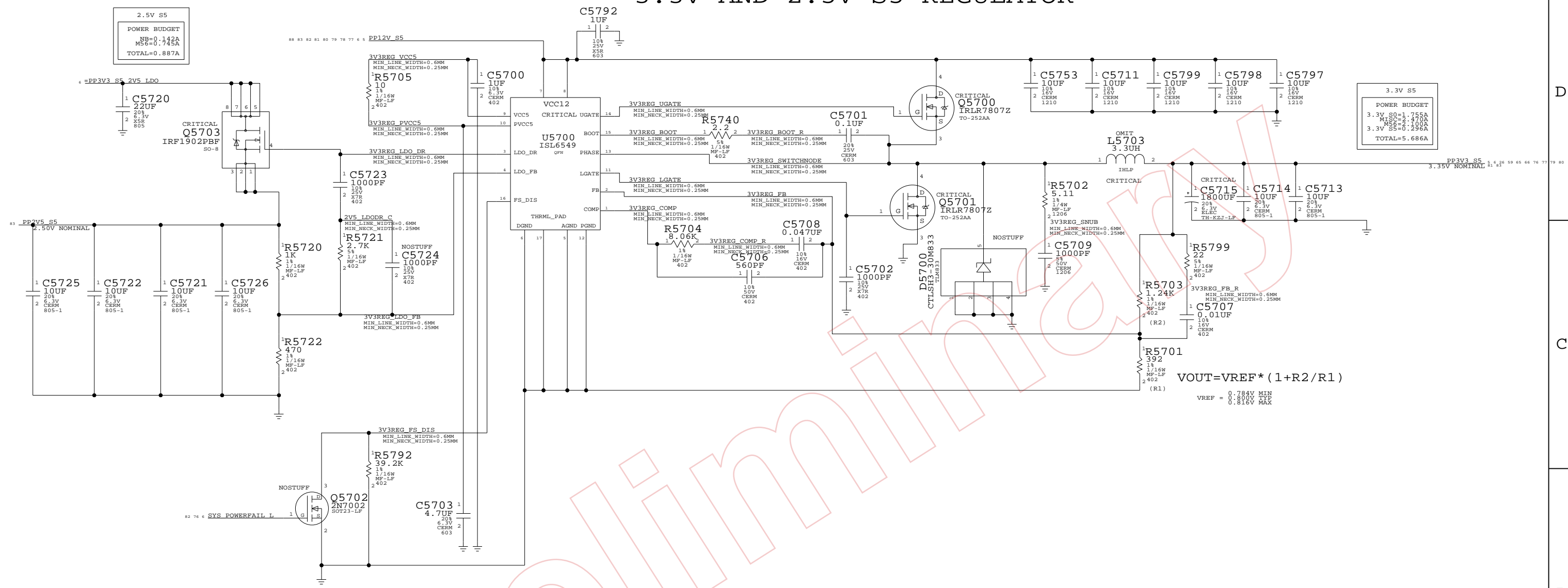
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	54	111	

3.3V AND 2.5V S5 REGULATOR

2.5V S5
POWER BUDGET
 NB=0.142A
 MS6=0.745A
 TOTAL=0.887A

3.3V S5
POWER BUDGET
 3.3V S0=1.755A
 MS0=2.470A
 MS6=2.100A
 TOTAL=5.686A



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

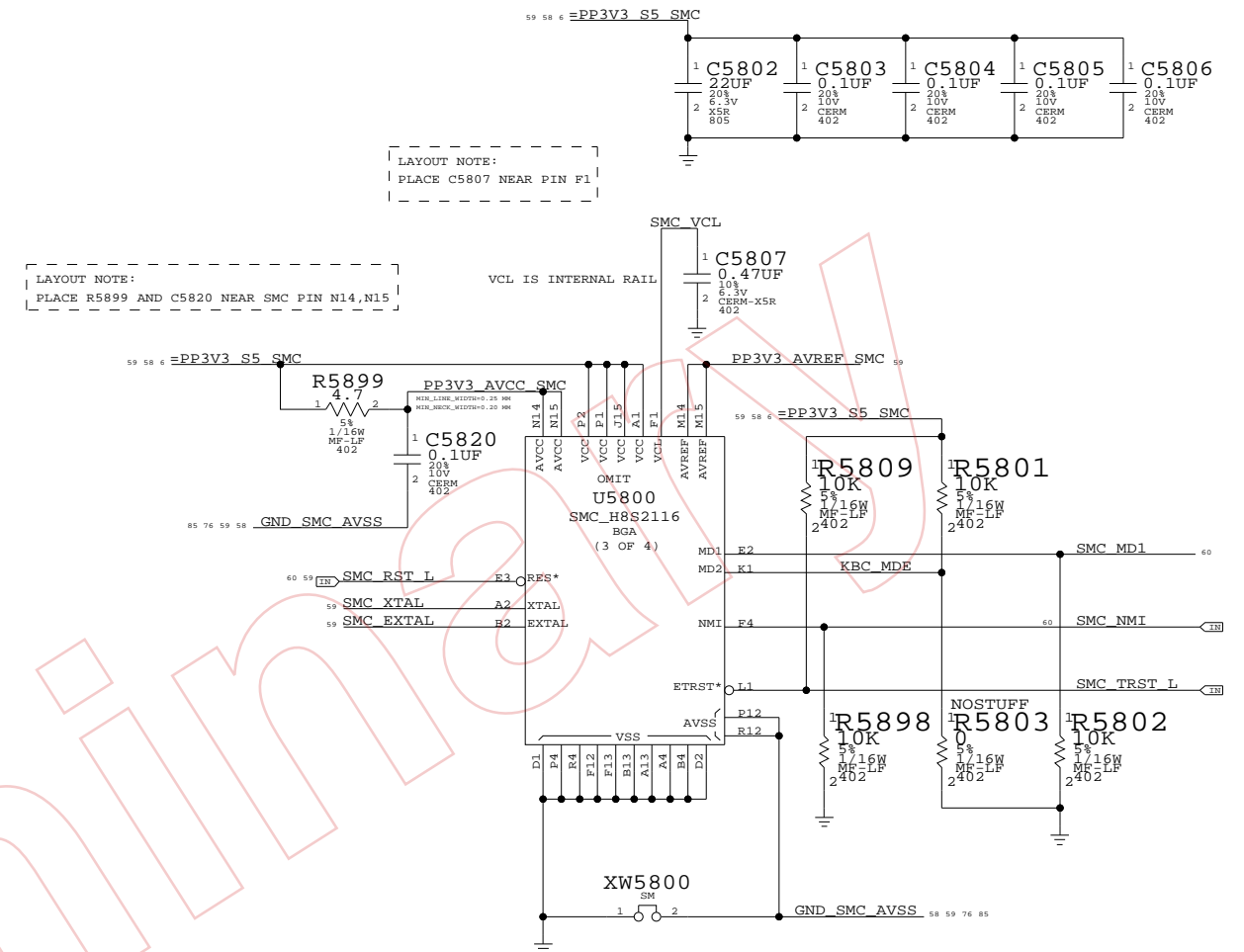
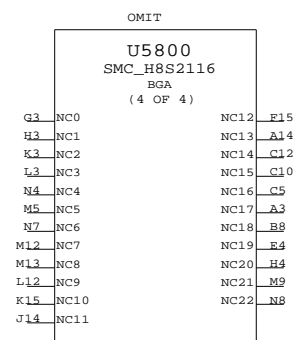
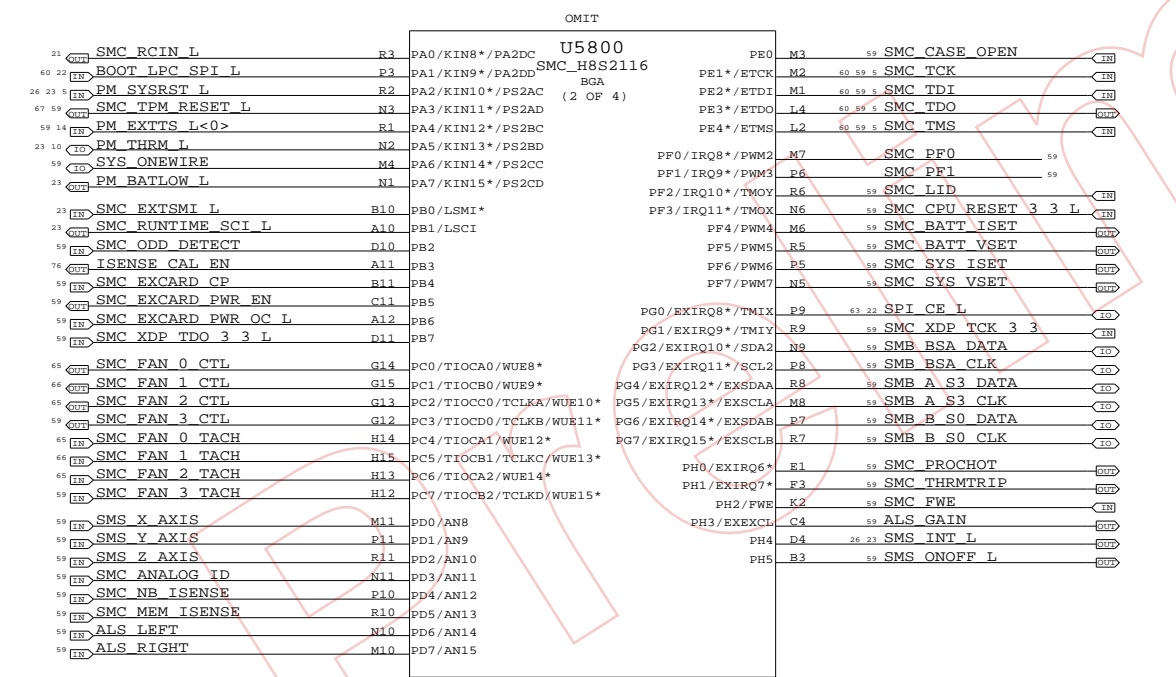
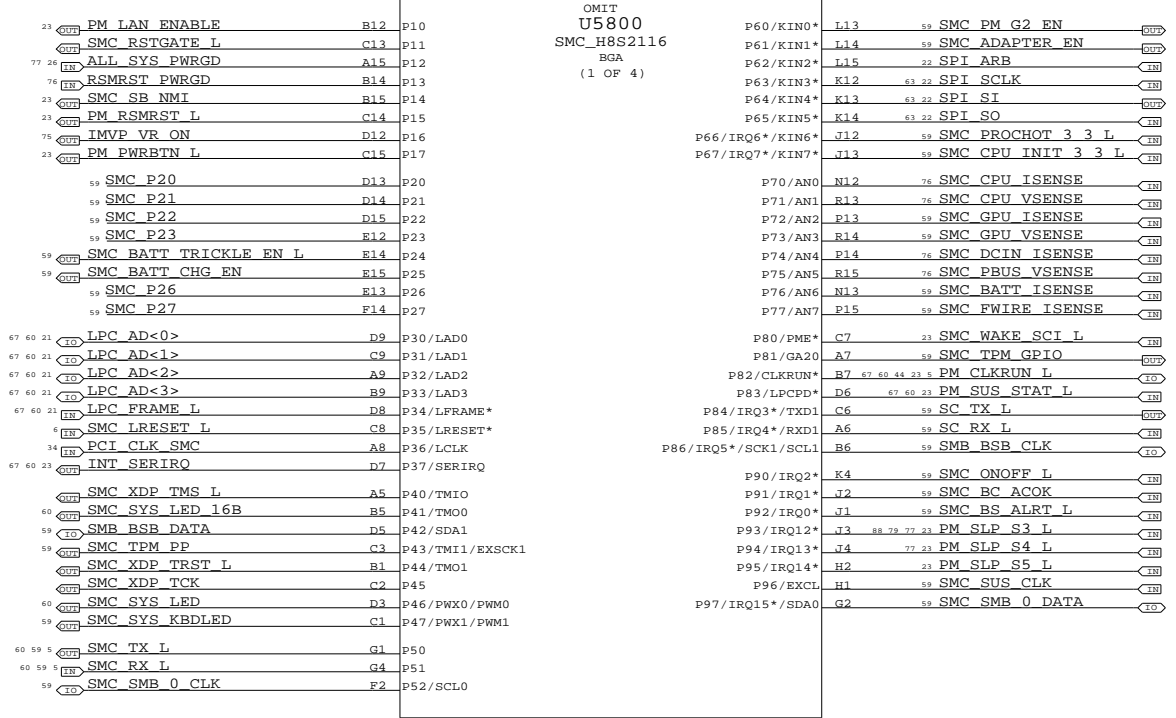
VREF = 0.784V MIN
 0.800V TYP
 0.816V MAX

3.3V DC/DC 2.5V

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	57 OF	111
NONE			

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

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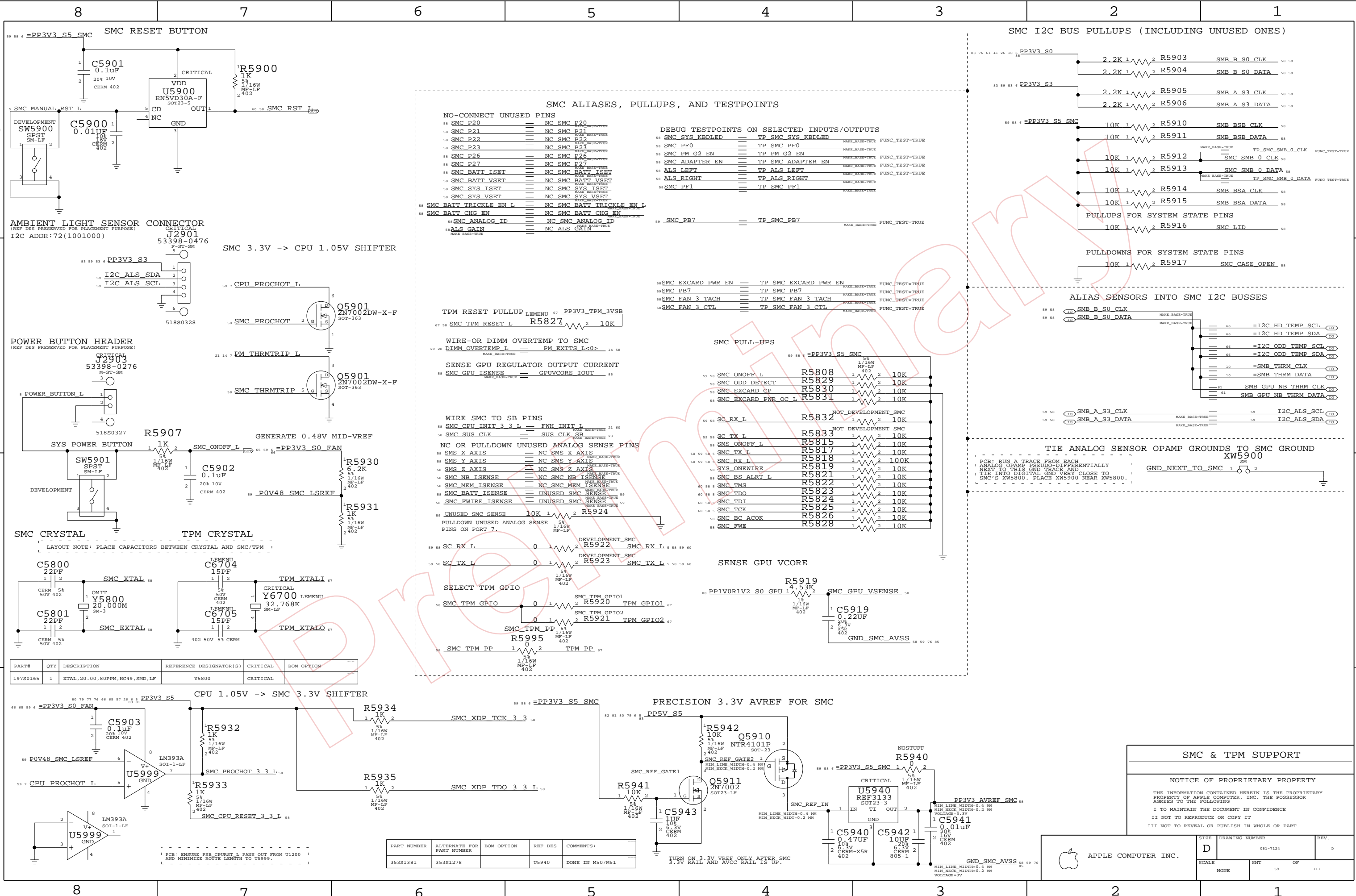
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7124 REV. D

SCALE NONE SHEET 58 OF 111



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S1381	353S1278		U5940	DONE IN M50/M51

SMC & TPM SUPPORT

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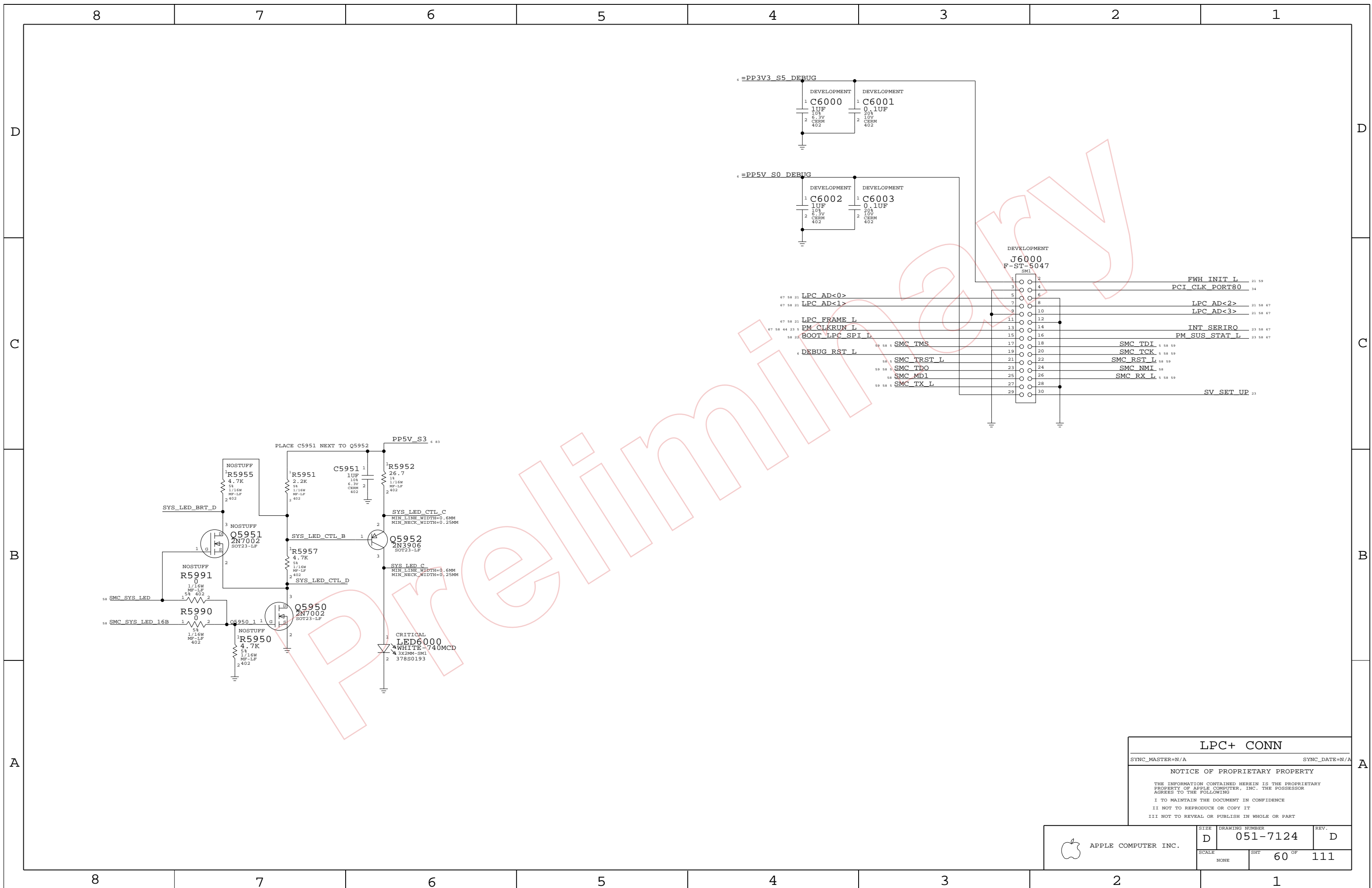
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-7124	D
SCALE	SHT	OF
NONE	59	111

1 PCB: ENSURE FSB_CPUREST_L PINS OUT FROM U1200 AND MINIMIZE ROUTER LENGTH TO U5999.

2 PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

3 PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

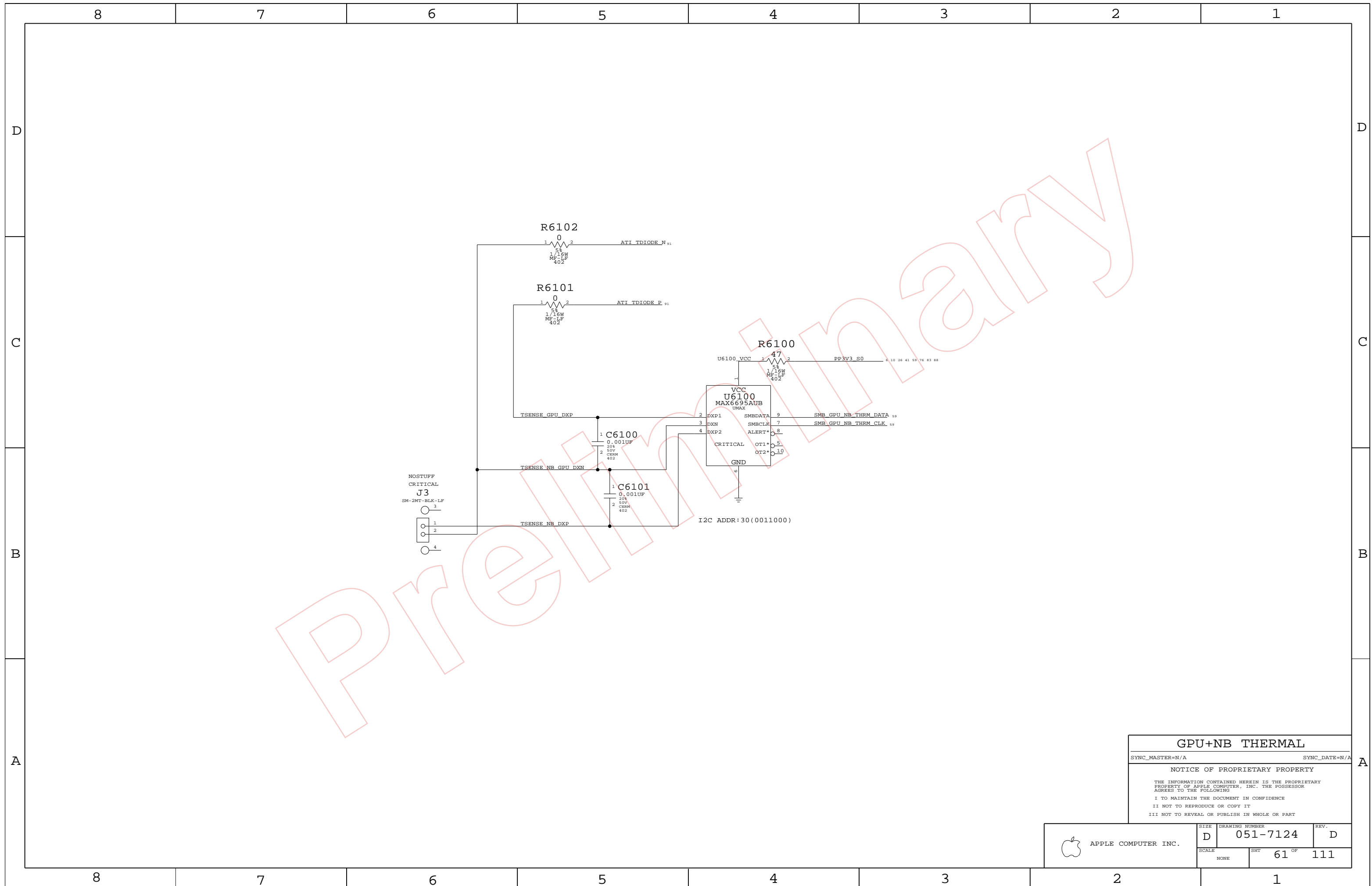
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	D	051-7124	D
SCALE	SHT	60 OF	111
NONE			



GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

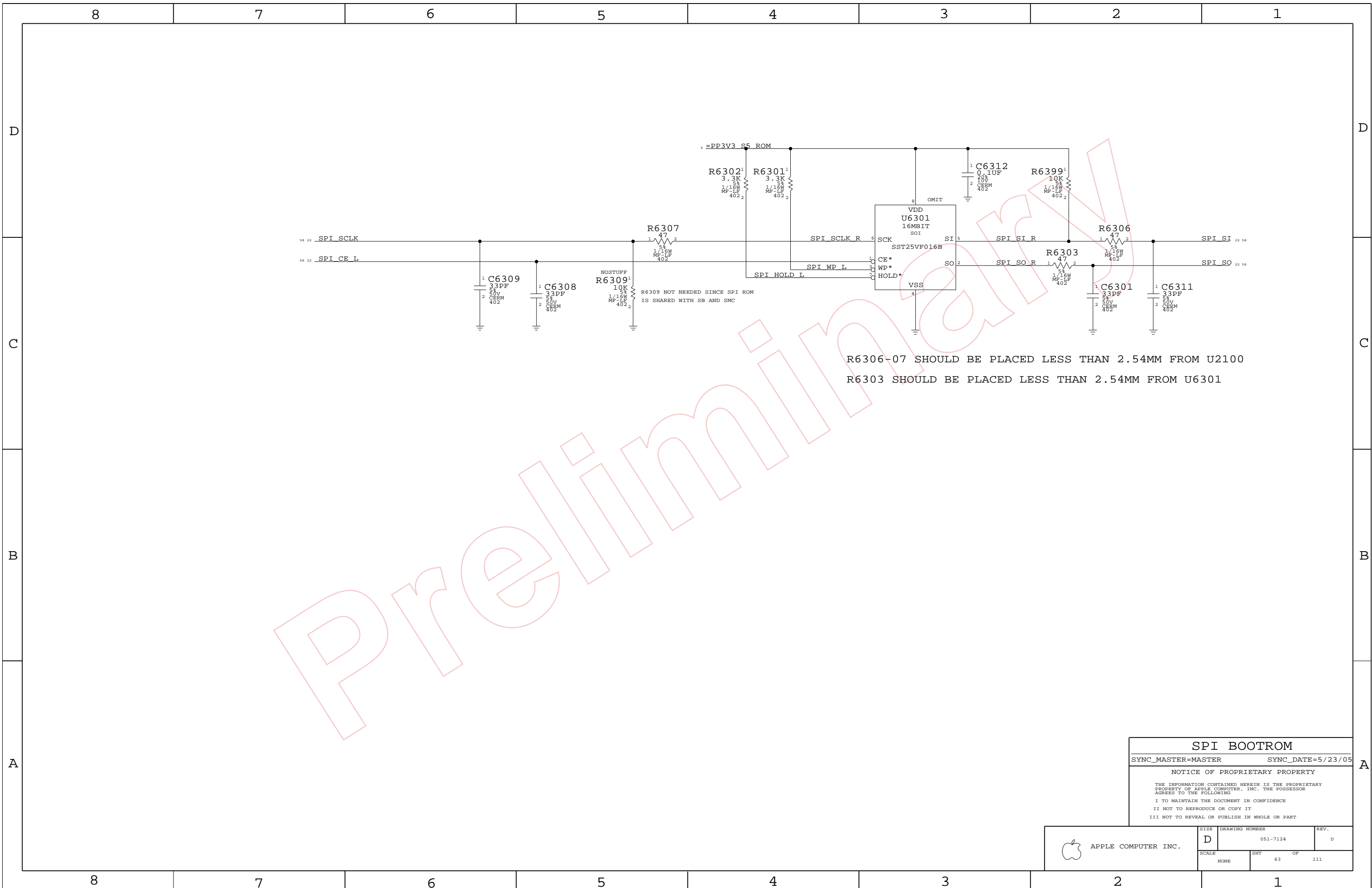
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET 61 OF 111	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

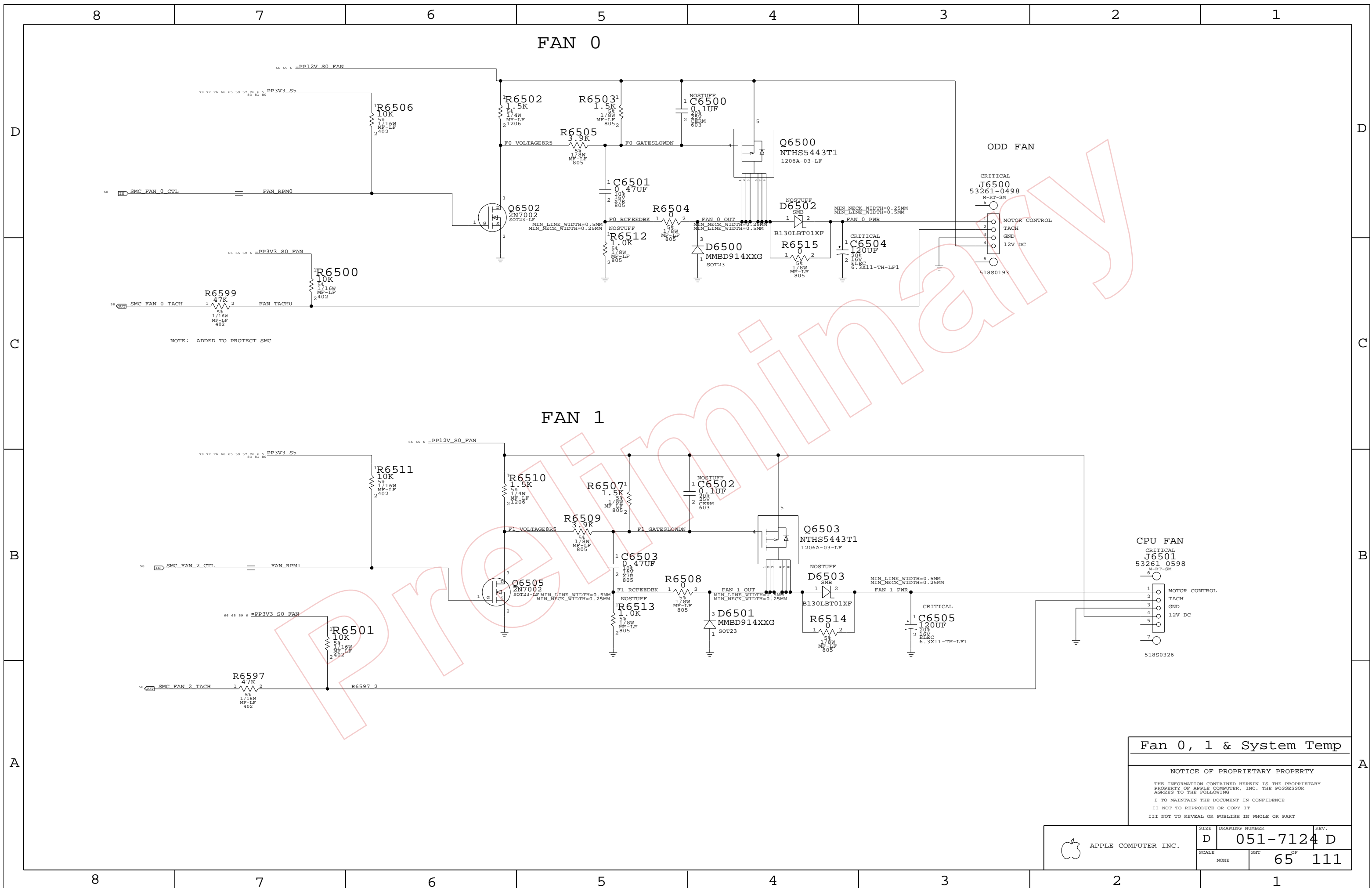
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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	D	051-7124	D
SCALE	SHT	OF	REV.
NONE	63	111	



FAN 0

FAN 1

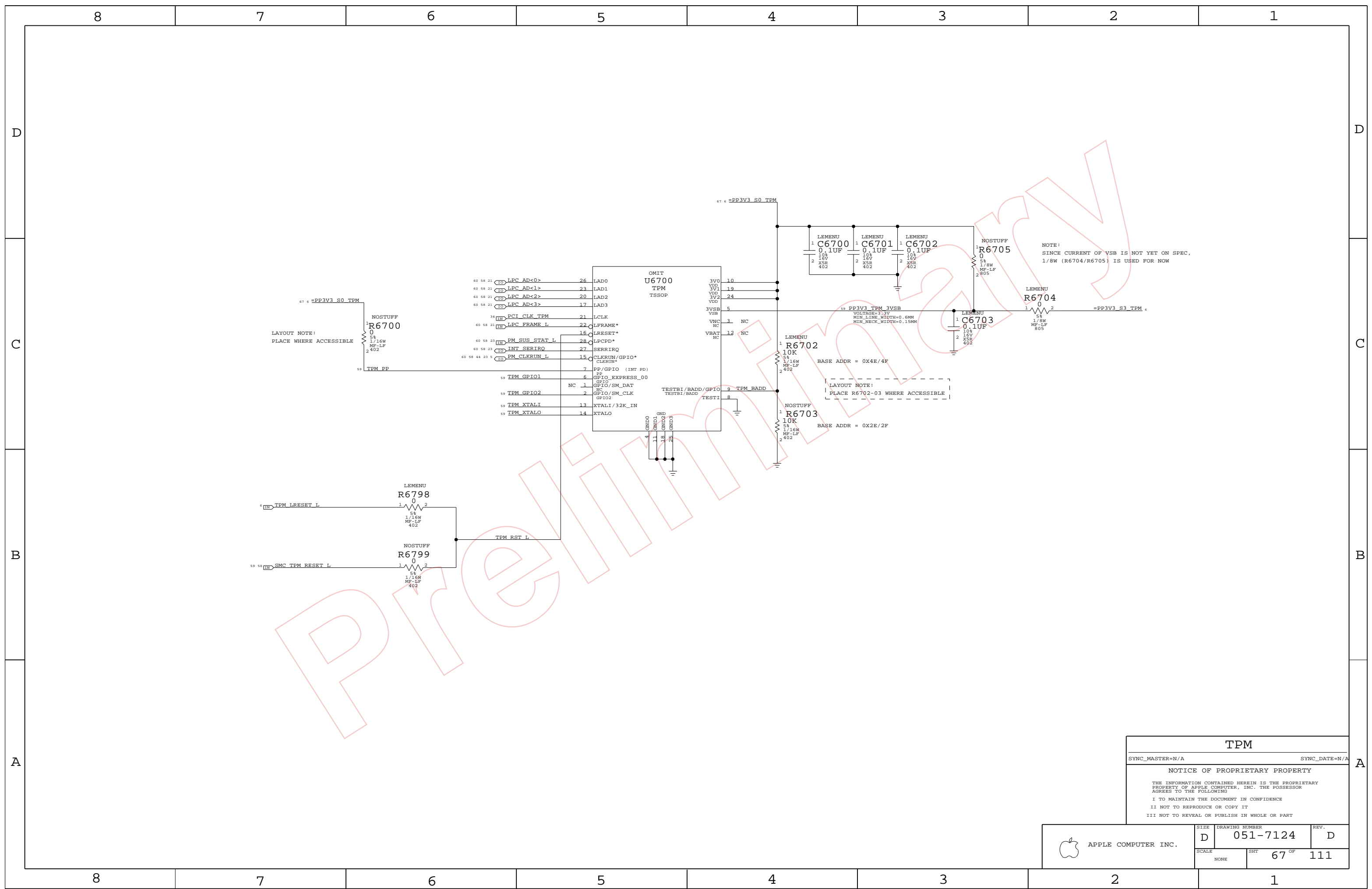
ODD FAN

CPU FAN

Fan 0, 1 & System Temp

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	NONE	051-7124 D	D
SCALE		SHT	OF
NONE		65	111



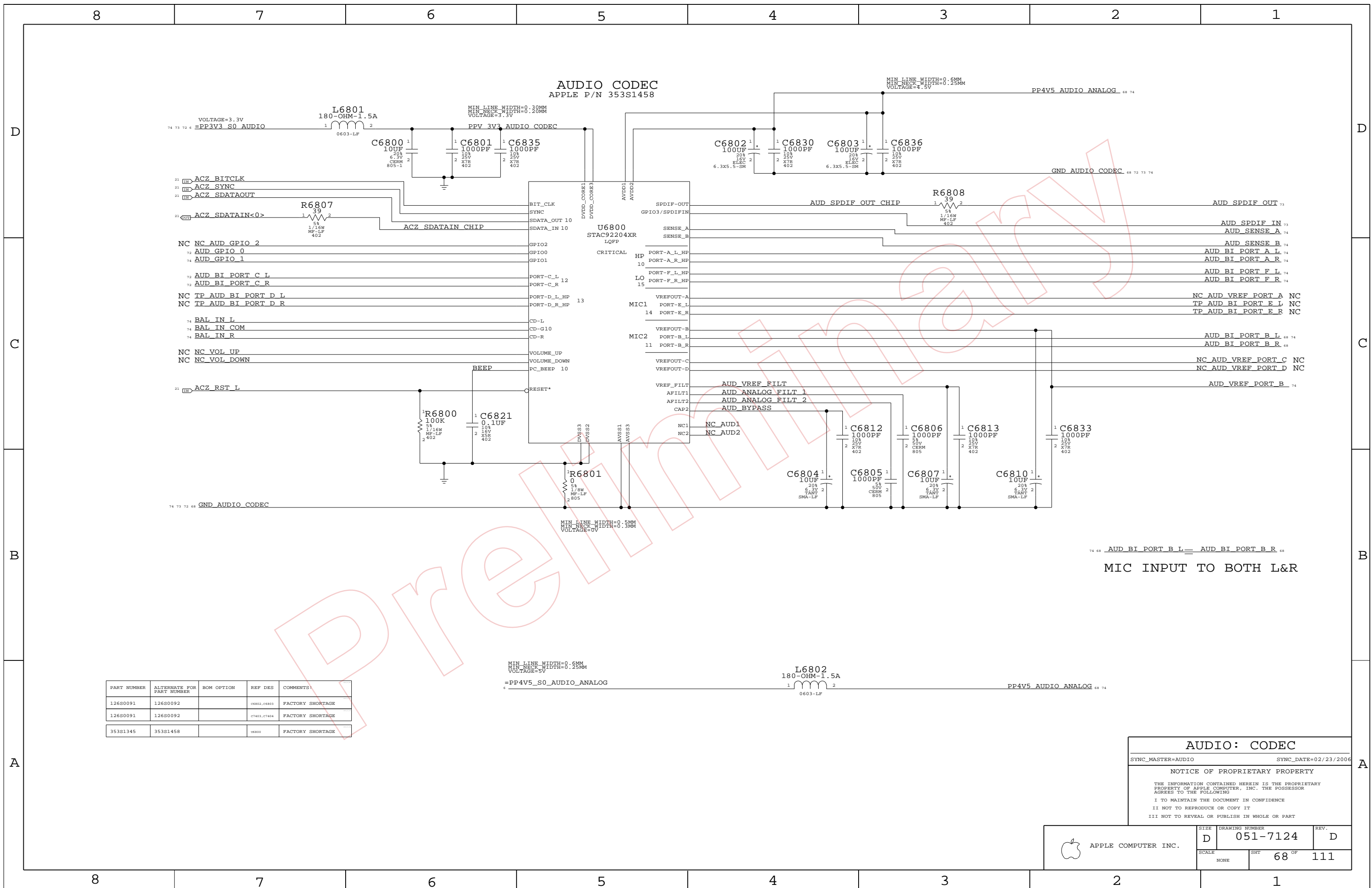
LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	67 OF	111
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C802,C803	FACTORY SHORTAGE
126S0091	126S0092		C7403,C7404	FACTORY SHORTAGE
353S1345	353S1458		U6800	FACTORY SHORTAGE

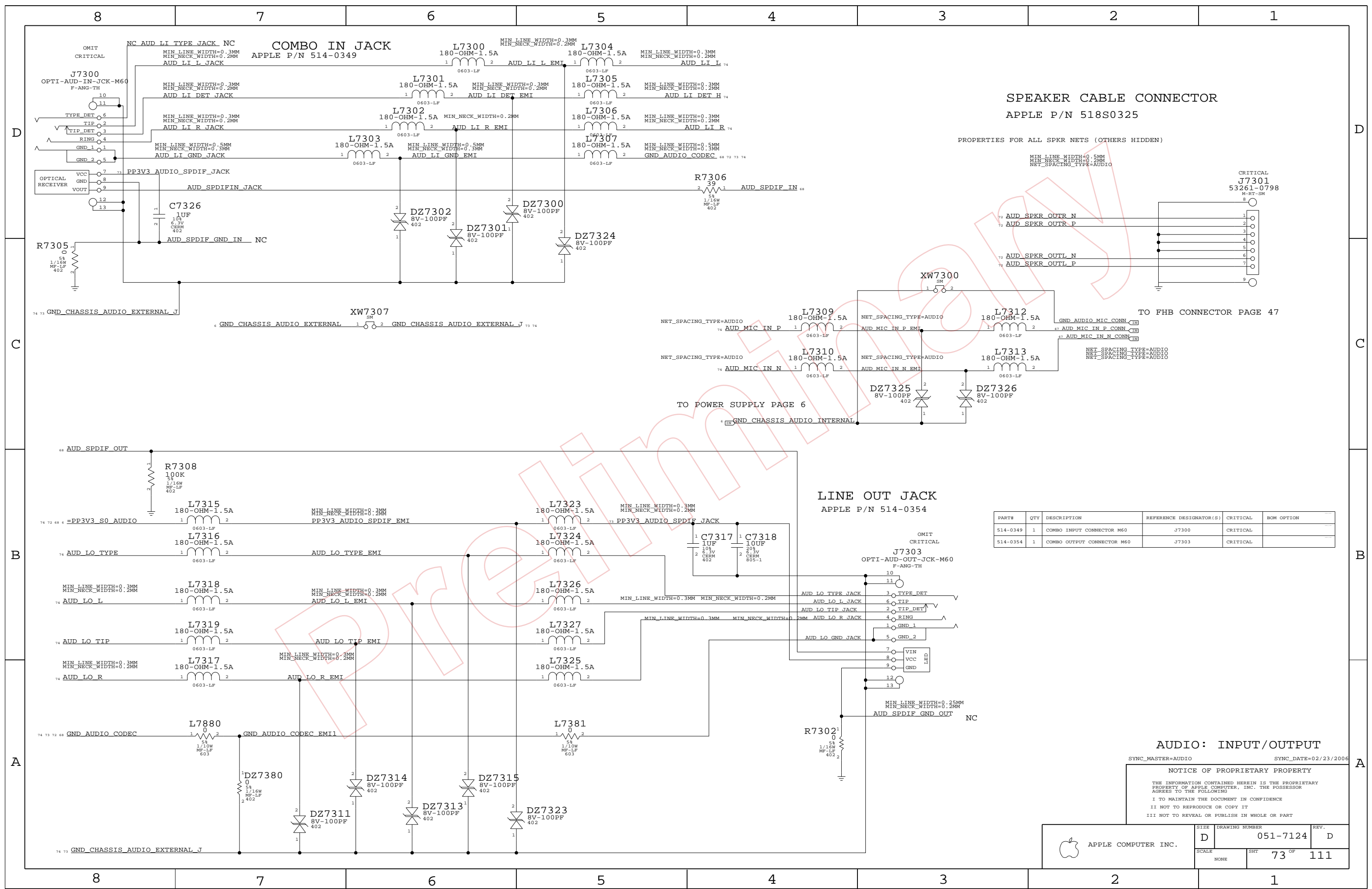
MIN LINE WIDTH=0.6MM
 MIN NECK WIDTH=0.25MM
 VOLTAGE=5V
 =PP4V5_S0_AUDIO_ANALOG

L6802
 180-OHM-1.5A
 0603-LF

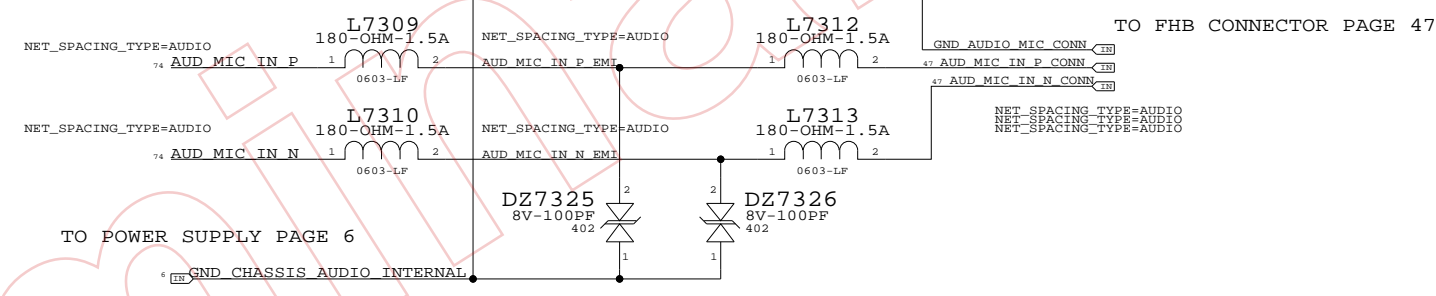
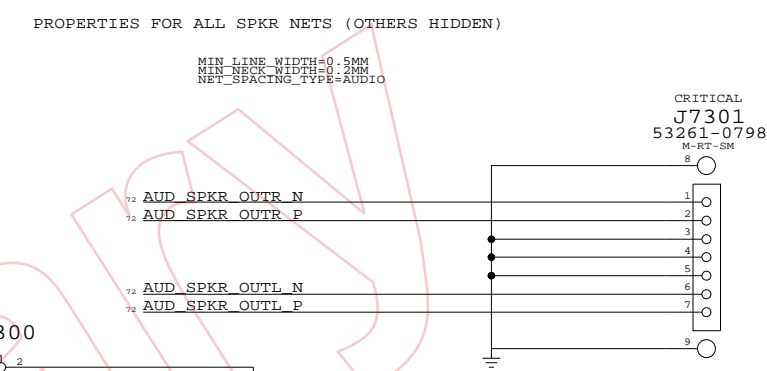
74 68 AUD BI PORT B L = AUD BI PORT B R 68
 MIC INPUT TO BOTH L&R

AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	68 OF	111
NONE			



SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



LINE OUT JACK
APPLE P/N 514-0354

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0349	1	COMBO INPUT CONNECTOR M60	J7300	CRITICAL	
514-0354	1	COMBO OUTPUT CONNECTOR M60	J7303	CRITICAL	

AUDIO: INPUT/OUTPUT

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

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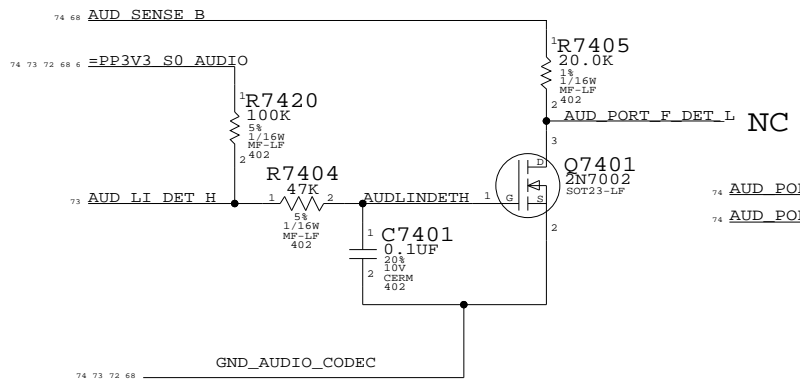
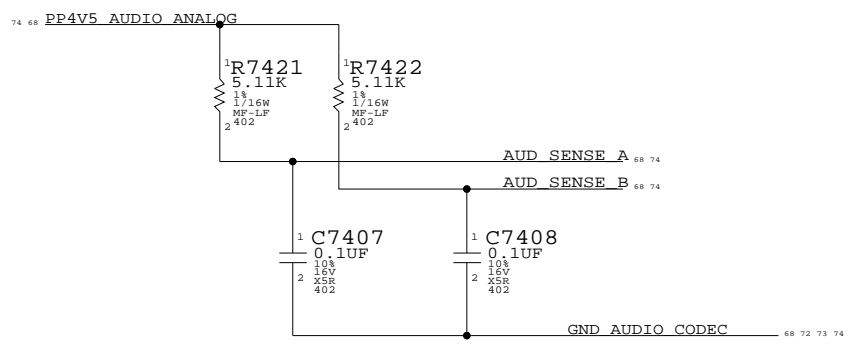
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

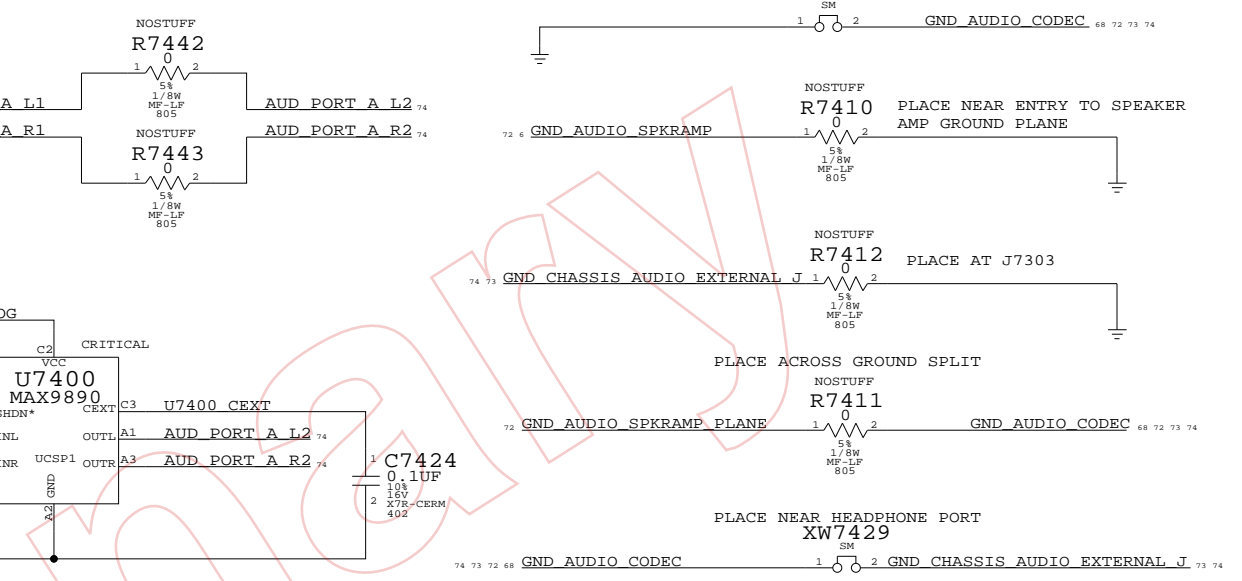
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	73 OF	111
NONE			

PORT F (LI) PLUG DETECT AUDIO GROUND RETURNS

JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



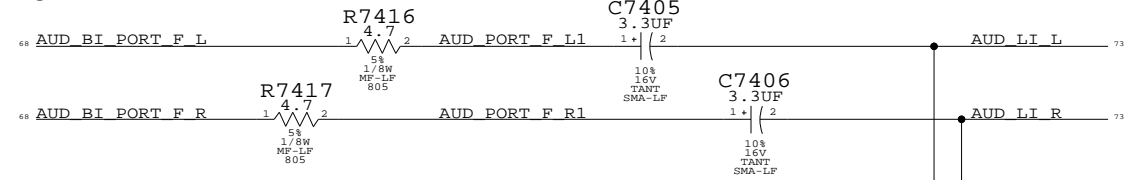
AUDIO GROUND RETURNS



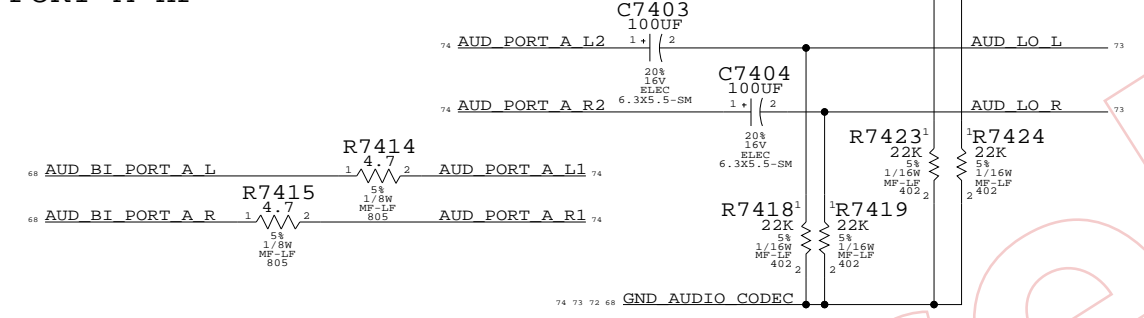
USED PORTS
 PORT A HP
 PORT B MIC IN VREF =80%
 PORT C BI SPEAKERS
 PORT F LI

UNUSED PORTS
 PORT E DETECT DELEGATE
 PORT D

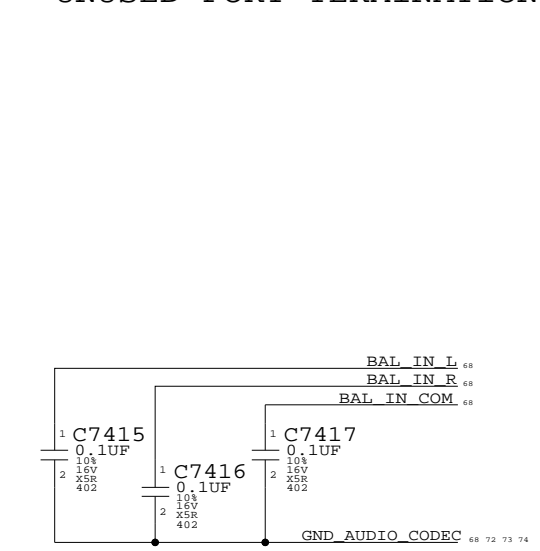
PORT F LI



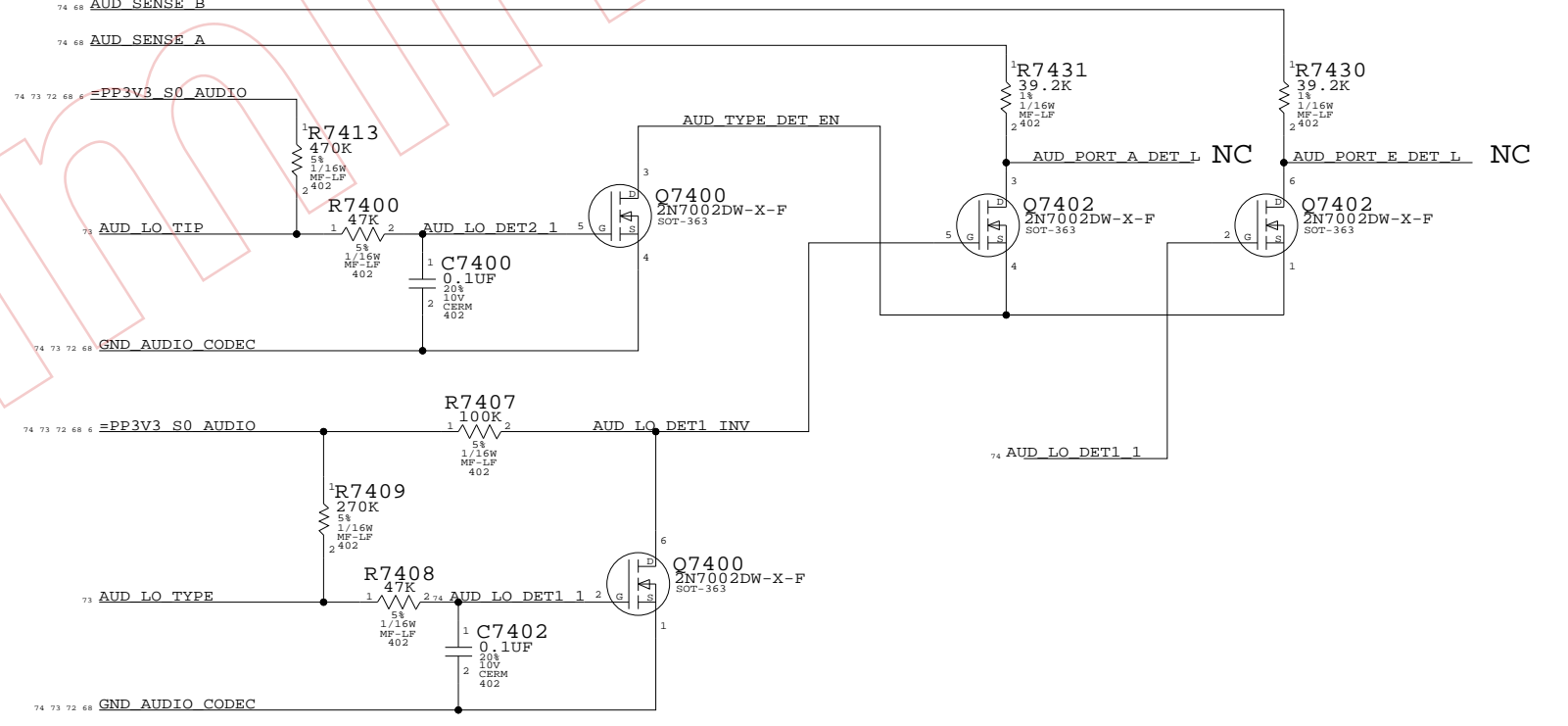
PORT A HP



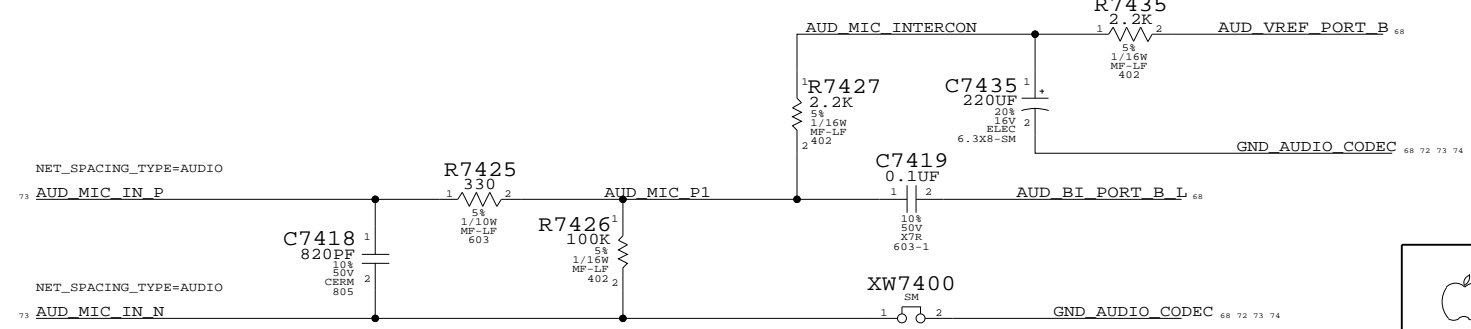
UNUSED PORT TERMINATION



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

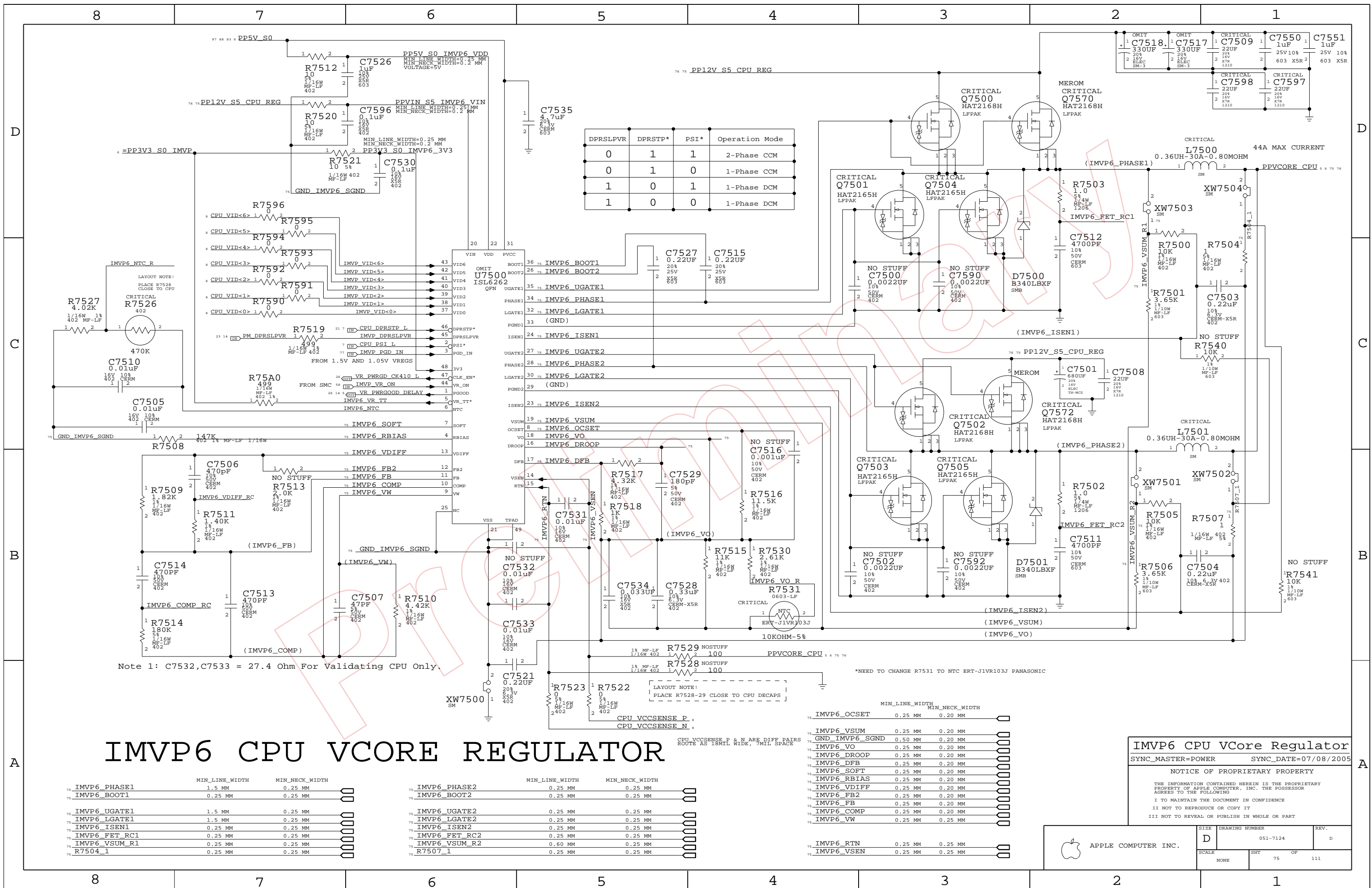


MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: JACK DETECT
 SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006
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	D	051-7124	D
SCALE	SHT	74 OF	111
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

IMVP6_OCSET	IMVP6_VSUM	IMVP6_VO	IMVP6_DROOP	IMVP6_DFB	IMVP6_VSEN	IMVP6_VSEN1	IMVP6_VSEN2	IMVP6_VSUM_R1	IMVP6_VSUM_R2	IMVP6_FET_RC1	IMVP6_FET_RC2	IMVP6_PHASE1	IMVP6_PHASE2
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHEET	OF	111
NONE	75		

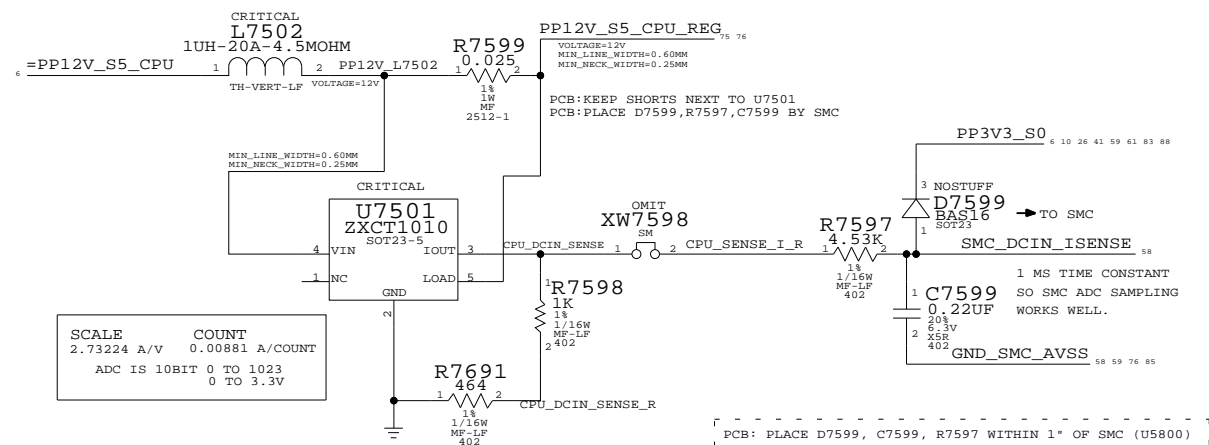
Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

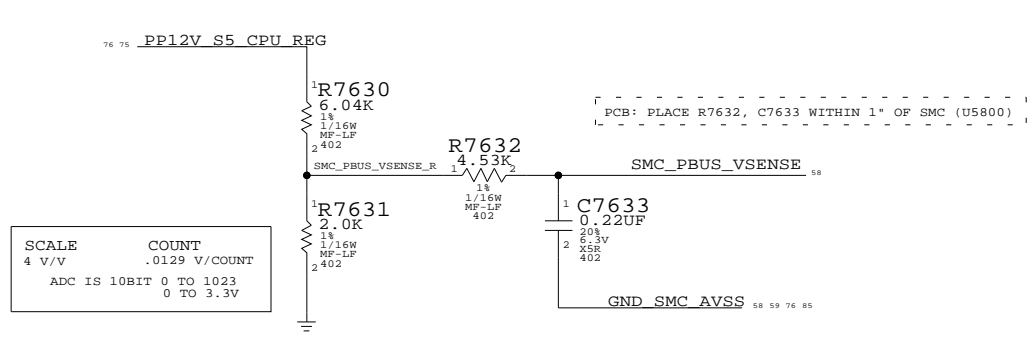
LAYOUT NOTE:
PLACE R7528-29 CLOSE TO CPU DECAPS

CPU VCCSENSE P & N ARE DIFF PAIRS
ROUTE AS 18MIL WIDE, 7MIL SPACE

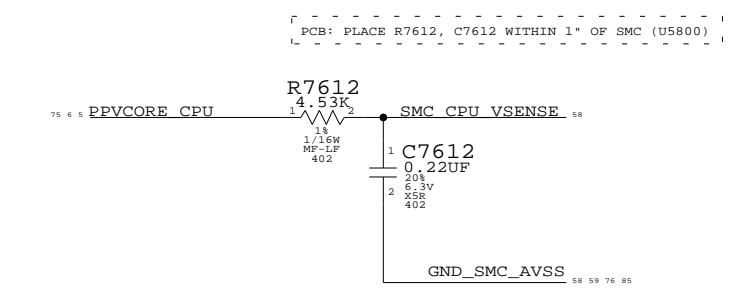
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



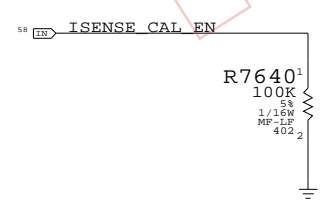
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



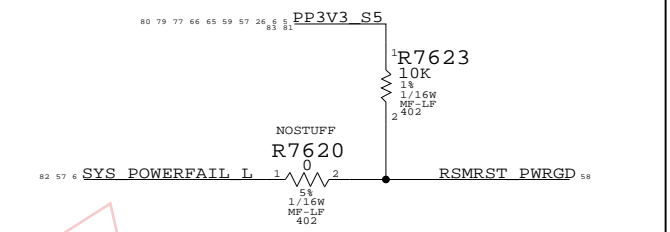
PROCESSOR VCORE SENSE



Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



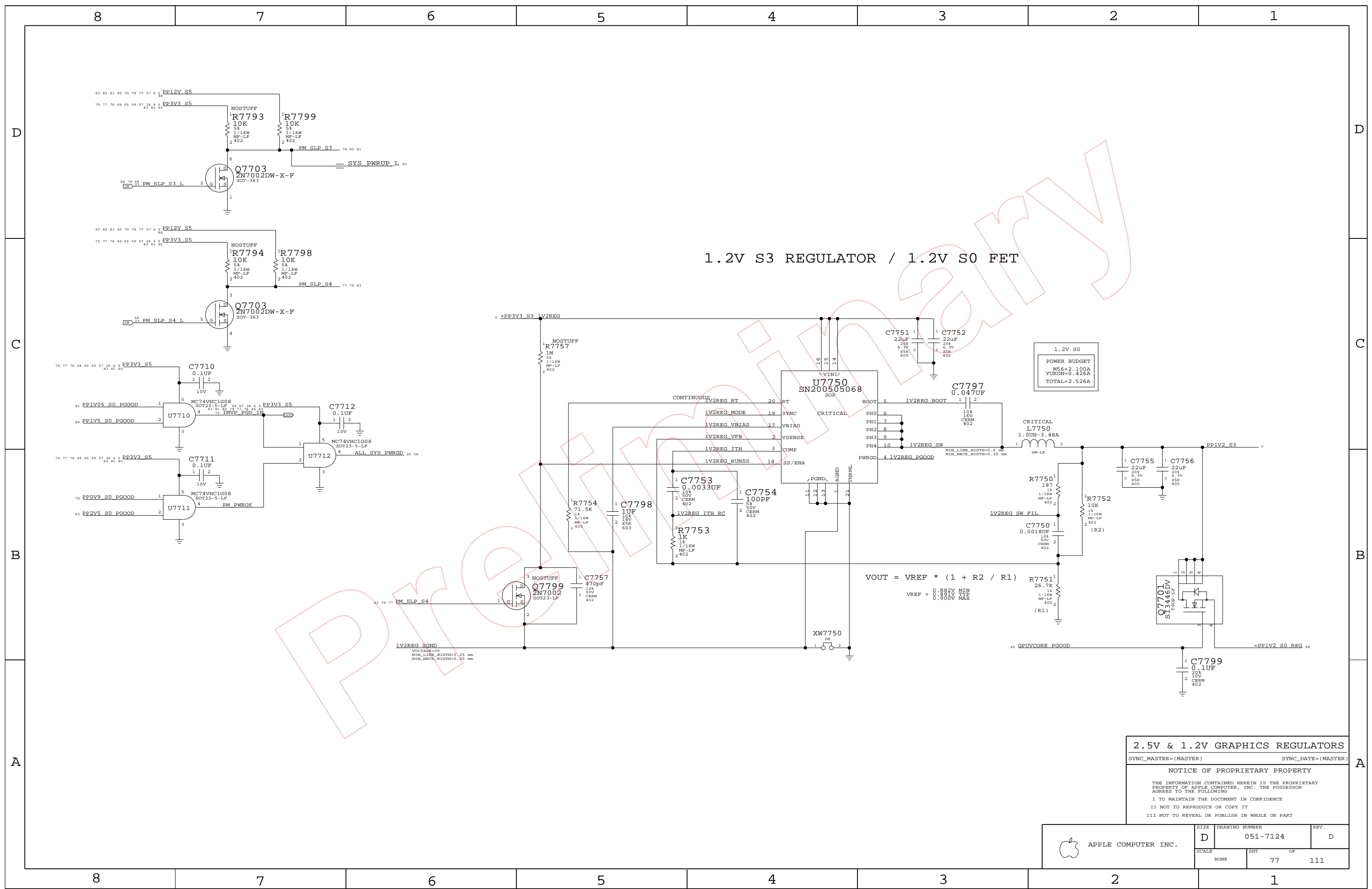
SMC PWRGD PULLUP



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	76 OF	111
NONE			



1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S0
POWER BUDGET
M56=2.100A
YUKON=0.426A
TOTAL=2.526A

$$V_{OUT} = V_{REF} * (1 + R2 / R1)$$

$$V_{REF} = 0.82V \text{ MIN}$$

$$V_{REF} = 0.91V \text{ TYP}$$

$$V_{REF} = 0.90V \text{ MAX}$$

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	77	111	

D

D

C

C

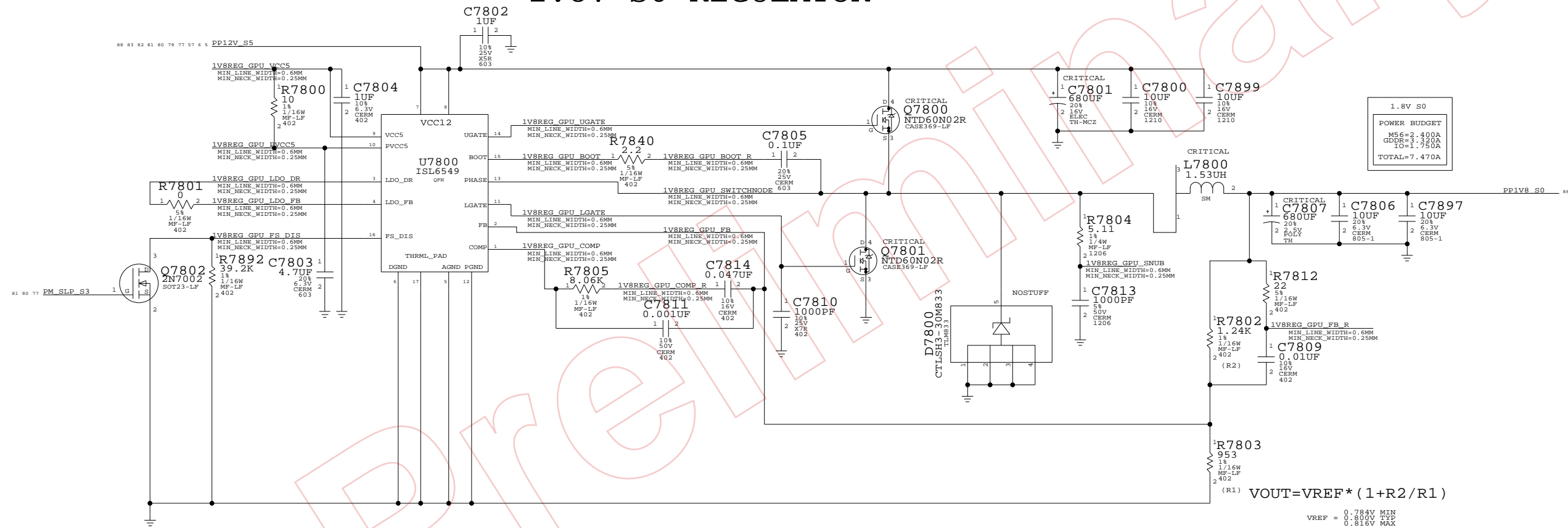
B

B

A

A

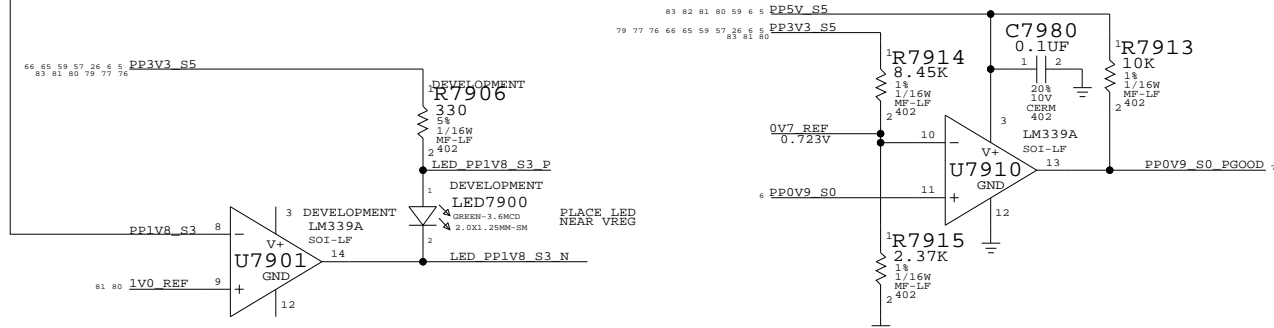
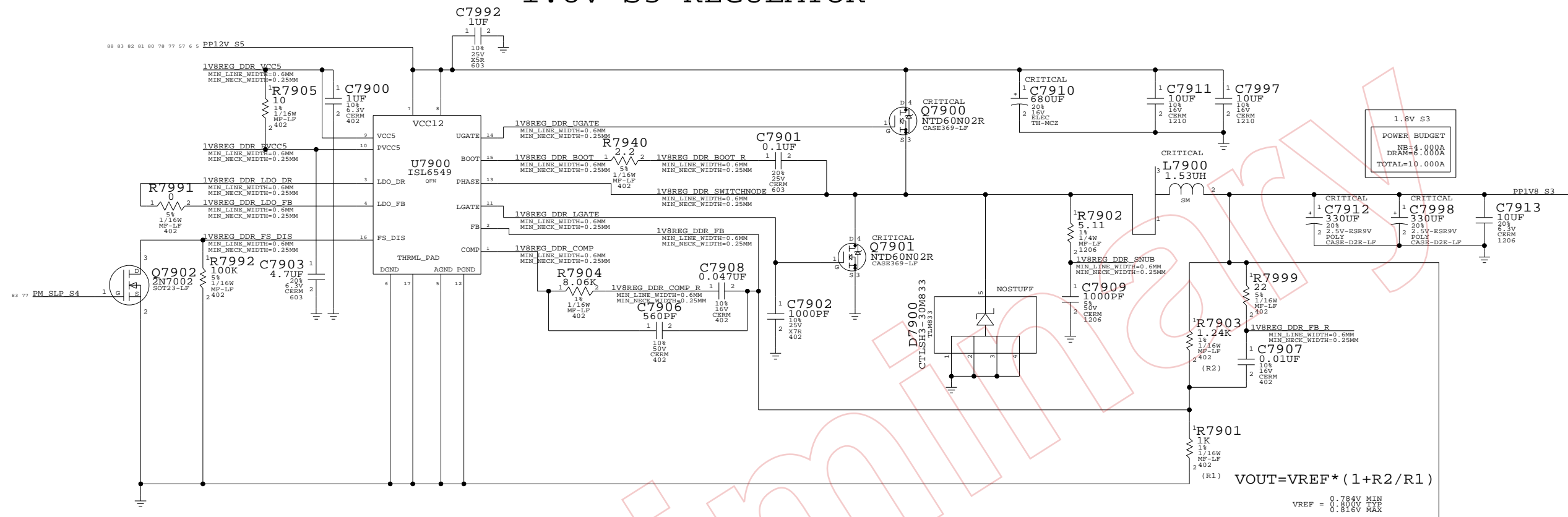
1.8V S0 REGULATOR



1.8V GDDR REGULATOR
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	78 OF	111
NONE			

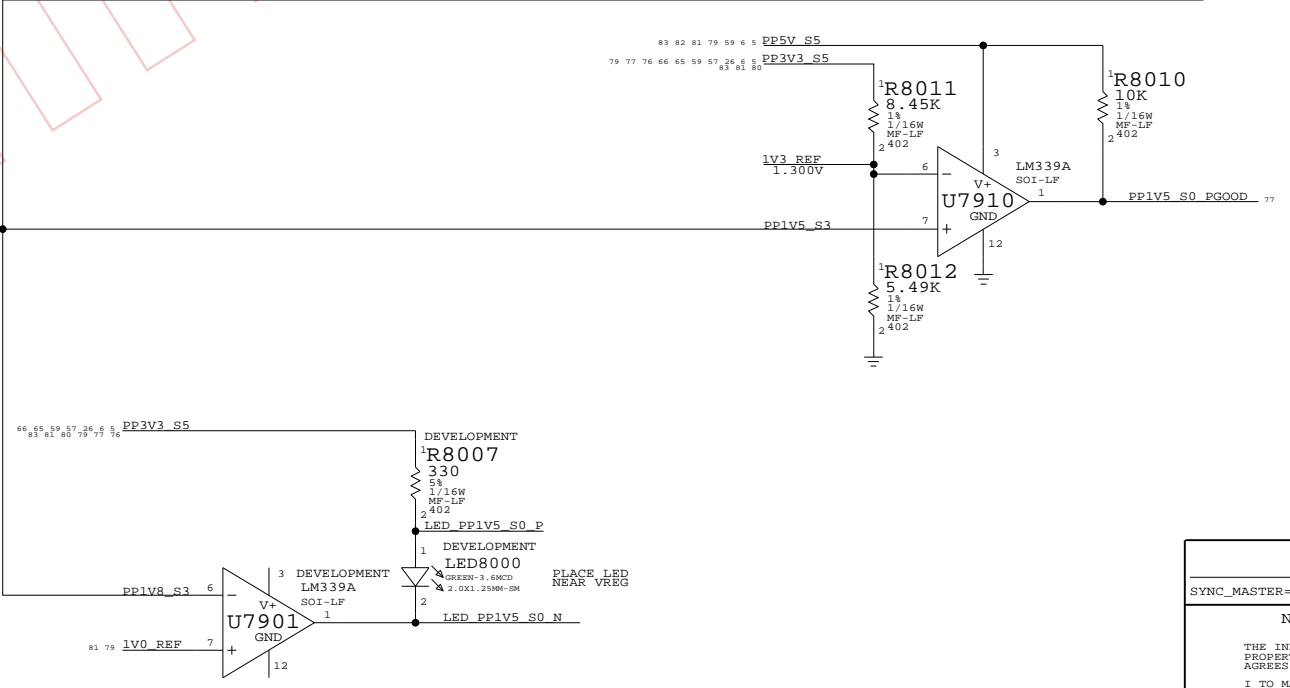
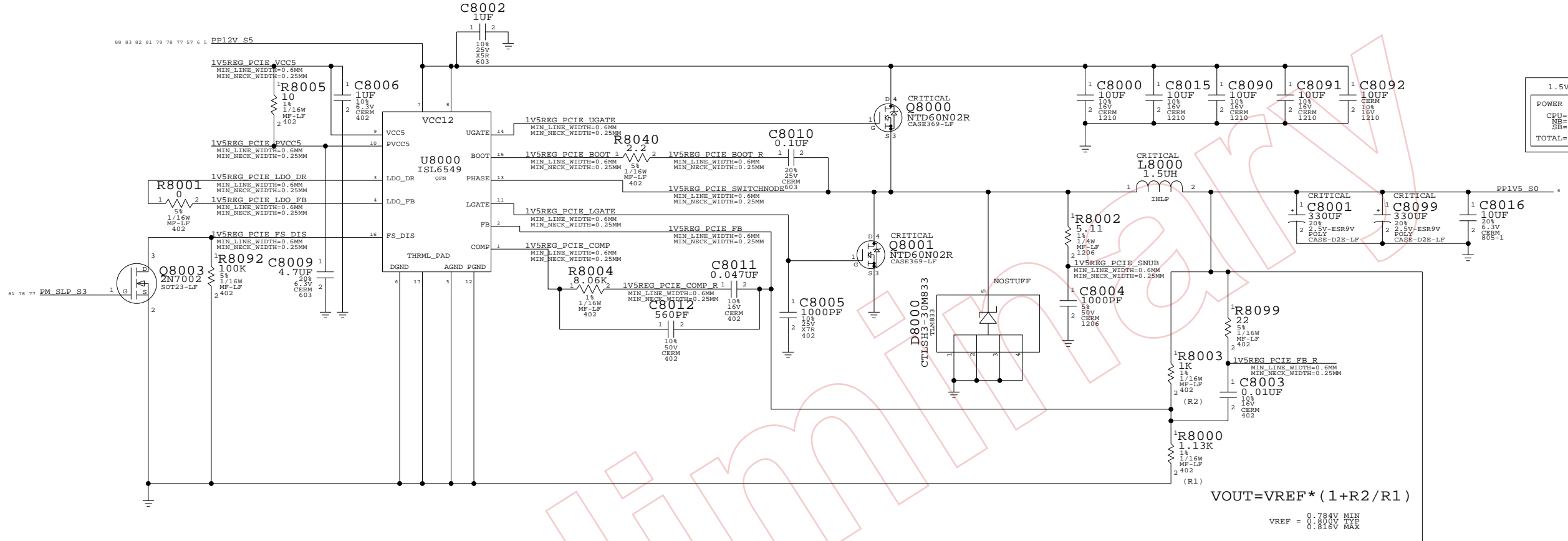
1.8V S3 REGULATOR



1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	79 OF	111
NONE			

1.5V S0 REGULATOR

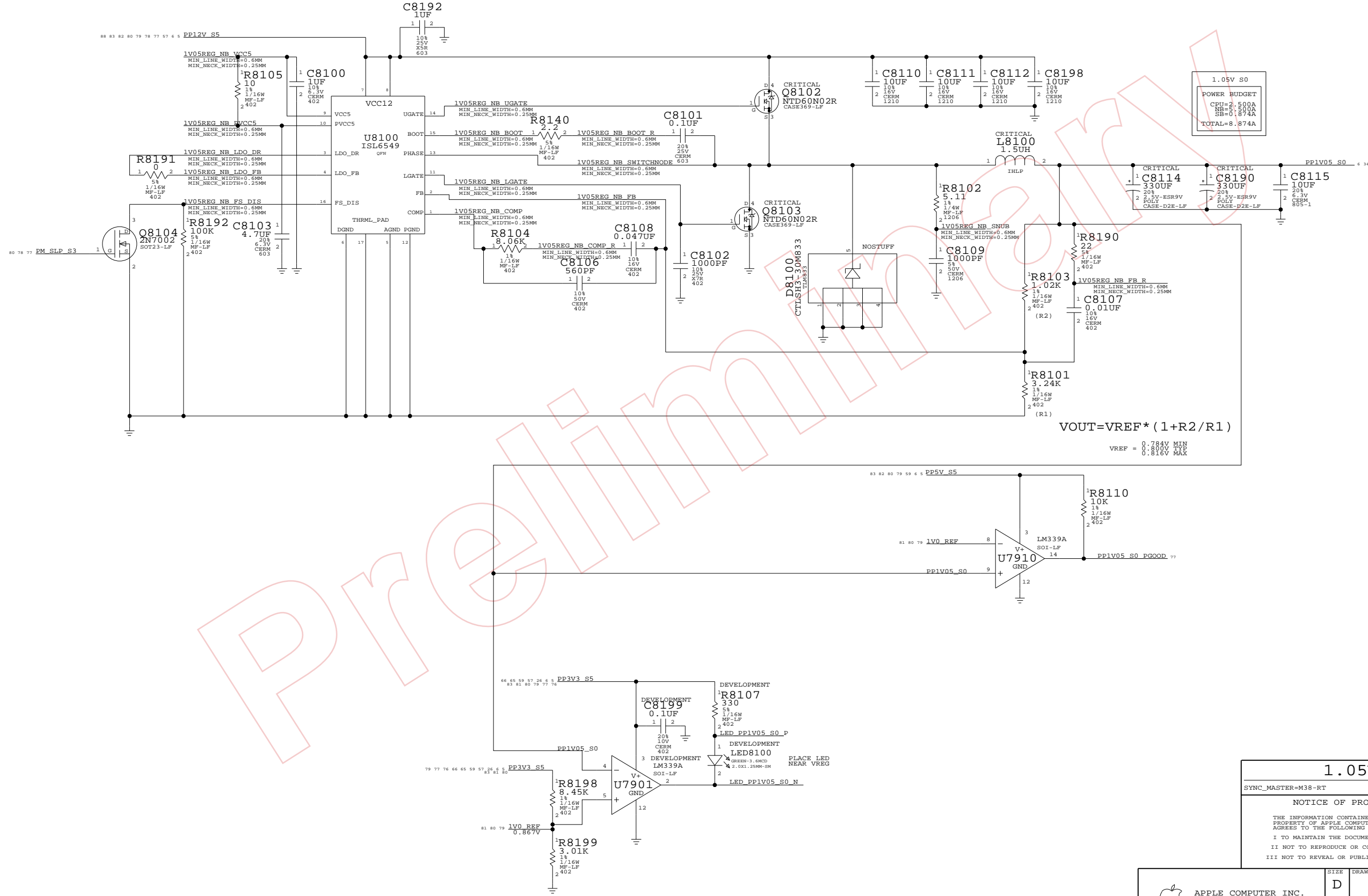


1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	80 OF	111
NONE			

1.05V S0 REGULATOR



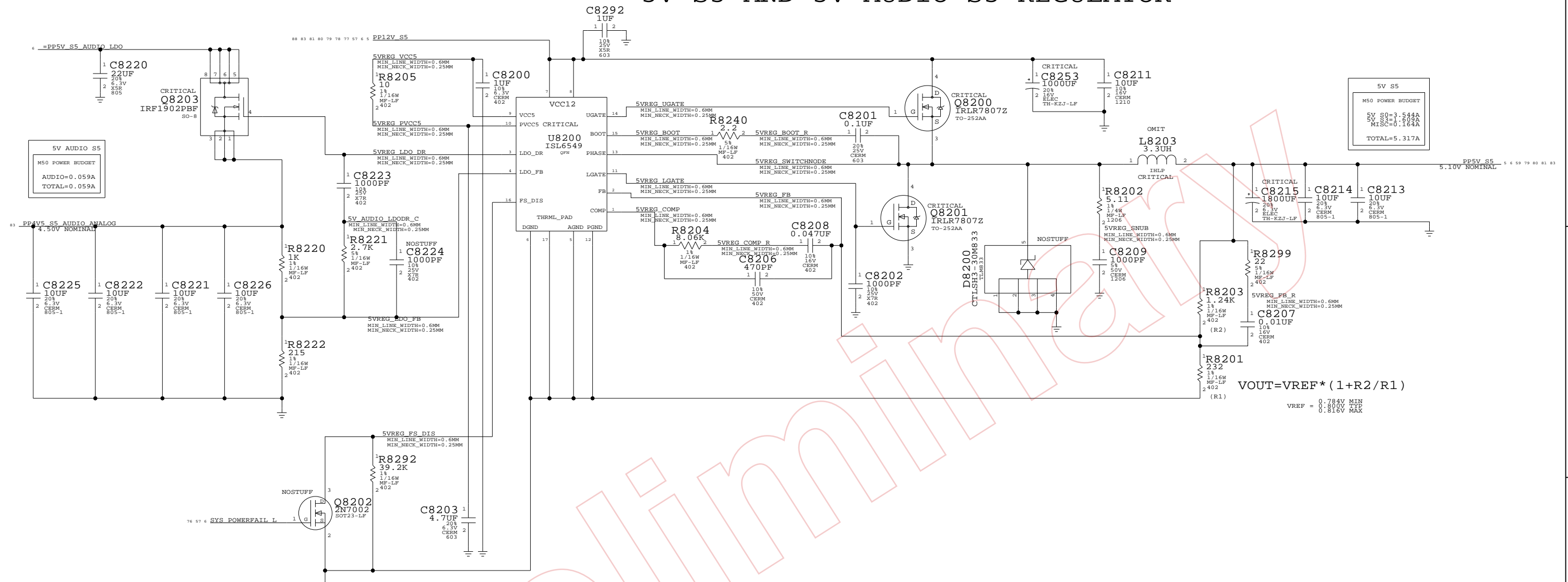
D
C
B
A

D
C
B
A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

5V S5 AND 5V AUDIO S5 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

5V S5	
M50 POWER BUDGET	
5V S5=3.544A	
5V S5=1.809A	
MISC=0.164A	
TOTAL=5.317A	

5V AUDIO S5	
M50 POWER BUDGET	
AUDIO=0.059A	
TOTAL=0.059A	

5V DC/DC 4.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

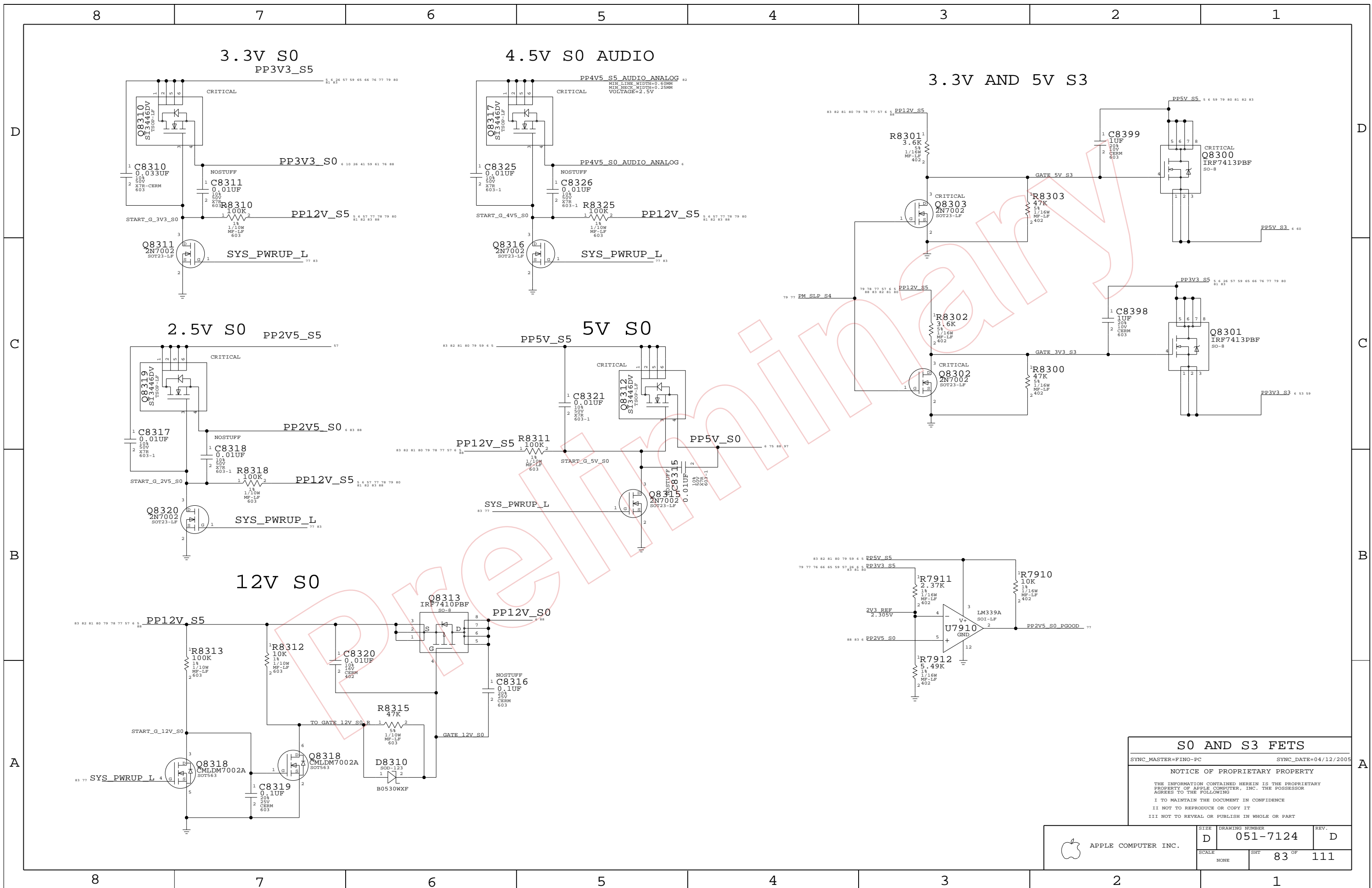
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	82 OF	111
NONE			



S0 AND S3 FETS

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

NOTICE OF PROPRIETARY PROPERTY

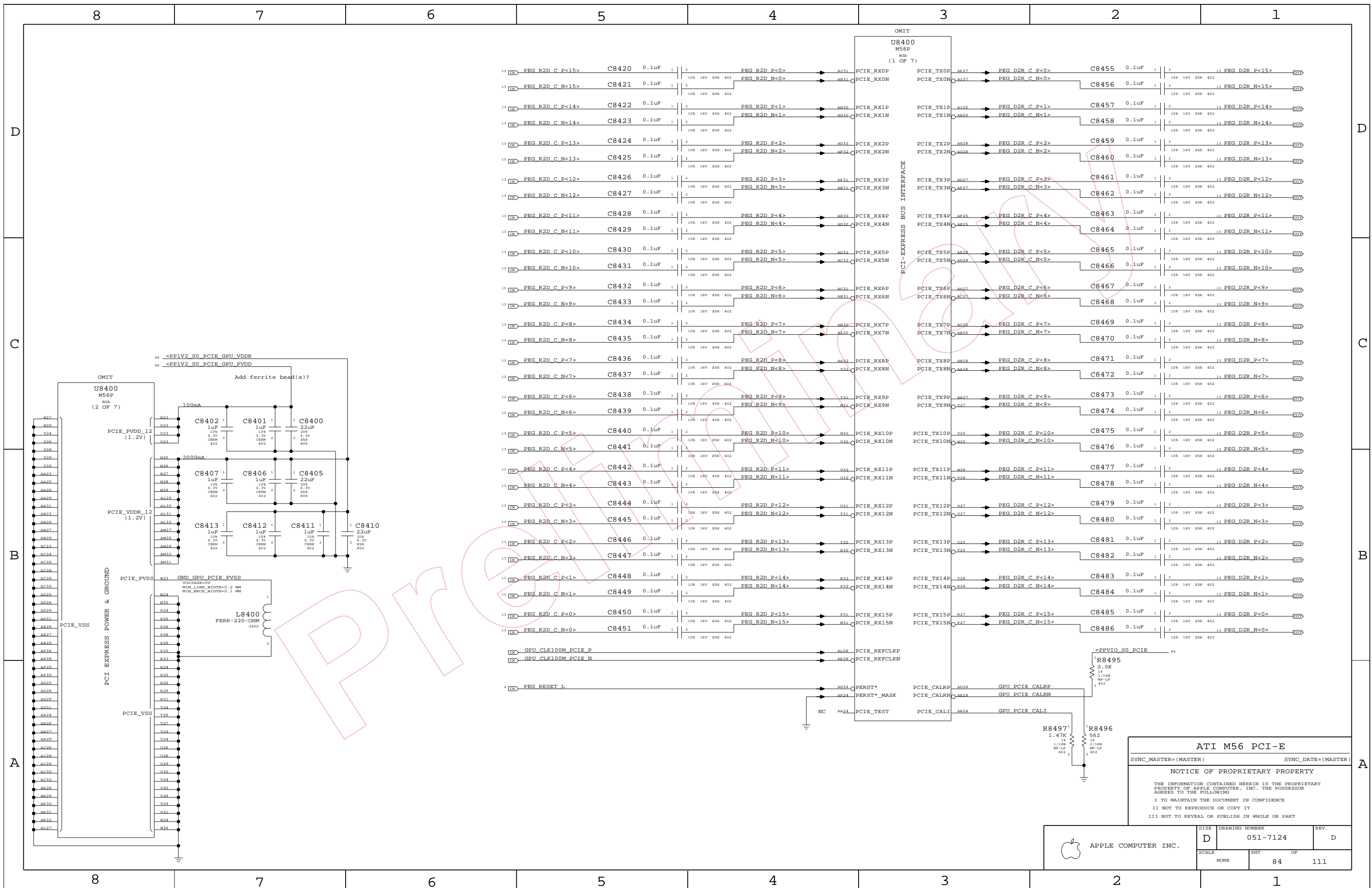
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHT 83 OF	111



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

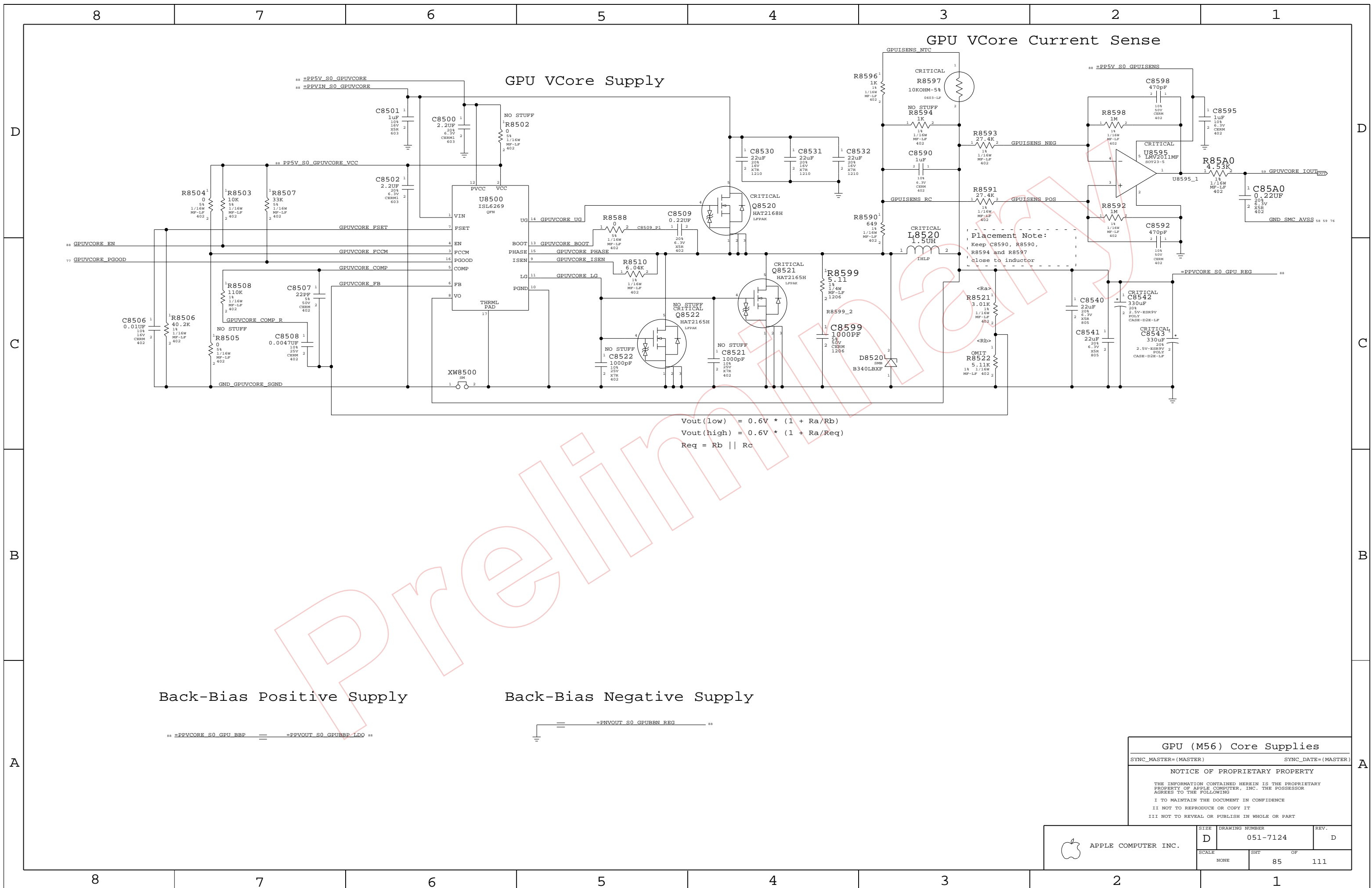
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	DRAWING NUMBER		REV.
	D	051-7124	D
SCALE		SHT	OF
NONE		84	111



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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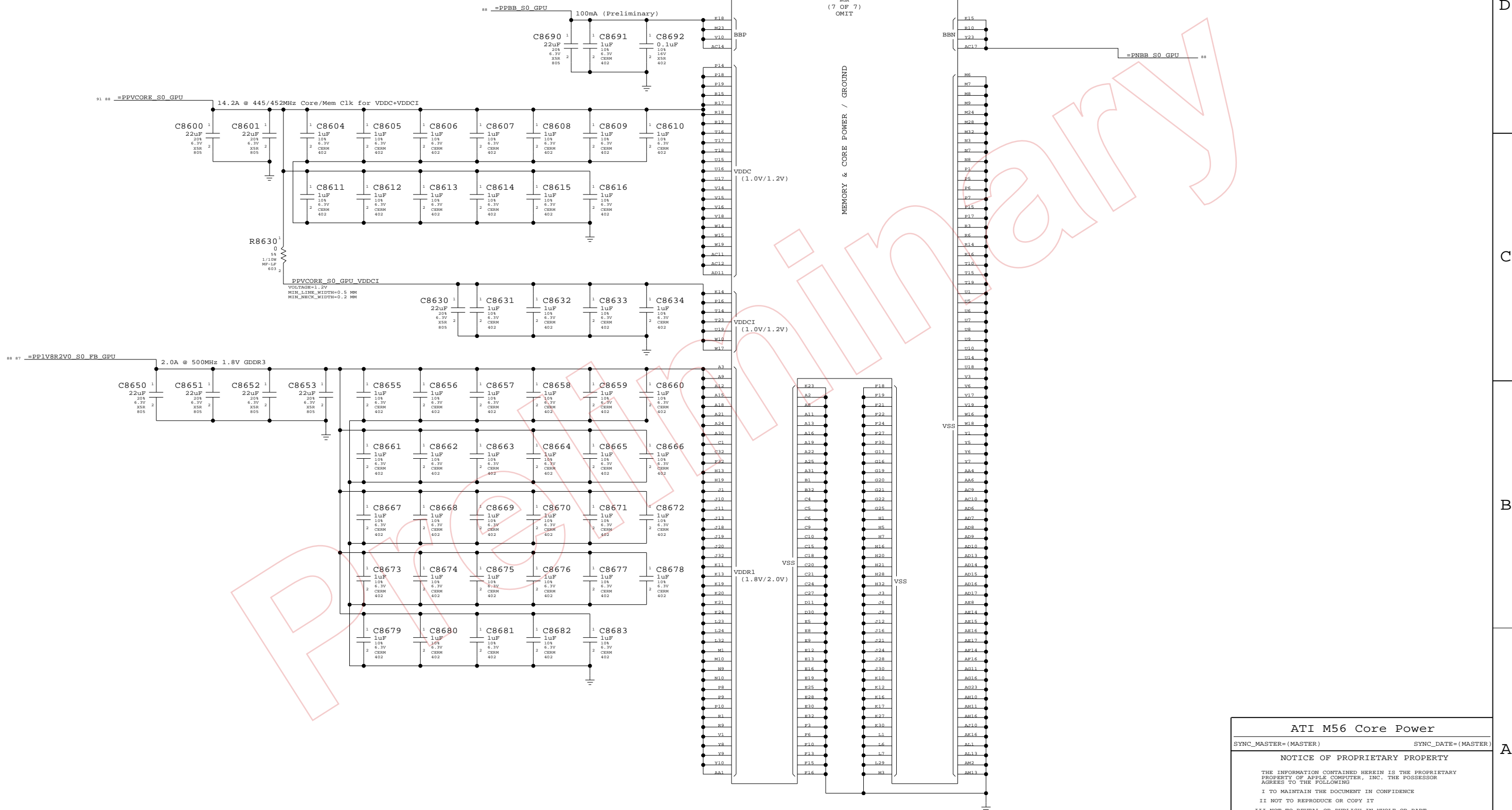
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHEET OF 85 OF 111	

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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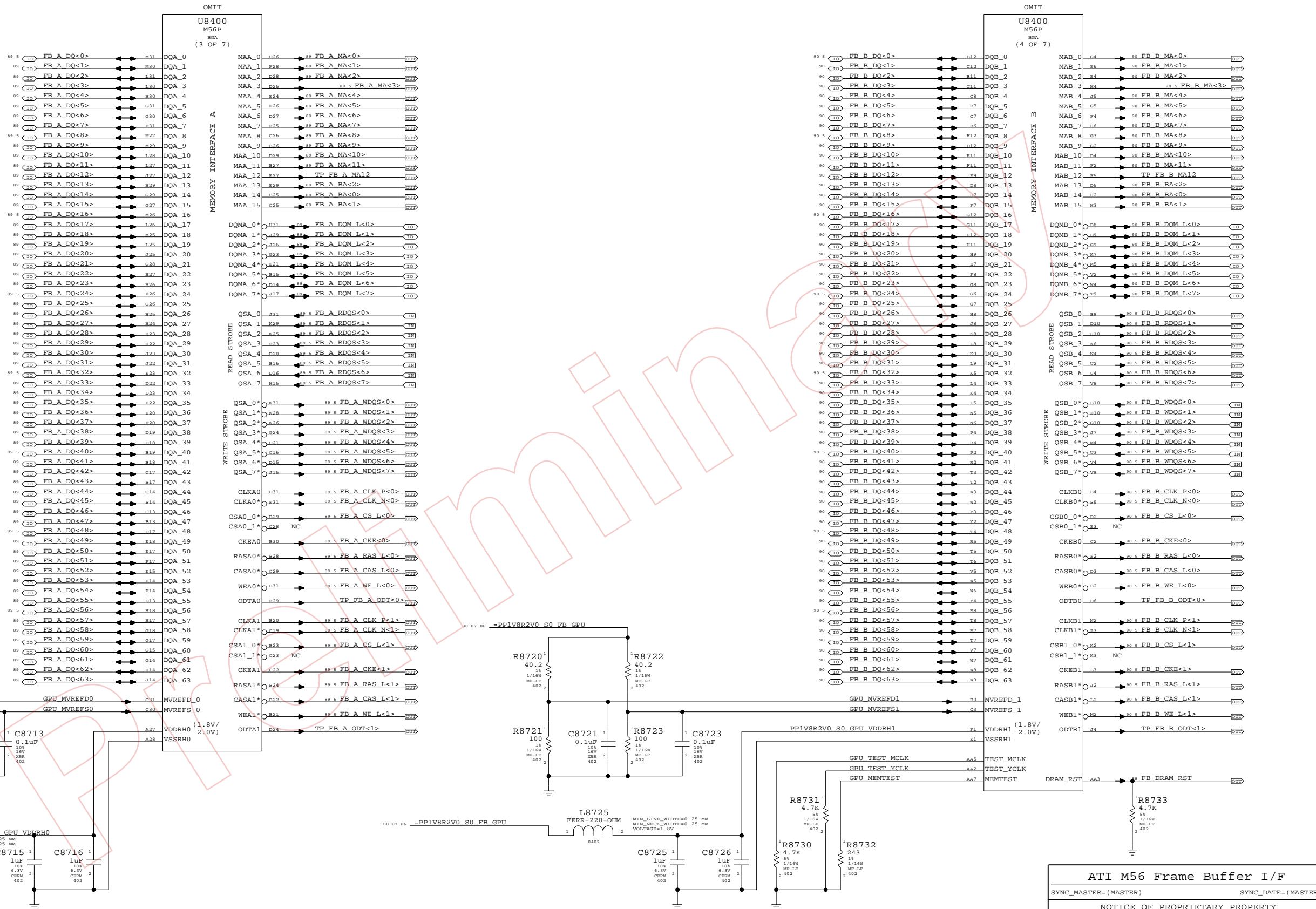
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	86	111	

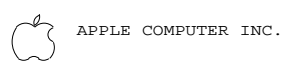
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF, PART NUMBER. Values include D, 051-7124, D, NONE, 87, 111.



8

7

6

5

4

3

2

1

"S0" GPU RAILS

ONLY ON IN RUN

M56 GPIOs

=PP3V3_S0_GPU_VDDR3 #8 #1

59 EP1V0R1V2_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

=PPVCORE_S0_GPU_REG #85
 =PPVCORE_S0_GPU #86 #1
 =PPVCORE_S0_GPU_BB# #85

85 PP5V_S0_GPUVCORE_VCC
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

10k 1/16W 2 R8800
 =PP5V_S0_GPUVCORE #85
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

PP1V2_GPU_IO_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

=PP1V2_S0_PCIE_GPU_VDDR #84
 =PP1V2_S0_PCIE_GPU_VDD# #84
 =PPVIO_S0_PCIE #84
 =PP1V2_S0_REG #77
 =PP1V2_S0_GPU_VDDPLL #91

PPBB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

=PPVOUT_S0_GPUBBP_LDO #85
 =PPBB_S0_GPU #86

PPNB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.2MM
 VOLTAGE=0

=PPNVOUT_S0_GPUBBN_REG #85
 =PPNB_S0_GPU #86

83 76 61 59 41 26 10 6 PP3V3_S0
 MAKE_BASE=TRUE

=PP3V3_S0_GPUBBP
 =PP3V3_S0_GPUBBCTL
 =PP3V3_DDC_DVI #97
 =PP3V3_S0_LCD #94
 =PP3V3_S0_GPU_VDDR3 #88 #1
 =PP3V3_S0_GPU #91 #93 #97
 =PP3V3_S0_GPUBBN
 =PP3V3_S0_GPU_CLOCKS
 =PP3V3_DDC_LCD #94
 =PP3V3_GPU #94

83 6 PP2V5_S0
 MAKE_BASE=TRUE

=PP2V5_S0_GPU_VDD# #91
 =PP2V5_S0_GPU_VDD25 #91
 =PP2V5_S0_GPU_VDDC_CT# #91
 =PP2V5_S0_GPU #93

PP1V8R2V0_S0_FB_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.8V

=PP1V8_S0_FB_VDD #89 #90
 =PP1V8R3V3_S0_GPU_VDDR4 #91
 =PP1V8R3V3_S0_GPU_VDDR5 #91
 =PP1V8_S0_FB_VDDQ #89 #90
 =PP1V8_S0 #78
 =PP1V8R2V0_S0_FB_GPU #86 #87

83 82 81 80 79 78 77 57 6 5 PP12V_S5
 MAKE_BASE=TRUE

=PPVIN_S0_GPUVCORE #85

83 6 PP12V_S0
 MAKE_BASE=TRUE

=PP12V_GPU #94

97 83 76 6 PP5V_S0
 MAKE_BASE=TRUE

=PP5V_S0_GPUBBCTL
 =PP5V_S0_DVI_DDC #97
 =PP5V_S0_GPUISENS #85

85 GPUVCORE_EN
 MAKE_BASE=TRUE

33k 1/16W 2 R8801
 =PM_SLP_S3 #23 #58 #77 #79

97 FB_DRAM_RST
 MAKE_BASE=TRUE

=DRAM_RST #89 #90

94 91 GPU_GPIO_0
 GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
 GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
 GPIO 2 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_3
 GPIO 3 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_4
 GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
 GPIO 5 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_6
 GPIO 6 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

TP_GPU_GPIO_7
 MAKE_BASE=TRUE
 GPU_GPIO_7 #91

91 GPU_GPIO_8
 GPIO 8 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

NC_GPU_GPIO_10
 MAKE_BASE=TRUE
 GPU_GPIO_10 #91

91 GPU_GPIO_9
 GPIO 9 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_13
 GPIO 13 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_12
 GPIO 12 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_11
 GPIO 11 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_24
 GPIO 24 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_27
 GPIO 27 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

GPU_VCORE_LOW
 MAKE_BASE=TRUE
 GPU_GPIO_15 #91

GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
 EXTERNAL PULL DOWN RECOMMENDED

91 GPU_GPIO_28
 GPIO 28 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_29
 GPIO 29 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

TP_GPU_GPIO_14
 MAKE_BASE=TRUE
 GPU_GPIO_14 #91

TP_GPU_GPIO_17
 MAKE_BASE=TRUE
 GPU_GPIO_17 #91

TP_GPU_VGA_R
 MAKE_BASE=TRUE
 GPU_VGA_R #93

TP_GPU_VGA_G
 MAKE_BASE=TRUE
 GPU_VGA_G #93

TP_GPU_VGA_B
 MAKE_BASE=TRUE
 GPU_VGA_B #93

TP_GPU_VGA_HSYNC
 MAKE_BASE=TRUE
 GPU_VGA_HSYNC #93

TP_GPU_VGA_VSYNC
 MAKE_BASE=TRUE
 GPU_VGA_VSYNC #93

TP_GPU_TV_Y
 MAKE_BASE=TRUE
 GPU_TV_Y #93

TP_GPU_TV_COMP
 MAKE_BASE=TRUE
 GPU_TV_COMP #93

TP_GPU_TV_C
 MAKE_BASE=TRUE
 GPU_TV_C #93

TP_GPU_DDC_B_CLK
 MAKE_BASE=TRUE
 GPU_DDC_B_CLK #93

TP_GPU_DDC_B_DATA
 MAKE_BASE=TRUE
 GPU_DDC_B_DATA #93

GPU MISC

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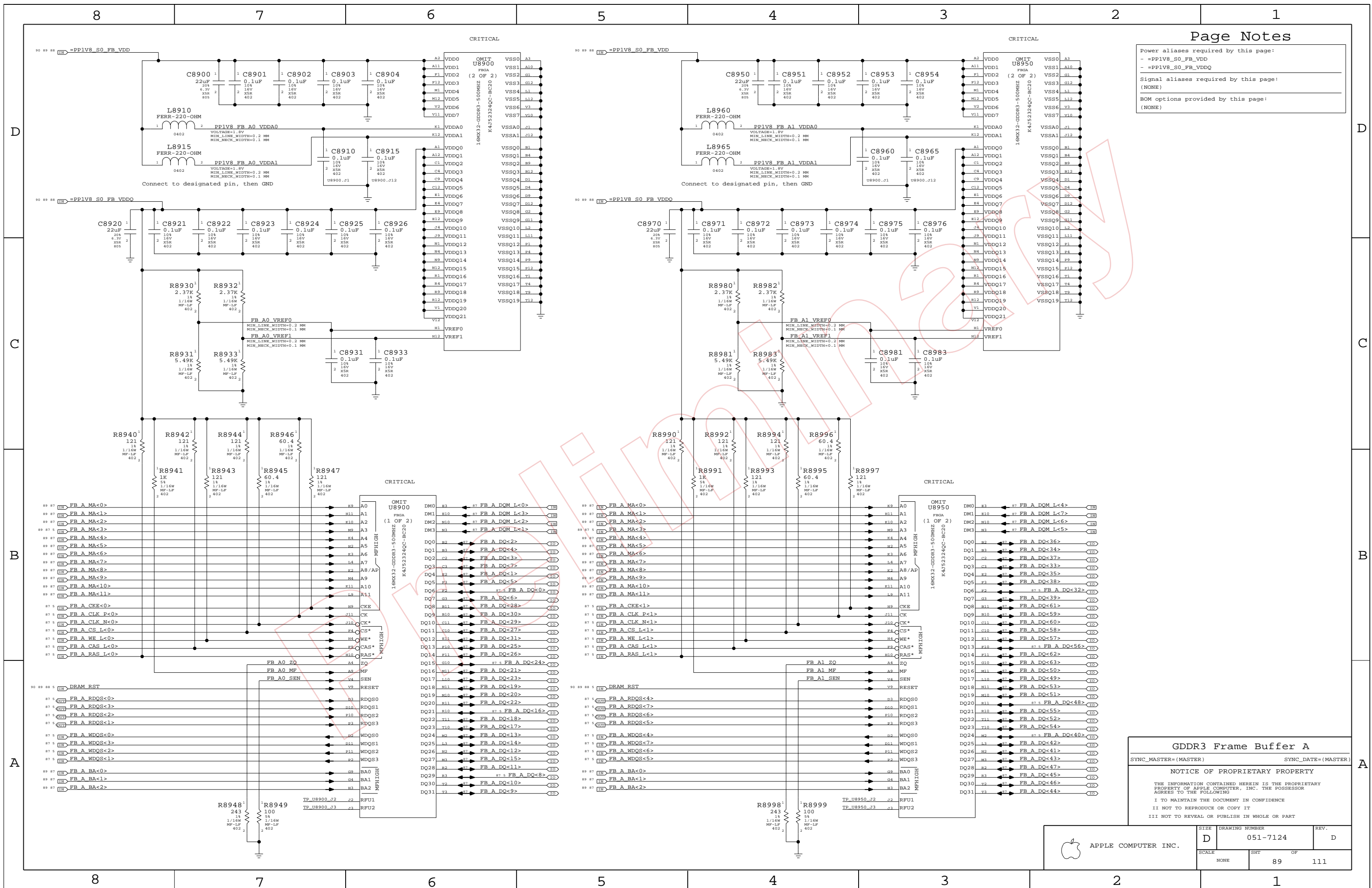
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Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



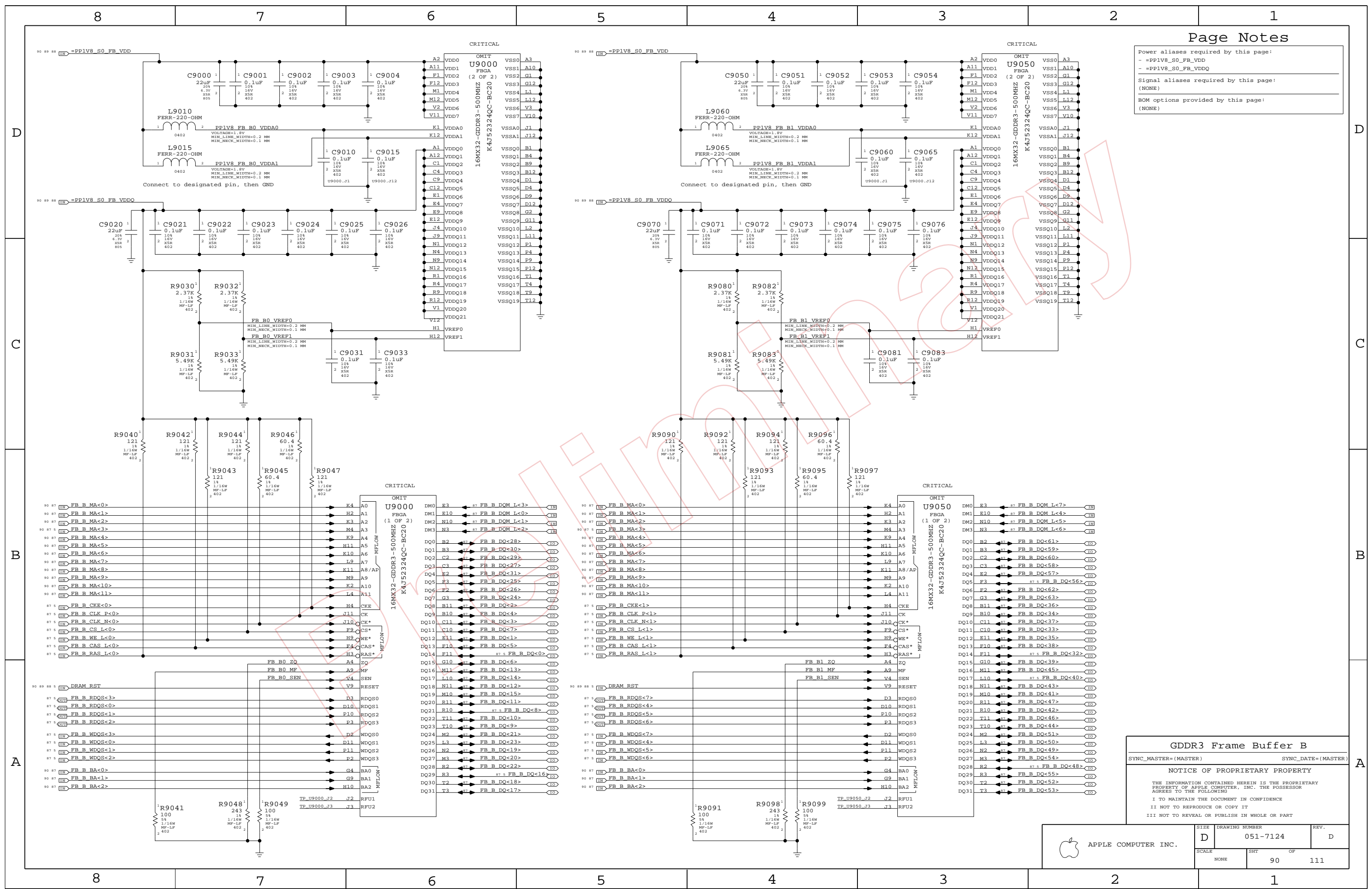
GDDR3 Frame Buffer A
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	90	111	

Page Notes

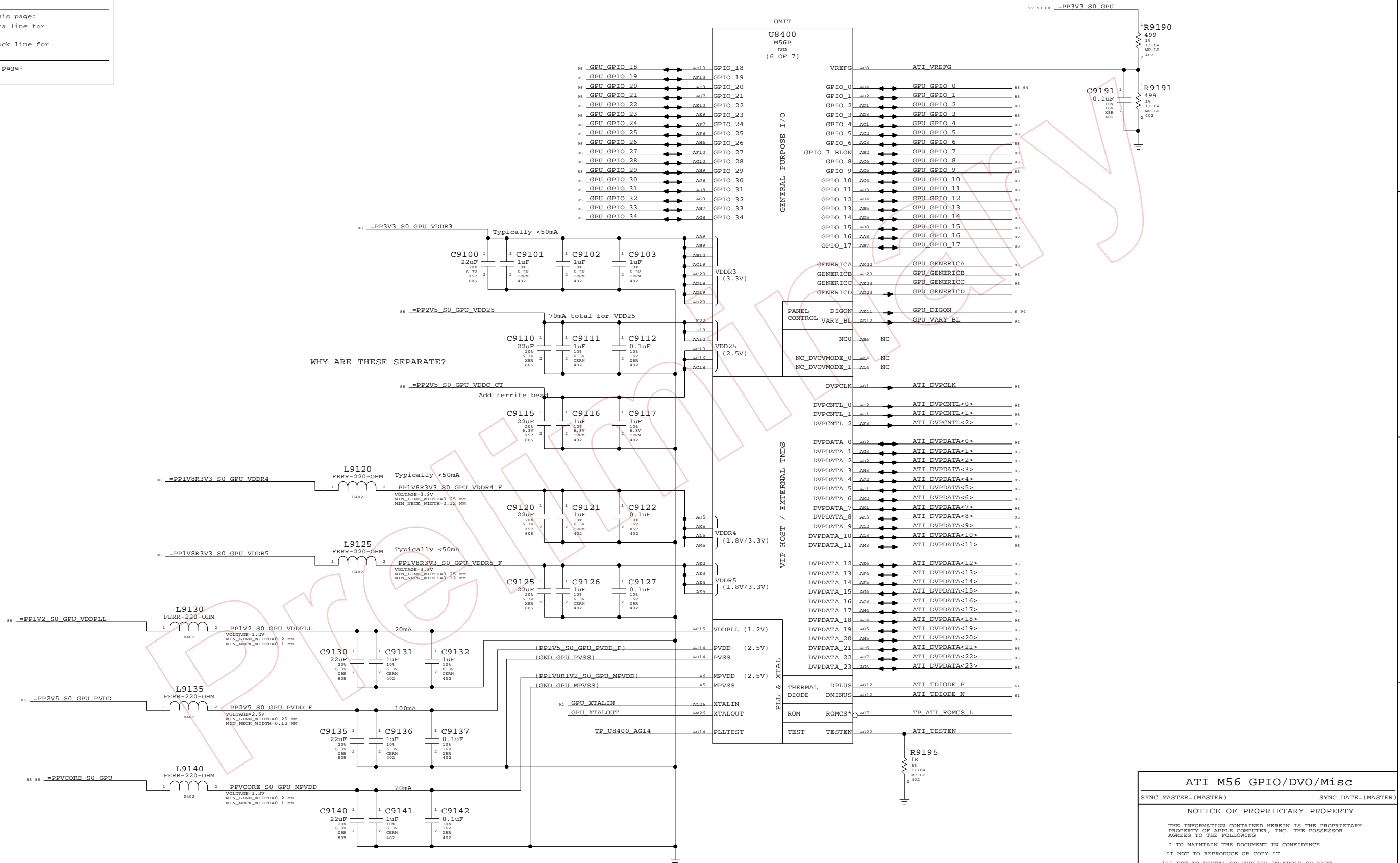
Power aliases required by this page:

- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	D
SCALE	SHT	OF	
NONE	91	111	

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Page Notes

Power aliases required by this page:

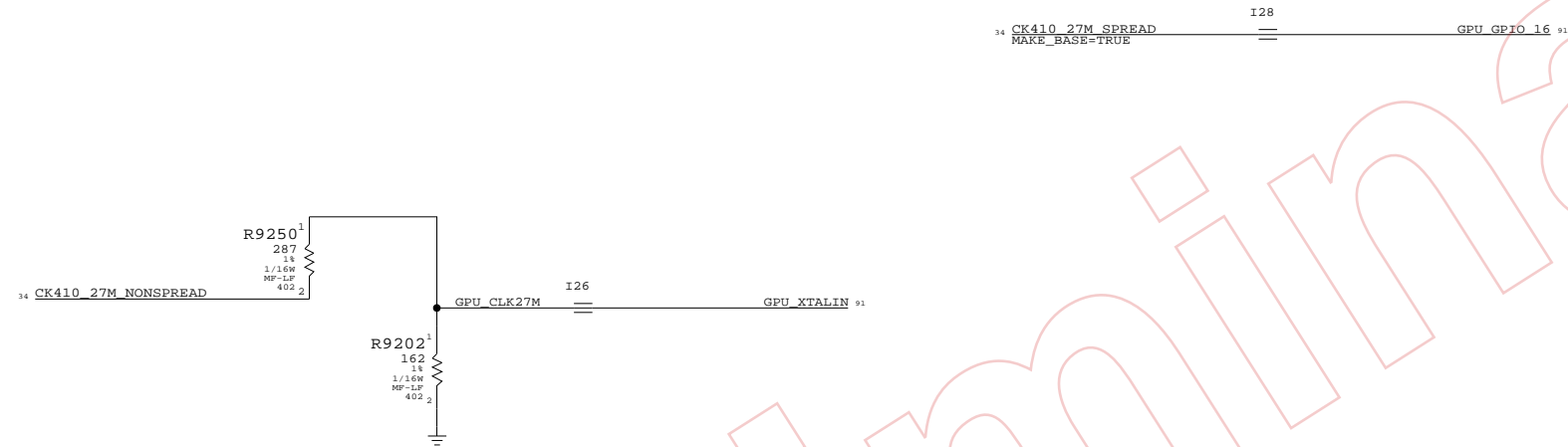
- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8



Preliminary

GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. D
	SCALE NONE	SHT 92	OF 111

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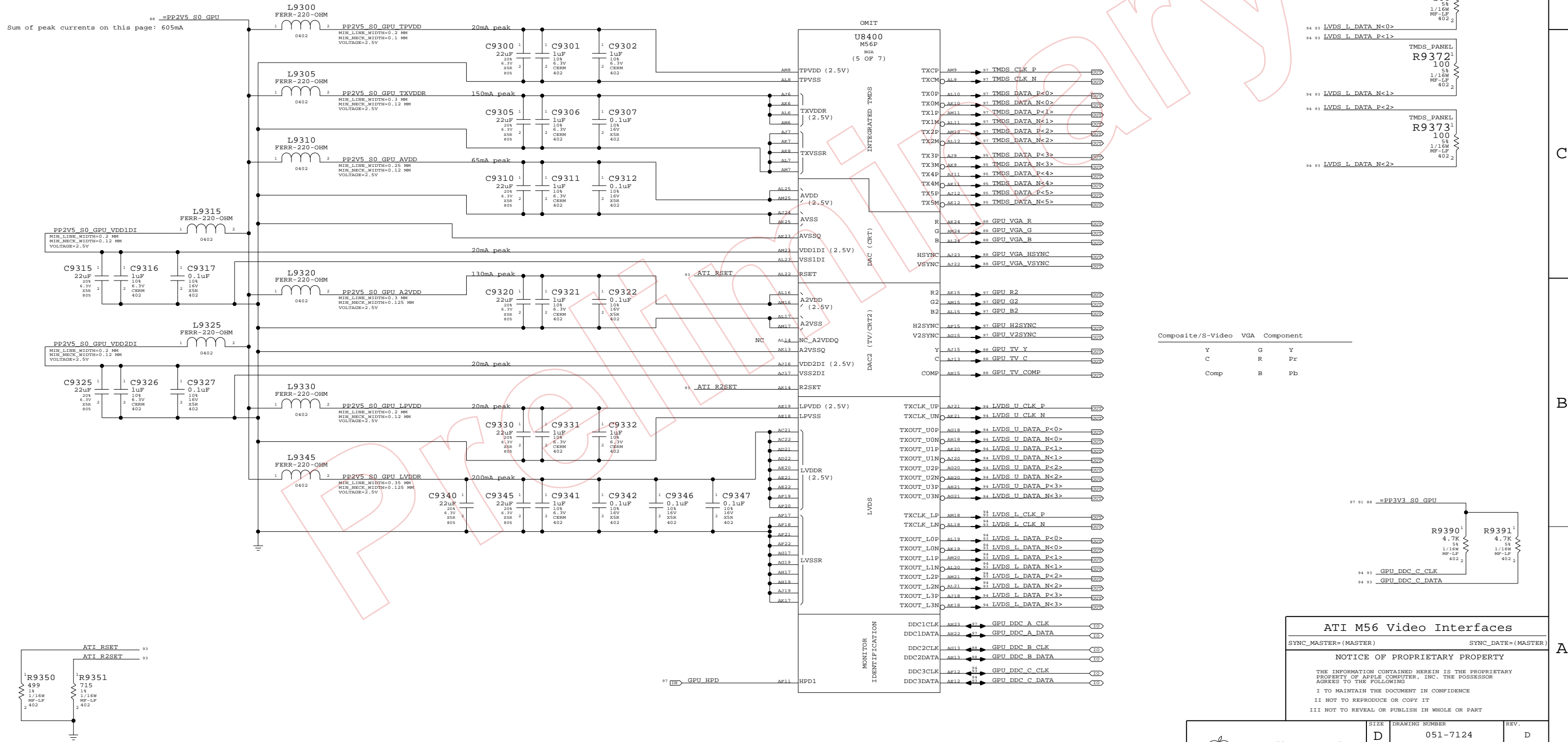
Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

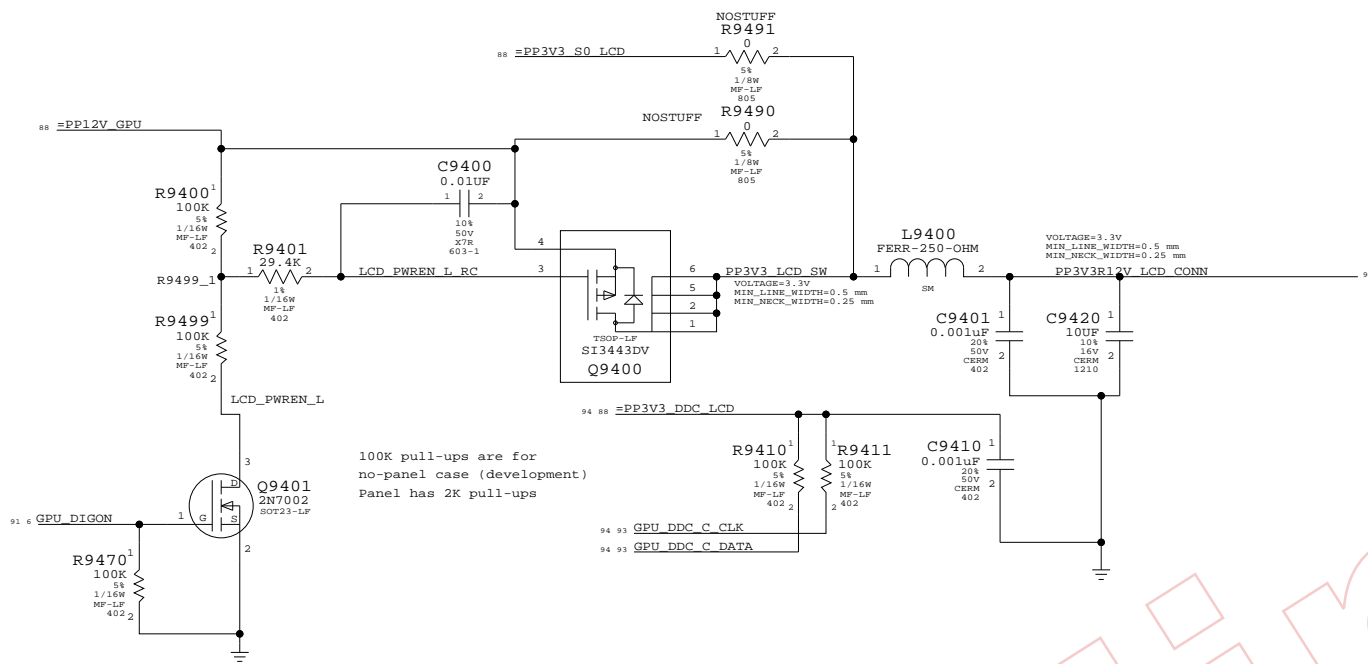
Signal aliases required by this page:
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BOM options provided by this page:
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TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)

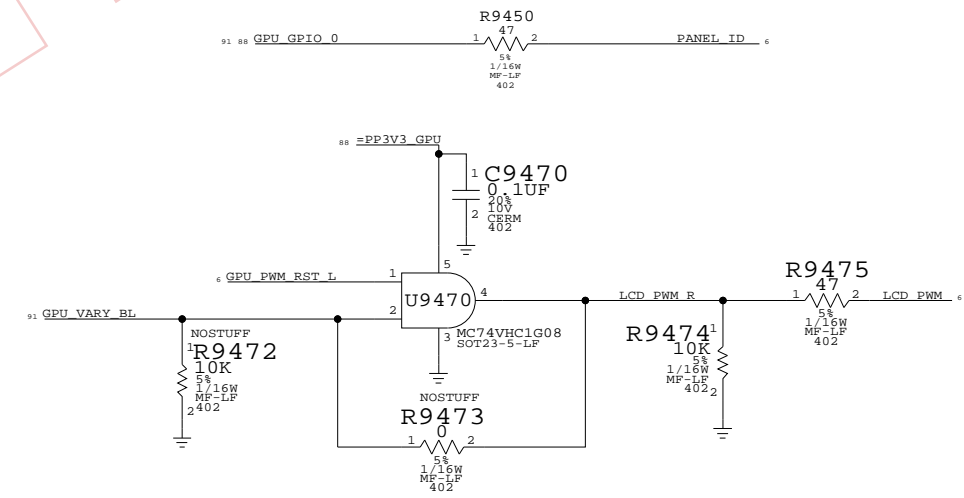
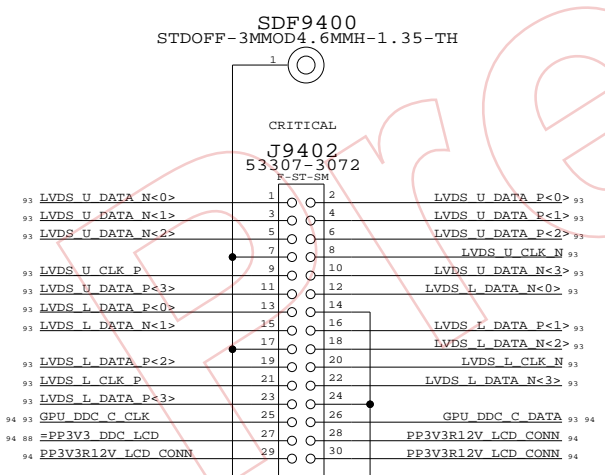


LCD (LVDS) INTERFACE



100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups

GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL



Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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	D	051-7124	D
SCALE	SHT	OF	
NONE	94	111	

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TP ATI DVPNTL<2> == ATI DVPNTL<2> 91
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TP GPU GPIO<34> == GPU_GPIO_34 91
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TP GPU GPIO<33> == GPU_GPIO_33 91
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TP GPU GPIO<32> == GPU_GPIO_32 91
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TP GPU GPIO<31> == GPU_GPIO_31 91
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TP GPU GPIO<30> == GPU_GPIO_30 91
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TP GPU GPIO<26> == GPU_GPIO_26 91
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TP GPU GPIO<25> == GPU_GPIO_25 91
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TP GPU GPIO<21> == GPU_GPIO_21 91
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TP GPU GPIO<19> == GPU_GPIO_19 91
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TP GPU GPIO<18> == GPU_GPIO_18 91
 MAKE_BASE=TRUE

TP GPU GENERIC A == GPU_GENERIC A 91
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TP GPU GENERIC B == GPU_GENERIC B 91
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TP GPU GENERIC C == GPU_GENERIC C 91
 MAKE_BASE=TRUE

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M56 TPS

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SCALE	SHT	OF	111
NONE	95		

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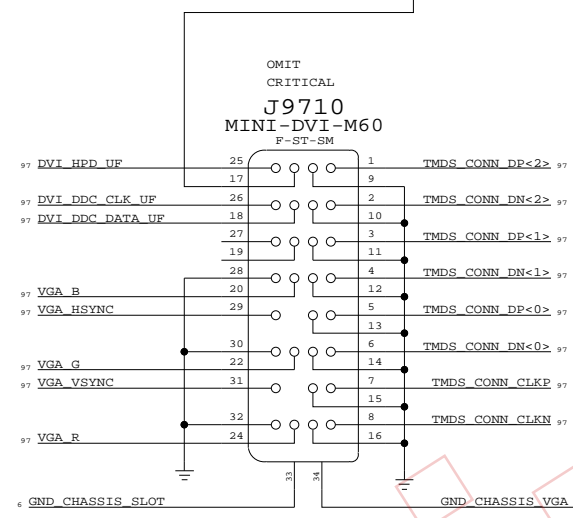
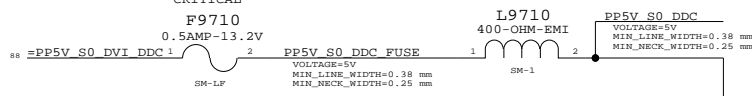
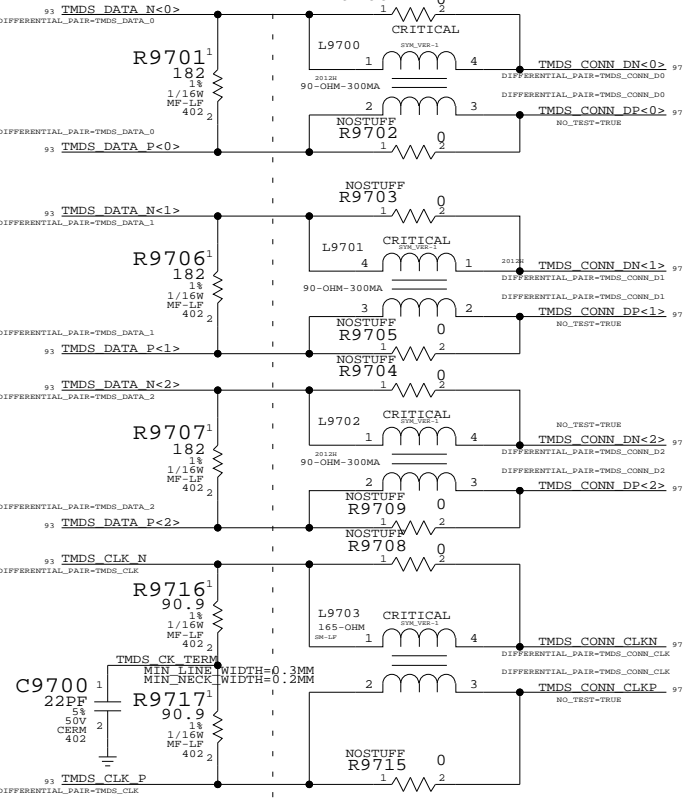
1

PLACE LEFT SIDE AS CLOSE TO GPU (U8400) AS POSSIBLE

PLACE FILTER CLOSE TO TMD5 CONNECTOR

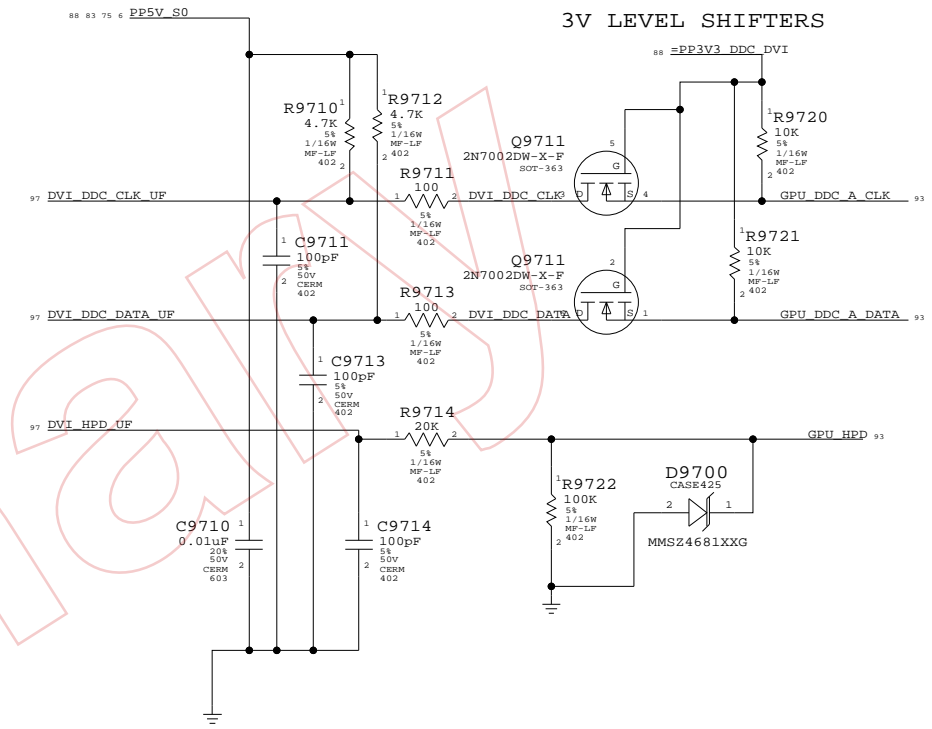
DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)



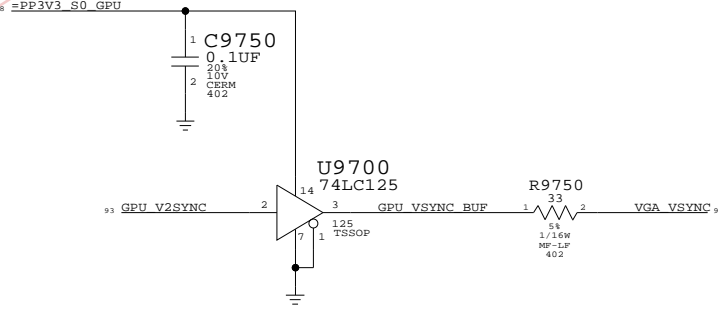
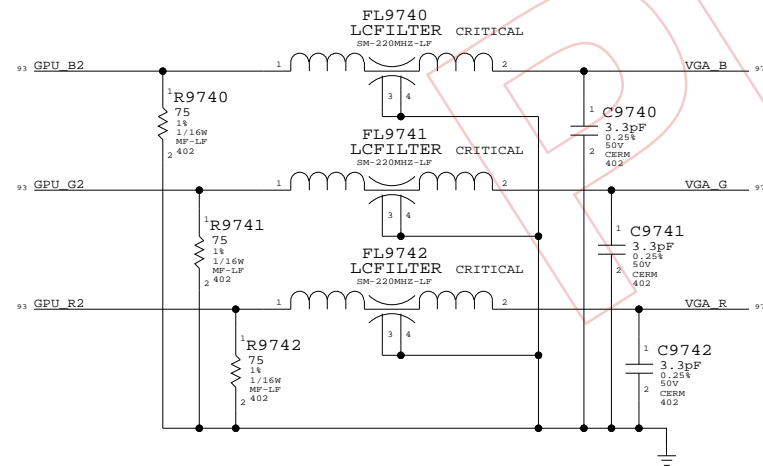
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514S0125	1	M39 MINI-DVI CONN	J9710	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
740S0044	740S0028		F9710	FUSE



ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

External Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

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	NONE	97	111	D

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Table with 8 columns and multiple rows, containing a list of hardware components and their associated identifiers. The columns are numbered 8 to 1 from left to right. The table includes various device names and their corresponding part numbers.

D

D

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8			7			6			5			4			3			2			1		
D	GV3801	HOLE_VIA	m6[38A8]	L7324	IND_0603-LF	m6[73B5]	PP627	PROBEPOINT_SM	m6[5C8]	PP8908	PROBEPOINT_SM	m6[5B5]	D										
	GV3802	HOLE_VIA	m6[38A7]	L7325	IND_0603-LF	m6[73A5]	PP628	PROBEPOINT_SM	m6[5C8]	PP8909	PROBEPOINT_SM	m6[5B5]											
	GV3803	HOLE_VIA	m6[38A8]	L7326	IND_0603-LF	m6[73B5]	PP629	PROBEPOINT_SM	m6[5C8]	PP8910	PROBEPOINT_SM	m6[5B5]											
	GV3804	HOLE_VIA	m6[38A7]	L7327	IND_0603-LF	m6[73A5]	PP630	PROBEPOINT_SM	m6[5C8]	PP8911	PROBEPOINT_SM	m6[5B5]											
	GV3805	HOLE_VIA	m6[38A8]	L7381	IND_0603-LF	m6[73A5]	PP631	PROBEPOINT_SM	m6[5D6]	PP8912	PROBEPOINT_SM	m6[5B5]											
	GV3806	HOLE_VIA	m6[38A7]	L7500	IND_SM	m6[75D1]	PP632	PROBEPOINT_SM	m6[5D6]	PP8913	PROBEPOINT_SM	m6[5B5]											
	GV3807	HOLE_VIA	m6[38A8]	L7501	IND_SM	m6[75B2]	PP633	PROBEPOINT_SM	m6[5D6]	PP8914	PROBEPOINT_SM	m6[5A5]											
	GV3808	HOLE_VIA	m6[38A7]	L7502	IND_TH-VERT-LF	m6[76D8]	PP634	PROBEPOINT_SM	m6[5D6]	PP8915	PROBEPOINT_SM	m6[5A5]											
	J3	CON_2RTSM_125_SM-2MT	m6[61B6]	L7750	IND_SM-LF	m6[77B2]	PP635	PROBEPOINT_SM	m6[5D6]	PP8916	PROBEPOINT_SM	m6[5A5]											
	J600	CON_M14RT_D_THA_M-RT	m6[6D7]	L7800	IND_3P_SM	m6[78C3]	PP636	PROBEPOINT_SM	m6[5D6]	PP8920	PROBEPOINT_SM	m6[5A5]											
C	J7070	CPU_YONAH_SKT_BGA	m6[7C3 7D7]	L7880	IND_0603-LF	m6[73A7]	PP637	PROBEPOINT_SM	m6[5D6]	PP8921	PROBEPOINT_SM	m6[5A5]											
	J7070	CPU_YONAH_SKT_BGA	m6[8D4 8D8]	L7900	IND_3P_SM	m6[79C3]	PP638	PROBEPOINT_SM	m6[5D6]	PP8922	PROBEPOINT_SM	m6[5A5]											
	J1000	CON_2RTSM_125_SM-2MT	m6[10B7]	L8000	IND_IHLP	m6[80C3]	PP639	PROBEPOINT_SM	m6[5D6]	PP8923	PROBEPOINT_SM	m6[5A5]											
	J1101	CON_F28RT_S2MT_SM_F-	m6[11C2]	L8100	IND_IHLP	m6[81C3]	PP640	PROBEPOINT_SM	m6[5D6]	PP8924	PROBEPOINT_SM	m6[5A5]											
	J2600	BATTERY_2P_SM	m6[26C8]	L8203	IND_IHLP	m6[82D3]	PP641	PROBEPOINT_SM	m6[5D6]	PP8925	PROBEPOINT_SM	m6[5A5]											
	J2800	CON_F200RT_D0R2D1MM	m6[28D5]	L8400	IND_0402	m6[84B7]	PP642	PROBEPOINT_SM	m6[5D6]	PP8926	PROBEPOINT_SM	m6[5A5]											
	J2900	CON_F200RT_D0R2D1MM	m6[29D5]	L8520	IND_IHLP	m6[85C3]	PP643	PROBEPOINT_SM	m6[5D6]	PP8927	PROBEPOINT_SM	m6[5A5]											
	J2901	CON_F45T_S2MT_SM_F-S	m6[59C7]	L8715	IND_0402	m6[87A7]	PP644	PROBEPOINT_SM	m6[5D6]	PP8928	PROBEPOINT_SM	m6[5A5]											
	J2903	CON_M25T_S2MT_SM_M-S	m6[59C8]	L8725	IND_0402	m6[87A4]	PP645	PROBEPOINT_SM	m6[5D6]	PP8929	PROBEPOINT_SM	m6[5A5]											
	J4700	CON_F105T_D_SMA_F-ST	m6[47A2]	L8910	IND_0402	m6[89D7]	PP646	PROBEPOINT_SM	m6[5D6]	PP8930	PROBEPOINT_SM	m6[5A5]											
B	J5300	CON_F52RT_D2MT_SM_F-	m6[53C5]	L8915	IND_0402	m6[89D7]	PP647	PROBEPOINT_SM	m6[5D6]	PP8931	PROBEPOINT_SM	m6[5A5]											
	J6000	CON_F305TSM_5047_SM1	m6[60C3]	L8960	IND_0402	m6[89D4]	PP648	PROBEPOINT_SM	m6[5D6]	PP8932	PROBEPOINT_SM	m6[5A5]											
	J6500	CON_M4RT_S2MT_SM_M-R	m6[65D3]	L8965	IND_0402	m6[89D4]	PP649	PROBEPOINT_SM	m6[5D6]	PP8933	PROBEPOINT_SM	m6[5A5]											
	J6501	CON_M5RT_S2MT_SM_M-R	m6[65B2]	L9010	IND_0402	m6[90D7]	PP650	PROBEPOINT_SM	m6[5D6]	PP8934	PROBEPOINT_SM	m6[5A5]											
	J6600	CON_F45T_S2MT_SM_F-S	m6[66C2]	L9015	IND_0402	m6[90D7]	PP651	PROBEPOINT_SM	m6[5D6]	PP8935	PROBEPOINT_SM	m6[5A5]											
	J6601	CON_M4RT_S2MT_SM_M-R	m6[66B5]	L9060	IND_0402	m6[90D4]	PP652	PROBEPOINT_SM	m6[5C6]	PP8936	PROBEPOINT_SM	m6[5A5]											
	J6602	CON_M4RT_S2MT_SM_M-R	m6[66B3]	L9065	IND_0402	m6[90D4]	PP653	PROBEPOINT_SM	m6[5C6]	PP9000	PROBEPOINT_SM	m6[5B4]											
	J7300	CON_F9ANG_S4MT_TH3_F	m6[73D8]	L9120	IND_0402	m6[91B6]	PP654	PROBEPOINT_SM	m6[5C6]	PP9001	PROBEPOINT_SM	m6[5B4]											
	J7301	CON_M7RT_S2MT_SM_M-R	m6[73C1]	L9125	IND_0402	m6[91B6]	PP655	PROBEPOINT_SM	m6[5C6]	PP9002	PROBEPOINT_SM	m6[5B4]											
	J7303	CON_F9ANG_S4MT_TH1_F	m6[73B3]	L9130	IND_0402	m6[91B7]	PP656	PROBEPOINT_SM	m6[5C6]	PP9003	PROBEPOINT_SM	m6[5B4]											
A	J9402	CON_F30ST_D_SM_F-ST	m6[94B6]	L9135	IND_0402	m6[91A7]	PP657	PROBEPOINT_SM	m6[5C6]	PP9004	PROBEPOINT_SM	m6[5B4]											
	J9710	CON_DVI_F325T_Q2MT_S	m6[97D5]	L9140	IND_0402	m6[91A7]	PP658	PROBEPOINT_SM	m6[5C6]	PP9005	PROBEPOINT_SM	m6[5B4]											
	JC900	CON_M7ST_SATA_SM_M-S	m6[38B8]	L9300	IND_0402	m6[93C7]	PP659	PROBEPOINT_SM	m6[5C6]	PP9006	PROBEPOINT_SM	m6[5B4]											
	JC901	CON_M505M_5MM_M-ST-S	m6[38C2]	L9305	IND_0402	m6[93C7]	PP660	PROBEPOINT_SM	m6[5C6]	PP9007	PROBEPOINT_SM	m6[5B4]											
	JD600	CON_R145_10ANG_S3MT	m6[43C6]	L9310	IND_0402	m6[93C7]	PP661	PROBEPOINT_SM	m6[5C6]	PP9008	PROBEPOINT_SM	m6[5B4]											
	JE000	CON_F6ANG_S4MT_TH1_F	m6[46C2]	L9315	IND_0402	m6[93C7]	PP662	PROBEPOINT_SM	m6[5C6]	PP9009	PROBEPOINT_SM	m6[5B4]											
	JE001	CON_F6ANG_S4MT_TH1_F	m6[46B2]	L9320	IND_0402	m6[93B7]	PP663	PROBEPOINT_SM	m6[5C6]	PP9010	PROBEPOINT_SM	m6[5B4]											
	JE310	CON_F4ANG_3MT_USB_TH	m6[47D4]	L9325	IND_0402	m6[93B7]	PP664	PROBEPOINT_SM	m6[5C6]	PP9011	PROBEPOINT_SM	m6[5B4]											
	JE320	CON_F4ANG_3MT_USB_TH	m6[47B4]	L9330	IND_0402	m6[93B7]	PP665	PROBEPOINT_SM	m6[5C6]	PP9012	PROBEPOINT_SM	m6[5B4]											
	JE330	CON_F4ANG_3MT_USB_TH	m6[47A4]	L9345	IND_0402	m6[93B7]	PP666	PROBEPOINT_SM	m6[5C6]	PP9013	PROBEPOINT_SM	m6[5B4]											

	8	7	6	5	4	3	2	1				
D	Q8300	TRA_IRF7413_SO-8	m6[83D2]	R2303	RES_402	m6[23D3]	R3446	RES_402	m6[34B1]	R5809	RES_402	m6[58C2]
	Q8301	TRA_IRF7413_SO-8	m6[83C2]	R2305	RES_402	m6[23D3]	R3451	RES_402	m6[34C4]	R5815	RES_402	m6[58B3]
	Q8302	TRA_2N7002_SOT23-LF	m6[83C3]	R2306	RES_402	m6[23B7]	R3452	RES_402	m6[34B7]	R5817	RES_402	m6[58B3]
	Q8303	TRA_2N7002_SOT23-LF	m6[83D3]	R2307	RES_402	m6[23A7]	R3453	RES_402	m6[34B8]	R5818	RES_402	m6[58B3]
	Q8310	TRA_S13446DV_TSOP-LF	m6[83D8]	R2308	RES_402	m6[23B7]	R3454	RES_402	m6[34B7]	R5819	RES_402	m6[58B3]
	Q8311	TRA_2N7002_SOT23-LF	m6[83C7]	R2309	RES_402	m6[23A7]	R3455	RES_402	m6[34B8]	R5821	RES_402	m6[58B3]
	Q8312	TRA_S13446DV_TSOP-LF	m6[83C5]	R2310	RES_402	m6[23A7]	R3456	RES_402	m6[34B7]	R5822	RES_402	m6[58B3]
	Q8313	TRA_IRF7410_SO-8	m6[83B6]	R2311	RES_402	m6[23A7]	R3457	RES_402	m6[34B7]	R5823	RES_402	m6[58B3]
	Q8315	TRA_2N7002_SOT23-LF	m6[83B5]	R2313	RES_402	m6[23A7]	R3458	RES_402	m6[34B8]	R5824	RES_402	m6[58B3]
	Q8316	TRA_2N7002_SOT23-LF	m6[83C5]	R2314	RES_402	m6[23A7]	R3459	RES_402	m6[34A7]	R5825	RES_402	m6[58B3]
C	Q8317	TRA_S13446DV_TSOP-LF	m6[83D5]	R2316	RES_402	m6[23D7]	R3460	RES_402	m6[34A7]	R5826	RES_402	m6[58B3]
	Q8318	TRA_DUAL_2N7002A_SOT	m6[83A8 83A7]	R2317	RES_402	m6[23D7]	R3461	RES_402	m6[34A7]	R5827	RES_402	m6[58C5]
	Q8319	TRA_S13446DV_TSOP-LF	m6[83C8]	R2318	RES_402	m6[23D7]	R3462	RES_402	m6[34A8]	R5828	RES_402	m6[58B3]
	Q8320	TRA_2N7002_SOT23-LF	m6[83B7]	R2319	RES_402	m6[23D2]	R3463	RES_402	m6[34A7]	R5829	RES_402	m6[58C3]
	Q8520	TRA_HAT2168H_LFFPAK	m6[85D4]	R2320	RES_402	m6[23D7]	R3470	RES_402	m6[34A5]	R5830	RES_402	m6[58C3]
	Q8521	TRA_HAT2168H_LFFPAK	m6[85C4]	R2323	RES_402	m6[23D5]	R3471	RES_402	m6[34A5]	R5831	RES_402	m6[58C3]
	Q8522	TRA_HAT2165H_LFFPAK	m6[85C5]	R2326	RES_402	m6[23D6]	R3485	RES_402	m6[34D1]	R5832	RES_402	m6[58C3]
	Q9400	TRA_S13443DV_TSOP-LF	m6[94C7]	R2327	RES_402	m6[23D6]	R3486	RES_402	m6[34D1]	R5833	RES_402	m6[58C5]
	Q9401	TRA_2N7002_SOT23-LF	m6[94C8]	R2343	RES_402	m6[23D1]	R3487	RES_402	m6[34D1]	R5838	RES_402	m6[58C2]
	Q9711	TRA_2N7002DW_SOT-363	m6[97D2 97C2]	R2388	RES_402	m6[23A3]	R3488	RES_402	m6[34D1]	R5899	RES_402	m6[58D3]
B	R75A0	RES_402	m6[75C7]	R2389	RES_402	m6[38D5]	R3489	RES_402	m6[34D2]	R5900	RES_402	m6[58D7]
	R85A0	RES_402	m6[85D1]	R2390	RES_402	m6[23B3]	R3490	RES_402	m6[34D2]	R5903	RES_402	m6[58D2]
	R600	RES_402	m6[6A7]	R2395	RES_402	m6[23D7]	R3491	RES_402	m6[34D2]	R5904	RES_402	m6[58D2]
	R602	RES_402	m6[6A8]	R2396	RES_402	m6[23D6]	R3492	RES_402	m6[34D2]	R5905	RES_402	m6[58D2]
	R603	RES_402	m6[6B1]	R2397	RES_402	m6[23D6]	R3493	RES_402	m6[34D7]	R5906	RES_402	m6[58D2]
	R605	RES_402	m6[6A5]	R2398	RES_402	m6[23D8]	R3494	RES_402	m6[34D7]	R5907	RES_402	m6[58B7]
	R611	RES_402	m6[6B7]	R2399	RES_402	m6[23C1]	R3495	RES_402	m6[34D7]	R5910	RES_402	m6[58D2]
	R612	RES_402	m6[6B7]	R2500	RES_402	m6[25A8]	R3496	RES_402	m6[34C5]	R5911	RES_402	m6[58D2]
	R614	RES_402	m6[6B7]	R2501	RES_402	m6[25C8]	R3497	RES_402	m6[34D4]	R5912	RES_402	m6[58D2]
	R615	RES_402	m6[6B7]	R2502	RES_402	m6[25D8]	R3498	RES_402	m6[34D5]	R5913	RES_402	m6[58D2]
A	R616	RES_402	m6[6A7]	R2600	RES_402	m6[26C7]	R3499	RES_402	m6[34D5]	R5914	RES_402	m6[58D2]
	R617	RES_402	m6[6A7]	R2606	RES_402	m6[26C7]	R3824	RES_402	m6[38D2]	R5915	RES_402	m6[58D2]
	R618	RES_402	m6[6C7]	R2607	RES_402	m6[26C8]	R3851	RES_402	m6[38D3]	R5916	RES_402	m6[58C2]
	R619	RES_402	m6[6B7]	R2609	RES_402	m6[26D7]	R3852	RES_402	m6[38D2]	R5917	RES_402	m6[58C2]
	R0701	RES_402	m6[7C6]	R2611	RES_402	m6[26D5]	R3853	RES_402	m6[38D2]	R5919	RES_402	m6[58B4]
	R0702	RES_402	m6[7C6]	R2612	RES_402	m6[26D5]	R3857	RES_402	m6[38B3]	R5920	RES_402	m6[58B5]
	R0703	RES_402	m6[7C5]	R2622	RES_402	m6[26D4]	R3858	RES_402	m6[38B3]	R5921	RES_402	m6[58B5]
	R0704	RES_402	m6[7C5]	R2623	RES_402	m6[26D2]	R3859	RES_402	m6[38B2]	R5922	RES_402	m6[58B5]
	R0705	RES_402	m6[7B4]	R2624	RES_402	m6[26D2]	R3897	RES_402	m6[38B7]	R5923	RES_402	m6[58B5]
	R0706	RES_402	m6[7B5]	R2625	RES_402	m6[26D2]	R3899	RES_402	m6[38B5]	R5924	RES_402	m6[58B5]

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ZH526	HOLE_VIA	m60[5B1]
ZH527	HOLE_VIA	m60[5B1]
ZH528	HOLE_VIA	m60[5B1]
ZH529	HOLE_VIA	m60[5B1]
ZH601	MTGHOLE	m60[6A3]
ZH602	MTGHOLE	m60[6A3]
ZH603	MTGHOLE	m60[6A3]
ZH606	MTGHOLE	m60[6A1]
ZH607	MTGHOLE	m60[9D4]
ZH608	MTGHOLE	m60[9D3]
ZH609	MTGHOLE	m60[9D2]
ZH610	MTGHOLE	m60[9D2]

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