1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M38A - DVT

06/22/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
13		445818	ENGINEERING RELEASED	06/22/06	06/22/04

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

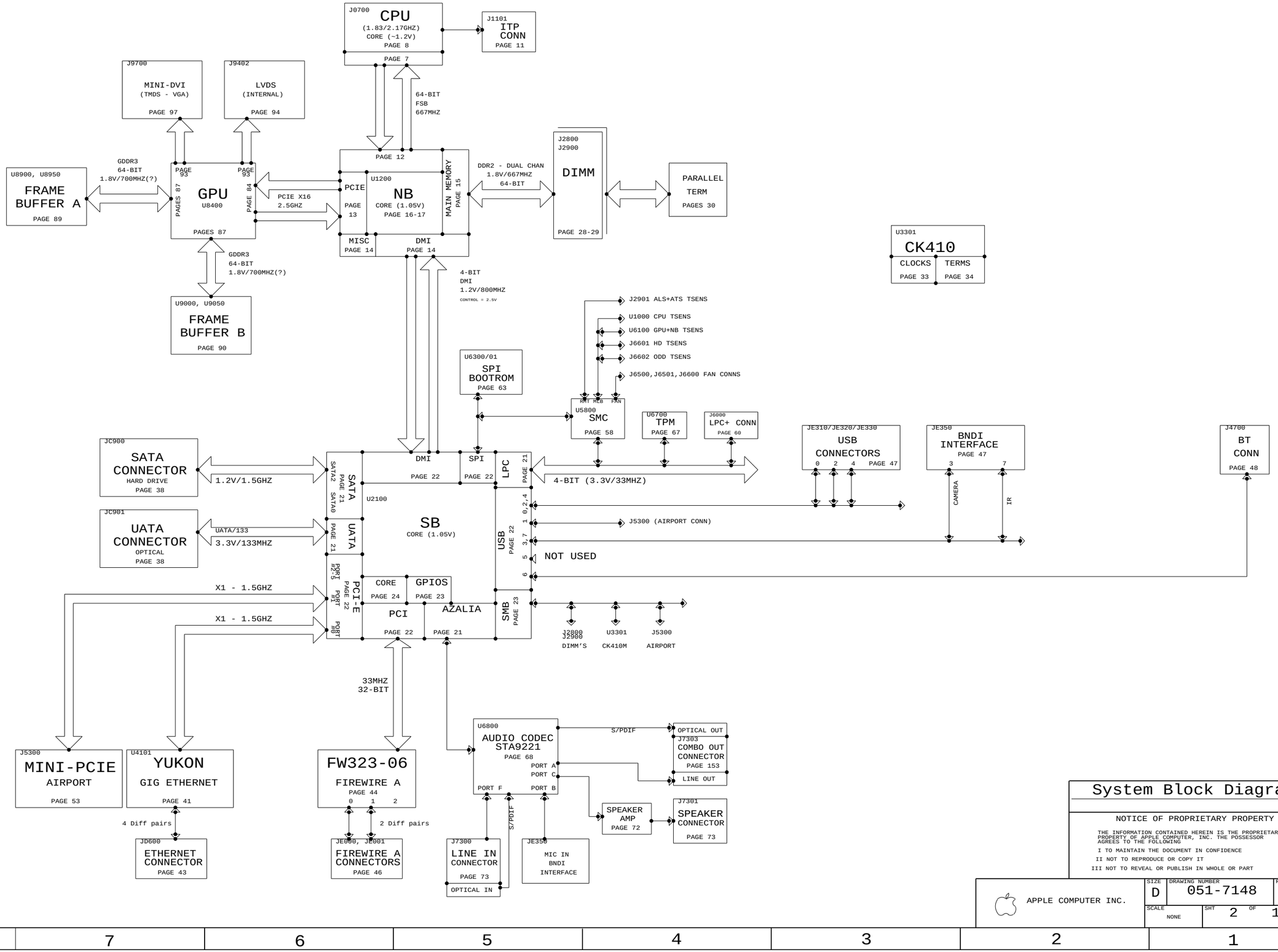
DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,M38A

DRAWING NUMBER 051-7148
REV. 13
SHT 1 OF 110

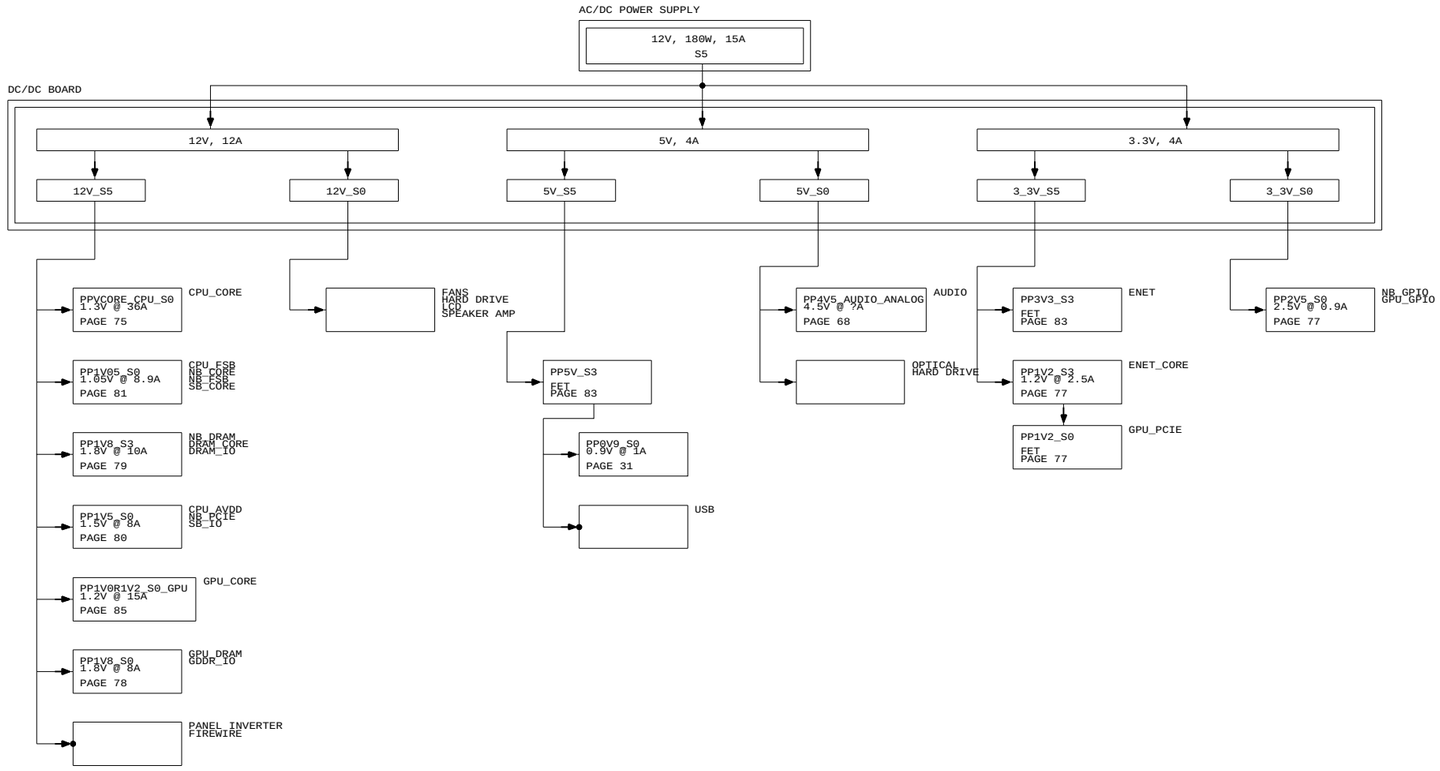


System Block Diagram

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 2 OF 110	



Power Block Diagram

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7148 | REV. 13

SCALE NONE | SHT 3 OF 110

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
	338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
	343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
	338S0344	1	IC,ATI,M56P,GRAFIXCTLR,880BGA,LF	U8400	CRITICAL	
	359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
	338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
	338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
	341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1235	353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	
	128S0078	3	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	
	825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16CE680KX 680UF 16V LF
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330FS 330UF 6.3V LF
128S0080	128S0078		C7517,C7518,C7910	SANYO 16SVP330M 330UF 16V SMD LF
124-0338	124-0333		C7501,C8014	CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
353S1321	353S1105		U7910	LM339
378S0141	378S0140		LED601,LED602,LED603	LED
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7148	1	PCB,SCHEM,MLB,M38A	SCH1		17_INCH_LCD
	820-2052	1	PCB,FAB,MLB,M38A	MLB1		17_INCH_LCD
(341S1908 - DEVEL) (341S1909 - FINAL) (335S0384 - BLNK)	341T0040	1	EFI ROM,M38A	U6301	CRITICAL	17_INCH_LCD
	114S0264	1	3.01K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P2V
(341S1907 - PROG) (338S0274 - BLNK)	341T0039	1	IC,SMC,M38A	U5800	CRITICAL	17_INCH_LCD
	338S0315	1	IC,ATI,M56LP,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
	114S0287	1	5.11K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_0P953V
	114S0281	1	4.53K,1%,1/16W,402,MF-LF	R8522		GPU_VCORE_1P0V
	337S3299	1	2.00GHZ MEROM	CPU	CRITICAL	2P00_CPU
	337S3293	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

Table Items

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7148 | REV. 13

SCALE NONE | SHT 4 OF 110

LAYOUT NOTE: PLACE NEAR J0700

12 7 5	FSB_A_L<6>	PP600	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP601	OMIT P4MM
12 7 5	FSB_A_L<27>	PP602	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP603	OMIT P4MM
12 7 5	FSB_D_L<0>	PP604	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP605	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP606	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP607	OMIT P4MM
12 7 5	FSB_D_L<16>	PP608	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP609	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP610	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP611	OMIT P4MM
12 7 5	FSB_D_L<41>	PP612	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP613	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP614	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP615	OMIT P4MM
12 7 5	FSB_D_L<59>	PP616	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP617	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP618	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP619	OMIT P4MM
12 7 5	FSB_LOCK_L	PP620	OMIT P4MM
12 11 7	FSB_CPURST_L	PP621	OMIT P4MM
21 7	CPU_INIT_L	PP622	OMIT P4MM
21 7	CPU_A20M_L	PP623	OMIT P4MM
21 7	CPU_IGNNE_L	PP624	OMIT P4MM
21 7	CPU_STPCLK_L	PP625	OMIT P4MM
21 7	CPU_INTR	PP626	OMIT P4MM
21 7	CPU_NMI	PP627	OMIT P4MM
21 7	CPU_SMI_L	PP628	OMIT P4MM
34 7	FSB_CLK_CPU_P	PP629	OMIT P4MM
34 7	FSB_CLK_CPU_N	PP630	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

34 21	SB_CLK100M_SATA_P	PP6C4	OMIT P4MM
34 21	SB_CLK100M_SATA_N	PP6C5	OMIT P4MM
38 21	IDE_PDIOR_L	PP6C6	OMIT P4MM
38 21	IDE_PDIORDY	PP6C7	OMIT P4MM
38 21	IDE_PDD<9>	PP6C8	OMIT P4MM
34 22	PCI_CLK_SB	PP6D0	OMIT P4MM
41 22	PCIE_A_D2R_P	PP6D1	OMIT P4MM
41 22	PCIE_A_D2R_N	PP6D2	OMIT P4MM
53 22	PCIE_B_D2R_P	PP5E1	OMIT P4MM
53 22	PCIE_B_D2R_N	PP5E2	OMIT P4MM
22 14	DMI_N2S_P<0>	PP6D3	OMIT P4MM
22 14	DMI_N2S_N<0>	PP6D4	OMIT P4MM
34 22	SB_CLK100M_DMI_P	PP6D5	OMIT P4MM
34 22	SB_CLK100M_DMI_N	PP6D6	OMIT P4MM
58 26 23	PM_SYSRST_L	PP6D7	OMIT P4MM
58 44 23 67 60	PM_CLKRUN_L	PP6D8	OMIT P4MM
34 23	SB_CLK14P3M_TIMER	PP6D9	OMIT P4MM
34 23	SB_CLK48M_USBCTLR	PP6E0	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1200

12 7 5	FSB_A_L<6>	PP631	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP632	OMIT P4MM
12 7 5	FSB_A_L<27>	PP633	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP634	OMIT P4MM
12 7 5	FSB_D_L<0>	PP635	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP636	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP637	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP638	OMIT P4MM
12 7 5	FSB_D_L<16>	PP639	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP640	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP641	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP642	OMIT P4MM
12 7 5	FSB_D_L<41>	PP643	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP644	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP645	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP646	OMIT P4MM
12 7 5	FSB_D_L<59>	PP647	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP648	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP649	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP650	OMIT P4MM
12 7 5	FSB_LOCK_L	PP651	OMIT P4MM
12 7	FSB_HIT_L	PP652	OMIT P4MM
12 7	FSB_HITM_L	PP653	OMIT P4MM
12 7	FSB_BNR_L	PP654	OMIT P4MM
12 7	FSB_BREQ0_L	PP655	OMIT P4MM
12 7	FSB_DBSY_L	PP656	OMIT P4MM
12 7	FSB_DPWR_L	PP657	OMIT P4MM
12 7	FSB_REQ_L<0>	PP658	OMIT P4MM
12 7	FSB_REQ_L<1>	PP659	OMIT P4MM
12 7	FSB_REQ_L<2>	PP660	OMIT P4MM
12 7	FSB_REQ_L<3>	PP661	OMIT P4MM
12 7	FSB_REQ_L<4>	PP662	OMIT P4MM
34 12	FSB_CLK_NB_P	PP663	OMIT P4MM
34 12	FSB_CLK_NB_N	PP664	OMIT P4MM
75 26 14	VR_PWRGOOD_DELAY	PP665	OMIT P4MM
14	NB_RST_IN_L_R	PP666	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_P	PP667	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_N	PP668	OMIT P4MM
22 14	DMI_S2N_N<0>	PP673	OMIT P4MM
22 14	DMI_S2N_P<0>	PP674	OMIT P4MM
19 14	MEM_VREF_NB_0	PP6E1	OMIT P4MM
19 14	MEM_VREF_NB_1	PP675	OMIT P4MM
28 15	MEM_A_DQ<7>	PP676	OMIT P4MM
28 15	MEM_A_DQ<14>	PP677	OMIT P4MM
28 15	MEM_A_DQ<16>	PP678	OMIT P4MM
28 15	MEM_A_DQ<25>	PP679	OMIT P4MM
28 15	MEM_A_DQ<39>	PP680	OMIT P4MM
28 15	MEM_A_DQ<47>	PP681	OMIT P4MM
28 15	MEM_A_DQ<54>	PP682	OMIT P4MM
28 15	MEM_A_DQ<59>	PP683	OMIT P4MM
29 15	MEM_A_DQS_P<0>	PP684	OMIT P4MM
29 15	MEM_A_DQS_N<0>	PP685	OMIT P4MM
28 15	MEM_A_DQS_P<1>	PP686	OMIT P4MM
28 15	MEM_A_DQS_N<1>	PP687	OMIT P4MM
28 15	MEM_A_DQS_P<2>	PP688	OMIT P4MM
28 15	MEM_A_DQS_N<2>	PP689	OMIT P4MM
28 15	MEM_A_DQS_P<3>	PP690	OMIT P4MM
28 15	MEM_A_DQS_N<3>	PP691	OMIT P4MM
28 15	MEM_A_DQS_P<4>	PP692	OMIT P4MM
28 15	MEM_A_DQS_N<4>	PP693	OMIT P4MM
28 15	MEM_A_DQS_P<5>	PP694	OMIT P4MM
28 15	MEM_A_DQS_N<5>	PP695	OMIT P4MM
28 15	MEM_A_DQS_P<6>	PP696	OMIT P4MM
28 15	MEM_A_DQS_N<6>	PP697	OMIT P4MM
28 15	MEM_A_DQS_P<7>	PP698	OMIT P4MM
28 15	MEM_A_DQS_N<7>	PP699	OMIT P4MM
29 15	MEM_B_DQ<6>	PP6A0	OMIT P4MM
29 15	MEM_B_DQ<8>	PP6A1	OMIT P4MM
29 15	MEM_B_DQ<23>	PP6A2	OMIT P4MM
29 15	MEM_B_DQ<25>	PP6A3	OMIT P4MM
29 15	MEM_B_DQ<38>	PP6A4	OMIT P4MM
29 15	MEM_B_DQ<44>	PP6A5	OMIT P4MM
29 15	MEM_B_DQ<48>	PP6A6	OMIT P4MM
29 15	MEM_B_DQ<62>	PP6A7	OMIT P4MM
29 15	MEM_B_DQS_P<0>	PP6A8	OMIT P4MM
29 15	MEM_B_DQS_N<0>	PP6A9	OMIT P4MM
29 15	MEM_B_DQS_P<1>	PP6B0	OMIT P4MM
29 15	MEM_B_DQS_N<1>	PP6B1	OMIT P4MM
29 15	MEM_B_DQS_P<2>	PP6B2	OMIT P4MM
29 15	MEM_B_DQS_N<2>	PP6B3	OMIT P4MM
29 15	MEM_B_DQS_P<3>	PP6B4	OMIT P4MM
29 15	MEM_B_DQS_N<3>	PP6B5	OMIT P4MM
29 15	MEM_B_DQS_P<4>	PP6B6	OMIT P4MM
29 15	MEM_B_DQS_N<4>	PP6B7	OMIT P4MM
29 15	MEM_B_DQS_P<5>	PP6B8	OMIT P4MM
29 15	MEM_B_DQS_N<5>	PP6B9	OMIT P4MM
29 15	MEM_B_DQS_P<6>	PP6C0	OMIT P4MM
29 15	MEM_B_DQS_N<6>	PP6C1	OMIT P4MM
29 15	MEM_B_DQS_P<7>	PP6C2	OMIT P4MM
29 15	MEM_B_DQS_N<7>	PP6C3	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U8400

89 87 5	FB_A_DQ<0>	PP8700	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8701	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8702	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8703	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8704	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8705	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8706	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8707	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8708	OMIT P4MM
89 87	FB_A_RDQS<0>	PP8709	OMIT P4MM
89 87	FB_A_RDQS<1>	PP8710	OMIT P4MM
89 87	FB_A_RDQS<2>	PP8711	OMIT P4MM
89 87	FB_A_RDQS<3>	PP8712	OMIT P4MM
89 87	FB_A_RDQS<4>	PP8713	OMIT P4MM
89 87	FB_A_RDQS<5>	PP8714	OMIT P4MM
89 87	FB_A_RDQS<6>	PP8715	OMIT P4MM
89 87	FB_A_RDQS<7>	PP8716	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP8720	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP8721	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP8722	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP8723	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP8724	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP8725	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP8726	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP8727	OMIT P4MM
90 87 5	FB_B_MA<3>	PP8728	OMIT P4MM
90 87	FB_B_RDQS<0>	PP8729	OMIT P4MM
90 87	FB_B_RDQS<1>	PP8730	OMIT P4MM
90 87	FB_B_RDQS<2>	PP8731	OMIT P4MM
90 87	FB_B_RDQS<3>	PP8732	OMIT P4MM
90 87	FB_B_RDQS<4>	PP8733	OMIT P4MM
90 87	FB_B_RDQS<5>	PP8734	OMIT P4MM
90 87	FB_B_RDQS<6>	PP8735	OMIT P4MM
90 87	FB_B_RDQS<7>	PP8736	OMIT P4MM
84 34	GPU_CLK100M_PCIE_P	PP8400	OMIT P4MM
84 34	GPU_CLK100M_PCIE_N	PP8401	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4101

41 34	ENET_CLK100M_PCIE_P	PP4100	OMIT P4MM
41 34	ENET_CLK100M_PCIE_N	PP4101	OMIT P4MM

PLACE NEAR U8900

89 87	FB_A_CKE<0>	PP8900	OMIT P4MM
89 87	FB_A_CLK_P<0>	PP8901	OMIT P4MM
89 87	FB_A_CLK_N<0>	PP8902	OMIT P4MM
89 87	FB_A_CS_L<0>	PP8903	OMIT P4MM
89 87	FB_A_WE_L<0>	PP8904	OMIT P4MM
89 87	FB_A_CAS_L<0>	PP8905	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8906	OMIT P4MM
89 87	FB_A_RAS_L<0>	PP8907	OMIT P4MM
90 89 88 5	DRAM_RST	PP8908	OMIT P4MM
89 87	FB_A_WDQS<0>	PP8909	OMIT P4MM
89 87	FB_A_WDQS<1>	PP8910	OMIT P4MM
89 87	FB_A_WDQS<3>	PP8911	OMIT P4MM
89 87	FB_A_WDQS<2>	PP8912	OMIT P4MM
89 87 5	FB_A_DQ<0>	PP8913	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8914	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8915	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8916	OMIT P4MM

PLACE NEAR U8950

89 87	FB_A_CKE<1>	PP8920	OMIT P4MM
89 87	FB_A_CLK_P<1>	PP8921	OMIT P4MM
89 87	FB_A_CLK_N<1>	PP8922	OMIT P4MM
89 87	FB_A_CS_L<1>	PP8923	OMIT P4MM
89 87	FB_A_WE_L<1>	PP8924	OMIT P4MM
89 87	FB_A_CAS_L<1>	PP8925	OMIT P4MM
89 87	FB_A_RAS_L<1>	PP8926	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8927	OMIT P4MM
90 89 88 5	DRAM_RST	PP8928	OMIT P4MM
89 87	FB_A_WDQS<5>	PP8929	OMIT P4MM
89 87	FB_A_WDQS<6>	PP8930	OMIT P4MM
89 87	FB_A_WDQS<4>	PP8931	OMIT P4MM
89 87	FB_A_WDQS<7>	PP8932	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8933	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8934	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8935	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8936	OMIT P4MM

PLACE NEAR U9000

90 87	FB_B_CKE<0>	PP9000	OMIT P4MM
90 87	FB_B_CLK_P<0>	PP9001	OMIT P4MM
90 87	FB_B_CLK_N<0>	PP9002	OMIT P4MM
90 87	FB_B_CS_L<0>	PP9003	OMIT P4MM
90 87	FB_B_WE_L<0>	PP9004	OMIT P4MM
90 87	FB_B_CAS_L<0>	PP9005	OMIT P4MM
90 87	FB_B_RAS_L<0>	PP9006	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9007	OMIT P4MM
90 89 88 5	DRAM_RST	PP9008	OMIT P4MM
90 87	FB_B_WDQS<0>	PP9009	OMIT P4MM
90 87	FB_B_WDQS<1>	PP9010	OMIT P4MM
90 87	FB_B_WDQS<3>	PP9011	OMIT P4MM
90 87	FB_B_WDQS<2>	PP9012	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP9013	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP9014	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP9015	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP9016	OMIT P4MM

PLACE NEAR U9050

90 87	FB_B_CKE<1>	PP9020	OMIT P4MM
90 87	FB_B_CLK_P<1>	PP9021	OMIT P4MM
90 87	FB_B_CLK_N<1>	PP9022	OMIT P4MM
90 87	FB_B_CS_L<1>	PP9023	OMIT P4MM
90 87	FB_B_WE_L<1>	PP9024	OMIT P4MM
90 87	FB_B_CAS_L<1>	PP9025	OMIT P4MM
90 87	FB_B_RAS_L<1>	PP9026	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9027	OMIT P4MM
90 89 88 5	DRAM_RST	PP9028	OMIT P4MM
90 87	FB_B_WDQS<5>	PP9029	OMIT P4MM
90 87	FB_B_WDQS<6>	PP9030	OMIT P4MM
90 87	FB_B_WDQS<7>	PP9031	OMIT P4MM
90 87	FB_B_WDQS<4>	PP9032	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP9033	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP9034	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP9035	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP9036	OMIT P4MM

PLACE NEAR R1210 AND R1211

12	NB_FSB_VREF	PP1200	SM-TP50-TOP
19 12 6	=PP1V05_S0_FSB_NB	PP1201	SM-TP50-TOP
		PP1202	SM-TP50-TOP

PLACE NEAR R0705 AND R0706

11 9 8 7 6	=PP1V05_S0_CPU	PP700	SM-TP50-TOP
7	CPU_GTLREF	PP701	SM-TP50-TOP
		PP702	SM-TP50-TOP

PLACE NEAR R2800 AND R2801

29 28 6	=PP1V8_S3_MEM	PP2800	SM-TP50-TOP
29 28	MEM_VREF	PP2801	SM-TP50-TOP
		PP2802	SM-TP50-TOP

77 76 66 65 59 26 11 6	PP3V3_S5	FUNC_TEST=TRUE
83 81 80 79 59 6	PP5V_S5	FUNC_TEST=TRUE
88 83 81 80 79 78 77 11 6	PP12V_S5	FUNC_TEST=TRUE
79 6	PP1V8_S3	FUNC_TEST=TRUE
76 75 6	PPVCORE_CPU	FUNC_TEST=TRUE
26 25 24 21	PP3V3_S5_S8_RTC	FUNC_TEST=TRUE
	8 TESTPOINTS	FUNC_TEST=TRUE

60 59 58	SMC_TCK	FUNC_TEST=TRUE
60 59 58	SMC_TDI	FUNC_TEST=TRUE
60 59 58	SMC_TDO	FUNC_TEST=TRUE
60 59 58	SMC_TMS	FUNC_TEST=TRUE
60 58	SMC_TRST_L	FUNC_TEST=TRUE
60 59 58	SMC_TX_L	FUNC_TEST=TRUE
60 59 58	SMC_RX_L	FUNC_TEST=TRUE
59	SMC_MANUAL_RST_L	FUNC_TEST=TRUE
11 7	XDP_TCK	FUNC_TEST=TRUE
11 7	XDP_TDI	FUNC_TEST=TRUE
11 7	XDP_TDO	FUNC_TEST=TRUE
11 7	XDP_TMS	FUNC_TEST=TRUE
11 7	XDP_TRST_L	FUNC_TEST=TRUE
59	POWER_BUTTON_L	FUNC_TEST=TRUE
26	SW_RST_BTN_L	FUNC_TEST=TRUE

34	TP_PCI_CLK_SPARE	NO_TEST=TRUE
29	TP_MEM_B_A<14>	NO_TEST=TRUE
29	TP_MEM_B_A<15>	NO_TEST=TRUE
43	ENET_MDI_R_N<0>	NO_TEST=TRUE
43	ENET_MDI_R_N<1>	NO_TEST=TRUE
43	ENET_MDI_R_N<2>	NO_TEST=TRUE
43	ENET_MDI_R_N<3>	NO_TEST=TRUE
43	ENET_MDI_R_P<0>	NO_TEST=TRUE
43	ENET_MDI_R_P<1>	NO_TEST=TRUE
43	ENET_MDI_R_P<2>	NO_TEST=TRUE
43	ENET_MDI_R_P<3>	NO_TEST=TRUE

MISC GROUND VIAS

ZH500	HOLE-VIA	ZH510	HOLE-VIA
ZH501	HOLE-VIA	ZH511	HOLE-VIA
ZH502	HOLE-VIA	ZH512	HOLE-VIA
ZH503	HOLE-VIA	ZH513	HOLE-VIA
ZH504	HOLE-VIA	ZH514	HOLE-VIA
ZH505	HOLE-VIA	ZH515	HOLE-VIA
ZH506	HOLE-VIA	ZH516	HOLE-VIA
ZH507	HOLE-VIA	ZH517	HOLE-VIA
ZH508	HOLE-VIA	ZH518	HOLE-VIA
ZH509	HOLE-VIA	ZH519	HOLE-VIA

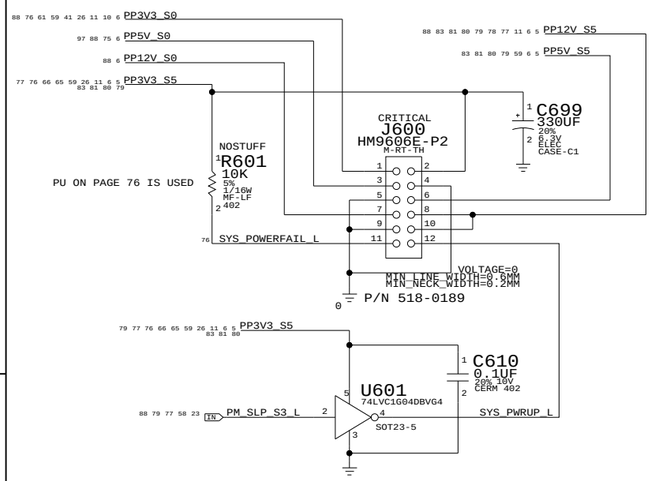
ZH520	HOLE-VIA	
ZH521	HOLE-VIA	
ZH522	HOLE-VIA	
ZH523	HOLE-VIA	
ZH524	HOLE-VIA	
ZH525	HOLE-VIA	
ZH526	HOLE-VIA	
ZH527	HOLE-VIA	
ZH528	HOLE-VIA	
ZH529	HOLE-VIA	

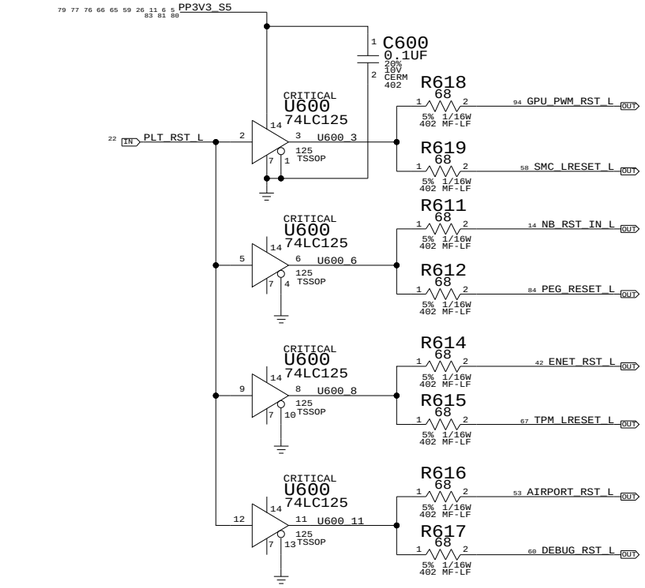
FUNC TEST 1 OF 2

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7148 | REV. 13

SCALE NONE | SHT 5 OF 110





"S0" RAILS

ONLY ON IN RUN

PP0V9_S0 (MAKE_BASE=TRUE, VOLTAGE=0.9V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM)
- =PP0V9_S0_MEMVTT_LDO 31
- =PP0V9_S0_MEM_TERM 30

PPVCORE_CPU (MAKE_BASE=TRUE, VOLTAGE=1.25V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
- =PPVCORE_S0_CPU 8 9

PP1V05_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM)
- =PPVCORE_S0_NB 16 19
- =PP1V05_S0_CPU 5 7 8 9 11
- =PP1V05_S0_FSB_NB 5 12 19
- =PP1V05_S0_NB_VTT 17 19
- =PP1V05_S0_NB 19
- =PP1V05_S0_SB_CPU_IO 21 24 25
- =PPVCORE_S0_SB 24 25

PP1V5_S0 (MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
- =PP1V5_S0_CPU 8
- =PP1V5_S0_NB_PCIE 13 19
- =PP1V5_S0_NB_VCCAUX 6 16 17 19
- =PP1V5_S0_NB_VCCD_HMPLL 17 19
- =PP1V5_S0_NB_VCCAUX 6 16 17 19
- =PP1V5_S0_NB_PLL 19
- =PP1V5_S0_NB 19
- =PP1V5_S0_NB_TVDAC 19
- =PP1V5_S0_NB_3GPLL 19
- =PP1V5_S0_SB_VCC1_5_A_ARX 24 25
- =PP1V5_S0_SB_VCCSATAPLL 24 25
- =PP1V5_S0_SB_VCC1_5_A_ATX 24 25
- =PP1V5_S0_SB_VCCUSBPLL 24 25
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE 24 25
- =PP1V5_S0_SB_VCC1_5_A 24 25
- =PP1V5_S0_SB 25
- =PP1V5_S0_AIRPORT 53

PP2V5_S0 (MAKE_BASE=TRUE, VOLTAGE=2.5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
- =PP2V5_S0_NB_VCCA_3GBG 17 19

PP3V3_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
- =PP3V3_S0_NB_PM
- =PP3V3_S0_NB_VCC_HV 17 19
- =PP3V3_S0_NB_TVDAC 19
- =PP3V3_S0_SB 22 25 27
- =PP3V3_S0_SB_GPIO 21 23
- =PP3V3_S0_SB_VCC3_3 24 25
- =PP3V3_S0_SB_VCC3_3_PCI 24 25
- =PP3V3_S0_SB_VCC3_3_IDE 24 25
- =PP3V3_S0_SB_PCI 26
- =PP3V3_S0_SB_PM 26
- =PP3V3_S0_PATA 38
- =PP3V3_S0_FAN 59 65 66
- =PP3V3_S0_HD_TSENS 66
- =PP3V3_S0_ODD_TSENS 66
- =PP3V3_S0_SB_3V3_1V5_VCCHDA 24 25
- =PP3V3_S0_TPM 67
- =PPSPD_S0_MEM 28 29
- =PP3V3_S0_CK410 33 34
- =PP3V3_S0_IMVP 75
- =PP3V3_S0_AUDIO 68 72 73 74
- =PP3V3_S0_PCI 44
- =PP3V3_S0_SB_VCCLAN3_3 24 25
- =PP3V3_S0_AIRPORT 53
- =PP3V3_S0_2V5REG 77
- =PP3V3_S0_NB 14 19 20

PP5V_S0 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
- =PP5V_S0_SB 25
- =PP5V_S0_PATA 38
- XW604 SM OMIT: PP5V_S0_AUDIO =PP5V_S0_AUDIO 68 (MAKE_BASE=TRUE)
- =PP5V_S0_DEBUG 60

PP12V_S0 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
- =PP12V_S0_FAN 65 66
- XW605 SM OMIT: PP12V_S0_AUDIO_SPKRAMP =PP12V_S0_AUDIO_SPKRAMP 72 (MAKE_BASE=TRUE)

"S3" RAILS

ON IN RUN AND SLEEP

PP1V2_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- =PP1V2_S3_LAN 42

PP1V8_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- =PP1V8_S3_MEM_NB 6 14 16 19
- =PP1V8_S3_MEM_NB 6 14 16 19
- =PP1V8_S3_MEM 5 28 29
- =PP1V8_S0_MEMVTT 31

PP3V3_S3 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
- =PP3V3_S3_ENET 41 42
- =PP3V3_S3_TPM 67
- =PP3V3_S3_1V2REG 77
- =PP3V3_S3_BT 47
- =PP3V3_S3_USB
- =PP3V3_S3_VGASYNC

PP5V_S3 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
- =PP5V_S3_USB 47
- =PP5V_S3_BNDI 47
- =PP5V_S0_MEMVTT 31

ZH704P1 — OMIT ZH604 4P25R3P5
ZH701P1 — OMIT ZH601 4P25R3P5
ZH702P1 — OMIT ZH602 4P25R3P5
ZH703P1 — OMIT ZH603 4P25R3P5

NOSTUFF C604 0.01UF 20% 16V CERM 402
NOSTUFF C601 0.01UF 20% 16V CERM 402
NOSTUFF C602 0.01UF 20% 16V CERM 402
NOSTUFF C603 0.01UF 20% 16V CERM 402

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP3V3_S5 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- =PP3V3_S5_SB 23 25 26
- =PP3V3_S5_SB_USB 22
- =PP3V3_S5_SB_PM 11 23
- =PP3V3_S5_SB_VCCSUS3_3 24 25
- =PP3V3_S5_SB_VCCSUS3_3_USB 24 25
- =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 24
- =PP3V3_S5_SB_IO 22 27
- =PP3V3_S5_FW 44 45 46
- =PP3V3_S5_SMC 58 59
- =PP3V3_S5_DEBUG 60
- =PP3V3_S5_ROM 63

PP5V_S5 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- =PP5V_S5_SB 25

PP12V_S5 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- =PP12V_S5_FW 46
- =PP12V_S5_CPU 76

GND RAILS

XW601 SM NOSTUFF — GND_AUDIO
XW602 SM NOSTUFF — GND_AUDIO_SPKRAMP

CHASSIS GND

NOSTUFF R603 0 5% 1/10W MF-LF 402

GND_CHASSIS_IO_LEFT (MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- GND_CHASSIS_AUDIO_EXTERNAL 73
- GND_CHASSIS_USB 47

GND_CHASSIS_IO_RIGHT (MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- GND_CHASSIS_FIREWIRE 46
- GND_CHASSIS_VGA 97
- GND_CHASSIS_RJ45 43

OMIT ZH606 160R138
- GND_CHASSIS_AUDIO_INTERNAL 73
- GND_CHASSIS_BNDI 47

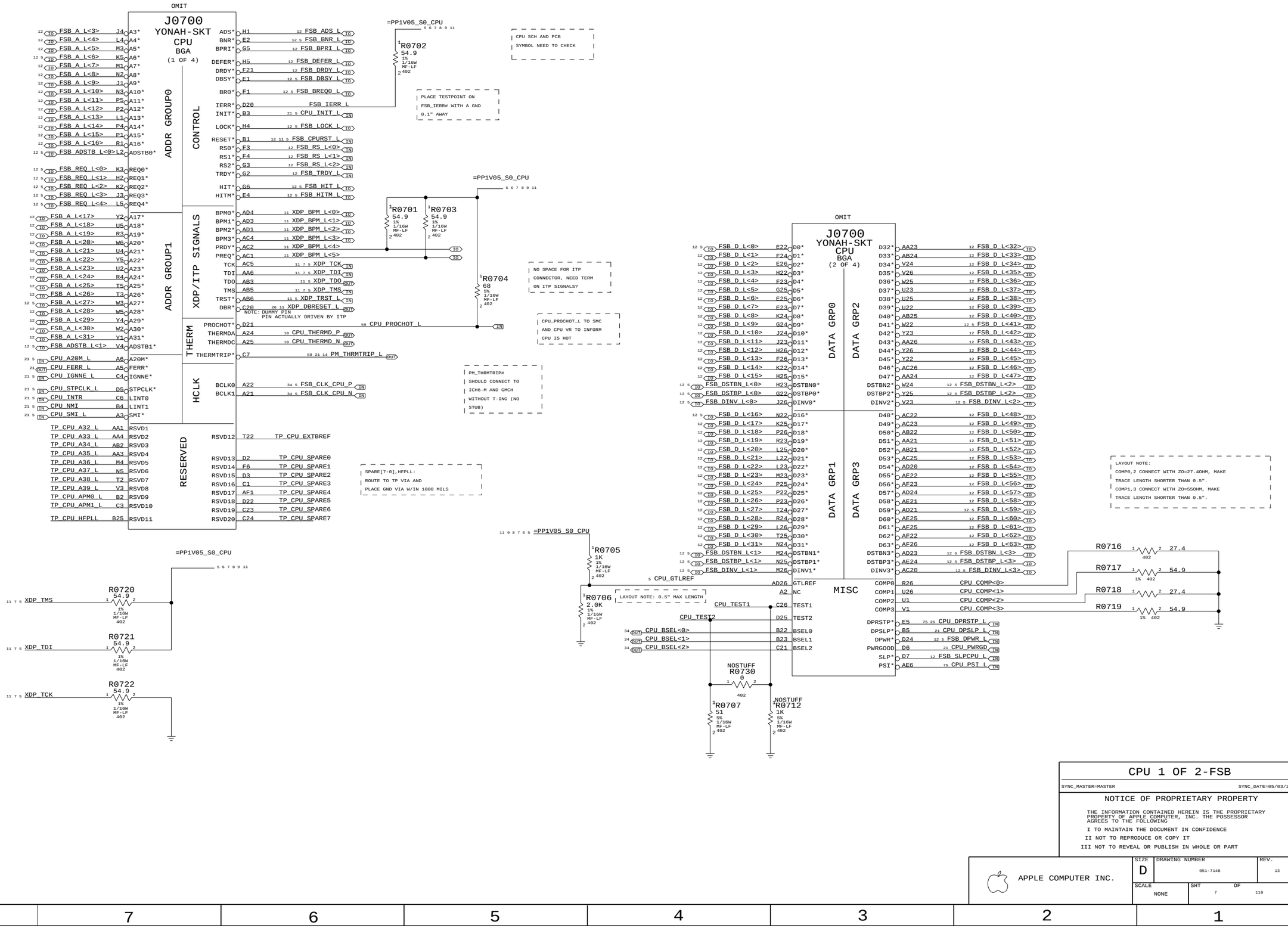
(MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0, MAKE_BASE=TRUE)

Power Conn / Alias

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 6 OF 110	



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 7	OF 110

=PPVCORE_S0_CPU 6 8 9

OMIT

J0700 YONAH-SKT CPU BGA (3 OF 4)

A7	VCC_1	VCC_68	AB20
A9	VCC_2	VCC_69	AB7
A10	VCC_3	VCC_70	AC7
A12	VCC_4	VCC_71	AC9
A13	VCC_5	VCC_72	AC12
A15	VCC_6	VCC_73	AC13
A17	VCC_7	VCC_74	AC15
A18	VCC_8	VCC_75	AC17
A20	VCC_9	VCC_76	AC18
B7	VCC_10	VCC_77	AD7
B9	VCC_11	VCC_78	AD9
B10	VCC_12	VCC_79	AD10
B12	VCC_13	VCC_80	AD12
B14	VCC_14	VCC_81	AD14
B15	VCC_15	VCC_82	AD15
B17	VCC_16	VCC_83	AD17
B18	VCC_17	VCC_84	AD18
B20	VCC_18	VCC_85	AE9
C9	VCC_19	VCC_86	AE10
C10	VCC_20	VCC_87	AE12
C12	VCC_21	VCC_88	AE13
C13	VCC_22	VCC_89	AE15
C15	VCC_23	VCC_90	AE17
C17	VCC_24	VCC_91	AE18
C18	VCC_25	VCC_92	AE20
D9	VCC_26	VCC_93	AF9
D10	VCC_27	VCC_94	AF10
D12	VCC_28	VCC_95	AF12
D14	VCC_29	VCC_96	AF14
D15	VCC_30	VCC_97	AF15
D17	VCC_31	VCC_98	AF17
D18	VCC_32	VCC_99	AF18
E7	VCC_33	VCC_100	AF20
E9	VCC_34		
E10	VCC_35	VCCP_1	V6
E12	VCC_36	VCCP_2	G21
E13	VCC_37	VCCP_3	J6
E15	VCC_38	VCCP_4	K6
E17	VCC_39	VCCP_5	M6
E18	VCC_40	VCCP_6	J21
E20	VCC_41	VCCP_7	K21
F7	VCC_42	VCCP_8	M21
F9	VCC_43	VCCP_9	N21
F10	VCC_44	VCCP_10	N6
F12	VCC_45	VCCP_11	R21
F14	VCC_46	VCCP_12	R6
F15	VCC_47	VCCP_13	T21
F17	VCC_48	VCCP_14	T6
F18	VCC_49	VCCP_15	V21
F20	VCC_50	VCCP_16	W21
AA7	VCC_51		
AA9	VCC_52		
AA10	VCC_53		
AA12	VCC_54		
AA13	VCC_55		
AA15	VCC_56		
AA17	VCC_57		
AA18	VCC_58		
AA20	VCC_59		
AB9	VCC_60		
AC10	VCC_61		
AB10	VCC_62		
AB12	VCC_63		
AB14	VCC_64		
AB15	VCC_65		
AB17	VCC_66		
AB18	VCC_67		

=PPVCORE_S0_CPU 6 8 9

=PP1V05_S0_CPU 5 6 7 9 11

=PP1V5_S0_CPU 6 8

VCCA=1.5 ONLY

VCCA	B26	
VID0	AD6	75 CPU_VID<0> OUT
VID1	AF5	75 CPU_VID<1> OUT
VID2	AE5	75 CPU_VID<2> OUT
VID3	AF4	75 CPU_VID<3> OUT
VID4	AE3	75 CPU_VID<4> OUT
VID5	AF2	75 CPU_VID<5> OUT
VID6	AE2	75 CPU_VID<6> OUT
VCCSENSE	AF7	75 CPU_VCCSENSE_P OUT
VSSSENSE	AE7	75 CPU_VCCSENSE_N OUT

=PPVCORE_S0_CPU 6 8 9

R0802 100 1% 1/16W MF-LF 402

R0803 100 1% 1/16W MF-LF 402

LAYOUT NOTE: CONNECT R0802-03 TO VCCSENSE_P/N WITH NO STUB

LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENCTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE AT THE
LOCATION WHERE THE TWO 54.9 OHM
RESISTORS TERMINATE THE 55 OHM
TRANSMISSION LINE

=PP1V5_S0_CPU 6 8

C0800 0.01UF 20% 16V CERM 402

C0801 10UF 20% 6.3V X5R 603

OMIT

J0700 YONAH-SKT CPU BGA (4 OF 4)

A4	VSS_1	VSS_82	P6
A8	VSS_2	VSS_83	P21
A11	VSS_3	VSS_84	P24
A14	VSS_4	VSS_85	R2
A16	VSS_5	VSS_86	R5
A19	VSS_6	VSS_87	R22
A23	VSS_7	VSS_88	R25
A26	VSS_8	VSS_89	T1
B6	VSS_9	VSS_90	T4
B8	VSS_10	VSS_91	T23
B11	VSS_11	VSS_92	T26
B13	VSS_12	VSS_93	U3
B16	VSS_13	VSS_94	U6
B19	VSS_14	VSS_95	U21
B21	VSS_15	VSS_96	U24
B24	VSS_16	VSS_97	V2
C5	VSS_17	VSS_98	V5
C8	VSS_18	VSS_99	V22
C11	VSS_19	VSS_100	V25
C14	VSS_20	VSS_101	W1
C16	VSS_21	VSS_102	W4
C19	VSS_22	VSS_103	W23
C2	VSS_23	VSS_104	W26
C22	VSS_24	VSS_105	Y3
C25	VSS_25	VSS_106	Y6
D1	VSS_26	VSS_107	Y21
D4	VSS_27	VSS_108	Y24
D8	VSS_28	VSS_109	AA2
D11	VSS_29	VSS_110	AA5
D13	VSS_30	VSS_111	AA8
D16	VSS_31	VSS_112	AA11
D19	VSS_32	VSS_113	AA14
D23	VSS_33	VSS_114	AA16
D26	VSS_34	VSS_115	AA19
E3	VSS_35	VSS_116	AA22
E6	VSS_36	VSS_117	AA25
E8	VSS_37	VSS_118	AB1
E11	VSS_38	VSS_119	AB4
E14	VSS_39	VSS_120	AB8
E16	VSS_40	VSS_121	AB11
E19	VSS_41	VSS_122	AB13
E21	VSS_42	VSS_123	AB16
E24	VSS_43	VSS_124	AB19
F5	VSS_44	VSS_125	AB23
F8	VSS_45	VSS_126	AB26
F11	VSS_46	VSS_127	AC3
F13	VSS_47	VSS_128	AC6
F16	VSS_48	VSS_129	AC8
F19	VSS_49	VSS_130	AC11
F2	VSS_50	VSS_131	AC14
F22	VSS_51	VSS_132	AC16
F25	VSS_52	VSS_133	AC19
G4	VSS_53	VSS_134	AC21
G1	VSS_54	VSS_135	AC24
G23	VSS_55	VSS_136	AD2
G26	VSS_56	VSS_137	AD5
H3	VSS_57	VSS_138	AD8
H6	VSS_58	VSS_139	AD11
H21	VSS_59	VSS_140	AD13
H24	VSS_60	VSS_141	AD16
J2	VSS_61	VSS_142	AD19
J5	VSS_62	VSS_143	AD22
J22	VSS_63	VSS_144	AD25
J25	VSS_64	VSS_145	AE1
K1	VSS_65	VSS_146	AE4
K4	VSS_66	VSS_147	AE8
K23	VSS_67	VSS_148	AE11
K26	VSS_68	VSS_149	AE14
L3	VSS_69	VSS_150	AE16
L6	VSS_70	VSS_151	AE19
L21	VSS_71	VSS_152	AE23
L24	VSS_72	VSS_153	AE26
M2	VSS_73	VSS_154	AF3
M5	VSS_74	VSS_155	AF6
M22	VSS_75	VSS_156	AF8
M25	VSS_76	VSS_157	AF11
N1	VSS_77	VSS_158	AF13
N4	VSS_78	VSS_159	AF16
N23	VSS_79	VSS_160	AF19
N26	VSS_80	VSS_161	AF21
P3	VSS_81	VSS_162	AF24

CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER

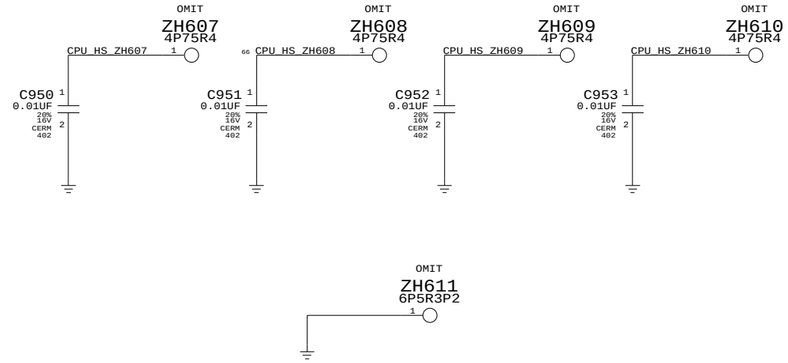
SYNC_DATE=05/03/2005

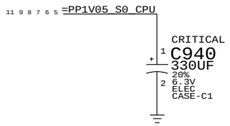
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

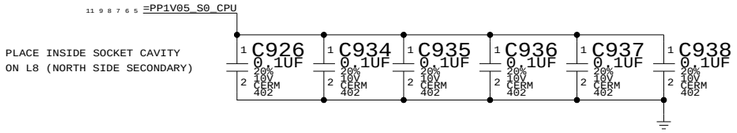
SCALE	SHT	OF
NONE	8	110

CPU HEATSINK MOUNTING HOLES

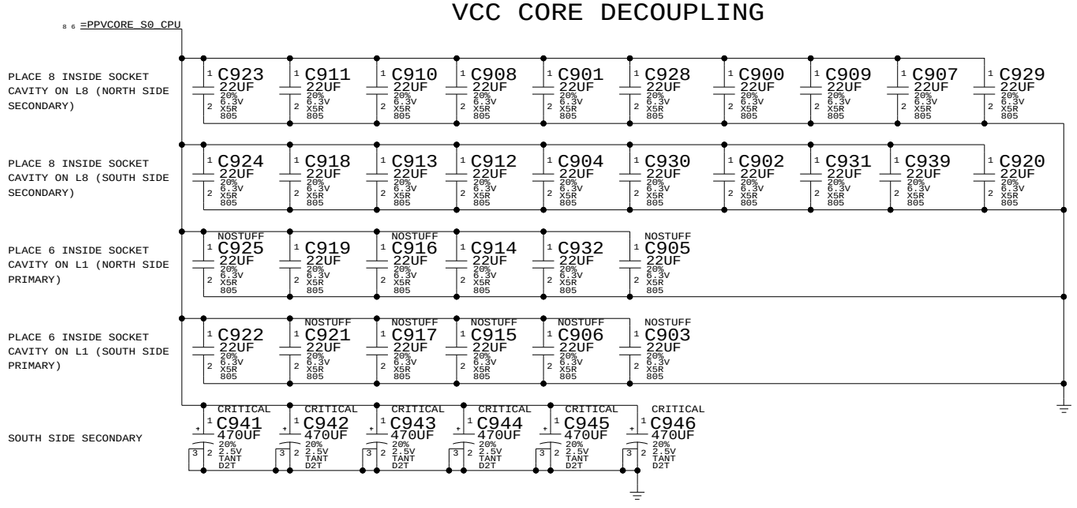




VCCP CORE DECOUPLING



VCC CORE DECOUPLING



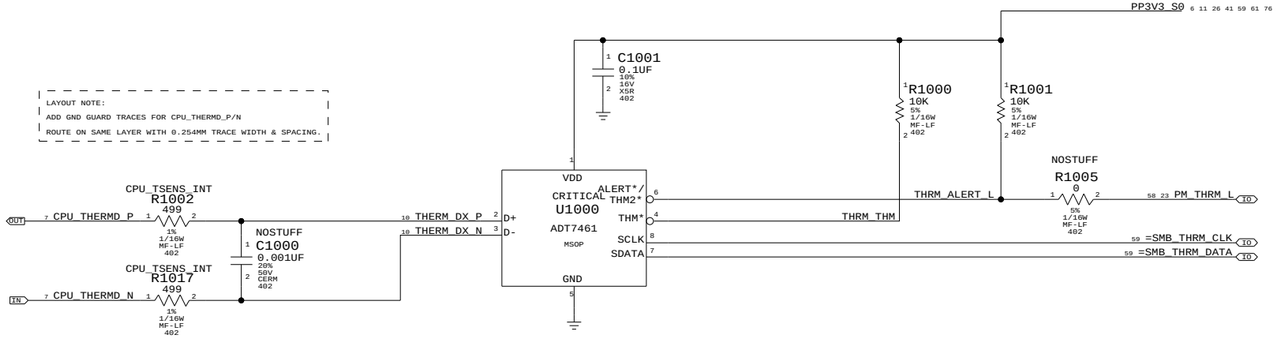
CPU DECAPS & VID<>

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 9 OF 110	

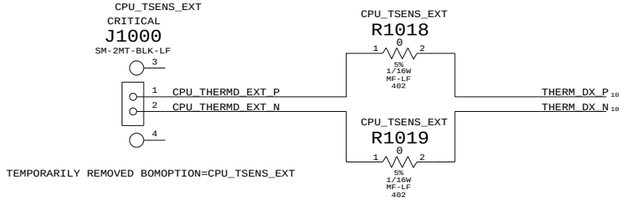
CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

CPU TEMP SENSOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	10	110

CPU ITP700FLEX DEBUG SUPPORT

C1150 0.1UF 10% 16V X5R 402 — PP3V3_S5 — PP12V_S5
C1151 0.1UF 10% 16V X5R 402
C1152 0.1UF 10% 16V X5R 402

C1153 0.1UF 10% 16V X5R 402 — PP2V5_S0 — PP12V_S5
C1154 0.1UF 10% 16V X5R 402
C1155 0.1UF 10% 16V X5R 402

C1156 0.1UF 10% 16V X5R 402 — PP3V3_S0 — PP1V5_S0
C1157 0.1UF 10% 16V X5R 402

C1158 0.1UF 10% 16V X5R 402 — PP2V5_S0 — PP1V5_S0
C1159 0.1UF 10% 16V X5R 402

C1160 0.1UF 10% 16V X5R 402 — PP12V_S5 — PP1V5_S0

=PP1V05_S0_CPU
R1101 54.9 1% 1/16W MF-LF 402
R1103 54.9 1% 1/16W MF-LF 402
R1102 22.6 1% 1/16W MF-LF 402 — XDP_TDO
R1100 22.6 1% 1/16W MF-LF 402 — FSB_CPURST_L

=PP3V3_S5_SB_PM
R1104 240 5% 1/16W MF-LF 402

(AND WITH RESET BUTTON)

XDP_DBRESET_L

(FROM CK410M HOST 133/167MHZ)

DEVELOPMENT
J1101 52435-2872 F-RT-SM

XDP_TDI	1	
XDP_TMS	2	
XDP_TRST_L	3	
XDP_TCK (TCK)	4	
NC	5	
NC	6	
ITP_TDO	7	
CPU_XDP_CLK_N	8	
CPU_XDP_CLK_P	9	
XDP_TCK (FBO)	10	
ITPRESET_L	11	
XDP_BPM_L<5>	12	
XDP_BPM_L<4>	13	
XDP_BPM_L<3>	14	
XDP_BPM_L<2>	15	
XDP_BPM_L<1>	16	
XDP_BPM_L<0>	17	
NC	18	
=PP1V05_S0_CPU	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	

518S0320

C1100 0.1UF 10% 16V X5R 402

R1106 680 5% 1/16W MF-LF 402

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM. (DEBUG PORT ACTIVE)
(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC (DEBUG PORT RESET)

NOTE: PLACE C1199 AT J1101 PINS 13 AND 14

XDP_BPM_L<5>

NOSTUFF C1199 56PF 5% 50V CERM 402

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

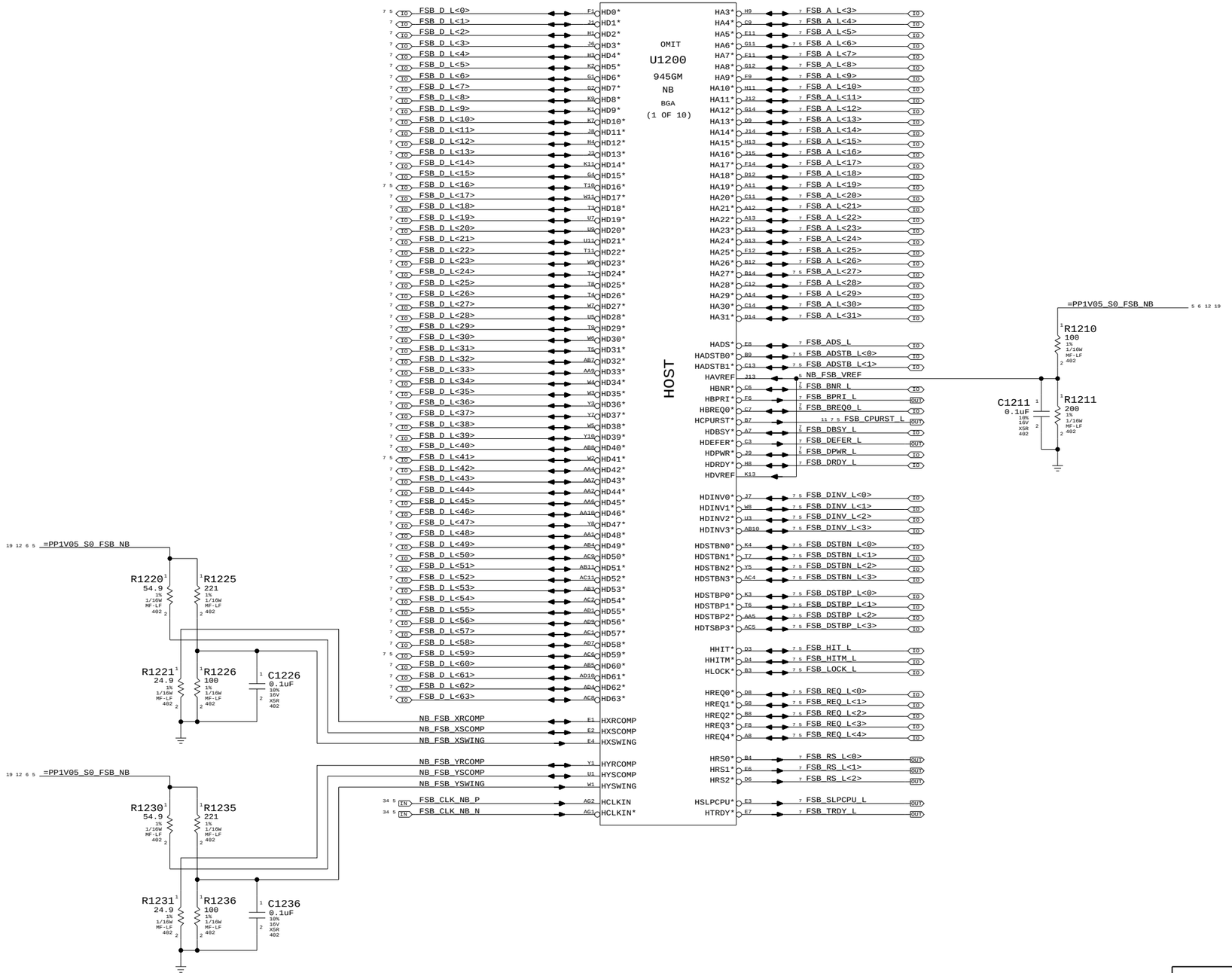
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	11	110



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	12	110

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

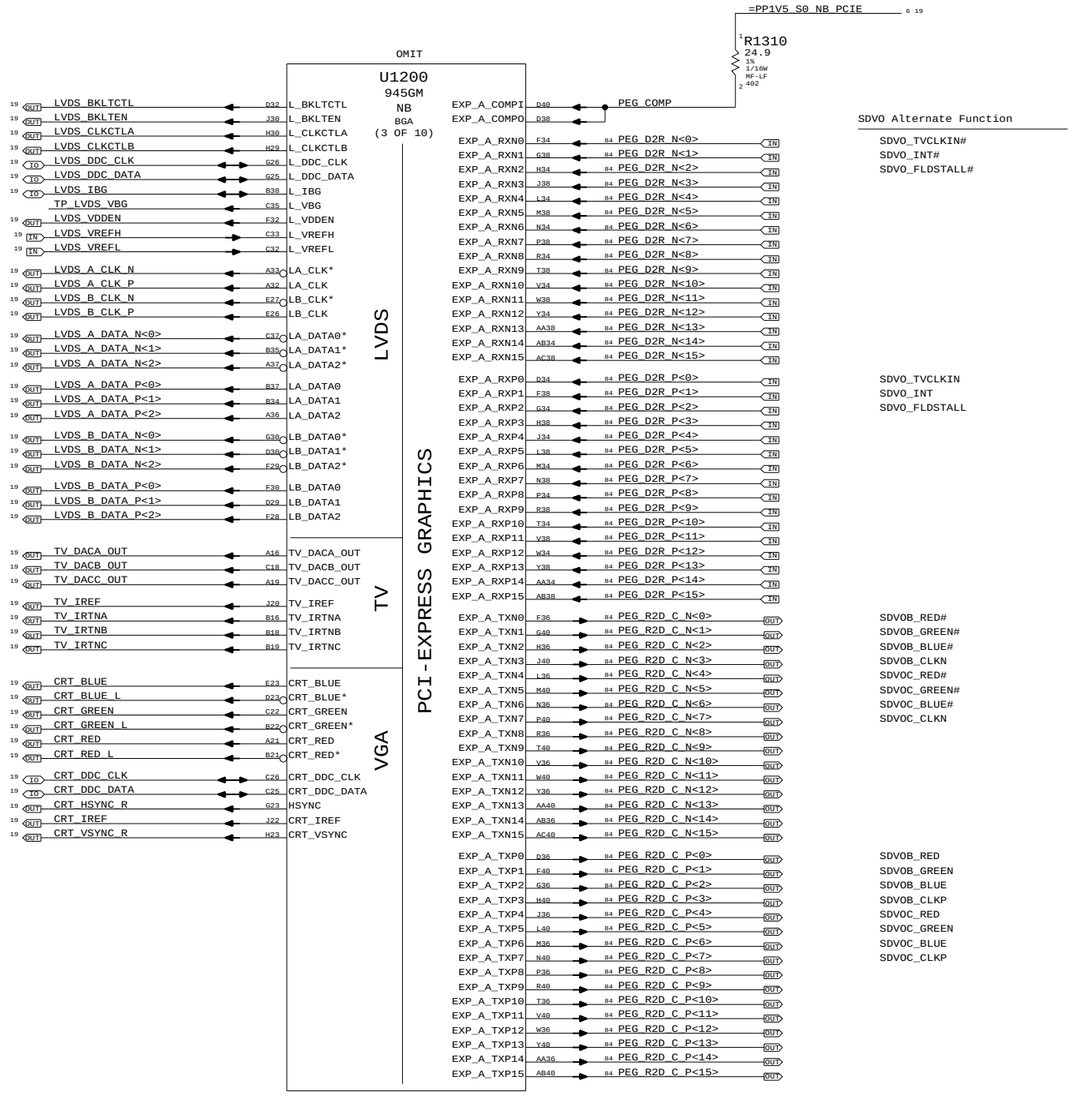
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



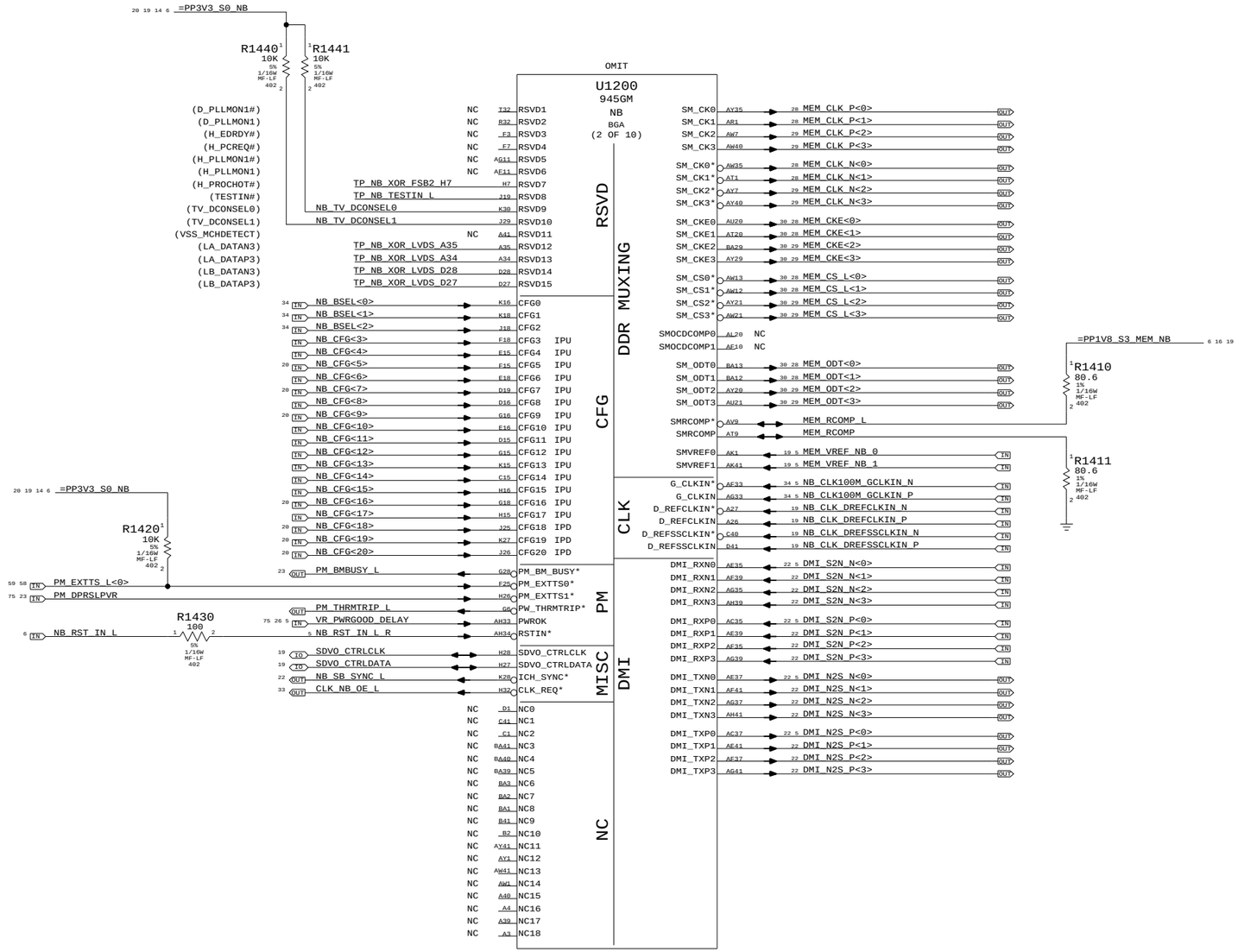
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	13	110

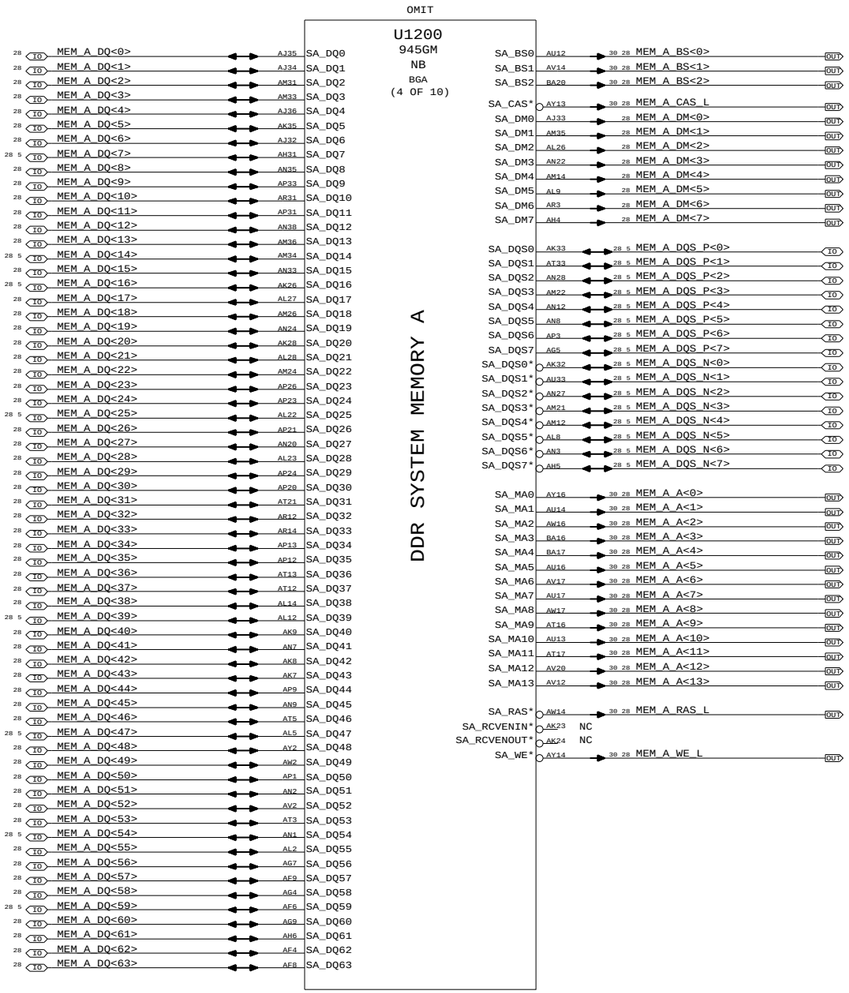


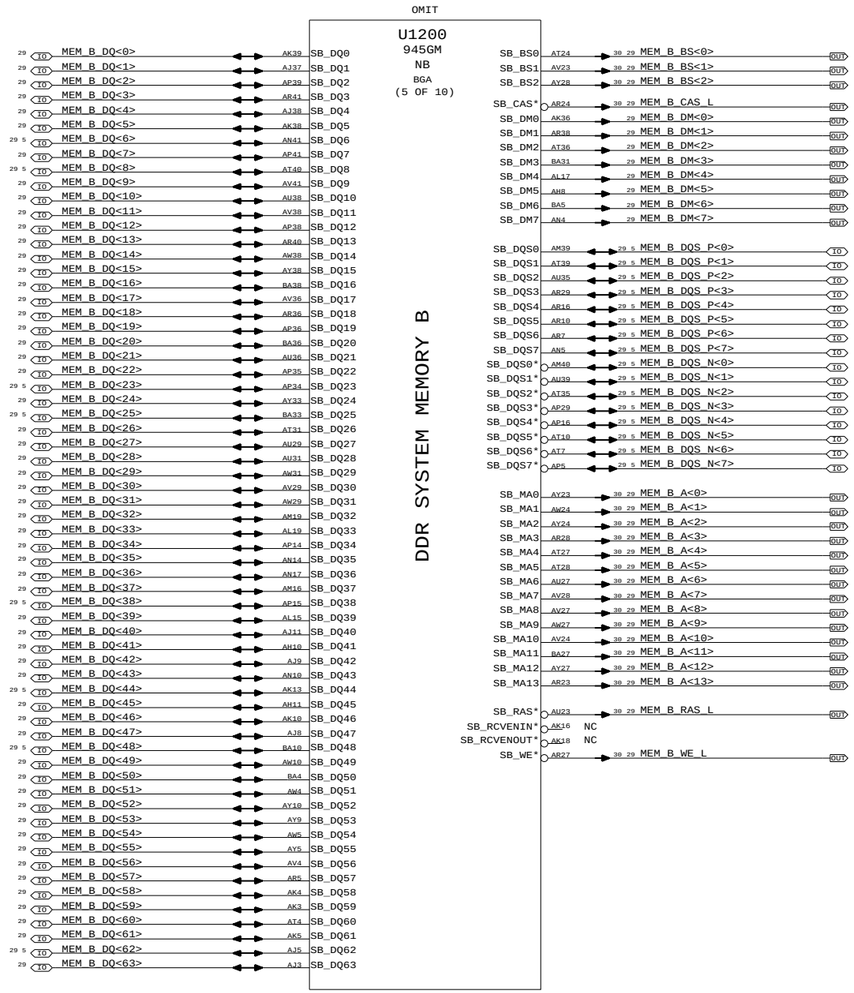
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 14 OF 110	





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE: NONE

SHT 15 OF 110

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 19 16 6

OMIT

U1200
945GM
NB
BGA
(7 OF 10)

NCTF

AD27	VCC_NCTF0	VSS_NCTF0	AE27
AC27	VCC_NCTF1	VSS_NCTF1	AE26
AB27	VCC_NCTF2	VSS_NCTF2	AE25
AA27	VCC_NCTF3	VSS_NCTF3	AE24
Y27	VCC_NCTF4	VSS_NCTF4	AE23
W27	VCC_NCTF5	VSS_NCTF5	AE22
V27	VCC_NCTF6	VSS_NCTF6	AE21
U27	VCC_NCTF7	VSS_NCTF7	AE20
T27	VCC_NCTF8	VSS_NCTF8	AE19
R27	VCC_NCTF9	VSS_NCTF9	AE18
AD26	VCC_NCTF10	VSS_NCTF10	AC17
AC26	VCC_NCTF11	VSS_NCTF11	Y17
AB26	VCC_NCTF12	VSS_NCTF12	U17
AA26	VCC_NCTF13		
Y26	VCC_NCTF14		
W26	VCC_NCTF15		
V26	VCC_NCTF16		
U26	VCC_NCTF17		
T26	VCC_NCTF18		
R26	VCC_NCTF19		
AD25	VCC_NCTF20		
AC25	VCC_NCTF21		
AB25	VCC_NCTF22		
AA25	VCC_NCTF23		
Y25	VCC_NCTF24		
W25	VCC_NCTF25		
V25	VCC_NCTF26		
U25	VCC_NCTF27		
T25	VCC_NCTF28		
R25	VCC_NCTF29		
AD24	VCC_NCTF30		
AC24	VCC_NCTF31		
AB24	VCC_NCTF32		
AA24	VCC_NCTF33		
Y24	VCC_NCTF34		
W24	VCC_NCTF35		
V24	VCC_NCTF36		
U24	VCC_NCTF37		
T24	VCC_NCTF38		
R24	VCC_NCTF39		
AD23	VCC_NCTF40		
V23	VCC_NCTF41		
U23	VCC_NCTF42		
T23	VCC_NCTF43		
R23	VCC_NCTF44		
AD22	VCC_NCTF45		
V22	VCC_NCTF46		
U22	VCC_NCTF47		
T22	VCC_NCTF48		
R22	VCC_NCTF49		
AD21	VCC_NCTF50		
V21	VCC_NCTF51		
U21	VCC_NCTF52		
T21	VCC_NCTF53		
R21	VCC_NCTF54		
AD20	VCC_NCTF55		
V20	VCC_NCTF56		
U20	VCC_NCTF57		
T20	VCC_NCTF58		
R20	VCC_NCTF59		
AD19	VCC_NCTF60		
V19	VCC_NCTF61		
U19	VCC_NCTF62		
T19	VCC_NCTF63		
AD18	VCC_NCTF64		
AC18	VCC_NCTF65		
AB18	VCC_NCTF66		
AA18	VCC_NCTF67		
Y18	VCC_NCTF68		
W18	VCC_NCTF69		
V18	VCC_NCTF70		
U18	VCC_NCTF71		
T18	VCC_NCTF72		

=PP1V5_S0_NB_VCCAUX 6 17 19

		VCCAUX_NCTF0	AG27
		VCCAUX_NCTF1	AF27
		VCCAUX_NCTF2	AG26
		VCCAUX_NCTF3	AF26
		VCCAUX_NCTF4	AG25
		VCCAUX_NCTF5	AF25
		VCCAUX_NCTF6	AG24
		VCCAUX_NCTF7	AF24
		VCCAUX_NCTF8	AG23
		VCCAUX_NCTF9	AF23
		VCCAUX_NCTF10	AG22
		VCCAUX_NCTF11	AF22
		VCCAUX_NCTF12	AG21
		VCCAUX_NCTF13	AF21
		VCCAUX_NCTF14	AG20
		VCCAUX_NCTF15	AF20
		VCCAUX_NCTF16	AG19
		VCCAUX_NCTF17	AF19
		VCCAUX_NCTF18	R19
		VCCAUX_NCTF19	AG18
		VCCAUX_NCTF20	AF18
		VCCAUX_NCTF21	R18
		VCCAUX_NCTF22	AG17
		VCCAUX_NCTF23	AF17
		VCCAUX_NCTF24	AE17
		VCCAUX_NCTF25	AD17
		VCCAUX_NCTF26	AB17
		VCCAUX_NCTF27	AA17
		VCCAUX_NCTF28	W17
		VCCAUX_NCTF29	V17
		VCCAUX_NCTF30	T17
		VCCAUX_NCTF31	R17
		VCCAUX_NCTF32	AG16
		VCCAUX_NCTF33	AF16
		VCCAUX_NCTF34	AE16
		VCCAUX_NCTF35	AD16
		VCCAUX_NCTF36	AC16
		VCCAUX_NCTF37	AB16
		VCCAUX_NCTF38	AA16
		VCCAUX_NCTF39	Y16
		VCCAUX_NCTF40	W16
		VCCAUX_NCTF41	V16
		VCCAUX_NCTF42	U16
		VCCAUX_NCTF43	T16
		VCCAUX_NCTF44	R16
		VCCAUX_NCTF45	AG15
		VCCAUX_NCTF46	AF15
		VCCAUX_NCTF47	AE15
		VCCAUX_NCTF48	AD15
		VCCAUX_NCTF49	AC15
		VCCAUX_NCTF50	AB15
		VCCAUX_NCTF51	AA15
		VCCAUX_NCTF52	Y15
		VCCAUX_NCTF53	W15
		VCCAUX_NCTF54	V15
		VCCAUX_NCTF55	U15
		VCCAUX_NCTF56	T15
		VCCAUX_NCTF57	R15

=PPVCORE_S0_NB 6 16 19

1.05V or 1.5V

U1200
945GM
NB
BGA
(6 OF 10)

OMIT

VCC

AA33	VCC_0	VCC_SM0	AU41
AK33	VCC_1	VCC_SM1	AT41
P33	VCC_2	VCC_SM2	AM41
N33	VCC_3	VCC_SM3	AU40
L33	VCC_4	VCC_SM4	BA34
J33	VCC_5	VCC_SM5	AT34
AA32	VCC_6	VCC_SM6	AH34
Y32	VCC_7	VCC_SM7	AV34
W32	VCC_8	VCC_SM8	AU34
V32	VCC_9	VCC_SM9	AT34
P32	VCC_10	VCC_SM10	AR34
N32	VCC_11	VCC_SM11	BA30
M32	VCC_12	VCC_SM12	AY30
L32	VCC_13	VCC_SM13	AW30
J32	VCC_14	VCC_SM14	AV30
AA31	VCC_15	VCC_SM15	AU30
W31	VCC_16	VCC_SM16	AT30
V31	VCC_17	VCC_SM17	AR30
T31	VCC_18	VCC_SM18	AP30
R31	VCC_19	VCC_SM19	AN30
P31	VCC_20	VCC_SM20	AM30
N31	VCC_21	VCC_SM21	AM29
AA30	VCC_22	VCC_SM22	AL29
W30	VCC_23	VCC_SM23	AK29
V30	VCC_24	VCC_SM24	AJ29
U30	VCC_25	VCC_SM25	AH29
T30	VCC_26	VCC_SM26	AJ28
R30	VCC_27	VCC_SM27	AH28
P30	VCC_28	VCC_SM28	AJ27
N30	VCC_29	VCC_SM29	AH27
M30	VCC_30	VCC_SM30	BA26
L30	VCC_31	VCC_SM31	AY26
AA29	VCC_32	VCC_SM32	AW26
V29	VCC_33	VCC_SM33	AU26
U29	VCC_34	VCC_SM34	AT26
M29	VCC_35	VCC_SM35	AR26
V29	VCC_36	VCC_SM36	AJ26
U29	VCC_37	VCC_SM37	AH26
P29	VCC_38	VCC_SM38	AJ25
M29	VCC_39	VCC_SM39	AH25
L29	VCC_40	VCC_SM40	AJ24
AB28	VCC_41	VCC_SM41	AH24
AA28	VCC_42	VCC_SM42	BA23
Y28	VCC_43	VCC_SM43	BA22
V28	VCC_44	VCC_SM44	AJ23
U28	VCC_45	VCC_SM45	AY22
T28	VCC_46	VCC_SM46	AW22
R28	VCC_47	VCC_SM47	AV22
P28	VCC_48	VCC_SM48	AU22
N28	VCC_49	VCC_SM49	AT22
M28	VCC_50	VCC_SM50	AR22
L28	VCC_51	VCC_SM51	AP22
P27	VCC_52	VCC_SM52	AK22
N27	VCC_53	VCC_SM53	AJ22
M27	VCC_54	VCC_SM54	AK21
L27	VCC_55	VCC_SM55	AK20
P26	VCC_56	VCC_SM56	BA19
N26	VCC_57	VCC_SM57	AY19
L26	VCC_58	VCC_SM58	AW19
M25	VCC_59	VCC_SM59	AV19
L25	VCC_60	VCC_SM60	AT19
P24	VCC_61	VCC_SM61	AU19
M24	VCC_62	VCC_SM62	AR19
L24	VCC_63	VCC_SM63	AP19
AB23	VCC_64	VCC_SM64	AK19
AA23	VCC_65	VCC_SM65	AJ19
Y23	VCC_66	VCC_SM66	AJ18
P23	VCC_67	VCC_SM67	AH18
M23	VCC_68	VCC_SM68	AJ17
L23	VCC_69	VCC_SM69	AH17
AC22	VCC_70	VCC_SM70	AJ16
AB22	VCC_71	VCC_SM71	AH16
Y22	VCC_72	VCC_SM72	BA15
P22	VCC_73	VCC_SM73	AY15
M22	VCC_74	VCC_SM74	AW15
L22	VCC_75	VCC_SM75	AV15
AC21	VCC_76	VCC_SM76	AU15
AA21	VCC_77	VCC_SM77	AT15
V21	VCC_78	VCC_SM78	AR15
N21	VCC_79	VCC_SM79	AJ15
L21	VCC_80	VCC_SM80	AJ14
AC20	VCC_81	VCC_SM81	AJ13
AB20	VCC_82	VCC_SM82	AH13
Y20	VCC_83	VCC_SM83	AK12
P20	VCC_84	VCC_SM84	AJ12
M20	VCC_85	VCC_SM85	AH12
L20	VCC_86	VCC_SM86	AG12
AB19	VCC_87	VCC_SM87	AK11
AA19	VCC_88	VCC_SM88	BA9
Y19	VCC_89	VCC_SM89	AY9
M19	VCC_90	VCC_SM90	AW9
L19	VCC_91	VCC_SM91	AV9
P19	VCC_92	VCC_SM92	AU9
M19	VCC_93	VCC_SM93	AT9
L18	VCC_94	VCC_SM94	AR9
AB19	VCC_95	VCC_SM95	BA6
AA19	VCC_96	VCC_SM96	AY6
Y19	VCC_97	VCC_SM97	AW6
M19	VCC_98	VCC_SM98	AV6
L19	VCC_99	VCC_SM99	AT6
R18	VCC_100	VCC_SM100	AM6
L18	VCC_101	VCC_SM101	AP6
P17	VCC_102	VCC_SM102	AN6
N17	VCC_103	VCC_SM103	AL6
M17	VCC_104	VCC_SM104	AK6
N16	VCC_105	VCC_SM105	AJ6
L16	VCC_106	VCC_SM106	AV1
	VCC_107	VCC_SM107	AJ1
	VCC_108		
	VCC_109		
	VCC_110		

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 1 2 0.47UF 10% 6.3V CERM-X5R 402

C1613 1 2 0.47UF 10% 6.3V CERM-X5R 402

C1615 1 2 0.47UF 10% 6.3V CERM-X5R 402

Layout Note:
Place near pin BA23

19 14 6 =PP1V8_S3_MEM_NB

C1620 1 2 10UF 20% 6.3V CERM 805-1

C1621 1 2 10UF 20% 6.3V CERM 805-1

Layout Note:
Place in cavity
(Need to better define cavity)

C1610 1 2 0.47UF 10% 6.3V CERM-X5R 402

Layout Note:
Place near pin BA15

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 1 2 0.47UF 10% 6.3V CERM-X5R 402

C1611 1 2 0.47UF 10% 6.3V CERM-X5R 402

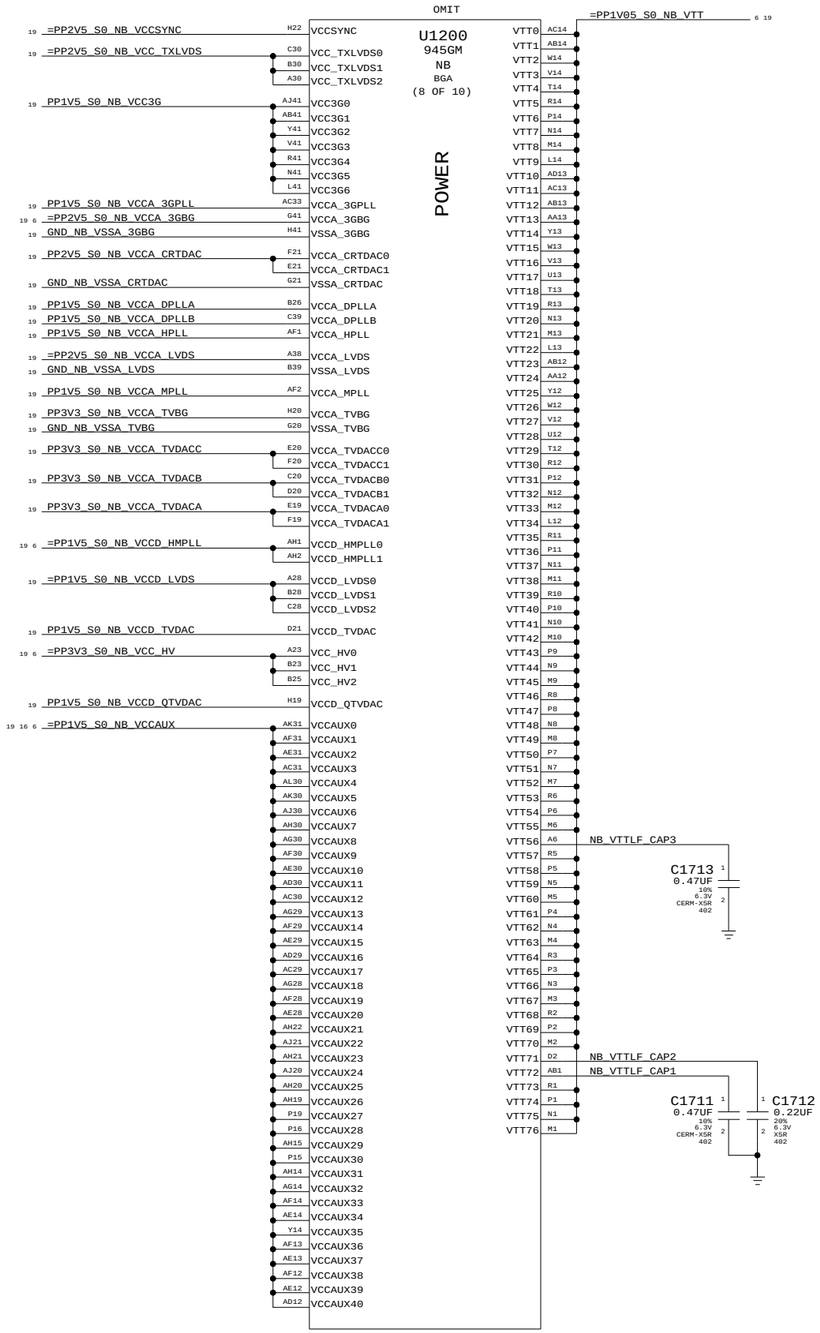
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	16	110



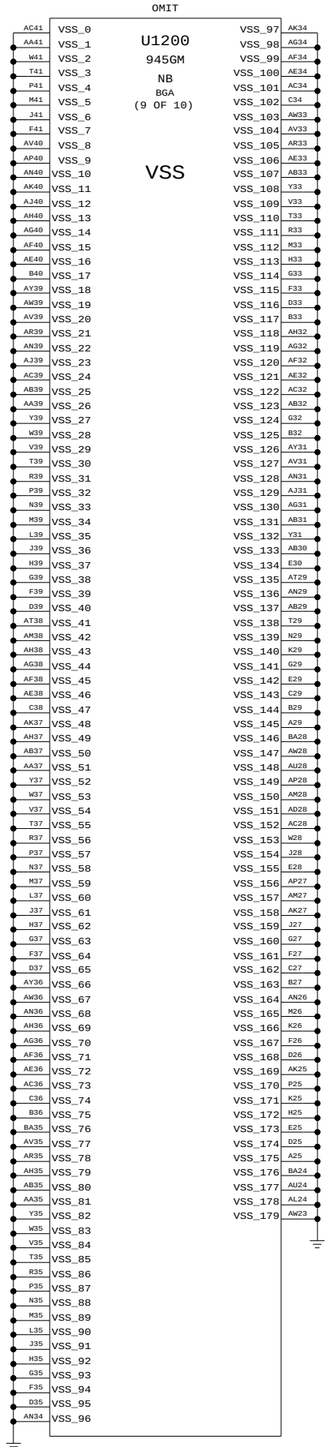
NB Power 2

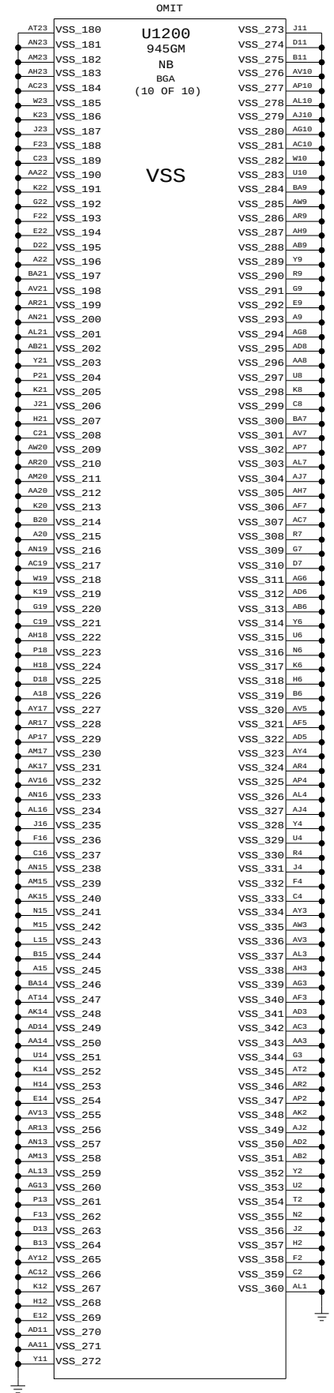
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	17	110





NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	18	110

Power Interface

These are the power signals that leave the NB "block"

=PP1V05_S0_FSB_NB — 5 6 12
=PPVCORE_S0_NB — 6 16 19
=PP1V05_S0_NB — 6
=PP1V05_S0_NB_VTT — 6 17 19
=PP1V5_S0_NB — 6 19
=PP1V5_S0_NB_PCIE — 6 13
=PP1V5_S0_NB_PLL — 6 19
=PP1V5_S0_NB_TVDAC — 6 19
=PP1V5_S0_NB_VCCD_HMPLL — 6 17
=PP1V5_S0_NB_VCCD_LVDS — 17 19
=PP1V5_S0_NB_VCCAUX — 6 16 17 19
=PP1V8_S3_MEM_NB — 6 14 16 19

=PP2V5_S0_NB_VCCSYNC — 17 19
=PP2V5_S0_NB_VCC_TXLVDS — 17 19
=PP2V5_S0_NB_VCCA_3GBG — 6 17 19
=PP2V5_S0_NB_VCCA_LVDS — 17 19

=PP3V3_S0_NB — 6 14 20
=PP3V3_S0_NB_TVDAC — 6
=PP3V3_S0_NB_VCC_HV — 6 17 19

19 6 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402

L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402

Layout Note:
These 4 0.1uF caps should
be within 5 mm of NB edge

19 17 6 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 10% 6.3V CERM1 603
Layout Note:
Place in cavity

C1967 0.22uF 20% 6.3V X5R 402
NOSTUFF C1968 330UF 20% 6.3V ELEC CASE-C1
Layout Note:
Place on the edge

19 16 14 6 =PP1V8_S3_MEM_NB
R1982 1K 5% 1/16W MF-LF 402
R1983 1K 5% 1/16W MF-LF 402
C1982 0.1uF 20% 16V CERM 603
MEM_VREF_NB_1 — 5 14

R1980 1K 5% 1/16W MF-LF 402
R1981 1K 5% 1/16W MF-LF 402
C1981 0.1uF 20% 16V CERM 603
MEM_VREF_NB_0 — 5 14

19 17 6 =PP3V3_S0_NB_VCC_HV
C1914 10UF 20% 6.3V CERM 805-1
C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

TVOUT DISABLE

16 6 19 =PPVCORE_S0_NB
PP2V5_S0_NB_VCCA_CRTDAC — 17
CRT_RED — 13
CRT_RED_L — 13
CRT_GREEN — 13
CRT_GREEN_L — 13
CRT_BLUE — 13
CRT_BLUE_L — 13
CRT_IREF — 13

CRT_VSYNC_R — 13
CRT_HSYNC_R — 13
=PP2V5_S0_NB_VCCSYNC — 17 19
GND_NB_VSSA_CRTDAC — 17

TP_CRT_DDC_CLK TRUE — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA TRUE — CRT_DDC_DATA — 13

DISPLAY DISABLE

TP_NB_VCCA_DPLLA TRUE — PP1V5_S0_NB_VCCA_DPLLA — 17
TP_NB_VCCA_DPLLB TRUE — PP1V5_S0_NB_VCCA_DPLLB — 17

NB_CLK_DREFCLKIN_N (IN) — 14
NB_CLK_DREFCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_N (OUT) — 14

19 6 =PPVCORE_S0_NB
C1900 330UF 20% 6.3V ELEC CASE-C1
C1901 330UF 20% 6.3V ELEC CASE-C1
C1902 10UF 20% 6.3V CERM 805-1
C1903 10UF 20% 6.3V CERM 805-1
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

19 6 =PP1V5_S0_NB_3GPLL
L1970 91NH 1210
Layout Note:
Place L and C
close to MCH
C1970 220UF 20% 2.5V POLY SMB2
C1971 10UF 20% 6.3V CERM 805-1
C1972 10UF 20% 6.3V CERM 805-1
PP1V5_S0_NB_VCC3G — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
Layout Note:
10uF caps should
be close to MCH
on opposite side.

1uH, 20%
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
Should be 1%
R1975 0.51 1% 1/16W MF-LF 402
C1975 10UF 20% 6.3V CERM 805-1
C1976 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_3GPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
GND_NB_VSSA_3GBG — 17
Layout Note:
3GPLL 10uF cap should
be placed in cavity
Layout Note: Route to caps, then GND

LVDS DISABLE

LVDS_A_CLK_N (TO) — TRUE — TP_LVDS_A_CLK_N
LVDS_A_CLK_P (TO) — TRUE — TP_LVDS_A_CLK_P
LVDS_B_CLK_N (TO) — TRUE — TP_LVDS_B_CLK_N
LVDS_B_CLK_P (TO) — TRUE — TP_LVDS_B_CLK_P

LVDS_A_DATA_N<0> (TO) — TRUE — TP_LVDS_A_DATA_N<0>
LVDS_A_DATA_N<1> (TO) — TRUE — TP_LVDS_A_DATA_N<1>
LVDS_A_DATA_N<2> (TO) — TRUE — TP_LVDS_A_DATA_N<2>

LVDS_A_DATA_P<0> (TO) — TRUE — TP_LVDS_A_DATA_P<0>
LVDS_A_DATA_P<1> (TO) — TRUE — TP_LVDS_A_DATA_P<1>
LVDS_A_DATA_P<2> (TO) — TRUE — TP_LVDS_A_DATA_P<2>

LVDS_B_DATA_N<0> (TO) — TRUE — TP_LVDS_B_DATA_N<0>
LVDS_B_DATA_N<1> (TO) — TRUE — TP_LVDS_B_DATA_N<1>
LVDS_B_DATA_N<2> (TO) — TRUE — TP_LVDS_B_DATA_N<2>

LVDS_B_DATA_P<0> (TO) — TRUE — TP_LVDS_B_DATA_P<0>
LVDS_B_DATA_P<1> (TO) — TRUE — TP_LVDS_B_DATA_P<1>
LVDS_B_DATA_P<2> (TO) — TRUE — TP_LVDS_B_DATA_P<2>

LVDS_BKLTEN (IN) — TRUE — TP_LVDS_BKLTEN
LVDS_VDDEN (IN) — TRUE — TP_LVDS_VDDEN
LVDS_IBG (IN) — TRUE — TP_LVDS_IBG
GND_NB_VSSA_LVDS (IN) — TRUE — TP_GND_NB_VSSA_LVDS

LVDS_VREFH (OUT) — TRUE — TP_LVDS_VREFH
LVDS_VREFL (OUT) — TRUE — TP_LVDS_VREFL

19 17 =PP2V5_S0_NB_VCCA_LVDS
19 17 =PP1V5_S0_NB_VCCD_LVDS
19 17 =PP2V5_S0_NB_VCC_TXLVDS

LVDS_BKLTCTL (IN) — TRUE — TP_LVDS_BKLTCTL
LVDS_CLKCTLA (IN) — TRUE — TP_LVDS_CLKCTLA
LVDS_CLKCTLB (IN) — TRUE — TP_LVDS_CLKCTLB
LVDS_DDC_CLK (IN) — TRUE — TP_LVDS_DDC_CLK
LVDS_DDC_DATA (IN) — TRUE — TP_LVDS_DDC_DATA

TVOUT DISABLE

19 6 =PP1V5_S0_NB
PP3V3_S0_NB_VCCA_TVDACA — 17
PP3V3_S0_NB_VCCA_TVDACB — 17
PP3V3_S0_NB_VCCA_TVDACC — 17
PP3V3_S0_NB_VCCA_TVBG — 17
TV_DACA_OUT (IN) — 13
TV_DACB_OUT (IN) — 13
TV_DACC_OUT (IN) — 13
TV_IREF (IN) — 13
TV_IRTNA (IN) — 13
TV_IRTNB (IN) — 13
TV_IRTNC (IN) — 13

GND_NB_VSSA_TVBG — 17

6 19 =PP1V5_S0_NB_TVDAC
PP1V5_S0_NB_VCCD_TVDAC — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.15MM
PP1V5_S0_NB_VCCD_QTVDAC — 17
Layout Note:
THESE 2 CAPS SHOULD BE
within 6.35 mm of NB edge

SDVO_CTRLCLK (IN) — 14 — TP_SDVO_CTRLCLK
SDVO_CTRLDATA (IN) — 14 — TP_SDVO_CTRLDATA

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7148	13
SCALE: NONE	SHT 19 OF 110	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 6 14 19 20
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 6 14 19 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 6 14 19 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

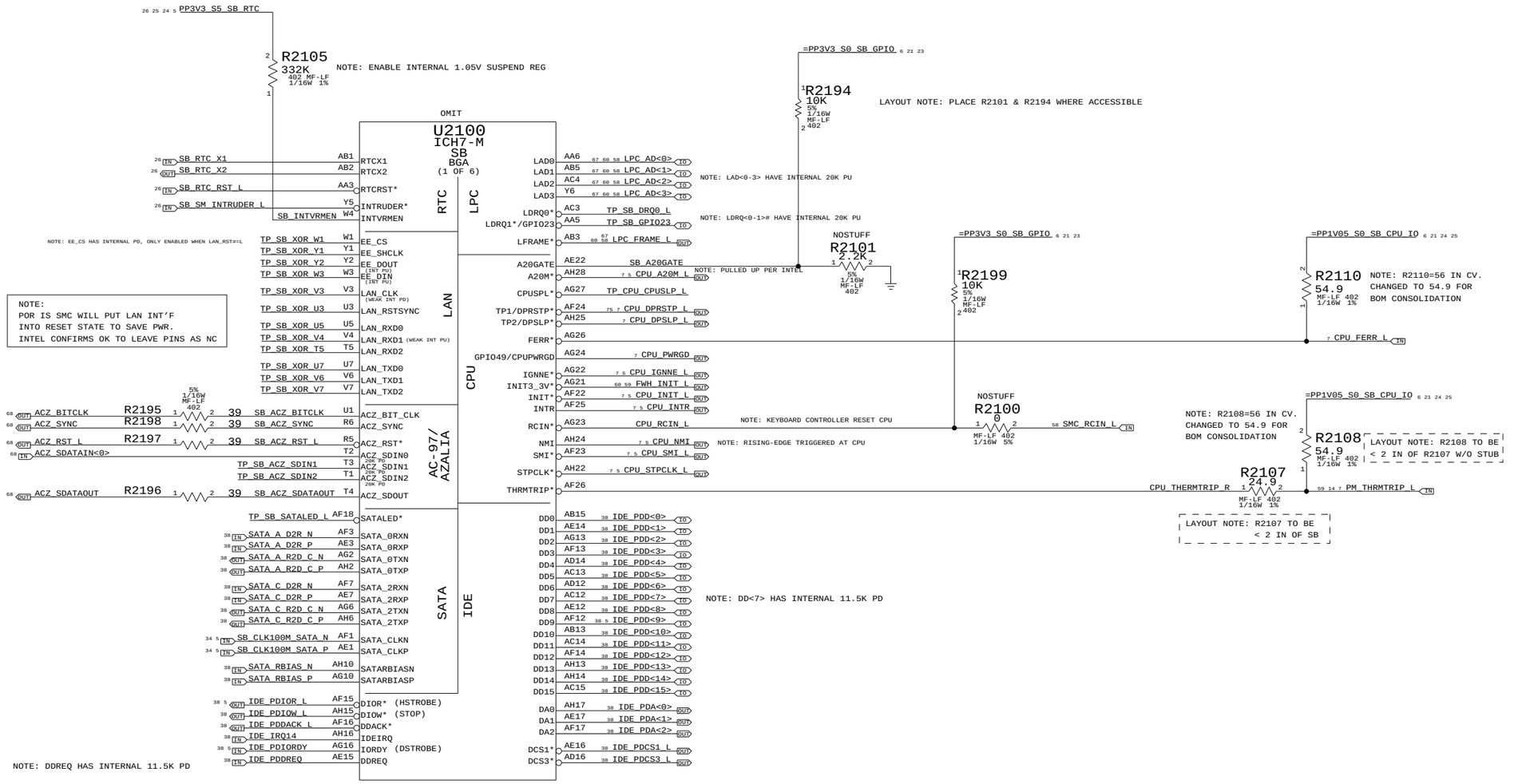
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7148 | REV. 13

SCALE NONE | SHT 20 OF 110



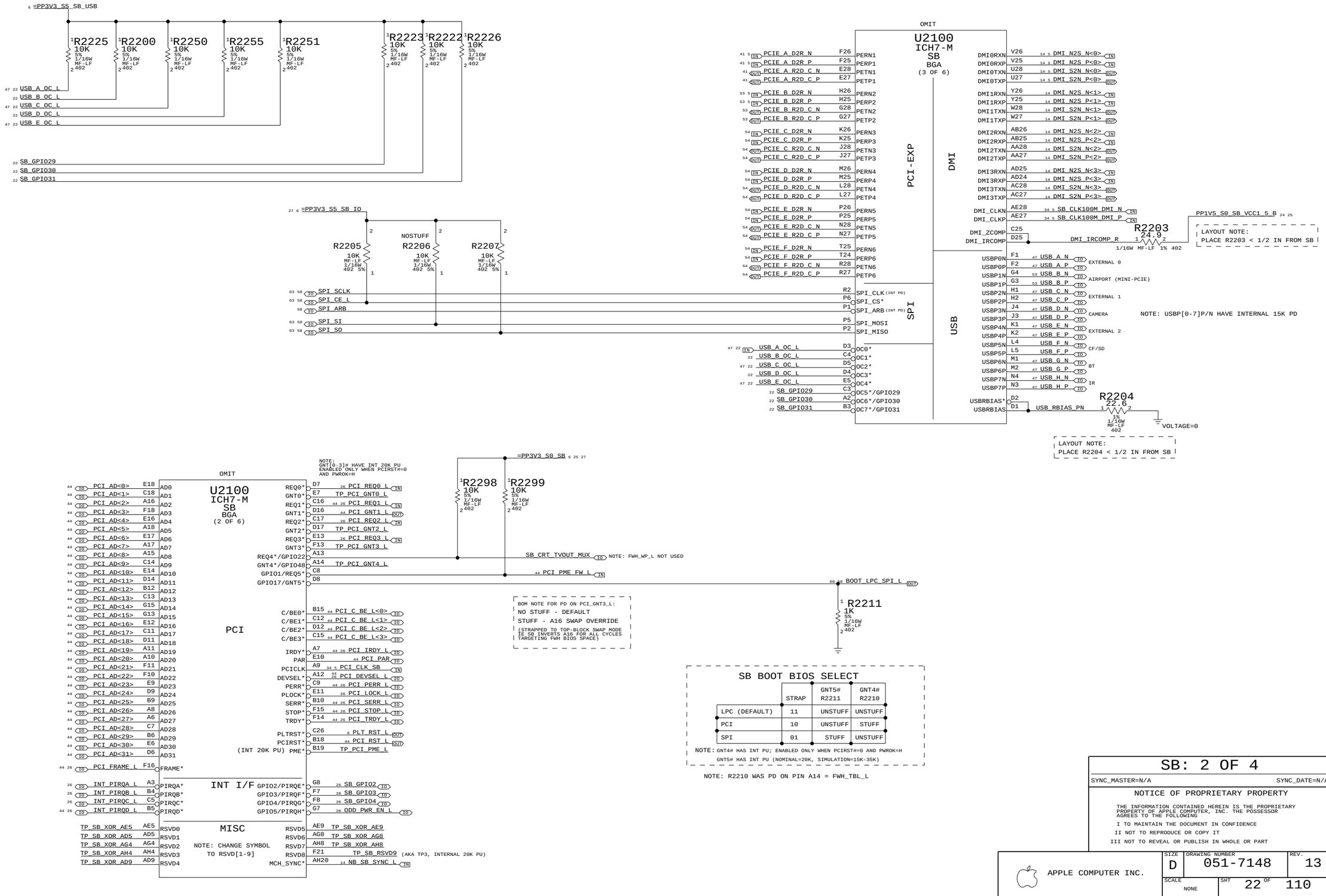
	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 21 OF 110	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2222 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCI-EXP
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
SPI
SPI_CLK (INT PD)
SPI_CS*
SPI_ARB (INT PD)
SPI_MOSI
SPI_MISO
USB
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
DMI
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_CLKN
DMI_CLKP
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
USB_A_N
USB_A_P
USB_B_N
USB_B_P
USB_C_N
USB_C_P
USB_D_N
USB_D_P
USB_E_N
USB_E_P
USB_F_N
USB_F_P
USB_G_N
USB_G_P
USB_H_N
USB_H_P
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
R2204 22.6 1% 1/16W MF-LF 402
USB_RBIAS_PN
VOLTAGE=0
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IE SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
OMIT
U2100
ICH7-M
SB
BGA
(2 OF 6)
PCI
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
INT I/F
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
TP_SB_XOR_AE5
TP_SB_XOR_AD5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AD9
REQ0*
GNT0*
REQ1*
GNT1*
REQ2*
GNT2*
REQ3*
GNT3*
REQ4*/GPIO22
GNT4*/GPIO48
GPIO1/REQ5*
GPIO17/GNT5*
PCI_REQ0_L
TP_PCI_GNT0_L
PCI_REQ1_L
PCI_GNT1_L
PCI_REQ2_L
TP_PCI_GNT2_L
PCI_REQ3_L
TP_PCI_GNT3_L
TP_PCI_GNT4_L
C/BE0*
C/BE1*
C/BE2*
C/BE3*
IRDY*
PAR
PCICLK
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
PLTRST*
PCIRST*
(INT 20K PU) PME*
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
GPIO2/PIRQE*
GPIO3/PIRQF*
GPIO4/PIRQG*
GPIO5/PIRQH*
SB_GPIO2
SB_GPIO3
SB_GPIO4
ODD_PWR_EN_L
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
NB_SB_SYNC_L
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
SYNC_MASTER=N/A
SYNC_DATE=N/A
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7148
REV. 13
SCALE NONE
SHT 22 OF 110

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 6 21 23

=PP3V3_S5_SB 6 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

26 25 23 6 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27 SMB_CLK	C22	SMBCLK
27 SMB_DATA	B22	SMBDATA
SMB_LINK_ALERT_L	A26	LINKALERT*
SMLINK<0>	B25	SMLINK0
SMLINK<1>	A25	SMLINK1
NOT USED		
PM_RI_L	A28	RI*
SB_SPKR	A19	SPKR (INT WEAK PD)
67 60 58 PM_SUS_STAT_L	A27	SUS_STAT*
58 26 5 PM_SYSRST_L	A22	SYS_RST*
14 PM_BMBUSY_L	AB18	GPIO0/BM_BUSY*
SMB_ALERT_L NOTE: RESERVED FOR FUTURE	B23	GPIO11/SMBALERT*
33 PM_STPPCI_L	AC20	GPIO18/STPPCI*
33 PM_STPCPU_L	AF21	GPIO20/STPCPU*
SB_GPIO26	A21	GPIO26
23 BIOS_REC	B21	GPIO27
23 FWH_MFG_MODE	E23	GPIO28
67 60 58 44 5 PM_CLKRUN_L	AG18	GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F: TP_AZ_DOCK_EN_L	AC19	GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L	U2	GPIO34/AZ_DOCK_RST*
53 41 PCIE_WAKE_L	F20	WAKE*
67 60 58 INT_SERIRQ	AH21	SERIRQ
58 10 PM_THRM_L	AF20	THRM*
26 VR_PWRGD_CK410	AD22	VRMPWRGD
TP_SB_GPIO6	AC21	GPIO6
	AC18	GPIO7
58 SMC_RUNTIME_SCI_L	E21	GPIO8
58 SMC_EXTSMI_L		

SYS GPIO

PWR MNGT

SATA GPIO

GPIO21/SATA0GP	AF19	SB_GPIO21 100 R2302
GPIO19/SATA1GP	AH18	SB_GPIO19 100 R2303
GPIO36/SATA2GP	AH19	
GPIO37/SATA3GP	AE19	SB_GPIO37 100 R2305

38 SATA_C_DET_L

CLKS

CLK14	AC1	34 5 SB_CLK14P3M_TIMER
CLK48	B2	34 5 SB_CLK48M_USBCTLR
SUSCLK	C20	59 SUS_CLK_SB

SLP_S3*	B24	79 77 88 86 PM_SLP_S3_L
SLP_S4*	D23	77 58 PM_SLP_S4_L
SLP_S5*	F22	58 PM_SLP_S5_L
PWROK	AA4	26 PM_SB_PWROK
GPIO16/DPRSLPVR	AC22	75 14 PM_DPRSLPVR
TP0/BATLOW*	C21	NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN*	C23	58 PM_PWRBTN_L
LAN_RST*	C19	58 PM_LAN_ENABLE
RSMRST*	Y4	

NOTE:
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F
IN RESET STATE TO SAVE PWR

GPIO

GPIO9	E20	58 26 SMS_INT_L
GPIO10	A20	58 SMC_SB_NMI
DEF=GPI GPIO12	F19	23 PATA_PWR_EN_L
GPIO13	E19	
DEF=GPI GPIO14	R4	38 IDE_RESET_L
GPIO15	E22	SV_SET_UP 23 60
GPIO24	R3	CRB_SV_DET 23
GPIO25	D20	TP_SB_GPIO25_DO_NOT_USE
OD GPIO35	AD21	33 SB_CLK100M_SATA_OE_L
GPIO38	AD20	TP_SB_GPIO38
DEF=GPI GPIO39	AE20	23 SATA_C_PWR_EN_L

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 6 11

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L

R2399 100K 5% 1/16W 402 MF-LF

58 PM_RSMRST_L

58 SMC_WAKE_SCI_L

26 25 23 6 =PP3V3_S5_SB

R2306 10K 1/16W 402 MF-LF 5% NOSTUFF
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 0 1/16W 402 MF-LF 5% NOSTUFF

SV_SET_UP 23 60
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 6 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 0 1/16W 402 MF-LF 5% NOSTUFF
R2311 10K 1/16W 402 MF-LF 5% NOSTUFF

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 6 23 25 26

R2390 10K 5% 1/16W MF-LF 402

23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 6 21 23

R2388 10K 5% 1/16W MF-LF 402

23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE: NONE SHT 23 OF 110

OMIT

U2100
ICH7-M
SB
BGA
(6 OF 6)

VSS

A4	AD3
A23	AD4
N24	AD7
P24	AD8
R18	AD15
U14	AD19
V27	AD23
AA24	AE2
AB27	AE4
AD11	AE8
B1	AE11
D10	AE13
F4	AE18
G18	AE21
J1	B8
L24	B11
M17	B14
N14	B17
N17	B20
N18	B26
N25	B28
N26	C2
P3	C6
P4	C27
P12	D13
P13	D18
P14	D21
P15	D24
P16	E1
P17	E2
P27	E4
P28	E8
R1	E15
R11	F3
R12	F5
R13	F12
R14	F27
R15	F28
R16	G1
R17	G2
T6	G5
T12	G6
T13	G9
T14	G14
T15	G21
T16	G24
T17	G25
U4	G26
U12	H3
U13	H4
U15	H5
U16	H24
U17	H27
U24	H28
U25	J2
U26	J5
V2	J24
V13	J25
V15	J26
V24	K24
V28	K27
W6	K28
W24	L13
W25	L15
W26	L25
Y3	L26
Y24	M3
Y27	M4
Y28	M5
AA1	M12
AA25	M13
AA26	M14
AB4	M15
AB6	M16
AB11	M24
AB14	M27
AB16	M28
AB19	N1
AB21	N2
AB24	N5
AB28	N6
AC2	N11
AC5	N12
AC9	N13
AC11	N15
AD1	N16
AE24	AG11
AE25	AG14
AF2	AG17
AF4	AG20
AF8	AG25
AF11	AH1
AF27	AH3
AF28	AH7
AG1	AH12
AG3	AH23
AG7	AH27

0 0

OMIT

U2100
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SB
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25 PP5V_S0_SB_V5REF	G10	
	AD17	V5REF
25 PP5V_S5_SB_V5REF_SUS	F6	V5REF_SUS
25 22 PP1V5_S0_SB_VCC1_5_B	AA22	
	AA23	
	AB22	
	AB23	
	AC23	
	AC24	
	AC25	
	AC26	
	AD26	
	AD27	
	AD28	
	D26	
	D27	
	D28	
	E24	
	E25	
	E26	
	F23	
	F24	
	G22	
	G23	VCCA3GP
	H22	VCC1_5_B
	H23	
	J22	
	J23	
	K22	
	K23	
	L22	
	L23	
	M22	
	M23	
	N22	
	N23	
	P22	
	P23	
	R22	
	R23	
	R24	
	R25	
	R26	
	T22	
	T23	
	T26	
	T27	
	T28	
	U22	
	U23	
	V22	
	V23	
	W22	
	W23	
	Y22	
	Y23	
25 24 6 =PP3V3_S0_SB_VCC3_3	B27	VCC3_3
25 PP1V5_S0_SB_VCCDMIPLL	AG28	VCCDMIPLL
25 6 =PP1V5_S0_SB_VCC1_5_A_ARX	AB7	
	AC6	
	AC7	
	AD6	ARX
	AE6	VCC1_5_A
	AF5	
	AF6	
	AG5	
	AH5	
25 6 =PP1V5_S0_SB_VCCSATAPLL	AD2	VCCSATAPLL
25 24 6 =PP3V3_S0_SB_VCC3_3	AH11	VCC3_3
25 6 =PP1V5_S0_SB_VCC1_5_A_ATX	AB10	
	AB9	
	AC10	
	AD10	ATX
	AE10	VCC1_5_A
	AF10	
	AF9	
	AG9	
	AH9	
25 24 6 =PP3V3_S5_SB_VCCSUS3_3	E3	VCCSUS3_3
25 6 =PP1V5_S0_SB_VCCUSBPLL	C1	VCCUSBPLL
VOLTAGE GENERATED INTERNALLY SO NO CONNECT HERE	AA2	VCCLAN1_5
	Y7	CHANGE SYMBOL TO 1.05

CORE VCC1_05	L11	=PPVCORE_S0_SB 6 25
	L12	
	L14	
	L16	
	L17	
	L18	
	M11	
	M18	
	P11	
	P18	
	T11	
	T18	
	U11	
	U18	
	V11	
	V12	
	V14	
	V16	
	V17	
	V18	
VCC_PAUX VCCLAN_3_3	V5	=PP3V3_S0_SB_VCCLAN3_3 6 25
	V1	
	W2	
	W7	
VCC3_3/VCCHDA	U6	=PP3V3_S0_SB_3V3_1V5_VCCHDA 6 25
VCCSUS3_3/VCCSUSHDA	R7	=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 6
V_CPU_IO	AE23	=PP1V05_S0_SB_CPU_IO 6 21 25
	AE26	
	AH26	
IDE VCC3_3	AA7	=PP3V3_S0_SB_VCC3_3_IDE 6 25
	AB12	
	AB20	
	AC16	
	AD13	
	AD18	
	AG12	
	AG15	
	AG19	
PCI VCC3_3	A5	
	B13	
	B16	
	B7	
	C10	
	D15	
	F9	
	G11	
	G12	
	G16	=PP3V3_S0_SB_VCC3_3_PCI 6 25
VCCRTC	W5	PP3V3_S5_SB_RTC 5 21 25 26
	P7	=PP3V3_S5_SB_VCCSUS3_3 6 24 25
VCCSUS3_3	A24	
	C24	
	D19	
	D22	
	G19	
USB VCCSUS3_3	K3	
	K4	
	K5	
	K6	
	L1	
	L2	
	L3	
	L6	
	L7	
	M6	
	M7	
	N7	=PP3V3_S5_SB_VCCSUS3_3_USB 6 25
VCC1_5_A	AB17	
	AC17	
	T7	
VCC1_5_A	F17	
	G17	=PP1V5_S0_SB_VCC1_5_A 6 25
VCC1_5_A	AB8	
	AC8	
	K7	
VCCSAUS1_5 CHANGE SYMBOL TO 1.05	C28	VOLTAGE GENERATED INTERNALLY SO NO CONNECT HERE
	G20	
USB CORE VCC1_5_A	A1	
	H6	
	H7	
	J6	
	J7	=PP1V5_S0_SB_VCC1_5_A_USB_CORE 6 25

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

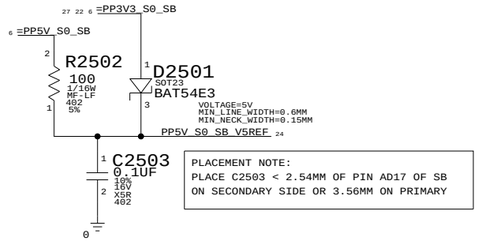
SYNC_MASTER=N/A SYNC_DATE=N/A

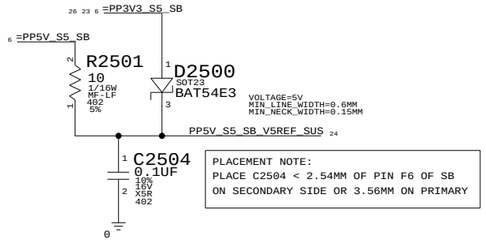
APPLE COMPUTER INC.

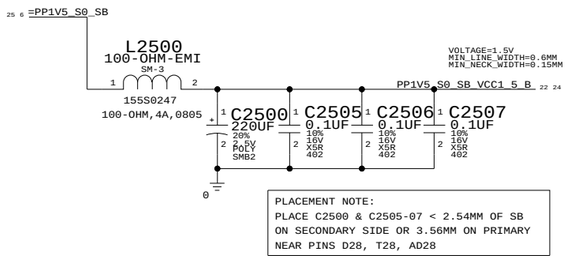
SIZE	DRAWING NUMBER	REV.
D	051-7148	13

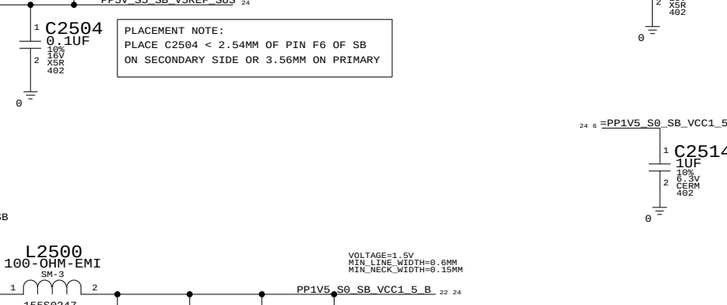
SCALE NONE

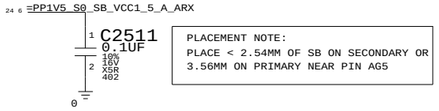
SHT 24 OF 110

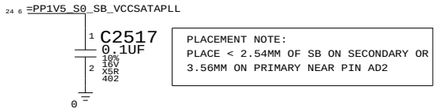


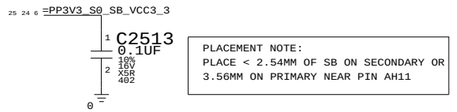


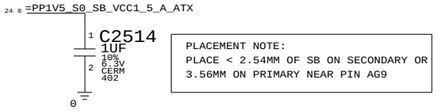


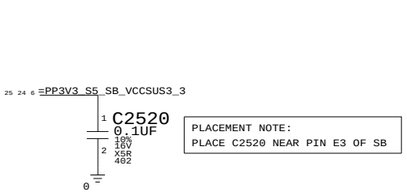


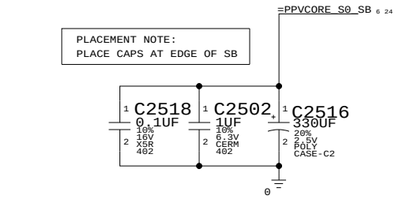


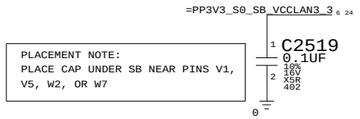


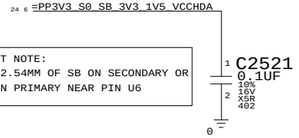


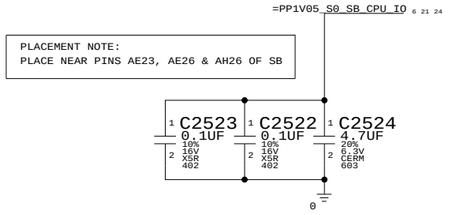


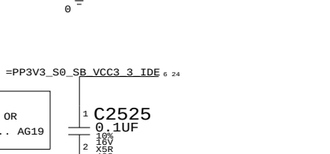


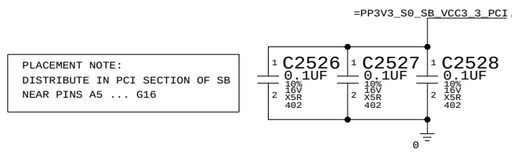


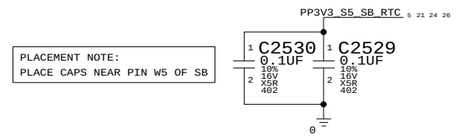


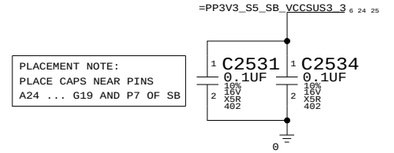


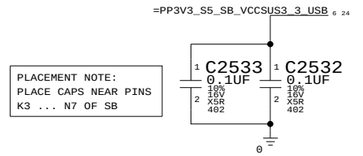


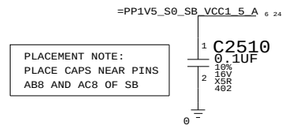


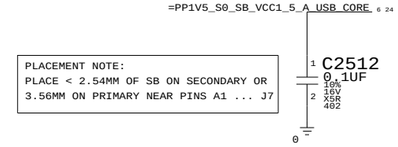










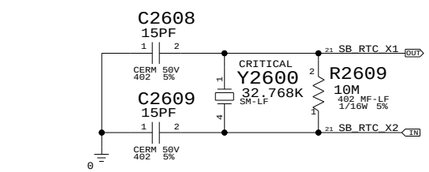


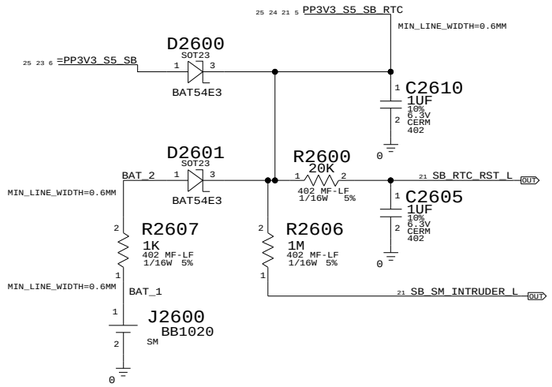
SB:DECOUPLING

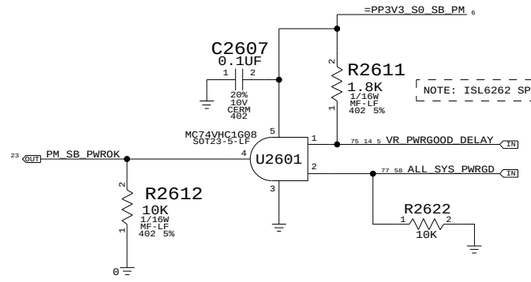
SYNC_MASTER=N/A SYNC_DATE=N/A

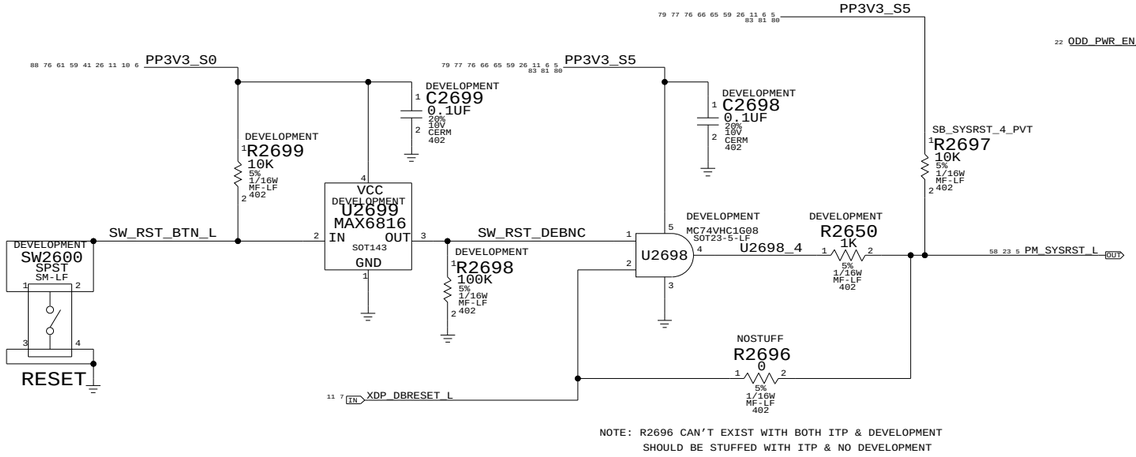
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 25 OF 110	

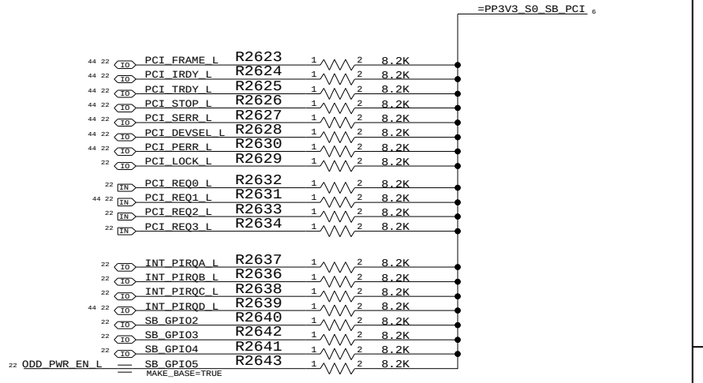


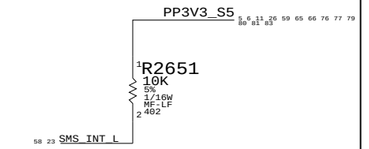


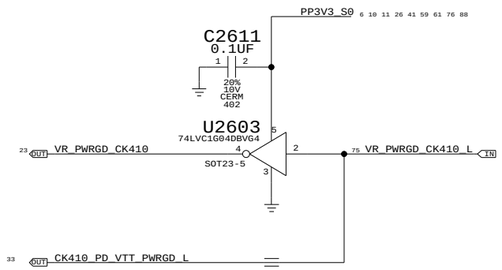




NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT







SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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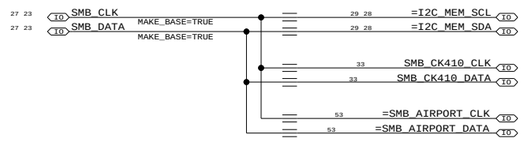
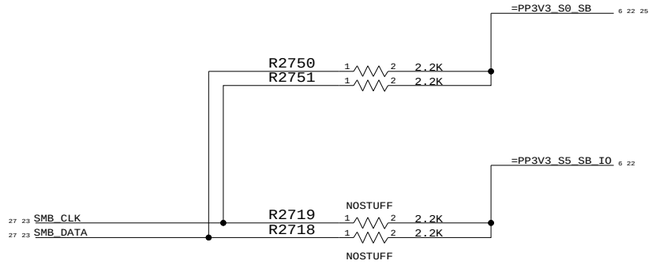
D	051-7148	13

SCALE NONE SHT 26 OF 110

SB I2C BUSSES





SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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D	051-7148	13

SCALE	SHT
NONE	27 OF 110

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

29 28 6 5 =PP1V8_S3_MEM

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF 5 28 29
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

29 28 5 MEM_VREF

C2850 2.2UF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

29 28 6 5 =PP1V8_S3_MEM

OMIT

CRITICAL
J2800
F-RT-SM1
DDR2-SODIMM-STD

1	VREF		
3	VSS1		
5	DQ0	15	MEM_A_DQ<0>
7	DQ1	15	MEM_A_DQ<1>
9	VSS4		
11	DQS0*	15 5	MEM_A_DQS_N<0>
13	DQS0	15 5	MEM_A_DQS_P<0>
15	VSS6		
17	DQ2	15	MEM_A_DQ<2>
19	DQ3	15	MEM_A_DQ<3>
21	VSS8		
23	DQ8	15	MEM_A_DQ<8>
25	DQ9	15	MEM_A_DQ<9>
27	VSS10		
29	DQS1*	15 5	MEM_A_DQS_N<1>
31	DQS1	15 5	MEM_A_DQS_P<1>
33	VSS12		
35	DQ10	15	MEM_A_DQ<10>
37	DQ11	15	MEM_A_DQ<11>
39	VSS14		
41	VSS16		
43	DQ16	15 5	MEM_A_DQ<16>
45	DQ17	15	MEM_A_DQ<17>
47	VSS18		
49	DQS2*	15 5	MEM_A_DQS_N<2>
51	DQS2	15 5	MEM_A_DQS_P<2>
53	VSS21		
55	DQ18	15	MEM_A_DQ<18>
57	DQ19	15	MEM_A_DQ<19>
59	VSS23		
61	DQ24	15	MEM_A_DQ<24>
63	DQ25	15 5	MEM_A_DQ<25>
65	VSS25		
67	DM3	15	MEM_A_DM<3>
69	NC1	NC	
71	VSS27		
73	DQ26	15	MEM_A_DQ<26>
75	DQ27	15	MEM_A_DQ<27>
77	VSS29		
79	CKE0	30 14	MEM_CKE<0>
81	VDD0		
83	NC2	NC	
85	BA2	30 15	MEM_A_BS<2>
87	VDD2		
89	A12	30 15	MEM_A_A<12>
91	A9	30 15	MEM_A_A<9>
93	A8	30 15	MEM_A_A<8>
95	VDD4		
97	A5	30 15	MEM_A_A<5>
99	A3	30 15	MEM_A_A<3>
101	A1	30 15	MEM_A_A<1>
103	VDD6		
105	A10/AP	30 15	MEM_A_A<10>
107	BA0	30 15	MEM_A_BS<0>
109	WE*	30 15	MEM_A_WE_L
111	VDD8		
113	CAS*	30 15	MEM_A_CAS_L
115	NC/S1*	30 14	MEM_CS_L<1>
117	VDD10		
119	NC/ODT1	30 14	MEM_ODT<1>
121	VSS31		
123	DQ32	15	MEM_A_DQ<32>
125	DQ33	15	MEM_A_DQ<33>
127	VSS33		
129	DQS4*	15 5	MEM_A_DQS_N<4>
131	DQS4	15 5	MEM_A_DQS_P<4>
133	VSS36		
135	DQ34	15	MEM_A_DQ<34>
137	DQ35	15	MEM_A_DQ<35>
139	VSS38		
141	DQ40	15	MEM_A_DQ<40>
143	DQ41	15	MEM_A_DQ<41>
145	VSS40		
147	DM5	15	MEM_A_DM<5>
149	VSS41		
151	DQ42	15	MEM_A_DQ<42>
153	DQ43	15	MEM_A_DQ<43>
155	VSS43		
157	DQ48	15	MEM_A_DQ<48>
159	DQ49	15	MEM_A_DQ<49>
161	VSS45		
163	NC_TEST	NC	
165	VSS47		
167	DQS6*	15 5	MEM_A_DQS_N<6>
169	DQS6	15 5	MEM_A_DQS_P<6>
171	VSS49		
173	DQ50	15	MEM_A_DQ<50>
175	DQ51	15	MEM_A_DQ<51>
177	VSS51		
179	DQ56	15	MEM_A_DQ<56>
181	DQ57	15	MEM_A_DQ<57>
183	VSS53		
185	DM7	15	MEM_A_DM<7>
187	VSS55		
189	DQ58	15	MEM_A_DQ<58>
191	DQ59	15 5	MEM_A_DQ<59>
193	VSS57		
195	SDA	29 27	=I2C_MEM_SDA
197	SCL	29 27	=I2C_MEM_SCL
199	VDDSPD		
201	GND		
202	GND		
203	GND		
204	GND		
205	GND		

2	VSS0		
4	DQ4	15	MEM_A_DQ<4>
6	DQ5	15	MEM_A_DQ<5>
8	VSS2		
10	DM0	15	MEM_A_DM<0>
12	VSS5		
14	DQ6	15	MEM_A_DQ<6>
16	DQ7	5 15	MEM_A_DQ<7>
18	VSS7		
20	DQ12	15	MEM_A_DQ<12>
22	DQ13	15	MEM_A_DQ<13>
24	VSS9		
26	DM1	15	MEM_A_DM<1>
28	VSS11		
30	CK0	14	MEM_CLK_P<0>
32	CK0*	14	MEM_CLK_N<0>
34	VSS13		
36	DQ14	5 15	MEM_A_DQ<14>
38	DQ15	15	MEM_A_DQ<15>
40	VSS15		
42	VSS17		
44	DQ20	15	MEM_A_DQ<20>
46	DQ21	15	MEM_A_DQ<21>
48	VSS19		
50	NC0	29 59	DIMM_OVERTEMP_L
52	DM2	15	MEM_A_DM<2>
54	VSS22		
56	DQ22	15	MEM_A_DQ<22>
58	DQ23	15	MEM_A_DQ<23>
60	VSS24		
62	DQ28	15	MEM_A_DQ<28>
64	DQ29	15	MEM_A_DQ<29>
66	VSS26		
68	DQS3*	5 15	MEM_A_DQS_N<3>
70	DQS3	5 15	MEM_A_DQS_P<3>
72	VSS28		
74	DQ30	15	MEM_A_DQ<30>
76	DQ31	15	MEM_A_DQ<31>
78	VSS30		
80	NC/CKE1	14 30	MEM_CKE<1>
82	VDD1		
84	NC/A15		TP_MEM_A_A<15>
86	NC/A14		TP_MEM_A_A<14>
88	VDD3		
90	A11	15 30	MEM_A_A<11>
92	A7	15 30	MEM_A_A<7>
94	A6	15 30	MEM_A_A<6>
96	VDD5		
98	A4	15 30	MEM_A_A<4>
100	A2	15 30	MEM_A_A<2>
102	A0	15 30	MEM_A_A<0>
104	VDD7		
106	BA1	15 30	MEM_A_BS<1>
108	RAS*	15 30	MEM_A_RAS_L
110	S0*	14 30	MEM_CS_L<0>
112	VDD9		
114	ODT0	14 30	MEM_ODT<0>
116	NC/A13	15 30	MEM_A_A<13>
118	VDD11		
120	NC3	NC	
122	VSS32		
124	DQ36	15	MEM_A_DQ<36>
126	DQ37	15	MEM_A_DQ<37>
128	VSS34		
130	DM4	15	MEM_A_DM<4>
132	VSS35		
134	DQ38	15	MEM_A_DQ<38>
136	DQ39	5 15	MEM_A_DQ<39>
138	VSS37		
140	DQ44	15	MEM_A_DQ<44>
142	DQ45	15	MEM_A_DQ<45>
144	VSS39		
146	DQS5*	5 15	MEM_A_DQS_N<5>
148	DQS5	5 15	MEM_A_DQS_P<5>
150	VSS42		
152	DQ46	15	MEM_A_DQ<46>
154	DQ47	5 15	MEM_A_DQ<47>
156	VSS44		
158	DQ52	15	MEM_A_DQ<52>
160	DQ53	15	MEM_A_DQ<53>
162	VSS46		
164	CK1	14	MEM_CLK_P<1>
166	CK1*	14	MEM_CLK_N<1>
168	VSS48		
170	DM6	15	MEM_A_DM<6>
172	VSS50		
174	DQ54	5 15	MEM_A_DQ<54>
176	DQ55	15	MEM_A_DQ<55>
178	VSS52		
180	DQ60	15	MEM_A_DQ<60>
182	DQ61	15	MEM_A_DQ<61>
184	VSS54		
186	DQS7*	5 15	MEM_A_DQS_N<7>
188	DQS7	5 15	MEM_A_DQS_P<7>
190	VSS56		
192	DQ62	15	MEM_A_DQ<62>
194	DQ63	15	MEM_A_DQ<63>
196	VSS58		
198	SA0		
200	SA1		ADDR=0xA0(WR)/0xA1(RD)

516S0403 ALL NC'S

29 6 =PPSPD_S0_MEM

C2851 2.2UF 20% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

DDR2 Bypass Caps

(For return current)

29 28 6 5 =PP1V8_S3_MEM

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0503	1	DDR2 SODIMM STD CONN	J2800	CRITICAL	

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE: NONE SHT: 28 OF: 110

Page Notes

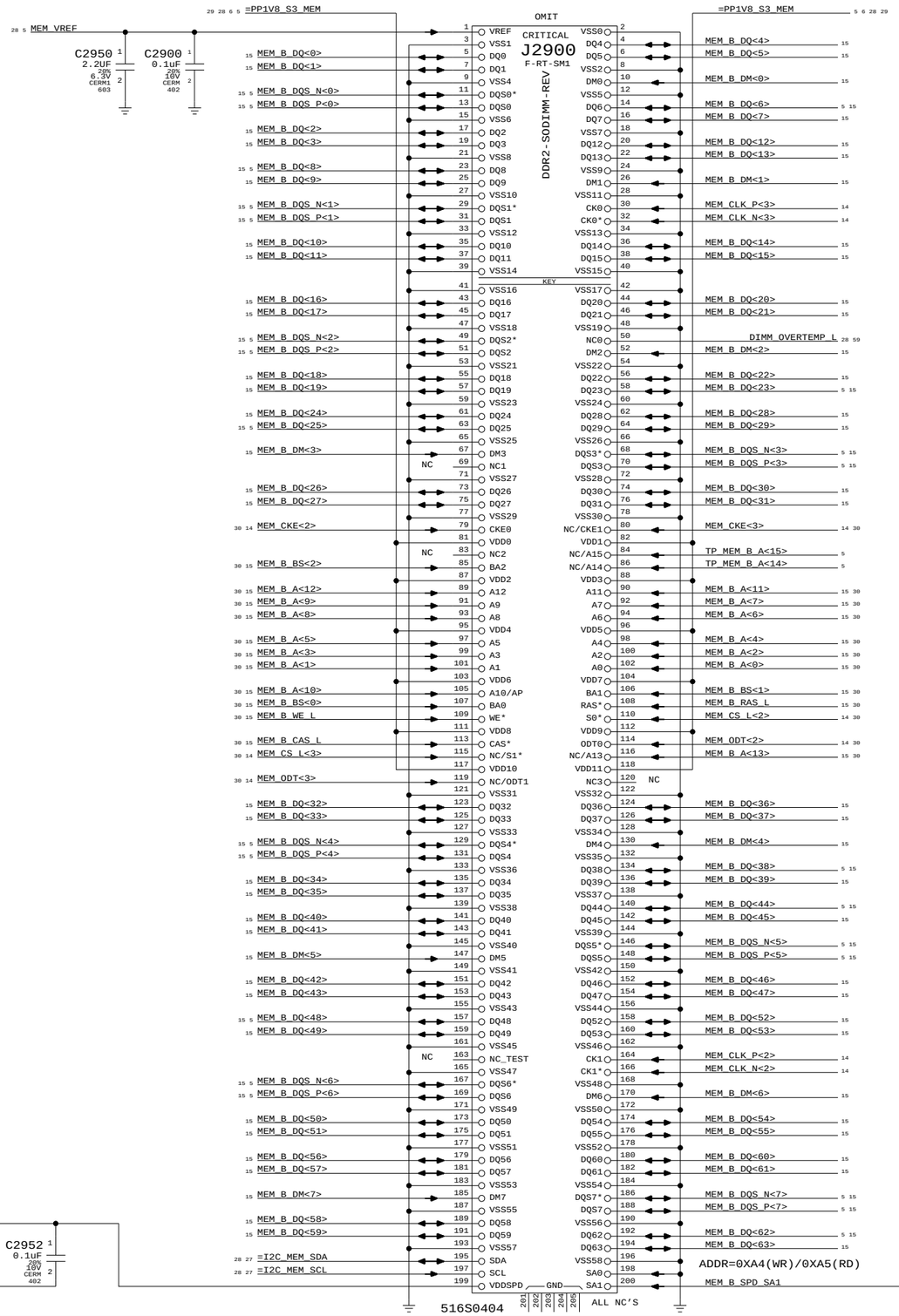
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

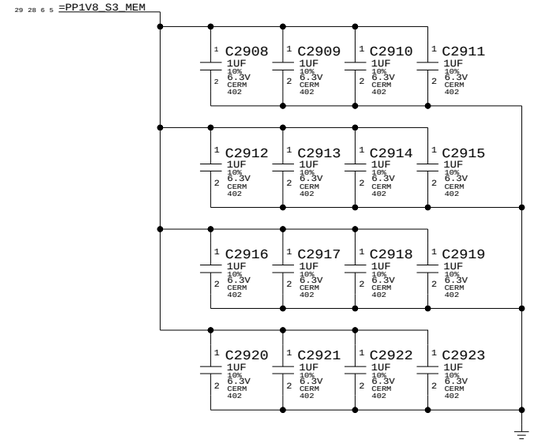
NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

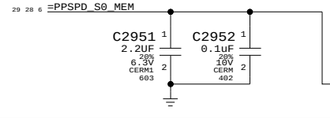
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0504	1	DDR2 SODIMM REV CONN	J2900	CRITICAL	

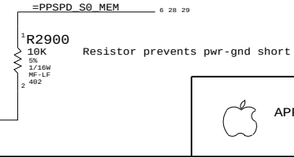


DDR2 Bypass Caps

(For return current)







DDR2 SO-DIMM Connector B

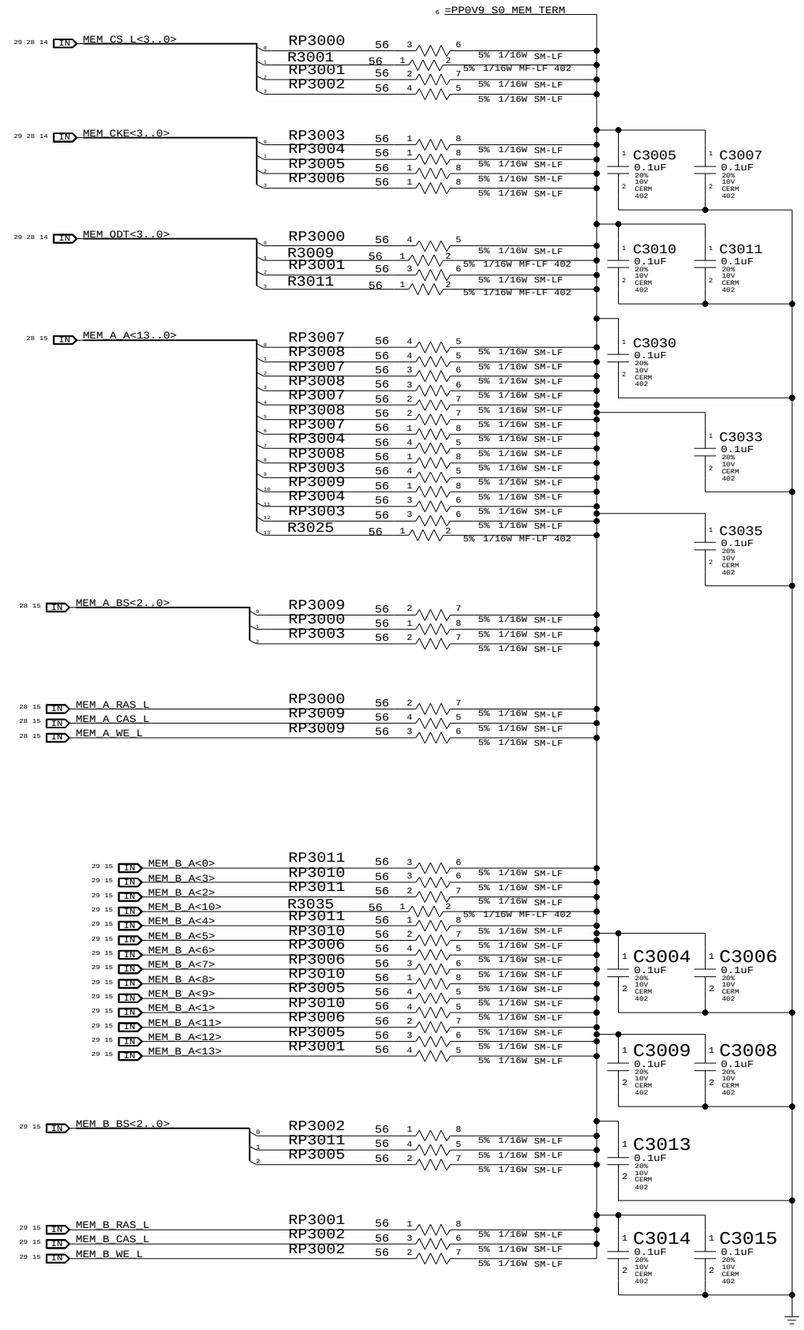
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	29	110

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	30	110

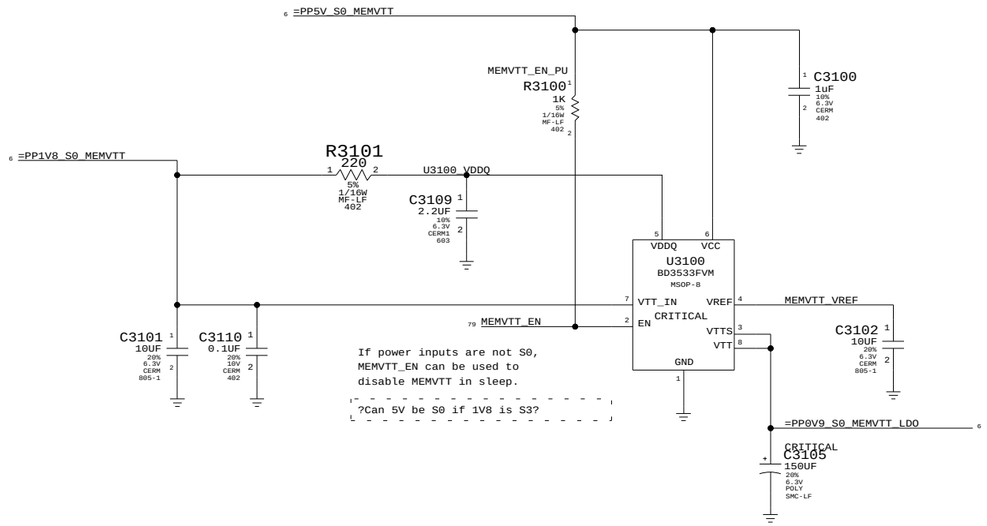
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



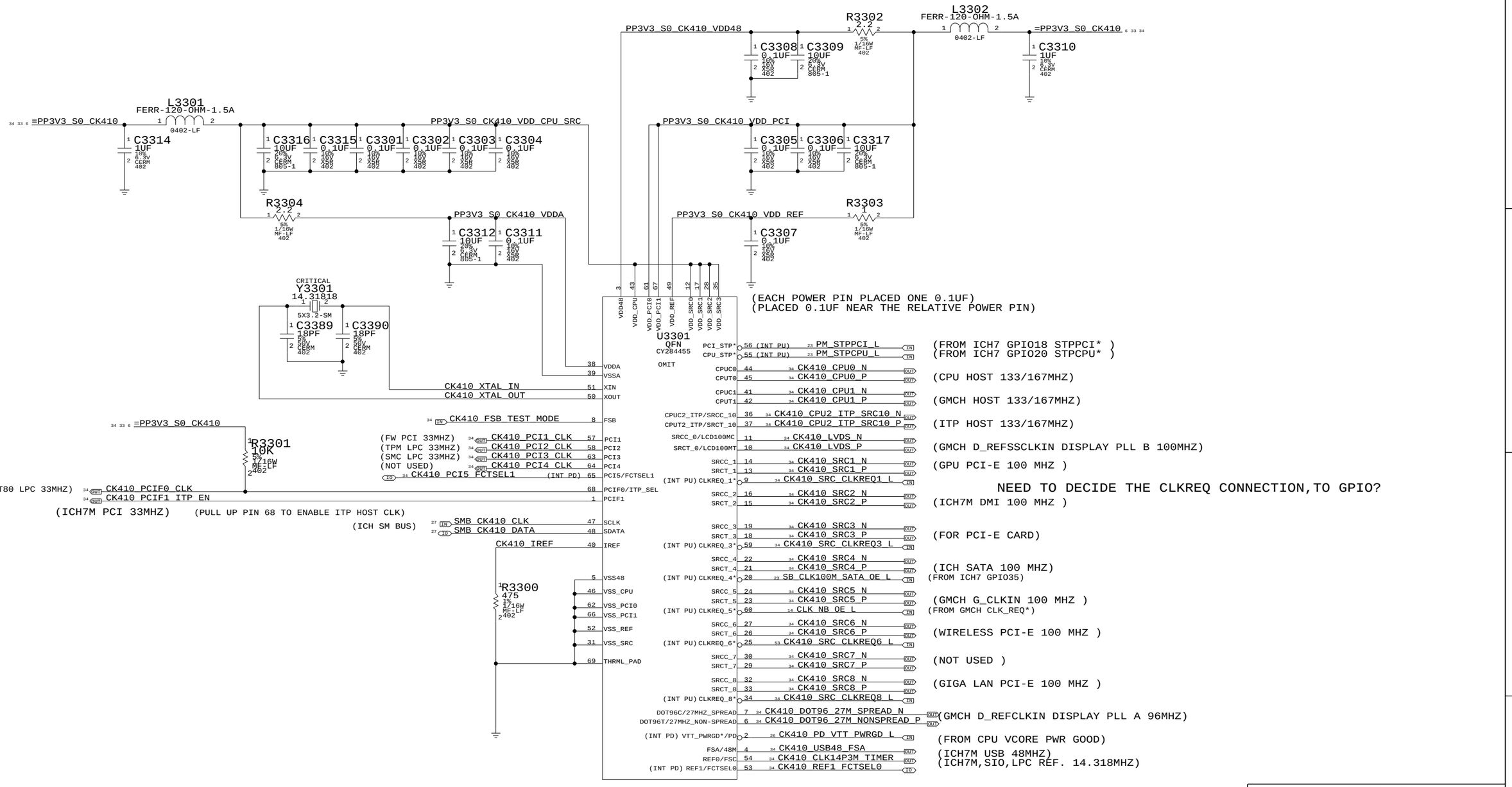
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	31	110



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	33	110

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) R3495 1K
33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) R3494 1K
33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) R3493 1K

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

81 34 6 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402
14 NB_BSEL<0>
34 CK410_FSA
R3455 1K 1/16W 5% MF-LF 402
7 CPU_BSEL<0>

NOSTUFF R3452 56 5% 1/16W MF-LF 402
R3454 0 5% 1/16W MF-LF 402

81 34 6 PP1V05_S0

R3458 1K 1/16W 5% MF-LF 402
14 NB_BSEL<1>
33 CK410_FSB_TEST_MODE
7 CPU_BSEL<1>

R3456 1K 5% 1/16W MF-LF 402
NOSTUFF R3457 0 5% 1/16W MF-LF 402
R3459 0 5% 1/16W MF-LF 402

81 34 6 PP1V05_S0

R3462 1K 1/16W 5% MF-LF 402
14 NB_BSEL<2>
34 CK410_FSC
7 CPU_BSEL<2>

R3460 1K 5% 1/16W MF-LF 402
NOSTUFF R3461 0 5% 1/16W MF-LF 402
R3463 0 5% 1/16W MF-LF 402

=PP3V3_S0_CK410 6 33

33 IO CK410_PCI5_FCTSEL1 R3499 1K 1/16W 5% MF-LF 402

R3497 2.2K 5% 1/16W MF-LF 402 CK410_FSC 34

33 IN CK410_CLK14P3M_TIMER R3498 33 1/16W 5% MF-LF 402 SB_CLK14P3M_TIMER OUT 5 23

33 IN CK410_REF1_FCTSEL0 R3496 33 TP_CLK14P3M_SPARE OUT

R3451 2.2K 5% 1/16W MF-LF 402 CK410_FSA 34

33 IN CK410_USB48_FSA R3400 33 1/16W 5% MF-LF 402 SB_CLK48M_USBCTLR OUT 5 23
33 IN CK410_PCI4_CLK R3406 33 TP_PCI_CLK_SPARE OUT 9
33 IN CK410_PCI3_CLK R3405 33 PCI_CLK_SMC OUT 58
33 IN CK410_PCI2_CLK R3404 33 PCI_CLK_TPM OUT 67
33 IN CK410_PCI1_CLK R3403 33 PCI_CLK_FW OUT 44
33 IN CK410_PCIF1_ITP_EN R3401 33 PCI_CLK_SB OUT 5 22
33 IN CK410_PCIF0_CLK R3402 33 PCI_CLK_PORT80 OUT 60

33 IN CK410_CPU1_P R3407 33
33 IN CK410_CPU1_N R3408 33 FSB_CLK_NB_P OUT 5 12 34 / FSB_CLK_NB_N OUT 5 12 34
33 IN CK410_CPU0_P R3409 33
33 IN CK410_CPU0_N R3410 33 FSB_CLK_CPU_P OUT 5 7 34 / FSB_CLK_CPU_N OUT 5 7 34
33 IN CK410_CPU2_ITP_SRC10_P R3411 33
33 IN CK410_CPU2_ITP_SRC10_N R3412 33 MAKE_BASE=TRUE
34 FSB_CLK_XDP_P — CPU_XDP_CLK_P 11
34 FSB_CLK_XDP_N — CPU_XDP_CLK_N 11

33 IN CK410_SRC6_P R3413 33 AIRPORT_CLK100M_PCIE_P OUT 34 53
33 IN CK410_SRC6_N R3414 33 AIRPORT_CLK100M_PCIE_N OUT 34 53
33 IN CK410_SRC5_P R3415 33 NB_CLK100M_GCLKIN_P OUT 5 14 34
33 IN CK410_SRC5_N R3416 33 NB_CLK100M_GCLKIN_N OUT 5 14 34
33 IN CK410_SRC4_P R3417 33 SB_CLK100M_SATA_P OUT 5 21 34
33 IN CK410_SRC4_N R3418 33 SB_CLK100M_SATA_N OUT 5 21 34
33 IN CK410_SRC2_P R3419 33 SB_CLK100M_DMI_P OUT 5 22 34
33 IN CK410_SRC2_N R3420 33 SB_CLK100M_DMI_N OUT 5 22 34
33 IN CK410_SRC8_P R3421 33 ENET_CLK100M_PCIE_P OUT 5 34 41
33 IN CK410_SRC8_N R3422 33 ENET_CLK100M_PCIE_N OUT 5 34 41
33 IN CK410_SRC1_P R3423 33 GPU_CLK100M_PCIE_P OUT 5 34 84
33 IN CK410_SRC1_N R3424 33 GPU_CLK100M_PCIE_N OUT 5 34 84
33 IN CK410_LVDS_P — TP_CK410_LVDS_P
33 IN CK410_LVDS_N — TP_CK410_LVDS_N

33 IN CK410_DOT96_27M_SPREAD_N R3470 33 CK410_27M_SPREAD OUT 92
33 IN CK410_DOT96_27M_NONSPREAD_P R3471 33 CK410_27M_NONSPREAD OUT 92

33 IN CK410_SRC3_P R3492 33 SPARE_SRC3_P R3488 49.9
33 IN CK410_SRC3_N R3491 33 SPARE_SRC3_N R3487 49.9
33 IN CK410_SRC7_P R3490 33 SPARE_SRC7_P R3486 49.9
33 IN CK410_SRC7_N R3489 33 SPARE_SRC7_N R3485 49.9

1% 402 1/16W MF-LF

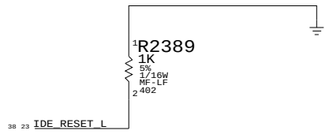
34 12 5 FSB_CLK_NB_P R3429 49.9
34 12 5 FSB_CLK_NB_N R3430 49.9
34 7 5 FSB_CLK_CPU_P R3431 49.9
34 7 5 FSB_CLK_CPU_N R3432 49.9
34 FSB_CLK_XDP_P R3433 49.9
34 FSB_CLK_XDP_N R3434 49.9
53 34 AIRPORT_CLK100M_PCIE_P R3435 49.9
53 34 AIRPORT_CLK100M_PCIE_N R3436 49.9
34 14 5 NB_CLK100M_GCLKIN_P R3438 49.9
34 14 5 NB_CLK100M_GCLKIN_N R3437 49.9
34 21 5 SB_CLK100M_SATA_P R3439 49.9
34 21 5 SB_CLK100M_SATA_N R3440 49.9
34 22 5 SB_CLK100M_DMI_P R3442 49.9
34 22 5 SB_CLK100M_DMI_N R3441 49.9
41 34 5 ENET_CLK100M_PCIE_P R3443 49.9
41 34 5 ENET_CLK100M_PCIE_N R3444 49.9
84 34 5 GPU_CLK100M_PCIE_P R3446 49.9
84 34 5 GPU_CLK100M_PCIE_N R3445 49.9

CLOCKS: TERMINATIONS

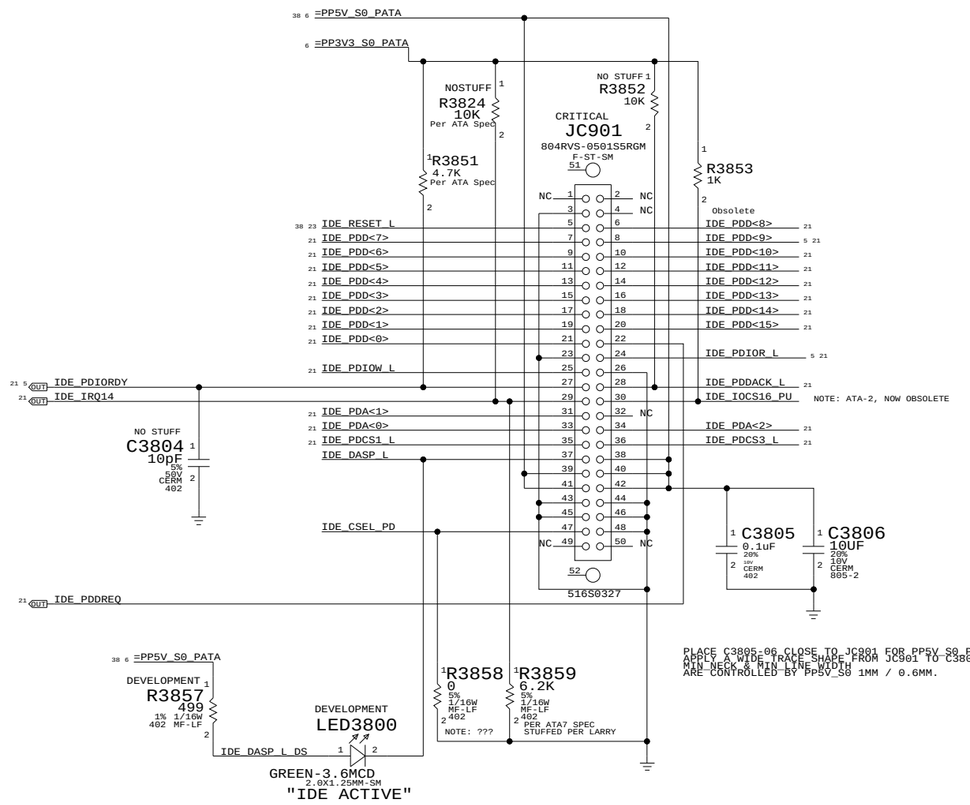
SYNC_MASTER=N/A SYNC_DATE=N/A

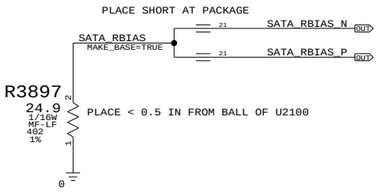
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 34 OF 110	

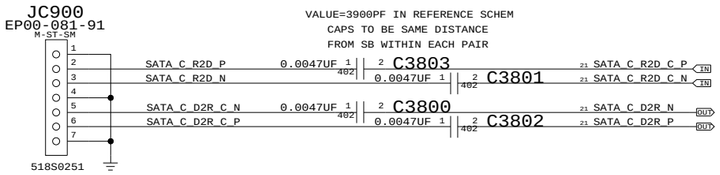


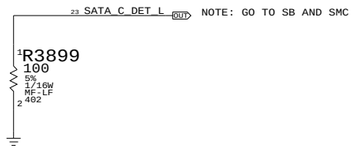
PATA CONNECTOR

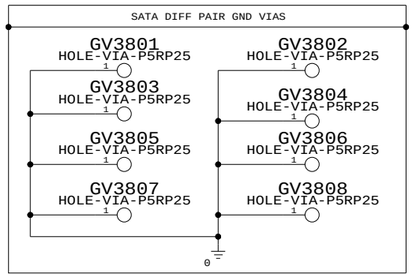




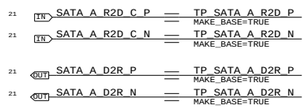
SATA CONNECTOR







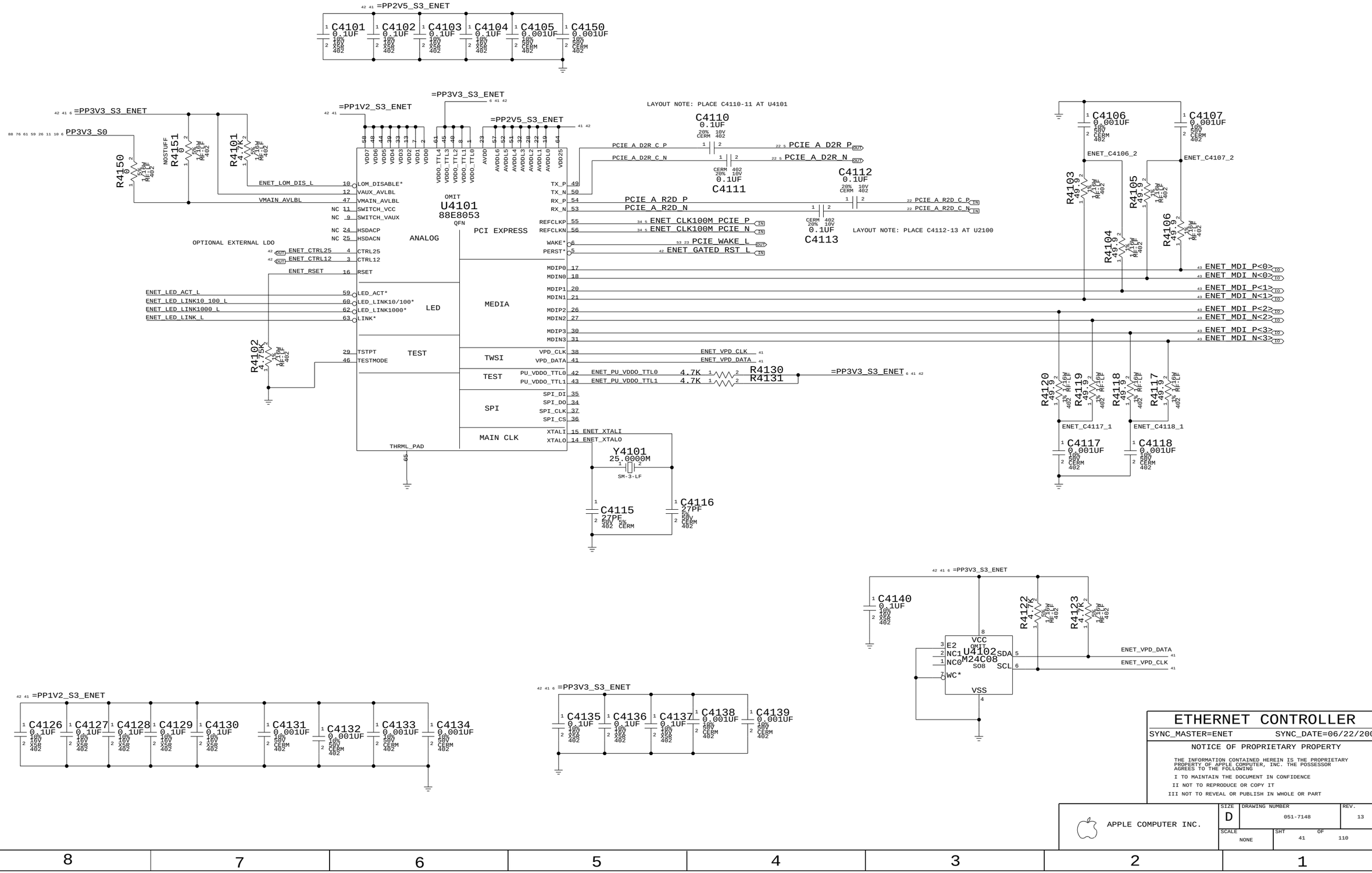
SATA PORT 0 IS NOT USED



Disk Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 38 OF 110	



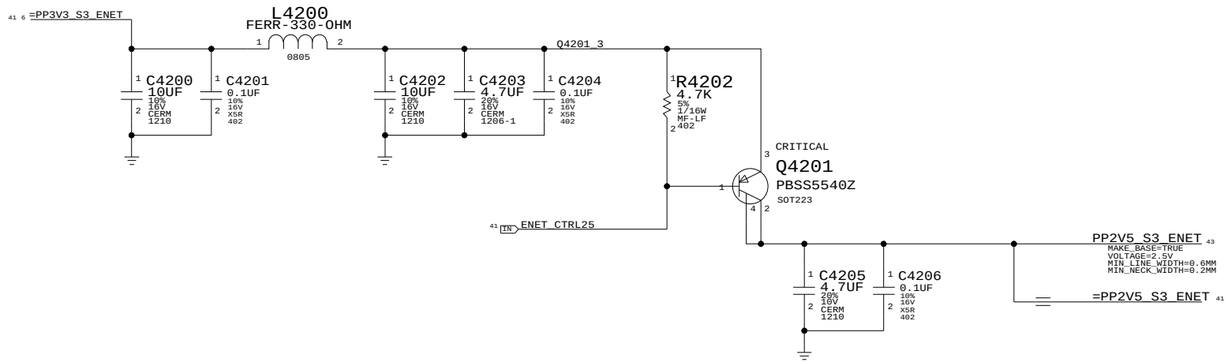
ETHERNET CONTROLLER

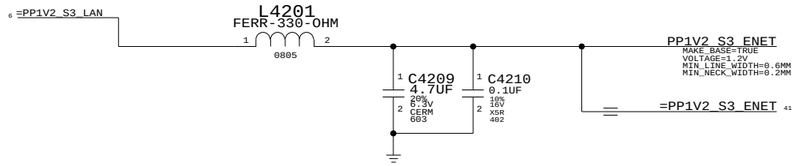
SYNC_MASTER=ENET SYNC_DATE=06/22/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 41 OF 110	

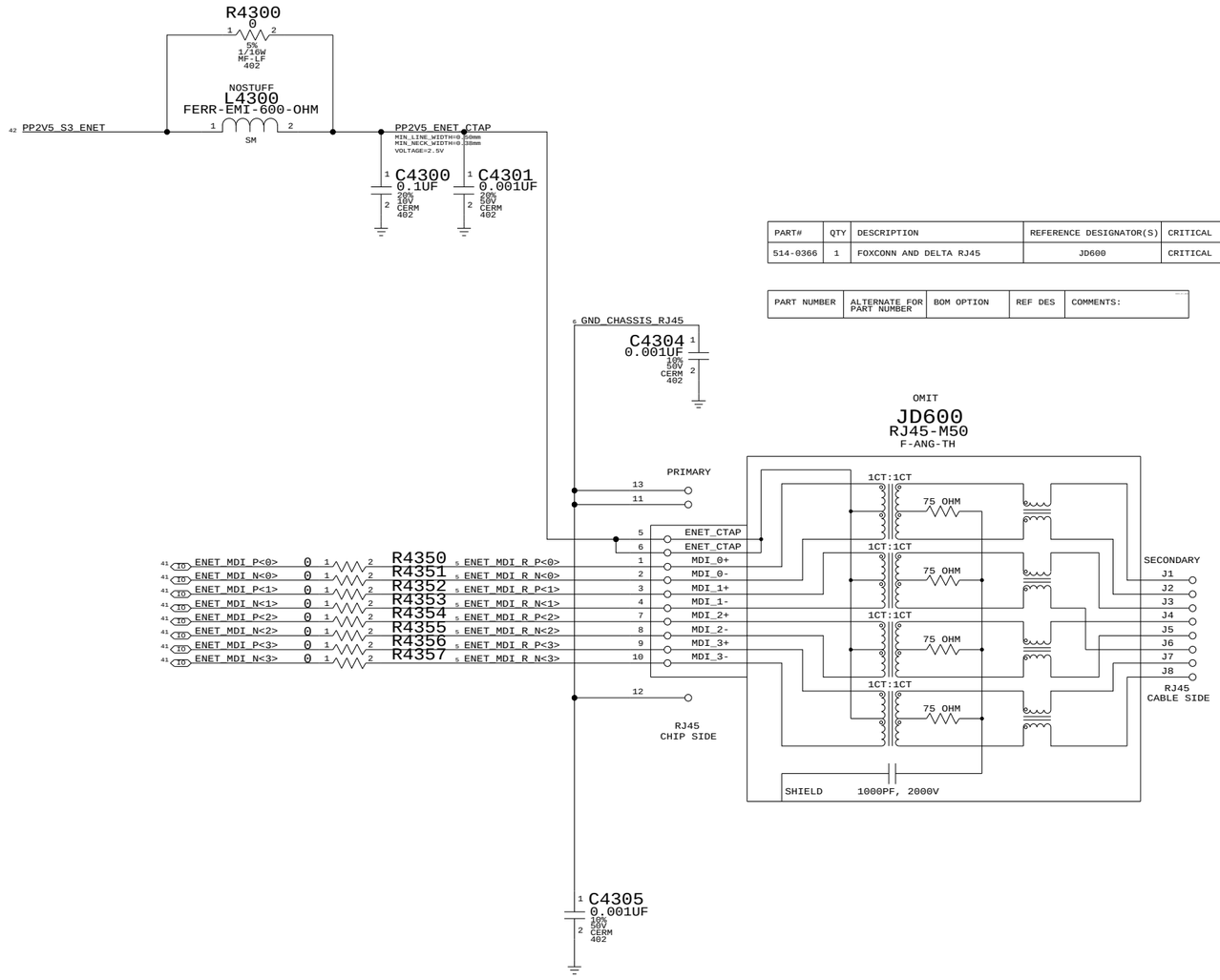




ETHERNET MISC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 42 OF 110	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0366	1	FOXCONN AND DELTA RJ45	JD600	CRITICAL	

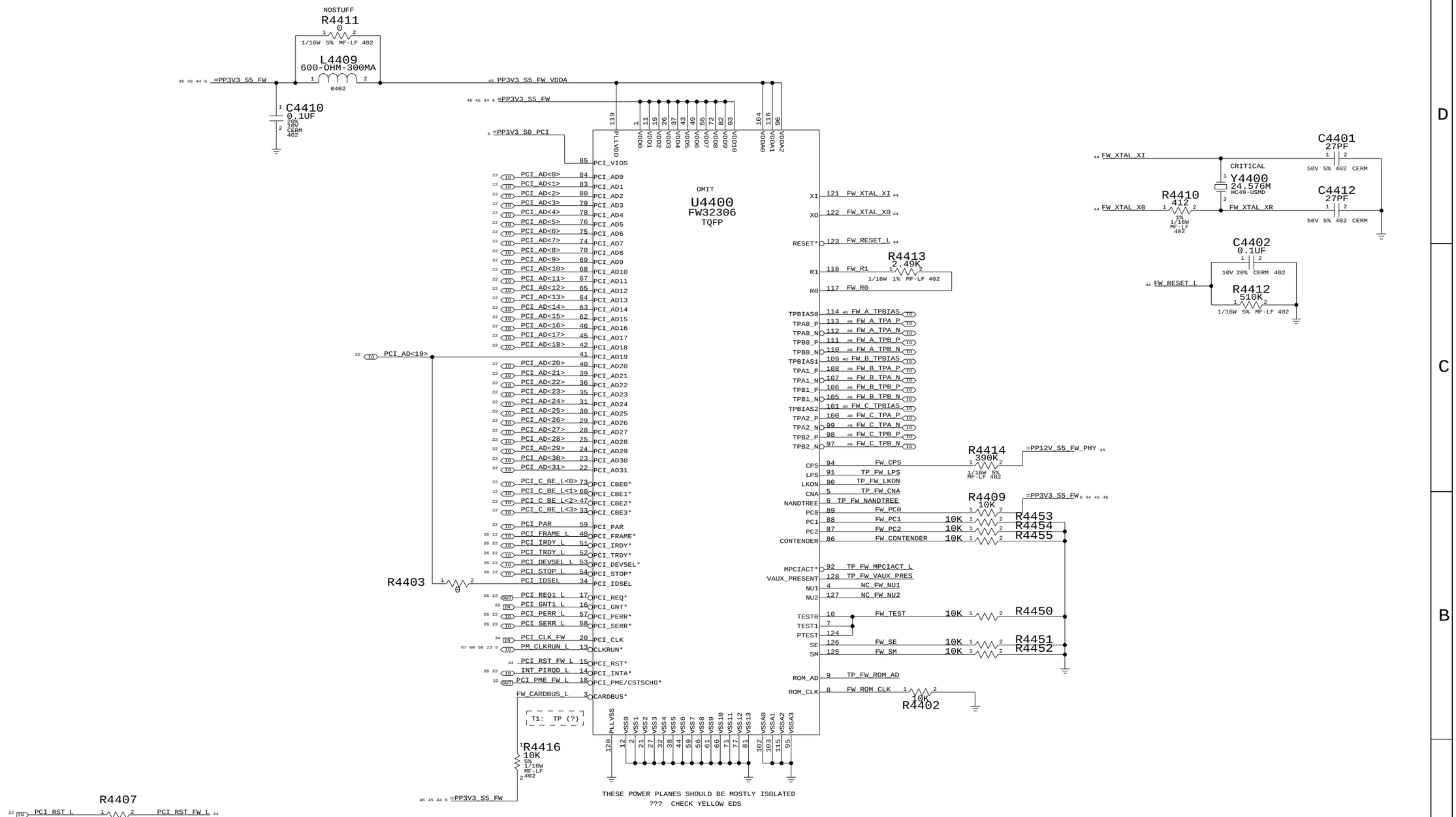
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

ETHERNET CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	43	110



FW: FW323-06			
SYNC_MASTER=N/A	SYNC_DATE=N/A		
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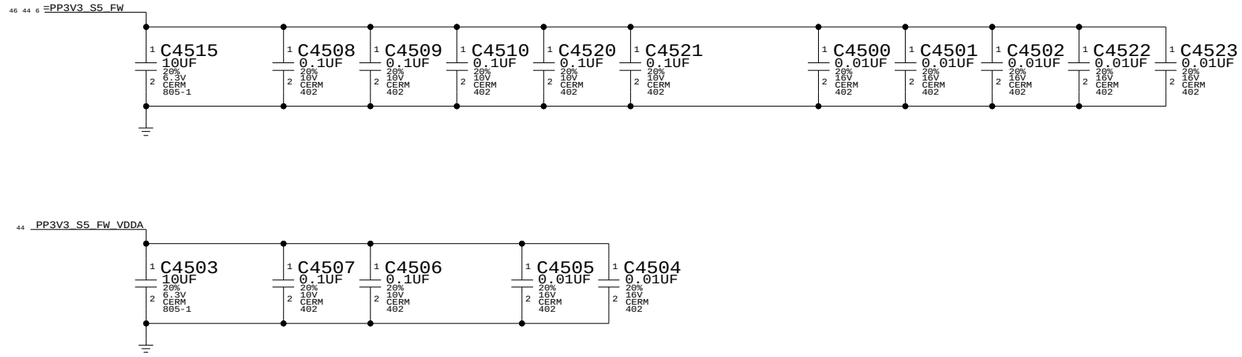
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7148	REV: 13
	SCALE: NONE	SHT 44 OF 110	



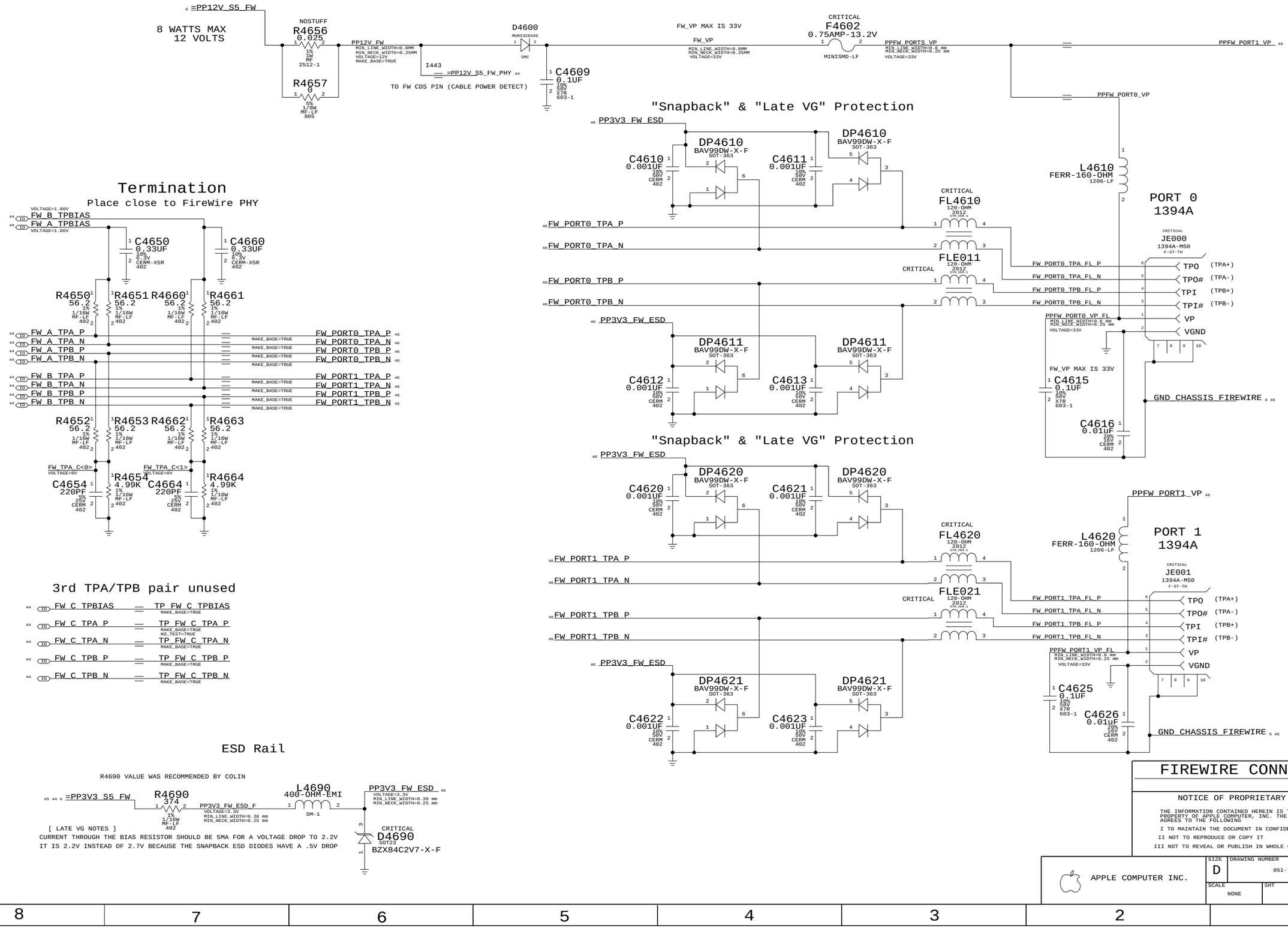
FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT
NONE	45 OF 110


=PP12V_S5_FW
8 WATTS MAX
12 VOLTS
NOSTUFF
R4656
0.025
1% 1W MF 2512-1
R4657
0
5% 1/8W MF-LF 805
PP12V_FW
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V
MAKE_BASE=TRUE
D4600
MURS320XXG
SMC
I443
=PP12V_S5_FW_PHY
TO FW CDS PIN (CABLE POWER DETECT)
C4609
0.1UF
10% 50V X7R 603-1
FW_VP MAX IS 33V
FW_VP
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=33V
CRITICAL
F4602
0.75AMP-13.2V
MINISMD-LF
PPFW_PORTS_VP
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V
PPFW_PORT1_VP
PPFW_PORT0_VP
Termination
Place close to FireWire PHY
VOLTAGE=1.86V
FW_B_TPBIAS
FW_A_TPBIAS
C4650
0.33UF
10% 6.3V CERM-X5R 402
C4660
0.33UF
10% 6.3V CERM-X5R 402
R4650 56.2
R4651 56.2
R4660 56.2
R4661 56.2
1% 1/16W MF-LF 402
FW_A_TPA_P
FW_A_TPA_N
FW_A_TPB_P
FW_A_TPB_N
FW_B_TPA_P
FW_B_TPA_N
FW_B_TPB_P
FW_B_TPB_N
MAKE_BASE=TRUE
FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N
FW_PORT1_TPA_P
FW_PORT1_TPA_N
FW_PORT1_TPB_P
FW_PORT1_TPB_N
R4652 56.2
R4653 56.2
R4662 56.2
R4663 56.2
FW_TPA_C<0>
FW_TPA_C<1>
C4654 220PF
C4664 220PF
5% 25V CERM 402
R4654 4.99K
R4664 4.99K
1% 1/16W MF-LF 402
"Snapback" & "Late VG" Protection
PP3V3_FW_ESD
DP4610
BAV99DW-X-F
SOT-363
C4610 0.001UF
C4611 0.001UF
10% 50V CERM 402
CRITICAL
FL4610
120-OHM 2012
SYM_VER-1
FLE011
FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N
DP4611
C4612 0.001UF
C4613 0.001UF
L4610
FERR-160-OHM
1206-LF
PORT 0
1394A
JE000
1394A-M50
F-ST-TH
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
PPFW_PORT0_VP_FL
C4615
0.1UF
C4616
0.01uF
GND_CHASSIS_FIREWIRE
"Snapback" & "Late VG" Protection
DP4620
C4620 0.001UF
C4621 0.001UF
FL4620
FLE021
DP4621
C4622 0.001UF
C4623 0.001UF
L4620
FERR-160-OHM
1206-LF
PORT 1
1394A
JE001
1394A-M50
F-ST-TH
PPFW_PORT1_VP_FL
C4625
0.1UF
C4626
0.01uF
3rd TPA/TPB pair unused
FW_C_TPBIAS
FW_C_TPA_P
FW_C_TPA_N
FW_C_TPB_P
FW_C_TPB_N
TP_FW_C_TPBIAS
TP_FW_C_TPA_P
TP_FW_C_TPA_N
TP_FW_C_TPB_P
TP_FW_C_TPB_N
MAKE_BASE=TRUE
NO_TEST=TRUE
ESD Rail
R4690 VALUE WAS RECOMMENDED BY COLIN
=PP3V3_S5_FW
R4690
374
1% 1/16W MF-LF 402
PP3V3_FW_ESD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
L4690
400-OHM-EMI
SM-1
PP3V3_FW_ESD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
CRITICAL
D4690
SOT23
BZX84C2V7-X-F
[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP
FIREWIRE CONNECTORS
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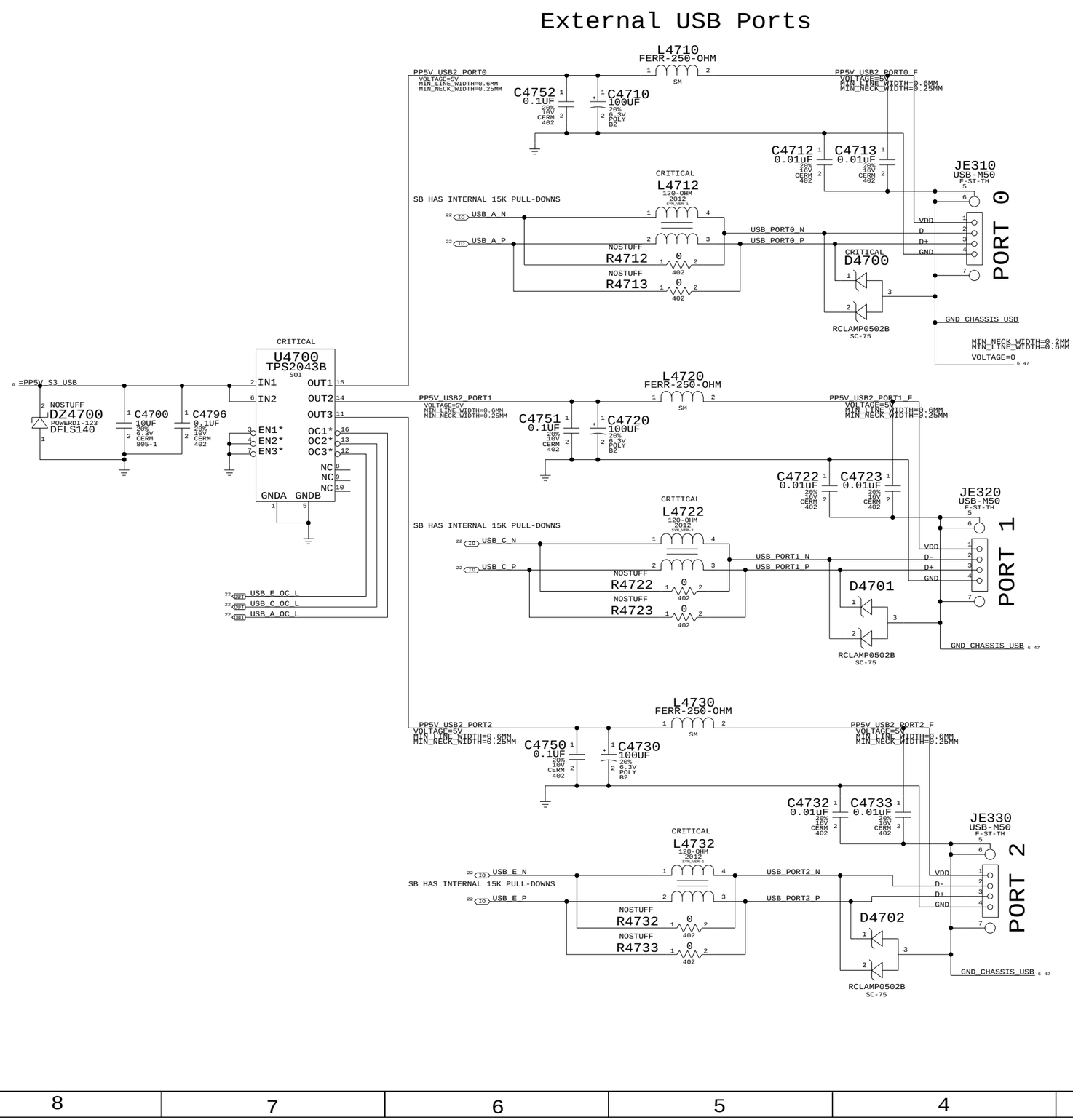
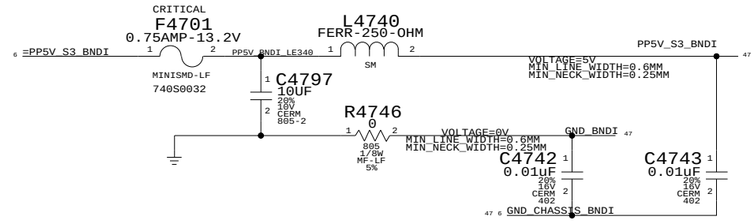
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7148
REV. 13
SCALE NONE
SHT 46 OF 110

External USB Ports

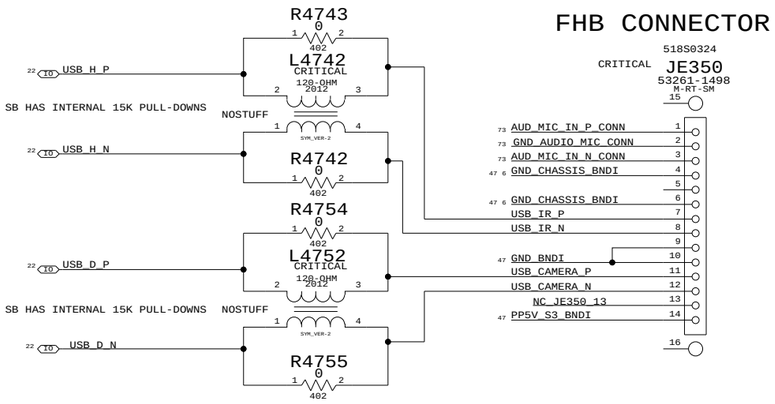




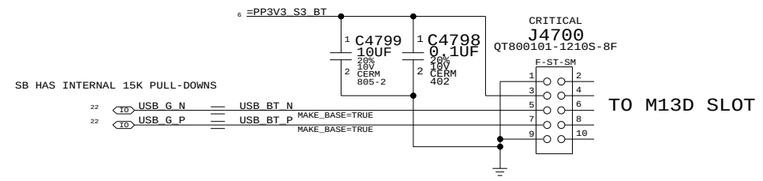
LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO JE350.

FHB CONNECTOR



BLUETOOTH



NOTE: STANDOFFS FOR J4700

SDF4700
STDOFF-40D4.5H-1.35-TH

SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT: 47	OF: 110

BLANK

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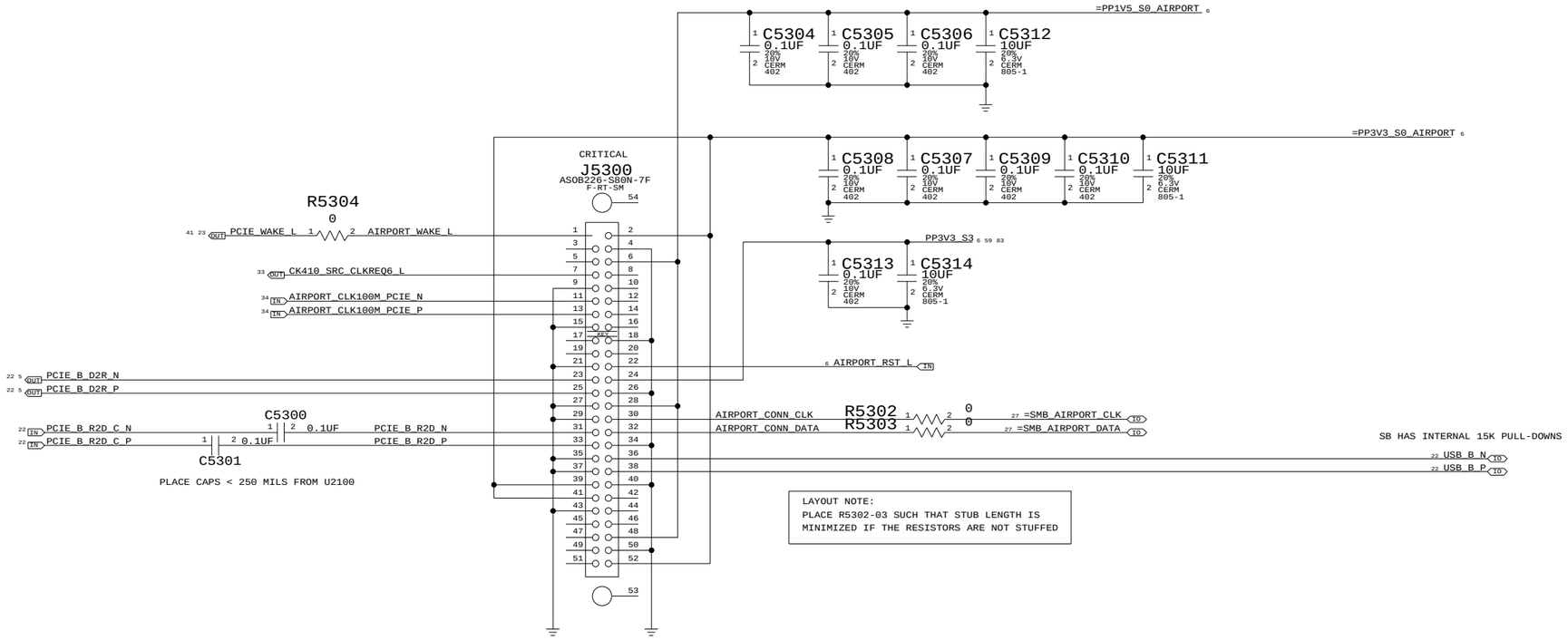
SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT
NONE	48 OF 110



AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 53 OF 110	

22 IN PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N — TP_PCIE_C_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_C_D2R_P — TP_PCIE_C_D2R_P MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N — TP_PCIE_D_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_D_D2R_P — TP_PCIE_D_D2R_P MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N — TP_PCIE_E_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_E_D2R_P — TP_PCIE_E_D2R_P MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N — TP_PCIE_F_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_F_D2R_P — TP_PCIE_F_D2R_P MAKE_BASE=TRUE

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE NONE SHT 54 OF 110

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	59	SMC_PM_G2_EN
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	59	SMC_ADAPTER_EN
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22	SPI_SCLK
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22	SPI_SI
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22	SPI_SO
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	59	SMC_PROCHOT_3_3_L
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	59	SMC_CPU_INIT_3_3_L
SMC_P20	D13	P20	P70/AN0	N12	76	SMC_CPU_ISENSE
SMC_P21	D14	P21	P71/AN1	R13	76	SMC_CPU_VSENSE
SMC_P22	D15	P22	P72/AN2	P13	59	SMC_GPU_ISENSE
SMC_P23	E12	P23	P73/AN3	R14	59	SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	76	SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	76	SMC_PBUS_VSENSE
SMC_P26	E13	P26	P76/AN6	N13	59	SMC_BATT_ISENSE
SMC_P27	F14	P27	P77/AN7	P15	59	SMC_FWIRE_ISENSE
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	59	SMC_TPM_GPIO
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 44 23 5	PM_CLKRUN_L
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23	PM_SUS_STAT_L
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	59	SC_TX_L
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	59	SC_RX_L
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	59	SMB_BSB_CLK
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	59	SMC_ONOFF_L
SMC_XDP_TMS_L	A5	P40/TMI0	P91/IRQ1*	J2	59	SMC_BC_ACOK
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	59	SMC_BS_ALRT_L
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	88 79 77 23 6	PM_SLP_S3_L
SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23	PM_SLP_S4_L
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	59	SMC_SUS_CLK
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	59	SMC_SMB_0_DATA
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
SMC_TX_L	G1	P50				
SMC_RX_L	G4	P51				
SMC_SMB_0_CLK	F2	P52/SCL0				

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	59	SMC_CASE_OPEN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5	SMC_TCK
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5	SMC_TDI
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5	SMC_TDO
PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5	SMC_TMS
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0 59
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1 59
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59	SMC_LID
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59	SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59	SMC_BATT_ISET
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59	SMC_BATT_VSET
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59	SMC_SYS_ISET
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59	SMC_SYS_VSET
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22	SPI_CE_L
SMC_EXCARD_PWR_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59	SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3_L	D11	PB7	PG2/EXIRQ10*/SDA2	N9	59	SMB_BSA_DATA
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	59	SMB_BSA_CLK
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	59	SMB_A_S3_DATA
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	59	SMB_A_S3_CLK
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	59	SMB_B_S0_DATA
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	59	SMB_B_S0_CLK
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59	SMC_PROCHOT
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59	SMC_THRMTRIP
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59	SMC_FWE
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59	ALS_GAIN
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23	SMS_INT_L
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59	SMS_ONOFF_L
SMC_ANALOG_ID	N11	PD3/AN11				
SMC_NB_ISENSE	P10	PD4/AN12				
SMC_MEM_ISENSE	R10	PD5/AN13				
ALS_LEFT	N10	PD6/AN14				
ALS_RIGHT	M10	PD7/AN15				

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 6 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 10% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 6 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
85 76 59 58 GND_SMC_AVSS

PP3V3_AVREF_SMC 59
59 58 6 =PP3V3_S5_SMC

AVCC N14, AVCC N15, VCC P2, VCC P1, VCC J15, VCC A1, VCC F1, AVREF M14, AVREF M15

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

60 59 IN SMC_RST_L → RES* E3
59 SMC_XTAL → XTAL A2
59 SMC_EXTAL → EXTAL B2

MD1 F2 → SMC_MD1 60
MD2 K1 → KBC_MDE
NMI F4 → SMC_NMI 60 IN
ETRST* L1 → SMC_TRST_L IN
AVSS P12, R12
VSS D1, P4, R4, F12, F13, B13, A13, A4, B4, D2

R5809 10K 5% 1/16W MF-LF 2402
R5801 10K 5% 1/16W MF-LF 2402
NOSTUFF
R5898 10K 5% 1/16W MF-LF 2402
R5803 0 5% 1/16W MF-LF 2402
R5802 10K 5% 1/16W MF-LF 2402

XW5800 SM
GND_SMC_AVSS 58 59 76 85

SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 58 OF 110	

SMC RESET BUTTON

=PP3V3_S5_SMC

C5901 0.1uF 20% 10V CERM 402

C5900 0.01UF 10V CERM 402

U5900 RN5VD30A-F SOT23-5 — CRITICAL — VDD, CD, NC, GND, OUT

R5900 1K 5% 1/16W MF-LF 402

SW5900 SPST SM-LF — DEVELOPMENT

SMC_MANUAL_RST_L → SMC_RST_L (OUT)

AMBIENT LIGHT SENSOR CONNECTOR

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

I2C ADDR:72(1001000)

J2901 53398-0476 F-ST-SM — CRITICAL

PP3V3_S3

I2C_ALS_SDA

I2C_ALS_SCL

518S0328

SMC 3.3V -> CPU 1.05V SHIFTER

CPU_PROCHOT_L → Q5901 2N7002DW-X-F SOT-363 → SMC_PROCHOT

PM_THRMTRIP_L → Q5901 2N7002DW-X-F SOT-363 → SMC_THRMTRIP

POWER BUTTON HEADER

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

J2903 53398-0276 M-ST-SM

POWER_BUTTON_L

518S0327

R5907 1K 5% 1/16W MF-LF 402

SYS POWER BUTTON — SW5901 SPST SM-LF — DEVELOPMENT

SMC_ONOFF_L

C5902 0.1uF 20% 10V CERM 402

GENERATE 0.48V MID-VREF

=PP3V3_S0_FAN

R5930 6.2K 5% 1/16W MF-LF 402

P0V48_SMC_LSREF

R5931 1K 5% 1/16W MF-LF 402

SMC CRYSTAL

C5800 22PF CERM 5% 50V 402

C5801 22PF CERM 5% 50V 402

OMIT Y5800 20.000M SM-3

SMC_XTAL, SMC_EXTAL

TPM CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

C6704 15PF 5% 50V CERM 402

C6705 15PF 5% 50V CERM 402

CRITICAL Y6700 32.768K SM-LF

TPM_XTALI, TPM_XTALO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL,20.00,80PPM,HC49,SMD,LF	Y5800	CRITICAL	

CPU 1.05V -> SMC 3.3V SHIFTER

PP3V3_S5

=PP3V3_S0_FAN

C5903 0.1UF 20% 10V CERM 402

U5999 LM393A SOI-1-LF

P0V48_SMC_LSREF

CPU_PROCHOT_L

R5932 1K 5% 1/16W MF-LF 402

R5933 1K 5% 1/16W MF-LF 402

SMC_PROCHOT_3_3_L

SMC_CPU_RESET_3_3_L

U5999 LM393A SOI-1-LF

R5934 1K 5% 1/16W MF-LF 402 → SMC_XDP_TCK_3_3

R5935 1K 5% 1/16W MF-LF 402 → SMC_XDP_TDO_3_3_L

PCB: ENSURE FSB_CPURST_L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		U5940	DONE IN M50/M51

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20
SMC_P21	NC_SMC_P21
SMC_P22	NC_SMC_P22
SMC_P23	NC_SMC_P23
SMC_P26	NC_SMC_P26
SMC_P27	NC_SMC_P27
SMC_BATT_ISET	NC_SMC_BATT_ISET
SMC_BATT_VSET	NC_SMC_BATT_VSET
SMC_SYS_ISET	NC_SMC_SYS_ISET
SMC_SYS_VSET	NC_SMC_SYS_VSET
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN
SMC_ANALOG_ID	NC_SMC_ANALOG_ID
ALS_GAIN	NC_ALS_GAIN

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	FUNC_TEST=TRUE
SMC_PF0	TP_SMC_PF0	
SMC_PM_G2_EN	TP_PM_G2_EN	FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	
SMC_PF1	TP_SMC_PF1	
SMC_PB7	TP_SMC_PB7	FUNC_TEST=TRUE
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	FUNC_TEST=TRUE

TPM RESET PULLUP

PP3V3_TPM_3VSB → R5827 10K → SMC_TPM_RESET_L

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L<0>

SENSE GPU REGULATOR OUTPUT CURRENT

SMC_GPU_ISENSE — GPUVCORE_IOUT

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L
SMC_SUS_CLK	SUS_CLK_SB

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_NB_ISENSE	NC_SMC_NB_ISENSE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE

UNUSED_SMC_SENSE — 10K R5924 — PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SC_RX_L — 0 R5922 — DEVELOPMENT_SMC — SMC_RX_L

SC_TX_L — 0 R5923 — DEVELOPMENT_SMC — SMC_TX_L

SELECT TPM GPIO

SMC_TPM_GPIO — 0 R5920 — SMC_TPM_GPIO1 — TPM_GPIO1

SMC_TPM_GPIO — 0 R5921 — SMC_TPM_GPIO2 — TPM_GPIO2

SMC_TPM_PP — R5995 0 5% 1/16W MF-LF 402 — TPM_PP

SMC PULL-UPS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SMC_EXCARD_CP	R5830	10K
SMC_EXCARD_PWR_OC_L	R5831	10K
SC_RX_L	R5832 NOT_DEVELOPMENT_SMC	10K
SC_TX_L	R5833 NOT_DEVELOPMENT_SMC	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K

SENSE GPU VCORE

PP1V0R1V2_S0_GPU — R5919 4.53K 1% 1/16W MF-LF 402 — SMC_GPU_VSENSE

C5919 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS

PRECISION 3.3V AVREF FOR SMC

PP5V_S5

R5942 10K 5% 1/16W MF-LF 402

Q5910 NTR4101P SOT-23

SMC_REF_GATE2

SMC_REF_GATE1

R5941 10K 5% 1/16W MF-LF 402

Q5911 2N7002 SOT23-LF

C5943 1UF 10% 6.3V CERM 402

SMC_REF_IN

NOSTUFF R5940 0 5% 1/16W MF-LF 402

CRITICAL U5940 REF3133 SOT23-3 — IN, TI, OUT, GND

C5940 0.47UF 10% 6.3V CERM-X5R 402

C5942 10UF 20% 6.3V CERM 805-1

PP3V3_AVREF_SMC

C5941 0.01uF 20% 16V CERM 402

GND_SMC_AVSS

TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

SMC I2C BUS PULLUPS (INCLUDING UNUSED ONES)

PP3V3_S0

2.2K	R5903	SMB_B_S0_CLK
2.2K	R5904	SMB_B_S0_DATA

PP3V3_S3

2.2K	R5905	SMB_A_S3_CLK
2.2K	R5906	SMB_A_S3_DATA

=PP3V3_S5_SMC

10K	R5910	SMB_BSB_CLK
10K	R5911	SMB_BSB_DATA
10K	R5912	TP_SMC_SMB_0_CLK (FUNC_TEST=TRUE) → SMC_SMB_0_CLK
10K	R5913	SMC_SMB_0_DATA → TP_SMC_SMB_0_DATA (FUNC_TEST=TRUE)
10K	R5914	SMB_BSA_CLK
10K	R5915	SMB_BSA_DATA

PULLUPS FOR SYSTEM STATE PINS

10K	R5916	SMC_LID

PULLDOWNS FOR SYSTEM STATE PINS

10K	R5917	SMC_CASE_OPEN

ALIAS SENSORS INTO SMC I2C BUSSES

SMB_B_S0_CLK, SMB_B_S0_DATA

=I2C_HD_TEMP_SCL, =I2C_HD_TEMP_SDA

=I2C_ODD_TEMP_SCL, =I2C_ODD_TEMP_SDA

=SMB_THRM_CLK, =SMB_THRM_DATA

SMB_GPU_NB_THRM_CLK, SMB_GPU_NB_THRM_DATA

SMB_A_S3_CLK → I2C_ALS_SCL

SMB_A_S3_DATA → I2C_ALS_SDA

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM — GND_NEXT_TO_SMC

SMC & TPM SUPPORT

NOTICE OF PROPRIETARY PROPERTY

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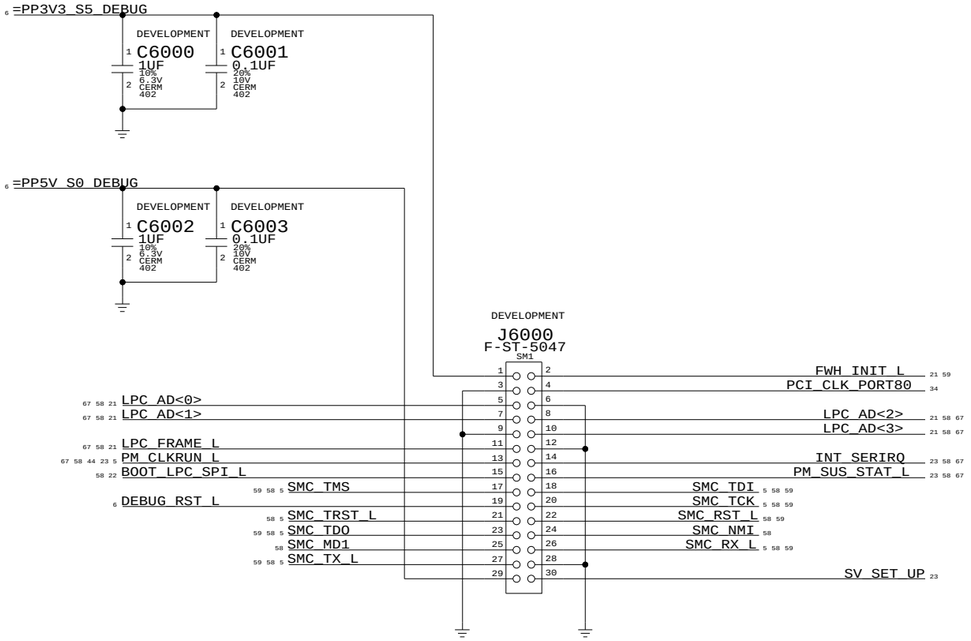
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE: NONE — SHT 59 OF 110



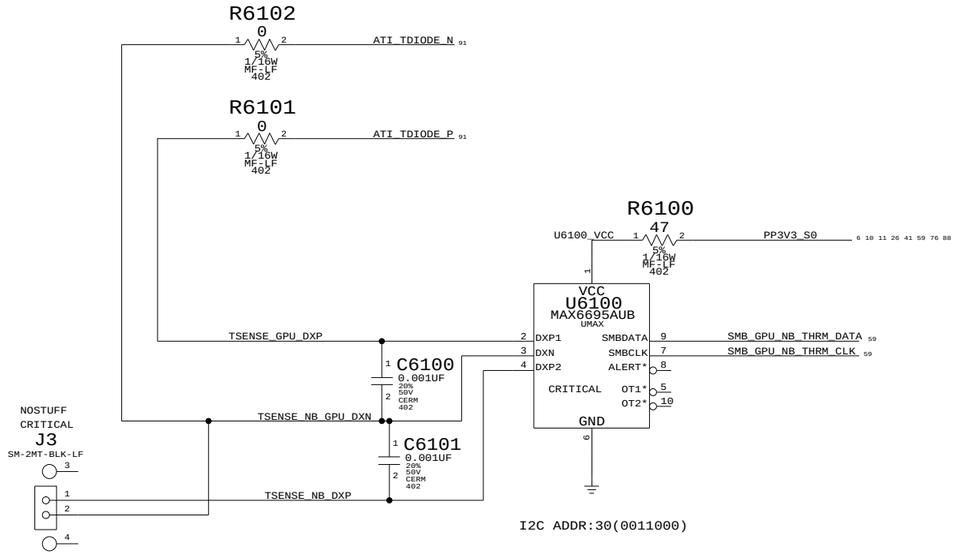
LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 60 OF 110	

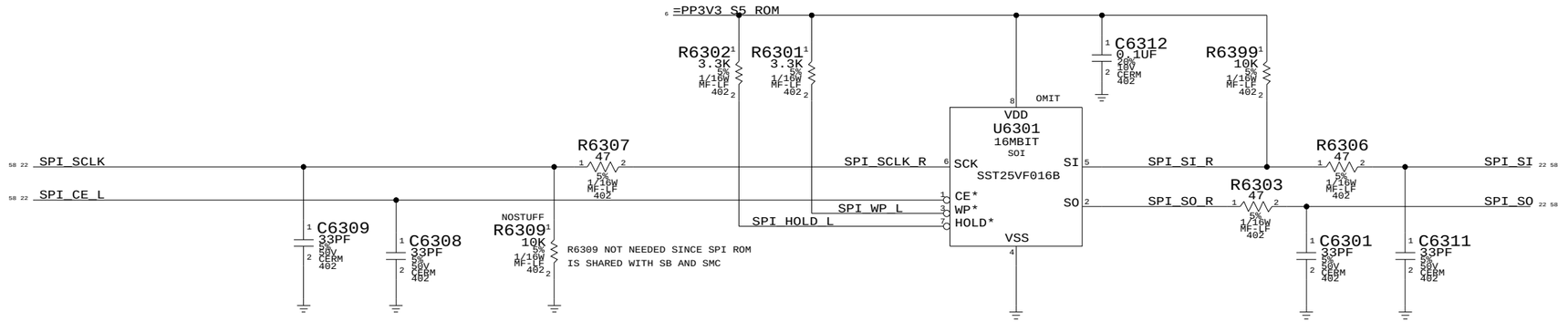


GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 61 OF 110	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

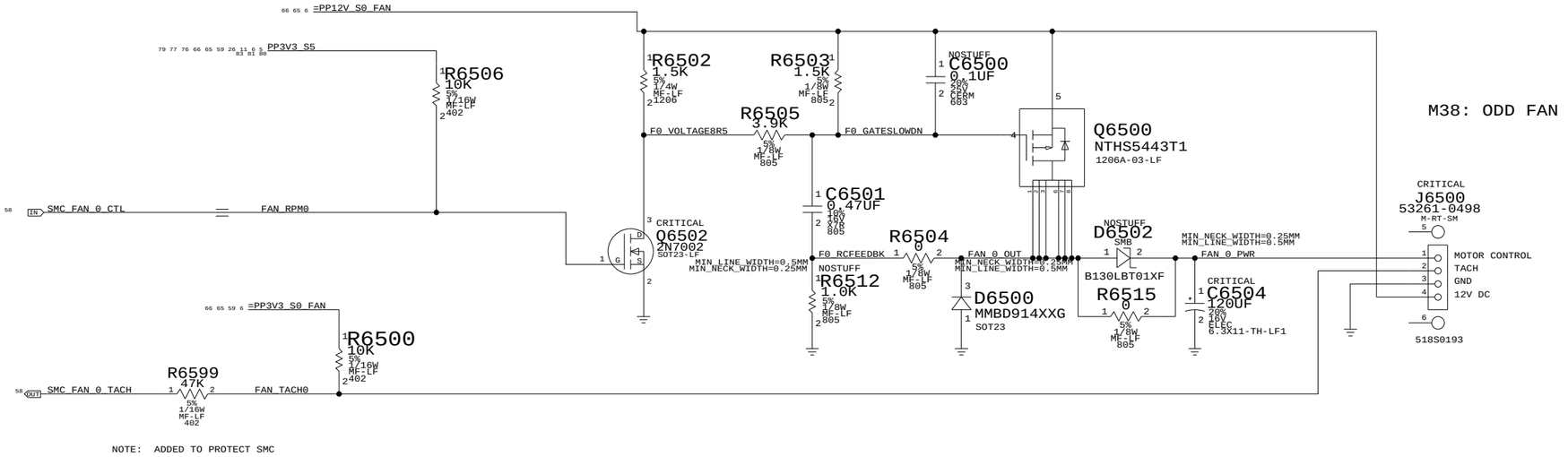
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

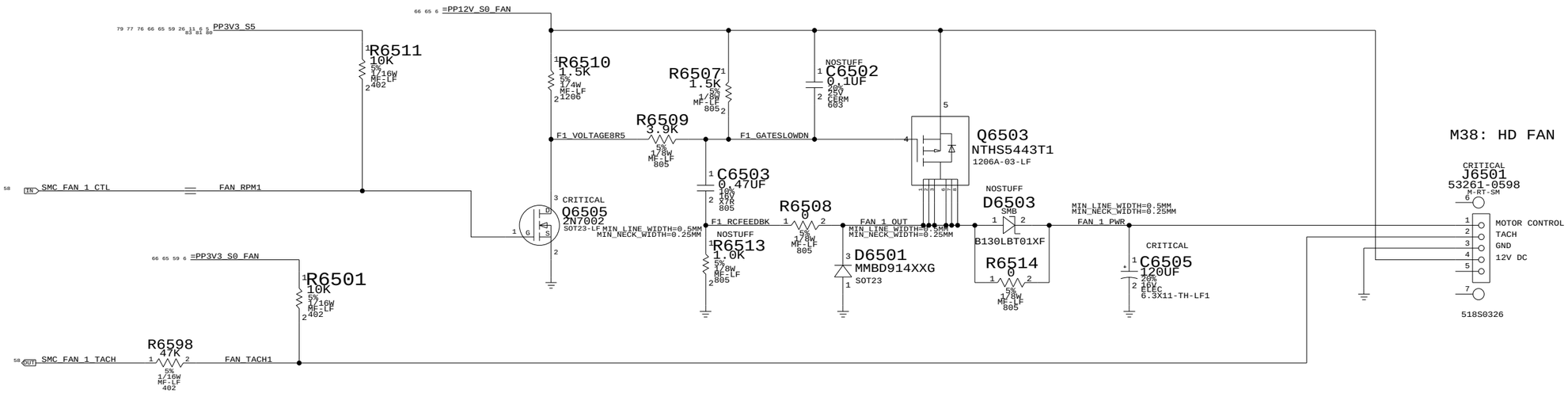
SCALE	SHT	OF
NONE	63	110

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1

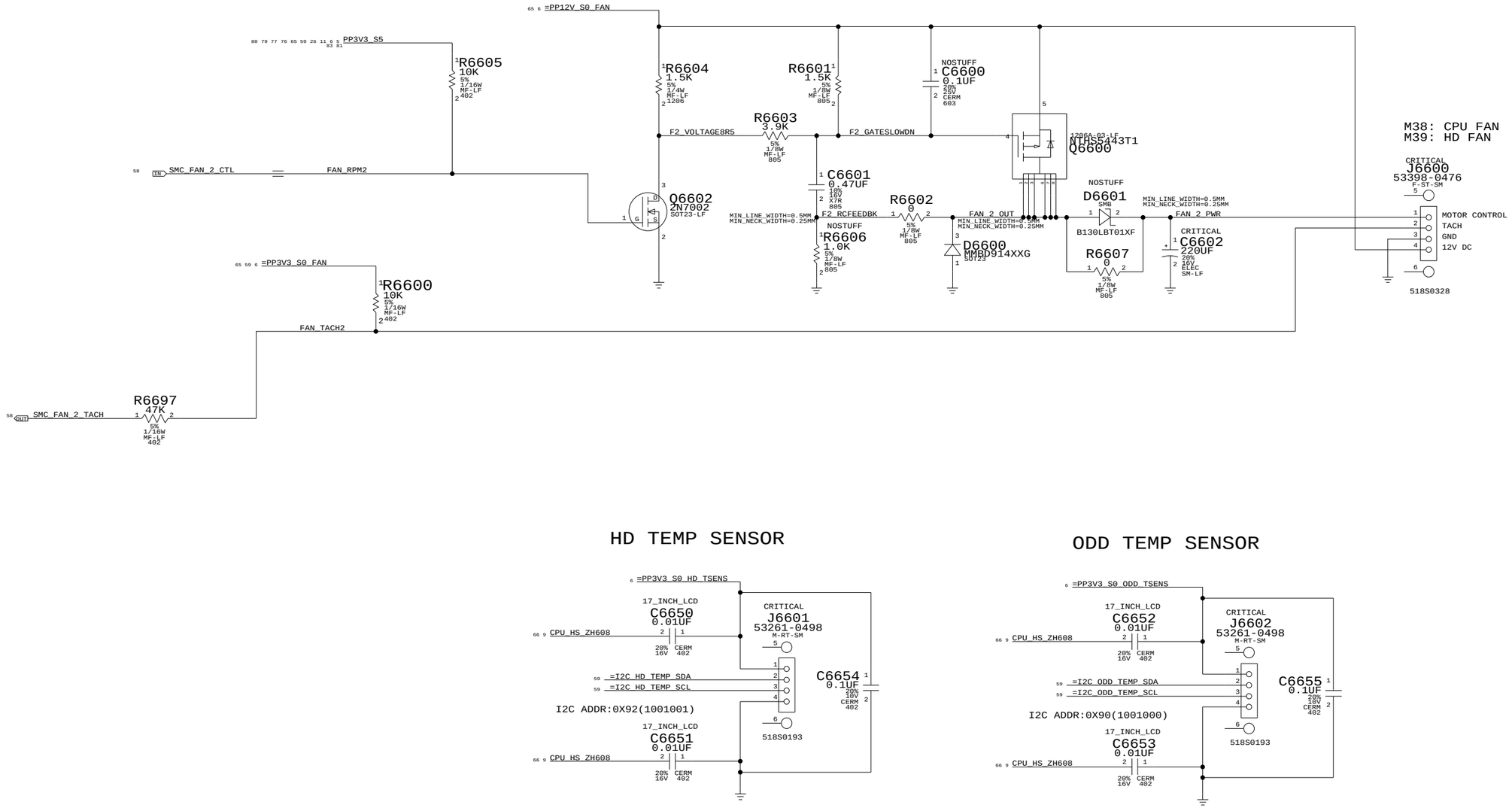


Fan 0, 1 & System Temp

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 65 OF 110	

FAN 2



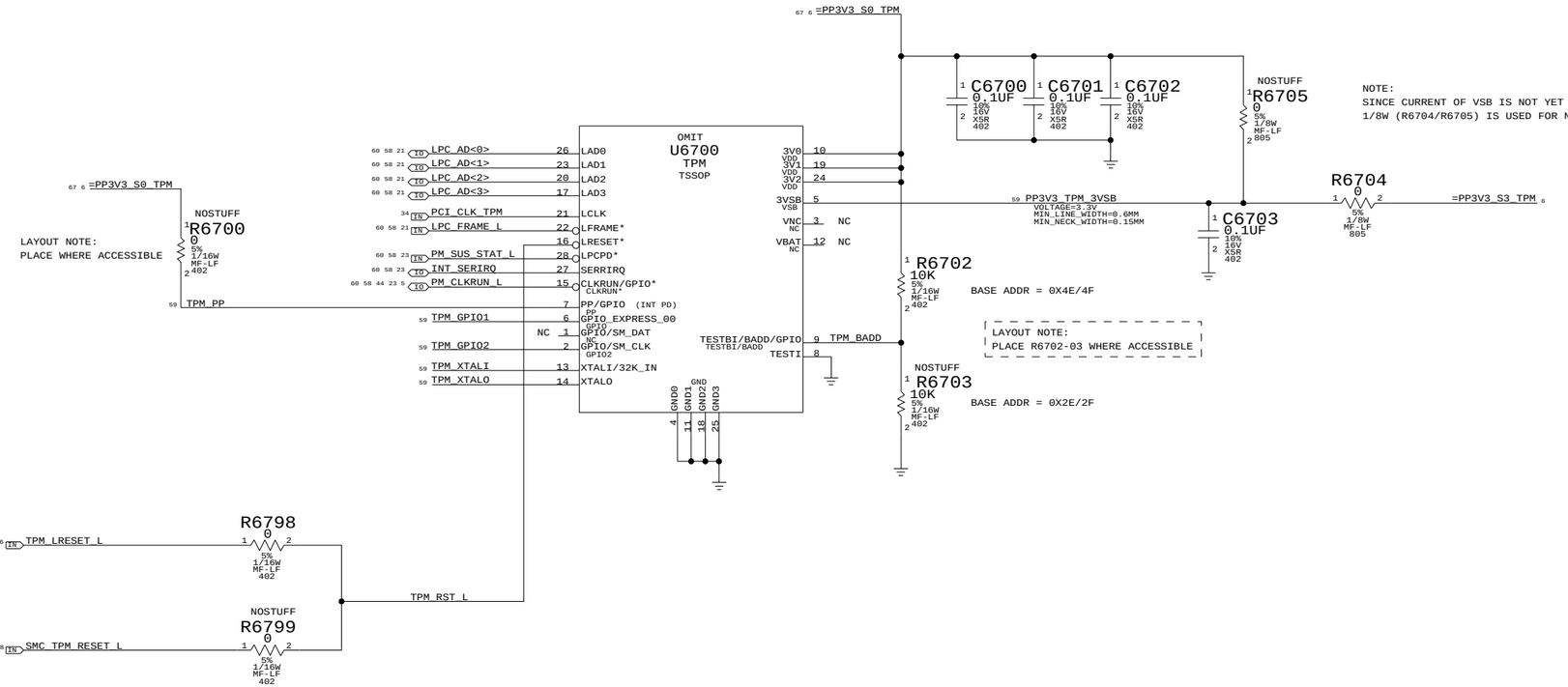
HD TEMP SENSOR

ODD TEMP SENSOR

Fan 2 & HD Temp

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 66 OF 110	



TPM

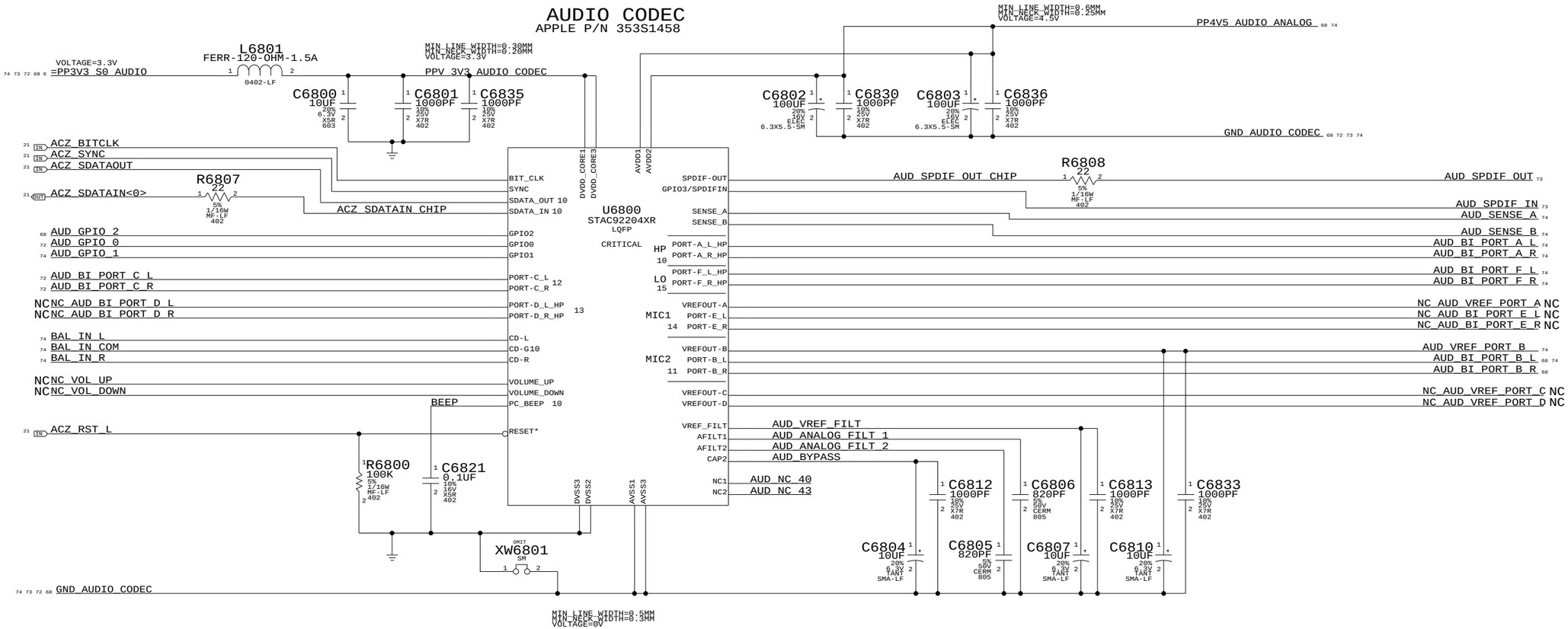
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

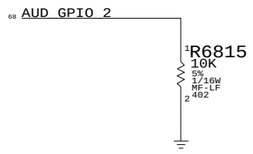
SCALE	SHT
NONE	67 OF 110

AUDIO CODEC
APPLE P/N 353S1458

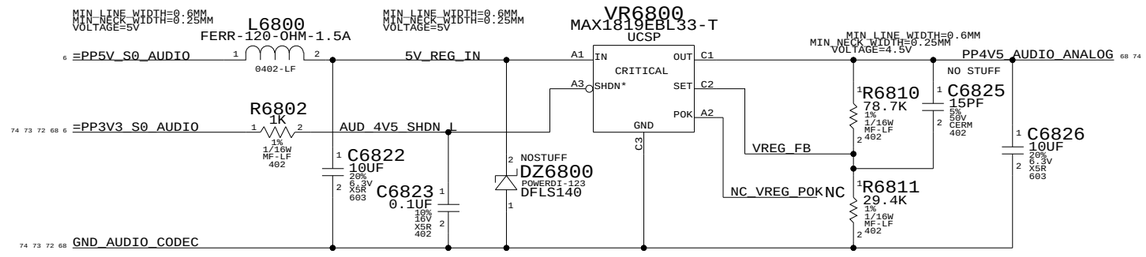


AUD_BI_PORT_B_L = AUD_BI_PORT_B_R

MIC INPUT TO BOTH L&R



4.5V POWER SUPPLY FOR CODEC
APN: 353S1455



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C6802,C6803	FACTORY SHORTAGE
126S0091	126S0092		C7403,C7404	FACTORY SHORTAGE

AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 68 OF 110	

SPEAKER AMP

APPLE P/N 353S0680

=PP12V_S0_AUDIO_SPKRAMP — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

L7200 FERR-250-OHM (SM-1) — PP12V_AUD_SPKRAMP_PLANE — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

C7217 220UF 20% 16V ELEC 6.3X8-SM
C7200 220UF 20% 16V ELEC 6.3X8-SM
C7201 10UF 10% 16V CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 16V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V CERM 1210
C7223 10UF 10% 16V CERM 1210

GND_AUDIO_SPKRAMP_PLANE (72 74)

=PP3V3_S0_AUDIO (74 73 72 68 6)

AUD_BI_PORT_C_L (68) — L7205 1K-OHM-100MA 0603 — AUDSAMPINLN — C7204 0.47UF 10% 16V X7R 805 — AUD_SAMP_INL_N
C7215 100PF 5% 50V CERM 402

GND_AUDIO_CODEC (74 73 72 68)

L7206 1K-OHM-100MA 0603 — AUDSAMPINLP — C7205 0.47UF 10% 16V X7R 805 — AUD_SAMP_INL_P

L7207 1K-OHM-100MA 0603 — AUDSAMPINRP — C7206 0.47UF 10% 16V X7R 805 — AUD_SAMP_INR_P
C7216 100PF 5% 50V CERM 402

AUD_BI_PORT_C_R (68) — L7208 1K-OHM-100MA 0603 — AUDSAMPINRN — C7207 0.47UF 10% 16V X7R 805 — AUD_SAMP_INR_N

R7214 10K 1% 1/16W MF-LF 402 — =PP3V3_S0_AUDIO (74 73 72 68 6 / 72 73)

U7200 MAX9714 QFN-LF

VDD	3, 4, 21, 22	CHOLD	7
INL-	9	OUTL+	31, 32
INL+	10	OUTL-	29, 30
INR+	16	C1+	6
INR-	15	C1-	5
G1	17	OUTR+	27, 28
G2	18	OUTR-	25, 26
FS1	19	SS	12
FS2	20	AGND PAD	13, 33
SHDN*	11	PGND	1, 2, 23, 24
NC	8		
REG	14		

AUD_SAMP_G1 (72) — AUD_SAMP_G2 (72) — AUD_SAMP_FS1 (72) — AUD_SAMP_FS2 (72) — AUD_SAMP_SHDN_L — AUD_MAX9714_VREG (MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM)

MIN_LINE_WIDTH=0.8MM, MIN_NECK_WIDTH=0.2MM — AUD_MAX9714_CHOLD

NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM — AUDSAMPOUTLP — L7201 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTL_P (73)

NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM — AUDSAMPOUTLN — L7202 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTL_N (73)

MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM — AUDSAMPCPP
C7208 0.1UF 10% 50V X7R 603-1
MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM — AUDSAMPCPN

NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM — AUDSAMPOUTRTP — L7203 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTR_P (73)

NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM — AUDSAMPOUTRTN — L7204 180-OHM-1.5A 0603-LF — AUD_SPKR_OUTR_N (73)

MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM — SPKRAMP_SS

C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402

C7209 0.47UF 10% 16V X7R 805

XC7200 50MIL28 — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

XW7201 SM OMIT — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM — GND_AUDIO_SPKRAMP (6 74)

GND_AUDIO_SPKRAMP_PLANE (72 74)

R7215 10K 5% 1/16W MF-LF 402 — PP3V3_INTERCON

NOSTUFF R7216 0 5% 1/16W MF-LF 402 — SPKRAMP_MUTE

R7217 0 5% 1/16W MF-LF 402

Q7200 2N7002DW-X-F SOT-363 (D, G, S)

AUD_GPIO_0 (68) — R7213 100 5% 1/16W MF-LF 402 — AUD_DEBOUNCE — C7221 100PF 5% 50V CERM 402

R7212 10K 5% 1/16W MF-LF 402 *

C7214 1UF 10% 25V X5R 603

NOSTUFF R7219 0 5% 1/16W MF-LF 402

GND_AUDIO_CODEC (74 73 72 68)

GND_AUDIO_SPKRAMP_PLANE (72 74)

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO (74 73 72 68 6)

RP7200 47K 5% 1/16W SM-LF (8 7 6 5 / 1 2 3 4)

AUD_SAMP_FS2 (72)
AUD_SAMP_FS1 (72)
AUD_SAMP_G2 (72)
AUD_SAMP_G1 (72)

NOSTUFF R7218 0 5% 1/16W MF-LF 402

R7208 0 5% 1/16W MF-LF 402

GND_AUDIO_SPKRAMP_PLANE (72 74)

AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE NONE — SHT 72 OF 110

COMBO IN JACK
APPLE P/N 514-0341

CRITICAL
J7300
OPTI-AUD-JCK
WO-RIB-M50
F-5.5-DEG-TH

L7302 180-OHM-1.5A 0603-LF
L7300 180-OHM-1.5A 0603-LF
L7301 180-OHM-1.5A 0603-LF
L7303 180-OHM-1.5A 0603-LF
L7306 180-OHM-1.5A 0603-LF
L7304 180-OHM-1.5A 0603-LF
L7305 180-OHM-1.5A 0603-LF
L7307 180-OHM-1.5A 0603-LF

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
AUD_LI_R_JACK
AUD_LI_R_EMI
AUD_LI_R 74
AUD_LI_L_JACK
AUD_LI_L_EMI
AUD_LI_L 74
AUD_LI_DET_JACK
AUD_LI_DET_EMI
AUD_LI_DET_H 74
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.3MM
AUD_LI_GND_JACK
AUD_LI_GND_EMI
GND_AUDIO_CODEC 68 72 73 74

73 PP3V3_AUDIO_SPDIF_JACK
AUD_SPDIFIN_JACK
R7306 39 5% 1/16W MF-LF 402
AUD_SPDIF_IN 68
LED VCC GND VOUT SHELL
C7326 1UF 10% 6.3V CERM 402
R7305 0 5% 1/16W MF-LF 402
AUD_SPDIF_GND_IN
74 73 GND_CHASSIS_AUDIO_EXTERNAL_J

DZ7302 8V-100PF 402
DZ7300 8V-100PF 402
DZ7324 8V-100PF 402
DZ7301 8V-100PF 402

XW7307 SM
6 GND_CHASSIS_AUDIO_EXTERNAL
GND_CHASSIS_AUDIO_EXTERNAL_J 73 74

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325
PROPERTIES FOR ALL SPKR NETS (OTHERS HIDDEN)
MIN_LINE_WIDTH=0.5MM
NET_SPACING_TYPE=AUDIO
MIN_NECK_WIDTH=0.2MM

J7301
53261-0798
M-RT-SM
72 AUD_SPKR_OUTR_N
72 AUD_SPKR_OUTR_P
72 AUD_SPKR_OUTL_N
72 AUD_SPKR_OUTL_P

XW7300 SM
L7309 180-OHM-1.5A 0603-LF
L7312 180-OHM-1.5A 0603-LF
L7310 180-OHM-1.5A 0603-LF
L7313 180-OHM-1.5A 0603-LF
NET_SPACING_TYPE=AUDIO
74 AUD_MIC_IN_P
AUD_MIC_IN_P_EMI
GND_AUDIO_MIC_CONN
47 AUD_MIC_IN_P_CONN TH
47 AUD_MIC_IN_N_CONN TH
74 AUD_MIC_IN_N
AUD_MIC_IN_N_EMI
NET_SPACING_TYPE=AUDIO
NET_SPACING_TYPE=AUDIO
NET_SPACING_TYPE=AUDIO

DZ7325 8V-100PF 402
DZ7326 8V-100PF 402

TO FHB CONNECTOR PAGE 47
TO POWER SUPPLY PAGE 6
6 GND_CHASSIS_AUDIO_INTERNAL TH

68 AUD_SPDIF_OUT
R7308 100K 5% 1/10W MF-LF 402

L7315 180-OHM-1.5A 0603-LF
L7316 180-OHM-1.5A 0603-LF
L7318 180-OHM-1.5A 0603-LF
L7319 180-OHM-1.5A 0603-LF
L7317 180-OHM-1.5A 0603-LF
L7880 180-OHM-1.5A 0603-LF
L7323 180-OHM-1.5A 0603-LF
L7324 180-OHM-1.5A 0603-LF
L7326 180-OHM-1.5A 0603-LF
L7327 180-OHM-1.5A 0603-LF
L7325 180-OHM-1.5A 0603-LF
L7381 180-OHM-1.5A 0603-LF

74 72 68 6 =PP3V3_S0_AUDIO
PP3V3_AUDIO_SPDIF_EMI
74 AUD_LO_TYPE
AUD_LO_TYPE_EMI
74 AUD_LO_L
AUD_LO_L_EMI
74 AUD_LO_TIP
AUD_LO_TIP_EMI
74 AUD_LO_R
AUD_LO_R_EMI
74 73 72 68 GND_AUDIO_CODEC
GND_AUDIO_CODEC_EMI1
74 73 GND_CHASSIS_AUDIO_EXTERNAL_J

73 PP3V3_AUDIO_SPDIF_JACK
C7317 1UF 10% 6.3V CERM 402
C7318 10UF 20% 6.3V CERM 805-1

DZ7380 8V-100PF 402
DZ7311 8V-100PF 402
DZ7314 8V-100PF 402
DZ7313 8V-100PF 402
DZ7315 8V-100PF 402
DZ7323 8V-100PF 402

LINE OUT JACK
APPLE P/N 514-0338

CRITICAL
J7303
OPTI-AUD-OUT-JCK-M50
F-ANG-TH

AUD_LO_TYPE_JACK TYPE_DET
AUD_LO_L_JACK TIP
AUD_LO_TIP_JACK TIP_DET
AUD_LO_R_JACK RING
GND_1
AUD_LO_GND_JACK GND_2
VIN VCC GND LED
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM AUD_LO_TYPE_JACK
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM AUD_LO_L_JACK
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM AUD_LO_TIP_JACK
MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM AUD_LO_R_JACK
MIN_LINE_WIDTH=0.25MM MIN_NECK_WIDTH=0.2MM
AUD_SPDIF_GND_OUT

R7302 0 5% 1/10W MF-LF 402

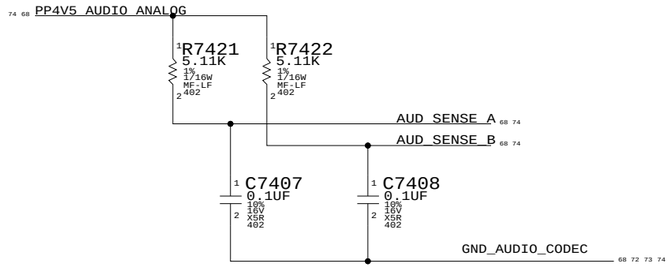
AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=01/10/2006

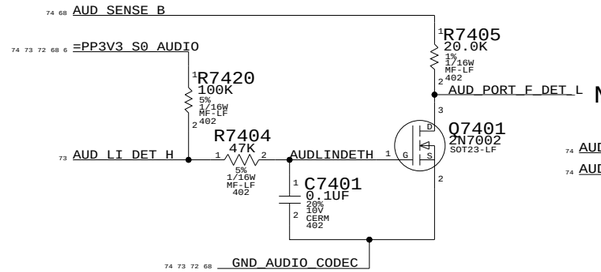
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 73 OF 110	

JACK SENSE PULL UPS(PLACE NEXT TO CODEC)

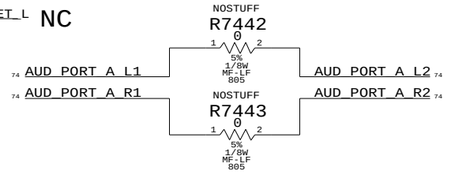


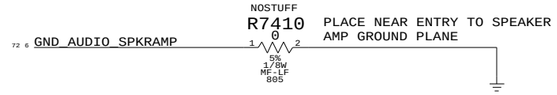
PORT F (LI) PLUG DETECT

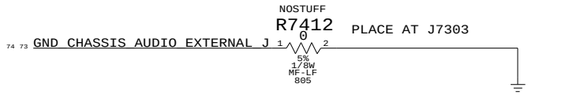


AUDIO GROUND RETURNS

NC

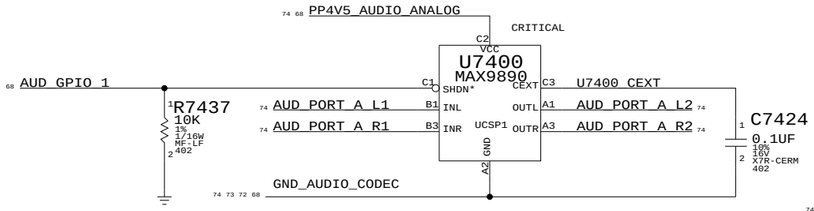




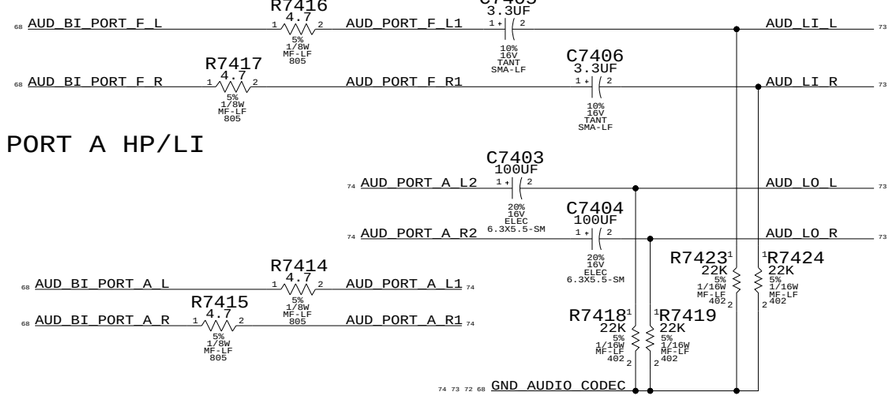


USED PORTS
PORT A HP/LI
PORT B MIC IN, VREF 80%
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E SPDIF OUT DELEGATE
PORT D

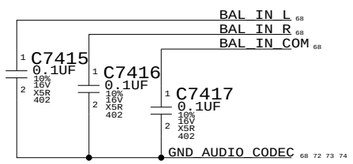


PORT F LI/LO

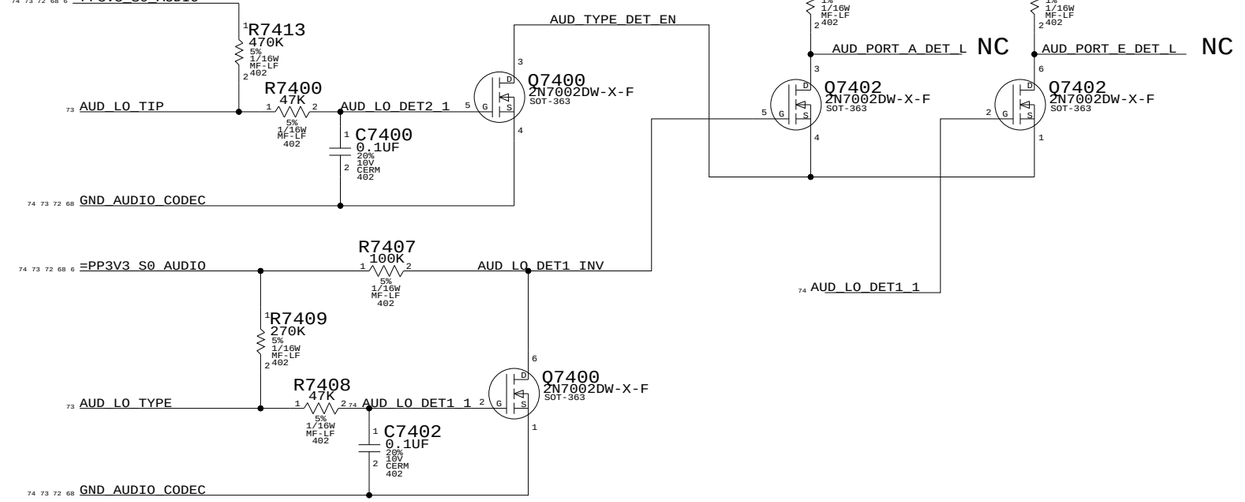


PORT A HP/LI

UNUSED PORT TERMINATION



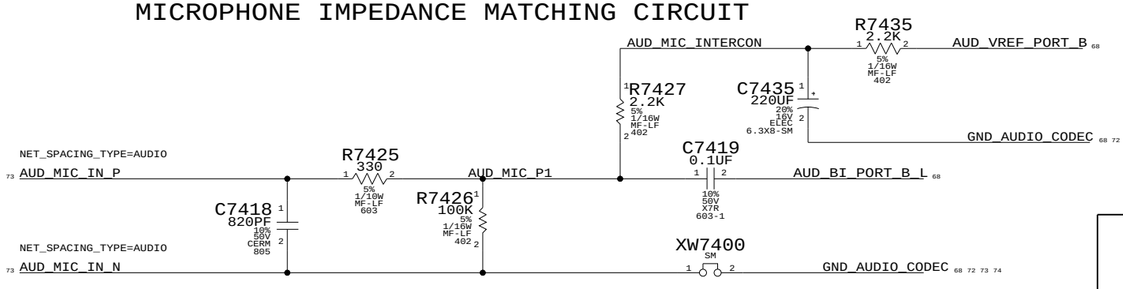
PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



NC

NC

MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 74 OF 110	

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

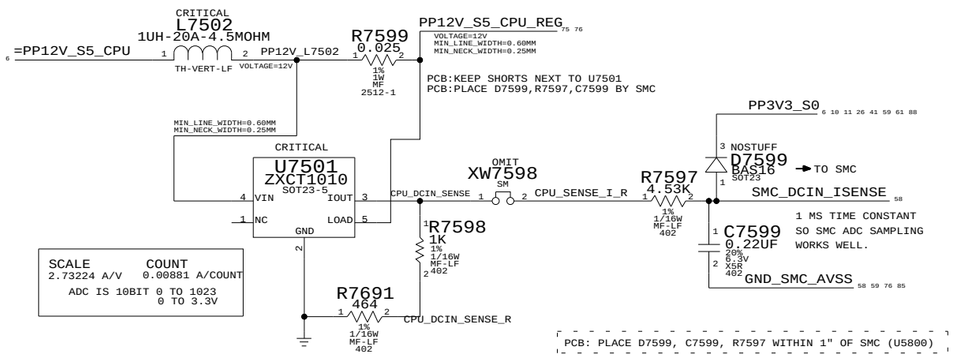
CPU_VCCSENSE_P & N ARE DIFF PAIRS
ROUTE AS 18MIL WIDE, 7MIL SPACE

IMVP6 CPU VCore Regulator	
SYNC_MASTER=POWER	SYNC_DATE=07/08/2005

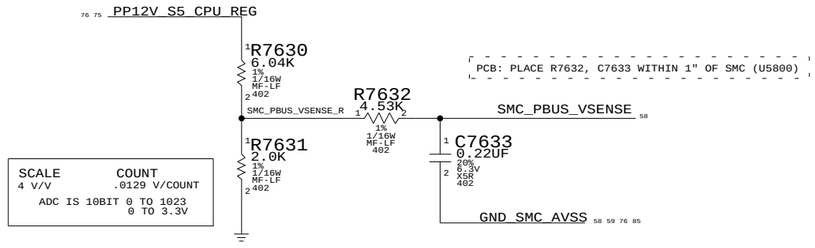
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 75 OF 110	

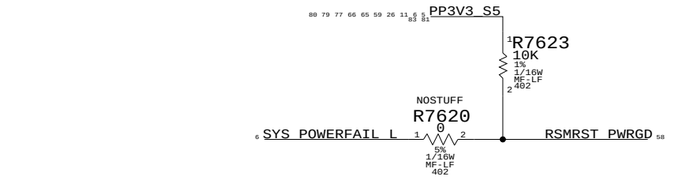
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



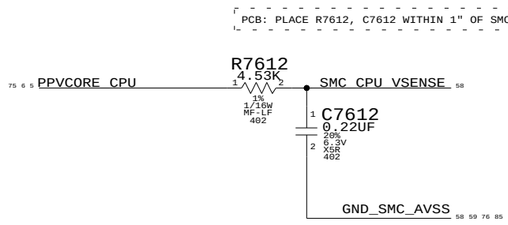
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



SMC PWRGD PULLUP

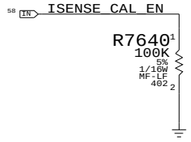


PROCESSOR VCORE SENSE



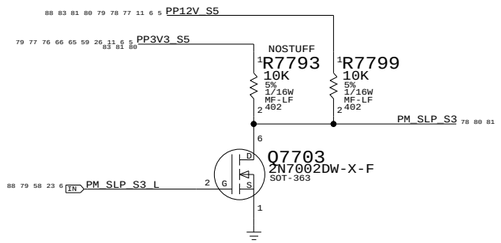
Current Sense Calibration Circuit

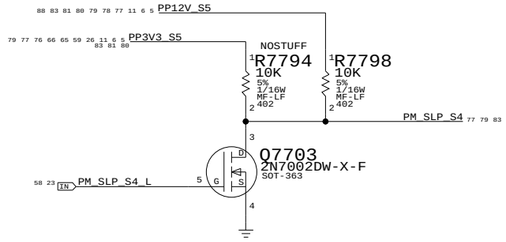
Switches in fixed load on power supplies to calibrate current sense circuits

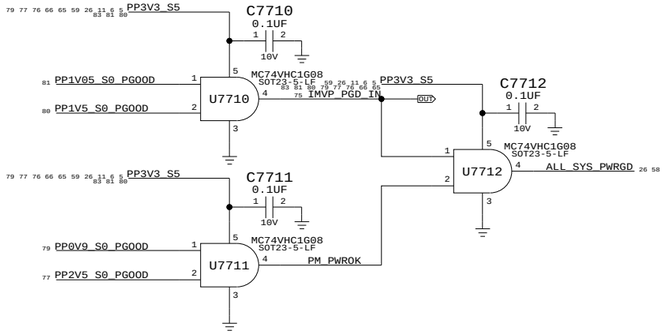


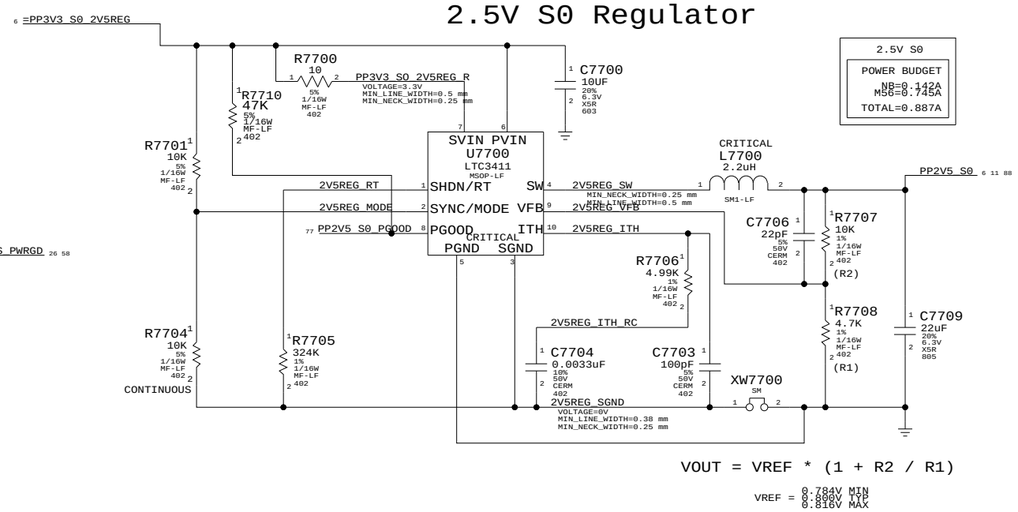
CPU SENSE CIRCUITRIES		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7148	13
	SCALE NONE	SHT 76 OF 110	

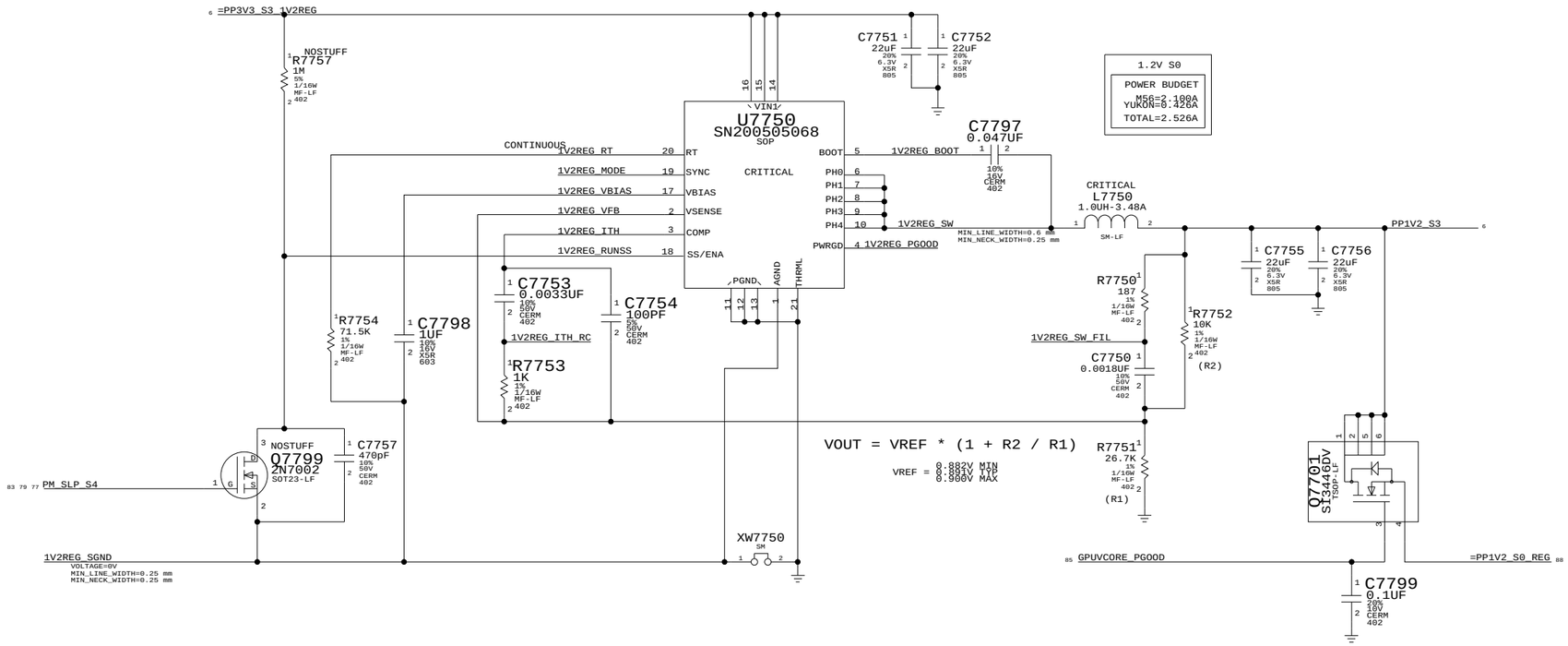








1.2V S3 REGULATOR / 1.2V S0 FET



2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

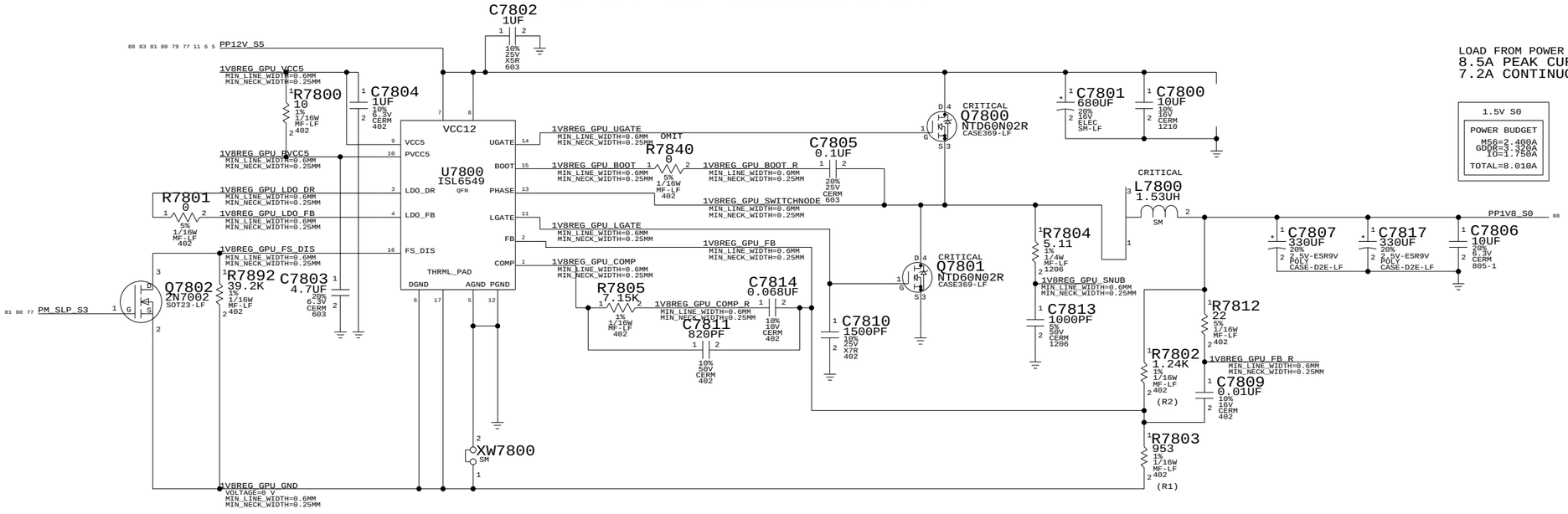
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	77	110

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0514	1	5.11 OHM 0402 1% 1/16W LF	R7840		

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0

POWER BUDGET
M56=2.400A
GDDR=3.730A
IO=1.750A
TOTAL=8.010A

VOUT=VREF*(1+R2/R1)

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.8V GDDR REGULATOR

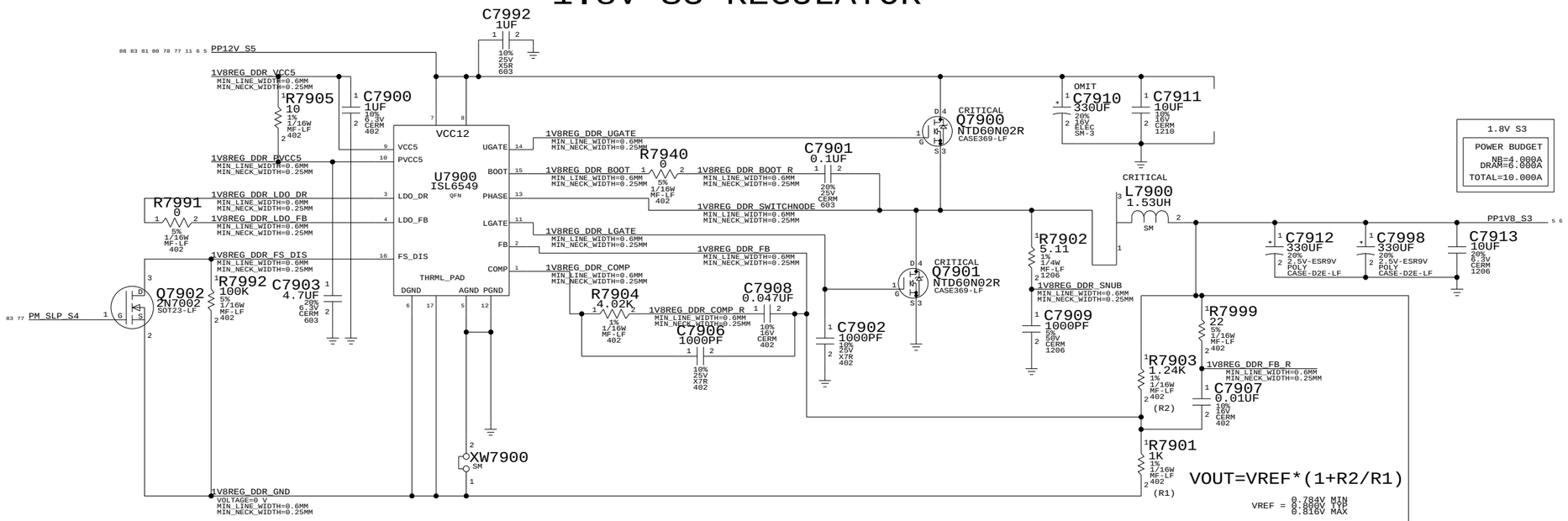
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 78 OF 110	

TRUE

1.8V S3 REGULATOR



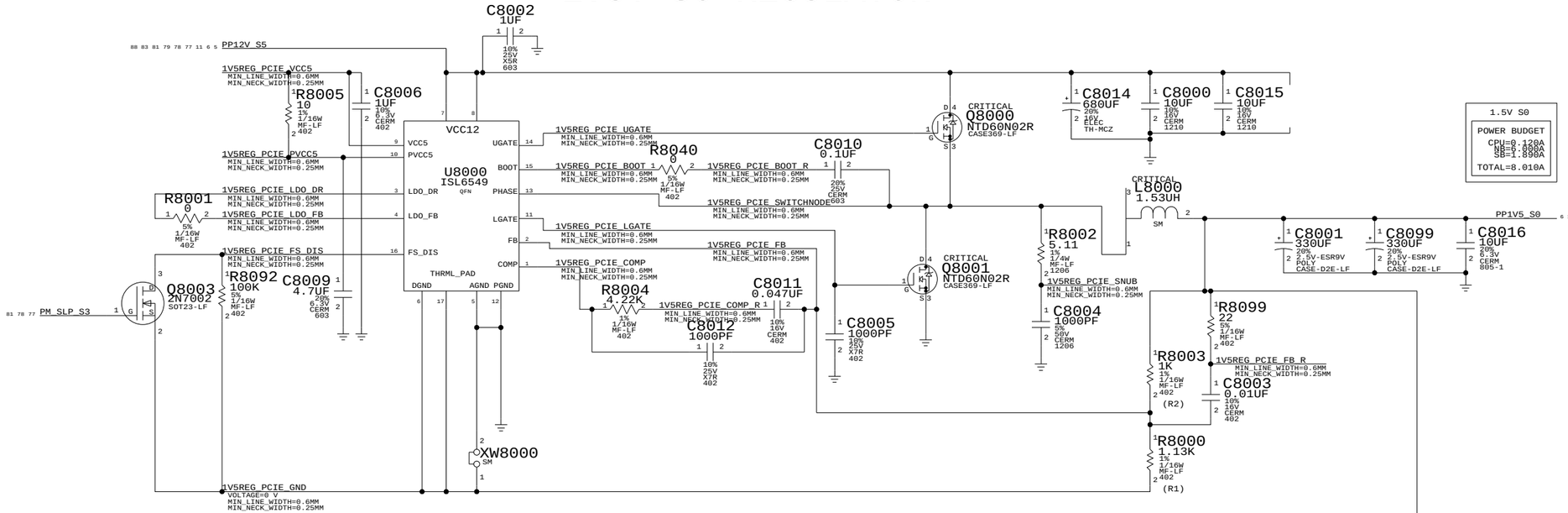
1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 79 OF 110	

1.5V S0 REGULATOR



1.5V Vreg

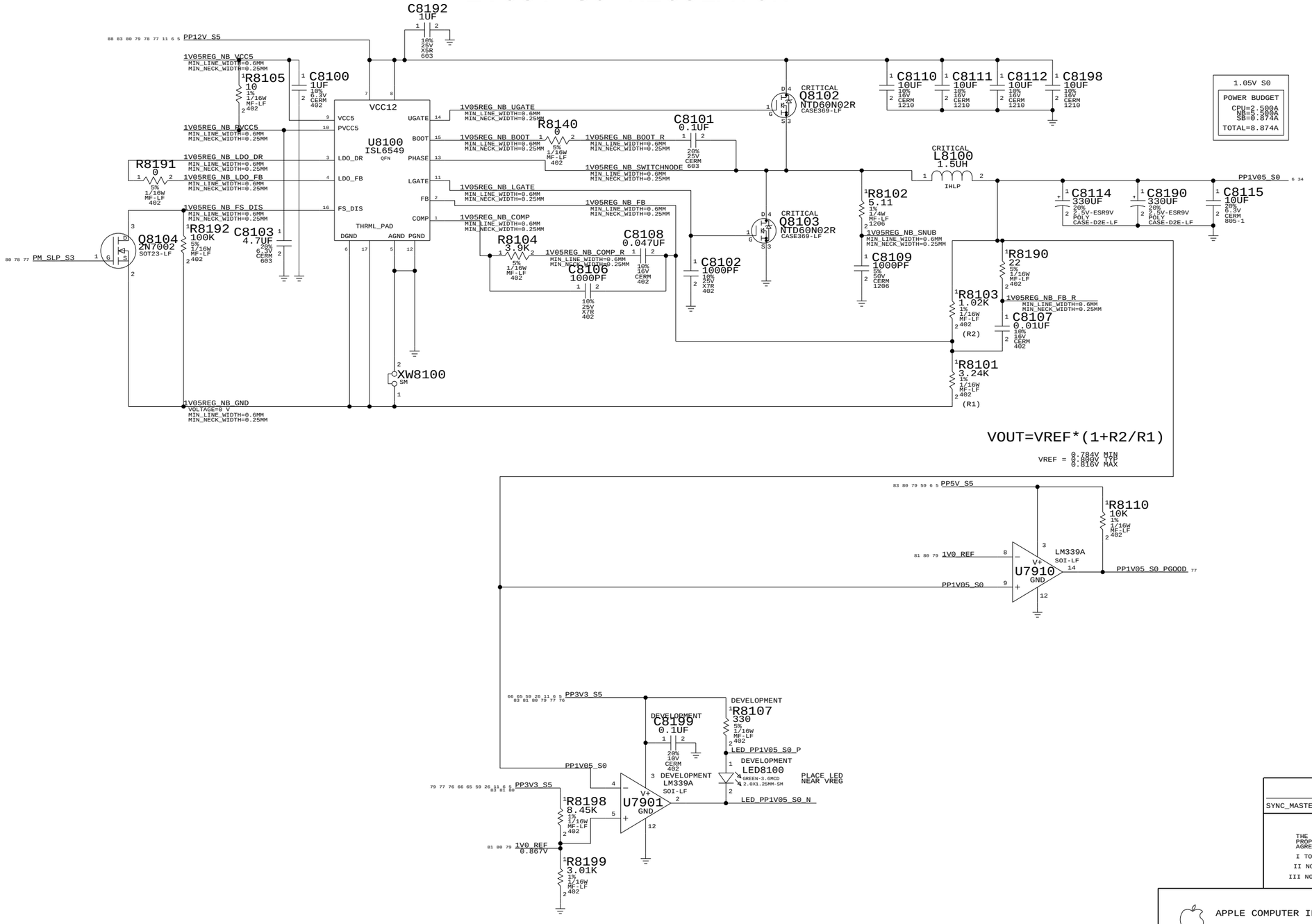
SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT
NONE	80 OF 110

1.05V S0 REGULATOR



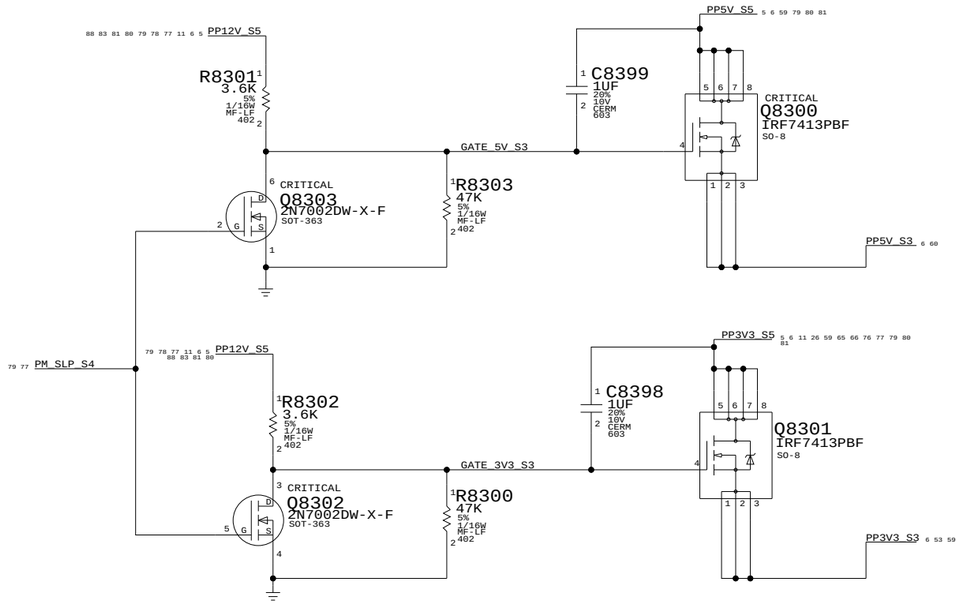
1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE NONE SHT 81 OF 110



5V & 3.3V Fets

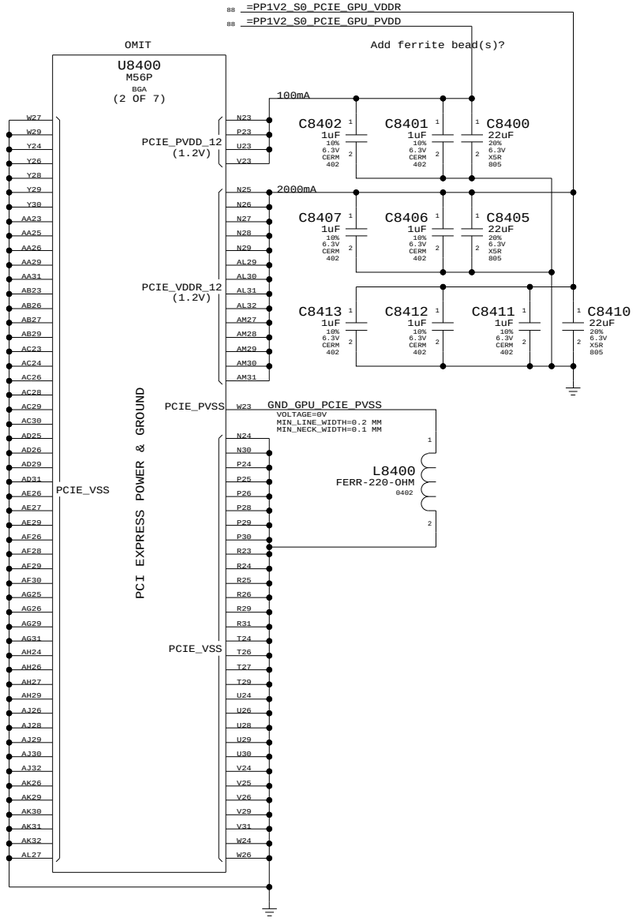
SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

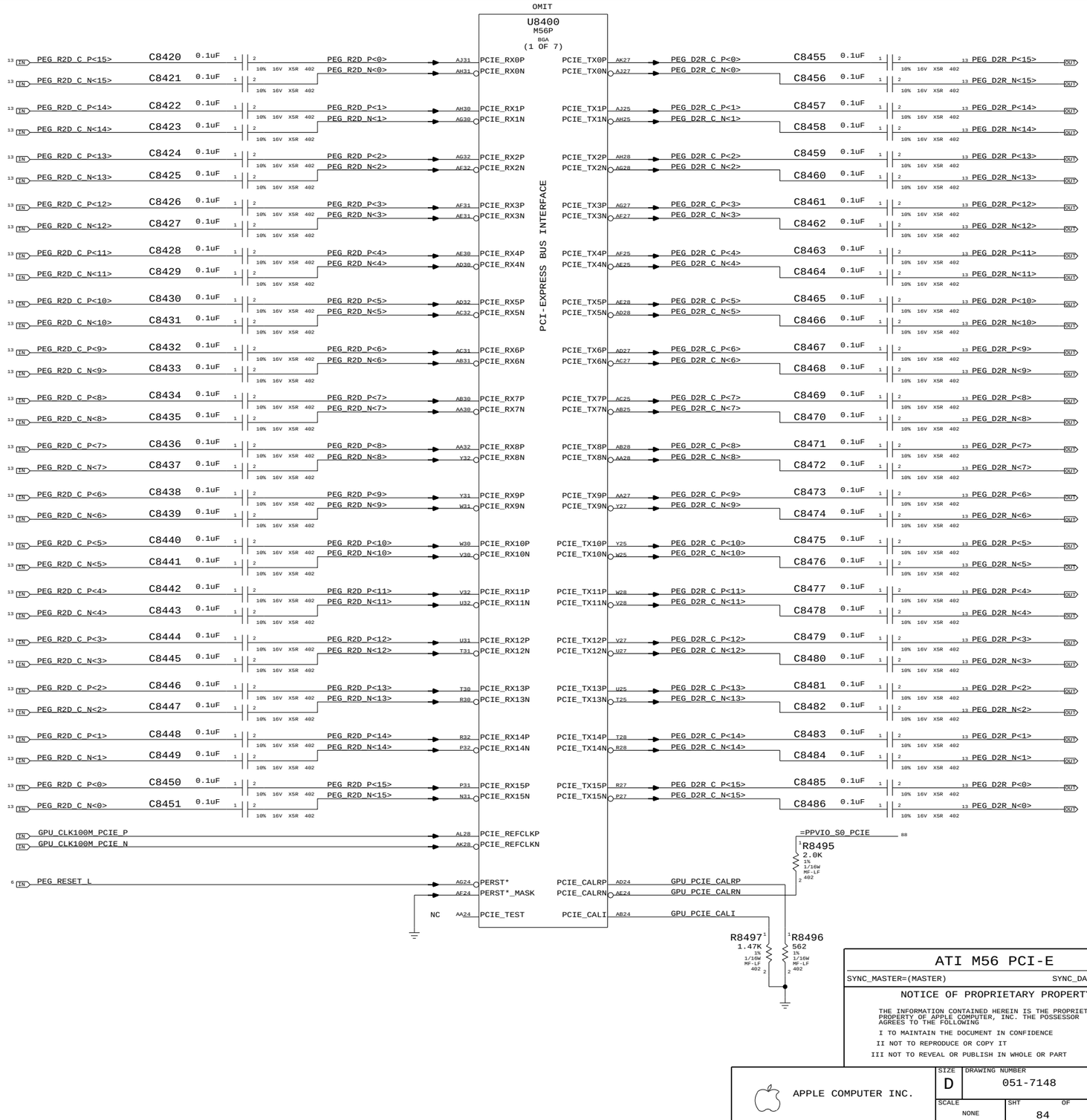
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE: NONE

SHT 83 OF 110





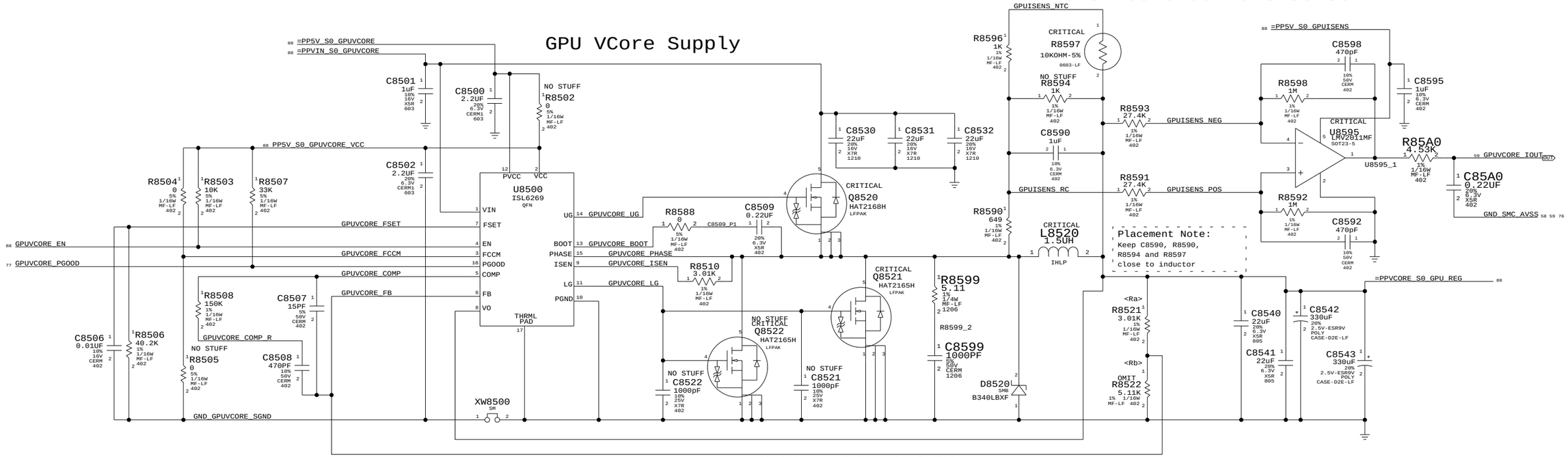
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 84 OF 110	

GPU VCore Current Sense



Back-Bias Positive Supply

=PPVCORE_S0_GPU_BBP ⟶ =PPVOUT_S0_GPUBBP_LDO

Back-Bias Negative Supply

=PNVOUT_S0_GPUBBN_REG

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

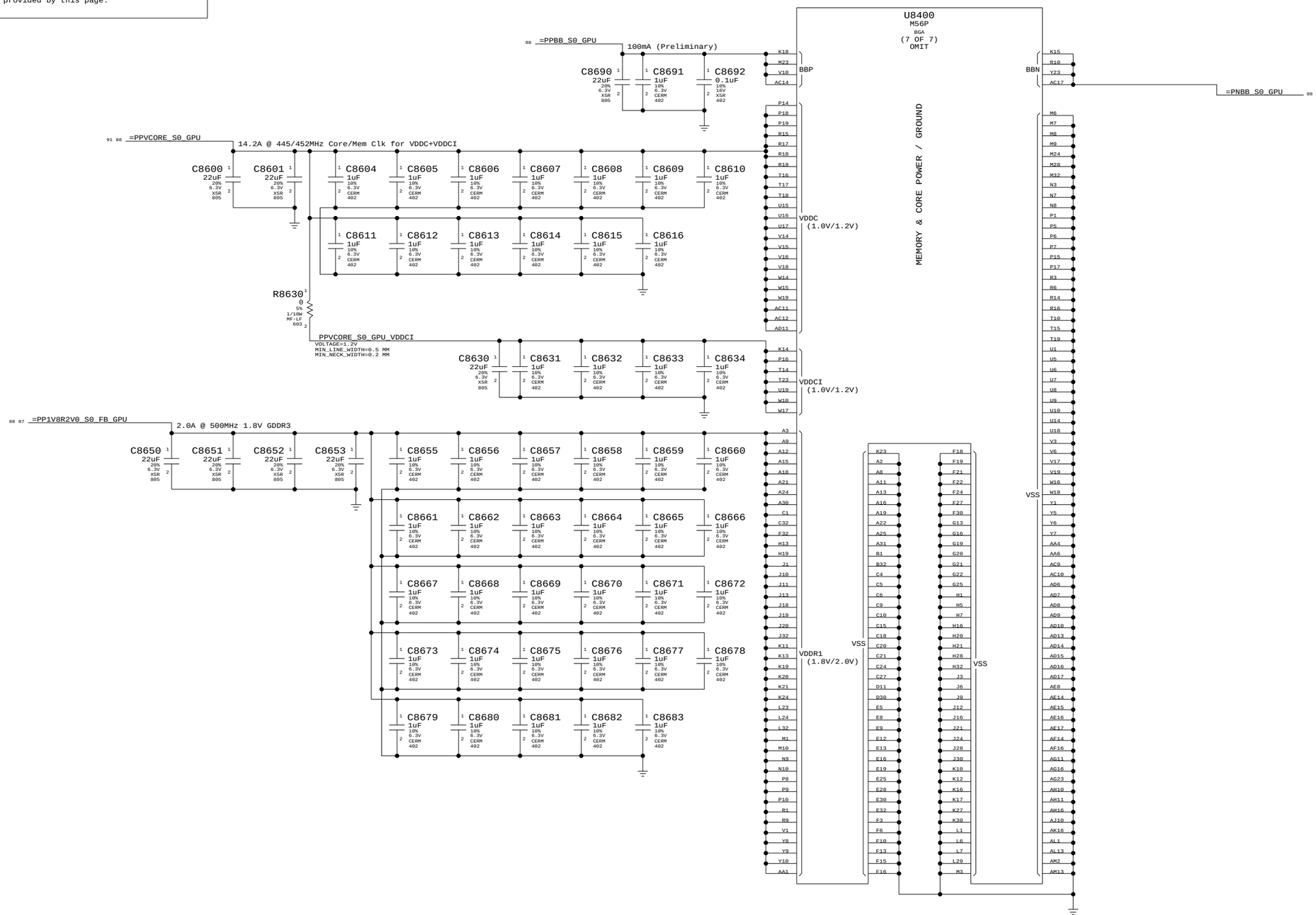
SCALE	SHT	OF
NONE	85	110

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

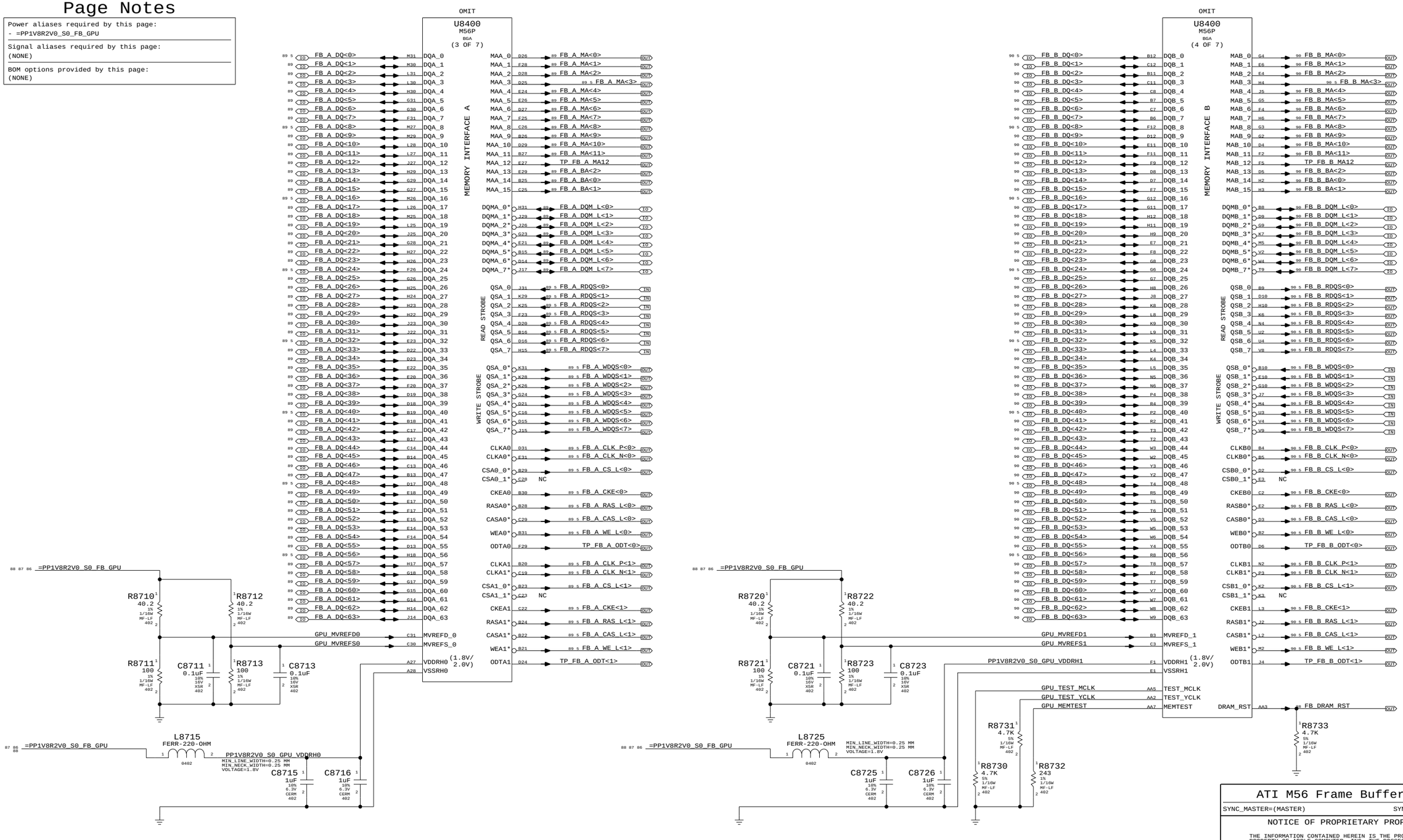
SCALE	SHT	OF
NONE	86	110

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	87	110

"S0" GPU RAILS

ONLY ON IN RUN

59 PP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVCORE_S0_GPU_REG 85
=PPVCORE_S0_GPU 86 91
=PPVCORE_S0_GPU_BBP 85

85 PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V
10 1 R8800 2 603 MF-LF 5% 1/10W
=PP5V_S0_GPUVCORE 85
GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PP1V2_S0_PCIE_GPU_VDDR 84
=PP1V2_S0_PCIE_GPU_PVDD 84
=PPVIO_S0_PCIE 84
=PP1V2_S0_REG 77
=PP1V2_S0_GPU_VDDPLL 91

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVOUT_S0_GPUBBP_LDO 85
=PPBB_S0_GPU 86

PNBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0
=PNVOUT_S0_GPUBBN_REG 85
=PNBB_S0_GPU 86

76 61 59 41 26 11 10 6 PP3V3_S0
=PP3V3_S0_GPUBBP
=PP3V3_S0_GPUBBCTL
=PP3V3_DDC_DVI 97
=PP3V3_S0_LCD 94
=PP3V3_S0_GPU_VDDR3 88 91
=PP3V3_S0_GPU 6 91 93 97
=PP3V3_S0_GPUBBN
=PP3V3_S0_GPU_CLOCKS
=PP3V3_DDC_LCD 94
=PP3V3_GPU 94

77 11 6 PP2V5_S0
=PP2V5_S0_GPU_PVDD 91
=PP2V5_S0_GPU_VDD25 91
=PP2V5_S0_GPU_VDDC_CT 91
=PP2V5_S0_GPU 93

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V
=PP1V8_S0_FB_VDD 89 90
=PP1V8R3V3_S0_GPU_VDDR4 91
=PP1V8R3V3_S0_GPU_VDDR5 91
=PP1V8_S0_FB_VDDQ 89 90
PP1V8_S0 78
=PP1V8R2V0_S0_FB_GPU 86 87

83 81 80 79 78 77 11 6 5 PP12V_S5
=PPVIN_S0_GPUVCORE 85

6 PP12V_S0
=PP12V_GPU 94

97 75 6 PP5V_S0
=PP5V_S0_GPUBBCTL
=PP5V_S0_DVI_DDC 97
=PP5V_S0_GPUISENS 85

85 GPUVCORE_EN
33 1 R8801 2 402 MF-LF 5% 1/16W
PM_SLP_S3_L 6 23 58 77 79

87 FB_DRAM_RST
MAKE_BASE=TRUE
DRAM_RST 5 89 90

M56 GPIOS

=PP3V3_S0_GPU_VDDR3 88 91

94 91 GPU_GPIO_0
10K 1 R8813 2 402 MF-LF 5% 1/16W

GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
10K 1 R8802 2 402 MF-LF 5% 1/16W

GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
NOSTUFF 10K 1 R8803 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_3
NOSTUFF 10K 1 R8804 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_4
NOSTUFF 10K 1 R8805 2 402 MF-LF 5% 1/16W

GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
10K 1 R8806 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_6
NOSTUFF 10K 1 R8807 2 402 MF-LF 5% 1/16W

TP_GPU_GPIO_7
MAKE_BASE=TRUE
GPU_GPIO_7 91

91 GPU_GPIO_8
NOSTUFF 10K 1 R8808 2 402 MF-LF 5% 1/16W

NC_GPU_GPIO_10
MAKE_BASE=TRUE
GPU_GPIO_10 91

91 GPU_GPIO_9
NOSTUFF 10K 1 R8809 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_13
NOSTUFF 10K 1 R8812 2 402 MF-LF 5% 1/16W
ATI_FB_256M

91 GPU_GPIO_12
10K 1 R8810 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_11
NOSTUFF 10K 1 R8811 2 402 MF-LF 5% 1/16W

GPIO 9,13,12,11 = ROM ID CFG
INTERNAL PULL DOWN
0010 = 256 M APERATURE SIZE

ATI_FB_256M
91 GPU_GPIO_24
10K 1 R8830 2 402 MF-LF 5% 1/16W

ATI_FB_HYNIX
91 GPU_GPIO_27
10K 1 R8831 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_28
10K 1 R8832 2 402 MF-LF 5% 1/16W

TMDS_PANEL
91 GPU_GPIO_29
10K 1 R8833 2 402 MF-LF 5% 1/16W

GPU_VCORE_LOW
MAKE_BASE=TRUE
GPU_GPIO_15 91
10K 1 R8850 2 402 MF-LF 5% 1/16W

GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
MAKE_BASE=TRUE
GPU_GPIO_14 91

TP_GPU_GPIO_17
MAKE_BASE=TRUE
GPU_GPIO_17 91

TP_GPU_VGA_R
MAKE_BASE=TRUE
GPU_VGA_R 93

TP_GPU_VGA_G
MAKE_BASE=TRUE
GPU_VGA_G 93

TP_GPU_VGA_B
MAKE_BASE=TRUE
GPU_VGA_B 93

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE
GPU_VGA_HSYNC 93

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE
GPU_VGA_VSYNC 93

TP_GPU_TV_Y
MAKE_BASE=TRUE
GPU_TV_Y 93

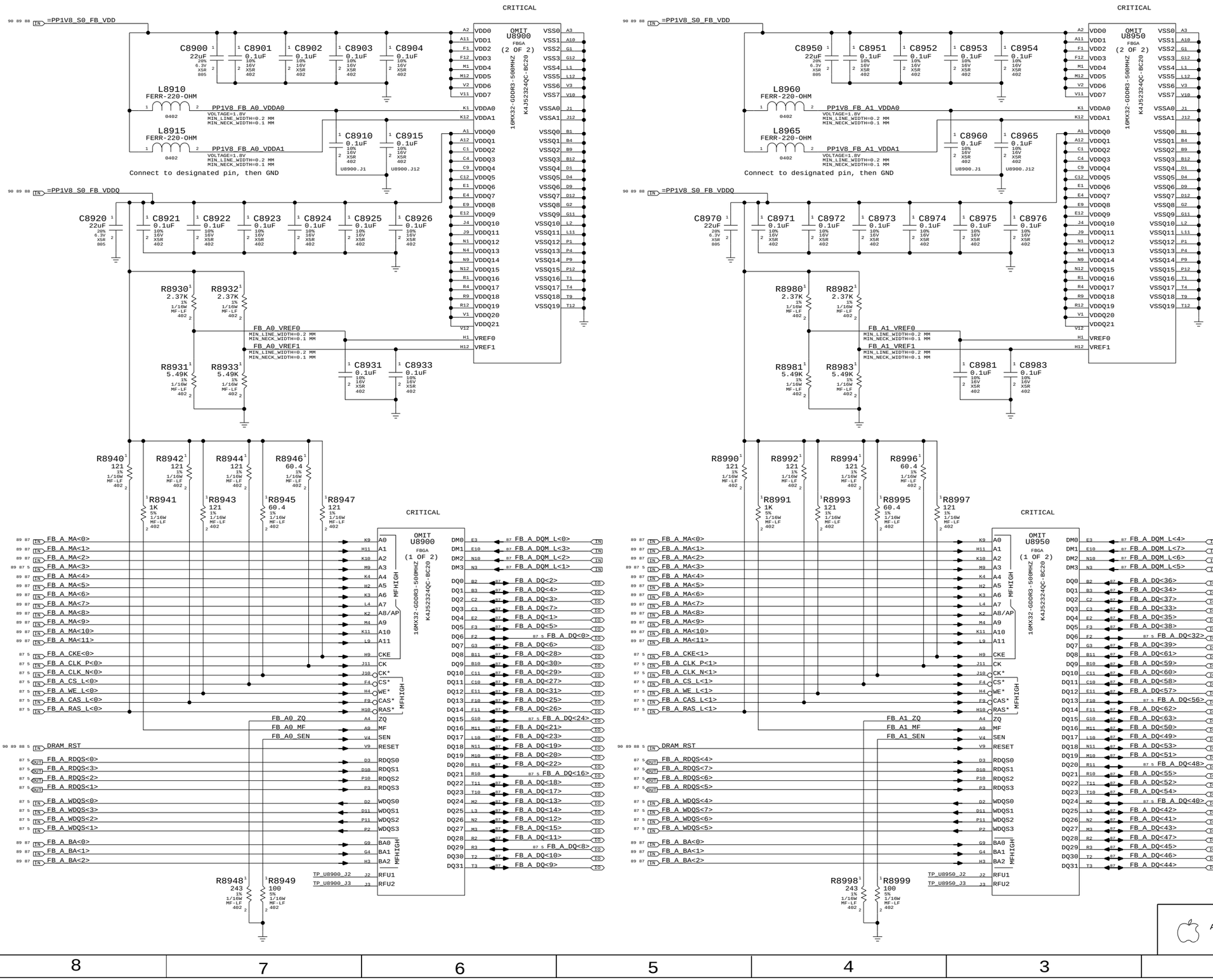
TP_GPU_TV_COMP
MAKE_BASE=TRUE
GPU_TV_COMP 93

TP_GPU_TV_C
MAKE_BASE=TRUE
GPU_TV_C 93

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE
GPU_DDC_B_CLK 93

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE
GPU_DDC_B_DATA 93

GPU MISC



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

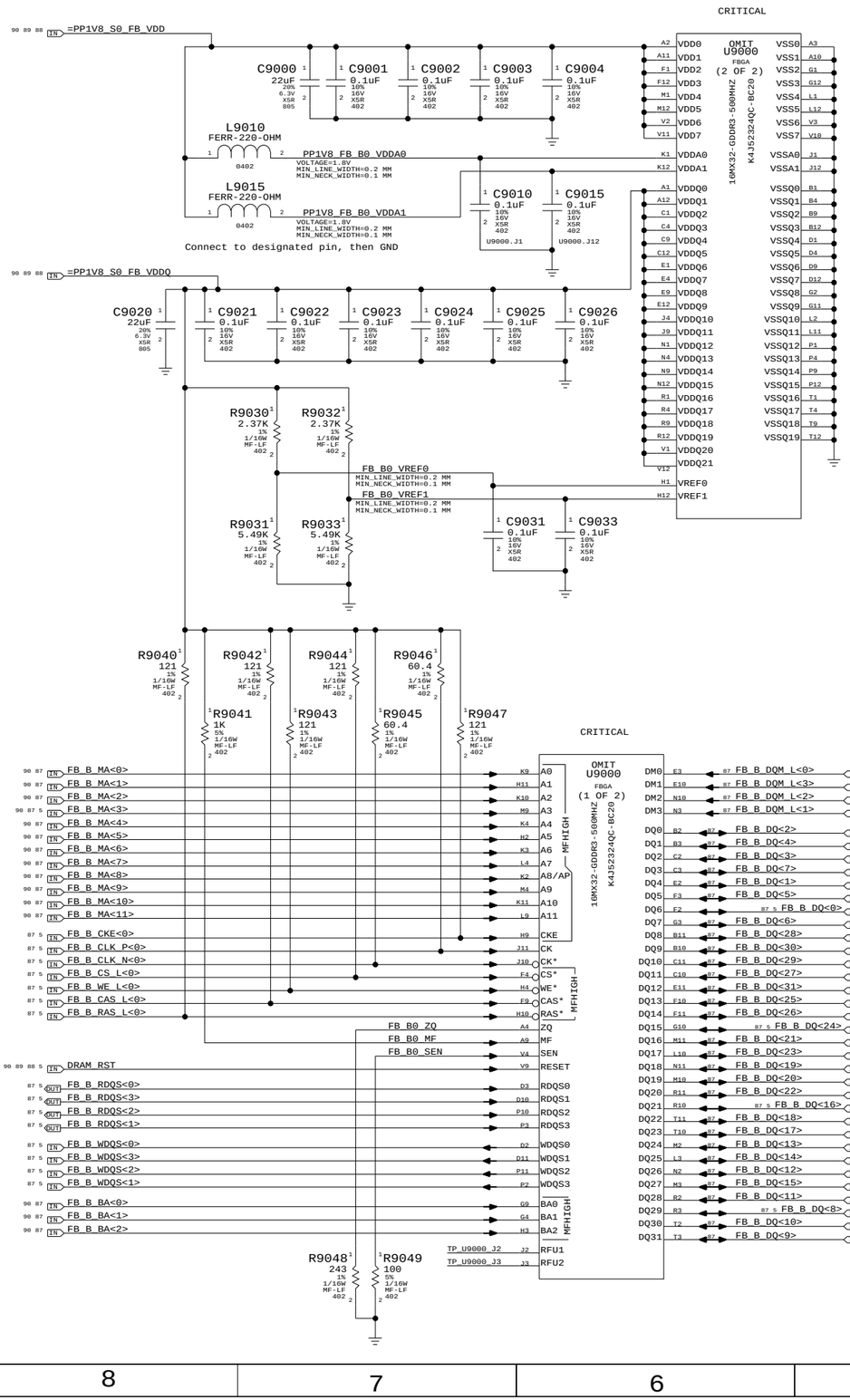
SCALE	SHT	OF
NONE	89	110

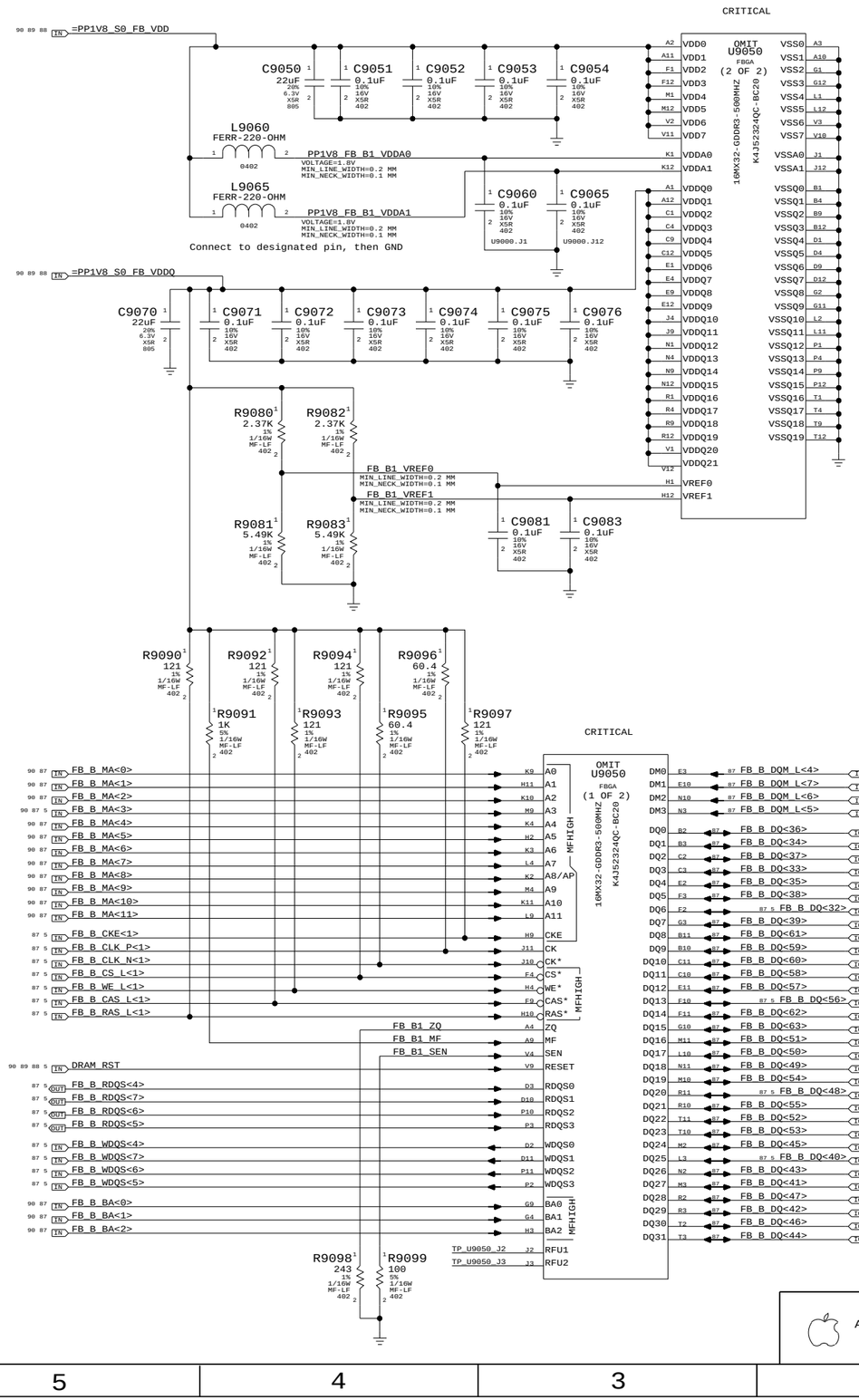
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

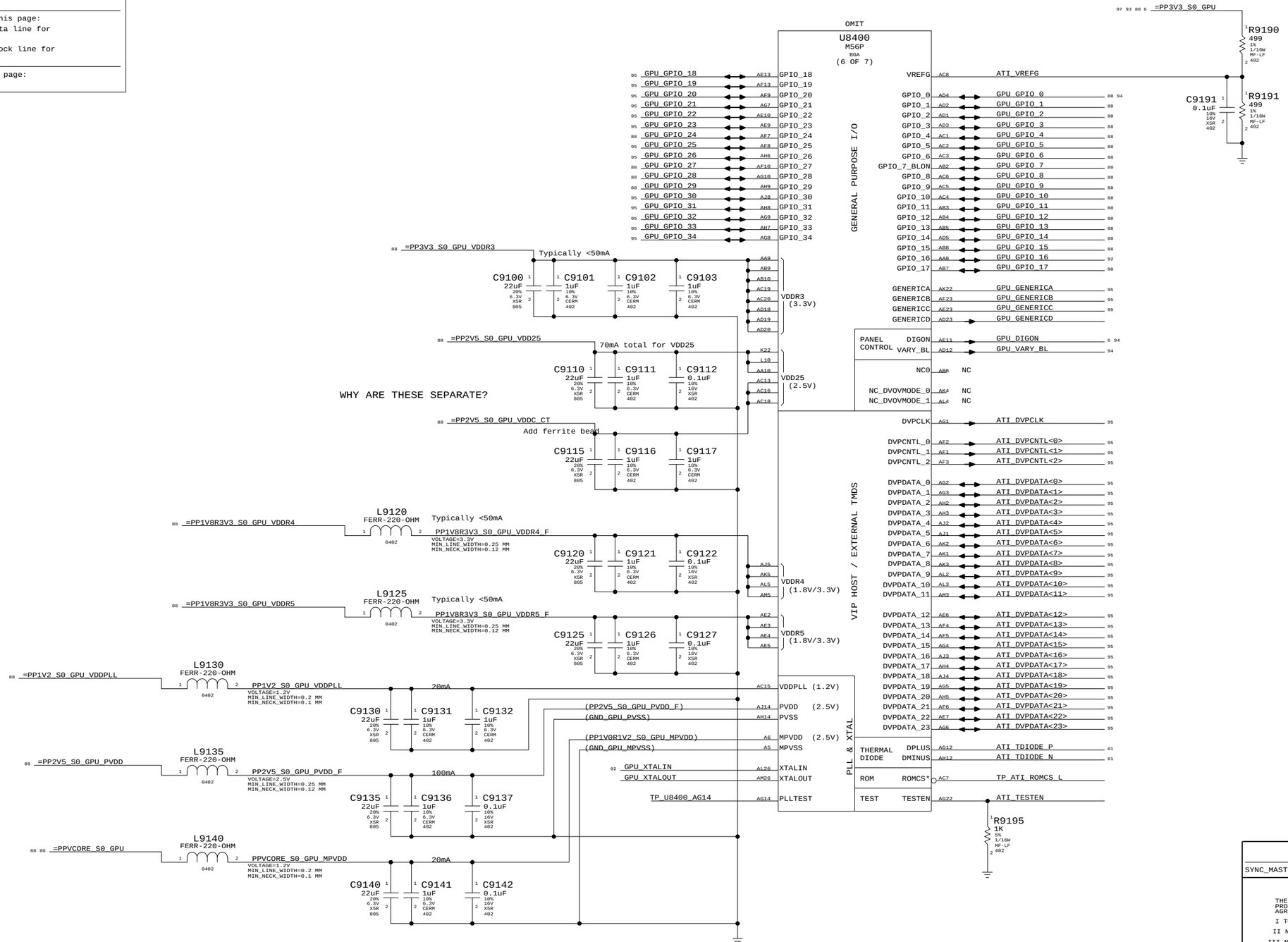
SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 90 OF 110	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

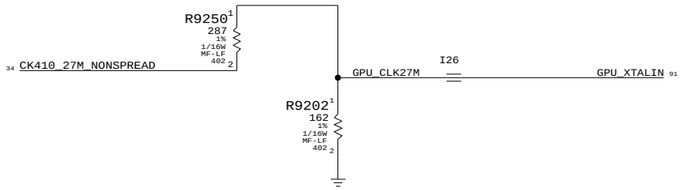
SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 91 OF 110	

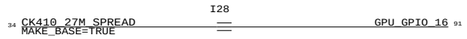
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8





GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	92	110

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents on this page: 605mA

88 =PP2V5_S0_GPU

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=2.5V — 20mA peak
C9300 22uF 20% 6.3V X5R 805
C9301 1uF 10% 6.3V CERM 402
C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V — 150mA peak
C9305 22uF 20% 6.3V X5R 805
C9306 1uF 10% 6.3V CERM 402
C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V — 65mA peak
C9310 22uF 20% 6.3V X5R 805
C9311 1uF 10% 6.3V CERM 402
C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V — 20mA peak
C9315 22uF 20% 6.3V X5R 805
C9316 1uF 10% 6.3V CERM 402
C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=2.5V — 130mA peak
C9320 22uF 20% 6.3V X5R 805
C9321 1uF 10% 6.3V CERM 402
C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V — 20mA peak
C9325 22uF 20% 6.3V X5R 805
C9326 1uF 10% 6.3V CERM 402
C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V — 20mA peak
C9330 22uF 20% 6.3V X5R 805
C9331 1uF 10% 6.3V CERM 402
C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=2.5V — 200mA peak
C9340 22uF 20% 6.3V X5R 805
C9345 22uF 20% 6.3V X5R 805
C9341 1uF 10% 6.3V CERM 402
C9342 0.1uF 10% 16V X5R 402
C9346 0.1uF 10% 16V X5R 402
C9347 0.1uF 10% 16V X5R 402

ATI_RSET 93 — R9350 499 1% 1/16W MF-LF 402
ATI_R2SET 93 — R9351 715 1% 1/16W MF-LF 402

OMIT

U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR
- AL25 AVDD (2.5V)
- AM25 AVDD (2.5V)
- AJ24 AVSS
- AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI

DAC (CRT)
- 93 ATI_RSET → AL22 RSET

DAC2 (TV/CRT2)
- AL16 A2VDD (2.5V)
- AM16 A2VDD (2.5V)
- AL17 A2VSS
- AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- 93 ATI_R2SET → AK14 R2SET

LVDS
- AE19 LVPDD (2.5V)
- AE18 LVPSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AE19, AE20 LVDDR (2.5V)
- AE17, AE18, AE21, AE22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- 97 GPU_HPD → AE11 HPD1

INTEGRATED TMDS
- TXCP AM9 → 97 TMDS_CLK_P (OUT)
- TXCM AL9 → 97 TMDS_CLK_N (OUT)
- TX0P AL10 → 97 TMDS_DATA_P<0> (OUT)
- TX0M AK10 → 97 TMDS_DATA_N<0> (OUT)
- TX1P AM11 → 97 TMDS_DATA_P<1> (OUT)
- TX1M AL11 → 97 TMDS_DATA_N<1> (OUT)
- TX2P AM12 → 97 TMDS_DATA_P<2> (OUT)
- TX2M AL12 → 97 TMDS_DATA_N<2> (OUT)
- TX3P AJ9 → 95 TMDS_DATA_P<3> (OUT)
- TX3M AK9 → 95 TMDS_DATA_N<3> (OUT)
- TX4P AJ11 → 95 TMDS_DATA_P<4> (OUT)
- TX4M AK11 → 95 TMDS_DATA_N<4> (OUT)
- TX5P AJ12 → 95 TMDS_DATA_P<5> (OUT)
- TX5M AK12 → 95 TMDS_DATA_N<5> (OUT)

DAC (CRT)
- R AK24 → 88 GPU_VGA_R (OUT)
- G AM24 → 88 GPU_VGA_G (OUT)
- B AL24 → 88 GPU_VGA_B (OUT)
- HSYNC AJ23 → 88 GPU_VGA_HSYNC (OUT)
- VSYNC AJ22 → 88 GPU_VGA_VSYNC (OUT)

DAC2 (TV/CRT2)
- R2 AK15 → 97 GPU_R2 (OUT)
- G2 AM15 → 97 GPU_G2 (OUT)
- B2 AL15 → 97 GPU_B2 (OUT)
- H2SYNC AE15 → 97 GPU_H2SYNC (OUT)
- V2SYNC AG15 → 97 GPU_V2SYNC (OUT)
- Y AJ15 → 88 GPU_TV_Y (OUT)
- C AJ13 → 88 GPU_TV_C (OUT)
- COMP AH15 → 88 GPU_TV_COMP (OUT)

LVDS
- TXCLK_UP AJ21 → 94 LVDS_U_CLK_P (OUT)
- TXCLK_UN AK21 → 94 LVDS_U_CLK_N (OUT)
- TXOUT_U0P AG18 → 94 LVDS_U_DATA_P<0> (OUT)
- TXOUT_U0N AH18 → 94 LVDS_U_DATA_N<0> (OUT)
- TXOUT_U1P AK20 → 94 LVDS_U_DATA_P<1> (OUT)
- TXOUT_U1N AJ20 → 94 LVDS_U_DATA_N<1> (OUT)
- TXOUT_U2P AG20 → 94 LVDS_U_DATA_P<2> (OUT)
- TXOUT_U2N AH20 → 94 LVDS_U_DATA_N<2> (OUT)
- TXOUT_U3P AH21 → 94 LVDS_U_DATA_P<3> (OUT)
- TXOUT_U3N AG21 → 94 LVDS_U_DATA_N<3> (OUT)
- TXCLK_LP AM18 → 94 93 LVDS_L_CLK_P (OUT)
- TXCLK_LN AL18 → 94 93 LVDS_L_CLK_N (OUT)
- TXOUT_L0P AL19 → 94 93 LVDS_L_DATA_P<0> (OUT)
- TXOUT_L0N AK19 → 94 93 LVDS_L_DATA_N<0> (OUT)
- TXOUT_L1P AM20 → 94 93 LVDS_L_DATA_P<1> (OUT)
- TXOUT_L1N AL20 → 94 93 LVDS_L_DATA_N<1> (OUT)
- TXOUT_L2P AM21 → 94 93 LVDS_L_DATA_P<2> (OUT)
- TXOUT_L2N AL21 → 94 93 LVDS_L_DATA_N<2> (OUT)
- TXOUT_L3P AJ18 → 94 LVDS_L_DATA_P<3> (OUT)
- TXOUT_L3N AK18 → 94 LVDS_L_DATA_N<3> (OUT)

MONITOR IDENTIFICATION
- DDC1CLK AH23 → 97 GPU_DDC_A_CLK (TO)
- DDC1DATA AH22 → 97 GPU_DDC_A_DATA (TO)
- DDC2CLK AG13 → 88 GPU_DDC_B_CLK (TO)
- DDC2DATA AH13 → 88 GPU_DDC_B_DATA (TO)
- DDC3CLK AF12 → 94 93 GPU_DDC_C_CLK (TO)
- DDC3DATA AE12 → 94 93 GPU_DDC_C_DATA (TO)

TERMINATION FOR TMDS USAGE OF LVDS PINS
PLACE CLOSE TO GPU (U8400)

94 93 LVDS_L_CLK_P → TMDS_PANEL R9370 100 5% 1/10W MF-LF 402
94 93 LVDS_L_CLK_N
94 93 LVDS_L_DATA_P<0> → TMDS_PANEL R9371 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<0>
94 93 LVDS_L_DATA_P<1> → TMDS_PANEL R9372 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<1>
94 93 LVDS_L_DATA_P<2> → TMDS_PANEL R9373 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<2>

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

97 91 88 6 =PP3V3_S0_GPU
R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402
94 93 GPU_DDC_C_CLK
94 93 GPU_DDC_C_DATA

ATI M56 Video Interfaces

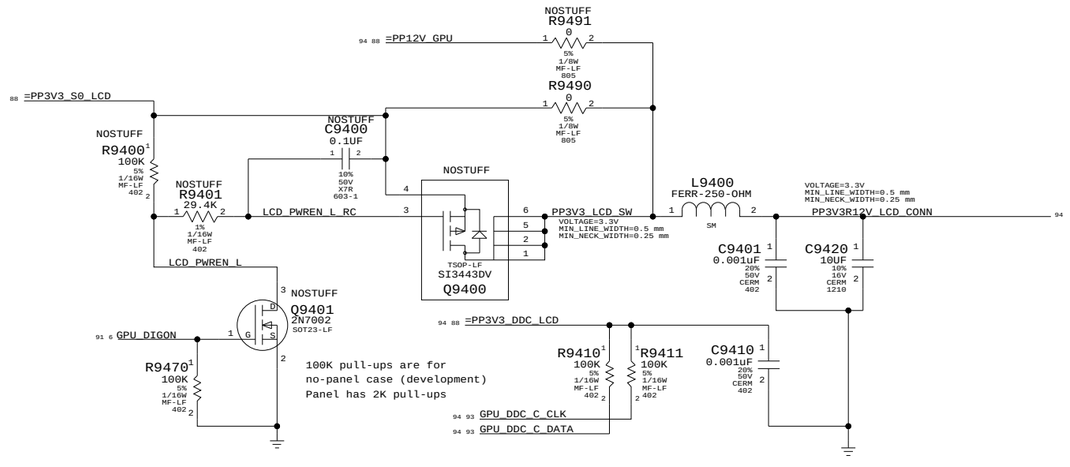
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

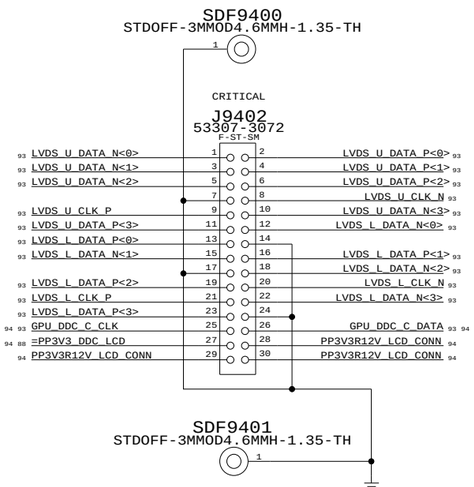
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

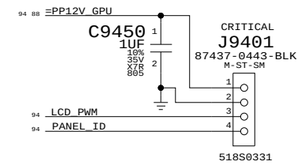
SCALE	SHT	OF
NONE	93	110

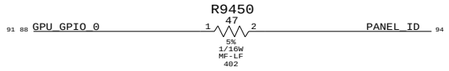
LCD (LVDS) INTERFACE

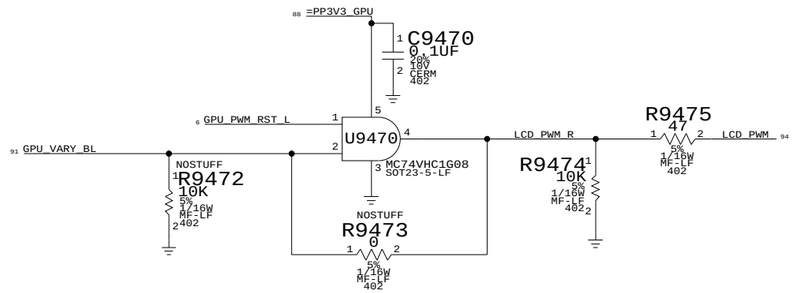




INVERTER INTERFACE







GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL

Internal Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13

SCALE	SHT	OF
NONE	94	110

TP_TMDS_DATA_P<3> — TMDS_DATA_P<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<3> — TMDS_DATA_N<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<4> — TMDS_DATA_P<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<4> — TMDS_DATA_N<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<5> — TMDS_DATA_P<5> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<5> — TMDS_DATA_N<5> 93
MAKE_BASE=TRUE

TP_ATI_DVPDATA<23> — ATI_DVPDATA<23> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<22> — ATI_DVPDATA<22> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<21> — ATI_DVPDATA<21> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<20> — ATI_DVPDATA<20> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<19> — ATI_DVPDATA<19> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<18> — ATI_DVPDATA<18> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<17> — ATI_DVPDATA<17> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<16> — ATI_DVPDATA<16> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<15> — ATI_DVPDATA<15> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<14> — ATI_DVPDATA<14> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<13> — ATI_DVPDATA<13> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<12> — ATI_DVPDATA<12> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<11> — ATI_DVPDATA<11> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<10> — ATI_DVPDATA<10> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<9> — ATI_DVPDATA<9> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<8> — ATI_DVPDATA<8> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<7> — ATI_DVPDATA<7> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<6> — ATI_DVPDATA<6> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<5> — ATI_DVPDATA<5> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<4> — ATI_DVPDATA<4> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<3> — ATI_DVPDATA<3> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<2> — ATI_DVPDATA<2> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<1> — ATI_DVPDATA<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<0> — ATI_DVPDATA<0> 91
MAKE_BASE=TRUE

TP_ATI_DVPCLK — ATI_DVPCLK 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<0> — ATI_DVPCNTL<0> 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<1> — ATI_DVPCNTL<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<2> — ATI_DVPCNTL<2> 91
MAKE_BASE=TRUE

TP_GPU_GPIO<34> — GPU_GPIO_34 91
MAKE_BASE=TRUE

TP_GPU_GPIO<33> — GPU_GPIO_33 91
MAKE_BASE=TRUE

TP_GPU_GPIO<32> — GPU_GPIO_32 91
MAKE_BASE=TRUE

TP_GPU_GPIO<31> — GPU_GPIO_31 91
MAKE_BASE=TRUE

TP_GPU_GPIO<30> — GPU_GPIO_30 91
MAKE_BASE=TRUE
NO_TEST=TRUE

TP_GPU_GPIO<26> — GPU_GPIO_26 91
MAKE_BASE=TRUE

TP_GPU_GPIO<25> — GPU_GPIO_25 91
MAKE_BASE=TRUE

TP_GPU_GPIO<23> — GPU_GPIO_23 91
MAKE_BASE=TRUE

TP_GPU_GPIO<22> — GPU_GPIO_22 91
MAKE_BASE=TRUE

TP_GPU_GPIO<21> — GPU_GPIO_21 91
MAKE_BASE=TRUE

TP_GPU_GPIO<20> — GPU_GPIO_20 91
MAKE_BASE=TRUE

TP_GPU_GPIO<19> — GPU_GPIO_19 91
MAKE_BASE=TRUE

TP_GPU_GPIO<18> — GPU_GPIO_18 91
MAKE_BASE=TRUE

TP_GPU_GENERICA — GPU_GENERICA 91
MAKE_BASE=TRUE

TP_GPU_GENERICB — GPU_GENERICB 91
MAKE_BASE=TRUE

TP_GPU_GENERICC — GPU_GENERICC 91
MAKE_BASE=TRUE

M56 TPS

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 95 OF 110	

DVI INTERFACE

PLACE LEFT SIDE AS CLOSE TO GPU (U8400) AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

93 TMDS_DATA_N<0> — DIFFERENTIAL_PAIR=TMDS_DATA_0
R9701 182 1% 1/10W MF-LF 402
L9700 CRITICAL SYM_VER-1 2012M 90-OHM-300MA
TMDS_CONN_DN<0> 97 — DIFFERENTIAL_PAIR=TMDS_CONN_D0
TMDS_CONN_DP<0> 97 — DIFFERENTIAL_PAIR=TMDS_CONN_D0 — NO_TEST=TRUE
93 TMDS_DATA_P<0> — DIFFERENTIAL_PAIR=TMDS_DATA_0

93 TMDS_DATA_N<1> — DIFFERENTIAL_PAIR=TMDS_DATA_1
R9706 182 1% 1/10W MF-LF 402
L9701 CRITICAL SYM_VER-1 2012M 90-OHM-300MA
TMDS_CONN_DN<1> 97 — DIFFERENTIAL_PAIR=TMDS_CONN_D1
TMDS_CONN_DP<1> 97 — DIFFERENTIAL_PAIR=TMDS_CONN_D1 — NO_TEST=TRUE
93 TMDS_DATA_P<1> — DIFFERENTIAL_PAIR=TMDS_DATA_1

93 TMDS_DATA_N<2> — DIFFERENTIAL_PAIR=TMDS_DATA_2
R9707 182 1% 1/10W MF-LF 402
L9702 CRITICAL SYM_VER-1 2012M 90-OHM-300MA
TMDS_CONN_DN<2> 97 — DIFFERENTIAL_PAIR=TMDS_CONN_D2
TMDS_CONN_DP<2> 97 — DIFFERENTIAL_PAIR=TMDS_CONN_D2 — NO_TEST=TRUE
93 TMDS_DATA_P<2> — DIFFERENTIAL_PAIR=TMDS_DATA_2

93 TMDS_CLK_N — DIFFERENTIAL_PAIR=TMDS_CLK
R9716 90.9 1% 1/10W MF-LF 402
TMDS_CK_TERM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM, NO_TEST=TRUE
C9700 22PF 5% 50V CERM 402
R9717 90.9 1% 1/10W MF-LF 402
93 TMDS_CLK_P — DIFFERENTIAL_PAIR=TMDS_CLK
L9703 165-OHM SM-LF CRITICAL SYM_VER-1
TMDS_CONN_CLKN 97 — DIFFERENTIAL_PAIR=TMDS_CONN_CLK
TMDS_CONN_CLKP 97 — DIFFERENTIAL_PAIR=TMDS_CONN_CLK — NO_TEST=TRUE

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

88 =PP5V_S0_DVI_DDC — CRITICAL F9710 0.5AMP-13.2V SM-LF — PP5V_S0_DDC_FUSE — VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm
L9710 400-OHM-EMI SM-1 — PP5V_S0_DDC — VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm

J9710 MINI-DVI F-ST-SM4

97 DVI_HPD_UF	25	1	TMDS_CONN_DP<2> 97
	17	9	
97 DVI_DDC_CLK_UF	26	2	TMDS_CONN_DN<2> 97
97 DVI_DDC_DATA_UF	18	10	
	27	3	TMDS_CONN_DP<1> 97
	19	11	
	28	4	TMDS_CONN_DN<1> 97
97 VGA_B	20	12	
97 VGA_HSYNC	29	5	TMDS_CONN_DP<0> 97
		13	
	30	6	TMDS_CONN_DN<0> 97
97 VGA_G	22	14	
97 VGA_VSYNC	31	7	TMDS_CONN_CLKP 97
		15	
	32	8	TMDS_CONN_CLKN 97
97 VGA_R	24	16	
	33	34	GND_CHASSIS_VGA 6

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
740S0044	740S0028		F9710	FUSE

3V LEVEL SHIFTERS

88 75 6 PP5V_S0
88 =PP3V3_DDC_DVI
R9710 4.7K 5% 1/16W MF-LF 402
R9712 4.7K 5% 1/16W MF-LF 402
R9720 10K 5% 1/10W MF-LF 402
Q9711 2N7002DW-X-F SOT-363
R9711 100 5% 1/16W MF-LF 402
97 DVI_DDC_CLK_UF — DVI_DDC_CLK — GPU_DDC_A_CLK 93
C9711 100PF 5% 50V CERM 402
R9721 10K 5% 1/16W MF-LF 402
Q9711 2N7002DW-X-F SOT-363
R9713 100 5% 1/16W MF-LF 402
97 DVI_DDC_DATA_UF — DVI_DDC_DATA — GPU_DDC_A_DATA 93
C9713 100PF 5% 50V CERM 402
R9714 20K 5% 1/16W MF-LF 402
97 DVI_HPD_UF — GPU_HPD 93
R9722 100K 5% 1/16W MF-LF 402
D9700 CASE425 MMSZ4681XXG
C9710 0.01uF 20% 50V CERM 603
C9714 100PF 5% 50V CERM 402

ANALOG FILTERING

PLACE CLOSE TO CONNECTOR

93 GPU_B2 — FL9740 LCFILTER CRITICAL SM-220MHZ-LF — VGA_B 97
R9740 75 1% 1/16W MF-LF 402
C9740 3.3PF 0.25% 50V CERM 402
93 GPU_G2 — FL9741 LCFILTER CRITICAL SM-220MHZ-LF — VGA_G 97
R9741 75 1% 1/16W MF-LF 402
C9741 3.3PF 0.25% 50V CERM 402
93 GPU_R2 — FL9742 LCFILTER CRITICAL SM-220MHZ-LF — VGA_R 97
R9742 75 1% 1/16W MF-LF 402
C9742 3.3PF 0.25% 50V CERM 402

VGA SYNC BUFFERS

97 93 91 88 6 =PP3V3_S0_GPU
C9750 0.1UF 20% 10V CERM 402
U9750 74AHC1G32 SM-LF
93 GPU_V2SYNC — GPU_VSYNC_BUF — R9750 33 5% 1/16W MF-LF 402 — VGA_VSYNC 97

97 93 91 88 6 =PP3V3_S0_GPU
C9751 0.1UF 20% 10V CERM 402
U9751 74AHC1G32 SM-LF
93 GPU_H2SYNC — GPU_HSYNC_BUF — R9751 33 5% 1/16W MF-LF 402 — VGA_HSYNC 97

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

External Display Conns

SYNC_MASTER=BOZEMAN — SYNC_DATE=04/14/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7148	13
SCALE: NONE	SHT 97 OF 110	

Title: Basenet Report
Design: m38a
Date: Jun 21 19:41:15 2006

Base nets and synonyms for m38a_lib.M38A(@m38a_lib.m38a(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
0V7_REF	0V7_REF - @m38a_lib.M38A	79A3
1V0_REF	1V0_REF - @m38a_lib.M38A	79A5 80A5 81A5 81B3
1V2REG_BOOT	1V2REG_BOOT - @m38a_lib.M38A	77B5
1V2REG_ITH	1V2REG_ITH - @m38a_lib.M38A	77B6
1V2REG_ITH_RC	1V2REG_ITH_RC - @m38a_lib.M38A	77B6
1V2REG_MODE	1V2REG_MODE - @m38a_lib.M38A	77B6
1V2REG_PGOOD	1V2REG_PGOOD - @m38a_lib.M38A	77B5
1V2REG_RT	1V2REG_RT - @m38a_lib.M38A	77B6
1V2REG_RUNSS	1V2REG_RUNSS - @m38a_lib.M38A	77B6
1V2REG_SGND	1V2REG_SGND - @m38a_lib.M38A	77A8
1V2REG_SW	1V2REG_SW - @m38a_lib.M38A	77B5
1V2REG_SW_FIL	1V2REG_SW_FIL - @m38a_lib.M38A	77B4
1V2REG_VBIAS	1V2REG_VBIAS - @m38a_lib.M38A	77B6
1V2REG_VFB	1V2REG_VFB - @m38a_lib.M38A	77B6
1V3_REF	1V3_REF - @m38a_lib.M38A	80B3
1V05REG_NB_BOOT	1V05REG_NB_BOOT - @m38a_lib.M38A	81C6
1V05REG_NB_BOOT_R	1V05REG_NB_BOOT_R - @m38a_lib.M38A	81C5
1V05REG_NB_COMP	1V05REG_NB_COMP - @m38a_lib.M38A	81C6
1V05REG_NB_COMP_R	1V05REG_NB_COMP_R - @m38a_lib.M38A	81C5
1V05REG_NB_FB	1V05REG_NB_FB - @m38a_lib.M38A	81C5
1V05REG_NB_FB_R	1V05REG_NB_FB_R - @m38a_lib.M38A	81C3
1V05REG_NB_FS_DIS	1V05REG_NB_FS_DIS - @m38a_lib.M38A	81C7
1V05REG_NB_GND	1V05REG_NB_GND - @m38a_lib.M38A	81B7
1V05REG_NB_LDO_DR	1V05REG_NB_LDO_DR - @m38a_lib.M38A	81C7
1V05REG_NB_LDO_FB	1V05REG_NB_LDO_FB - @m38a_lib.M38A	81C7
1V05REG_NB_LGATE	1V05REG_NB_LGATE - @m38a_lib.M38A	81C6
1V05REG_NB_PVCC5	1V05REG_NB_PVCC5 - @m38a_lib.M38A	81D7
1V05REG_NB_SNUB	1V05REG_NB_SNUB - @m38a_lib.M38A	81C3
1V05REG_NB_SWITCHNODE	1V05REG_NB_SWITCHNODE - @m38a_lib.M38A	81C5
1V05REG_NB_UGATE	1V05REG_NB_UGATE - @m38a_lib.M38A	81D6
1V05REG_NB_VCC5	1V05REG_NB_VCC5 - @m38a_lib.M38A	81D7
1V5REG_PCIE_BOOT	1V5REG_PCIE_BOOT - @m38a_lib.M38A	80C6
1V5REG_PCIE_BOOT_R	1V5REG_PCIE_BOOT_R - @m38a_lib.M38A	80C5
1V5REG_PCIE_COMP	1V5REG_PCIE_COMP - @m38a_lib.M38A	80C6
1V5REG_PCIE_COMP_R	1V5REG_PCIE_COMP_R - @m38a_lib.M38A	80C5
1V5REG_PCIE_FB	1V5REG_PCIE_FB - @m38a_lib.M38A	80C5
1V5REG_PCIE_FB_R	1V5REG_PCIE_FB_R - @m38a_lib.M38A	80C3
1V5REG_PCIE_FS_DIS	1V5REG_PCIE_FS_DIS - @m38a_lib.M38A	80C7
1V5REG_PCIE_GND	1V5REG_PCIE_GND - @m38a_lib.M38A	80B7
1V5REG_PCIE_LDO_DR	1V5REG_PCIE_LDO_DR - @m38a_lib.M38A	80C7
1V5REG_PCIE_LDO_FB	1V5REG_PCIE_LDO_FB - @m38a_lib.M38A	80C7
1V5REG_PCIE_LGATE	1V5REG_PCIE_LGATE - @m38a_lib.M38A	80C6
1V5REG_PCIE_PVCC5	1V5REG_PCIE_PVCC5 - @m38a_lib.M38A	80D7
1V5REG_PCIE_SNUB	1V5REG_PCIE_SNUB - @m38a_lib.M38A	80C3
1V5REG_PCIE_SWITCHNODE	1V5REG_PCIE_SWITCHNODE - @m38a_lib.M38A	80C5
1V5REG_PCIE_UGATE	1V5REG_PCIE_UGATE - @m38a_lib.M38A	80D6
1V5REG_PCIE_VCC5	1V5REG_PCIE_VCC5 - @m38a_lib.M38A	80D7
1V8_REF	1V8_REF - @m38a_lib.M38A	79B3
1V8REG_DDR_BOOT	1V8REG_DDR_BOOT - @m38a_lib.M38A	79D6
1V8REG_DDR_BOOT_R	1V8REG_DDR_BOOT_R - @m38a_lib.M38A	79D5
1V8REG_DDR_COMP	1V8REG_DDR_COMP - @m38a_lib.M38A	79C6
1V8REG_DDR_COMP_R	1V8REG_DDR_COMP_R - @m38a_lib.M38A	79C5
1V8REG_DDR_FB	1V8REG_DDR_FB - @m38a_lib.M38A	79C5
1V8REG_DDR_FB_R	1V8REG_DDR_FB_R - @m38a_lib.M38A	79C3
1V8REG_DDR_FS_DIS	1V8REG_DDR_FS_DIS - @m38a_lib.M38A	79C7
1V8REG_DDR_GND	1V8REG_DDR_GND - @m38a_lib.M38A	79C7
1V8REG_DDR_LDO_DR	1V8REG_DDR_LDO_DR - @m38a_lib.M38A	79C7
1V8REG_DDR_LDO_FB	1V8REG_DDR_LDO_FB - @m38a_lib.M38A	79C7
1V8REG_DDR_LGATE	1V8REG_DDR_LGATE - @m38a_lib.M38A	79C6
1V8REG_DDR_PVCC5	1V8REG_DDR_PVCC5 - @m38a_lib.M38A	79D7
1V8REG_DDR_SNUB	1V8REG_DDR_SNUB - @m38a_lib.M38A	79C3
1V8REG_DDR_SWITCHNODE	1V8REG_DDR_SWITCHNODE - @m38a_lib.M38A	79C5
1V8REG_DDR_UGATE	1V8REG_DDR_UGATE - @m38a_lib.M38A	79D6
1V8REG_DDR_VCC5	1V8REG_DDR_VCC5 - @m38a_lib.M38A	79D7
1V8REG_GPU_BOOT	1V8REG_GPU_BOOT - @m38a_lib.M38A	78C6
1V8REG_GPU_BOOT_R	1V8REG_GPU_BOOT_R - @m38a_lib.M38A	78C5
1V8REG_GPU_COMP	1V8REG_GPU_COMP - @m38a_lib.M38A	78B6
1V8REG_GPU_COMP_R	1V8REG_GPU_COMP_R - @m38a_lib.M38A	78B5
1V8REG_GPU_FB	1V8REG_GPU_FB - @m38a_lib.M38A	78B5
1V8REG_GPU_FB_R	1V8REG_GPU_FB_R - @m38a_lib.M38A	78B3
1V8REG_GPU_FS_DIS	1V8REG_GPU_FS_DIS - @m38a_lib.M38A	78B7
1V8REG_GPU_GND	1V8REG_GPU_GND - @m38a_lib.M38A	78B7
1V8REG_GPU_LDO_DR	1V8REG_GPU_LDO_DR - @m38a_lib.M38A	78C7
1V8REG_GPU_LDO_FB	1V8REG_GPU_LDO_FB - @m38a_lib.M38A	78B7
1V8REG_GPU_LGATE	1V8REG_GPU_LGATE - @m38a_lib.M38A	78B6
1V8REG_GPU_PVCC5	1V8REG_GPU_PVCC5 - @m38a_lib.M38A	78C7
1V8REG_GPU_SNUB	1V8REG_GPU_SNUB - @m38a_lib.M38A	78B3
1V8REG_GPU_SWITCHNODE	1V8REG_GPU_SWITCHNODE - @m38a_lib.M38A	78B5
1V8REG_GPU_UGATE	1V8REG_GPU_UGATE - @m38a_lib.M38A	78C6
1V8REG_GPU_VCC5	1V8REG_GPU_VCC5 - @m38a_lib.M38A	78C7
2V5REG_ITH	2V5REG_ITH - @m38a_lib.M38A	77D2
2V5REG_ITH_RC	2V5REG_ITH_RC - @m38a_lib.M38A	77D2
2V5REG_MODE	2V5REG_MODE - @m38a_lib.M38A	77D3
2V5REG_RT	2V5REG_RT - @m38a_lib.M38A	77D3
2V5REG_SGND	2V5REG_SGND - @m38a_lib.M38A	77C2
2V5REG_SW	2V5REG_SW - @m38a_lib.M38A	77D2
2V5REG_VFB	2V5REG_VFB - @m38a_lib.M38A	77D2
5V_REG_IN	5V_REG_IN - @m38a_lib.M38A	68A4
=I2C_HD_TEMP_SCL	=I2C_HD_TEMP_SCL - @m38a_lib.M38A	59C1 66B6
	=I2C_ODD_TEMP_SCL - @m38a_lib.M38A	59C1 66B4
	=SMB_THRM_CLK - @m38a_lib.M38A	10C3 59C1
	SMB_B_S0_CLK - @m38a_lib.M38A	58B5 59C2 59D1
	SMB_GPU_NB_THRM_CLK - @m38a_lib.M38A	59C1 61C3
	SMB_B_S0_CLK - @m38a_lib.M38A	58B5 59C2 59D1
	=SMB_THRM_CLK - @m38a_lib.M38A	10C3 59C1
	=I2C_ODD_TEMP_SCL - @m38a_lib.M38A	59C1 66B4
=I2C_HD_TEMP_SDA	=I2C_HD_TEMP_SDA - @m38a_lib.M38A	59C1 66B6
	=I2C_ODD_TEMP_SDA - @m38a_lib.M38A	59C1 66B4
	=SMB_THRM_DATA - @m38a_lib.M38A	10C3 59C1
	SMB_B_S0_DATA - @m38a_lib.M38A	58B5 59C2 59D1
	SMB_GPU_NB_THRM_DATA - @m38a_lib.M38A	59C1 61C3
	SMB_B_S0_DATA - @m38a_lib.M38A	58B5 59C2 59D1
	=SMB_THRM_DATA - @m38a_lib.M38A	10C3 59C1
	=I2C_ODD_TEMP_SDA - @m38a_lib.M38A	59C1 66B4
=I2C_MEM_SCL	=I2C_MEM_SCL - @m38a_lib.M38A	27D6 28A6 29A6
	=SMB_AIRPORT_CLK - @m38a_lib.M38A	27D6 53B4
	SMB_CK410_CLK - @m38a_lib.M38A	27D6 33B6
	SMB_CLK - @m38a_lib.M38A	23D5 27B8 27D7
	SMB_CK410_CLK - @m38a_lib.M38A	27D6 33B6
	=SMB_AIRPORT_CLK - @m38a_lib.M38A	27D6 53B4
=I2C_MEM_SDA	=I2C_MEM_SDA - @m38a_lib.M38A	27D6 28A6 29A6

	=SMB_AIRPORT_DATA - @m38a_lib.M38A	27C6 53B4
	SMB_CK410_DATA - @m38a_lib.M38A	27D6 33B6
	SMB_DATA - @m38a_lib.M38A	23D5 27B8 27D7
	SMB_CK410_DATA - @m38a_lib.M38A	27D6 33B6
	=SMB_AIRPORT_DATA - @m38a_lib.M38A	27C6 53B4
=PP0V9_S0_MEMVTT_LDO	=PP0V9_S0_MEMVTT_LDO - @m38a_lib.M38A	6D4 31B3
	=PP0V9_S0_MEM_TERM - @m38a_lib.M38A	6D4 30D4
	PP0V9_S0 - @m38a_lib.M38A	6D6 79A3
	=PP0V9_S0_MEM_TERM - @m38a_lib.M38A	6D4 30D4
=PP1V2_S0_GPU_VDDPLL	=PP1V2_S0_GPU_VDDPLL - @m38a_lib.M38A	88C6 91B8
	=PPVIO_S0_PCIE - @m38a_lib.M38A	84A2 88C6
	=PP1V2_S0_REG - @m38a_lib.M38A	77A3 88C6
	=PP1V2_S0_PCIE_GPU_PVDD - @m38a_lib.M38A	84C8 88D6
	=PP1V2_S0_PCIE_GPU_VDDR - @m38a_lib.M38A	84C8 88D6
	PP1V2_GPU_IO_S0 - @m38a_lib.M38A	88D8
	=PPVIO_S0_PCIE - @m38a_lib.M38A	84A2 88C6
	=PP1V2_S0_REG - @m38a_lib.M38A	77A3 88C6
	=PP1V2_S0_PCIE_GPU_VDDR - @m38a_lib.M38A	84C8 88D6
	=PP1V2_S0_PCIE_GPU_PVDD - @m38a_lib.M38A	84C8 88D6
=PP1V2_S3_ENET	=PP1V2_S3_ENET - @m38a_lib.M38A	41A8 41D6 42B5
	PP1V2_S3_ENET - @m38a_lib.M38A	42B5
=PP1V2_S3_LAN	=PP1V2_S3_LAN - @m38a_lib.M38A	6D3 42B8
	PP1V2_S3 - @m38a_lib.M38A	6D4 77B3
=PP1V8_S0_FB_VDD	=PP1V8_S0_FB_VDD - @m38a_lib.M38A	88B6 89D5 89D8 90D5 90D8
	=PP1V8_S0_FB_VDDQ - @m38a_lib.M38A	88B6 89D5 89D8 90D5 90D8
	=PP1V8R2V0_S0_FB_GPU - @m38a_lib.M38A	86B8 87A5 87A8 87B5 87B8
	PP1V8_S0 - @m38a_lib.M38A	78B2 88B6
	=PP1V8R3V3_S0_GPU_VDDR5 - @m38a_lib.M38A	88B6 91B7
	=PP1V8R2V0_S0_GPU_VDDR4 - @m38a_lib.M38A	88B6 91B7
	PP1V8_S0 - @m38a_lib.M38A	78B2 88B6
	PP1V8R2V0_S0_FB_GPU - @m38a_lib.M38A	88B8
	=PP1V8_S0_FB_VDDQ - @m38a_lib.M38A	88B6 89D5 89D8 90D5 90D8
	=PP1V8R3V3_S0_GPU_VDDR5 - @m38a_lib.M38A	88B6 91B7
	=PP1V8R2V0_S0_GPU_VDDR4 - @m38a_lib.M38A	88B6 91B7
	=PP1V8R2V0_S0_FB_GPU - @m38a_lib.M38A	86B8 87A5 87A8 87B5 87B8
		88B6
=PP1V8_S3_MEM_NB	=PP1V8_S3_MEM_NB - @m38a_lib.M38A	6D3 6D3 14C2 16B6 19B8
		19D7
	=PP1V8_S0_MEMVTT - @m38a_lib.M38A	6D3 31C7
	PP1V8_S3 - @m38a_lib.M38A	5D2 6D4 79C2
	=PP1V8_S3_MEM - @m38a_lib.M38A	5C4 6D3 28B2 28C8 28D3 28D6 29B2 29D3 29D6
	PP1V8_S3 - @m38a_lib.M38A	5D2 6D4 79C2
	=PP1V8_S3_MEM - @m38a_lib.M38A	5C4 6D3 28B2 28C8 28D3 28D6 29B2 29D3 29D6
	=PP1V8_S0_MEMVTT - @m38a_lib.M38A	6D3 31C7
=PP2V5_S0_NB_VCCA_3GBG	=PP2V5_S0_NB_VCCA_3GBG - @m38a_lib.M38A	6B4 17D6 19A8 19C7
	=PP2V5_S0_GPU - @m38a_lib.M38A	88B6 93C8
	PP2V5_S0 - @m38a_lib.M38A	6B6 11B8 11C8 77D1 88C8
	=PP2V5_S0_GPU_VDD25 - @m38a_lib.M38A	88B6 91C6
	=PP2V5_S0_GPU_VDDC_CT - @m38a_lib.M38A	88B6 91C6
	=PP2V5_S0_GPU_PVDD - @m38a_lib.M38A	88B6 91A8
	=PP2V5_S0_GPU_VDDC_CT - @m38a_lib.M38A	88B6 91C6
	=PP2V5_S0_GPU_VDD25 - @m38a_lib.M38A	88B6 91C6
	=PP2V5_S0_GPU_PVDD - @m38a_lib.M38A	88B6 91A8
=PP2V5_S3_ENET	=PP2V5_S3_ENET - @m38a_lib.M38A	41D5 41D6 42C4
	PP2V5_S3_ENET - @m38a_lib.M38A	42C4 43D8
=PP3V3_S0_NB	=PP3V3_S0_NB - @m38a_lib.M38A	6A4 14C7 14D6 19C7 20A4 20B4 20B4
	=PP3V3_DDC_DVI - @m38a_lib.M38A	88C6 97D2
	=PP3V3_DDC_LCD - @m38a_lib.M38A	88C6 94A7 94C7
	=PP3V3_S0_FB_VDD - @m38a_lib.M38A	88C6 93B3
	PP3V3_S0 - @m38a_lib.M38A	6B6 6D8 10D2 11B8 26B7 26C6 41D8 59D3 61C3 76D6 88C8
	=PP3V3_S0_GPU - @m38a_lib.M38A	6A7 88C6 91D2 93A1 97A5 97B5
	=PP3V3_S0_GPU_VDDR3 - @m38a_lib.M38A	88C6 88D3 91C6
	=PP3V3_S0_LCD - @m38a_lib.M38A	88C6 94C8
	=PP3V3_S0_2V5REG - @m38a_lib.M38A	6A4 77D4
	=PP3V3_S0_AIRPORT - @m38a_lib.M38A	6A4 53C2
	=PP3V3_S0_PCI - @m38a_lib.M38A	6A4 44D5
	=PP3V3_S0_AUDIO - @m38a_lib.M38A	6A4 68A5 68D7 72A6 72C8 72D5 73B8 74B5 74C5 74D6
	=PP3V3_S0_IMVP - @m38a_lib.M38A	6A4 75D8
	=PP3V3_S0_CK410 - @m38a_lib.M38A	6A4 33C8 33D3 33D8 34D4
	=PPSPD_S0_MEM - @m38a_lib.M38A	6A4 28A7 29A3 29A7
	=PP3V3_S0_TPM - @m38a_lib.M38A	6A4 67C7 67D4
	=PP3V3_S0_SB_3V3_1V5_VCCHDA - @m38a_lib.M38A	6A4 24C3 25C4
	=PP3V3_S0_ODD_TSENS - @m38a_lib.M38A	6A4 66B4
	=PP3V3_S0_HD_TSENS - @m38a_lib.M38A	6B4 66B5
	=PP3V3_S0_FAN - @m38a_lib.M38A	6B4 59A8 59B7 65B7 65C7 66C7
	=PP3V3_S0_PATA - @m38a_lib.M38A	6B4 38D3
	=PP3V3_S0_SB_PM - @m38a_lib.M38A	6B4 26D4
	=PP3V3_S0_SB_PCI - @m38a_lib.M38A	6B4 26D1
	=PP3V3_S0_SB_VCC3_3_IDE - @m38a_lib.M38A	6B4 24C3 25B3
	=PP3V3_S0_SB_VCC3_3_PCI - @m38a_lib.M38A	6B4 24B3 25A3
	=PP3V3_S0_SB_VCC3_3 - @m38a_lib.M38A	6B4 24B5 24B5 25B8 25C6
	=PP3V3_S0_NB_VCC_HV - @m38a_lib.M38A	6B4 17C6 19A8 19C7
	=PP3V3_S0_SB_GPIO - @m38a_lib.M38A	6B4 21C3 21D3 23B3 23D5
	=PP3V3_S0_SB_VCCLAN3_3 - @m38a_lib.M38A	6A4 24D3 25D3
	=PP3V3_S0_SB - @m38a_lib.M38A	6B4 22B5 25D8 27C6
	PP3V3_S0 - @m38a_lib.M38A	6B6 6D8 10D2 11B8 26B7 26C6 41D8 59D3 61C3 76D6 88C8
	=PPSPD_S0_MEM - @m38a_lib.M38A	6A4 28A7 29A3 29A7

	=PP3V3_S0_TPM - @m38a_lib.M38A	6A4 67C7 67D4
	=PP3V3_S0_SB_VCCLAN3_3 - @m38a_lib.M38A	6A4 24D3 25D3
	=PP3V3_S0_SB_VCC3_3_PCI - @m38a_lib.M38A	6B4 24B3 25A3
	=PP3V3_S0_SB_VCC3_3_IDE - @m38a_lib.M38A	6B4 24C3 25B3
	=PP3V3_S0_SB_VCC3_3 - @m38a_lib.M38A	6B4 24B5 24B5 25B8 25C6
	=PP3V3_S0_SB_PM - @m38a_lib.M38A	6B4 26D4
	=PP3V3_S0_SB_PCI - @m38a_lib.M38A	6B4 26D1
	=PP3V3_S0_SB_3V3_1V5_VCCSUSHDA - @m38a_lib.M38A	6A4 24C3 25C4
	=PP3V3_S0_SB - @m38a_lib.M38A	6B4 22B5 25D8 27C6
	=PP3V3_S0_PCI - @m38a_lib.M38A	6A4 44D5
	=PP3V3_S0_PATA - @m38a_lib.M38A	6B4 38D3
	=PP3V3_S0_ODD_TSENS - @m38a_lib.M38A	6A4 66B4
	=PP3V3_S0_NB_VCC_HV - @m38a_lib.M38A	6B4 17C6 19A8 19C7
	=PP3V3_S0_NB_TVDAC - @m38a_lib.M38A	6B4 19C7
	=PP3V3_S0_NB_PM - @m38a_lib.M38A	6B4
	=PP3V3_S0_LCD - @m38a_lib.M38A	88C6 94C8
	=PP3V3_S0_IMVP - @m38a_lib.M38A	6A4 75D8
	=PP3V3_S0_HD_TSENS - @m38a_lib.M38A	6B4 66B5
	=PP3V3_S0_GPU_CLOCKS - @m38a_lib.M38A	88C6
	=PP3V3_S0_GPUBBP - @m38a_lib.M38A	88C6
	=PP3V3_S0_GPUBBN - @m38a_lib.M38A	88C6
	=PP3V3_S0_GPUBBCTL - @m38a_lib.M38A	88C6
	=PP3V3_S0_GPU - @m38a_lib.M38A	6A7 88C6 91D2 93A1 97A5 97B5
	=PP3V3_S0_FAN - @m38a_lib.M38A	6B4 59A8 59B7 65B7 65C7 66C7
	=PP3V3_S0_CK410 - @m38a_lib.M38A	6A4 33C8 33D3 33D8 34D4
	=PP3V3_S0_AUDIO - @m38a_lib.M38A	6A4 68A5 68D7 72A6 72C8 72D5 73B8 74B5 74C5 74D6
	=PP3V3_S0_AIRPORT - @m38a_lib.M38A	6A4 53C2
	=PP3V3_S0_2V5REG - @m38a_lib.M38A	6A4 77D4
	=PP3V3_GPU - @m38a_lib.M38A	88C6 94B3
	=PP3V3_DDC_LCD - @m38a_lib.M38A	88C6 94A7 94C7
	=PP3V3_DDC_DVI - @m38a_lib.M38A	88C6 97D2
=PP3V3_S3_1V2REG	=PP3V3_S3_1V2REG - @m38a_lib.M38A	6D3 77C7
	PP3V3_S3 - @m38a_lib.M38A	6A7 6D4 53C4 59C8 59D3 83B3
	=PP3V3_S3_BT - @m38a_lib.M38A	6D3 47B2
	=PP3V3_S3_TPM - @m38a_lib.M38A	6D3 67C2
	=PP3V3_S3_ENET - @m38a_lib.M38A	6D3 41A5 41B3 41C3 41D6 41D8 42D8
	PP3V3_S3 - @m38a_lib.M38A	6A7 6D4 53C4 59C8 59D3 83B3
	=PP3V3_S3_VGASYNC - @m38a_lib.M38A	6C3
	=PP3V3_S3_USB - @m38a_lib.M38A	6C3
	=PP3V3_S3_TPM - @m38a_lib.M38A	6D3 67C2
	=PP3V3_S3_ENET - @m38a_lib.M38A	6D3 41A5 41B3 41C3 41D6 41D8 42D8
	=PP3V3_S3_BT - @m38a_lib.M38A	6D3 47B2
=PP3V3_S5_DEBUG	=PP3V3_S5_DEBUG - @m38a_lib.M38A	6D1 60D4
	=PP3V3_S5_ROM - @m38a_lib.M38A	6D1 63D4
	PP3V3_S5 - @m38a_lib.M38A	5D2 6A8 6C8 6D2 6D8 6D8 11D8 26C1 26C4 26C4 59A8 65B7 65D7 66D7 76D2 77C8 77D5 77D6 77D6 77D8 79A3 79A5 79B3 80A5 80B3 81A5 81A5 83C3
	=PP3V3_S5_SMC - @m38a_lib.M38A	6D1 58C2 58D3 58D4 59A4 59A5 59C4 59D3 59D8
	=PP3V3_S5_FW - @m38a_lib.M38A	6D1 44A6 44B2 44D5 44D7 45D6 46A8
	=PP3V3_S5_SB_IO - @m38a_lib.M38A	6D1 22C6 27C6
	=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA - @m38a_lib.M38A	6D1 24C3
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m38a_lib.M38A	6D1 24B3 25D1
	=PP3V3_S5_SB_VCCSUS3_3 - @m38a_lib.M38A	6D1 24A5 24B3 25B6 25D1
	=PP3V3_S5_SB_PM - @m38a_lib.M38A	6D1 11B5 23D1
	=PP3V3_S5_SB_USB - @m38a_lib.M38A	6D1 22D8
	=PP3V3_S5_SB - @m38a_lib.M38A	6D1 23A7 23B3 23B7 23D4 23D8 25C8 26D8
	PP3V3_S5 - @m38a_lib.M38A	5D2 6A8 6C8 6D2 6D8 6D8 11D8 26C1 26C4 26C4 59A8 65B7 65D7 66D7 76D2 77C8 77D5 77D6 77D6 77D8 79A3 79A5 79B3 80A5 80B3 81A5 81A5 83C3
	=PP3V3_S5_SMC - @m38a_lib.M38A	6D1 58C2 58D3 58D4 59A4 59A5 59C4 59D3 59D8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m38a_lib.M38A	6D1 24B3 25D1
	=PP3V3_S5_SB_VCCSUS3_3 - @m38a_lib.M38A	6D1 24A5 24B3 25B6 25D1
	=PP3V3_S5_SB_USB - @m38a_lib.M38A	6D1 22D8
	=PP3V3_S5_SB_PM - @m38a_lib.M38A	6D1 11B5 23D1
	=PP3V3_S5_SB_IO - @m38a_lib.M38A	6D1 22C6 27C6
	=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA - @m38a_lib.M38A	6D1 24C3
	=PP3V3_S5_SB - @m38a_lib.M38A	6D1 23A7 23B3 23B7 23D4 23D8 25C8 26D8
	=PP3V3_S5_ROM - @m38a_lib.M38A	6D1 63D4
	=PP3V3_S5_FW - @m38a_lib.M38A	6D1 44A6 44B2 44D5 44D7 45D6 46A8
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO - @m38a_lib.M38A	6A4 68A5
	PP5V_S0_AUDIO - @m38a_lib.M38A	6A5
=PP5V_S0_DEBUG	=PP5V_S0_DEBUG - @m38a_lib.M38A	6A4 60D4
	=PP5V_S0_DVI_DDC - @m38a_lib.M38A	88A6 97D6
	=PP5V_S0_GPUISENS - @m38a_lib.M38A	85D2 88A6
	PP5V_S0 - @m38a_lib.M38A	6A6 6D8 75D7 88B8 97D3
	=PP5V_S0_SB - @m38a_lib.M38A	6A4 25D8
	=PP5V_S0_PATA - @m38a_lib.M38A	6A4 38C4 38D3
	P5V_S0 - @m38a_lib.M38A	6A6 6D8 75D7 88B8 97D3
	=PP5V_S0_SB - @m38a_lib.M38A	6A4 25D8
	=PP5V_S0_PATA - @m38a_lib.M38A	6A4 38C4 38D3
	=PP5V_S0_GPUISENS - @m38a_lib.M38A	85D2 88A6
	=PP5V_S0_GPUBBCTL - @m38a_lib.M38A	88B6
	=PP5V_S0_DVI_DDC - @m38a_lib.M38A	88A6 97D6
=PP5V_S0_GPUVCORE	=PP5V_S0_GPUVCORE - @m38a_lib.M38A	85D7 88D6
	GPUVCORE_VCC - @m38a_lib.M38A	88D6
=PP5V_S0_MEMVTT	=PP5V_S0_MEMVTT - @m38a_lib.M38A	6C3 31C6
	P5V_S3 - @m38a_lib.M38A	6C4 60B6 83C3
	=PP5V_S3_BNDI - @m38a_lib.M38A	6C3 47D3
	=PP5V_S3_USB - @m38a_lib.M38A	6C3 47C8
	P5V_S3 - @m38a_lib.M38A	6C4 60B6 83C3

	=PP5V_S3_USB - @m38a_lib.M38A	6C3 47C8
	=PP5V_S3_BNDI - @m38a_lib.M38A	6C3 47D3
=PP5V_S5_SB	=PP5V_S5_SB - @m38a_lib.M38A	6D1 25C8
	PP5V_S5 - @m38a_lib.M38A	5D2 6D2 6D7 59A5 79B3 79B3 80B3 81B3 83C3
=PP12V_GPU	=PP12V_GPU - @m38a_lib.M38A	88B6 94C3 94D7
	PP12V_S0 - @m38a_lib.M38A	6A6 6D8 88B8
	=PP12V_S0_FAN - @m38a_lib.M38A	6A4 65B6 65D7 66D6
	PP12V_S0 - @m38a_lib.M38A	6A6 6D8 88B8
	=PP12V_S0_FAN - @m38a_lib.M38A	6A4 65B6 65D7 66D6
=PP12V_S0_AUDIO_SPKR AMP	=PP12V_S0_AUDIO_SPKRAMP - @m38a_lib.M38A	6A4 72D8
	PP12V_S0_AUDIO_SPKRAMP - @m38a_lib.M38A	6A5
=PP12V_S5_CPU	=PP12V_S5_CPU - @m38a_lib.M38A	6C1 76D8
	=PPVIN_S0_GPUVCORE - @m38a_lib.M38A	85D7 88B6
	PP12V_S5 - @m38a_lib.M38A	5D2 6C2 6D7 11A8 11C7 11D7 77C8 77D8 78C7 79D7 80D7 81D7 83C5 83C5 88B8
	=PP12V_S5_FW - @m38a_lib.M38A	6C1 46D7
	PP12V_S5 - @m38a_lib.M38A	5D2 6C2 6D7 11A8 11C7 11D7 77C8 77D8 78C7 79D7 80D7 81D7 83C5 83C5 88B8
	=PPVIN_S0_GPUVCORE - @m38a_lib.M38A	85D7 88B6
	=PP12V_S5_FW - @m38a_lib.M38A	6C1 46D7
=PP12V_S5_FW_PHY	=PP12V_S5_FW_PHY - @m38a_lib.M38A	44C2 46D5
	PP12V_FW - @m38a_lib.M38A	46D6
=PPBB_S0_GPU	=PPBB_S0_GPU - @m38a_lib.M38A	86D6 88C6
	=PPVCORE_S0_GPU - @m38a_lib.M38A	86D8 88D6 91A7
	PP1V0R1V2_S0_GPU - @m38a_lib.M38A	59B4 88D8
	=PPVCORE_S0_GPU_REG - @m38a_lib.M38A	85C1 88D6
	PPBB_S0_GPU - @m38a_lib.M38A	88C8
	PP1V0R1V2_S0_GPU - @m38a_lib.M38A	59B4 88D8
	=PPVOUT_S0_GPUBBP_LDO - @m38a_lib.M38A	85A6 88C6
	=PPVCORE_S0_GPU_REG - @m38a_lib.M38A	85C1 88D6
	=PPVCORE_S0_GPU_BBP - @m38a_lib.M38A	85A8 88D6
	=PPVCORE_S0_GPU - @m38a_lib.M38A	86D8 88D6 91A7
=PPVCORE_S0_CPU	=PPVCORE_S0_CPU - @m38a_lib.M38A	6D4 8B6 8D7 8D8 9B8
	PPVCORE_CPU - @m38a_lib.M38A	5D2 6D6 75A4 75D1 76B3
ACZ_BITCLK	ACZ_BITCLK - @m38a_lib.M38A	21C7 68D7
ACZ_RST_L	ACZ_RST_L - @m38a_lib.M38A	21C7 68C7
ACZ_SDATAIN<0>	ACZ_SDATAIN<0> - @m38a_lib.M38A	21C7 68D7
ACZ_SDATAIN_CHIP	ACZ_SDATAIN_CHIP - @m38a_lib.M38A	68C6
ACZ_SDATAOUT	ACZ_SDATAOUT - @m38a_lib.M38A	21C7 68D7
ACZ_SYNC	ACZ_SYNC - @m38a_lib.M38A	21C7 68D7
AIRPORT_CLK100M_PCIE_N	AIRPORT_CLK100M_PCIE_N - @m38a_lib.M38A	34B4 34C2 53C6
AIRPORT_CLK100M_PCIE_P	AIRPORT_CLK100M_PCIE_P - @m38a_lib.M38A	34B4 34C2 53C6
AIRPORT_CONN_CLK	AIRPORT_CONN_CLK - @m38a_lib.M38A	53B5
AIRPORT_CONN_DATA	AIRPORT_CONN_DATA - @m38a_lib.M38A	53B5
AIRPORT_RST_L	AIRPORT

AUD_GPIO_1	AUD_GPIO_1 - @m38a_lib.M38A	68C7 74C5
AUD_GPIO_2	AUD_GPIO_2 - @m38a_lib.M38A	68B7 68C7
AUD_LI_DET_EMI	AUD_LI_DET_EMI - @m38a_lib.M38A	73D6
AUD_LI_DET_H	AUD_LI_DET_H - @m38a_lib.M38A	73D4 74D6
AUD_LI_DET_JACK	AUD_LI_DET_JACK - @m38a_lib.M38A	73D7
AUD_LI_GND_EMI	AUD_LI_GND_EMI - @m38a_lib.M38A	73D6
AUD_LI_GND_JACK	AUD_LI_GND_JACK - @m38a_lib.M38A	73D7
AUD_LI_L	AUD_LI_L - @m38a_lib.M38A	73D4 74C5
AUD_LI_L_EMI	AUD_LI_L_EMI - @m38a_lib.M38A	73D6
AUD_LI_L_JACK	AUD_LI_L_JACK - @m38a_lib.M38A	73D7
AUD_LI_R	AUD_LI_R - @m38a_lib.M38A	73D4 74C5
AUD_LI_R_EMI	AUD_LI_R_EMI - @m38a_lib.M38A	73D6
AUD_LI_R_JACK	AUD_LI_R_JACK - @m38a_lib.M38A	73D7
AUD_LO_DET1_1	AUD_LO_DET1_1 - @m38a_lib.M38A	74A4 74B2
AUD_LO_DET1_INV	AUD_LO_DET1_INV - @m38a_lib.M38A	74B3
AUD_LO_DET2_1	AUD_LO_DET2_1 - @m38a_lib.M38A	74B4
AUD_LO_GND_JACK	AUD_LO_GND_JACK - @m38a_lib.M38A	73B4
AUD_LO_L	AUD_LO_L - @m38a_lib.M38A	73B8 74B5
AUD_LO_L_EMI	AUD_LO_L_EMI - @m38a_lib.M38A	73B7
AUD_LO_L_JACK	AUD_LO_L_JACK - @m38a_lib.M38A	73B4
AUD_LO_R	AUD_LO_R - @m38a_lib.M38A	73A8 74B5
AUD_LO_R_EMI	AUD_LO_R_EMI - @m38a_lib.M38A	73A7
AUD_LO_R_JACK	AUD_LO_R_JACK - @m38a_lib.M38A	73B4
AUD_LO_TIP	AUD_LO_TIP - @m38a_lib.M38A	73B8 74B5
AUD_LO_TIP_EMI	AUD_LO_TIP_EMI - @m38a_lib.M38A	73B7
AUD_LO_TIP_JACK	AUD_LO_TIP_JACK - @m38a_lib.M38A	73B4
AUD_LO_TYPE	AUD_LO_TYPE - @m38a_lib.M38A	73B8 74A5
AUD_LO_TYPE_EMI	AUD_LO_TYPE_EMI - @m38a_lib.M38A	73B7
AUD_LO_TYPE_JACK	AUD_LO_TYPE_JACK - @m38a_lib.M38A	73B4
AUD_MAX9714_CHOLD	AUD_MAX9714_CHOLD - @m38a_lib.M38A	72C4
AUD_MAX9714_VREG	AUD_MAX9714_VREG - @m38a_lib.M38A	72C5
AUD_MIC_INTERCON	AUD_MIC_INTERCON - @m38a_lib.M38A	74A4
AUD_MIC_IN_N	AUD_MIC_IN_N - @m38a_lib.M38A	73C4 74A6
AUD_MIC_IN_N_CONN	AUD_MIC_IN_N_CONN - @m38a_lib.M38A	47C2 73C2
AUD_MIC_IN_N_EMI	AUD_MIC_IN_N_EMI - @m38a_lib.M38A	73C3
AUD_MIC_IN_P	AUD_MIC_IN_P - @m38a_lib.M38A	73C4 74A6
AUD_MIC_IN_P_CONN	AUD_MIC_IN_P_CONN - @m38a_lib.M38A	47C2 73C2
AUD_MIC_IN_P_EMI	AUD_MIC_IN_P_EMI - @m38a_lib.M38A	73C3
AUD_MIC_P1	AUD_MIC_P1 - @m38a_lib.M38A	74A4
AUD_NC_40	AUD_NC_40 - @m38a_lib.M38A	68C4
AUD_NC_43	AUD_NC_43 - @m38a_lib.M38A	68B4
AUD_PORT_A_DET_L	AUD_PORT_A_DET_L - @m38a_lib.M38A	74B2
AUD_PORT_A_L1	AUD_PORT_A_L1 - @m38a_lib.M38A	74B7 74C4 74D4
AUD_PORT_A_L2	AUD_PORT_A_L2 - @m38a_lib.M38A	74B7 74C3 74D3
AUD_PORT_A_R1	AUD_PORT_A_R1 - @m38a_lib.M38A	74B7 74C4 74D4
AUD_PORT_A_R2	AUD_PORT_A_R2 - @m38a_lib.M38A	74B7 74C3 74D3
AUD_PORT_E_DET_L	AUD_PORT_E_DET_L - @m38a_lib.M38A	74B1
AUD_PORT_F_DET_L	AUD_PORT_F_DET_L - @m38a_lib.M38A	74D4
AUD_PORT_F_L1	AUD_PORT_F_L1 - @m38a_lib.M38A	74C7
AUD_PORT_F_R1	AUD_PORT_F_R1 - @m38a_lib.M38A	74C7
AUD_SAMP_FS1	AUD_SAMP_FS1 - @m38a_lib.M38A	72A6 72C5
AUD_SAMP_FS2	AUD_SAMP_FS2 - @m38a_lib.M38A	72A6 72C5
AUD_SAMP_G1	AUD_SAMP_G1 - @m38a_lib.M38A	72A6 72C5
AUD_SAMP_G2	AUD_SAMP_G2 - @m38a_lib.M38A	72A6 72C5
AUD_SAMP_INL_N	AUD_SAMP_INL_N - @m38a_lib.M38A	72C5
AUD_SAMP_INL_P	AUD_SAMP_INL_P - @m38a_lib.M38A	72C5
AUD_SAMP_INR_N	AUD_SAMP_INR_N - @m38a_lib.M38A	72C5
AUD_SAMP_INR_P	AUD_SAMP_INR_P - @m38a_lib.M38A	72C5
AUD_SAMP_SHDN_L	AUD_SAMP_SHDN_L - @m38a_lib.M38A	72C5
AUD_SENSE_A	AUD_SENSE_A - @m38a_lib.M38A	68C1 74C5 74D7
AUD_SENSE_B	AUD_SENSE_B - @m38a_lib.M38A	68C1 74C5 74D6 74D7
AUD_SPDIFIN_JACK	AUD_SPDIFIN_JACK - @m38a_lib.M38A	73D7
AUD_SPDIF_GND_IN	AUD_SPDIF_GND_IN - @m38a_lib.M38A	73C7
AUD_SPDIF_GND_OUT	AUD_SPDIF_GND_OUT - @m38a_lib.M38A	73A3
AUD_SPDIF_IN	AUD_SPDIF_IN - @m38a_lib.M38A	68C1 73D4
AUD_SPDIF_OUT	AUD_SPDIF_OUT - @m38a_lib.M38A	68D1 73B8
AUD_SPDIF_OUT_CHIP	AUD_SPDIF_OUT_CHIP - @m38a_lib.M38A	68D4
AUD_SPKR_OUTL_N	AUD_SPKR_OUTL_N - @m38a_lib.M38A	72C1 73D2
AUD_SPKR_OUTL_P	AUD_SPKR_OUTL_P - @m38a_lib.M38A	72C1 73D2
AUD_SPKR_OUTR_N	AUD_SPKR_OUTR_N - @m38a_lib.M38A	72C1 73D2
AUD_SPKR_OUTR_P	AUD_SPKR_OUTR_P - @m38a_lib.M38A	72C1 73D2
AUD_TYPE_DET_EN	AUD_TYPE_DET_EN - @m38a_lib.M38A	74B3
AUD_VREF_FILT	AUD_VREF_FILT - @m38a_lib.M38A	68C4
AUD_VREF_PORT_B	AUD_VREF_PORT_B - @m38a_lib.M38A	68C1 74A2
BAL_IN_COM	BAL_IN_COM - @m38a_lib.M38A	68C7 74A7
BAL_IN_L	BAL_IN_L - @m38a_lib.M38A	68C7 74A7
BAL_IN_R	BAL_IN_R - @m38a_lib.M38A	68C7 74A7
BAT_1	BAT_1 - @m38a_lib.M38A	26C8
BAT_2	BAT_2 - @m38a_lib.M38A	26C8
BEEP	BEEP - @m38a_lib.M38A	68C6
BIOS_REC	BIOS_REC - @m38a_lib.M38A	23A6 23C5
BOOT_LPC_SPI_L	BOOT_LPC_SPI_L - @m38a_lib.M38A	22B3 58C7 60C4
C8509_P1	C8509_P1 - @m38a_lib.M38A	85C5
CK410_27M_NONSPREAD	CK410_27M_NONSPREAD - @m38a_lib.M38A	34A4 92C7
CK410_27M_SPREAD	CK410_27M_SPREAD - @m38a_lib.M38A	34A4 92C5
CK410_CLK14P3M_TIMER	GPU_GPIO_16 - @m38a_lib.M38A	91C3 92C3
	CK410_CLK14P3M_TIMER - @m38a_lib.M38A	33A4 34D6
CK410_CPU0_N	CK410_CPU0_N - @m38a_lib.M38A	33C4 34B6
CK410_CPU0_P	CK410_CPU0_P - @m38a_lib.M38A	33C4 34B6
CK410_CPU1_N	CK410_CPU1_N - @m38a_lib.M38A	33C4 34B6
CK410_CPU1_P	CK410_CPU1_P - @m38a_lib.M38A	33C4 34B6
CK410_CPU2_ITP_SRC10_N	CK410_CPU2_ITP_SRC10_N - @m38a_lib.M38A	33C4 34B6
CK410_CPU2_ITP_SRC10_P	CK410_CPU2_ITP_SRC10_P - @m38a_lib.M38A	33C4 34B6
CK410_DOT96_27M_NONSPREAD_P	CK410_DOT96_27M_NONSPREAD_P - @m38a_lib.M38A	33A4 34A6
CK410_DOT96_27M_SPREAD_N	CK410_DOT96_27M_SPREAD_N - @m38a_lib.M38A	33A4 34A6
CK410_FSA	CK410_FSA - @m38a_lib.M38A	34B8 34C4
CK410_FSB_TEST_MODE	CK410_FSB_TEST_MODE - @m38a_lib.M38A	33C6 34A8
CK410_FSC	CK410_FSC - @m38a_lib.M38A	34A8 34D4
CK410_IREF	CK410_IREF - @m38a_lib.M38A	33B6
CK410_LVDS_N	CK410_LVDS_N - @m38a_lib.M38A TP_CK410_LVDS_N - @m38a_lib.M38A	33B4 34A6 34A4
CK410_LVDS_P	CK410_LVDS_P - @m38a_lib.M38A TP_CK410_LVDS_P - @m38a_lib.M38A	33B4 34A6 34A4
CK410_PCI1_CLK	CK410_PCI1_CLK - @m38a_lib.M38A	33B6 34C6
CK410_PCI2_CLK	CK410_PCI2_CLK - @m38a_lib.M38A	33B6 34C6
CK410_PCI3_CLK	CK410_PCI3_CLK - @m38a_lib.M38A	33B6 34C6
CK410_PCI4_CLK	CK410_PCI4_CLK - @m38a_lib.M38A	33B6 34C6
CK410_PCI5_FCTSEL1	CK410_PCI5_FCTSEL1 - @m38a_lib.M38A	33B6 34D6
CK410_PCIF0_CLK	CK410_PCIF0_CLK - @m38a_lib.M38A	33B8 34B6
CK410_PCIF1_ITP_EN	CK410_PCIF1_ITP_EN - @m38a_lib.M38A	33B8 34B6
CK410_PD_VTT_PWRGD_L	CK410_PD_VTT_PWRGD_L - @m38a_lib.M38A VR_PWRGD_CK410_L - @m38a_lib.M38A	26A8 33A4 26A7 75C6
CK410_REF1_FCTSEL0	CK410_REF1_FCTSEL0 - @m38a_lib.M38A	33A4 34C6
CK410_SRC1_N	CK410_SRC1_N - @m38a_lib.M38A	33B4 34A6
CK410_SRC1_P	CK410_SRC1_P - @m38a_lib.M38A	33B4 34A6
CK410_SRC2_N	CK410_SRC2_N - @m38a_lib.M38A	33B4 34A6
CK410_SRC2_P	CK410_SRC2_P - @m38a_lib.M38A	33B4 34A6
CK410_SRC3_N	CK410_SRC3_N - @m38a_lib.M38A	33B4 34D3
CK410_SRC3_P	CK410_SRC3_P - @m38a_lib.M38A	33B4 34D3
CK410_SRC4_N	CK410_SRC4_N - @m38a_lib.M38A	33B4 34B6
CK410_SRC4_P	CK410_SRC4_P - @m38a_lib.M38A	33B4 34B6
CK410_SRC5_N	CK410_SRC5_N - @m38a_lib.M38A	33B4 34B6
CK410_SRC5_P	CK410_SRC5_P - @m38a_lib.M38A	33B4 34B6
CK410_SRC6_N	CK410_SRC6_N - @m38a_lib.M38A	33B4 34B6
CK410_SRC6_P	CK410_SRC6_P - @m38a_lib.M38A	33B4 34B6
CK410_SRC7_N	CK410_SRC7_N - @m38a_lib.M38A	33B4 34D3
CK410_SRC7_P	CK410_SRC7_P - @m38a_lib.M38A	33B4 34D3
CK410_SRC8_N	CK410_SRC8_N - @m38a_lib.M38A	33A4 34A6
CK410_SRC8_P	CK410_SRC8_P - @m38a_lib.M38A	33A4 34A6
CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L - @m38a_lib.M38A	33B4 34D8
CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L - @m38a_lib.M38A	33B4 34D8
CK410_SRC_CLKREQ6_L	CK410_SRC_CLKREQ6_L - @m38a_lib.M38A	33B4 53C6
CK410_SRC_CLKREQ8_L	CK410_SRC_CLKREQ8_L - @m38a_lib.M38A	33A4 34D8
CK410_USB48_FSA	CK410_USB48_FSA - @m38a_lib.M38A	33A4 34C6
CK410_XTAL_IN	CK410_XTAL_IN - @m38a_lib.M38A	33C6
CK410_XTAL_OUT	CK410_XTAL_OUT - @m38a_lib.M38A	33C6
CLK_NB_OE_L	CLK_NB_OE_L - @m38a_lib.M38A	14B6 33B4
CPU_A20M_L	CPU_A20M_L - @m38a_lib.M38A	5C8 7C7 21C4
CPU_BSEL<0>	CPU_BSEL<0> - @m38a_lib.M38A	7B4 34B8
CPU_BSEL<1>	CPU_BSEL<1> - @m38a_lib.M38A	7B4 34A8
CPU_BSEL<2>	CPU_BSEL<2> - @m38a_lib.M38A	7B4 34A8
CPU_COMP<0>	CPU_COMP<0> - @m38a_lib.M38A	7B2
CPU_COMP<1>	CPU_COMP<1> - @m38a_lib.M38A	7B2
CPU_COMP<2>	CPU_COMP<2> - @m38a_lib.M38A	7B2
CPU_COMP<3>	CPU_COMP<3> - @m38a_lib.M38A	7B2
CPU_DCIN_SENSE	CPU_DCIN_SENSE - @m38a_lib.M38A	76D7
CPU_DCIN_SENSE_R	CPU_DCIN_SENSE_R - @m38a_lib.M38A	76C7
CPU_DPRSTP_L	CPU_DPRSTP_L - @m38a_lib.M38A	7B3 21C4 75C6
CPU_DPSLP_L	CPU_DPSLP_L - @m38a_lib.M38A	7B3 21C4
CPU_FERR_L	CPU_FERR_L - @m38a_lib.M38A	7C7 21C2
CPU_GTLREF	CPU_GTLREF - @m38a_lib.M38A	5D4 7B4
CPU_HS_ZH607	CPU_HS_ZH607 - @m38a_lib.M38A	9D4
CPU_HS_ZH608	CPU_HS_ZH608 - @m38a_lib.M38A	9D3 66A4 66A6 66B4 66B6
CPU_HS_ZH609	CPU_HS_ZH609 - @m38a_lib.M38A	9D3
CPU_HS_ZH610	CPU_HS_ZH610 - @m38a_lib.M38A	9D2
CPU_IGNNE_L	CPU_IGNNE_L - @m38a_lib.M38A	5C8 7C7 21C4
CPU_INIT_L	CPU_INIT_L - @m38a_lib.M38A	5C8 7D6 21C4
CPU_INTR	CPU_INTR - @m38a_lib.M38A	5C8 7C7 21C4
CPU_NMI	CPU_NMI - @m38a_lib.M38A	5C8 7C7 21C4
CPU_PROCHOT_L	CPU_PROCHOT_L - @m38a_lib.M38A	7C6 59A8 59C7
CPU_PSI_L	CPU_PSI_L - @m38a_lib.M38A	7A3 75C6
CPU_PWRGD	CPU_PWRGD - @m38a_lib.M38A	7B3 21C4
CPU_RCIN_L	CPU_RCIN_L - @m38a_lib.M38A	21C4
CPU_SENSE_I_R	CPU_SENSE_I_R - @m38a_lib.M38A	76D7
CPU_SMI_L	CPU_SMI_L - @m38a_lib.M38A	5C8 7C7 21C4
CPU_STPCLK_L	CPU_STPCLK_L - @m38a_lib.M38A	5C8 7C7 21C4
CPU_TEST1	CPU_TEST1 - @m38a_lib.M38A	7B4
CPU_TEST2	CPU_TEST2 - @m38a_lib.M38A	7B4
CPU_THERMD_EXT_N	CPU_THERMD_EXT_N - @m38a_lib.M38A	10B6
CPU_THERMD_EXT_P	CPU_THERMD_EXT_P - @m38a_lib.M38A	10B6
CPU_THERMD_N	CPU_THERMD_N - @m38a_lib.M38A	7C6 10C6
CPU_THERMD_P	CPU_THERMD_P - @m38a_lib.M38A	7C6 10C6
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @m38a_lib.M38A	21C2
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @m38a_lib.M38A	8B6 75A4
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @m38a_lib.M38A	8B6 75A4
CPU_VID<0>	CPU_VID<0> - @m38a_lib.M38A	8B7 75C7
CPU_VID<1>	CPU_VID<1> - @m38a_lib.M38A	8B7 75C7
CPU_VID<2>	CPU_VID<2> - @m38a_lib.M38A	8B7 75C7
CPU_VID<3>	CPU_VID<3> - @m38a_lib.M38A	8B7 75C7
CPU_VID<4>	CPU_VID<4> - @m38a_lib.M38A	8B7 75C7
CPU_VID<5>	CPU_VID<5> - @m38a_lib.M38A	8B7 75C7
CPU_VID<6>	CPU_VID<6> - @m38a_lib.M38A	8B7 75D7
CPU_XDP_CLK_N	CPU_XDP_CLK_N - @m38a_lib.M38A FSB_CLK_XDP_N - @m38a_lib.M38A	11B3 34B3 34B4 34C2
CPU_XDP_CLK_P	CPU_XDP_CLK_P - @m38a_lib.M38A FSB_CLK_XDP_P - @m38a_lib.M38A	11B3 34B3 34B4 34C2
CRB_SV_DET	CRB_SV_DET - @m38a_lib.M38A	23B6 23C3
CRT_BLUE	CRT_BLUE - @m38a_lib.M38A =PPVCORE_S0_NB - @m38a_lib.M38A CRT_BLUE_L - @m38a_lib.M38A CRT_IREF - @m38a_lib.M38A CRT_GREEN_L - @m38a_lib.M38A CRT_GREEN - @m38a_lib.M38A PP2V5_S0_NB_VCCA_CRTDAC - @m38a_lib.M38A CRT_RED - @m38a_lib.M38A CRT_RED_L - @m38a_lib.M38A PP1V05_S0 - @m38a_lib.M38A =PP1V05_S0_CPU - @m38a_lib.M38A =PPVCORE_S0_SB - @m38a_lib.M38A =PP1V05_S0_SB_CPU_IO - @m38a_lib.M38A =PP1V05_S0_NB_VTT - @m38a_lib.M38A =PP1V05_S0_FSB_NB - @m38a_lib.M38A PP2V5_S0_NB_VCCA_CRTDAC - @m38a_lib.M38A PP1V05_S0 - @m38a_lib.M38A CRT_RED_L - @m38a_lib.M38A CRT_RED - @m38a_lib.M38A CRT_IREF - @m38a_lib.M38A CRT_GREEN_L - @m38a_lib.M38A CRT_GREEN - @m38a_lib.M38A CRT_BLUE_L - @m38a_lib.M38A =PPVCORE_S0_SB - @m38a_lib.M38A =PPVCORE_S0_NB - @m38a_lib.M38A =PP1V05_S0_SB_CPU_IO - @m38a_lib.M38A =PP1V05_S0_NB_VTT - @m38a_lib.M38A =PP1V05_S0_NB - @m38a_lib.M38A =PP1V05_S0_FSB_NB - @m38a_lib.M38A =PP1V05_S0_CPU - @m38a_lib.M38A	13B5 19D4 19D7 13B5 19D4 13B5 19D4 13B5 19D4 13B5 19D4 17D6 19D4 13B5 19D4 13B5 19D4 6D6 34A8 34B8 34C7 81C2 5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 11B3 11C5 6D4 24D3 25D3 6D4 21C1 21C1 24C3 25C3 6D4 17D3 19B8 19D7 5D4 6D4 12A7 12B7 12C2 19D7 17D6 19D4 6D6 34A8 34B8 34C7 81C2 13B5 19D4 13B5 19D4 13B5 19D4 13B5 19D4 13B5 19D4 6D4 24D3 25D3 6D4 16C8 16D3 19B6 19D5 19D7 6D4 21C1 21C1 24C3 25C3 6D4 17D3 19B8 19D7 6D4 19D7 5D4 6D4 12A7 12B7 12C2 19D7 5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 9C8 11B3 11C5
CRT_DDC_CLK	CRT_DDC_CLK - @m38a_lib.M38A TP_CRT_DDC_CLK - @m38a_lib.M38A	13B5 19C4 19C5
CRT_DDC_DATA	CRT_DDC_DATA - @m38a_lib.M38A TP_CRT_DDC_DATA - @m38a_lib.M38A	13B5 19C4 19C5
DEBUG_RST_L	DEBUG_RST_L - @m38a_lib.M38A	6B7 60C4
DMI_IRCOMP_R	DMI_IRCOMP_R - @m38a_lib.M38A	22C2
DMI_N2S_N<0>	DMI_N2S_N<0> - @m38a_lib.M38A	5B8 14B4 22D2
DMI_N2S_N<1>	DMI_N2S_N<1> - @m38a_lib.M38A	14B4 22D2
DMI_N2S_N<2>	DMI_N2S_N<2> - @m38a_lib.M38A	14B4 22D2
DMI_N2S_N<3>	DMI_N2S_N<3> - @m38a_lib.M38A	14B4 22D2
DMI_N2S_P<0>	DMI_N2S_P<0> - @m38a_lib.M38A	5B8 14B4 22D2
DMI_N2S_P<1>	DMI_N2S_P<1> - @m38a_lib.M38A	14B4 22D2
DMI_N2S_P<2>	DMI_N2S_P<2> - @m38a_lib.M38A	14B4 22D2
DMI_N2S_P<3>	DMI_N2S_P<3> - @m38a_lib.M38A	14B4 22D2
DMI_S2N_N<0>	DMI_S2N_N<0> - @m38a_lib.M38A	5C7 14B4 22D2
DMI_S2N_N<1>	DMI_S2N_N<1> - @m38a_lib.M38A	14B4 22D2
DMI_S2N_N<2>	DMI_S2N_N<2> - @m38a_lib.M38A	14B4 22D2
DMI_S2N_N<3>	DMI_S2N_N<3> - @m38a_lib.M38A	14B4 22D2
DMI_S2N_P<0>	DMI_S2N_P<0> - @m38a_lib.M38A	5C7 14B4 22D2
DMI_S2N_P<1>	DMI_S2N_P<1> - @m38a_lib.M38A	14B4 22D2
DMI_S2N_P<2>	DMI_S2N_P<2> - @m38a_lib.M38A	14B4 22D2
DMI_S2N_P<3>	DMI_S2N_P<3> - @m38a_lib.M38A	14B4 22D2
DVI_DDC_CLK	DVI_DDC_CLK - @m38a_lib.M38A	97D2
DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @m38a_lib.M38A	97D3 97D5
DVI_DDC_DATA	DVI_DDC_DATA - @m38a_lib.M38A	97C2
DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @m38a_lib.M38A	97C3 97D5
DVI_HPD_UF	DVI_HPD_UF - @m38a_lib.M38A	97C3 97D5
ENET_C4106_2	ENET_C4106_2 - @m38a_lib.M38A	41D2
ENET_C4107_2	ENET_C4107_2 - @m38a_lib.M38A	41D2
ENET_C4117_1	ENET_C4117_1 - @m38a_lib.M38A	41B2
ENET_C4118_1	ENET_C4118_1 - @m38a_lib.M38A	41B2
ENET_CLK100M_PCIE_N	ENET_CLK100M_PCIE_N - @m38a_lib.M38A	5D5 34A4 34B2 41C5
ENET_CLK100M_PCIE_P	ENET_CLK100M_PCIE_P - @m38a_lib.M38A	5D5 34A4 34B2 41C5
ENET_CTRL12	ENET_CTRL12 - @m38a_lib.M38A TP_ENET_CTRL12 - @m38a_lib.M38A	41C7 42B8 42B7
ENET_CTRL25	ENET_CTRL25 - @m38a_lib.M38A	41C7 42C6
ENET_GATED_RST_L	ENET_GATED_RST_L - @m38a_lib.M38A	41C5 42D2
	ENET_RST_L - @m38a_lib.M38A	6B7 42D3
ENET_LED_ACT_L	ENET_LED_ACT_L - @m38a_lib.M38A	41C8
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m38a_lib.M38A	41C8
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m38a_lib.M38A	41C8
ENET_LED_LINK_L	ENET_LED_LINK_L - @m38a_lib.M38A	41C8
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m38a_lib.M38A	41C7
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ENET_RSET	ENET_RSET - @m38a_lib.M38A	41C7
ENET_VPD_CLK	ENET_VPD_CLK - @m38a_lib.M38A	41A2 41C4
ENET_VPD_DATA	ENET_VPD_DATA - @m38a_lib.M38A	41A2 41C4
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F0_RCFEEDBK	F0_RCFEEDBK - @m38a_lib.M38A	65C5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @m38a_lib.M38A	65D6
F1_GATESLOWDN	F1_GATESLOWDN - @m38a_lib.M38A	65B5
F1_RCFEEDBK	F1_RCFEEDBK - @m38a_lib.M38A	65B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @m38a_lib.M38A	65B6
F2_GATESLOWDN	F2_GATESLOWDN - @m38a_lib.M38A	66D4
F2_RCFEEDBK	F2_RCFEEDBK - @m38a_lib.M38A	66C5
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @m38a_lib.M38A	66D5
FAN_0_OUT	FAN_0_OUT - @m38a_lib.M38A	65C4
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FAN_1_OUT	FAN_1_OUT - @m38a_lib.M38A	65B4
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FSB_BPRI_L	FSB_BPRI_L - @m38a_lib.M38A	7D6 12C4

FSB_BREQ0_L	FSB_BREQ0_L - @m38a_lib.M38A	5C7 7D6 12C4
FSB_CLK_CPU_N	FSB_CLK_CPU_N - @m38a_lib.M38A	5C8 7C6 34B4 34C2
FSB_CLK_CPU_P	FSB_CLK_CPU_P - @m38a_lib.M38A	5C8 7C6 34B4 34C2
FSB_CLK_NB_N	FSB_CLK_NB_N - @m38a_lib.M38A	5C7 12A6 34B4 34C2
FSB_CLK_NB_P	FSB_CLK_NB_P - @m38a_lib.M38A	5C7 12A6 34B4 34C2
FSB_CPURST_L	FSB_CPURST_L - @m38a_lib.M38A	5C8 7D6 11B5 12C4
FSB_DBSY_L	FSB_DBSY_L - @m38a_lib.M38A	5C7 7D6 12B4
FSB_DEFER_L	FSB_DEFER_L - @m38a_lib.M38A	7D6 12B4
FSB_DINV_L<0>	FSB_DINV_L<0> - @m38a_lib.M38A	5D7 5D8 7C4 12B4
FSB_DINV_L<1>	FSB_DINV_L<1> - @m38a_lib.M38A	5D7 5D8 7B4 12B4
FSB_DINV_L<2>	FSB_DINV_L<2> - @m38a_lib.M38A	5D7 5D8 7C2 12B4
FSB_DINV_L<3>	FSB_DINV_L<3> - @m38a_lib.M38A	5D7 5D8 7B2 12B4
FSB_DPWR_L	FSB_DPWR_L - @m38a_lib.M38A	5C7 7B3 12B4
FSB_DRDY_L	FSB_DRDY_L - @m38a_lib.M38A	7D6 12B4
FSB_DSTBN_L<0>	FSB_DSTBN_L<0> - @m38a_lib.M38A	5D7 5D8 7C4 12B4
FSB_DSTBN_L<1>	FSB_DSTBN_L<1> - @m38a_lib.M38A	5D7 5D8 7B4 12B4
FSB_DSTBN_L<2>	FSB_DSTBN_L<2> - @m38a_lib.M38A	5D7 5D8 7C2 12B4
FSB_DSTBN_L<3>	FSB_DSTBN_L<3> - @m38a_lib.M38A	5D7 5D8 7B2 12B4
FSB_DSTBP_L<0>	FSB_DSTBP_L<0> - @m38a_lib.M38A	5D7 5D8 7C4 12B4
FSB_DSTBP_L<1>	FSB_DSTBP_L<1> - @m38a_lib.M38A	5D7 5D8 7B4 12B4
FSB_DSTBP_L<2>	FSB_DSTBP_L<2> - @m38a_lib.M38A	5D7 5D8 7C2 12B4
FSB_DSTBP_L<3>	FSB_DSTBP_L<3> - @m38a_lib.M38A	5D7 5D8 7B2 12B4
FSB_D_L<0>	FSB_D_L<0> - @m38a_lib.M38A	5D7 5D8 7C4 12D6
FSB_D_L<1>	FSB_D_L<1> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<2>	FSB_D_L<2> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<3>	FSB_D_L<3> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<4>	FSB_D_L<4> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<5>	FSB_D_L<5> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<6>	FSB_D_L<6> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<7>	FSB_D_L<7> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<8>	FSB_D_L<8> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<9>	FSB_D_L<9> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<10>	FSB_D_L<10> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<11>	FSB_D_L<11> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<12>	FSB_D_L<12> - @m38a_lib.M38A	7C4 12D6
FSB_D_L<13>	FSB_D_L<13> - @m38a_lib.M38A	7C4 12C6
FSB_D_L<14>	FSB_D_L<14> - @m38a_lib.M38A	7C4 12C6
FSB_D_L<15>	FSB_D_L<15> - @m38a_lib.M38A	7C4 12C6
FSB_D_L<16>	FSB_D_L<16> - @m38a_lib.M38A	5D7 5D8 7C4 12C6
FSB_D_L<17>	FSB_D_L<17> - @m38a_lib.M38A	7C4 12C6
FSB_D_L<18>	FSB_D_L<18> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<19>	FSB_D_L<19> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<20>	FSB_D_L<20> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<21>	FSB_D_L<21> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<22>	FSB_D_L<22> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<23>	FSB_D_L<23> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<24>	FSB_D_L<24> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<25>	FSB_D_L<25> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<26>	FSB_D_L<26> - @m38a_lib.M38A	7B4 12C6
FSB_D_L<27>	FSB_D_L<27> - @m38a_lib.M38A	7B4 12C6
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FSB_D_L<30>	FSB_D_L<30> - @m38a_lib.M38A	7B4 12C6
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FSB_D_L<32>	FSB_D_L<32> - @m38a_lib.M38A	7C2 12C6
FSB_D_L<33>	FSB_D_L<33> - @m38a_lib.M38A	7C2 12C6
FSB_D_L<34>	FSB_D_L<34> - @m38a_lib.M38A	7C2 12C6
FSB_D_L<35>	FSB_D_L<35> - @m38a_lib.M38A	7C2 12C6
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FSB_D_L<38>	FSB_D_L<38> - @m38a_lib.M38A	7C2 12C6
FSB_D_L<39>	FSB_D_L<39> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<40>	FSB_D_L<40> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<41>	FSB_D_L<41> - @m38a_lib.M38A	5D7 5D8 7C2 12B6
FSB_D_L<42>	FSB_D_L<42> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<43>	FSB_D_L<43> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<44>	FSB_D_L<44> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<45>	FSB_D_L<45> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<46>	FSB_D_L<46> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<47>	FSB_D_L<47> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<48>	FSB_D_L<48> - @m38a_lib.M38A	7C2 12B6
FSB_D_L<49>	FSB_D_L<49> - @m38a_lib.M38A	7C2 12B6
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FSB_D_L<52>	FSB_D_L<52> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<53>	FSB_D_L<53> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<54>	FSB_D_L<54> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<55>	FSB_D_L<55> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<56>	FSB_D_L<56> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<57>	FSB_D_L<57> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<58>	FSB_D_L<58> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<59>	FSB_D_L<59> - @m38a_lib.M38A	5D7 5D8 7B2 12B6
FSB_D_L<60>	FSB_D_L<60> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<61>	FSB_D_L<61> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<62>	FSB_D_L<62> - @m38a_lib.M38A	7B2 12B6
FSB_D_L<63>	FSB_D_L<63> - @m38a_lib.M38A	7B2 12B6
FSB_HITM_L	FSB_HITM_L - @m38a_lib.M38A	5C7 7D6 12B4
FSB_HIT_L	FSB_HIT_L - @m38a_lib.M38A	5C7 7D6 12B4
FSB_IERR_L	FSB_IERR_L - @m38a_lib.M38A	7D6
FSB_LOCK_L	FSB_LOCK_L - @m38a_lib.M38A	5D7 5D8 7D6 12B4
FSB_REQ_L<0>	FSB_REQ_L<0> - @m38a_lib.M38A	5C7 7D7 12B4
FSB_REQ_L<1>	FSB_REQ_L<1> - @m38a_lib.M38A	5C7 7D7 12B4
FSB_REQ_L<2>	FSB_REQ_L<2> - @m38a_lib.M38A	5C7 7D7 12A4
FSB_REQ_L<3>	FSB_REQ_L<3> - @m38a_lib.M38A	5C7 7D7 12A4
FSB_REQ_L<4>	FSB_REQ_L<4> - @m38a_lib.M38A	5C7 7D7 12A4
FSB_RS_L<0>	FSB_RS_L<0> - @m38a_lib.M38A	7D6 12A4
FSB_RS_L<1>	FSB_RS_L<1> - @m38a_lib.M38A	7D6 12A4
FSB_RS_L<2>	FSB_RS_L<2> - @m38a_lib.M38A	7D6 12A4
FSB_SLPCPU_L	FSB_SLPCPU_L - @m38a_lib.M38A	7A3 12A4
FSB_TRDY_L	FSB_TRDY_L - @m38a_lib.M38A	7D6 12A4
FWH_INIT_L	FWH_INIT_L - @m38a_lib.M38A	21C4 59C5 60C1
	SMC_CPU_INIT_3_3_L - @m38a_lib.M38A	58D5 59C6
FWH_MFG_MODE	FWH_MFG_MODE - @m38a_lib.M38A	23A6 23C5
FW_A_TPA_N	FW_A_TPA_N - @m38a_lib.M38A	44C3 46C8
	FW_PORT0_TPA_N - @m38a_lib.M38A	46C5 46C6
FW_A_TPA_P	FW_A_TPA_P - @m38a_lib.M38A	44C3 46C8
	FW_PORT0_TPA_P - @m38a_lib.M38A	46C5 46C6
FW_A_TPBIAS	FW_A_TPBIAS - @m38a_lib.M38A	44C4 46C8
FW_A_TPB_N	FW_A_TPB_N - @m38a_lib.M38A	44C3 46C8
	FW_PORT0_TPB_N - @m38a_lib.M38A	46C5 46C6
FW_A_TPB_P	FW_A_TPB_P - @m38a_lib.M38A	44C3 46C8
	FW_PORT0_TPB_P - @m38a_lib.M38A	46C5 46C6
FW_B_TPA_N	FW_B_TPA_N - @m38a_lib.M38A	44C3 46C8
	FW_PORT1_TPA_N - @m38a_lib.M38A	46B5 46C6
FW_B_TPA_P	FW_B_TPA_P - @m38a_lib.M38A	44C3 46C8
	FW_PORT1_TPA_P - @m38a_lib.M38A	46B5 46C6
FW_B_TPBIAS	FW_B_TPBIAS - @m38a_lib.M38A	44C4 46C8
FW_B_TPB_N	FW_B_TPB_N - @m38a_lib.M38A	44C3 46C8
	FW_PORT1_TPB_N - @m38a_lib.M38A	46B5 46C6
FW_B_TPB_P	FW_B_TPB_P - @m38a_lib.M38A	44C3 46C8
	FW_PORT1_TPB_P - @m38a_lib.M38A	46B5 46C6
FW_CARDBUS_L	FW_CARDBUS_L - @m38a_lib.M38A	44B5
FW_CONTENDER	FW_CONTENDER - @m38a_lib.M38A	44B3
FW_CPS	FW_CPS - @m38a_lib.M38A	44C3

FW_C_TPA_N	FW_C_TPA_N - @m38a_lib.M38A	44C3 46B8
	TP_FW_C_TPA_N - @m38a_lib.M38A	46B7
FW_C_TPA_P	FW_C_TPA_P - @m38a_lib.M38A	44C3 46B8
	TP_FW_C_TPA_P - @m38a_lib.M38A	46B7
FW_C_TPBIAS	FW_C_TPBIAS - @m38a_lib.M38A	44C4 46B8
	TP_FW_C_TPBIAS - @m38a_lib.M38A	46B7
FW_C_TPB_N	FW_C_TPB_N - @m38a_lib.M38A	44C3 46A8
	TP_FW_C_TPB_N - @m38a_lib.M38A	46A7
FW_C_TPB_P	FW_C_TPB_P - @m38a_lib.M38A	44C3 46A8
	TP_FW_C_TPB_P - @m38a_lib.M38A	46A7
FW_PC0	FW_PC0 - @m38a_lib.M38A	44B3
FW_PC1	FW_PC1 - @m38a_lib.M38A	44B3
FW_PC2	FW_PC2 - @m38a_lib.M38A	44B3
FW_PORT0_TPA_FL_N	FW_PORT0_TPA_FL_N - @m38a_lib.M38A	46C2
FW_PORT0_TPA_FL_P	FW_PORT0_TPA_FL_P - @m38a_lib.M38A	46C2
FW_PORT0_TPB_FL_N	FW_PORT0_TPB_FL_N - @m38a_lib.M38A	46C2
FW_PORT0_TPB_FL_P	FW_PORT0_TPB_FL_P - @m38a_lib.M38A	46C2
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m38a_lib.M38A	46B2
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m38a_lib.M38A	46B2
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m38a_lib.M38A	46B2
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m38a_lib.M38A	46B2
FW_R0	FW_R0 - @m38a_lib.M38A	44C4
FW_R1	FW_R1 - @m38a_lib.M38A	44C4
FW_RESET_L	FW_RESET_L - @m38a_lib.M38A	44C2 44C3
FW_ROM_CLK	FW_ROM_CLK - @m38a_lib.M38A	44B4
FW_SE	FW_SE - @m38a_lib.M38A	44B3
FW_SM	FW_SM - @m38a_lib.M38A	44B3
FW_TEST	FW_TEST - @m38a_lib.M38A	44B3
FW_TPA_C<0>	FW_TPA_C<0> - @m38a_lib.M38A	46B8
FW_TPA_C<1>	FW_TPA_C<1> - @m38a_lib.M38A	46B7
FW_VP	FW_VP - @m38a_lib.M38A	46D4
FW_XTAL_X0	FW_XTAL_X0 - @m38a_lib.M38A	44D2 44D3
FW_XTAL_XI	FW_XTAL_XI - @m38a_lib.M38A	44D2 44D3
FW_XTAL_XR	FW_XTAL_XR - @m38a_lib.M38A	44D2
GATE_3V3_S3	GATE_3V3_S3 - @m38a_lib.M38A	83B4
GATE_5V_S3	GATE_5V_S3 - @m38a_lib.M38A	83C4
GND_AUDIO	GND_AUDIO - @m38a_lib.M38A	6C2 74D2
GND_AUDIO_CODEC	GND_AUDIO_CODEC - @m38a_lib.M38A	68A5 68B7 68D2 72B8 72C8 73A8 73D4 74A2 74A3 74A5 74A7 74B5 74B7 74C1 74C3 74C5 74C6 74D1 74D5
GND_AUDIO_CODEC_EMI1	GND_AUDIO_CODEC_EMI1 - @m38a_lib.M38A	73A7
GND_AUDIO_MIC_CONN	GND_AUDIO_MIC_CONN - @m38a_lib.M38A	47C2 73C2
GND_AUDIO_SPKRAMP	GND_AUDIO_SPKRAMP - @m38a_lib.M38A	6C2 72B1 74D3
GND_AUDIO_SPKRAMP_PL ANE	GND_AUDIO_SPKRAMP_PLANE - @m38a_lib.M38A	72A6 72B2 72B5 72D2 72D8 74C3
GND_BNDI	GND_BNDI - @m38a_lib.M38A	47B2 47D1
GND_CHASSIS_AUDIO_EX TERNAL	GND_CHASSIS_AUDIO_EXTERNAL - @m38a_lib.M38A	6B2 73C7
	GND_CHASSIS_IO_LEFT - @m38a_lib.M38A	6B2
	GND_CHASSIS_USB - @m38a_lib.M38A	6B2 47A4 47B4 47C4
	GND_CHASSIS_IO_LEFT - @m38a_lib.M38A	6B2
GND_CHASSIS_AUDIO_EX TERNAL_J	GND_CHASSIS_AUDIO_EXTERNAL_J - @m38a_lib.M38A	73A8 73C5 73C8 74C1 74C3
GND_CHASSIS_AUDIO_IN TERNAL	GND_CHASSIS_AUDIO_INTERNAL - @m38a_lib.M38A	6A2 73C4
	GND_CHASSIS_BNDI - @m38a_lib.M38A	6A2 47C2 47C2 47D2
GND_CHASSIS_FIREWIRE	GND_CHASSIS_FIREWIRE - @m38a_lib.M38A	6B2 46A1 46C1
	GND_CHASSIS_RJ45 - @m38a_lib.M38A	6B2 43C6
	GND_CHASSIS_VGA - @m38a_lib.M38A	6B2 97C4
	GND_CHASSIS_RJ45 - @m38a_lib.M38A	6B2 43C6
	GND_CHASSIS_IO_RIGHT - @m38a_lib.M38A	6B1
GND_GPUVCORE_SGND	GND_GPUVCORE_SGND - @m38a_lib.M38A	85C7
GND_GPU_PCIE_PVSS	GND_GPU_PCIE_PVSS - @m38a_lib.M38A	84B8
GND_IMVP6_SGND	GND_IMVP6_SGND - @m38a_lib.M38A	75A4 75B6 75B8 75D7
GND_NB_VSSA_LVDS	GND_NB_VSSA_LVDS - @m38a_lib.M38A	17C6 19C2
	TP_GND_NB_VSSA_LVDS - @m38a_lib.M38A	19C1
GND_NEXT_TO_SMC	GND_NEXT_TO_SMC - @m38a_lib.M38A	59B2
GND_SMC_AVSS	GND_SMC_AVSS - @m38a_lib.M38A	58B2 58C4 59A3 59B3 76B2 76B6 76C5 85C1
GPUISENS_NEG	GPUISENS_NEG - @m38a_lib.M38A	85D3
GPUISENS_NTC	GPUISENS_NTC - @m38a_lib.M38A	85D3
GPUISENS_POS	GPUISENS_POS - @m38a_lib.M38A	85D3
GPUISENS_RC	GPUISENS_RC - @m38a_lib.M38A	85D3
GPUVCORE_BOOT	GPUVCORE_BOOT - @m38a_lib.M38A	85C5
GPUVCORE_COMP	GPUVCORE_COMP - @m38a_lib.M38A	85C7
GPUVCORE_COMP_R	GPUVCORE_COMP_R - @m38a_lib.M38A	85C7
GPUVCORE_EN	GPUVCORE_EN - @m38a_lib.M38A	85C8 88A8
GPUVCORE_FB	GPUVCORE_FB - @m38a_lib.M38A	85C7
GPUVCORE_FCCM	GPUVCORE_FCCM - @m38a_lib.M38A	85C7
GPUVCORE_FSET	GPUVCORE_FSET - @m38a_lib.M38A	85C7
GPUVCORE_IOUT	GPUVCORE_IOUT - @m38a_lib.M38A	59C5 85D1
	SMC_GPU_ISENSE - @m38a_lib.M38A	58D5 59C6
GPUVCORE_ISEN	GPUVCORE_ISEN - @m38a_lib.M38A	85C5
GPUVCORE_LG	GPUVCORE_LG - @m38a_lib.M38A	85C5
GPUVCORE_PGOOD	GPUVCORE_PGOOD - @m38a_lib.M38A	77A4 85C8
GPUVCORE_PHASE	GPUVCORE_PHASE - @m38a_lib.M38A	85C5
GPUVCORE_UG	GPUVCORE_UG - @m38a_lib.M38A	85C5
GPU_B2	GPU_B2 - @m38a_lib.M38A	93B3 97B8
GPU_CLK27M	GPU_CLK27M - @m38a_lib.M38A	92C6
	GPU_XTALIN - @m38a_lib

IMVP6_UGATE1	IMVP6_UGATE1 - @m38a_lib.M38A	75A8 75C5
IMVP6_UGATE2	IMVP6_UGATE2 - @m38a_lib.M38A	75A6 75C5
IMVP6_VDIFF	IMVP6_VDIFF - @m38a_lib.M38A	75A4 75B6
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m38a_lib.M38A	75B7
IMVP6_VO	IMVP6_VO - @m38a_lib.M38A	75A4 75B4
IMVP6_VO_R	IMVP6_VO_R - @m38a_lib.M38A	75B4
IMVP6_VR_TT	IMVP6_VR_TT - @m38a_lib.M38A	75C7
IMVP6_VSEN	IMVP6_VSEN - @m38a_lib.M38A	75A4 75B5
IMVP6_VSUM	IMVP6_VSUM - @m38a_lib.M38A	75A4 75C5
IMVP6_VSUM_R1	IMVP6_VSUM_R1 - @m38a_lib.M38A	75A8 75C2
IMVP6_VSUM_R2	IMVP6_VSUM_R2 - @m38a_lib.M38A	75A6 75B2
IMVP6_VW	IMVP6_VW - @m38a_lib.M38A	75A4 75B6
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m38a_lib.M38A	75C6
IMVP_PGD_IN	IMVP_PGD_IN - @m38a_lib.M38A	75C6 77D5
IMVP_VID<0>	IMVP_VID<0> - @m38a_lib.M38A	75C6
IMVP_VID<1>	IMVP_VID<1> - @m38a_lib.M38A	75C7
IMVP_VID<2>	IMVP_VID<2> - @m38a_lib.M38A	75C7
IMVP_VID<3>	IMVP_VID<3> - @m38a_lib.M38A	75C7
IMVP_VID<4>	IMVP_VID<4> - @m38a_lib.M38A	75C7
IMVP_VID<5>	IMVP_VID<5> - @m38a_lib.M38A	75C7
IMVP_VID<6>	IMVP_VID<6> - @m38a_lib.M38A	75C7
IMVP_VR_ON	IMVP_VR_ON - @m38a_lib.M38A	58D7 75C6
INT_PIRQA_L	INT_PIRQA_L - @m38a_lib.M38A	22A7 26D2
INT_PIRQB_L	INT_PIRQB_L - @m38a_lib.M38A	22A7 26D2
INT_PIRQC_L	INT_PIRQC_L - @m38a_lib.M38A	22A7 26D2
INT_PIRQD_L	INT_PIRQD_L - @m38a_lib.M38A	22A7 26D2 44B5
INT_SERIRQ	INT_SERIRQ - @m38a_lib.M38A	23C8 58C7 60C1 67C6
ISENSE_CAL_EN	ISENSE_CAL_EN - @m38a_lib.M38A	58B7 76A8
ITPRESET_L	ITPRESET_L - @m38a_lib.M38A	11B3
ITP_TDO	ITP_TDO - @m38a_lib.M38A	11B3
ITS_ALIVE	ITS_ALIVE - @m38a_lib.M38A	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @m38a_lib.M38A	6A7
KBC_MDE	KBC_MDE - @m38a_lib.M38A	58C2
LCD_PWM	LCD_PWM - @m38a_lib.M38A	94B1 94C3
LCD_PWM_R	LCD_PWM_R - @m38a_lib.M38A	94B2
LCD_PWREN_L	LCD_PWREN_L - @m38a_lib.M38A	94C8
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @m38a_lib.M38A	94C7
LCD_SHOULD_ON	LCD_SHOULD_ON - @m38a_lib.M38A	6A6
LED_PP1V05_S0_N	LED_PP1V05_S0_N - @m38a_lib.M38A	81A4
LED_PP1V05_S0_P	LED_PP1V05_S0_P - @m38a_lib.M38A	81A4
LED_PP1V5_S0_N	LED_PP1V5_S0_N - @m38a_lib.M38A	80A3
LED_PP1V5_S0_P	LED_PP1V5_S0_P - @m38a_lib.M38A	80A4
LED_PP1V8_S3_N	LED_PP1V8_S3_N - @m38a_lib.M38A	79A4
LED_PP1V8_S3_P	LED_PP1V8_S3_P - @m38a_lib.M38A	79A4
LPC_AD<0>	LPC_AD<0> - @m38a_lib.M38A	21D4 58D7 60C4 67C6
LPC_AD<1>	LPC_AD<1> - @m38a_lib.M38A	21D4 58D7 60C4 67C6
LPC_AD<2>	LPC_AD<2> - @m38a_lib.M38A	21D4 58C7 60C1 67C6
LPC_AD<3>	LPC_AD<3> - @m38a_lib.M38A	21D4 58C7 60C1 67C6
LPC_FRAME_L	LPC_FRAME_L - @m38a_lib.M38A	21C5 58C7 60C4 67C6
LVDS_A_CLK_N	LVDS_A_CLK_N - @m38a_lib.M38A	13D5 19D2
	TP_LVDS_A_CLK_N - @m38a_lib.M38A	19D1
LVDS_A_CLK_P	LVDS_A_CLK_P - @m38a_lib.M38A	13C5 19D2
	TP_LVDS_A_CLK_P - @m38a_lib.M38A	19D1
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m38a_lib.M38A	13C5 19D2
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m38a_lib.M38A	13C5 19D2
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m38a_lib.M38A	13C5 19D2
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m38a_lib.M38A	13C5 19D2
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m38a_lib.M38A	13C5 19D2
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m38a_lib.M38A	13C5 19D2
LVDS_BKLTCTL	LVDS_BKLTCTL - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_BKLTCTL - @m38a_lib.M38A	19C1
LVDS_BKLTEN	LVDS_BKLTEN - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_BKLTEN - @m38a_lib.M38A	19C1
LVDS_B_CLK_N	LVDS_B_CLK_N - @m38a_lib.M38A	13C5 19D2
	TP_LVDS_B_CLK_N - @m38a_lib.M38A	19D1
LVDS_B_CLK_P	LVDS_B_CLK_P - @m38a_lib.M38A	13C5 19D2
	TP_LVDS_B_CLK_P - @m38a_lib.M38A	19D1
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m38a_lib.M38A	13C5 19D2
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m38a_lib.M38A	13C5 19D2
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m38a_lib.M38A	13C5 19D2
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m38a_lib.M38A	13C5 19D2
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m38a_lib.M38A	13C5 19D2
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m38a_lib.M38A	13C5 19D2
LVDS_CLKCTLA	LVDS_CLKCTLA - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_CLKCTLA - @m38a_lib.M38A	19C1
LVDS_CLKCTLB	LVDS_CLKCTLB - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_CLKCTLB - @m38a_lib.M38A	19C1
LVDS_DDC_CLK	LVDS_DDC_CLK - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_DDC_CLK - @m38a_lib.M38A	19C1
LVDS_DDC_DATA	LVDS_DDC_DATA - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_DDC_DATA - @m38a_lib.M38A	19C1
LVDS_IBG	LVDS_IBG - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_IBG - @m38a_lib.M38A	19C1
LVDS_L_CLK_N	LVDS_L_CLK_N - @m38a_lib.M38A	93A3 93D2 94A6
LVDS_L_CLK_P	LVDS_L_CLK_P - @m38a_lib.M38A	93A3 93D2 94A7
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @m38a_lib.M38A	93A3 93C2 94A6
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @m38a_lib.M38A	93A3 93C2 94A7
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @m38a_lib.M38A	93A3 93C2 94A6
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @m38a_lib.M38A	93A3 94A6
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @m38a_lib.M38A	93A3 93D2 94A7
LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @m38a_lib.M38A	93A3 93C2 94A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @m38a_lib.M38A	93A3 93C2 94A7
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @m38a_lib.M38A	93A3 94A7
LVDS_U_CLK_N	LVDS_U_CLK_N - @m38a_lib.M38A	93B3 94B6
LVDS_U_CLK_P	LVDS_U_CLK_P - @m38a_lib.M38A	93B3 94A7
LVDS_U_DATA_N<0>	LVDS_U_DATA_N<0> - @m38a_lib.M38A	93B3 94B7
LVDS_U_DATA_N<1>	LVDS_U_DATA_N<1> - @m38a_lib.M38A	93B3 94B7
LVDS_U_DATA_N<2>	LVDS_U_DATA_N<2> - @m38a_lib.M38A	93B3 94B7
LVDS_U_DATA_N<3>	LVDS_U_DATA_N<3> - @m38a_lib.M38A	93B3 94A6
LVDS_U_DATA_P<0>	LVDS_U_DATA_P<0> - @m38a_lib.M38A	93B3 94B6
LVDS_U_DATA_P<1>	LVDS_U_DATA_P<1> - @m38a_lib.M38A	93B3 94B6
LVDS_U_DATA_P<2>	LVDS_U_DATA_P<2> - @m38a_lib.M38A	93B3 94B6
LVDS_U_DATA_P<3>	LVDS_U_DATA_P<3> - @m38a_lib.M38A	93B3 94A7
LVDS_VDDEN	LVDS_VDDEN - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_VDDEN - @m38a_lib.M38A	19C1
LVDS_VREFH	LVDS_VREFH - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_VREFH - @m38a_lib.M38A	19C1
LVDS_VREFL	LVDS_VREFL - @m38a_lib.M38A	13D5 19C2
	TP_LVDS_VREFL - @m38a_lib.M38A	19C1
MEMVTT_VREF	MEMVTT_VREF - @m38a_lib.M38A	31B4
MEM_A_A<0>	MEM_A_A<0> - @m38a_lib.M38A	15C5 28B3
MEM_A_A<13..0>	MEM_A_A<13..0> - @m38a_lib.M38A	30C6
MEM_A_A<1>	MEM_A_A<1> - @m38a_lib.M38A	15C5 28B6
MEM_A_A<2>	MEM_A_A<2> - @m38a_lib.M38A	15C5 28B3
MEM_A_A<3>	MEM_A_A<3> - @m38a_lib.M38A	15B5 28B6
MEM_A_A<4>	MEM_A_A<4> - @m38a_lib.M38A	15B5 28B3
MEM_A_A<5>	MEM_A_A<5> - @m38a_lib.M38A	15B5 28B6
MEM_A_A<6>	MEM_A_A<6> - @m38a_lib.M38A	15B5 28C3
MEM_A_A<7>	MEM_A_A<7> - @m38a_lib.M38A	15B5 28C3
MEM_A_A<8>	MEM_A_A<8> - @m38a_lib.M38A	15B5 28B6
MEM_A_A<9>	MEM_A_A<9> - @m38a_lib.M38A	15B5 28C6
MEM_A_A<10>	MEM_A_A<10> - @m38a_lib.M38A	15B5 28C6
MEM_A_A<11>	MEM_A_A<11> - @m38a_lib.M38A	15B5 28C3
MEM_A_A<12>	MEM_A_A<12> - @m38a_lib.M38A	15B5 28C6
MEM_A_A<13>	MEM_A_A<13> - @m38a_lib.M38A	15B5 28B3
MEM_A_BS<0>	MEM_A_BS<0> - @m38a_lib.M38A	15D5 28B3
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @m38a_lib.M38A	30C6
MEM_A_BS<1>	MEM_A_BS<1> - @m38a_lib.M38A	15D5 28B3
MEM_A_BS<2>	MEM_A_BS<2> - @m38a_lib.M38A	15D5 28C6
MEM_A_CAS_L	MEM_A_CAS_L - @m38a_lib.M38A	15D5 28B6 30B6
MEM_A_DM<0>	MEM_A_DM<0> - @m38a_lib.M38A	15D5 28D3
MEM_A_DM<1>	MEM_A_DM<1> - @m38a_lib.M38A	15D5 28D3
MEM_A_DM<2>	MEM_A_DM<2> - @m38a_lib.M38A	15D5 28C3
MEM_A_DM<3>	MEM_A_DM<3> - @m38a_lib.M38A	15C5 28C6
MEM_A_DM<4>	MEM_A_DM<4> - @m38a_lib.M38A	15C5 28B3
MEM_A_DM<5>	MEM_A_DM<5> - @m38a_lib.M38A	15C5 28A6
MEM_A_DM<6>	MEM_A_DM<6> - @m38a_lib.M38A	15C5 28A3
MEM_A_DM<7>	MEM_A_DM<7> - @m38a_lib.M38A	15C5 28A6
MEM_A_DQ<0>	MEM_A_DQ<0> - @m38a_lib.M38A	15D7 28D6
MEM_A_DQ<1>	MEM_A_DQ<1> - @m38a_lib.M38A	15D7 28D6
MEM_A_DQ<2>	MEM_A_DQ<2> - @m38a_lib.M38A	15D7 28D6
MEM_A_DQ<3>	MEM_A_DQ<3> - @m38a_lib.M38A	15D7 28D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @m38a_lib.M38A	15D7 28D3
MEM_A_DQ<5>	MEM_A_DQ<5> - @m38a_lib.M38A	15D7 28D3
MEM_A_DQ<6>	MEM_A_DQ<6> - @m38a_lib.M38A	15D7 28D3
MEM_A_DQ<7>	MEM_A_DQ<7> - @m38a_lib.M38A	5B7 15D7 28D3
MEM_A_DQ<8>	MEM_A_DQ<8> - @m38a_lib.M38A	15C7 28D6
MEM_A_DQ<9>	MEM_A_DQ<9> - @m38a_lib.M38A	15C7 28D6
MEM_A_DQ<10>	MEM_A_DQ<10> - @m38a_lib.M38A	15C7 28D6
MEM_A_DQ<11>	MEM_A_DQ<11> - @m38a_lib.M38A	15C7 28D6
MEM_A_DQ<12>	MEM_A_DQ<12> - @m38a_lib.M38A	15C7 28D3
MEM_A_DQ<13>	MEM_A_DQ<13> - @m38a_lib.M38A	15C7 28D3
MEM_A_DQ<14>	MEM_A_DQ<14> - @m38a_lib.M38A	5B7 15C7 28D3
MEM_A_DQ<15>	MEM_A_DQ<15> - @m38a_lib.M38A	15C7 28D3
MEM_A_DQ<16>	MEM_A_DQ<16> - @m38a_lib.M38A	5B7 15C7 28C6
MEM_A_DQ<17>	MEM_A_DQ<17> - @m38a_lib.M38A	15C7 28C6
MEM_A_DQ<18>	MEM_A_DQ<18> - @m38a_lib.M38A	15C7 28C6
MEM_A_DQ<19>	MEM_A_DQ<19> - @m38a_lib.M38A	15C7 28C6
MEM_A_DQ<20>	MEM_A_DQ<20> - @m38a_lib.M38A	15C7 28C3
MEM_A_DQ<21>	MEM_A_DQ<21> - @m38a_lib.M38A	15C7 28C3
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MEM_A_DQ<24>	MEM_A_DQ<24> - @m38a_lib.M38A	15C7 28C6
MEM_A_DQ<25>	MEM_A_DQ<25> - @m38a_lib.M38A	5B7 15C7 28C6
MEM_A_DQ<26>	MEM_A_DQ<26> - @m38a_lib.M38A	15C7 28C6
MEM_A_DQ<27>	MEM_A_DQ<27> - @m38a_lib.M38A	15C7 28C6
MEM_A_DQ<28>	MEM_A_DQ<28> - @m38a_lib.M38A	15C7 28C3
MEM_A_DQ<29>	MEM_A_DQ<29> - @m38a_lib.M38A	15C7 28C3
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MEM_A_DQ<32>	MEM_A_DQ<32> - @m38a_lib.M38A	15C7 28B6
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MEM_A_DQ<34>	MEM_A_DQ<34> - @m38a_lib.M38A	15B7 28B6
MEM_A_DQ<35>	MEM_A_DQ<35> - @m38a_lib.M38A	15B7 28B6
MEM_A_DQ<36>	MEM_A_DQ<36> - @m38a_lib.M38A	15B7 28B3
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MEM_A_DQ<40>	MEM_A_DQ<40> - @m38a_lib.M38A	15B7 28B6
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MEM_A_DQ<42>	MEM_A_DQ<42> - @m38a_lib.M38A	15B7 28A6
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MEM_A_DQ<44>	MEM_A_DQ<44> - @m38a_lib.M38A	15B7 28B3
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MEM_A_DQ<47>	MEM_A_DQ<47> - @m38a_lib.M38A	5B7 15B7 28A3
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MEM_A_DQ<54>	MEM_A_DQ<54> - @m38a_lib.M38A	5B7 15B7 28A3
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MEM_A_DQ<58>	MEM_A_DQ<58> - @m38a_lib.M38A	15B7 28A6
MEM_A_DQ<59>	MEM_A_DQ<59> - @m38a_lib.M38A	5B7 15B7 28A6
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MEM_A_DQ<61>	MEM_A_DQ<61> - @m38a_lib.M38A	15A7 28A3
MEM_A_DQ<62>	MEM_A_DQ<62> - @m38a_lib.M38A	15A7 28A3
MEM_A_DQ<63>	MEM_A_DQ<63> - @m38a_lib.M38A	15A7 28A3
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @m38a_lib.M38A	5B7 15C5 28D6
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @m38a_lib.M38A	5B7 15C5 28D6
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @m38a_lib.M38A	5B7 15C5 28C6
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @m38a_lib.M38A	5B7 15C5 28C3
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @m38a_lib.M38A	5B7 15C5 28B6
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @m38a_lib.M38A	5B7 15C5 28B3
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @m38a_lib.M38A	5B7 15C5 28A6
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @m38a_lib.M38A	5B7 15C5 28A3
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @m38a_lib.M38A	5B7 15C5 28D6
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @m38a_lib.M38A	5B7 15C5 28D6
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @m38a_lib.M38A	5B7 15C5 28C6
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @m38a_lib.M38A	5B7 15C5 28C3
MEM_A_DQS_P<4>	MEM_A_DQS_P<4> - @m38a_lib.M38A	5B7 15C5 28B6
MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @m38a_lib.M38A	5B7 15C5 28A3
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @m38a_lib.M38A	5B7 15C5 28A6
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @m38a_lib.M38A	5B7 15C5 28A3
MEM_A_RAS_L	MEM_A_RAS_L - @m38a_lib.M38A	15B5 28B3 30B6
MEM_A_WE_L	MEM_A_WE_L - @m38a_lib.M38A	15B5 28B6 30B6
MEM_B_A<0>	MEM_B_A<0> - @m38a_lib.M38A	15C2 29B3 30B5
MEM_B_A<1>	MEM_B_A<1> - @m38a_lib.M38A	15C2 29B6 30B5
MEM_B_A<2>	MEM_B_A<2> - @m38a_lib.M38A	15C2 29B3 30B5
MEM_B_A<3>	MEM_B_A<3> - @m38a_lib.M38A	15B2 29B6 30B5
MEM_B_A<4>	MEM_B_A<4> - @m38a_lib.M38A	15B2 29B3 30B5
MEM_B_A<5>	MEM_B_A<5> - @m38a_lib.M38A	15B2 29B6 30B5
MEM_B_A<6>	MEM_B_A<6> - @m38a_lib.M38A	15B2 29C3 30B5
MEM_B_A<7>	MEM_B_A<7> - @m38a_lib.M38A	15B2 29C3 30B5
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MEM_B_BS<2..0>	MEM_B_BS<2..0> - @m38a_lib.M38A	30A6
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PCI_CLK_PORT80	PCI_CLK_PORT80 - @m38a_lib.M38A 34B4 60C1
PCI_CLK_SB	PCI_CLK_SB - @m38a_lib.M38A 5C8 22A6 34B4
PCI_CLK_SMC	PCI_CLK_SMC - @m38a_lib.M38A 34C4 58C7
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PCI_FRAME_L	PCI_FRAME_L - @m38a_lib.M38A 22A7 26D2 44B5
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PLT_RST_L	PLT_RST_L - @m38a_lib.M38A 6C8 22A6
PM_BATLOW_L	PM_BATLOW_L - @m38a_lib.M38A 23C1 58B7
PM_BMBUSY_L	PM_BMBUSY_L - @m38a_lib.M38A 14B6 23C5
PM_CLKRUN_L	PM_CLKRUN_L - @m38a_lib.M38A 5B8 23C8 44B5 58C5 60C4 67C6
PM_DPRSLPVR	PM_DPRSLPVR - @m38a_lib.M38A 14B7 23C3 75C7
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	DIMM_OVERTEMP_L - @m38a_lib.M38A 28C3 29C3 59C6
PM_LAN_ENABLE	PM_LAN_ENABLE - @m38a_lib.M38A 23C3 58D7
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PM_PWROK	PM_PWROK - @m38a_lib.M38A 77C5
PM_RI_L	PM_RI_L - @m38a_lib.M38A 23D5
PM_RSMRST_L	PM_RSMRST_L - @m38a_lib.M38A 23C1 58D7
PM_SB_PWROK	PM_SB_PWROK - @m38a_lib.M38A 23C3 26D6
PM_SLP_S3	PM_SLP_S3 - @m38a_lib.M38A 77D7 78B8 80C8 81C8
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	MEMVTT_EN - @m38a_lib.M38A 31B5 79A6
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PM_SLP_S4_L	PM_SLP_S4_L - @m38a_lib.M38A 23C3 58C5 77C8
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PM_THRMTRIP_L	PM_THRMTRIP_L - @m38a_lib.M38A 7C6 14B6 21C2 59C7
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POWER_BUTTON_L	POWER_BUTTON_L - @m38a_lib.M38A 5D1 59C8
PP0V9_S0_PGOOD	PP0V9_S0_PGOOD - @m38a_lib.M38A 77D6 79A2
PP1V2_S0_GPU_VDDPLL	PP1V2_S0_GPU_VDDPLL - @m38a_lib.M38A 91B6
PP1V05_S0_PGOOD	PP1V05_S0_PGOOD - @m38a_lib.M38A 77D6 81B2
PP1V5_S0_NB_3GPLL_F	PP1V5_S0_NB_3GPLL_F - @m38a_lib.M38A 19A5
PP1V5_S0_NB_VCC3G	PP1V5_S0_NB_VCC3G - @m38a_lib.M38A 17D6 19A3
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	PP1V5_S0_NB_VCCA_DPLLA - @m38a_lib.M38A 19C5
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PP1V5_S0_SB_R	PP1V5_S0_SB_R - @m38a_lib.M38A 25A7
PP1V5_S0_SB_VCC1_5_B	PP1V5_S0_SB_VCC1_5_B - @m38a_lib.M38A 22C1 24D5 25B7
PP1V5_S0_SB_VCCDMIPL	PP1V5_S0_SB_VCCDMIPLL - @m38a_lib.M38A 24B5 25A6
PP1V8R2V0_S0_GPU_VDD	PP1V8R2V0_S0_GPU_VDDRH0 - @m38a_lib.M38A 87A7
PP1V8R2V0_S0_GPU_VDD	PP1V8R2V0_S0_GPU_VDDRH1 - @m38a_lib.M38A 87B3
PP1V8R3V3_S0_GPU_VDD	PP1V8R3V3_S0_GPU_VDDR4_F - @m38a_lib.M38A 91B6
PP1V8R3V3_S0_GPU_VDD	PP1V8R3V3_S0_GPU_VDDR5_F - @m38a_lib.M38A 91B6
PP1V8_FB_A0_VDDA0	PP1V8_FB_A0_VDDA0 - @m38a_lib.M38A 89D7
PP1V8_FB_A0_VDDA1	PP1V8_FB_A0_VDDA1 - @m38a_lib.M38A 89D7
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PP1V8_FB_B1_VDDA1	PP1V8_FB_B1_VDDA1 - @m38a_lib.M38A 90D4
PP1V8_S3_PGOOD	PP1V8_S3_PGOOD - @m38a_lib.M38A 79B2
PP2V5_S0_PGOOD	PP2V5_S0_PGOOD - @m38a_lib.M38A 77C6 77D3
PP2V5_ENET_CTAP	PP2V5_ENET_CTAP - @m38a_lib.M38A 43D7
PP2V5_S0_GPU_A2VDD	PP2V5_S0_GPU_A2VDD - @m38a_lib.M38A 93B7
PP2V5_S0_GPU_AVDD	PP2V5_S0_GPU_AVDD - @m38a_lib.M38A 93C7
PP2V5_S0_GPU_LPVDD	PP2V5_S0_GPU_LPVDD - @m38a_lib.M38A 93B7
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PP2V5_S0_GPU_TPVDD	PP2V5_S0_GPU_TPVDD - @m38a_lib.M38A 93C7
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PP2V5_S0_GPU_VDD2DI	PP2V5_S0_GPU_VDD2DI - @m38a_lib.M38A 93B8
PP3V3R12V_LCD_CONN	PP3V3R12V_LCD_CONN - @m38a_lib.M38A 94A6 94A6 94A7 94C5
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PP3V3_AUDIO_SPDIF_JACK	PP3V3_AUDIO_SPDIF_JACK - @m38a_lib.M38A 73B5 73D8
PP3V3_AVCC_SMC	PP3V3_AVCC_SMC - @m38a_lib.M38A 58D3
PP3V3_AVREF_SMC	PP3V3_AVREF_SMC - @m38a_lib.M38A 58D2 59A3
PP3V3_FW_ESD	PP3V3_FW_ESD - @m38a_lib.M38A 46A5 46A6 46B5 46C5 46D5
PP3V3_FW_ESD_F	PP3V3_FW_ESD_F - @m38a_lib.M38A 46A7
PP3V3_INTERCON	PP3V3_INTERCON - @m38a_lib.M38A 72C7
PP3V3_LCD_SW	PP3V3_LCD_SW - @m38a_lib.M38A 94C6
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PP3V3_S0_CK410_VDDA	PP3V3_S0_CK410_VDDA - @m38a_lib.M38A 33C6
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PP3V3_S0_CK410_VDD_P CI	PP3V3_S0_CK410_VDD_PCI - @m38a_lib.M38A 33D5
PP3V3_S0_CK410_VDD_R EF	PP3V3_S0_CK410_VDD_REF - @m38a_lib.M38A 33C5
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PP3V3_S5_FW_VDDA	PP3V3_S5_FW_VDDA - @m38a_lib.M38A 44D5 45C6
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PP3V3_SO_2V5REG_R	PP3V3_SO_2V5REG_R - @m38a_lib.M38A 77D3
PP3V3_TPM_3VSB	PP3V3_TPM_3VSB - @m38a_lib.M38A 59C5 67C4
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @m38a_lib.M38A 68A2 68D2 74C4 74D8
PP5V_BNDI_LE340	PP5V_BNDI_LE340 - @m38a_lib.M38A 47D3
PP5V_S0_DDC	PP5V_S0_DDC - @m38a_lib.M38A 97D4
PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @m38a_lib.M38A 97D5
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PP5V_S3_BNDI	PP5V_S3_BNDI - @m38a_lib.M38A 47B2 47D1
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PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @m38a_lib.M38A 47D6
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PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @m38a_lib.M38A 47C6
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @m38a_lib.M38A 47C5
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @m38a_lib.M38A 47B6
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @m38a_lib.M38A 47B4
PP12V_AUD_SPKRAMP_PL ANE	PP12V_AUD_SPKRAMP_PLANE - @m38a_lib.M38A 72D5
PP12V_L7502	PP12V_L7502 - @m38a_lib.M38A 76D7
PP12V_S5_CPU_REG	PP12V_S5_CPU_REG - @m38a_lib.M38A 75C3 75D4 75D7 76C8 76D6
PPFW_PORT0_VP	PPFW_PORT0_VP - @m38a_lib.M38A 46D2
	PPFW_PORT1_VP - @m38a_lib.M38A 46B2 46D1
	PPFW_PORTS_VP - @m38a_lib.M38A 46D3
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PPFW_PORT1_VP_FL	PPFW_PORT1_VP_FL - @m38a_lib.M38A 46B2
PPVCORE_S0_GPU_MPVDD	PPVCORE_S0_GPU_MPVDD - @m38a_lib.M38A 91A6
PPVCORE_S0_GPU_VDDCI	PPVCORE_S0_GPU_VDDCI - @m38a_lib.M38A 86C7
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @m38a_lib.M38A 75D6
PPV_3V3_AUDIO_CODEC	PPV_3V3_AUDIO_CODEC - @m38a_lib.M38A 68D6
Q4201_3	Q4201_3 - @m38a_lib.M38A 42D6
Q5950_1	Q5950_1 - @m38a_lib.M38A 60A7
R6000_1	R6000_1 - @m38a_lib.M38A 60A6
R6001_1	R6001_1 - @m38a_lib.M38A 60A6
R6002_1	R6002_1 - @m38a_lib.M38A 60A6
R6003_2	R6003_2 - @m38a_lib.M38A 60A5
R7504_1	R7504_1 - @m38a_lib.M38A 75A8 75C1
R7507_1	R7507_1 - @m38a_lib.M38A 75A6 75B1
R8599_2	R8599_2 - @m38a_lib.M38A 85C4
RSMRST_PWRGD	RSMRST_PWRGD - @m38a_lib.M38A 58D7 76D1
SATA_A_D2R_N	SATA_A_D2R_N - @m38a_lib.M38A 21B6 38A6
	TP_SATA_A_D2R_N - @m38a_lib.M38A 38A5
SATA_A_D2R_P	SATA_A_D2R_P - @m38a_lib.M38A 21B6 38A6
	TP_SATA_A_D2R_P - @m38a_lib.M38A 38A5
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @m38a_lib.M38A 21B6 38A6
	TP_SATA_A_R2D_N - @m38a_lib.M38A 38A5
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @m38a_lib.M38A 21B6 38A6
	TP_SATA_A_R2D_P - @m38a_lib.M38A 38A5
SATA_C_D2R_C_N	SATA_C_D2R_C_N - @m38a_lib.M38A 38B8
SATA_C_D2R_C_P	SATA_C_D2R_C_P - @m38a_lib.M38A 38B8
SATA_C_D2R_N	SATA_C_D2R_N - @m38a_lib.M38A 21B6 38B6
SATA_C_D2R_P	SATA_C_D2R_P - @m38a_lib.M38A 21B6 38B6
SATA_C_DET_L	SATA_C_DET_L - @m38a_lib.M38A 23D2 38B5
SATA_C_PWR_EN_L	SATA_C_PWR_EN_L - @m38a_lib.M38A 23A3 23B3
SATA_C_R2D_C_N	SATA_C_R2D_C_N - @m38a_lib.M38A 21B6 38B6
SATA_C_R2D_C_P	SATA_C_R2D_C_P - @m38a_lib.M38A 21B6 38B6
SATA_C_R2D_N	SATA_C_R2D_N - @m38a_lib.M38A 38B8
SATA_C_R2D_P	SATA_C_R2D_P - @m38a_lib.M38A 38B8
SATA_RBIAS_N	SATA_RBIAS_N - @m38a_lib.M38A 21B6 38C7
	SATA_RBIAS_P - @m38a_lib.M38A 21B6 38C7
	SATA_RBIAS - @m38a_lib.M38A 38C7
	SATA_RBIAS_P - @m38a_lib.M38A 21B6 38C7
	SATA_RBIAS - @m38a_lib.M38A 38C7
SB_A20GATE	SB_A20GATE - @m38a_lib.M38A 21C4
SB_ACZ_BITCLK	SB_ACZ_BITCLK - @m38a_lib.M38A 21C6
SB_ACZ_RST_L	SB_ACZ_RST_L - @m38a_lib.M38A 21C6
SB_ACZ_SDATAOUT	SB_ACZ_SDATAOUT - @m38a_lib.M38A 21C6
SB_ACZ_SYNC	SB_ACZ_SYNC - @m38a_lib.M38A 21C6
SB_CLK14P3M_TIMER	SB_CLK14P3M_TIMER - @m38a_lib.M38A 5B8 23D3 34D4
SB_CLK48M_USBCTLR	SB_CLK48M_USBCTLR - @m38a_lib.M38A 5B8 23D3 34C4

SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @m38a_lib.M38A	23C1 58D5
SMC_XDP_TCK	SMC_XDP_TCK - @m38a_lib.M38A	58C7
SMC_XDP_TCK_3_3	SMC_XDP_TCK_3_3 - @m38a_lib.M38A	58B5 59A5
SMC_XDP_TDO_3_3_L	SMC_XDP_TDO_3_3_L - @m38a_lib.M38A	58B7 59A5
SMC_XDP_TMS_L	SMC_XDP_TMS_L - @m38a_lib.M38A	58C7
SMC_XDP_TRST_L	SMC_XDP_TRST_L - @m38a_lib.M38A	58C7
SMC_XTAL	SMC_XTAL - @m38a_lib.M38A	58C3 59B8
SMLINK<0>	SMLINK<0> - @m38a_lib.M38A	23D5
SMLINK<1>	SMLINK<1> - @m38a_lib.M38A	23D5
SMS_INT_L	SMS_INT_L - @m38a_lib.M38A	23C3 26C2 58B5
SMS_ONOFF_L	SMS_ONOFF_L - @m38a_lib.M38A	58A5 59B4
SMS_X_AXIS	SMS_X_AXIS - @m38a_lib.M38A	58B7 59B6
	NC_SMS_X_AXIS - @m38a_lib.M38A	59B5
SMS_Y_AXIS	SMS_Y_AXIS - @m38a_lib.M38A	58B7 59B6
	NC_SMS_Y_AXIS - @m38a_lib.M38A	59B5
SMS_Z_AXIS	SMS_Z_AXIS - @m38a_lib.M38A	58A7 59B6
	NC_SMS_Z_AXIS - @m38a_lib.M38A	59B5
SPARE_SRC3_N	SPARE_SRC3_N - @m38a_lib.M38A	34D2
SPARE_SRC3_P	SPARE_SRC3_P - @m38a_lib.M38A	34D2
SPARE_SRC7_N	SPARE_SRC7_N - @m38a_lib.M38A	34D2
SPARE_SRC7_P	SPARE_SRC7_P - @m38a_lib.M38A	34D2
SPI_ARB	SPI_ARB - @m38a_lib.M38A	22C6 58D5
SPI_CE_L	SPI_CE_L - @m38a_lib.M38A	22C6 58B5 63C7
SPI_HOLD_L	SPI_HOLD_L - @m38a_lib.M38A	63C4
SPI_SCLK	SPI_SCLK - @m38a_lib.M38A	22C6 58D5 63C7
SPI_SCLK_R	SPI_SCLK_R - @m38a_lib.M38A	63C4
SPI_SI	SPI_SI - @m38a_lib.M38A	22C6 58D5 63C1
SPI_SI_R	SPI_SI_R - @m38a_lib.M38A	63C3
SPI_SO	SPI_SO - @m38a_lib.M38A	22C6 58D5 63C1
SPI_SO_R	SPI_SO_R - @m38a_lib.M38A	63C3
SPI_WP_L	SPI_WP_L - @m38a_lib.M38A	63C4
SPKRAMP_MUTE	SPKRAMP_MUTE - @m38a_lib.M38A	72B5
SPKRAMP_SS	SPKRAMP_SS - @m38a_lib.M38A	72B4
SUS_CLK_SB	SUS_CLK_SB - @m38a_lib.M38A	23C3 59B5
	SMC_SUS_CLK - @m38a_lib.M38A	58C5 59B6
SV_SET_UP	SV_SET_UP - @m38a_lib.M38A	23B6 23C3 60C1
SW_RST_BTN_L	SW_RST_BTN_L - @m38a_lib.M38A	5D1 26C6
SW_RST_DEBNC	SW_RST_DEBNC - @m38a_lib.M38A	26C4
SYS_LED_BRT_D	SYS_LED_BRT_D - @m38a_lib.M38A	60B8
SYS_LED_C	SYS_LED_C - @m38a_lib.M38A	60A6
SYS_LED_CTL_B	SYS_LED_CTL_B - @m38a_lib.M38A	60B7
SYS_LED_CTL_C	SYS_LED_CTL_C - @m38a_lib.M38A	60B6
SYS_LED_CTL_D	SYS_LED_CTL_D - @m38a_lib.M38A	60A6
SYS_ONEWIRE	SYS_ONEWIRE - @m38a_lib.M38A	58B7 59B4
SYS_POWERFAIL_L	SYS_POWERFAIL_L - @m38a_lib.M38A	6D8 76D2
SYS_PWRUP_L	SYS_PWRUP_L - @m38a_lib.M38A	6C7
THERM_DX_N	THERM_DX_N - @m38a_lib.M38A	10B5 10C5
THERM_DX_P	THERM_DX_P - @m38a_lib.M38A	10B5 10C5
THRM_ALERT_L	THRM_ALERT_L - @m38a_lib.M38A	10D3
THRM_THM	THRM_THM - @m38a_lib.M38A	10C4
TMDS_CK_TERM	TMDS_CK_TERM - @m38a_lib.M38A	97C8
TMDS_CLK_N	TMDS_CLK_N - @m38a_lib.M38A	93C3 97C8
TMDS_CLK_P	TMDS_CLK_P - @m38a_lib.M38A	93C3 97C8
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @m38a_lib.M38A	97C4 97C7
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @m38a_lib.M38A	97C4 97C7
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @m38a_lib.M38A	97C4 97D7
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @m38a_lib.M38A	97C4 97D7
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @m38a_lib.M38A	97C7 97D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @m38a_lib.M38A	97C4 97D7
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @m38a_lib.M38A	97C4 97D7
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @m38a_lib.M38A	97C7 97D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @m38a_lib.M38A	93C3 97D8
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @m38a_lib.M38A	93C3 97D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @m38a_lib.M38A	93C3 97C8
TMDS_DATA_N<3>	TMDS_DATA_N<3> - @m38a_lib.M38A	93C3 95D6
TMDS_DATA_N<4>	TMDS_DATA_N<4> - @m38a_lib.M38A	93C3 95D6
TMDS_DATA_N<5>	TMDS_DATA_N<5> - @m38a_lib.M38A	93C3 95D6
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @m38a_lib.M38A	93C3 97D8
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @m38a_lib.M38A	93C3 97C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @m38a_lib.M38A	93C3 97C8
TMDS_DATA_P<3>	TMDS_DATA_P<3> - @m38a_lib.M38A	93C3 95D6
TMDS_DATA_P<4>	TMDS_DATA_P<4> - @m38a_lib.M38A	93C3 95D6
TMDS_DATA_P<5>	TMDS_DATA_P<5> - @m38a_lib.M38A	93C3 95D6
TPM_BADD	TPM_BADD - @m38a_lib.M38A	67C4
TPM_GPIO1	TPM_GPIO1 - @m38a_lib.M38A	59B5 67C6
TPM_GPIO2	TPM_GPIO2 - @m38a_lib.M38A	59B5 67C6
TPM_LRESET_L	TPM_LRESET_L - @m38a_lib.M38A	6B7 67B7
TPM_PP	TPM_PP - @m38a_lib.M38A	59A5 67C6
TPM_RST_L	TPM_RST_L - @m38a_lib.M38A	67B6
TPM_XTALI	TPM_XTALI - @m38a_lib.M38A	59B7 67C6
TPM_XTALO	TPM_XTALO - @m38a_lib.M38A	59B7 67C6
TP_ATI_ROMCS_L	TP_ATI_ROMCS_L - @m38a_lib.M38A	91A3
TP_AZ_DOCK_EN_L	TP_AZ_DOCK_EN_L - @m38a_lib.M38A	23C5
TP_AZ_DOCK_RST_L	TP_AZ_DOCK_RST_L - @m38a_lib.M38A	23C5
TP_CLK14P3M_SPARE	TP_CLK14P3M_SPARE - @m38a_lib.M38A	34C4
TP_CPU_A32_L	TP_CPU_A32_L - @m38a_lib.M38A	7C7
TP_CPU_A33_L	TP_CPU_A33_L - @m38a_lib.M38A	7B7
TP_CPU_A34_L	TP_CPU_A34_L - @m38a_lib.M38A	7B7
TP_CPU_A35_L	TP_CPU_A35_L - @m38a_lib.M38A	7B7
TP_CPU_A36_L	TP_CPU_A36_L - @m38a_lib.M38A	7B7
TP_CPU_A37_L	TP_CPU_A37_L - @m38a_lib.M38A	7B7
TP_CPU_A38_L	TP_CPU_A38_L - @m38a_lib.M38A	7B7
TP_CPU_A39_L	TP_CPU_A39_L - @m38a_lib.M38A	7B7
TP_CPU_APM0_L	TP_CPU_APM0_L - @m38a_lib.M38A	7B7
TP_CPU_APM1_L	TP_CPU_APM1_L - @m38a_lib.M38A	7B7
TP_CPU_CPUSLP_L	TP_CPU_CPUSLP_L - @m38a_lib.M38A	21C4
TP_CPU_EXTBREF	TP_CPU_EXTBREF - @m38a_lib.M38A	7B6
TP_CPU_HFPLL	TP_CPU_HFPLL - @m38a_lib.M38A	7B7
TP_CPU_SPARE0	TP_CPU_SPARE0 - @m38a_lib.M38A	7B6
TP_CPU_SPARE1	TP_CPU_SPARE1 - @m38a_lib.M38A	7B6
TP_CPU_SPARE2	TP_CPU_SPARE2 - @m38a_lib.M38A	7B6
TP_CPU_SPARE3	TP_CPU_SPARE3 - @m38a_lib.M38A	7B6
TP_CPU_SPARE4	TP_CPU_SPARE4 - @m38a_lib.M38A	7B6
TP_CPU_SPARE5	TP_CPU_SPARE5 - @m38a_lib.M38A	7B6
TP_CPU_SPARE6	TP_CPU_SPARE6 - @m38a_lib.M38A	7B6
TP_CPU_SPARE7	TP_CPU_SPARE7 - @m38a_lib.M38A	7B6
TP_FB_A_MA12	TP_FB_A_MA12 - @m38a_lib.M38A	87D5
TP_FB_A_ODT<0>	TP_FB_A_ODT<0> - @m38a_lib.M38A	87B5
TP_FB_A_ODT<1>	TP_FB_A_ODT<1> - @m38a_lib.M38A	87B5
TP_FB_B_MA12	TP_FB_B_MA12 - @m38a_lib.M38A	87D1
TP_FB_B_ODT<0>	TP_FB_B_ODT<0> - @m38a_lib.M38A	87B1
TP_FB_B_ODT<1>	TP_FB_B_ODT<1> - @m38a_lib.M38A	87B1
TP_FW_CNA	TP_FW_CNA - @m38a_lib.M38A	44B3
TP_FW_LKON	TP_FW_LKON - @m38a_lib.M38A	44B3
TP_FW_LPS	TP_FW_LPS - @m38a_lib.M38A	44B3
TP_FW_MPCIACT_L	TP_FW_MPCIACT_L - @m38a_lib.M38A	44B3
TP_FW_NANDTREE	TP_FW_NANDTREE - @m38a_lib.M38A	44B3
TP_FW_ROM_AD	TP_FW_ROM_AD - @m38a_lib.M38A	44B3
TP_FW_VAUX_PRES	TP_FW_VAUX_PRES - @m38a_lib.M38A	44B3
TP_LVDS_VBG	TP_LVDS_VBG - @m38a_lib.M38A	13D5
TP_MEM_A_A<14>	TP_MEM_A_A<14> - @m38a_lib.M38A	28C3
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @m38a_lib.M38A	28C3
TP_MEM_B_A<14>	TP_MEM_B_A<14> - @m38a_lib.M38A	5B4 29C3
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @m38a_lib.M38A	5B4 29C3

TP_NB_TESTIN_L	TP_NB_TESTIN_L - @m38a_lib.M38A	14D6
TP_NB_XOR_FSB2_H7	TP_NB_XOR_FSB2_H7 - @m38a_lib.M38A	14D6
TP_NB_XOR_LVDS_A34	TP_NB_XOR_LVDS_A34 - @m38a_lib.M38A	14C6
TP_NB_XOR_LVDS_A35	TP_NB_XOR_LVDS_A35 - @m38a_lib.M38A	14C6
TP_NB_XOR_LVDS_D27	TP_NB_XOR_LVDS_D27 - @m38a_lib.M38A	14C6
TP_NB_XOR_LVDS_D28	TP_NB_XOR_LVDS_D28 - @m38a_lib.M38A	14C6
TP_PCI_CLK_SPARE	TP_PCI_CLK_SPARE - @m38a_lib.M38A	5B4 34C4
TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m38a_lib.M38A	22B6
TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m38a_lib.M38A	22B6
TP_PCI_GNT3_L	TP_PCI_GNT3_L - @m38a_lib.M38A	22B6
TP_PCI_GNT4_L	TP_PCI_GNT4_L - @m38a_lib.M38A	22B6
TP_PCI_PME_L	TP_PCI_PME_L - @m38a_lib.M38A	22A6
TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m38a_lib.M38A	21C6
TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m38a_lib.M38A	21C6
TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m38a_lib.M38A	21D4
TP_SB_GPIO6	TP_SB_GPIO6 - @m38a_lib.M38A	23C5
TP_SB_GPIO23	TP_SB_GPIO23 - @m38a_lib.M38A	21D5
TP_SB_GPIO25_DO_NOT_USE	TP_SB_GPIO25_DO_NOT_USE - @m38a_lib.M38A	23C3
TP_SB_GPIO38	TP_SB_GPIO38 - @m38a_lib.M38A	23C3
TP_SB_RSVD9	TP_SB_RSVD9 - @m38a_lib.M38A	22A6
TP_SB_SATALED_L	TP_SB_SATALED_L - @m38a_lib.M38A	21C6
TP_SB_XOR_AD5	TP_SB_XOR_AD5 - @m38a_lib.M38A	22A7
TP_SB_XOR_AD9	TP_SB_XOR_AD9 - @m38a_lib.M38A	22A7
TP_SB_XOR_AE5	TP_SB_XOR_AE5 - @m38a_lib.M38A	22A7
TP_SB_XOR_AE9	TP_SB_XOR_AE9 - @m38a_lib.M38A	22A6
TP_SB_XOR_AG4	TP_SB_XOR_AG4 - @m38a_lib.M38A	22A7
TP_SB_XOR_AG8	TP_SB_XOR_AG8 - @m38a_lib.M38A	22A6
TP_SB_XOR_AH4	TP_SB_XOR_AH4 - @m38a_lib.M38A	22A7
TP_SB_XOR_AH8	TP_SB_XOR_AH8 - @m38a_lib.M38A	22A6
TP_SB_XOR_T5	TP_SB_XOR_T5 - @m38a_lib.M38A	21C6
TP_SB_XOR_U3	TP_SB_XOR_U3 - @m38a_lib.M38A	21C6
TP_SB_XOR_U5	TP_SB_XOR_U5 - @m38a_lib.M38A	21C6
TP_SB_XOR_U7	TP_SB_XOR_U7 - @m38a_lib.M38A	21C6
TP_SB_XOR_V3	TP_SB_XOR_V3 - @m38a_lib.M38A	21C6
TP_SB_XOR_V4	TP_SB_XOR_V4 - @m38a_lib.M38A	21C6
TP_SB_XOR_V6	TP_SB_XOR_V6 - @m38a_lib.M38A	21C6
TP_SB_XOR_V7	TP_SB_XOR_V7 - @m38a_lib.M38A	21C6
TP_SB_XOR_W1	TP_SB_XOR_W1 - @m38a_lib.M38A	21C6
TP_SB_XOR_W3	TP_SB_XOR_W3 - @m38a_lib.M38A	21C6
TP_SB_XOR_Y1	TP_SB_XOR_Y1 - @m38a_lib.M38A	21C6
TP_SB_XOR_Y2	TP_SB_XOR_Y2 - @m38a_lib.M38A	21C6
TP_U8400_AG14	TP_U8400_AG14 - @m38a_lib.M38A	91A5
TP_U8900_J2	TP_U8900_J2 - @m38a_lib.M38A	89A7
TP_U8900_J3	TP_U8900_J3 - @m38a_lib.M38A	89A7
TP_U8950_J2	TP_U8950_J2 - @m38a_lib.M38A	89A4
TP_U8950_J3	TP_U8950_J3 - @m38a_lib.M38A	89A4
TP_U9000_J2	TP_U9000_J2 - @m38a_lib.M38A	90A7
TP_U9000_J3	TP_U9000_J3 - @m38a_lib.M38A	90A7
TP_U9050_J2	TP_U9050_J2 - @m38a_lib.M38A	90A4
TP_U9050_J3	TP_U9050_J3 - @m38a_lib.M38A	90A4
TSENSE_GPU_DXP	TSENSE_GPU_DXP - @m38a_lib.M38A	61C5
TSENSE_NB_DXP	TSENSE_NB_DXP - @m38a_lib.M38A	61B5
TSENSE_NB_GPU_DXN	TSENSE_NB_GPU_DXN - @m38a_lib.M38A	61B5
TV_DACA_OUT	TV_DACA_OUT - @m38a_lib.M38A	13C5 19B1
	TV_DACB_OUT - @m38a_lib.M38A	13C5 19B1
	TV_DACC_OUT - @m38a_lib.M38A	13C5 19B1
	TV_IRTNA - @m38a_lib.M38A	13C5 19B1
	TV_IRTNB - @m38a_lib.M38A	13C5 19B1
	TV_IRTNC - @m38a_lib.M38A	13C5 19B1
	TV_IREF - @m38a_lib.M38A	13C5 19B1
	PP3V3_S0_NB_VCCA_TVBG - @m38a_lib.M38A	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACC - @m38a_lib.M38A	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACB - @m38a_lib.M38A	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACA - @m38a_lib.M38A	17C6 19B1
	PP1V5_S0_NB_VCCD_TVDAC - @m38a_lib.M38A	17C6 19B1
	PP1V5_S0_NB_VCCD_QTVDAC - @m38a_lib.M38A	17B6 19A1
	=PP1V5_S0_AIRPORT - @m38a_lib.M38A	6C4 53D3
	PP1V5_S0 - @m38a_lib.M38A	6C6 11A7 11B7 11B7 80C2
	=PP1V5_S0_SB - @m38a_lib.M38A	6C4 25A8 25C8
	=PP1V5_S0_SB_VCC1_5_A - @m38a_lib.M38A	6C4 24A3 25C1
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m38a_lib.M38A	6C4 24A3 25B1
	=PP1V5_S0_SB_VCCUSBPLL - @m38a_lib.M38A	6C4 24A5 25B6
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m38a_lib.M38A	6C4 24A5 25C6
	=PP1V5_S0_SB_VCCSATAPLL - @m38a_lib.M38A	6C4 24B5 25D6
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m38a_lib.M38A	6C4 24B5 25D6
	=PP1V5_S0_NB_3GPLL - @m38a_lib.M38A	6C4 19A6 19A6
	=PP1V5_S0_NB_PLL - @m38a_lib.M38A	6C4 19C8 19D7
	=PP1V5_S0_NB_VCCAUX - @m38a_lib.M38A	6C4 6C4 16D1 17B6 19A7
	=PP1V5_S0_NB_VCCD_HMPLL - @m38a_lib.M38A	6C4 17C6 19D7
	=PP1V5_S0_NB_PCIE - @m38a_lib.M38A	6C4 13D2 19D7
	=PP1V5_S0_CPU - @m38a_lib.M38A	6C4 8B6 8C5

	@m38a_lib.M38A	
	=PP1V5_S0_SB_VCC1_5_A - @m38a_lib.M38A	6C4 24A3 25C1
	@m38a_lib.M38A	
	=PP1V5_S0_SB - @m38a_lib.M38A	6C4 25A8 25C8
	=PP1V5_S0_NB_VCCD_HMPLL - @m38a_lib.M38A	6C4 17C6 19D7
	@m38a_lib.M38A	
	=PP1V5_S0_NB_VCCAUX - @m38a_lib.M38A	6C4 6C4 16D1 17B6 19A7
	@m38a_lib.M38A	19D7
	=PP1V5_S0_NB_TVDAC - @m38a_lib.M38A	6C4 19B2 19D7
	=PP1V5_S0_NB_PLL - @m38a_lib.M38A	6C4 19C8 19D7
	=PP1V5_S0_NB_PCIE - @m38a_lib.M38A	6C4 13D2 19D7
	=PP1V5_S0_NB_3GPLL - @m38a_lib.M38A	6C4 19A6 19A6
	=PP1V5_S0_NB - @m38a_lib.M38A	6C4 19B2 19D7
	=PP1V5_S0_CPU - @m38a_lib.M38A	6C4 8B6 8C5
	=PP1V5_S0_AIRPORT - @m38a_lib.M38A	6C4 53D3
U600_3	U600_3 - @m38a_lib.M38A	6C7
U600_6	U600_6 - @m38a_lib.M38A	6B7
U600_8	U600_8 - @m38a_lib.M38A	6B7
U600_11	U600_11 - @m38a_lib.M38A	6B7
U650_4	U650_4 - @m38a_lib.M38A	6A6
U2698_4	U2698_4 - @m38a_lib.M38A	26C4
U3100_VDDQ	U3100_VDDQ - @m38a_lib.M38A	31C5
U6100_VCC	U6100_VCC - @m38a_lib.M38A	61C4
U7400_CEXT	U7400_CEXT - @m38a_lib.M38A	74C4
U8595_1	U8595_1 - @m38a_lib.M38A	85D2
USB_A_N	USB_A_N - @m38a_lib.M38A	22C2 47D6
USB_A_OC_L	USB_A_OC_L - @m38a_lib.M38A	22C4 22D8 47B7
USB_A_P	USB_A_P - @m38a_lib.M38A	22C2 47C6
USB_B_N	USB_B_N - @m38a_lib.M38A	22C2 53B2
USB_B_OC_L	USB_B_OC_L - @m38a_lib.M38A	22C4 22D8
USB_B_P	USB_B_P - @m38a_lib.M38A	22C2 53B2
USB_CAMERA_N	USB_CAMERA_N - @m38a_lib.M38A	47B2
USB_CAMERA_P	USB_CAMERA_P - @m38a_lib.M38A	47B2
USB_C_N	USB_C_N - @m38a_lib.M38A	22C2 47B6
USB_C_OC_L	USB_C_OC_L - @m38a_lib.M38A	22C4 22D8 47B7
USB_C_P	USB_C_P - @m38a_lib.M38A	22C2 47B6
USB_D_N	USB_D_N - @m38a_lib.M38A	22C2 47B3
USB_D_OC_L	USB_D_OC_L - @m38a_lib.M38A	22C4 22D8
USB_D_P	USB_D_P - @m38a_lib.M38A	22C2 47B3
USB_E_N	USB_E_N - @m38a_lib.M38A	22C2 47A6
USB_E_OC_L	USB_E_OC_L - @m38a_lib.M38A	22C4 22D8 47B7
USB_E_P	USB_E_P - @m38a_lib.M38A	22C2 47A6
USB_F_N	USB_F_N - @m38a_lib.M38A	22C2
USB_F_P	USB_F_P - @m38a_lib.M38A	22C2
USB_G_N	USB_G_N - @m38a_lib.M38A	22C2 47A3
	USB_BT_N - @m38a_lib.M38A	47A2
USB_G_P	USB_G_P - @m38a_lib.M38A	22C2 47A3
	USB_BT_P - @m38a_lib.M38A	47A2
USB_H_N	USB_H_N - @m38a_lib.M38A	22C2 47C3
USB_H_P	USB_H_P - @m38a_lib.M38A	22C2 47C3
USB_IR_N	USB_IR_N - @m38a_lib.M38A	47C2
USB_IR_P	USB_IR_P - @m38a_lib.M38A	47C2
USB_PORT0_N	USB_PORT0_N - @m38a_lib.M38A	47D5
USB_PORT0_P	USB_PORT0_P - @m38a_lib.M38A	47C5
USB_PORT1_N	USB_PORT1_N - @m38a_lib.M38A	47B5
USB_PORT1_P	USB_PORT1_P - @m38a_lib.M38A	47B5
USB_PORT2_N	USB_PORT2_N - @m38a_lib.M38A	47A5
USB_PORT2_P	USB_PORT2_P - @m38a_lib.M38A	47A5
USB_RBIAS_PN	USB_RBIAS_PN - @m38a_lib.M38A	22C2
VGA_B	VGA_B - @m38a_lib.M38A	97B6 97C5
VGA_G	VGA_G - @m38a_lib.M38A	97A6 97C5
VGA_HSYNC	VGA_HSYNC - @m38a_lib.M38A	97A3 97C5
VGA_R	VGA_R - @m38a_lib.M38A	97A6 97C5
VGA_VSYNC	VGA_VSYNC - @m38a_lib.M38A	97B3 97C5
VMAIN_AVLBL	VMAIN_AVLBL - @m38a_lib.M38A	41C7
VREG_FB	VREG_FB - @m38a_lib.M38A	68A3
VR_PWRGD_CK410	VR_PWRGD_CK410 - @m38a_lib.M38A	23C5 26A8
VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m38a_lib.M38A	5C7 14B6 26D5 75C6
XDP_BPM_L<0>	XDP_BPM_L<0> - @m38a_lib.M38A	7C6 11B3
XDP_BPM_L<1>	XDP_BPM_L<1> - @m38a_lib.M38A	7C6 11B3
XDP_BPM_L<2>	XDP_BPM_L<2> - @m38a_lib.M38A	7C6 11B3
XDP_BPM_L<3>	XDP_BPM_L<3> - @m38a_lib.M38A	7C6 11B3
XDP_BPM_L<4>	XDP_BPM_L<4> - @m38a_lib.M38A	7C6 11B3
XDP_BPM_L<5>	XDP_BPM_L<5> - @m38a_lib.M38A	7C6 11B1 11B3
XDP_DBRESET_L	XDP_DBRESET_L - @m38a_lib.M38A	7C6 11B4 26B5
XDP_TCK	XDP_TCK - @m38a_lib.M38A	5D1 7A8 7C6 11B3 11B3
XDP_TDI	XDP_TDI - @m38a_lib.M38A	5D1 7B8 7C6 11B3
XDP_TDO	XDP_TDO - @m38a_lib.M38A	5D1 7C6 11B5
XDP_TMS	XDP_TMS - @m38a_lib.M38A	5D1 7B8 7C6 11B3
XDP_TRST_L	XDP_TRST_L - @m38a_lib.M38A	5D1 7C6 11B3
ZH701P1	ZH701P1 - @m38a_lib.M38A	6A3
ZH702P1	ZH702P1 - @m38a_lib.M38A	6A3
ZH703P1	ZH703P1 - @m38a_lib.M38A	6A3
ZH704P1	ZH704P1 - @m38a_lib.M38A	6B3

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C1972	CAP_805-1	m38a[19A4]
C1975	CAP_805-1	m38a[19A4]
C1976	CAP_402	m38a[19A4]
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C1982	CAP_603	m38a[19B8]
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C5311	CAP_805-1	m38a[53C3]
C5312	CAP_805-1	m38a[53D4]
C5313	CAP_402	m38a[53C5]
C5314	CAP_805-1	m38a[53C4]
C5800	CAP_402	m38a[59B8]
C5801	CAP_402	m38a[59B8]
C5802	CAP_805	m38a[58D3]
C5803	CAP_402	m38a[58D2]
C5804	CAP_402	m38a[58D2]
C5805	CAP_402	m38a[58D2]
C5806	CAP_402	m38a[58D1]
C5807	CAP_402	m38a[58D2]
C5820	CAP_402	m38a[58C3]
C5900	CAP_402	m38a[59D8]
C5901	CAP_402	m38a[59D8]
C5902	CAP_402	m38a[59B7]
C5903	CAP_402	m38a[59A8]
C5919	CAP_402	m38a[59B4]
C5940	CAP_402	m38a[59A4]
C5941	CAP_402	m38a[59A3]
C5942	CAP_805-1	m38a[59A3]
C5943	CAP_402	m38a[59A5]
C5951	CAP_402	m38a[60B6]
C6000	CAP_402	m38a[60D4]
C6001	CAP_402	m38a[60D4]
C6002	CAP_402	m38a[60D4]
C6003	CAP_402	m38a[60D4]
C6100	CAP_402	m38a[61B5]
C6101	CAP_402	m38a[61B5]
C6301	CAP_402	m38a[63C2]
C6308	CAP_402	m38a[63C5]
C6309	CAP_402	m38a[63C6]
C6311	CAP_402	m38a[63C2]
C6312	CAP_402	m38a[63D3]
C6500	CAP_603	m38a[65D5]
C6501	CAP_805	m38a[65D5]
C6502	CAP_603	m38a[65B4]
C6503	CAP_805	m38a[65B5]
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C6505	CAP_P_6.3X11-TH-LF1	m38a[65B3]
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C6601	CAP_805	m38a[66C5]
C6602	CAP_P_SM-LF	m38a[66C3]
C6650	CAP_402	m38a[66B5]
C6651	CAP_402	m38a[66A5]
C6652	CAP_402	m38a[66B3]
C6653	CAP_402	m38a[66A3]
C6654	CAP_402	m38a[66B4]
C6655	CAP_402	m38a[66B2]
C6700	CAP_402	m38a[67C4]
C6701	CAP_402	m38a[67C4]
C6702	CAP_402	m38a[67C3]
C6703	CAP_402	m38a[67C3]
C6704	CAP_402	m38a[59B7]
C6705	CAP_402	m38a[59B7]
C6800	CAP_603	m38a[68D6]
C6801	CAP_402	m38a[68D6]
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C6803	CAP_P_6.3X5.5-SM	m38a[68D3]
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C6807	CAP_P_SMA-LF	m38a[68B3]
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C6812	CAP_402	m38a[68B4]
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C6821	CAP_402	m38a[68C6]
C6822	CAP_603	m38a[68A5]
C6823	CAP_402	m38a[68A4]
C6825	CAP_402	m38a[68A3]
C6826	CAP_603	m38a[68A2]
C6830	CAP_402	m38a[68D4]
C6833	CAP_402	m38a[68B3]
C6835	CAP_402	m38a[68D6]
C6836	CAP_402	m38a[68D3]
C7200	CAP_P_6.3X8-SM	m38a[72D5]
C7201	CAP_1210	m38a[72D5]
C7202	CAP_805	m38a[72D4]
C7203	CAP_1210	m38a[72D3]
C7204	CAP_805	m38a[72D6]
C7205	CAP_805	m38a[72C6]
C7206	CAP_805	m38a[72C6]
C7207	CAP_805	m38a[72C6]
C7208	CAP_603-1	m38a[72C4]
C7209	CAP_805	m38a[72B4]
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C7212	CAP_402	m38a[72B2]
C7213	CAP_402	m38a[72B2]
C7214	CAP_603	m38a[72B5]
C7215	CAP_402	m38a[72C6]
C7216	CAP_402	m38a[72C6]
C7217	CAP_P_6.3X8-SM	m38a[72D6]
C7218	CAP_603	m38a[72D5]
C7219	CAP_603	m38a[72D4]
C7221	CAP_402	m38a[72B7]
C7223	CAP_1210	m38a[72D3]
C7317	CAP_402	m38a[73B4]
C7318	CAP_805-1	m38a[73B4]
C7326	CAP_402	m38a[73C7]
C7400	CAP_402	m38a[74B4]
C7401	CAP_402	m38a[74D5]
C7402	CAP_402	m38a[74A4]
C7403	CAP_P_6.3X5.5-SM	m38a[74B7]
C7404	CAP_P_6.3X5.5-SM	m38a[74B6]
C7405	CAP_P_SMA-LF	m38a[74C7]
C7406	CAP_P_SMA-LF	m38a[74C6]
C7407	CAP_402	m38a[74D8]
C7408	CAP_402	m38a[74D7]
C7415	CAP_402	m38a[74A8]
C7416	CAP_402	m38a[74A8]
C7417	CAP_402	m38a[74A8]
C7418	CAP_805	m38a[74A5]
C7419	CAP_603-1	m38a[74A4]
C7424	CAP_402	m38a[74C3]
C7435	CAP_P_6.3X8-SM	m38a[74A3]
C7500	CAP_402	m38a[75C4]
C7501	CAP_P_TH-MCZ	m38a[75C2]
C7502	CAP_402	m38a[75B4]
C7503	CAP_402	m38a[75C1]
C7504	CAP_402	m38a[75B1]
C7505	CAP_402	m38a[75C8]
C7506	CAP_402	m38a[75B7]
C7507	CAP_402	m38a[75B7]
C7508	CAP_1210	m38a[75C2]
C7509	CAP_1210	m38a[75D1]
C7510	CAP_402	m38a[75C8]
C7511	CAP_603	m38a[75B2]
C7512	CAP_603	m38a[75C2]
C7513	CAP_402	m38a[75B7]
C7514	CAP_402	m38a[75B8]
C7515	CAP_603	m38a[75C4]
C7516	CAP_402	m38a[75B4]
C7517	CAP_P_SM-3	m38a[75D2]
C7518	CAP_P_SM-3	m38a[75D2]
C7521	CAP_402	m38a[75A6]
C7526	CAP_603	m38a[75D6]
C7527	CAP_603	m38a[75C5]

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C7534	CAP_402	m38a[75B5]
C7535	CAP_603	m38a[75D5]
C7550	CAP_603	m38a[75D1]
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C7592	CAP_402	m38a[75B3]
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C7598	CAP_1210	m38a[75D1]
C7599	CAP_402	m38a[76D6]
C7612	CAP_402	m38a[76B2]
C7633	CAP_402	m38a[76C7]
C7700	CAP_603	m38a[77D2]
C7703	CAP_402	m38a[77C2]
C7704	CAP_402	m38a[77C2]
C7706	CAP_402	m38a[77D2]
C7709	CAP_805	m38a[77D1]
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C7711	CAP_402	m38a[77D5]
C7712	CAP_402	m38a[77D4]
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C7751	CAP_805	m38a[77B5]
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C7753	CAP_402	m38a[77B6]
C7754	CAP_402	m38a[77B6]
C7755	CAP_805	m38a[77B4]
C7756	CAP_805	m38a[77B3]
C7757	CAP_402	m38a[77A7]
C7797	CAP_402	m38a[77B4]
C7798	CAP_603	m38a[77B7]
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C7803	CAP_603	m38a[78B6]
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C7805	CAP_603	m38a[78C4]
C7806	CAP_805-1	m38a[78B2]
C7807	CAP_P_CASE-D2E-LF	m38a[78B3]
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C7810	CAP_402	m38a[78B4]
C7811	CAP_402	m38a[78B5]
C7813	CAP_1206	m38a[78B4]
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C7817	CAP_P_CASE-D2E-LF	m38a[78B2]
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C7901	CAP_603	m38a[79D5]
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C7903	CAP_603	m38a[79C7]
C7906	CAP_402	m38a[79C5]
C7907	CAP_402	m38a[79C3]
C7908	CAP_402	m38a[79C5]
C7909	CAP_1206	m38a[79C4]
C7910	CAP_P_SM-3	m38a[79D4]
C7911	CAP_1210	m38a[79D3]
C7912	CAP_P_CASE-D2E-LF	m38a[79C3]
C7913	CAP_1206	m38a[79C2]
C7980	CAP_402	m38a[79B3]
C7992	CAP_603	m38a[79D6]
C7998	CAP_P_CASE-D2E-LF	m38a[79C3]
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C8004	CAP_1206	m38a[80C4]
C8005	CAP_402	m38a[80C4]
C8006	CAP_402	m38a[80D6]
C8009	CAP_603	m38a[80C6]
C8010	CAP_603	m38a[80C4]
C8011	CAP_402	m38a[80C5]
C8012	CAP_402	m38a[80C5]
C8014	CAP_P_TH-MCZ	m38a[80D4]
C8015	CAP_1210	m38a[80D3]
C8016	CAP_805-1	m38a[80C2]
C8099	CAP_P_CASE-D2E-LF	m38a[80C2]
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C8101	CAP_603	m38a[81C5]
C8102	CAP_402	m38a[81C5]
C8103	CAP_603	m38a[81C7]
C8106	CAP_402	m38a[81C5]
C8107	CAP_402	m38a[81C3]
C8108	CAP_402	m38a[81C5]
C8109	CAP_1206	m38a[81C4]
C8110	CAP_1210	m38a[81D4]
C8111	CAP_1210	m38a[81D3]
C8112	CAP_1210	m38a[81D3]
C8114	CAP_P_CASE-D2E-LF	m38a[81C3]
C8115	CAP_805-1	m38a[81C2]
C8190	CAP_P_CASE-D2E-LF	m38a[81C3]
C8192	CAP_603	m38a[81D6]
C8198	CAP_1210	m38a[81D3]
C8199	CAP_402	m38a[81A5]
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C8399	CAP_603	m38a[83C4]
C8400	CAP_805	m38a[84C7]
C8401	CAP_402	m38a[84C7]
C8402	CAP_402	m38a[84C7]
C8405	CAP_805	m38a[84B7]
C8406	CAP_402	m38a[84B7]
C8407	CAP_402	m38a[84B7]
C8410	CAP_805	m38a[84B6]
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C8599	CAP_1206	m38a[85C4]
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C8715	CAP_402	m38a[87A7]
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C8723	CAP_402	m38a[87B4]
C8725	CAP_402	m38a[87A4]
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C8901	CAP_402	m38a[89D7]
C8902	CAP_402	m38a[89D7]
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C8910	CAP_402	m38a[89D7]
C8915	CAP_402	m38a[89D6]
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C8924	CAP_402	m38a[89C7]
C8925	CAP_402	m38a[89C7]
C8926	CAP_402	m38a[89C6]
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C8933	CAP_402	m38a[89C6]
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C9015	CAP_402	m38a[90D6]
C9020	CAP_805	m38a[90C8]
C9021	CAP_402	m38a[90C8]
C9022	CAP_402	m38a[90C7]
C9023	CAP_402	m38a[90C7]
C9024	CAP_402	m38a[90C7]
C9025	CAP_402	m38a[90C7]
C9026	CAP_402	m38a[90C6]
C9031	CAP_402	m38a[90C7]
C9033	CAP_402	m38a[90C6]
C9050	CAP_805	m38a[90D4]
C9051	CAP_402	m38a[90D4]
C9052	CAP_402	m38a[90D4]
C9053	CAP_402	m38a[90D3]
C9054	CAP_402	m38a[90D3]
C9060	CAP_402	m38a[90D3]
C9065	CAP_402	m38a[90D3]
C9070	CAP_805	m38a[90C5]
C9071	CAP_402	m38a[90C4]
C9072	CAP_402	m38a[90C4]
C9073	CAP_402	m38a[90C4]
C9074	CAP_402	m38a[90C4]
C9075	CAP_402	m38a[90C3]
C9076	CAP_402	m38a[90C3]
C9081	CAP_402	m38a[90C3]
C9083	CAP_402	m38a[90C3]
C9100	CAP_805	m38a[91C5]
C9101	CAP_402	m38a[91C5]
C9102	CAP_402	m38a[91C5]
C9103	CAP_402	m38a[91C5]
C9110	CAP_805	m38a[91C5]
C9111	CAP_402	m38a[91C5]
C9112	CAP_402	m38a[91C5]
C9115	CAP_805	m38a[91B5]
C9116	CAP_402	m38a[91B5]
C9117	CAP_402	m38a[91B5]
C9120	CAP_805	m38a[91B5]
C9121	CAP_402	m38a[91B5]
C9122	CAP_402	m38a[91B5]
C9125	CAP_805	m38a[91B5]
C9126	CAP_402	m38a[91B5]
C9127	CAP_402	m38a[91B5]
C9130	CAP_805	m38a[91A6]
C9131	CAP_402	m38a[91A6]
C9132	CAP_402	m38a[91A5]
C9135	CAP_805	m38a[91A6]
C9136	CAP_402	m38a[91A6]
C9137	CAP_402	m38a[91A5]
C9140	CAP_805	m38a[91A6]
C9141	CAP_402	m38a[91A6]
C9142	CAP_402	m38a[91A5]
C9191	CAP_402	m38a[91D2]
C9300	CAP_805	m38a[93C6]
C9301	CAP_402	m38a[93C6]
C9302	CAP_402	m38a[93C5]
C9305	CAP_805	m38a[93C6]
C9306	CAP_402	m38a[93C6]
C9307	CAP_402	m38a[93C5]
C9310	CAP_805	m38a[93C6]
C9311	CAP_402	m38a[93C6]
C9312	CAP_402	m38a[93C5]
C9315	CAP_805	m38a[93B8]
C9316	CAP_402	m38a[93B8]
C9317	CAP_402	m38a[93B7]
C9320	CAP_805	m38a[93B6]
C9321	CAP_402	m38a[93B6]
C9322	CAP_402	m38a[93B5]
C9325	CAP_805	m38a[93B8]
C9326	CAP_402	m38a[93B8]
C9327	CAP_402	m38a[93B7]
C9330	CAP_805	m38a[93B6]
C9331	CAP_402	m38a[93B6]
C9332	CAP_402	m38a[93B5]
C9340	CAP_805	m38a[93A6]
C9341	CAP_402	m38a[93A6]
C9342	CAP_402	m38a[93A5]
C9345	CAP_805	m38a[93A6]
C9346	CAP_402	m38a[93A5]
C9347	CAP_402	m38a[93A5]
C9400	CAP_603-1	m38a[94C7]
C9401	CAP_402	m38a[94C6]
C9410	CAP_402	m38a[94C6]
C9420	CAP_1210	m38a[94C5]
C9450	CAP_805	m38a[94C2]
C9470	CAP_402	m38a[94B2]
C9700	CAP_402	m38a[97C8]
C9710	CAP_603	m38a[97C3]
C9711	CAP_402	m38a[97D3]
C9713	CAP_402	m38a[97C2]
C9714	CAP_402	m38a[97C2]
C9740	CAP_402	m38a[97A7]
C9741	CAP_402	m38a[97A6]
C9742	CAP_402	m38a[97A6]
C9750	CAP_402	m38a[97B4]
C9751	CAP_402	m38a[97A4]
D2500	DIODE_SCHOT_SOT23	m38a[25C8]
D2501	DIODE_SCHOT_SOT23	m38a[25D8]
D2600	DIODE_SCHOT_SOT23	m38a[26D8]
D2601	DIODE_SCHOT_SOT23	m38a[26C8]
D4600	DIODE_SMC	m38a[46D5]
D4690	ZENER_SOT23	m38a[46A6]
D4700	DIODE_SCHOT_3P_A_SC-75	m38a[47C4]
D4701	DIODE_SCHOT_3P_A_SC-75	m38a[47B4]
D4702	DIODE_SCHOT_3P_A_SC-75	m38a[47A4]
D6500	DIODE_SOT23	m38a[65C4]
D6501	DIODE_SOT23	m38a[65B4]
D6502	DIODE_SCHOT_SMB	m38a[65C4]
D6503	DIODE_SCHOT_SMB	m38a[65B4]
D6600	DIODE_SOT23	m38a[66C4]
D6601	DIODE_SCHOT_SMB	m38a[66C3]
D7500	DIODE_SCHOT_SMB	m38a[75C3]
D7501	DIODE_SCHOT_SMB	m38a[75B2]
D7599	DIODE_SOT23	m38a[76D6]
D8520	DIODE_SCHOT_SMB	m38a[85C3]
D9700	ZENER_CASE425	m38a[97C1]
DP4610	DIODE_DUAL_6P_SOT-363	m38a[46D4 46D3]
DP4611	DIODE_DUAL_6P_SOT-363	m38a[46C4 46C3]
DP4620	DIODE_DUAL_6P_SOT-363	m38a[46B4 46B3]
DP4621	DIODE_DUAL_6P_SOT-363	m38a[46A4 46A3]
DZ4700	DIODE_SCHOT_POWERDI-123	m38a[47C8]
DZ6800	DIODE_SCHOT_POWERDI-123	m38a[68A4]
DZ7300	SUPPR_TRANSIENT1_402	m38a[73C6]
DZ7301	SUPPR_TRANSIENT1_402	m38a[73C5]
DZ7302	SUPPR_TRANSIENT1_402	m38a[73C6]
DZ7311	SUPPR_TRANSIENT1_402	m38a[73A7]
DZ7313	SUPPR_TRANSIENT1_402	m38a[73A6]
DZ7314	SUPPR_TRANSIENT1_402	m38a[73A6]
DZ7315	SUPPR_TRANSIENT1_402	m38a[73A6]
DZ7323	SUPPR_TRANSIENT1_402	m38a[73A5]
DZ7324	SUPPR_TRANSIENT1_402	m38a[73C5]
DZ7325	SUPPR_TRANSIENT1_402	m38a[73C3]
DZ7326	SUPPR_TRANSIENT1_402	m38a[73C3]
DZ7380	SUPPR_TRANSIENT1_402	m38a[73A7]
F4602	FUSE_MINISMD-LF	m38a[46D3]
F4701	FUSE_MINISMD-LF	m38a[47D3]
F9710	FUSE_SM-LF	m38a[97D5]
FL4610	FILTER_4P_2012	m38a[46C3]
FL4620	FILTER_4P_2012	m38a[46B3]
FL9740	FILTER_LC_SM-220MHZ-LF	m38a[97B7]
FL9741	FILTER_LC_SM-220MHZ-LF	m38a[97A7]
FL9742	FILTER_LC_SM-220MHZ-LF	m38a[97A7]
FLE011	FILTER_4P_2012	m38a[46C3]
FLE021	FILTER_4P_2012	m38a[46B3]
GV3801	HOLE_VIA	m38a[38A8]
GV3802	HOLE_VIA	m38a[38A7]
GV3803	HOLE_VIA	m38a[38A8]
GV3804	HOLE_VIA	m38a[38A7]
GV3805	HOLE_VIA	m38a[38A8]
GV3806	HOLE_VIA	m38a[38A7]
GV3807	HOLE_VIA	m38a[38A8]
GV3808	HOLE_VIA	m38a[38A7]
J3	CON_2RTSM_125_SM-2MT-BLK-LF	m38a[61B6]
J600	CON_M12RT_D_THA_M-RT-TH	m38a[6D7]
J0700	CPU_YONAH_SKT_BGA	m38a[7C3 7D7]
J0700	CPU_YONAH_SKT_BGA	m38a[8D4 8D8]
J1000	CON_2RTSM_125_SM-2MT-BLK-LF	m38a[10B7]
J1101	CON_F28RT_S2MT_SM_F-RT-SM	m38a[11C2]
J2600	BATTERY_2P_SM	m38a[26C8]
J2800	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m38a[28D5]
J2900	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m38a[29D5]
J2901	CON_F4ST_S2MT_SM_F-ST-SM	m38a[59C7]
J2903	CON_M2ST_S2MT_SM_M-ST-SM	m38a[59C8]
J4700	CON_F10ST_D_SMA_F-SM	m38a[47B1]
J5300	CON_F52RT_D2MT_SM_F-RT-SM	m38a[53C5]
J6000	CON_F30STSM_5047_SM1	m38a[60C3]
J6500	CON_M4RT_S2MT_SM_M-RT-SM	m38a[65D3]
J6501	CON_M5RT_S2MT_SMA_M-RT-SM	m38a[65B2]
J6600	CON_F4ST_S2MT_SM_F-ST-SM	m38a[66C2]
J6601	CON_M4RT_S2MT_SM_M-RT-SM	m38a[66B5]
J6602	CON_M4RT_S2MT_SM_M-RT-SM	m38a[66B3]
J7300	CON_F9ANG_4MT_OPTAUD_JCK_TH1_F-5.5-DEG-TH	m38a[73D8]

J7301	CON_M7RT_S2MT_SM_M-R-T-SM	m38a[73D1]
J7303	CON_F9ANG_S4MT_TH1_F-ANG-TH	m38a[73B3]
J9401	CON_M4ST_S_SM_M-ST-SM	m38a[94C2]
J9402	CON_F30ST_D_SM_F-ST-SM	m38a[94B6]
J9710	CON_DVI_F32ST_Q2MT_SM_F-ST-SM4	m38a[97D5]
JC900	CON_M7ST_SATA_SM_M-ST-SM	m38a[38B8]
JC901	CON_F50ST_D2MT_SM_F-ST-SM	m38a[38D2]
JD600	CON_RJ45_10ANG_S3MT_TH1_F-ANG-TH	m38a[43C6]
JE000	CON_F6ST_S4MT_TH1_F-ST-TH	m38a[46C2]
JE001	CON_F6ST_S4MT_TH1_F-ST-TH	m38a[46B2]
JE310	CON_F4ST_USB_S3MT_TH_F-ST-TH	m38a[47D4]
JE320	CON_F4ST_USB_S3MT_TH_F-ST-TH	m38a[47B4]
JE330	CON_F4ST_USB_S3MT_TH_F-ST-TH	m38a[47A4]
JE350	CON_M14RT_S2MT_SM_M-RT-SM	m38a[47C1]
L1934	IND_0603	m38a[19C7]
L1936	IND_0603	m38a[19C7]
L1970	IND_1210	m38a[19A5]
L1975	IND_0805	m38a[19A5]
L2500	IND_SM-3	m38a[25B8]
L2507	IND_1206	m38a[25A7]
L3301	IND_0402-LF	m38a[33D7]
L3302	IND_0402-LF	m38a[33D3]
L4200	IND_0805	m38a[42D7]
L4201	IND_0805	m38a[42B7]
L4300	IND_SM	m38a[43D7]
L4409	IND_0402	m38a[44D6]
L4610	IND_1206-LF	m38a[46D2]
L4620	IND_1206-LF	m38a[46B2]
L4690	IND_SM-1	m38a[46A6]
L4710	IND_SM	m38a[47D5]
L4712	FILTER_4P_2012	m38a[47C5]
L4720	IND_SM	m38a[47C5]
L4722	FILTER_4P_2012	m38a[47B5]
L4730	IND_SM	m38a[47B5]
L4732	FILTER_4P_2012	m38a[47A5]
L4740	IND_SM	m38a[47D2]
L4742	FILTER_4P_2012	m38a[47C2]
L4752	FILTER_4P_2012	m38a[47B2]
L6800	IND_0402-LF	m38a[68A5]
L6801	IND_0402-LF	m38a[68D6]
L7200	IND_SM-1	m38a[72D6]
L7201	IND_0603-LF	m38a[72C2]
L7202	IND_0603-LF	m38a[72C2]
L7203	IND_0603-LF	m38a[72C3]
L7204	IND_0603-LF	m38a[72C3]
L7205	IND_0603	m38a[72D6]
L7206	IND_0603	m38a[72C6]
L7207	IND_0603	m38a[72C6]
L7208	IND_0603	m38a[72C6]
L7300	IND_0603-LF	m38a[73D6]
L7301	IND_0603-LF	m38a[73D6]
L7302	IND_0603-LF	m38a[73D6]
L7303	IND_0603-LF	m38a[73D6]
L7304	IND_0603-LF	m38a[73D5]
L7305	IND_0603-LF	m38a[73D5]
L7306	IND_0603-LF	m38a[73D5]
L7307	IND_0603-LF	m38a[73D5]
L7309	IND_0603-LF	m38a[73C4]
L7310	IND_0603-LF	m38a[73C4]
L7312	IND_0603-LF	m38a[73C3]
L7313	IND_0603-LF	m38a[73C3]
L7315	IND_0603-LF	m38a[73B7]
L7316	IND_0603-LF	m38a[73B7]
L7317	IND_0603-LF	m38a[73A7]
L7318	IND_0603-LF	m38a[73B7]
L7319	IND_0603-LF	m38a[73B7]
L7323	IND_0603-LF	m38a[73B5]
L7324	IND_0603-LF	m38a[73B5]
L7325	IND_0603-LF	m38a[73A5]
L7326	IND_0603-LF	m38a[73B5]
L7327	IND_0603-LF	m38a[73B5]
L7381	IND_0603-LF	m38a[73A5]
L7500	IND_SM	m38a[75D1]
L7501	IND_SM	m38a[75B2]
L7502	IND_TH-VERT-LF	m38a[76D8]
L7700	IND_SM1-LF	m38a[77D2]
L7750	IND_SM-LF	m38a[77B4]
L7800	IND_3P_SM	m38a[78B3]
L7880	IND_0603-LF	m38a[73A7]
L7900	IND_3P_SM	m38a[79C3]
L8000	IND_3P_SM	m38a[80C3]
L8100	IND_IHLP	m38a[81C3]
L8400	IND_0402	m38a[84B7]
L8520	IND_IHLP	m38a[85C3]
L8715	IND_0402	m38a[87A7]
L8725	IND_0402	m38a[87A4]
L8910	IND_0402	m38a[89D7]
L8915	IND_0402	m38a[89D7]
L8960	IND_0402	m38a[89D4]
L8965	IND_0402	m38a[89D4]
L9010	IND_0402	m38a[90D7]
L9015	IND_0402	m38a[90D7]
L9060	IND_0402	m38a[90D4]
L9065	IND_0402	m38a[90D4]
L9120	IND_0402	m38a[91B6]
L9125	IND_0402	m38a[91B6]
L9130	IND_0402	m38a[91B7]
L9135	IND_0402	m38a[91A7]
L9140	IND_0402	m38a[91A7]
L9300	IND_0402	m38a[93C7]
L9305	IND_0402	m38a[93C7]
L9310	IND_0402	m38a[93C7]
L9315	IND_0402	m38a[93C7]
L9320	IND_0402	m38a[93B7]
L9325	IND_0402	m38a[93B7]
L9330	IND_0402	m38a[93B7]
L9345	IND_0402	m38a[93B7]
L9400	IND_SM	m38a[94C6]
L9700	FILTER_4P_2012H	m38a[97D7]
L9701	FILTER_4P_2012H	m38a[97D7]
L9702	FILTER_4P_2012H	m38a[97C7]
L9703	FILTER_4P_SM-LF	m38a[97C7]
L9710	IND_SM-1	m38a[97D5]
LED601	LED_2.0X1.25MM-SM	m38a[6A8]
LED602	LED_2.0X1.25MM-SM	m38a[6A7]
LED603	LED_2.0X1.25MM-SM	m38a[6A6]
LED3800	LED_2.0X1.25MM-SM	m38a[38B3]
LED5950	LED_3X2MM-SM	m38a[60A6]
LED6000	LED_NS3W315_ST-SM	m38a[60A6]
LED7900	LED_2.0X1.25MM-SM	m38a[79A4]
LED8000	LED_2.0X1.25MM-SM	m38a[80A4]
LED8100	LED_2.0X1.25MM-SM	m38a[81A4]
PP5E1	PROBEPOINT_SM	m38a[5B8]
PP5E2	PROBEPOINT_SM	m38a[5B8]
PP6A0	PROBEPOINT_SM	m38a[5A6]
PP6A1	PROBEPOINT_SM	m38a[5A6]
PP6A2	PROBEPOINT_SM	m38a[5A6]
PP6A3	PROBEPOINT_SM	m38a[5A6]
PP6A4	PROBEPOINT_SM	m38a[5A6]
PP6A5	PROBEPOINT_SM	m38a[5A6]
PP6A6	PROBEPOINT_SM	m38a[5A6]
PP6A7	PROBEPOINT_SM	m38a[5A6]
PP6A8	PROBEPOINT_SM	m38a[5A6]
PP6A9	PROBEPOINT_SM	m38a[5A6]
PP6B0	PROBEPOINT_SM	m38a[5A6]
PP6B1	PROBEPOINT_SM	m38a[5A6]
PP6B2	PROBEPOINT_SM	m38a[5A6]
PP6B3	PROBEPOINT_SM	m38a[5A6]
PP6B4	PROBEPOINT_SM	m38a[5A6]
PP6B5	PROBEPOINT_SM	m38a[5A6]
PP6B6	PROBEPOINT_SM	m38a[5A6]
PP6B7	PROBEPOINT_SM	m38a[5A6]
PP6B8	PROBEPOINT_SM	m38a[5A6]
PP6B9	PROBEPOINT_SM	m38a[5A6]
PP6C0	PROBEPOINT_SM	m38a[5A6]
PP6C1	PROBEPOINT_SM	m38a[5A6]
PP6C2	PROBEPOINT_SM	m38a[5A6]
PP6C3	PROBEPOINT_SM	m38a[5A6]
PP6C4	PROBEPOINT_SM	m38a[5C8]
PP6C5	PROBEPOINT_SM	m38a[5C8]
PP6C6	PROBEPOINT_SM	m38a[5C8]
PP6C7	PROBEPOINT_SM	m38a[5C8]
PP6C8	PROBEPOINT_SM	m38a[5C8]
PP6D0	PROBEPOINT_SM	m38a[5C8]
PP6D1	PROBEPOINT_SM	m38a[5C8]
PP6D2	PROBEPOINT_SM	m38a[5B8]
PP6D3	PROBEPOINT_SM	m38a[5B8]
PP6D4	PROBEPOINT_SM	m38a[5B8]
PP6D5	PROBEPOINT_SM	m38a[5B8]
PP6D6	PROBEPOINT_SM	m38a[5B8]
PP6D7	PROBEPOINT_SM	m38a[5B8]
PP6D8	PROBEPOINT_SM	m38a[5B8]
PP6D9	PROBEPOINT_SM	m38a[5B8]
PP6E0	PROBEPOINT_SM	m38a[5B8]
PP6E1	PROBEPOINT_SM	m38a[5B6]
PP6600	PROBEPOINT_SM	m38a[5D8]
PP661	PROBEPOINT_SM	m38a[5D8]
PP602	PROBEPOINT_SM	m38a[5D8]
PP603	PROBEPOINT_SM	m38a[5D8]
PP604	PROBEPOINT_SM	m38a[5D8]
PP605	PROBEPOINT_SM	m38a[5D8]
PP606	PROBEPOINT_SM	m38a[5D8]
PP607	PROBEPOINT_SM	m38a[5D8]
PP608	PROBEPOINT_SM	m38a[5D8]
PP609	PROBEPOINT_SM	m38a[5D8]
PP610	PROBEPOINT_SM	m38a[5D8]
PP611	PROBEPOINT_SM	m38a[5D8]
PP612	PROBEPOINT_SM	m38a[5D8]
PP613	PROBEPOINT_SM	m38a[5D8]
PP614	PROBEPOINT_SM	m38a[5D8]
PP615	PROBEPOINT_SM	m38a[5D8]
PP616	PROBEPOINT_SM	m38a[5D8]
PP617	PROBEPOINT_SM	m38a[5D8]
PP618	PROBEPOINT_SM	m38a[5D8]
PP619	PROBEPOINT_SM	m38a[5D8]
PP620	PROBEPOINT_SM	m38a[5D8]
PP621	PROBEPOINT_SM	m38a[5C8]
PP622	PROBEPOINT_SM	m38a[5C8]
PP623	PROBEPOINT_SM	m38a[5C8]
PP624	PROBEPOINT_SM	m38a[5C8]
PP625	PROBEPOINT_SM	m38a[5C8]
PP626	PROBEPOINT_SM	m38a[5C8]
PP627	PROBEPOINT_SM	m38a[5C8]
PP628	PROBEPOINT_SM	m38a[5C8]
PP629	PROBEPOINT_SM	m38a[5C8]
PP630	PROBEPOINT_SM	m38a[5C8]
PP631	PROBEPOINT_SM	m38a[5D6]
PP632	PROBEPOINT_SM	m38a[5D6]
PP633	PROBEPOINT_SM	m38a[5D6]
PP634	PROBEPOINT_SM	m38a[5D6]
PP635	PROBEPOINT_SM	m38a[5D6]
PP636	PROBEPOINT_SM	m38a[5D6]
PP637	PROBEPOINT_SM	m38a[5D6]
PP638	PROBEPOINT_SM	m38a[5D6]
PP639	PROBEPOINT_SM	m38a[5D6]
PP640	PROBEPOINT_SM	m38a[5D6]
PP641	PROBEPOINT_SM	m38a[5D6]
PP642	PROBEPOINT_SM	m38a[5D6]
PP643	PROBEPOINT_SM	m38a[5D6]
PP644	PROBEPOINT_SM	m38a[5D6]
PP645	PROBEPOINT_SM	m38a[5D6]
PP646	PROBEPOINT_SM	m38a[5D6]
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PP653	PROBEPOINT_SM	m38a[5C6]
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PP665	PROBEPOINT_SM	m38a[5C6]
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PP667	PROBEPOINT_SM	m38a[5C6]
PP668	PROBEPOINT_SM	m38a[5C6]
PP673	PROBEPOINT_SM	m38a[5C6]
PP674	PROBEPOINT_SM	m38a[5C6]
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PP699	PROBEPOINT_SM	m38a[5B6]
PP700	TP_SM-TP50-TOP	m38a[5D3]
PP701	TP_SM-TP50-TOP	m38a[5D3]
PP702	TP_SM-TP50-TOP	m38a[5D3]
PP1200	TP_SM-TP50-TOP	m38a[5D3]
PP1201	TP_SM-TP50-TOP	m38a[5D3]
PP1202	TP_SM-TP50-TOP	m38a[5D3]
PP2800	TP_SM-TP50-TOP	m38a[5C3]
PP2801	TP_SM-TP50-TOP	m38a[5C3]
PP2802	TP_SM-TP50-TOP	m38a[5C3]
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PP4101	PROBEPOINT_SM	m38a[5D4]
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PP8401	PROBEPOINT_SM	m38a[5C5]
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PP8701	PROBEPOINT_SM	m38a[5D5]
PP8702	PROBEPOINT_SM	m38a[5D5]
PP8703	PROBEPOINT_SM	m38a[5D5]
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PP8705	PROBEPOINT_SM	m38a[5D5]
PP8706	PROBEPOINT_SM	m38a[5D5]
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PP8713	PROBEPOINT_SM	m38a[5D5]
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PP8728	PROBEPOINT_SM	m38a[5C5]
PP8729	PROBEPOINT_SM	m38a[5C5]
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PP8731	PROBEPOINT_SM	m38a[5C5]
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PP8733	PROBEPOINT_SM	m38a[5C5]
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PP8901	PROBEPOINT_SM	m38a[5B5]
PP8902	PROBEPOINT_SM	m38a[5B5]
PP8903	PROBEPOINT_SM	m38a[5B5]
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Q5901	TRA_2N7002DW_SOT-363	m38a[59C7 59C7]
Q5910	TRA_SINGLE_MOSFET_PC-HN_SOT-23	m38a[59A4]
Q5911	TRA_2N7002_SOT23-LF	m38a[59A4]
Q5950	TRA_2N7002_SOT23-LF	m38a[60A7]
Q5951	TRA_2N7002_SOT23-LF	m38a[60B7]
Q5952	TRA_2N3906_SOT23-LF	m38a[60B6]
Q6500	TRA_NTHS5443T1_1206A-03-LF	m38a[65D4]
Q6502	TRA_2N7002_SOT23-LF	m38a[65D6]
Q6503	TRA_NTHS5443T1_1206A-03-LF	m38a[65B4]
Q6505	TRA_2N7002_SOT23-LF	m38a[65B6]
Q6600	TRA_NTHS5443T1_1206A-03-LF	m38a[66D4]
Q6602	TRA_2N7002_SOT23-LF	m38a[66C5]
Q7200	TRA_2N7002DW_SOT-363	m38a[72B6 72B7]
Q7400	TRA_2N7002DW_SOT-363	m38a[74B3 74B3]
Q7401	TRA_2N7002_SOT23-LF	m38a[74D5]
Q7402	TRA_2N7002DW_SOT-363	m38a[74B2 74B2]
Q7500	TRA_HAT2168H_LFPAK	m38a[75D3]
Q7501	TRA_HAT2165H_LFPAK	m38a[75D3]
Q7502	TRA_HAT2168H_LFPAK	m38a[75C3]
Q7503	TRA_HAT2165H_LFPAK	m38a[75B3]
Q7504	TRA_HAT2165H_LFPAK	m38a[75D3]
Q7505	TRA_HAT2168H_LFPAK	m38a[75B3]
Q7570	TRA_HAT2168H_LFPAK	m38a[75D2]
Q7572	TRA_HAT2168H_LFPAK	m38a[75C3]
Q7701	TRA_SI3446DV_TSOP-LF	m38a[77A3]
Q7703	TRA_2N7002DW_SOT-363	m38a[77C7 77D7]
Q7799	TRA_2N7002_SOT23-LF	m38a[77A7]
Q7800	TRA_NTD60N02R_CASE369-LF	m38a[78C4]
Q7801	TRA_NTD60N02R_CASE369-LF	m38a[78B4]
Q7802	TRA_2N7002_SOT23-LF	m38a[78B7]
Q7900	TRA_NTD60N02R_CASE369-LF	m38a[79D4]
Q7901	TRA_NTD60N02R_CASE369-LF	m38a[79C4]
Q7902	TRA_2N7002_SOT23-LF	m38a[79C7]
Q8000	TRA_NTD60N02R_CASE369-LF	m38a[80D4]
Q8001	TRA_NTD60N02R_CASE369-LF	m38a[80C4]
Q8003	TRA_2N7002_SOT23-LF	m38a[80C7]
Q8102	TRA_NTD60N02R_CASE369-LF	m38a[81D4]
Q8103	TRA_NTD60N02R_CASE369-LF	m38a[81C4]
Q8104	TRA_2N7002_SOT23-LF	m38a[81C7]
Q8300	TRA_IRF7413_SO-8	m38a[83C4]
Q8301	TRA_IRF7413_SO-8	m38a[83B4]
Q8302	TRA_2N7002DW_SOT-363	m38a[83B5]
Q8303	TRA_2N7002DW_SOT-363	m38a[83C5]
Q8520	TRA_HAT2168H_LFPAK	m38a[85D4]
Q8521	TRA_HAT2165H_LFPAK	m38a[85C4]
Q8522	TRA_HAT2165H_LFPAK	m38a[85C5]
Q9400	TRA_SI3443DV_TSOP-LF	m38a[94C7]
Q9401	TRA_2N7002_SOT23-LF	m38a[94C7]
Q9711	TRA_2N7002DW_SOT-363	m38a[97D2 97C2]
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R600	RES_402	m38a[6A7]
R601	RES_402	m38a[6D8]
R602	RES_402	m38a[6A8]
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R605	RES_603	m38a[6A6]
R611	RES_402	m38a[6B7]
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R618	RES_402	m38a[6C7]
R619	RES_402	m38a[6C7]
R0701	RES_402	m38a[7C6]
R0702	RES_402	m38a[7D6]
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R0719	RES_402	m38a[7B1]
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R1005	RES_402	m38a[10D3]
R1017	RES_402	m38a[10C6]
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R1100	RES_402	m38a[11B5]
R1101	RES_402	m38a[11C5]
R1102	RES_402	m38a[11B4]
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R1104	RES_402	m38a[11B5]
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R2059	RES_402	m38a[20B4]
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R2075	RES_402	m38a[20C7]
R2077	RES_402	m38a[20B7]
R2079	RES_402	m38a[20B7]
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R2107	RES_402	m38a[21C2]
R2108	RES_402	m38a[21C2]
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R2194	RES_402	m38a[21D4]
R2195	RES_402	m38a[21C6]
R2196	RES_402	m38a[21C6]
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R2205	RES_402	m38a[22C6]
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R2222	RES_402	m38a[22D6]
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R2502	RES_402	m38a[25D8]
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R2719	RES_402	m38a[27B7]
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R3035	RES_402	m38a[30B4]
R3100	RES_402	m38a[31C5]
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R3300	RES_402	m38a[33B6]
R3301	RES_402	m38a[33B7]
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R3404	RES_402	m38a[34C5]
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R4651	RES_402	m38a[46C7]
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R6301	RES_402	m38a[63D4]
R6302	RES_402	m38a[63D4]
R6303	RES_402	m38a[63C2]
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R6307	RES_402	m38a[63C5]
R6309	RES_402	m38a[63C5]
R6399	RES_402	m38a[63D2]
R6500	RES_402	m38a[65C7]
R6501	RES_402	m38a[65A7]
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R6503	RES_805	m38a[65D5]
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R6506	RES_402	m38a[65D6]
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R6510	RES_1206	m38a[65B6]
R6511	RES_402	m38a[65B6]
R6512	RES_805	m38a[65C5]
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R6514	RES_805	m38a[65B4]
R6515	RES_805	m38a[65C4]
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R6605	RES_402	m38a[66D6]
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R6808	RES_402	m38a[68D3]
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R7214	RES_402	m38a[72C5]
R7215	RES_402	m38a[72C7]
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R7219	RES_402	m38a[72B6]
R7302	RES_402	m38a[73A3]
R7305	RES_402	m38a[73C8]
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R7308	RES_402	m38a[73B8]
R7400	RES_402	m38a[74B4]
R7404	RES_402	m38a[74D5]
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R7408	RES_402	m38a[74A4]
R7409	RES_402	m38a[74B4]
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R7418	RES_402	m38a[74B6]
R7419	RES_402	m38a[74B6]
R7420	RES_402	m38a[74D5]
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R7422	RES_402	m38a[74D7]
R7423	RES_402	m38a[74B6]
R7424	RES_402	m38a[74B6]
R7425	RES_603	m38a[74A5]
R7426	RES_402	m38a[74A4]
R7427	RES_402	m38a[74A4]
R7430	RES_402	m38a[74C1]
R7431	RES_402	m38a[74C2]
R7435	RES_402	m38a[74A3]
R7437	RES_402	m38a[74C5]
R7440	RES_805	m38a[74D2]
R7442	RES_805	m38a[74D3]
R7443	RES_805	m38a[74D3]
R7500	RES_402	m38a[75C2]
R7501	RES_603	m38a[75C2]
R7502	RES_1206	m38a[75B2]
R7503	RES_1206	m38a[75D2]
R7504	RES_402	m38a[75C1]
R7505	RES_402	m38a[75B2]
R7506	RES_603	m38a[75B2]
R7507	RES_402	m38a[75B1]
R7508	RES_402	m38a[75B8]
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R7510	RES_402	m38a[75B6]
R7511	RES_402	m38a[75B7]
R7512	RES_402	m38a[75D7]
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R7527	RES_402	m38a[75C8]
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R7595	RES_402	m38a[75C7]
R7596	RES_402	m38a[75D7]
R7597	RES_402	m38a[76D6]
R7598	RES_402	m38a[76D7]
R7599	RES_2512-1	m38a[76D7]
R7602	RES_402	m38a[76D3]

R7612	RES_402	m38a[76B2]
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R7623	RES_402	m38a[76D1]
R7630	RES_402	m38a[76C8]
R7631	RES_402	m38a[76C8]
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R7640	RES_402	m38a[76A7]
R7691	RES_402	m38a[76C7]
R7700	RES_402	m38a[77D3]
R7701	RES_402	m38a[77D4]
R7704	RES_402	m38a[77C4]
R7705	RES_402	m38a[77C3]
R7706	RES_402	m38a[77D2]
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R8001	RES_402	m38a[80C7]
R8002	RES_1206	m38a[80C4]
R8003	RES_402	m38a[80C3]
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R8005	RES_402	m38a[80D7]
R8007	RES_402	m38a[80A4]
R8010	RES_402	m38a[80B2]
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R8192	RES_402	m38a[81C7]
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R8301	RES_402	m38a[83C5]
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R8303	RES_402	m38a[83C4]
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R8496	RES_402	m38a[84A2]
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R8598	RES_402	m38a[85D2]
R8599	RES_1206	m38a[85C4]
R8630	RES_603	m38a[86C7]
R8710	RES_402	m38a[87B8]
R8711	RES_402	m38a[87A8]
R8712	RES_402	m38a[87B7]
R8713	RES_402	m38a[87A7]
R8720	RES_402	m38a[87B4]
R8721	RES_402	m38a[87A4]
R8722	RES_402	m38a[87B4]
R8723	RES_402	m38a[87A4]
R8730	RES_402	m38a[87A3]
R8731	RES_402	m38a[87A3]
R8732	RES_402	m38a[87A3]
R8733	RES_402	m38a[87A1]
R8800	RES_603	m38a[88D7]
R8801	RES_402	m38a[88A7]
R8802	RES_402	m38a[88D4]
R8803	RES_402	m38a[88D4]
R8804	RES_402	m38a[88D4]
R8805	RES_402	m38a[88C4]
R8806	RES_402	m38a[88C4]

R8807	RES_402	m38a[88C4]
R8808	RES_402	m38a[88C4]
R8809	RES_402	m38a[88C4]
R8810	RES_402	m38a[88C4]
R8811	RES_402	m38a[88B4]
R8812	RES_402	m38a[88C4]
R8813	RES_402	m38a[88D4]
R8830	RES_402	m38a[88B4]
R8831	RES_402	m38a[88B4]
R8832	RES_402	m38a[88B4]
R8833	RES_402	m38a[88B4]
R8850	RES_402	m38a[88B4]
R8930	RES_402	m38a[89C7]
R8931	RES_402	m38a[89C7]
R8932	RES_402	m38a[89C7]
R8933	RES_402	m38a[89C7]
R8940	RES_402	m38a[89B8]
R8941	RES_402	m38a[89B8]
R8942	RES_402	m38a[89B7]
R8943	RES_402	m38a[89B7]
R8944	RES_402	m38a[89B7]
R8945	RES_402	m38a[89B7]
R8946	RES_402	m38a[89B7]
R8947	RES_402	m38a[89B7]
R8948	RES_402	m38a[89A7]
R8949	RES_402	m38a[89A7]
R8980	RES_402	m38a[89C4]
R8981	RES_402	m38a[89C4]
R8982	RES_402	m38a[89C4]
R8983	RES_402	m38a[89C4]
R8990	RES_402	m38a[89B5]
R8991	RES_402	m38a[89B4]
R8992	RES_402	m38a[89B4]
R8993	RES_402	m38a[89B4]
R8994	RES_402	m38a[89B4]
R8995	RES_402	m38a[89B4]
R8996	RES_402	m38a[89B4]
R8997	RES_402	m38a[89B4]
R8998	RES_402	m38a[89A4]
R8999	RES_402	m38a[89A4]
R9030	RES_402	m38a[90C7]
R9031	RES_402	m38a[90C7]
R9032	RES_402	m38a[90C7]
R9033	RES_402	m38a[90C7]
R9040	RES_402	m38a[90B8]
R9041	RES_402	m38a[90B8]
R9042	RES_402	m38a[90B7]
R9043	RES_402	m38a[90B7]
R9044	RES_402	m38a[90B7]
R9045	RES_402	m38a[90B7]
R9046	RES_402	m38a[90B7]
R9047	RES_402	m38a[90B7]
R9048	RES_402	m38a[90A7]
R9049	RES_402	m38a[90A7]
R9080	RES_402	m38a[90C4]
R9081	RES_402	m38a[90C4]
R9082	RES_402	m38a[90C4]
R9083	RES_402	m38a[90C4]
R9090	RES_402	m38a[90B5]
R9091	RES_402	m38a[90B4]
R9092	RES_402	m38a[90B4]
R9093	RES_402	m38a[90B4]
R9094	RES_402	m38a[90B4]
R9095	RES_402	m38a[90B4]
R9096	RES_402	m38a[90B4]
R9097	RES_402	m38a[90B4]
R9098	RES_402	m38a[90A4]
R9099	RES_402	m38a[90A4]
R9190	RES_402	m38a[91D2]
R9191	RES_402	m38a[91D2]
R9195	RES_402	m38a[91A3]
R9202	RES_402	m38a[92C6]
R9250	RES_402	m38a[92C6]
R9350	RES_402	m38a[93A8]
R9351	RES_402	m38a[93A8]
R9370	RES_402	m38a[93D1]
R9371	RES_402	m38a[93D1]
R9372	RES_402	m38a[93C1]
R9373	RES_402	m38a[93C1]
R9390	RES_402	m38a[93A1]
R9391	RES_402	m38a[93A1]
R9400	RES_402	m38a[94C8]
R9401	RES_402	m38a[94C7]
R9410	RES_402	m38a[94C6]
R9411	RES_402	m38a[94C6]
R9450	RES_402	m38a[94C2]
R9470	RES_402	m38a[94C7]
R9472	RES_402	m38a[94B3]
R9473	RES_402	m38a[94B2]
R9474	RES_402	m38a[94B2]
R9475	RES_402	m38a[94B1]
R9490	RES_805	m38a[94C6]
R9491	RES_805	m38a[94D6]
R9701	RES_402	m38a[97D8]
R9706	RES_402	m38a[97D8]
R9707	RES_402	m38a[97C8]
R9710	RES_402	m38a[97D2]
R9711	RES_402	m38a[97D2]
R9712	RES_402	m38a[97D2]
R9713	RES_402	m38a[97C2]
R9714	RES_402	m38a[97C2]
R9716	RES_402	m38a[97C8]
R9717	RES_402	m38a[97C8]
R9720	RES_402	m38a[97D1]
R9721	RES_402	m38a[97D1]
R9722	RES_402	m38a[97C2]
R9740	RES_402	m38a[97A8]
R9741	RES_402	m38a[97A8]
R9742	RES_402	m38a[97A7]
R9750	RES_402	m38a[97B3]
R9751	RES_402	m38a[97A3]
RP2300	RPAK4P_SM-LF	m38a[23D5]
RP3000	RPAK4P_SM-LF	m38a[30B4 30C4 30D4 30D4]
RP3001	RPAK4P_SM-LF	m38a[30C4 30A4 30A4 30D4]
RP3002	RPAK4P_SM-LF	m38a[30A4 30A4 30A4 30D4]
RP3003	RPAK4P_SM-LF	m38a[30C4 30C4 30C4 30D4]
RP3004	RPAK4P_SM-LF	m38a[30C4 30C4 30D4]
RP3005	RPAK4P_SM-LF	m38a[30B4 30A4 30A4 30D4]
RP3006	RPAK4P_SM-LF	m38a[30B4 30B4 30A4 30D4]
RP3007	RPAK4P_SM-LF	m38a[30C4 30C4 30C4 30C4]
RP3008	RPAK4P_SM-LF	m38a[30C4 30C4 30C4 30C4]
RP3009	RPAK4P_SM-LF	m38a[30B4 30B4 30C4 30C4]
RP3010	RPAK4P_SM-LF	m38a[30B4 30B4 30B4 30B4]
RP3011	RPAK4P_SM-LF	m38a[30B4 30A4 30B4 30B4]

RP7200	RPAK4P_SM-LF	m38a[72A4]
SDF4700	PCB_STANDOFF	m38a[47A2]
SDF4701	PCB_STANDOFF	m38a[47A2]
SDF5300	PCB_STANDOFF	m38a[53A5]
SDF5301	PCB_STANDOFF	m38a[53A5]
SDF9400	PCB_STANDOFF	m38a[94B6]
SDF9401	PCB_STANDOFF	m38a[94A6]
SW2600	SWI_TACT_4SM_EVQPH_S-M-LF	m38a[26C6]
SW5900	SWI_TACT_4SM_EVQPH_S-M-LF	m38a[59D8]
SW5901	SWI_TACT_4SM_EVQPH_S-M-LF	m38a[59B8]
U600	74LC125_TSSOP	m38a[6B7 6B7 6B7 6C7]
U601	SN74LVC1G04_SOT23-5	m38a[6C7]
U650	74AHC1G32_SM-LF	m38a[6A7]
U1000	ADT7461_MSOP	m38a[10D5]
U1200	NB_945GM_BGA	m38a[12D5]
U1200	NB_945GM_BGA	m38a[13D4]
U1200	NB_945GM_BGA	m38a[14D5]
U1200	NB_945GM_BGA	m38a[15D3 15D7]
U1200	NB_945GM_BGA	m38a[16D2 16C8]
U1200	NB_945GM_BGA	m38a[17D5]
U1200	NB_945GM_BGA	m38a[18D4 18D7]
U2100	SB_ICH7M_BGA	m38a[21D6]
U2100	SB_ICH7M_BGA	m38a[22B7 22D3]
U2100	SB_ICH7M_BGA	m38a[23D4]
U2100	SB_ICH7M_BGA	m38a[24D4 24D7]
U2601	MC74VHC1G08_SOT23-5-LF	m38a[26D5]
U2603	SN74LVC1G04_SOT23-5	m38a[26A7]
U2698	MC74VHC1G08_SOT23-5-LF	m38a[26C4]
U2699	MAX6816_SOT143	m38a[26C5]
U3100	LREG_BD3533FVM_MSOP-8	m38a[31C5]
U3301	CLK_GEN_CY284455_QFN	m38a[33C5]
U4101	88E8053_QFN	m38a[41D5]
U4102	EEPROM_M24C08_SO8	m38a[41A3]
U4400	FW32306_TQFP	m38a[44D5]
U4700	SWI_TPS2043_SOI	m38a[47C7]
U5800	SMC_H8S2116_BGA	m38a[58A8 58C3 58C6 58D6]
U5900	VDET_RN5VD_SOT23-5	m38a[59D8]
U5940	VREF_REF3133_SOT23-3	m38a[59A4]
U5999	COMPARATOR_LM393_SOI-1-LF	m38a[59A8 59A8]
U6100	MAX6695_UMAX	m38a[61C4]
U6301	FLASH_SST25VF016B_SOI_SOI	m38a[63D3]
U6700	TPM_TSSOP	m38a[67C5]
U6800	AUDIO_STAC92204XR_LQFP	m38a[68D5]
U7200	MAX9714_QFN-LF	m38a[72C5]
U7400	MAX9890_UCSP1	m38a[74C4]
U7500	ISL6262_QFN	m38a[75C6]
U7501	ZXCT1010_SOT23-5	m38a[76D7]
U7700	LTC3411_MSOP-LF	m38a[77D3]
U7710	MC74VHC1G08_SOT23-5-LF	m38a[77D5]
U7711	MC74VHC1G08_SOT23-5-LF	m38a[77C5]
U7712	MC74VHC1G08_SOT23-5-LF	m38a[77D4]
U7750	SN200505068_SOP	m38a[77B6]
U7800	ISL6549_QFN	m38a[78C6]
U7900	ISL6549_QFN	m38a[79D6]
U7901	COMPARATOR_LM339A_SOI-LF	m38a[79A5]
U7901	COMPARATOR_LM339A_SOI-LF	m38a[80A4]
U7901	COMPARATOR_LM339A_SOI-LF	m38a[81A5]
U7910	COMPARATOR_LM339A_SOI-LF	m38a[79A3 79B3]
U7910	COMPARATOR_LM339A_SOI-LF	m38a[80B2]
U7910	COMPARATOR_LM339A_SOI-LF	m38a[81B3]
U8000	ISL6549_QFN	m38a[80D6]
U8100	ISL6549_QFN	m38a[81D6]
U8400	ATI_M56P_BGA	m38a[84C8 84D4]
U8400	ATI_M56P_BGA	m38a[86D4]
U8400	ATI_M56P_BGA	m38a[87D2 87D6]
U8400	ATI_M56P_BGA	m38a[91D4]
U8400	ATI_M56P_BGA	m38a[93C4]
U8500	ISL6269_QFN	m38a[85D6]
U8595	OPAMP_LMV2011_SOT23-5	m38a[85D2]
U8900	SGRAM_16MX32_GDDR3_136H_FBGA	m38a[89D6 89B6]
U8950	SGRAM_16MX32_GDDR3_136H_FBGA	m38a[89D3 89B3]
U9000	SGRAM_16MX32_GDDR3_136H_FBGA	m38a[90D6 90B6]
U9050	SGRAM_16MX32_GDDR3_136H_FBGA	m38a[90D3 90B3]
U9470	MC74VHC1G08_SOT23-5-LF	m38a[94B2]
U9750	74AHC1G32_SM-LF	m38a[97B4]
U9751	74AHC1G32_SM-LF	m38a[97A4]
VR6800	LREG_MAX1819_UCSP	m38a[68A4]
XC7200	MTGHOLE	m38a[72B3]
XW601	SHORT_SM	m38a[6C2]
XW602	SHORT_SM	m38a[6C2]
XW604	SHORT_SM	m38a[6A5]
XW605	SHORT_SM	m38a[6A5]
XW5800	SHORT_SM	m38a[58B3]
XW5900	SHORT_SM	m38a[59B1]
XW6801	SHORT_SM	m38a[68B5]
XW7201	SHORT_SM	m38a[72B2]
XW7300	SHORT_SM	m38a[73C3]
XW7307	SHORT_SM	m38a[73C6]
XW7400	SHORT_SM	m38a[74A4]
XW7440	SHORT_SM	m38a[74C2]
XW7500	SHORT_SM	m38a[75A6]
XW7501	SHORT_SM	m38a[75B2]
XW7502	SHORT_SM	m38a[75B1]
XW7503	SHORT_SM	m38a[75D2]
XW7504	SHORT_SM	m38a[75D1]
XW7598	SHORT_SM	m38a[76D7]
XW7700	SHORT_SM	m38a[77C2]
XW7750	SHORT_SM	m38a[77A5]
XW7800	SHORT_SM	m38a[78B6]
XW7900	SHORT_SM	m38a[79C6]

XW8000	SHORT_SM	m38a[80C6]
XW8100	SHORT_SM	m38a[81C6]
XW8500	SHORT_SM	m38a[85C6]
Y2600	CRYSTAL_4PIN_SM-LF	m38a[26D8]
Y3301	CRYSTAL_5X3.2-SM	m38a[33C7]
Y4101	CRYSTAL_SM-3-LF	m38a[41B5]
Y4400	CRYSTAL_HC49-USMD	m38a[44D2]
Y5800	CRYSTAL_SM-3	m38a[59B8]
Y6700	CRYSTAL_4PIN_SM-LF	m38a[59B7]
ZH500	HOLE_VIA	m38a[5C1]
ZH501	HOLE_VIA	m38a[5C1]
ZH502	HOLE_VIA	m38a[5C1]
ZH503	HOLE_VIA	m38a[5C1]
ZH504	HOLE_VIA	m38a[5B1]
ZH505	HOLE_VIA	m38a[5B1]
ZH506	HOLE_VIA	m38a[5B1]
ZH507	HOLE_VIA	m38a[5B1]
ZH508	HOLE_VIA	m38a[5B1]
ZH509	HOLE_VIA	m38a[5B1]
ZH510	HOLE_VIA	m38a[5C1]
ZH511	HOLE_VIA	m38a[5C1]
ZH512	HOLE_VIA	m38a[5C1]
ZH513	HOLE_VIA	m38a[5C1]
ZH514	HOLE_VIA	m38a[5B1]
ZH515	HOLE_VIA	m38a[5B1]
ZH516	HOLE_VIA	m38a[5B1]
ZH517	HOLE_VIA	m38a[5B1]
ZH518	HOLE_VIA	m38a[5B1]
ZH519	HOLE_VIA	m38a[5B1]
ZH520	HOLE_VIA	m38a[5C1]
ZH521	HOLE_VIA	m38a[5C1]
ZH522	HOLE_VIA	m38a[5C1]
ZH523	HOLE_VIA	m38a[5C1]
ZH524	HOLE_VIA	m38a[5B1]
ZH525	HOLE_VIA	m38a[5B1]
ZH526	HOLE_VIA	m38a[5B1]
ZH527	HOLE_VIA	m38a[5B1]
ZH528	HOLE_VIA	m38a[5B1]
ZH529	HOLE_VIA	m38a[5B1]
ZH601	MTGHOLE	m38a[6A3]
ZH602	MTGHOLE	m38a[6A3]
ZH603	MTGHOLE	m38a[6A3]
ZH604	MTGHOLE	m38a[6B3]
ZH606	MTGHOLE	m38a[6A1]
ZH607	MTGHOLE	m38a[9D4]
ZH608	MTGHOLE	m38a[9D3]
ZH609	MTGHOLE	m38a[9D2]
ZH610	MTGHOLE	m38a[9D2]
ZH611	MTGHOLE	m38a[9C3]