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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IMAC 5,2 -- REV A

7/25/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
A		451207	PRODUCTION RELEASED		
				DATE	DATE
				07/26/06	06/22/04

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
5	5	FUNC TEST 1 OF 2	MASTER	MASTER	
6	6	Power Conn / Alias	MASTER	MASTER	
7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38		01/05/2006
12	12	NB CPU Interface	M1		01/05/2006
13	13	NB PEG / Video Interfaces	M1		01/05/2006
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1		01/05/2006
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40		01/05/2006
18	18	NB Grounds	M1		01/05/2006
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1		01/05/2006
21	21	SB: 1 OF 4	M38		01/05/2006
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38		01/05/2006
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector	AMASTER	MASTER	
29	29	DDR2 SO-DIMM Connector	BMASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1		01/05/2006
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38		12/09/2005
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38		01/05/2006
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38		01/05/2006
52	68	AUDIO: CODEC	AUDIO		05/12/2006
53	72	AUDIO: SPEAKER AMP	AUDIO		05/12/2006
54	73	AUDIO: CONNECTORS	AUDIO		05/12/2006
55	74	AUDIO: POWER SUPPLIES	AUDIO		05/12/2006
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUM	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	



DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7199	REV. A
SHT 1 OF 97					

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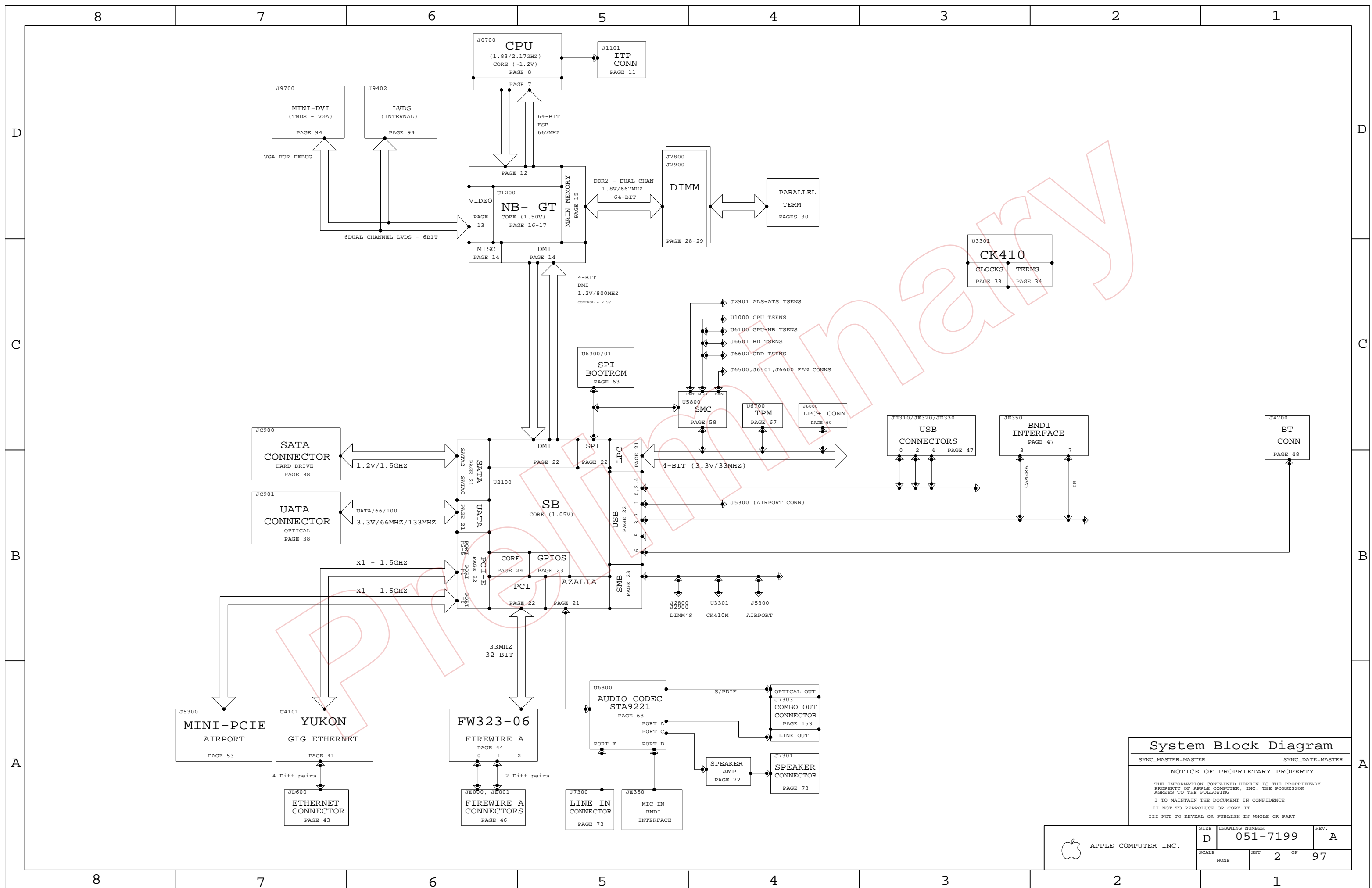
5

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System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

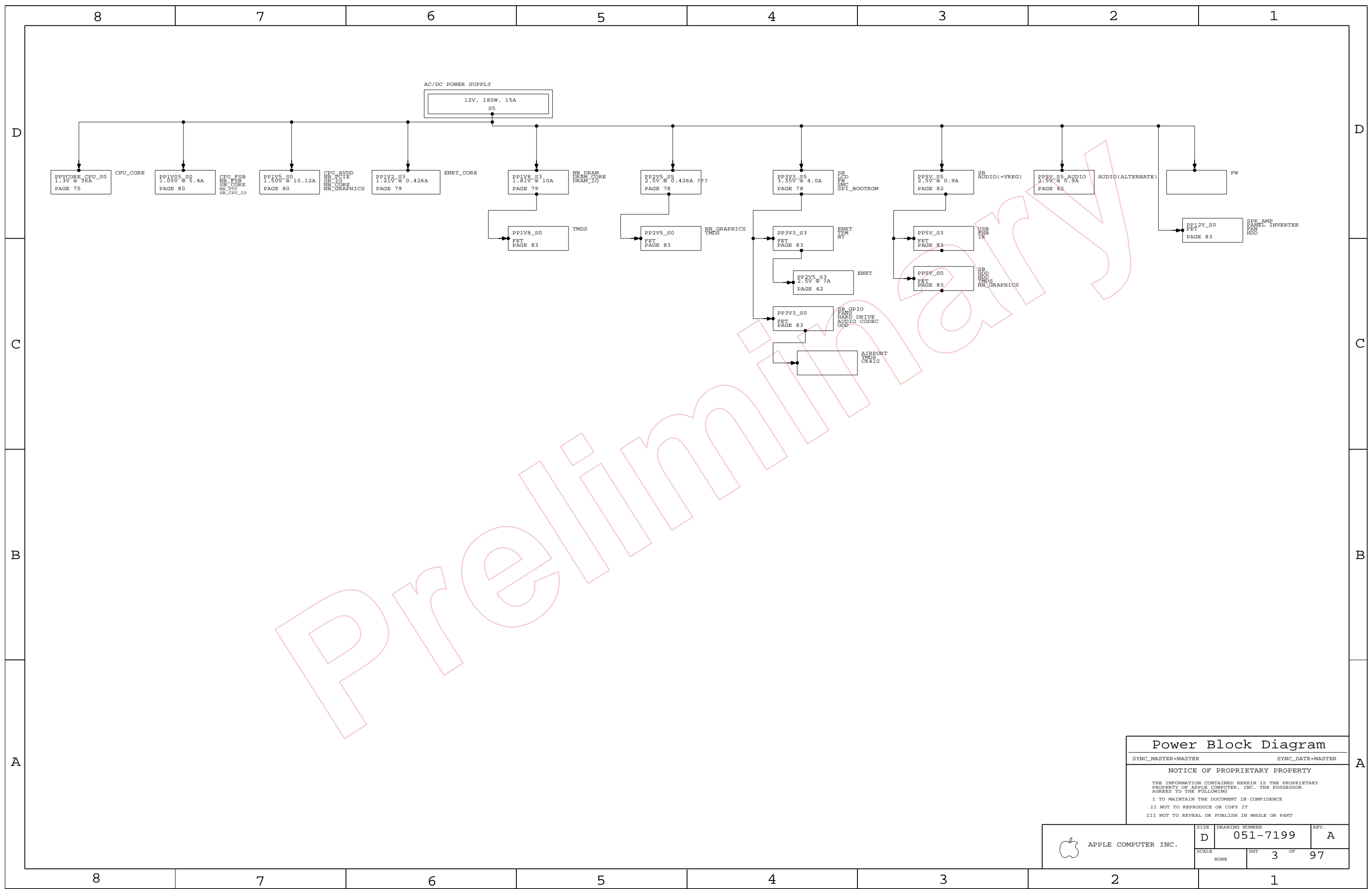
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	OF	
NONE	2	97	



Preliminary

Power Block Diagram

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 3	OF 97

8

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1461	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7199	1	PCB,SCHEM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0042	1	EFI ROM,M50A	U6301	CRITICAL	
337S3386	1	M50 MEROM CPU	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1465	353S1461		U7500	CPU VREG, OLD DIE, SCREENED PART
124-0338	124-0333		C7953,C7954	FOR SUPPLY

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50A	[EEE:WJ9]	CRITICAL	MEROM

Pre-internal

Table Items

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SIZE	DRAWING NUMBER	REV.
D	051-7199	A
SCALE	SHT	OF
NONE	4	97

8

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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS

Table of test points for FSB A L<6> through FSB CLK CPU N. Includes columns for test point name, value, and status.

Table of test points for FSB A L<6> through FSB HIT L. Includes columns for test point name, value, and status.

Table of test points for ENET CLK100M PCIE P through FSB REO L<4>. Includes columns for test point name, value, and status.

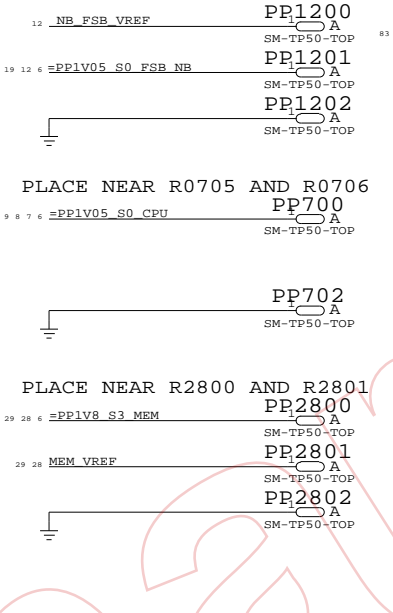


Table of test points for SMC TCK, SMC TDI, SMC TDO, SMC TMS, SMC TRST L, SMC TX L, SMC RX L, SMC MANUAL_RST L, XDP TCK, XDP TDI, XDP TDO, XDP TMS, XDP TRST L, POWER_BUTTON L, and SW_RST_BTN L.

LAYOUT NOTE: PLACE NEAR U2100

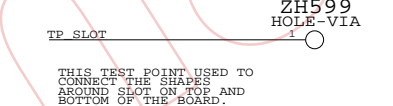
Table of test points for SB CLK100M SATA P, SB CLK100M SATA N, IDE PDIOR L, IDE PDIORY, IDE PDD<9>, PCI CLK SB, PCIE A D2R P, PCIE A D2R N, PCIE B D2R P, PCIE B D2R N, DMI N2S P<0>, DMI N2S N<0>, SB CLK100M DMI P, SB CLK100M DMI N, FM SYSRST L, FM CLKRUN L, SB CLK14PM TIMER, SB CLK48M USBCTLR.

Table of test points for VR_PWRGOOD_DELAY, NB_RST_IN_L_R, NB CLK100M GCLKIN P, NB CLK100M GCLKIN N, NB CLK DREFSSCLKIN P, NB CLK DREFSSCLKIN N.

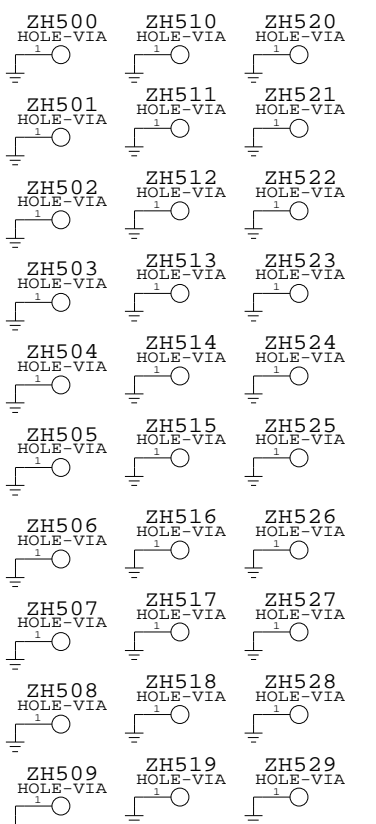
Table of test points for NB CLK DREFSSCLKIN P, NB CLK DREFSSCLKIN N, DMI S2N N<0>, DMI S2N P<0>, MEM VREF NB_0, MEM VREF NB_1, MEM A DQ<7>, MEM A DQ<14>, MEM A DQ<16>, MEM A DQ<25>, MEM A DQ<39>, MEM A DQ<47>, MEM A DQ<54>, MEM A DQ<59>, MEM A DQS P<0>, MEM A DQS N<0>, MEM A DQS P<1>, MEM A DQS N<1>, MEM A DQS P<2>, MEM A DQS N<2>, MEM A DQS P<3>, MEM A DQS N<3>, MEM A DQS P<4>, MEM A DQS N<4>, MEM A DQS P<5>, MEM A DQS N<5>, MEM A DQS P<6>, MEM A DQS N<6>, MEM A DQS P<7>, MEM A DQS N<7>, MEM B DQ<6>, MEM B DQ<8>, MEM B DQ<23>, MEM B DQ<25>, MEM B DQ<38>, MEM B DQ<44>, MEM B DQ<48>, MEM B DQ<62>, MEM B DQS P<0>, MEM B DQS N<0>, MEM B DQS P<1>, MEM B DQS N<1>, MEM B DQS P<2>, MEM B DQS N<2>, MEM B DQS P<3>, MEM B DQS N<3>, MEM B DQS P<4>, MEM B DQS N<4>, MEM B DQS P<5>, MEM B DQS N<5>, MEM B DQS P<6>, MEM B DQS N<6>, MEM B DQS P<7>, MEM B DQS N<7>.

Table of test points for PEG R2D C N<4> through PEG D2R N<15>. Includes columns for test point name, value, and status.

Table of test points for SPARE USB PORT, USB_F_N, USB_F_P, and LVDS_BKLTEN. Includes columns for test point name, value, and status.



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.



FUNC TEST 1 OF 2

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"S0" RAILS

ONLY ON IN RUN

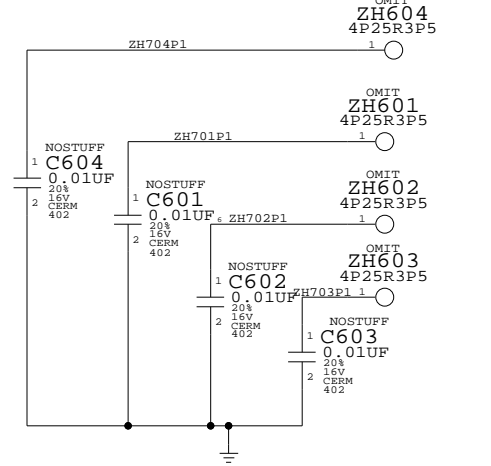
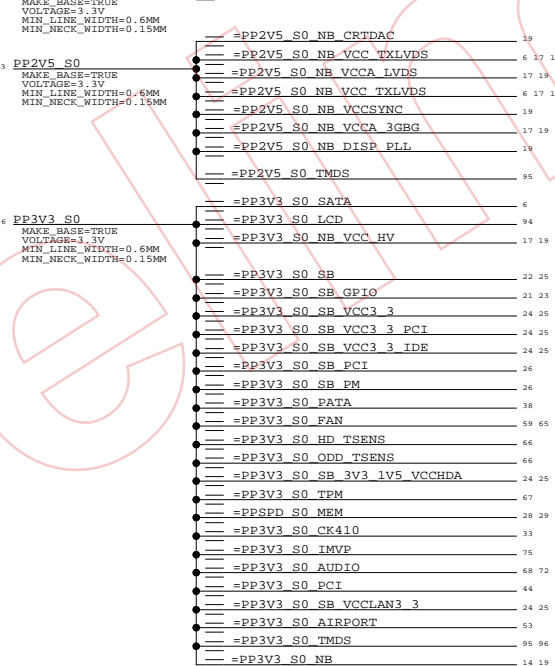
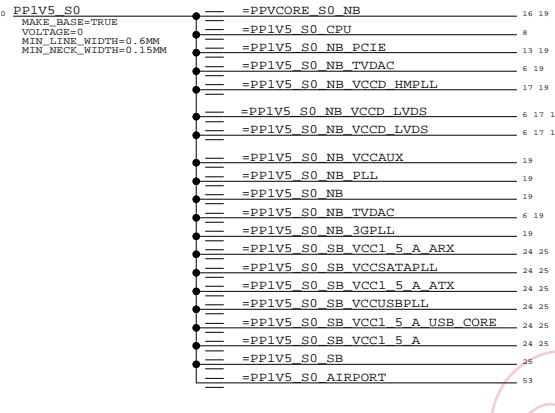
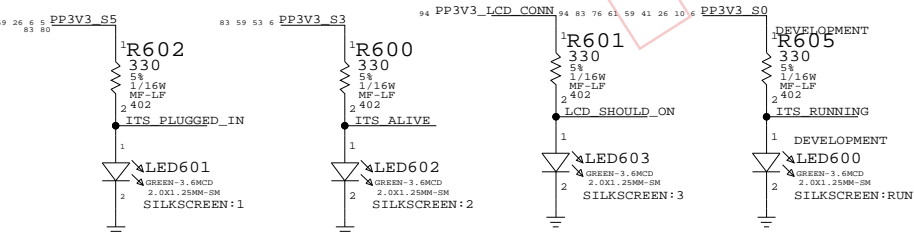
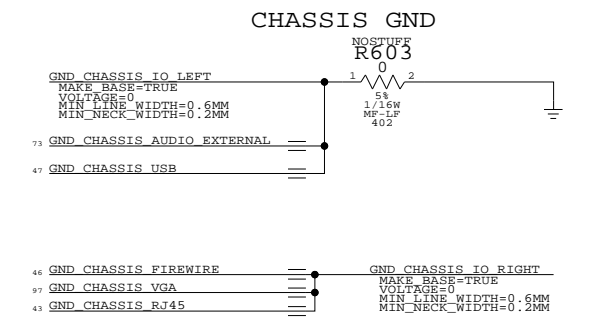
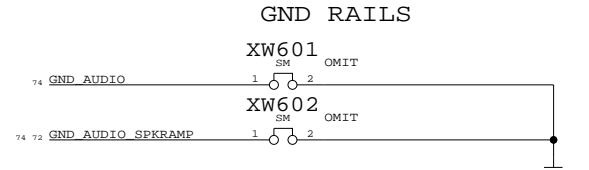
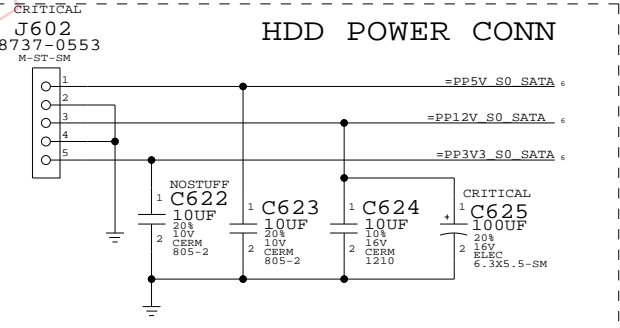
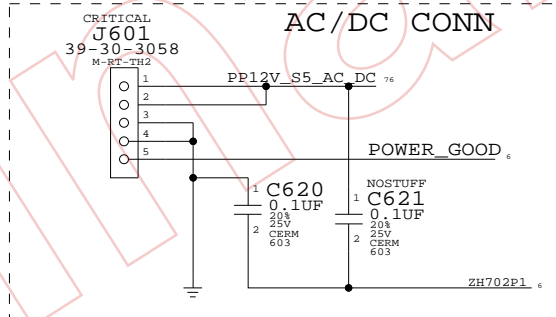
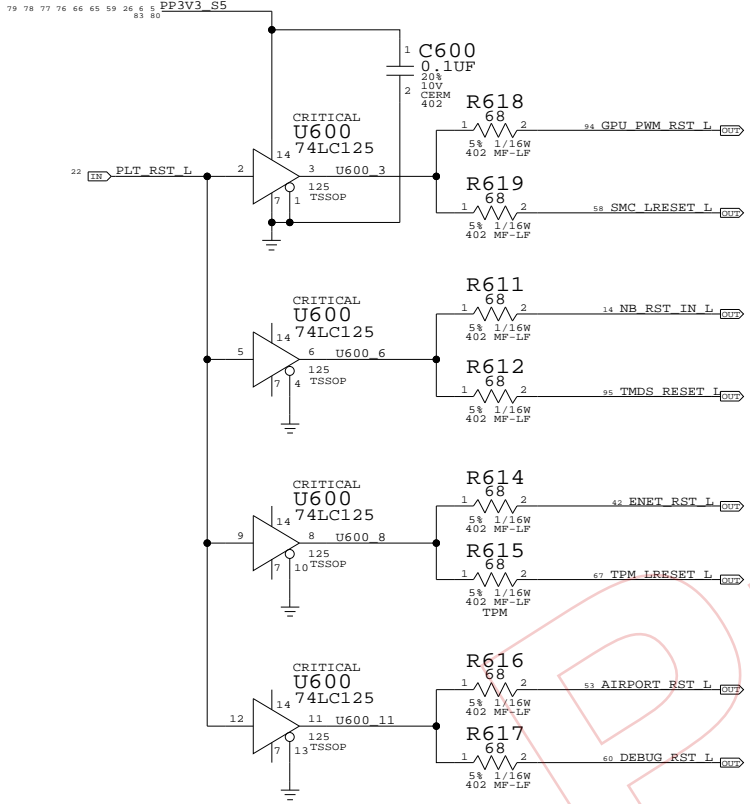
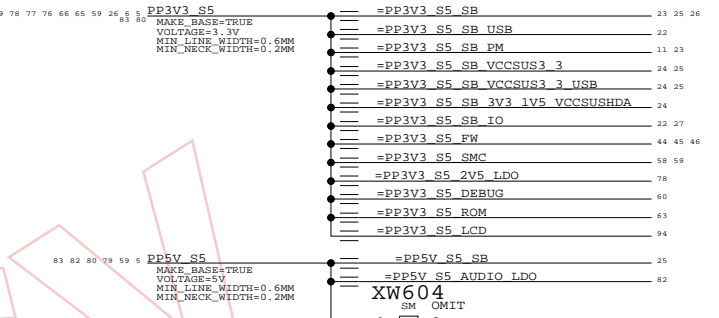
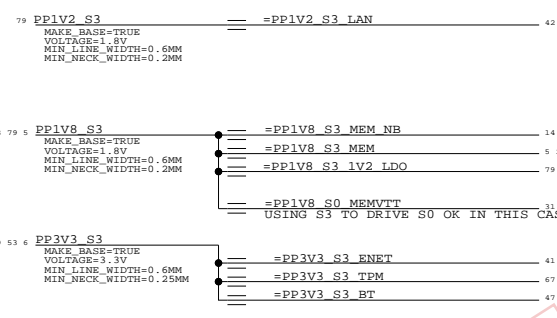
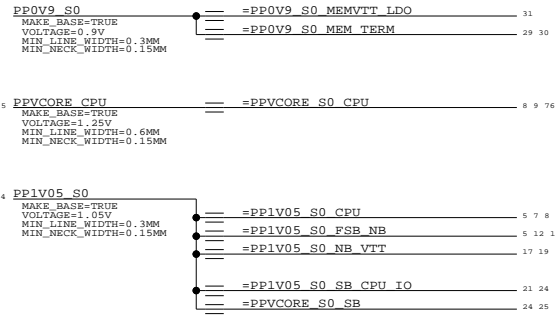
"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

I632 POWER_GOOD

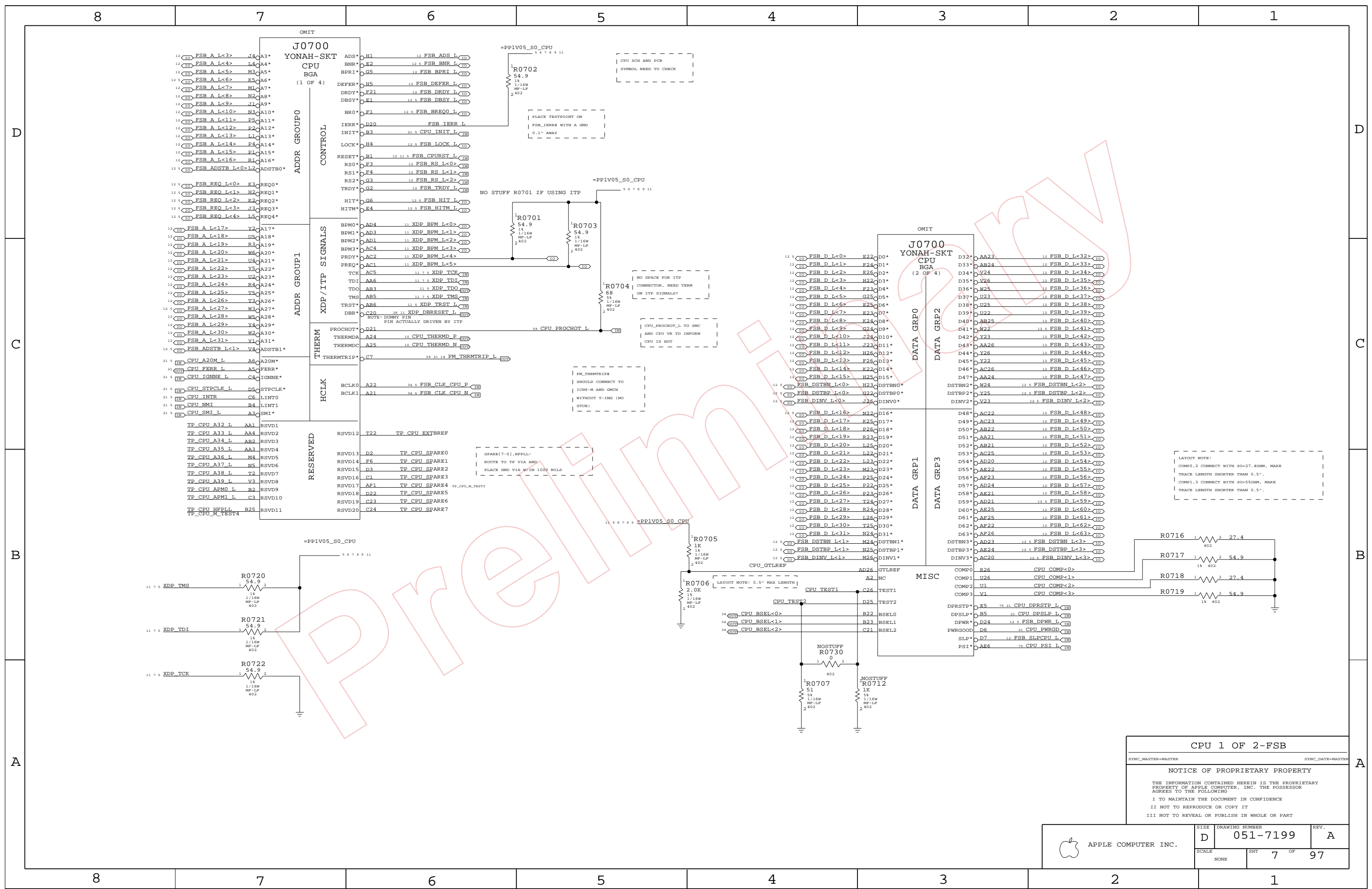


Power Conn / Alias

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATE-MASTER

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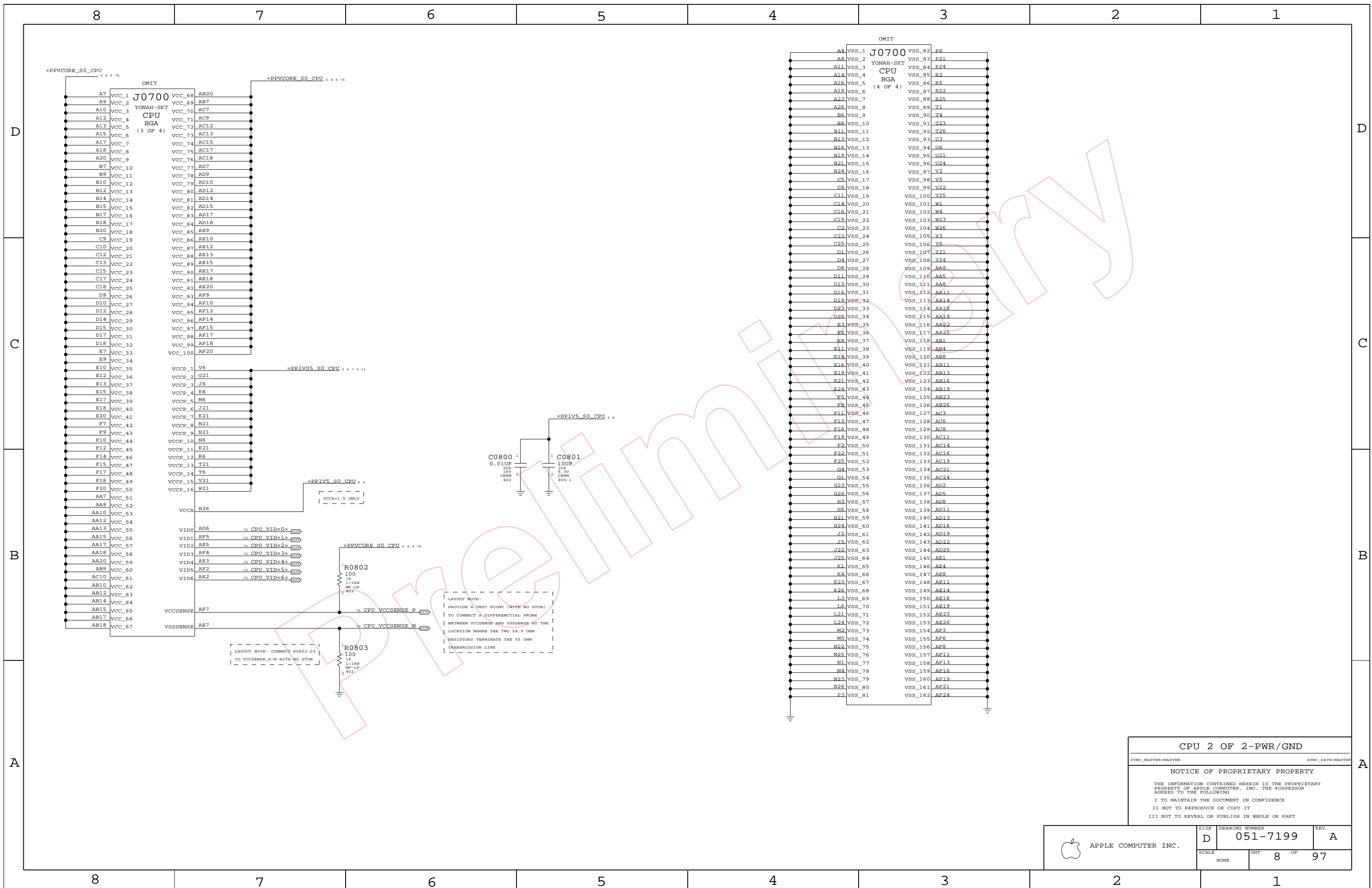
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	SCALE NONE	SHEET 7 OF 97	



CPU 2 OF 2-PWR/GND

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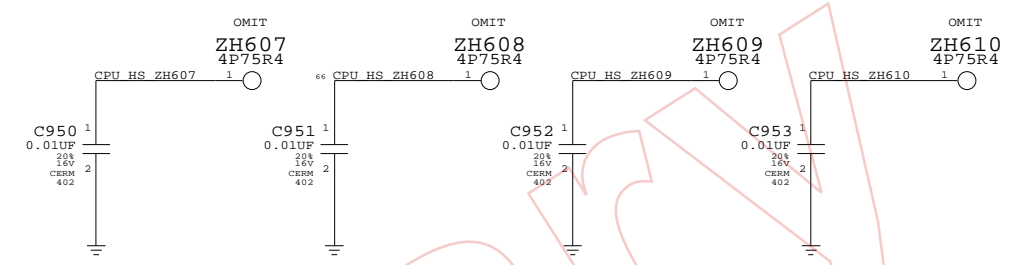
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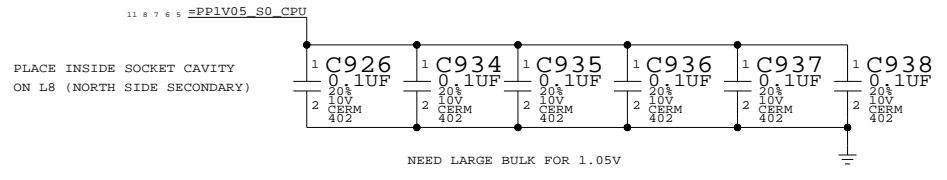
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 8 OF 97	

CPU HEATSINK MOUNTING HOLES



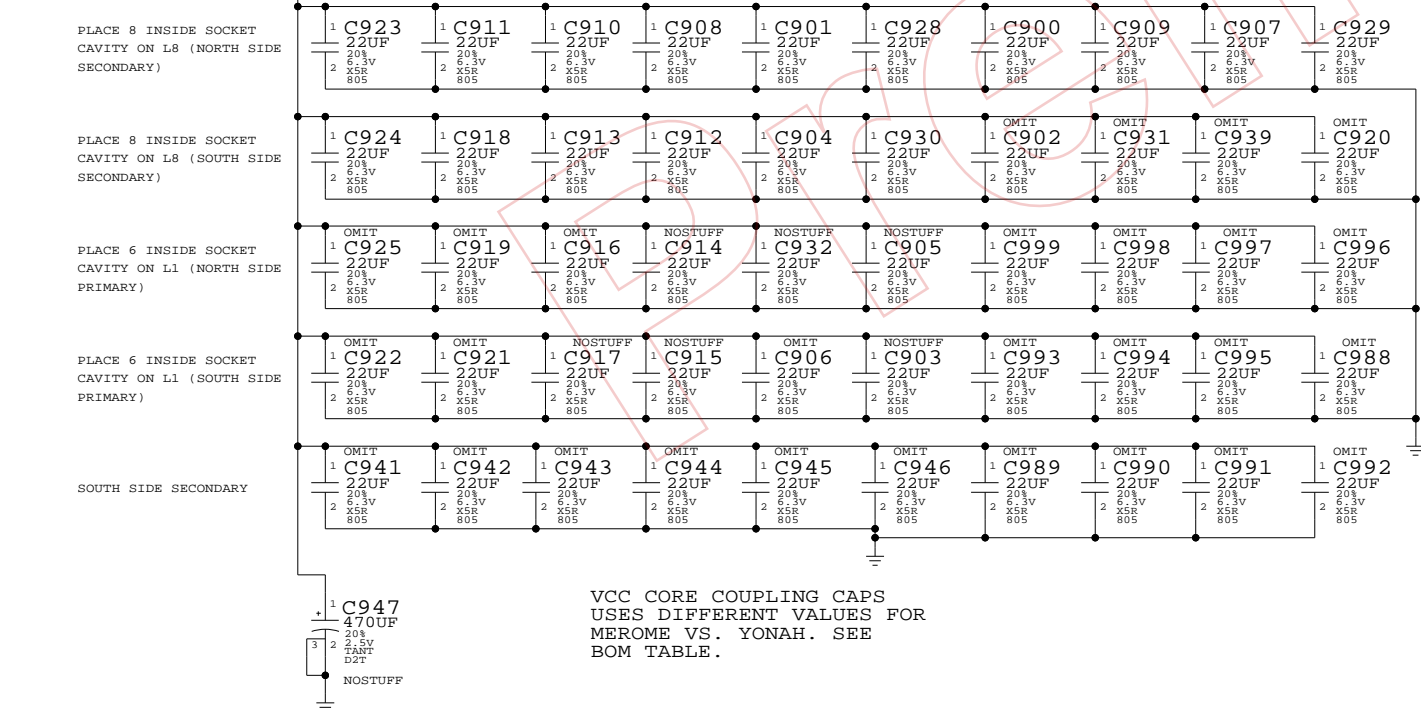
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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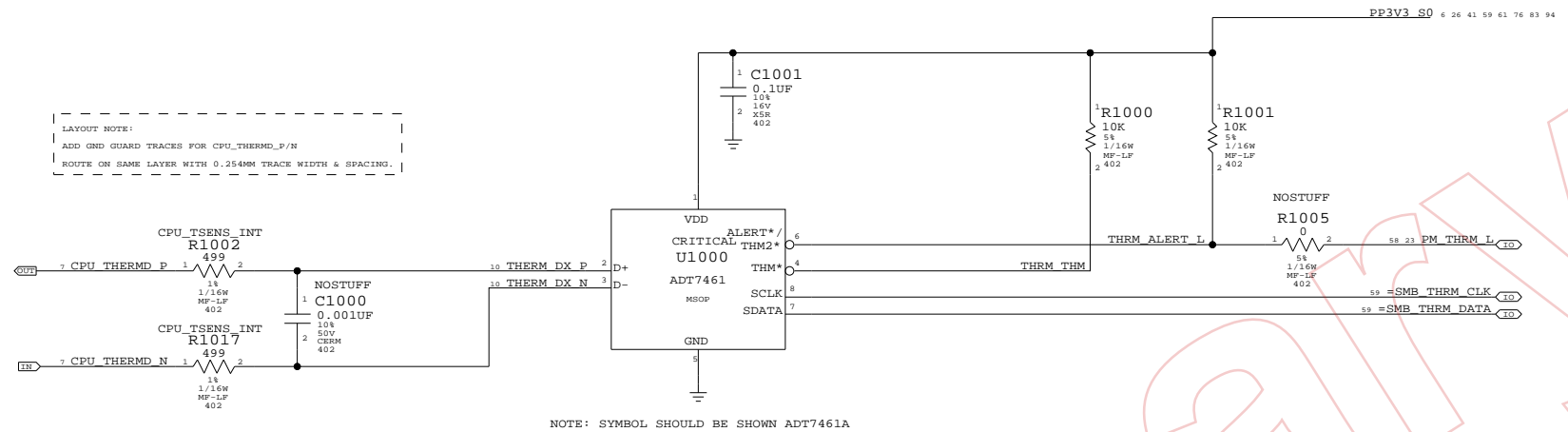
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	9 OF	97
NONE			

CPU THERMAL SENSOR

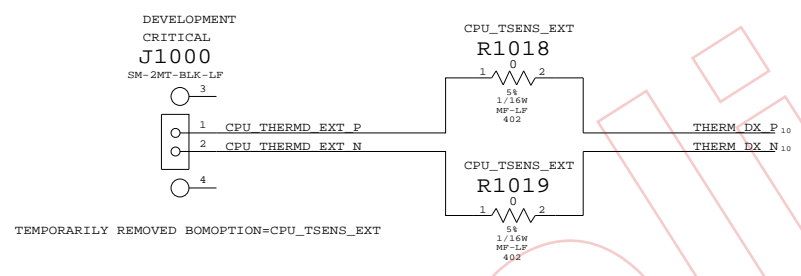
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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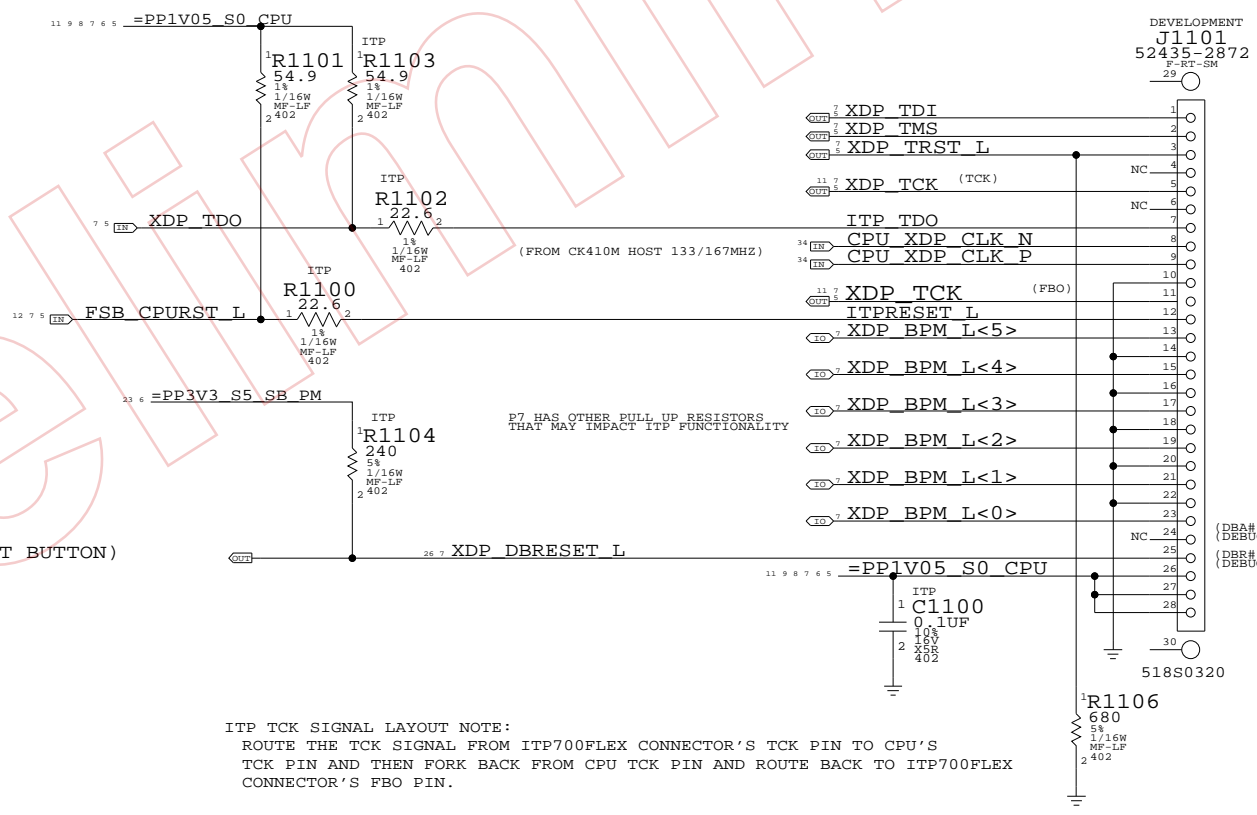
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	10 OF 97	
NONE			

CPU ITP700FLEX DEBUG SUPPORT



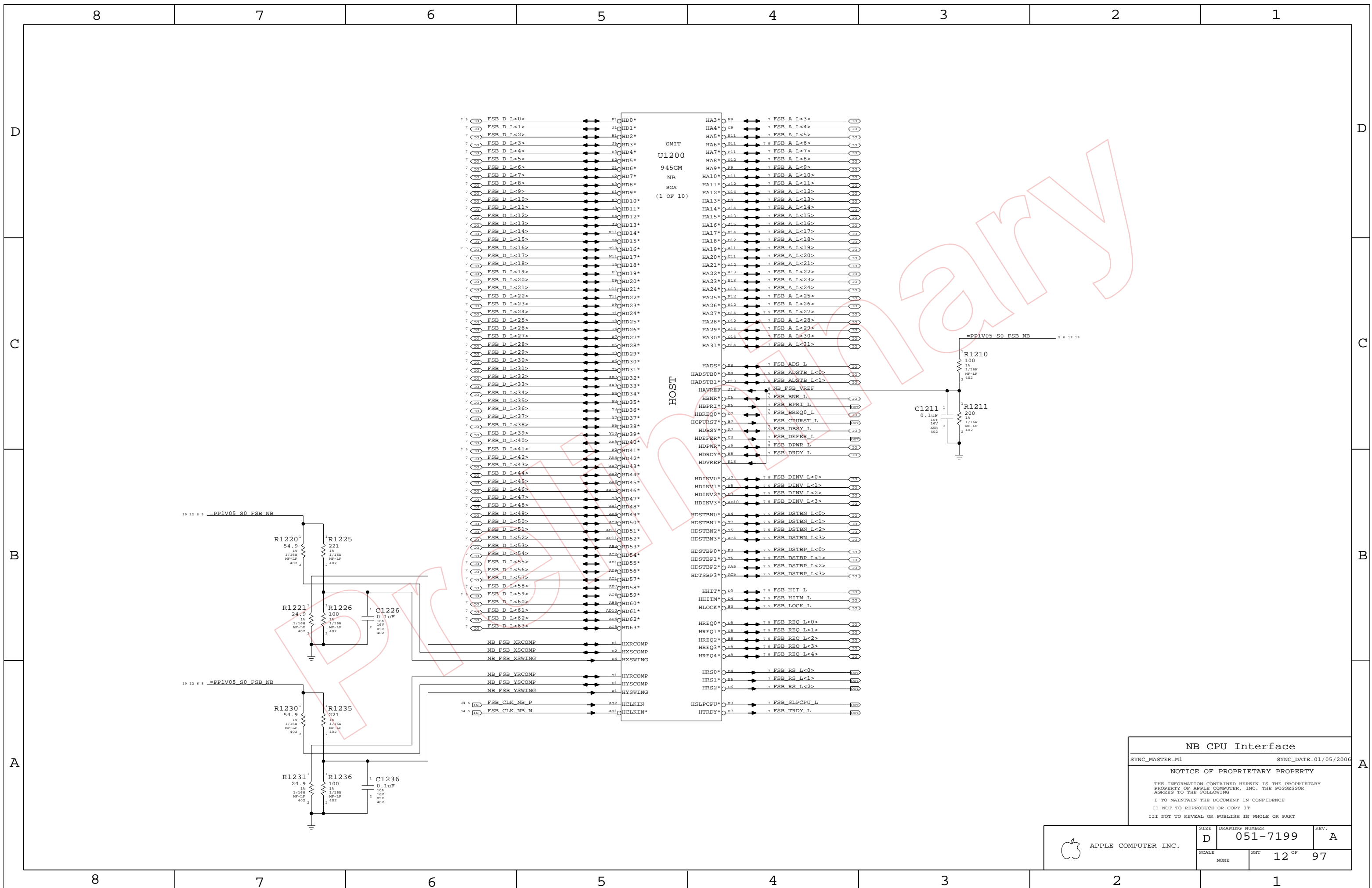
ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
 CONNECTOR'S FBO PIN.

DEVELOPMENT
 J1101
 52435-2872
 P-ST-SM
 29

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
 (DEBUG PORT ACTIVE)
 (DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
 (DEBUG PORT RESET)

CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 12 OF 97	

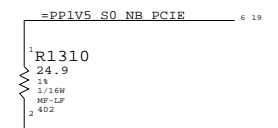
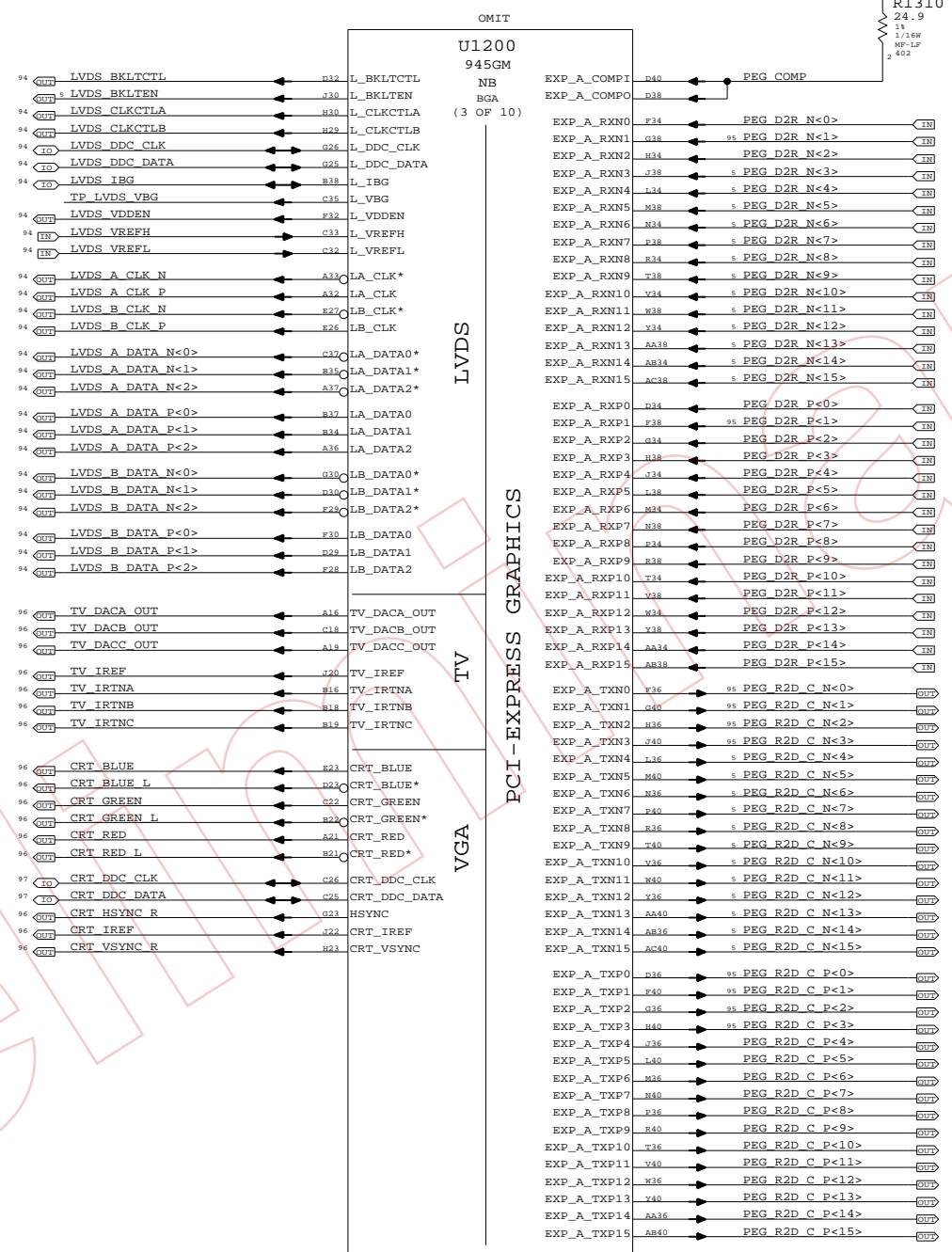
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function
 SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

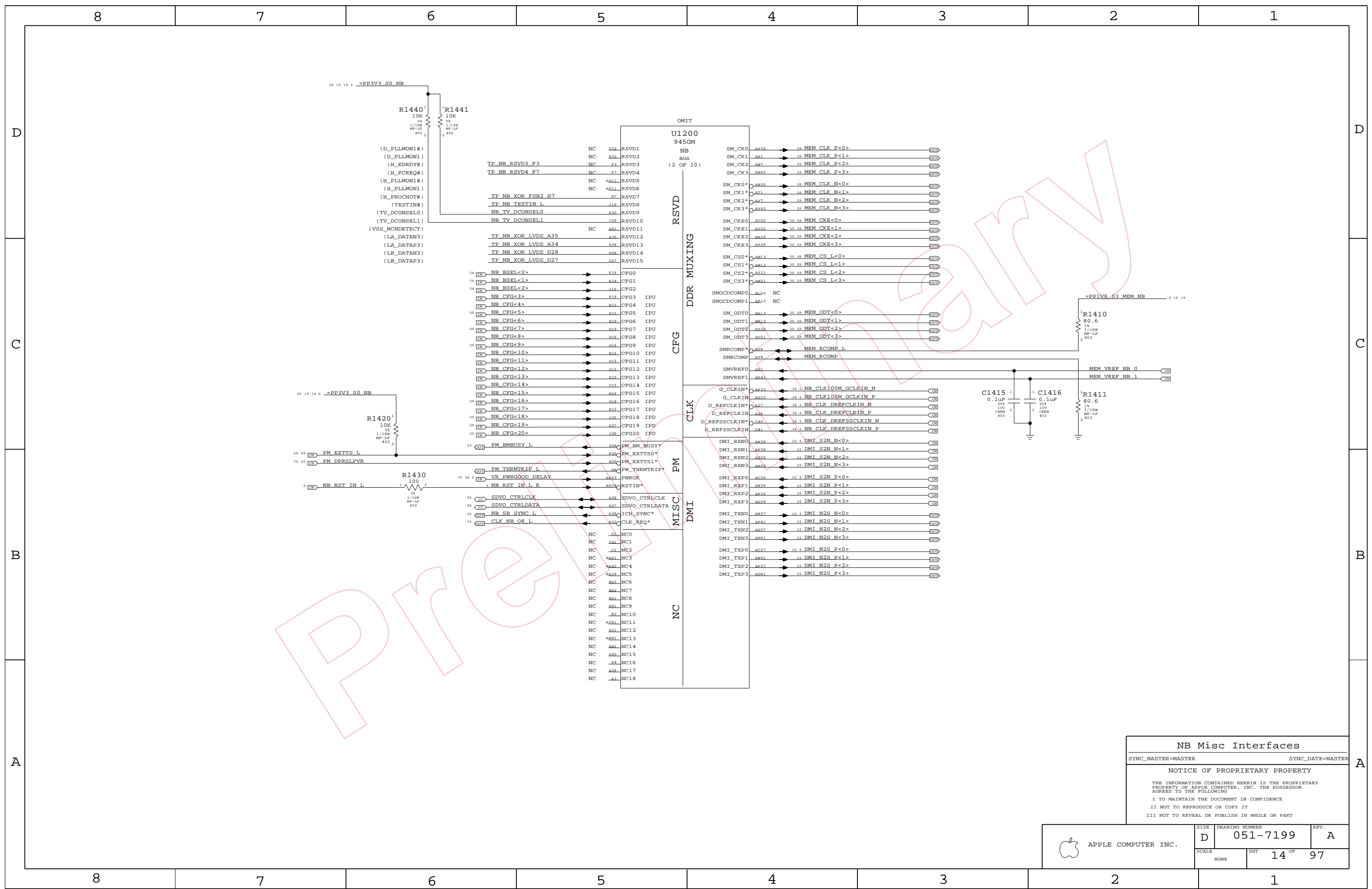
SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

Pre-release

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	D	051-7199	A
SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

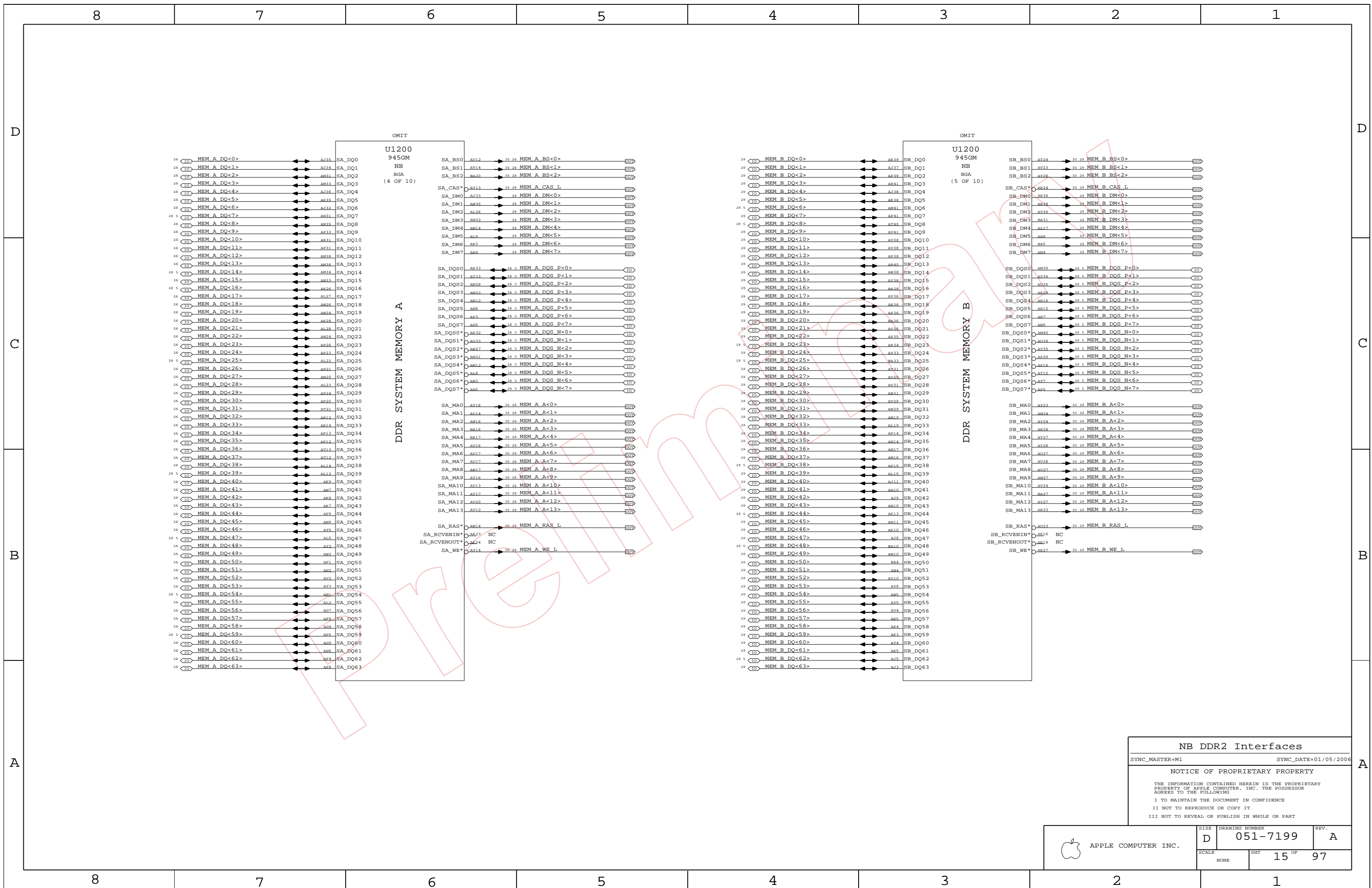
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	SCALE NONE	SHEET 14 OF 97	



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

NOTICE OF PROPRIETARY PROPERTY

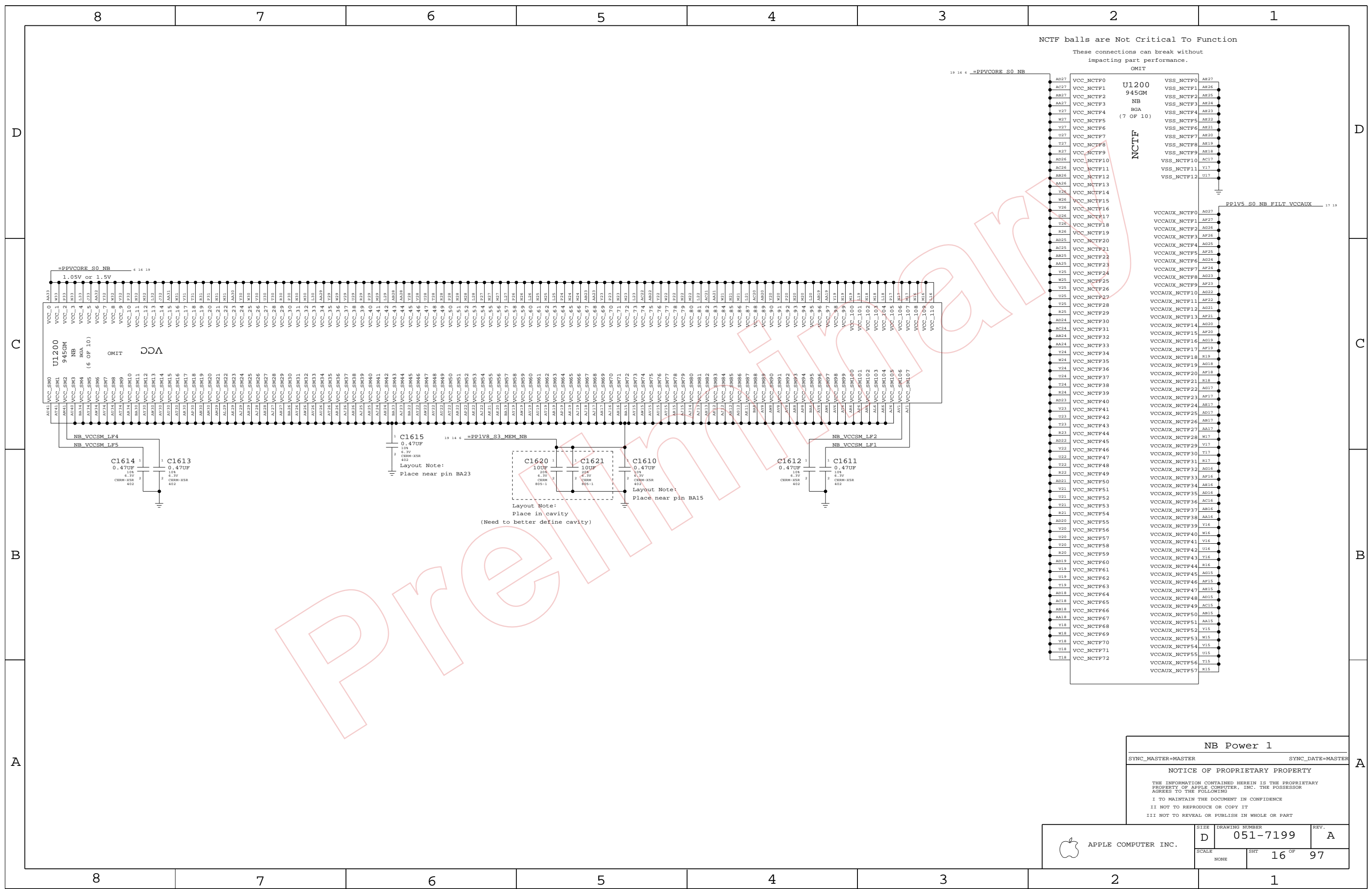
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	SCALE NONE	SHEET 15 OF 97	



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.
 OMIT

U1200
 945GM
 NB
 BGA
 (7 OF 10)
 NCTF

VCCAUX_NCTF0
 VCCAUX_NCTF1
 VCCAUX_NCTF2
 VCCAUX_NCTF3
 VCCAUX_NCTF4
 VCCAUX_NCTF5
 VCCAUX_NCTF6
 VCCAUX_NCTF7
 VCCAUX_NCTF8
 VCCAUX_NCTF9
 VCCAUX_NCTF10
 VCCAUX_NCTF11
 VCCAUX_NCTF12

VCC
 (6 OF 10)
 OMIT

NB VCCSM LP4
 NB VCCSM LP5

C1614
 0.47UF
 6.3V
 CERM-XSR
 402

C1613
 0.47UF
 6.3V
 CERM-XSR
 402

C1615
 0.47UF
 6.3V
 CERM-XSR
 402
 Layout Note:
 Place near pin BA23

C1620
 10UF
 6.3V
 CERM-XSR
 805-1

C1621
 10UF
 6.3V
 CERM-XSR
 805-1
 Layout Note:
 Place in cavity
 (Need to better define cavity)

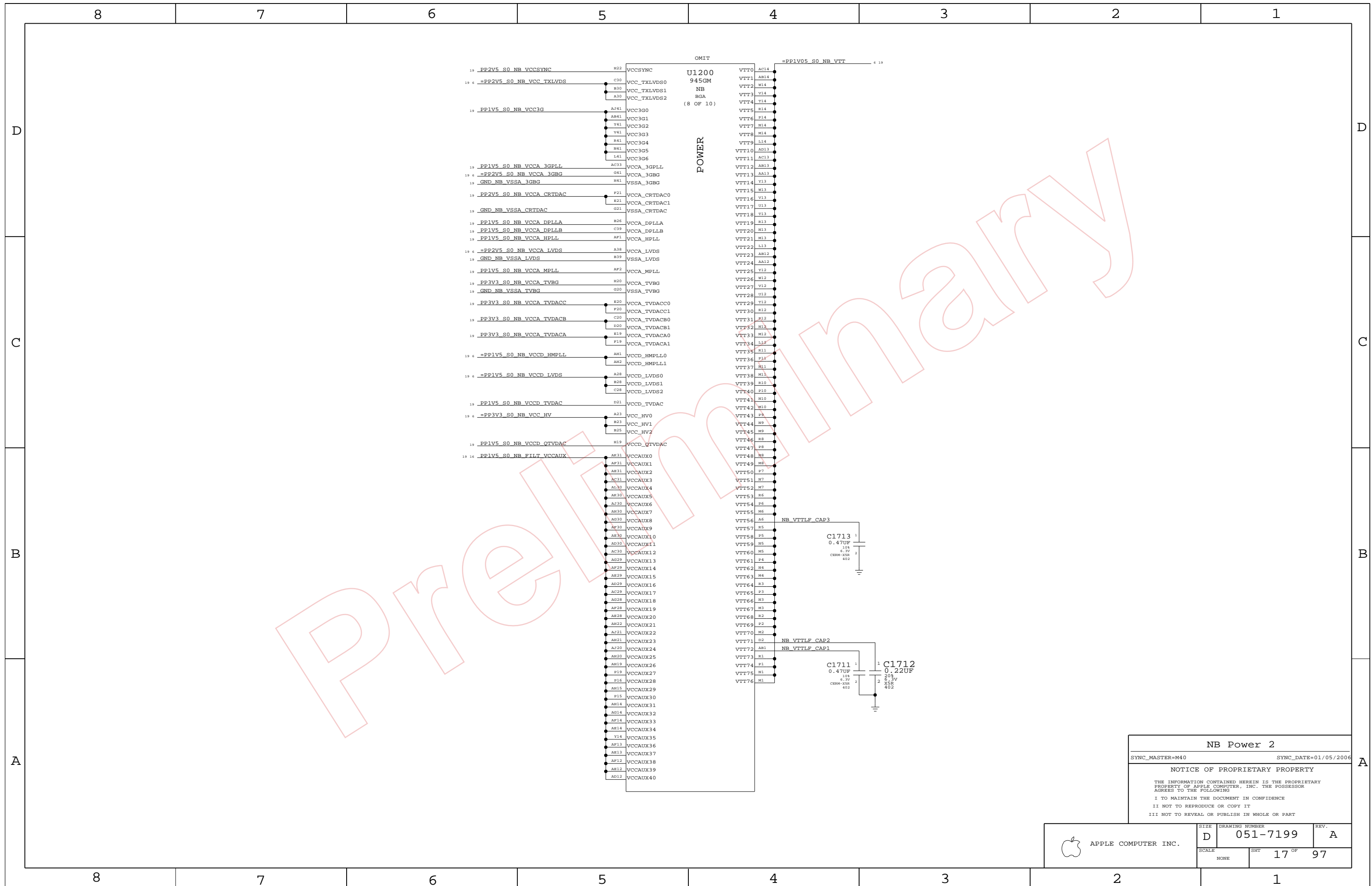
C1610
 0.47UF
 6.3V
 CERM-XSR
 402
 Layout Note:
 Place near pin BA15

C1612
 0.47UF
 6.3V
 CERM-XSR
 402

C1611
 0.47UF
 6.3V
 CERM-XSR
 402

NB Power 1
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	16 OF	97
NONE			



NB Power 2

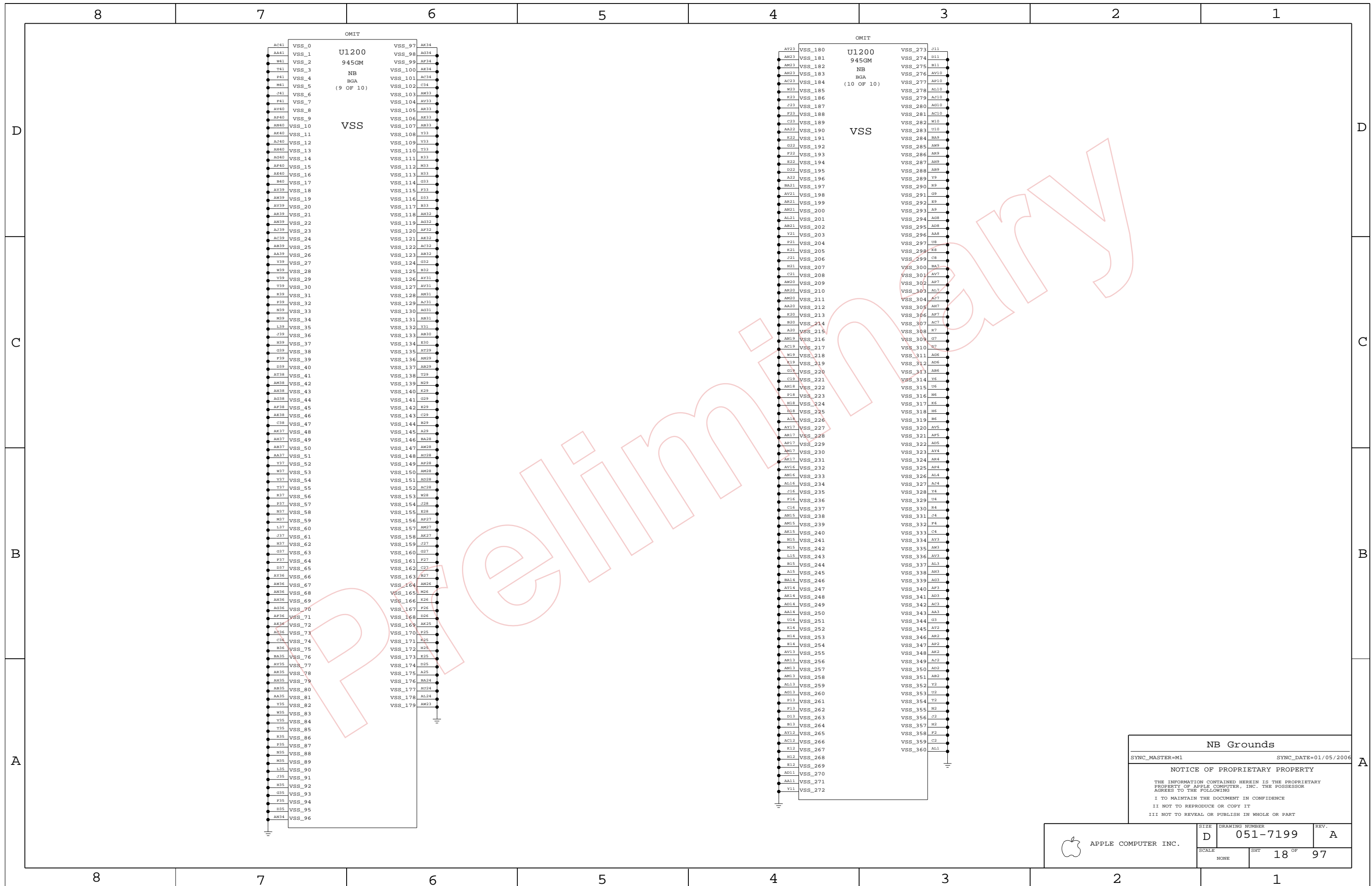
SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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	D	051-7199	A
SCALE	SHT	17 OF 97	
NONE			



NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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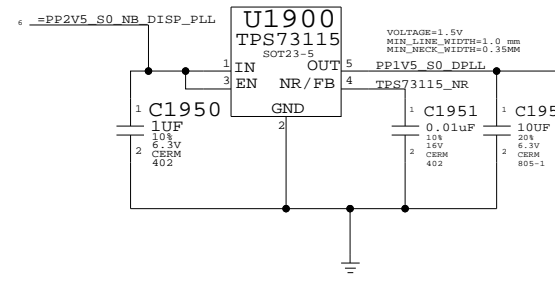
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 18 OF 97	

Power Interface

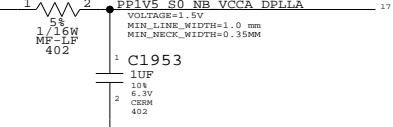
These are the power signals that leave the NB "block"

- PP1V05_S0_FSB_NB 5 6 12
- PPVCORE_S0_NB 6 16 19
- PP1V05_S0_NB_VTT 6 17 19
- PP1V5_S0_NB 6 19
- PP1V5_S0_NB_PCIE 6 13
- PP1V5_S0_NB_PLL 6 19
- PP1V5_S0_NB_TVDAC 6 19
- PP1V5_S0_NB_VCCD_HMPLL 6 17
- PP1V5_S0_NB_VCCD_LVDS 6 17 19
- PP1V5_S0_NB_VCCAUX 6 19
- PP1V8_S3_MEM_NB 6 14 16 19
- PP2V5_S0_NB_VCCSYNC 19 6
- PP2V5_S0_NB_VCC_TXLVDS 6 17 19
- PP2V5_S0_NB_VCCA_3GBG 6 17 19
- PP2V5_S0_NB_VCCA_LVDS 6 17 19
- PP3V3_S0_NB 6 14 20
- PP3V3_S0_NB_VCC_HV 6 17 19
- PP5V_S0_NB_TVDAC 6 19

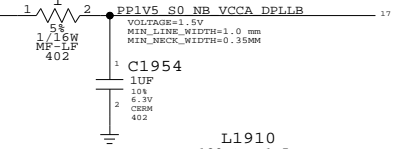
MCH DISPLAY PLL POWER LDO



MCH VCCA_DPLL_A FILTER



GMCH VCCA_DPLL_B FILTER



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 2.5V PWR)

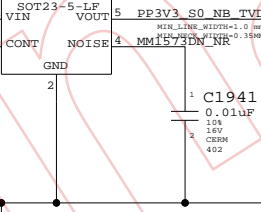


FILTERING REQUIRED FOR

INTEGRATED GFX (PG. 333)



U1901 MM157



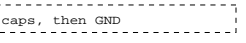
MCH VCCA_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)



MCH VCCA_CRITDAC BYPASS

(MCH CRITDAC ANALOG 2.5V PWR)



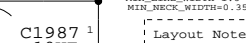
MCH VCCA_TV DAC FILTER

(MCH TV OUT CHANNEL A 3.3V PWR)



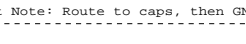
MCH VCCA_TV DAC FILTER

(MCH TV OUT CHANNEL B 3.3V PWR)



MCH VCCA_TV DAC FILTER

(MCH TV OUT CHANNEL C 3.3V PWR)

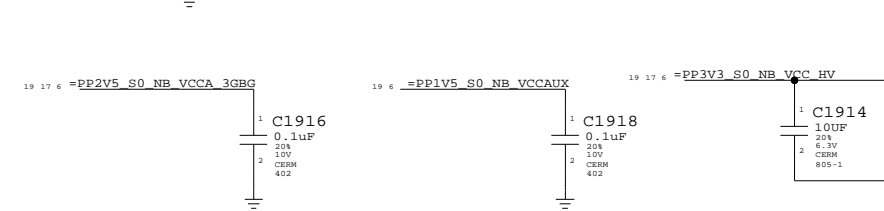
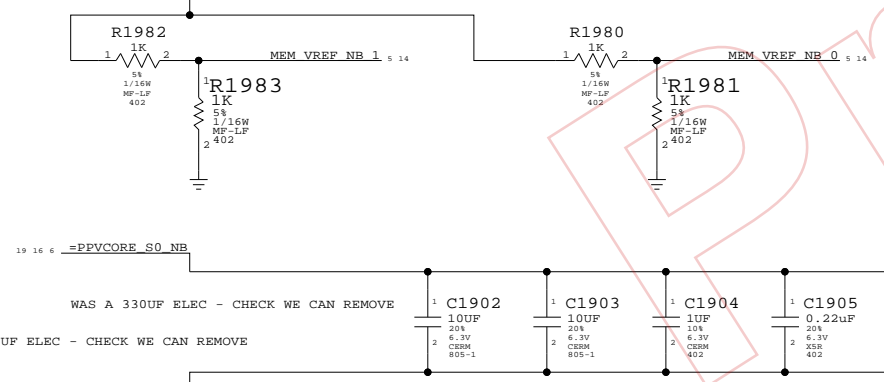
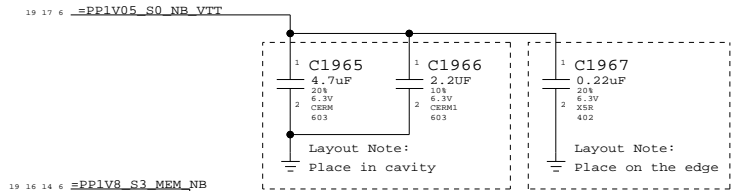
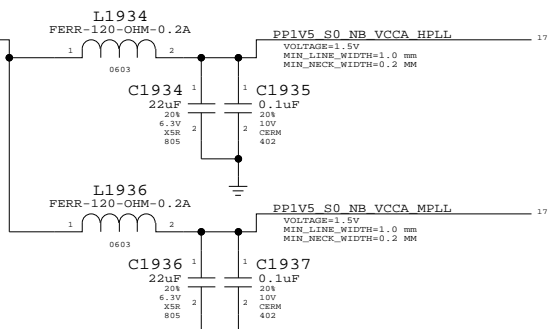


MCH VCCA_TV BKG FILTER

(MCH TV DAC BAND GAP 3.3V PWR)



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge



Layout Note:
Place L and C close to MCH

Layout Note:
3GPLL 10uF cap should be placed in cavity

Layout Note:
PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

Layout Note:
10uF caps should be close to MCH on opposite side.

Layout Note:
This 0.1uF cap should be within 5 mm of NB edge

Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
These 8 caps should be within 6.35 mm of NB edge

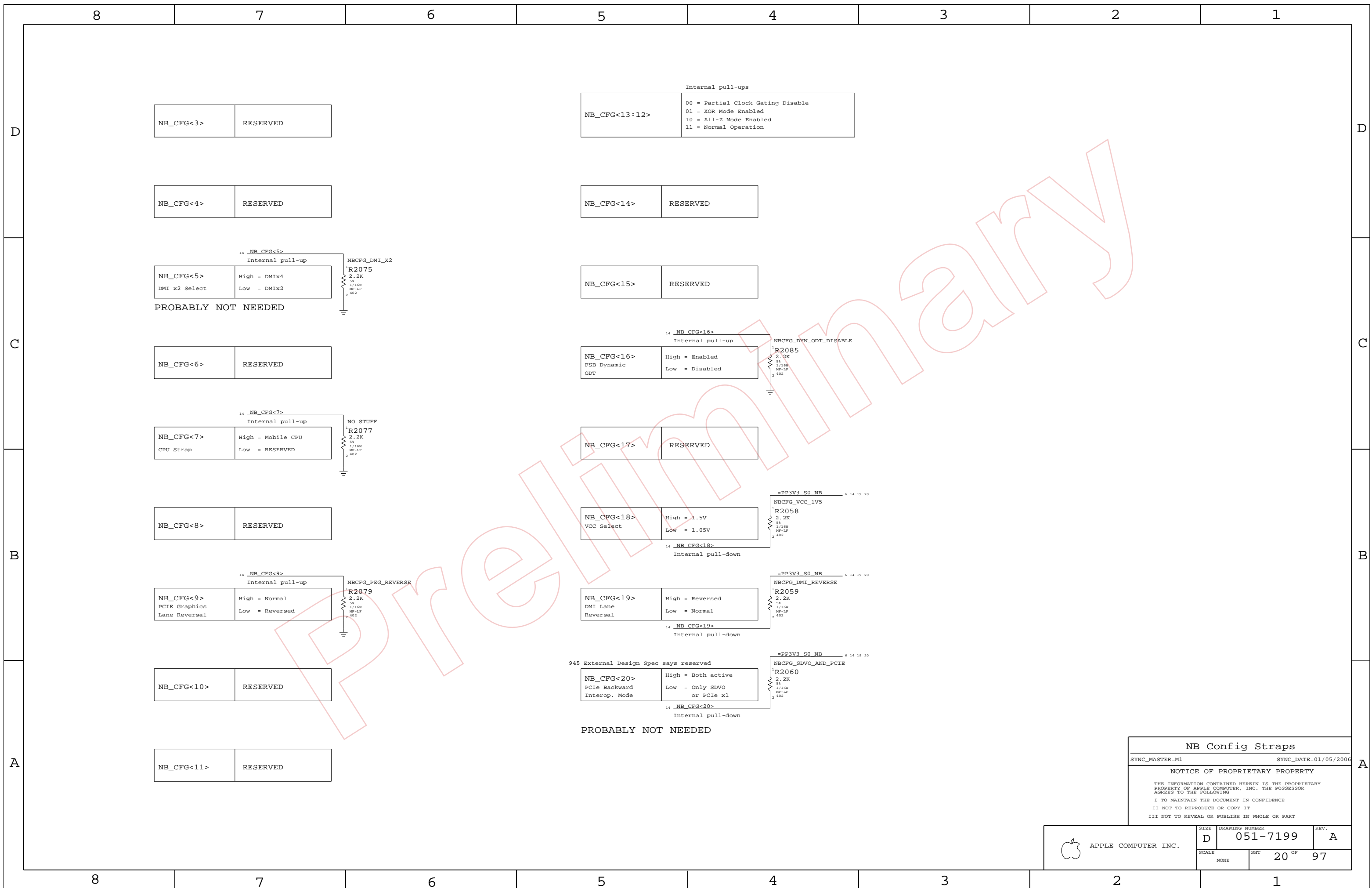
Layout Note:
Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	19 OF 97	
NONE			



NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

NB_CFG<10>	RESERVED
------------	----------

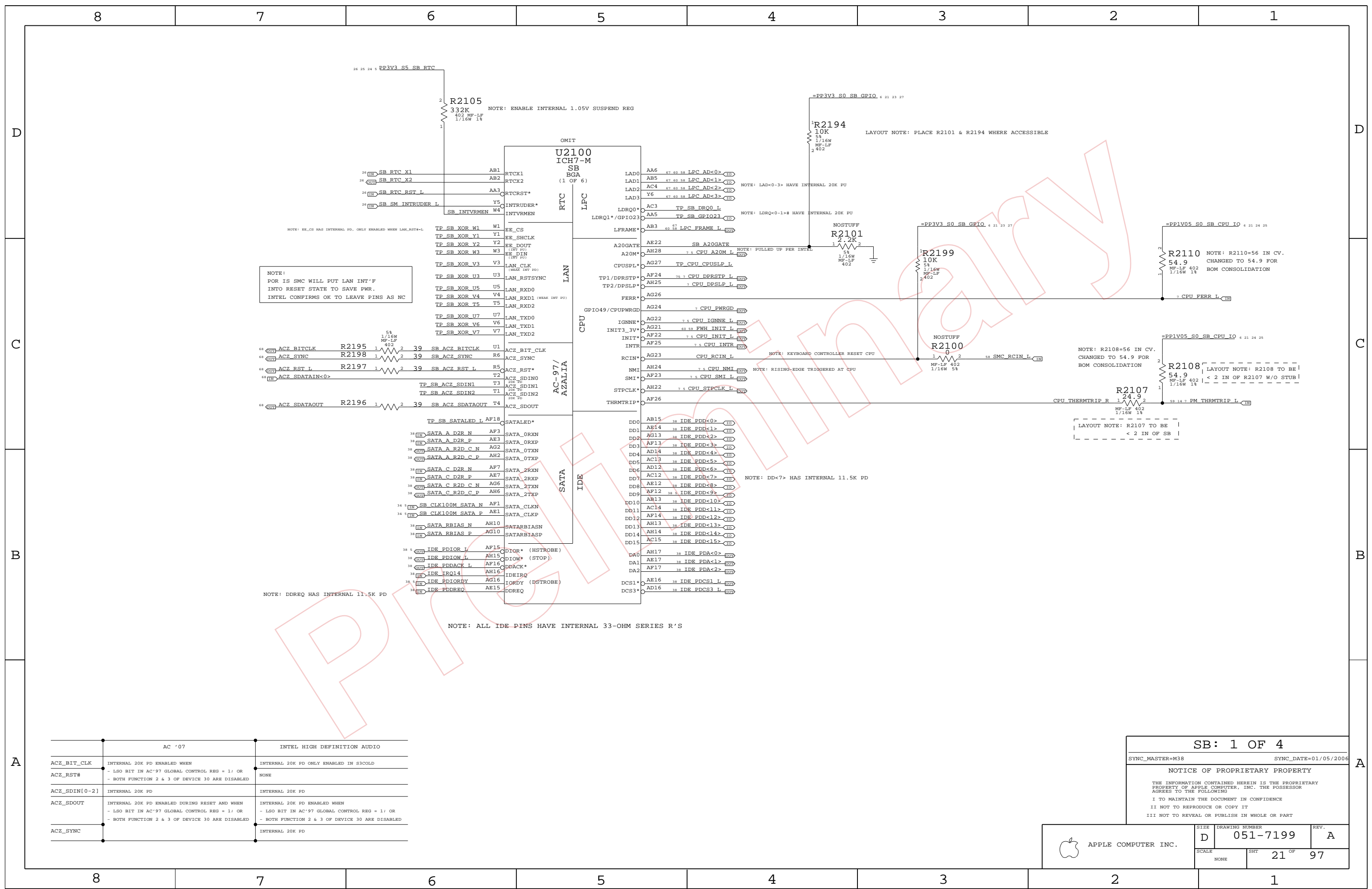
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

NB Config Straps
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	D	051-7199	A
SCALE	SHT	20 OF 97	
NONE			



NOTE:
POR IS SMC WILL PUT LAN INT'F INTO RESET STATE TO SAVE PWR. INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

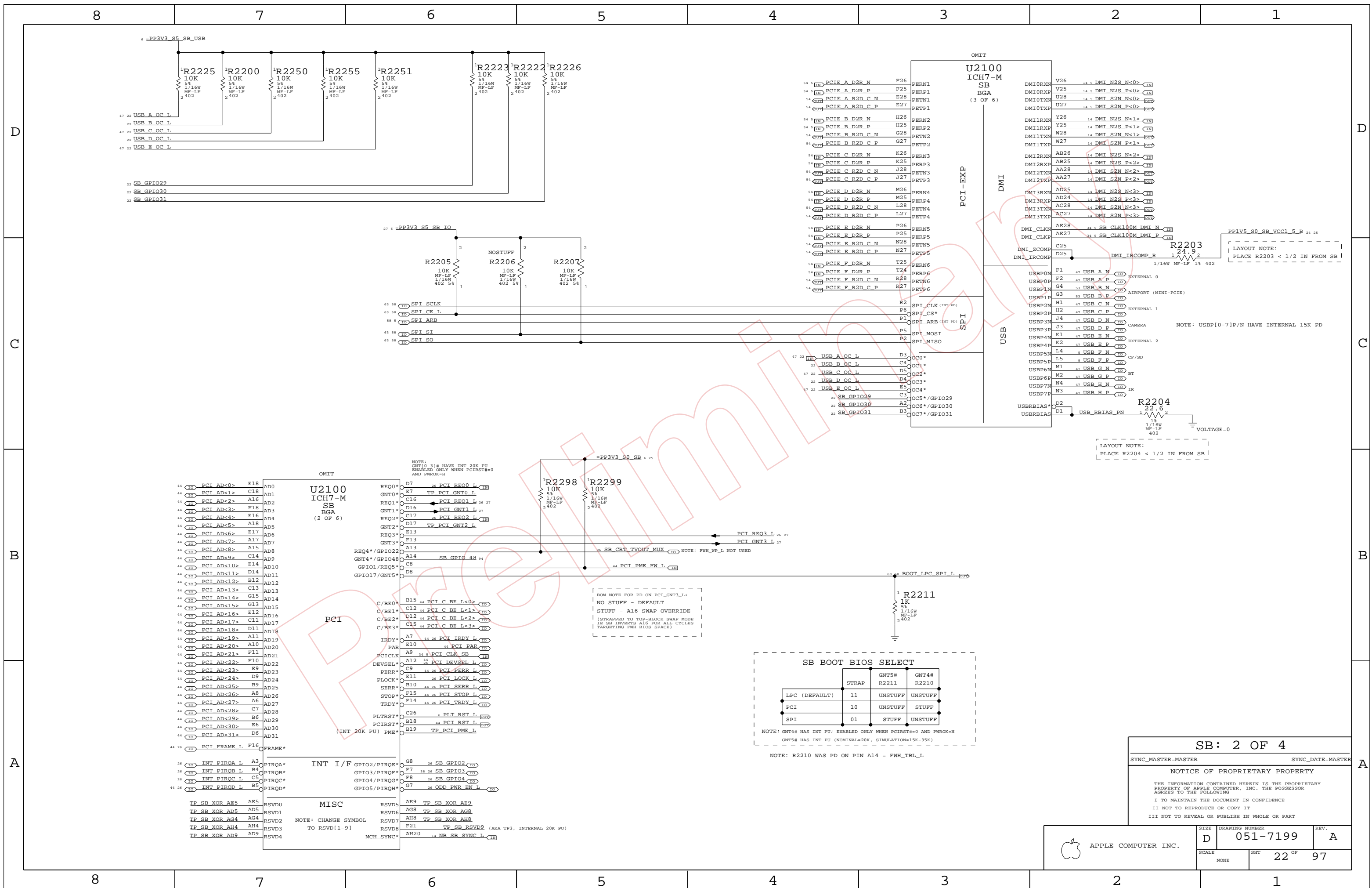
NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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SIZE	D	DRAWING NUMBER	051-7199	REV.	A
SCALE	NONE	SHT	21 OF 97		



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SCALE	SHT	22 OF	97
NONE			

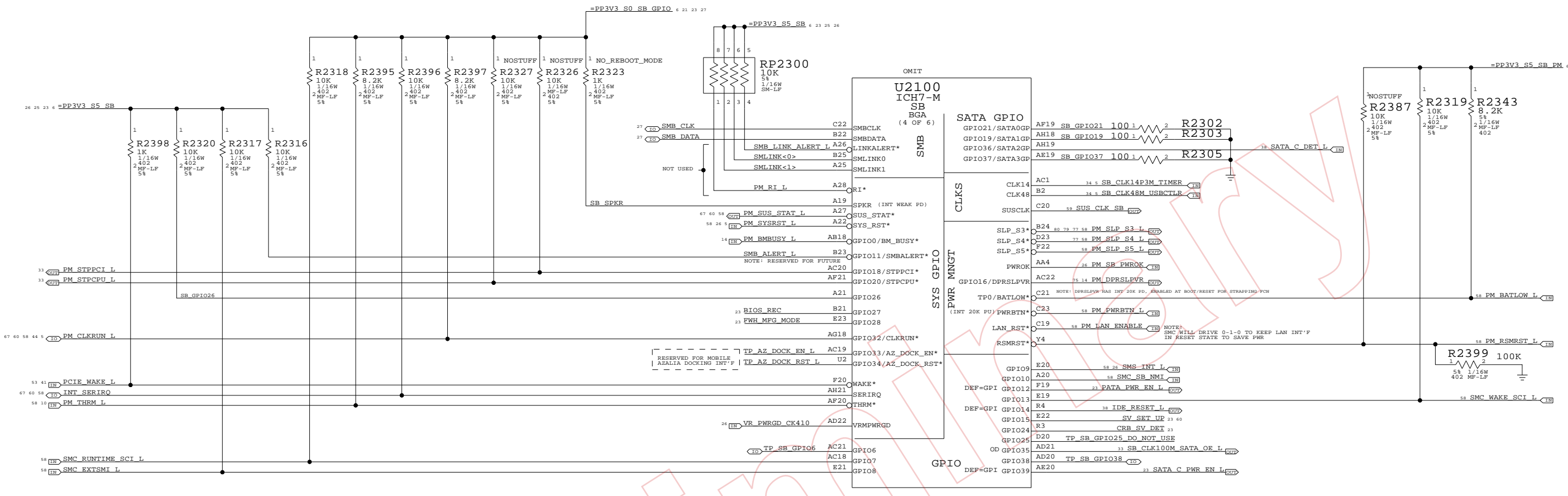
D

C

B

A

NOTE FOR R2323 (DEF=NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

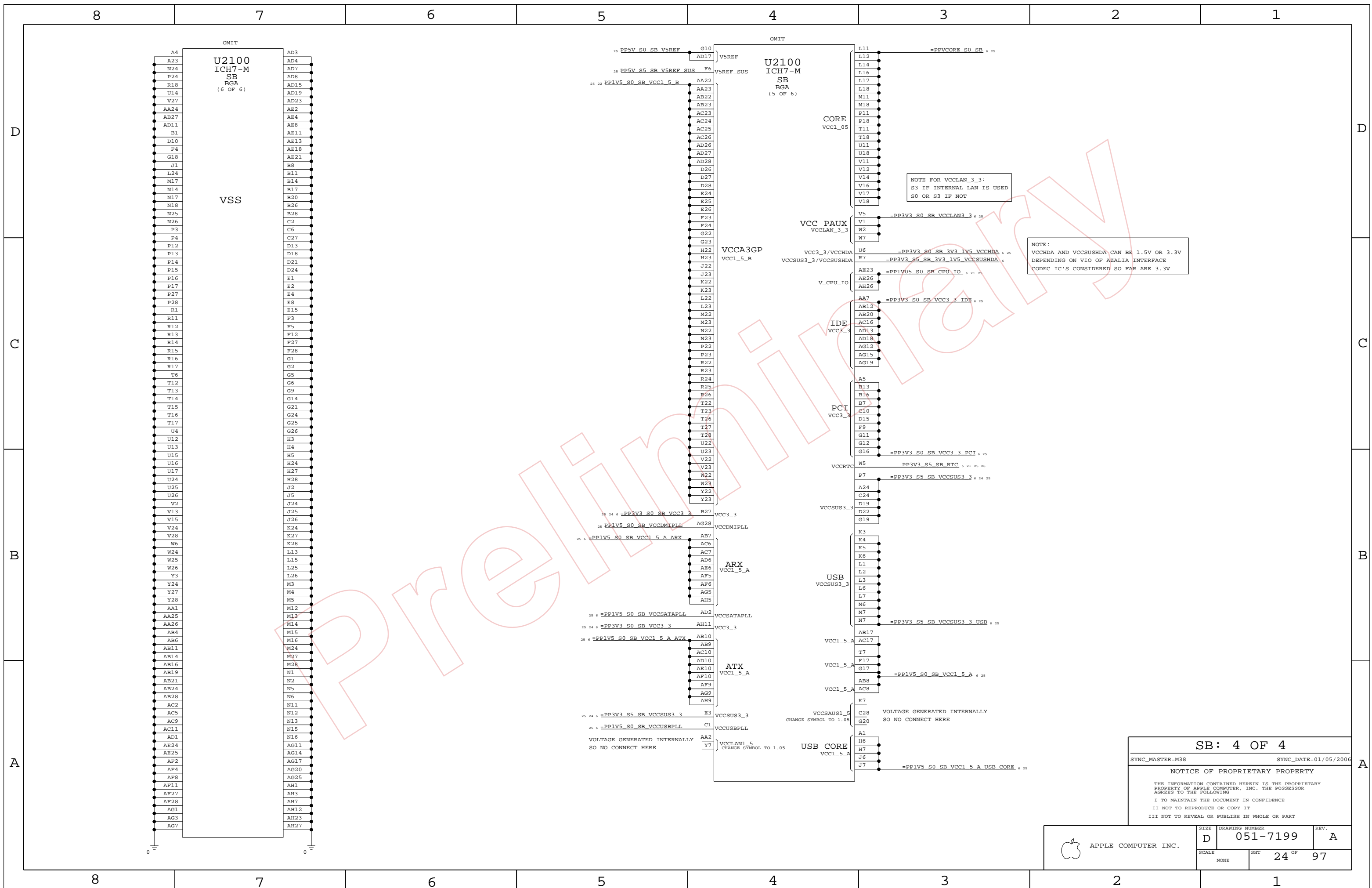


NOTE FOR GPIO25:
 * HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 * CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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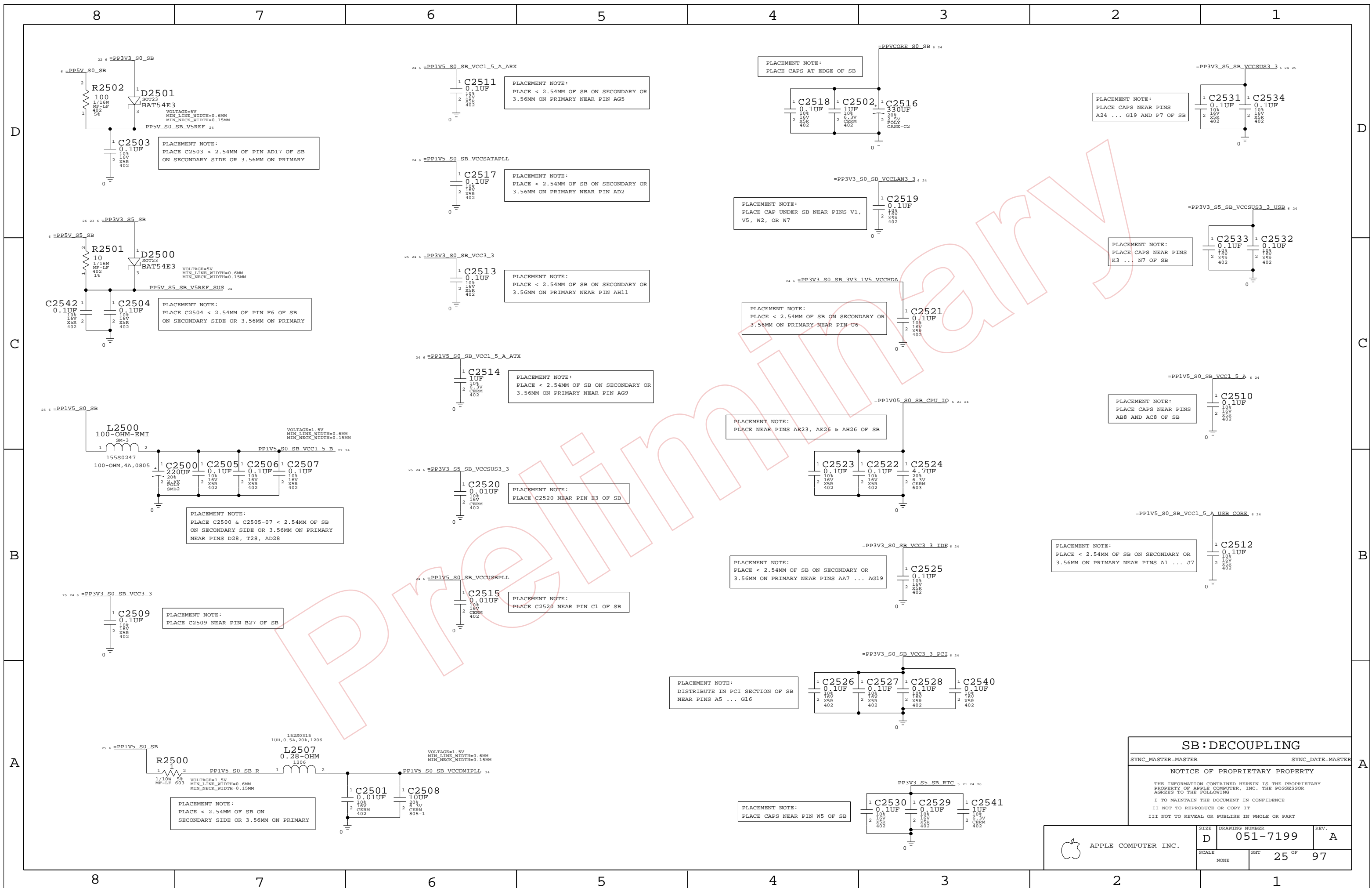
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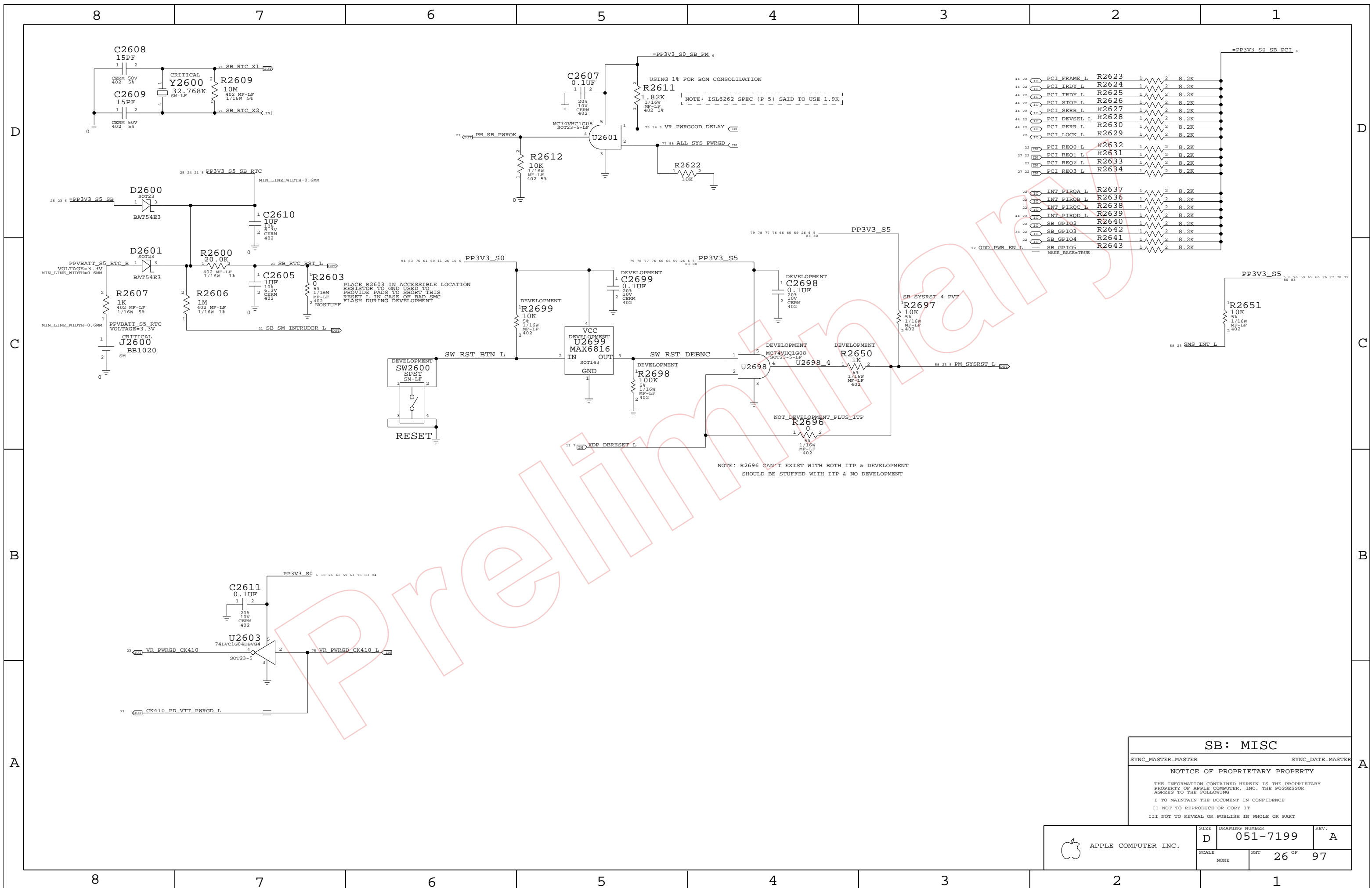
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 24 OF 97	



SB: DECOUPLING
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	25 OF	97
NONE			



SB: MISC
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7199	A
SCALE	SHT	26 OF	97
NONE			

8

7

6

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3

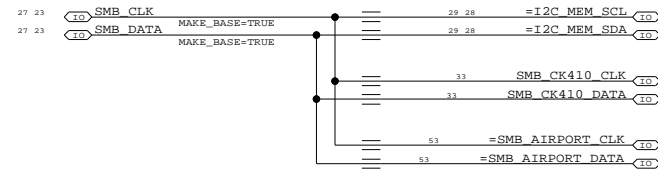
2

1

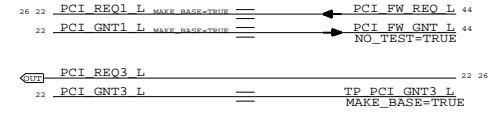
D

D

SB I2C BUSSES

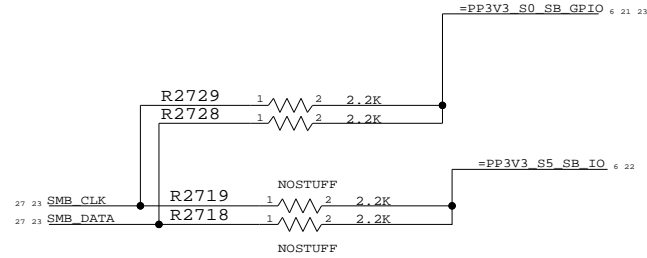


PCI CONTROL



C

C



B

B

Preliminary

A

A

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
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NONE			

8

7

6

5

4

3

2

1

Page Notes

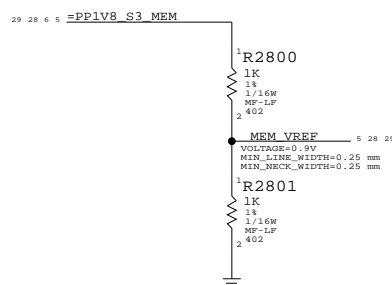
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

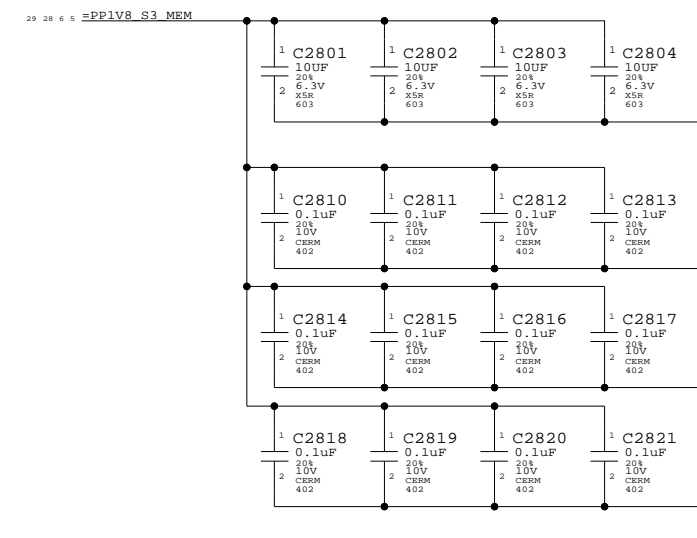
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 28 OF 97	

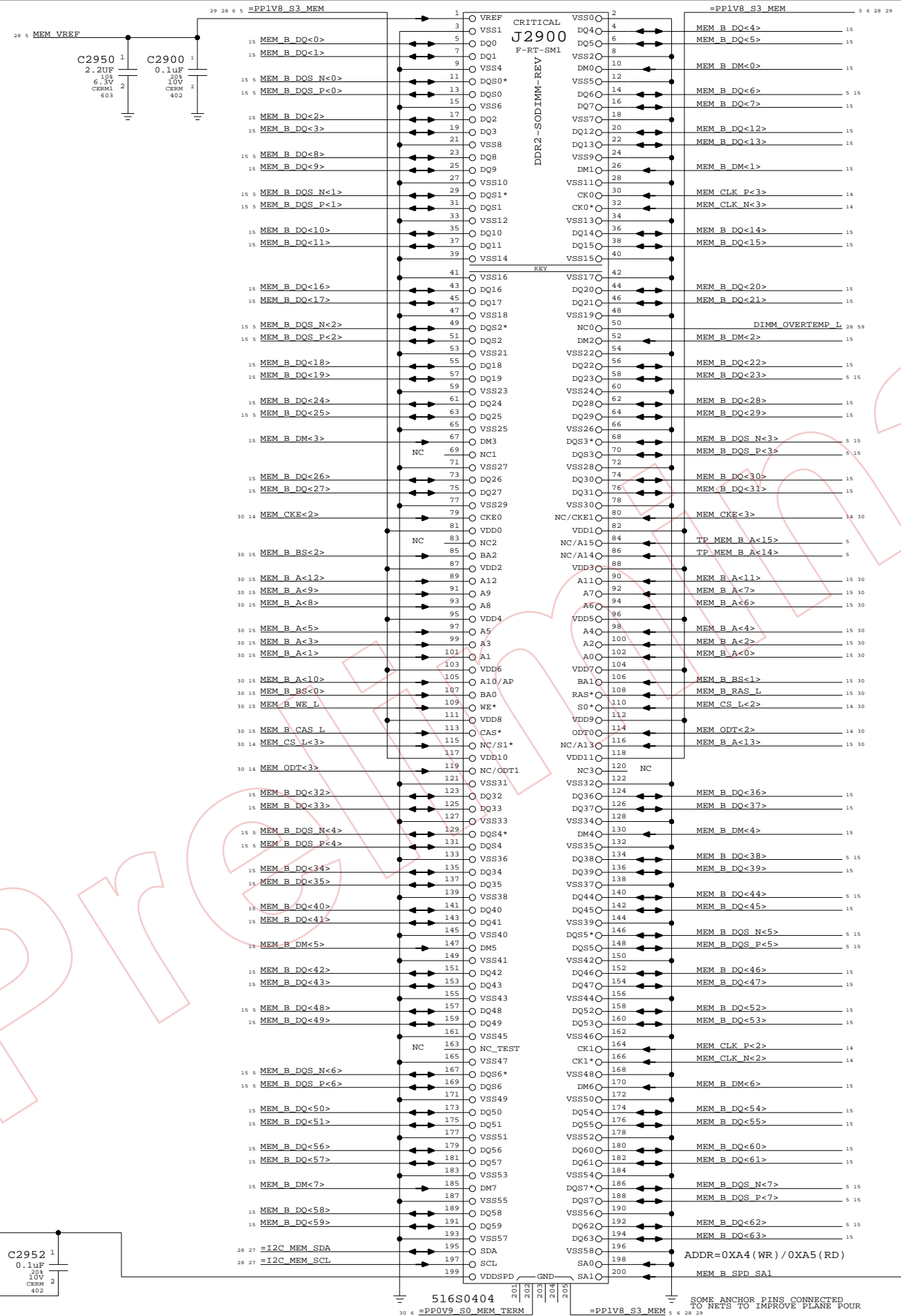
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

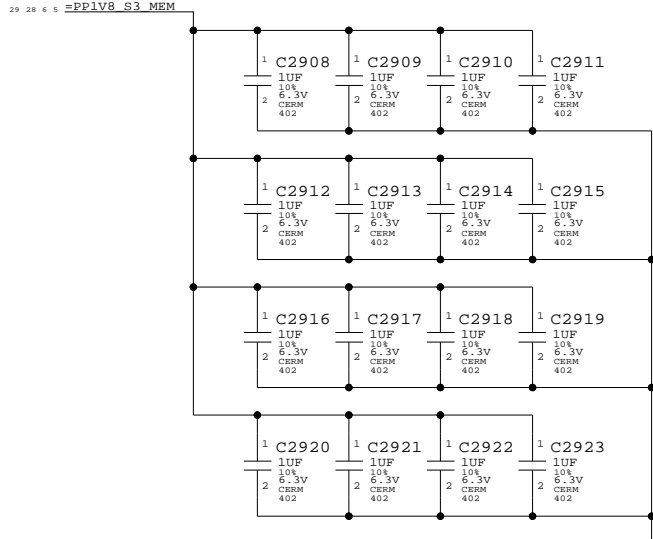
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

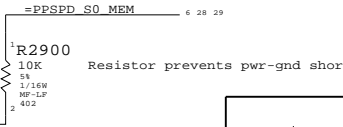
NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)

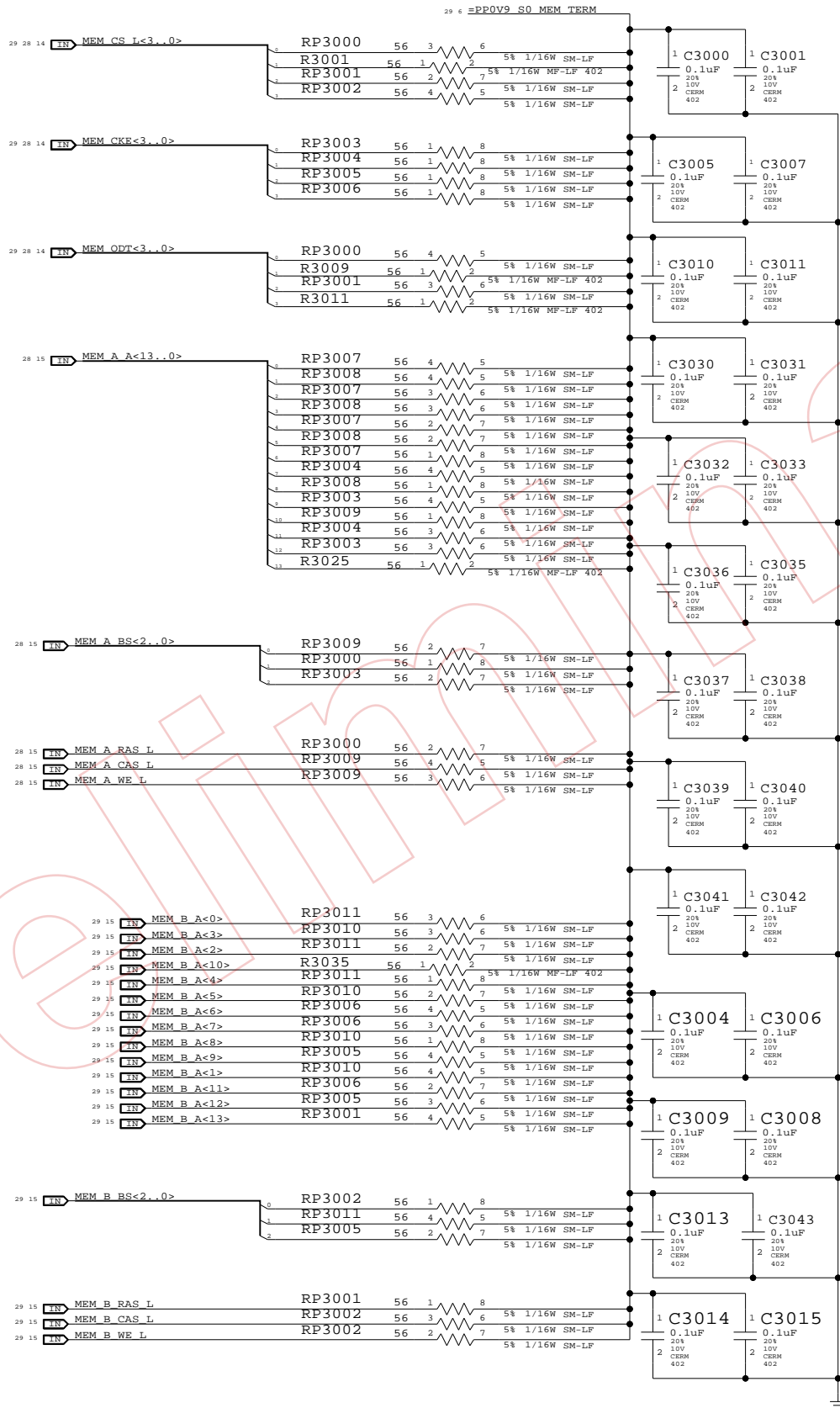


DDR2 SO-DIMM Connector B	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 29 OF 97	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



PRELIMINARY

Memory Active Termination

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	D	051-7199	A
SCALE	SHT	30 OF 97	
NONE			

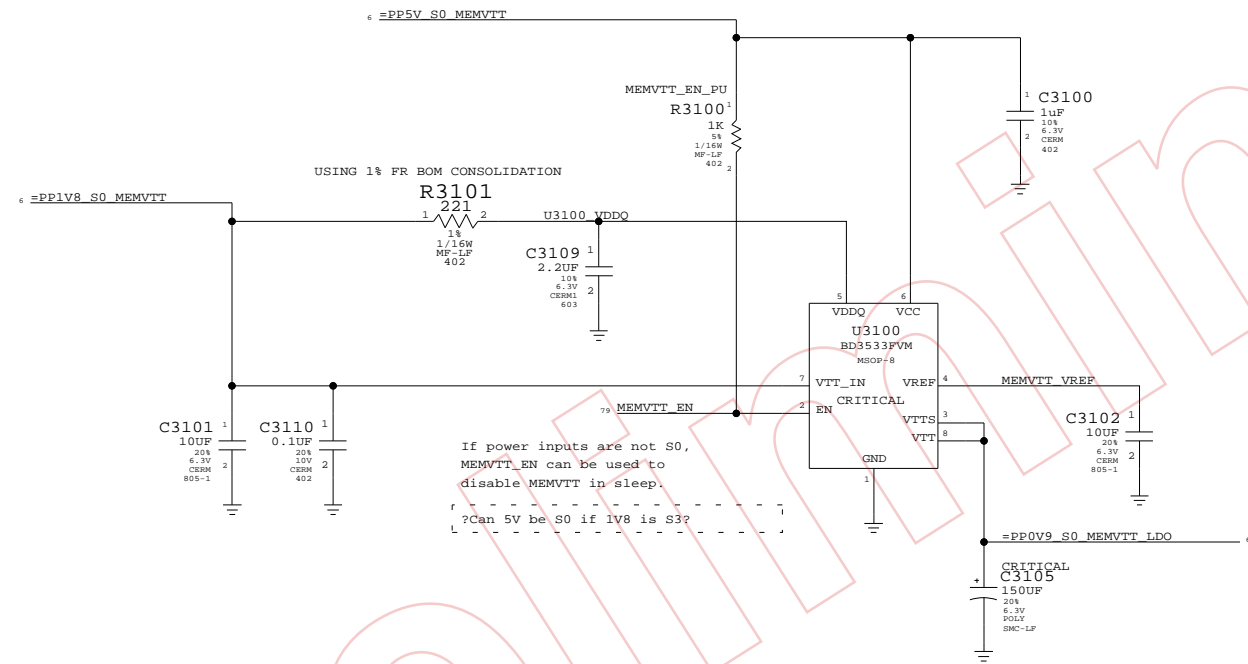
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Preliminary

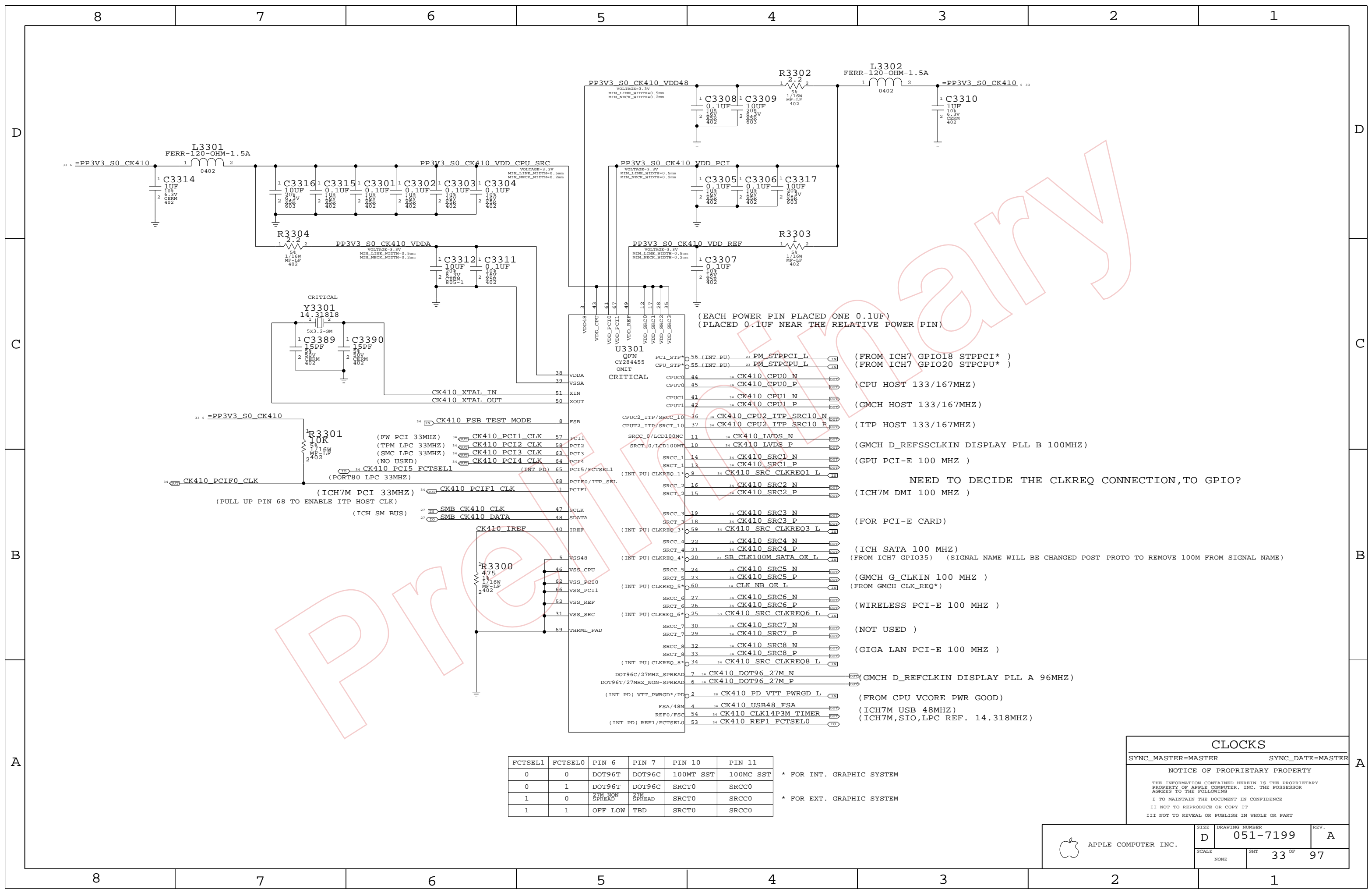
Memory Vtt Supply

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	D	051-7199	A
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) PM_STPPCI L (FROM ICH7 GPIO18 STPPCI*)
- 55 (INT PU) PM_STPCPU L (FROM ICH7 GPIO20 STPCPU*)
- 34 CK410 CPU0 N (CPU HOST 133/167MHZ)
- 34 CK410 CPU0 P (CPU HOST 133/167MHZ)
- 34 CK410 CPU1 N (GMCH HOST 133/167MHZ)
- 34 CK410 CPU1 P (GMCH HOST 133/167MHZ)
- 34 CK410 CPU2 ITP_SRC10_N (ITP HOST 133/167MHZ)
- 34 CK410 CPU2 ITP_SRC10_P (ITP HOST 133/167MHZ)
- 34 CK410 LVDS N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 34 CK410 LVDS P (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 34 CK410 SRC1 N (GPU PCI-E 100 MHZ)
- 34 CK410 SRC1 P (GPU PCI-E 100 MHZ)
- 34 CK410 SRC2 N (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 34 CK410 SRC2 P (ICH7M DMI 100 MHZ)
- 34 CK410 SRC3 N (FOR PCI-E CARD)
- 34 CK410 SRC3 P (FOR PCI-E CARD)
- 34 CK410 SRC4 N (ICH SATA 100 MHZ)
- 34 CK410 SRC4 P (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 34 CK410 SRC5 N (GMCH G_CLKIN 100 MHZ)
- 34 CK410 SRC5 P (FROM GMCH CLK_REQ*)
- 34 CK410 SRC6 N (WIRELESS PCI-E 100 MHZ)
- 34 CK410 SRC6 P (WIRELESS PCI-E 100 MHZ)
- 34 CK410 SRC7 N (NOT USED)
- 34 CK410 SRC7 P (NOT USED)
- 34 CK410 SRC8 N (GIGA LAN PCI-E 100 MHZ)
- 34 CK410 SRC8 P (GIGA LAN PCI-E 100 MHZ)
- 34 CK410 SRC_CLKREQ3 L (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ3 P (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ4 L (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ4 P (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ5 L (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ5 P (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ6 L (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ6 P (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ8 L (FROM CPU VCORE PWR GOOD)
- 34 CK410 SRC_CLKREQ8 P (FROM CPU VCORE PWR GOOD)
- 34 CK410 DOT96 27M N (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 34 CK410 DOT96 27M P (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 34 CK410 PD_VTT_PWRGD L (FROM CPU VCORE PWR GOOD)
- 34 CK410 PD_VTT_PWRGD P (FROM CPU VCORE PWR GOOD)
- 34 CK410 USB48_FSA (ICH7M USB 48MHZ)
- 34 CK410 CLK14P3M_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 34 CK410 REF1_FCTSELO (ICH7M, SIO, LPC REF. 14.318MHZ)

FCTSEL1	FCTSELO	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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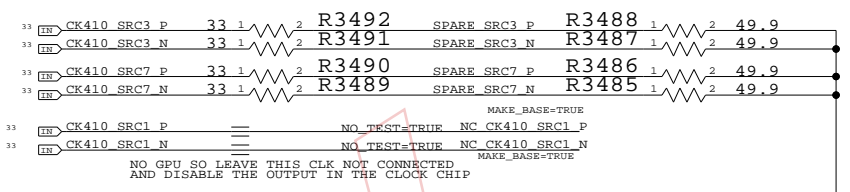
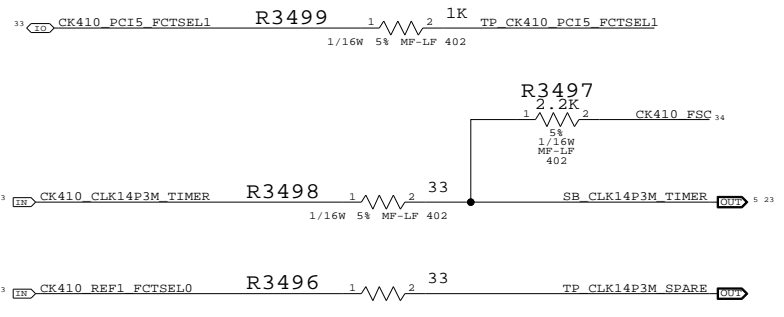
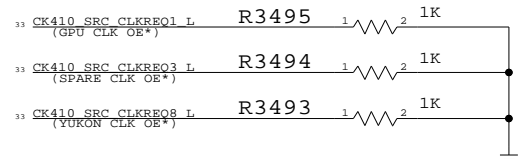
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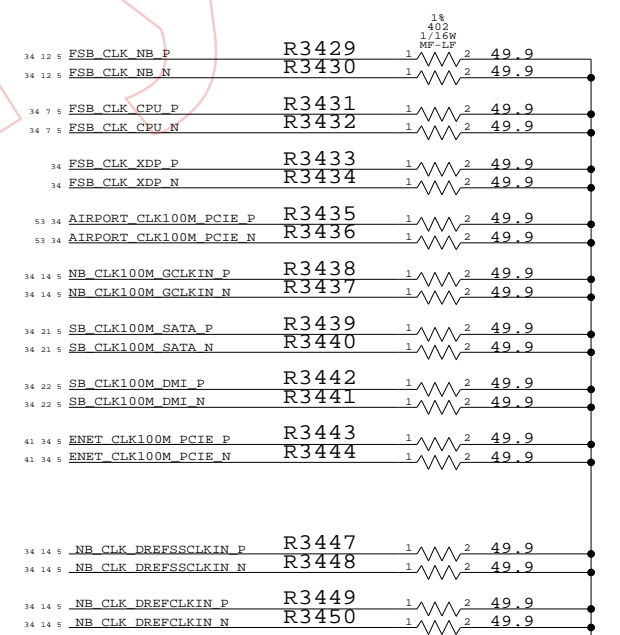
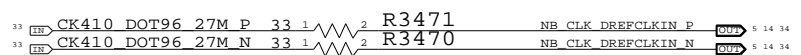
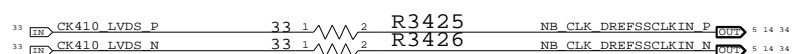
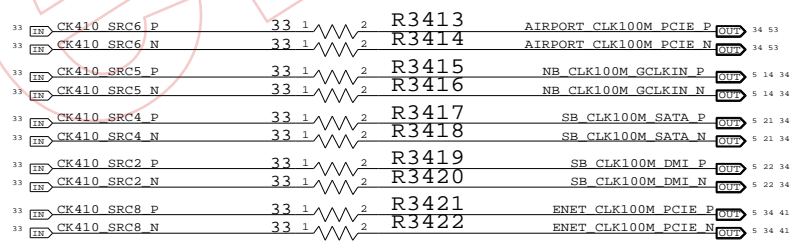
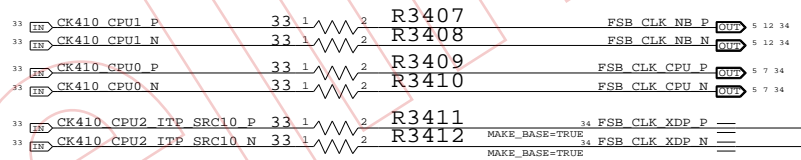
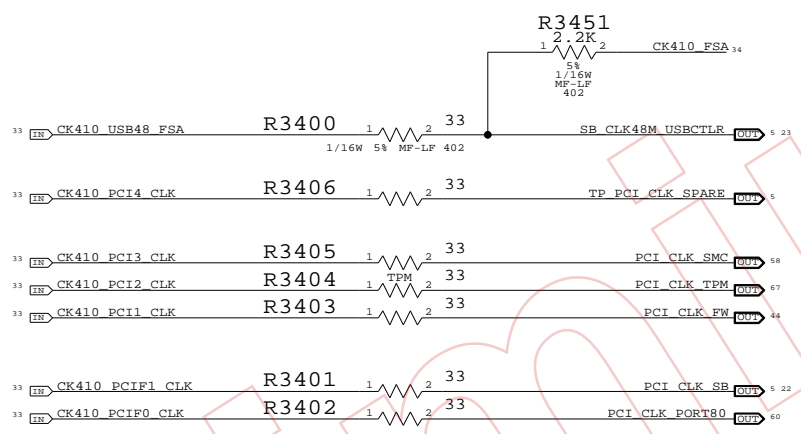
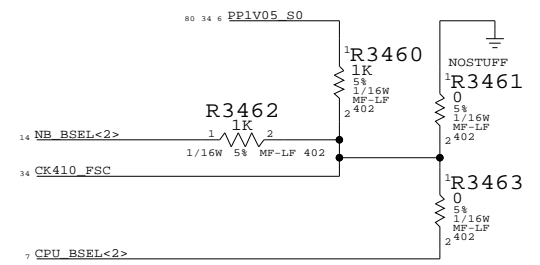
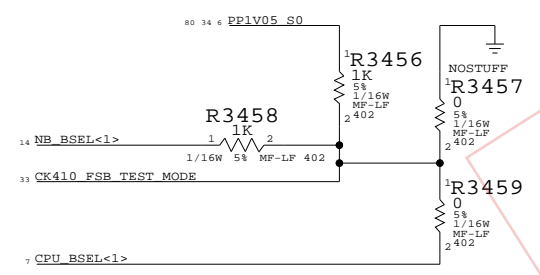
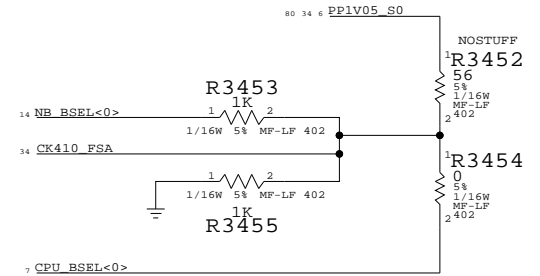
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	NONE	SHT	33 OF 97

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3452 R3453 R3454 R3455	R3456 R3457 R3458 R3459
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3456 R3457 R3458 R3459
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3454 R3455	R3456 R3457 R3458 R3459



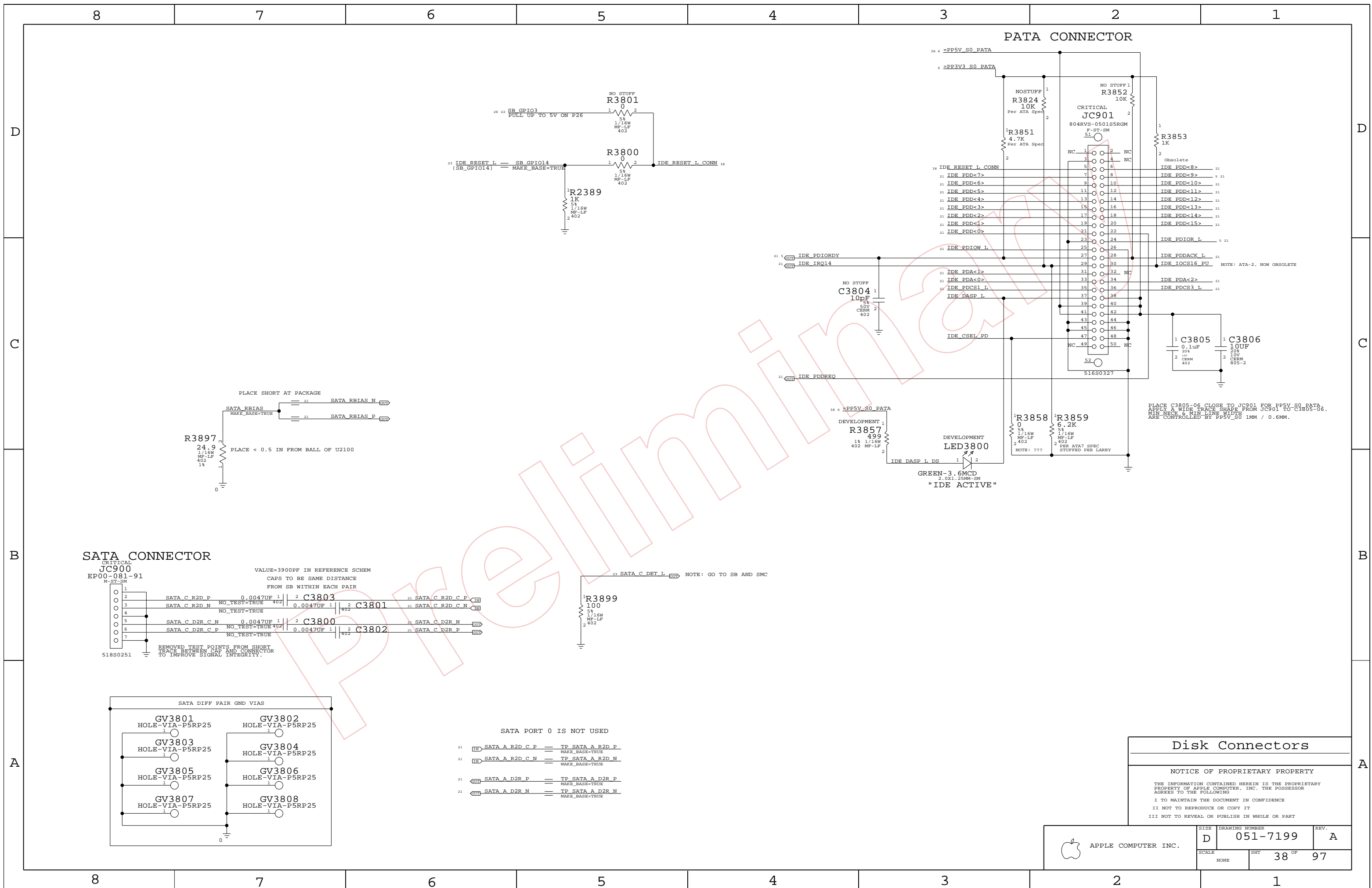
CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	34 OF 97	
NONE			



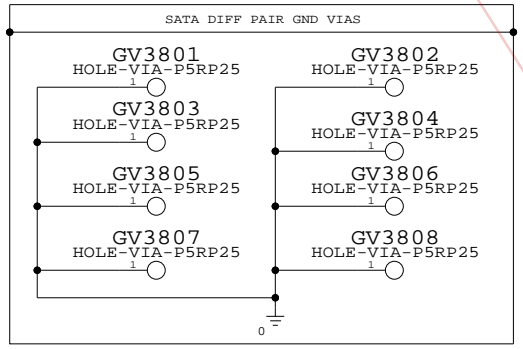
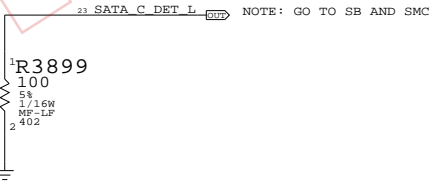
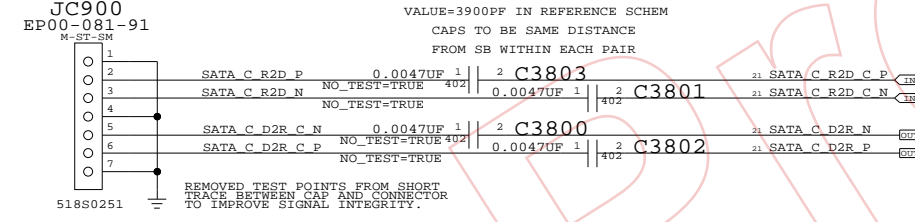
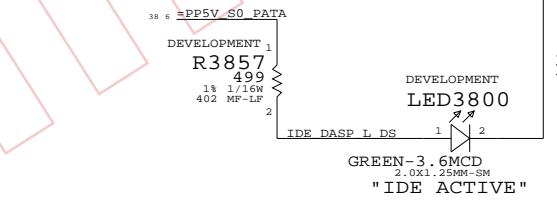
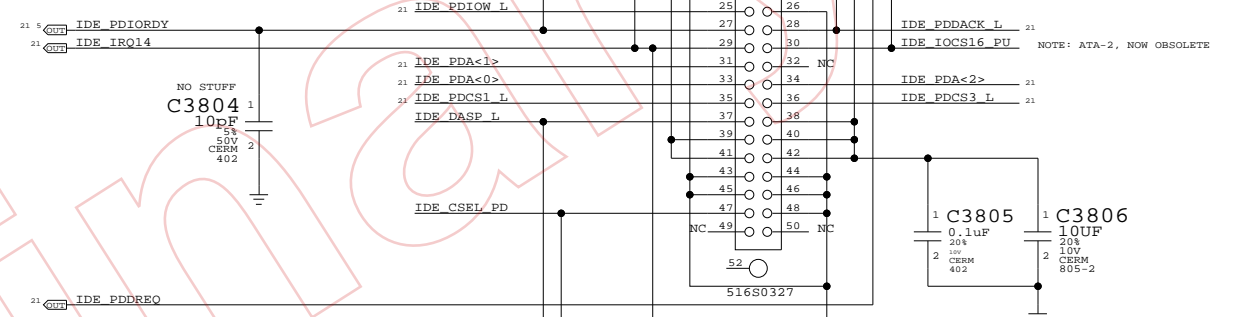
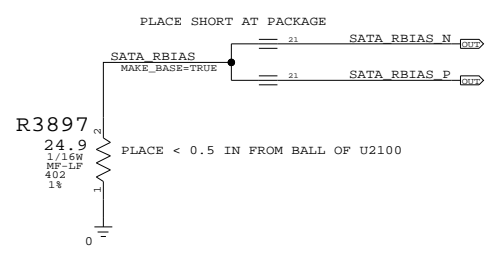
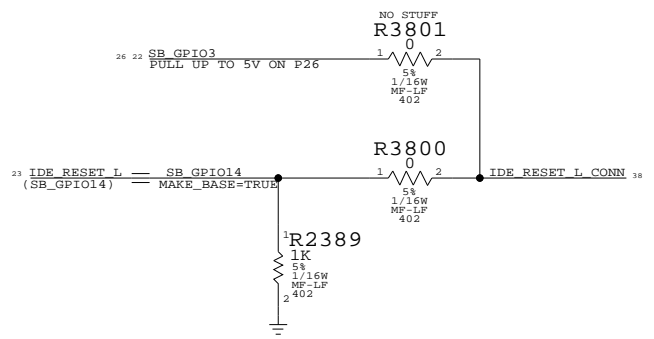
PATA CONNECTOR

Disk Connectors

SATA CONNECTOR

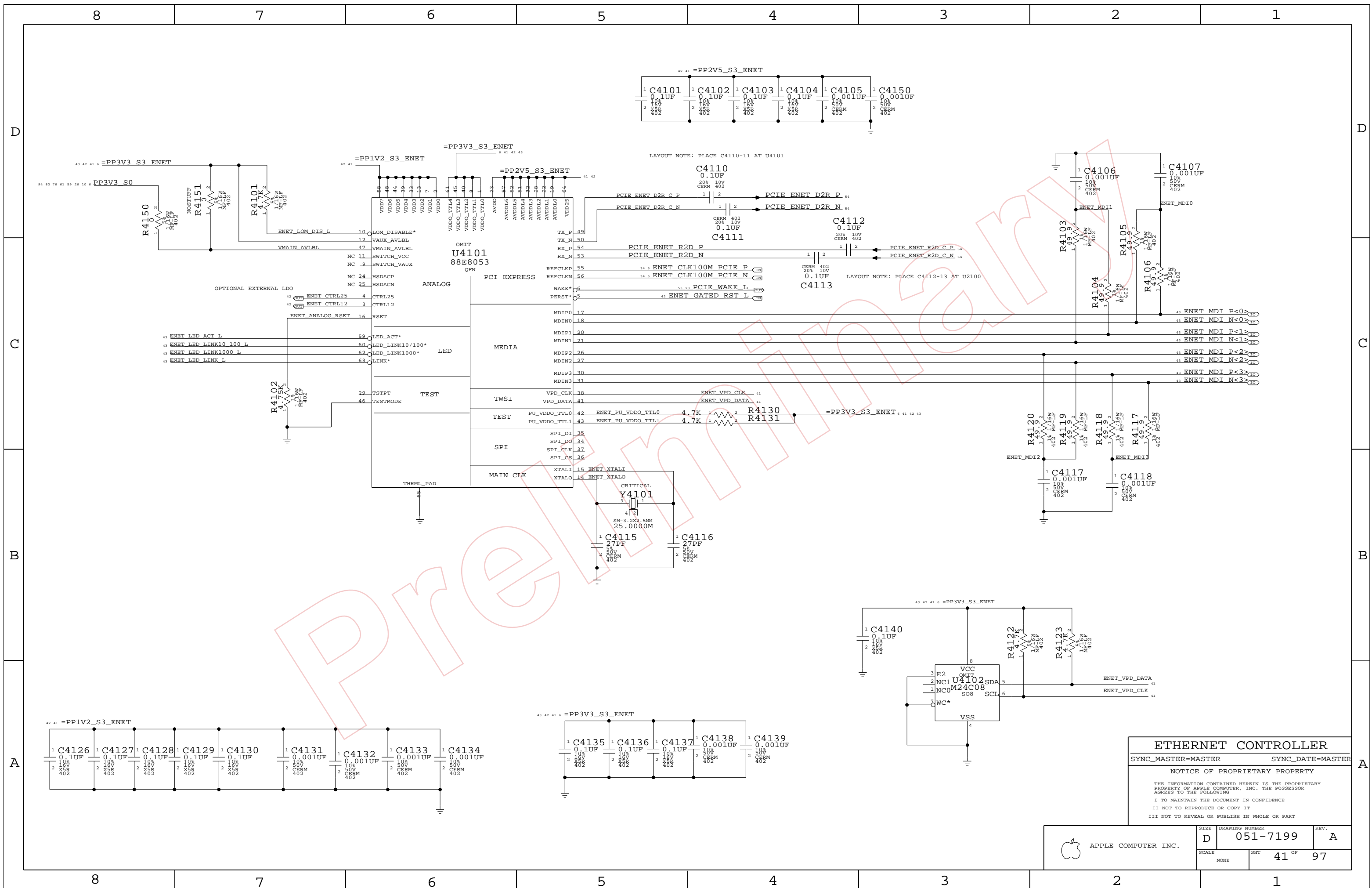
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	D	051-7199	A
SCALE	SHT	38 OF 97	
NONE			



- SATA PORT 0 IS NOT USED
- TP SATA A R2D P MAKE_BASE=TRUE
 - TP SATA A R2D N MAKE_BASE=TRUE
 - TP SATA A D2R P MAKE_BASE=TRUE
 - TP SATA A D2R N MAKE_BASE=TRUE

PLACE C3805-06 CLOSE TO JC901 FOR PP5V_S0_PATA. APPLY A WIDE TRACE SHADE FROM JC901 TO C3805-06. MIN NECK & MIN LINE WIDTH ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.



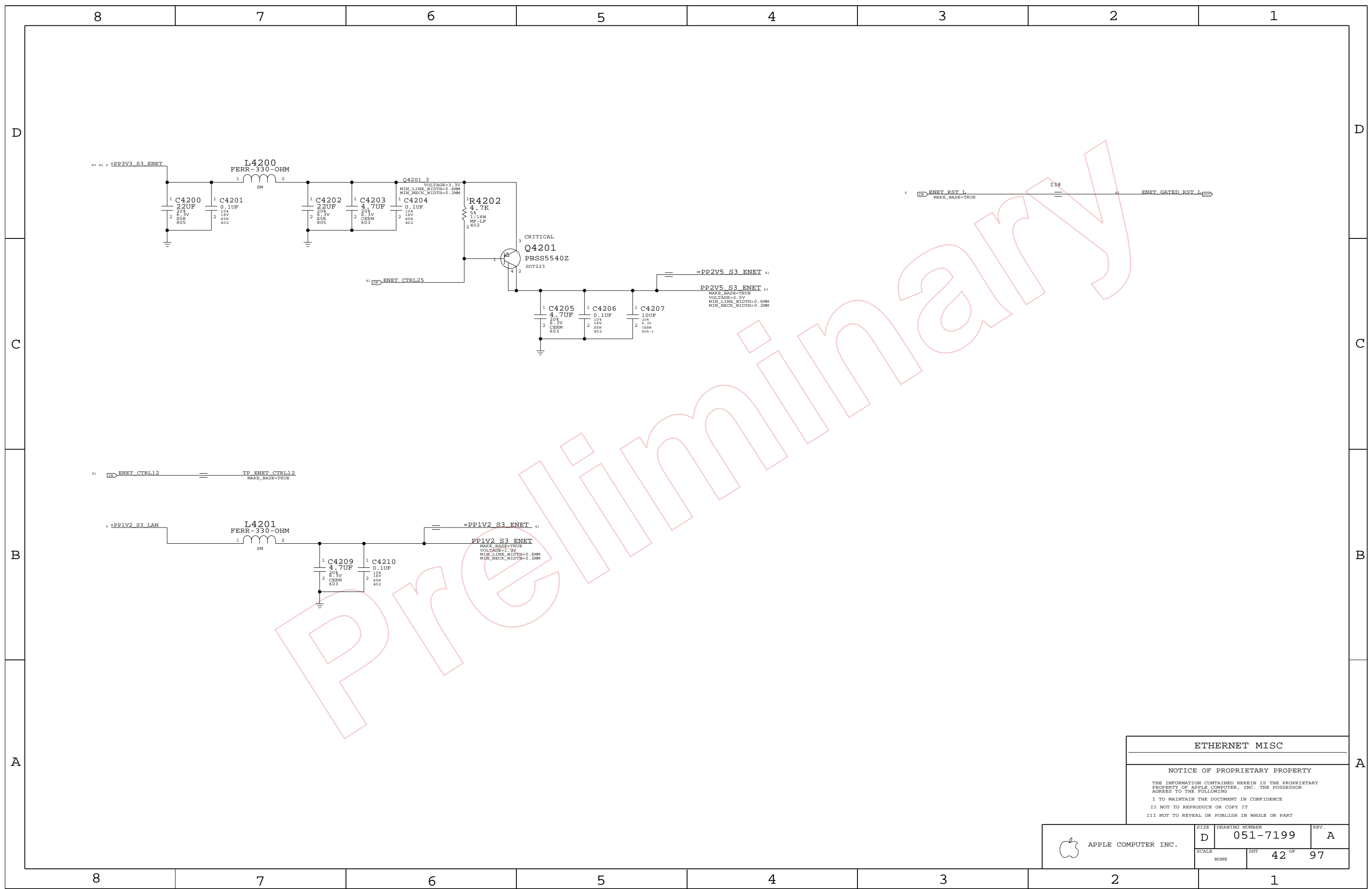
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

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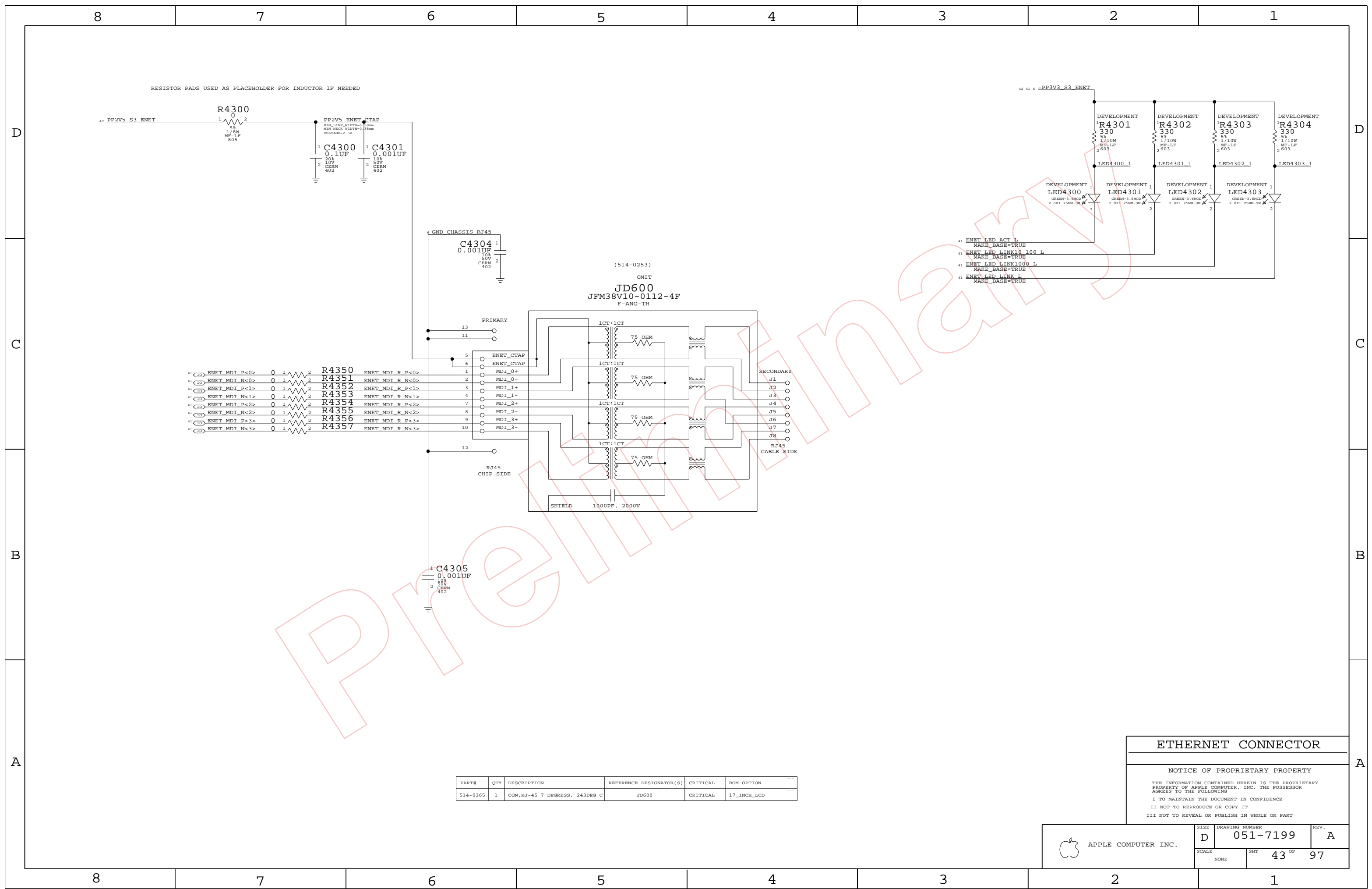
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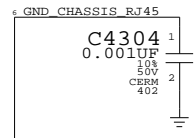
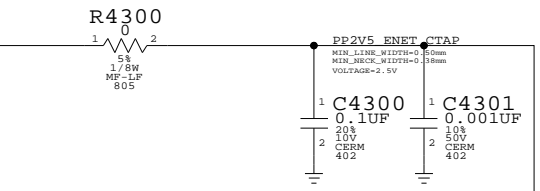
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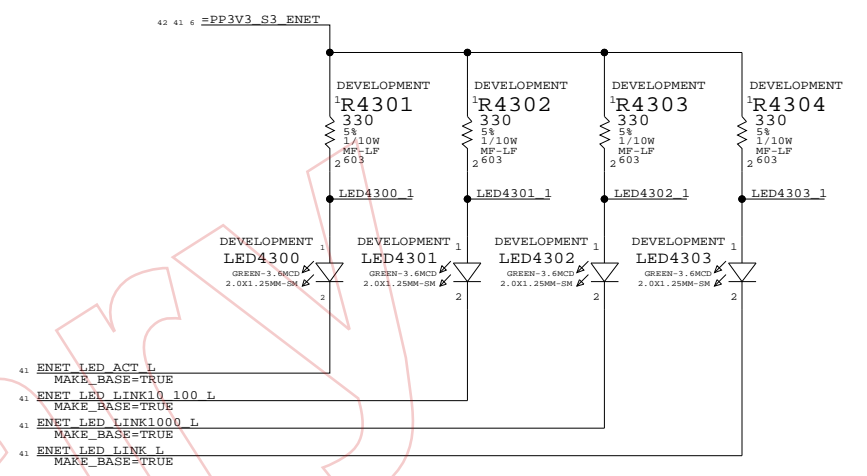
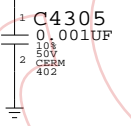
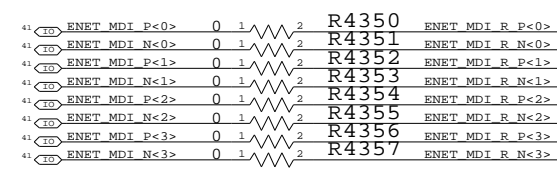
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 42 OF 97	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

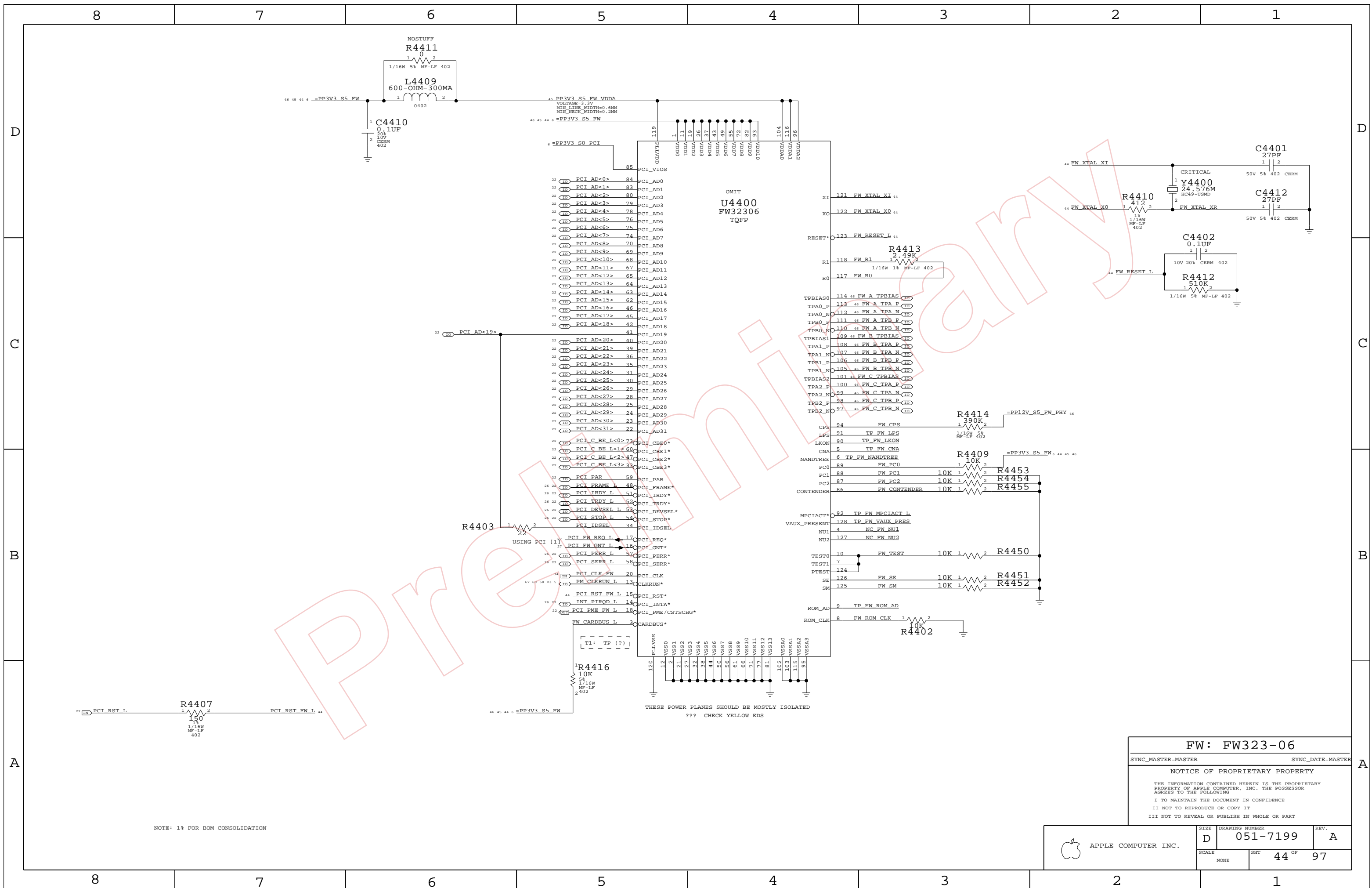
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	D	051-7199	A
SCALE	SHT	43 OF 97	
NONE			



FW: FW323-06

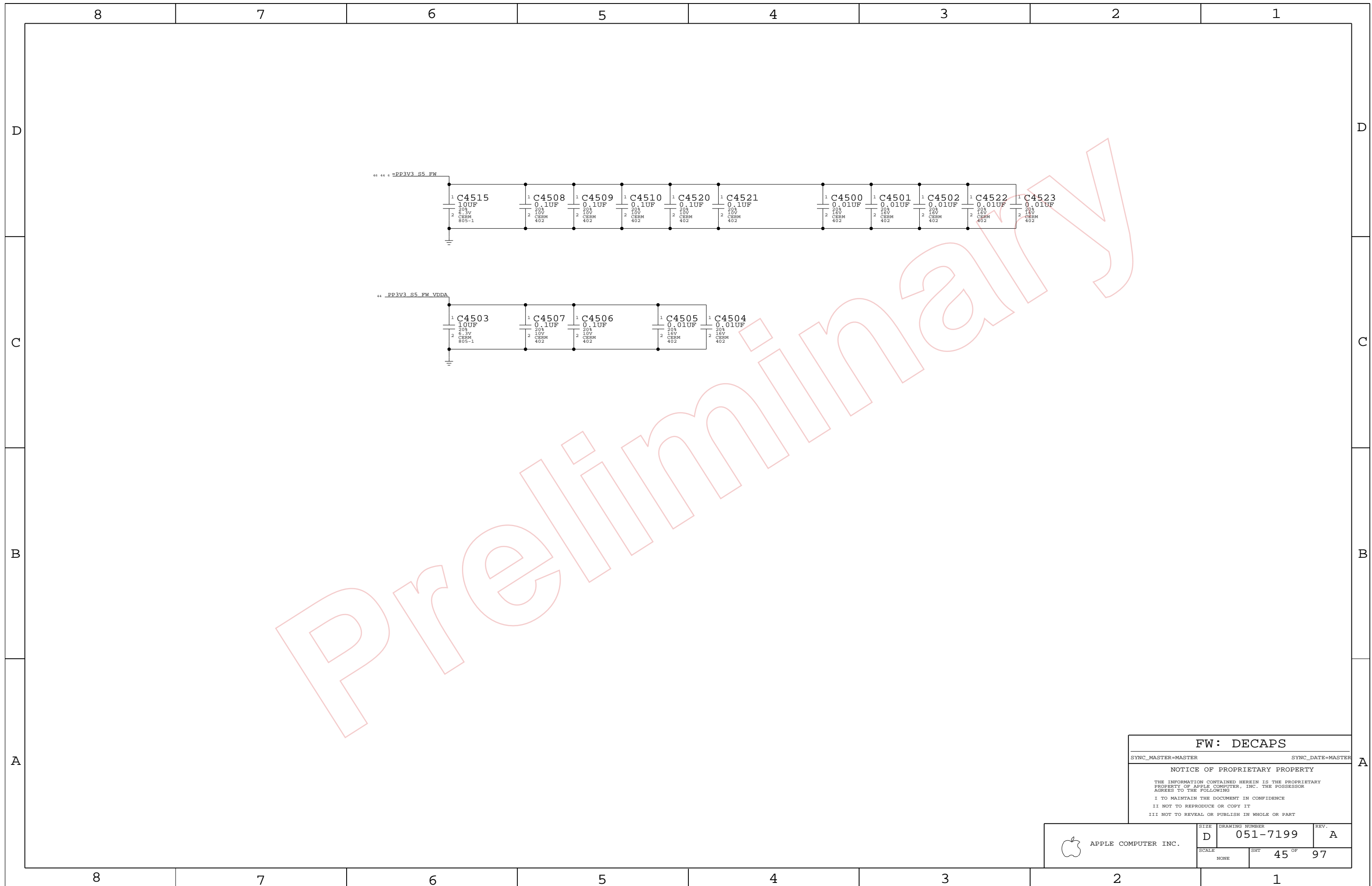
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NOTE: 1% FOR BOM CONSOLIDATION

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	44 OF 97	
NONE			



Preliminary

FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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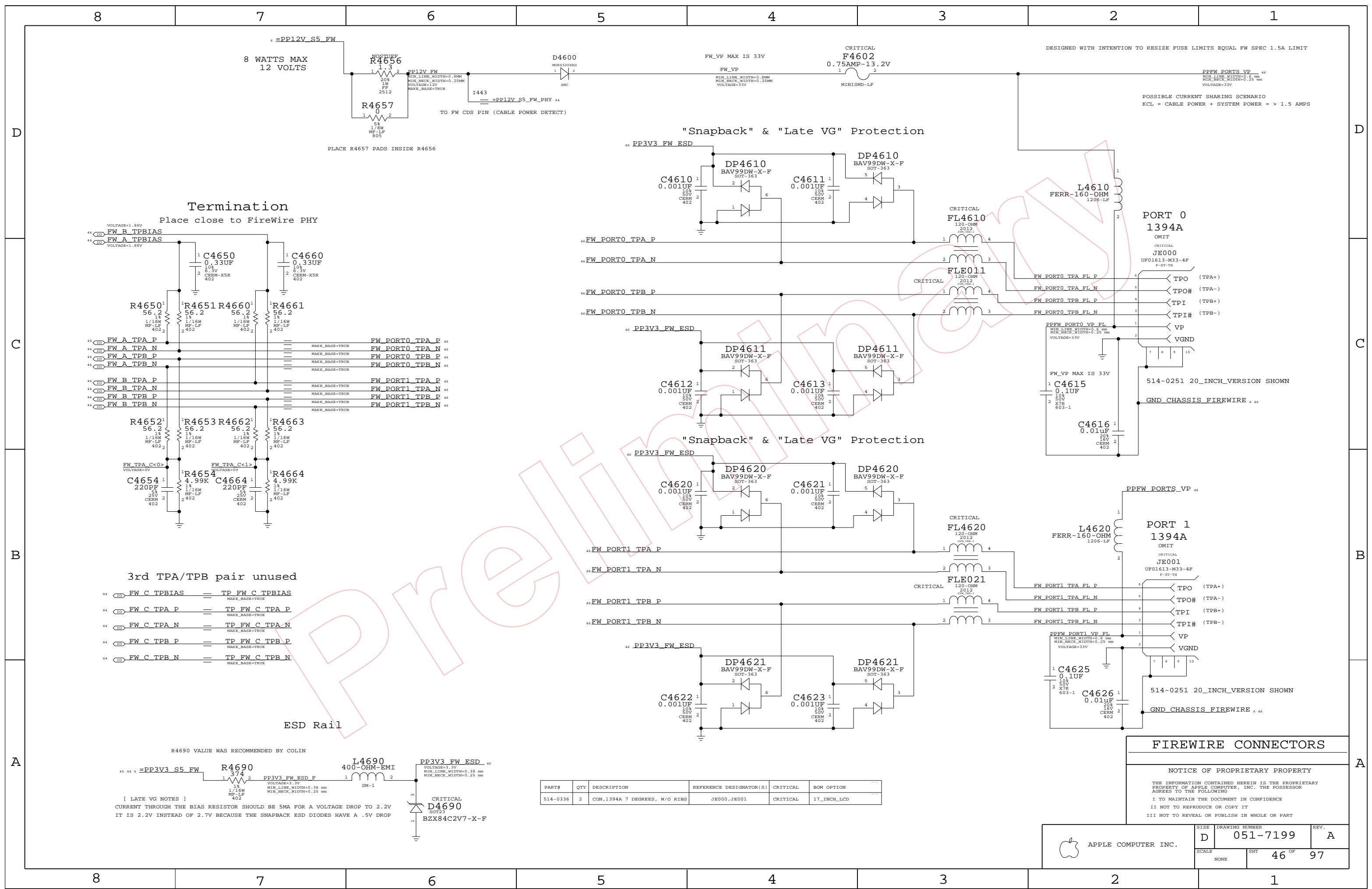
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHIT 45 OF 97	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

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	SCALE NONE	SHEET 46 OF 97	

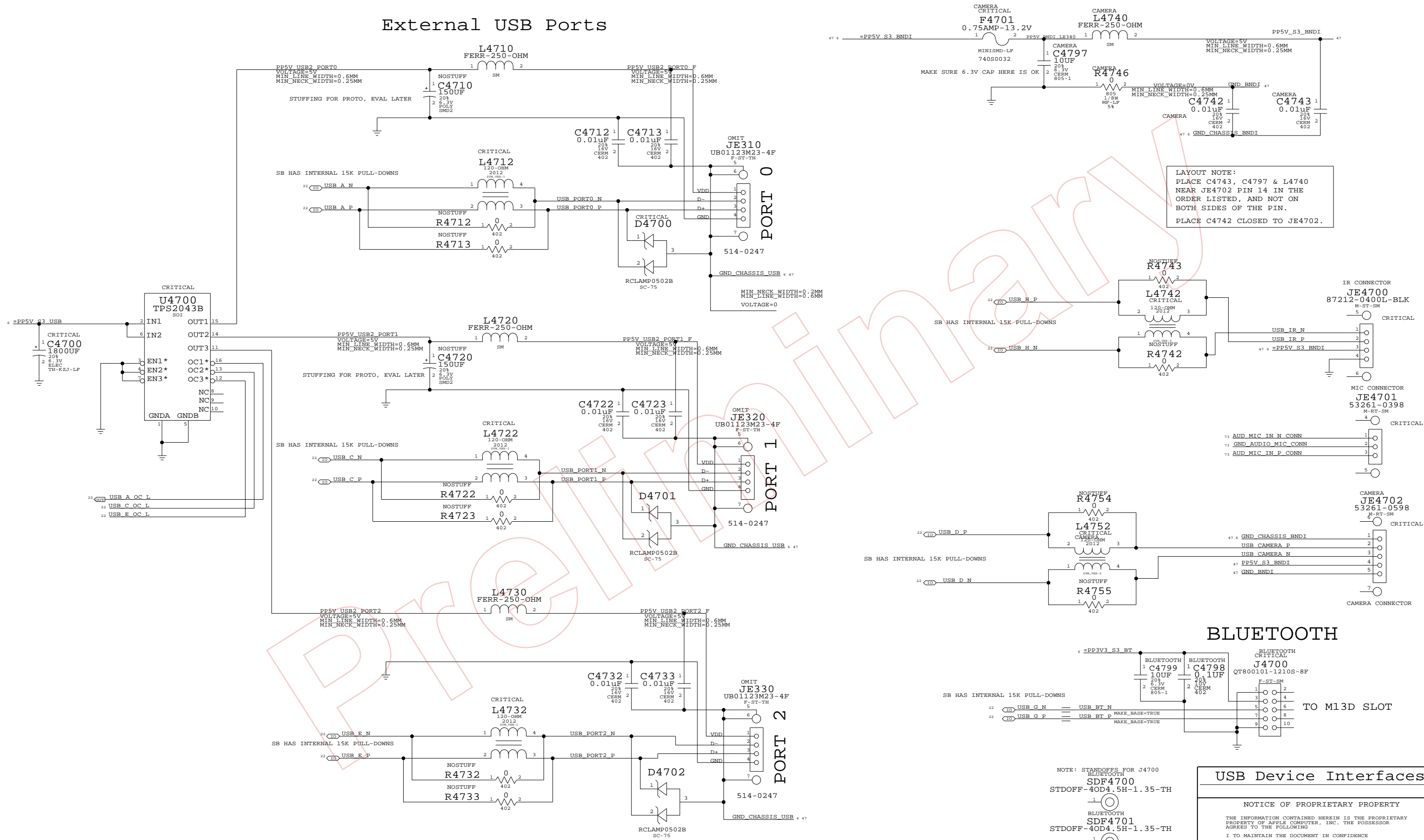
[LATE VG NOTES]
 CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

R4690 VALUE WAS RECOMMENDED BY COLIN

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

POSSIBLE CURRENT SHARING SCENARIO
 KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

External USB Ports



LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE4702 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE4702.

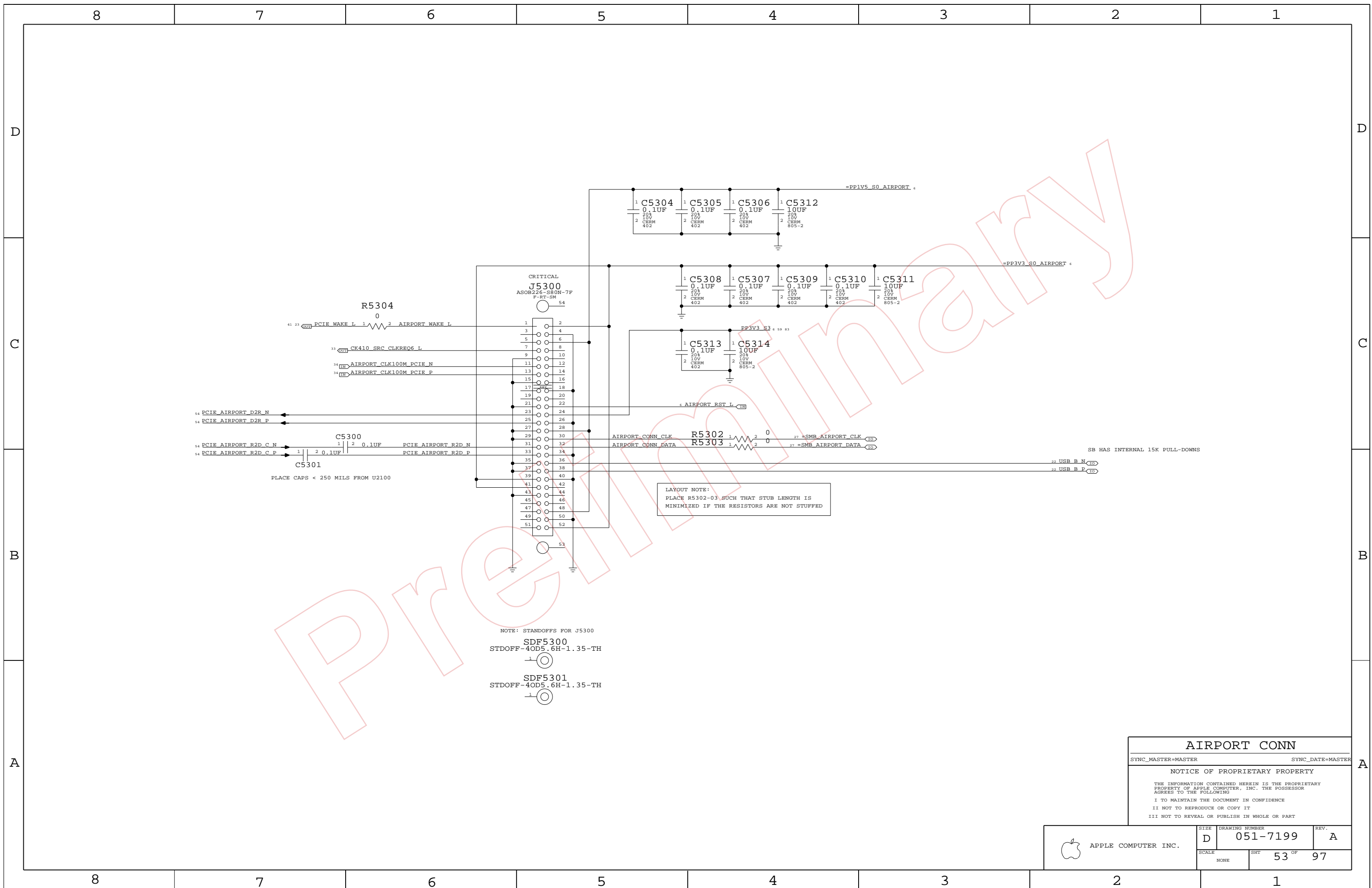
BLUETOOTH

USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 47 OF 97	



PROTECTED

AIRPORT CONN

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE		SHT	REV.
NONE		53 OF	97

8

7

6

5

4

3

2

1

D

D

C


C


B


B


A


A


22  PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE


22  PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE


22  PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE


22  PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE


22  PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE


22  PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE


22  PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE


22  PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE


22  PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE


22  PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE


22  PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22  PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE


22  PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE


22  PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE


22  PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE


22  PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE


USED PCIE PORTS


22  PCIE A R2D C N == PCIE AIRPORT R2D C N 53
MAKE_BASE=TRUE


22  PCIE A R2D C P == PCIE AIRPORT R2D C P 53
MAKE_BASE=TRUE


22 5  PCIE A D2R N == PCIE AIRPORT D2R N 53
MAKE_BASE=TRUE

22 5  PCIE A D2R P == PCIE AIRPORT D2R P 53
MAKE_BASE=TRUE

22  PCIE B R2D C N == PCIE ENET R2D C N 41
MAKE_BASE=TRUE

22  PCIE B R2D C P == PCIE ENET R2D C P 41
MAKE_BASE=TRUE

22 5  PCIE B D2R N == PCIE ENET D2R N 41
MAKE_BASE=TRUE

22 5  PCIE B D2R P == PCIE ENET D2R P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7199	A
SCALE	SHT	
NONE	54 OF 97	

8

7

6

5

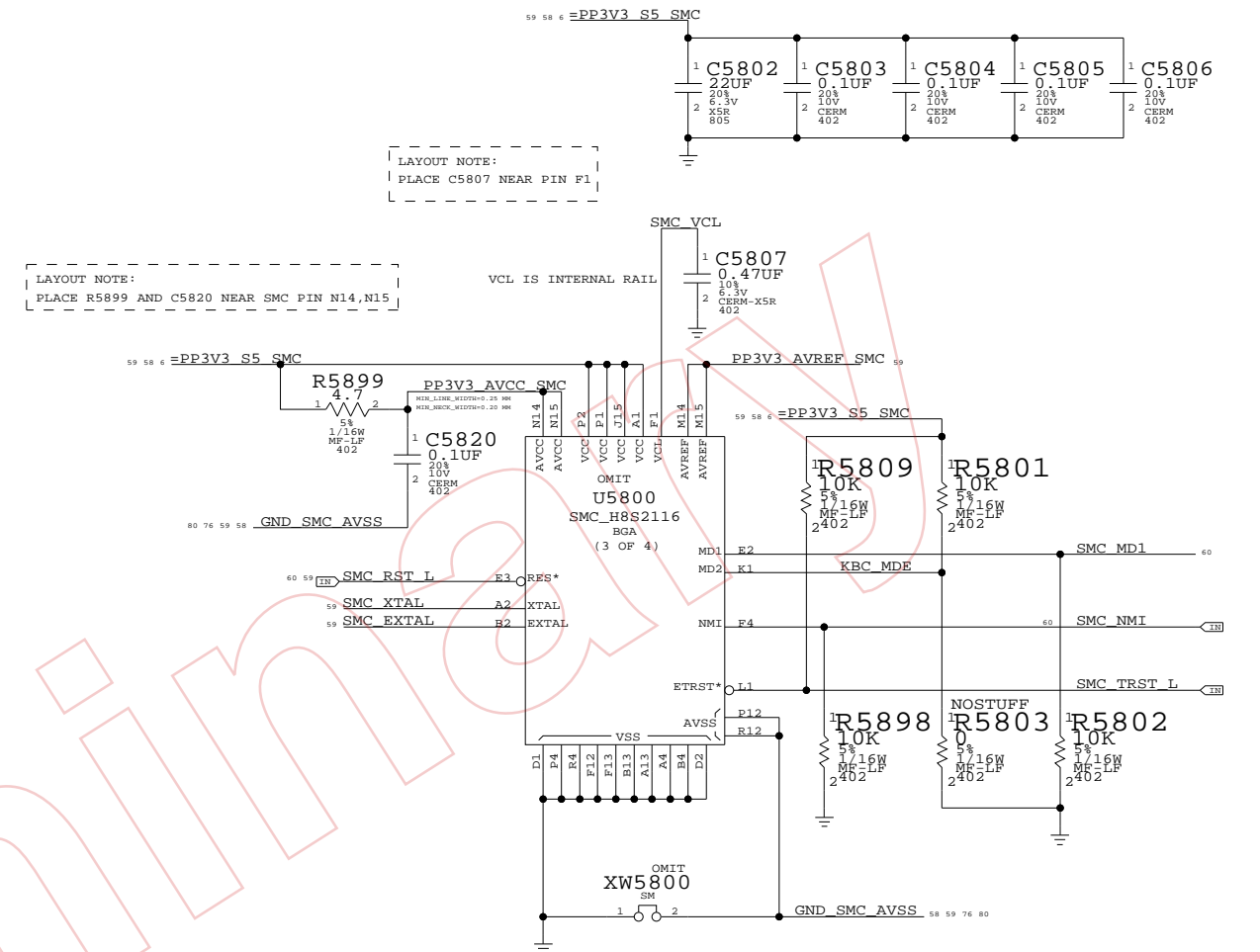
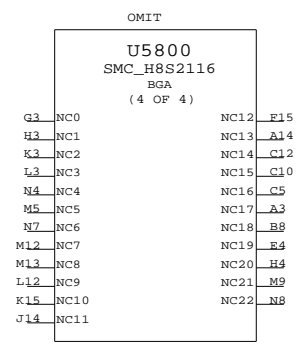
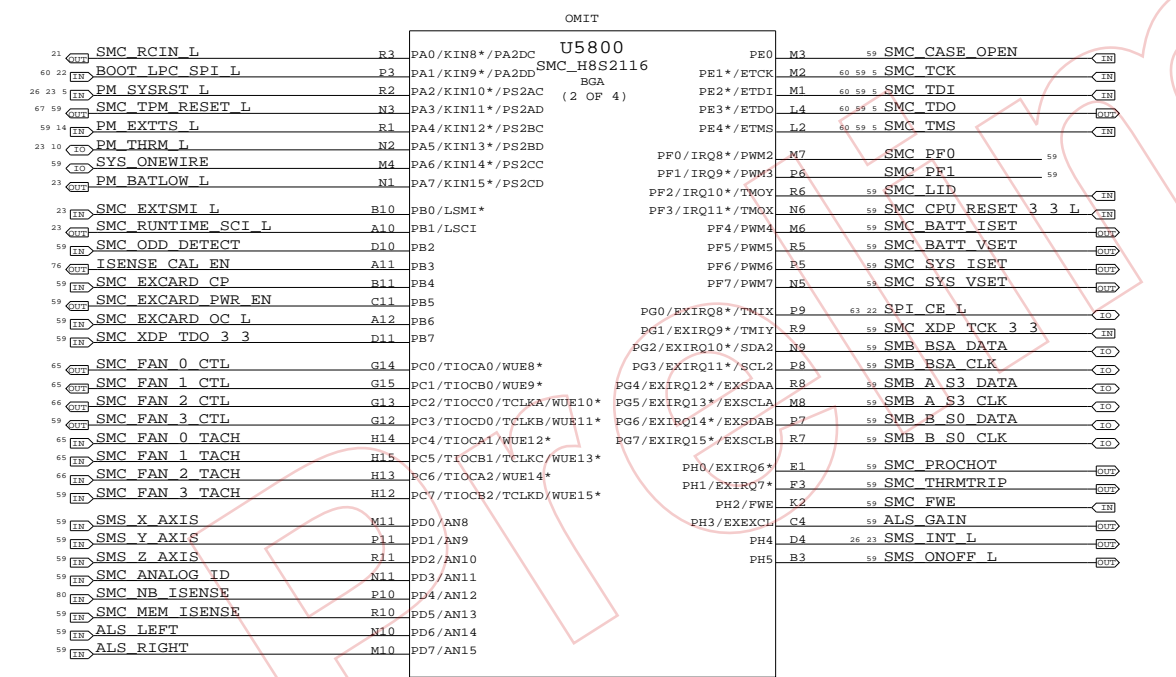
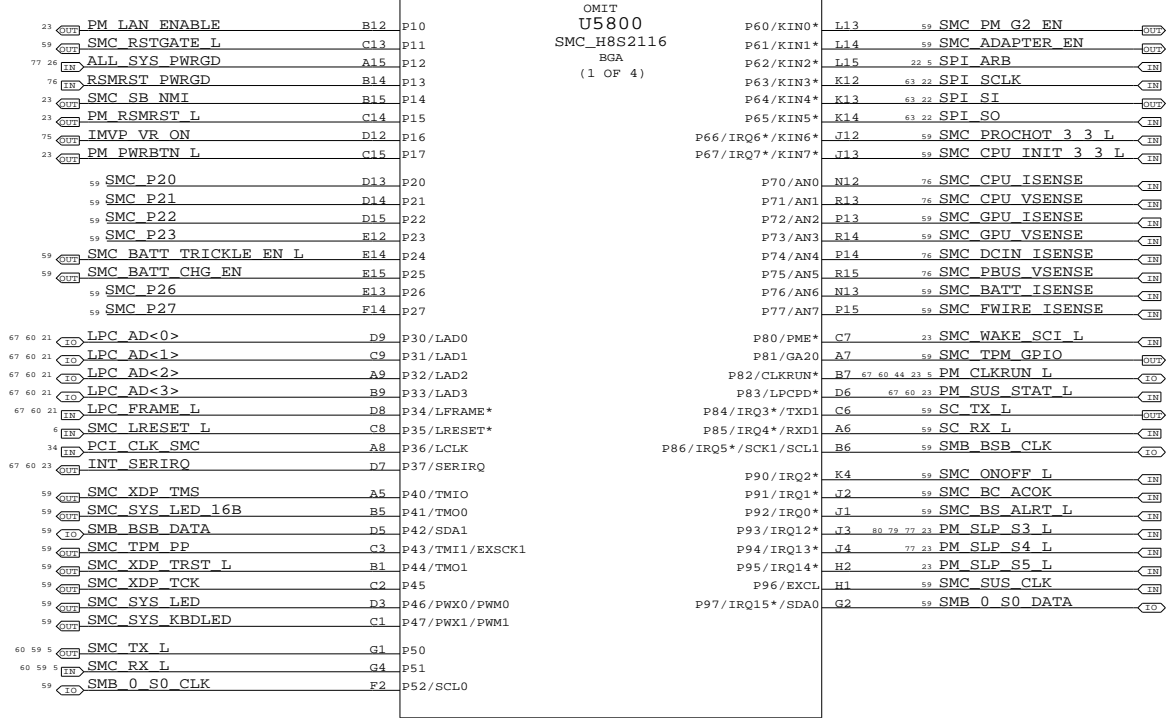
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

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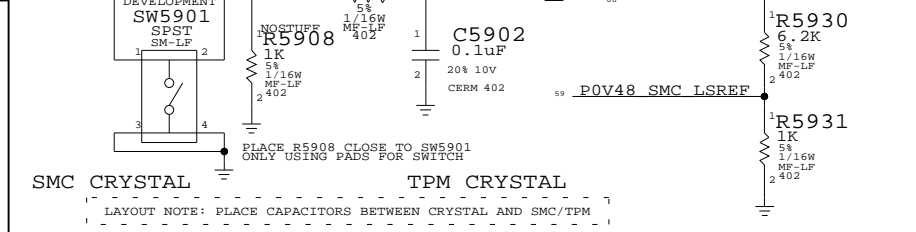
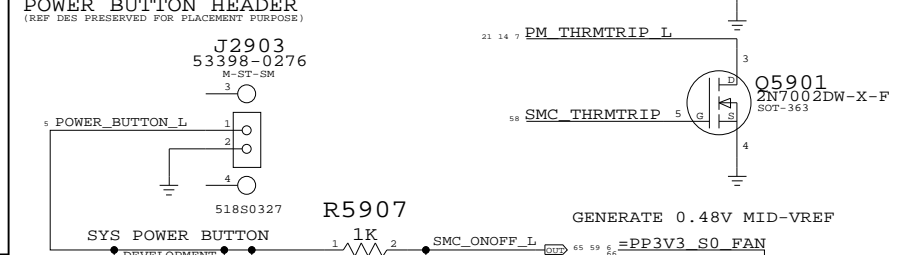
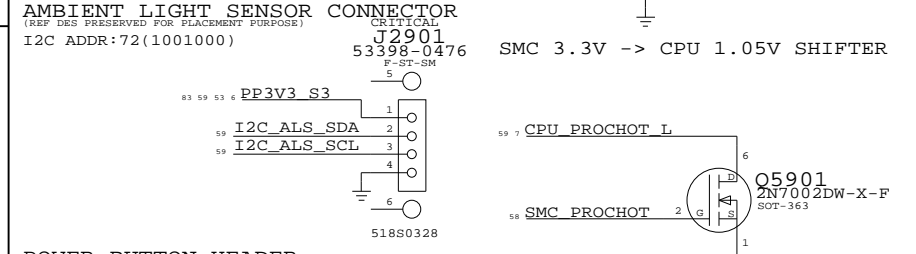
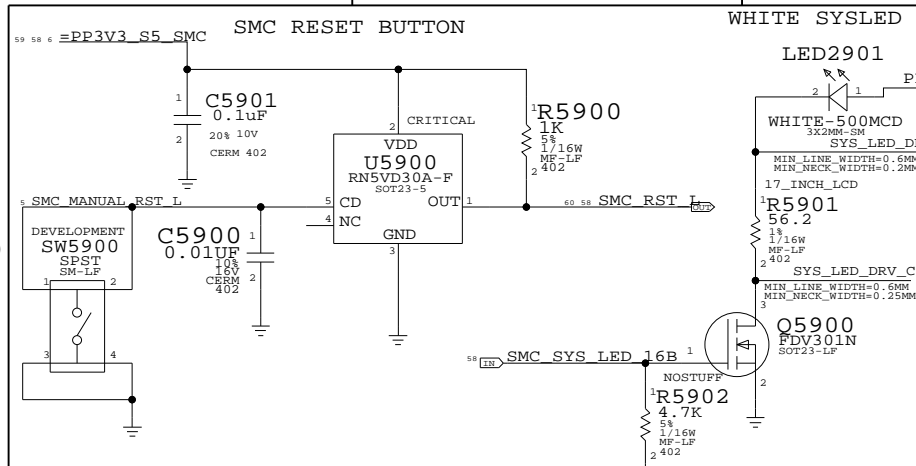
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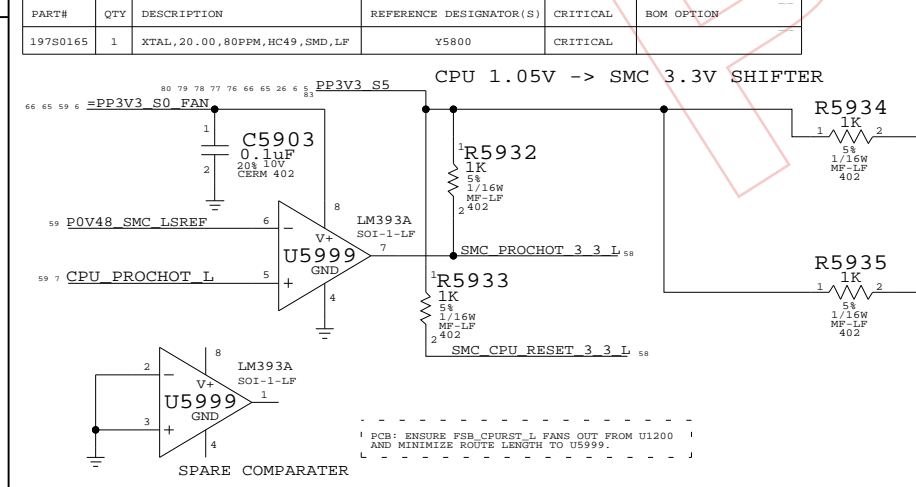
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

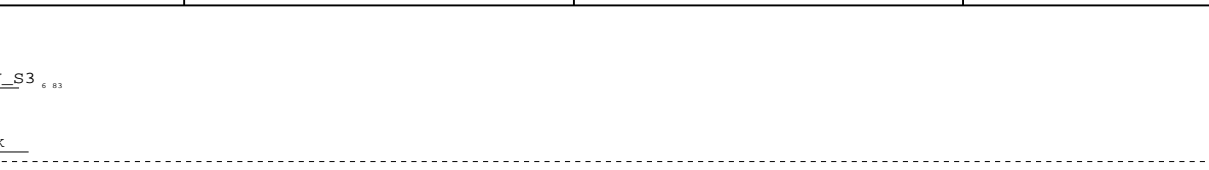
	DRAWING NUMBER		REV.
	D	051-7199	A
SCALE		SHT	OF
NONE		58	97



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

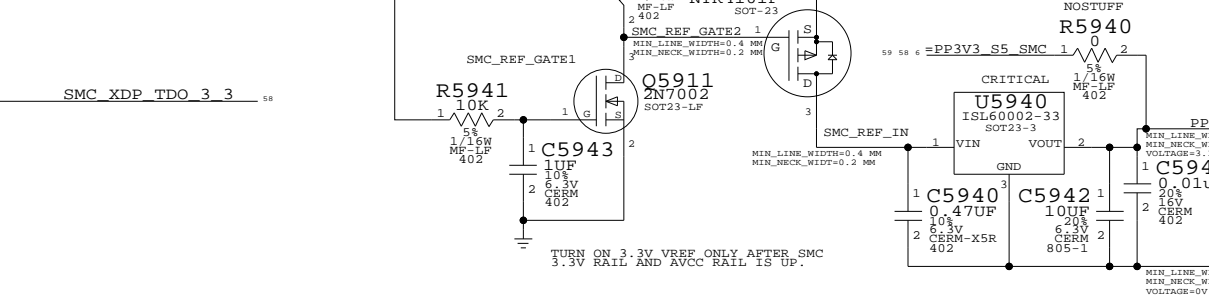
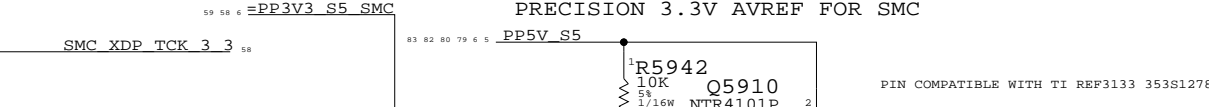
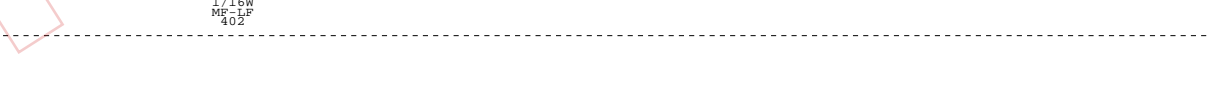
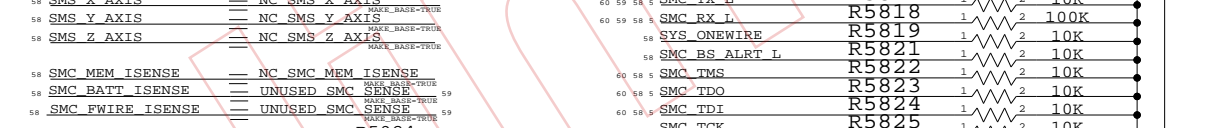
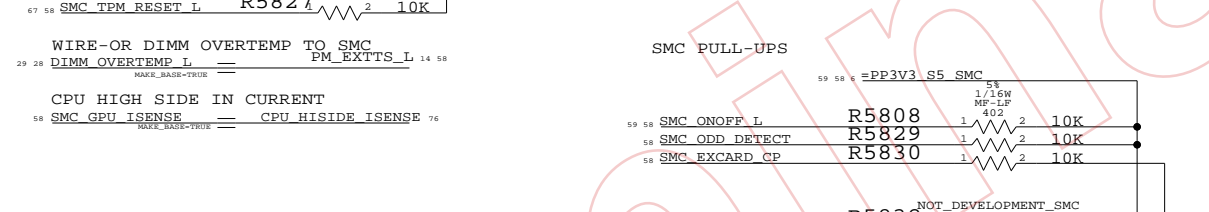


PCB: ENSURE FSB_CPURST_L PINS OUT FROM U1200 AND MINIMIZE ROUTER LENGTH TO U5999.

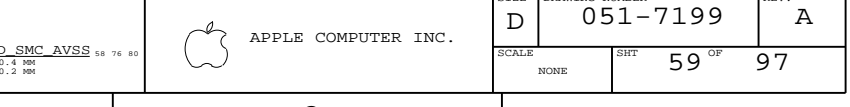
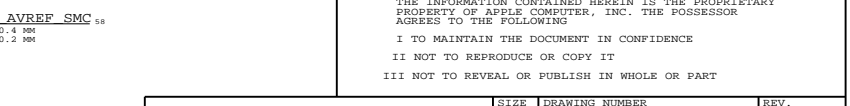
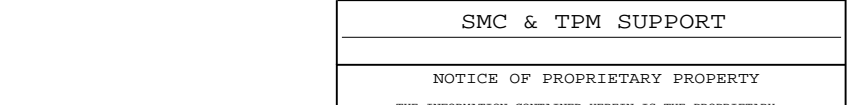
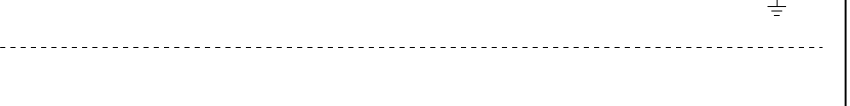
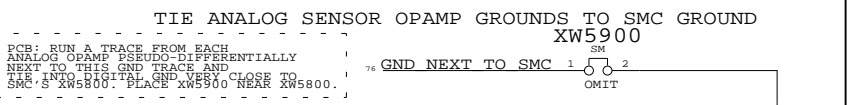
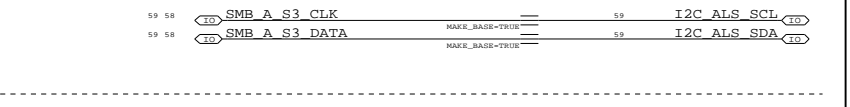
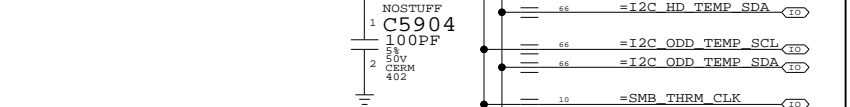
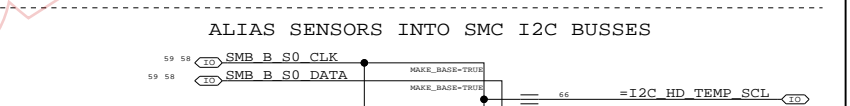
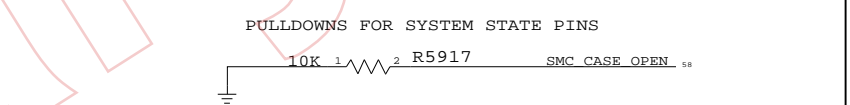
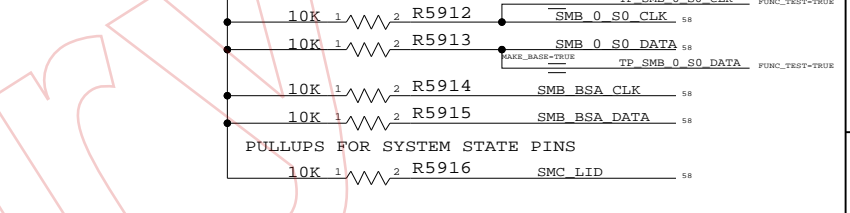
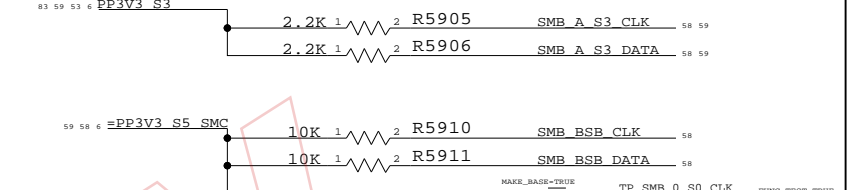
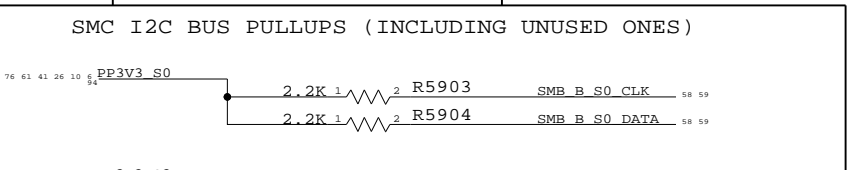


SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	SMC ALIASES	PULLUPS	TESTPOINTS
SMC P20	NC SMC P20	10K	TP SMC P20
SMC P21	NC SMC P21	10K	TP SMC P21
SMC P22	NC SMC P22	10K	TP SMC P22
SMC P23	NC SMC P23	10K	TP SMC P23
SMC P26	NC SMC P26	10K	TP SMC P26
SMC P27	NC SMC P27	10K	TP SMC P27
SMC BATT ISET	NC SMC BATT ISET	10K	TP SMC BATT ISET
SMC BATT VSET	NC SMC BATT VSET	10K	TP SMC BATT VSET
SMC SYS ISET	NC SMC SYS ISET	10K	TP SMC SYS ISET
SMC SYS VSET	NC SMC SYS VSET	10K	TP SMC SYS VSET
SMC BATT TRICKLE EN L	NC SMC BATT TRICKLE EN L	10K	TP SMC BATT TRICKLE EN L
SMC BATT CHG EN	NC SMC BATT CHG EN	10K	TP SMC BATT CHG EN
SMC ANALOG ID	NC SMC ANALOG ID	10K	TP SMC ANALOG ID
ALS GAIN	NC ALS GAIN	10K	TP ALS GAIN
SMC P20	TP SMC P20	10K	TP SMC P20
SMC P21	TP SMC P21	10K	TP SMC P21
SMC P22	TP SMC P22	10K	TP SMC P22
SMC P23	TP SMC P23	10K	TP SMC P23
SMC P26	TP SMC P26	10K	TP SMC P26
SMC P27	TP SMC P27	10K	TP SMC P27
SMC BATT ISET	TP SMC BATT ISET	10K	TP SMC BATT ISET
SMC BATT VSET	TP SMC BATT VSET	10K	TP SMC BATT VSET
SMC SYS ISET	TP SMC SYS ISET	10K	TP SMC SYS ISET
SMC SYS VSET	TP SMC SYS VSET	10K	TP SMC SYS VSET
SMC BATT TRICKLE EN L	TP SMC BATT TRICKLE EN L	10K	TP SMC BATT TRICKLE EN L
SMC BATT CHG EN	TP SMC BATT CHG EN	10K	TP SMC BATT CHG EN
SMC ANALOG ID	TP SMC ANALOG ID	10K	TP SMC ANALOG ID
ALS GAIN	TP ALS GAIN	10K	TP ALS GAIN
SMC P20	TP SMC P20	10K	TP SMC P20
SMC P21	TP SMC P21	10K	TP SMC P21
SMC P22	TP SMC P22	10K	TP SMC P22
SMC P23	TP SMC P23	10K	TP SMC P23
SMC P26	TP SMC P26	10K	TP SMC P26
SMC P27	TP SMC P27	10K	TP SMC P27
SMC BATT ISET	TP SMC BATT ISET	10K	TP SMC BATT ISET
SMC BATT VSET	TP SMC BATT VSET	10K	TP SMC BATT VSET
SMC SYS ISET	TP SMC SYS ISET	10K	TP SMC SYS ISET
SMC SYS VSET	TP SMC SYS VSET	10K	TP SMC SYS VSET
SMC BATT TRICKLE EN L	TP SMC BATT TRICKLE EN L	10K	TP SMC BATT TRICKLE EN L
SMC BATT CHG EN	TP SMC BATT CHG EN	10K	TP SMC BATT CHG EN
SMC ANALOG ID	TP SMC ANALOG ID	10K	TP SMC ANALOG ID
ALS GAIN	TP ALS GAIN	10K	TP ALS GAIN
SMC P20	TP SMC P20	10K	TP SMC P20
SMC P21	TP SMC P21	10K	TP SMC P21
SMC P22	TP SMC P22	10K	TP SMC P22
SMC P23	TP SMC P23	10K	TP SMC P23
SMC P26	TP SMC P26	10K	TP SMC P26
SMC P27	TP SMC P27	10K	TP SMC P27
SMC BATT ISET	TP SMC BATT ISET	10K	TP SMC BATT ISET
SMC BATT VSET	TP SMC BATT VSET	10K	TP SMC BATT VSET
SMC SYS ISET	TP SMC SYS ISET	10K	TP SMC SYS ISET
SMC SYS VSET	TP SMC SYS VSET	10K	TP SMC SYS VSET
SMC BATT TRICKLE EN L	TP SMC BATT TRICKLE EN L	10K	TP SMC BATT TRICKLE EN L
SMC BATT CHG EN	TP SMC BATT CHG EN	10K	TP SMC BATT CHG EN
SMC ANALOG ID	TP SMC ANALOG ID	10K	TP SMC ANALOG ID
ALS GAIN	TP ALS GAIN	10K	TP ALS GAIN
SMC P20	TP SMC P20	10K	TP SMC P20
SMC P21	TP SMC P21	10K	TP SMC P21
SMC P22	TP SMC P22	10K	TP SMC P22
SMC P23	TP SMC P23	10K	TP SMC P23
SMC P26	TP SMC P26	10K	TP SMC P26
SMC P27	TP SMC P27	10K	TP SMC P27
SMC BATT ISET	TP SMC BATT ISET	10K	TP SMC BATT ISET
SMC BATT VSET	TP SMC BATT VSET	10K	TP SMC BATT VSET
SMC SYS ISET	TP SMC SYS ISET	10K	TP SMC SYS ISET
SMC SYS VSET	TP SMC SYS VSET	10K	TP SMC SYS VSET
SMC BATT TRICKLE EN L	TP SMC BATT TRICKLE EN L	10K	TP SMC BATT TRICKLE EN L
SMC BATT CHG EN	TP SMC BATT CHG EN	10K	TP SMC BATT CHG EN
SMC ANALOG ID	TP SMC ANALOG ID	10K	TP SMC ANALOG ID
ALS GAIN	TP ALS GAIN	10K	TP ALS GAIN



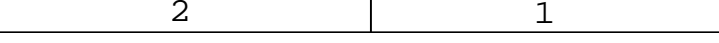
TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

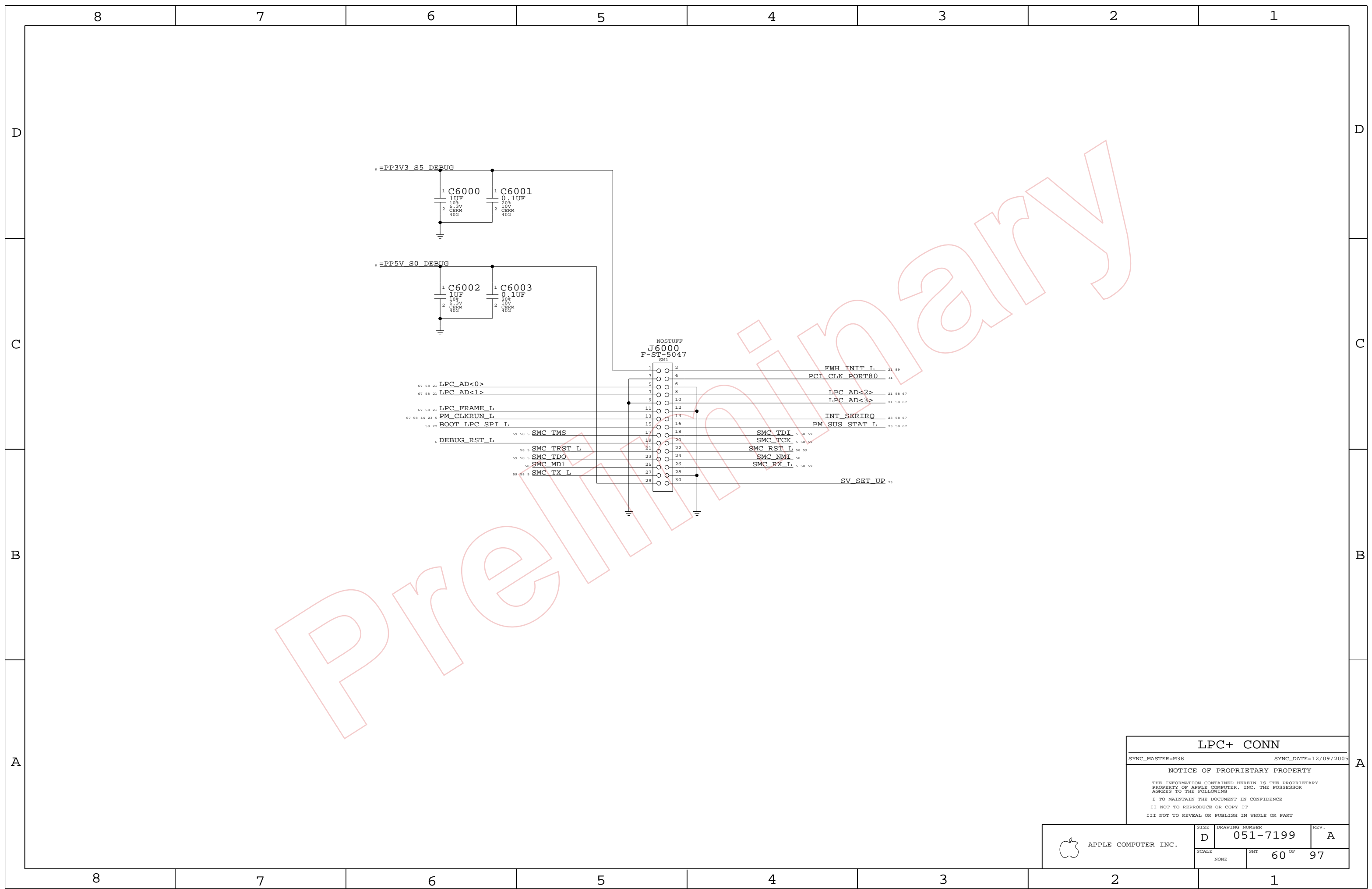


TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND XW5900. GND NEXT TO SMC 1 OMIT.

SMC & TPM SUPPORT
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SCALE	SHT	59 OF 97
NONE		





Pre-release

LPC+ CONN

SYNC_MASTER=M38 SYNC_DATE=12/09/2005

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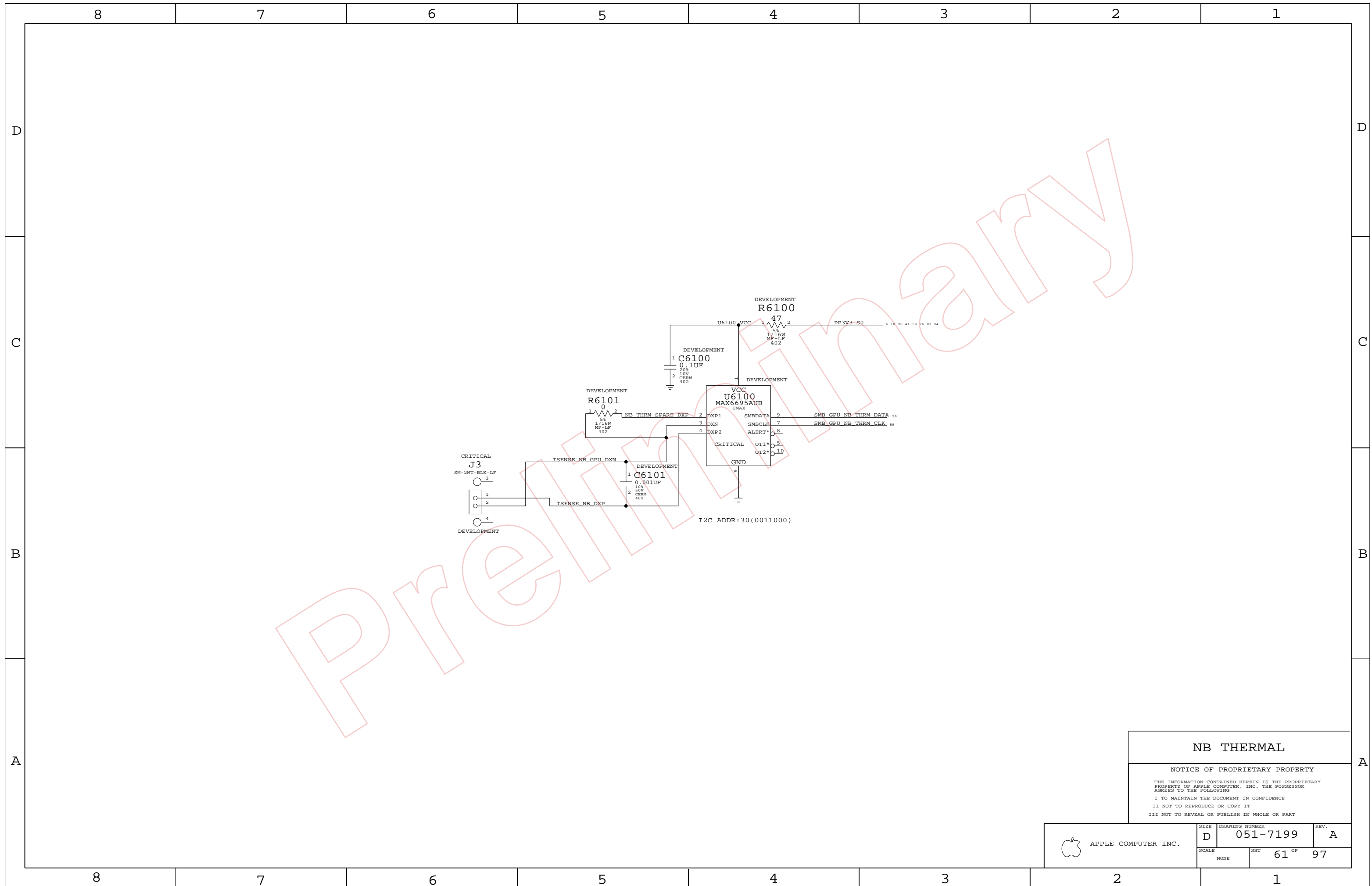
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	SCALE NONE	SHIT 60 OF 97	



NB THERMAL


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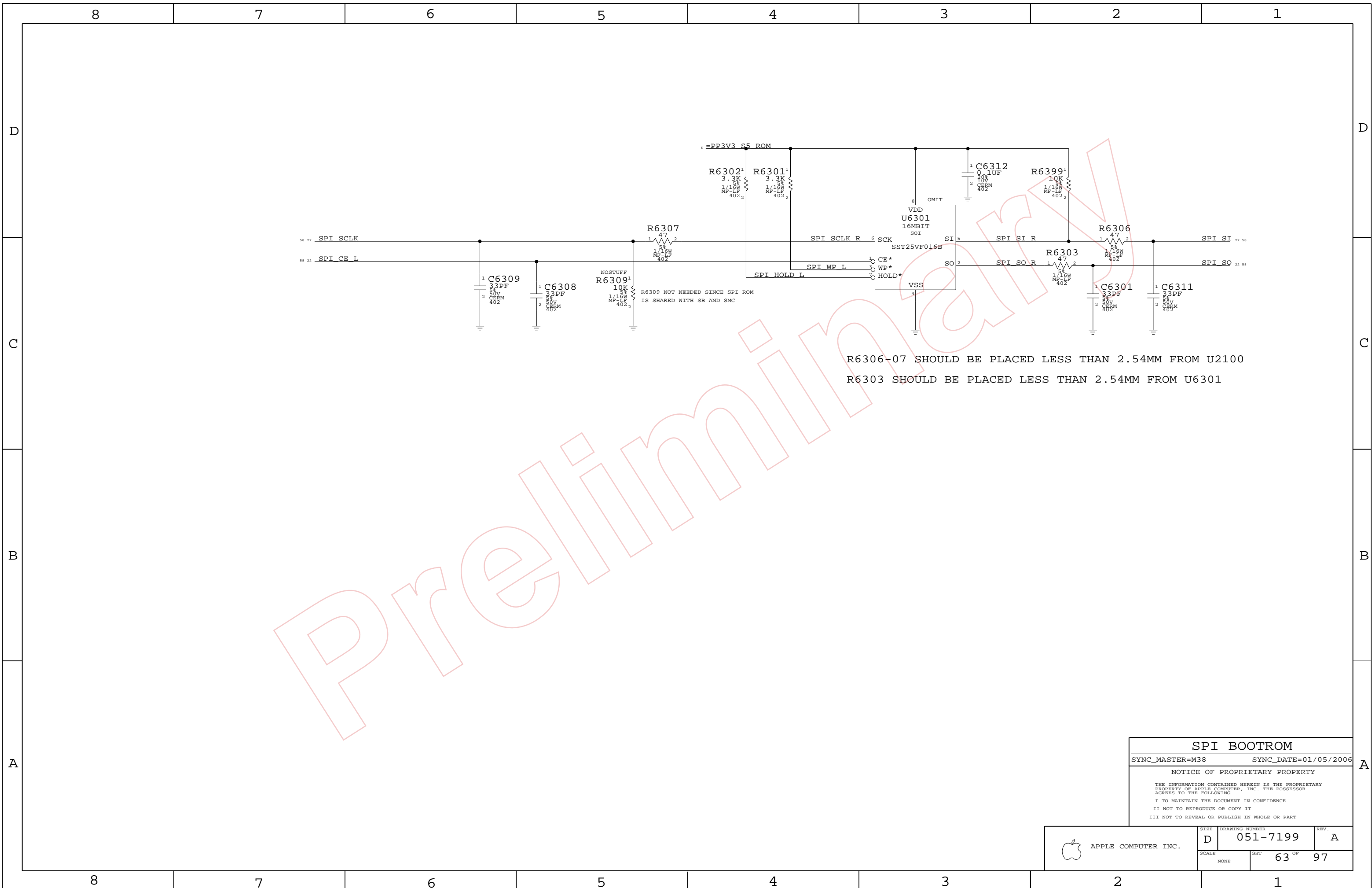
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	D	051-7199	A
SCALE	SHT	61 OF 97	
NONE			

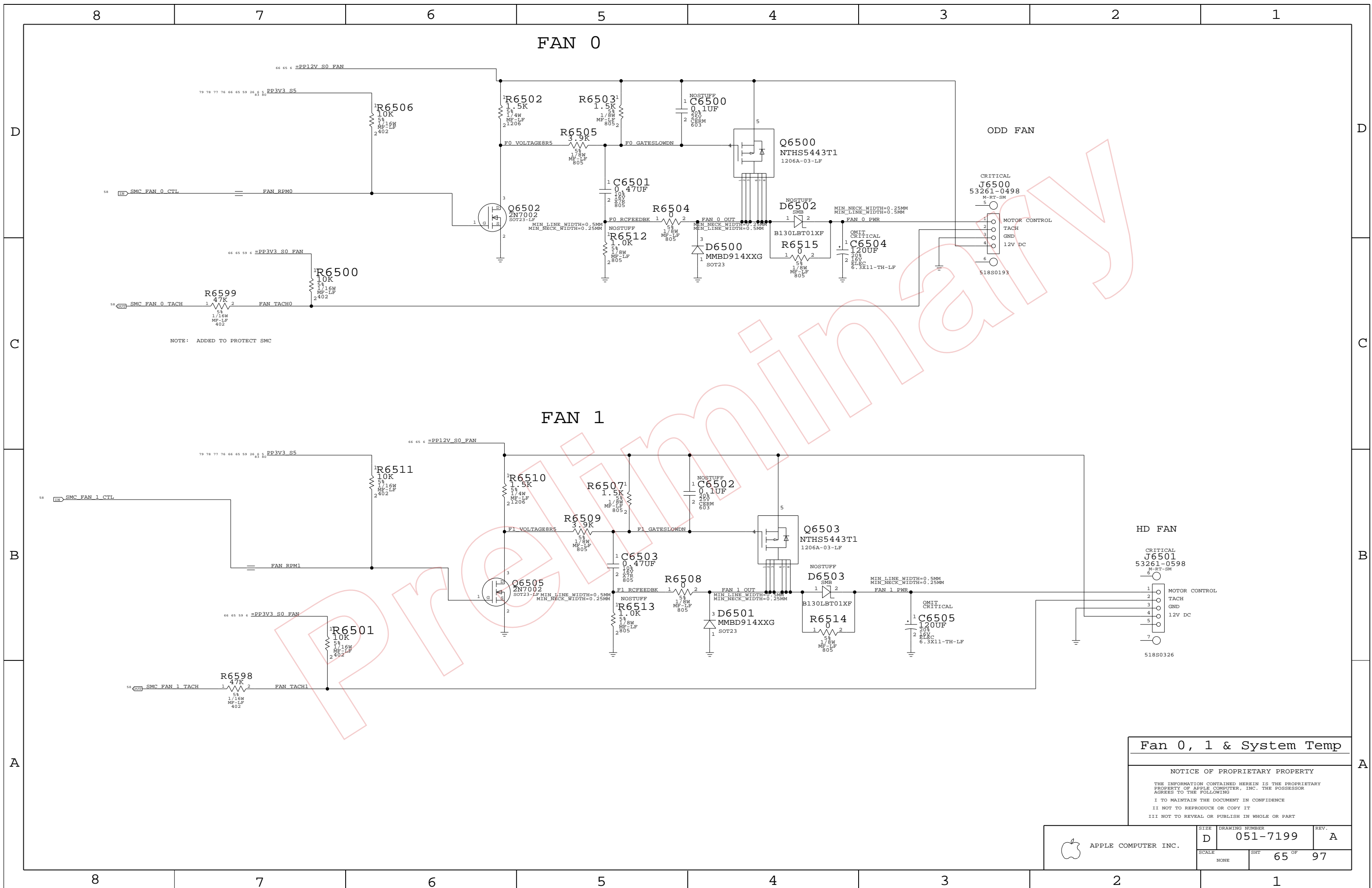


R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

Preliminary

SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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	SCALE NONE	SHEET 63 OF 97	



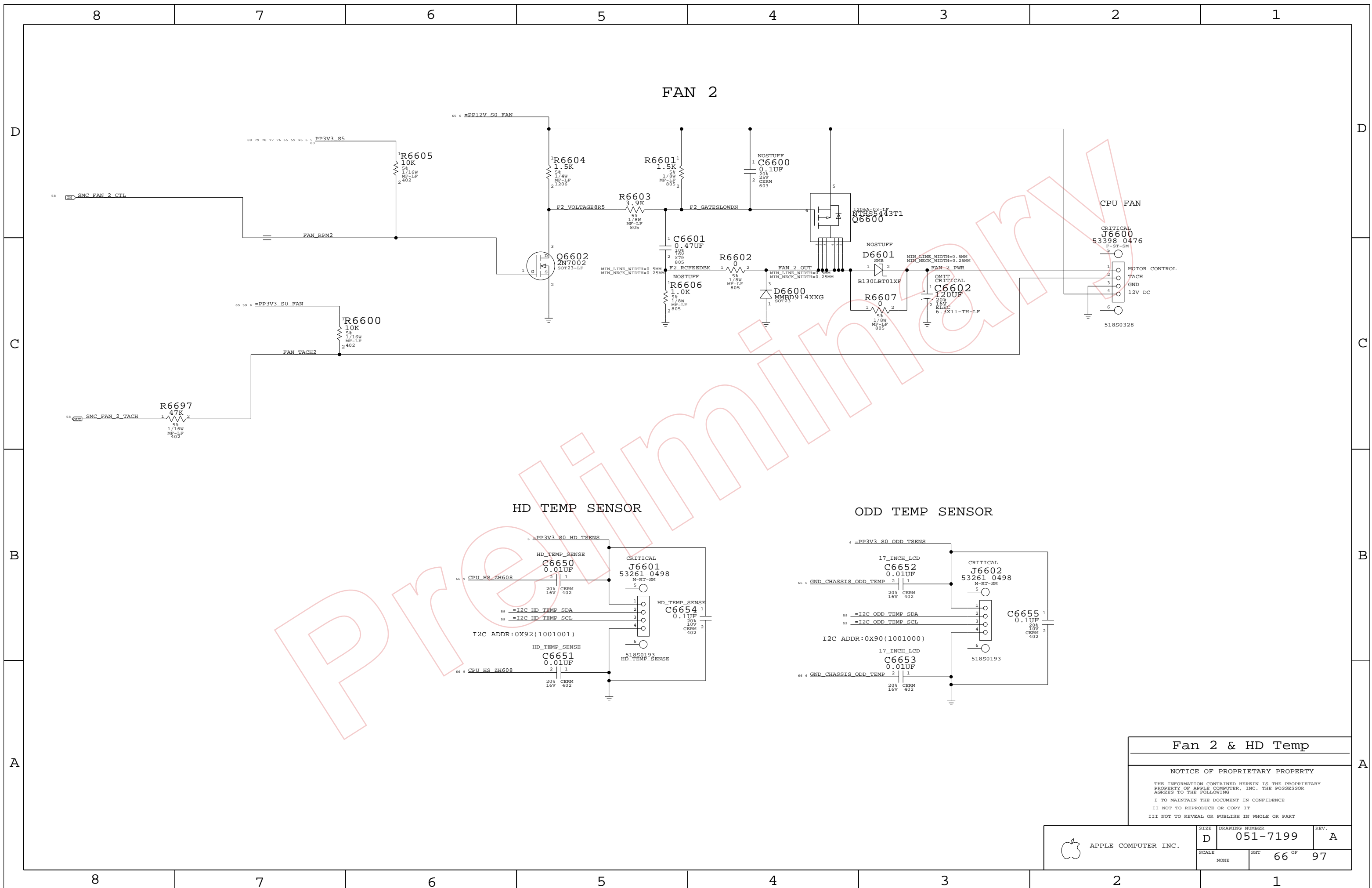
NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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	D	051-7199	A
SCALE	SHT	65 OF 97	
NONE			



FAN 2

HD TEMP SENSOR

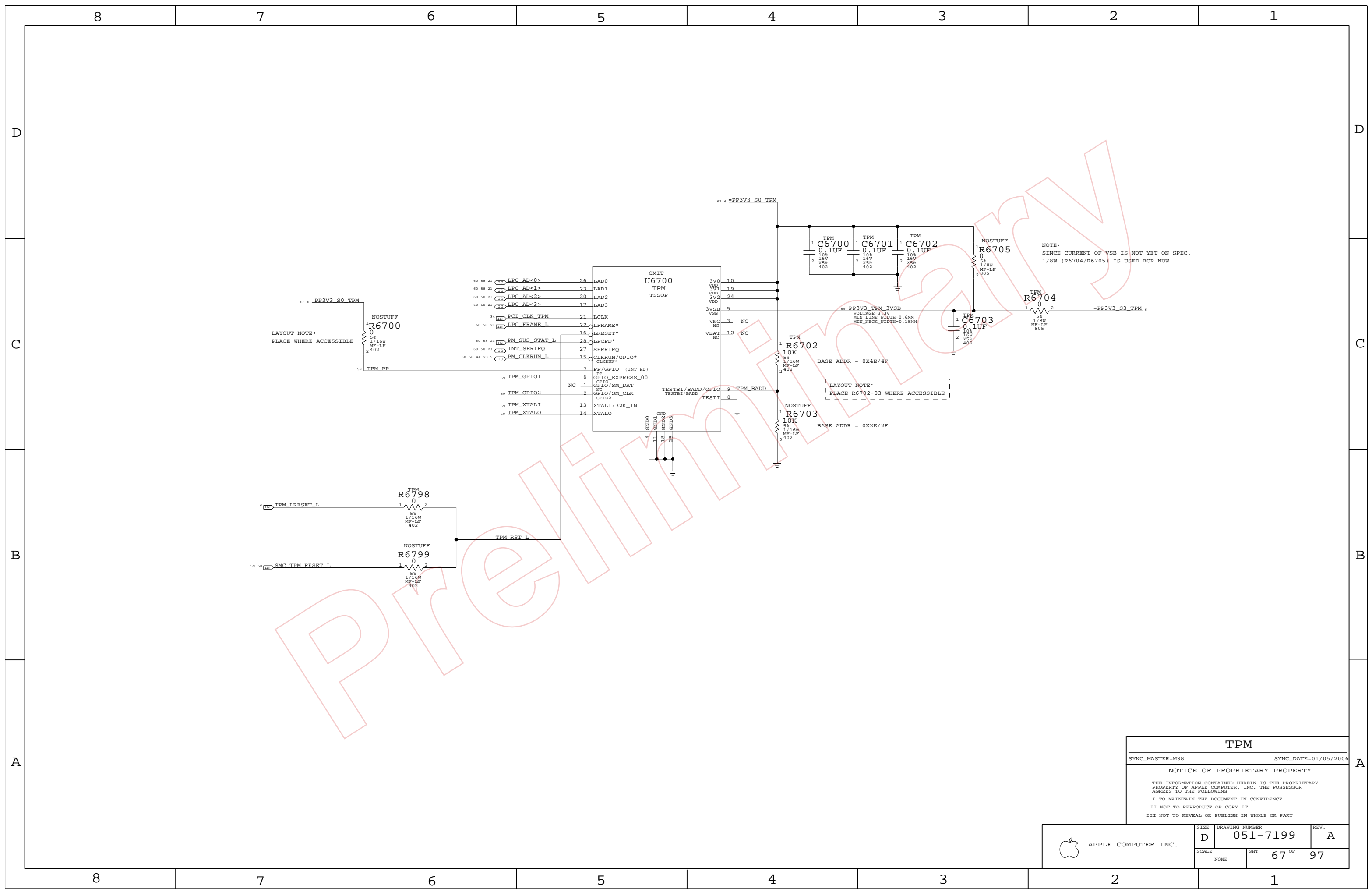
ODD TEMP SENSOR

Fan 2 & HD Temp

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	D	051-7199	A
SCALE	SHT	66 OF	97
NONE			



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

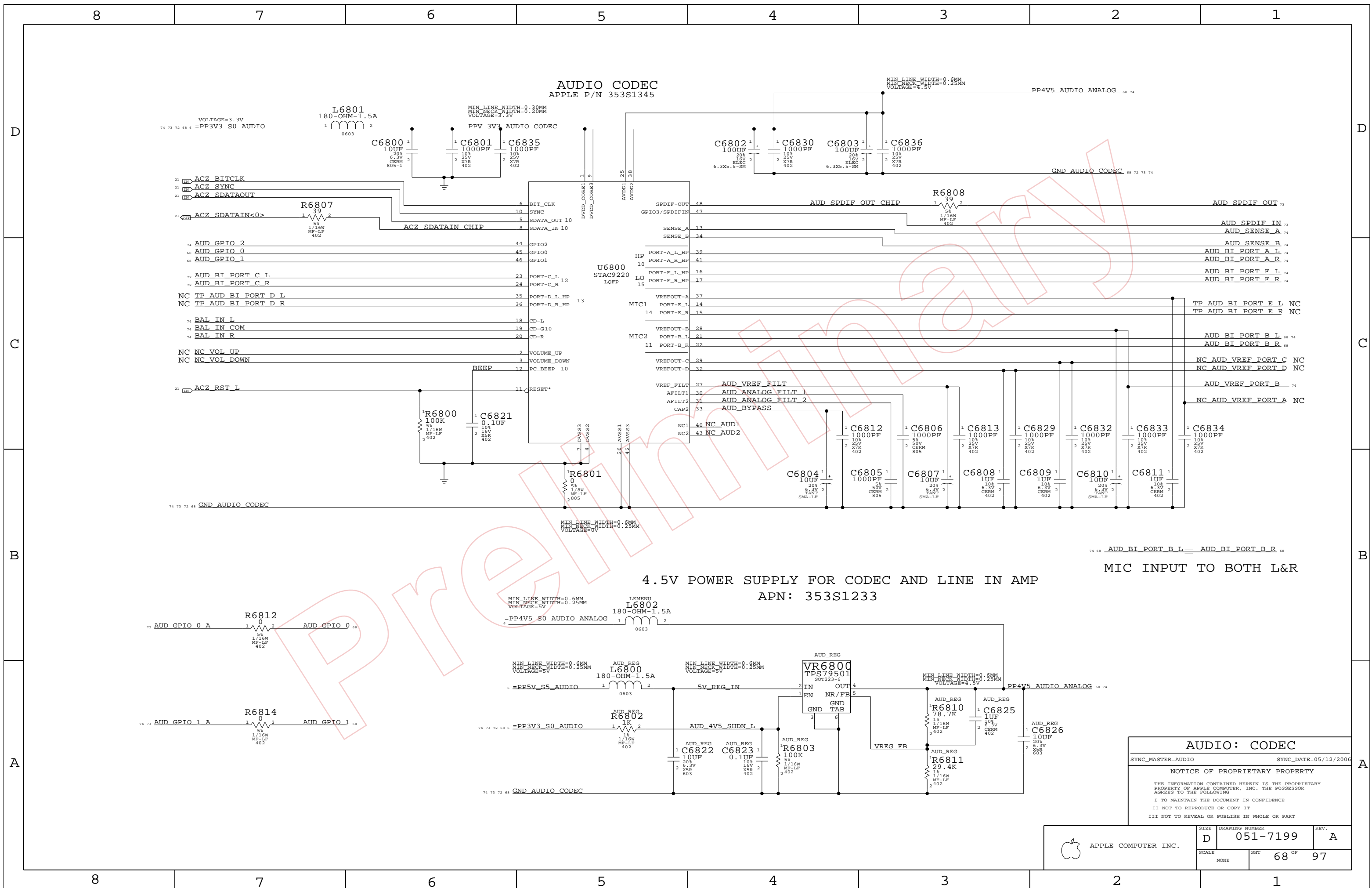
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7199	A
SCALE	SHT	67 OF 97	
NONE			



AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

NOTICE OF PROPRIETARY PROPERTY

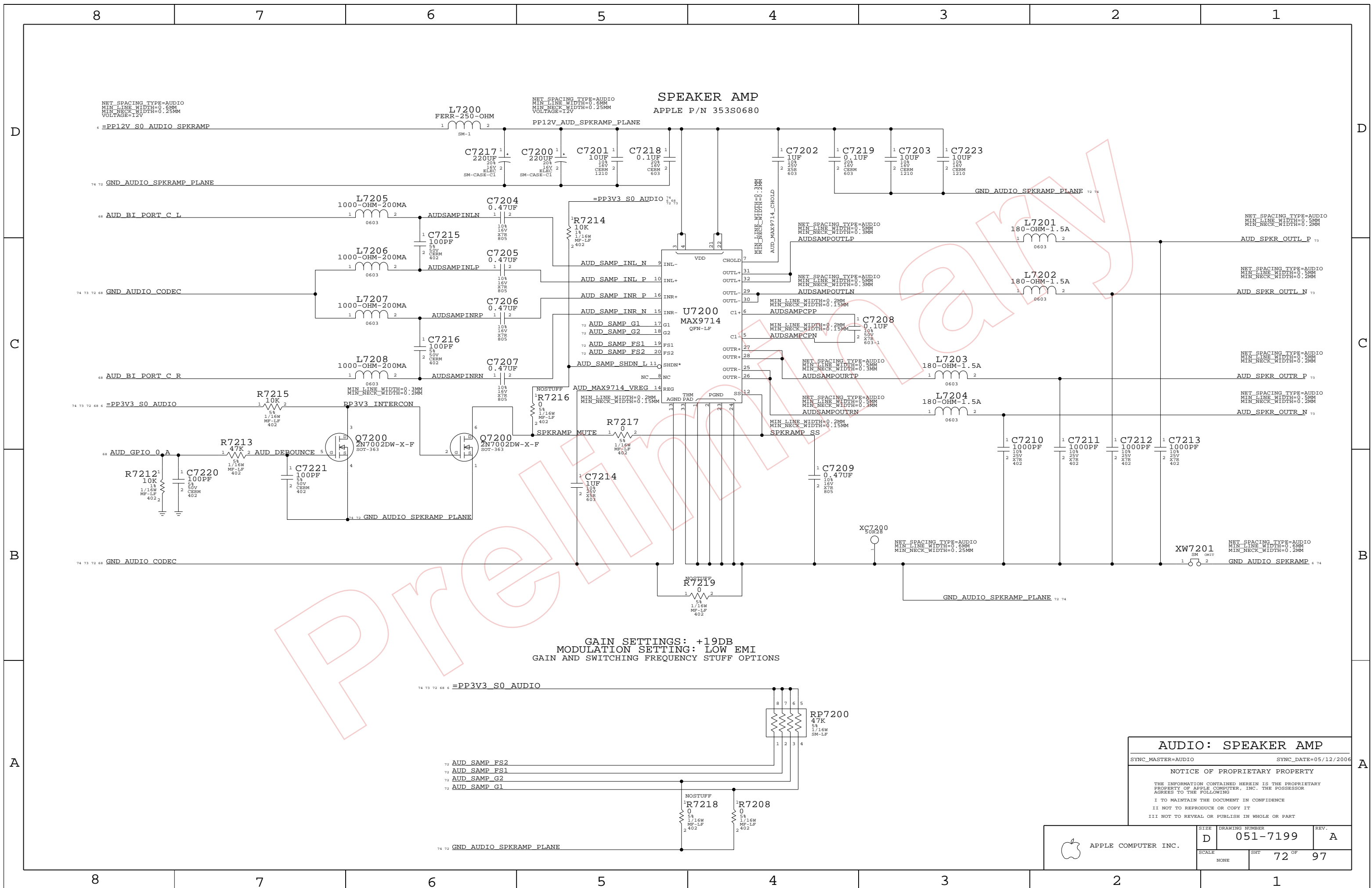
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	SCALE NONE	SHEET 68 OF 97	



SPEAKER AMP
APPLE P/N 353S0680

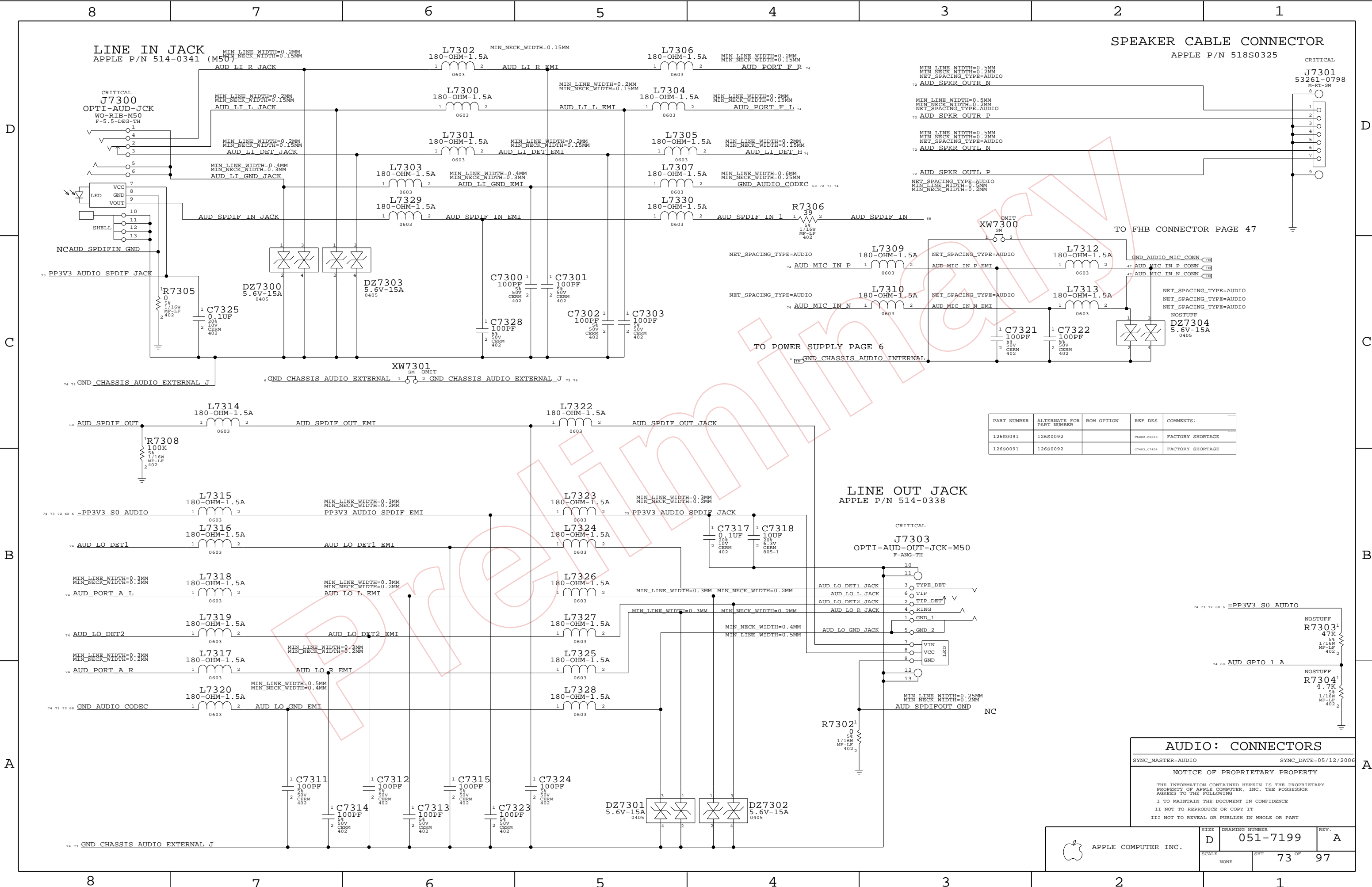
GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	D	051-7199	A
SCALE	SHT	72 OF 97	
NONE			

LINE IN JACK
APPLE P/N 514-0341 (M50)

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

LINE OUT JACK
APPLE P/N 514-0338

AUDIO: CONNECTORS
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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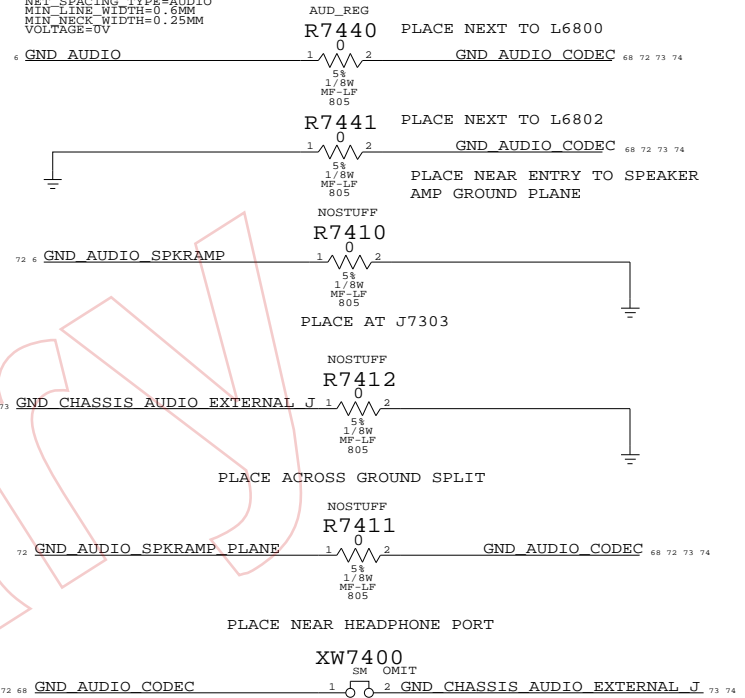
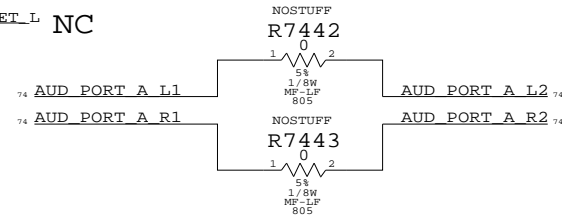
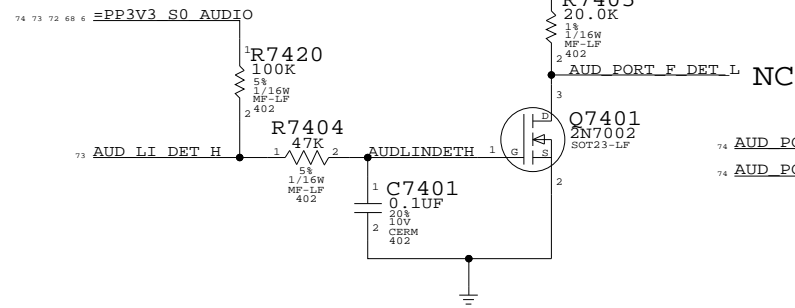
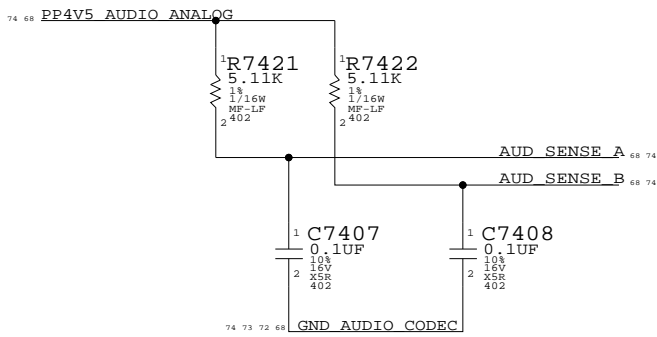
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	73 OF	97
NONE			

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

NET SPACING TYPE=AUDIO
MIN LINE WIDTH=0.6MM
MIN SPC WIDTH=0.25MM
VOLTAGE=0V

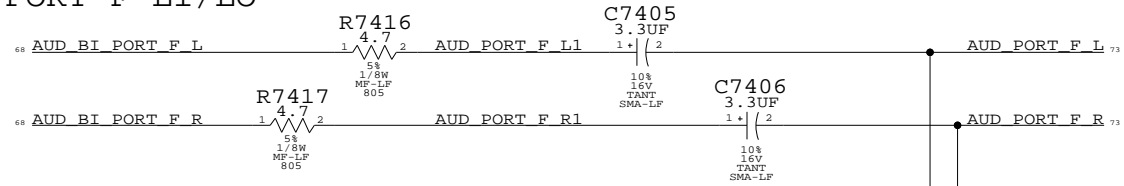
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



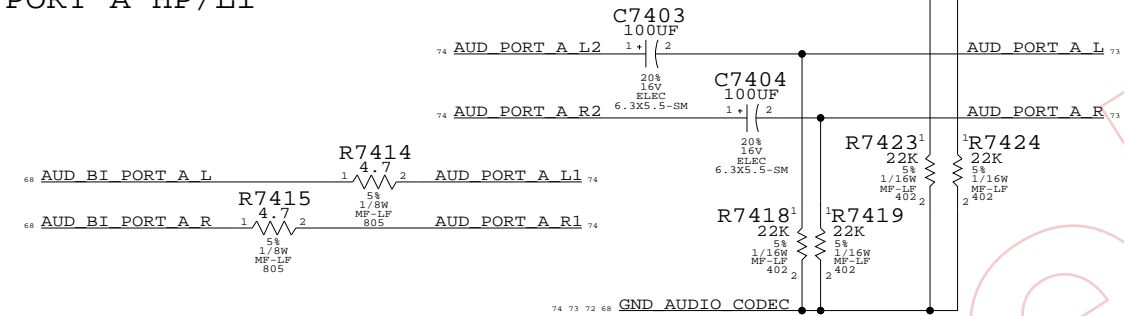
USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E
PORT D

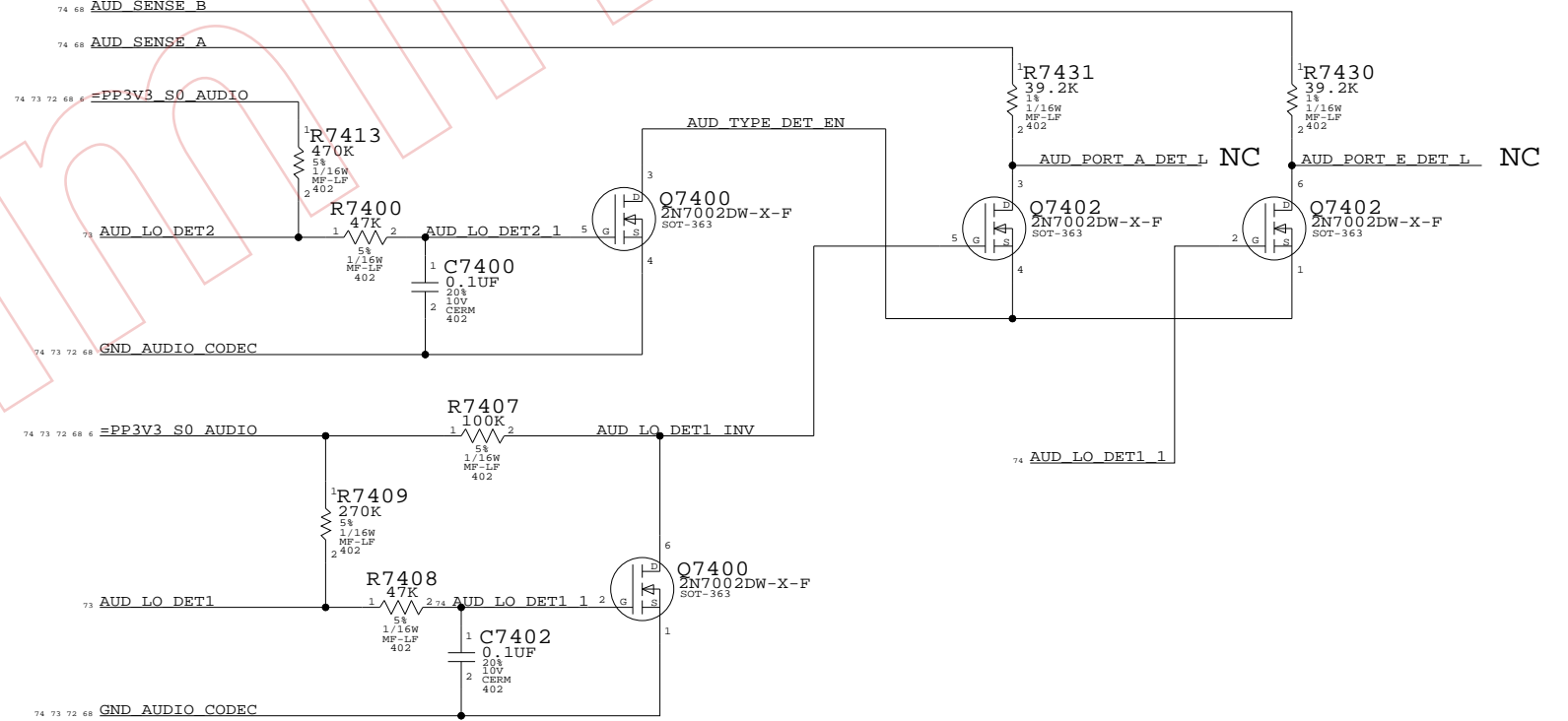
PORT F LI/LO



PORT A HP/LI

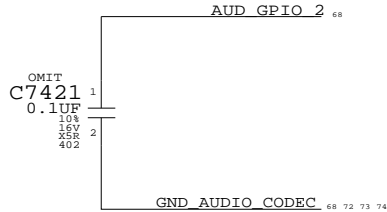


PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

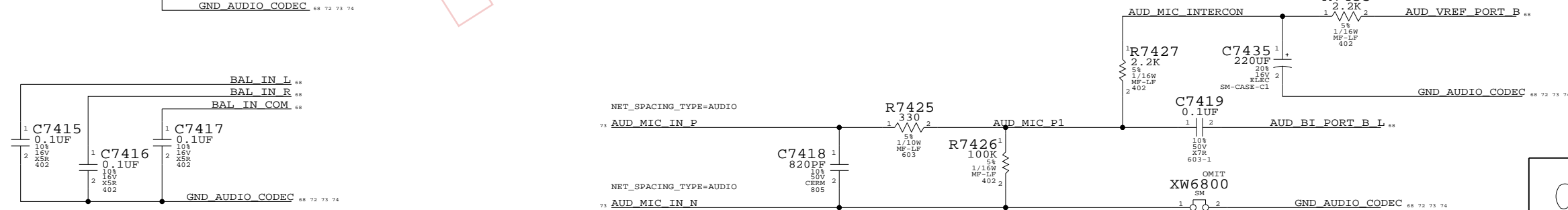


UNUSED PORT TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA



MICROPHONE IMPEDANCE MATCHING CIRCUIT



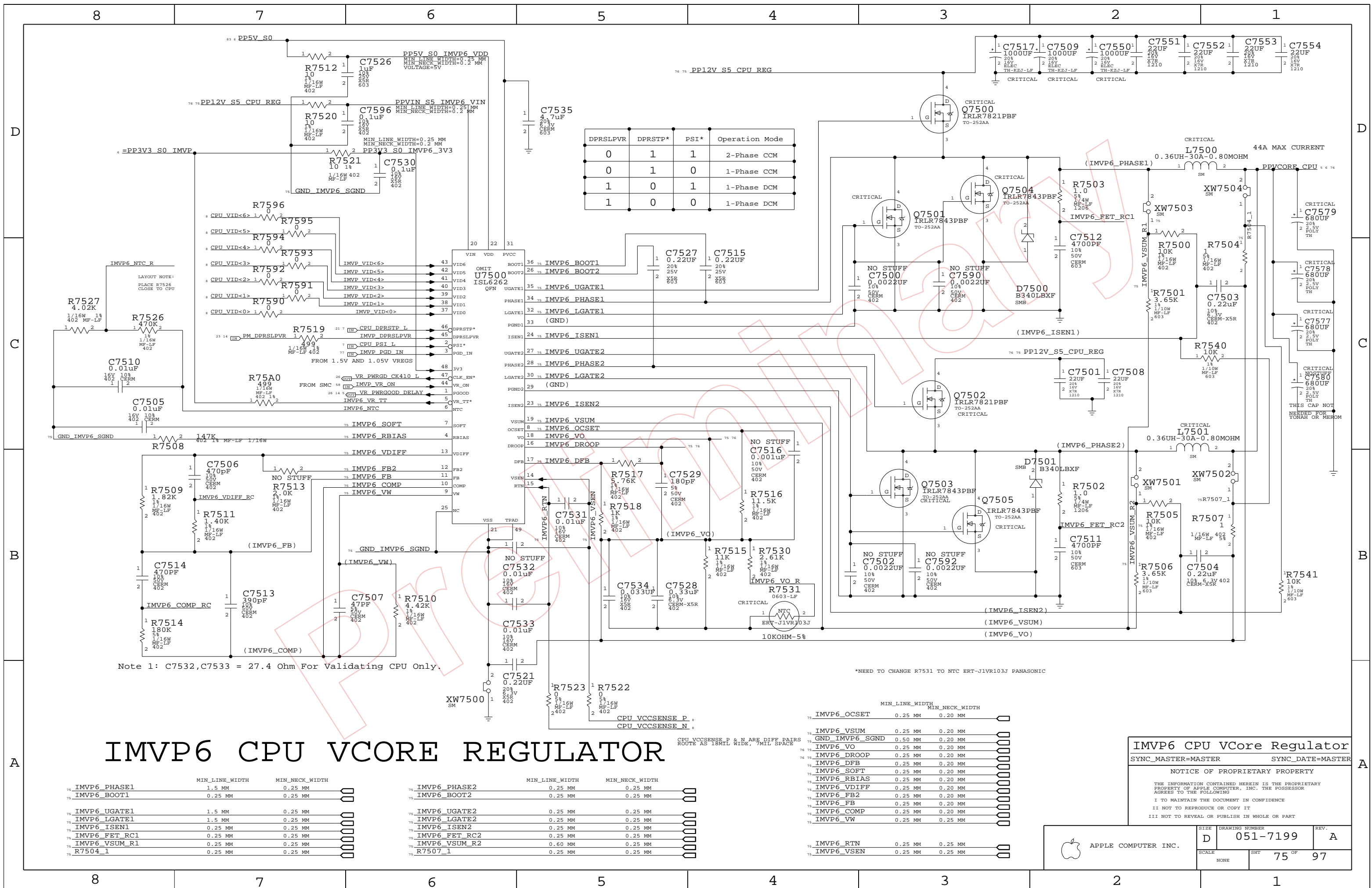
AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

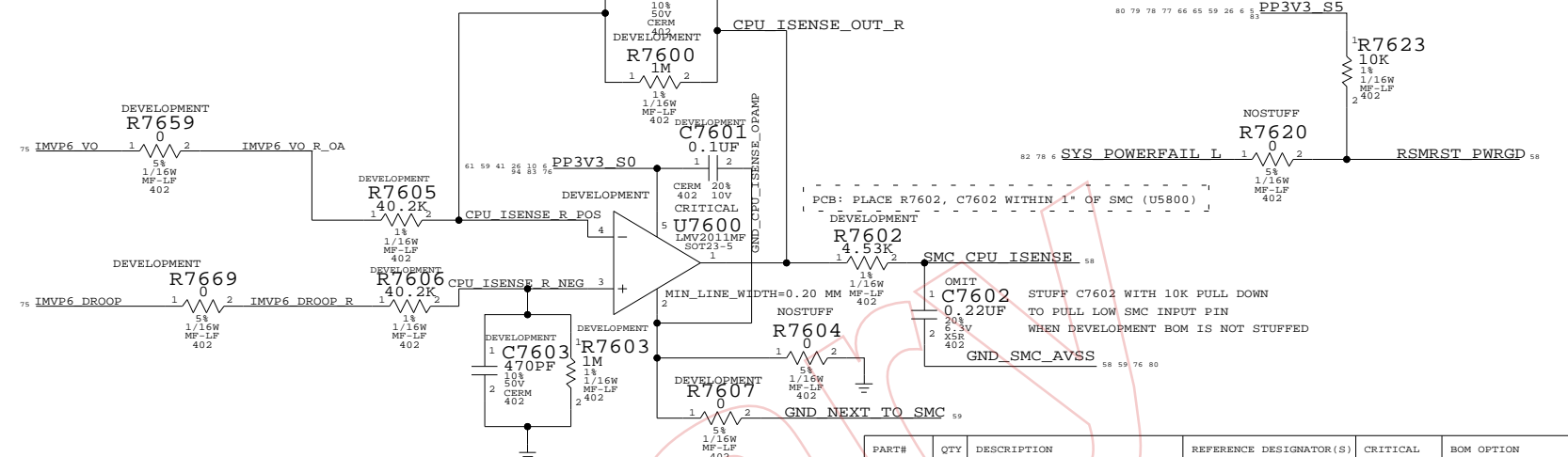
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

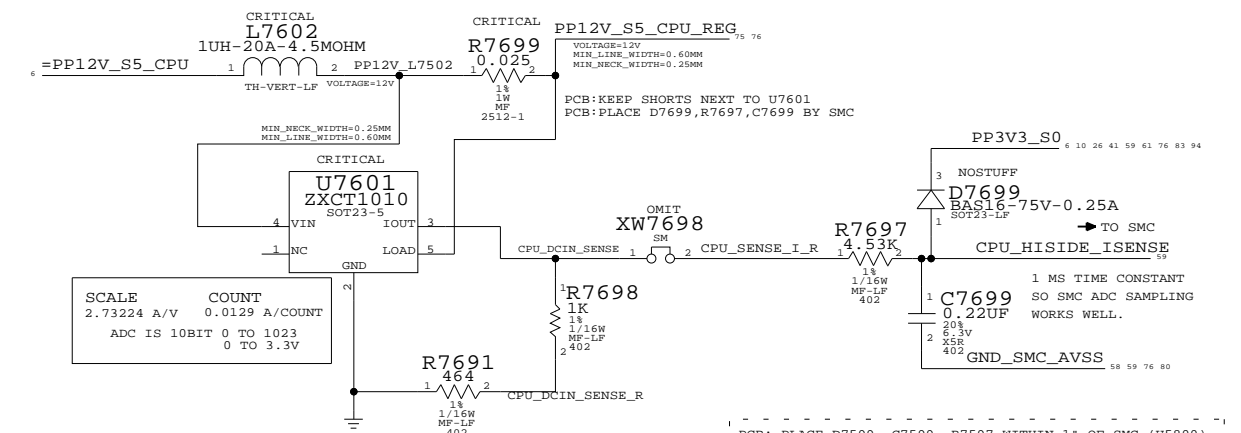
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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7199	REV.: A
	SCALE: NONE	SHEET: 75 OF 97	

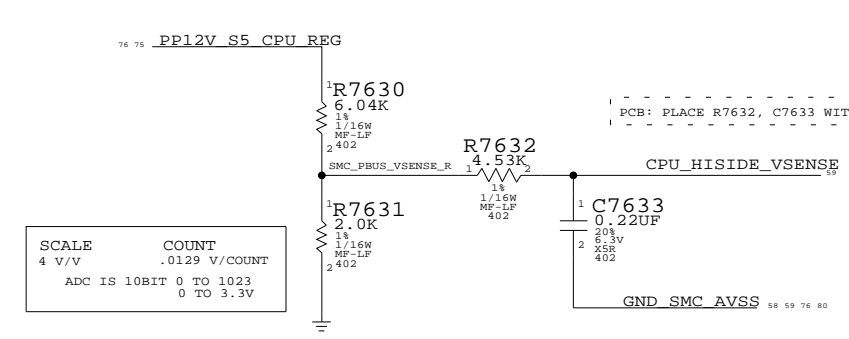
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)



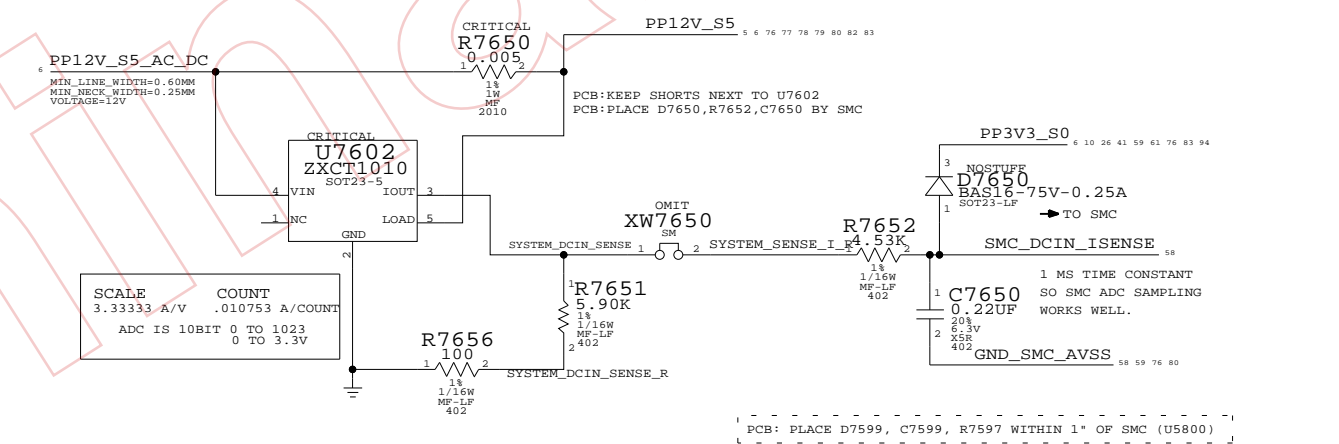
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



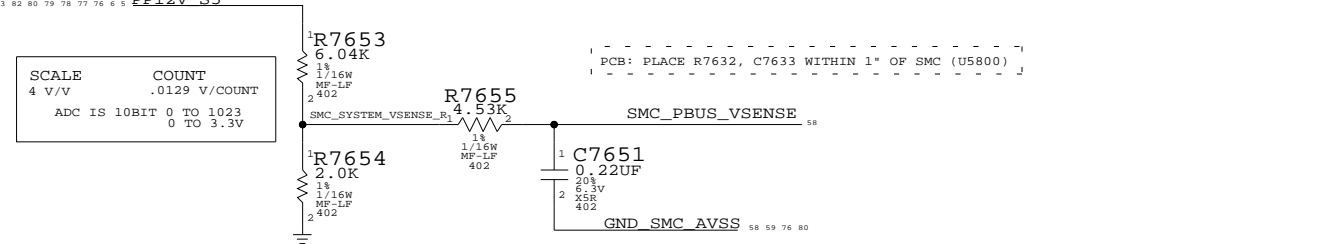
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



SYSTEM CURRENT SENSE

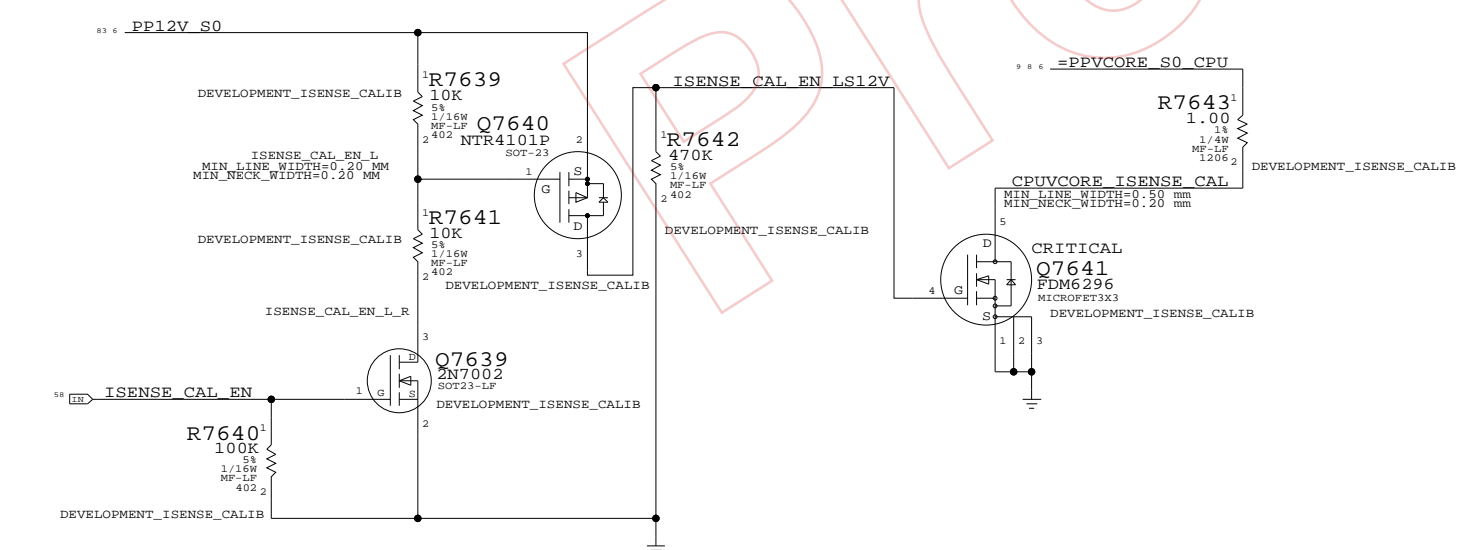


SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

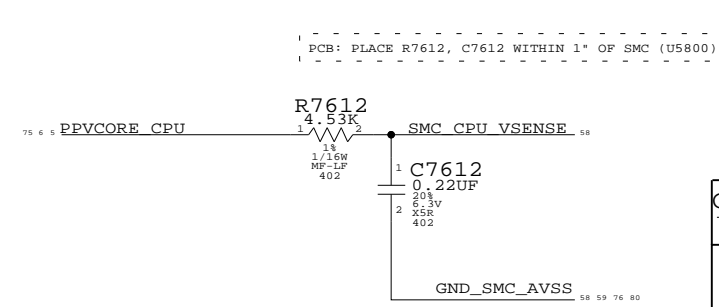


Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

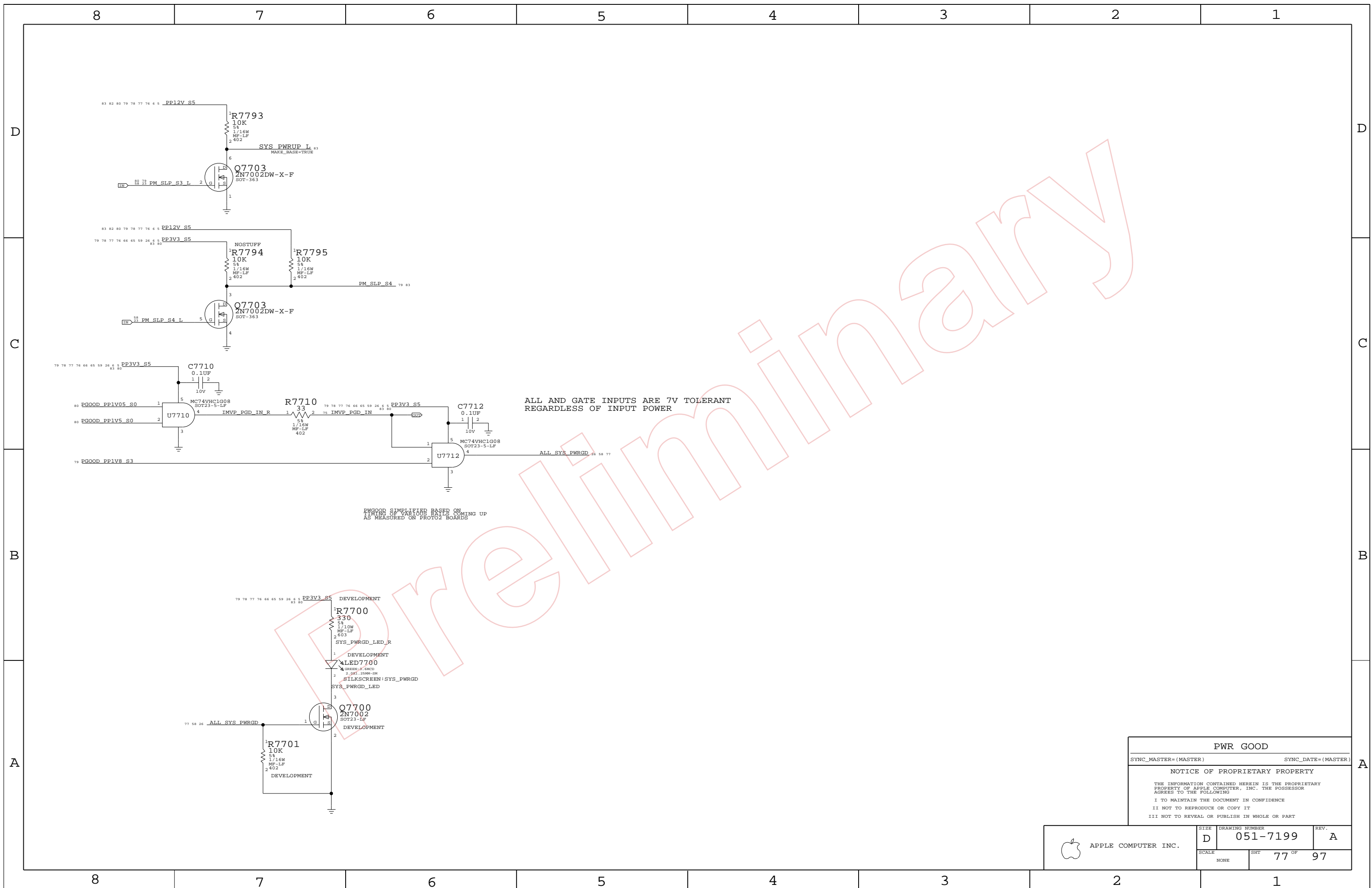


PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWRGOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS


PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

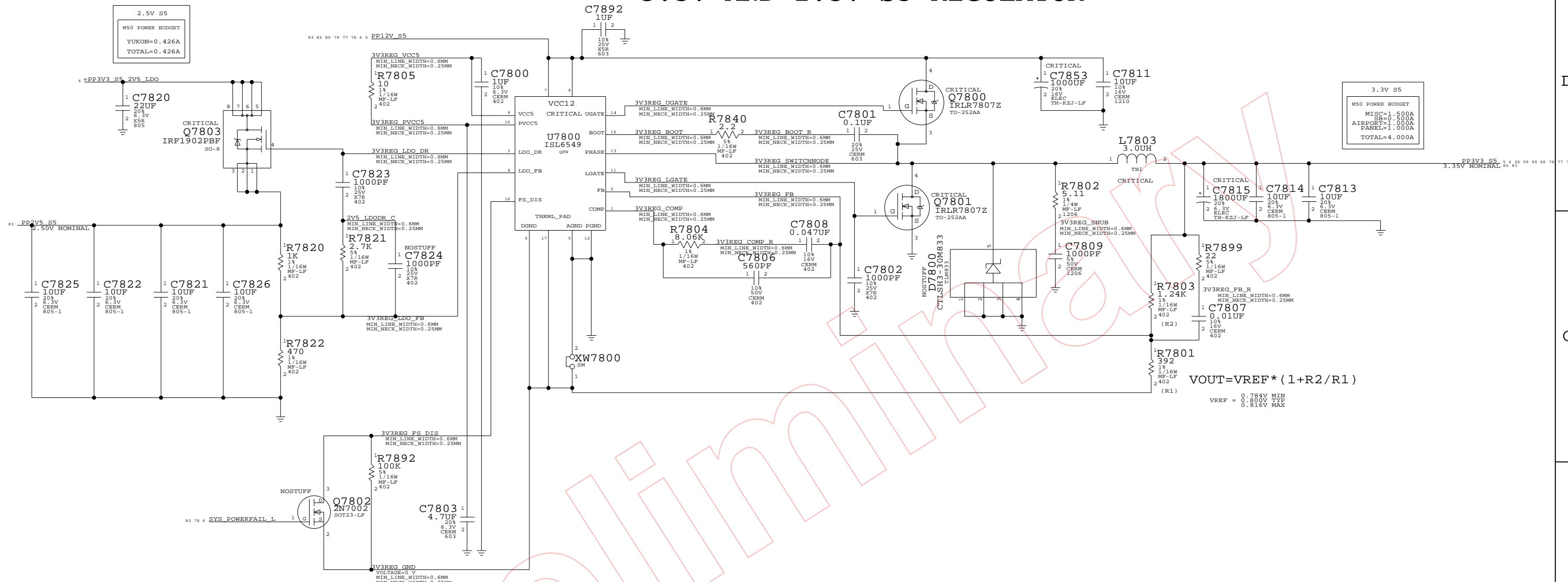
NOTICE OF PROPRIETARY PROPERTY

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PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
AGREES TO THE FOLLOWING

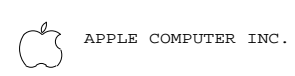
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHT 77 OF	97

3.3V AND 2.5V S5 REGULATOR



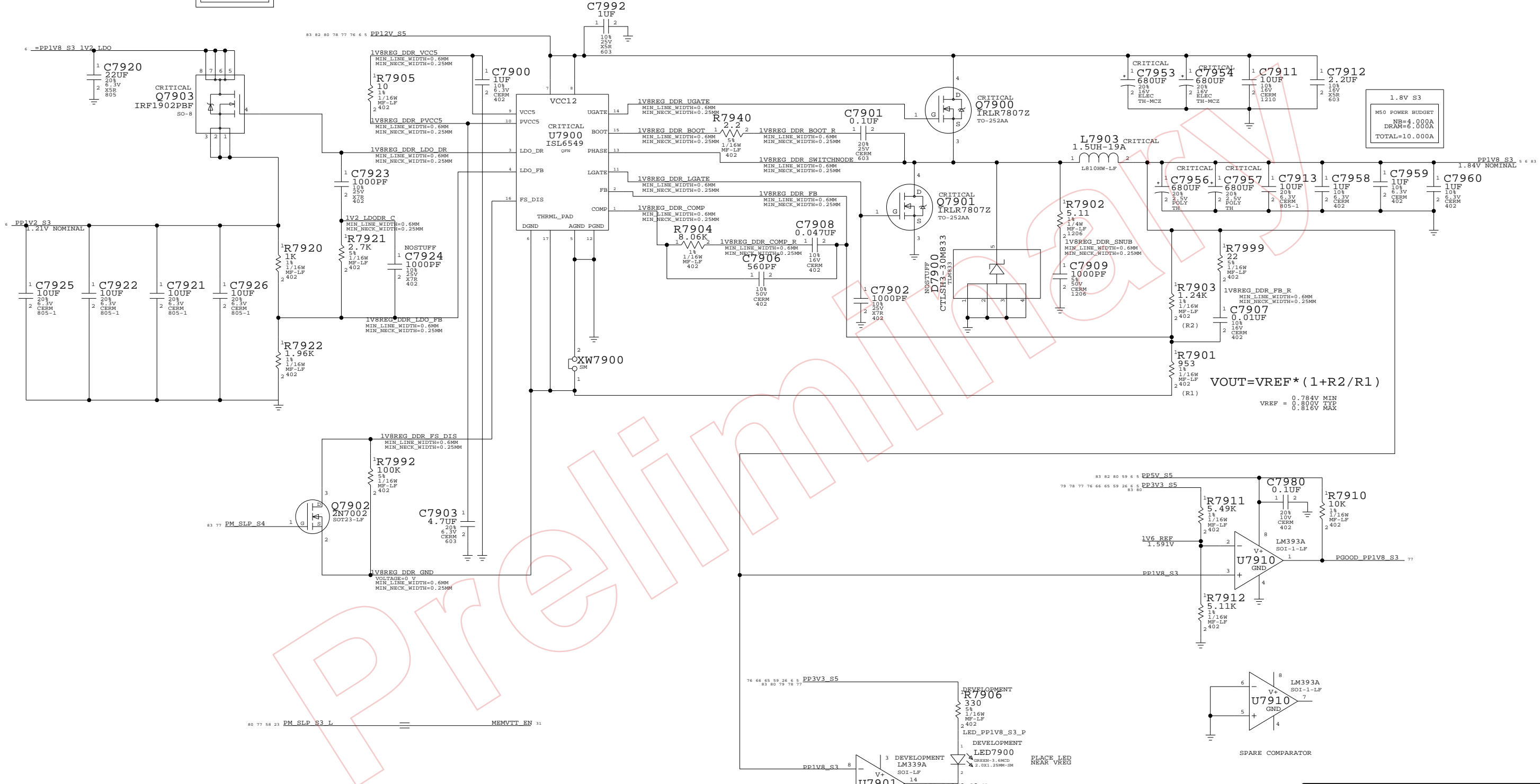
3V DC/DC 2.5V		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY		
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II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
SIZE	DRAWING NUMBER	REV.
D	051-7199	A
SCALE	SHT	78 OF 97
NONE		
TRUE		



1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NE=4.000A
DRAM=6.000A
TOTAL=10.000A



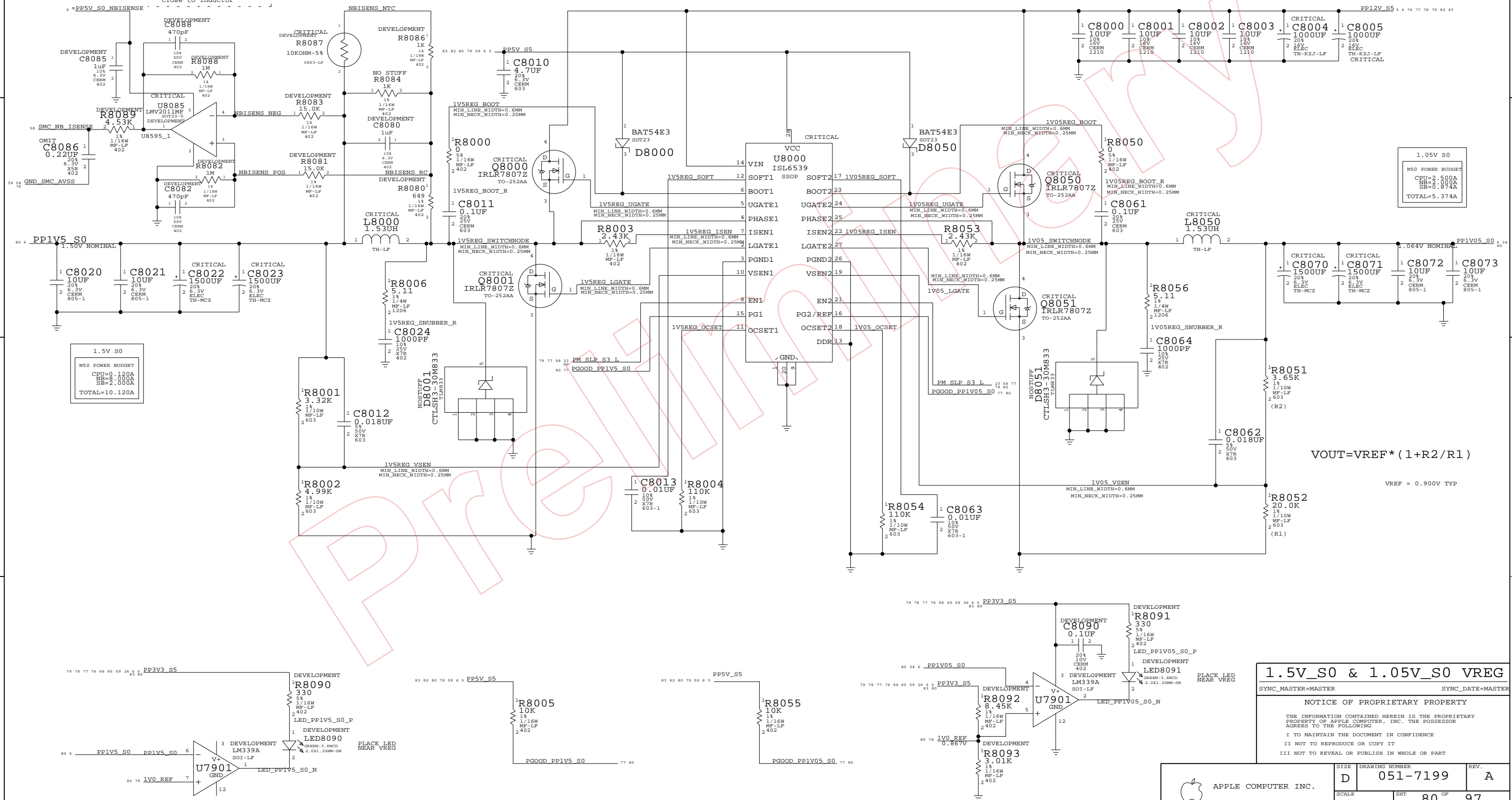
1.8V & 1.2V VREG
SYNC_MASTER=MASTER SYNC_DATE=MASTER
NOTICE OF PROPRIETARY PROPERTY
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	79 OF	97
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V S0
MS0 POWER BUDGET
CPU=0.120A
NB=8.0000A
SB=2.0000A
TOTAL=10.120A

1.05V S0
MS0 POWER BUDGET
CPU=2.500A
NB=2.0000A
SB=0.874A
TOTAL=5.374A

$$V_{OUT} = V_{REF} * (1 + R_2/R_1)$$

VREF = 0.900V TYP

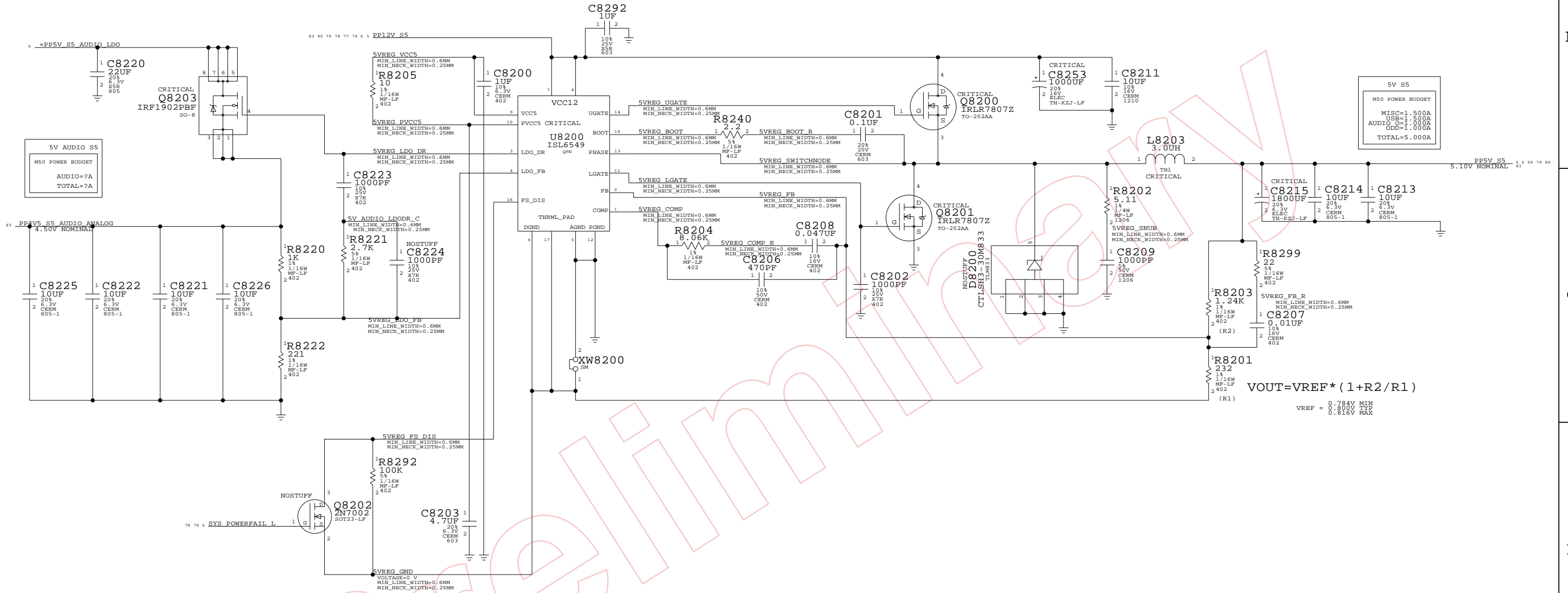
1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR

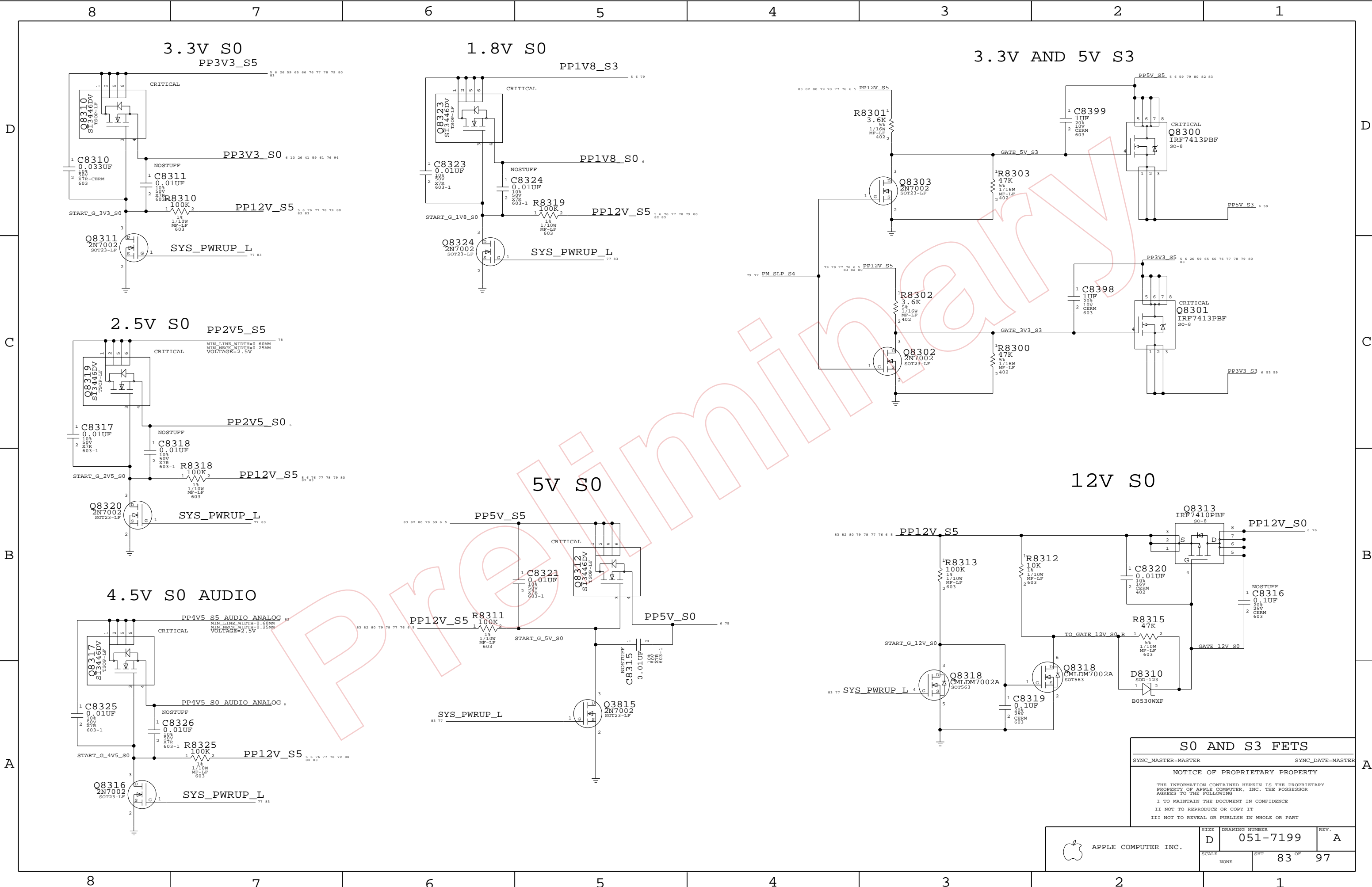


$V_{OUT} = V_{REF} * (1 + R2/R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
NOTICE OF PROPRIETARY PROPERTY	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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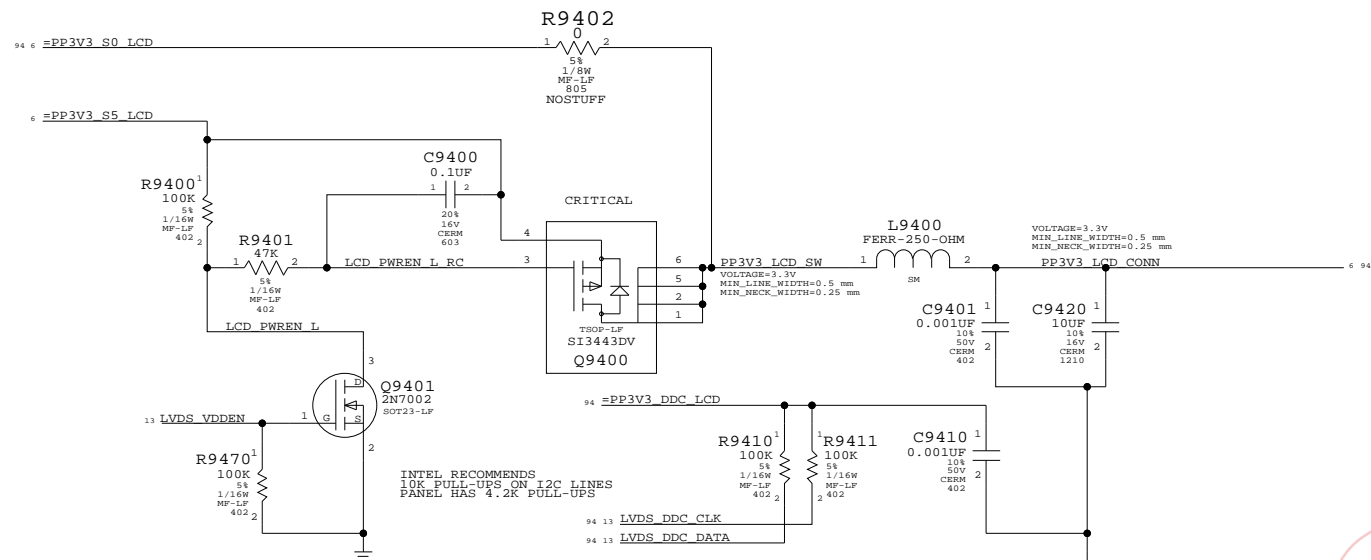
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

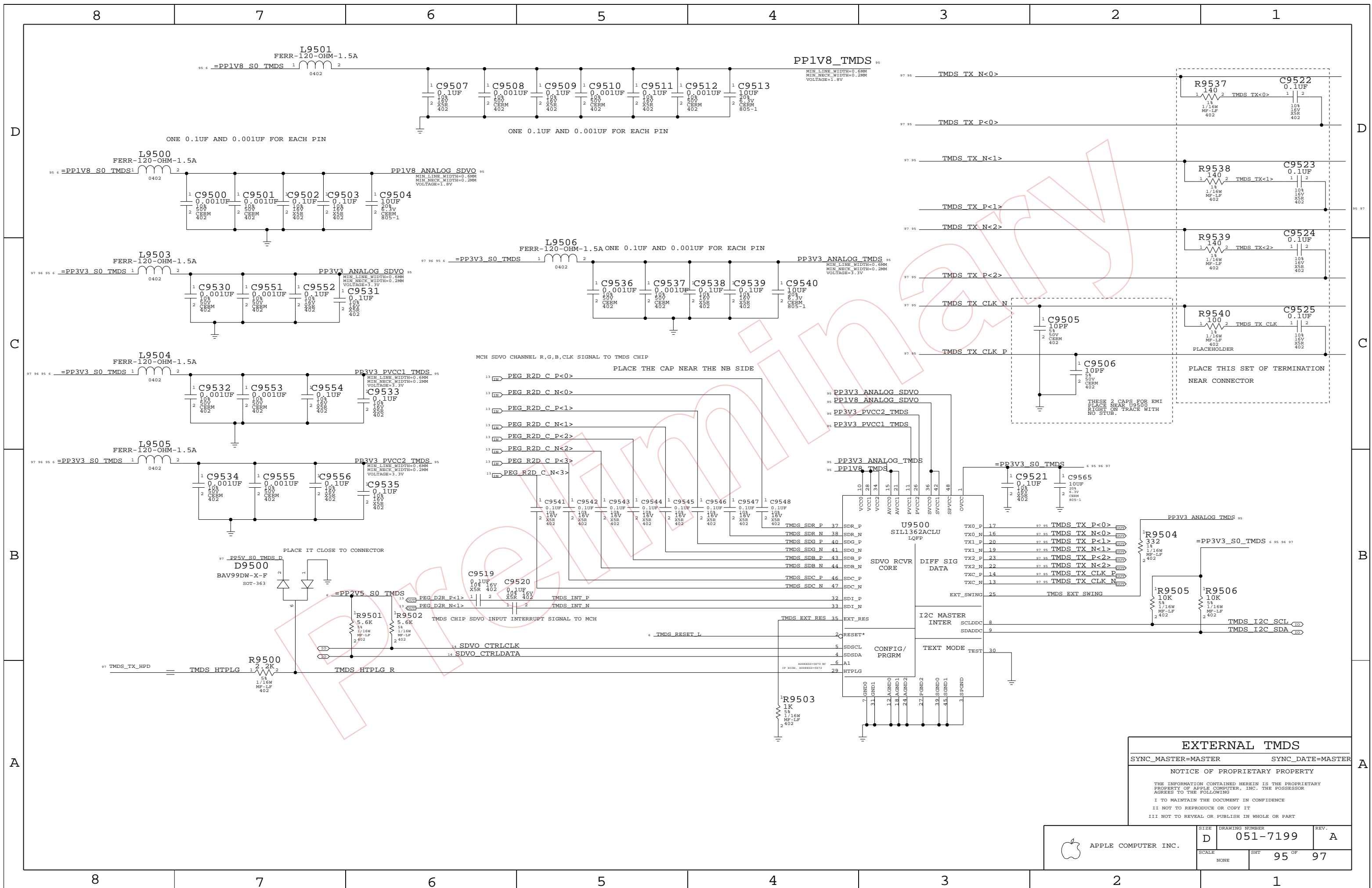
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 83 OF 97	

LCD (LVDS) INTERFACE

INVERTER INTERFACE



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	94 OF	97
NONE			



EXTERNAL TMSD

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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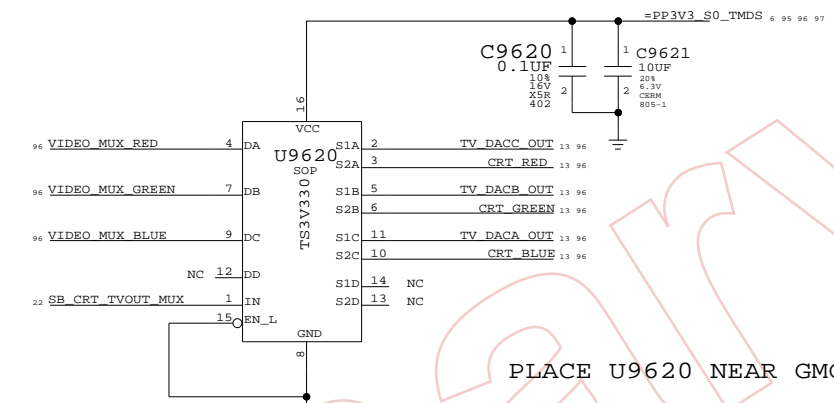
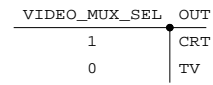
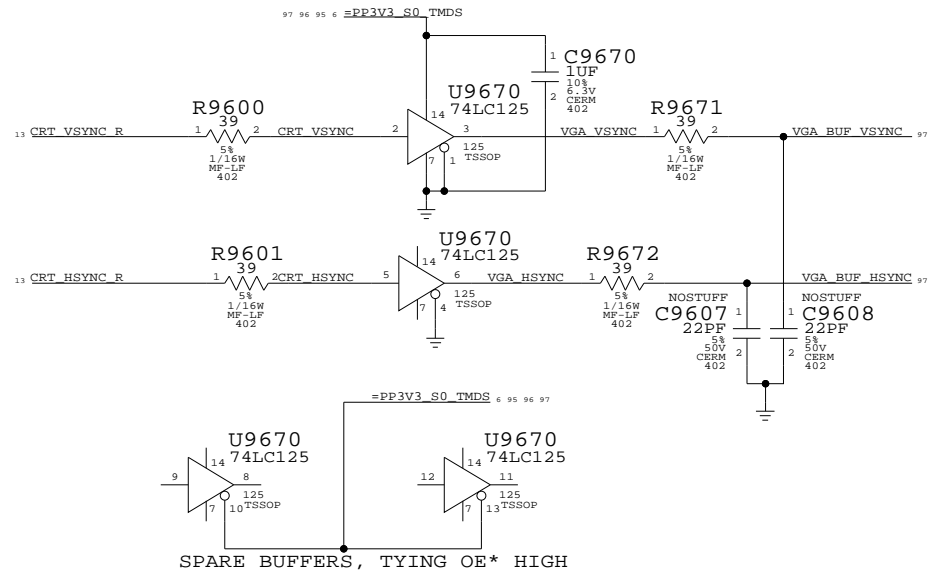
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

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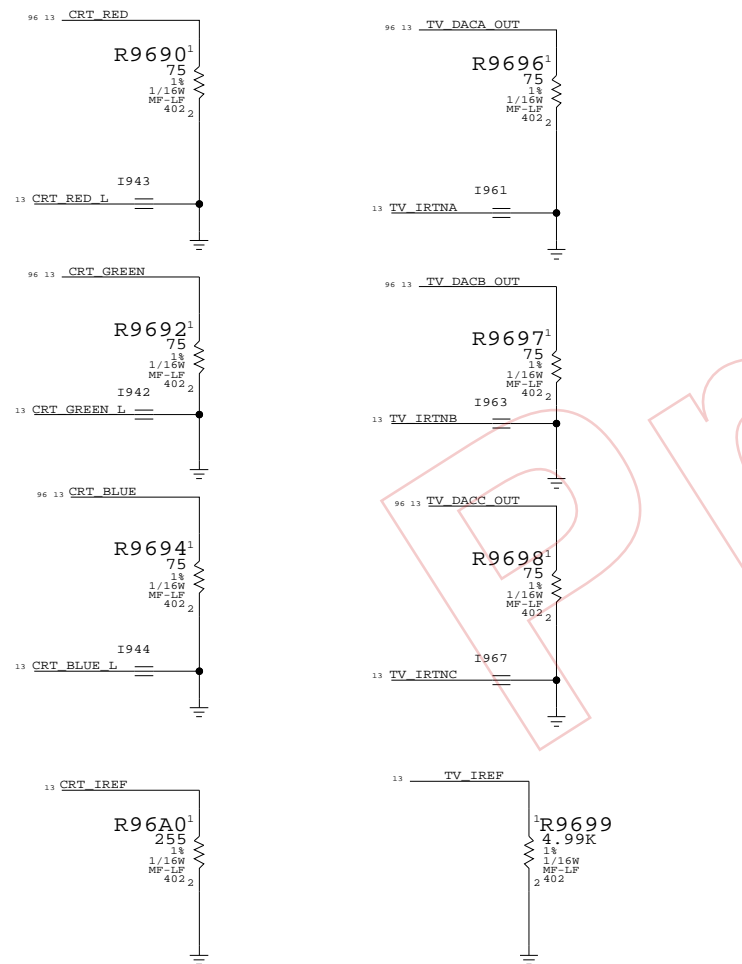
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. A
	SCALE NONE	SHEET 95 OF 97	

VGA SYNC BUFFERS

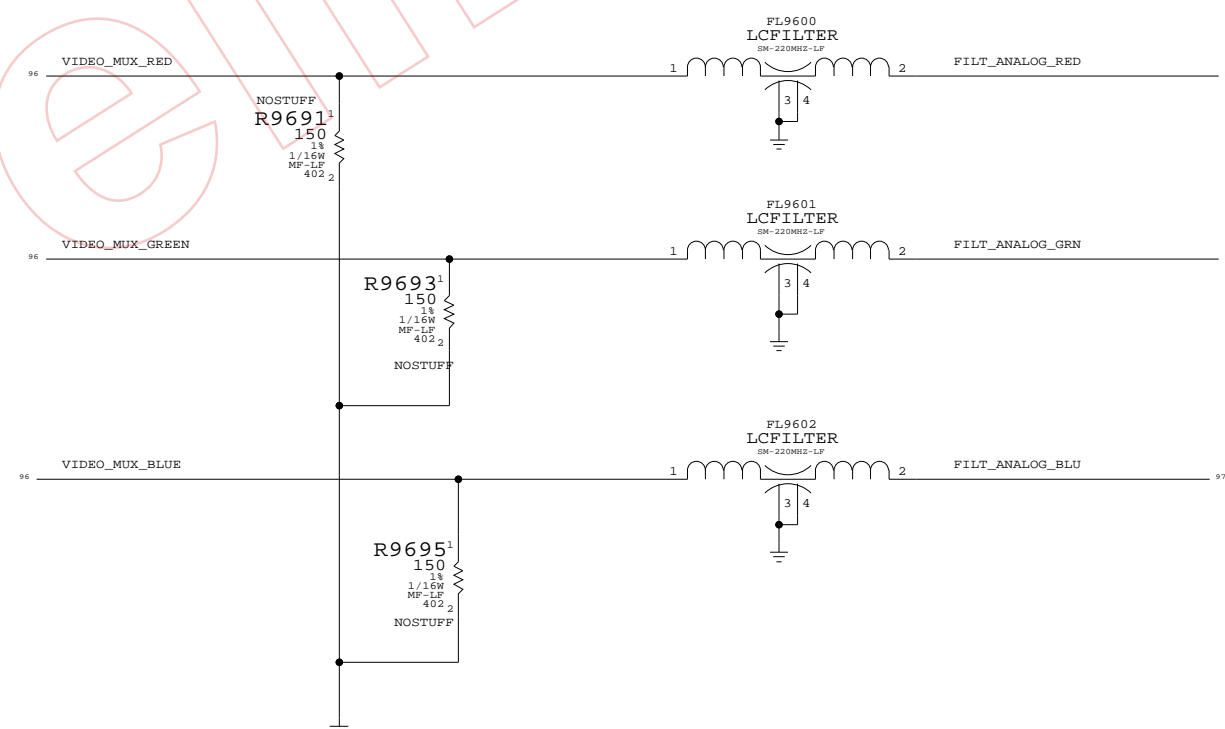


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE

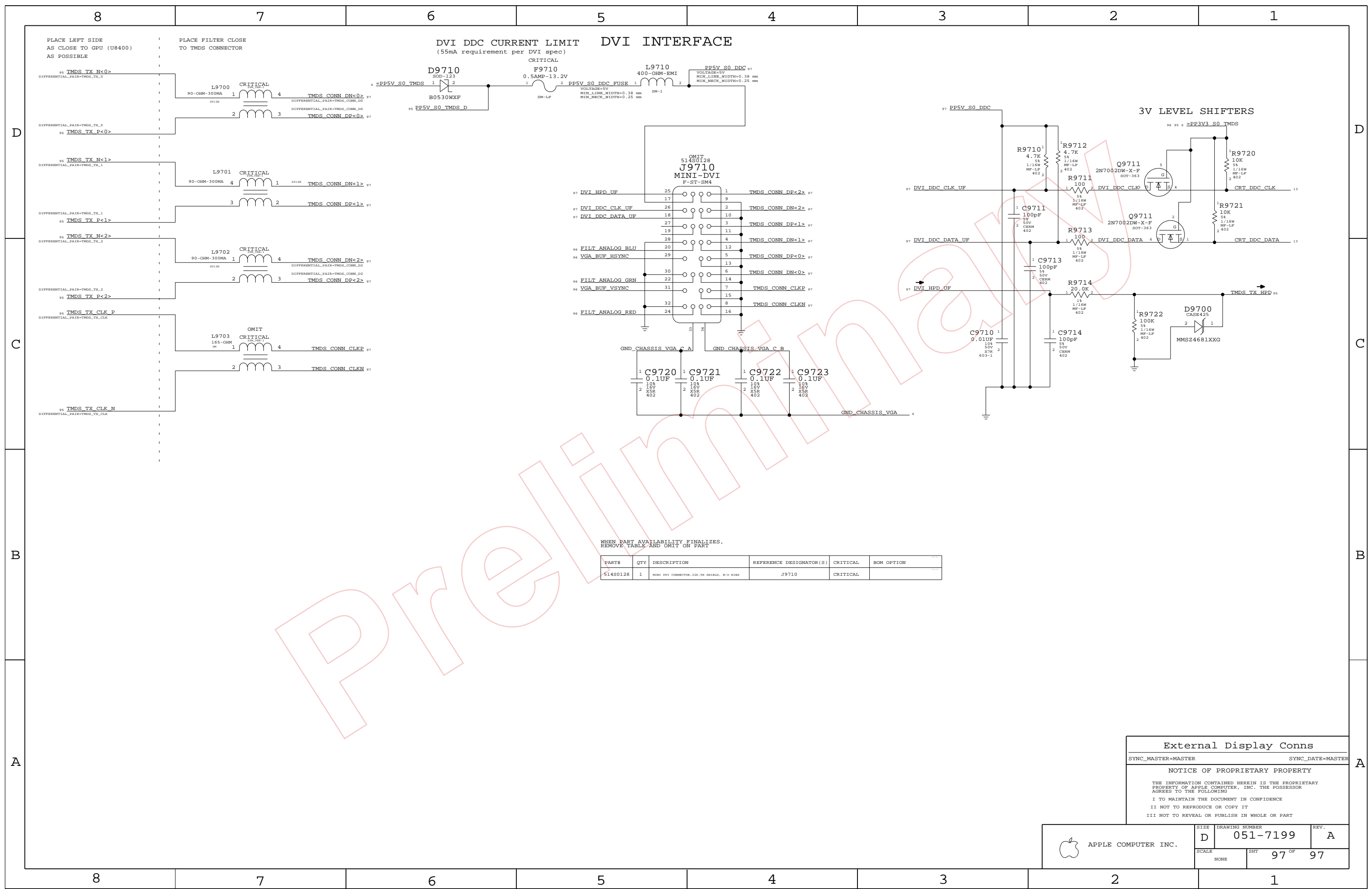


ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	A
SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

DVI INTERFACE

MINI-DVI
F-ST-SM4

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 25P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	A
SCALE	SHT	97 OF	97
NONE			