

# IM4, 2 - REV B

09/11/06

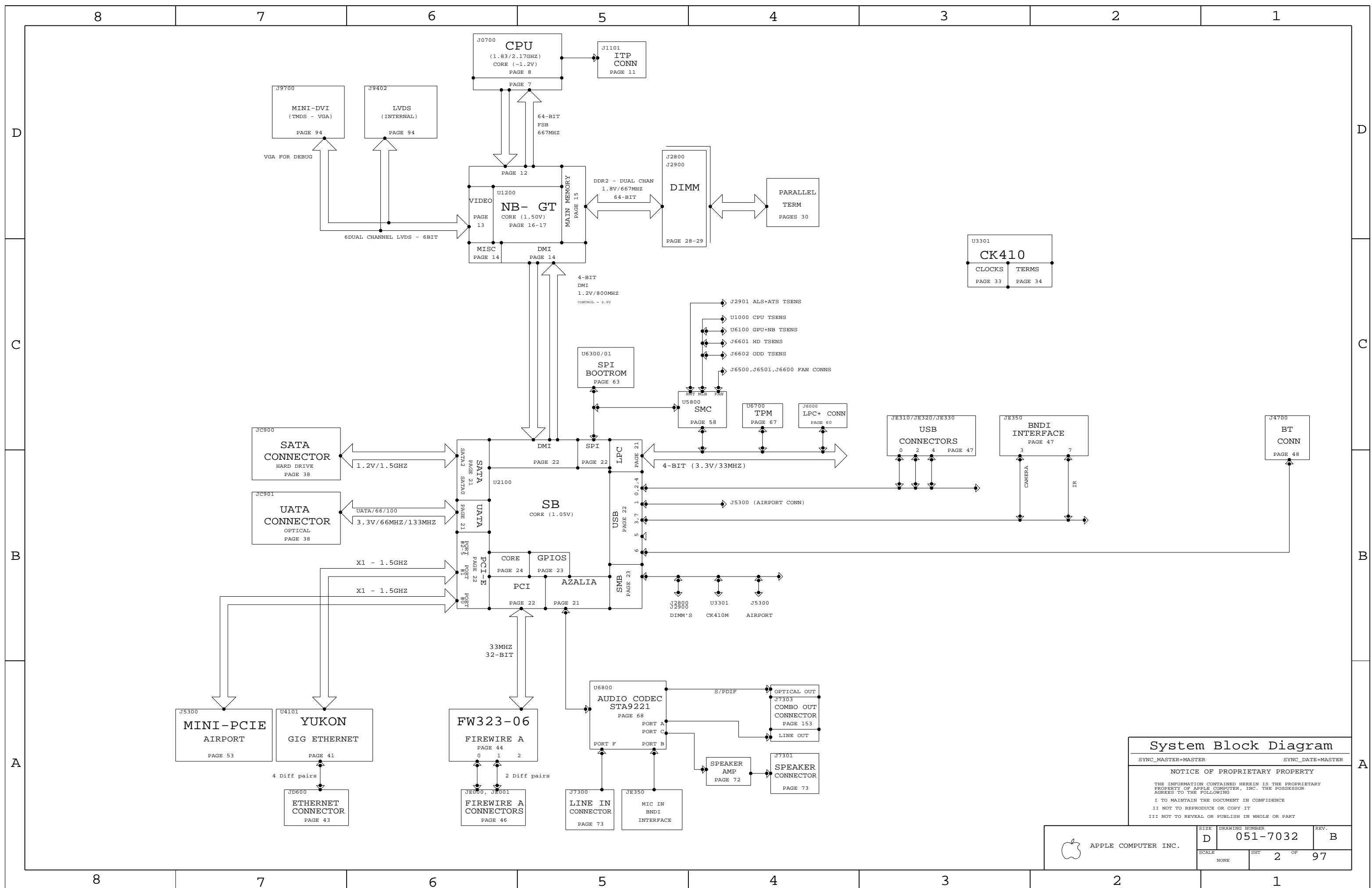
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
B		461143	PRODUCTION RELEASED	09/12/06	06/22/04

PDF	CSA	CONTENTS	SYNC MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER
3	3	Power Block Diagram	MASTER	MASTER
4	4	Table Items	MASTER	MASTER
5	5	FUNC TEST 1 OF 2	MASTER	MASTER
6	6	Power Conn / Alias	MASTER	MASTER
7	7	CPU 1 OF 2-FSB	MASTER	MASTER
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER
9	9	CPU DECAPS & VID<>	MASTER	MASTER
10	10	CPU TEMP SENSOR	MASTER	MASTER
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006
12	12	NB CPU Interface	M1	01/05/2006
13	13	NB PEG / Video Interfaces	M1	01/05/2006
14	14	NB Misc Interfaces	MASTER	MASTER
15	15	NB DDR2 Interfaces	M1	01/05/2006
16	16	NB Power 1	MASTER	MASTER
17	17	NB Power 2	M40	01/05/2006
18	18	NB Grounds	M1	01/05/2006
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)
20	20	NB Config Straps	M1	01/05/2006
21	21	SB: 1 OF 4	M38	01/05/2006
22	22	SB: 2 OF 4	MASTER	MASTER
23	23	SB: 3 OF 4	MASTER	MASTER
24	24	SB: 4 OF 4	M38	01/05/2006
25	25	SB: DECOUPLING	MASTER	MASTER
26	26	SB: MISC	MASTER	MASTER
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER
30	30	Memory Active Termination	MASTER	MASTER
31	31	Memory Vtt Supply	MASTER	MASTER
32	33	CLOCKS	MASTER	MASTER
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER
34	38	Disk Connectors	MASTER	MASTER
35	41	ETHERNET CONTROLLER	MASTER	MASTER
36	42	ETHERNET MISC	MASTER	MASTER
37	43	ETHERNET CONNECTOR	MASTER	MASTER

PDF	CSA	CONTENTS	SYNC MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER
39	45	FW: DECAPS	MASTER	MASTER
40	46	FIREWIRE CONNECTORS	MASTER	MASTER
41	47	USB Device Interfaces	MASTER	MASTER
42	53	AIRPORT CONN	MASTER	MASTER
43	54	PCIE PORT ALIASES	MASTER	MASTER
44	58	SMC	M1	01/05/2006
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)
46	60	LPC+ CONN	M38	12/09/2005
47	61	NB THERMAL	MASTER	MASTER
48	63	SPI BOOTROM	M38	01/05/2006
49	65	Fan 0, 1 & System Temp	MASTER	MASTER
50	66	Fan 2 & HD Temp	MASTER	MASTER
51	67	TPM	M38	01/05/2006
52	68	AUDIO: CODEC	AUDIO	05/12/2006
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER
57	76	CPU & SYSTEM SENSE CIRCUI	(MASTER)	(MASTER)
58	77	PWR GOOD	(MASTER)	(MASTER)
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)
60	79	1.8V & 1.2V VREG	MASTER	MASTER
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER
62	82	5V DC/DC	MASTER	MASTER
63	83	S0 AND S3 FETS	MASTER	MASTER
64	94	Internal Display Conns	MASTER	MASTER
65	95	EXTERNAL TMD5	MASTER	MASTER
66	96	TMD5/Inverter/ExtVGA	MASTER	MASTER
67	97	External Display Conns	MASTER	MASTER

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p><b>METRIC</b></p>	<div style="text-align: right;"> <p>Apple Computer Inc.</p> </div> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small; text-align: center;">II. NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small; text-align: center;">III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <div style="text-align: center;"> <p><b>SCHEM VALLCO</b></p> </div>																						
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAWER</td> <td style="width: 25%;">DESIGN CK</td> <td style="width: 25%;">MFG APPD</td> <td style="width: 25%;">DESIGNER</td> </tr> <tr> <td>ENG APPD</td> <td></td> <td></td> <td></td> </tr> <tr> <td>QA APPD</td> <td></td> <td></td> <td></td> </tr> <tr> <td>RELEASE</td> <td></td> <td>SCALE</td> <td>NONE</td> </tr> </table>	DRAWER	DESIGN CK	MFG APPD	DESIGNER	ENG APPD				QA APPD				RELEASE		SCALE	NONE	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> <td style="width: 50%;">SIZE D</td> </tr> </table>	MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">DRAWING NUMBER</td> <td style="width: 30%;">REV.</td> </tr> <tr> <td style="text-align: center;">051-7032</td> <td style="text-align: center;">B</td> </tr> </table>	DRAWING NUMBER	REV.	051-7032	B
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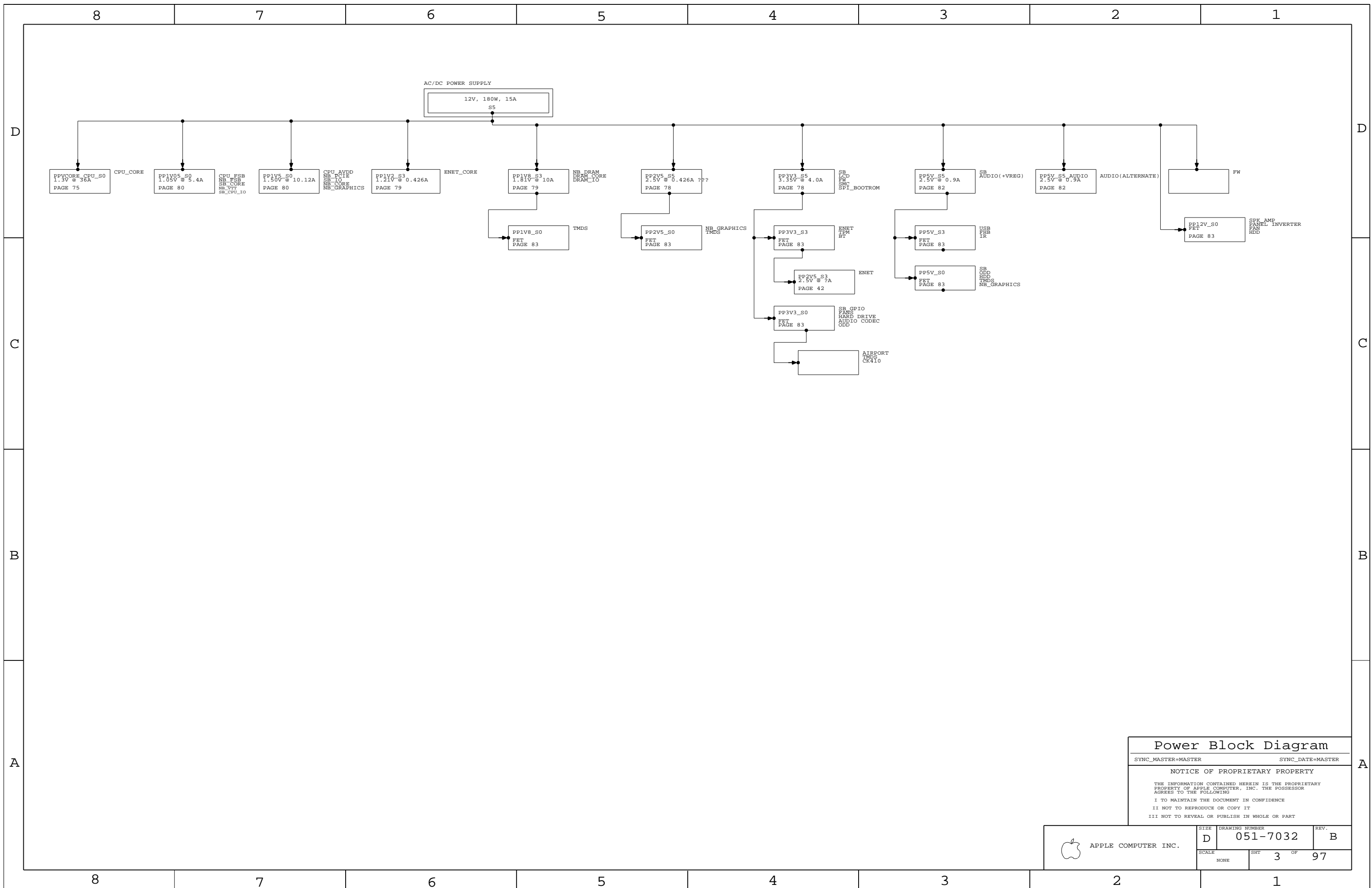
### System Block Diagram

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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SCALE	SHT	OF	
NONE	2	97	



**Power Block Diagram**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	OF	
NONE	3	97	

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## COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,888053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0021	1	EFI ROM,M50	U6301	CRITICAL	
337S3242	1	M38 CPU (C0)	CPU	CRITICAL	YONAH_1_83

341S1859 IC EFI BOOTROM DEV M50  
 337S3242 M38 CPU(C0)  
 337S3280 M50 1.83G LOW SPEED CPU (D0)  
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

## OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

## ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1235	353S1465		U7500	CPU VREG, NON-SCREENED PART

## MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:XOM]	CRITICAL	YONAH_1_83

## Table Items

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SIZE	DRAWING NUMBER	REV.
D	051-7032	B
SCALE	SHT	OF
NONE	4	97

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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

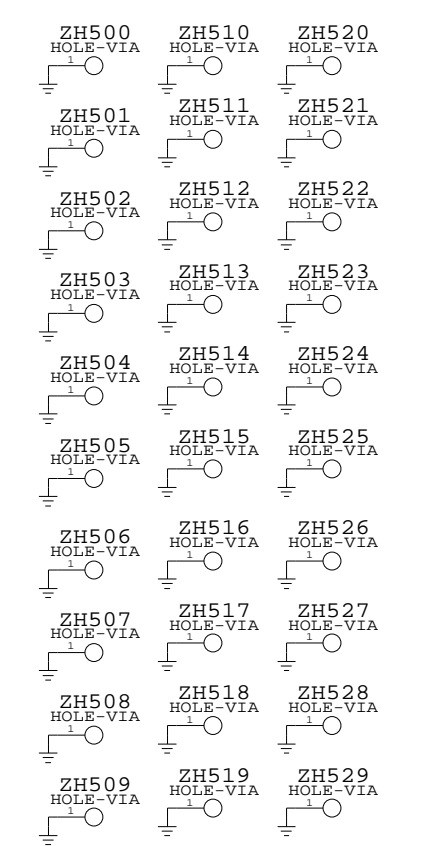
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

**FUNC TEST 1 OF 2**

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APPLE COMPUTER INC.

SCALE NONE SHEET 5 OF 97

DRAWING NUMBER 051-7032

REV. B

D

D

C

C

B

B

A

A

"S0" RAILS

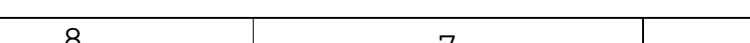
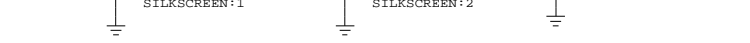
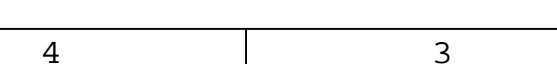
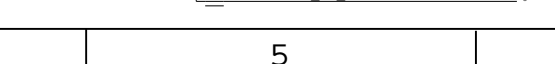
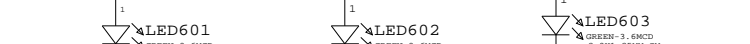
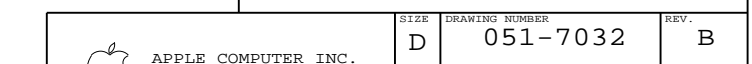
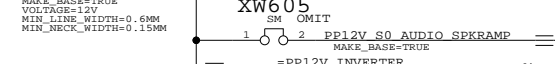
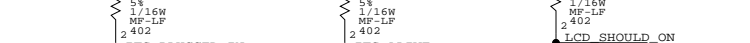
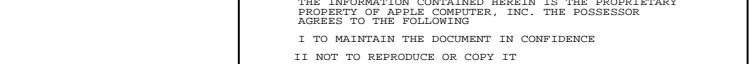
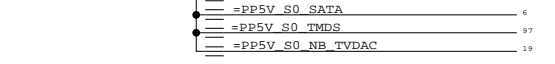
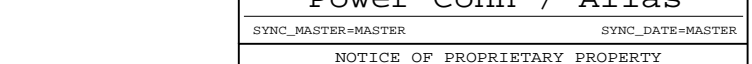
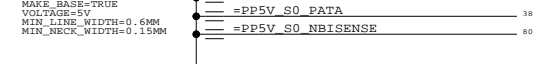
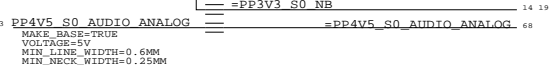
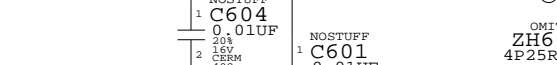
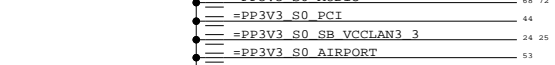
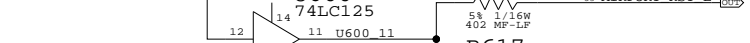
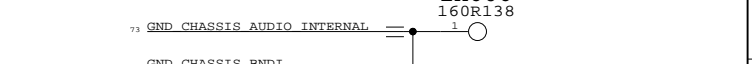
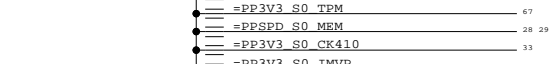
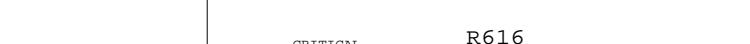
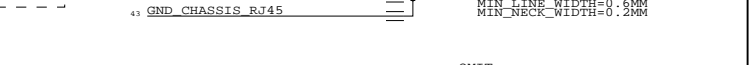
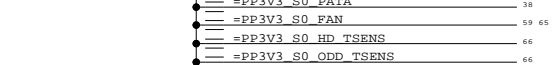
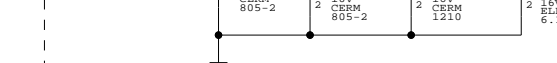
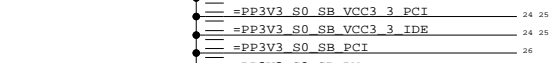
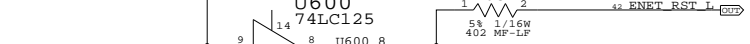
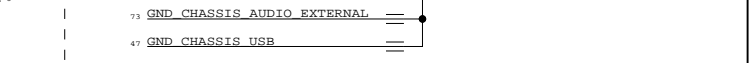
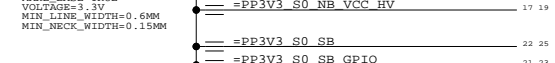
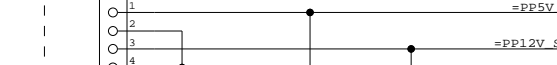
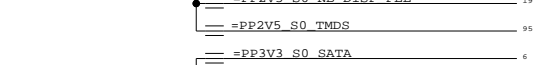
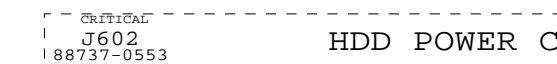
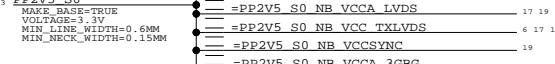
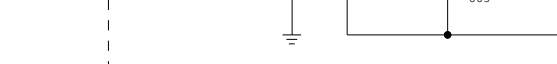
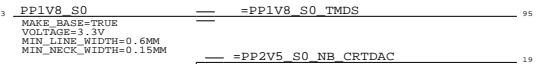
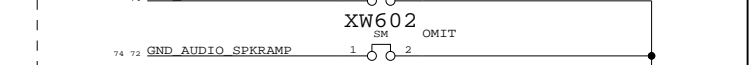
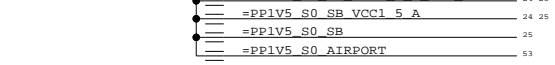
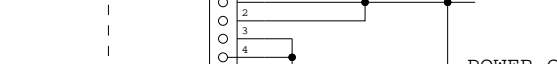
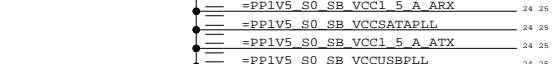
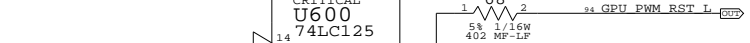
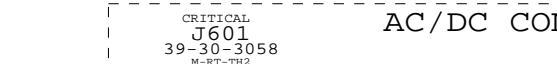
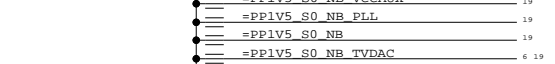
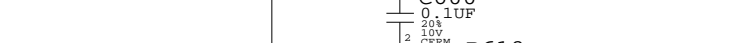
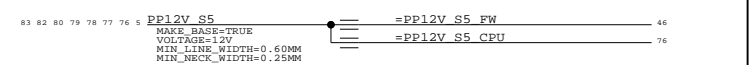
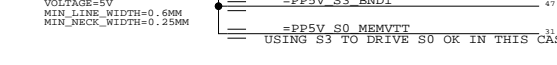
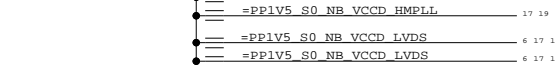
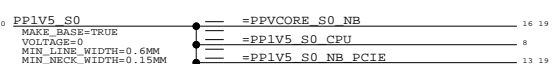
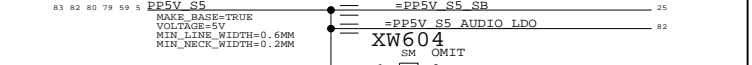
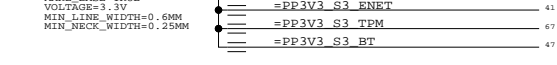
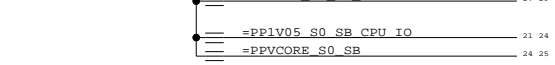
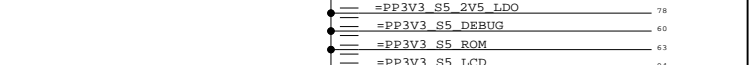
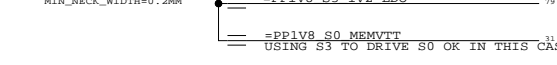
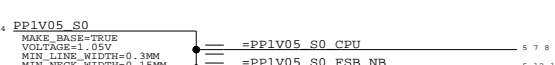
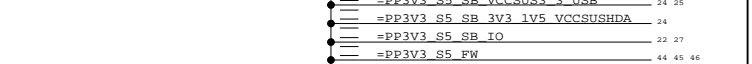
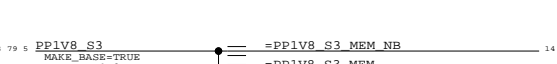
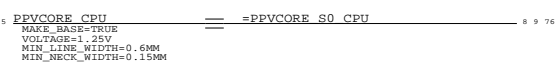
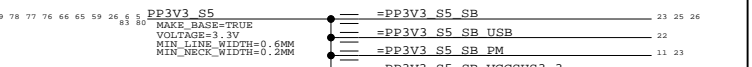
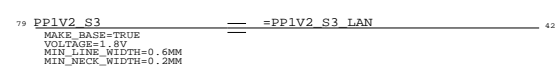
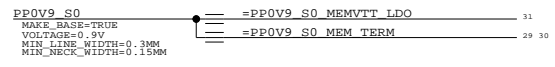
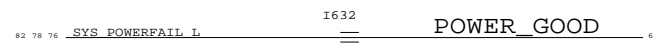
ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

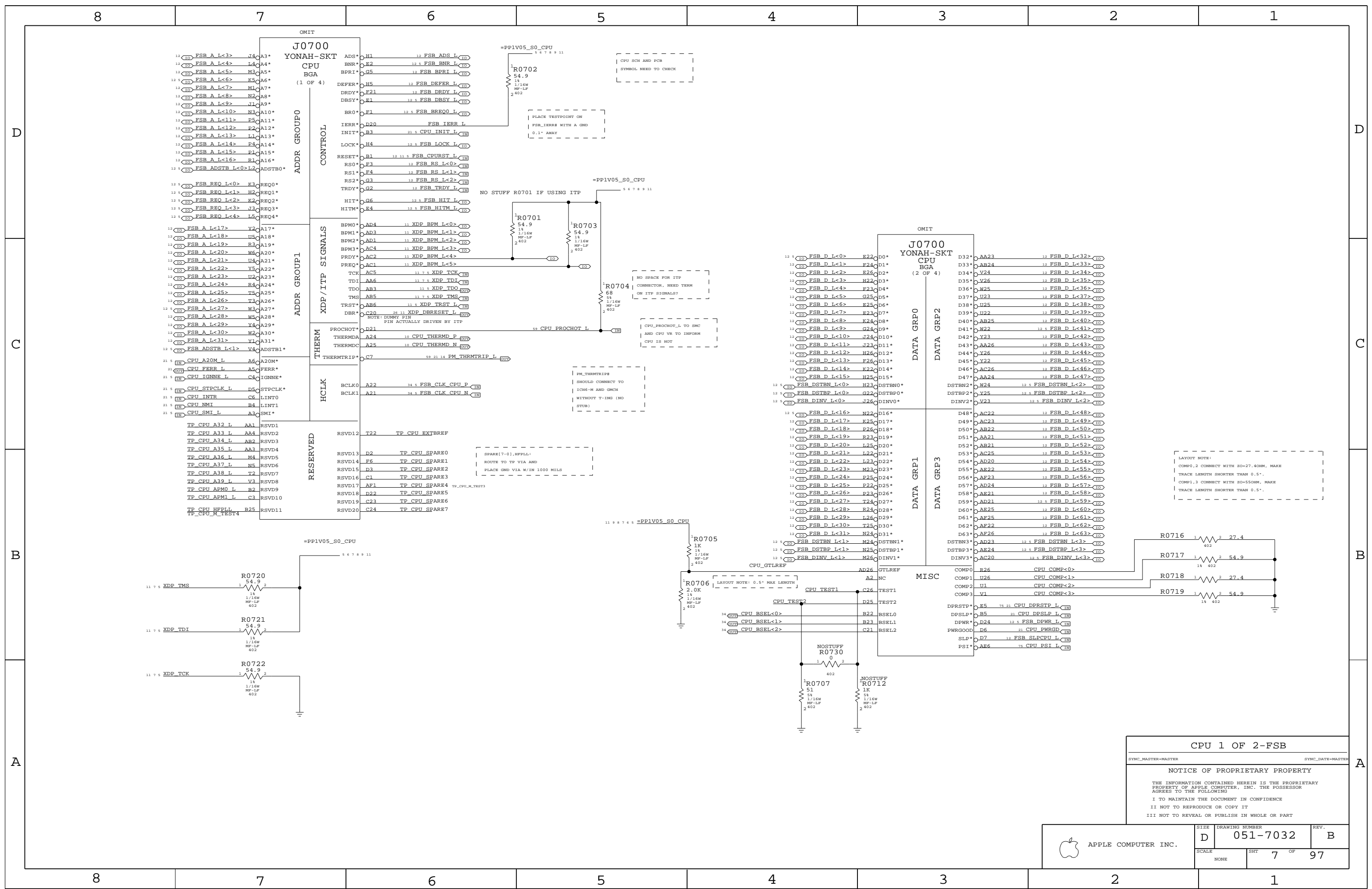
"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



Power Conn / Alias	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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	D	051-7032	B
SCALE	SHT	OF	97
NONE	6		



**CPU 1 OF 2-FSB**

SYNC\_MASTER-MASTER      SYNC\_DATE-MASTER

**NOTICE OF PROPRIETARY PROPERTY**

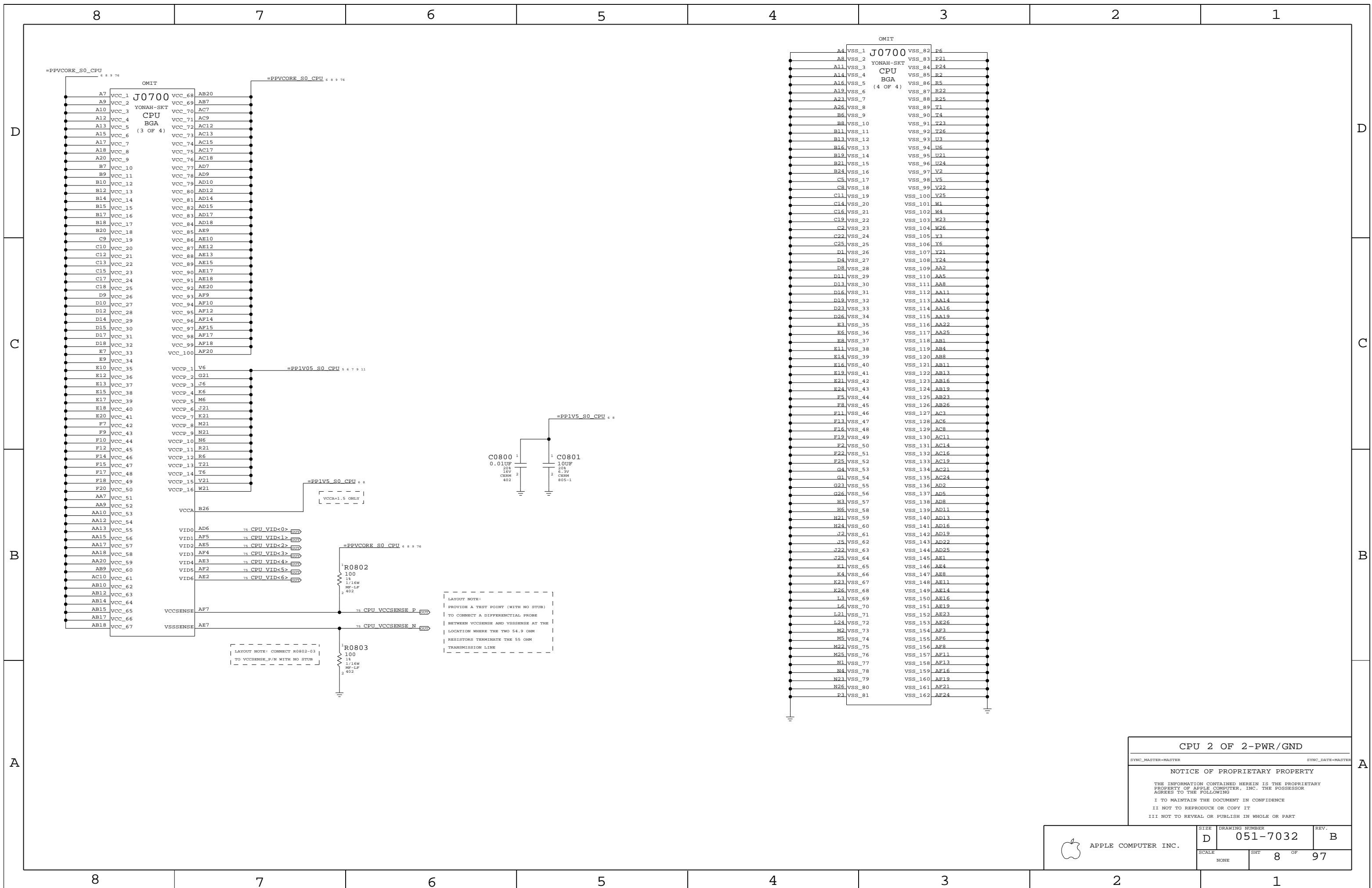
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	SCALE NONE	SHEET 7 OF 97	



**CPU 2 OF 2-PWR/GND**

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	SCALE NONE	SHEET 8 OF 97	



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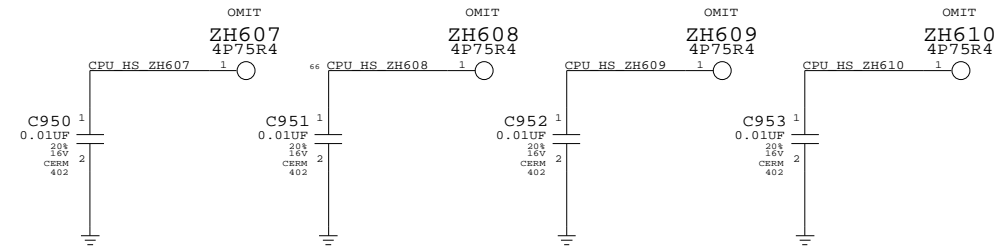
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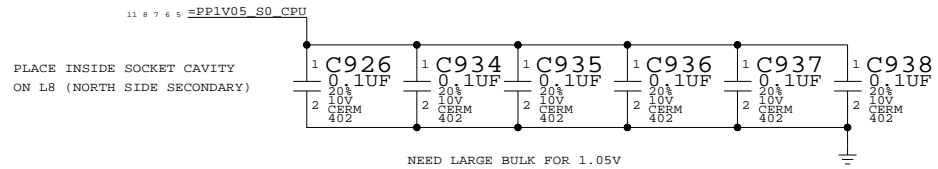
1

### CPU HEATSINK MOUNTING HOLES



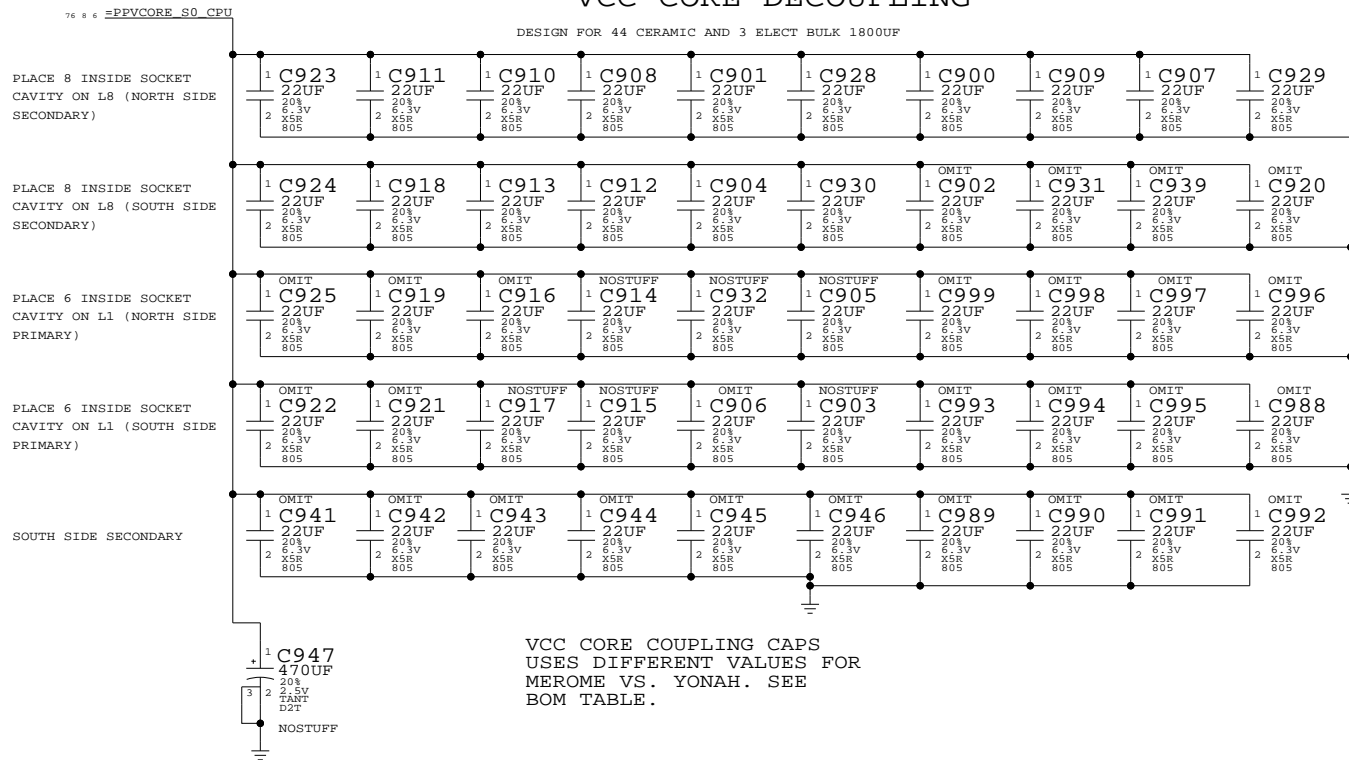
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

### VCCP CORE DECOUPLING



### VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

### CPU DECAPS & VID<>

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	9 OF	97
NONE			

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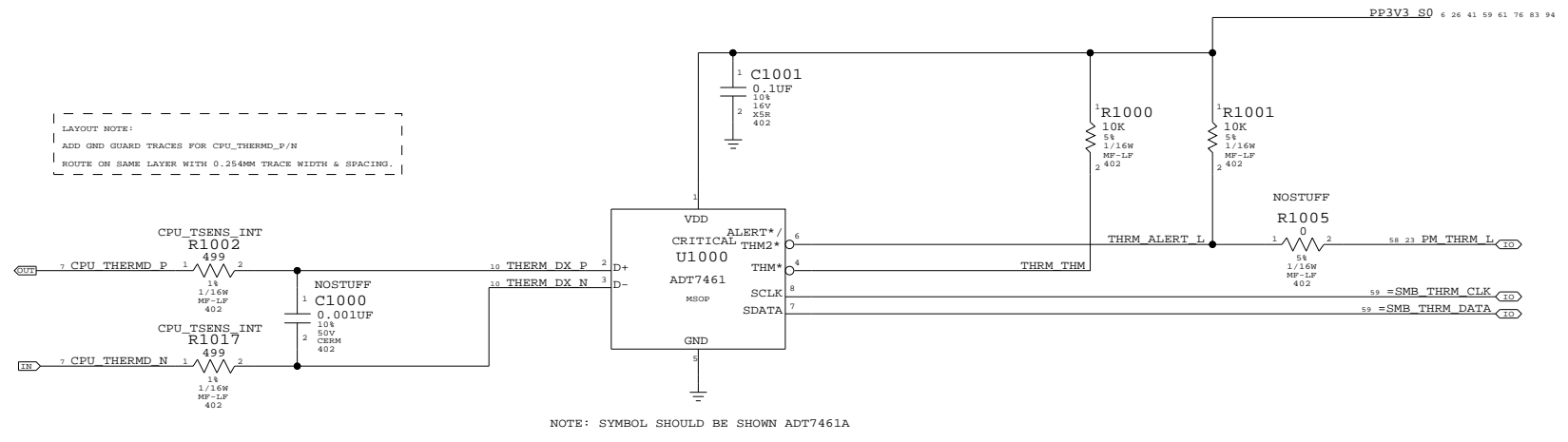
2

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### CPU THERMAL SENSOR

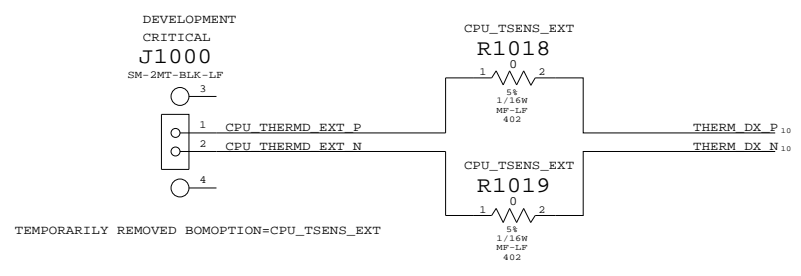
NOTE:  
 IF CPU T DIODE TO BE READ IN OFF STATE,  
 THEN THIS SHOULD BE S5

LAYOUT NOTE:  
 ADD GND GUARD TRACKS FOR CPU\_THERMD\_P/N  
 ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:  
 PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD  
 PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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	D	051-7032	B
SCALE	SHT	10 OF 97	
NONE			

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C

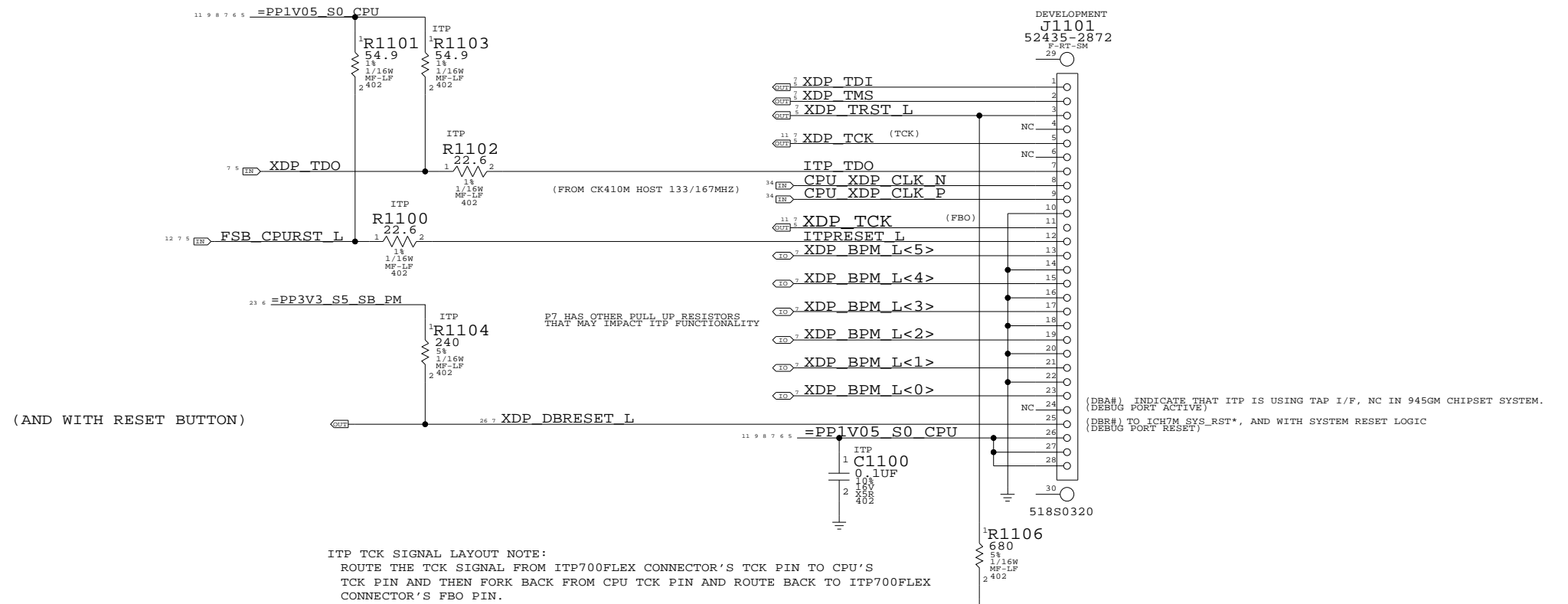
B

B

A

A

# CPU ITP700FLEX DEBUG SUPPORT



**CPU ITP700FLEX DEBUG**

SYNC\_MASTER=M38 SYNC\_DATE=01/05/2006

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	D	051-7032	B
SCALE	SHT	11 OF	97
NONE			

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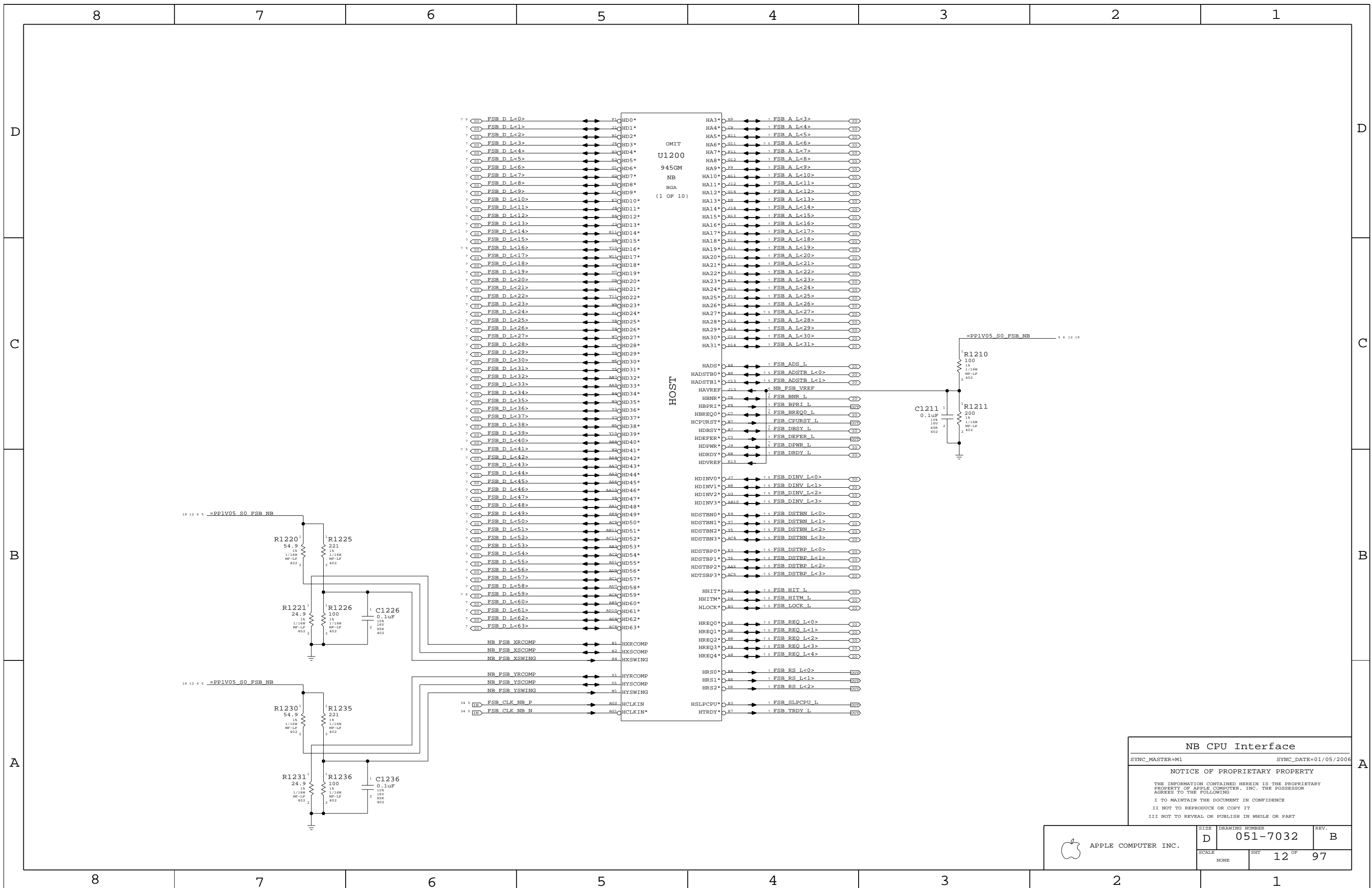
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**NB CPU Interface**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHEET 12 OF 97	

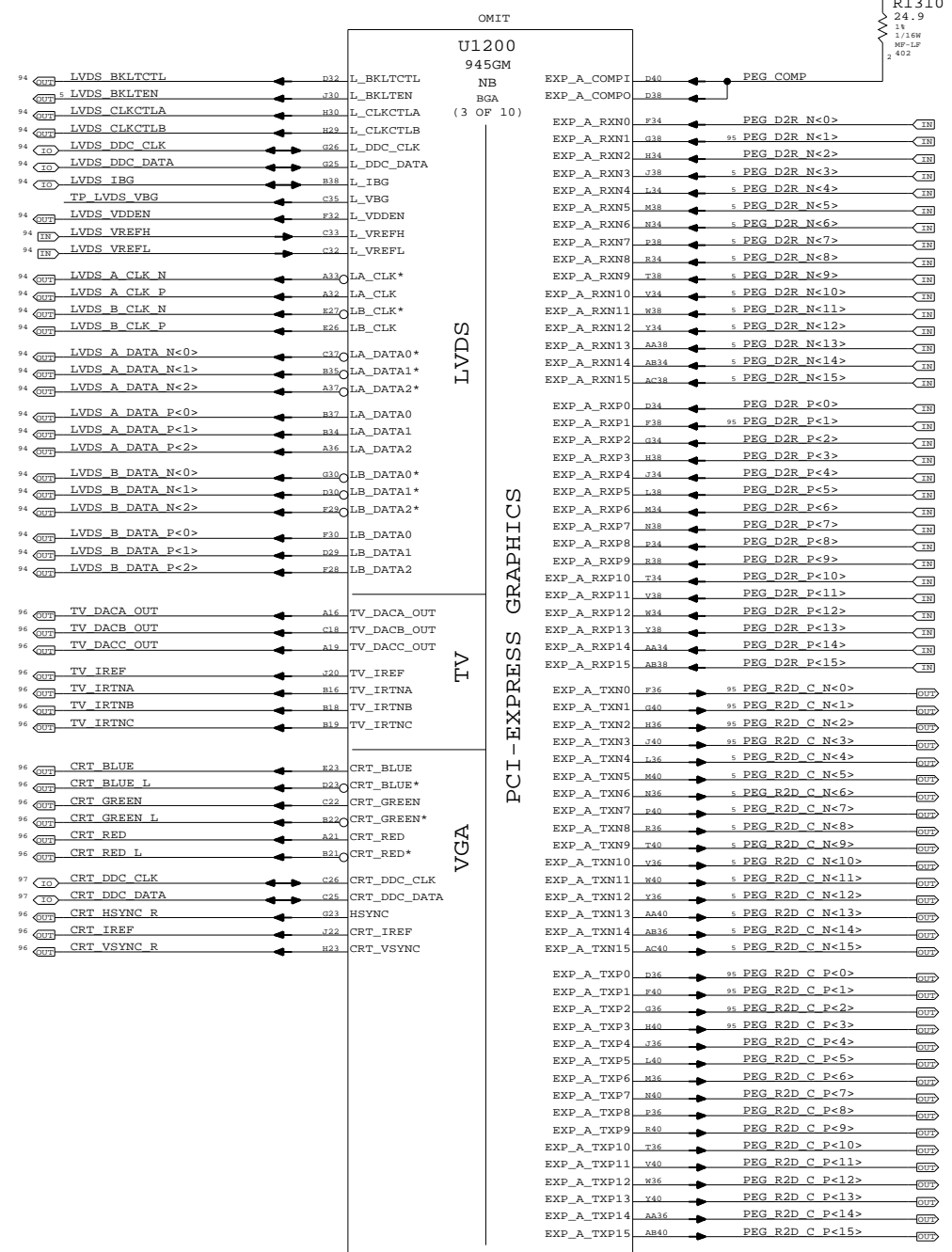
**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented  
 Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
 VCCD\_LVDS must remain powered with proper decoupling.  
 Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**  
 Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit  
 filtering components. Unused DAC outputs should  
 connect to GND through 75-ohm resistors.

**TV-Out Disable**  
 Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
 Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
 VCCA\_TVVBG to 1.5V power rail. Tie VSSA\_TVVBG to GND.

**CRT Disable**  
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
 HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
 rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.



SDVO Alternate Function

SDVO\_TVCLKIN#  
 SDVO\_INT#  
 SDVO\_FLDSTALL#

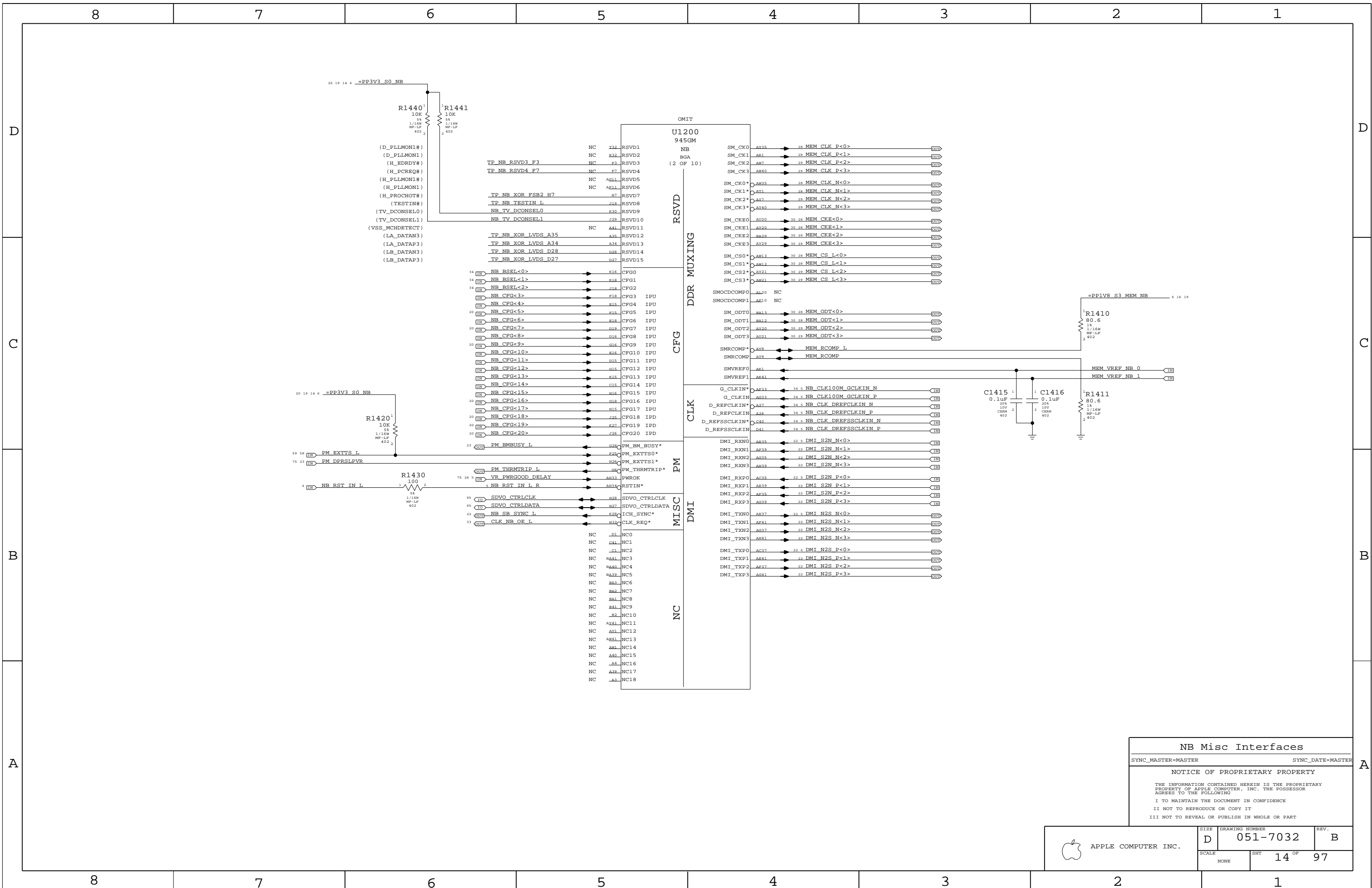
SDVO\_TVCLKIN  
 SDVO\_INT  
 SDVO\_FLDSTALL

SDVOB\_RED#  
 SDVOB\_GREEN#  
 SDVOB\_BLUE#  
 SDVOB\_CLKN  
 SDVOC\_RED#  
 SDVOC\_GREEN#  
 SDVOC\_BLUE#  
 SDVOC\_CLKN

SDVOB\_RED  
 SDVOB\_GREEN  
 SDVOB\_BLUE  
 SDVOB\_CLKP  
 SDVOC\_RED  
 SDVOC\_GREEN  
 SDVOC\_BLUE  
 SDVOC\_CLKP

**NB PEG / Video Interfaces**  
 SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006  
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	D	051-7032	B
SCALE	SHT	13 OF 97	
NONE			



**NB Misc Interfaces**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

**NOTICE OF PROPRIETARY PROPERTY**

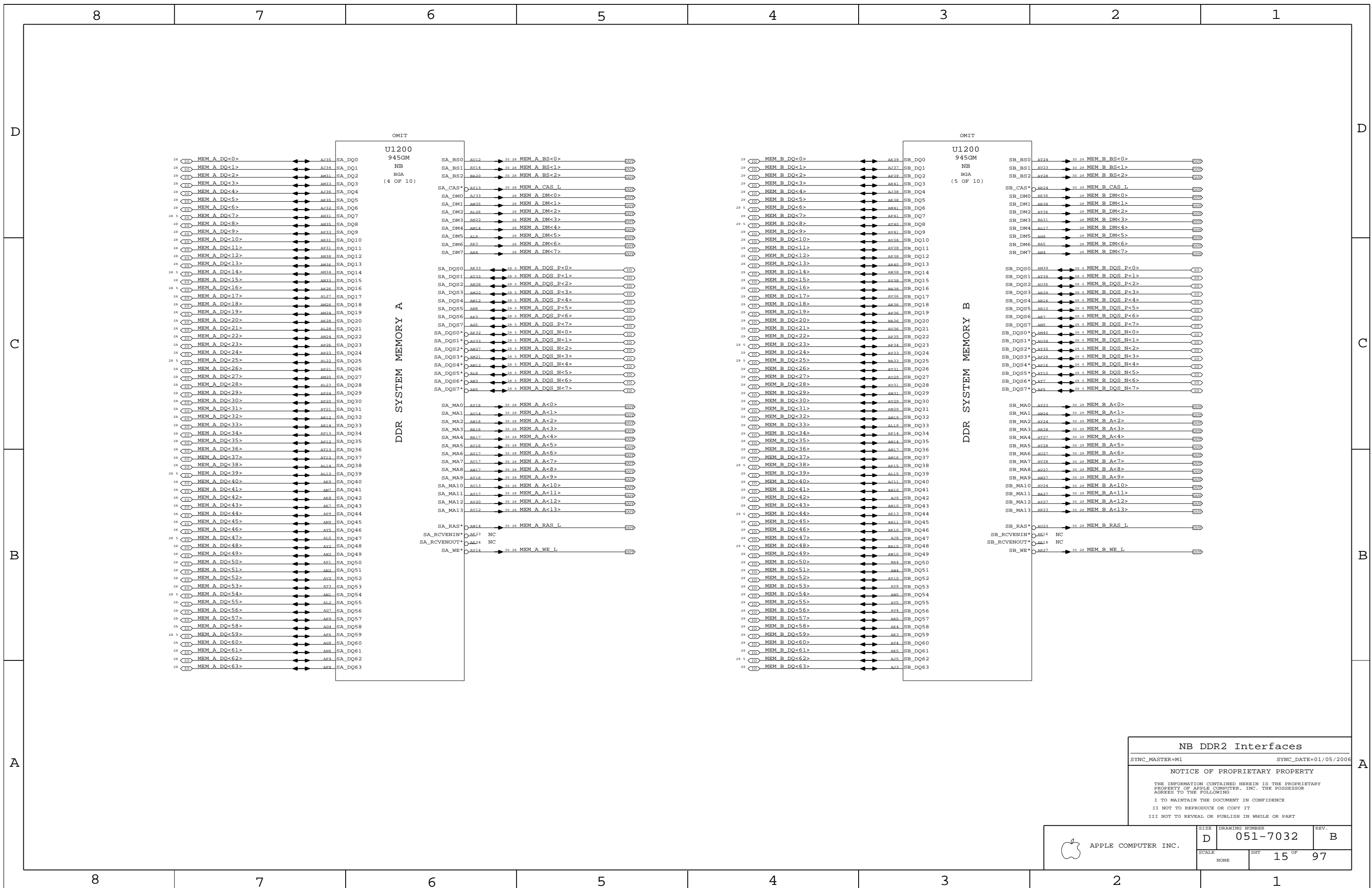
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	SCALE NONE	SHEET 14 OF 97	



**NB DDR2 Interfaces**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

**NOTICE OF PROPRIETARY PROPERTY**

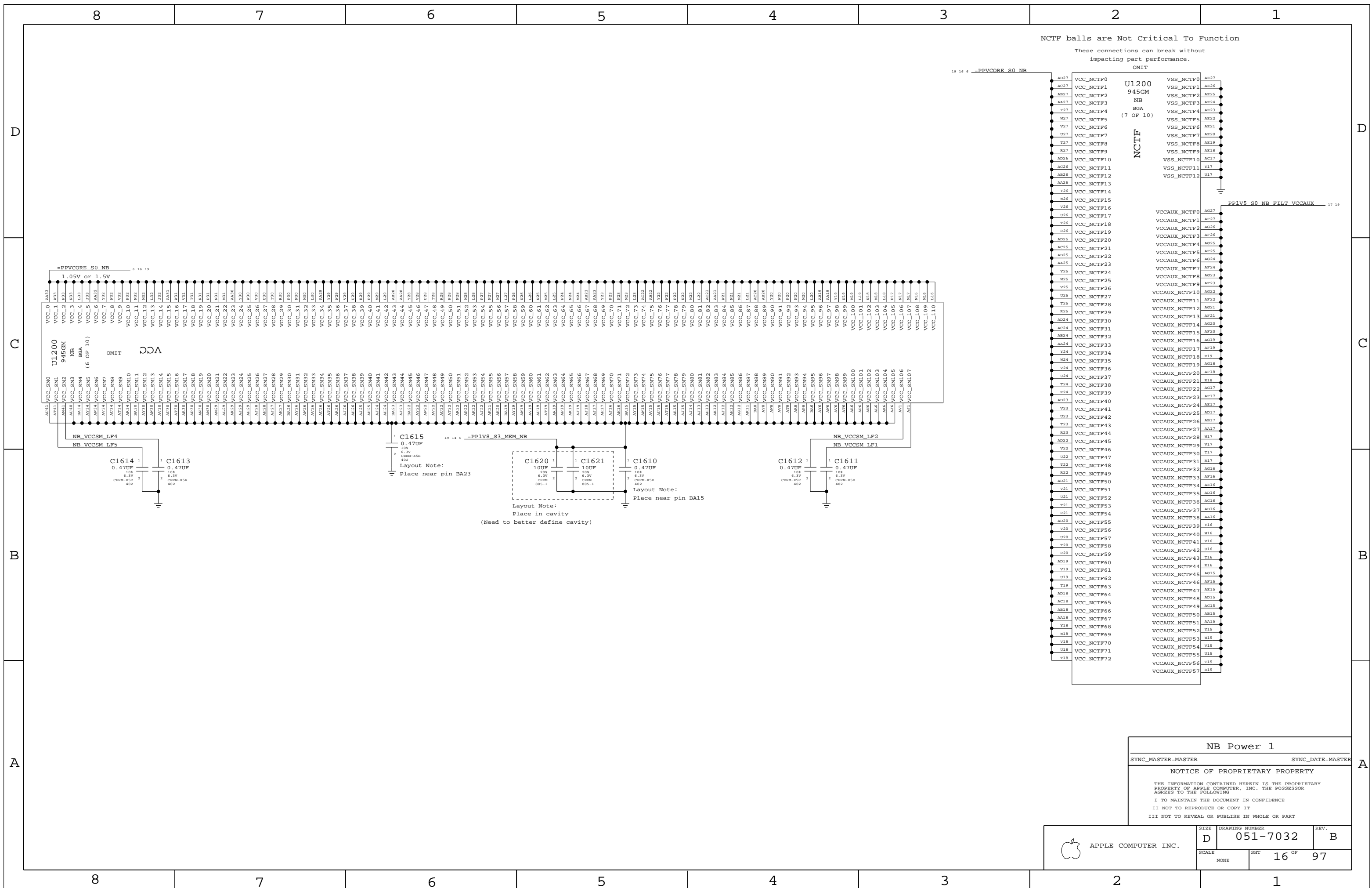
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	SCALE NONE	SHEET 15 OF 97	



**NB Power 1**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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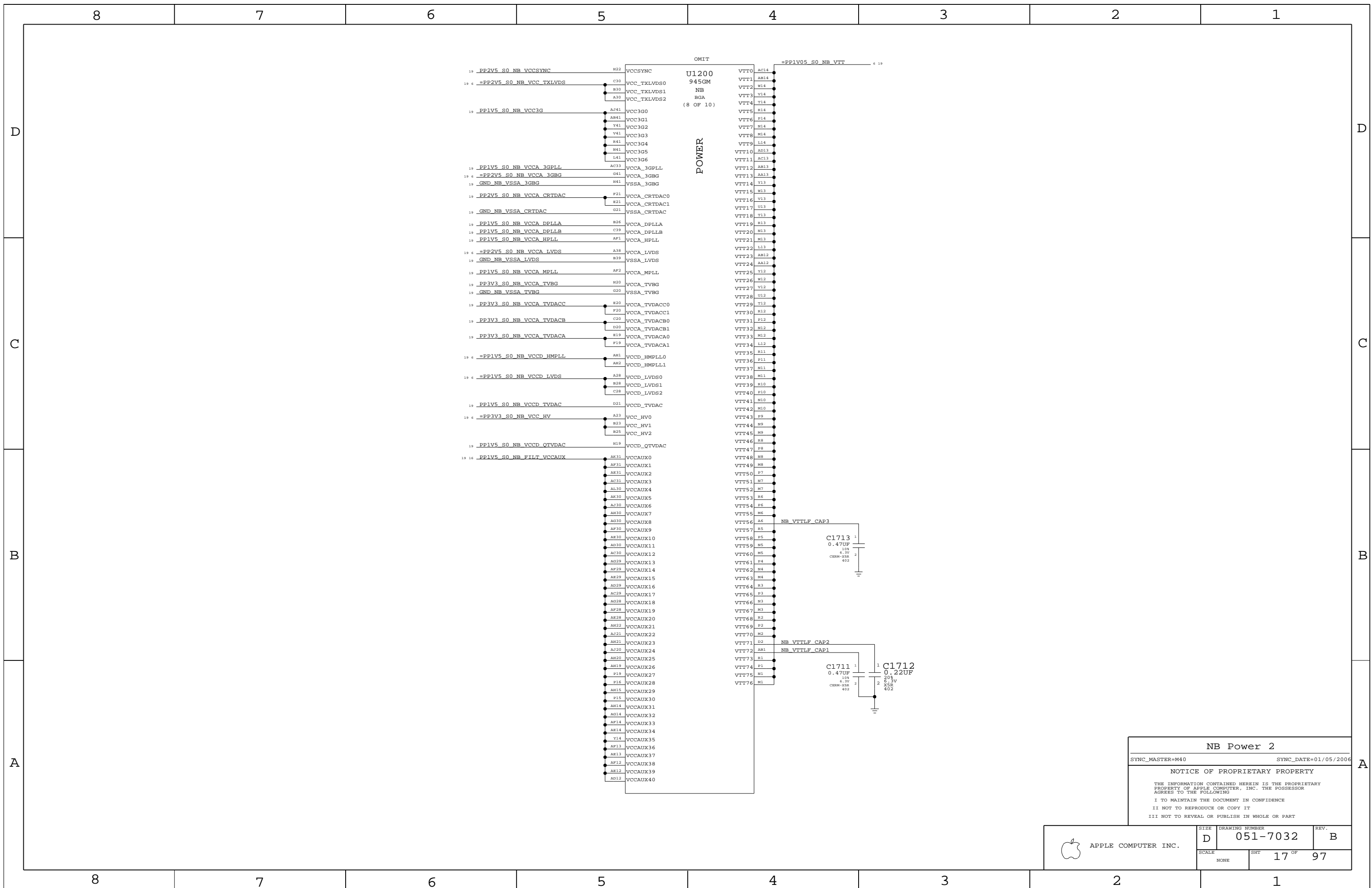
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHT 16 OF 97	

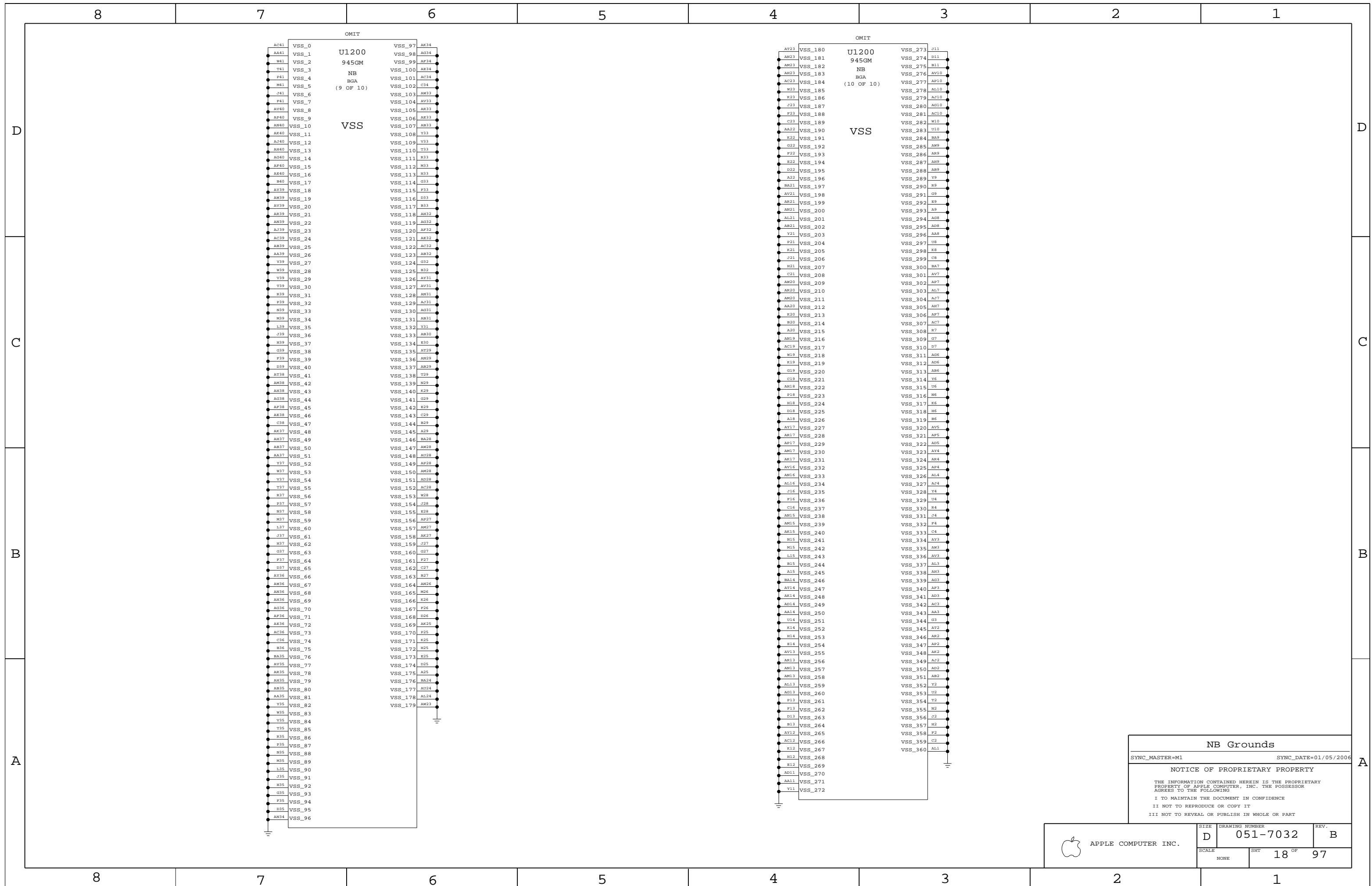




NB Power 2  
SYNC\_MASTER=M40 SYNC\_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	17 OF 97	
NONE			



**NB Grounds**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

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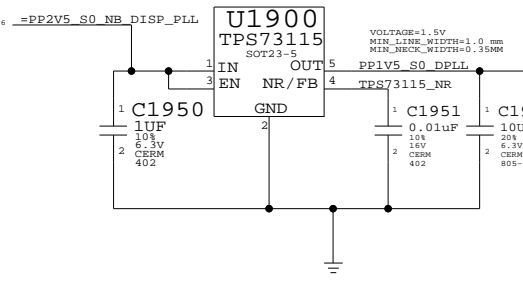
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHEET 18 OF 97	

### Power Interface

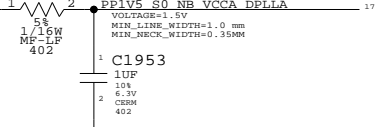
These are the power signals that leave the NB "block"

- PP1V05\_S0\_FSB\_NB
- PPVCORE\_S0\_NB
- PP1V05\_S0\_NB\_VTT
- PP1V5\_S0\_NB
- PP1V5\_S0\_NB\_PCIE
- PP1V5\_S0\_NB\_PLL
- PP1V5\_S0\_NB\_TVDAC
- PP1V5\_S0\_NB\_VCCD\_HMPLL
- PP1V5\_S0\_NB\_VCCD\_LVDS
- PP1V5\_S0\_NB\_VCCAUX
- PP1V8\_S3\_MEM\_NB
- PP2V5\_S0\_NB\_VCCSYNC
- PP2V5\_S0\_NB\_VCC\_TXLVDS
- PP2V5\_S0\_NB\_VCCA\_3GBG
- PP2V5\_S0\_NB\_VCCA\_LVDS
- PP3V3\_S0\_NB
- PP3V3\_S0\_NB\_VCC\_HV
- PP5V\_S0\_NB\_TVDAC

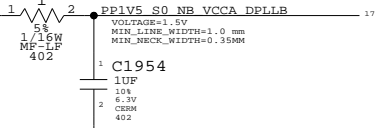
### MCH DISPLAY PLL POWER LDO



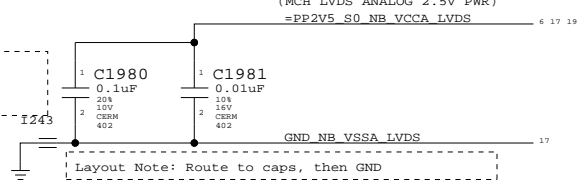
### MCH VCCA\_DPLL\_A FILTER



### GMCH VCCA\_DPLL\_B FILTER



### MCH VCCA\_LVDS FILTER



Layout Note:  
This 0.1uF cap should be within 5 mm of NB edge

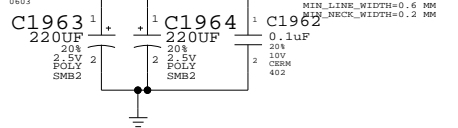
Layout Note: Route to caps, then GND

### GMCH VCCD\_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)

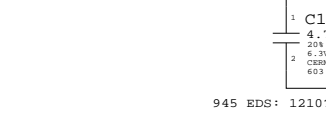


FILTERING REQUIRED FOR INTEGRATED GFX (PG. 333)



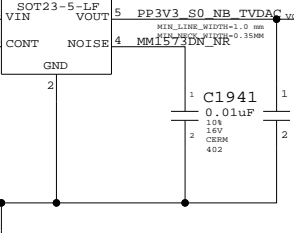
### GMCH VCCD\_LVDS BYPASS

(MCH LVDS DIGITAL TX 2.5V PWR)

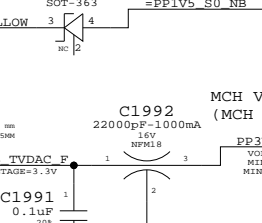


945 EDS: 1210?

### U1901 MM157

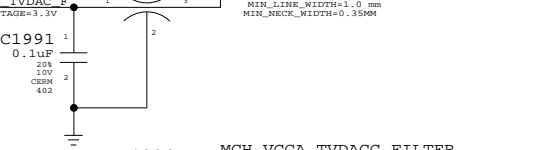


### D1986 BAT54DW



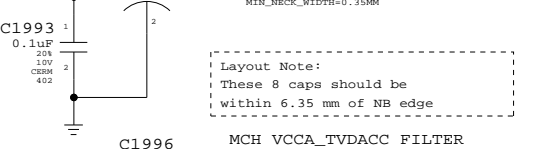
### MCH VCCA\_TVDACC FILTER

(MCH TV OUT CHANNEL A 3.3V PWR)



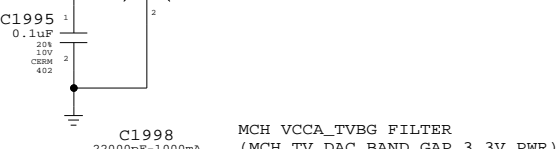
### MCH VCCA\_TVDACC FILTER

(MCH TV OUT CHANNEL B 3.3V PWR)



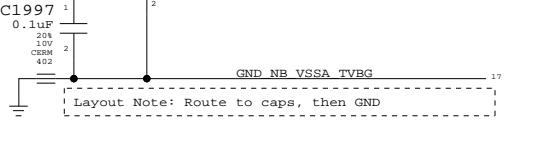
### MCH VCCA\_TVDACC FILTER

(MCH TV OUT CHANNEL C 3.3V PWR)

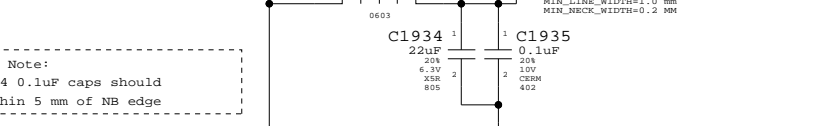


### MCH VCCA\_TVBG FILTER

(MCH TV DAC BAND GAP 3.3V PWR)

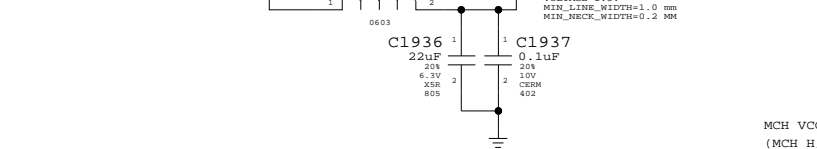


### PP1V5\_S0\_NB\_VTT

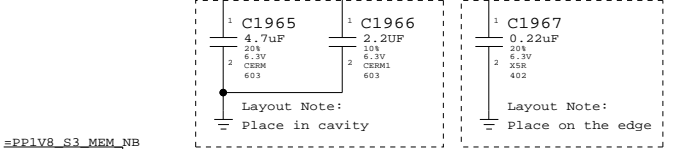


Layout Note:  
These 4 0.1uF caps should be within 5 mm of NB edge

### PP1V5\_S0\_NB\_VCCA\_HPLL



### PP1V05\_S0\_NB\_VTT



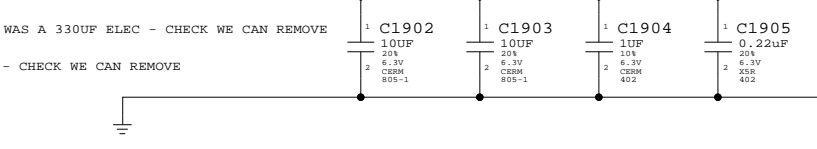
Layout Note:  
Place in cavity

Layout Note:  
Place on the edge

### PP1V8\_S3\_MEM\_NB



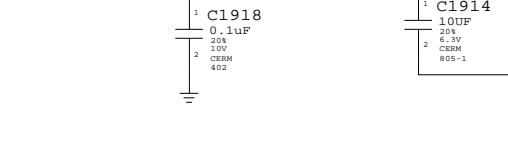
### PPVCORE\_S0\_NB



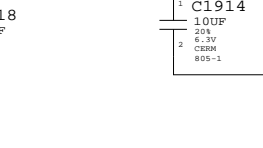
### PP2V5\_S0\_NB\_VCCA\_3GBG



### PP1V5\_S0\_NB\_VCCAUX



### PP3V3\_S0\_NB\_VCC\_HV

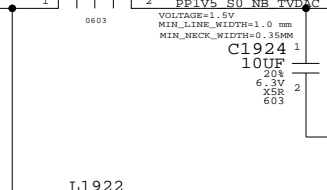


### MCH VCCSYNC BYPASS

(MCH H/V SYNC 2.5V PWR)

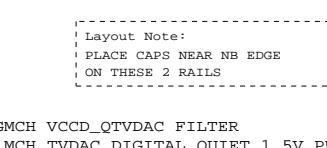


### PP1V5\_S0\_NB\_TVDAC



### GMCH VCCD\_TVDAC FILTER

(MCH TVDAC DEDICATED PWR 1.5V)



Layout Note:  
PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

### PP1V5\_S0\_NB\_QTVDAC



### GMCH VCCD\_QTVDAC FILTER

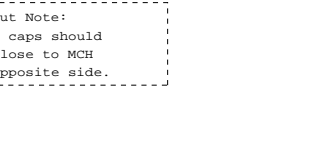
(MCH TVDAC DIGITAL QUIET 1.5V PWR)



### PP1V5\_S0\_NB\_VCC3G

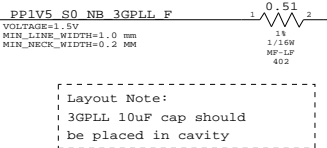


### PP1V5\_S0\_NB\_VCCA\_3GBG

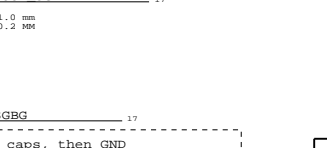


Layout Note:  
10uF caps should be close to MCH on opposite side.

### PP1V5\_S0\_NB\_VCCAUX



### PP1V5\_S0\_NB\_VCCA\_3GBG



Layout Note:  
3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

### NB (GM) Decoupling

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

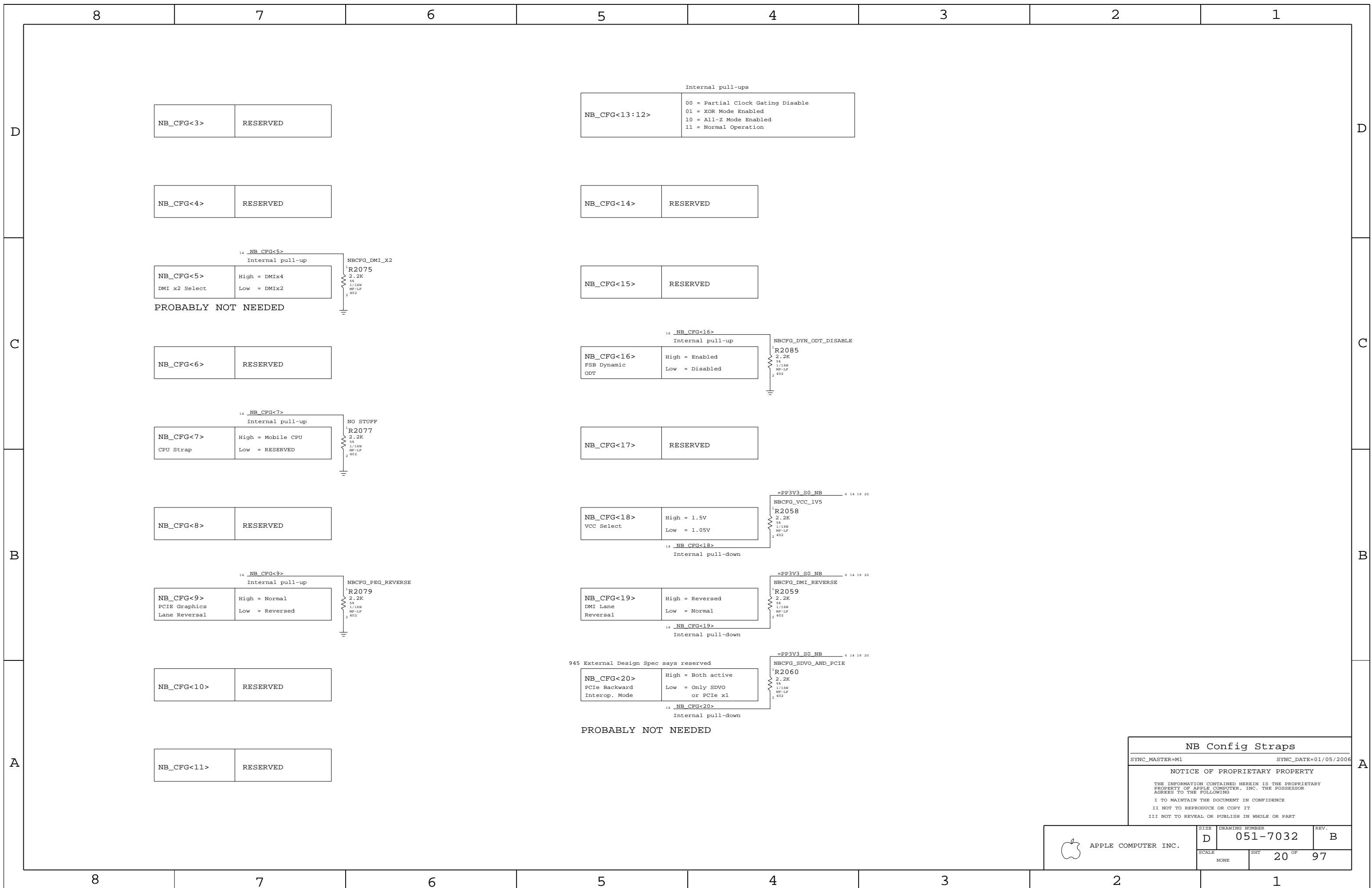
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SCALE	DRAWING NUMBER	REV.
NONE	SHT 19 OF 97	



APPLE COMPUTER INC.



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<4>	RESERVED
-----------	----------

14 NB\_CFG<5>  
Internal pull-up

NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
-----------	--

PROBABLY NOT NEEDED

NBCFG\_DMI\_X2  
R2075  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB\_CFG<16>  
Internal pull-up

NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
------------	--

NBCFG\_DYN\_ODT\_DISABLE  
R2085  
2.2K  
5%  
1/16W  
MF-LP  
402

14 NB\_CFG<7>  
Internal pull-up

NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED
-----------	--

NO STUFF  
R2077  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14 NB\_CFG<18>  
Internal pull-down

NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V
------------	--

=PP3V3\_S0\_NB 6 14 19 20  
NBCFG\_VCC\_LV5  
R2058  
2.2K  
5%  
1/16W  
MF-LP  
402

14 NB\_CFG<9>  
Internal pull-up

NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
-----------	---

NBCFG\_PEG\_REVERSE  
R2079  
2.2K  
5%  
1/16W  
MF-LP  
402

14 NB\_CFG<19>  
Internal pull-down

NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
------------	---

=PP3V3\_S0\_NB 6 14 19 20  
NBCFG\_DMI\_REVERSE  
R2059  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved

14 NB\_CFG<20>  
Internal pull-down

NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
------------	---

=PP3V3\_S0\_NB 6 14 19 20  
NBCFG\_SDVO\_AND\_PCIE  
R2060  
2.2K  
5%  
1/16W  
MF-LP  
402

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

**NB Config Straps**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

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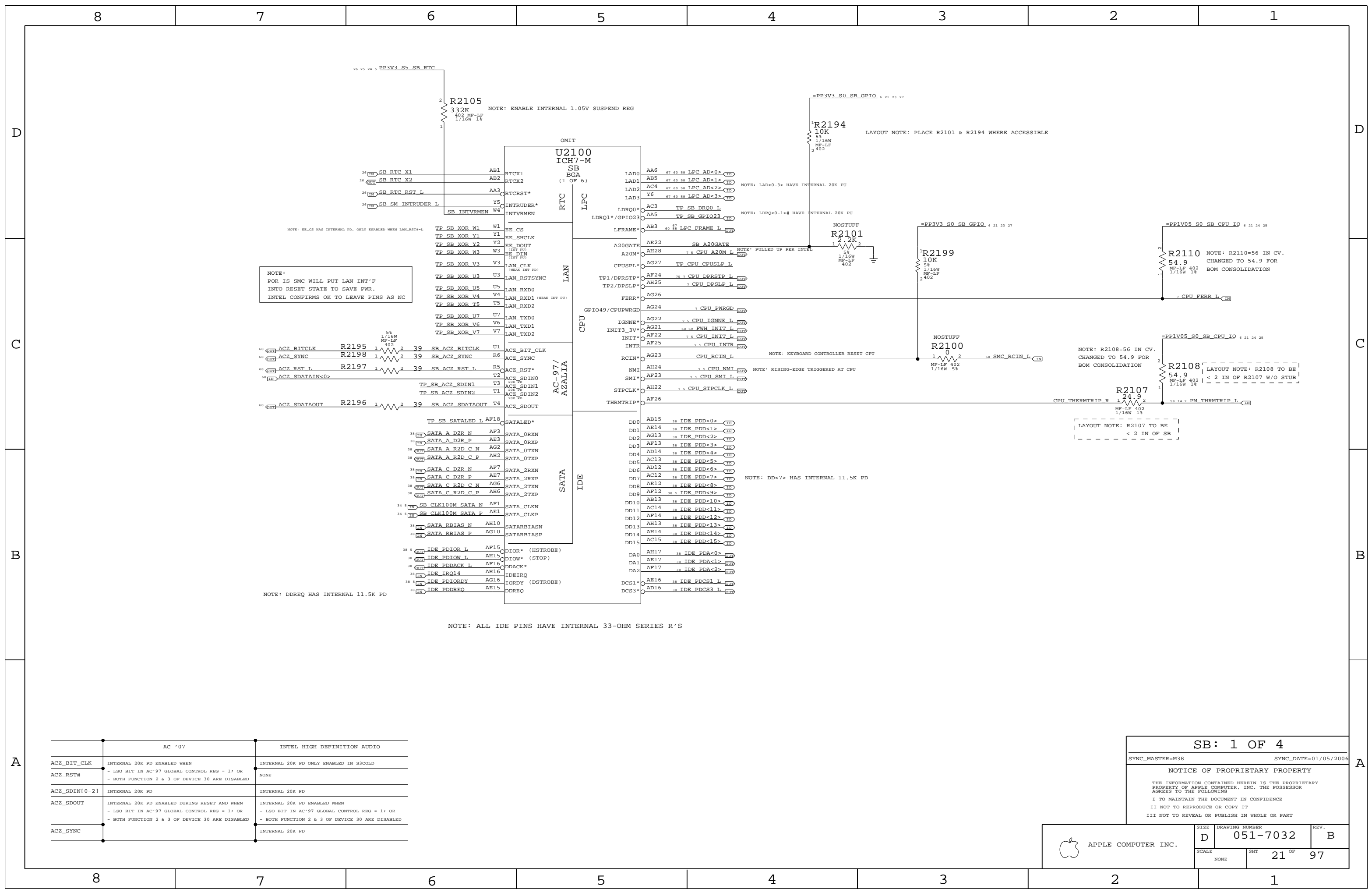
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	D	051-7032	B
SCALE	SHT	20 OF 97	
NONE			



NOTE:  
 POR IS SMC WILL PUT LAN INT'F  
 INTO RESET STATE TO SAVE PWR.  
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

**SB: 1 OF 4**

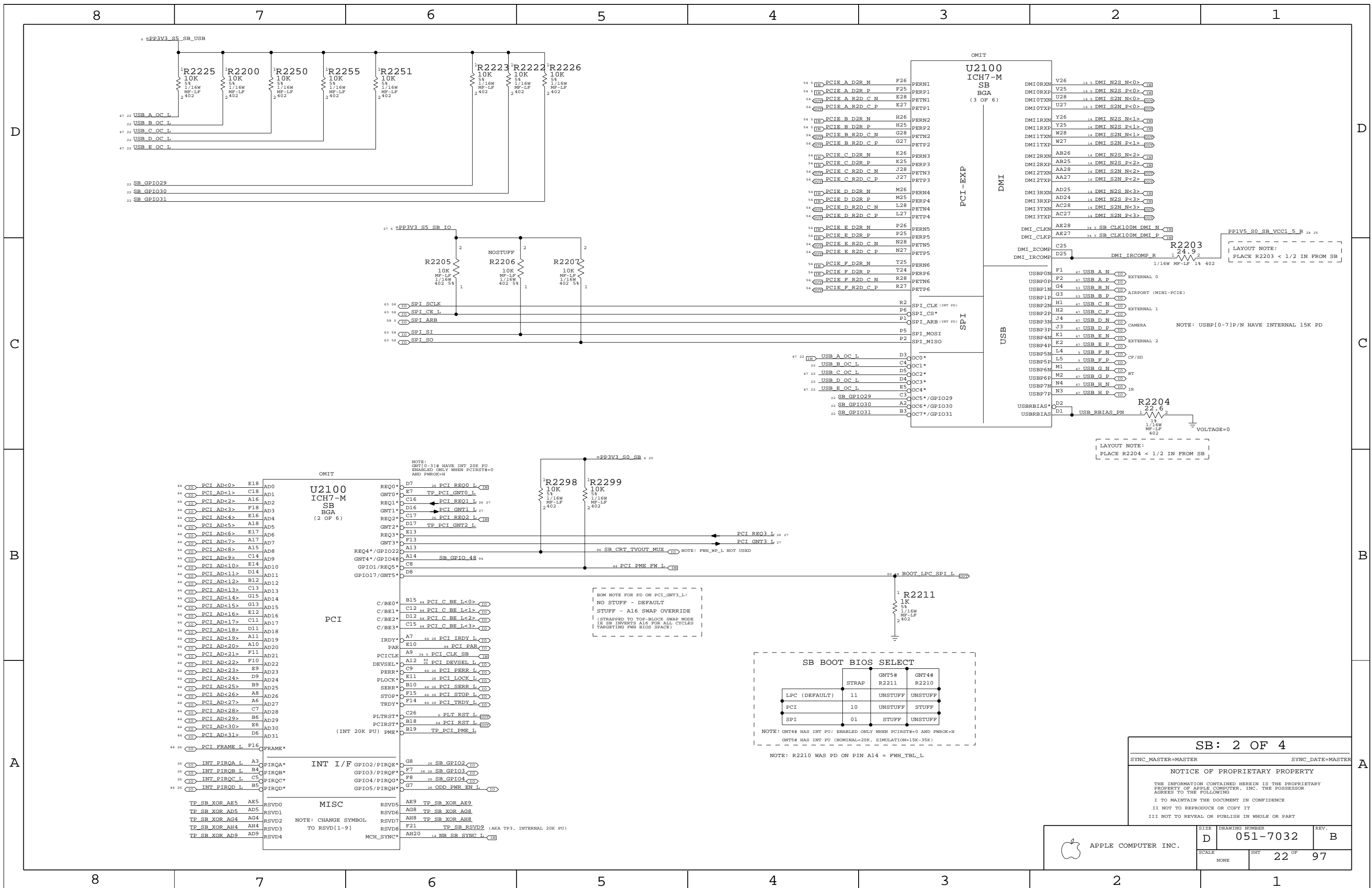
SYNC\_MASTER=M38 SYNC\_DATE=01/05/2006

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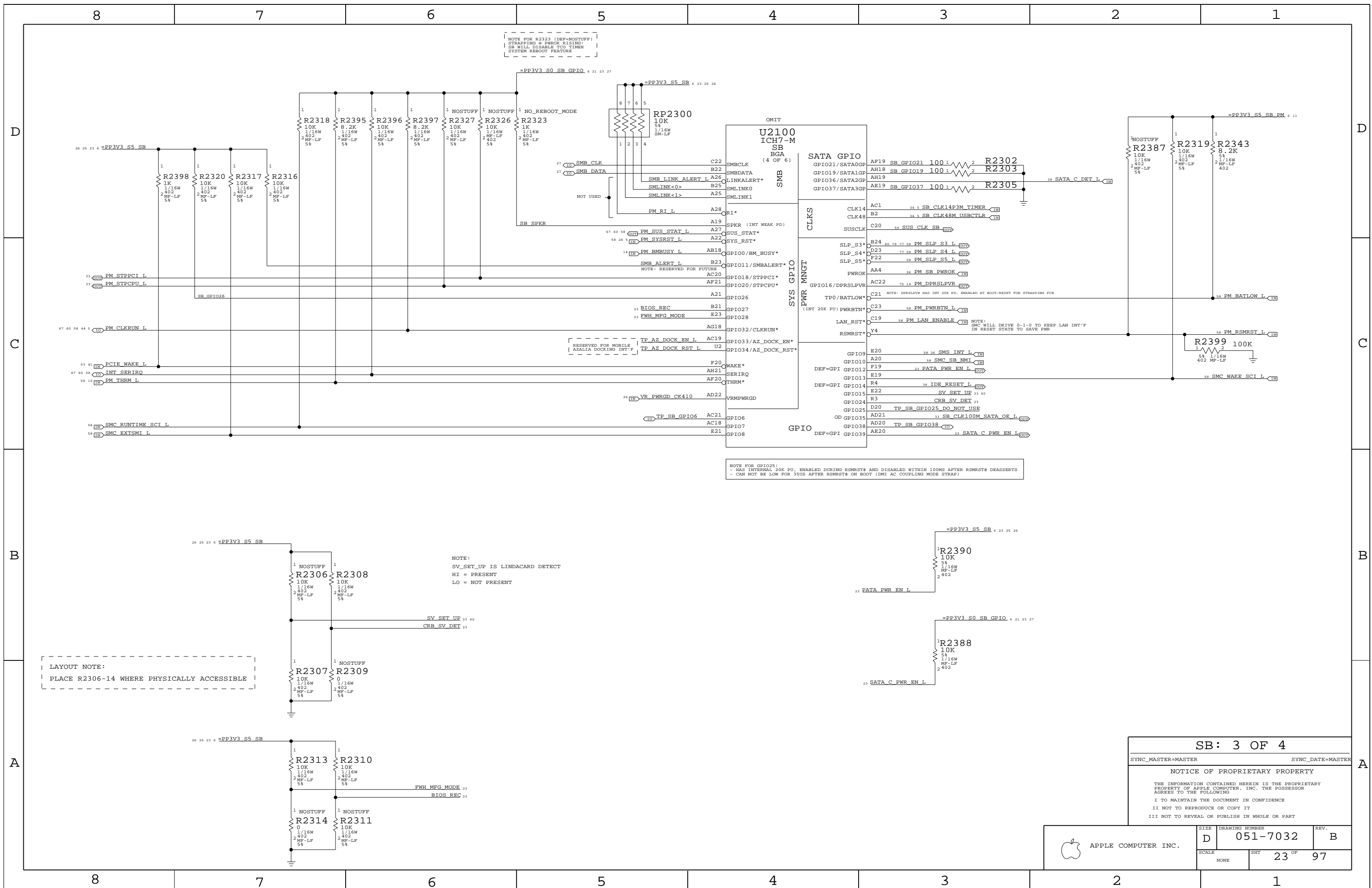
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	21 OF 97	
NONE			



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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHEET <b>22</b> OF <b>97</b>	



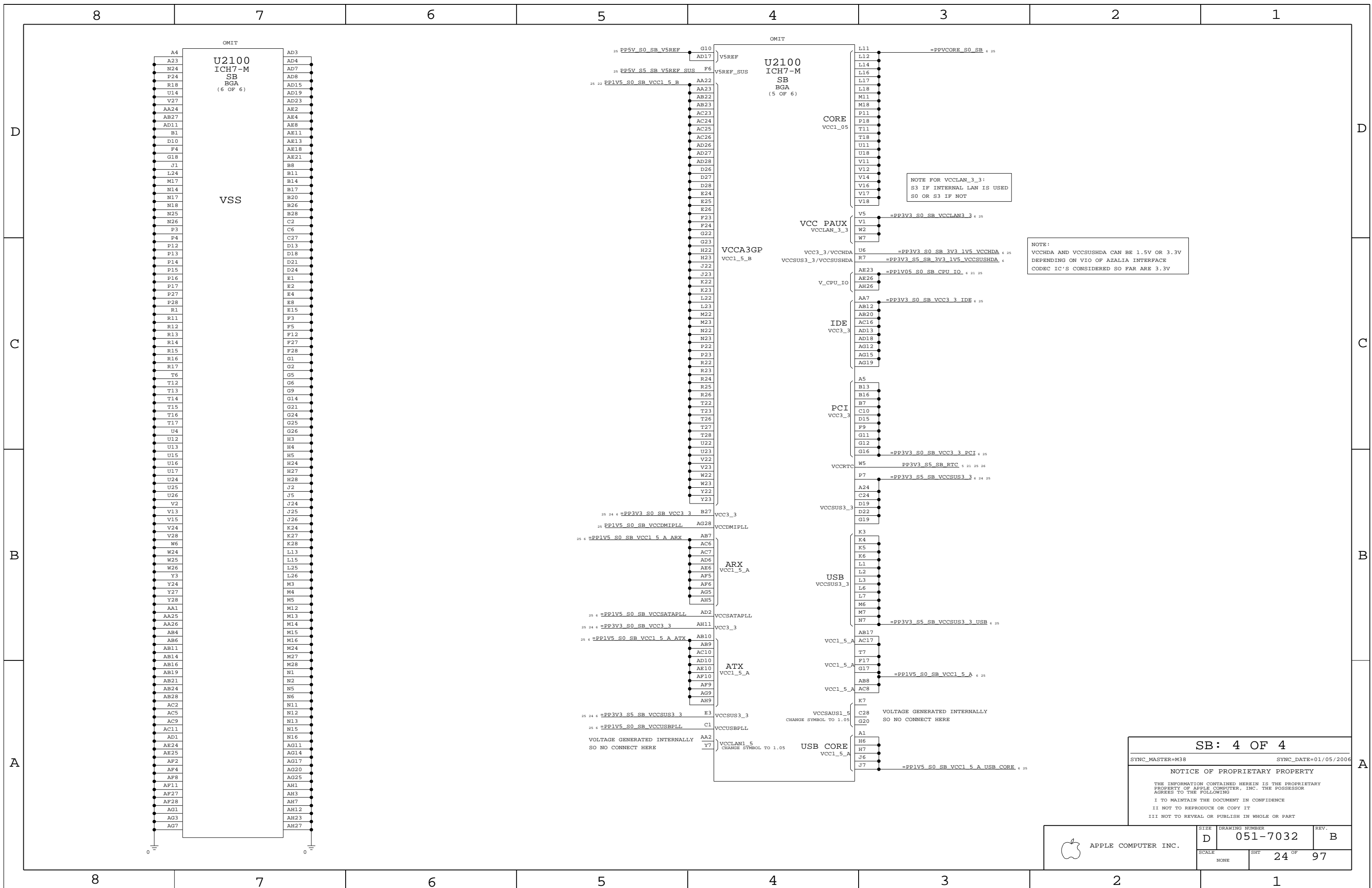
NOTE FOR R2323 (DEF-NOSTUFF)  
STRAPPING & PWROK RISING:  
SB WILL DISABLE TOO TIMER  
SYSTEM REBOOT FEATURE

NOTE FOR GPIO25:  
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS  
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:  
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:  
SV\_SET\_UP IS LINDACARD DETECT  
HI = PRESENT  
LO = NOT PRESENT

SB: 3 OF 4  
SYNC\_MASTER=MASTER SYNC\_DATE=MASTER  
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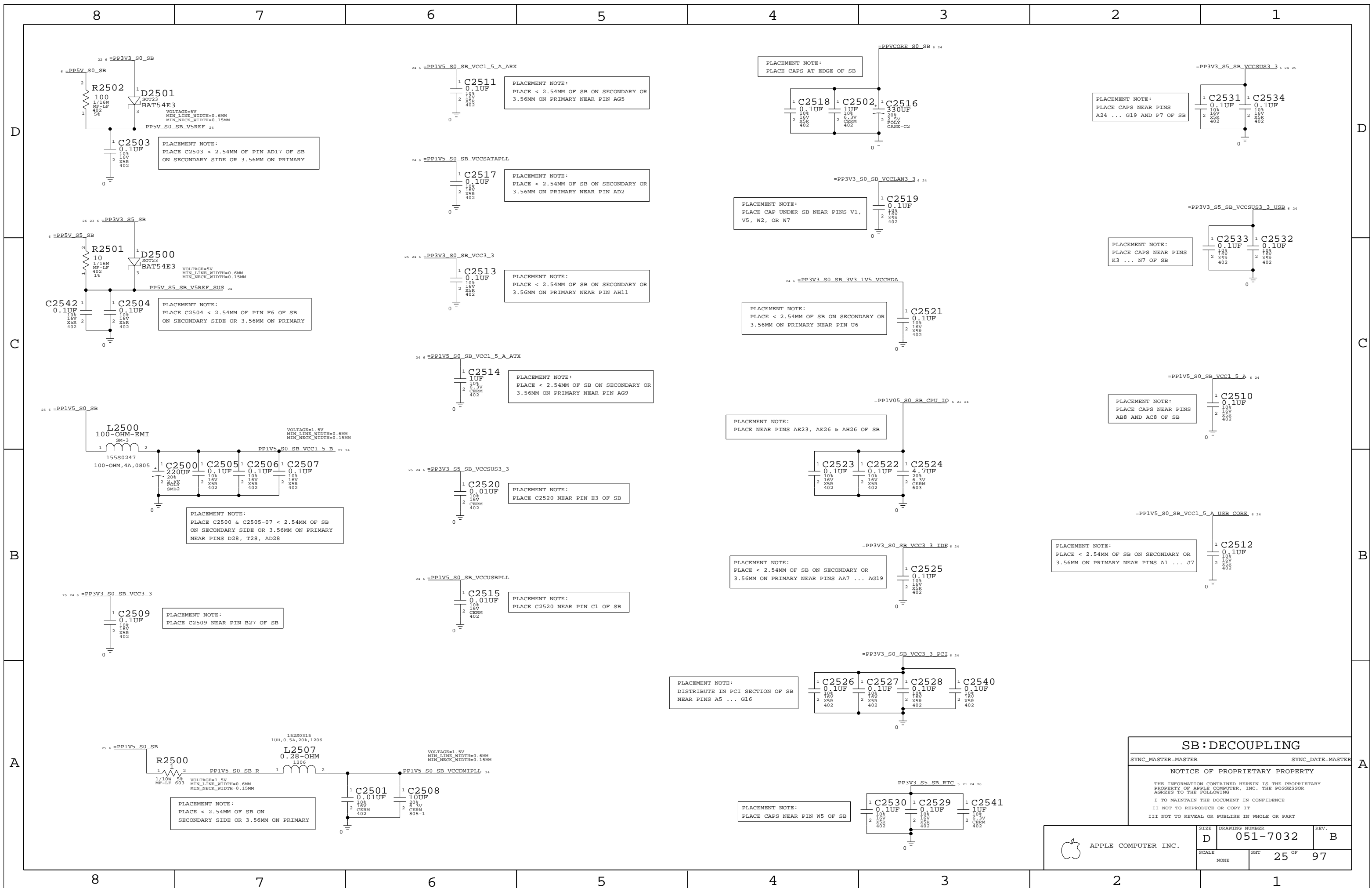
NOTE FOR VCCLAN\_3\_3:  
S3 IF INTERNAL LAN IS USED  
S0 OR S3 IF NOT

NOTE:  
VCCCHDA AND VCCSUS3\_3 CAN BE 1.5V OR 3.3V  
DEPENDING ON VIO OF AZALIA INTERFACE  
CODIC IC'S CONSIDERED SO FAR ARE 3.3V

<b>SB: 4 OF 4</b>	
SYNC_MASTER=M38	SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	24 OF 97	
NONE			





PLACEMENT NOTE:  
 PLACE C2503 < 2.54MM OF PIN AD17 OF SB  
 ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:  
 PLACE C2504 < 2.54MM OF PIN F6 OF SB  
 ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:  
 PLACE C2500 & C2505-07 < 2.54MM OF SB  
 ON SECONDARY SIDE OR 3.56MM ON PRIMARY  
 NEAR PINS D28, T28, AD28

PLACEMENT NOTE:  
 PLACE C2509 NEAR PIN B27 OF SB

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON  
 SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PIN AG5

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PIN AD2

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PIN AH11

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PIN AG9

PLACEMENT NOTE:  
 PLACE C2520 NEAR PIN E3 OF SB

PLACEMENT NOTE:  
 PLACE C2520 NEAR PIN C1 OF SB

PLACEMENT NOTE:  
 PLACE CAPS AT EDGE OF SB

PLACEMENT NOTE:  
 PLACE CAP UNDER SB NEAR PINS V1,  
 V5, W2, OR W7

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PIN U6

PLACEMENT NOTE:  
 PLACE NEAR PINS AE23, AE26 & AH26 OF SB

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PINS AA7 ... AG19

PLACEMENT NOTE:  
 DISTRIBUTE IN PCI SECTION OF SB  
 NEAR PINS A5 ... G16

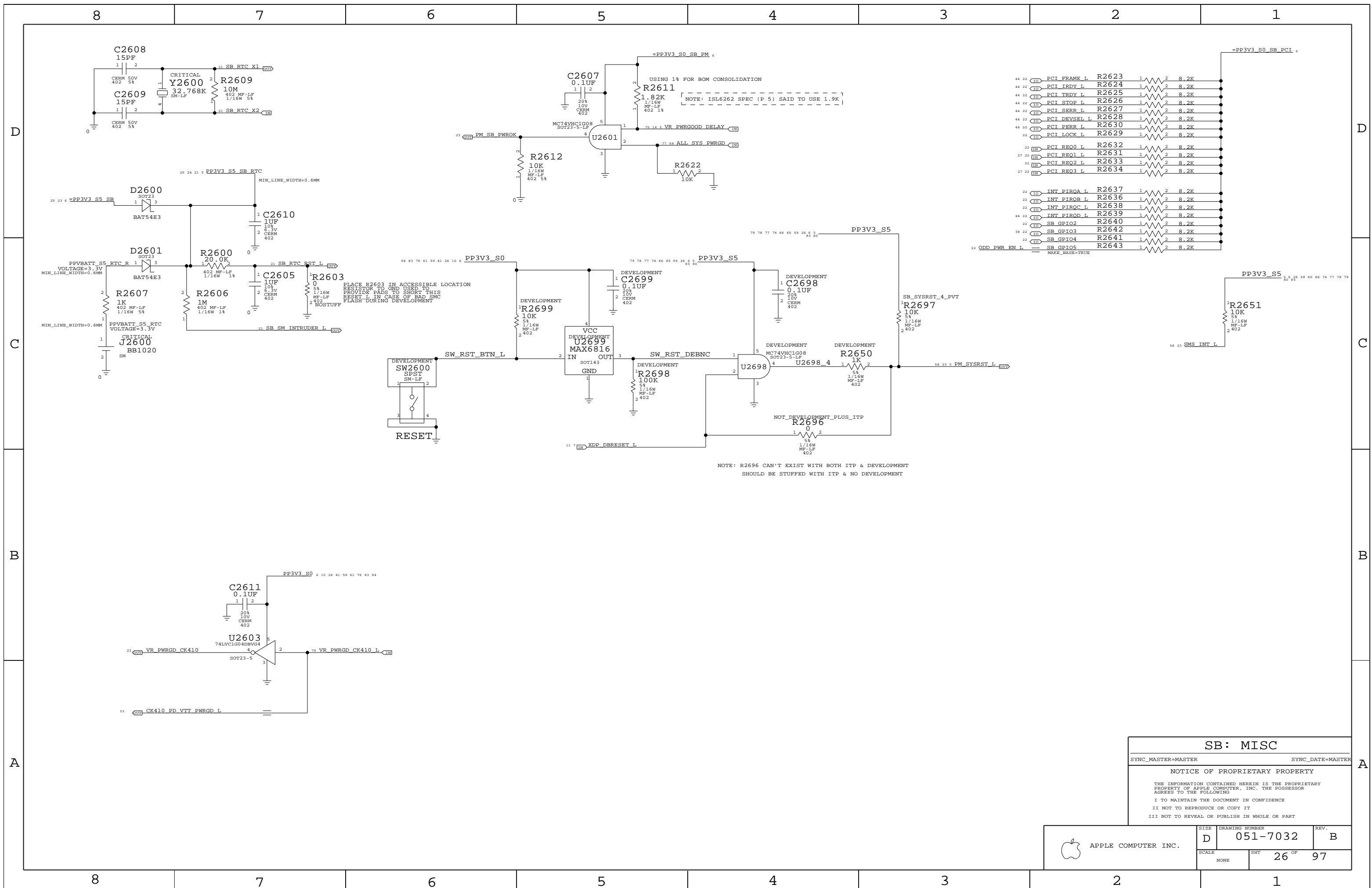
PLACEMENT NOTE:  
 PLACE CAPS NEAR PIN W5 OF SB

PLACEMENT NOTE:  
 PLACE CAPS NEAR PINS  
 A24 ... G19 AND P7 OF SB

PLACEMENT NOTE:  
 PLACE CAPS NEAR PINS  
 K3 ... N7 OF SB

PLACEMENT NOTE:  
 PLACE CAPS NEAR PINS  
 AB8 AND AC8 OF SB

PLACEMENT NOTE:  
 PLACE < 2.54MM OF SB ON SECONDARY OR  
 3.56MM ON PRIMARY NEAR PINS A1 ... J7



**SB: MISC**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER


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	D	051-7032	B
SCALE	SHT	26 OF	97
NONE			

8

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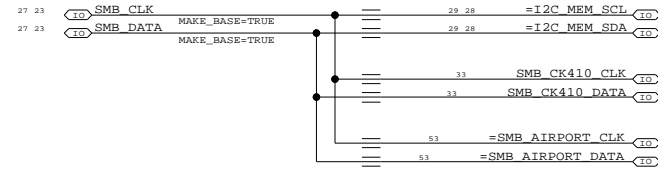
2

1

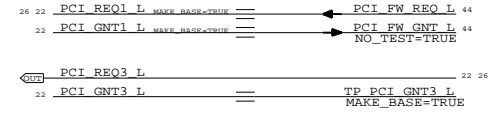
D

D

### SB I2C BUSSES

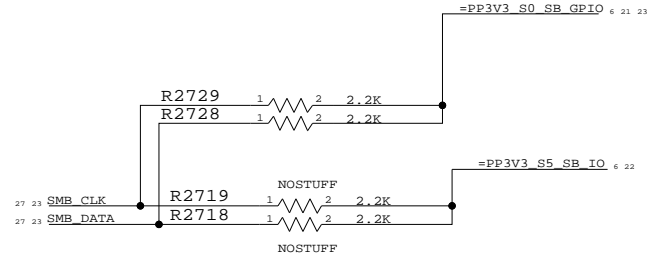


### PCI CONTROL



C

C



B

B

A

A

### SB: SMB HUB AND ALIAS

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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	D	051-7032	B
SCALE	SHT		OF
NONE	27		97

8

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# Page Notes

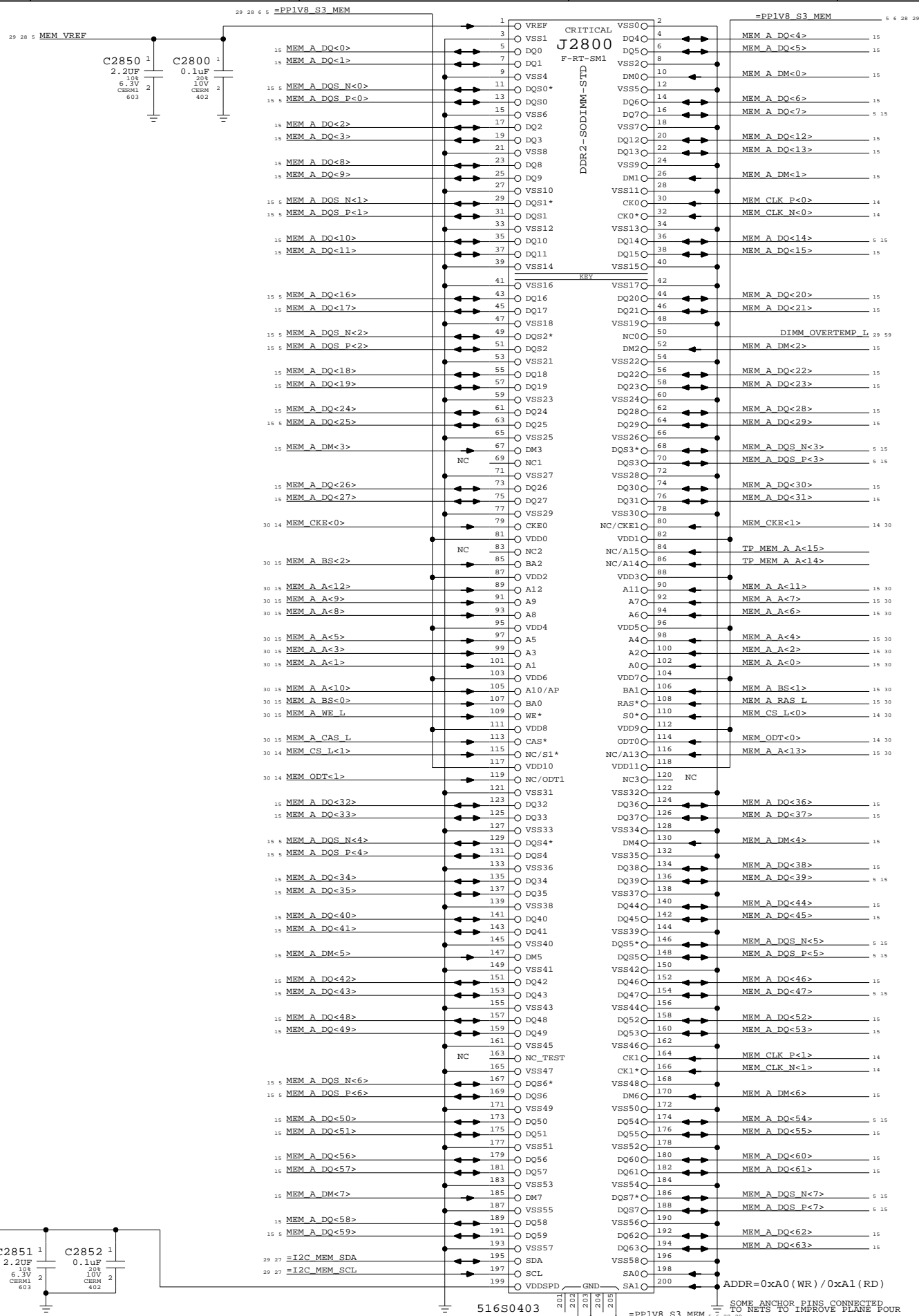
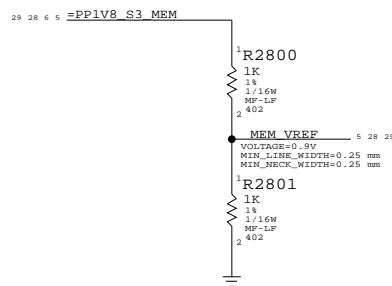
Power aliases required by this page:  
 - =PPIV8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

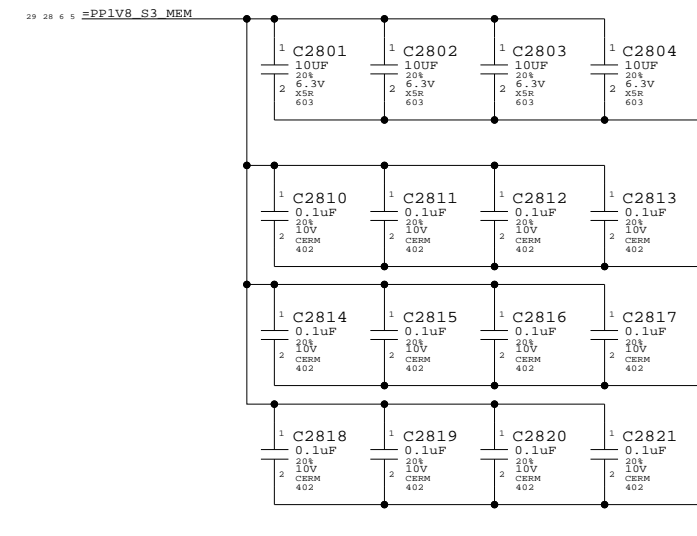
## DDR2 VRef

One 0.1uF per connector



## DDR2 Bypass Caps

(For return current)



**DDR2 SO-DIMM Connector A**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	28 OF 97	
NONE			

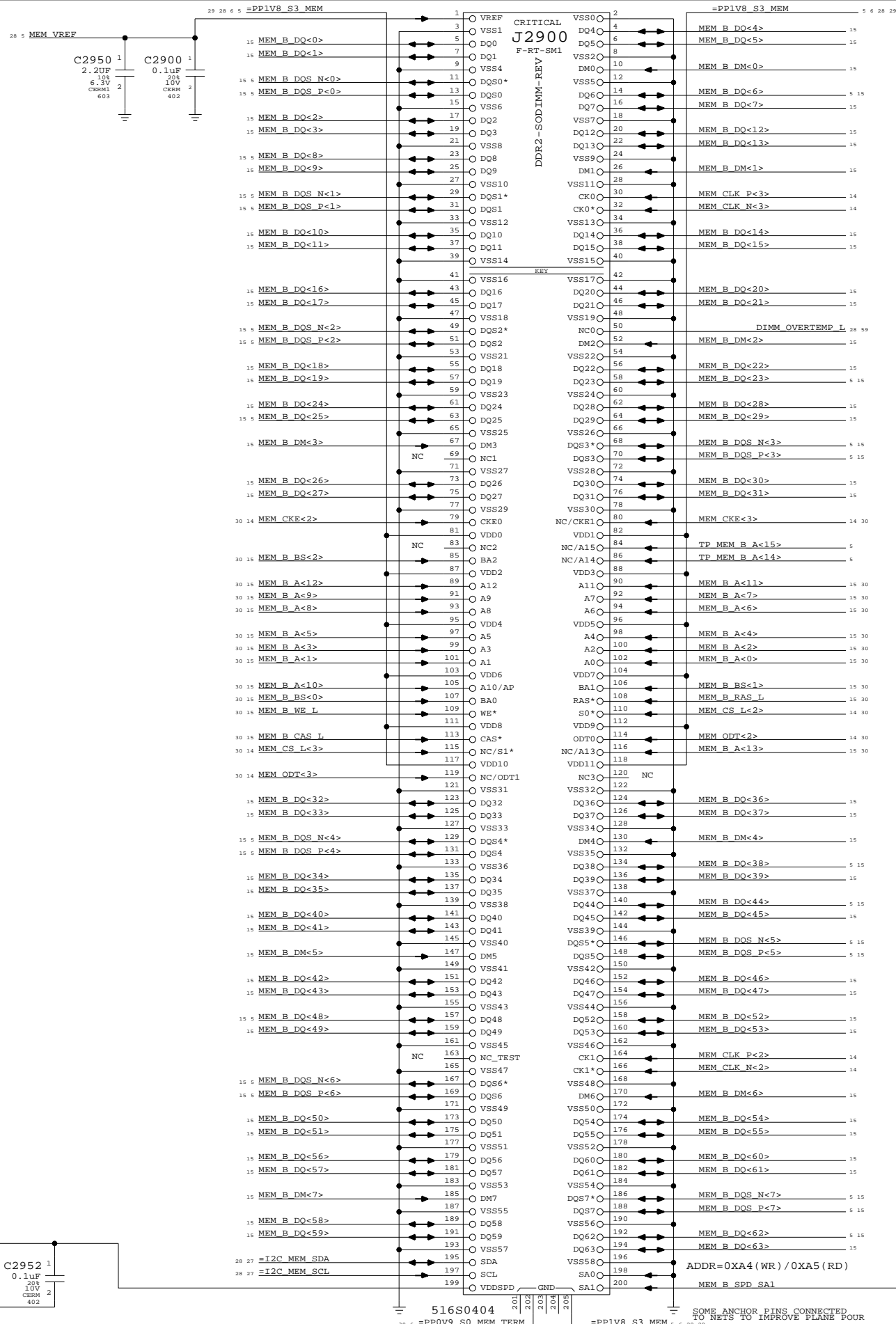
# Page Notes

Power aliases required by this page:  
 - =PP1V8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

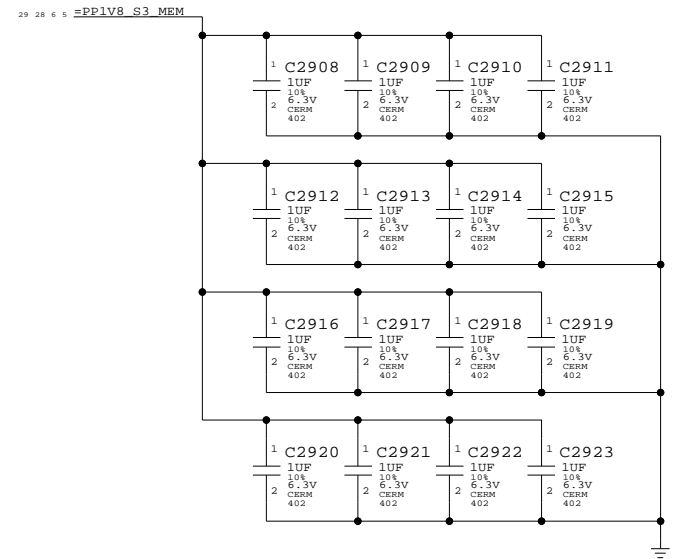
Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

NOTE: This page does not supply VREF.  
 The reference voltage must be provided by another page.



## DDR2 Bypass Caps (For return current)



**DDR2 SO-DIMM Connector B**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 29 OF 97	

8

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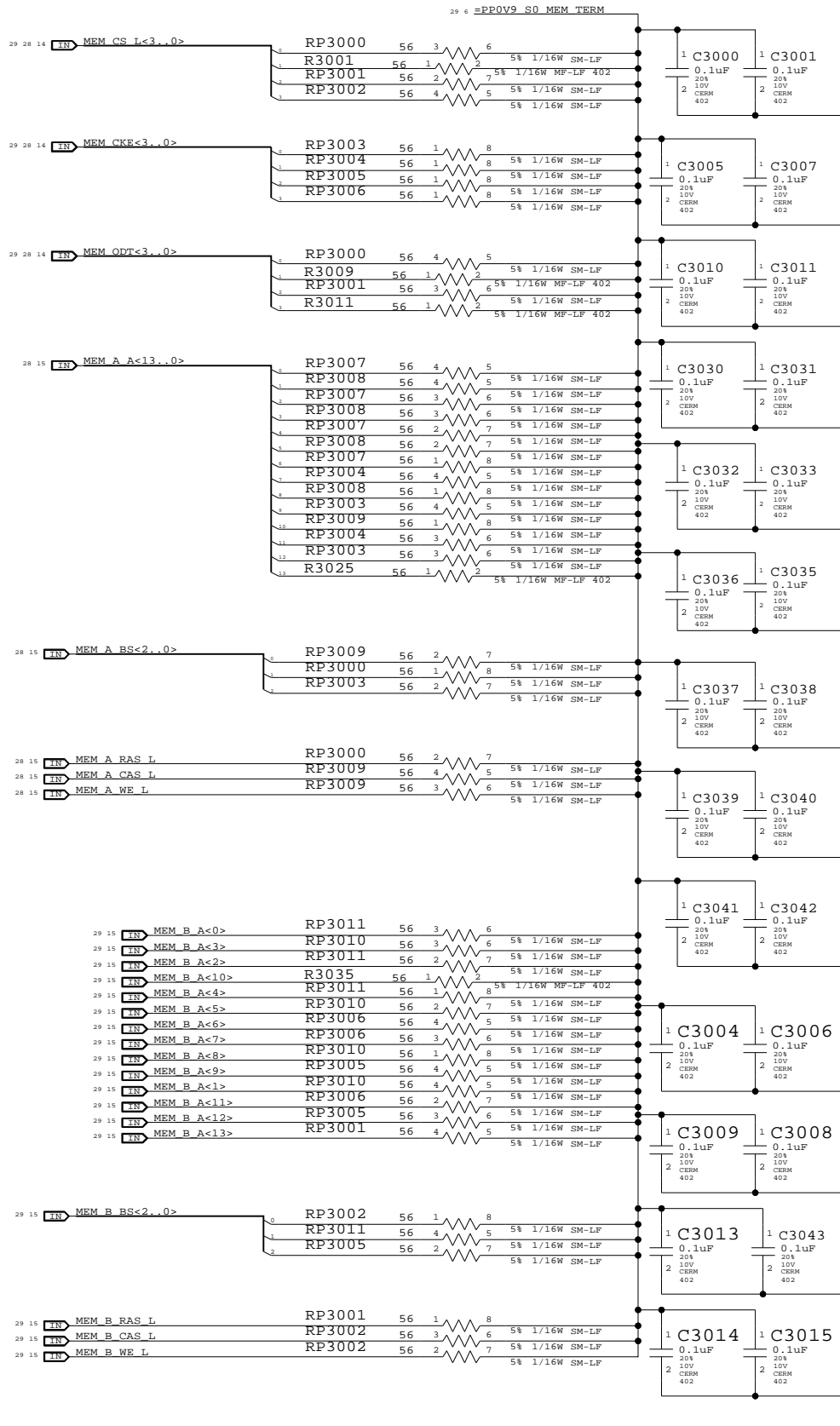
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One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it



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Memory Active Termination

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	D	051-7032	B
SCALE	SHT	OF	
NONE	30	97	

Page Notes

Power aliases required by this page:  
 - =PP5V\_S0\_MEMVTT  
 - =PP1V8\_S0\_MEMVTT  
 - =PP0V9\_S0\_MEMVTT\_LDO

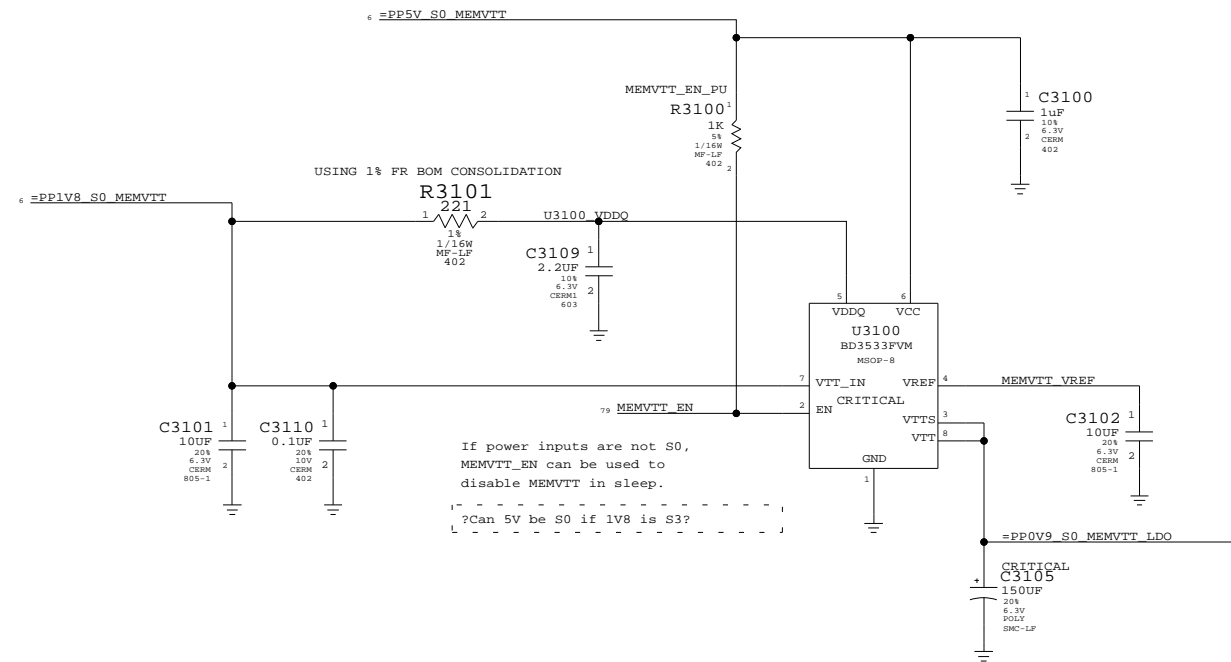
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Signal aliases required by this page:  
 (NONE)

---

BOM options provided by this page:  
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

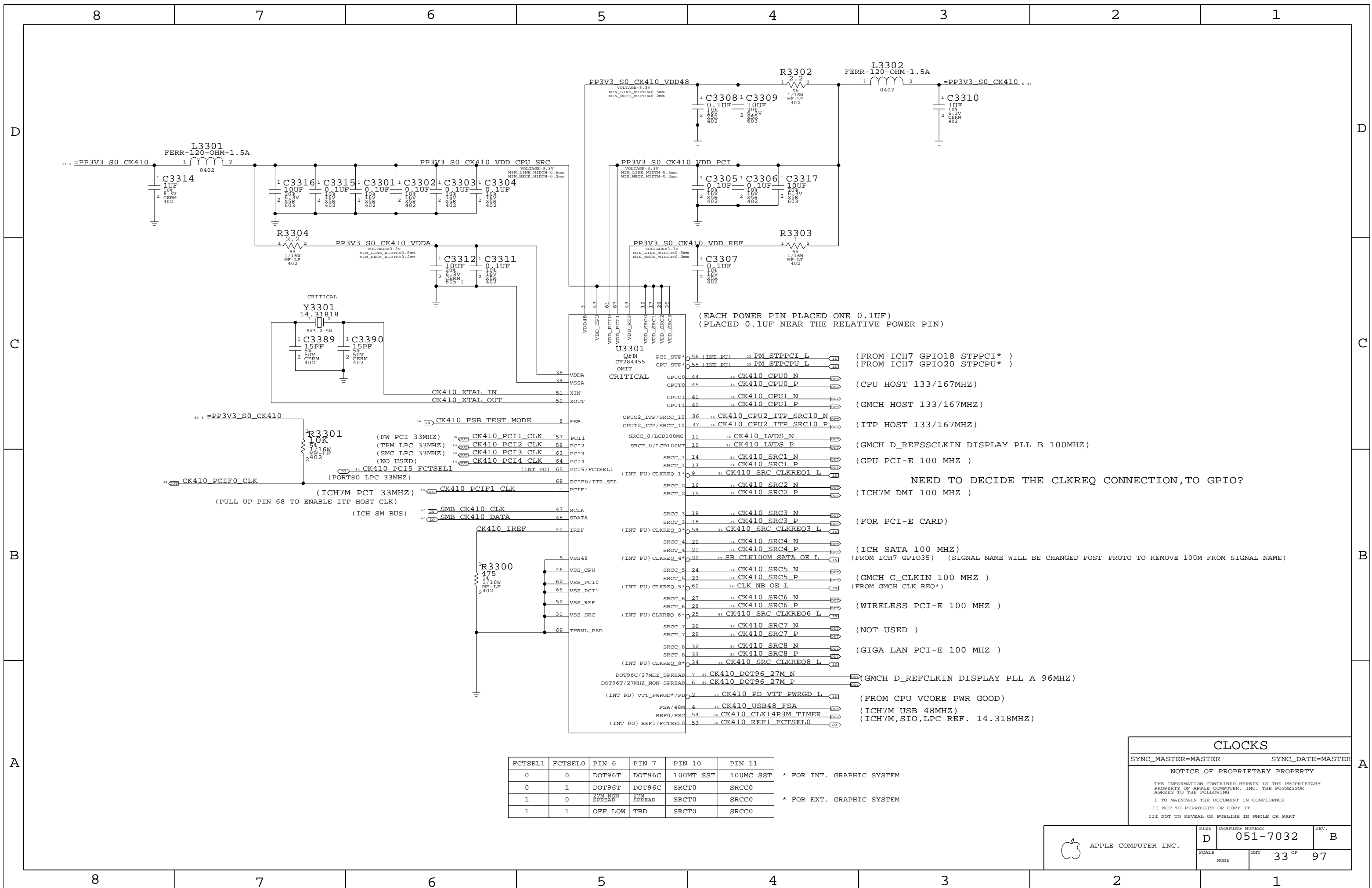
SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI\* )  
(FROM ICH7 GPIO20 STPCPU\* )

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ )

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ )

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)  
(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G\_CLKIN 100 MHZ )  
(FROM GMCH CLK\_REQ\*)

(WIRELESS PCI-E 100 MHZ )

(NOT USED )

(GIGA LAN PCI-E 100 MHZ )

(GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)  
(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM

\* FOR EXT. GRAPHIC SYSTEM

**CLOCKS**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

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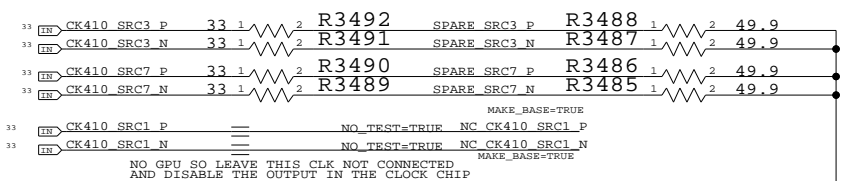
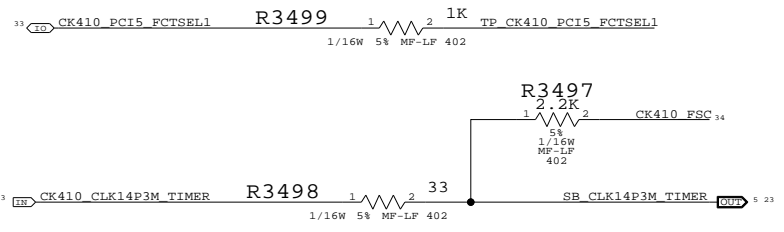
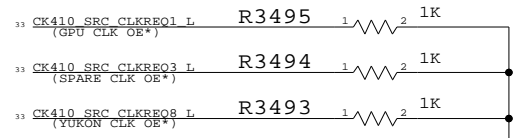
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	33 OF 97	
NONE			

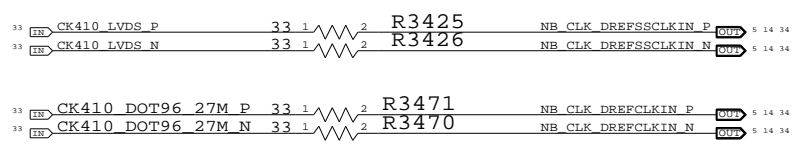
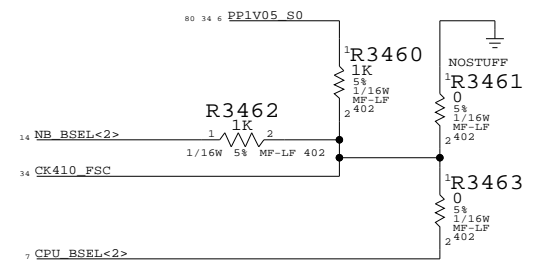
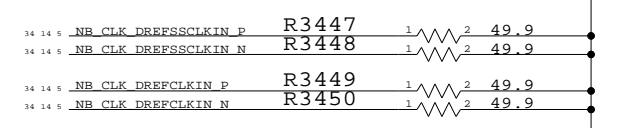
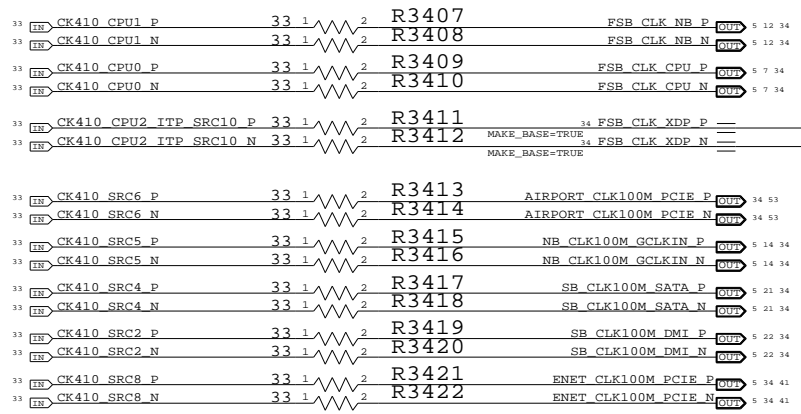
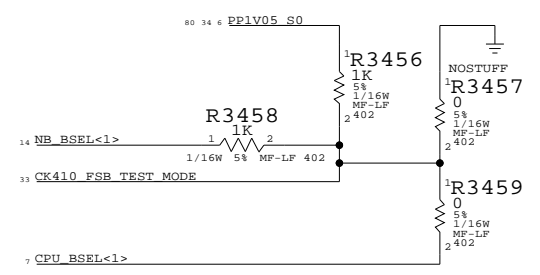
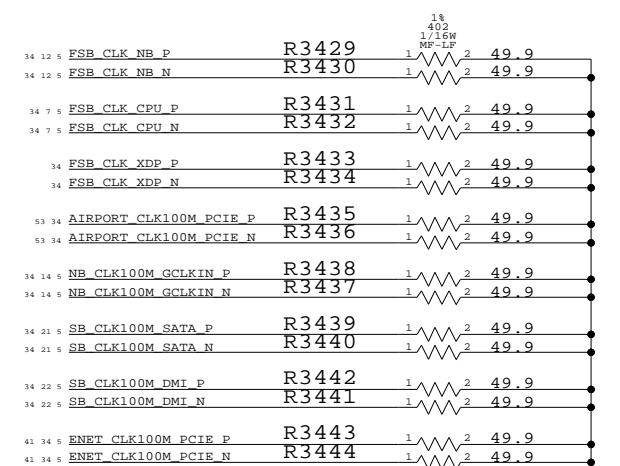
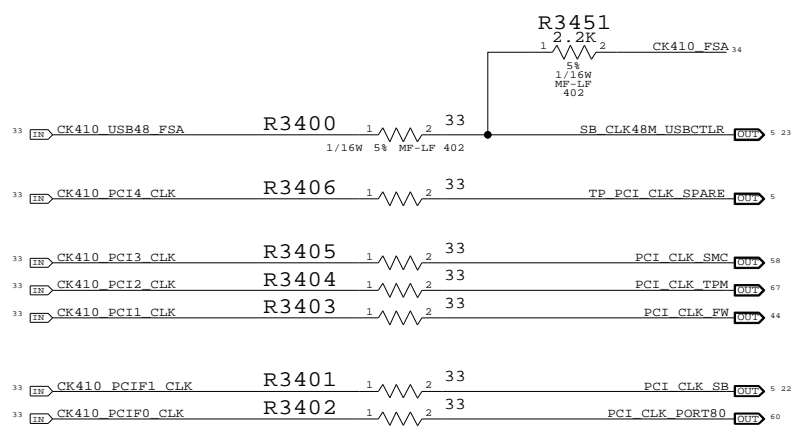
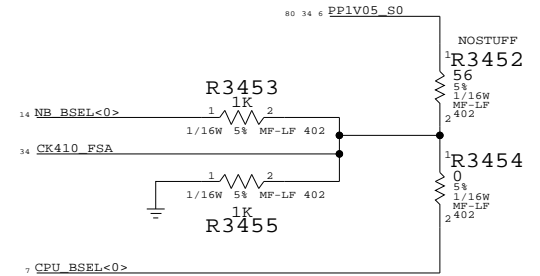


NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457 R3458
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458



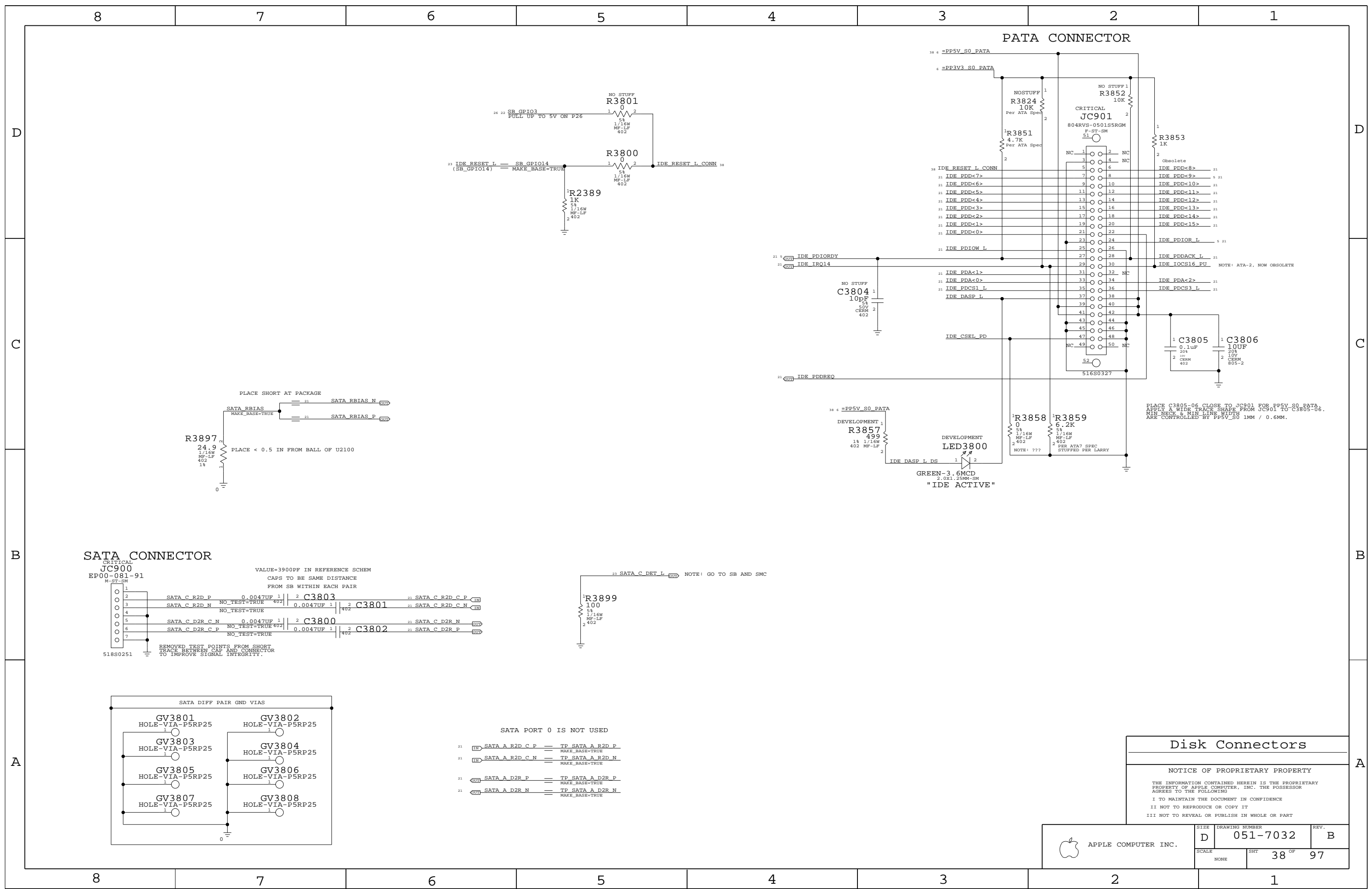
**CLOCKS: TERMINATIONS**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

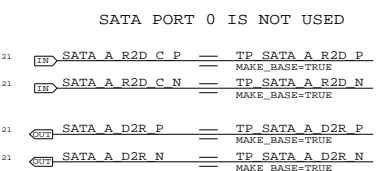
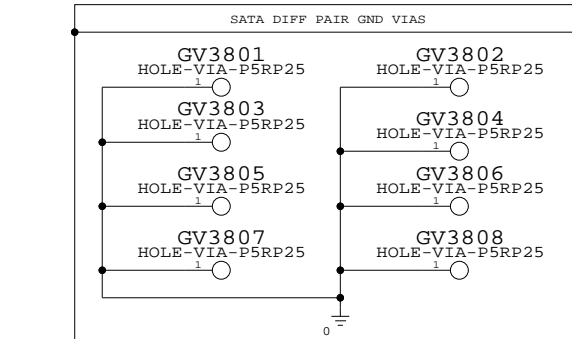
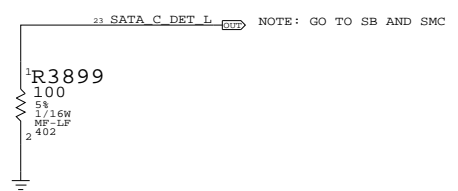
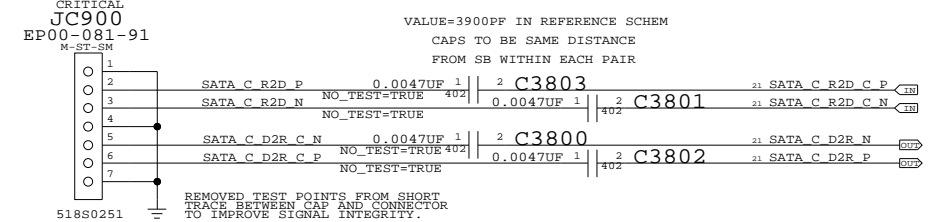
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	D	051-7032	B
SCALE	SHT	34 OF 97	
NONE			



**SATA CONNECTOR**



**Disk Connectors**

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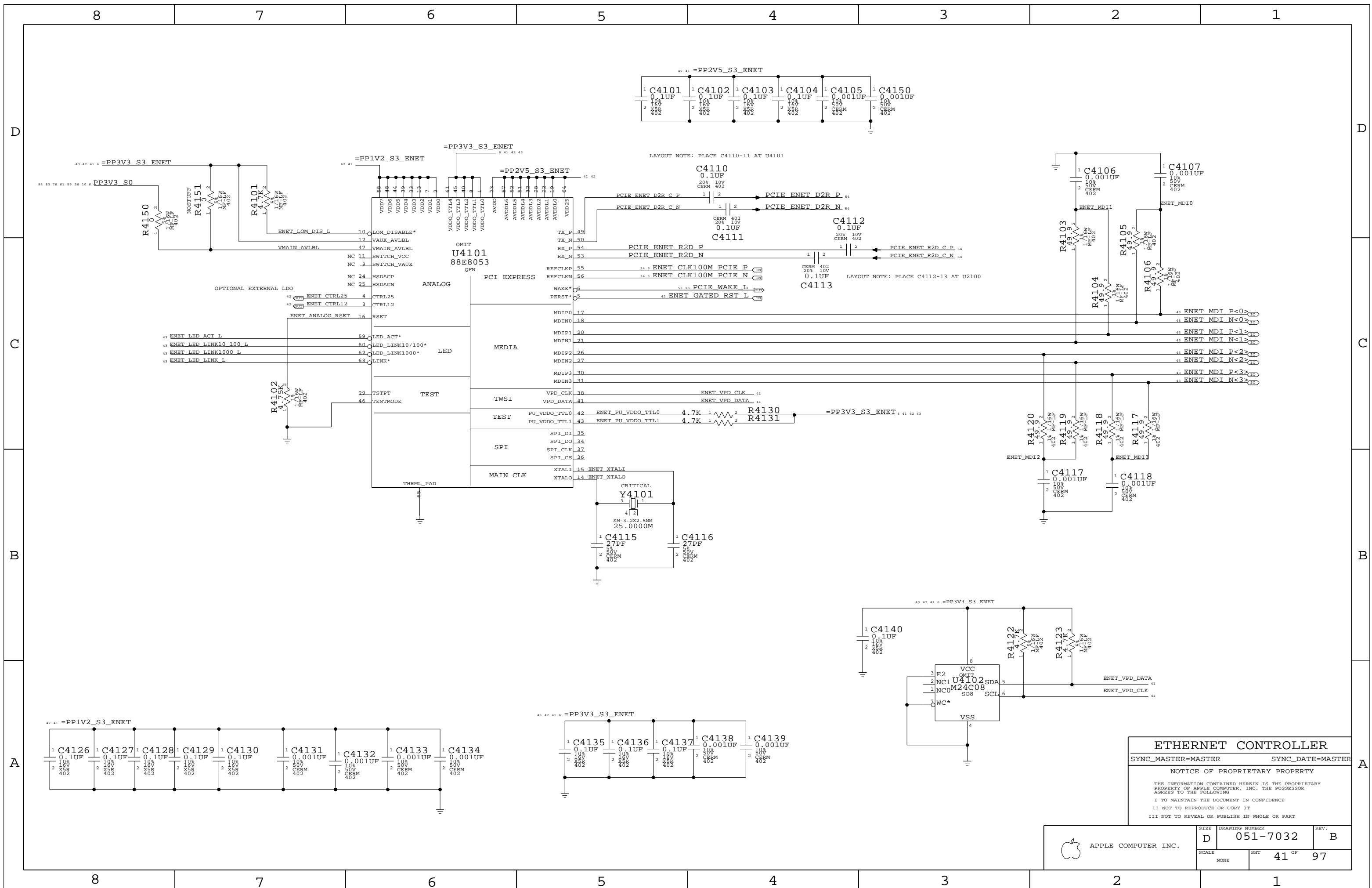
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SCALE	SHT	38 OF 97	
NONE			



**ETHERNET CONTROLLER**

SYNC\_MASTER=MASTER SYNC\_DATA=MASTER

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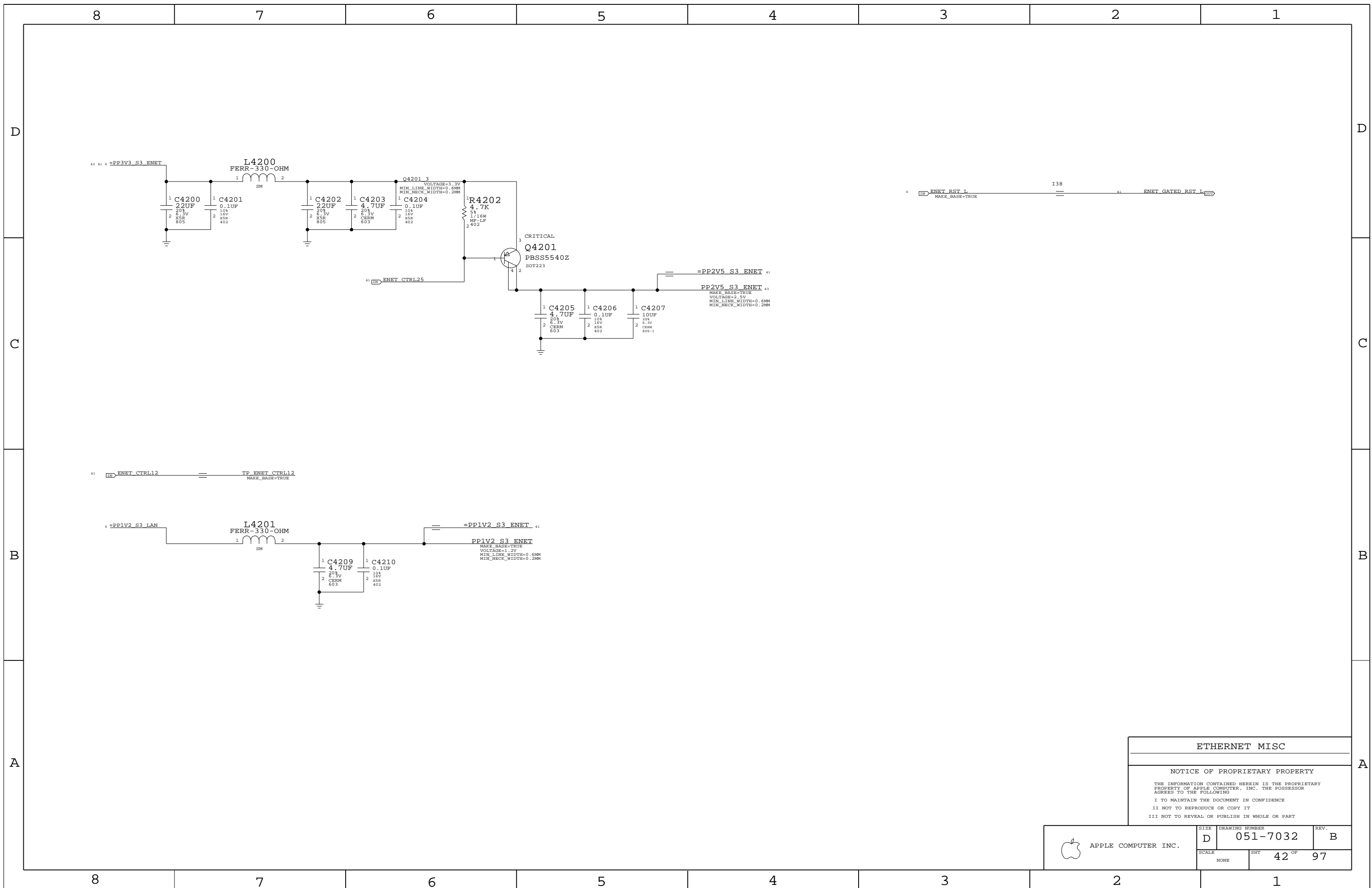
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	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

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NOTICE OF PROPRIETARY PROPERTY

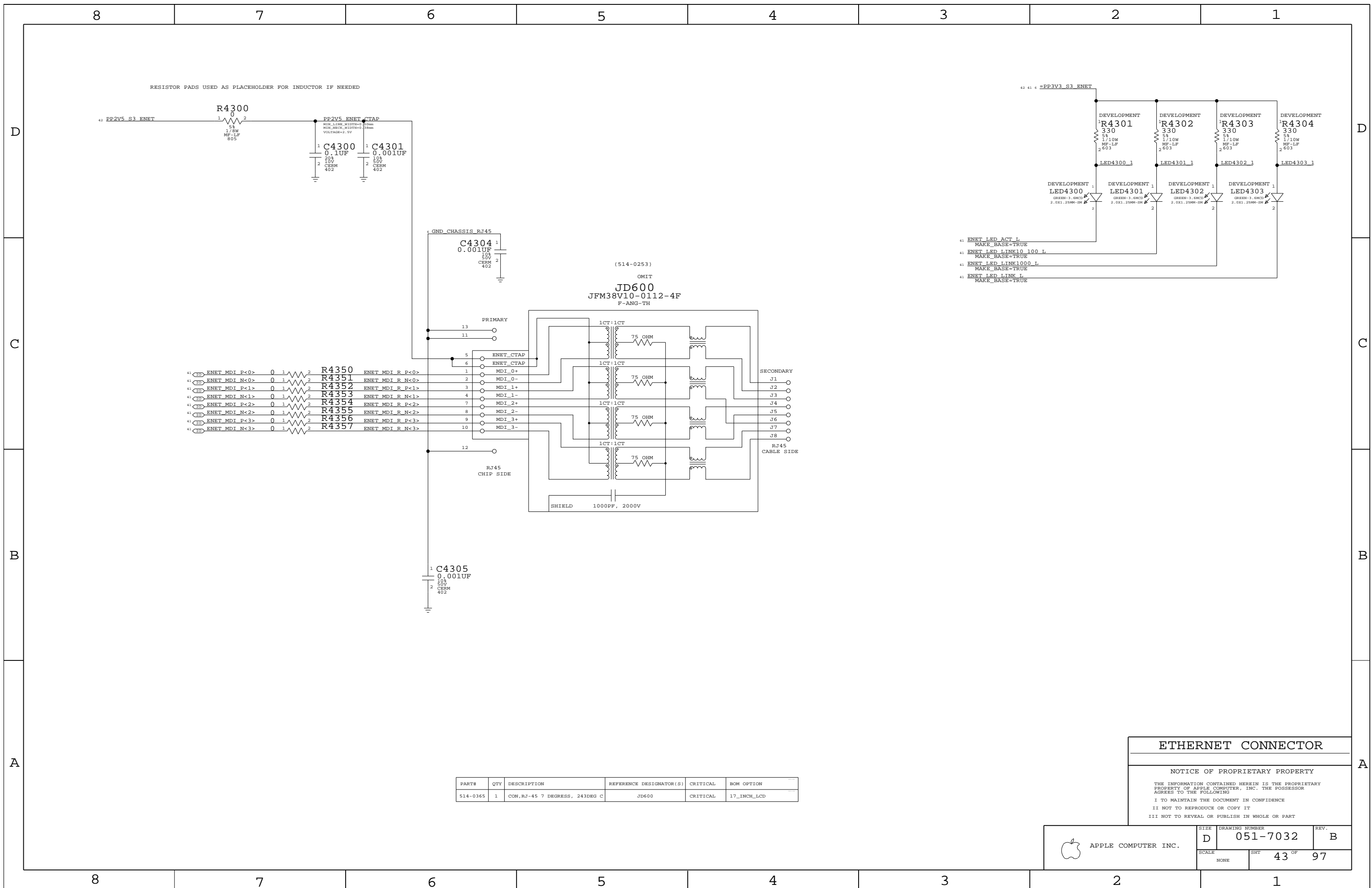
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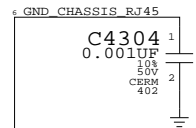
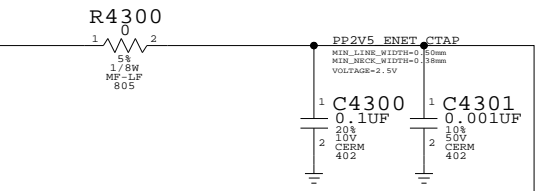
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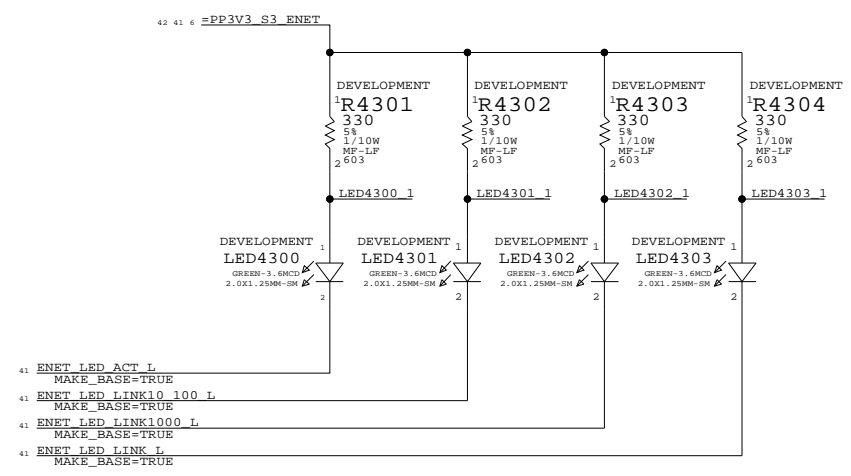
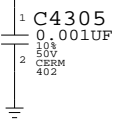
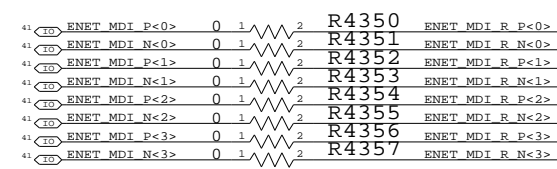
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHEET <b>42</b> OF <b>97</b>	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



(514-0253)  
OMIT  
JD600  
JFM38V10-0112-4F  
F-ANG-TH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

**ETHERNET CONNECTOR**

NOTICE OF PROPRIETARY PROPERTY

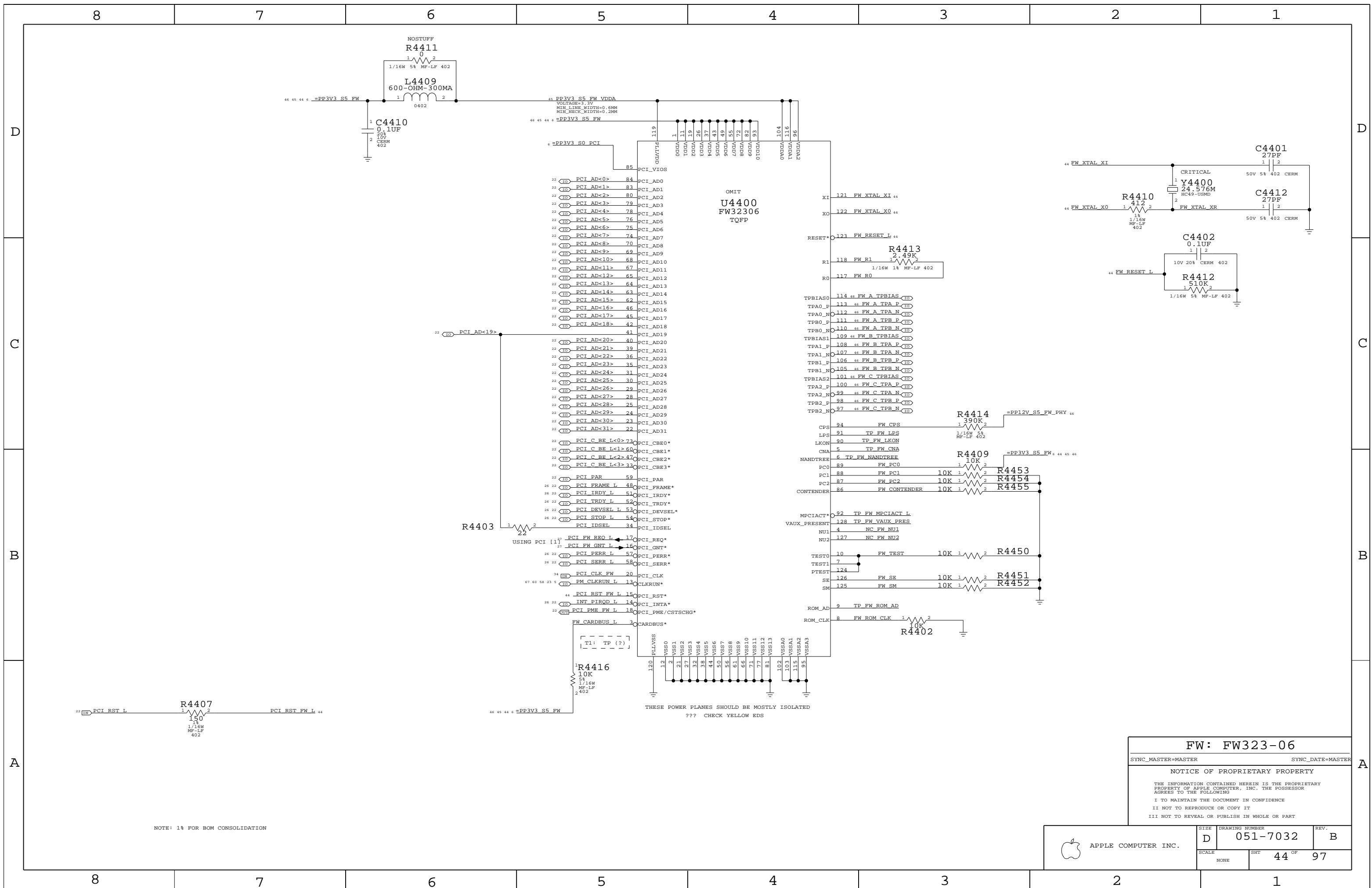
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SCALE	SHT	43 OF 97	
NONE			



**FW: FW323-06**

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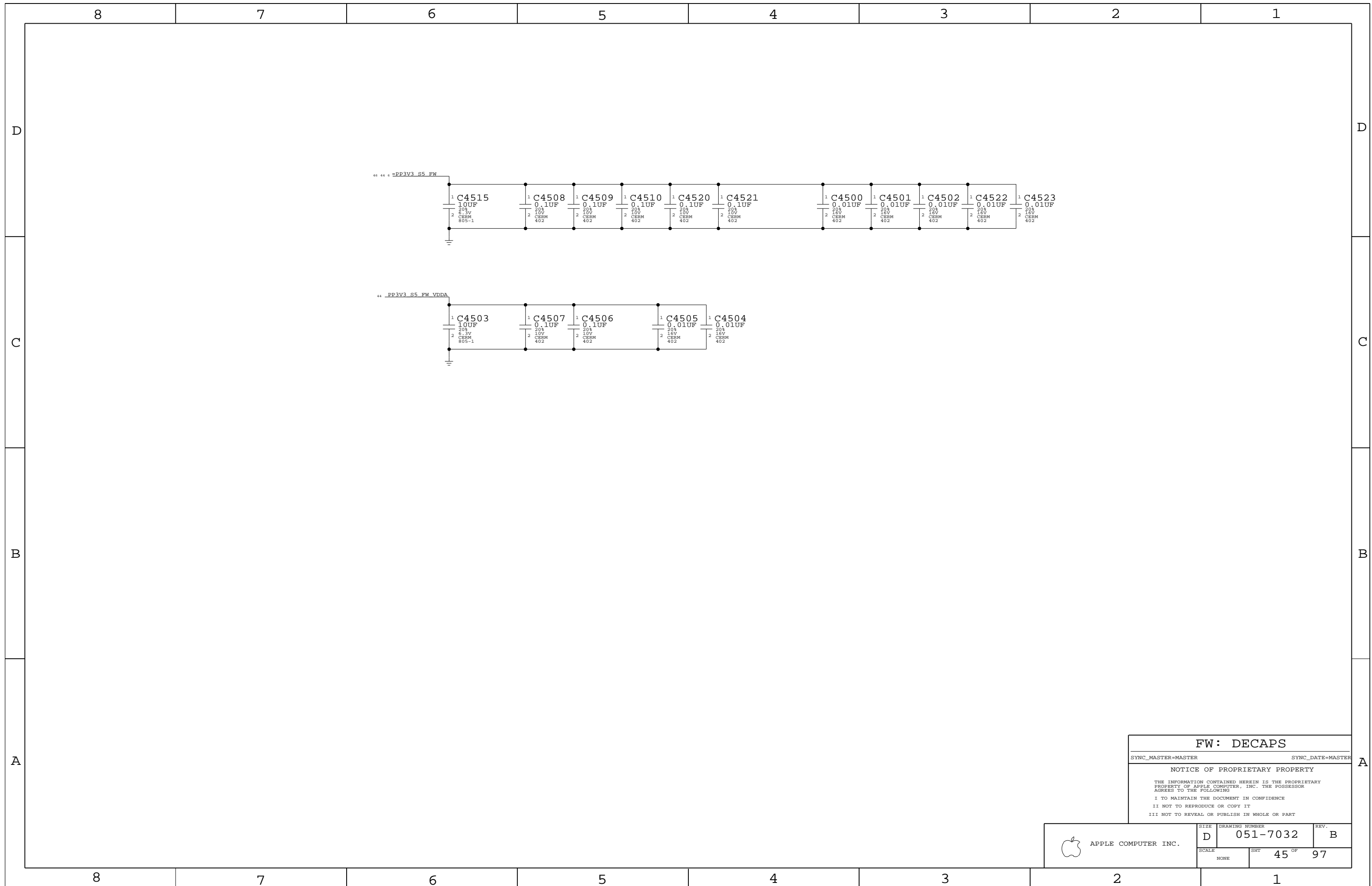
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	44 OF 97	
NONE			

NOTE: 1% FOR BOM CONSOLIDATION



**FW: DECAPS**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER


**NOTICE OF PROPRIETARY PROPERTY**

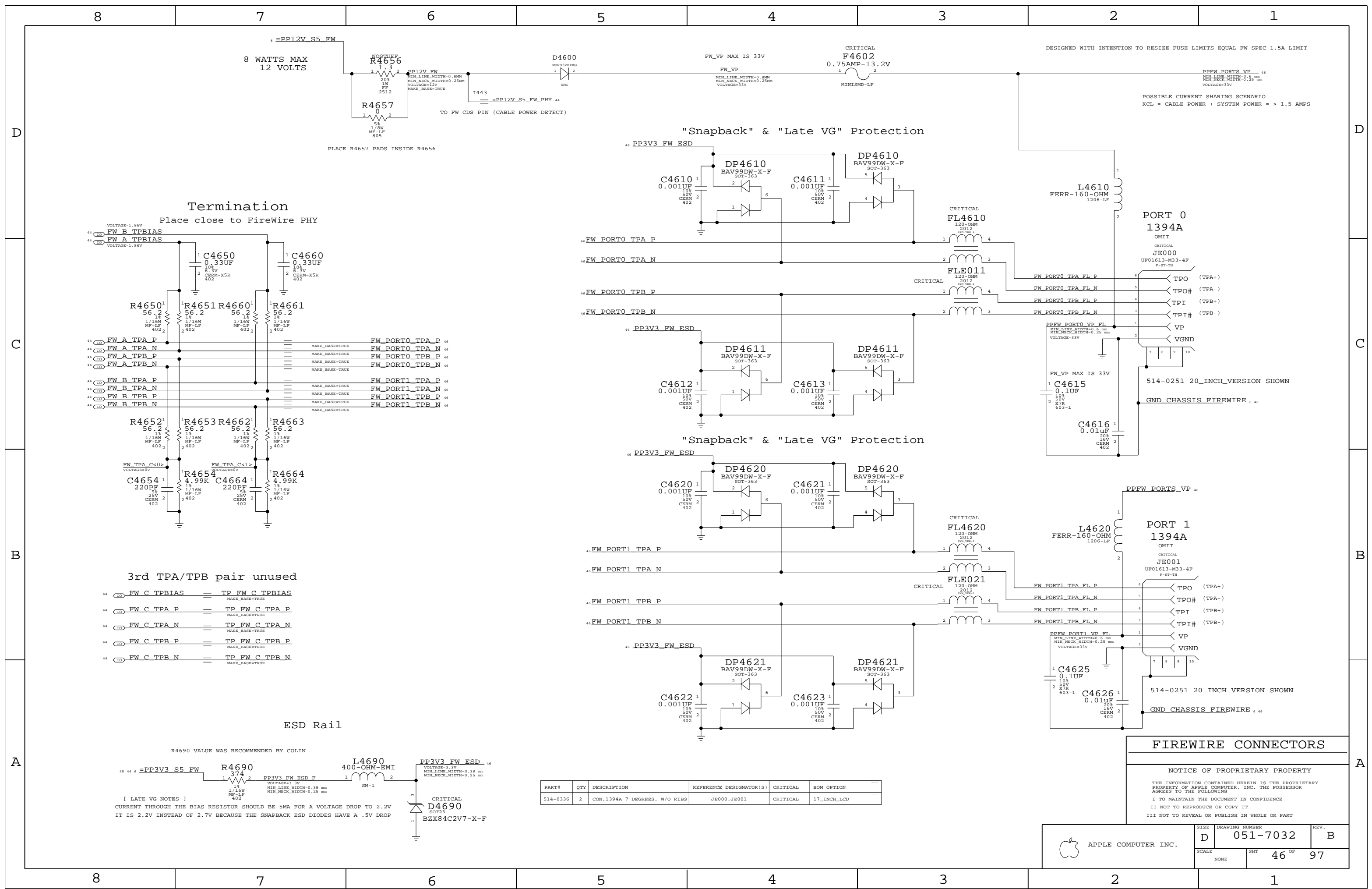
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	D	051-7032	B
SCALE	SHT	OF	
NONE	45	97	



DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

PPFW\_PORTS\_VP 46  
 MIN\_LINE\_WIDTH=0.5 mm  
 MIN\_NECK\_WIDTH=0.25 mm  
 VOLTAGE=3.3V

POSSIBLE CURRENT SHARING SCENARIO  
 KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

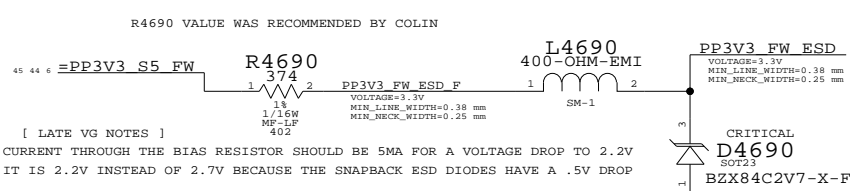
**Termination**  
 Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

**FIREWIRE CONNECTORS**

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APPLE COMPUTER INC.

SCALE: NONE

SHEET: 46 OF 97

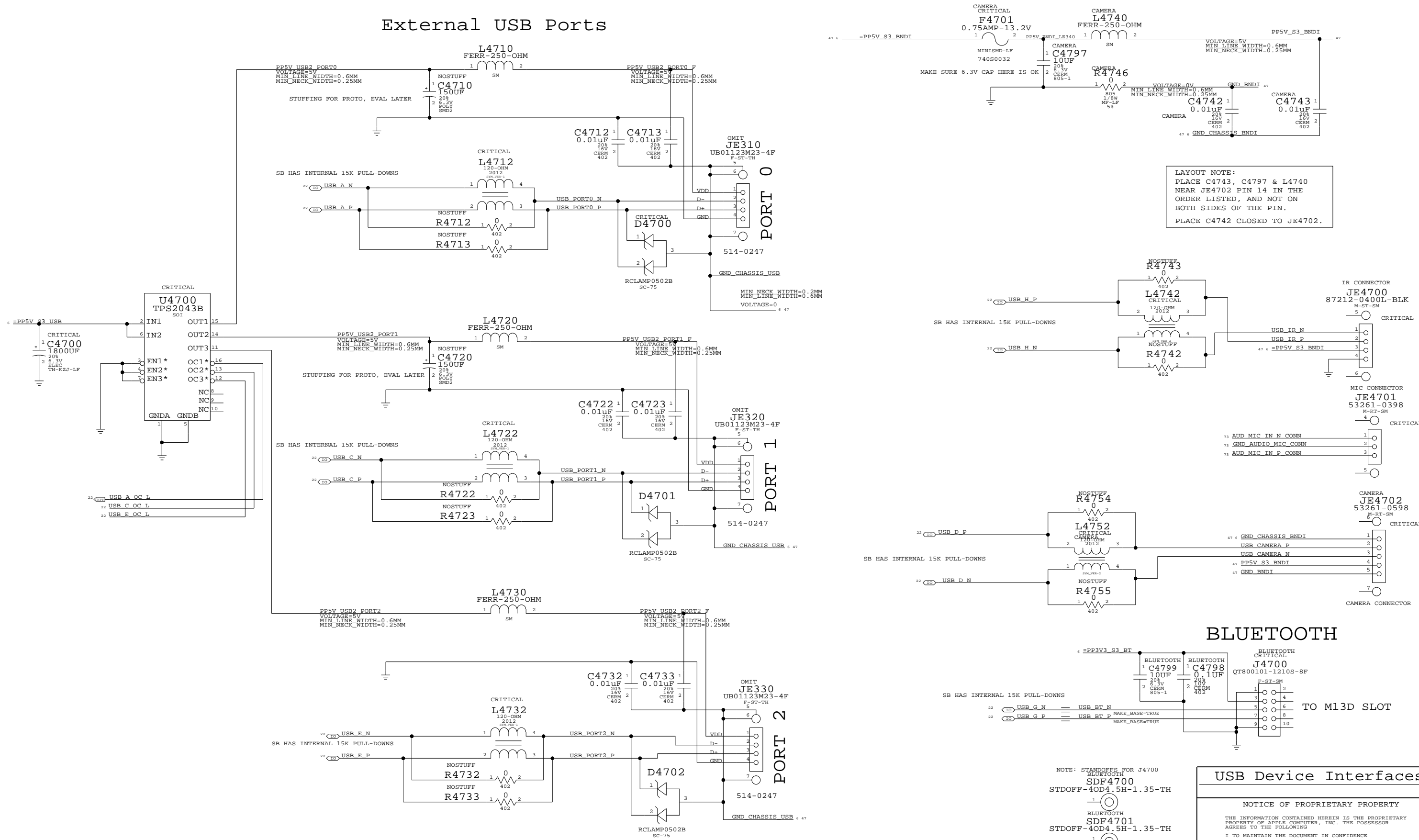
SIZE: D

DRAWING NUMBER: 051-7032

REV.: B



# External USB Ports



LAYOUT NOTE:  
 PLACE C4743, C4797 & L4740  
 NEAR JE4702 PIN 14 IN THE  
 ORDER LISTED, AND NOT ON  
 BOTH SIDES OF THE PIN.  
 PLACE C4742 CLOSED TO JE4702.

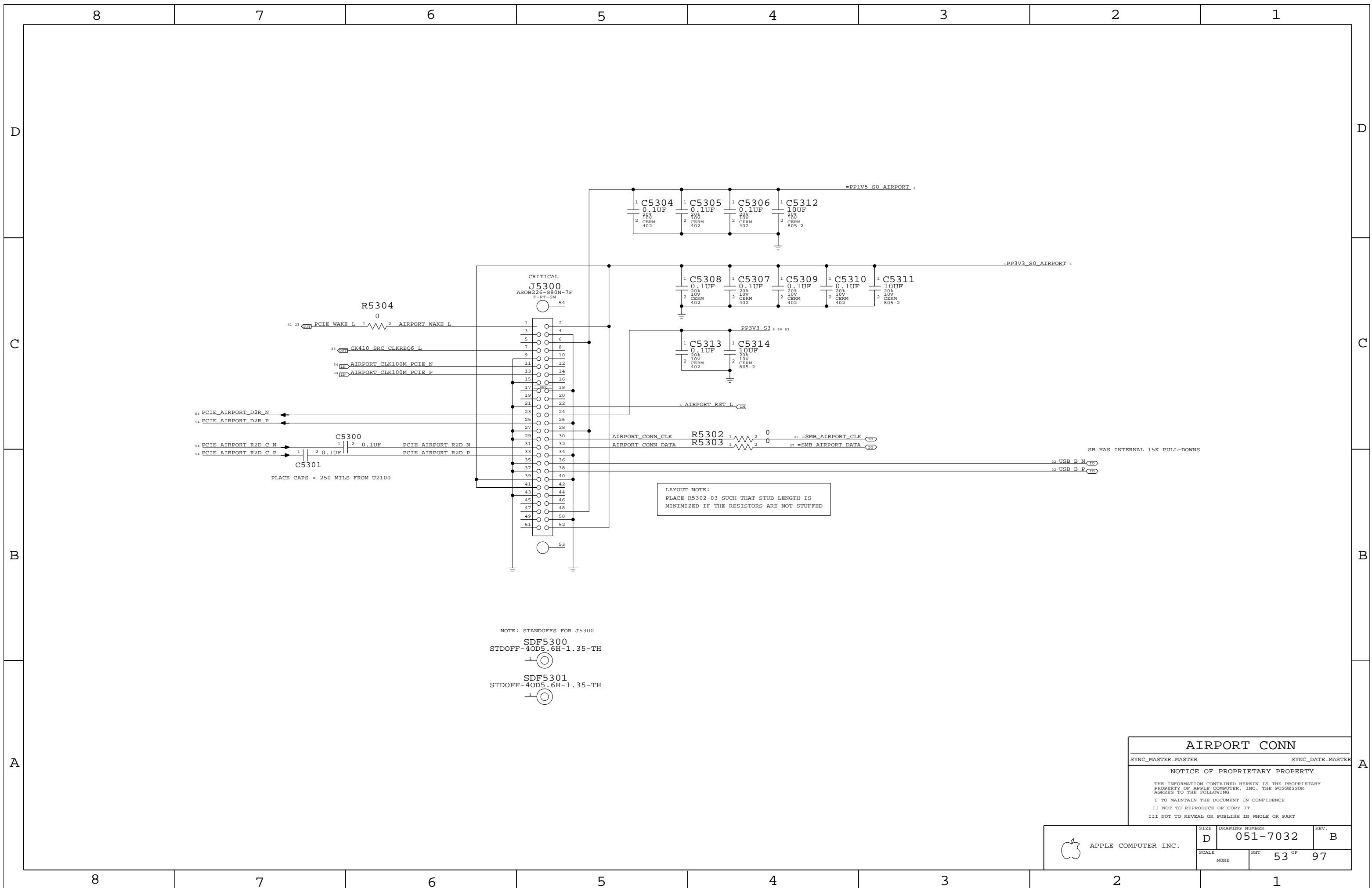
## BLUETOOTH

## USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	47 OF 97	
NONE			



R5304  
0

41 23 PCIE\_WAKE L 1 2 AIRPORT\_WAKE L

33 CK410\_SRC\_CLKREQ6 L

34 AIRPORT\_CLK100M\_PCIE\_N

34 AIRPORT\_CLK100M\_PCIE\_P

54 PCIE\_AIRPORT\_D2R\_N

54 PCIE\_AIRPORT\_D2R\_P

54 PCIE\_AIRPORT\_R2D\_C\_N

54 PCIE\_AIRPORT\_R2D\_C\_P

C5300  
1 2 0.1UF  
PCIE\_AIRPORT\_R2D\_N  
PCIE\_AIRPORT\_R2D\_P

C5301

PLACE CAPS < 250 MILS FROM U2100

AIRPORT\_CONN\_CLK R5302 1 2 0  
AIRPORT\_CONN\_DATA R5303 1 2 0

PP3V3\_S3 6 59 83

23 =SMB\_AIRPORT\_CLK  
27 =SMB\_AIRPORT\_DATA

SB HAS INTERNAL 15K PULL-DOWNS

22 USB\_B\_N

22 USB\_B\_P

LAYOUT NOTE:  
PLACE R5302-03 SUCH THAT STUB LENGTH IS  
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300

SDF5300  
STDOFF-40D5.6H-1.35-TH



SDF5301  
STDOFF-40D5.6H-1.35-TH



**AIRPORT CONN**  
 SYNC\_MASTER=MASTER SYNC\_DATE=MASTER  
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	D	051-7032	B
SCALE	SHT	53 OF 97	
NONE			

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 IN PCIE C R2D C N == TP PCIE C R2D C N  
MAKE\_BASE=TRUE

22 IN PCIE C R2D C P == TP PCIE C R2D C P  
MAKE\_BASE=TRUE

22 OUT PCIE C D2R N == TP PCIE C D2R N  
MAKE\_BASE=TRUE

22 OUT PCIE C D2R P == TP PCIE C D2R P  
MAKE\_BASE=TRUE

22 IN PCIE D R2D C N == TP PCIE D R2D C N  
MAKE\_BASE=TRUE

22 IN PCIE D R2D C P == TP PCIE D R2D C P  
MAKE\_BASE=TRUE

22 OUT PCIE D D2R N == TP PCIE D D2R N  
MAKE\_BASE=TRUE

22 OUT PCIE D D2R P == TP PCIE D D2R P  
MAKE\_BASE=TRUE

22 IN PCIE E R2D C N == TP PCIE E R2D C N  
MAKE\_BASE=TRUE

22 IN PCIE E R2D C P == TP PCIE E R2D C P  
MAKE\_BASE=TRUE

22 OUT PCIE E D2R N == TP PCIE E D2R N  
MAKE\_BASE=TRUE

22 OUT PCIE E D2R P == TP PCIE E D2R P  
MAKE\_BASE=TRUE

22 IN PCIE F R2D C N == TP PCIE F R2D C N  
MAKE\_BASE=TRUE

22 IN PCIE F R2D C P == TP PCIE F R2D C P  
MAKE\_BASE=TRUE

22 OUT PCIE F D2R N == TP PCIE F D2R N  
MAKE\_BASE=TRUE

22 OUT PCIE F D2R P == TP PCIE F D2R P  
MAKE\_BASE=TRUE

USED PCIE PORTS

22 IN PCIE A R2D C N == PCIE AIRPORT R2D C N 53  
MAKE\_BASE=TRUE

22 IN PCIE A R2D C P == PCIE AIRPORT R2D C P 53  
MAKE\_BASE=TRUE

22 5 OUT PCIE A D2R N == PCIE AIRPORT D2R N 53  
MAKE\_BASE=TRUE

22 5 OUT PCIE A D2R P == PCIE AIRPORT D2R P 53  
MAKE\_BASE=TRUE


22 IN PCIE B R2D C N == PCIE ENET R2D C N 41  
MAKE\_BASE=TRUE

22 IN PCIE B R2D C P == PCIE ENET R2D C P 41  
MAKE\_BASE=TRUE

22 5 OUT PCIE B D2R N == PCIE ENET D2R N 41  
MAKE\_BASE=TRUE

22 5 OUT PCIE B D2R P == PCIE ENET D2R P 41  
MAKE\_BASE=TRUE

PCIE PORT ALIASES			
SYNC_MASTER=MASTER		SYNC_DATE=MASTER	
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	SCALE NONE	SHIT 54 OF 97	

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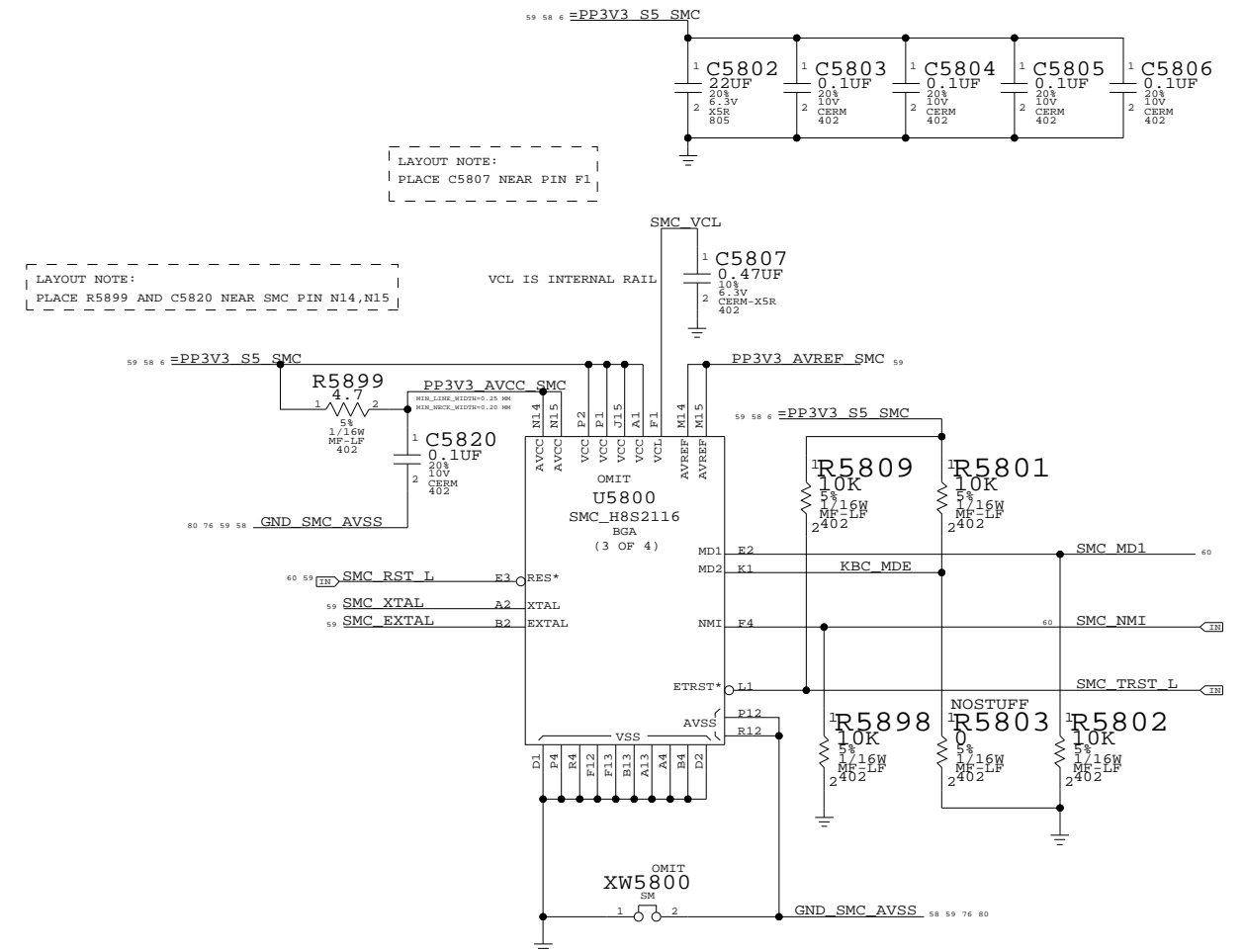
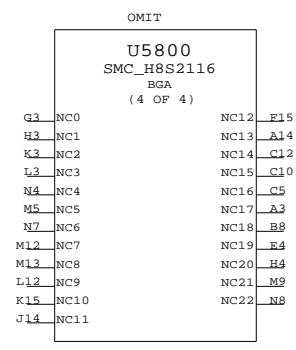
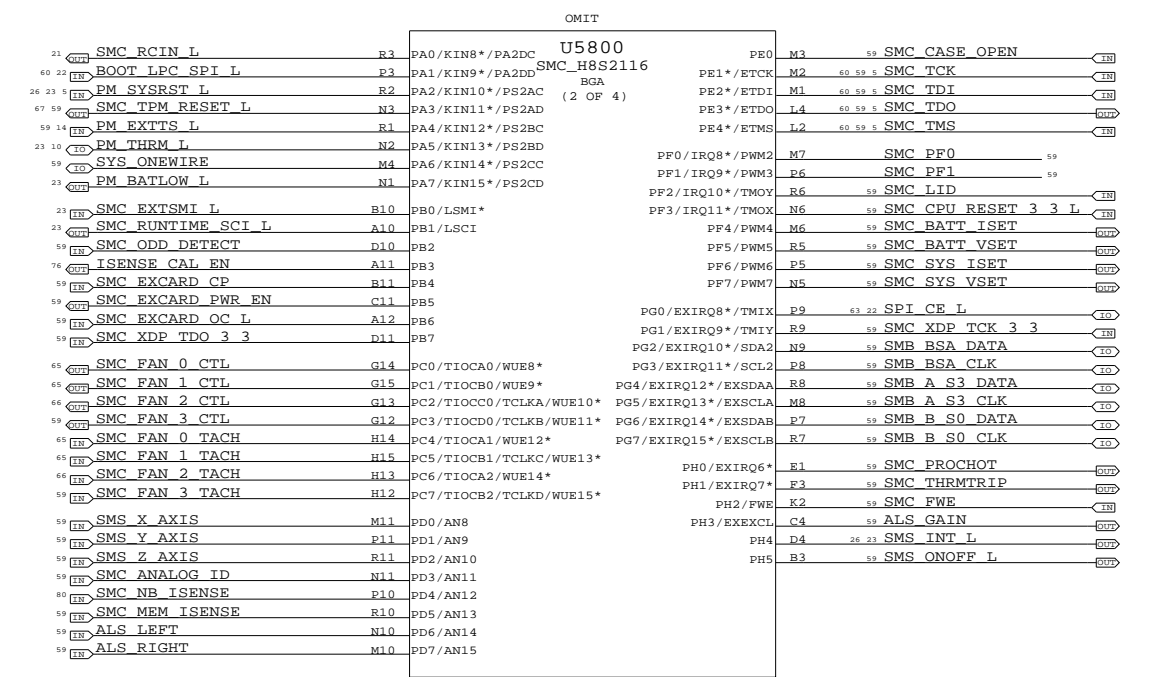
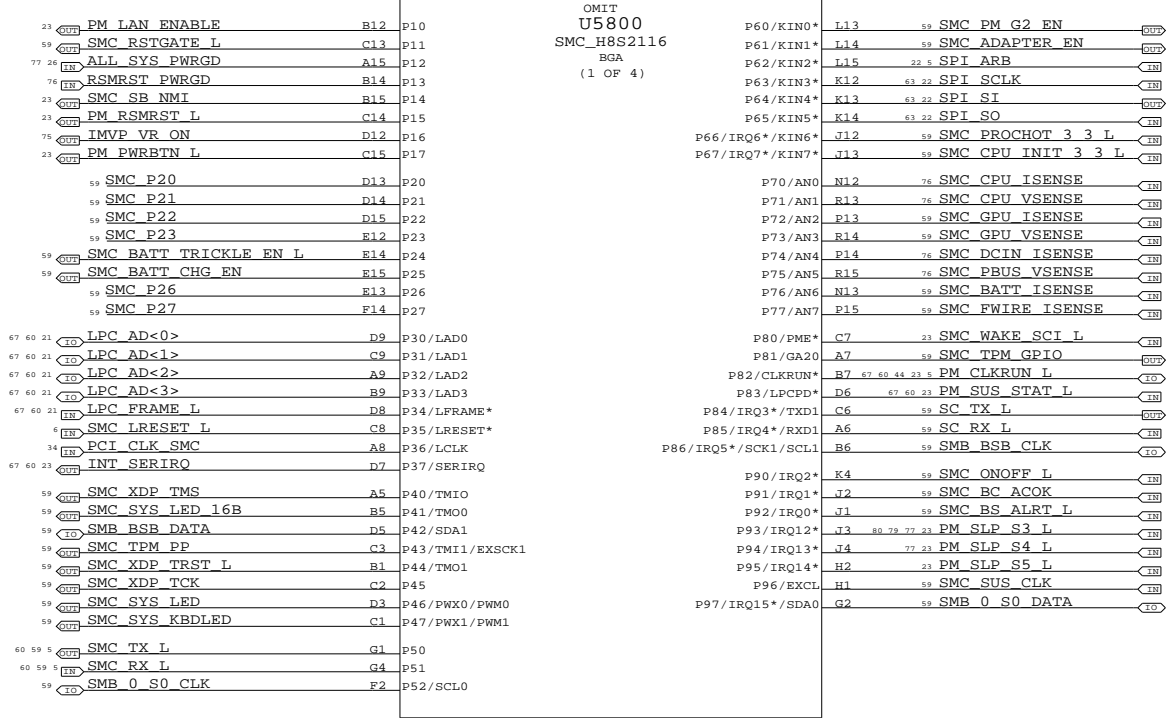
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC\_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

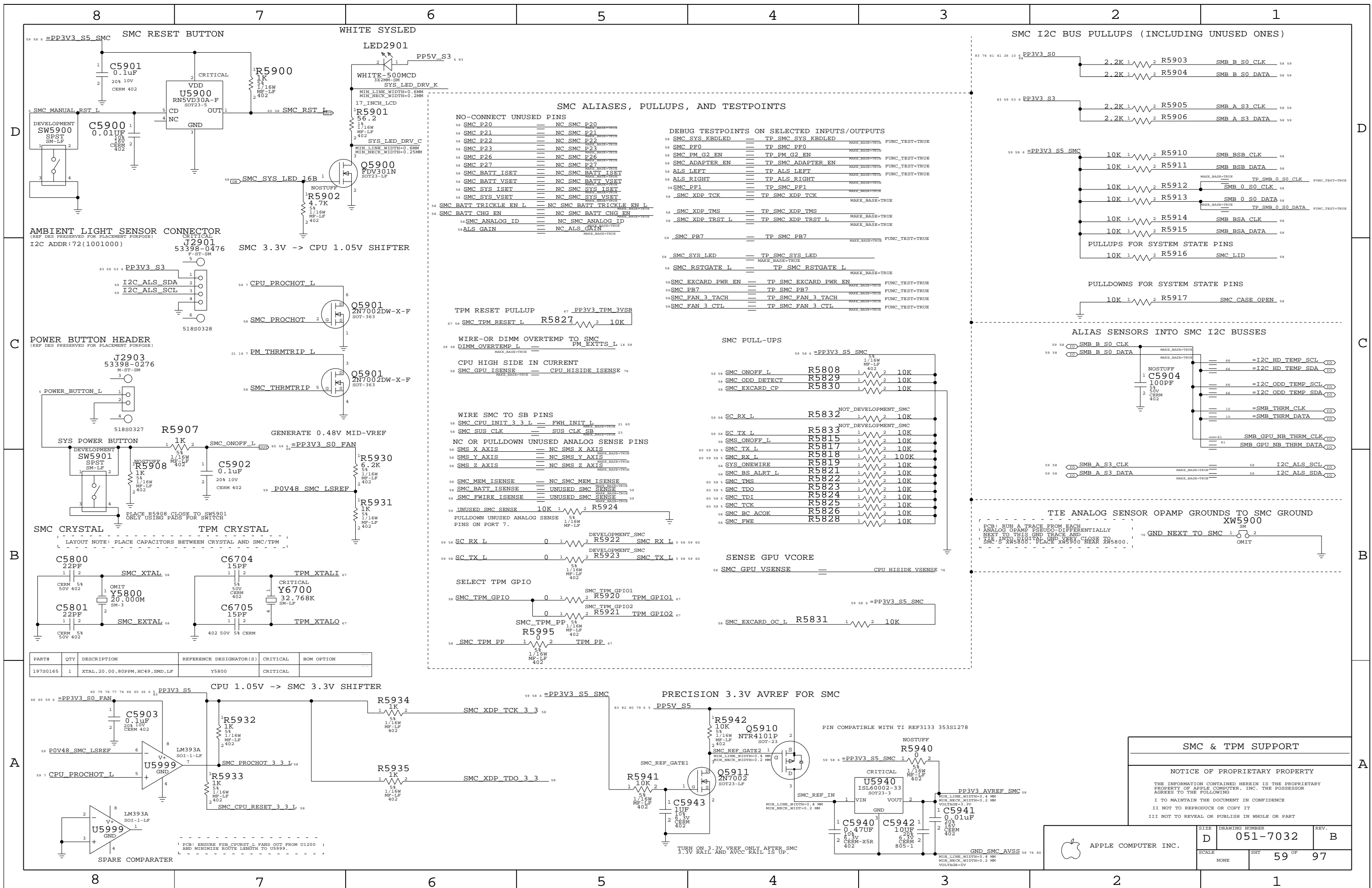
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### SMC ALIASES, PULLUPS, AND TESTPOINTS

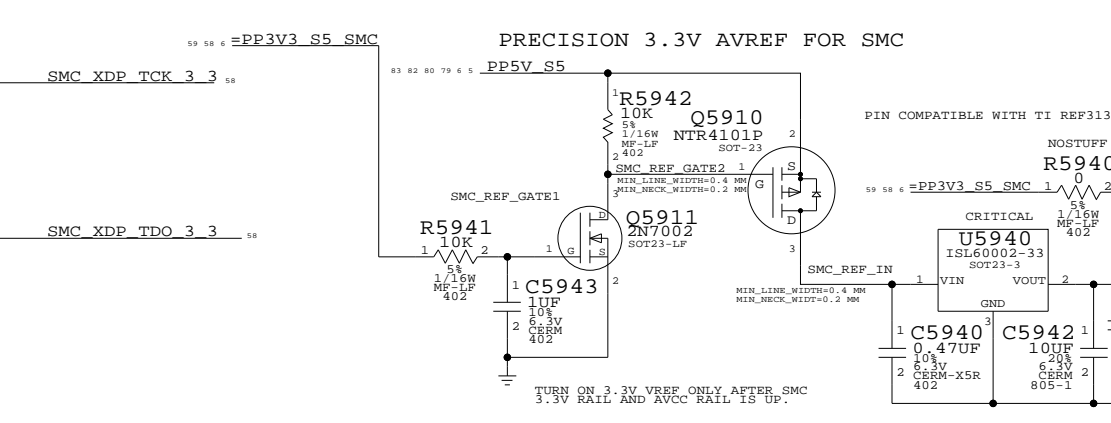
NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC PM_G2_EN == TP_PM_G2_EN MAKE_BASE=TRUE
58 SMC P23 == NC SMC P23	58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P26 == NC SMC P26	58 ALS_LEFT == TP_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P27 == NC SMC P27	58 ALS_RIGHT == TP_ALS_RIGHT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_ISET == NC_SMC_BATT_ISET MAKE_BASE=TRUE	58 SMC_PFI == TP_SMC_PFI MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC_SMC_BATT_VSET MAKE_BASE=TRUE	58 SMC_XDP_TCK == TP_SMC_XDP_TCK MAKE_BASE=TRUE
58 SMC_SYS_ISET == NC_SMC_SYS_ISET MAKE_BASE=TRUE	58 SMC_XDP_TMS == TP_SMC_XDP_TMS MAKE_BASE=TRUE
58 SMC_SYS_VSET == NC_SMC_SYS_VSET MAKE_BASE=TRUE	58 SMC_XDP_TRST_L == TP_SMC_XDP_TRST_L MAKE_BASE=TRUE
58 SMC_BATT_TRICKLE_EN_L == NC_SMC_BATT_TRICKLE_EN_L MAKE_BASE=TRUE	59 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_CHG_EN == NC_SMC_BATT_CHG_EN MAKE_BASE=TRUE	58 SMC_SYS_LED == TP_SMC_SYS_LED MAKE_BASE=TRUE
58 SMC_ANALOG_ID == NC_SMC_ANALOG_ID MAKE_BASE=TRUE	58 SMC_RSTGATE_L == TP_SMC_RSTGATE_L MAKE_BASE=TRUE
58 ALS_GAIN == NC_ALS_GAIN MAKE_BASE=TRUE	58 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL MAKE_BASE=TRUE FUNC_TEST=TRUE

### SMC PULL-UPS

58 SMC_ONOFF_L	R5808	10K
58 SMC_ODD_DETECT	R5829	10K
58 SMC_EXCARD_CP	R5830	10K
58 SC_RX_L	R5832	10K
58 SC_TX_L	R5833	10K
58 SMS_ONOFF_L	R5815	10K
58 SMC_TX_L	R5817	10K
58 SMC_RX_L	R5818	100K
58 SYS_ONWIRE	R5819	10K
58 SMC_BS_ALERT_L	R5821	10K
58 SMC_TMS	R5822	10K
58 SMC_TDO	R5823	10K
58 SMC_TDI	R5824	10K
58 SMC_TCK	R5825	10K
58 SMC_BC_ACOK	R5826	10K
58 SMC_FWE	R5828	10K

### WIRE SMC TO SB PINS

58 SMC_CPU_INIT_3_3_L	FWH_INIT_L	21
58 SMC_SUS_CLK	SUS_CLK_SB	23
58 SMC_TPM_GPIO	SMC_TPM_GPIO1	67
58 SMC_TPM_PP	SMC_TPM_PP	67



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND  
 XW5900  
 PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

**SMC & TPM SUPPORT**

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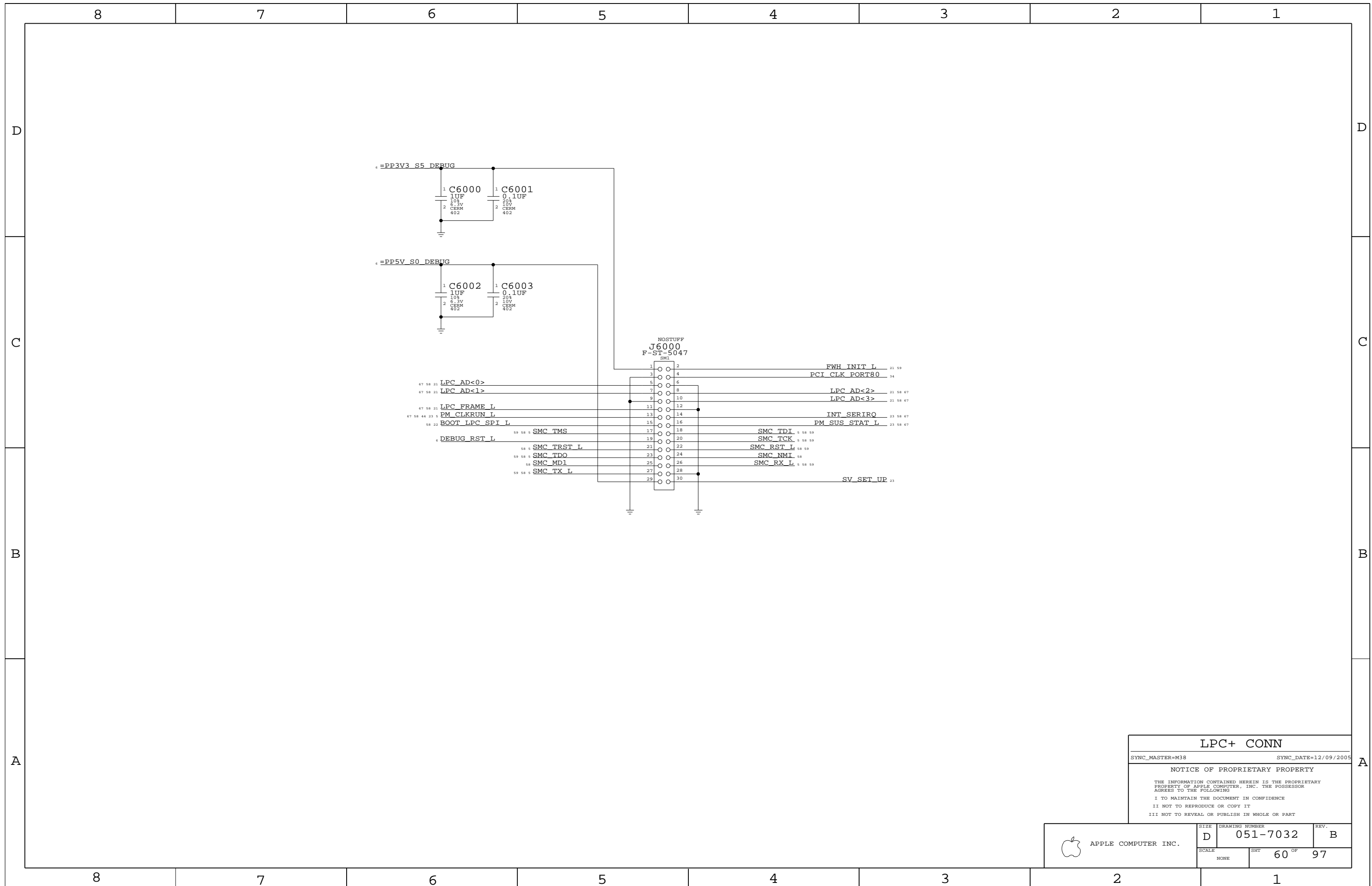
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SCALE	SHT	59 OF 97
NONE		



**LPC+ CONN**

SYNC\_MASTER=M38 SYNC\_DATE=12/09/2005

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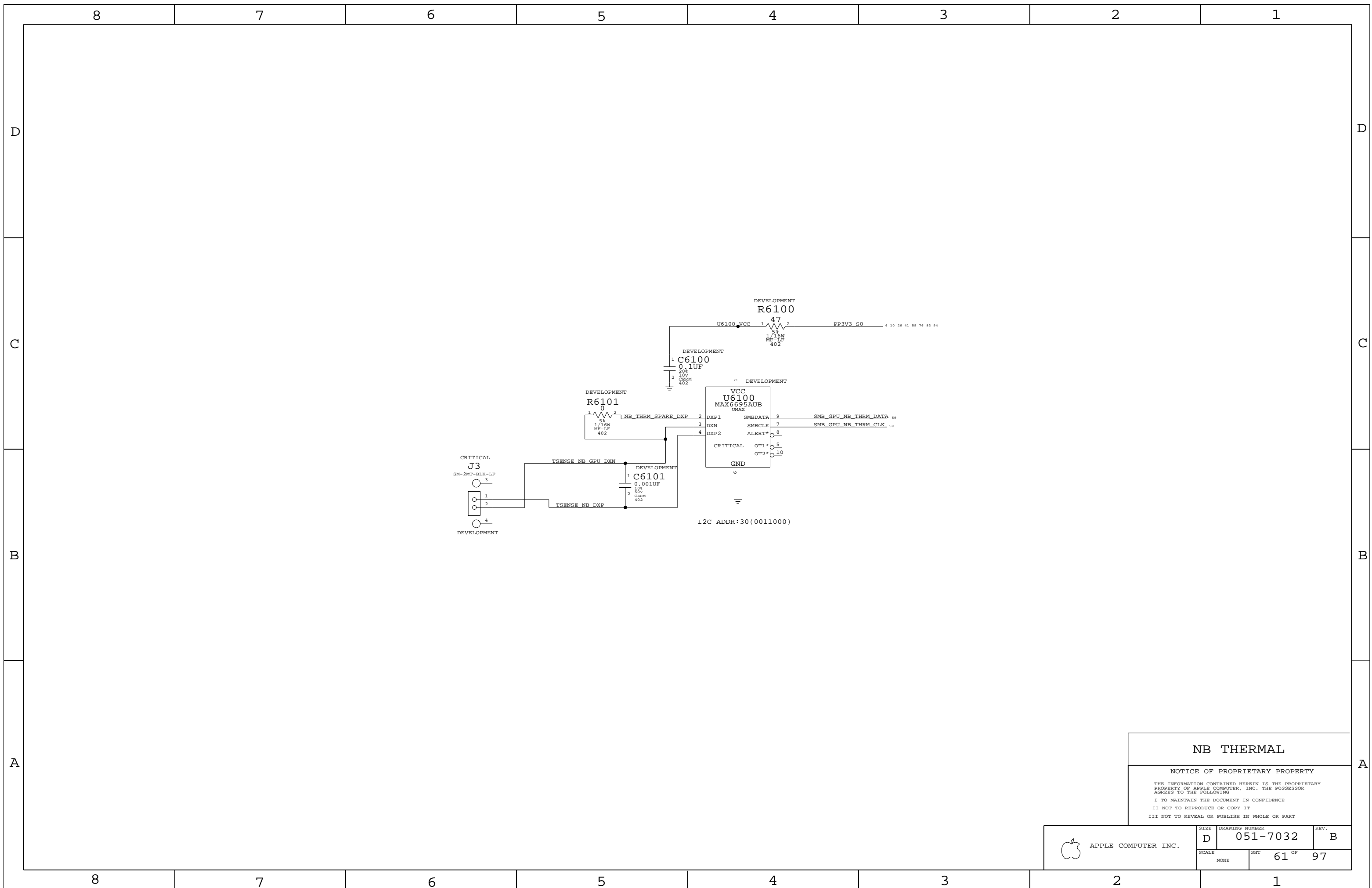
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHIT 60 OF 97	

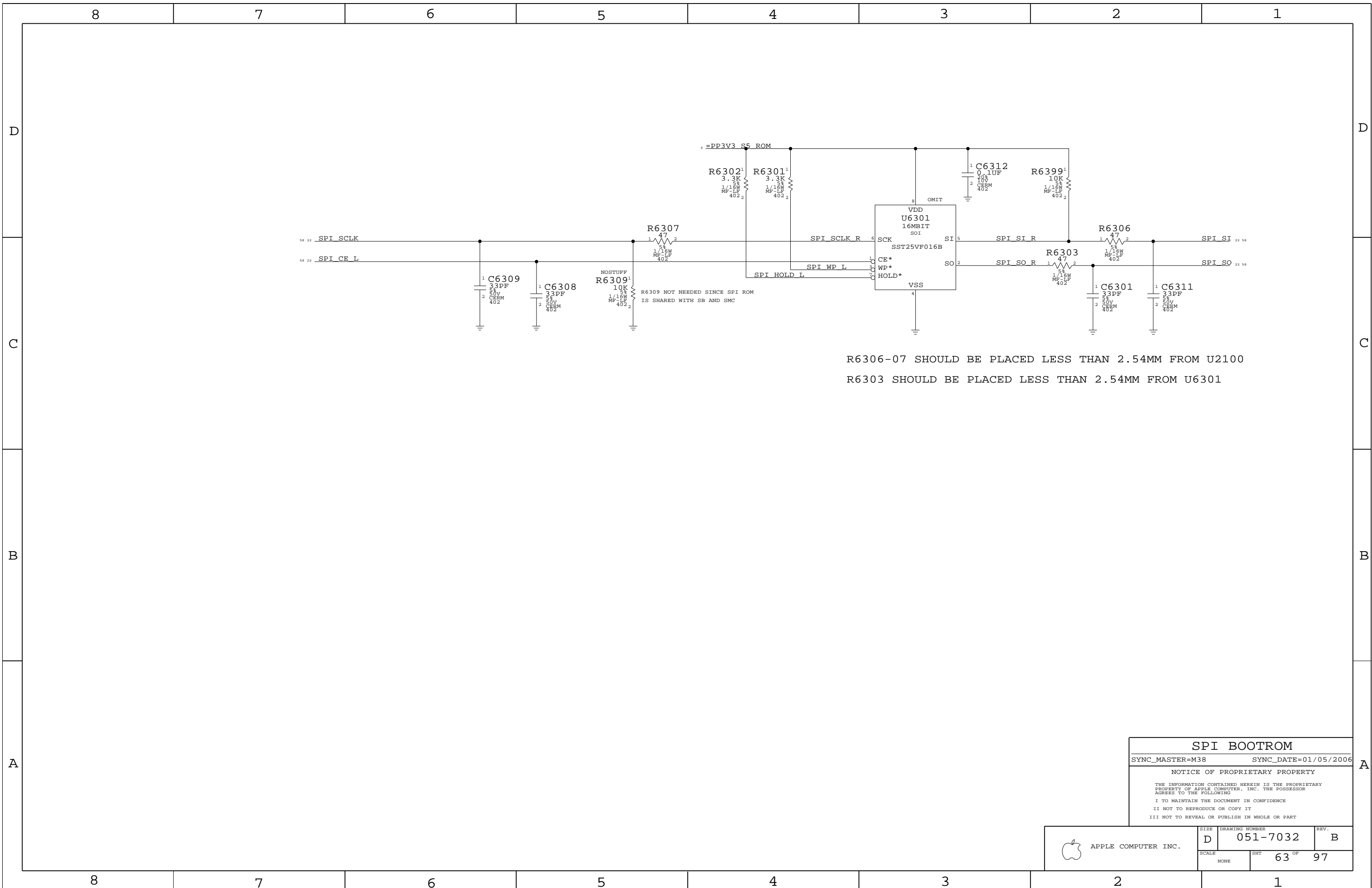


**NB THERMAL**

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHIT 61 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100  
R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

**SPI BOOTROM**  
 SYNC\_MASTER=M38      SYNC\_DATE=01/05/2006

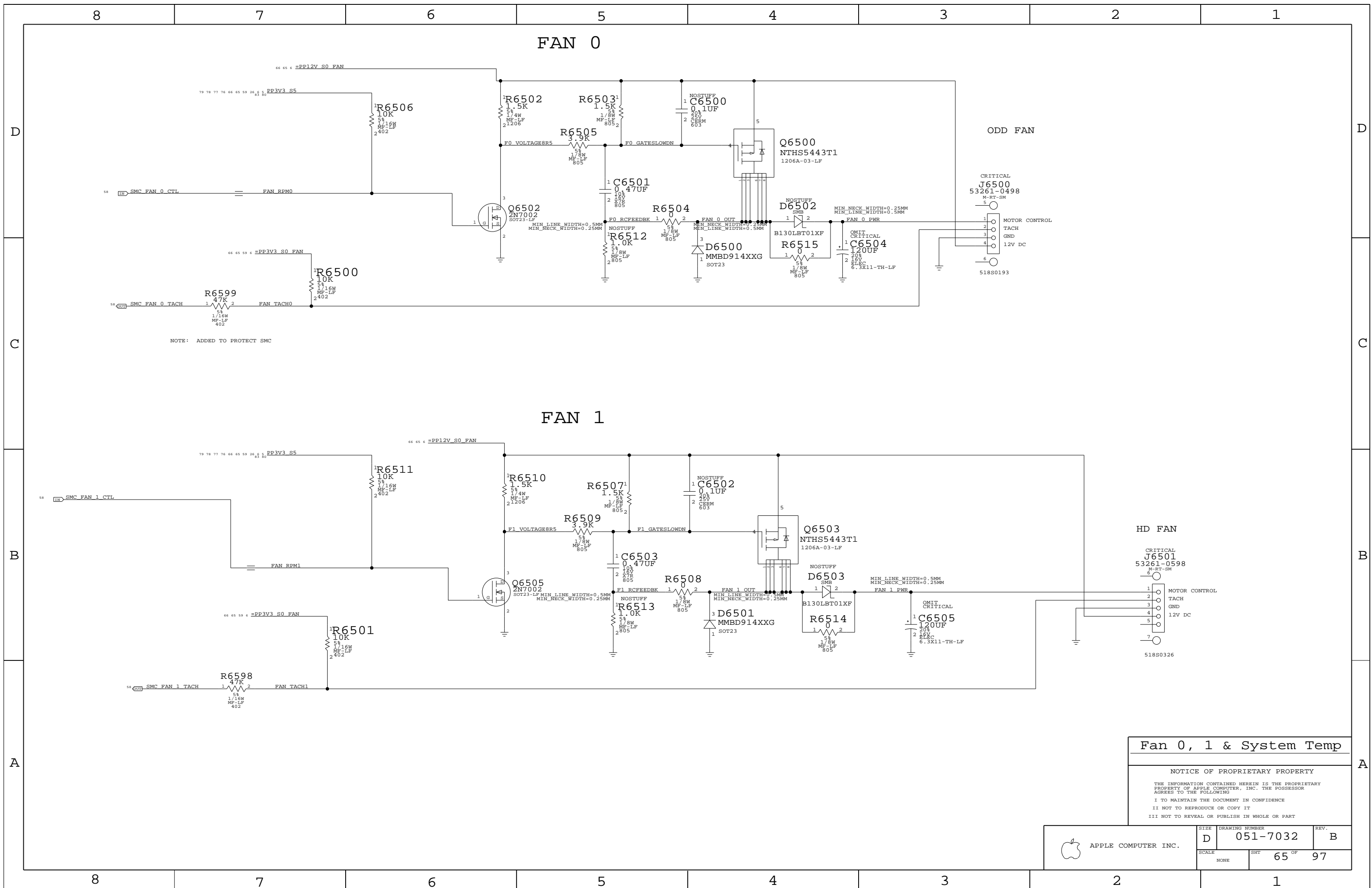
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	D	051-7032	B
SCALE	SHT		OF
NONE	63		97



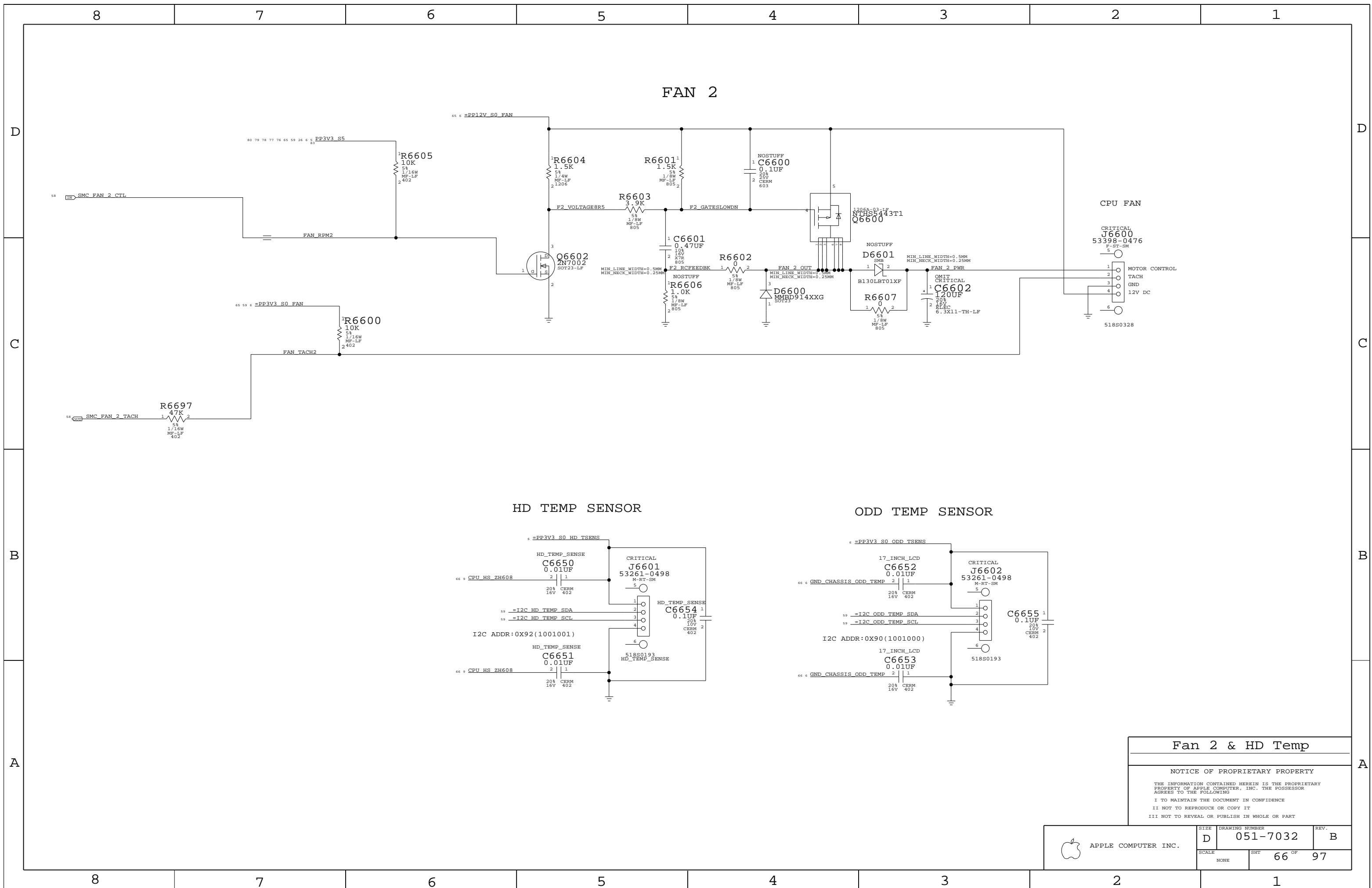


NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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	SCALE NONE	SHEET <b>65</b> OF <b>97</b>	



FAN 2

HD TEMP SENSOR

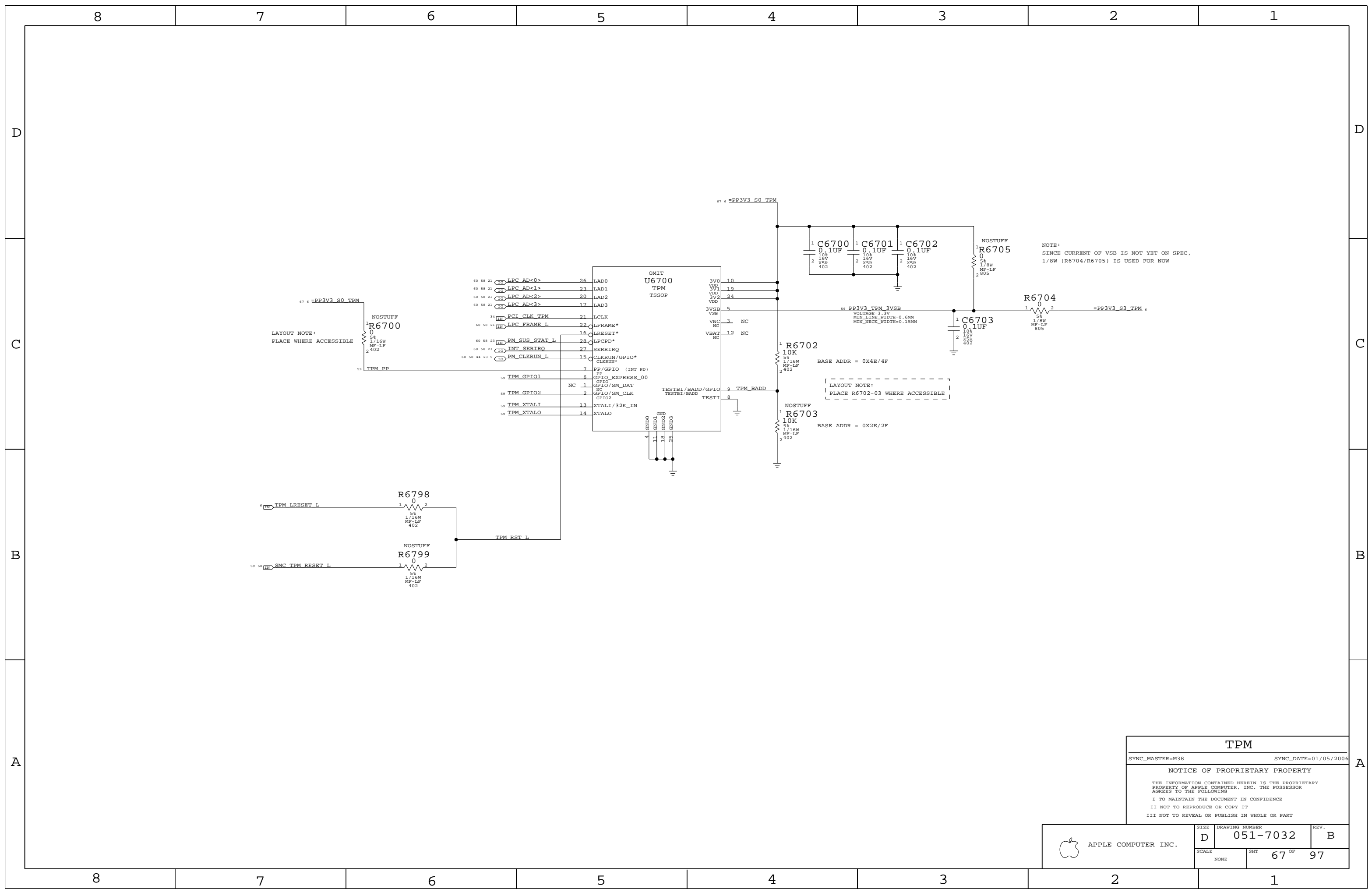
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	66 OF	97
NONE			



LAYOUT NOTE:  
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:  
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:  
SINCE CURRENT OF VSB IS NOT YET ON SPEC,  
1/8W (R6704/R6705) IS USED FOR NOW

**TPM**

SYNC\_MASTER=M38      SYNC\_DATE=01/05/2006


**NOTICE OF PROPRIETARY PROPERTY**

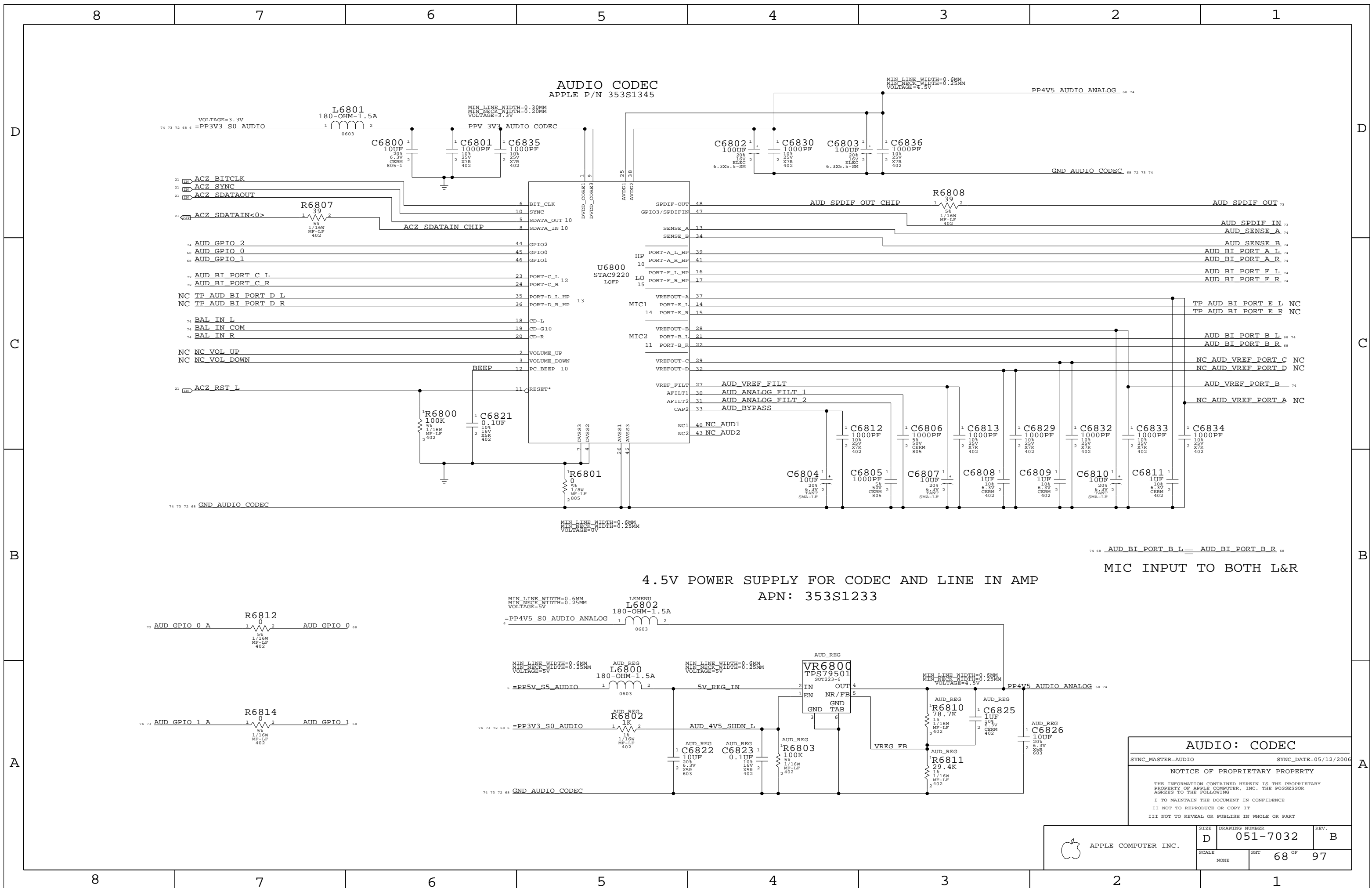
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	D	051-7032	B
SCALE	SHT	67 OF 97	
NONE			

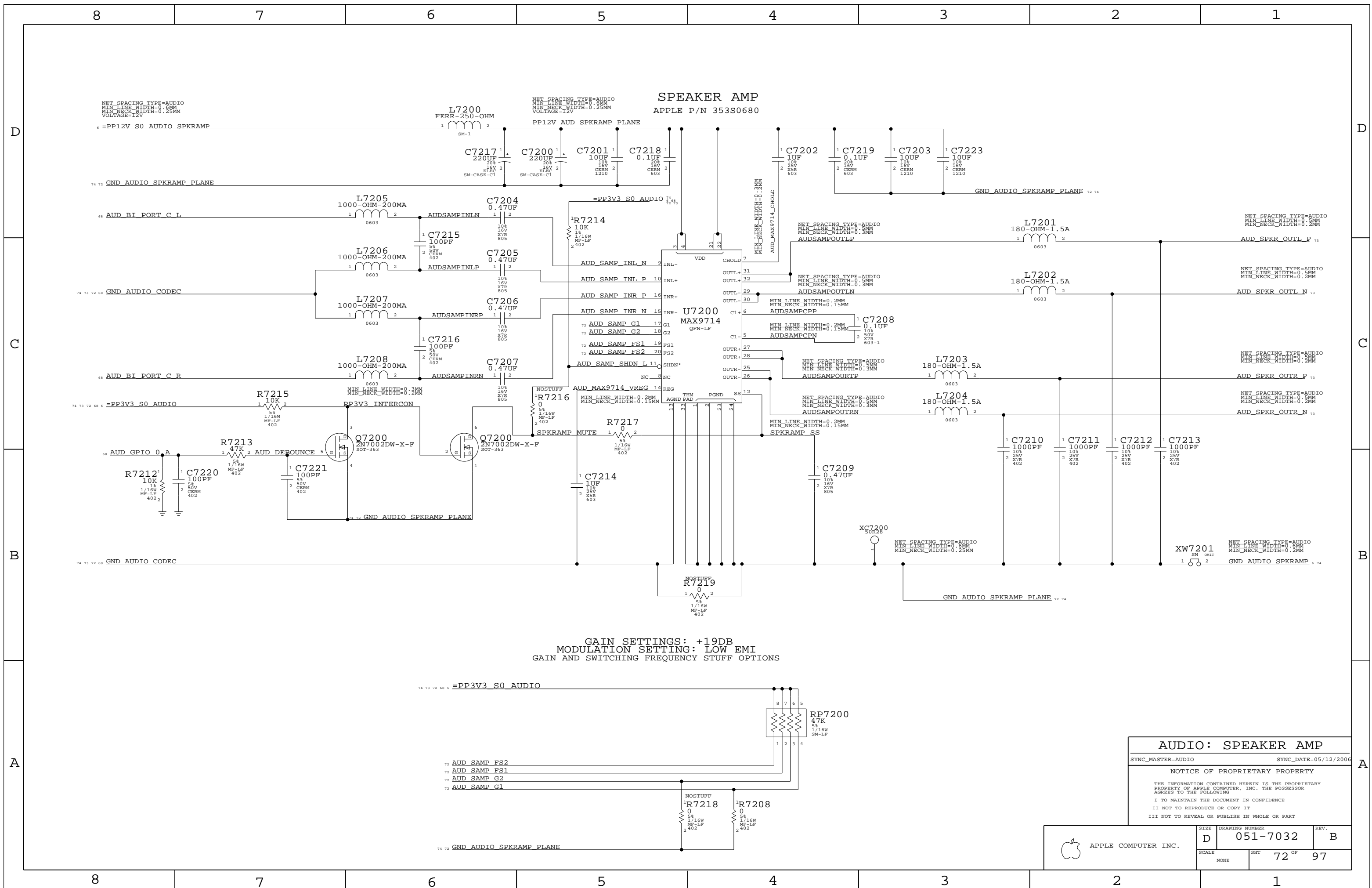


**AUDIO CODEC**  
APPLE P/N 353S1345

**4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP**  
APN: 353S1233

**AUDIO: CODEC**  
 SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006  
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	SCALE NONE	SHEET <b>68</b> OF <b>97</b>	



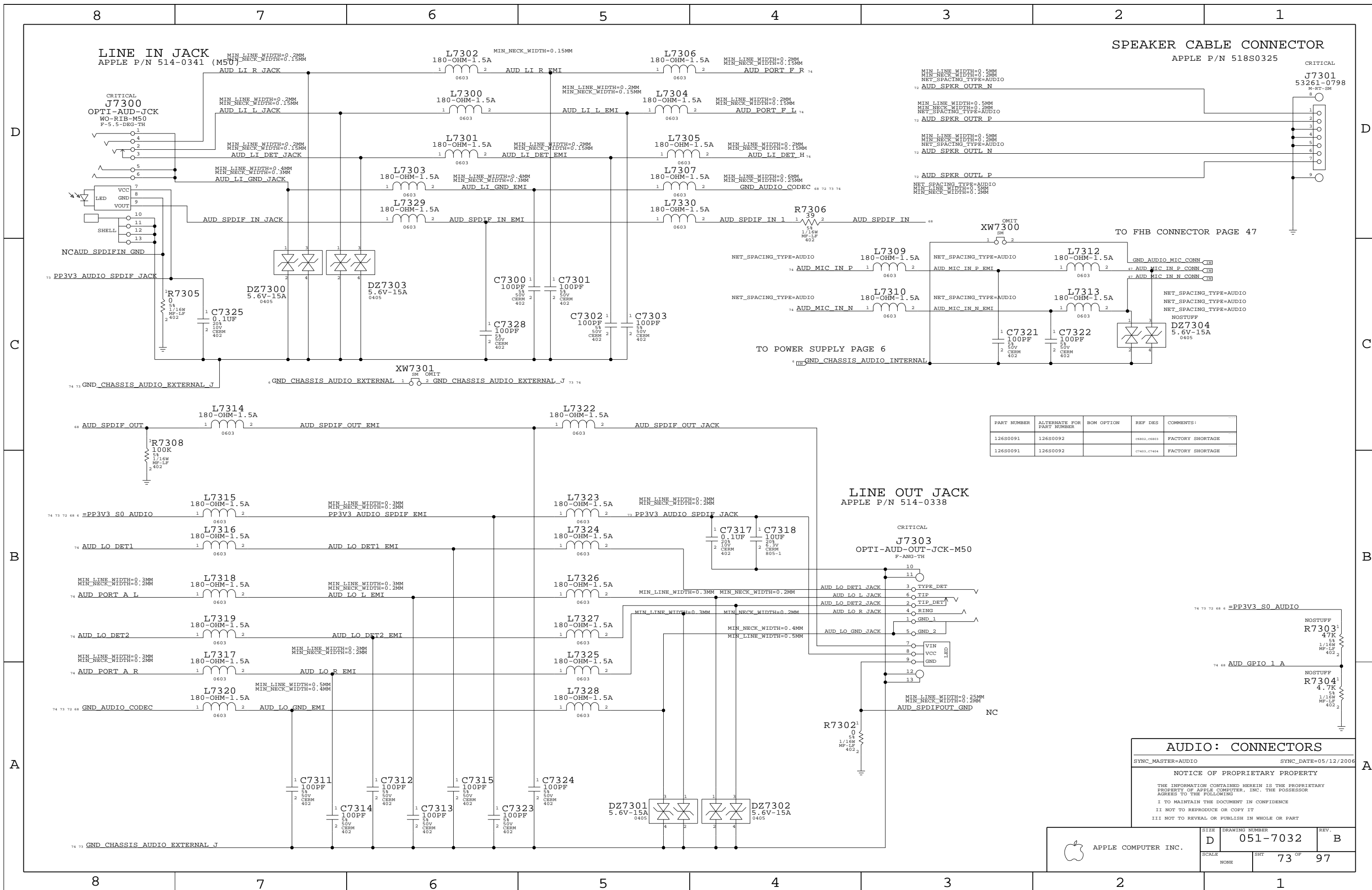
GAIN SETTINGS: +19DB  
 MODULATION SETTING: LOW EMI  
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

**AUDIO: SPEAKER AMP**  
 SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006  
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	D	051-7032	B
SCALE	SHT	72 OF	97
NONE			

**LINE IN JACK**  
APPLE P/N 514-0341 (M50)

**SPEAKER CABLE CONNECTOR**  
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

**LINE OUT JACK**  
APPLE P/N 514-0338

**AUDIO: CONNECTORS**

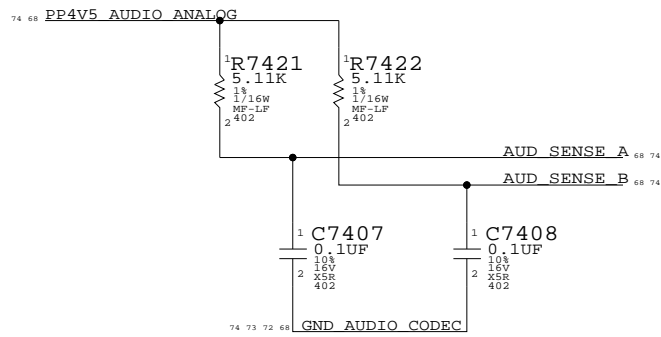
SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	73 OF	97
NONE			

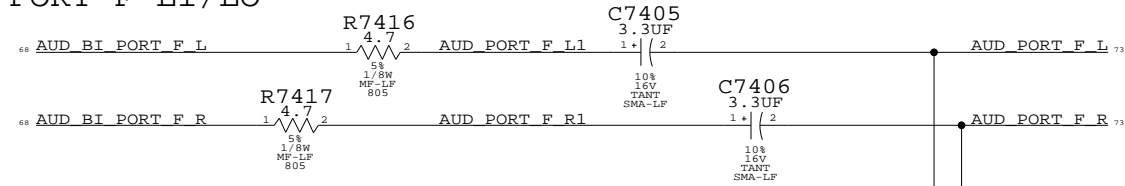
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



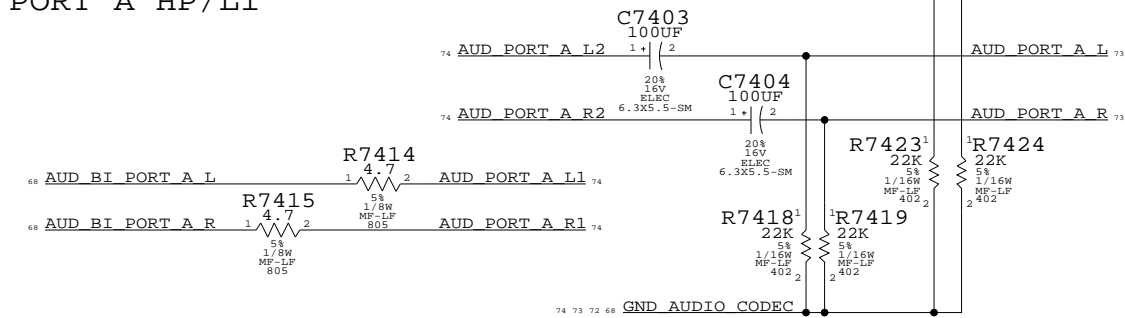
USED PORTS  
 PORT A HP/LI  
 PORT B MIC IN  
 PORT C BI SPEAKERS  
 PORT F LI/LO

UNUSED PORTS  
 PORT E  
 PORT D

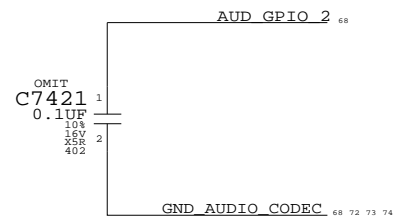
PORT F LI/LO



PORT A HP/LI

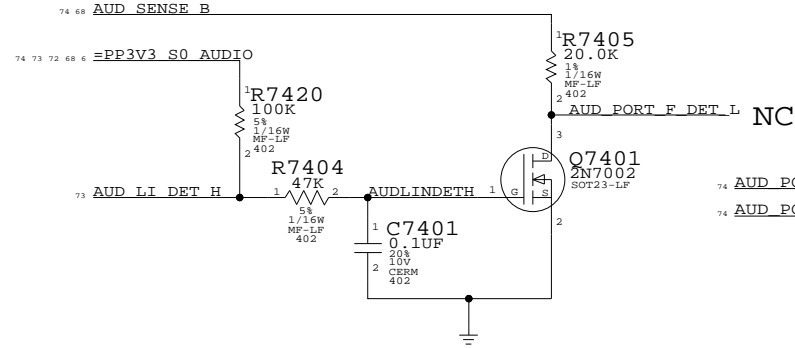


UNUSED PORT TERMINATION

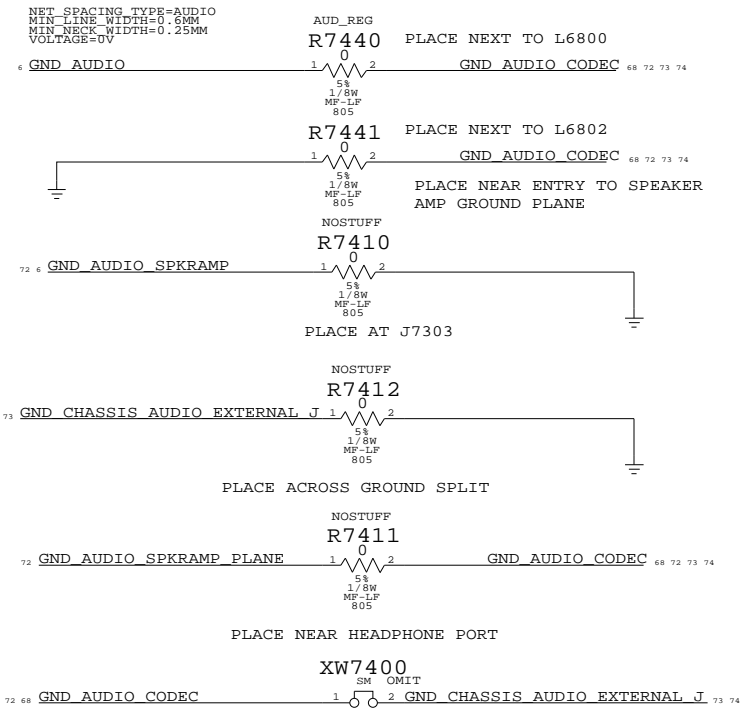


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

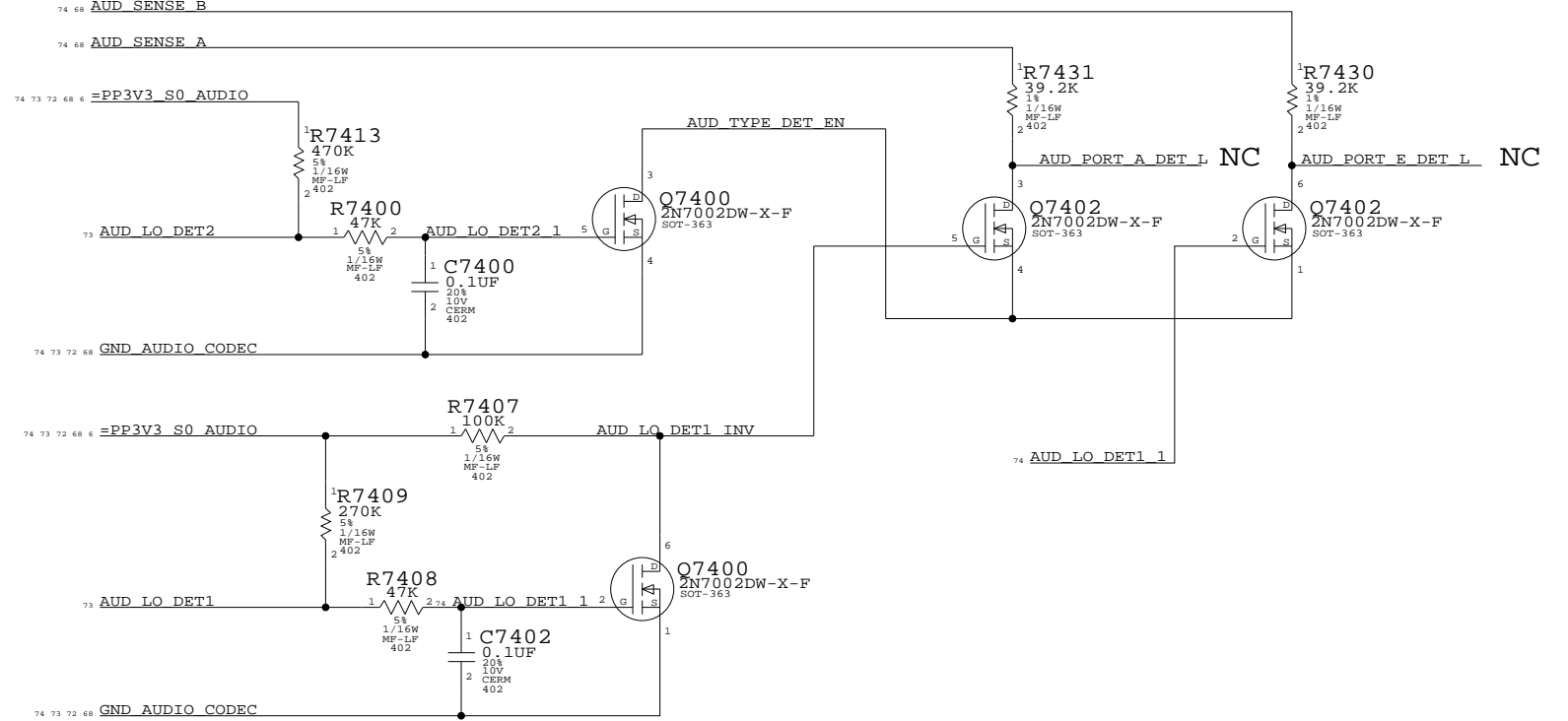
PORT F (LI) PLUG DETECT



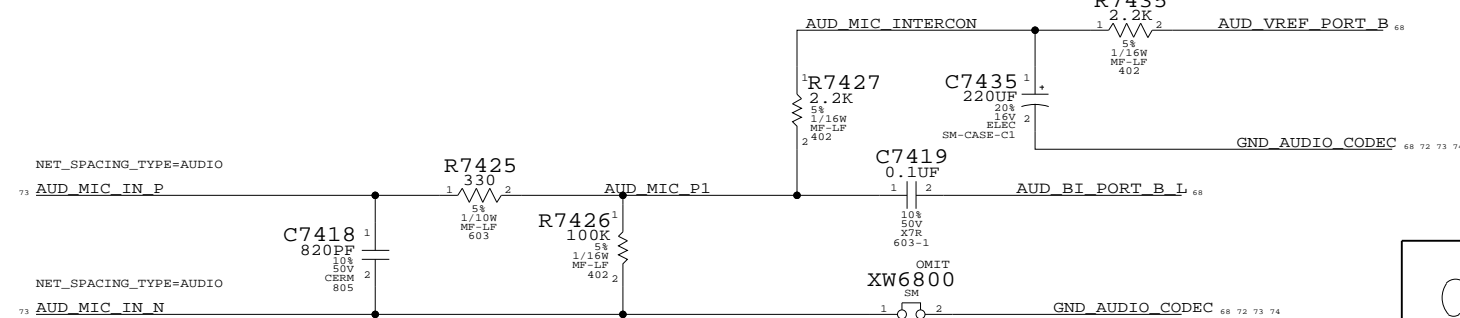
AUDIO GROUND RETURNS



PORT A/H (LO/DIG\_OUT) PLUG DETECT (E TELLS H TO COME ON)



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006

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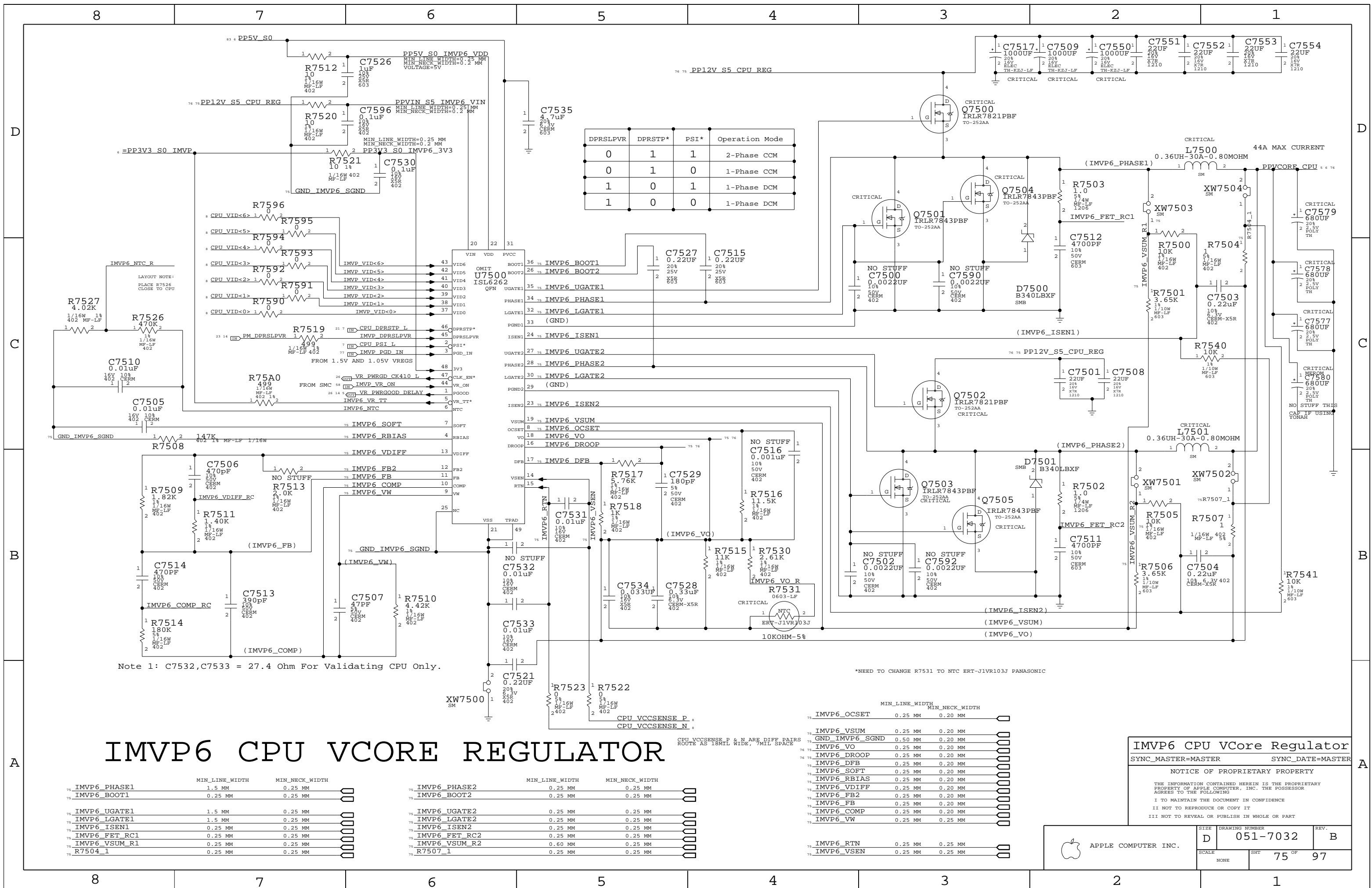
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	D	051-7032	B
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Pin	Signal
36	IMVP6_BOOT1
26	IMVP6_BOOT2
35	IMVP6_UGATE1
34	IMVP6_PHASE1
32	IMVP6_LGATE1
33	(GND)
24	IMVP6_ISEN1
27	IMVP6_UGATE2
28	IMVP6_PHASE2
30	IMVP6_LGATE2
29	(GND)
23	IMVP6_ISEN2
19	IMVP6_VSUM
8	IMVP6_OCSET
18	IMVP6_VO
16	IMVP6_DROOP
17	IMVP6_DFB
14	VSEN
15	RTN
21	IMVP6_RTN
49	IMVP6_VSEN
75	IMVP6_VSEN
75	IMVP6_VO
75	IMVP6_VO_R
75	IMVP6_VSUM
75	IMVP6_VO

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

\*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

# IMVP6 CPU VCore Regulator

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75	IMVP6_PHASE1	1.5 MM	0.25 MM
75	IMVP6_BOOT1	0.25 MM	0.25 MM
75	IMVP6_UGATE1	1.5 MM	0.25 MM
75	IMVP6_LGATE1	1.5 MM	0.25 MM
75	IMVP6_ISEN1	0.25 MM	0.25 MM
75	IMVP6_FET_RC1	0.25 MM	0.25 MM
75	IMVP6_VSUM_R1	0.25 MM	0.25 MM
75	R7504_1	0.25 MM	0.25 MM

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75	IMVP6_PHASE2	0.25 MM	0.25 MM
75	IMVP6_BOOT2	0.25 MM	0.25 MM
75	IMVP6_UGATE2	0.25 MM	0.25 MM
75	IMVP6_LGATE2	0.25 MM	0.25 MM
75	IMVP6_ISEN2	0.25 MM	0.25 MM
75	IMVP6_FET_RC2	0.25 MM	0.25 MM
75	IMVP6_VSUM_R2	0.60 MM	0.25 MM
75	R7507_1	0.25 MM	0.25 MM

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75	IMVP6_OCSET	0.25 MM	0.20 MM
75	IMVP6_VSUM	0.25 MM	0.20 MM
75	GND_IMVP6_SGND	0.50 MM	0.20 MM
75	IMVP6_VO	0.25 MM	0.20 MM
75	IMVP6_DROOP	0.25 MM	0.20 MM
75	IMVP6_DFB	0.25 MM	0.20 MM
75	IMVP6_SOFT	0.25 MM	0.20 MM
75	IMVP6_RBIAS	0.25 MM	0.20 MM
75	IMVP6_VDIFF	0.25 MM	0.20 MM
75	IMVP6_FB2	0.25 MM	0.20 MM
75	IMVP6_FB	0.25 MM	0.20 MM
75	IMVP6_COMP	0.25 MM	0.20 MM
75	IMVP6_VW	0.25 MM	0.25 MM
75	IMVP6_RTN	0.25 MM	0.25 MM
75	IMVP6_VSEN	0.25 MM	0.25 MM

## IMVP6 CPU VCore Regulator

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

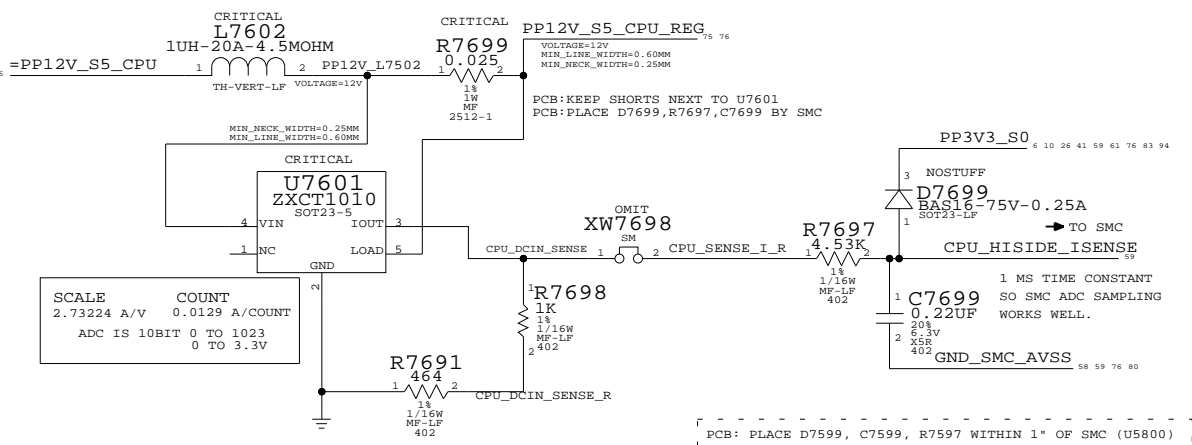
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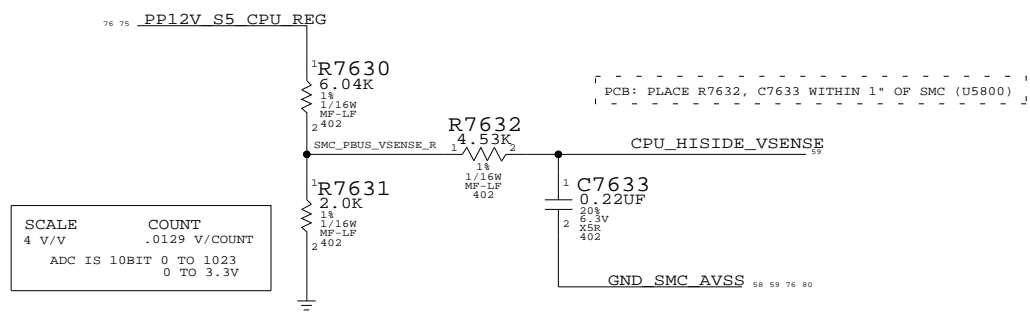
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7032	REV.: B
	SCALE: NONE	SHEET: 75 OF 97	



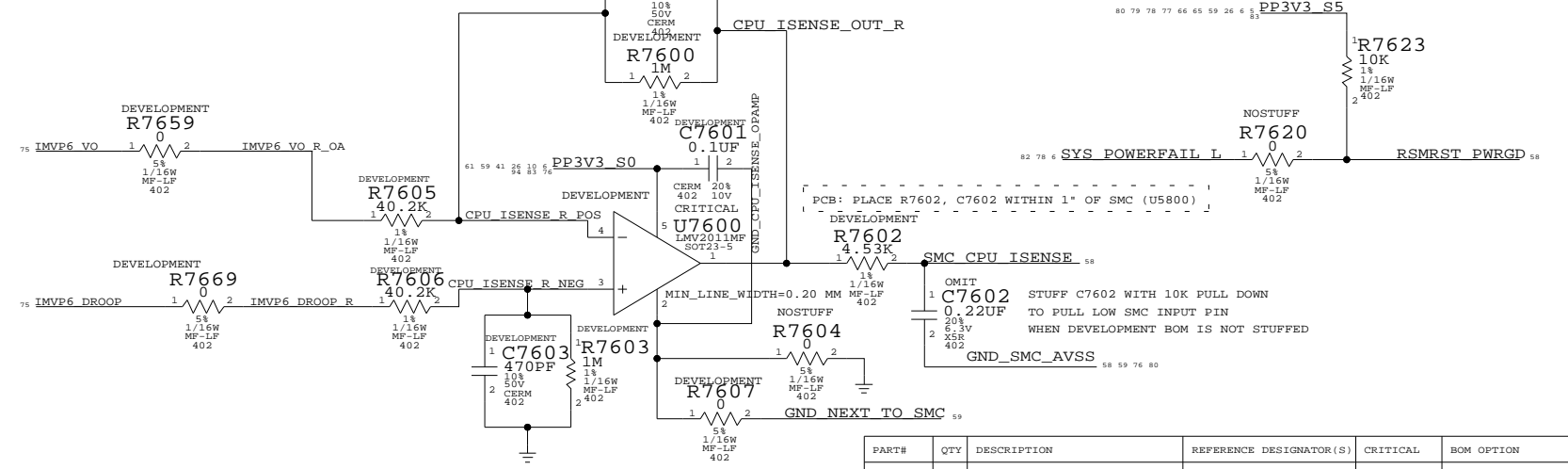
**PROCESSOR VCORE CURRENT SENSE**  
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



**PROCESSOR DCIN VOLTAGE SENSE**  
(SCALING 12V INPUT VOLTAGE TO SMC)

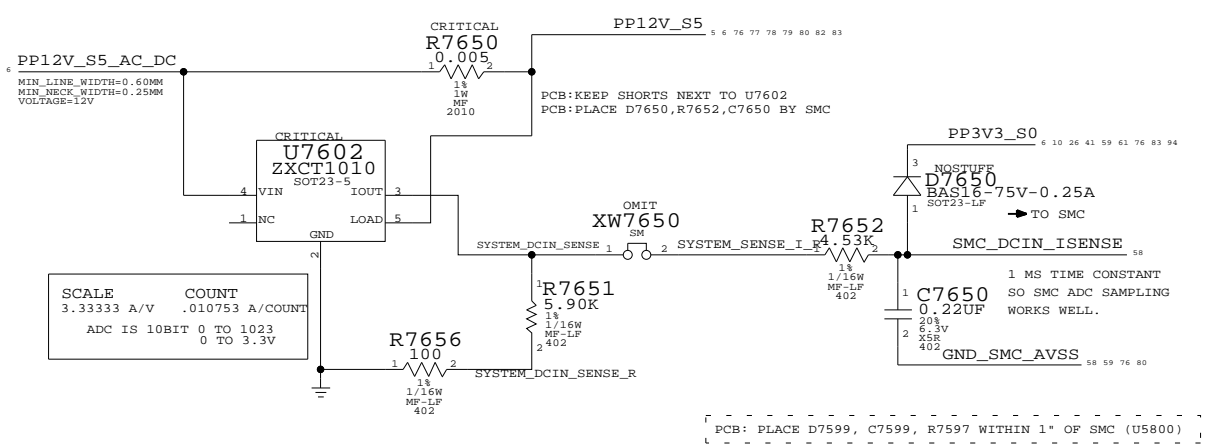


**PROCESSOR VCORE CURRENT SENSE**  
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

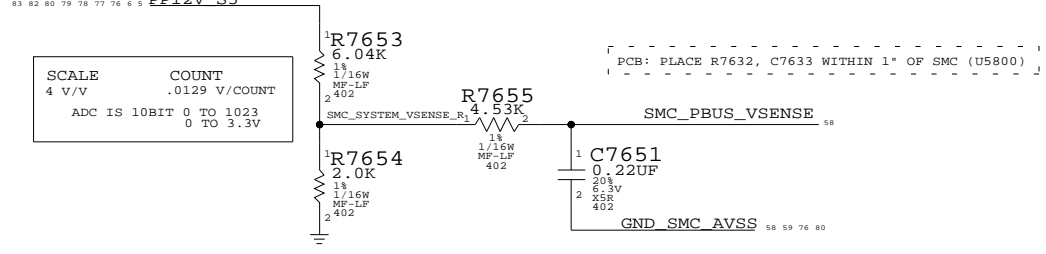


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP,0.22UF,6.3V,20%,0402	C7602		DEVELOPMENT
116S0090	1	RES,10K,5%,0402	C7602		NOT_DEVELOPMENT

**SYSTEM CURRENT SENSE**

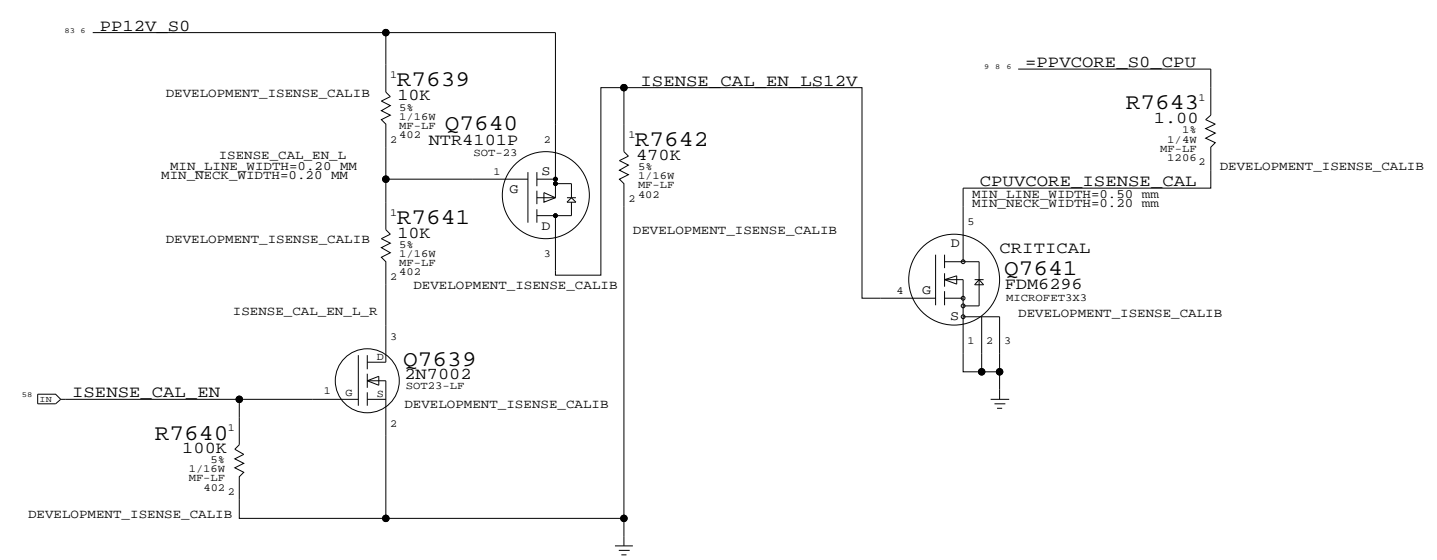


**SYSTEM VOLTAGE SENSE**  
(SCALING 12V INPUT VOLTAGE TO SMC)

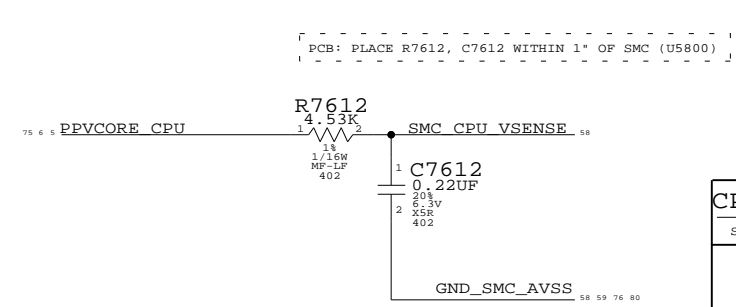


**Current Sense Calibration Circuit**

Switches in fixed load on power supplies to calibrate current sense circuits

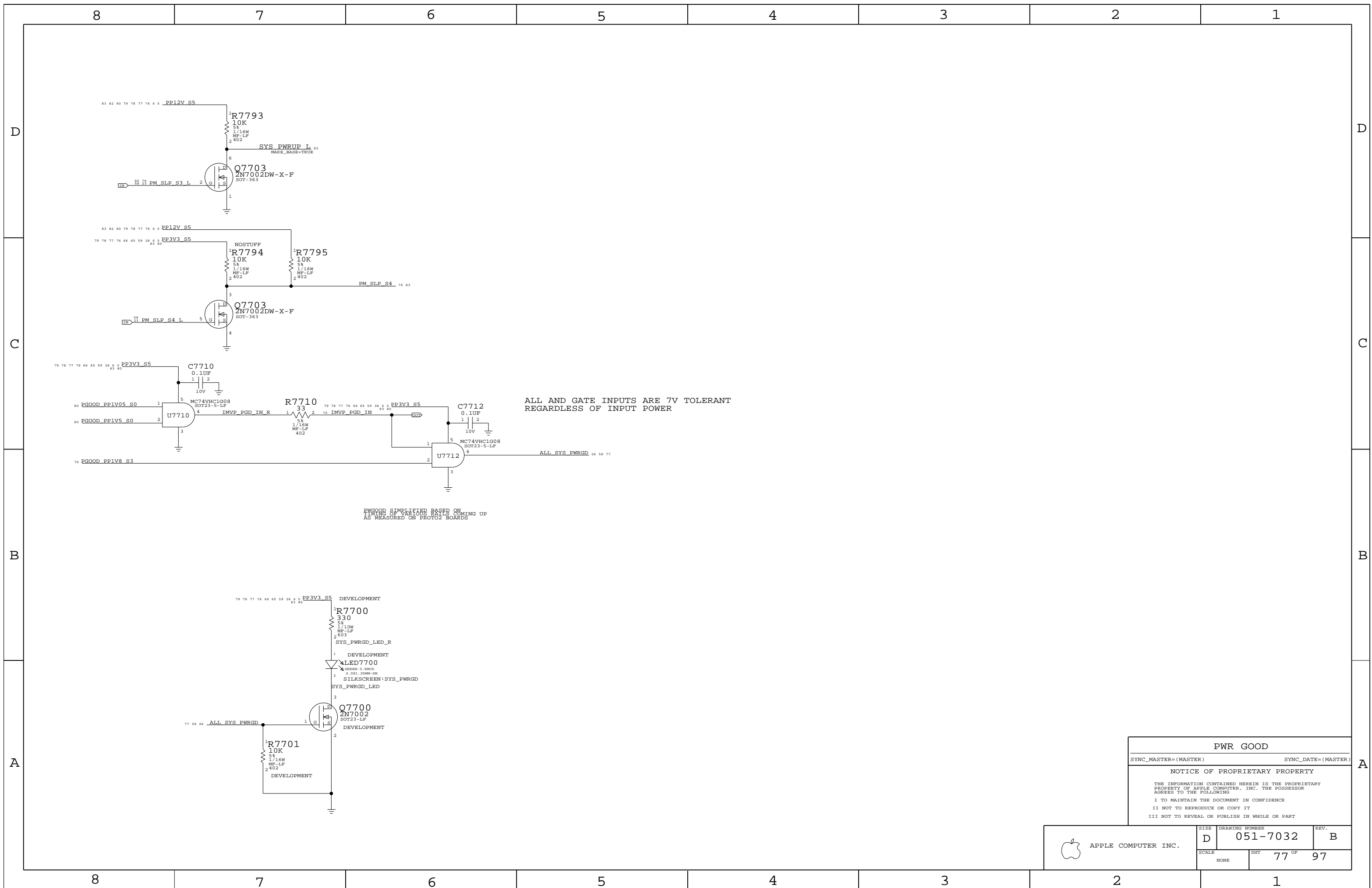


**PROCESSOR VCORE SENSE**



**CPU & SYSTEM SENSE CIRCUITRIES**

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ALL AND GATE INPUTS ARE 7V TOLERANT  
REGARDLESS OF INPUT POWER

PWGOOD SIMPLIFIED BASED ON  
TIMING OF VARIOUS RAILS COMING UP  
AS MEASURED ON PROTO2 BOARDS


**PWR GOOD**

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

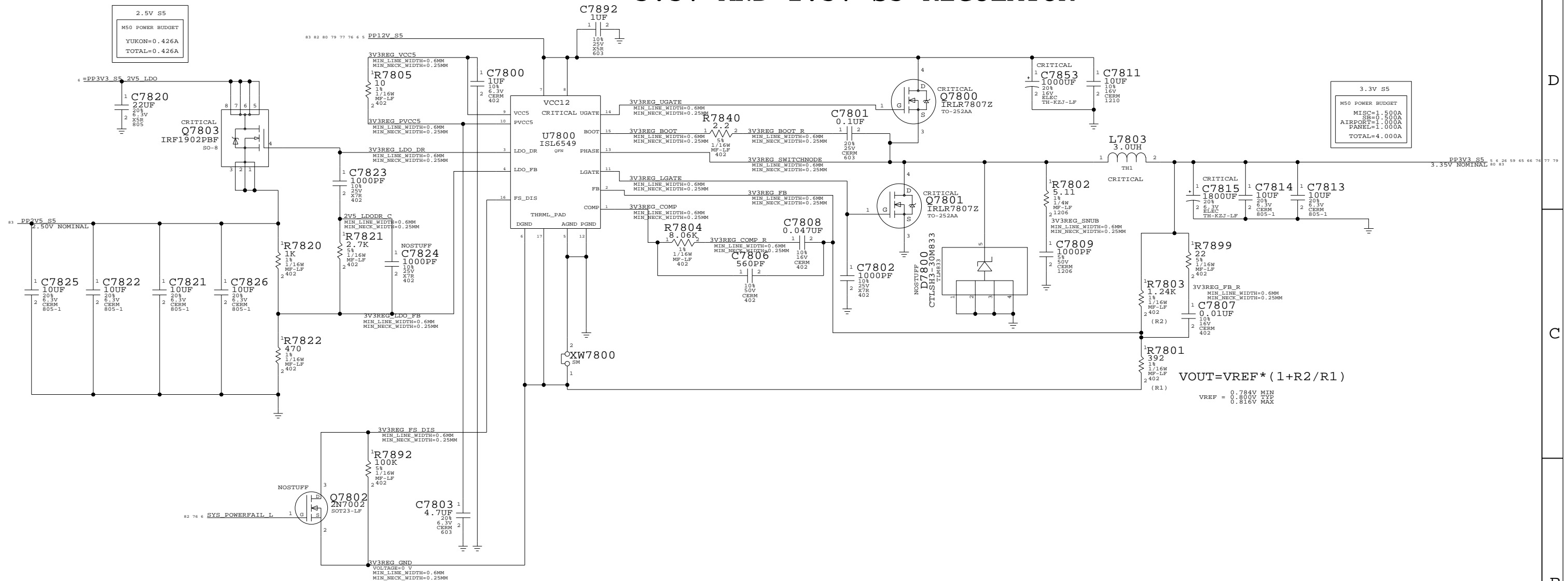
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	SCALE NONE	SHT 77 OF 97	

# 3.3V AND 2.5V S5 REGULATOR



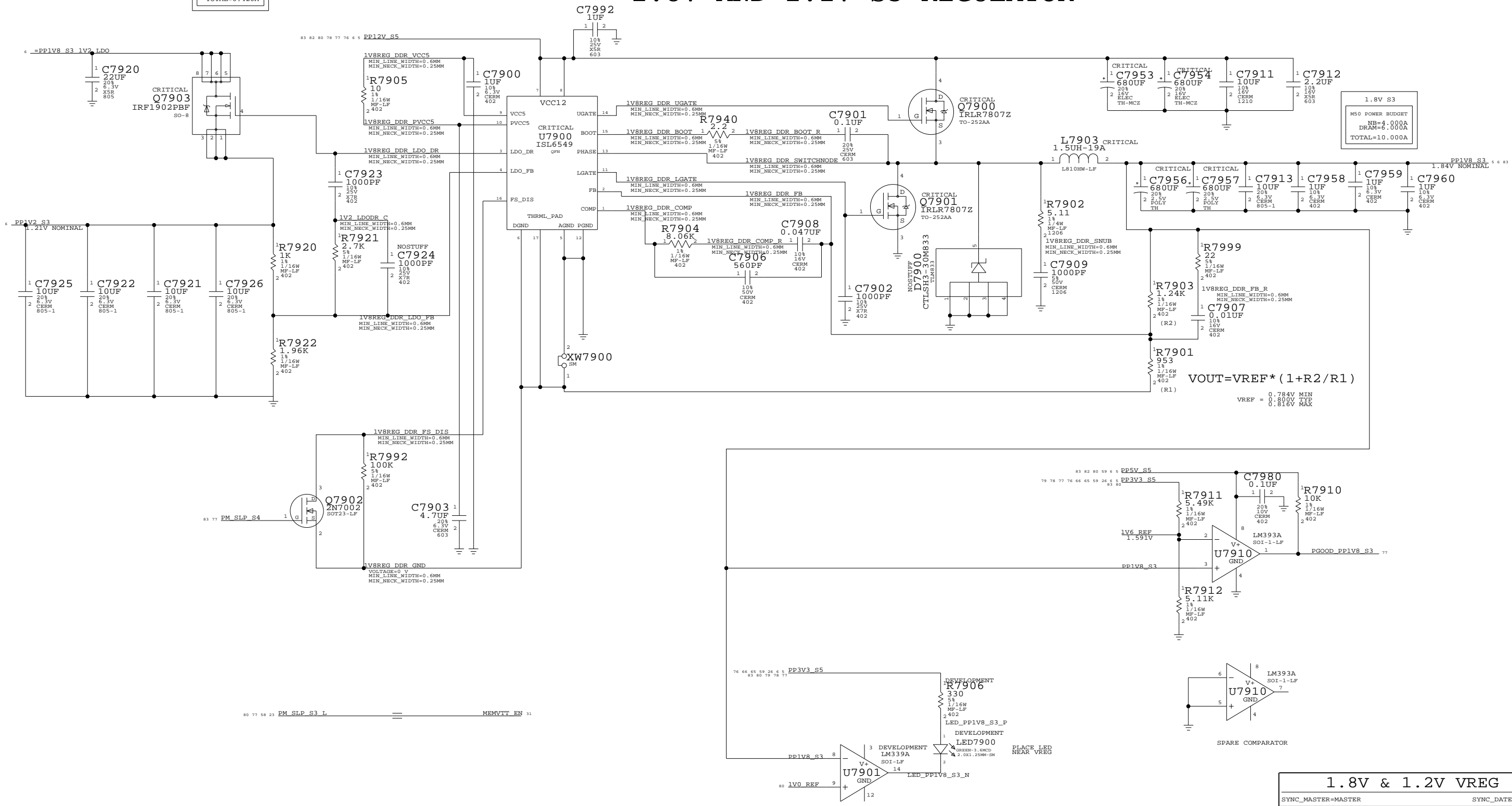
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	78 OF 97	
NONE			

TRUE 1

# 1.8V AND 1.2V S3 REGULATOR

1.2V S3  
MS0 POWER BUDGET  
YUKON=0.426A  
TOTAL=0.426A

1.8V S3  
MS0 POWER BUDGET  
NB=4.000A  
DRAM=6.000A  
TOTAL=10.000A



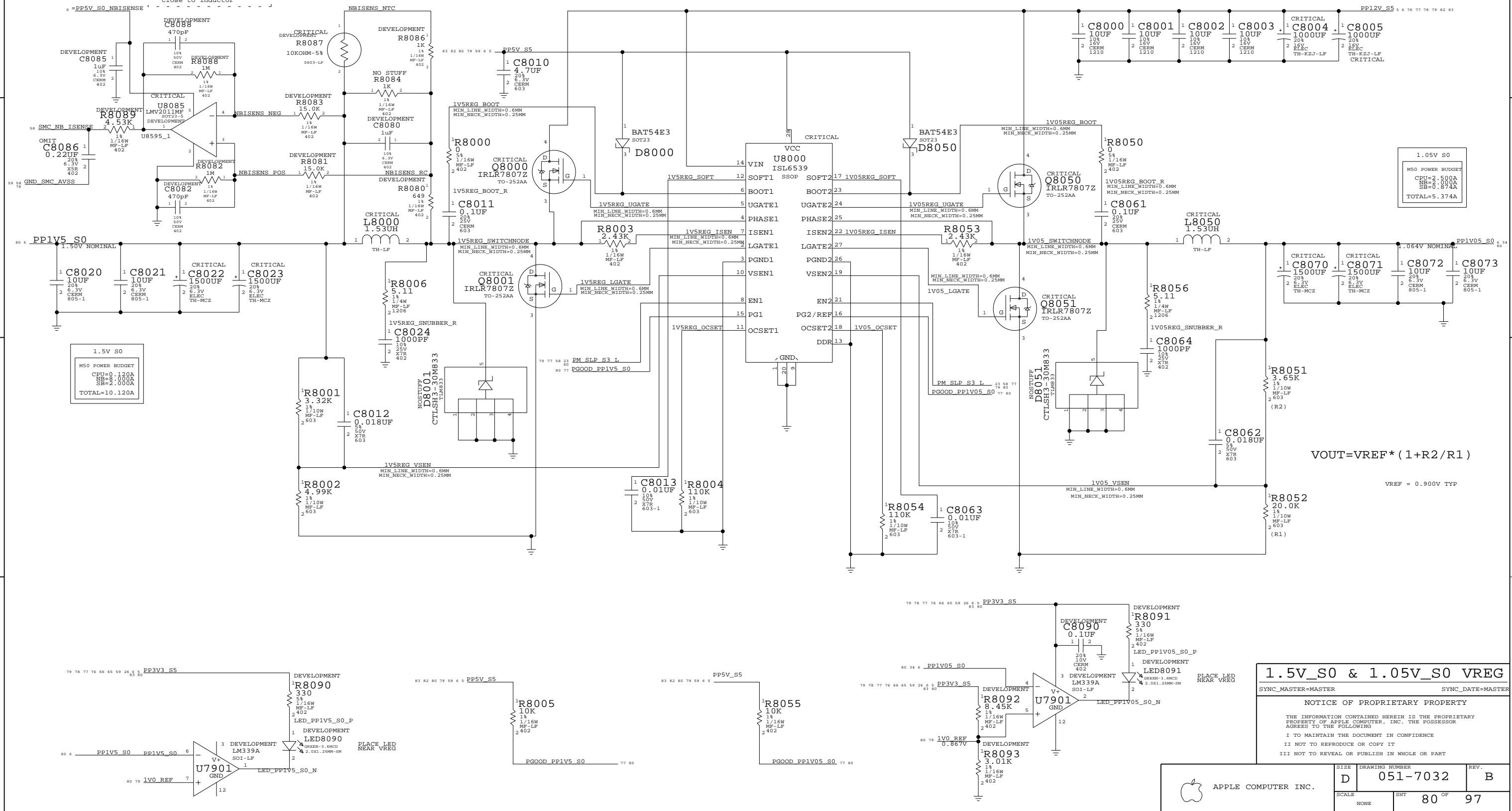
**1.8V & 1.2V VREG**  
 SYNC\_MASTER=MASTER SYNC\_DATE=MASTER  
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	D	051-7032	B
SCALE	SHT	79 OF	97
NONE			

# 1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:  
KEEP C8080, R8080,  
R8084 AND R8087  
close to inductor



1.5V S0  
M50 POWER BUDGET  
CPU=0.120A  
NB=8.0000A  
SB=2.0000A  
TOTAL=10.120A

1.05V S0  
M50 POWER BUDGET  
CPU=2.500A  
NB=2.0000A  
SB=0.874A  
TOTAL=5.374A

$$V_{OUT} = V_{REF} * (1 + R_2/R_1)$$

VREF = 0.900V TYP

## 1.5V\_S0 & 1.05V\_S0 VREG

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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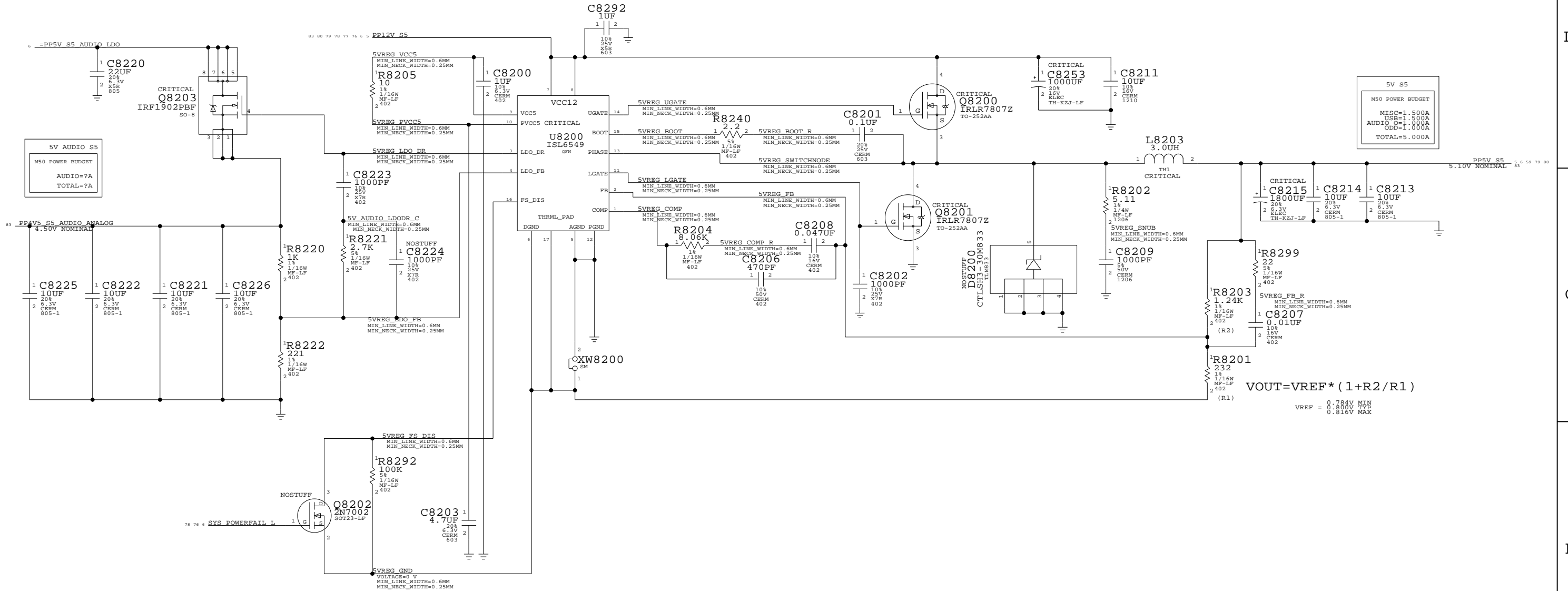
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	80 OF	97
NONE			

# 5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

## 5V DC/DC

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

### NOTICE OF PROPRIETARY PROPERTY

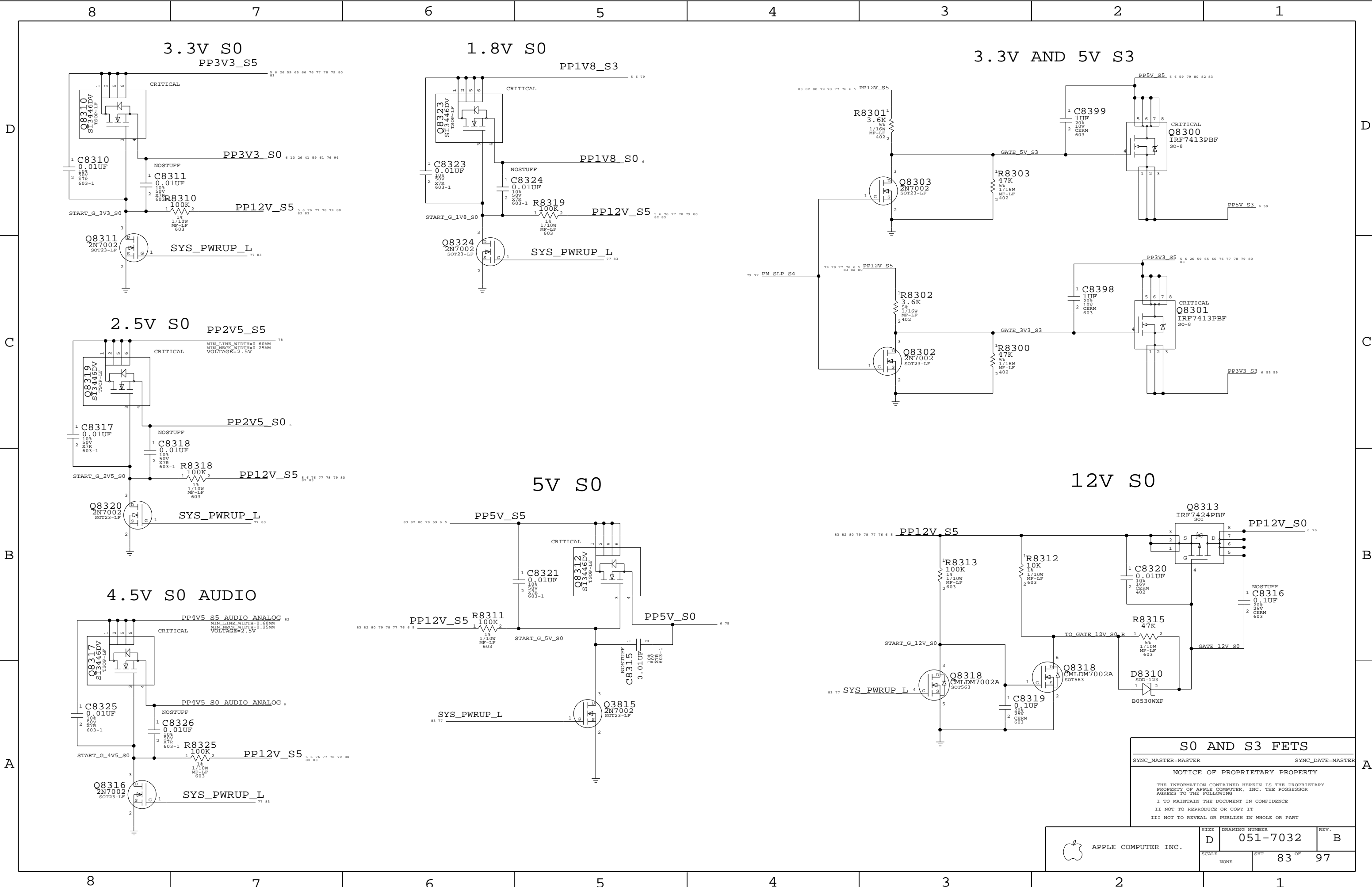
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	82 OF	97
NONE			



**S0 AND S3 FETS**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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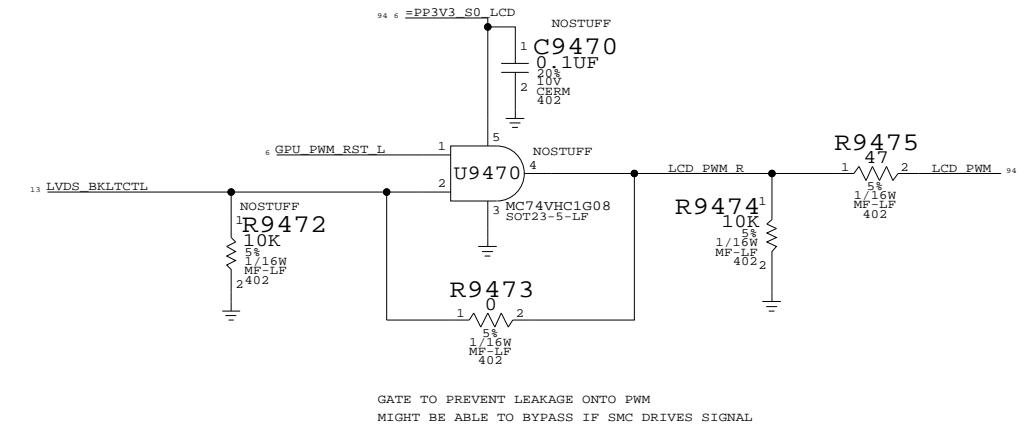
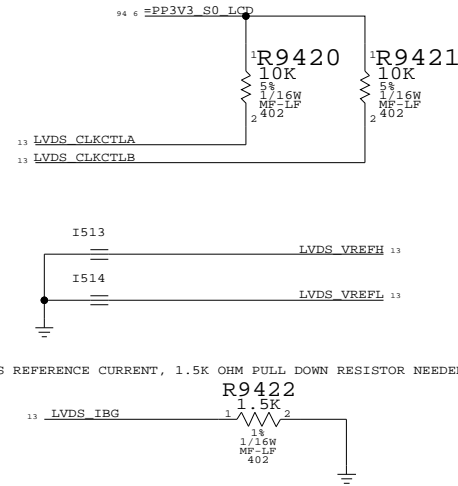
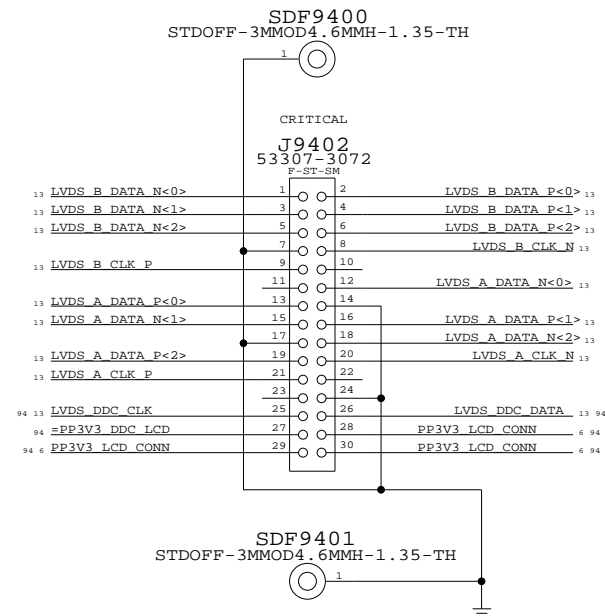
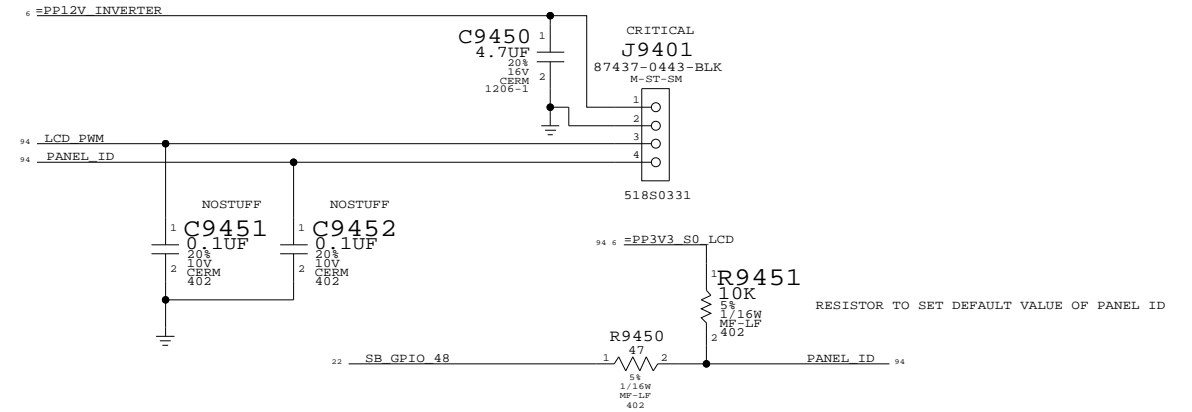
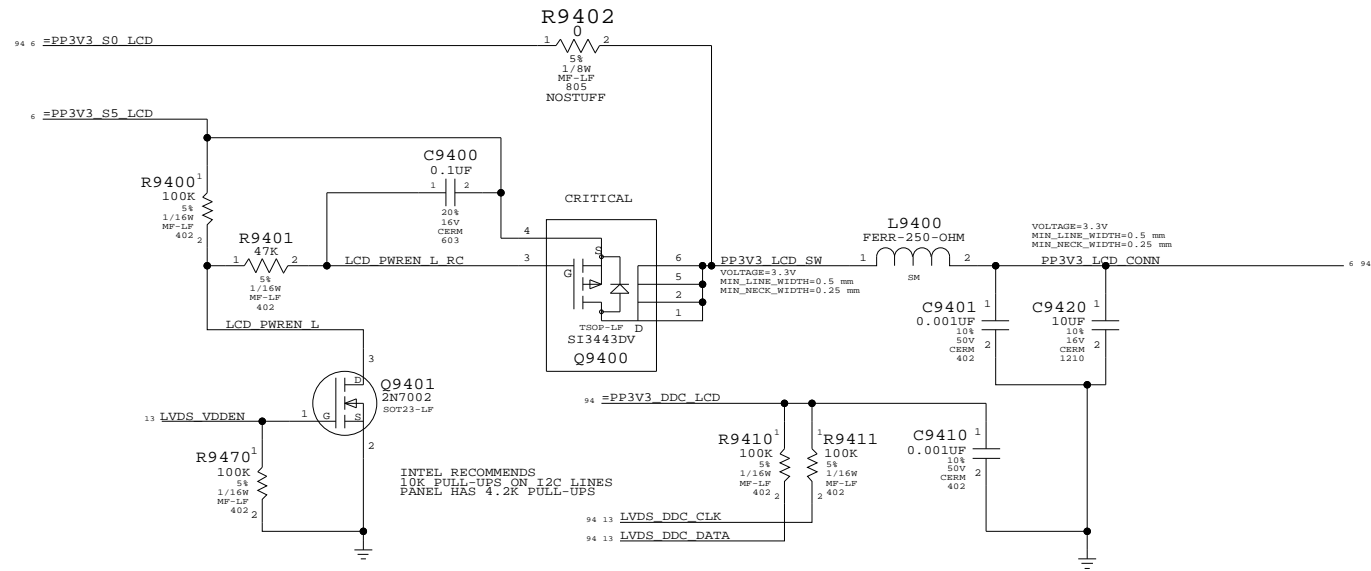
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	SCALE NONE	SHEET 83 OF 97	

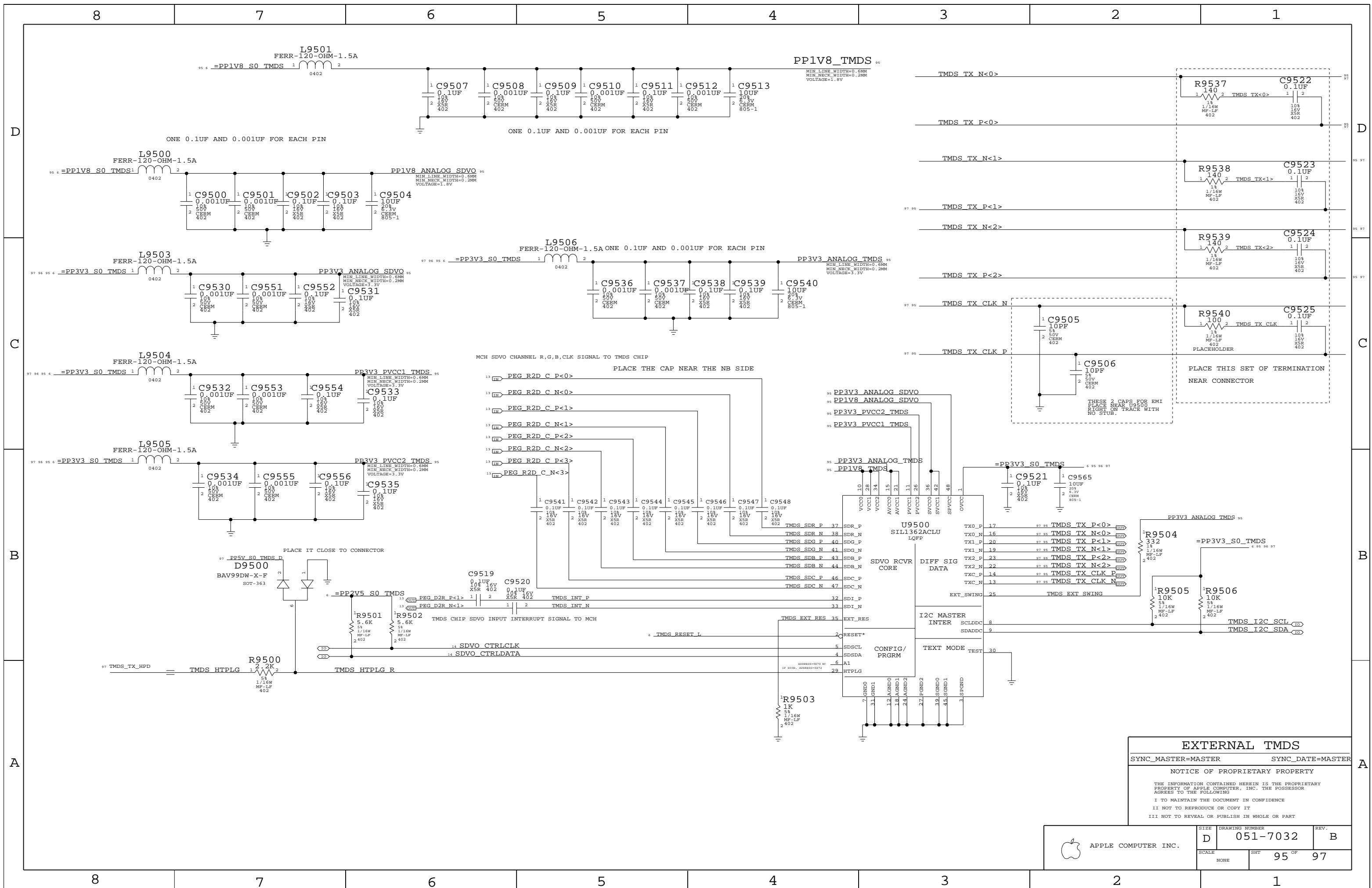
# LCD (LVDS) INTERFACE

# INVERTER INTERFACE



**Internal Display Conns**  
 SYNC\_MASTER=MASTER SYNC\_DATE=MASTER  
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**EXTERNAL TMSD**

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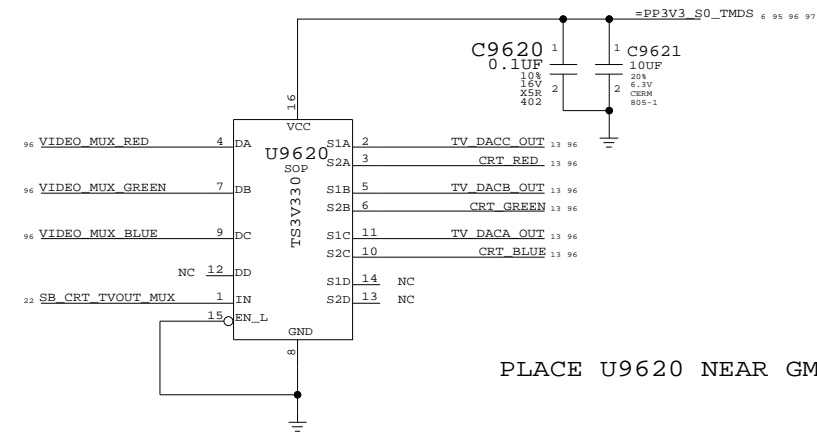
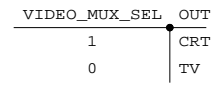
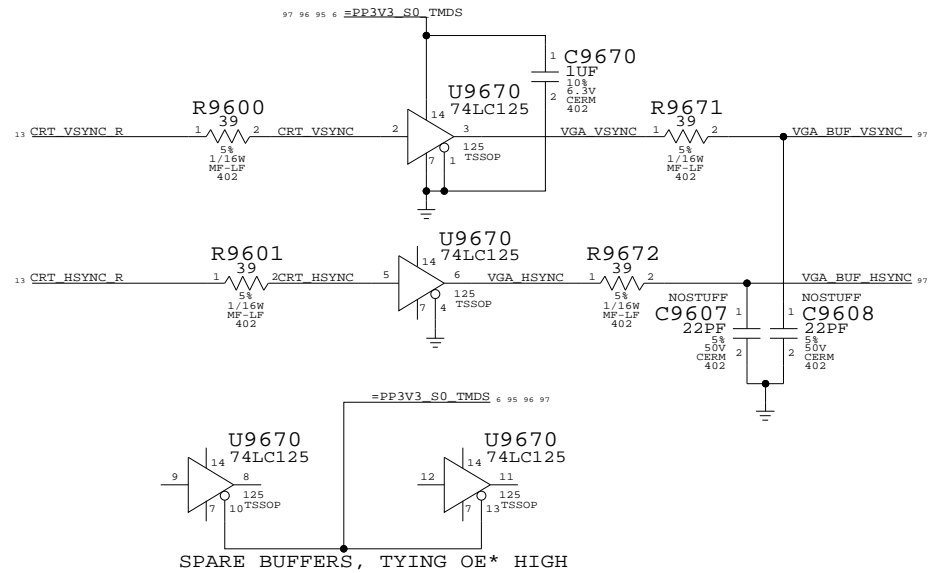
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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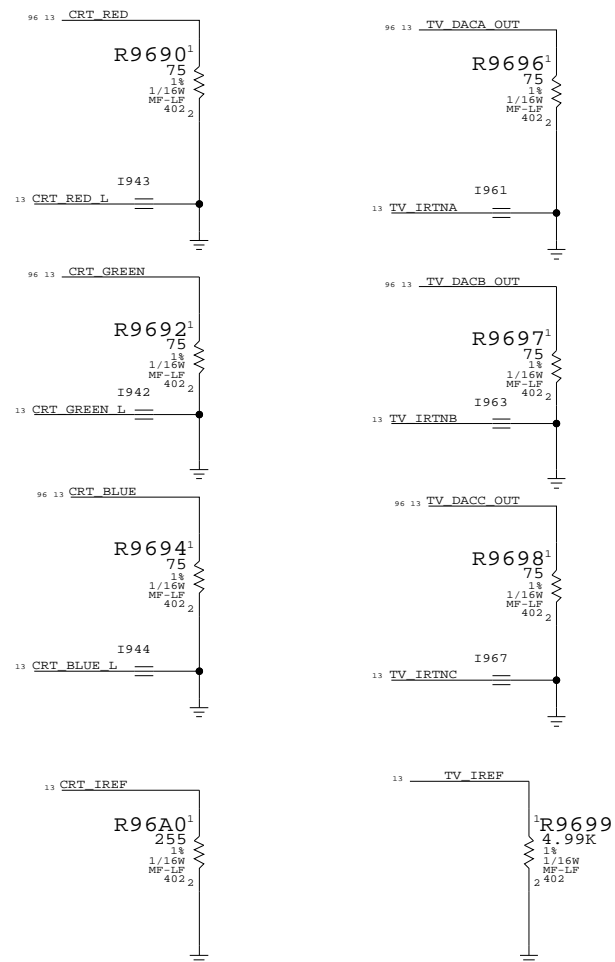
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>B</b>
	SCALE NONE	SHEET 95 OF 97	

# VGA SYNC BUFFERS

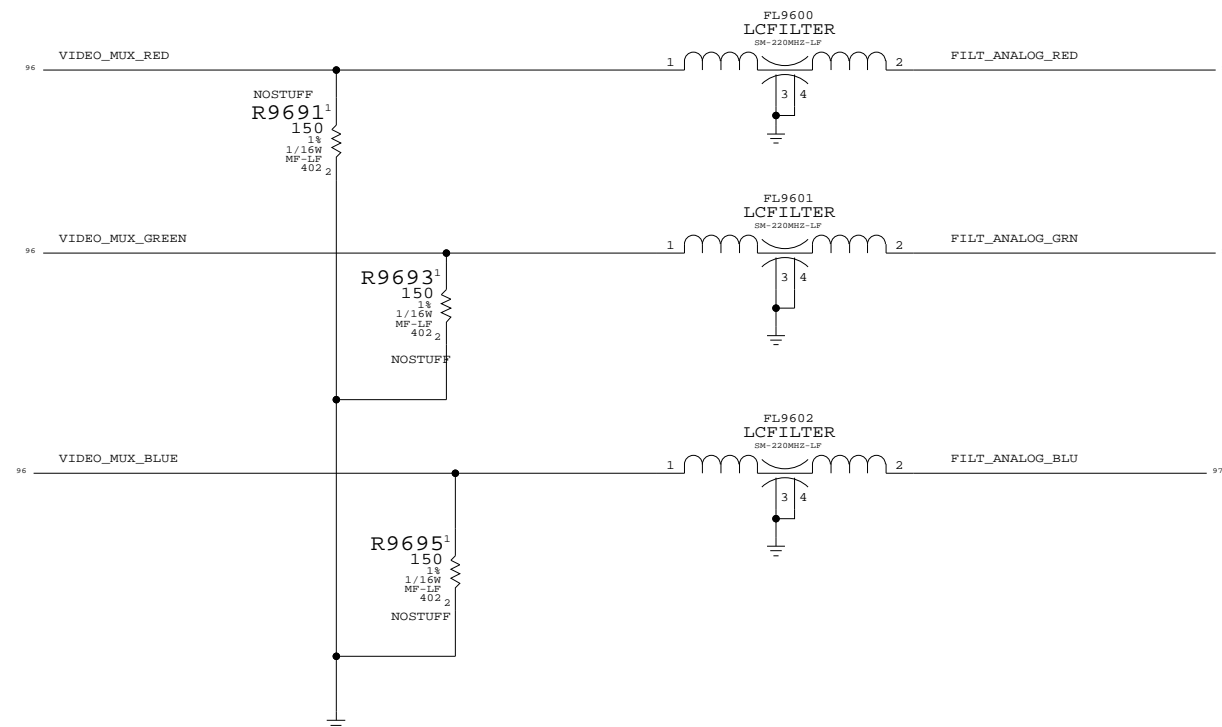


PLACE U9620 NEAR GMCH

## PLACE RESISTORS AT NORTHBRIDGE

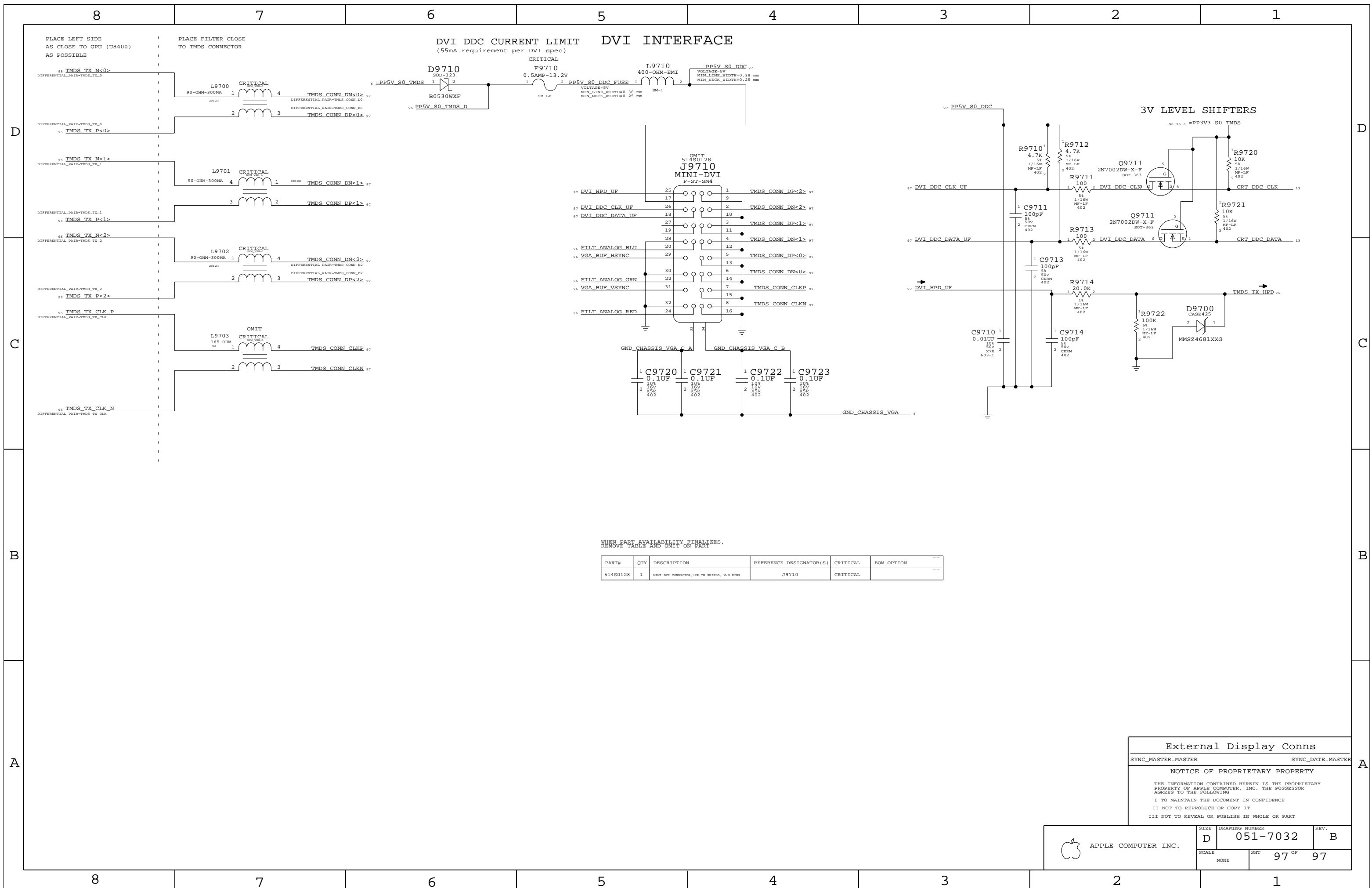


## ANALOG FILTERING PLACE BY CONNECTOR



**TMDS/Inverter/ExtVGA**  
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SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE  
(55mA requirement per DVI spec)

WHEN PART AVAILABILITY FINALIZES,  
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 3P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns  
 SYNC\_MASTER=MASTER SYNC\_DATE=MASTER  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT		97 OF 97
NONE			