

# IM4, 2 - REV A

05/18/06

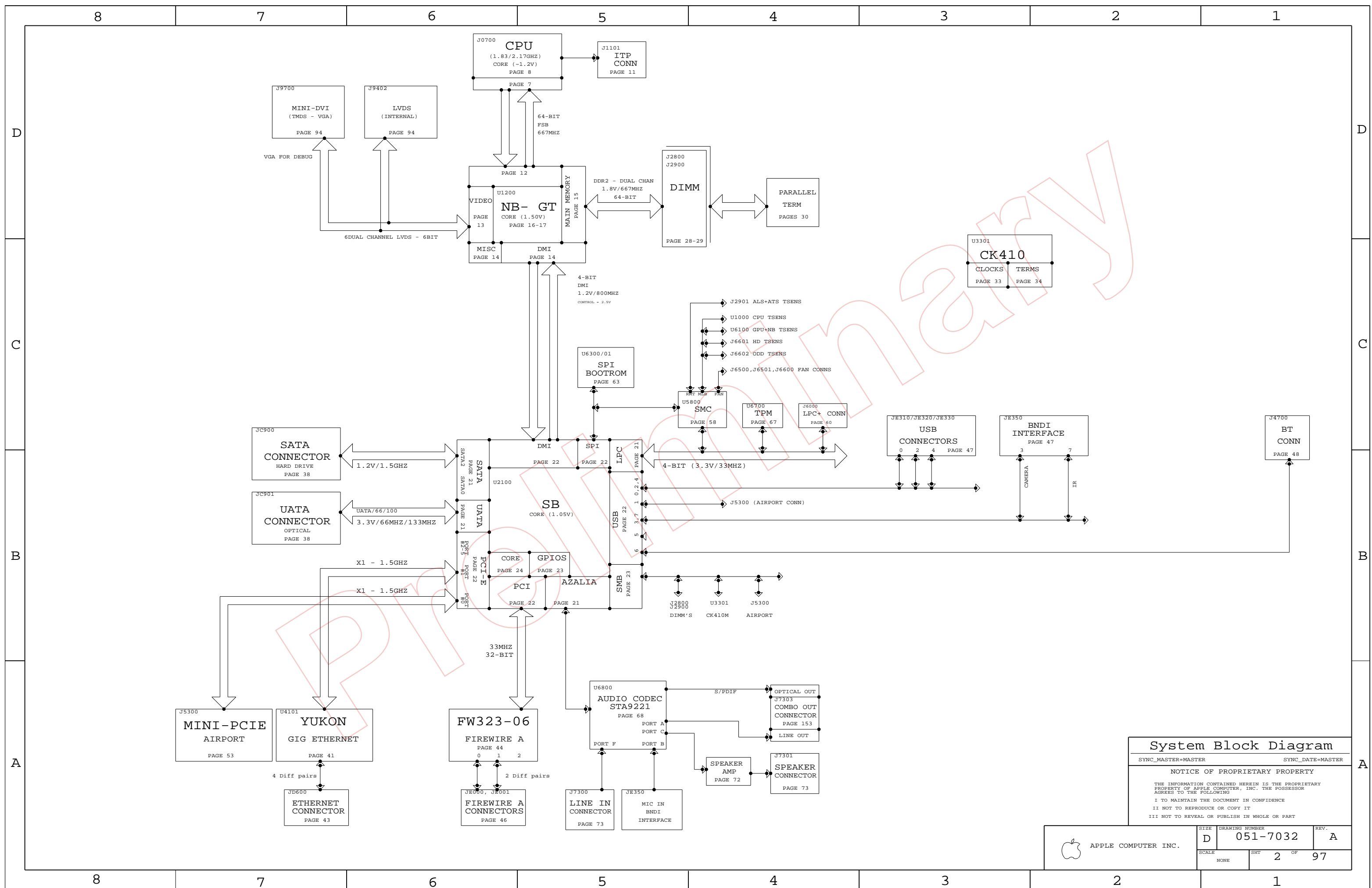
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
A		440263	PRODUCTION RELEASED	05/18/06	06/22/04

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
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18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
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25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector	AMASTER	MASTER	
29	29	DDR2 SO-DIMM Connector	BMASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUM	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p><b>METRIC</b></p>	<div style="text-align: right;"> <p>Apple Computer Inc.</p> </div> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small; text-align: center;">II. NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small; text-align: center;">III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <div style="text-align: center;"> <p><b>TITLE</b></p> <p><b>SCHEM VALLCO</b></p> </div>																						
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAWER</td> <td style="width: 25%;">DESIGN CK</td> <td style="width: 25%;">MFG APPD</td> <td style="width: 25%;">DESIGNER</td> </tr> <tr> <td>ENG APPD</td> <td></td> <td></td> <td></td> </tr> <tr> <td>QA APPD</td> <td></td> <td></td> <td></td> </tr> <tr> <td>RELEASE</td> <td></td> <td>SCALE</td> <td>NONE</td> </tr> </table>	DRAWER	DESIGN CK	MFG APPD	DESIGNER	ENG APPD				QA APPD				RELEASE		SCALE	NONE	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> <td style="width: 50%;">SIZE D</td> </tr> </table>	MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 70%;">DRAWING NUMBER</td> <td style="width: 30%;">REV.</td> </tr> <tr> <td style="text-align: center;">051-7032</td> <td style="text-align: center;">A</td> </tr> </table>	DRAWING NUMBER	REV.	051-7032	A
DRAWER	DESIGN CK	MFG APPD	DESIGNER																					
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DRAWING NUMBER	REV.																							
051-7032	A																							
SHT 1 OF 97																								



**System Block Diagram**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

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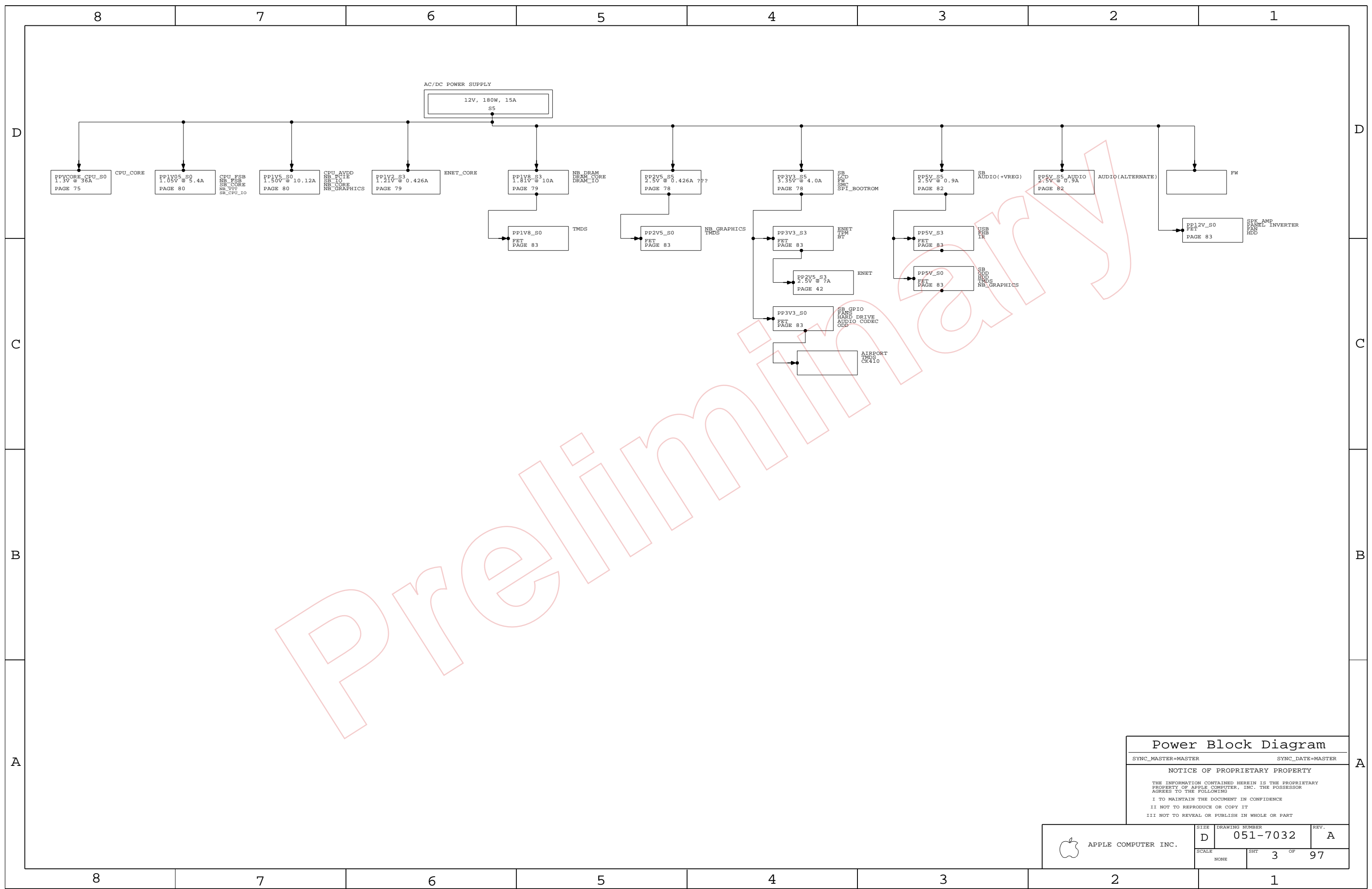
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SCALE	SHT	OF	REV.
NONE	2	97	



Preliminary

**Power Block Diagram**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

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	SCALE NONE	SHEET 3 OF 97	

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1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHEM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0021	1	EFI ROM,M50	U6301	CRITICAL	
337S3242	1	M38 CPU (C0)	CPU	CRITICAL	YONAH_1_83

341S1859 IC EFI BOOTROM DEV M50  
 337S3242 M38 CPU(C0)  
 337S3280 M50 1.83G LOW SPEED CPU (D0)  
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1235	353S1465		U7500	CPU VREG, NON-SCREENED PART

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:V3M]	CRITICAL	YONAH_1_83


Pre-internal

Table Items

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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SCALE	SHT	OF	
NONE	4	97	

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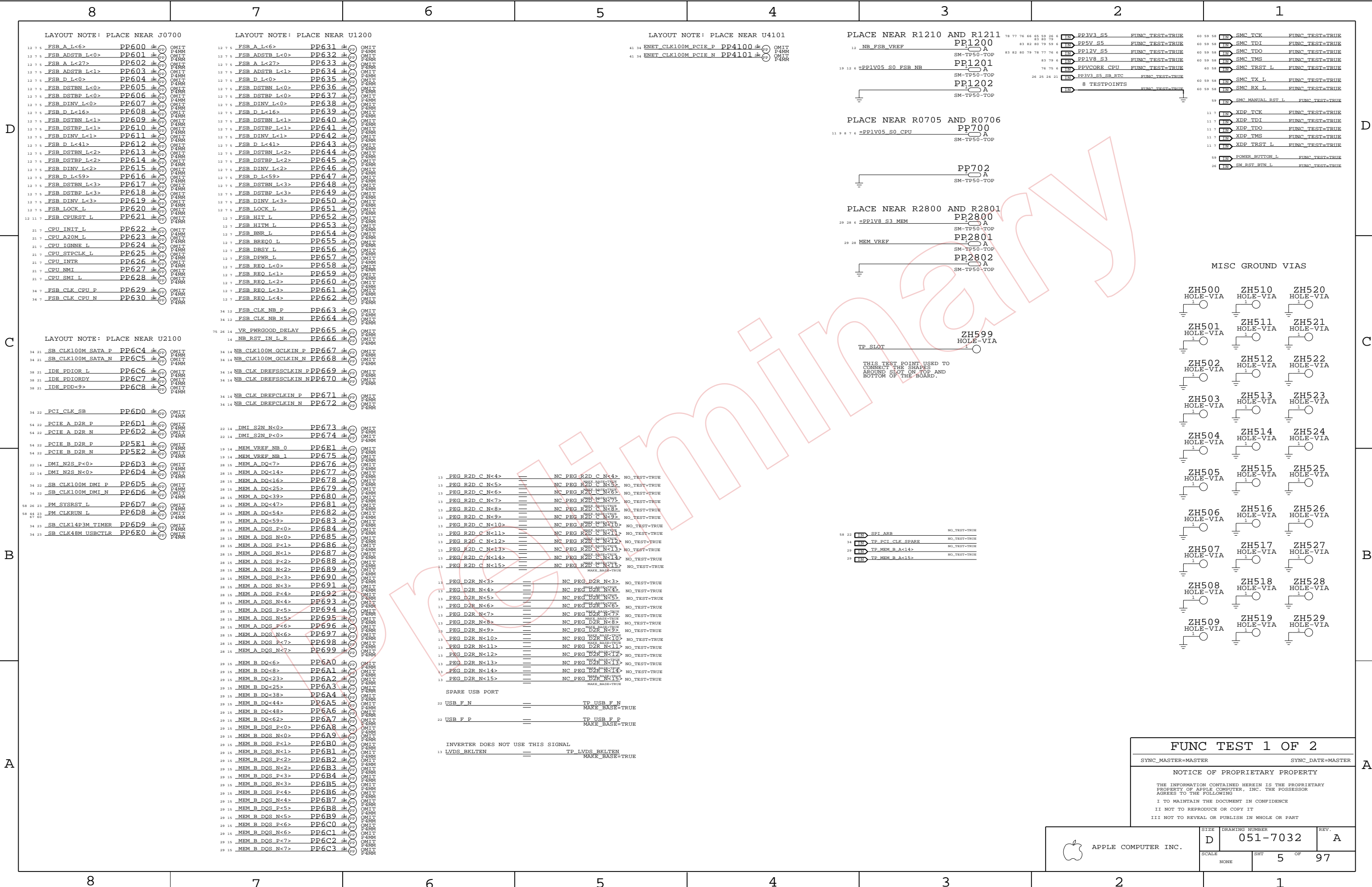
5

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1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

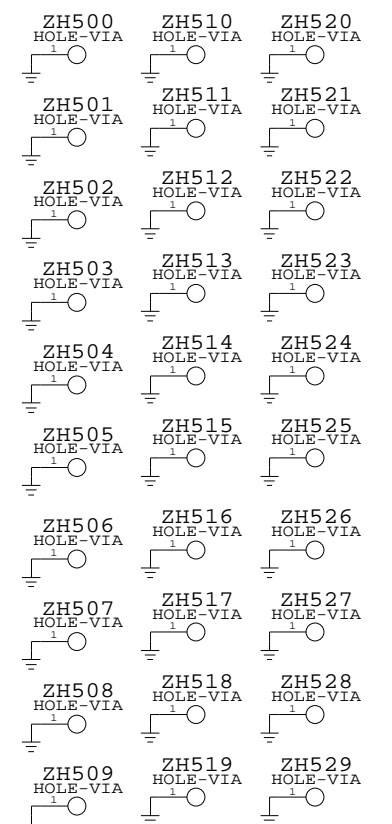
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

**FUNC TEST 1 OF 2**

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SCALE	SHEET	OF	
NONE	5	97	

D

D

C

C

B

B

A

A

"S0" RAILS

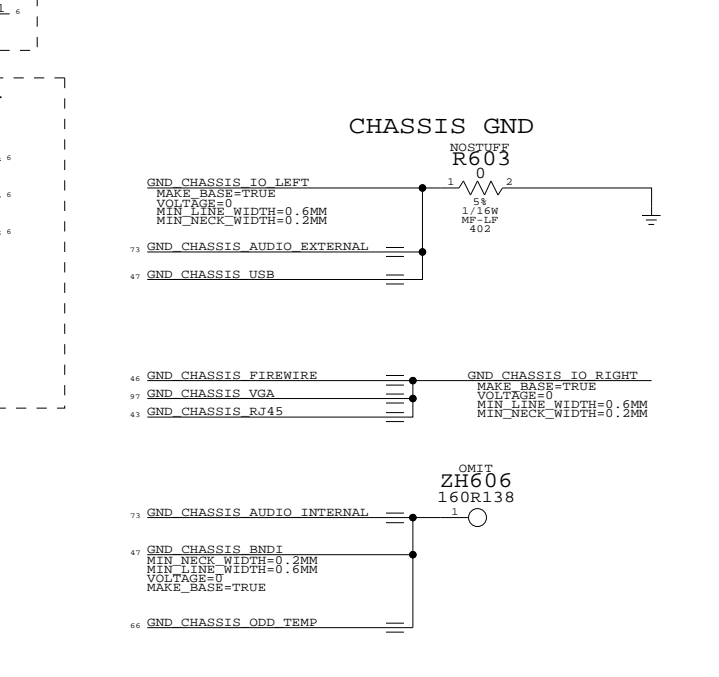
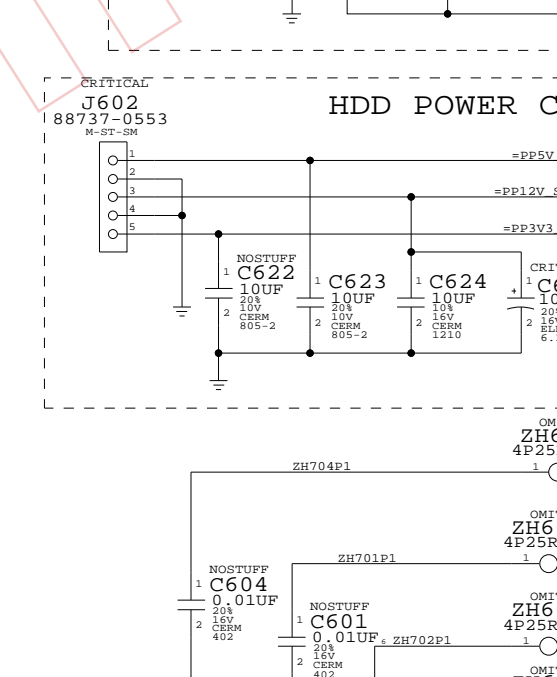
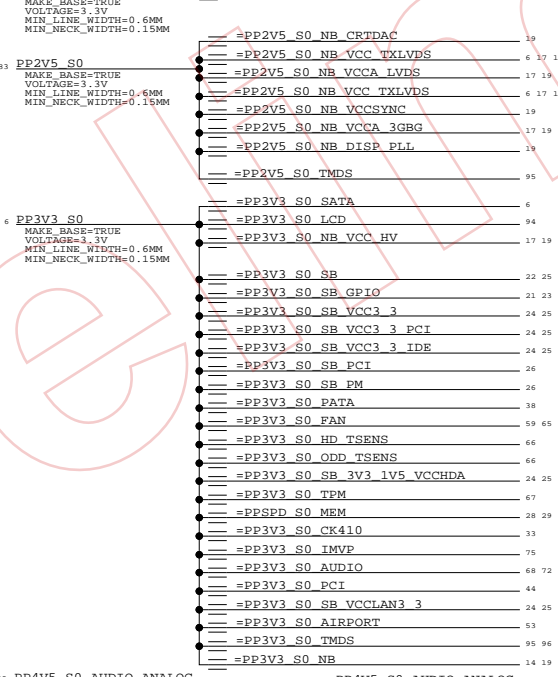
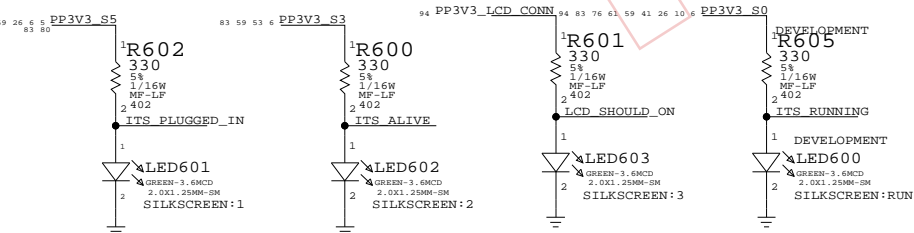
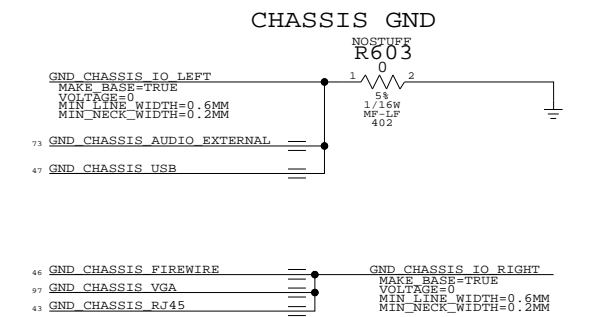
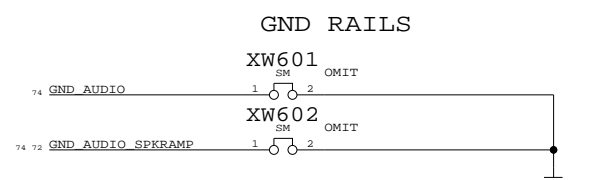
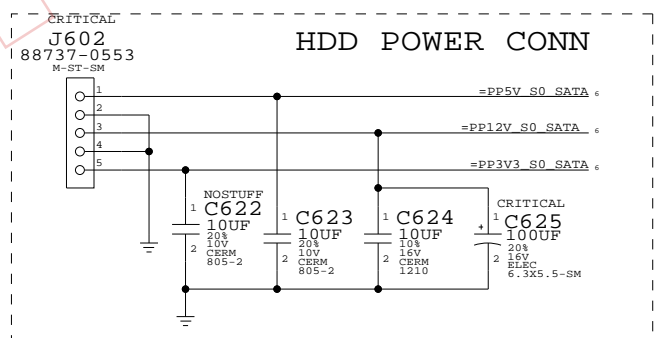
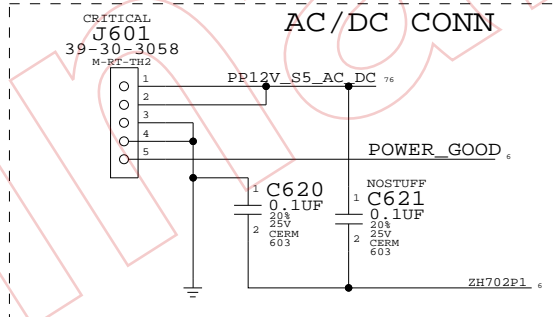
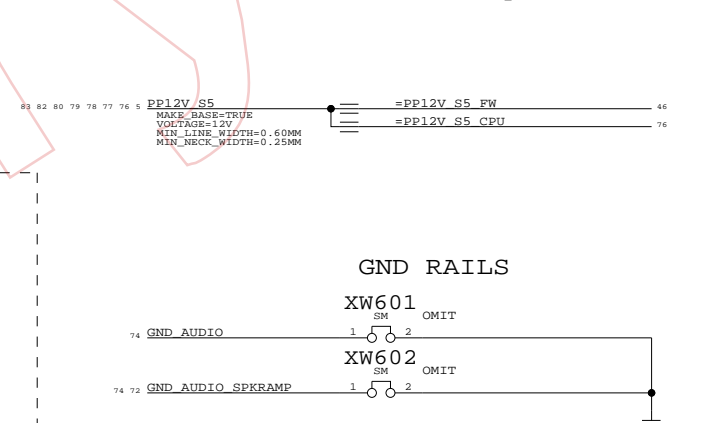
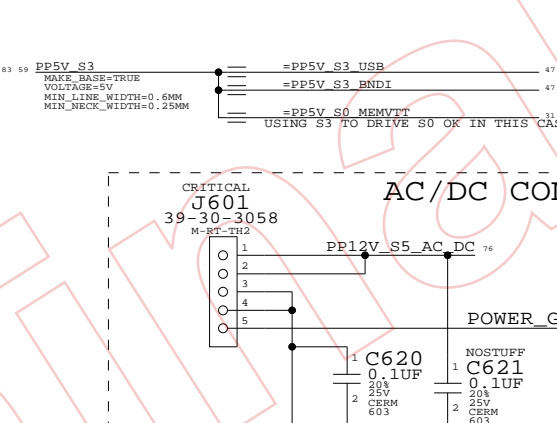
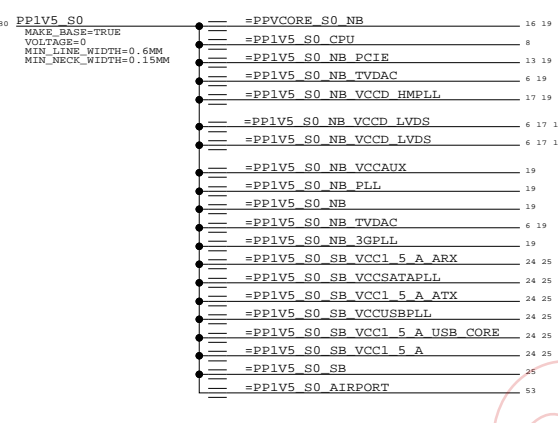
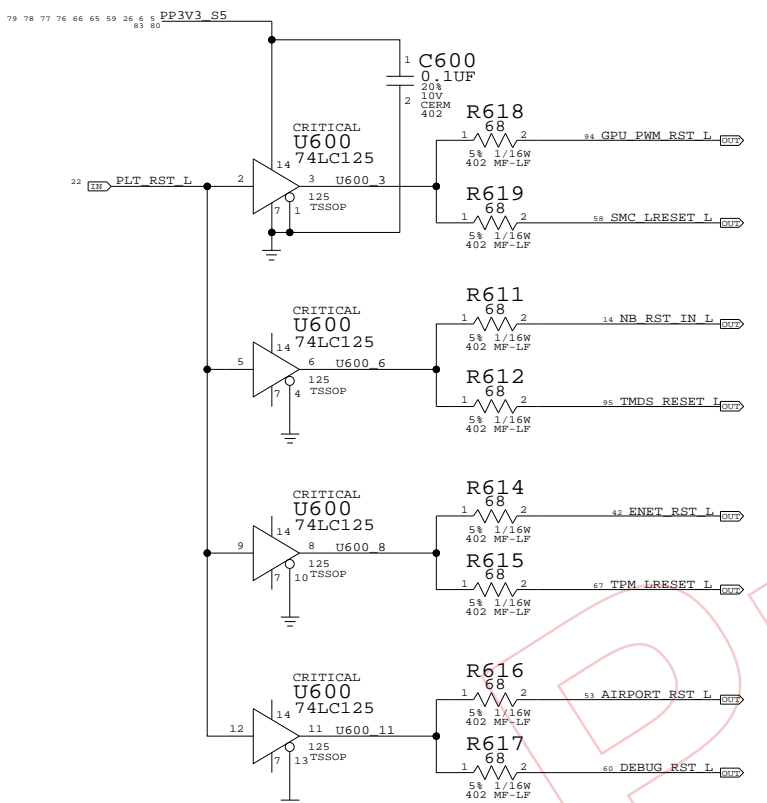
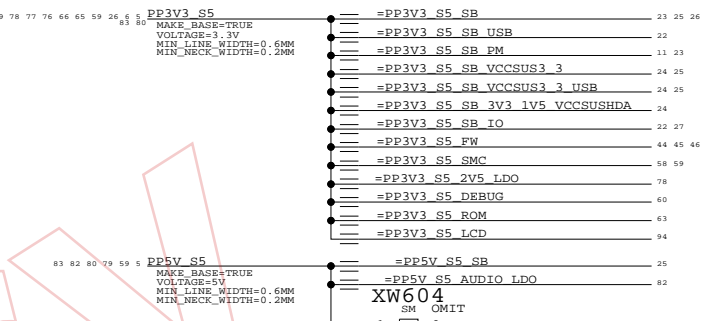
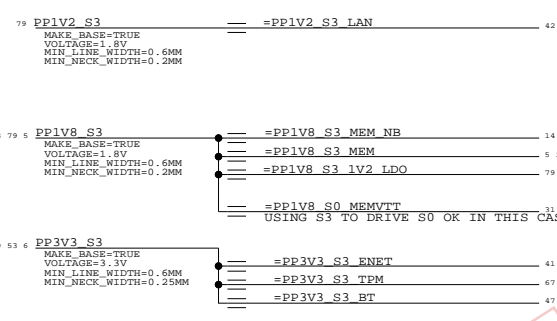
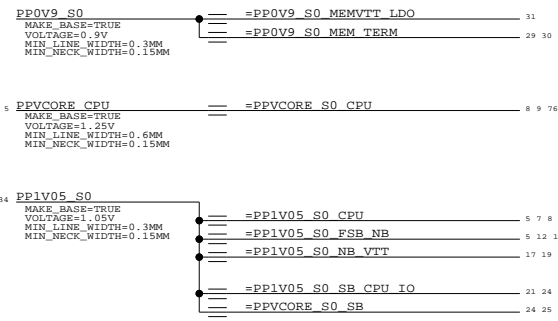
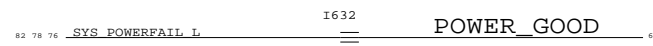
ONLY ON IN RUN

"S3" RAILS

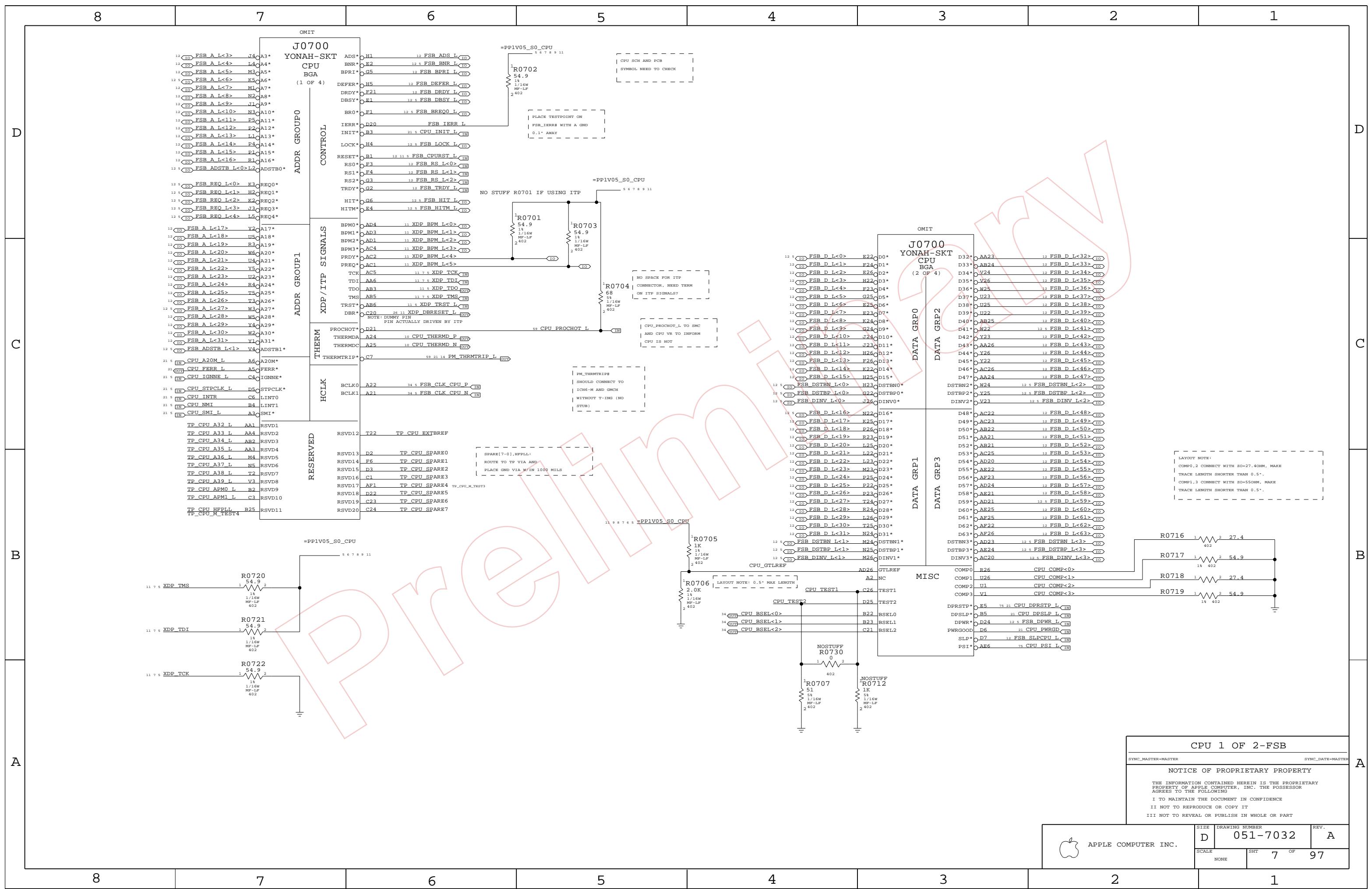
ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



Power Conn / Alias
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**CPU 1 OF 2-FSB**

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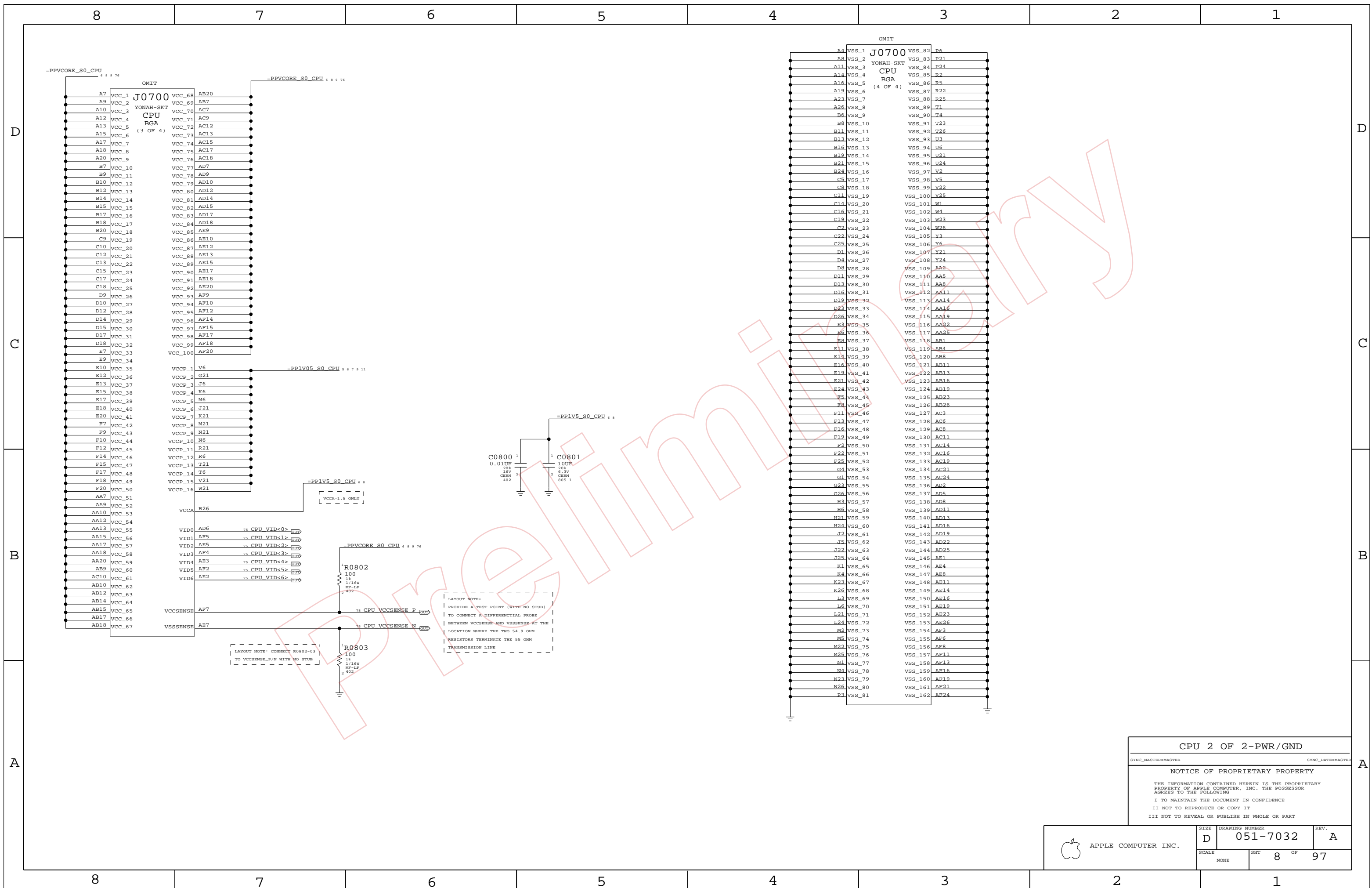
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	SCALE NONE	SHEET 7 OF 97	



**CPU 2 OF 2-PWR/GND**

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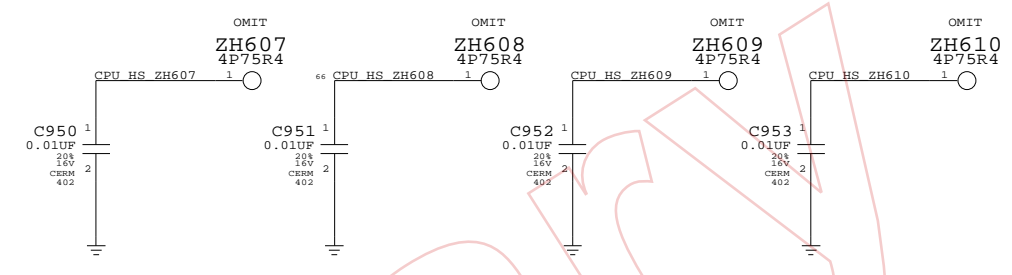
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SCALE	SHT	OF	REV.
NONE	8	97	



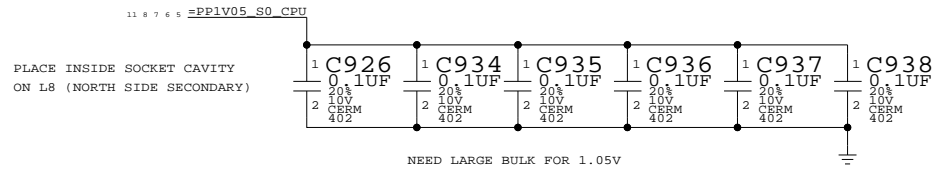
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### CPU HEATSINK MOUNTING HOLES



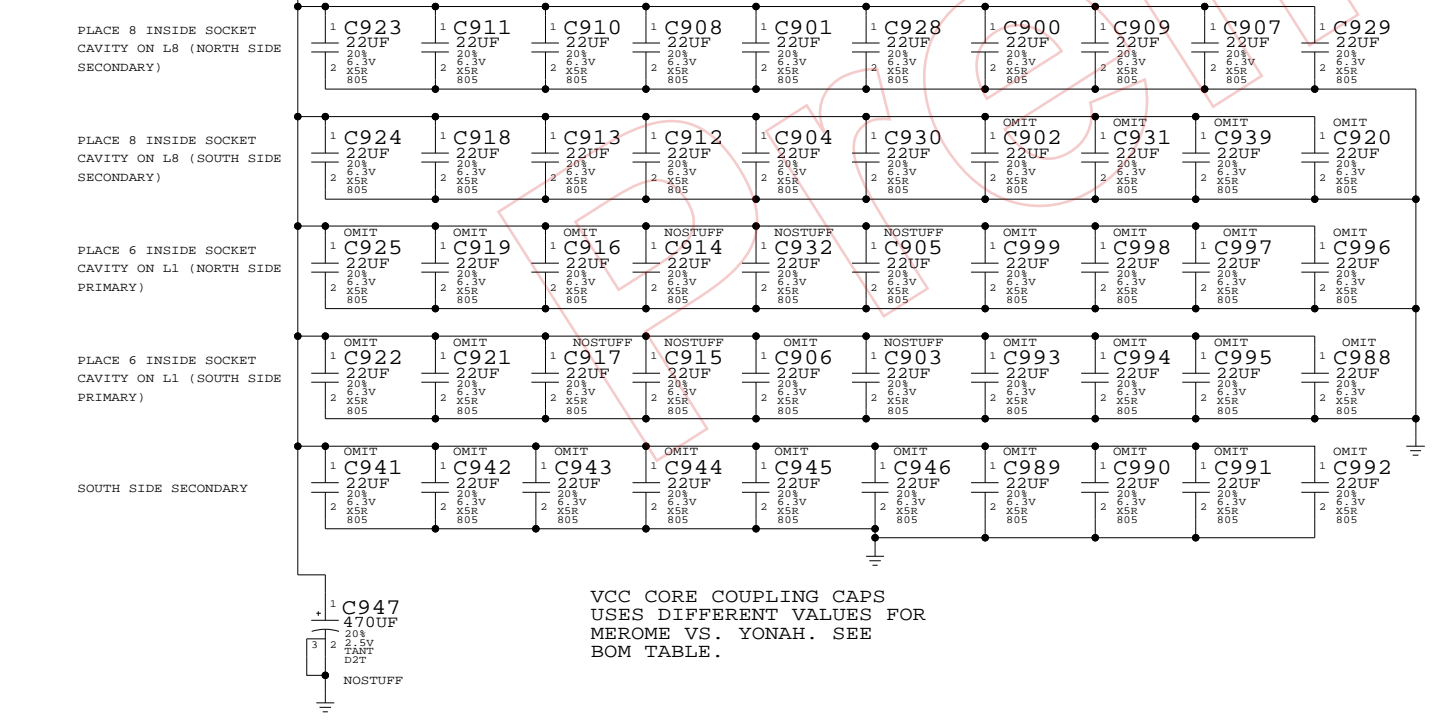
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

### VCCP CORE DECOUPLING



### VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20k, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROM C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20k, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

**CPU DECAPS & VID<>**

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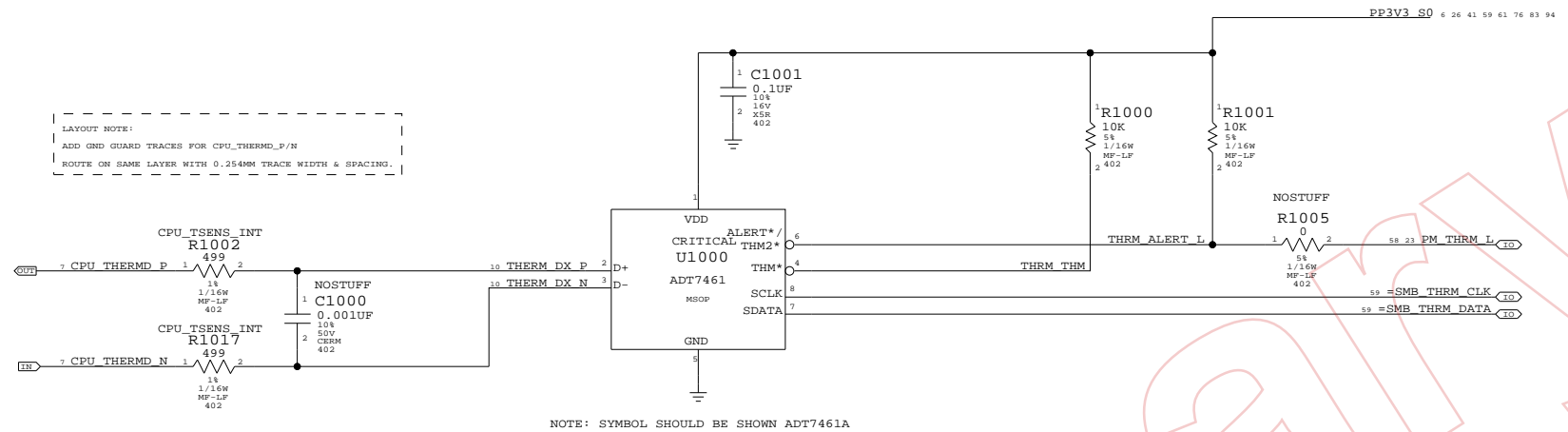
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	9 OF	97
NONE			

8 7 6 5 4 3 2 1

# CPU THERMAL SENSOR

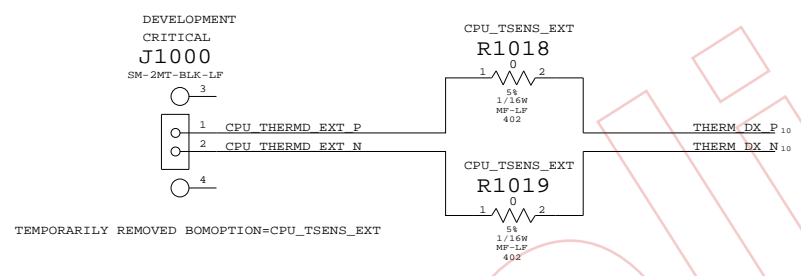
NOTE:  
IF CPU T DIODE TO BE READ IN OFF STATE,  
THEN THIS SHOULD BE S5

LAYOUT NOTE:  
ADD GND GUARD TRACKS FOR CPU\_THERMD\_P/N  
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:  
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD  
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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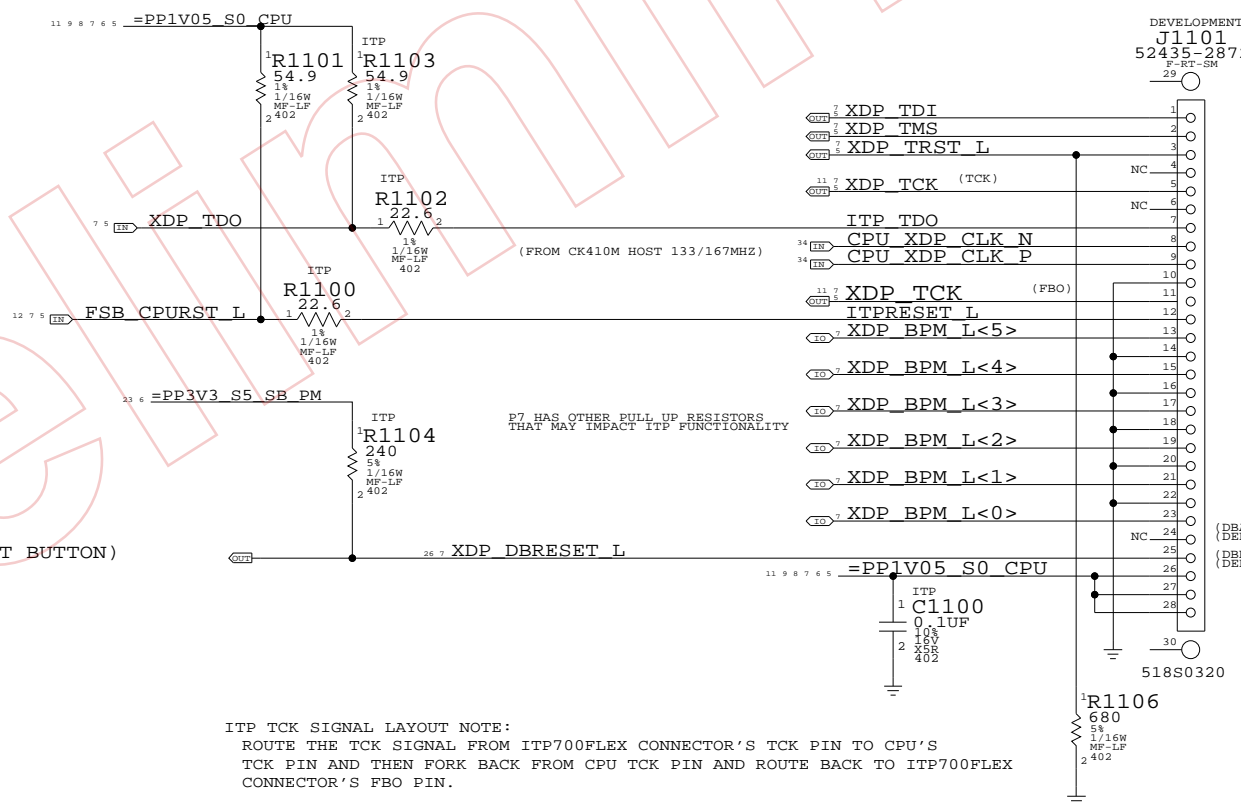
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SCALE	SHT	10 OF 97	
NONE			

### CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:  
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
 CONNECTOR'S FBO PIN.

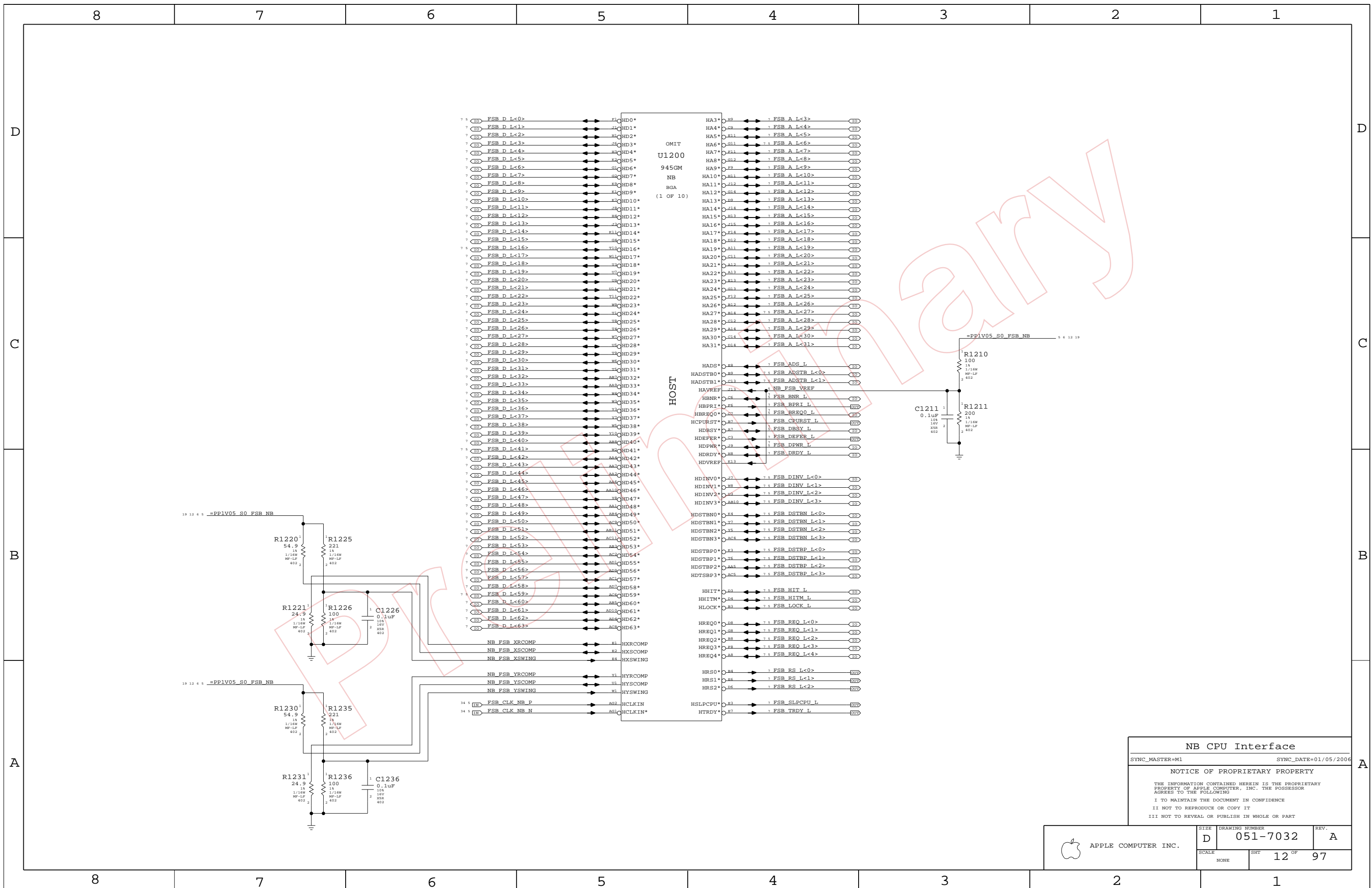
DEVELOPMENT  
 J1101  
 52435-2872  
 P-ST-SM  
 29

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.  
 (DEBUG PORT ACTIVE)  
 (DBR#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
 (DEBUG PORT RESET)

**CPU ITP700FLEX DEBUG**  
 SYNC\_MASTER=M38 SYNC\_DATE=01/05/2006

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SCALE	SHT	11 OF	97
NONE			



**NB CPU Interface**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

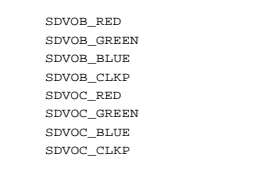
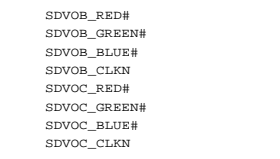
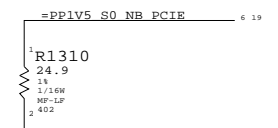
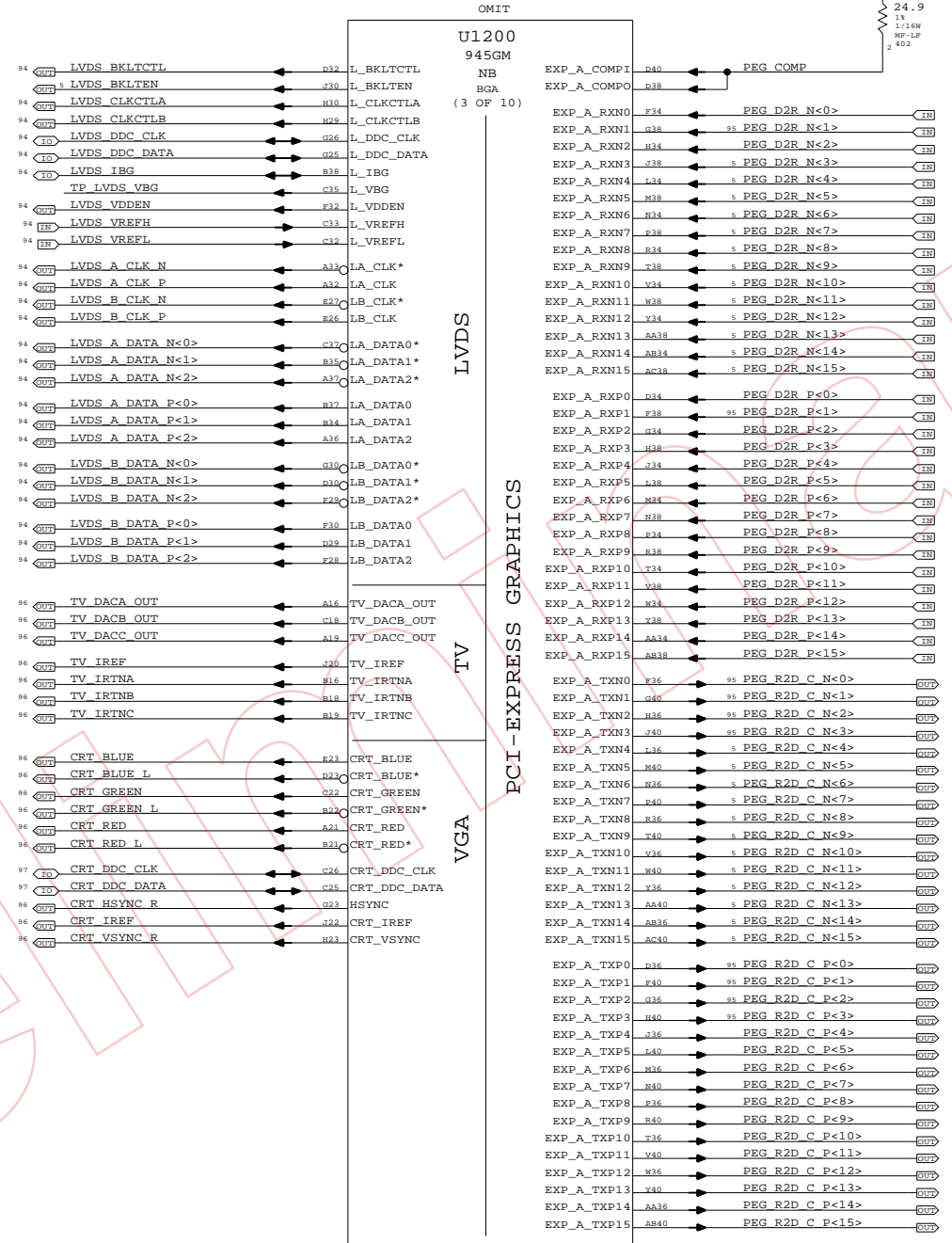
**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented  
 Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
 VCCD\_LVDS must remain powered with proper decoupling.  
 Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**  
 Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit  
 filtering components. Unused DAC outputs should  
 connect to GND through 75-ohm resistors.

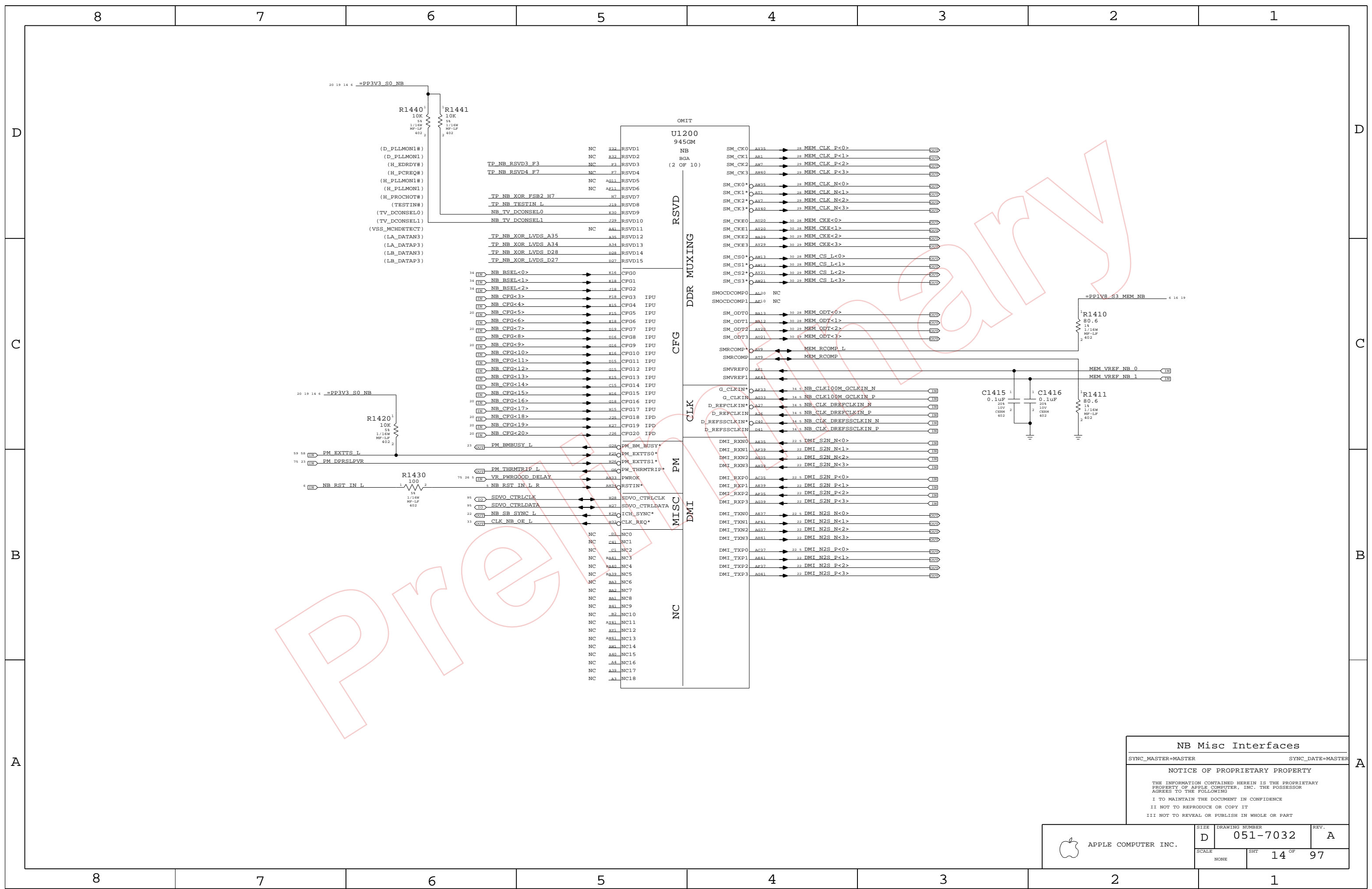
**TV-Out Disable**  
 Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
 Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
 VCCA\_TVVBG to 1.5V power rail. Tie VSSA\_TVVBG to GND.

**CRT Disable**  
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
 HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
 rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.



**NB PEG / Video Interfaces**  
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NONE			



**NB Misc Interfaces**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

**NOTICE OF PROPRIETARY PROPERTY**

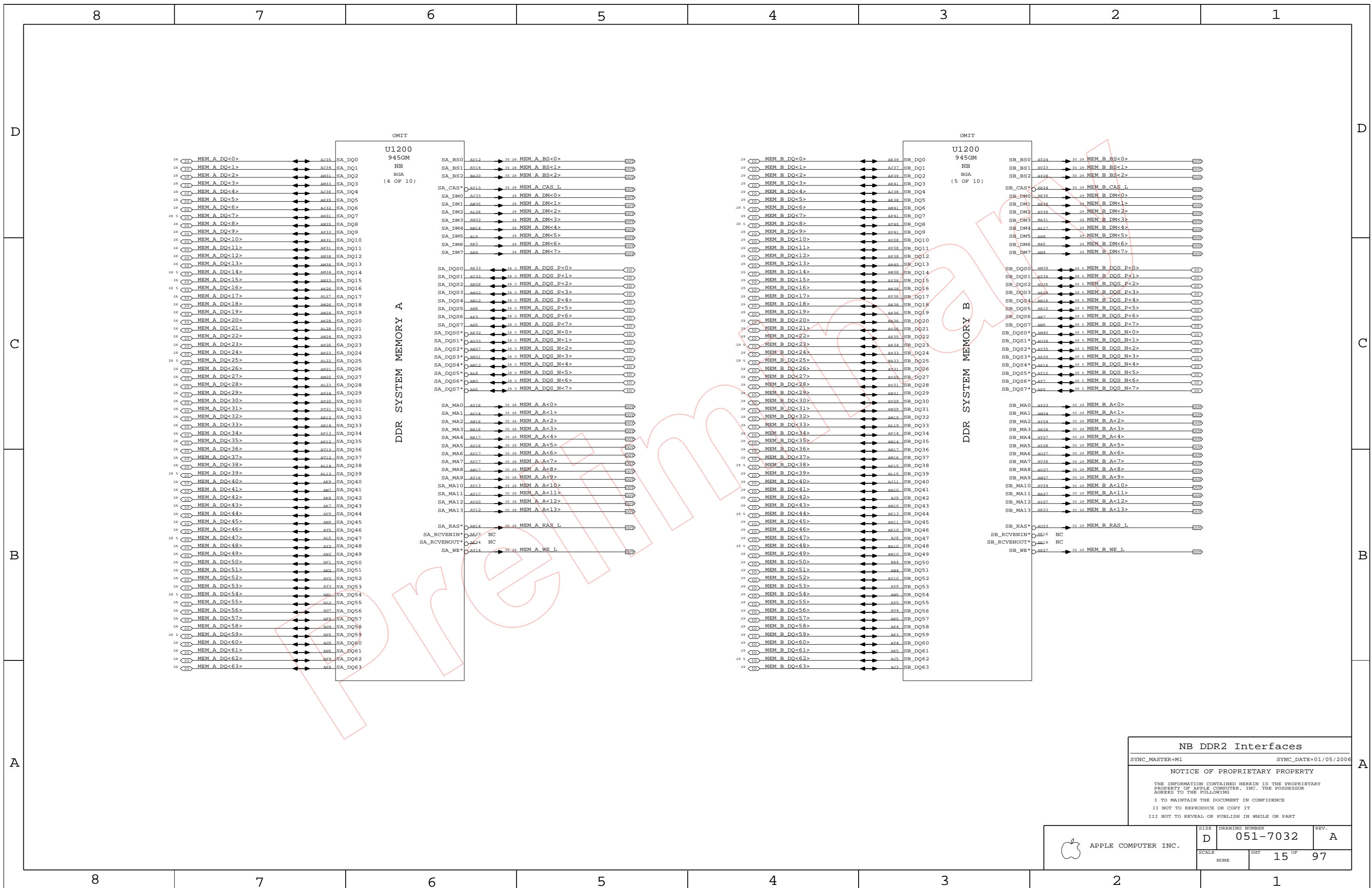
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**NB DDR2 Interfaces**

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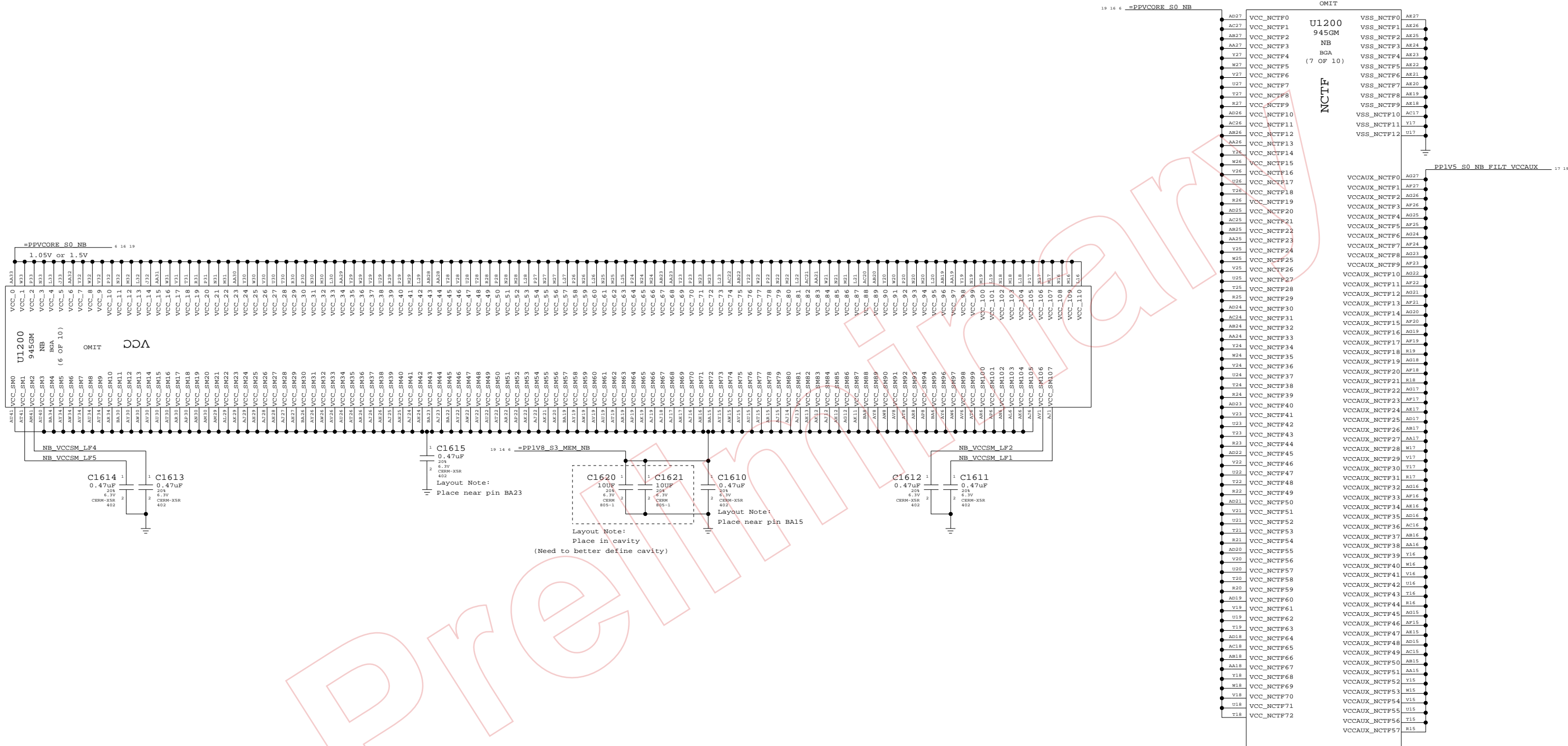
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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	SCALE NONE	SHEET 15 OF 97	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

OMIT



**NB Power 1**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

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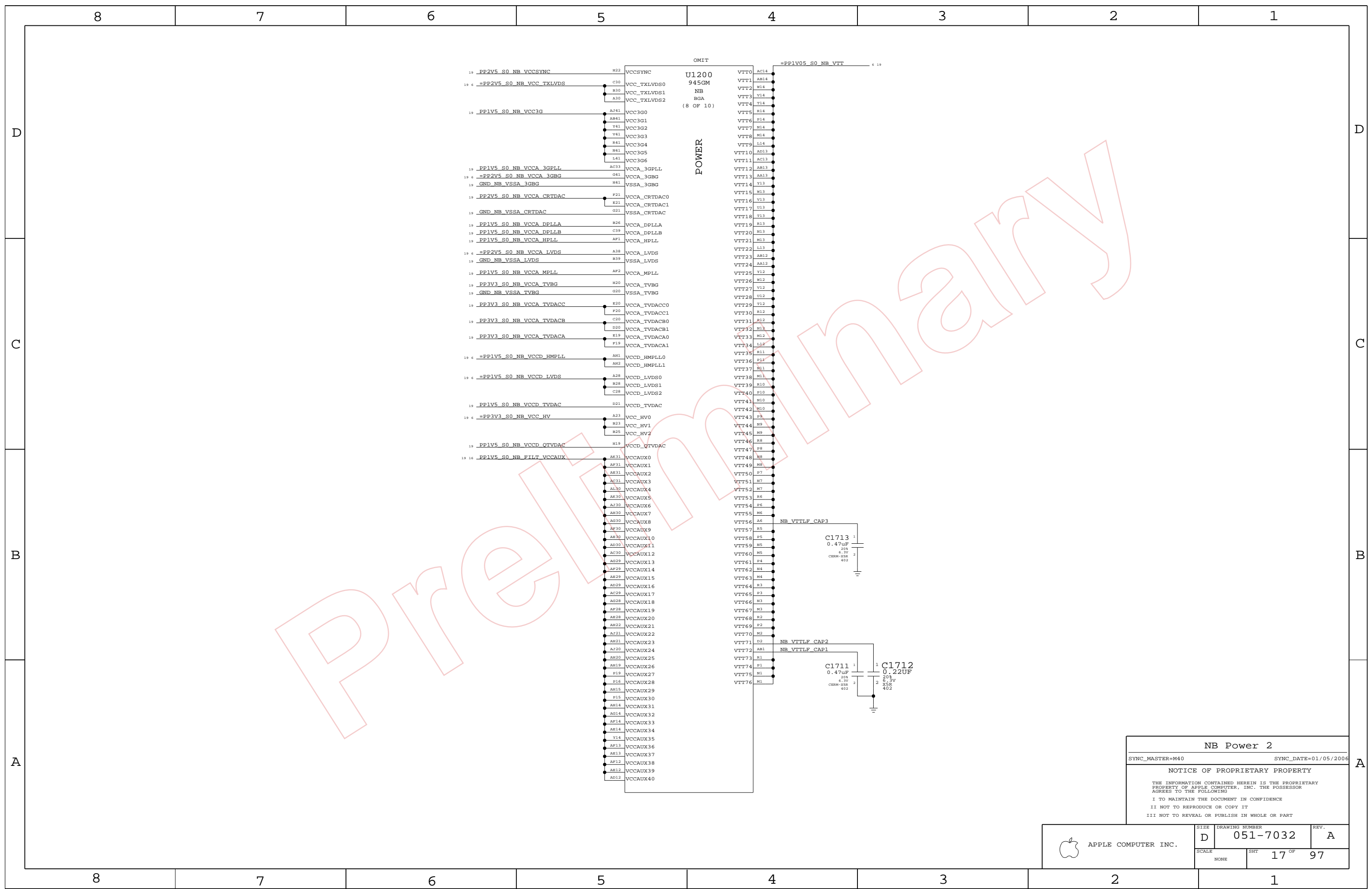
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SCALE	SHT	16 OF 97	
NONE			

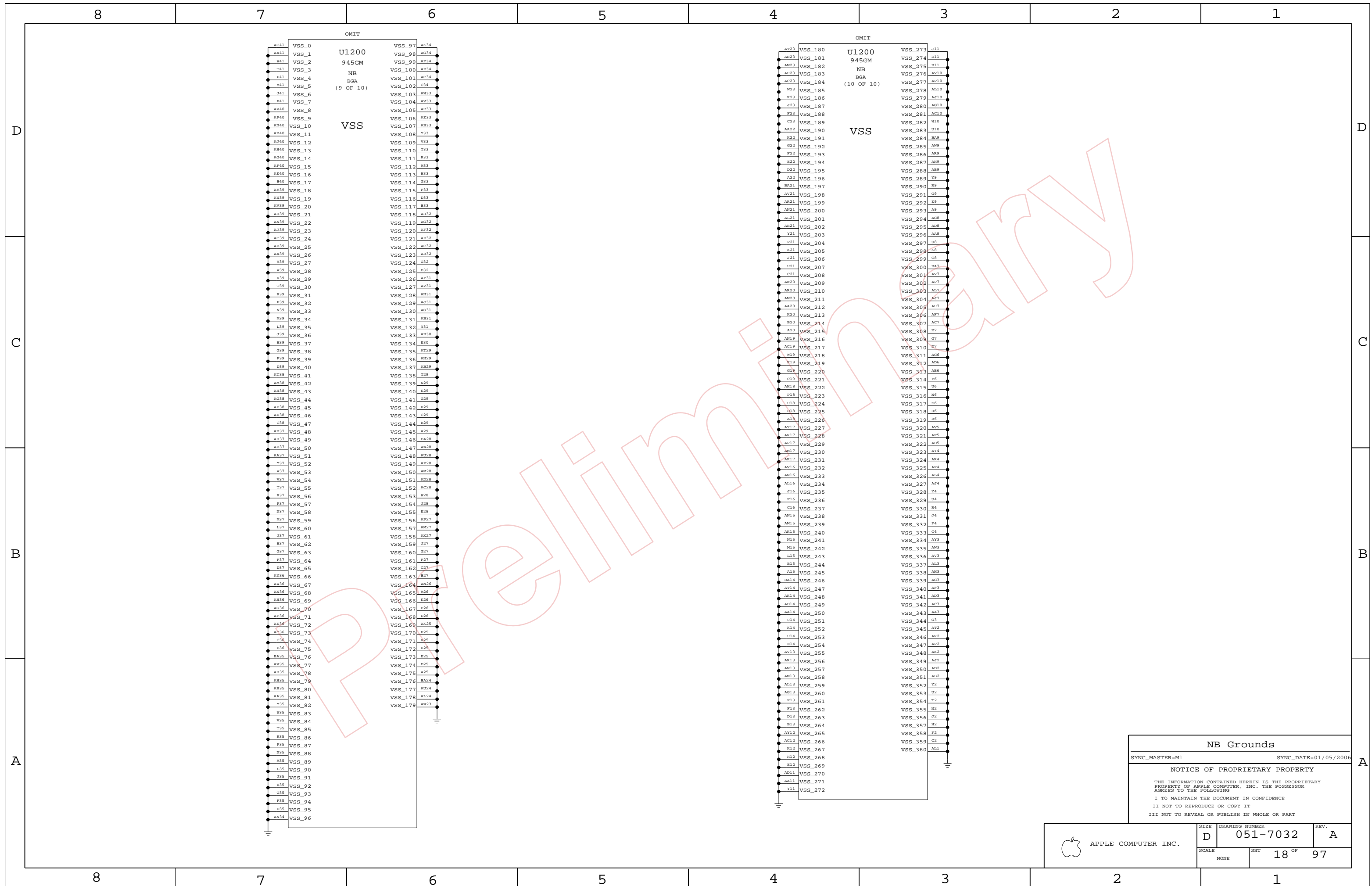




NB Power 2  
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	D	051-7032	A
SCALE	NONE	SHT	17 OF 97



**NB Grounds**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

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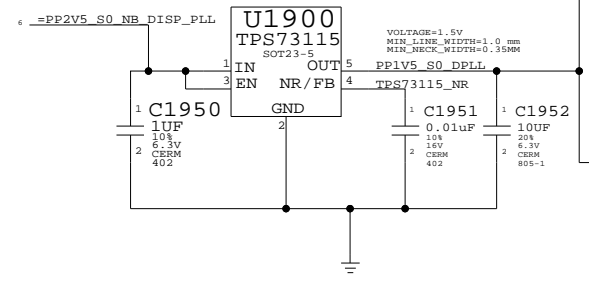
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	18 OF 97	
NONE			

### Power Interface

These are the power signals that leave the NB "block"

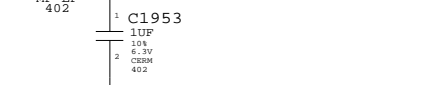
- PP1V05\_S0\_FSB\_NB 5 6 12
- PPVCORE\_S0\_NB 6 16 19
- PP1V05\_S0\_NB\_VTT 6 17 19
- PP1V5\_S0\_NB 6 19
- PP1V5\_S0\_NB\_PCIE 6 13
- PP1V5\_S0\_NB\_PLL 6 19
- PP1V5\_S0\_NB\_TVDAC 6 19
- PP1V5\_S0\_NB\_VCCD\_HMPLL 6 17
- PP1V5\_S0\_NB\_VCCD\_LVDS 6 17 19
- PP1V5\_S0\_NB\_VCCAUX 6 19
- PP1V8\_S3\_MEM\_NB 6 14 16 19
- PP2V5\_S0\_NB\_VCCSYNC 19 6
- PP2V5\_S0\_NB\_VCC\_TXLVDS 6 17 19
- PP2V5\_S0\_NB\_VCCA\_3GBG 6 17 19
- PP2V5\_S0\_NB\_VCCA\_LVDS 6 17 19
- PP3V3\_S0\_NB 6 14 20
- PP3V3\_S0\_NB\_VCC\_HV 6 17 19
- PP5V\_S0\_NB\_TVDAC 6 19

### MCH DISPLAY PLL POWER LDO



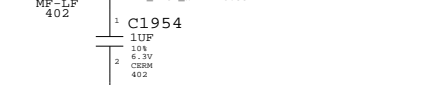
### MCH VCCA\_DPLL FILTER

(MCH DISPLAY A PLL 1.5V PWR)



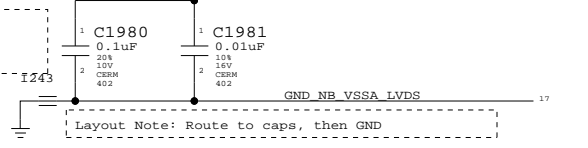
### GMCH VCCA\_DPLL\_B FILTER

(MCH DISPLAY B PLL 1.5V PWR)



### MCH VCCA\_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)



Layout Note:  
This 0.1uF cap should be within 5 mm of NB edge

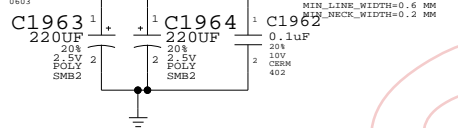
Layout Note: Route to caps, then GND

### GMCH VCCD\_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)

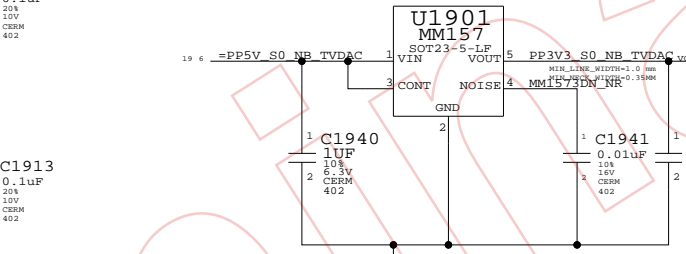


FILTERING REQUIRED FOR INTEGRATED GFX (PG. 333)



### GMCH VCCD\_LVDS BYPASS

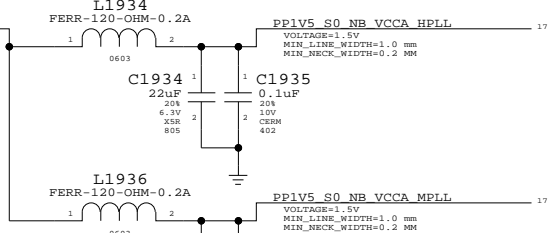
(MCH LVDS DIGITAL 1.5V PWR)



Layout Note:  
These 2 caps should be within 6.35 mm of NB edge

Layout Note: Route to caps, then GND

Layout Note:  
These 4 0.1uF caps should be within 5 mm of NB edge



### MCH VCCSYNC BYPASS

(MCH H/V SYNC 2.5V PWR)



### GMCH VCCD\_TVDAC FILTER

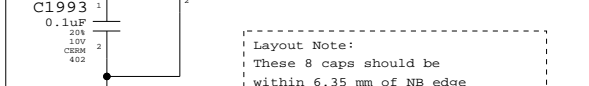
(MCH TVDAC DEDICATED PWR 1.5V)



Layout Note:  
PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

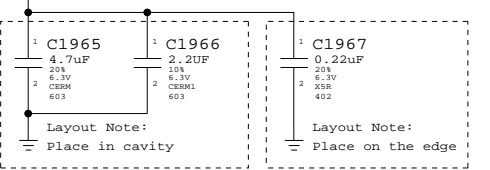
### MCH VCCA\_TVDACC FILTER

(MCH TV OUT CHANNEL A 3.3V PWR)



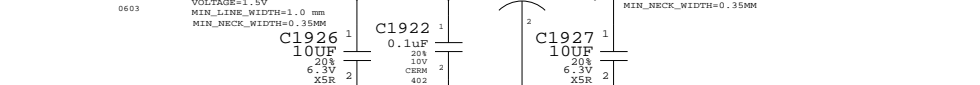
Layout Note:  
These 8 caps should be within 6.35 mm of NB edge

Layout Note:  
Place in cavity



### GMCH VCCD\_QTVDAC FILTER

(MCH TVDAC DIGITAL QUIET 1.5V PWR)



### MCH VCCA\_TVDAC FILTER

(MCH TV OUT CHANNEL B 3.3V PWR)



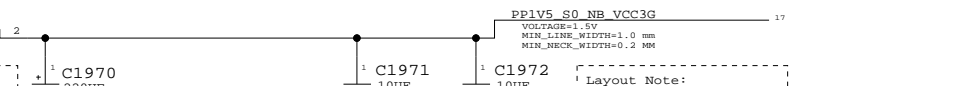
Layout Note:  
These 8 caps should be within 6.35 mm of NB edge

Layout Note:  
Place in cavity



### GMCH VCCD\_QTVDAC FILTER

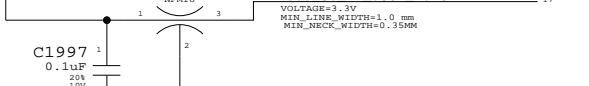
(MCH TVDAC DIGITAL QUIET 1.5V PWR)



Layout Note:  
10uF caps should be close to MCH on opposite side.

### MCH VCCA\_TVDBG FILTER

(MCH TV DAC BAND GAP 3.3V PWR)

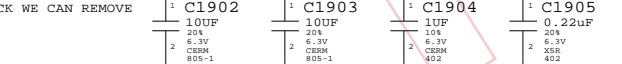


Layout Note: Route to caps, then GND

Layout Note:  
Place L and C close to MCH



Layout Note:  
Place in cavity



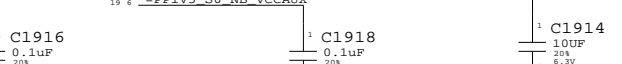
Layout Note:  
Place in cavity



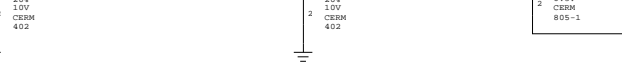
Layout Note:  
Place in cavity



Layout Note:  
Place in cavity



Layout Note:  
Place in cavity



### NB (GM) Decoupling

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

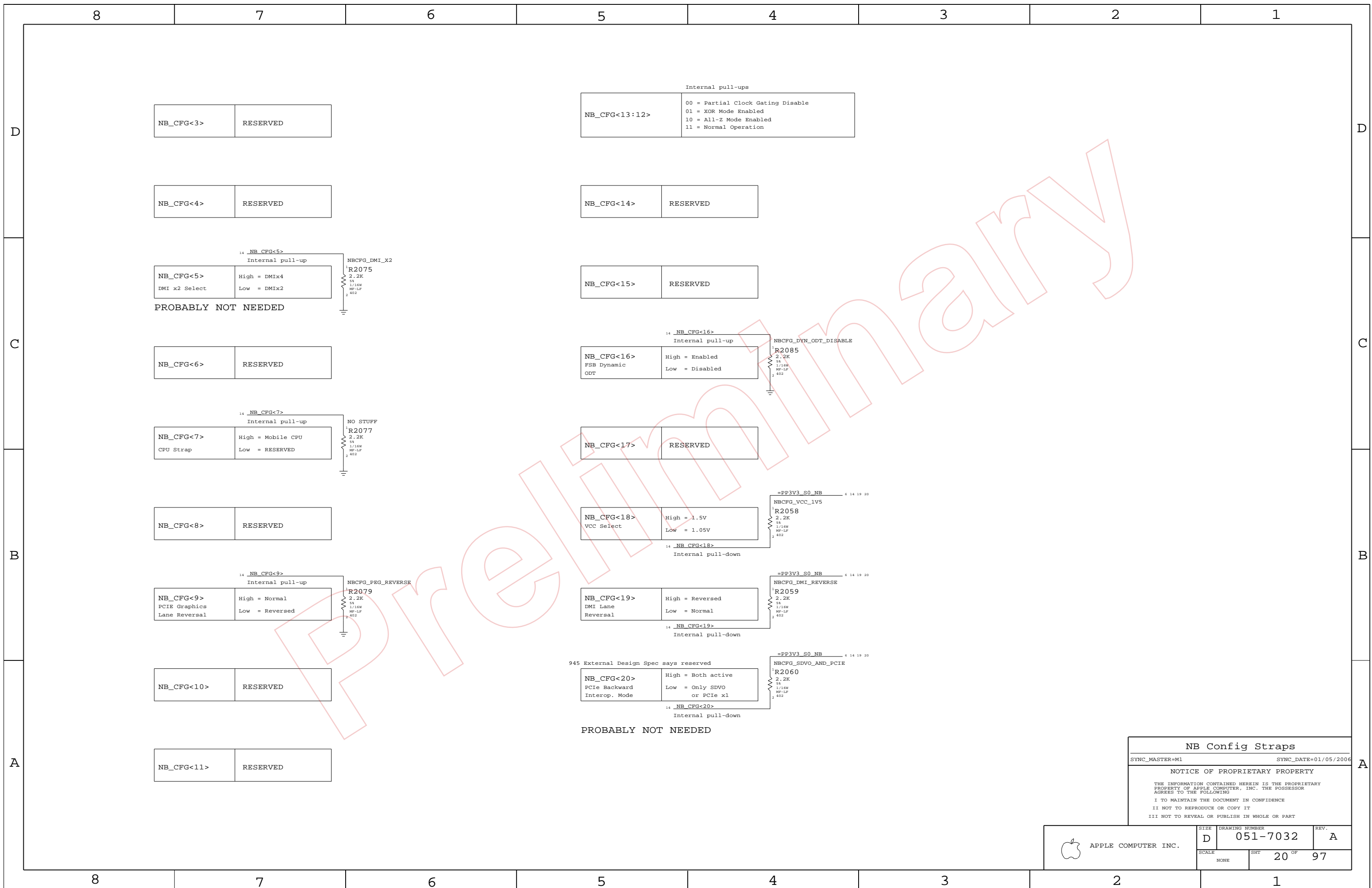
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		A
NONE	051-7032	19 OF 97



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**NB Config Straps**

SYNC\_MASTER=M1 SYNC\_DATE=01/05/2006

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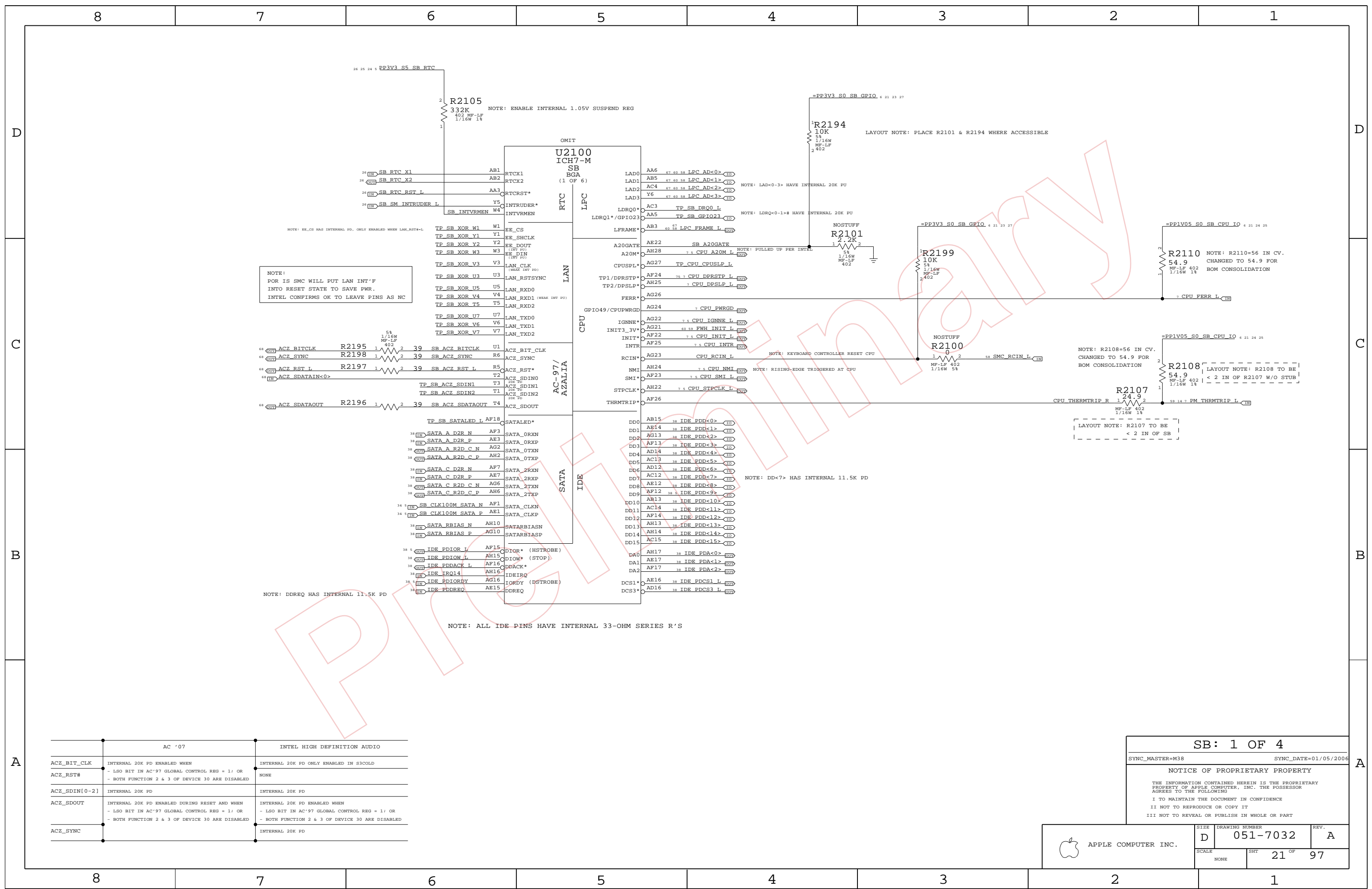
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SCALE	SHT	20 OF 97	
NONE			



NOTE:  
 POR IS SMC WILL PUT LAN INT'F  
 INTO RESET STATE TO SAVE PWR.  
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

**SB: 1 OF 4**

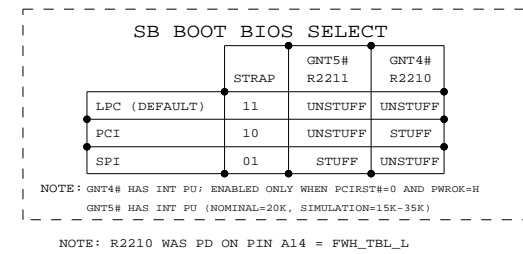
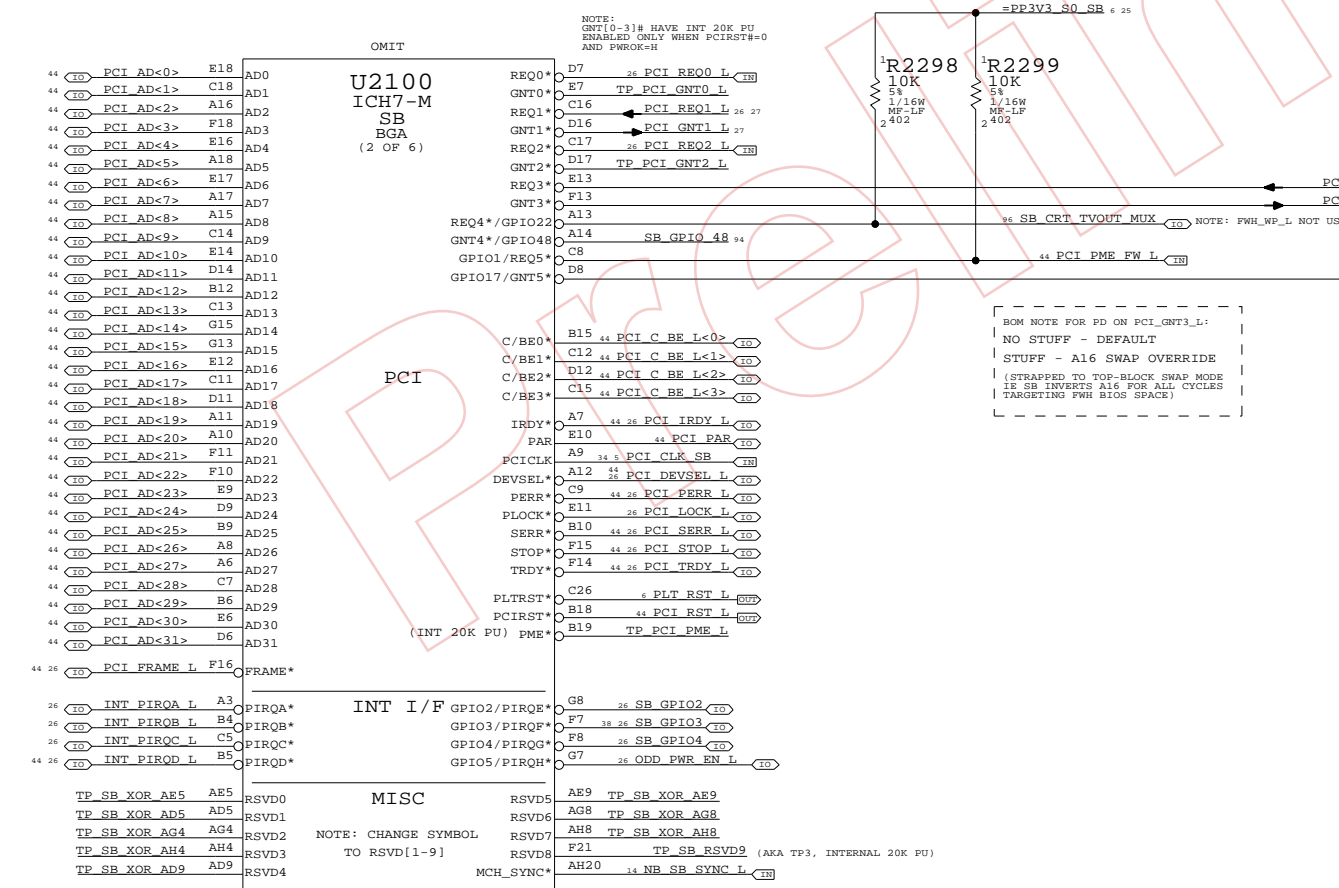
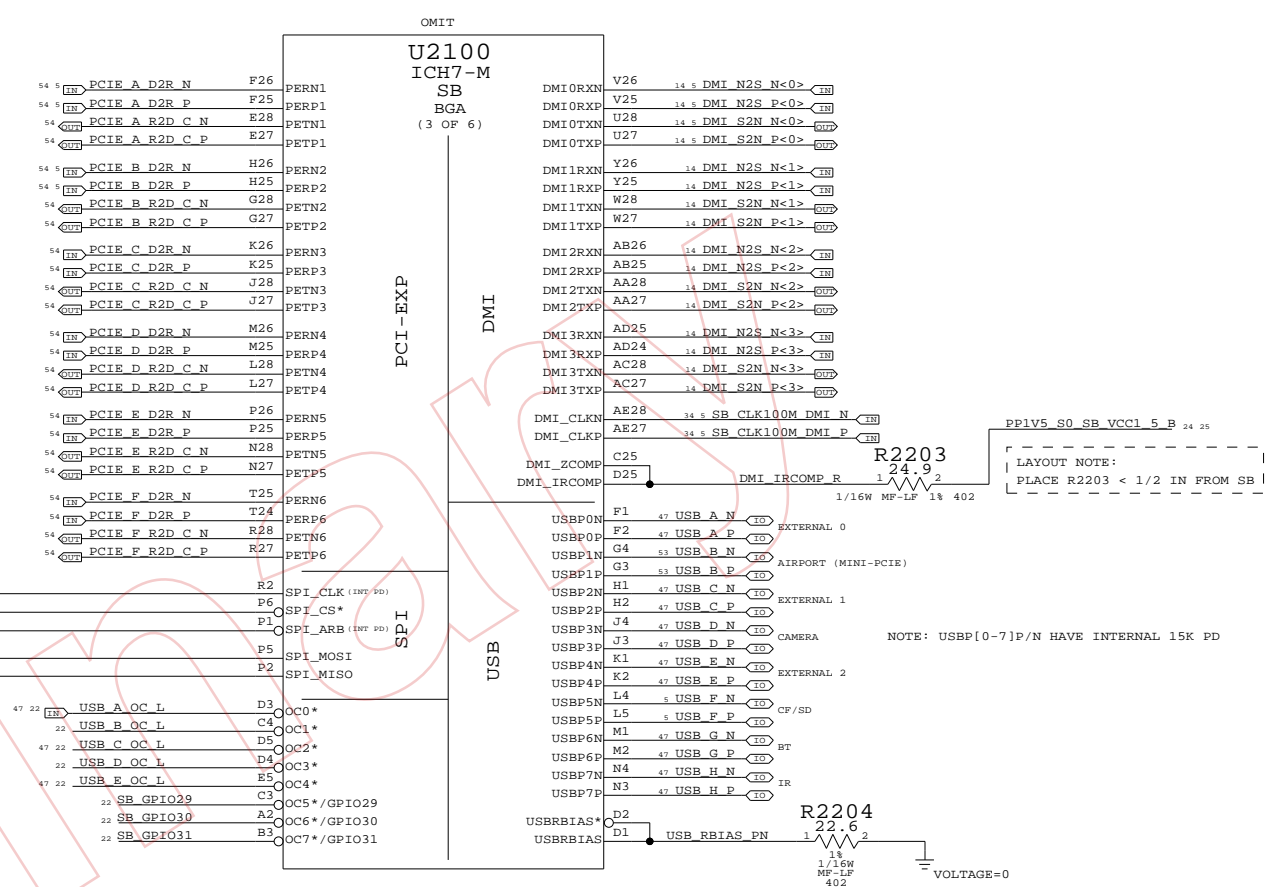
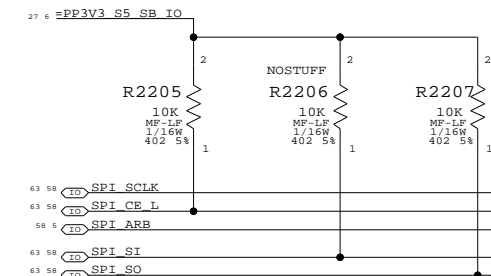
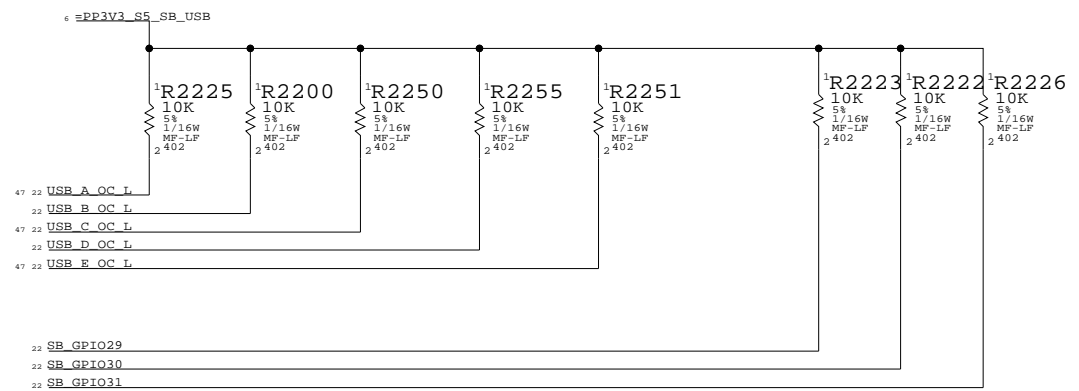
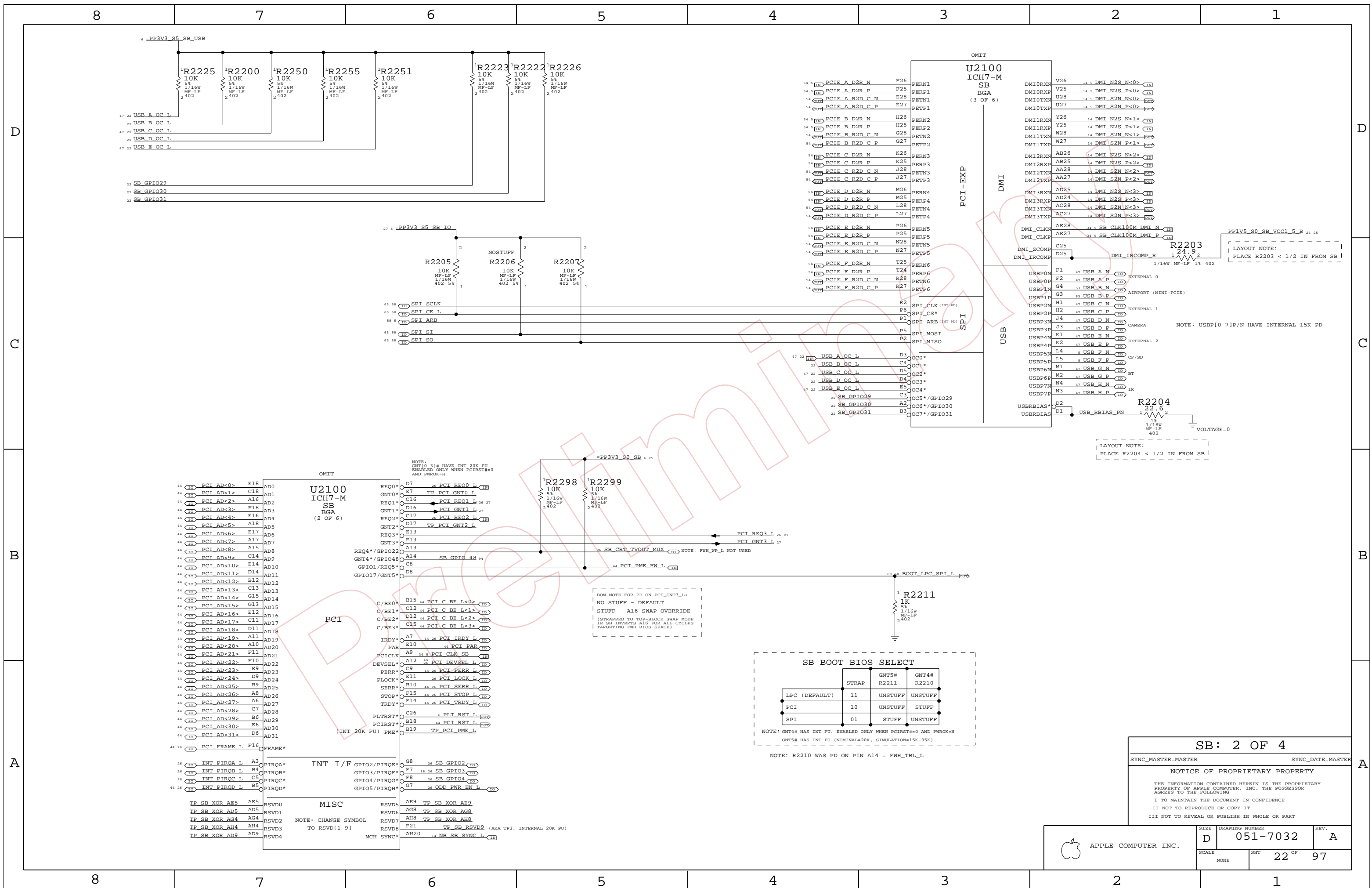
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SB: 2 OF 4

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

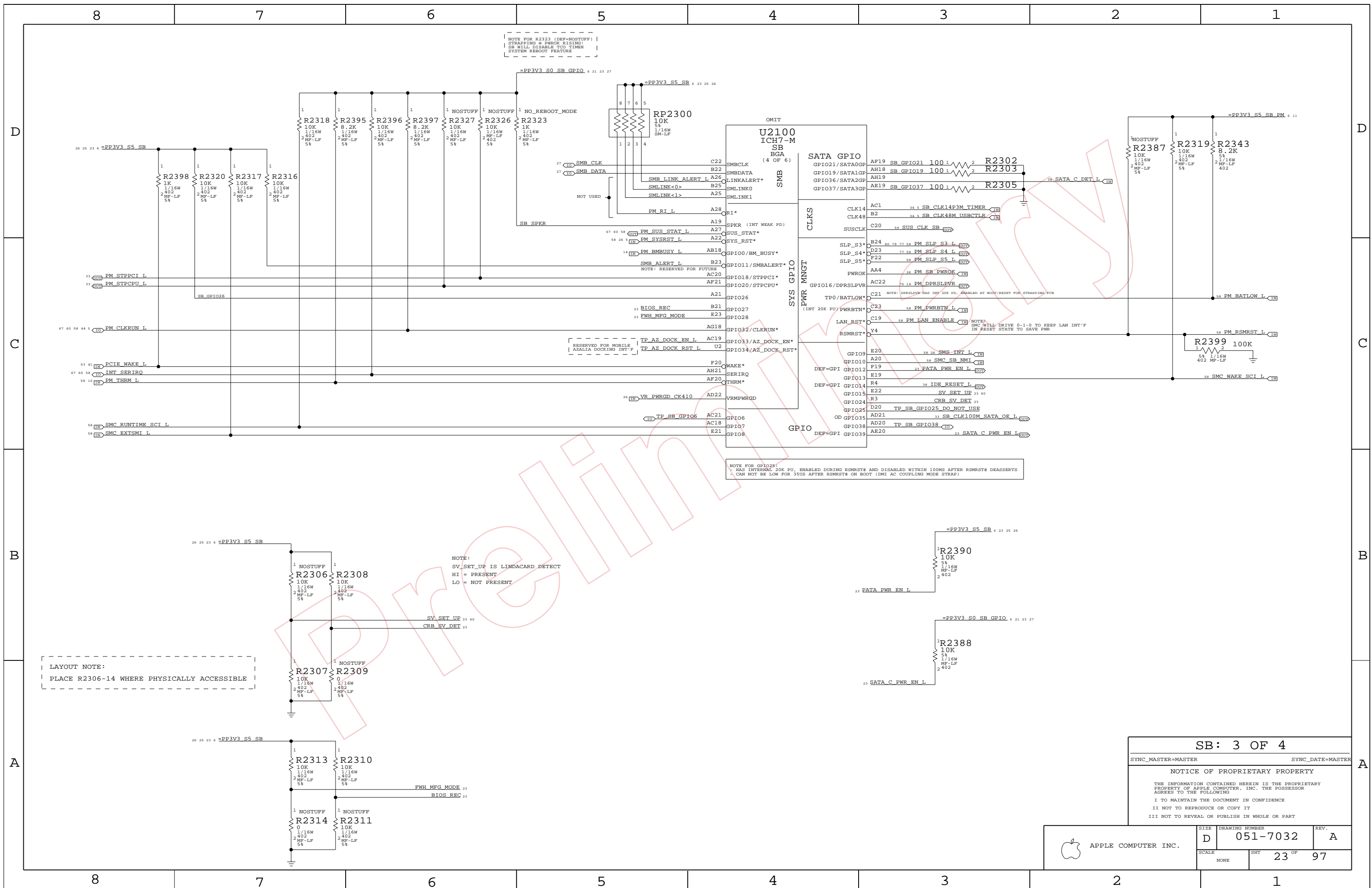
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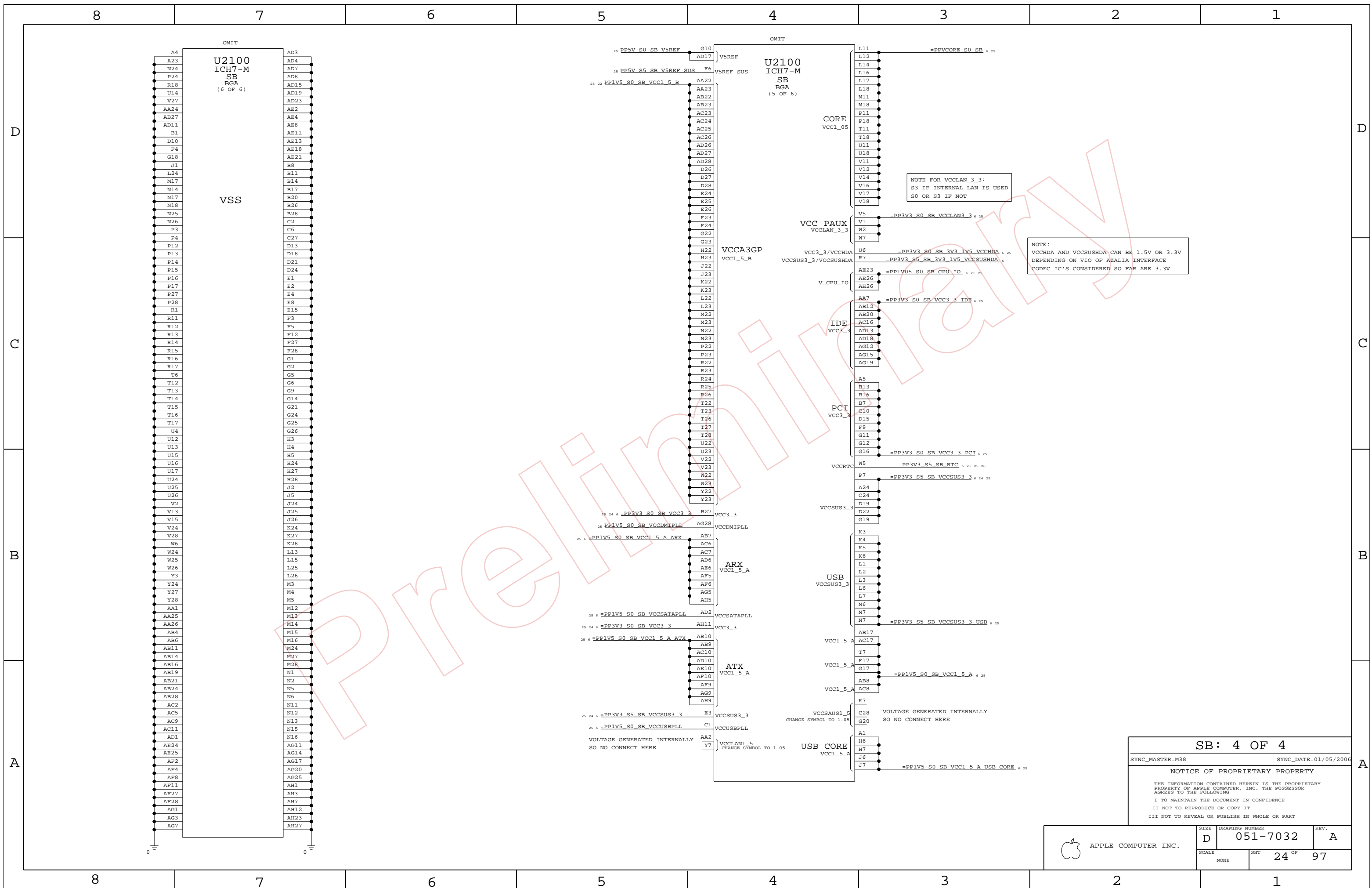
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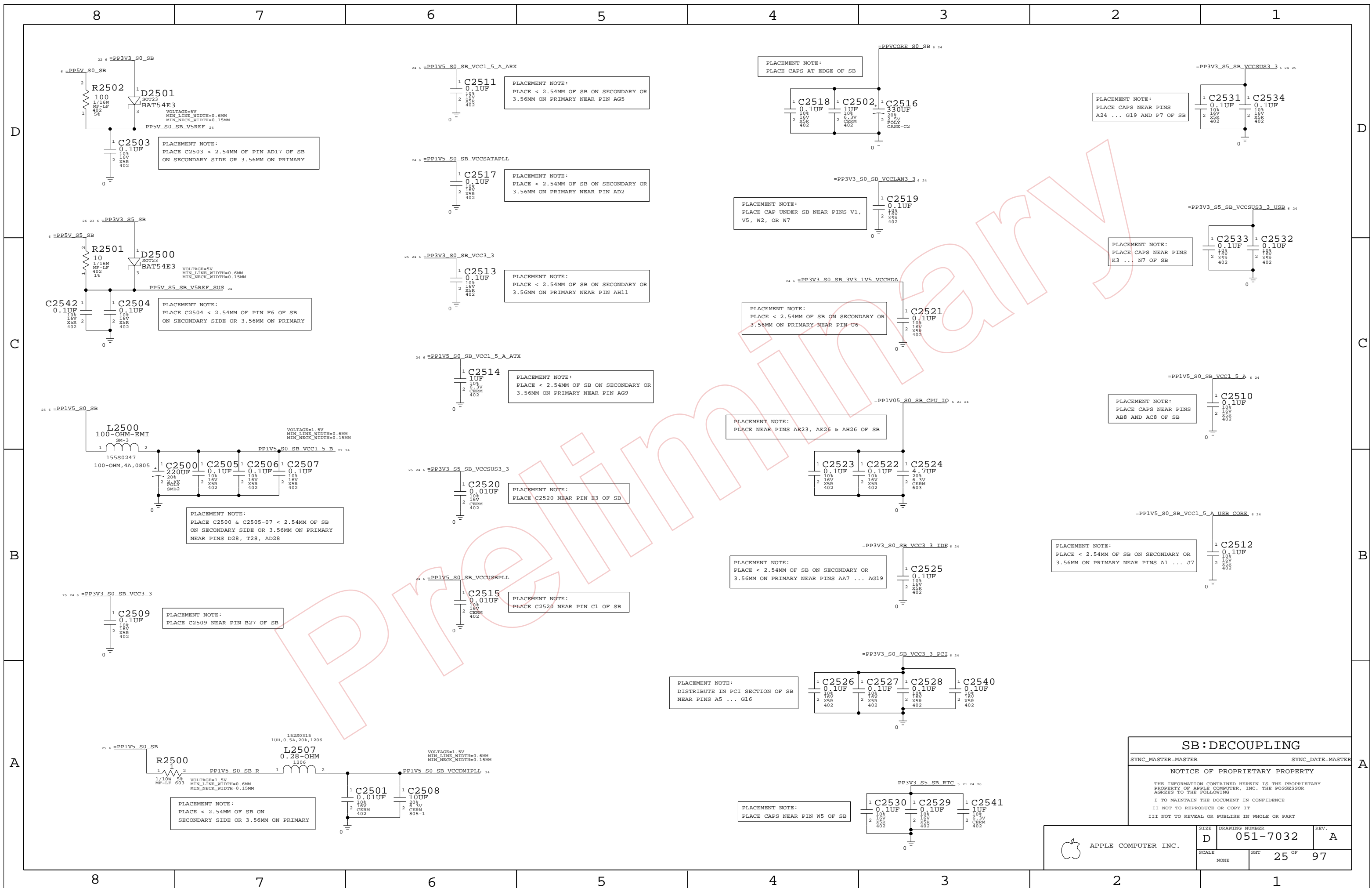
NOTE FOR VCCLAN\_3\_3:  
S3 IF INTERNAL LAN IS USED  
S0 OR S3 IF NOT

NOTE:  
VCCCHDA AND VCCSUS3\_3 CAN BE 1.5V OR 3.3V  
DEPENDING ON VIO OF AZALIA INTERFACE  
CODIC IC'S CONSIDERED SO FAR ARE 3.3V

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NONE			





**SB: DECOUPLING**

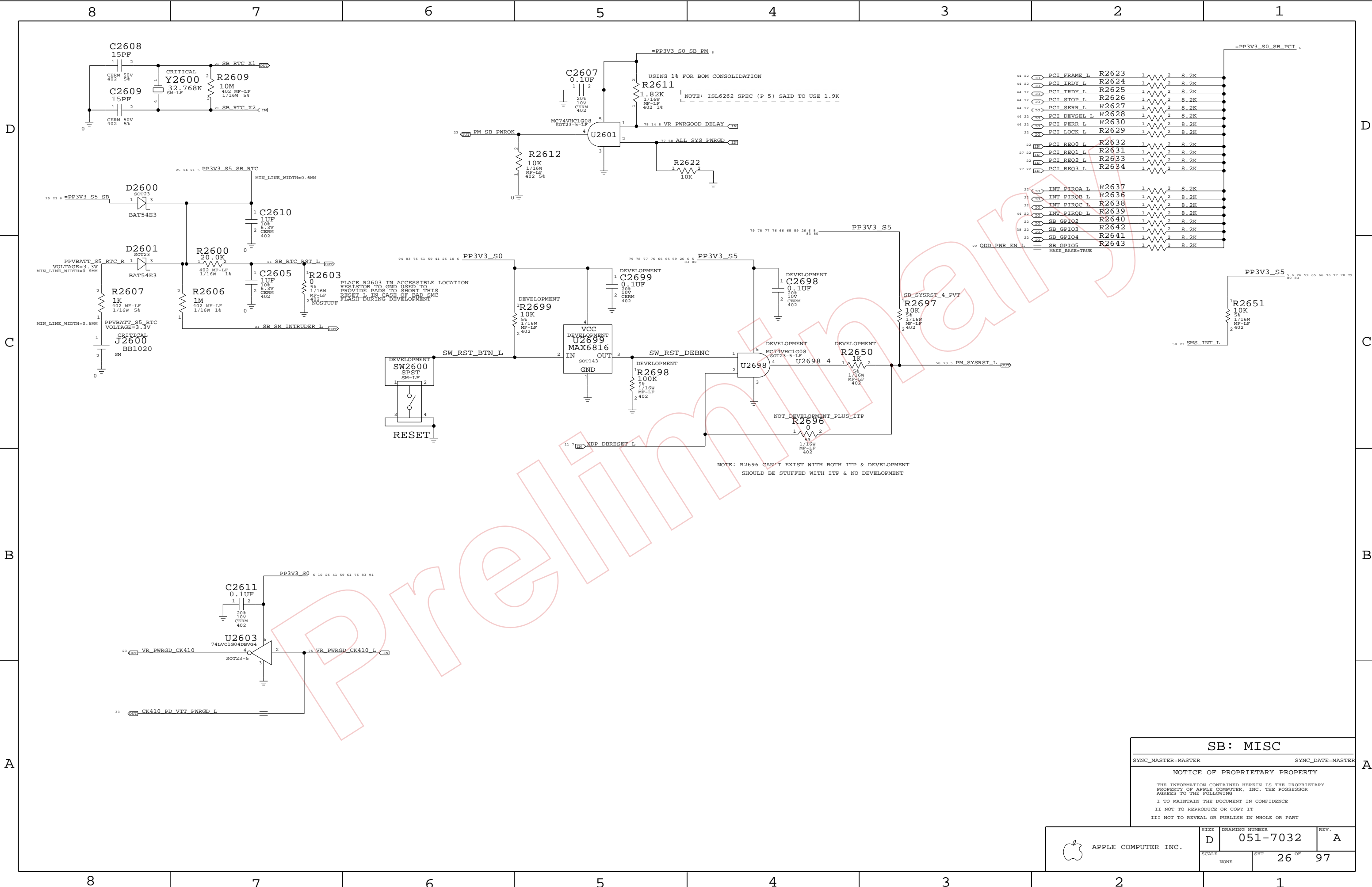
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NONE			



**SB: MISC**

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SCALE	SHT	26 OF	97
NONE			

8

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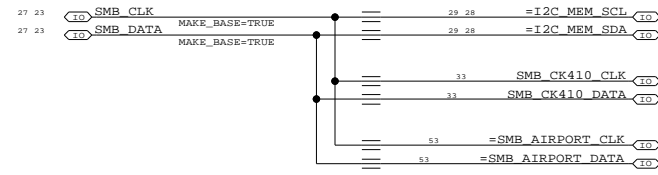
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1

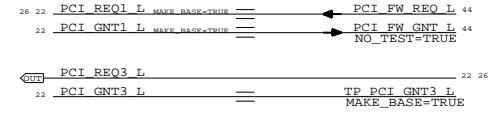
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D

### SB I2C BUSSES

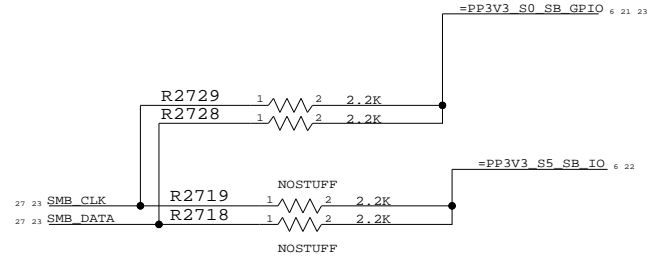


### PCI CONTROL



C

C



B

B

Preliminary

A

A

### SB: SMB HUB AND ALIAS

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	SCALE NONE	SHEET 27 OF 97	

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7

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5

4

3

2

1

# Page Notes

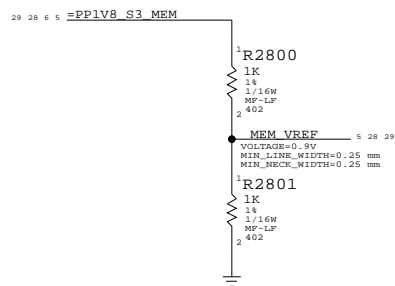
Power aliases required by this page:  
 - =PPIV8\_S3\_MEM  
 - =PPSPD\_S0\_MEM (2.5V - 3.3V)

Signal aliases required by this page:  
 - =I2C\_MEM\_SCL  
 - =I2C\_MEM\_SDA

BOM options provided by this page:  
 (NONE)

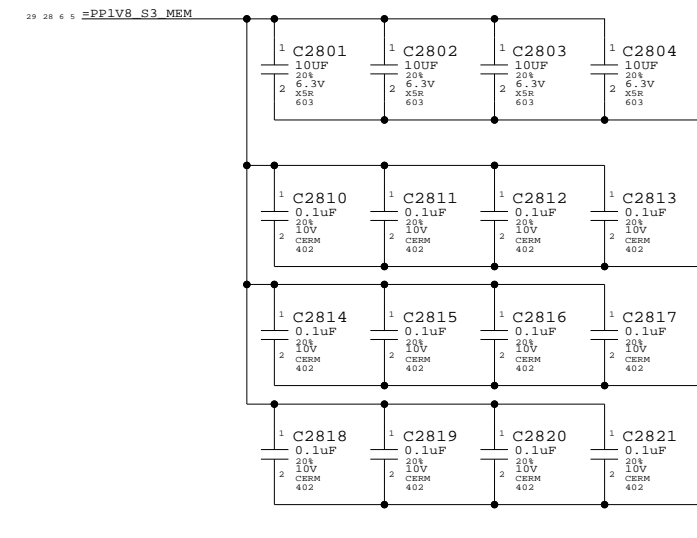
## DDR2 VRef

One 0.1uF per connector



## DDR2 Bypass Caps

(For return current)



**DDR2 SO-DIMM Connector A**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. A
	SCALE NONE	SHEET 28 OF 97	

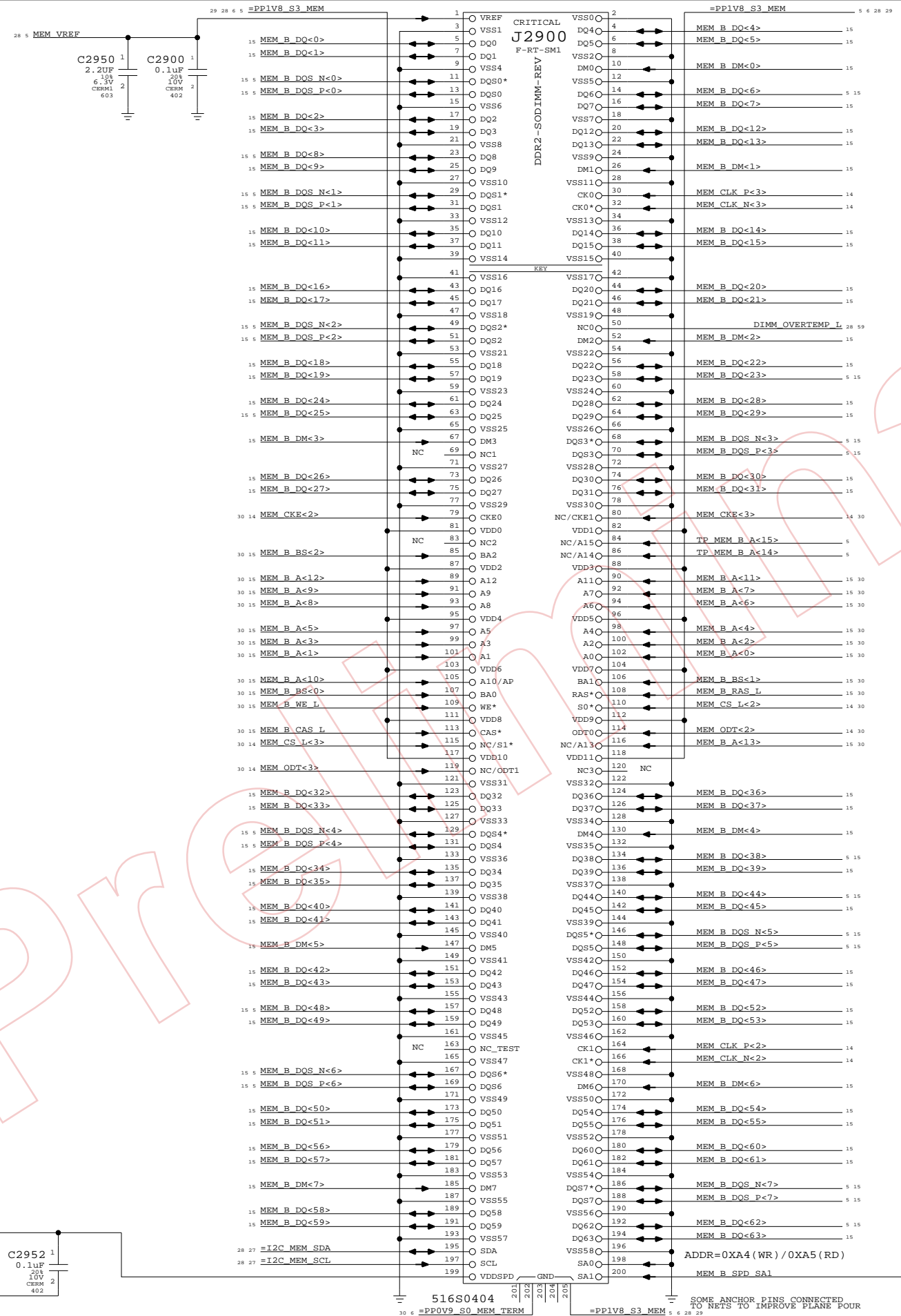
# Page Notes

Power aliases required by this page:  
- =PP1V8\_S3\_MEM  
- =PPSPD\_S0\_MEM (2.5V - 3.3V)

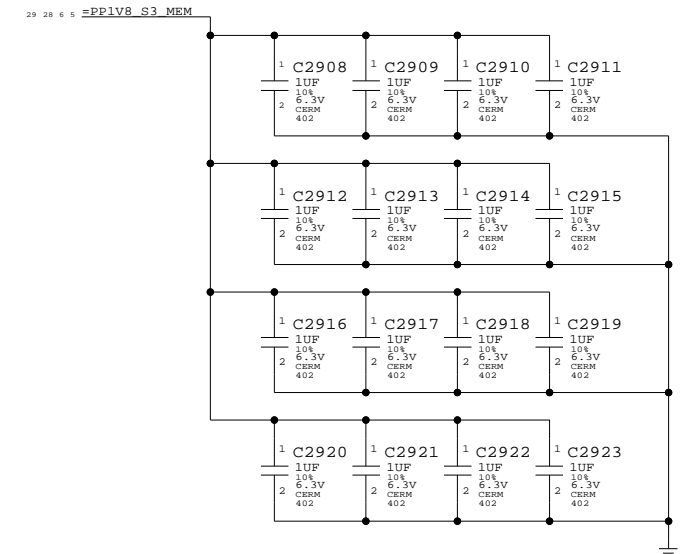
Signal aliases required by this page:  
- =I2C\_MEM\_SCL  
- =I2C\_MEM\_SDA

BOM options provided by this page:  
(NONE)

NOTE: This page does not supply VREF.  
The reference voltage must be provided by another page.



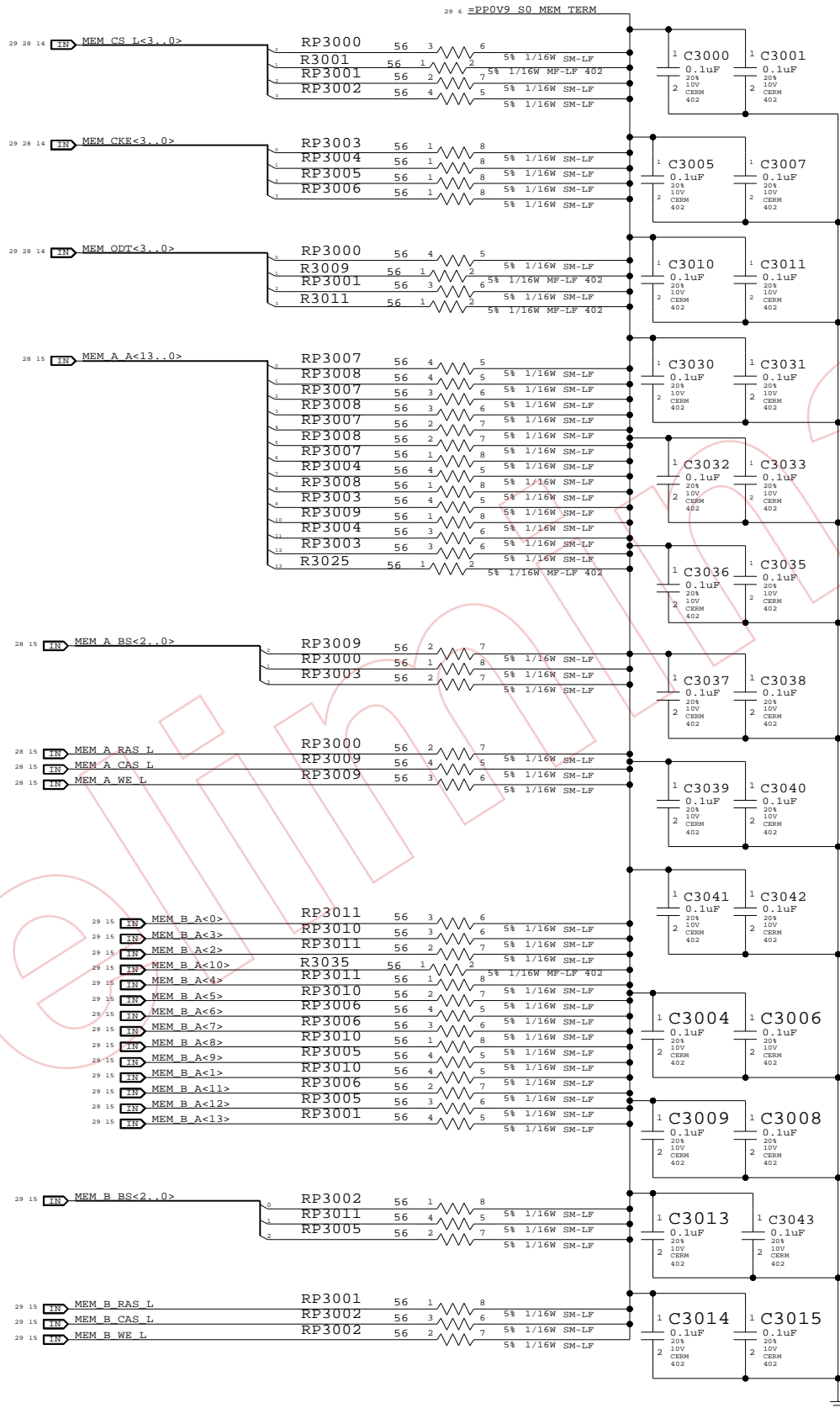
## DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B	
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	D	051-7032	A
SCALE	SHT	29 OF	97
NONE			

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it



PRELIMINARY

Memory Active Termination

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	D	051-7032	A
SCALE	SHT	30 OF 97	
NONE			

Page Notes

Power aliases required by this page:  
 - =PP5V\_S0\_MEMVTT  
 - =PP1V8\_S0\_MEMVTT  
 - =PP0V9\_S0\_MEMVTT\_LDO

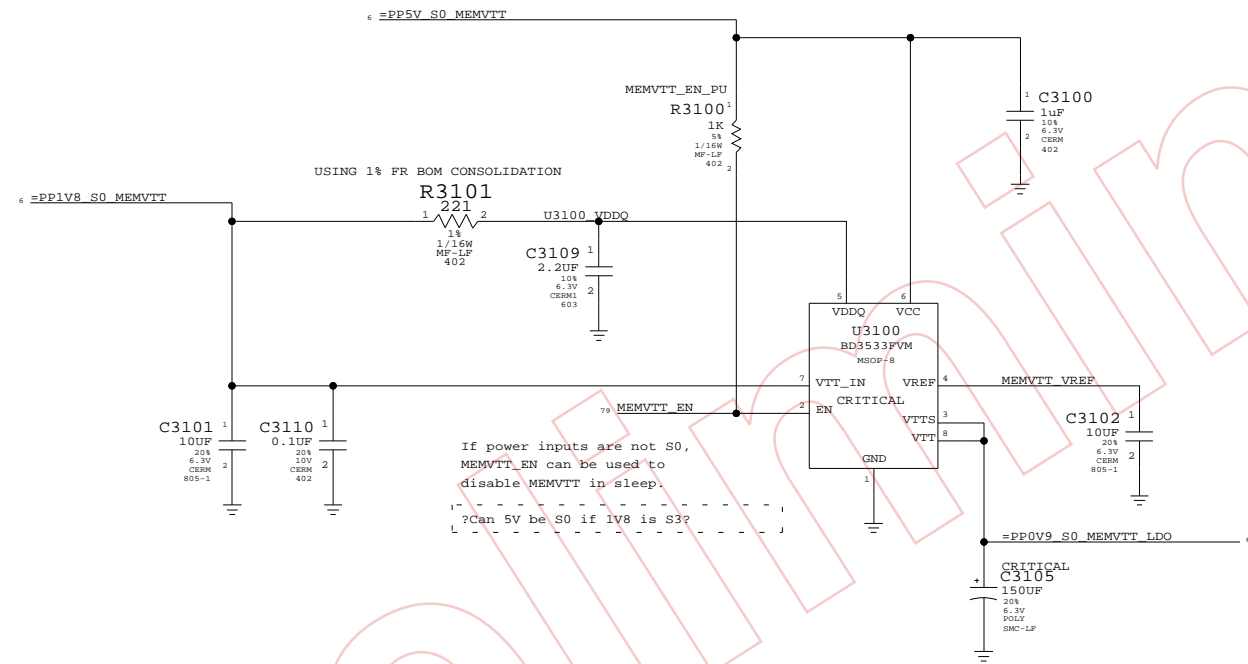
---

Signal aliases required by this page:  
 (NONE)

---

BOM options provided by this page:  
 (NONE)

DDR2 Vtt Regulator

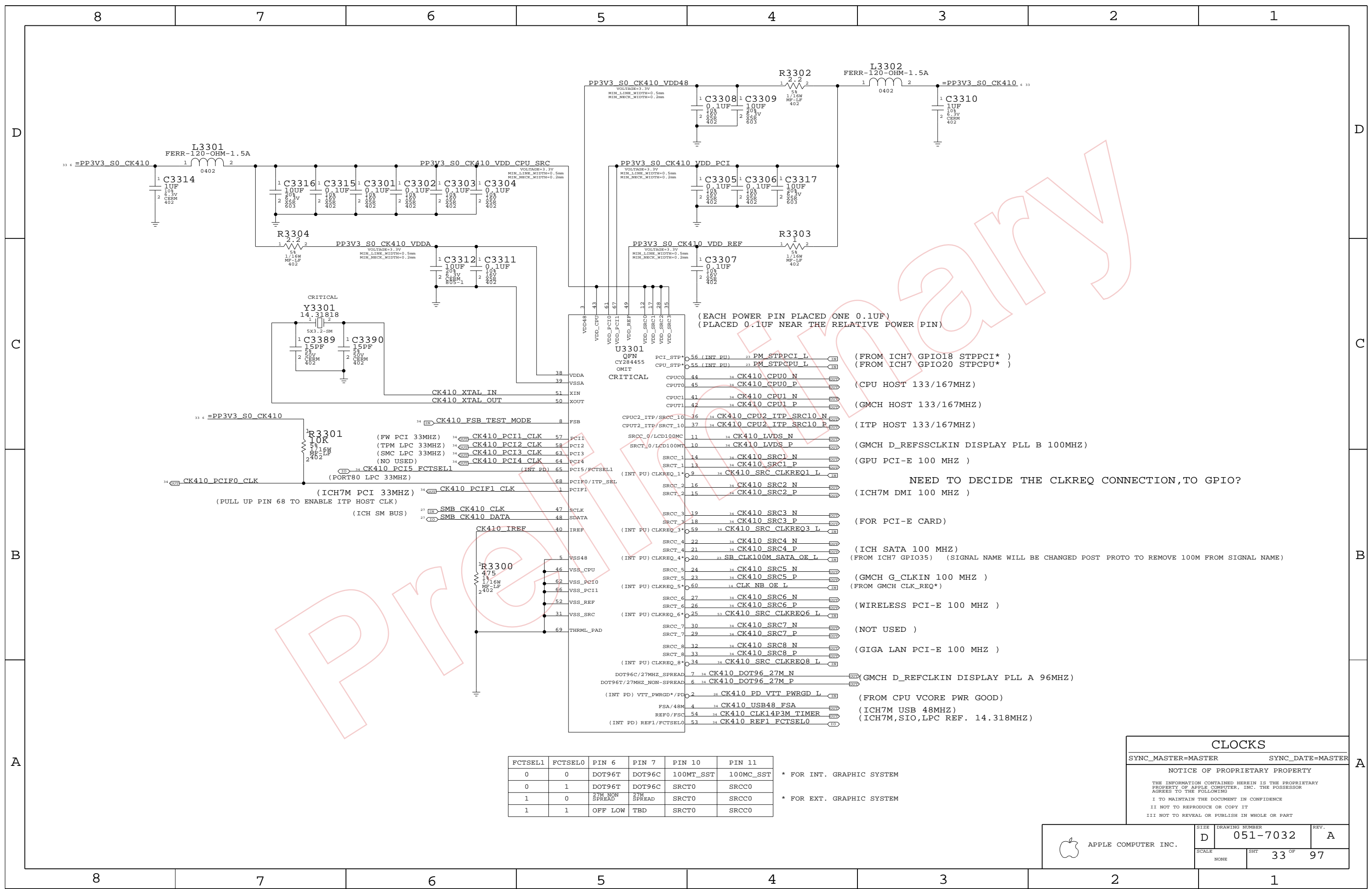


Preliminary

Memory Vtt Supply  
 SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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	D	051-7032	A
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) 23 PM\_STPPCI\_L (FROM ICH7 GPIO18 STPPCI\*)
- 55 (INT PU) 23 PM\_STPCPU\_L (FROM ICH7 GPIO20 STPCPU\*)
- 44 34 CK410\_CPU0\_N (CPU HOST 133/167MHZ)
- 45 34 CK410\_CPU0\_P
- 41 34 CK410\_CPU1\_N (GMCH HOST 133/167MHZ)
- 42 34 CK410\_CPU1\_P
- 36 34 CK410\_CPU2\_ITP\_SRC10\_N (ITP HOST 133/167MHZ)
- 37 34 CK410\_CPU2\_ITP\_SRC10\_P
- 11 34 CK410\_LVDS\_N (GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 10 34 CK410\_LVDS\_P
- 14 34 CK410\_SRC1\_N (GPU PCI-E 100 MHZ)
- 13 34 CK410\_SRC1\_P
- 9 34 CK410\_SRC\_CLKREQ1\_L NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?
- 16 34 CK410\_SRC2\_N (ICH7M DMI 100 MHZ)
- 15 34 CK410\_SRC2\_P
- 19 34 CK410\_SRC3\_N (FOR PCI-E CARD)
- 18 34 CK410\_SRC3\_P
- 59 34 CK410\_SRC\_CLKREQ3\_L (ICH SATA 100 MHZ)
- 22 34 CK410\_SRC4\_N (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 21 34 CK410\_SRC4\_P
- 20 34 SB\_CLK100M\_SATA\_OE\_L
- 24 34 CK410\_SRC5\_N (GMCH G\_CLKIN 100 MHZ)
- 23 34 CK410\_SRC5\_P (FROM GMCH CLK\_REQ\*)
- 60 34 CLK\_NB\_OE\_L
- 27 34 CK410\_SRC6\_N (WIRELESS PCI-E 100 MHZ)
- 26 34 CK410\_SRC6\_P
- 25 34 CK410\_SRC\_CLKREQ6\_L
- 30 34 CK410\_SRC7\_N (NOT USED)
- 29 34 CK410\_SRC7\_P
- 32 34 CK410\_SRC8\_N (GIGA LAN PCI-E 100 MHZ)
- 33 34 CK410\_SRC8\_P
- 34 34 CK410\_SRC\_CLKREQ8\_L
- 7 34 CK410\_DOT96\_27M\_N (GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)
- 6 34 CK410\_DOT96\_27M\_P
- 2 34 CK410\_PD\_VTT\_PWRGD\_L (FROM CPU VCORE PWR GOOD)
- 4 34 CK410\_USB48\_FSA (ICH7M USB 48MHZ)
- 54 34 CK410\_CLK14P3M\_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 53 34 CK410\_REF1\_FCTSEL0

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0
1	1	OFF_LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM  
\* FOR EXT. GRAPHIC SYSTEM

**CLOCKS**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

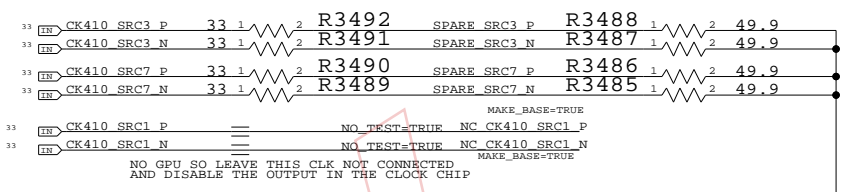
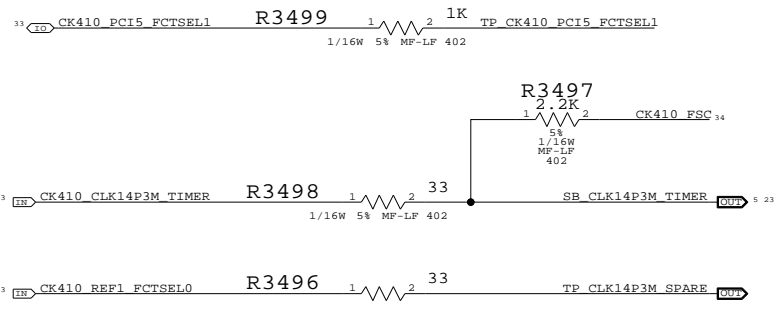
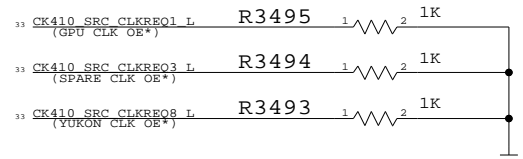
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	D	051-7032	A
SCALE	SHT	33 OF 97	
NONE			

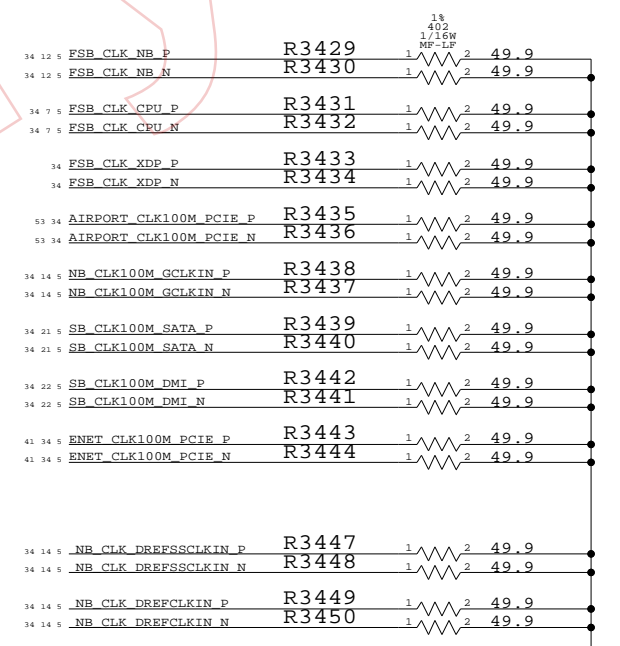
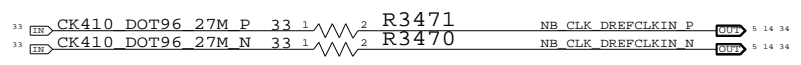
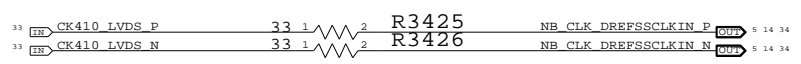
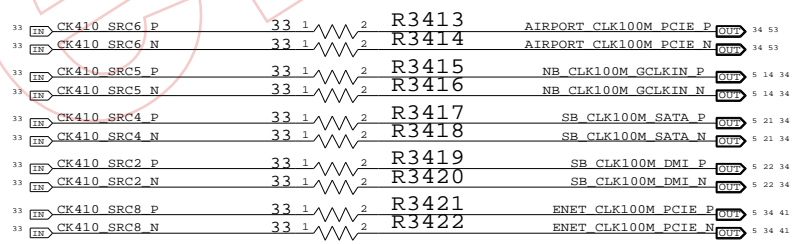
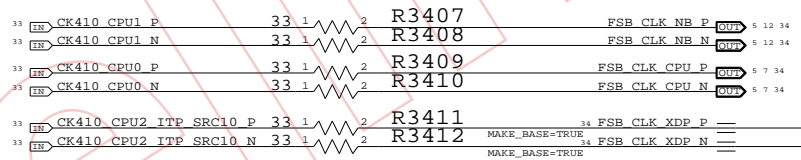
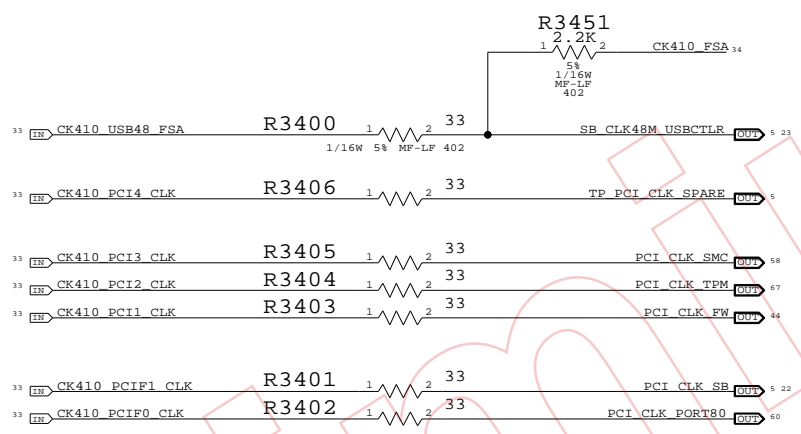
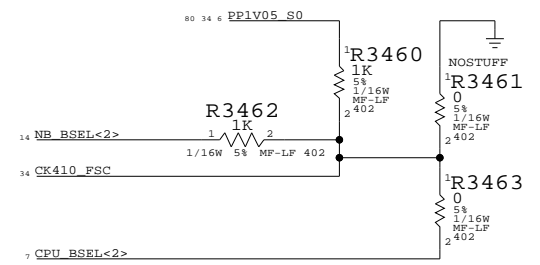
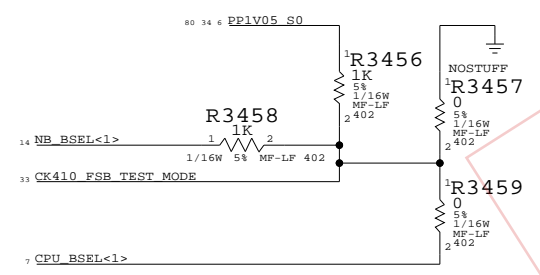
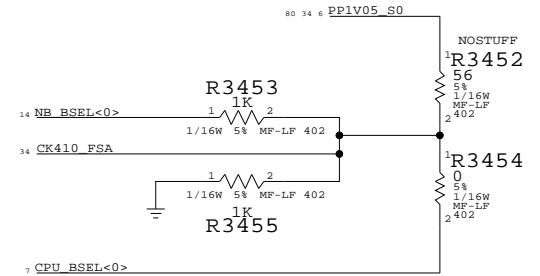


NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3452 R3451 R3457
533MHZ (133MHZ CPU CLK)	R3453 R3454 R3455	R3452 R3451 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3451 R3457	R3453 R3454 R3455



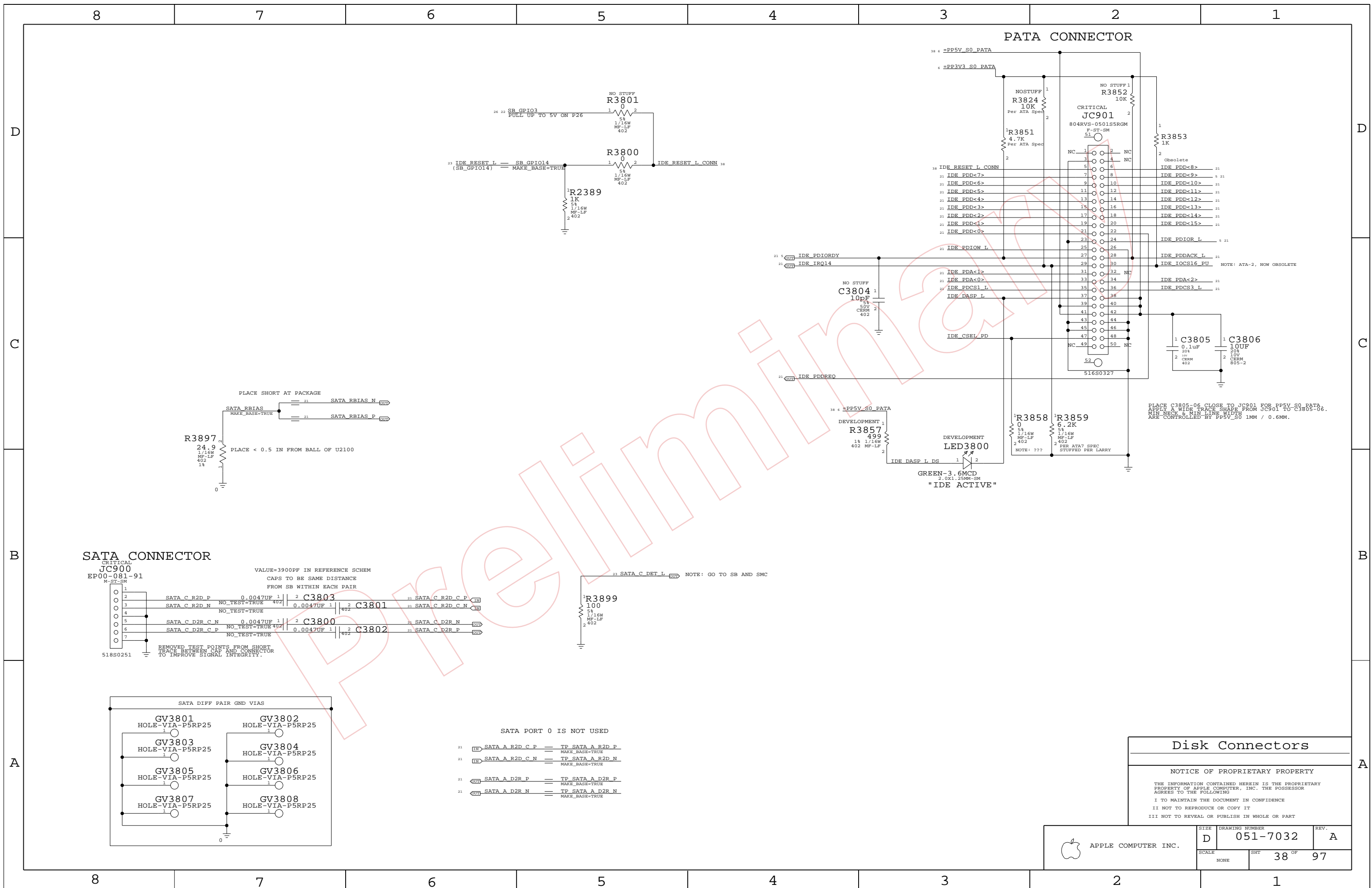
**CLOCKS: TERMINATIONS**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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	D	051-7032	A
SCALE	SHT	34 OF 97	
NONE			



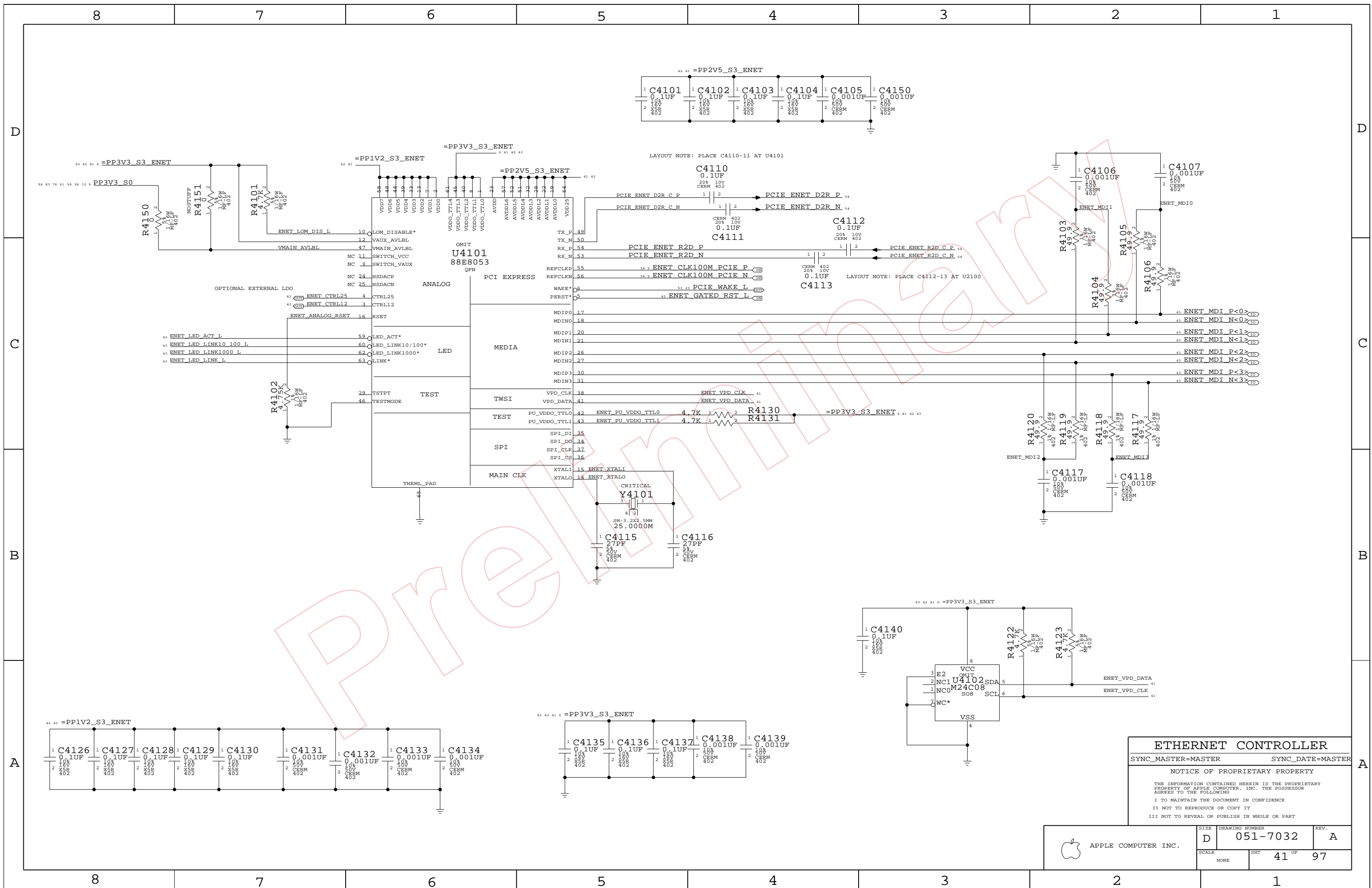
**Disk Connectors**

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	SCALE NONE	SHT 38 OF 97	



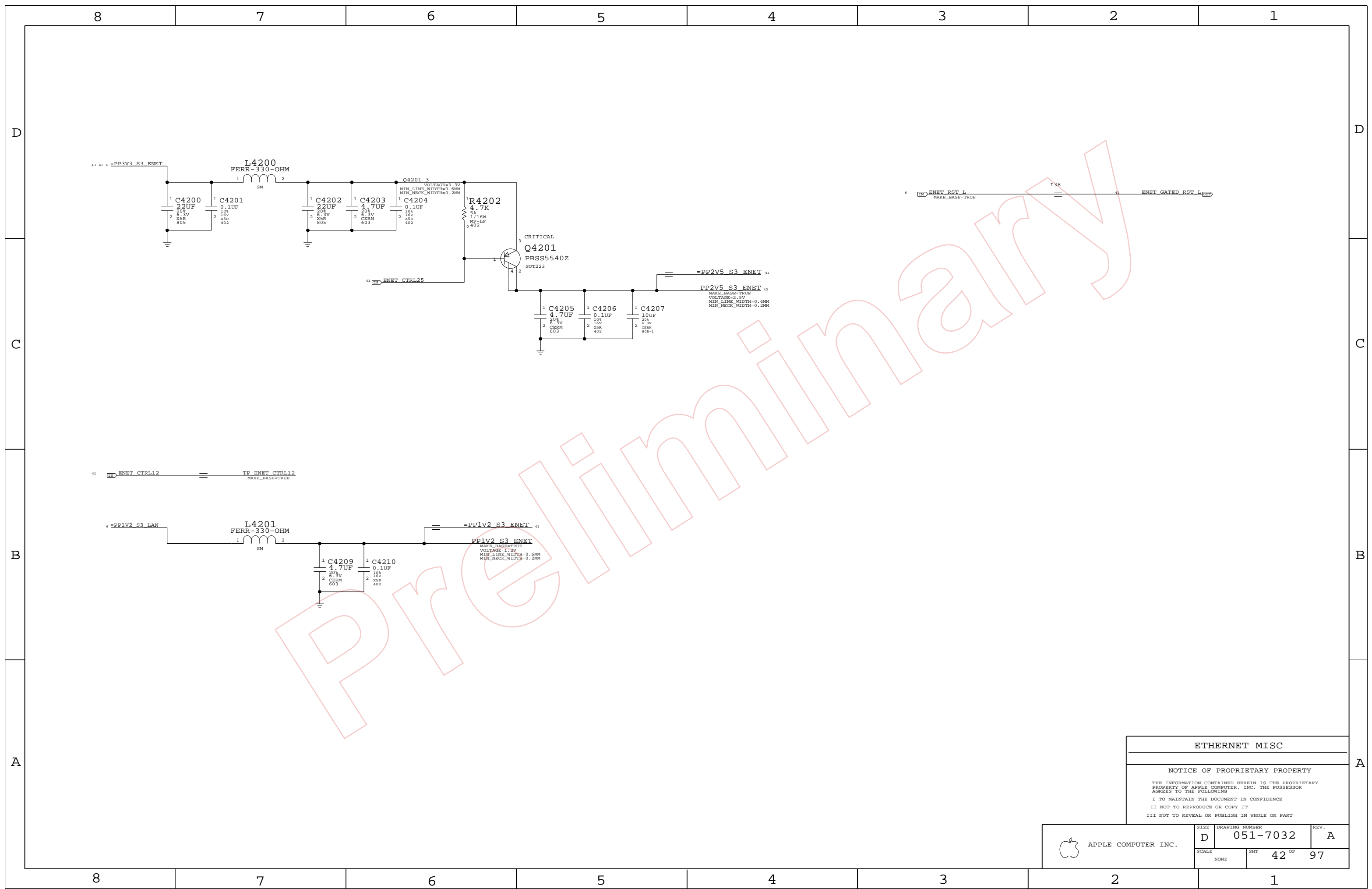
**ETHERNET CONTROLLER**

SYNC\_MASTER=MASTER SYNC\_DATA=MASTER

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	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

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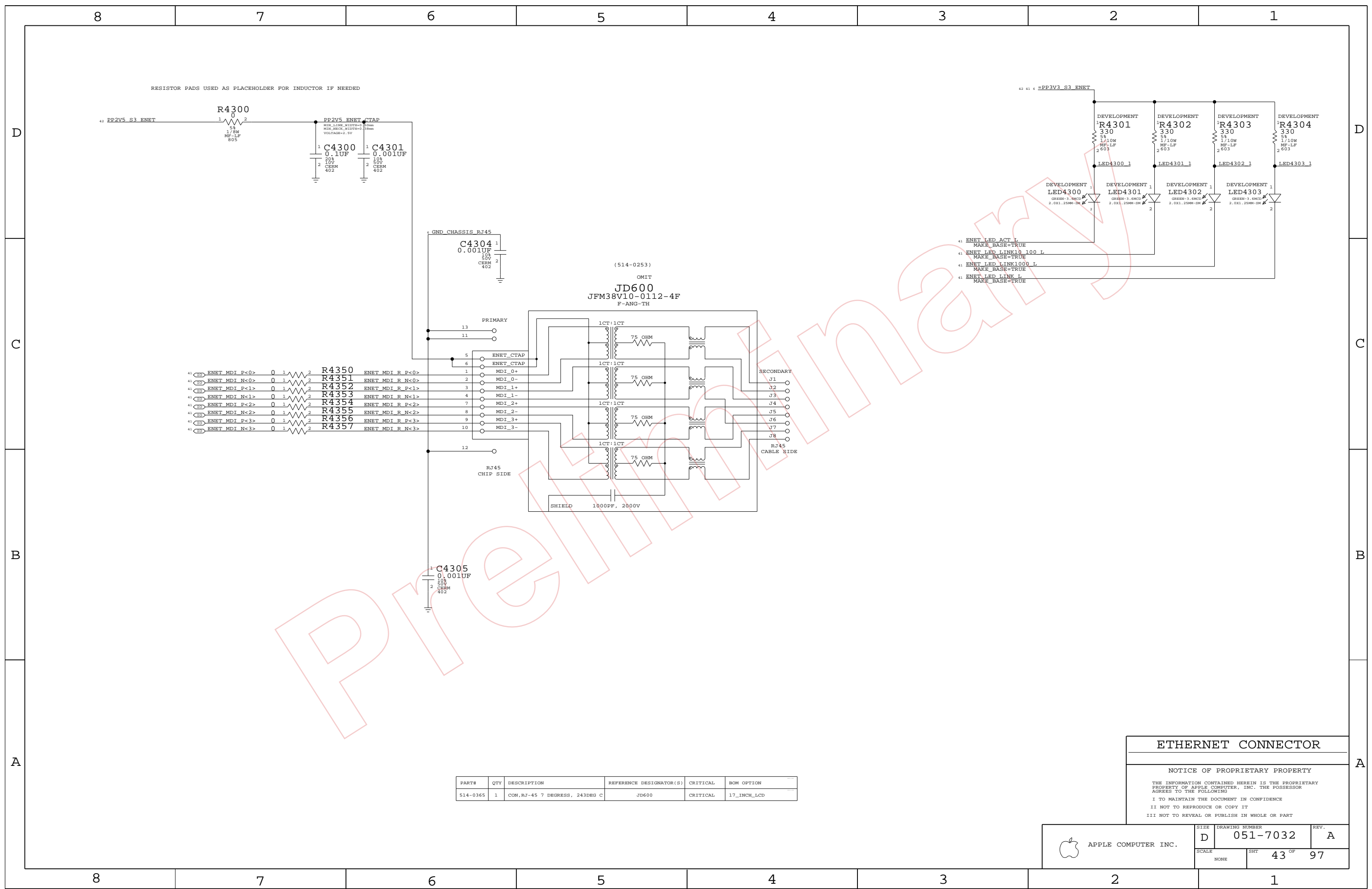
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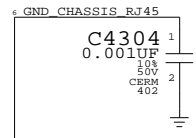
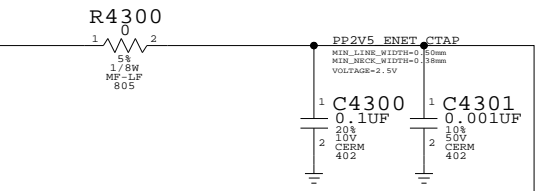
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

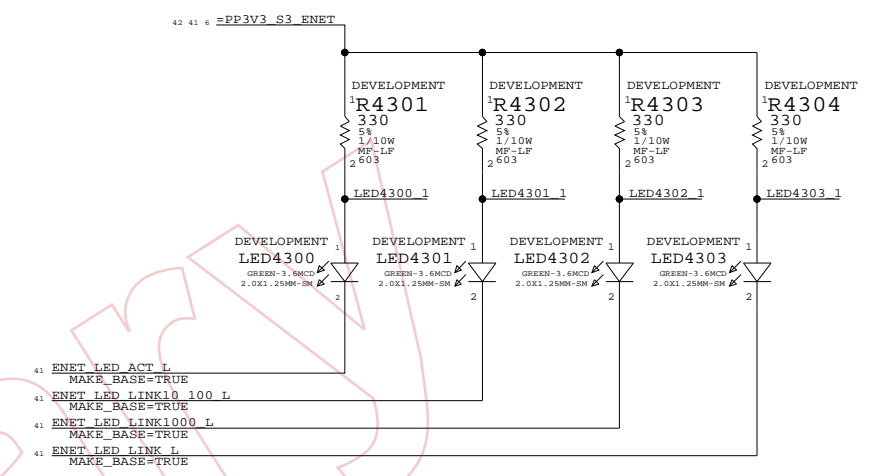
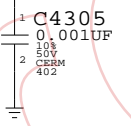
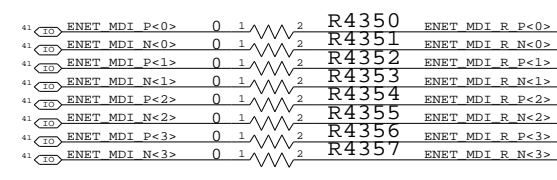
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>A</b>
	SCALE NONE	SHEET 42 OF 97	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



(514-0253)  
OMIT  
JD600  
JFM38V10-0112-4F  
F-ANG-TH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

**ETHERNET CONNECTOR**

NOTICE OF PROPRIETARY PROPERTY

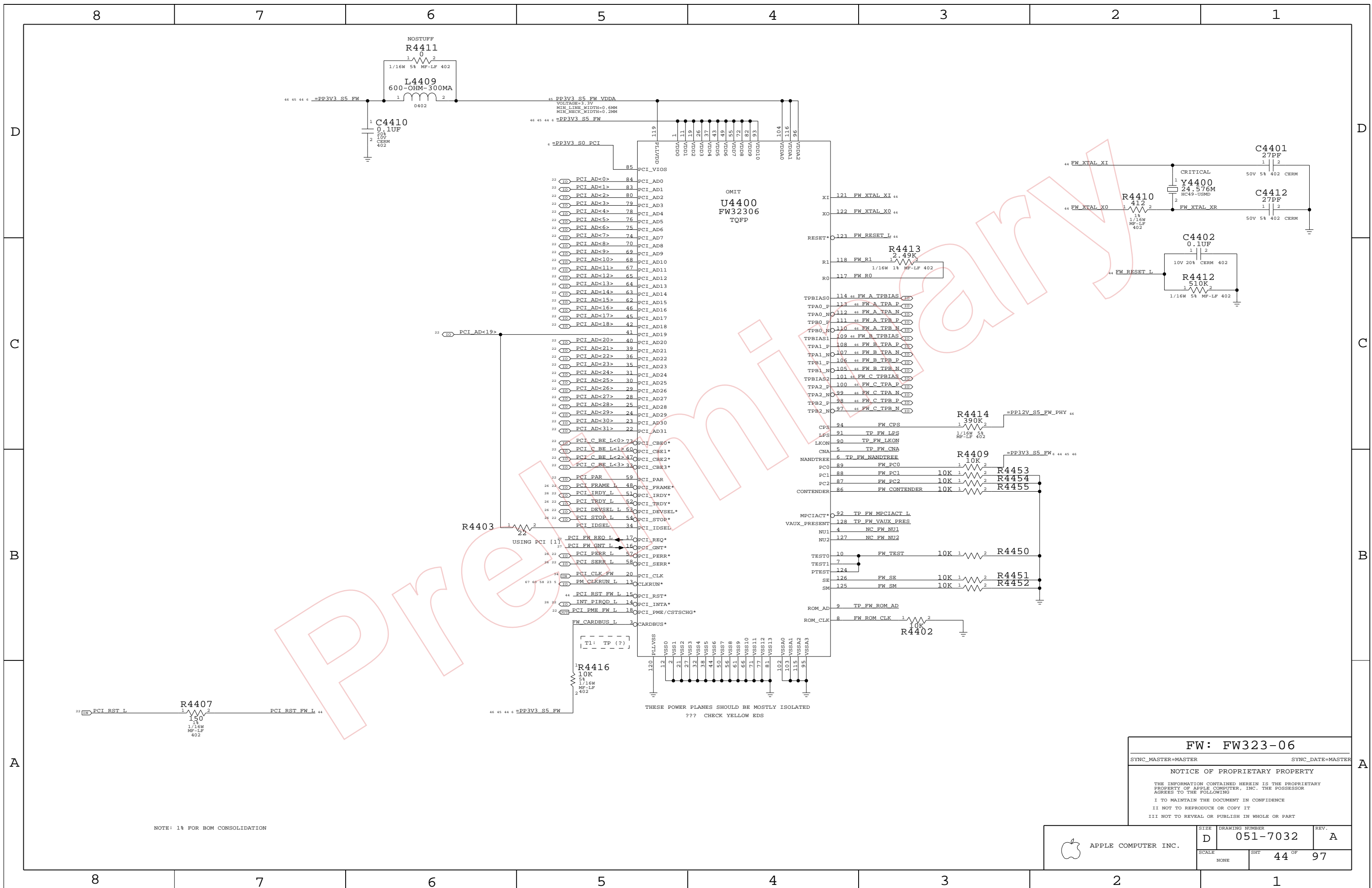
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	D	051-7032	A
SCALE	SHT	43 OF 97	
NONE			



PRELIMINARY

THESE POWER PLANES SHOULD BE MOSTLY ISOLATED  
 ??? CHECK YELLOW EDS

NOTE: 1% FOR BOM CONSOLIDATION

**FW: FW323-06**

SYNC\_MASTER=MASTER      SYNC\_DATE=MASTER

**NOTICE OF PROPRIETARY PROPERTY**

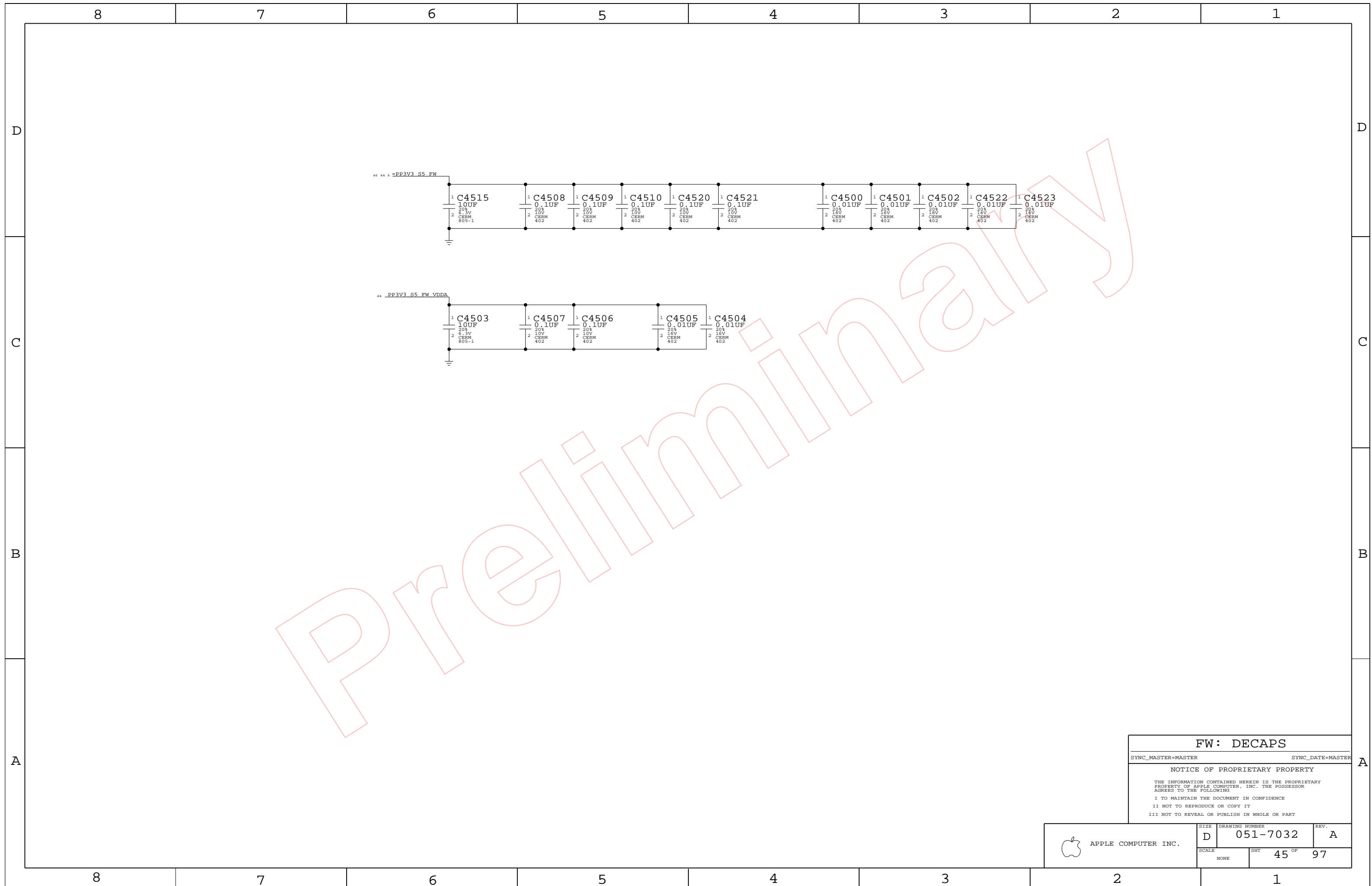
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	D	051-7032	A
SCALE	SHT	44 OF 97	
NONE			



Preliminary

**FW: DECAPS**

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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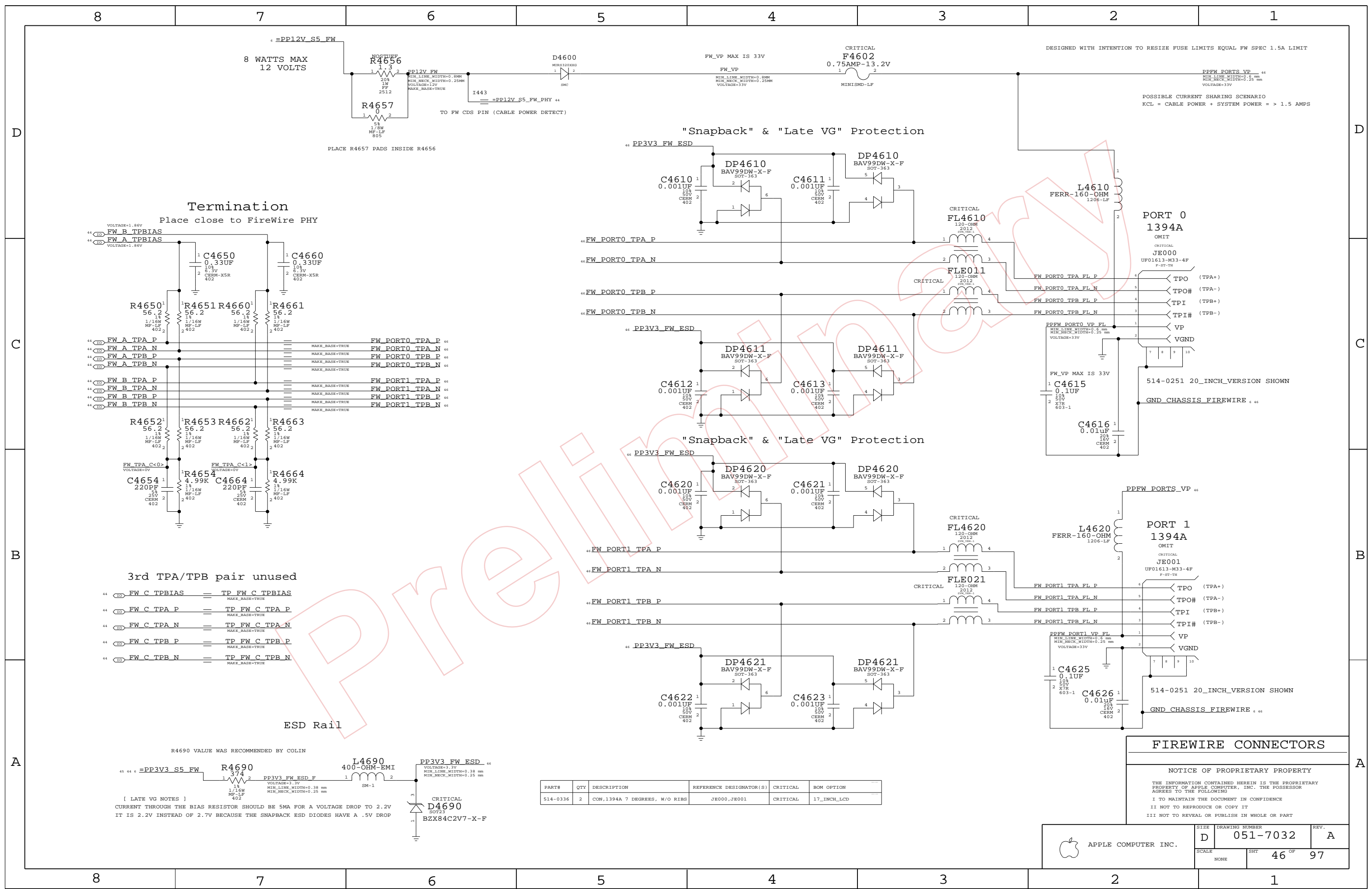
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	SCALE NONE	SHIT 45 OF 97	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

**FIREWIRE CONNECTORS**

**NOTICE OF PROPRIETARY PROPERTY**

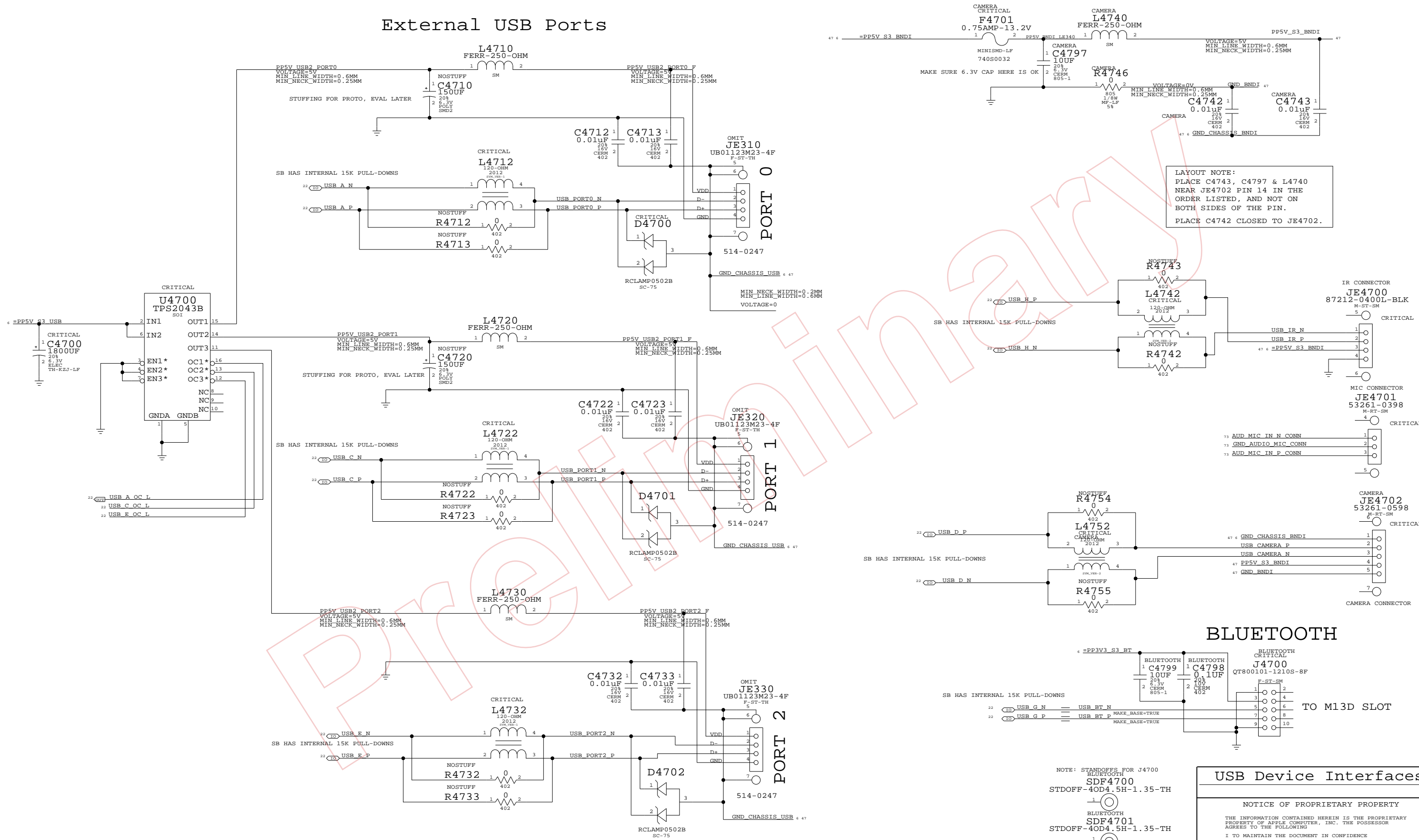
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	SCALE NONE	SHEET <b>46</b> OF <b>97</b>	

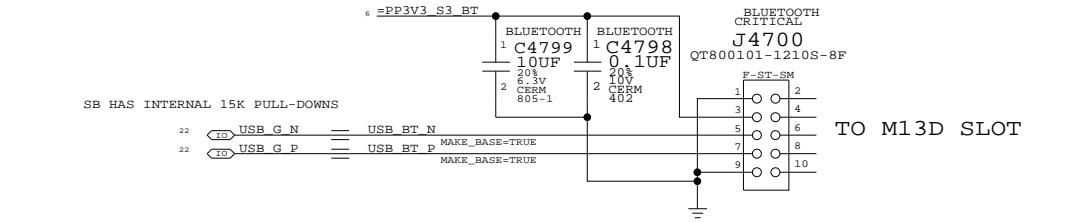


# External USB Ports



LAYOUT NOTE:  
 PLACE C4743, C4797 & L4740  
 NEAR JE4702 PIN 14 IN THE  
 ORDER LISTED, AND NOT ON  
 BOTH SIDES OF THE PIN.  
 PLACE C4742 CLOSED TO JE4702.

## BLUETOOTH



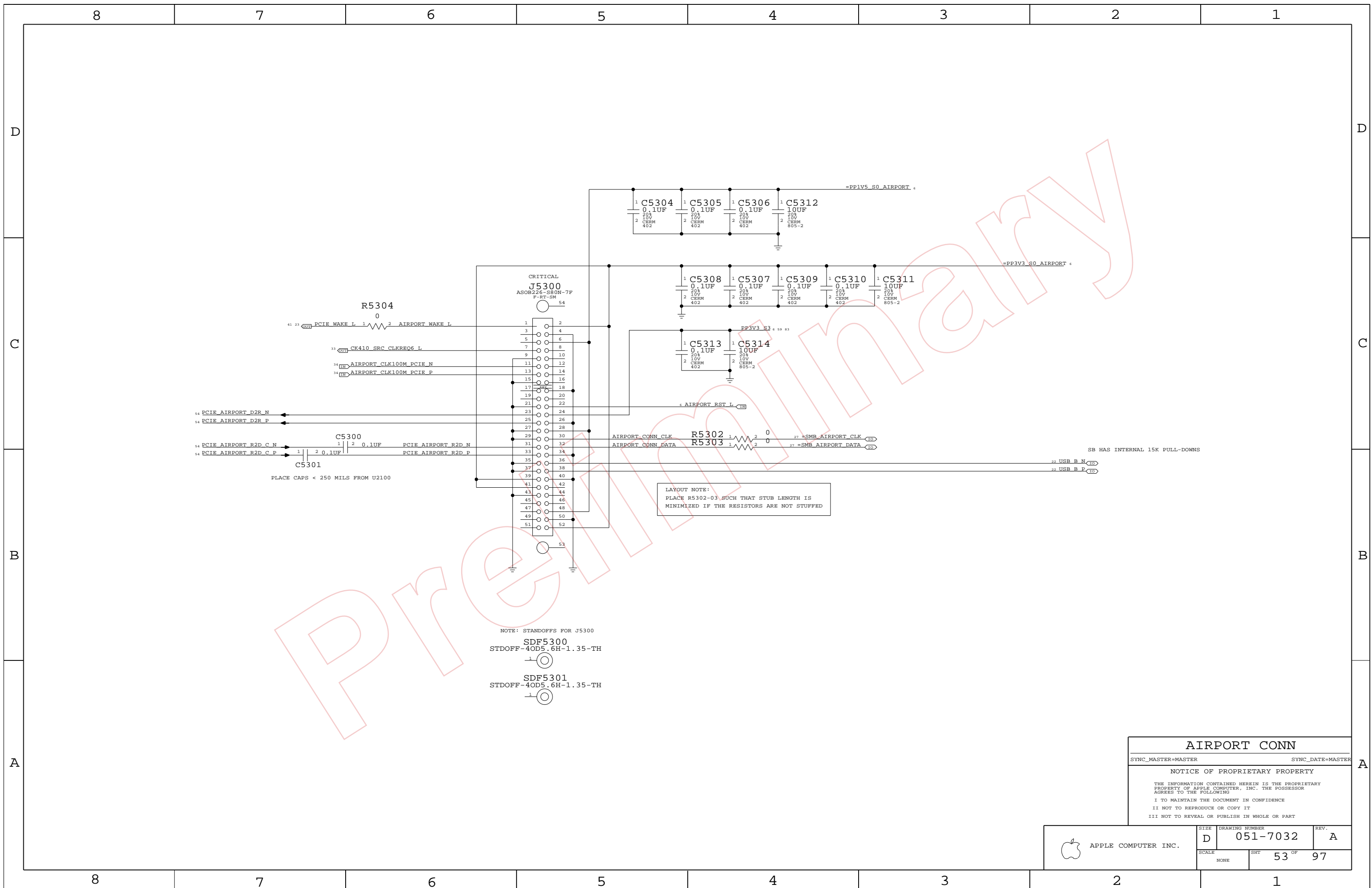
NOTE: STANDOFFS FOR J4700  
 BLUETOOTH  
 SDF4700  
 STDOFF-40D4.5H-1.35-TH  
 BLUETOOTH  
 SDF4701  
 STDOFF-40D4.5H-1.35-TH

## USB Device Interfaces



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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	47 OF 97	
NONE			



PROTECTED

NOTE: STANDOFFS FOR J5300  
 SDF5300  
 STDOFF-40D5.6H-1.35-TH  
  
 SDF5301  
 STDOFF-40D5.6H-1.35-TH  


LAYOUT NOTE:  
 PLACE R5302-03 SUCH THAT STUB LENGTH IS  
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

SB HAS INTERNAL 15K PULL-DOWNS

**AIRPORT CONN**

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	SCALE NONE	SHEET 53 OF 97	

8

7

6

5

4

3

2

1

D

D

C


C


B


B


A


A


22  PCIE C R2D C N == TP PCIE C R2D C N  
MAKE\_BASE=TRUE


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MAKE\_BASE=TRUE


22  PCIE C D2R N == TP PCIE C D2R N  
MAKE\_BASE=TRUE


22  PCIE C D2R P == TP PCIE C D2R P  
MAKE\_BASE=TRUE


22  PCIE D R2D C N == TP PCIE D R2D C N  
MAKE\_BASE=TRUE


22  PCIE D R2D C P == TP PCIE D R2D C P  
MAKE\_BASE=TRUE


22  PCIE D D2R N == TP PCIE D D2R N  
MAKE\_BASE=TRUE


22  PCIE D D2R P == TP PCIE D D2R P  
MAKE\_BASE=TRUE


22  PCIE E R2D C N == TP PCIE E R2D C N  
MAKE\_BASE=TRUE


22  PCIE E R2D C P == TP PCIE E R2D C P  
MAKE\_BASE=TRUE


22  PCIE E D2R N == TP PCIE E D2R N  
MAKE\_BASE=TRUE

22  PCIE E D2R P == TP PCIE E D2R P  
MAKE\_BASE=TRUE


22  PCIE F R2D C N == TP PCIE F R2D C N  
MAKE\_BASE=TRUE


22  PCIE F R2D C P == TP PCIE F R2D C P  
MAKE\_BASE=TRUE


22  PCIE F D2R N == TP PCIE F D2R N  
MAKE\_BASE=TRUE


22  PCIE F D2R P == TP PCIE F D2R P  
MAKE\_BASE=TRUE


USED PCIE PORTS


22  PCIE A R2D C N == PCIE AIRPORT R2D C N 53  
MAKE\_BASE=TRUE


22  PCIE A R2D C P == PCIE AIRPORT R2D C P 53  
MAKE\_BASE=TRUE


22 5  PCIE A D2R N == PCIE AIRPORT D2R N 53  
MAKE\_BASE=TRUE

22 5  PCIE A D2R P == PCIE AIRPORT D2R P 53  
MAKE\_BASE=TRUE

22  PCIE B R2D C N == PCIE ENET R2D C N 41  
MAKE\_BASE=TRUE

22  PCIE B R2D C P == PCIE ENET R2D C P 41  
MAKE\_BASE=TRUE

22 5  PCIE B D2R N == PCIE ENET D2R N 41  
MAKE\_BASE=TRUE

22 5  PCIE B D2R P == PCIE ENET D2R P 41  
MAKE\_BASE=TRUE

PCIE PORT ALIASES

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	A
SCALE	SHT	
NONE	54 OF 97	

8

7

6

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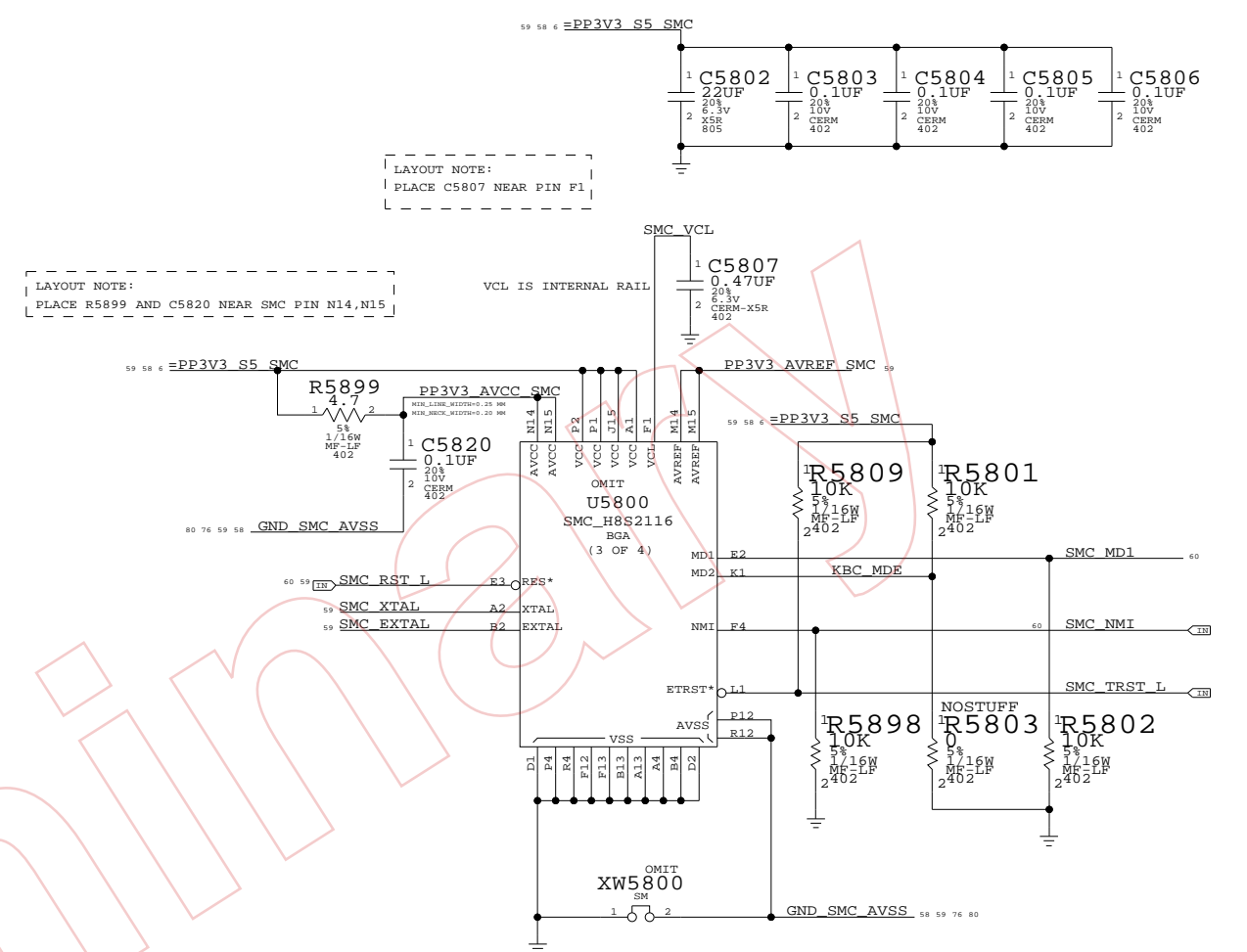
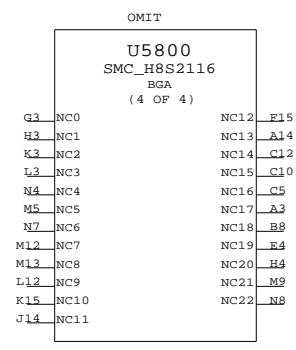
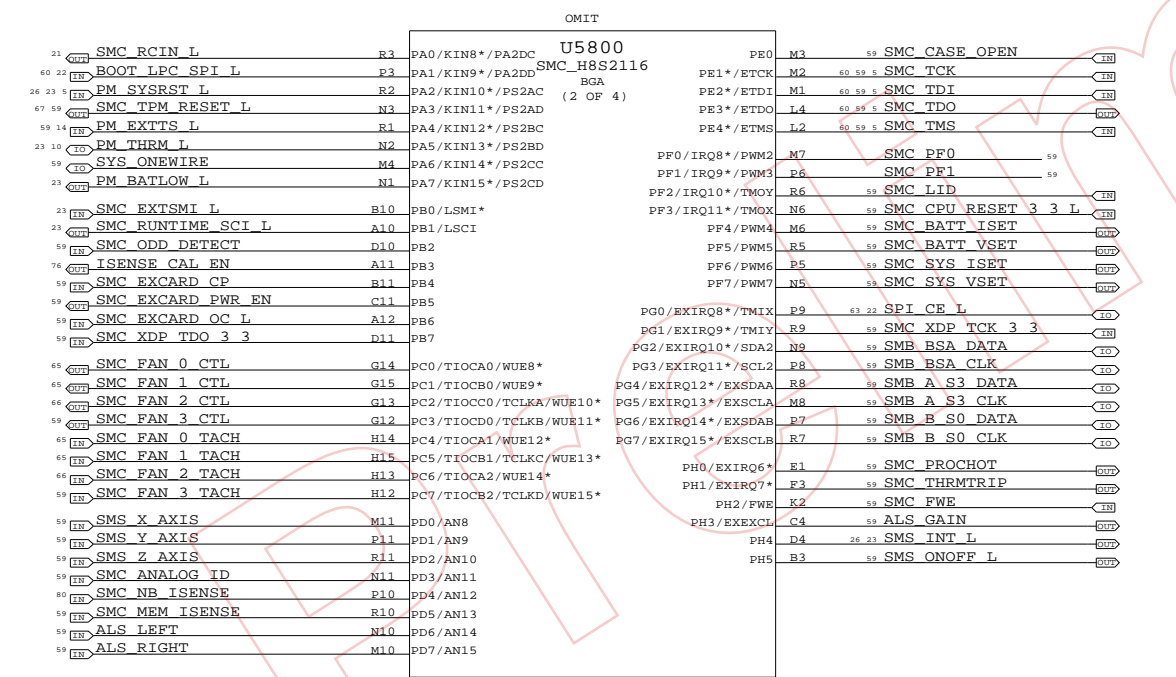
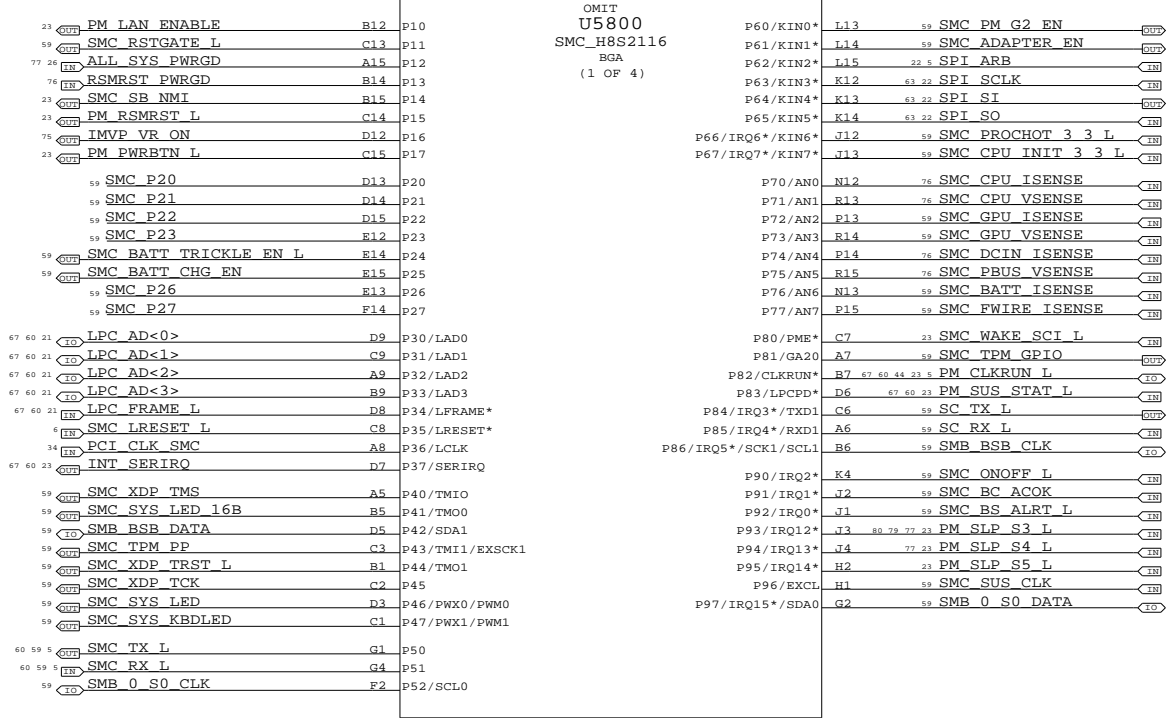
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC\_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



**SMC**

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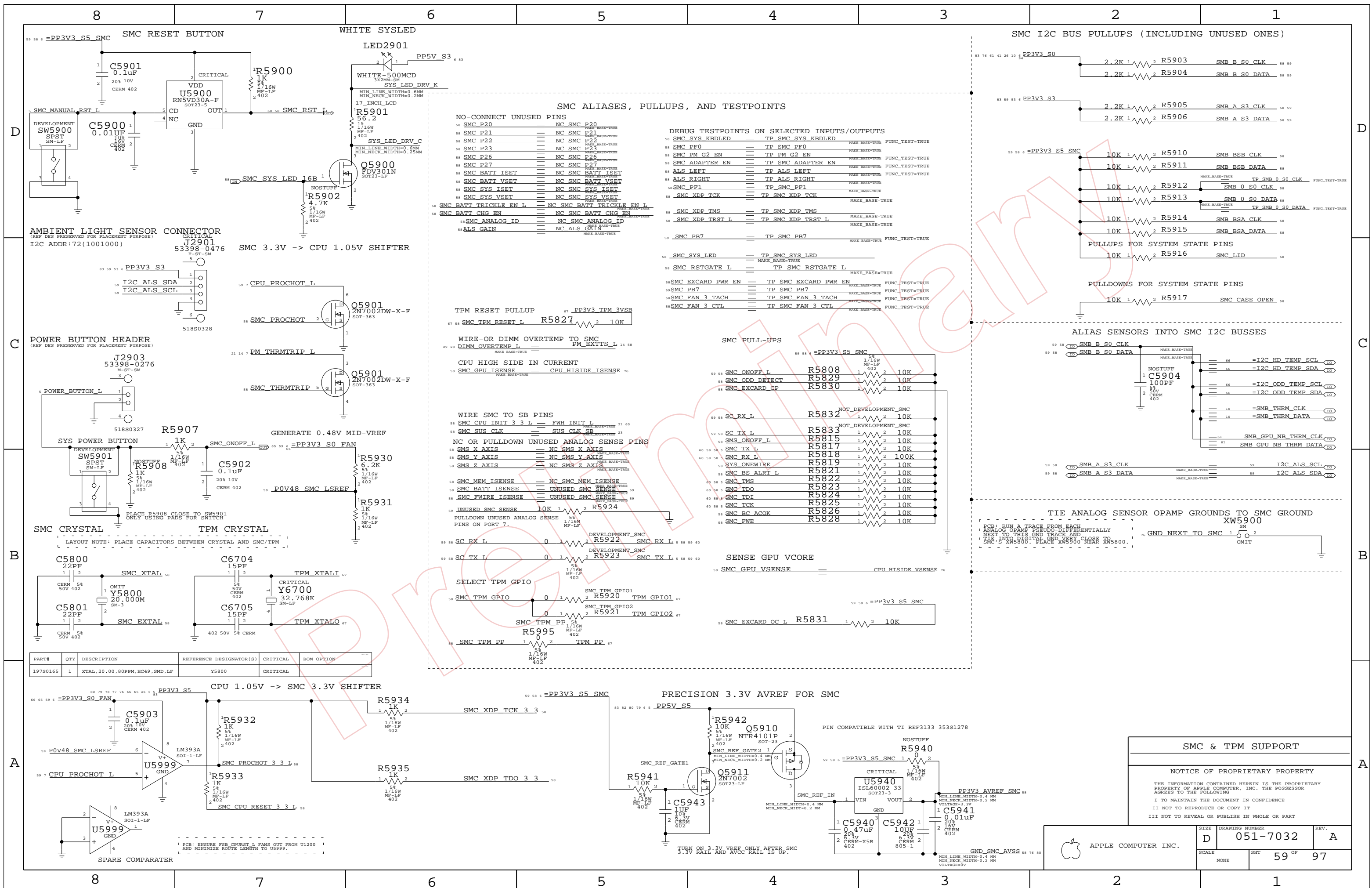
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<p>APPLE COMPUTER INC.</p>	<p>SIZE</p> <p style="text-align: center;">D</p>	<p>DRAWING NUMBER</p> <p style="text-align: center;">051-7032</p>	<p>REV.</p> <p style="text-align: center;">A</p>
	<p>SCALE</p> <p style="text-align: center;">NONE</p>	<p>SHT</p> <p style="text-align: center;">58 OF 97</p>	



### SMC ALIASES, PULLUPS, AND TESTPOINTS

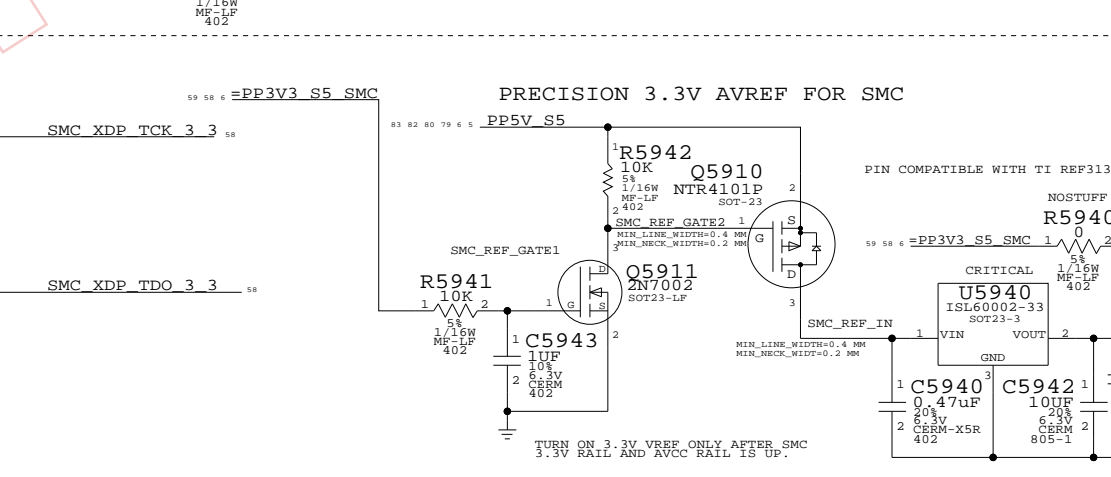
NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC_PM_G2_EN == TP_PM_G2_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P23 == NC SMC P23	58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P26 == NC SMC P26	58 ALS_LEFT == TP_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P27 == NC SMC P27	58 ALS_RIGHT == TP_ALS_RIGHT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_ISET == NC SMC_BATT_ISET	58 SMC_PFI == TP_SMC_PFI MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC SMC_BATT_VSET	58 SMC_XDP_TCK == TP_SMC_XDP_TCK MAKE_BASE=TRUE
58 SMC_SYS_ISET == NC SMC_SYS_ISET	58 SMC_XDP_TMS == TP_SMC_XDP_TMS MAKE_BASE=TRUE
58 SMC_SYS_VSET == NC SMC_SYS_VSET	58 SMC_XDP_TRST_L == TP_SMC_XDP_TRST_L MAKE_BASE=TRUE
58 SMC_BATT_TRICKLE_EN_L == NC SMC_BATT_TRICKLE_EN_L	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_CHG_EN == NC SMC_BATT_CHG_EN	58 SMC_SYS_LED == TP_SMC_SYS_LED MAKE_BASE=TRUE
58 SMC_ANALOG_ID == NC SMC_ANALOG_ID	58 SMC_RSTGATE_L == TP_SMC_RSTGATE_L MAKE_BASE=TRUE
58 ALS_GAIN == NC ALS_GAIN MAKE_BASE=TRUE	58 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL MAKE_BASE=TRUE FUNC_TEST=TRUE

### SMC PULL-UPS

58 SMC_ONOFF_L	R5808	10K
58 SMC_ODD_DETECT	R5829	10K
58 SMC_EXCARD_CP	R5830	10K
58 SC_RX_L	R5832	10K
58 SC_TX_L	R5833	10K
58 SMS_ONOFF_L	R5815	10K
58 SMC_TX_L	R5817	10K
58 SMC_RX_L	R5818	100K
58 SYS_ONEWIRE	R5819	10K
58 SMC_BS_ALERT_L	R5821	10K
58 SMC_TMS	R5822	10K
58 SMC_TDO	R5823	10K
58 SMC_TDI	R5824	10K
58 SMC_TCK	R5825	10K
58 SMC_BC_ACOK	R5826	10K
58 SMC_FWE	R5828	10K

### WIRE SMC TO SB PINS

58 SMC_CPU_INIT_3_3_L	FWH_INIT_L	21
58 SMC_SUS_CLK	SUS_CLK_SB	23
58 NC_OR_PULLDOWN_UNUSED_ANALOG_SENSE_PINS		
58 SMC_X_AXIS	NC_SMC_X_AXIS	
58 SMC_Y_AXIS	NC_SMC_Y_AXIS	
58 SMC_Z_AXIS	NC_SMC_Z_AXIS	
58 SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE	
58 SMC_BATT_ISENSE	UNUSED_SMC_ISENSE	59
58 SMC_FWIRE_ISENSE	UNUSED_SMC_ISENSE	59
58 UNUSED_SMC_SENSE	10K	R5924
58 PULLDOWN_UNUSED_ANALOG_SENSE_PINS_ON_PORT_7		
58 SC_RX_L	R5922	10K
58 SC_TX_L	R5923	10K
58 SMC_TPM_GPIO	R5920	10K
58 SMC_TPM_PP	R5921	10K
58 SMC_TPM_PP	R5995	10K
58 SMC_EXCARD_OC_L	R5831	10K



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

**SMC & TPM SUPPORT**

**NOTICE OF PROPRIETARY PROPERTY**

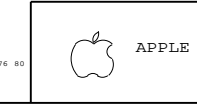
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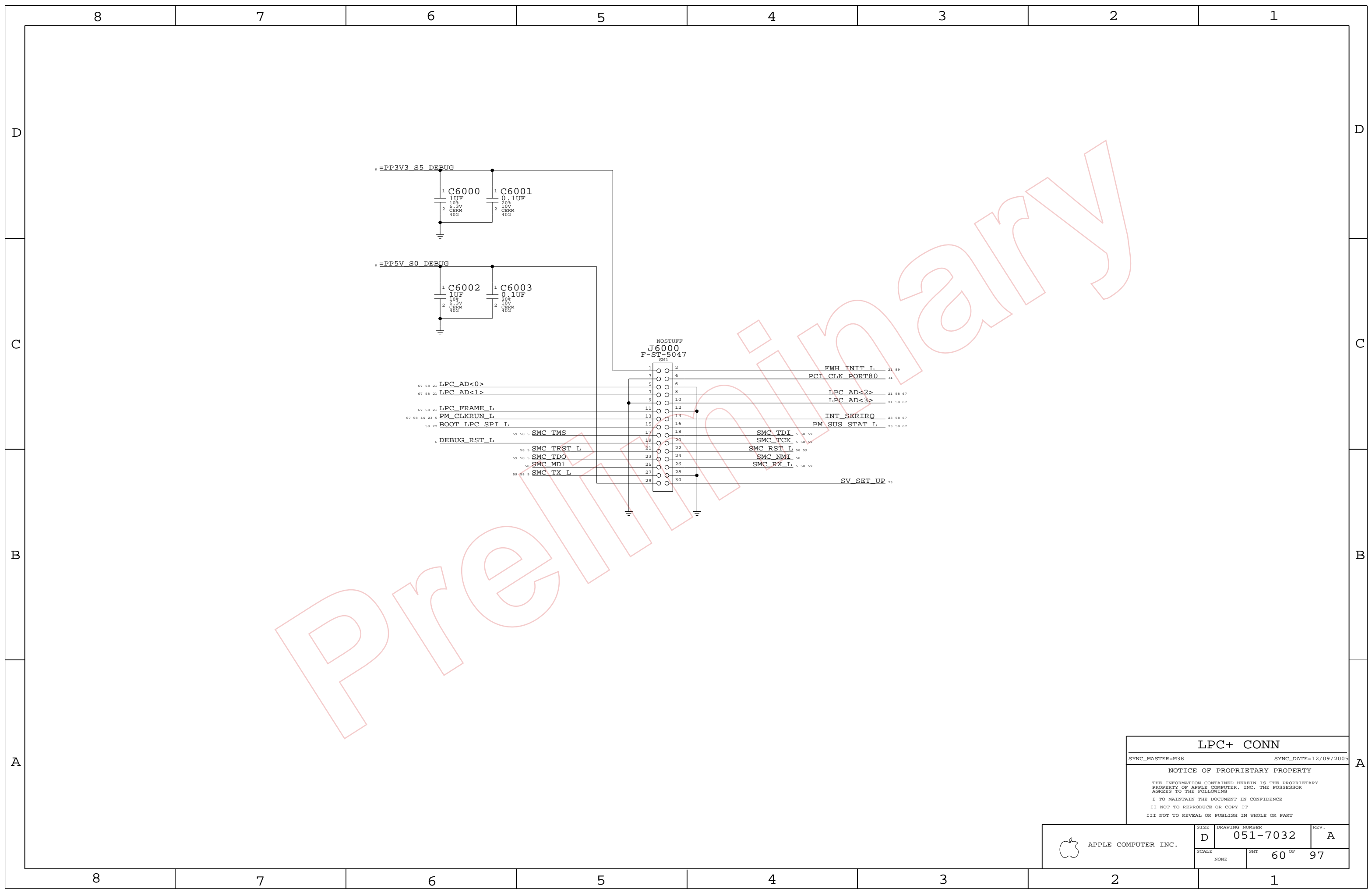
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SIZE	DRAWING NUMBER	REV.
D	051-7032	A
SCALE	SHT	59 OF 97
NONE		





Pre-release

**LPC+ CONN**

SYNC\_MASTER=M38 SYNC\_DATE=12/09/2005

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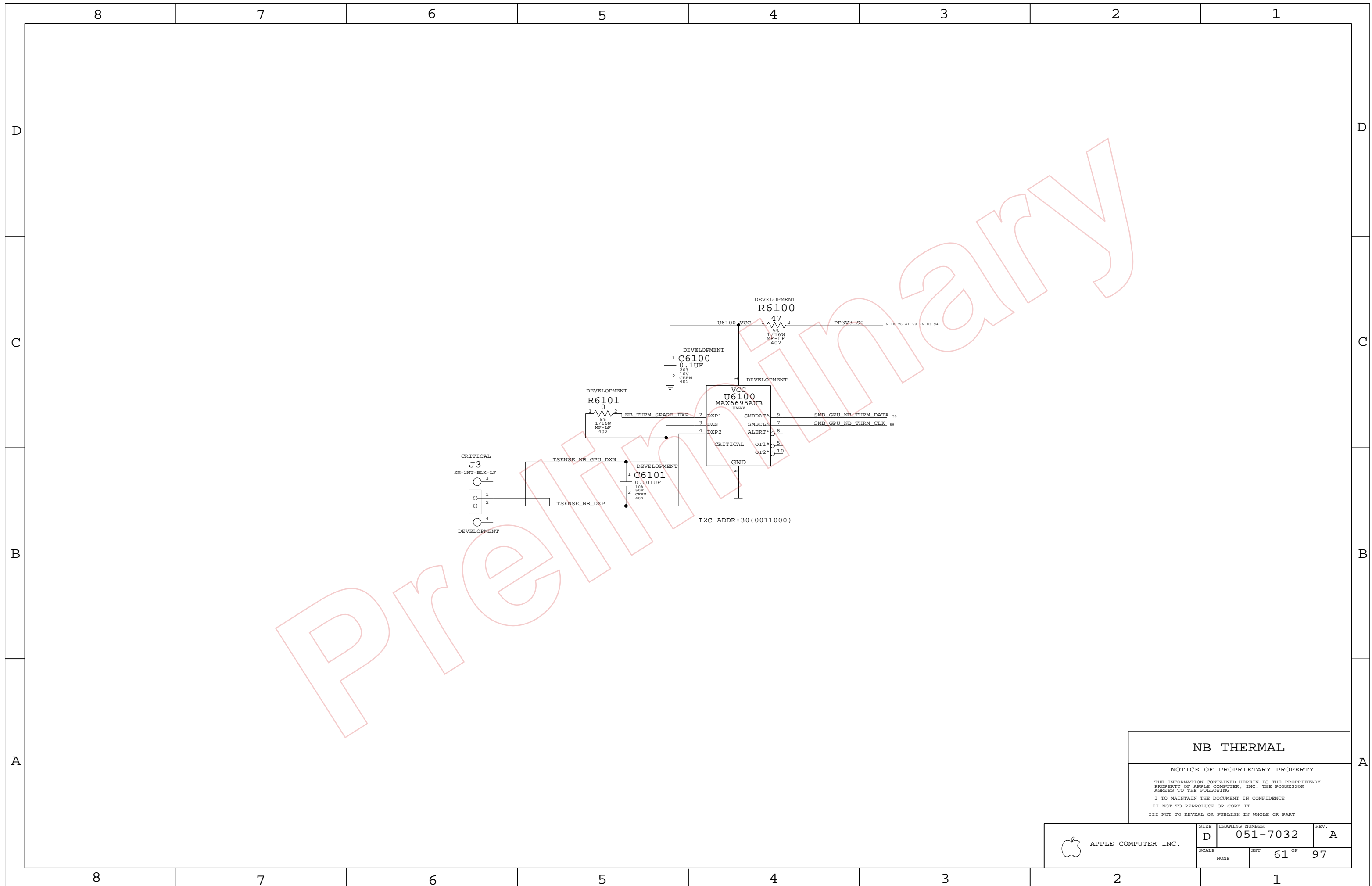
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	SCALE	NONE	SHT	60 OF 97		

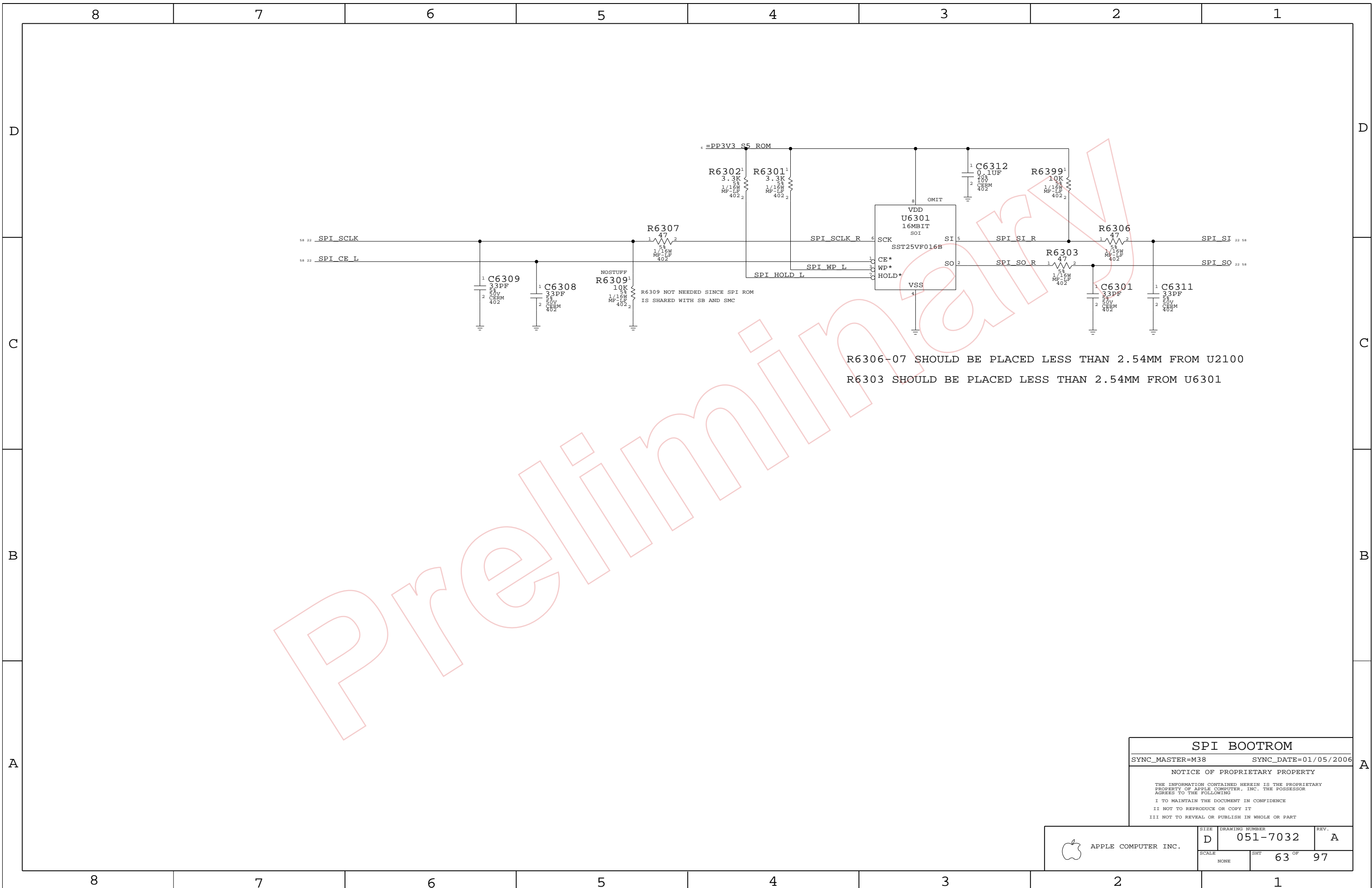


NB THERMAL

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	61 OF 97	
NONE			



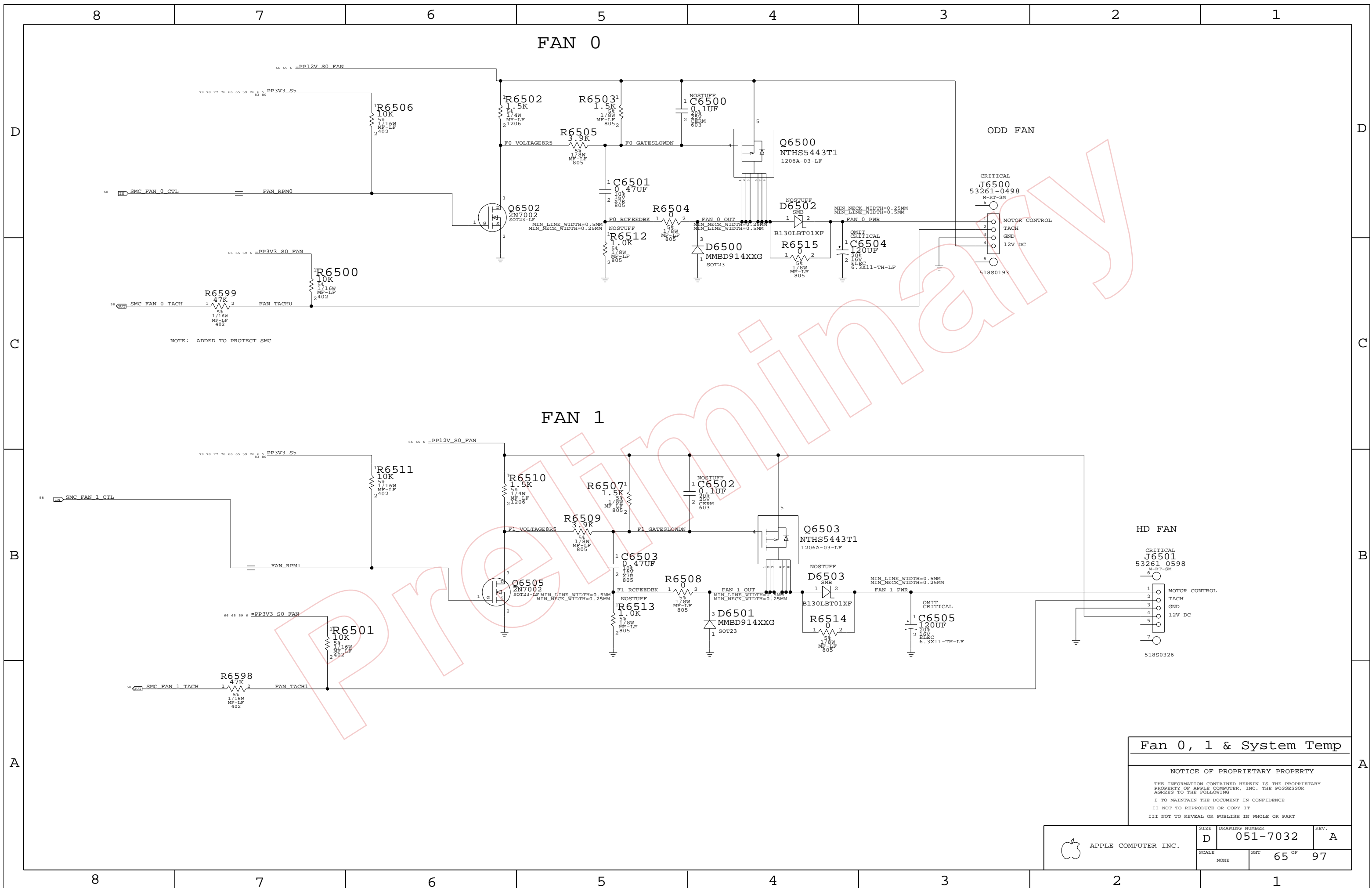
R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100  
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

**SPI BOOTROM**  
 SYNC\_MASTER=M38      SYNC\_DATE=01/05/2006

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT		OF
NONE	63		97



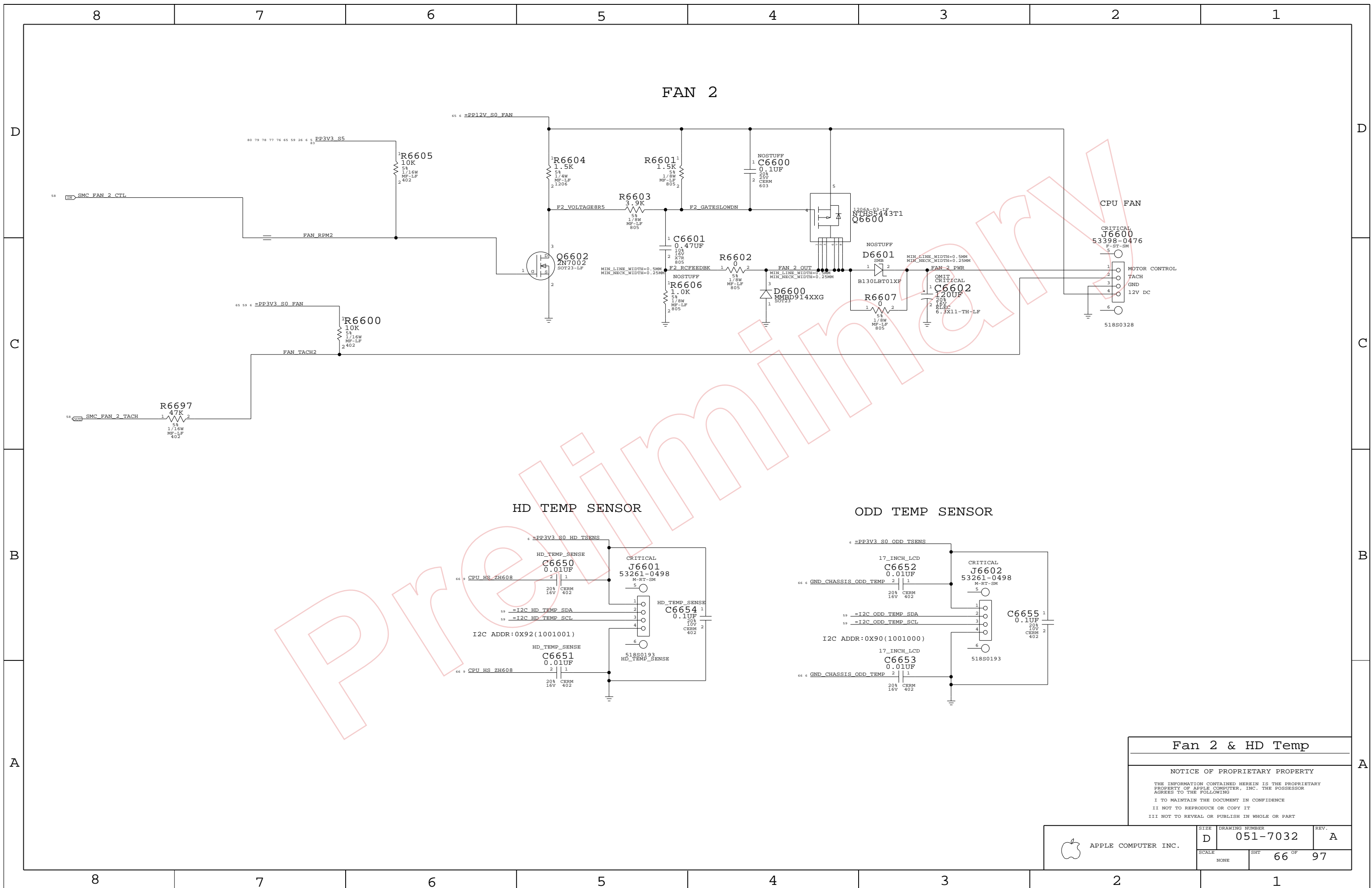


Fan 0, 1 & System Temp

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	D	051-7032	A
SCALE	SHT	65 OF 97	
NONE			



Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	66 OF	97
NONE			

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1

D

D

C

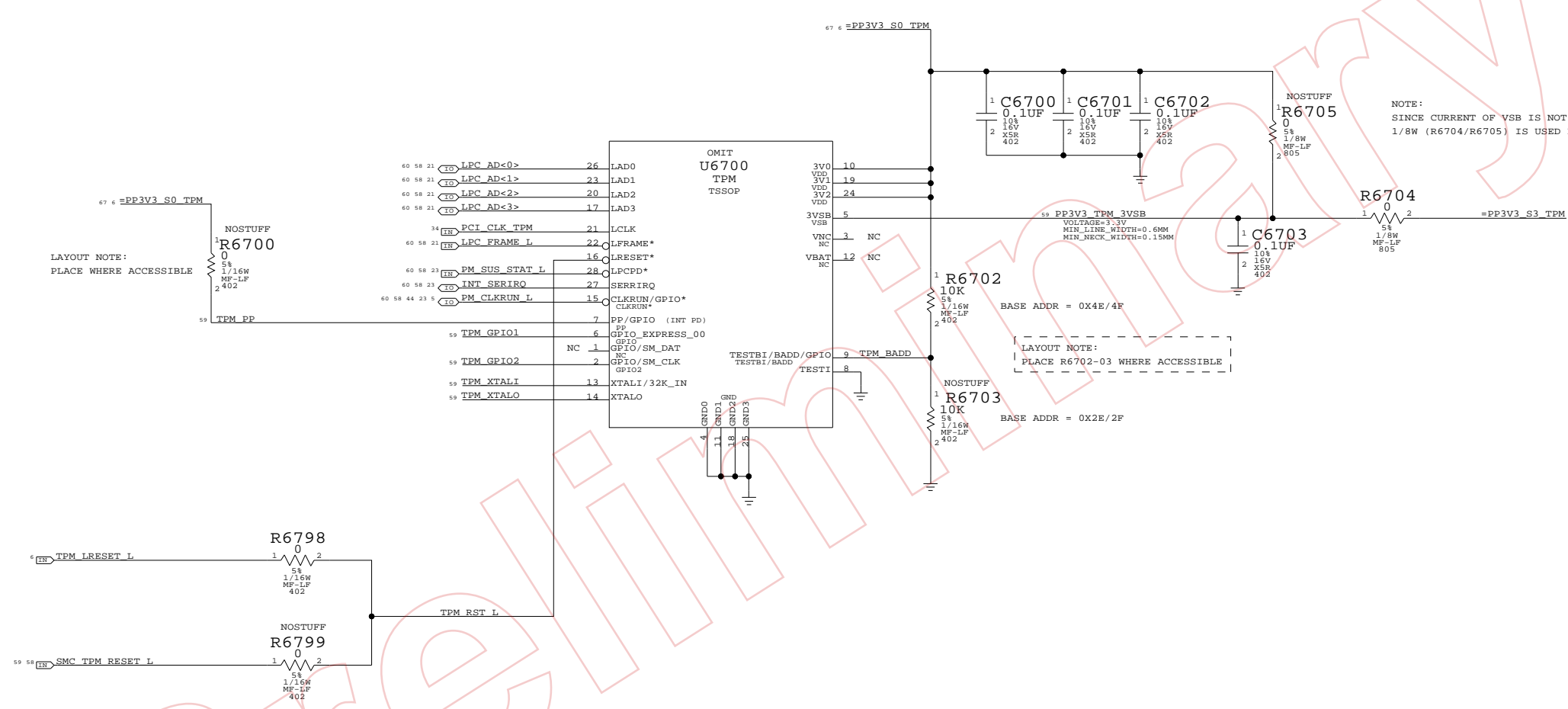
C

B

B

A

A



LAYOUT NOTE:  
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:  
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:  
SINCE CURRENT OF VSB IS NOT YET ON SPEC,  
1/8W (R6704/R6705) IS USED FOR NOW

TPM	
SYNC_MASTER=M38	SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	67 OF 97	
NONE			

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7

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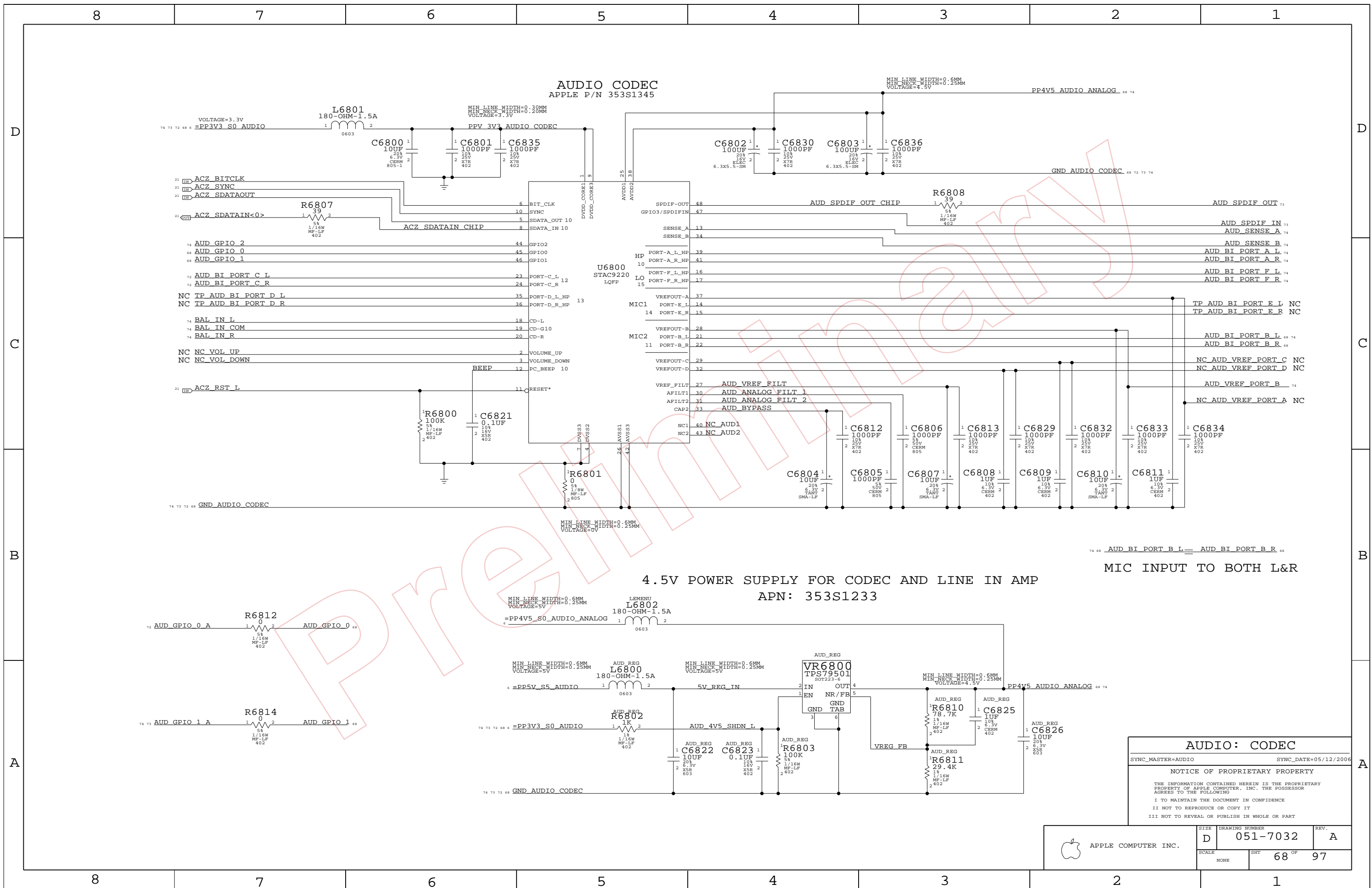
5

4

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1



**AUDIO: CODEC**

SYNC\_MASTER=AUDIO      SYNC\_DATE=05/12/2006

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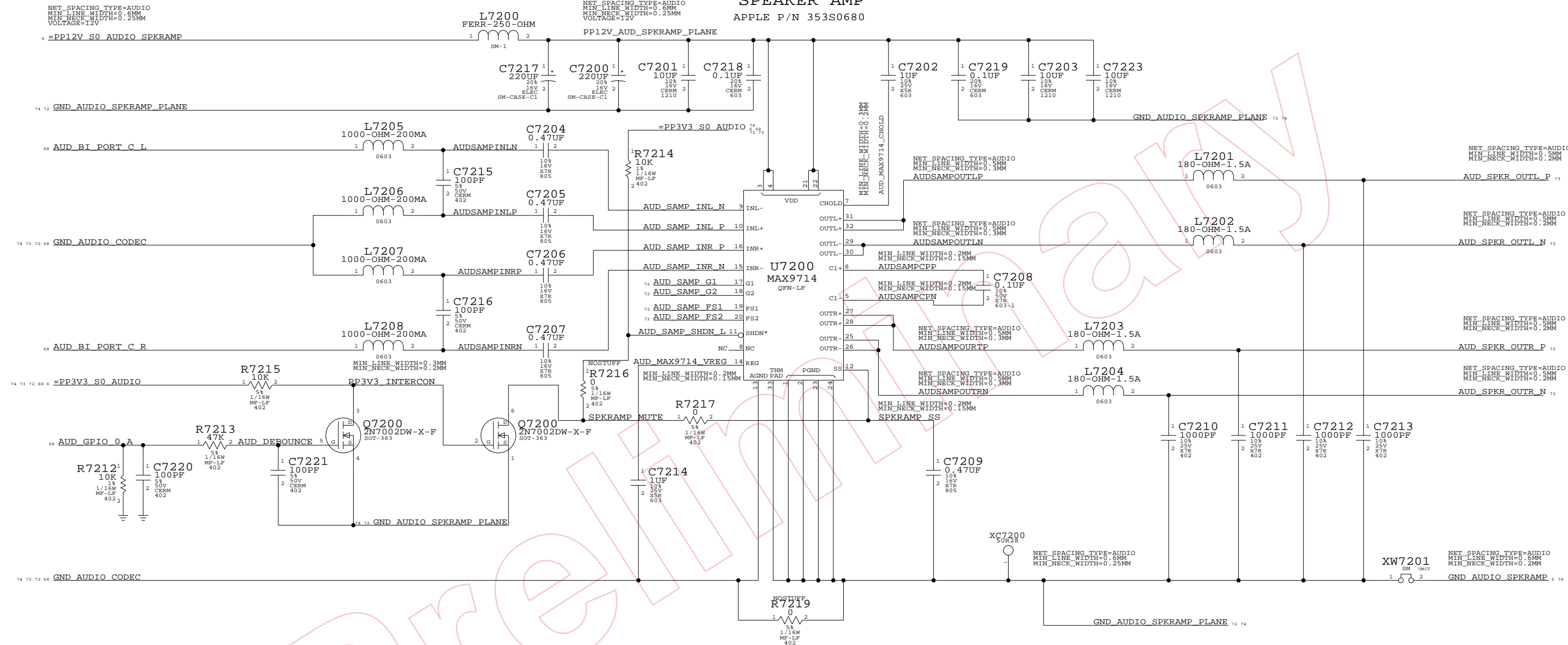
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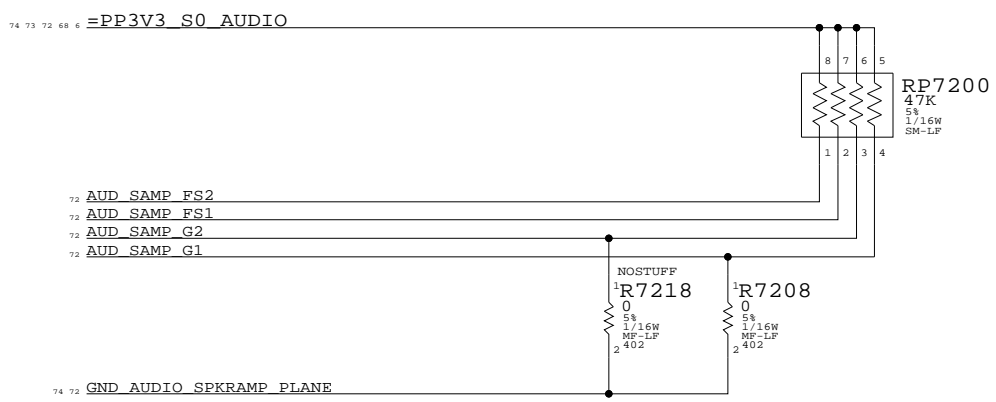
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>A</b>
	SCALE NONE	SHEET 68 OF 97	

**SPEAKER AMP**  
APPLE P/N 353S0680



GAIN SETTINGS: +19DB  
MODULATION SETTING: LOW EMI  
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

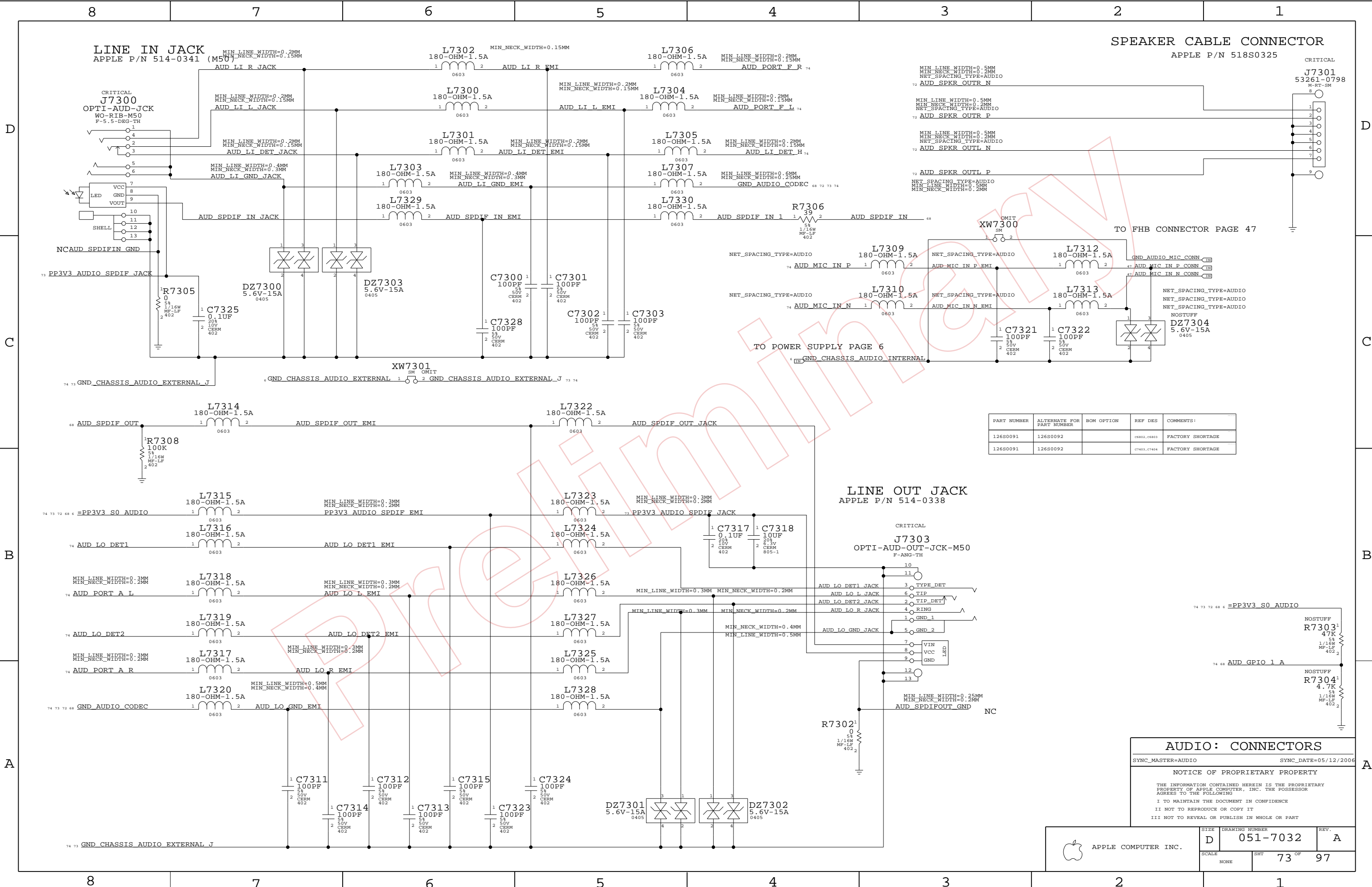


**AUDIO: SPEAKER AMP**  
SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006  
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	D	051-7032	A
SCALE	SHT	72 OF	97
NONE			

**LINE IN JACK**  
APPLE P/N 514-0341 (M50)

**SPEAKER CABLE CONNECTOR**  
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

**LINE OUT JACK**  
APPLE P/N 514-0338

**AUDIO: CONNECTORS**

SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006

**NOTICE OF PROPRIETARY PROPERTY**

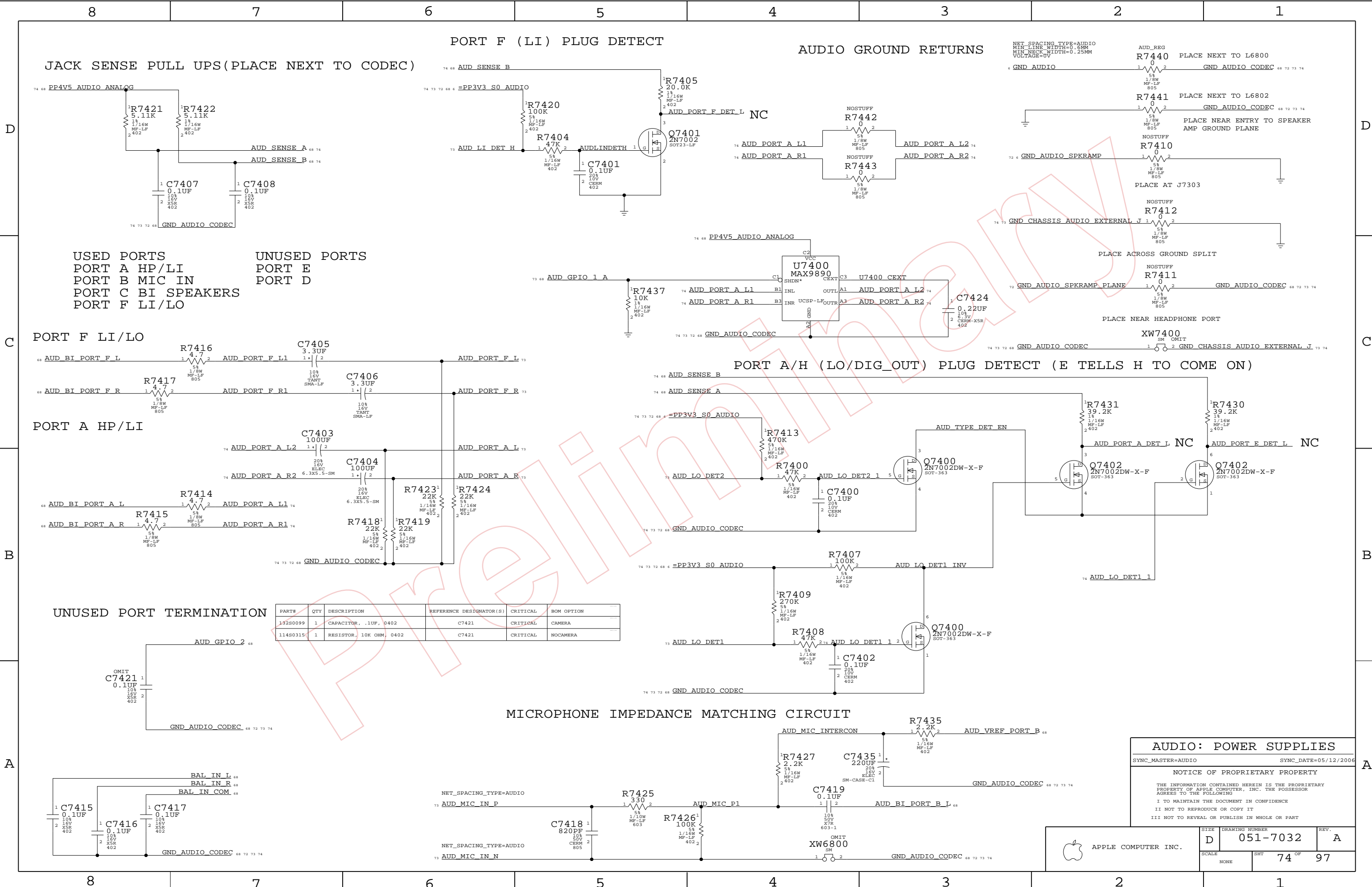
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	D	051-7032	A
SCALE	SHT	73 OF	97
NONE			



JACK SENSE PULL UPS (PLACE NEXT TO CODEC)

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

NET SPACING TYPE=AUDIO  
MIN LINE WIDTH=0.6MM  
MIN SPC WIDTH=0.25MM  
VOLTAGE=0V

USED PORTS  
PORT A HP/LI  
PORT B MIC IN  
PORT C BI SPEAKERS  
PORT F LI/LO

UNUSED PORTS  
PORT E  
PORT D

PORT F LI/LO

PORT A HP/LI

PORT A/H (LO/DIG\_OUT) PLUG DETECT (E TELLS H TO COME ON)

UNUSED PORT TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

MICROPHONE IMPEDANCE MATCHING CIRCUIT

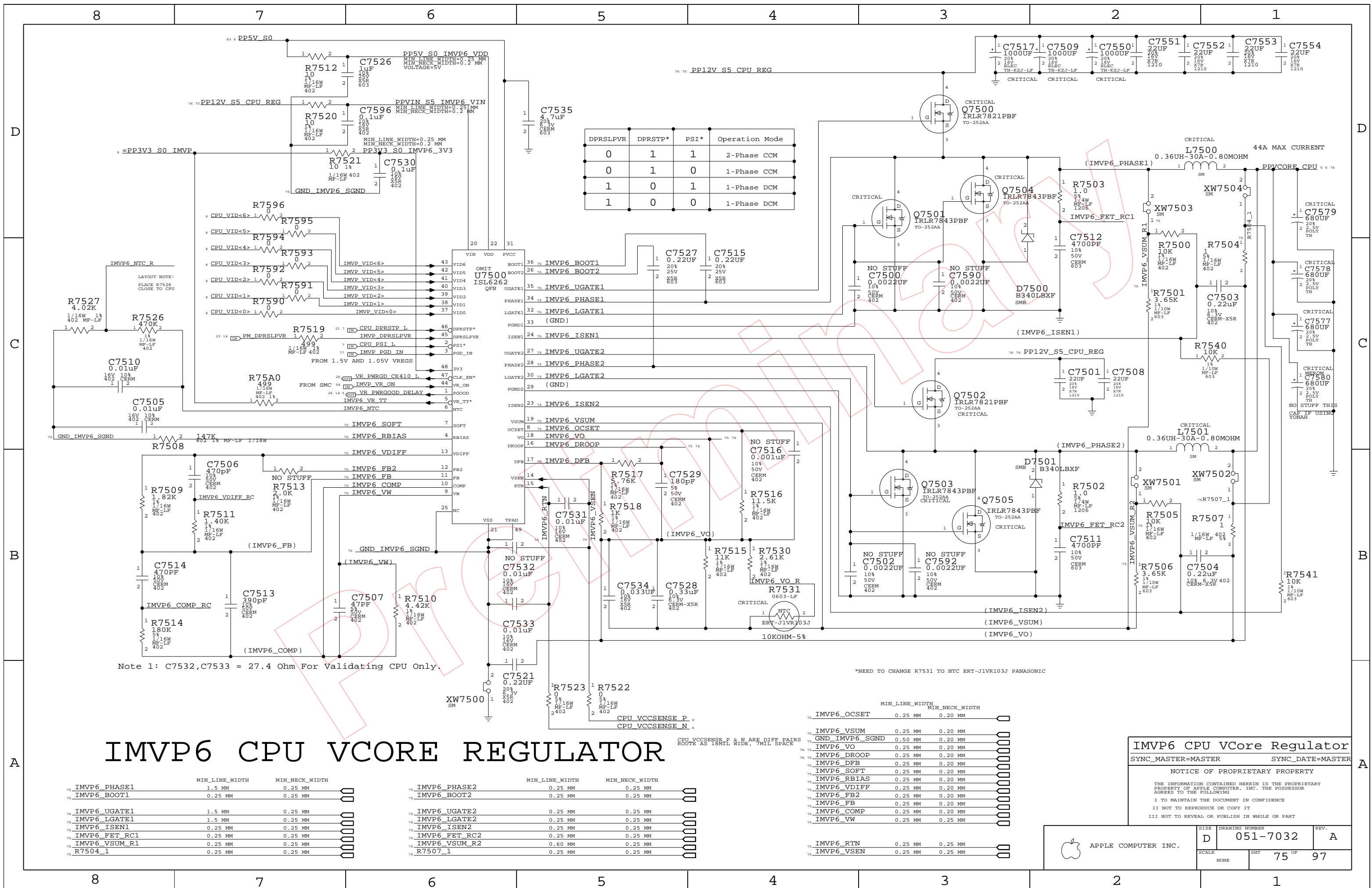
AUDIO: POWER SUPPLIES

SYNC\_MASTER=AUDIO SYNC\_DATE=05/12/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

\*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

# IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_RBIAS	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

## IMVP6 CPU VCore Regulator

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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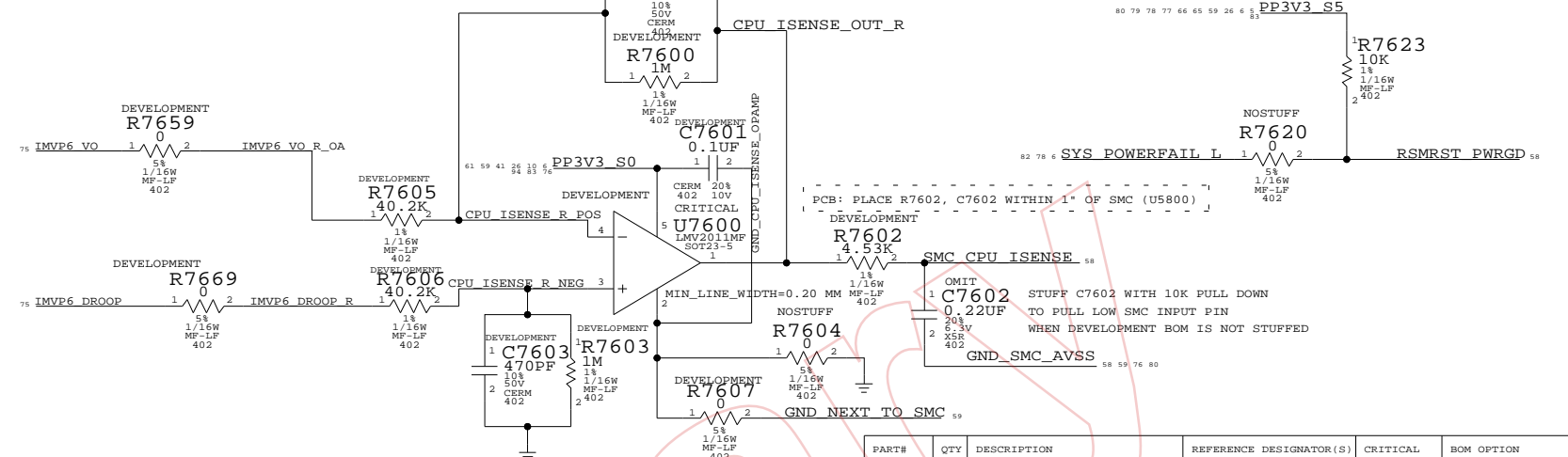
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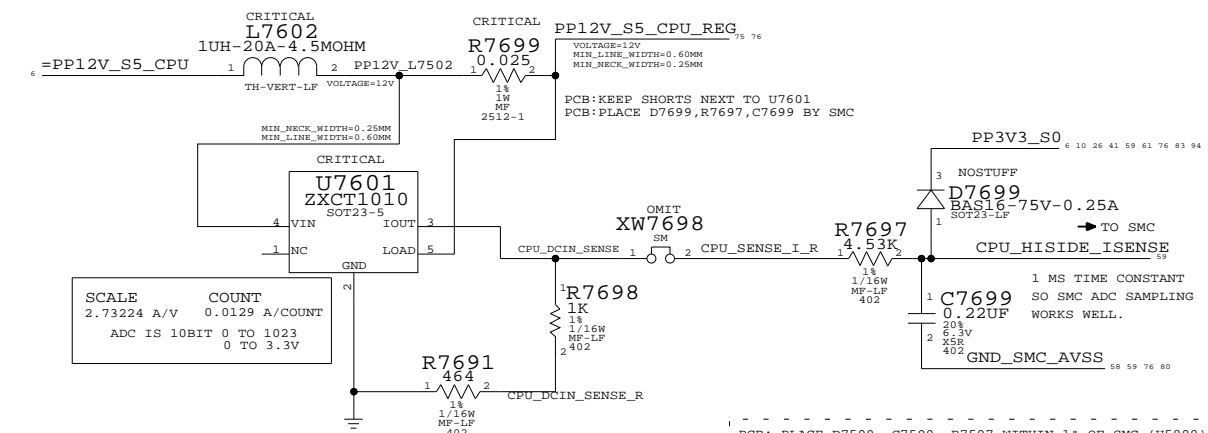
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7032</b>	REV. <b>A</b>
	SCALE NONE	SHEET <b>75</b>	OF <b>97</b>



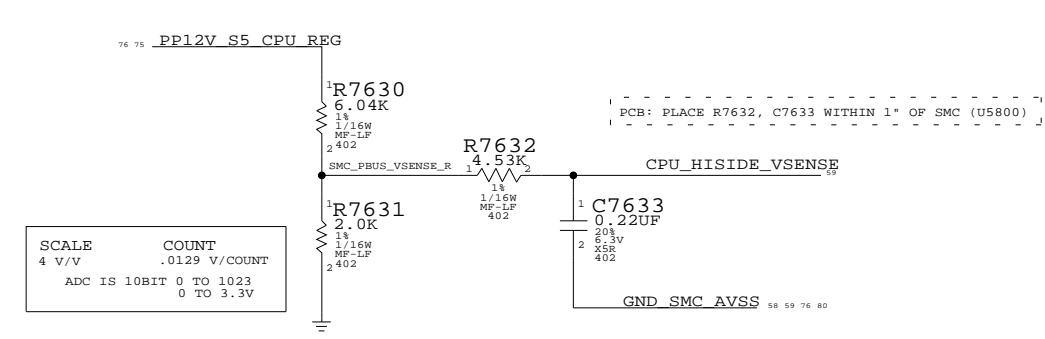
PROCESSOR VCORE CURRENT SENSE  
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)



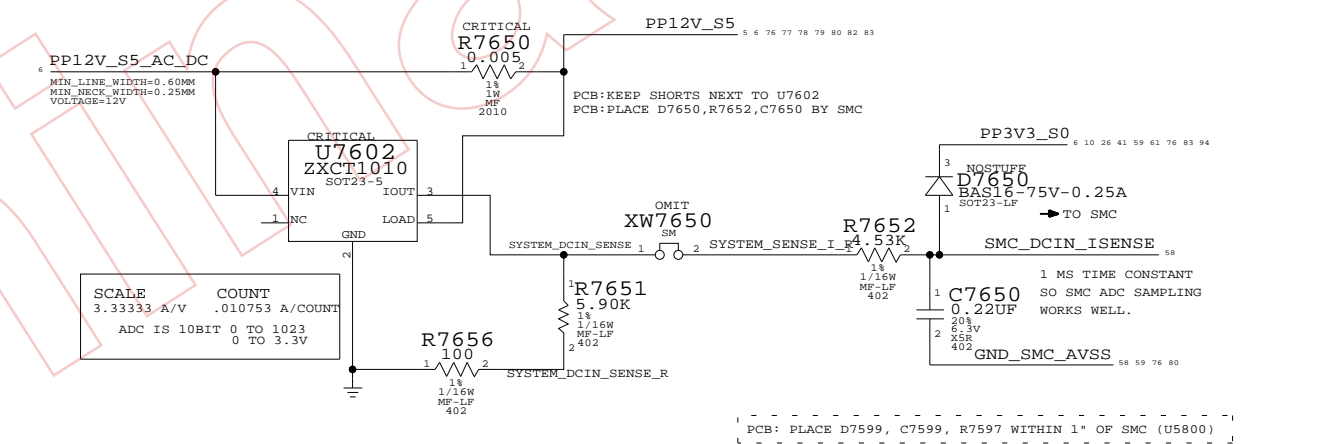
PROCESSOR VCORE CURRENT SENSE  
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



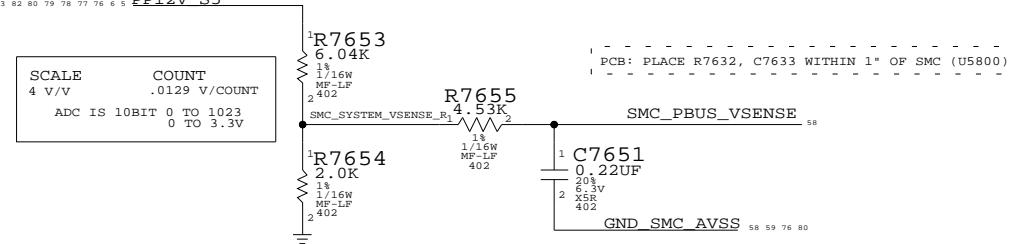
PROCESSOR DCIN VOLTAGE SENSE  
(SCALING 12V INPUT VOLTAGE TO SMC)



SYSTEM CURRENT SENSE

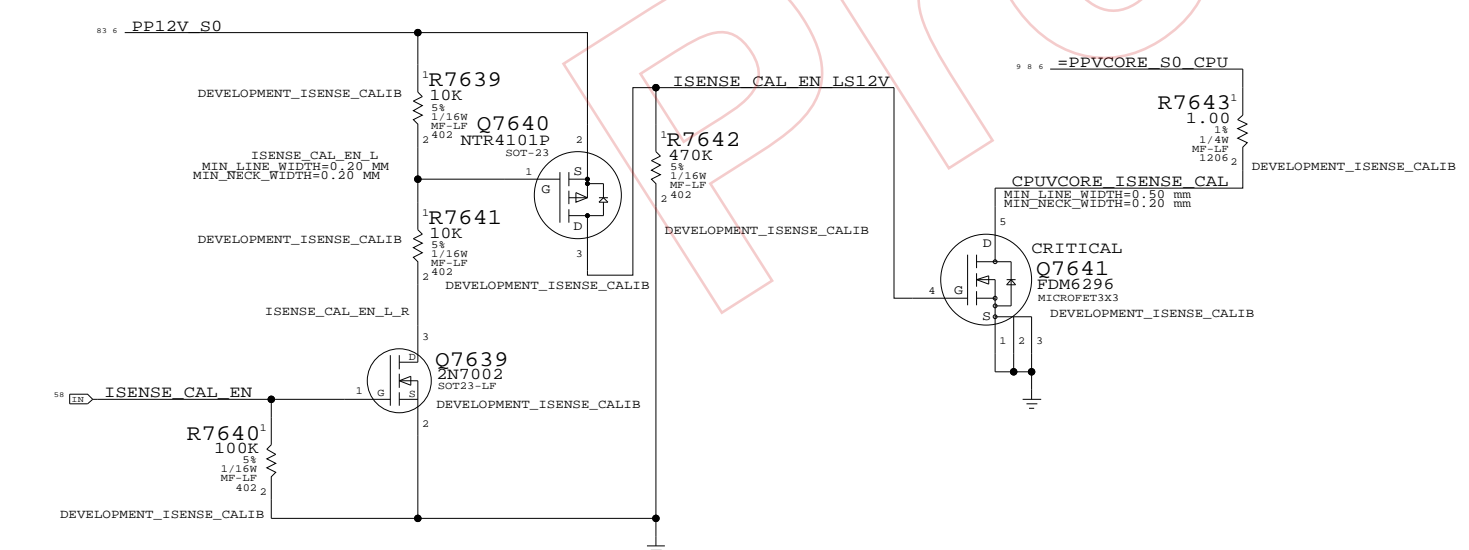


SYSTEM VOLTAGE SENSE  
(SCALING 12V INPUT VOLTAGE TO SMC)

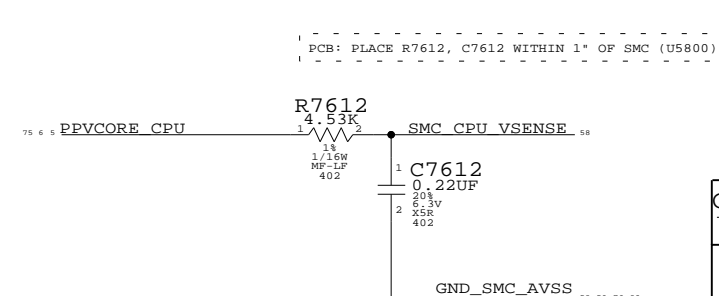


Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

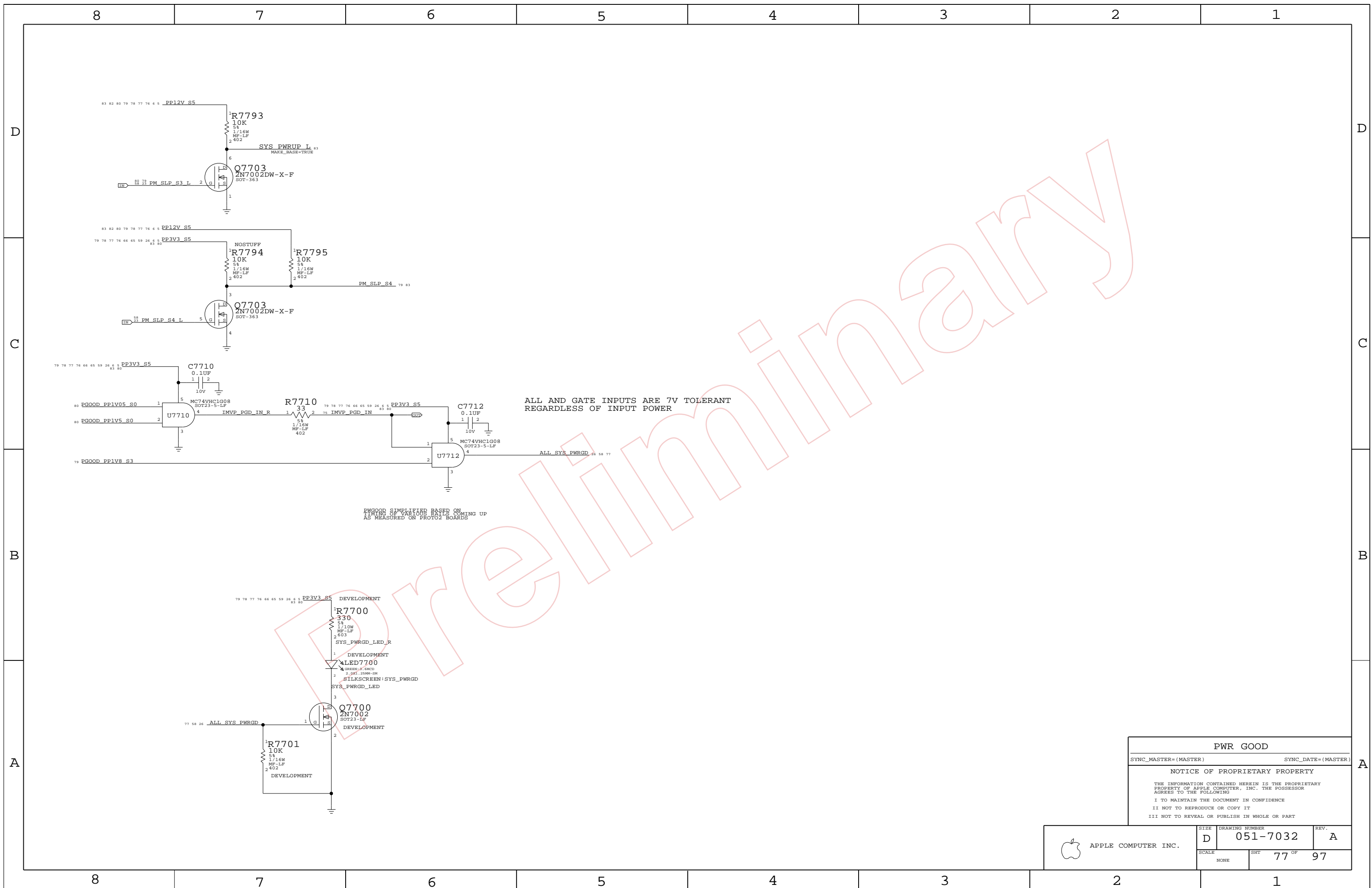


PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

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Preliminary

**PWR GOOD**

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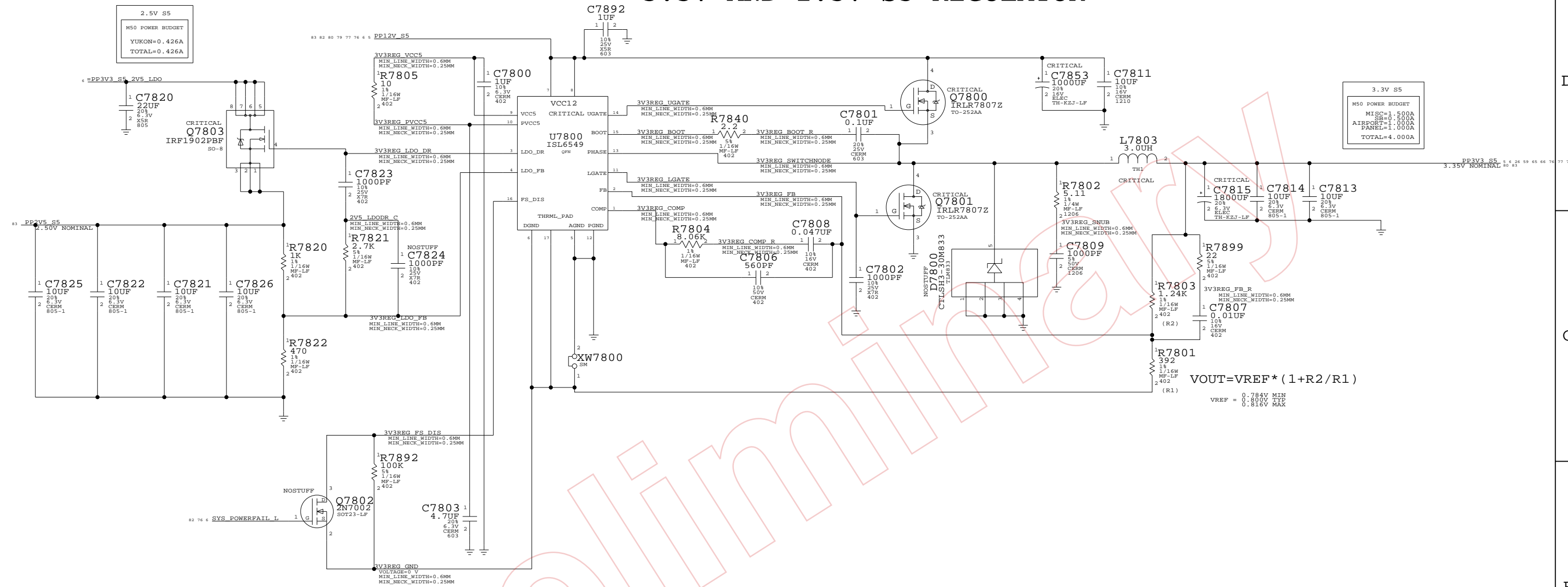
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	SCALE NONE	SHT 77 OF	97

# 3.3V AND 2.5V S5 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN  
0.800V TYP  
0.816V MAX

**3V DC/DC 2.5V**

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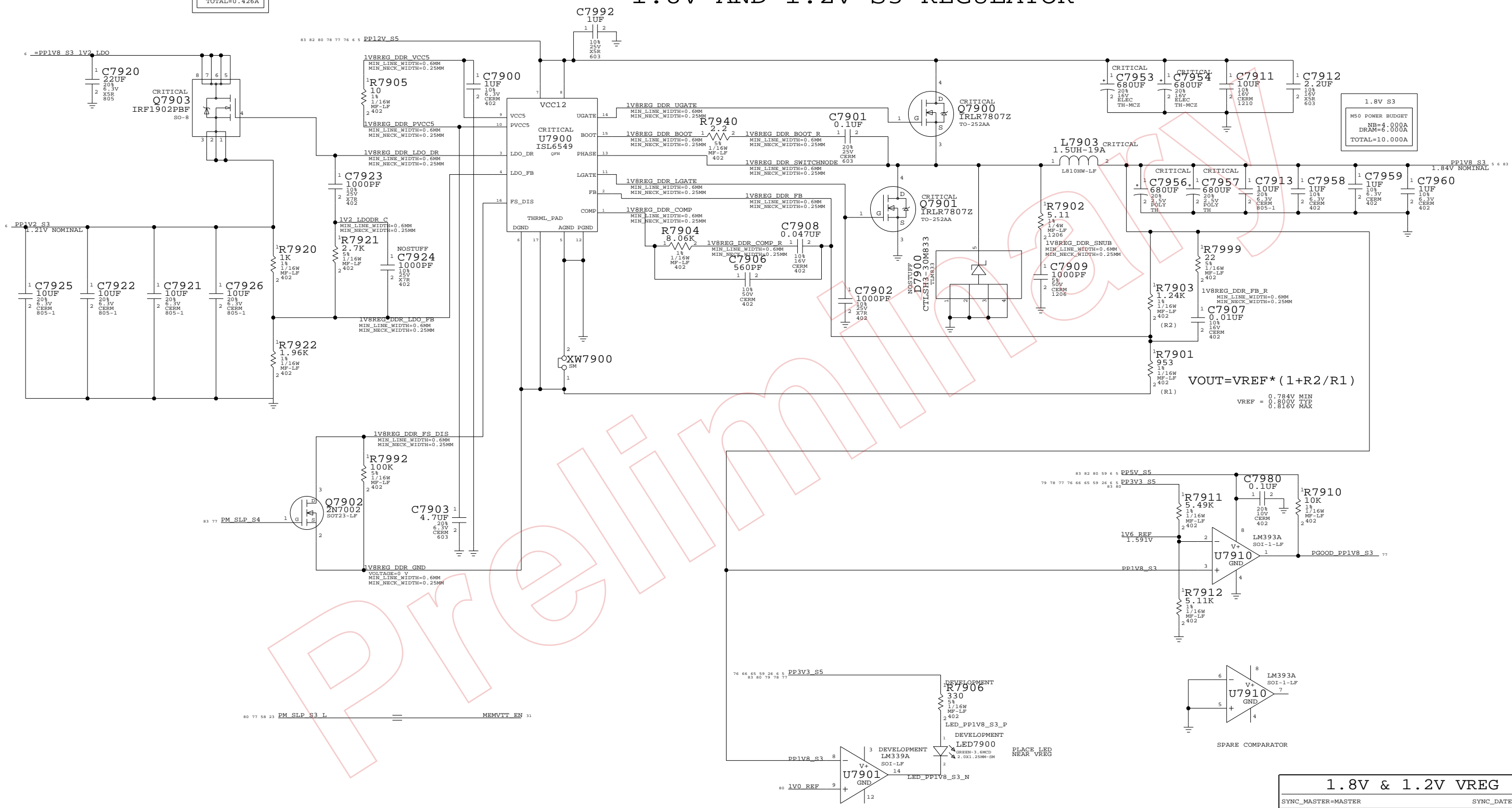
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	A
SCALE	SHT	78 OF	97
NONE			

# 1.8V AND 1.2V S3 REGULATOR

1.2V S3  
M50 POWER BUDGET  
YUKON=0.426A  
TOTAL=0.426A

1.8V S3  
M50 POWER BUDGET  
M5=4.000A  
DRAM=6.000A  
TOTAL=10.000A



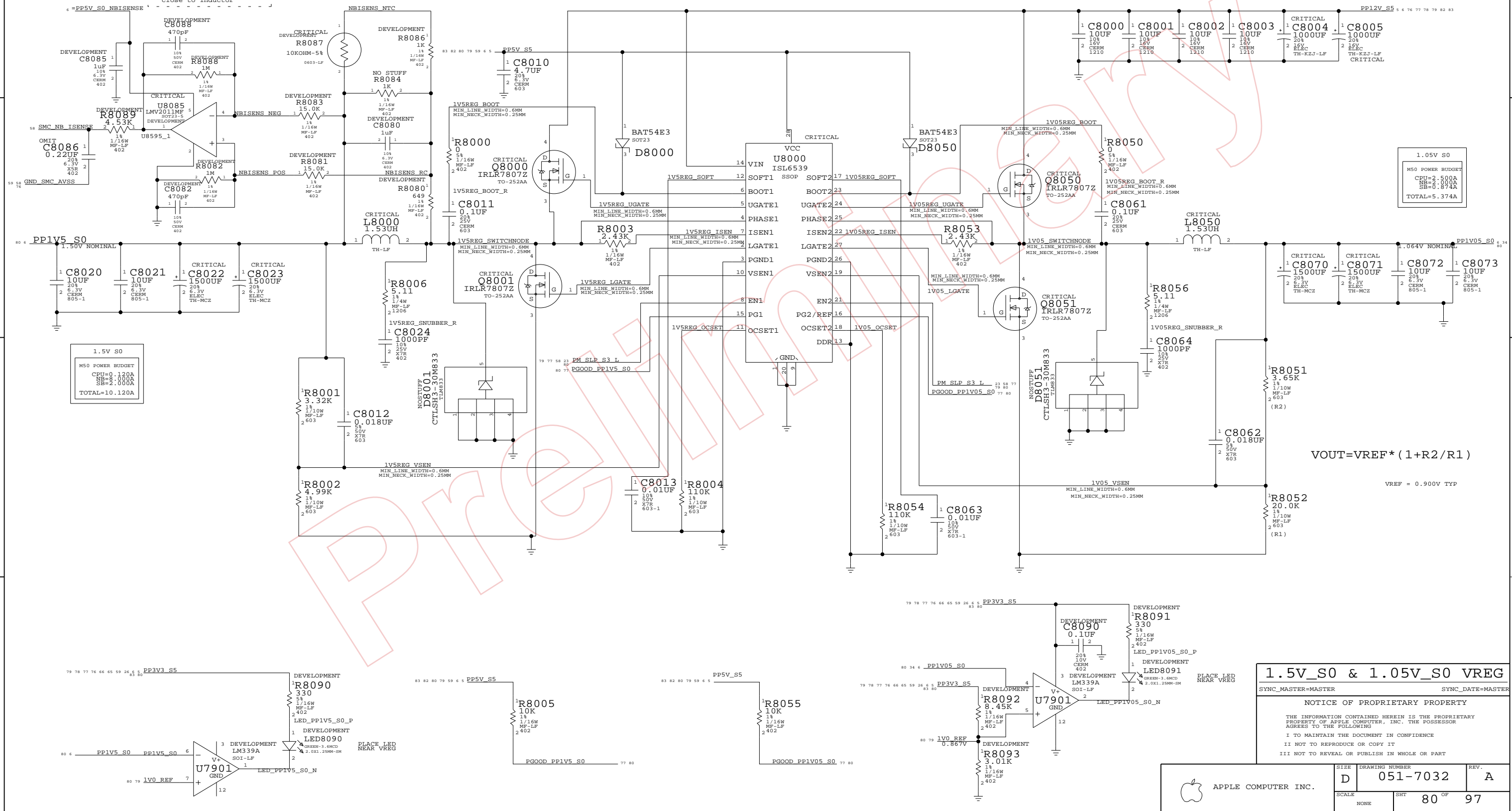
**1.8V & 1.2V VREG**  
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SCALE	SHT	79 OF	97
NONE			

# 1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:  
KEEP C8080, R8080,  
R8084 AND R8087  
close to inductor



## 1.5V\_S0 & 1.05V\_S0 VREG

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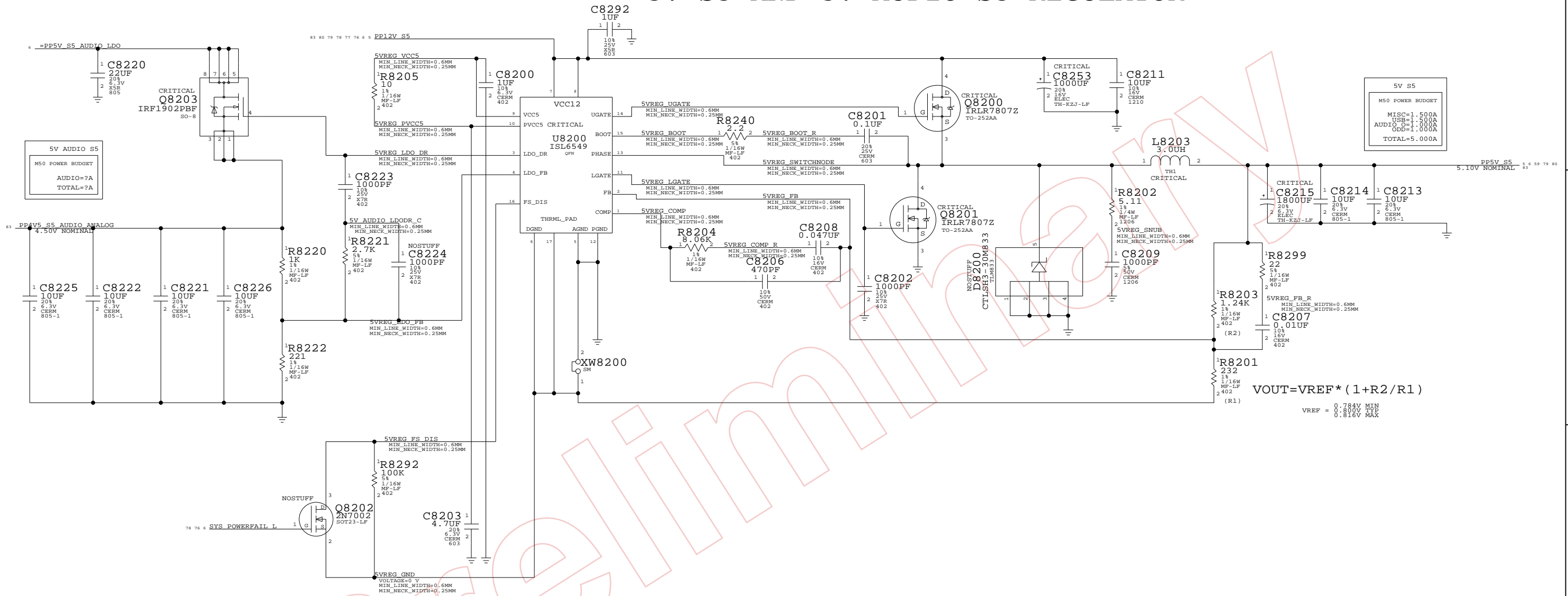
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	80 OF	97
NONE			

# 5V S5 AND 5V AUDIO S5 REGULATOR



5V AUDIO S5  
M50 POWER BUDGET  
AUDIO=7A  
TOTAL=7A

5V S5  
M50 POWER BUDGET  
MISC=1.500A  
USB=1.500A  
AUDIO\_O=1.000A  
ODD=1.000A  
TOTAL=5.000A

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN  
0.800V TYP  
0.816V MAX

POWER SUPPLY 3.3V/5V MAIN SWITCH

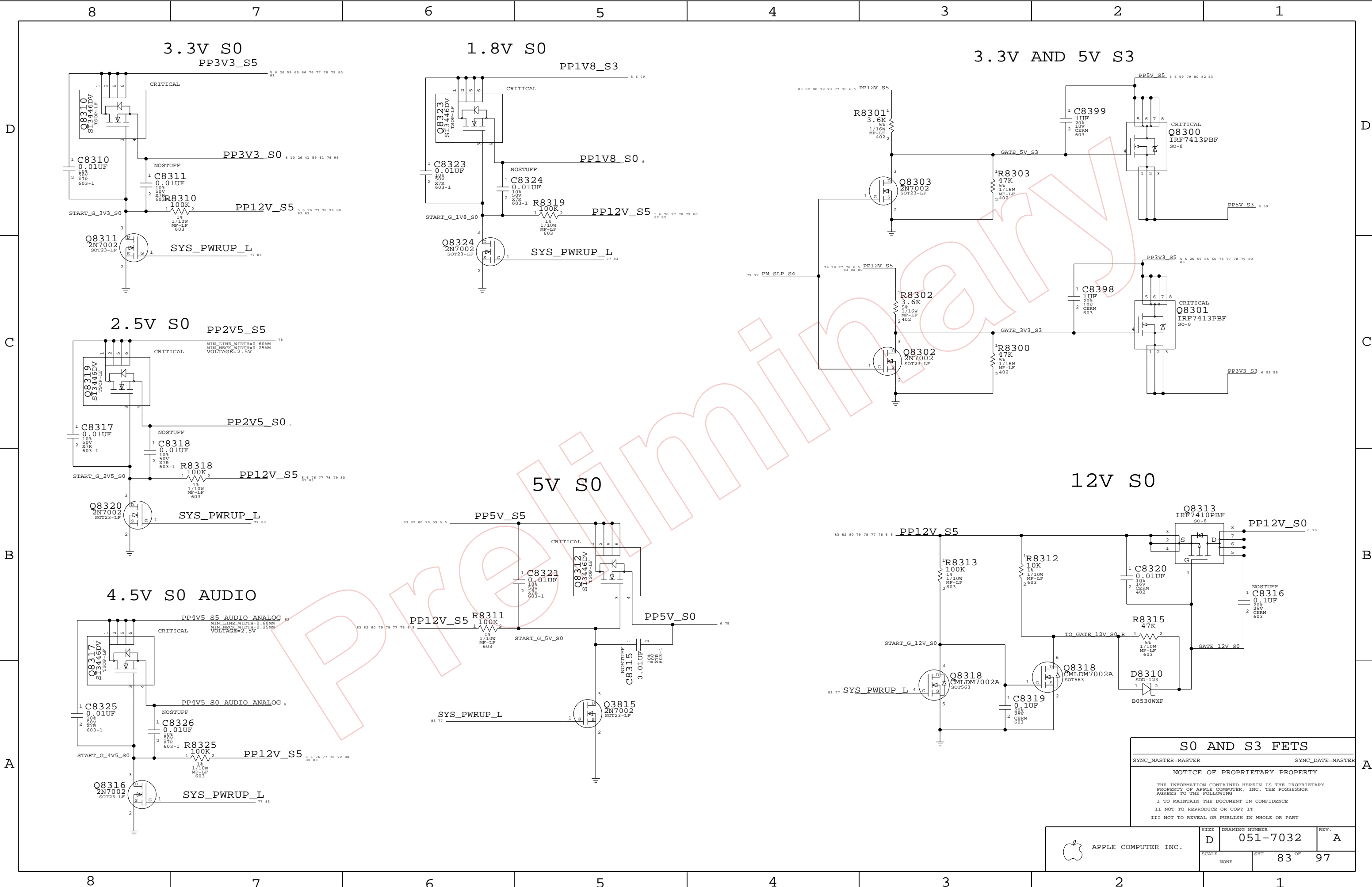
## 5V DC/DC

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NONE			



**S0 AND S3 FETS**

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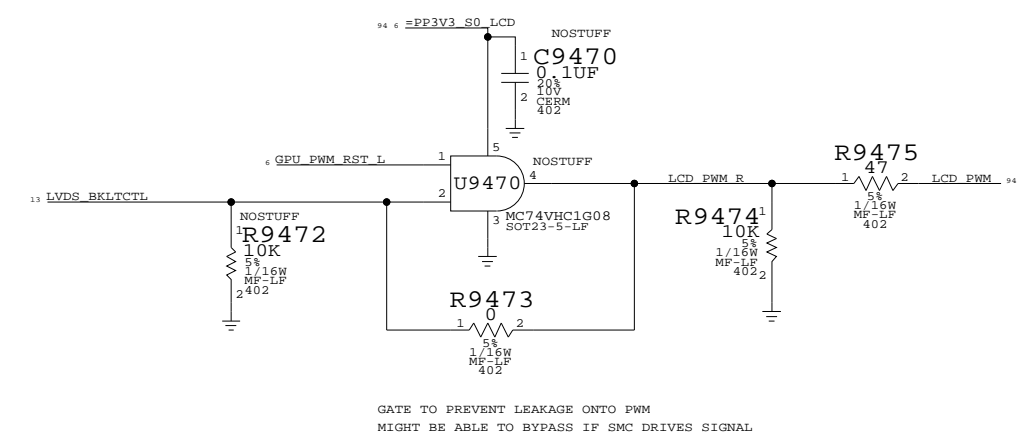
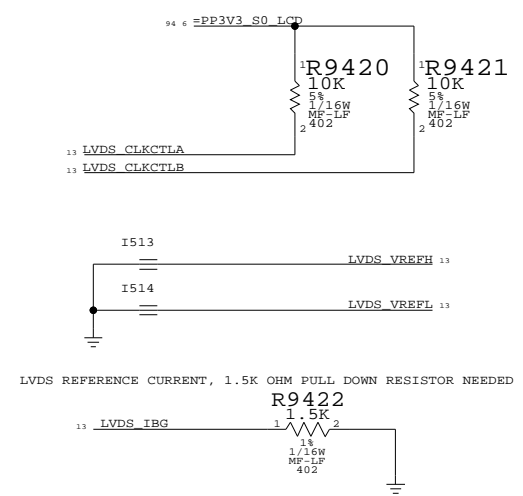
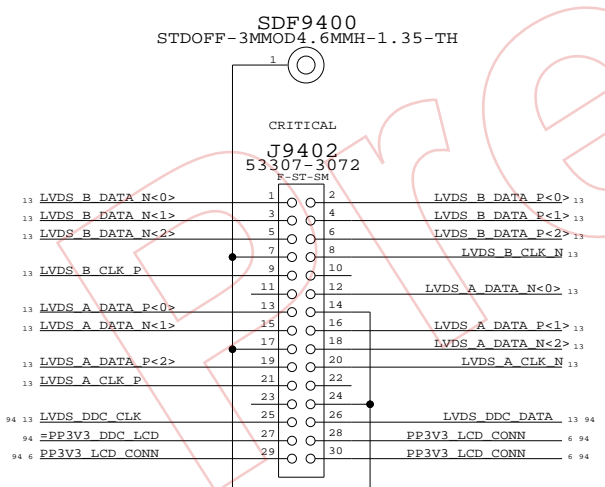
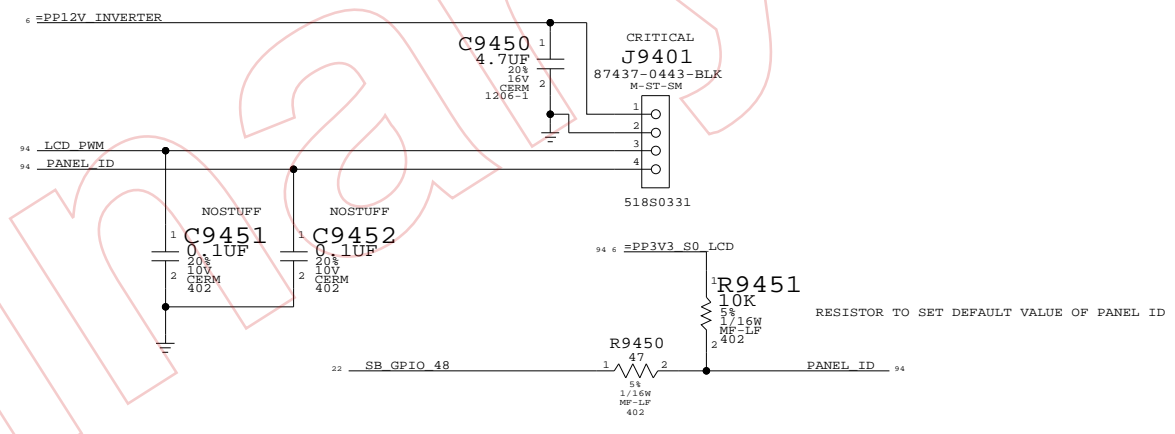
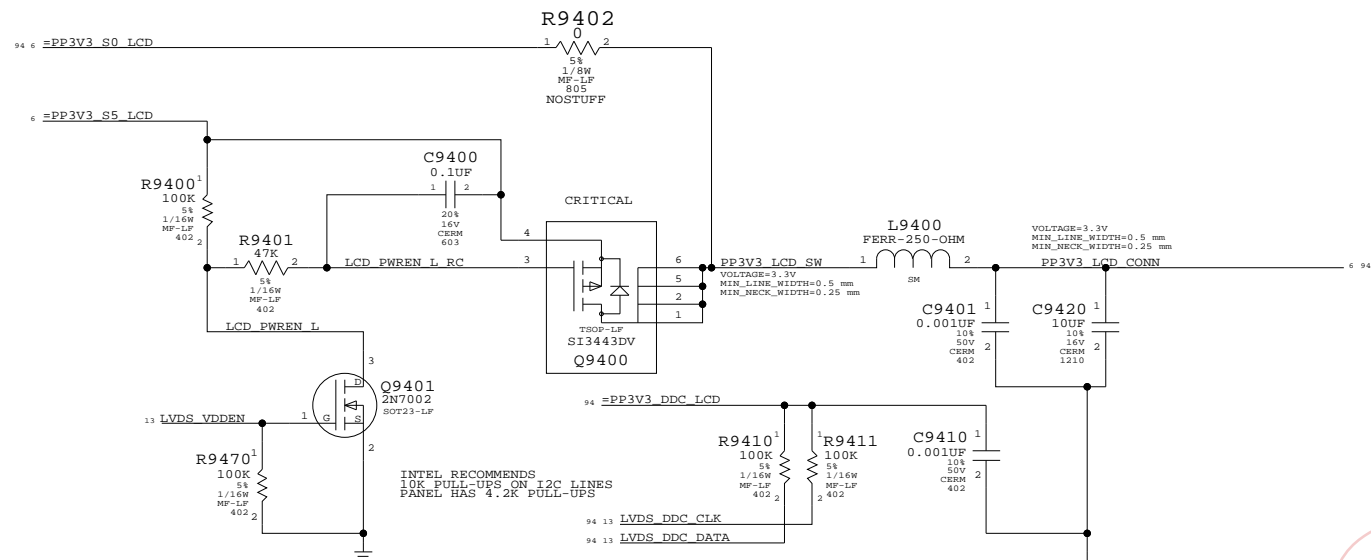
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NONE			

# LCD (LVDS) INTERFACE

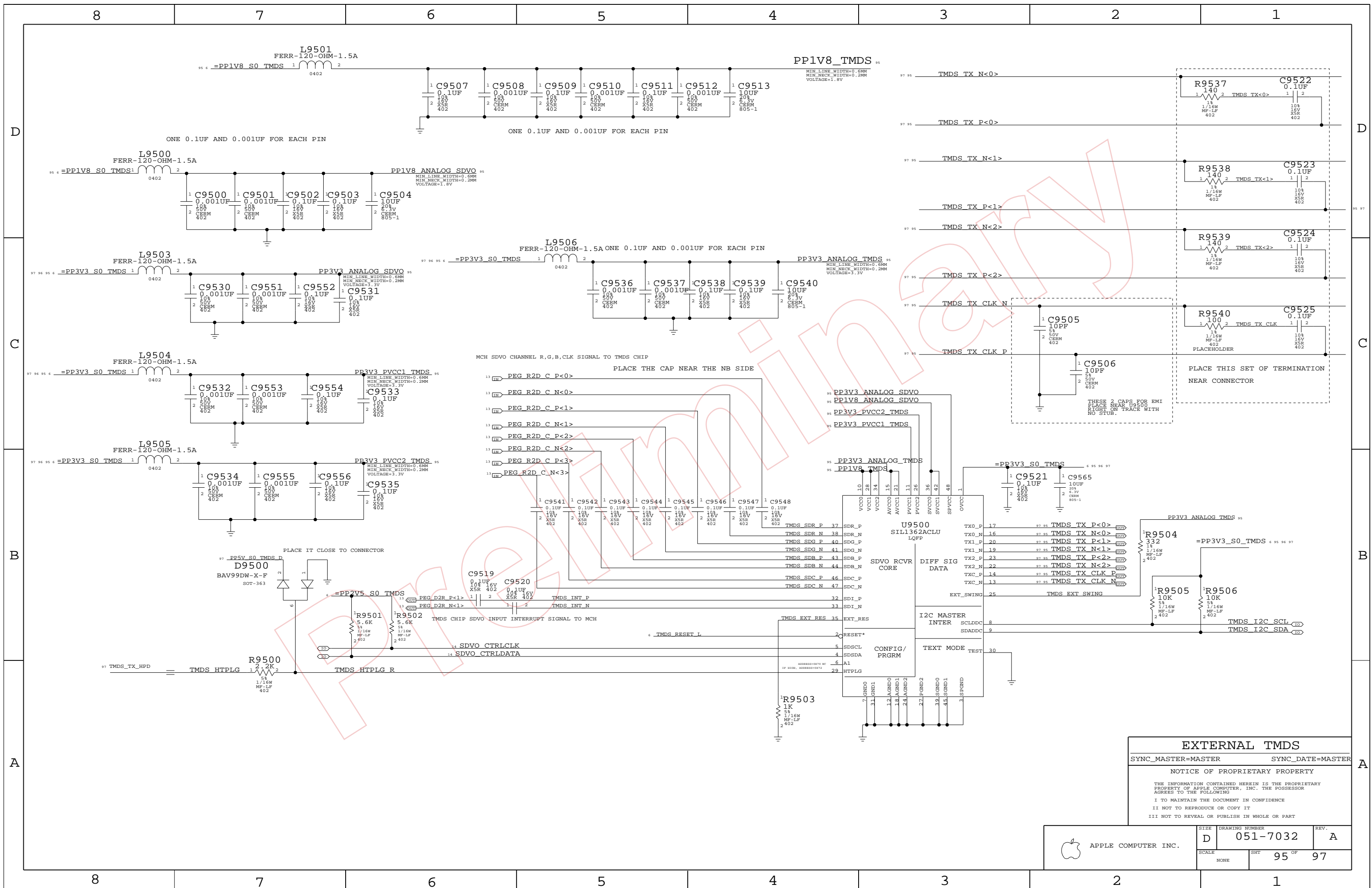
# INVERTER INTERFACE



**Internal Display Conns**  
 SYNC\_MASTER=MASTER SYNC\_DATE=MASTER  
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**EXTERNAL TMSD**

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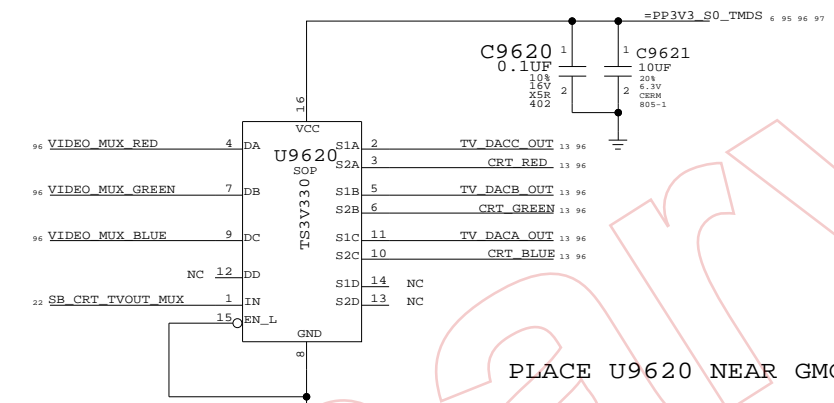
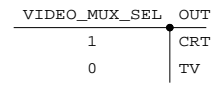
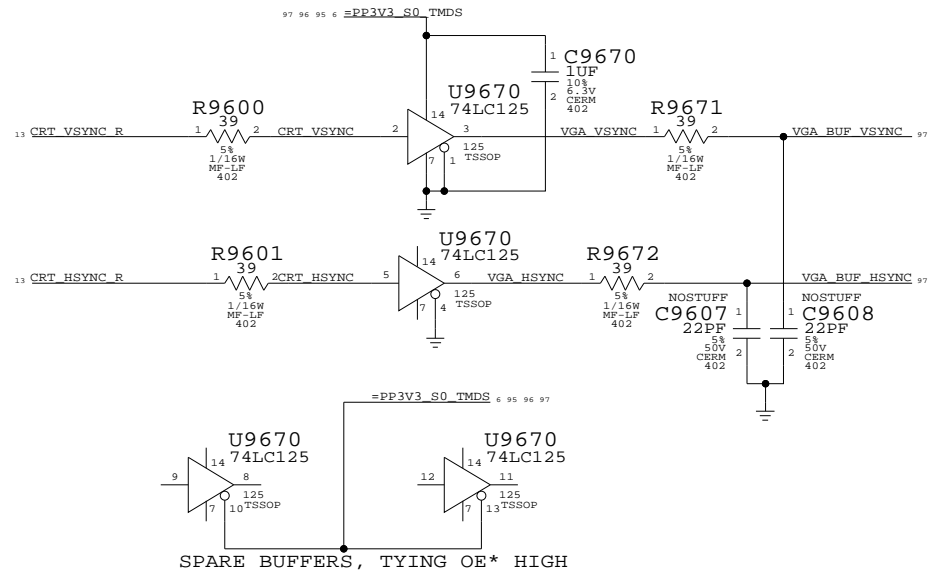
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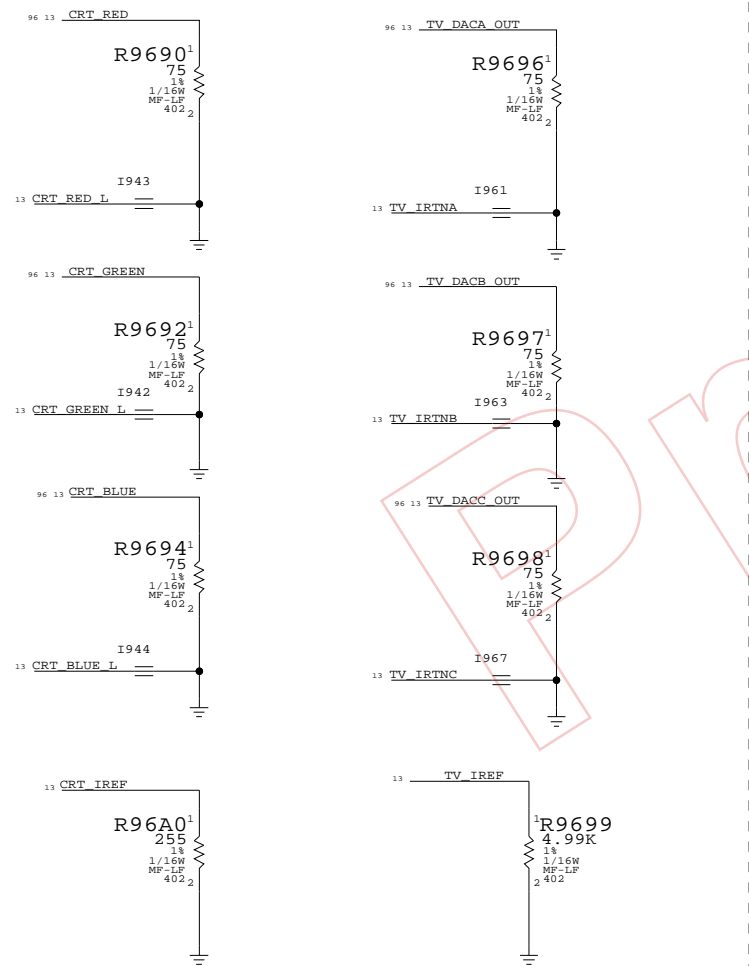
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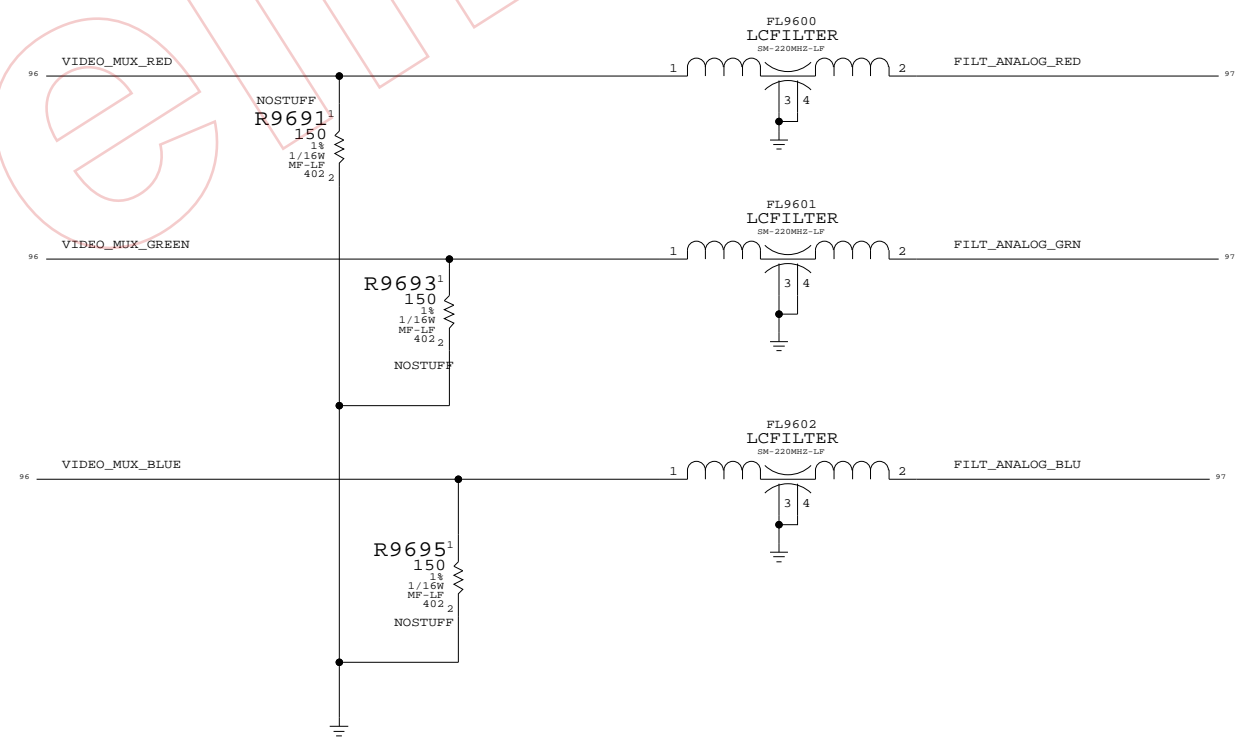
# VGA SYNC BUFFERS



## PLACE RESISTORS AT NORTHBRIDGE

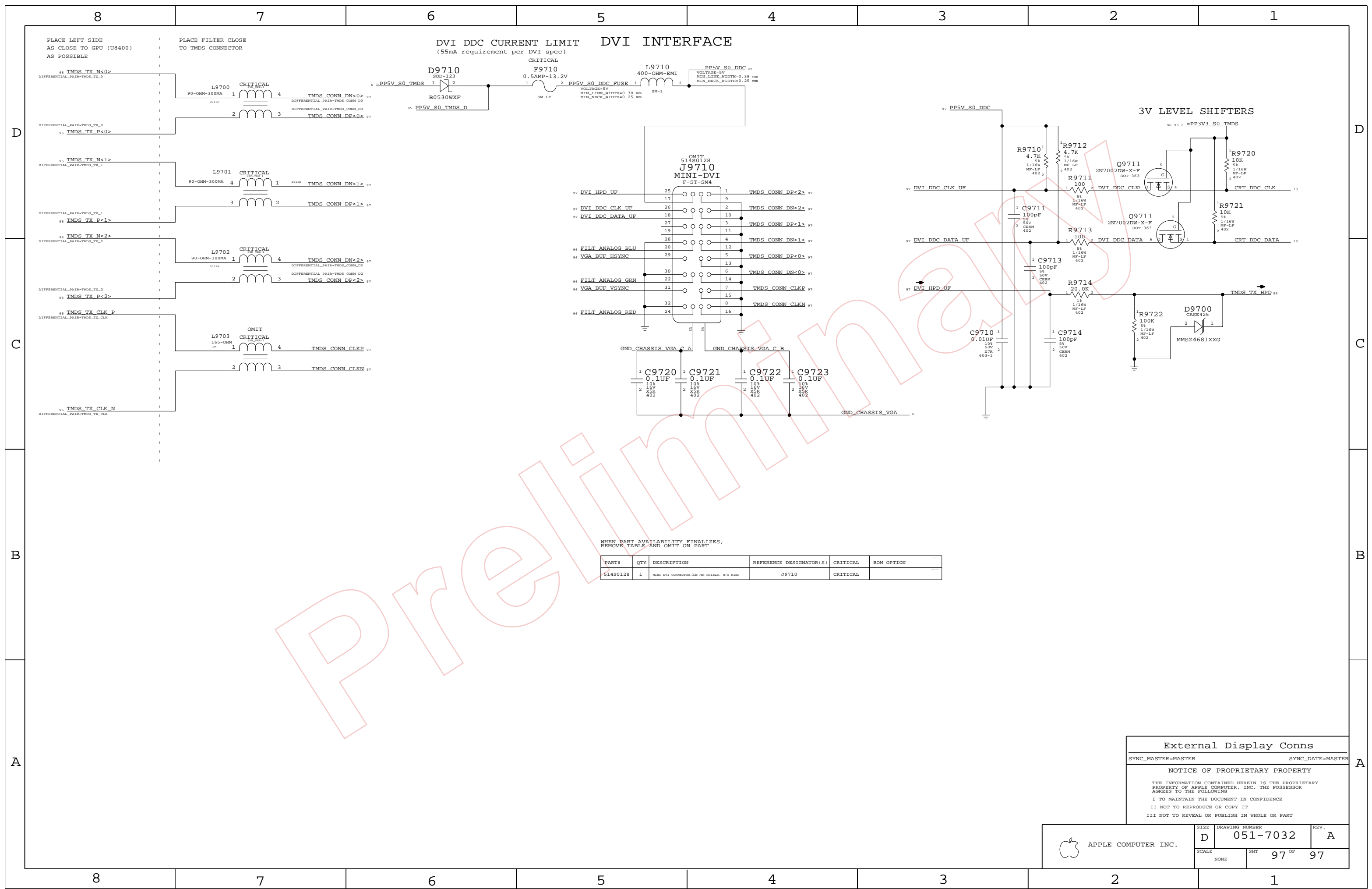


## ANALOG FILTERING PLACE BY CONNECTOR



**TMDS/Inverter/ExtVGA**  
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NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

DVI INTERFACE

MINI-DVI

F-ST-SM4

WHEN PART AVAILABILITY FINALIZES, REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 32P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns

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