1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M38 - DVT

11/16/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
09		400372	ENGINEERING RELEASED	09/16/05	06/22/04

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

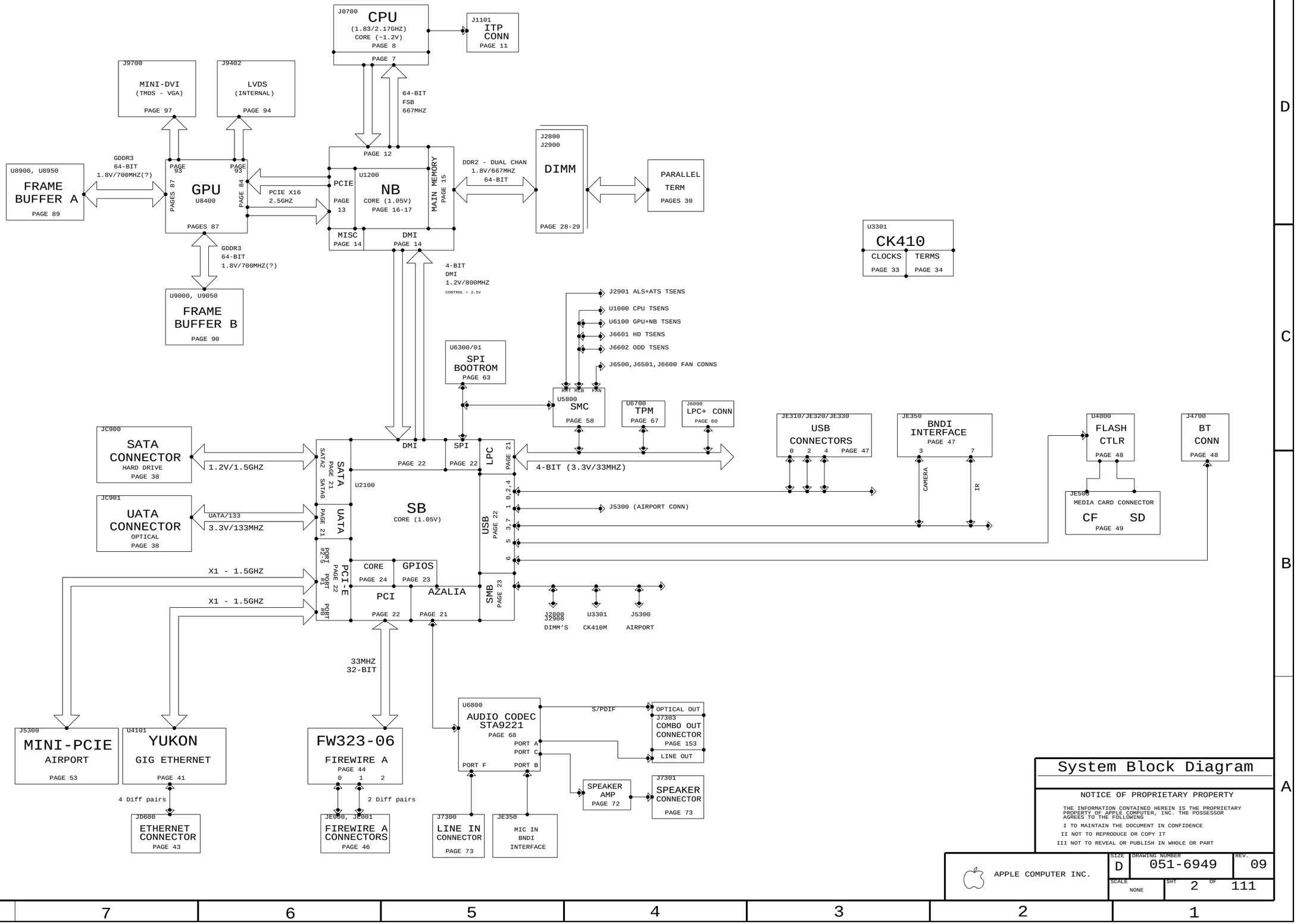
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE: SCHEM,M38

DRAWING NUMBER 051-6949 REV. 09

SHT 1 OF 111



System Block Diagram

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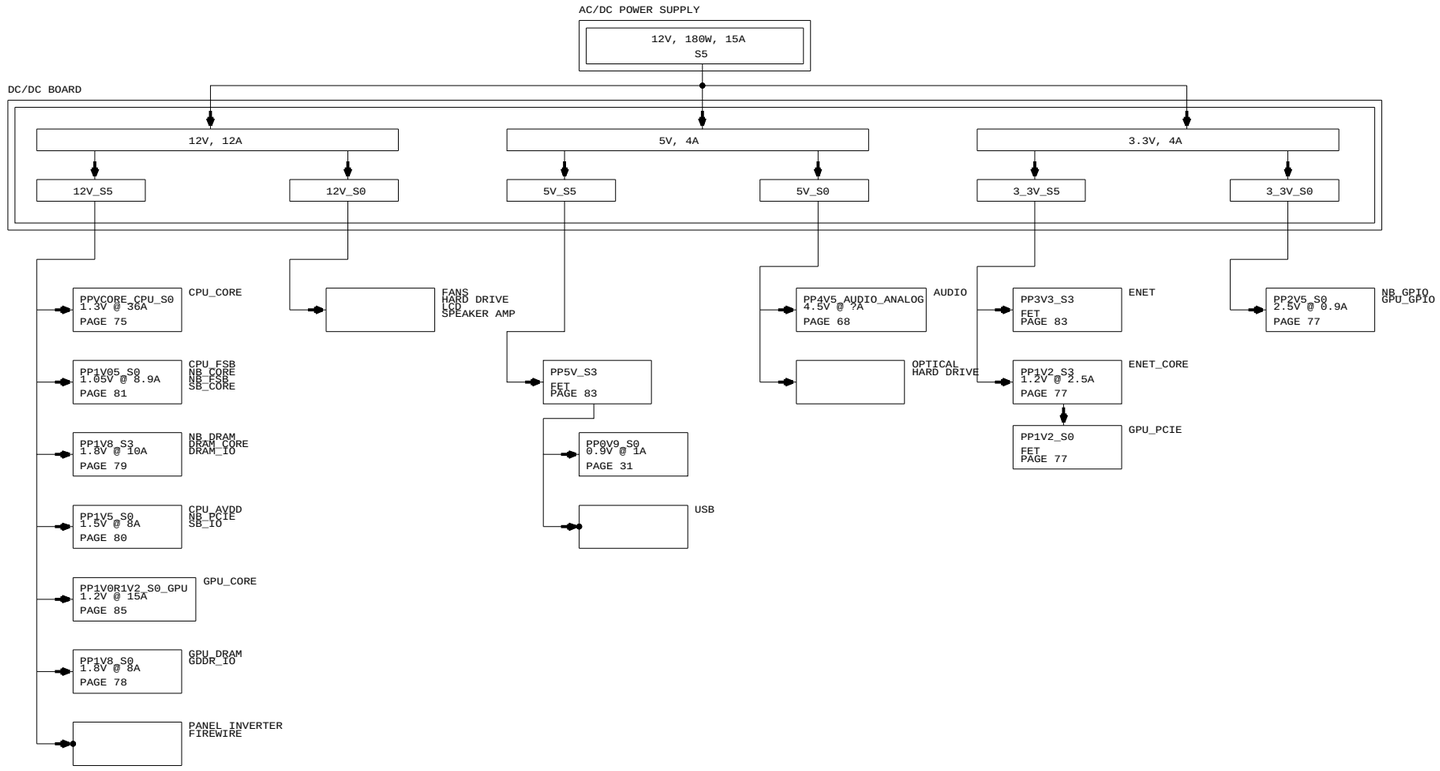
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 2 OF 111	



Power Block Diagram

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6949 | REV. 09

SCALE NONE | SHT 3 OF 111

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
	338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
	343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
	742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
	359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
	338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
	338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
	338S0274	1	IC,SMC,HS8/2116,BLANK	U5800	CRITICAL	
	341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
	353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	
	338S0266	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_B24
	338S0305	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_A24
	128S0078	3	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16CE680KX 680UF 16V LF
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330FS 330UF 6.3V LF
128S0080	128S0078		C7517,C7518,C7910	SANYO 16SVP330M 330UF 16V SMD LF
197S0177	197S0020		Y4101	XTAL,25MHZ,50PPM,16PF,3.2X2.5 SMD,LF
338S0302	338S0266		U8400	IC,ATI,M36D,GRAFIX CTLR,880BGA,LF

M38

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-6949	1	PCB,SCHEM,MLB,M38	SCH1		17_INCH_LCD
	820-1919	1	PCB,FAB,MLB,M38	MLB1		17_INCH_LCD
(335S0384)	341T0003	1	EFI ROM,M38	U6301	CRITICAL	17_INCH_LCD
	337S3241	1	M38/M39 LOW-SPEED CPU (QINY)	CPU	CRITICAL	CPU_M38
	337S3242	1	M00-SPEED CPU (QINZ)	CPU	CRITICAL	CPU_M00

M39

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-6950	1	PCB,SCHEM,MLB,M39	SCH1		20_INCH_LCD
	820-1888	1	PCB,FAB,MLB,M39	MLB1		20_INCH_LCD
(335S0384)	341T0004	1	EFI ROM,M39	U6301	CRITICAL	20_INCH_LCD
	337S3243	1	M39 HI-SPEED CPU (QHJJ)	CPU	CRITICAL	CPU_M39

M38 / M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX

M39 - CTO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX

Table Items

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6949 | REV. 09

SCALE NONE | SHT 4 OF 111

LAYOUT NOTE: PLACE NEAR J0700

12 7 5	FSB_A_L<6>	PP600	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP601	OMIT P4MM
12 7 5	FSB_A_L<27>	PP602	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP603	OMIT P4MM
12 7 5	FSB_D_L<0>	PP604	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP605	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP606	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP607	OMIT P4MM
12 7 5	FSB_D_L<16>	PP608	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP609	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP610	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP611	OMIT P4MM
12 7 5	FSB_D_L<41>	PP612	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP613	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP614	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP615	OMIT P4MM
12 7 5	FSB_D_L<59>	PP616	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP617	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP618	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP619	OMIT P4MM
12 7 5	FSB_LOCK_L	PP620	OMIT P4MM
12 11 7	FSB_CPURST_L	PP621	OMIT P4MM
21 7	CPU_INIT_L	PP622	OMIT P4MM
21 7	CPU_A20M_L	PP623	OMIT P4MM
21 7	CPU_IGNNE_L	PP624	OMIT P4MM
21 7	CPU_STPCLK_L	PP625	OMIT P4MM
21 7	CPU_INTR	PP626	OMIT P4MM
21 7	CPU_NMI	PP627	OMIT P4MM
21 7	CPU_SMI_L	PP628	OMIT P4MM
34 7	FSB_CLK_CPU_P	PP629	OMIT P4MM
34 7	FSB_CLK_CPU_N	PP630	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

34 21	SB_CLK100M_SATA_P	PP6C4	OMIT P4MM
34 21	SB_CLK100M_SATA_N	PP6C5	OMIT P4MM
38 21	IDE_PDIOR_L	PP6C6	OMIT P4MM
38 21	IDE_PDIORDY	PP6C7	OMIT P4MM
38 21	IDE_PDD<9>	PP6C8	OMIT P4MM
34 22	PCI_CLK_SB	PP6D0	OMIT P4MM
41 22	PCIE_A_D2R_P	PP6D1	OMIT P4MM
41 22	PCIE_A_D2R_N	PP6D2	OMIT P4MM
53 22	PCIE_B_D2R_P	PP5E1	OMIT P4MM
53 22	PCIE_B_D2R_N	PP5E2	OMIT P4MM
22 14	DMI_N2S_P<0>	PP6D3	OMIT P4MM
22 14	DMI_N2S_N<0>	PP6D4	OMIT P4MM
34 22	SB_CLK100M_DMI_P	PP6D5	OMIT P4MM
34 22	SB_CLK100M_DMI_N	PP6D6	OMIT P4MM
58 26 23	PM_SYSRST_L	PP6D7	OMIT P4MM
58 44 23 67 60	PM_CLKRUN_L	PP6D8	OMIT P4MM
34 23	SB_CLK14P3M_TIMER	PP6D9	OMIT P4MM
34 23	SB_CLK48M_USBCTLR	PP6E0	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1200

12 7 5	FSB_A_L<6>	PP631	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP632	OMIT P4MM
12 7 5	FSB_A_L<27>	PP633	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP634	OMIT P4MM
12 7 5	FSB_D_L<0>	PP635	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP636	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP637	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP638	OMIT P4MM
12 7 5	FSB_D_L<16>	PP639	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP640	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP641	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP642	OMIT P4MM
12 7 5	FSB_D_L<41>	PP643	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP644	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP645	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP646	OMIT P4MM
12 7 5	FSB_D_L<59>	PP647	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP648	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP649	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP650	OMIT P4MM
12 7 5	FSB_LOCK_L	PP651	OMIT P4MM
12 7	FSB_HIT_L	PP652	OMIT P4MM
12 7	FSB_HITM_L	PP653	OMIT P4MM
12 7	FSB_BNR_L	PP654	OMIT P4MM
12 7	FSB_BREQ0_L	PP655	OMIT P4MM
12 7	FSB_DBSY_L	PP656	OMIT P4MM
12 7	FSB_DPWR_L	PP657	OMIT P4MM
12 7	FSB_REQ_L<0>	PP658	OMIT P4MM
12 7	FSB_REQ_L<1>	PP659	OMIT P4MM
12 7	FSB_REQ_L<2>	PP660	OMIT P4MM
12 7	FSB_REQ_L<3>	PP661	OMIT P4MM
12 7	FSB_REQ_L<4>	PP662	OMIT P4MM
34 12	FSB_CLK_NB_P	PP663	OMIT P4MM
34 12	FSB_CLK_NB_N	PP664	OMIT P4MM
75 26 14	VR_PWRGOOD_DELAY	PP665	OMIT P4MM
14	NB_RST_IN_L_R	PP666	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_P	PP667	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_N	PP668	OMIT P4MM
22 14	DMI_S2N_N<0>	PP673	OMIT P4MM
22 14	DMI_S2N_P<0>	PP674	OMIT P4MM
19 14	MEM_VREF_NB_0	PP6E1	OMIT P4MM
19 14	MEM_VREF_NB_1	PP675	OMIT P4MM
28 15	MEM_A_DQ<7>	PP676	OMIT P4MM
28 15	MEM_A_DQ<14>	PP677	OMIT P4MM
28 15	MEM_A_DQ<16>	PP678	OMIT P4MM
28 15	MEM_A_DQ<25>	PP679	OMIT P4MM
28 15	MEM_A_DQ<39>	PP680	OMIT P4MM
28 15	MEM_A_DQ<47>	PP681	OMIT P4MM
28 15	MEM_A_DQ<54>	PP682	OMIT P4MM
28 15	MEM_A_DQ<59>	PP683	OMIT P4MM
29 15	MEM_A_DQS_P<0>	PP684	OMIT P4MM
28 15	MEM_A_DQS_N<0>	PP685	OMIT P4MM
28 15	MEM_A_DQS_P<1>	PP686	OMIT P4MM
28 15	MEM_A_DQS_N<1>	PP687	OMIT P4MM
28 15	MEM_A_DQS_P<2>	PP688	OMIT P4MM
28 15	MEM_A_DQS_N<2>	PP689	OMIT P4MM
28 15	MEM_A_DQS_P<3>	PP690	OMIT P4MM
28 15	MEM_A_DQS_N<3>	PP691	OMIT P4MM
28 15	MEM_A_DQS_P<4>	PP692	OMIT P4MM
28 15	MEM_A_DQS_N<4>	PP693	OMIT P4MM
28 15	MEM_A_DQS_P<5>	PP694	OMIT P4MM
28 15	MEM_A_DQS_N<5>	PP695	OMIT P4MM
28 15	MEM_A_DQS_P<6>	PP696	OMIT P4MM
28 15	MEM_A_DQS_N<6>	PP697	OMIT P4MM
28 15	MEM_A_DQS_P<7>	PP698	OMIT P4MM
28 15	MEM_A_DQS_N<7>	PP699	OMIT P4MM
29 15	MEM_B_DQ<6>	PP6A0	OMIT P4MM
29 15	MEM_B_DQ<8>	PP6A1	OMIT P4MM
29 15	MEM_B_DQ<23>	PP6A2	OMIT P4MM
29 15	MEM_B_DQ<25>	PP6A3	OMIT P4MM
29 15	MEM_B_DQ<38>	PP6A4	OMIT P4MM
29 15	MEM_B_DQ<44>	PP6A5	OMIT P4MM
29 15	MEM_B_DQ<48>	PP6A6	OMIT P4MM
29 15	MEM_B_DQ<62>	PP6A7	OMIT P4MM
29 15	MEM_B_DQS_P<0>	PP6A8	OMIT P4MM
29 15	MEM_B_DQS_N<0>	PP6A9	OMIT P4MM
29 15	MEM_B_DQS_P<1>	PP6B0	OMIT P4MM
29 15	MEM_B_DQS_N<1>	PP6B1	OMIT P4MM
29 15	MEM_B_DQS_P<2>	PP6B2	OMIT P4MM
29 15	MEM_B_DQS_N<2>	PP6B3	OMIT P4MM
29 15	MEM_B_DQS_P<3>	PP6B4	OMIT P4MM
29 15	MEM_B_DQS_N<3>	PP6B5	OMIT P4MM
29 15	MEM_B_DQS_P<4>	PP6B6	OMIT P4MM
29 15	MEM_B_DQS_N<4>	PP6B7	OMIT P4MM
29 15	MEM_B_DQS_P<5>	PP6B8	OMIT P4MM
29 15	MEM_B_DQS_N<5>	PP6B9	OMIT P4MM
29 15	MEM_B_DQS_P<6>	PP6C0	OMIT P4MM
29 15	MEM_B_DQS_N<6>	PP6C1	OMIT P4MM
29 15	MEM_B_DQS_P<7>	PP6C2	OMIT P4MM
29 15	MEM_B_DQS_N<7>	PP6C3	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U8400

89 87 5	FB_A_DQ<0>	PP8700	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8701	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8702	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8703	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8704	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8705	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8706	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8707	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8708	OMIT P4MM
89 87	FB_A_RDQS<0>	PP8709	OMIT P4MM
89 87	FB_A_RDQS<1>	PP8710	OMIT P4MM
89 87	FB_A_RDQS<2>	PP8711	OMIT P4MM
89 87	FB_A_RDQS<3>	PP8712	OMIT P4MM
89 87	FB_A_RDQS<4>	PP8713	OMIT P4MM
89 87	FB_A_RDQS<5>	PP8714	OMIT P4MM
89 87	FB_A_RDQS<6>	PP8715	OMIT P4MM
89 87	FB_A_RDQS<7>	PP8716	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP8720	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP8721	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP8722	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP8723	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP8724	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP8725	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP8726	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP8727	OMIT P4MM
90 87 5	FB_B_MA<3>	PP8728	OMIT P4MM
90 87	FB_B_RDQS<0>	PP8729	OMIT P4MM
90 87	FB_B_RDQS<1>	PP8730	OMIT P4MM
90 87	FB_B_RDQS<2>	PP8731	OMIT P4MM
90 87	FB_B_RDQS<3>	PP8732	OMIT P4MM
90 87	FB_B_RDQS<4>	PP8733	OMIT P4MM
90 87	FB_B_RDQS<5>	PP8734	OMIT P4MM
90 87	FB_B_RDQS<6>	PP8735	OMIT P4MM
90 87	FB_B_RDQS<7>	PP8736	OMIT P4MM
84 34	GPU_CLK100M_PCIE_P	PP8400	OMIT P4MM
84 34	GPU_CLK100M_PCIE_N	PP8401	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4101

41 34	ENET_CLK100M_PCIE_P	PP4100	OMIT P4MM
41 34	ENET_CLK100M_PCIE_N	PP4101	OMIT P4MM

PLACE NEAR U8900

89 87	FB_A_CKE<0>	PP8900	OMIT P4MM
89 87	FB_A_CLK_P<0>	PP8901	OMIT P4MM
89 87	FB_A_CLK_N<0>	PP8902	OMIT P4MM
89 87	FB_A_CS_L<0>	PP8903	OMIT P4MM
89 87	FB_A_WE_L<0>	PP8904	OMIT P4MM
89 87	FB_A_CAS_L<0>	PP8905	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8906	OMIT P4MM
89 87	FB_A_RAS_L<0>	PP8907	OMIT P4MM
90 89 88 5	DRAM_RST	PP8908	OMIT P4MM
89 87	FB_A_WDQS<0>	PP8909	OMIT P4MM
89 87	FB_A_WDQS<1>	PP8910	OMIT P4MM
89 87	FB_A_WDQS<3>	PP8911	OMIT P4MM
89 87	FB_A_WDQS<2>	PP8912	OMIT P4MM
89 87 5	FB_A_DQ<0>	PP8913	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8914	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8915	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8916	OMIT P4MM

PLACE NEAR U8950

89 87	FB_A_CKE<1>	PP8920	OMIT P4MM
89 87	FB_A_CLK_P<1>	PP8921	OMIT P4MM
89 87	FB_A_CLK_N<1>	PP8922	OMIT P4MM
89 87	FB_A_CS_L<1>	PP8923	OMIT P4MM
89 87	FB_A_WE_L<1>	PP8924	OMIT P4MM
89 87	FB_A_CAS_L<1>	PP8925	OMIT P4MM
89 87	FB_A_RAS_L<1>	PP8926	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8927	OMIT P4MM
90 89 88 5	DRAM_RST	PP8928	OMIT P4MM
89 87	FB_A_WDQS<5>	PP8929	OMIT P4MM
89 87	FB_A_WDQS<6>	PP8930	OMIT P4MM
89 87	FB_A_WDQS<4>	PP8931	OMIT P4MM
89 87	FB_A_WDQS<7>	PP8932	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8933	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8934	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8935	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8936	OMIT P4MM

PLACE NEAR U9000

90 87	FB_B_CKE<0>	PP9000	OMIT P4MM
90 87	FB_B_CLK_P<0>	PP9001	OMIT P4MM
90 87	FB_B_CLK_N<0>	PP9002	OMIT P4MM
90 87	FB_B_CS_L<0>	PP9003	OMIT P4MM
90 87	FB_B_WE_L<0>	PP9004	OMIT P4MM
90 87	FB_B_CAS_L<0>	PP9005	OMIT P4MM
90 87	FB_B_RAS_L<0>	PP9006	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9007	OMIT P4MM
90 89 88 5	DRAM_RST	PP9008	OMIT P4MM
90 87	FB_B_WDQS<0>	PP9009	OMIT P4MM
90 87	FB_B_WDQS<1>	PP9010	OMIT P4MM
90 87	FB_B_WDQS<3>	PP9011	OMIT P4MM
90 87	FB_B_WDQS<2>	PP9012	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP9013	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP9014	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP9015	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP9016	OMIT P4MM

PLACE NEAR U9050

90 87	FB_B_CKE<1>	PP9020	OMIT P4MM
90 87	FB_B_CLK_P<1>	PP9021	OMIT P4MM
90 87	FB_B_CLK_N<1>	PP9022	OMIT P4MM
90 87	FB_B_CS_L<1>	PP9023	OMIT P4MM
90 87	FB_B_WE_L<1>	PP9024	OMIT P4MM
90 87	FB_B_CAS_L<1>	PP9025	OMIT P4MM
90 87	FB_B_RAS_L<1>	PP9026	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9027	OMIT P4MM
90 89 88 5	DRAM_RST	PP9028	OMIT P4MM
90 87	FB_B_WDQS<5>	PP9029	OMIT P4MM
90 87	FB_B_WDQS<6>	PP9030	OMIT P4MM
90 87	FB_B_WDQS<7>	PP9031	OMIT P4MM
90 87	FB_B_WDQS<4>	PP9032	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP9033	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP9034	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP9035	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP9036	OMIT P4MM

PLACE NEAR R1210 AND R1211

12	NB_FSB_VREF	PP1200	SM-TP50-TOP
19 12 6	=PP1V05_S0_FSB_NB	PP1201	SM-TP50-TOP
		PP1202	SM-TP50-TOP

PLACE NEAR R0705 AND R0706

59 11 9 8 7 6	=PP1V05_S0_CPU	PP700	SM-TP50-TOP
7	CPU_GTLREF	PP701	SM-TP50-TOP
		PP702	SM-TP50-TOP

PLACE NEAR R2800 AND R2801

29 28 6	=PP1V8_S3_MEM	PP2800	SM-TP50-TOP
29 28	MEM_VREF	PP2801	SM-TP50-TOP
		PP2802	SM-TP50-TOP

79 77 76 66 65 59 26 6	TP	PP3V3_S5	FUNC_TEST=TRUE
83 81 80 79 59 6	TP	PP5V_S5	FUNC_TEST=TRUE
88 83 81 80 79 78 6	TP	PP12V_S5	FUNC_TEST=TRUE
83 81 80 79 59 6	TP	PP1V8_S3	FUNC_TEST=TRUE
79 6	TP	PPVCORE_CPU	FUNC_TEST=TRUE
76 75 6	TP	PP3V3_S5_S0_RTC	FUNC_TEST=TRUE
26 25 24 21	TP	8 TESTPOINTS	FUNC_TEST=TRUE

60 59 58	TP	SMC_TCK	FUNC_TEST=TRUE
60 59 58	TP	SMC_TDI	FUNC_TEST=TRUE
60 59 58	TP	SMC_TDO	FUNC_TEST=TRUE
60 59 58	TP	SMC_TMS	FUNC_TEST=TRUE
60 58	TP	SMC_TRST_L	FUNC_TEST=TRUE
60 59 58	TP	SMC_TX_L	FUNC_TEST=TRUE
60 59 58	TP	SMC_RX_L	FUNC_TEST=TRUE
59	TP	SMC_MANUAL_RST_L	FUNC_TEST=TRUE
59 11 7	TP	XDP_TCK	FUNC_TEST=TRUE
59 11 7	TP	XDP_TDI	FUNC_TEST=TRUE
59 11 7	TP	XDP_TDO	FUNC_TEST=TRUE
59 11 7	TP	XDP_TMS	FUNC_TEST=TRUE
59 11 7	TP	XDP_TRST_L	FUNC_TEST=TRUE
59	TP	POWER_BUTTON_L	FUNC_TEST=TRUE
26	TP	SW_RST_BTN_L	FUNC_TEST=TRUE

34	TP	TP_PCI_CLK_SPARE	NO_TEST=TRUE
29	TP	TP_MEM_B_A<14>	NO_TEST=TRUE
29	TP	TP_MEM_B_A<15>	NO_TEST=TRUE

MISC GROUND VIAS

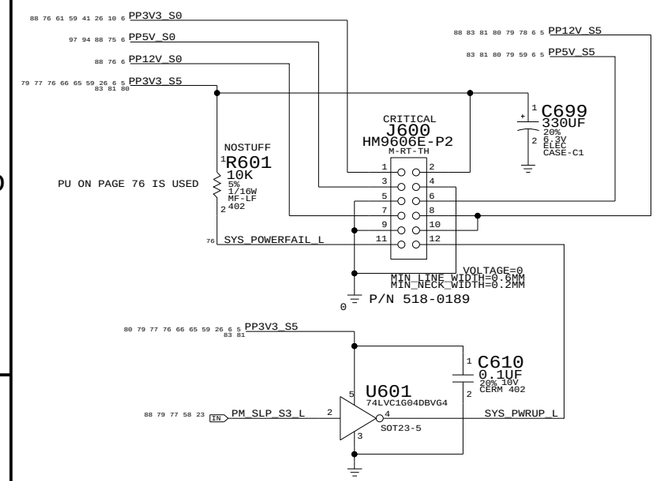
ZH500	HOLE-VIA	ZH510	HOLE-VIA
ZH501	HOLE-VIA	ZH511	HOLE-VIA
ZH502	HOLE-VIA	ZH512	HOLE-VIA
ZH503	HOLE-VIA	ZH513	HOLE-VIA
ZH504	HOLE-VIA	ZH514	HOLE-VIA
ZH505	HOLE-VIA	ZH515	HOLE-VIA
ZH506	HOLE-VIA	ZH516	HOLE-VIA
ZH507	HOLE-VIA	ZH517	HOLE-VIA
ZH508	HOLE-VIA	ZH518	HOLE-VIA
ZH509	HOLE-VIA	ZH519	HOLE-VIA

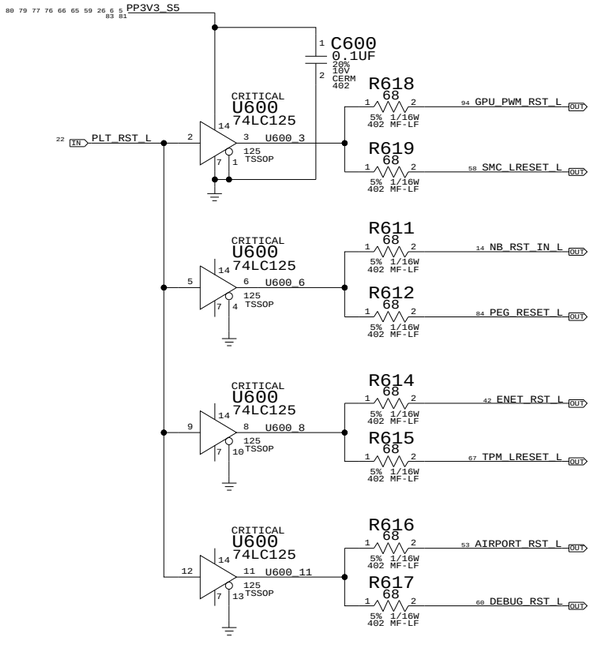
ZH520	HOLE-VIA	
ZH521	HOLE-VIA	
ZH522	HOLE-VIA	
ZH523	HOLE-VIA	
ZH524	HOLE-VIA	
ZH525	HOLE-VIA	
ZH526	HOLE-VIA	
ZH527	HOLE-VIA	
ZH528	HOLE-VIA	
ZH529	HOLE-VIA	

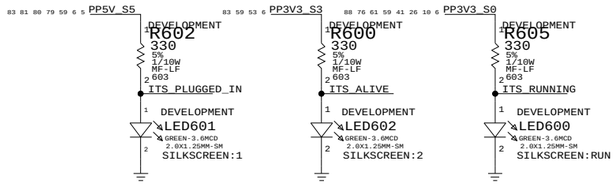
FUNC TEST 1 OF 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 5 OF 111	







"S0" RAILS

ONLY ON IN RUN

- PP0V9_S0 (MAKE_BASE=TRUE, VOLTAGE=0.9V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM) → =PP0V9_S0_MEMVTT_LDO (31), =PP0V9_S0_MEM_TERM (30)
- PPVCORE_CPU (MAKE_BASE=TRUE, VOLTAGE=1.25V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM) → =PPVCORE_S0_CPU (8 9 76)
- PP1V05_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM) → =PPVCORE_S0_NB (16 19), =PP1V05_S0_CPU (5 7 8 9 11 59), =PP1V05_S0_FSB_NB (5 12 19), =PP1V05_S0_NB_VTT (17 19), =PP1V05_S0_NB (19), =PP1V05_S0_SB_CPU_IO (21 24 25), =PPVCORE_S0_SB (24 25)
- PP1V5_S0 (MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM) → =PP1V5_S0_CPU (8), =PP1V5_S0_NB_PCIE (13 19), =PP1V5_S0_NB_VCCAUX (6 16 17 19), =PP1V5_S0_NB_VCCD_HMPLL (17 19), =PP1V5_S0_NB_VCCAUX (6 16 17 19), =PP1V5_S0_NB_PLL (19), =PP1V5_S0_NB (19), =PP1V5_S0_NB_TVDAC (19), =PP1V5_S0_NB_3GPLL (19), =PP1V5_S0_SB_VCC1_5_A_ARX (24 25), =PP1V5_S0_SB_VCCSATAPLL (24 25), =PP1V5_S0_SB_VCC1_5_A_ATX (24 25), =PP1V5_S0_SB_VCCUSBPLL (24 25), =PP1V5_S0_SB_VCC1_5_A_USB_CORE (24 25), =PP1V5_S0_SB_VCC1_5_A (24 25), =PP1V5_S0_SB (25), =PP1V5_S0_AIRPORT (53)
- PP2V5_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM) → =PP2V5_S0_NB_VCCA_3GBG (17 19)
- PP3V3_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM) → =PP3V3_S0_NB_PM, =PP3V3_S0_NB_VCC_HV (17 19), =PP3V3_S0_NB_TVDAC (19), =PP3V3_S0_SB (22 25), =PP3V3_S0_SB_GPIO (21 23), =PP3V3_S0_SB_VCC3_3 (24 25), =PP3V3_S0_SB_VCC3_3_PCI (24 25), =PP3V3_S0_SB_VCC3_3_IDE (24 25), =PP3V3_S0_SB_PCI (26), =PP3V3_S0_SB_PM (26), =PP3V3_S0_PATA (38), =PP3V3_S0_FAN (59 65 66), =PP3V3_S0_HD_TSENS (66), =PP3V3_S0_ODD_TSENS (66), =PP3V3_S0_SB_3V3_1V5_VCCHDA (24 25), =PP3V3_S0_TPM (67), =PPSPD_S0_MEM (28 29), =PP3V3_S0_CK410 (33 34), =PP3V3_S0_IMVP (75), =PP3V3_S0_AUDIO (68 72 73 74), =PP3V3_S0_PCI (44), =PP3V3_S0_SB_VCCLAN3_3 (24 25), =PP3V3_S0_AIRPORT (53), =PP3V3_S0_2V5REG (77), =PP3V3_S0_NB (14 19 20)
- PP5V_S0 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM) → =PP5V_S0_SB (25), =PP5V_S0_PATA (38), XW604 SM OMIT: PP5V_S0_AUDIO (MAKE_BASE=TRUE) → =PP5V_S0_AUDIO (68); =PP5V_S0_DEBUG (60)
- PP12V_S0 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM) → =PP12V_S0_FAN (65 66), XW605 SM OMIT: PP12V_S0_AUDIO_SPKRAMP (MAKE_BASE=TRUE) → =PP12V_S0_AUDIO_SPKRAMP (72)

"S3" RAILS

ON IN RUN AND SLEEP

- PP1V2_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM) → =PP1V2_S3_LAN (42)
- PP1V8_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM) → =PP1V8_S3_MEM_NB (6 14 16 19), =PP1V8_S3_MEM_NB (6 14 16 19), =PP1V8_S3_MEM (5 28 29), =PP1V8_S0_MEMVTT (31)
- PP3V3_S3 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) → =PP3V3_S3_ENET (41 42 43), =PP3V3_S3_TPM (67), =PP3V3_S3_1V2REG (77), =PP3V3_S3_BT (47), =PP3V3_S3_USB (49), =PP3V3_S3_VGASYNC (97)
- PP5V_S3 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) → =PP5V_S3_USB (47), =PP5V_S3_BNDI (47), =PP5V_S0_MEMVTT (31)

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

- PP3V3_S5 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM) → =PP3V3_S5_SB (23 25 26), =PP3V3_S5_SB_USB (22), =PP3V3_S5_SB_PM (11 23), =PP3V3_S5_SB_VCCSUS3_3 (24 25), =PP3V3_S5_SB_VCCSUS3_3_USB (24 25), =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA (24), =PP3V3_S5_SB_IO (22 27), =PP3V3_S5_FW (44 45 46), =PP3V3_S5_SMC (58 59), =PP3V3_S5_DEBUG (60), =PP3V3_S5_ROM (63)
- PP5V_S5 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM) → =PP5V_S5_SB (25)
- PP12V_S5 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM) → =PP12V_S5_FW (46), =PP12V_S5_CPU (76)

GND RAILS

XW601 SM NOSTUFF: GND_AUDIO (74)
XW602 SM NOSTUFF: GND_AUDIO_SPKRAMP (74 72)

CHASSIS GND

NOSTUFF R603 0 5% 1/10W MF-LF 402

- GND_CHASSIS_IO_LEFT (MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- GND_CHASSIS_AUDIO_EXTERNAL (74 73)
- GND_CHASSIS_USB (47)
- GND_CHASSIS_FIREWIRE (46)
- GND_CHASSIS_VGA (97)
- GND_CHASSIS_RJ45 (43)
- GND_CHASSIS_IO_RIGHT (MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- GND_CHASSIS_AUDIO_INTERNAL (73)
- GND_CHASSIS_BNDI (47) (MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0, MAKE_BASE=TRUE)

OMIT ZH604 4P25R3P5 (ZH704P1)
OMIT ZH601 4P25R3P5 (ZH701P1)
OMIT ZH602 4P25R3P5 (ZH702P1)
OMIT ZH603 4P25R3P5 (ZH703P1)
OMIT ZH606 160R138
NOSTUFF C604 0.01UF 20% 16V CERM 402
NOSTUFF C601 0.01UF 20% 16V CERM 402
NOSTUFF C602 0.01UF 20% 16V CERM 402
NOSTUFF C603 0.01UF 20% 16V CERM 402

Power Conn / Alias

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 6 OF 111	

OMIT

J0700
YONAH-SKT
CPU
BGA
(1 OF 4)

ADDR GROUP0

FSB_A_L<3>	J4	A3*
FSB_A_L<4>	L4	A4*
FSB_A_L<5>	M3	A5*
FSB_A_L<6>	K5	A6*
FSB_A_L<7>	M1	A7*
FSB_A_L<8>	N2	A8*
FSB_A_L<9>	J1	A9*
FSB_A_L<10>	N3	A10*
FSB_A_L<11>	P5	A11*
FSB_A_L<12>	P2	A12*
FSB_A_L<13>	L1	A13*
FSB_A_L<14>	P4	A14*
FSB_A_L<15>	P1	A15*
FSB_A_L<16>	R1	A16*
FSB_ADSTB_L<0>	L2	ADSTB0*

ADDR GROUP1

FSB_A_L<17>	Y2	A17*
FSB_A_L<18>	U5	A18*
FSB_A_L<19>	R3	A19*
FSB_A_L<20>	W6	A20*
FSB_A_L<21>	U4	A21*
FSB_A_L<22>	Y5	A22*
FSB_A_L<23>	U2	A23*
FSB_A_L<24>	R4	A24*
FSB_A_L<25>	T5	A25*
FSB_A_L<26>	T3	A26*
FSB_A_L<27>	W3	A27*
FSB_A_L<28>	W5	A28*
FSB_A_L<29>	Y4	A29*
FSB_A_L<30>	W2	A30*
FSB_A_L<31>	Y1	A31*
FSB_ADSTB_L<1>	V4	ADSTB1*

CONTROL

FSB_REQ_L<0>	K3	REQ0*
FSB_REQ_L<1>	H2	REQ1*
FSB_REQ_L<2>	K2	REQ2*
FSB_REQ_L<3>	J3	REQ3*
FSB_REQ_L<4>	L5	REQ4*

ADS*	H1	FSB_ADS_L
BNR*	E2	FSB_BNR_L
BPRI*	G5	FSB_BPRI_L
DEFER*	H5	FSB_DEFER_L
DRDY*	F21	FSB_DRDY_L
DBSY*	E1	FSB_DBSY_L
BR0*	F1	FSB_BREQ0_L
IERR*	D20	FSB_IERR_L
INIT*	B3	CPU_INIT_L
LOCK*	H4	FSB_LOCK_L
RESET*	B1	FSB_CPURST_L
RS0*	F3	FSB_RS_L<0>
RS1*	F4	FSB_RS_L<1>
RS2*	G3	FSB_RS_L<2>
TRDY*	G2	FSB_TRDY_L
HIT*	G6	FSB_HIT_L
HITM*	E4	FSB_HITM_L

XDP/ITP SIGNALS

BPM0*	AD4	XDP_BPM_L<0>
BPM1*	AD3	XDP_BPM_L<1>
BPM2*	AD1	XDP_BPM_L<2>
BPM3*	AC4	XDP_BPM_L<3>
PRDY*	AC2	XDP_BPM_L<4>
PREQ*	AC1	XDP_BPM_L<5>
TCK	AC5	XDP_TCK
TDI	AA6	XDP_TDI
TDO	AB3	XDP_TDO
TMS	AB5	XDP_TMS
TRST*	AB6	XDP_TRST_L
DBR*	C20	XDP_DBRESET_L

NOTE: DUMMY PIN
PIN ACTUALLY DRIVEN BY ITP

THERM

PROCHOT*	D21	CPU_PROCHOT_L
THERMDA	A24	CPU_THERMD_P
THERMDC	A25	CPU_THERMD_N
THERMTRIP*	C7	PM_THRMTRIP_L

HCLK

BCLK0	A22	FSB_CLK_CPU_P
BCLK1	A21	FSB_CLK_CPU_N

CPU_A20M_L	A6	A20M*
CPU_FERR_L	A5	FERR*
CPU_IGNNE_L	C4	IGNNE*
CPU_STPCLK_L	D5	STPCLK*
CPU_INTR	C6	LINT0
CPU_NMI	B4	LINT1
CPU_SMI_L	A3	SMI*

RESERVED

TP_CPU_A32_L	AA1	RSVD1
TP_CPU_A33_L	AA4	RSVD2
TP_CPU_A34_L	AB2	RSVD3
TP_CPU_A35_L	AA3	RSVD4
TP_CPU_A36_L	M4	RSVD5
TP_CPU_A37_L	N5	RSVD6
TP_CPU_A38_L	T2	RSVD7
TP_CPU_A39_L	V3	RSVD8
TP_CPU_APM0_L	B2	RSVD9
TP_CPU_APM1_L	C3	RSVD10
TP_CPU_HFPLL	B25	RSVD11
	T22	RSVD12 — TP_CPU_EXTBREF
	D2	RSVD13 — TP_CPU_SPARE0
	F6	RSVD14 — TP_CPU_SPARE1
	D3	RSVD15 — TP_CPU_SPARE2
	C1	RSVD16 — TP_CPU_SPARE3
	AF1	RSVD17 — TP_CPU_SPARE4
	D22	RSVD18 — TP_CPU_SPARE5
	C23	RSVD19 — TP_CPU_SPARE6
	C24	RSVD20 — TP_CPU_SPARE7

SPARE[7-0],HFPLL:
ROUTE TO TP VIA AND
PLACE GND VIA W/IN 1000 MILS

=PP1V05_S0_CPU

R0702 54.9 1% 1/16W MF-LF 402

CPU SCH AND PCB
SYMBOL NEED TO CHECK

PLACE TESTPOINT ON
FSB_IERR# WITH A GND
0.1" AWAY

=PP1V05_S0_CPU

NOSTUFF
R0703 54.9 1% 1/16W MF-LF 402

R0704 68 5% 1/16W MF-LF 402

NO SPACE FOR ITP
CONNECTOR, NEED TERM
ON ITP SIGNALS?

CPU_PROCHOT_L TO SMC
AND CPU VR TO INFORM
CPU IS HOT

PM_THRMTRIP#
SHOULD CONNECT TO
ICH6-M AND GMCH
WITHOUT T-ING (NO
STUB)

=PP1V05_S0_CPU

R0720 54.9 1% 1/16W MF-LF 402 — XDP_TMS

R0721 54.9 1% 1/16W MF-LF 402 — XDP_TDI

R0722 54.9 1% 1/16W MF-LF 402 — XDP_TCK

OMIT

J0700
YONAH-SKT
CPU
BGA
(2 OF 4)

DATA GRP0

FSB_D_L<0>	E22	D0*
FSB_D_L<1>	F24	D1*
FSB_D_L<2>	E26	D2*
FSB_D_L<3>	H22	D3*
FSB_D_L<4>	F23	D4*
FSB_D_L<5>	G25	D5*
FSB_D_L<6>	E25	D6*
FSB_D_L<7>	E23	D7*
FSB_D_L<8>	K24	D8*
FSB_D_L<9>	G24	D9*
FSB_D_L<10>	J24	D10*
FSB_D_L<11>	J23	D11*
FSB_D_L<12>	H26	D12*
FSB_D_L<13>	F26	D13*
FSB_D_L<14>	K22	D14*
FSB_D_L<15>	H25	D15*
FSB_DSTBN_L<0>	H23	DSTBN0*
FSB_DSTBP_L<0>	G22	DSTBP0*
FSB_DINV_L<0>	J26	DINV0*

DATA GRP1

FSB_D_L<16>	N22	D16*
FSB_D_L<17>	K25	D17*
FSB_D_L<18>	P26	D18*
FSB_D_L<19>	R23	D19*
FSB_D_L<20>	L25	D20*
FSB_D_L<21>	L22	D21*
FSB_D_L<22>	L23	D22*
FSB_D_L<23>	M23	D23*
FSB_D_L<24>	P25	D24*
FSB_D_L<25>	P22	D25*
FSB_D_L<26>	P23	D26*
FSB_D_L<27>	T24	D27*
FSB_D_L<28>	R24	D28*
FSB_D_L<29>	L26	D29*
FSB_D_L<30>	T25	D30*
FSB_D_L<31>	N24	D31*
FSB_DSTBN_L<1>	M24	DSTBN1*
FSB_DSTBP_L<1>	N25	DSTBP1*
FSB_DINV_L<1>	M26	DINV1*

DATA GRP2

D32*	AA23	FSB_D_L<32>
D33*	AB24	FSB_D_L<33>
D34*	V24	FSB_D_L<34>
D35*	V26	FSB_D_L<35>
D36*	W25	FSB_D_L<36>
D37*	U23	FSB_D_L<37>
D38*	U25	FSB_D_L<38>
D39*	U22	FSB_D_L<39>
D40*	AB25	FSB_D_L<40>
D41*	W22	FSB_D_L<41>
D42*	Y23	FSB_D_L<42>
D43*	AA26	FSB_D_L<43>
D44*	Y26	FSB_D_L<44>
D45*	Y22	FSB_D_L<45>
D46*	AC26	FSB_D_L<46>
D47*	AA24	FSB_D_L<47>
DSTBN2*	W24	FSB_DSTBN_L<2>
DSTBP2*	Y25	FSB_DSTBP_L<2>
DINV2*	V23	FSB_DINV_L<2>

DATA GRP3

D48*	AC22	FSB_D_L<48>
D49*	AC23	FSB_D_L<49>
D50*	AB22	FSB_D_L<50>
D51*	AA21	FSB_D_L<51>
D52*	AB21	FSB_D_L<52>
D53*	AC25	FSB_D_L<53>
D54*	AD20	FSB_D_L<54>
D55*	AE22	FSB_D_L<55>
D56*	AF23	FSB_D_L<56>
D57*	AD24	FSB_D_L<57>
D58*	AE21	FSB_D_L<58>
D59*	AD21	FSB_D_L<59>
D60*	AE25	FSB_D_L<60>
D61*	AF25	FSB_D_L<61>
D62*	AF22	FSB_D_L<62>
D63*	AF26	FSB_D_L<63>
DSTBN3*	AD23	FSB_DSTBN_L<3>
DSTBP3*	AE24	FSB_DSTBP_L<3>
DINV3*	AC20	FSB_DINV_L<3>

MISC

COMP0	R26	CPU_COMP<0>
COMP1	U26	CPU_COMP<1>
COMP2	U1	CPU_COMP<2>
COMP3	V1	CPU_COMP<3>
DPRSTP*	E5	CPU_DPRSTP_L
DPSLP*	B5	CPU_DPSLP_L
DPWR*	D24	FSB_DPWR_L
PWRGOOD	D6	CPU_PWRGD
SLP*	D7	FSB_SLPCPU_L
PSI*	AE6	CPU_PSI_L

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402

=PP1V05_S0_CPU

R0705 1K 1% 1/16W MF-LF 402

R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH

CPU_GTLREF

CPU_TEST1

CPU_TEST2

CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

NOSTUFF
R0730 0 402

R0707 51 5% 1/16W MF-LF 402

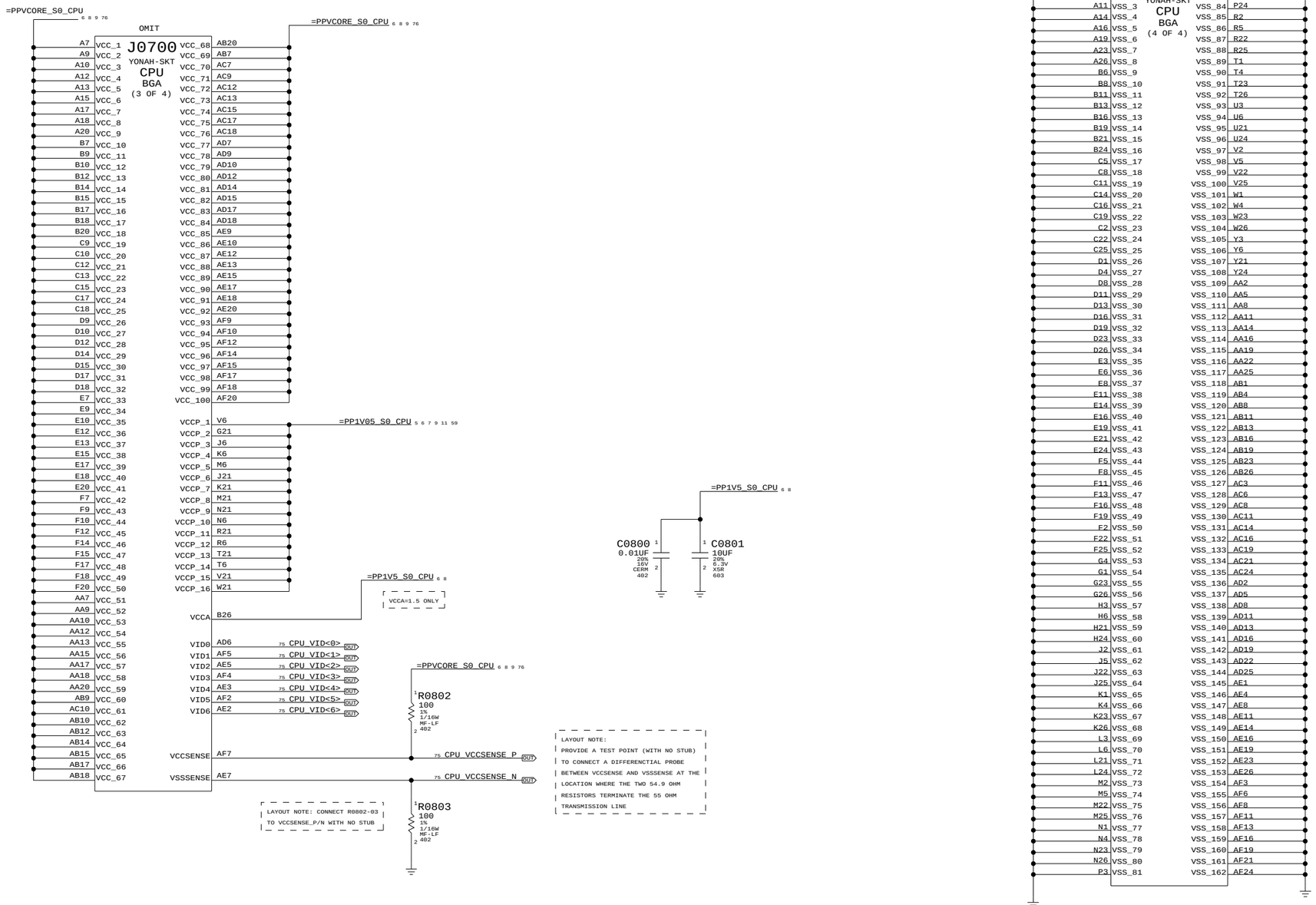
NOSTUFF
R0712 1K 5% 1/16W MF-LF 402

CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 7 OF 111	



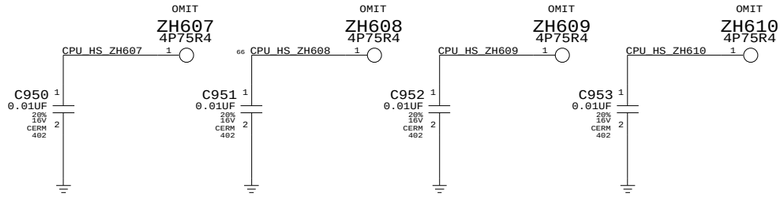
CPU 2 OF 2-PWR/GND

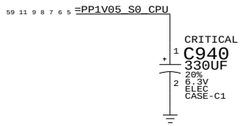
SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE COMPUTER INC.

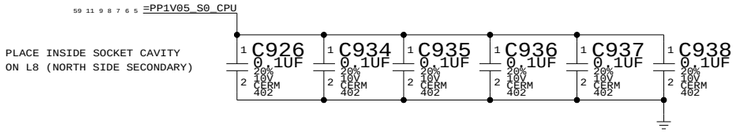
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 8 OF 111	

CPU HEATSINK MOUNTING HOLES

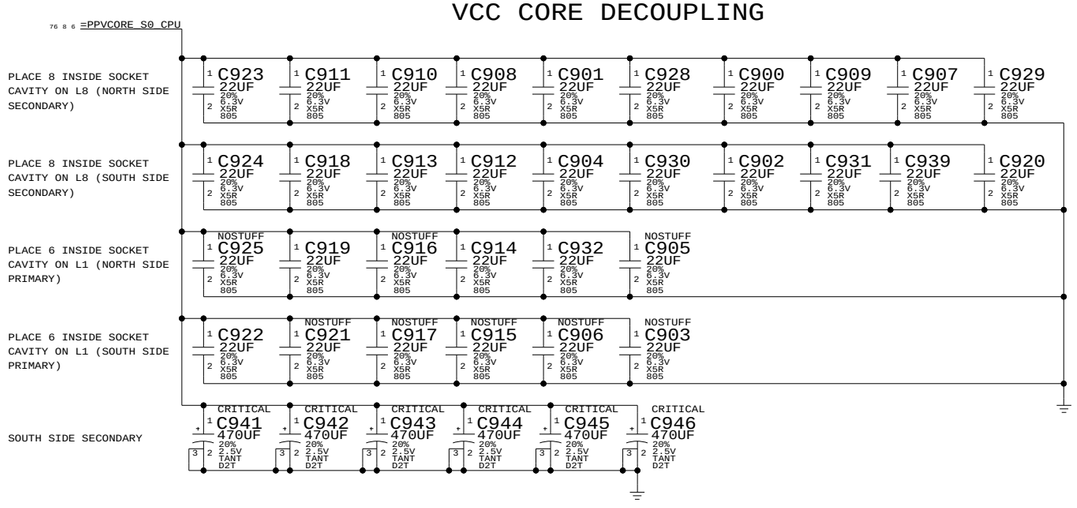




VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

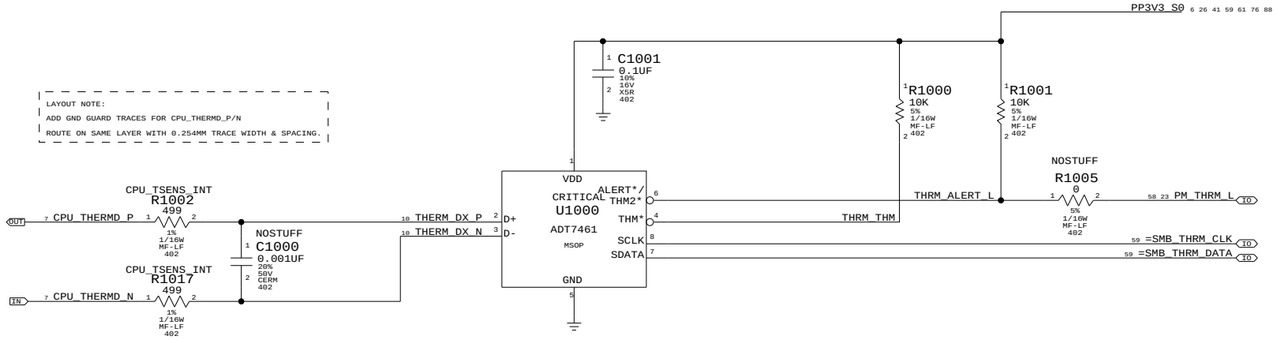
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 9 OF 111	

CPU THERMAL SENSOR

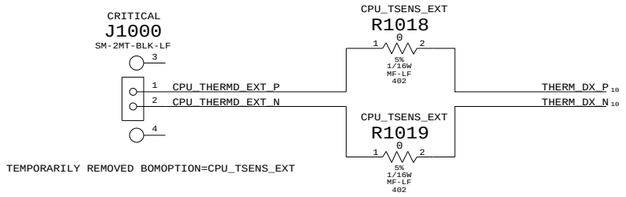
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SHOULD THAT THEY SHARE ONE PAD



TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

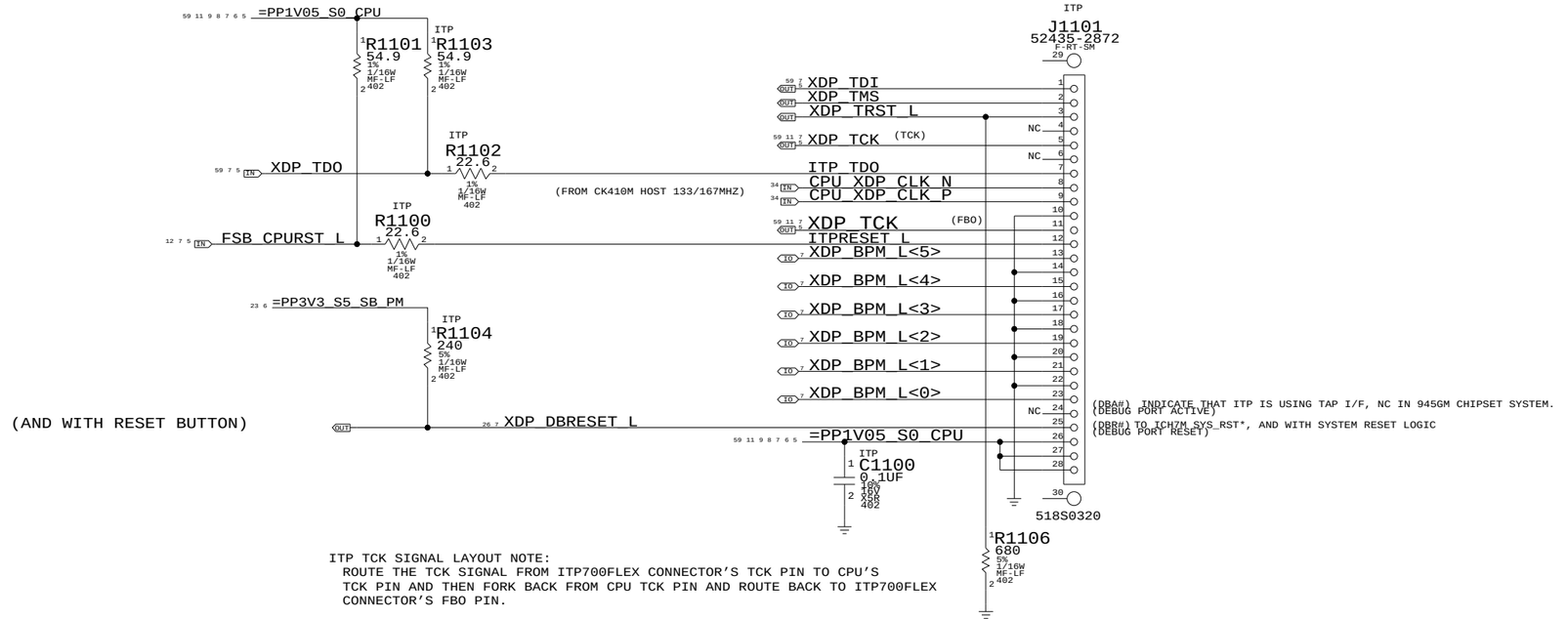
CPU TEMP SENSOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	10	111

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

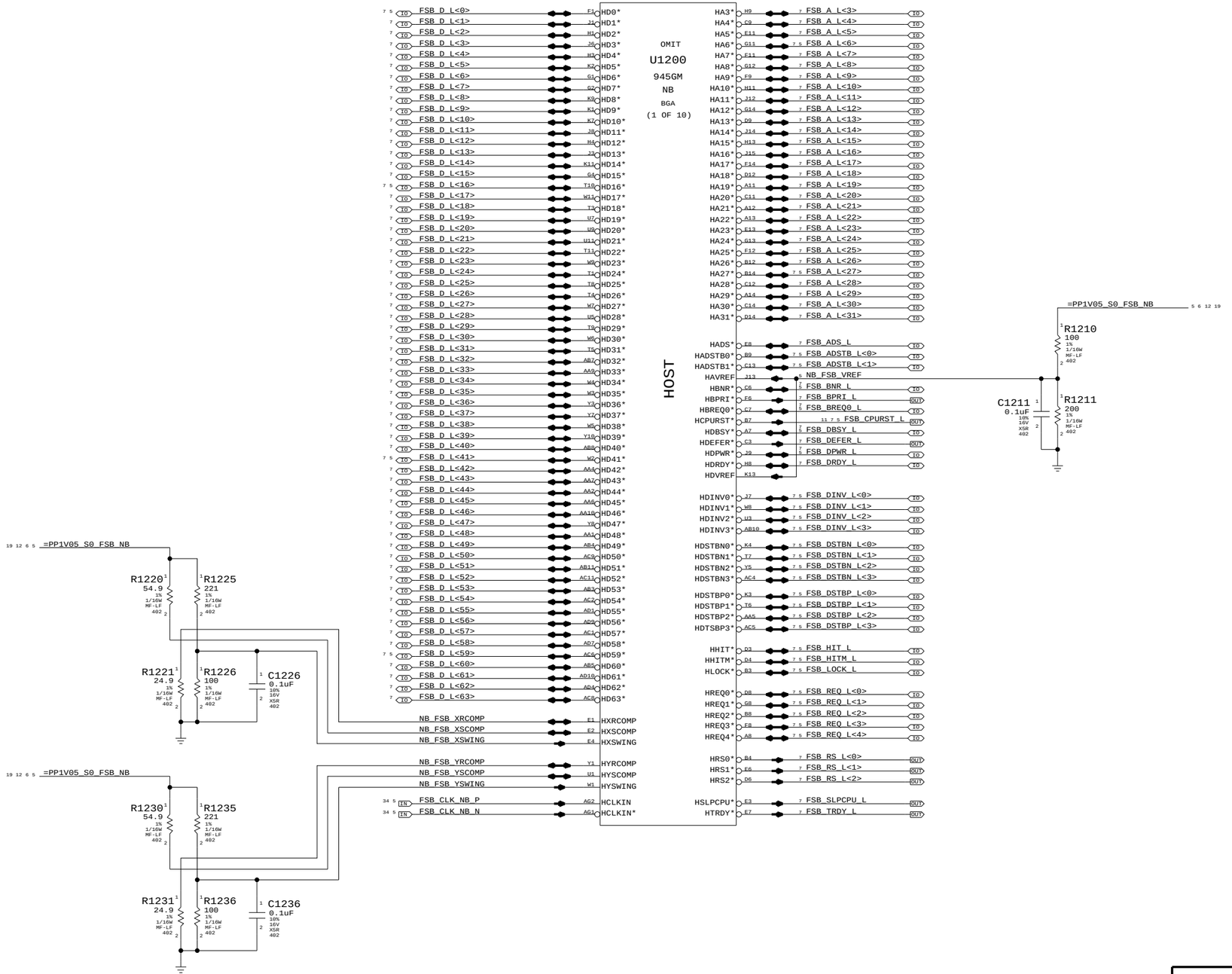
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	11	111



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 12 OF 111	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

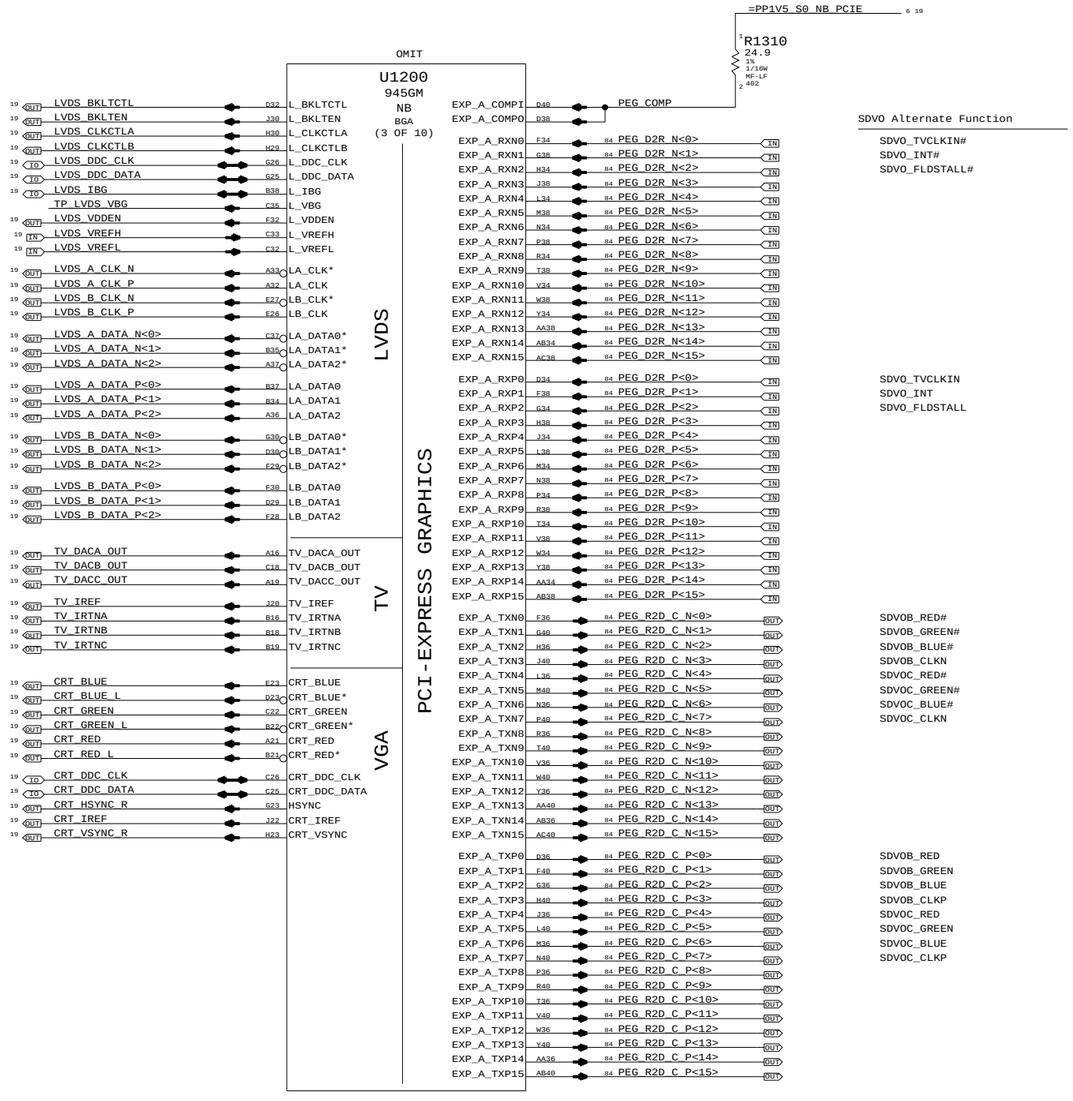
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



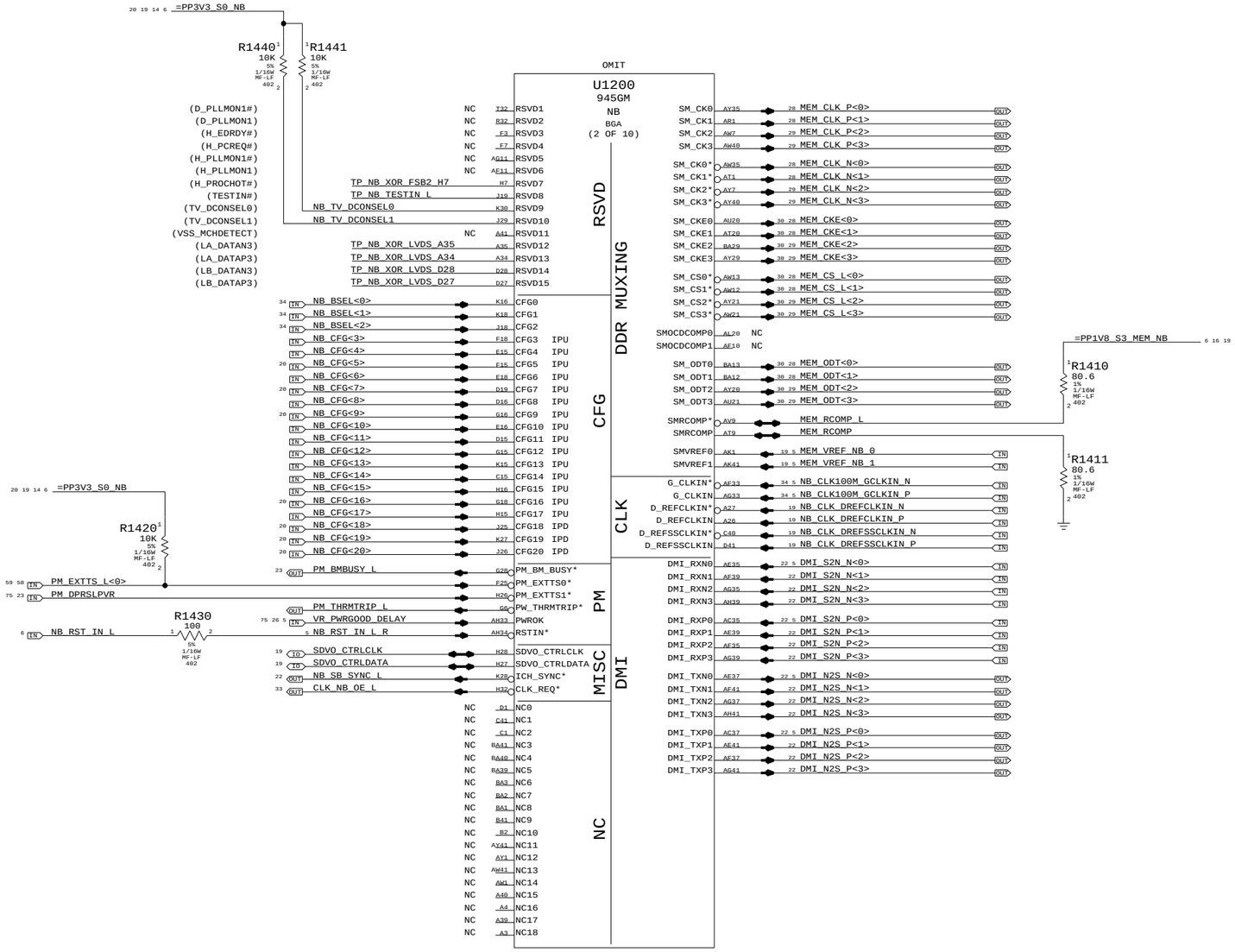
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	13	111



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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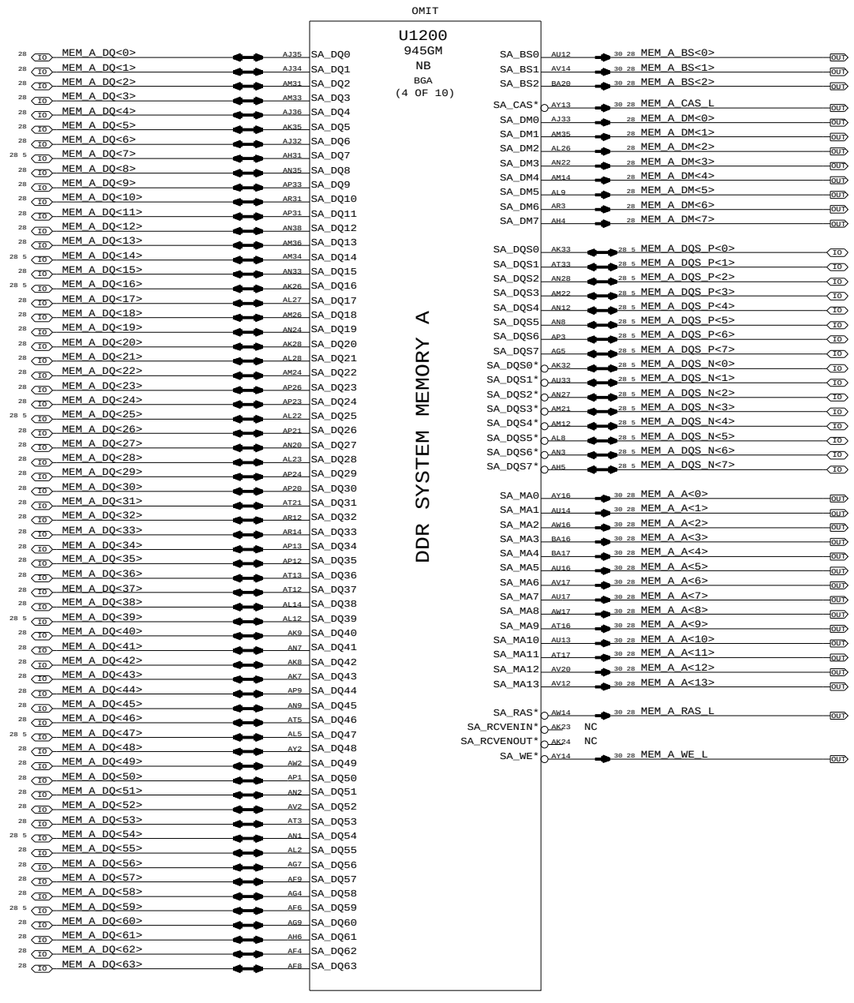
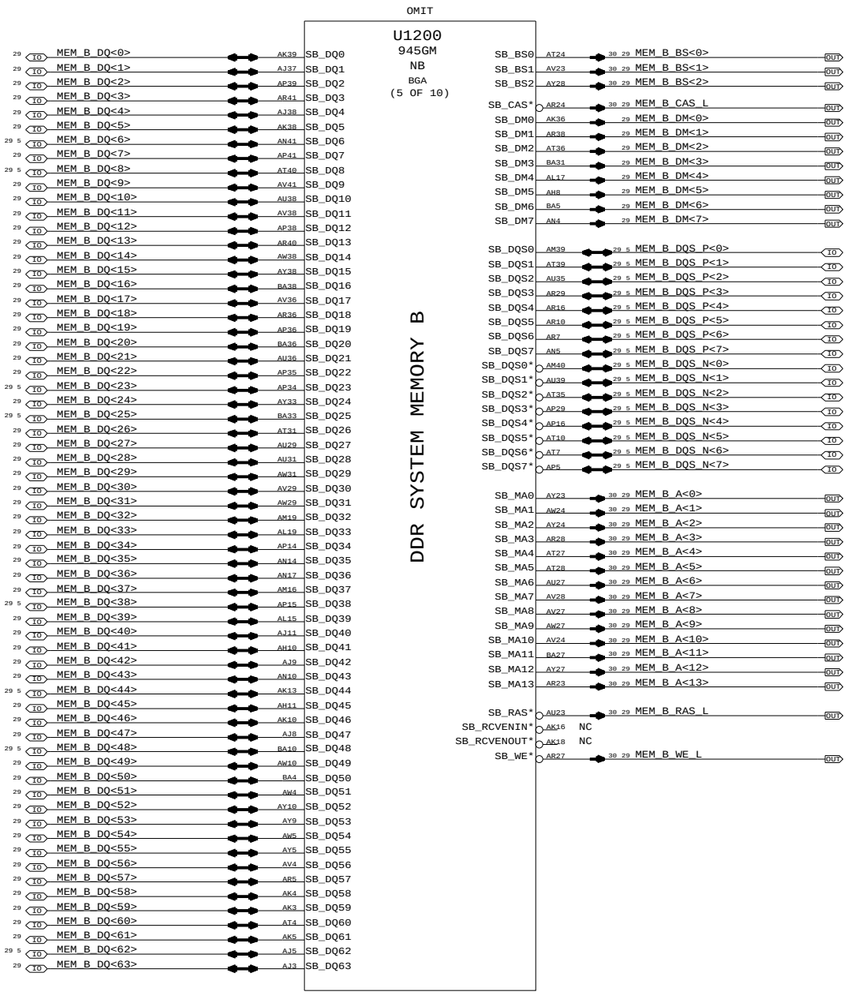
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 14 OF 111	





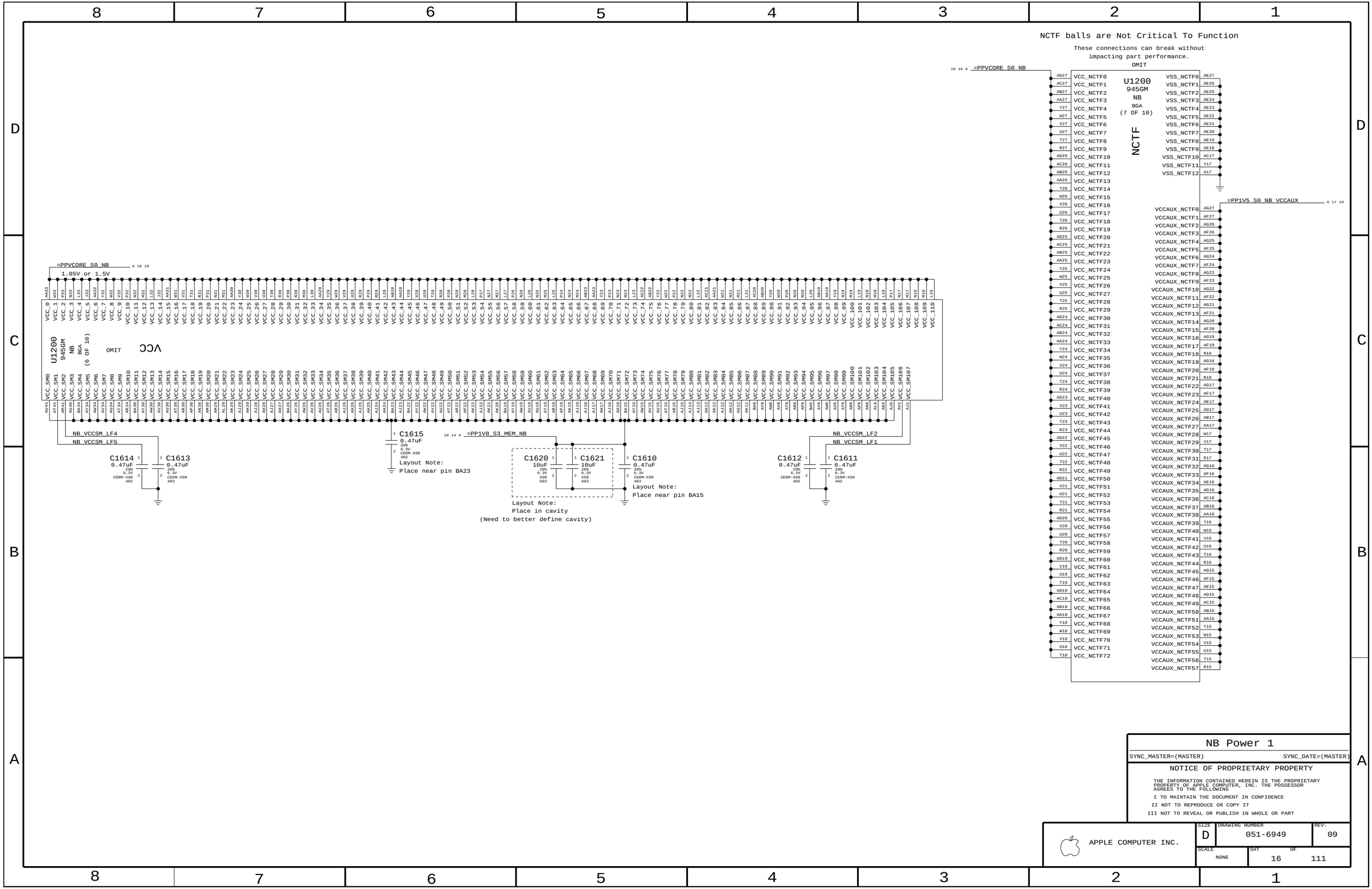
NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	15	111



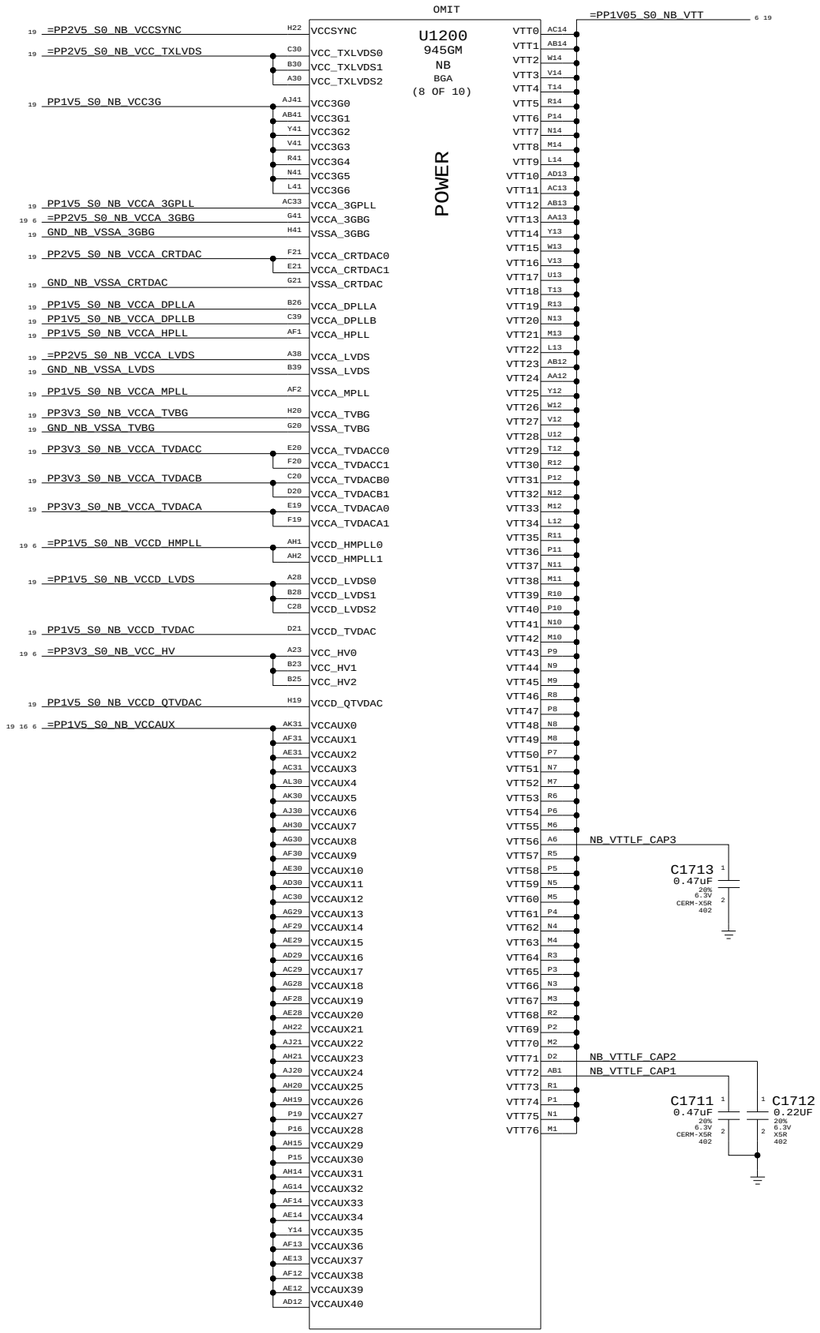
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	16	111



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	17	111

OMIT

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	18	111

Power Interface

These are the power signals that leave the NB "block"

IN =PP1V05_S0_FSB_NB — 5 6 12
IN =PPVCORE_S0_NB — 6 16 19
IN =PP1V05_S0_NB — 6
IN =PP1V05_S0_NB_VTT — 6 17 19
IN =PP1V5_S0_NB — 6 19
IN =PP1V5_S0_NB_PCIE — 6 13
IN =PP1V5_S0_NB_PLL — 6 19
IN =PP1V5_S0_NB_TVDAC — 6 19
IN =PP1V5_S0_NB_VCCD_HMPLL — 6 17
IN =PP1V5_S0_NB_VCCD_LVDS — 17 19
IN =PP1V5_S0_NB_VCCAUX — 6 16 17 19
IN =PP1V8_S3_MEM_NB — 6 14 16 19

IN =PP2V5_S0_NB_VCCSYNC — 17 19
IN =PP2V5_S0_NB_VCC_TXLVDS — 17 19
IN =PP2V5_S0_NB_VCCA_3GBG — 6 17 19
IN =PP2V5_S0_NB_VCCA_LVDS — 17 19
IN =PP3V3_S0_NB — 6 14 20
IN =PP3V3_S0_NB_TVDAC — 6
IN =PP3V3_S0_NB_VCC_HV — 6 17 19

19 6 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402

Layout Note:
These 4 0.1uF caps should
be within 5 mm of NB edge

L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402

19 17 6 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 10% 6.3V CERM1 603
Layout Note: Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
C1968 330UF 20% 6.3V ELEC CASE-C1
Layout Note: Place on the edge

19 16 14 6 =PP1V8_S3_MEM_NB
R1982 1K 5% 1/16W MF-LF 402
MEM_VREF_NB_1 — 5 14
R1983 1K 5% 1/16W MF-LF 402
C1982 0.1uF 20% 16V CERM 603
R1980 1K 5% 1/16W MF-LF 402
MEM_VREF_NB_0 — 5 14
R1981 1K 5% 1/16W MF-LF 402
C1981 0.1uF 20% 16V CERM 603

19 17 6 =PP3V3_S0_NB_VCC_HV
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

19 17 6 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

19 17 16 6 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

TVOUT DISABLE

16 6 19 =PPVCORE_S0_NB
PP2V5_S0_NB_VCCA_CRTDAC — 17
CRT_RED — 13
CRT_RED_L — 13
CRT_GREEN — 13
CRT_GREEN_L — 13
CRT_BLUE — 13
CRT_BLUE_L — 13
CRT_IREF — 13

CRT_VSYNC_R — 13
CRT_HSYNC_R — 13
=PP2V5_S0_NB_VCCSYNC — 17 19
GND_NB_VSSA_CRTDAC — 17

TP_CRT_DDC_CLK TRUE — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA TRUE — CRT_DDC_DATA — 13

DISPLAY DISABLE

TP_NB_VCCA_DPLLA TRUE — PP1V5_S0_NB_VCCA_DPLLA — 17
TP_NB_VCCA_DPLLB TRUE — PP1V5_S0_NB_VCCA_DPLLB — 17

NB_CLK_DREFCLKIN_N (IN) — 14
NB_CLK_DREFCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_N (OUT) — 14

19 16 6 =PPVCORE_S0_NB
C1900 330UF 20% 6.3V ELEC CASE-C1
C1901 330UF 20% 6.3V ELEC CASE-C1
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

19 16 6 =PP1V8_S3_MEM_NB

19 6 =PP1V5_S0_NB_3GPLL
L1970 91NH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY SMB2
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
PP1V5_S0_NB_VCC3G — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
Layout Note: 10uF caps should be close to MCH on opposite side.

1uH, 20%
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
Should be 1%
R1975 0.51 1% 1/16W MF-LF 402
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCA_3GPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
GND_NB_VSSA_3GBG — 17
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

LVDS DISABLE

13 LVDS_A_CLK_N TRUE TP_LVDS_A_CLK_N
13 LVDS_A_CLK_P TRUE TP_LVDS_A_CLK_P
13 LVDS_B_CLK_N TRUE TP_LVDS_B_CLK_N
13 LVDS_B_CLK_P TRUE TP_LVDS_B_CLK_P

13 LVDS_A_DATA_N<0> TRUE TP_LVDS_A_DATA_N<0>
13 LVDS_A_DATA_N<1> TRUE TP_LVDS_A_DATA_N<1>
13 LVDS_A_DATA_N<2> TRUE TP_LVDS_A_DATA_N<2>

13 LVDS_A_DATA_P<0> TRUE TP_LVDS_A_DATA_P<0>
13 LVDS_A_DATA_P<1> TRUE TP_LVDS_A_DATA_P<1>
13 LVDS_A_DATA_P<2> TRUE TP_LVDS_A_DATA_P<2>

13 LVDS_B_DATA_N<0> TRUE TP_LVDS_B_DATA_N<0>
13 LVDS_B_DATA_N<1> TRUE TP_LVDS_B_DATA_N<1>
13 LVDS_B_DATA_N<2> TRUE TP_LVDS_B_DATA_N<2>

13 LVDS_B_DATA_P<0> TRUE TP_LVDS_B_DATA_P<0>
13 LVDS_B_DATA_P<1> TRUE TP_LVDS_B_DATA_P<1>
13 LVDS_B_DATA_P<2> TRUE TP_LVDS_B_DATA_P<2>

13 LVDS_BKLTEN TRUE TP_LVDS_BKLTEN
13 LVDS_VDDEN TRUE TP_LVDS_VDDEN
13 LVDS_IBG TRUE TP_LVDS_IBG
17 GND_NB_VSSA_LVDS TRUE TP_GND_NB_VSSA_LVDS

13 LVDS_VREFH TRUE TP_LVDS_VREFH
13 LVDS_VREFL TRUE TP_LVDS_VREFL

19 17 =PP2V5_S0_NB_VCCA_LVDS
19 17 =PP1V5_S0_NB_VCCD_LVDS
19 17 =PP2V5_S0_NB_VCC_TXLVDS

13 LVDS_BKLTCTL TRUE TP_LVDS_BKLTCTL
13 LVDS_CLKCTLA TRUE TP_LVDS_CLKCTLA
13 LVDS_CLKCTLB TRUE TP_LVDS_CLKCTLB
13 LVDS_DDC_CLK TRUE TP_LVDS_DDC_CLK
13 LVDS_DDC_DATA TRUE TP_LVDS_DDC_DATA

TVOUT DISABLE

19 6 =PP1V5_S0_NB
PP3V3_S0_NB_VCCA_TVDACA — 17
PP3V3_S0_NB_VCCA_TVDACB — 17
PP3V3_S0_NB_VCCA_TVDACC — 17
PP3V3_S0_NB_VCCA_TVBG — 17
TV_DACA_OUT — 13
TV_DACB_OUT — 13
TV_DACC_OUT — 13
TV_IREF — 13
TV_IRTNA — 13
TV_IRTNB — 13
TV_IRTNC — 13

GND_NB_VSSA_TVBG — 17

CRITICAL
C1921 22000pF-1000mA 16V NFM10
6 19 =PP1V5_S0_NB_TVDAC
PP1V5_S0_NB_VCCD_TVDAC — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1920 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCD_QTVDAC — 17
Layout Note: THESE 2 CAPS SHOULD BE within 6.35 mm of NB edge

14 SDVO_CTRLCLK (IN) — TP_SDVO_CTRLCLK
14 SDVO_CTRLDATA (IN) — TP_SDVO_CTRLDATA

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

14 NB_CFG<5>
Internal pull-up
NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

14 NB_CFG<7>
Internal pull-up
NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

14 NB_CFG<9>
Internal pull-up
NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

14 NB_CFG<16>
Internal pull-up
NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

=PP3V3_S0_NB 6 14 19 20
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

14 NB_CFG<18>
Internal pull-down

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

=PP3V3_S0_NB 6 14 19 20
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

=PP3V3_S0_NB 6 14 19 20
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6949	09

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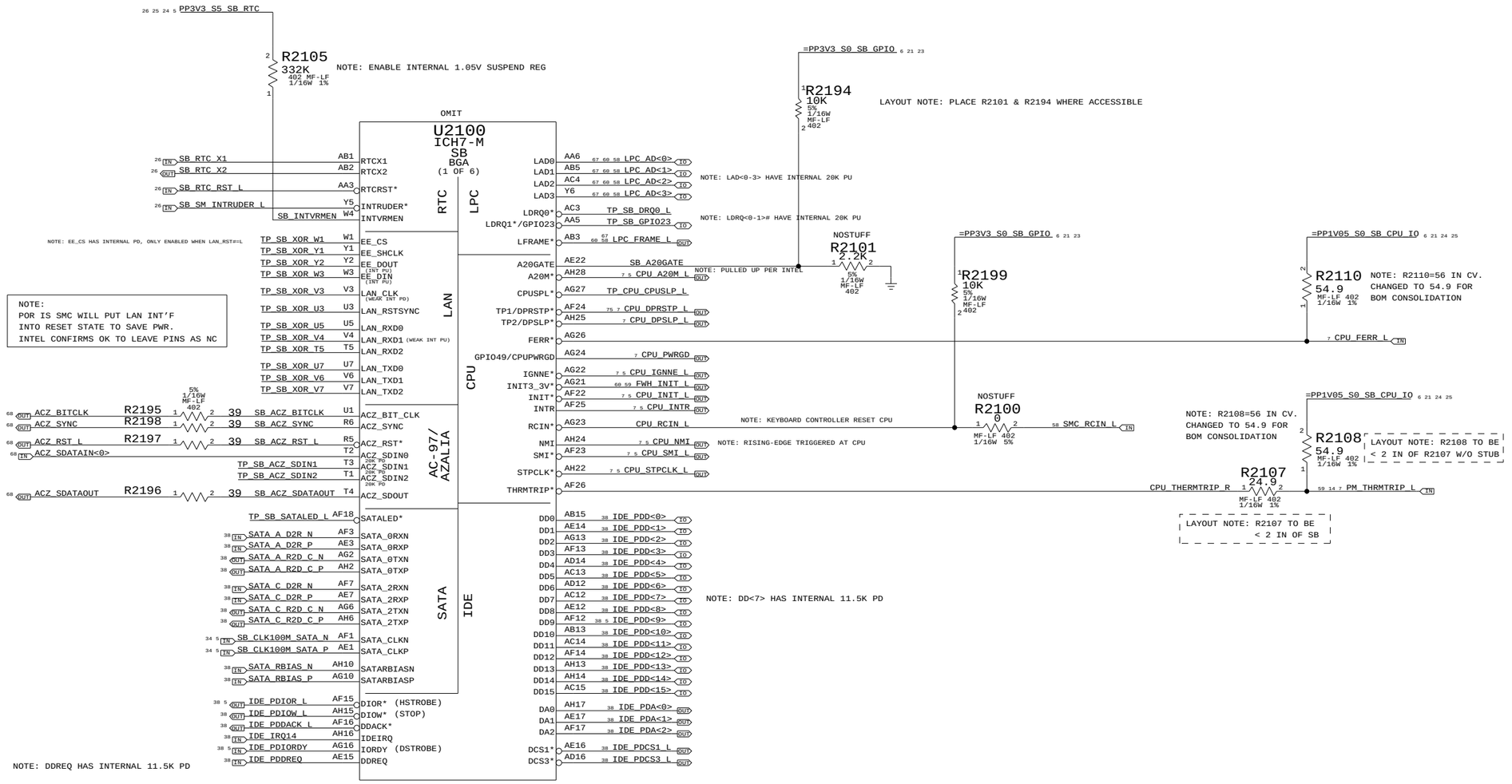
NONE	20	111



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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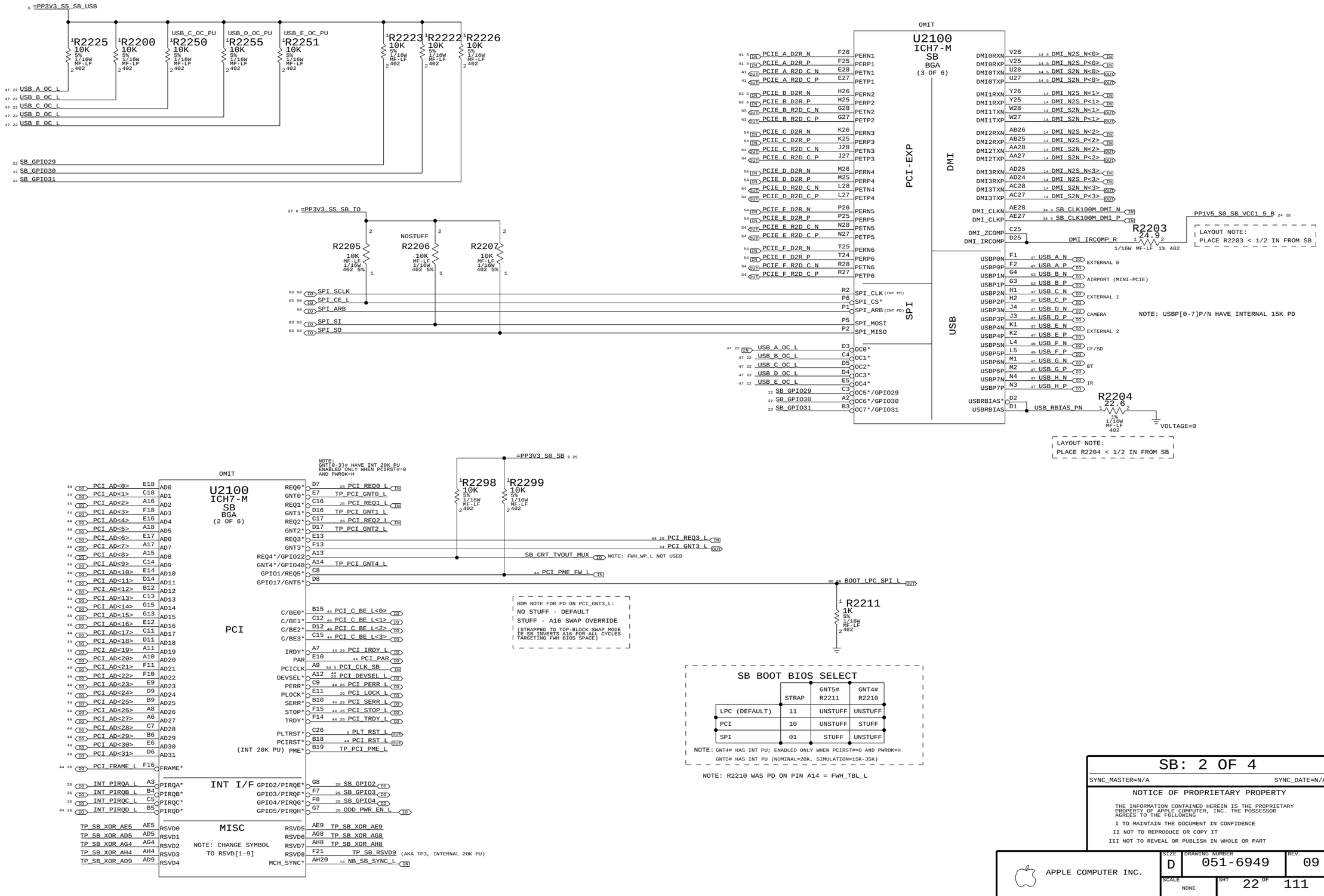

SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE: NONE SHT 22 OF 111

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 6 21 23

=PP3V3_S5_SB 6 23 25 26

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

26 25 23 6 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

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27 IO SMB_CLK — C22 SMBCLK
27 IO SMB_DATA — B22 SMBDATA
SMB_LINK_ALERT_L — A26 LINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
SMB

PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
67 60 58 OUT PM_SUS_STAT_L — A27 SUS_STAT*
58 26 5 IN PM_SYSRST_L — A22 SYS_RST*

34 IN PM_BMBUSY_L — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

33 OUT PM_STPPCI_L — AC20 GPIO18/STPPCI*
33 OUT PM_STPCPU_L — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
23 BIOS_REC — B21 GPIO27
23 FWH_MFG_MODE — E23 GPIO28
67 60 58 44 5 IO PM_CLKRUN_L — AG18 GPIO32/CLKRUN*

RESERVED FOR MOBILE AZALIA DOCKING INT'F
TP_AZ_DOCK_EN_L — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L — U2 GPIO34/AZ_DOCK_RST*

53 41 IN PCIE_WAKE_L — F20 WAKE*
67 60 58 IO INT_SERIRQ — AH21 SERIRQ
58 10 IN PM_THRM_L — AF20 THERM*
26 IN VR_PWRGD_CK410 — AD22 VRMPWRGD
IO TP_SB_GPIO6 — AC21 GPIO6
AC18 GPIO7
58 IN SMC_RUNTIME_SCI_L — E21 GPIO8
58 IN SMC_EXTSMI_L

SYS GPIO

SATA GPIO
GPIO21/SATA0GP — AF19 SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 — 100 — R2305
38 SATA_C_DET_L IN

CLKS
CLK14 — AC1 — 34 5 SB_CLK14P3M_TIMER IN
CLK48 — B2 — 34 5 SB_CLK48M_USBCTLR IN
SUSCLK — C20 — 59 SUS_CLK_SB OUT

PWR MNGT
SLP_S3* — B24 — 79 77 88 86 PM_SLP_S3_L OUT
SLP_S4* — D23 — 77 58 PM_SLP_S4_L OUT
SLP_S5* — F22 — 58 PM_SLP_S5_L OUT
PWROK — AA4 — 26 PM_SB_PWROK IN
GPIO16/DPRSLPVR — AC22 — 75 14 PM_DPRSLPVR OUT
TP0/BATLOW* — C21 — NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* — C23 — 58 PM_PWRBTN_L IN
LAN_RST* — C19 — 58 PM_LAN_ENABLE IN — NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO
GPIO9 — E20 — 58 26 SMS_INT_L IN
GPIO10 — A20 — 58 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 38 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 23 60
GPIO24 — R3 — CRB_SV_DET 23
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 33 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 IO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

=PP3V3_S5_SB_PM 6 11

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

58 PM_BATLOW_L IN
58 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
58 SMC_WAKE_SCI_L IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

26 25 23 6 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 23 60
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

26 25 23 6 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

=PP3V3_S5_SB 6 23 25 26

R2390 10K 5% 1/16W 402 MF-LF
23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 6 21 23

R2388 10K 5% 1/16W MF-LF 402
23 SATA_C_PWR_EN_L

SB: 3 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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VSS

A4	AD3
A23	AD4
N24	AD7
P24	AD8
R18	AD15
U14	AD19
V27	AD23
AA24	AE2
AB27	AE4
AD11	AE8
B1	AE11
D10	AE13
F4	AE18
G18	AE21
J1	B8
L24	B11
M17	B14
N14	B17
N17	B20
N18	B26
N25	B28
N26	C2
P3	C6
P4	C27
P12	D13
P13	D18
P14	D21
P15	D24
P16	E1
P17	E2
P27	E4
P28	E8
R1	E15
R11	F3
R12	F5
R13	F12
R14	F27
R15	F28
R16	G1
R17	G2
T6	G5
T12	G6
T13	G9
T14	G14
T15	G21
T16	G24
T17	G25
U4	G26
U12	H3
U13	H4
U15	H5
U16	H24
U17	H27
U24	H28
U25	J2
U26	J5
V2	J24
V13	J25
V15	J26
V24	K24
V28	K27
W6	K28
W24	L13
W25	L15
W26	L25
Y3	L26
Y24	M3
Y27	M4
Y28	M5
AA1	M12
AA25	M13
AA26	M14
AB4	M15
AB6	M16
AB11	M24
AB14	M27
AB16	M28
AB19	N1
AB21	N2
AB24	N5
AB28	N6
AC2	N11
AC5	N12
AC9	N13
AC11	N15
AD1	N16
AE24	AG11
AE25	AG14
AF2	AG17
AF4	AG20
AF8	AG25
AF11	AH1
AF27	AH3
AF28	AH7
AG1	AH12
AG3	AH23
AG7	AH27

0 0

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25 PP5V_S0_SB_V5REF — G10, AD17 — V5REF
25 PP5V_S5_SB_V5REF_SUS — F6 — V5REF_SUS
25 22 PP1V5_S0_SB_VCC1_5_B — AA22

VCCA3GP (VCC1_5_B): AA23, AB22, AB23, AC23, AC24, AC25, AC26, AD26, AD27, AD28, D26, D27, D28, E24, E25, E26, F23, F24, G22, G23, H22, H23, J22, J23, K22, K23, L22, L23, M22, M23, N22, N23, P22, P23, R22, R23, R24, R25, R26, T22, T23, T26, T27, T28, U22, U23, V22, V23, W22, W23, Y22, Y23

25 24 6 =PP3V3_S0_SB_VCC3_3 — B27 — VCC3_3
25 PP1V5_S0_SB_VCCDMIPLL — AG28 — VCCDMIPLL
25 6 =PP1V5_S0_SB_VCC1_5_A_ARX — AB7

ARX (VCC1_5_A): AC6, AC7, AD6, AE6, AF5, AF6, AG5, AH5

25 6 =PP1V5_S0_SB_VCCSATAPLL — AD2 — VCCSATAPLL
25 24 6 =PP3V3_S0_SB_VCC3_3 — AH11 — VCC3_3
25 6 =PP1V5_S0_SB_VCC1_5_A_ATX — AB10

ATX (VCC1_5_A): AB9, AC10, AD10, AE10, AF10, AF9, AG9, AH9

25 24 6 =PP3V3_S5_SB_VCCSUS3_3 — E3 — VCCSUS3_3
25 6 =PP1V5_S0_SB_VCCUSBPLL — C1 — VCCUSBPLL

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

AA2, Y7 — VCCLAN1_5 (CHANGE SYMBOL TO 1.05)

CORE (VCC1_05): L11, L12, L14, L16, L17, L18, M11, M18, P11, P18, T11, T18, U11, U18, V11, V12, V14, V16, V17, V18 — =PPVCORE_S0_SB 6 25

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

VCC_PAUX (VCCLAN_3_3): V5, V1, W2, W7 — =PP3V3_S0_SB_VCCLAN3_3 6 25

VCC3_3/VCCHDA: U6 — =PP3V3_S0_SB_3V3_1V5_VCCHDA 6 25
VCCSUS3_3/VCCSUSHDA: R7 — =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 6

V_CPU_IO: AE23, AE26, AH26 — =PP1V05_S0_SB_CPU_IO 6 21 25

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

IDE (VCC3_3): AA7, AB12, AB20, AC16, AD13, AD18, AG12, AG15, AG19 — =PP3V3_S0_SB_VCC3_3_IDE 6 25

PCI (VCC3_3): A5, B13, B16, B7, C10, D15, F9, G11, G12, G16 — =PP3V3_S0_SB_VCC3_3_PCI 6 25

VCCRTC: W5 — PP3V3_S5_SB_RTC 5 21 25 26

P7 — =PP3V3_S5_SB_VCCSUS3_3 6 24 25

VCCSUS3_3: A24, C24, D19, D22, G19

USB (VCCSUS3_3): K3, K4, K5, K6, L1, L2, L3, L6, L7, M6, M7, N7 — =PP3V3_S5_SB_VCCSUS3_3_USB 6 25

VCC1_5_A: AB17, AC17, T7, F17, G17, AB8, AC8 — =PP1V5_S0_SB_VCC1_5_A 6 25

VCCSAUS1_5 (CHANGE SYMBOL TO 1.05): K7, C28, G20

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

USB CORE (VCC1_5_A): A1, H6, H7, J6, J7 — =PP1V5_S0_SB_VCC1_5_A_USB_CORE 6 25

SB: 4 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-6949	09
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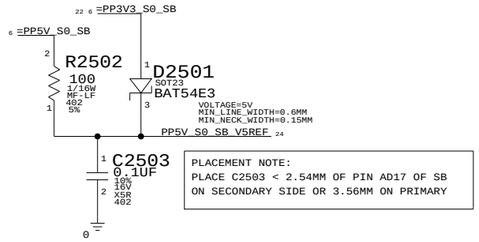
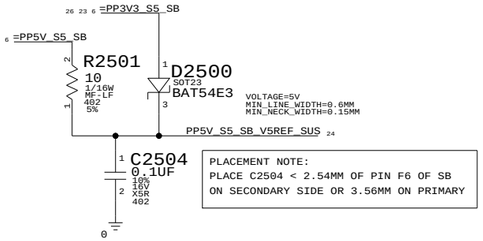
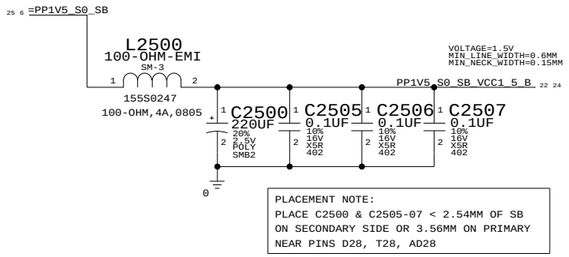
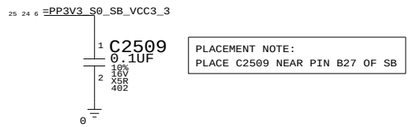
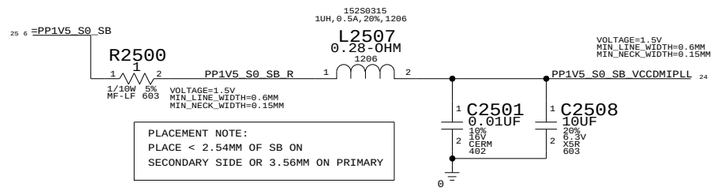
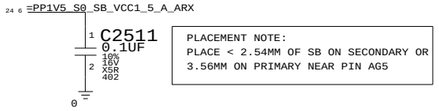


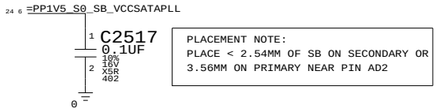


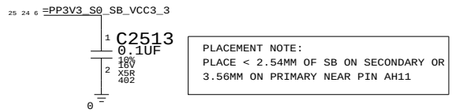


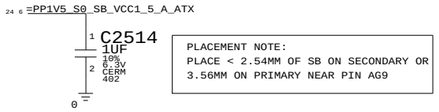


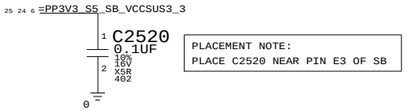


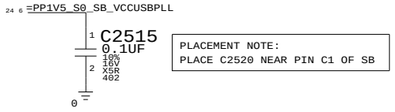


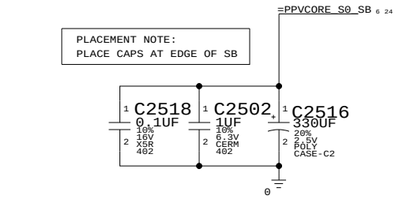


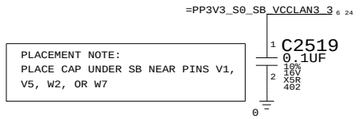


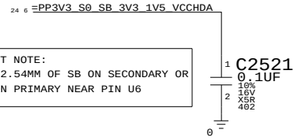


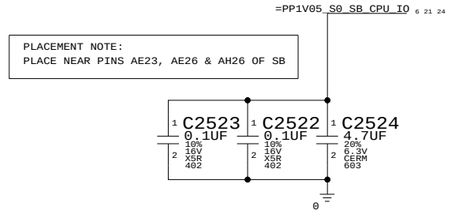


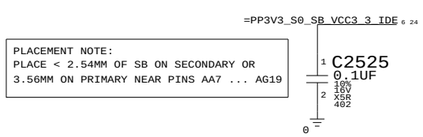


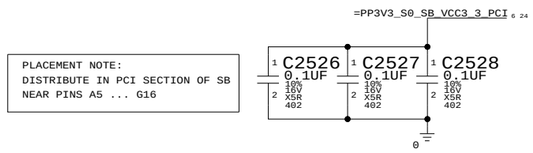


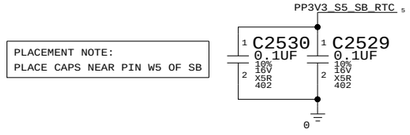


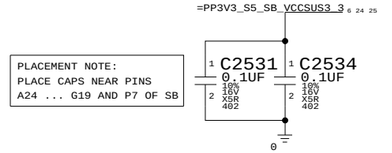


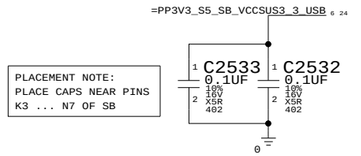


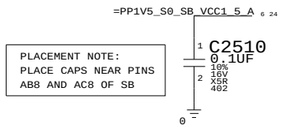


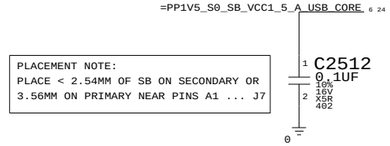












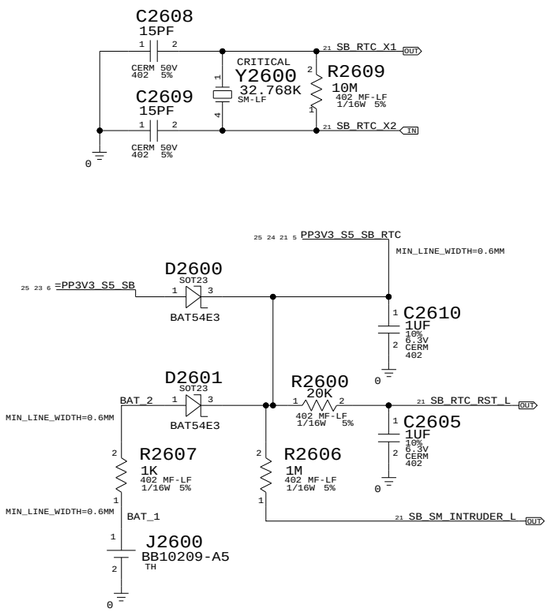
SB:DECOUPLING

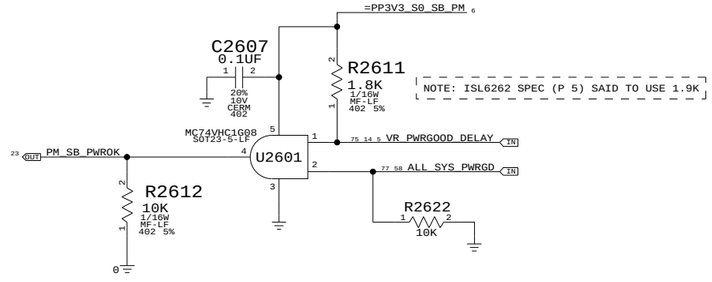
SYNC_MASTER=N/A SYNC_DATE=N/A

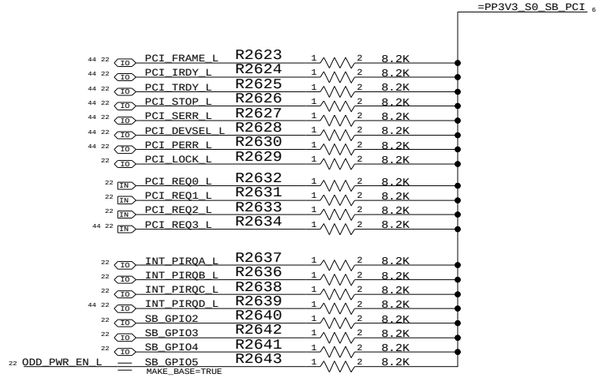
APPLE COMPUTER INC.

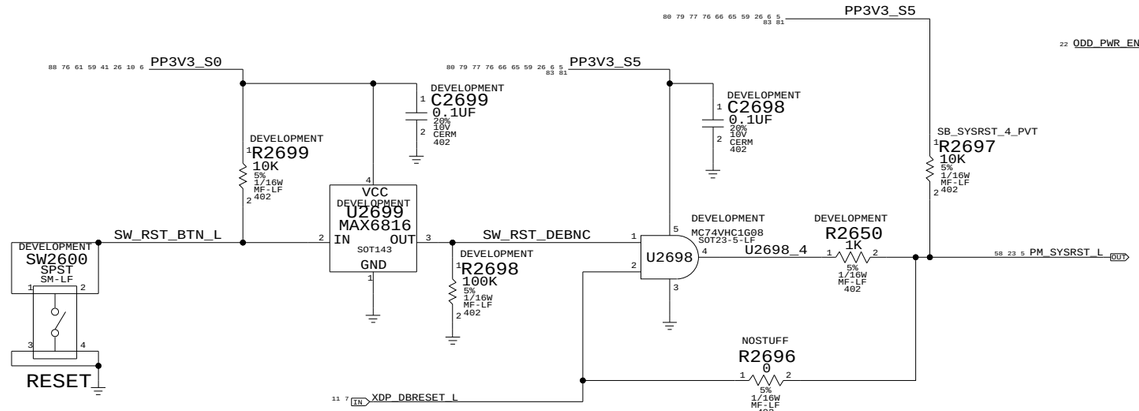
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

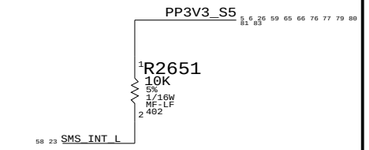
SCALE: NONE SHT 25 OF 111

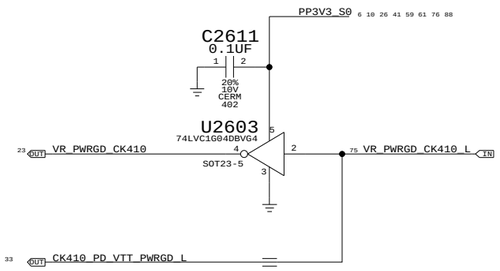












SB: MISC			
SYNC_MASTER=N/A	SYNC_DATE=N/A		

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
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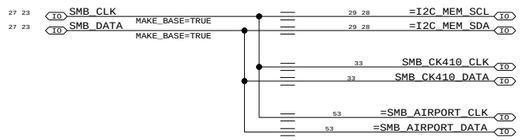
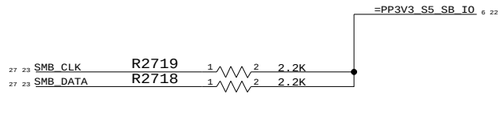
SB I2C BUSSES





SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	27 OF 111

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

29 28 6 5 =PP1V8_S3_MEM

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF 5 28 29
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

29 28 5 MEM_VREF

C2850 2.2UF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

29 28 6 5 =PP1V8_S3_MEM

J2800 — DDR2-SODIMM-STD

CRITICAL
F-RT-SM1

	1	VREF	VSS0	2	
	3	VSS1	DQ4	4	MEM_A_DQ<4> 15
15	5	MEM_A_DQ<0>	DQ5	6	MEM_A_DQ<5> 15
15	7	MEM_A_DQ<1>	VSS2	8	
	9	VSS4	DM0	10	MEM_A_DM<0> 15
15 5	11	MEM_A_DQS_N<0>	VSS5	12	
15 5	13	MEM_A_DQS_P<0>	DQ6	14	MEM_A_DQ<6> 15
	15	VSS6	DQ7	16	MEM_A_DQ<7> 5 15
15	17	MEM_A_DQ<2>	VSS7	18	
15	19	MEM_A_DQ<3>	DQ12	20	MEM_A_DQ<12> 15
	21	VSS8	DQ13	22	MEM_A_DQ<13> 15
15	23	MEM_A_DQ<8>	VSS9	24	
15	25	MEM_A_DQ<9>	DM1	26	MEM_A_DM<1> 15
	27	VSS10	VSS11	28	
15 5	29	MEM_A_DQS_N<1>	CK0	30	MEM_CLK_P<0> 14
15 5	31	MEM_A_DQS_P<1>	CK0*	32	MEM_CLK_N<0> 14
	33	VSS12	VSS13	34	
15	35	MEM_A_DQ<10>	DQ14	36	MEM_A_DQ<14> 5 15
15	37	MEM_A_DQ<11>	DQ15	38	MEM_A_DQ<15> 15
	39	VSS14	VSS15	40	
		KEY			
	41	VSS16	VSS17	42	
15 5	43	MEM_A_DQ<16>	DQ20	44	MEM_A_DQ<20> 15
15	45	MEM_A_DQ<17>	DQ21	46	MEM_A_DQ<21> 15
	47	VSS18	VSS19	48	
15 5	49	MEM_A_DQS_N<2>	NC0	50	DIMM_OVERTEMP_L 29 59
15 5	51	MEM_A_DQS_P<2>	DM2	52	MEM_A_DM<2> 15
	53	VSS21	VSS22	54	
15	55	MEM_A_DQ<18>	DQ22	56	MEM_A_DQ<22> 15
15	57	MEM_A_DQ<19>	DQ23	58	MEM_A_DQ<23> 15
	59	VSS23	VSS24	60	
15	61	MEM_A_DQ<24>	DQ28	62	MEM_A_DQ<28> 15
15 5	63	MEM_A_DQ<25>	DQ29	64	MEM_A_DQ<29> 15
	65	VSS25	VSS26	66	
15	67	MEM_A_DM<3>	DQS3*	68	MEM_A_DQS_N<3> 5 15
NC	69	NC1	DQS3	70	MEM_A_DQS_P<3> 5 15
	71	VSS27	VSS28	72	
15	73	MEM_A_DQ<26>	DQ30	74	MEM_A_DQ<30> 15
15	75	MEM_A_DQ<27>	DQ31	76	MEM_A_DQ<31> 15
	77	VSS29	VSS30	78	
30 14	79	MEM_CKE<0>	NC/CKE1	80	MEM_CKE<1> 14 30
	81	VDD0	VDD1	82	
NC	83	NC2	NC/A15	84	TP_MEM_A_A<15>
30 15	85	MEM_A_BS<2>	NC/A14	86	TP_MEM_A_A<14>
	87	VDD2	VDD3	88	
30 15	89	MEM_A_A<12>	A11	90	MEM_A_A<11> 15 30
30 15	91	MEM_A_A<9>	A7	92	MEM_A_A<7> 15 30
30 15	93	MEM_A_A<8>	A6	94	MEM_A_A<6> 15 30
	95	VDD4	VDD5	96	
30 15	97	MEM_A_A<5>	A4	98	MEM_A_A<4> 15 30
30 15	99	MEM_A_A<3>	A2	100	MEM_A_A<2> 15 30
30 15	101	MEM_A_A<1>	A0	102	MEM_A_A<0> 15 30
	103	VDD6	VDD7	104	
30 15	105	MEM_A_A<10>	BA1	106	MEM_A_BS<1> 15 30
30 15	107	MEM_A_BS<0>	RAS*	108	MEM_A_RAS_L 15 30
30 15	109	MEM_A_WE_L	S0*	110	MEM_CS_L<0> 14 30
	111	VDD8	VDD9	112	
30 15	113	MEM_A_CAS_L	ODT0	114	MEM_ODT<0> 14 30
30 14	115	MEM_CS_L<1>	NC/A13	116	MEM_A_A<13> 15 30
	117	VDD10	VDD11	118	
30 14	119	MEM_ODT<1>	NC3	120	NC
	121	VSS31	VSS32	122	
15	123	MEM_A_DQ<32>	DQ36	124	MEM_A_DQ<36> 15
15	125	MEM_A_DQ<33>	DQ37	126	MEM_A_DQ<37> 15
	127	VSS33	VSS34	128	
15 5	129	MEM_A_DQS_N<4>	DM4	130	MEM_A_DM<4> 15
15 5	131	MEM_A_DQS_P<4>	VSS35	132	
	133	VSS36	DQ38	134	MEM_A_DQ<38> 15
15	135	MEM_A_DQ<34>	DQ39	136	MEM_A_DQ<39> 5 15
15	137	MEM_A_DQ<35>	VSS37	138	
	139	VSS38	DQ44	140	MEM_A_DQ<44> 15
15	141	MEM_A_DQ<40>	DQ45	142	MEM_A_DQ<45> 15
15	143	MEM_A_DQ<41>	VSS39	144	
	145	VSS40	DQS5*	146	MEM_A_DQS_N<5> 5 15
15	147	MEM_A_DM<5>	DQS5	148	MEM_A_DQS_P<5> 5 15
	149	VSS41	VSS42	150	
15	151	MEM_A_DQ<42>	DQ46	152	MEM_A_DQ<46> 15
15	153	MEM_A_DQ<43>	DQ47	154	MEM_A_DQ<47> 5 15
	155	VSS43	VSS44	156	
15	157	MEM_A_DQ<48>	DQ52	158	MEM_A_DQ<52> 15
15	159	MEM_A_DQ<49>	DQ53	160	MEM_A_DQ<53> 15
	161	VSS45	VSS46	162	
NC	163	NC_TEST	CK1	164	MEM_CLK_P<1> 14
	165	VSS47	CK1*	166	MEM_CLK_N<1> 14
15 5	167	MEM_A_DQS_N<6>	VSS48	168	
15 5	169	MEM_A_DQS_P<6>	DM6	170	MEM_A_DM<6> 15
	171	VSS49	VSS50	172	
15	173	MEM_A_DQ<50>	DQ54	174	MEM_A_DQ<54> 5 15
15	175	MEM_A_DQ<51>	DQ55	176	MEM_A_DQ<55> 15
	177	VSS51	VSS52	178	
15	179	MEM_A_DQ<56>	DQ60	180	MEM_A_DQ<60> 15
15	181	MEM_A_DQ<57>	DQ61	182	MEM_A_DQ<61> 15
	183	VSS53	VSS54	184	
15	185	MEM_A_DM<7>	DQS7*	186	MEM_A_DQS_N<7> 5 15
	187	VSS55	DQS7	188	MEM_A_DQS_P<7> 5 15
15	189	MEM_A_DQ<58>	VSS56	190	
15 5	191	MEM_A_DQ<59>	DQ62	192	MEM_A_DQ<62> 15
	193	VSS57	DQ63	194	MEM_A_DQ<63> 15
29 27	195	=I2C_MEM_SDA	VSS58	196	
29 27	197	=I2C_MEM_SCL	SA0	198	
	199	VDDSPD	SA1	200	ADDR=0xA0(WR)/0xA1(RD)
	201	GND			
	202	GND			
	203	GND			
	204	GND			
	205	GND			ALL NC'S

516S0403

=PP1V8_S3_MEM 5 6 28 29

DDR2 Bypass Caps

(For return current)

29 28 6 5 =PP1V8_S3_MEM

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

29 6 =PPSPD_S0_MEM

C2851 2.2UF 20% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 28 OF 111	

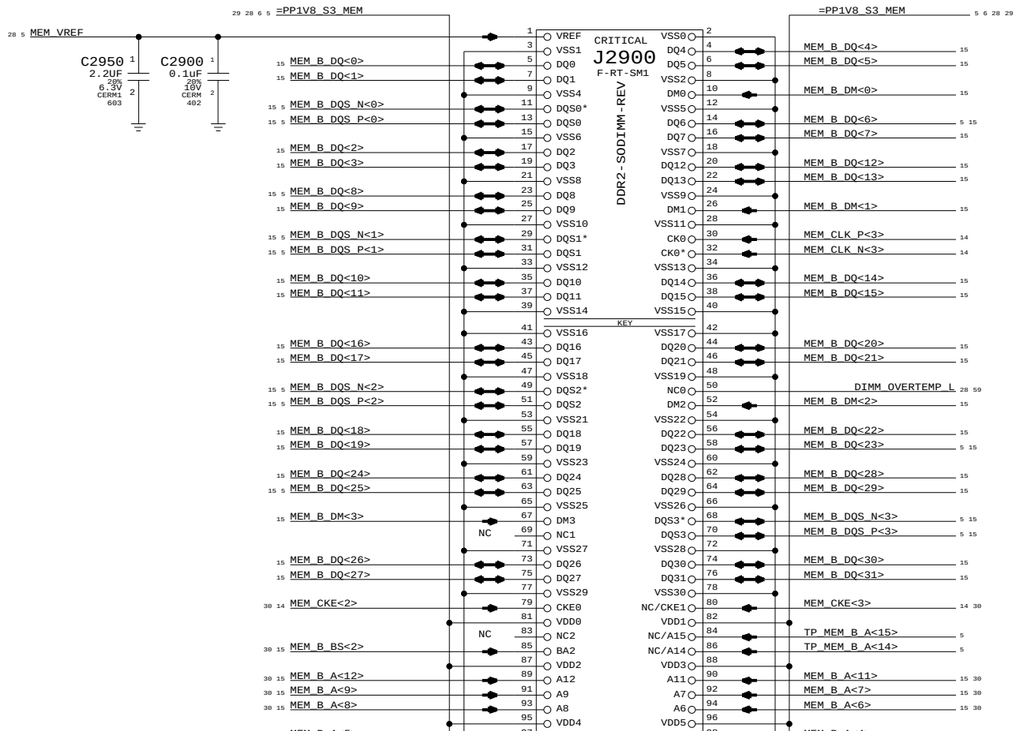
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

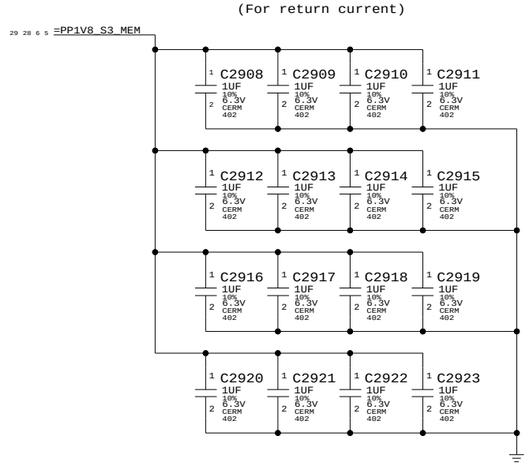
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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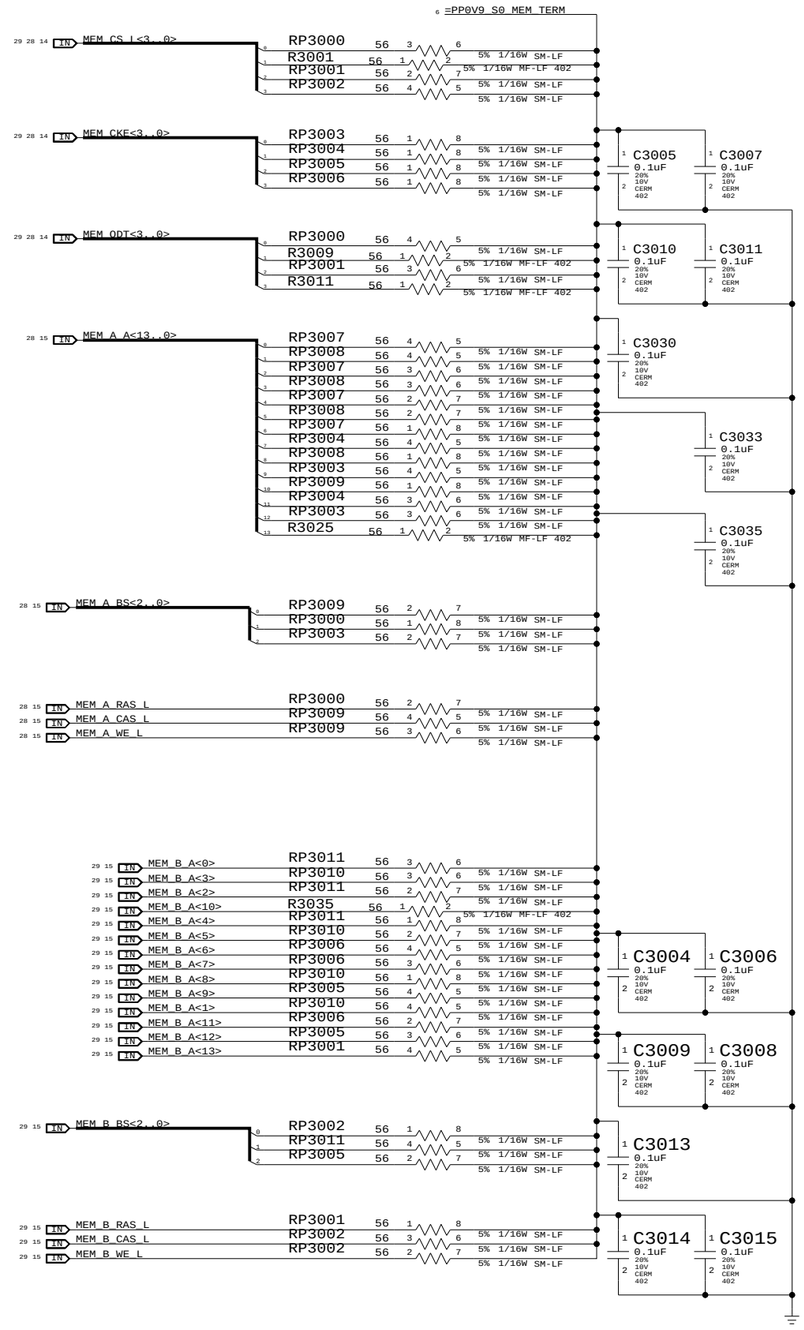
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	29	111

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	30	111

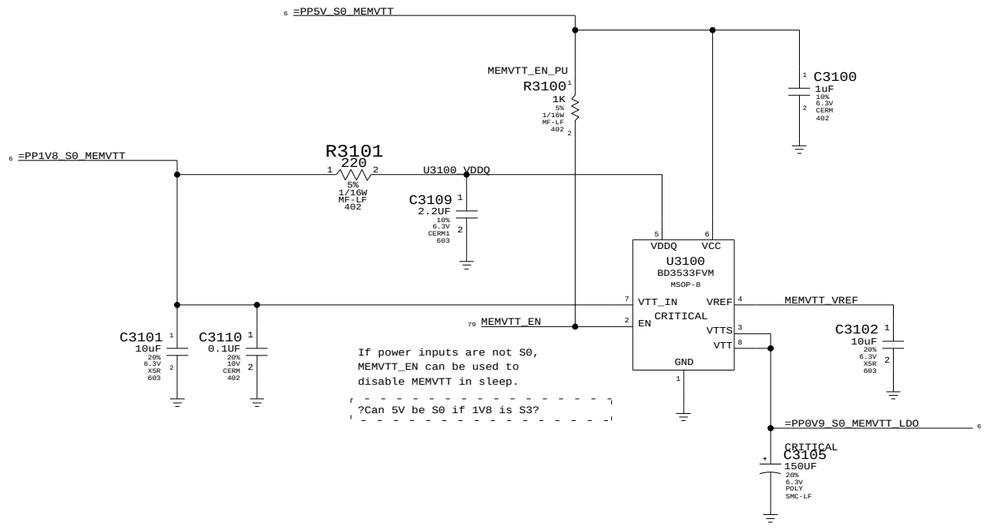
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



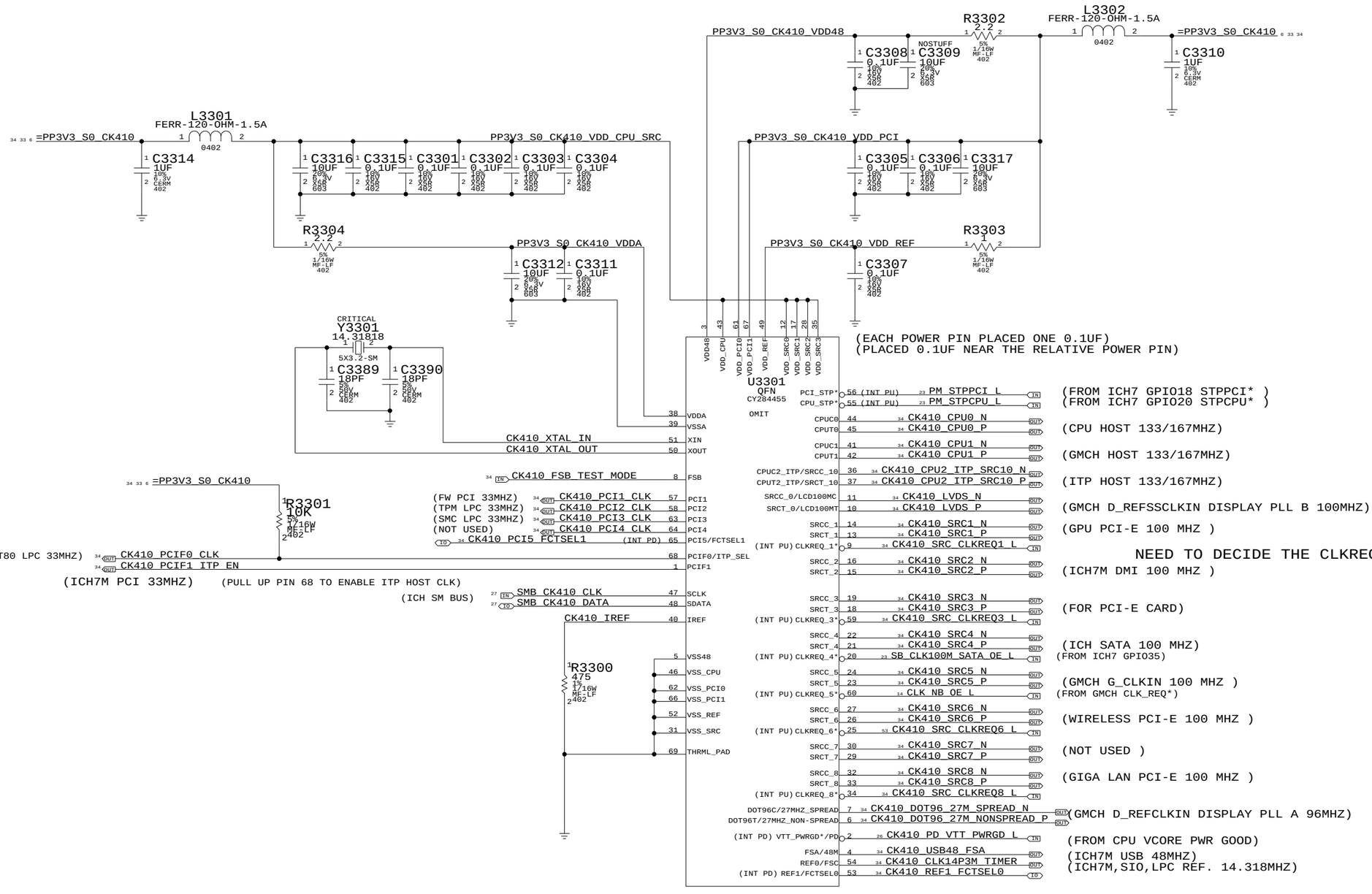
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	31	111



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

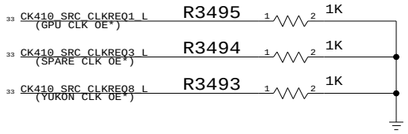
CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE COMPUTER INC.

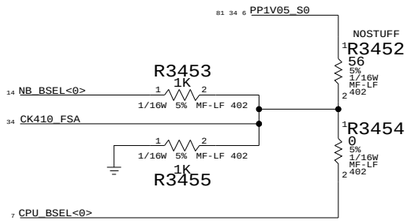
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 33 OF 111	

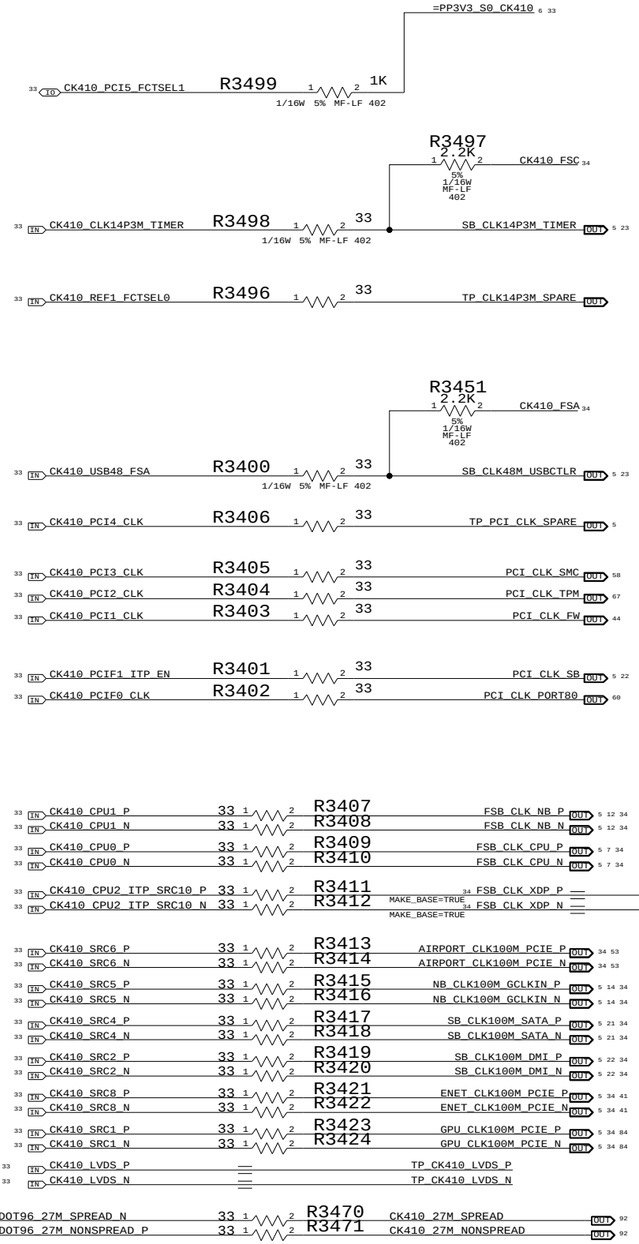
NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

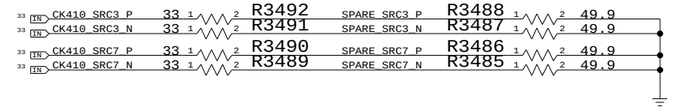


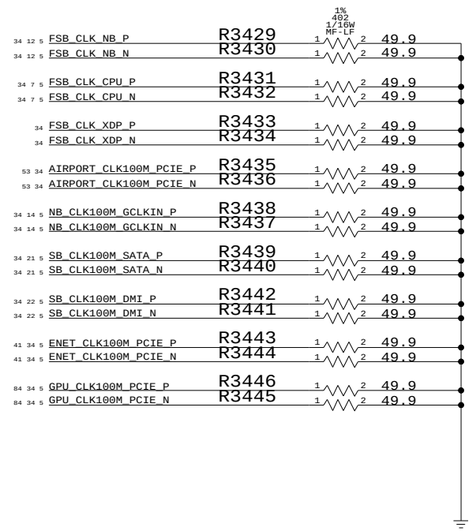
FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457









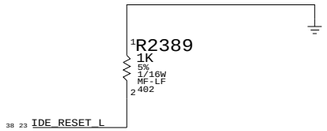
CLOCKS: TERMINATIONS

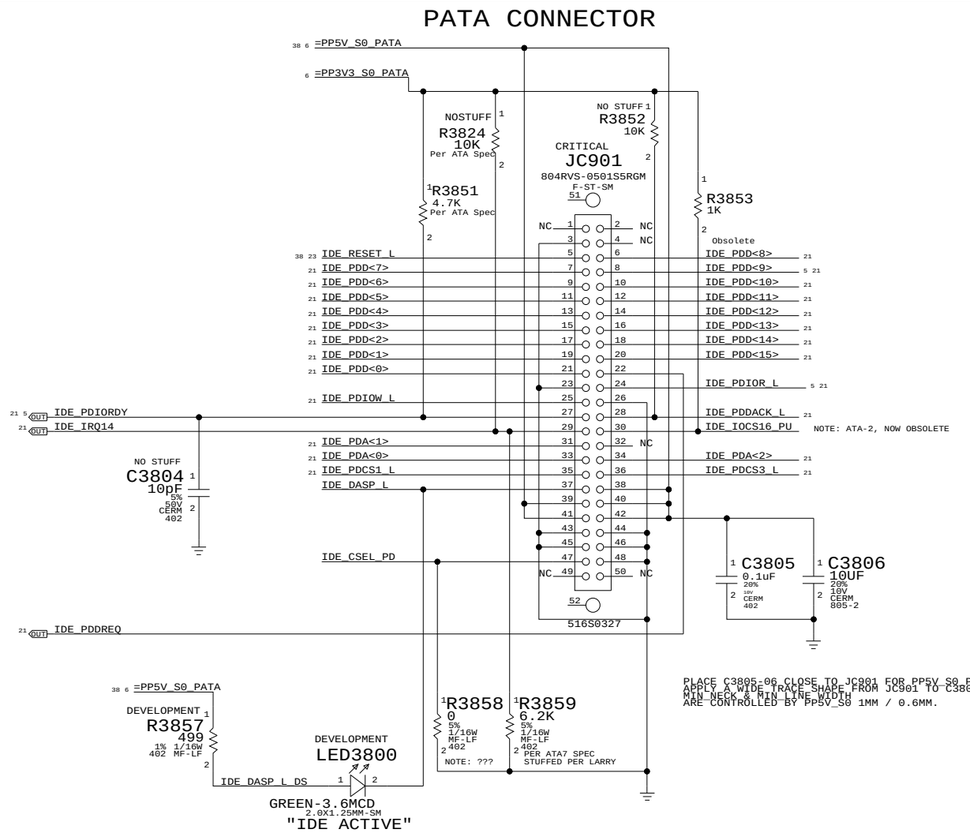
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

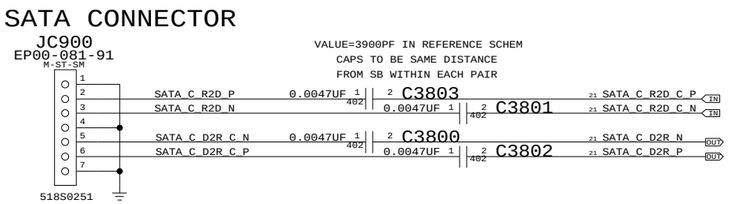
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 34 OF 111	

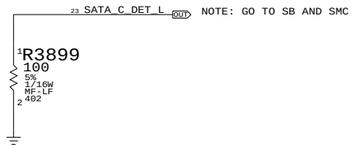
PATA CONNECTOR

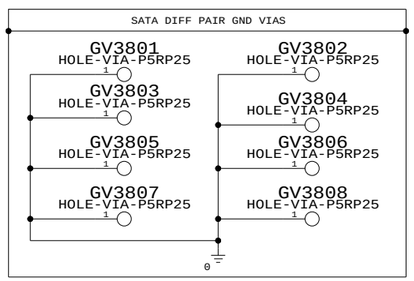


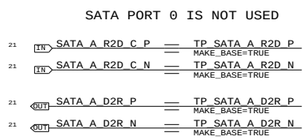


SATA CONNECTOR





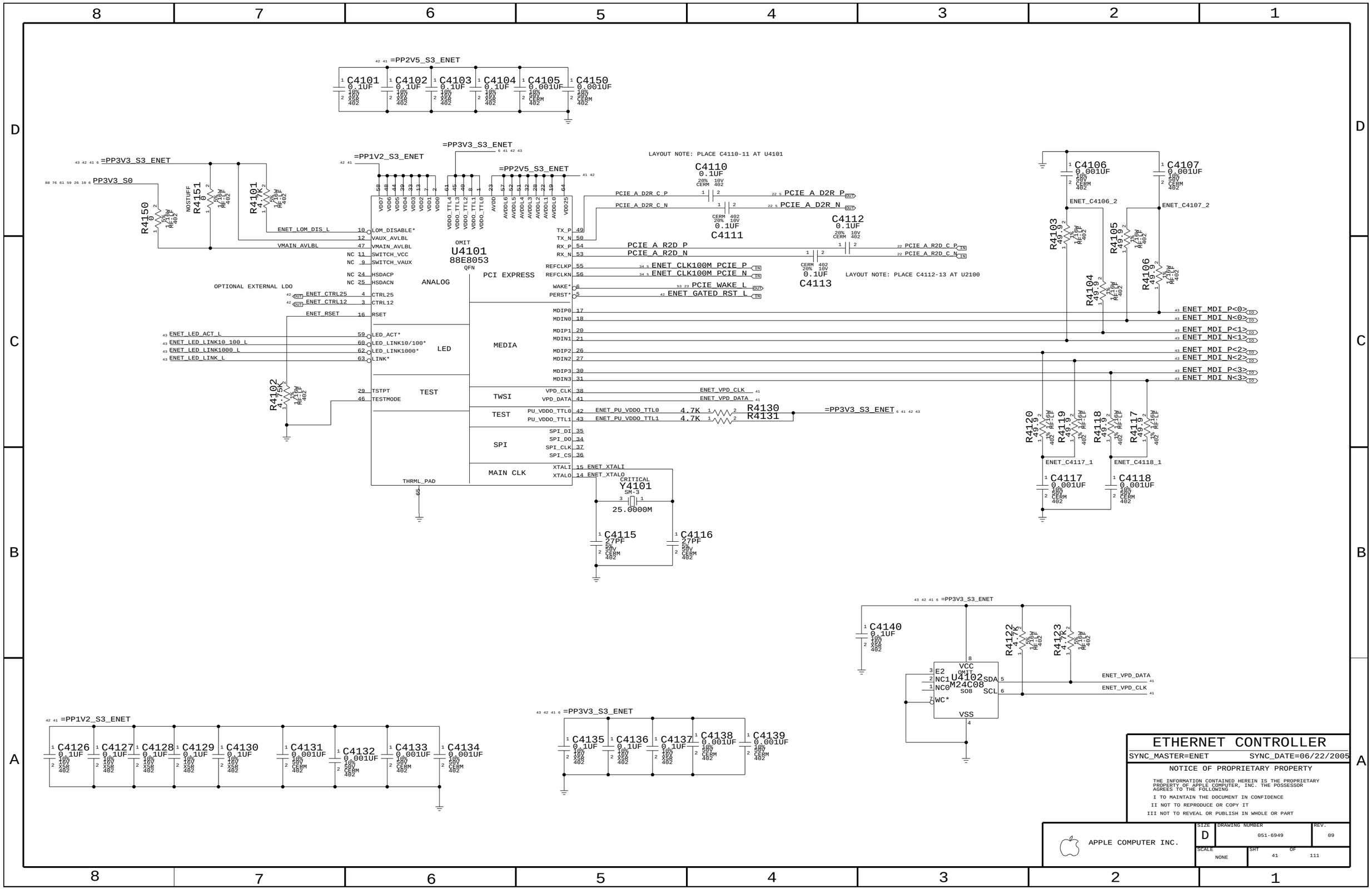




Disk Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 38 OF 111	



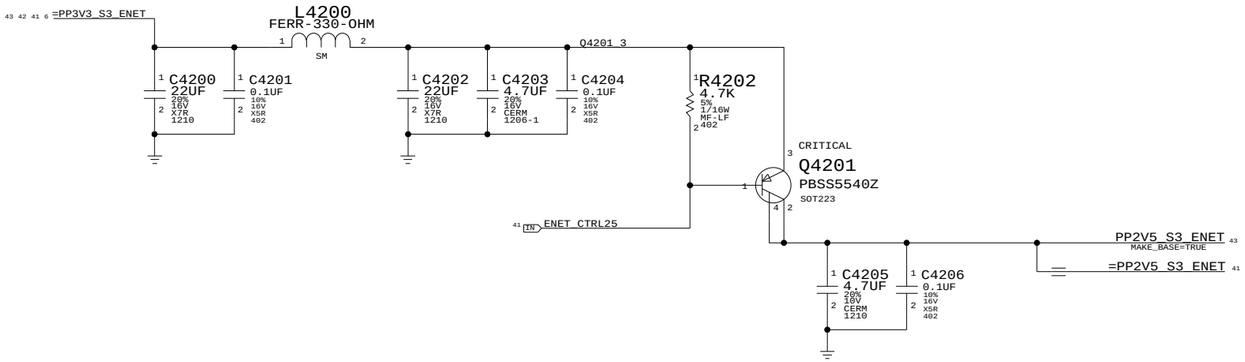
ETHERNET CONTROLLER

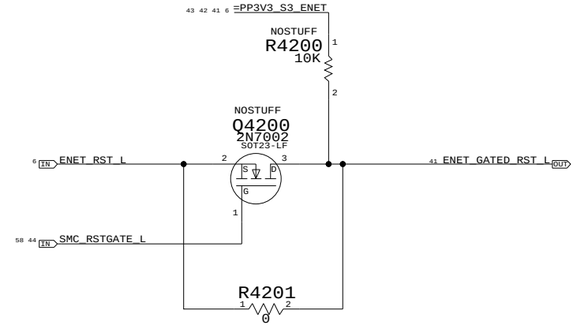
SYNC_MASTER=ENET SYNC_DATE=06/22/2005

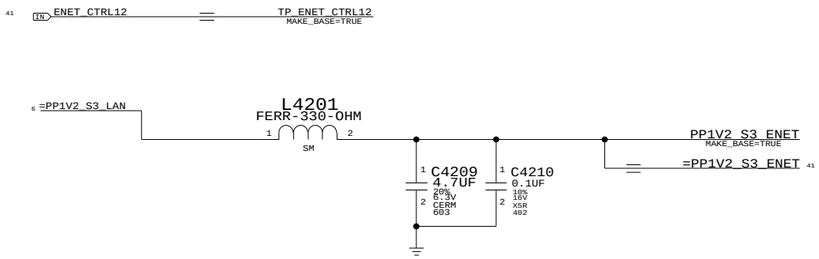
NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 41 OF 111	







ETHERNET MISC

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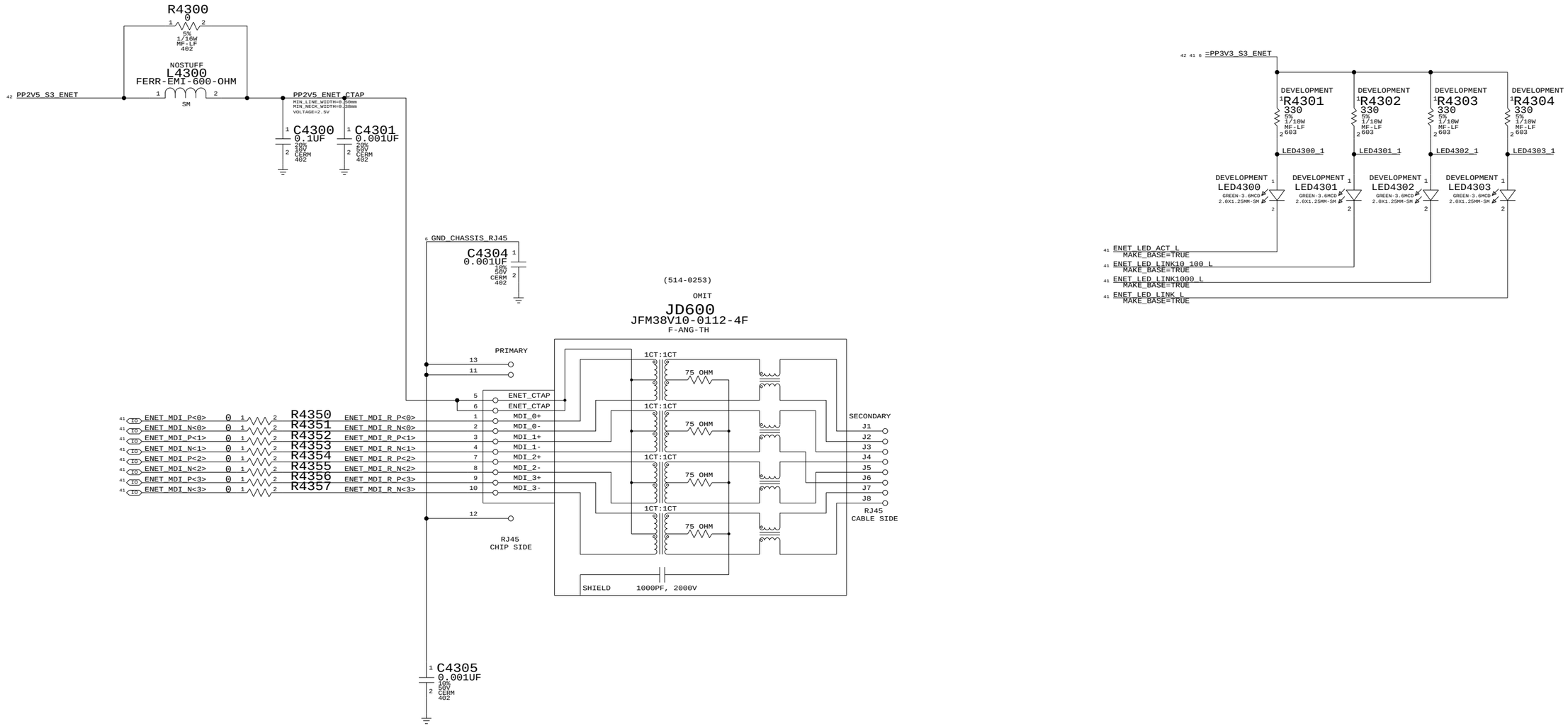
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	42	111

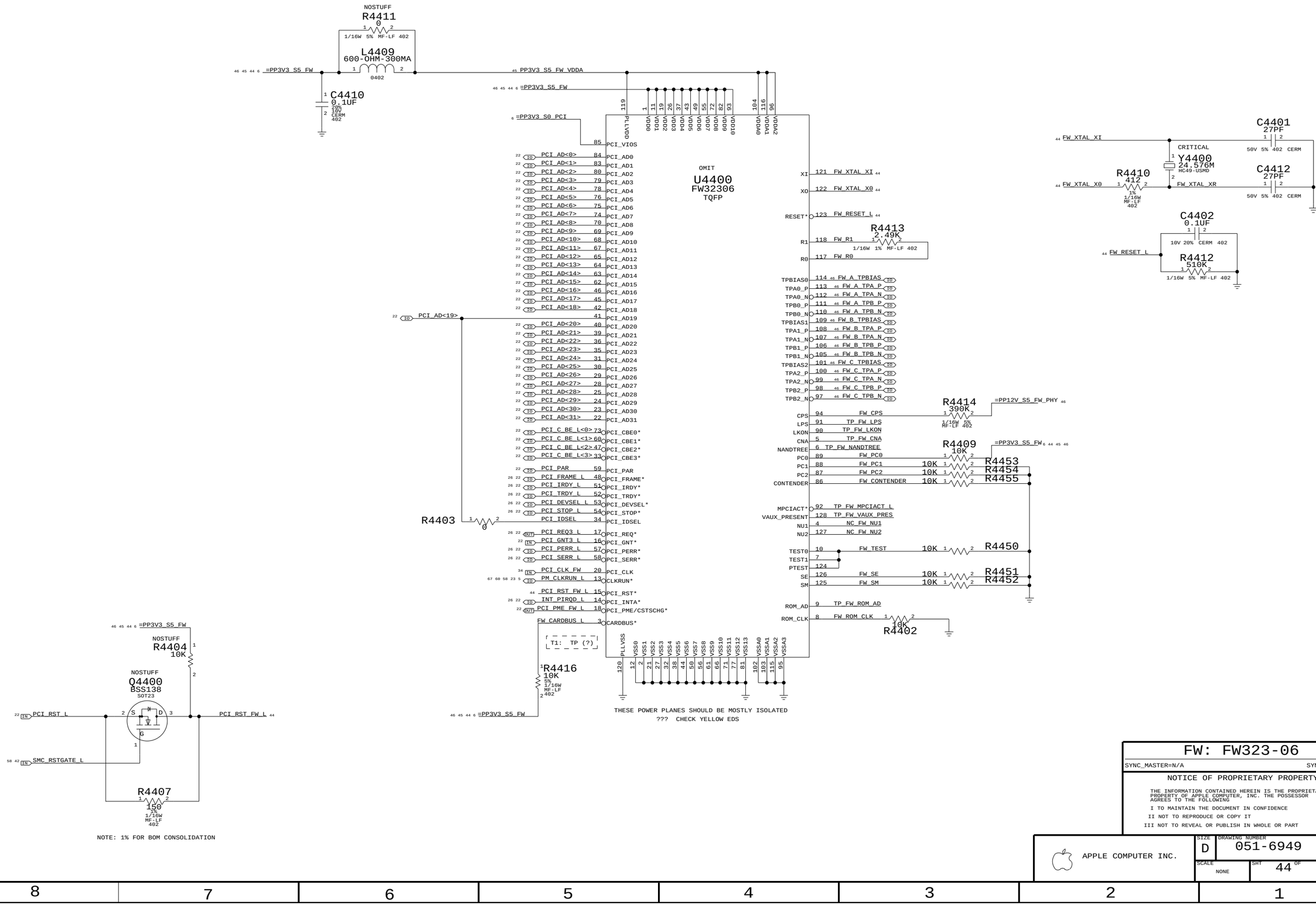


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0300	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0301	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

ETHERNET CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 43 OF 111	



FW:	FW323-06
SYNC_MASTER=N/A	SYNC_DATE=N/A

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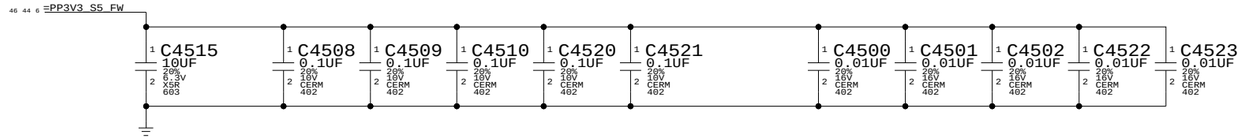
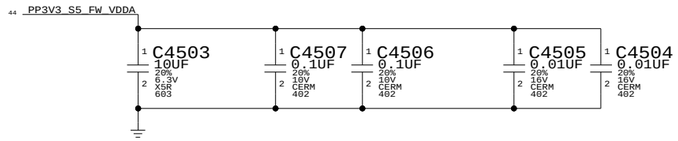
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 44 OF 111	





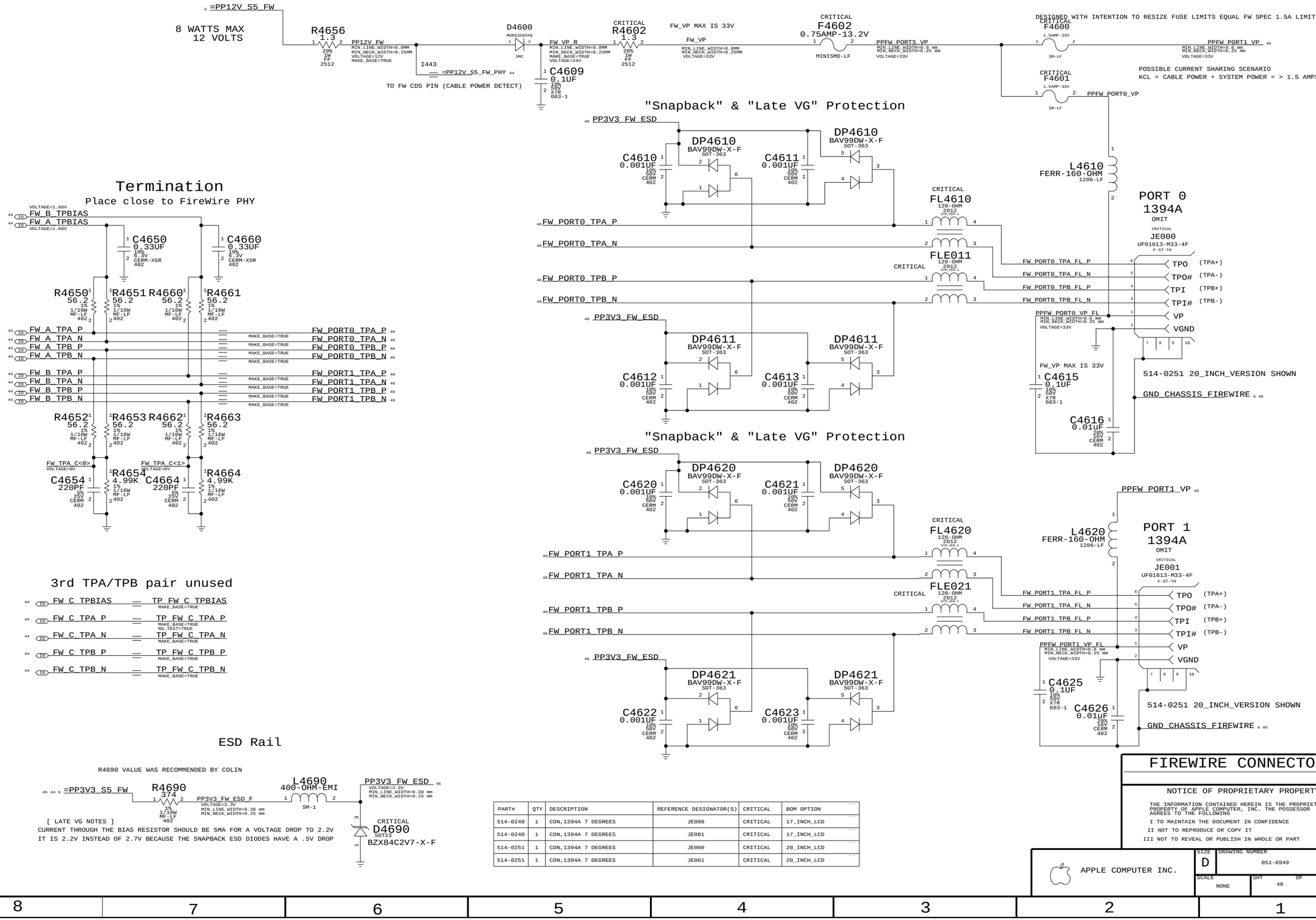
FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	45 OF 111



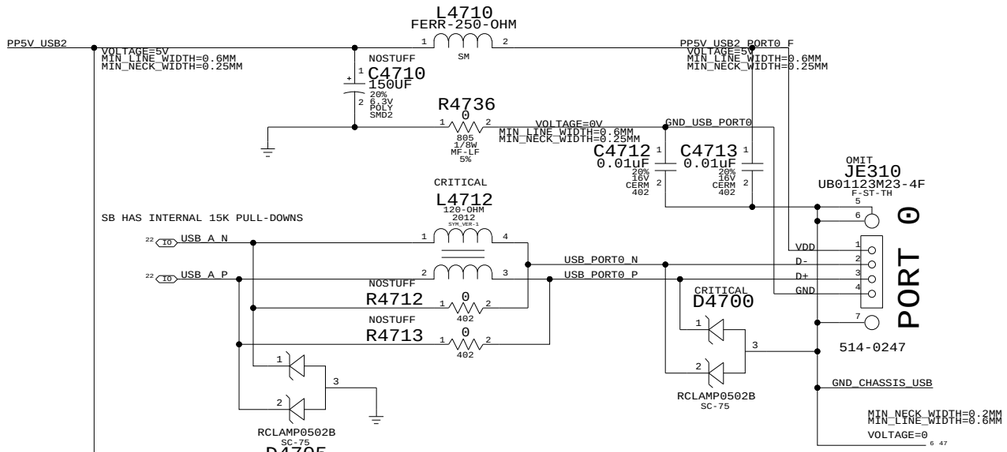
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

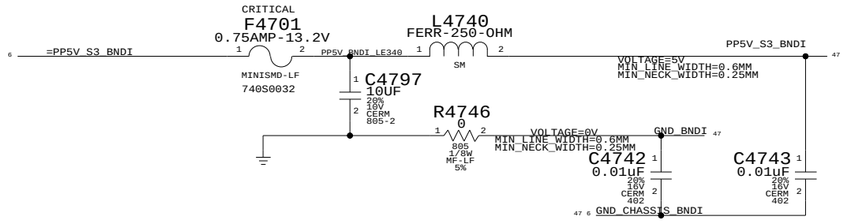
FIREWIRE CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 46 OF 111	

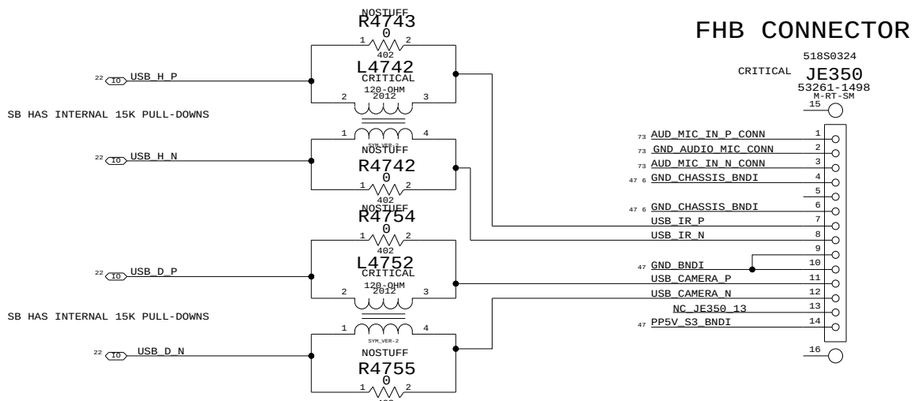
External USB Ports



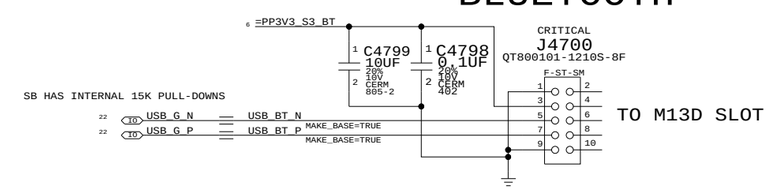


LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO JE350.



BLUETOOTH



NOTE: STANDOFFS FOR J4700

SDF4700
STDOFF-40D4.5H-1.35-TH

SDF4701
STDOFF-40D4.5H-1.35-TH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

USB Device Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 47 OF 111	

BLANK

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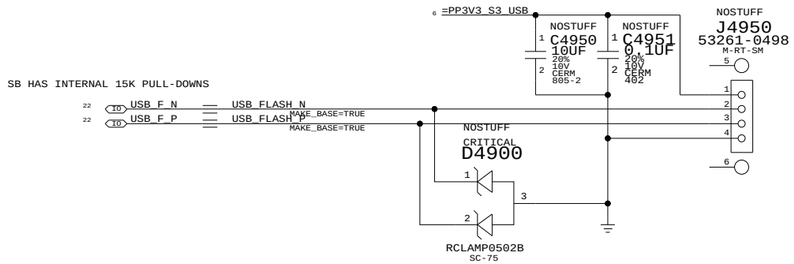
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	48 OF 111

CARD-READER USB CONN

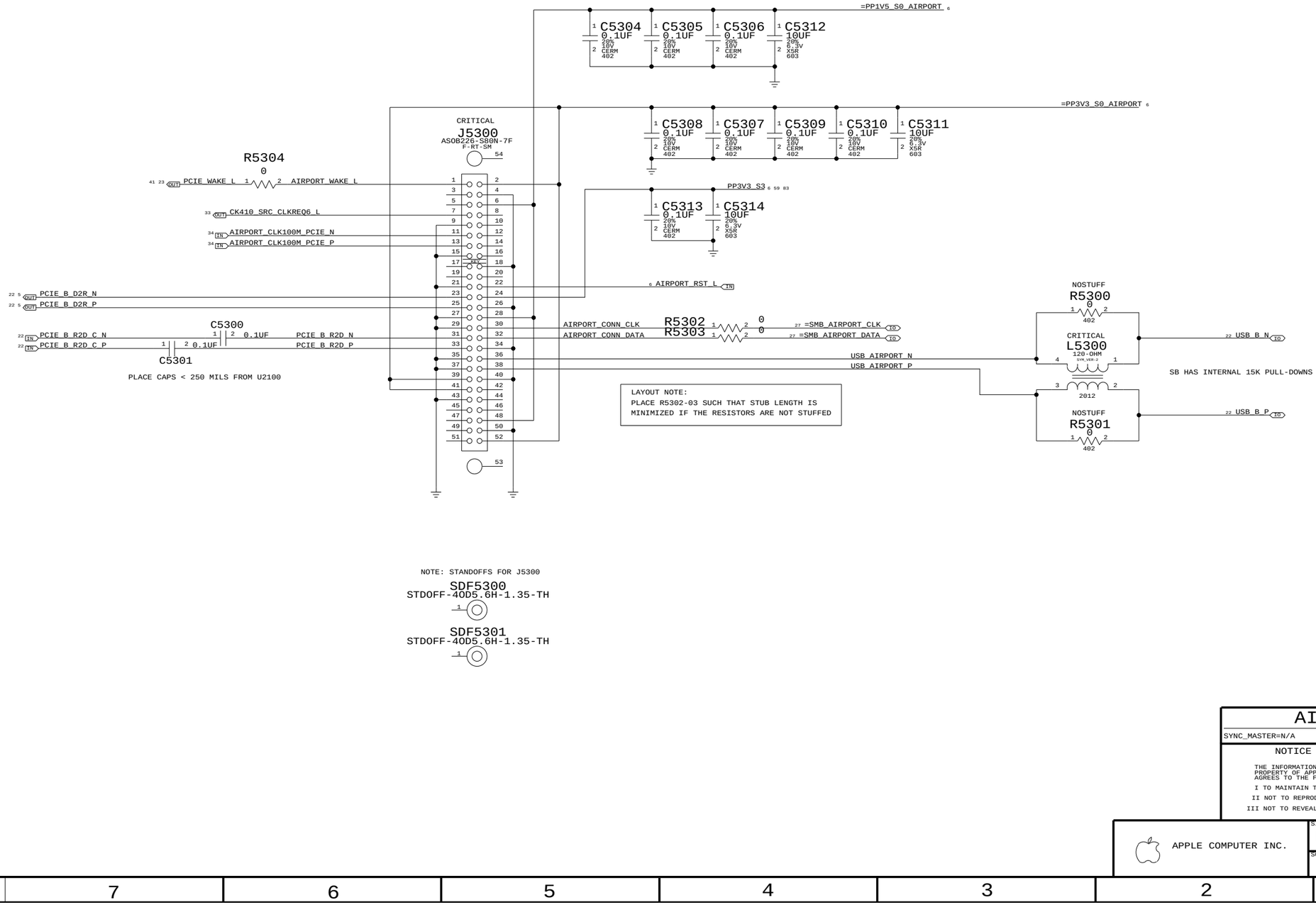


Flash Connector

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	49 OF 111



AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE NONE SHT 53 OF 111

22 IN PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N — TP_PCIE_C_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_C_D2R_P — TP_PCIE_C_D2R_P MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N — TP_PCIE_D_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_D_D2R_P — TP_PCIE_D_D2R_P MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N — TP_PCIE_E_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_E_D2R_P — TP_PCIE_E_D2R_P MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N — TP_PCIE_F_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_F_D2R_P — TP_PCIE_F_D2R_P MAKE_BASE=TRUE

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 54 OF 111	

UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

23 OUT	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	59	SMC_PM_G2_EN OUT
44 42 OUT	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	59	SMC_ADAPTER_EN OUT
77 26 IN	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB IN
76 IN	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22	SPI_SCLK IN
23 OUT	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22	SPI_SI OUT
23 OUT	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22	SPI_SO IN
75 OUT	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	59	SMC_PROCHOT_3_3_L IN
23 OUT	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	59	SMC_CPU_INIT_3_3_L IN
59	SMC_P20	D13	P20	P70/AN0	N12	76	SMC_CPU_ISENSE IN
59	SMC_P21	D14	P21	P71/AN1	R13	76	SMC_CPU_VSENSE IN
59	SMC_P22	D15	P22	P72/AN2	P13	59	SMC_GPU_ISENSE IN
59	SMC_P23	E12	P23	P73/AN3	R14	59	SMC_GPU_VSENSE IN
59 OUT	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	76	SMC_DCIN_ISENSE IN
59 OUT	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	76	SMC_PBUS_VSENSE IN
59	SMC_P26	E13	P26	P76/AN6	N13	59	SMC_BATT_ISENSE IN
59	SMC_P27	F14	P27	P77/AN7	P15	59	SMC_FWIRE_ISENSE IN
67 60 21 IO	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L IN
67 60 21 IO	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	59	SMC_TPM_GPIO OUT
67 60 21 IO	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 44 23 5	PM_CLKRUN_L IO
67 60 21 IO	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23	PM_SUS_STAT_L IN
67 60 21 IN	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	59	SC_TX_L OUT
6 IN	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	59	SC_RX_L IN
34 IN	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	59	SMB_BSB_CLK IO
67 60 23 OUT	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	59	SMC_ONOFF_L IN
59 OUT	SMC_XDP_TMS_L	A5	P40/TMI0	P91/IRQ1*	J2	59	SMC_BC_ACOK IN
59 OUT	SMC_XDP_TDI_L	B5	P41/TMO0	P92/IRQ0*	J1	59	SMC_BS_ALRT_L IN
59 IO	SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	88 79 77 23 6	PM_SLP_S3_L IN
59 OUT	SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23	PM_SLP_S4_L IN
59 OUT	SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L IN
59 OUT	SMC_XDP_TCK	C2	P45	P96/EXCL	H1	59	SMC_SUS_CLK IN
59 OUT	SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	59	SMC_SMB_0_DATA IO
59 OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
60 59 5 OUT	SMC_TX_L	G1	P50				
60 59 5 IN	SMC_RX_L	G4	P51				
59 IO	SMC_SMB_0_CLK	F2	P52/SCL0				

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

21 OUT	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	59	SMC_CASE_OPEN IN
60 22 IN	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5	SMC_TCK IN
26 23 5 IN	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5	SMC_TDI IN
67 59 OUT	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5	SMC_TDO OUT
59 14 IN	PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5	SMC_TMS IN
23 10 IO	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0 59
59 IO	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1 59
23 OUT	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59	SMC_LID IN
23 IN	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59	SMC_CPU_RESET_3_3_L IN
23 OUT	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59	SMC_BATT_ISET OUT
59 IN	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59	SMC_BATT_VSET OUT
76 OUT	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59	SMC_SYS_ISET OUT
59 IN	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59	SMC_SYS_VSET OUT
59 OUT	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22	SPI_CE_L IO
59 IN	SMC_EXCARD_PWR_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59	SMC_XDP_TCK_3_3 IN
59 IN	SMC_XDP_TDO_3_3_L	D11	PB7	PG2/EXIRQ10*/SDA2	N9	59	SMB_BSA_DATA IO
65 OUT	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	59	SMB_BSA_CLK IO
66 65 OUT	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	59	SMB_A_S3_DATA IO
66 65 OUT	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	59	SMB_A_S3_CLK IO
59 OUT	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	59	SMB_B_S0_DATA IO
65 IN	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	59	SMB_B_S0_CLK IO
66 65 IN	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59	SMC_PROCHOT OUT
66 65 IN	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59	SMC_THRMTRIP OUT
59 IN	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59	SMC_FWE IN
59 IN	SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59	ALS_GAIN OUT
59 IN	SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23	SMS_INT_L OUT
59 IN	SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59	SMS_ONOFF_L OUT
59 IN	SMC_ANALOG_ID	N11	PD3/AN11				
59 IN	SMC_NB_ISENSE	P10	PD4/AN12				
59 IN	SMC_MEM_ISENSE	R10	PD5/AN13				
59 IN	ALS_LEFT	N10	PD6/AN14				
59 IN	ALS_RIGHT	M10	PD7/AN15				

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 6 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 6 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
85 76 59 58 GND_SMC_AVSS

PP3V3_AVREF_SMC 59
59 58 6 =PP3V3_S5_SMC

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

N14	AVCC	AVREF	M14
N15	AVCC	AVREF	M15
P2	VCC		
P1	VCC		
J15	VCC		
A1	VCC		
F1	VCL		
E3	RES*		
A2	XTAL		
B2	EXTAL		
F2	MD1		
K1	MD2		
F4	NMI		
L1	ETRST*		
P12	AVSS		
R12	AVSS		
D1	VSS		
R4	VSS		
F12	VSS		
F13	VSS		
B13	VSS		
A13	VSS		
A4	VSS		
B4	VSS		
D2	VSS		

60 59 IN SMC_RST_L
59 SMC_XTAL
59 SMC_EXTAL

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
KBC_MDE
SMC_MD1 60
SMC_NMI 60 IN
SMC_TRST_L IN

NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800 SM
GND_SMC_AVSS 58 59 76 85

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6949 | REV. 09

SCALE NONE | SHT 58 OF 111

SMC RESET BUTTON

=PP3V3_S5_SMC

C5901 0.1uF 20% 10V CERM 402

CRITICAL U5900 RN5VD30A-F SOT23-5 VDD CD NC GND OUT

R5900 1K 5% 1/16W MF-LF 402

SMC_MANUAL_RST_L

DEVELOPMENT SW5900 SPST SM-LF

C5900 0.01UF 10% 16V CERM 402

SMC_RST_L

WHITE SYSLED

LED2901 WHITE-500MCD 3X2MM-SM

PP5V_S3

SYS_LED_DRV_K

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

17_INCH_LCD

R5901 56.2 1% 1/16W MF-LF 402

SYS_LED_DRV_C

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q5900 FDV301N SOT23-LF

SMC_SYS_LED

NOSTUFF R5902 4.7K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES,LF,MTL FILM,39.2 OHM,1%,402	R5901	20_INCH_LCD

SMC I2C BUS PULLUPS (INCLUDING UNUSED ONES)

PP3V3_S0

2.2K R5903 SMB_B_S0_CLK

2.2K R5904 SMB_B_S0_DATA

PP3V3_S3

2.2K R5905 SMB_A_S3_CLK

2.2K R5906 SMB_A_S3_DATA

=PP3V3_S5_SMC

10K R5910 SMB_BSB_CLK

10K R5911 SMB_BSB_DATA

10K R5912 SMC_SMB_0_CLK

10K R5913 SMC_SMB_0_DATA

10K R5914 SMB_BSA_CLK

10K R5915 SMB_BSA_DATA

PULLUPS FOR SYSTEM STATE PINS

10K R5916 SMC_LID

PULLDOWNS FOR SYSTEM STATE PINS

10K R5917 SMC_CASE_OPEN

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20
SMC_P21	NC_SMC_P21
SMC_P22	NC_SMC_P22
SMC_P23	NC_SMC_P23
SMC_P26	NC_SMC_P26
SMC_P27	NC_SMC_P27
SMC_BATT_ISET	NC_SMC_BATT_ISET
SMC_BATT_VSET	NC_SMC_BATT_VSET
SMC_SYS_ISET	NC_SMC_SYS_ISET
SMC_SYS_VSET	NC_SMC_SYS_VSET
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN
SMC_ANALOG_ID	NC_SMC_ANALOG_ID
ALS_GAIN	NC_ALS_GAIN

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	
SMC_PF0	TP_SMC_PF0	
SMC_PM_G2_EN	TP_PM_G2_EN	FUNC_TEST=TRUE
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	FUNC_TEST=TRUE
ALS_LEFT	TP_ALS_LEFT	FUNC_TEST=TRUE
ALS_RIGHT	TP_ALS_RIGHT	FUNC_TEST=TRUE
SMC_PF1	TP_SMC_PF1	
SMC_PB7	TP_SMC_PB7	FUNC_TEST=TRUE
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	FUNC_TEST=TRUE
SMC_PB7	TP_SMC_PB7	FUNC_TEST=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	FUNC_TEST=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	FUNC_TEST=TRUE

TPM RESET PULLUP

PP3V3_TPM_3VSB

SMC_TPM_RESET_L R5827 10K

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L<0>

SENSE GPU REGULATOR OUTPUT CURRENT

SMC_GPU_ISENSE — GPUVCORE_IOUT

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L
SMC_SUS_CLK	SUS_CLK_SB

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_NB_ISENSE	NC_SMC_NB_ISENSE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE

UNUSED_SMC_SENSE 10K R5924

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SMC_EXCARD_CP	R5830	10K
SMC_EXCARD_PWR_OC_L	R5831	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K

NOT_DEVELOPMENT_SMC

SC_RX_L 0 R5922 SMC_RX_L

SC_TX_L 0 R5923 SMC_TX_L

DEVELOPMENT_SMC

SELECT TPM GPIO

SMC_TPM_GPIO 0 R5920 TPM_GPIO1

0 R5921 TPM_GPIO2

SMC_TPM_PP R5995 0

SMC_TPM_PP — TPM_PP

SENSE GPU VCORE

PP1V0R1V2_S0_GPU R5919 4.53K 1% 1/16W MF-LF 402

SMC_GPU_VSENSE

C5919 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

ALIAS SENSORS INTO SMC I2C BUSSES

SMB_B_S0_CLK — =I2C_HD_TEMP_SCL

SMB_B_S0_DATA — =I2C_HD_TEMP_SDA

=I2C_ODD_TEMP_SCL

=I2C_ODD_TEMP_SDA

=SMB_THRM_CLK

=SMB_THRM_DATA

SMB_GPU_NB_THRM_CLK

SMB_GPU_NB_THRM_DATA

SMB_A_S3_CLK — I2C_ALS_SCL

SMB_A_S3_DATA — I2C_ALS_SDA

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM

GND_NEXT_TO_SMC

SMC-CPU JTAG LEVEL-SHIFTER

XDP_TDI — (PULLUP ON CPU PAGE) NOSTUFF Q5902 2N7002DW-X-F SOT-363 — SMC_XDP_TDI_L

XDP_TMS — (PULLUP ON CPU PAGE) NOSTUFF Q5902 2N7002DW-X-F SOT-363 — SMC_XDP_TMS_L

=PP1V05_S0_CPU

SMC_XDP_TRST_L_R — NOSTUFF R5927 1K — SMC_XDP_TRST_L — NOSTUFF Q5903 MMDT3904XF SOT-363-LF — XDP_TRST_L

(PULLDOWN ON ITP CONNECTOR PAGE) R5927 VALUE SUBJECT TO CHANGE.

SMC_XDP_TCK_R — NOSTUFF R5925 1K — SMC_XDP_TCK — NOSTUFF Q5903 MMDT3904XF SOT-363-LF — XDP_TCK

R5925 VALUE SUBJECT TO CHANGE. (PULLDOWN ON CPU PAGE)

AMBIENT LIGHT SENSOR CONNECTOR

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

I2C ADDR:72(1001000)

CRITICAL J2901 53398-0476 F-ST-SM

PP3V3_S3

I2C_ALS_SDA

I2C_ALS_SCL

518S0328

SMC 3.3V -> CPU 1.05V SHIFTER

CPU_PROCHOT_L — Q5901 2N7002DW-X-F SOT-363 — SMC_PROCHOT

PM_THRMTRIP_L — Q5901 2N7002DW-X-F SOT-363 — SMC_THRMTRIP

POWER BUTTON HEADER

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

J2903 53398-0276 M-ST-SM

POWER_BUTTON_L

518S0327

R5907 1K 5% 1/16W MF-LF 402

SYS POWER BUTTON

SW5901 SPST SM-LF

SMC_ONOFF_L

C5902 0.1uF 20% 10V CERM 402

GENERATE 0.48V MID-VREF

=PP3V3_S0_FAN

R5930 6.2K 5% 1/16W MF-LF 402

P0V48_SMC_LSREF

R5931 1K 5% 1/16W MF-LF 402

SMC CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

C5800 22PF CERM 5% 50V 402

SMC_XTAL

OMIT Y5800 20.000M SM-3

C5801 22PF CERM 5% 50V 402

SMC_EXTAL

TPM CRYSTAL

C6704 15PF 5% 50V CERM 402

TPM_XTALI

CRITICAL Y6700 32.768K SM-LF

C6705 15PF 402 50V 5% CERM

TPM_XTALO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL,20.00,80PPM,HC49,SMD,LF	Y5800	CRITICAL	

CPU 1.05V -> SMC 3.3V SHIFTER

PP3V3_S5

=PP3V3_S0_FAN

C5903 0.1UF 20% 10V CERM 402

P0V48_SMC_LSREF

CPU_PROCHOT_L

U5999 LMV339 TSSOP

R5932 1K — SMC_PROCHOT_3_3_L

R5933 1K — SMC_CPU_RESET_3_3_L

TP_U5999_P1

PCB: ENSURE FSB_CPURST_L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

R5934 1K — SMC_XDP_TCK_3_3

XDP_TCK

R5935 1K — SMC_XDP_TDO_3_3_L

XDP_TDO

P0V48_SMC_LSREF

TP_U5999_P13

TP_U5999_P14

PRECISION 3.3V AVREF FOR SMC

PP5V_S5

R5942 10K — Q5910 NTR4101P SOT-23 — SMC_REF_GATE2

SMC_REF_GATE1

R5941 10K

C5943 1UF 10% 6.3V CERM 402

SMC_REF_IN

TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

NOSTUFF R5940 0

=PP3V3_S5_SMC

CRITICAL U5940 REF3133 SOT23-3 IN TI OUT GND

C5940 0.47UF 20% 6.3V CERM-X5R 402

C5942 10UF 20% 6.3V X5R 603

PP3V3_AVREF_SMC

C5941 0.01UF 20% 16V CERM 402

GND_SMC_AVSS

SMC & TPM SUPPORT

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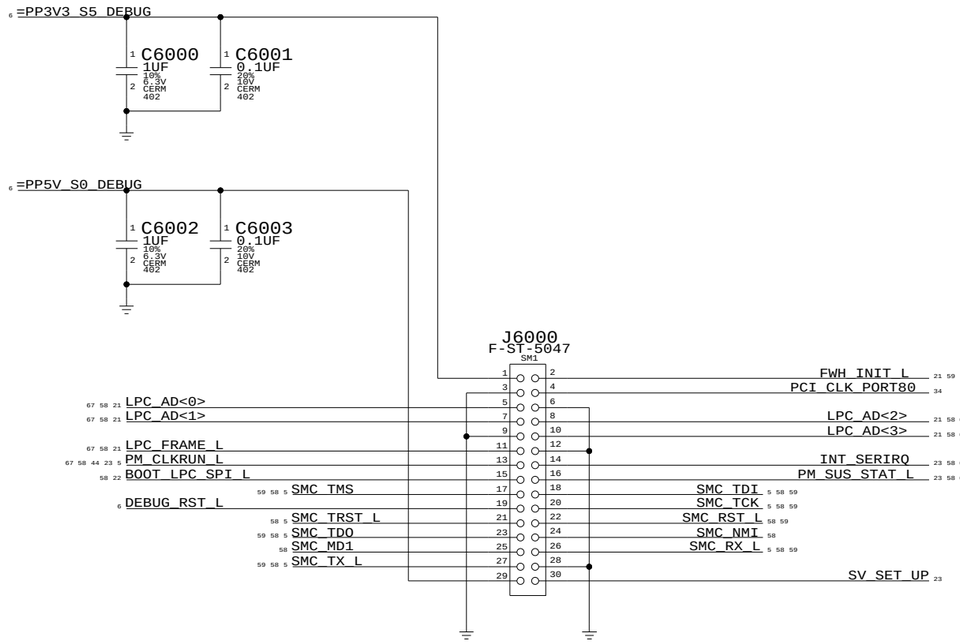
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 59 OF 111	



LPC+ CONN

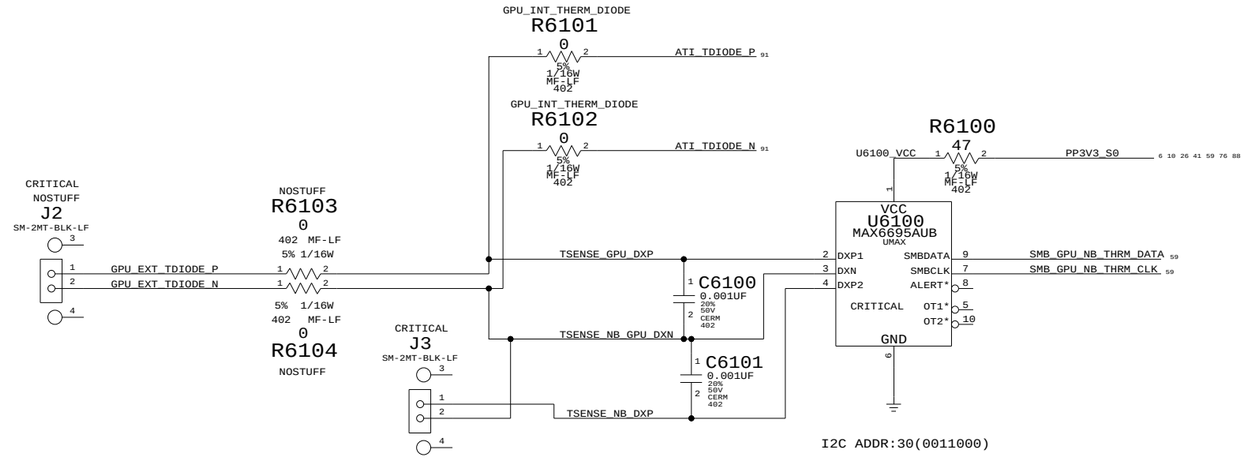
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE

SHT 60 OF 111



GPU+NB THERMAL

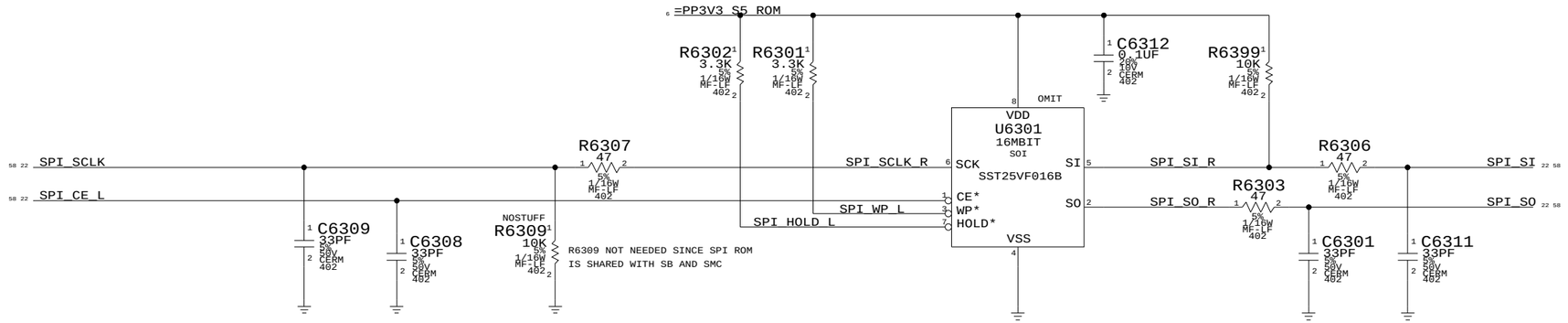
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE NONE

SHT 61 OF 111



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

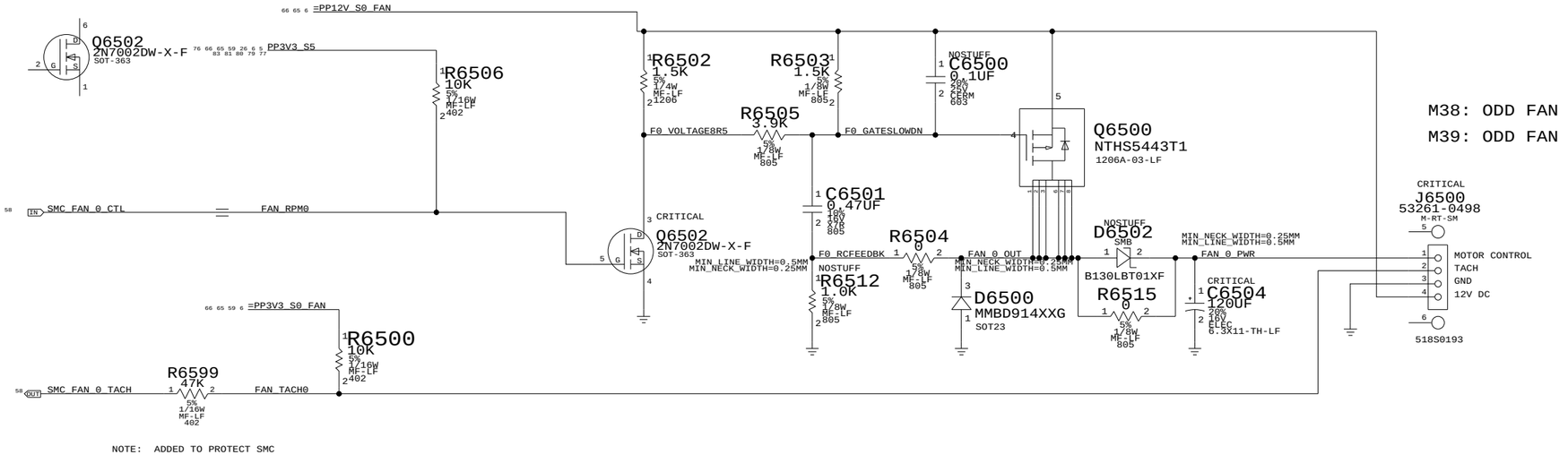
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

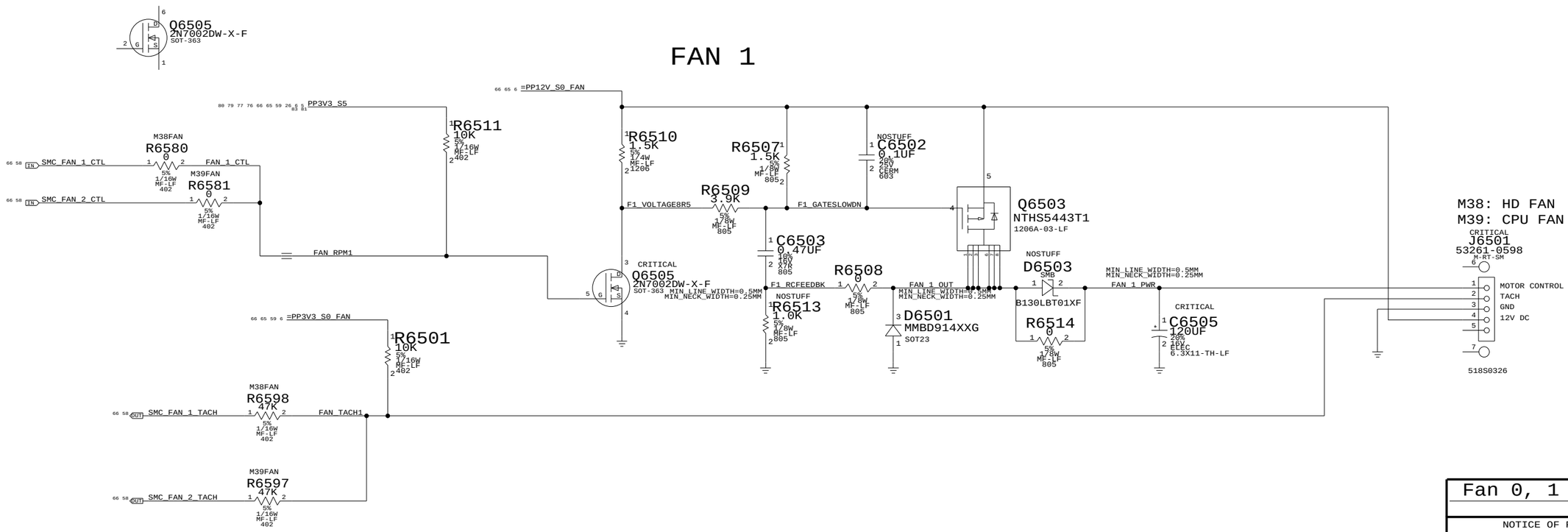
SCALE	SHT	OF
NONE	63	111

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



Fan 0, 1 & System Temp

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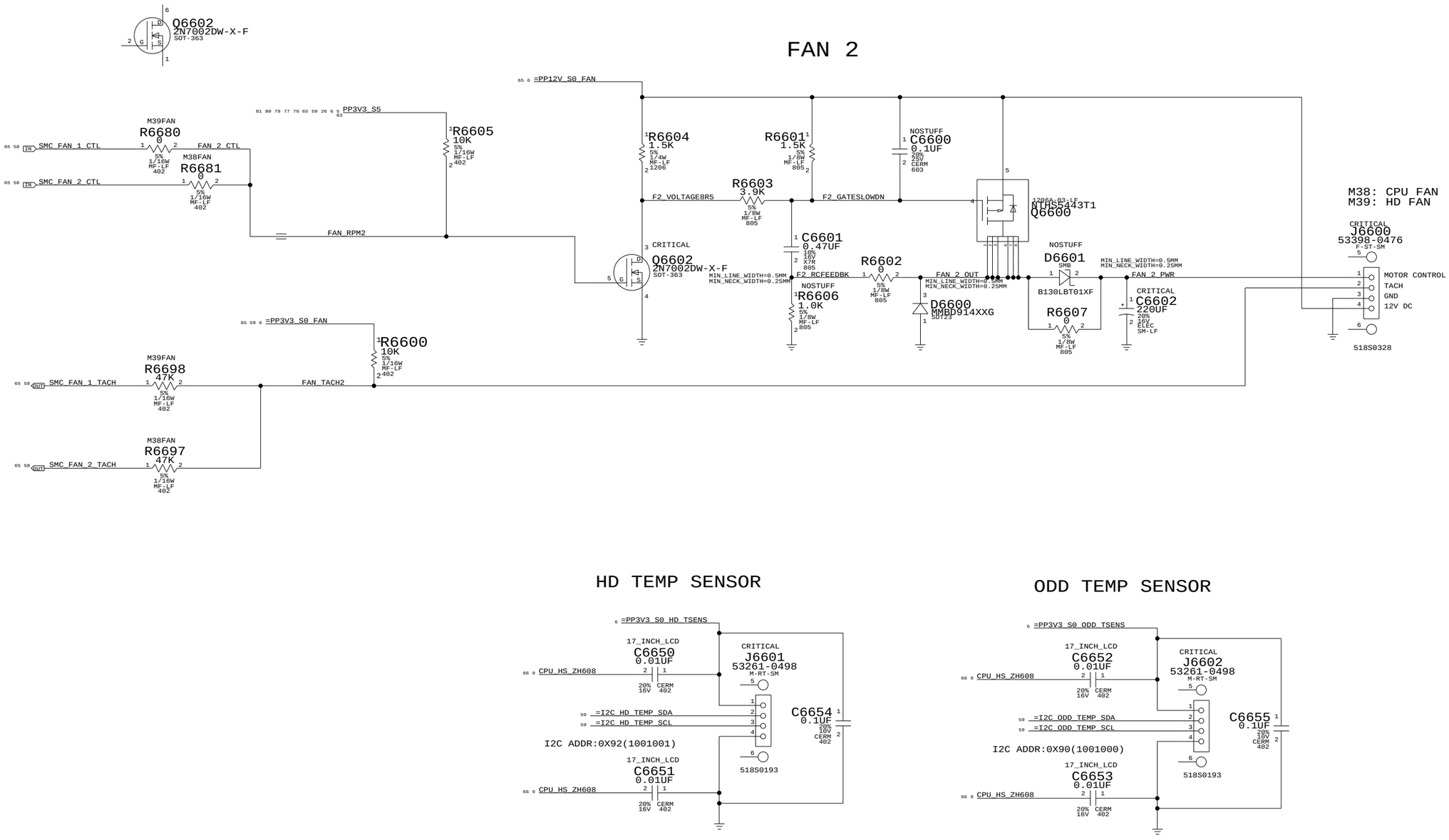
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 65 OF	111

FAN 2



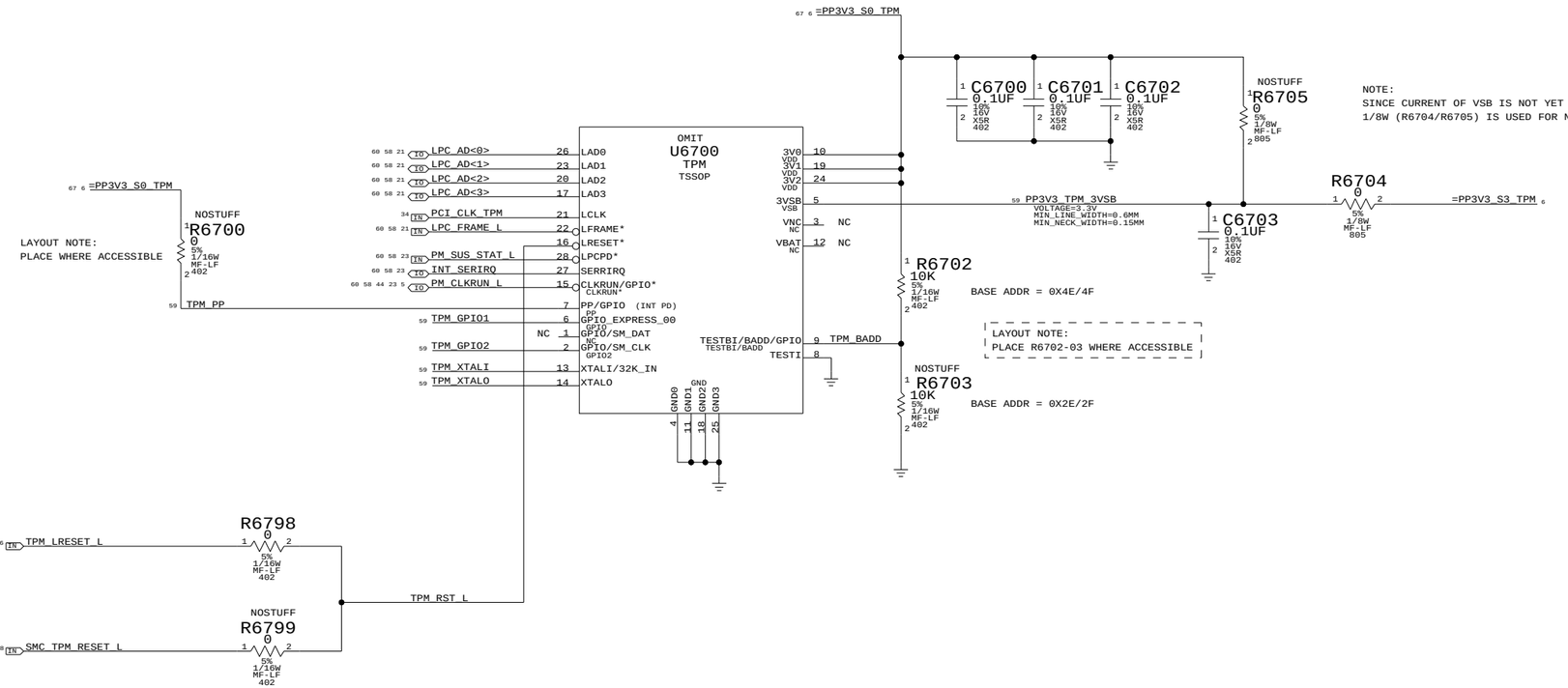
HD TEMP SENSOR

ODD TEMP SENSOR

Fan 2 & HD Temp

APPLE COMPUTER INC.

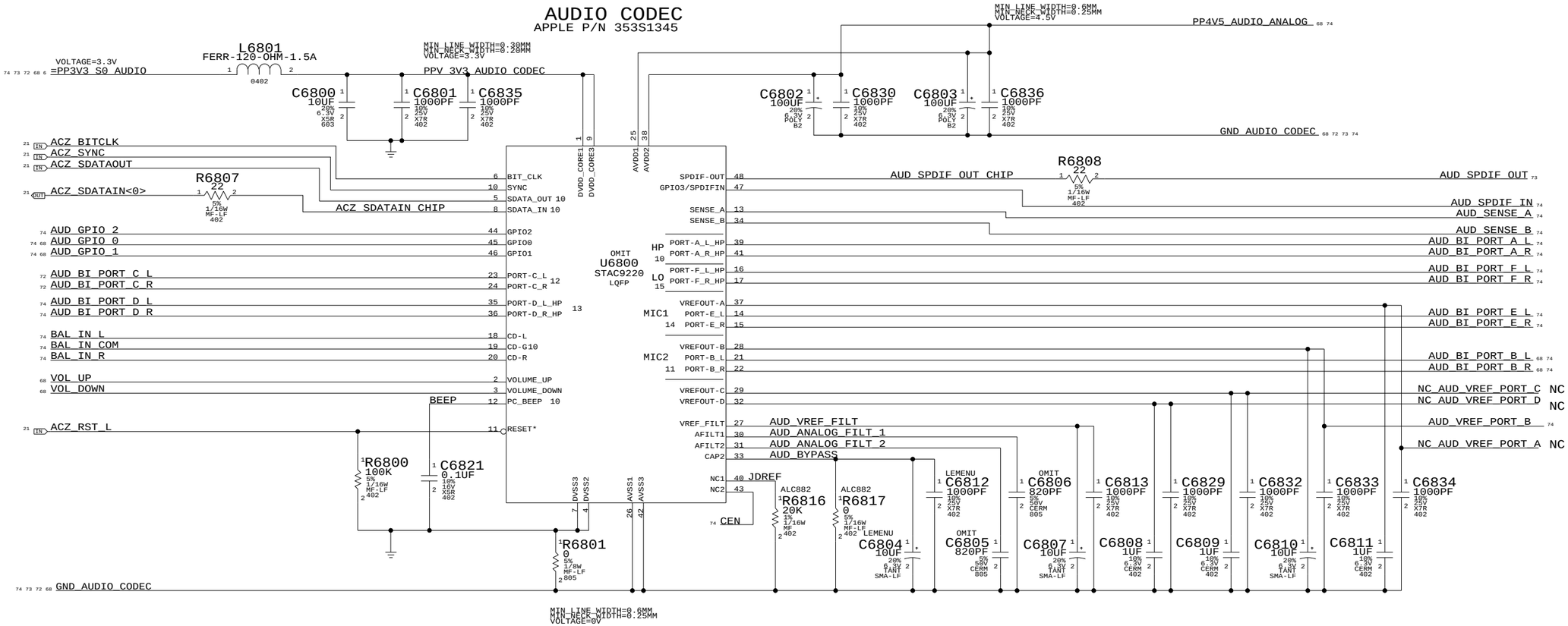
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 66 OF 111	

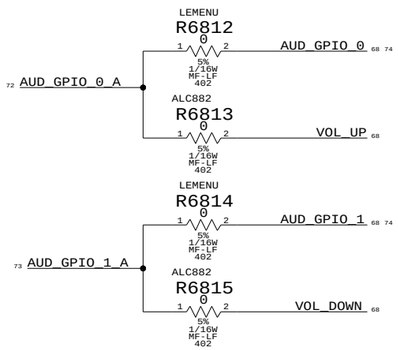


TPM	
SYNC_MASTER=N/A	SYNC_DATE=N/A

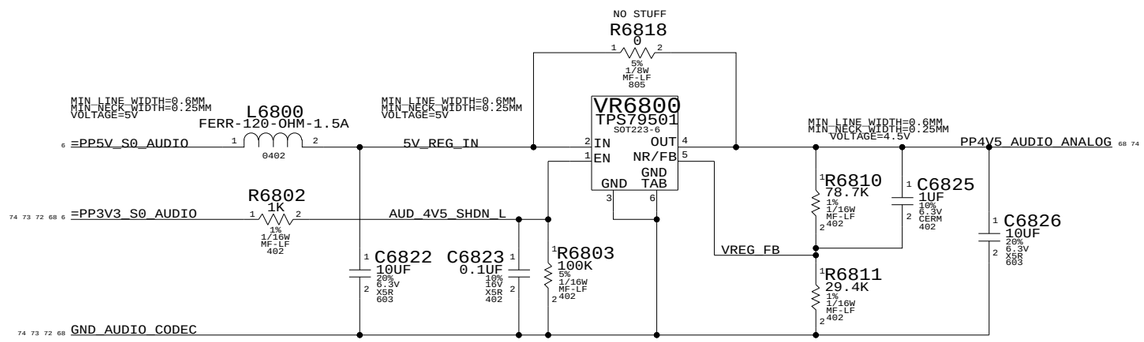
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6949	REV. 09
	SCALE NONE	SHT 67 OF 111	

AUDIO CODEC
APPLE P/N 353S1345





4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233



MIC INPUT TO BOTH L&R

AUD_BI_PORT_B_L — AUD_BI_PORT_B_R

SYNC_MASTER=FINO-SO	SYNC_DATE=04/28/2005

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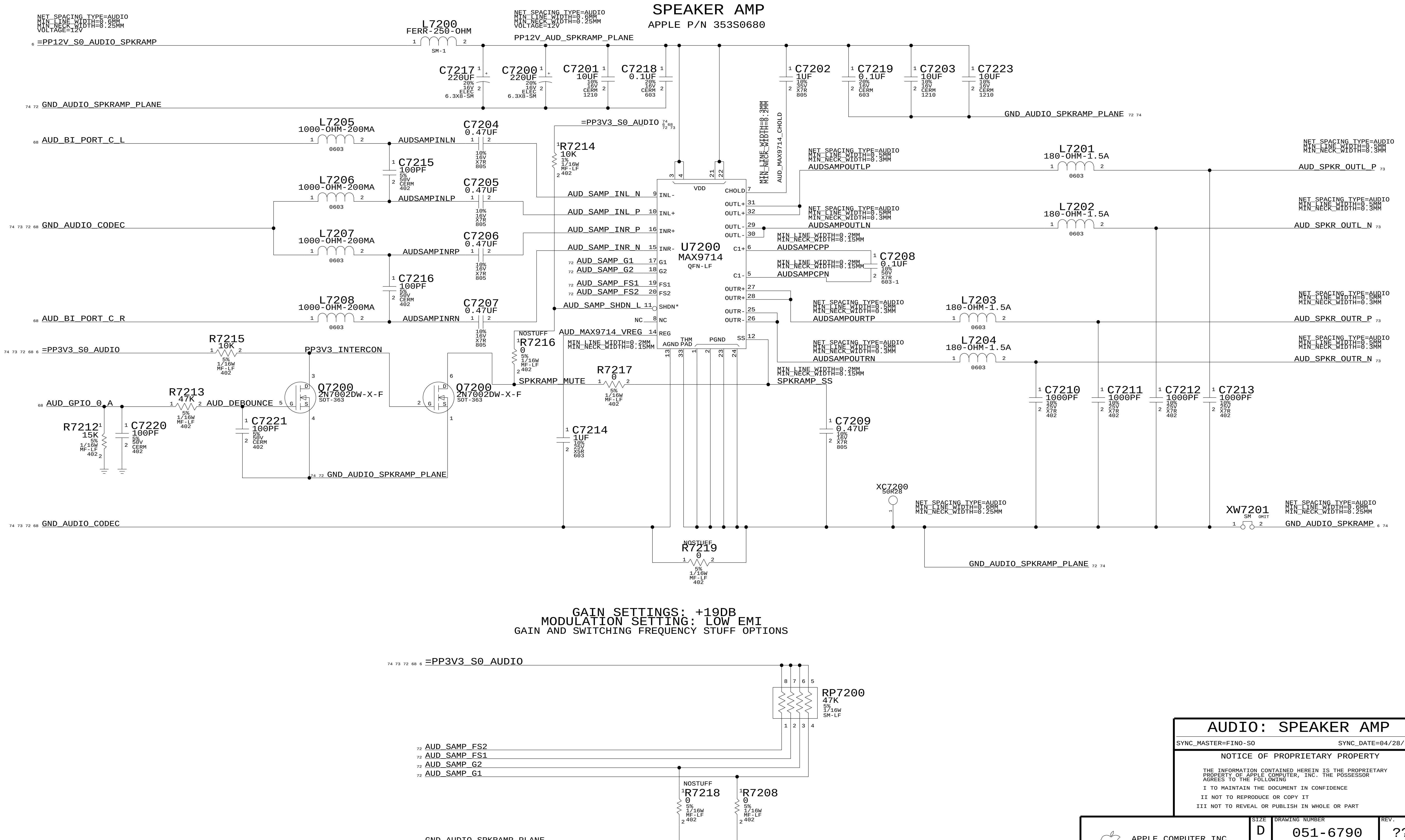
AUDIO: CODEC

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
	SCALE: NONE	SHT 68 OF 154	



SPEAKER AMP
APPLE P/N 353S0680
=PP12V_S0_AUDIO_SPKRAMP
L7200
FERR-250-OHM
PP12V_AUD_SPKRAMP_PLANE
GND_AUDIO_SPKRAMP_PLANE
C7217 220UF
C7200 220UF
C7201 10UF
C7218 0.1UF
C7202 1UF
C7219 0.1UF
C7203 10UF
C7223 10UF
AUD_BI_PORT_C_L
L7205 1000-OHM-200MA
AUDSAMPINLN
C7204 0.47UF
C7215 100PF
L7206 1000-OHM-200MA
AUDSAMPINLP
C7205 0.47UF
GND_AUDIO_CODEC
L7207 1000-OHM-200MA
AUDSAMPINRP
C7206 0.47UF
C7216 100PF
L7208 1000-OHM-200MA
AUD_BI_PORT_C_R
AUDSAMPINRN
C7207 0.47UF
=PP3V3_S0_AUDIO
R7214 10K
AUD_SAMP_INL_N
AUD_SAMP_INL_P
AUD_SAMP_INR_P
AUD_SAMP_INR_N
AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2
AUD_SAMP_SHDN_L
AUD_MAX9714_VREG
U7200
MAX9714
QFN-LF
AUD_MAX9714_CHOLD
AUDSAMPOUTLP
L7201 180-OHM-1.5A
AUD_SPKR_OUTL_P
AUDSAMPOUTLN
L7202 180-OHM-1.5A
AUD_SPKR_OUTL_N
AUDSAMPCPP
C7208 0.1UF
AUDSAMPCPN
AUDSAMPOUTRP
L7203 180-OHM-1.5A
AUD_SPKR_OUTR_P
AUDSAMPOUTRN
L7204 180-OHM-1.5A
AUD_SPKR_OUTR_N
R7215 10K
PP3V3_INTERCON
NOSTUFF R7216 0
SPKRAMP_MUTE
R7217 0
SPKRAMP_SS
AUD_GPIO_0_A
R7213 47K
AUD_DEBOUNCE
Q7200 2N7002DW-X-F
Q7200 2N7002DW-X-F
R7212 15K
C7220 100PF
C7221 100PF
C7214 1UF
C7209 0.47UF
C7210 1000PF
C7211 1000PF
C7212 1000PF
C7213 1000PF
XC7200
XW7201
GND_AUDIO_SPKRAMP
NOSTUFF R7219 0
GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS
=PP3V3_S0_AUDIO
RP7200 47K
AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1
NOSTUFF R7218 0
R7208 0
GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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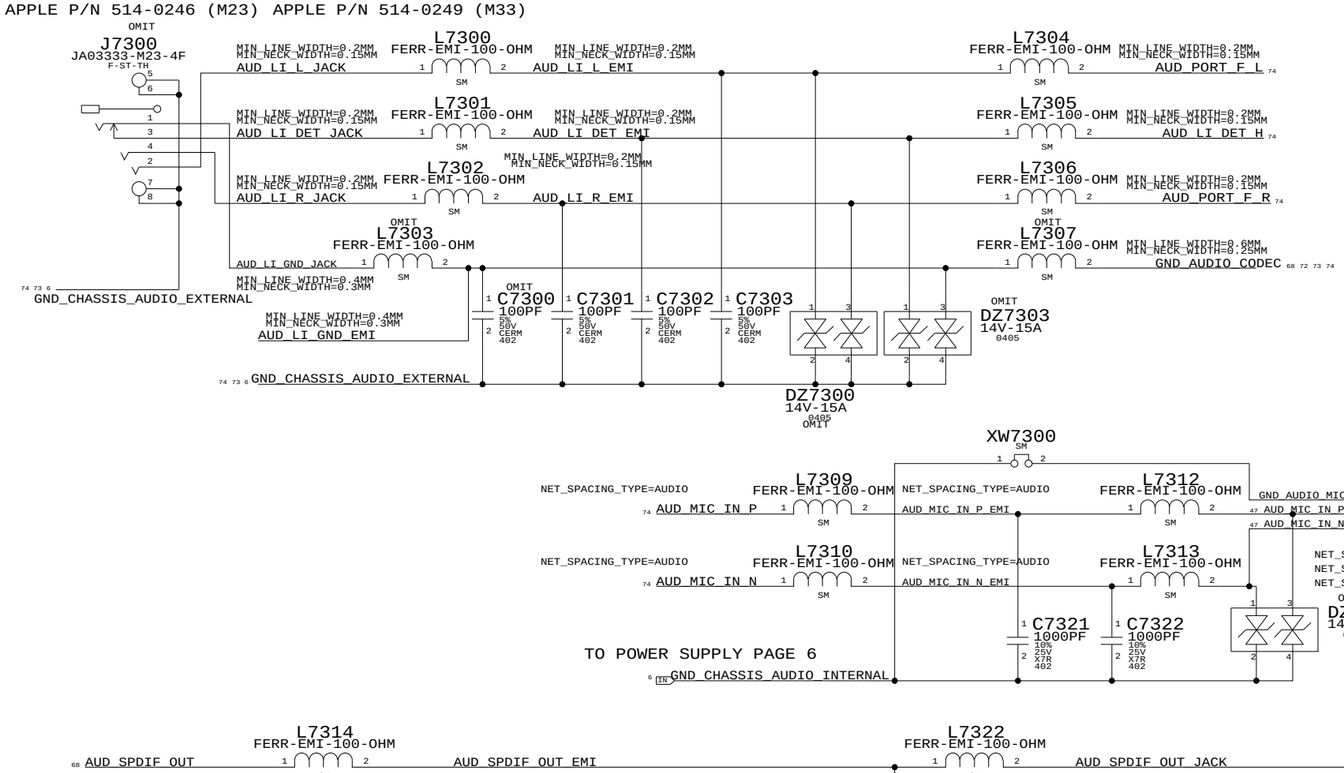
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	??
SCALE NONE	SHT 72	OF 154

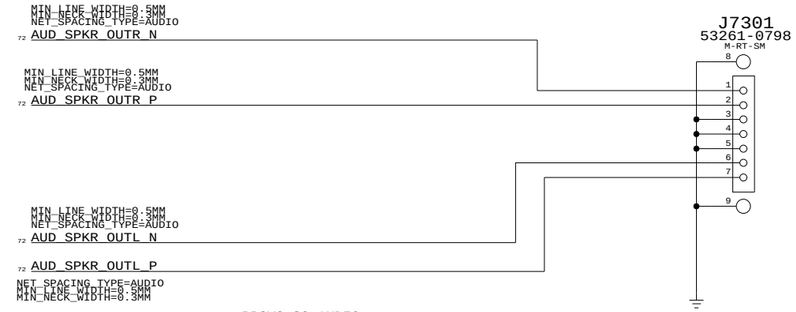
LINE IN JACK

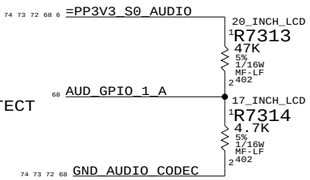
APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)



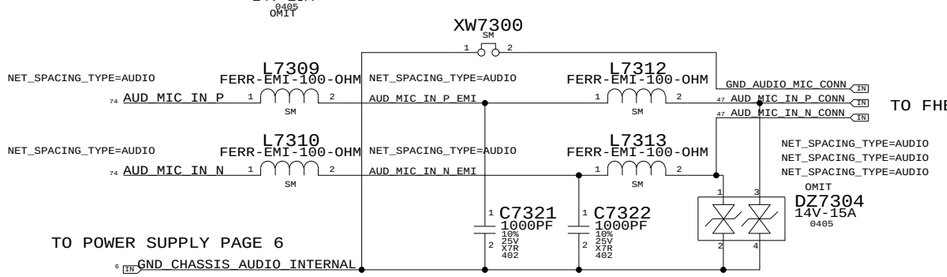
SPEAKER CABLE CONNECTOR

APPLE P/N 518S0325



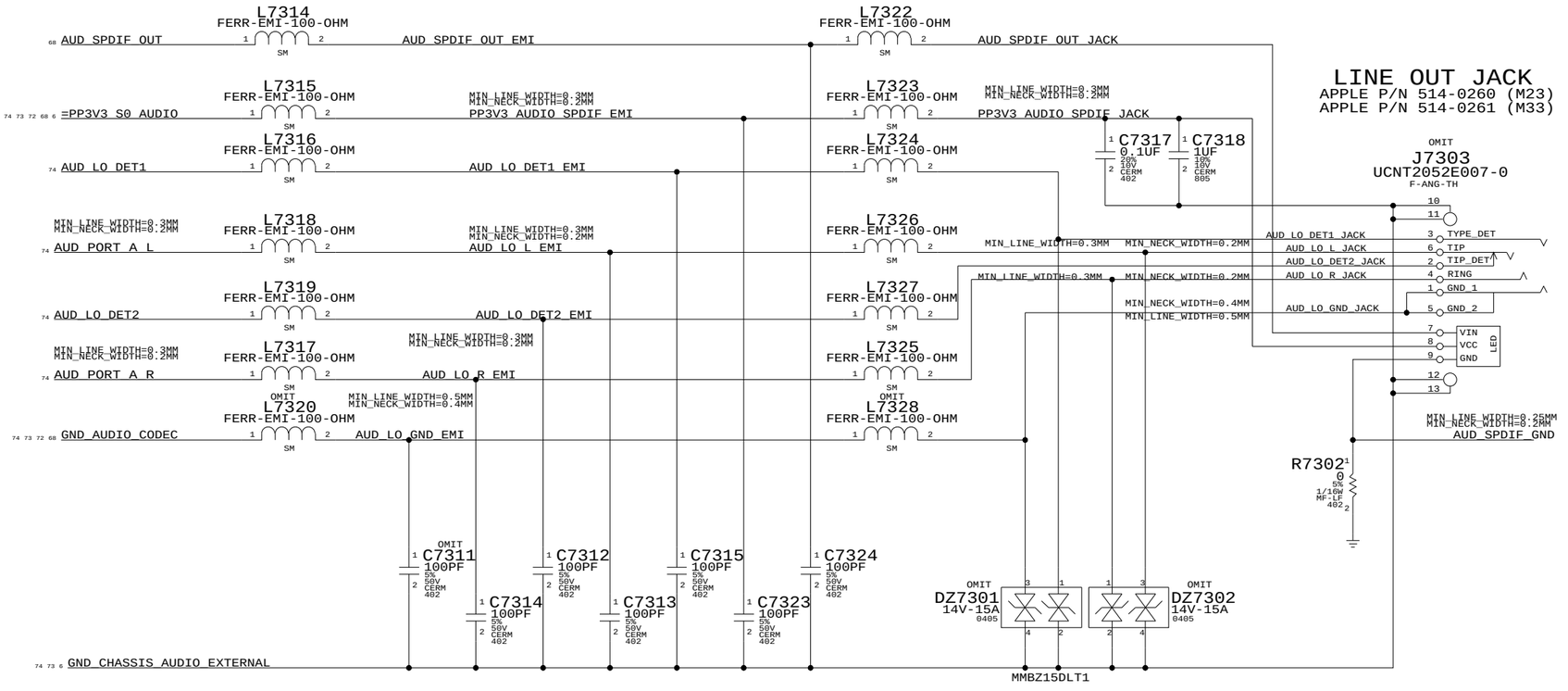


TO GPIO 1
SPEAKER TYPE DETECT



TO POWER SUPPLY PAGE 6

TO FHB CONNECTOR PAGE 47



LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	J7300	CRITICAL	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 5.5 DEG	J7303	CRITICAL	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 4.5 DEG	J7300	CRITICAL	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	J7303	CRITICAL	20_INCH_LCD
353S1345	1	SIGMATEL STAC9220	U6800	CRITICAL	LEMENU
353S1268	1	REALTEK ALC882	U6800	CRITICAL	ALC882
131S8223	2	CAPACITOR, 820PF	C6805,C6806	CRITICAL	LEMENU
131S0534	2	CAPACITOR, 1UF	C6805,C6806	CRITICAL	ALC882
377S0043	5	TRANSIENT VOLTAGE DIODE	DZ7300,DZ7301,DZ7302,DZ7303,DZ7304	CRITICAL	
113S0022	4	RESISTOR, 0 OHM, 0603	L7303,L7307,L7320,L7328		
116S0004	2	RESISTOR, 0 OHM, 0402	C7300,C7311		

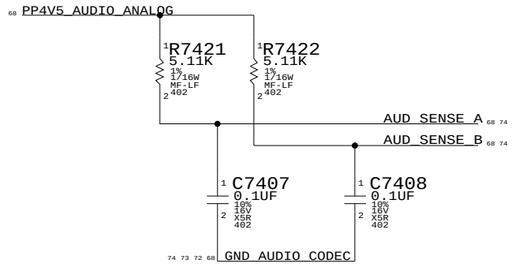
AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	??
SCALE: NONE	SHT 73 OF 154	

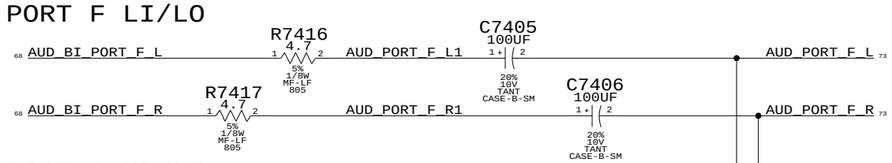
JACK SENSE PULL UPS(PLACE NEXT TO CODEC)



USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

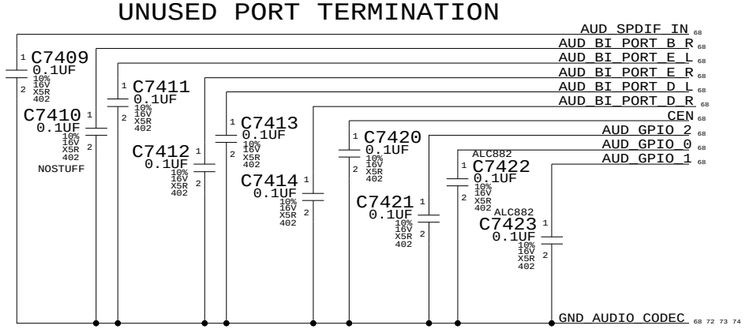
UNUSED PORTS
PORT E
PORT D

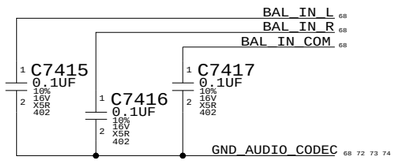
PORT F LI/LO



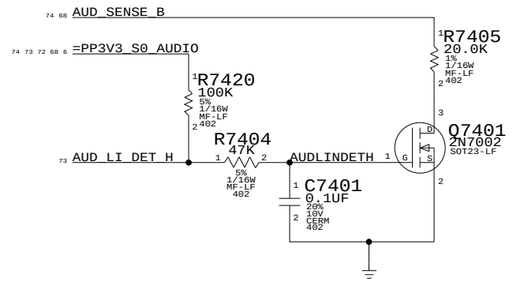
PORT A HP/LI

UNUSED PORT TERMINATION

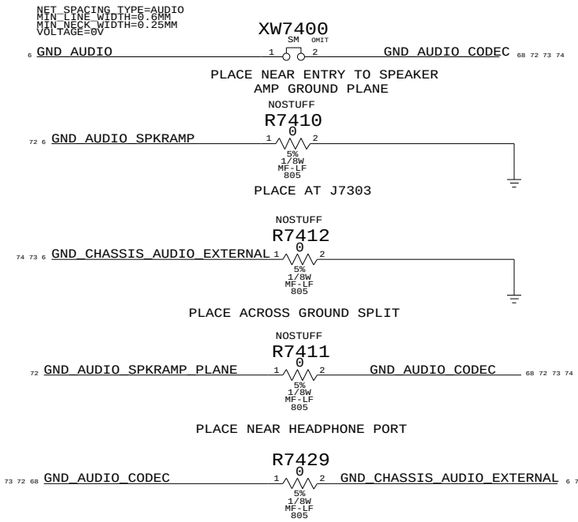




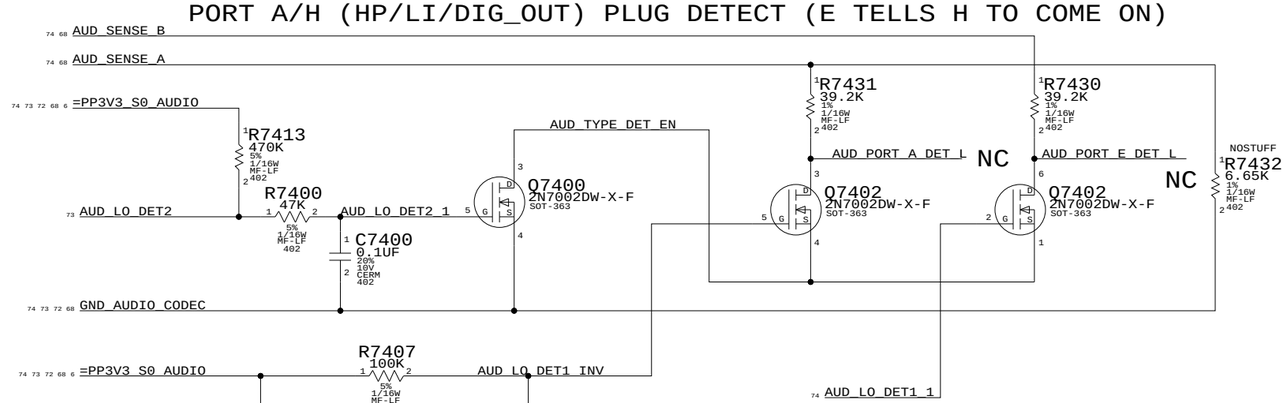
PORT F (LI/LO) PLUG DETECT



AUDIO GROUND RETURNS

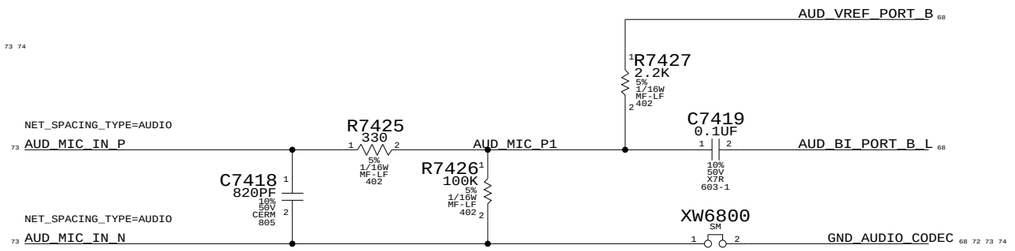


PORT A/H (HP/LI/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



R7432 ENABLES PORT B AND C

MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6790	??
SCALE: NONE	SHT 74	OF 154

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

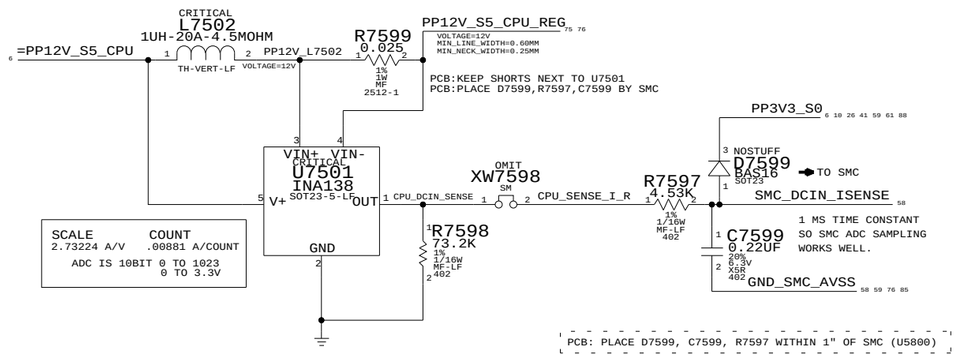
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

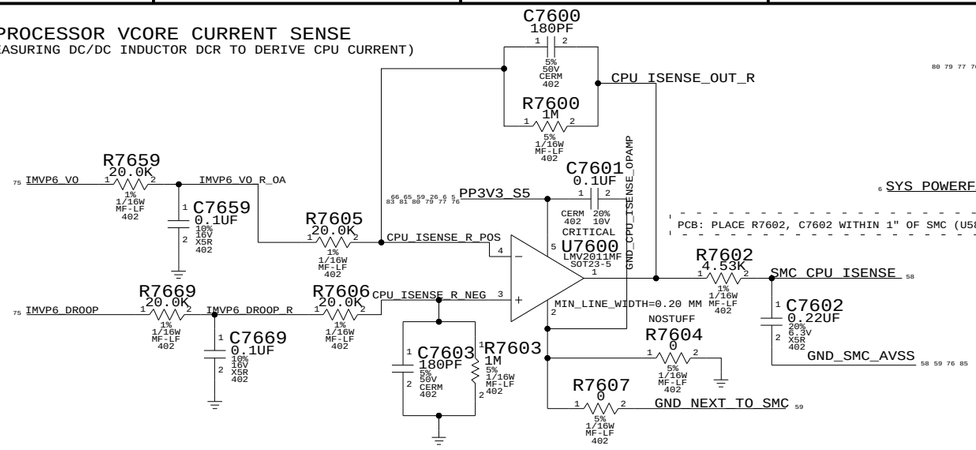
IMVP6 CPU VCore Regulator	
SYNC_MASTER=POWER	SYNC_DATE=07/08/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6949	09
	SCALE: NONE	SHT 75 OF 111	

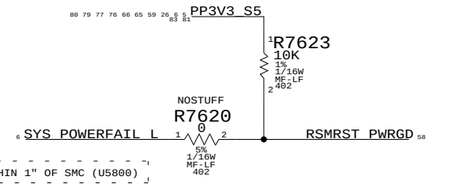
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



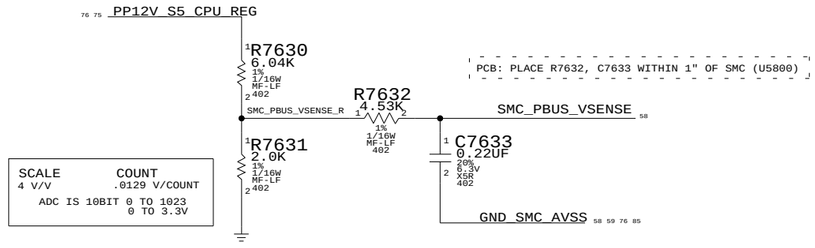
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)



SMC PWRGD PULLUP



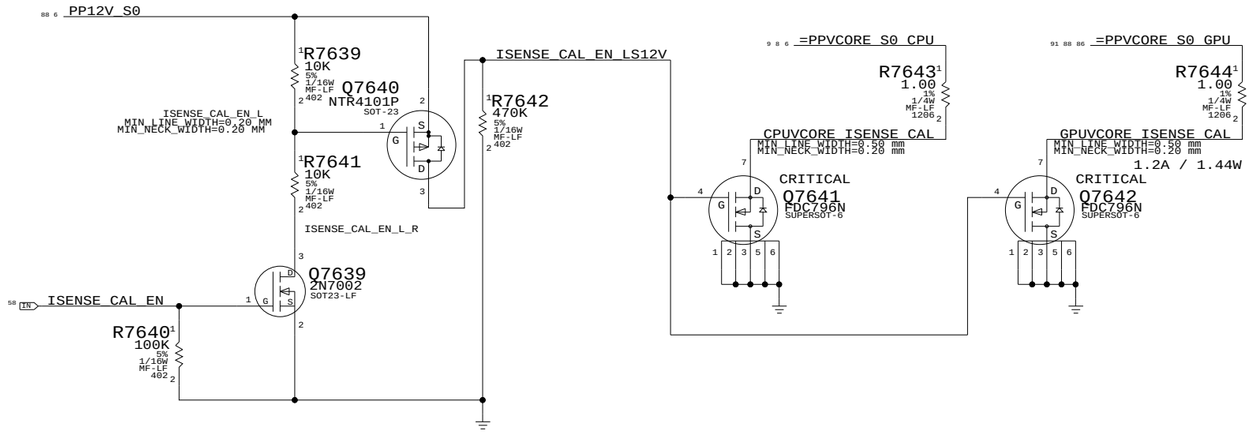
PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



PROCESSOR VCORE SENSE

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

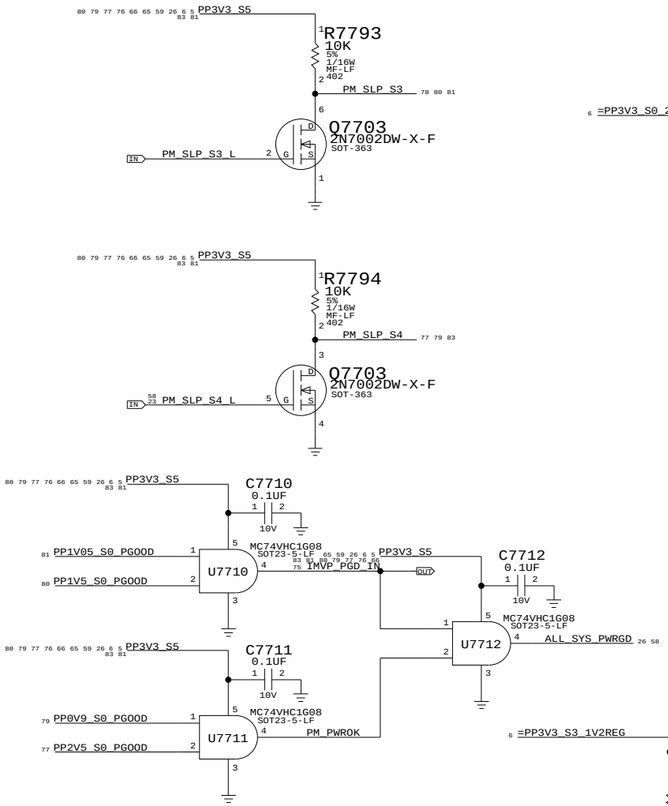


CPU SENSE CIRCUITRIES

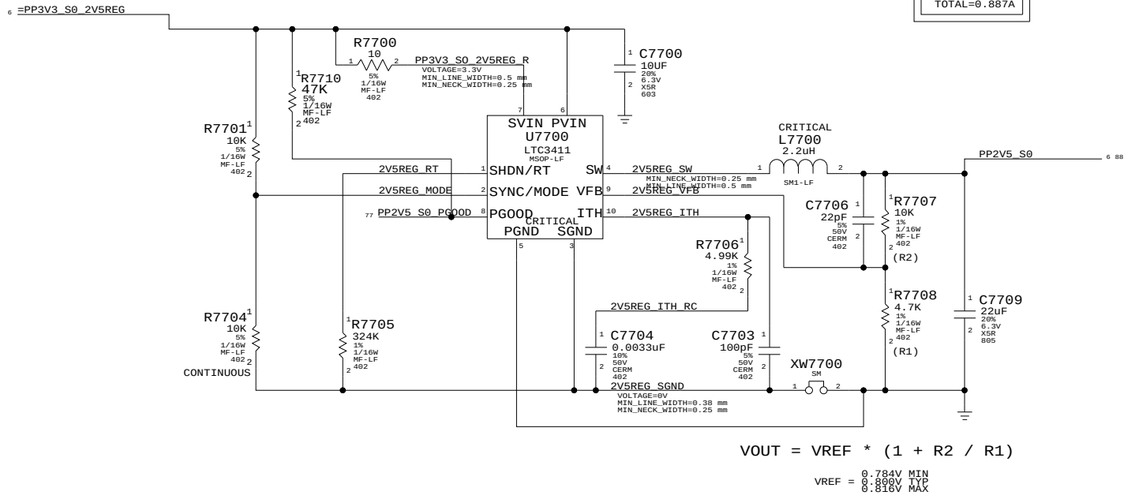
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

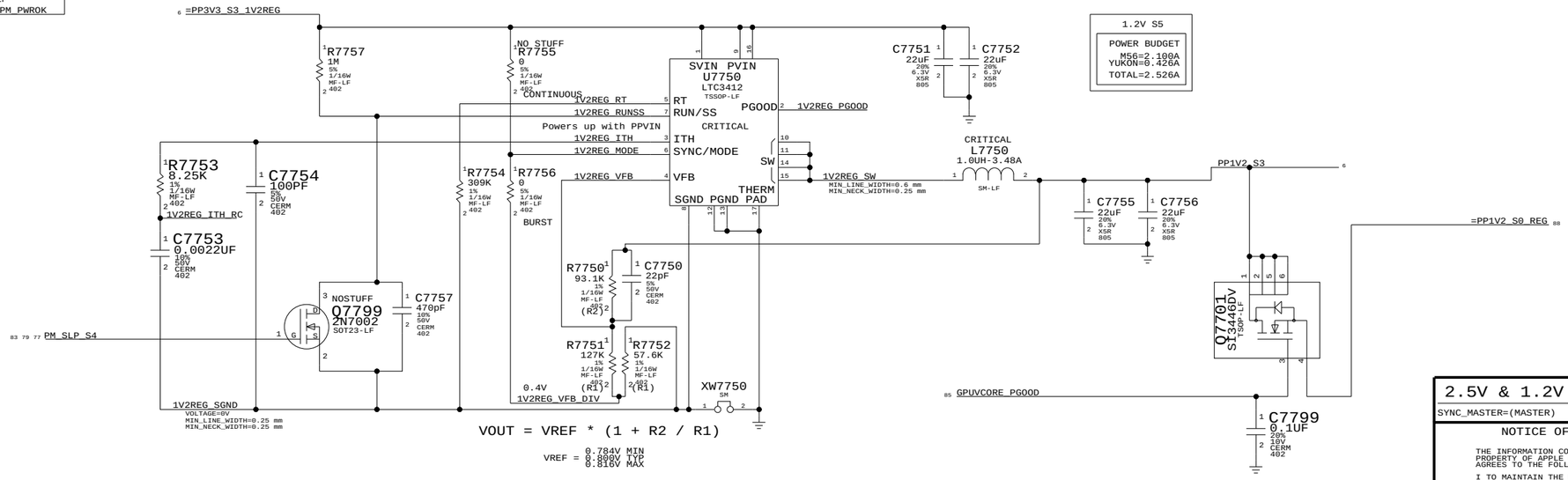
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE NONE	SHT 76 OF 111	



2.5V S0 Regulator



1.2V S3 REGULATOR / 1.2V S0 FET



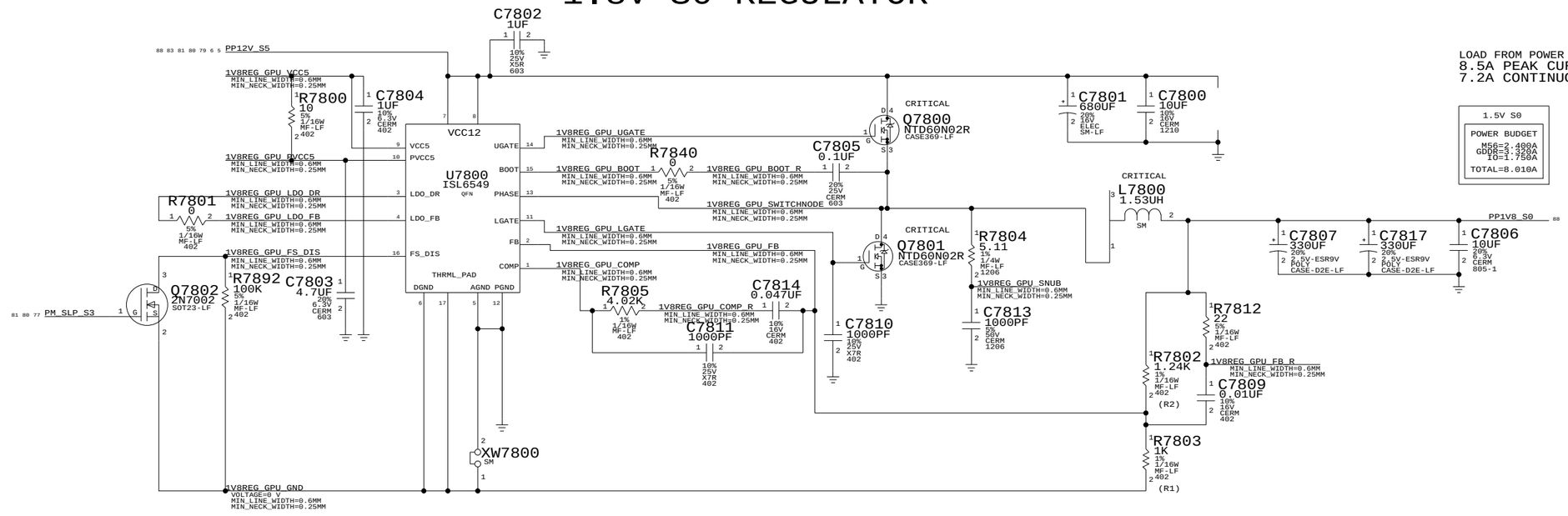
2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	77	111

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0

POWER BUDGET
M56=2.400A
GDDR=3.730A
IO=1.750A
TOTAL=8.010A

VOUT=VREF*(1+R2/R1)

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.8V GDDR REGULATOR

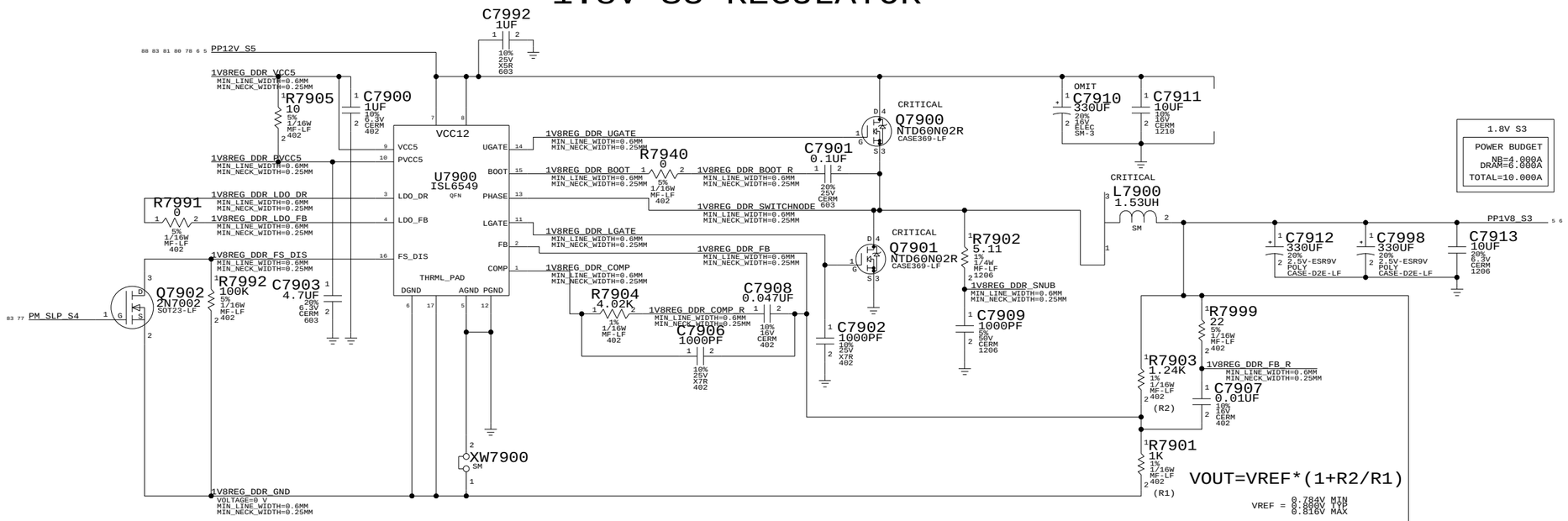
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

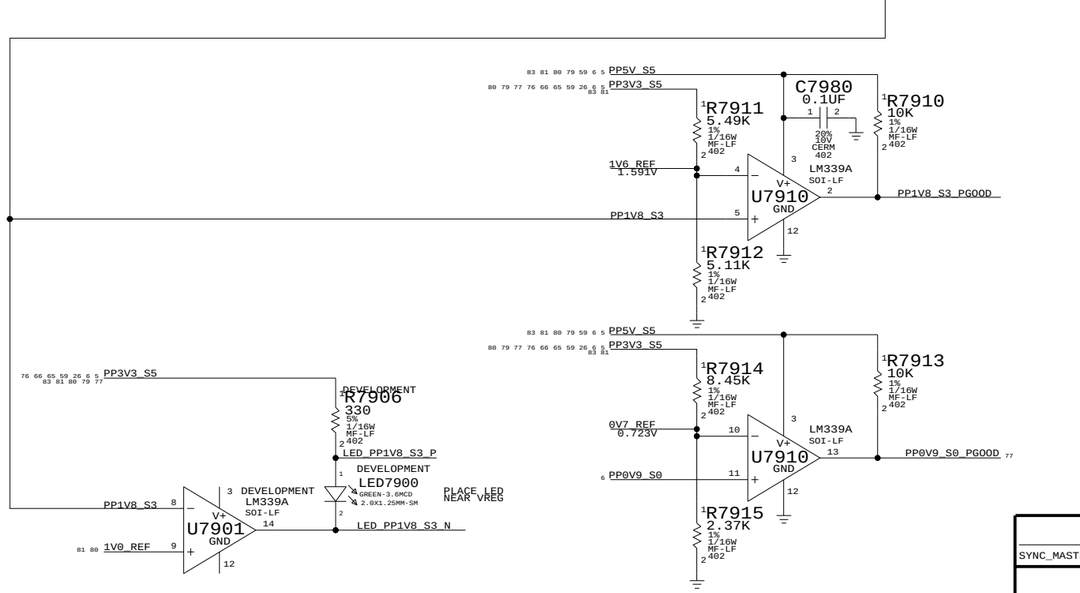
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 78 OF 111	

TRUE

1.8V S3 REGULATOR





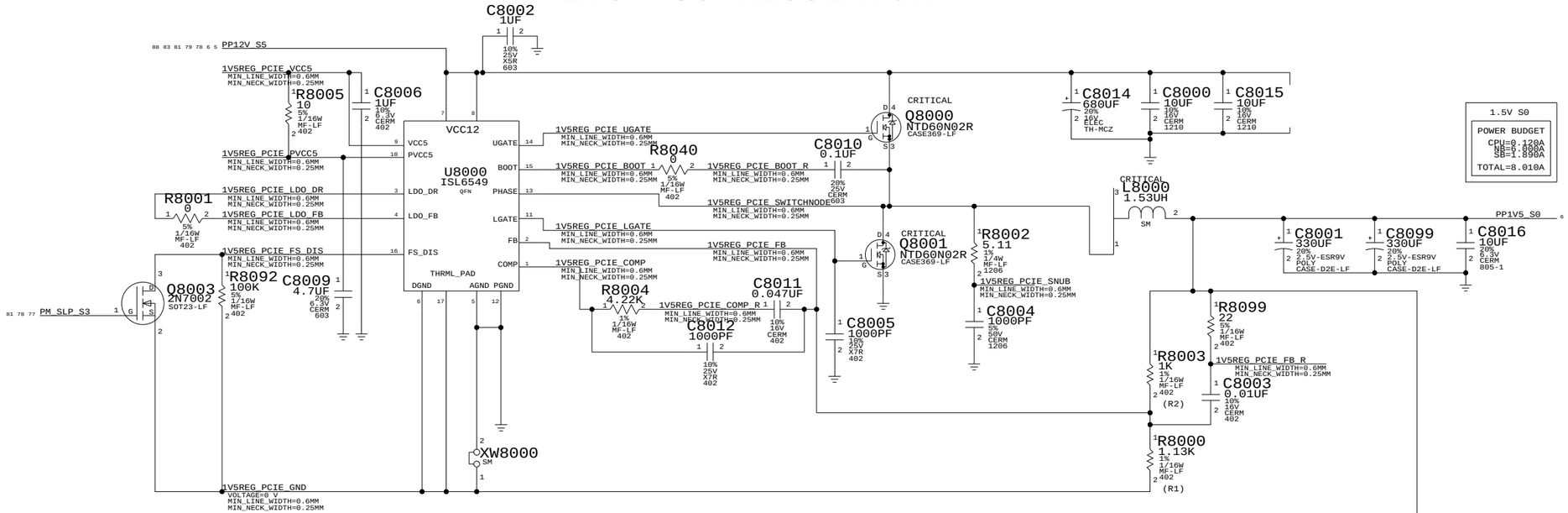
1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 79 OF 111	

1.5V S0 REGULATOR



1.5V Vreg

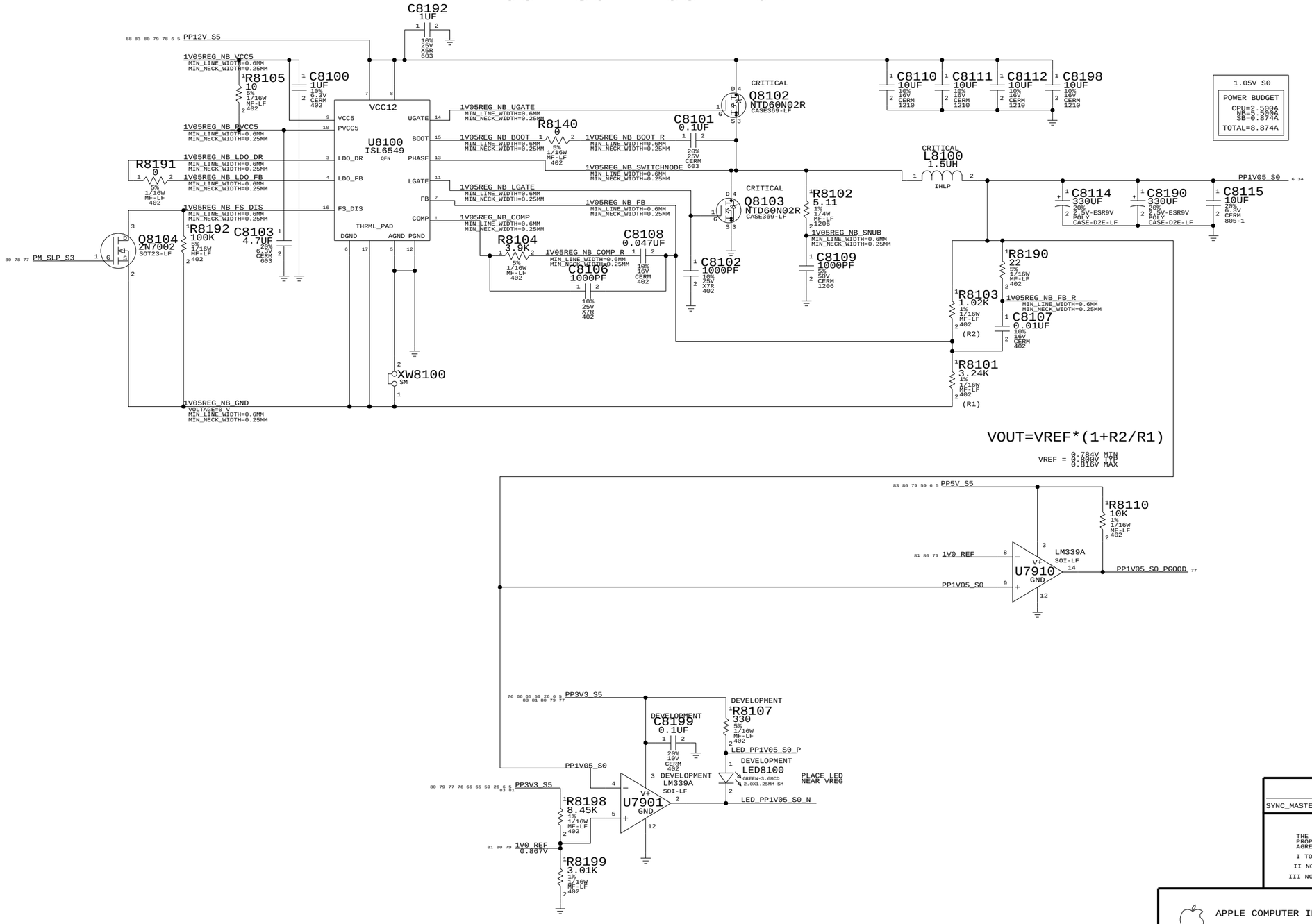
SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE SHT 80 OF 111

1.05V S0 REGULATOR



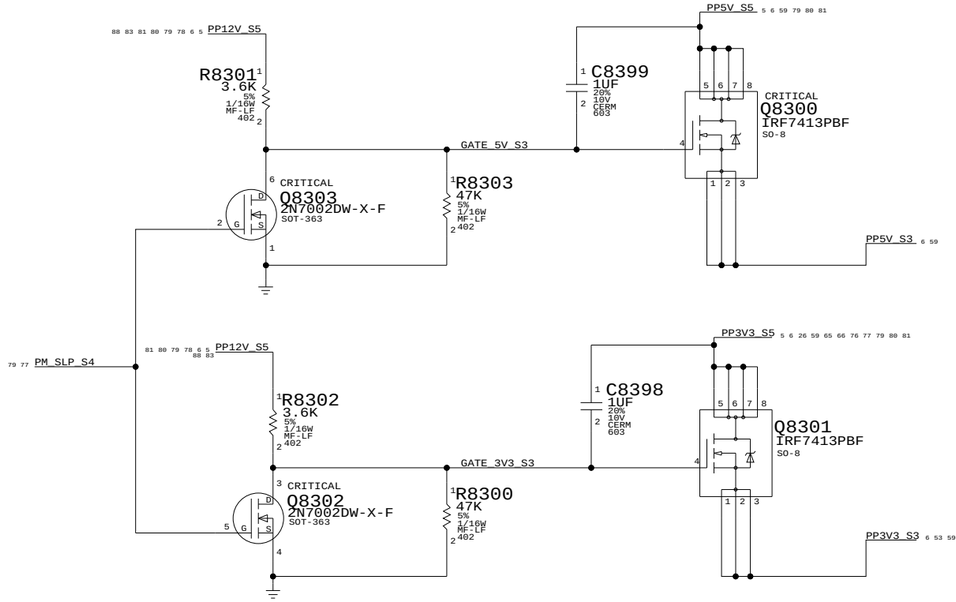
1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE SHT 81 OF 111



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

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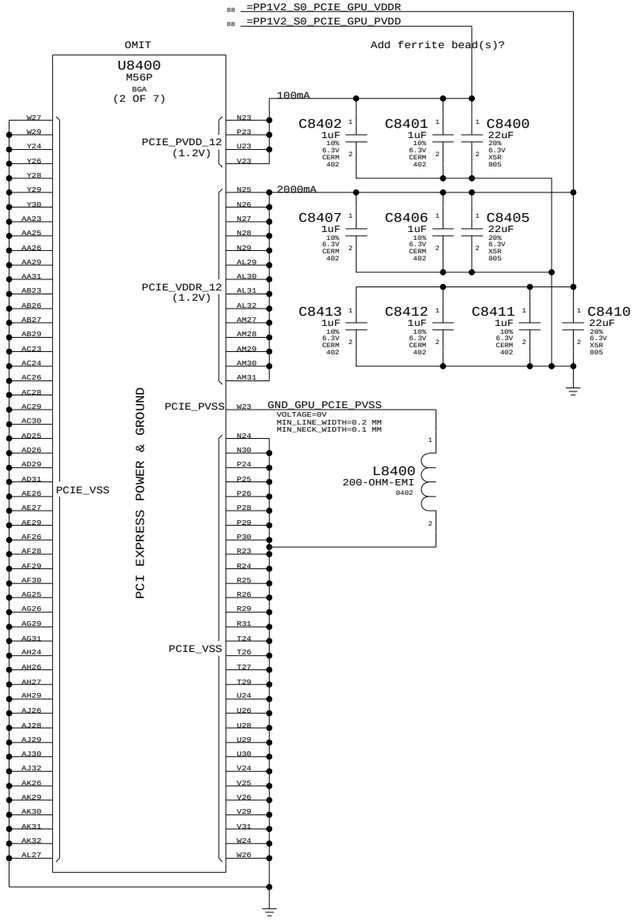
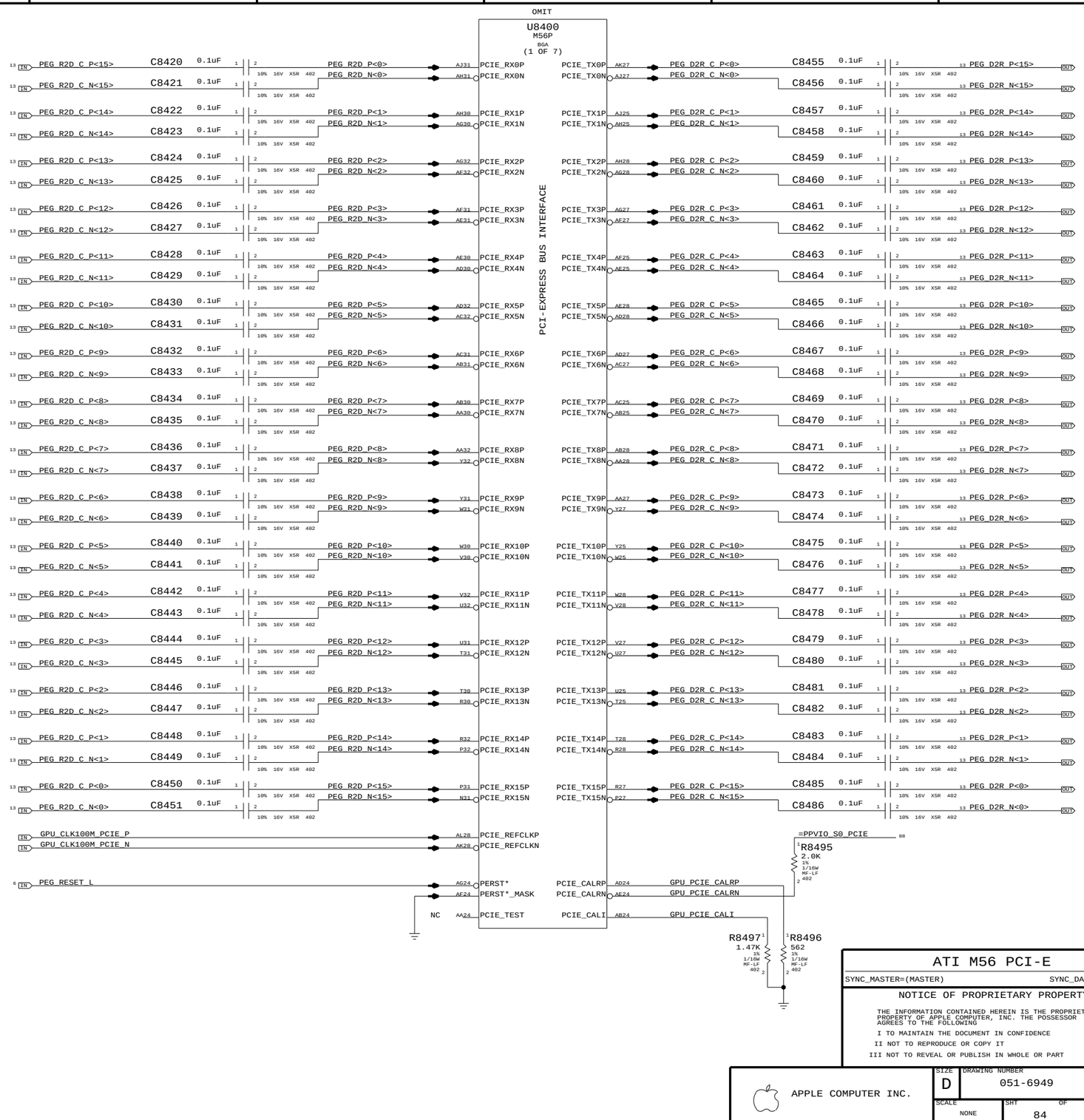
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE SHT 83 OF 111





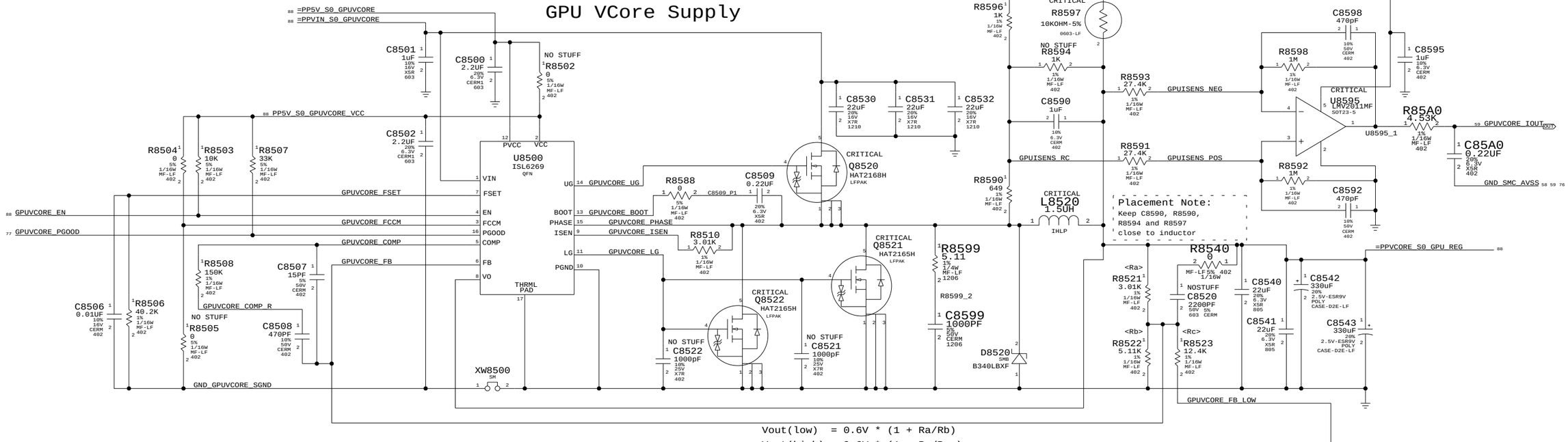
ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 84 OF 111	

GPU VCore Supply

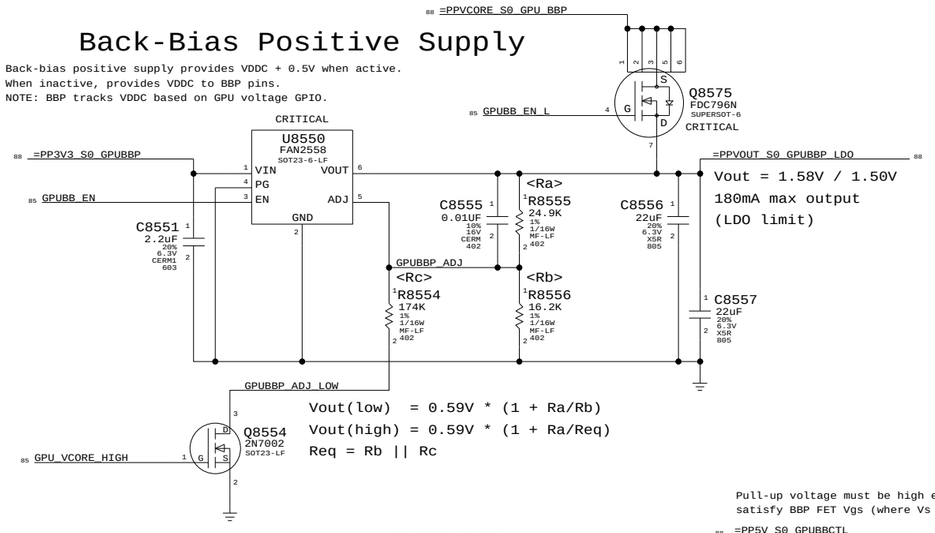


Vout(low) = 0.6V * (1 + Ra/Rb)
Vout(high) = 0.6V * (1 + Ra/Req)
Req = Rb || Rc

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

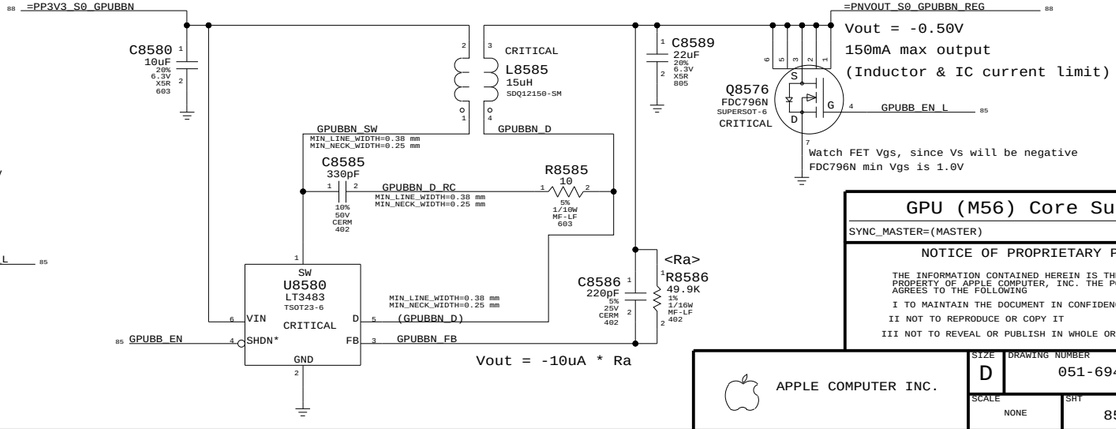


Vout = 1.58V / 1.50V
180mA max output
(LDO limit)

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active.
When inactive, provides VSS to BBN pins.

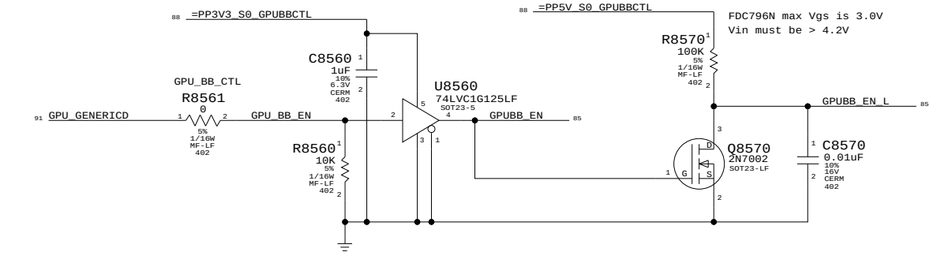


Vout = -0.5V
150mA max output
(Inductor & IC current limit)

Watch FET Vgs, since Vs will be negative
FDC796N min Vgs is 1.0V

Vout = -10uA * Ra

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)



FDC796N max Vgs is 3.0V
Vin must be > 4.2V

=PP3V3_S0_GPU
R8526 100K 5% 1/16W MF-LF 402
R8525 0 5% 1/16W MF-LF 402
GPU_VCORE_HIGH
GPU_VCORE_HIGH_RC
Q8523 2N7002DW-X-F SOT-363
C8523 0.1uF 10% 16V X5R 402
GPU_VCORE_LOW
R8524 10K 5% 1/16W MF-LF 402

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

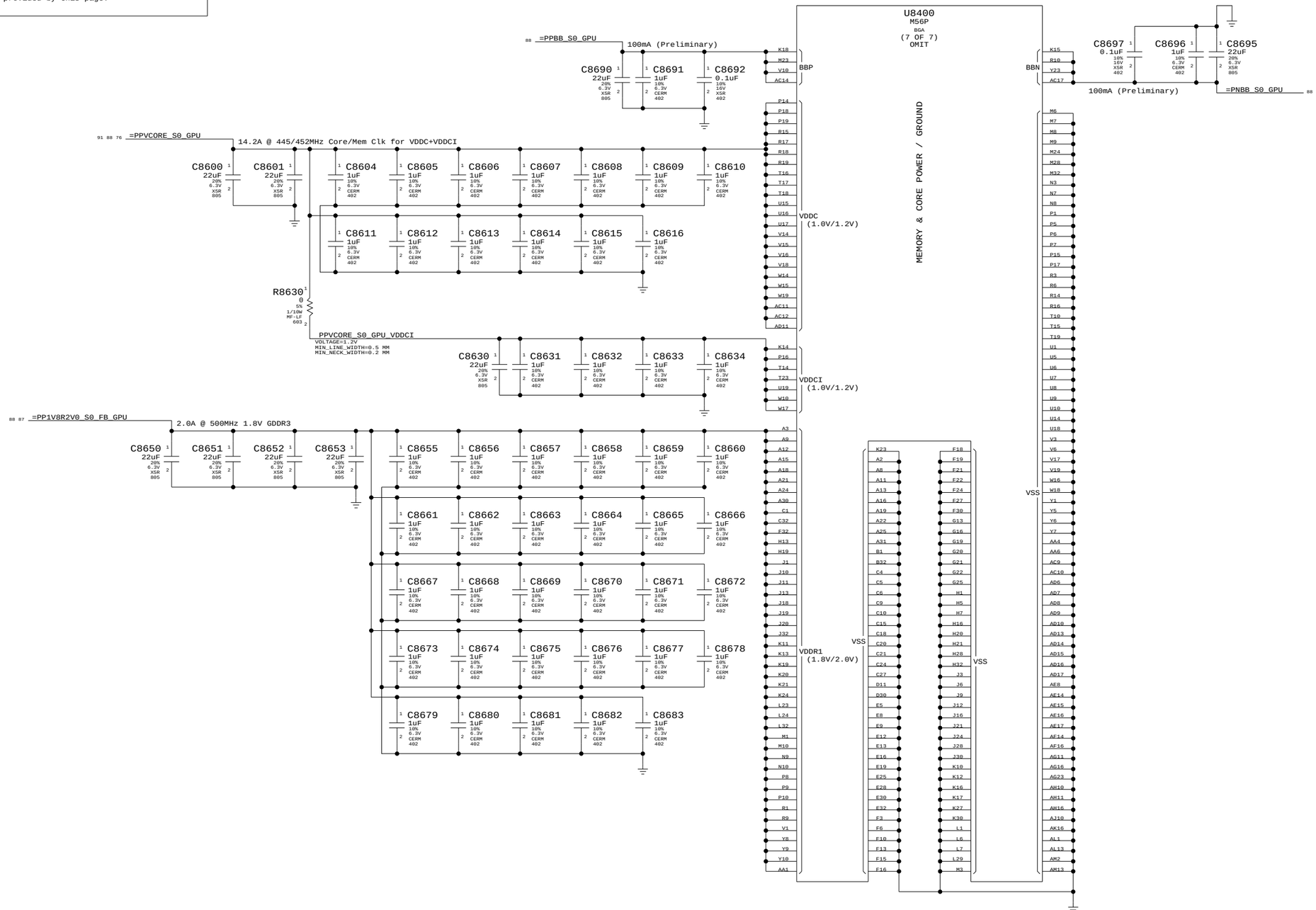
SCALE	SHT	OF
NONE	85	111

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	86	111

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8400
M56P
BGA
(3 OF 7)
MEMORY INTERFACE A
READ STROBE
WRITE STROBE

FB_A_DQ<0>	M31	DQA_0	MAA_0	D26	FB_A_MA<0>	DQMA_0*	H31
FB_A_DQ<1>	M30	DQA_1	MAA_1	F28	FB_A_MA<1>	DQMA_1*	J29
FB_A_DQ<2>	L31	DQA_2	MAA_2	D28	FB_A_MA<2>	DQMA_2*	J26
FB_A_DQ<3>	L30	DQA_3	MAA_3	D25	FB_A_MA<3>	DQMA_3*	G23
FB_A_DQ<4>	H30	DQA_4	MAA_4	E24	FB_A_MA<4>	DQMA_4*	E21
FB_A_DQ<5>	G31	DQA_5	MAA_5	E26	FB_A_MA<5>	DQMA_5*	B15
FB_A_DQ<6>	G30	DQA_6	MAA_6	D27	FB_A_MA<6>	DQMA_6*	D14
FB_A_DQ<7>	F31	DQA_7	MAA_7	F25	FB_A_MA<7>	DQMA_7*	J17
FB_A_DQ<8>	M27	DQA_8	MAA_8	C26	FB_A_MA<8>		
FB_A_DQ<9>	M29	DQA_9	MAA_9	B26	FB_A_MA<9>	QSA_0	J31
FB_A_DQ<10>	L28	DQA_10	MAA_10	D29	FB_A_MA<10>	QSA_1	K29
FB_A_DQ<11>	L27	DQA_11	MAA_11	B27	FB_A_MA<11>	QSA_2	K25
FB_A_DQ<12>	J27	DQA_12	MAA_12	E27	TP_FB_A_MA12	QSA_3	F23
FB_A_DQ<13>	H29	DQA_13	MAA_13	E29	FB_A_BA<2>	QSA_4	D20
FB_A_DQ<14>	G29	DQA_14	MAA_14	B25	FB_A_BA<0>	QSA_5	B16
FB_A_DQ<15>	G27	DQA_15	MAA_15	C25	FB_A_BA<1>	QSA_6	D16
FB_A_DQ<16>	M26	DQA_16				QSA_7	H15
FB_A_DQ<17>	L26	DQA_17					
FB_A_DQ<18>	M25	DQA_18				QSA_0*	K31
FB_A_DQ<19>	L25	DQA_19				QSA_1*	K28
FB_A_DQ<20>	J25	DQA_20				QSA_2*	K26
FB_A_DQ<21>	G28	DQA_21				QSA_3*	G24
FB_A_DQ<22>	H27	DQA_22				QSA_4*	D21
FB_A_DQ<23>	H26	DQA_23				QSA_5*	C16
FB_A_DQ<24>	F26	DQA_24				QSA_6*	D15
FB_A_DQ<25>	G26	DQA_25				QSA_7*	J15
FB_A_DQ<26>	H25	DQA_26					
FB_A_DQ<27>	H24	DQA_27				CLKA0	D31
FB_A_DQ<28>	H23	DQA_28				CLKA0*	E31
FB_A_DQ<29>	H22	DQA_29					
FB_A_DQ<30>	J23	DQA_30				CSA0_0*	B29
FB_A_DQ<31>	J22	DQA_31				CSA0_1*	C28 NC
FB_A_DQ<32>	E23	DQA_32					
FB_A_DQ<33>	D22	DQA_33				CKEA0	B30
FB_A_DQ<34>	D23	DQA_34				RASA0*	B28
FB_A_DQ<35>	E22	DQA_35				CASA0*	C29
FB_A_DQ<36>	E20	DQA_36				WEA0*	B31
FB_A_DQ<37>	F20	DQA_37				ODTA0	F29
FB_A_DQ<38>	D19	DQA_38					
FB_A_DQ<39>	D18	DQA_39				CLKA1	B20
FB_A_DQ<40>	B19	DQA_40				CLKA1*	C19
FB_A_DQ<41>	B18	DQA_41					
FB_A_DQ<42>	C17	DQA_42				CSA1_0*	B23
FB_A_DQ<43>	B17	DQA_43				CSA1_1*	C23 NC
FB_A_DQ<44>	C14	DQA_44					
FB_A_DQ<45>	B14	DQA_45				CKEA1	C22
FB_A_DQ<46>	C13	DQA_46				RASA1*	B24
FB_A_DQ<47>	B13	DQA_47				CASA1*	B22
FB_A_DQ<48>	D17	DQA_48				WEA1*	B21
FB_A_DQ<49>	E18	DQA_49				ODTA1	D24
FB_A_DQ<50>	E17	DQA_50					
FB_A_DQ<51>	F17	DQA_51					
FB_A_DQ<52>	E15	DQA_52					
FB_A_DQ<53>	E14	DQA_53					
FB_A_DQ<54>	F14	DQA_54					
FB_A_DQ<55>	D13	DQA_55					
FB_A_DQ<56>	H18	DQA_56					
FB_A_DQ<57>	H17	DQA_57					
FB_A_DQ<58>	G18	DQA_58					
FB_A_DQ<59>	G17	DQA_59					
FB_A_DQ<60>	G15	DQA_60					
FB_A_DQ<61>	G14	DQA_61					
FB_A_DQ<62>	H14	DQA_62					
FB_A_DQ<63>	J14	DQA_63					

=PP1V8R2V0_S0_FB_GPU
R8710 40.2 1% 1/16W MF-LF 402
R8712 40.2 1% 1/16W MF-LF 402
R8711 100 1% 1/16W MF-LF 402
C8711 0.1uF 10% 16V X5R 402
R8713 100 1% 1/16W MF-LF 402
C8713 0.1uF 10% 16V X5R 402
GPU_MVREFD0 → MVREFD_0
GPU_MVREFS0 → MVREFS_0
VDDRH0 (1.8V/2.0V)
VSSRH0

=PP1V8R2V0_S0_FB_GPU
L8715 FERR-220-OHM 0402
PP1V8R2V0_S0_GPU_VDDRH0
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
C8715 1uF 10% 6.3V CERM 402
C8716 1uF 10% 6.3V CERM 402
XW8715 SM
GND_GPU_VSSRH0
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V

OMIT
U8400
M56P
BGA
(4 OF 7)
MEMORY INTERFACE B
READ STROBE
WRITE STROBE

FB_B_DQ<0>	B12	DQB_0	MAB_0	G4	FB_B_MA<0>	DQMB_0*	B8
FB_B_DQ<1>	C12	DQB_1	MAB_1	E6	FB_B_MA<1>	DQMB_1*	D9
FB_B_DQ<2>	B11	DQB_2	MAB_2	E4	FB_B_MA<2>	DQMB_2*	G9
FB_B_DQ<3>	C11	DQB_3	MAB_3	H4	FB_B_MA<3>	DQMB_3*	K7
FB_B_DQ<4>	C8	DQB_4	MAB_4	J5	FB_B_MA<4>	DQMB_4*	M5
FB_B_DQ<5>	B7	DQB_5	MAB_5	G5	FB_B_MA<5>	DQMB_5*	V2
FB_B_DQ<6>	C7	DQB_6	MAB_6	F4	FB_B_MA<6>	DQMB_6*	W4
FB_B_DQ<7>	B6	DQB_7	MAB_7	H6	FB_B_MA<7>	DQMB_7*	T9
FB_B_DQ<8>	F12	DQB_8	MAB_8	G3	FB_B_MA<8>		
FB_B_DQ<9>	D12	DQB_9	MAB_9	G2	FB_B_MA<9>	QSB_0	B9
FB_B_DQ<10>	E11	DQB_10	MAB_10	D4	FB_B_MA<10>	QSB_1	D10
FB_B_DQ<11>	F11	DQB_11	MAB_11	F2	FB_B_MA<11>	QSB_2	H10
FB_B_DQ<12>	F9	DQB_12	MAB_12	F5	TP_FB_B_MA12	QSB_3	K6
FB_B_DQ<13>	D8	DQB_13	MAB_13	D5	FB_B_BA<2>	QSB_4	N4
FB_B_DQ<14>	D7	DQB_14	MAB_14	H2	FB_B_BA<0>	QSB_5	U2
FB_B_DQ<15>	F7	DQB_15	MAB_15	H3	FB_B_BA<1>	QSB_6	U4
FB_B_DQ<16>	G12	DQB_16				QSB_7	V8
FB_B_DQ<17>	G11	DQB_17					
FB_B_DQ<18>	H12	DQB_18				QSB_0*	B10
FB_B_DQ<19>	H11	DQB_19				QSB_1*	E10
FB_B_DQ<20>	H9	DQB_20				QSB_2*	G10
FB_B_DQ<21>	E7	DQB_21				QSB_3*	J7
FB_B_DQ<22>	F8	DQB_22				QSB_4*	M4
FB_B_DQ<23>	G8	DQB_23				QSB_5*	U3
FB_B_DQ<24>	G6	DQB_24				QSB_6*	V4
FB_B_DQ<25>	G7	DQB_25				QSB_7*	V9
FB_B_DQ<26>	H8	DQB_26					
FB_B_DQ<27>	J8	DQB_27				CLKB0	B4
FB_B_DQ<28>	K8	DQB_28				CLKB0*	B5
FB_B_DQ<29>	L8	DQB_29					
FB_B_DQ<30>	K9	DQB_30				CSB0_0*	D2
FB_B_DQ<31>	L9	DQB_31				CSB0_1*	E3 NC
FB_B_DQ<32>	K5	DQB_32					
FB_B_DQ<33>	L4	DQB_33				CKEB0	C2
FB_B_DQ<34>	K4	DQB_34				RASB0*	E2
FB_B_DQ<35>	L5	DQB_35				CASB0*	D3
FB_B_DQ<36>	N5	DQB_36				WEB0*	B2
FB_B_DQ<37>	N6	DQB_37				ODTB0	D6
FB_B_DQ<38>	P4	DQB_38					
FB_B_DQ<39>	R4	DQB_39				CLKB1	N2
FB_B_DQ<40>	P2	DQB_40				CLKB1*	P3
FB_B_DQ<41>	R2	DQB_41					
FB_B_DQ<42>	T3	DQB_42				CSB1_0*	K2
FB_B_DQ<43>	T2	DQB_43				CSB1_1*	K3 NC
FB_B_DQ<44>	W3	DQB_44					
FB_B_DQ<45>	W2	DQB_45				CKEB1	L3
FB_B_DQ<46>	Y3	DQB_46				RASB1*	J2
FB_B_DQ<47>	Y2	DQB_47				CASB1*	L2
FB_B_DQ<48>	T4	DQB_48				WEB1*	M2
FB_B_DQ<49>	R5	DQB_49				ODTB1	J4
FB_B_DQ<50>	T5	DQB_50					
FB_B_DQ<51>	T6	DQB_51					
FB_B_DQ<52>	V5	DQB_52					
FB_B_DQ<53>	W5	DQB_53					
FB_B_DQ<54>	W6	DQB_54					
FB_B_DQ<55>	Y4	DQB_55					
FB_B_DQ<56>	R8	DQB_56					
FB_B_DQ<57>	T8	DQB_57					
FB_B_DQ<58>	R7	DQB_58					
FB_B_DQ<59>	T7	DQB_59					
FB_B_DQ<60>	V7	DQB_60					
FB_B_DQ<61>	W7	DQB_61					
FB_B_DQ<62>	W8	DQB_62					
FB_B_DQ<63>	W9	DQB_63					

=PP1V8R2V0_S0_FB_GPU
R8720 40.2 1% 1/16W MF-LF 402
R8722 40.2 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
C8721 0.1uF 10% 16V X5R 402
R8723 100 1% 1/16W MF-LF 402
C8723 0.1uF 10% 16V X5R 402
GPU_MVREFD1 → MVREFD_1
GPU_MVREFS1 → MVREFS_1
PP1V8R2V0_S0_GPU_VDDRH1 → VDDRH1 (1.8V/2.0V)
VSSRH1
GPU_TEST_MCLK → TEST_MCLK
GPU_TEST_YCLK → TEST_YCLK
GPU_MEMTEST → MEMTEST
DRAM_RST → FB_DRAM_RST
R8731 4.7K 5% 1/16W MF-LF 402
R8730 4.7K 5% 1/16W MF-LF 402
R8732 243 1% 1/16W MF-LF 402
R8733 4.7K 5% 1/16W MF-LF 402

=PP1V8R2V0_S0_FB_GPU
L8725 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
C8725 1uF 10% 6.3V CERM 402
C8726 1uF 10% 6.3V CERM 402
XW8725 SM
GND_GPU_VSSRH1
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=0V

ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 87 OF 111	

"S0" GPU RAILS

ONLY ON IN RUN

59 PP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVCORE_S0_GPU_REG 85
=PPVCORE_S0_GPU 76 86 91
=PPVCORE_S0_GPU_BBP 85

85 PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V
10 1 R8800 2 603 MF-LF 5% 1/10W
=PP5V_S0_GPUVCORE 85
GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PP1V2_S0_PCIE_GPU_VDDR 84
=PP1V2_S0_PCIE_GPU_PVDD 84
=PPVIO_S0_PCIE 84
=PP1V2_S0_REG 77
=PP1V2_S0_GPU_VDDPLL 91

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVOUT_S0_GPUBBP_LDO 85
=PPBB_S0_GPU 86

PNBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=0V
=PNVOUT_S0_GPUBBN_REG 85
=PNBB_S0_GPU 86

76 61 59 41 26 10 6 PP3V3_S0
=PP3V3_S0_GPUBBP 85
=PP3V3_S0_GPUBBCTL 85
=PP3V3_DDC_DVI 97
=PP3V3_S0_LCD 94
=PP3V3_S0_GPU_VDDR3 88 91
=PP3V3_S0_GPU 85 91 93
=PP3V3_S0_GPUBBN 85
=PP3V3_S0_GPU_CLOCKS
=PP3V3_DDC_LCD 94
=PP3V3_GPU 94

77 6 PP2V5_S0
=PP2V5_S0_GPU_PVDD 91
=PP2V5_S0_GPU_VDD25 91
=PP2V5_S0_GPU_VDDC_CT 91
=PP2V5_S0_GPU 93

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V
=PP1V8_S0_FB_VDD 89 90
=PP1V8R3V3_S0_GPU_VDDR4 91
=PP1V8R3V3_S0_GPU_VDDR5 91
=PP1V8_S0_FB_VDDQ 89 90
PP1V8_S0 78
=PP1V8R2V0_S0_FB_GPU 86 87

83 81 80 79 78 6 5 PP12V_S5
=PPVIN_S0_GPUVCORE 85

76 6 PP12V_S0
=PP12V_GPU 94

97 94 75 6 PP5V_S0
=PP5V_S0_GPUBBCTL 85
=PP5V_S0_DVI_DDC 97
=PP5V_S0_GPUISENS 85

85 GPUVCORE_EN
33 1 R8801 2 402 MF-LF 5% 1/16W
PM_SLP_S3_L 6 23 58 77 79

87 FB_DRAM_RST
MAKE_BASE=TRUE
DRAM_RST 5 89 90

M56 GPIOS

=PP3V3_S0_GPU_VDDR3 88 91

94 91 GPU_GPIO_0
10K 1 R8813 2 402 MF-LF 5% 1/16W
GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
10K 1 R8802 2 402 MF-LF 5% 1/16W
GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
NOSTUFF R8803 10K 1 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_3
NOSTUFF R8804 10K 1 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_4
NOSTUFF R8805 10K 1 2 402 MF-LF 5% 1/16W
GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
10K 1 R8806 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_6
NOSTUFF R8807 10K 1 2 402 MF-LF 5% 1/16W

TP_GPU_GPIO_7
MAKE_BASE=TRUE
GPU_GPIO_7 91

91 GPU_GPIO_8
NOSTUFF R8808 10K 1 2 402 MF-LF 5% 1/16W

NC_GPU_GPIO_10
MAKE_BASE=TRUE
GPU_GPIO_10 91

91 GPU_GPIO_9
NOSTUFF R8809 10K 1 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_13
NOSTUFF R8812 10K 1 2 402 MF-LF 5% 1/16W
ATI_FB_256M

91 GPU_GPIO_12
10K 1 R8810 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_11
NOSTUFF R8811 10K 1 2 402 MF-LF 5% 1/16W
GPIO 9,13,12,11 = ROM ID CFG
INTERNAL PULL DOWN
0010 = 256 M APERATURE SIZE

ATI_FB_256M
91 GPU_GPIO_24
10K 1 R8830 2 402 MF-LF 5% 1/16W

ATI_FB_HYNIX
91 GPU_GPIO_27
10K 1 R8831 2 402 MF-LF 5% 1/16W

91 GPU_GPIO_28
10K 1 R8832 2 402 MF-LF 5% 1/16W

TMDS_PANEL
91 GPU_GPIO_29
10K 1 R8833 2 402 MF-LF 5% 1/16W

85 GPU_VCORE_LOW
MAKE_BASE=TRUE
GPU_GPIO_15 91
10K 1 R8850 2 402 MF-LF 5% 1/16W
GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
MAKE_BASE=TRUE
GPU_GPIO_14 91

TP_GPU_GPIO_17
MAKE_BASE=TRUE
GPU_GPIO_17 91

TP_GPU_VGA_R
MAKE_BASE=TRUE
GPU_VGA_R 93

TP_GPU_VGA_G
MAKE_BASE=TRUE
GPU_VGA_G 93

TP_GPU_VGA_B
MAKE_BASE=TRUE
GPU_VGA_B 93

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE
GPU_VGA_HSYNC 93

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE
GPU_VGA_VSYNC 93

TP_GPU_TV_Y
MAKE_BASE=TRUE
GPU_TV_Y 93

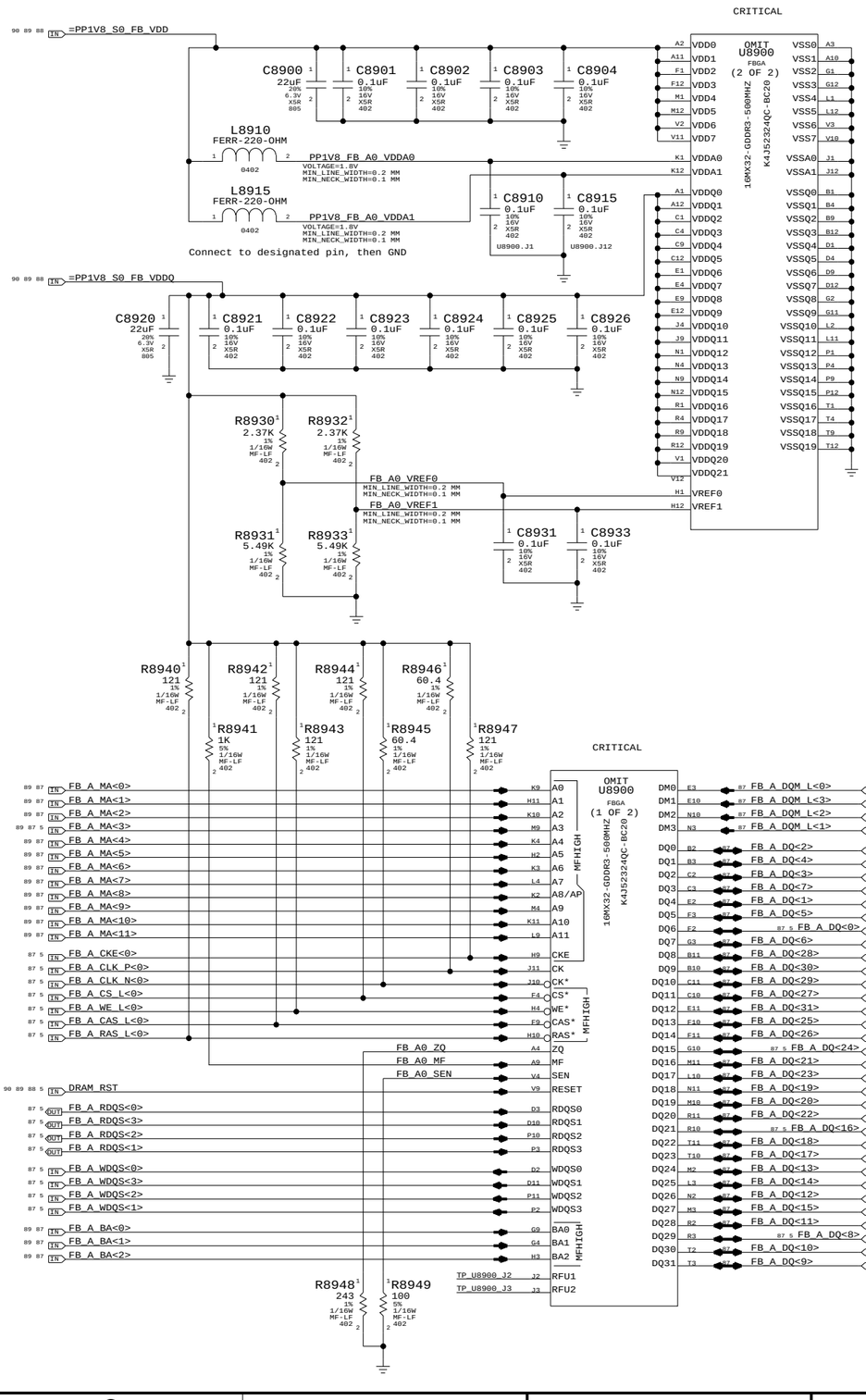
TP_GPU_TV_COMP
MAKE_BASE=TRUE
GPU_TV_COMP 93

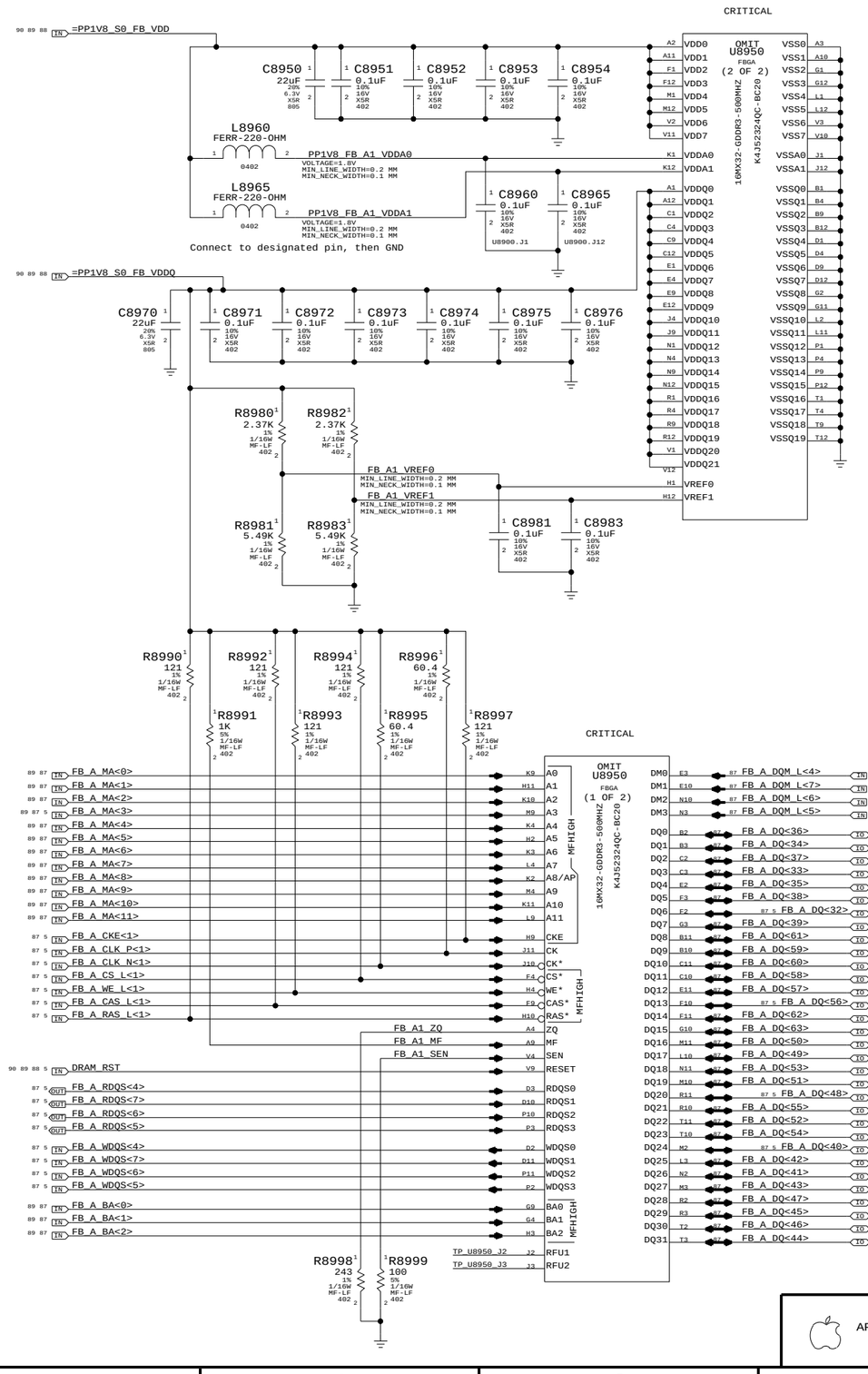
TP_GPU_TV_C
MAKE_BASE=TRUE
GPU_TV_C 93

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE
GPU_DDC_B_CLK 93

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE
GPU_DDC_B_DATA 93

GPU MISC





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

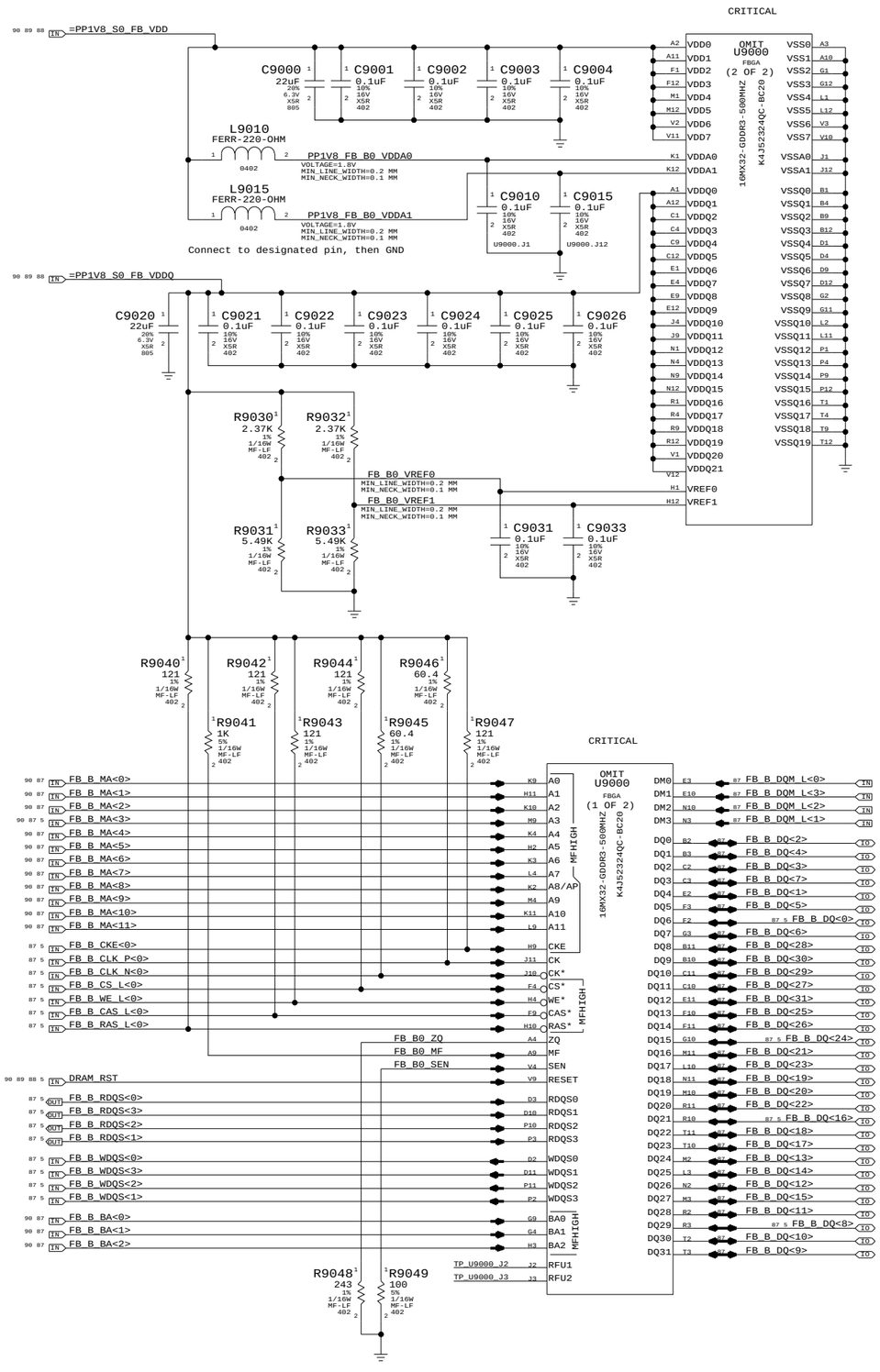
BOM options provided by this page:
(NONE)

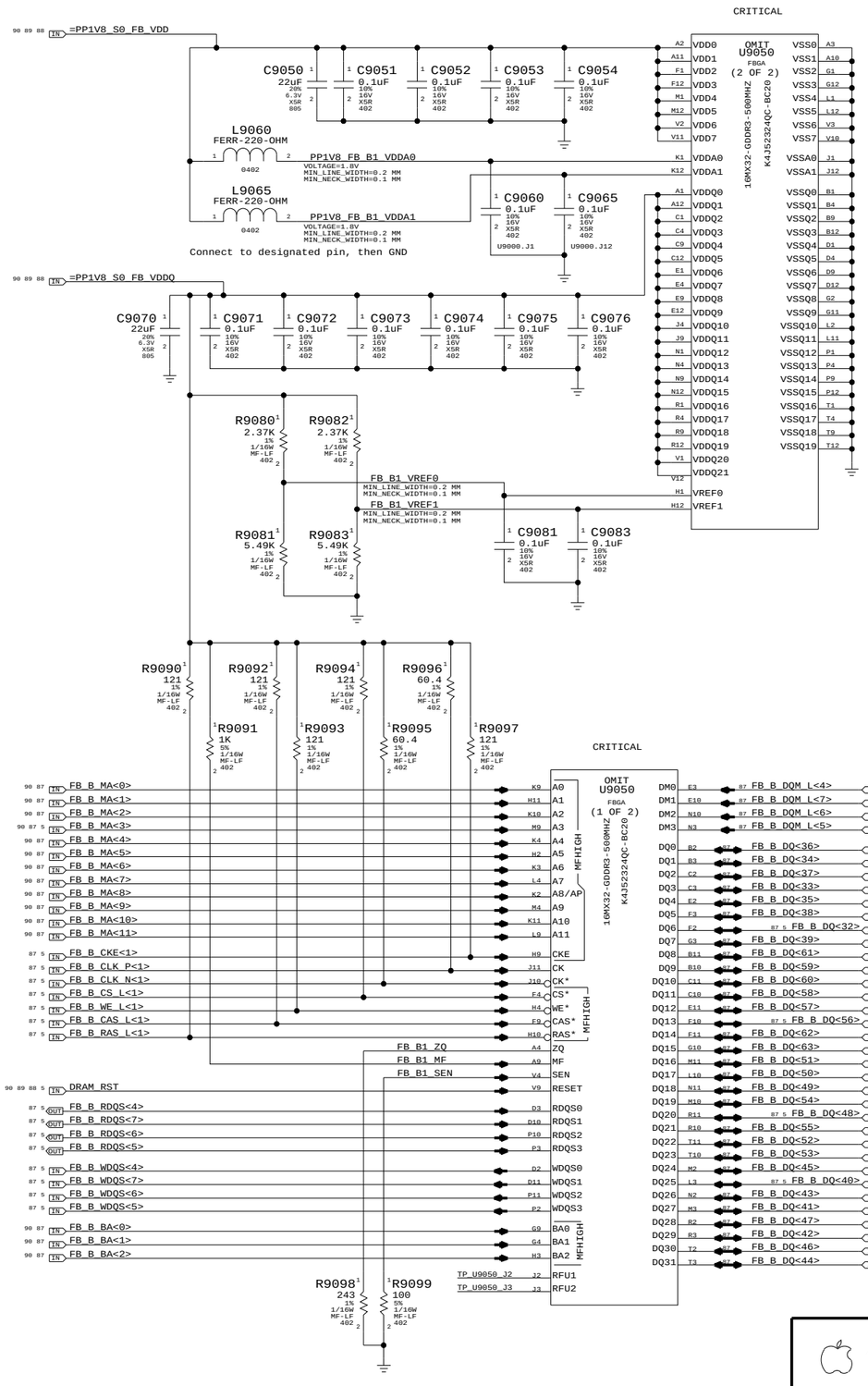
GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 89 OF 111	





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

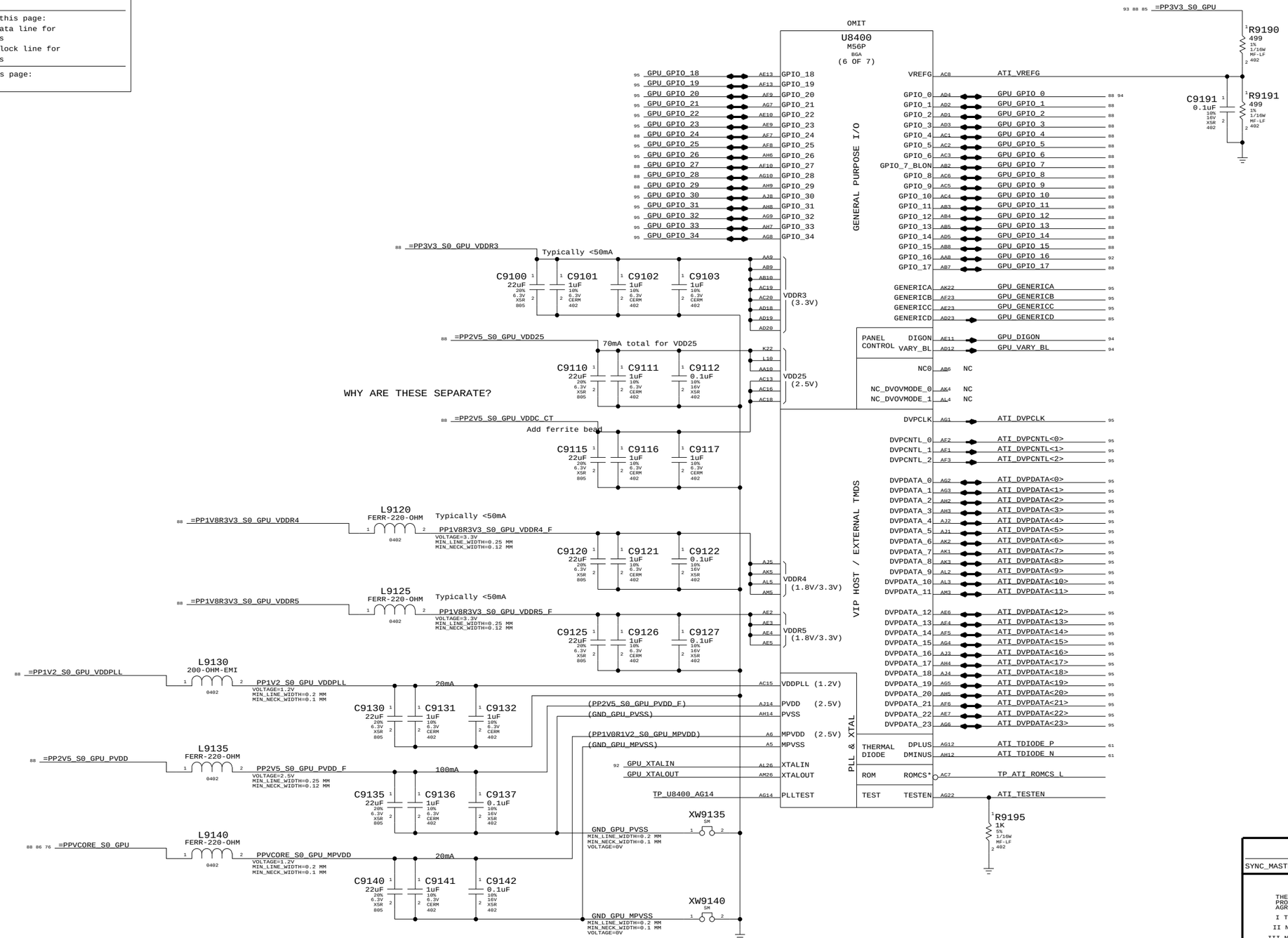
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 90 OF 111	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

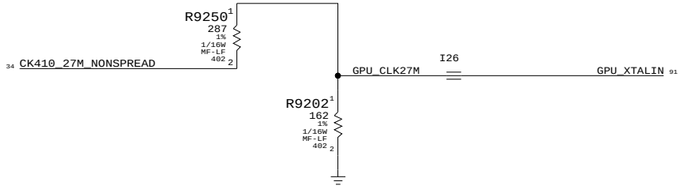
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 91 OF 111	

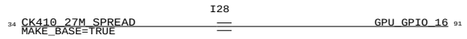
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8





GPU CLOCKS

SYNC_MASTER=BOZEMAN
SYNC_DATE=05/21/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	92	111

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents on this page: 605mA

88 =PP2V5_S0_GPU

L9300 FERR-220-OHM 0402
PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=2.5V
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=0V
20mA peak
C9300 22uF 20% 6.3V X5R 805
C9301 1uF 10% 6.3V CERM 402
C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402
PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=0V
150mA peak
C9305 22uF 20% 6.3V X5R 805
C9306 1uF 10% 6.3V CERM 402
C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402
PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=0V
XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
65mA peak
C9310 22uF 20% 6.3V X5R 805
C9311 1uF 10% 6.3V CERM 402
C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402
PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
20mA peak
C9315 22uF 20% 6.3V X5R 805
C9316 1uF 10% 6.3V CERM 402
C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402
PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=2.5V
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
130mA peak
C9320 22uF 20% 6.3V X5R 805
C9321 1uF 10% 6.3V CERM 402
C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402
PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
20mA peak
C9325 22uF 20% 6.3V X5R 805
C9326 1uF 10% 6.3V CERM 402
C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402
PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=0V
20mA peak
C9330 22uF 20% 6.3V X5R 805
C9331 1uF 10% 6.3V CERM 402
C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402
PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=2.5V
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
200mA peak
C9340 22uF 20% 6.3V X5R 805
C9345 22uF 20% 6.3V X5R 805
C9341 1uF 10% 6.3V CERM 402
C9342 0.1uF 10% 16V X5R 402
C9346 0.1uF 10% 16V X5R 402
C9347 0.1uF 10% 16V X5R 402

OMIT

U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR
- AL25, AM25 AVDD (2.5V)
- AJ24, AK25 AVSS
- AK23 AVSSQ

DAC (CRT)
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- 93 ATI_RSET → AL22 RSET

DAC2 (TV/CRT2)
- AL16, AM16 A2VDD (2.5V)
- AL17, AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- 93 ATI_R2SET → AK14 R2SET

LVDS
- AE19 LPVDD (2.5V)
- AE18 LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AE19, AE20 LVDDR (2.5V)
- AE17, AF22, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- 97 GPU_HPD → AF11 HPD1

TMDS outputs:
- AM9 TXCP → 97 TMDS_CLK_P OUT
- AL9 TXCM → 97 TMDS_CLK_N OUT
- AL10 TX0P → 97 TMDS_DATA_P<0> OUT
- AK10 TX0M → 97 TMDS_DATA_N<0> OUT
- AM11 TX1P → 97 TMDS_DATA_P<1> OUT
- AL11 TX1M → 97 TMDS_DATA_N<1> OUT
- AM12 TX2P → 97 TMDS_DATA_P<2> OUT
- AL12 TX2M → 97 TMDS_DATA_N<2> OUT
- AJ9 TX3P → 95 TMDS_DATA_P<3> OUT
- AK9 TX3M → 95 TMDS_DATA_N<3> OUT
- AJ11 TX4P → 95 TMDS_DATA_P<4> OUT
- AK11 TX4M → 95 TMDS_DATA_N<4> OUT
- AJ12 TX5P → 95 TMDS_DATA_P<5> OUT
- AK12 TX5M → 95 TMDS_DATA_N<5> OUT

DAC outputs:
- R AK24 → 88 GPU_VGA_R OUT
- G AM24 → 88 GPU_VGA_G OUT
- B AL24 → 88 GPU_VGA_B OUT
- HSYNC AJ23 → 88 GPU_VGA_HSYNC OUT
- VSYNC AJ22 → 88 GPU_VGA_VSYNC OUT

DAC2 outputs:
- R2 AK15 → 97 GPU_R2 OUT
- G2 AM15 → 97 GPU_G2 OUT
- B2 AL15 → 97 GPU_B2 OUT
- H2SYNC AF15 → 97 GPU_H2SYNC OUT
- V2SYNC AG15 → 97 GPU_V2SYNC OUT
- Y AJ15 → 88 GPU_TV_Y OUT
- C AJ13 → 88 GPU_TV_C OUT
- COMP AH15 → 88 GPU_TV_COMP OUT

LVDS outputs:
- TXCLK_UP AJ21 → 94 LVDS_U_CLK_P OUT
- TXCLK_UN AK21 → 94 LVDS_U_CLK_N OUT
- TXOUT_U0P AG18 → 94 LVDS_U_DATA_P<0> OUT
- TXOUT_U0N AH18 → 94 LVDS_U_DATA_N<0> OUT
- TXOUT_U1P AK20 → 94 LVDS_U_DATA_P<1> OUT
- TXOUT_U1N AJ20 → 94 LVDS_U_DATA_N<1> OUT
- TXOUT_U2P AG20 → 94 LVDS_U_DATA_P<2> OUT
- TXOUT_U2N AH20 → 94 LVDS_U_DATA_N<2> OUT
- TXOUT_U3P AH21 → 94 LVDS_U_DATA_P<3> OUT
- TXOUT_U3N AG21 → 94 LVDS_U_DATA_N<3> OUT
- TXCLK_LP AM18 → 94 93 LVDS_L_CLK_P OUT
- TXCLK_LN AL18 → 94 93 LVDS_L_CLK_N OUT
- TXOUT_L0P AL19 → 94 93 LVDS_L_DATA_P<0> OUT
- TXOUT_L0N AK19 → 94 93 LVDS_L_DATA_N<0> OUT
- TXOUT_L1P AM20 → 94 93 LVDS_L_DATA_P<1> OUT
- TXOUT_L1N AL20 → 94 93 LVDS_L_DATA_N<1> OUT
- TXOUT_L2P AM21 → 94 93 LVDS_L_DATA_P<2> OUT
- TXOUT_L2N AL21 → 94 93 LVDS_L_DATA_N<2> OUT
- TXOUT_L3P AJ18 → 94 LVDS_L_DATA_P<3> OUT
- TXOUT_L3N AK18 → 94 LVDS_L_DATA_N<3> OUT

MONITOR IDENTIFICATION outputs:
- DDC1CLK AH23 → 97 GPU_DDC_A_CLK TO
- DDC1DATA AH22 → 97 GPU_DDC_A_DATA TO
- DDC2CLK AG13 → 88 GPU_DDC_B_CLK TO
- DDC2DATA AH13 → 88 GPU_DDC_B_DATA TO
- DDC3CLK AF12 → 94 93 GPU_DDC_C_CLK TO
- DDC3DATA AE12 → 94 93 GPU_DDC_C_DATA TO

ATI_RSET 93 — R9350 499 1% 1/16W MF-LF 402
ATI_R2SET 93 — R9351 715 1% 1/16W MF-LF 402

TERMINATION FOR TMDS USAGE OF LVDS PINS
PLACE CLOSE TO GPU (U8400)

94 93 LVDS_L_CLK_P → TMDS_PANEL R9370 100 5% 1/10W MF-LF 402
94 93 LVDS_L_CLK_N
94 93 LVDS_L_DATA_P<0> → TMDS_PANEL R9371 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<0>
94 93 LVDS_L_DATA_P<1> → TMDS_PANEL R9372 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<1>
94 93 LVDS_L_DATA_P<2> → TMDS_PANEL R9373 100 5% 1/10W MF-LF 402
94 93 LVDS_L_DATA_N<2>

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

91 88 85 =PP3V3_S0_GPU
R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402
94 93 GPU_DDC_C_CLK
94 93 GPU_DDC_C_DATA

ATI M56 Video Interfaces

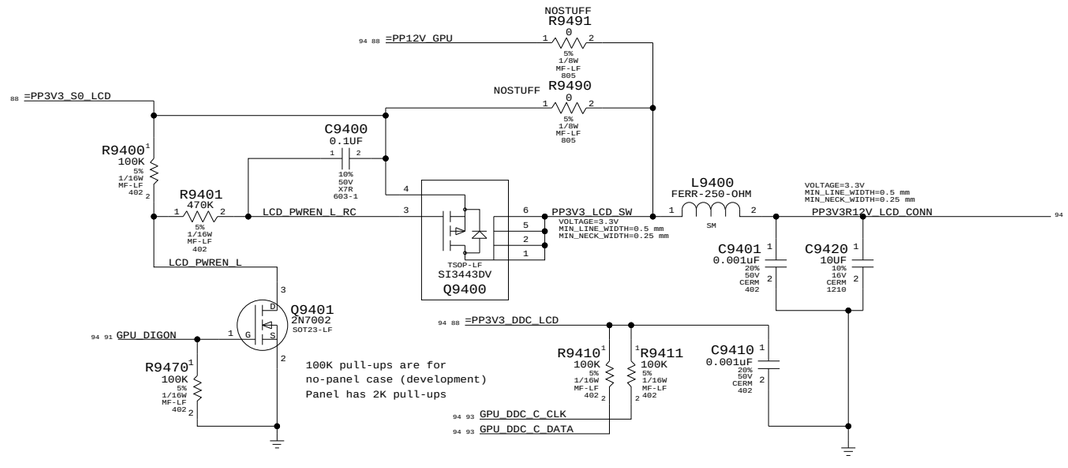
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

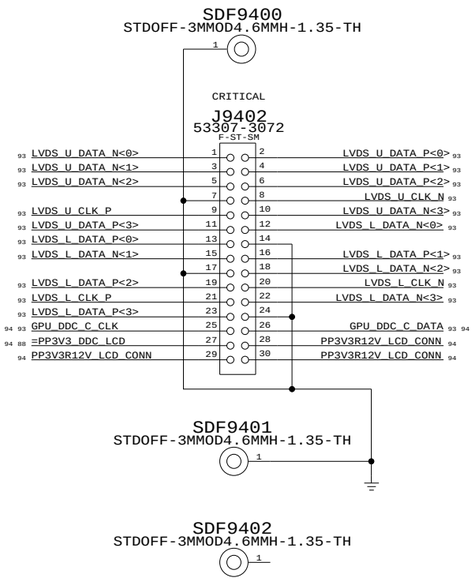
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	93	111

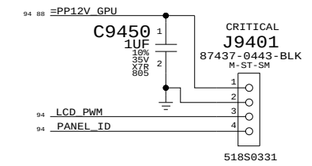
LCD (LVDS) INTERFACE

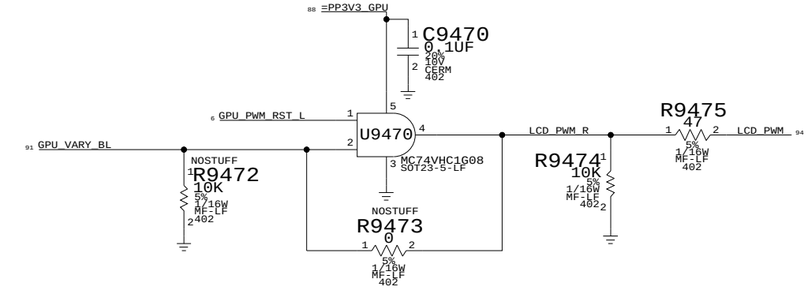




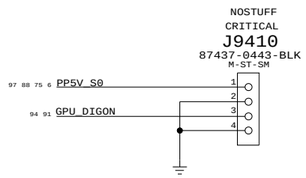
NOTE: 3RD STANDOFF FOR LVDS->TMDS CONVERTER BOARD

INVERTER INTERFACE





GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL



Internal Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	94	111

TP_TMDS_DATA_P<3> — TMDS_DATA_P<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<3> — TMDS_DATA_N<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<4> — TMDS_DATA_P<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<4> — TMDS_DATA_N<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<5> — TMDS_DATA_P<5> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<5> — TMDS_DATA_N<5> 93
MAKE_BASE=TRUE

TP_ATI_DVPDATA<23> — ATI_DVPDATA<23> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<22> — ATI_DVPDATA<22> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<21> — ATI_DVPDATA<21> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<20> — ATI_DVPDATA<20> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<19> — ATI_DVPDATA<19> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<18> — ATI_DVPDATA<18> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<17> — ATI_DVPDATA<17> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<16> — ATI_DVPDATA<16> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<15> — ATI_DVPDATA<15> 91
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TP_ATI_DVPDATA<14> — ATI_DVPDATA<14> 91
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TP_ATI_DVPDATA<13> — ATI_DVPDATA<13> 91
MAKE_BASE=TRUE

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TP_ATI_DVPDATA<11> — ATI_DVPDATA<11> 91
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TP_ATI_DVPDATA<10> — ATI_DVPDATA<10> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<9> — ATI_DVPDATA<9> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<8> — ATI_DVPDATA<8> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<7> — ATI_DVPDATA<7> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<6> — ATI_DVPDATA<6> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<5> — ATI_DVPDATA<5> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<4> — ATI_DVPDATA<4> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<3> — ATI_DVPDATA<3> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<2> — ATI_DVPDATA<2> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<1> — ATI_DVPDATA<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<0> — ATI_DVPDATA<0> 91
MAKE_BASE=TRUE

TP_ATI_DVPCLK — ATI_DVPCLK 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<0> — ATI_DVPCNTL<0> 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<1> — ATI_DVPCNTL<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPCNTL<2> — ATI_DVPCNTL<2> 91
MAKE_BASE=TRUE

TP_GPU_GPIO<34> — GPU_GPIO_34 91
MAKE_BASE=TRUE

TP_GPU_GPIO<33> — GPU_GPIO_33 91
MAKE_BASE=TRUE

TP_GPU_GPIO<32> — GPU_GPIO_32 91
MAKE_BASE=TRUE

TP_GPU_GPIO<31> — GPU_GPIO_31 91
MAKE_BASE=TRUE

TP_GPU_GPIO<30> — GPU_GPIO_30 91
MAKE_BASE=TRUE

TP_GPU_GPIO<26> — GPU_GPIO_26 91
MAKE_BASE=TRUE

TP_GPU_GPIO<25> — GPU_GPIO_25 91
MAKE_BASE=TRUE

TP_GPU_GPIO<23> — GPU_GPIO_23 91
MAKE_BASE=TRUE

TP_GPU_GPIO<22> — GPU_GPIO_22 91
MAKE_BASE=TRUE

TP_GPU_GPIO<21> — GPU_GPIO_21 91
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TP_GPU_GPIO<20> — GPU_GPIO_20 91
MAKE_BASE=TRUE

TP_GPU_GPIO<19> — GPU_GPIO_19 91
MAKE_BASE=TRUE

TP_GPU_GPIO<18> — GPU_GPIO_18 91
MAKE_BASE=TRUE

TP_GPU_GENERICA — GPU_GENERICA 91
MAKE_BASE=TRUE

TP_GPU_GENERICB — GPU_GENERICB 91
MAKE_BASE=TRUE

TP_GPU_GENERICC — GPU_GENERICC 91
MAKE_BASE=TRUE

M56 TPS

NOTICE OF PROPRIETARY PROPERTY

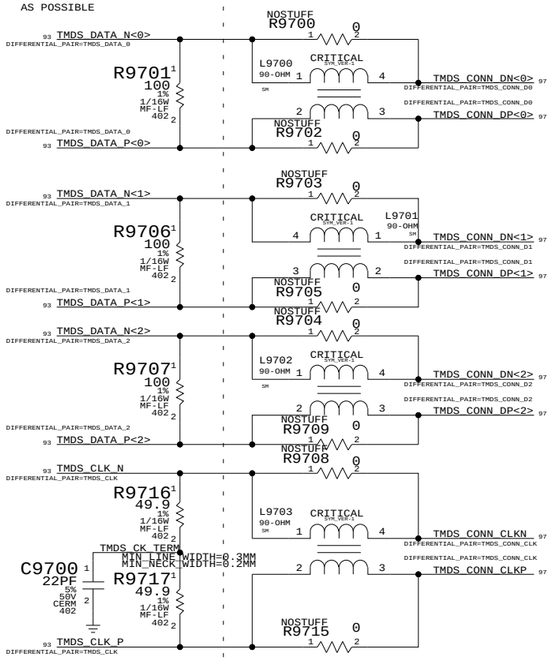
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 95 OF 111	

DVI INTERFACE

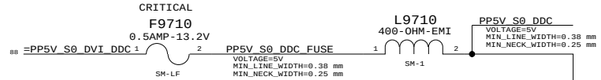
PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

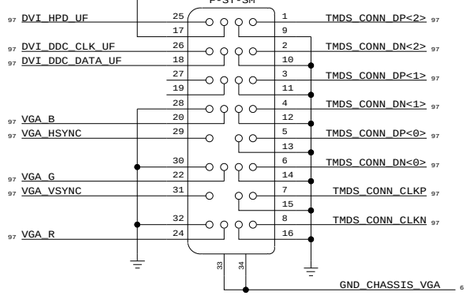
PLACE FILTER CLOSE
TO TMDS CONNECTOR



DVI DDC CURRENT LIMIT

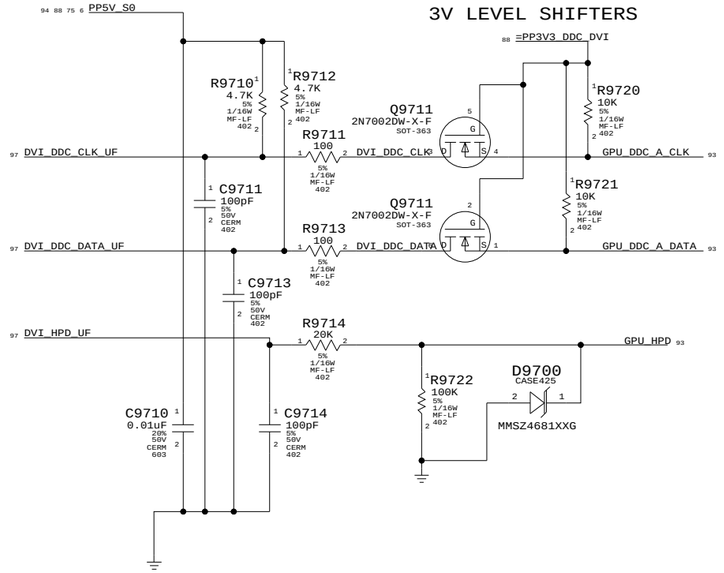
(55mA requirement per DVI spec)





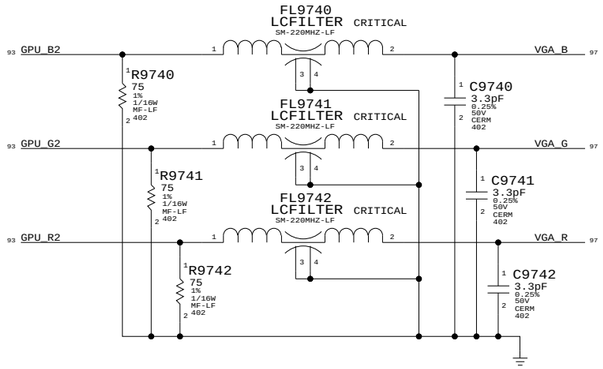
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0114	1	CONN,32-P MINI-DVI RCPT MG3,LF	J9710	CRITICAL	17_INCH_LCD
514S0116	1	CONN,32-P MINI-DVI RCPT MG3,LF	J9710	CRITICAL	20_INCH_LCD

3V LEVEL SHIFTERS

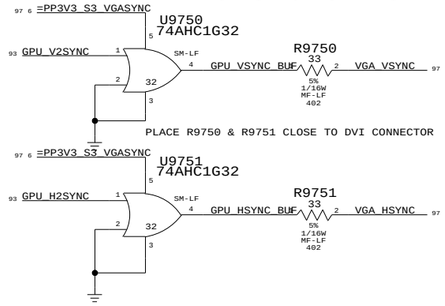


ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS



External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	97	111

Title: Basenet Report
Design: m38
Date: Nov 15 17:44:33 2005

Base nets and synonyms for m38_lib.M38(@m38_lib.m38(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
0V7_REF	0V7_REF - @m38_lib.M38	79A3
1V0_REF	1V0_REF - @m38_lib.M38	79A5 80A5 81A5 81B3
1V2REG_ITH	1V2REG_ITH - @m38_lib.M38	77B5
1V2REG_ITH_RC	1V2REG_ITH_RC - @m38_lib.M38	77B6
1V2REG_MODE	1V2REG_MODE - @m38_lib.M38	77B5
1V2REG_PGOOD	1V2REG_PGOOD - @m38_lib.M38	77B4
1V2REG_RT	1V2REG_RT - @m38_lib.M38	77B5
1V2REG_RUNSS	1V2REG_RUNSS - @m38_lib.M38	77B5
1V2REG_SGND	1V2REG_SGND - @m38_lib.M38	77A7
1V2REG_SW	1V2REG_SW - @m38_lib.M38	77B4
1V2REG_VFB	1V2REG_VFB - @m38_lib.M38	77B5
1V2REG_VFB_DIV	1V2REG_VFB_DIV - @m38_lib.M38	77A5
1V3_REF	1V3_REF - @m38_lib.M38	80B3
1V05REG_NB_BOOT	1V05REG_NB_BOOT - @m38_lib.M38	81C6
1V05REG_NB_BOOT_R	1V05REG_NB_BOOT_R - @m38_lib.M38	81C5
1V05REG_NB_COMP	1V05REG_NB_COMP - @m38_lib.M38	81C6
1V05REG_NB_COMP_R	1V05REG_NB_COMP_R - @m38_lib.M38	81C5
1V05REG_NB_FB	1V05REG_NB_FB - @m38_lib.M38	81C5
1V05REG_NB_FB_R	1V05REG_NB_FB_R - @m38_lib.M38	81C3
1V05REG_NB_FS_DIS	1V05REG_NB_FS_DIS - @m38_lib.M38	81C7
1V05REG_NB_GND	1V05REG_NB_GND - @m38_lib.M38	81B7
1V05REG_NB_LDO_DR	1V05REG_NB_LDO_DR - @m38_lib.M38	81C7
1V05REG_NB_LDO_FB	1V05REG_NB_LDO_FB - @m38_lib.M38	81C7
1V05REG_NB_LGATE	1V05REG_NB_LGATE - @m38_lib.M38	81C6
1V05REG_NB_PVCC5	1V05REG_NB_PVCC5 - @m38_lib.M38	81D7
1V05REG_NB_SNUB	1V05REG_NB_SNUB - @m38_lib.M38	81C4
1V05REG_NB_SWITCHNODE	1V05REG_NB_SWITCHNODE - @m38_lib.M38	81C5
1V05REG_NB_UGATE	1V05REG_NB_UGATE - @m38_lib.M38	81D6
1V05REG_NB_VCC5	1V05REG_NB_VCC5 - @m38_lib.M38	81D7
1V5REG_PCIE_BOOT	1V5REG_PCIE_BOOT - @m38_lib.M38	80C6
1V5REG_PCIE_BOOT_R	1V5REG_PCIE_BOOT_R - @m38_lib.M38	80C5
1V5REG_PCIE_COMP	1V5REG_PCIE_COMP - @m38_lib.M38	80C6
1V5REG_PCIE_COMP_R	1V5REG_PCIE_COMP_R - @m38_lib.M38	80C5
1V5REG_PCIE_FB	1V5REG_PCIE_FB - @m38_lib.M38	80C5
1V5REG_PCIE_FB_R	1V5REG_PCIE_FB_R - @m38_lib.M38	80C3
1V5REG_PCIE_FS_DIS	1V5REG_PCIE_FS_DIS - @m38_lib.M38	80C7
1V5REG_PCIE_GND	1V5REG_PCIE_GND - @m38_lib.M38	80B7
1V5REG_PCIE_LDO_DR	1V5REG_PCIE_LDO_DR - @m38_lib.M38	80C7
1V5REG_PCIE_LDO_FB	1V5REG_PCIE_LDO_FB - @m38_lib.M38	80C7
1V5REG_PCIE_LGATE	1V5REG_PCIE_LGATE - @m38_lib.M38	80C6
1V5REG_PCIE_PVCC5	1V5REG_PCIE_PVCC5 - @m38_lib.M38	80D7
1V5REG_PCIE_SNUB	1V5REG_PCIE_SNUB - @m38_lib.M38	80C4
1V5REG_PCIE_SWITCHNODE	1V5REG_PCIE_SWITCHNODE - @m38_lib.M38	80C5
1V5REG_PCIE_UGATE	1V5REG_PCIE_UGATE - @m38_lib.M38	80D6
1V5REG_PCIE_VCC5	1V5REG_PCIE_VCC5 - @m38_lib.M38	80D7
1V6_REF	1V6_REF - @m38_lib.M38	79B3
1V8REG_DDR_BOOT	1V8REG_DDR_BOOT - @m38_lib.M38	79D6
1V8REG_DDR_BOOT_R	1V8REG_DDR_BOOT_R - @m38_lib.M38	79D5
1V8REG_DDR_COMP	1V8REG_DDR_COMP - @m38_lib.M38	79C6
1V8REG_DDR_COMP_R	1V8REG_DDR_COMP_R - @m38_lib.M38	79C5
1V8REG_DDR_FB	1V8REG_DDR_FB - @m38_lib.M38	79C5
1V8REG_DDR_FB_R	1V8REG_DDR_FB_R - @m38_lib.M38	79C3
1V8REG_DDR_FS_DIS	1V8REG_DDR_FS_DIS - @m38_lib.M38	79C7
1V8REG_DDR_GND	1V8REG_DDR_GND - @m38_lib.M38	79C7
1V8REG_DDR_LDO_DR	1V8REG_DDR_LDO_DR - @m38_lib.M38	79C7
1V8REG_DDR_LDO_FB	1V8REG_DDR_LDO_FB - @m38_lib.M38	79C7
1V8REG_DDR_LGATE	1V8REG_DDR_LGATE - @m38_lib.M38	79C6
1V8REG_DDR_PVCC5	1V8REG_DDR_PVCC5 - @m38_lib.M38	79D7
1V8REG_DDR_SNUB	1V8REG_DDR_SNUB - @m38_lib.M38	79C4
1V8REG_DDR_SWITCHNODE	1V8REG_DDR_SWITCHNODE - @m38_lib.M38	79C5
1V8REG_DDR_UGATE	1V8REG_DDR_UGATE - @m38_lib.M38	79D6
1V8REG_DDR_VCC5	1V8REG_DDR_VCC5 - @m38_lib.M38	79D7
1V8REG_GPU_BOOT	1V8REG_GPU_BOOT - @m38_lib.M38	78C6
1V8REG_GPU_BOOT_R	1V8REG_GPU_BOOT_R - @m38_lib.M38	78C5
1V8REG_GPU_COMP	1V8REG_GPU_COMP - @m38_lib.M38	78B6
1V8REG_GPU_COMP_R	1V8REG_GPU_COMP_R - @m38_lib.M38	78B5
1V8REG_GPU_FB	1V8REG_GPU_FB - @m38_lib.M38	78B5
1V8REG_GPU_FB_R	1V8REG_GPU_FB_R - @m38_lib.M38	78B3
1V8REG_GPU_FS_DIS	1V8REG_GPU_FS_DIS - @m38_lib.M38	78B7
1V8REG_GPU_GND	1V8REG_GPU_GND - @m38_lib.M38	78B7
1V8REG_GPU_LDO_DR	1V8REG_GPU_LDO_DR - @m38_lib.M38	78C7
1V8REG_GPU_LDO_FB	1V8REG_GPU_LDO_FB - @m38_lib.M38	78B7
1V8REG_GPU_LGATE	1V8REG_GPU_LGATE - @m38_lib.M38	78B6
1V8REG_GPU_PVCC5	1V8REG_GPU_PVCC5 - @m38_lib.M38	78C7
1V8REG_GPU_SNUB	1V8REG_GPU_SNUB - @m38_lib.M38	78B4
1V8REG_GPU_SWITCHNODE	1V8REG_GPU_SWITCHNODE - @m38_lib.M38	78B5
1V8REG_GPU_UGATE	1V8REG_GPU_UGATE - @m38_lib.M38	78C6
1V8REG_GPU_VCC5	1V8REG_GPU_VCC5 - @m38_lib.M38	78C7
2V5REG_ITH	2V5REG_ITH - @m38_lib.M38	77C4
2V5REG_ITH_RC	2V5REG_ITH_RC - @m38_lib.M38	77C4
2V5REG_MODE	2V5REG_MODE - @m38_lib.M38	77C5
2V5REG_RT	2V5REG_RT - @m38_lib.M38	77C5
2V5REG_SGND	2V5REG_SGND - @m38_lib.M38	77C4
2V5REG_SW	2V5REG_SW - @m38_lib.M38	77C4
2V5REG_VFB	2V5REG_VFB - @m38_lib.M38	77C4
5V_REG_IN	5V_REG_IN - @m38_lib.M38	68A4
=I2C_HD_TEMP_SCL	=I2C_HD_TEMP_SCL - @m38_lib.M38	59C1 66B6
	=I2C_ODD_TEMP_SCL - @m38_lib.M38	59C1 66B4
	=SMB_THRM_CLK - @m38_lib.M38	10C3 59C1
	SMB_B_S0_CLK - @m38_lib.M38	58B5 59C2 59D1
	SMB_GPU_NB_THRM_CLK - @m38_lib.M38	59B1 61C3
	SMB_B_S0_CLK - @m38_lib.M38	58B5 59C2 59D1
	=SMB_THRM_CLK - @m38_lib.M38	10C3 59C1
	=I2C_ODD_TEMP_SCL - @m38_lib.M38	59C1 66B4
=I2C_HD_TEMP_SDA	=I2C_HD_TEMP_SDA - @m38_lib.M38	59C1 66B6
	=I2C_ODD_TEMP_SDA - @m38_lib.M38	59C1 66B4
	=SMB_THRM_DATA - @m38_lib.M38	10C3 59C1
	SMB_B_S0_DATA - @m38_lib.M38	58B5 59C2 59D1
	SMB_GPU_NB_THRM_DATA - @m38_lib.M38	59B1 61C3
	SMB_B_S0_DATA - @m38_lib.M38	58B5 59C2 59D1
	=SMB_THRM_DATA - @m38_lib.M38	10C3 59C1
	=I2C_ODD_TEMP_SDA - @m38_lib.M38	59C1 66B4
=I2C_MEM_SCL	=I2C_MEM_SCL - @m38_lib.M38	27D6 28A6 29A6
	=SMB_AIRPORT_CLK - @m38_lib.M38	27D6 53B4
	SMB_CK410_CLK - @m38_lib.M38	27D6 33B6
	SMB_CLK - @m38_lib.M38	23D5 27B7 27D7
	SMB_CK410_CLK - @m38_lib.M38	27D6 33B6
	=SMB_AIRPORT_CLK - @m38_lib.M38	27D6 53B4
=I2C_MEM_SDA	=I2C_MEM_SDA - @m38_lib.M38	27D6 28A6 29A6
	=SMB_AIRPORT_DATA - @m38_lib.M38	27C6 53B4
	SMB_CK410_DATA - @m38_lib.M38	27D6 33B6
	SMB_DATA - @m38_lib.M38	23D5 27B7 27D7
	SMB_CK410_DATA - @m38_lib.M38	27D6 33B6

	=SMB_AIRPORT_DATA - @m38_lib.M38	27C6 53B4
=PNBB_S0_GPU	=PNBB_S0_GPU - @m38_lib.M38	86D2 88C6
	=PNVOUT_S0_GPUBBN_REG - @m38_lib.M38	85B1 88C6
	PNBB_S0_GPU - @m38_lib.M38	88C8
	=PNVOUT_S0_GPUBBN_REG - @m38_lib.M38	85B1 88C6
=PP0V9_S0_MEMVTT_LDO	=PP0V9_S0_MEMVTT_LDO - @m38_lib.M38	6D4 31B3
	=PP0V9_S0_MEM_TERM - @m38_lib.M38	6D4 30D4
	PP0V9_S0 - @m38_lib.M38	6D6 79A3
	=PP0V9_S0_MEM_TERM - @m38_lib.M38	6D4 30D4
=PP1V2_S0_GPU_VDDPLL	=PP1V2_S0_GPU_VDDPLL - @m38_lib.M38	88C6 91B8
	=PPVIO_S0_PCIE - @m38_lib.M38	84A2 88C6
	=PP1V2_S0_REG - @m38_lib.M38	77A1 88C6
	=PP1V2_S0_PCIE_GPU_PVDD - @m38_lib.M38	84C8 88D6
	=PP1V2_S0_PCIE_GPU_VDDR - @m38_lib.M38	84C8 88D6
=PP1V2_S3_ENET	=PP1V2_S3_ENET - @m38_lib.M38	41A8 41D6 42B5
	PP1V2_S3_ENET - @m38_lib.M38	42B5
=PP1V2_S3_LAN	=PP1V2_S3_LAN - @m38_lib.M38	6D3 42B8
	PP1V2_S3 - @m38_lib.M38	6D4 77B2
=PP1V8_S0_FB_VDD	=PP1V8_S0_FB_VDD - @m38_lib.M38	88B6 89D5 89D8 90D5 90D8
	=PP1V8_S0_FB_VDDQ - @m38_lib.M38	88B6 89D5 89D8 90D5 90D8
	=PP1V8R2V0_S0_FB_GPU - @m38_lib.M38	86B8 87A5 87A8 87B5 87B8 88B6
	PP1V8_S0 - @m38_lib.M38	78B2 88B6
	=PP1V8R3V3_S0_GPU_VDDR5 - @m38_lib.M38	88B6 91B7
	=PP1V8R3V3_S0_GPU_VDDR4 - @m38_lib.M38	88B6 91B7
	PP1V8_S0 - @m38_lib.M38	78B2 88B6
	PP1V8R2V0_S0_FB_GPU - @m38_lib.M38	88B8
	=PP1V8_S0_FB_VDDQ - @m38_lib.M38	88B6 89D5 89D8 90D5 90D8
	=PP1V8R3V3_S0_GPU_VDDR5 - @m38_lib.M38	88B6 91B7
	=PP1V8R3V3_S0_GPU_VDDR4 - @m38_lib.M38	88B6 91B7
	=PP1V8R2V0_S0_FB_GPU - @m38_lib.M38	86B8 87A5 87A8 87B5 87B8 88B6
=PP1V8_S3_MEM_NB	=PP1V8_S3_MEM_NB - @m38_lib.M38	6D3 6D3 14C2 16B6 19B8 19D7
	=PP1V8_S0_MEMVTT - @m38_lib.M38	6D3 31C7
	PP1V8_S3 - @m38_lib.M38	5D2 6D4 79C2
	=PP1V8_S3_MEM - @m38_lib.M38	5C4 6D3 28B2 28C8 28D3 28D6 29B2 29D3 29D6
	PP1V8_S3 - @m38_lib.M38	5D2 6D4 79C2
	=PP1V8_S3_MEM - @m38_lib.M38	5C4 6D3 28B2 28C8 28D3 28D6 29B2 29D3 29D6
	=PP1V8_S0_MEMVTT - @m38_lib.M38	6D3 31C7
=PP2V5_S0_NB_VCCA_3GBG	=PP2V5_S0_NB_VCCA_3GBG - @m38_lib.M38	6B4 17D6 19A8 19C7
	=PP2V5_S0_GPU - @m38_lib.M38	88B6 93C8
	PP2V5_S0 - @m38_lib.M38	6B6 77C3 88C8
	=PP2V5_S0_GPU_VDD25 - @m38_lib.M38	88B6 91C6
	=PP2V5_S0_GPU_VDDC_CT - @m38_lib.M38	88B6 91C6
	=PP2V5_S0_GPU_PVDD - @m38_lib.M38	88B6 91A8
=PP2V5_S3_ENET	=PP2V5_S3_ENET - @m38_lib.M38	41D5 41D6 42C4
	PP2V5_S3_ENET - @m38_lib.M38	42C4 43D8
=PP3V3_S0_NB	=PP3V3_S0_NB - @m38_lib.M38	6A4 14C6 14D6 19C7 20A4 20B4 20B4
	=PP3V3_DDC_DVI - @m38_lib.M38	88C6 97D2
	=PP3V3_DDC_LCD - @m38_lib.M38	88C6 94A7 94C7
	=PP3V3_GPU - @m38_lib.M38	88C6 94B3
	PP3V3_S0 - @m38_lib.M38	6A7 6B6 6D8 10D2 26B7 26C6 41D8 59D3 61C3 76D6 88C8
	=PP3V3_S0_GPUBBCTL - @m38_lib.M38	85A7 88C6
	=PP3V3_S0_GPUBBN - @m38_lib.M38	85B5 88C6
	=PP3V3_S0_GPU - @m38_lib.M38	85B3 88C6 91D2 93A1
	=PP3V3_S0_GPU_VDDR3 - @m38_lib.M38	88C6 88D3 91C6
	=PP3V3_S0_LCD - @m38_lib.M38	88C6 94C8
	=PP3V3_S0_GPUBBP - @m38_lib.M38	85B8 88C6
	=PP3V3_S0_2V5REG - @m38_lib.M38	6A4 77D6
	=PP3V3_S0_AIRPORT - @m38_lib.M38	6A4 53C2
	=PP3V3_S0_PCI - @m38_lib.M38	6A4 44D5
	=PP3V3_S0_AUDIO - @m38_lib.M38	6A4 68A6 68D7 72A6 72C8 72D5 73B8 73C2 74B5 74C5 74D5
	=PP3V3_S0_IMVP - @m38_lib.M38	6A4 75D8
	=PP3V3_S0_CK410 - @m38_lib.M38	6A4 33C8 33D3 33D8 34D4
	=PPSPD_S0_MEM - @m38_lib.M38	6A4 28A7 29A3 29A7
	=PP3V3_S0_TPM - @m38_lib.M38	6A4 67C7 67D4
	=PP3V3_S0_3V3_1V5_VCCHDA - @m38_lib.M38	6A4 24C3 25C4
	=PP3V3_S0_ODD_TSENS - @m38_lib.M38	6A4 66B4
	=PP3V3_S0_HD_TSENS - @m38_lib.M38	6B4 66B5
	=PP3V3_S0_FAN - @m38_lib.M38	6B4 59A8 59B7 65B7 65C7 66C7
	=PP3V3_S0_PATA - @m38_lib.M38	6B4 38D3
	=PP3V3_S0_SB_PM - @m38_lib.M38	6B4 26D4
	=PP3V3_S0_SB_PCI - @m38_lib.M38	6B4 26D1
	=PP3V3_S0_SB_VCC3_3_IDE - @m38_lib.M38	6B4 24C3 25B3
	=PP3V3_S0_SB_VCC3_3_PCI - @m38_lib.M38	6B4 24B3 25A3
	=PP3V3_S0_SB_VCC3_3 - @m38_lib.M38	6B4 24B5 24B5 25B8 25C6
	=PP3V3_S0_NB_VCC_HV - @m38_lib.M38	6B4 17C6 19A8 19C7
	=PP3V3_S0_SB_GPIO - @m38_lib.M38	6B4 21C3 21D3 23B3 23D5
	=PP3V3_S0_SB_VCCLAN3_3 - @m38_lib.M38	6A4 24D3 25D3
	=PP3V3_S0_SB - @m38_lib.M38	6B4 22B5 25D8
	PP3V3_S0 - @m38_lib.M38	6A7 6B6 6D8 10D2 26B7 26C6 41D8 59D3 61C3 76D6 88C8
	=PPSPD_S0_MEM - @m38_lib.M38	6A4 28A7 29A3 29A7
	=PP3V3_S0_TPM - @m38_lib.M38	6A4 67C7 67D4
	=PP3V3_S0_SB_VCCLAN3_3 - @m38_lib.M38	6A4 24D3 25D3
	=PP3V3_S0_SB_VCC3_3_PCI -	6B4 24B3 25A3

	@m38_lib.M38	
	=PP3V3_S0_SB_VCC3_3_IDE - @m38_lib.M38	6B4 24C3 25B3
	=PP3V3_S0_SB_VCC3_3 - @m38_lib.M38	6B4 24B5 24B5 25B8 25C6
	=PP3V3_S0_SB_PM - @m38_lib.M38	6B4 26D4
	=PP3V3_S0_SB_PCI - @m38_lib.M38	6B4 26D1
	=PP3V3_S0_SB_GPIO - @m38_lib.M38	6B4 21C3 21D3 23B3 23D5
	=PP3V3_S0_SB_3V3_1V5_VCCHDA - @m38_lib.M38	6A4 24C3 25C4
	=PP3V3_S0_SB - @m38_lib.M38	6B4 22B5 25D8
	=PP3V3_S0_PCI - @m38_lib.M38	6A4 44D5
	=PP3V3_S0_PATA - @m38_lib.M38	6B4 38D3
	=PP3V3_S0_ODD_TSENS - @m38_lib.M38	6A4 66B4
	=PP3V3_S0_VCC_HV - @m38_lib.M38	6B4 17C6 19A8 19C7
	=PP3V3_S0_PVCC5 - @m38_lib.M38	6A4 68D7
	=PP3V3_S0_LCD - @m38_lib.M38	88C6 94C8
	=PP3V3_S0_IMVP - @m38_lib.M38	6A4 75D8
	=PP3V3_S0_GPU_CLOCKS - @m38_lib.M38	88C6
	=PP3V3_S0_GPUBBP - @m38_lib.M38	85B8 88C6
	=PP3V3_S0_GPUBBN - @m38_lib.M38	85B5 88C6
	=PP3V3_S0_GPUBBCTL - @m38_lib.M38	85A7 88C6
	=PP3V3_S0_GPU - @m38_lib.M38	85B3 88C6 91D2 93A1
	=PP3V3_S0_FAN - @m38_lib.M38	6B4 59A8 59B7 65B7 65C7 66C7
	=PP3V3_S0_CK410 - @m38_lib.M38	6A4 33C8 33D3 33D8 34D4
	=PP3V3_S0_AUDIO - @m38_lib.M38	6A4 68A6 68D7 72A6 72C8 72D5 73B8 73C2 74B5 74C5 74D5
	=PP3V3_S0_AIRPORT - @m38_lib.M38	6A4 53C2
	=PP3V3_S0_2V5REG - @m38_lib.M38	6A4 77D6
	=PP3V3_GPU - @m38_lib.M38	88C6 94B3
	=PP3V3_DDC_LCD - @m38_lib.M38	88C6 94A7 94C7
	=PP3V3_DDC_DVI - @m38_lib.M38	88C6 97D2
=PP3V3_S3_1V2REG	=PP3V3_S3_1V2REG - @m38_lib.M38	6D3 77B7
	=PP3V3_S3_USB - @m38_lib.M38	6C3 49C5
	=PP3V3_S3_VGASYNC - @m38_lib.M38	6C3 97A4 97B4
	PP3V3_S3 - @m38_lib.M38	6A7 6D4 53C4 59C8 59D3 83B3
	=PP3V3_S3_BT - @m38_lib.M38	6D3 47B3
	=PP3V3_S3_TPM - @m38_lib.M38	6D3 67C2
	=PP3V3_S3_ENET - @m38_lib.M38	6D3 41A5 41B3 41C3 41D6 41D8 42D3 42D8 43D2
	PP3V3_S3 - @m38_lib.M38	6A7 6D4 53C4 59C8 59D3 83B3
	=PP3V3_S3_VGASYNC - @m38_lib.M38	6C3 97A4 97B4
	=PP3V3_S3_USB - @m38_lib.M38	6C3 49C5
	=PP3V3_S3_TPM - @m38_lib.M38	6D3 67C2
	=PP3V3_S3_ENET - @m38_lib.M38	6D3 41A5 41B3 41C3 41D6 41D8 42D3 42D8 43D2
=PP3V3_S5_DEBUG	=PP3V3_S5_DEBUG - @m38_lib.M38	6D1 60D6
	=PP3V3_S5_ROM - @m38_lib.M38	6D1 63D4
	PP3V3_S5 - @m38_lib.M38	5D2 6C8 6D2 6D8 6D8 26C1 26C4 26C4 59A8 65B7 65D7 77C8 77C8 77D8 79A3 79A5 79B3 80A5 80B3 81A5 81A5 83C3
	=PP3V3_S5_SMC - @m38_lib.M38	6D1 58C2 58D3 58D4 59A4 59A5 59C4 59D3 59D8
	=PP3V3_S5_FW - @m38_lib.M38	6D1 44A6 44B2 44B7 44D5 44D7 45D6 46A8
	=PP3V3_S5_SB_IO - @m38_lib.M38	6D1 22C6 27C6
	=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA - @m38_lib.M38	6D1 24C3
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m38_lib.M38	6D1 24B3 25D1
	=PP3V3_S5_SB_VCCSUS3_3 - @m38_lib.M38	6D1 24A5 24B3 25B6 25D1
	=PP3V3_S5_SB_PM - @m38_lib.M38	6D1 11B5 23D1
	=PP3V3_S5_SB_USB - @m38_lib.M38	6D1 22D8
	=PP3V3_S5_SB - @m38_lib.M38	6D1 23A7 23B3 23B7 23D4 23D8 25C8 26D8
	PP3V3_S5 - @m38_lib.M38	5D2 6C8 6D2 6D8 6D8 26C1 26C4 26C4 59A8 65B7 65D7 66D7 76D2 76D4 77B8 77C7 77C8 77C8 77D8 79A3 79A5 79B3 80A5 80B3 81A5 81A5 83C3
	=PP3V3_S5_SMC - @m38_lib.M38	6D1 58C2 58D3 58D4 59A4 59A5 59C4 59D3 59D8
	=PP3V3_S5_FW - @m38_lib.M38	6D1 44A6 44B2 44B7 44D5 44D7 45D6 46A8
	=PP3V3_S5_SB_IO - @m38_lib.M38	6D1 22C6 27C6
	=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA - @m38_lib.M38	6D1 24C3
	=PP3V3_S5_SB_VCCSUS3_3_USB - @m38_lib.M38	6D1 24B3 25D1
	=PP3V3_S5_SB_VCCSUS3_3 - @m38_lib.M38	6D1 24A5 24B3 25B6 25D1
	=PP3V3_S5_SB_PM - @m38_lib.M38	6D1 11B5 23D1
	=PP3V3_S5_SB_USB - @m38_lib.M38	6D1 22D8
	=PP3V3_S5_SB - @m38_lib.M38	6D1 23A7 23B3 23B7 23D4 23D8 25C8 26D8
	=PP3V3_S5_ROM - @m38_lib.M38	6D1 63D4
	=PP3V3_S5_FW - @m38_lib.M38	6D1 44A6 44B2 44B7 44D5 44D7 45D6 46A8
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO - @m38_lib.M38	6A4 68A6
	PP5V_S0_AUDIO - @m38_lib.M38	6A5
=PP5V_S0_DEBUG	=PP5V_S0_DEBUG - @m38_lib.M38	6A4 60C6
	=PP5V_S0_DVI_DDC - @m38_lib.M38	88A6 97D6
	=PP5V_S0_GPUISENS - @m38_lib.M38	85D2 88A6
	PP5V_S0 - @m38_lib.M38	6A6 6D8 75D7 88B8 94A4 97D3
	=PP5V_S0_GPUBBCTL - @m38_lib.M38	85A6 88B6
	=PP5V_S0_SB - @m38_lib.M38	6A4 25D8
	=PP5V_S0_PATA - @m38_lib.M38	6A4 38C4 38D3
	PP5V_S0 - @m38_lib.M38	6A6 6D8 75D7 88B8 94A4 97D3
	=PP5V_S0_SB - @m38_lib.M38	6A4 25D8
	=PP5V_S0_PATA - @m38_lib.M38	6A4 38C4 38D3
	=PP5V_S0_GPUISENS - @m38_lib.M38	85D2 88A6
	=PP5V_S0_GPUBBCTL - @m38_lib.M38	85A6 88B6
	=PP5V_S0_DVI_DDC - @m38_lib.M38	88A6 97D6
=PP5V_S0_GPUVCORE	=PP5V_S0_GPUVCORE - @m38_lib.M38	85D7 88D6
	GPUVCORE_VCC - @m38_lib.M38	88D6
=PP5V_S0_MEMVTT	=PP5V_S0_MEMVTT - @m38_lib.M38	6C3 31C6
	PP5V_S3 - @m38_lib.M38	6C4 59D6 83C3
	=PP5V_S3_BNDI - @m38_lib.M38	6C3 47D4
	=PP5V_S3_USB - @m38_lib.M38	6C3 47C8
	PP5V_S3 - @m38_lib.M38	6C4 59D6 83C3
	=PP5V_S3_USB - @m38_lib.M38	6C3 47C8
	=PP5V_S3_BNDI - @m38_lib.M38	6C3 47D4
=PP5V_S5_SB	=PP5V_S5_SB - @m38_lib.M38	6D1 25C8

	PP5V_S5 - @m38_lib.M38	5D2 6A8 6D2 6D7 59A5 79B3 79B3 80B3 81B3 83C3
=PP12V_GPU	=PP12V_GPU - @m38_lib.M38	88B6 94C3 94D7
	PP12V_S0 - @m38_lib.M38	6A6 6D8 76B8 88B8
	=PP12V_S0_FAN - @m38_lib.M38	6A4 65B6 65D7 66D6
	PP12V_S0 - @m38_lib.M38	6A6 6D8 76B8 88B8
	=PP12V_S0_FAN - @m38_lib.M38	6A4 65B6 65D7 66D6
=PP12V_S0_AUDIO_SPKR AMP	=PP12V_S0_AUDIO_SPKRAMP - @m38_lib.M38	6A4 72D8
	PP12V_S0_AUDIO_SPKRAMP - @m38_lib.M38	6A5
=PP12V_S5_CPU	=PP12V_S5_CPU - @m38_lib.M38	6C1 76D8
	=PPVIN_S0_GPUVCORE - @m38_lib.M38	85D7 88B6
	PP12V_S5 - @m38_lib.M38	5D2 6C2 6D7 78C7 79D7 80D7 81D7 83C5 83C5 88B8
	=PP12V_S5_FW - @m38_lib.M38	6C1 46D7
	PP12V_S5 - @m38_lib.M38	5D2 6C2 6D7 78C7 79D7 80D7 81D7 83C5 83C5 88B8
	=PPVIN_S0_GPUVCORE - @m38_lib.M38	85D7 88B6
	=PP12V_S5_FW - @m38_lib.M38	6C1 46D7
=PP12V_S5_FW_PHY	=PP12V_S5_FW_PHY - @m38_lib.M38	44C2 46D5
	PP12V_FW - @m38_lib.M38	46D6
=PPBB_S0_GPU	=PPBB_S0_GPU - @m38_lib.M38	86D6 88C6
	=PPVOUT_S0_GPUBBP_LDO - @m38_lib.M38	85B5 88C6
	PPBB_S0_GPU - @m38_lib.M38	88C8
	=PPVOUT_S0_GPUBBP_LDO - @m38_lib.M38	85B5 88C6
=PPVCORE_S0_CPU	=PPVCORE_S0_CPU - @m38_lib.M38	6D4 8B6 8D7 8D8 9B8 76B5
	PPVCORE_CPU - @m38_lib.M38	5D2 6D6 75A4 75D1 76B4
=PPVCORE_S0_GPU	=PPVCORE_S0_GPU - @m38_lib.M38	76B4 86D8 88D6 91A7
	=PPVCORE_S0_GPU_BBP - @m38_lib.M38	85B7 88D6
	PP1V0R1V2_S0_GPU - @m38_lib.M38	59B4 88D8
	=PPVCORE_S0_GPU_REG - @m38_lib.M38	85C1 88D6
	PP1V0R1V2_S0_GPU - @m38_lib.M38	59B4 88D8
	=PPVCORE_S0_GPU_REG - @m38_lib.M38	85C1 88D6
	=PPVCORE_S0_GPU_BBP - @m38_lib.M38	85B7 88D6
ACZ_BITCLK	ACZ_BITCLK - @m38_lib.M38	21C7 68D7
ACZ_RST_L	ACZ_RST_L - @m38_lib.M38	21C7 68C7
ACZ_SDATAIN<0>	ACZ_SDATAIN<0> - @m38_lib.M38	21C7 68D7
ACZ_SDATAIN_CHIP	ACZ_SDATAIN_CHIP - @m38_lib.M38	68C6
ACZ_SDATAOUT	ACZ_SDATAOUT - @m38_lib.M38	21C7 68D7
ACZ_SYNC	ACZ_SYNC - @m38_lib.M38	21C7 68D7
AIRPORT_CLK100M_PCIE_N	AIRPORT_CLK100M_PCIE_N - @m38_lib.M38	34B4 34C2 53C6
AIRPORT_CLK100M_PCIE_P	AIRPORT_CLK100M_PCIE_P - @m38_lib.M38	34B4 34C2 53C6
AIRPORT_CONN_CLK	AIRPORT_CONN_CLK - @m38_lib.M38	53B5
AIRPORT_CONN_DATA	AIRPORT_CONN_DATA - @m38_lib.M38	53B5
AIRPORT_RST_L	AIRPORT_RST_L - @m38_lib.M38	5A7 53C5
AIRPORT_WAKE_L	AIRPORT_WAKE_L - @m38_lib.M38	53C6
ALL_SYS_PWRGD	ALL_SYS_PWRGD - @m38_lib.M38	26D5 58D7 77B6
ALS_GAIN	ALS_GAIN - @m38_lib.M38	58B5 59C6
	NC_ALS_GAIN - @m38_lib.M38	59C5
ALS_LEFT	ALS_LEFT - @m38_lib.M38	58A7 59D5
	TP_ALS_LEFT - @m38_lib.M38	59D3
ALS_RIGHT	ALS_RIGHT - @m38_lib.M38

AUD_GPIO_1_A	AUD_GPIO_1_A - @m38_lib.M38	68A8 73C2
AUD_GPIO_2	AUD_GPIO_2 - @m38_lib.M38	68C7 74A6
AUD_LI_DET_EMI	AUD_LI_DET_EMI - @m38_lib.M38	73D7
AUD_LI_DET_H	AUD_LI_DET_H - @m38_lib.M38	73D4 74C5
AUD_LI_DET_JACK	AUD_LI_DET_JACK - @m38_lib.M38	73D8
AUD_LI_GND_EMI	AUD_LI_GND_EMI - @m38_lib.M38	73C7
AUD_LI_GND_JACK	AUD_LI_GND_JACK - @m38_lib.M38	73D8
AUD_LI_L_EMI	AUD_LI_L_EMI - @m38_lib.M38	73D7
AUD_LI_L_JACK	AUD_LI_L_JACK - @m38_lib.M38	73D8
AUD_LI_R_EMI	AUD_LI_R_EMI - @m38_lib.M38	73D7
AUD_LI_R_JACK	AUD_LI_R_JACK - @m38_lib.M38	73D8
AUD_LO_DET1	AUD_LO_DET1 - @m38_lib.M38	73B8 74A5
AUD_LO_DET1_1	AUD_LO_DET1_1 - @m38_lib.M38	74A4 74B2
AUD_LO_DET1_EMI	AUD_LO_DET1_EMI - @m38_lib.M38	73B7
AUD_LO_DET1_INV	AUD_LO_DET1_INV - @m38_lib.M38	74B3
AUD_LO_DET1_JACK	AUD_LO_DET1_JACK - @m38_lib.M38	73B4
AUD_LO_DET2	AUD_LO_DET2 - @m38_lib.M38	73B8 74B5
AUD_LO_DET2_1	AUD_LO_DET2_1 - @m38_lib.M38	74B4
AUD_LO_DET2_EMI	AUD_LO_DET2_EMI - @m38_lib.M38	73B7
AUD_LO_DET2_JACK	AUD_LO_DET2_JACK - @m38_lib.M38	73B4
AUD_LO_GND_EMI	AUD_LO_GND_EMI - @m38_lib.M38	73A7
AUD_LO_GND_JACK	AUD_LO_GND_JACK - @m38_lib.M38	73B4
AUD_LO_L_EMI	AUD_LO_L_EMI - @m38_lib.M38	73B7
AUD_LO_L_JACK	AUD_LO_L_JACK - @m38_lib.M38	73B4
AUD_LO_R_EMI	AUD_LO_R_EMI - @m38_lib.M38	73A7
AUD_LO_R_JACK	AUD_LO_R_JACK - @m38_lib.M38	73B4
AUD_MAX9714_CHOLD	AUD_MAX9714_CHOLD - @m38_lib.M38	72C4
AUD_MAX9714_VREG	AUD_MAX9714_VREG - @m38_lib.M38	72C5
AUD_MIC_IN_N	AUD_MIC_IN_N - @m38_lib.M38	73C6 74A6
AUD_MIC_IN_N_CONN	AUD_MIC_IN_N_CONN - @m38_lib.M38	47C2 73C4
AUD_MIC_IN_N_EMI	AUD_MIC_IN_N_EMI - @m38_lib.M38	73C5
AUD_MIC_IN_P	AUD_MIC_IN_P - @m38_lib.M38	73C6 74A6
AUD_MIC_IN_P_CONN	AUD_MIC_IN_P_CONN - @m38_lib.M38	47C2 73C4
AUD_MIC_IN_P_EMI	AUD_MIC_IN_P_EMI - @m38_lib.M38	73C5
AUD_MIC_P1	AUD_MIC_P1 - @m38_lib.M38	74A4
AUD_PORT_A_DET_L	AUD_PORT_A_DET_L - @m38_lib.M38	74B2
AUD_PORT_A_L	AUD_PORT_A_L - @m38_lib.M38	73B8 74B5
AUD_PORT_A_L1	AUD_PORT_A_L1 - @m38_lib.M38	74B7
AUD_PORT_A_R	AUD_PORT_A_R - @m38_lib.M38	73A8 74B5
AUD_PORT_A_R1	AUD_PORT_A_R1 - @m38_lib.M38	74B7
AUD_PORT_E_DET_L	AUD_PORT_E_DET_L - @m38_lib.M38	74B1
AUD_PORT_F_L	AUD_PORT_F_L - @m38_lib.M38	73D4 74C5
AUD_PORT_F_L1	AUD_PORT_F_L1 - @m38_lib.M38	74C7
AUD_PORT_F_R	AUD_PORT_F_R - @m38_lib.M38	73D4 74C5
AUD_PORT_F_R1	AUD_PORT_F_R1 - @m38_lib.M38	74C7
AUD_SAMP_FS1	AUD_SAMP_FS1 - @m38_lib.M38	72A6 72C5
AUD_SAMP_FS2	AUD_SAMP_FS2 - @m38_lib.M38	72A6 72C5
AUD_SAMP_G1	AUD_SAMP_G1 - @m38_lib.M38	72A6 72C5
AUD_SAMP_G2	AUD_SAMP_G2 - @m38_lib.M38	72A6 72C5
AUD_SAMP_INL_N	AUD_SAMP_INL_N - @m38_lib.M38	72C5
AUD_SAMP_INL_P	AUD_SAMP_INL_P - @m38_lib.M38	72C5
AUD_SAMP_INR_N	AUD_SAMP_INR_N - @m38_lib.M38	72C5
AUD_SAMP_INR_P	AUD_SAMP_INR_P - @m38_lib.M38	72C5
AUD_SAMP_SHDN_L	AUD_SAMP_SHDN_L - @m38_lib.M38	72C5
AUD_SENSE_A	AUD_SENSE_A - @m38_lib.M38	68C1 74C5 74D7
AUD_SENSE_B	AUD_SENSE_B - @m38_lib.M38	68C1 74C5 74D5 74D7
AUD_SPDIF_GND	AUD_SPDIF_GND - @m38_lib.M38	73A3
AUD_SPDIF_IN	AUD_SPDIF_IN - @m38_lib.M38	68C1 74B6
AUD_SPDIF_OUT	AUD_SPDIF_OUT - @m38_lib.M38	68D1 73B8
AUD_SPDIF_OUT_CHIP	AUD_SPDIF_OUT_CHIP - @m38_lib.M38	68D4
AUD_SPDIF_OUT_EMI	AUD_SPDIF_OUT_EMI - @m38_lib.M38	73B7
AUD_SPDIF_OUT_JACK	AUD_SPDIF_OUT_JACK - @m38_lib.M38	73B5
AUD_SPKR_OUTL_N	AUD_SPKR_OUTL_N - @m38_lib.M38	72C1 73D3
AUD_SPKR_OUTL_P	AUD_SPKR_OUTL_P - @m38_lib.M38	72C1 73D3
AUD_SPKR_OUTR_N	AUD_SPKR_OUTR_N - @m38_lib.M38	72C1 73D3
AUD_SPKR_OUTR_P	AUD_SPKR_OUTR_P - @m38_lib.M38	72C1 73D3
AUD_TYPE_DET_EN	AUD_TYPE_DET_EN - @m38_lib.M38	74B3
AUD_VREF_FIL	AUD_VREF_FIL - @m38_lib.M38	68C4
AUD_VREF_PORT_B	AUD_VREF_PORT_B - @m38_lib.M38	68C1 74A3
BAL_IN_COM	BAL_IN_COM - @m38_lib.M38	68C7 74A7
BAL_IN_L	BAL_IN_L - @m38_lib.M38	68C7 74A7
BAL_IN_R	BAL_IN_R - @m38_lib.M38	68C7 74A7
BAT_1	BAT_1 - @m38_lib.M38	26C8
BAT_2	BAT_2 - @m38_lib.M38	26C8
BEEP	BEEP - @m38_lib.M38	68C6
BIOS_REC	BIOS_REC - @m38_lib.M38	23A6 23C5
BOOT_LPC_SPI_L	BOOT_LPC_SPI_L - @m38_lib.M38	22B3 58C7 60C6
C8509_P1	C8509_P1 - @m38_lib.M38	85C5
CEN	CEN - @m38_lib.M38	68B5 74B6
CK410_27M_NONSPREAD	CK410_27M_NONSPREAD - @m38_lib.M38	34A4 92C7
CK410_27M_SPREAD	CK410_27M_SPREAD - @m38_lib.M38	34A4 92C5
	GPU_GPIO_16 - @m38_lib.M38	91C3 92C3
CK410_CLK14P3M_TIMER	CK410_CLK14P3M_TIMER - @m38_lib.M38	33A4 34D6
CK410_CPU0_N	CK410_CPU0_N - @m38_lib.M38	33C4 34B6
CK410_CPU0_P	CK410_CPU0_P - @m38_lib.M38	33C4 34B6
CK410_CPU1_N	CK410_CPU1_N - @m38_lib.M38	33C4 34B6
CK410_CPU1_P	CK410_CPU1_P - @m38_lib.M38	33C4 34B6
CK410_CPU2_ITP_SRC10_N	CK410_CPU2_ITP_SRC10_N - @m38_lib.M38	33C4 34B6
CK410_CPU2_ITP_SRC10_P	CK410_CPU2_ITP_SRC10_P - @m38_lib.M38	33C4 34B6
CK410_DOT96_27M_NONS PREAD_P	CK410_DOT96_27M_NONSPREAD_P - @m38_lib.M38	33A4 34A6
CK410_DOT96_27M_SPRE AD_N	CK410_DOT96_27M_SPREAD_N - @m38_lib.M38	33A4 34A6
CK410_FSA	CK410_FSA - @m38_lib.M38	34B8 34C4
CK410_FSB_TEST_MODE	CK410_FSB_TEST_MODE - @m38_lib.M38	33C6 34A8
CK410_FSC	CK410_FSC - @m38_lib.M38	34A8 34D4
CK410_IREF	CK410_IREF - @m38_lib.M38	33B6
CK410_LVDS_N	CK410_LVDS_N - @m38_lib.M38	33B4 34A6
	TP_CK410_LVDS_N - @m38_lib.M38	34A4
CK410_LVDS_P	CK410_LVDS_P - @m38_lib.M38	33B4 34A6
	TP_CK410_LVDS_P - @m38_lib.M38	34A4
CK410_PCI1_CLK	CK410_PCI1_CLK - @m38_lib.M38	33B6 34C6
CK410_PCI2_CLK	CK410_PCI2_CLK - @m38_lib.M38	33B6 34C6
CK410_PCI3_CLK	CK410_PCI3_CLK - @m38_lib.M38	33B6 34C6
CK410_PCI4_CLK	CK410_PCI4_CLK - @m38_lib.M38	33B6 34C6
CK410_PCI5_FCTSEL1	CK410_PCI5_FCTSEL1 - @m38_lib.M38	33B6 34D6
CK410_PCIF0_CLK	CK410_PCIF0_CLK - @m38_lib.M38	33B8 34B6
CK410_PCIF1_ITP_EN	CK410_PCIF1_ITP_EN - @m38_lib.M38	33B8 34B6
CK410_PD_VTT_PWRGD_L	CK410_PD_VTT_PWRGD_L - @m38_lib.M38 VR_PWRGD_CK410_L - @m38_lib.M38	26A8 33A4 26A7 75C6
CK410_REF1_FCTSEL0	CK410_REF1_FCTSEL0 - @m38_lib.M38	33A4 34C6
CK410_SRC1_N	CK410_SRC1_N - @m38_lib.M38	33B4 34A6
CK410_SRC1_P	CK410_SRC1_P - @m38_lib.M38	33B4 34A6
CK410_SRC2_N	CK410_SRC2_N - @m38_lib.M38	33B4 34A6
CK410_SRC2_P	CK410_SRC2_P - @m38_lib.M38	33B4 34A6
CK410_SRC3_N	CK410_SRC3_N - @m38_lib.M38	33B4 34D3
CK410_SRC3_P	CK410_SRC3_P - @m38_lib.M38	33B4 34D3
CK410_SRC4_N	CK410_SRC4_N - @m38_lib.M38	33B4 34B6
CK410_SRC4_P	CK410_SRC4_P - @m38_lib.M38	33B4 34B6
CK410_SRC5_N	CK410_SRC5_N - @m38_lib.M38	33B4 34B6
CK410_SRC5_P	CK410_SRC5_P - @m38_lib.M38	33B4 34B6
CK410_SRC6_N	CK410_SRC6_N - @m38_lib.M38	33B4 34B6

CK410_SRC6_P	CK410_SRC6_P - @m38_lib.M38	33B4 34B6
CK410_SRC7_N	CK410_SRC7_N - @m38_lib.M38	33B4 34D3
CK410_SRC7_P	CK410_SRC7_P - @m38_lib.M38	33B4 34D3
CK410_SRC8_N	CK410_SRC8_N - @m38_lib.M38	33A4 34A6
CK410_SRC8_P	CK410_SRC8_P - @m38_lib.M38	33A4 34A6
CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L - @m38_lib.M38	33B4 34D8
CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L - @m38_lib.M38	33B4 34D8
CK410_SRC_CLKREQ6_L	CK410_SRC_CLKREQ6_L - @m38_lib.M38	33B4 53C6
CK410_SRC_CLKREQ8_L	CK410_SRC_CLKREQ8_L - @m38_lib.M38	33A4 34D8
CK410_USB48_FSA	CK410_USB48_FSA - @m38_lib.M38	33A4 34C6
CK410_XTAL_IN	CK410_XTAL_IN - @m38_lib.M38	33C6
CK410_XTAL_OUT	CK410_XTAL_OUT - @m38_lib.M38	33C6
CLK_NB_OE_L	CLK_NB_OE_L - @m38_lib.M38	14B6 33B4
CPUVCORE_ISENSE_CAL	CPUVCORE_ISENSE_CAL - @m38_lib.M38	76A5
CPU_A20M_L	CPU_A20M_L - @m38_lib.M38	5C8 7C7 21C4
CPU_BSEL<0>	CPU_BSEL<0> - @m38_lib.M38	7B4 34B8
CPU_BSEL<1>	CPU_BSEL<1> - @m38_lib.M38	7B4 34A8
CPU_BSEL<2>	CPU_BSEL<2> - @m38_lib.M38	7B4 34A8
CPU_COMP<0>	CPU_COMP<0> - @m38_lib.M38	7B2
CPU_COMP<1>	CPU_COMP<1> - @m38_lib.M38	7B2
CPU_COMP<2>	CPU_COMP<2> - @m38_lib.M38	7B2
CPU_COMP<3>	CPU_COMP<3> - @m38_lib.M38	7B2
CPU_DCIN_SENSE	CPU_DCIN_SENSE - @m38_lib.M38	76D7
CPU_DPRSTP_L	CPU_DPRSTP_L - @m38_lib.M38	7B3 21C4 75C6
CPU_DPSLP_L	CPU_DPSLP_L - @m38_lib.M38	7B3 21C4
CPU_FERR_L	CPU_FERR_L - @m38_lib.M38	7C7 21C2
CPU_GTLREF	CPU_GTLREF - @m38_lib.M38	5D4 7B4
CPU_HS_ZH607	CPU_HS_ZH607 - @m38_lib.M38	9D4
CPU_HS_ZH608	CPU_HS_ZH608 - @m38_lib.M38	9D3 66A4 66A6 66B4 66B6
CPU_HS_ZH609	CPU_HS_ZH609 - @m38_lib.M38	9D3
CPU_HS_ZH610	CPU_HS_ZH610 - @m38_lib.M38	9D2
CPU_IGNNE_L	CPU_IGNNE_L - @m38_lib.M38	5C8 7C7 21C4
CPU_INIT_L	CPU_INIT_L - @m38_lib.M38	5C8 7D6 21C4
CPU_INTR	CPU_INTR - @m38_lib.M38	5C8 7C7 21C4
CPU_ISENSE_OUT_R	CPU_ISENSE_OUT_R - @m38_lib.M38	76D3
CPU_ISENSE_R_NEG	CPU_ISENSE_R_NEG - @m38_lib.M38	76D4
CPU_ISENSE_R_POS	CPU_ISENSE_R_POS - @m38_lib.M38	76D4
CPU_NMI	CPU_NMI - @m38_lib.M38	5C8 7C7 21C4
CPU_PROCHOT_L	CPU_PROCHOT_L - @m38_lib.M38	7C6 59A8 59C7
CPU_PSI_L	CPU_PSI_L - @m38_lib.M38	7A3 75C6
CPU_PWRGD	CPU_PWRGD - @m38_lib.M38	7B3 21C4
CPU_RCIN_L	CPU_RCIN_L - @m38_lib.M38	21C4
CPU_SENSE_I_R	CPU_SENSE_I_R - @m38_lib.M38	76D7
CPU_SMI_L	CPU_SMI_L - @m38_lib.M38	5C8 7C7 21C4
CPU_STPCLK_L	CPU_STPCLK_L - @m38_lib.M38	5C8 7C7 21C4
CPU_TEST1	CPU_TEST1 - @m38_lib.M38	7B4
CPU_TEST2	CPU_TEST2 - @m38_lib.M38	7B4
CPU_THERMD_EXT_N	CPU_THERMD_EXT_N - @m38_lib.M38	10B6
CPU_THERMD_EXT_P	CPU_THERMD_EXT_P - @m38_lib.M38	10B6
CPU_THERMD_N	CPU_THERMD_N - @m38_lib.M38	7C6 10C6
CPU_THERMD_P	CPU_THERMD_P - @m38_lib.M38	7C6 10C6
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @m38_lib.M38	21C2
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @m38_lib.M38	8B6 75A4
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @m38_lib.M38	8B6 75A4
CPU_VID<0>	CPU_VID<0> - @m38_lib.M38	8B7 75C7
CPU_VID<1>	CPU_VID<1> - @m38_lib.M38	8B7 75C7
CPU_VID<2>	CPU_VID<2> - @m38_lib.M38	8B7 75C7
CPU_VID<3>	CPU_VID<3> - @m38_lib.M38	8B7 75C7
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CPU_VID<5>	CPU_VID<5> - @m38_lib.M38	8B7 75C7
CPU_VID<6>	CPU_VID<6> - @m38_lib.M38	8B7 75D7
CPU_XDP_CLK_N	CPU_XDP_CLK_N - @m38_lib.M38 FSB_CLK_XDP_N - @m38_lib.M38	11B3 34B3 34B4 34C2
CPU_XDP_CLK_P	CPU_XDP_CLK_P - @m38_lib.M38 FSB_CLK_XDP_P - @m38_lib.M38	11B3 34B3 34B4 34C2
CRB_SV_DET	CRB_SV_DET - @m38_lib.M38	23B6 23C3
CRT_BLUE	CRT_BLUE - @m38_lib.M38 =PPVCORE_S0_NB - @m38_lib.M38	13B5 19D4 6D4 16C8 16D3 19B6 19D5 19D7
	CRT_BLUE_L - @m38_lib.M38	13B5 19D4
	CRT_IREF - @m38_lib.M38	13B5 19D4
	CRT_GREEN_L - @m38_lib.M38	13B5 19D4
	CRT_GREEN - @m38_lib.M38	13B5 19D4
	PP2V5_S0_NB_VCCA_CRTDAC - @m38_lib.M38	17D6 19D4
	CRT_RED - @m38_lib.M38	13B5 19D4
	CRT_RED_L - @m38_lib.M38	13B5 19D4
	PP1V05_S0 - @m38_lib.M38	6D6 34A8 34B8 34C7 81C2
	PP1V05_S0_SB_CPU_IO - @m38_lib.M38	6D4 21C1 21C1 24C3 25C3
	PP1V05_S0_NB_VTT - @m38_lib.M38	6D4 17D3 19B8 19D7
	PP1V05_S0_FSB_NB - @m38_lib.M38	5D4 6D4 12A7 12B7 12C2 19D7
	PP2V5_S0_NB_VCCA_CRTDAC - @m38_lib.M38	17D6 19D4
	PP1V05_S0 - @m38_lib.M38	6D6 34A8 34B8 34C7 81C2
	CRT_RED_L - @m38_lib.M38	13B5 19D4
	CRT_RED - @m38_lib.M38	13B5 19D4
	CRT_IREF - @m38_lib.M38	13B5 19D4
	CRT_GREEN_L - @m38_lib.M38	13B5 19D4
	CRT_GREEN - @m38_lib.M38	13B5 19D4
	CRT_BLUE_L - @m38_lib.M38	13B5 19D4
	=PPVCORE_S0_SB - @m38_lib.M38	6D4 24D3 25D3
	=PPVCORE_S0_NB - @m38_lib.M38	6D4 16C8 16D3 19B6 19D5 19D7
	=PP1V05_S0_SB_CPU_IO - @m38_lib.M38	6D4 21C1 21C1 24C3 25C3
	=PP1V05_S0_NB_VTT - @m38_lib.M38	6D4 17D3 19B8 19D7
	=PP1V05_S0_NB - @m38_lib.M38	6D4 19D7
	=PP1V05_S0_FSB_NB - @m38_lib.M38	5D4 6D4 12A7 12B7 12C2 19D7
	=PP1V05_S0_CPU - @m38_lib.M38	5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 9C8 11B3 11C5 59A1 59A3
CRT_DDC_CLK	CRT_DDC_CLK - @m38_lib.M38	13B5 19C4
	TP_CRT_DDC_CLK - @m38_lib.M38	19C5
CRT_DDC_DATA	CRT_DDC_DATA - @m38_lib.M38	13B5 19C4
	TP_CRT_DDC_DATA - @m38_lib.M38	19C5
DEBUG_RST_L	DEBUG_RST_L - @m38_lib.M38	6A7 60B6
DMI_IRCOMP_R	DMI_IRCOMP_R - @m38_lib.M38	22C2
DMI_N2S_N<0>	DMI_N2S_N<0> - @m38_lib.M38	5B8 14B4 22D2
DMI_N2S_N<1>	DMI_N2S_N<1> - @m38_lib.M38	14B4 22D2
DMI_N2S_N<2>	DMI_N2S_N<2> - @m38_lib.M38	14B4 22D2
DMI_N2S_N<3>	DMI_N2S_N<3> - @m38_lib.M38	14B4 22D2
DMI_N2S_P<0>	DMI_N2S_P<0> - @m38_lib.M38	5B8 14B4 22D2
DMI_N2S_P<1>	DMI_N2S_P<1> - @m38_lib.M38	14B4 22D2
DMI_N2S_P<2>	DMI_N2S_P<2> - @m38_lib.M38	14B4 22D2
DMI_N2S_P<3>	DMI_N2S_P<3> - @m38_lib.M38	14B4 22D2
DMI_S2N_N<0>	DMI_S2N_N<0> - @m38_lib.M38	5C7 14B4 22D2
DMI_S2N_N<1>	DMI_S2N_N<1> - @m38_lib.M38	14B4 22D2
DMI_S2N_N<2>	DMI_S2N_N<2> - @m38_lib.M38	14B4 22D2
DMI_S2N_N<3>	DMI_S2N_N<3> - @m38_lib.M38	14B4 22D2

DMI_S2N_P<0>	DMI_S2N_P<0> - @m38_lib.M38	5C7 14B4 22D2
DMI_S2N_P<1>	DMI_S2N_P<1> - @m38_lib.M38	14B4 22D2
DMI_S2N_P<2>	DMI_S2N_P<2> - @m38_lib.M38	14B4 22D2
DMI_S2N_P<3>	DMI_S2N_P<3> - @m38_lib.M38	14B4 22D2
DVI_DDC_CLK	DVI_DDC_CLK - @m38_lib.M38	97D2
DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @m38_lib.M38	97D3 97D5
DVI_DDC_DATA	DVI_DDC_DATA - @m38_lib.M38	97C2
DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @m38_lib.M38	97C3 97D5
DVI_HPD_UF	DVI_HPD_UF - @m38_lib.M38	97C3 97D5
ENET_C4106_2	ENET_C4106_2 - @m38_lib.M38	41D2
ENET_C4107_2	ENET_C4107_2 - @m38_lib.M38	41D2
ENET_C4117_1	ENET_C4117_1 - @m38_lib.M38	41B2
ENET_C4118_1	ENET_C4118_1 - @m38_lib.M38	41B2
ENET_CLK100M_PCIE_N	ENET_CLK100M_PCIE_N - @m38_lib.M38	5D5 34A4 34B2 41C5
ENET_CLK100M_PCIE_P	ENET_CLK100M_PCIE_P - @m38_lib.M38	5D5 34A4 34B2 41C5
ENET_CTRL12	ENET_CTRL12 - @m38_lib.M38 TP_ENET_CTRL12 - @m38_lib.M38	41C7 42B8 42B7
ENET_CTRL25	ENET_CTRL25 - @m38_lib.M38	41C7 42C6
ENET_GATED_RST_L	ENET_GATED_RST_L - @m38_lib.M38	41C5 42D2
ENET_LED_ACT_L	ENET_LED_ACT_L - @m38_lib.M38	41C8 43C3
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m38_lib.M38	41C8 43C3
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m38_lib.M38	41C8 43C3
ENET_LED_LINK_L	ENET_LED_LINK_L - @m38_lib.M38	41C8 43C3
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m38_lib.M38	41C7
ENET_MDI_N<0>	ENET_MDI_N<0> - @m38_lib.M38	41C2 43C7
ENET_MDI_N<1>	ENET_MDI_N<1> - @m38_lib.M38	41C2 43C7
ENET_MDI_N<2>	ENET_MDI_N<2> - @m38_lib.M38	41C2 43C7
ENET_MDI_N<3>	ENET_MDI_N<3> - @m38_lib.M38	41C2 43B7
ENET_MDI_P<0>	ENET_MDI_P<0> - @m38_lib.M38	41C2 43C7
ENET_MDI_P<1>	ENET_MDI_P<1> - @m38_lib.M38	41C2 43C7
ENET_MDI_P<2>	ENET_MDI_P<2> - @m38_lib.M38	41C2 43C7
ENET_MDI_P<3>	ENET_MDI_P<3> - @m38_lib.M38	41C2 43C7
ENET_MDI_R_N<0>	ENET_MDI_R_N<0> - @m38_lib.M38	43C6
ENET_MDI_R_N<1>	ENET_MDI_R_N<1> - @m38_lib.M38	43C6
ENET_MDI_R_N<2>	ENET_MDI_R_N<2> - @m38_lib.M38	43C6
ENET_MDI_R_N<3>	ENET_MDI_R_N<3> - @m38_lib.M38	43B6
ENET_MDI_R_P<0>	ENET_MDI_R_P<0> - @m38_lib.M38	43C6
ENET_MDI_R_P<1>	ENET_MDI_R_P<1> - @m38_lib.M38	43C6
ENET_MDI_R_P<2>	ENET_MDI_R_P<2> - @m38_lib.M38	43C6
ENET_MDI_R_P<3>	ENET_MDI_R_P<3> - @m38_lib.M38	43C6
ENET_PU_VDDO_TTL0	ENET_PU_VDDO_TTL0 - @m38_lib.M38	41C5
ENET_PU_VDDO_TTL1	ENET_PU_VDDO_TTL1 - @m38_lib.M38	41C5
ENET_RSET	ENET_RSET - @m38_lib.M38	41C7
ENET_RST_L	ENET_RST_L - @m38_lib.M38	6B7 42D3
ENET_VPD_CLK	ENET_VPD_CLK - @m38_lib.M38	41A2 41C4
ENET_VPD_DATA	ENET_VPD_DATA - @m38_lib.M38	41A2 41C4
ENET_XTALI	ENET_XTALI - @m38_lib.M38	41B5
ENET_XTALO	ENET_XTALO - @m38_lib.M38	41B5
F0_GATESLOWDN	F0_GATESLOWDN - @m38_lib.M38	65D5
F0_RCFEEDBK	F0_RCFEEDBK - @m38_lib.M38	65C5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @m38_lib.M38	65D6
F1_GATESLOWDN	F1_GATESLOWDN - @m38_lib.M38	65B5
F1_RCFEEDBK	F1_RCFEEDBK - @m38_lib.M38	65B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @m38_lib.M38	65B6
F2_GATESLOWDN	F2_GATESLOWDN - @m38_lib.M38	66D4
F2_RCFEEDBK	F2_RCFEEDBK - @m38_lib.M38	66C5
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @m38_lib.M38	66D5
FAN_0_OUT	FAN_0_OUT - @m38_lib.M38	65C4
FAN_0_PWR	FAN_0_PWR - @m38_lib.M38	65C4
FAN_1_CTL	FAN_1_CTL - @m38_lib.M38 FAN_RPM1 - @m38_lib.M38	65B7 65B7
FAN_1_OUT	FAN_1_OUT - @m38_lib.M38	65B4
FAN_1_PWR	FAN_1_PWR - @m38_lib.M38	65B3
FAN_2_CTL	FAN_2_CTL - @m38_lib.M38 FAN_RPM2 - @m38_lib.M38	66D7 66C7
FAN_2_OUT	FAN_2_OUT - @m38_lib.M38	66C4
FAN_2_PWR	FAN_2_PWR - @m38_lib.M38	66C3
FAN_TACH0	FAN_TACH0 - @m38_lib.M38	65C7
FAN_TACH1	FAN_TACH1 - @m38_lib.M38	65A7
FAN_TACH2	FAN_TACH2 - @m38_lib.M38	66C7
FB_A0_MF	FB_A0_MF - @m38_lib.M38	89A7
FB_A0_SEN	FB_A0_SEN - @m38_lib.M38	89A7
FB_A0_VREF0	FB_A0_VREF0 - @m38_lib.M38	89C7
FB_A0_VREF1	FB_A0_VREF1 - @m38_lib.M38	89C7
FB_A0_ZQ	FB_A0_ZQ - @m38_lib.M38	89A7
FB_A1_MF	FB_A1_MF - @m38_lib.M38	89A4
FB_A1_SEN	FB_A1_SEN - @m38_lib.M38	89A4
FB_A1_VREF0	FB_A1_VREF0 - @m38_lib.M38	89C4
FB_A1_VREF1	FB_A1_VREF1 - @m38_lib.M38	89C4
FB_A1_ZQ	FB_A1_ZQ - @m38_lib.M38	89A4
FB_A_BA<0>	FB_A_BA<0> - @m38_lib.M38	87D5 89A5 89A8
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FB_A_BA<2>	FB_A_BA<2> - @m38_lib.M38	87D5 89A5 89A8
FB_A_CAS_L<0>	FB_A_CAS_L<0> - @m38_lib.M38	5B6 87B5 89A8
FB_A_CAS_L<1>	FB_A_CAS_L<1> - @m38_lib.M38	5A6 87B5 89A5
FB_A_CKE<0>	FB_A_CKE<0> - @m38_lib.M38	5B6 87B5 89B8
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FB_A_CLK_P<0>	FB_A_CLK_P<0> - @m38_lib.M38	5B6 87B5 89B8
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FB_B_DQ<41>	FB_B_DQ<41> - @m38_lib.M38	87C3 90A3
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	SMC_CPU_INIT_3_L - @m38_lib.M38	58D5 59C6
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FW_A_TPB_P	FW_A_TPB_P - @m38_lib.M38	44C3 46C8
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	TP_FW_C_TPA_P - @m38_lib.M38	46B7
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	TP_FW_C_TPB_P - @m38_lib.M38	46A7
FW_PC0	FW_PC0 - @m38_lib.M38	44B3
FW_PC1	FW_PC1 - @m38_lib.M38	44B3
FW_PC2	FW_PC2 - @m38_lib.M38	44B3
FW_PORT0_TPA_FL_N	FW_PORT0_TPA_FL_N - @m38_lib.M38	46C2
FW_PORT0_TPA_FL_P	FW_PORT0_TPA_FL_P - @m38_lib.M38	46C2
FW_PORT0_TPB_FL_N	FW_PORT0_TPB_FL_N - @m38_lib.M38	46C2
FW_PORT0_TPB_FL_P	FW_PORT0_TPB_FL_P - @m38_lib.M38	46C2
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m38_lib.M38	46B2
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m38_lib.M38	46B2
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m38_lib.M38	46B2
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m38_lib.M38	46B2
FW_R0	FW_R0 - @m38_lib.M38	44C4
FW_R1	FW_R1 - @m38_lib.M38	44C4
FW_RESET_L	FW_RESET_L - @m38_lib.M38	44C2 44C3
FW_ROM_CLK	FW_ROM_CLK - @m38_lib.M38	44B4
FW_SE	FW_SE - @m38_lib.M38	44B3
FW_SM	FW_SM - @m38_lib.M38	44B3
FW_TEST	FW_TEST - @m38_lib.M38	44B3
FW_TPA_C<0>	FW_TPA_C<0> - @m38_lib.M38	46B8
FW_TPA_C<1>	FW_TPA_C<1> - @m38_lib.M38	46B7
FW_VP	FW_VP - @m38_lib.M38	46D4
FW_VP_R	FW_VP_R - @m38_lib.M38	46D5
FW_XTAL_X0	FW_XTAL_X0 - @m38_lib.M38	44D2 44D3
FW_XTAL_XI	FW_XTAL_XI - @m38_lib.M38	44D2 44D3
FW_XTAL_XR	FW_XTAL_XR - @m38_lib.M38	44D2
GATE_3V3_S3	GATE_3V3_S3 - @m38_lib.M38	83B4
GATE_5V_S3	GATE_5V_S3 - @m38_lib.M38	83C4
GND_AUDIO	GND_AUDIO - @m38_lib.M38	6C2 74D2
GND_AUDIO_CODEC	GND_AUDIO_CODEC - @m38_lib.M38	66A6 68B7 68D2 72B8 72C8 73A8 73C2 73D4 74A3 74A5 74A6 74A7 74B5 74B7 74C1 74C2 74C8 74D1
GND_AUDIO_MIC_CONN	GND_AUDIO_MIC_CONN - @m38_lib.M38	47C2 73C4
GND_AUDIO_SPKRAMP	GND_AUDIO_SPKRAMP - @m38_lib.M38	6C2 72B1 74D2
GND_AUDIO_SPKRAMP_PL ANE	GND_AUDIO_SPKRAMP_PLANE - @m38_lib.M38	72A6 72B2 72B6 72D2 72D8 74C2
GND_BNDI	GND_BNDI - @m38_lib.M38	47B2 47D2
GND_CHASSIS_AUDIO_EX TERNAL	GND_CHASSIS_AUDIO_EXTERNAL - @m38_lib.M38	6B2 73A8 73C7 73D8 74C1 74D2
	GND_CHASSIS_IO_LEFT - @m38_lib.M38	6B2
	GND_CHASSIS_USB - @m38_lib.M38	6B2 47A4 47B4 47C4
	GND_CHASSIS_IO_LEFT - @m38_lib.M38	6B2
GND_CHASSIS_AUDIO_IN TERNAL	GND_CHASSIS_AUDIO_INTERNAL - @m38_lib.M38	6A2 73C6
	GND_CHASSIS_BNDI - @m38_lib.M38	6A2 47C2 47C2 47D2
GND_CHASSIS_FIREWIRE	GND_CHASSIS_FIREWIRE - @m38_lib.M38	6B2 46A1 46C1
	GND_CHASSIS_RJ45 - @m38_lib.M38	6B2 43C6
	GND_CHASSIS_VGA - @m38_lib.M38	6B2 97C4
	GND_CHASSIS_RJ45 - @m38_lib.M38	6B2 43C6
	GND_CHASSIS_IO_RIGHT - @m38_lib.M38	6B1
GND_CPU_ISENSE_OPAMP	GND_CPU_ISENSE_OPAMP - @m38_lib.M38	76D3
GND_GPUVCORE_SGND	GND_GPUVCORE_SGND - @m38_lib.M38	85C7
GND_GPU_A2VSSN	GND_GPU_A2VSSN - @m38_lib.M38	93B7
GND_GPU_A2VSSQ	GND_GPU_A2VSSQ - @m38_lib.M38	93B7
GND_GPU_AVSSN	GND_GPU_AVSSN - @m38_lib.M38	93C7
GND_GPU_AVSSQ	GND_GPU_AVSSQ - @m38_lib.M38	93C7
GND_GPU_LPVSS	GND_GPU_LPVSS - @m38_lib.M38	93B7
GND_GPU_LVSSR	GND_GPU_LVSSR - @m38_lib.M38	93A7
GND_GPU_MPVSS	GND_GPU_MPVSS - @m38_lib.M38	91A5
GND_GPU_PCIE_PVSS	GND_GPU_PCIE_PVSS - @m38_lib.M38	84B8
GND_GPU_PVSS	GND_GPU_PVSS - @m38_lib.M38	91A5
GND_GPU_TPVSS	GND_GPU_TPVSS - @m38_lib.M38	93C7
GND_GPU_TXVSSR	GND_GPU_TXVSSR - @m38_lib.M38	93C7
GND_GPU_VSSRH0	GND_GPU_VSSRH0 - @m38_lib.M38	87A7
GND_GPU_VSSRH1	GND_GPU_VSSRH1 - @m38_lib.M38	87A4
GND_IMVP6_SGND	GND_IMVP6_SGND - @m38_lib.M38	75A4 75B6 75B8 75D7
GND_NB_VSSA_LVDS	GND_NB_VSSA_LVDS - @m38_lib.M38	17C6 19C2
	TP_GND_NB_VSSA_LVDS - @m38_lib.M38	19C1
GND_NEXT_TO_SMC	GND_NEXT_TO_SMC - @m38_lib.M38	59B2 76C2
GND_SMC_AVSS	GND_SMC_AVSS - @m38_lib.M38	58B2 58C4 59A3 59B3 76B2 76B6 76C2 76C5 85C1
GND_USB_PORT0	GND_USB_PORT0 - @m38_lib.M38	47D5
GND_USB_PORT1	GND_USB_PORT1 - @m38_lib.M38	47C5
GND_USB_PORT2	GND_USB_PORT2 - @m38_lib.M38	47A5
GPUBBN_D	GPUBBN_D - @m38_lib.M38	85A3
GPUBBN_D_RC	GPUBBN_D_RC - @m38_lib.M38	85A3
GPUBBN_FB	GPUBBN_FB - @m38_lib.M38	85A3
GPUBBN_SW	GPUBBN_SW - @m38_lib.M38	85A4
GPUBBP_ADJ	GPUBBP_ADJ - @m38_lib.M38	85B7
GPUBBP_ADJ_LOW	GPUBBP_ADJ_LOW - @m38_lib.M38	85A7
GPUBB_EN	GPUBB_EN - @m38_lib.M38	85A4 85A6 85B8
GPUBB_EN_L	GPUBB_EN_L - @m38_lib.M38	85A1 85A5 85B7
GPUISENS_NEG	GPUISENS_NEG - @m38_lib.M38	85D3
GPUISENS_NTC	GPUISENS_NTC - @m38_lib.M38	85D3
GPUISENS_POS	GPUISENS_POS - @m38_lib.M38	85D3
GPUISENS_RC	GPUISENS_RC - @m38_lib.M38	85D3
GPUVCORE_BOOT	GPUVCORE_BOOT - @m38_lib.M38	85C5
GPUVCORE_COMP	GPUVCORE_COMP - @m38_lib.M38	85C7
GPUVCORE_COMP_R	GPUVCORE_COMP_R - @m38_lib.M38	85C7
GPUVCORE_EN	GPUVCORE_EN - @m38_lib.M38	85C8 88A8
GPUVCORE_FB	GPUVCORE_FB - @m38_lib.M38	85C7
GPUVCORE_FB_LOW	GPUVCORE_FB_LOW - @m38_lib.M38	85C3
GPUVCORE_FCCM	GPUVCORE_FCCM - @m38_lib.M38	85C7
GPUVCORE_FSET	GPUVCORE_FSET - @m38_lib.M38	85C7
GPUVCORE_IOUT	GPUVCORE_IOUT - @m38_lib.M38	59C5 85D1
	SMC_GPU_ISENSE - @m38_lib.M38	58D5 59C6
GPUVCORE_ISEN

IMVP6_FB	IMVP6_FB - @m38_lib.M38	75A4 75B6
IMVP6_FB2	IMVP6_FB2 - @m38_lib.M38	75A4 75B6
IMVP6_FET_RC1	IMVP6_FET_RC1 - @m38_lib.M38	75A8 75C2
IMVP6_FET_RC2	IMVP6_FET_RC2 - @m38_lib.M38	75A6 75B2
IMVP6_ISEN1	IMVP6_ISEN1 - @m38_lib.M38	75A8 75C5
IMVP6_ISEN2	IMVP6_ISEN2 - @m38_lib.M38	75A6 75C5
IMVP6_LGATE1	IMVP6_LGATE1 - @m38_lib.M38	75A8 75C5
IMVP6_LGATE2	IMVP6_LGATE2 - @m38_lib.M38	75A6 75C5
IMVP6_NTC	IMVP6_NTC - @m38_lib.M38	75C7
IMVP6_NTC_R	IMVP6_NTC_R - @m38_lib.M38	75C7
IMVP6_OCSET	IMVP6_OCSET - @m38_lib.M38	75A4 75B5
IMVP6_PHASE1	IMVP6_PHASE1 - @m38_lib.M38	75A8 75C5
IMVP6_PHASE2	IMVP6_PHASE2 - @m38_lib.M38	75A6 75C5
IMVP6_RBIAS	IMVP6_RBIAS - @m38_lib.M38	75A4 75B6
IMVP6_RTN	IMVP6_RTN - @m38_lib.M38	75A4 75B5
IMVP6_SOFT	IMVP6_SOFT - @m38_lib.M38	75A4 75C6
IMVP6_UGATE1	IMVP6_UGATE1 - @m38_lib.M38	75A8 75C5
IMVP6_UGATE2	IMVP6_UGATE2 - @m38_lib.M38	75A6 75C5
IMVP6_VDIFF	IMVP6_VDIFF - @m38_lib.M38	75A4 75B6
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m38_lib.M38	75B7
IMVP6_VO	IMVP6_VO - @m38_lib.M38	75A4 75B4 76D5
IMVP6_VO_R	IMVP6_VO_R - @m38_lib.M38	75B4
IMVP6_VO_R_OA	IMVP6_VO_R_OA - @m38_lib.M38	76D4
IMVP6_VR_TT	IMVP6_VR_TT - @m38_lib.M38	75C7
IMVP6_VSEN	IMVP6_VSEN - @m38_lib.M38	75A4 75B5
IMVP6_VSUM	IMVP6_VSUM - @m38_lib.M38	75A4 75C5
IMVP6_VSUM_R1	IMVP6_VSUM_R1 - @m38_lib.M38	75A8 75C2
IMVP6_VSUM_R2	IMVP6_VSUM_R2 - @m38_lib.M38	75A6 75B2
IMVP6_VW	IMVP6_VW - @m38_lib.M38	75A4 75B6
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m38_lib.M38	75C6
IMVP_PGD_IN	IMVP_PGD_IN - @m38_lib.M38	75C6 77C7
IMVP_VID<0>	IMVP_VID<0> - @m38_lib.M38	75C6
IMVP_VID<1>	IMVP_VID<1> - @m38_lib.M38	75C7
IMVP_VID<2>	IMVP_VID<2> - @m38_lib.M38	75C7
IMVP_VID<3>	IMVP_VID<3> - @m38_lib.M38	75C7
IMVP_VID<4>	IMVP_VID<4> - @m38_lib.M38	75C7
IMVP_VID<5>	IMVP_VID<5> - @m38_lib.M38	75C7
IMVP_VID<6>	IMVP_VID<6> - @m38_lib.M38	75C7
IMVP_VR_ON	IMVP_VR_ON - @m38_lib.M38	58D7 75C6
INT_PIRQA_L	INT_PIRQA_L - @m38_lib.M38	22A7 26D2
INT_PIRQB_L	INT_PIRQB_L - @m38_lib.M38	22A7 26D2
INT_PIRQC_L	INT_PIRQC_L - @m38_lib.M38	22A7 26D2
INT_PIRQD_L	INT_PIRQD_L - @m38_lib.M38	22A7 26D2 44B5
INT_SERIRQ	INT_SERIRQ - @m38_lib.M38	23C8 58C7 60C3 67C6
ISENSE_CAL_EN	ISENSE_CAL_EN - @m38_lib.M38	58B7 76A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @m38_lib.M38	76B7
ISENSE_CAL_EN_LS12V	ISENSE_CAL_EN_LS12V - @m38_lib.M38	76B6
ISENSE_CAL_EN_L_R	ISENSE_CAL_EN_L_R - @m38_lib.M38	76A7
ITPRESET_L	ITPRESET_L - @m38_lib.M38	11B3
ITP_TDO	ITP_TDO - @m38_lib.M38	11B3
ITS_ALIVE	ITS_ALIVE - @m38_lib.M38	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @m38_lib.M38	6A8
ITS_RUNNING	ITS_RUNNING - @m38_lib.M38	6A6
JDREF	JDREF - @m38_lib.M38	68C4
KBC_MDE	KBC_MDE - @m38_lib.M38	58C2
LCD_PWM	LCD_PWM - @m38_lib.M38	94B1 94C3
LCD_PWM_R	LCD_PWM_R - @m38_lib.M38	94B2
LCD_PWREN_L	LCD_PWREN_L - @m38_lib.M38	94C8
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @m38_lib.M38	94C7
LED4300_1	LED4300_1 - @m38_lib.M38	43D2
LED4301_1	LED4301_1 - @m38_lib.M38	43D1
LED4302_1	LED4302_1 - @m38_lib.M38	43D1
LED4303_1	LED4303_1 - @m38_lib.M38	43D1
LED_PP1V05_S0_N	LED_PP1V05_S0_N - @m38_lib.M38	81A4
LED_PP1V05_S0_P	LED_PP1V05_S0_P - @m38_lib.M38	81A4
LED_PP1V5_S0_N	LED_PP1V5_S0_N - @m38_lib.M38	80A3
LED_PP1V5_S0_P	LED_PP1V5_S0_P - @m38_lib.M38	80A4
LED_PP1V8_S3_N	LED_PP1V8_S3_N - @m38_lib.M38	79A4
LED_PP1V8_S3_P	LED_PP1V8_S3_P - @m38_lib.M38	79A4
LPC_AD<0>	LPC_AD<0> - @m38_lib.M38	21D4 58D7 60C6 67C6
LPC_AD<1>	LPC_AD<1> - @m38_lib.M38	21D4 58D7 60C6 67C6
LPC_AD<2>	LPC_AD<2> - @m38_lib.M38	21D4 58C7 60C3 67C6
LPC_AD<3>	LPC_AD<3> - @m38_lib.M38	21D4 58C7 60C3 67C6
LPC_FRAME_L	LPC_FRAME_L - @m38_lib.M38	21C5 58C7 60C6 67C6
LVDS_A_CLK_N	LVDS_A_CLK_N - @m38_lib.M38	13D5 19D2
	TP_LVDS_A_CLK_N - @m38_lib.M38	19D1
LVDS_A_CLK_P	LVDS_A_CLK_P - @m38_lib.M38	13C5 19D2
	TP_LVDS_A_CLK_P - @m38_lib.M38	19D1
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m38_lib.M38	13C5 19D2
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m38_lib.M38	13C5 19D2
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m38_lib.M38	13C5 19D2
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m38_lib.M38	13C5 19D2
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m38_lib.M38	13C5 19D2
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m38_lib.M38	13C5 19D2
LVDS_BKLTCTL	LVDS_BKLTCTL - @m38_lib.M38	13D5 19C2
	TP_LVDS_BKLTCTL - @m38_lib.M38	19C1
LVDS_BKLTEN	LVDS_BKLTEN - @m38_lib.M38	13D5 19C2
	TP_LVDS_BKLTEN - @m38_lib.M38	19C1
LVDS_B_CLK_N	LVDS_B_CLK_N - @m38_lib.M38	13C5 19D2
	TP_LVDS_B_CLK_N - @m38_lib.M38	19D1
LVDS_B_CLK_P	LVDS_B_CLK_P - @m38_lib.M38	13C5 19D2
	TP_LVDS_B_CLK_P - @m38_lib.M38	19D1
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m38_lib.M38	13C5 19D2
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m38_lib.M38	13C5 19D2
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m38_lib.M38	13C5 19D2
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m38_lib.M38	13C5 19D2
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m38_lib.M38	13C5 19D2
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m38_lib.M38	13C5 19D2
LVDS_CLKCTLA	LVDS_CLKCTLA - @m38_lib.M38	13D5 19C2
	TP_LVDS_CLKCTLA - @m38_lib.M38	19C1
LVDS_CLKCTLB	LVDS_CLKCTLB - @m38_lib.M38	13D5 19C2
	TP_LVDS_CLKCTLB - @m38_lib.M38	19C1
LVDS_DDC_CLK	LVDS_DDC_CLK - @m38_lib.M38	13D5 19C2
	TP_LVDS_DDC_CLK - @m38_lib.M38	19C1
LVDS_DDC_DATA	LVDS_DDC_DATA - @m38_lib.M38	13D5 19C2
	TP_LVDS_DDC_DATA - @m38_lib.M38	19C1
LVDS_IBG	LVDS_IBG - @m38_lib.M38	13D5 19C2
	TP_LVDS_IBG - @m38_lib.M38	19C1
LVDS_L_CLK_N	LVDS_L_CLK_N - @m38_lib.M38	93A3 93D2 94A6
LVDS_L_CLK_P	LVDS_L_CLK_P - @m38_lib.M38	93A3 93D2 94A7
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @m38_lib.M38	93A3 93C2 94A6
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @m38_lib.M38	93A3 93C2 94A7
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @m38_lib.M38	93A3 93C2 94A6
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @m38_lib.M38	93A3 94A6
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @m38_lib.M38	93A3 93D2 94A7
LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @m38_lib.M38	93A3 93C2 94A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @m38_lib.M38	93A3 93C2 94A7
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @m38_lib.M38	93A3 94A7
LVDS_U_CLK_N	LVDS_U_CLK_N - @m38_lib.M38	93B3 94B6
LVDS_U_CLK_P	LVDS_U_CLK_P - @m38_lib.M38	93B3 94A7
LVDS_U_DATA_N<0>	LVDS_U_DATA_N<0> - @m38_lib.M38	93B3 94B7
LVDS_U_DATA_N<1>	LVDS_U_DATA_N<1> - @m38_lib.M38	93B3 94B7
LVDS_U_DATA_N<2>	LVDS_U_DATA_N<2> - @m38_lib.M38	93B3 94B7
LVDS_U_DATA_N<3>	LVDS_U_DATA_N<3> - @m38_lib.M38	93B3 94A6

LVDS_U_DATA_P<0>	LVDS_U_DATA_P<0> - @m38_lib.M38	93B3 94B6
LVDS_U_DATA_P<1>	LVDS_U_DATA_P<1> - @m38_lib.M38	93B3 94B6
LVDS_U_DATA_P<2>	LVDS_U_DATA_P<2> - @m38_lib.M38	93B3 94B6
LVDS_U_DATA_P<3>	LVDS_U_DATA_P<3> - @m38_lib.M38	93B3 94A7
LVDS_VDDEN	LVDS_VDDEN - @m38_lib.M38	13D5 19C2
	TP_LVDS_VDDEN - @m38_lib.M38	19C1
LVDS_VREFH	LVDS_VREFH - @m38_lib.M38	13D5 19C2
	TP_LVDS_VREFH - @m38_lib.M38	19C1
LVDS_VREFL	LVDS_VREFL - @m38_lib.M38	13D5 19C2
	TP_LVDS_VREFL - @m38_lib.M38	19C1
MEMVTT_VREF	MEMVTT_VREF - @m38_lib.M38	31B4
MEM_A_A<0>	MEM_A_A<0> - @m38_lib.M38	15C5 28B3
MEM_A_A<13..0>	MEM_A_A<13..0> - @m38_lib.M38	30C6
MEM_A_A<1>	MEM_A_A<1> - @m38_lib.M38	15C5 28B6
MEM_A_A<2>	MEM_A_A<2> - @m38_lib.M38	15C5 28B3
MEM_A_A<3>	MEM_A_A<3> - @m38_lib.M38	15B5 28B6
MEM_A_A<4>	MEM_A_A<4> - @m38_lib.M38	15B5 28B3
MEM_A_A<5>	MEM_A_A<5> - @m38_lib.M38	15B5 28B6
MEM_A_A<6>	MEM_A_A<6> - @m38_lib.M38	15B5 28C3
MEM_A_A<7>	MEM_A_A<7> - @m38_lib.M38	15B5 28C3
MEM_A_A<8>	MEM_A_A<8> - @m38_lib.M38	15B5 28C6
MEM_A_A<9>	MEM_A_A<9> - @m38_lib.M38	15B5 28C6
MEM_A_A<10>	MEM_A_A<10> - @m38_lib.M38	15B5 28B6
MEM_A_A<11>	MEM_A_A<11> - @m38_lib.M38	15B5 28C3
MEM_A_A<12>	MEM_A_A<12> - @m38_lib.M38	15B5 28C6
MEM_A_A<13>	MEM_A_A<13> - @m38_lib.M38	15B5 28B3
MEM_A_BS<0>	MEM_A_BS<0> - @m38_lib.M38	15D5 28B6
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @m38_lib.M38	30C6
MEM_A_BS<1>	MEM_A_BS<1> - @m38_lib.M38	15D5 28B3
MEM_A_BS<2>	MEM_A_BS<2> - @m38_lib.M38	15D5 28C6
MEM_A_CAS_L	MEM_A_CAS_L - @m38_lib.M38	15D5 28B6 30B6
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MEM_A_DM<1>	MEM_A_DM<1> - @m38_lib.M38	15D5 28D3
MEM_A_DM<2>	MEM_A_DM<2> - @m38_lib.M38	15D5 28C3
MEM_A_DM<3>	MEM_A_DM<3> - @m38_lib.M38	15C5 28C6
MEM_A_DM<4>	MEM_A_DM<4> - @m38_lib.M38	15C5 28B3
MEM_A_DM<5>	MEM_A_DM<5> - @m38_lib.M38	15C5 28A6
MEM_A_DM<6>	MEM_A_DM<6> - @m38_lib.M38	15C5 28A3
MEM_A_DM<7>	MEM_A_DM<7> - @m38_lib.M38	15C5 28A6
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MEM_A_DQ<3>	MEM_A_DQ<3> - @m38_lib.M38	15D7 28D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @m38_lib.M38	15D7 28D3
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MEM_A_DQ<58>	MEM_A_DQ<58> - @m38_lib.M38	15B7 28A6
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MEM_A_RAS_L	MEM_A_RAS_L - @m38_lib.M38	15B5 28B3 30B6
MEM_A_WE_L	MEM_A_WE_L - @m38_lib.M38	15B5 28B6 30B6
MEM_B_A<0>	MEM_B_A<0> - @m38_lib.M38	15C2 29B3 30B5
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MEM_B_A<2>	MEM_B_A<2> - @m38_lib.M38	15C2 29B3 30B5

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MEM_B_A<13>	MEM_B_A<13> - @m38_lib.M38	15B2 29B3 30A5
MEM_B_BS<0>	MEM_B_BS<0> - @m38_lib.M38	15D2 29B6
MEM_B_BS<2..0>	MEM_B_BS<2..0> - @m38_lib.M38	30A6
MEM_B_BS<1>	MEM_B_BS<1> - @m38_lib.M38	15D2 29B3
MEM_B_BS<2>	MEM_B_BS<2> - @m38_lib.M38	15D2 29C6
MEM_B_CAS_L	MEM_B_CAS_L - @m38_lib.M38	15D2 29B6 30A6
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MEM_B_DQ<24>	MEM_B_DQ<24> - @m38_lib.M38	15C4 29C6
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PCI_AD<6>	PCI_AD<6> - @m38_lib.M38	22B7 44C5
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PCI_AD<19>	PCI_AD<19> - @m38_lib.M38	22A7 44C6
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PCI_AD<31>	PCI_AD<31> - @m38_lib.M38	22A7 44B5
PCI_CLK_FW	PCI_CLK_FW - @m38_lib.M38	34C4 44B5
PCI_CLK_PORT80	PCI_CLK_PORT80 - @m38_lib.M38	34B4 60C3
PCI_CLK_SB	PCI_CLK_SB - @m38_lib.M38	5C8 22A6 34B4
PCI_CLK_SMC	PCI_CLK_SMC - @m38_lib.M38	34C4 58C7
PCI_CLK_TPM	PCI_CLK_TPM - @m38_lib.M38	34C4 67C6
PCI_C_BE_L<0>	PCI_C_BE_L<0> - @m38_lib.M38	22B6 44B5
PCI_C_BE_L<1>	PCI_C_BE_L<1> - @m38_lib.M38	22B6 44B5
PCI_C_BE_L<2>	PCI_C_BE_L<2> - @m38_lib.M38	22B6 44B5
PCI_C_BE_L<3>	PCI_C_BE_L<3> - @m38_lib.M38	22B6 44B5
PCI_DEVSEL_L	PCI_DEVSEL_L - @m38_lib.M38	22A6 26D2 44B5
PCI_FRAME_L	PCI_FRAME_L - @m38_lib.M38	22A7 26D2 44B5
PCI_GNT3_L	PCI_GNT3_L - @m38_lib.M38	22B4 44B5
PCI_IDSEL	PCI_IDSEL - @m38_lib.M38	44B5
PCI_IRDY_L	PCI_IRDY_L - @m38_lib.M38	22A6 26D2 44B5
PCI_LOCK_L	PCI_LOCK_L - @m38_lib.M38	22A6 26D2
PCI_PAR	PCI_PAR - @m38_lib.M38	22A6 44B5
PCI_PERR_L	PCI_PERR_L - @m38_lib.M38	22A6 26D2 44B5
PCI_PME_FW_L	PCI_PME_FW_L - @m38_lib.M38	22B5 44B5
PCI_REQ0_L	PCI_REQ0_L - @m38_lib.M38	22B6 26D2
PCI_REQ1_L	PCI_REQ1_L - @m38_lib.M38	22B6 26D2
PCI_REQ2_L	PCI_REQ2_L - @m38_lib.M38	22B6 26D2
PCI_REQ3_L	PCI_REQ3_L - @m38_lib.M38	22B4 26D2 44B5
PCI_RST_FW_L	PCI_RST_FW_L - @m38_lib.M38	44A7 44B5
PCI_RST_L	PCI_RST_L - @m38_lib.M38	22A6 44A8
PCI_SERR_L	PCI_SERR_L - @m38_lib.M38	22A6 26D2 44B5
PCI_STOP_L	PCI_STOP_L - @m38_lib.M38	22A6 26D2 44B5
PCI_TRDY_L	PCI_TRDY_L - @m38_lib.M38	22A6 26D2 44B5
PEG_COMP	PEG_COMP - @m38_lib.M38	13D3
PEG_D2R_C_N<0>	PEG_D2R_C_N<0> - @m38_lib.M38	84D3
PEG_D2R_C_N<1>	PEG_D2R_C_N<1> - @m38_lib.M38	84D3
PEG_D2R_C_N<2>	PEG_D2R_C_N<2> - @m38_lib.M38	84D3
PEG_D2R_C_N<3>	PEG_D2R_C_N<3> - @m38_lib.M38	84D3
PEG_D2R_C_N<4>	PEG_D2R_C_N<4> - @m38_lib.M38	84C3
PEG_D2R_C_N<5>	PEG_D2R_C_N<5> - @m38_lib.M38	84C3
PEG_D2R_C_N<6>	PEG_D2R_C_N<6> - @m38_lib.M38	84C3
PEG_D2R_C_N<7>	PEG_D2R_C_N<7> - @m38_lib.M38	84C3
PEG_D2R_C_N<8>	PEG_D2R_C_N<8> - @m38_lib.M38	84C3
PEG_D2R_C_N<9>	PEG_D2R_C_N<9> - @m38_lib.M38	84C3
PEG_D2R_C_N<10>	PEG_D2R_C_N<10> - @m38_lib.M38	84B3
PEG_D2R_C_N<11>	PEG_D2R_C_N<11> - @m38_lib.M38	84B3
PEG_D2R_C_N<12>	PEG_D2R_C_N<12> - @m38_lib.M38	84B3
PEG_D2R_C_N<13>	PEG_D2R_C_N<13> - @m38_lib.M38	84B3
PEG_D2R_C_N<14>	PEG_D2R_C_N<14> - @m38_lib.M38	84B3
PEG_D2R_C_N<15>	PEG_D2R_C_N<15> - @m38_lib.M38	84B3
PEG_D2R_C_P<0>	PEG_D2R_C_P<0> - @m38_lib.M38	84D3
PEG_D2R_C_P<1>	PEG_D2R_C_P<1> - @m38_lib.M38	84D3
PEG_D2R_C_P<2>	PEG_D2R_C_P<2> - @m38_lib.M38	84D3
PEG_D2R_C_P<3>	PEG_D2R_C_P<3> - @m38_lib.M38	84D3
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PEG_D2R_C_P<6>	PEG_D2R_C_P<6> - @m38_lib.M38	84C3
PEG_D2R_C_P<7>	PEG_D2R_C_P<7> - @m38_lib.M38	84C3
PEG_D2R_C_P<8>	PEG_D2R_C_P<8> - @m38_lib.M38	84C3
PEG_D2R_C_P<9>	PEG_D2R_C_P<9> - @m38_lib.M38	84C3
PEG_D2R_C_P<10>	PEG_D2R_C_P<10> - @m38_lib.M38	84B3
PEG_D2R_C_P<11>	PEG_D2R_C_P<11> - @m38_lib.M38	84B3
PEG_D2R_C_P<12>	PEG_D2R_C_P<12> - @m38_lib.M38	84B3
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PEG_D2R_C_P<14>	PEG_D2R_C_P<14> - @m38_lib.M38	84B3
PEG_D2R_C_P<15>	PEG_D2R_C_P<15> - @m38_lib.M38	84B3
PEG_D2R_N<0>	PEG_D2R_N<0> - @m38_lib.M38	13D3 84B1
PEG_D2R_N<1>	PEG_D2R_N<1> - @m38_lib.M38	13D3 84B1
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PEG_D2R_N<7>	PEG_D2R_N<7> - @m38_lib.M38	13D3 84C1
PEG_D2R_N<8>	PEG_D2R_N<8> - @m38_lib.M38	13D3 84C1
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PEG_D2R_N<13>	PEG_D2R_N<13> - @m38_lib.M38	13C3 84D1
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PEG_D2R_P<1>	PEG_D2R_P<1> - @m38_lib.M38	13C3 84B1
PEG_D2R_P<2>	PEG_D2R_P<2> - @m38_lib.M38	13C3 84B1
PEG_D2R_P<3>	PEG_D2R_P<3> - @m38_lib.M38	13C3 84B1
PEG_D2R_P<4>	PEG_D2R_P<4> - @m38_lib.M38	13C3 84B1
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PEG_D2R_P<7>	PEG_D2R_P<7> - @m38_lib.M38	13C3 84B1
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PEG_D2R_P<10>	PEG_D2R_P<10> - @m38_lib.M38	13C3 84C1
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PEG_D2R_C_N<0>	PEG_D2R_C_N<0> - @m38_lib.M38	13C3 84B5

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PEG_R2D_C_P<13>	PEG_R2D_C_P<13> - @m38_lib.M38	13A3 84D5
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PEG_R2D_P<3>	PEG_R2D_P<3> - @m38_lib.M38	84D4
PEG_R2D_P<4>	PEG_R2D_P<4> - @m38_lib.M38	84D4
PEG_R2D_P<5>	PEG_R2D_P<5> - @m38_lib.M38	84C4
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PEG_R2D_P<7>	PEG_R2D_P<7> - @m38_lib.M38	84C4
PEG_R2D_P<8>	PEG_R2D_P<8> - @m38_lib.M38	84C4
PEG_R2D_P<9>	PEG_R2D_P<9> - @m38_lib.M38	84C4
PEG_R2D_P<10>	PEG_R2D_P<10> - @m38_lib.M38	84B4
PEG_R2D_P<11>	PEG_R2D_P<11> - @m38_lib.M38	84B4
PEG_R2D_P<12>	PEG_R2D_P<12> - @m38_lib.M38	84B4
PEG_R2D_P<13>	PEG_R2D_P<13> - @m38_lib.M38	84B4
PEG_R2D_P<14>	PEG_R2D_P<14> - @m38_lib.M38	84B4
PEG_R2D_P<15>	PEG_R2D_P<15> - @m38_lib.M38	84B4
PEG_RESET_L	PEG_RESET_L - @m38_lib.M38	6B7 84A5
PLT_RST_L	PLT_RST_L - @m38_lib.M38	6C8 22A6
PM_BATLOW_L	PM_BATLOW_L - @m38_lib.M38	23C1 58B7
PM_BMBUSY_L	PM_BMBUSY_L - @m38_lib.M38	14B6 23C5
PM_CLKRUN_L	PM_CLKRUN_L - @m38_lib.M38	58B 23C8 44B5 58C5 60C6
		67C6
PM_DPRSLPVR	PM_DPRSLPVR - @m38_lib.M38	14B7 23C3 75C7
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @m38_lib.M38	14B7 58B7 59C5
	DIMM_OVERTEMP_L - @m38_lib.M38	28C3 29C3 59C6
PM_LAN_ENABLE	PM_LAN_ENABLE - @m38_lib.M38	23C3 58D7
PM_PWRBTN_L	PM_PWRBTN_L - @m38_lib.M38	23C3 58D7
PM_PWROK	PM_PWROK - @m38_lib.M38	77B7
PM_RI_L	PM_RI_L - @m38_lib.M38	23D5
PM_RSMRST_L	PM_RSMRST_L - @m38_lib.M38	23C1 58D7
PM_SB_PWROK	PM_SB_PWROK - @m38_lib.M38	23C3 26D6
PM_SLP_S3	PM_SLP_S3 - @m38_lib.M38	77D7 78B8 80C8 81C8
PM_SLP_S3_L	PM_SLP_S3_L - @m38_lib.M38	6C8 23C3 58C5 77D8 79A7
		88A6
	MEMVTT_EN - @m38_lib.M38	31B5 79A6
PM_SLP_S4	PM_SLP_S4 - @m38_lib.M38	77A7 77C7 79C8 83C6
PM_SLP_S4_L	PM_SLP_S4_L - @m38_lib.M38	23C3 58C5 77C8
PM_SLP_S5_L	PM_SLP_S5_L - @m38_lib.M38	23C3 58C5
PM_STPCPU_L	PM_STPCPU_L - @m38_lib.M38	23C8 33C4
PM_STPPCI_L	PM_STPPCI_L - @m38_lib.M38	23C8 33C4
PM_SUS_STAT_L	PM_SUS_STAT_L - @m38_lib.M38	23C5 58C5 60C3 67C6
PM_SYSRST_L	PM_SYSRST_L - @m38_lib.M38	5B8 23C5 26C3 58B7
PM_THRMTRIP_L	PM_THRMTRIP_L - @m38_lib.M38	7C6 14B6 21C2 59C7
PM_THRM_L	PM_THRM_L - @m38_lib.M38	10D3 23C8 58B7
POWER_BUTTON_L	POWER_BUTTON_L - @m38_lib.M38	5D1 59C8
PP0V9_S0_PGOOD	PP0V9_S0_PGOOD - @m38_lib.M38	77B8 79A2
PP1V2_S0_GPU_VDDPLL	PP1V2_S0_GPU_VDDPLL - @m38_lib.M38	91B6
PP1V05_S0_PGOOD	PP1V05_S0_PGOOD - @m38_lib.M38	77C8 81B2
PP1V5_S0_NB_3GPLL_F	PP1V5_S0_NB_3GPLL_F - @m38_lib.M38	19A5
PP1V5_S0_NB_VCC3G	PP1V5_S0_NB_VCC3G - @m38_lib.M38	17D6 19A3
PP1V5_S0_NB_VCCA_3GP	PP1V5_S0_NB_VCCA_3GPLL -	17D6 19A3
LL	@m38_lib.M38	
PP1V5_S0_NB_VCCA_DPL	PP1V5_S0_NB_VCCA_DPLLA -	17C6 19C4
LA	@m38_lib.M38	
	TP_NB_VCCA_DPLLA - @m38_lib.M38	19C5
PP1V5_S0_NB_VCCA_DPL	PP1V5_S0_NB_VCCA_DPLLB -	17C6 19C4
LB	@m38_lib.M38	
	TP_NB_VCCA_DPLLB - @m38_lib.M38	19C5
PP1V5_S0_NB_VCCA_HPL	PP1V5_S0_NB_VCCA_HPLL -	17C6 19C6
L	@m38_lib.M38	
PP1V5_S0_NB_VCCA_MPL	PP1V5_S0_NB_VCCA_MPLL -	17C6 19C6
L	@m38_lib.M38	
PP1V5_S0_NB_VCCD_QTV	PP1V5_S0_NB_VCCD_QTVDAC -	17B6 19A1
DAC	@m38_lib.M38	
	PP1V5_S0_NB_VCCD_TVDAC -	17C6 19B1
	@m38_lib.M38	
PP1V5_S0_PGOOD	PP1V5_S0_PGOOD - @m38_lib.M38	77C8 80B2
PP1V5_S0_SB_R	PP1V5_S0_SB_R - @m38_lib.M38	25A7
PP1V5_S0_SB_VCC1_5_B	PP1V5_S0_SB_VCC1_5_B - @m38_lib.M38	22C1 24D5 25B7
PP1V5_S0_SB_VCCDMIPL	PP1V5_S0_SB_VCCDMIPLL -	24B5 25A6
L	@m38_lib.M38	
PP1V8R2V0_S0_GPU_VDD	PP1V8R2V0_S0_GPU_VDDRH0 -	87A7
RH0	@m38_lib.M38	
PP1V8R2V0_S0_GPU_VDD	PP1V8R2V0_S0_GPU_VDDRH1 -	87B3
RH1	@m38_lib.M38	
PP1V8R3V3_S0_GPU_VDD	PP1V8R3V3_S0_GPU_VDDR4_F -	91B6
R4_F	@m38_lib.M38	

PP1V8R3V3_S0_GPU_VDD	PP1V8R3V3_S0_GPU_VDDR5_F -	91B6
R5_F	@m38_lib.M38	
PP1V8_FB_A0_VDDA0	PP1V8_FB_A0_VDDA0 - @m38_lib.M38	89D7
PP1V8_FB_A0_VDDA1	PP1V8_FB_A0_VDDA1 - @m38_lib.M38	89D7
PP1V8_FB_A1_VDDA0	PP1V8_FB_A1_VDDA0 - @m38_lib.M38	89D4
PP1V8_FB_A1_VDDA1	PP1V8_FB_A1_VDDA1 - @m38_lib.M38	89D4
PP1V8_FB_B0_VDDA0	PP1V8_FB_B0_VDDA0 - @m38_lib.M38	90D7
PP1V8_FB_B0_VDDA1	PP1V8_FB_B0_VDDA1 - @m38_lib.M38	90D7
PP1V8_FB_B1_VDDA0	PP1V8_FB_B1_VDDA0 - @m38_lib.M38	90D4
PP1V8_FB_B1_VDDA1	PP1V8_FB_B1_VDDA1 - @m38_lib.M38	90D4
PP1V8_S3_PGOOD	PP1V8_S3_PGOOD - @m38_lib.M38	79B2
PP2V5_S0_PGOOD	PP2V5_S0_PGOOD - @m38_lib.M38	77B8 77C5
PP2V5_ENET_CTAP	PP2V5_ENET_CTAP - @m38_lib.M38	43D7
PP2V5_S0_GPU_A2VDD	PP2V5_S0_GPU_A2VDD - @m38_lib.M38	93B7
PP2V5_S0_GPU_AVDD	PP2V5_S0_GPU_AVDD - @m38_lib.M38	93C7
PP2V5_S0_GPU_LPVDD	PP2V5_S0_GPU_LPVDD - @m38_lib.M38	93B7
PP2V5_S0_GPU_LVDDR	PP2V5_S0_GPU_LVDDR - @m38_lib.M38	93B7
PP2V5_S0_GPU_PVDD_F	PP2V5_S0_GPU_PVDD_F - @m38_lib.M38	91A6
PP2V5_S0_GPU_TPVDD	PP2V5_S0_GPU_TPVDD - @m38_lib.M38	93C7
PP2V5_S0_GPU_TXVDDR	PP2V5_S0_GPU_TXVDDR - @m38_lib.M38	93C7
PP2V5_S0_GPU_VDD1DI	PP2V5_S0_GPU_VDD1DI - @m38_lib.M38	93C8
PP2V5_S0_GPU_VDD2DI	PP2V5_S0_GPU_VDD2DI - @m38_lib.M38	93B8
PP3V3R12V_LCD_CONN	PP3V3R12V_LCD_CONN - @m38_lib.M38	94A6 94A6 94A7 94C5
PP3V3_AUDIO_SPDIF_EM	PP3V3_AUDIO_SPDIF_EMI -	73B7
I	@m38_lib.M38	
PP3V3_AUDIO_SPDIF_JA	PP3V3_AUDIO_SPDIF_JACK -	73B5
CK	@m38_lib.M38	
PP3V3_AVCC_SMC	PP3V3_AVCC_SMC - @m38_lib.M38	58D3
PP3V3_AVREF_SMC	PP3V3_AVREF_SMC - @m38_lib.M38	58D2 59A3
PP3V3_FW_ESD	PP3V3_FW_ESD - @m38_lib.M38	46A5 46A6 46B5 46C5 46D5
PP3V3_FW_ESD_F	PP3V3_FW_ESD_F - @m38_lib.M38	46A7
PP3V3_INTERCON	PP3V3_INTERCON - @m38_lib.M38	72C7
PP3V3_LCD_SW	PP3V3_LCD_SW - @m38_lib.M38	94C6
PP3V3_S0_CK410_VDD48	PP3V3_S0_CK410_VDD48 - @m38_lib.M38	33D5
PP3V3_S0_CK410_VDDA	PP3V3_S0_CK410_VDDA - @m38_lib.M38	33C6
PP3V3_S0_CK410_VDD_C	PP3V3_S0_CK410_VDD_CPU_SRC -	33D6
PU_SRC	@m38_lib.M38	
PP3V3_S0_CK410_VDD_P	PP3V3_S0_CK410_VDD_PCI -	33D5
CI	@m38_lib.M38	
PP3V3_S0_CK410_VDD_R	PP3V3_S0_CK410_VDD_REF -	33C5
EF	@m38_lib.M38	
PP3V3_S0_IMVP6_3V3	PP3V3_S0_IMVP6_3V3 - @m38_lib.M38	75D6
PP3V3_S5_FW_VDDA	PP3V3_S5_FW_VDDA - @m38_lib.M38	44D5 45C6
PP3V3_S5_SB_RTC	PP3V3_S5_SB_RTC - @m38_lib.M38	5D2 21D6 24B3 25A3 26D7
PP3V3_S0_2V5REG_R	PP3V3_S0_2V5REG_R - @m38_lib.M38	77D5
PP3V3_TPM_3VSB	PP3V3_TPM_3VSB - @m38_lib.M38	59C5 67C4
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @m38_lib.M38	68A2 68D2 74D8
PP5V_BNDI_LE340	PP5V_BNDI_LE340 - @m38_lib.M38	47D3
PP5V_S0_DDC	PP5V_S0_DDC - @m38_lib.M38	97D4
PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @m38_lib.M38	97D5
PP5V_S0_GPUVCORE_VCC	PP5V_S0_GPUVCORE_VCC - @m38_lib.M38	85D7 88D8
PP5V_S0_IMVP6_VDD	PP5V_S0_IMVP6_VDD - @m38_lib.M38	75D6
PP5V_S0_SB_V5REF	PP5V_S0_SB_V5REF - @m38_lib.M38	24D5 25D7
PP5V_S3_BNDI	PP5V_S3_BNDI - @m38_lib.M38	47B2 47D1
PP5V_S5_SB_V5REF_SUS	PP5V_S5_SB_V5REF_SUS - @m38_lib.M38	24D5 25C7
PP5V_USB2	PP5V_USB2 - @m38_lib.M38	47D7
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @m38_lib.M38	47D5
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @m38_lib.M38	47C5
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @m38_lib.M38	47B5
PP12V_AUD_SPKRAMP_PL	PP12V_AUD_SPKRAMP_PLANE -	72D5
ANE	@m38_lib.M38	
PP12V_L7502	PP12V_L7502 - @m38_lib.M38	76D7
PP12V_S5_CPU_REG	PP12V_S5_CPU_REG - @m38_lib.M38	75C3 75D4 75D7 76C8 76D6
PPFW_PORT0_VP	PPFW_PORT0_VP - @m38_lib.M38	46D2
PPFW_PORT0_VP_FL	PPFW_PORT0_VP_FL - @m38_lib.M38	46C2
PPFW_PORT1_VP	PPFW_PORT1_VP - @m38_lib.M38	46B2 46D1
PPFW_PORT1_VP_FL	PPFW_PORT1_VP_FL - @m38_lib.M38	46B2
PPFW_PORTS_VP	PPFW_PORTS_VP - @m38_lib.M38	46D3
PPVCORE_S0_GPU_MPVDD	PPVCORE_S0_GPU_MPVDD - @m38_lib.M38	91A6
PPVCORE_S0_GPU_VDDCI	PPVCORE_S0_GPU_VDDCI - @m38_lib.M38	86C7
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @m38_lib.M38	75D6
PPV_3V3_AUDIO_CODEC	PPV_3V3_AUDIO_CODEC - @m38_lib.M38	68D6
Q4201_3	Q4201_3 - @m38_lib.M38	42D6
R7504_1	R7504_1 - @m38_lib.M38	75A8 75C1
R7507_1	R7507_1 - @m38_lib.M38	75A6 75B1
R8599_2	R8599_2 - @m38_lib.M38	85C4
RSMRST_PWRGD	RSMRST_PWRGD - @m38_lib.M38	58D7 76D1
SATA_A_D2R_N	SATA_A_D2R_N - @m38_lib.M38	21B6 38A6
	TP_SATA_A_D2R_N - @m38_lib.M38	38A5
SATA_A_D2R_P	SATA_A_D2R_P - @m38_lib.M38	21B6 38A6
	TP_SATA_A_D2R_P - @m38_lib.M38	38A5
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @m38_lib.M38	21B6 38A6
	TP_SATA_A_R2D_N - @m38_lib.M38	38A5
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @m38_lib.M38	21B6 38A6
	TP_SATA_A_R2D_P - @m38_lib.M38	38A5
SATA_C_D2R_C_N	SATA_C_D2R_C_N - @m38_lib.M38	38B8
SATA_C_D2R_C_P	SATA_C_D2R_C_P - @m38_lib.M38	38B8
SATA_C_D2R_N	SATA_C_D2R_N - @m38_lib.M38	21B6 38B6
SATA_C_D2R_P	SATA_C_D2R_P - @m38_lib.M38	21B6 38B6
SATA_C_DET_L	SATA_C_DET_L - @m38_lib.M38	23D2 38B5
SATA_C_PWR_EN_L	SATA_C_PWR_EN_L - @m38

SMC_XDP_TRST_L_R	SMC_XDP_TRST_L_R - @m38_lib.M38	59A3
SMC_XTAL	SMC_XTAL - @m38_lib.M38	58C3 59B8
SMLINK<0>	SMLINK<0> - @m38_lib.M38	23D5
SMLINK<1>	SMLINK<1> - @m38_lib.M38	23D5
SMS_INT_L	SMS_INT_L - @m38_lib.M38	23C3 26C2 58B5
SMS_ONOFF_L	SMS_ONOFF_L - @m38_lib.M38	58A5 59B4
SMS_X_AXIS	SMS_X_AXIS - @m38_lib.M38	58B7 59B6
	NC_SMS_X_AXIS - @m38_lib.M38	59B5
SMS_Y_AXIS	SMS_Y_AXIS - @m38_lib.M38	58B7 59B6
	NC_SMS_Y_AXIS - @m38_lib.M38	59B5
SMS_Z_AXIS	SMS_Z_AXIS - @m38_lib.M38	58A7 59B6
	NC_SMS_Z_AXIS - @m38_lib.M38	59B5
SPARE_SRC3_N	SPARE_SRC3_N - @m38_lib.M38	34D2
SPARE_SRC3_P	SPARE_SRC3_P - @m38_lib.M38	34D2
SPARE_SRC7_N	SPARE_SRC7_N - @m38_lib.M38	34D2
SPARE_SRC7_P	SPARE_SRC7_P - @m38_lib.M38	34D2
SPI_ARB	SPI_ARB - @m38_lib.M38	22C6 58D5
SPI_CE_L	SPI_CE_L - @m38_lib.M38	22C6 58B5 63C7
SPI_HOLD_L	SPI_HOLD_L - @m38_lib.M38	63C4
SPI_SCLK	SPI_SCLK - @m38_lib.M38	22C6 58D5 63C7
SPI_SCLK_R	SPI_SCLK_R - @m38_lib.M38	63C4
SPI_SI	SPI_SI - @m38_lib.M38	22C6 58D5 63C1
SPI_SI_R	SPI_SI_R - @m38_lib.M38	63C3
SPI_SO	SPI_SO - @m38_lib.M38	22C6 58D5 63C1
SPI_SO_R	SPI_SO_R - @m38_lib.M38	63C3
SPI_WP_L	SPI_WP_L - @m38_lib.M38	63C4
SPKRAMP_MUTE	SPKRAMP_MUTE - @m38_lib.M38	72B5
SPKRAMP_SS	SPKRAMP_SS - @m38_lib.M38	72B4
SUS_CLK_SB	SUS_CLK_SB - @m38_lib.M38	23C3 59B5
	SMC_SUS_CLK - @m38_lib.M38	58C5 59B6
SV_SET_UP	SV_SET_UP - @m38_lib.M38	23B6 23C3 60B3
SW_RST_BTN_L	SW_RST_BTN_L - @m38_lib.M38	5D1 26C6
SW_RST_DEBNC	SW_RST_DEBNC - @m38_lib.M38	26C4
SYS_LED_DRV_C	SYS_LED_DRV_C - @m38_lib.M38	59D6
SYS_LED_DRV_K	SYS_LED_DRV_K - @m38_lib.M38	59D6
SYS_ONEWIRE	SYS_ONEWIRE - @m38_lib.M38	58B7 59B4
SYS_POWERFAIL_L	SYS_POWERFAIL_L - @m38_lib.M38	6D8 76D2
SYS_PWRUP_L	SYS_PWRUP_L - @m38_lib.M38	6C7
THERM_DX_N	THERM_DX_N - @m38_lib.M38	10B5 10C5
THERM_DX_P	THERM_DX_P - @m38_lib.M38	10B5 10C5
THRM_ALERT_L	THRM_ALERT_L - @m38_lib.M38	10D3
THRM_THM	THRM_THM - @m38_lib.M38	10C4
TMDS_CK_TERM	TMDS_CK_TERM - @m38_lib.M38	97C8
TMDS_CLK_N	TMDS_CLK_N - @m38_lib.M38	93C3 97C8
TMDS_CLK_P	TMDS_CLK_P - @m38_lib.M38	93C3 97C8
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @m38_lib.M38	97C4 97C7
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @m38_lib.M38	97C4 97C7
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @m38_lib.M38	97C4 97D7
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @m38_lib.M38	97C4 97D7
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @m38_lib.M38	97C7 97D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @m38_lib.M38	97C4 97D7
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @m38_lib.M38	97C4 97D7
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @m38_lib.M38	97C7 97D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @m38_lib.M38	93C3 97D8
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @m38_lib.M38	93C3 97D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @m38_lib.M38	93C3 97C8
TMDS_DATA_N<3>	TMDS_DATA_N<3> - @m38_lib.M38	93C3 95D6
TMDS_DATA_N<4>	TMDS_DATA_N<4> - @m38_lib.M38	93C3 95D6
TMDS_DATA_N<5>	TMDS_DATA_N<5> - @m38_lib.M38	93C3 95D6
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @m38_lib.M38	93C3 97D8
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @m38_lib.M38	93C3 97C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @m38_lib.M38	93C3 97C8
TMDS_DATA_P<3>	TMDS_DATA_P<3> - @m38_lib.M38	93C3 95D6
TMDS_DATA_P<4>	TMDS_DATA_P<4> - @m38_lib.M38	93C3 95D6
TMDS_DATA_P<5>	TMDS_DATA_P<5> - @m38_lib.M38	93C3 95D6
TPM_BADD	TPM_BADD - @m38_lib.M38	67C4
TPM_GPIO1	TPM_GPIO1 - @m38_lib.M38	59B5 67C6
TPM_GPIO2	TPM_GPIO2 - @m38_lib.M38	59B5 67C6
TPM_LRESET_L	TPM_LRESET_L - @m38_lib.M38	6B7 67B7
TPM_PP	TPM_PP - @m38_lib.M38	59A5 67C6
TPM_RST_L	TPM_RST_L - @m38_lib.M38	67B6
TPM_XTALI	TPM_XTALI - @m38_lib.M38	59B7 67C6
TPM_XTALO	TPM_XTALO - @m38_lib.M38	59B7 67C6
TP_ATI_ROMCS_L	TP_ATI_ROMCS_L - @m38_lib.M38	91A3
TP_AZ_DOCK_EN_L	TP_AZ_DOCK_EN_L - @m38_lib.M38	23C5
TP_AZ_DOCK_RST_L	TP_AZ_DOCK_RST_L - @m38_lib.M38	23C5
TP_CLK14P3M_SPARE	TP_CLK14P3M_SPARE - @m38_lib.M38	34C4
TP_CPU_A32_L	TP_CPU_A32_L - @m38_lib.M38	7C7
TP_CPU_A33_L	TP_CPU_A33_L - @m38_lib.M38	7B7
TP_CPU_A34_L	TP_CPU_A34_L - @m38_lib.M38	7B7
TP_CPU_A35_L	TP_CPU_A35_L - @m38_lib.M38	7B7
TP_CPU_A36_L	TP_CPU_A36_L - @m38_lib.M38	7B7
TP_CPU_A37_L	TP_CPU_A37_L - @m38_lib.M38	7B7
TP_CPU_A38_L	TP_CPU_A38_L - @m38_lib.M38	7B7
TP_CPU_A39_L	TP_CPU_A39_L - @m38_lib.M38	7B7
TP_CPU_APM0_L	TP_CPU_APM0_L - @m38_lib.M38	7B7
TP_CPU_APM1_L	TP_CPU_APM1_L - @m38_lib.M38	7B7
TP_CPU_CPUSLP_L	TP_CPU_CPUSLP_L - @m38_lib.M38	21C4
TP_CPU_EXTBREF	TP_CPU_EXTBREF - @m38_lib.M38	7B6
TP_CPU_HFPLL	TP_CPU_HFPLL - @m38_lib.M38	7B7
TP_CPU_SPARE0	TP_CPU_SPARE0 - @m38_lib.M38	7B6
TP_CPU_SPARE1	TP_CPU_SPARE1 - @m38_lib.M38	7B6
TP_CPU_SPARE2	TP_CPU_SPARE2 - @m38_lib.M38	7B6
TP_CPU_SPARE3	TP_CPU_SPARE3 - @m38_lib.M38	7B6
TP_CPU_SPARE4	TP_CPU_SPARE4 - @m38_lib.M38	7B6
TP_CPU_SPARE5	TP_CPU_SPARE5 - @m38_lib.M38	7B6
TP_CPU_SPARE6	TP_CPU_SPARE6 - @m38_lib.M38	7B6
TP_CPU_SPARE7	TP_CPU_SPARE7 - @m38_lib.M38	7B6
TP_FB_A_MA12	TP_FB_A_MA12 - @m38_lib.M38	87D5
TP_FB_A_ODT<0>	TP_FB_A_ODT<0> - @m38_lib.M38	87B5
TP_FB_A_ODT<1>	TP_FB_A_ODT<1> - @m38_lib.M38	87B5
TP_FB_B_MA12	TP_FB_B_MA12 - @m38_lib.M38	87D1
TP_FB_B_ODT<0>	TP_FB_B_ODT<0> - @m38_lib.M38	87B1
TP_FB_B_ODT<1>	TP_FB_B_ODT<1> - @m38_lib.M38	87B1
TP_FW_CNA	TP_FW_CNA - @m38_lib.M38	44B3
TP_FW_LKON	TP_FW_LKON - @m38_lib.M38	44B3
TP_FW_LPS	TP_FW_LPS - @m38_lib.M38	44B3
TP_FW_MPCIACT_L	TP_FW_MPCIACT_L - @m38_lib.M38	44B3
TP_FW_NANDTREE	TP_FW_NANDTREE - @m38_lib.M38	44B3
TP_FW_ROM_AD	TP_FW_ROM_AD - @m38_lib.M38	44B3
TP_FW_VAUX_PRES	TP_FW_VAUX_PRES - @m38_lib.M38	44B3
TP_LVDS_VBG	TP_LVDS_VBG - @m38_lib.M38	13D5
TP_MEM_A_A<14>	TP_MEM_A_A<14> - @m38_lib.M38	28C3
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @m38_lib.M38	28C3
TP_MEM_B_A<14>	TP_MEM_B_A<14> - @m38_lib.M38	5B4 29C3
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @m38_lib.M38	5B4 29C3
TP_NB_TESTIN_L	TP_NB_TESTIN_L - @m38_lib.M38	14D6
TP_NB_XOR_FSB2_H7	TP_NB_XOR_FSB2_H7 - @m38_lib.M38	14D6
TP_NB_XOR_LVDS_A34	TP_NB_XOR_LVDS_A34 - @m38_lib.M38	14C6
TP_NB_XOR_LVDS_A35	TP_NB_XOR_LVDS_A35 - @m38_lib.M38	14C6
TP_NB_XOR_LVDS_D27	TP_NB_XOR_LVDS_D27 - @m38_lib.M38	14C6
TP_NB_XOR_LVDS_D28	TP_NB_XOR_LVDS_D28 - @m38_lib.M38	14C6
TP_PCI_CLK_SPARE	TP_PCI_CLK_SPARE - @m38_lib.M38	5B4 34C4
TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m38_lib.M38	22B6
TP_PCI_GNT1_L	TP_PCI_GNT1_L - @m38_lib.M38	22B6
TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m38_lib.M38	22B6
TP_PCI_GNT4_L	TP_PCI_GNT4_L - @m38_lib.M38	22B6
TP_PCI_PME_L	TP_PCI_PME_L - @m38_lib.M38	22A6
TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m38_lib.M38	21C6
TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m38_lib.M38	21C6
TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m38_lib.M38	21D4
TP_SB_GPIO6	TP_SB_GPIO6 - @m38_lib.M38	23C5
TP_SB_GPIO23	TP_SB_GPIO23 - @m38_lib.M38	21D5
TP_SB_GPIO25_DO_NOT_USE	TP_SB_GPIO25_DO_NOT_USE - @m38_lib.M38	23C3
TP_SB_GPIO38	TP_SB_GPIO38 - @m38_lib.M38	23C3
TP_SB_RSVD9	TP_SB_RSVD9 - @m38_lib.M38	22A6
TP_SB_SATALED_L	TP_SB_SATALED_L - @m38_lib.M38	21C6
TP_SB_XOR_AD5	TP_SB_XOR_AD5 - @m38_lib.M38	22A7
TP_SB_XOR_AD9	TP_SB_XOR_AD9 - @m38_lib.M38	22A7
TP_SB_XOR_AE5	TP_SB_XOR_AE5 - @m38_lib.M38	22A7
TP_SB_XOR_AE9	TP_SB_XOR_AE9 - @m38_lib.M38	22A6
TP_SB_XOR_AG4	TP_SB_XOR_AG4 - @m38_lib.M38	22A7
TP_SB_XOR_AG8	TP_SB_XOR_AG8 - @m38_lib.M38	22A6
TP_SB_XOR_AH4	TP_SB_XOR_AH4 - @m38_lib.M38	22A7
TP_SB_XOR_AH8	TP_SB_XOR_AH8 - @m38_lib.M38	22A6
TP_SB_XOR_T5	TP_SB_XOR_T5 - @m38_lib.M38	21C6
TP_SB_XOR_U3	TP_SB_XOR_U3 - @m38_lib.M38	21C6
TP_SB_XOR_U5	TP_SB_XOR_U5 - @m38_lib.M38	21C6
TP_SB_XOR_U7	TP_SB_XOR_U7 - @m38_lib.M38	21C6
TP_SB_XOR_V3	TP_SB_XOR_V3 - @m38_lib.M38	21C6
TP_SB_XOR_V4	TP_SB_XOR_V4 - @m38_lib.M38	21C6
TP_SB_XOR_V6	TP_SB_XOR_V6 - @m38_lib.M38	21C6
TP_SB_XOR_V7	TP_SB_XOR_V7 - @m38_lib.M38	21C6
TP_SB_XOR_W1	TP_SB_XOR_W1 - @m38_lib.M38	21C6
TP_SB_XOR_W3	TP_SB_XOR_W3 - @m38_lib.M38	21C6
TP_SB_XOR_Y1	TP_SB_XOR_Y1 - @m38_lib.M38	21C6
TP_SB_XOR_Y2	TP_SB_XOR_Y2 - @m38_lib.M38	21C6
TP_U5999_P1	TP_U5999_P1 - @m38_lib.M38	59A7
TP_U5999_P13	TP_U5999_P13 - @m38_lib.M38	59A5
TP_U5999_P14	TP_U5999_P14 - @m38_lib.M38	59A5
TP_UB400_AG14	TP_UB400_AG14 - @m38_lib.M38	91A5
TP_UB900_J2	TP_UB900_J2 - @m38_lib.M38	89A7
TP_UB900_J3	TP_UB900_J3 - @m38_lib.M38	89A7
TP_UB950_J2	TP_UB950_J2 - @m38_lib.M38	89A4
TP_UB950_J3	TP_UB950_J3 - @m38_lib.M38	89A4
TP_U9000_J2	TP_U9000_J2 - @m38_lib.M38	90A7
TP_U9000_J3	TP_U9000_J3 - @m38_lib.M38	90A7
TP_U9050_J2	TP_U9050_J2 - @m38_lib.M38	90A4
TP_U9050_J3	TP_U9050_J3 - @m38_lib.M38	90A4
TSENSE_GPU_DXP	TSENSE_GPU_DXP - @m38_lib.M38	61C5
TSENSE_NB_DXP	TSENSE_NB_DXP - @m38_lib.M38	61B5
TSENSE_NB_GPU_DXN	TSENSE_NB_GPU_DXN - @m38_lib.M38	61B5
TV_DACA_OUT	TV_DACA_OUT - @m38_lib.M38	13C5 19B1
	TV_DACB_OUT - @m38_lib.M38	13C5 19B1
	TV_DACC_OUT - @m38_lib.M38	13C5 19B1
	TV_IRTNA - @m38_lib.M38	13C5 19B1
	TV_IRTNB - @m38_lib.M38	13C5 19B1
	TV_IRTNC - @m38_lib.M38	13C5 19B1
	TV_IREF - @m38_lib.M38	13C5 19B1
	PP3V3_S0_NB_VCCA_TVBG - @m38_lib.M38	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACC - @m38_lib.M38	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACB - @m38_lib.M38	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACA - @m38_lib.M38	17C6 19B1
	=PP1V5_S0_NB_TVDAC - @m38_lib.M38	6C4 19B2 19D7
	=PP1V5_S0_AIRPORT - @m38_lib.M38	6C4 53D3
	PP1V5_S0 - @m38_lib.M38	6C6 80C2
	=PP1V5_S0_SB - @m38_lib.M38	6C4 25A8 25C8
	=PP1V5_S0_SB_VCC1_5_A - @m38_lib.M38	6C4 24A3 25C1
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m38_lib.M38	6C4 24A3 25B1
	=PP1V5_S0_SB_VCCUSBPLL - @m38_lib.M38	6C4 24A5 25B6
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m38_lib.M38	6C4 24A5 25C6
	=PP1V5_S0_SB_VCCSATAPLL - @m38_lib.M38	6C4 24B5 25D6
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m38_lib.M38	6C4 24B5 25D6
	=PP1V5_S0_NB_3GPLL - @m38_lib.M38	6C4 19A6 19A6
	=PP1V5_S0_NB_PLL - @m38_lib.M38	6C4 19C8 19D7
	=PP1V5_S0_NB_VCCAUX - @m38_lib.M38	6C4 6C4 16D1 17B6 19A7 19D7
	=PP1V5_S0_NB_VCCD_HMPLL - @m38_lib.M38	6C4 17C6 19D7
	=PP1V5_S0_NB_PCIE - @m38_lib.M38	6C4 13D2 19D7
	=PP1V5_S0_CPU - @m38_lib.M38	6C4 8B6 8C5
	=PP1V5_S0_NB_TVDAC - @m38_lib.M38	6C4 19B2 19D7
	=PP1V5_S0_AIRPORT - @m38_lib.M38	6C4 53D3
	=PP1V5_S0_CPU - @m38_lib.M38	6C4 8B6 8C5
	=PP1V5_S0_AIRPORT - @m38_lib.M38	6C4 53D3
U600_3	U600_3 - @m38_lib.M38	6C7
U600_6	U600_6 - @m38_lib.M38	6B7
U600_8	U600_8 - @m38_lib.M38	6B7
U600_11	U600_11 - @m38_lib.M38	6A7
U2698_4	U2698_4 - @m38_lib.M38	26C4
U3100_VDDQ	U3100_VDDQ - @m38_lib.M38	31C5
U6100_VCC	U6100_VCC - @m38_lib.M38	61C4
U8595_1	U8595_1 - @m38_lib.M38	85D2
USB_AIRPORT_N	USB_AIRPORT_N - @m38_lib.M38	53B4
USB_AIRPORT_P	USB_AIRPORT_P - @m38_lib.M38	53B4
USB_A_N	USB_A_N - @m38_lib.M38	22C2 47D7
USB_A_OC_L	USB_A_OC_L - @m38_lib.M38	22C4 22D8 47B8 47B8
USB_A_P	USB_A_P - @m38_lib.M38	22C2 47C7
USB_B_N	USB_B_N - @m38_lib.M38	22C2 53B2
USB_B_OC_L	USB_B_OC_L - @m38_lib.M38	22C4 22D8 47B8
USB_B_P	USB_B_P - @m38_lib.M38	22C2 53B2
USB_CAMERA_N	USB_CAMERA_N - @m38_lib.M38	47B2
USB_CAMERA_P	USB_CAMERA_P - @m38_lib.M38	47B2
USB_C_N	USB_C_N - @m38_lib.M38	22C2 47B7
USB_C_OC_L	USB_C_OC_L - @m38_lib.M38	22C4 22D8 47B7 47B8
USB_C_P	USB_C_P - @m38_lib.M38	22C2 47B7
USB_D_N	USB_D_N - @m38_lib.M38	22C2 47B3
USB_D_OC_L	USB_D_OC_L - @m38_lib.M38	22C4 22D8 47B7
USB_D_P	USB_D_P - @m38_lib.M38	22C2 47B3
USB_E_N	USB_E_N - @m38_lib.M38	22C2 47A7
USB_E_OC_L	USB_E_OC_L - @m38_lib.M38	22C4 22D8 47B7
USB_E_P	USB_E_P - @m38_lib.M38	22C2 47A7
USB_F_N	USB_F_N - @m38_lib.M38	22C2 49C6
	USB_FLASH_N - @m38_lib.M38	49C5
USB_F_P	USB_F_P - @m38_lib.M38	22C2 49C6
	USB_FLASH_P - @m38_lib.M38	49C5
USB_G_N	USB_G_N - @m38_lib.M38	22C2 47A3
	USB_BT_N - @m38_lib.M38	47A3
USB_G_P	USB_G_P - @m38_lib.M38	22C2 47A3
	USB_BT_P - @m38_lib.M38	47A3
USB_H_N	USB_H_N - @m38_lib.M38	22C2 47C3
USB_H_P	USB_H_P - @m38_lib.M38	22C2 47C3
USB_IR_N	USB_IR_N - @m38_lib.M38	47C2
USB_IR_P	USB_IR_P - @m38_lib.M38	47C2
USB_PORT0_N	USB_PORT0_N - @m38_lib.M38	47D5
USB_PORT0_P	USB_PORT0_P - @m38_lib.M38	47C5
USB_PORT1_N	USB_PORT1_N - @m38_lib.M38	47B5
USB_PORT1_P	USB_PORT1_P - @m38_lib.M38	47B5
USB_PORT2_N	USB_PORT2_N - @m38_lib.M38	47A5
USB_PORT2_P	USB_PORT2_P - @m38_lib.M38	47A5
USB_RBIAS_PN	USB_RBIAS_PN - @m38_lib.M38	22C2
VGA_B	VGA_B - @m38_lib.M38	97B6 97C5
VGA_G	VGA_G - @m38_lib.M38	97A6 97C5
VGA_HSYNC	VGA_HSYNC - @m38_lib.M38	97A3 97C5
VGA_R	VGA_R - @m38_lib.M38	97A6 97C5
VGA_VSYNC	VGA_VSYNC - @m38_lib.M38	97A3 97C5
VMAIN_AVLBL	VMAIN_AVLBL - @m38_lib.M38	41C7
VOL_DOWN	VOL_DOWN - @m38_lib.M38	68A6 68C7
VOL_UP	VOL_UP - @m38_lib.M38	68A6 68C7
VREG_FB	VREG_FB - @m38_lib.M38	68A3
VR_PWRGD_CK410	VR_PWRGD_CK410 - @m38_lib.M38	23C5 26A8
VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m38_lib.M38	5C7 14B6 26D5 75C6
XDP_BPM_L<0>	XDP_BPM_L<0> - @m38_lib.M38	7C6 11B3
XDP_BPM_L<1>	XDP_BPM_L<1> - @m38_lib.M38	7C6 11B3
XDP_BPM_L<2>	XDP_BPM_L<2> - @m38_lib.M38	7C6 11B3
XDP_BPM_L<3>	XDP_BPM_L<3> - @m38_lib.M38	7C6 11B3
XDP_BPM_L<4>	XDP_BPM_L<4> - @m38_lib.M38	7C6 11B3
XDP_BPM_L<5>	XDP_BPM_L<5> - @m38_lib.M38	7C6 11B3
XDP_DBRESET_L	XDP_DBRESET_L - @m38_lib.M38	7C6 11B4 26B5
XDP_TCK	XDP_TCK - @m38_lib.M38	5D1 7A8 7C6 11B3 11B3 59A1 59A6
XDP_TDI	XDP_TDI - @m38_lib.M38	5D1 7B8 7C6 11B3 59B2
XDP_TDO	XDP_TDO - @m38_lib.M38	5D1 7C6 11B5 59A6
XDP_TMS	XDP_TMS - @m38_lib.M38	5D1 7B8 7C6 11B3 59B1
XDP_TRST_L	XDP_TRST_L - @m38_lib.M38	5D1 7C6 11B3 59A2
ZH701P1	ZH701P1 - @m38_lib.M38	6A3
ZH702P1	ZH702P1 - @m38_lib.M38	6A3
ZH703P1	ZH703P1 - @m38_lib.M38	6A3
ZH704P1	ZH704P1 - @m38_lib.M38	6B3

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C601	CAP_402	m38[6A3]
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C603	CAP_402	m38[6A3]
C604	CAP_402	m38[6A4]
C610	CAP_402	m38[6C7]
C699	CAP_P_CASE-C1	m38[6D7]
C0800	CAP_402	m38[8B5]
C0801	CAP_603	m38[8B5]
C900	CAP_805	m38[9B6]
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C1972	CAP_603	m38[19A4]
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C1976	CAP_402	m38[19A4]
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C1982	CAP_603	m38[19B8]
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C4503	CAP_603	m38[45C6]
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C4507	CAP_402	m38[45C5]
C4508	CAP_402	m38[45D5]
C4509	CAP_402	m38[45D5]
C4510	CAP_402	m38[45D5]
C4515	CAP_603	m38[45D6]
C4520	CAP_402	m38[45D5]
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C4523	CAP_402	m38[45D3]
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C4613	CAP_402	m38[46C4]
C4615	CAP_603-1	m38[46C2]
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C4620	CAP_402	m38[46B4]
C4621	CAP_402	m38[46B4]
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C4623	CAP_402	m38[46A4]
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C4626	CAP_402	m38[46A2]
C4650	CAP_402	m38[46C7]
C4654	CAP_402	m38[46B8]
C4660	CAP_402	m38[46C7]
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C4710	CAP_P_SMD2	m38[47D6]
C4712	CAP_402	m38[47D5]
C4713	CAP_402	m38[47D5]
C4720	CAP_P_SMD	m38[47C6]
C4722	CAP_402	m38[47C5]
C4723	CAP_402	m38[47C5]
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C4742	CAP_402	m38[47D2]
C4743	CAP_402	m38[47D1]
C4797	CAP_805-2	m38[47D3]
C4798	CAP_402	m38[47A2]
C4799	CAP_805-2	m38[47A2]
C4950	CAP_805-2	m38[49C4]
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C5301	CAP_402	m38[53B7]
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C5306	CAP_402	m38[53D4]
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C5308	CAP_402	m38[53C5]
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C5310	CAP_402	m38[53C4]
C5311	CAP_603	m38[53C3]
C5312	CAP_603	m38[53D4]
C5313	CAP_402	m38[53C5]
C5314	CAP_603	m38[53C4]
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C5801	CAP_402	m38[59B8]
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C6311	CAP_402	m38[63C2]
C6312	CAP_402	m38[63D3]
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C6501	CAP_805	m38[65D5]
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C6503	CAP_805	m38[65B5]
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C6505	CAP_P_6.3X11-TH-LF	m38[65B3]
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C6601	CAP_805	m38[66C5]
C6602	CAP_P_SM-LF	m38[66C3]
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C6651	CAP_402	m38[66A5]
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C6654	CAP_402	m38[66B4]
C6655	CAP_402	m38[66B2]
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C6704	CAP_402	m38[59B7]
C6705	CAP_402	m38[59B7]
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C6823	CAP_402	m38[68A4]
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C6836	CAP_402	m38[68D3]
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C7203	CAP_1210	m38[72D3]
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C7206	CAP_805	m38[72C6]
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C7208	CAP_603-1	m38[72C4]
C7209	CAP_805	m38[72B4]
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C7211	CAP_402	m38[72B2]
C7212	CAP_402	m38[72B2]
C7213	CAP_402	m38[72B2]
C7214	CAP_603	m38[72B5]
C7215	CAP_402	m38[72C6]
C7216	CAP_402	m38[72C6]
C7217	CAP_P_6.3X8-SM	m38[72D6]
C7218	CAP_603	m38[72D5]
C7219	CAP_603	m38[72D4]
C7220	CAP_402	m38[72B7]
C7221	CAP_402	m38[72B7]
C7223	CAP_1210	m38[72D3]
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C7303	CAP_402	m38[73D6]
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C7312	CAP_402	m38[73A6]
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C7314	CAP_402	m38[73A7]
C7315	CAP_402	m38[73A6]
C7317	CAP_402	m38[73B4]
C7318	CAP_805	m38[73B4]
C7321	CAP_402	m38[73C5]
C7322	CAP_402	m38[73C5]
C7323	CAP_402	m38[73A6]
C7324	CAP_402	m38[73A5]
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C7401	CAP_402	m38[74C4]
C7402	CAP_402	m38[74A4]
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C7404	CAP_P_CASE-B-SM	m38[74B6]
C7405	CAP_P_CASE-B-SM	m38[74C7]
C7406	CAP_P_CASE-B-SM	m38[74C6]
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C7408	CAP_402	m38[74D7]
C7409	CAP_402	m38[74B8]
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C7411	CAP_402	m38[74B8]
C7412	CAP_402	m38[74A8]
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C7414	CAP_402	m38[74A7]
C7415	CAP_402	m38[74A8]
C7416	CAP_402	m38[74A8]
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C7418	CAP_805	m38[74A5]
C7419	CAP_603-1	m38[74A4]
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C7423	CAP_402	m38[74A7]
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C7513	CAP_402	m38[75B7]
C7514	CAP_402	m38[75B8]
C7515	CAP_603	m38[75C4]
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C7518	CAP_P_SM-3	m38[75D2]
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C7527	CAP_603	m38[75C5]
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C7534	CAP_402	m38[75B5]
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C7712	CAP_402	m38[77C7]
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C7754	CAP_402	m38[77B6]
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C7756	CAP_805	m38[77B3]
C7757	CAP_402	m38[77A6]
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C7805	CAP_603	m38[78C4]
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C7810	CAP_402	m38[78B4]
C7811	CAP_402	m38[78B5]
C7813	CAP_1206	m38[78B4]
C7814	CAP_402	m38[78B5]
C7817	CAP_P_CASE-D2E-LF	m38[78B2]
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C7901	CAP_603	m38[79D5]
C7902	CAP_402	m38[79C5]
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C7906	CAP_402	m38[79C5]
C7907	CAP_402	m38[79C3]
C7908	CAP_402	m38[79C5]
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C7912	CAP_P_CASE-D2E-LF	m38[79C3]
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C7980	CAP_402	m38[79B3]
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C8108	CAP_402	m38[81C5]
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C8110	CAP_1210	m38[81D4]
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C8112	CAP_1210	m38[81D3]
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C8399	CAP_603	m38[83C4]
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C8672	CAP_402	m38[86B5]
C8673	CAP_402	m38[86B6]
C8674	CAP_402	m38[86B6]
C8675	CAP_402	m38[86B6]
C8676	CAP_402	m38[86B5]
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C8678	CAP_402	m38[86B5]
C8679	CAP_402	m38[86A6]
C8680	CAP_402	m38[86A6]
C8681	CAP_402	m38[86A6]
C8682	CAP_402	m38[86A5]
C8683	CAP_402	m38[86A5]
C8690	CAP_805	m38[86D5]
C8691	CAP_402	m38[86D5]
C8692	CAP_402	m38[86D5]
C8695	CAP_805	m38[86D2]
C8696	CAP_402	m38[86D3]
C8697	CAP_402	m38[86D3]
C8711	CAP_402	m38[87B7]
C8713	CAP_402	m38[87B7]
C8715	CAP_402	m38[87A7]
C8716	CAP_402	m38[87A6]
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C8723	CAP_402	m38[87B4]
C8725	CAP_402	m38[87A4]
C8726	CAP_402	m38[87A3]
C8900	CAP_805	m38[89D7]
C8901	CAP_402	m38[89D7]
C8902	CAP_402	m38[89D7]
C8903	CAP_402	m38[89D7]
C8904	CAP_402	m38[89D6]
C8910	CAP_402	m38[89D7]
C8915	CAP_402	m38[89D6]
C8920	CAP_805	m38[89C8]
C8921	CAP_402	m38[89C8]
C8922	CAP_402	m38[89C7]
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C8925	CAP_402	m38[89C7]
C8926	CAP_402	m38[89C6]
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C8933	CAP_402	m38[89C6]
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C8965	CAP_402	m38[89D3]
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C8972	CAP_402	m38[89C4]
C8973	CAP_402	m38[89C4]
C8974	CAP_402	m38[89C4]
C8975	CAP_402	m38[89C3]
C8976	CAP_402	m38[89C3]
C8981	CAP_402	m38[89C3]
C8983	CAP_402	m38[89C3]
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C9001	CAP_402	m38[90D7]
C9002	CAP_402	m38[90D7]
C9003	CAP_402	m38[90D7]
C9004	CAP_402	m38[90D6]
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C9015	CAP_402	m38[90D6]
C9020	CAP_805	m38[90C8]
C9021	CAP_402	m38[90C8]
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C9025	CAP_402	m38[90C7]
C9026	CAP_402	m38[90C6]
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C9033	CAP_402	m38[90C6]
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C9065	CAP_402	m38[90D3]
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C9071	CAP_402	m38[90C4]
C9072	CAP_402	m38[90C4]
C9073	CAP_402	m38[90C4]
C9074	CAP_402	m38[90C4]
C9075	CAP_402	m38[90C3]
C9076	CAP_402	m38[90C3]
C9081	CAP_402	m38[90C3]
C9083	CAP_402	m38[90C3]
C9100	CAP_805	m38[91C5]
C9101	CAP_402	m38[91C5]
C9102	CAP_402	m38[91C5]
C9103	CAP_402	m38[91C5]
C9110	CAP_805	m38[91C5]
C9111	CAP_402	m38[91C5]
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C9116	CAP_402	m38[91B5]
C9117	CAP_402	m38[91B5]
C9120	CAP_805	m38[91B5]
C9121	CAP_402	m38[91B5]
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C9125	CAP_805	m38[91B5]
C9126	CAP_402	m38[91B5]
C9127	CAP_402	m38[91B5]
C9130	CAP_805	m38[91A6]
C9131	CAP_402	m38[91A6]
C9132	CAP_402	m38[91A5]
C9135	CAP_805	m38[91A6]
C9136	CAP_402	m38[91A6]
C9137	CAP_402	m38[91A5]
C9140	CAP_805	m38[91A6]
C9141	CAP_402	m38[91A6]
C9142	CAP_402	m38[91A5]
C9191	CAP_402	m38[91D2]
C9300	CAP_805	m38[93C6]
C9301	CAP_402	m38[93C6]
C9302	CAP_402	m38[93C5]
C9305	CAP_805	m38[93C6]
C9306	CAP_402	m38[93C6]
C9307	CAP_402	m38[93C5]
C9310	CAP_805	m38[93C6]
C9311	CAP_402	m38[93C6]
C9312	CAP_402	m38[93C5]
C9315	CAP_805	m38[93B8]
C9316	CAP_402	m38[93B8]
C9317	CAP_402	m38[93B7]
C9320	CAP_805	m38[93B6]
C9321	CAP_402	m38[93B6]
C9322	CAP_402	m38[93B5]
C9325	CAP_805	m38[93B8]
C9326	CAP_402	m38[93B8]
C9327	CAP_402	m38[93B7]
C9330	CAP_805	m38[93B6]
C9331	CAP_402	m38[93B6]
C9332	CAP_402	m38[93B5]
C9340	CAP_805	m38[93A6]
C9341	CAP_402	m38[93A6]
C9342	CAP_402	m38[93A5]
C9345	CAP_805	m38[93A6]
C9346	CAP_402	m38[93A5]
C9347	CAP_402	m38[93A5]
C9400	CAP_603-1	m38[94C7]
C9401	CAP_402	m38[94C6]
C9410	CAP_402	m38[94C6]
C9420	CAP_1210	m38[94C5]
C9450	CAP_805	m38[94C2]
C9470	CAP_402	m38[94B2]
C9700	CAP_402	m38[97C8]
C9710	CAP_603	m38[97C3]
C9711	CAP_402	m38[97D3]
C9713	CAP_402	m38[97C2]
C9714	CAP_402	m38[97C2]
C9740	CAP_402	m38[97A7]
C9741	CAP_402	m38[97A6]
C9742	CAP_402	m38[97A6]
D2500	DIODE_SCHOT_SOT23	m38[25C8]
D2501	DIODE_SCHOT_SOT23	m38[25D8]
D2600	DIODE_SCHOT_SOT23	m38[26D8]
D2601	DIODE_SCHOT_SOT23	m38[26C8]
D4600	DIODE_SMC	m38[46D5]
D4690	ZENER_SOT23	m38[46A6]
D4700	DIODE_SCHOT_3P_A_SC-75	m38[47C5]
D4701	DIODE_SCHOT_3P_A_SC-75	m38[47B5]
D4702	DIODE_SCHOT_3P_A_SC-75	m38[47A5]
D4705	DIODE_SCHOT_3P_A_SC-75	m38[47C6]
D4706	DIODE_SCHOT_3P_A_SC-75	m38[47B6]
D4707	DIODE_SCHOT_3P_A_SC-75	m38[47A6]
D4900	DIODE_SCHOT_3P_A_SC-75	m38[49B4]
D6500	DIODE_SOT23	m38[65C4]
D6501	DIODE_SOT23	m38[65B4]
D6502	DIODE_SCHOT_SMB	m38[65C4]
D6503	DIODE_SCHOT_SMB	m38[65B4]
D6600	DIODE_SOT23	m38[66C4]
D6601	DIODE_SCHOT_SMB	m38[66C3]
D7500	DIODE_SCHOT_SMB	m38[75C3]
D7501	DIODE_SCHOT_SMB	m38[75B2]
D7599	DIODE_SOT23	m38[76D6]
D8520	DIODE_SCHOT_SMB	m38[85C3]
D9700	ZENER_CASE425	m38[97C1]
DP4610	DIODE_DUAL_6P_SOT-363	m38[46D4 46D3]
DP4611	DIODE_DUAL_6P_SOT-363	m38[46C4 46C3]
DP4620	DIODE_DUAL_6P_SOT-363	m38[46B4 46B3]
DP4621	DIODE_DUAL_6P_SOT-363	m38[46A4 46A3]
DZ7300	SUPPR_TRANSIENT_4P1_0405	m38[73C6]
DZ7301	SUPPR_TRANSIENT_4P1_0405	m38[73A5]
DZ7302	SUPPR_TRANSIENT_4P1_0405	m38[73A4]
DZ7303	SUPPR_TRANSIENT_4P1_0405	m38[73C5]
DZ7304	SUPPR_TRANSIENT_4P1_0405	m38[73C4]
F4600	FUSE_SM-LF	m38[46D2]
F4601	FUSE_SM-LF	m38[46D2]
F4602	FUSE_MINISMD-LF	m38[46D3]
F4701	FUSE_MINISMD-LF	m38[47D3]
F9710	FUSE_SM-LF	m38[97D5]
FL4610	FILTER_4P_2012	m38[46C3]
FL4620	FILTER_4P_2012	m38[46B3]
FL9740	FILTER_LC_SM-220MHZ-LF	m38[97B7]
FL9741	FILTER_LC_SM-220MHZ-LF	m38[97A7]
FL9742	FILTER_LC_SM-220MHZ-LF	m38[97A7]
FLE011	FILTER_4P_2012	m38[46C3]
FLE021	FILTER_4P_2012	m38[46B3]
GV3801	HOLE_VIA	m38[38A8]
GV3802	HOLE_VIA	m38[38A7]
GV3803	HOLE_VIA	m38[38A8]
GV3804	HOLE_VIA	m38[38A7]
GV3805	HOLE_VIA	m38[38A8]
GV3806	HOLE_VIA	m38[38A7]
GV3807	HOLE_VIA	m38[38A8]
GV3808	HOLE_VIA	m38[38A7]
J2	CON_2RTSM_125_SM-2MT-BLK-LF	m38[61B7]
J3	CON_2RTSM_125_SM-2MT-BLK-LF	m38[61B6]

J600	CON_M12RT_D_THA_M-RT-TH	m38[6D7]
J0700	CPU_YONAH_SKT_BGA	m38[7C3 7D7]
J0700	CPU_YONAH_SKT_BGA	m38[8D4 8D8]
J1000	CON_2RTSM_125_SM-2MT-BLK-LF	m38[10B7]
J1101	CON_F28RT_S2MT_SM_F-RT-SM	m38[11C2]
J2600	BATTERY_2P_TH	m38[26C8]
J2800	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m38[28D5]
J2900	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m38[29D5]
J2901	CON_F4ST_S2MT_SM_F-T-SM	m38[59C7]
J2903	CON_M2ST_S2MT_SM_M-S-T-SM	m38[59C8]
J4700	CON_F10ST_D_SMA_F-ST-SM	m38[47A2]
J4950	CON_M4RT_S2MT_SM_M-R-T-SM	m38[49C4]
J5300	CON_F52RT_D2MT_SM_F-RT-SM	m38[53C5]
J6000	CON_F30STSM_5047_SM1	m38[60B5]
J6500	CON_M4RT_S2MT_SM_M-R-T-SM	m38[65D3]
J6501	CON_M5RT_S2MT_SMA_M-RT-SM	m38[65B2]
J6600	CON_F4ST_S2MT_SM_F-S-T-SM	m38[66C2]
J6601	CON_M4RT_S2MT_SM_M-R-T-SM	m38[66B5]
J6602	CON_M4RT_S2MT_SM_M-R-T-SM	m38[66B3]
J7300	CON_F4ST_S4MT_TH1_F-ST-TH	m38[73D8]
J7301	CON_M7RT_S2MT_SM_M-R-T-SM	m38[73D1]
J7303	CON_F9ANG_S4MT_TH1_F-ANG-TH	m38[73B3]
J9401	CON_M4ST_S_SM_M-ST-SM	m38[94C2]
J9402	CON_F30ST_D_SM_F-ST-SM	m38[94B6]
J9410	CON_M4ST_S_SM_M-ST-SM	m38[94A3]
J9710	CON_DVI_F32ST_Q2MT_S-M_F-ST-SM	m38[97D5]
JC900	CON_M7ST_SATA_SM_M-S-T-SM	m38[38B8]
JC901	CON_F50ST_D2MT_SM_F-ST-SM	m38[38D2]
JD600	CON_RJ45_10ANG_S3MT_TH1_F-ANG-TH	m38[43C6]
JE000	CON_F6ST_S4MT_TH1_F-ST-TH	m38[46C2]
JE001	CON_F6ST_S4MT_TH1_F-ST-TH	m38[46B2]
JE310	CON_F4ST_USB_S3MT_TH_F-ST-TH	m38[47D4]
JE320	CON_F4ST_USB_S3MT_TH_F-ST-TH	m38[47B4]
JE330	CON_F4ST_USB_S3MT_TH_F-ST-TH	m38[47A4]
JE350	CON_M14RT_S2MT_SM_M-RT-SM	m38[47C1]
L1934	IND_0603	m38[19C7]
L1936	IND_0603	m38[19C7]
L1970	IND_1210	m38[19A5]
L1975	IND_0805	m38[19A5]
L2500	IND_SM-3	m38[25B8]
L2507	IND_1206	m38[25A7]
L3301	IND_0402	m38[33D7]
L3302	IND_0402	m38[33D3]
L4200	IND_SM	m38[42D7]
L4201	IND_SM	m38[42B7]
L4300	IND_SM	m38[43D7]
L4409	IND_0402	m38[44D6]
L4610	IND_1206-LF	m38[46D2]
L4620	IND_1206-LF	m38[46B2]
L4690	IND_SM-1	m38[46A6]
L4710	IND_SM	m38[47D6]
L4712	FILTER_4P_2012	m38[47C6]
L4720	IND_SM	m38[47C6]
L4722	FILTER_4P_2012	m38[47B6]
L4730	IND_SM	m38[47B6]
L4732	FILTER_4P_2012	m38[47A6]
L4740	IND_SM	m38[47D2]
L4742	FILTER_4P_2012	m38[47C2]
L4752	FILTER_4P_2012	m38[47B2]
L5300	FILTER_4P_2012	m38[53B3]
L6800	IND_0402	m38[68A5]
L6801	IND_0402	m38[68D6]
L7200	IND_SM-1	m38[72D6]
L7201	IND_0603	m38[72C2]
L7202	IND_0603	m38[72C2]
L7203	IND_0603	m38[72C3]
L7204	IND_0603	m38[72C3]
L7205	IND_0603	m38[72D6]
L7206	IND_0603	m38[72C6]
L7207	IND_0603	m38[72C6]
L7208	IND_0603	m38[72C6]
L7300	IND_SM	m38[73D7]
L7301	IND_SM	m38[73D7]
L7302	IND_SM	m38[73D7]
L7303	IND_SM	m38[73D7]
L7304	IND_SM	m38[73D5]
L7305	IND_SM	m38[73D5]
L7306	IND_SM	m38[73D5]
L7307	IND_SM	m38[73D5]
L7309	IND_SM	m38[73C6]
L7310	IND_SM	m38[73C6]
L7312	IND_SM	m38[73C4]
L7313	IND_SM	m38[73C4]
L7314	IND_SM	m38[73B7]
L7315	IND_SM	m38[73B7]
L7316	IND_SM	m38[73B7]
L7317	IND_SM	m38[73A7]
L7318	IND_SM	m38[73B7]
L7319	IND_SM	m38[73B7]
L7320	IND_SM	m38[73A7]
L7322	IND_SM	m38[73B5]
L7323	IND_SM	m38[73B5]
L7324	IND_SM	m38[73B5]
L7325	IND_SM	m38[73A5]
L7326	IND_SM	m38[73B5]
L7327	IND_SM	m38[73B5]
L7328	IND_SM	m38[73A5]
L7500	IND_SM	m38[75D1]
L7501	IND_SM	m38[75B2]
L7502	IND_TH-VERT-LF	m38[76D8]
L7700	IND_SM1-LF	m38[77C4]
L7750	IND_SM-LF	m38[77B4]
L7800	IND_3P_SM	m38[78B3]
L7900	IND_3P_SM	m38[79C3]
L8000	IND_3P_SM	m38[80C3]
L8100	IND_IHLP	m38[81C3]
L8400	IND_0402	m38[84B7]
L8520	IND_IHLP	m38[85C3]
L8585	IND_4P_2COIL_SDQ1215-0-SM	m38[85A3]
L8715	IND_0402	m38[87A7]
L8725	IND_0402	m38[87A4]
L8910	IND_0402	m38[89D7]
L8915	IND_0402	m38[89D7]
L8960	IND_0402	m38[89D4]
L8965	IND_0402	m38[89D4]
L9010	IND_0402	m38[90D7]
L9015	IND_0402	m38[90D7]
L9060	IND_0402	m38[90D4]
L9065	IND_0402	m38[90D4]
L9120	IND_0402	m38[91B6]
L9125	IND_0402	m38[91B6]
L9130	IND_0402	m38[91B7]
L9135	IND_0402	m38[91A7]
L9140	IND_0402	m38[91A7]
L9300	IND_0402	m38[93C7]
L9305	IND_0402	m38[93C7]
L9310	IND_0402	m38[93C7]
L9315	IND_0402	m38[93C7]
L9320	IND_0402	m38[93B7]
L9325	IND_0402	m38[93B7]
L9330	IND_0402	m38[93B7]
L9345	IND_0402	m38[93B7]
L9400	IND_SM	m38[94C6]
L9700	FILTER_4P_SM	m38[97D7]
L9701	FILTER_4P_SM	m38[97D7]
L9702	FILTER_4P_SM	m38[97C7]
L9703	FILTER_4P_SM	m38[97C7]
L9710	IND_SM-1	m38[97D5]
LED600	LED_2.0X1.25MM-SM	m38[6A7]
LED601	LED_2.0X1.25MM-SM	m38[6A8]
LED602	LED_2.0X1.25MM-SM	m38[6A7]
LED2901	LED_3X2MM-SM	m38[59D6]
LED3800	LED_2.0X1.25MM-SM	m38[38B3]
LED4300	LED_2.0X1.25MM-SM	m38[43D2]
LED4301	LED_2.0X1.25MM-SM	m38[43D2]
LED4302	LED_2.0X1.25MM-SM	m38[43D1]
LED4303	LED_2.0X1.25MM-SM	m38[43D1]
LED7000	LED_2.0X1.25MM-SM	m38[79A4]
LED8000	LED_2.0X1.25MM-SM	m38[80A4]
LED8100	LED_2.0X1.25MM-SM	m38[81A4]
PP5E1	PROBEPOINT_SM	m38[5B8]
PP5E2	PROBEPOINT_SM	m38[5B8]
PP6A0	PROBEPOINT_SM	m38[5A6]
PP6A1	PROBEPOINT_SM	m38[5A6]
PP6A2	PROBEPOINT_SM	m38[5A6]
PP6A3	PROBEPOINT_SM	m38[5A6]
PP6A4	PROBEPOINT_SM	m38[5A6]
PP6A5	PROBEPOINT_SM	m38[5A6]
PP6A6	PROBEPOINT_SM	m38[5A6]
PP6A7	PROBEPOINT_SM	m38[5A6]
PP6A8	PROBEPOINT_SM	m38[5A6]
PP6A9	PROBEPOINT_SM	m38[5A6]
PP6B0	PROBEPOINT_SM	m38[5A6]
PP6B1	PROBEPOINT_SM	m38[5A6]
PP6B2	PROBEPOINT_SM	m38[5A6]
PP6B3	PROBEPOINT_SM	m38[5A6]
PP6B4	PROBEPOINT_SM	m38[5A6]
PP6B5	PROBEPOINT_SM	m38[5A6]
PP6B6	PROBEPOINT_SM	m38[5A6]
PP6B7	PROBEPOINT_SM	m38[5A6]
PP6B8	PROBEPOINT_SM	m38[5A6]
PP6B9	PROBEPOINT_SM	m38[5A6]
PP6C0	PROBEPOINT_SM	m38[5A6]
PP6C1	PROBEPOINT_SM	m38[5A6]
PP6C2	PROBEPOINT_SM	m38[5A6]
PP6C3	PROBEPOINT_SM	m38[5A6]
PP6C4	PROBEPOINT_SM	m38[5C8]
PP6C5	PROBEPOINT_SM	m38[5C8]
PP6C6	PROBEPOINT_SM	m38[5C8]
PP6C7	PROBEPOINT_SM	m38[5C8]
PP6C8	PROBEPOINT_SM	m38[5C8]
PP6D0	PROBEPOINT_SM	m38[5C8]
PP6D1	PROBEPOINT_SM	m38[5C8]
PP6D2	PROBEPOINT_SM	m38[588]
PP6D3	PROBEPOINT_SM	m38[588]
PP6D4	PROBEPOINT_SM	m38[588]
PP6D5	PROBEPOINT_SM	m38[588]
PP6D6	PROBEPOINT_SM	m38[588]
PP6D7	PROBEPOINT_SM	m38[588]
PP6D8	PROBEPOINT_SM	m38[588]
PP6D9	PROBEPOINT_SM	m38[588]
PP6E0	PROBEPOINT_SM	m38[588]
PP6E1	PROBEPOINT_SM	m38[586]
PP600	PROBEPOINT_SM	m38[5D8]
PP601	PROBEPOINT_SM	m38[5D8]
PP602	PROBEPOINT_SM	m38[5D8]
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PP617	PROBEPOINT_SM	m38[5D8]
PP618	PROBEPOINT_SM	m38[5D8]
PP619	PROBEPOINT_SM	m38[5D8]
PP620	PROBEPOINT_SM	m38[5D8]
PP621	PROBEPOINT_SM	m38[5C8]
PP622	PROBEPOINT_SM	m38[5C8]
PP623	PROBEPOINT_SM	m38[5C8]
PP624	PROBEPOINT_SM	m38[5C8]
PP625	PROBEPOINT_SM	m38[5C8]
PP626	PROBEPOINT_SM	m38[5C8]
PP627	PROBEPOINT_SM	m38[5C8]
PP628	PROBEPOINT_SM	m38[5C8]
PP629	PROBEPOINT_SM	m38[5C8]
PP630	PROBEPOINT_SM	m38[5C8]
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PP634	PROBEPOINT_SM	m38[5D6]
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PP639	PROBEPOINT_SM	m38[5D6]
PP640	PROBEPOINT_SM	m38[5D6]
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PP653	PROBEPOINT_SM	m38[5C6]
PP654	PROBEPOINT_SM	m38[5C6]
PP655	PROBEPOINT_SM	m38[5C6]
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PP678	PROBEPOINT_SM	m38[5B6]
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PP697	PROBEPOINT_SM	m38[5B6]
PP698	PROBEPOINT_SM	m38[5B6]
PP699	PROBEPOINT_SM	m38[5B6]
PP700	TP_SM-TP50-TOP	m38[5D3]
PP701	TP_SM-TP50-TOP	m38[5D3]
PP702	TP_SM-TP50-TOP	m38[5D3]
PP1200	TP_SM-TP50-TOP	m38[5D3]
PP1201	TP_SM-TP50-TOP	m38[5D3]
PP1202	TP_SM-TP50-TOP	m38[5D3]
PP2800	TP_SM-TP50-TOP	m38[5C3]
PP2801	TP_SM-TP50-TOP	m38[5C3]
PP2802	TP_SM-TP50-TOP	m38[5C3]
PP4100	PROBEPOINT_SM	m38[5D4]
PP4101	PROBEPOINT_SM	m38[5D4]
PP8400	PROBEPOINT_SM	m38[5C5]
PP8401	PROBEPOINT_SM	m38[5C5]
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PP8701	PROBEPOINT_SM	m38[5D5]
PP8702	PROBEPOINT_SM	m38[5D5]
PP8703	PROBEPOINT_SM	m38[5D5]
PP8704	PROBEPOINT_SM	m38[5D5]
PP8705	PROBEPOINT_SM	m38[5D5]
PP8706	PROBEPOINT_SM	m38[5D5]
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PP8709	PROBEPOINT_SM	m38[5D5]
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PP8715	PROBEPOINT_SM	m38[5D5]
PP8716	PROBEPOINT_SM	m38[5D5]
PP8720	PROBEPOINT_SM	m38[5D5]
PP8721	PROBEPOINT_SM	m38[5D5]
PP8722	PROBEPOINT_SM	m38[5D5]
PP8723	PROBEPOINT_SM	m38[5C5]
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PP8736	PROBEPOINT_SM	m38[5C5]
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PP8902	PROBEPOINT_SM	m38[5B5]
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PP8905	PROBEPOINT_SM	m38[5B5]
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PP8915	PROBEPOINT_SM	m38[5A5]
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PP9034	PROBEPOINT_SM	m38[5A4]
PP9035	PROBEPOINT_SM	m38[5A4]
PP9036	PROBEPOINT_SM	m38[5A4]
Q4200	TRA_2N7002_SOT23-LF	m38[42D2]
Q4201	TRA_PBSS5540Z_SOT223	m38[42C6]
Q4400	TRA_SINGLE_MOSFET_NC_HN_SOT23	m38[44A7]
Q5900	TRA_FDV301N_SOT23-LF	m38[59D7]
Q5901	TRA_2N7002DW_SOT-363	m38[59C7 59C7]
Q5902	TRA_2N7002DW_SOT-363	m38[59B1 59B2]
Q5903	TRA_DUAL_MMDT3904_SOT-363-LF	m38[59A2 59A1]
Q5910	TRA_SINGLE_MOSFET_PC_HN_SOT-23	m38[59A4]
Q5911	TRA_2N7002_SOT23-LF	m38[59A4]
Q6500	TRA_NTHS5443T1_1206A-03-LF	m38[65D4]
Q6502	TRA_2N7002DW_SOT-363	m38[65D8 65D6]
Q6503	TRA_NTHS5443T1_1206A-03-LF	m38[65B4]
Q6505	TRA_2N7002DW_SOT-363	m38[65C8 65B6]
Q6600	TRA_NTHS5443T1_1206A-03-LF	m38[66D4]
Q6602	TRA_2N7002DW_SOT-363	m38[66D8 66C5]
Q7200	TRA_2N7002DW_SOT-363	m38[72B6 72B7]
Q7400	TRA_2N7002DW_SOT-363	m38[74B3 74B3]
Q7401	TRA_2N7002_SOT23-LF	m38[74C3]
Q7402	TRA_2N7002DW_SOT-363	m38[74B2 74B2]
Q7500	TRA_HAT2168H_LFPAK	m38[75D3]
Q7501	TRA_HAT2165H_LFPAK	m38[75D3]
Q7502	TRA_HAT2168H_LFPAK	m38[75C3]
Q7503	TRA_HAT2165H_LFPAK	m38[75B3]
Q7504	TRA_HAT2165H_LFPAK	m38[75D3]
Q7505	TRA_HAT2165H_LFPAK	m38[75B3]
Q7570	TRA_HAT2168H_LFPAK	m38[75D2]
Q7572	TRA_HAT2168H_LFPAK	m38[75C3]
Q7639	TRA_2N7002_SOT23-LF	m38[76A7]
Q7640	TRA_SINGLE_MOSFET_PC_HN_SOT-23	m38[76A6]
Q7641	TRA_FDC796N_SUPERSOT-6	m38[76A5]
Q7642	TRA_FDC796N_SUPERSOT-6	m38[76A4]
Q7701	TRA_SI3446DV_TSOP-LF	m38[77A3]
Q7703	TRA_2N7002DW_SOT-363	m38[77C7 77D7]
Q7799	TRA_2N7002_SOT23-LF	m38[77A6]
Q7800	TRA_NTD60N02R_CASE369-LF	m38[78C4]
Q7801	TRA_NTD60N02R_CASE369-LF	m38[78B4]
Q7802	TRA_2N7002_SOT23-LF	m38[78B7]
Q7900	TRA_NTD60N02R_CASE369-LF	m38[79D4]
Q7901	TRA_NTD60N02R_CASE369-LF	m38[79C4]
Q7902	TRA_2N7002_SOT23-LF	m38[79C7]
Q8000	TRA_NTD60N02R_CASE369-LF	m38[80D4]
Q8001	TRA_NTD60N02R_CASE369-LF	m38[80C4]
Q8003	TRA_2N7002_SOT23-LF	m38[80C7]
Q8102	TRA_NTD60N02R_CASE369-LF	m38[81D4]

Q8103	TRA_NTD60N02R_CASE369-LF	m38[81C4]
Q8104	TRA_2N7002_SOT23-LF	m38[81C7]
Q8300	TRA_IRF7413_SO-8	m38[83C4]
Q8301	TRA_IRF7413_SO-8	m38[83B4]
Q8302	TRA_2N7002DW_SOT-363	m38[83B5]
Q8303	TRA_2N7002DW_SOT-363	m38[83C5]
Q8520	TRA_HAT2168H_LFPAK	m38[85D4]
Q8521	TRA_HAT2165H_LFPAK	m38[85C4]
Q8522	TRA_HAT2165H_LFPAK	m38[85C5]
Q8523	TRA_2N7002DW_SOT-363	m38[85B3 85B2]
Q8554	TRA_2N7002_SOT23-LF	m38[85A8]
Q8570	TRA_2N7002_SOT23-LF	m38[85A5]
Q8575	TRA_FDC796N_SUPERSOT-6	m38[85B6]
Q8576	TRA_FDC796N_SUPERSOT-6	m38[85A2]
Q9400	TRA_SI3443DV_TSOP-LF	m38[94C7]
Q9401	TRA_2N7002_SOT23-LF	m38[94C7]
Q9711	TRA_2N7002DW_SOT-363	m38[97D2 97C2]
R75A0	RES_402	m38[75C7]
R85A0	RES_402	m38[85D1]
R600	RES_603	m38[6A7]
R601	RES_402	m38[6D8]
R602	RES_603	m38[6A8]
R603	RES_402	m38[6B1]
R605	RES_603	m38[6A7]
R611	RES_402	m38[6B7]
R612	RES_402	m38[6B7]
R614	RES_402	m38[6B7]
R615	RES_402	m38[6B7]
R616	RES_402	m38[6A7]
R617	RES_402	m38[6A7]
R618	RES_402	m38[6C7]
R619	RES_402	m38[6B7]
R0702	RES_402	m38[7D6]
R0703	RES_402	m38[7C6]
R0704	RES_402	m38[7C5]
R0705	RES_402	m38[7B4]
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R0707	RES_402	m38[7A4]
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R0716	RES_402	m38[7B1]
R0717	RES_402	m38[7B1]
R0718	RES_402	m38[7B1]
R0719	RES_402	m38[7B1]
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R0722	RES_402	m38[7A7]
R0730	RES_402	m38[7A4]
R0802	RES_402	m38[8B7]
R0803	RES_402	m38[8A7]
R1000	RES_402	m38[10D3]
R1001	RES_402	m38[10D3]
R1002	RES_402	m38[10C6]
R1005	RES_402	m38[10D3]
R1017	RES_402	m38[10C6]
R1018	RES_402	m38[10B6]
R1019	RES_402	m38[10B6]
R1100	RES_402	m38[11B5]
R1101	RES_402	m38[11C5]
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R1103	RES_402	m38[11C5]
R1104	RES_402	m38[11B5]
R1106	RES_402	m38[11A3]
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R1410	RES_402	m38[14C3]
R1411	RES_402	m38[14C3]
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R1440	RES_402	m38[14D6]
R1441	RES_402	m38[14D6]
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R1983	RES_402	m38[19B8]
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R2060	RES_402	m38[20A4]
R2075	RES_402	m38[20C7]
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R2079	RES_402	m38[20B7]
R2085	RES_402	m38[20C4]
R2100	RES_402	m38[21C3]
R2101	RES_402	m38[21C4]
R2105	RES_402	m38[21D6]
R2107	RES_402	m38[21C2]
R2108	RES_402	m38[21C2]
R2110	RES_402	m38[21C2]
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R2203	RES_402	m38[22C2]
R2204	RES_402	m38[22C2]
R2205	RES_402	m38[22C6]
R2206	RES_402	m38[22C5]
R2207	RES_402	m38[22C5]
R2211	RES_402	m38[22B3]
R2222	RES_402	m38[22D6]
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R2226	RES_402	m38[22D5]
R2250	RES_402	m38[22D7]
R2251	RES_402	m38[22D6]
R2252	RES_402	m38[47B8]
R2253	RES_402	m38[47B8]
R2254	RES_402	m38[47B8]
R2255	RES_402	m38[22D7]
R2298	RES_402	m38[22B5]
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R2302	RES_402	m38[23D3]
R2303	RES_402	m38[23D3]
R2305	RES_402	m38[23D3]
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R2309	RES_402	m38[23A7]
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R2313	RES_402	m38[23A7]
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R2323	RES_402	m38[23D5]
R2326	RES_402	m38[23D6]
R2327	RES_402	m38[23D6]
R2343	RES_402	m38[23D1]
R2388	RES_402	m38[23A3]
R2389	RES_402	m38[38D5]
R2390	RES_402	m38[23B3]
R2395	RES_402	m38[23D7]
R2396	RES_402	m38[23D6]
R2397	RES_402	m38[23D6]
R2398	RES_402	m38[23D8]
R2399	RES_402	m38[23C1]
R2500	RES_603	m38[25A8]
R2501	RES_402	m38[25C8]
R2502	RES_402	m38[25D8]
R2600	RES_402	m38[26C7]
R2606	RES_402	m38[26C7]
R2607	RES_402	m38[26C8]
R2609	RES_402	m38[26D7]
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R2632	RES_402	m38[26D2]
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R8103	RES_402	m38[81C3]
R8104	RES_402	m38[81C5]
R8105	RES_402	m38[81D7]
R8107	RES_402	m38[81A4]
R8110	RES_402	m38[81B3]
R8140	RES_402	m38[81C5]
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R8191	RES_402	m38[81C7]
R8192	RES_402	m38[81C7]
R8198	RES_402	m38[81A5]
R8199	RES_402	m38[81A5]
R8300	RES_402	m38[83B4]
R8301	RES_402	m38[83C5]
R8302	RES_402	m38[83B5]
R8303	RES_402	m38[83C4]
R8495	RES_402	m38[84A2]
R8496	RES_402	m38[84A2]
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R8502	RES_402	m38[85D6]
R8503	RES_402	m38[85D7]
R8504	RES_402	m38[85D7]
R8505	RES_402	m38[85C7]
R8506	RES_402	m38[85C8]
R8507	RES_402	m38[85D7]
R8508	RES_402	m38[85C7]
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R8522	RES_402	m38[85C3]
R8523	RES_402	m38[85C3]
R8524	RES_402	m38[85B3]
R8525	RES_402	m38[85B3]
R8526	RES_402	m38[85B3]
R8540	RES_402	m38[85C2]
R8554	RES_402	m38[85B7]
R8555	RES_402	m38[85B6]
R8556	RES_402	m38[85B6]
R8560	RES_402	m38[85A6]
R8561	RES_402	m38[85A7]
R8570	RES_402	m38[85A5]
R8585	RES_603	m38[85A3]
R8586	RES_402	m38[85A3]
R8588	RES_402	m38[85C5]
R8590	RES_402	m38[85C3]
R8591	RES_402	m38[85D3]
R8592	RES_402	m38[85D2]
R8593	RES_402	m38[85D3]
R8594	RES_402	m38[85D3]
R8596	RES_402	m38[85D3]
R8597	THERMISTER_0603-LF	m38[85D3]
R8598	RES_402	m38[85D2]
R8599	RES_1206	m38[85C4]
R8630	RES_603	m38[86C7]
R8710	RES_402	m38[87B8]
R8711	RES_402	m38[87A8]
R8712	RES_402	m38[87B7]
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R8721	RES_402	m38[87A4]
R8722	RES_402	m38[87B4]
R8723	RES_402	m38[87A4]
R8730	RES_402	m38[87A3]
R8731	RES_402	m38[87A3]
R8732	RES_402	m38[87A3]
R8733	RES_402	m38[87A1]
R8800	RES_603	m38[88D7]
R8801	RES_402	m38[88A7]
R8802	RES_402	m38[88D4]
R8803	RES_402	m38[88D4]
R8804	RES_402	m38[88D4]
R8805	RES_402	m38[88C4]
R8806	RES_402	m38[88C4]
R8807	RES_402	m38[88C4]
R8808	RES_402	m38[88C4]
R8809	RES_402	m38[88C4]
R8810	RES_402	m38[88C4]
R8811	RES_402	m38[88B4]
R8812	RES_402	m38[88C4]
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R8830	RES_402	m38[88B4]
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R8940	RES_402	m38[89B8]
R8941	RES_402	m38[89B8]
R8942	RES_402	m38[89B7]
R8943	RES_402	m38[89B7]

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R8946	RES_402	m38[89B7]
R8947	RES_402	m38[89B7]
R8948	RES_402	m38[89A7]
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R8981	RES_402	m38[89C4]
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R9046	RES_402	m38[90B7]
R9047	RES_402	m38[90B7]
R9048	RES_402	m38[90A7]
R9049	RES_402	m38[90A7]
R9080	RES_402	m38[90C4]
R9081	RES_402	m38[90C4]
R9082	RES_402	m38[90C4]
R9083	RES_402	m38[90C4]
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R9099	RES_402	m38[90A4]
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R9191	RES_402	m38[91D2]
R9195	RES_402	m38[91A3]
R9202	RES_402	m38[92C6]
R9250	RES_402	m38[92C6]
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R9351	RES_402	m38[93A8]
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R9371	RES_402	m38[93D1]
R9372	RES_402	m38[93C1]
R9373	RES_402	m38[93C1]
R9390	RES_402	m38[93A1]
R9391	RES_402	m38[93A1]
R9400	RES_402	m38[94C8]
R9401	RES_402	m38[94C7]
R9410	RES_402	m38[94C6]
R9411	RES_402	m38[94C6]
R9450	RES_402	m38[94C2]
R9470	RES_402	m38[94C7]
R9472	RES_402	m38[94B3]
R9473	RES_402	m38[94B2]
R9474	RES_402	m38[94B2]
R9475	RES_402	m38[94B1]
R9490	RES_805	m38[94C6]
R9491	RES_805	m38[94D6]
R9700	RES_402	m38[97D7]
R9701	RES_402	m38[97D8]
R9702	RES_402	m38[97D7]
R9703	RES_402	m38[97D7]
R9704	RES_402	m38[97C7]
R9705	RES_402	m38[97C7]
R9706	RES_402	m38[97D8]
R9707	RES_402	m38[97C8]
R9708	RES_402	m38[97C7]
R9709	RES_402	m38[97C7]
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R9712	RES_402	m38[97D2]
R9713	RES_402	m38[97C2]
R9714	RES_402	m38[97C2]
R9715	RES_402	m38[97C7]
R9716	RES_402	m38[97C8]
R9717	RES_402	m38[97C8]
R9720	RES_402	m38[97D1]
R9721	RES_402	m38[97D1]
R9722	RES_402	m38[97C2]
R9740	RES_402	m38[97A8]
R9741	RES_402	m38[97A8]
R9742	RES_402	m38[97A7]
R9750	RES_402	m38[97A3]
R9751	RES_402	m38[97A3]
RP2300	RPAK4P_SM-LF	m38[23D5]
RP3000	RPAK4P_SM-LF	m38[30B4 30C4 30D4 30D4]
RP3001	RPAK4P_SM-LF	m38[30C4 30A4 30A4 30D4]
RP3002	RPAK4P_SM-LF	m38[30A4 30A4 30A4 30D4]
RP3003	RPAK4P_SM-LF	m38[30C4 30C4 30C4 30D4]
RP3004	RPAK4P_SM-LF	m38[30C4 30C4 30D4]
RP3005	RPAK4P_SM-LF	m38[30B4 30A4 30A4 30D4]
RP3006	RPAK4P_SM-LF	m38[30B4 30B4 30A4 30D4]
RP3007	RPAK4P_SM-LF	m38[30C4 30C4 30C4 30C4]
RP3008	RPAK4P_SM-LF	m38[30C4 30C4 30C4 30C4]
RP3009	RPAK4P_SM-LF	m38[30B4 30B4 30C4 30C4]
RP3010	RPAK4P_SM-LF	m38[30B4 30B4 30B4 30B4]
RP3011	RPAK4P_SM-LF	m38[30B4 30A4 30B4 30B4]
RP7200	RPAK4P_SM-LF	m38[72A4]
SDF4700	PCB_STANDOFF	m38[47A2]
SDF4701	PCB_STANDOFF	m38[47A2]
SDF5300	PCB_STANDOFF	m38[53A5]
SDF5301	PCB_STANDOFF	m38[53A5]
SDF9400	PCB_STANDOFF	m38[94B6]
SDF9401	PCB_STANDOFF	m38[94A6]
SDF9402	PCB_STANDOFF	m38[94A6]
SW2600	SWI_TACT_4SM_EVQPH_S M-LF	m38[26C6]
SW5900	SWI_TACT_4SM_EVQPH_S M-LF	m38[59D8]

SW5901	SWI_TACT_4SM_EVQPH_S M-LF	m38[59B8]
U600	74LC125_TSSOP	m38[6A7 6B7 6B7 6C7]
U601	SN74LVC1G04_SOT23-5	m38[6C7]
U1000	ADT7461_MSOP	m38[10D5]
U1200	NB_945GM_BGA	m38[12D5]
U1200	NB_945GM_BGA	m38[13D4]
U1200	NB_945GM_BGA	m38[14D5]
U1200	NB_945GM_BGA	m38[15D3 15D7]
U1200	NB_945GM_BGA	m38[16D2 16C8]
U1200	NB_945GM_BGA	m38[17D5]
U1200	NB_945GM_BGA	m38[18D4 18D7]
U2100	SB_ICH7M_BGA	m38[21D6]
U2100	SB_ICH7M_BGA	m38[22B7 22D3]
U2100	SB_ICH7M_BGA	m38[23D4]
U2100	SB_ICH7M_BGA	m38[24D4 24D7]
U2601	MC74VHC1G08_SOT23-5-LF	m38[26D5]
U2603	SN74LVC1G04_SOT23-5	m38[26A7]
U2698	MC74VHC1G08_SOT23-5-LF	m38[26C4]
U2699	MAX6816_SOT143	m38[26C5]
U3100	LREG_BD3533FVM_MSOP-8	m38[31C5]
U3301	CLK_GEN_CY284455_QFN	m38[33C5]
U4101	88E8053_QFN	m38[41D5]
U4102	EEPROM_M24C08_SO8	m38[41A3]
U4400	FW32306_TQFP	m38[44D5]
U4700	SWI_TPS2024_SOI	m38[47C8]
U5000	SMC_H8S2116_BGA	m38[58A8 58C3 58C6 58D6]
U5900	VDET_RN5VD_SOT23-5	m38[59D8]
U5940	VREF_REF3133_SOT23-3	m38[59A4]
U5999	COMPARATOR_LMV339_TS SOP	m38[59A6 59A6 59A8 59A8]
U6100	MAX6695_UMAX	m38[61C4]
U6301	FLASH_SST25VF016B_SOI	m38[63D3]
U6700	TPM_TSSOP	m38[67C5]
U6800	AUDIO_STAC9220_LQFP	m38[68D5]
U7200	MAX9714_QFN-LF	m38[72C5]
U7500	ISL6262_QFN	m38[75C6]
U7501	INA138_SOT23-5-LF	m38[76D7]
U7600	OPAMP_LMV2011_SOT23-5	m38[76D3]
U7700	LTC3411_MSOP-LF	m38[77D5]
U7710	MC74VHC1G08_SOT23-5-LF	m38[77C7]
U7711	MC74VHC1G08_SOT23-5-LF	m38[77B7]
U7712	MC74VHC1G08_SOT23-5-LF	m38[77B7]
U7750	LTC3412_TSSOP-LF	m38[77B5]
U7800	ISL6549_QFN	m38[78C6]
U7900	ISL6549_QFN	m38[79D6]
U7901	COMPARATOR_LM339A_SO I-LF	m38[79A5]
U7901	COMPARATOR_LM339A_SO I-LF	m38[80A4]
U7901	COMPARATOR_LM339A_SO I-LF	m38[81A5]
U7910	COMPARATOR_LM339A_SO I-LF	m38[79A3 79B3]
U7910	COMPARATOR_LM339A_SO I-LF	m38[80B2]
U7910	COMPARATOR_LM339A_SO I-LF	m38[81B3]
U8000	ISL6549_QFN	m38[80D6]
U8100	ISL6549_QFN	m38[81D6]
U8400	ATI_M56P_BGA	m38[84C8 84D4]
U8400	ATI_M56P_BGA	m38[86D4]
U8400	ATI_M56P_BGA	m38[87D2 87D6]
U8400	ATI_M56P_BGA	m38[91D4]
U8400	ATI_M56P_BGA	m38[93C4]
U8500	ISL6269_QFN	m38[85D6]
U8550	FAN2558_SOT23-6-LF	m38[85B7]
U8560	74LVC1G125LF_SOT23-5	m38[85A6]
U8580	LT3483_TSOT23-6	m38[85A4]
U8595	OPAMP_LMV2011_SOT23-5	m38[85D2]
U8900	SGRAM_16MX32_GDDR3_1 36H_FBGA	m38[89D6 89B6]
U8950	SGRAM_16MX32_GDDR3_1 36H_FBGA	m38[89D3 89B3]
U9000	SGRAM_16MX32_GDDR3_1 36H_FBGA	m38[90D6 90B6]
U9050	SGRAM_16MX32_GDDR3_1 36H_FBGA	m38[90D3 90B3]
U9470	MC74VHC1G08_SOT23-5-LF	m38[94B2]
U9750	74AHC1G32_SM-LF	m38[97A4]
U9751	74AHC1G32_SM-LF	m38[97A4]
VR6800	LREG_TPS79501_SOT223-6	m38[68A4]
XC7200	MTGHOLE	m38[72B3]
XW601	SHORT_SM	m38[6C2]
XW602	SHORT_SM	m38[6C2]
XW604	SHORT_SM	m38[6A5]
XW605	SHORT_SM	m38[6A5]
XW5800	SHORT_SM	m38[58B3]
XW5900	SHORT_SM	m38[59B1]
XW6800	SHORT_SM	m38[74A4]
XW7201	SHORT_SM	m38[72B2]
XW7300	SHORT_SM	m38[73C5]
XW7400	SHORT_SM	m38[74D2]
XW7500	SHORT_SM	m38[75A6]
XW7501	SHORT_SM	m38[75B2]
XW7502	SHORT_SM	m38[75B1]
XW7503	SHORT_SM	m38[75D2]
XW7504	SHORT_SM	m38[75D1]
XW7598	SHORT_SM	m38[76D7]
XW7700	SHORT_SM	m38[77C4]
XW7750	SHORT_SM	m38[77A5]
XW7800	SHORT_SM	m38[78B6]
XW7900	SHORT_SM	m38[79C6]
XW8000	SHORT_SM	m38[80C6]
XW8100	SHORT_SM	m38[81C6]
XW8500	SHORT_SM	m38[85C6]
XW8715	SHORT_SM	m38[87A7]
XW8725	SHORT_SM	m38[87A4]
XW9135	SHORT_SM	m38[91A4]
XW9140	SHORT_SM	m38[91A4]
XW9300	SHORT_SM	m38[93C7]
XW9305	SHORT_SM	m38[93C7]
XW9310	SHORT_SM	m38[93C7]

XW9314	SHORT_SM	m38[93C7]
XW9320	SHORT_SM	m38[93B7]
XW9324	SHORT_SM	m38[93B7]
XW9330	SHORT_SM	m38[93B7]
XW9345	SHORT_SM	m38[93A7]
Y2600	CRYSTAL_4PIN_SM-LF	m38[26D8]
Y3301	CRYSTAL_5X3.2-SM	m38[33C7]
Y4101	CRYSTAL_4PIN_SM-3	m38[41B5]
Y4400	CRYSTAL_HC49-USMD	m38[44D2]
Y5800	CRYSTAL_SM-3	m38[59B8]
Y6700	CRYSTAL_4PIN_SM-LF	m38[59B7]
ZH500	HOLE_VIA	m38[5C1]
ZH501	HOLE_VIA	m38[5C1]
ZH502	HOLE_VIA	m38[5C1]
ZH503	HOLE_VIA	m38[5C1]
ZH504	HOLE_VIA	m38[5B1]
ZH505	HOLE_VIA	m38[5B1]
ZH506	HOLE_VIA	m38[5B1]
ZH507	HOLE_VIA	m38[5B1]
ZH508	HOLE_VIA	m38[5B1]
ZH509	HOLE_VIA	m38[5B1]
ZH510	HOLE_VIA	m38[5C1]
ZH511	HOLE_VIA	m38[5C1]
ZH512	HOLE_VIA	m38[5C1]
ZH513	HOLE_VIA	m38[5C1]
ZH514	HOLE_VIA	m38[5B1]
ZH515	HOLE_VIA	m38[5B1]
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ZH518	HOLE_VIA	m38[5B1]
ZH519	HOLE_VIA	m38[5B1]
ZH520	HOLE_VIA	m38[5C1]
ZH521	HOLE_VIA	m38[5C1]
ZH522	HOLE_VIA	m38[5C1]
ZH523	HOLE_VIA	m38[5C1]
ZH524	HOLE_VIA	m38[5B1]
ZH525	HOLE_VIA	m38[5B1]
ZH526	HOLE_VIA	m38[5B1]
ZH527	HOLE_VIA	m38[5B1]
ZH528	HOLE_VIA	m38[5B1]
ZH529	HOLE_VIA	m38[5B1]
ZH601	MTGHOLE	m38[6A3]
ZH602	MTGHOLE	m38[6A3]
ZH603	MTGHOLE	m38[6A3]
ZH604	MTGHOLE	m38[6B3]
ZH606	MTGHOLE	m38[6A1]
ZH607	MTGHOLE	m38[9D4]
ZH608	MTGHOLE	m38[9D3]
ZH609	MTGHOLE	m38[9D2]
ZH610	MTGHOLE	m38[9D2]