

M60 - PVT

09/27/06

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
				DATE	DATE
H		464264	PRODUCTION RELEASED	09/27/06	06/22/04

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79	MY	61 VR - "S3" 1.8V
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88	JH	70 GPU - MISC
89	JH	71 GPU - GDDR SDRAM A
90	JH	72 GPU - GDDR SDRAM B
91	JH	73 GPU - M56 GPIO, DVO, MISC
92	JH	74 GPU - M56 CLOCKS
93	JH	75 GPU - M56 VIDEO INTERFACES
94	JH	76 GPU - INTERNAL DISPLAY CONN'S
95	JH	77 GPU - TP'S
96	JH	78 GPU - TMDS, INVERTER, EXT VGA
97	JH	79 GPU - EXTERNAL DISPLAY CONN'S

<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<p>Apple Computer Inc.</p>
<p>DRAPTER</p> <p>ENG APPD</p> <p>QA APPD</p> <p>RELEASE</p>	<p>DESIGN CK</p> <p>MFG APPD</p> <p>DESIGNER</p> <p>SCALE</p>	<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p>II NOT TO REPRODUCE OR COPY IT</p> <p>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p>
<p>SCH, MLB, M60</p>		<p>TITLE</p>
<p>MATERIAL/FINISH NOTED AS APPLICABLE</p>		<p>DRAWING NUMBER 051-7124 REV. H</p>
<p>SIZE D</p>		<p>SHT 1 OF 111</p>

D

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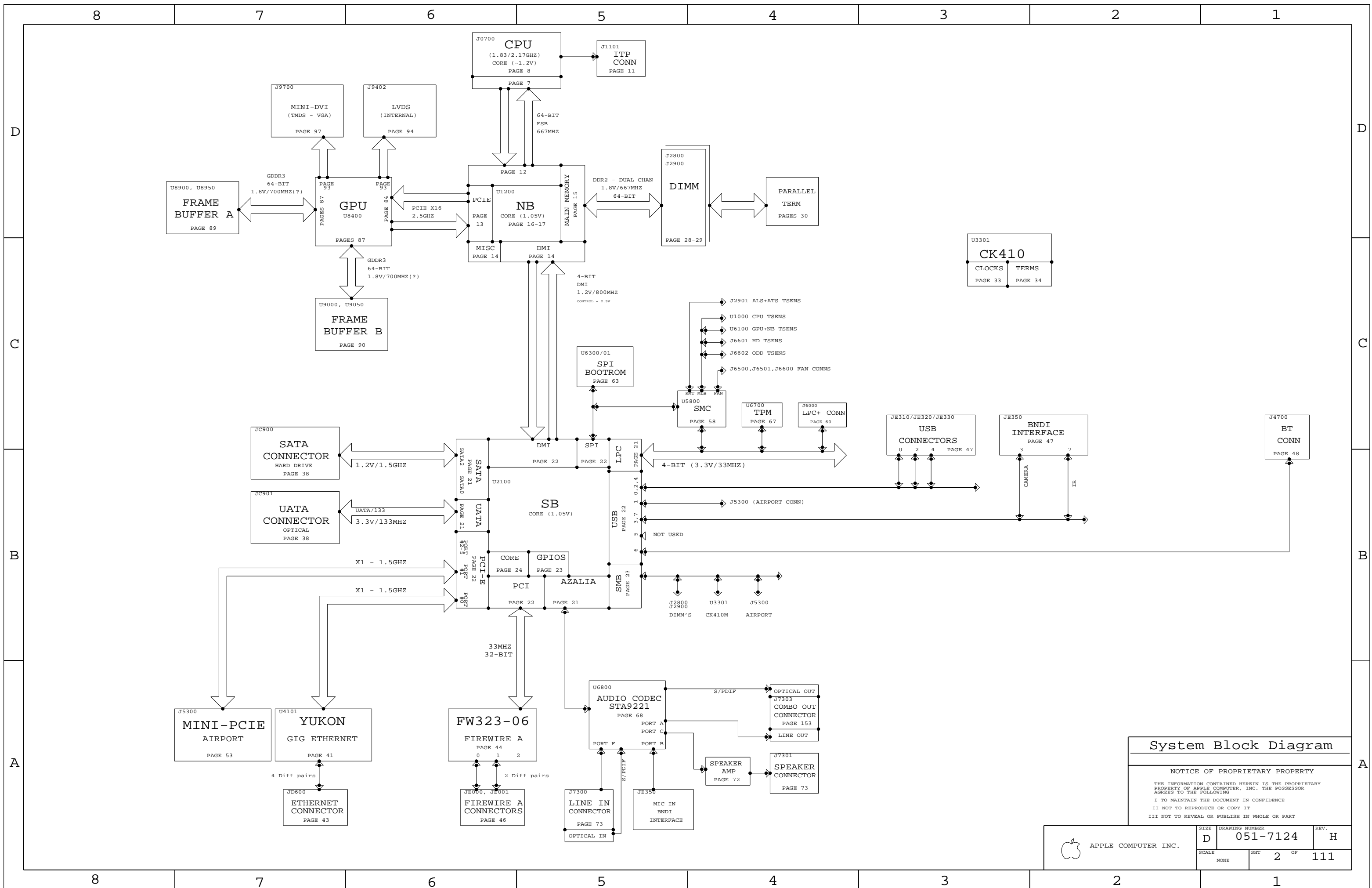
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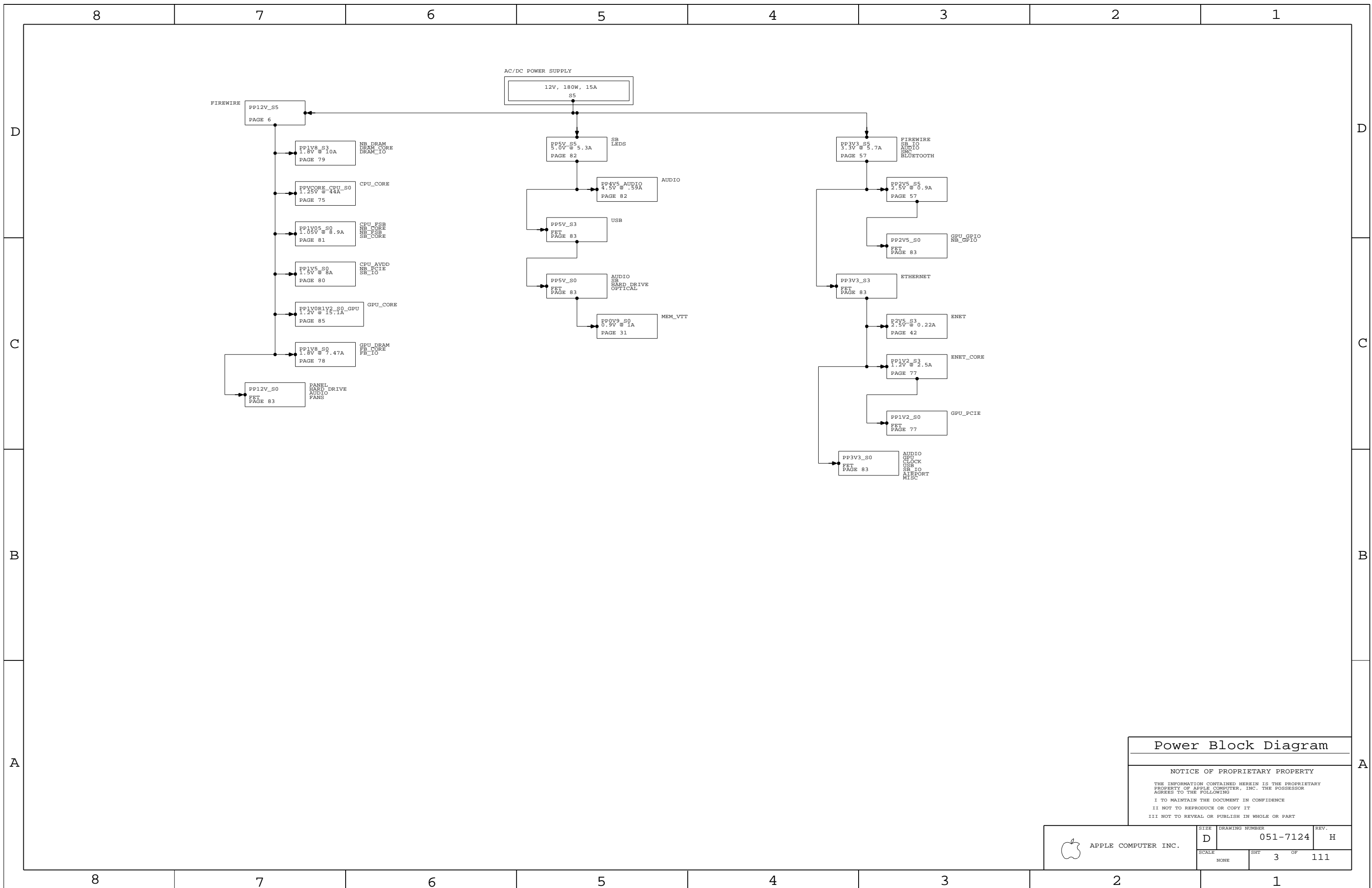
System Block Diagram

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Power Block Diagram

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NONE	3	111	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0328	1	IC,945PM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
338S0345	1	IC,ATI,M56D,GRAFIXCTLR,880BGA,LF	U8400	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
338S0270	1	IC,88E8053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
UNSCREENED P/N 353S1235 353S1465	1	IC,CPU VREG,1MVP,TWO PHASE	U7500	CRITICAL	
152S0138	2	IND,PWR,SMD,3.3OH,20%,6A,30MHZ,LF,MD	L5703,L8203	CRITICAL	
128S0078	2	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518	CRITICAL	
825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
155S0289	7	EMI CHOKE	FLR011,FLR021,FL4610,FL4620,L4712,L4722,L4732	CRITICAL	

(341S1904 - DEV)
 (341S1905 - PVT)
 (335S0384 - BLNK)
 (341S1903 - PROG)
 (338S0274 - BLNK)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7124	1	PCB,SCHEM,MLB,M60	SCH1		20_INCH_LCD
820-2031	1	PCB,FAB,MLB,M60	MLB1		20_INCH_LCD
341T0036	1	EPI ROM,M60	U6301	CRITICAL	20_INCH_LCD
341T0035	1	IC,SMC,M60	U5800	CRITICAL	20_INCH_LCD
338S0315	1	IC,ATI,M56LP,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	GPU_B26_LP
114S0264	1	3.01K,1%,1/16W,402,MP-LF	R8522		GPU_VCORE_1P2V
337S3390	1	2.16GHZ MEROM	CPU	CRITICAL	2P16_CPU
337S3392	1	2.33GHZ MEROM	CPU	CRITICAL	2P33_CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX
333S0376	4	IC,SDRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_INFINEON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SDRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SDRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX
333S0377	4	IC,SDRAM,GDDR3,16MX32,600MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_INFINEON

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0086	126S0078		C940,C1900,C1901,C1968	SANYO W6CE330FS 330UF 6.3V LF
128S0080	128S0078		C7517,C7518	SANYO 165VP330W 330UF 16V SMD LF
124-0338	124-0333			CAP,AL,EL,680UF,16V,RAD,10X12.5MM
138S0580	138S0552			22UF 0805
124-0361	124-0339		C7807	SANYO
353S1321	353S1105		U7910	LM339
338S0344	338S0345		U8400	M56 B26 P - DIFF P/N
353S1461	353S1465		U7500	CPU REGULATOR - ISL9504
378S0141	378S0140		LED01,LED02,LED03	LED
138S0598	138S0512			SAMSUNG
155S0232	155S0289		FLR011,FLR021,FL4610,FL4620	L4712,L4722,L4732 EMI CHOKE

Table Items

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SCALE	SHT	OF
NONE	4	111

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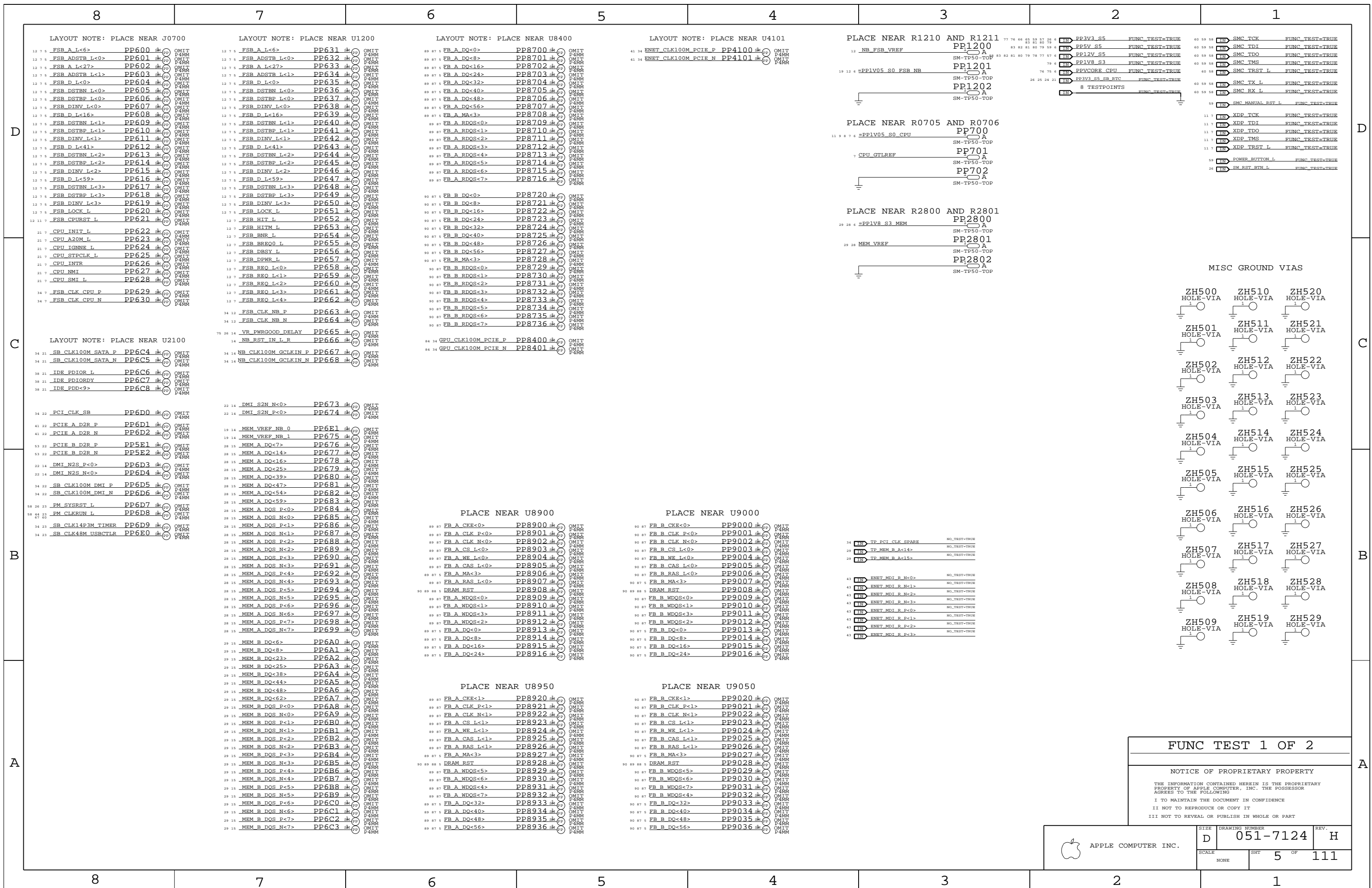
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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

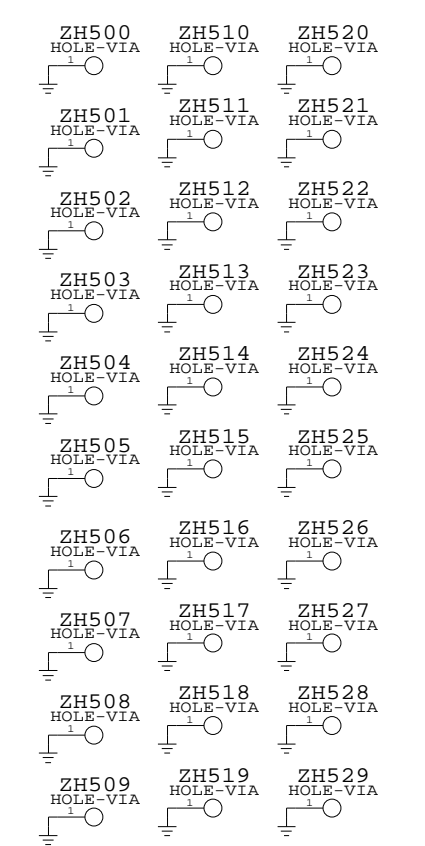
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

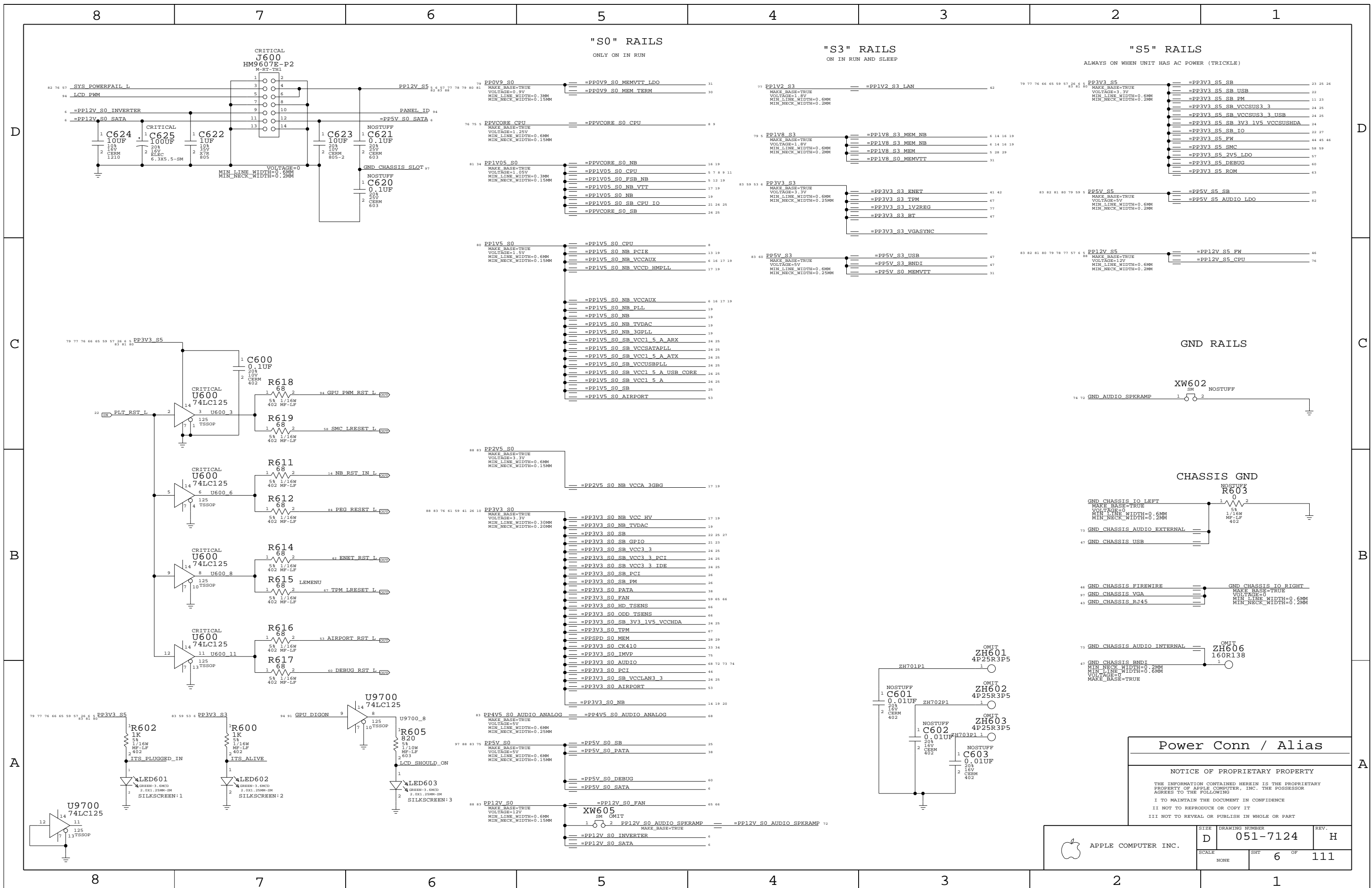
MISC GROUND VIAS



FUNC TEST 1 OF 2

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APPLE COMPUTER INC. DRAWING NUMBER 051-7124 REV. H SCALE NONE SHEET 5 OF 111



"S0" RAILS

ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

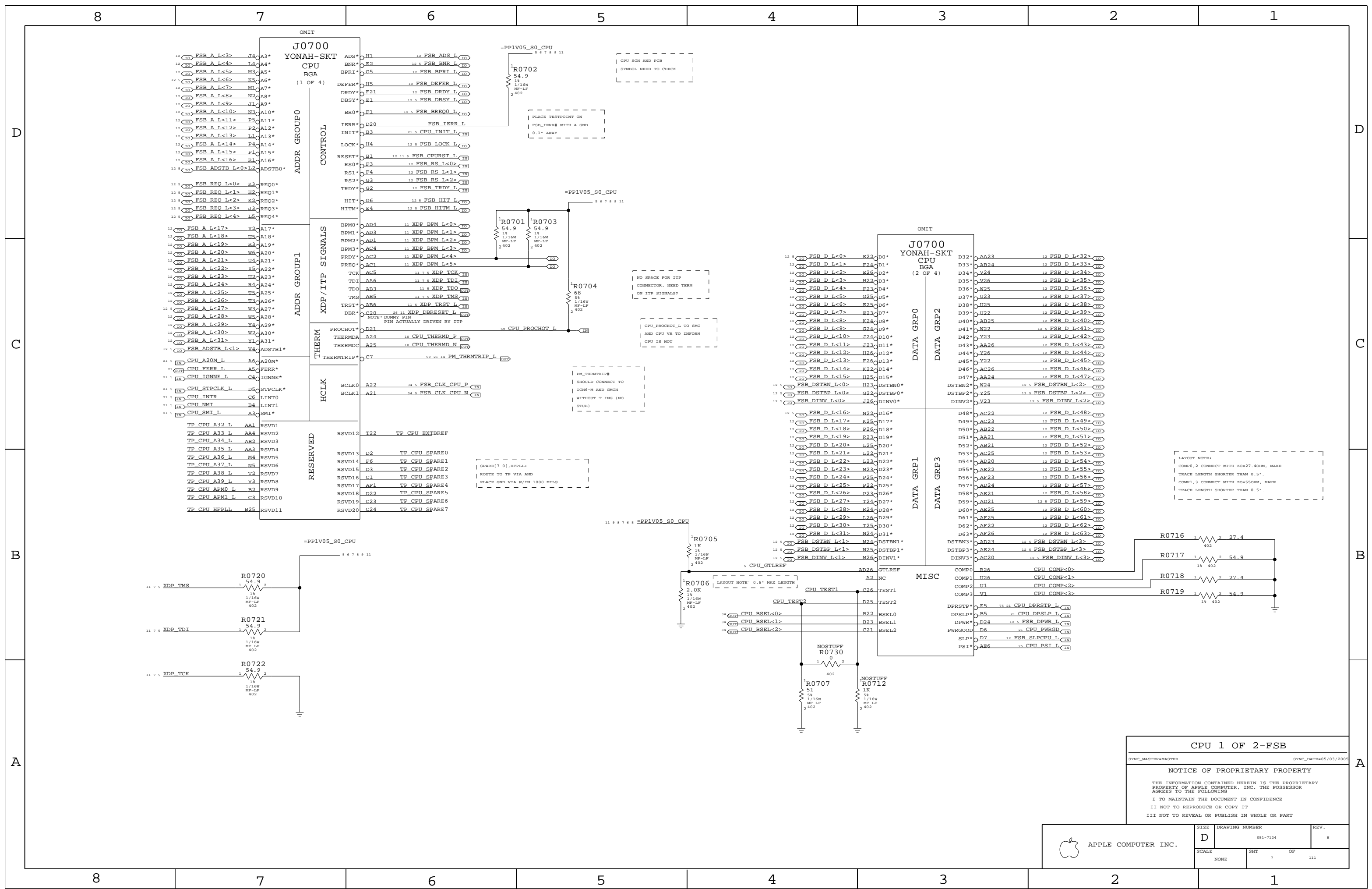
CHASSIS GND

Power Conn / Alias

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	SCALE NONE	SHEET 6 OF 111	



CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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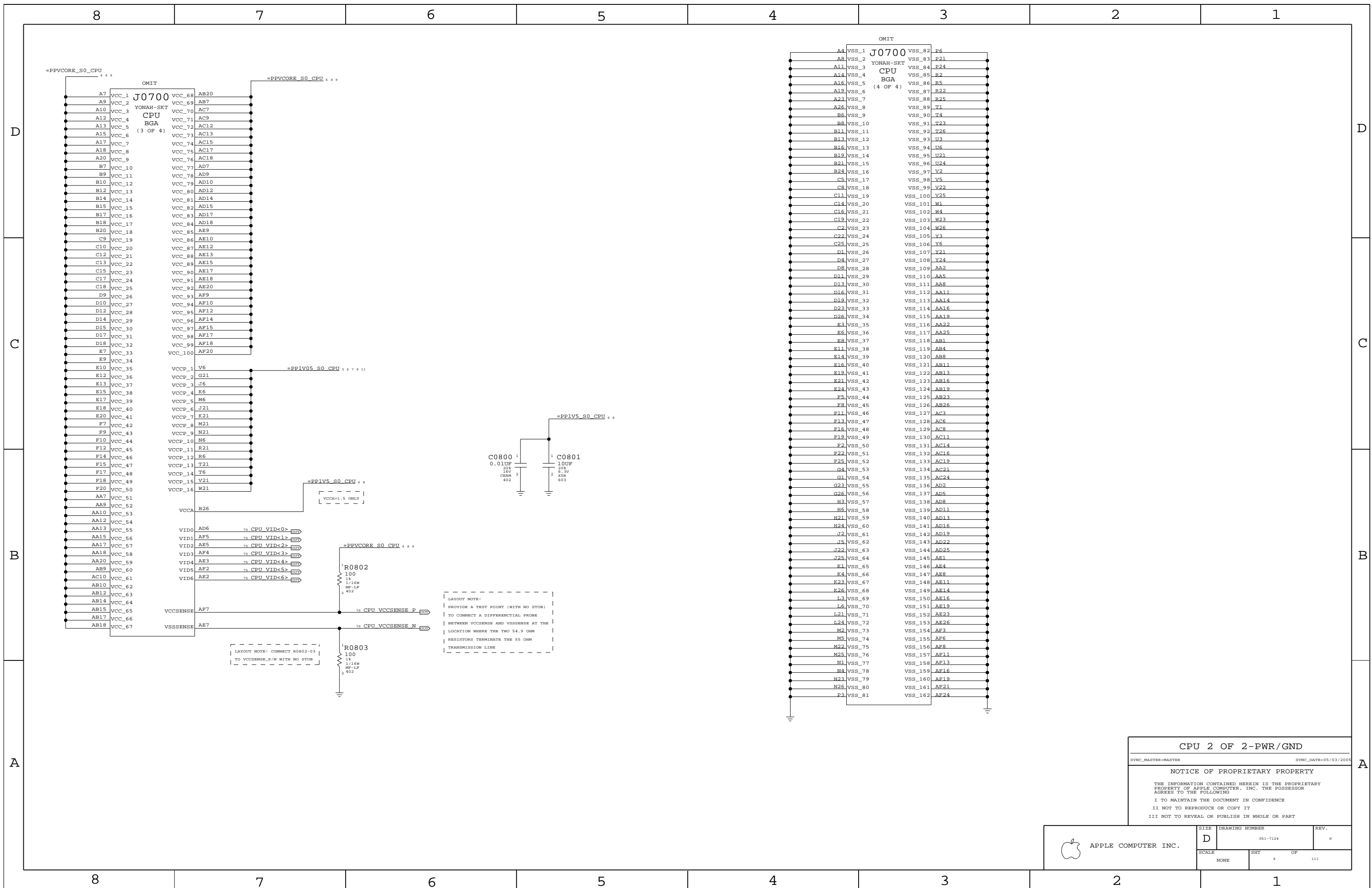
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	SCALE NONE	SHEET 7	OF 111



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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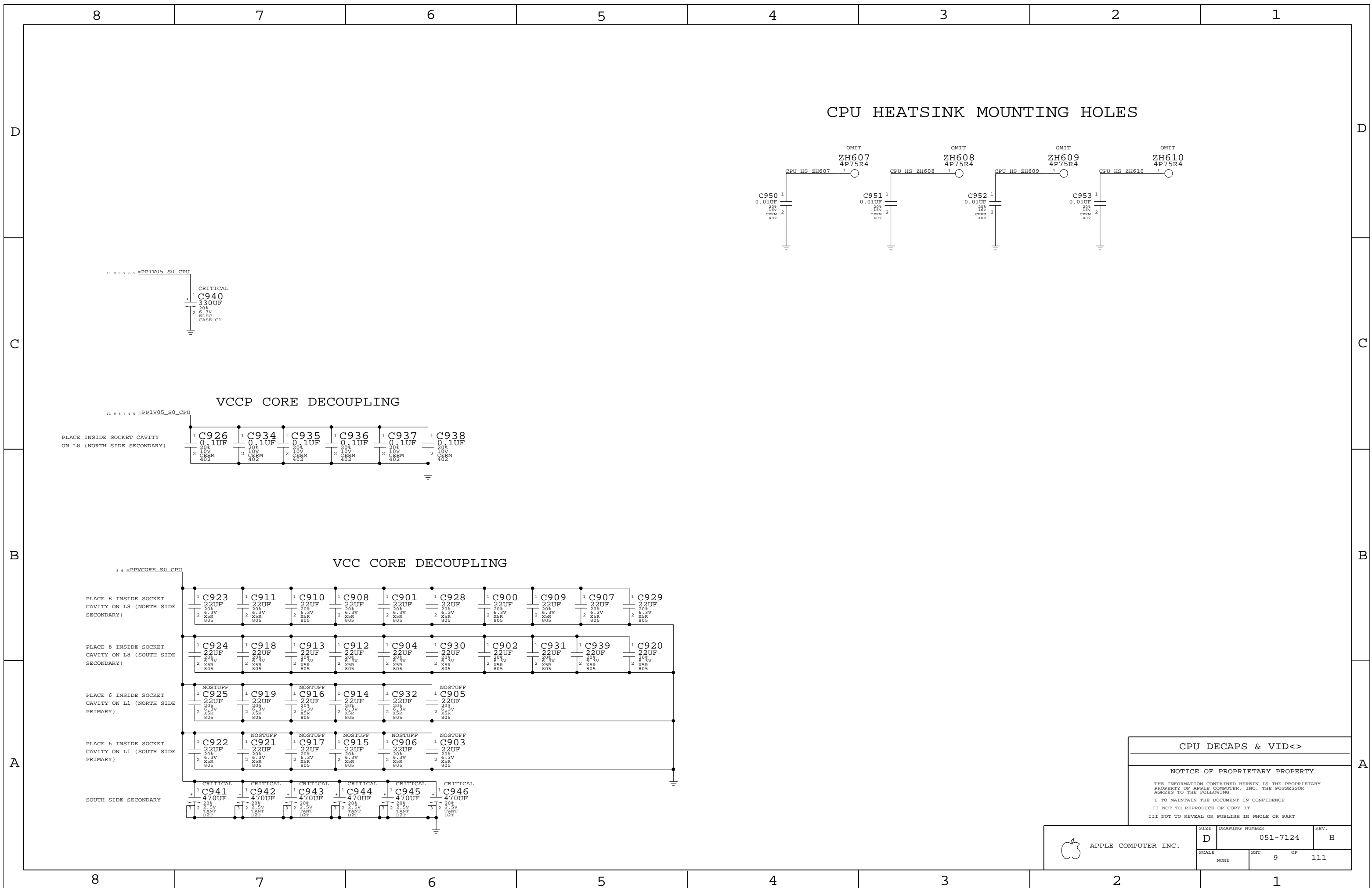
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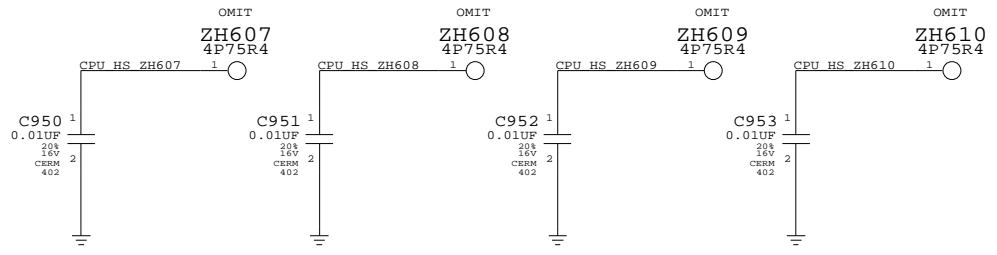
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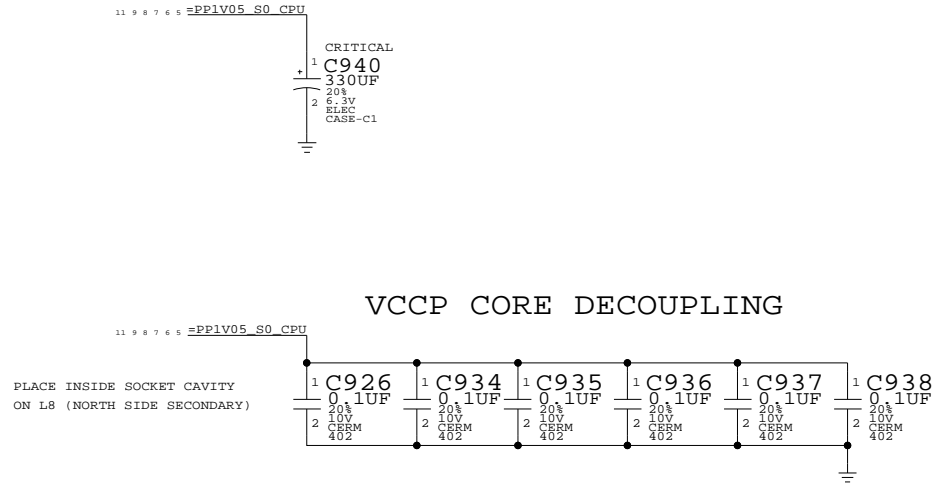
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SCALE	SHT OF		REV.
NONE	8 111		



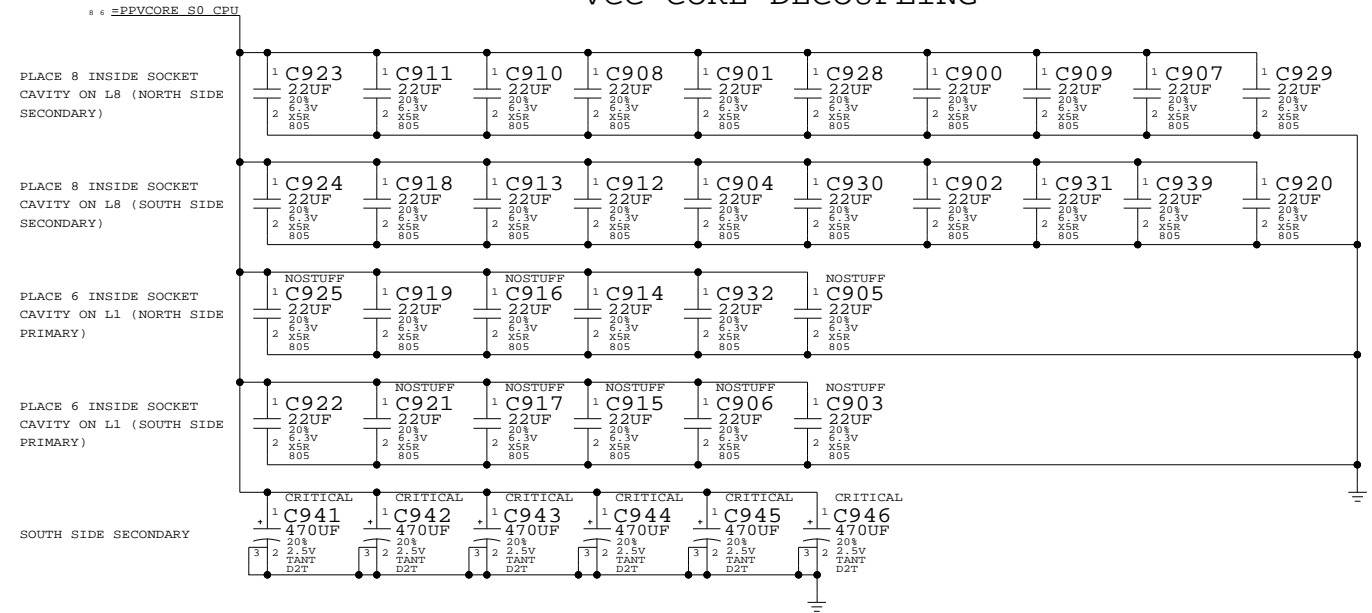
CPU HEATSINK MOUNTING HOLES



VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

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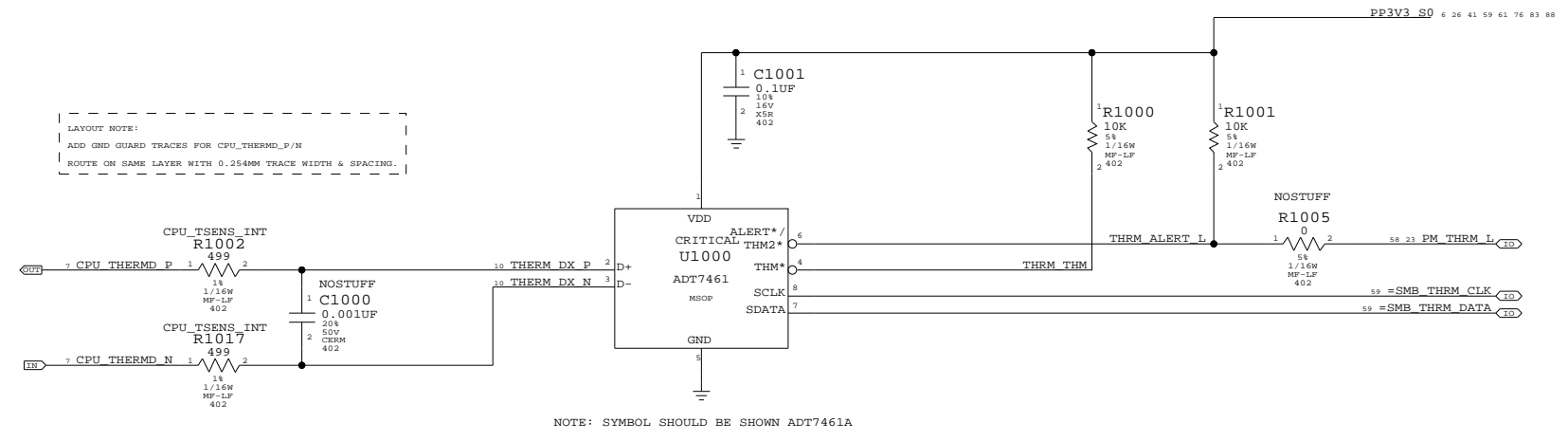
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NONE	9	111	

CPU THERMAL SENSOR

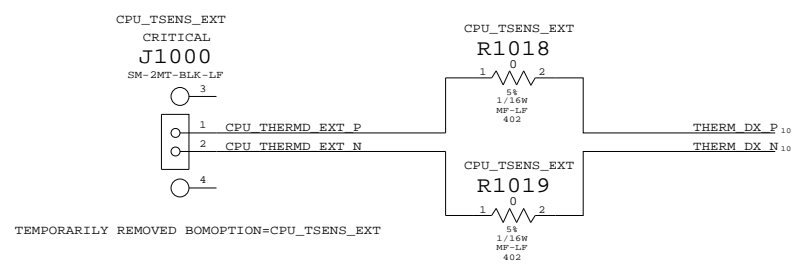
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.

NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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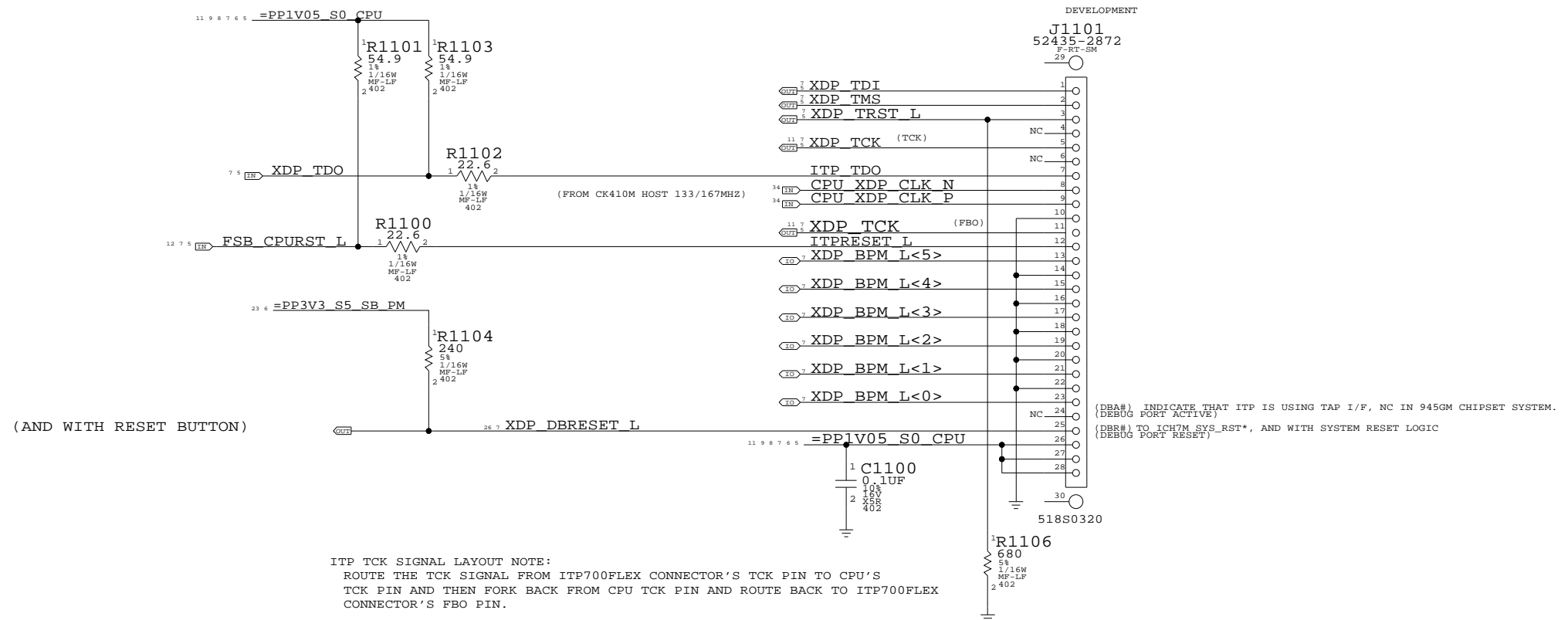
B

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CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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SCALE	SHT	OF	111
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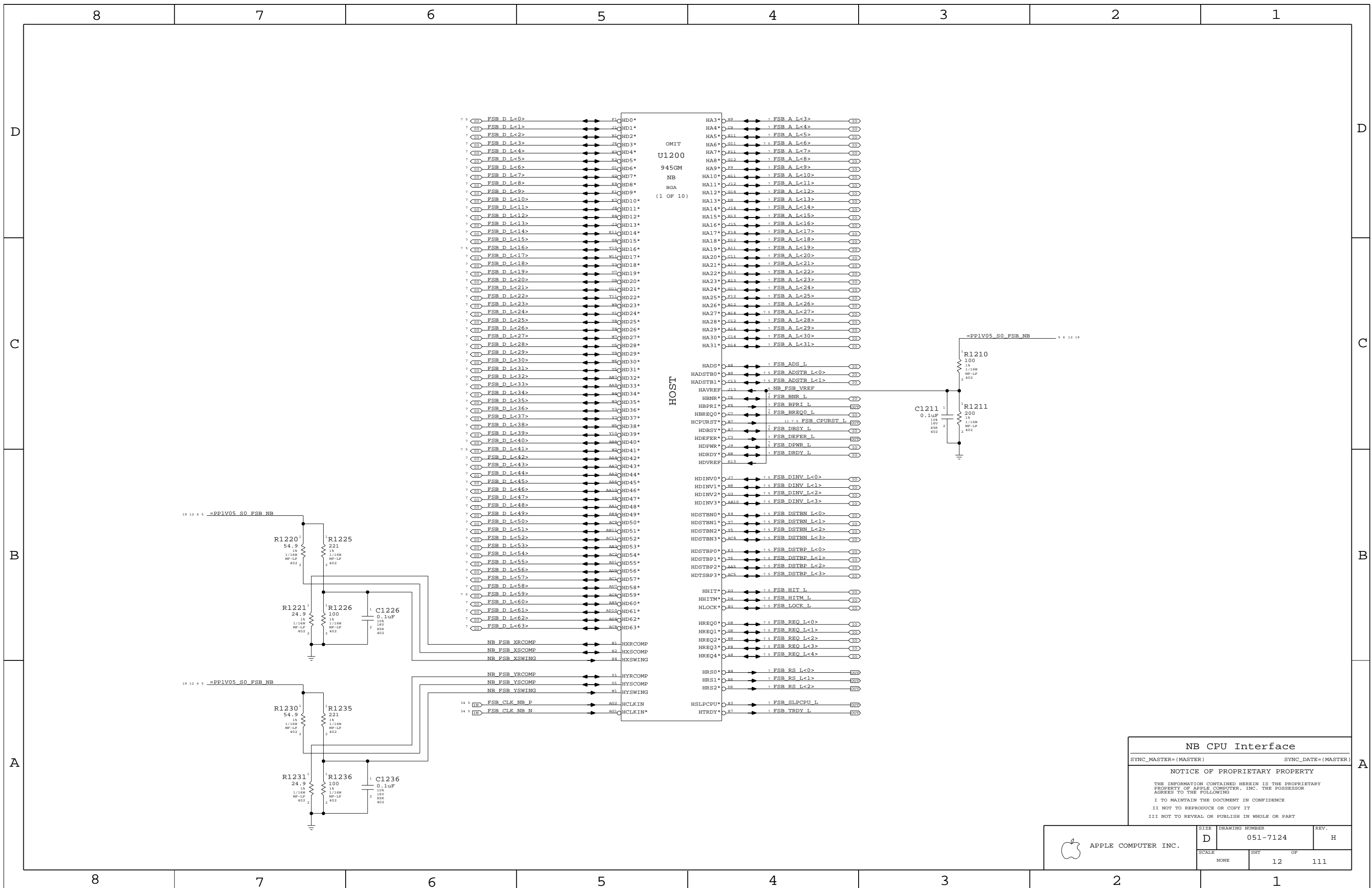
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NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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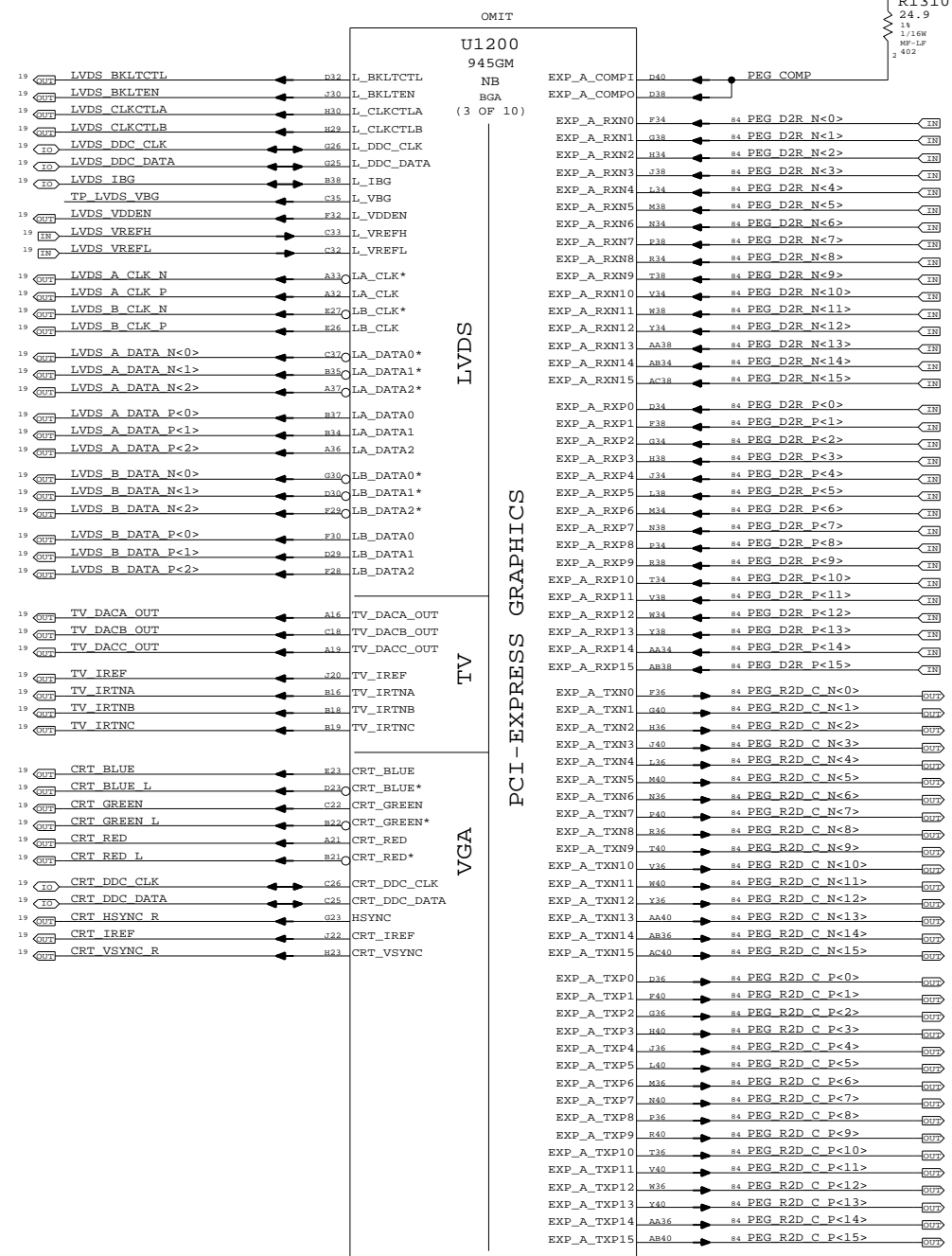
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 12	OF 111

LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC
 Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

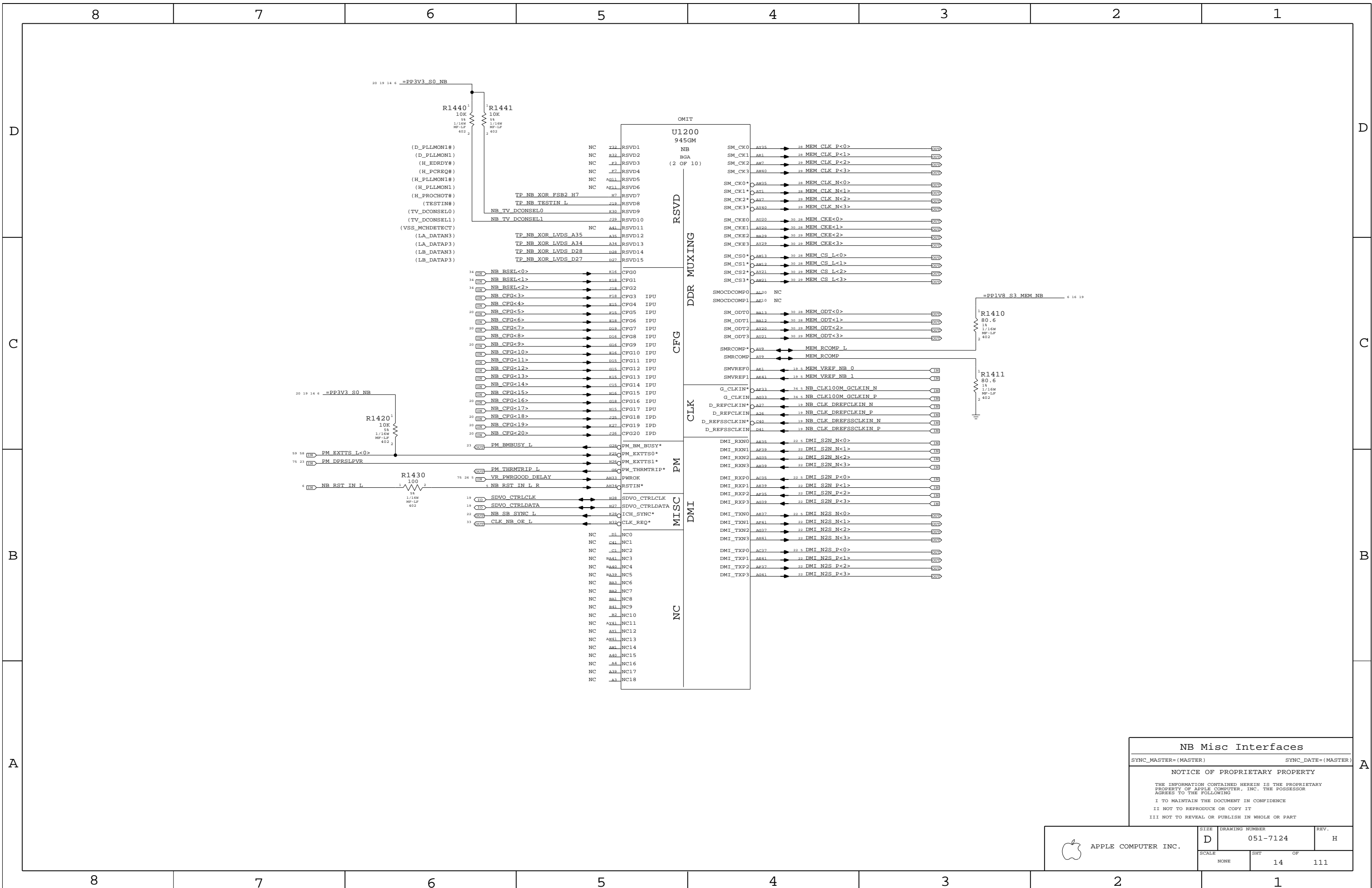
SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	13	111	



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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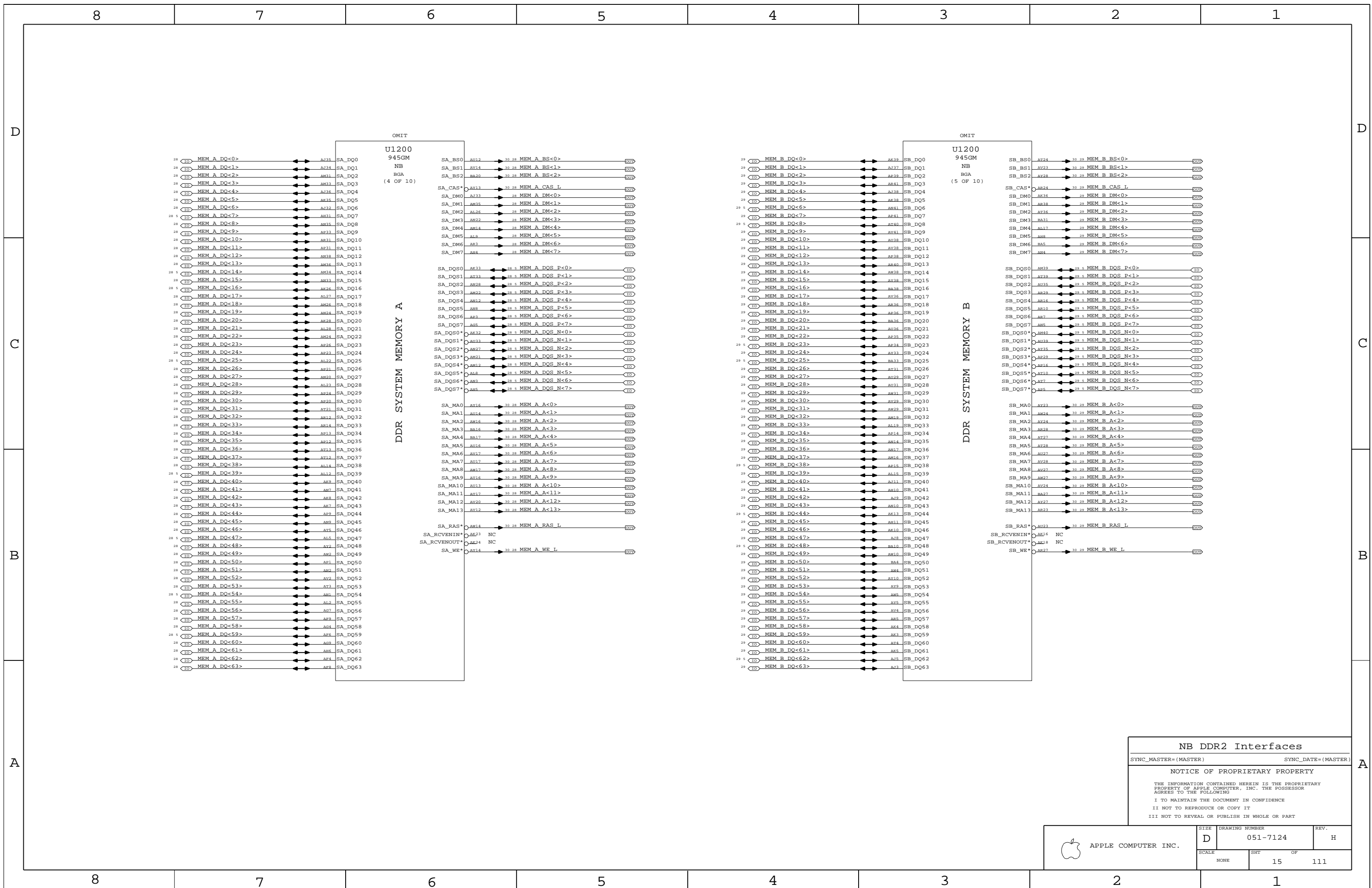
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	SCALE NONE	SHEET OF 14 OF 111	



NB DDR2 Interfaces

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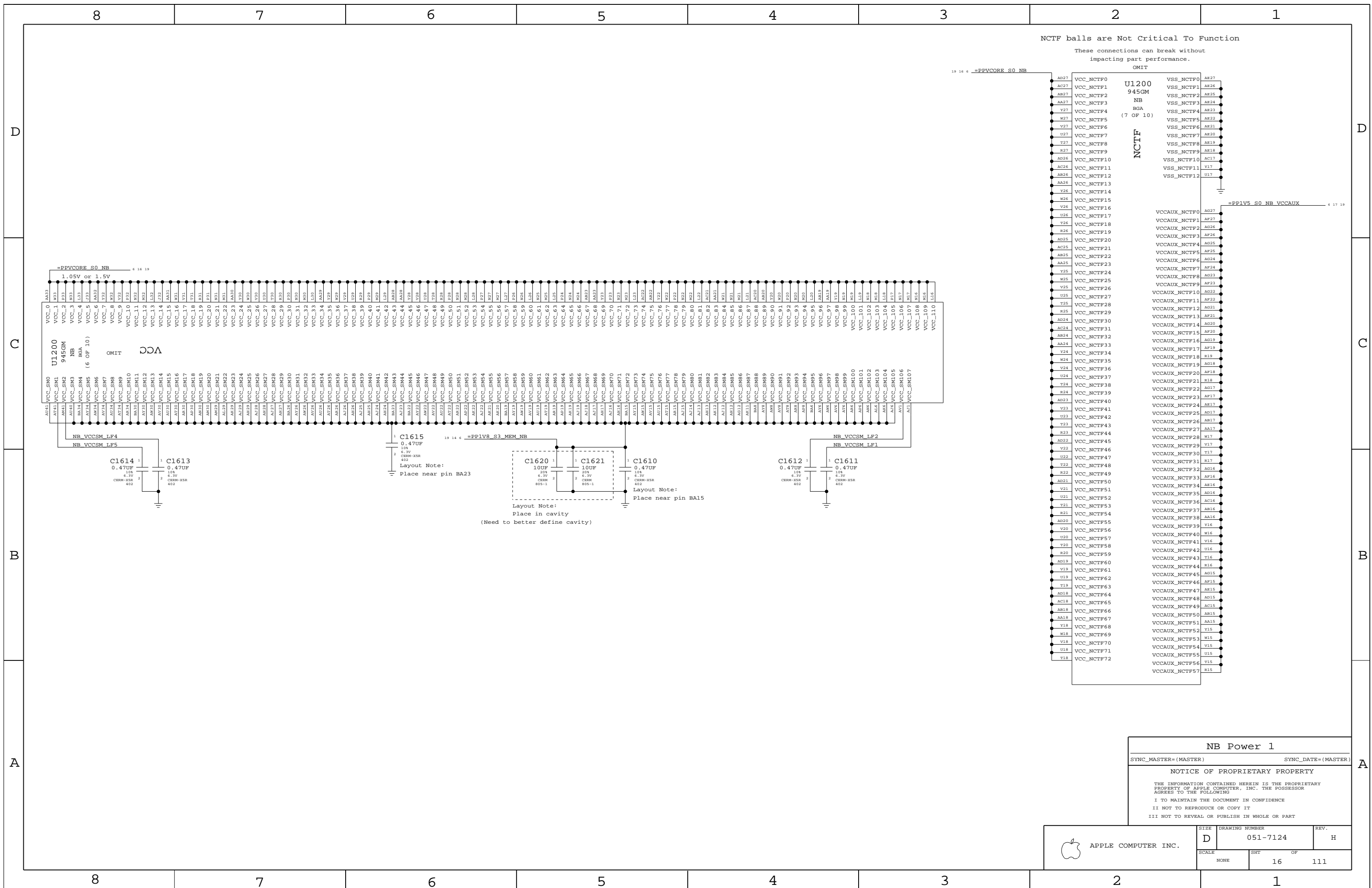
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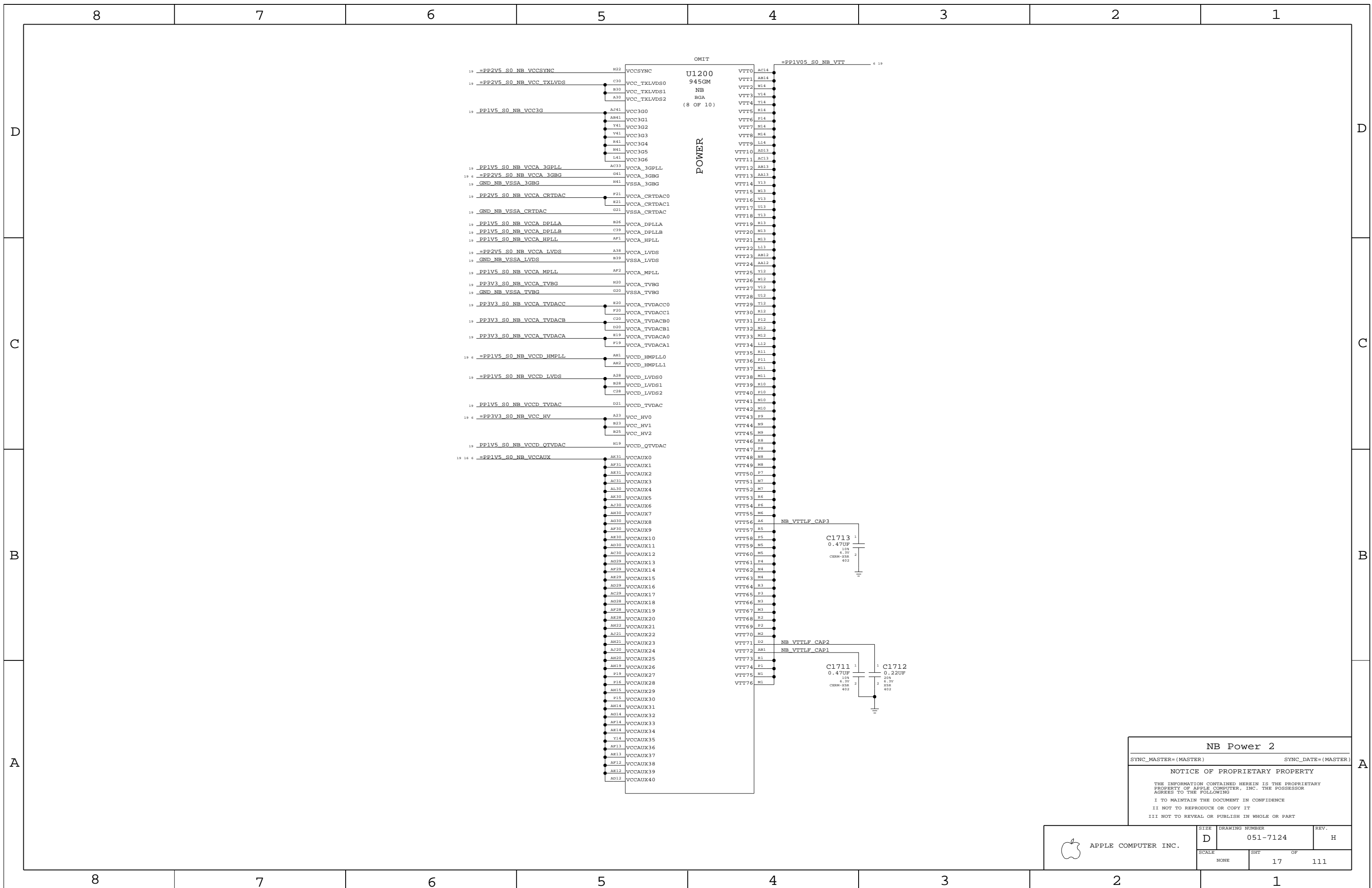
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 15	OF 111



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	16	111	



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

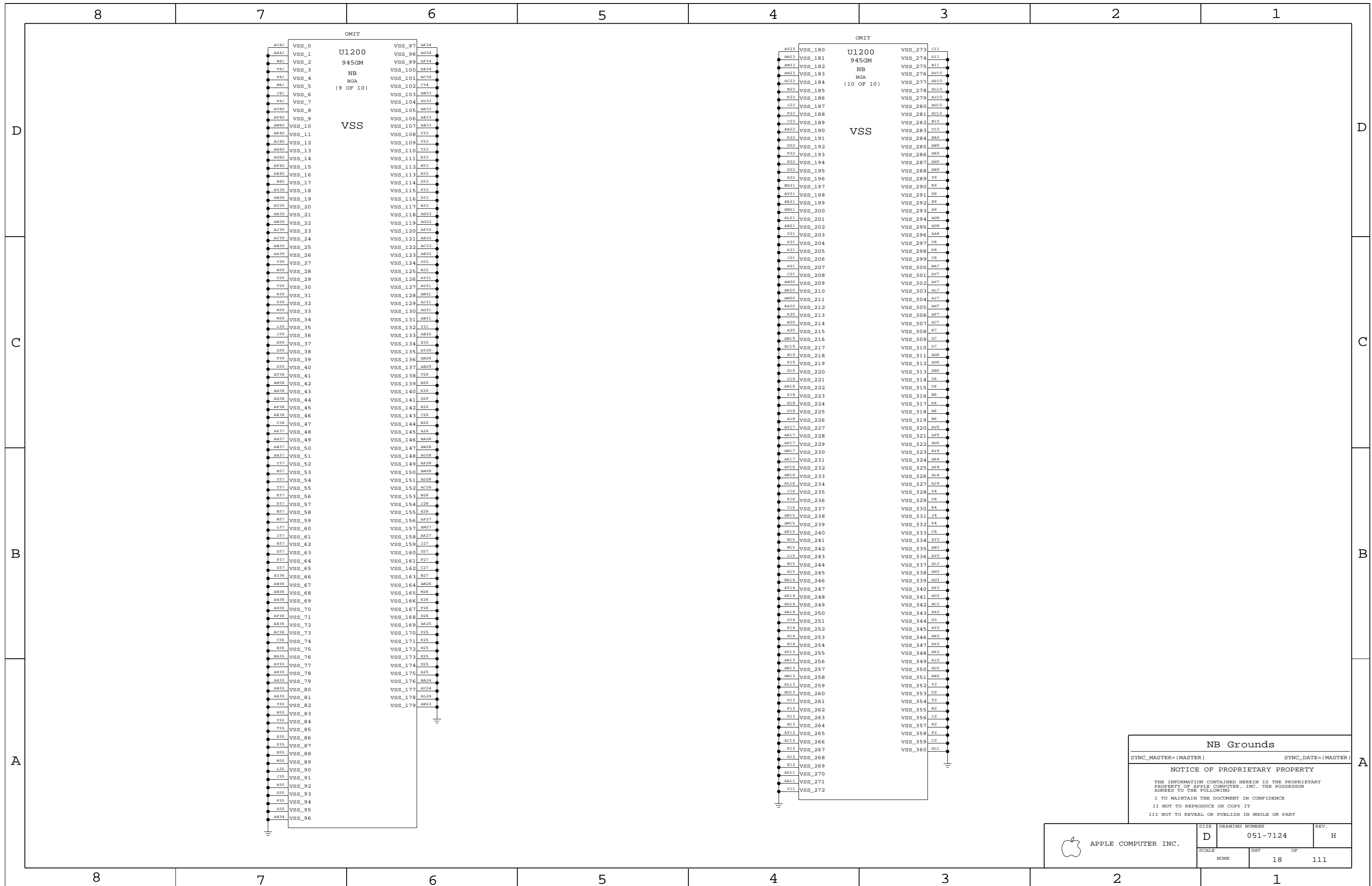
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEETS OF 17 OF 111	



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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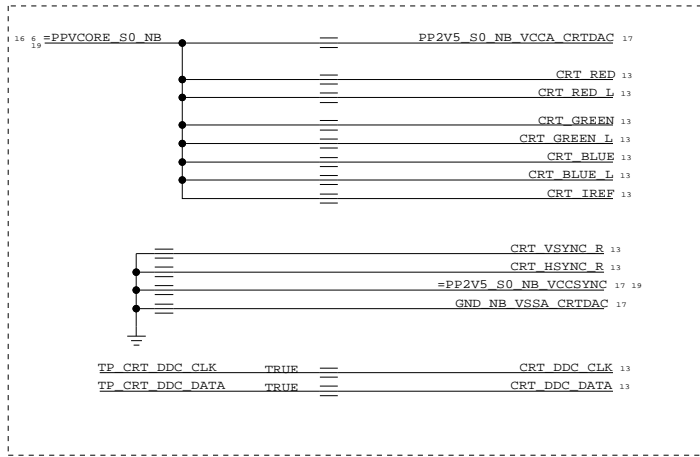
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHT 18	OF 111

Power Interface

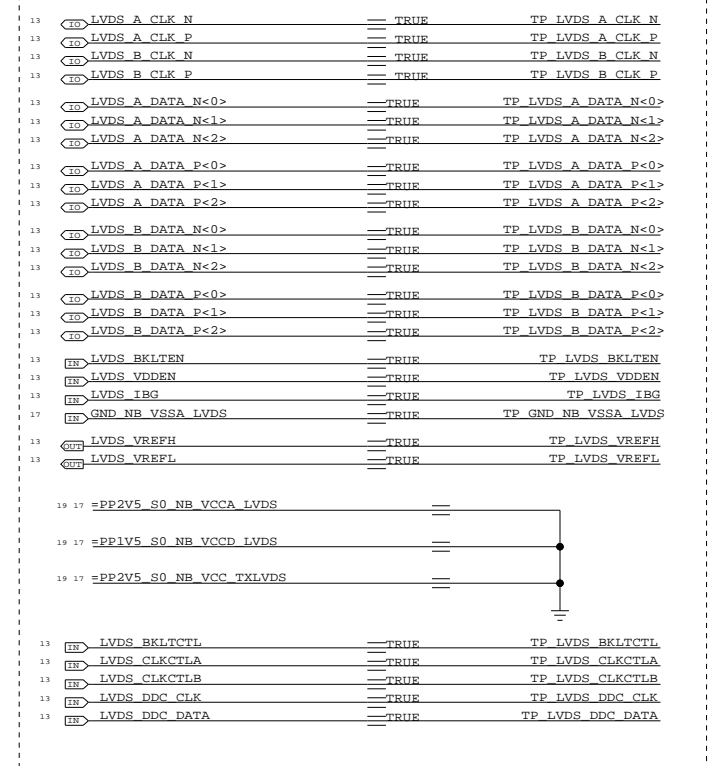
These are the power signals that leave the NB "block"

IN	=PP1V05_S0_FSB_NB	5 6 12
IN	=PPVCORE_S0_NB	6 16 19
IN	=PP1V05_S0_NB	6
IN	=PP1V05_S0_NB_VTT	6 17 19
IN	=PP1V5_S0_NB	6 19
IN	=PP1V5_S0_NB_PCIE	6 13
IN	=PP1V5_S0_NB_PLL	6 19
IN	=PP1V5_S0_NB_TVDAC	6 19
IN	=PP1V5_S0_NB_VCCD_HMPLL	6 19
IN	=PP1V5_S0_NB_VCCD_HMPLL	6 17
IN	=PP1V5_S0_NB_VCCD_LVDS	17 19
IN	=PP1V5_S0_NB_VCCAUX	6 16 17 19
IN	=PP1V8_S3_MEM_NB	6 14 16 19
IN	=PP2V5_S0_NB_VCCSYNCR	17 19
IN	=PP2V5_S0_NB_VCC_TXLVDS	17 19
IN	=PP2V5_S0_NB_VCCA_3GBG	6 17 19
IN	=PP2V5_S0_NB_VCCA_LVDS	17 19
IN	=PP3V3_S0_NB	6 14 20
IN	=PP3V3_S0_NB_TVDAC	6
IN	=PP3V3_S0_NB_VCC_HV	6 17 19

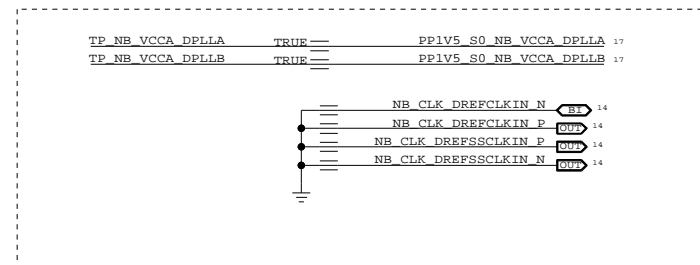
TVOUT DISABLE



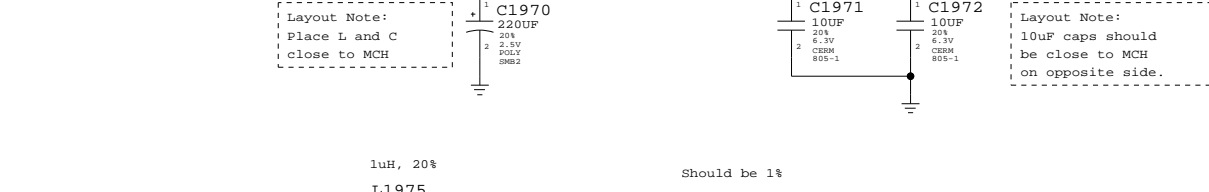
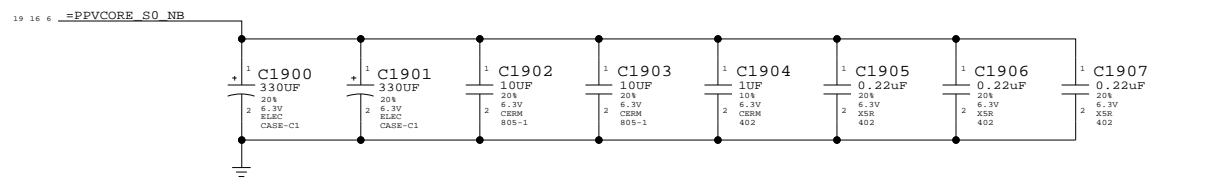
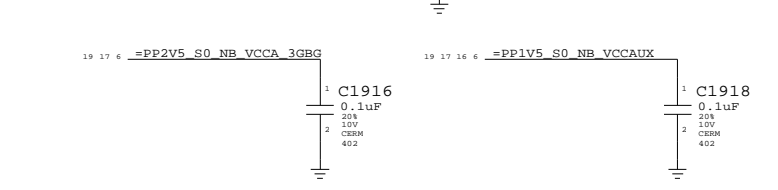
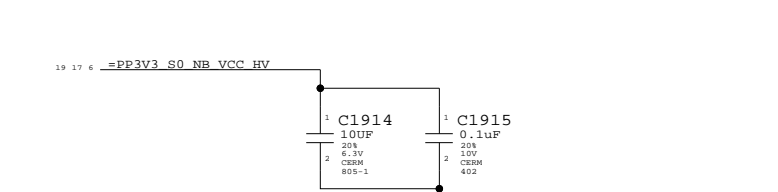
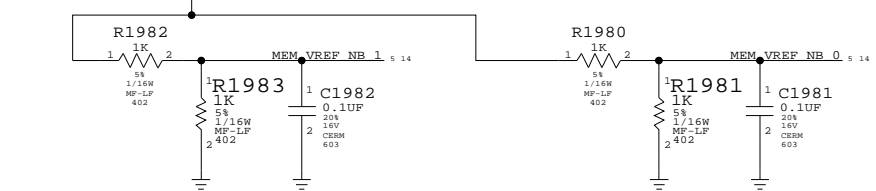
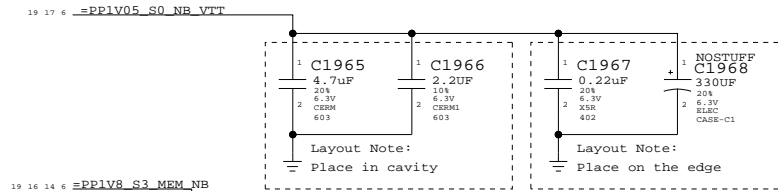
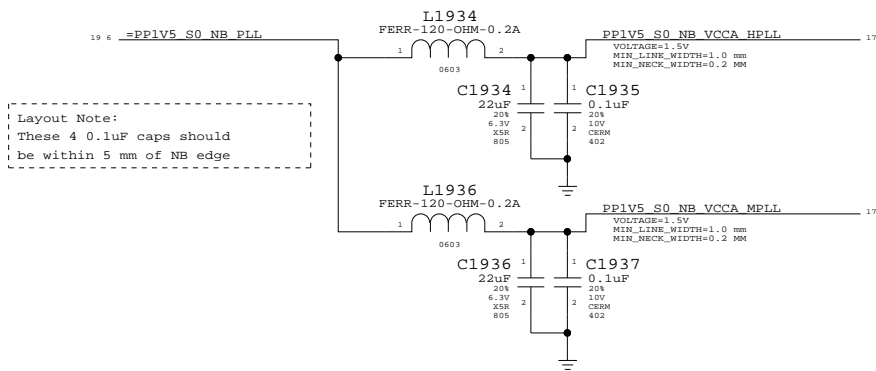
LVDS DISABLE



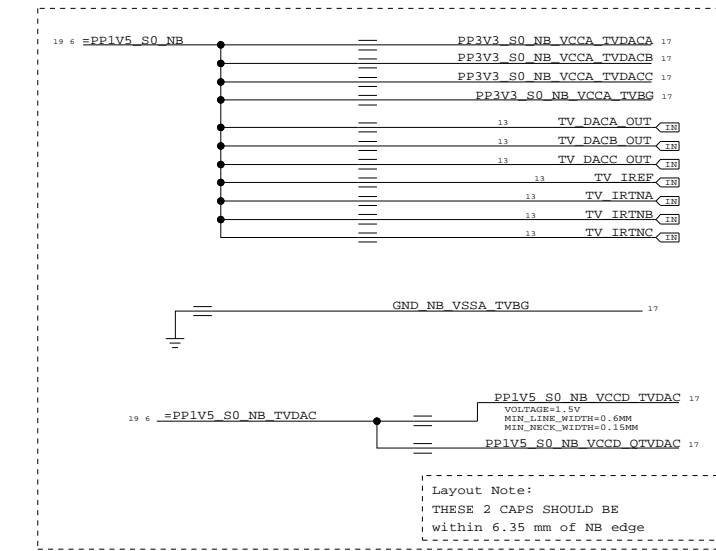
DISPLAY DISABLE



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge



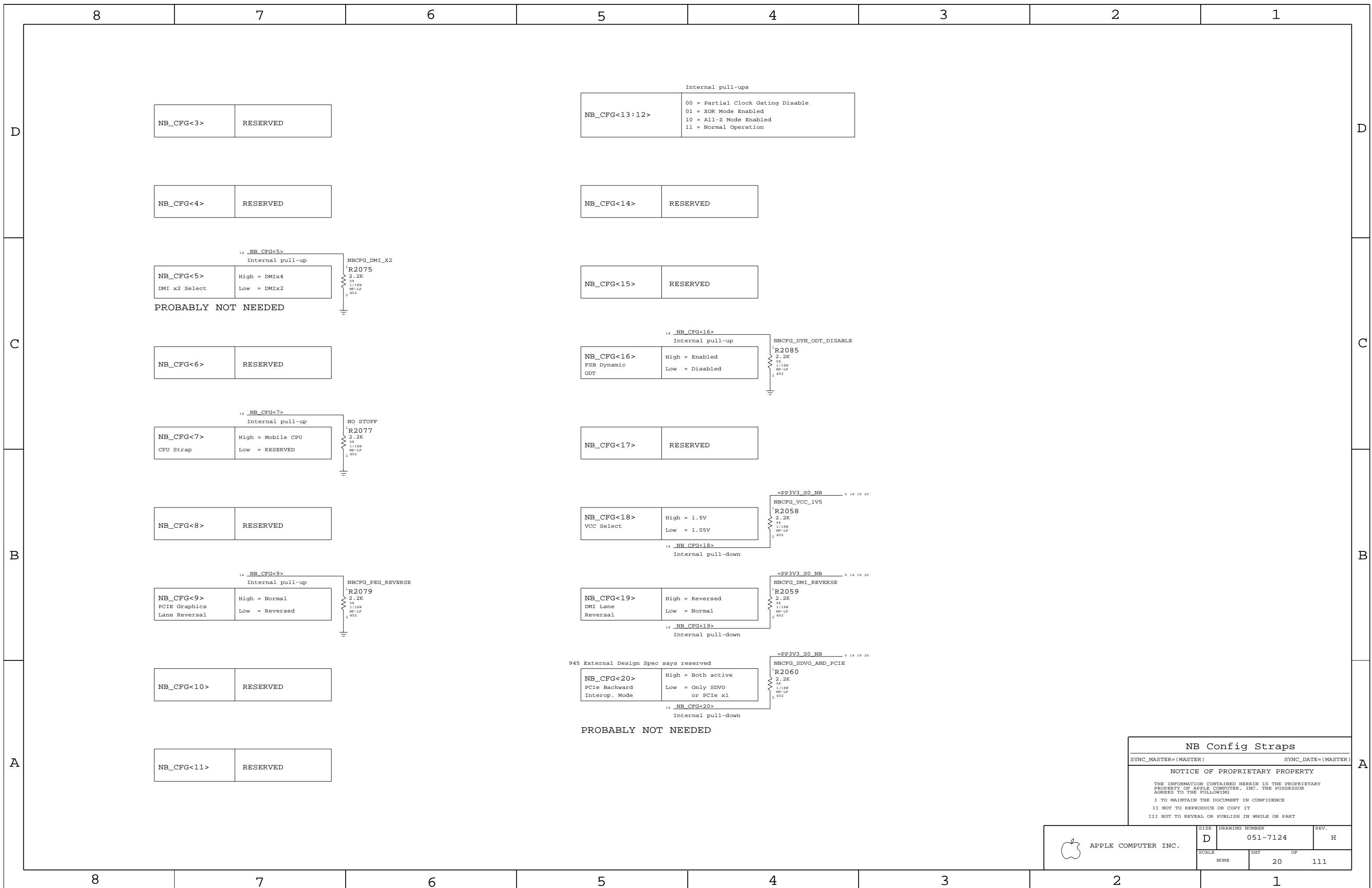
TVOUT DISABLE



Layout Note:
THESE 2 CAPS SHOULD BE WITHIN 6.35 mm OF NB EDGE

NB (GM) Decoupling
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7124	H
SCALE	SHT	OF	
NONE	19	111	



NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<13:12>	Internal pull-ups 00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	---

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

14 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2

PROBABLY NOT NEEDED

NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled

14 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED

NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

14 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V

14 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

14 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal

NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved	
14 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1

NB_CFG<11>	RESERVED
------------	----------

PROBABLY NOT NEEDED

NB Config Straps

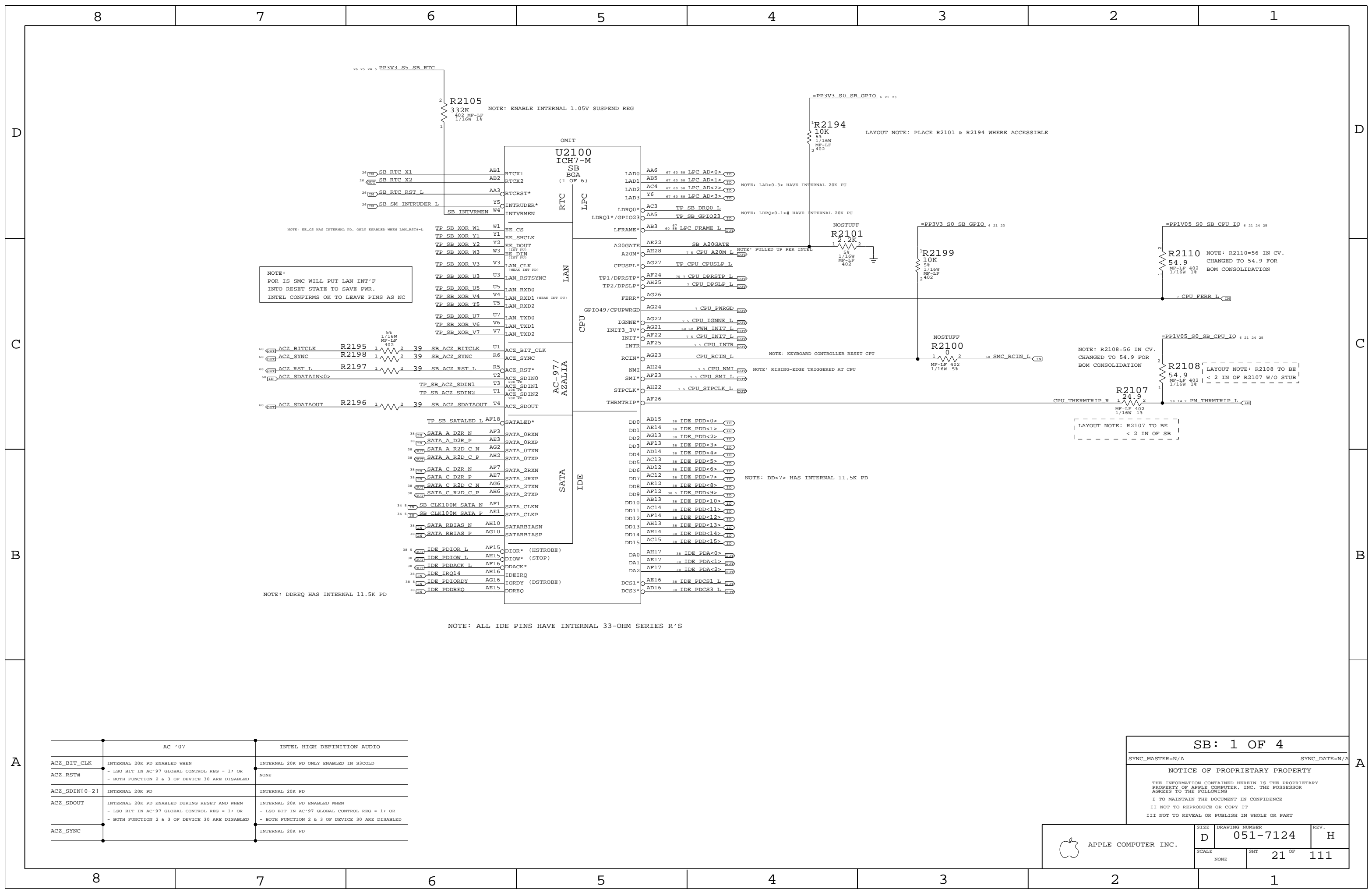
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	H
SCALE	SHT	OF	
NONE	20	111	



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

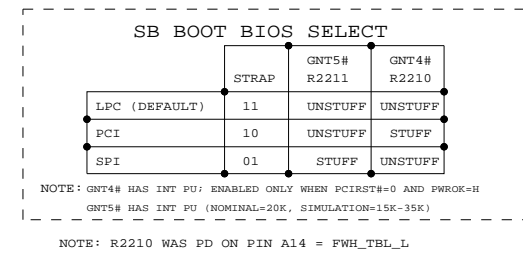
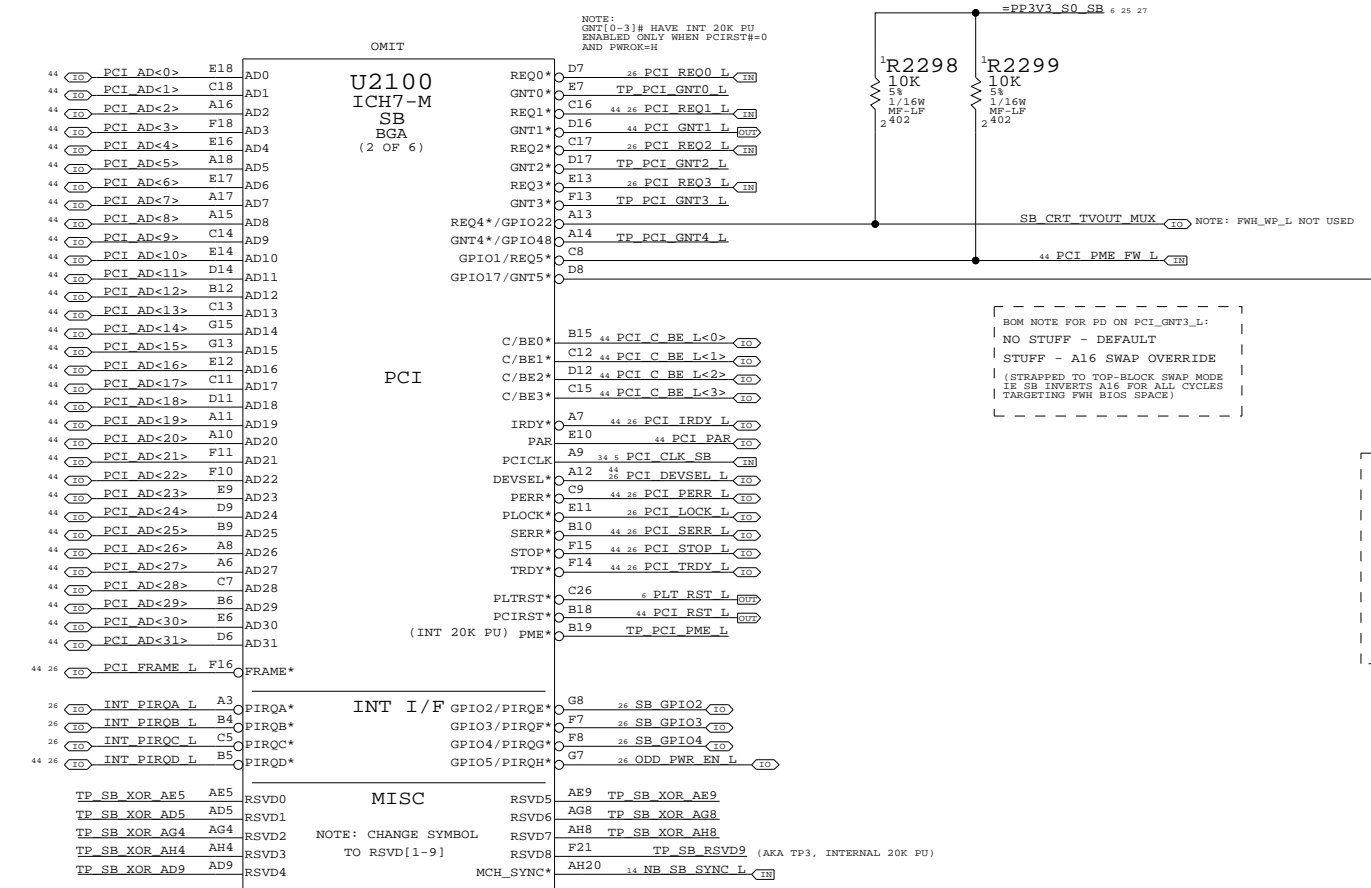
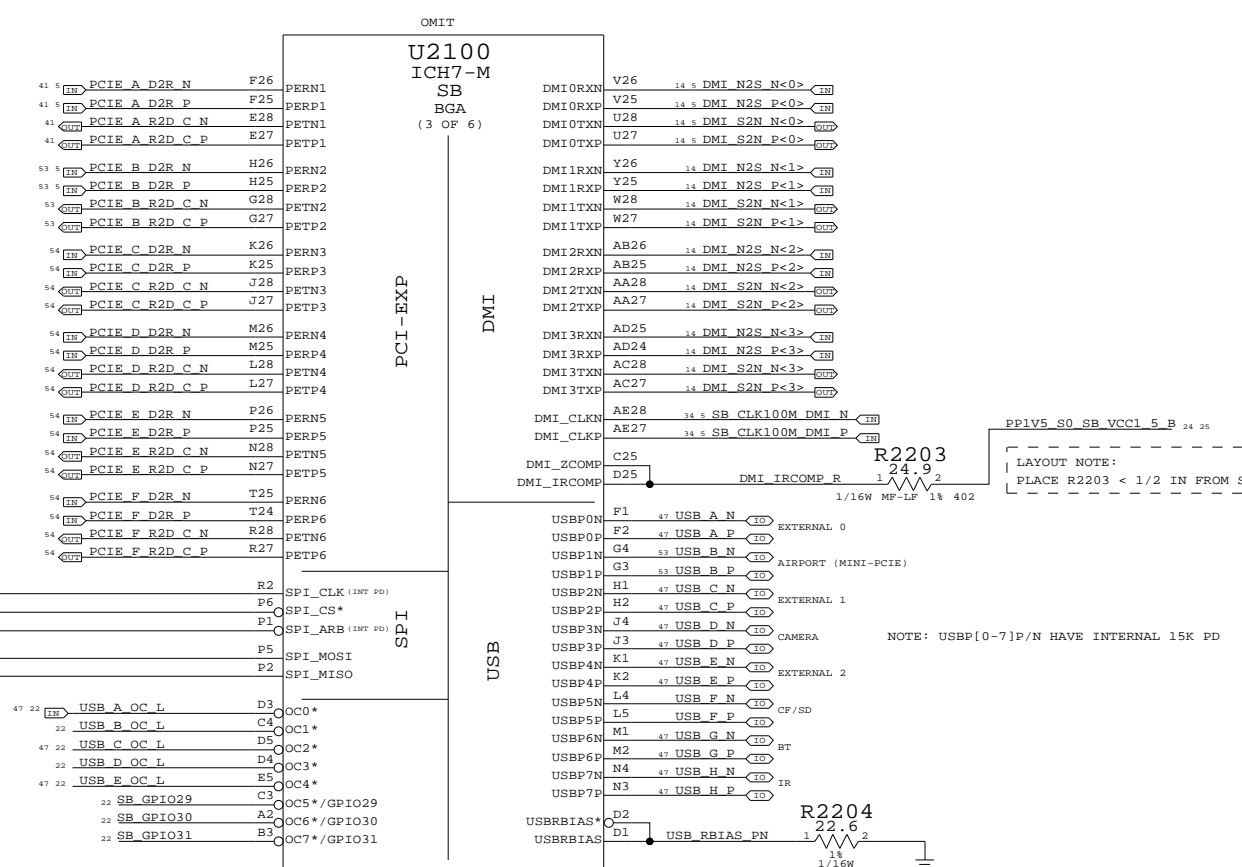
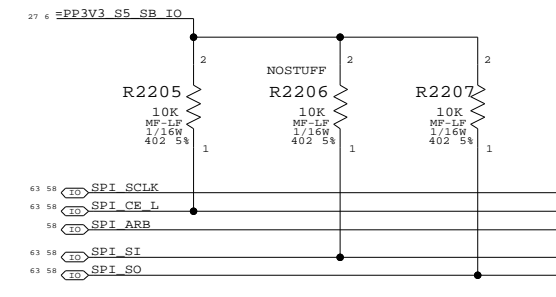
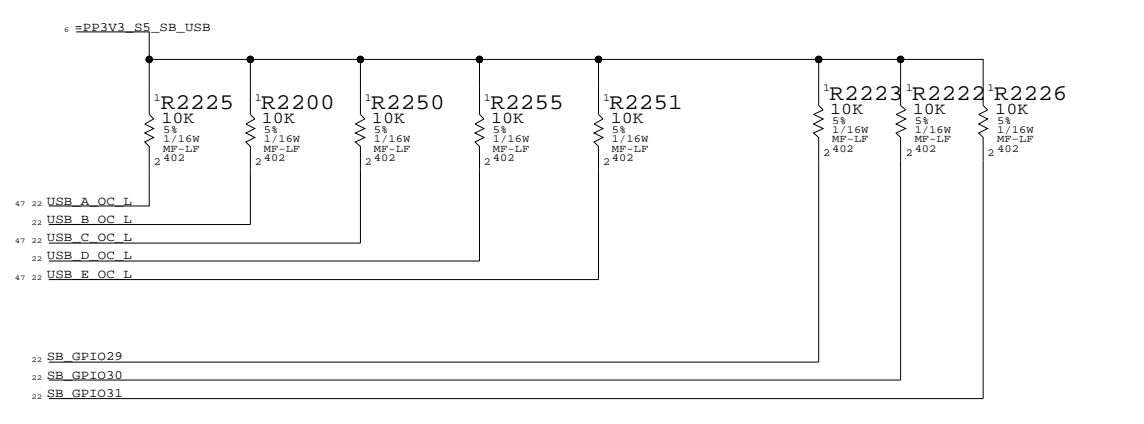
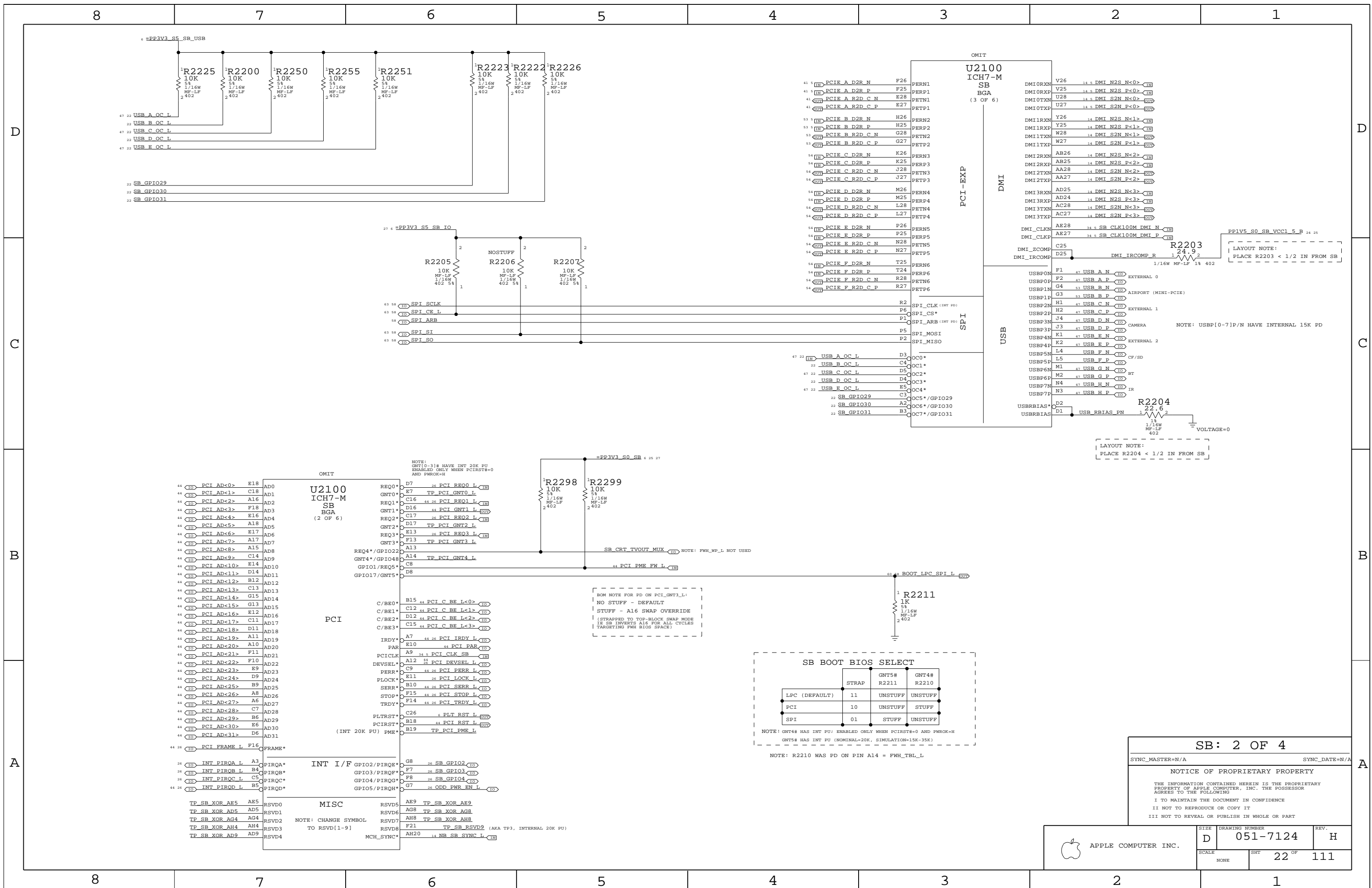
SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7124	H
SCALE	SHT	21 OF	111
NONE			



SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

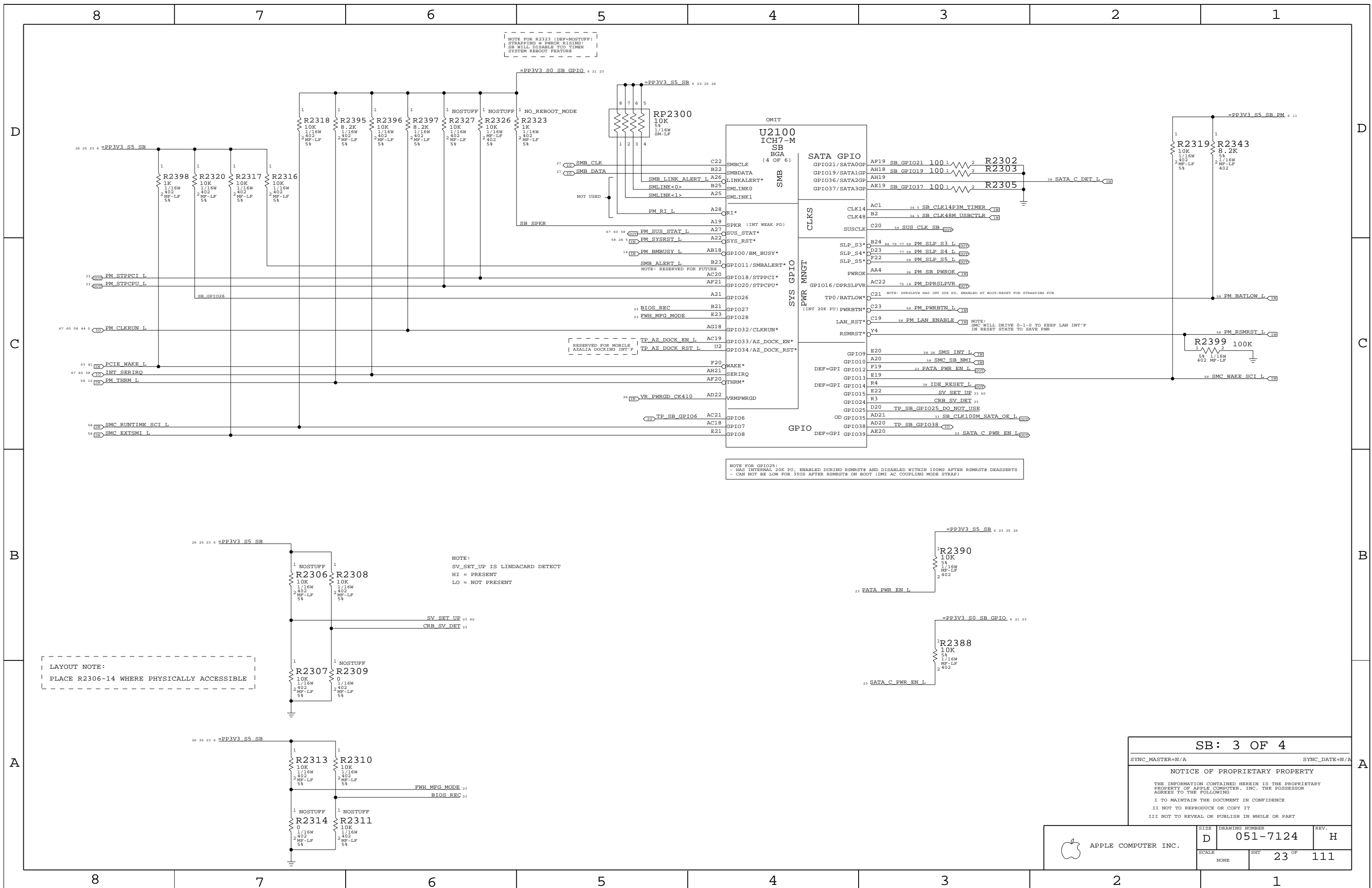
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NOTE FOR R2323 (DEF-NOSTUFF)
STRAPPING & PWROK RISING:
SB WILL DISABLE TOO TIMER
SYSTEM REBOOT FEATURE

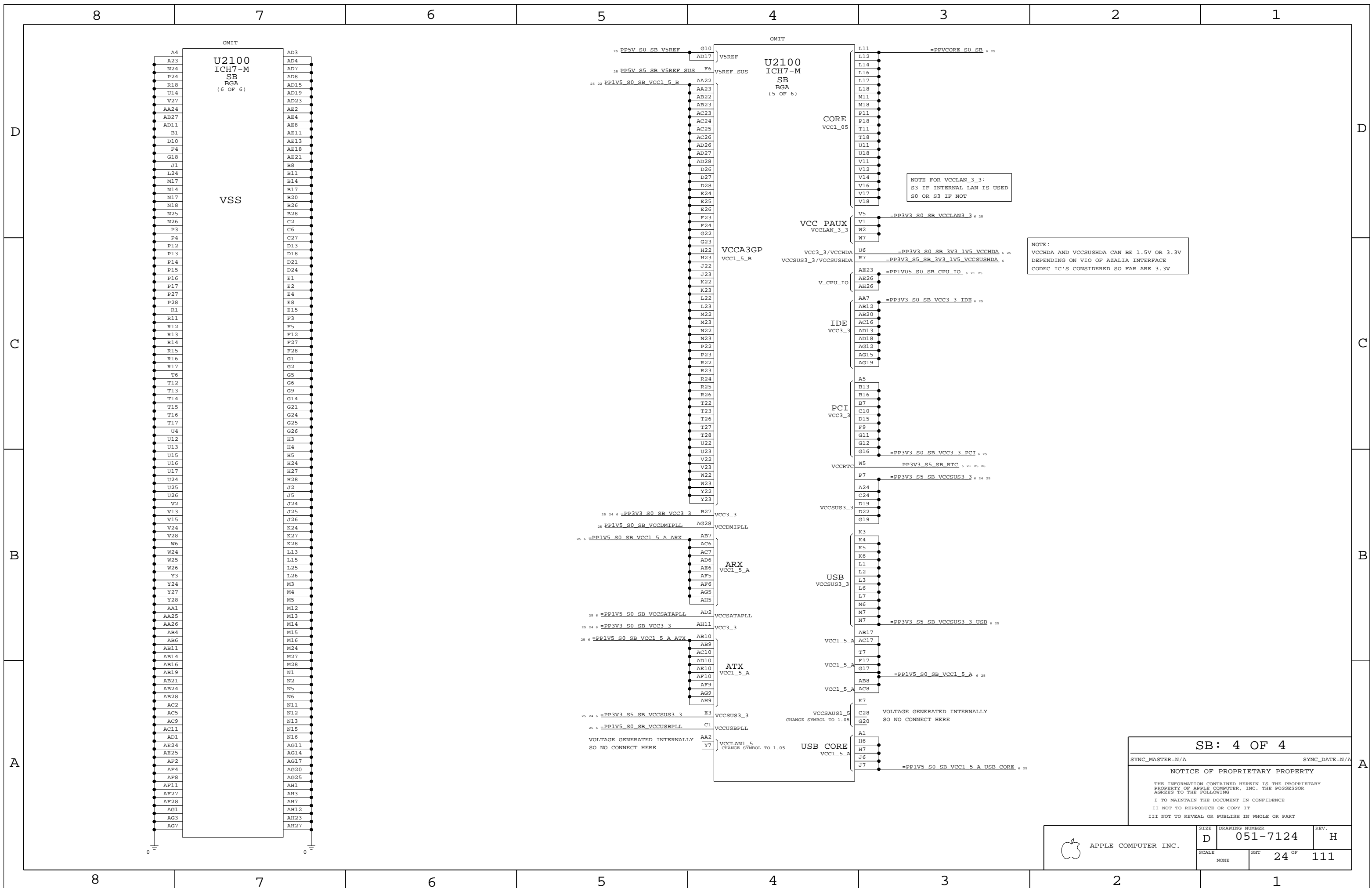
NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SB: 3 OF 4
SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	23 OF	111
NONE			



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCCCHDA AND VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODERC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

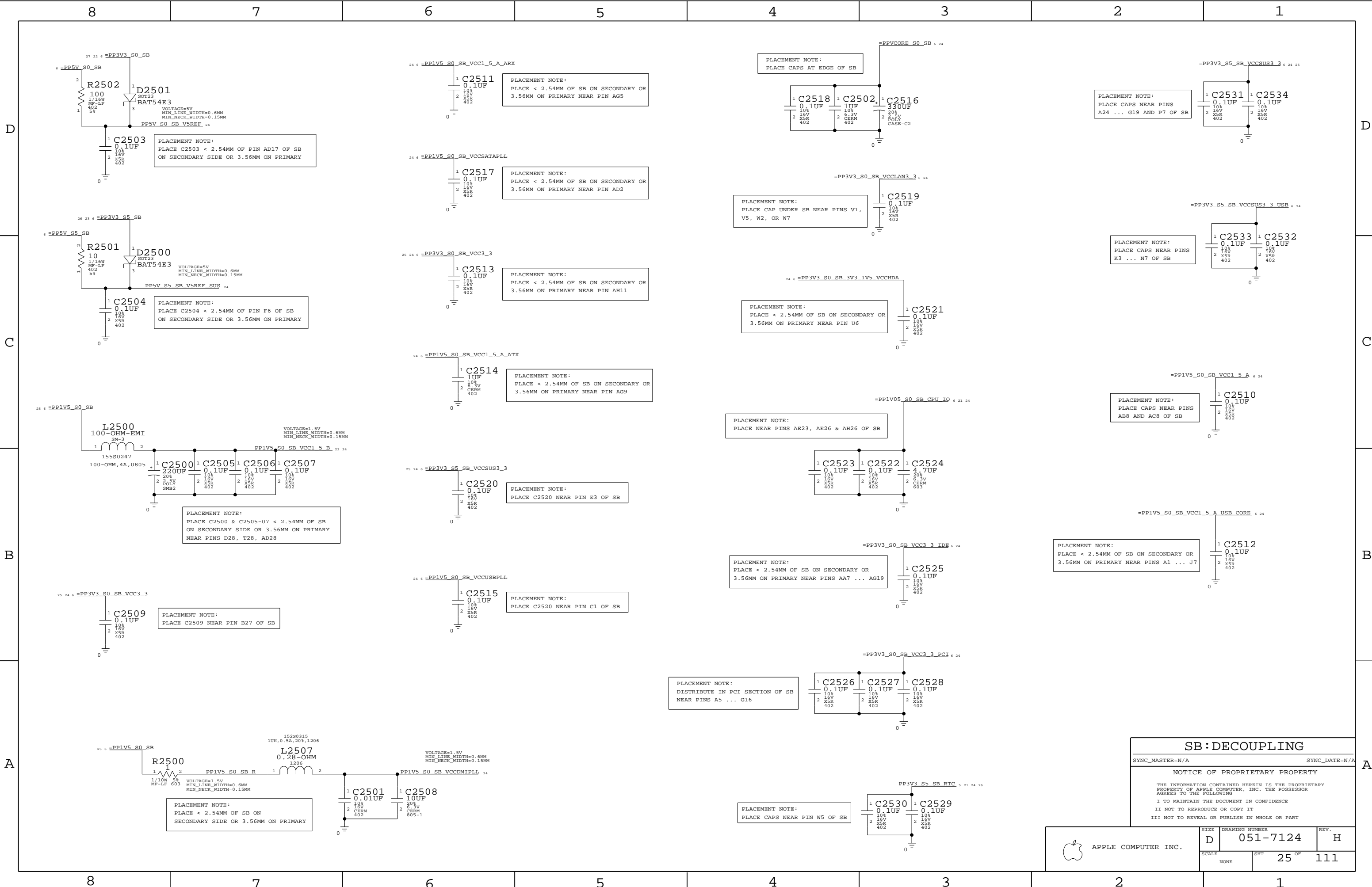
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	D	051-7124	H
SCALE	SHT	24 OF	111
NONE			



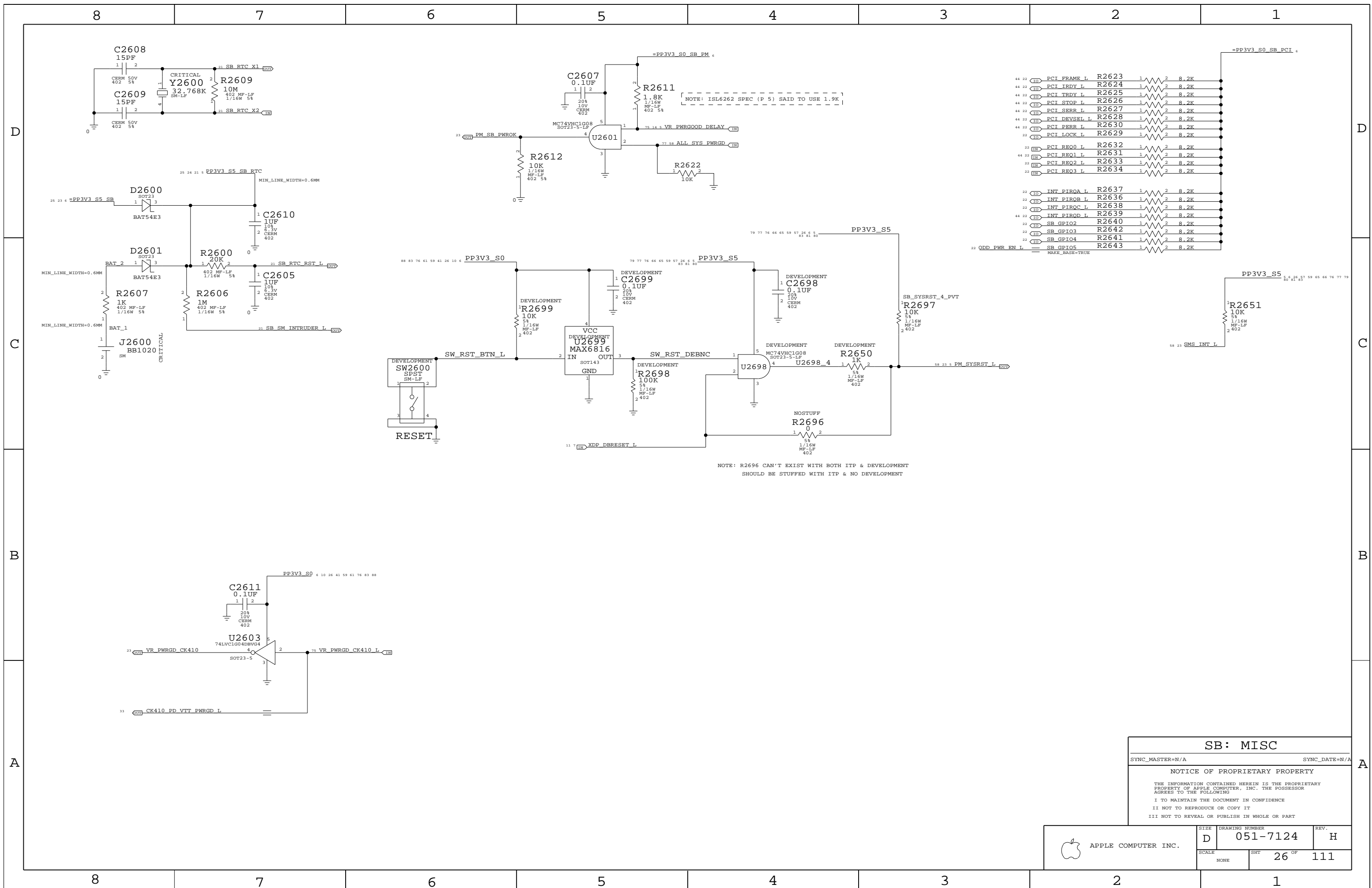
SB : DECOUPLING

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	25 OF	111
NONE			



SB: MISC

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7124	H
SCALE	SHT	26 OF	111
NONE			

NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT

8

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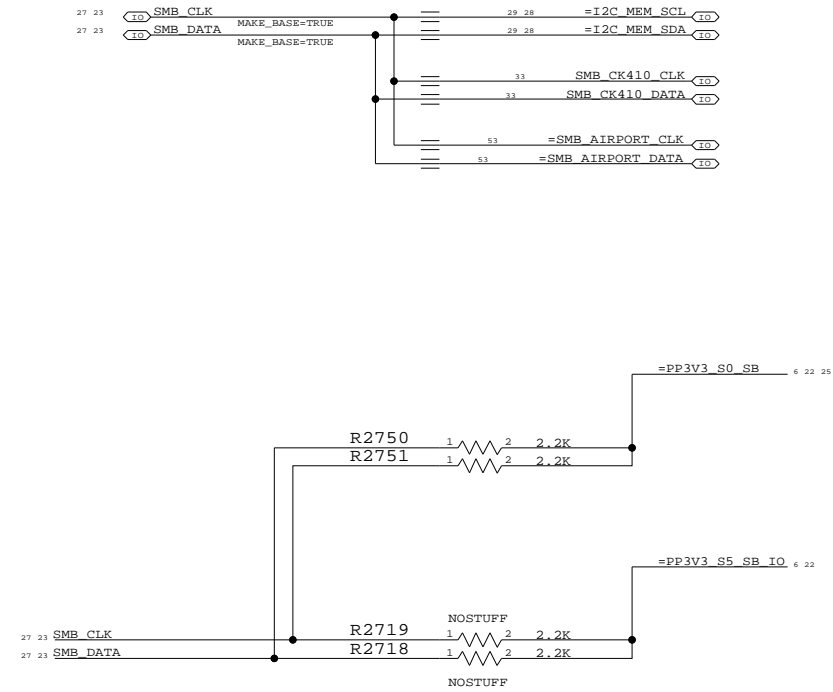
4

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1

SB I2C BUSSES



SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7124	H
SCALE	SHT	OF
NONE	27	111

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Page Notes

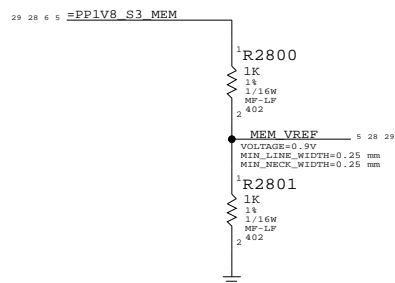
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

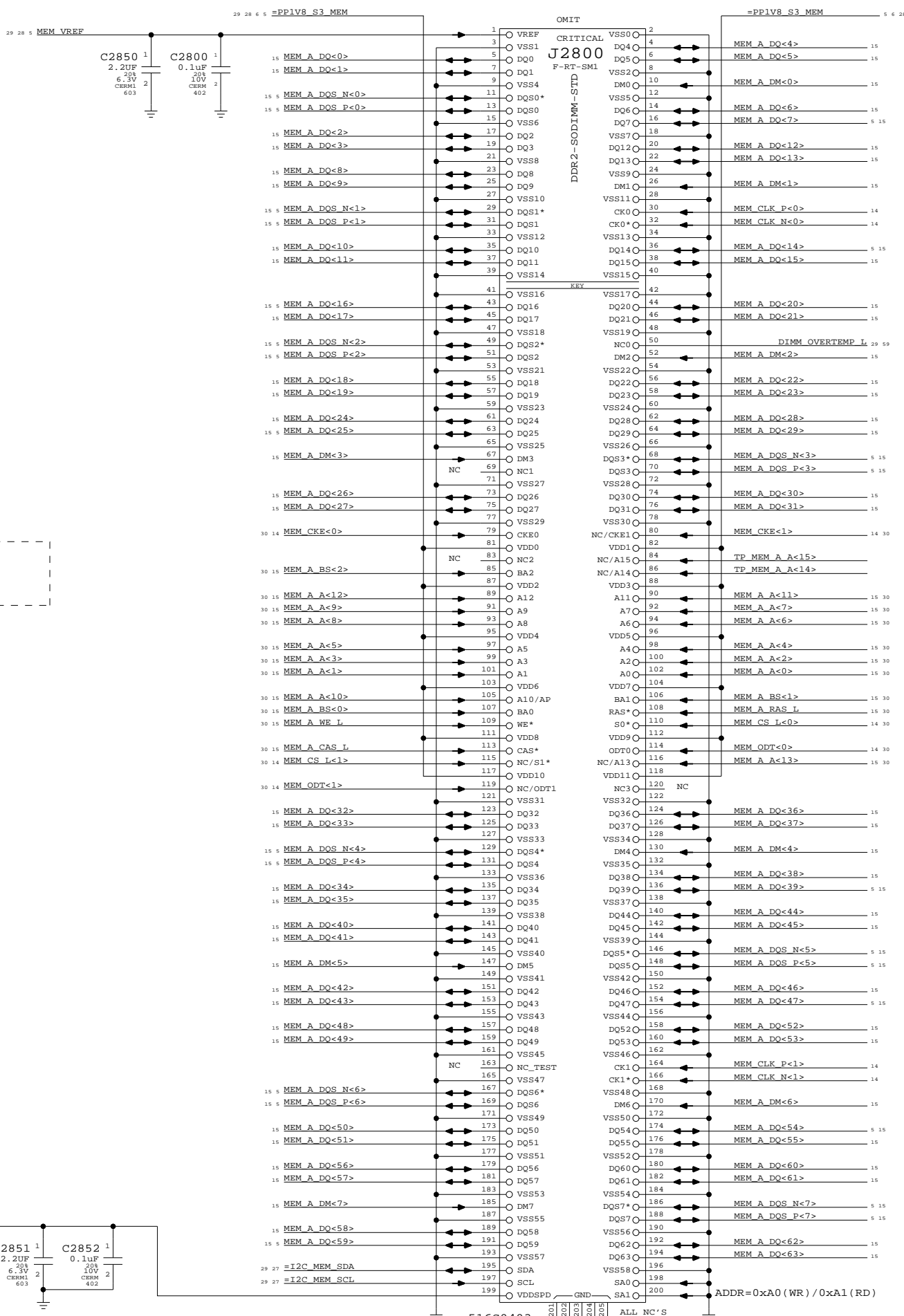
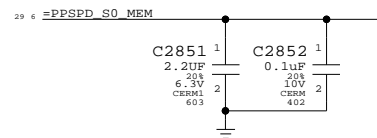
BOM options provided by this page:
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DDR2 VRef

One 0.1uF per connector



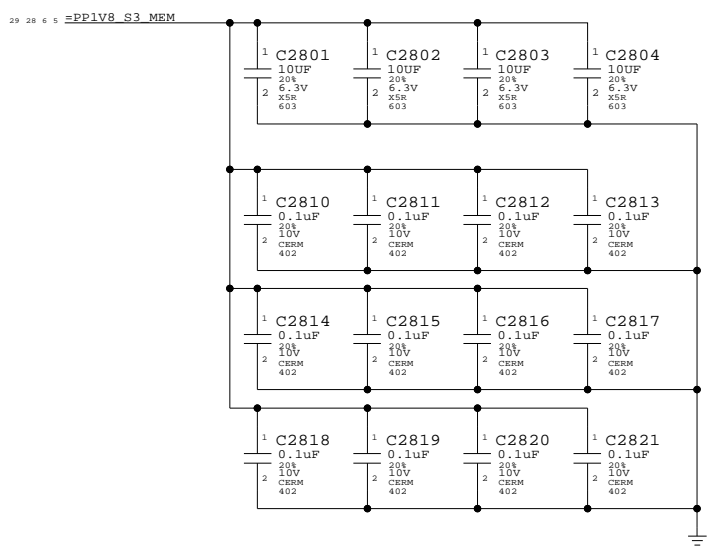
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
 (See Capell Valley pg 47)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0503	1	DDR2 SODIMM STD	J2800	CRITICAL	

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7124	H
SCALE	SHT	OF	
NONE	28	111	

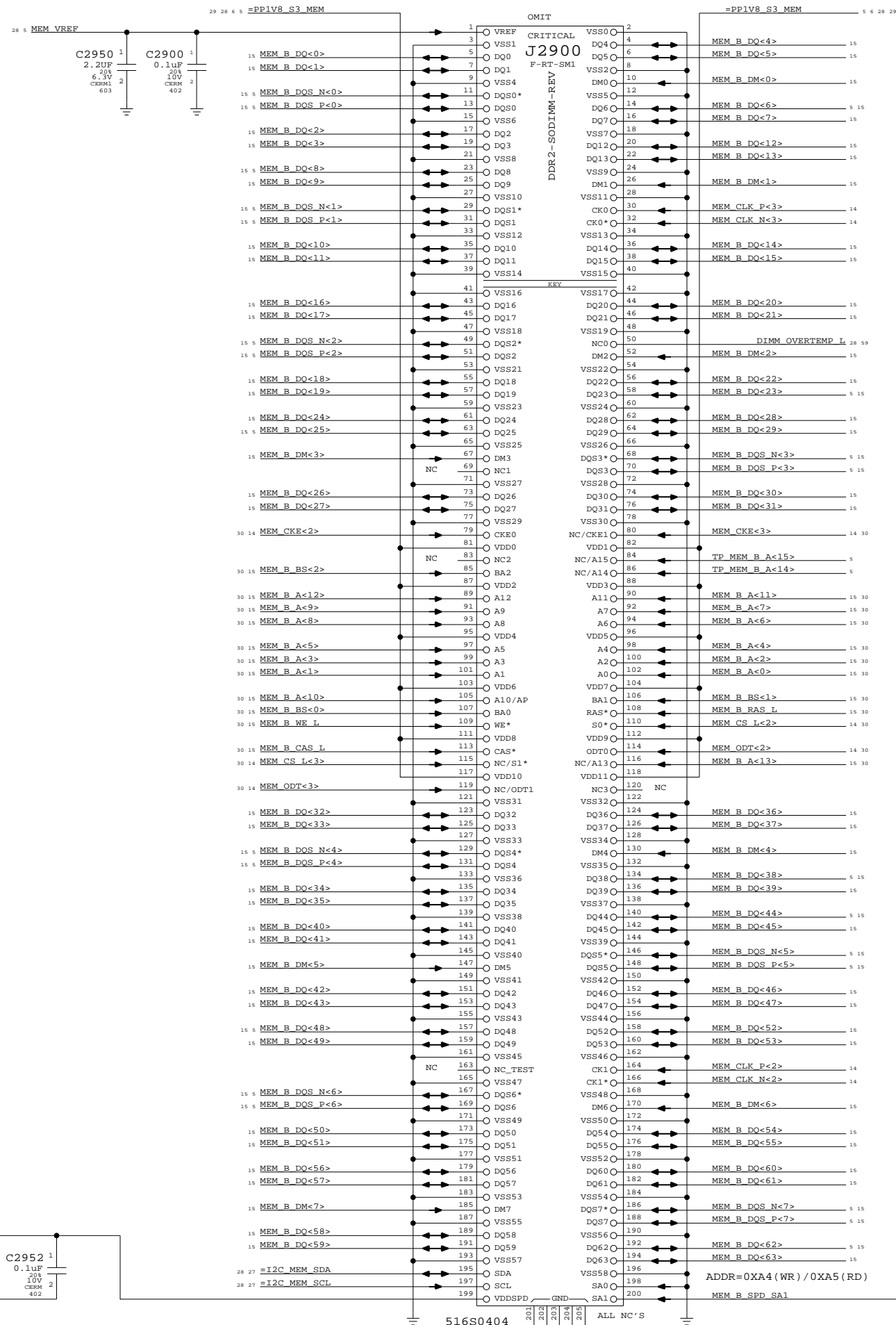
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

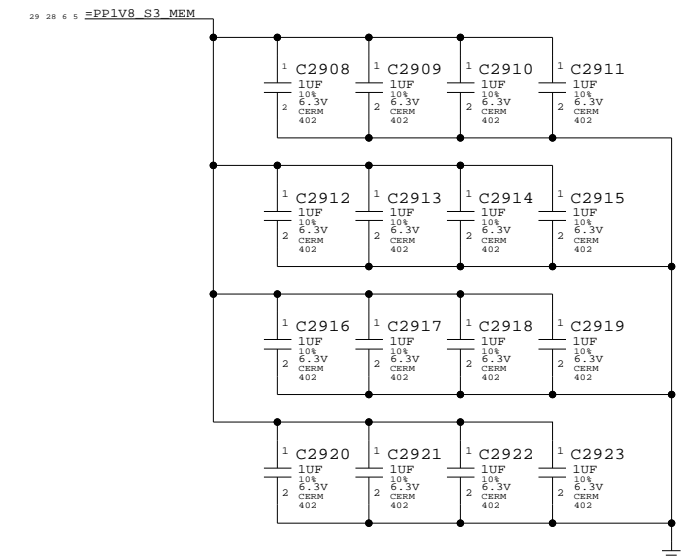
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0504	1	DDR2 SODIMM REV	J2900	CRITICAL	

DDR2 Bypass Caps
 (For return current)



DDR2 SO-DIMM Connector B
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	REV.
NONE	29	111	H

APPLE COMPUTER INC.

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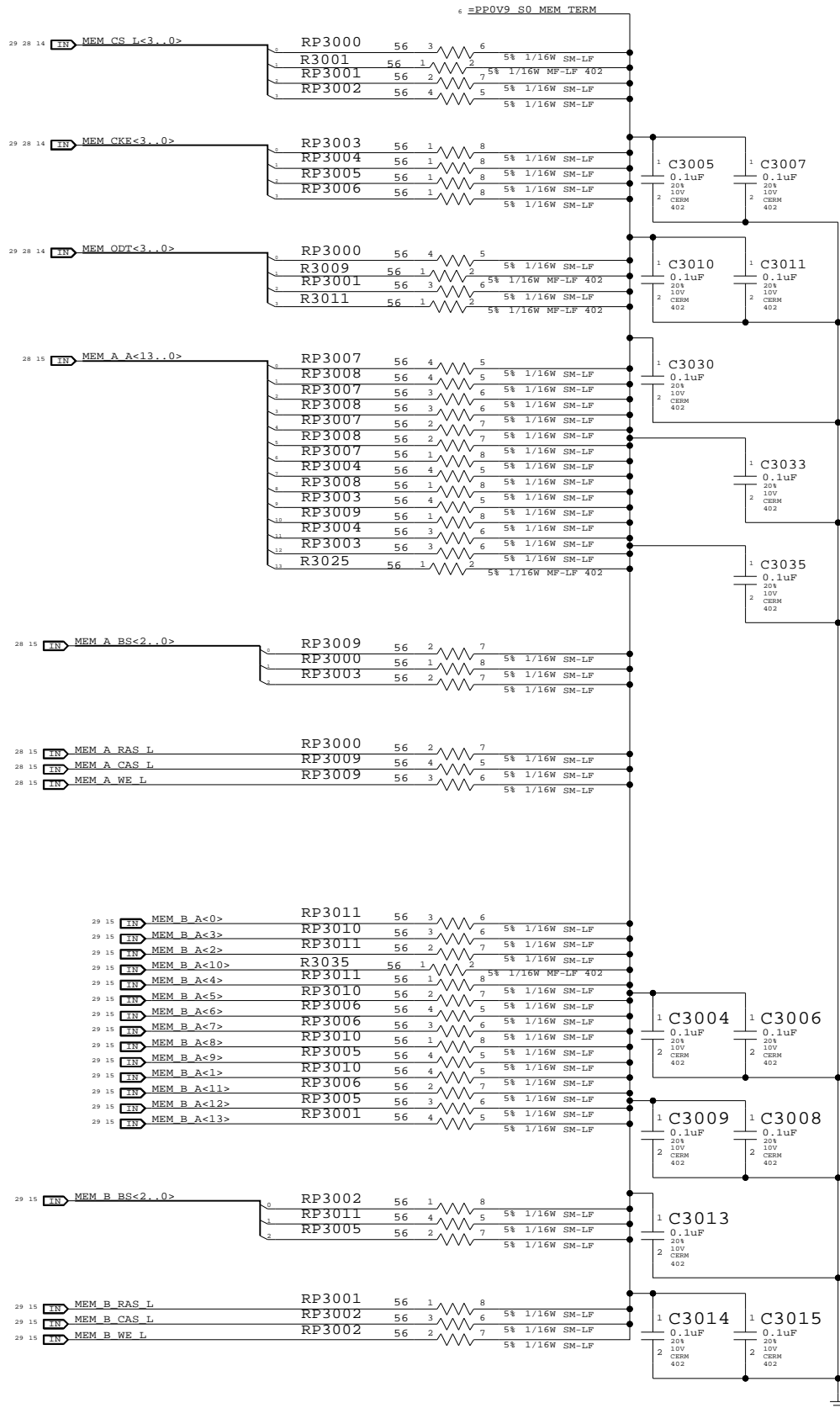
4

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1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7124	H
SCALE	SHT	OF	
NONE	30	111	

8

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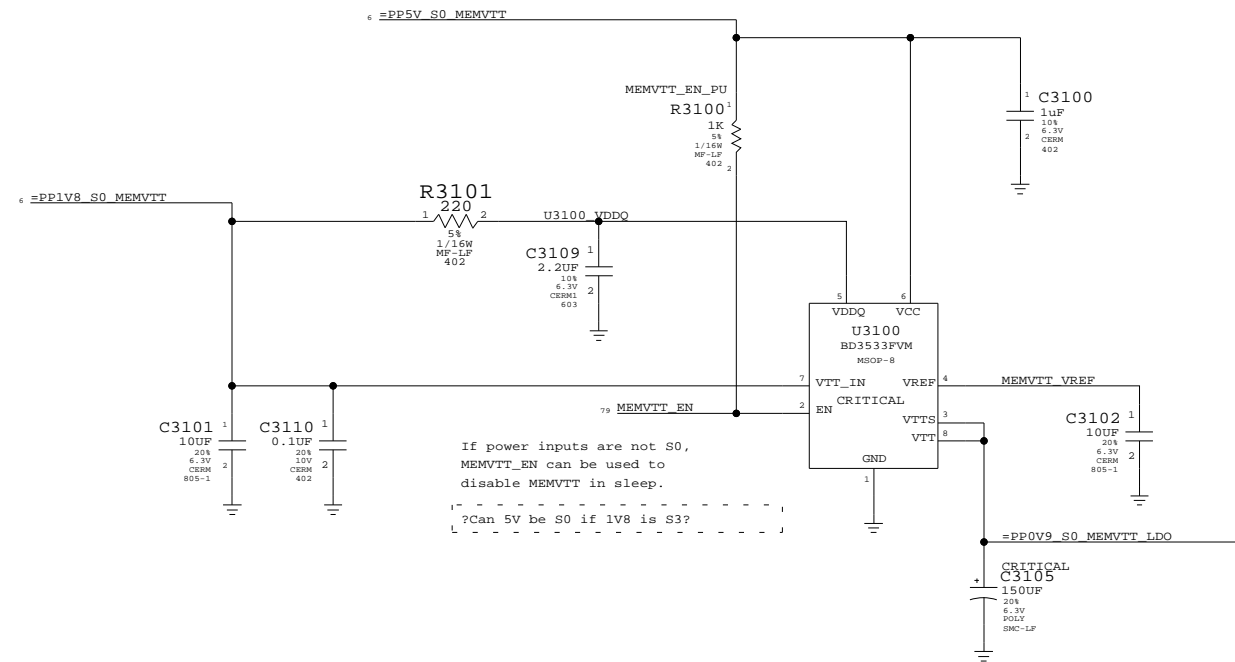
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

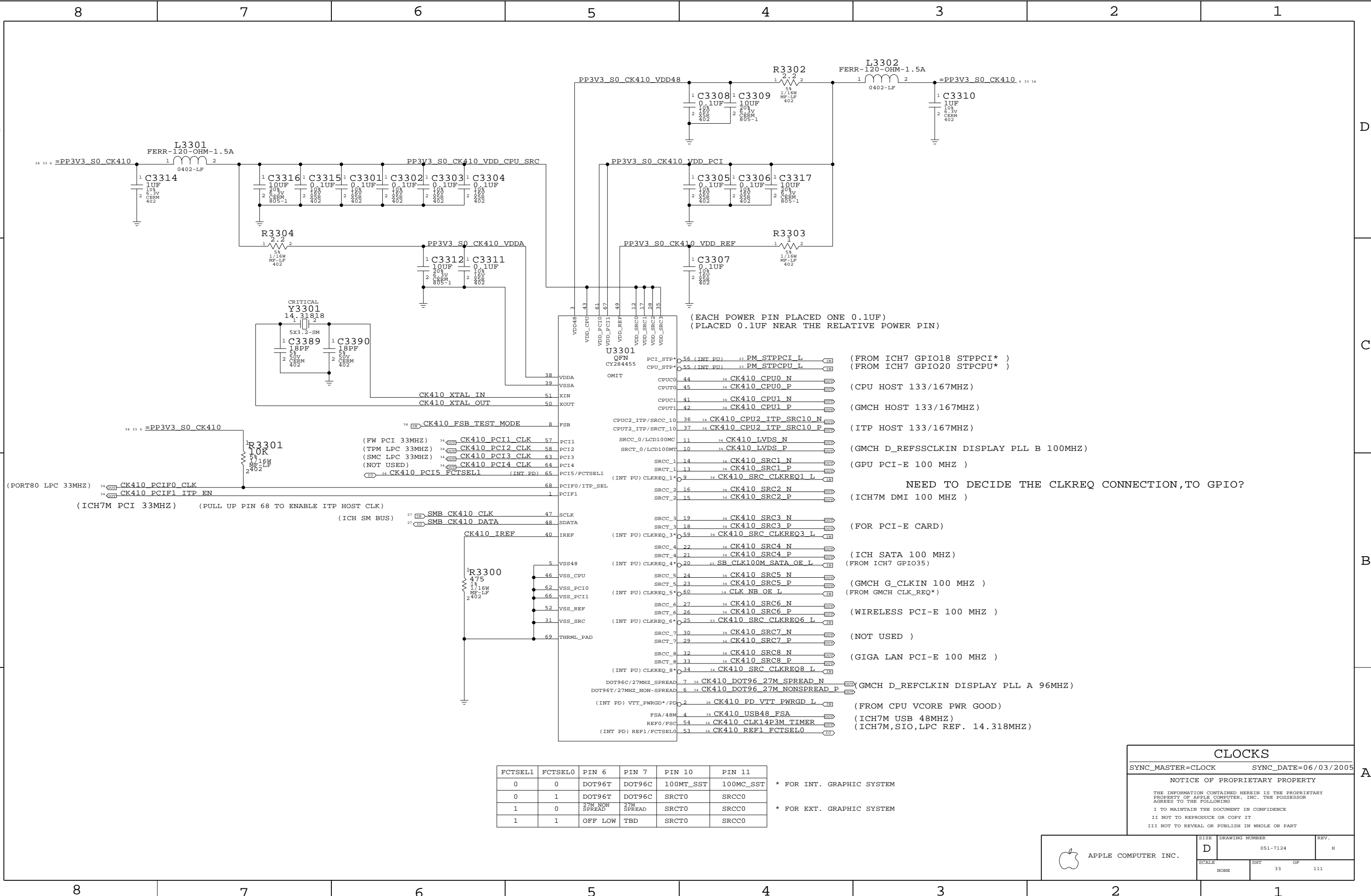
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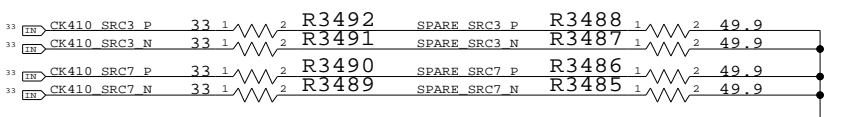
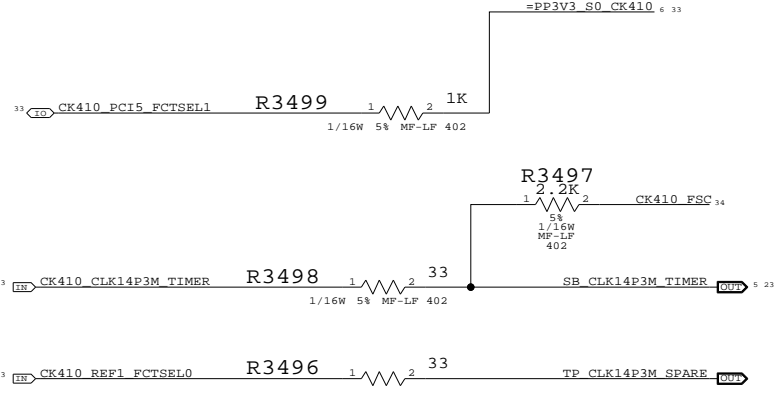
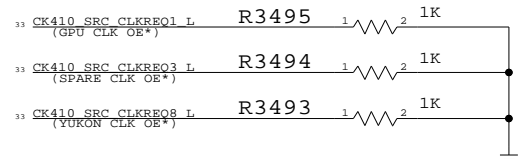
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	REV.
NONE	31	111	



CLOCKS
 SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

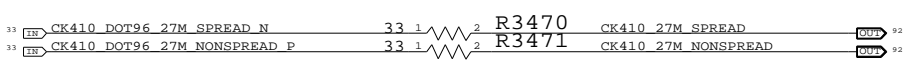
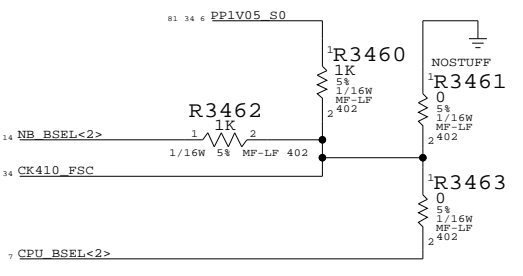
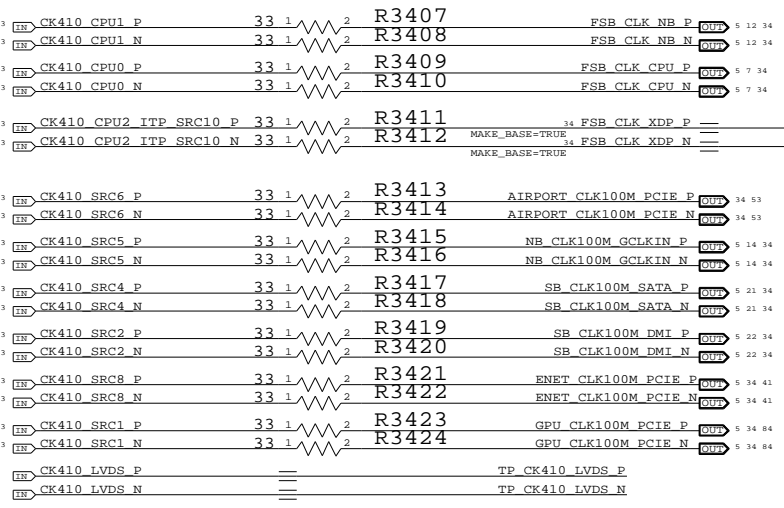
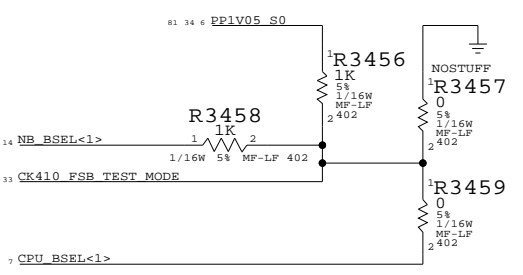
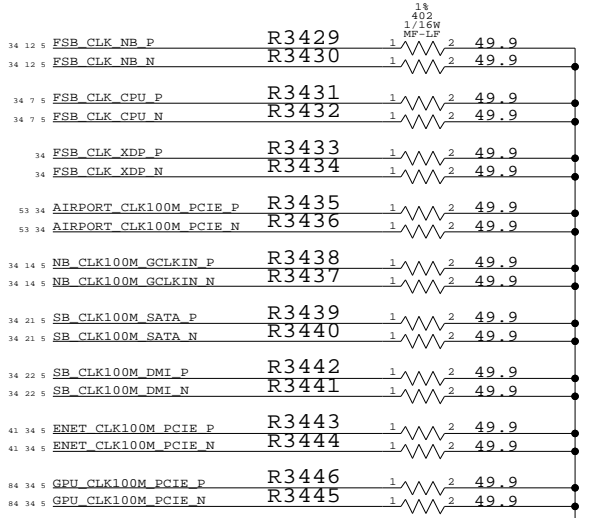
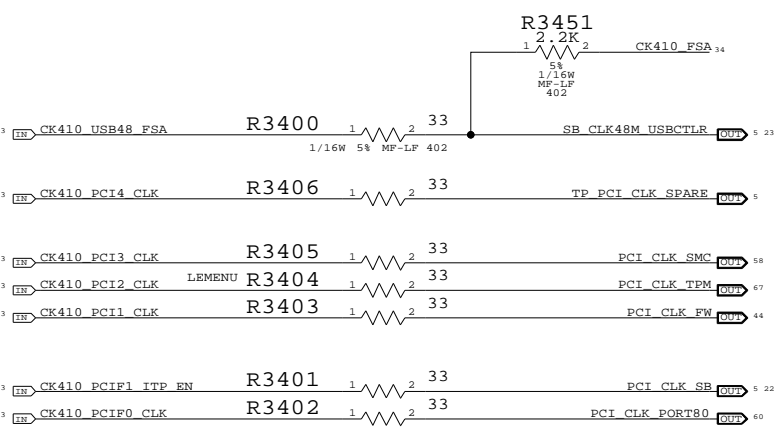
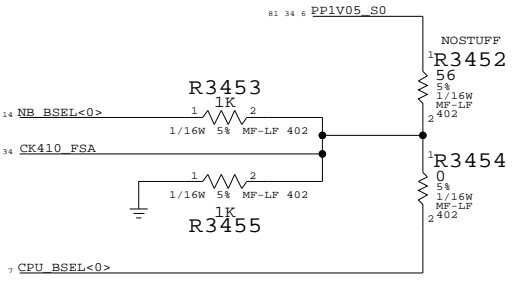
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NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457 R3458
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

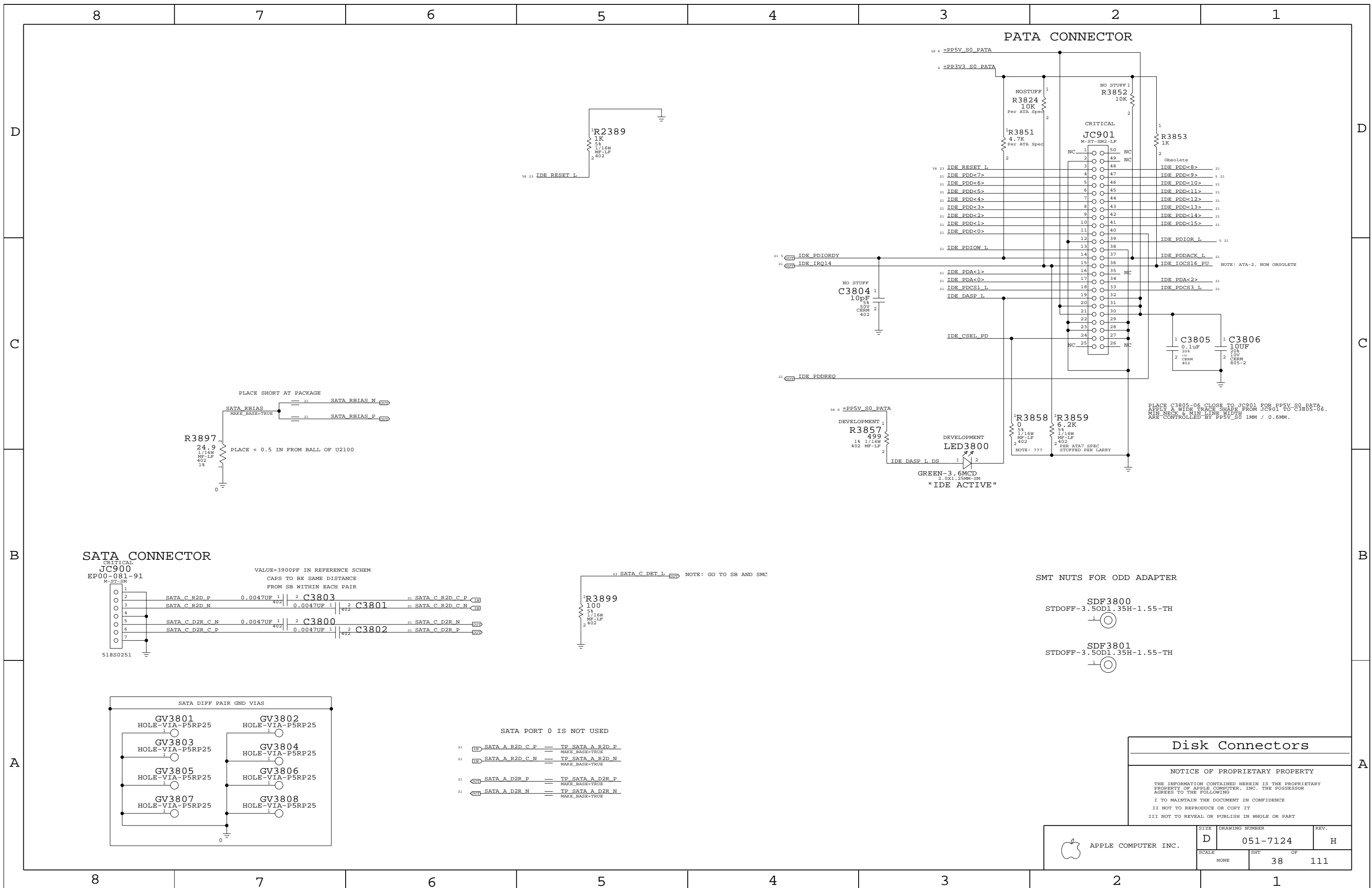
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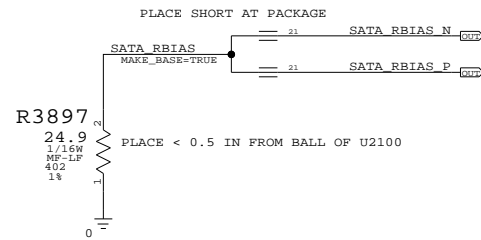
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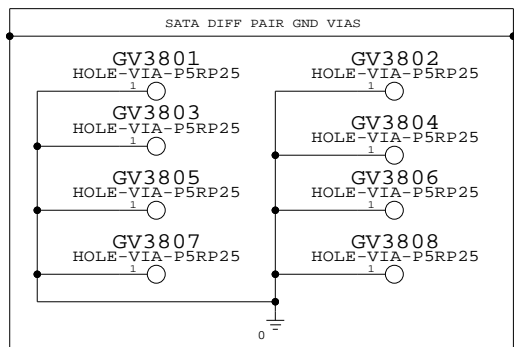
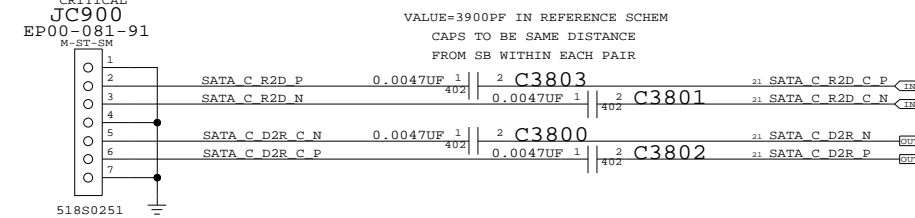
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	REV.
NONE	34	111	



PATA CONNECTOR



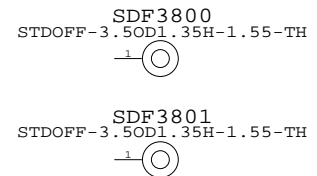
SATA CONNECTOR



SATA PORT 0 IS NOT USED

IN	SATA A R2D C P	TP_SATA A R2D P
		MAKE_BASE=TRUE
IN	SATA A R2D C N	TP_SATA A R2D N
		MAKE_BASE=TRUE
OUT	SATA A D2R P	TP_SATA A D2R P
		MAKE_BASE=TRUE
OUT	SATA A D2R N	TP_SATA A D2R N
		MAKE_BASE=TRUE

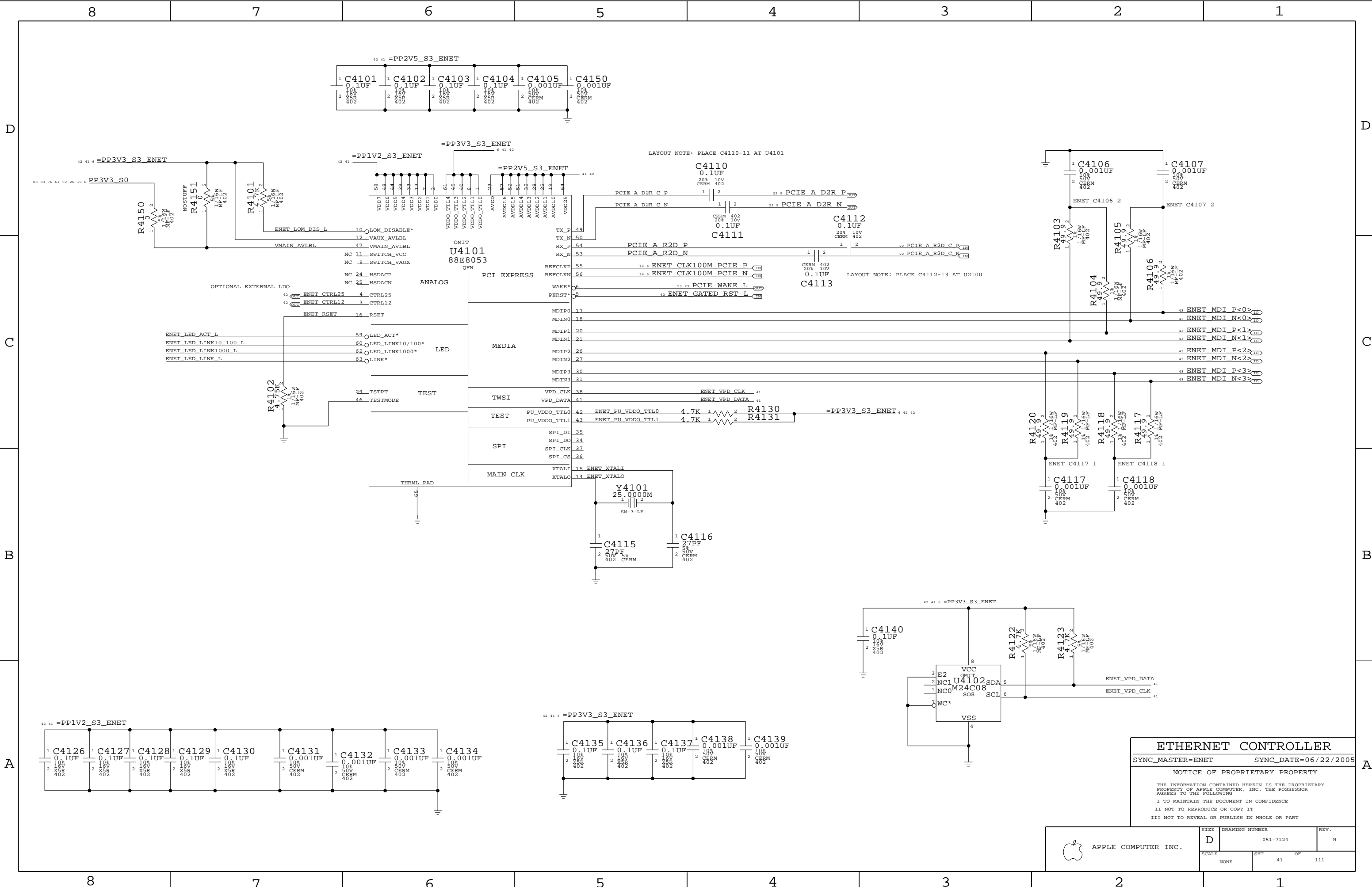
SMT NUTS FOR ODD ADAPTER



Disk Connectors

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	D	051-7124	H
SCALE	SHT OF		
NONE	38		111



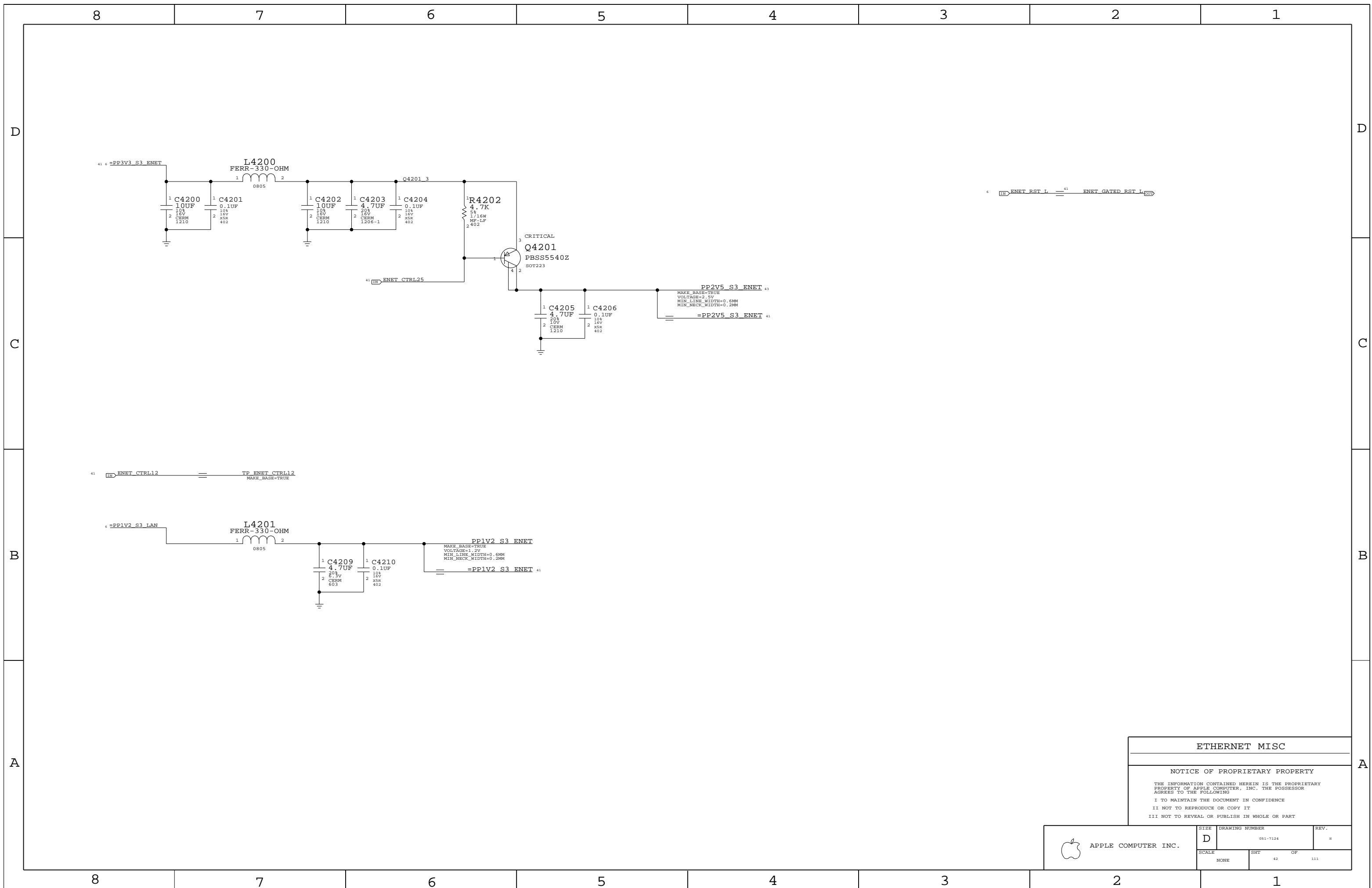
ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 41	OF 111



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

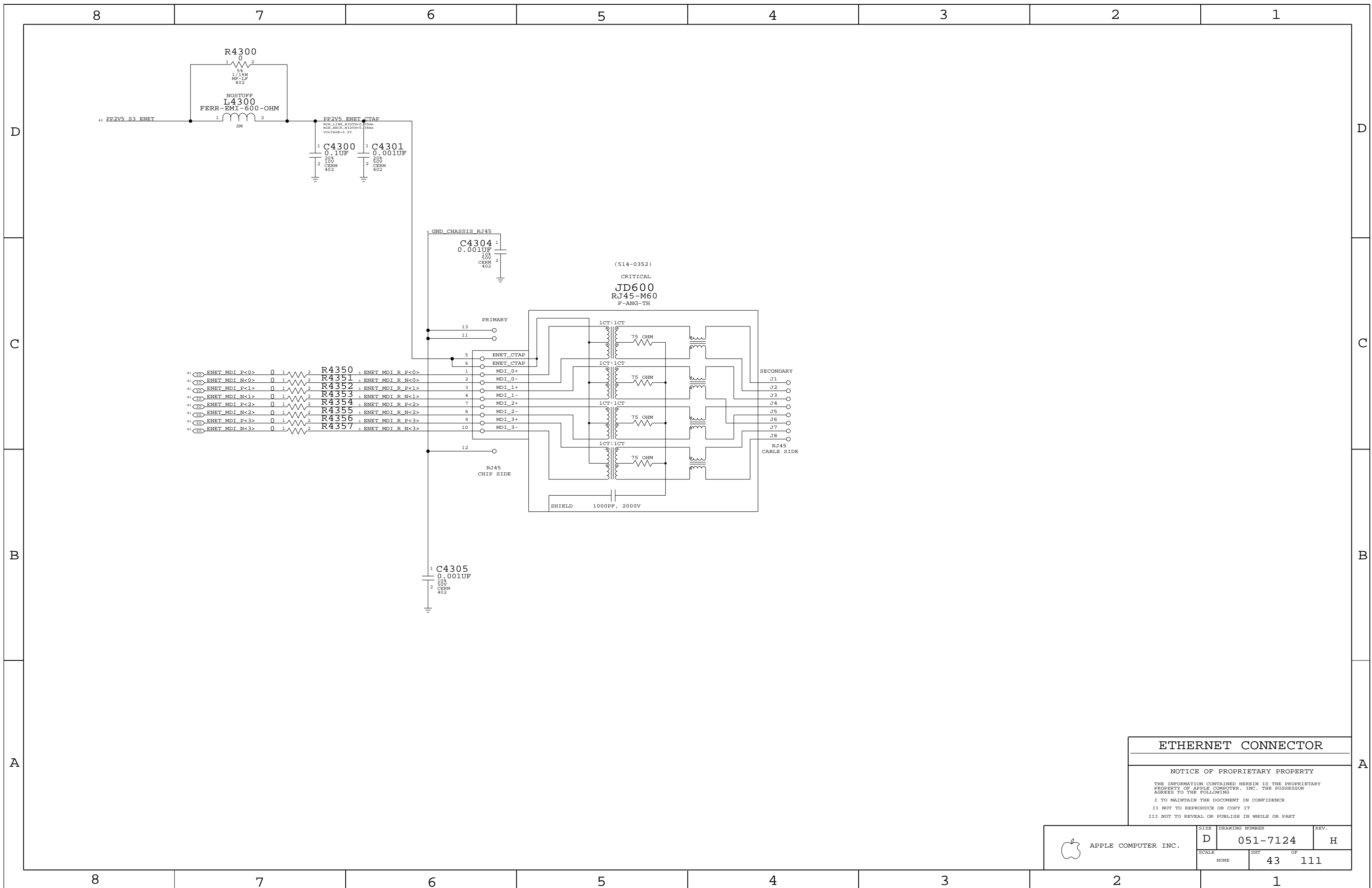
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. B
	SCALE NONE	SHEET 42	OF 111



ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

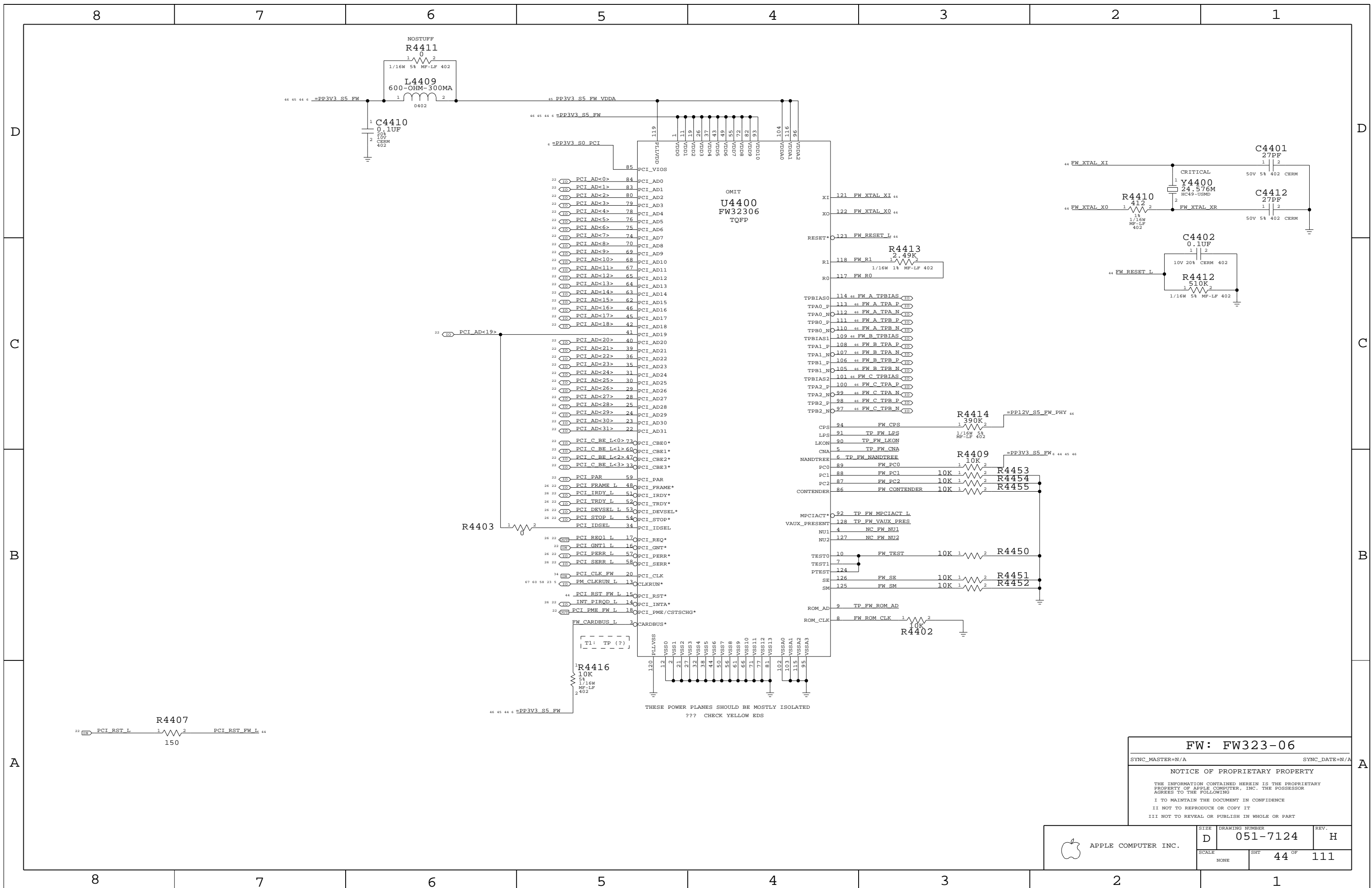
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHIT 43	OF 111



THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
 ??? CHECK YELLOW EDS

FW: FW323-06

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

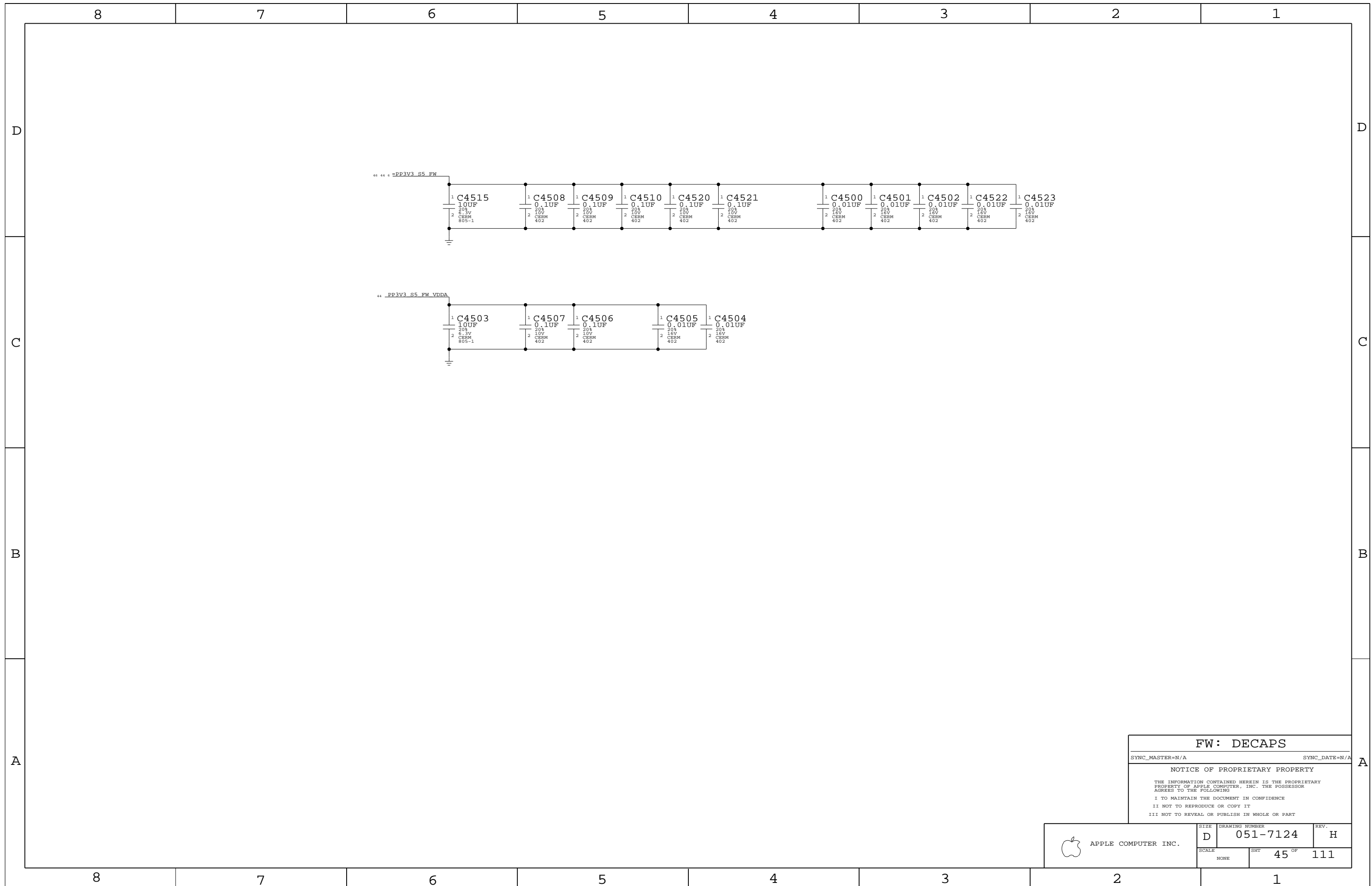
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	D	051-7124	H
SCALE	SHT	44 OF	111
NONE			



FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A


NOTICE OF PROPRIETARY PROPERTY

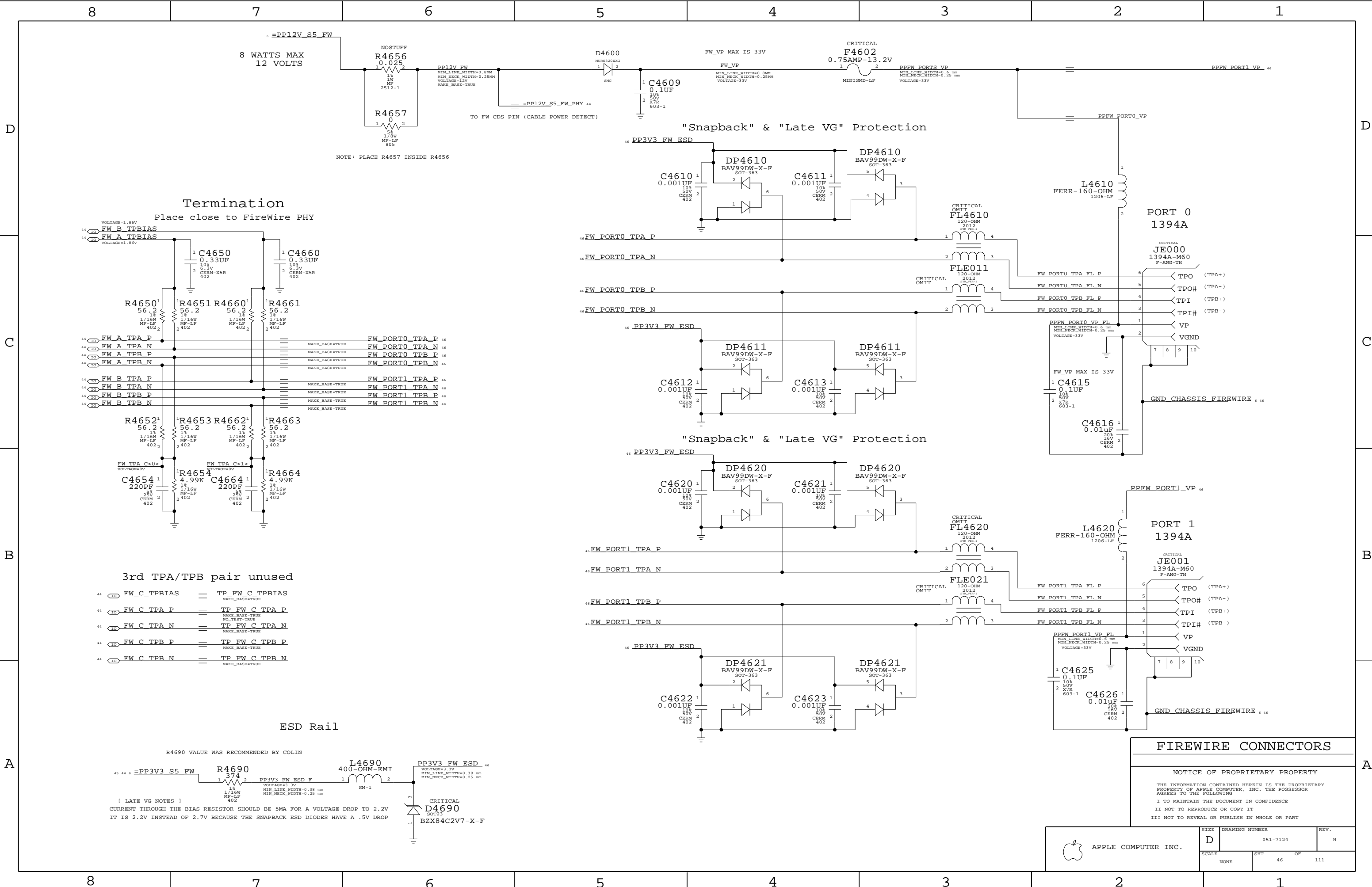
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	D	051-7124	H
SCALE	SHT	OF	REV.
NONE	45	111	



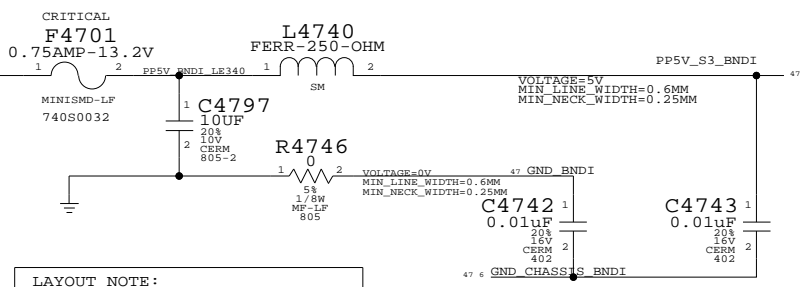
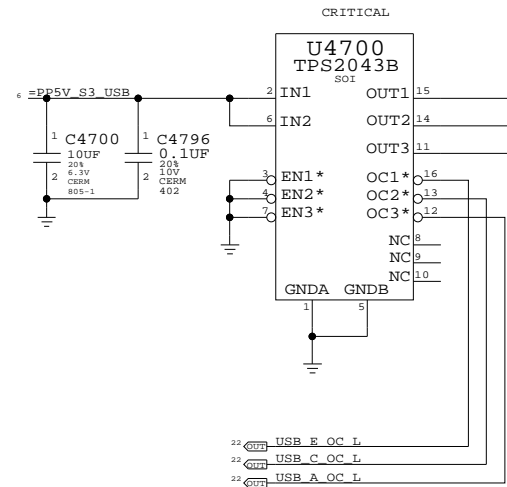
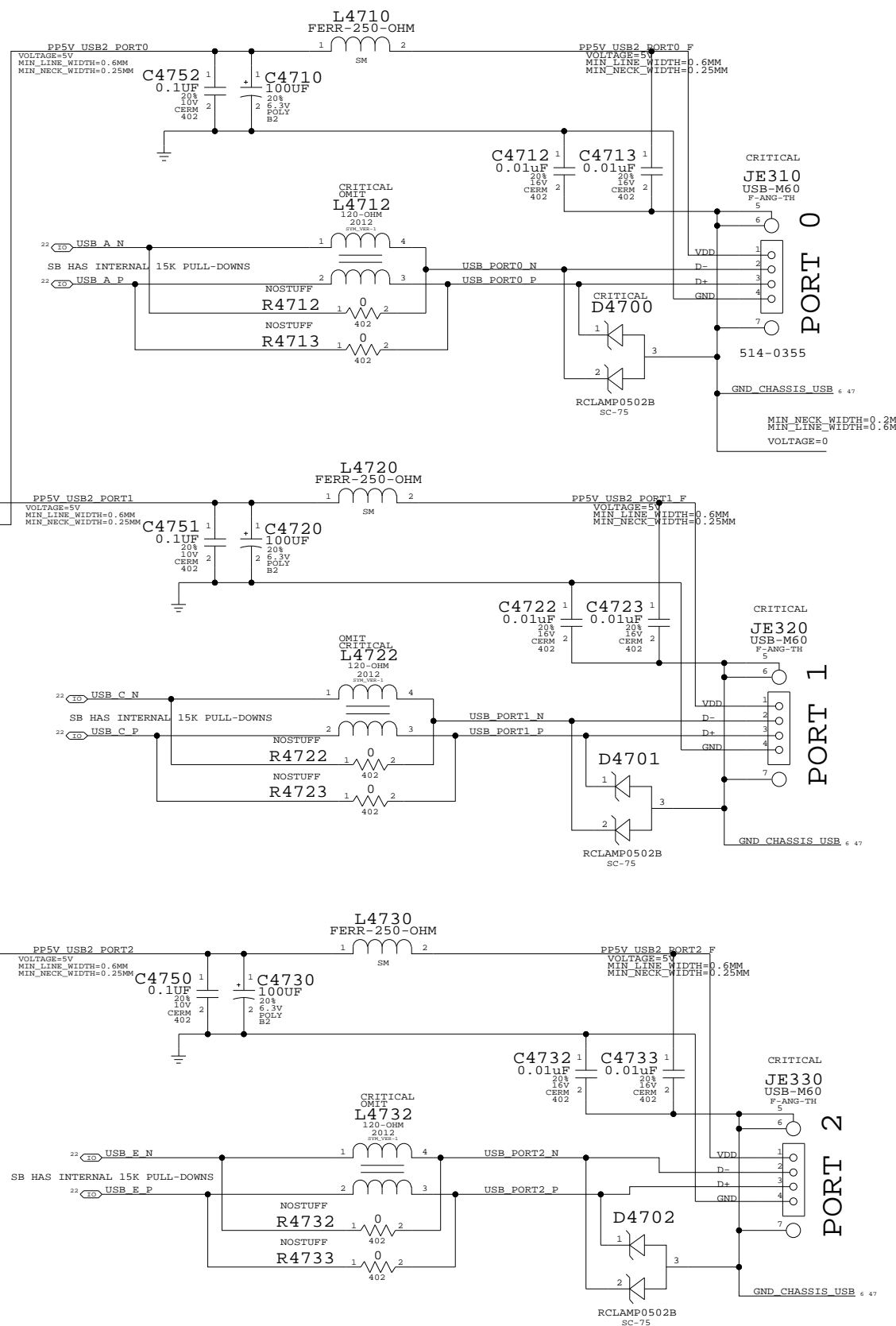
FIREWIRE CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

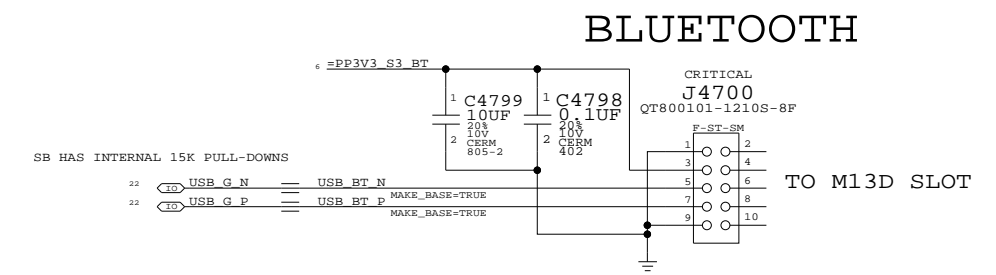
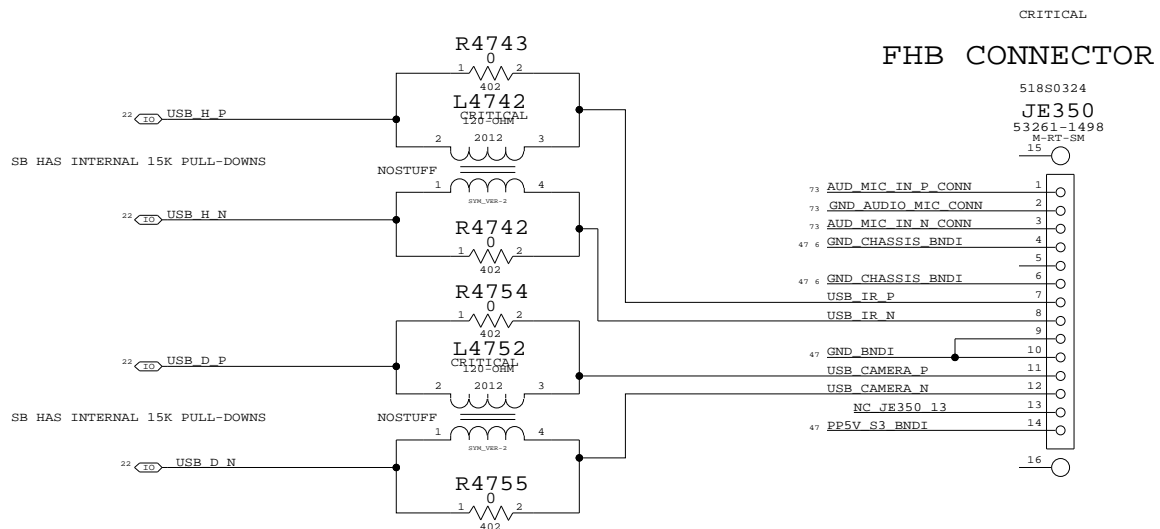
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 46	OF 111

External USB Ports



LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO JE350.



NOTE: STANDOFFS FOR J4700
SDF4700
STDOFF-40D4.5H-1.35-TH
SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

NOTICE OF PROPRIETARY PROPERTY

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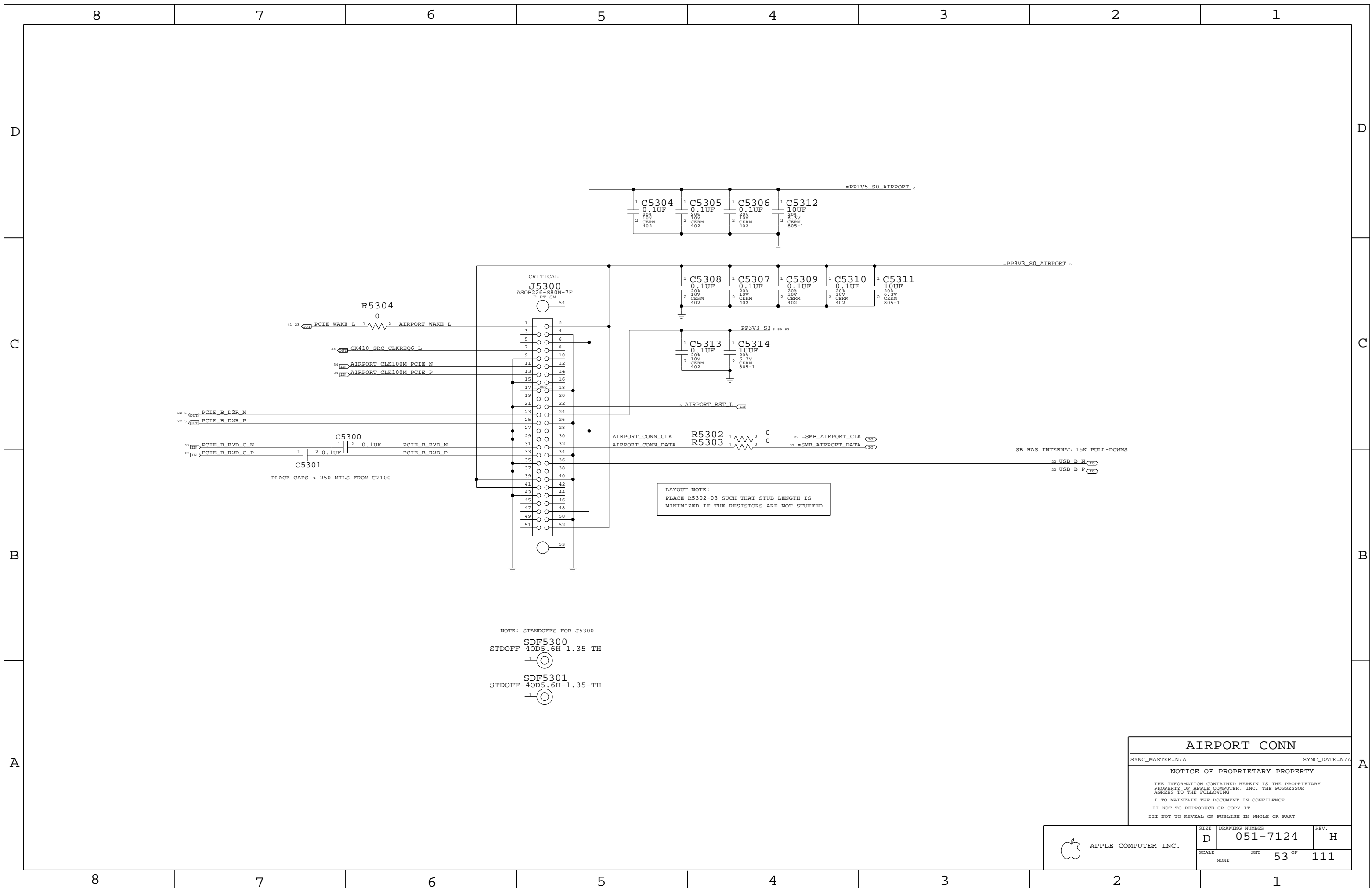
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0355	3	USB RECEPTACLE, 4P, RIBLESS	JE310, JE320, JE330	CRITICAL	20_INCH_LCD

APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	47	111	H



NOTE: STANDOFFS FOR J5300

SDF5300
STDOFF-40D5.6H-1.35-TH

SDF5301
STDOFF-40D5.6H-1.35-TH

LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHIT 53 OF	111

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE

22 PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE

22 PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE

22 PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22 PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22 PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

8

7

6

5

4

3

2

1

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A


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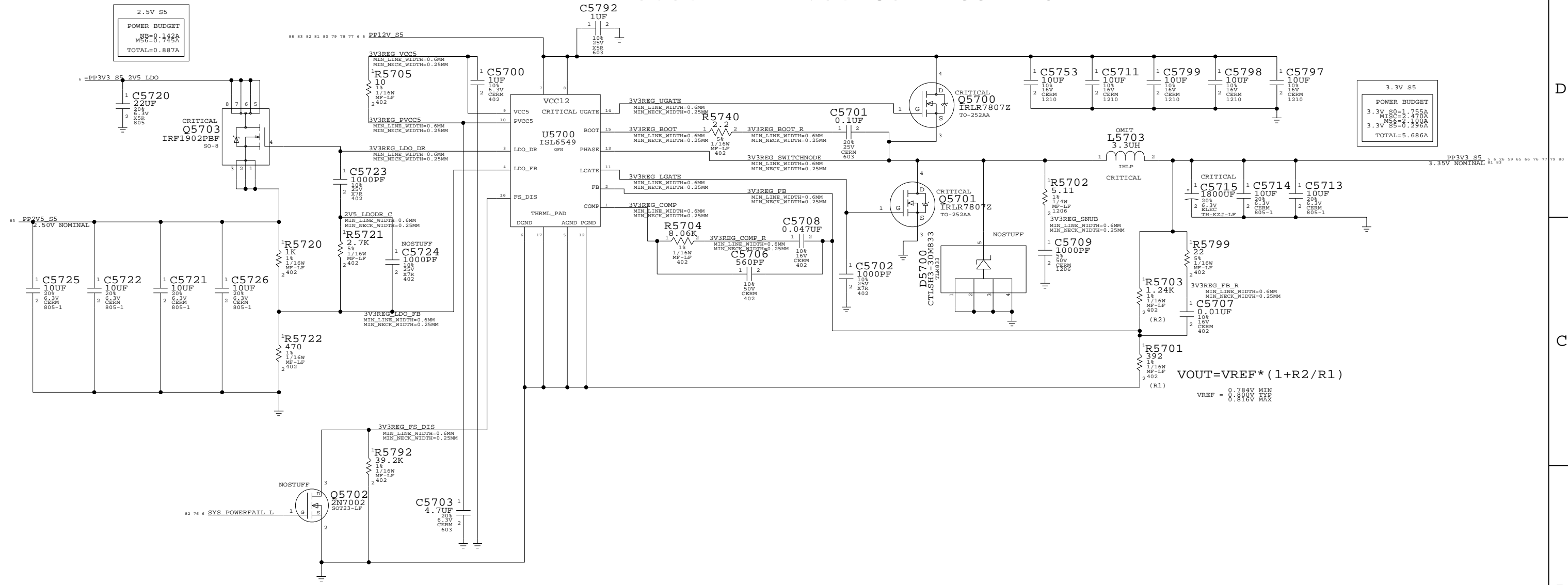
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	54	111	

3.3V AND 2.5V S5 REGULATOR



2.5V S5

POWER BUDGET	
NB=	0.142A
M56=	0.745A
TOTAL=	0.887A

3.3V S5

POWER BUDGET	
3.3V S0=	1.755A
M56=	2.470A
M57=	2.100A
3.3V S5=	0.296A
TOTAL=	5.686A

$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

3.3V DC/DC 2.5V

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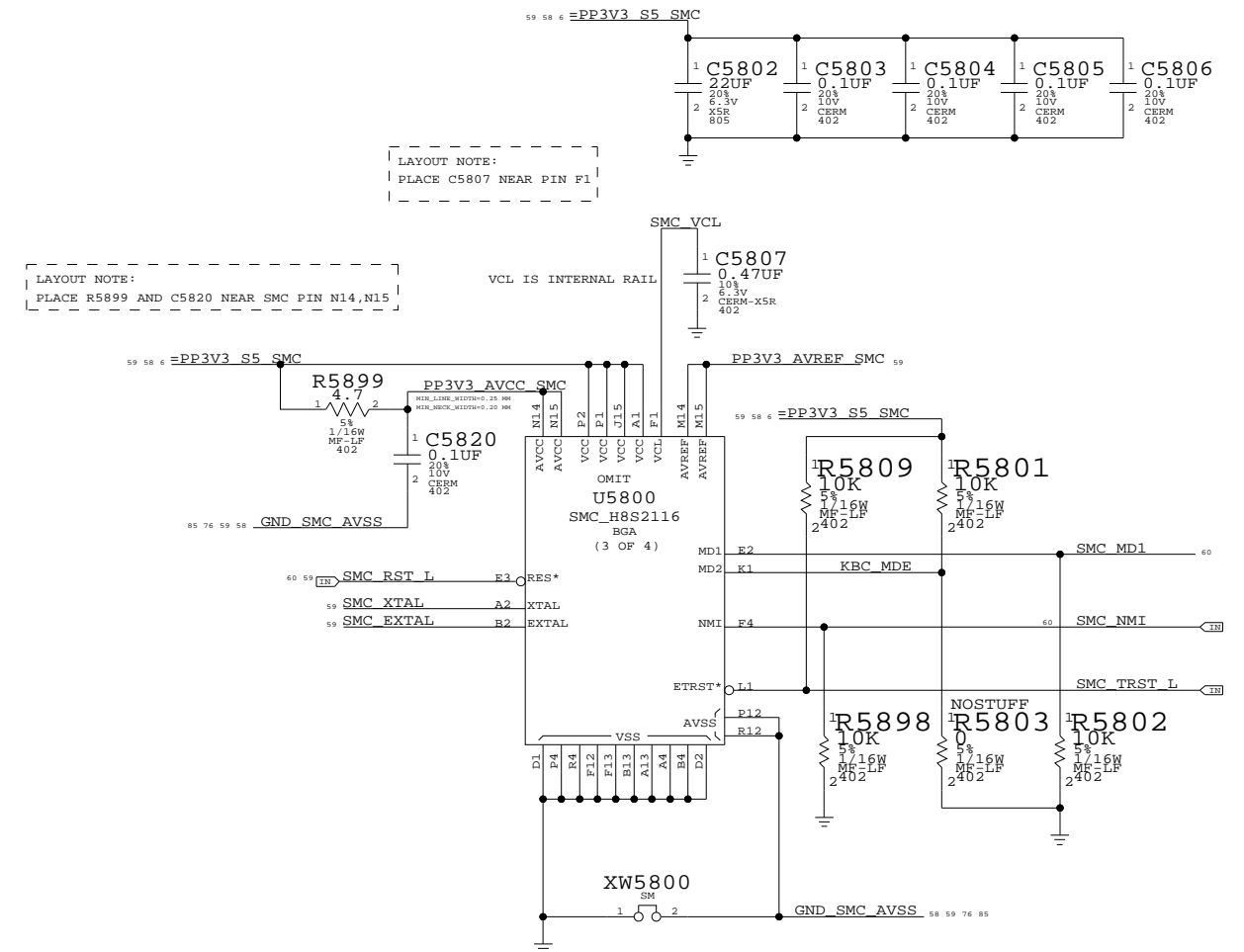
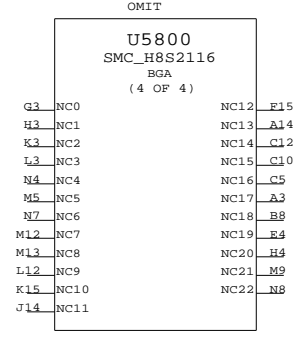
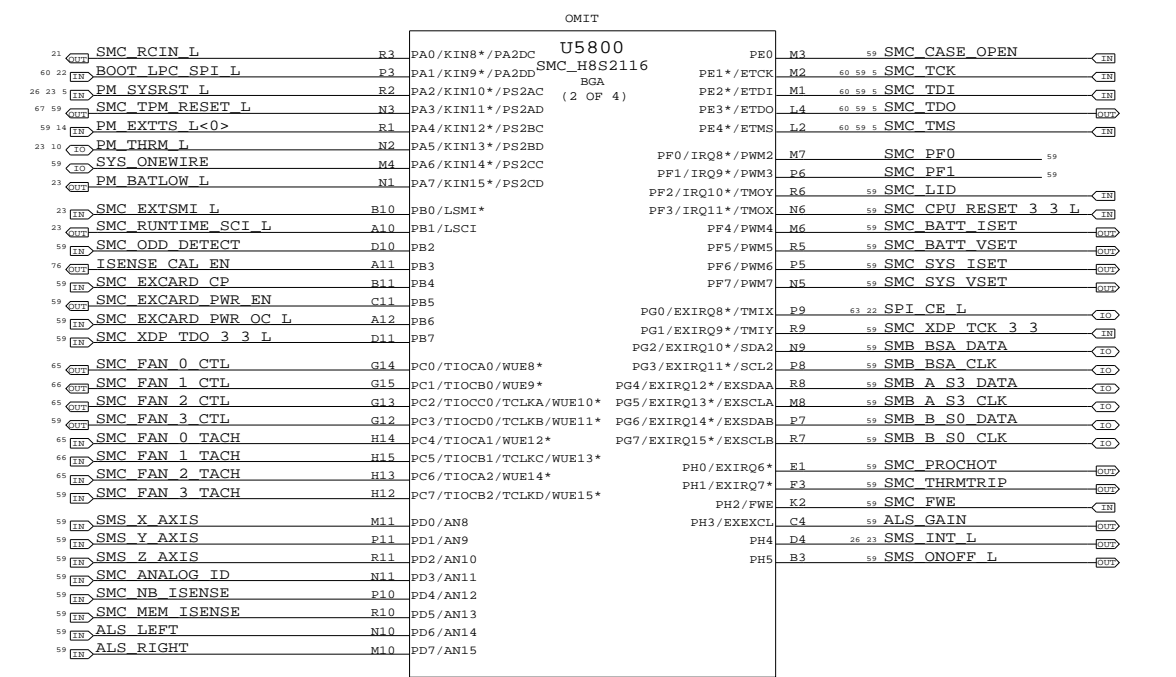
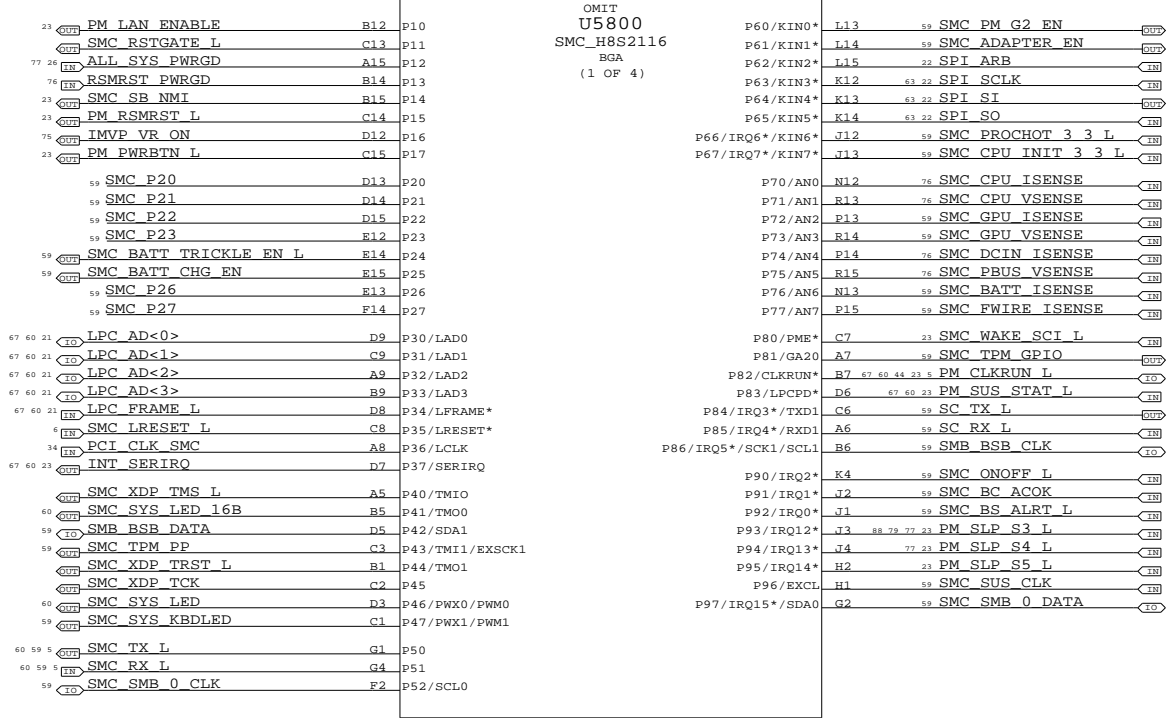
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	57 OF	111
NONE			

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



LAYOUT NOTE: PLACE C5807 NEAR PIN F1

LAYOUT NOTE: PLACE R5899 AND C5820 NEAR SMC PIN N14, N15

SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

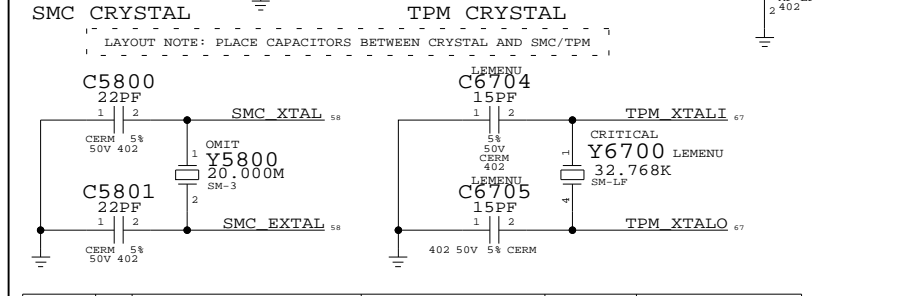
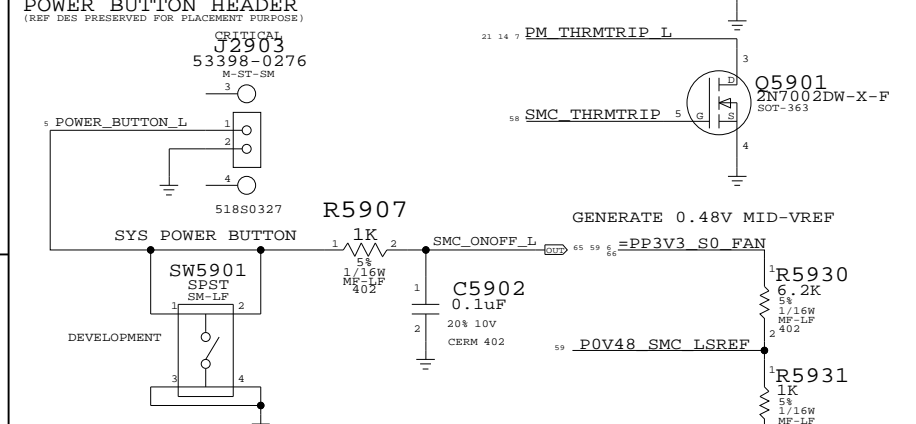
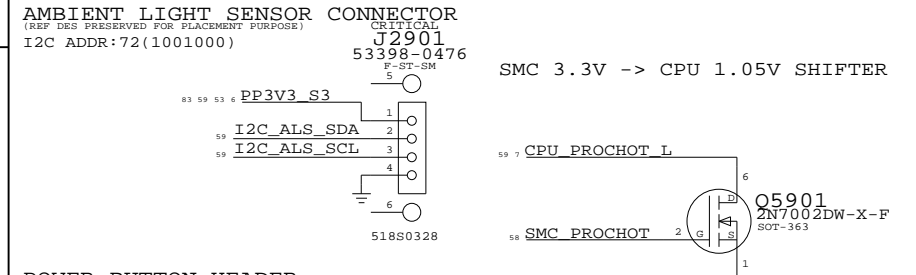
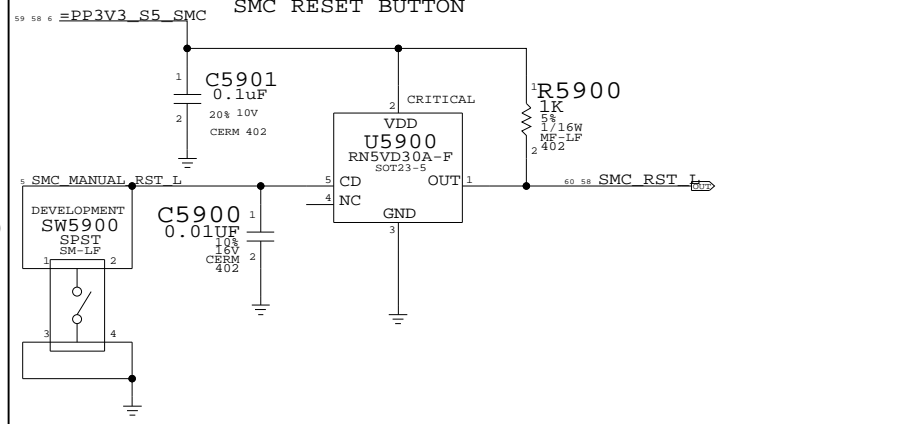
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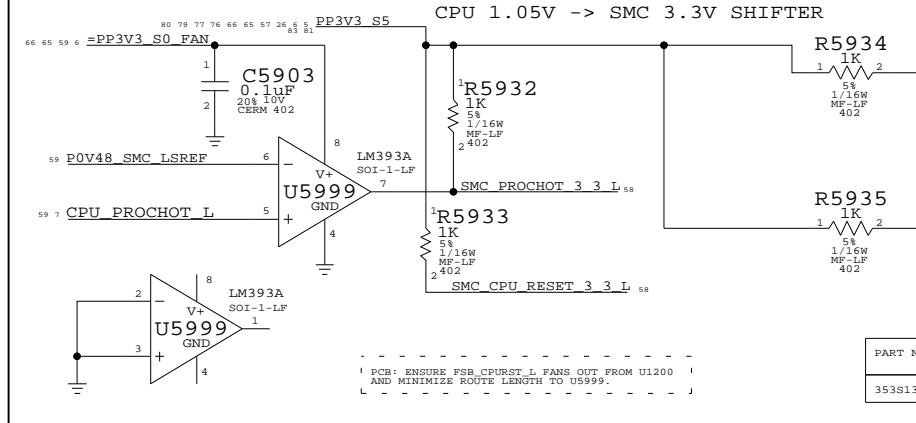
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	58 OF	111
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

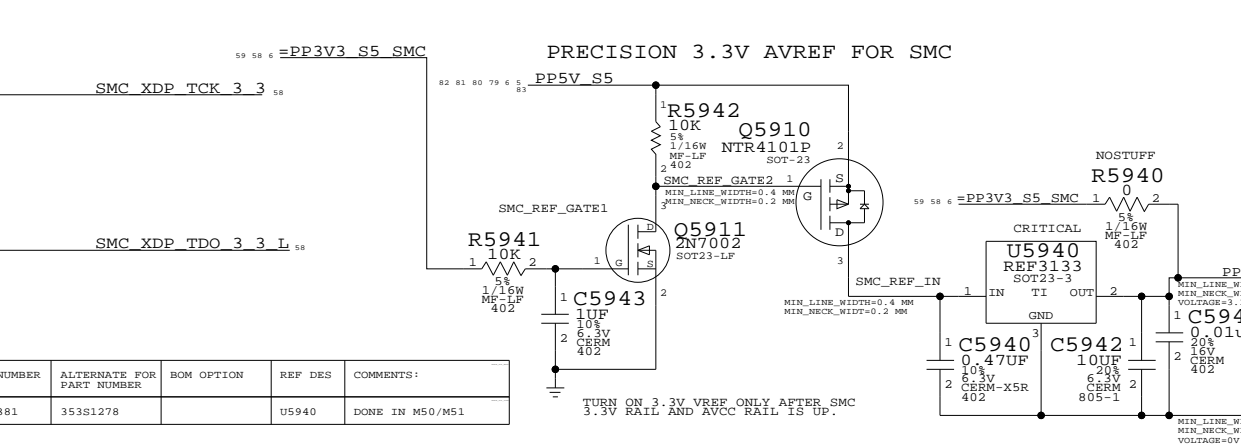
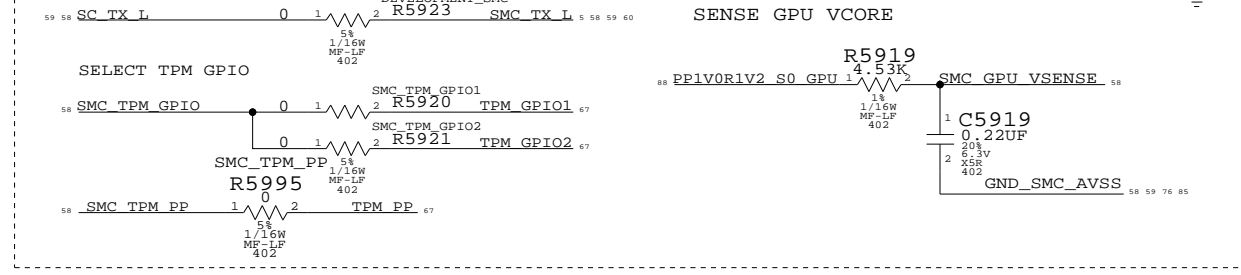
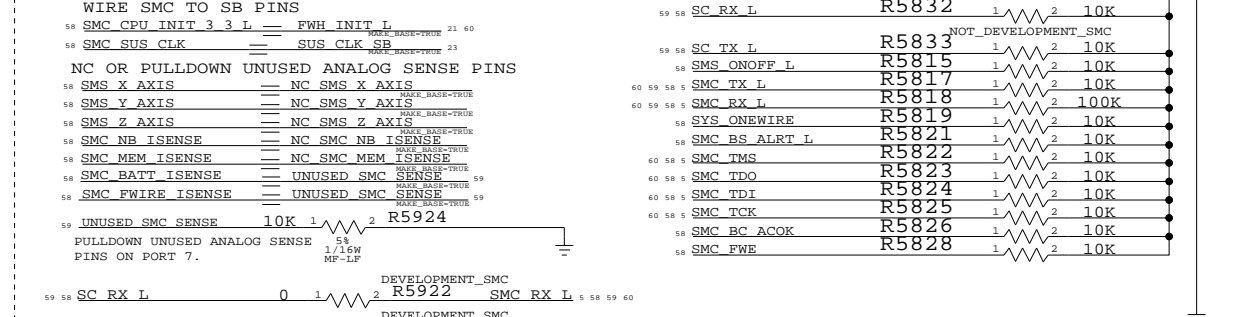


SMC ALIASES, PULLUPS, AND TESTPOINTS

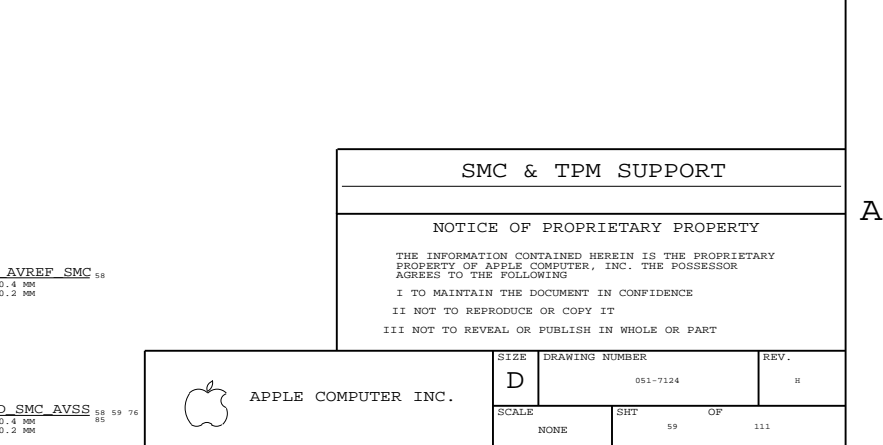
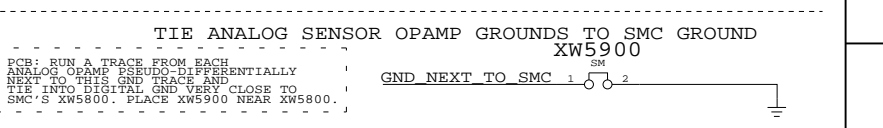
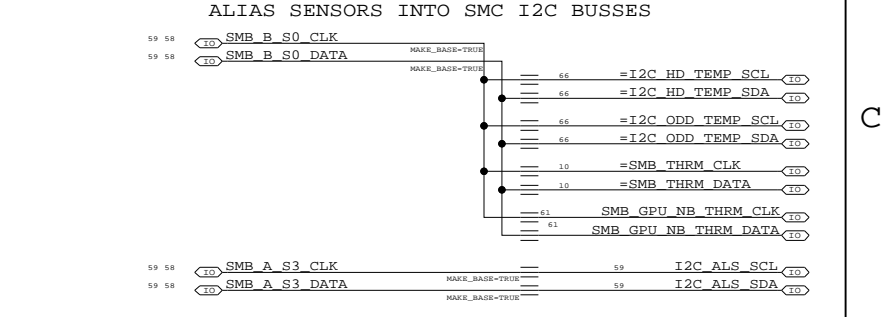
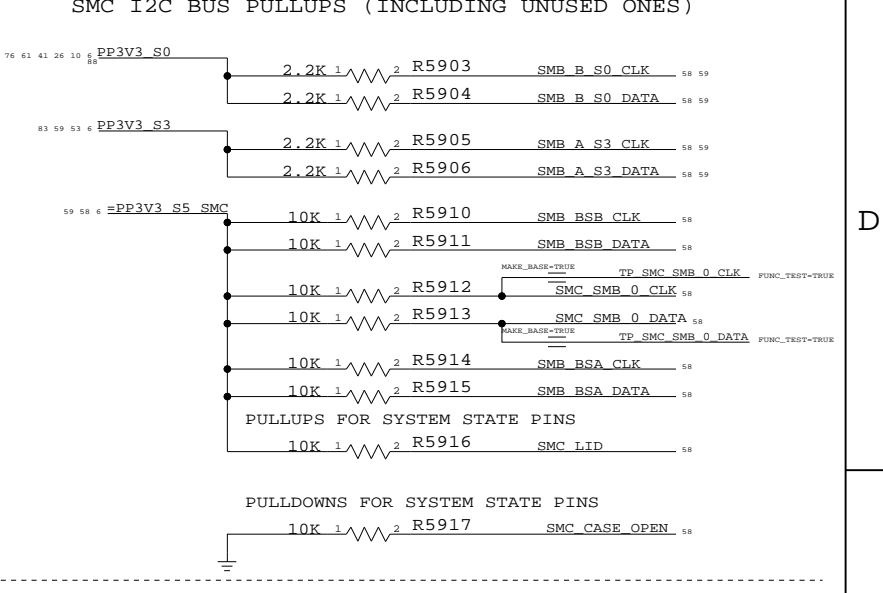
NO-CONNECT UNUSED PINS	SMC ALIASES	PULLUPS	TESTPOINTS
SMC P20	NC SMC P20		
SMC P21	NC SMC P21		
SMC P22	NC SMC P22		
SMC P23	NC SMC P23		
SMC P26	NC SMC P26		
SMC P27	NC SMC P27		
SMC BATT ISET	NC SMC BATT ISET		
SMC BATT VSET	NC SMC BATT VSET		
SMC SYS ISET	NC SMC SYS ISET		
SMC SYS VSET	NC SMC SYS VSET		
SMC BATT TRICKLE EN L	NC SMC BATT TRICKLE EN L		
SMC BATT CHG EN	NC SMC BATT CHG EN		
SMC ANALOG ID	NC SMC ANALOG ID		
ALS GAIN	NC ALS GAIN		

SMC PULL-UPS

SMC PIN	PULL-UP RESISTOR	VALUE
SMC ONOFF L	R5808	10K
SMC ODD DETECT	R5829	10K
SMC EXCARD CP	R5830	10K
SMC EXCARD PWR OC L	R5831	10K
SC RX L	R5832	10K
SC TX L	R5833	10K
SMS ONOFF L	R5815	10K
SMC TX L	R5817	10K
SMC RX L	R5818	100K
SYS ONEWIRE	R5819	10K
SMC BS ALERT L	R5821	10K
SMC TMS	R5822	10K
SMC TDO	R5823	10K
SMC TDI	R5824	10K
SMC TCK	R5825	10K
SMC BC ACOK	R5826	10K
SMC FWE	R5828	10K



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S1381	353S1278		U5940	DONE IN M50/M51



SMC & TPM SUPPORT

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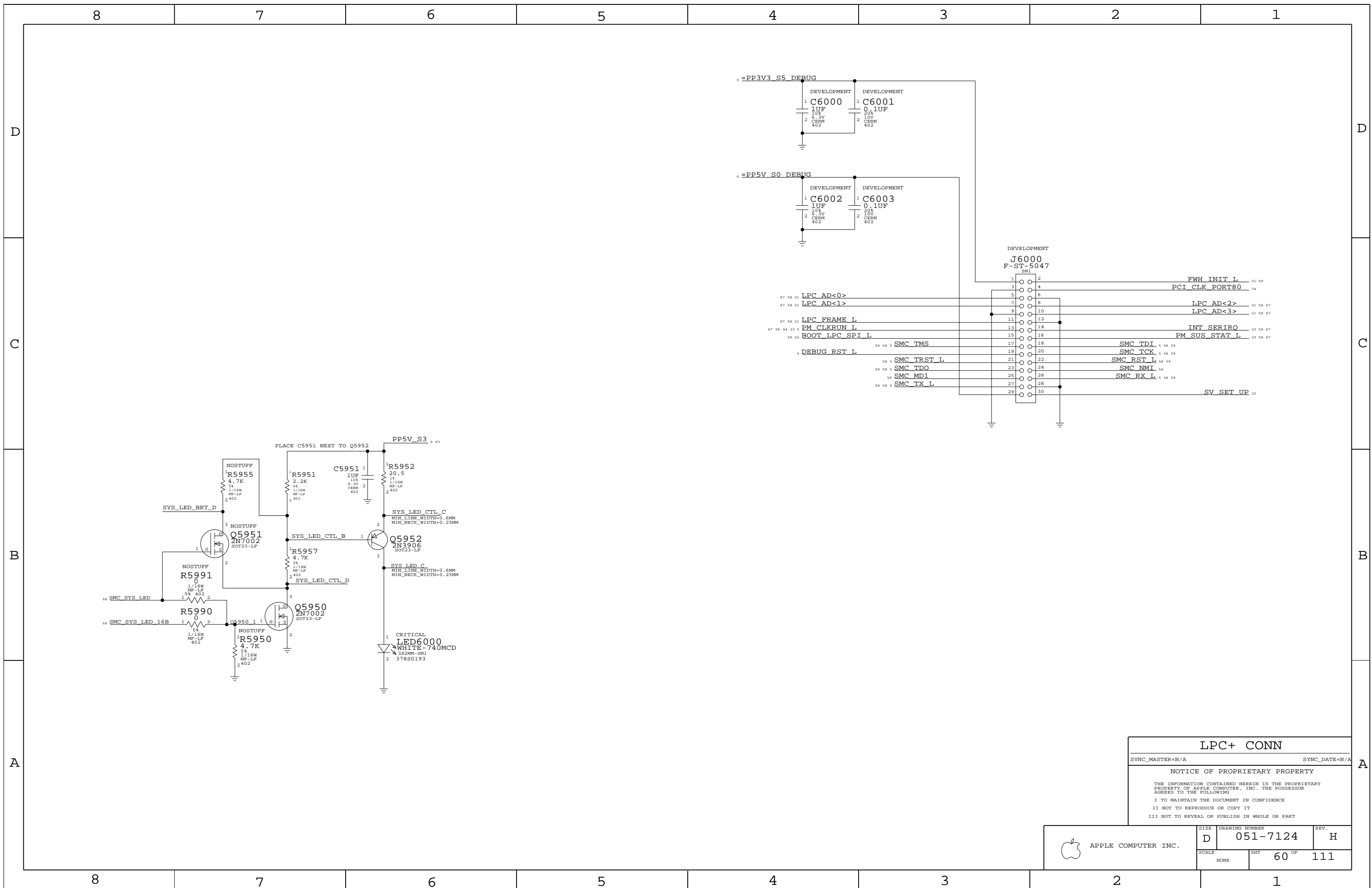
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SIZE	DRAWING NUMBER	REV.
D	051-7124	II

SCALE: NONE SHEET: 59 OF 111

APPLE COMPUTER INC.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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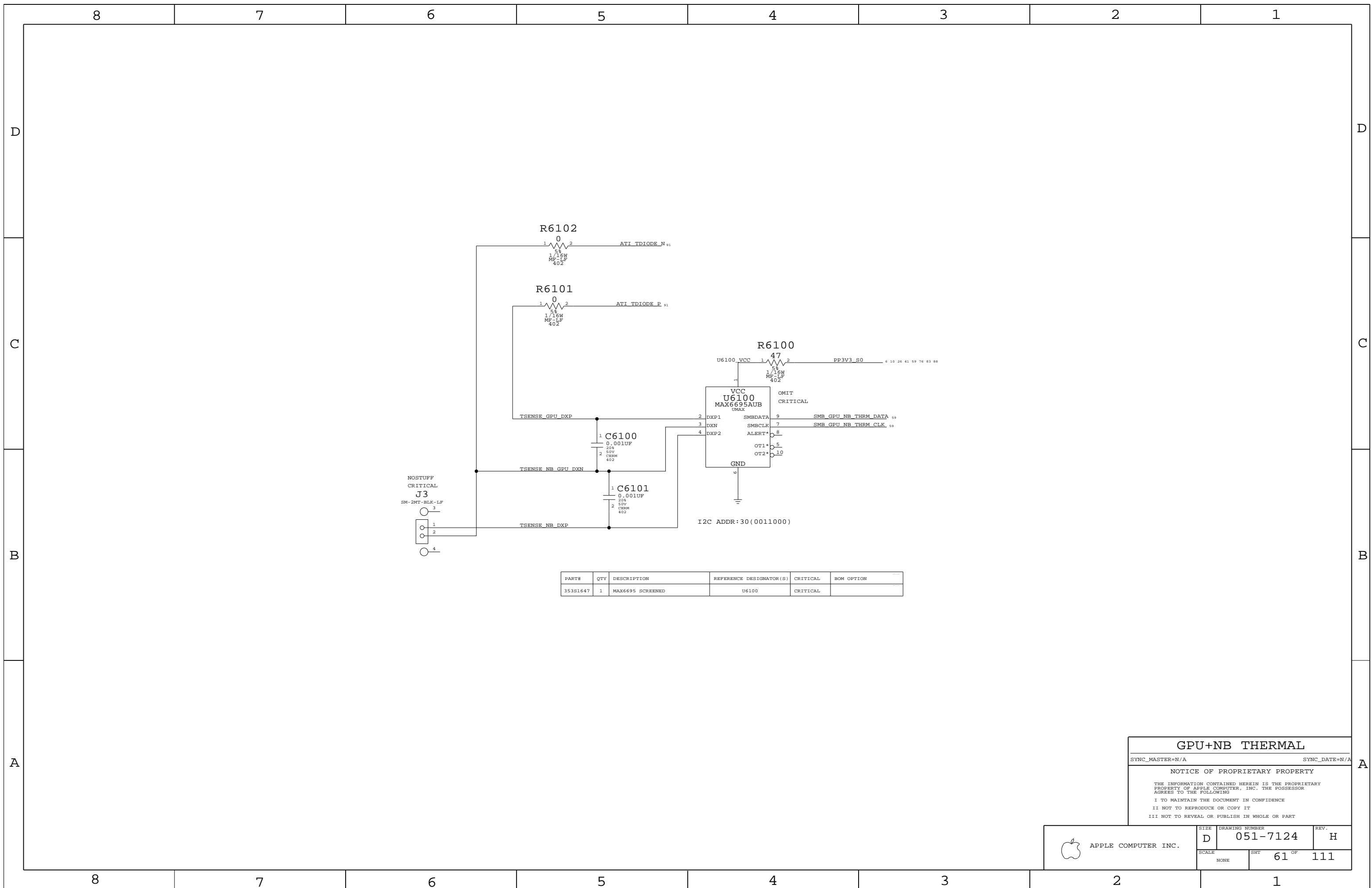
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 60 OF 111	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35381647	1	MAX6695 SCREENED	U6100	CRITICAL	

GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

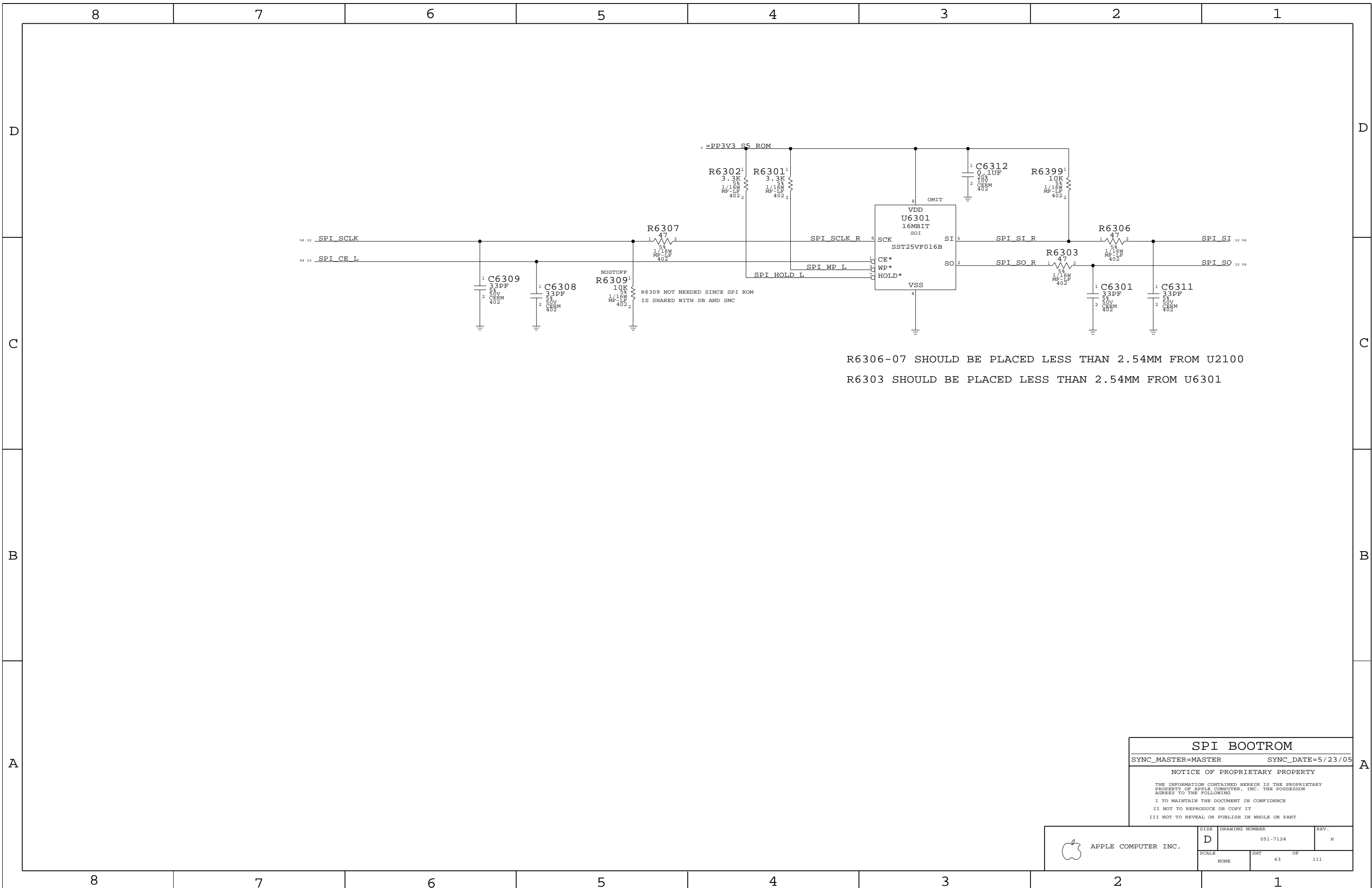
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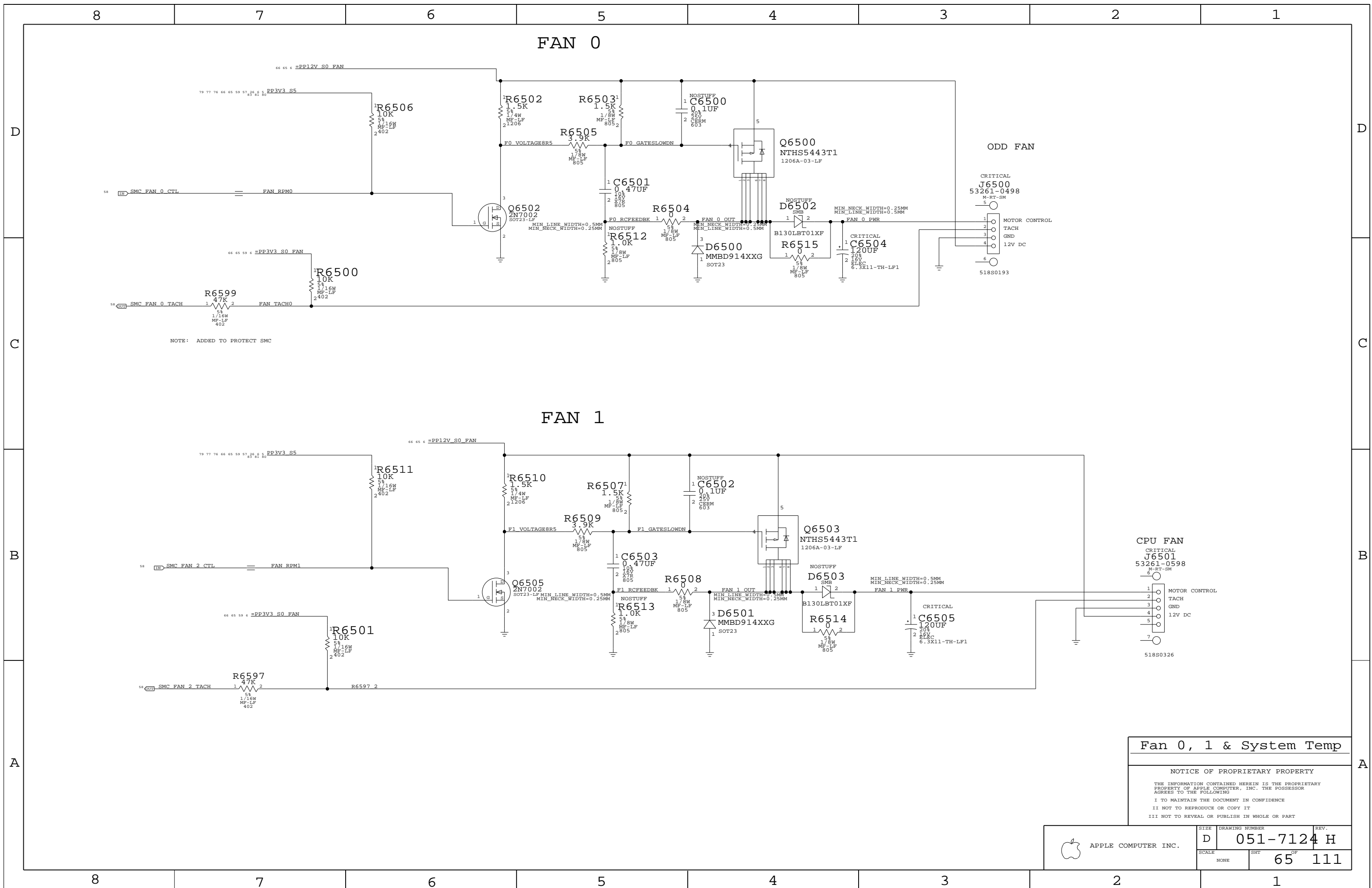
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	61	111	



SPI BOOTROM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 63	OF 111



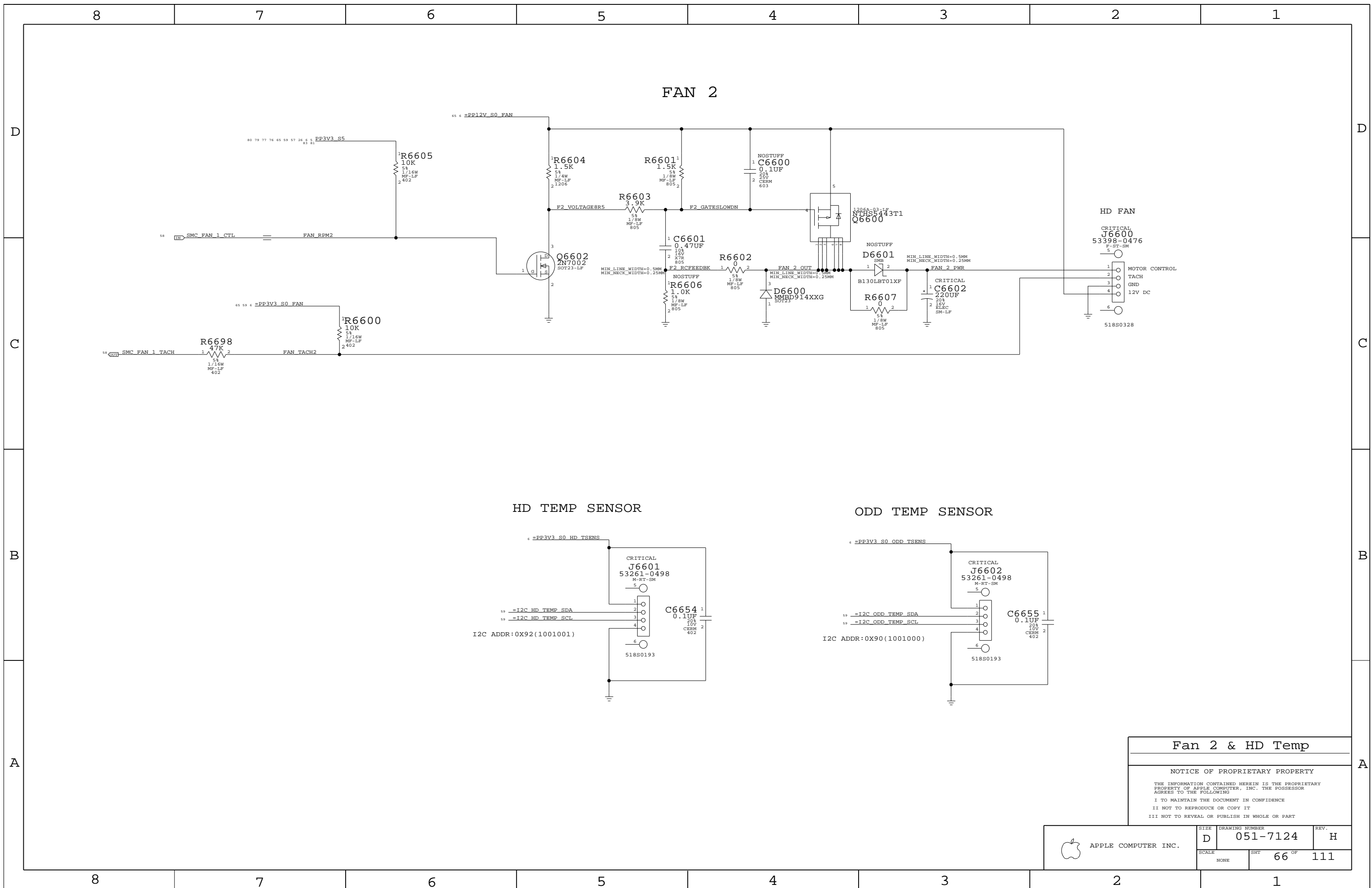
NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-7124 H	
	SCALE	SHT	OF
		65	111



FAN 2

HD TEMP SENSOR

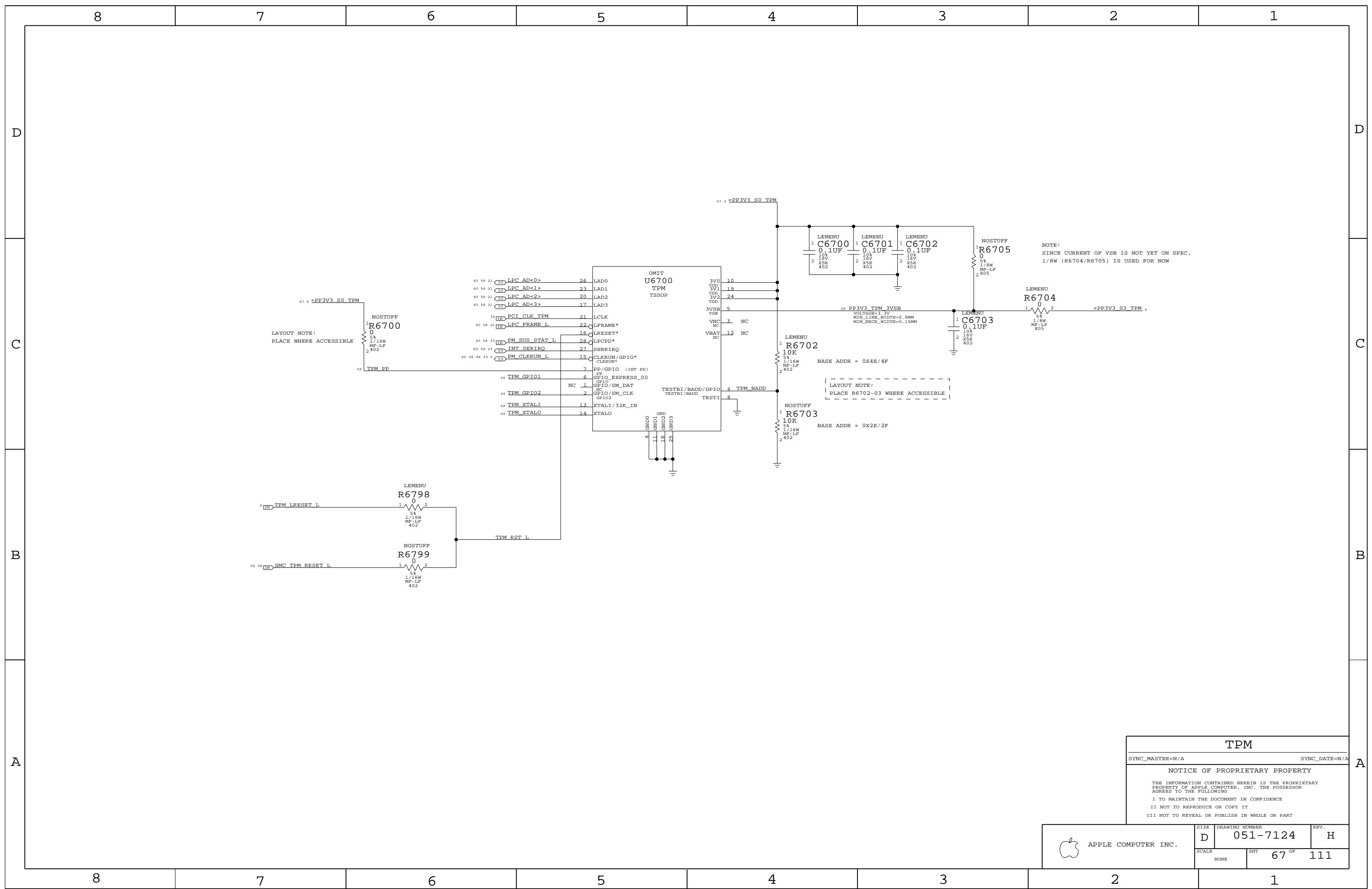
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	REV.
NONE	66	111	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW


TPM

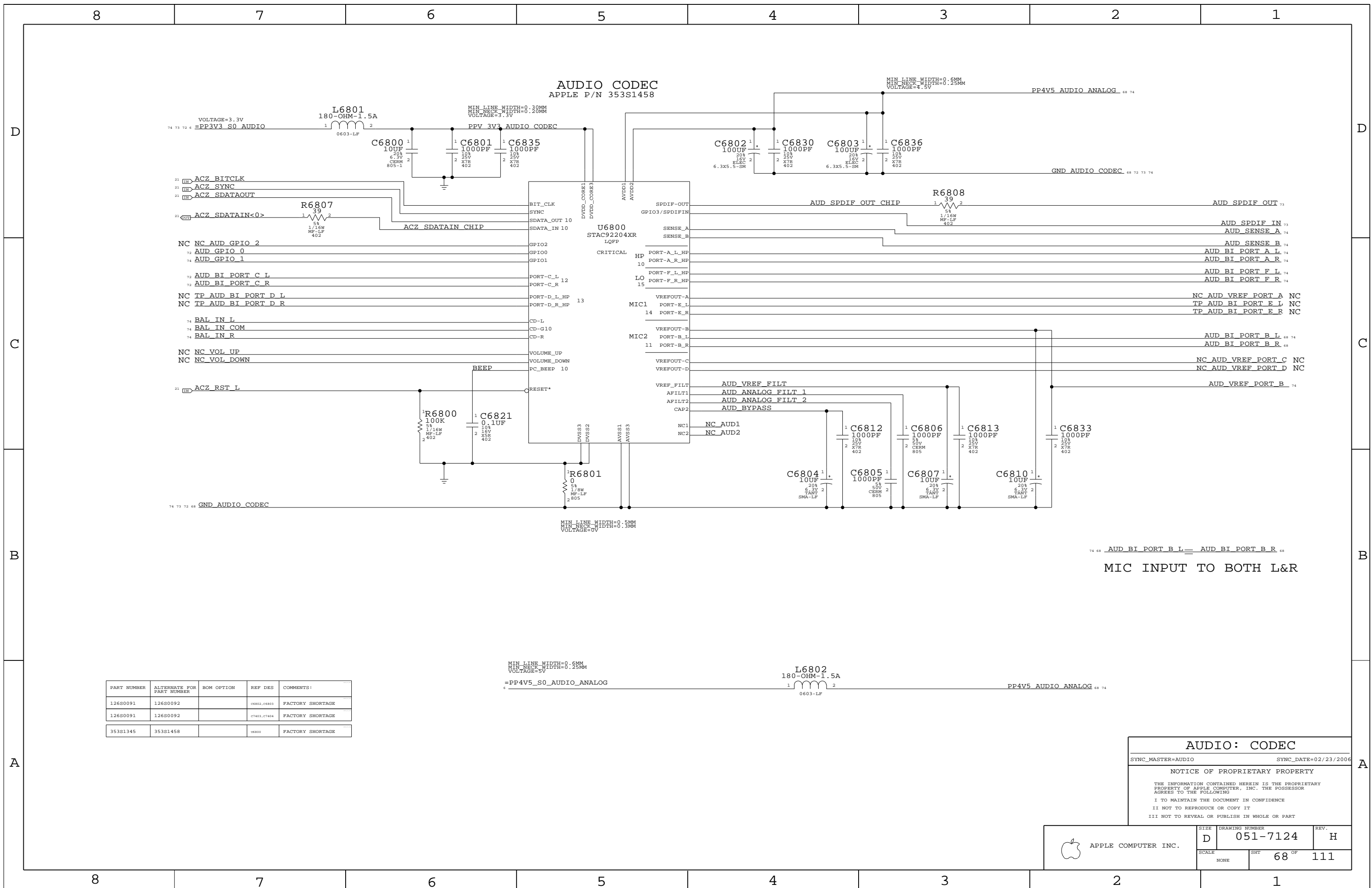
SYNC_MASTER=N/A SYNC_DATE=N/A

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	67 OF 111	
NONE			



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C802,C803	FACTORY SHORTAGE
126S0091	126S0092		C7403,C7404	FACTORY SHORTAGE
353S1345	353S1458		U6800	FACTORY SHORTAGE

AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

NOTICE OF PROPRIETARY PROPERTY

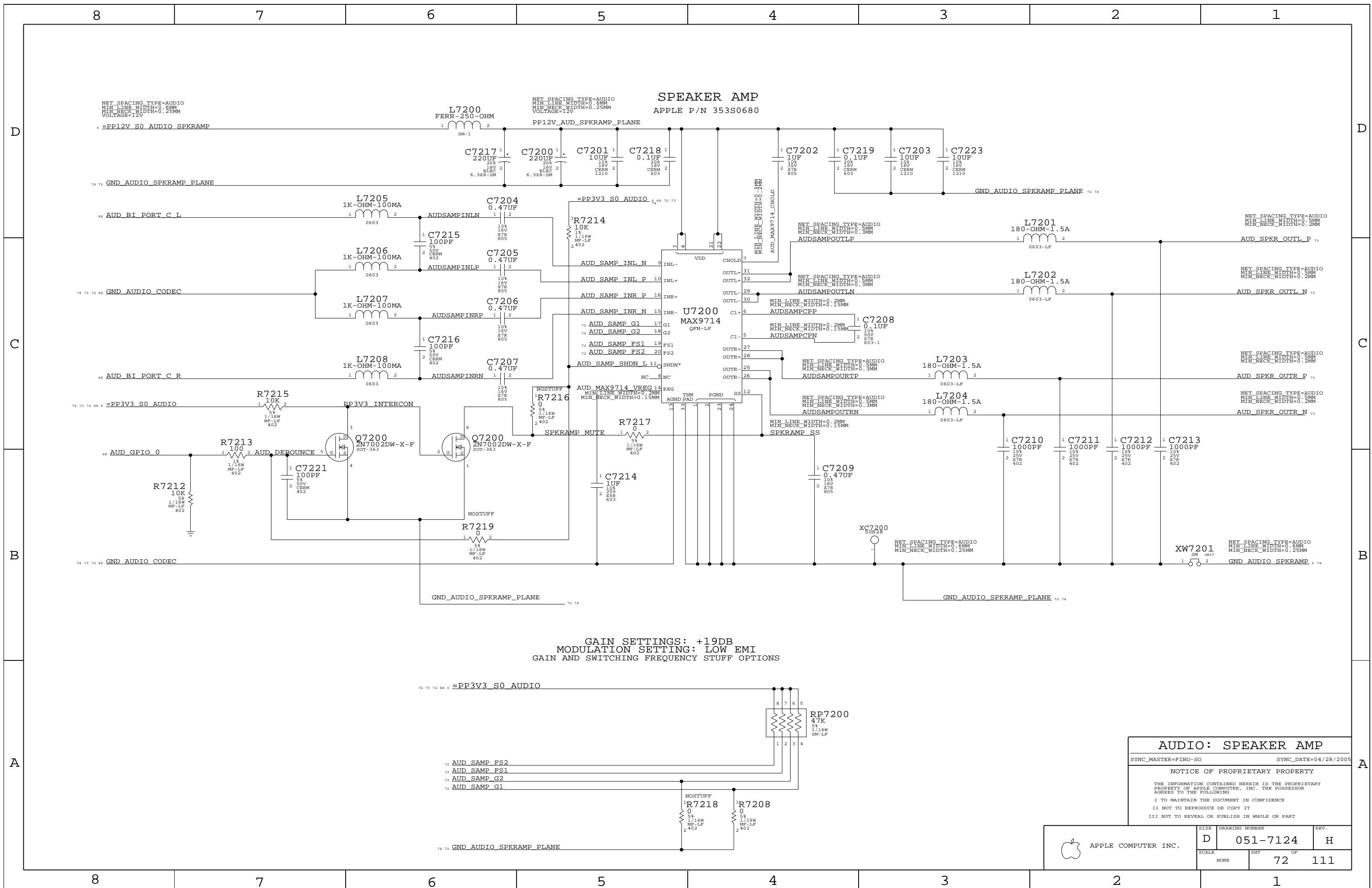
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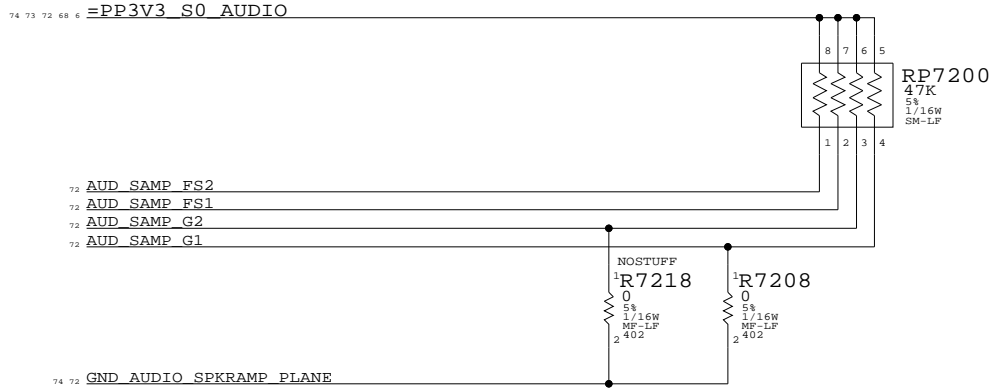
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	68 OF	111
NONE			



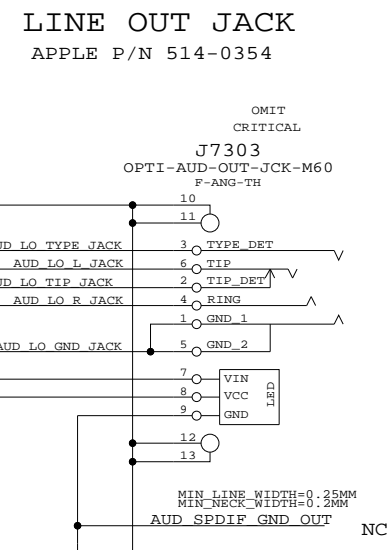
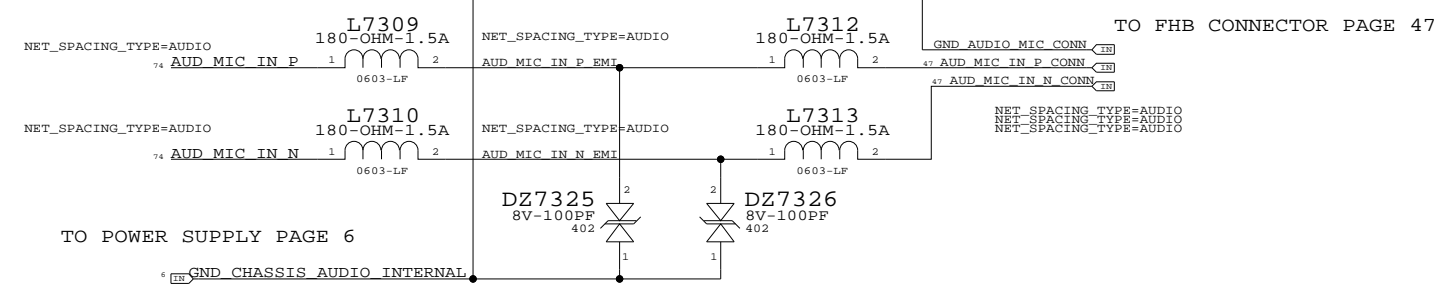
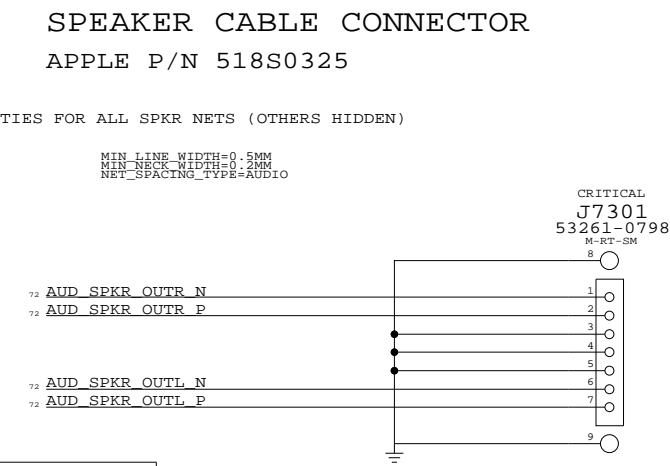
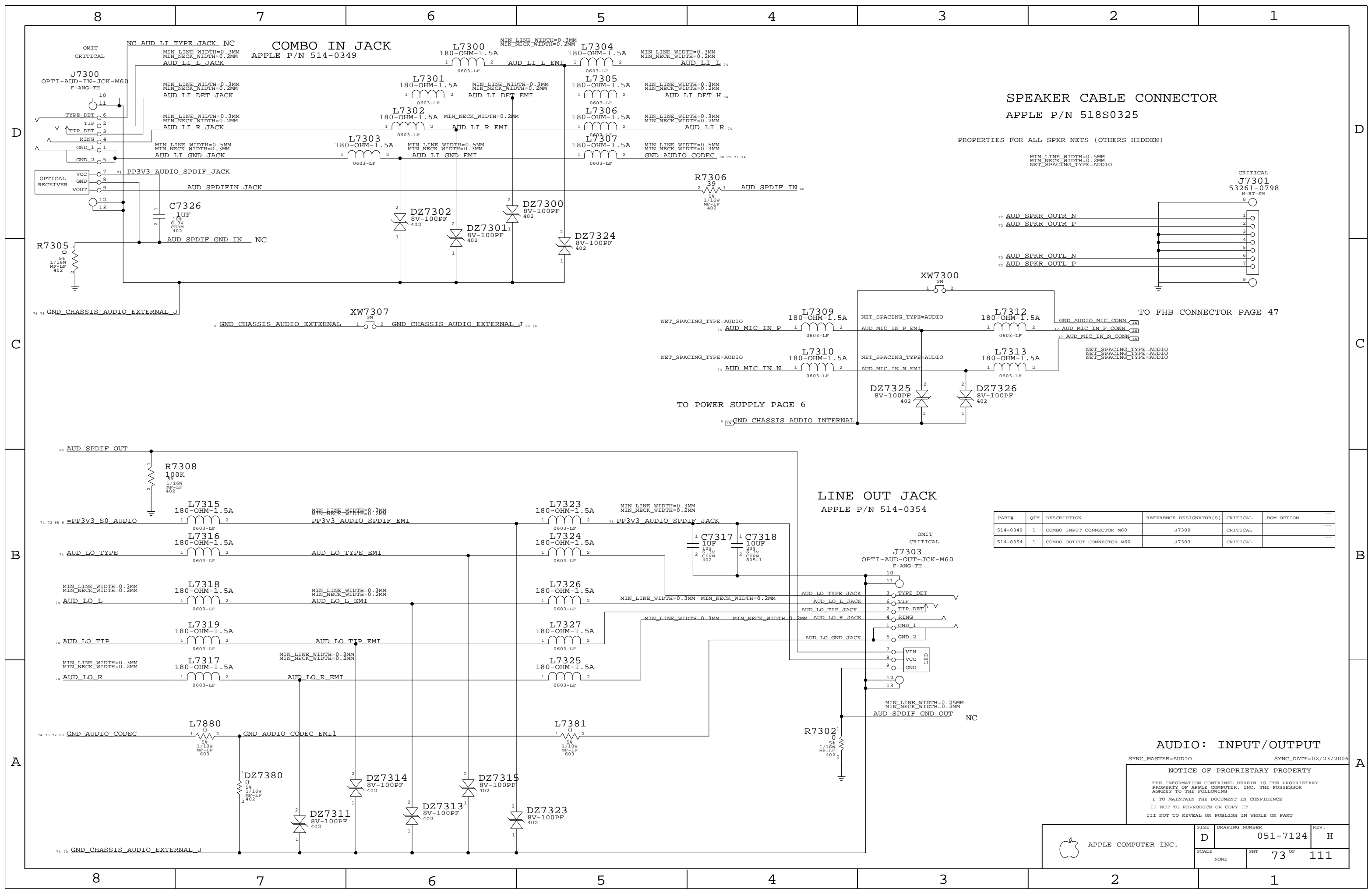
SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP
 SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	NONE	SHT OF	72 OF 111



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0349	1	COMBO INPUT CONNECTOR M60	J7300	CRITICAL	
514-0354	1	COMBO OUTPUT CONNECTOR M60	J7303	CRITICAL	

AUDIO: INPUT/OUTPUT

SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006

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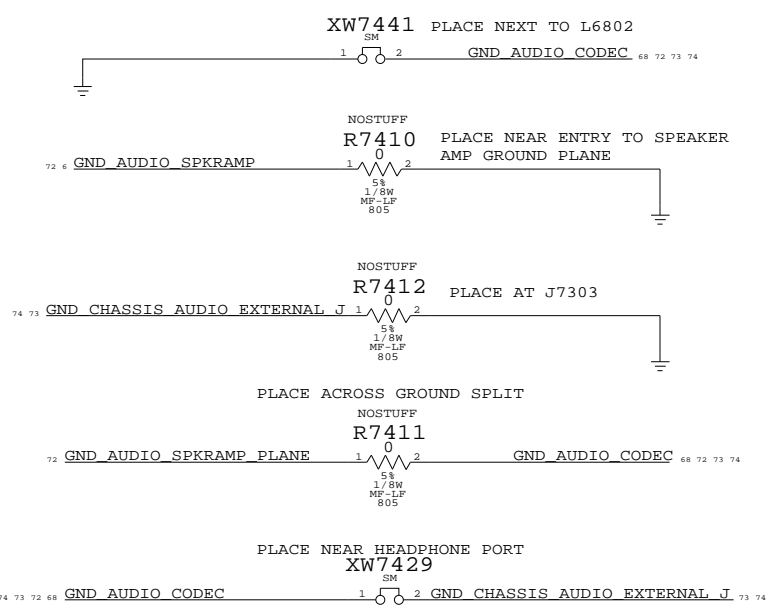
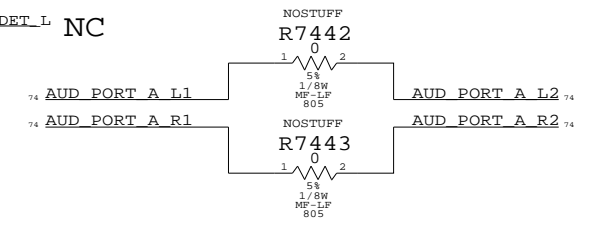
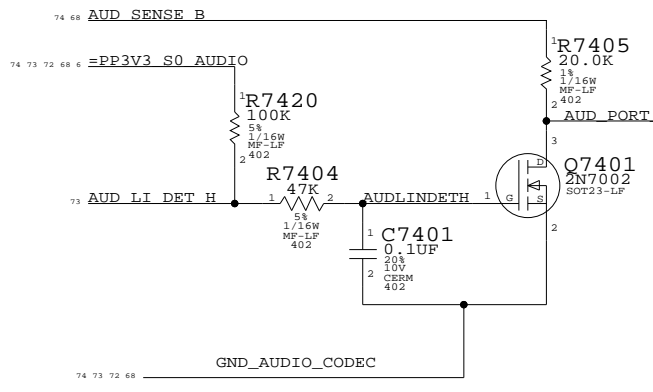
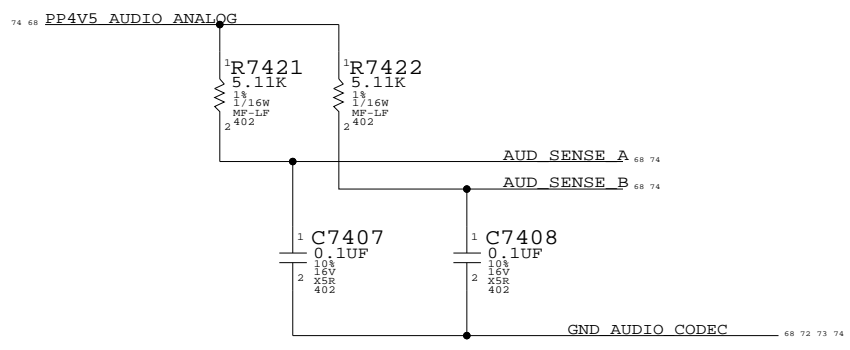
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	73 OF	111
NONE			

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

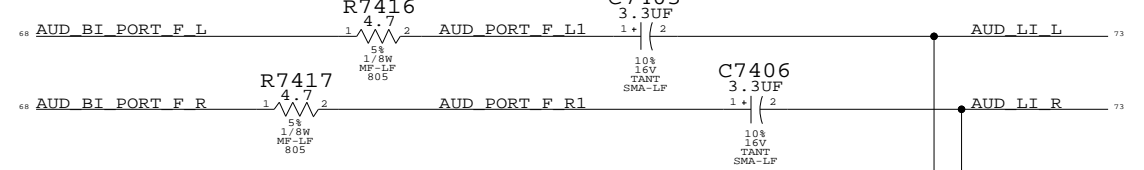
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



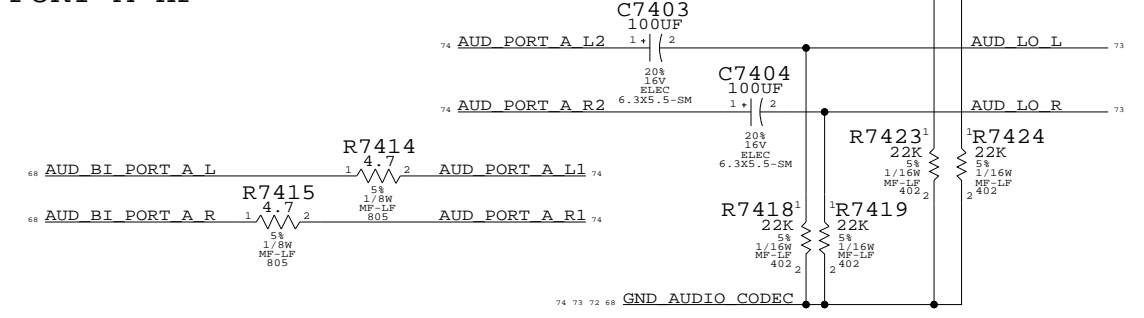
USED PORTS
 PORT A HP
 PORT B MIC IN VREF =80%
 PORT C BI SPEAKERS
 PORT F LI

UNUSED PORTS
 PORT E DETECT DELEGATE
 PORT D

PORT F LI



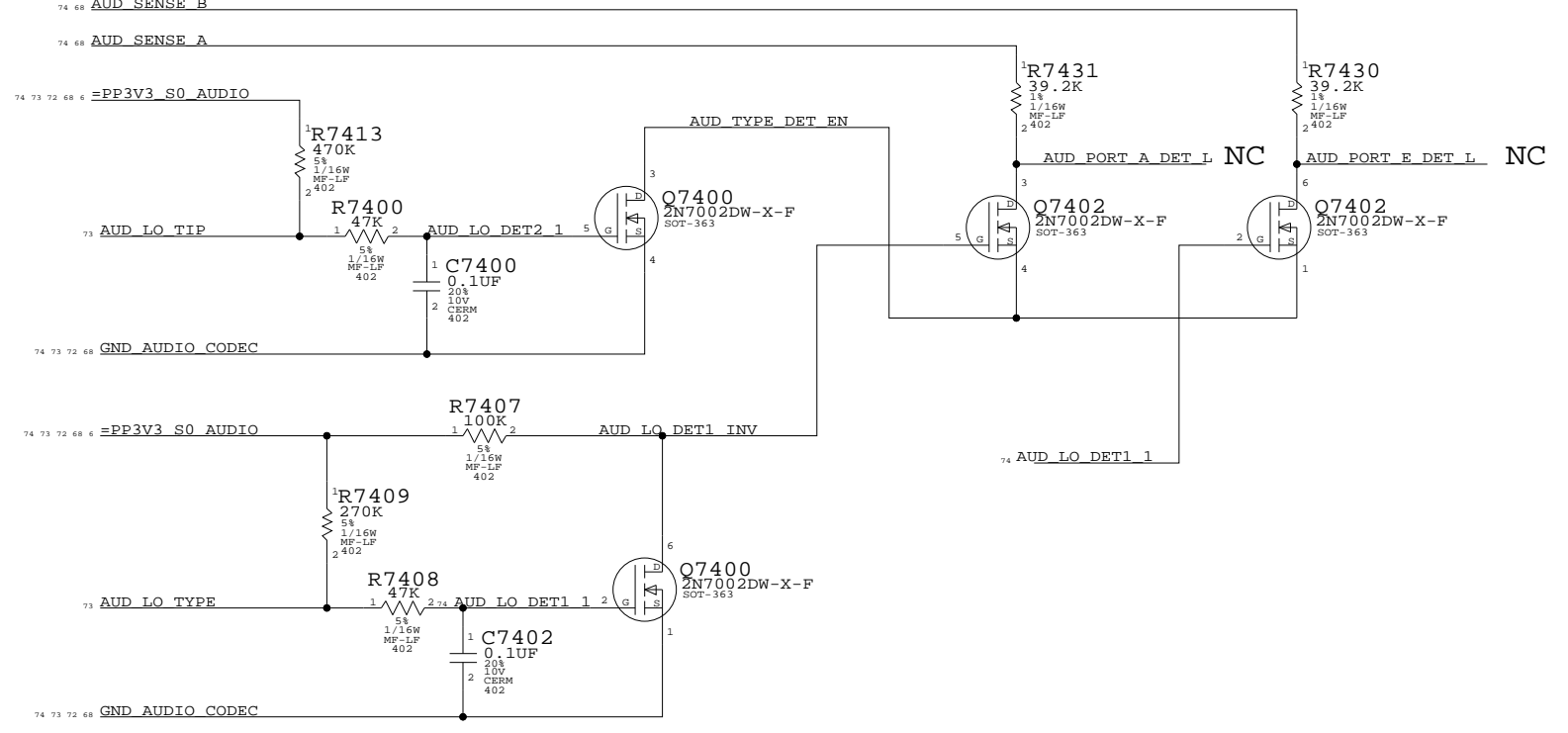
PORT A HP



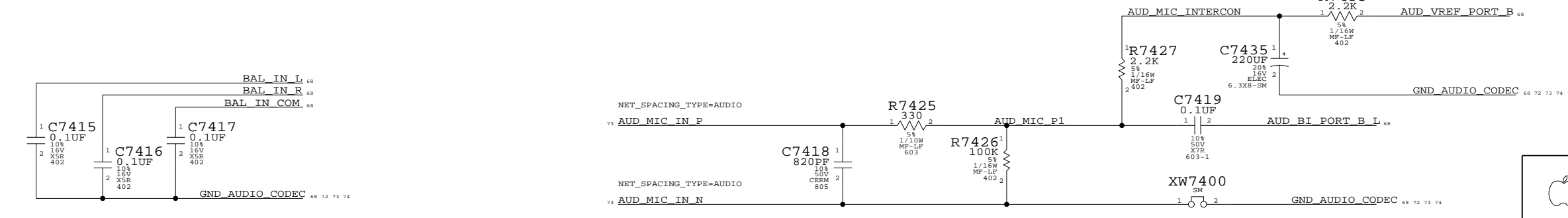
UNUSED PORT TERMINATION



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

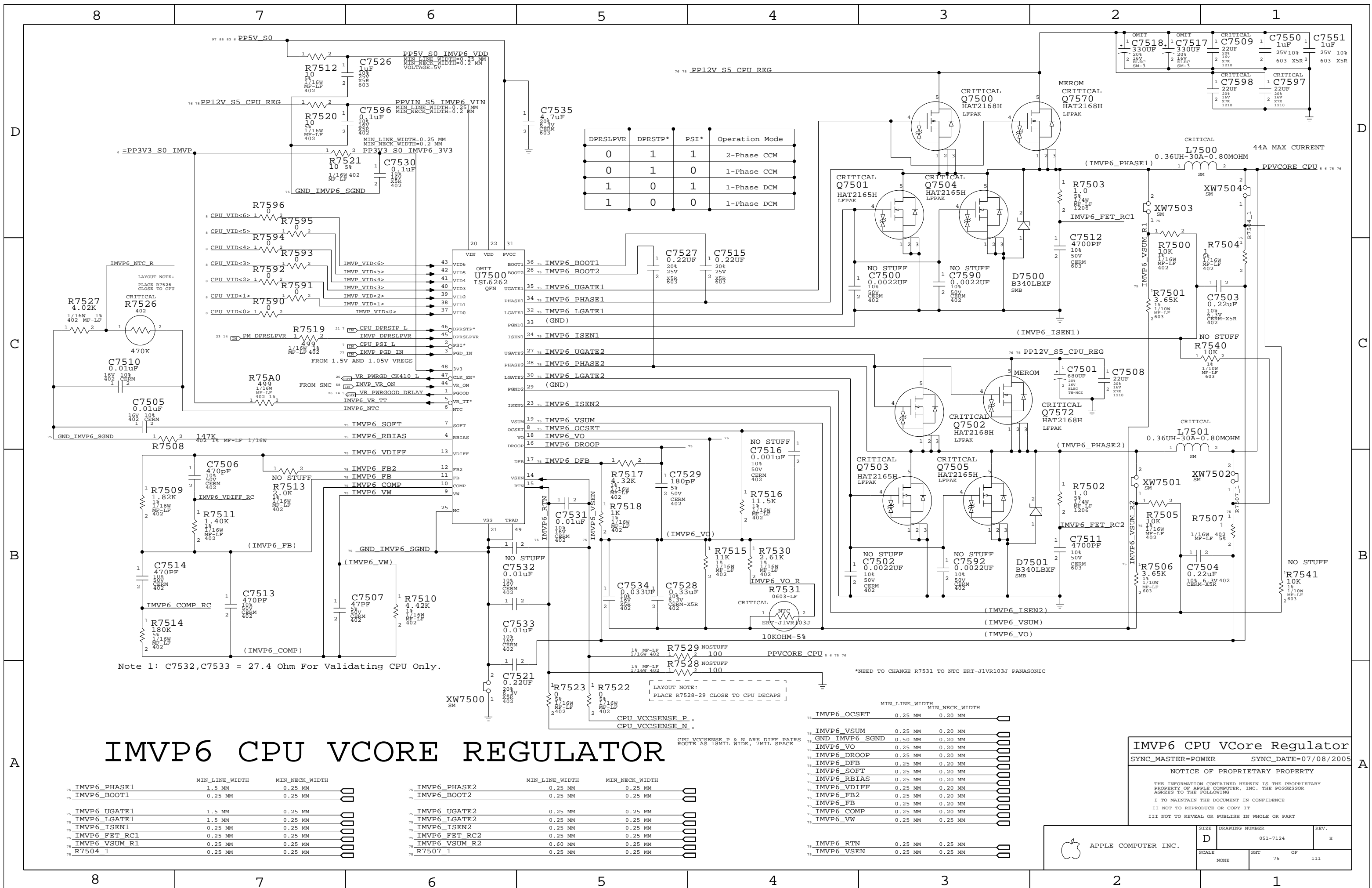


MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: JACK DETECT
 SYNC_MASTER=AUDIO SYNC_DATE=02/23/2006
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	D	051-7124	H
SCALE	SHT	74 OF	111
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Signal	Value
C7527	0.22uF
C7515	0.22uF
C7516	0.001uF
C7517	4.32K
C7529	180pF
C7518	330uF
C7519	22uF
C7520	0.1uF
C7521	0.22uF
C7522	0.22uF
C7523	0.033uF
C7524	0.33uF
C7525	0.01uF
C7526	1uF
C7527	0.22uF
C7528	0.33uF
C7529	180pF
C7530	0.1uF
C7531	0.01uF
C7532	0.01uF
C7533	0.01uF
C7534	0.033uF
C7535	4.7uF

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

LAYOUT NOTE:
PLACE R7528-29 CLOSE TO CPU DECAPS

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

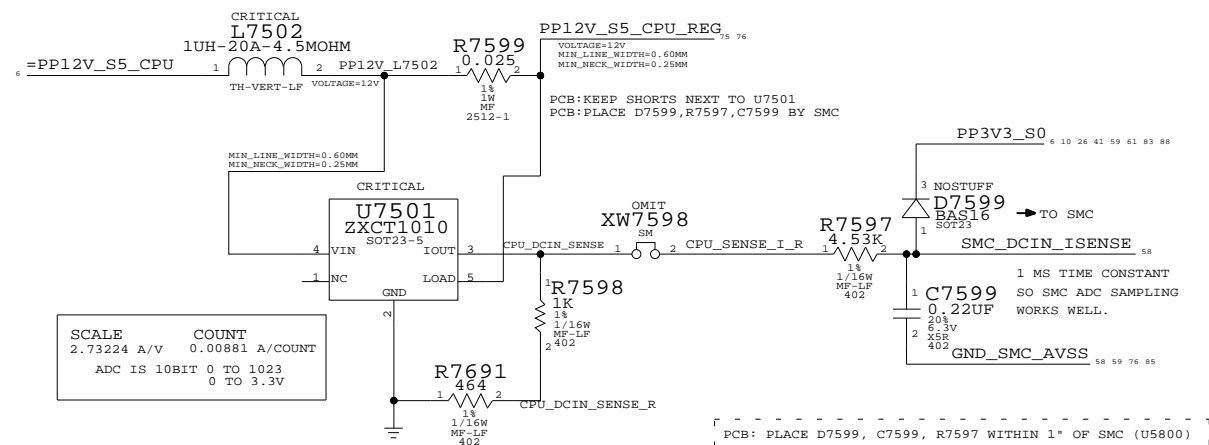
Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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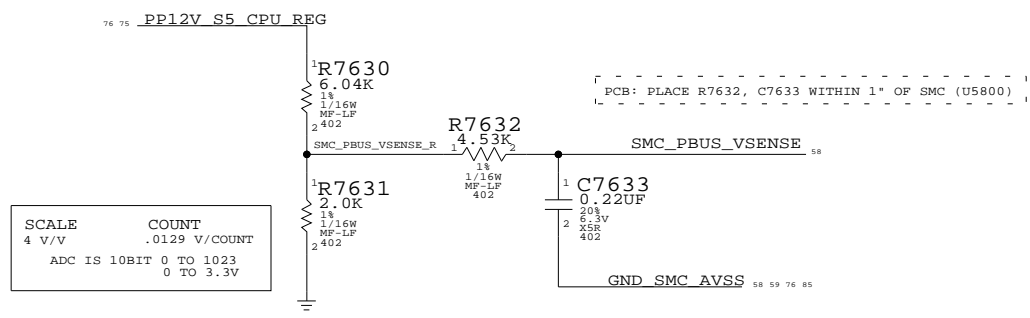
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHEET	OF	111
NONE	75		

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



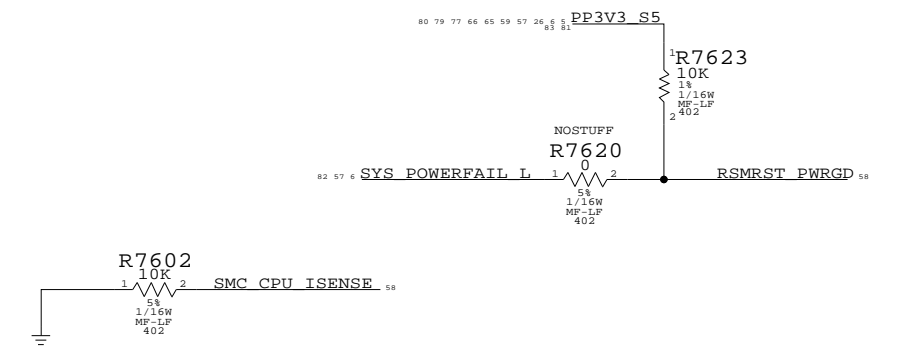
SCALE	COUNT
2.73224 A/V	0.00881 A/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

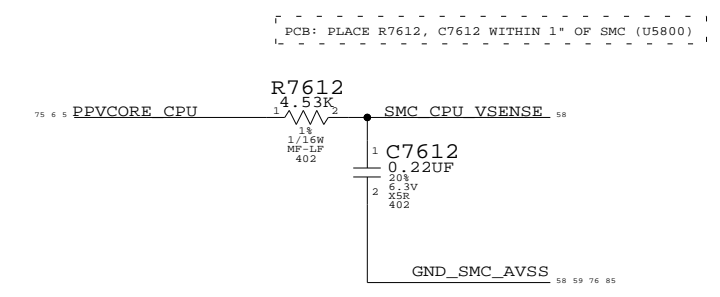


SCALE	COUNT
4 V/V	.0129 V/COUNT
ADC IS 10BIT 0 TO 1023	
0 TO 3.3V	

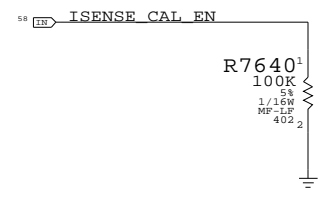
SMC PWRGD PULLUP



PROCESSOR VCORE SENSE

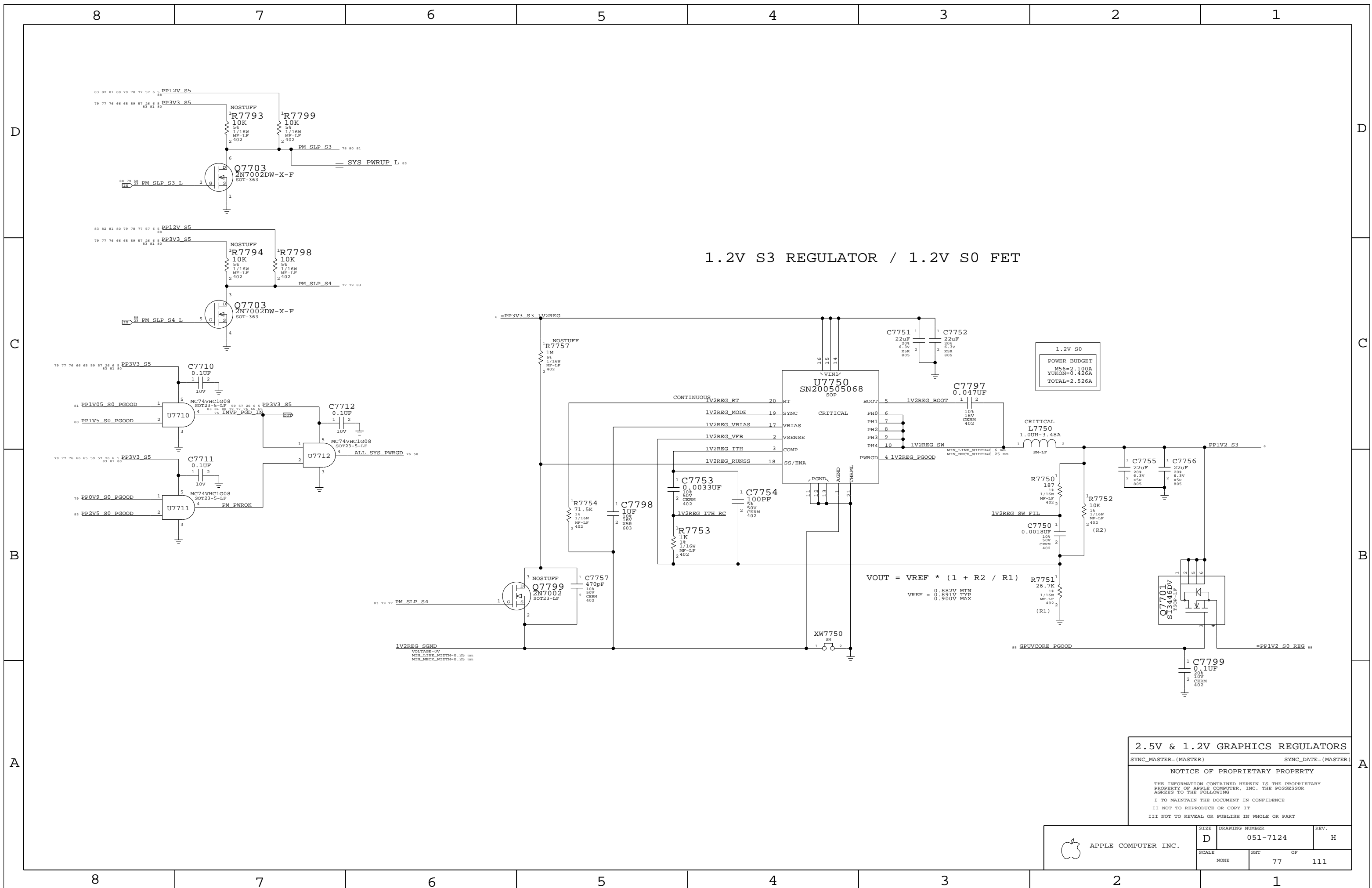


Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	76 OF	111
NONE			



1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S0
POWER BUDGET
M56=2.100A
YUKON=0.426A
TOTAL=2.526A

$$V_{OUT} = V_{REF} * (1 + R2 / R1)$$

VREF = 0.82V MIN
0.831V TYP
0.900V MAX

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	77	111	

D

D

C

C

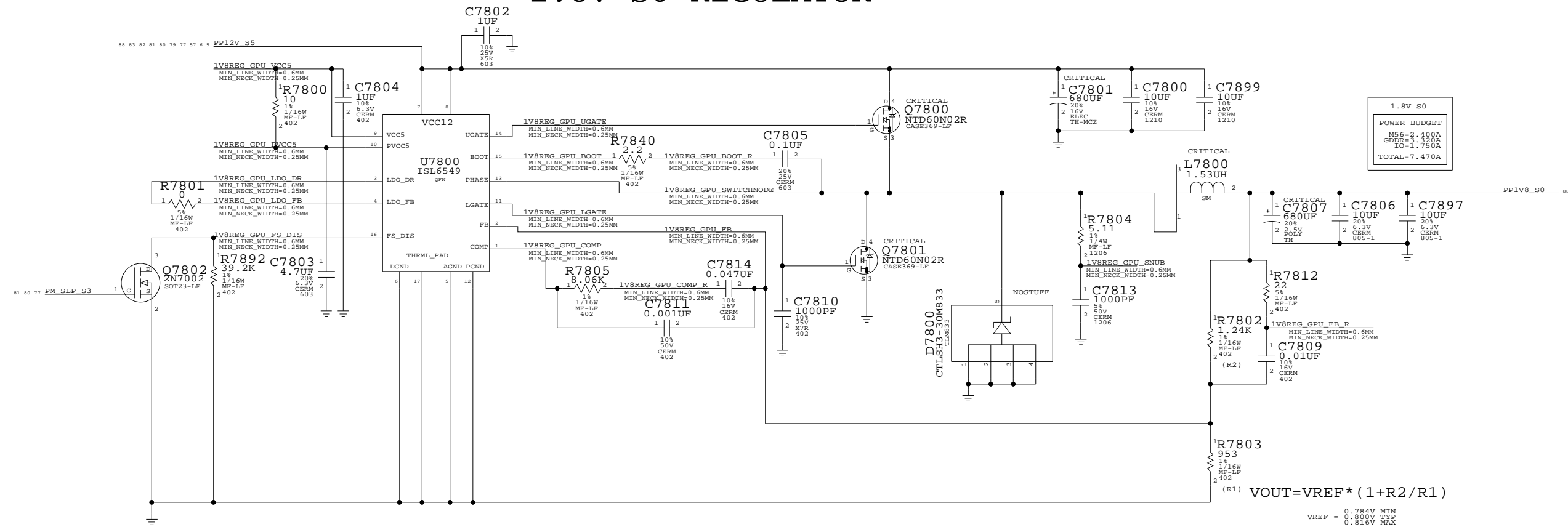
B

B

A

A

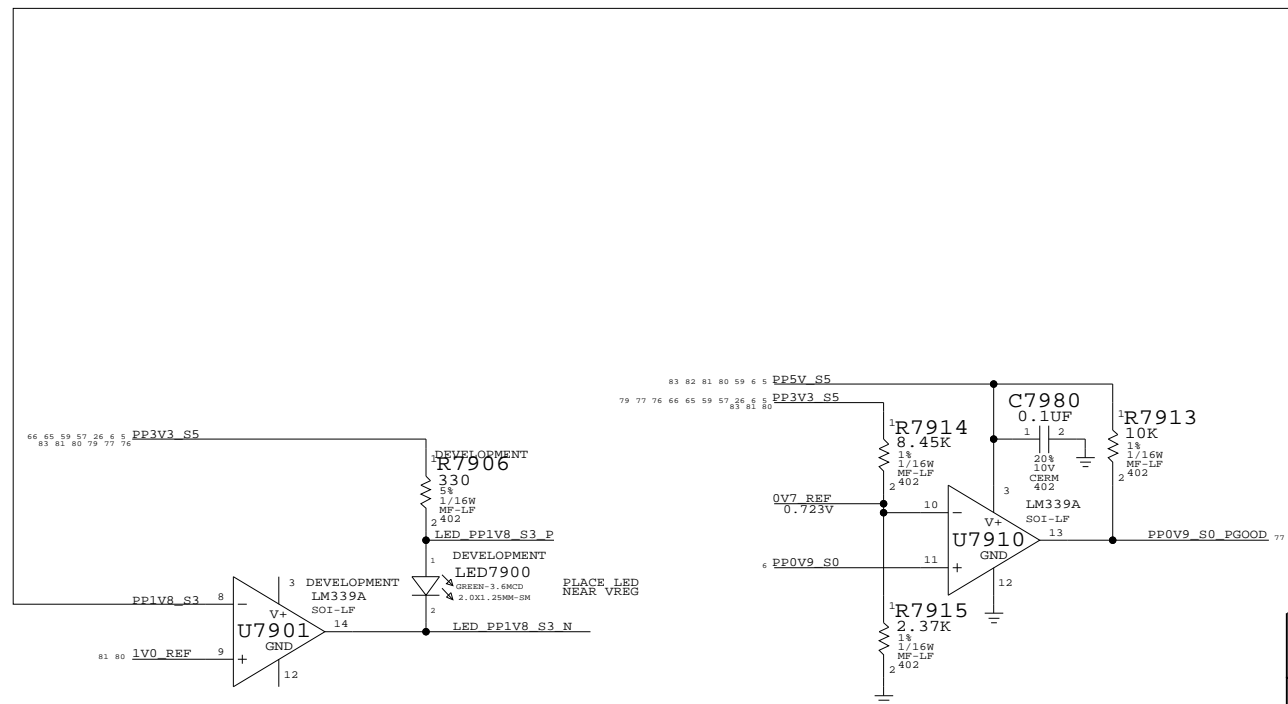
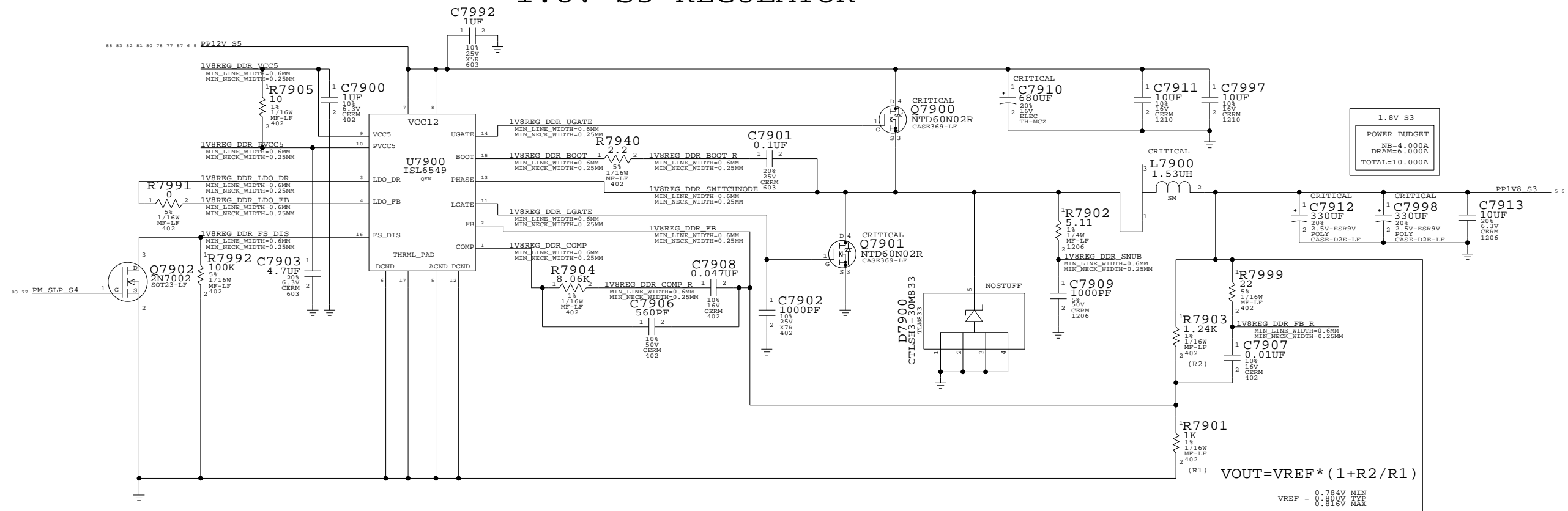
1.8V S0 REGULATOR



1.8V GDDR REGULATOR
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7124	H
SCALE	SHT	78 OF	111
NONE			

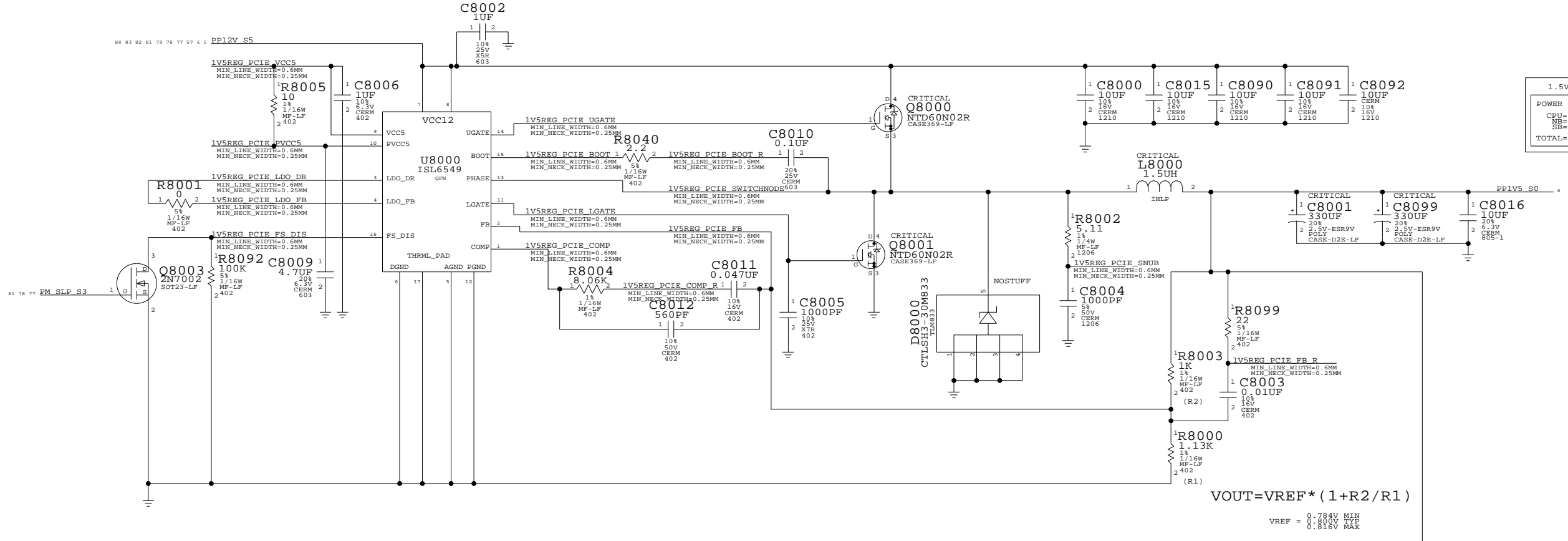
1.8V S3 REGULATOR



1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005
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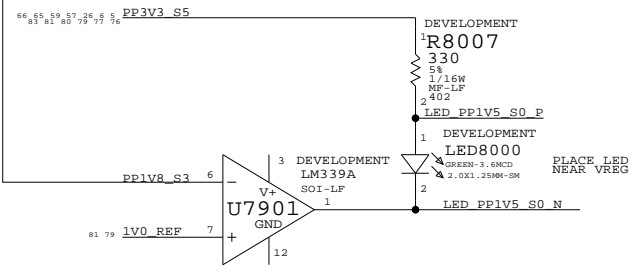
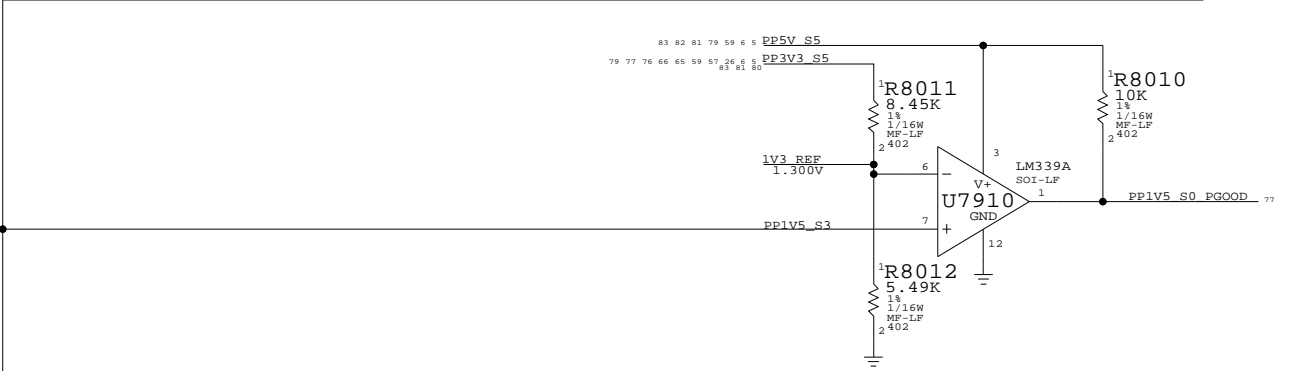
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	79 OF	111
NONE			

1.5V S0 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

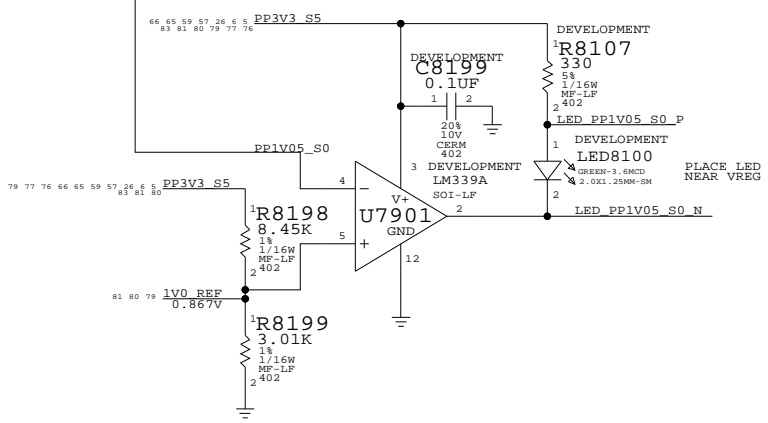
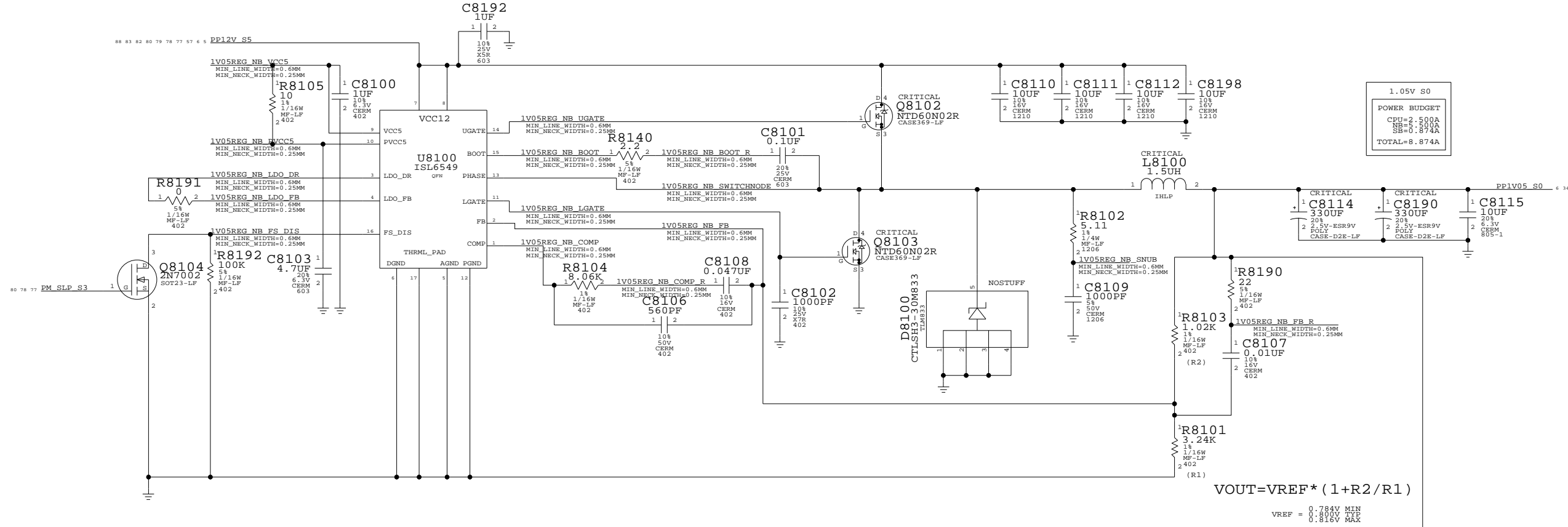
VREF = 0.784V MIN
0.800V TYP
0.816V MAX



1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	80 OF	111
NONE			

1.05V S0 REGULATOR



1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

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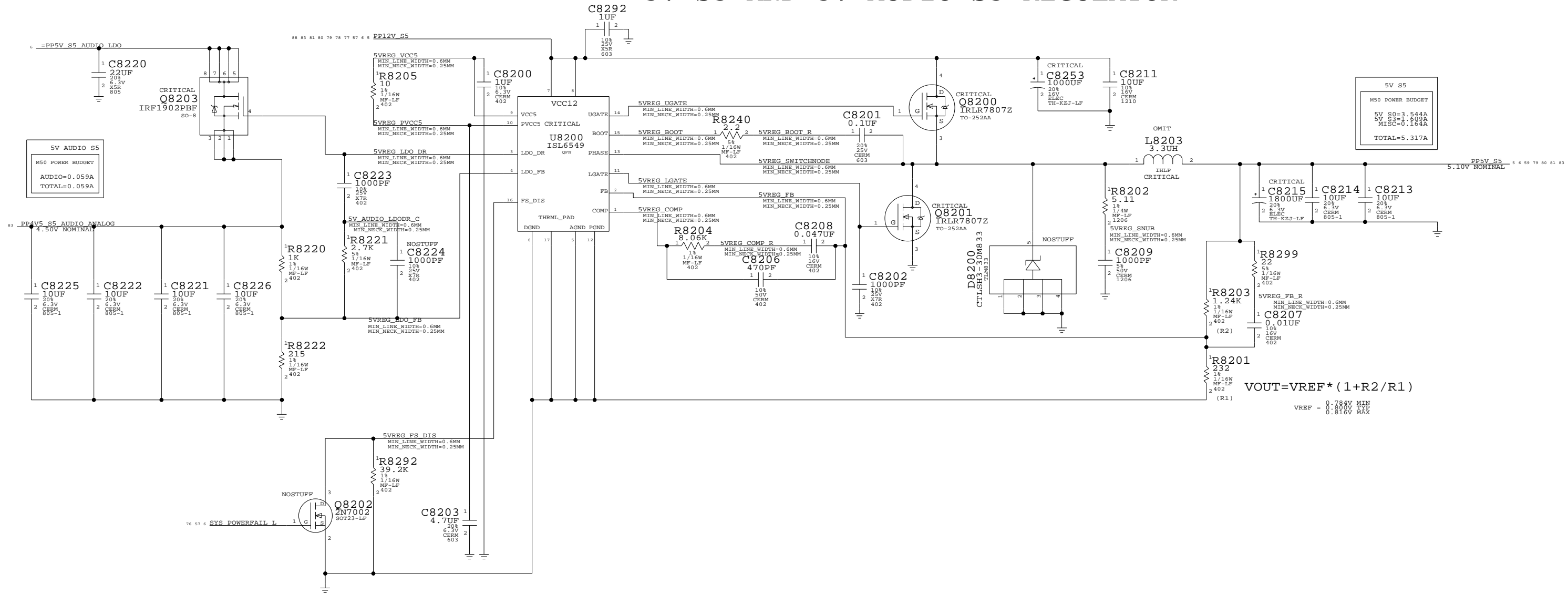
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II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	81 OF	111
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

5V DC/DC 4.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

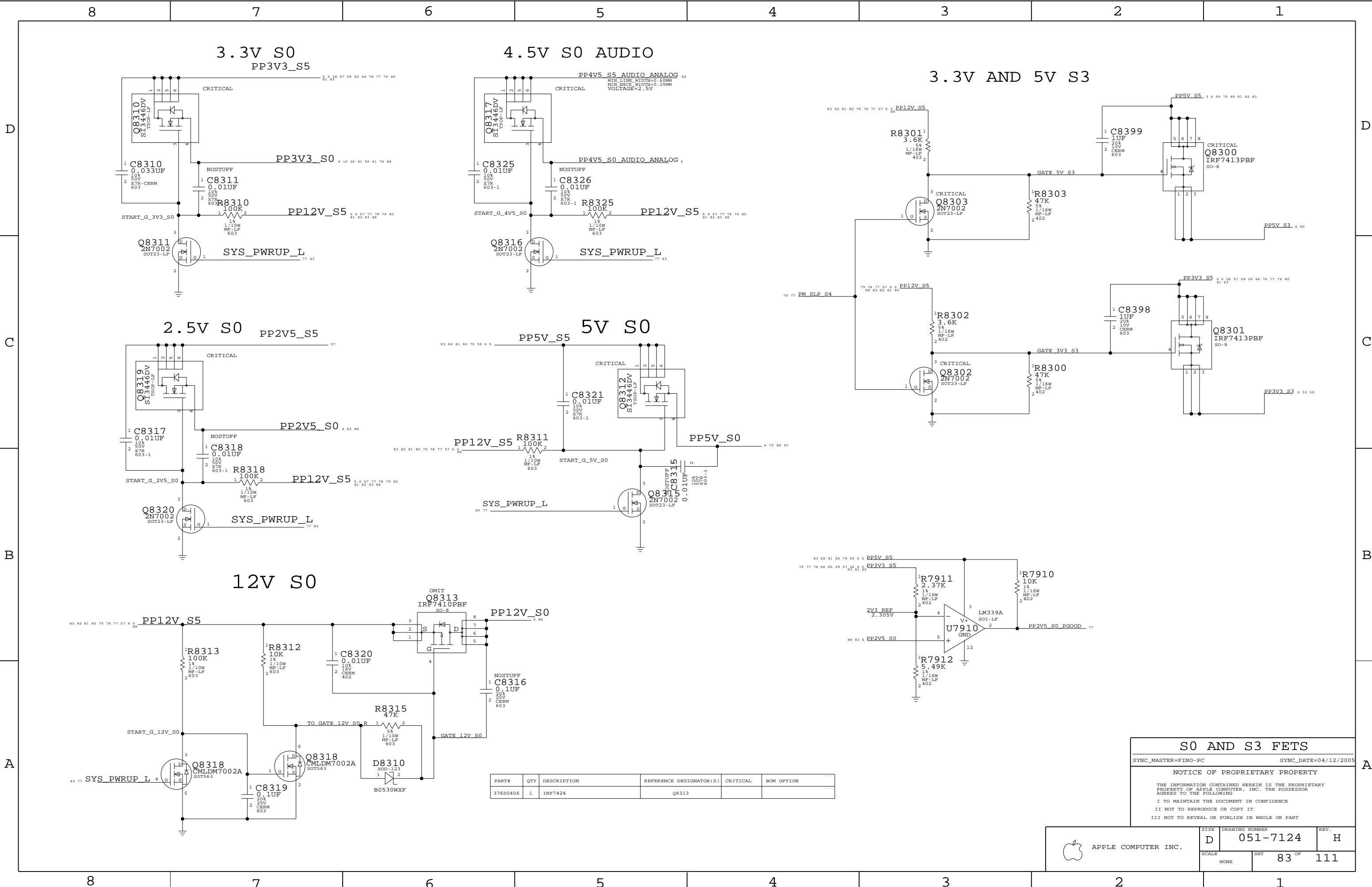
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	82 OF	111
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S0406	1	IRF7424	Q8313		

S0 AND S3 FETS

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

NOTICE OF PROPRIETARY PROPERTY

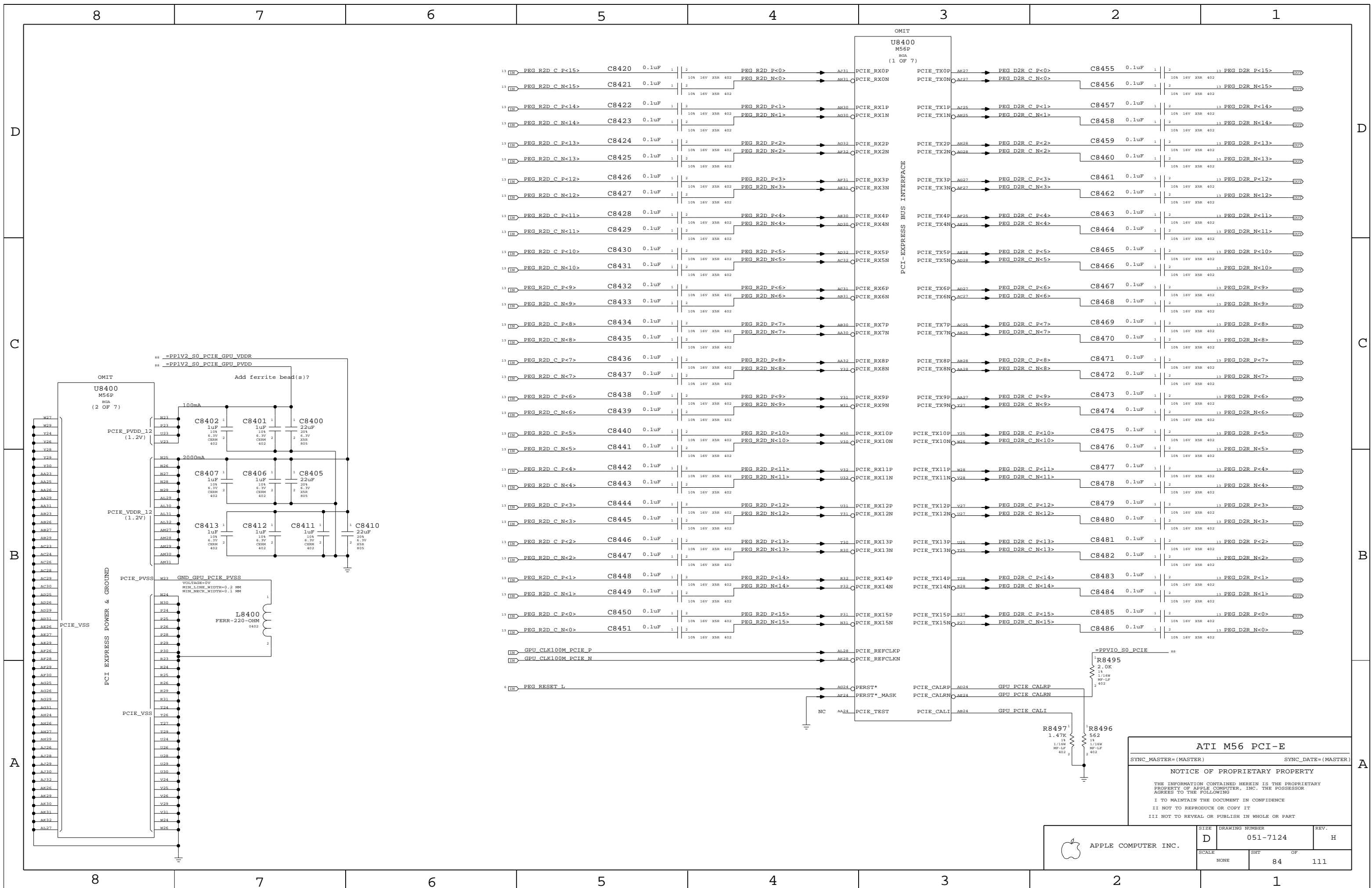
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	83 OF	111
NONE			



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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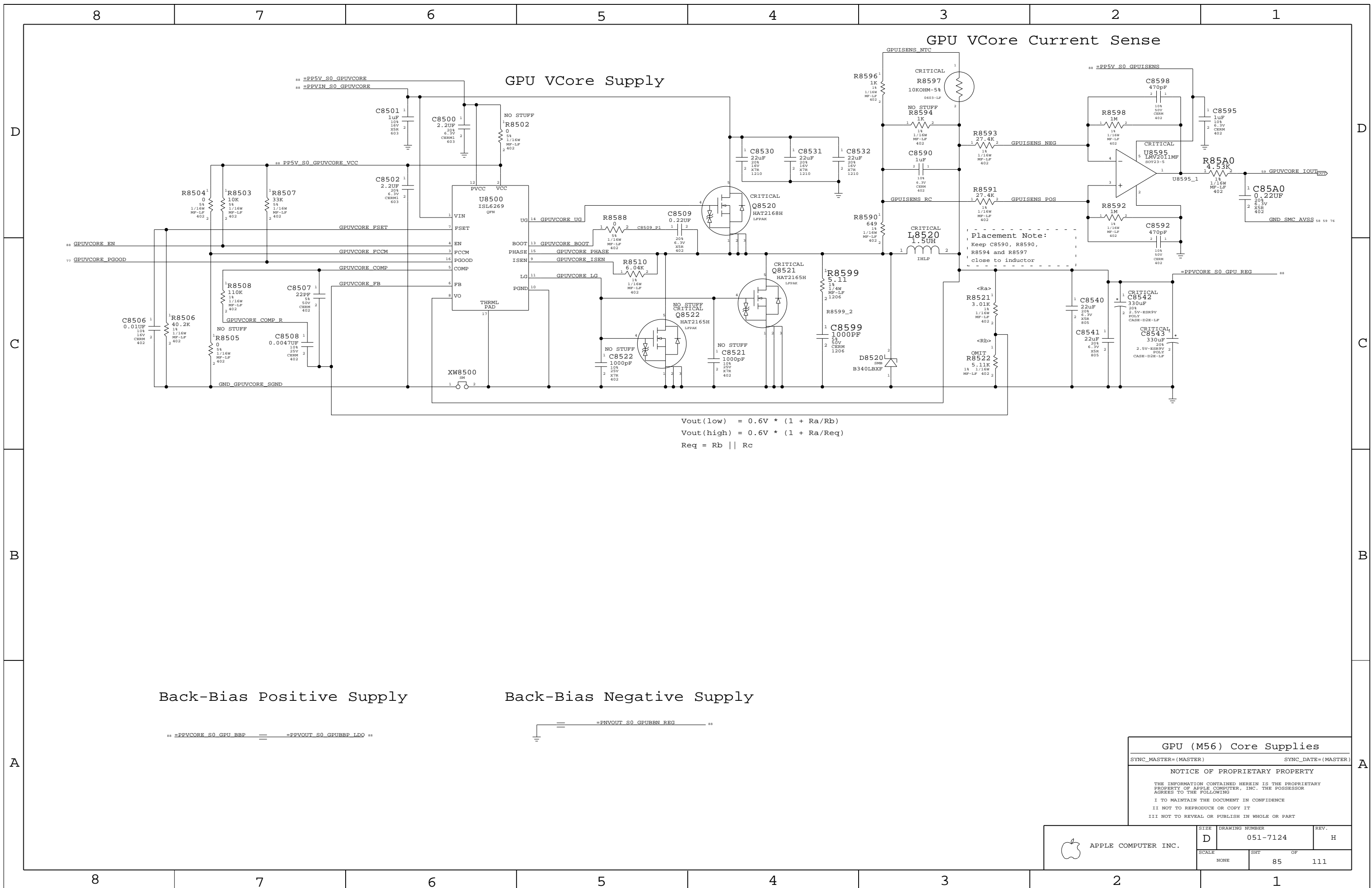
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHEET 84	OF 111



GPU VCore Supply

GPU VCore Current Sense

Placement Note:
 Keep C8590, R8590,
 R8594 and R8597
 close to inductor

$$V_{out}(low) = 0.6V * (1 + R_a/R_b)$$

$$V_{out}(high) = 0.6V * (1 + R_a/R_{eq})$$

$$R_{eq} = R_b || R_c$$

Back-Bias Positive Supply

Back-Bias Negative Supply

== =PPVCORE_S0_GPU_BBP == =PPVOUT_S0_GPUBBP_LDO ==

=PENVOUT_S0_GPUBBN_REG

GPU (M56) Core Supplies
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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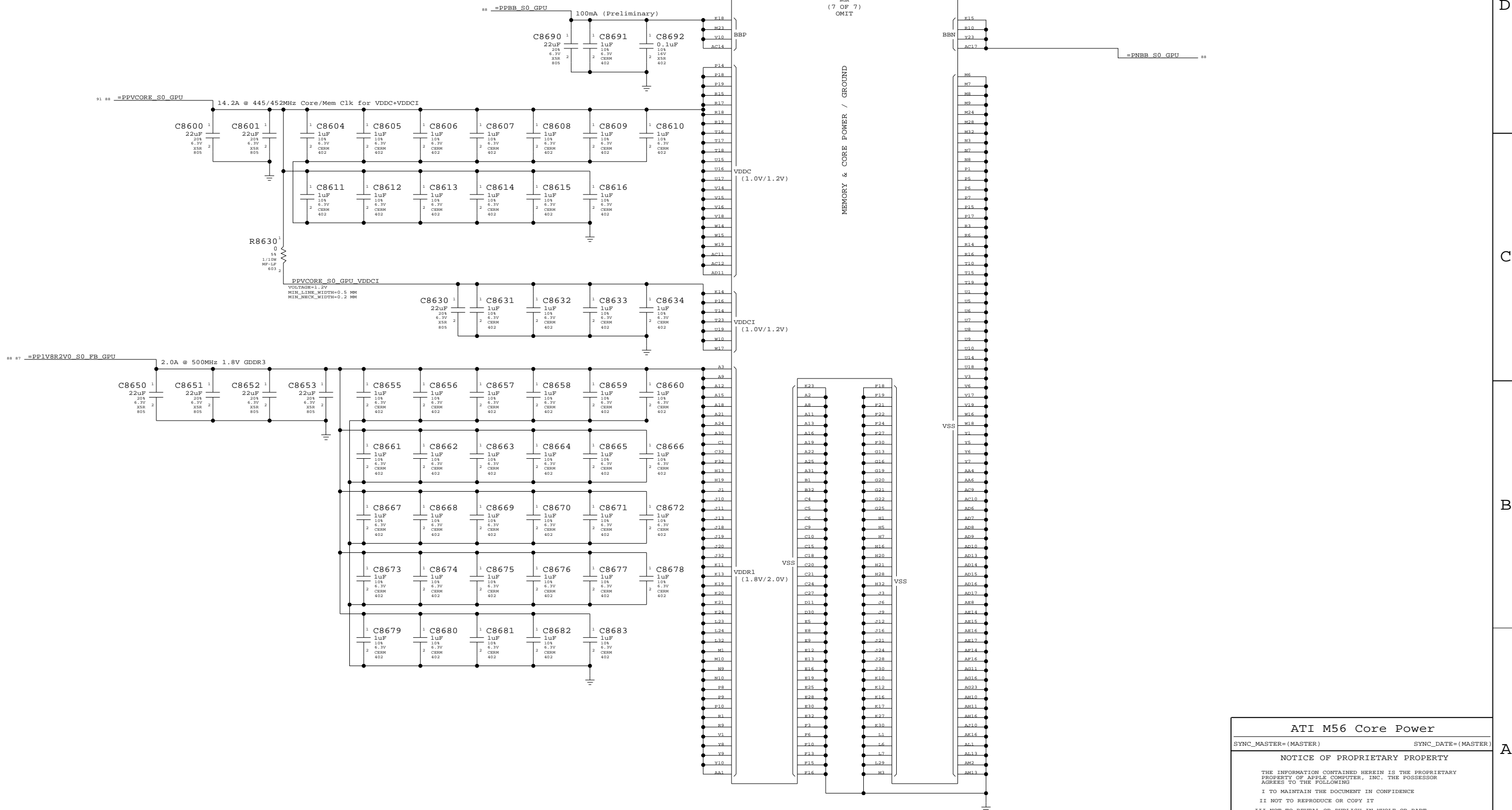
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	85	111	

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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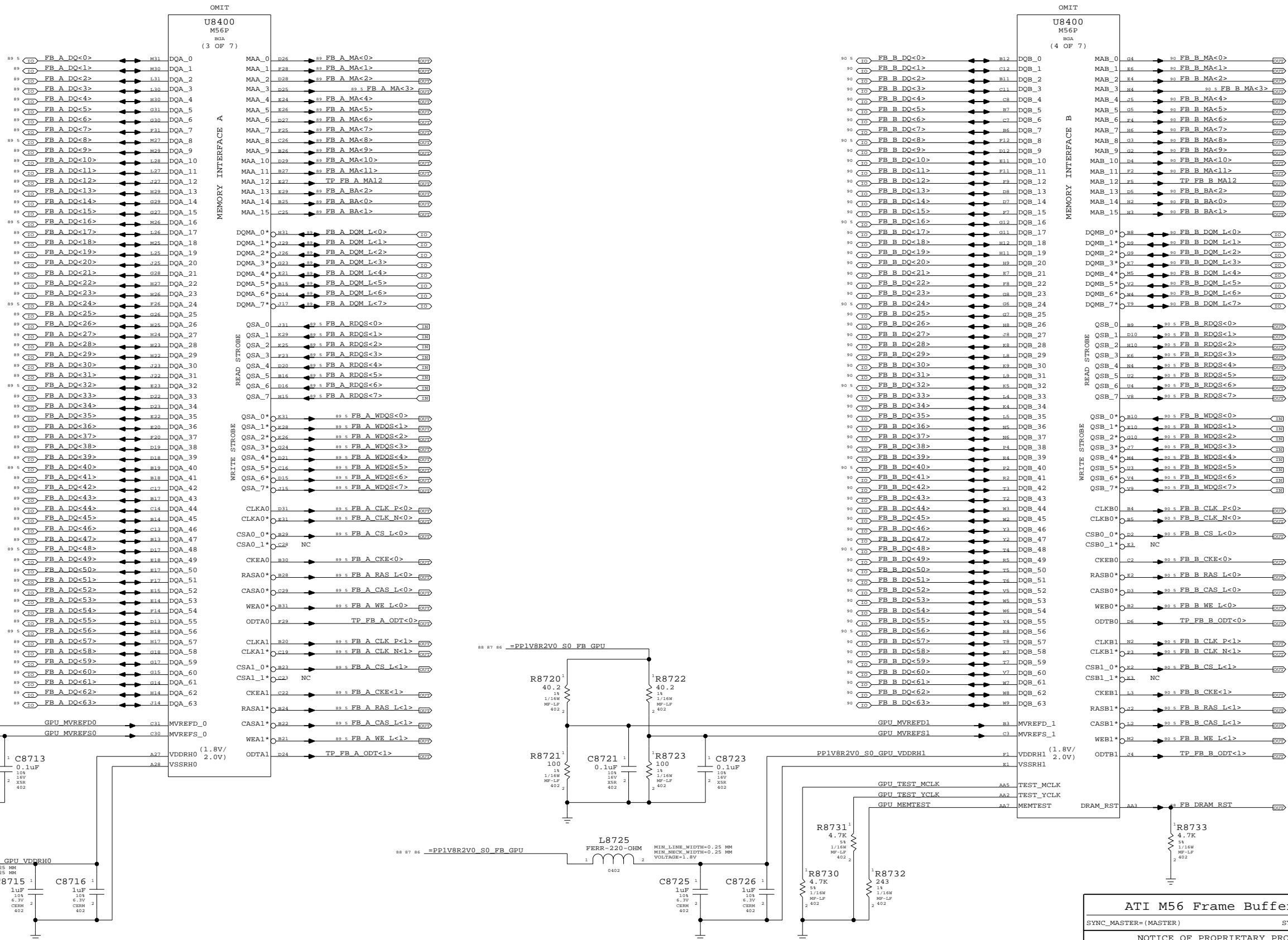
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	86	111	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



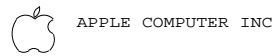
ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Table with columns for SIZE, DRAWING NUMBER, REV., SCALE, SHEET, and OF. Values include D, 051-7124, H, NONE, 87, 111.



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"S0" GPU RAILS

ONLY ON IN RUN

59 EP1V0R1V2_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

85 PP5V_S0_GPUVCORE_VCC
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

PP1V2_GPU_IO_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PPBB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PNBB_S0_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.2MM
 VOLTAGE=0

83 76 61 59 41 26 10 6 PP3V3_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

83 6 PP2V5_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

PP1V8R2V0_S0_FB_GPU
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.8V

83 82 81 80 79 78 77 57 6 5 PP12V_S5
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

83 6 PP12V_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=1.2V

97 83 76 6 PP5V_S0
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

85 GPUVCORE_EN
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

87 FB_DRAM_RST
 MAKE_BASE=TRUE
 MIN_LINE_WIDTH=0.6MM
 MIN_NECK_WIDTH=0.125MM
 VOLTAGE=5V

M56 GPIOs

94 91 GPU_GPIO_0
 10K 1/16W 2 R8813
 GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
 10K 1/16W 2 R8802
 GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
 INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
 NOSTUFF R8803

91 GPU_GPIO_3
 NOSTUFF R8804

91 GPU_GPIO_4
 NOSTUFF R8805
 GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
 10K 1/16W 2 R8806

91 GPU_GPIO_6
 NOSTUFF R8807

TP_GPU_GPIO_7
 MAKE_BASE=TRUE
 GPU_GPIO_7 91

91 GPU_GPIO_8
 NOSTUFF R8808

NC_GPU_GPIO_10
 MAKE_BASE=TRUE
 GPU_GPIO_10 91

91 GPU_GPIO_9
 NOSTUFF R8809

91 GPU_GPIO_13
 NOSTUFF R8812

91 GPU_GPIO_12
 10K 1/16W 2 R8810
 ATI_FB_256M

91 GPU_GPIO_11
 NOSTUFF R8811

91 GPU_GPIO_24
 10K 1/16W 2 R8830
 ATI_FB_256M

91 GPU_GPIO_27
 10K 1/16W 2 R8831
 ATI_FB_HYNIX

91 GPU_GPIO_28
 10K 1/16W 2 R8832

91 GPU_GPIO_29
 10K 1/16W 2 R8833
 TMD5_PANEL

GPU_VCORE_LOW
 MAKE_BASE=TRUE
 GPU_GPIO_15 91

91 GPU_GPIO_15
 10K 1/16W 2 R8850
 GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
 EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
 MAKE_BASE=TRUE
 GPU_GPIO_14 91

TP_GPU_GPIO_17
 MAKE_BASE=TRUE
 GPU_GPIO_17 91

TP_GPU_VGA_R
 MAKE_BASE=TRUE
 GPU_VGA_R 91

TP_GPU_VGA_G
 MAKE_BASE=TRUE
 GPU_VGA_G 91

TP_GPU_VGA_B
 MAKE_BASE=TRUE
 GPU_VGA_B 91

TP_GPU_VGA_HSYNC
 MAKE_BASE=TRUE
 GPU_VGA_HSYNC 91

TP_GPU_VGA_VSYNC
 MAKE_BASE=TRUE
 GPU_VGA_VSYNC 91

TP_GPU_TV_Y
 MAKE_BASE=TRUE
 GPU_TV_Y 91

TP_GPU_TV_COMP
 MAKE_BASE=TRUE
 GPU_TV_COMP 91

TP_GPU_TV_C
 MAKE_BASE=TRUE
 GPU_TV_C 91

TP_GPU_DDC_B_CLK
 MAKE_BASE=TRUE
 GPU_DDC_B_CLK 91

TP_GPU_DDC_B_DATA
 MAKE_BASE=TRUE
 GPU_DDC_B_DATA 91

GPU MISC

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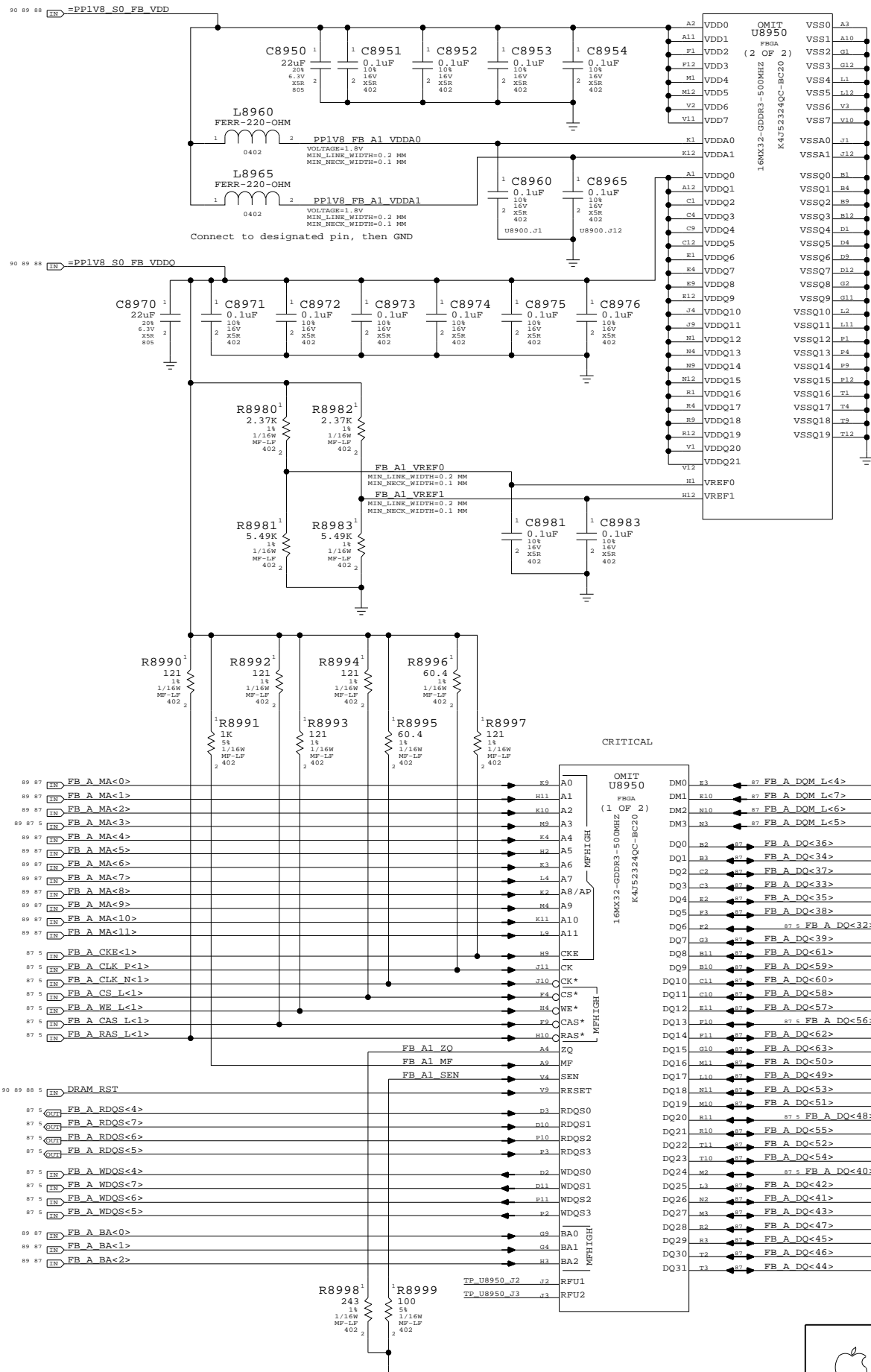
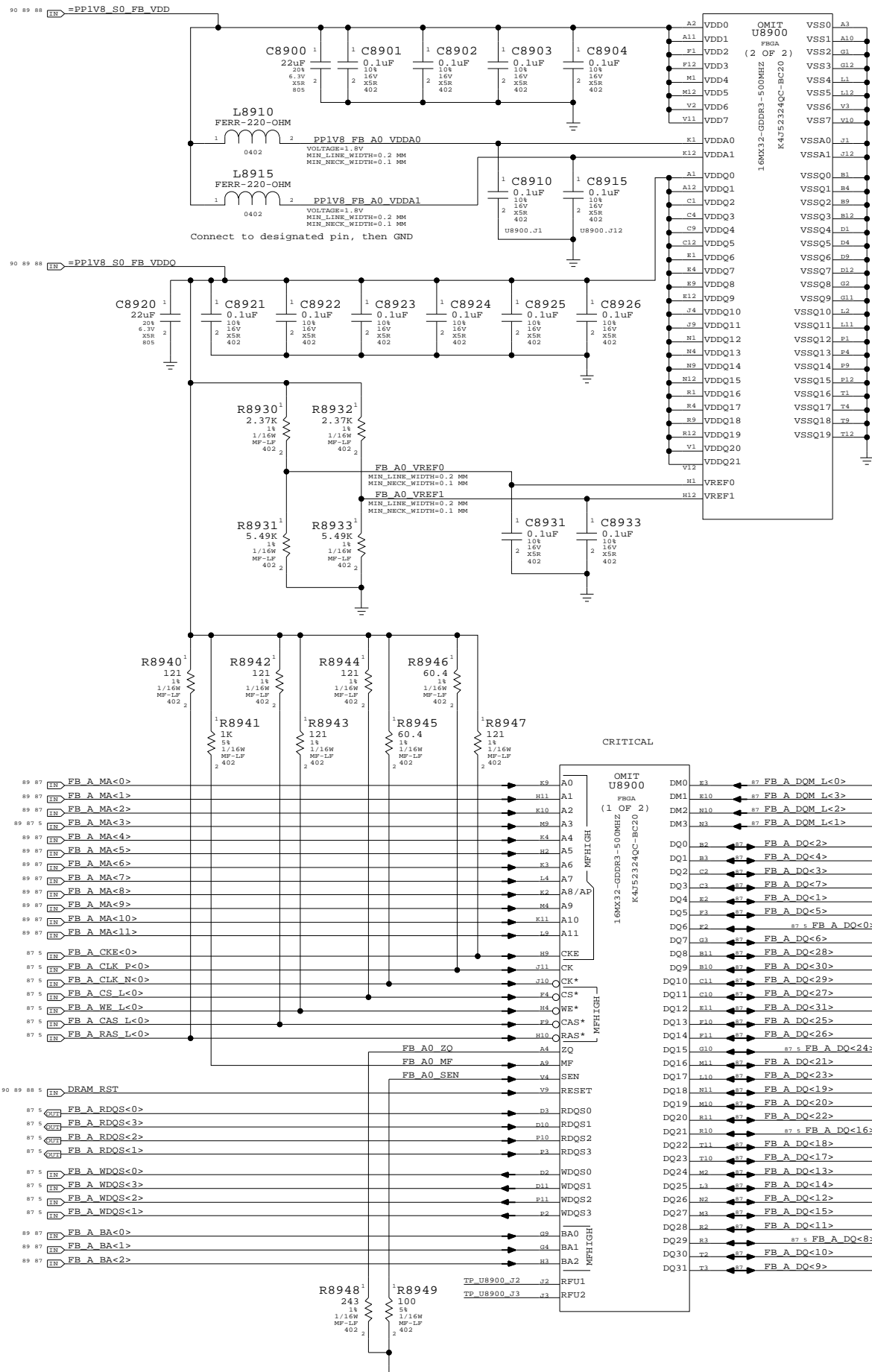
Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

CRITICAL

CRITICAL



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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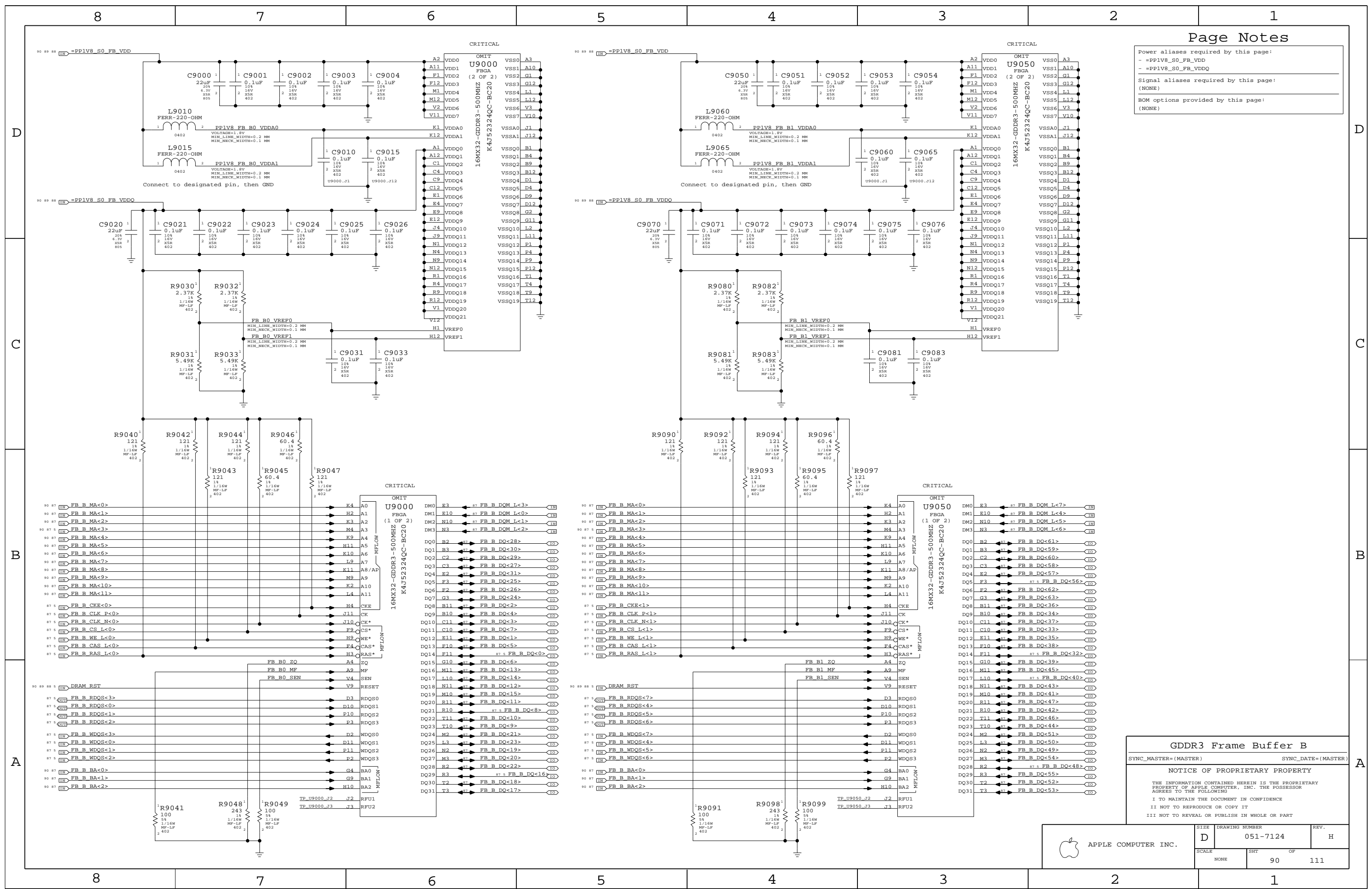
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	89	111	

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7124	H
90		OF	111



APPLE COMPUTER INC.

Page Notes

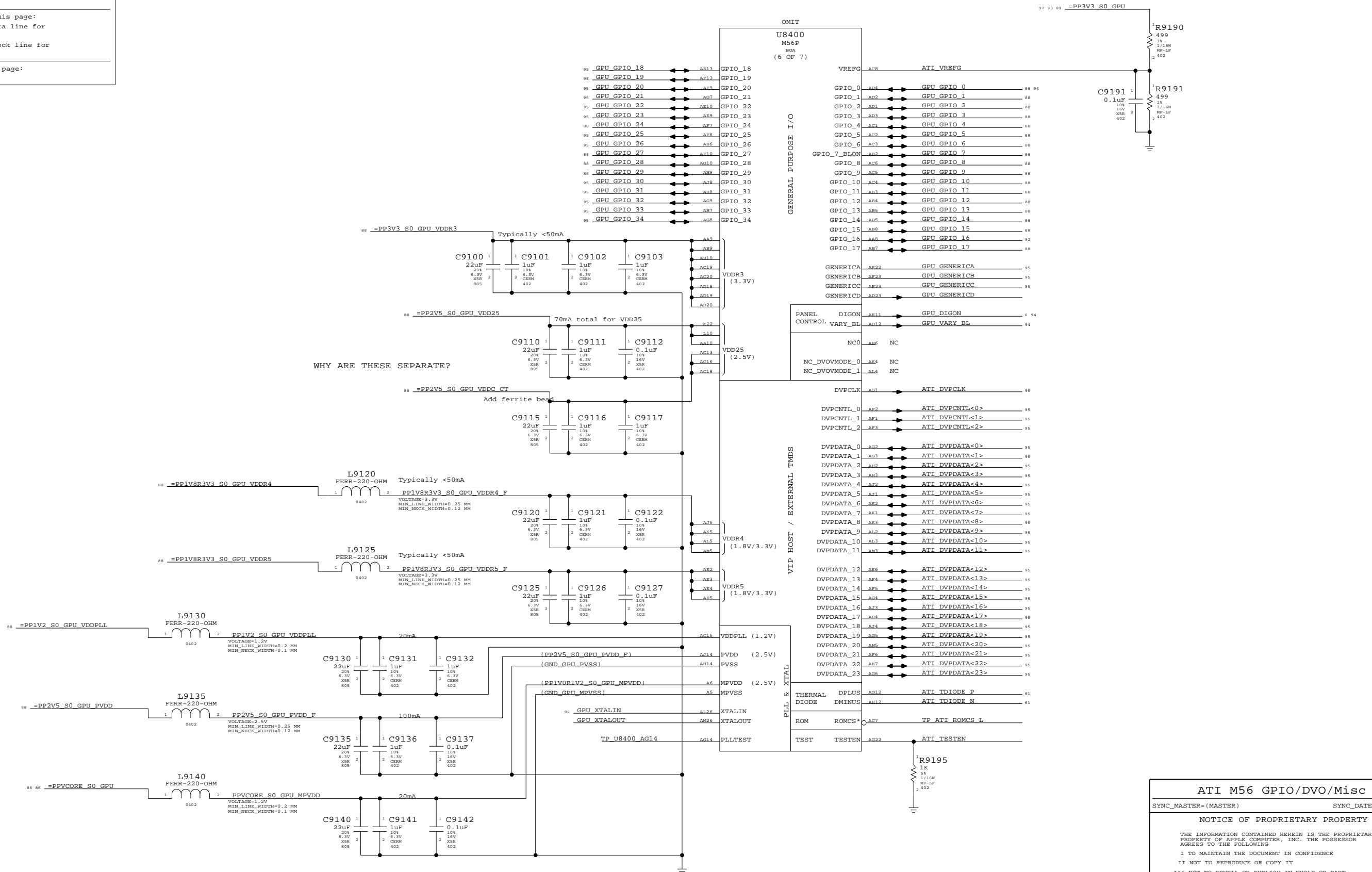
Power aliases required by this page:

- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:

- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7124	H
SCALE	SHT	OF	
NONE	91	111	

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Page Notes

Power aliases required by this page:

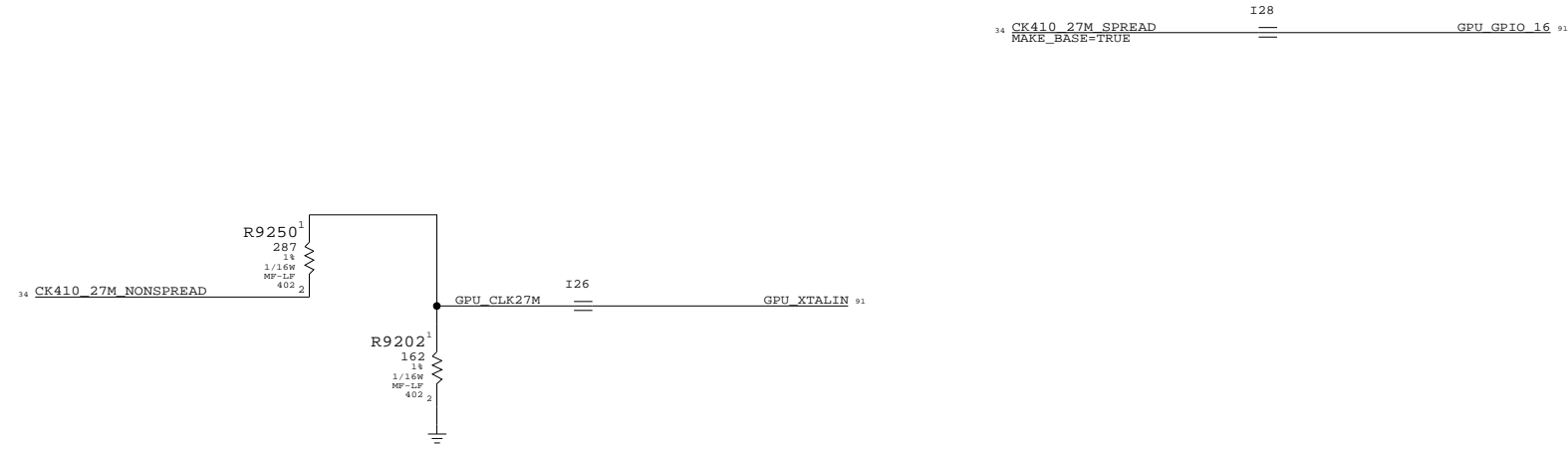
- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8




GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7124	REV. H
	SCALE NONE	SHT 92	OF 111

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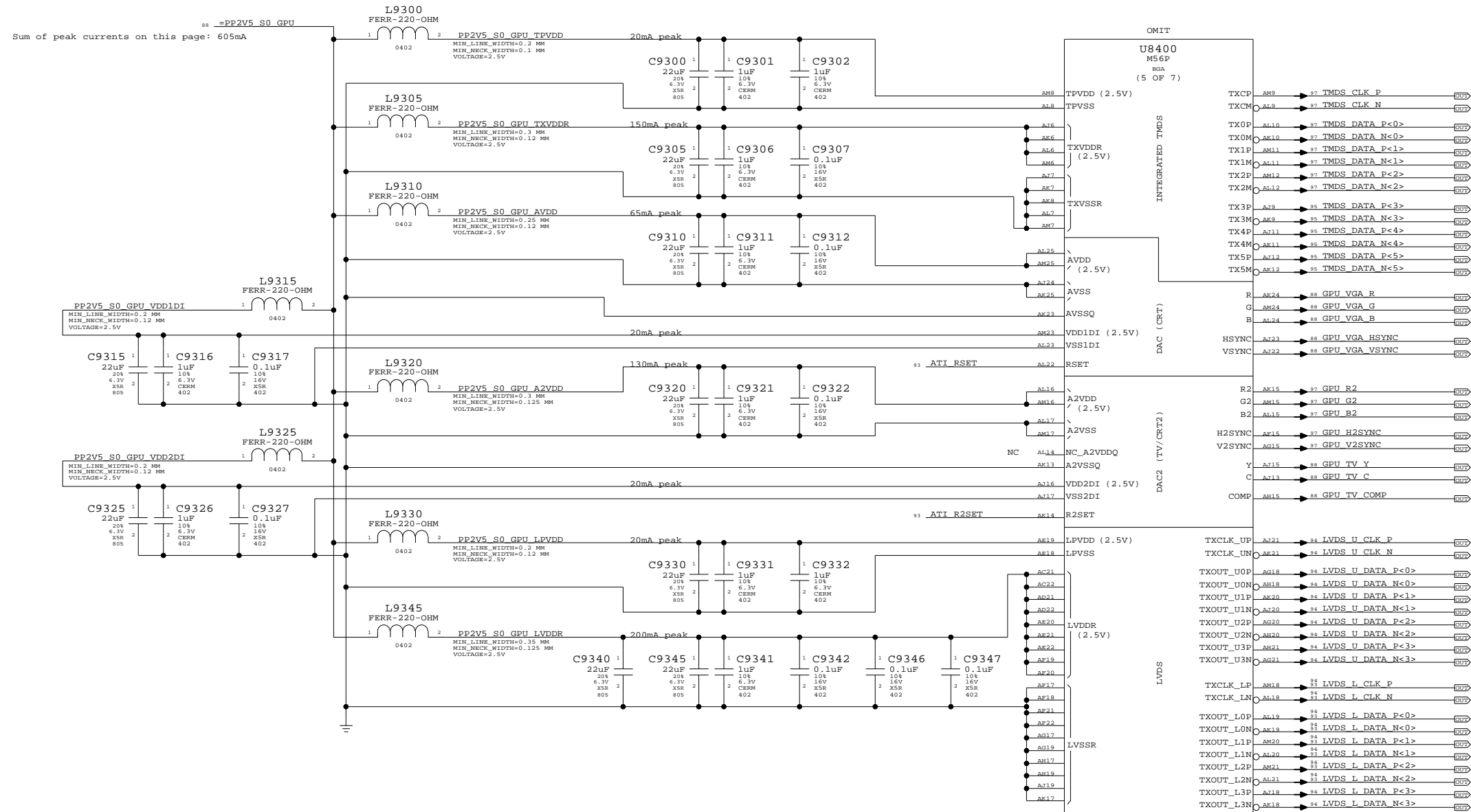
Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

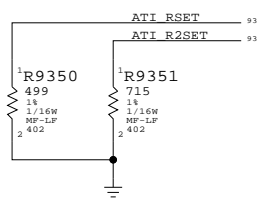
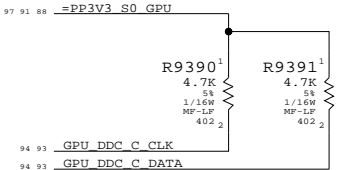
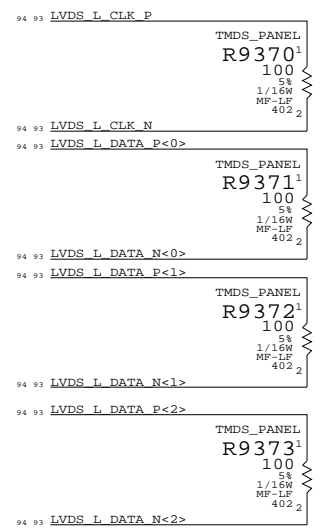
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb



ATI M56 Video Interfaces

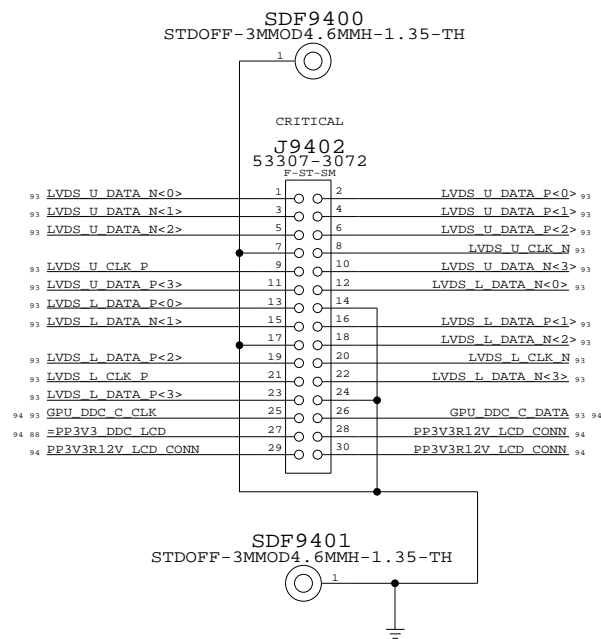
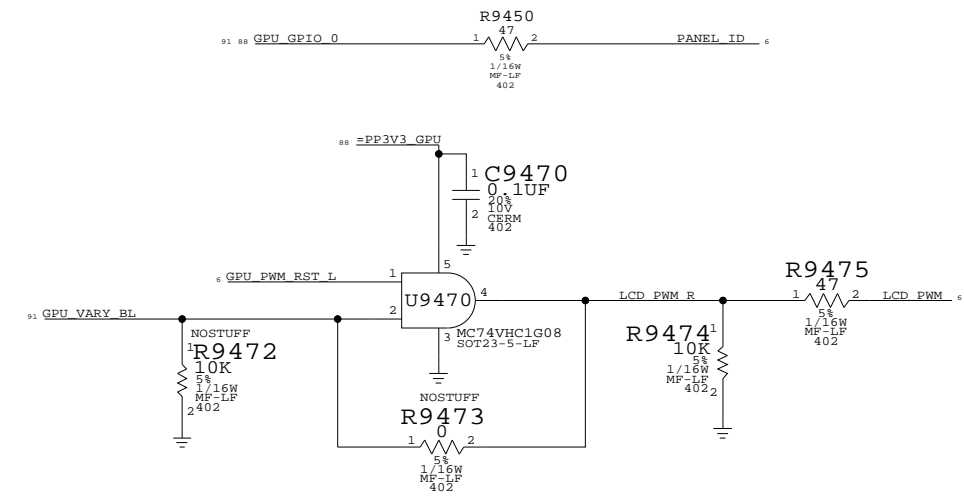
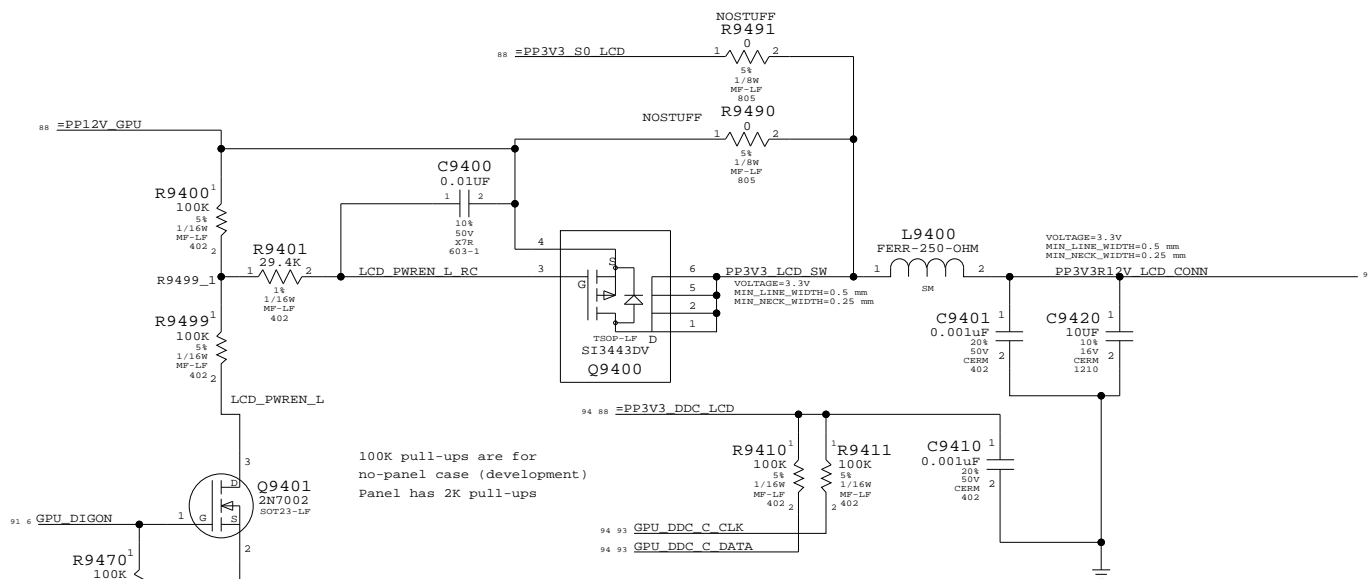
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	NONE	93	111	H

LCD (LVDS) INTERFACE



Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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	D	051-7124	H
SCALE	SHT	OF	
NONE	94	111	

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TP TMSD DATA P<3> == TMSD DATA P<3> 91
 MAKE_BASE=TRUE

TP TMSD DATA N<3> == TMSD DATA N<3> 91
 MAKE_BASE=TRUE

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TP GPU GPIO<26> == GPU_GPIO_26 91
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TP GPU GENERICB == GPU_GENERICB 91
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TP GPU GENERICC == GPU_GENERICC 91
 MAKE_BASE=TRUE

M56 TPS

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SIZE	DRAWING NUMBER	REV.
D	051-7124	H
SCALE	SHT	OF
NONE	95	111

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8 7 6 5 4 3 2 1

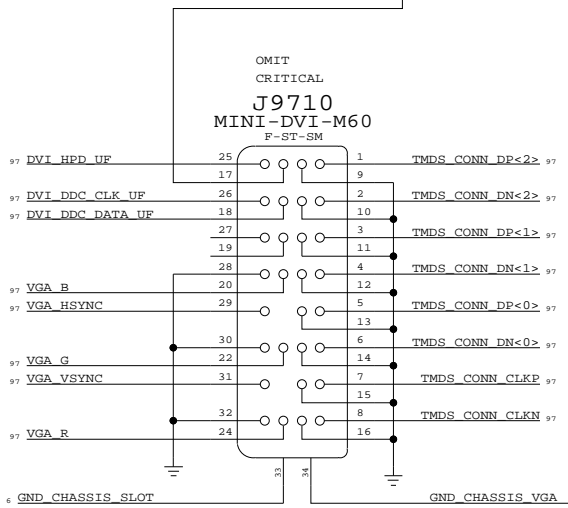
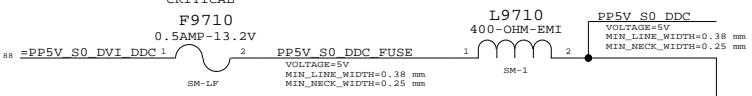
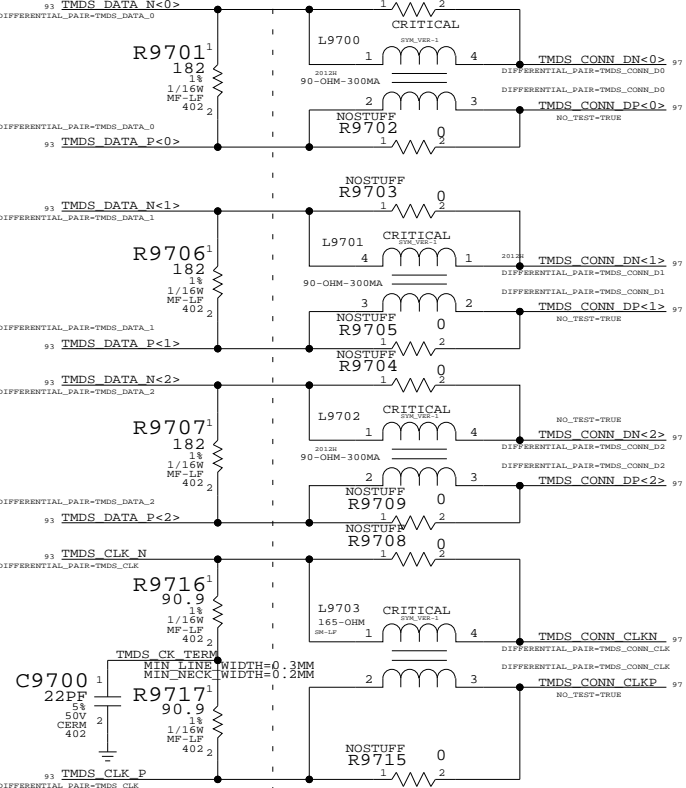
PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

PLACE FILTER CLOSE
TO TMD5 CONNECTOR

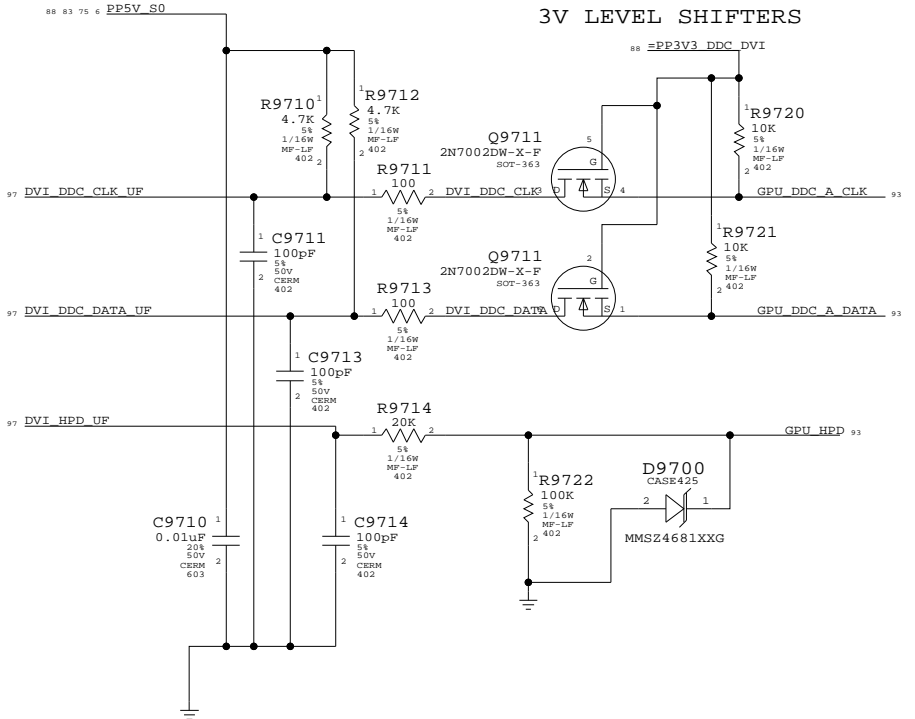
DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
740S0044	740S0028		F9710	FUSE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514S0125	1	M39 MINI-DVI CONN	J9710	



D

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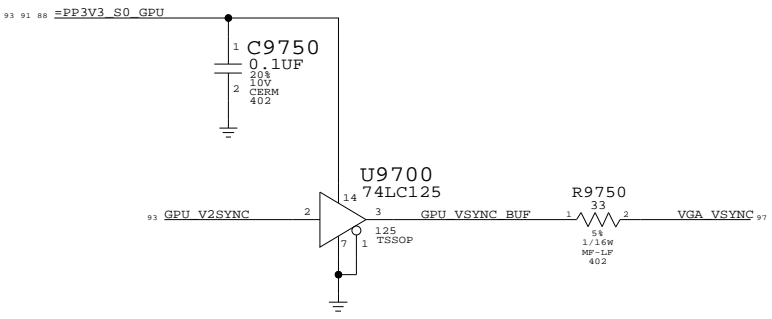
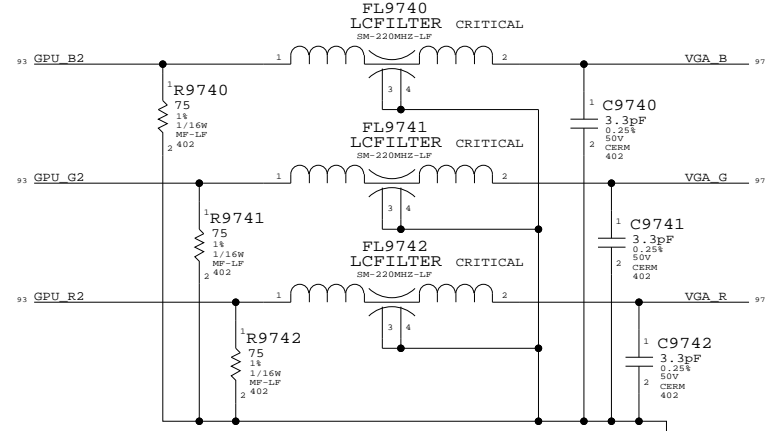
B

B

A

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ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

External Display Conns
SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005
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	<p>Title: Cref Part Report Design: m60 Date: Jun 23 16:28:15 2006</p> <p>C85A0 CAP_402 m60[85D1] C600 CAP_402 m60[6C7] C601 CAP_402 m60[6A3] C602 CAP_402 m60[6A3] C603 CAP_402 m60[6A3] C620 CAP_603 m60[6D6] C621 CAP_603 m60[6D6] C622 CAP_805 m60[6D7] C623 CAP_805-2 m60[6D7] C624 CAP_1210 m60[6D8] C625 CAP_P_6_3X5.5-SM m60[6D8] C0800 CAP_402 m60[8B5] C0901 CAP_603 m60[9B5] C900 CAP_805 m60[9B6] C901 CAP_805 m60[9B6] C902 CAP_805 m60[9A6] C903 CAP_805 m60[9A6] C904 CAP_805 m60[9A6] C905 CAP_805 m60[9A6] C906 CAP_805 m60[9A6] C907 CAP_805 m60[9B5] C908 CAP_805 m60[9B7] C909 CAP_805 m60[9B5] C910 CAP_805 m60[9B7] C911 CAP_805 m60[9B7] C912 CAP_805 m60[9A7] C913 CAP_805 m60[9A7] C914 CAP_805 m60[9A7] C915 CAP_805 m60[9A7] C916 CAP_805 m60[9A7] C917 CAP_805 m60[9A7] C918 CAP_P_CASE-C1 m60[9A7] C919 CAP_805 m60[9A7] C920 CAP_805 m60[9A5] C921 CAP_805 m60[9A7] C922 CAP_805 m60[9A7] C923 CAP_805 m60[9B7] C924 CAP_805 m60[9A7] C925 CAP_805 m60[9A7] C926 CAP_402 m60[9B7] C928 CAP_805 m60[9B6] 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m60[45C4] C4505 CAP_402 m60[45C5] C4506 CAP_402 m60[45C5] C4507 CAP_402 m60[45C5] C4508 CAP_402 m60[45D5] C4509 CAP_402 m60[45D5] C4510 CAP_402 m60[45D5] C4515 CAP_805-1 m60[45D6] C4520 CAP_402 m60[45D5] C4521 CAP_402 m60[45D4] C4522 CAP_402 m60[45D3] C4523 CAP_402 m60[45D3] C4609 CAP_603-1 m60[46D5] C4610 CAP_402 m60[46D4] C4611 CAP_402 m60[46D4] C4612 CAP_402 m60[46C4] C4613 CAP_402 m60[46C4] C4615 CAP_603-1 m60[46C2] C4616 CAP_402 m60[46B2] C4620 CAP_402 m60[46B4] C4621 CAP_402 m60[46B4] C4622 CAP_402 m60[46A4] C4623 CAP_402 m60[46A4] C4625 CAP_603-1 m60[46A2] C4626 CAP_402 m60[46A2] C4650 CAP_402 m60[46C7] C4654 CAP_402 m60[46B8] C4660 CAP_402 m60[46C7] C4664 CAP_402 m60[46B7] C4700 CAP_805-1 m60[47C8] C4710 CAP_P_B2 m60[47D6] C4712 CAP_402 m60[47D5] C4713 CAP_402 m60[47D5] C4720 CAP_P_B2 m60[47C5] C4722 CAP_402 m60[47C5] C4723 CAP_402 m60[47C5] C4730 CAP_P_B2 m60[47B6] C4732 CAP_402 m60[47A5] C4733 CAP_402 m60[47A5] C4742 CAP_402 m60[47D2] C4743 CAP_402 m60[47D1] C4750 CAP_402 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C7512 CAP_603 m60[75C2] C7513 CAP_402 m60[75B7] C7514 CAP_402 m60[75B8] C7515 CAP_603 m60[75C4]</p>				

Table with 8 columns and 8 rows. Each cell contains alphanumeric identifiers and codes. The grid is labeled with 'A', 'B', 'C', and 'D' along the edges. The columns are numbered 1 to 8 from right to left, and the rows are numbered 1 to 8 from bottom to top.

Main grid structure with columns 1-8 and rows A-D. Contains detailed component lists with part numbers, descriptions, and quantities.

8 7 6 5 4 3 2 1

D

C

B

A

D

C

B

A

Column 8 table containing component data for the first column of the grid.

Column 7 table containing component data for the second column of the grid.

Column 6 table containing component data for the third column of the grid.

Column 5 table containing component data for the fourth column of the grid.

Column 4 table containing component data for the fifth column of the grid.

Column 3 table containing component data for the sixth column of the grid.

Column 2 table containing component data for the seventh column of the grid.

Column 1 table containing component data for the eighth column of the grid.

8 7 6 5 4 3 2 1

