1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M39 - DVT

11/16/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
06		400374	ENGINEERING RELEASED	09/16/05	06/22/04

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

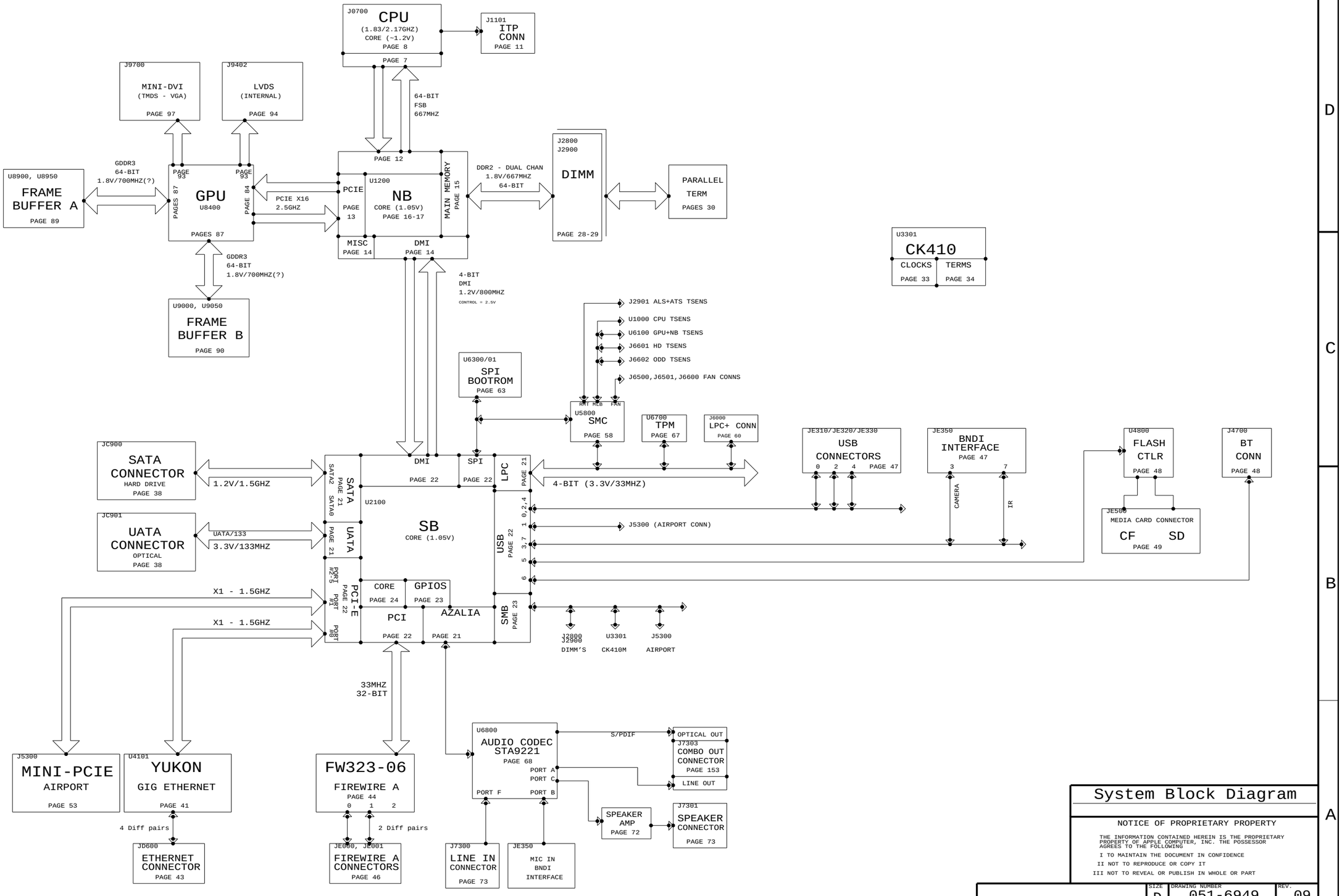
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE: SCHEM,M39

DRAWING NUMBER 051-6950 REV. 06

SHT 1 OF 111



System Block Diagram

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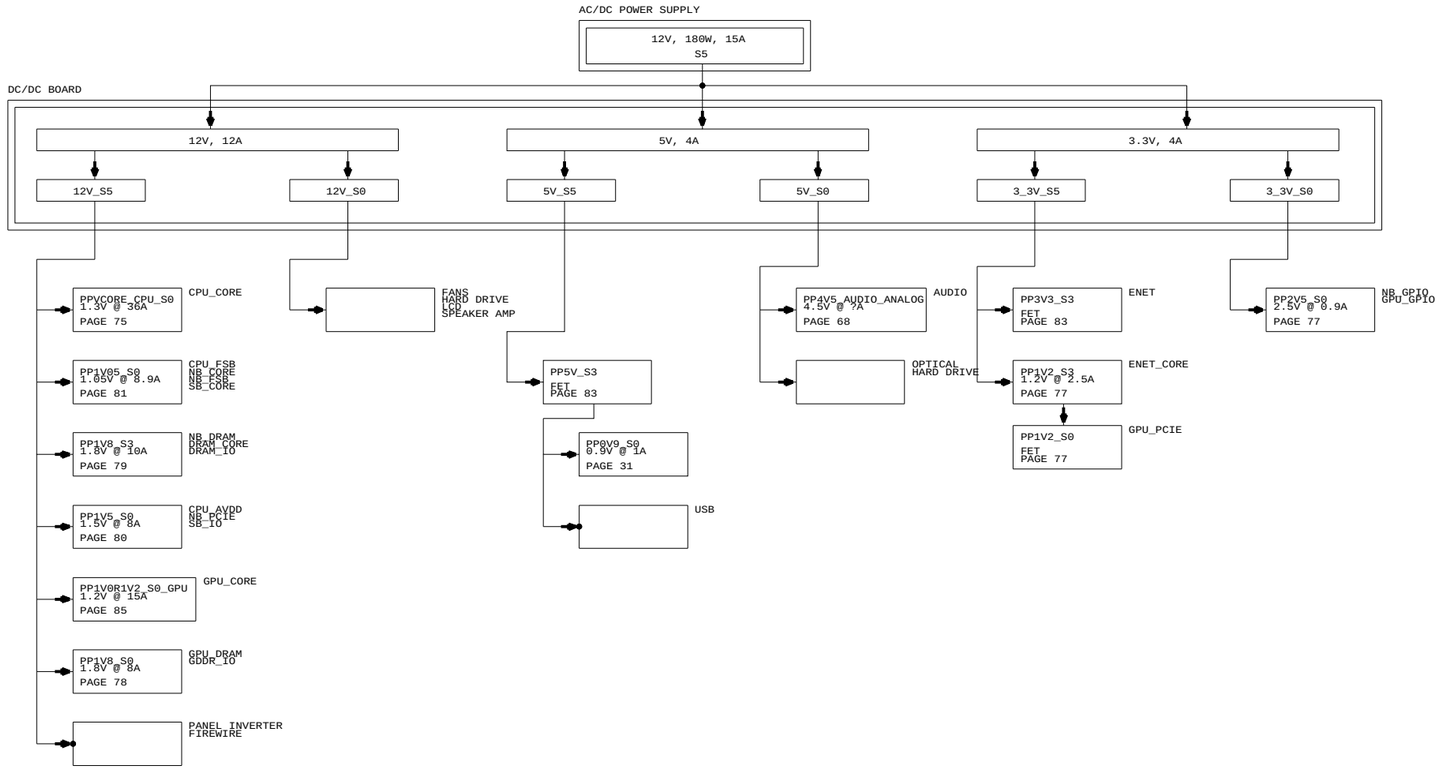
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 2 OF 111	



Power Block Diagram

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	3	111

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN,NO	U4101	CRITICAL	
(335S0382)	341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274	1	IC,SMC,HS8/2116,BLANK	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	
338S0266	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_B24
338S0305	1	IC,ATI,M56P,GRAFIX CTLR,880BGA,LF	U8400	CRITICAL	ATI_A24
128S0078	3	CAP,EL,AL,330UF,20%,16V,10X12.7MM,SMD,LF	C7517,C7518,C7910	CRITICAL	

M38

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6949	1	PCB,SCHEM,MLB,M38	SCH1		17_INCH_LCD
820-1919	1	PCB,FAB,MLB,M38	MLB1		17_INCH_LCD
(335S0384)	341T0003	1	EFI ROM,M38	U6301	CRITICAL
337S3241	1	M38/M39 LOW-SPEED CPU (QINY)	CPU	CRITICAL	CPU_M38
337S3242	1	M00-SPEED CPU (QINZ)	CPU	CRITICAL	CPU_M00

M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-6950	1	PCB,SCHEM,MLB,M39	SCH1		20_INCH_LCD
820-1888	1	PCB,FAB,MLB,M39	MLB1		20_INCH_LCD
(335S0384)	341T0004	1	EFI ROM,M39	U6301	CRITICAL
337S3243	1	M39 HI-SPEED CPU (QHJJ)	CPU	CRITICAL	CPU_M39

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0096	126S0076		C7801	SANYO W16CE680KX 680UF 16V LF
126S0086	126S0078		C699,C940,C1900,C1901,C1968	SANYO W6CE330FS 330UF 6.3V LF
128S0080	128S0078		C7517,C7518,C7910	SANYO 16SVP330M 330UF 16V SMD LF
197S0177	197S0020		Y4101	XTAL,25MHZ,50PPM,16PF,3.2X2.5 SMD,LF
338S0302	338S0266		U8400	IC,ATI,M36D,GRAFIX CTLR,880BGA,LF

M38 / M39

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_128M_HYNIX

M39 - CTO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_SAMSUNG
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136FBGA	U8900,U8950,U9000,U9050	CRITICAL	ATI_FB_256M_HYNIX

Table Items

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6949 | REV. 09

SCALE NONE | SHT 4 OF 111

LAYOUT NOTE: PLACE NEAR J0700

12 7 5	FSB_A_L<6>	PP600	PP	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP601	PP	OMIT P4MM
12 7 5	FSB_A_L<27>	PP602	PP	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP603	PP	OMIT P4MM
12 7 5	FSB_D_L<0>	PP604	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP605	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP606	PP	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP607	PP	OMIT P4MM
12 7 5	FSB_D_L<16>	PP608	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP609	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP610	PP	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP611	PP	OMIT P4MM
12 7 5	FSB_D_L<41>	PP612	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP613	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP614	PP	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP615	PP	OMIT P4MM
12 7 5	FSB_D_L<59>	PP616	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP617	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP618	PP	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP619	PP	OMIT P4MM
12 7 5	FSB_LOCK_L	PP620	PP	OMIT P4MM
12 11 7	FSB_CPURST_L	PP621	PP	OMIT P4MM
21 7	CPU_INIT_L	PP622	PP	OMIT P4MM
21 7	CPU_A20M_L	PP623	PP	OMIT P4MM
21 7	CPU_IGNNE_L	PP624	PP	OMIT P4MM
21 7	CPU_STPCLK_L	PP625	PP	OMIT P4MM
21 7	CPU_INTR	PP626	PP	OMIT P4MM
21 7	CPU_NMI	PP627	PP	OMIT P4MM
21 7	CPU_SMI_L	PP628	PP	OMIT P4MM
34 7	FSB_CLK_CPU_P	PP629	PP	OMIT P4MM
34 7	FSB_CLK_CPU_N	PP630	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

34 21	SB_CLK100M_SATA_P	PP6C4	PP	OMIT P4MM
34 21	SB_CLK100M_SATA_N	PP6C5	PP	OMIT P4MM
38 21	IDE_PDIOR_L	PP6C6	PP	OMIT P4MM
38 21	IDE_PDIORDY	PP6C7	PP	OMIT P4MM
38 21	IDE_PDD<9>	PP6C8	PP	OMIT P4MM
34 22	PCI_CLK_SB	PP6D0	PP	OMIT P4MM
41 22	PCIE_A_D2R_P	PP6D1	PP	OMIT P4MM
41 22	PCIE_A_D2R_N	PP6D2	PP	OMIT P4MM
53 22	PCIE_B_D2R_P	PP5E1	PP	OMIT P4MM
53 22	PCIE_B_D2R_N	PP5E2	PP	OMIT P4MM
22 14	DMI_N2S_P<0>	PP6D3	PP	OMIT P4MM
22 14	DMI_N2S_N<0>	PP6D4	PP	OMIT P4MM
34 22	SB_CLK100M_DMI_P	PP6D5	PP	OMIT P4MM
34 22	SB_CLK100M_DMI_N	PP6D6	PP	OMIT P4MM
58 26 23	PM_SYSRST_L	PP6D7	PP	OMIT P4MM
58 44 23 67 60	PM_CLKRUN_L	PP6D8	PP	OMIT P4MM
34 23	SB_CLK14P3M_TIMER	PP6D9	PP	OMIT P4MM
34 23	SB_CLK48M_USBCTLR	PP6E0	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1200

12 7 5	FSB_A_L<6>	PP631	PP	OMIT P4MM
12 7 5	FSB_ADSTB_L<0>	PP632	PP	OMIT P4MM
12 7 5	FSB_A_L<27>	PP633	PP	OMIT P4MM
12 7 5	FSB_ADSTB_L<1>	PP634	PP	OMIT P4MM
12 7 5	FSB_D_L<0>	PP635	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<0>	PP636	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<0>	PP637	PP	OMIT P4MM
12 7 5	FSB_DINV_L<0>	PP638	PP	OMIT P4MM
12 7 5	FSB_D_L<16>	PP639	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<1>	PP640	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<1>	PP641	PP	OMIT P4MM
12 7 5	FSB_DINV_L<1>	PP642	PP	OMIT P4MM
12 7 5	FSB_D_L<41>	PP643	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<2>	PP644	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<2>	PP645	PP	OMIT P4MM
12 7 5	FSB_DINV_L<2>	PP646	PP	OMIT P4MM
12 7 5	FSB_D_L<59>	PP647	PP	OMIT P4MM
12 7 5	FSB_DSTBN_L<3>	PP648	PP	OMIT P4MM
12 7 5	FSB_DSTBP_L<3>	PP649	PP	OMIT P4MM
12 7 5	FSB_DINV_L<3>	PP650	PP	OMIT P4MM
12 7 5	FSB_LOCK_L	PP651	PP	OMIT P4MM
12 7	FSB_HIT_L	PP652	PP	OMIT P4MM
12 7	FSB_HITM_L	PP653	PP	OMIT P4MM
12 7	FSB_BNR_L	PP654	PP	OMIT P4MM
12 7	FSB_BREQ0_L	PP655	PP	OMIT P4MM
12 7	FSB_DBSY_L	PP656	PP	OMIT P4MM
12 7	FSB_DPWR_L	PP657	PP	OMIT P4MM
12 7	FSB_REQ_L<0>	PP658	PP	OMIT P4MM
12 7	FSB_REQ_L<1>	PP659	PP	OMIT P4MM
12 7	FSB_REQ_L<2>	PP660	PP	OMIT P4MM
12 7	FSB_REQ_L<3>	PP661	PP	OMIT P4MM
12 7	FSB_REQ_L<4>	PP662	PP	OMIT P4MM
34 12	FSB_CLK_NB_P	PP663	PP	OMIT P4MM
34 12	FSB_CLK_NB_N	PP664	PP	OMIT P4MM
75 26 14	VR_PWRGOOD_DELAY	PP665	PP	OMIT P4MM
14	NB_RST_IN_L_R	PP666	PP	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_P	PP667	PP	OMIT P4MM
34 14	NB_CLK100M_GCLKIN_N	PP668	PP	OMIT P4MM
22 14	DMI_S2N_N<0>	PP673	PP	OMIT P4MM
22 14	DMI_S2N_P<0>	PP674	PP	OMIT P4MM
19 14	MEM_VREF_NB_0	PP6E1	PP	OMIT P4MM
19 14	MEM_VREF_NB_1	PP675	PP	OMIT P4MM
28 15	MEM_A_DQ<7>	PP676	PP	OMIT P4MM
28 15	MEM_A_DQ<14>	PP677	PP	OMIT P4MM
28 15	MEM_A_DQ<16>	PP678	PP	OMIT P4MM
28 15	MEM_A_DQ<25>	PP679	PP	OMIT P4MM
28 15	MEM_A_DQ<39>	PP680	PP	OMIT P4MM
28 15	MEM_A_DQ<47>	PP681	PP	OMIT P4MM
28 15	MEM_A_DQ<54>	PP682	PP	OMIT P4MM
28 15	MEM_A_DQ<59>	PP683	PP	OMIT P4MM
29 15	MEM_A_DQS_P<0>	PP684	PP	OMIT P4MM
29 15	MEM_A_DQS_N<0>	PP685	PP	OMIT P4MM
28 15	MEM_A_DQS_P<1>	PP686	PP	OMIT P4MM
28 15	MEM_A_DQS_N<1>	PP687	PP	OMIT P4MM
28 15	MEM_A_DQS_P<2>	PP688	PP	OMIT P4MM
28 15	MEM_A_DQS_N<2>	PP689	PP	OMIT P4MM
28 15	MEM_A_DQS_P<3>	PP690	PP	OMIT P4MM
28 15	MEM_A_DQS_N<3>	PP691	PP	OMIT P4MM
28 15	MEM_A_DQS_P<4>	PP692	PP	OMIT P4MM
28 15	MEM_A_DQS_N<4>	PP693	PP	OMIT P4MM
28 15	MEM_A_DQS_P<5>	PP694	PP	OMIT P4MM
28 15	MEM_A_DQS_N<5>	PP695	PP	OMIT P4MM
28 15	MEM_A_DQS_P<6>	PP696	PP	OMIT P4MM
28 15	MEM_A_DQS_N<6>	PP697	PP	OMIT P4MM
28 15	MEM_A_DQS_P<7>	PP698	PP	OMIT P4MM
28 15	MEM_A_DQS_N<7>	PP699	PP	OMIT P4MM
29 15	MEM_B_DQ<6>	PP6A0	PP	OMIT P4MM
29 15	MEM_B_DQ<8>	PP6A1	PP	OMIT P4MM
29 15	MEM_B_DQ<23>	PP6A2	PP	OMIT P4MM
29 15	MEM_B_DQ<25>	PP6A3	PP	OMIT P4MM
29 15	MEM_B_DQ<38>	PP6A4	PP	OMIT P4MM
29 15	MEM_B_DQ<44>	PP6A5	PP	OMIT P4MM
29 15	MEM_B_DQ<48>	PP6A6	PP	OMIT P4MM
29 15	MEM_B_DQ<62>	PP6A7	PP	OMIT P4MM
29 15	MEM_B_DQS_P<0>	PP6A8	PP	OMIT P4MM
29 15	MEM_B_DQS_N<0>	PP6A9	PP	OMIT P4MM
29 15	MEM_B_DQS_P<1>	PP6B0	PP	OMIT P4MM
29 15	MEM_B_DQS_N<1>	PP6B1	PP	OMIT P4MM
29 15	MEM_B_DQS_P<2>	PP6B2	PP	OMIT P4MM
29 15	MEM_B_DQS_N<2>	PP6B3	PP	OMIT P4MM
29 15	MEM_B_DQS_P<3>	PP6B4	PP	OMIT P4MM
29 15	MEM_B_DQS_N<3>	PP6B5	PP	OMIT P4MM
29 15	MEM_B_DQS_P<4>	PP6B6	PP	OMIT P4MM
29 15	MEM_B_DQS_N<4>	PP6B7	PP	OMIT P4MM
29 15	MEM_B_DQS_P<5>	PP6B8	PP	OMIT P4MM
29 15	MEM_B_DQS_N<5>	PP6B9	PP	OMIT P4MM
29 15	MEM_B_DQS_P<6>	PP6C0	PP	OMIT P4MM
29 15	MEM_B_DQS_N<6>	PP6C1	PP	OMIT P4MM
29 15	MEM_B_DQS_P<7>	PP6C2	PP	OMIT P4MM
29 15	MEM_B_DQS_N<7>	PP6C3	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U8400

89 87 5	FB_A_DQ<0>	PP8700	PP	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8701	PP	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8702	PP	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8703	PP	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8704	PP	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8705	PP	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8706	PP	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8707	PP	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8708	PP	OMIT P4MM
89 87	FB_A_RDQS<0>	PP8709	PP	OMIT P4MM
89 87	FB_A_RDQS<1>	PP8710	PP	OMIT P4MM
89 87	FB_A_RDQS<2>	PP8711	PP	OMIT P4MM
89 87	FB_A_RDQS<3>	PP8712	PP	OMIT P4MM
89 87	FB_A_RDQS<4>	PP8713	PP	OMIT P4MM
89 87	FB_A_RDQS<5>	PP8714	PP	OMIT P4MM
89 87	FB_A_RDQS<6>	PP8715	PP	OMIT P4MM
89 87	FB_A_RDQS<7>	PP8716	PP	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP8720	PP	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP8721	PP	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP8722	PP	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP8723	PP	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP8724	PP	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP8725	PP	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP8726	PP	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP8727	PP	OMIT P4MM
90 87 5	FB_B_MA<3>	PP8728	PP	OMIT P4MM
90 87	FB_B_RDQS<0>	PP8729	PP	OMIT P4MM
90 87	FB_B_RDQS<1>	PP8730	PP	OMIT P4MM
90 87	FB_B_RDQS<2>	PP8731	PP	OMIT P4MM
90 87	FB_B_RDQS<3>	PP8732	PP	OMIT P4MM
90 87	FB_B_RDQS<4>	PP8733	PP	OMIT P4MM
90 87	FB_B_RDQS<5>	PP8734	PP	OMIT P4MM
90 87	FB_B_RDQS<6>	PP8735	PP	OMIT P4MM
90 87	FB_B_RDQS<7>	PP8736	PP	OMIT P4MM
84 34	GPU_CLK100M_PCIE_P	PP8400	PP	OMIT P4MM
84 34	GPU_CLK100M_PCIE_N	PP8401	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4101

41 34	ENET_CLK100M_PCIE_P	PP4100	PP	OMIT P4MM
41 34	ENET_CLK100M_PCIE_N	PP4101	PP	OMIT P4MM

PLACE NEAR U8900

89 87	FB_A_CKE<0>	PP8900	PP	OMIT P4MM
89 87	FB_A_CLK_P<0>	PP8901	PP	OMIT P4MM
89 87	FB_A_CLK_N<0>	PP8902	PP	OMIT P4MM
89 87	FB_A_CS_L<0>	PP8903	PP	OMIT P4MM
89 87	FB_A_WE_L<0>	PP8904	PP	OMIT P4MM
89 87	FB_A_CAS_L<0>	PP8905	PP	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8906	PP	OMIT P4MM
89 87	FB_A_RAS_L<0>	PP8907	PP	OMIT P4MM
90 89 88 5	DRAM_RST	PP8908	PP	OMIT P4MM
89 87	FB_A_WDQS<0>	PP8909	PP	OMIT P4MM
89 87	FB_A_WDQS<1>	PP8910	PP	OMIT P4MM
89 87	FB_A_WDQS<3>	PP8911	PP	OMIT P4MM
89 87	FB_A_WDQS<2>	PP8912	PP	OMIT P4MM
89 87 5	FB_A_DQ<0>	PP8913	PP	OMIT P4MM
89 87 5	FB_A_DQ<8>	PP8914	PP	OMIT P4MM
89 87 5	FB_A_DQ<16>	PP8915	PP	OMIT P4MM
89 87 5	FB_A_DQ<24>	PP8916	PP	OMIT P4MM

PLACE NEAR U8950

89 87	FB_A_CKE<1>	PP8920	PP	OMIT P4MM
89 87	FB_A_CLK_P<1>	PP8921	PP	OMIT P4MM
89 87	FB_A_CLK_N<1>	PP8922	PP	OMIT P4MM
89 87	FB_A_CS_L<1>	PP8923	PP	OMIT P4MM
89 87	FB_A_WE_L<1>	PP8924	PP	OMIT P4MM
89 87	FB_A_CAS_L<1>	PP8925	PP	OMIT P4MM
89 87	FB_A_RAS_L<1>	PP8926	PP	OMIT P4MM
89 87 5	FB_A_MA<3>	PP8927	PP	OMIT P4MM
90 89 88 5	DRAM_RST	PP8928	PP	OMIT P4MM
89 87	FB_A_WDQS<5>	PP8929	PP	OMIT P4MM
89 87	FB_A_WDQS<6>	PP8930	PP	OMIT P4MM
89 87	FB_A_WDQS<4>	PP8931	PP	OMIT P4MM
89 87	FB_A_WDQS<7>	PP8932	PP	OMIT P4MM
89 87 5	FB_A_DQ<32>	PP8933	PP	OMIT P4MM
89 87 5	FB_A_DQ<40>	PP8934	PP	OMIT P4MM
89 87 5	FB_A_DQ<48>	PP8935	PP	OMIT P4MM
89 87 5	FB_A_DQ<56>	PP8936	PP	OMIT P4MM

PLACE NEAR U9000

90 87	FB_B_CKE<0>	PP9000	PP	OMIT P4MM
90 87	FB_B_CLK_P<0>	PP9001	PP	OMIT P4MM
90 87	FB_B_CLK_N<0>	PP9002	PP	OMIT P4MM
90 87	FB_B_CS_L<0>	PP9003	PP	OMIT P4MM
90 87	FB_B_WE_L<0>	PP9004	PP	OMIT P4MM
90 87	FB_B_CAS_L<0>	PP9005	PP	OMIT P4MM
90 87	FB_B_RAS_L<0>	PP9006	PP	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9007	PP	OMIT P4MM
90 89 88 5	DRAM_RST	PP9008	PP	OMIT P4MM
90 87	FB_B_WDQS<0>	PP9009	PP	OMIT P4MM
90 87	FB_B_WDQS<1>	PP9010	PP	OMIT P4MM
90 87	FB_B_WDQS<3>	PP9011	PP	OMIT P4MM
90 87	FB_B_WDQS<2>	PP9012	PP	OMIT P4MM
90 87 5	FB_B_DQ<0>	PP9013	PP	OMIT P4MM
90 87 5	FB_B_DQ<8>	PP9014	PP	OMIT P4MM
90 87 5	FB_B_DQ<16>	PP9015	PP	OMIT P4MM
90 87 5	FB_B_DQ<24>	PP9016	PP	OMIT P4MM

PLACE NEAR U9050

90 87	FB_B_CKE<1>	PP9020	PP	OMIT P4MM
90 87	FB_B_CLK_P<1>	PP9021	PP	OMIT P4MM
90 87	FB_B_CLK_N<1>	PP9022	PP	OMIT P4MM
90 87	FB_B_CS_L<1>	PP9023	PP	OMIT P4MM
90 87	FB_B_WE_L<1>	PP9024	PP	OMIT P4MM
90 87	FB_B_CAS_L<1>	PP9025	PP	OMIT P4MM
90 87	FB_B_RAS_L<1>	PP9026	PP	OMIT P4MM
90 87 5	FB_B_MA<3>	PP9027	PP	OMIT P4MM
90 89 88 5	DRAM_RST	PP9028	PP	OMIT P4MM
90 87	FB_B_WDQS<5>	PP9029	PP	OMIT P4MM
90 87	FB_B_WDQS<6>	PP9030	PP	OMIT P4MM
90 87	FB_B_WDQS<7>	PP9031	PP	OMIT P4MM
90 87	FB_B_WDQS<4>	PP9032	PP	OMIT P4MM
90 87 5	FB_B_DQ<32>	PP9033	PP	OMIT P4MM
90 87 5	FB_B_DQ<40>	PP9034	PP	OMIT P4MM
90 87 5	FB_B_DQ<48>	PP9035	PP	OMIT P4MM
90 87 5	FB_B_DQ<56>	PP9036	PP	OMIT P4MM

PLACE NEAR R1210 AND R1211

12	NB_FSB_VREF	PP1200	1 A SM-TP50-TOP
19 12 6	=PP1V05_S0_FSB_NB	PP1201	1 A SM-TP50-TOP
		PP1202	1 A SM-TP50-TOP

PLACE NEAR R0705 AND R0706

59 11 9 8 7 6	=PP1V05_S0_CPU	PP700	1 A SM-TP50-TOP
7	CPU_GTLREF	PP701	1 A SM-TP50-TOP
		PP702	1 A SM-TP50-TOP

PLACE NEAR R2800 AND R2801

29 28 6	=PP1V8_S3_MEM	PP2800	1 A SM-TP50-TOP
29 28	MEM_VREF	PP2801	1 A SM-TP50-TOP
		PP2802	1 A SM-TP50-TOP

34	TP_PCI_CLK_SPARE	NO_TEST=TRUE	
29	TP_MEM_B_A<14>	NO_TEST=TRUE	
29	TP_MEM_B_A<15>	NO_TEST=TRUE	

79 77 76 66 65 59 26 6 83 81 80	PP3V3_S5	FUNC_TEST=TRUE	
83 81 80 79 59 6	PP5V_S5	FUNC_TEST=TRUE	
88 83 81 80 79 78 6	PP12V_S5	FUNC_TEST=TRUE	
79 6	PP1V8_S3	FUNC_TEST=TRUE	
76 75 6	PPVCORE_CPU	FUNC_TEST=TRUE	
26 25 24 21	PP3V3_S5_S0_RTC	FUNC_TEST=TRUE	
	8 TESTPOINTS	FUNC_TEST=TRUE	

60 59 58	SMC_TCK	FUNC_TEST=TRUE	
60 59 58	SMC_TDI	FUNC_TEST=TRUE	
60 59 58	SMC_TDO	FUNC_TEST=TRUE	
60 59 58	SMC_TMS	FUNC_TEST=TRUE	
60 58	SMC_TRST_L	FUNC_TEST=TRUE	
60 59 58	SMC_TX_L	FUNC_TEST=TRUE	
60 59 58	SMC_RX_L	FUNC_TEST=TRUE	
59	SMC_MANUAL_RST_L	FUNC_TEST=TRUE	
59 11 7	XDP_TCK	FUNC_TEST=TRUE	
59 11 7	XDP_TDI	FUNC_TEST=TRUE	
59 11 7	XDP_TDO	FUNC_TEST=TRUE	
59 11 7	XDP_TMS	FUNC_TEST=TRUE	
59 11 7	XDP_TRST_L	FUNC_TEST=TRUE	
59	POWER_BUTTON_L	FUNC_TEST=TRUE	
26	SW_RST_BTN_L	FUNC_TEST=TRUE	

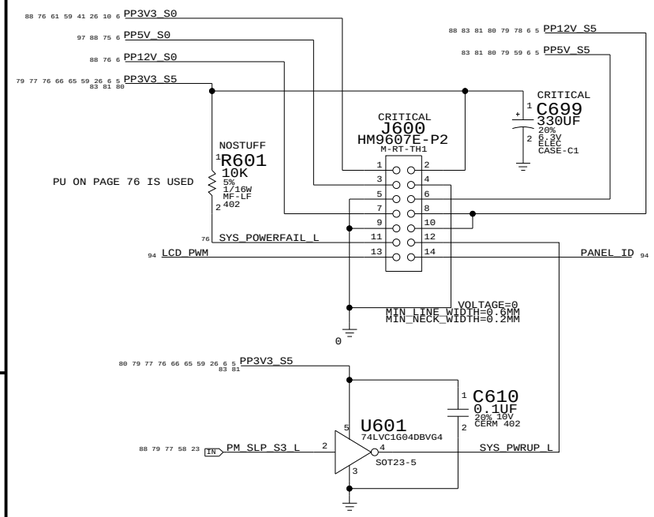
MISC GROUND VIAS

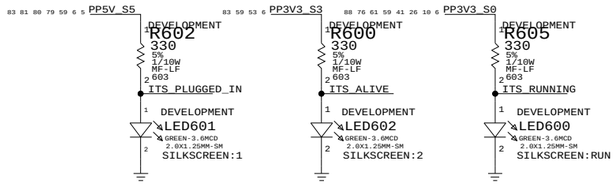
ZH500 HOLE-VIA	ZH510 HOLE-VIA	ZH520 HOLE-VIA
ZH501 HOLE-VIA	ZH511 HOLE-VIA	ZH521 HOLE-VIA
ZH502 HOLE-VIA	ZH512 HOLE-VIA	ZH522 HOLE-VIA
ZH503 HOLE-VIA	ZH513 HOLE-VIA	ZH523 HOLE-VIA
ZH504 HOLE-VIA	ZH514 HOLE-VIA	ZH524 HOLE-VIA
ZH505 HOLE-VIA	ZH515 HOLE-VIA	ZH525 HOLE-VIA
ZH506 HOLE-VIA	ZH516 HOLE-VIA	ZH526 HOLE-VIA
ZH507 HOLE-VIA	ZH517 HOLE-VIA	ZH527 HOLE-VIA
ZH508 HOLE-VIA	ZH518 HOLE-VIA	ZH528 HOLE-VIA
ZH509 HOLE-VIA	ZH519 HOLE-VIA	ZH529 HOLE-VIA

FUNC TEST 1 OF 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 5 OF 111	





"S0" RAILS

ONLY ON IN RUN

- PP0V9_S0 (MAKE_BASE=TRUE, VOLTAGE=0.9V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM)
  - =PP0V9_S0_MEMVTT_LDO (31)
  - =PP0V9_S0_MEM_TERM (30)
- PPVCORE_CPU (MAKE_BASE=TRUE, VOLTAGE=1.25V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
  - =PPVCORE_S0_CPU (8 9 76)
- PP1V05_S0 (MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.15MM)
  - =PPVCORE_S0_NB (16 19)
  - =PP1V05_S0_CPU (5 7 8 9 11 59)
  - =PP1V05_S0_FSB_NB (5 12 19)
  - =PP1V05_S0_NB_VTT (17 19)
  - =PP1V05_S0_NB (19)
  - =PP1V05_S0_SB_CPU_IO (21 24 25)
  - =PPVCORE_S0_SB (24 25)
- PP1V5_S0 (MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
  - =PP1V5_S0_CPU (8)
  - =PP1V5_S0_NB_PCIE (13 19)
  - =PP1V5_S0_NB_VCCAUX (6 16 17 19)
  - =PP1V5_S0_NB_VCCD_HMPLL (17 19)
  - =PP1V5_S0_NB_VCCAUX (6 16 17 19)
  - =PP1V5_S0_NB_PLL (19)
  - =PP1V5_S0_NB (19)
  - =PP1V5_S0_NB_TVDAC (19)
  - =PP1V5_S0_NB_3GPLL (19)
  - =PP1V5_S0_SB_VCC1_5_A_ARX (24 25)
  - =PP1V5_S0_SB_VCCSATAPLL (24 25)
  - =PP1V5_S0_SB_VCC1_5_A_ATX (24 25)
  - =PP1V5_S0_SB_VCCUSBPLL (24 25)
  - =PP1V5_S0_SB_VCC1_5_A_USB_CORE (24 25)
  - =PP1V5_S0_SB_VCC1_5_A (24 25)
  - =PP1V5_S0_SB (25)
  - =PP1V5_S0_AIRPORT (53)
- PP2V5_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
  - =PP2V5_S0_NB_VCCA_3GBG (17 19)
- PP3V3_S0 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
  - =PP3V3_S0_NB_PM
  - =PP3V3_S0_NB_VCC_HV (17 19)
  - =PP3V3_S0_NB_TVDAC (19)
  - =PP3V3_S0_SB (22 25)
  - =PP3V3_S0_SB_GPIO (21 23)
  - =PP3V3_S0_SB_VCC3_3 (24 25)
  - =PP3V3_S0_SB_VCC3_3_PCI (24 25)
  - =PP3V3_S0_SB_VCC3_3_IDE (24 25)
  - =PP3V3_S0_SB_PCI (26)
  - =PP3V3_S0_SB_PM (26)
  - =PP3V3_S0_PATA (38)
  - =PP3V3_S0_FAN (59 65 66)
  - =PP3V3_S0_HD_TSENS (66)
  - =PP3V3_S0_ODD_TSENS (66)
  - =PP3V3_S0_SB_3V3_1V5_VCCHDA (24 25)
  - =PP3V3_S0_TPM (67)
  - =PPSPD_S0_MEM (28 29)
  - =PP3V3_S0_CK410 (33 34)
  - =PP3V3_S0_IMVP (75)
  - =PP3V3_S0_AUDIO (68 72 73 74)
  - =PP3V3_S0_PCI (44)
  - =PP3V3_S0_SB_VCCLAN3_3 (24 25)
  - =PP3V3_S0_AIRPORT (53)
  - =PP3V3_S0_2V5REG (77)
  - =PP3V3_S0_NB (14 19 20)
- PP5V_S0 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
  - =PP5V_S0_SB (25)
  - =PP5V_S0_PATA (38)
  - XW604 SM OMIT: PP5V_S0_AUDIO (MAKE_BASE=TRUE) =PP5V_S0_AUDIO (68)
  - =PP5V_S0_DEBUG (60)
- PP12V_S0 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.15MM)
  - =PP12V_S0_FAN (65 66)
  - XW605 SM OMIT: PP12V_S0_AUDIO_SPKRAMP (MAKE_BASE=TRUE) =PP12V_S0_AUDIO_SPKRAMP (72)

"S3" RAILS

ON IN RUN AND SLEEP

- PP1V2_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
  - =PP1V2_S3_LAN (42)
- PP1V8_S3 (MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
  - =PP1V8_S3_MEM_NB (6 14 16 19)
  - =PP1V8_S3_MEM_NB (6 14 16 19)
  - =PP1V8_S3_MEM (5 28 29)
  - =PP1V8_S0_MEMVTT (31)
- PP3V3_S3 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
  - =PP3V3_S3_ENET (41 42 43)
  - =PP3V3_S3_TPM (67)
  - =PP3V3_S3_1V2REG (77)
  - =PP3V3_S3_BT (47)
  - =PP3V3_S3_USB (49)
  - =PP3V3_S3_VGASYNC (97)
- PP5V_S3 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
  - =PP5V_S3_USB (47)
  - =PP5V_S3_BNDI (47)
  - =PP5V_S0_MEMVTT (31)

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

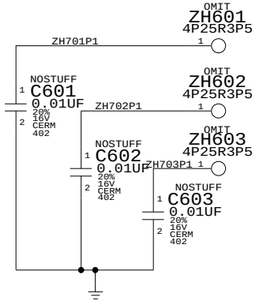
- PP3V3_S5 (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
  - =PP3V3_S5_SB (23 25 26)
  - =PP3V3_S5_SB_USB (22)
  - =PP3V3_S5_SB_PM (11 23)
  - =PP3V3_S5_SB_VCCSUS3_3 (24 25)
  - =PP3V3_S5_SB_VCCSUS3_3_USB (24 25)
  - =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA (24)
  - =PP3V3_S5_SB_IO (22 27)
  - =PP3V3_S5_FW (44 45 46)
  - =PP3V3_S5_SMC (58 59)
  - =PP3V3_S5_DEBUG (60)
  - =PP3V3_S5_ROM (63)
- PP5V_S5 (MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
  - =PP5V_S5_SB (25)
- PP12V_S5 (MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
  - =PP12V_S5_FW (46)
  - =PP12V_S5_CPU (76)

GND RAILS

- XW601 SM NOSTUFF: GND_AUDIO (74)
- XW602 SM NOSTUFF: GND_AUDIO_SPKRAMP (74 72)

CHASSIS GND

- NOSTUFF R603 0 5% 1/10W MF-LF 402
  - GND_CHASSIS_IO_LEFT (MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
  - GND_CHASSIS_AUDIO_EXTERNAL (74 73)
  - GND_CHASSIS_USB (47)
- GND_CHASSIS_FIREWIRE (46)
- GND_CHASSIS_VGA (97)
- GND_CHASSIS_RJ45 (43)
- GND_CHASSIS_IO_RIGHT (MAKE_BASE=TRUE, VOLTAGE=0, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM)
- GND_CHASSIS_AUDIO_INTERNAL (73)
- OMIT ZH606 160R138
- GND_CHASSIS_BNDI (47) (MIN_NECK_WIDTH=0.2MM, MIN_LINE_WIDTH=0.6MM, VOLTAGE=0, MAKE_BASE=TRUE)



Power Conn / Alias

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6950	06
SCALE: NONE	SHT 6 OF 111	

OMIT

J0700
YONAH-SKT
CPU
BGA
(1 OF 4)

ADDR GROUP0

FSB_A_L<3>	J4	A3*
FSB_A_L<4>	L4	A4*
FSB_A_L<5>	M3	A5*
FSB_A_L<6>	K5	A6*
FSB_A_L<7>	M1	A7*
FSB_A_L<8>	N2	A8*
FSB_A_L<9>	J1	A9*
FSB_A_L<10>	N3	A10*
FSB_A_L<11>	P5	A11*
FSB_A_L<12>	P2	A12*
FSB_A_L<13>	L1	A13*
FSB_A_L<14>	P4	A14*
FSB_A_L<15>	P1	A15*
FSB_A_L<16>	R1	A16*
FSB_ADSTB_L<0>	L2	ADSTB0*

ADDR GROUP1

FSB_A_L<17>	Y2	A17*
FSB_A_L<18>	U5	A18*
FSB_A_L<19>	R3	A19*
FSB_A_L<20>	W6	A20*
FSB_A_L<21>	U4	A21*
FSB_A_L<22>	Y5	A22*
FSB_A_L<23>	U2	A23*
FSB_A_L<24>	R4	A24*
FSB_A_L<25>	T5	A25*
FSB_A_L<26>	T3	A26*
FSB_A_L<27>	W3	A27*
FSB_A_L<28>	W5	A28*
FSB_A_L<29>	Y4	A29*
FSB_A_L<30>	W2	A30*
FSB_A_L<31>	Y1	A31*
FSB_ADSTB_L<1>	V4	ADSTB1*

CPU_A20M_L	A6	A20M*
CPU_FERR_L	A5	FERR*
CPU_IGNNE_L	C4	IGNNE*
CPU_STPCLK_L	D5	STPCLK*
CPU_INTR	C6	LINT0
CPU_NMI	B4	LINT1
CPU_SMI_L	A3	SMI*

RESERVED

TP_CPU_A32_L	AA1	RSVD1
TP_CPU_A33_L	AA4	RSVD2
TP_CPU_A34_L	AB2	RSVD3
TP_CPU_A35_L	AA3	RSVD4
TP_CPU_A36_L	M4	RSVD5
TP_CPU_A37_L	N5	RSVD6
TP_CPU_A38_L	T2	RSVD7
TP_CPU_A39_L	V3	RSVD8
TP_CPU_APM0_L	B2	RSVD9
TP_CPU_APM1_L	C3	RSVD10
TP_CPU_HFPLL	B25	RSVD11
	T22	RSVD12 — TP_CPU_EXTBREF
	D2	RSVD13 — TP_CPU_SPARE0
	F6	RSVD14 — TP_CPU_SPARE1
	D3	RSVD15 — TP_CPU_SPARE2
	C1	RSVD16 — TP_CPU_SPARE3
	AF1	RSVD17 — TP_CPU_SPARE4
	D22	RSVD18 — TP_CPU_SPARE5
	C23	RSVD19 — TP_CPU_SPARE6
	C24	RSVD20 — TP_CPU_SPARE7

CONTROL

ADS*	H1	FSB_ADS_L
BNR*	E2	FSB_BNR_L
BPRI*	G5	FSB_BPRI_L
DEFER*	H5	FSB_DEFER_L
DRDY*	F21	FSB_DRDY_L
DBSY*	E1	FSB_DBSY_L
BR0*	F1	FSB_BREQ0_L
IERR*	D20	FSB_IERR_L
INIT*	B3	CPU_INIT_L
LOCK*	H4	FSB_LOCK_L
RESET*	B1	FSB_CPURST_L
RS0*	F3	FSB_RS_L<0>
RS1*	F4	FSB_RS_L<1>
RS2*	G3	FSB_RS_L<2>
TRDY*	G2	FSB_TRDY_L
HIT*	G6	FSB_HIT_L
HITM*	E4	FSB_HITM_L

XDP/ITP SIGNALS

BPM0*	AD4	XDP_BPM_L<0>
BPM1*	AD3	XDP_BPM_L<1>
BPM2*	AD1	XDP_BPM_L<2>
BPM3*	AC4	XDP_BPM_L<3>
PRDY*	AC2	XDP_BPM_L<4>
PREQ*	AC1	XDP_BPM_L<5>
TCK	AC5	XDP_TCK
TDI	AA6	XDP_TDI
TDO	AB3	XDP_TDO
TMS	AB5	XDP_TMS
TRST*	AB6	XDP_TRST_L
DBR*	C20	XDP_DBRESET_L

NOTE: DUMMY PIN
PIN ACTUALLY DRIVEN BY ITP

THERM

PROCHOT*	D21	CPU_PROCHOT_L
THERMDA	A24	CPU_THERMD_P
THERMDC	A25	CPU_THERMD_N
THERMTRIP*	C7	PM_THRMTRIP_L

HCLK

BCLK0	A22	FSB_CLK_CPU_P
BCLK1	A21	FSB_CLK_CPU_N

=PP1V05_S0_CPU

R0702 54.9 1% 1/16W MF-LF 402

CPU SCH AND PCB SYMBOL NEED TO CHECK

PLACE TESTPOINT ON FSB_IERR# WITH A GND 0.1" AWAY

=PP1V05_S0_CPU

NOSTUFF R0703 54.9 1% 1/16W MF-LF 402

R0704 68 5% 1/16W MF-LF 402

NO SPACE FOR ITP CONNECTOR, NEED TERM ON ITP SIGNALS?

CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT

PM_THRMTRIP# SHOULD CONNECT TO ICH6-M AND GMCH WITHOUT T-ING (NO STUB)

SPARE[7-0],HFPLL: ROUTE TO TP VIA AND PLACE GND VIA W/IN 1000 MILS

=PP1V05_S0_CPU

R0720 54.9 1% 1/16W MF-LF 402 — XDP_TMS

R0721 54.9 1% 1/16W MF-LF 402 — XDP_TDI

R0722 54.9 1% 1/16W MF-LF 402 — XDP_TCK

OMIT

J0700
YONAH-SKT
CPU
BGA
(2 OF 4)

DATA GRP0

FSB_D_L<0>	E22	D0*
FSB_D_L<1>	F24	D1*
FSB_D_L<2>	E26	D2*
FSB_D_L<3>	H22	D3*
FSB_D_L<4>	F23	D4*
FSB_D_L<5>	G25	D5*
FSB_D_L<6>	E25	D6*
FSB_D_L<7>	E23	D7*
FSB_D_L<8>	K24	D8*
FSB_D_L<9>	G24	D9*
FSB_D_L<10>	J24	D10*
FSB_D_L<11>	J23	D11*
FSB_D_L<12>	H26	D12*
FSB_D_L<13>	F26	D13*
FSB_D_L<14>	K22	D14*
FSB_D_L<15>	H25	D15*
FSB_DSTBN_L<0>	H23	DSTBN0*
FSB_DSTBP_L<0>	G22	DSTBP0*
FSB_DINV_L<0>	J26	DINV0*

DATA GRP1

FSB_D_L<16>	N22	D16*
FSB_D_L<17>	K25	D17*
FSB_D_L<18>	P26	D18*
FSB_D_L<19>	R23	D19*
FSB_D_L<20>	L25	D20*
FSB_D_L<21>	L22	D21*
FSB_D_L<22>	L23	D22*
FSB_D_L<23>	M23	D23*
FSB_D_L<24>	P25	D24*
FSB_D_L<25>	P22	D25*
FSB_D_L<26>	P23	D26*
FSB_D_L<27>	T24	D27*
FSB_D_L<28>	R24	D28*
FSB_D_L<29>	L26	D29*
FSB_D_L<30>	T25	D30*
FSB_D_L<31>	N24	D31*
FSB_DSTBN_L<1>	M24	DSTBN1*
FSB_DSTBP_L<1>	N25	DSTBP1*
FSB_DINV_L<1>	M26	DINV1*

DATA GRP2

D32*	AA23	FSB_D_L<32>
D33*	AB24	FSB_D_L<33>
D34*	V24	FSB_D_L<34>
D35*	V26	FSB_D_L<35>
D36*	W25	FSB_D_L<36>
D37*	U23	FSB_D_L<37>
D38*	U25	FSB_D_L<38>
D39*	U22	FSB_D_L<39>
D40*	AB25	FSB_D_L<40>
D41*	W22	FSB_D_L<41>
D42*	Y23	FSB_D_L<42>
D43*	AA26	FSB_D_L<43>
D44*	Y26	FSB_D_L<44>
D45*	Y22	FSB_D_L<45>
D46*	AC26	FSB_D_L<46>
D47*	AA24	FSB_D_L<47>
DSTBN2*	W24	FSB_DSTBN_L<2>
DSTBP2*	Y25	FSB_DSTBP_L<2>
DINV2*	V23	FSB_DINV_L<2>

DATA GRP3

D48*	AC22	FSB_D_L<48>
D49*	AC23	FSB_D_L<49>
D50*	AB22	FSB_D_L<50>
D51*	AA21	FSB_D_L<51>
D52*	AB21	FSB_D_L<52>
D53*	AC25	FSB_D_L<53>
D54*	AD20	FSB_D_L<54>
D55*	AE22	FSB_D_L<55>
D56*	AF23	FSB_D_L<56>
D57*	AD24	FSB_D_L<57>
D58*	AE21	FSB_D_L<58>
D59*	AD21	FSB_D_L<59>
D60*	AE25	FSB_D_L<60>
D61*	AF25	FSB_D_L<61>
D62*	AF22	FSB_D_L<62>
D63*	AF26	FSB_D_L<63>
DSTBN3*	AD23	FSB_DSTBN_L<3>
DSTBP3*	AE24	FSB_DSTBP_L<3>
DINV3*	AC20	FSB_DINV_L<3>

MISC

COMP0	R26	CPU_COMP<0>
COMP1	U26	CPU_COMP<1>
COMP2	U1	CPU_COMP<2>
COMP3	V1	CPU_COMP<3>
DPRSTP*	E5	CPU_DPRSTP_L
DPSLP*	B5	CPU_DPSLP_L
DPWR*	D24	FSB_DPWR_L
PWRGOOD	D6	CPU_PWRGD
SLP*	D7	FSB_SLPCPU_L
PSI*	AE6	CPU_PSI_L

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402

=PP1V05_S0_CPU

R0705 1K 1% 1/16W MF-LF 402

R0706 2.0K 1% 1/16W MF-LF 402 — LAYOUT NOTE: 0.5" MAX LENGTH

CPU_GTLREF

CPU_TEST1

CPU_TEST2

CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

NOSTUFF R0730 0 402

R0707 51 5% 1/16W MF-LF 402

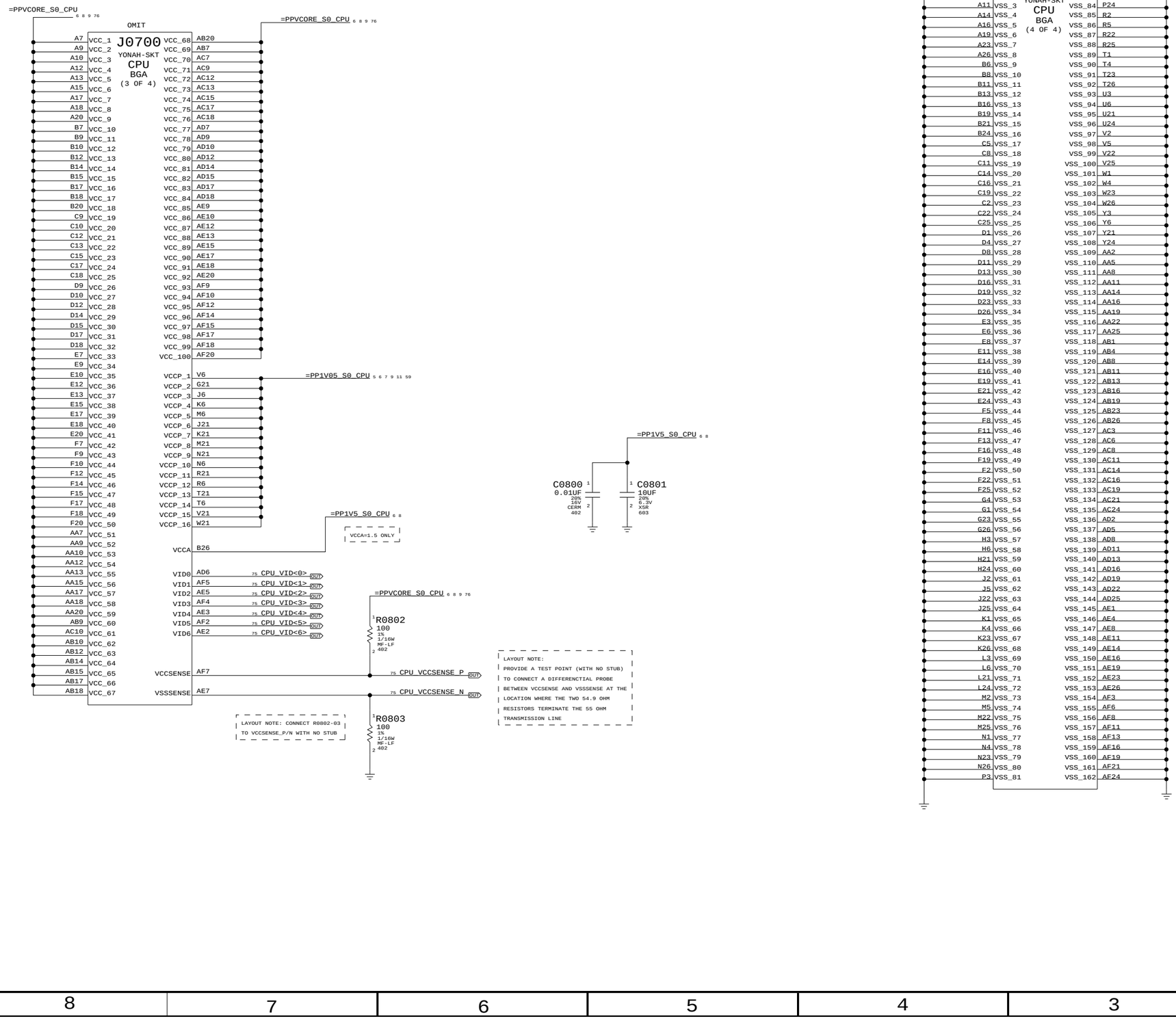
NOSTUFF R0712 1K 5% 1/16W MF-LF 402

CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 7 OF 111	



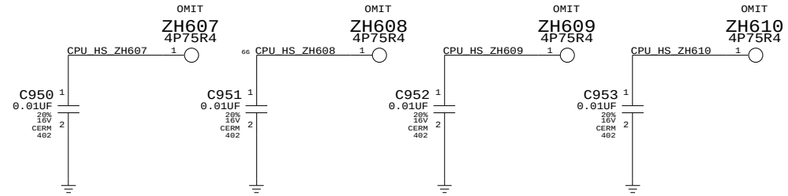
CPU 2 OF 2-PWR/GND

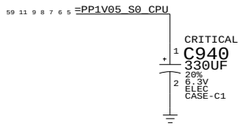
SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE COMPUTER INC.

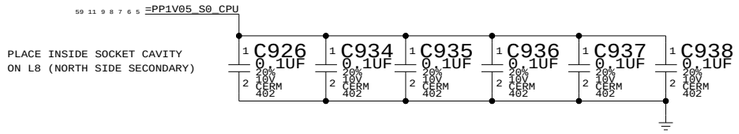
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 8 OF 111	

CPU HEATSINK MOUNTING HOLES

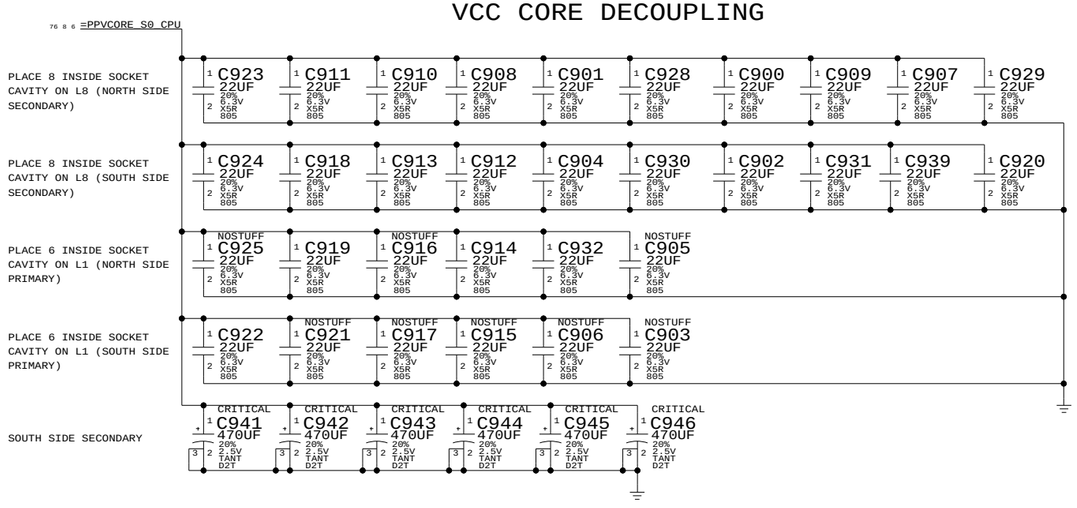




VCCP CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

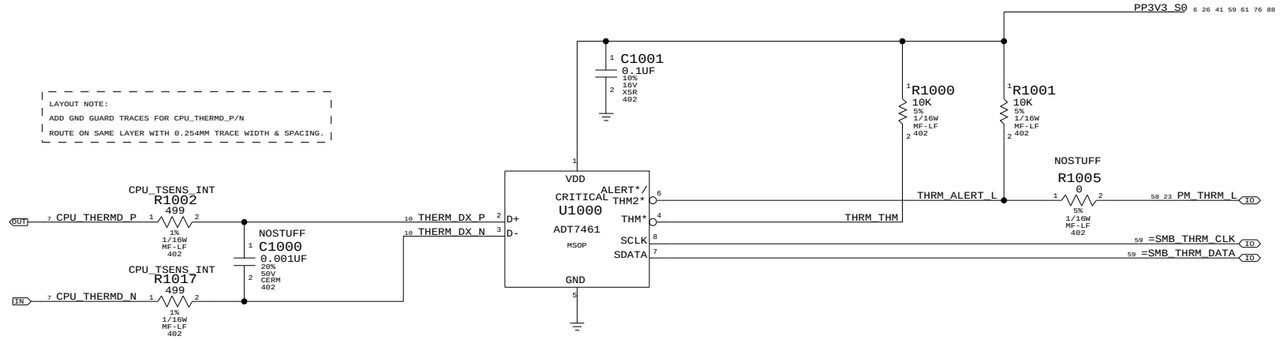
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 9 OF 111	

CPU THERMAL SENSOR

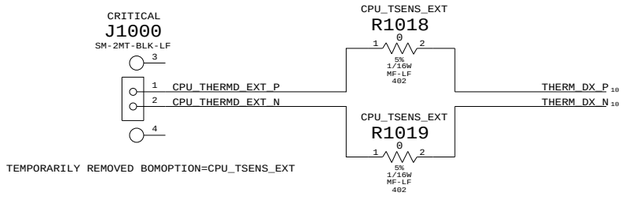
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACES FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



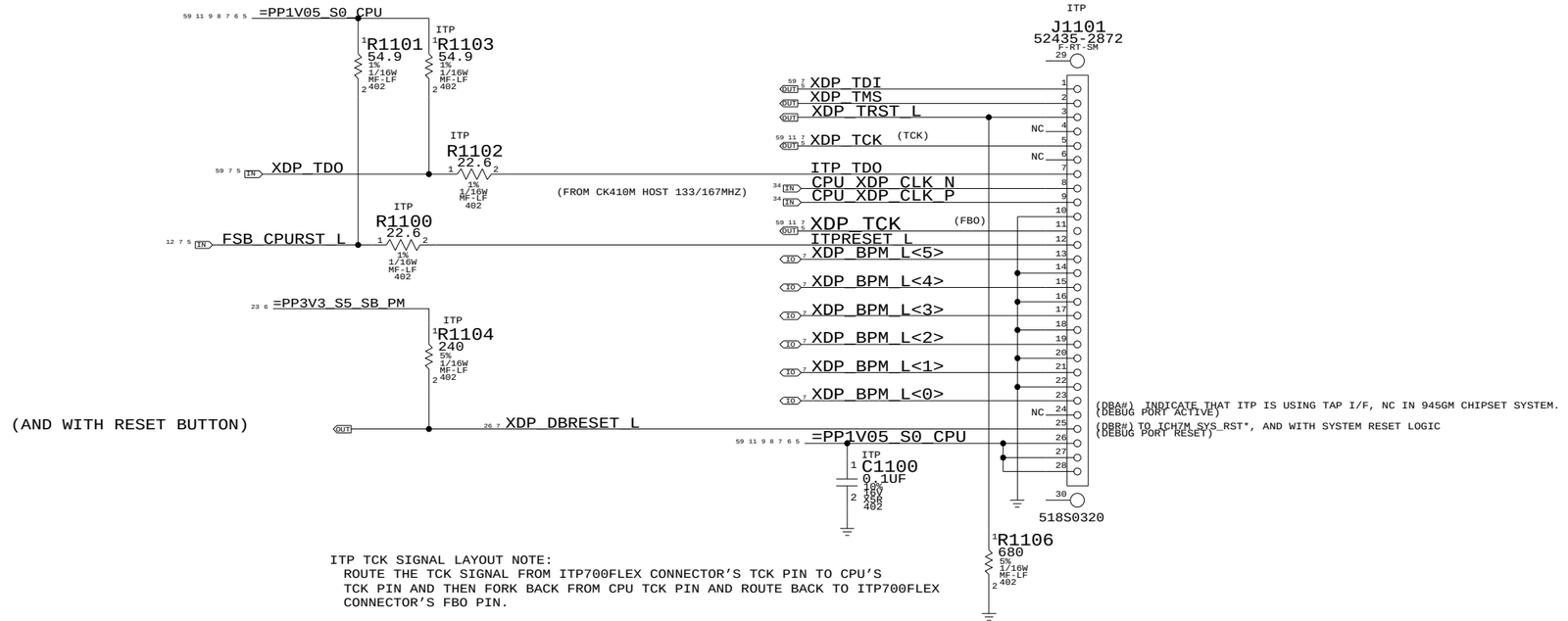
TEMPORARILY REMOVED BOMOPTION=CPU_TSENS_EXT

CPU TEMP SENSOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 10 OF 111	

CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

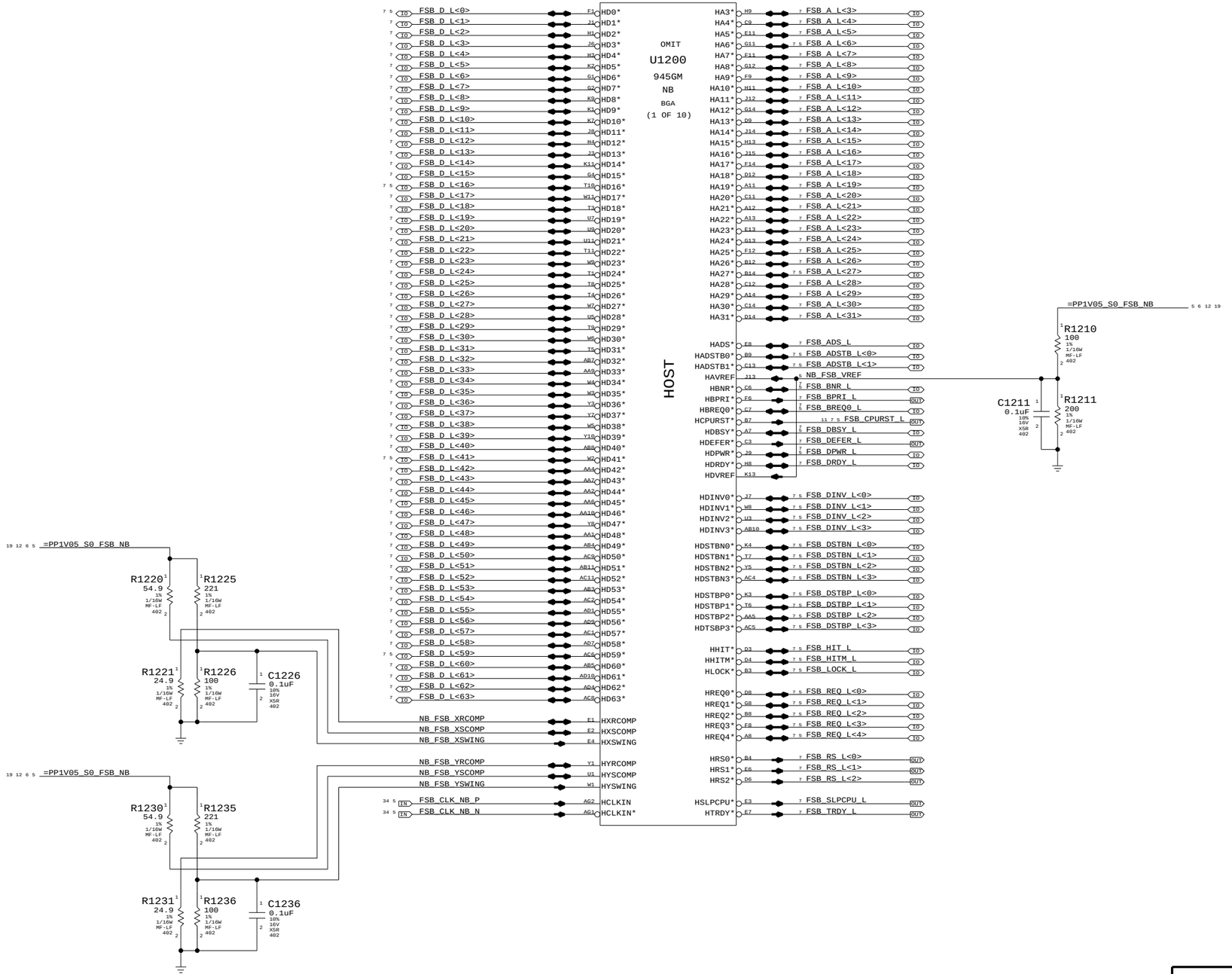
CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	11	111



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 12 OF 111	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

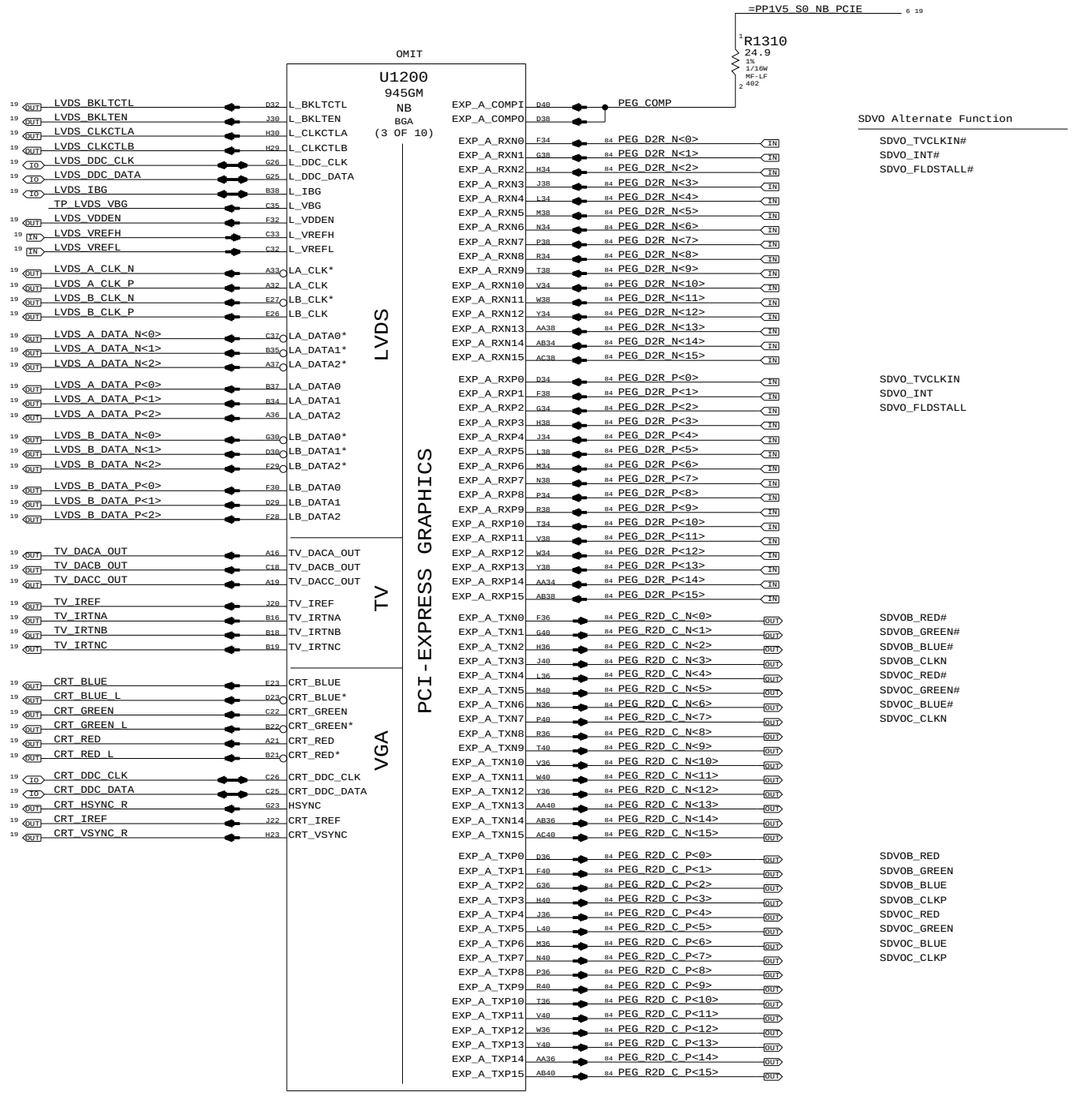
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

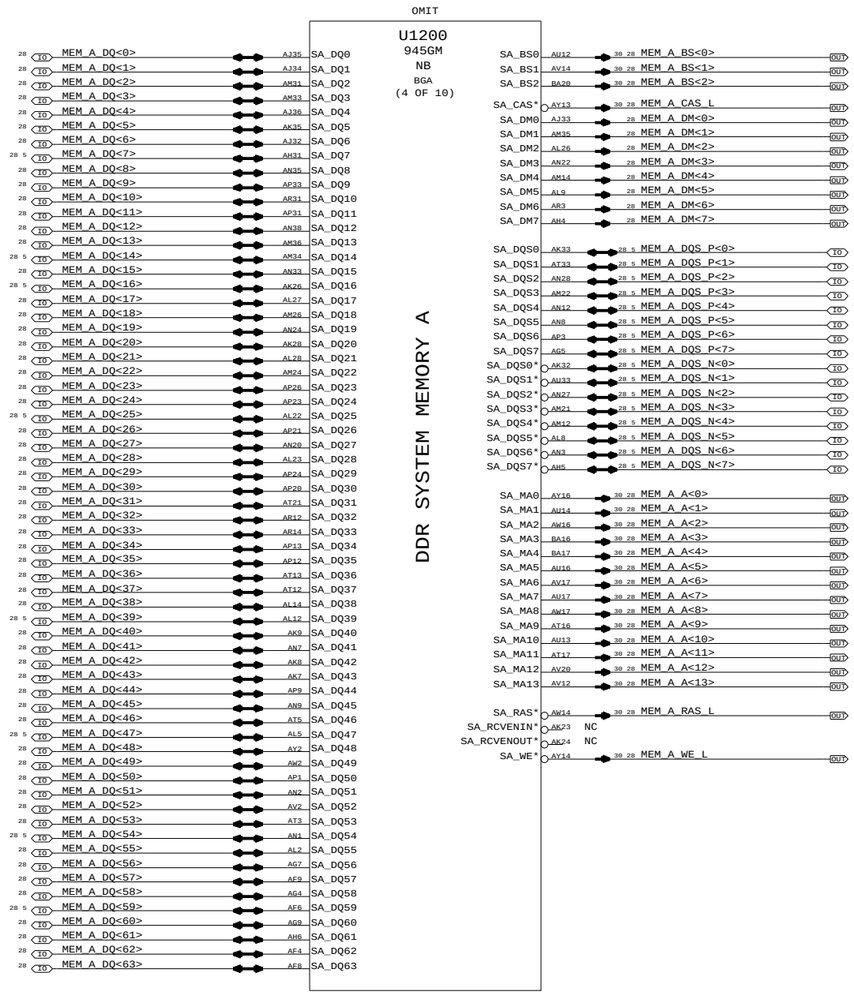
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 13 OF 111	

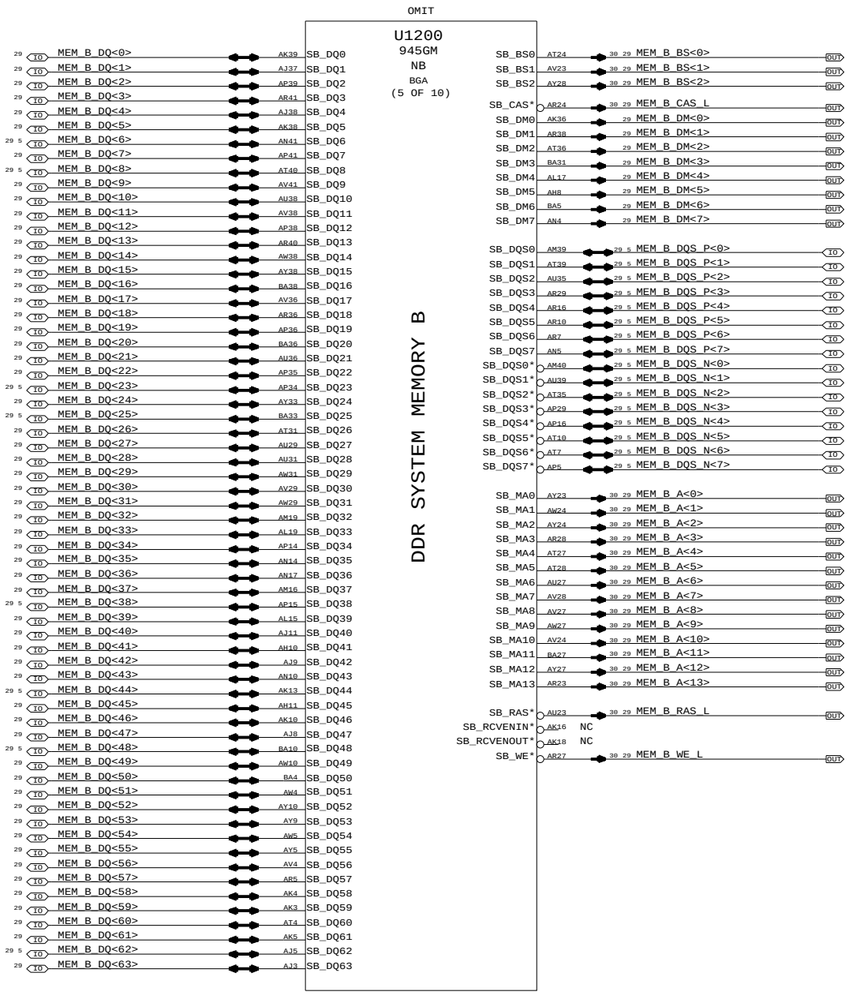
NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 14 OF 111	





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	15	111

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

=PPVCORE_S0_NB 6 16 19

1.05V or 1.5V

U1200 945GM NB BGA (6 OF 10) OMIT VCC

VCC_0	AA33	
VCC_1	AK3	
VCC_2	AP33	
VCC_3	AR3	
VCC_4	L33	
VCC_5	J33	
VCC_6	AA32	
VCC_7	Y32	
VCC_8	W32	
VCC_9	V32	
VCC_10	P32	
VCC_11	N32	
VCC_12	M32	
VCC_13	L32	
VCC_14	J32	
VCC_15	AA31	
VCC_16	W31	
VCC_17	V31	
VCC_18	T31	
VCC_19	R31	
VCC_20	P31	
VCC_21	N31	
VCC_22	K31	
VCC_23	AA30	
VCC_24	Y30	
VCC_25	W30	
VCC_26	V30	
VCC_27	U30	
VCC_28	T30	
VCC_29	R30	
VCC_30	P30	
VCC_31	N30	
VCC_32	L30	
VCC_33	AA29	
VCC_34	Y29	
VCC_35	W29	
VCC_36	V29	
VCC_37	U29	
VCC_38	P29	
VCC_39	M29	
VCC_40	L29	
VCC_41	AB28	
VCC_42	L28	
VCC_43	AA28	
VCC_44	V28	
VCC_45	U28	
VCC_46	T28	
VCC_47	R28	
VCC_48	P28	
VCC_49	N28	
VCC_50	L27	
VCC_51	M27	
VCC_52	L26	
VCC_53	P27	
VCC_54	L26	
VCC_55	M25	
VCC_56	L25	
VCC_57	P24	
VCC_58	M24	
VCC_59	L24	
VCC_60	AB23	
VCC_61	Y23	
VCC_62	P23	
VCC_63	N23	
VCC_64	L23	
VCC_65	AC22	
VCC_66	AB22	
VCC_67	Y22	
VCC_68	W22	
VCC_69	P22	
VCC_70	N22	
VCC_71	L22	
VCC_72	AC21	
VCC_73	AA21	
VCC_74	W21	
VCC_75	N21	
VCC_76	L21	
VCC_77	AC20	
VCC_78	AB20	
VCC_79	Y20	
VCC_80	W20	
VCC_81	L20	
VCC_82	AC19	
VCC_83	AA19	
VCC_84	W19	
VCC_85	N19	
VCC_86	L19	
VCC_87	AC18	
VCC_88	AB18	
VCC_89	Y18	
VCC_90	W18	
VCC_91	P18	
VCC_92	N18	
VCC_93	M18	
VCC_94	L18	
VCC_95	P17	
VCC_96	AA19	
VCC_97	Y19	
VCC_98	T19	
VCC_99	R19	
VCC_100	M19	
VCC_101	L19	
VCC_102	N18	
VCC_103	R18	
VCC_104	L18	
VCC_105	P17	
VCC_106	N17	
VCC_107	M17	
VCC_108	N16	
VCC_109	M16	
VCC_110	L16	
VCC_SM0	AU41	
VCC_SM1	AT41	
VCC_SM2	AM41	
VCC_SM3	AU40	
VCC_SM4	BA34	
VCC_SM5	AT34	
VCC_SM6	AH34	
VCC_SM7	AV34	
VCC_SM8	AU34	
VCC_SM9	AT34	
VCC_SM10	AR34	
VCC_SM11	BA30	
VCC_SM12	AY30	
VCC_SM13	AW30	
VCC_SM14	AV30	
VCC_SM15	AU30	
VCC_SM16	AT30	
VCC_SM17	AR30	
VCC_SM18	AP30	
VCC_SM19	AN30	
VCC_SM20	AM30	
VCC_SM21	AM29	
VCC_SM22	AL29	
VCC_SM23	AK29	
VCC_SM24	AJ29	
VCC_SM25	AH29	
VCC_SM26	AJ28	
VCC_SM27	AH28	
VCC_SM28	AJ27	
VCC_SM29	AH27	
VCC_SM30	BA26	
VCC_SM31	AY26	
VCC_SM32	AW26	
VCC_SM33	AV26	
VCC_SM34	AU26	
VCC_SM35	AT26	
VCC_SM36	AR26	
VCC_SM37	AJ26	
VCC_SM38	AH26	
VCC_SM39	AJ25	
VCC_SM40	AH25	
VCC_SM41	AJ24	
VCC_SM42	AH24	
VCC_SM43	BA23	
VCC_SM44	AJ23	
VCC_SM45	BA22	
VCC_SM46	AY22	
VCC_SM47	AM22	
VCC_SM48	AV22	
VCC_SM49	AU22	
VCC_SM50	AT22	
VCC_SM51	AR22	
VCC_SM52	AP22	
VCC_SM53	AK22	
VCC_SM54	AJ22	
VCC_SM55	AK21	
VCC_SM56	AK20	
VCC_SM57	BA19	
VCC_SM58	AY19	
VCC_SM59	AW19	
VCC_SM60	AV19	
VCC_SM61	AT19	
VCC_SM62	AU19	
VCC_SM63	AR19	
VCC_SM64	AP19	
VCC_SM65	AK19	
VCC_SM66	AJ19	
VCC_SM67	AJ18	
VCC_SM68	AH17	
VCC_SM69	AJ16	
VCC_SM70	AH16	
VCC_SM71	BA15	
VCC_SM72	AY15	
VCC_SM73	AW15	
VCC_SM74	AV15	
VCC_SM75	AU15	
VCC_SM76	AT15	
VCC_SM77	AR15	
VCC_SM78	AJ15	
VCC_SM79	AJ14	
VCC_SM80	AJ13	
VCC_SM81	AH13	
VCC_SM82	AK12	
VCC_SM83	AJ12	
VCC_SM84	AH12	
VCC_SM85	AG12	
VCC_SM86	AK11	
VCC_SM87	BA9	
VCC_SM88	AY9	
VCC_SM89	AW9	
VCC_SM90	AV9	
VCC_SM91	AU9	
VCC_SM92	AT9	
VCC_SM93	AR9	
VCC_SM94	AP9	
VCC_SM95	BA6	
VCC_SM96	AY6	
VCC_SM97	AW6	
VCC_SM98	AV6	
VCC_SM99	AU6	
VCC_SM100	AM6	
VCC_SM101	AP6	
VCC_SM102	AN6	
VCC_SM103	AL6	
VCC_SM104	AK6	
VCC_SM105	AJ6	
VCC_SM106	AV1	
VCC_SM107	AJ1	

NB_VCCSM_LF4

NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402

C1613 0.47uF 20% 6.3V CERM-X5R 402

C1615 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA23

19 14 6 =PP1V8_S3_MEM_NB

C1620 10uF 20% 6.3V X5R 603

C1621 10uF 20% 6.3V X5R 603

Layout Note: Place in cavity (Need to better define cavity)

C1610 0.47uF 20% 6.3V CERM-X5R 402

Layout Note: Place near pin BA15

NB_VCCSM_LF2

NB_VCCSM_LF1

C1612 0.47uF 20% 6.3V CERM-X5R 402

C1611 0.47uF 20% 6.3V CERM-X5R 402

19 16 6 =PPVCORE_S0_NB

OMIT

U1200 945GM NB BGA (7 OF 10) NCTF

VCC_NCTF0	AD27	
VCC_NCTF1	AC27	
VCC_NCTF2	AB27	
VCC_NCTF3	AA27	
VCC_NCTF4	Y27	
VCC_NCTF5	W27	
VCC_NCTF6	V27	
VCC_NCTF7	U27	
VCC_NCTF8	T27	
VCC_NCTF9	R27	
VCC_NCTF10	AD26	
VCC_NCTF11	AC26	
VCC_NCTF12	AB26	
VCC_NCTF13	AA26	
VCC_NCTF14	Y26	
VCC_NCTF15	W26	
VCC_NCTF16	V26	
VCC_NCTF17	U26	
VCC_NCTF18	T26	
VCC_NCTF19	R26	
VCC_NCTF20	AD25	
VCC_NCTF21	AC25	
VCC_NCTF22	AB25	
VCC_NCTF23	AA25	
VCC_NCTF24	Y25	
VCC_NCTF25	W25	
VCC_NCTF26	V25	
VCC_NCTF27	U25	
VCC_NCTF28	T25	
VCC_NCTF29	R25	
VCC_NCTF30	AD24	
VCC_NCTF31	AC24	
VCC_NCTF32	AB24	
VCC_NCTF33	AA24	
VCC_NCTF34	Y24	
VCC_NCTF35	W24	
VCC_NCTF36	V24	
VCC_NCTF37	U24	
VCC_NCTF38	T24	
VCC_NCTF39	R24	
VCC_NCTF40	AD23	
VCC_NCTF41	U23	
VCC_NCTF42	T23	
VCC_NCTF43	R23	
VCC_NCTF44	AD22	
VCC_NCTF45	V22	
VCC_NCTF46	U22	
VCC_NCTF47	T22	
VCC_NCTF48	R22	
VCC_NCTF49	AD21	
VCC_NCTF50	V21	
VCC_NCTF51	U21	
VCC_NCTF52	T21	
VCC_NCTF53	R21	
VCC_NCTF54	AD20	
VCC_NCTF55	V20	
VCC_NCTF56	U20	
VCC_NCTF57	T20	
VCC_NCTF58	R20	
VCC_NCTF59	AD19	
VCC_NCTF60	V19	
VCC_NCTF61	U19	
VCC_NCTF62	T19	
VCC_NCTF63	AD18	
VCC_NCTF64	AC18	
VCC_NCTF65	AB18	
VCC_NCTF66	AA18	
VCC_NCTF67	Y18	
VCC_NCTF68	W18	
VCC_NCTF69	V18	
VCC_NCTF70	U18	
VCC_NCTF71	T18	
VCC_NCTF72		
VSS_NCTF0	AE27	
VSS_NCTF1	AE26	
VSS_NCTF2	AE25	
VSS_NCTF3	AE24	
VSS_NCTF4	AE23	
VSS_NCTF5	AE22	
VSS_NCTF6	AE21	
VSS_NCTF7	AE20	
VSS_NCTF8	AE19	
VSS_NCTF9	AE18	
VSS_NCTF10	AC17	
VSS_NCTF11	Y17	
VSS_NCTF12	U17	

=PP1V5_S0_NB_VCCAUX 6 17 19

VCCAUX_NCTF0	AG27	
VCCAUX_NCTF1	AF27	
VCCAUX_NCTF2	AG26	
VCCAUX_NCTF3	AF26	
VCCAUX_NCTF4	AG25	
VCCAUX_NCTF5	AF25	
VCCAUX_NCTF6	AG24	
VCCAUX_NCTF7	AF24	
VCCAUX_NCTF8	AG23	
VCCAUX_NCTF9	AF23	
VCCAUX_NCTF10	AG22	
VCCAUX_NCTF11	AF22	
VCCAUX_NCTF12	AG21	
VCCAUX_NCTF13	AF21	
VCCAUX_NCTF14	AG20	
VCCAUX_NCTF15	AF20	
VCCAUX_NCTF16	AG19	
VCCAUX_NCTF17	AF19	
VCCAUX_NCTF18	R19	
VCCAUX_NCTF19	AG18	
VCCAUX_NCTF20	AF18	
VCCAUX_NCTF21	R18	
VCCAUX_NCTF22	AG17	
VCCAUX_NCTF23	AF17	
VCCAUX_NCTF24	AE17	
VCCAUX_NCTF25	AD17	
VCCAUX_NCTF26	AB17	
VCCAUX_NCTF27	AA17	
VCCAUX_NCTF28	W17	
VCCAUX_NCTF29	V17	
VCCAUX_NCTF30	T17	
VCCAUX_NCTF31	R17	
VCCAUX_NCTF32	AG16	
VCCAUX_NCTF33	AF16	
VCCAUX_NCTF34	AE16	
VCCAUX_NCTF35	AD16	
VCCAUX_NCTF36	AC16	
VCCAUX_NCTF37	AB16	
VCCAUX_NCTF38	AA16	
VCCAUX_NCTF39	Y16	
VCCAUX_NCTF40	W16	
VCCAUX_NCTF41	V16	
VCCAUX_NCTF42	U16	
VCCAUX_NCTF43	T16	
VCCAUX_NCTF44	R16	
VCCAUX_NCTF45	AG15	
VCCAUX_NCTF46	AF15	
VCCAUX_NCTF47	AE15	
VCCAUX_NCTF48	AD15	
VCCAUX_NCTF49	AC15	
VCCAUX_NCTF50	AB15	
VCCAUX_NCTF51	AA15	
VCCAUX_NCTF52	Y15	
VCCAUX_NCTF53	W15	
VCCAUX_NCTF54	V15	
VCCAUX_NCTF55	U15	
VCCAUX_NCTF56	T15	
VCCAUX_NCTF57	R15	

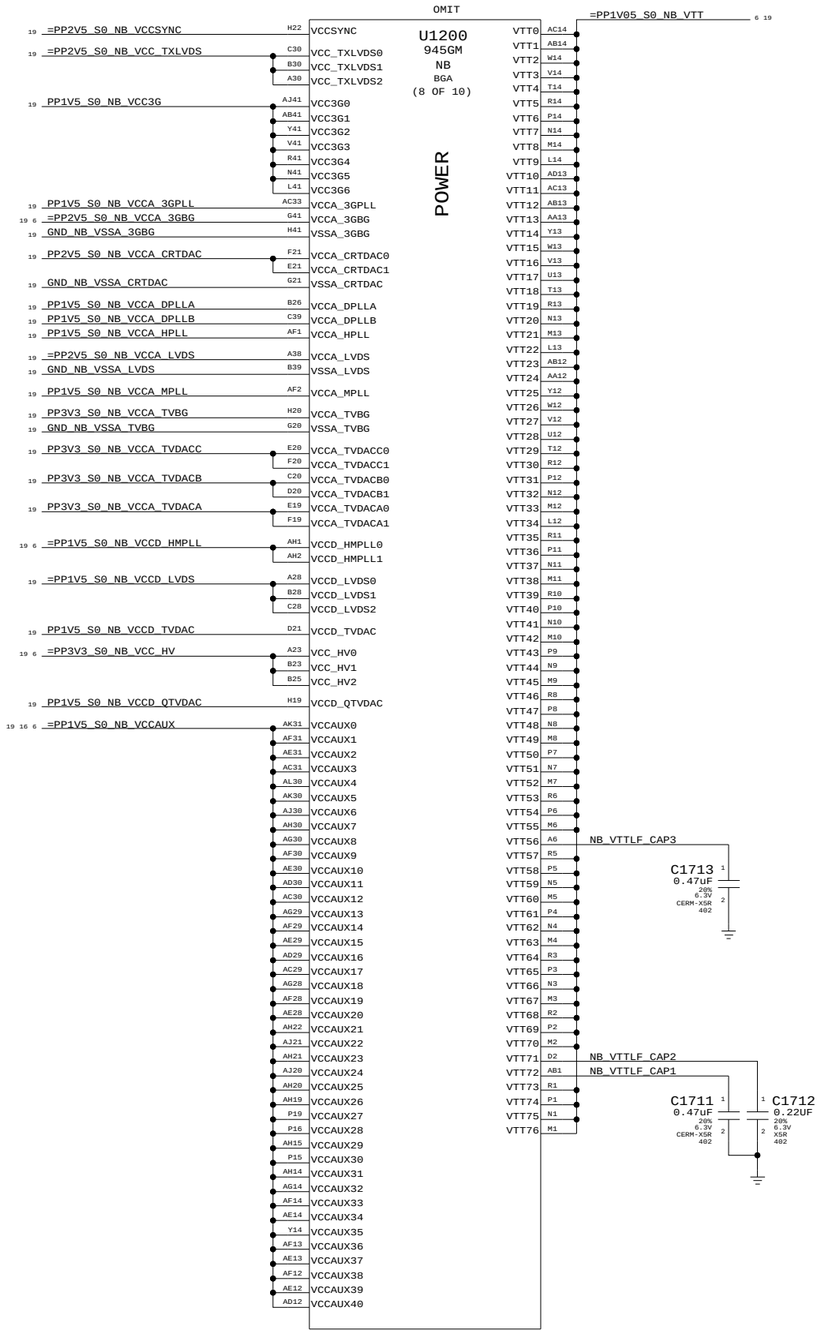
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	16	111



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	17	111

OMIT

U1200
945GM
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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

OMIT

U1200
945GM
NB
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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	18	111

Power Interface

These are the power signals that leave the NB "block"

IN =PP1V05_S0_FSB_NB — 5 6 12
IN =PPVCORE_S0_NB — 6 16 19
IN =PP1V05_S0_NB — 6
IN =PP1V05_S0_NB_VTT — 6 17 19
IN =PP1V5_S0_NB — 6 19
IN =PP1V5_S0_NB_PCIE — 6 13
IN =PP1V5_S0_NB_PLL — 6 19
IN =PP1V5_S0_NB_TVDAC — 6 19
IN =PP1V5_S0_NB_VCCD_HMPLL — 6 17
IN =PP1V5_S0_NB_VCCD_LVDS — 17 19
IN =PP1V5_S0_NB_VCCAUX — 6 16 17 19
IN =PP1V8_S3_MEM_NB — 6 14 16 19

IN =PP2V5_S0_NB_VCCSYNC — 17 19
IN =PP2V5_S0_NB_VCC_TXLVDS — 17 19
IN =PP2V5_S0_NB_VCCA_3GBG — 6 17 19
IN =PP2V5_S0_NB_VCCA_LVDS — 17 19
IN =PP3V3_S0_NB — 6 14 20
IN =PP3V3_S0_NB_TVDAC — 6
IN =PP3V3_S0_NB_VCC_HV — 6 17 19

19 6 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402

Layout Note:
These 4 0.1uF caps should
be within 5 mm of NB edge

L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402

19 17 6 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 10% 6.3V CERM1 603
Layout Note: Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
C1968 330UF 20% 6.3V ELEC CASE-C1
Layout Note: Place on the edge

19 16 14 6 =PP1V8_S3_MEM_NB
R1982 1K 5% 1/16W MF-LF 402
MEM_VREF_NB_1 — 5 14
R1983 1K 5% 1/16W MF-LF 402
C1982 0.1uF 20% 16V CERM 603
R1980 1K 5% 1/16W MF-LF 402
MEM_VREF_NB_0 — 5 14
R1981 1K 5% 1/16W MF-LF 402
C1981 0.1uF 20% 16V CERM 603

19 17 6 =PP3V3_S0_NB_VCC_HV
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

19 17 6 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

19 17 16 6 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

TVOUT DISABLE

16 6 19 =PPVCORE_S0_NB
PP2V5_S0_NB_VCCA_CRTDAC — 17
CRT_RED — 13
CRT_RED_L — 13
CRT_GREEN — 13
CRT_GREEN_L — 13
CRT_BLUE — 13
CRT_BLUE_L — 13
CRT_IREF — 13

CRT_VSYNC_R — 13
CRT_HSYNC_R — 13
=PP2V5_S0_NB_VCCSYNC — 17 19
GND_NB_VSSA_CRTDAC — 17

TP_CRT_DDC_CLK TRUE — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA TRUE — CRT_DDC_DATA — 13

DISPLAY DISABLE

TP_NB_VCCA_DPLLA TRUE — PP1V5_S0_NB_VCCA_DPLLA — 17
TP_NB_VCCA_DPLLB TRUE — PP1V5_S0_NB_VCCA_DPLLB — 17

NB_CLK_DREFCLKIN_N (IN) — 14
NB_CLK_DREFCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_P (OUT) — 14
NB_CLK_DREFSSCLKIN_N (OUT) — 14

19 16 6 =PPVCORE_S0_NB
C1900 330UF 20% 6.3V ELEC CASE-C1
C1901 330UF 20% 6.3V ELEC CASE-C1
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

19 6 =PP1V5_S0_NB_3GPLL
L1970 91NH 1210
C1970 220UF 20% 2.5V POLY SMD2
Layout Note: Place L and C close to MCH
PP1V5_S0_NB_VCC3G — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

1uH, 20%
19 6 =PP1V5_S0_NB_3GPLL
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
VOLTAGE=1.5V MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 MM
Should be 1%
R1975 0.51 1% 1/16W MF-LF 402
PP1V5_S0_NB_VCCA_3GPLL — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GND_NB_VSSA_3GBG — 17
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

LVDS DISABLE

13 (IO) LVDS_A_CLK_N — TRUE — TP_LVDS_A_CLK_N
13 (IO) LVDS_A_CLK_P — TRUE — TP_LVDS_A_CLK_P
13 (IO) LVDS_B_CLK_N — TRUE — TP_LVDS_B_CLK_N
13 (IO) LVDS_B_CLK_P — TRUE — TP_LVDS_B_CLK_P

13 (IO) LVDS_A_DATA_N<0> — TRUE — TP_LVDS_A_DATA_N<0>
13 (IO) LVDS_A_DATA_N<1> — TRUE — TP_LVDS_A_DATA_N<1>
13 (IO) LVDS_A_DATA_N<2> — TRUE — TP_LVDS_A_DATA_N<2>

13 (IO) LVDS_A_DATA_P<0> — TRUE — TP_LVDS_A_DATA_P<0>
13 (IO) LVDS_A_DATA_P<1> — TRUE — TP_LVDS_A_DATA_P<1>
13 (IO) LVDS_A_DATA_P<2> — TRUE — TP_LVDS_A_DATA_P<2>

13 (IO) LVDS_B_DATA_N<0> — TRUE — TP_LVDS_B_DATA_N<0>
13 (IO) LVDS_B_DATA_N<1> — TRUE — TP_LVDS_B_DATA_N<1>
13 (IO) LVDS_B_DATA_N<2> — TRUE — TP_LVDS_B_DATA_N<2>

13 (IO) LVDS_B_DATA_P<0> — TRUE — TP_LVDS_B_DATA_P<0>
13 (IO) LVDS_B_DATA_P<1> — TRUE — TP_LVDS_B_DATA_P<1>
13 (IO) LVDS_B_DATA_P<2> — TRUE — TP_LVDS_B_DATA_P<2>

13 (IN) LVDS_BKLTEN — TRUE — TP_LVDS_BKLTEN
13 (IN) LVDS_VDDEN — TRUE — TP_LVDS_VDDEN
13 (IN) LVDS_IBG — TRUE — TP_LVDS_IBG
17 (IN) GND_NB_VSSA_LVDS — TRUE — TP_GND_NB_VSSA_LVDS

13 (OUT) LVDS_VREFH — TRUE — TP_LVDS_VREFH
13 (OUT) LVDS_VREFL — TRUE — TP_LVDS_VREFL

19 17 =PP2V5_S0_NB_VCCA_LVDS
19 17 =PP1V5_S0_NB_VCCD_LVDS
19 17 =PP2V5_S0_NB_VCC_TXLVDS

13 (IN) LVDS_BKLTCTL — TRUE — TP_LVDS_BKLTCTL
13 (IN) LVDS_CLKCTLA — TRUE — TP_LVDS_CLKCTLA
13 (IN) LVDS_CLKCTLB — TRUE — TP_LVDS_CLKCTLB
13 (IN) LVDS_DDC_CLK — TRUE — TP_LVDS_DDC_CLK
13 (IN) LVDS_DDC_DATA — TRUE — TP_LVDS_DDC_DATA

TVOUT DISABLE

19 6 =PP1V5_S0_NB
PP3V3_S0_NB_VCCA_TVDACA — 17
PP3V3_S0_NB_VCCA_TVDACB — 17
PP3V3_S0_NB_VCCA_TVDACC — 17
PP3V3_S0_NB_VCCA_TVBG — 17
13 TV_DACA_OUT (IN)
13 TV_DACB_OUT (IN)
13 TV_DACC_OUT (IN)
13 TV_IREF (IN)
13 TV_IRTNA (IN)
13 TV_IRTNB (IN)
13 TV_IRTNC (IN)

GND_NB_VSSA_TVBG — 17

CRITICAL
C1921 22000pF-1000mA 16V NFM10
6 19 =PP1V5_S0_NB_TVDAC
PP1V5_S0_NB_VCCD_TVDAC — 17
VOLTAGE=1.5V MIN_LINE_WIDTH=1.0 mm MIN_NECK_WIDTH=0.2 MM
C1920 0.1uF 20% 10V CERM 402
PP1V5_S0_NB_VCCD_QTVDAC — 17
Layout Note: THESE 2 CAPS SHOULD BE within 6.35 mm of NB edge

14 (IN) SDVO_CTRLCLK — TP_SDVO_CTRLCLK
14 (IN) SDVO_CTRLDATA — TP_SDVO_CTRLDATA

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 19 OF 111	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

NB_CFG<12>	Internal pull-ups 00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 6 14 19 20

NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

14 NB_CFG<18>
Internal pull-down

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

=PP3V3_S0_NB 6 14 19 20

NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

14 NB_CFG<19>
Internal pull-down

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

945 External Design Spec says reserved

=PP3V3_S0_NB 6 14 19 20

NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

14 NB_CFG<20>
Internal pull-down

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

PROBABLY NOT NEEDED

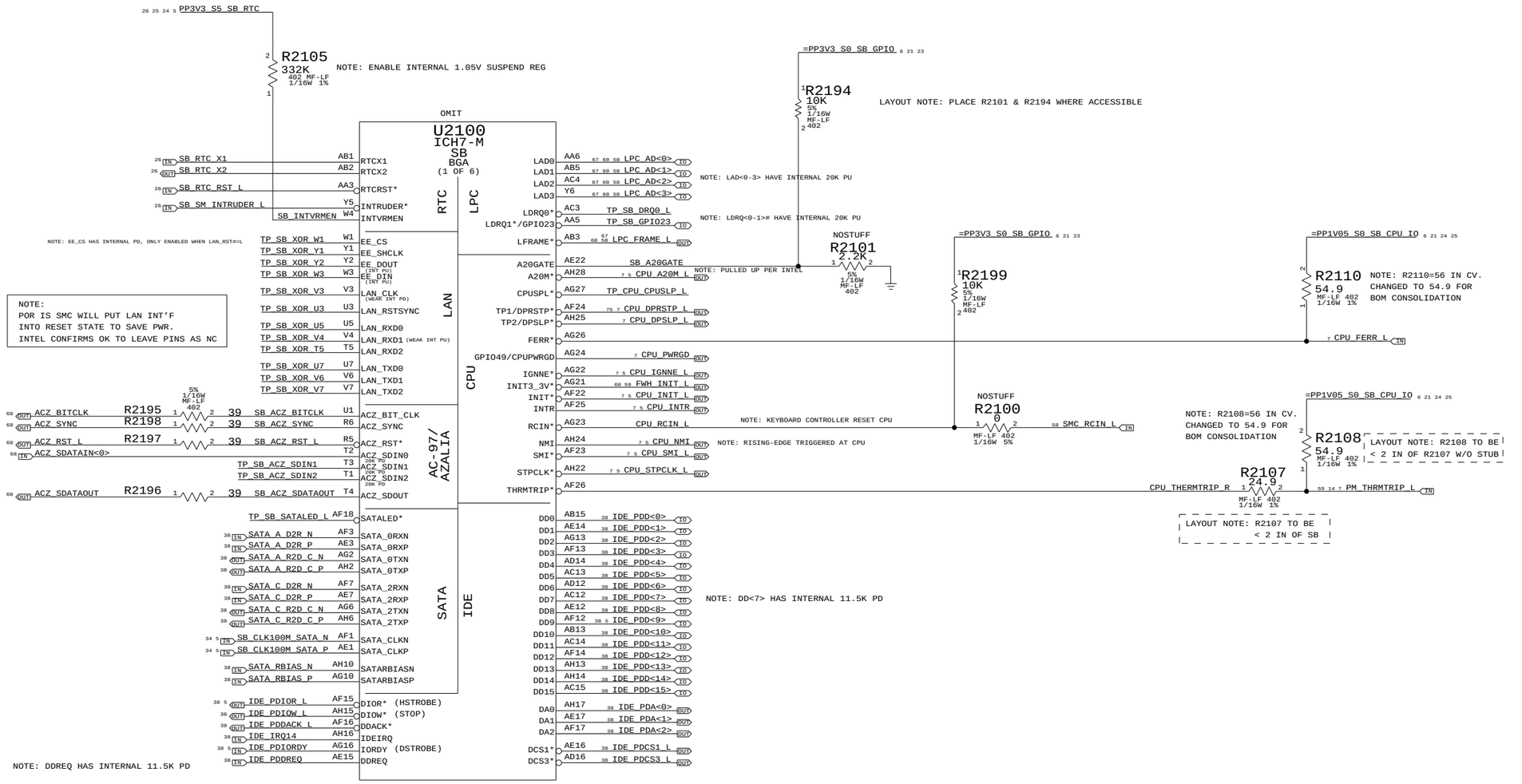
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	20	111



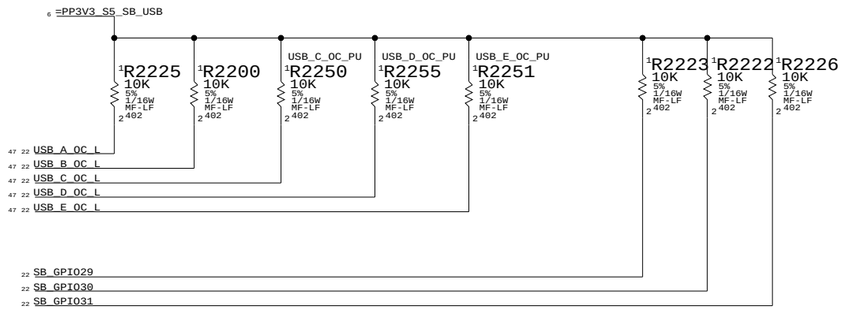
	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

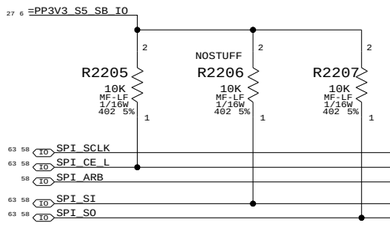
SB: 1 OF 4

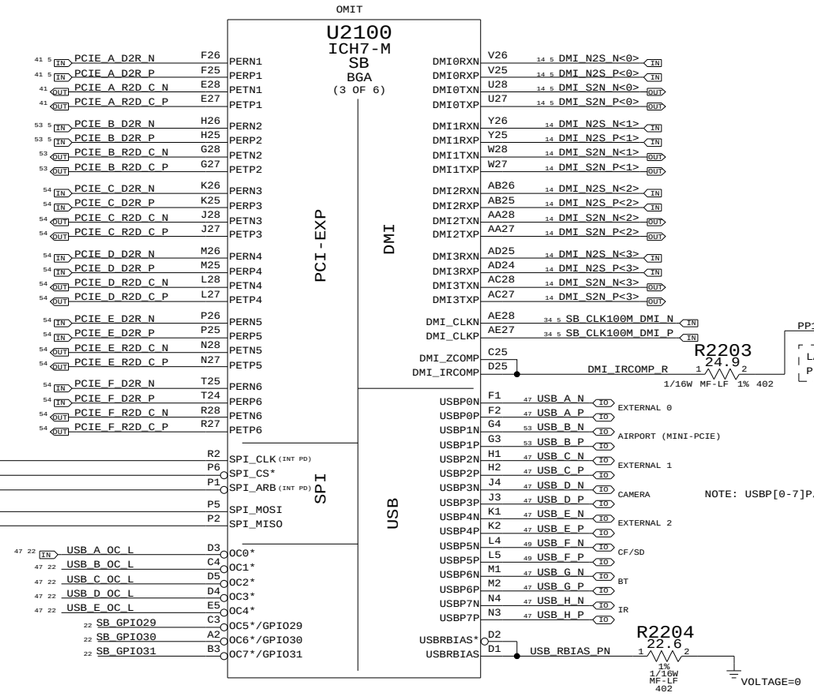
SYNC_MASTER=N/A SYNC_DATE=N/A

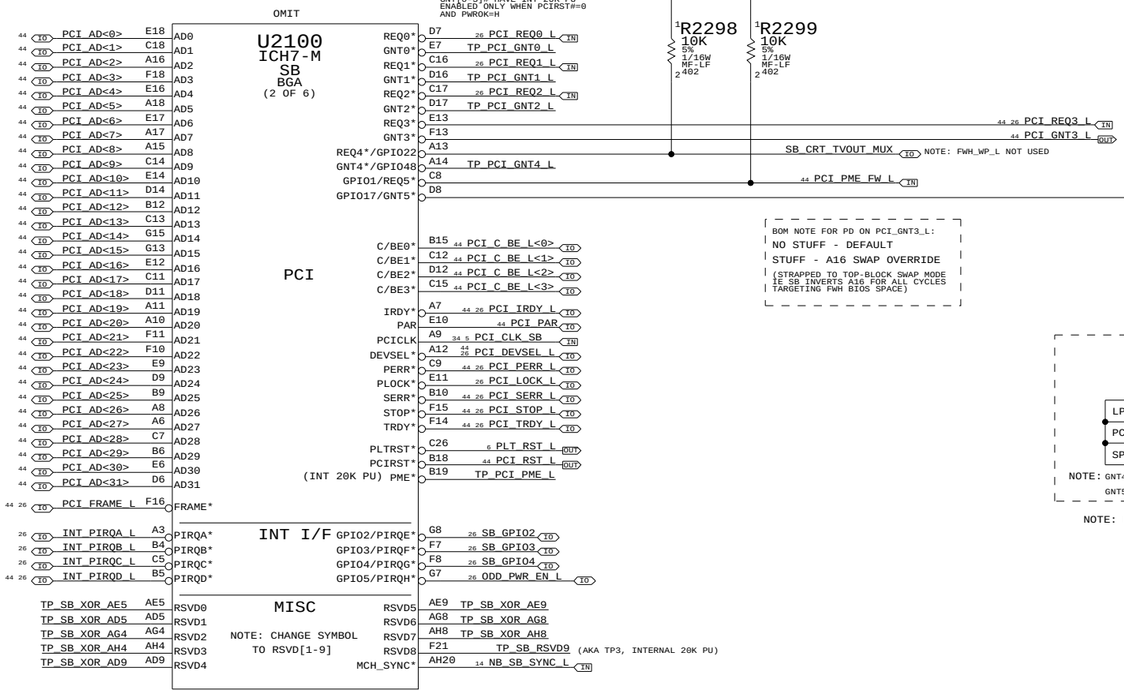
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 21 OF 111	









SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

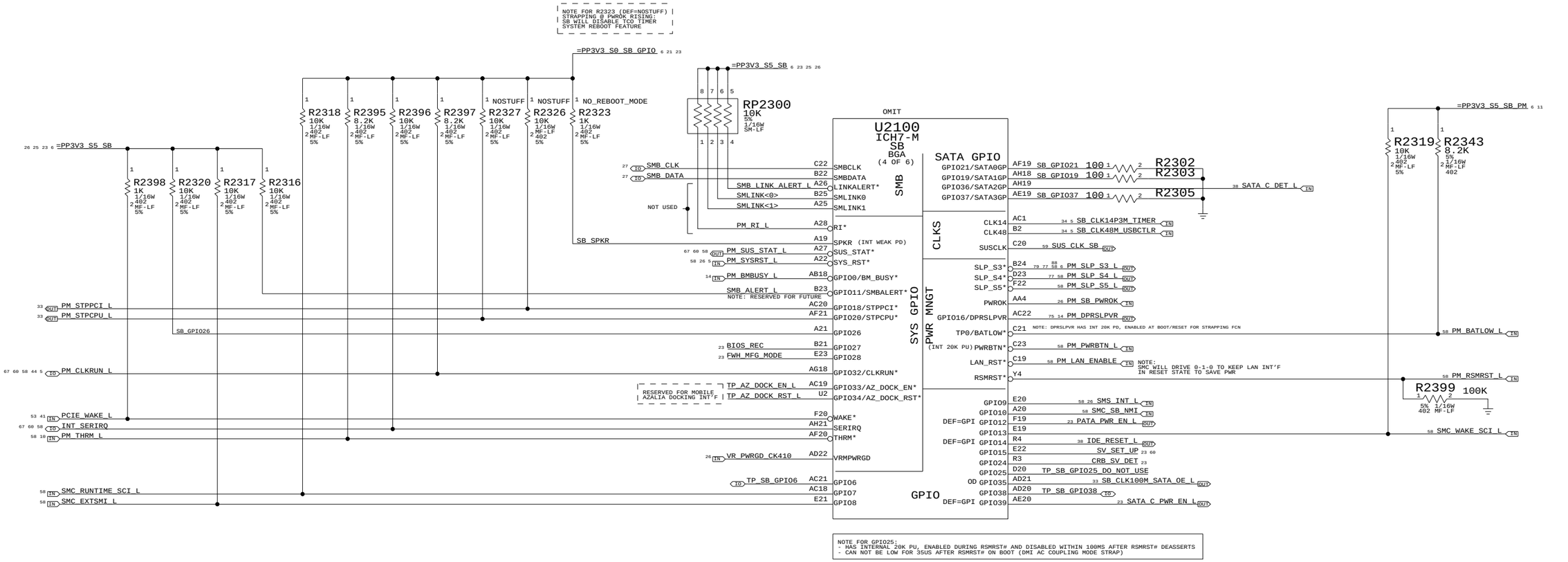
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 22 OF 111	



SB: 3 OF 4

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE SHT 23 OF 111

OMIT

U2100
ICH7-M
SB
BGA
(6 OF 6)

VSS

A4			AD3
A23			AD4
N24			AD7
P24			AD8
R18			AD15
U14			AD19
V27			AD23
AA24			AE2
AB27			AE4
AD11			AE8
B1			AE11
D10			AE13
F4			AE18
G18			AE21
J1			B8
L24			B11
M17			B14
N14			B17
N17			B20
N18			B26
N25			B28
N26			C2
P3			C6
P4			C27
P12			D13
P13			D18
P14			D21
P15			D24
P16			E1
P17			E2
P27			E4
P28			E8
R1			E15
R11			F3
R12			F5
R13			F12
R14			F27
R15			F28
R16			G1
R17			G2
T6			G5
T12			G6
T13			G9
T14			G14
T15			G21
T16			G24
T17			G25
U4			G26
U12			H3
U13			H4
U15			H5
U16			H24
U17			H27
U24			H28
U25			J2
U26			J5
V2			J24
V13			J25
V15			J26
V24			K24
V28			K27
W6			K28
W24			L13
W25			L15
W26			L25
Y3			L26
Y24			M3
Y27			M4
Y28			M5
AA1			M12
AA25			M13
AA26			M14
AB4			M15
AB6			M16
AB11			M24
AB14			M27
AB16			M28
AB19			N1
AB21			N2
AB24			N5
AB28			N6
AC2			N11
AC5			N12
AC9			N13
AC11			N15
AD1			N16
AE24			AG11
AE25			AG14
AF2			AG17
AF4			AG20
AF8			AG25
AF11			AH1
AF27			AH3
AF28			AH7
AG1			AH12
AG3			AH23
AG7			AH27

0 0

OMIT

U2100
ICH7-M
SB
BGA
(5 OF 6)

25 PP5V_S0_SB_V5REF	G10		L11
	AD17	V5REF	L12
25 PP5V_S5_SB_V5REF_SUS	F6	V5REF_SUS	L14
25 22 PP1V5_S0_SB_VCC1_5_B	AA22		L16
	AA23		L17
	AB22		L18
	AB23		M11
	AC23		M18
	AC24		P11
	AC25		P18
	AC26		T11
	AD26		T18
	AD27		U11
	AD28		U18
	D26		V11
	D27		V12
	D28		V14
	E24		V16
	E25		V17
	E26		V18
	F23		V5
	F24		V1
	G22		W2
	G23		W7
	H22	VCCA3GP	U6
	H23	VCC1_5_B	R7
	J22		AE23
	J23		AE26
	K22		AH26
	K23		AA7
	L22		AB12
	L23		AB20
	M22		AC16
	M23		AD13
	N22		AD18
	N23		AG12
	P22		AG15
	P23		AG19
	R22		A5
	R23		B13
	R24		B16
	R25		B7
	R26		C10
	T22		D15
	T23		F9
	T26		G11
	T27		G12
	T28		G16
	U22		W5
	U23		P7
	V22		A24
	V23		C24
	W22		D19
	W23		D22
	Y22		G19
	Y23		K3
25 24 6 =PP3V3_S0_SB_VCC3_3	B27	VCC3_3	K4
25 PP1V5_S0_SB_VCCDMIPLL	AG28	VCCDMIPLL	K5
25 6 =PP1V5_S0_SB_VCC1_5_A_ARX	AB7		K6
	AC6		L1
	AC7		L2
	AD6	ARX	L3
	AE6	VCC1_5_A	L6
	AF5		L7
	AF6		M6
	AG5		M7
	AH5		N7
25 6 =PP1V5_S0_SB_VCCSATAPLL	AD2	VCCSATAPLL	AB17
25 24 6 =PP3V3_S0_SB_VCC3_3	AH11	VCC3_3	AC17
25 6 =PP1V5_S0_SB_VCC1_5_A_ATX	AB10		T7
	AB9		F17
	AC10		G17
	AD10	ATX	AB8
	AE10	VCC1_5_A	AC8
	AF10		K7
	AF9		C28
	AG9		G20
	AH9		A1
25 24 6 =PP3V3_S5_SB_VCCSUS3_3	E3	VCCSUS3_3	H6
25 6 =PP1V5_S0_SB_VCCUSBPLL	C1	VCCUSBPLL	H7
	AA2		J6
	Y7	VCCLAN1_5	J7

CHANGE SYMBOL TO 1.05

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

CHANGE SYMBOL TO 1.05

USB CORE
VCC1_5_A

CORE
VCC1_05

VCC_PAUX
VCCLAN_3_3

V_CPU_IO

IDE
VCC3_3

PCI
VCC3_3

VCCRTC

USB
VCCSUS3_3

VCCSAUS1_5

=PPVCORE_S0_SB 6 25

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

=PP3V3_S0_SB_VCCLAN3_3 6 25

VCC3_3/VCCHDA =PP3V3_S0_SB_3V3_1V5_VCCHDA 6 25
VCCSUS3_3/VCCSUSHDA =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 6

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

=PP1V05_S0_SB_CPU_IO 6 21 25

=PP3V3_S0_SB_VCC3_3_IDE 6 25

=PP3V3_S0_SB_VCC3_3_PCI 6 25

PP3V3_S5_SB_RTC 5 21 25 26

=PP3V3_S5_SB_VCCSUS3_3 6 24 25

=PP3V3_S0_SB_VCCSUS3_3_USB 6 25

=PP1V5_S0_SB_VCC1_5_A 6 25

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE

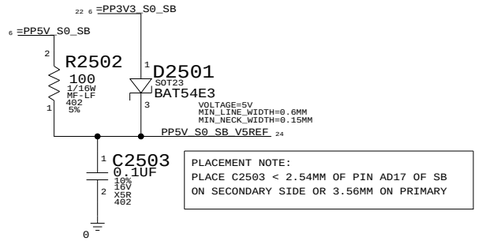
=PP1V5_S0_SB_VCC1_5_A_USB_CORE 6 25

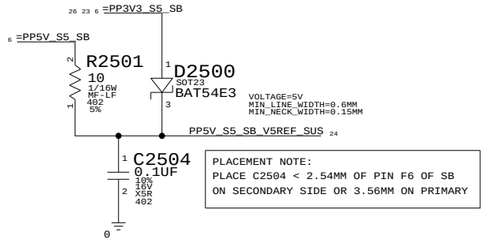
SB: 4 OF 4

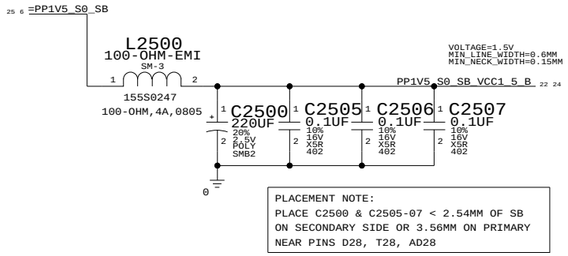
SYNC_MASTER=N/A SYNC_DATE=N/A

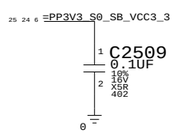
APPLE COMPUTER INC.

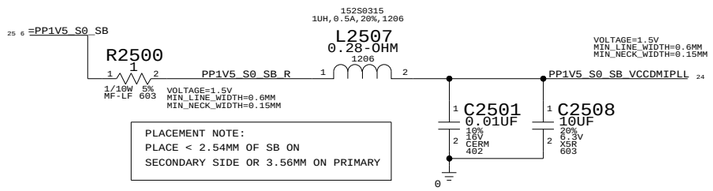
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE NONE	SHT 24 OF 111	

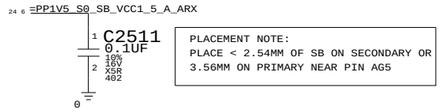


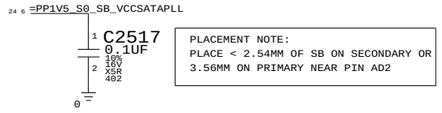


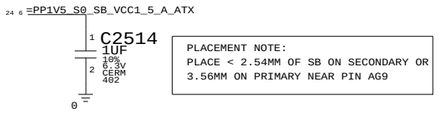


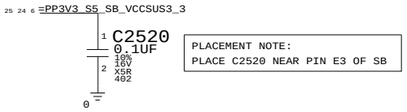


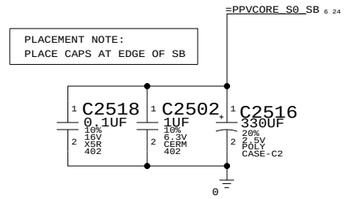


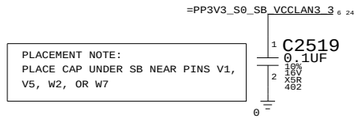


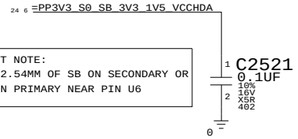


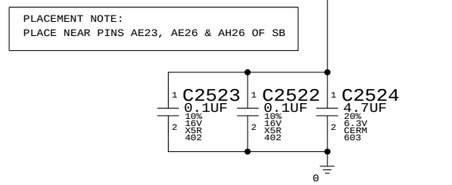


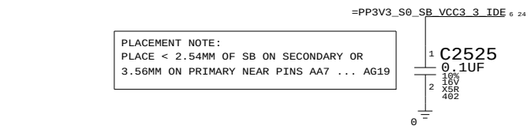


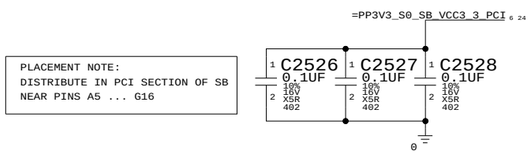


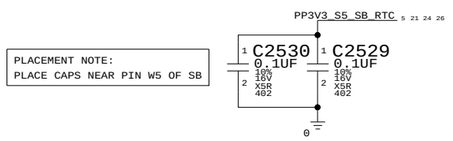


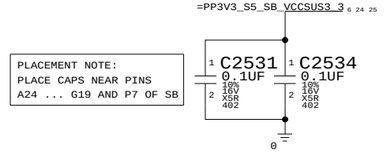


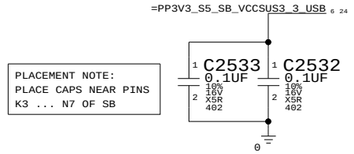


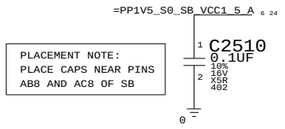


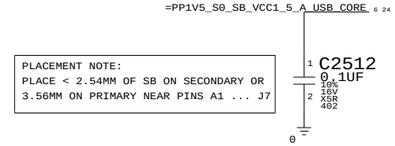












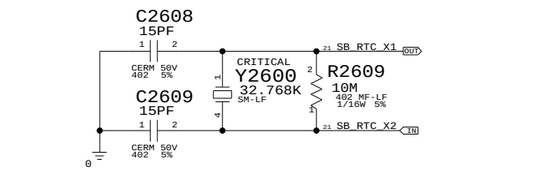
SB:DECOUPLING

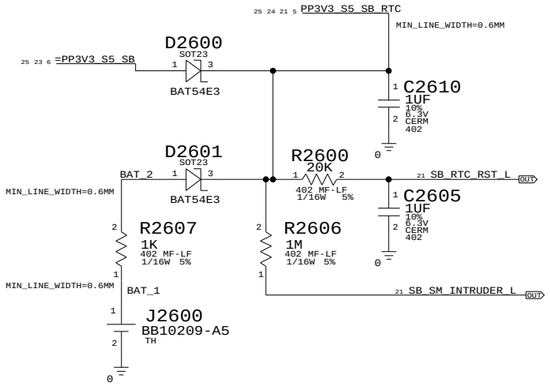
SYNC_MASTER=N/A SYNC_DATE=N/A

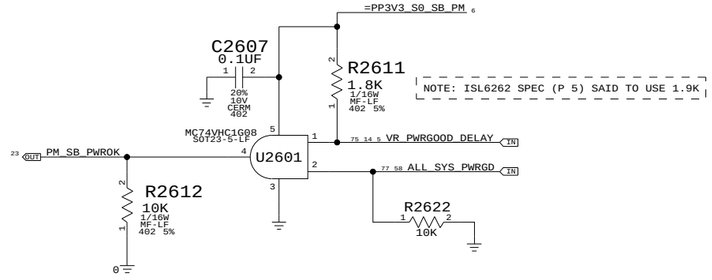
APPLE COMPUTER INC.

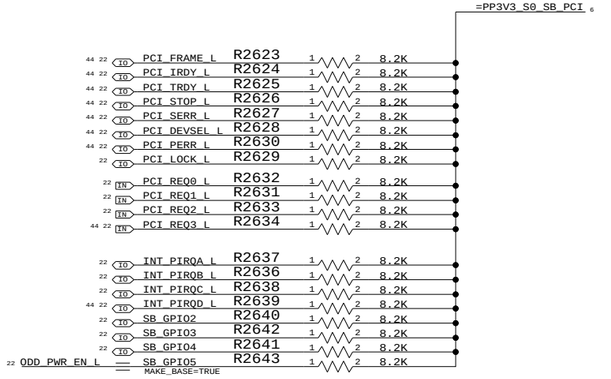
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

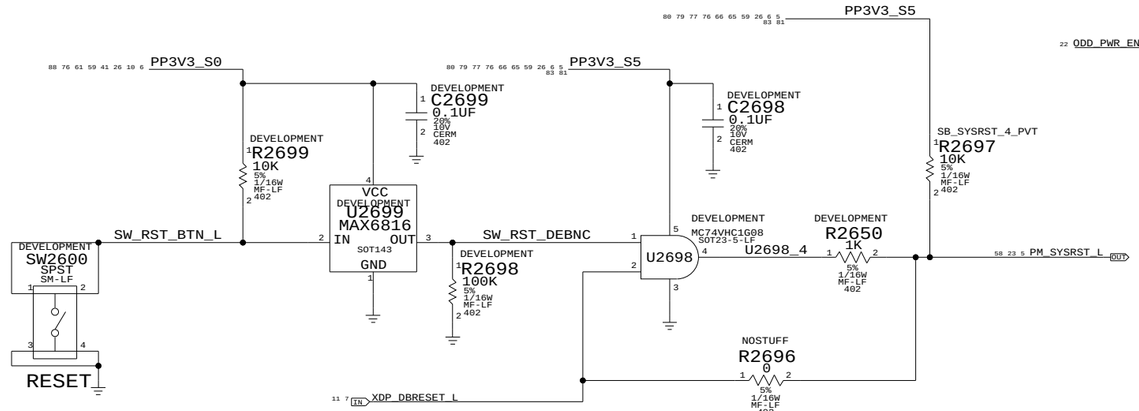
SCALE: NONE SHT 25 OF 111



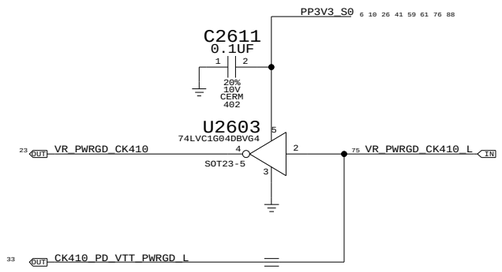








NOTE: R2696 CAN'T EXIST WITH BOTH ITP & DEVELOPMENT
SHOULD BE STUFFED WITH ITP & NO DEVELOPMENT



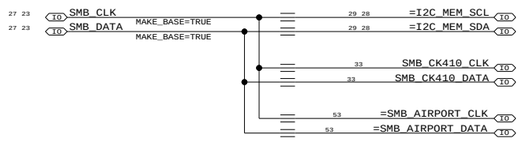
SB: MISC

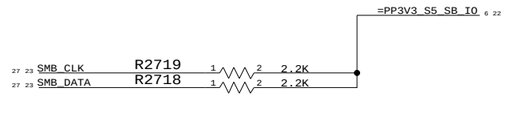
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 26 OF 111	

SB I2C BUSSES





SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 27 OF 111	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 VRef

One 0.1uF per connector

29 28 6 5 =PP1V8_S3_MEM

R2800 1K 1% 1/16W MF-LF 402

MEM_VREF 5 28 29
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R2801 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

29 28 5 MEM_VREF

C2850 2.2UF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

29 28 6 5 =PP1V8_S3_MEM

CRITICAL
J2800
F-RT-SM1
DDR2-SODIMM-STD

		VREF	1	VSS0	2	
		VSS1	3	DQ4	4	MEM_A_DQ<4> 15
15	MEM_A_DQ<0>	DQ0	5	DQ5	6	MEM_A_DQ<5> 15
15	MEM_A_DQ<1>	DQ1	7	VSS2	8	
		VSS4	9	DM0	10	MEM_A_DM<0> 15
15 5	MEM_A_DQS_N<0>	DQS0*	11	VSS5	12	
15 5	MEM_A_DQS_P<0>	DQS0	13	DQ6	14	MEM_A_DQ<6> 15
		VSS6	15	DQ7	16	MEM_A_DQ<7> 5 15
15	MEM_A_DQ<2>	DQ2	17	VSS7	18	
15	MEM_A_DQ<3>	DQ3	19	DQ12	20	MEM_A_DQ<12> 15
		VSS8	21	DQ13	22	MEM_A_DQ<13> 15
15	MEM_A_DQ<8>	DQ8	23	VSS9	24	
15	MEM_A_DQ<9>	DQ9	25	DM1	26	MEM_A_DM<1> 15
		VSS10	27	VSS11	28	
15 5	MEM_A_DQS_N<1>	DQS1*	29	CK0	30	MEM_CLK_P<0> 14
15 5	MEM_A_DQS_P<1>	DQS1	31	CK0*	32	MEM_CLK_N<0> 14
		VSS12	33	VSS13	34	
15	MEM_A_DQ<10>	DQ10	35	DQ14	36	MEM_A_DQ<14> 5 15
15	MEM_A_DQ<11>	DQ11	37	DQ15	38	MEM_A_DQ<15> 15
		VSS14	39	VSS15	40	
				KEY		
		VSS16	41	VSS17	42	
15 5	MEM_A_DQ<16>	DQ16	43	DQ20	44	MEM_A_DQ<20> 15
15	MEM_A_DQ<17>	DQ17	45	DQ21	46	MEM_A_DQ<21> 15
		VSS18	47	VSS19	48	
15 5	MEM_A_DQS_N<2>	DQS2*	49	NC0	50	DIMM_OVERTEMP_L 29 59
15 5	MEM_A_DQS_P<2>	DQS2	51	DM2	52	MEM_A_DM<2> 15
		VSS21	53	VSS22	54	
15	MEM_A_DQ<18>	DQ18	55	DQ22	56	MEM_A_DQ<22> 15
15	MEM_A_DQ<19>	DQ19	57	DQ23	58	MEM_A_DQ<23> 15
		VSS23	59	VSS24	60	
15	MEM_A_DQ<24>	DQ24	61	DQ28	62	MEM_A_DQ<28> 15
15 5	MEM_A_DQ<25>	DQ25	63	DQ29	64	MEM_A_DQ<29> 15
		VSS25	65	VSS26	66	
15	MEM_A_DM<3>	DM3	67	DQS3*	68	MEM_A_DQS_N<3> 5 15
	NC	NC1	69	DQS3	70	MEM_A_DQS_P<3> 5 15
		VSS27	71	VSS28	72	
15	MEM_A_DQ<26>	DQ26	73	DQ30	74	MEM_A_DQ<30> 15
15	MEM_A_DQ<27>	DQ27	75	DQ31	76	MEM_A_DQ<31> 15
		VSS29	77	VSS30	78	
30 14	MEM_CKE<0>	CKE0	79	NC/CKE1	80	MEM_CKE<1> 14 30
		VDD0	81	VDD1	82	
	NC	NC2	83	NC/A15	84	TP_MEM_A_A<15>
30 15	MEM_A_BS<2>	BA2	85	NC/A14	86	TP_MEM_A_A<14>
		VDD2	87	VDD3	88	
30 15	MEM_A_A<12>	A12	89	A11	90	MEM_A_A<11> 15 30
30 15	MEM_A_A<9>	A9	91	A7	92	MEM_A_A<7> 15 30
30 15	MEM_A_A<8>	A8	93	A6	94	MEM_A_A<6> 15 30
		VDD4	95	VDD5	96	
30 15	MEM_A_A<5>	A5	97	A4	98	MEM_A_A<4> 15 30
30 15	MEM_A_A<3>	A3	99	A2	100	MEM_A_A<2> 15 30
30 15	MEM_A_A<1>	A1	101	A0	102	MEM_A_A<0> 15 30
		VDD6	103	VDD7	104	
30 15	MEM_A_A<10>	A10/AP	105	BA1	106	MEM_A_BS<1> 15 30
30 15	MEM_A_BS<0>	BA0	107	RAS*	108	MEM_A_RAS_L 15 30
30 15	MEM_A_WE_L	WE*	109	S0*	110	MEM_CS_L<0> 14 30
		VDD8	111	VDD9	112	
30 15	MEM_A_CAS_L	CAS*	113	ODT0	114	MEM_ODT<0> 14 30
30 14	MEM_CS_L<1>	NC/S1*	115	NC/A13	116	MEM_A_A<13> 15 30
		VDD10	117	VDD11	118	
30 14	MEM_ODT<1>	NC/ODT1	119	NC3	120	NC
		VSS31	121	VSS32	122	
15	MEM_A_DQ<32>	DQ32	123	DQ36	124	MEM_A_DQ<36> 15
15	MEM_A_DQ<33>	DQ33	125	DQ37	126	MEM_A_DQ<37> 15
		VSS33	127	VSS34	128	
15 5	MEM_A_DQS_N<4>	DQS4*	129	DM4	130	MEM_A_DM<4> 15
15 5	MEM_A_DQS_P<4>	DQS4	131	VSS35	132	
		VSS36	133	DQ38	134	MEM_A_DQ<38> 15
15	MEM_A_DQ<34>	DQ34	135	DQ39	136	MEM_A_DQ<39> 5 15
15	MEM_A_DQ<35>	DQ35	137	VSS37	138	
		VSS38	139	DQ44	140	MEM_A_DQ<44> 15
15	MEM_A_DQ<40>	DQ40	141	DQ45	142	MEM_A_DQ<45> 15
15	MEM_A_DQ<41>	DQ41	143	VSS39	144	
		VSS40	145	DQS5*	146	MEM_A_DQS_N<5> 5 15
15	MEM_A_DM<5>	DM5	147	DQS5	148	MEM_A_DQS_P<5> 5 15
		VSS41	149	VSS42	150	
15	MEM_A_DQ<42>	DQ42	151	DQ46	152	MEM_A_DQ<46> 15
15	MEM_A_DQ<43>	DQ43	153	DQ47	154	MEM_A_DQ<47> 5 15
		VSS43	155	VSS44	156	
15	MEM_A_DQ<48>	DQ48	157	DQ52	158	MEM_A_DQ<52> 15
15	MEM_A_DQ<49>	DQ49	159	DQ53	160	MEM_A_DQ<53> 15
		VSS45	161	VSS46	162	
	NC	NC_TEST	163	CK1	164	MEM_CLK_P<1> 14
		VSS47	165	CK1*	166	MEM_CLK_N<1> 14
15 5	MEM_A_DQS_N<6>	DQS6*	167	VSS48	168	
15 5	MEM_A_DQS_P<6>	DQS6	169	DM6	170	MEM_A_DM<6> 15
		VSS49	171	VSS50	172	
15	MEM_A_DQ<50>	DQ50	173	DQ54	174	MEM_A_DQ<54> 5 15
15	MEM_A_DQ<51>	DQ51	175	DQ55	176	MEM_A_DQ<55> 15
		VSS51	177	VSS52	178	
15	MEM_A_DQ<56>	DQ56	179	DQ60	180	MEM_A_DQ<60> 15
15	MEM_A_DQ<57>	DQ57	181	DQ61	182	MEM_A_DQ<61> 15
		VSS53	183	VSS54	184	
15	MEM_A_DM<7>	DM7	185	DQS7*	186	MEM_A_DQS_N<7> 5 15
		VSS55	187	DQS7	188	MEM_A_DQS_P<7> 5 15
15	MEM_A_DQ<58>	DQ58	189	VSS56	190	
15 5	MEM_A_DQ<59>	DQ59	191	DQ62	192	MEM_A_DQ<62> 15
		VSS57	193	DQ63	194	MEM_A_DQ<63> 15
29 27	=I2C_MEM_SDA	SDA	195	VSS58	196	
29 27	=I2C_MEM_SCL	SCL	197	SA0	198	
		VDDSPD	199	SA1	200	ADDR=0xA0(WR)/0xA1(RD)
				GND	201 202 203 204 205	ALL NC'S

516S0403

29 6 =PPSPD_S0_MEM

C2851 2.2UF 20% 6.3V CERM1 603

C2852 0.1uF 20% 10V CERM 402

DDR2 Bypass Caps

(For return current)

29 28 6 5 =PP1V8_S3_MEM

C2801 10UF 20% 6.3V X5R 603
C2802 10UF 20% 6.3V X5R 603
C2803 10UF 20% 6.3V X5R 603
C2804 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402
C2811 0.1uF 20% 10V CERM 402
C2812 0.1uF 20% 10V CERM 402
C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402
C2815 0.1uF 20% 10V CERM 402
C2816 0.1uF 20% 10V CERM 402
C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402
C2819 0.1uF 20% 10V CERM 402
C2820 0.1uF 20% 10V CERM 402
C2821 0.1uF 20% 10V CERM 402

=PP1V8_S3_MEM 5 6 28 29

DIMM_OVERTEMP_L 29 59

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

=PP1V8_S3_MEM

MEM_VREF

C2950 2.2UF 20% 6.3V CERM1 603
C2900 0.1uF 20% 10V CERM 402

CRITICAL
J2900
F-RT-SM1
DDR2-SODIMM-REV

1	VREF	VSS0	2				
3	VSS1	DQ4	4	MEM_B_DQ<4>			
5	DQ0	DQ5	6	MEM_B_DQ<5>			
7	DQ1	VSS2	8				
9	VSS4	DM0	10	MEM_B_DM<0>			
11	DQS0*	VSS5	12				
13	DQS0	DQ6	14	MEM_B_DQ<6>			
15	VSS6	DQ7	16	MEM_B_DQ<7>			
17	DQ2	VSS7	18				
19	DQ3	DQ12	20	MEM_B_DQ<12>			
21	VSS8	DQ13	22	MEM_B_DQ<13>			
23	DQ8	VSS9	24				
25	DQ9	DM1	26	MEM_B_DM<1>			
27	VSS10	VSS11	28				
29	DQS1*	CK0	30	MEM_CLK_P<3>			
31	DQS1	CK0*	32	MEM_CLK_N<3>			
33	VSS12	VSS13	34				
35	DQ10	DQ14	36	MEM_B_DQ<14>			
37	DQ11	DQ15	38	MEM_B_DQ<15>			
39	VSS14	VSS15	40				
KEY							
41	VSS16	VSS17	42				
43	DQ16	DQ20	44	MEM_B_DQ<20>			
45	DQ17	DQ21	46	MEM_B_DQ<21>			
47	VSS18	VSS19	48				
49	DQS2*	NC0	50	DIMM_OVERTEMP_L	28 59		
51	DQS2	DM2	52	MEM_B_DM<2>			
53	VSS21	VSS22	54				
55	DQ18	DQ22	56	MEM_B_DQ<22>			
57	DQ19	DQ23	58	MEM_B_DQ<23>			
59	VSS23	VSS24	60				
61	DQ24	DQ28	62	MEM_B_DQ<28>			
63	DQ25	DQ29	64	MEM_B_DQ<29>			
65	VSS25	VSS26	66				
67	DM3	DQS3*	68	MEM_B_DQS_N<3>			
NC 69	NC1	DQS3	70	MEM_B_DQS_P<3>			
71	VSS27	VSS28	72				
73	DQ26	DQ30	74	MEM_B_DQ<30>			
75	DQ27	DQ31	76	MEM_B_DQ<31>			
77	VSS29	VSS30	78				
79	CKE0	NC/CKE1	80	MEM_CKE<3>			
81	VDD0	VDD1	82				
NC 83	NC2	NC/A15	84	TP_MEM_B_A<15>			
85	BA2	NC/A14	86	TP_MEM_B_A<14>			
87	VDD2	VDD3	88				
89	A12	A11	90	MEM_B_A<11>			
91	A9	A7	92	MEM_B_A<7>			
93	A8	A6	94	MEM_B_A<6>			
95	VDD4	VDD5	96				
97	A5	A4	98	MEM_B_A<4>			
99	A3	A2	100	MEM_B_A<2>			
101	A1	A0	102	MEM_B_A<0>			
103	VDD6	VDD7	104				
105	A10/AP	BA1	106	MEM_B_BS<1>			
107	BA0	RAS*	108	MEM_B_RAS_L			
109	WE*	S0*	110	MEM_CS_L<2>			
111	VDD8	VDD9	112				
113	CAS*	ODT0	114	MEM_ODT<2>			
115	NC/S1*	NC/A13	116	MEM_B_A<13>			
117	VDD10	VDD11	118				
119	NC/ODT1	NC3	120	NC			
121	VSS31	VSS32	122				
123	DQ32	DQ36	124	MEM_B_DQ<36>			
125	DQ33	DQ37	126	MEM_B_DQ<37>			
127	VSS33	VSS34	128				
129	DQS4*	DM4	130	MEM_B_DM<4>			
131	DQS4	VSS35	132				
133	VSS36	DQ38	134	MEM_B_DQ<38>			
135	DQ34	DQ39	136	MEM_B_DQ<39>			
137	DQ35	VSS37	138				
139	VSS38	DQ44	140	MEM_B_DQ<44>			
141	DQ40	DQ45	142	MEM_B_DQ<45>			
143	DQ41	VSS39	144				
145	VSS40	DQS5*	146	MEM_B_DQS_N<5>			
147	DM5	DQS5	148	MEM_B_DQS_P<5>			
149	VSS41	VSS42	150				
151	DQ42	DQ46	152	MEM_B_DQ<46>			
153	DQ43	DQ47	154	MEM_B_DQ<47>			
155	VSS43	VSS44	156				
157	DQ48	DQ52	158	MEM_B_DQ<52>			
159	DQ49	DQ53	160	MEM_B_DQ<53>			
161	VSS45	VSS46	162				
NC 163	NC_TEST	CK1	164	MEM_CLK_P<2>			
165	VSS47	CK1*	166	MEM_CLK_N<2>			
167	DQS6*	VSS48	168				
169	DQS6	DM6	170	MEM_B_DM<6>			
171	VSS49	VSS50	172				
173	DQ50	DQ54	174	MEM_B_DQ<54>			
175	DQ51	DQ55	176	MEM_B_DQ<55>			
177	VSS51	VSS52	178				
179	DQ56	DQ60	180	MEM_B_DQ<60>			
181	DQ57	DQ61	182	MEM_B_DQ<61>			
183	VSS53	VSS54	184				
185	DM7	DQS7*	186	MEM_B_DQS_N<7>			
187	VSS55	DQS7	188	MEM_B_DQS_P<7>			
189	DQ58	VSS56	190				
191	DQ59	DQ62	192	MEM_B_DQ<62>			
193	VSS57	DQ63	194	MEM_B_DQ<63>			
195	SDA	VSS58	196	ADDR=0XA4(WR)/0XA5(RD)			
197	SCL	SA0	198				
199	VDDSPD	SA1	200	MEM_B_SPD_SA1			
201	GND						
202	GND						
203	GND						
204	GND						
205	GND						

ALL NC'S

516S0404

=PPSPD_S0_MEM

C2951 2.2UF 20% 6.3V CERM1 603
C2952 0.1uF 20% 10V CERM 402

=PPSPD_S0_MEM

R2900 10K 5% 1/16W MF-LF 402

Resistor prevents pwr-gnd short

DDR2 Bypass Caps

(For return current)

=PP1V8_S3_MEM

C2908 C2909 C2910 C2911
C2912 C2913 C2914 C2915
C2916 C2917 C2918 C2919
C2920 C2921 C2922 C2923

1UF 10% 6.3V CERM 402

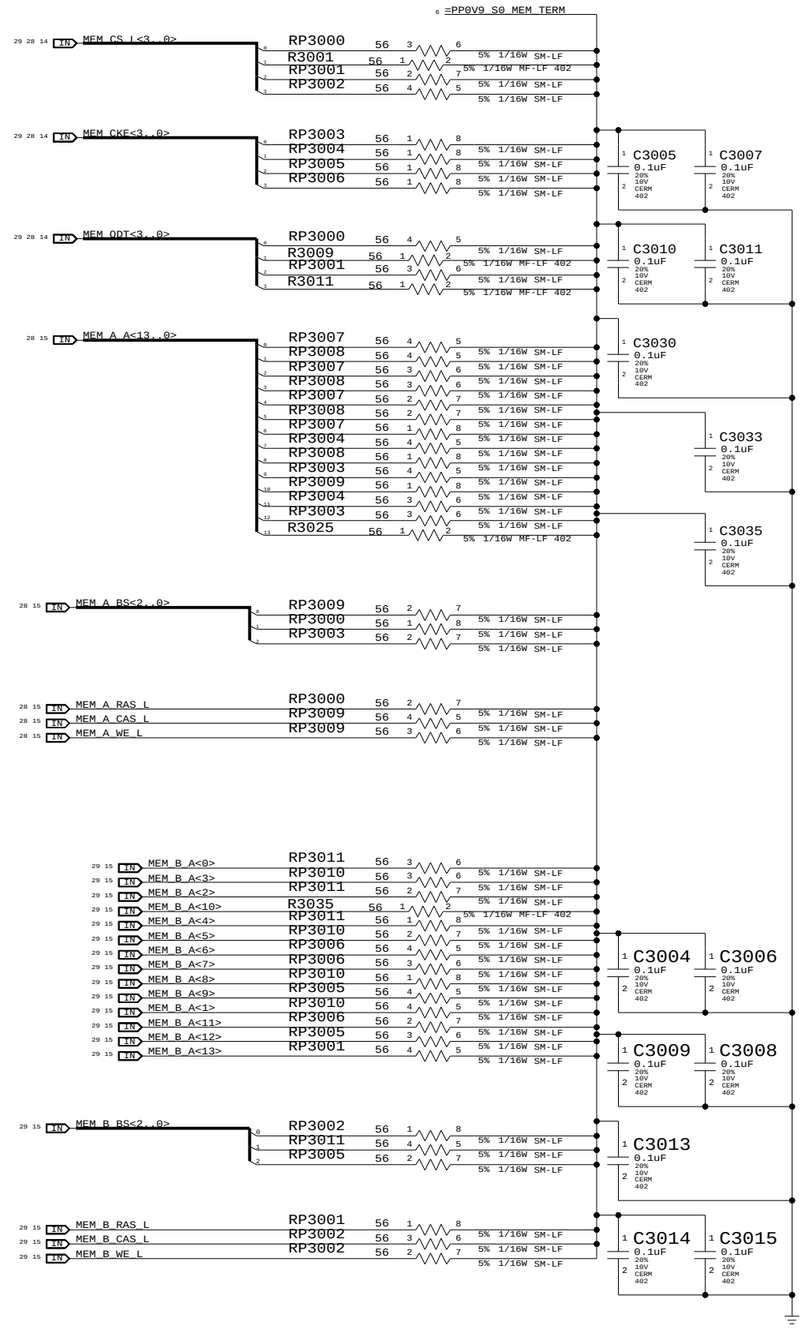
DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 29 OF 111	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	30	111

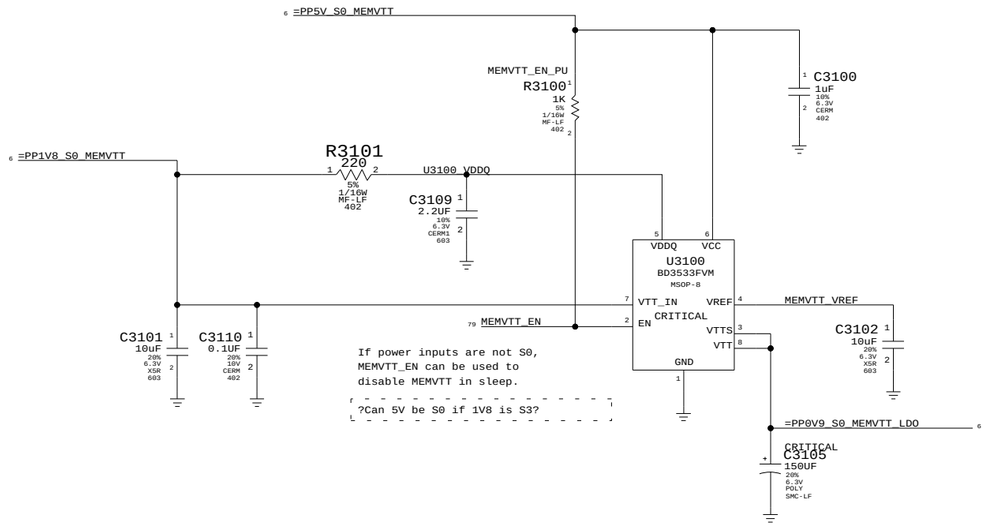
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



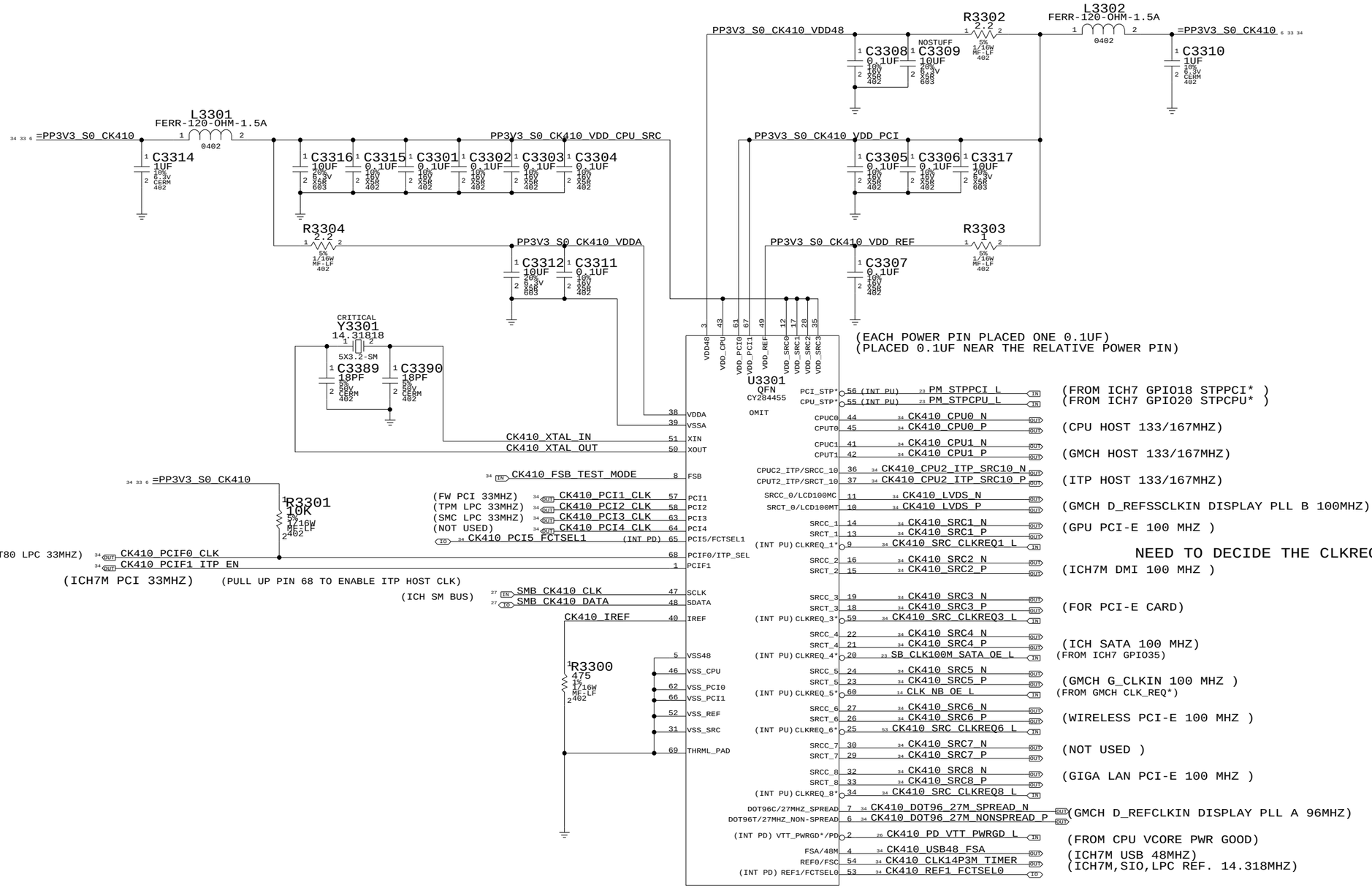
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	31	111



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 33 OF 111	

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S

33 CK410_SRC_CLKREQ1_L (GPU CLK OE*) — R3495 1K
33 CK410_SRC_CLKREQ3_L (SPARE CLK OE*) — R3494 1K
33 CK410_SRC_CLKREQ8_L (YUKON CLK OE*) — R3493 1K

FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3459 R3463	R3452 R3457 R3461
533MHZ (133MHZ CPU CLK)	R3452 R3457 R3461	R3454 R3459 R3463
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3454 R3459 R3463 R3457

81 34 6 PP1V05_S0

R3453 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<0>
34 CK410_FSA
R3455 1K 1/16W 5% MF-LF 402
7 CPU_BSEL<0>

NOSTUFF R3452 56 5% 1/16W MF-LF 402
R3454 0 5% 1/16W MF-LF 402

81 34 6 PP1V05_S0

R3458 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<1>
33 CK410_FSB_TEST_MODE
7 CPU_BSEL<1>

R3456 1K 5% 1/16W MF-LF 402
NOSTUFF R3457 0 5% 1/16W MF-LF 402
R3459 0 5% 1/16W MF-LF 402

81 34 6 PP1V05_S0

R3462 1K 1/16W 5% MF-LF 402 — 14 NB_BSEL<2>
34 CK410_FSC
7 CPU_BSEL<2>

R3460 1K 5% 1/16W MF-LF 402
NOSTUFF R3461 0 5% 1/16W MF-LF 402
R3463 0 5% 1/16W MF-LF 402

=PP3V3_S0_CK410 6 33

33 IO CK410_PCI5_FCTSEL1 — R3499 1K 1/16W 5% MF-LF 402

R3497 2.2K 5% 1/16W MF-LF 402 — CK410_FSC 34

33 IN CK410_CLK14P3M_TIMER — R3498 33 1/16W 5% MF-LF 402 — SB_CLK14P3M_TIMER OUT 5 23

33 IN CK410_REF1_FCTSEL0 — R3496 33 — TP_CLK14P3M_SPARE OUT

R3451 2.2K 5% 1/16W MF-LF 402 — CK410_FSA 34

33 IN CK410_USB48_FSA — R3400 33 1/16W 5% MF-LF 402 — SB_CLK48M_USBCTLR OUT 5 23
33 IN CK410_PCI4_CLK — R3406 33 — TP_PCI_CLK_SPARE OUT 9
33 IN CK410_PCI3_CLK — R3405 33 — PCI_CLK_SMC OUT 58
33 IN CK410_PCI2_CLK — R3404 33 — PCI_CLK_TPM OUT 67
33 IN CK410_PCI1_CLK — R3403 33 — PCI_CLK_FW OUT 44
33 IN CK410_PCIF1_ITP_EN — R3401 33 — PCI_CLK_SB OUT 5 22
33 IN CK410_PCIF0_CLK — R3402 33 — PCI_CLK_PORT80 OUT 60

33 IN CK410_CPU1_P — R3407 33 — FSB_CLK_NB_P OUT 5 12 34
33 IN CK410_CPU1_N — R3408 33 — FSB_CLK_NB_N OUT 5 12 34
33 IN CK410_CPU0_P — R3409 33 — FSB_CLK_CPU_P OUT 5 7 34
33 IN CK410_CPU0_N — R3410 33 — FSB_CLK_CPU_N OUT 5 7 34
33 IN CK410_CPU2_ITP_SRC10_P — R3411 33 — 34 FSB_CLK_XDP_P — CPU_XDP_CLK_P 11
33 IN CK410_CPU2_ITP_SRC10_N — R3412 33 — MAKE_BASE=TRUE — 34 FSB_CLK_XDP_N — MAKE_BASE=TRUE — CPU_XDP_CLK_N 11

33 IN CK410_SRC6_P — R3413 33 — AIRPORT_CLK100M_PCIE_P OUT 34 53
33 IN CK410_SRC6_N — R3414 33 — AIRPORT_CLK100M_PCIE_N OUT 34 53
33 IN CK410_SRC5_P — R3415 33 — NB_CLK100M_GCLKIN_P OUT 5 14 34
33 IN CK410_SRC5_N — R3416 33 — NB_CLK100M_GCLKIN_N OUT 5 14 34
33 IN CK410_SRC4_P — R3417 33 — SB_CLK100M_SATA_P OUT 5 21 34
33 IN CK410_SRC4_N — R3418 33 — SB_CLK100M_SATA_N OUT 5 21 34
33 IN CK410_SRC2_P — R3419 33 — SB_CLK100M_DMI_P OUT 5 22 34
33 IN CK410_SRC2_N — R3420 33 — SB_CLK100M_DMI_N OUT 5 22 34
33 IN CK410_SRC8_P — R3421 33 — ENET_CLK100M_PCIE_P OUT 5 34 41
33 IN CK410_SRC8_N — R3422 33 — ENET_CLK100M_PCIE_N OUT 5 34 41
33 IN CK410_SRC1_P — R3423 33 — GPU_CLK100M_PCIE_P OUT 5 34 84
33 IN CK410_SRC1_N — R3424 33 — GPU_CLK100M_PCIE_N OUT 5 34 84
33 IN CK410_LVDS_P — TP_CK410_LVDS_P
33 IN CK410_LVDS_N — TP_CK410_LVDS_N

33 IN CK410_DOT96_27M_SPREAD_N — R3470 33 — CK410_27M_SPREAD OUT 92
33 IN CK410_DOT96_27M_NONSPREAD_P — R3471 33 — CK410_27M_NONSPREAD OUT 92

33 IN CK410_SRC3_P — R3492 33 — SPARE_SRC3_P — R3488 49.9
33 IN CK410_SRC3_N — R3491 33 — SPARE_SRC3_N — R3487 49.9
33 IN CK410_SRC7_P — R3490 33 — SPARE_SRC7_P — R3486 49.9
33 IN CK410_SRC7_N — R3489 33 — SPARE_SRC7_N — R3485 49.9

1% 402 1/16W MF-LF

34 12 5 FSB_CLK_NB_P — R3429 49.9
34 12 5 FSB_CLK_NB_N — R3430 49.9
34 7 5 FSB_CLK_CPU_P — R3431 49.9
34 7 5 FSB_CLK_CPU_N — R3432 49.9
34 FSB_CLK_XDP_P — R3433 49.9
34 FSB_CLK_XDP_N — R3434 49.9
53 34 AIRPORT_CLK100M_PCIE_P — R3435 49.9
53 34 AIRPORT_CLK100M_PCIE_N — R3436 49.9
34 14 5 NB_CLK100M_GCLKIN_P — R3438 49.9
34 14 5 NB_CLK100M_GCLKIN_N — R3437 49.9
34 21 5 SB_CLK100M_SATA_P — R3439 49.9
34 21 5 SB_CLK100M_SATA_N — R3440 49.9
34 22 5 SB_CLK100M_DMI_P — R3442 49.9
34 22 5 SB_CLK100M_DMI_N — R3441 49.9
41 34 5 ENET_CLK100M_PCIE_P — R3443 49.9
41 34 5 ENET_CLK100M_PCIE_N — R3444 49.9
84 34 5 GPU_CLK100M_PCIE_P — R3446 49.9
84 34 5 GPU_CLK100M_PCIE_N — R3445 49.9

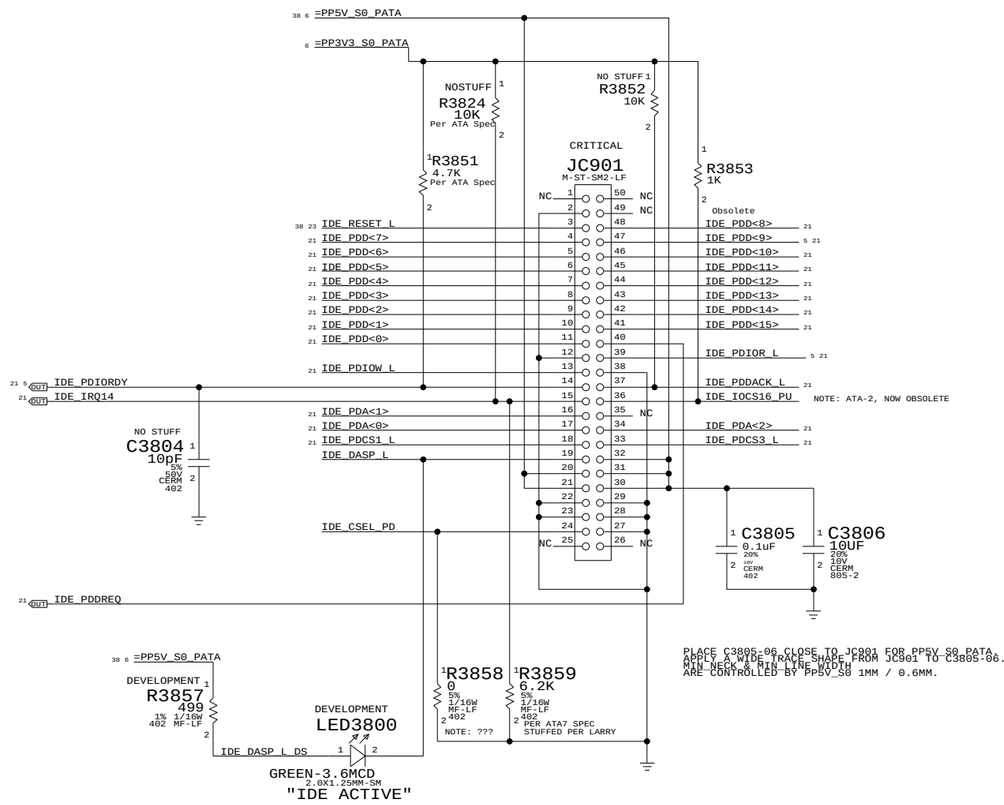
CLOCKS: TERMINATIONS

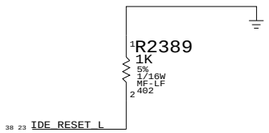
SYNC_MASTER=N/A SYNC_DATE=N/A

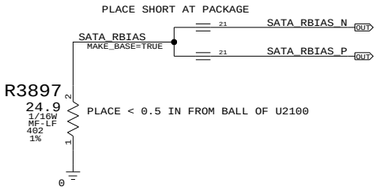
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 34 OF 111	

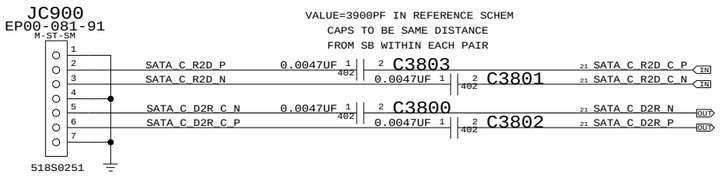
PATA CONNECTOR

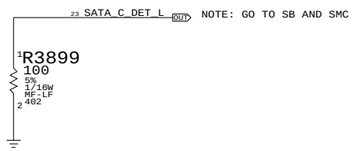






SATA CONNECTOR

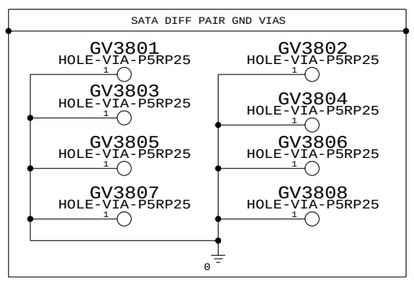




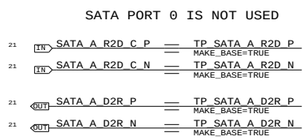
SMT NUTS FOR ODD ADAPTER

SDF3800
STDOFF-3.50D1.35H-1.55-TH

SDF3801
STDOFF-3.50D1.35H-1.55-TH



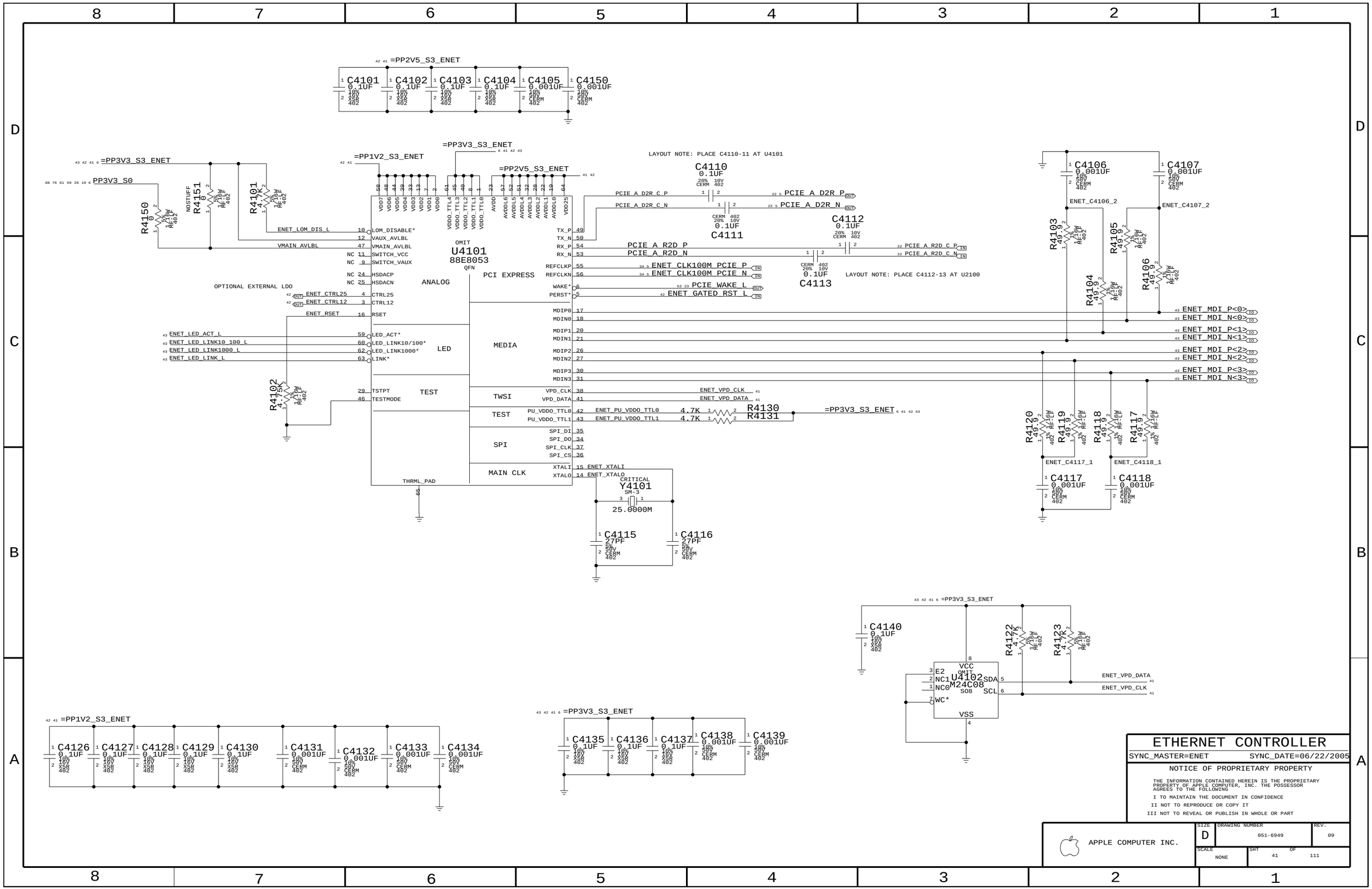
SATA PORT 0 IS NOT USED



Disk Connectors

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6950	06
SCALE: NONE	SHT 38 OF 111	


=PP2V5_S3_ENET
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4150 0.001UF 10% 50V CERM 402
=PP3V3_S3_ENET
=PP1V2_S3_ENET
=PP2V5_S3_ENET
PP3V3_S0
R4150 0 5% 1/16W MF-LF 402
R4151 NOSTUFF 10K 5% 1/16W MF-LF 402
R4101 4.7K 5% 1/16W MF-LF 402
ENET_LOM_DIS_L
VMAIN_AVLBL
OMIT
U4101
88E8053
QFN
ANALOG
PCI EXPRESS
MEDIA
LED
TEST
TWSI
SPI
MAIN CLK
THRML_PAD
LAYOUT NOTE: PLACE C4110-11 AT U4101
C4110 0.1UF 20% 10V CERM 402
C4111 0.1UF 20% 10V CERM 402
C4112 0.1UF 20% 10V CERM 402
C4113 0.1UF 20% 10V CERM 402
PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N
ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_GATED_RST_L
LAYOUT NOTE: PLACE C4112-13 AT U2100
OPTIONAL EXTERNAL LDO
ENET_CTRL25
ENET_CTRL12
ENET_RSET
R4102 4.75K 1% 1/16W MF-LF 402
ENET_LED_ACT_L
ENET_LED_LINK10_100_L
ENET_LED_LINK1000_L
ENET_LED_LINK_L
ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDDO_TTL0
ENET_PU_VDDO_TTL1
R4130 4.7K
R4131 4.7K
=PP3V3_S3_ENET
SPI_DI
SPI_DO
SPI_CLK
SPI_CS
ENET_XTALI
ENET_XTALO
CRITICAL
Y4101
SM-3
25.0000M
C4115 27PF 5% 50V CERM 402
C4116 27PF 5% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.001UF 10% 50V CERM 402
ENET_C4106_2
ENET_C4107_2
R4103 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4106 49.9 1% 1/16W MF-LF 402
ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402
ENET_C4117_1
ENET_C4118_1
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402
C4140 0.1UF 10% 16V X5R 402
U4102
M24C08
SO8
VCC
OMIT
E2
NC1
NC0
WC*
VSS
SDA
SCL
R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402
C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402
ETHERNET CONTROLLER
SYNC_MASTER=ENET
SYNC_DATE=06/22/2005
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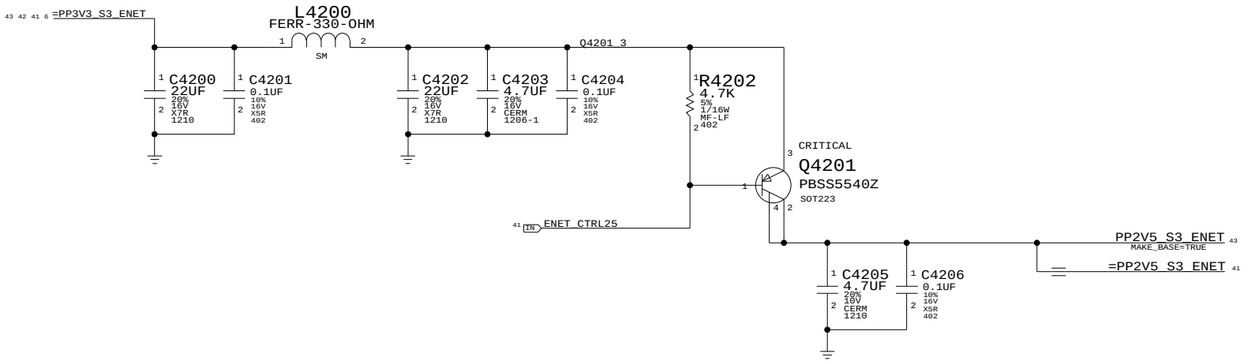
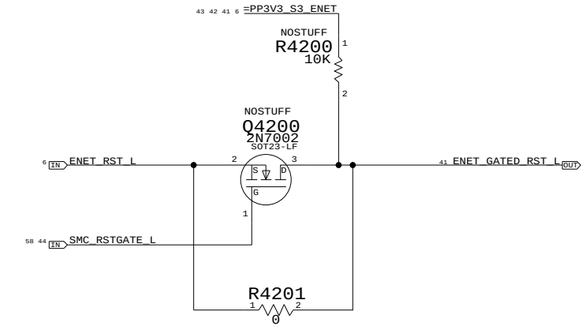
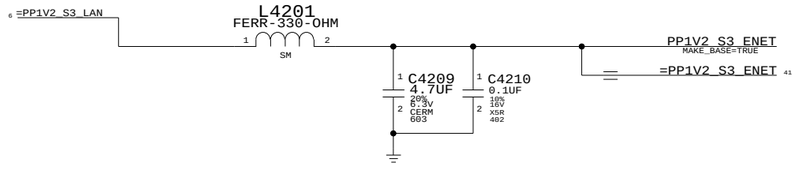
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6949
REV. 09
SCALE NONE
SHT 41 OF 111







ETHERNET MISC

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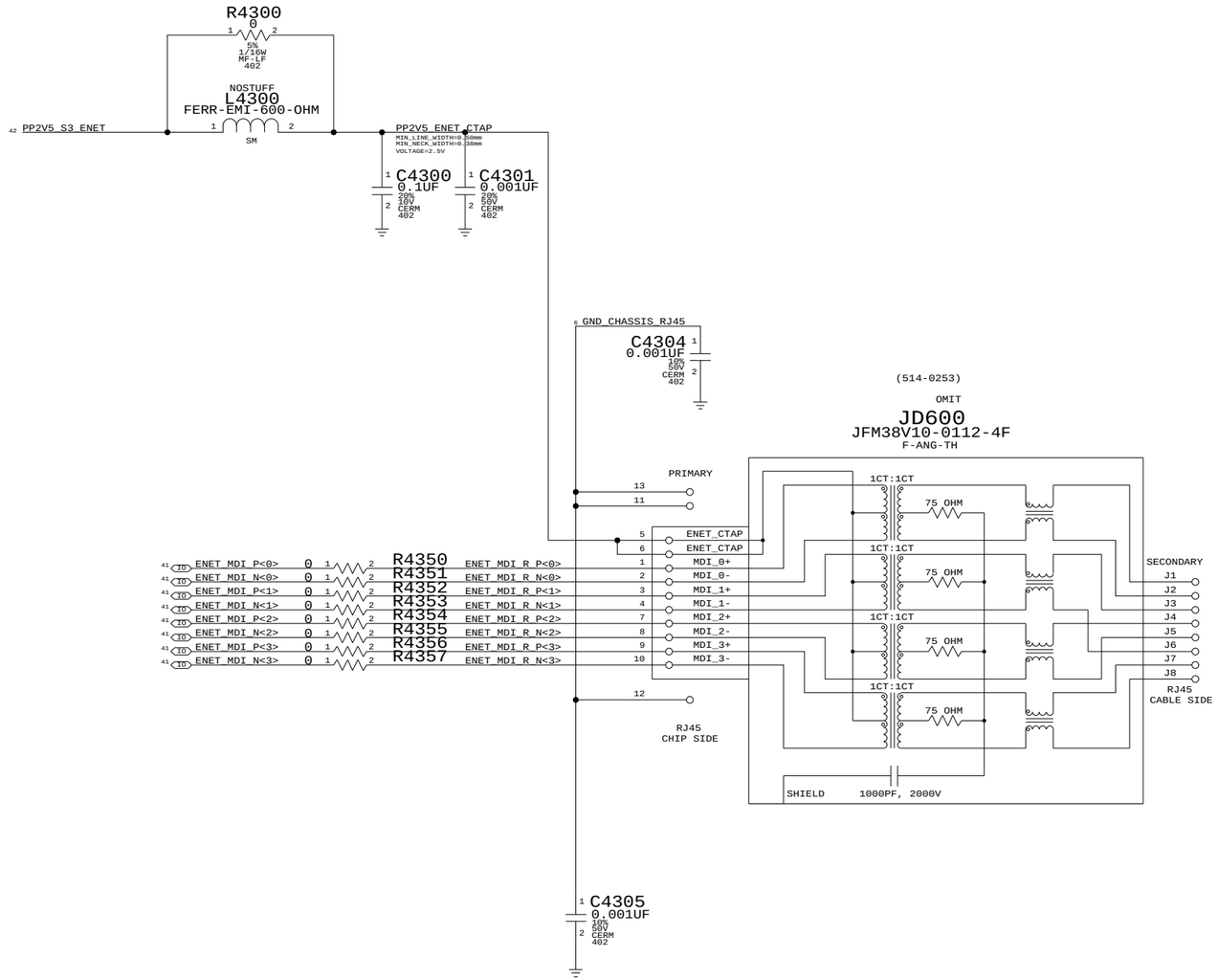
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE	SHT	OF
NONE	42	111

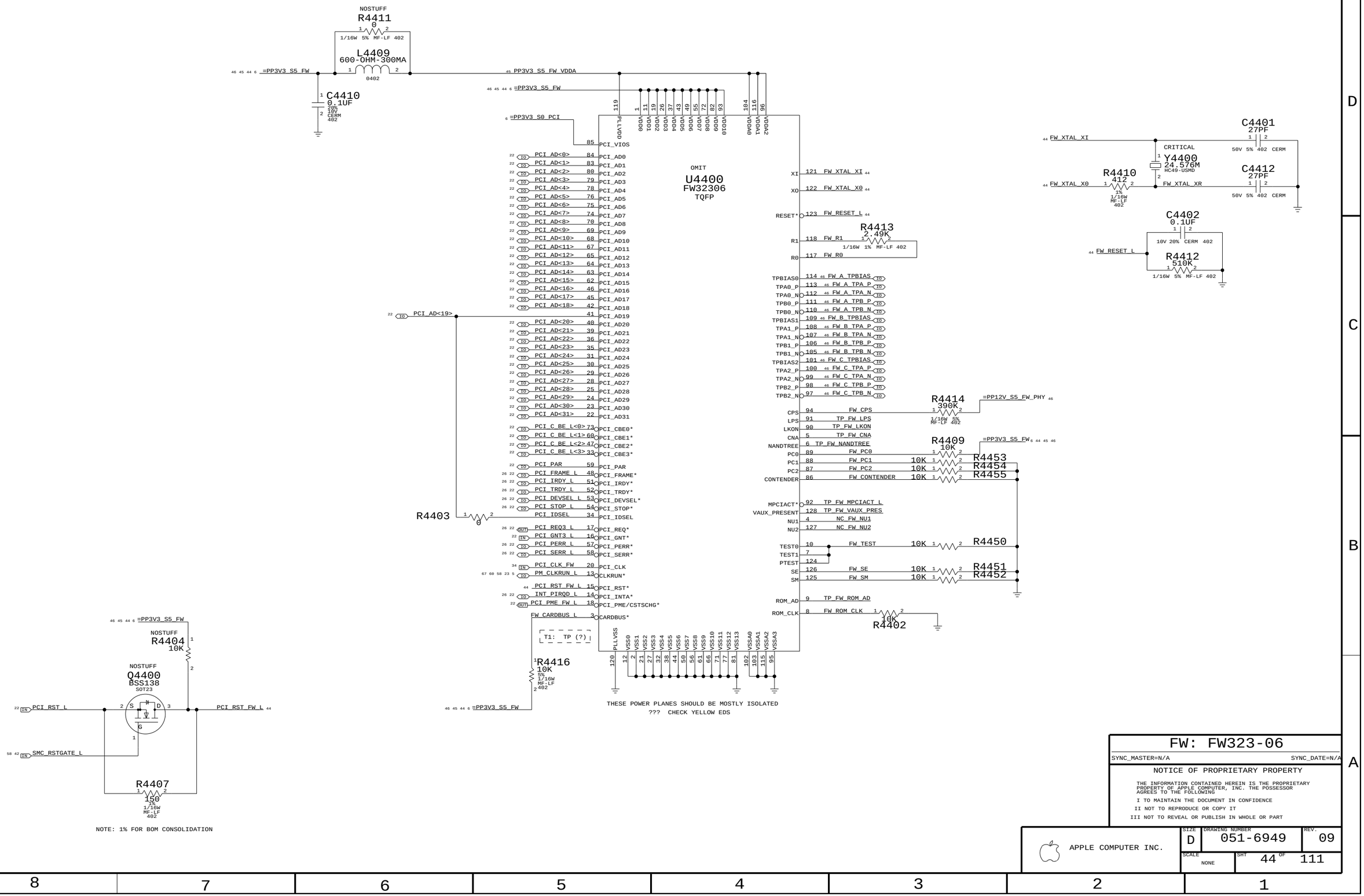


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0300	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0301	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

ETHERNET CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 43 OF 111	



FW:	FW323-06
SYNC_MASTER=N/A	SYNC_DATE=N/A

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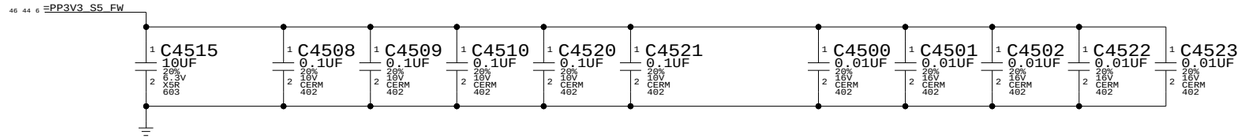
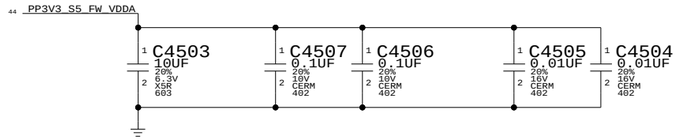
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6949	REV: 09
	SCALE: NONE	SHT 44 OF 111	





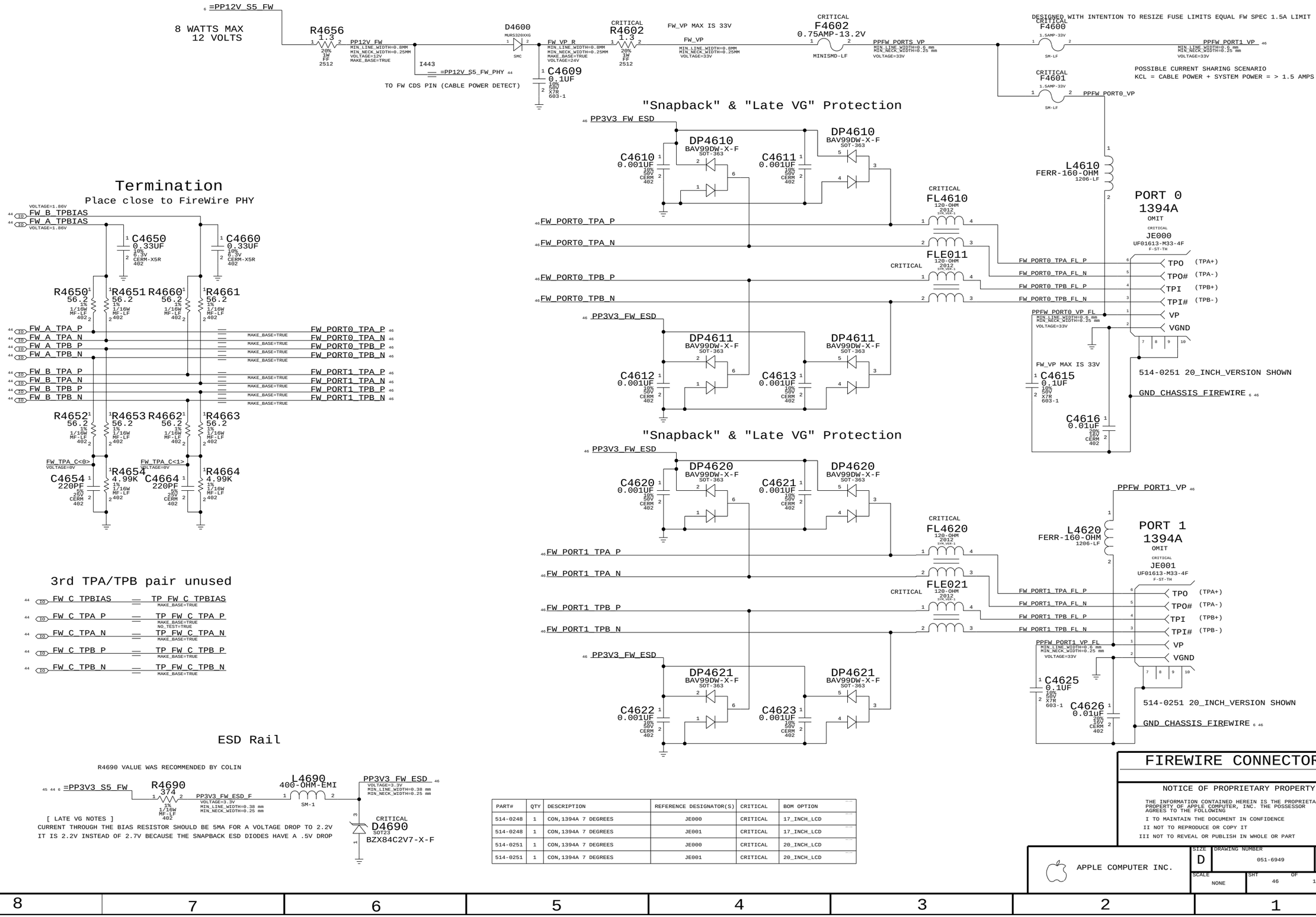
FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	45 OF 111



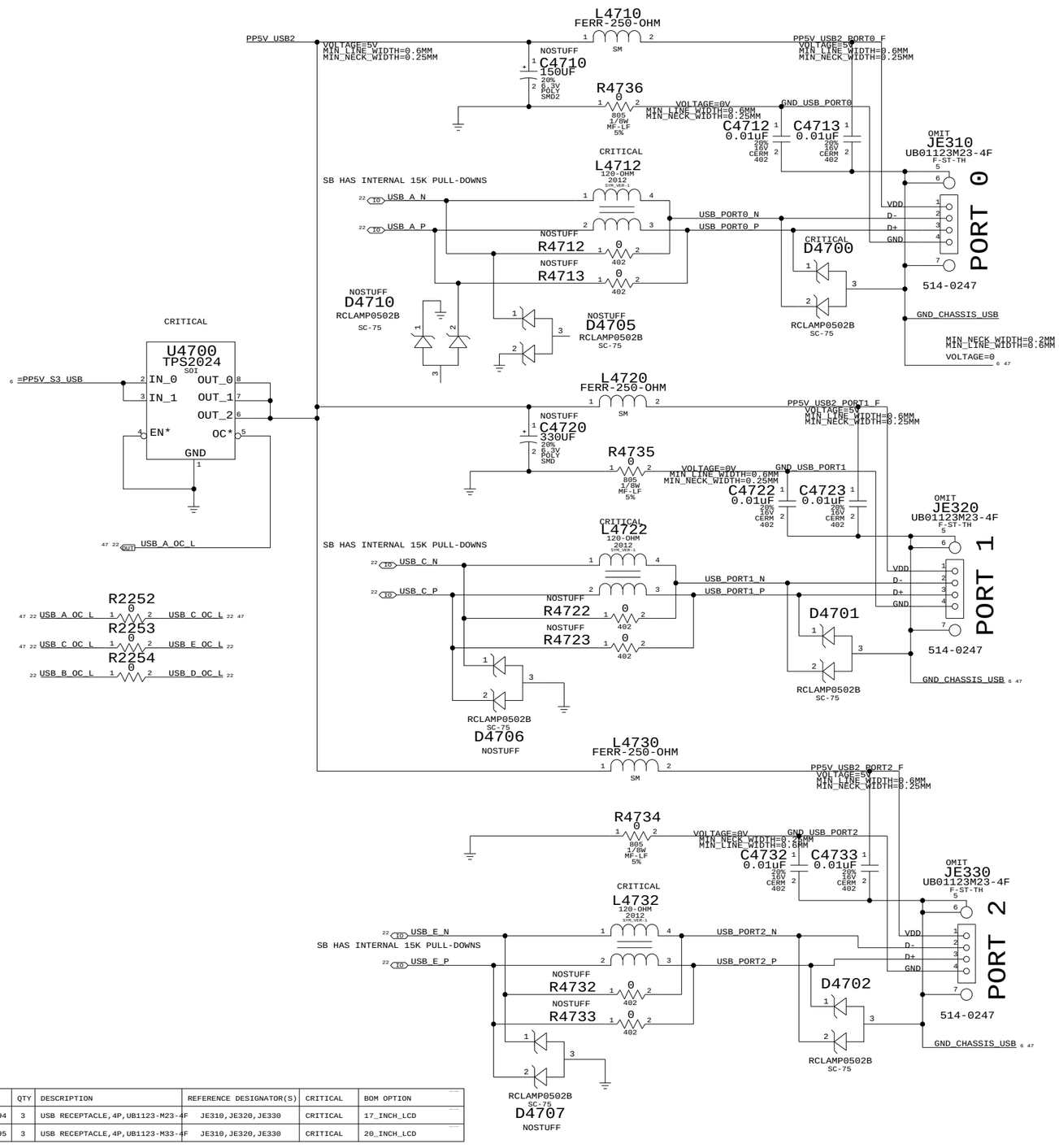
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

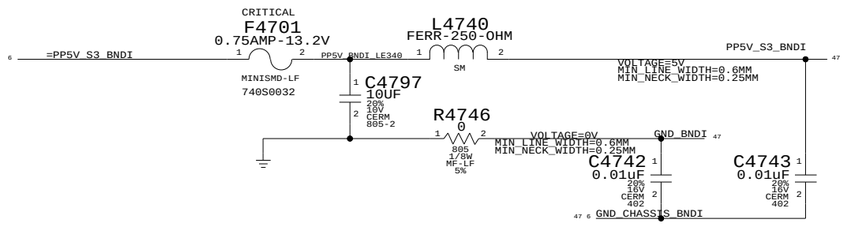
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 46 OF 111	

External USB Ports

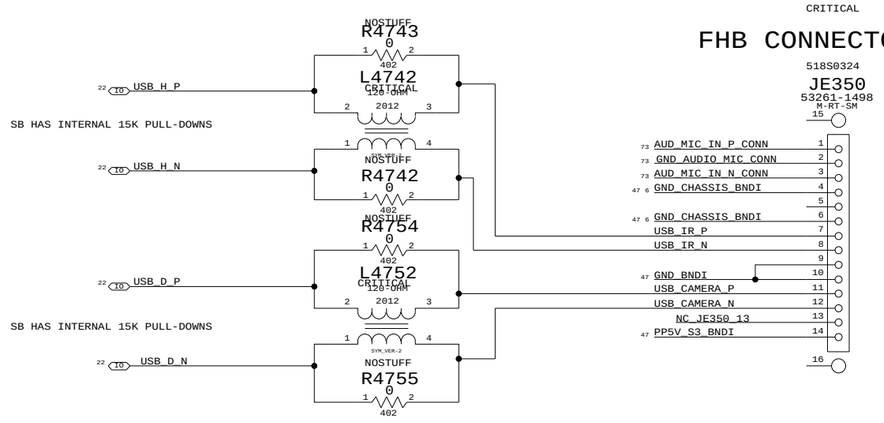


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

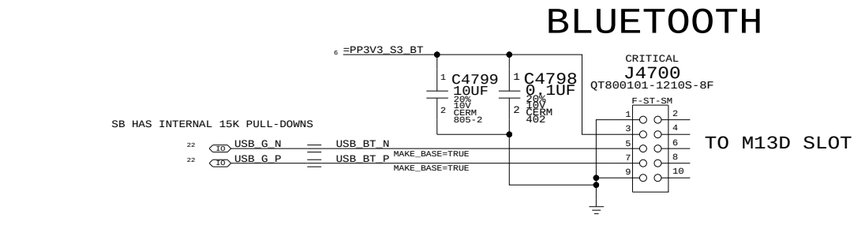


LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR JE350 PIN 14 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

PLACE C4742 CLOSED TO JE350.



BLUETOOTH



NOTE: STANDOFFS FOR J4700

SDF4700
STDOFF-40D4.5H-1.35-TH

SDF4701
STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6950	06
SCALE: NONE	SHT 47 OF 111	

BLANK

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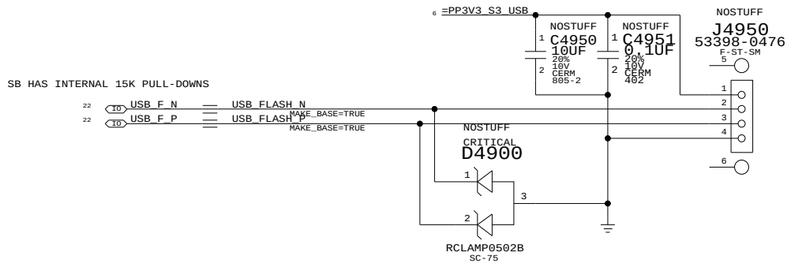
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	48 OF 111

CARD-READER USB CONN

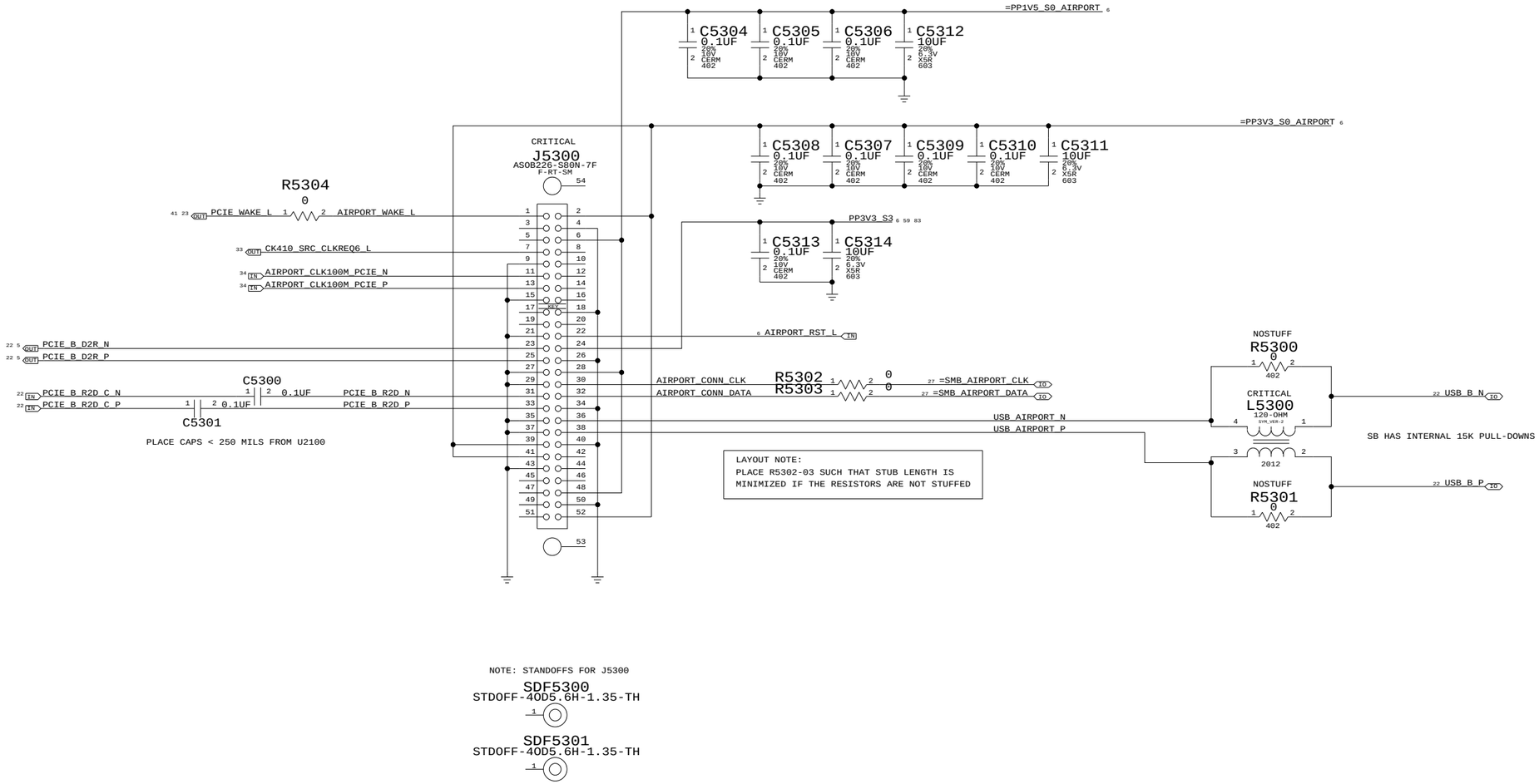


Flash Connector

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT
NONE	49 OF 111



AIRPORT CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE

SHT 53 OF 111

22 IN PCIE_C_R2D_C_N — TP_PCIE_C_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_C_R2D_C_P — TP_PCIE_C_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_C_D2R_N — TP_PCIE_C_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_C_D2R_P — TP_PCIE_C_D2R_P MAKE_BASE=TRUE

22 IN PCIE_D_R2D_C_N — TP_PCIE_D_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_D_R2D_C_P — TP_PCIE_D_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_D_D2R_N — TP_PCIE_D_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_D_D2R_P — TP_PCIE_D_D2R_P MAKE_BASE=TRUE

22 IN PCIE_E_R2D_C_N — TP_PCIE_E_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_E_R2D_C_P — TP_PCIE_E_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_E_D2R_N — TP_PCIE_E_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_E_D2R_P — TP_PCIE_E_D2R_P MAKE_BASE=TRUE

22 IN PCIE_F_R2D_C_N — TP_PCIE_F_R2D_C_N MAKE_BASE=TRUE
22 IN PCIE_F_R2D_C_P — TP_PCIE_F_R2D_C_P MAKE_BASE=TRUE

22 OUT PCIE_F_D2R_N — TP_PCIE_F_D2R_N MAKE_BASE=TRUE
22 OUT PCIE_F_D2R_P — TP_PCIE_F_D2R_P MAKE_BASE=TRUE

PCIE UNUSED PORTS

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 54 OF 111	

UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

23 OUT	PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	59	SMC_PM_G2_EN OUT
44 42 OUT	SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	59	SMC_ADAPTER_EN OUT
77 26 IN	ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22	SPI_ARB IN
76 IN	RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	63 22	SPI_SCLK IN
23 OUT	SMC_SB_NMI	B15	P14	P64/KIN4*	K13	63 22	SPI_SI OUT
23 OUT	PM_RSMRST_L	C14	P15	P65/KIN5*	K14	63 22	SPI_SO IN
75 OUT	IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	59	SMC_PROCHOT_3_3_L IN
23 OUT	PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	59	SMC_CPU_INIT_3_3_L IN
59	SMC_P20	D13	P20	P70/AN0	N12	76	SMC_CPU_ISENSE IN
59	SMC_P21	D14	P21	P71/AN1	R13	76	SMC_CPU_VSENSE IN
59	SMC_P22	D15	P22	P72/AN2	P13	59	SMC_GPU_ISENSE IN
59	SMC_P23	E12	P23	P73/AN3	R14	59	SMC_GPU_VSENSE IN
59 OUT	SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	76	SMC_DCIN_ISENSE IN
59 OUT	SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	76	SMC_PBUS_VSENSE IN
59	SMC_P26	E13	P26	P76/AN6	N13	59	SMC_BATT_ISENSE IN
59	SMC_P27	F14	P27	P77/AN7	P15	59	SMC_FWIRE_ISENSE IN
67 60 21 IO	LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23	SMC_WAKE_SCI_L IN
67 60 21 IO	LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	59	SMC_TPM_GPIO OUT
67 60 21 IO	LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	67 60 44 23 5	PM_CLKRUN_L IO
67 60 21 IO	LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	67 60 23	PM_SUS_STAT_L IN
67 60 21 IN	LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	59	SC_TX_L OUT
6 IN	SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	59	SC_RX_L IN
34 IN	PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	59	SMB_BSB_CLK IO
67 60 23 OUT	INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	59	SMC_ONOFF_L IN
59 OUT	SMC_XDP_TMS_L	A5	P40/TMI0	P91/IRQ1*	J2	59	SMC_BC_ACOK IN
59 OUT	SMC_XDP_TDI_L	B5	P41/TMO0	P92/IRQ0*	J1	59	SMC_BS_ALRT_L IN
59 IO	SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	88 79 77 23 6	PM_SLP_S3_L IN
59 OUT	SMC_TPM_PP	C3	P43/TMI1/EXSCK1	P94/IRQ13*	J4	77 23	PM_SLP_S4_L IN
59 OUT	SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	23	PM_SLP_S5_L IN
59 OUT	SMC_XDP_TCK	C2	P45	P96/EXCL	H1	59	SMC_SUS_CLK IN
59 OUT	SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	59	SMC_SMB_0_DATA IO
59 OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
60 59 5 OUT	SMC_TX_L	G1	P50				
60 59 5 IN	SMC_RX_L	G4	P51				
59 IO	SMC_SMB_0_CLK	F2	P52/SCL0				

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

21 OUT	SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	59	SMC_CASE_OPEN IN
60 22 IN	BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	60 59 5	SMC_TCK IN
26 23 5 IN	PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	60 59 5	SMC_TDI IN
67 59 OUT	SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	60 59 5	SMC_TDO OUT
59 14 IN	PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	60 59 5	SMC_TMS IN
23 10 IO	PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7		SMC_PF0 59
59 IO	SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6		SMC_PF1 59
23 OUT	PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	59	SMC_LID IN
23 IN	SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	59	SMC_CPU_RESET_3_3_L IN
23 OUT	SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	59	SMC_BATT_ISET OUT
59 IO	SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	59	SMC_BATT_VSET OUT
76 OUT	ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	59	SMC_SYS_ISET OUT
59 IN	SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	59	SMC_SYS_VSET OUT
59 OUT	SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	63 22	SPI_CE_L IO
59 IN	SMC_EXCARD_PWR_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	59	SMC_XDP_TCK_3_3 IN
59 IN	SMC_XDP_TDO_3_3_L	D11	PB7	PG2/EXIRQ10*/SDA2	N9	59	SMB_BSA_DATA IO
65 OUT	SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	59	SMB_BSA_CLK IO
66 65 OUT	SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	59	SMB_A_S3_DATA IO
66 65 OUT	SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	59	SMB_A_S3_CLK IO
59 OUT	SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	59	SMB_B_S0_DATA IO
65 IN	SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	59	SMB_B_S0_CLK IO
66 65 IN	SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	59	SMC_PROCHOT OUT
66 65 IN	SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	59	SMC_THRMTRIP OUT
59 IN	SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	59	SMC_FWE IN
59 IN	SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	59	ALS_GAIN OUT
59 IN	SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	26 23	SMS_INT_L OUT
59 IN	SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	59	SMS_ONOFF_L OUT
59 IN	SMC_ANALOG_ID	N11	PD3/AN11				
59 IN	SMC_NB_ISENSE	P10	PD4/AN12				
59 IN	SMC_MEM_ISENSE	R10	PD5/AN13				
59 IN	ALS_LEFT	N10	PD6/AN14				
59 IN	ALS_RIGHT	M10	PD7/AN15				

OMIT
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SMC_H8S2116
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G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

59 58 6 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
VCL IS INTERNAL RAIL
C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

59 58 6 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
85 76 59 58 GND_SMC_AVSS

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

AVCC1 N14, AVCC2 N15, VCC1 P2, VCC2 P1, VCC3 J15, VCC4 A1, VCC5 F1, VCL M14, AVREF M15
PP3V3_AVREF_SMC 59
59 58 6 =PP3V3_S5_SMC

60 59 IN SMC_RST_L E3 RES*
59 SMC_XTAL A2 XTAL
59 SMC_EXTAL B2 EXTAL

MD1 F2 — SMC_MD1 60
MD2 K1 — KBC_MDE
NMI F4 — SMC_NMI 60 IN
ETRST* L1 — SMC_TRST_L IN
AVSS P12, R12
VSS D1, P4, R4, F12, F13, B13, A13, A4, B4, D2

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
NOSTUFF
R5898 10K 5% 1/16W MF-LF 402
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800 SM
GND_SMC_AVSS 58 59 76 85

SMC

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 58 OF 111	

SMC RESET BUTTON

=PP3V3_S5_SMC

C5901 0.1uF 20% 10V CERM 402

CRITICAL U5900 RN5VD30A-F SOT23-5 VDD CD NC GND OUT

R5900 1K 5% 1/16W MF-LF 402

SMC_MANUAL_RST_L

DEVELOPMENT SW5900 SPST SM-LF

C5900 0.01UF 10% 16V CERM 402

SMC_RST_L

WHITE SYSLED

LED2901 WHITE-500MCD 3X2MM-SM

PP5V_S3

SYS_LED_DRV_K

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM

17_INCH_LCD

R5901 56.2 1% 1/16W MF-LF 402

SYS_LED_DRV_C

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

Q5900 FDV301N SOT23-LF

SMC_SYS_LED

NOSTUFF R5902 4.7K 5% 1/16W MF-LF 402

AMBIENT LIGHT SENSOR CONNECTOR

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

I2C ADDR:72(1001000)

CRITICAL J2901 53398-0476 F-ST-SM

PP3V3_S3

I2C_ALS_SDA

I2C_ALS_SCL

518S0328

SMC 3.3V -> CPU 1.05V SHIFTER

CPU_PROCHOT_L

Q5901 2N7002DW-X-F SOT-363

SMC_PROCHOT

PM_THRMTRIP_L

Q5901 2N7002DW-X-F SOT-363

SMC_THRMTRIP

POWER BUTTON HEADER

(REF DES PRESERVED FOR PLACEMENT PURPOSE)

J2903 53398-0276 M-ST-SM

POWER_BUTTON_L

518S0327

R5907

GENERATE 0.48V MID-VREF

SYS POWER BUTTON

SW5901 SPST SM-LF

R5907 1K 5% 1/16W MF-LF 402

SMC_ONOFF_L

C5902 0.1uF 20% 10V CERM 402

=PP3V3_S0_FAN

R5930 6.2K 5% 1/16W MF-LF 402

P0V48_SMC_LSREF

R5931 1K 5% 1/16W MF-LF 402

SMC CRYSTAL

LAYOUT NOTE: PLACE CAPACITORS BETWEEN CRYSTAL AND SMC/TPM

C5800 22PF CERM 5% 50V 402

SMC_XTAL

OMIT Y5800 20.000M SM-3

C5801 22PF CERM 5% 50V 402

SMC_EXTAL

TPM CRYSTAL

C6704 15PF 5% 50V CERM 402

TPM_XTALI

CRITICAL Y6700 32.768K SM-LF

C6705 15PF 402 50V 5% CERM

TPM_XTALO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL,20.00,80PPM,HC49,SMD,LF	Y5800	CRITICAL	

CPU 1.05V -> SMC 3.3V SHIFTER

PP3V3_S5

=PP3V3_S0_FAN

C5903 0.1UF 20% 10V CERM 402

R5932 1K 5% 1/16W MF-LF 402

P0V48_SMC_LSREF

U5999 LMV339 TSSOP GND

SMC_PROCHOST_3_3_L

CPU_PROCHOT_L

R5933 1K 5% 1/16W MF-LF 402

SMC_CPU_RESET_3_3_L

TP_U5999_P1

PCB: ENSURE FSB_CPURST_L FANS OUT FROM U1200 AND MINIMIZE ROUTE LENGTH TO U5999.

R5934 1K 5% 1/16W MF-LF 402

SMC_XDP_TCK_3_3

U5999 LMV339 TSSOP GND

TP_U5999_P13

XDP_TCK

R5935 1K 5% 1/16W MF-LF 402

SMC_XDP_TDO_3_3_L

XDP_TDO

U5999 LMV339 TSSOP GND

TP_U5999_P14

P0V48_SMC_LSREF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES,LF,MTL FILM,39.2 OHM,1%,402	R5901	20_INCH_LCD

SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS

SMC_P20	NC_SMC_P20
SMC_P21	NC_SMC_P21
SMC_P22	NC_SMC_P22
SMC_P23	NC_SMC_P23
SMC_P26	NC_SMC_P26
SMC_P27	NC_SMC_P27
SMC_BATT_ISET	NC_SMC_BATT_ISET
SMC_BATT_VSET	NC_SMC_BATT_VSET
SMC_SYS_ISET	NC_SMC_SYS_ISET
SMC_SYS_VSET	NC_SMC_SYS_VSET
SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L
SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN
SMC_ANALOG_ID	NC_SMC_ANALOG_ID
ALS_GAIN	NC_ALS_GAIN

DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS

SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED
SMC_PF0	TP_SMC_PF0
SMC_PM_G2_EN	TP_PM_G2_EN
SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN
ALS_LEFT	TP_ALS_LEFT
ALS_RIGHT	TP_ALS_RIGHT
SMC_PF1	TP_SMC_PF1
SMC_PB7	TP_SMC_PB7
SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN
SMC_PB7	TP_SMC_PB7
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL

TPM RESET PULLUP

PP3V3_TPM_3VSB

SMC_TPM_RESET_L R5827 10K

WIRE-OR DIMM OVERTEMP TO SMC

DIMM_OVERTEMP_L — PM_EXTTS_L<0>

SENSE GPU REGULATOR OUTPUT CURRENT

SMC_GPU_ISENSE — GPUVCORE_IOUT

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L
SMC_SUS_CLK	SUS_CLK_SB

NC OR PULLDOWN UNUSED ANALOG SENSE PINS

SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_NB_ISENSE	NC_SMC_NB_ISENSE
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE
SMC_BATT_ISENSE	UNUSED_SMC_SENSE
SMC_FWIRE_ISENSE	UNUSED_SMC_SENSE

UNUSED_SMC_SENSE — R5924 10K

PULLDOWN UNUSED ANALOG SENSE PINS ON PORT 7.

SMC PULL-UPS

=PP3V3_S5_SMC

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SMC_EXCARD_CP	R5830	10K
SMC_EXCARD_PWR_OC_L	R5831	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K

5% 1/16W MF-LF 402

NOT_DEVELOPMENT_SMC

DEVELOPMENT_SMC

SENSE GPU VCORE

PP1V0R1V2_S0_GPU — R5919 4.53K 1% 1/16W MF-LF 402 — SMC_GPU_VSENSE

C5919 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS

SELECT TPM GPIO

SMC_TPM_GPIO — R5920 0 — TPM_GPIO1

SMC_TPM_GPIO1

SMC_TPM_GPIO2

R5921 0 — TPM_GPIO2

SMC_TPM_PP R5995 0 5% 1/16W MF-LF 402

SMC_TPM_PP — TPM_PP

PRECISION 3.3V AVREF FOR SMC

PP5V_S5

R5942 10K 5% 1/16W MF-LF 402

Q5910 NTR4101P SOT-23

SMC_REF_GATE2

SMC_REF_GATE1

R5941 10K 5% 1/16W MF-LF 402

Q5911 2N7002 SOT23-LF

C5943 1UF 10% 6.3V CERM 402

TURN ON 3.3V VREF ONLY AFTER SMC 3.3V RAIL AND AVCC RAIL IS UP.

SMC_REF_IN

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDT=0.2 MM

NOSTUFF R5940 0 5% 1/16W MF-LF 402

=PP3V3_S5_SMC

CRITICAL U5940 REF3133 SOT23-3 IN TI OUT GND

PP3V3_AVREF_SMC

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

C5941 0.01UF 20% 16V CERM 402

C5940 0.47UF 20% 6.3V CERM-X5R 402

C5942 10UF 20% 6.3V X5R 603

GND_SMC_AVSS

MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V

SMC I2C BUS PULLUPS (INCLUDING UNUSED ONES)

PP3V3_S0

2.2K R5903 SMB_B_S0_CLK

2.2K R5904 SMB_B_S0_DATA

PP3V3_S3

2.2K R5905 SMB_A_S3_CLK

2.2K R5906 SMB_A_S3_DATA

=PP3V3_S5_SMC

10K R5910 SMB_BSB_CLK

10K R5911 SMB_BSB_DATA

10K R5912 SMC_SMB_0_CLK — TP_SMC_SMB_0_CLK

10K R5913 SMC_SMB_0_DATA — TP_SMC_SMB_0_DATA

10K R5914 SMB_BSA_CLK

10K R5915 SMB_BSA_DATA

PULLUPS FOR SYSTEM STATE PINS

10K R5916 SMC_LID

PULLDOWNS FOR SYSTEM STATE PINS

10K R5917 SMC_CASE_OPEN

ALIAS SENSORS INTO SMC I2C BUSSES

SMB_B_S0_CLK — =I2C_HD_TEMP_SCL

SMB_B_S0_DATA — =I2C_HD_TEMP_SDA

=I2C_ODD_TEMP_SCL

=I2C_ODD_TEMP_SDA

=SMB_THRM_CLK

=SMB_THRM_DATA

SMB_GPU_NB_THRM_CLK

SMB_GPU_NB_THRM_DATA

SMB_A_S3_CLK — I2C_ALS_SCL

SMB_A_S3_DATA — I2C_ALS_SDA

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

XW5900 SM

GND_NEXT_TO_SMC

SMC-CPU JTAG LEVEL-SHIFTER

XDP_TDI

(PULLUP ON CPU PAGE)

NOSTUFF Q5902 2N7002DW-X-F SOT-363

SMC_XDP_TDI_L

XDP_TMS

(PULLUP ON CPU PAGE)

NOSTUFF Q5902 2N7002DW-X-F SOT-363

SMC_XDP_TMS_L

=PP1V05_S0_CPU

SMC_XDP_TRST_L_R

NOSTUFF R5927 1K 5% 1/16W MF-LF 402

NOSTUFF Q5903 MMDT3904XF SOT-363-LF

SMC_XDP_TRST_L

(PULLDOWN ON ITP CONNECTOR PAGE)

R5927 VALUE SUBJECT TO CHANGE.

XDP_TRST_L

=PP1V05_S0_CPU

SMC_XDP_TCK_R

NOSTUFF R5925 1K 5% 1/16W MF-LF 402

NOSTUFF Q5903 MMDT3904XF SOT-363-LF

SMC_XDP_TCK

R5925 VALUE SUBJECT TO CHANGE.

(PULLDOWN ON CPU PAGE)

XDP_TCK

SMC & TPM SUPPORT

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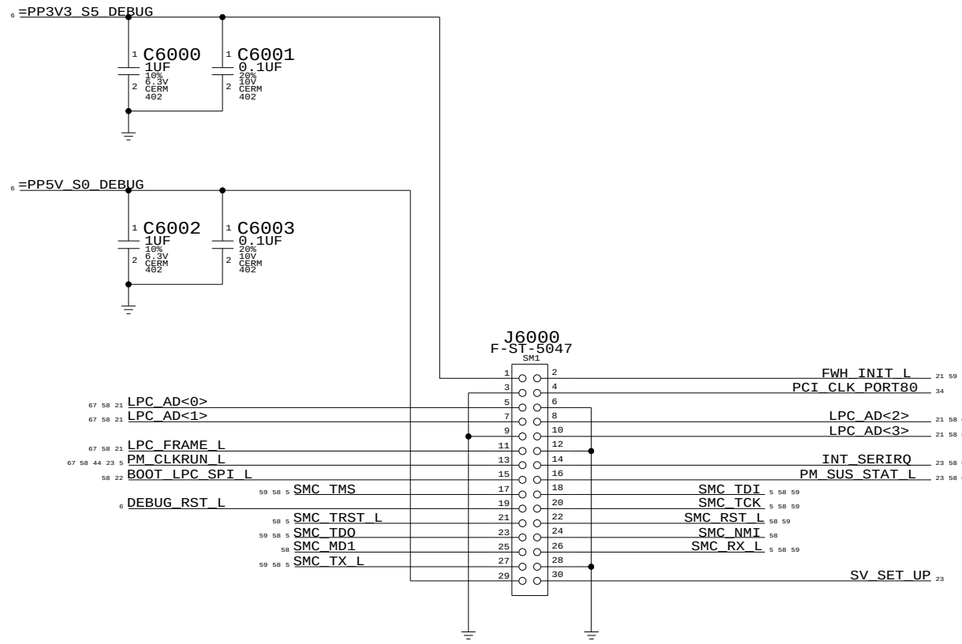
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 59 OF 111	



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

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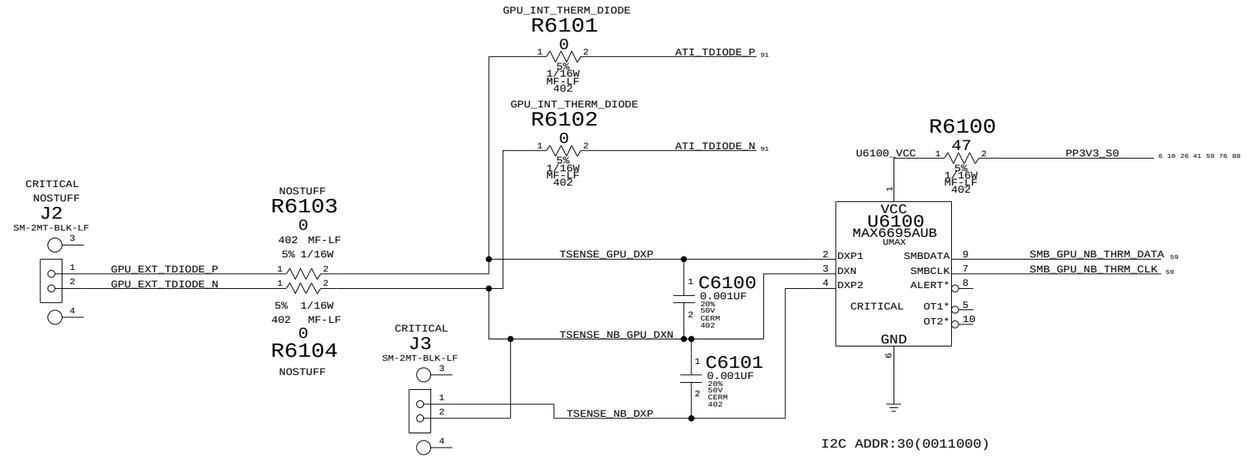
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE

SHT 60 OF 111



GPU+NB THERMAL

SYNC_MASTER=N/A SYNC_DATE=N/A

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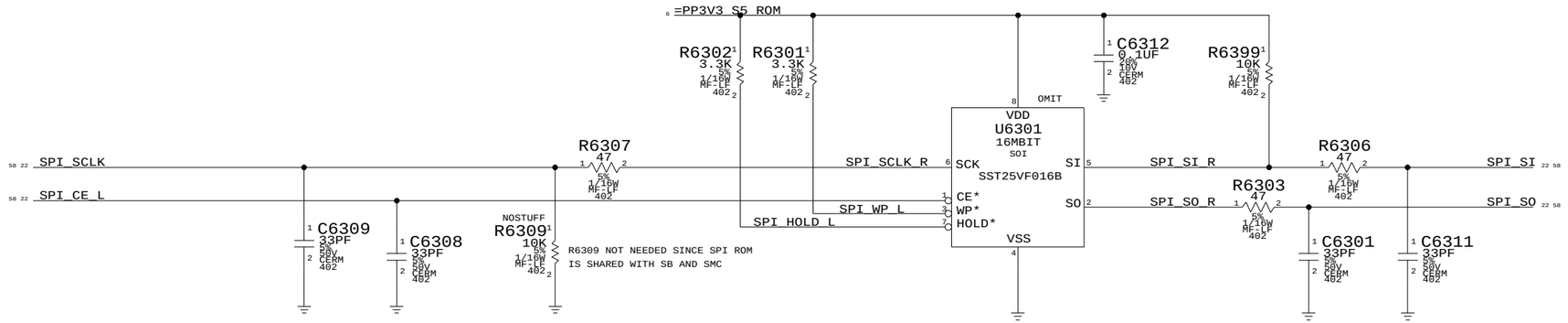
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE NONE

SHT 61 OF 111



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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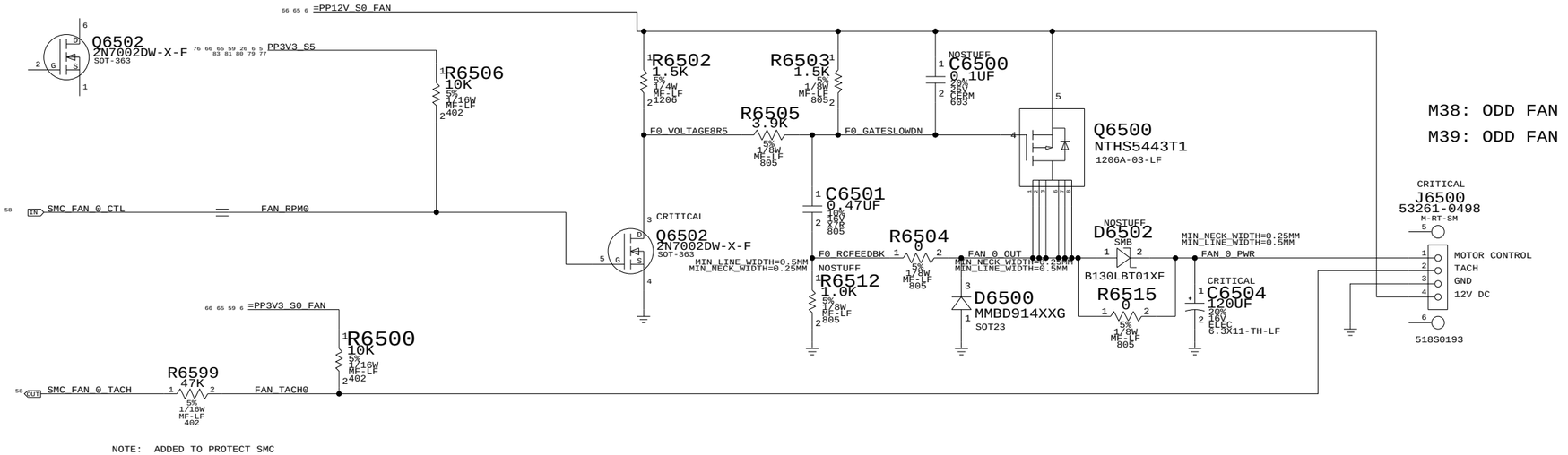
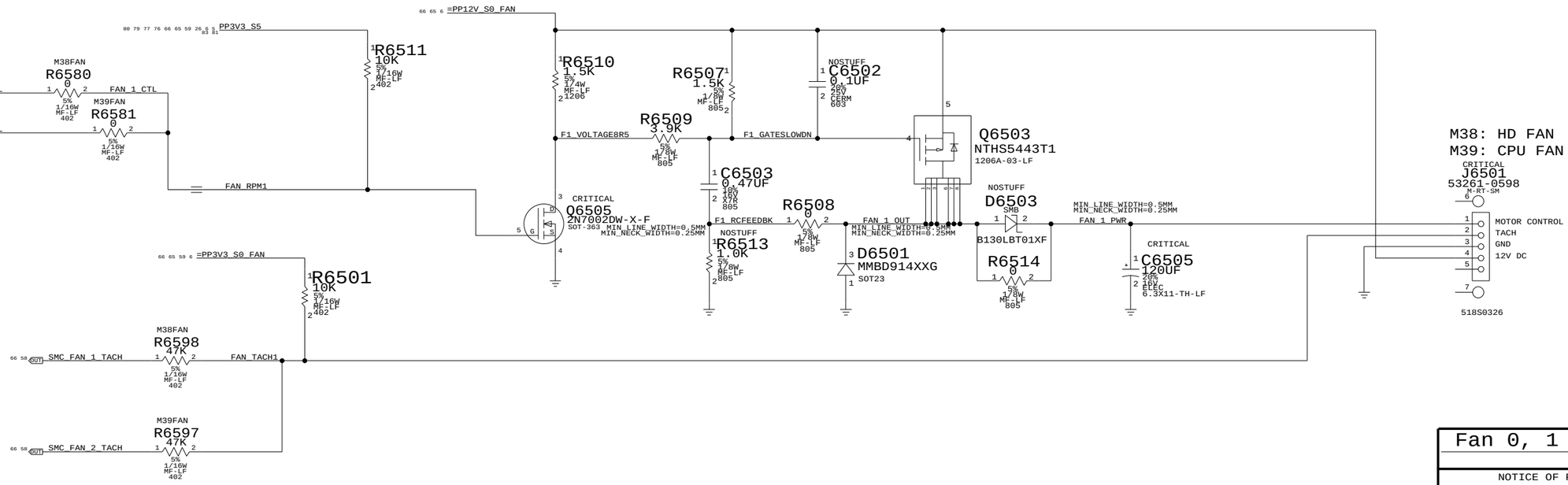
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 63 OF 111	

FAN 0



FAN 1



Fan 0, 1 & System Temp

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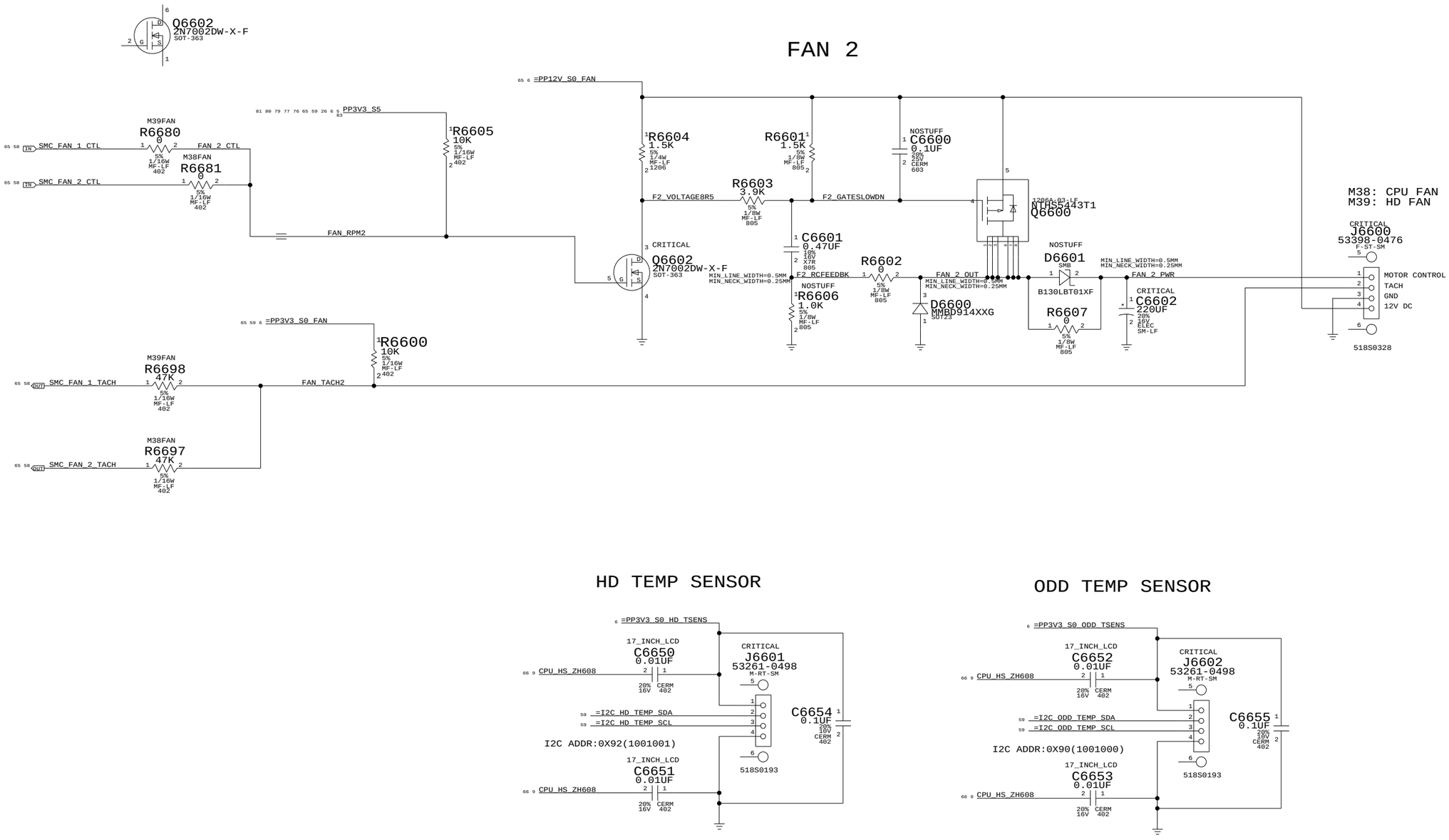
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 65 OF 111	

FAN 2



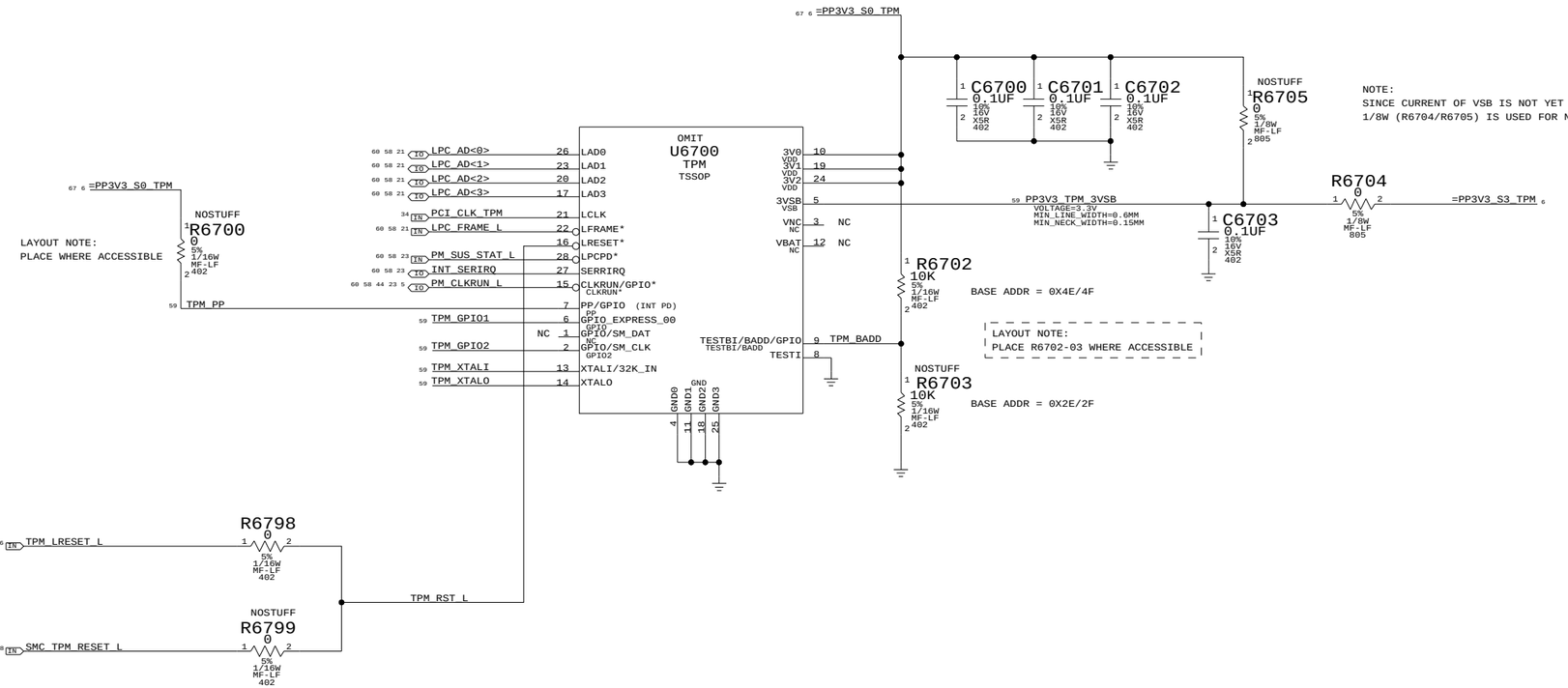
HD TEMP SENSOR

ODD TEMP SENSOR

Fan 2 & HD Temp

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 66 OF 111	



TPM

SYNC_MASTER=N/A SYNC_DATE=N/A

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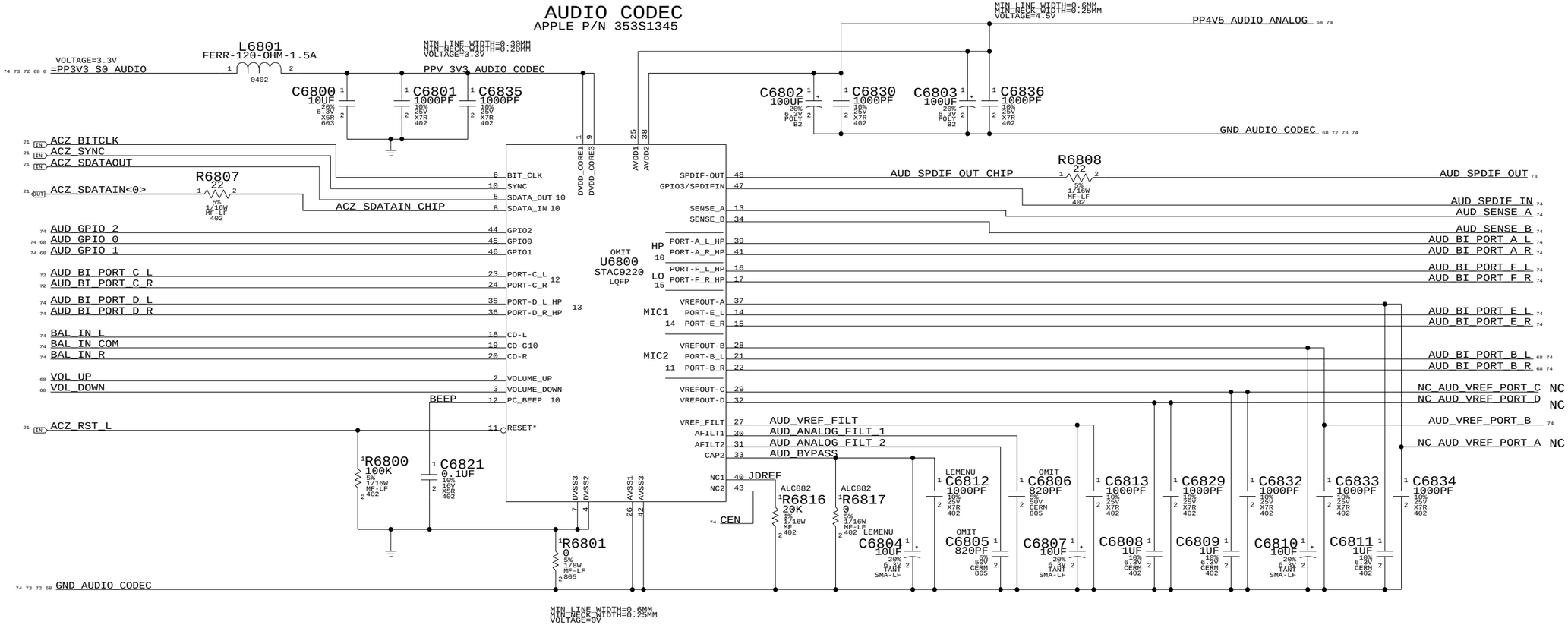
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

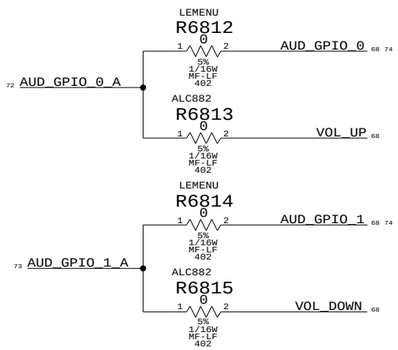
SCALE	SHT
NONE	67 OF 111

AUDIO CODEC
APPLE P/N 353S1345

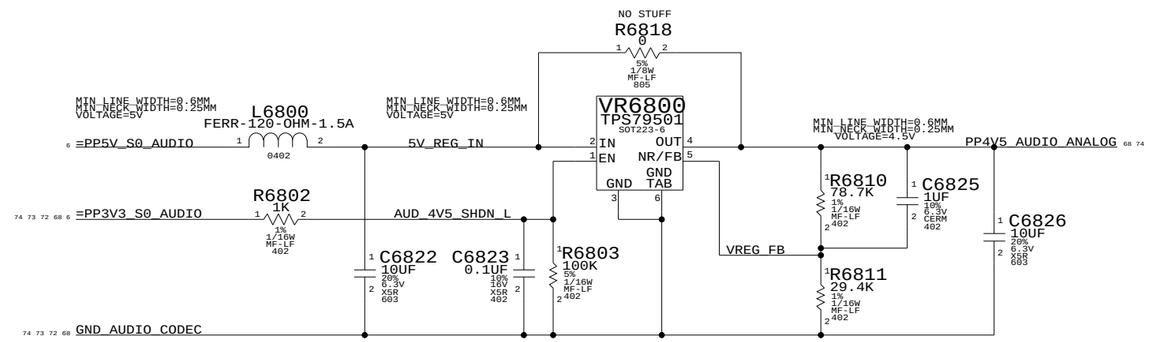


AUD_BI_PORT_B_L — AUD_BI_PORT_B_R

MIC INPUT TO BOTH L&R



4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233



AUDIO: CODEC		
SYNC_MASTER=FINO-SO	SYNC_DATE=04/28/2005	

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6790	??
	SCALE: NONE	SHT 68 OF 154	

SPEAKER AMP

APPLE P/N 353S0680

=PP12V_S0_AUDIO_SPKRAMP — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V

L7200 FERR-250-OHM (SM-1) → PP12V_AUD_SPKRAMP_PLANE (NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM, VOLTAGE=12V)

C7217 220UF 20% 16V ELEC 6.3X8-SM
C7200 220UF 20% 16V ELEC 6.3X8-SM
C7201 10UF 10% 16V CERM 1210
C7218 0.1UF 20% 16V CERM 603
C7202 1UF 10% 16V X7R 805
C7219 0.1UF 20% 16V CERM 603
C7203 10UF 10% 16V CERM 1210
C7223 10UF 10% 16V CERM 1210

GND_AUDIO_SPKRAMP_PLANE (74 72)

=PP3V3_S0_AUDIO (74 69 68 72 73)

AUD_BI_PORT_C_L (68) → L7205 1000-OHM-200MA (0603) → AUDSAMPINLN → C7204 0.47UF 10% 16V X7R 805 → AUD_SAMP_INL_N (9)
C7215 100PF 5% 50V CERM 402

AUD_BI_PORT_C_L (68) → L7206 1000-OHM-200MA (0603) → AUDSAMPINLP → C7205 0.47UF 10% 16V X7R 805 → AUD_SAMP_INL_P (10)

GND_AUDIO_CODEC (74 73 72 68) → L7207 1000-OHM-200MA (0603) → AUDSAMPINRP → C7206 0.47UF 10% 16V X7R 805 → AUD_SAMP_INR_P (16)
C7216 100PF 5% 50V CERM 402

AUD_BI_PORT_C_R (68) → L7208 1000-OHM-200MA (0603) → AUDSAMPINRN → C7207 0.47UF 10% 16V X7R 805 → AUD_SAMP_INR_N (15)

R7214 10K 1% 1/16W MF-LF 402 (=PP3V3_S0_AUDIO)

U7200 MAX9714 QFN-LF

VDD	3, 4, 21, 22	CHOLD	7
INL-	9	OUTL+	31, 32
INL+	10	OUTL-	29, 30
INR+	16	C1+	6
INR-	15	C1-	5
G1	17	OUTR+	27, 28
G2	18	OUTR-	25, 26
FS1	19	SS	12
FS2	20	THM	13
SHDN*	11	AGND PAD	33
NC	8	PGND	1, 2, 23, 24
REG	14		

AUD_SAMP_G1 (72), AUD_SAMP_G2 (72), AUD_SAMP_FS1 (72), AUD_SAMP_FS2 (72), AUD_SAMP_SHDN_L, NC, AUD_MAX9714_VREG

MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM, AUD_MAX9714_CHOLD

AUDSAMPOUTLP (NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM) → L7201 180-OHM-1.5A (0603) → AUD_SPKR_OUTL_P (73)

AUDSAMPOUTLN (NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM) → L7202 180-OHM-1.5A (0603) → AUD_SPKR_OUTL_N (73)

AUDSAMPCPP (MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM) — C7208 0.1UF 10% 50V X7R 603-1 — AUDSAMPCPN (MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM)

AUDSAMPOURTP (NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM) → L7203 180-OHM-1.5A (0603) → AUD_SPKR_OUTR_P (73)

AUDSAMPOUTRN (NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM) → L7204 180-OHM-1.5A (0603) → AUD_SPKR_OUTR_N (73)

SPKRAMP_SS (MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM)

C7210 1000PF 10% 25V X7R 402
C7211 1000PF 10% 25V X7R 402
C7212 1000PF 10% 25V X7R 402
C7213 1000PF 10% 25V X7R 402

C7209 0.47UF 10% 16V X7R 805

XC7200 50MIL28

XW7201 SM OMIT — NET SPACING TYPE=AUDIO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM → GND_AUDIO_SPKRAMP (6 74)

GND_AUDIO_SPKRAMP_PLANE (72 74)

R7215 10K 5% 1/16W MF-LF 402 (=PP3V3_S0_AUDIO) → PP3V3_INTERCON

NOSTUFF R7216 0 5% 1/16W MF-LF 402 → SPKRAMP_MUTE

R7217 0 5% 1/16W MF-LF 402 (SPKRAMP_MUTE → SPKRAMP_SS)

AUD_GPIO_0_A (68) → R7213 47K 5% 1/16W MF-LF 402 → AUD_DEBOUNCE

R7212 15K 5% 1/16W MF-LF 402 — C7220 100PF 5% 50V CERM 402

C7221 100PF 5% 50V CERM 402

Q7200 2N7002DW-X-F SOT-363 (D, G, S)

Q7200 2N7002DW-X-F SOT-363 (D, G, S)

GND_AUDIO_SPKRAMP_PLANE (74 72)

C7214 1UF 10% 25V X5R 603

GND_AUDIO_CODEC (74 73 72 68)

NOSTUFF R7219 0 5% 1/16W MF-LF 402

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_S0_AUDIO (74 73 72 68 6) → RP7200 47K 5% 1/16W SM-LF (8 7 6 5 / 1 2 3 4)

AUD_SAMP_FS2 (72)
AUD_SAMP_FS1 (72)
AUD_SAMP_G2 (72)
AUD_SAMP_G1 (72)

NOSTUFF R7218 0 5% 1/16W MF-LF 402

R7208 0 5% 1/16W MF-LF 402

GND_AUDIO_SPKRAMP_PLANE (74 72)

AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

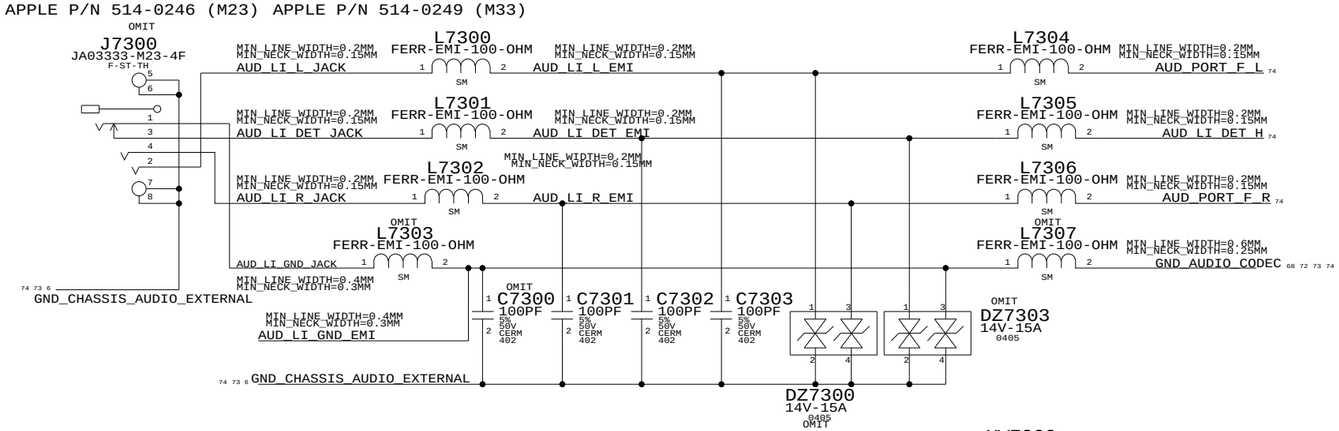
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	??

SCALE	SHT	OF
NONE	72	154

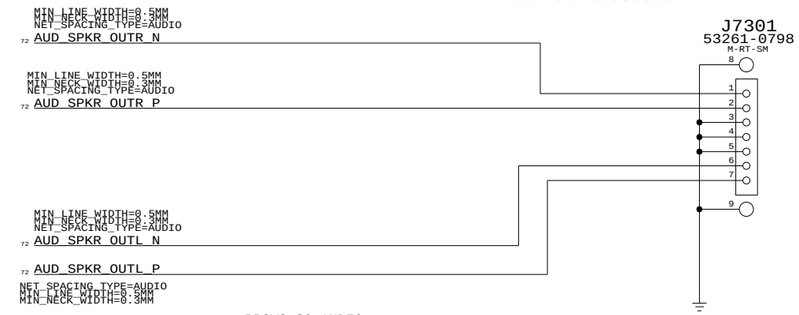
LINE IN JACK

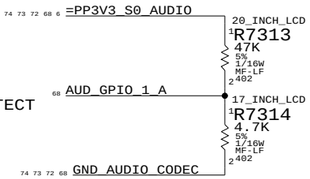
APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)



SPEAKER CABLE CONNECTOR

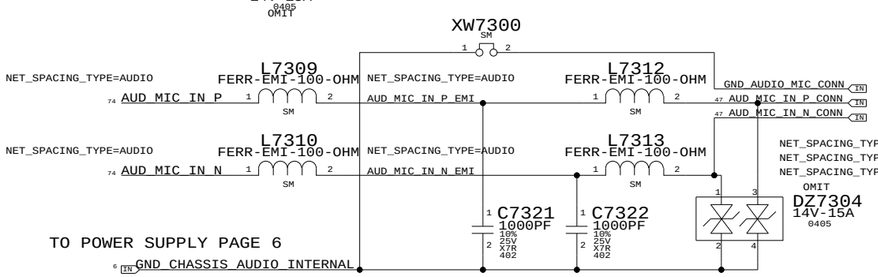
APPLE P/N 518S0325





TO GPIO 1
SPEAKER TYPE DETECT

AUD_GPIO_1_A



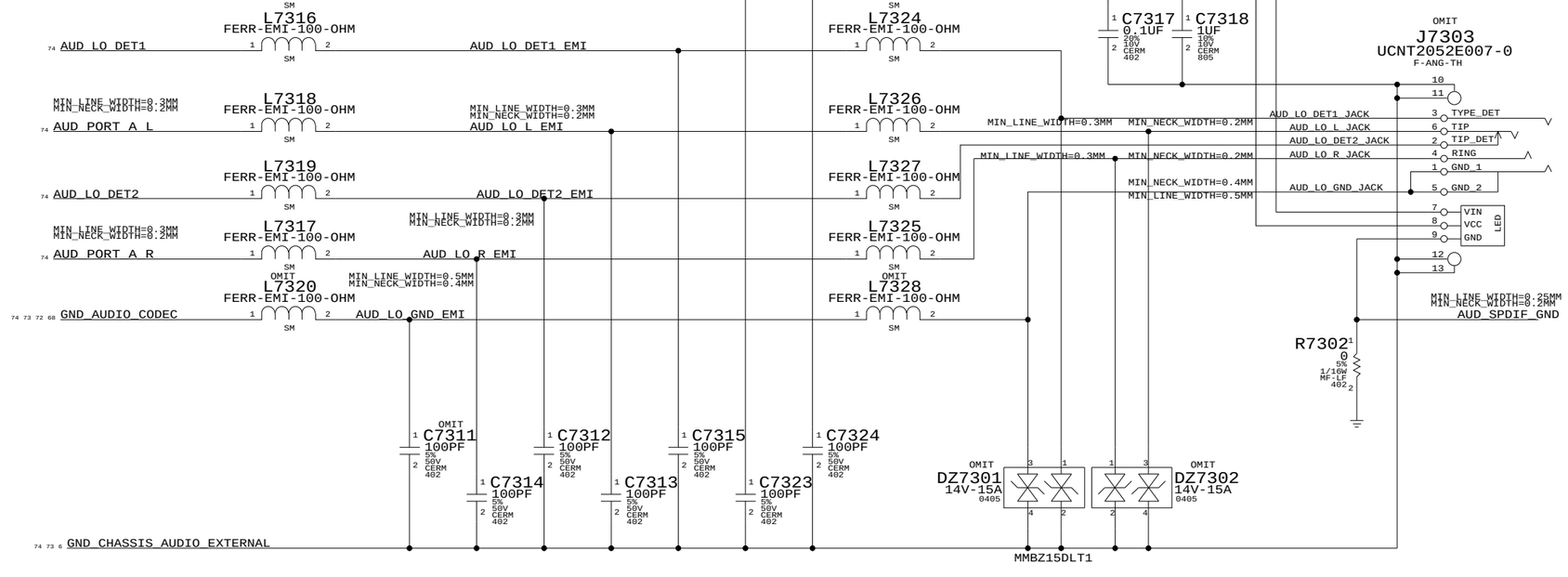
TO FHB CONNECTOR PAGE 47

TO POWER SUPPLY PAGE 6

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	J7300	CRITICAL	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 5.5 DEG	J7303	CRITICAL	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 4.5 DEG	J7300	CRITICAL	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	J7303	CRITICAL	20_INCH_LCD
353S1345	1	SIGMATEL STAC9220	U6800	CRITICAL	LEMENU
353S1268	1	REALTEK ALC882	U6800	CRITICAL	ALC882
131S8223	2	CAPACITOR, 820PF	C6805,C6806	CRITICAL	LEMENU
131S0534	2	CAPACITOR, 1UF	C6805,C6806	CRITICAL	ALC882
377S0043	5	TRANSIENT VOLTAGE DIODE	DZ7300,DZ7301,DZ7302,DZ7303,DZ7304	CRITICAL	
113S0022	4	RESISTOR, 0 OHM, 0603	L7303,L7307,L7320,L7328		
116S0004	2	RESISTOR, 0 OHM, 0402	C7300,C7311		

LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)



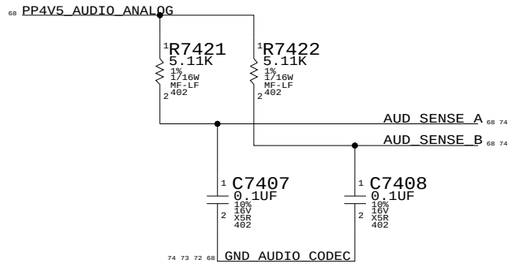
AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	??
SCALE: NONE	SHT 73 OF 154	

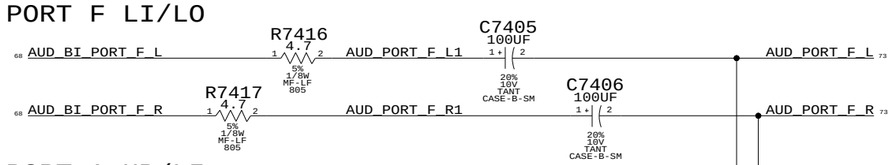
JACK SENSE PULL UPS(PLACE NEXT TO CODEC)



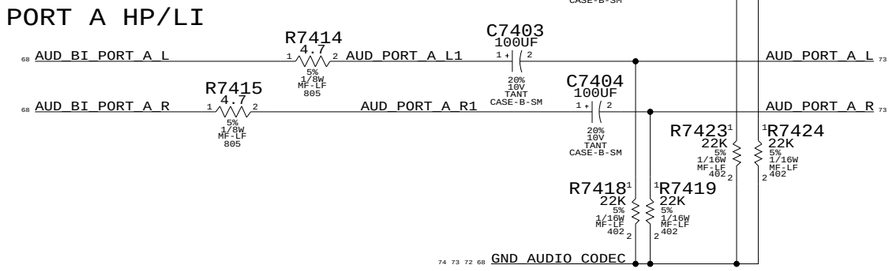
USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E
PORT D

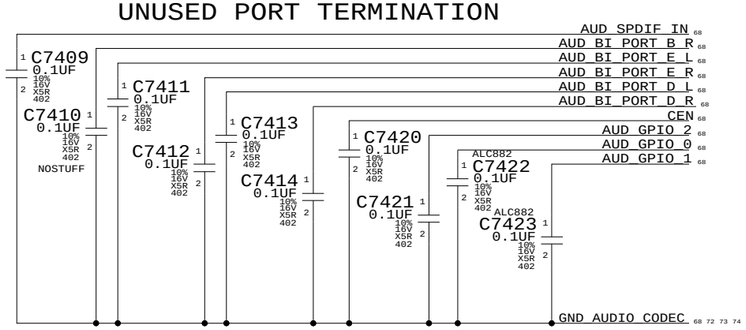
PORT F LI/LO

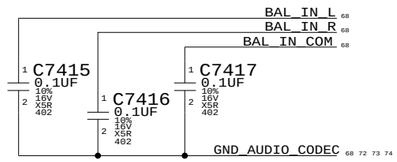


PORT A HP/LI

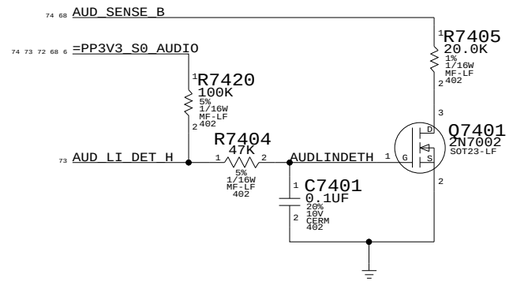


UNUSED PORT TERMINATION

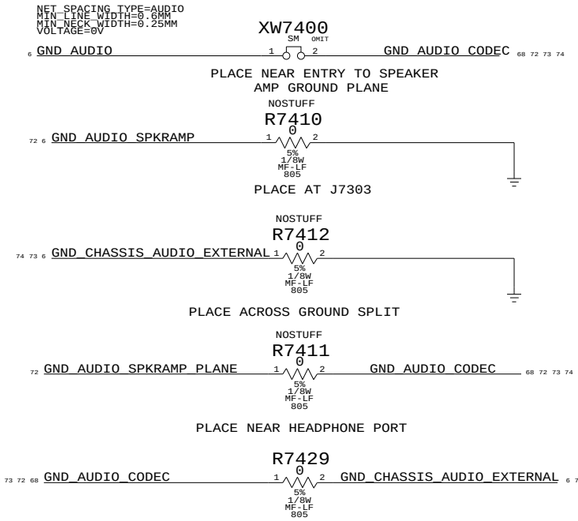




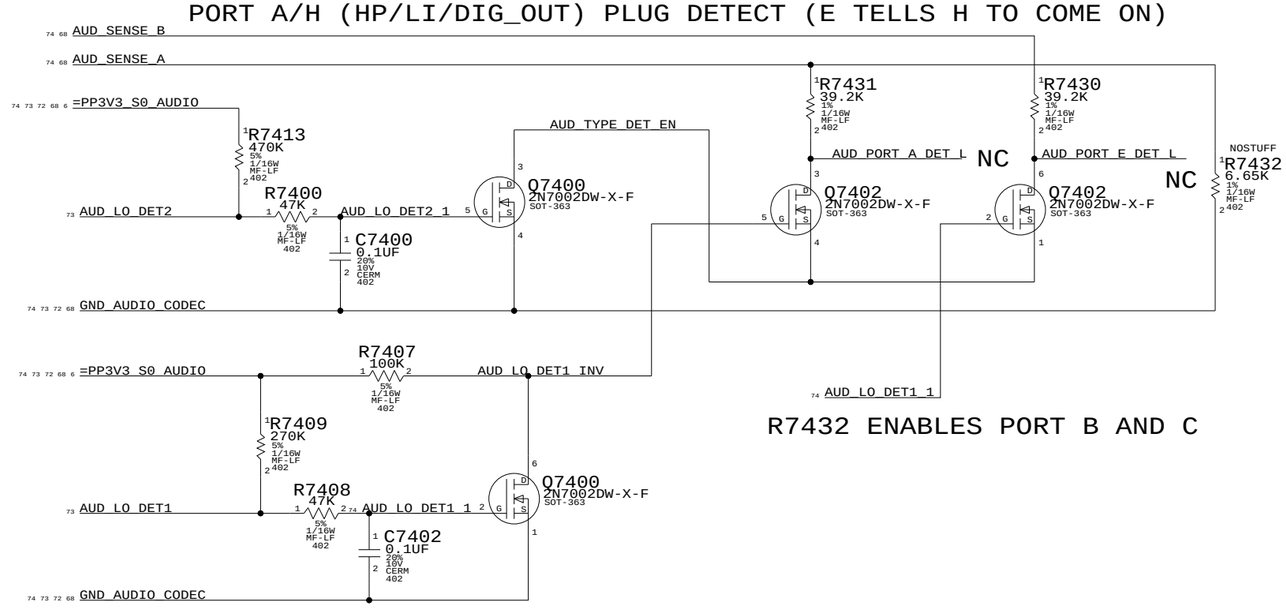
PORT F (LI/LO) PLUG DETECT



AUDIO GROUND RETURNS

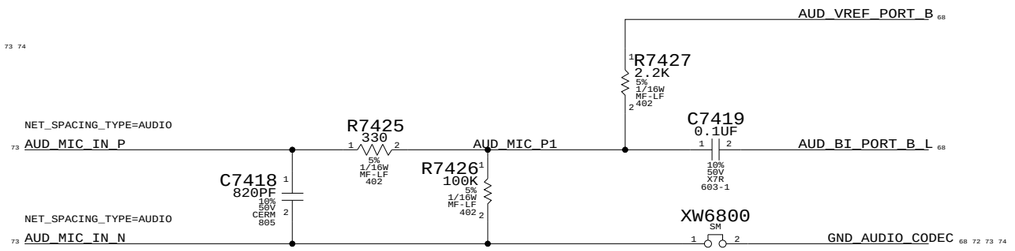


PORT A/H (HP/LI/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



R7432 ENABLES PORT B AND C

MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	??
SCALE: NONE	SHT 74	OF 154

IMVP6 CPU VCORE REGULATOR

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

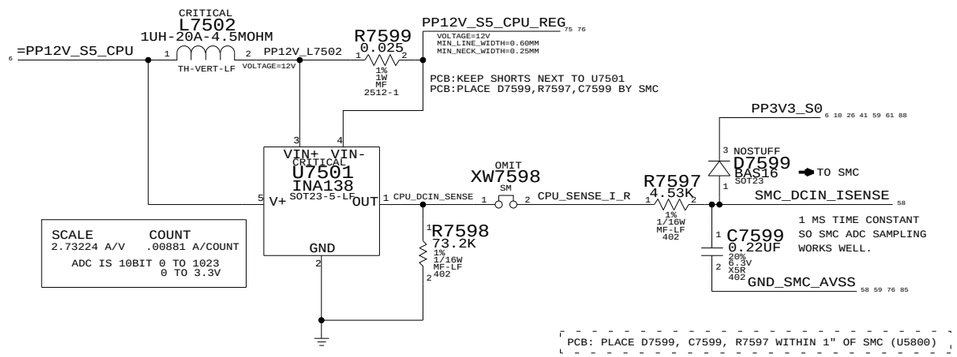
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator	
SYNC_MASTER=POWER	SYNC_DATE=07/08/2005

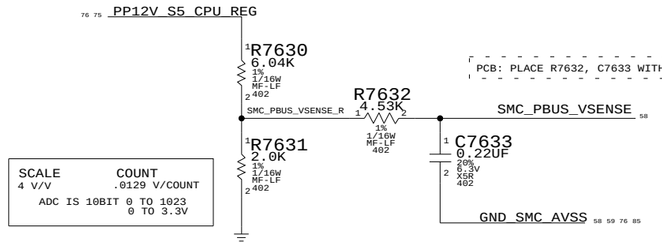
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 75 OF 111	

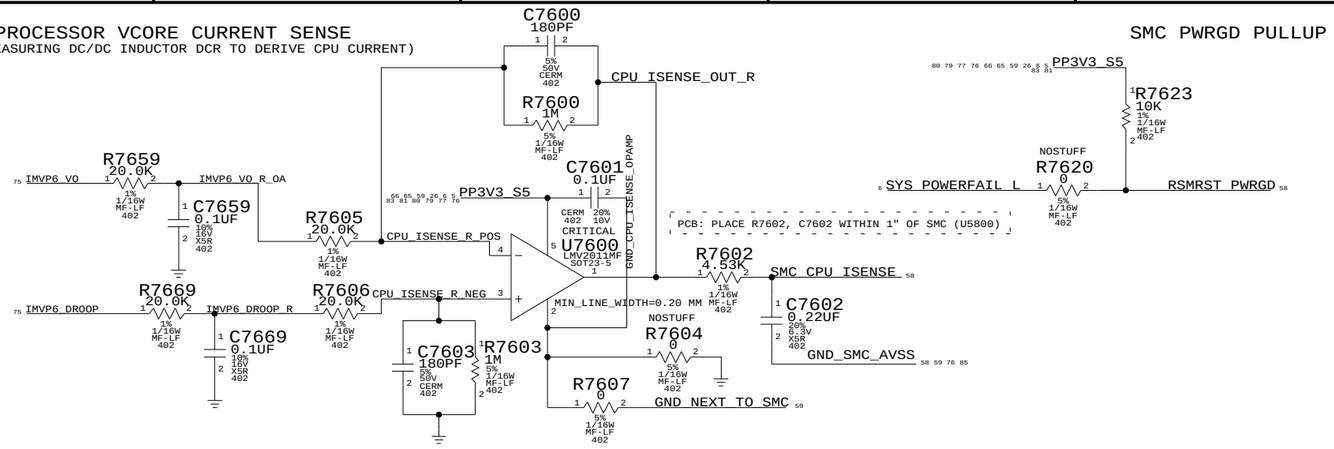
PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



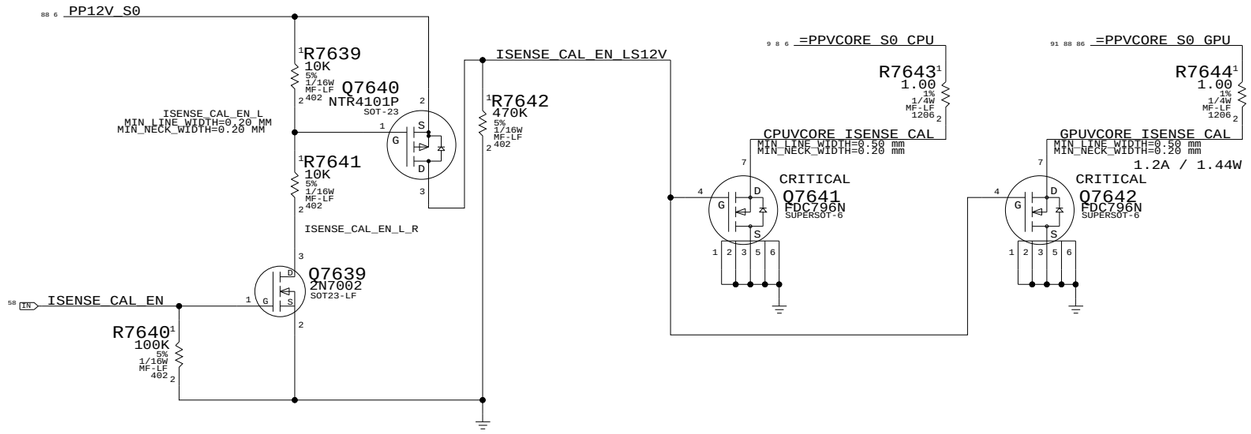
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)



PROCESSOR VCORE SENSE

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

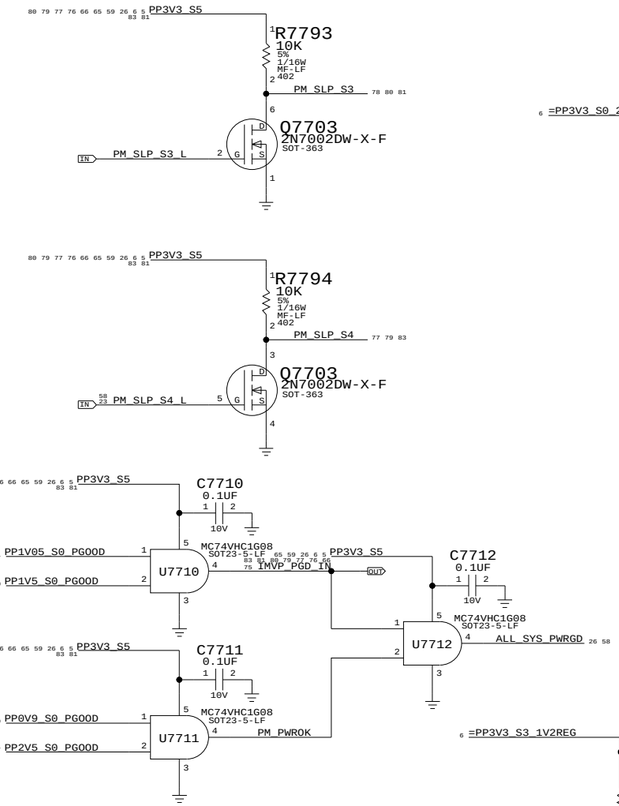


CPU SENSE CIRCUITRIES

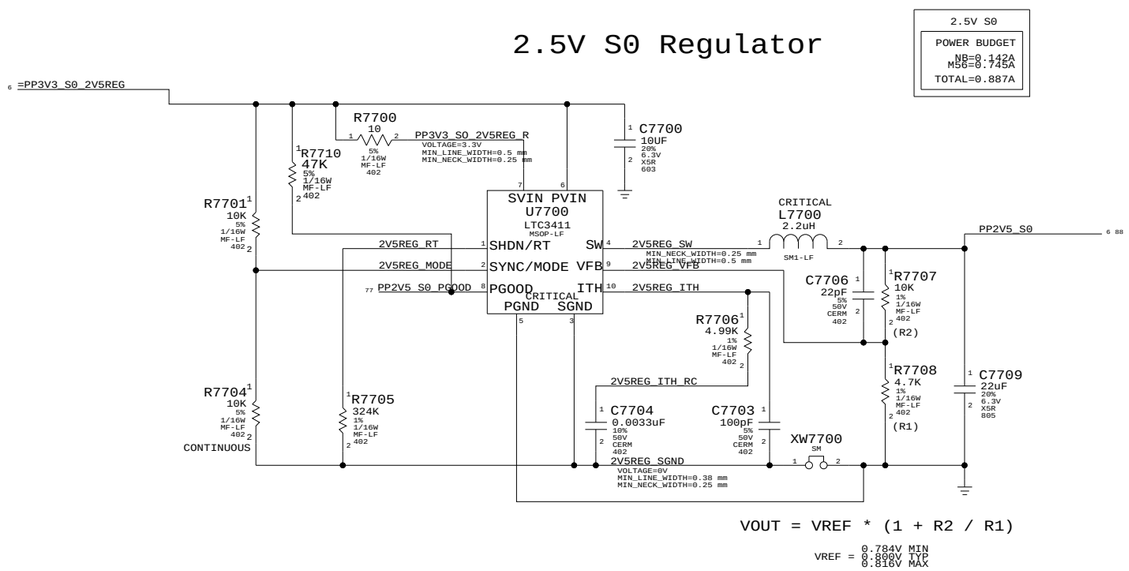
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

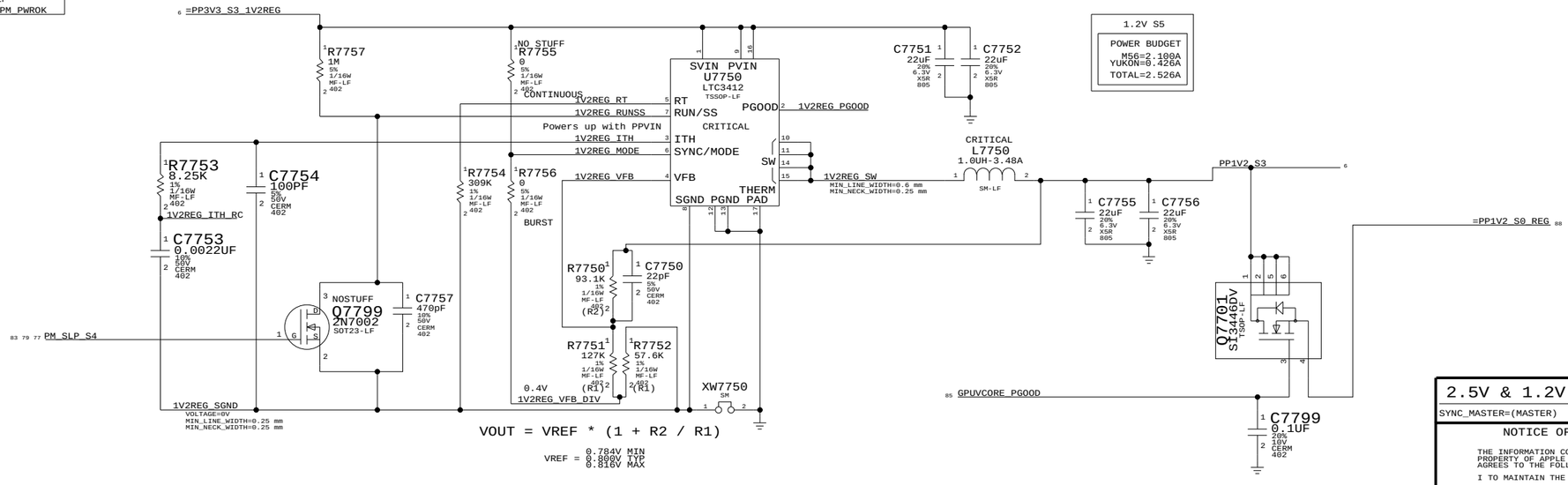
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 76 OF 111	



2.5V S0 Regulator



1.2V S3 REGULATOR / 1.2V S0 FET



2.5V & 1.2V GRAPHICS REGULATORS

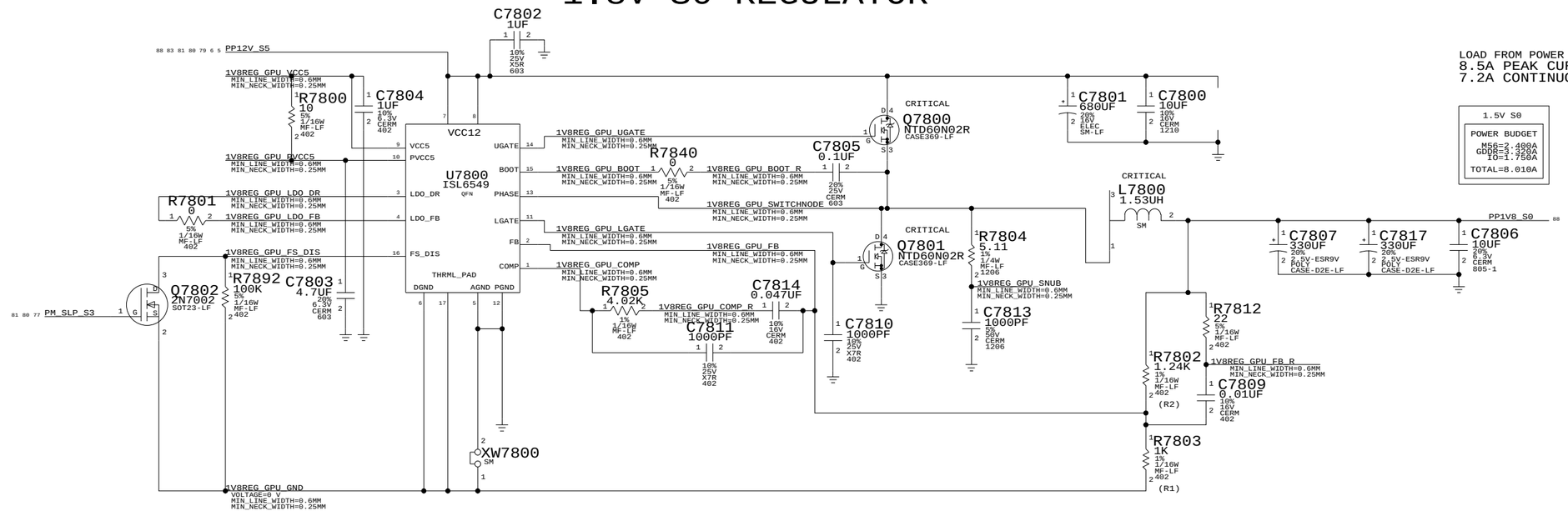
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 77 OF 111	

PAGE_BORDER=TRUE

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0

POWER BUDGET
M56=2.400A
GDDR=3.780A
IO=1.750A
TOTAL=8.010A

VOUT=VREF*(1+R2/R1)

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.8V GDDR REGULATOR

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

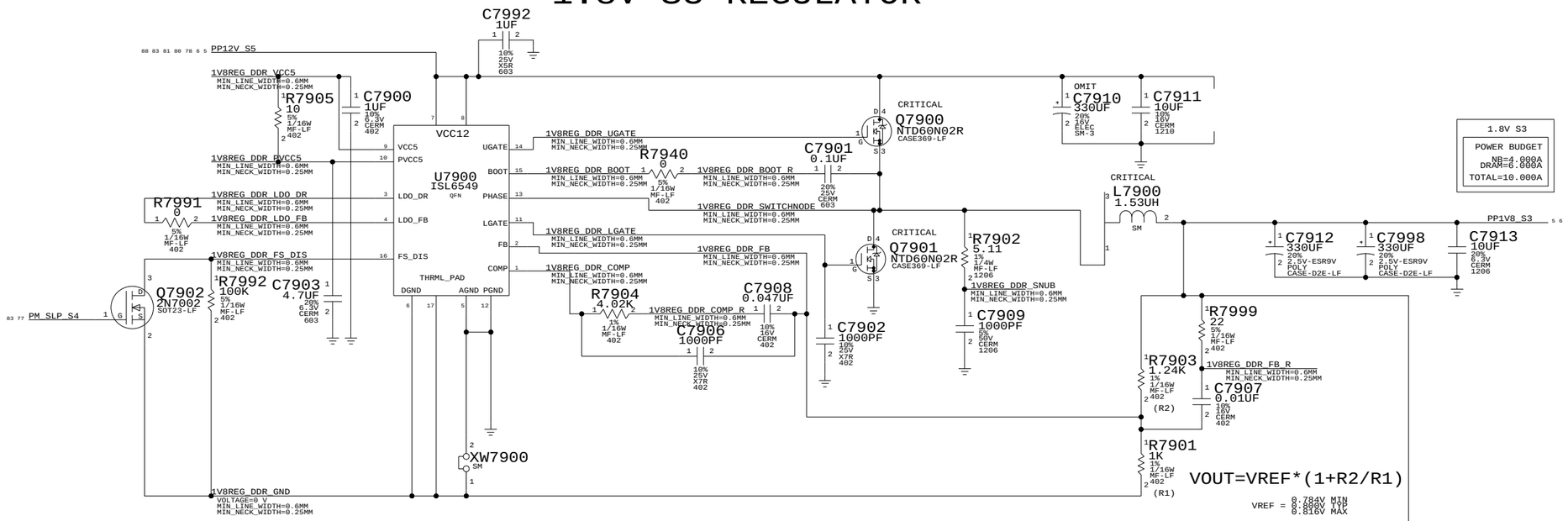
SIZE	DRAWING NUMBER	REV.
D	051-6949	09

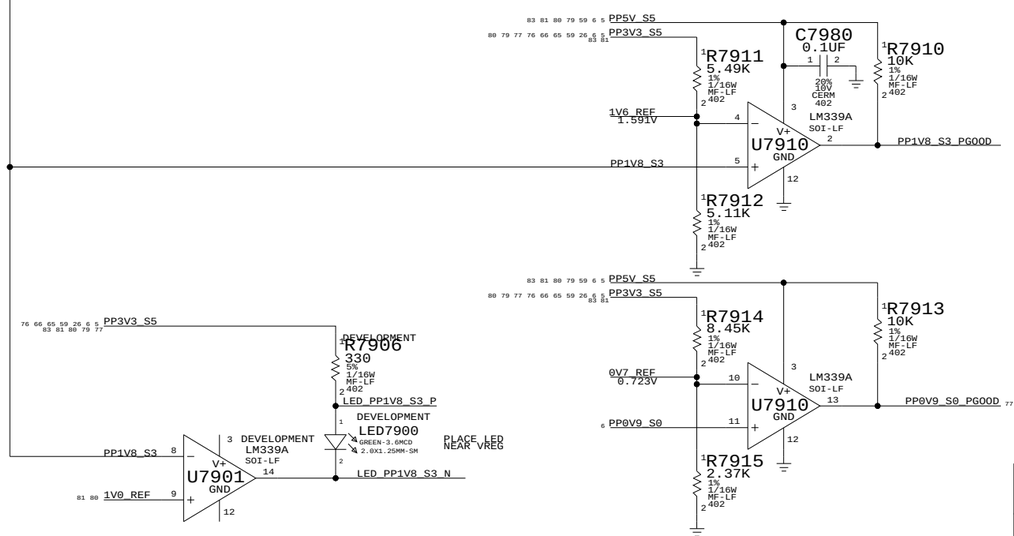
SCALE: NONE

SHT 78 OF 111

TRUE

1.8V S3 REGULATOR





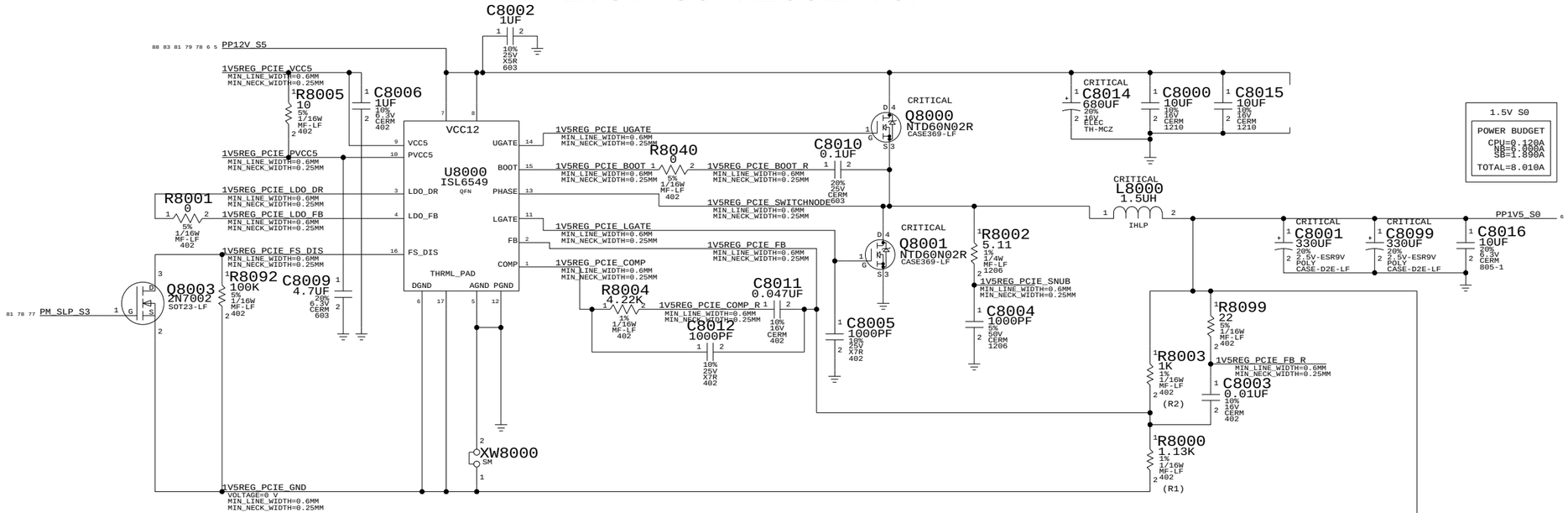
1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 79 OF 111	

1.5V S0 REGULATOR



1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005

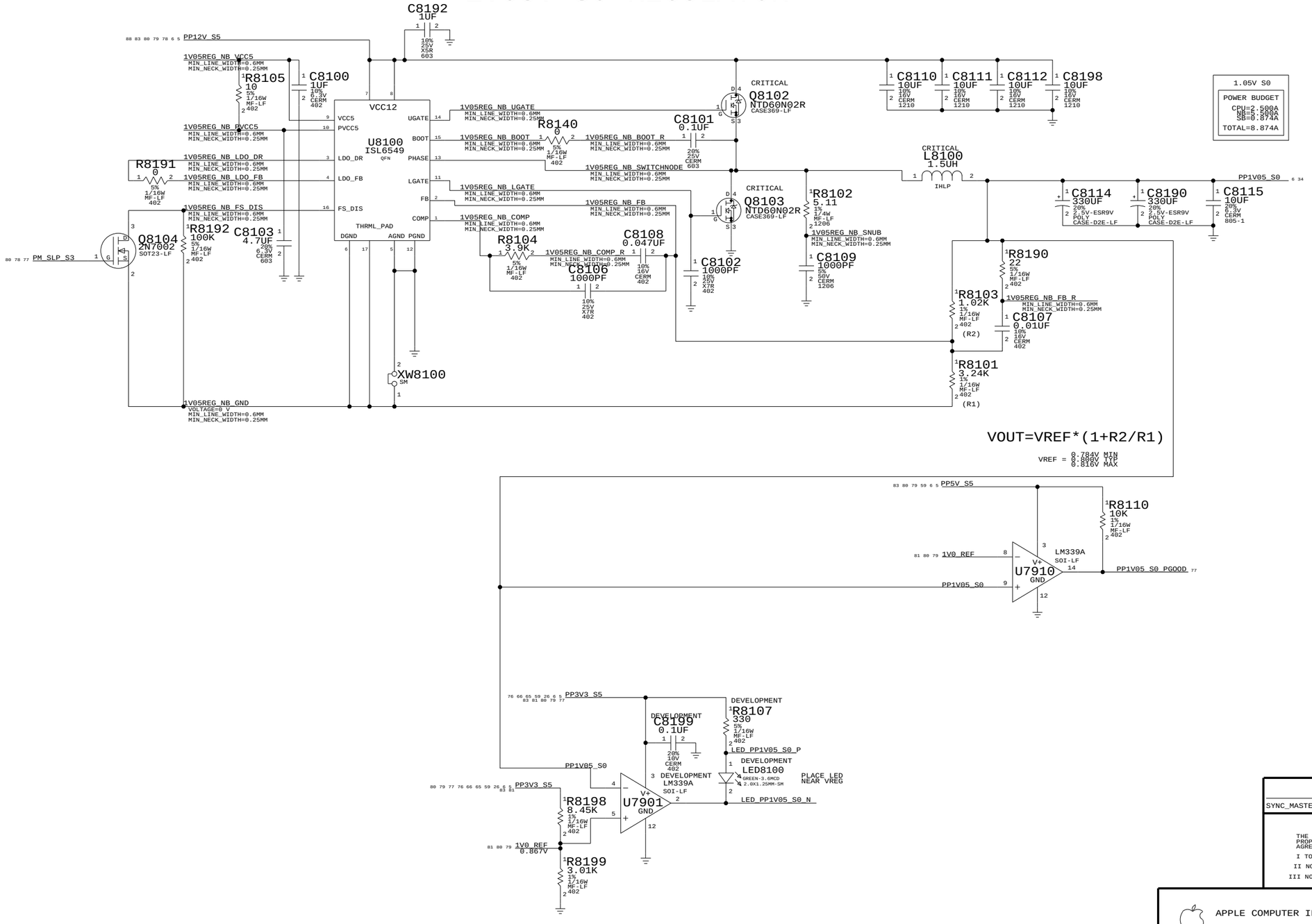
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6950	06

SCALE: NONE

SHT 80 OF 111

1.05V S0 REGULATOR



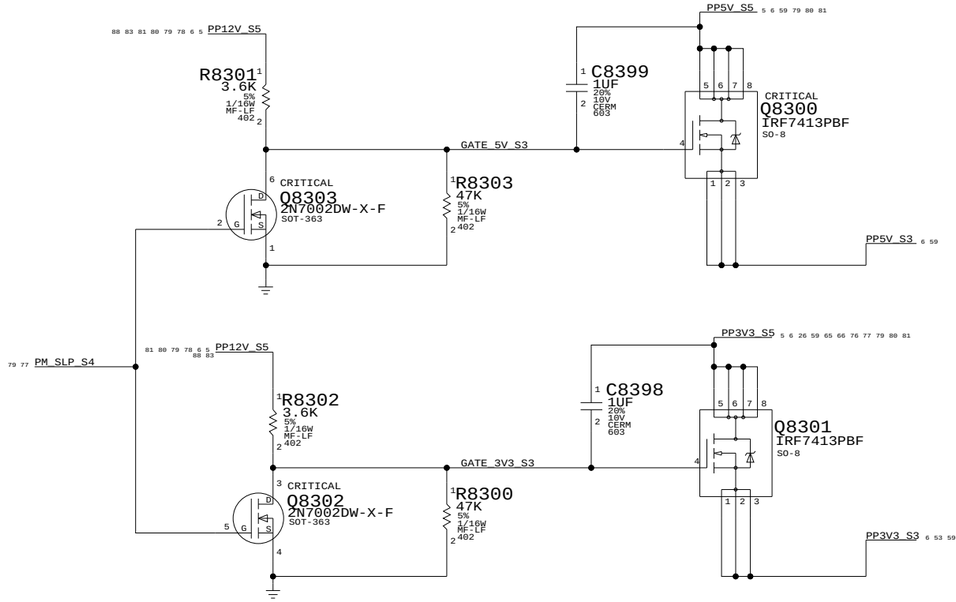
1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE SHT 81 OF 111



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

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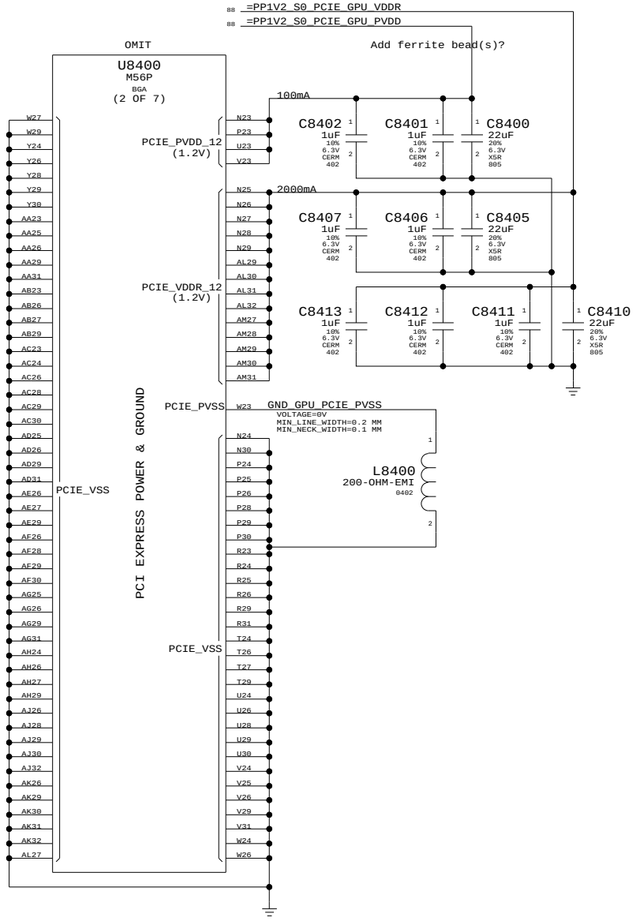
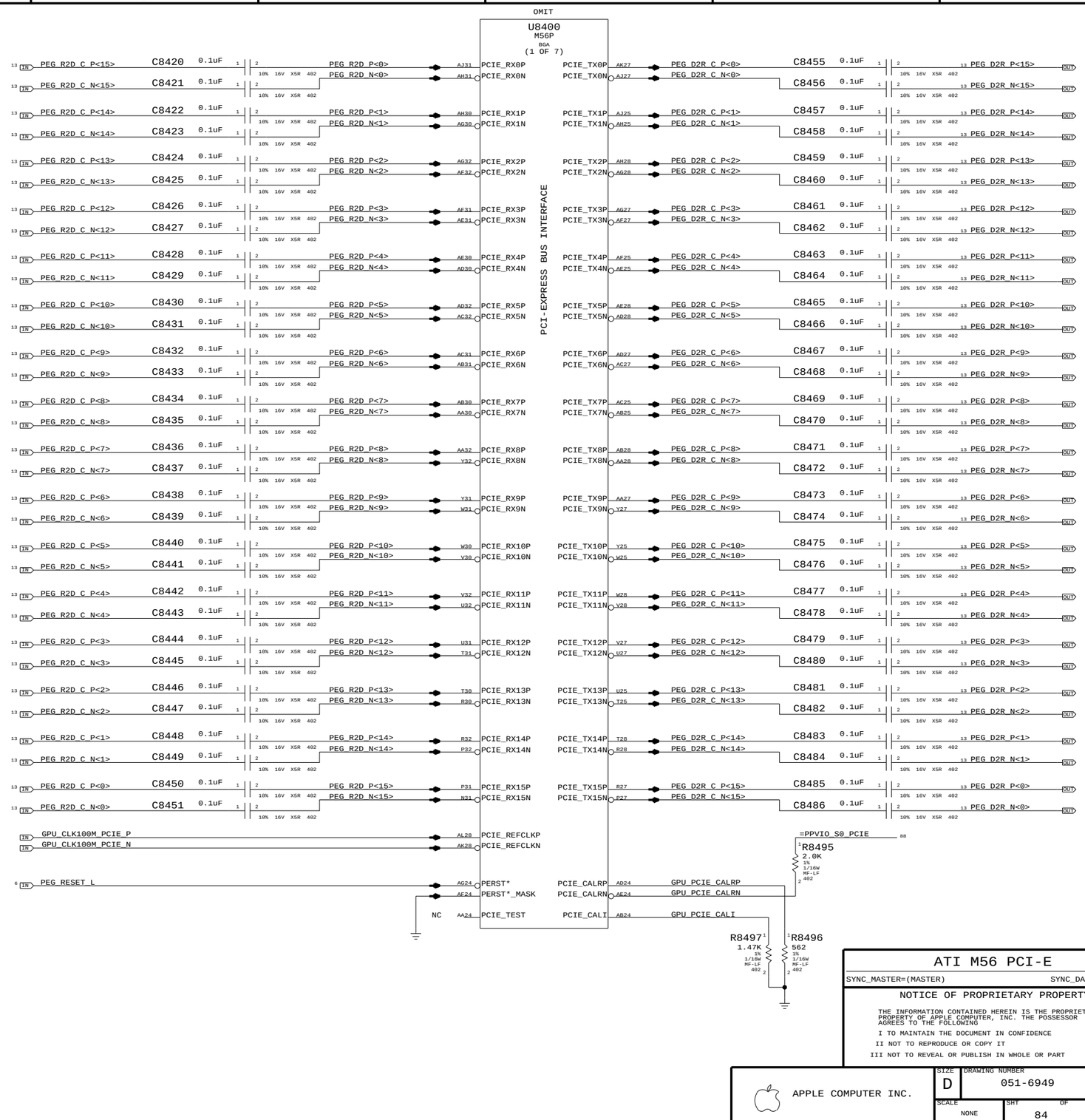
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE: NONE SHT 83 OF 111





ATI M56 PCI-E

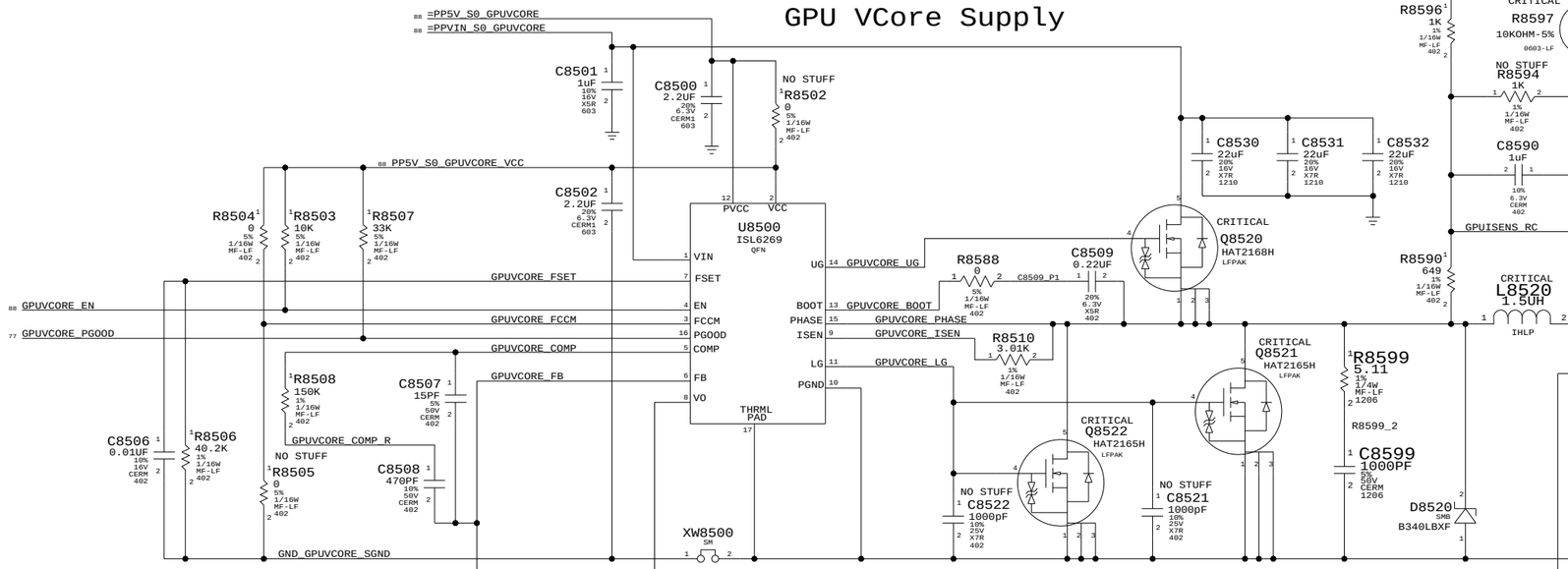
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	84	111

GPU VCore Supply

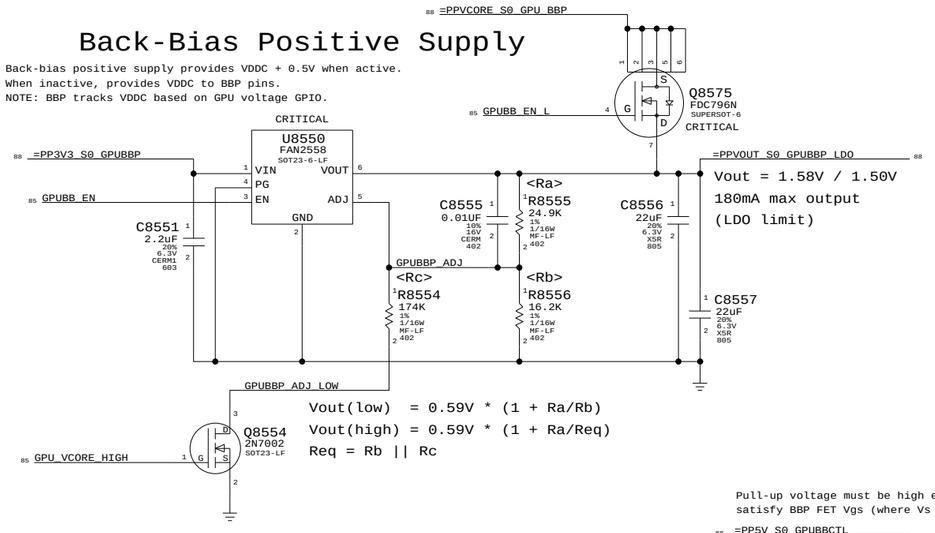


GPU VCore Current Sense

Vout(low) = 0.6V * (1 + Ra/Rb)
Vout(high) = 0.6V * (1 + Ra/Req)
Req = Rb || Rc

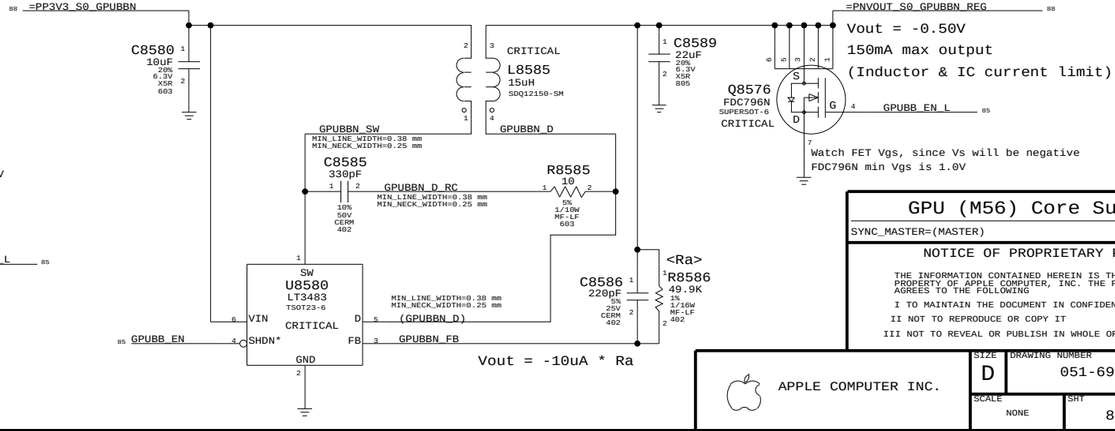
Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



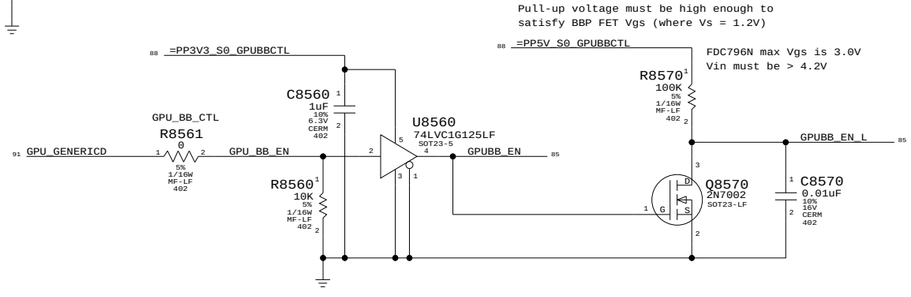
Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active.
When inactive, provides VSS to BBN pins.

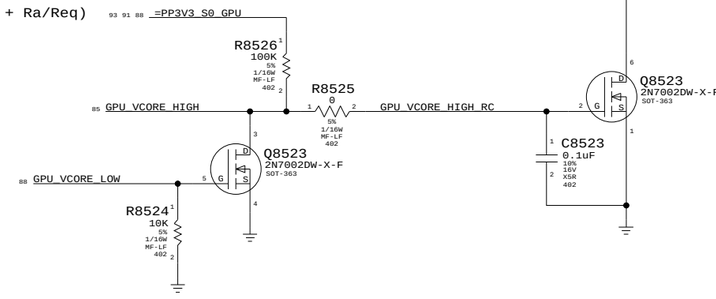


Back-Bias Pull-up Supply

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)



Back-Bias Positive Supply



GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

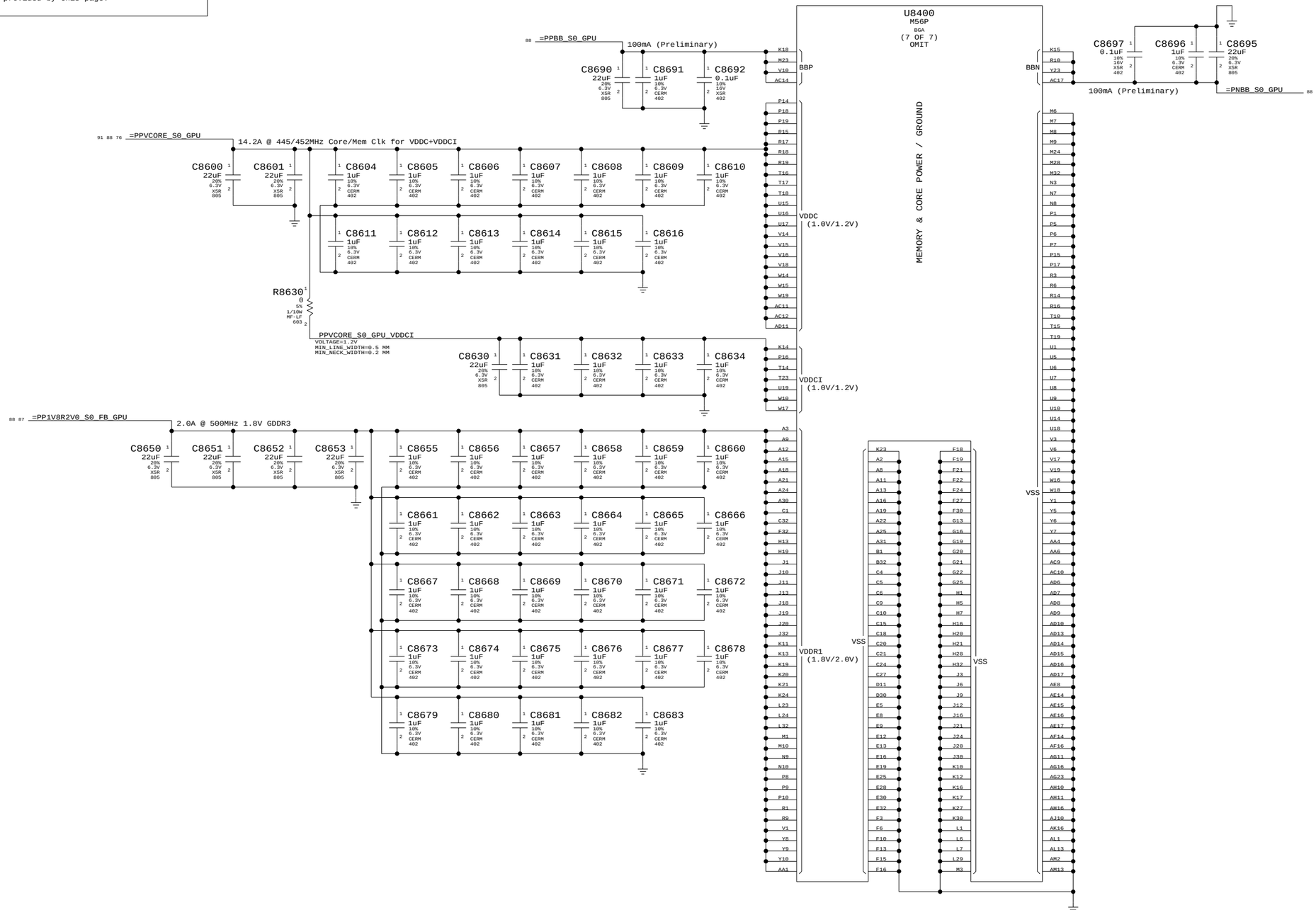
SCALE	SHT	OF
NONE	85	111

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

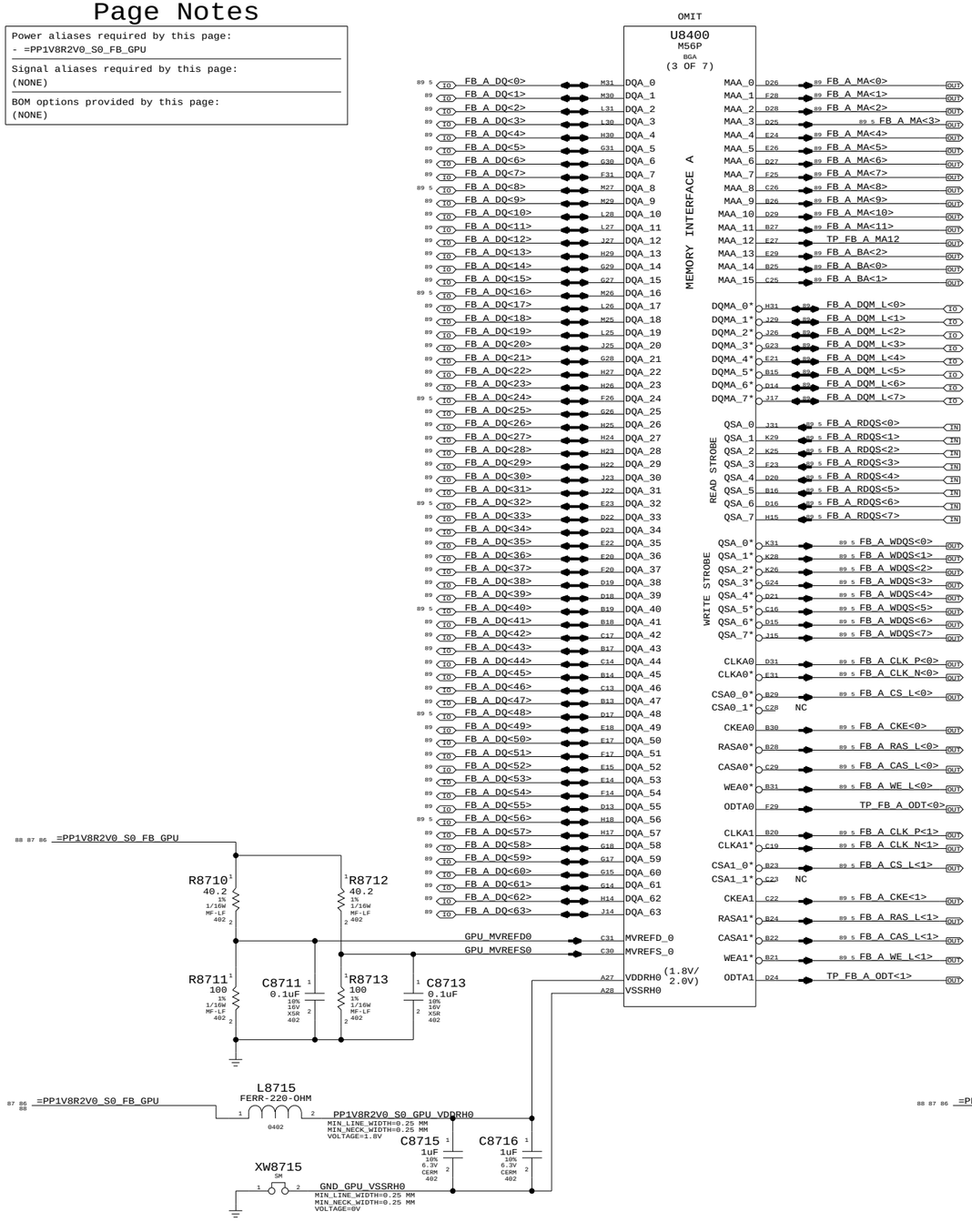
SCALE	SHT	OF
NONE	86	111

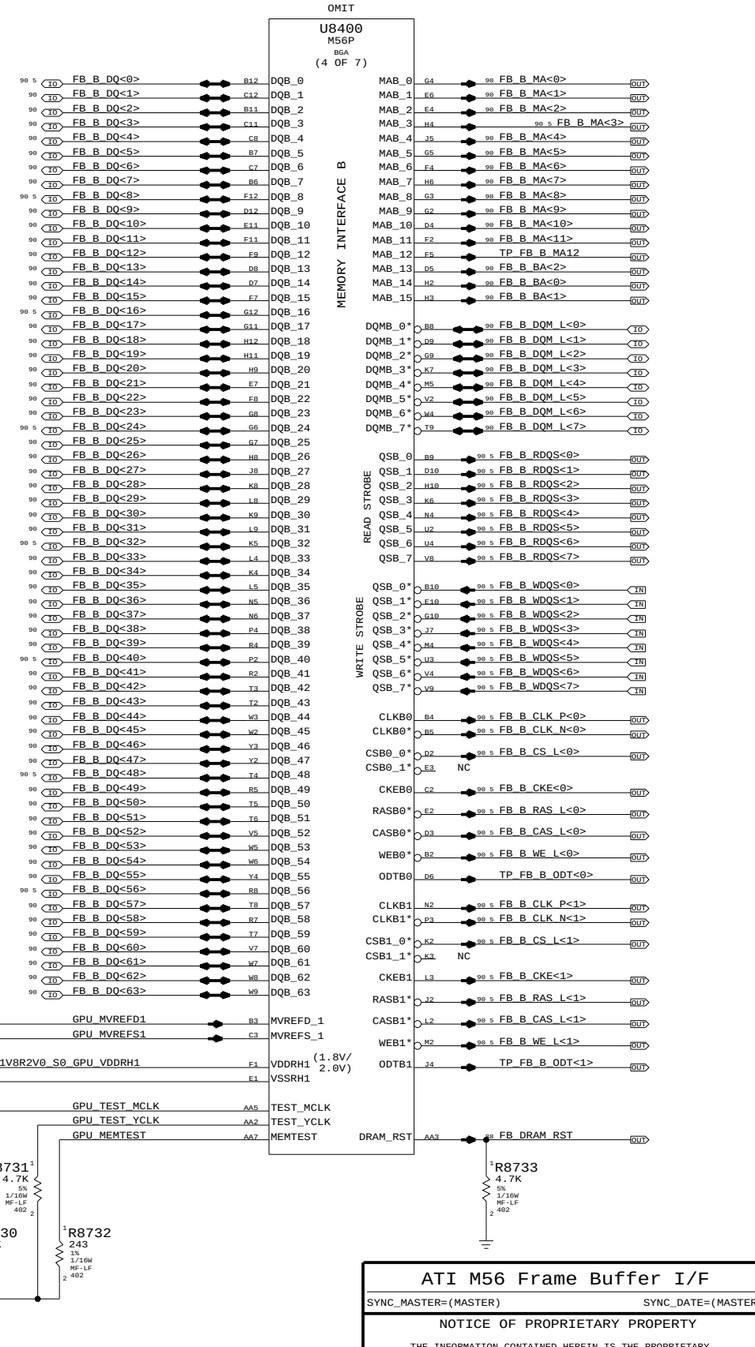
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	87	111

"S0" GPU RAILS

ONLY ON IN RUN

PP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVCORE_S0_GPU_REG
=PPVCORE_S0_GPU
=PPVCORE_S0_GPU_BBP

PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V
R8800 10 1/16W 603 MF-LF 5%
=PP5V_S0_GPUVCORE
GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PP1V2_S0_PCIE_GPU_VDDR
=PP1V2_S0_PCIE_GPU_PVDD
=PPVIO_S0_PCIE
=PP1V2_S0_REG
=PP1V2_S0_GPU_VDDPLL

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V
=PPVOUT_S0_GPUBBP_LDO
=PPBB_S0_GPU

PNBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=0V
=PNVOUT_S0_GPUBBN_REG
=PNBB_S0_GPU

PP3V3_S0
=PP3V3_S0_GPUBBP
=PP3V3_S0_GPUBBCTL
=PP3V3_DDC_DVI
=PP3V3_S0_LCD
=PP3V3_S0_GPU_VDDR3
=PP3V3_S0_GPU
=PP3V3_S0_GPUBBN
=PP3V3_S0_GPU_CLOCKS
=PP3V3_DDC_LCD
=PP3V3_GPU

PP2V5_S0
=PP2V5_S0_GPU_PVDD
=PP2V5_S0_GPU_VDD25
=PP2V5_S0_GPU_VDDC_CT
=PP2V5_S0_GPU

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V
=PP1V8_S0_FB_VDD
=PP1V8R3V3_S0_GPU_VDDR4
=PP1V8R3V3_S0_GPU_VDDR5
=PP1V8_S0_FB_VDDQ
PP1V8_S0
=PP1V8R2V0_S0_FB_GPU

PP12V_S5
=PPVIN_S0_GPUVCORE

PP12V_S0
=PP12V_GPU

PP5V_S0
=PP5V_S0_GPUBBCTL
=PP5V_S0_DVI_DDC
=PP5V_S0_GPUISENS

GPUVCORE_EN
R8801 33 1/16W 402 MF-LF 5%
PM_SLP_S3_L

FB_DRAM_RST
MAKE_BASE=TRUE
DRAM_RST

M56 GPIOS

=PP3V3_S0_GPU_VDDR3

GPU_GPIO_0
R8813 10K 1/16W 402 MF-LF 5%

GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

GPU_GPIO_1
R8802 10K 1/16W 402 MF-LF 5%

GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

GPU_GPIO_2
R8803 NOSTUFF 10K 1/16W 402 MF-LF 5%

GPU_GPIO_3
R8804 NOSTUFF 10K 1/16W 402 MF-LF 5%

GPU_GPIO_4
R8805 NOSTUFF 10K 1/16W 402 MF-LF 5%

GPIO 4 = DEBUG SIGNALS OUT

GPU_GPIO_5
R8806 10K 1/16W 402 MF-LF 5%

GPU_GPIO_6
R8807 NOSTUFF 10K 1/16W 402 MF-LF 5%

TP_GPU_GPIO_7
MAKE_BASE=TRUE
GPU_GPIO_7

GPU_GPIO_8
R8808 NOSTUFF 10K 1/16W 402 MF-LF 5%

NC_GPU_GPIO_10
MAKE_BASE=TRUE
GPU_GPIO_10

GPU_GPIO_9
R8809 NOSTUFF 10K 1/16W 402 MF-LF 5%

GPU_GPIO_13
R8812 NOSTUFF 10K 1/16W 402 MF-LF 5%
ATI_FB_256M

GPU_GPIO_12
R8810 10K 1/16W 402 MF-LF 5%

GPU_GPIO_11
R8811 NOSTUFF 10K 1/16W 402 MF-LF 5%

GPIO 9,13,12,11 = ROM ID CFG
INTERNAL PULL DOWN
0010 = 256 M APERATURE SIZE

ATI_FB_256M
GPU_GPIO_24
R8830 10K 1/16W 402 MF-LF 5%

ATI_FB_HYNIX
GPU_GPIO_27
R8831 10K 1/16W 402 MF-LF 5%

GPU_GPIO_28
R8832 10K 1/16W 402 MF-LF 5%

TMDS_PANEL
GPU_GPIO_29
R8833 10K 1/16W 402 MF-LF 5%

GPU_VCORE_LOW
MAKE_BASE=TRUE
GPU_GPIO_15
R8850 10K 1/16W 402 MF-LF 5%

GPIO 15 = SWITCH CORE VOLTAGE HIGH TO LOW
EXTERNAL PULL DOWN RECOMMENDED

TP_GPU_GPIO_14
MAKE_BASE=TRUE
GPU_GPIO_14

TP_GPU_GPIO_17
MAKE_BASE=TRUE
GPU_GPIO_17

TP_GPU_VGA_R
MAKE_BASE=TRUE
GPU_VGA_R

TP_GPU_VGA_G
MAKE_BASE=TRUE
GPU_VGA_G

TP_GPU_VGA_B
MAKE_BASE=TRUE
GPU_VGA_B

TP_GPU_VGA_HSYNC
MAKE_BASE=TRUE
GPU_VGA_HSYNC

TP_GPU_VGA_VSYNC
MAKE_BASE=TRUE
GPU_VGA_VSYNC

TP_GPU_TV_Y
MAKE_BASE=TRUE
GPU_TV_Y

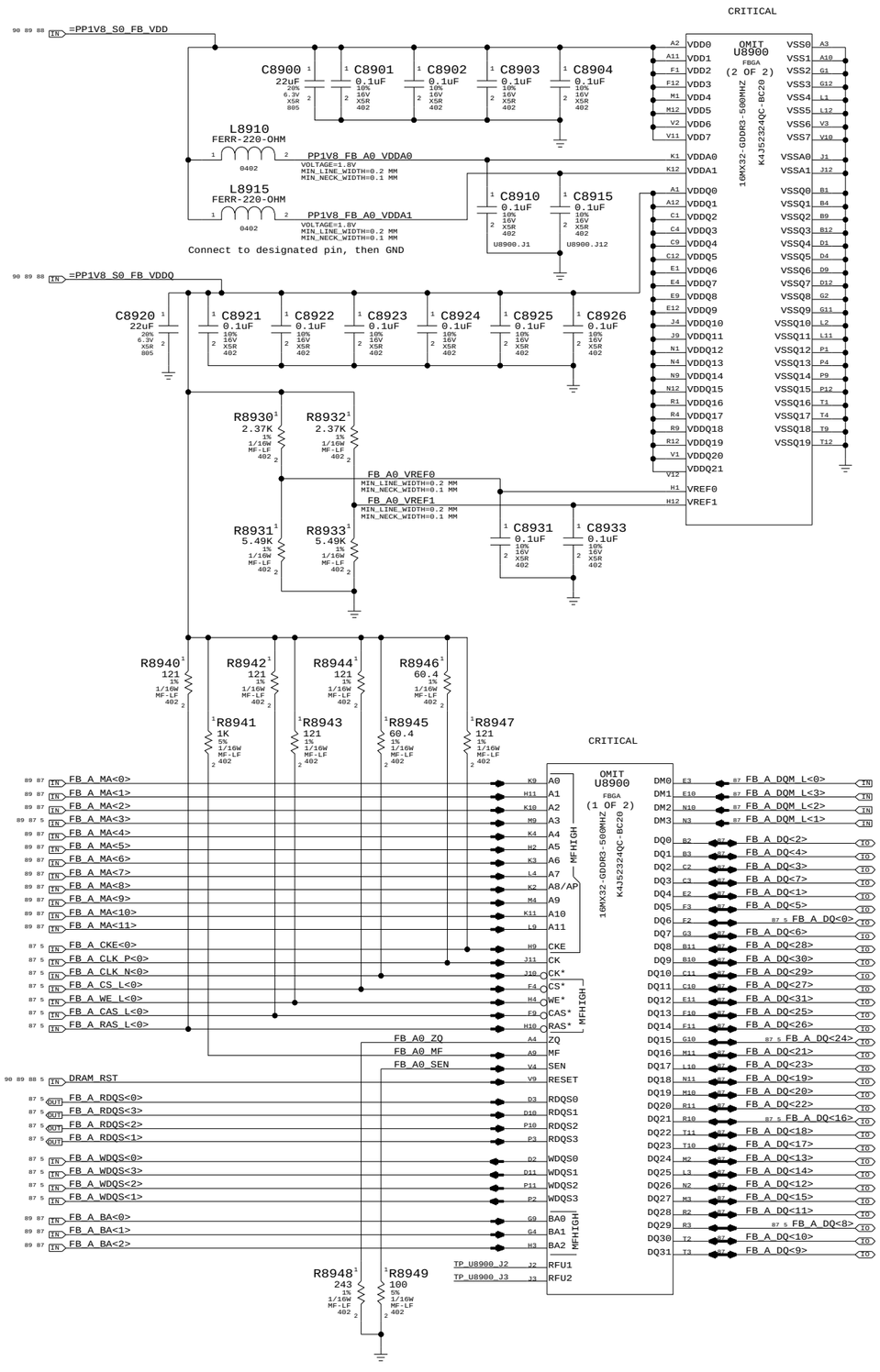
TP_GPU_TV_COMP
MAKE_BASE=TRUE
GPU_TV_COMP

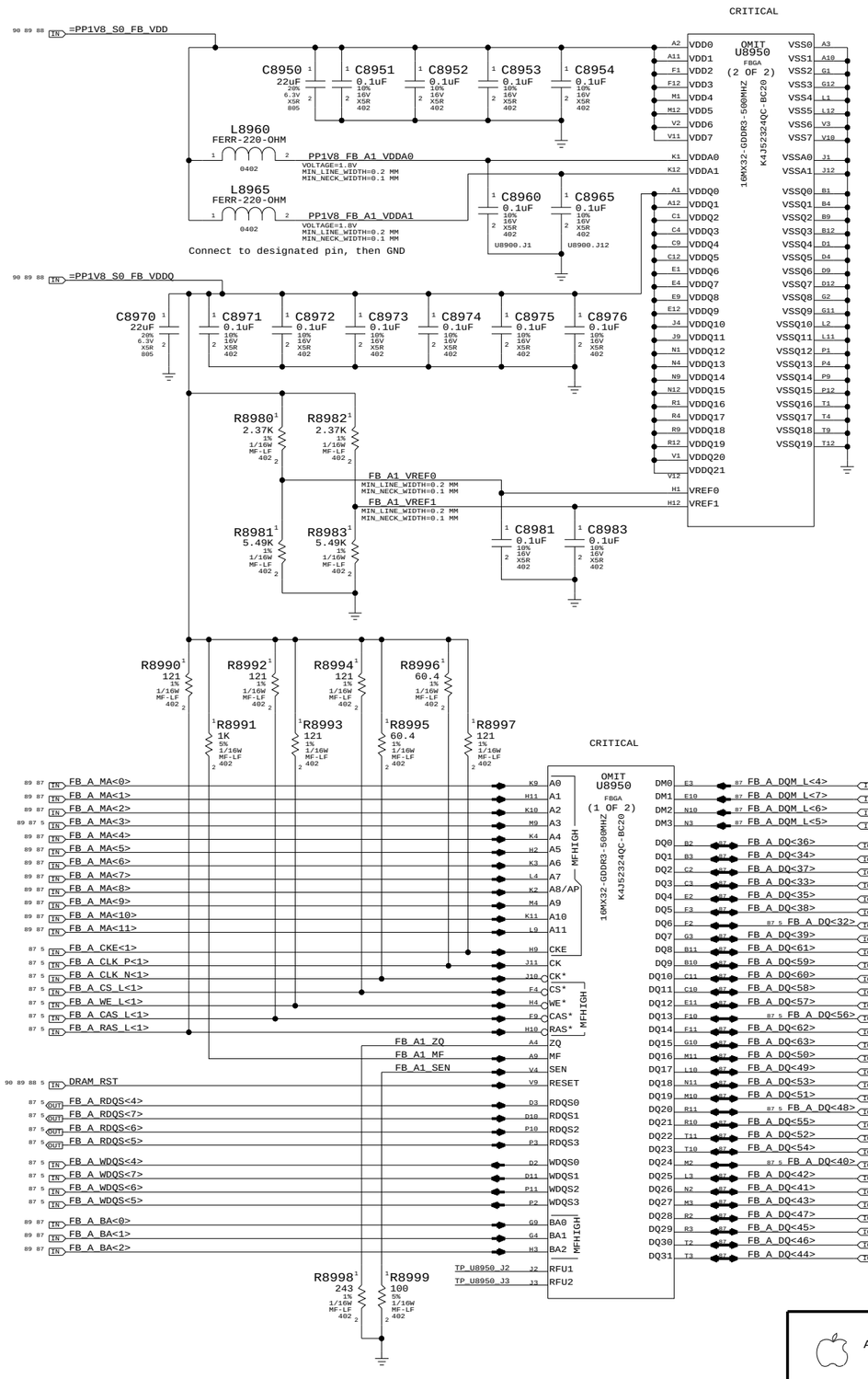
TP_GPU_TV_C
MAKE_BASE=TRUE
GPU_TV_C

TP_GPU_DDC_B_CLK
MAKE_BASE=TRUE
GPU_DDC_B_CLK

TP_GPU_DDC_B_DATA
MAKE_BASE=TRUE
GPU_DDC_B_DATA

GPU MISC





Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

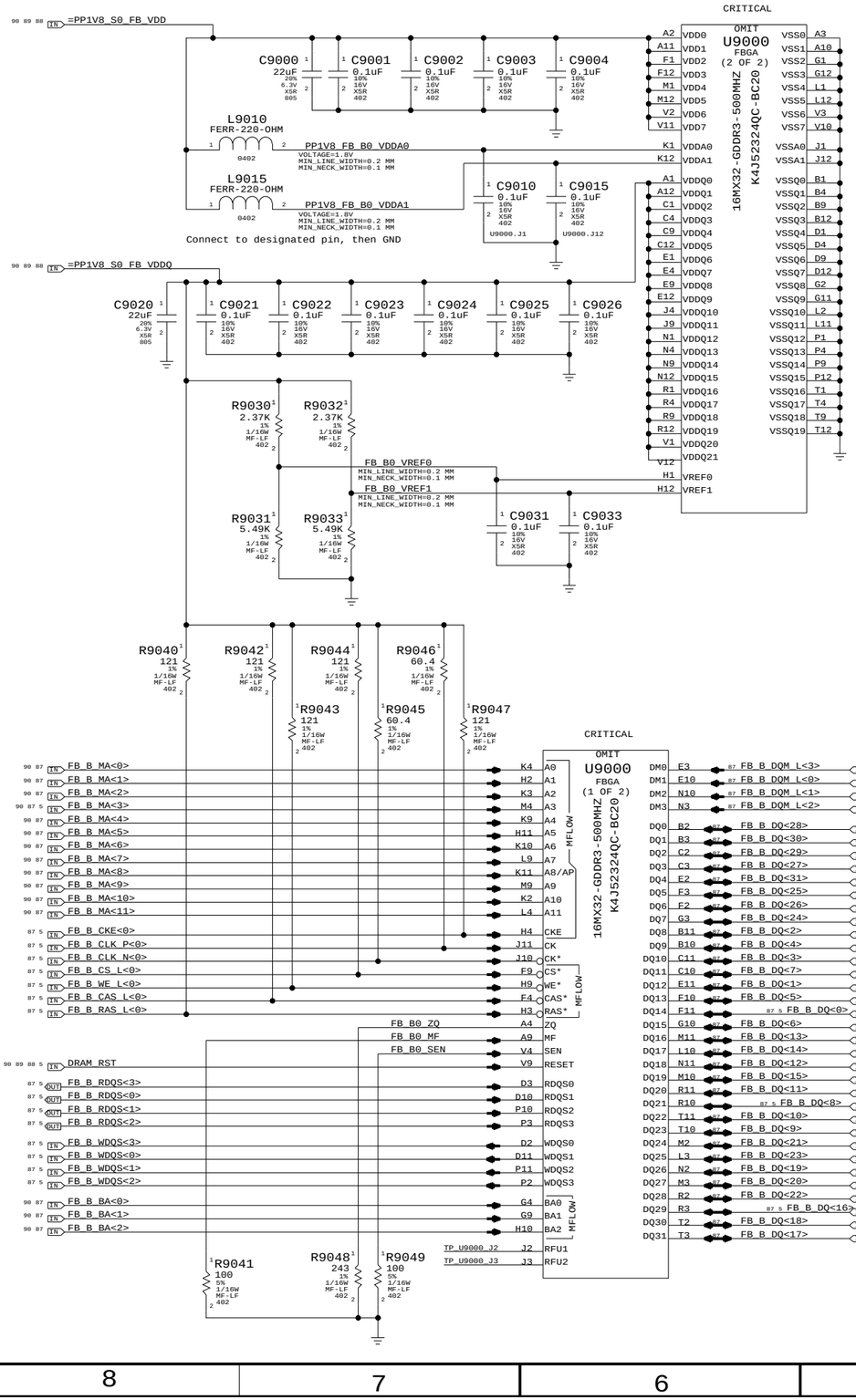
BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 89 OF 111	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6950	06

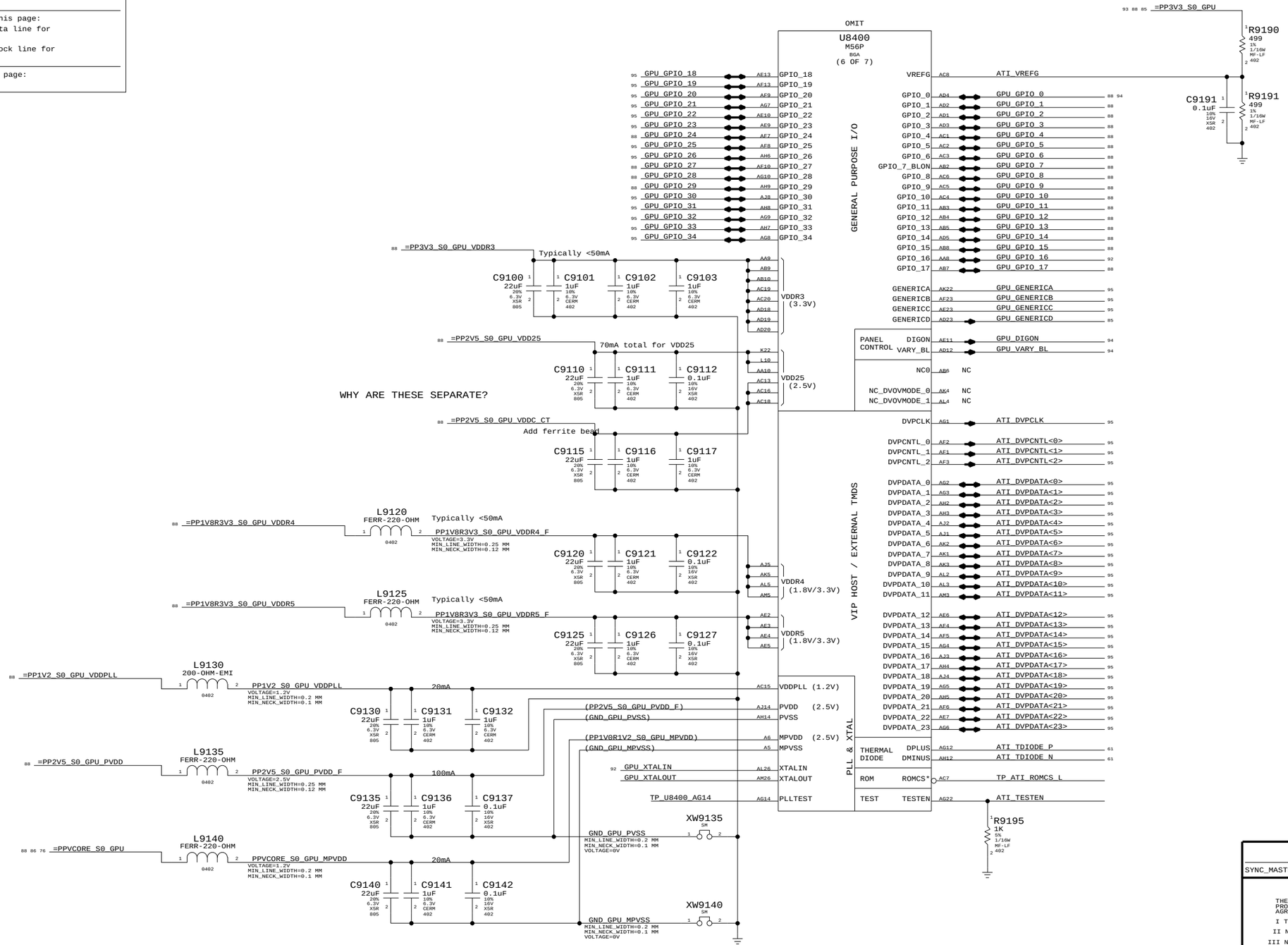
SCALE	SHT	OF
NONE	90	111

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

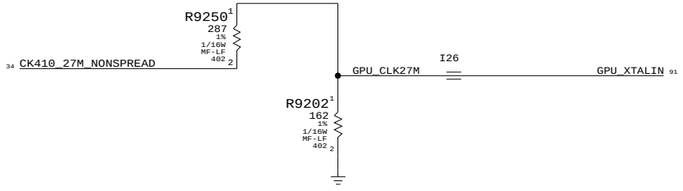
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 91 OF 111	

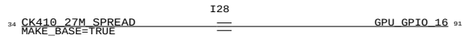
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8





GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09

SCALE	SHT	OF
NONE	92	111

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents on this page: 605mA

88 =PP2V5_S0_GPU

L9300 FERR-220-OHM 0402
PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=2.5V
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=0V
20mA peak
C9300 22uF 20% 6.3V X5R 805
C9301 1uF 10% 6.3V CERM 402
C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402
PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=0V
150mA peak
C9305 22uF 20% 6.3V X5R 805
C9306 1uF 10% 6.3V CERM 402
C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402
PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=0V
XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
65mA peak
C9310 22uF 20% 6.3V X5R 805
C9311 1uF 10% 6.3V CERM 402
C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402
PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
20mA peak
C9315 22uF 20% 6.3V X5R 805
C9316 1uF 10% 6.3V CERM 402
C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402
PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=2.5V
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
130mA peak
C9320 22uF 20% 6.3V X5R 805
C9321 1uF 10% 6.3V CERM 402
C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402
PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
20mA peak
C9325 22uF 20% 6.3V X5R 805
C9326 1uF 10% 6.3V CERM 402
C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402
PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=2.5V
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.12 MM, VOLTAGE=0V
20mA peak
C9330 22uF 20% 6.3V X5R 805
C9331 1uF 10% 6.3V CERM 402
C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402
PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=2.5V
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 MM, MIN_NECK_WIDTH=0.125 MM, VOLTAGE=0V
200mA peak
C9340 22uF 20% 6.3V X5R 805
C9345 22uF 20% 6.3V X5R 805
C9341 1uF 10% 6.3V CERM 402
C9342 0.1uF 10% 16V X5R 402
C9346 0.1uF 10% 16V X5R 402
C9347 0.1uF 10% 16V X5R 402

OMIT

U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR
- AL25 AVDD (2.5V)
- AM25 AVDD (2.5V)
- AJ24 AVSS
- AK25 AVSS
- AK23 AVSSQ

DAC (CRT)
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- 93 ATI_RSET → AL22 RSET

DAC2 (TV/CRT2)
- AL16 A2VDD (2.5V)
- AM16 A2VDD (2.5V)
- AL17 A2VSS
- AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- 93 ATI_R2SET → AK14 R2SET

LVDS
- AE19 LVPDD (2.5V)
- AE18 LVPSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AE19, AE20 LVDDR (2.5V)
- AE17, AF17, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- DDC1CLK AH23 → 97 GPU_DDC_A_CLK → TO
- DDC1DATA AH22 → 97 GPU_DDC_A_DATA → TO
- DDC2CLK AG13 → 88 GPU_DDC_B_CLK → TO
- DDC2DATA AH13 → 88 GPU_DDC_B_DATA → TO
- DDC3CLK AF12 → 94 93 GPU_DDC_C_CLK → TO
- DDC3DATA AE12 → 94 93 GPU_DDC_C_DATA → TO
- 97 HN GPU_HPD → AF11 HPD1

TMDS
- TXCP AM9 → 97 TMDS_CLK_P → OUT
- TXCM AL9 → 97 TMDS_CLK_N → OUT
- TX0P AL10 → 97 TMDS_DATA_P<0> → OUT
- TX0M AK10 → 97 TMDS_DATA_N<0> → OUT
- TX1P AM11 → 97 TMDS_DATA_P<1> → OUT
- TX1M AL11 → 97 TMDS_DATA_N<1> → OUT
- TX2P AM12 → 97 TMDS_DATA_P<2> → OUT
- TX2M AL12 → 97 TMDS_DATA_N<2> → OUT
- TX3P AJ9 → 95 TMDS_DATA_P<3> → OUT
- TX3M AK9 → 95 TMDS_DATA_N<3> → OUT
- TX4P AJ11 → 95 TMDS_DATA_P<4> → OUT
- TX4M AK11 → 95 TMDS_DATA_N<4> → OUT
- TX5P AJ12 → 95 TMDS_DATA_P<5> → OUT
- TX5M AK12 → 95 TMDS_DATA_N<5> → OUT

DAC (CRT)
- R AK24 → 88 GPU_VGA_R → OUT
- G AM24 → 88 GPU_VGA_G → OUT
- B AL24 → 88 GPU_VGA_B → OUT
- HSYNC AJ23 → 88 GPU_VGA_HSYNC → OUT
- VSYNC AJ22 → 88 GPU_VGA_VSYNC → OUT

DAC2 (TV/CRT2)
- R2 AK15 → 97 GPU_R2 → OUT
- G2 AM15 → 97 GPU_G2 → OUT
- B2 AL15 → 97 GPU_B2 → OUT
- H2SYNC AF15 → 97 GPU_H2SYNC → OUT
- V2SYNC AG15 → 97 GPU_V2SYNC → OUT
- Y AJ15 → 88 GPU_TV_Y → OUT
- C AJ13 → 88 GPU_TV_C → OUT
- COMP AH15 → 88 GPU_TV_COMP → OUT

LVDS
- TXCLK_UP AJ21 → 94 LVDS_U_CLK_P → OUT
- TXCLK_UN AK21 → 94 LVDS_U_CLK_N → OUT
- TXOUT_U0P AG18 → 94 LVDS_U_DATA_P<0> → OUT
- TXOUT_U0N AH18 → 94 LVDS_U_DATA_N<0> → OUT
- TXOUT_U1P AK20 → 94 LVDS_U_DATA_P<1> → OUT
- TXOUT_U1N AJ20 → 94 LVDS_U_DATA_N<1> → OUT
- TXOUT_U2P AG20 → 94 LVDS_U_DATA_P<2> → OUT
- TXOUT_U2N AH20 → 94 LVDS_U_DATA_N<2> → OUT
- TXOUT_U3P AH21 → 94 LVDS_U_DATA_P<3> → OUT
- TXOUT_U3N AG21 → 94 LVDS_U_DATA_N<3> → OUT
- TXCLK_LP AM18 → 94 93 LVDS_L_CLK_P → OUT
- TXCLK_LN AL18 → 94 93 LVDS_L_CLK_N → OUT
- TXOUT_L0P AL19 → 94 93 LVDS_L_DATA_P<0> → OUT
- TXOUT_L0N AK19 → 94 93 LVDS_L_DATA_N<0> → OUT
- TXOUT_L1P AM20 → 94 93 LVDS_L_DATA_P<1> → OUT
- TXOUT_L1N AL20 → 94 93 LVDS_L_DATA_N<1> → OUT
- TXOUT_L2P AM21 → 94 93 LVDS_L_DATA_P<2> → OUT
- TXOUT_L2N AL21 → 94 93 LVDS_L_DATA_N<2> → OUT
- TXOUT_L3P AJ18 → 94 LVDS_L_DATA_P<3> → OUT
- TXOUT_L3N AK18 → 94 LVDS_L_DATA_N<3> → OUT

TERMINATION FOR TMDS USAGE OF LVDS PINS
PLACE CLOSE TO GPU (U8400)

- 94 93 LVDS_L_CLK_P → TMDS_PANEL R9370 100 5% 1/10W MF-LF 402
- 94 93 LVDS_L_CLK_N
- 94 93 LVDS_L_DATA_P<0> → TMDS_PANEL R9371 100 5% 1/10W MF-LF 402
- 94 93 LVDS_L_DATA_N<0>
- 94 93 LVDS_L_DATA_P<1> → TMDS_PANEL R9372 100 5% 1/10W MF-LF 402
- 94 93 LVDS_L_DATA_N<1>
- 94 93 LVDS_L_DATA_P<2> → TMDS_PANEL R9373 100 5% 1/10W MF-LF 402
- 94 93 LVDS_L_DATA_N<2>

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

91 88 85 =PP3V3_S0_GPU

- R9390 4.7K 5% 1/16W MF-LF 402
- R9391 4.7K 5% 1/16W MF-LF 402
- 94 93 GPU_DDC_C_CLK
- 94 93 GPU_DDC_C_DATA

ATI_RSET 93
ATI_R2SET 93
- R9350 499 1% 1/16W MF-LF 402
- R9351 715 1% 1/16W MF-LF 402

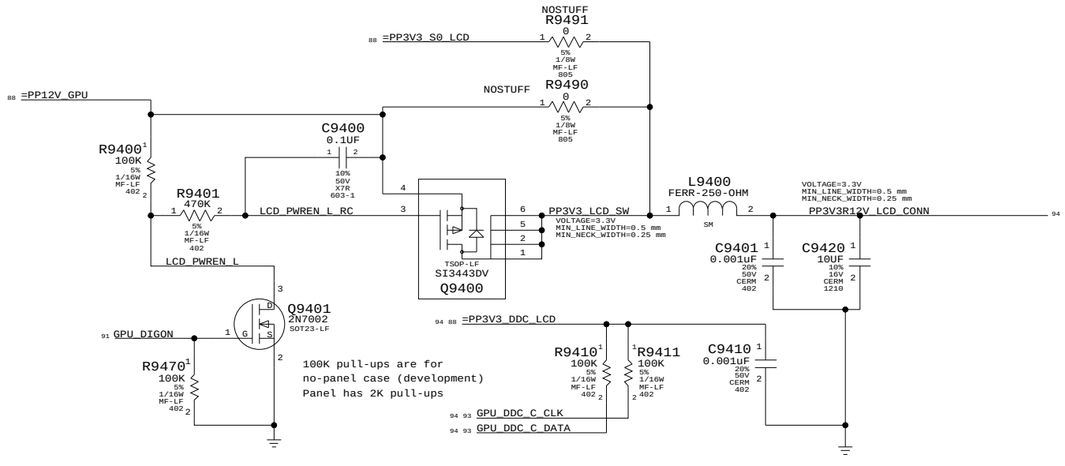
ATI M56 Video Interfaces

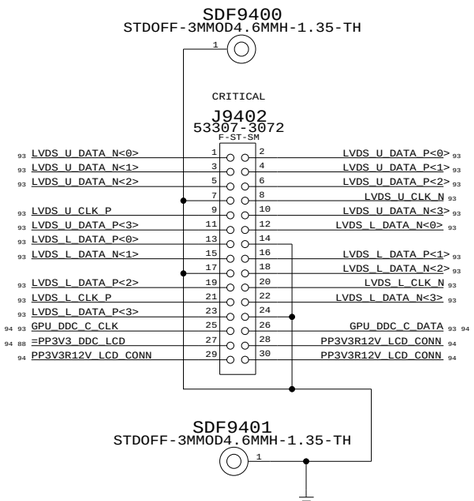
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

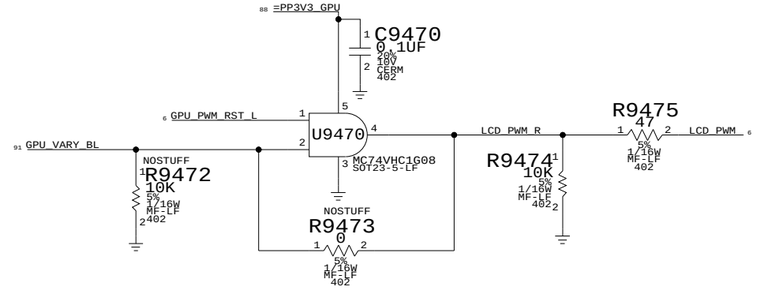
SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 93 OF 111	

LCD (LVDS) INTERFACE





INVERTER INTERFACE



GATE TO PREVENT LEAKAGE ONTO PWM
MIGHT BE ABLE TO BYPASS IF SMC DRIVES SIGNAL

Internal Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6950	06

SCALE	SHT	OF
NONE	94	111

TP_TMDS_DATA_P<3> == TMDS_DATA_P<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<3> == TMDS_DATA_N<3> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<4> == TMDS_DATA_P<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<4> == TMDS_DATA_N<4> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_P<5> == TMDS_DATA_P<5> 93
MAKE_BASE=TRUE

TP_TMDS_DATA_N<5> == TMDS_DATA_N<5> 93
MAKE_BASE=TRUE

TP_ATI_DVPDATA<23> == ATI_DVPDATA<23> 91
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TP_ATI_DVPDATA<22> == ATI_DVPDATA<22> 91
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TP_ATI_DVPDATA<21> == ATI_DVPDATA<21> 91
MAKE_BASE=TRUE

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TP_ATI_DVPDATA<18> == ATI_DVPDATA<18> 91
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MAKE_BASE=TRUE

TP_ATI_DVPDATA<4> == ATI_DVPDATA<4> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<3> == ATI_DVPDATA<3> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<2> == ATI_DVPDATA<2> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<1> == ATI_DVPDATA<1> 91
MAKE_BASE=TRUE

TP_ATI_DVPDATA<0> == ATI_DVPDATA<0> 91
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TP_ATI_DVPCLK == ATI_DVPCLK 91
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TP_ATI_DVPCNTL<0> == ATI_DVPCNTL<0> 91
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TP_ATI_DVPCNTL<1> == ATI_DVPCNTL<1> 91
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TP_ATI_DVPCNTL<2> == ATI_DVPCNTL<2> 91
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TP_GPU_GPIO<34> == GPU_GPIO_34 91
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TP_GPU_GPIO<33> == GPU_GPIO_33 91
MAKE_BASE=TRUE

TP_GPU_GPIO<32> == GPU_GPIO_32 91
MAKE_BASE=TRUE

TP_GPU_GPIO<31> == GPU_GPIO_31 91
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TP_GPU_GPIO<30> == GPU_GPIO_30 91
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TP_GPU_GPIO<19> == GPU_GPIO_19 91
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TP_GPU_GPIO<18> == GPU_GPIO_18 91
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TP_GPU_GENERICA == GPU_GENERICA 91
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TP_GPU_GENERICB == GPU_GENERICB 91
MAKE_BASE=TRUE

TP_GPU_GENERICC == GPU_GENERICC 91
MAKE_BASE=TRUE

M56 TPS

NOTICE OF PROPRIETARY PROPERTY

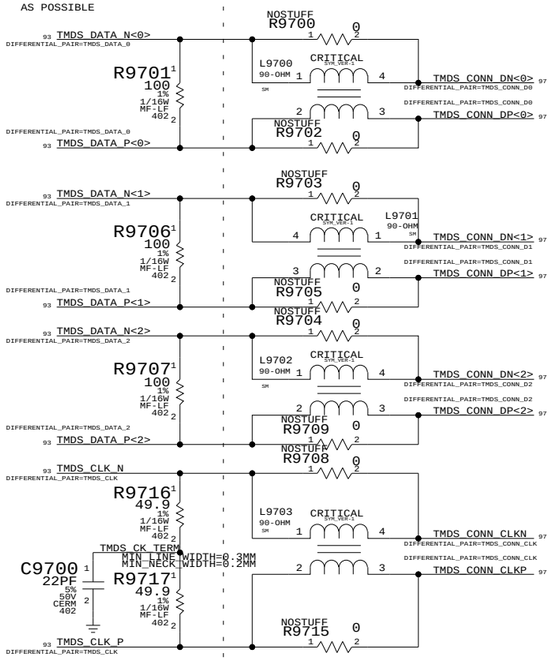
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 95 OF 111	

DVI INTERFACE

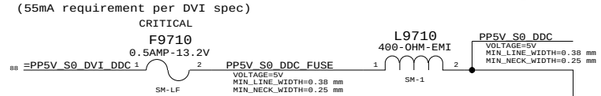
PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

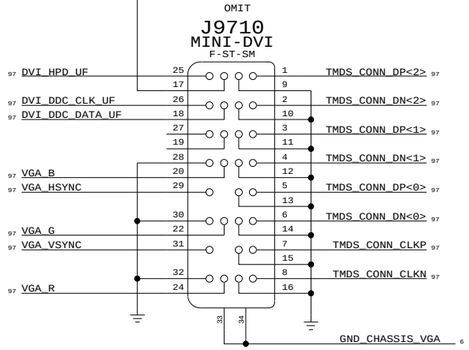
PLACE FILTER CLOSE
TO TMDS CONNECTOR



DVI DDC CURRENT LIMIT

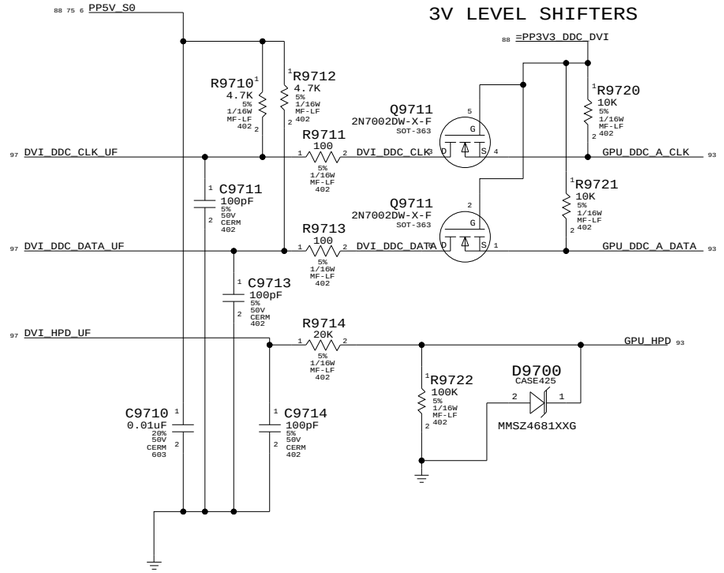
(55mA requirement per DVI spec)





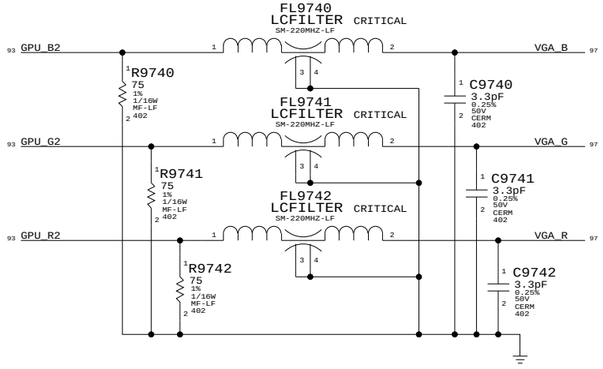
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0114	1	CONN,32-P MINI-DVI RCPT MG3,LF	J9710	CRITICAL	17_INCH_LCD
514S0116	1	CONN,32-P MINI-DVI RCPT MG3,LF	J9710	CRITICAL	20_INCH_LCD

3V LEVEL SHIFTERS

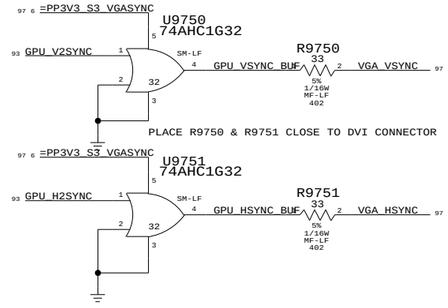


ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS



External Display Conns

SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6949	09
SCALE: NONE	SHT 97 OF 111	

```
Title:       Basenet Report
Design:      m39
Date:        Nov 15 18:33:07 2005

Base nets and synonyms for m39_lib.M39(@m39_lib.m39(sch_1))
Base Signal          Synonyms                              Location([Zone][dir])

0V7_REF              0V7_REF - @m39_lib.M39                79A3
1V0_REF              1V0_REF - @m39_lib.M39                79A5 80A5 81A5 81B3
1V2REG_ITH           1V2REG_ITH - @m39_lib.M39             77B5
1V2REG_ITH_RC        1V2REG_ITH_RC - @m39_lib.M39          77B6
1V2REG_MODE          1V2REG_MODE - @m39_lib.M39            77B5
1V2REG_PGOOD         1V2REG_PGOOD - @m39_lib.M39           77B4
1V2REG_RT            1V2REG_RT - @m39_lib.M39              77B5
1V2REG_RUNSS         1V2REG_RUNSS - @m39_lib.M39           77B5
1V2REG_SGND          1V2REG_SGND - @m39_lib.M39            77A7
1V2REG_SW            1V2REG_SW - @m39_lib.M39              77B4
1V2REG_VFB           1V2REG_VFB - @m39_lib.M39             77B5
1V2REG_VFB_DIV       1V2REG_VFB_DIV - @m39_lib.M39         77A5
1V3_REF              1V3_REF - @m39_lib.M39                80B3
1V05REG_NB_BOOT      1V05REG_NB_BOOT - @m39_lib.M39        81C6
1V05REG_NB_BOOT_R    1V05REG_NB_BOOT_R - @m39_lib.M39      81C5
1V05REG_NB_COMP      1V05REG_NB_COMP - @m39_lib.M39        81C6
1V05REG_NB_COMP_R    1V05REG_NB_COMP_R - @m39_lib.M39      81C5
1V05REG_NB_FB        1V05REG_NB_FB - @m39_lib.M39          81C5
1V05REG_NB_FB_R      1V05REG_NB_FB_R - @m39_lib.M39        81C3
1V05REG_NB_FS_DIS    1V05REG_NB_FS_DIS - @m39_lib.M39      81C7
1V05REG_NB_GND       1V05REG_NB_GND - @m39_lib.M39         81B7
1V05REG_NB_LDO_DR    1V05REG_NB_LDO_DR - @m39_lib.M39      81C7
1V05REG_NB_LDO_FB    1V05REG_NB_LDO_FB - @m39_lib.M39      81C7
1V05REG_NB_LGATE     1V05REG_NB_LGATE - @m39_lib.M39       81C6
1V05REG_NB_PVCC5     1V05REG_NB_PVCC5 - @m39_lib.M39       81D7
1V05REG_NB_SNUB      1V05REG_NB_SNUB - @m39_lib.M39        81C4
1V05REG_NB_SWITCHNOD 1V05REG_NB_SWITCHNODE -               81C5
E                    @m39_lib.M39
1V05REG_NB_UGATE     1V05REG_NB_UGATE - @m39_lib.M39       81D6
1V05REG_NB_VCC5      1V05REG_NB_VCC5 - @m39_lib.M39        81D7
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1V5REG_PCIE_BOOT_R   1V5REG_PCIE_BOOT_R - @m39_lib.M39     80C5
1V5REG_PCIE_COMP     1V5REG_PCIE_COMP - @m39_lib.M39       80C6
1V5REG_PCIE_COMP_R   1V5REG_PCIE_COMP_R - @m39_lib.M39     80C5
1V5REG_PCIE_FB       1V5REG_PCIE_FB - @m39_lib.M39         80C5
1V5REG_PCIE_FB_R     1V5REG_PCIE_FB_R - @m39_lib.M39       80C3
1V5REG_PCIE_FS_DIS   1V5REG_PCIE_FS_DIS - @m39_lib.M39     80C7
1V5REG_PCIE_GND      1V5REG_PCIE_GND - @m39_lib.M39        80B7
1V5REG_PCIE_LDO_DR   1V5REG_PCIE_LDO_DR - @m39_lib.M39     80C7
1V5REG_PCIE_LDO_FB   1V5REG_PCIE_LDO_FB - @m39_lib.M39     80C7
1V5REG_PCIE_LGATE    1V5REG_PCIE_LGATE - @m39_lib.M39      80C6
1V5REG_PCIE_PVCC5    1V5REG_PCIE_PVCC5 - @m39_lib.M39      80D7
1V5REG_PCIE_SNUB     1V5REG_PCIE_SNUB - @m39_lib.M39       80C4
1V5REG_PCIE_SWITCHNO 1V5REG_PCIE_SWITCHNODE -              80C5
DE                   @m39_lib.M39
1V5REG_PCIE_UGATE    1V5REG_PCIE_UGATE - @m39_lib.M39      80D6
1V5REG_PCIE_VCC5     1V5REG_PCIE_VCC5 - @m39_lib.M39       80D7
1V6_REF              1V6_REF - @m39_lib.M39                79B3
1V8REG_DDR_BOOT      1V8REG_DDR_BOOT - @m39_lib.M39        79D6
1V8REG_DDR_BOOT_R    1V8REG_DDR_BOOT_R - @m39_lib.M39      79D5
1V8REG_DDR_COMP      1V8REG_DDR_COMP - @m39_lib.M39        79C6
1V8REG_DDR_COMP_R    1V8REG_DDR_COMP_R - @m39_lib.M39      79C5
1V8REG_DDR_FB        1V8REG_DDR_FB - @m39_lib.M39          79C5
1V8REG_DDR_FB_R      1V8REG_DDR_FB_R - @m39_lib.M39        79C3
1V8REG_DDR_FS_DIS    1V8REG_DDR_FS_DIS - @m39_lib.M39      79C7
1V8REG_DDR_GND       1V8REG_DDR_GND - @m39_lib.M39         79C7
1V8REG_DDR_LDO_DR    1V8REG_DDR_LDO_DR - @m39_lib.M39      79C7
1V8REG_DDR_LDO_FB    1V8REG_DDR_LDO_FB - @m39_lib.M39      79C7
1V8REG_DDR_LGATE     1V8REG_DDR_LGATE - @m39_lib.M39       79C6
1V8REG_DDR_PVCC5     1V8REG_DDR_PVCC5 - @m39_lib.M39       79D7
1V8REG_DDR_SNUB      1V8REG_DDR_SNUB - @m39_lib.M39        79C4
1V8REG_DDR_SWITCHNOD 1V8REG_DDR_SWITCHNODE -               79C5
E                    @m39_lib.M39
1V8REG_DDR_UGATE     1V8REG_DDR_UGATE - @m39_lib.M39       79D6
1V8REG_DDR_VCC5      1V8REG_DDR_VCC5 - @m39_lib.M39        79D7
1V8REG_GPU_BOOT      1V8REG_GPU_BOOT - @m39_lib.M39        78C6
1V8REG_GPU_BOOT_R    1V8REG_GPU_BOOT_R - @m39_lib.M39      78C5
1V8REG_GPU_COMP      1V8REG_GPU_COMP - @m39_lib.M39        78B6
1V8REG_GPU_COMP_R    1V8REG_GPU_COMP_R - @m39_lib.M39      78B5
1V8REG_GPU_FB        1V8REG_GPU_FB - @m39_lib.M39          78B5
1V8REG_GPU_FB_R      1V8REG_GPU_FB_R - @m39_lib.M39        78B3
1V8REG_GPU_FS_DIS    1V8REG_GPU_FS_DIS - @m39_lib.M39      78B7
1V8REG_GPU_GND       1V8REG_GPU_GND - @m39_lib.M39         78B7
1V8REG_GPU_LDO_DR    1V8REG_GPU_LDO_DR - @m39_lib.M39      78C7
1V8REG_GPU_LDO_FB    1V8REG_GPU_LDO_FB - @m39_lib.M39      78B7
1V8REG_GPU_LGATE     1V8REG_GPU_LGATE - @m39_lib.M39       78B6
1V8REG_GPU_PVCC5     1V8REG_GPU_PVCC5 - @m39_lib.M39       78C7
1V8REG_GPU_SNUB      1V8REG_GPU_SNUB - @m39_lib.M39        78B4
1V8REG_GPU_SWITCHNOD 1V8REG_GPU_SWITCHNODE -               78B5
E                    @m39_lib.M39
1V8REG_GPU_UGATE     1V8REG_GPU_UGATE - @m39_lib.M39       78C6
1V8REG_GPU_VCC5      1V8REG_GPU_VCC5 - @m39_lib.M39        78C7
2V5REG_ITH           2V5REG_ITH - @m39_lib.M39             77C4
2V5REG_ITH_RC        2V5REG_ITH_RC - @m39_lib.M39          77C4
2V5REG_MODE          2V5REG_MODE - @m39_lib.M39            77C5
2V5REG_RT            2V5REG_RT - @m39_lib.M39              77C5
2V5REG_SGND          2V5REG_SGND - @m39_lib.M39            77C4
2V5REG_SW            2V5REG_SW - @m39_lib.M39              77C4
2V5REG_VFB           2V5REG_VFB - @m39_lib.M39             77C4
5V_REG_IN            5V_REG_IN - @m39_lib.M39              68A4
=I2C_HD_TEMP_SCL     =I2C_HD_TEMP_SCL - @m39_lib.M39       59C1 66B6
                     =I2C_ODD_TEMP_SCL - @m39_lib.M39      59C1 66B4
                     =SMB_THRM_CLK - @m39_lib.M39          10C3 59C1
                     SMB_B_S0_CLK - @m39_lib.M39           58B5 59C2 59D1
                     SMB_GPU_NB_THRM_CLK - @m39_lib.M39    59B1 61C3
                     SMB_B_S0_CLK - @m39_lib.M39           58B5 59C2 59D1
                     =SMB_THRM_CLK - @m39_lib.M39          10C3 59C1
                     =I2C_ODD_TEMP_SCL - @m39_lib.M39      59C1 66B4
=I2C_HD_TEMP_SDA     =I2C_HD_TEMP_SDA - @m39_lib.M39       59C1 66B6
                     =I2C_ODD_TEMP_SDA - @m39_lib.M39      59C1 66B4
                     =SMB_THRM_DATA - @m39_lib.M39         10C3 59C1
                     SMB_B_S0_DATA - @m39_lib.M39          58B5 59C2 59D1
                     SMB_GPU_NB_THRM_DATA - @m39_lib.M39   59B1 61C3
                     SMB_B_S0_DATA - @m39_lib.M39          58B5 59C2 59D1
                     =SMB_THRM_DATA - @m39_lib.M39         10C3 59C1
                     =I2C_ODD_TEMP_SDA - @m39_lib.M39      59C1 66B4
=I2C_MEM_SCL         =I2C_MEM_SCL - @m39_lib.M39           27D6 28A6 29A6
                     =SMB_AIRPORT_CLK - @m39_lib.M39       27D6 53B4
                     SMB_CK410_CLK - @m39_lib.M39          27D6 33B6
                     SMB_CLK - @m39_lib.M39                23D5 27B7 27D7
                     SMB_CK410_CLK - @m39_lib.M39          27D6 33B6
                     =SMB_AIRPORT_CLK - @m39_lib.M39       27D6 53B4
=I2C_MEM_SDA         =I2C_MEM_SDA - @m39_lib.M39           27D6 28A6 29A6
                     =SMB_AIRPORT_DATA - @m39_lib.M39      27C6 53B4
                     SMB_CK410_DATA - @m39_lib.M39         27D6 33B6
                     SMB_DATA - @m39_lib.M39               23D5 27B7 27D7
                     SMB_CK410_DATA - @m39_lib.M39         27D6 33B6

                     =SMB_AIRPORT_DATA - @m39_lib.M39      27C6 53B4
=PNBB_S0_GPU         =PNBB_S0_GPU - @m39_lib.M39           86D2 88C6
                     =PNVOUT_S0_GPUBBN_REG -               85B1 88C6
                     @m39_lib.M39
                     PNBB_S0_GPU - @m39_lib.M39            88C8
                     =PNVOUT_S0_GPUBBN_REG -               85B1 88C6
                     @m39_lib.M39
=PP0V9_S0_MEMVTT_LDO =PP0V9_S0_MEMVTT_LDO - @m39_lib.M39   6D4 31B3
                     =PP0V9_S0_MEM_TERM - @m39_lib.M39     6D4 30D4
                     PP0V9_S0 - @m39_lib.M39               6D6 79A3
                     =PP0V9_S0_MEM_TERM - @m39_lib.M39     6D4 30D4
=PP1V2_S0_GPU_VDDPLL =PP1V2_S0_GPU_VDDPLL - @m39_lib.M39   88C6 91B8
                     =PPVIO_S0_PCIE - @m39_lib.M39         84A2 88C6
                     =PP1V2_S0_REG - @m39_lib.M39          77A1 88C6
                     =PP1V2_S0_PCIE_GPU_PVDD -             84C8 88D6
                     @m39_lib.M39
                     =PP1V2_S0_PCIE_GPU_VDDR -             84C8 88D6
                     @m39_lib.M39
                     PP1V2_GPU_IO_S0 - @m39_lib.M39        88D8
                     =PPVIO_S0_PCIE - @m39_lib.M39         84A2 88C6
                     =PP1V2_S0_REG - @m39_lib.M39          77A1 88C6
                     =PP1V2_S0_PCIE_GPU_VDDR -             84C8 88D6
                     @m39_lib.M39
                     =PP1V2_S0_PCIE_GPU_PVDD -             84C8 88D6
                     @m39_lib.M39
=PP1V2_S3_ENET       =PP1V2_S3_ENET - @m39_lib.M39         41A8 41D6 42B5
                     PP1V2_S3_ENET - @m39_lib.M39          42B5
=PP1V2_S3_LAN        =PP1V2_S3_LAN - @m39_lib.M39          6D3 42B8
                     PP1V2_S3 - @m39_lib.M39               6D4 77B2
=PP1V8_S0_FB_VDD     =PP1V8_S0_FB_VDD - @m39_lib.M39       88B6 89D5 89D8 90D5 90D8
                     =PP1V8_S0_FB_VDDQ - @m39_lib.M39      88B6 89D5 89D8 90D5 90D8
                     =PP1V8R2V0_S0_FB_GPU - @m39_lib.M39   86B8 87A5 87A8 87B5 87B8
                                                           88B6
                     PP1V8_S0 - @m39_lib.M39               78B2 88B6
                     =PP1V8R3V3_S0_GPU_VDDR5 -             88B6 91B7
                     @m39_lib.M39
                     =PP1V8R3V3_S0_GPU_VDDR4 -             88B6 91B7
                     @m39_lib.M39
                     PP1V8_S0 - @m39_lib.M39               78B2 88B6
                     PP1V8R2V0_S0_FB_GPU - @m39_lib.M39    88B8
                     =PP1V8_S0_FB_VDDQ - @m39_lib.M39      88B6 89D5 89D8 90D5 90D8
                     =PP1V8R3V3_S0_GPU_VDDR5 -             88B6 91B7
                     @m39_lib.M39
                     =PP1V8R3V3_S0_GPU_VDDR4 -             88B6 91B7
                     @m39_lib.M39
                     =PP1V8R2V0_S0_FB_GPU - @m39_lib.M39   86B8 87A5 87A8 87B5 87B8
                                                           88B6
=PP1V8_S3_MEM_NB     =PP1V8_S3_MEM_NB - @m39_lib.M39       6D3 6D3 14C2 16B6 19B8
                                                           19D7
                     =PP1V8_S0_MEMVTT - @m39_lib.M39       6D3 31C7
                     PP1V8_S3 - @m39_lib.M39               5D2 6D4 79C2
                     =PP1V8_S3_MEM - @m39_lib.M39          5C4 6D3 28B2 28C8 28D3
                                                           28D6 29B2 29D3 29D6
                     PP1V8_S3 - @m39_lib.M39               5D2 6D4 79C2
                     =PP1V8_S3_MEM - @m39_lib.M39          5C4 6D3 28B2 28C8 28D3
                                                           28D6 29B2 29D3 29D6
                     =PP1V8_S0_MEMVTT - @m39_lib.M39       6D3 31C7
=PP2V5_S0_NB_VCCA_3G =PP2V5_S0_NB_VCCA_3GBG -              6B4 17D6 19A8 19C7
BG                   @m39_lib.M39
                     =PP2V5_S0_GPU - @m39_lib.M39          88B6 93C8
                     PP2V5_S0 - @m39_lib.M39               6B6 77C3 88C8
                     =PP2V5_S0_GPU_VDD25 - @m39_lib.M39    88B6 91C6
                     =PP2V5_S0_GPU_VDDC_CT -               88B6 91C6
                     @m39_lib.M39
                     =PP2V5_S0_GPU_PVDD - @m39_lib.M39     88B6 91A8
                     PP2V5_S0 - @m39_lib.M39               6B6 77C3 88C8
                     =PP2V5_S0_GPU_VDDC_CT -               88B6 91C6
                     @m39_lib.M39
                     =PP2V5_S0_GPU_VDD25 - @m39_lib.M39    88B6 91C6
                     =PP2V5_S0_GPU_PVDD - @m39_lib.M39     88B6 91A8
                     =PP2V5_S0_GPU - @m39_lib.M39          88B6 93C8
=PP2V5_S3_ENET       =PP2V5_S3_ENET - @m39_lib.M39         41D5 41D6 42C4
                     PP2V5_S3_ENET - @m39_lib.M39          42C4 43D8
=PP3V3_S0_NB         =PP3V3_S0_NB - @m39_lib.M39           6A4 14C7 14D6 19C7 20A4
                                                           20B4 20B4
                     =PP3V3_DDC_DVI - @m39_lib.M39         88C6 97D2
                     =PP3V3_DDC_LCD - @m39_lib.M39         88C6 94A7 94C7
                     =PP3V3_GPU - @m39_lib.M39             88C6 94B3
                     PP3V3_S0 - @m39_lib.M39               6A7 6B6 6D8 10D2 26B7
                                                           26C6 41D8 59D3 61C3 76D6
                                                           88C8
                     =PP3V3_S0_GPUBBCTL - @m39_lib.M39     85A7 88C6
                     =PP3V3_S0_GPUBBN - @m39_lib.M39       85B5 88C6
                     =PP3V3_S0_GPU - @m39_lib.M39          85B3 88C6 91D2 93A1
                     =PP3V3_S0_GPU_VDDR3 - @m39_lib.M39    88C6 88D3 91C6
                     =PP3V3_S0_LCD - @m39_lib.M39          88C6 94D7
                     =PP3V3_S0_GPUBBP - @m39_lib.M39       85B8 88C6
                     =PP3V3_S0_2V5REG - @m39_lib.M39       6A4 77D6
                     =PP3V3_S0_AIRPORT - @m39_lib.M39      6A4 53C2
                     =PP3V3_S0_PCI - @m39_lib.M39          6A4 44D5
                     =PP3V3_S0_AUDIO - @m39_lib.M39        6A4 68A6 68D7 72A6 72C8
                                                           72D5 73B8 73C2 74B5 74C5
                                                           74D5
                     =PP3V3_S0_IMVP - @m39_lib.M39         6A4 75D8
                     =PP3V3_S0_CK410 - @m39_lib.M39        6A4 33C8 33D3 33D8 34D4
                     =PPSPD_S0_MEM - @m39_lib.M39          6A4 28A7 29A3 29A7
                     =PP3V3_S0_TPM - @m39_lib.M39          6A4 67C7 67D4
                     =PP3V3_S0_SB_3V3_1V5_VCCHDA -         6A4 24C3 25C4
                     @m39_lib.M39
                     =PP3V3_S0_ODD_TSENS - @m39_lib.M39    6A4 66B4
                     =PP3V3_S0_HD_TSENS - @m39_lib.M39     6B4 66B5
                     =PP3V3_S0_FAN - @m39_lib.M39          6B4 59A8 59B7 65B7 65C7
                                                           66C7
                     =PP3V3_S0_PATA - @m39_lib.M39         6B4 38D3
                     =PP3V3_S0_SB_PM - @m39_lib.M39        6B4 26D4
                     =PP3V3_S0_SB_PCI - @m39_lib.M39       6B4 26D1
                     =PP3V3_S0_SB_VCC3_3_IDE -             6B4 24C3 25B3
                     @m39_lib.M39
                     =PP3V3_S0_SB_VCC3_3_PCI -             6B4 24B3 25A3
                     @m39_lib.M39
                     =PP3V3_S0_SB_VCC3_3 - @m39_lib.M39    6B4 24B5 24B5 25B8 25C6
                     =PP3V3_S0_NB_VCC_HV - @m39_lib.M39    6B4 17C6 19A8 19C7
                     =PP3V3_S0_SB_GPIO - @m39_lib.M39      6B4 21C3 21D3 23B3 23D5
                     =PP3V3_S0_SB_VCCLAN3_3 -              6A4 24D3 25D3
                     @m39_lib.M39
                     =PP3V3_S0_SB - @m39_lib.M39           6B4 22B5 25D8
                     PP3V3_S0 - @m39_lib.M39               6A7 6B6 6D8 10D2 26B7
                                                           26C6 41D8 59D3 61C3 76D6
                                                           88C8
                     =PPSPD_S0_MEM - @m39_lib.M39          6A4 28A7 29A3 29A7
                     =PP3V3_S0_TPM - @m39_lib.M39          6A4 67C7 67D4
                     =PP3V3_S0_SB_VCCLAN3_3 -              6A4 24D3 25D3
                     @m39_lib.M39
                     =PP3V3_S0_SB_VCC3_3_PCI -             6B4 24B3 25A3

                     @m39_lib.M39
                     =PP3V3_S0_SB_VCC3_3_IDE -             6B4 24C3 25B3
                     @m39_lib.M39
                     =PP3V3_S0_SB_VCC3_3 - @m39_lib.M39    6B4 24B5 24B5 25B8 25C6
                     =PP3V3_S0_SB_PM - @m39_lib.M39        6B4 26D4
                     =PP3V3_S0_SB_PCI - @m39_lib.M39       6B4 26D1
                     =PP3V3_S0_SB_GPIO - @m39_lib.M39      6B4 21C3 21D3 23B3 23D5
                     =PP3V3_S0_SB_3V3_1V5_VCCHDA -         6A4 24C3 25C4
                     @m39_lib.M39
                     =PP3V3_S0_SB - @m39_lib.M39           6B4 22B5 25D8
                     =PP3V3_S0_PCI - @m39_lib.M39          6A4 44D5
                     =PP3V3_S0_PATA - @m39_lib.M39         6B4 38D3
                     =PP3V3_S0_ODD_TSENS - @m39_lib.M39    6A4 66B4
                     =PP3V3_S0_NB_VCC_HV - @m39_lib.M39    6B4 17C6 19A8 19C7
                     =PP3V3_S0_NB_TVDAC - @m39_lib.M39     6B4 19C7
                     =PP3V3_S0_NB_PM - @m39_lib.M39        6B4
                     =PP3V3_S0_LCD - @m39_lib.M39          88C6 94D7
                     =PP3V3_S0_IMVP - @m39_lib.M39         6A4 75D8
                     =PP3V3_S0_HD_TSENS - @m39_lib.M39     6B4 66B5
                     =PP3V3_S0_GPU_CLOCKS - @m39_lib.M39   88C6
                     =PP3V3_S0_GPUBBP - @m39_lib.M39       85B8 88C6
                     =PP3V3_S0_GPUBBN - @m39_lib.M39       85B5 88C6
                     =PP3V3_S0_GPUBBCTL - @m39_lib.M39     85A7 88C6
                     =PP3V3_S0_GPU - @m39_lib.M39          85B3 88C6 91D2 93A1
                     =PP3V3_S0_FAN - @m39_lib.M39          6B4 59A8 59B7 65B7 65C7
                                                           66C7
                     =PP3V3_S0_CK410 - @m39_lib.M39        6A4 33C8 33D3 33D8 34D4
                     =PP3V3_S0_AUDIO - @m39_lib.M39        6A4 68A6 68D7 72A6 72C8
                                                           72D5 73B8 73C2 74B5 74C5
                                                           74D5
                     =PP3V3_S0_AIRPORT - @m39_lib.M39      6A4 53C2
                     =PP3V3_S0_2V5REG - @m39_lib.M39       6A4 77D6
                     =PP3V3_GPU - @m39_lib.M39             88C6 94B3
                     =PP3V3_DDC_LCD - @m39_lib.M39         88C6 94A7 94C7
                     =PP3V3_DDC_DVI - @m39_lib.M39         88C6 97D2
=PP3V3_S3_1V2REG     =PP3V3_S3_1V2REG - @m39_lib.M39       6D3 77B7
                     =PP3V3_S3_USB - @m39_lib.M39          6C3 49C5
                     =PP3V3_S3_VGASYNC - @m39_lib.M39      6C3 97A4 97B4
                     PP3V3_S3 - @m39_lib.M39               6A7 6D4 53C4 59C8 59D3
                                                           83B3
                     =PP3V3_S3_BT - @m39_lib.M39           6D3 47B3
                     =PP3V3_S3_TPM - @m39_lib.M39          6D3 67C2
                     =PP3V3_S3_ENET - @m39_lib.M39         6D3 41A5 41B3 41C3 41D6
                                                           41D8 42D3 42D8 43D2
                     PP3V3_S3 - @m39_lib.M39               6A7 6D4 53C4 59C8 59D3
                                                           83B3
                     =PP3V3_S3_VGASYNC - @m39_lib.M39      6C3 97A4 97B4
                     =PP3V3_S3_USB - @m39_lib.M39          6C3 49C5
                     =PP3V3_S3_TPM - @m39_lib.M39          6D3 67C2
                     =PP3V3_S3_ENET - @m39_lib.M39         6D3 41A5 41B3 41C3 41D6
                                                           41D8 42D3 42D8 43D2
                     =PP3V3_S3_BT - @m39_lib.M39           6D3 47B3
=PP3V3_S5_DEBUG      =PP3V3_S5_DEBUG - @m39_lib.M39        6D1 60D6
                     =PP3V3_S5_ROM - @m39_lib.M39          6D1 63D4
                     PP3V3_S5 - @m39_lib.M39               5D2 6C8 6C8 6D2 6D8 26C1
                                                           26C4 26C4 59A8 65B7 65D7
                                                           66D7 76D2 76D4 77B8 77C7
                                                           77C8 77C8 77D8 79A3 79A5
                                                           79B3 80A5 80B3 81A5 81A5
                                                           83C3
                     =PP3V3_S5_SMC - @m39_lib.M39          6D1 58C2 58D3 58D4 59A4
                                                           59A5 59C4 59D3 59D8
                     =PP3V3_S5_FW - @m39_lib.M39           6D1 44A6 44B2 44B7 44D5
                                                           44D7 45D6 46A8
                     =PP3V3_S5_SB_IO - @m39_lib.M39        6D1 22C6 27C6
                     =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA -      6D1 24C3
                     @m39_lib.M39
                     =PP3V3_S5_SB_VCCSUS3_3_USB -          6D1 24B3 25D1
                     @m39_lib.M39
                     =PP3V3_S5_SB_VCCSUS3_3 -              6D1 24A5 24B3 25B6 25D1
                     @m39_lib.M39
                     =PP3V3_S5_SB_PM - @m39_lib.M39        6D1 11B5 23D1
                     =PP3V3_S5_SB_USB - @m39_lib.M39       6D1 22D8
                     =PP3V3_S5_SB - @m39_lib.M39           6D1 23A7 23B3 23B7 23D4
                                                           23D8 25C8 26D8
                     PP3V3_S5 - @m39_lib.M39               5D2 6C8 6C8 6D2 6D8 26C1
                                                           26C4 26C4 59A8 65B7 65D7
                                                           66D7 76D2 76D4 77B8 77C7
                                                           77C8 77C8 77D8 79A3 79A5
                                                           79B3 80A5 80B3 81A5 81A5
                                                           83C3
                     =PP3V3_S5_SMC - @m39_lib.M39          6D1 58C2 58D3 58D4 59A4
                                                           59A5 59C4 59D3 59D8
                     =PP3V3_S5_SB_VCCSUS3_3_USB -          6D1 24B3 25D1
                     @m39_lib.M39
                     =PP3V3_S5_SB_VCCSUS3_3 -              6D1 24A5 24B3 25B6 25D1
                     @m39_lib.M39
                     =PP3V3_S5_SB_USB - @m39_lib.M39       6D1 22D8
                     =PP3V3_S5_SB_PM - @m39_lib.M39        6D1 11B5 23D1
                     =PP3V3_S5_SB_IO - @m39_lib.M39        6D1 22C6 27C6
                     =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA -      6D1 24C3
                     @m39_lib.M39
                     =PP3V3_S5_SB - @m39_lib.M39           6D1 23A7 23B3 23B7 23D4
                                                           23D8 25C8 26D8
                     =PP3V3_S5_ROM - @m39_lib.M39          6D1 63D4
                     =PP3V3_S5_FW - @m39_lib.M39           6D1 44A6 44B2 44B7 44D5
                                                           44D7 45D6 46A8
=PP5V_S0_AUDIO       =PP5V_S0_AUDIO - @m39_lib.M39         6A4 68A6
                     PP5V_S0_AUDIO - @m39_lib.M39          6A5
=PP5V_S0_DEBUG       =PP5V_S0_DEBUG - @m39_lib.M39         6A4 60C6
                     =PP5V_S0_DVI_DDC - @m39_lib.M39       88A6 97D6
                     =PP5V_S0_GPUISENS - @m39_lib.M39      85D2 88A6
                     PP5V_S0 - @m39_lib.M39                6A6 6D8 75D7 88B8 97D3
                     =PP5V_S0_GPUBBCTL - @m39_lib.M39      85A6 88B6
                     =PP5V_S0_SB - @m39_lib.M39            6A4 25D8
                     =PP5V_S0_PATA - @m39_lib.M39          6A4 38C4 38D3
                     PP5V_S0 - @m39_lib.M39                6A6 6D8 75D7 88B8 97D3
                     =PP5V_S0_SB - @m39_lib.M39            6A4 25D8
                     =PP5V_S0_PATA - @m39_lib.M39          6A4 38C4 38D3
                     =PP5V_S0_GPUISENS - @m39_lib.M39      85D2 88A6
                     =PP5V_S0_GPUBBCTL - @m39_lib.M39      85A6 88B6
                     =PP5V_S0_DVI_DDC - @m39_lib.M39       88A6 97D6
=PP5V_S0_GPUVCORE    =PP5V_S0_GPUVCORE - @m39_lib.M39      85D7 88D6
                     GPUVCORE_VCC - @m39_lib.M39           88D6
=PP5V_S0_MEMVTT      =PP5V_S0_MEMVTT - @m39_lib.M39        6C3 31C6
                     PP5V_S3 - @m39_lib.M39                6C4 59D6 83C3
                     =PP5V_S3_BNDI - @m39_lib.M39          6C3 47D4
                     =PP5V_S3_USB - @m39_lib.M39           6C3 47C8
                     PP5V_S3 - @m39_lib.M39                6C4 59D6 83C3
                     =PP5V_S3_USB - @m39_lib.M39           6C3 47C8
                     =PP5V_S3_BNDI - @m39_lib.M39          6C3 47D4
=PP5V_S5_SB          =PP5V_S5_SB - @m39_lib.M39            6D1 25C8
                     PP5V_S5 - @m39_lib.M39                5D2 6A8 6D2 6D7 59A5 79B3
                                                           79B3 80B3 81B3 83C3

=PP12V_GPU           =PP12V_GPU - @m39_lib.M39             88B6 94C8
                     PP12V_S0 - @m39_lib.M39               6A6 6D8 76B8 88B8
                     =PP12V_S0_FAN - @m39_lib.M39          6A4 65B6 65D7 66D6
                     PP12V_S0 - @m39_lib.M39               6A6 6D8 76B8 88B8
                     =PP12V_S0_FAN - @m39_lib.M39          6A4 65B6 65D7 66D6
=PP12V_S0_AUDIO_SPKR =PP12V_S0_AUDIO_SPKRAMP -             6A4 72D8
AMP                  @m39_lib.M39
                     PP12V_S0_AUDIO_SPKRAMP -              6A5
                     @m39_lib.M39
=PP12V_S5_CPU        =PP12V_S5_CPU - @m39_lib.M39          6C1 76D8
                     =PPVIN_S0_GPUVCORE - @m39_lib.M39     85D7 88B6
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                                                           80D7 81D7 83C5 83C5 88B8
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                     =PPVOUT_S0_GPUBBP_LDO -               85B5 88C6
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                     =PPVCORE_S0_GPU_REG - @m39_lib.M39    85C1 88D6
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                     =PPVCORE_S0_GPU_REG - @m39_lib.M39    85C1 88D6
                     =PPVCORE_S0_GPU_BBP - @m39_lib.M39    85B7 88D6
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ACZ_SDATAIN_CHIP     ACZ_SDATAIN_CHIP - @m39_lib.M39       68C6
ACZ_SDATAOUT         ACZ_SDATAOUT - @m39_lib.M39           21C7 68D7
ACZ_SYNC             ACZ_SYNC - @m39_lib.M39               21C7 68D7
AIRPORT_CLK100M_PCIE AIRPORT_CLK100M_PCIE_N -              34B4 34C2 53C6
_N                   @m39_lib.M39
AIRPORT_CLK100M_PCIE AIRPORT_CLK100M_PCIE_P -              34B4 34C2 53C6
_P                   @m39_lib.M39
AIRPORT_CONN_CLK     AIRPORT_CONN_CLK - @m39_lib.M39       53B5
AIRPORT_CONN_DATA    AIRPORT_CONN_DATA - @m39_lib.M39      53B5
AIRPORT_RST_L        AIRPORT_RST_L - @m39_lib.M39          6A7 53C5
AIRPORT_WAKE_L       AIRPORT_WAKE_L - @m39_lib.M39         53C6
ALL_SYS_PWRGD        ALL_SYS_PWRGD - @m39_lib.M39          26D5 58D7 77B6
ALS_GAIN             ALS_GAIN - @m39_lib.M39               58B5 59C6
                     NC_ALS_GAIN - @m39_lib.M39            59C5
ALS_LEFT             ALS_LEFT - @m39_lib.M39               58A7 59D5
                     TP_ALS_LEFT - @m39_lib.M39            59D3
ALS_RIGHT            ALS_RIGHT - @m39_lib.M39              58A7 59D5
                     TP_ALS_RIGHT - @m39_lib.M39           59D3
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                     TP_ATI_DVPCLK - @m39_lib.M39          95A8
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ATI_R2SET            ATI_R2SET - @m39_lib.M39              93A8 93B5
ATI_RSET             ATI_RSET - @m39_lib.M39               93A8 93B5
ATI_TDIODE_N         ATI_TDIODE_N - @m39_lib.M39           61C5 91A3
ATI_TDIODE_P         ATI_TDIODE_P - @m39_lib.M39           61C5 91A3
ATI_TESTEN           ATI_TESTEN - @m39_lib.M39             91A3
ATI_VREFG            ATI_VREFG - @m39_lib.M39              91D3
AUDLINDETH           AUDLINDETH - @m39_lib.M39             74C4
AUDSAMPCPN           AUDSAMPCPN - @m39_lib.M39             72C4
AUDSAMPCPP           AUDSAMPCPP - @m39_lib.M39             72C4
AUDSAMPINLN          AUDSAMPINLN - @m39_lib.M39            72D6
AUDSAMPINLP          AUDSAMPINLP - @m39_lib.M39            72C6
AUDSAMPINRN          AUDSAMPINRN - @m39_lib.M39            72C6
AUDSAMPINRP          AUDSAMPINRP - @m39_lib.M39            72C6
AUDSAMPOURTP         AUDSAMPOURTP - @m39_lib.M39           72C4
AUDSAMPOUTLN         AUDSAMPOUTLN - @m39_lib.M39           72C4
AUDSAMPOUTLP         AUDSAMPOUTLP - @m39_lib.M39           72C4
AUDSAMPOUTRN         AUDSAMPOUTRN - @m39_lib.M39           72C4
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AUD_ANALOG_FILT_1    AUD_ANALOG_FILT_1 - @m39_lib.M39      68C4
AUD_ANALOG_FILT_2    AUD_ANALOG_FILT_2 - @m39_lib.M39      68C4
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AUD_BI_PORT_A_R      AUD_BI_PORT_A_R - @m39_lib.M39        68C1 74B8
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                     AUD_BI_PORT_B_R - @m39_lib.M39        68B1 68C1 74B6
AUD_BI_PORT_C_L      AUD_BI_PORT_C_L - @m39_lib.M39        68C7 72D8
AUD_BI_PORT_C_R      AUD_BI_PORT_C_R - @m39_lib.M39        68C7 72C8
AUD_BI_PORT_D_L      AUD_BI_PORT_D_L - @m39_lib.M39        68C7 74B6
AUD_BI_PORT_D_R      AUD_BI_PORT_D_R - @m39_lib.M39        68C7 74B6
AUD_BI_PORT_E_L      AUD_BI_PORT_E_L - @m39_lib.M39        68C1 74B6
AUD_BI_PORT_E_R      AUD_BI_PORT_E_R - @m39_lib.M39        68C1 74B6
AUD_BI_PORT_F_L      AUD_BI_PORT_F_L - @m39_lib.M39        68C1 74C8
AUD_BI_PORT_F_R      AUD_BI_PORT_F_R - @m39_lib.M39        68C1 74C8
AUD_BYPASS           AUD_BYPASS - @m39_lib.M39             68C4
AUD_DEBOUNCE         AUD_DEBOUNCE - @m39_lib.M39           72B7
AUD_GPIO_0           AUD_GPIO_0 - @m39_lib.M39             68B6 68C7 74A6
AUD_GPIO_0_A         AUD_GPIO_0_A - @m39_lib.M39           68B8 72B8
AUD_GPIO_1           AUD_GPIO_1 - @m39_lib.M39             68A6 68C7 74A6
AUD_GPIO_1_A         AUD_GPIO_1_A - @m39_lib.M39           68A8 73C2
AUD_GPIO_2           AUD_GPIO_2 - @m39_lib.M39             68C7 74A6
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AUD_LI_DET_EMI	AUD_LI_DET_EMI - @m39_lib.M39	73D7
AUD_LI_DET_H	AUD_LI_DET_H - @m39_lib.M39	73D4 74C5
AUD_LI_DET_JACK	AUD_LI_DET_JACK - @m39_lib.M39	73D8
AUD_LI_GND_EMI	AUD_LI_GND_EMI - @m39_lib.M39	73C7
AUD_LI_GND_JACK	AUD_LI_GND_JACK - @m39_lib.M39	73D8
AUD_LI_L_EMI	AUD_LI_L_EMI - @m39_lib.M39	73D7
AUD_LI_L_JACK	AUD_LI_L_JACK - @m39_lib.M39	73D8
AUD_LI_R_EMI	AUD_LI_R_EMI - @m39_lib.M39	73D7
AUD_LI_R_JACK	AUD_LI_R_JACK - @m39_lib.M39	73D8
AUD_LO_DET1	AUD_LO_DET1 - @m39_lib.M39	73B8 74A5
AUD_LO_DET1_1	AUD_LO_DET1_1 - @m39_lib.M39	74A4 74B2
AUD_LO_DET1_EMI	AUD_LO_DET1_EMI - @m39_lib.M39	73B7
AUD_LO_DET1_INV	AUD_LO_DET1_INV - @m39_lib.M39	74B3
AUD_LO_DET1_JACK	AUD_LO_DET1_JACK - @m39_lib.M39	73B4
AUD_LO_DET2	AUD_LO_DET2 - @m39_lib.M39	73B8 74B5
AUD_LO_DET2_1	AUD_LO_DET2_1 - @m39_lib.M39	74B4
AUD_LO_DET2_EMI	AUD_LO_DET2_EMI - @m39_lib.M39	73B7
AUD_LO_DET2_JACK	AUD_LO_DET2_JACK - @m39_lib.M39	73B4
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AUD_LO_GND_JACK	AUD_LO_GND_JACK - @m39_lib.M39	73B4
AUD_LO_L_EMI	AUD_LO_L_EMI - @m39_lib.M39	73B7
AUD_LO_L_JACK	AUD_LO_L_JACK - @m39_lib.M39	73B4
AUD_LO_R_EMI	AUD_LO_R_EMI - @m39_lib.M39	73A7
AUD_LO_R_JACK	AUD_LO_R_JACK - @m39_lib.M39	73B4
AUD_MAX9714_CHOLD	AUD_MAX9714_CHOLD - @m39_lib.M39	72C4
AUD_MAX9714_VREG	AUD_MAX9714_VREG - @m39_lib.M39	72C5
AUD_MIC_IN_N	AUD_MIC_IN_N - @m39_lib.M39	73C6 74A6
AUD_MIC_IN_N_CONN	AUD_MIC_IN_N_CONN - @m39_lib.M39	47C2 73C4
AUD_MIC_IN_N_EMI	AUD_MIC_IN_N_EMI - @m39_lib.M39	73C5
AUD_MIC_IN_P	AUD_MIC_IN_P - @m39_lib.M39	73C6 74A6
AUD_MIC_IN_P_CONN	AUD_MIC_IN_P_CONN - @m39_lib.M39	47C2 73C4
AUD_MIC_IN_P_EMI	AUD_MIC_IN_P_EMI - @m39_lib.M39	73C5
AUD_MIC_P1	AUD_MIC_P1 - @m39_lib.M39	74A4
AUD_PORT_A_DET_L	AUD_PORT_A_DET_L - @m39_lib.M39	74B2
AUD_PORT_A_L	AUD_PORT_A_L - @m39_lib.M39	73B8 74B5
AUD_PORT_A_L1	AUD_PORT_A_L1 - @m39_lib.M39	74B7
AUD_PORT_A_R	AUD_PORT_A_R - @m39_lib.M39	73A8 74B5
AUD_PORT_A_R1	AUD_PORT_A_R1 - @m39_lib.M39	74B7
AUD_PORT_E_DET_L	AUD_PORT_E_DET_L - @m39_lib.M39	74B1
AUD_PORT_F_L	AUD_PORT_F_L - @m39_lib.M39	73D4 74C5
AUD_PORT_F_L1	AUD_PORT_F_L1 - @m39_lib.M39	74C7
AUD_PORT_F_R	AUD_PORT_F_R - @m39_lib.M39	73D4 74C5
AUD_PORT_F_R1	AUD_PORT_F_R1 - @m39_lib.M39	74C7
AUD_SAMP_FS1	AUD_SAMP_FS1 - @m39_lib.M39	72A6 72C5
AUD_SAMP_FS2	AUD_SAMP_FS2 - @m39_lib.M39	72A6 72C5
AUD_SAMP_G1	AUD_SAMP_G1 - @m39_lib.M39	72A6 72C5
AUD_SAMP_G2	AUD_SAMP_G2 - @m39_lib.M39	72A6 72C5
AUD_SAMP_INL_N	AUD_SAMP_INL_N - @m39_lib.M39	72C5
AUD_SAMP_INL_P	AUD_SAMP_INL_P - @m39_lib.M39	72C5
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AUD_SAMP_INR_P	AUD_SAMP_INR_P - @m39_lib.M39	72C5
AUD_SAMP_SHDN_L	AUD_SAMP_SHDN_L - @m39_lib.M39	72C5
AUD_SENSE_A	AUD_SENSE_A - @m39_lib.M39	68C1 74C5 74D7
AUD_SENSE_B	AUD_SENSE_B - @m39_lib.M39	68C1 74C5 74D5 74D7
AUD_SPDIF_GND	AUD_SPDIF_GND - @m39_lib.M39	73A3
AUD_SPDIF_IN	AUD_SPDIF_IN - @m39_lib.M39	68C1 74B6
AUD_SPDIF_OUT	AUD_SPDIF_OUT - @m39_lib.M39	68D1 73B8
AUD_SPDIF_OUT_CHIP	AUD_SPDIF_OUT_CHIP - @m39_lib.M39	68D4
AUD_SPDIF_OUT_EMI	AUD_SPDIF_OUT_EMI - @m39_lib.M39	73B7
AUD_SPDIF_OUT_JACK	AUD_SPDIF_OUT_JACK - @m39_lib.M39	73B5
AUD_SPKR_OUTL_N	AUD_SPKR_OUTL_N - @m39_lib.M39	72C1 73D3
AUD_SPKR_OUTL_P	AUD_SPKR_OUTL_P - @m39_lib.M39	72C1 73D3
AUD_SPKR_OUTR_N	AUD_SPKR_OUTR_N - @m39_lib.M39	72C1 73D3
AUD_SPKR_OUTR_P	AUD_SPKR_OUTR_P - @m39_lib.M39	72C1 73D3
AUD_TYPE_DET_EN	AUD_TYPE_DET_EN - @m39_lib.M39	74B3
AUD_VREF_FILT	AUD_VREF_FILT - @m39_lib.M39	68C4
AUD_VREF_PORT_B	AUD_VREF_PORT_B - @m39_lib.M39	68C1 74A3
BAL_IN_COM	BAL_IN_COM - @m39_lib.M39	68C7 74A7
BAL_IN_L	BAL_IN_L - @m39_lib.M39	68C7 74A7
BAL_IN_R	BAL_IN_R - @m39_lib.M39	68C7 74A7
BAT_1	BAT_1 - @m39_lib.M39	26C8
BAT_2	BAT_2 - @m39_lib.M39	26C8
BEEP	BEEP - @m39_lib.M39	68C6
BIOS_REC	BIOS_REC - @m39_lib.M39	23A6 23C5
BOOT_LPC_SPI_L	BOOT_LPC_SPI_L - @m39_lib.M39	22B3 58C7 60C6
C8509_P1	C8509_P1 - @m39_lib.M39	85C5
CEN	CEN - @m39_lib.M39	68B5 74B6
CK410_27M_NONSPREAD	CK410_27M_NONSPREAD - @m39_lib.M39	34A4 92C7
CK410_27M_SPREAD	CK410_27M_SPREAD - @m39_lib.M39	34A4 92C5
	GPU_GPIO_16 - @m39_lib.M39	91C3 92C3
CK410_CLK14P3M_TIMER	CK410_CLK14P3M_TIMER - @m39_lib.M39	33A4 34D6
CK410_CPU0_N	CK410_CPU0_N - @m39_lib.M39	33C4 34B6
CK410_CPU0_P	CK410_CPU0_P - @m39_lib.M39	33C4 34B6
CK410_CPU1_N	CK410_CPU1_N - @m39_lib.M39	33C4 34B6
CK410_CPU1_P	CK410_CPU1_P - @m39_lib.M39	33C4 34B6
CK410_CPU2_ITP_SRC10_N	CK410_CPU2_ITP_SRC10_N - @m39_lib.M39	33C4 34B6
CK410_CPU2_ITP_SRC10_P	CK410_CPU2_ITP_SRC10_P - @m39_lib.M39	33C4 34B6
CK410_DOT96_27M_NONSPREAD_P	CK410_DOT96_27M_NONSPREAD_P - @m39_lib.M39	33A4 34A6
CK410_DOT96_27M_SPREAD_N	CK410_DOT96_27M_SPREAD_N - @m39_lib.M39	33A4 34A6
CK410_FSA	CK410_FSA - @m39_lib.M39	34B8 34C4
CK410_FSB_TEST_MODE	CK410_FSB_TEST_MODE - @m39_lib.M39	33C6 34A8
CK410_FSC	CK410_FSC - @m39_lib.M39	34A8 34D4
CK410_IREF	CK410_IREF - @m39_lib.M39	33B6
CK410_LVDS_N	CK410_LVDS_N - @m39_lib.M39	33B4 34A6
	TP_CK410_LVDS_N - @m39_lib.M39	34A4
CK410_LVDS_P	CK410_LVDS_P - @m39_lib.M39	33B4 34A6
	TP_CK410_LVDS_P - @m39_lib.M39	34A4
CK410_PCI1_CLK	CK410_PCI1_CLK - @m39_lib.M39	33B6 34C6
CK410_PCI2_CLK	CK410_PCI2_CLK - @m39_lib.M39	33B6 34C6
CK410_PCI3_CLK	CK410_PCI3_CLK - @m39_lib.M39	33B6 34C6
CK410_PCI4_CLK	CK410_PCI4_CLK - @m39_lib.M39	33B6 34C6
CK410_PCI5_FCTSEL1	CK410_PCI5_FCTSEL1 - @m39_lib.M39	33B6 34D6
CK410_PCIF0_CLK	CK410_PCIF0_CLK - @m39_lib.M39	33B8 34B6
CK410_PCIF1_ITP_EN	CK410_PCIF1_ITP_EN - @m39_lib.M39	33B8 34B6
CK410_PD_VTT_PWRGD_L	CK410_PD_VTT_PWRGD_L - @m39_lib.M39	26A8 33A4
	VR_PWRGD_CK410_L - @m39_lib.M39	26A7 75C6
CK410_REF1_FCTSEL0	CK410_REF1_FCTSEL0 - @m39_lib.M39	33A4 34C6
CK410_SRC1_N	CK410_SRC1_N - @m39_lib.M39	33B4 34A6
CK410_SRC1_P	CK410_SRC1_P - @m39_lib.M39	33B4 34A6
CK410_SRC2_N	CK410_SRC2_N - @m39_lib.M39	33B4 34A6
CK410_SRC2_P	CK410_SRC2_P - @m39_lib.M39	33B4 34A6
CK410_SRC3_N	CK410_SRC3_N - @m39_lib.M39	33B4 34D3
CK410_SRC3_P	CK410_SRC3_P - @m39_lib.M39	33B4 34D3
CK410_SRC4_N	CK410_SRC4_N - @m39_lib.M39	33B4 34B6
CK410_SRC4_P	CK410_SRC4_P - @m39_lib.M39	33B4 34B6
CK410_SRC5_N	CK410_SRC5_N - @m39_lib.M39	33B4 34B6
CK410_SRC5_P	CK410_SRC5_P - @m39_lib.M39	33B4 34B6
CK410_SRC6_N	CK410_SRC6_N - @m39_lib.M39	33B4 34B6
CK410_SRC6_P	CK410_SRC6_P - @m39_lib.M39	33B4 34B6
CK410_SRC7_N	CK410_SRC7_N - @m39_lib.M39	33B4 34D3
CK410_SRC7_P	CK410_SRC7_P - @m39_lib.M39	33B4 34D3
CK410_SRC8_N	CK410_SRC8_N - @m39_lib.M39	33A4 34A6
CK410_SRC8_P	CK410_SRC8_P - @m39_lib.M39	33A4 34A6
CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L - @m39_lib.M39	33B4 34D8
CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L - @m39_lib.M39	33B4 34D8
CK410_SRC_CLKREQ6_L	CK410_SRC_CLKREQ6_L - @m39_lib.M39	33B4 53C6
CK410_SRC_CLKREQ8_L	CK410_SRC_CLKREQ8_L - @m39_lib.M39	33A4 34D8
CK410_USB48_FSA	CK410_USB48_FSA - @m39_lib.M39	33A4 34C6
CK410_XTAL_IN	CK410_XTAL_IN - @m39_lib.M39	33C6
CK410_XTAL_OUT	CK410_XTAL_OUT - @m39_lib.M39	33C6
CLK_NB_OE_L	CLK_NB_OE_L - @m39_lib.M39	14B6 33B4
CPUVCORE_ISENSE_CAL	CPUVCORE_ISENSE_CAL - @m39_lib.M39	76A5
CPU_A20M_L	CPU_A20M_L - @m39_lib.M39	5C8 7C7 21C4
CPU_BSEL<0>	CPU_BSEL<0> - @m39_lib.M39	7B4 34B8
CPU_BSEL<1>	CPU_BSEL<1> - @m39_lib.M39	7B4 34A8
CPU_BSEL<2>	CPU_BSEL<2> - @m39_lib.M39	7B4 34A8
CPU_COMP<0>	CPU_COMP<0> - @m39_lib.M39	7B2
CPU_COMP<1>	CPU_COMP<1> - @m39_lib.M39	7B2
CPU_COMP<2>	CPU_COMP<2> - @m39_lib.M39	7B2
CPU_COMP<3>	CPU_COMP<3> - @m39_lib.M39	7B2
CPU_DCIN_SENSE	CPU_DCIN_SENSE - @m39_lib.M39	76D7
CPU_DPRSTP_L	CPU_DPRSTP_L - @m39_lib.M39	7B3 21C4 75C6
CPU_DPSLP_L	CPU_DPSLP_L - @m39_lib.M39	7B3 21C4
CPU_FERR_L	CPU_FERR_L - @m39_lib.M39	7C7 21C2
CPU_GTLREF	CPU_GTLREF - @m39_lib.M39	5D4 7B4
CPU_HS_ZH607	CPU_HS_ZH607 - @m39_lib.M39	9D4
CPU_HS_ZH608	CPU_HS_ZH608 - @m39_lib.M39	9D3 66A4 66A6 66B4 66B6
CPU_HS_ZH609	CPU_HS_ZH609 - @m39_lib.M39	9D3
CPU_HS_ZH610	CPU_HS_ZH610 - @m39_lib.M39	9D2
CPU_IGNNE_L	CPU_IGNNE_L - @m39_lib.M39	5C8 7C7 21C4
CPU_INIT_L	CPU_INIT_L - @m39_lib.M39	5C8 7D6 21C4
CPU_INTR	CPU_INTR - @m39_lib.M39	5C8 7C7 21C4
CPU_ISENSE_OUT_R	CPU_ISENSE_OUT_R - @m39_lib.M39	76D3
CPU_ISENSE_R_NEG	CPU_ISENSE_R_NEG - @m39_lib.M39	76D4
CPU_ISENSE_R_POS	CPU_ISENSE_R_POS - @m39_lib.M39	76D4
CPU_NMI	CPU_NMI - @m39_lib.M39	5C8 7C7 21C4
CPU_PROCHOT_L	CPU_PROCHOT_L - @m39_lib.M39	7C6 59A8 59C7
CPU_PSI_L	CPU_PSI_L - @m39_lib.M39	7A3 75C6
CPU_PWRGD	CPU_PWRGD - @m39_lib.M39	7B3 21C4
CPU_RCIN_L	CPU_RCIN_L - @m39_lib.M39	21C4
CPU_SENSE_I_R	CPU_SENSE_I_R - @m39_lib.M39	76D7
CPU_SMI_L	CPU_SMI_L - @m39_lib.M39	5C8 7C7 21C4
CPU_STPCLK_L	CPU_STPCLK_L - @m39_lib.M39	5C8 7C7 21C4
CPU_TEST1	CPU_TEST1 - @m39_lib.M39	7B4
CPU_TEST2	CPU_TEST2 - @m39_lib.M39	7B4
CPU_THERMD_EXT_N	CPU_THERMD_EXT_N - @m39_lib.M39	10B6
CPU_THERMD_EXT_P	CPU_THERMD_EXT_P - @m39_lib.M39	10B6
CPU_THERMD_N	CPU_THERMD_N - @m39_lib.M39	7C6 10C6
CPU_THERMD_P	CPU_THERMD_P - @m39_lib.M39	7C6 10C6
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @m39_lib.M39	21C2
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @m39_lib.M39	8B6 75A4
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @m39_lib.M39	8B6 75A4
CPU_VID<0>	CPU_VID<0> - @m39_lib.M39	8B7 75C7
CPU_VID<1>	CPU_VID<1> - @m39_lib.M39	8B7 75C7
CPU_VID<2>	CPU_VID<2> - @m39_lib.M39	8B7 75C7
CPU_VID<3>	CPU_VID<3> - @m39_lib.M39	8B7 75C7
CPU_VID<4>	CPU_VID<4> - @m39_lib.M39	8B7 75C7
CPU_VID<5>	CPU_VID<5> - @m39_lib.M39	8B7 75C7
CPU_VID<6>	CPU_VID<6> - @m39_lib.M39	8B7 75D7
CPU_XDP_CLK_N	CPU_XDP_CLK_N - @m39_lib.M39	11B3 34B3
	FSB_CLK_XDP_N - @m39_lib.M39	34B4 34C2
CPU_XDP_CLK_P	CPU_XDP_CLK_P - @m39_lib.M39	11B3 34B3
	FSB_CLK_XDP_P - @m39_lib.M39	34B4 34C2
CRB_SV_DET	CRB_SV_DET - @m39_lib.M39	23B6 23C3
CRT_BLUE	CRT_BLUE - @m39_lib.M39	13B5 19D4
	=PPVCORE_S0_NB - @m39_lib.M39	6D4 16C8 16D3 19B6 19D5 19D7
	CRT_BLUE_L - @m39_lib.M39	13B5 19D4
	CRT_IREF - @m39_lib.M39	13B5 19D4
	CRT_GREEN_L - @m39_lib.M39	13B5 19D4
	CRT_GREEN - @m39_lib.M39	13B5 19D4
	PP2V5_S0_NB_VCCA_CRTDAC - @m39_lib.M39	17D6 19D4
	CRT_RED - @m39_lib.M39	13B5 19D4
	CRT_RED_L - @m39_lib.M39	13B5 19D4
	PP1V05_S0 - @m39_lib.M39	6D6 34A8 34B8 34C7 81C2
	=PP1V05_S0_CPU - @m39_lib.M39	5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 9C8 11B3 11C5 59A1 59A3
	=PPVCORE_S0_SB - @m39_lib.M39	6D4 24D3 25D3
	=PP1V05_S0_SB_CPU_IO - @m39_lib.M39	6D4 21C1 21C1 24C3 25C3
	=PP1V05_S0_NB_VTT - @m39_lib.M39	6D4 17D3 19B8 19D7
	=PP1V05_S0_FSB_NB - @m39_lib.M39	5D4 6D4 12A7 12B7 12C2 19D7
	PP2V5_S0_NB_VCCA_CRTDAC - @m39_lib.M39	17D6 19D4
	PP1V05_S0 - @m39_lib.M39	6D6 34A8 34B8 34C7 81C2
	CRT_RED_L - @m39_lib.M39	13B5 19D4
	CRT_RED - @m39_lib.M39	13B5 19D4
	CRT_IREF - @m39_lib.M39	13B5 19D4
	CRT_GREEN_L - @m39_lib.M39	13B5 19D4
	CRT_GREEN - @m39_lib.M39	13B5 19D4
	CRT_BLUE_L - @m39_lib.M39	13B5 19D4
	=PPVCORE_S0_SB - @m39_lib.M39	6D4 24D3 25D3
	=PPVCORE_S0_NB - @m39_lib.M39	6D4 16C8 16D3 19B6 19D5 19D7
	=PP1V05_S0_SB_CPU_IO - @m39_lib.M39	6D4 21C1 21C1 24C3 25C3
	=PP1V05_S0_NB_VTT - @m39_lib.M39	6D4 17D3 19B8 19D7
	=PP1V05_S0_NB - @m39_lib.M39	6D4 19D7
	=PP1V05_S0_FSB_NB - @m39_lib.M39	5D4 6D4 12A7 12B7 12C2 19D7
	=PP1V05_S0_CPU - @m39_lib.M39	5D4 6D4 7B5 7B7 7D5 7D5 8C7 9C8 9C8 11B3 11C5 59A1 59A3
CRT_DDC_CLK	CRT_DDC_CLK - @m39_lib.M39	13B5 19C4
	TP_CRT_DDC_CLK - @m39_lib.M39	19C5
CRT_DDC_DATA	CRT_DDC_DATA - @m39_lib.M39	13B5 19C4
	TP_CRT_DDC_DATA - @m39_lib.M39	19C5
DEBUG_RST_L	DEBUG_RST_L - @m39_lib.M39	6A7 60B6
DMI_IRCOMP_R	DMI_IRCOMP_R - @m39_lib.M39	22C2
DMI_N2S_N<0>	DMI_N2S_N<0> - @m39_lib.M39	5B8 14B4 22D2
DMI_N2S_N<1>	DMI_N2S_N<1> - @m39_lib.M39	14B4 22D2
DMI_N2S_N<2>	DMI_N2S_N<2> - @m39_lib.M39	14B4 22D2
DMI_N2S_N<3>	DMI_N2S_N<3> - @m39_lib.M39	14B4 22D2
DMI_N2S_P<0>	DMI_N2S_P<0> - @m39_lib.M39	5B8 14B4 22D2
DMI_N2S_P<1>	DMI_N2S_P<1> - @m39_lib.M39	14B4 22D2
DMI_N2S_P<2>	DMI_N2S_P<2> - @m39_lib.M39	14B4 22D2
DMI_N2S_P<3>	DMI_N2S_P<3> - @m39_lib.M39	14B4 22D2
DMI_S2N_N<0>	DMI_S2N_N<0> - @m39_lib.M39	5C7 14B4 22D2
DMI_S2N_N<1>	DMI_S2N_N<1> - @m39_lib.M39	14B4 22D2
DMI_S2N_N<2>	DMI_S2N_N<2> - @m39_lib.M39	14B4 22D2
DMI_S2N_N<3>	DMI_S2N_N<3> - @m39_lib.M39	14B4 22D2
DMI_S2N_P<0>	DMI_S2N_P<0> - @m39_lib.M39	5C7 14B4 22D2
DMI_S2N_P<1>	DMI_S2N_P<1> - @m39_lib.M39	14B4 22D2
DMI_S2N_P<2>	DMI_S2N_P<2> - @m39_lib.M39	14B4 22D2
DMI_S2N_P<3>	DMI_S2N_P<3> - @m39_lib.M39	14B4 22D2
DVI_DDC_CLK	DVI_DDC_CLK - @m39_lib.M39	97D2
DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @m39_lib.M39	97D3 97D5
DVI_DDC_DATA	DVI_DDC_DATA - @m39_lib.M39	97C2
DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @m39_lib.M39	97C3 97D5
DVI_HPD_UF	DVI_HPD_UF - @m39_lib.M39	97C3 97D5
ENET_C4106_2	ENET_C4106_2 - @m39_lib.M39	41D2
ENET_C4107_2	ENET_C4107_2 - @m39_lib.M39	41D2
ENET_C4117_1	ENET_C4117_1 - @m39_lib.M39	41B2
ENET_C4118_1	ENET_C4118_1 - @m39_lib.M39	41B2
ENET_CLK100M_PCIE_N	ENET_CLK100M_PCIE_N - @m39_lib.M39	5D5 34A4 34B2 41C5
ENET_CLK100M_PCIE_P	ENET_CLK100M_PCIE_P - @m39_lib.M39	5D5 34A4 34B2 41C5
ENET_CTRL12	ENET_CTRL12 - @m39_lib.M39	41C7 42B8
	TP_ENET_CTRL12 - @m39_lib.M39	42B7
ENET_CTRL25	ENET_CTRL25 - @m39_lib.M39	41C7 42C6
ENET_GATED_RST_L	ENET_GATED_RST_L - @m39_lib.M39	41C5 42D2
ENET_LED_ACT_L	ENET_LED_ACT_L - @m39_lib.M39	41C8 43C3
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @m39_lib.M39	41C8 43C3
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @m39_lib.M39	41C8 43C3
ENET_LED_LINK_L	ENET_LED_LINK_L - @m39_lib.M39	41C8 43C3
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @m39_lib.M39	41C7
ENET_MDI_N<0>	ENET_MDI_N<0> - @m39_lib.M39	41C2 43C7
ENET_MDI_N<1>	ENET_MDI_N<1> - @m39_lib.M39	41C2 43C7
ENET_MDI_N<2>	ENET_MDI_N<2> - @m39_lib.M39	41C2 43C7
ENET_MDI_N<3>	ENET_MDI_N<3> - @m39_lib.M39	41C2 43B7
ENET_MDI_P<0>	ENET_MDI_P<0> - @m39_lib.M39	41C2 43C7
ENET_MDI_P<1>	ENET_MDI_P<1> - @m39_lib.M39	41C2 43C7
ENET_MDI_P<2>	ENET_MDI_P<2> - @m39_lib.M39	41C2 43C7
ENET_MDI_P<3>	ENET_MDI_P<3> - @m39_lib.M39	41C2 43C7
ENET_MDI_R_N<0>	ENET_MDI_R_N<0> - @m39_lib.M39	43C6
ENET_MDI_R_N<1>	ENET_MDI_R_N<1> - @m39_lib.M39	43C6
ENET_MDI_R_N<2>	ENET_MDI_R_N<2> - @m39_lib.M39	43C6
ENET_MDI_R_N<3>	ENET_MDI_R_N<3> - @m39_lib.M39	43B6
ENET_MDI_R_P<0>	ENET_MDI_R_P<0> - @m39_lib.M39	43C6
ENET_MDI_R_P<1>	ENET_MDI_R_P<1> - @m39_lib.M39	43C6
ENET_MDI_R_P<2>	ENET_MDI_R_P<2> - @m39_lib.M39	43C6
ENET_MDI_R_P<3>	ENET_MDI_R_P<3> - @m39_lib.M39	43C6
ENET_PU_VDDO_TTL0	ENET_PU_VDDO_TTL0 - @m39_lib.M39	41C5
ENET_PU_VDDO_TTL1	ENET_PU_VDDO_TTL1 - @m39_lib.M39	41C5
ENET_RSET	ENET_RSET - @m39_lib.M39	41C7
ENET_RST_L	ENET_RST_L - @m39_lib.M39	6B7 42D3
ENET_VPD_CLK	ENET_VPD_CLK - @m39_lib.M39	41A2 41C4
ENET_VPD_DATA	ENET_VPD_DATA - @m39_lib.M39	41A2 41C4
ENET_XTALI	ENET_XTALI - @m39_lib.M39	41B5
ENET_XTALO	ENET_XTALO - @m39_lib.M39	41B5
F0_GATESLOWDN	F0_GATESLOWDN - @m39_lib.M39	65D5
F0_RCFEEDBK	F0_RCFEEDBK - @m39_lib.M39	65C5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @m39_lib.M39	65D6
F1_GATESLOWDN	F1_GATESLOWDN - @m39_lib.M39	65B5
F1_RCFEEDBK	F1_RCFEEDBK - @m39_lib.M39	65B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @m39_lib.M39	65B6
F2_GATESLOWDN	F2_GATESLOWDN - @m39_lib.M39	66D4
F2_RCFEEDBK	F2_RCFEEDBK - @m39_lib.M39	66C5
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @m39_lib.M39	66D5
FAN_0_OUT	FAN_0_OUT - @m39_lib.M39	65C4
FAN_0_PWR	FAN_0_PWR - @m39_lib.M39	65C4
FAN_1_CTL	FAN_1_CTL - @m39_lib.M39	65B7
	FAN_RPM1 - @m39_lib.M39	65B7
FAN_1_OUT	FAN_1_OUT - @m39_lib.M39	65B4
FAN_1_PWR	FAN_1_PWR - @m39_lib.M39	65B3
FAN_2_CTL	FAN_2_CTL - @m39_lib.M39	66D7
	FAN_RPM2 - @m39_lib.M39	66C7
FAN_2_OUT	FAN_2_OUT - @m39_lib.M39	66C4
FAN_2_PWR	FAN_2_PWR - @m39_lib.M39	66C3
FAN_TACH0	FAN_TACH0 - @m39_lib.M39	65C7
FAN_TACH1	FAN_TACH1 - @m39_lib.M39	65A7
FAN_TACH2	FAN_TACH2 - @m39_lib.M39	66C7
FB_A0_MF	FB_A0_MF - @m39_lib.M39	89A7
FB_A0_SEN	FB_A0_SEN - @m39_lib.M39	89A7
FB_A0_VREF0	FB_A0_VREF0 - @m39_lib.M39	89C7
FB_A0_VREF1	FB_A0_VREF1 - @m39_lib.M39	89C7
FB_A0_ZQ	FB_A0_ZQ - @m39_lib.M39	89A7
FB_A1_MF	FB_A1_MF - @m39_lib.M39	89A4
FB_A1_SEN	FB_A1_SEN - @m39_lib.M39	89A4
FB_A1_VREF0	FB_A1_VREF0 - @m39_lib.M39	89C4
FB_A1_VREF1	FB_A1_VREF1 - @m39_lib.M39	89C4
FB_A1_ZQ	FB_A1_ZQ - @m39_lib.M39	89A4
FB_A_BA<0>	FB_A_BA<0> - @m39_lib.M39	87D5 89A5 89A8
FB_A_BA<1>	FB_A_BA<1> - @m39_lib.M39	87D5 89A5 89A8
FB_A_BA<2>	FB_A_BA<2> - @m39_lib.M39	87D5 89A5 89A8
FB_A_CAS_L<0>	FB_A_CAS_L<0> - @m39_lib.M39	5B6 87B5 89A8
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FB_A_CKE<0>	FB_A_CKE<0> - @m39_lib.M39	5B6 87B5 89B8
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FB_A_CLK_N<0>	FB_A_CLK_N<0> - @m39_lib.M39	5B6 87B5 89B8
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FB_A_DQ<7>	FB_A_DQ<7> - @m39_lib.M39	87D7 89B6
FB_A_DQ<8>	FB_A_DQ<8> - @m39_lib.M39	5A6 5D6 87D7 89A6
FB_A_DQ<9>	FB_A_DQ<9> - @m39_lib.M39	87D7 89A6
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FB_A_DQ<17>	FB_A_DQ<17> - @m39_lib.M39	87D7 89A6
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FB_A_DQ<32>	FB_A_DQ<32> - @m39_lib.M39	5A6 5D6 87C7 89B2
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FB_A_DQ<34>	FB_A_DQ<34> - @m39_lib.M39	87C7 89B3
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FB_A_DQ<40>	FB_A_DQ<40> - @m39_lib.M39	5A6 5D6 87C7 89A2
FB_A_DQ<41>	FB_A_DQ<41> - @m39_lib.M39	87C7 89A3
FB_A_DQ<42>	FB_A_DQ<42> - @m39_lib.M39	87C7 89A3
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FB_A_DQ<44>	FB_A_DQ<44> - @m39_lib.M39	87B7 89A3
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FSB_A_L<29>	FSB_A_L<29> - @m39_lib.M39	7C7 12C4
FSB_A_L<30>	FSB_A_L<30> - @m39_lib.M39	7C7 12C4
FSB_A_L<31>	FSB_A_L<31> - @m39_lib.M39	7C7 12C4
FSB_BNR_L	FSB_BNR_L - @m39_lib.M39	5C7 7D6 12C4
FSB_BPRI_L	FSB_BPRI_L - @m39_lib.M39	7D6 12C4
FSB_BREQ0_L	FSB_BREQ0_L - @m39_lib.M39	5C7 7D6 12C4
FSB_CLK_CPU_N	FSB_CLK_CPU_N - @m39_lib.M39	5C8 7C6 34B4 34C2
FSB_CLK_CPU_P	FSB_CLK_CPU_P - @m39_lib.M39	5C8 7C6 34B4 34C2
FSB_CLK_NB_N	FSB_CLK_NB_N - @m39_lib.M39	5C7 12A6 34B4 34C2
FSB_CLK_NB_P	FSB_CLK_NB_P - @m39_lib.M39	5C7 12A6 34B4 34C2
FSB_CPURST_L	FSB_CPURST_L - @m39_lib.M39	5C8 7D6 11B5 12C4
FSB_DBSY_L	FSB_DBSY_L - @m39_lib.M39	5C7 7D6 12B4
FSB_DEFER_L	FSB_DEFER_L - @m39_lib.M39	7D6 12B4
FSB_DINV_L<0>	FSB_DINV_L<0> - @m39_lib.M39	5D7 5D8 7C4 12B4
FSB_DINV_L<1>	FSB_DINV_L<1> - @m39_lib.M39	5D7 5D8 7B4 12B4
FSB_DINV_L<2>	FSB_DINV_L<2> - @m39_lib.M39	5D7 5D8 7C2 12B4
FSB_DINV_L<3>	FSB_DINV_L<3> - @m39_lib.M39	5D7 5D8 7B2 12B4
FSB_DPWR_L	FSB_DPWR_L - @m39_lib.M39	5C7 7B3 12B4
FSB_DRDY_L	FSB_DRDY_L - @m39_lib.M39	7D6 12B4
FSB_DSTBN_L<0>	FSB_DSTBN_L<0> - @m39_lib.M39	5D7 5D8 7C4 12B4
FSB_DSTBN_L<1>	FSB_DSTBN_L<1> - @m39_lib.M39	5D7 5D8 7B4 12B4
FSB_DSTBN_L<2>	FSB_DSTBN_L<2> - @m39_lib.M39	5D7 5D8 7C2 12B4
FSB_DSTBN_L<3>	FSB_DSTBN_L<3> - @m39_lib.M39	5D7 5D8 7B2 12B4
FSB_DSTBP_L<0>	FSB_DSTBP_L<0> - @m39_lib.M39	5D7 5D8 7C4 12B4
FSB_DSTBP_L<1>	FSB_DSTBP_L<1> - @m39_lib.M39	5D7 5D8 7B4 12B4
FSB_DSTBP_L<2>	FSB_DSTBP_L<2> - @m39_lib.M39	5D7 5D8 7C2 12B4
FSB_DSTBP_L<3>	FSB_DSTBP_L<3> - @m39_lib.M39	5D7 5D8 7B2 12B4
FSB_D_L<0>	FSB_D_L<0> - @m39_lib.M39	5D7 5D8 7C4 12D6
FSB_D_L<1>	FSB_D_L<1> - @m39_lib.M39	7C4 12D6
FSB_D_L<2>	FSB_D_L<2> - @m39_lib.M39	7C4 12D6
FSB_D_L<3>	FSB_D_L<3> - @m39_lib.M39	7C4 12D6
FSB_D_L<4>	FSB_D_L<4> - @m39_lib.M39	7C4 12D6
FSB_D_L<5>	FSB_D_L<5> - @m39_lib.M39	7C4 12D6
FSB_D_L<6>	FSB_D_L<6> - @m39_lib.M39	7C4 12D6
FSB_D_L<7>	FSB_D_L<7> - @m39_lib.M39	7C4 12D6
FSB_D_L<8>	FSB_D_L<8> - @m39_lib.M39	7C4 12D6
FSB_D_L<9>	FSB_D_L<9> - @m39_lib.M39	7C4 12D6
FSB_D_L<10>	FSB_D_L<10> - @m39_lib.M39	7C4 12D6
FSB_D_L<11>	FSB_D_L<11> - @m39_lib.M39	7C4 12D6
FSB_D_L<12>	FSB_D_L<12> - @m39_lib.M39	7C4 12D6
FSB_D_L<13>	FSB_D_L<13> - @m39_lib.M39	7C4 12C6
FSB_D_L<14>	FSB_D_L<14> - @m39_lib.M39	7C4 12C6
FSB_D_L<15>	FSB_D_L<15> - @m39_lib.M39	7C4 12C6
FSB_D_L<16>	FSB_D_L<16> - @m39_lib.M39	5D7 5D8 7C4 12C6
FSB_D_L<17>	FSB_D_L<17> - @m39_lib.M39	7C4 12C6
FSB_D_L<18>	FSB_D_L<18> - @m39_lib.M39	7B4 12C6
FSB_D_L<19>	FSB_D_L<19> - @m39_lib.M39	7B4 12C6
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FSB_D_L<23>	FSB_D_L<23> - @m39_lib.M39	7B4 12C6
FSB_D_L<24>	FSB_D_L<24> - @m39_lib.M39	7B4 12C6
FSB_D_L<25>	FSB_D_L<25> - @m39_lib.M39	7B4 12C6
FSB_D_L<26>	FSB_D_L<26> - @m39_lib.M39	7B4 12C6
FSB_D_L<27>	FSB_D_L<27> - @m39_lib.M39	7B4 12C6
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FSB_D_L<32>	FSB_D_L<32> - @m39_lib.M39	7C2 12C6
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FSB_D_L<34>	FSB_D_L<34> - @m39_lib.M39	7C2 12C6
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FSB_D_L<39>	FSB_D_L<39> - @m39_lib.M39	7C2 12B6
FSB_D_L<40>	FSB_D_L<40> - @m39_lib.M39	7C2 12B6
FSB_D_L<41>	FSB_D_L<41> - @m39_lib.M39	5D7 5D8 7C2 12B6
FSB_D_L<42>	FSB_D_L<42> - @m39_lib.M39	7C2 12B6
FSB_D_L<43>	FSB_D_L<43> - @m39_lib.M39	7C2 12B6
FSB_D_L<44>	FSB_D_L<44> - @m39_lib.M39	7C2 12B6
FSB_D_L<45>	FSB_D_L<45> - @m39_lib.M39	7C2 12B6
FSB_D_L<46>	FSB_D_L<46> - @m39_lib.M39	7C2 12B6
FSB_D_L<47>	FSB_D_L<47> - @m39_lib.M39	7C2 12B6
FSB_D_L<48>	FSB_D_L<48> - @m39_lib.M39	7C2 12B6
FSB_D_L<49>	FSB_D_L<49> - @m39_lib.M39	7C2 12B6
FSB_D_L<50>	FSB_D_L<50> - @m39_lib.M39	7B2 12B6
FSB_D_L<51>	FSB_D_L<51> - @m39_lib.M39	7B2 12B6
FSB_D_L<52>	FSB_D_L<52> - @m39_lib.M39	7B2 12B6
FSB_D_L<53>	FSB_D_L<53> - @m39_lib.M39	7B2 12B6
FSB_D_L<54>	FSB_D_L<54> - @m39_lib.M39	7B2 12B6
FSB_D_L<55>	FSB_D_L<55> - @m39_lib.M39	7B2 12B6
FSB_D_L<56>	FSB_D_L<56> - @m39_lib.M39	7B2 12B6
FSB_D_L<57>	FSB_D_L<57> - @m39_lib.M39	7B2 12B6
FSB_D_L<58>	FSB_D_L<58> - @m39_lib.M39	7B2 12B6
FSB_D_L<59>	FSB_D_L<59> - @m39_lib.M39	5D7 5D8 7B2 12B6
FSB_D_L<60>	FSB_D_L<60> - @m39_lib.M39	7B2 12B6
FSB_D_L<61>	FSB_D_L<61> - @m39_lib.M39	7B2 12B6
FSB_D_L<62>	FSB_D_L<62> - @m39_lib.M39	7B2 12B6
FSB_D_L<63>	FSB_D_L<63> - @m39_lib.M39	7B2 12B6
FSB_HITM_L	FSB_HITM_L - @m39_lib.M39	5C7 7D6 12B4
FSB_HIT_L	FSB_HIT_L - @m39_lib.M39	5C7 7D6 12B4
FSB_IERR_L	FSB_IERR_L - @m39_lib.M39	7D6
FSB_LOCK_L	FSB_LOCK_L - @m39_lib.M39	5D7 5D8 7D6 12B4
FSB_REQ_L<0>	FSB_REQ_L<0> - @m39_lib.M39	5C7 7D7 12B4
FSB_REQ_L<1>	FSB_REQ_L<1> - @m39_lib.M39	5C7 7D7 12B4
FSB_REQ_L<2>	FSB_REQ_L<2> - @m39_lib.M39	5C7 7D7 12A4
FSB_REQ_L<3>	FSB_REQ_L<3> - @m39_lib.M39	5C7 7D7 12A4
FSB_REQ_L<4>	FSB_REQ_L<4> - @m39_lib.M39	5C7 7D7 12A4
FSB_RS_L<0>	FSB_RS_L<0> - @m39_lib.M39	7D6 12A4
FSB_RS_L<1>	FSB_RS_L<1> - @m39_lib.M39	7D6 12A4
FSB_RS_L<2>	FSB_RS_L<2> - @m39_lib.M39	7D6 12A4
FSB_SLPCPU_L	FSB_SLPCPU_L - @m39_lib.M39	7A3 12A4
FSB_TRDY_L	FSB_TRDY_L - @m39_lib.M39	7D6 12A4
FWH_INIT_L	FWH_INIT_L - @m39_lib.M39	21C4 59C5 60C3
	SMC_CPU_INIT_3_3_L - @m39_lib.M39	58D5 59C6
FWH_MFG_MODE	FWH_MFG_MODE - @m39_lib.M39	23A6 23C5
FW_A_TPA_N	FW_A_TPA_N - @m39_lib.M39	44C3 46C8
	FW_PORT0_TPA_N - @m39_lib.M39	46C5 46C6
FW_A_TPA_P	FW_A_TPA_P - @m39_lib.M39	44C3 46C8
	FW_PORT0_TPA_P - @m39_lib.M39	46C5 46C6
FW_A_TPBIAS	FW_A_TPBIAS - @m39_lib.M39	44C4 46C8
FW_A_TPB_N	FW_A_TPB_N - @m39_lib.M39	44C3 46C8
	FW_PORT0_TPB_N - @m39_lib.M39	46C5 46C6
FW_A_TPB_P	FW_A_TPB_P - @m39_lib.M39	44C3 46C8
	FW_PORT0_TPB_P - @m39_lib.M39	46C5 46C6
FW_B_TPA_N	FW_B_TPA_N - @m39_lib.M39	44C3 46C8
	FW_PORT1_TPA_N - @m39_lib.M39	46B5 46C6
FW_B_TPA_P	FW_B_TPA_P - @m39_lib.M39	44C3 46C8
	FW_PORT1_TPA_P - @m39_lib.M39	46B5 46C6
FW_B_TPBIAS	FW_B_TPBIAS - @m39_lib.M39	44C4 46C8
FW_B_TPB_N	FW_B_TPB_N - @m39_lib.M39	44C3 46C8
	FW_PORT1_TPB_N - @m39_lib.M39	46B5 46C6
FW_B_TPB_P	FW_B_TPB_P - @m39_lib.M39	44C3 46C8
	FW_PORT1_TPB_P - @m39_lib.M39	46B5 46C6
FW_CARDBUS_L	FW_CARDBUS_L - @m39_lib.M39	44B5
FW_CONTENDER	FW_CONTENDER - @m39_lib.M39	44B3
FW_CPS	FW_CPS - @m39_lib.M39	44C3
FW_C_TPA_N	FW_C_TPA_N - @m39_lib.M39	44C3 46B8
	TP_FW_C_TPA_N - @m39_lib.M39	46B7
FW_C_TPA_P	FW_C_TPA_P - @m39_lib.M39	44C3 46B8
	TP_FW_C_TPA_P - @m39_lib.M39	46B7
FW_C_TPBIAS	FW_C_TPBIAS - @m39_lib.M39	44C4 46B8
	TP_FW_C_TPBIAS - @m39_lib.M39	46B7
FW_C_TPB_N	FW_C_TPB_N - @m39_lib.M39	44C3 46A8
	TP_FW_C_TPB_N - @m39_lib.M39	46A7
FW_C_TPB_P	FW_C_TPB_P - @m39_lib.M39	44C3 46A8
	TP_FW_C_TPB_P - @m39_lib.M39	46A7
FW_PC0	FW_PC0 - @m39_lib.M39	44B3
FW_PC1	FW_PC1 - @m39_lib.M39	44B3
FW_PC2	FW_PC2 - @m39_lib.M39	44B3
FW_PORT0_TPA_FL_N	FW_PORT0_TPA_FL_N - @m39_lib.M39	46C2
FW_PORT0_TPA_FL_P	FW_PORT0_TPA_FL_P - @m39_lib.M39	46C2
FW_PORT0_TPB_FL_N	FW_PORT0_TPB_FL_N - @m39_lib.M39	46C2
FW_PORT0_TPB_FL_P	FW_PORT0_TPB_FL_P - @m39_lib.M39	46C2
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @m39_lib.M39	46B2
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @m39_lib.M39	46B2
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @m39_lib.M39	46B2
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @m39_lib.M39	46B2
FW_R0	FW_R0 - @m39_lib.M39	44C4
FW_R1	FW_R1 - @m39_lib.M39	44C4
FW_RESET_L	FW_RESET_L - @m39_lib.M39	44C2 44C3
FW_ROM_CLK	FW_ROM_CLK - @m39_lib.M39	44B4
FW_SE	FW_SE - @m39_lib.M39	44B3
FW_SM	FW_SM - @m39_lib.M39	44B3
FW_TEST	FW_TEST - @m39_lib.M39	44B3
FW_TPA_C<0>	FW_TPA_C<0> - @m39_lib.M39	46B8
FW_TPA_C<1>	FW_TPA_C<1> - @m39_lib.M39	46B7
FW_VP	FW_VP - @m39_lib.M39	46D4
FW_VP_R	FW_VP_R - @m39_lib.M39	46D5
FW_XTAL_X0	FW_XTAL_X0 - @m39_lib.M39	44D2 44D3
FW_XTAL_XI	FW_XTAL_XI - @m39_lib.M39	44D2 44D3
FW_XTAL_XR	FW_XTAL_XR - @m39_lib.M39	44D2
GATE_3V3_S3	GATE_3V3_S3 - @m39_lib.M39	83B4
GATE_5V_S3	GATE_5V_S3 - @m39_lib.M39	83C4
GND_AUDIO	GND_AUDIO - @m39_lib.M39	6C2 74D2
GND_AUDIO_CODEC	GND_AUDIO_CODEC - @m39_lib.M39	68A6 68B7 68D2 72B8 72C8 73A8 73C2 73D4 74A3 74A5 74A6 74A7 74B5 74B7 74C1 74C2 74C8 74D1
GND_AUDIO_MIC_CONN	GND_AUDIO_MIC_CONN - @m39_lib.M39	47C2 73C4
GND_AUDIO_SPKRAMP	GND_AUDIO_SPKRAMP - @m39_lib.M39	6C2 72B1 74D2
GND_AUDIO_SPKRAMP_PLANE	GND_AUDIO_SPKRAMP_PLANE - @m39_lib.M39	72A6 72B2 72B6 72D2 72D8 74C2
GND_BNDI	GND_BNDI - @m39_lib.M39	47B2 47D2
GND_CHASSIS_AUDIO_EXTERNAL	GND_CHASSIS_AUDIO_EXTERNAL - @m39_lib.M39	6B2 73A8 73C7 73D8 74C1 74D2
	GND_CHASSIS_IO_LEFT - @m39_lib.M39	6B2
	GND_CHASSIS_USB - @m39_lib.M39	6B2 47A4 47B4 47C4
	GND_CHASSIS_IO_LEFT - @m39_lib.M39	6B2
GND_CHASSIS_AUDIO_INTERNAL	GND_CHASSIS_AUDIO_INTERNAL - @m39_lib.M39	6A2 73C6
	GND_CHASSIS_BNDI - @m39_lib.M39	6A2 47C2 47C2 47D2
GND_CHASSIS_FIREWIRE	GND_CHASSIS_FIREWIRE - @m39_lib.M39	6B2 46A1 46C1
	GND_CHASSIS_RJ45 - @m39_lib.M39	6B2 43C6
	GND_CHASSIS_VGA - @m39_lib.M39	6B2 97C4
	GND_CHASSIS_RJ45 - @m39_lib.M39	6B2 43C6
	GND_CHASSIS_IO_RIGHT - @m39_lib.M39	6B1
GND_CPU_ISENSE_OPAMP	GND_CPU_ISENSE_OPAMP - @m39_lib.M39	76D3
GND_GPUVCORE_SGND	GND_GPUVCORE_SGND - @m39_lib.M39	85C7
GND_GPU_A2VSSN	GND_GPU_A2VSSN - @m39_lib.M39	93B7
GND_GPU_A2VSSQ	GND_GPU_A2VSSQ - @m39_lib.M39	93B7
GND_GPU_AVSSN	GND_GPU_AVSSN - @m39_lib.M39	93C7
GND_GPU_AVSSQ	GND_GPU_AVSSQ - @m39_lib.M39	93C7
GND_GPU_LPVSS	GND_GPU_LPVSS - @m39_lib.M39	93B7
GND_GPU_LVSSR	GND_GPU_LVSSR - @m39_lib.M39	93A7
GND_GPU_MPVSS	GND_GPU_MPVSS - @m39_lib.M39	91A5
GND_GPU_PCIE_PVSS	GND_GPU_PCIE_PVSS - @m39_lib.M39	84B8
GND_GPU_PVSS	GND_GPU_PVSS - @m39_lib.M39	91A5
GND_GPU_TPVSS	GND_GPU_TPVSS - @m39_lib.M39	93C7
GND_GPU_TXVSSR	GND_GPU_TXVSSR - @m39_lib.M39	93C7
GND_GPU_VSSRH0	GND_GPU_VSSRH0 - @m39_lib.M39	87A7
GND_GPU_VSSRH1	GND_GPU_VSSRH1 - @m39_lib.M39	87A4
GND_IMVP6_SGND	GND_IMVP6_SGND - @m39_lib.M39	75A4 75B6 75B8 75D7
GND_NB_VSSA_LVDS	GND_NB_VSSA_LVDS - @m39_lib.M39	17C6 19C2
	TP_GND_NB_VSSA_LVDS - @m39_lib.M39	19C1
GND_NEXT_TO_SMC	GND_NEXT_TO_SMC - @m39_lib.M39	59B2 76C2
GND_SMC_AVSS	GND_SMC_AVSS - @m39_lib.M39	58B2 58C4 59A3 59B3 76B2 76B6 76C2 76C5 85C1
GND_USB_PORT0	GND_USB_PORT0 - @m39_lib.M39	47D5
GND_USB_PORT1	GND_USB_PORT1 - @m39_lib.M39	47C5
GND_USB_PORT2	GND_USB_PORT2 - @m39_lib.M39	47A5
GPUBBN_D	GPUBBN_D - @m39_lib.M39	85A3
GPUBBN_D_RC	GPUBBN_D_RC - @m39_lib.M39	85A3
GPUBBN_FB	GPUBBN_FB - @m39_lib.M39	85A3
GPUBBN_SW	GPUBBN_SW - @m39_lib.M39	85A4
GPUBBP_ADJ	GPUBBP_ADJ - @m39_lib.M39	85B7
GPUBBP_ADJ_LOW	GPUBBP_ADJ_LOW - @m39_lib.M39	85A7
GPUBB_EN	GPUBB_EN - @m39_lib.M39	85A4 85A6 85B8
GPUBB_EN_L	GPUBB_EN_L - @m39_lib.M39	85A1 85A5 85B7
GPUISENS_NEG	GPUISENS_NEG - @m39_lib.M39	85D3
GPUISENS_NTC	GPUISENS_NTC - @m39_lib.M39	85D3
GPUISENS_POS	GPUISENS_POS - @m39_lib.M39	85D3
GPUISENS_RC	GPUISENS_RC - @m39_lib.M39	85D3
GPUVCORE_BOOT	GPUVCORE_BOOT - @m39_lib.M39	85C5
GPUVCORE_COMP	GPUVCORE_COMP - @m39_lib.M39	85C7
GPUVCORE_COMP_R	GPUVCORE_COMP_R - @m39_lib.M39	85C7
GPUVCORE_EN	GPUVCORE_EN - @m39_lib.M39	85C8 88A8
GPUVCORE_FB	GPUVCORE_FB - @m39_lib.M39	85C7
GPUVCORE_FB_LOW	GPUVCORE_FB_LOW - @m39_lib.M39	85C3
GPUVCORE_FCCM	GPUVCORE_FCCM - @m39_lib.M39	85C7
GPUVCORE_FSET	GPUVCORE_FSET - @m39_lib.M39	85C7
GPUVCORE_IOUT	GPUVCORE_IOUT - @m39_lib.M39	59C5 85D1
	SMC_GPU_ISENSE - @m39_lib.M39	58D5 59C6
GPUVCORE_ISEN	GPUVCORE_ISEN - @m39_lib.M39	85C5
GPUVCORE_ISENSE_CAL	GPUVCORE_ISENSE_CAL - @m39_lib.M39	76A4
GPUVCORE_LG	GPUVCORE_LG - @m39_lib.M39	85C5
GPUVCORE_PGOOD	GPUVCORE_PGOOD - @m39_lib.M39	77A4 85C8
GPUVCORE_PHASE	GPUVCORE_PHASE - @m39_lib.M39	85C5
GPUVCORE_UG	GPUVCORE_UG - @m39_lib.M39	85C5
GPU_B2	GPU_B2 - @m39_lib.M39	93B3 97B8
GPU_BB_EN	GPU_BB_EN - @m39_lib.M39	85A7
GPU_CLK27M	GPU_CLK27M - @m39_lib.M39	92C6
	GPU_XTALIN - @m39_lib.M39	91A5 92C5
GPU_CLK100M_PCIE_N	GPU_CLK100M_PCIE_N - @m39_lib.M39	5C6 34A4 34B2 84A5
GPU_CLK100M_PCIE_P	GPU_CLK100M_PCIE_P - @m39_lib.M39	5C6 34A4 34B2 84A5
GPU_DDC_A_CLK	GPU_DDC_A_CLK - @m39_lib.M39	93A3 97D1
GPU_DDC_A_DATA	GPU_DDC_A_DATA - @m39_lib.M39	93A3 97C1
GPU_DDC_B_CLK	GPU_DDC_B_CLK - @m39_lib.M39	88B1 93A3
	TP_GPU_DDC_B_CLK - @m39_lib.M39	88B3
GPU_DDC_B_DATA	GPU_DDC_B_DATA - @m39_lib.M39	88B1 93A3
	TP_GPU_DDC_B_DATA - @m39_lib.M39	88B3
GPU_DDC_C_CLK	GPU_DDC_C_CLK - @m39_lib.M39	93A1 93A3 94A7 94C7
GPU_DDC_C_DATA	GPU_DDC_C_DATA - @m39_lib.M39	93A1 93A3 94A6 94C7
GPU_DIGON	GPU_DIGON - @m39_lib.M39	91C3 94C8
GPU_EXT_TDIODE_N	GPU_EXT_TDIODE_N - @m39_lib.M39	61B7
GPU_EXT_TDIODE_P	GPU_EXT_TDIODE_P - @m39_lib.M39	61C7
GPU_G2	GPU_G2 - @m39_lib.M39	93B3 97A8
GPU_GENERICA	GPU_GENERICA - @m39_lib.M39	91C3 95B4
	TP_GPU_GENERICA - @m39_lib.M39	95B6
GPU_GENERICB	GPU_GENERICB - @m39_lib.M39	91C3 95B4
	TP_GPU_GENERICB - @m39_lib.M39	95B6
GPU_GENERICC	GPU_GENERICC - @m39_lib.M39	91C3 95B4
	TP_GPU_GENERICC - @m39_lib.M39	95B6
GPU_GENERICD	GPU_GENERICD - @m39_lib.M39	85A7 91C3
GPU_GPIO_0	GPU_GPIO_0 - @m39_lib.M39	88D5 91D3 94C3
GPU_GPIO_1	GPU_GPIO_1 - @m39_lib.M39	88D5 91D3
GPU_GPIO_2	GPU_GPIO_2 - @m39_lib.M39	88D5 91D3
GPU_GPIO_3	GPU_GPIO_3 - @m39_lib.M39	88D5 91D3
GPU_GPIO_4	GPU_GPIO_4 - @m39_lib.M39	88C5 91D3
GPU_GPIO_5	GPU_GPIO_5 - @m39_lib.M39	88C5 91D3
GPU_GPIO_6	GPU_GPIO_6 - @m39_lib.M39	88C5 91D3
GPU_GPIO_7	GPU_GPIO_7 - @m39_lib.M39	88C3 91D3
	TP_GPU_GPIO_7 - @m39_lib.M39	88C5
GPU_GPIO_8	GPU_GPIO_8 - @m39_lib.M39	88C5 91D3
GPU_GPIO_9	GPU_GPIO_9 - @m39_lib.M39	88C5 91C3
GPU_GPIO_10	GPU_GPIO_10 - @m39_lib.M39	88C3 91C3
	NC_GPU_GPIO_10 - @m39_lib.M39	88C5
GPU_GPIO_11	GPU_GPIO_11 - @m39_lib.M39	88B5 91C3
GPU_GPIO_12	GPU_GPIO_12 - @m39_lib.M39	88C5 91C3
GPU_GPIO_13	GPU_GPIO_13 - @m39_lib.M39	88C5 91C3
GPU_GPIO_14	GPU_GPIO_14 - @m39_lib.M39	88C1 91C3
	TP_GPU_GPIO_14 - @m39_lib.M39	88C3
GPU_GPIO_15	GPU_GPIO_15 - @m39_lib.M39	88B4 91C3
	GPU_VCORE_LOW - @m39_lib.M39	85B4 88B5
GPU_GPIO_17	GPU_GPIO_17 - @m39_lib.M39	88C1 91C3
	TP_GPU_GPIO_17 - @m39_lib.M39	88C3
GPU_GPIO_18	GPU_GPIO_18 - @m39_lib.M39	91D5 95B4
GPU_GPIO_19	GPU_GPIO_19 - @m39_lib.M39	91D5 95B4
GPU_GPIO_20	GPU_GPIO_20 - @m39_lib.M39	91D5 95B4
GPU_GPIO_21	GPU_GPIO_21 - @m39_lib.M39	91D5 95B4
GPU_GPIO_22	GPU_GPIO_22 - @m39_lib.M39	91D5 95B4
GPU_GPIO_23	GPU_GPIO_23 - @m39_lib.M39	91D5 95B4
GPU_GPIO_24	GPU_GPIO_24 - @m39_lib.M39	88B5 91D5
GPU_GPIO_25	GPU_GPIO_25 - @m39_lib.M39	91D5 95C4
GPU_GPIO_26	GPU_GPIO_26 - @m39_lib.M39	91D5 95C4
GPU_GPIO_27	GPU_GPIO_27 - @m39_lib.M39	88B5 91D5
GPU_GPIO_28	GPU_GPIO_28 - @m39_lib.M39	88B5 91D5
GPU_GPIO_29	GPU_GPIO_29 - @m39_lib.M39	88B5 91C5
GPU_GPIO_30	GPU_GPIO_30 - @m39_lib.M39	91C5 95C4
GPU_GPIO_31	GPU_GPIO_31 - @m39_lib.M39	91C5 95C4
GPU_GPIO_32	GPU_GPIO_32 - @m39_lib.M39	91C5 95C4
GPU_GPIO_33	GPU_GPIO_33 - @m39_lib.M39	91C5 95C4
GPU_GPIO_34	GPU_GPIO_34 - @m39_lib.M39	91C5 95C4
GPU_H2SYNC	GPU_H2SYNC - @m39_lib.M39	93B3 97A4
GPU_HPD	GPU_HPD - @m39_lib.M39	93A5 97C1
GPU_HSYNC_BUF	GPU_HSYNC_BUF - @m39_lib.M39	97A4
GPU_MEMTEST	GPU_MEMTEST - @m39_lib.M39	87A3
GPU_MVREFD0	GPU_MVREFD0 - @m39_lib.M39	87B7
GPU_MVREFD1	GPU_MVREFD1 - @m39_lib.M39	87B3
GPU_MVREFS0	GPU_MVREFS0 - @m39_lib.M39	87B7
GPU_MVREFS1	GPU_MVREFS1 - @m39_lib.M39	87B3
GPU_PCIE_CALI	GPU_PCIE_CALI - @m39_lib.M39	84A3
GPU_PCIE_CALRN	GPU_PCIE_CALRN - @m39_lib.M39	84A3
GPU_PCIE_CALRP	GPU_PCIE_CALRP - @m39_lib.M39	84A3
GPU_PWM_RST_L	GPU_PWM_RST_L - @m39_lib.M39	6C7 94B3
GPU_R2	GPU_R2 - @m39_lib.M39	93B3 97A8
GPU_TEST_MCLK	GPU_TEST_MCLK - @m39_lib.M39	87A3
GPU_TEST_YCLK	GPU_TEST_YCLK - @m39_lib.M39	87A3
GPU_TV_C	GPU_TV_C - @m39_lib.M39	88B1 93B3
	TP_GPU_TV_C - @m39_lib.M39	88B3
GPU_TV_COMP	GPU_TV_COMP - @m39_lib.M39	88B1 93B3
	TP_GPU_TV_COMP - @m39_lib.M39	88B3
GPU_TV_Y	GPU_TV_Y - @m39_lib.M39	88B1 93B3
	TP_GPU_TV_Y - @m39_lib.M39	88B3
GPU_V2SYNC	GPU_V2SYNC - @m39_lib.M39	93B3 97B4
GPU_VARY_BL	GPU_VARY_BL - @m39_lib.M39	91C3 94B3
GPU_VCORE_HIGH	GPU_VCORE_HIGH - @m39_lib.M39	85A8 85B4
GPU_VCORE_HIGH_RC	GPU_VCORE_HIGH_RC - @m39_lib.M39	85B3
GPU_VGA_B	GPU_VGA_B - @m39_lib.M39	88C1 93C3
	TP_GPU_VGA_B - @m39_lib.M39	88C3
GPU_VGA_G	GPU_VGA_G - @m39_lib.M39	88C1 93C3
	TP_GPU_VGA_G - @m39_lib.M39	88C3
GPU_VGA_HSYNC	GPU_VGA_HSYNC - @m39_lib.M39	88B1 93B3
	TP_GPU_VGA_HSYNC - @m39_lib.M39	88B3
GPU_VGA_R	GPU_VGA_R - @m39_lib.M39	88C1 93C3
	TP_GPU_VGA_R - @m39_lib.M39	88C3
GPU_VGA_VSYNC	GPU_VGA_VSYNC - @m39_lib.M39	88B1 93B3
	TP_GPU_VGA_VSYNC - @m39_lib.M39	88B3
GPU_VSYNC_BUF	GPU_VSYNC_BUF - @m39_lib.M39	97A4
GPU_XTALOUT	GPU_XTALOUT - @m39_lib.M39	91A5
I2C_ALS_SCL	I2C_ALS_SCL - @m39_lib.M39	59B1 59C8
	SMB_A_S3_CLK - @m39_lib.M39	58B5 59B2 59D1
I2C_ALS_SDA	I2C_ALS_SDA - @m39_lib.M39	59B1 59C8
	SMB_A_S3_DATA - @m39_lib.M39	58B5 59B2 59D1
IDE_CSEL_PD	IDE_CSEL_PD - @m39_lib.M39	38C3
IDE_DASP_L	IDE_DASP_L - @m39_lib.M39	38C3
IDE_DASP_L_DS	IDE_DASP_L_DS - @m39_lib.M39	38B3
IDE_IOCS16_PU	IDE_IOCS16_PU - @m39_lib.M39	38C1
IDE_IRQ14	IDE_IRQ14 - @m39_lib.M39	21B6 38C4
IDE_PDA<0>	IDE_PDA<0> - @m39_lib.M39	21B5 38C3
IDE_PDA<1>	IDE_PDA<1> - @m39_lib.M39	21B5 38C3
IDE_PDA<2>	IDE_PDA<2> - @m39_lib.M39	21B5 38C1
IDE_PDCS1_L	IDE_PDCS1_L - @m39_lib.M39	21B5 38C3
IDE_PDCS3_L	IDE_PDCS3_L - @m39_lib.M39	21B5 38C1
IDE_PDD<0>	IDE_PDD<0> - @m39_lib.M39	21C5 38C3
IDE_PDD<1>	IDE_PDD<1> - @m39_lib.M39	21B5 38C3
IDE_PDD<2>	IDE_PDD<2> - @m39_lib.M39	21B5 38D3
IDE_PDD<3>	IDE_PDD<3> - @m39_lib.M39	21B5 38D3
IDE_PDD<4>	IDE_PDD<4> - @m39_lib.M39	21B5 38D3
IDE_PDD<5>	IDE_PDD<5> - @m39_lib.M39	21B5 38D3
IDE_PDD<6>	IDE_PDD<6> - @m39_lib.M39	21B5 38D3
IDE_PDD<7>	IDE_PDD<7> - @m39_lib.M39	21B5 38D3
IDE_PDD<8>	IDE_PDD<8> - @m39_lib.M39	21B5 38D1
IDE_PDD<9>	IDE_PDD<9> - @m39_lib.M39	5C8 21B5 38D1
IDE_PDD<10>	IDE_PDD<10> - @m39_lib.M39	21B5 38D1
IDE_PDD<11>	IDE_PDD<11> - @m39_lib.M39	21B5 38D1
IDE_PDD<12>	IDE_PDD<12> - @m39_lib.M39	21B5 38D1
IDE_PDD<13>	IDE_PDD<13> - @m39_lib.M39	21B5 38D1
IDE_PDD<14>	IDE_PDD<14> - @m39_lib.M39	21B5 38D1
IDE_PDD<15>	IDE_PDD<15> - @m39_lib.M39	21B5 38C1
IDE_PDDACK_L	IDE_PDDACK_L - @m39_lib.M39	21B6 38C1
IDE_PDDREQ	IDE_PDDREQ - @m39_lib.M39	21B6 38C4
IDE_PDIORDY	IDE_PDIORDY - @m39_lib.M39	5C8 21B6 38C4
IDE_PDIOR_L	IDE_PDIOR_L - @m39_lib.M39	5C8 21B6 38C1
IDE_PDIOW_L	IDE_PDIOW_L - @m39_lib.M39	21B6 38C3
IDE_RESET_L	IDE_RESET_L - @m39_lib.M39	23C3 38D3 38D5
IMVP6_BOOT1	IMVP6_BOOT1 - @m39_lib.M39	75A8 75C5
IMVP6_BOOT2	IMVP6_BOOT2 - @m39_lib.M39	75A6 75C5
IMVP6_COMP	IMVP6_COMP - @m39_lib.M39	75A4 75B6
IMVP6_COMP_RC	IMVP6_COMP_RC - @m39_lib.M39	75B7
IMVP6_DFB	IMVP6_DFB - @m39_lib.M39	75A4 75B5
IMVP6_DROOP	IMVP6_DROOP - @m39_lib.M39	75A4 75B4 76D5
IMVP6_DROOP_R	IMVP6_DROOP_R - @m39_lib.M39	76D4
IMVP6_FB	IMVP6_FB - @m39_lib.M39	75A4 75B6
IMVP6_FB2	IMVP6_FB2 - @m39_lib.M39	75A4 75B6

IMVP6_FET_RC1	IMVP6_FET_RC1 - @m39_lib.M39	75A8 75C2
IMVP6_FET_RC2	IMVP6_FET_RC2 - @m39_lib.M39	75A6 75B2
IMVP6_ISEN1	IMVP6_ISEN1 - @m39_lib.M39	75A8 75C5
IMVP6_ISEN2	IMVP6_ISEN2 - @m39_lib.M39	75A6 75C5
IMVP6_LGATE1	IMVP6_LGATE1 - @m39_lib.M39	75A8 75C5
IMVP6_LGATE2	IMVP6_LGATE2 - @m39_lib.M39	75A6 75C5
IMVP6_NTC	IMVP6_NTC - @m39_lib.M39	75C7
IMVP6_NTC_R	IMVP6_NTC_R - @m39_lib.M39	75C7
IMVP6_OCSET	IMVP6_OCSET - @m39_lib.M39	75A4 75B5
IMVP6_PHASE1	IMVP6_PHASE1 - @m39_lib.M39	75A8 75C5
IMVP6_PHASE2	IMVP6_PHASE2 - @m39_lib.M39	75A6 75C5
IMVP6_RBIAS	IMVP6_RBIAS - @m39_lib.M39	75A4 75B6
IMVP6_RTN	IMVP6_RTN - @m39_lib.M39	75A4 75B5
IMVP6_SOFT	IMVP6_SOFT - @m39_lib.M39	75A4 75C6
IMVP6_UGATE1	IMVP6_UGATE1 - @m39_lib.M39	75A8 75C5
IMVP6_UGATE2	IMVP6_UGATE2 - @m39_lib.M39	75A6 75C5
IMVP6_VDIFF	IMVP6_VDIFF - @m39_lib.M39	75A4 75B6
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @m39_lib.M39	75B7
IMVP6_VO	IMVP6_VO - @m39_lib.M39	75A4 75B4 76D5
IMVP6_VO_R	IMVP6_VO_R - @m39_lib.M39	75B4
IMVP6_VO_R_OA	IMVP6_VO_R_OA - @m39_lib.M39	76D4
IMVP6_VR_TT	IMVP6_VR_TT - @m39_lib.M39	75C7
IMVP6_VSEN	IMVP6_VSEN - @m39_lib.M39	75A4 75B5
IMVP6_VSUM	IMVP6_VSUM - @m39_lib.M39	75A4 75C5
IMVP6_VSUM_R1	IMVP6_VSUM_R1 - @m39_lib.M39	75A8 75C2
IMVP6_VSUM_R2	IMVP6_VSUM_R2 - @m39_lib.M39	75A6 75B2
IMVP6_VW	IMVP6_VW - @m39_lib.M39	75A4 75B6
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @m39_lib.M39	75C6
IMVP_PGD_IN	IMVP_PGD_IN - @m39_lib.M39	75C6 77C7
IMVP_VID<0>	IMVP_VID<0> - @m39_lib.M39	75C6
IMVP_VID<1>	IMVP_VID<1> - @m39_lib.M39	75C7
IMVP_VID<2>	IMVP_VID<2> - @m39_lib.M39	75C7
IMVP_VID<3>	IMVP_VID<3> - @m39_lib.M39	75C7
IMVP_VID<4>	IMVP_VID<4> - @m39_lib.M39	75C7
IMVP_VID<5>	IMVP_VID<5> - @m39_lib.M39	75C7
IMVP_VID<6>	IMVP_VID<6> - @m39_lib.M39	75C7
IMVP_VR_ON	IMVP_VR_ON - @m39_lib.M39	58D7 75C6
INT_PIRQA_L	INT_PIRQA_L - @m39_lib.M39	22A7 26D2
INT_PIRQB_L	INT_PIRQB_L - @m39_lib.M39	22A7 26D2
INT_PIRQC_L	INT_PIRQC_L - @m39_lib.M39	22A7 26D2
INT_PIRQD_L	INT_PIRQD_L - @m39_lib.M39	22A7 26D2 44B5
INT_SERIRQ	INT_SERIRQ - @m39_lib.M39	23C8 58C7 60C3 67C6
ISENSE_CAL_EN	ISENSE_CAL_EN - @m39_lib.M39	58B7 76A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @m39_lib.M39	76B7
ISENSE_CAL_EN_LS12V	ISENSE_CAL_EN_LS12V - @m39_lib.M39	76B6
ISENSE_CAL_EN_L_R	ISENSE_CAL_EN_L_R - @m39_lib.M39	76A7
ITPRESET_L	ITPRESET_L - @m39_lib.M39	11B3
ITP_TDO	ITP_TDO - @m39_lib.M39	11B3
ITS_ALIVE	ITS_ALIVE - @m39_lib.M39	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @m39_lib.M39	6A8
ITS_RUNNING	ITS_RUNNING - @m39_lib.M39	6A6
JDREF	JDREF - @m39_lib.M39	68C4
KBC_MDE	KBC_MDE - @m39_lib.M39	58C2
LCD_PWM	LCD_PWM - @m39_lib.M39	6D8 94B1
LCD_PWM_R	LCD_PWM_R - @m39_lib.M39	94B2
LCD_PWREN_L	LCD_PWREN_L - @m39_lib.M39	94C8
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @m39_lib.M39	94C7
LED4300_1	LED4300_1 - @m39_lib.M39	43D2
LED4301_1	LED4301_1 - @m39_lib.M39	43D1
LED4302_1	LED4302_1 - @m39_lib.M39	43D1
LED4303_1	LED4303_1 - @m39_lib.M39	43D1
LED_PP1V05_S0_N	LED_PP1V05_S0_N - @m39_lib.M39	81A4
LED_PP1V05_S0_P	LED_PP1V05_S0_P - @m39_lib.M39	81A4
LED_PP1V5_S0_N	LED_PP1V5_S0_N - @m39_lib.M39	80A3
LED_PP1V5_S0_P	LED_PP1V5_S0_P - @m39_lib.M39	80A4
LED_PP1V8_S3_N	LED_PP1V8_S3_N - @m39_lib.M39	79A4
LED_PP1V8_S3_P	LED_PP1V8_S3_P - @m39_lib.M39	79A4
LPC_AD<0>	LPC_AD<0> - @m39_lib.M39	21D4 58D7 60C6 67C6
LPC_AD<1>	LPC_AD<1> - @m39_lib.M39	21D4 58D7 60C6 67C6
LPC_AD<2>	LPC_AD<2> - @m39_lib.M39	21D4 58C7 60C3 67C6
LPC_AD<3>	LPC_AD<3> - @m39_lib.M39	21D4 58C7 60C3 67C6
LPC_FRAME_L	LPC_FRAME_L - @m39_lib.M39	21C5 58C7 60C6 67C6
LVDS_A_CLK_N	LVDS_A_CLK_N - @m39_lib.M39	13D5 19D2
	TP_LVDS_A_CLK_N - @m39_lib.M39	19D1
LVDS_A_CLK_P	LVDS_A_CLK_P - @m39_lib.M39	13C5 19D2
	TP_LVDS_A_CLK_P - @m39_lib.M39	19D1
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @m39_lib.M39	13C5 19D2
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @m39_lib.M39	13C5 19D2
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @m39_lib.M39	13C5 19D2
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @m39_lib.M39	13C5 19D2
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @m39_lib.M39	13C5 19D2
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @m39_lib.M39	13C5 19D2
LVDS_BKLTCTL	LVDS_BKLTCTL - @m39_lib.M39	13D5 19C2
	TP_LVDS_BKLTCTL - @m39_lib.M39	19C1
LVDS_BKLTEN	LVDS_BKLTEN - @m39_lib.M39	13D5 19C2
	TP_LVDS_BKLTEN - @m39_lib.M39	19C1
LVDS_B_CLK_N	LVDS_B_CLK_N - @m39_lib.M39	13C5 19D2
	TP_LVDS_B_CLK_N - @m39_lib.M39	19D1
LVDS_B_CLK_P	LVDS_B_CLK_P - @m39_lib.M39	13C5 19D2
	TP_LVDS_B_CLK_P - @m39_lib.M39	19D1
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @m39_lib.M39	13C5 19D2
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @m39_lib.M39	13C5 19D2
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @m39_lib.M39	13C5 19D2
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @m39_lib.M39	13C5 19D2
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @m39_lib.M39	13C5 19D2
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @m39_lib.M39	13C5 19D2
LVDS_CLKCTLA	LVDS_CLKCTLA - @m39_lib.M39	13D5 19C2
	TP_LVDS_CLKCTLA - @m39_lib.M39	19C1
LVDS_CLKCTLB	LVDS_CLKCTLB - @m39_lib.M39	13D5 19C2
	TP_LVDS_CLKCTLB - @m39_lib.M39	19C1
LVDS_DDC_CLK	LVDS_DDC_CLK - @m39_lib.M39	13D5 19C2
	TP_LVDS_DDC_CLK - @m39_lib.M39	19C1
LVDS_DDC_DATA	LVDS_DDC_DATA - @m39_lib.M39	13D5 19C2
	TP_LVDS_DDC_DATA - @m39_lib.M39	19C1
LVDS_IBG	LVDS_IBG - @m39_lib.M39	13D5 19C2
	TP_LVDS_IBG - @m39_lib.M39	19C1
LVDS_L_CLK_N	LVDS_L_CLK_N - @m39_lib.M39	93A3 93D2 94A6
LVDS_L_CLK_P	LVDS_L_CLK_P - @m39_lib.M39	93A3 93D2 94A7
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @m39_lib.M39	93A3 93C2 94A6
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @m39_lib.M39	93A3 93C2 94A7
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @m39_lib.M39	93A3 93C2 94A6
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @m39_lib.M39	93A3 94A6
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @m39_lib.M39	93A3 93D2 94A7
LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @m39_lib.M39	93A3 93C2 94A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @m39_lib.M39	93A3 93C2 94A7
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @m39_lib.M39	93A3 94A7
LVDS_U_CLK_N	LVDS_U_CLK_N - @m39_lib.M39	93B3 94B6
LVDS_U_CLK_P	LVDS_U_CLK_P - @m39_lib.M39	93B3 94A7
LVDS_U_DATA_N<0>	LVDS_U_DATA_N<0> - @m39_lib.M39	93B3 94B7
LVDS_U_DATA_N<1>	LVDS_U_DATA_N<1> - @m39_lib.M39	93B3 94B7
LVDS_U_DATA_N<2>	LVDS_U_DATA_N<2> - @m39_lib.M39	93B3 94B7
LVDS_U_DATA_N<3>	LVDS_U_DATA_N<3> - @m39_lib.M39	93B3 94A6
LVDS_U_DATA_P<0>	LVDS_U_DATA_P<0> - @m39_lib.M39	93B3 94B6
LVDS_U_DATA_P<1>	LVDS_U_DATA_P<1> - @m39_lib.M39	93B3 94B6
LVDS_U_DATA_P<2>	LVDS_U_DATA_P<2> - @m39_lib.M39	93B3 94B6
LVDS_U_DATA_P<3>	LVDS_U_DATA_P<3> - @m39_lib.M39	93B3 94A7
LVDS_VDDEN	LVDS_VDDEN - @m39_lib.M39	13D5 19C2
	TP_LVDS_VDDEN - @m39_lib.M39	19C1
LVDS_VREFH	LVDS_VREFH - @m39_lib.M39	13D5 19C2
	TP_LVDS_VREFH - @m39_lib.M39	19C1
LVDS_VREFL	LVDS_VREFL - @m39_lib.M39	13D5 19C2
	TP_LVDS_VREFL - @m39_lib.M39	19C1
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MEM_A_A<13..0>	MEM_A_A<13..0> - @m39_lib.M39	30C6
MEM_A_A<1>	MEM_A_A<1> - @m39_lib.M39	15C5 28B6
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MEM_B_BS<2..0>	MEM_B_BS<2..0> - @m39_lib.M39	30A6
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MEM_B_BS<2>	MEM_B_BS<2> - @m39_lib.M39	15D2 29C6
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MEM_B_DQ<62>	MEM_B_DQ<62> - @m39_lib.M39	5A7 15A4 29A3
MEM_B_DQ<63>	MEM_B_DQ<63> - @m39_lib.M39	15A4 29A3
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @m39_lib.M39	5A7 15C2 29D6
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @m39_lib.M39	5A7 15C2 29D6
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @m39_lib.M39	5A7 15C2 29C6
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @m39_lib.M39	5A7 15C2 29C3
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @m39_lib.M39	5A7 15C2 29B6
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @m39_lib.M39	5A7 15C2 29B3
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @m39_lib.M39	5A7 15C2 29A6
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @m39_lib.M39	5A7 15C2 29A3
MEM_B_DQS_P<0>	MEM_B_DQS_P<0> - @m39_lib.M39	5A7 15C2 29D6
MEM_B_DQS_P<1>	MEM_B_DQS_P<1> - @m39_lib.M39	5A7 15C2 29D6
MEM_B_DQS_P<2>	MEM_B_DQS_P<2> - @m39_lib.M39	5A7 15C2 29C6
MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @m39_lib.M39	5A7 15C2 29C3
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @m39_lib.M39	5A7 15C2 29B6
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @m39_lib.M39	5A7 15C2 29A3
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @m39_lib.M39	5A7 15C2 29A6
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @m39_lib.M39	5A7 15C2 29A3
MEM_B_RAS_L	MEM_B_RAS_L - @m39_lib.M39	15B2 29B3 30A6
MEM_B_SPD_SA1	MEM_B_SPD_SA1 - @m39_lib.M39	29A4
MEM_B_WE_L	MEM_B_WE_L - @m39_lib.M39	15B2 29B6 30A6
MEM_CKE<0>	MEM_CKE<0> - @m39_lib.M39	14C4 28C6
MEM_CKE<3..0>	MEM_CKE<3..0> - @m39_lib.M39	30D6
MEM_CKE<1>	MEM_CKE<1> - @m39_lib.M39	14C4 28C3
MEM_CKE<2>	MEM_CKE<2> - @m39_lib.M39	14C4 29C6
MEM_CKE<3>	MEM_CKE<3> - @m39_lib.M39	14C4 29C3
MEM_CLK_N<0>	MEM_CLK_N<0> - @m39_lib.M39	14D4 28D3
MEM_CLK_N<1>	MEM_CLK_N<1> - @m39_lib.M39	14D4 28A3
MEM_CLK_N<2>	MEM_CLK_N<2> - @m39_lib.M39	14D4 29A3
MEM_CLK_N<3>	MEM_CLK_N<3> - @m39_lib.M39	14D4 29D3
MEM_CLK_P<0>	MEM_CLK_P<0> - @m39_lib.M39	14D4 28D3
MEM_CLK_P<1>	MEM_CLK_P<1> - @m39_lib.M39	14D4 28A3
MEM_CLK_P<2>	MEM_CLK_P<2> - @m39_lib.M39	14D4 29A3
MEM_CLK_P<3>	MEM_CLK_P<3> - @m39_lib.M39	14D4 29D3
MEM_CS_L<0>	MEM_CS_L<0> - @m39_lib.M39	14C4 28B3
MEM_CS_L<3..0>	MEM_CS_L<3..0> - @m39_lib.M39	30D6
MEM_CS_L<1>	MEM_CS_L<1> - @m39_lib.M39	14C4 28B6
MEM_CS_L<2>	MEM_CS_L<2> - @m39_lib.M39	14C4 29B3
MEM_CS_L<3>	MEM_CS_L<3> - @m39_lib.M39	14C4 29B6
MEM_ODT<0>	MEM_ODT<0> - @m39_lib.M39	14C4 28B3
MEM_ODT<3..0>	MEM_ODT<3..0> - @m39_lib.M39	30D6
MEM_ODT<1>	MEM_ODT<1> - @m39_lib.M39	14C4 28B6
MEM_ODT<2>	MEM_ODT<2> - @m39_lib.M39	14C4 29B3
MEM_ODT<3>	MEM_ODT<3> - @m39_lib.M39	14C4 29B6
MEM_RCOMP	MEM_RCOMP - @m39_lib.M39	14C4
MEM_RCOMP_L	MEM_RCOMP_L - @m39_lib.M39	14C4
MEM_VREF	MEM_VREF - @m39_lib.M39	5C4 28C7 28D6 29D6
MEM_VREF_NB_0	MEM_VREF_NB_0 - @m39_lib.M39	5B7 14C4 19B6
MEM_VREF_NB_1	MEM_VREF_NB_1 - @m39_lib.M39	5B7 14C4 19B7
NB_BSEL<0>	NB_BSEL<0> - @m39_lib.M39	14C6 34B8
NB_BSEL<1>	NB_BSEL<1> - @m39_lib.M39	14C6 34B8
NB_BSEL<2>	NB_BSEL<2> - @m39_lib.M39	14C6 34A8
NB_CFG<3>	NB_CFG<3> - @m39_lib.M39	14C6
NB_CFG<4>	NB_CFG<4> - @m39_lib.M39	14C6
NB_CFG<5>	NB_CFG<5> - @m39_lib.M39	14C6 20C7
NB_CFG<6>	NB_CFG<6> - @m39_lib.M39	14C6
NB_CFG<7>	NB_CFG<7> - @m39_lib.M39	14C6 20C7
NB_CFG<8>	NB_CFG<8> - @m39_lib.M39	14C6
NB_CFG<9>	NB_CFG<9> - @m39_lib.M39	14C6 20B7
NB_CFG<10>	NB_CFG<10> - @m39_lib.M39	14C6
NB_CFG<11>	NB_CFG<11> - @m39_lib.M39	14C6
NB_CFG<12>	NB_CFG<12> - @m39_lib.M39	14C6
NB_CFG<13>	NB_CFG<13> - @m39_lib.M39	14C6
NB_CFG<14>	NB_CFG<14> - @m39_lib.M39	14C6
NB_CFG<15>	NB_CFG<15> - @m39_lib.M39	14C6
NB_CFG<16>	NB_CFG<16> - @m39_lib.M39	14C6 20C5
NB_CFG<17>	NB_CFG<17> - @m39_lib.M39	14C6
NB_CFG<18>	NB_CFG<18> - @m39_lib.M39	14C6 20B5
NB_CFG<19>	NB_CFG<19> - @m39_lib.M39	14C6 20B5
NB_CFG<20>	NB_CFG<20> - @m39_lib.M39	14B6 20A5
NB_CLK100M_GCLKIN_N	NB_CLK100M_GCLKIN_N - @m39_lib.M39	5C7 14C4 34B4 34C2
NB_CLK100M_GCLKIN_P	NB_CLK100M_GCLKIN_P - @m39_lib.M39	5C7 14C4 34B4 34C2
NB_FSB_VREF	NB_FSB_VREF - @m39_lib.M39	5D4 12C4
NB_FSB_XRCOMP	NB_FSB_XRCOMP - @m39_lib.M39	12A6
NB_FSB_XSCOMP	NB_FSB_XSCOMP - @m39_lib.M39	12A6
NB_FSB_XSWING	NB_FSB_XSWING - @m39_lib.M39	12A6
NB_FSB_YRCOMP	NB_FSB_YRCOMP - @m39_lib.M39	12A6
NB_FSB_YSCOMP	NB_FSB_YSCOMP - @m39_lib.M39	12A6
NB_FSB_YSWING	NB_FSB_YSWING - @m39_lib.M39	12A6
NB_RST_IN_L	NB_RST_IN_L - @m39_lib.M39	6B7 14B7
NB_RST_IN_L_R	NB_RST_IN_L_R - @m39_lib.M39	5C7 14B6
NB_SB_SYNC_L	NB_SB_SYNC_L - @m39_lib.M39	14B6 22A6
NB_TV_DCONSEL0	NB_TV_DCONSEL0 - @m39_lib.M39	14D6
NB_TV_DCONSEL1	NB_TV_DCONSEL1 - @m39_lib.M39	14C6
NB_VCCSM_LF1	NB_VCCSM_LF1 - @m39_lib.M39	16B4
NB_VCCSM_LF2	NB_VCCSM_LF2 - @m39_lib.M39	16B4
NB_VCCSM_LF4	NB_VCCSM_LF4 - @m39_lib.M39	16B8
NB_VCCSM_LF5	NB_VCCSM_LF5 - @m39_lib.M39	16B8
NB_VTTLF_CAP1	NB_VTTLF_CAP1 - @m39_lib.M39	17A4
NB_VTTLF_CAP2	NB_VTTLF_CAP2 - @m39_lib.M39	17A4
NB_VTTLF_CAP3	NB_VTTLF_CAP3 - @m39_lib.M39	17B4
NC_AUD_VREF_PORT_A	NC_AUD_VREF_PORT_A - @m39_lib.M39	68C1
NC_AUD_VREF_PORT_C	NC_AUD_VREF_PORT_C - @m39_lib.M39	68C1
NC_AUD_VREF_PORT_D	NC_AUD_VREF_PORT_D - @m39_lib.M39	68C1
NC_FW_NU1	NC_FW_NU1 - @m39_lib.M39	44B3
NC_FW_NU2	NC_FW_NU2 - @m39_lib.M39	44B3
NC_JE350_13	NC_JE350_13 - @m39_lib.M39	47B1
NC_SMC_P20	NC_SMC_P20 - @m39_lib.M39	59D5
	SMC_P20 - @m39_lib.M39	58D7 59D6
NC_SMC_P21	NC_SMC_P21 - @m39_lib.M39	59D5
	SMC_P21 - @m39_lib.M39	58D7 59D6
NC_SMC_P22	NC_SMC_P22 - @m39_lib.M39	59D5
	SMC_P22 - @m39_lib.M39	58D7 59D6
NC_SMC_P23	NC_SMC_P23 - @m39_lib.M39	59D5
	SMC_P23 - @m39_lib.M39	58D7 59D6
NC_SMC_P26	NC_SMC_P26 - @m39_lib.M39	59D5
	SMC_P26 - @m39_lib.M39	58D7 59D6
NC_SMC_P27	NC_SMC_P27 - @m39_lib.M39	59D5
	SMC_P27 - @m39_lib.M39	58D7 59D6
ODD_PWR_EN_L	ODD_PWR_EN_L - @m39_lib.M39	22A6 26C3
	SB_GPIO5 - @m39_lib.M39	26C2
P0V48_SMC_LSREF	P0V48_SMC_LSREF - @m39_lib.M39	59A6 59A8 59B7
PANEL_ID	PANEL_ID - @m39_lib.M39	6D6 94C2
PATA_PWR_EN_L	PATA_PWR_EN_L - @m39_lib.M39	23B3 23C3
PCIE_A_D2R_C_N	PCIE_A_D2R_C_N - @m39_lib.M39	41D5
PCIE_A_D2R_C_P	PCIE_A_D2R_C_P - @m39_lib.M39	41D5
PCIE_A_D2R_N	PCIE_A_D2R_N - @m39_lib.M39	5B8 22D4 41D4
PCIE_A_D2R_P	PCIE_A_D2R_P - @m39_lib.M39	5C8 22D4 41D4
PCIE_A_R2D_C_N	PCIE_A_R2D_C_N - @m39_lib.M39	22D4 41C3
PCIE_A_R2D_C_P	PCIE_A_R2D_C_P - @m39_lib.M39	22D4 41C3
PCIE_A_R2D_N	PCIE_A_R2D_N - @m39_lib.M39	41C5
PCIE_A_R2D_P	PCIE_A_R2D_P - @m39_lib.M39	41C5
PCIE_B_D2R_N	PCIE_B_D2R_N - @m39_lib.M39	5B8 22D4 53C7
PCIE_B_D2R_P	PCIE_B_D2R_P - @m39_lib.M39	5B8 22D4 53C7
PCIE_B_R2D_C_N	PCIE_B_R2D_C_N - @m39_lib.M39	22D4 53B7
PCIE_B_R2D_C_P	PCIE_B_R2D_C_P - @m39_lib.M39	22D4 53B7
PCIE_B_R2D_N	PCIE_B_R2D_N - @m39_lib.M39	53B6
PCIE_B_R2D_P	PCIE_B_R2D_P - @m39_lib.M39	53B6
PCIE_C_D2R_N	PCIE_C_D2R_N - @m39_lib.M39	22D4 54D8
	TP_PCIE_C_D2R_N - @m39_lib.M39	54D6
PCIE_C_D2R_P	PCIE_C_D2R_P - @m39_lib.M39	22D4 54D8
	TP_PCIE_C_D2R_P - @m39_lib.M39	54D6
PCIE_C_R2D_C_N	PCIE_C_R2D_C_N - @m39_lib.M39	22D4 54D8
	TP_PCIE_C_R2D_C_N - @m39_lib.M39	54D6
PCIE_C_R2D_C_P	PCIE_C_R2D_C_P - @m39_lib.M39	22D4 54D8
	TP_PCIE_C_R2D_C_P - @m39_lib.M39	54D6
PCIE_D_D2R_N	PCIE_D_D2R_N - @m39_lib.M39	22D4 54C8
	TP_PCIE_D_D2R_N - @m39_lib.M39	54C6
PCIE_D_D2R_P	PCIE_D_D2R_P - @m39_lib.M39	22D4 54C8
	TP_PCIE_D_D2R_P - @m39_lib.M39	54C6
PCIE_D_R2D_C_N	PCIE_D_R2D_C_N - @m39_lib.M39	22D4 54D8
	TP_PCIE_D_R2D_C_N - @m39_lib.M39	54D6
PCIE_D_R2D_C_P	PCIE_D_R2D_C_P - @m39_lib.M39	22D4 54D8
	TP_PCIE_D_R2D_C_P - @m39_lib.M39	54D6
PCIE_E_D2R_N	PCIE_E_D2R_N - @m39_lib.M39	22C4 54C8
	TP_PCIE_E_D2R_N - @m39_lib.M39	54C6
PCIE_E_D2R_P	PCIE_E_D2R_P - @m39_lib.M39	22C4 54C8
	TP_PCIE_E_D2R_P - @m39_lib.M39	54C6
PCIE_E_R2D_C_N	PCIE_E_R2D_C_N - @m39_lib.M39	22C4 54C8
	TP_PCIE_E_R2D_C_N - @m39_lib.M39	54C6
PCIE_E_R2D_C_P	PCIE_E_R2D_C_P - @m39_lib.M39	22C4 54C8
	TP_PCIE_E_R2D_C_P - @m39_lib.M39	54C6
PCIE_F_D2R_N	PCIE_F_D2R_N - @m39_lib.M39	22C4 54B8
	TP_PCIE_F_D2R_N - @m39_lib.M39	54B6
PCIE_F_D2R_P	PCIE_F_D2R_P - @m39_lib.M39	22C4 54B8
	TP_PCIE_F_D2R_P - @m39_lib.M39	54B6
PCIE_F_R2D_C_N	PCIE_F_R2D_C_N - @m39_lib.M39	22C4 54C8
	TP_PCIE_F_R2D_C_N - @m39_lib.M39	54C6
PCIE_F_R2D_C_P	PCIE_F_R2D_C_P - @m39_lib.M39	22C4 54B8
	TP_PCIE_F_R2D_C_P - @m39_lib.M39	54B6
PCIE_WAKE_L	PCIE_WAKE_L - @m39_lib.M39	23C8 41C4 53C7
PCI_AD<0>	PCI_AD<0> - @m39_lib.M39	22B7 44D5
PCI_AD<1>	PCI_AD<1> - @m39_lib.M39	22B7 44D5
PCI_AD<2>	PCI_AD<2> - @m39_lib.M39	22B7 44D5

PCI_AD<3>	PCI_AD<3> - @m39_lib.M39	22B7 44D5
PCI_AD<4>	PCI_AD<4> - @m39_lib.M39	22B7 44D5
PCI_AD<5>	PCI_AD<5> - @m39_lib.M39	22B7 44C5
PCI_AD<6>	PCI_AD<6> - @m39_lib.M39	22B7 44C5
PCI_AD<7>	PCI_AD<7> - @m39_lib.M39	22B7 44C5
PCI_AD<8>	PCI_AD<8> - @m39_lib.M39	22B7 44C5
PCI_AD<9>	PCI_AD<9> - @m39_lib.M39	22B7 44C5
PCI_AD<10>	PCI_AD<10> - @m39_lib.M39	22B7 44C5
PCI_AD<11>	PCI_AD<11> - @m39_lib.M39	22B7 44C5
PCI_AD<12>	PCI_AD<12> - @m39_lib.M39	22B7 44C5
PCI_AD<13>	PCI_AD<13> - @m39_lib.M39	22B7 44C5
PCI_AD<14>	PCI_AD<14> - @m39_lib.M39	22B7 44C5
PCI_AD<15>	PCI_AD<15> - @m39_lib.M39	22B7 44C5
PCI_AD<16>	PCI_AD<16> - @m39_lib.M39	22B7 44C5
PCI_AD<17>	PCI_AD<17> - @m39_lib.M39	22B7 44C5
PCI_AD<18>	PCI_AD<18> - @m39_lib.M39	22B7 44C5
PCI_AD<19>	PCI_AD<19> - @m39_lib.M39	22A7 44C6
PCI_AD<20>	PCI_AD<20> - @m39_lib.M39	22A7 44C5
PCI_AD<21>	PCI_AD<21> - @m39_lib.M39	22A7 44C5
PCI_AD<22>	PCI_AD<22> - @m39_lib.M39	22A7 44C5
PCI_AD<23>	PCI_AD<23> - @m39_lib.M39	22A7 44C5
PCI_AD<24>	PCI_AD<24> - @m39_lib.M39	22A7 44C5
PCI_AD<25>	PCI_AD<25> - @m39_lib.M39	22A7 44C5
PCI_AD<26>	PCI_AD<26> - @m39_lib.M39	22A7 44C5
PCI_AD<27>	PCI_AD<27> - @m39_lib.M39	22A7 44C5
PCI_AD<28>	PCI_AD<28> - @m39_lib.M39	22A7 44C5
PCI_AD<29>	PCI_AD<29> - @m39_lib.M39	22A7 44C5
PCI_AD<30>	PCI_AD<30> - @m39_lib.M39	22A7 44C5
PCI_AD<31>	PCI_AD<31> - @m39_lib.M39	22A7 44B5
PCI_CLK_FW	PCI_CLK_FW - @m39_lib.M39	34C4 44B5
PCI_CLK_PORT80	PCI_CLK_PORT80 - @m39_lib.M39	34B4 60C3
PCI_CLK_SB	PCI_CLK_SB - @m39_lib.M39	5C8 22A6 34B4
PCI_CLK_SMC	PCI_CLK_SMC - @m39_lib.M39	34C4 58C7
PCI_CLK_TPM	PCI_CLK_TPM - @m39_lib.M39	34C4 67C6
PCI_C_BE_L<0>	PCI_C_BE_L<0> - @m39_lib.M39	22B6 44B5
PCI_C_BE_L<1>	PCI_C_BE_L<1> - @m39_lib.M39	22B6 44B5
PCI_C_BE_L<2>	PCI_C_BE_L<2> - @m39_lib.M39	22B6 44B5
PCI_C_BE_L<3>	PCI_C_BE_L<3> - @m39_lib.M39	22B6 44B5
PCI_DEVSEL_L	PCI_DEVSEL_L - @m39_lib.M39	22A6 26D2 44B5
PCI_FRAME_L	PCI_FRAME_L - @m39_lib.M39	22A7 26D2 44B5
PCI_GNT3_L	PCI_GNT3_L - @m39_lib.M39	22B4 44B5
PCI_IDSEL	PCI_IDSEL - @m39_lib.M39	44B5
PCI_IRDY_L	PCI_IRDY_L - @m39_lib.M39	22A6 26D2 44B5
PCI_LOCK_L	PCI_LOCK_L - @m39_lib.M39	22A6 26D2
PCI_PAR	PCI_PAR - @m39_lib.M39	22A6 44B5
PCI_PERR_L	PCI_PERR_L - @m39_lib.M39	22A6 26D2 44B5
PCI_PME_FW_L	PCI_PME_FW_L - @m39_lib.M39	22B5 44B5
PCI_REQ0_L	PCI_REQ0_L - @m39_lib.M39	22B6 26D2
PCI_REQ1_L	PCI_REQ1_L - @m39_lib.M39	22B6 26D2
PCI_REQ2_L	PCI_REQ2_L - @m39_lib.M39	22B6 26D2
PCI_REQ3_L	PCI_REQ3_L - @m39_lib.M39	22B4 26D2 44B5
PCI_RST_FW_L	PCI_RST_FW_L - @m39_lib.M39	44A7 44B5
PCI_RST_L	PCI_RST_L - @m39_lib.M39	22A6 44A8
PCI_SERR_L	PCI_SERR_L - @m39_lib.M39	22A6 26D2 44B5
PCI_STOP_L	PCI_STOP_L - @m39_lib.M39	22A6 26D2 44B5
PCI_TRDY_L	PCI_TRDY_L - @m39_lib.M39	22A6 26D2 44B5
PEG_COMP	PEG_COMP - @m39_lib.M39	13D3
PEG_D2R_C_N<0>	PEG_D2R_C_N<0> - @m39_lib.M39	84D3
PEG_D2R_C_N<1>	PEG_D2R_C_N<1> - @m39_lib.M39	84D3
PEG_D2R_C_N<2>	PEG_D2R_C_N<2> - @m39_lib.M39	84D3
PEG_D2R_C_N<3>	PEG_D2R_C_N<3> - @m39_lib.M39	84D3
PEG_D2R_C_N<4>	PEG_D2R_C_N<4> - @m39_lib.M39	84C3
PEG_D2R_C_N<5>	PEG_D2R_C_N<5> - @m39_lib.M39	84C3
PEG_D2R_C_N<6>	PEG_D2R_C_N<6> - @m39_lib.M39	84C3
PEG_D2R_C_N<7>	PEG_D2R_C_N<7> - @m39_lib.M39	84C3
PEG_D2R_C_N<8>	PEG_D2R_C_N<8> - @m39_lib.M39	84C3
PEG_D2R_C_N<9>	PEG_D2R_C_N<9> - @m39_lib.M39	84C3
PEG_D2R_C_N<10>	PEG_D2R_C_N<10> - @m39_lib.M39	84B3
PEG_D2R_C_N<11>	PEG_D2R_C_N<11> - @m39_lib.M39	84B3
PEG_D2R_C_N<12>	PEG_D2R_C_N<12> - @m39_lib.M39	84B3
PEG_D2R_C_N<13>	PEG_D2R_C_N<13> - @m39_lib.M39	84B3
PEG_D2R_C_N<14>	PEG_D2R_C_N<14> - @m39_lib.M39	84B3
PEG_D2R_C_N<15>	PEG_D2R_C_N<15> - @m39_lib.M39	84B3
PEG_D2R_C_P<0>	PEG_D2R_C_P<0> - @m39_lib.M39	84D3
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PEG_RESET_L	PEG_RESET_L - @m39_lib.M39	6B7 84A5
PLT_RST_L	PLT_RST_L - @m39_lib.M39	6C8 22A6
PM_BATLOW_L	PM_BATLOW_L - @m39_lib.M39	23C1 58B7
PM_BMBUSY_L	PM_BMBUSY_L - @m39_lib.M39	14B6 23C5
PM_CLKRUN_L	PM_CLKRUN_L - @m39_lib.M39	5B8 23C8 44B5 58C5 60C6 67C6
PM_DPRSLPVR	PM_DPRSLPVR - @m39_lib.M39	14B7 23C3 75C7
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @m39_lib.M39	14B7 58B7 59C5
	DIMM_OVERTEMP_L - @m39_lib.M39	28C3 29C3 59C6
PM_LAN_ENABLE	PM_LAN_ENABLE - @m39_lib.M39	23C3 58D7
PM_PWRBTN_L	PM_PWRBTN_L - @m39_lib.M39	23C3 58D7
PM_PWROK	PM_PWROK - @m39_lib.M39	77B7
PM_RI_L	PM_RI_L - @m39_lib.M39	23D5
PM_RSMRST_L	PM_RSMRST_L - @m39_lib.M39	23C1 58D7
PM_SB_PWROK	PM_SB_PWROK - @m39_lib.M39	23C3 26D6
PM_SLP_S3	PM_SLP_S3 - @m39_lib.M39	77D7 78B8 80C8 81C8
PM_SLP_S3_L	PM_SLP_S3_L - @m39_lib.M39	6C8 23C3 58C5 77D8 79A7 88A6
	MEMVTT_EN - @m39_lib.M39	31B5 79A6
PM_SLP_S4	PM_SLP_S4 - @m39_lib.M39	77A7 77C7 79C8 83C6
PM_SLP_S4_L	PM_SLP_S4_L - @m39_lib.M39	23C3 58C5 77C8
PM_SLP_S5_L	PM_SLP_S5_L - @m39_lib.M39	23C3 58C5
PM_STPCPU_L	PM_STPCPU_L - @m39_lib.M39	23C8 33C4
PM_STPPCI_L	PM_STPPCI_L - @m39_lib.M39	23C8 33C4
PM_SUS_STAT_L	PM_SUS_STAT_L - @m39_lib.M39	23C5 58C5 60C3 67C6
PM_SYSRST_L	PM_SYSRST_L - @m39_lib.M39	5B8 23C5 26C3 58B7
PM_THRMTRIP_L	PM_THRMTRIP_L - @m39_lib.M39	7C6 14B6 21C2 59C7
PM_THRM_L	PM_THRM_L - @m39_lib.M39	10D3 23C8 58B7
POWER_BUTTON_L	POWER_BUTTON_L - @m39_lib.M39	5D1 59C8
PP0V9_S0_PGOOD	PP0V9_S0_PGOOD - @m39_lib.M39	77B8 79A2
PP1V2_S0_GPU_VDDPLL	PP1V2_S0_GPU_VDDPLL - @m39_lib.M39	91B6
PP1V05_S0_PGOOD	PP1V05_S0_PGOOD - @m39_lib.M39	77C8 81B2
PP1V5_S0_NB_3GPLL_F	PP1V5_S0_NB_3GPLL_F - @m39_lib.M39	19A5
PP1V5_S0_NB_VCC3G	PP1V5_S0_NB_VCC3G - @m39_lib.M39	17D6 19A3
PP1V5_S0_NB_VCCA_3GPLL	PP1V5_S0_NB_VCCA_3GPLL - @m39_lib.M39	17D6 19A3
PP1V5_S0_NB_VCCA_DPLLA	PP1V5_S0_NB_VCCA_DPLLA - @m39_lib.M39	17C6 19C4
	TP_NB_VCCA_DPLLA - @m39_lib.M39	19C5
PP1V5_S0_NB_VCCA_DPLLB	PP1V5_S0_NB_VCCA_DPLLB - @m39_lib.M39	17C6 19C4
	TP_NB_VCCA_DPLLB - @m39_lib.M39	19C5
PP1V5_S0_NB_VCCA_HPLL	PP1V5_S0_NB_VCCA_HPLL - @m39_lib.M39	17C6 19C6
PP1V5_S0_NB_VCCA_MPLL	PP1V5_S0_NB_VCCA_MPLL - @m39_lib.M39	17C6 19C6
PP1V5_S0_NB_VCCD_QTVDAC	PP1V5_S0_NB_VCCD_QTVDAC - @m39_lib.M39	17B6 19A1
	PP1V5_S0_NB_VCCD_TVDAC - @m39_lib.M39	17C6 19B1
PP1V5_S0_PGOOD	PP1V5_S0_PGOOD - @m39_lib.M39	77C8 80B2
PP1V5_S0_SB_R	PP1V5_S0_SB_R - @m39_lib.M39	25A7
PP1V5_S0_SB_VCC1_5_B	PP1V5_S0_SB_VCC1_5_B - @m39_lib.M39	22C1 24D5 25B7
PP1V5_S0_SB_VCCDMIPLL	PP1V5_S0_SB_VCCDMIPLL - @m39_lib.M39	24B5 25A6
PP1V8R2V0_S0_GPU_VDDRH0	PP1V8R2V0_S0_GPU_VDDRH0 - @m39_lib.M39	87A7
PP1V8R2V0_S0_GPU_VDDRH1	PP1V8R2V0_S0_GPU_VDDRH1 - @m39_lib.M39	87B3
PP1V8R3V3_S0_GPU_VDDR4_F	PP1V8R3V3_S0_GPU_VDDR4_F - @m39_lib.M39	91B6
PP1V8R3V3_S0_GPU_VDDR5_F	PP1V8R3V3_S0_GPU_VDDR5_F - @m39_lib.M39	91B6
PP1V8_FB_A0_VDDA0	PP1V8_FB_A0_VDDA0 - @m39_lib.M39	89D7
PP1V8_FB_A0_VDDA1	PP1V8_FB_A0_VDDA1 - @m39_lib.M39	89D7
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PP1V8_FB_B0_VDDA0	PP1V8_FB_B0_VDDA0 - @m39_lib.M39	90D7
PP1V8_FB_B0_VDDA1	PP1V8_FB_B0_VDDA1 - @m39_lib.M39	90D7
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PP1V8_S3_PGOOD	PP1V8_S3_PGOOD - @m39_lib.M39	79B2
PP2V5 S0_PGOOD	PP2V5 S0_PGOOD - @m39_lib.M39	77B8 77C5
PP2V5_ENET_CTAP	PP2V5_ENET_CTAP - @m39_lib.M39	43D7
PP2V5_S0_GPU_A2VDD	PP2V5_S0_GPU_A2VDD - @m39_lib.M39	93B7
PP2V5_S0_GPU_AVDD	PP2V5_S0_GPU_AVDD - @m39_lib.M39	93C7
PP2V5_S0_GPU_LPVDD	PP2V5_S0_GPU_LPVDD - @m39_lib.M39	93B7
PP2V5_S0_GPU_LVDDR	PP2V5_S0_GPU_LVDDR - @m39_lib.M39	93B7
PP2V5_S0_GPU_PVDD_F	PP2V5_S0_GPU_PVDD_F - @m39_lib.M39	91A6
PP2V5_S0_GPU_TPVDD	PP2V5_S0_GPU_TPVDD - @m39_lib.M39	93C7
PP2V5_S0_GPU_TXVDDR	PP2V5_S0_GPU_TXVDDR - @m39_lib.M39	93C7
PP2V5_S0_GPU_VDD1DI	PP2V5_S0_GPU_VDD1DI - @m39_lib.M39	93C8
PP2V5_S0_GPU_VDD2DI	PP2V5_S0_GPU_VDD2DI - @m39_lib.M39	93B8
PP3V3R12V_LCD_CONN	PP3V3R12V_LCD_CONN - @m39_lib.M39	94A6 94A6 94A7 94C5
PP3V3_AUDIO_SPDIF_EMI	PP3V3_AUDIO_SPDIF_EMI - @m39_lib.M39	73B7
PP3V3_AUDIO_SPDIF_JACK	PP3V3_AUDIO_SPDIF_JACK - @m39_lib.M39	73B5
PP3V3_AVCC_SMC	PP3V3_AVCC_SMC - @m39_lib.M39	58D3
PP3V3_AVREF_SMC	PP3V3_AVREF_SMC - @m39_lib.M39	58D2 59A3
PP3V3_FW_ESD	PP3V3_FW_ESD - @m39_lib.M39	46A5 46A6 46B5 46C5 46D5
PP3V3_FW_ESD_F	PP3V3_FW_ESD_F - @m39_lib.M39	46A7
PP3V3_INTERCON	PP3V3_INTERCON - @m39_lib.M39	72C7
PP3V3_LCD_SW	PP3V3_LCD_SW - @m39_lib.M39	94C6
PP3V3_S0_CK410_VDD48	PP3V3_S0_CK410_VDD48 - @m39_lib.M39	33D5
PP3V3_S0_CK410_VDDA	PP3V3_S0_CK410_VDDA - @m39_lib.M39	33C6
PP3V3_S0_CK410_VDD_CPU_SRC	PP3V3_S0_CK410_VDD_CPU_SRC - @m39_lib.M39	33D6
PP3V3_S0_CK410_VDD_PCI	PP3V3_S0_CK410_VDD_PCI - @m39_lib.M39	33D5
PP3V3_S0_CK410_VDD_REF	PP3V3_S0_CK410_VDD_REF - @m39_lib.M39	33C5
PP3V3_S0_IMVP6_3V3	PP3V3_S0_IMVP6_3V3 - @m39_lib.M39	75D6
PP3V3_S5_FW_VDDA	PP3V3_S5_FW_VDDA - @m39_lib.M39	44D5 45C6
PP3V3_S5_SB_RTC	PP3V3_S5_SB_RTC - @m39_lib.M39	5D2 21D6 24B3 25A3 26D7
PP3V3_S0_2V5REG_R	PP3V3_S0_2V5REG_R - @m39_lib.M39	77D5
PP3V3_TPM_3VSB	PP3V3_TPM_3VSB - @m39_lib.M39	59C5 67C4
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @m39_lib.M39	68A2 68D2 74D8
PP5V_BNDI_LE340	PP5V_BNDI_LE340 - @m39_lib.M39	47D3
PP5V_S0_DDC	PP5V_S0_DDC - @m39_lib.M39	97D4
PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @m39_lib.M39	97D5
PP5V_S0_GPUVCORE_VCC	PP5V_S0_GPUVCORE_VCC - @m39_lib.M39	85D7 88D8
PP5V_S0_IMVP6_VDD	PP5V_S0_IMVP6_VDD - @m39_lib.M39	75D6
PP5V_S0_SB_V5REF	PP5V_S0_SB_V5REF - @m39_lib.M39	24D5 25D7
PP5V_S3_BNDI	PP5V_S3_BNDI - @m39_lib.M39	47B2 47D1
PP5V_S5_SB_V5REF_SUS	PP5V_S5_SB_V5REF_SUS - @m39_lib.M39	24D5 25C7
PP5V_USB2	PP5V_USB2 - @m39_lib.M39	47D7
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @m39_lib.M39	47D5
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @m39_lib.M39	47C5
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @m39_lib.M39	47B5
PP12V_AUD_SPKRAMP_PLANE	PP12V_AUD_SPKRAMP_PLANE - @m39_lib.M39	72D5
PP12V_L7502	PP12V_L7502 - @m39_lib.M39	76D7
PP12V_S5_CPU_REG	PP12V_S5_CPU_REG - @m39_lib.M39	75C3 75D4 75D7 76C8 76D6
PPFW_PORT0_VP	PPFW_PORT0_VP - @m39_lib.M39	46D2
PPFW_PORT0_VP_FL	PPFW_PORT0_VP_FL - @m39_lib.M39	46C2
PPFW_PORT1_VP	PPFW_PORT1_VP - @m39_lib.M39	46B2 46D1
PPFW_PORT1_VP_FL	PPFW_PORT1_VP_FL - @m39_lib.M39	46B2
PPFW_PORTS_VP	PPFW_PORTS_VP - @m39_lib.M39	46D3
PPVCORE_S0_GPU_MPVDD	PPVCORE_S0_GPU_MPVDD - @m39_lib.M39	91A6
PPVCORE_S0_GPU_VDDCI	PPVCORE_S0_GPU_VDDCI - @m39_lib.M39	86C7
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @m39_lib.M39	75D6
PPV_3V3_AUDIO_CODEC	PPV_3V3_AUDIO_CODEC - @m39_lib.M39	68D6
Q4201_3	Q4201_3 - @m39_lib.M39	42D6
R7504_1	R7504_1 - @m39_lib.M39	75A8 75C1
R7507_1	R7507_1 - @m39_lib.M39	75A6 75B1
R8599_2	R8599_2 - @m39_lib.M39	85C4
RSMRST_PWRGD	RSMRST_PWRGD - @m39_lib.M39	58D7 76D1
SATA_A_D2R_N	SATA_A_D2R_N - @m39_lib.M39	21B6 38A6
	TP_SATA_A_D2R_N - @m39_lib.M39	38A5
SATA_A_D2R_P	SATA_A_D2R_P - @m39_lib.M39	21B6 38A6
	TP_SATA_A_D2R_P - @m39_lib.M39	38A5
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @m39_lib.M39	21B6 38A6
	TP_SATA_A_R2D_N - @m39_lib.M39	38A5
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @m39_lib.M39	21B6 38A6
	TP_SATA_A_R2D_P - @m39_lib.M39	38A5
SATA_C_D2R_C_N	SATA_C_D2R_C_N - @m39_lib.M39	38B8
SATA_C_D2R_C_P	SATA_C_D2R_C_P - @m39_lib.M39	38B8
SATA_C_D2R_N	SATA_C_D2R_N - @m39_lib.M39	21B6 38B6
SATA_C_D2R_P	SATA_C_D2R_P - @m39_lib.M39	21B6 38B6
SATA_C_DET_L	SATA_C_DET_L - @m39_lib.M39	23D2 38B5
SATA_C_PWR_EN_L	SATA_C_PWR_EN_L - @m39_lib.M39	23A3 23B3
SATA_C_R2D_C_N	SATA_C_R2D_C_N - @m39_lib.M39	21B6 38B6
SATA_C_R2D_C_P	SATA_C_R2D_C_P - @m39_lib.M39	21B6 38B6
SATA_C_R2D_N	SATA_C_R2D_N - @m39_lib.M39	38B8
SATA_C_R2D_P	SATA_C_R2D_P - @m39_lib.M39	38B8
SATA_RBIAS_N	SATA_RBIAS_N - @m39_lib.M39	21B6 38C7
	SATA_RBIAS_P - @m39_lib.M39	21B6 38C7
	SATA_RBIAS - @m39_lib.M39	38C7
	SATA_RBIAS_P - @m39_lib.M39	21B6 38C7
	SATA_RBIAS - @m39_lib.M39	38C7
SB_A20GATE	SB_A20GATE - @m39_lib.M39	21C4
SB_ACZ_BITCLK	SB_ACZ_BITCLK - @m39_lib.M39	21C6
SB_ACZ_RST_L	SB_ACZ_RST_L - @m39_lib.M39	21C6
SB_ACZ_SDATAOUT	SB_ACZ_SDATAOUT - @m39_lib.M39	21C6
SB_ACZ_SYNC	SB_ACZ_SYNC - @m39_lib.M39	21C6
SB_CLK14P3M_TIMER	SB_CLK14P3M_TIMER - @m39_lib.M39	5B8 23D3 34D4
SB_CLK48M_USBCTLR	SB_CLK48M_USBCTLR - @m39_lib.M39	5B8 23D3 34C4
SB_CLK100M_DMI_N	SB_CLK100M_DMI_N - @m39_lib.M39	5B8 22C2 34A4 34C2
SB_CLK100M_DMI_P	SB_CLK100M_DMI_P - @m39_lib.M39	5B8 22C2 34A4 34C2
SB_CLK100M_SATA_N	SB_CLK100M_SATA_N - @m39_lib.M39	5C8 21B6 34B4 34C2
SB_CLK100M_SATA_OE_L	SB_CLK100M_SATA_OE_L - @m39_lib.M39	23C3 33B4
SB_CLK100M_SATA_P	SB_CLK100M_SATA_P - @m39_lib.M39	5C8 21B6 34B4 34C2
SB_CRT_TVOUT_MUX	SB_CRT_TVOUT_MUX - @m39_lib.M39	22B5
SB_GPIO2	SB_GPIO2 - @m39_lib.M39	22A6 26C2
SB_GPIO3	SB_GPIO3 - @m39_lib.M39	22A6 26C2
SB_GPIO4	SB_GPIO4 - @m39_lib.M39	22A6 26C2
SB_GPIO19	SB_GPIO19 - @m39_lib.M39	23D3
SB_GPIO21	SB_GPIO21 - @m39_lib.M39	23D3
SB_GPIO26	SB_GPIO26 - @m39_lib.M39	23C7
SB_GPIO29	SB_GPIO29 - @m39_lib.M39	22C4 22D8
SB_GPIO30	SB_GPIO30 - @m39_lib.M39	22C4 22D8
SB_GPIO31	SB_GPIO31 - @m39_lib.M39	22C4 22D8
SB_GPIO37	SB_GPIO37 - @m39_lib.M39	23D3
SB_INTVRMEN	SB_INTVRMEN - @m39_lib.M39	21D6
SB_RTC_RST_L	SB_RTC_RST_L - @m39_lib.M39	21D6 26C7
SB_RTC_X1	SB_RTC_X1 - @m39_lib.M39	21D6 26D7
SB_RTC_X2	SB_RTC_X2 - @m39_lib.M39	21D6 26D7
SB_SM_INTRUDER_L	SB_SM_INTRUDER_L - @m39_lib.M39	21D6 26C7
SB_SPKR	SB_SPKR - @m39_lib.M39	23C5
SC_RX_L	SC_RX_L - @m39_lib.M39	58C5 59B6 59C4
SC_TX_L	SC_TX_L - @m39_lib.M39	58C5 59B4 59B6
SDVO_CTRLCLK	SDVO_CTRLCLK - @m39_lib.M39	14B6 19A2
	TP_SDVO_CTRLCLK - @m39_lib.M39	19A1
SDVO_CTRLDATA	SDVO_CTRLDATA - @m39_lib.M39	14B6 19A2
	TP_SDVO_CTRLDATA - @m39_lib.M39	19A1
SMB_ALERT_L	SMB_ALERT_L - @m39_lib.M39	23C5
SMB_BSA_CLK	SMB_BSA_CLK - @m39_lib.M39	58B5 59C1
SMB_BSA_DATA	SMB_BSA_DATA - @m39_lib.M39	58B5 59C1
SMB_BSB_CLK	SMB_BSB_CLK - @m39_lib.M39	58C5 59D1
SMB_BSB_DATA	SMB_BSB_DATA - @m39_lib.M39	58C7 59D1
SMB_LINK_ALERT_L	SMB_LINK_ALERT_L - @m39_lib.M39	23D5
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @m39_lib.M39	58D5 59D5
	TP_SMC_ADAPTER_EN - @m39_lib.M39	59D3
SMC_ANALOG_ID	SMC_ANALOG_ID - @m39_lib.M39	58A7 59C6
	NC_SMC_ANALOG_ID - @m39_lib.M39	59C5
SMC_BATT_CHG_EN	SMC_BATT_CHG_EN - @m39_lib.M39	58D7 59D6
	NC_SMC_BATT_CHG_EN - @m39_lib.M39	59D5
SMC_BATT_ISENSE	SMC_BATT_ISENSE - @m39_lib.M39	58D5 59B6
	UNUSED_SMC_SENSE - @m39_lib.M39	59B5 59B5 59B6
	SMC_FWIRE_ISENSE - @m39_lib.M39	58D5 59B6
	UNUSED_SMC_SENSE - @m39_lib.M39	59B5 59B5 59B6
	SMC_FWIRE_ISENSE - @m39_lib.M39	58D5 59B6
SMC_BATT_ISET	SMC_BATT_ISET - @m39_lib.M39	58B5 59D6
	NC_SMC_BATT_ISET - @m39_lib.M39	59D5
SMC_BATT_TRICKLE_EN_L	SMC_BATT_TRICKLE_EN_L - @m39_lib.M39	58D7 59D6
	NC_SMC_BATT_TRICKLE_EN_L - @m39_lib.M39	59D5
SMC_BATT_VSET	SMC_BATT_VSET - @m39_lib.M39	58B5 59D6
	NC_SMC_BATT_VSET - @m39_lib.M39	59D5
SMC_BC_ACOK	SMC_BC_ACOK - @m39_lib.M39	58C5 59B4
SMC_BS_ALRT_L	SMC_BS_ALRT_L - @m39_lib.M39	58C5 59B4
SMC_CASE_OPEN	SMC_CASE_OPEN - @m39_lib.M39	58C5 59C1
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @m39_lib.M39	58D5 76D2
SMC_CPU_RESET_3_3_L	SMC_CPU_RESET_3_3_L - @m39_lib.M39	58B5 59A7
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @m39_lib.M39	58D5 76B2
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE - @m39_lib.M39	58D5 76D5
SMC_EXCARD_CP	SMC_EXCARD_CP - @m39_lib.M39	58B7 59C4
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @m39_lib.M39	58B7 59C5
	TP_SMC_EXCARD_PWR_EN - @m39_lib.M39	59C3
SMC_EXCARD_PWR_OC_L	SMC_EXCARD_PWR_OC_L - @m39_lib.M39	58B7 59C4
SMC_EXTAL	SMC_EXTAL - @m39_lib.M39	58C3 59B8
SMC_EXTSMI_L	SMC_EXTSMI_L - @m39_lib.M39	23B8 58B7
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @m39_lib.M39	58B7 65D8
	FAN_RPM0 - @m39_lib.M39	65D7
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @m39_lib.M39	58B7 65C8
SMC_FAN_1_CTL	SMC_FAN_1_CTL - @m39_lib.M39	58B7 65B8 66D8
SMC_FAN_1_TACH	SMC_FAN_1_TACH - @m39_lib.M39	58B7 65A8 66C8
SMC_FAN_2_CTL	SMC_FAN_2_CTL - @m39_lib.M39	58B7 65B8 66D8
SMC_FAN_2_TACH	SMC_FAN_2_TACH - @m39_lib.M39	58B7 65A8 66C8
SMC_FAN_3_CTL	SMC_FAN_3_CTL - @m39_lib.M39	58B7 59C5
	TP_SMC_FAN_3_CTL - @m39_lib.M39	59C3
SMC_FAN_3_TACH	SMC_FAN_3_TACH - @m39_lib.M39	58B7 59C5
	TP_SMC_FAN_3_TACH - @m39_lib.M39	59C3
SMC_FWE	SMC_FWE - @m39_lib.M39	58B5 59B4
SMC_GPU_VSENSE	SMC_GPU_VSENSE - @m39_lib.M39	58D5 59B3
SMC_LID	SMC_LID - @m39_lib.M39	58B5 59C1
SMC_LRESET_L	SMC_LRESET_L - @m39_lib.M39	6B7 58C7
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @m39_lib.M39	5D1 59D8
SMC_MD1	SMC_MD1 - @m39_lib.M39	58C1 60B5
SMC_MEM_ISENSE	SMC_MEM_ISENSE - @m39_lib.M39	58A7 59B6
	NC_SMC_MEM_ISENSE - @m39_lib.M39	59B5
SMC_NB_ISENSE	SMC_NB_ISENSE - @m39_lib.M39	58A7 59B6
	NC_SMC_NB_ISENSE - @m39_lib.M39	59B5
SMC_NMI	SMC_NMI - @m39_lib.M39	58C1 60B4
SMC_ODD_DETECT	SMC_ODD_DETECT - @m39_lib.M39	58B7 59C4
SMC_ONOFF_L	SMC_ONOFF_L - @m39_lib.M39	58C5 59B7 59C4
SMC_PB7	SMC_PB7 - @m39_lib.M39	59C5 59C5
	TP_SMC_PB7 - @m39_lib.M39	59C3 59C3
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE - @m39_lib.M39	58D5 76C6
SMC_PBUS_VSENSE_R	SMC_PBUS_VSENSE_R - @m39_lib.M39	76C8
SMC_PF0	SMC_PF0 - @m39_lib.M39	58B5 59D5
	TP_SMC_PF0 - @m39_lib.M39	59D3
SMC_PF1	SMC_PF1 - @m39_lib.M39	58B5 59D5
	TP_SMC_PF1 - @m39_lib.M39	59D3
SMC_PM_G2_EN	SMC_PM_G2_EN - @m39_lib.M39	58D5 59D5
	TP_PM_G2_EN - @m39_lib.M39	59D3
SMC_PROCHOT	SMC_PROCHOT - @m39_lib.M39	58B5 59C7
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @m39_lib.M39	58D5 59A7
SMC_RCIN_L	SMC_RCIN_L - @m39_lib.M39	21C3 58C7
SMC_REF_GATE1	SMC_REF_GATE1 - @m39_lib.M39	59A5
SMC_REF_GATE2	SMC_REF_GATE2 - @m39_lib.M39	59A4
SMC_REF_IN	SMC_REF_IN - @m39_lib.M39	59A4
SMC_RSTGATE_L	SMC_RSTGATE_L - @m39_lib.M39	42C3 44A8 58D7
SMC_RST_L	SMC_RST_L - @m39_lib.M39	58C3 59D7 60B4
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @m39_lib.M39	23C8 58B7
SMC_RX_L	SMC_RX_L - @m39_lib.M39	5D1 58C7 59B4 59B5 60B4
SMC_SB_NMI	SMC_SB_NMI - @m39_lib.M39	23C3 58D7
SMC_SMB_0_CLK	SMC_SMB_0_CLK - @m39_lib.M39	58C7 59D1
	TP_SMC_SMB_0_CLK - @m39_lib.M39	59D1
SMC_SMB_0_DATA	SMC_SMB_0_DATA - @m39_lib.M39	58C5 59D1
	TP_SMC_SMB_0_DATA - @m39_lib.M39	59D1
SMC_SYS_ISET	SMC_SYS_ISET - @m39_lib.M39	58B5 59D6
	NC_SMC_SYS_ISET - @m39_lib.M39	59D5
SMC_SYS_KBDLED	SMC_SYS_KBDLED - @m39_lib.M39	58C7 59D5
	TP_SMC_SYS_KBDLED - @m39_lib.M39	59D3
SMC_SYS_LED	SMC_SYS_LED - @m39_lib.M39	58C7 59D7
SMC_SYS_VSET	SMC_SYS_VSET - @m39_lib.M39	58B5 59D6
	NC_SMC_SYS_VSET - @m39_lib.M39	59D5
SMC_TCK	SMC_TCK - @m39_lib.M39	5D1 58C5 59B4 60B4
SMC_TDI	SMC_TDI - @m39_lib.M39	5D1 58B5 59B4 60B4
SMC_TDO	SMC_TDO - @m39_lib.M39	5D1 58B5 59B4 60B5
SMC_THRMTRIP	SMC_THRMTRIP - @m39_lib.M39	58B5 59C7
SMC_TMS	SMC_TMS - @m39_lib.M39	5D1 58B5 59B4 60B5
SMC_TPM_GPIO	SMC_TPM_GPIO - @m39_lib.M39	58D5 59B6
SMC_TPM_PP	SMC_TPM_PP - @m39_lib.M39	58C7 59A6
SMC_TPM_RESET_L	SMC_TPM_RESET_L - @m39_lib.M39	58B7 59C6 67B7
SMC_TRST_L	SMC_TRST_L - @m39_lib.M39	5D1 58C1 60B5
SMC_TX_L	SMC_TX_L - @m39_lib.M39	5D1 58C7 59B4 59B5 60B5
SMC_VCL	SMC_VCL - @m39_lib.M39	58D3
SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @m39_lib.M39	23C1 58D5
SMC_XDP_TCK	SMC_XDP_TCK - @m39_lib.M39	58C7 59A2
SMC_XDP_TCK_3_3	SMC_XDP_TCK_3_3 - @m39_lib.M39	58B5 59A5
SMC_XDP_TCK_R	SMC_XDP_TCK_R - @m39_lib.M39	59A1
SMC_XDP_TDI_L	SMC_XDP_TDI_L - @m39_lib.M39	58C7 59B3
SMC_XDP_TDO_3_3_L	SMC_XDP_TDO_3_3_L - @m39_lib.M39	58B7 59A5
SMC_XDP_TMS_L	SMC_XDP_TMS_L - @m39_lib.M39	58C7 59B2
SMC_XDP_TRST_L	SMC_XDP_TRST_L - @m39_lib.M39	58C7 59A3
SMC_XDP_TRST_L_R	SMC_XDP_TRST_L_R - @m39_lib.M39	59A3
SMC_XTAL	SMC_XTAL - @m39_lib.M39	58C3 59B8

SMLINK<0>	SMLINK<0> - @m39_lib.M39	23D5
SMLINK<1>	SMLINK<1> - @m39_lib.M39	23D5
SMS_INT_L	SMS_INT_L - @m39_lib.M39	23C3 26C2 58B5
SMS_ONOFF_L	SMS_ONOFF_L - @m39_lib.M39	58A5 59B4
SMS_X_AXIS	SMS_X_AXIS - @m39_lib.M39	58B7 59B6
	NC_SMS_X_AXIS - @m39_lib.M39	59B5
SMS_Y_AXIS	SMS_Y_AXIS - @m39_lib.M39	58B7 59B6
	NC_SMS_Y_AXIS - @m39_lib.M39	59B5
SMS_Z_AXIS	SMS_Z_AXIS - @m39_lib.M39	58A7 59B6
	NC_SMS_Z_AXIS - @m39_lib.M39	59B5
SPARE_SRC3_N	SPARE_SRC3_N - @m39_lib.M39	34D2
SPARE_SRC3_P	SPARE_SRC3_P - @m39_lib.M39	34D2
SPARE_SRC7_N	SPARE_SRC7_N - @m39_lib.M39	34D2
SPARE_SRC7_P	SPARE_SRC7_P - @m39_lib.M39	34D2
SPI_ARB	SPI_ARB - @m39_lib.M39	22C6 58D5
SPI_CE_L	SPI_CE_L - @m39_lib.M39	22C6 58B5 63C7
SPI_HOLD_L	SPI_HOLD_L - @m39_lib.M39	63C4
SPI_SCLK	SPI_SCLK - @m39_lib.M39	22C6 58D5 63C7
SPI_SCLK_R	SPI_SCLK_R - @m39_lib.M39	63C4
SPI_SI	SPI_SI - @m39_lib.M39	22C6 58D5 63C1
SPI_SI_R	SPI_SI_R - @m39_lib.M39	63C3
SPI_SO	SPI_SO - @m39_lib.M39	22C6 58D5 63C1
SPI_SO_R	SPI_SO_R - @m39_lib.M39	63C3
SPI_WP_L	SPI_WP_L - @m39_lib.M39	63C4
SPKRAMP_MUTE	SPKRAMP_MUTE - @m39_lib.M39	72B5
SPKRAMP_SS	SPKRAMP_SS - @m39_lib.M39	72B4
SUS_CLK_SB	SUS_CLK_SB - @m39_lib.M39	23C3 59B5
	SMC_SUS_CLK - @m39_lib.M39	58C5 59B6
SV_SET_UP	SV_SET_UP - @m39_lib.M39	23B6 23C3 60B3
SW_RST_BTN_L	SW_RST_BTN_L - @m39_lib.M39	5D1 26C6
SW_RST_DEBNC	SW_RST_DEBNC - @m39_lib.M39	26C4
SYS_LED_DRV_C	SYS_LED_DRV_C - @m39_lib.M39	59D6
SYS_LED_DRV_K	SYS_LED_DRV_K - @m39_lib.M39	59D6
SYS_ONEWIRE	SYS_ONEWIRE - @m39_lib.M39	58B7 59B4
SYS_POWERFAIL_L	SYS_POWERFAIL_L - @m39_lib.M39	6D8 76D2
SYS_PWRUP_L	SYS_PWRUP_L - @m39_lib.M39	6C7
THERM_DX_N	THERM_DX_N - @m39_lib.M39	10B5 10C5
THERM_DX_P	THERM_DX_P - @m39_lib.M39	10B5 10C5
THRM_ALERT_L	THRM_ALERT_L - @m39_lib.M39	10D3
THRM_THM	THRM_THM - @m39_lib.M39	10C4
TMDS_CK_TERM	TMDS_CK_TERM - @m39_lib.M39	97C8
TMDS_CLK_N	TMDS_CLK_N - @m39_lib.M39	93C3 97C8
TMDS_CLK_P	TMDS_CLK_P - @m39_lib.M39	93C3 97C8
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @m39_lib.M39	97C4 97C7
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @m39_lib.M39	97C4 97C7
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @m39_lib.M39	97C4 97D7
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @m39_lib.M39	97C4 97D7
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @m39_lib.M39	97C7 97D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @m39_lib.M39	97C4 97D7
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @m39_lib.M39	97C4 97D7
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @m39_lib.M39	97C7 97D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @m39_lib.M39	93C3 97D8
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @m39_lib.M39	93C3 97D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @m39_lib.M39	93C3 97C8
TMDS_DATA_N<3>	TMDS_DATA_N<3> - @m39_lib.M39	93C3 95D6
TMDS_DATA_N<4>	TMDS_DATA_N<4> - @m39_lib.M39	93C3 95D6
TMDS_DATA_N<5>	TMDS_DATA_N<5> - @m39_lib.M39	93C3 95D6
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @m39_lib.M39	93C3 97D8
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @m39_lib.M39	93C3 97C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @m39_lib.M39	93C3 97C8
TMDS_DATA_P<3>	TMDS_DATA_P<3> - @m39_lib.M39	93C3 95D6
TMDS_DATA_P<4>	TMDS_DATA_P<4> - @m39_lib.M39	93C3 95D6
TMDS_DATA_P<5>	TMDS_DATA_P<5> - @m39_lib.M39	93C3 95D6
TPM_BADD	TPM_BADD - @m39_lib.M39	67C4
TPM_GPIO1	TPM_GPIO1 - @m39_lib.M39	59B5 67C6
TPM_GPIO2	TPM_GPIO2 - @m39_lib.M39	59B5 67C6
TPM_LRESET_L	TPM_LRESET_L - @m39_lib.M39	6B7 67B7
TPM_PP	TPM_PP - @m39_lib.M39	59A5 67C6
TPM_RST_L	TPM_RST_L - @m39_lib.M39	67B6
TPM_XTALI	TPM_XTALI - @m39_lib.M39	59B7 67C6
TPM_XTALO	TPM_XTALO - @m39_lib.M39	59B7 67C6
TP_ATI_ROMCS_L	TP_ATI_ROMCS_L - @m39_lib.M39	91A3
TP_AZ_DOCK_EN_L	TP_AZ_DOCK_EN_L - @m39_lib.M39	23C5
TP_AZ_DOCK_RST_L	TP_AZ_DOCK_RST_L - @m39_lib.M39	23C5
TP_CLK14P5M_SPARE	TP_CLK14P5M_SPARE - @m39_lib.M39	34C4
TP_CPU_A32_L	TP_CPU_A32_L - @m39_lib.M39	7C7
TP_CPU_A33_L	TP_CPU_A33_L - @m39_lib.M39	7B7
TP_CPU_A34_L	TP_CPU_A34_L - @m39_lib.M39	7B7
TP_CPU_A35_L	TP_CPU_A35_L - @m39_lib.M39	7B7
TP_CPU_A36_L	TP_CPU_A36_L - @m39_lib.M39	7B7
TP_CPU_A37_L	TP_CPU_A37_L - @m39_lib.M39	7B7
TP_CPU_A38_L	TP_CPU_A38_L - @m39_lib.M39	7B7
TP_CPU_A39_L	TP_CPU_A39_L - @m39_lib.M39	7B7
TP_CPU_APM0_L	TP_CPU_APM0_L - @m39_lib.M39	7B7
TP_CPU_APM1_L	TP_CPU_APM1_L - @m39_lib.M39	7B7
TP_CPU_CPUSLP_L	TP_CPU_CPUSLP_L - @m39_lib.M39	21C4
TP_CPU_EXTBREF	TP_CPU_EXTBREF - @m39_lib.M39	7B6
TP_CPU_HFPLL	TP_CPU_HFPLL - @m39_lib.M39	7B7
TP_CPU_SPARE0	TP_CPU_SPARE0 - @m39_lib.M39	7B6
TP_CPU_SPARE1	TP_CPU_SPARE1 - @m39_lib.M39	7B6
TP_CPU_SPARE2	TP_CPU_SPARE2 - @m39_lib.M39	7B6
TP_CPU_SPARE3	TP_CPU_SPARE3 - @m39_lib.M39	7B6
TP_CPU_SPARE4	TP_CPU_SPARE4 - @m39_lib.M39	7B6
TP_CPU_SPARE5	TP_CPU_SPARE5 - @m39_lib.M39	7B6
TP_CPU_SPARE6	TP_CPU_SPARE6 - @m39_lib.M39	7B6
TP_CPU_SPARE7	TP_CPU_SPARE7 - @m39_lib.M39	7B6
TP_FB_A_MA12	TP_FB_A_MA12 - @m39_lib.M39	87D5
TP_FB_A_ODT<0>	TP_FB_A_ODT<0> - @m39_lib.M39	87B5
TP_FB_A_ODT<1>	TP_FB_A_ODT<1> - @m39_lib.M39	87B5
TP_FB_B_MA12	TP_FB_B_MA12 - @m39_lib.M39	87D1
TP_FB_B_ODT<0>	TP_FB_B_ODT<0> - @m39_lib.M39	87B1
TP_FB_B_ODT<1>	TP_FB_B_ODT<1> - @m39_lib.M39	87B1
TP_FW_CNA	TP_FW_CNA - @m39_lib.M39	44B3
TP_FW_LKON	TP_FW_LKON - @m39_lib.M39	44B3
TP_FW_LPS	TP_FW_LPS - @m39_lib.M39	44B3
TP_FW_MPCIACT_L	TP_FW_MPCIACT_L - @m39_lib.M39	44B3
TP_FW_NANDTREE	TP_FW_NANDTREE - @m39_lib.M39	44B3
TP_FW_ROM_AD	TP_FW_ROM_AD - @m39_lib.M39	44B3
TP_FW_VAUX_PRES	TP_FW_VAUX_PRES - @m39_lib.M39	44B3
TP_LVDS_VBG	TP_LVDS_VBG - @m39_lib.M39	13D5
TP_MEM_A_A<14>	TP_MEM_A_A<14> - @m39_lib.M39	28C3
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @m39_lib.M39	28C3
TP_MEM_B_A<14>	TP_MEM_B_A<14> - @m39_lib.M39	5B4 29C3
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @m39_lib.M39	5B4 29C3
TP_NB_TESTIN_L	TP_NB_TESTIN_L - @m39_lib.M39	14D6
TP_NB_XOR_FSB2_H7	TP_NB_XOR_FSB2_H7 - @m39_lib.M39	14D6
TP_NB_XOR_LVDS_A34	TP_NB_XOR_LVDS_A34 - @m39_lib.M39	14C6
TP_NB_XOR_LVDS_A35	TP_NB_XOR_LVDS_A35 - @m39_lib.M39	14C6
TP_NB_XOR_LVDS_D27	TP_NB_XOR_LVDS_D27 - @m39_lib.M39	14C6
TP_NB_XOR_LVDS_D28	TP_NB_XOR_LVDS_D28 - @m39_lib.M39	14C6
TP_PCI_CLK_SPARE	TP_PCI_CLK_SPARE - @m39_lib.M39	5B4 34C4
TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m39_lib.M39	22B6
TP_PCI_GNT1_L	TP_PCI_GNT1_L - @m39_lib.M39	22B6
TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m39_lib.M39	22B6
TP_PCI_GNT4_L	TP_PCI_GNT4_L - @m39_lib.M39	22B6
TP_PCI_PME_L	TP_PCI_PME_L - @m39_lib.M39	22A6
TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m39_lib.M39	21C6
TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m39_lib.M39	21C6
TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m39_lib.M39	21D4
TP_SB_GPIO6	TP_SB_GPIO6 - @m39_lib.M39	23C5
TP_SB_GPIO23	TP_SB_GPIO23 - @m39_lib.M39	21D5
TP_SB_GPIO25_DO_NOT_USE	TP_SB_GPIO25_DO_NOT_USE - @m39_lib.M39	23C3
TP_SB_GPIO38	TP_SB_GPIO38 - @m39_lib.M39	23C3
TP_SB_RSVD9	TP_SB_RSVD9 - @m39_lib.M39	22A6
TP_SB_SATALED_L	TP_SB_SATALED_L - @m39_lib.M39	21C6
TP_SB_XOR_AD5	TP_SB_XOR_AD5 - @m39_lib.M39	22A7
TP_SB_XOR_AD9	TP_SB_XOR_AD9 - @m39_lib.M39	22A7
TP_SB_XOR_AE5	TP_SB_XOR_AE5 - @m39_lib.M39	22A7
TP_SB_XOR_AE9	TP_SB_XOR_AE9 - @m39_lib.M39	22A6
TP_SB_XOR_AG4	TP_SB_XOR_AG4 - @m39_lib.M39	22A7
TP_SB_XOR_AG8	TP_SB_XOR_AG8 - @m39_lib.M39	22A6
TP_SB_XOR_AH4	TP_SB_XOR_AH4 - @m39_lib.M39	22A7
TP_SB_XOR_AH8	TP_SB_XOR_AH8 - @m39_lib.M39	22A6
TP_SB_XOR_T5	TP_SB_XOR_T5 - @m39_lib.M39	21C6
TP_SB_XOR_U3	TP_SB_XOR_U3 - @m39_lib.M39	21C6
TP_SB_XOR_U5	TP_SB_XOR_U5 - @m39_lib.M39	21C6
TP_SB_XOR_U7	TP_SB_XOR_U7 - @m39_lib.M39	21C6
TP_SB_XOR_V3	TP_SB_XOR_V3 - @m39_lib.M39	21C6
TP_SB_XOR_V4	TP_SB_XOR_V4 - @m39_lib.M39	21C6
TP_SB_XOR_V6	TP_SB_XOR_V6 - @m39_lib.M39	21C6
TP_SB_XOR_V7	TP_SB_XOR_V7 - @m39_lib.M39	21C6
TP_SB_XOR_W1	TP_SB_XOR_W1 - @m39_lib.M39	21C6
TP_SB_XOR_W3	TP_SB_XOR_W3 - @m39_lib.M39	21C6
TP_SB_XOR_Y1	TP_SB_XOR_Y1 - @m39_lib.M39	21C6
TP_SB_XOR_Y2	TP_SB_XOR_Y2 - @m39_lib.M39	21C6
TP_U5999_P1	TP_U5999_P1 - @m39_lib.M39	59A7
TP_U5999_P13	TP_U5999_P13 - @m39_lib.M39	59A5
TP_U5999_P14	TP_U5999_P14 - @m39_lib.M39	59A5
TP_U8400_AG14	TP_U8400_AG14 - @m39_lib.M39	91A5
TP_U8900_J2	TP_U8900_J2 - @m39_lib.M39	89A7
TP_U8900_J3	TP_U8900_J3 - @m39_lib.M39	89A7
TP_U8950_J2	TP_U8950_J2 - @m39_lib.M39	89A4
TP_U8950_J3	TP_U8950_J3 - @m39_lib.M39	89A4
TP_U9000_J2	TP_U9000_J2 - @m39_lib.M39	90A7
TP_U9000_J3	TP_U9000_J3 - @m39_lib.M39	90A7
TP_U9050_J2	TP_U9050_J2 - @m39_lib.M39	90A4
TP_U9050_J3	TP_U9050_J3 - @m39_lib.M39	90A4
TSENSE_GPU_DXP	TSENSE_GPU_DXP - @m39_lib.M39	61C5
TSENSE_NB_DXP	TSENSE_NB_DXP - @m39_lib.M39	61B5
TSENSE_NB_GPU_DXN	TSENSE_NB_GPU_DXN - @m39_lib.M39	61B5
TV_DACA_OUT	TV_DACA_OUT - @m39_lib.M39	13C5 19B1
	TV_DACB_OUT - @m39_lib.M39	13C5 19B1
	TV_DACC_OUT - @m39_lib.M39	13C5 19B1
	TV_IRTNA - @m39_lib.M39	13C5 19B1
	TV_IRTNB - @m39_lib.M39	13C5 19B1
	TV_IRTNC - @m39_lib.M39	13C5 19B1
	TV_IREF - @m39_lib.M39	13C5 19B1
	PP3V3_S0_NB_VCCA_TVBG - @m39_lib.M39	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACC - @m39_lib.M39	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACB - @m39_lib.M39	17C6 19B1
	PP3V3_S0_NB_VCCA_TVDACA - @m39_lib.M39	17C6 19B1
	=PP1V5_S0_NB_TVDAC - @m39_lib.M39	6C4 19B2 19D7
	=PP1V5_S0_AIRPORT - @m39_lib.M39	6C4 53D3
	PP1V5_S0 - @m39_lib.M39	6C6 80C2
	=PP1V5_S0_SB - @m39_lib.M39	6C4 25A8 25C8
	=PP1V5_S0_SB_VCC1_5_A - @m39_lib.M39	6C4 24A3 25C1
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @m39_lib.M39	6C4 24A3 25B1
	=PP1V5_S0_SB_VCCUSBPLL - @m39_lib.M39	6C4 24A5 25B6
	=PP1V5_S0_SB_VCC1_5_A_ATX - @m39_lib.M39	6C4 24A5 25C6
	=PP1V5_S0_SB_VCCSATAPLL - @m39_lib.M39	6C4 24B5 25D6
	=PP1V5_S0_SB_VCC1_5_A_ARX - @m39_lib.M39	6C4 24B5 25D6
	=PP1V5_S0_NB_3GPLL - @m39_lib.M39	6C4 19A6 19A6
	=PP1V5_S0_NB_PLL - @m39_lib.M39	6C4 19C8 19D7
	=PP1V5_S0_NB_VCCAUX - @m39_lib.M39	6C4 6C4 16D1 17B6 19A7 19D7
	=PP1V5_S0_NB_VCCD_HMPLL - @m39_lib.M39	6C4 17C6 19D7
	=PP1V5_S0_NB_PCIE - @m39_lib.M39	6C4 13D2 19D7
	=PP1V5_S0_CPU - @m39_lib.M39	6C4 8B6 8C5
	=PP1V5_S0_AIRPORT - @m39_lib.M39	6C4 53D3
U600_3	U600_3 - @m39_lib.M39	6C7
U600_6	U600_6 - @m39_lib.M39	6B7
U600_8	U600_8 - @m39_lib.M39	6B7
U600_11	U600_11 - @m39_lib.M39	6A7
U2698_4	U2698_4 - @m39_lib.M39	26C4
U3100_VDDQ	U3100_VDDQ - @m39_lib.M39	31C5
U6100_VCC	U6100_VCC - @m39_lib.M39	61C4
U8595_1	U8595_1 - @m39_lib.M39	85D2
USB_AIRPORT_N	USB_AIRPORT_N - @m39_lib.M39	53B4
USB_AIRPORT_P	USB_AIRPORT_P - @m39_lib.M39	53B4
USB_A_N	USB_A_N - @m39_lib.M39	22C2 47D7
USB_A_OC_L	USB_A_OC_L - @m39_lib.M39	22C4 22D8 47B8 47B8
USB_A_P	USB_A_P - @m39_lib.M39	22C2 47C7
USB_B_N	USB_B_N - @m39_lib.M39	22C2 53B2
USB_B_OC_L	USB_B_OC_L - @m39_lib.M39	22C4 22D8 47B8
USB_B_P	USB_B_P - @m39_lib.M39	22C2 53B2
USB_CAMERA_N	USB_CAMERA_N - @m39_lib.M39	47B2
USB_CAMERA_P	USB_CAMERA_P - @m39_lib.M39	47B2
USB_C_N	USB_C_N - @m39_lib.M39	22C2 47B7
USB_C_OC_L	USB_C_OC_L - @m39_lib.M39	22C4 22D8 47B7 47B8
USB_C_P	USB_C_P - @m39_lib.M39	22C2 47B7
USB_D_N	USB_D_N - @m39_lib.M39	22C2 47B3
USB_D_OC_L	USB_D_OC_L - @m39_lib.M39	22C4 22D8 47B7
USB_D_P	USB_D_P - @m39_lib.M39	22C2 47B3
USB_E_N	USB_E_N - @m39_lib.M39	22C2 47A7
USB_E_OC_L	USB_E_OC_L - @m39_lib.M39	22C4 22D8 47B7
USB_E_P	USB_E_P - @m39_lib.M39	22C2 47A7
USB_F_N	USB_F_N - @m39_lib.M39	22C2 49C6
	USB_FLASH_N - @m39_lib.M39	49C5
USB_F_P	USB_F_P - @m39_lib.M39	22C2 49C6
	USB_FLASH_P - @m39_lib.M39	49C5
USB_G_N	USB_G_N - @m39_lib.M39	22C2 47A3
	USB_BT_N - @m39_lib.M39	47A3
USB_G_P	USB_G_P - @m39_lib.M39	22C2 47A3
	USB_BT_P - @m39_lib.M39	47A3
USB_H_N	USB_H_N - @m39_lib.M39	22C2 47C3
USB_H_P	USB_H_P - @m39_lib.M39	22C2 47C3
USB_IR_N	USB_IR_N - @m39_lib.M39	47C2
USB_IR_P	USB_IR_P - @m39_lib.M39	47C2
USB_PORT0_N	USB_PORT0_N - @m39_lib.M39	47D5
USB_PORT0_P	USB_PORT0_P - @m39_lib.M39	47C5
USB_PORT1_N	USB_PORT1_N - @m39_lib.M39	47B5
USB_PORT1_P	USB_PORT1_P - @m39_lib.M39	47B5
USB_PORT2_N	USB_PORT2_N - @m39_lib.M39	47A5
USB_PORT2_P	USB_PORT2_P - @m39_lib.M39	47A5
USB_RBIAS_PN	USB_RBIAS_PN - @m39_lib.M39	22C2
VGA_B	VGA_B - @m39_lib.M39	97B6 97C5
VGA_G	VGA_G - @m39_lib.M39	97A6 97C5
VGA_HSYNC	VGA_HSYNC - @m39_lib.M39	97A3 97C5
VGA_R	VGA_R - @m39_lib.M39	97A6 97C5
VGA_VSYNC	VGA_VSYNC - @m39_lib.M39	97A3 97C5
VMAIN_AVLBL	VMAIN_AVLBL - @m39_lib.M39	41C7
VOL_DOWN	VOL_DOWN - @m39_lib.M39	68A6 68C7
VOL_UP	VOL_UP - @m39_lib.M39	68A6 68C7
VREG_FB	VREG_FB - @m39_lib.M39	68A3
VR_PWRGD_CK410	VR_PWRGD_CK410 - @m39_lib.M39	23C5 26A8
VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m39_lib.M39	5C7 14B6 26D5 75C6
XDP_BPM_L<0>	XDP_BPM_L<0> - @m39_lib.M39	7C6 11B3
XDP_BPM_L<1>	XDP_BPM_L<1> - @m39_lib.M39	7C6 11B3
XDP_BPM_L<2>	XDP_BPM_L<2> - @m39_lib.M39	7C6 11B3
XDP_BPM_L<3>	XDP_BPM_L<3> - @m39_lib.M39	7C6 11B3
XDP_BPM_L<4>	XDP_BPM_L<4> - @m39_lib.M39	7C6 11B3
XDP_BPM_L<5>	XDP_BPM_L<5> - @m39_lib.M39	7C6 11B3
XDP_DBRESET_L	XDP_DBRESET_L - @m39_lib.M39	7C6 11B4 26B5
XDP_TCK	XDP_TCK - @m39_lib.M39	5D1 7A8 7C6 11B3 11B3 59A1 59A6
XDP_TDI	XDP_TDI - @m39_lib.M39	5D1 7B8 7C6 11B3 59B2
XDP_TDO	XDP_TDO - @m39_lib.M39	5D1 7C6 11B5 59A6
XDP_TMS	XDP_TMS - @m39_lib.M39	5D1 7B8 7C6 11B3 59B1
XDP_TRST_L	XDP_TRST_L - @m39_lib.M39	5D1 7C6 11B3 59A2
ZH701P1	ZH701P1 - @m39_lib.M39	6A3
ZH702P1	ZH702P1 - @m39_lib.M39	6A3
ZH703P1	ZH703P1 - @m39_lib.M39	6A3

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C85A0	CAP_402	m39[85D1]
C600	CAP_402	m39[6C7]
C601	CAP_402	m39[6A3]
C602	CAP_402	m39[6A3]
C603	CAP_402	m39[6A3]
C610	CAP_402	m39[6C7]
C699	CAP_P_CASE-C1	m39[6D7]
C0800	CAP_402	m39[8B5]
C0801	CAP_603	m39[8B5]
C900	CAP_805	m39[9B6]
C901	CAP_805	m39[9B6]
C902	CAP_805	m39[9A6]
C903	CAP_805	m39[9A6]
C904	CAP_805	m39[9A6]
C905	CAP_805	m39[9A6]
C906	CAP_805	m39[9A6]
C907	CAP_805	m39[9B5]
C908	CAP_805	m39[9B7]
C909	CAP_805	m39[9B5]
C910	CAP_805	m39[9B7]
C911	CAP_805	m39[9B7]
C912	CAP_805	m39[9A7]
C913	CAP_805	m39[9A7]
C914	CAP_805	m39[9A7]
C915	CAP_805	m39[9A7]
C916	CAP_805	m39[9A7]
C917	CAP_805	m39[9A7]
C918	CAP_805	m39[9A7]
C919	CAP_805	m39[9A7]
C920	CAP_805	m39[9A5]
C921	CAP_805	m39[9A7]
C922	CAP_805	m39[9A7]
C923	CAP_805	m39[9B7]
C924	CAP_805	m39[9A7]
C925	CAP_805	m39[9A7]
C926	CAP_402	m39[9B7]
C928	CAP_805	m39[9B6]
C929	CAP_805	m39[9B5]
C930	CAP_805	m39[9A6]
C931	CAP_805	m39[9A5]
C932	CAP_805	m39[9A6]
C934	CAP_402	m39[9B7]
C935	CAP_402	m39[9B7]
C936	CAP_402	m39[9B7]
C937	CAP_402	m39[9B6]
C938	CAP_402	m39[9B6]
C939	CAP_805	m39[9A5]
C940	CAP_P_CASE-C1	m39[9C7]
C941	CAP_P_3P_D2T	m39[9A7]
C942	CAP_P_3P_D2T	m39[9A7]
C943	CAP_P_3P_D2T	m39[9A7]
C944	CAP_P_3P_D2T	m39[9A7]
C945	CAP_P_3P_D2T	m39[9A6]
C946	CAP_P_3P_D2T	m39[9A6]
C950	CAP_402	m39[9D4]
C951	CAP_402	m39[9D3]
C952	CAP_402	m39[9D3]
C953	CAP_402	m39[9D2]
C1000	CAP_402	m39[10C6]
C1001	CAP_402	m39[10D4]
C1100	CAP_402	m39[11A3]
C1211	CAP_402	m39[12C3]
C1226	CAP_402	m39[12B6]
C1236	CAP_402	m39[12A6]
C1610	CAP_402	m39[16B5]
C1611	CAP_402	m39[16B4]
C1612	CAP_402	m39[16B4]
C1613	CAP_402	m39[16B8]
C1614	CAP_402	m39[16B8]
C1615	CAP_402	m39[16B6]
C1620	CAP_603	m39[16B5]
C1621	CAP_603	m39[16B5]
C1711	CAP_402	m39[17A3]
C1712	CAP_402	m39[17A3]
C1713	CAP_402	m39[17B3]
C1900	CAP_P_CASE-C1	m39[19B5]
C1901	CAP_P_CASE-C1	m39[19B5]
C1902	CAP_603	m39[19B5]
C1903	CAP_603	m39[19B4]
C1904	CAP_402	m39[19B4]
C1905	CAP_402	m39[19B4]
C1906	CAP_402	m39[19B3]
C1907	CAP_402	m39[19B3]
C1914	CAP_603	m39[19A8]
C1915	CAP_402	m39[19A7]
C1916	CAP_402	m39[19A8]
C1918	CAP_402	m39[19A7]
C1920	CAP_402	m39[19A2]
C1921	FILTER_3P_A_NFM18	m39[19B2]
C1934	CAP_805	m39[19C7]
C1935	CAP_402	m39[19C7]
C1936	CAP_805	m39[19C7]
C1937	CAP_402	m39[19C7]
C1965	CAP_603	m39[19B8]
C1966	CAP_603	m39[19B7]
C1967	CAP_402	m39[19B7]
C1968	CAP_P_CASE-C1	m39[19B7]
C1970	CAP_P_SMB2	m39[19A5]
C1971	CAP_603	m39[19A4]
C1972	CAP_603	m39[19A4]
C1975	CAP_603	m39[19A4]
C1976	CAP_402	m39[19A4]
C1981	CAP_603	m39[19B6]
C1982	CAP_603	m39[19B8]
C2500	CAP_P_SMB2	m39[25B8]
C2501	CAP_402	m39[25A6]
C2502	CAP_402	m39[25D4]
C2503	CAP_402	m39[25D8]
C2504	CAP_402	m39[25C8]
C2505	CAP_402	m39[25B7]
C2506	CAP_402	m39[25B7]
C2507	CAP_402	m39[25B7]
C2508	CAP_603	m39[25A6]
C2509	CAP_402	m39[25B8]
C2510	CAP_402	m39[25C1]
C2511	CAP_402	m39[25D6]
C2512	CAP_402	m39[25B1]
C2513	CAP_402	m39[25C6]
C2514	CAP_402	m39[25C6]
C2515	CAP_402	m39[25B6]
C2516	CAP_P_CASE-C2	m39[25D3]
C2517	CAP_402	m39[25D6]
C2518	CAP_402	m39[25D4]
C2519	CAP_402	m39[25D3]
C2520	CAP_402	m39[25B6]
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C2533	CAP_402	m39[25C1]
C2534	CAP_402	m39[25D1]
C2605	CAP_402	m39[26C7]
C2607	CAP_402	m39[26D5]
C2608	CAP_402	m39[26D8]
C2609	CAP_402	m39[26D8]
C2610	CAP_402	m39[26C7]
C2611	CAP_402	m39[26B7]
C2698	CAP_402	m39[26C4]
C2699	CAP_402	m39[26C5]
C2800	CAP_402	m39[28D6]
C2801	CAP_603	m39[28B2]
C2802	CAP_603	m39[28B2]
C2803	CAP_603	m39[28B1]
C2804	CAP_603	m39[28B1]
C2810	CAP_402	m39[28B2]
C2811	CAP_402	m39[28B2]
C2812	CAP_402	m39[28B1]
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C2814	CAP_402	m39[28B2]
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C2816	CAP_402	m39[28B1]
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C2818	CAP_402	m39[28B2]
C2819	CAP_402	m39[28B2]
C2820	CAP_402	m39[28B1]
C2821	CAP_402	m39[28B1]
C2850	CAP_603	m39[28D6]
C2851	CAP_603	m39[28A6]
C2852	CAP_402	m39[28A6]
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C2908	CAP_402	m39[29B2]
C2909	CAP_402	m39[29B2]
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C2920	CAP_402	m39[29B2]
C2921	CAP_402	m39[29B2]
C2922	CAP_402	m39[29B1]
C2923	CAP_402	m39[29B1]
C2950	CAP_603	m39[29D6]
C2951	CAP_603	m39[29A7]
C2952	CAP_402	m39[29A6]
C3004	CAP_402	m39[30B4]
C3005	CAP_402	m39[30D4]
C3006	CAP_402	m39[30B3]
C3007	CAP_402	m39[30D3]
C3008	CAP_402	m39[30A3]
C3009	CAP_402	m39[30A4]
C3010	CAP_402	m39[30D4]
C3011	CAP_402	m39[30D3]
C3013	CAP_402	m39[30A4]
C3014	CAP_402	m39[30A4]
C3015	CAP_402	m39[30A3]
C3030	CAP_402	m39[30C4]
C3033	CAP_402	m39[30C3]
C3035	CAP_402	m39[30C3]
C3100	CAP_402	m39[31C4]
C3101	CAP_603	m39[31B6]
C3102	CAP_603	m39[31B4]
C3105	CAP_P_SMC-LF	m39[31B4]
C3109	CAP_603	m39[31C5]
C3110	CAP_402	m39[31B6]
C3301	CAP_402	m39[33D6]
C3302	CAP_402	m39[33D6]
C3303	CAP_402	m39[33D6]
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C3306	CAP_402	m39[33D4]
C3307	CAP_402	m39[33C4]
C3308	CAP_402	m39[33D4]
C3309	CAP_603	m39[33D4]
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C3314	CAP_402	m39[33D8]
C3315	CAP_402	m39[33D7]
C3316	CAP_603	m39[33D7]
C3317	CAP_603	m39[33D4]
C3389	CAP_402	m39[33C7]
C3390	CAP_402	m39[33C7]
C3800	CAP_402	m39[38B7]
C3801	CAP_402	m39[38B7]
C3802	CAP_402	m39[38B7]
C3803	CAP_402	m39[38B7]
C3804	CAP_402	m39[38C3]
C3805	CAP_402	m39[38C2]
C3806	CAP_805-2	m39[38C1]
C4101	CAP_402	m39[41D7]
C4102	CAP_402	m39[41D6]
C4103	CAP_402	m39[41D6]
C4104	CAP_402	m39[41D6]
C4105	CAP_402	m39[41D5]
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C4107	CAP_402	m39[41D2]
C4110	CAP_402	m39[41D4]
C4111	CAP_402	m39[41D4]
C4112	CAP_402	m39[41C4]
C4113	CAP_402	m39[41C4]
C4115	CAP_402	m39[41B5]
C4116	CAP_402	m39[41B5]
C4117	CAP_402	m39[41B2]
C4118	CAP_402	m39[41B2]
C4126	CAP_402	m39[41A8]
C4127	CAP_402	m39[41A8]
C4128	CAP_402	m39[41A8]
C4129	CAP_402	m39[41A8]
C4130	CAP_402	m39[41A7]
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C4137	CAP_402	m39[41A5]
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C4139	CAP_402	m39[41A4]
C4140	CAP_402	m39[41B3]
C4150	CAP_402	m39[41D5]
C4200	CAP_1210	m39[42D8]
C4201	CAP_402	m39[42D7]
C4202	CAP_1210	m39[42D7]
C4203	CAP_1206-1	m39[42D6]
C4204	CAP_402	m39[42D6]
C4205	CAP_1210	m39[42C5]
C4206	CAP_402	m39[42C5]
C4209	CAP_603	m39[42B7]
C4210	CAP_402	m39[42B6]
C4300	CAP_402	m39[43D7]
C4301	CAP_402	m39[43D6]
C4304	CAP_402	m39[43C6]
C4305	CAP_402	m39[43B6]
C4401	CAP_402	m39[44D1]
C4402	CAP_402	m39[44C1]
C4410	CAP_402	m39[44D6]
C4412	CAP_402	m39[44D1]
C4500	CAP_402	m39[45D4]
C4501	CAP_402	m39[45D3]
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C4503	CAP_603	m39[45C6]
C4504	CAP_402	m39[45C4]
C4505	CAP_402	m39[45C5]
C4506	CAP_402	m39[45C5]
C4507	CAP_402	m39[45C5]
C4508	CAP_402	m39[45D5]
C4509	CAP_402	m39[45D5]
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C4515	CAP_603	m39[45D6]
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C4522	CAP_402	m39[45D3]
C4523	CAP_402	m39[45D3]
C4609	CAP_603-1	m39[46D5]
C4610	CAP_402	m39[46D4]
C4611	CAP_402	m39[46D4]
C4612	CAP_402	m39[46C4]
C4613	CAP_402	m39[46C4]
C4615	CAP_603-1	m39[46C2]
C4616	CAP_402	m39[46B2]
C4620	CAP_402	m39[46B4]
C4621	CAP_402	m39[46B4]
C4622	CAP_402	m39[46A4]
C4623	CAP_402	m39[46A4]
C4625	CAP_603-1	m39[46A2]
C4626	CAP_402	m39[46A2]
C4650	CAP_402	m39[46C7]
C4654	CAP_402	m39[46B8]
C4660	CAP_402	m39[46C7]
C4664	CAP_402	m39[46B7]
C4710	CAP_P_SMD2	m39[47D6]
C4712	CAP_402	m39[47D5]
C4713	CAP_402	m39[47D5]
C4720	CAP_P_SMD	m39[47C6]
C4722	CAP_402	m39[47C5]
C4723	CAP_402	m39[47C5]
C4732	CAP_402	m39[47A5]
C4733	CAP_402	m39[47A5]
C4742	CAP_402	m39[47D2]
C4743	CAP_402	m39[47D1]
C4797	CAP_805-2	m39[47D3]
C4798	CAP_402	m39[47A2]
C4799	CAP_805-2	m39[47A2]
C4950	CAP_805-2	m39[49C4]
C4951	CAP_402	m39[49C4]
C5300	CAP_402	m39[53B7]
C5301	CAP_402	m39[53B7]
C5304	CAP_402	m39[53D5]
C5305	CAP_402	m39[53D5]
C5306	CAP_402	m39[53D4]
C5307	CAP_402	m39[53C4]
C5308	CAP_402	m39[53C5]
C5309	CAP_402	m39[53C4]
C5310	CAP_402	m39[53C4]
C5311	CAP_603	m39[53C3]
C5312	CAP_603	m39[53D4]
C5313	CAP_402	m39[53C5]
C5314	CAP_603	m39[53C4]
C5800	CAP_402	m39[59B8]
C5801	CAP_402	m39[59B8]
C5802	CAP_805	m39[58D3]
C5803	CAP_402	m39[58D2]
C5804	CAP_402	m39[58D2]
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C5806	CAP_402	m39[58D1]
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C5901	CAP_402	m39[59D8]
C5902	CAP_402	m39[59B7]
C5903	CAP_402	m39[59A8]
C5919	CAP_402	m39[59B4]
C5940	CAP_402	m39[59A4]
C5941	CAP_402	m39[59A3]
C5942	CAP_603	m39[59A3]
C5943	CAP_402	m39[59A5]
C6000	CAP_402	m39[60D6]
C6001	CAP_402	m39[60D6]
C6002	CAP_402	m39[60C6]
C6003	CAP_402	m39[60C6]
C6100	CAP_402	m39[61B5]
C6101	CAP_402	m39[61B5]
C6301	CAP_402	m39[63C2]
C6308	CAP_402	m39[63C5]
C6309	CAP_402	m39[63C6]
C6311	CAP_402	m39[63C2]
C6312	CAP_402	m39[63D3]
C6500	CAP_603	m39[65D5]
C6501	CAP_805	m39[65D5]
C6502	CAP_603	m39[65B4]
C6503	CAP_805	m39[65B5]
C6504	CAP_P_6.3X11-TH-LF	m39[65C4]
C6505	CAP_P_6.3X11-TH-LF	m39[65B3]
C6600	CAP_603	m39[66D4]
C6601	CAP_805	m39[66C5]
C6602	CAP_P_SM-LF	m39[66C3]
C6650	CAP_402	m39[66B5]
C6651	CAP_402	m39[66A5]
C6652	CAP_402	m39[66B3]
C6653	CAP_402	m39[66A3]
C6654	CAP_402	m39[66B4]
C6655	CAP_402	m39[66B2]
C6700	CAP_402	m39[67C4]
C6701	CAP_402	m39[67C4]
C6702	CAP_402	m39[67C3]
C6703	CAP_402	m39[67C3]
C6704	CAP_402	m39[59B7]
C6705	CAP_402	m39[59B7]
C6800	CAP_603	m39[68D6]
C6801	CAP_402	m39[68D6]
C6802	CAP_P_B2	m39[68D4]
C6803	CAP_P_B2	m39[68D3]
C6804	CAP_P_SMA-LF	m39[68B4]
C6805	CAP_805	m39[68B3]
C6806	CAP_805	m39[68B3]
C6807	CAP_P_SMA-LF	m39[68B3]
C6808	CAP_402	m39[68B3]
C6809	CAP_402	m39[68B2]
C6810	CAP_P_SMA-LF	m39[68B2]
C6811	CAP_402	m39[68B2]
C6812	CAP_402	m39[68B4]
C6813	CAP_402	m39[68B3]
C6821	CAP_402	m39[68C6]
C6822	CAP_603	m39[68A5]
C6823	CAP_402	m39[68A4]
C6825	CAP_402	m39[68A3]
C6826	CAP_603	m39[68A3]
C6829	CAP_402	m39[68B3]
C6830	CAP_402	m39[68D4]
C6832	CAP_402	m39[68B2]
C6833	CAP_402	m39[68B2]
C6834	CAP_402	m39[68B2]
C6835	CAP_402	m39[68D6]
C6836	CAP_402	m39[68D3]
C7200	CAP_P_6.3X8-SM	m39[72D5]
C7201	CAP_1210	m39[72D5]
C7202	CAP_805	m39[72D4]
C7203	CAP_1210	m39[72D3]
C7204	CAP_805	m39[72D6]
C7205	CAP_805	m39[72C6]
C7206	CAP_805	m39[72C6]
C7207	CAP_805	m39[72C6]
C7208	CAP_603-1	m39[72C4]
C7209	CAP_805	m39[72B4]
C7210	CAP_402	m39[72B3]
C7211	CAP_402	m39[72B2]
C7212	CAP_402	m39[72B2]
C7213	CAP_402	m39[72B2]
C7214	CAP_603	m39[72B5]
C7215	CAP_402	m39[72C6]
C7216	CAP_402	m39[72C6]
C7217	CAP_P_6.3X8-SM	m39[72D6]
C7218	CAP_603	m39[72D5]
C7219	CAP_603	m39[72D4]
C7220	CAP_402	m39[72B7]
C7221	CAP_402	m39[72B7]
C7223	CAP_1210	m39[72D3]
C7300	CAP_402	m39[73D7]
C7301	CAP_402	m39[73D6]
C7302	CAP_402	m39[73D6]
C7303	CAP_402	m39[73D6]
C7311	CAP_402	m39[73A7]
C7312	CAP_402	m39[73A6]
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C7314	CAP_402	m39[73A7]
C7315	CAP_402	m39[73A6]
C7317	CAP_402	m39[73B4]
C7318	CAP_805	m39[73B4]
C7321	CAP_402	m39[73C5]
C7322	CAP_402	m39[73C5]
C7323	CAP_402	m39[73A6]
C7324	CAP_402	m39[73A5]
C7400	CAP_402	m39[74B4]
C7401	CAP_402	m39[74C4]
C7402	CAP_402	m39[74A4]
C7403	CAP_P_CASE-B-SM	m39[74B7]
C7404	CAP_P_CASE-B-SM	m39[74B6]
C7405	CAP_P_CASE-B-SM	m39[74C7]
C7406	CAP_P_CASE-B-SM	m39[74C6]
C7407	CAP_402	m39[74D8]
C7408	CAP_402	m39[74D7]
C7409	CAP_402	m39[74B8]
C7410	CAP_402	m39[74A8]
C7411	CAP_402	m39[74B8]
C7412	CAP_402	m39[74A8]
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C7414	CAP_402	m39[74A7]
C7415	CAP_402	m39[74A8]
C7416	CAP_402	m39[74A8]
C7417	CAP_402	m39[74A8]
C7418	CAP_805	m39[74A5]
C7419	CAP_603-1	m39[74A4]
C7420	CAP_402	m39[74A7]
C7421	CAP_402	m39[74A7]
C7422	CAP_402	m39[74A7]
C7423	CAP_402	m39[74A7]
C7500	CAP_402	m39[75C4]
C7501	CAP_P_TH-MCZ	m39[75C2]
C7502	CAP_402	m39[75B4]
C7503	CAP_402	m39[75C1]
C7504	CAP_402	m39[75B1]
C7505	CAP_402	m39[75C8]
C7506	CAP_402	m39[75B7]
C7507	CAP_402	m39[75B7]
C7508	CAP_1210	m39[75C2]
C7509	CAP_1210	m39[75D1]
C7510	CAP_402	m39[75C8]
C7511	CAP_603	m39[75B2]

C7512	CAP_603	m39[75C2]
C7513	CAP_402	m39[75B7]
C7514	CAP_402	m39[75B8]
C7515	CAP_603	m39[75C4]
C7516	CAP_402	m39[75B4]
C7517	CAP_P_SM-3	m39[75D2]
C7518	CAP_P_SM-3	m39[75D2]
C7521	CAP_402	m39[75A6]
C7526	CAP_603	m39[75D6]
C7527	CAP_603	m39[75C5]
C7528	CAP_402	m39[75B5]
C7529	CAP_402	m39[75B5]
C7530	CAP_402	m39[75D6]
C7531	CAP_402	m39[75B5]
C7532	CAP_402	m39[75B6]
C7533	CAP_402	m39[75B6]
C7534	CAP_402	m39[75B5]
C7535	CAP_603	m39[75D5]
C7550	CAP_603	m39[75D1]
C7551	CAP_603	m39[75D1]
C7590	CAP_402	m39[75C3]
C7592	CAP_402	m39[75B3]
C7596	CAP_402	m39[75D6]
C7597	CAP_1210	m39[75D1]
C7598	CAP_1210	m39[75D1]
C7599	CAP_402	m39[76D6]
C7600	CAP_402	m39[76D3]
C7601	CAP_402	m39[76D3]
C7602	CAP_402	m39[76D2]
C7603	CAP_402	m39[76C4]
C7612	CAP_402	m39[76B2]
C7633	CAP_402	m39[76C7]
C7659	CAP_402	m39[76D4]
C7669	CAP_402	m39[76D4]
C7700	CAP_603	m39[77D4]
C7703	CAP_402	m39[77C4]
C7704	CAP_402	m39[77C4]
C7706	CAP_402	m39[77C4]
C7709	CAP_805	m39[77C3]
C7710	CAP_402	m39[77C7]
C7711	CAP_402	m39[77B7]
C7712	CAP_402	m39[77C7]
C7750	CAP_402	m39[77A5]
C7751	CAP_805	m39[77B4]
C7752	CAP_805	m39[77B4]
C7753	CAP_402	m39[77A7]
C7754	CAP_402	m39[77B6]
C7755	CAP_805	m39[77B3]
C7756	CAP_805	m39[77B3]
C7757	CAP_402	m39[77A6]
C7799	CAP_402	m39[77A3]
C7800	CAP_1210	m39[78C3]
C7801	CAP_P_SM-LF	m39[78C4]
C7802	CAP_603	m39[78C6]
C7803	CAP_603	m39[78B6]
C7804	CAP_402	m39[78C6]
C7805	CAP_603	m39[78C4]
C7806	CAP_805-1	m39[78B2]
C7807	CAP_P_CASE-D2E-LF	m39[78B3]
C7809	CAP_402	m39[78B3]
C7810	CAP_402	m39[78B4]
C7811	CAP_402	m39[78B5]
C7813	CAP_1206	m39[78B4]
C7814	CAP_402	m39[78B5]
C7817	CAP_P_CASE-D2E-LF	m39[78B2]
C7900	CAP_402	m39[79D6]
C7901	CAP_603	m39[79D5]
C7902	CAP_402	m39[79C5]
C7903	CAP_603	m39[79C7]
C7906	CAP_402	m39[79C5]
C7907	CAP_402	m39[79C3]
C7908	CAP_402	m39[79C5]
C7909	CAP_1206	m39[79C4]
C7910	CAP_P_SM-3	m39[79D4]
C7911	CAP_1210	m39[79D3]
C7912	CAP_P_CASE-D2E-LF	m39[79C3]
C7913	CAP_1206	m39[79C2]
C7980	CAP_402	m39[79B3]
C7992	CAP_603	m39[79D6]
C7998	CAP_P_CASE-D2E-LF	m39[79C3]
C8000	CAP_1210	m39[80D3]
C8001	CAP_P_CASE-D2E-LF	m39[80C3]
C8002	CAP_603	m39[80D6]
C8003	CAP_402	m39[80C3]
C8004	CAP_1206	m39[80C4]
C8005	CAP_402	m39[80C4]
C8006	CAP_402	m39[80D6]
C8009	CAP_603	m39[80C6]
C8010	CAP_603	m39[80C4]
C8011	CAP_402	m39[80C5]
C8012	CAP_402	m39[80C5]
C8014	CAP_P_TH-MCZ	m39[80D4]
C8015	CAP_1210	m39[80D3]
C8016	CAP_805-1	m39[80C2]
C8099	CAP_P_CASE-D2E-LF	m39[80C2]
C8100	CAP_402	m39[81D6]
C8101	CAP_603	m39[81C5]
C8102	CAP_402	m39[81C5]
C8103	CAP_603	m39[81C7]
C8106	CAP_402	m39[81C5]
C8107	CAP_402	m39[81C3]
C8108	CAP_402	m39[81C5]
C8109	CAP_1206	m39[81C4]
C8110	CAP_1210	m39[81D4]
C8111	CAP_1210	m39[81D3]
C8112	CAP_1210	m39[81D3]
C8114	CAP_P_CASE-D2E-LF	m39[81C3]
C8115	CAP_805-1	m39[81C2]
C8190	CAP_P_CASE-D2E-LF	m39[81C3]
C8192	CAP_603	m39[81D6]
C8198	CAP_1210	m39[81D3]
C8199	CAP_402	m39[81A5]
C8398	CAP_603	m39[83B4]
C8399	CAP_603	m39[83C4]
C8400	CAP_805	m39[84C7]
C8401	CAP_402	m39[84C7]
C8402	CAP_402	m39[84C7]
C8405	CAP_805	m39[84B7]
C8406	CAP_402	m39[84B7]
C8407	CAP_402	m39[84B7]
C8410	CAP_805	m39[84B6]
C8411	CAP_402	m39[84B7]
C8412	CAP_402	m39[84B7]
C8413	CAP_402	m39[84B7]

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C8451	CAP_402	m39[84B5]
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C8486	CAP_402	m39[84B2]
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C8502	CAP_603	m39[85D6]
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C8507	CAP_402	m39[85C7]
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C8522	CAP_402	m39[85C5]
C8523	CAP_402	m39[85B2]
C8530	CAP_1210	m39[85D4]
C8531	CAP_1210	m39[85D4]
C8532	CAP_1210	m39[85D4]
C8540	CAP_805	m39[85C2]
C8541	CAP_805	m39[85C2]
C8542	CAP_P_CASE-D2E-LF	m39[85C2]
C8543	CAP_P_CASE-D2E-LF	m39[85C2]
C8551	CAP_603	m39[85B8]
C8555	CAP_402	m39[85B7]
C8556	CAP_805	m39[85B6]
C8557	CAP_805	m39[85B6]
C8560	CAP_402	m39[85A6]
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C8586	CAP_402	m39[85A3]
C8589	CAP_805	m39[85A3]
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C8592	CAP_402	m39[85C2]
C8595	CAP_402	m39[85D1]
C8598	CAP_402	m39[85D2]
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C8614	CAP_402	m39[86C6]
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C8616	CAP_402	m39[86C5]
C8630	CAP_805	m39[86C6]
C8631	CAP_402	m39[86C6]
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C8634	CAP_402	m39[86C5]
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C8692	CAP_402	m39[86D5]
C8695	CAP_805	m39[86D2]
C8696	CAP_402	m39[86D3]
C8697	CAP_402	m39[86D3]
C8711	CAP_402	m39[87B7]
C8713	CAP_402	m39[87B7]
C8715	CAP_402	m39[87A7]
C8716	CAP_402	m39[87A6]
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C8723	CAP_402	m39[87B4]
C8725	CAP_402	m39[87A4]
C8726	CAP_402	m39[87A3]
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C8902	CAP_402	m39[89D7]
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C8920	CAP_805	m39[89C8]
C8921	CAP_402	m39[89C8]
C8922	CAP_402	m39[89C7]
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C8925	CAP_402	m39[89C7]
C8926	CAP_402	m39[89C6]
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C8933	CAP_402	m39[89C6]
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C8965	CAP_402	m39[89D3]
C8970	CAP_805	m39[89C5]
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C8974	CAP_402	m39[89C4]
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C8983	CAP_402	m39[89C3]
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C9033	CAP_402	m39[90C6]
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C9051	CAP_402	m39[90D4]
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C9060	CAP_402	m39[90D3]
C9065	CAP_402	m39[90D3]
C9070	CAP_805	m39[90C5]
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C9081	CAP_402	m39[90C3]
C9083	CAP_402	m39[90C3]
C9100	CAP_805	m39[91C5]
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C9102	CAP_402	m39[91C5]
C9103	CAP_402	m39[91C5]
C9110	CAP_805	m39[91C5]
C9111	CAP_402	m39[91C5]
C9112	CAP_402	m39[91C5]
C9115	CAP_805	m39[91B5]
C9116	CAP_402	m39[91B5]
C9117	CAP_402	m39[91B5]
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C9125	CAP_805	m39[91B5]
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C9127	CAP_402	m39[91B5]
C9130	CAP_805	m39[91A6]
C9131	CAP_402	m39[91A6]
C9132	CAP_402	m39[91A5]
C9135	CAP_805	m39[91A6]

C9136	CAP_402	m39[91A6]
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C9140	CAP_805	m39[91A6]
C9141	CAP_402	m39[91A6]
C9142	CAP_402	m39[91A5]
C9191	CAP_402	m39[91D2]
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C9302	CAP_402	m39[93C5]
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C9307	CAP_402	m39[93C5]
C9310	CAP_805	m39[93C6]
C9311	CAP_402	m39[93C6]
C9312	CAP_402	m39[93C5]
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C9316	CAP_402	m39[93B8]
C9317	CAP_402	m39[93B7]
C9320	CAP_805	m39[93B6]
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C9342	CAP_402	m39[93A5]
C9345	CAP_805	m39[93A6]
C9346	CAP_402	m39[93A5]
C9347	CAP_402	m39[93A5]
C9400	CAP_603-1	m39[94C7]
C9401	CAP_402	m39[94C6]
C9410	CAP_402	m39[94C6]
C9420	CAP_1210	m39[94C5]
C9470	CAP_402	m39[94B2]
C9700	CAP_402	m39[97C8]
C9710	CAP_603	m39[97C3]
C9711	CAP_402	m39[97D3]
C9713	CAP_402	m39[97C2]
C9714	CAP_402	m39[97C2]
C9740	CAP_402	m39[97A7]
C9741	CAP_402	m39[97A6]
C9742	CAP_402	m39[97A6]
D2500	DIODE_SCHOT_SOT23	m39[25C8]
D2501	DIODE_SCHOT_SOT23	m39[25D8]
D2600	DIODE_SCHOT_SOT23	m39[26D8]
D2601	DIODE_SCHOT_SOT23	m39[26C8]
D4600	DIODE_SMC	m39[46D5]
D4690	ZENER_SOT23	m39[46A6]
D4700	DIODE_SCHOT_3P_A_SC-75	m39[47C5]
D4701	DIODE_SCHOT_3P_A_SC-75	m39[47B5]
D4702	DIODE_SCHOT_3P_A_SC-75	m39[47A5]
D4705	DIODE_SCHOT_3P_A_SC-75	m39[47C6]
D4706	DIODE_SCHOT_3P_A_SC-75	m39[47B6]
D4707	DIODE_SCHOT_3P_A_SC-75	m39[47A6]
D4710	DIODE_SCHOT_3P_A_SC-75	m39[47C6]
D4900	DIODE_SCHOT_3P_A_SC-75	m39[49B4]
D6500	DIODE_SOT23	m39[65C4]
D6501	DIODE_SOT23	m39[65B4]
D6502	DIODE_SCHOT_SMB	m39[65C4]
D6503	DIODE_SCHOT_SMB	m39[65B4]
D6600	DIODE_SOT23	m39[66C4]
D6601	DIODE_SCHOT_SMB	m39[66C3]
D7500	DIODE_SCHOT_SMB	m39[75C3]
D7501	DIODE_SCHOT_SMB	m39[75B2]
D7599	DIODE_SOT23	m39[76D6]
D8520	DIODE_SCHOT_SMB	m39[85C3]
D9700	ZENER_CASE425	m39[97C1]
DP4610	DIODE_DUAL_6P_SOT-363	m39[46D4 46D3]
DP4611	DIODE_DUAL_6P_SOT-363	m39[46C4 46C3]
DP4620	DIODE_DUAL_6P_SOT-363	m39[46B4 46B3]
DP4621	DIODE_DUAL_6P_SOT-363	m39[46A4 46A3]
DZ7300	SUPPR_TRANSIENT_4P1_0405	m39[73C6]
DZ7301	SUPPR_TRANSIENT_4P1_0405	m39[73A5]
DZ7302	SUPPR_TRANSIENT_4P1_0405	m39[73A4]
DZ7303	SUPPR_TRANSIENT_4P1_0405	m39[73C5]
DZ7304	SUPPR_TRANSIENT_4P1_0405	m39[73C4]
F4600	FUSE_SM-LF	m39[46D2]
F4601	FUSE_SM-LF	m39[46D2]
F4602	FUSE_MINISMD-LF	m39[46D3]
F4701	FUSE_MINISMD-LF	m39[47D3]
F9710	FUSE_SM-LF	m39[97D5]
FL4610	FILTER_4P_2012	m39[46C3]
FL4620	FILTER_4P_2012	m39[46B3]
FL9740	FILTER_LC_SM-220MHZ-LF	m39[97B7]
FL9741	FILTER_LC_SM-220MHZ-LF	m39[97A7]
FL9742	FILTER_LC_SM-220MHZ-LF	m39[97A7]
FLE011	FILTER_4P_2012	m39[46C3]
FLE021	FILTER_4P_2012	m39[46B3]
GV3801	HOLE_VIA	m39[38A8]
GV3802	HOLE_VIA	m39[38A7]
GV3803	HOLE_VIA	m39[38A8]
GV3804	HOLE_VIA	m39[38A7]
GV3805	HOLE_VIA	m39[38A8]
GV3806	HOLE_VIA	m39[38A7]
GV3807	HOLE_VIA	m39[38A8]
GV3808	HOLE_VIA	m39[38A7]
J2	CON_2RTSM_125_SM-2MT-BLK-LF	m39[61B7]
J3	CON_2RTSM_125_SM-2MT-BLK-LF	m39[61B6]

J600	CON_M14RT_D_THA_M-RT-TH1	m39[6D7]
J0700	CPU_YONAH_SKT_BGA	m39[7C3 7D7]
J0700	CPU_YONAH_SKT_BGA	m39[8D4 8D8]
J1000	CON_2RTSM_125_SM-2MT-BLK-LF	m39[10B7]
J1101	CON_F28RT_S2MT_SM_F-RT-SM	m39[11C2]
J2600	BATTERY_2P_TH	m39[26C8]
J2800	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m39[28D5]
J2900	CON_F200RT_DDR2DIMM_5MT_SM_F-RT-SM1	m39[29D5]
J2901	CON_F4ST_S2MT_SM_F-T-SM	m39[59C7]
J2903	CON_M2ST_S2MT_SM_M-S-T-SM	m39[59C8]
J4700	CON_F10ST_D_SMA_F-ST-SM	m39[47A2]
J4950	CON_F4ST_S2MT_SM_F-S-T-SM	m39[49C4]
J5300	CON_F52RT_D2MT_SM_F-RT-SM	m39[53C5]
J6000	CON_F30STSM_5047_SM1	m39[60B5]
J6500	CON_M4RT_S2MT_SM_M-R-T-SM	m39[65D3]
J6501	CON_M5RT_S2MT_SMA_M-RT-SM	m39[65B2]
J6600	CON_F4ST_S2MT_SM_F-S-T-SM	m39[66C2]
J6601	CON_M4RT_S2MT_SM_M-R-T-SM	m39[66B5]
J6602	CON_M4RT_S2MT_SM_M-R-T-SM	m39[66B3]
J7300	CON_F4ST_S4MT_TH1_F-ST-TH	m39[73D8]
J7301	CON_M7RT_S2MT_SM_M-R-T-SM	m39[73D1]
J7303	CON_F9ANG_S4MT_TH1_F-ANG-TH	m39[73B3]
J9402	CON_F30ST_D_SM_F-ST-SM	m39[94B6]
J9710	CON_DVI_F32ST_Q2MT_SM_F-ST-SM	m39[97D5]
JC900	CON_M7ST_SATA_SM_M-S-T-SM	m39[38B8]
JC901	CON_M50SM_5MM_M-ST-S-M2-LF	m39[38C2]
JD600	CON_RJ45_10ANG_S3MT_TH1_F-ANG-TH	m39[43C6]
JE000	CON_F6ST_S4MT_TH1_F-ST-TH	m39[46C2]
JE001	CON_F6ST_S4MT_TH1_F-ST-TH	m39[46B2]
JE310	CON_F4ST_USB_S3MT_TH_F-ST-TH	m39[47D4]
JE320	CON_F4ST_USB_S3MT_TH_F-ST-TH	m39[47B4]
JE330	CON_F4ST_USB_S3MT_TH_F-ST-TH	m39[47A4]
JE350	CON_M14RT_S2MT_SM_M-RT-SM	m39[47C1]
L1934	IND_0603	m39[19C7]
L1936	IND_0603	m39[19C7]
L1970	IND_1210	m39[19A5]
L1975	IND_0805	m39[19A5]
L2500	IND_SM-3	m39[25B8]
L2507	IND_1206	m39[25A7]
L3301	IND_0402	m39[33D7]
L3302	IND_0402	m39[33D3]
L4200	IND_SM	m39[42D7]
L4201	IND_SM	m39[42B7]
L4300	IND_SM	m39[43D7]
L4409	IND_0402	m39[44D6]
L4610	IND_1206-LF	m39[46D2]
L4620	IND_1206-LF	m39[46B2]
L4690	IND_SM-1	m39[46A6]
L4710	IND_SM	m39[47D6]
L4712	FILTER_4P_2012	m39[47C6]
L4720	IND_SM	m39[47C6]
L4722	FILTER_4P_2012	m39[47B6]
L4730	IND_SM	m39[47B6]
L4732	FILTER_4P_2012	m39[47A6]
L4740	IND_SM	m39[47D2]
L4742	FILTER_4P_2012	m39[47C2]
L4752	FILTER_4P_2012	m39[47B2]
L5300	FILTER_4P_2012	m39[53B3]
L6800	IND_0402	m39[68A5]
L6801	IND_0402	m39[68D6]
L7200	IND_SM-1	m39[72D6]
L7201	IND_0603	m39[72C2]
L7202	IND_0603	m39[72C2]
L7203	IND_0603	m39[72C3]
L7204	IND_0603	m39[72C3]
L7205	IND_0603	m39[72D6]
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L7309	IND_SM	m39[73C6]
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L7325	IND_SM	m39[73A5]
L7326	IND_SM	m39[73B5]
L7327	IND_SM	m39[73B5]
L7328	IND_SM	m39[73A5]

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L7501	IND_SM	m39[75B2]
L7502	IND_TH-VERT-LF	m39[76D8]
L7700	IND_SM1-LF	m39[77C4]
L7750	IND_SM-LF	m39[77B4]
L7800	IND_3P_SM	m39[78B3]
L7900	IND_3P_SM	m39[79C3]
L8000	IND_IHLP	m39[80C3]
L8100	IND_IHLP	m39[81C3]
L8400	IND_0402	m39[84B7]
L8520	IND_IHLP	m39[85C3]
L8585	IND_4P_2COIL_SDQ1215-0-SM	m39[85A3]
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L9060	IND_0402	m39[90D4]
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L9125	IND_0402	m39[91B6]
L9130	IND_0402	m39[91B7]
L9135	IND_0402	m39[91A7]
L9140	IND_0402	m39[91A7]
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L9325	IND_0402	m39[93B7]
L9330	IND_0402	m39[93B7]
L9345	IND_0402	m39[93B7]
L9400	IND_SM	m39[94C6]
L9700	FILTER_4P_SM	m39[97D7]
L9701	FILTER_4P_SM	m39[97D7]
L9702	FILTER_4P_SM	m39[97C7]
L9703	FILTER_4P_SM	m39[97C7]
L9710	IND_SM-1	m39[97D5]
LED600	LED_2.0X1.25MM-SM	m39[6A7]
LED601	LED_2.0X1.25MM-SM	m39[6A8]
LED602	LED_2.0X1.25MM-SM	m39[6A7]
LED2901	LED_3X2MM-SM	m39[59D6]
LED3800	LED_2.0X1.25MM-SM	m39[38B3]
LED4300	LED_2.0X1.25MM-SM	m39[43D2]
LED4301	LED_2.0X1.25MM-SM	m39[43D2]
LED4302	LED_2.0X1.25MM-SM	m39[43D1]
LED4303	LED_2.0X1.25MM-SM	m39[43D1]
LED7900	LED_2.0X1.25MM-SM	m39[79A4]
LED8000	LED_2.0X1.25MM-SM	m39[80A4]
LED8100	LED_2.0X1.25MM-SM	m39[81A4]
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PP5E2	PROBEPOINT_SM	m39[5B8]
PP6A0	PROBEPOINT_SM	m39[5A6]
PP6A1	PROBEPOINT_SM	m39[5A6]
PP6A2	PROBEPOINT_SM	m39[5A6]
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PP6A7	PROBEPOINT_SM	m39[5A6]
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PP701	TP_SM-TP50-TOP	m39[5D3]
PP702	TP_SM-TP50-TOP	m39[5D3]
PP1200	TP_SM-TP50-TOP	m39[5D3]
PP1201	TP_SM-TP50-TOP	m39[5D3]
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PP2801	TP_SM-TP50-TOP	m39[5C3]
PP2802	TP_SM-TP50-TOP	m39[5C3]
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PP8729	PROBEPOINT_SM	m39[5C5]
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PP9036	PROBEPOINT_SM	m39[5A4]
Q4200	TRA_2N7002_SOT23-LF	m39[42D2]
Q4201	TRA_PBSS5540Z_SOT223	m39[42C6]
Q4400	TRA_SINGLE_MOSFET_NC_HN_SOT23	m39[44A7]
Q5900	TRA_FDV301N_SOT23-LF	m39[59D7]
Q5901	TRA_2N7002DW_SOT-363	m39[59C7 59C7]
Q5902	TRA_2N7002DW_SOT-363	m39[59B1 59B2]
Q5903	TRA_DUAL_MMDT3904_SO-T-363-LF	m39[59A2 59A1]
Q5910	TRA_SINGLE_MOSFET_PC_HN_SOT-23	m39[59A4]
Q5911	TRA_2N7002_SOT23-LF	m39[59A4]
Q6500	TRA_NTHS5443T1_1206A-03-LF	m39[65D4]
Q6502	TRA_2N7002DW_SOT-363	m39[65D8 65D6]
Q6503	TRA_NTHS5443T1_1206A-03-LF	m39[65B4]
Q6505	TRA_2N7002DW_SOT-363	m39[65C8 65B6]
Q6600	TRA_NTHS5443T1_1206A-03-LF	m39[66D4]
Q6602	TRA_2N7002DW_SOT-363	m39[66D8 66C5]
Q7200	TRA_2N7002DW_SOT-363	m39[72B6 72B7]
Q7400	TRA_2N7002DW_SOT-363	m39[74B3 74B3]
Q7401	TRA_2N7002_SOT23-LF	m39[74C3]
Q7402	TRA_2N7002DW_SOT-363	m39[74B2 74B2]
Q7500	TRA_HAT2168H_LFPAK	m39[75D3]
Q7501	TRA_HAT2165H_LFPAK	m39[75D3]
Q7502	TRA_HAT2168H_LFPAK	m39[75C3]
Q7503	TRA_HAT2165H_LFPAK	m39[75B3]
Q7504	TRA_HAT2165H_LFPAK	m39[75D3]
Q7505	TRA_HAT2165H_LFPAK	m39[75B3]
Q7570	TRA_HAT2168H_LFPAK	m39[75D2]
Q7572	TRA_HAT2168H_LFPAK	m39[75C3]
Q7639	TRA_2N7002_SOT23-LF	m39[76A7]
Q7640	TRA_SINGLE_MOSFET_PC_HN_SOT-23	m39[76A6]
Q7641	TRA_FDC796N_SUPERSOT-6	m39[76A5]
Q7642	TRA_FDC796N_SUPERSOT-6	m39[76A4]
Q7701	TRA_SI3446DV_TSOP-LF	m39[77A3]
Q7703	TRA_2N7002DW_SOT-363	m39[77C7 77D7]
Q7799	TRA_2N7002_SOT23-LF	m39[77A6]
Q7800	TRA_NTD60N02R_CASE36-9-LF	m39[78C4]
Q7801	TRA_NTD60N02R_CASE36-9-LF	m39[78B4]
Q7802	TRA_2N7002_SOT23-LF	m39[78B7]
Q7900	TRA_NTD60N02R_CASE36-9-LF	m39[79D4]
Q7901	TRA_NTD60N02R_CASE36-9-LF	m39[79C4]
Q7902	TRA_2N7002_SOT23-LF	m39[79C7]
Q8000	TRA_NTD60N02R_CASE36-9-LF	m39[80D4]
Q8001	TRA_NTD60N02R_CASE36-9-LF	m39[80C4]
Q8003	TRA_2N7002_SOT23-LF	m39[80C7]
Q8102	TRA_NTD60N02R_CASE36-9-LF	m39[81D4]
Q8103	TRA_NTD60N02R_CASE36-9-LF	m39[81C4]
Q8104	TRA_2N7002_SOT23-LF	m39[81C7]
Q8300	TRA_IRF7413_SO-8	m39[83C4]

Q8301	TRA_IRF7413_SO-8	m39[83B4]
Q8302	TRA_2N7002DW_SOT-363	m39[83B5]
Q8303	TRA_2N7002DW_SOT-363	m39[83C5]
Q8520	TRA_HAT2168H_LFPAK	m39[85D4]
Q8521	TRA_HAT2165H_LFPAK	m39[85C4]
Q8522	TRA_HAT2165H_LFPAK	m39[85C5]
Q8523	TRA_2N7002DW_SOT-363	m39[85B3 85B2]
Q8554	TRA_2N7002_SOT23-LF	m39[85A8]
Q8570	TRA_2N7002_SOT23-LF	m39[85A5]
Q8575	TRA_FDC796N_SUPERSOT -6	m39[85B6]
Q8576	TRA_FDC796N_SUPERSOT -6	m39[85A2]
Q9400	TRA_SI3443DV_TSOP-LF	m39[94C7]
Q9401	TRA_2N7002_SOT23-LF	m39[94C7]
Q9711	TRA_2N7002DW_SOT-363	m39[97D2 97C2]
R75A0	RES_402	m39[75C7]
R85A0	RES_402	m39[85D1]
R600	RES_603	m39[6A7]
R601	RES_402	m39[6D8]
R602	RES_603	m39[6A8]
R603	RES_402	m39[6B1]
R605	RES_603	m39[6A7]
R611	RES_402	m39[6B7]
R612	RES_402	m39[6B7]
R614	RES_402	m39[6B7]
R615	RES_402	m39[6B7]
R616	RES_402	m39[6A7]
R617	RES_402	m39[6A7]
R618	RES_402	m39[6C7]
R619	RES_402	m39[6B7]
R0702	RES_402	m39[7D6]
R0703	RES_402	m39[7C6]
R0704	RES_402	m39[7C5]
R0705	RES_402	m39[7B4]
R0706	RES_402	m39[7B5]
R0707	RES_402	m39[7A4]
R0712	RES_402	m39[7A3]
R0716	RES_402	m39[7B1]
R0717	RES_402	m39[7B1]
R0718	RES_402	m39[7B1]
R0719	RES_402	m39[7B1]
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R0721	RES_402	m39[7B7]
R0722	RES_402	m39[7A7]
R0730	RES_402	m39[7A4]
R0802	RES_402	m39[8B7]
R0803	RES_402	m39[8A7]
R1000	RES_402	m39[10D3]
R1001	RES_402	m39[10D3]
R1002	RES_402	m39[10C6]
R1005	RES_402	m39[10D3]
R1017	RES_402	m39[10C6]
R1018	RES_402	m39[10B6]
R1019	RES_402	m39[10B6]
R1100	RES_402	m39[11B5]
R1101	RES_402	m39[11C5]
R1102	RES_402	m39[11B4]
R1103	RES_402	m39[11C5]
R1104	RES_402	m39[11B5]
R1106	RES_402	m39[11A3]
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R1211	RES_402	m39[12C3]
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R1226	RES_402	m39[12B7]
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R1231	RES_402	m39[12A7]
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R1236	RES_402	m39[12A7]
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R1441	RES_402	m39[14D6]
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R1980	RES_402	m39[19B7]
R1981	RES_402	m39[19B7]
R1982	RES_402	m39[19B8]
R1983	RES_402	m39[19B8]
R2058	RES_402	m39[20B4]
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R2060	RES_402	m39[20A4]
R2075	RES_402	m39[20C7]
R2077	RES_402	m39[20B7]
R2079	RES_402	m39[20B7]
R2085	RES_402	m39[20C4]
R2100	RES_402	m39[21C3]
R2101	RES_402	m39[21C4]
R2105	RES_402	m39[21D6]
R2107	RES_402	m39[21C2]
R2108	RES_402	m39[21C2]
R2110	RES_402	m39[21C2]
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R2203	RES_402	m39[22C2]
R2204	RES_402	m39[22C2]
R2205	RES_402	m39[22C6]
R2206	RES_402	m39[22C5]
R2207	RES_402	m39[22C5]
R2211	RES_402	m39[22B3]
R2222	RES_402	m39[22D6]
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R2225	RES_402	m39[22D7]
R2226	RES_402	m39[22D5]
R2250	RES_402	m39[22D7]
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R2252	RES_402	m39[47B8]
R2253	RES_402	m39[47B8]
R2254	RES_402	m39[47B8]
R2255	RES_402	m39[22D7]
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R2299	RES_402	m39[22B5]
R2302	RES_402	m39[23D3]
R2303	RES_402	m39[23D3]
R2305	RES_402	m39[23D3]
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R2326	RES_402	m39[23D6]
R2327	RES_402	m39[23D6]
R2343	RES_402	m39[23D1]
R2388	RES_402	m39[23A3]
R2389	RES_402	m39[38D5]
R2390	RES_402	m39[23B3]
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R2396	RES_402	m39[23D6]
R2397	RES_402	m39[23D6]
R2398	RES_402	m39[23D8]
R2399	RES_402	m39[23C1]
R2500	RES_603	m39[25A8]
R2501	RES_402	m39[25C8]
R2502	RES_402	m39[25D8]
R2600	RES_402	m39[26C7]
R2606	RES_402	m39[26C7]
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R2643	RES_402	m39[26C2]
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R2696	RES_402	m39[26B4]
R2697	RES_402	m39[26C3]
R2698	RES_402	m39[26C5]
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R2718	RES_402	m39[27B7]
R2719	RES_402	m39[27B7]
R2800	RES_402	m39[28C7]
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R3025	RES_402	m39[30C4]
R3035	RES_402	m39[30B4]
R3100	RES_402	m39[31C5]
R3101	RES_402	m39[31C5]
R3300	RES_402	m39[33B6]
R3301	RES_402	m39[33B7]
R3302	RES_402	m39[33D4]
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R3304	RES_402	m39[33C7]
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R3403	RES_402	m39[34C5]
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R4119	RES_402	m39[41B2]
R4120	RES_402	m39[41B2]
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R4123	RES_402	m39[41A2]
R4130	RES_402	m39[41C4]
R4131	RES_402	m39[41C4]
R4150	RES_402	m39[41C8]
R4151	RES_402	m39[41D7]
R4200	RES_402	m39[42D2]
R4201	RES_402	m39[42C2]
R4202	RES_402	m39[42D6]
R4300	RES_402	m39[43D7]
R4301	RES_603	m39[43D2]
R4302	RES_603	m39[43D2]
R4303	RES_603	m39[43D1]
R4304	RES_603	m39[43D1]
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R4723	RES_402	m39[47B6]
R4732	RES_402	m39[47A6]
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R4735	RES_805	m39[47C6]
R4736	RES_805	m39[47D6]
R4742	RES_402	m39[47C2]
R4743	RES_402	m39[47C2]
R4746	RES_805	m39[47D2]
R4754	RES_402	m39[47C2]
R4755	RES_402	m39[47B2]
R5300	RES_402	m39[53C3]
R5301	RES_402	m39[53B3]
R5302	RES_402	m39[53B4]
R5303	RES_402	m39[53B4]
R5304	RES_402	m39[53C6]
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R5802	RES_402	m39[58C2]
R5803	RES_402	m39[58C2]
R5808	RES_402	m39[59C3]
R5809	RES_402	m39[58C2]
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R5912	RES_402	m39[59D2]
R5913	RES_402	m39[59D2]
R5914	RES_402	m39[59C2]
R5915	RES_402	m39[59C2]
R5916	RES_402	m39[59C2]
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R5919	RES_402	m39[59B4]
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R5942	RES_402	m39[59A4]
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R6103	RES_402	m39[61C6]
R6104	RES_402	m39[61B6]
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R6307	RES_402	m39[63C5]
R6309	RES_402	m39[63C5]
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R6501	RES_402	m39[65A7]
R6502	RES_1206	m39[65D6]
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R6511	RES_402	m39[65B6]
R6512	RES_805	m39[65C5]
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R6514	RES_805	m39[65B4]
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R6599	RES_402	m39[65C7]
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R7218	RES_402	m39[72A5]
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R7415	RES_805	m39[74B8]
R7416	RES_805	m39[74C7]
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R7430	RES_402	m39[74C1]
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R8599	RES_1206	m39[85C4]
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R9048	RES_402	m39[90A7]
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R9081	RES_402	m39[90C4]
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R9742	RES_402	m39[97A7]
R9750	RES_402	m39[97A3]
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RP3000	RPAK4P_SM-LF	m39[30B4 30C4 30D4 30D4]
RP3001	RPAK4P_SM-LF	m39[30C4 30A4 30A4 30D4]
RP3002	RPAK4P_SM-LF	m39[30A4 30A4 30A4 30D4]
RP3003	RPAK4P_SM-LF	m39[30C4 30C4 30C4 30D4]
RP3004	RPAK4P_SM-LF	m39[30C4 30C4 30D4]
RP3005	RPAK4P_SM-LF	m39[30B4 30A4 30A4 30D4]
RP3006	RPAK4P_SM-LF	m39[30B4 30B4 30A4 30D4]
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RP3008	RPAK4P_SM-LF	m39[30C4 30C4 30C4 30C4]
RP3009	RPAK4P_SM-LF	m39[30B4 30B4 30C4 30C4]
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RP3011	RPAK4P_SM-LF	m39[30B4 30A4 30B4 30B4]
RP7200	RPAK4P_SM-LF	m39[72A4]
SDF3800	PCB_STANDOFF	m39[38B2]
SDF3801	PCB_STANDOFF	m39[38A2]
SDF4700	PCB_STANDOFF	m39[47A2]
SDF4701	PCB_STANDOFF	m39[47A2]
SDF5300	PCB_STANDOFF	m39[53A5]
SDF5301	PCB_STANDOFF	m39[53A5]
SDF9400	PCB_STANDOFF	m39[94B6]
SDF9401	PCB_STANDOFF	m39[94A6]
SW2600	SWI_TACT_4SM_EVQPH_S M-LF	m39[26C6]
SW5900	SWI_TACT_4SM_EVQPH_S M-LF	m39[59D8]
SW5901	SWI_TACT_4SM_EVQPH_S M-LF	m39[59B8]
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U601	SN74LVC1G04_SOT23-5	m39[6C7]
U1000	ADT7461_MSOP	m39[10D5]
U1200	NB_945GM_BGA	m39[12D5]
U1200	NB_945GM_BGA	m39[13D4]
U1200	NB_945GM_BGA	m39[14D5]
U1200	NB_945GM_BGA	m39[15D3 15D7]
U1200	NB_945GM_BGA	m39[16D2 16C8]
U1200	NB_945GM_BGA	m39[17D5]
U1200	NB_945GM_BGA	m39[18D4 18D7]
U2100	SB_ICH7M_BGA	m39[21D6]
U2100	SB_ICH7M_BGA	m39[22B7 22D3]
U2100	SB_ICH7M_BGA	m39[23D4]
U2100	SB_ICH7M_BGA	m39[24D4 24D7]
U2601	MC74VHC1G08_SOT23-5-LF	m39[26D5]
U2603	SN74LVC1G04_SOT23-5	m39[26A7]
U2698	MC74VHC1G08_SOT23-5-LF	m39[26C4]
U2699	MAX6816_SOT143	m39[26C5]
U3100	LREG_BD3533FVM_MSOP-8	m39[31C5]
U3301	CLK_GEN_CY284455_QFN	m39[33C5]
U4101	88E8053_QFN	m39[41D5]
U4102	EEPROM_M24C08_SO8	m39[41A3]
U4400	FW32306_TQFP	m39[44D5]
U4700	SWI_TPS2024_SOI	m39[47C8]
U5800	SMC_H8S2116_BGA	m39[58A8 58C3 58C6 58D6]
U5900	VDET_RN5VD_SOT23-5	m39[59D8]
U5940	VREF_REF3133_SOT23-3	m39[59A4]
U5999	COMPARATOR_LMV339_TS SOP	m39[59A6 59A6 59A8 59A8]
U6100	MAX6695_UMAX	m39[61C4]
U6301	FLASH_SST25VF016B_SOI	m39[63D3]
U6700	TPM_TSSOP	m39[67C5]
U6800	AUDIO_STAC9220_LQFP	m39[68D5]
U7200	MAX9714_QFN-LF	m39[72C5]
U7500	ISL6262_QFN	m39[75C6]
U7501	INA138_SOT23-5-LF	m39[76D7]
U7600	OPAMP_LMV2011_SOT23-5	m39[76D3]
U7700	LTC3411_MSOP-LF	m39[77D5]
U7710	MC74VHC1G08_SOT23-5-LF	m39[77C7]
U7711	MC74VHC1G08_SOT23-5-LF	m39[77B7]
U7712	MC74VHC1G08_SOT23-5-LF	m39[77B7]
U7750	LTC3412_TSSOP-LF	m39[77B5]
U7800	ISL6549_QFN	m39[78C6]
U7900	ISL6549_QFN	m39[79D6]
U7901	COMPARATOR_LM339A_SO I-LF	m39[79A5]
U7901	COMPARATOR_LM339A_SO I-LF	m39[80A4]
U7901	COMPARATOR_LM339A_SO I-LF	m39[81A5]
U7910	COMPARATOR_LM339A_SO I-LF	m39[79A3 79B3]
U7910	COMPARATOR_LM339A_SO I-LF	m39[80B2]
U7910	COMPARATOR_LM339A_SO I-LF	m39[81B3]
U8000	ISL6549_QFN	m39[80D6]
U8100	ISL6549_QFN	m39[81D6]
U8400	ATI_M56P_BGA	m39[84C8 84D4]
U8400	ATI_M56P_BGA	m39[86D4]
U8400	ATI_M56P_BGA	m39[87D2 87D6]
U8400	ATI_M56P_BGA	m39[91D4]
U8400	ATI_M56P_BGA	m39[93C4]
U8500	ISL6269_QFN	m39[85D6]
U8550	FAN2558_SOT23-6-LF	m39[85B7]
U8560	74LVC1G125LF_SOT23-5	m39[85A6]
U8580	LT3483_TSOT23-6	m39[85A4]
U8595	OPAMP_LMV2011_SOT23-5	m39[85D2]
U8900	SGRAM_16MX32_GDDR3_1 36H_FBGA	m39[89D6 89B6]
U8950	SGRAM_16MX32_GDDR3_1 36H_FBGA	m39[89D3 89B3]
U9000	SGRAM_16MX32_GDDR3_1 36_FBGA	m39[90D6 90B6]
U9050	SGRAM_16MX32_GDDR3_1 36_FBGA	m39[90D3 90B3]
U9470	MC74VHC1G08_SOT23-5-LF	m39[94B2]
U9750	74AHC1G32_SM-LF	m39[97A4]
U9751	74AHC1G32_SM-LF	m39[97A4]
VR6800	LREG_TPS79501_SOT223 -6	m39[68A4]
XC7200	MTGHOLE	m39[72B3]
XW601	SHORT_SM	m39[6C2]
XW602	SHORT_SM	m39[6C2]
XW604	SHORT_SM	m39[6A5]
XW605	SHORT_SM	m39[6A5]
XW5800	SHORT_SM	m39[58B3]
XW5900	SHORT_SM	m39[59B1]
XW6800	SHORT_SM	m39[74A4]
XW7201	SHORT_SM	m39[72B2]
XW7300	SHORT_SM	m39[73C5]
XW7400	SHORT_SM	m39[74D2]
XW7500	SHORT_SM	m39[75A6]
XW7501	SHORT_SM	m39[75B2]
XW7502	SHORT_SM	m39[75B1]
XW7503	SHORT_SM	m39[75D2]
XW7504	SHORT_SM	m39[75D1]
XW7598	SHORT_SM	m39[76D7]
XW7700	SHORT_SM	m39[77C4]
XW7750	SHORT_SM	m39[77A5]
XW7800	SHORT_SM	m39[78B6]
XW7900	SHORT_SM	m39[79C6]
XW8000	SHORT_SM	m39[80C6]
XW8100	SHORT_SM	m39[81C6]
XW8500	SHORT_SM	m39[85C6]
XW8715	SHORT_SM	m39[87A7]
XW8725	SHORT_SM	m39[87A4]
XW9135	SHORT_SM	m39[91A4]
XW9140	SHORT_SM	m39[91A4]
XW9300	SHORT_SM	m39[93C7]
XW9305	SHORT_SM	m39[93C7]
XW9310	SHORT_SM	m39[93C7]
XW9314	SHORT_SM	m39[93C7]
XW9320	SHORT_SM	m39[93B7]
XW9324	SHORT_SM	m39[93B7]

XW9330	SHORT_SM	m39[93B7]
XW9345	SHORT_SM	m39[93A7]
Y2600	CRYSTAL_4PIN_SM-LF	m39[26D8]
Y3301	CRYSTAL_5X3.2-SM	m39[33C7]
Y4101	CRYSTAL_4PIN_SM-3	m39[41B5]
Y4400	CRYSTAL_HC49-USMD	m39[44D2]
Y5800	CRYSTAL_SM-3	m39[59B8]
Y6700	CRYSTAL_4PIN_SM-LF	m39[59B7]
ZH500	HOLE_VIA	m39[5C1]
ZH501	HOLE_VIA	m39[5C1]
ZH502	HOLE_VIA	m39[5C1]
ZH503	HOLE_VIA	m39[5C1]
ZH504	HOLE_VIA	m39[5B1]
ZH505	HOLE_VIA	m39[5B1]
ZH506	HOLE_VIA	m39[5B1]
ZH507	HOLE_VIA	m39[5B1]
ZH508	HOLE_VIA	m39[5B1]
ZH509	HOLE_VIA	m39[5B1]
ZH510	HOLE_VIA	m39[5C1]
ZH511	HOLE_VIA	m39[5C1]
ZH512	HOLE_VIA	m39[5C1]
ZH513	HOLE_VIA	m39[5C1]
ZH514	HOLE_VIA	m39[5B1]
ZH515	HOLE_VIA	m39[5B1]
ZH516	HOLE_VIA	m39[5B1]
ZH517	HOLE_VIA	m39[5B1]
ZH518	HOLE_VIA	m39[5B1]
ZH519	HOLE_VIA	m39[5B1]
ZH520	HOLE_VIA	m39[5C1]
ZH521	HOLE_VIA	m39[5C1]
ZH522	HOLE_VIA	m39[5C1]
ZH523	HOLE_VIA	m39[5C1]
ZH524	HOLE_VIA	m39[5B1]
ZH525	HOLE_VIA	m39[5B1]
ZH526	HOLE_VIA	m39[5B1]
ZH527	HOLE_VIA	m39[5B1]
ZH528	HOLE_VIA	m39[5B1]
ZH529	HOLE_VIA	m39[5B1]
ZH601	MTGHOLE	m39[6A3]
ZH602	MTGHOLE	m39[6A3]
ZH603	MTGHOLE	m39[6A3]
ZH606	MTGHOLE	m39[6A1]
ZH607	MTGHOLE	m39[9D4]
ZH608	MTGHOLE	m39[9D3]
ZH609	MTGHOLE	m39[9D2]
ZH610	MTGHOLE	m39[9D2]