

M39 - DVT

12/07/05

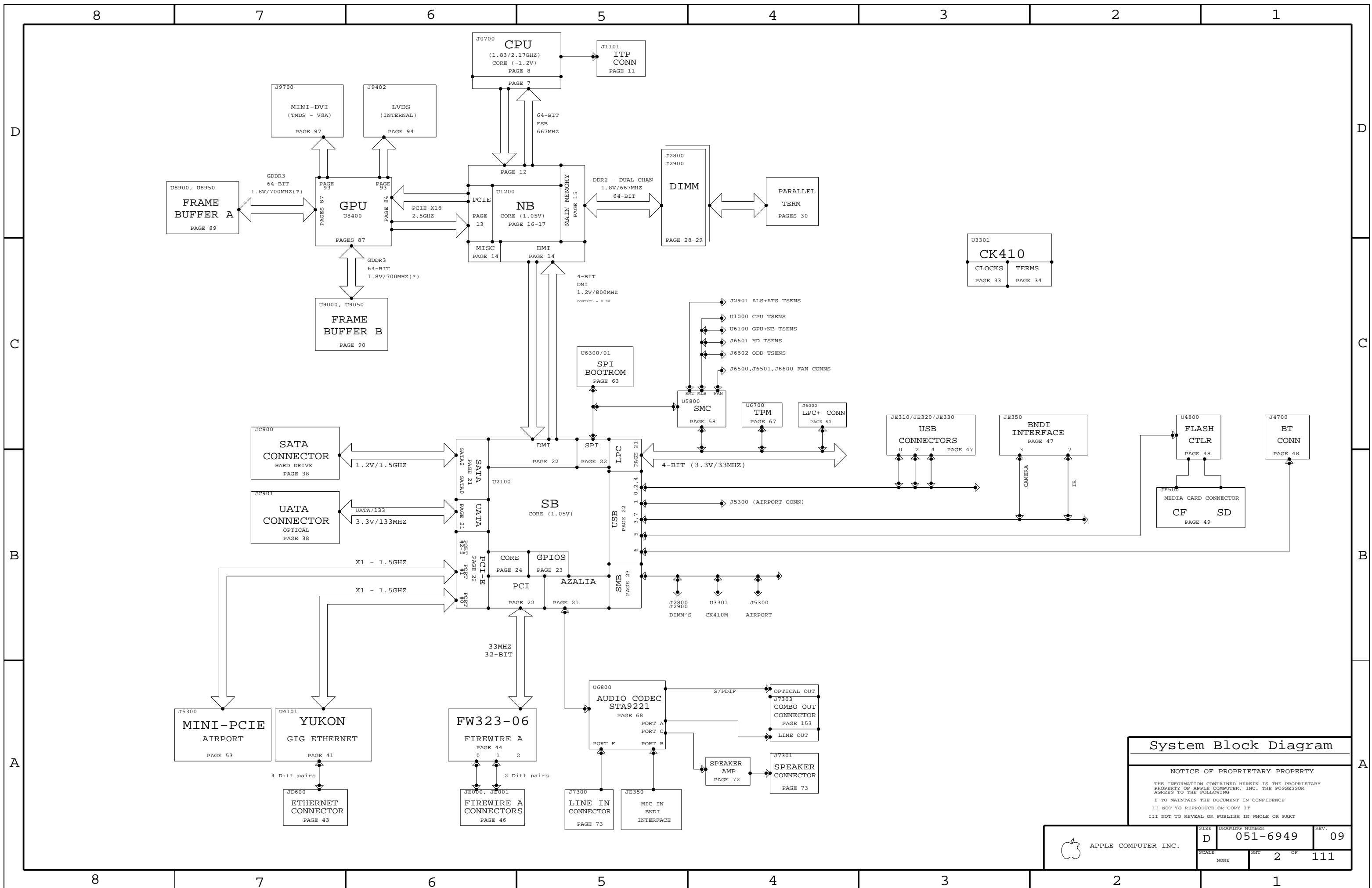
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| REV | ZONE | ECN | DESCRIPTION OF CHANGE | CK APPD | ENG APPD |
|-----|------|--------|-----------------------|----------|----------|
| | | | | DATE | DATE |
| 06 | | 400374 | ENGINEERING RELEASED | 09/16/05 | 06/22/04 |

| PAGE | DRI | PDF | CIRCUIT |
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| 9 | MS | JD | 9 CPU - DECAPS |
| (M42) 10 | MS | JD | 10 CPU - THERMAL SENSOR |
| M42 11 | MS | JD | 11 CPU - ITP CONN |
| M1 12 | PS | JH | 12 NB - CPU INTERFACE |
| M1 13 | PS | JH | 13 NB - VIDEO INTERFACE |
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| M1 15 | PS | JH | 15 NB - DDR2 INTERFACE |
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| M1 17 | PS | JH | 17 NB - POWER 2 |
| M1 18 | PS | JH | 18 NB - GROUNDS |
| 19 | PS | JH | 19 NB - DECAPS |
| M1 20 | PS | JH | 20 NB - CONFIG STRAPS |
| 21 | JD | JD | 21 SB - RTC, LAN, AUDIO, ATA, CPU, LPC |
| 22 | JD | JD | 22 SB - PCIE, SPI, USB, DMI, PCI |
| 23 | JD | JD | 23 SB - SMB, GPIO, PM, CLKS |
| 24 | JD | JD | 24 SB - POWERS AND GROUNDS |
| 25 | JD | JD | 25 SB - DECAPS |
| 26 | JD | JD | 26 SB - MISC |
| 27 | JD | JD | 27 SB - SMB BUS CONNECTIONS |
| 28 | PS | JD | 28 DDR2 - SO-DIMM CONN A |
| 29 | PS | JD | 29 DDR2 - SO-DIMM CONN B (REVERSED) |
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| 42 | JD | JD | 42 LAN - YUKON'S PWR, MISC |
| 43 | JD | JD | 43 LAN - CONN |
| 44 | JD | JD | 44 FIREWIRE - FW323-06 |
| 45 | JD | JD | 45 FIREWIRE - DECAPS |
| 46 | JD | JD | 46 FIREWIRE - CONN'S |
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| 49 | JD | JD | 49 USB - FLASH CONN |

| PAGE | DRI | PDF | CIRCUIT |
|-------|-----|-----|-----------------------------------|
| 53 | JD | JD | 43 PCI-E - AIRPORT MINI-PCIE CONN |
| 54 | JD | JD | 44 PCI-E - UNUSED PORTS |
| 58 | MS | MS | 45 SMC - H8S2116 |
| 59 | MS | MS | 46 SMC - SMB BUSSES, MISC |
| 60 | MS | MS | 47 SMC - LPC+ CONN |
| 61 | JH | JH | 48 SMC - GPU/NB THERMAL SENSOR |
| RX 63 | MS | JD | 49 SMC - SPI BOOTROM |
| 65 | MS | MS | 50 SMC - FANS |
| 66 | MS | MS | 51 SMC - FANS |
| 67 | JD | JD | 52 SMC - TPM |
| SO 68 | PT | JD | 53 AUDIO - CODEC, VREG, MIC BIAS |
| SO 72 | PT | JD | 54 AUDIO - INTERNAL SPEAKER AMP |
| SO 73 | PT | JD | 55 AUDIO - I/O CONN'S, EMC |
| SO 74 | PT | JD | 56 AUDIO - DETECT TRANSLATORS |
| RP 75 | RT | RT | 57 VR - CPU CORE |
| RP 76 | RT | RT | 58 VR - CPU I-V SENSE CKT |
| RP 77 | RT | RT | 59 VR - "S0" 1.2V & 2.5V (GRAFIX) |
| RP 78 | RT | RT | 60 VR - "S0" 1.8V |
| RP 79 | RT | RT | 61 VR - "S3" 1.8V |
| RP 80 | RT | RT | 62 VR - "S0" 1.5V |
| RP 81 | RT | RT | 63 VR - "S0" 1.05V |
| RP 83 | RT | RT | 64 VR - "S3" 3.3V AND 5V |
| JH 84 | JH | JH | 65 GPU - M56 PCI-E |
| M1 85 | JH | JH | 66 GPU - VCORE SUPPLY |
| M1 86 | JH | JH | 67 GPU - M56 CORE PWR |
| M1 87 | JH | JH | 68 GPU - M56 FRAME BUFFER |
| M1 88 | JH | JH | 69 GPU - MISC |
| M1 89 | JH | JH | 70 GPU - GDDR SDRAM A |
| M1 90 | JH | JH | 71 GPU - GDDR SDRAM B |
| M1 91 | JH | JH | 72 GPU - M56 GPIO, DVO, MISC |
| M1 92 | JH | JH | 73 GPU - M56 CLOCKS |
| M1 93 | JH | JH | 74 GPU - M56 VIDEO INTERFACES |
| JH 94 | JH | JH | 75 GPU - INTERNAL DISPLAY CONN'S |
| JH 95 | JH | JH | 76 GPU - TP'S |
| JH 96 | JH | JH | 77 GPU - TMDS, INVERTER, EXT VGA |
| JH 97 | JH | JH | 78 GPU - EXTERNAL DISPLAY CONN'S |

| | | | | | | | | | | | | | | | | | | | | |
|--|----------------------|---|-------|-------|----------|----------|-------|-------|---------|----------|-------|-------|---------|-------|------|--|---|-------------------------------------|--------|--|
| <p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center; font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div> | <p>METRIC</p> | <div style="text-align: right;"> <p>Apple Computer Inc.</p> </div> <hr/> <p style="font-size: x-small; text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: x-small; text-align: center;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: x-small; text-align: center;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p style="font-size: x-small; text-align: center;">II NOT TO REPRODUCE OR COPY IT</p> <p style="font-size: x-small; text-align: center;">III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <hr/> <p style="text-align: center; font-weight: bold; font-size: large;">SCHEM, M39</p> <hr/> <p style="text-align: right;">DRAWING NUMBER 051-6950 REV. 06</p> | | | | | | | | | | | | | | | | | | |
| <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 25%;">DRAFTER</td> <td style="width: 25%;">DESIGN CR</td> <td style="width: 25%;">SCALE</td> <td style="width: 25%;">TITLE</td> </tr> <tr> <td>ENG APPD</td> <td>MFG APPD</td> <td>SCALE</td> <td>TITLE</td> </tr> <tr> <td>QA APPD</td> <td>DESIGNER</td> <td>SCALE</td> <td>TITLE</td> </tr> <tr> <td>RELEASE</td> <td>SCALE</td> <td>NONE</td> <td></td> </tr> </table> | DRAFTER | DESIGN CR | SCALE | TITLE | ENG APPD | MFG APPD | SCALE | TITLE | QA APPD | DESIGNER | SCALE | TITLE | RELEASE | SCALE | NONE | | <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">MATERIAL/FINISH NOTED AS APPLICABLE</td> <td style="width: 50%;">SIZE D</td> </tr> </table> | MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D | <p style="margin: 0;">SHT 1 OF 111</p> |
| DRAFTER | DESIGN CR | SCALE | TITLE | | | | | | | | | | | | | | | | | |
| ENG APPD | MFG APPD | SCALE | TITLE | | | | | | | | | | | | | | | | | |
| QA APPD | DESIGNER | SCALE | TITLE | | | | | | | | | | | | | | | | | |
| RELEASE | SCALE | NONE | | | | | | | | | | | | | | | | | | |
| MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D | | | | | | | | | | | | | | | | | | | |



System Block Diagram

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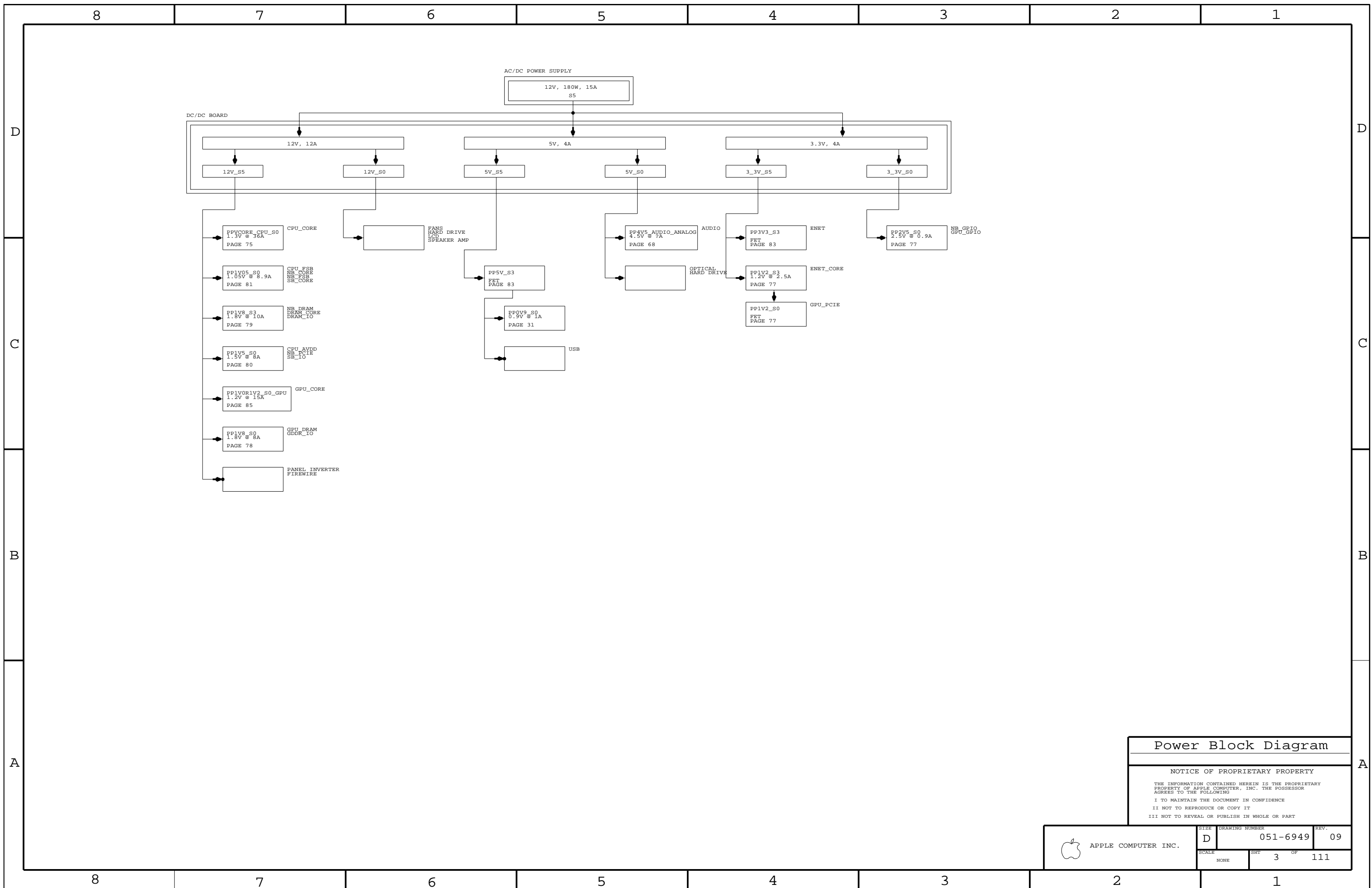
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Power Block Diagram

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COMMON

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---------------------|-----|--|-------------------------|----------|------------|
| 511S0025 | 1 | IC,CPU-SKT,479BGA | J0700 | CRITICAL | |
| 338S0269 | 1 | IC,945GM,NORTHBRIDGE | U1200 | CRITICAL | |
| 343S0385 | 1 | IC,SB,652BGA | U2100 | CRITICAL | |
| 742-0048 | 1 | BAT,COIN,3V,220MAH,CR2032 | BT2600 | CRITICAL | |
| 359S0101 | 1 | IC,CY28445-5,CLK GEN,68PIN QFP | U3301 | CRITICAL | |
| 338S0270 | 1 | IC,888053,GIGABIT EMT XCVR,64P QFN,MD | U4101 | CRITICAL | |
| (335S0382) 341S1797 | 1 | IC,ENET LAN ROM | U4102 | CRITICAL | |
| 338S0279 | 1 | IC,FW32306,1394A LINK,TQFP | U4400 | CRITICAL | |
| 338S0274 | 1 | IC,SMC,HSS/2116,BLANK | U5800 | CRITICAL | |
| 341S1789 | 1 | IC,TPM,TSSOP,28P | U6700 | CRITICAL | LEMENU |
| 353S1235 | 1 | IC,CPU VREG,IMVP,TWO PHASE | U7500 | CRITICAL | |
| 338S0266 | 1 | IC,ATI,M56P,GRAFIX CTLR,880BGA,LF | U8400 | CRITICAL | ATI_B24 |
| 338S0305 | 1 | IC,ATI,M56P,GRAFIX CTLR,880BGA,LF | U8400 | CRITICAL | ATI_A24 |
| 128S0078 | 3 | CAP,EL,AL,330UF,20A,16V,10X12.7MM,SMD,LF | C7517,C7518,C7910 | CRITICAL | |
| 825-6402 | 1 | LBL,SERIAL NUMBER | X14 | CRITICAL | |

M38

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---------------------|-----|------------------------------|-------------------------|----------|-------------|
| 051-6949 | 1 | PCB,SCHEM,MLB,M38 | SCH1 | | 17_INCH_LCD |
| 820-1919 | 1 | PCB,FAB,MLB,M38 | MLB1 | | 17_INCH_LCD |
| (335S0384) 341T0003 | 1 | EFI ROM,M38 | U6301 | CRITICAL | 17_INCH_LCD |
| 114S0287 | 1 | 5.11K,1%,1/16W,402,MF-LF | R8522 | | 17_INCH_LCD |
| 337S3242 | 1 | M00-SPEED CPU (QINZ) | CPU | CRITICAL | CPU_M00 |
| 337S3241 | 1 | M38/M39 LOW-SPEED CPU (QINY) | CPU | CRITICAL | CPU_M38 |

M39

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---------------------|-----|--------------------------|-------------------------|----------|-------------|
| 051-6950 | 1 | PCB,SCHEM,MLB,M39 | SCH1 | | 20_INCH_LCD |
| 820-1888 | 1 | PCB,FAB,MLB,M39 | MLB1 | | 20_INCH_LCD |
| (335S0384) 341T0004 | 1 | EFI ROM,M39 | U6301 | CRITICAL | 20_INCH_LCD |
| 114S0276 | 1 | 4.02K,1%,1/16W,402,MF-LF | R8522 | | 20_INCH_LCD |
| 337S3243 | 1 | M39 HI-SPEED CPU (QHJY) | CPU | CRITICAL | CPU_M39 |

M38 / M39

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-------------------------------------|-------------------------|----------|---------------------|
| 333S0354 | 4 | IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA | U8900,U8950,U9000,U9050 | CRITICAL | ATI_FB_128M_SAMSUNG |
| 333S0358 | 4 | IC,SURAM,GDDR3,8MX32,700MHZ,136FBGA | U8900,U8950,U9000,U9050 | CRITICAL | ATI_FB_128M_HYNIX |

M39 - CTO

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|--------------------------------------|-------------------------|----------|---------------------|
| 333S0350 | 4 | IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA | U8900,U8950,U9000,U9050 | CRITICAL | ATI_FB_256M_SAMSUNG |
| 333S0351 | 4 | IC,SURAM,GDDR3,16MX32,700MHZ,136FBGA | U8900,U8950,U9000,U9050 | CRITICAL | ATI_FB_256M_HYNIX |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|-----------------------------|---------------------------------------|
| 126S0096 | 126S0076 | | C7801 | SANYO W16C680EX 680UF 16V LFP |
| 126S0086 | 126S0078 | | C699,C940,C1900,C1901,C1968 | SANYO W6CE330F8 330UF 6.3V LFP |
| 128S0080 | 128S0078 | | C7517,C7518,C7910 | SANYO 160VP330W 330UF 16V SMD LFP |
| 338S0309 | 338S0266 | | U8400 | IC,ATI,M56LP,GRAFIX CTLR,880PBGA,LF |
| 197S0177 | 197S0020 | | Y4101 | XTAL,25MHZ,50PFM,16PF,3.220+-5 SMD,LF |

124-0338 124-0333 C7501,C8014 CAP,AL,EL,680UF,16V,RAD,10X12.5MM

Table Items

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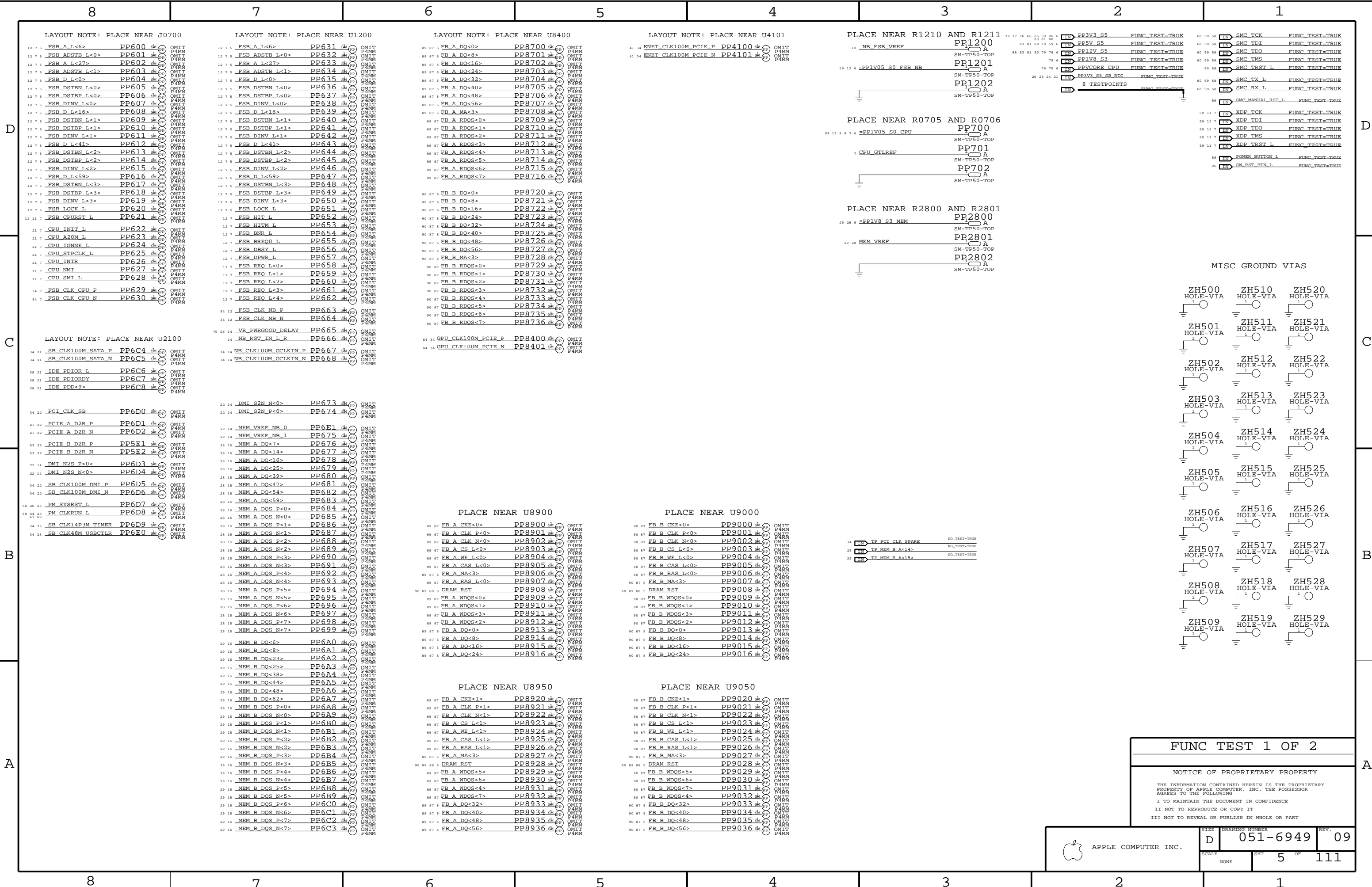
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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

LAYOUT NOTE: PLACE NEAR U8400

LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS

PLACE NEAR U8900

PLACE NEAR U9000

PLACE NEAR U8950

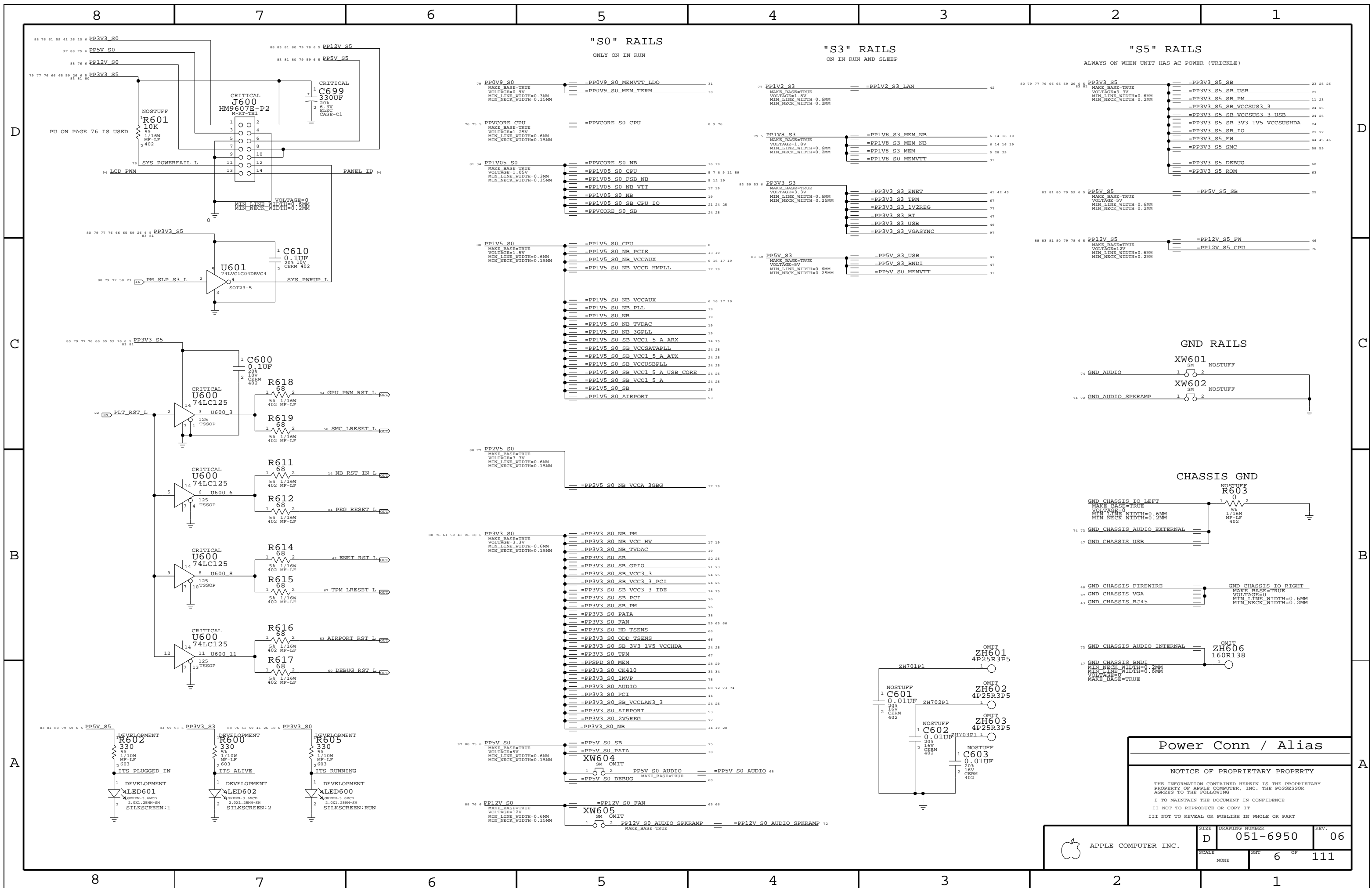
PLACE NEAR U9050

FUNC TEST 1 OF 2

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"S0" RAILS

ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

GND RAILS

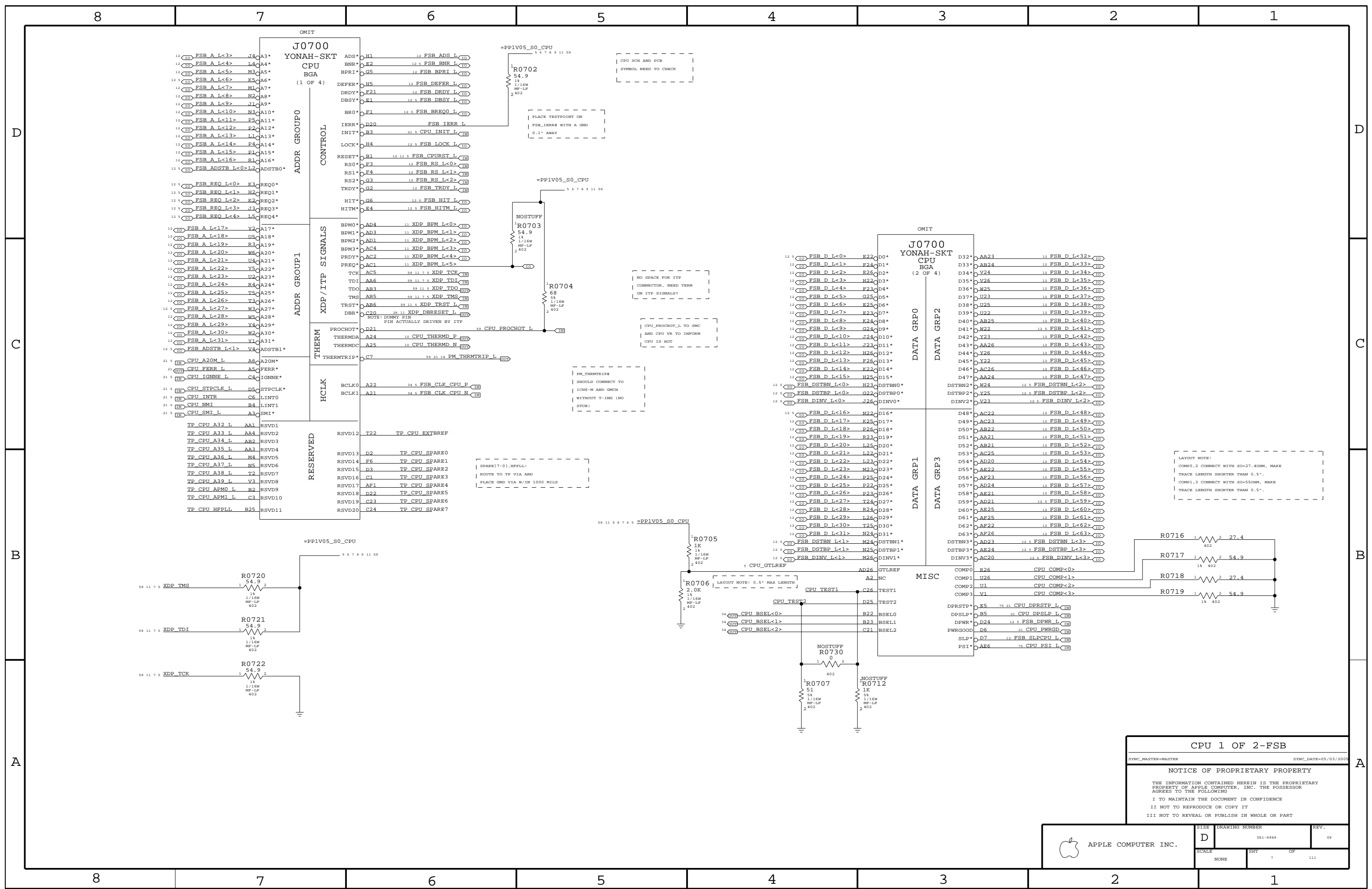
CHASSIS GND

Power Conn / Alias

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CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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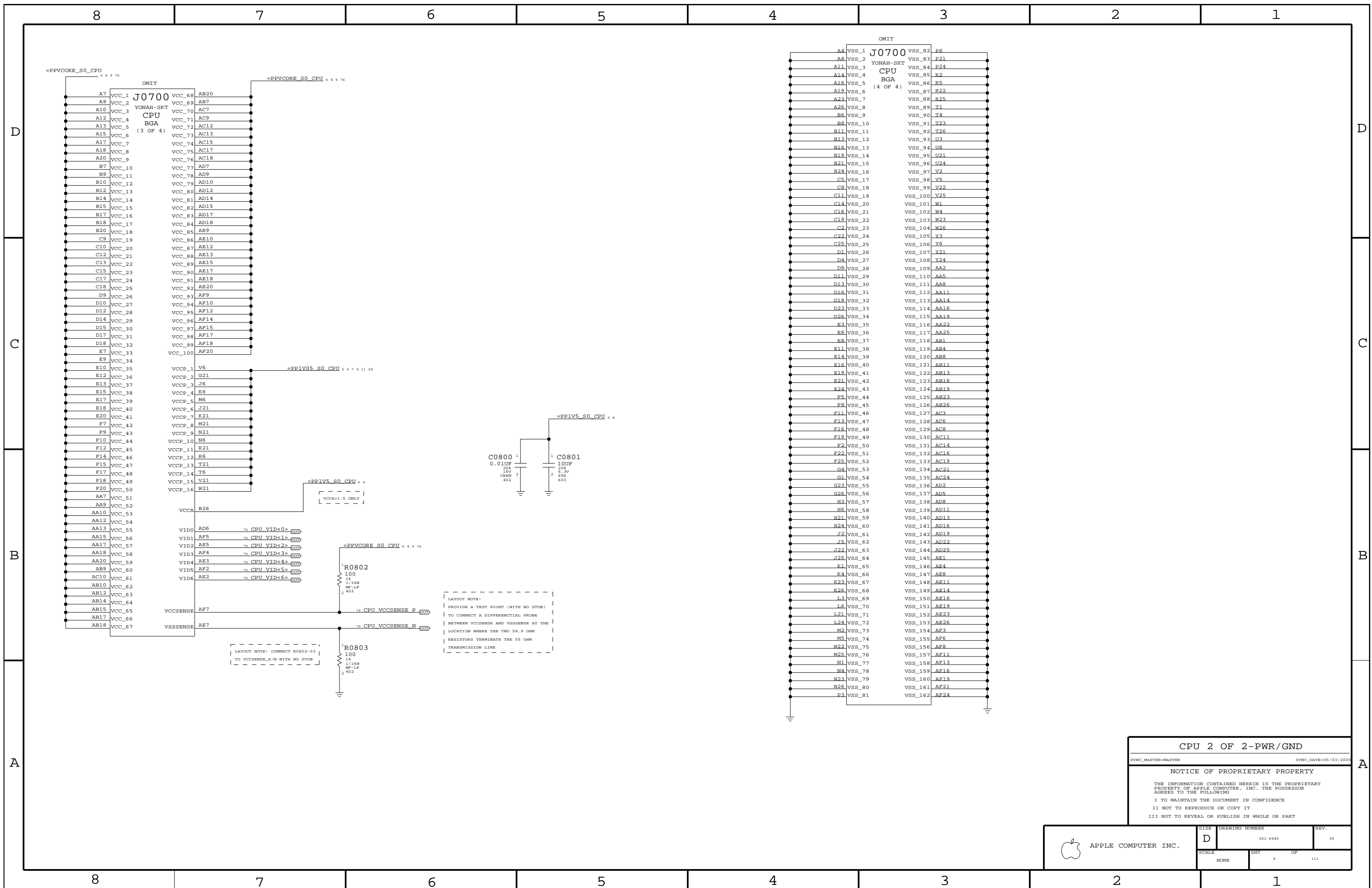
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CPU 2 OF 2-PWR/GND

SYNC_MASTER-MASTER SYNC_DATE=05/03/2005

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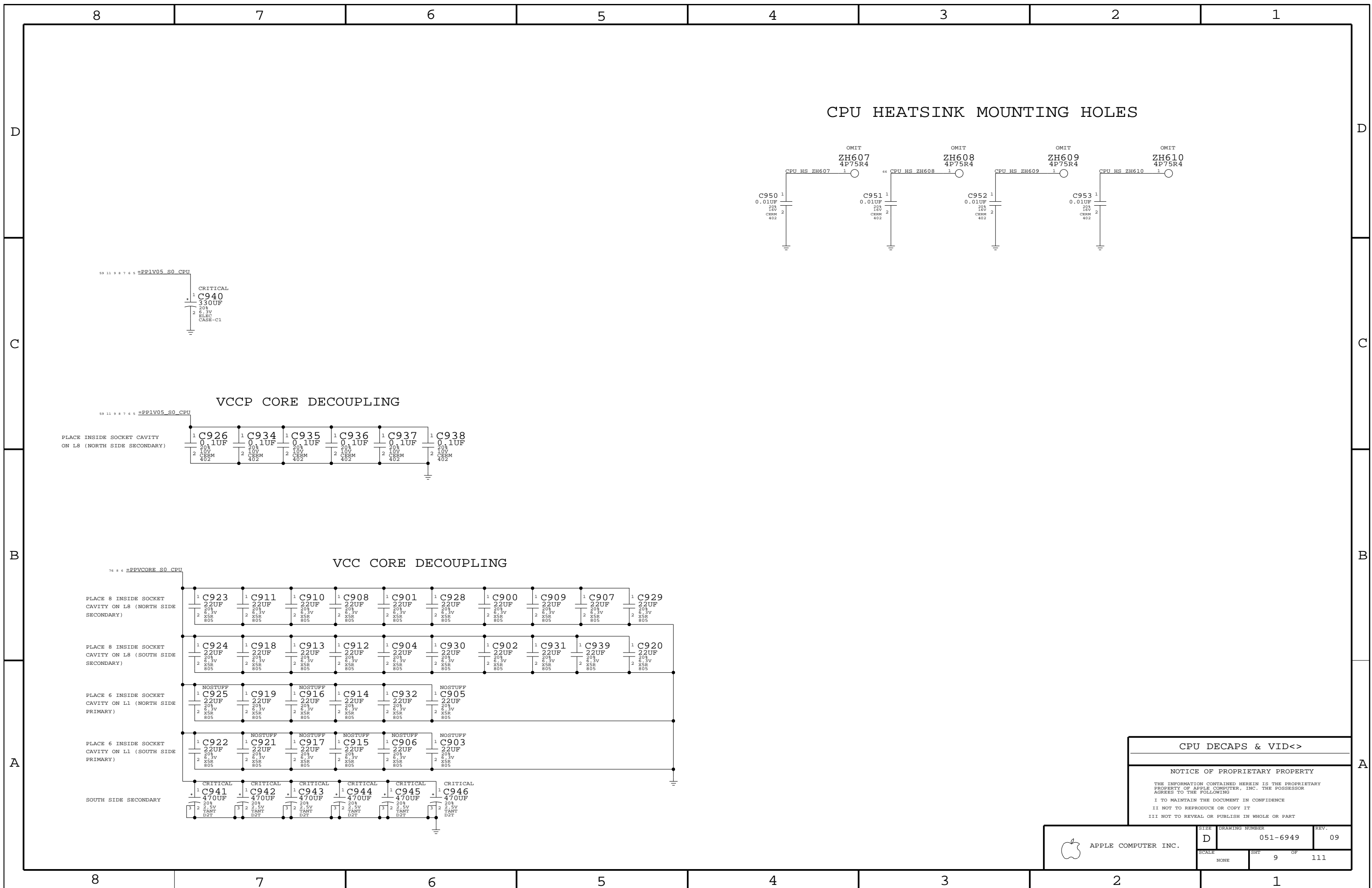
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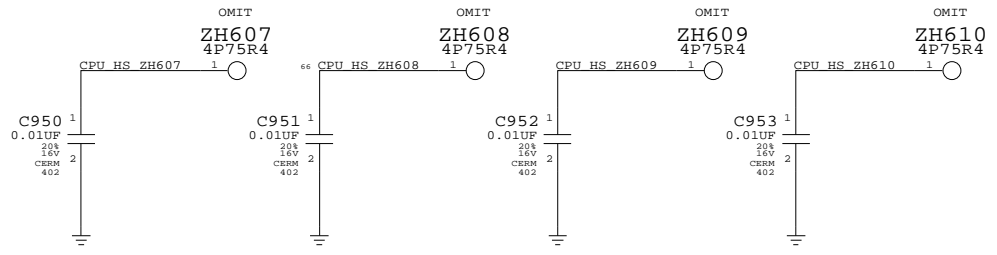
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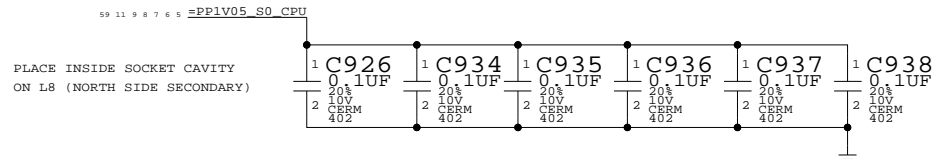
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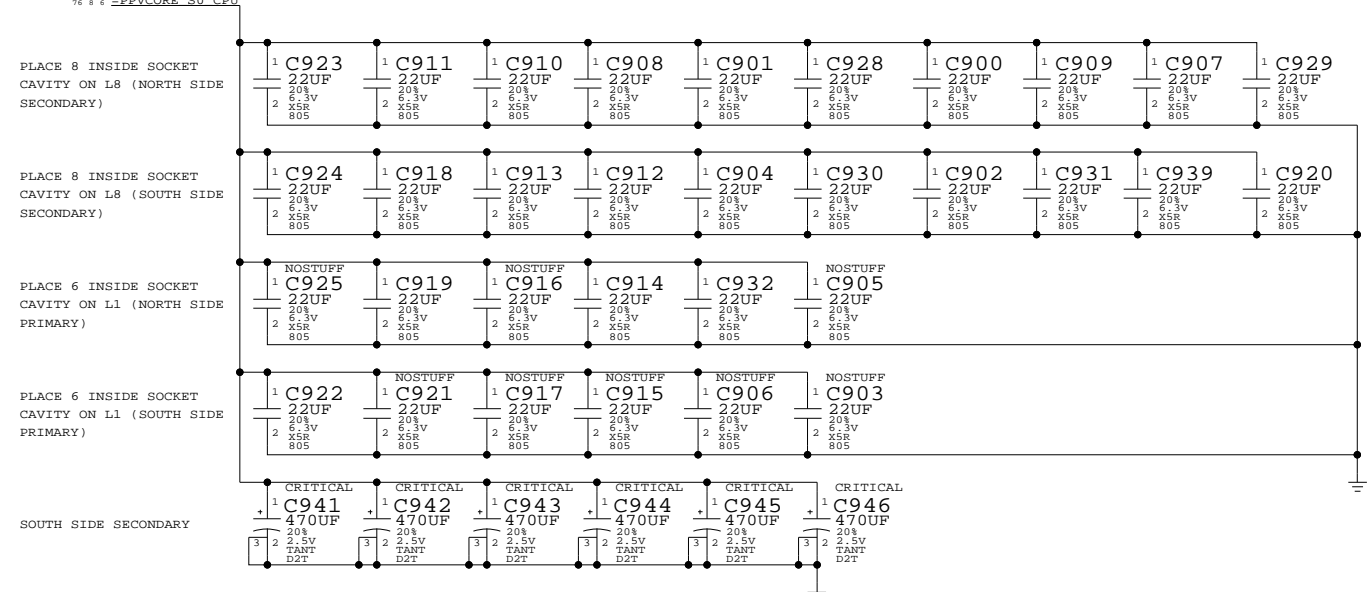
CPU HEATSINK MOUNTING HOLES



VCC CORE DECOUPLING



VCC CORE DECOUPLING



CPU DECAPS & VID<>

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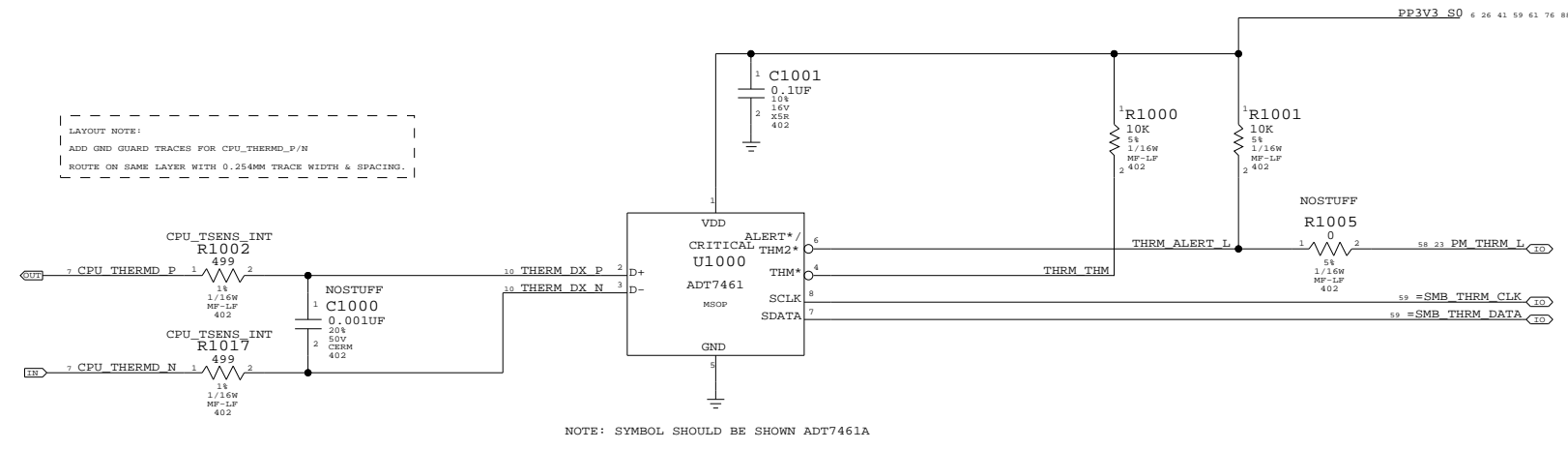
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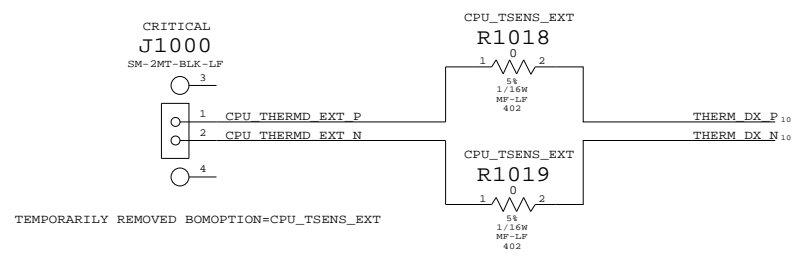
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CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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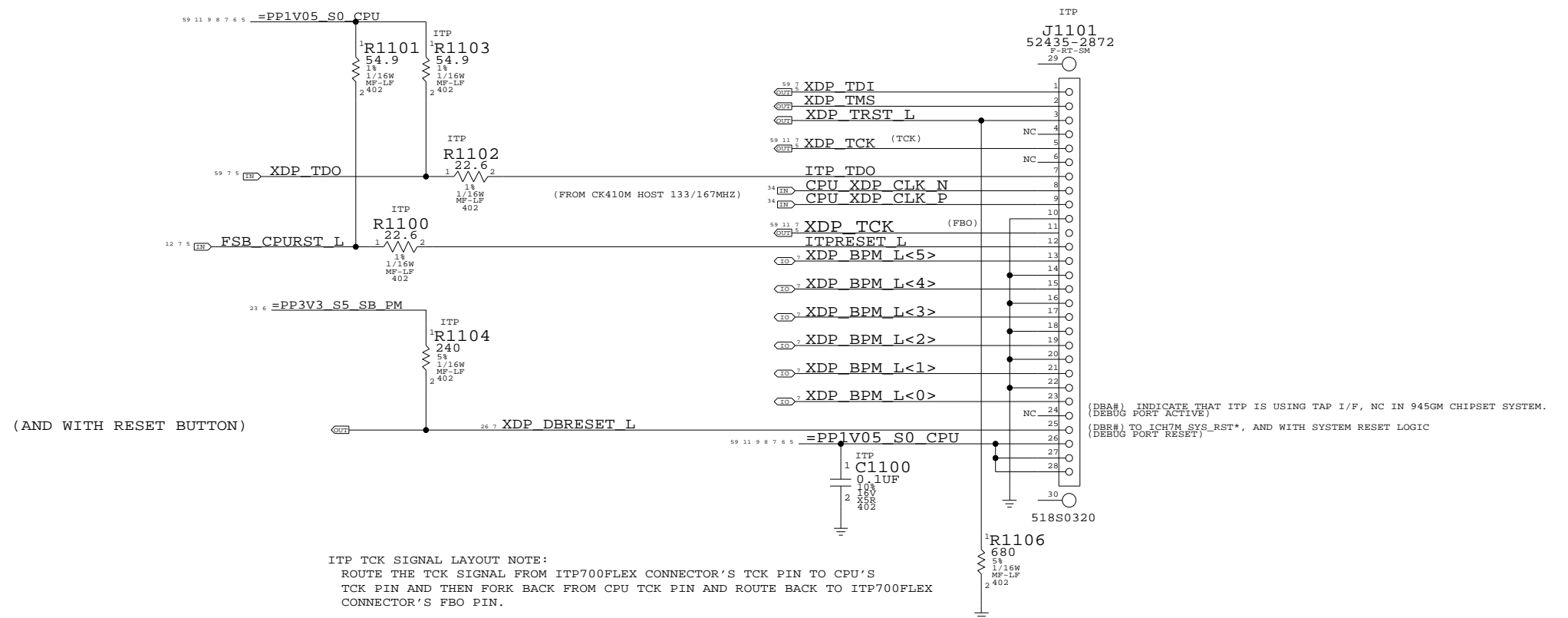
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CPU ITP700FLEX DEBUG SUPPORT



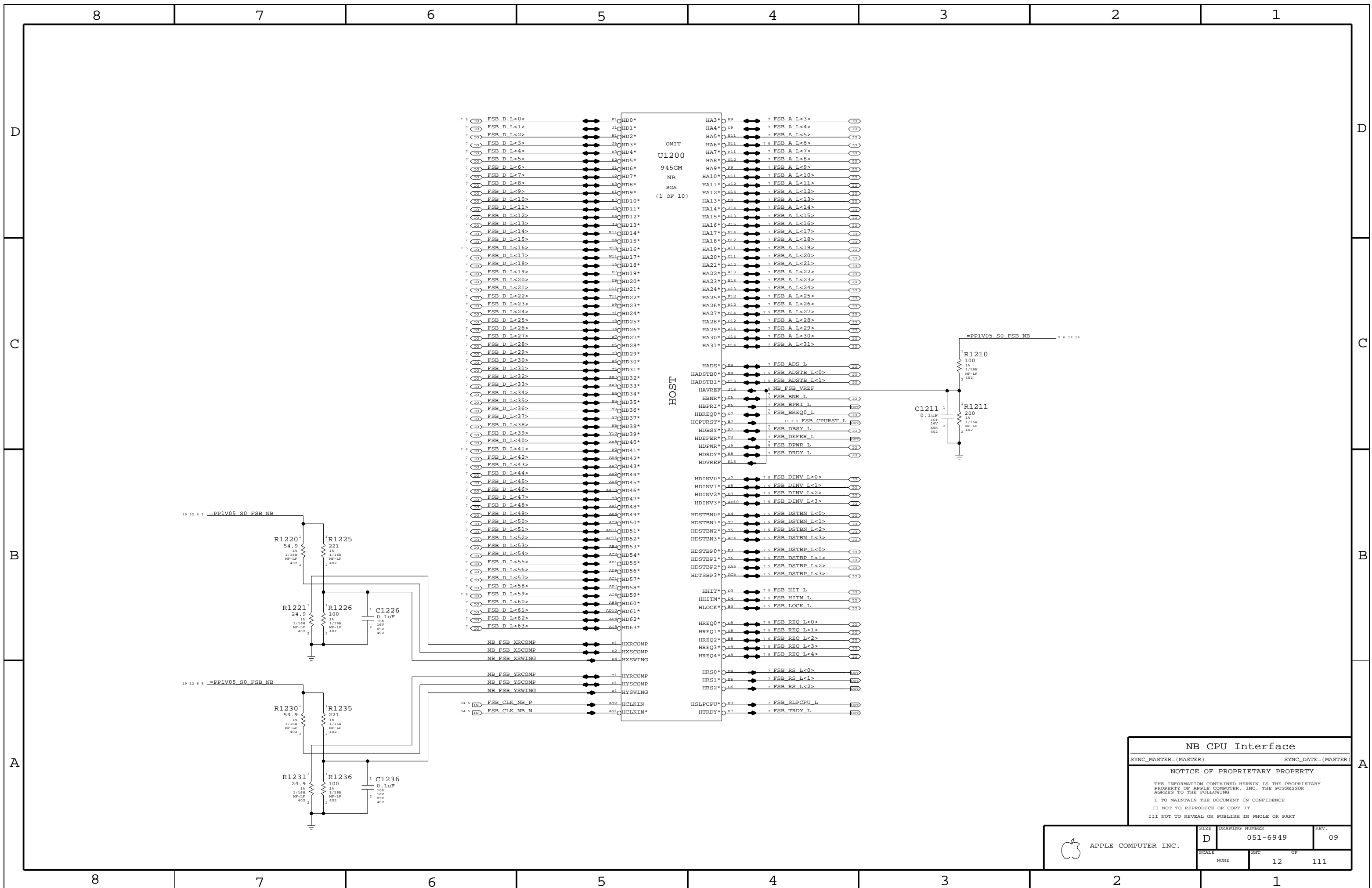
CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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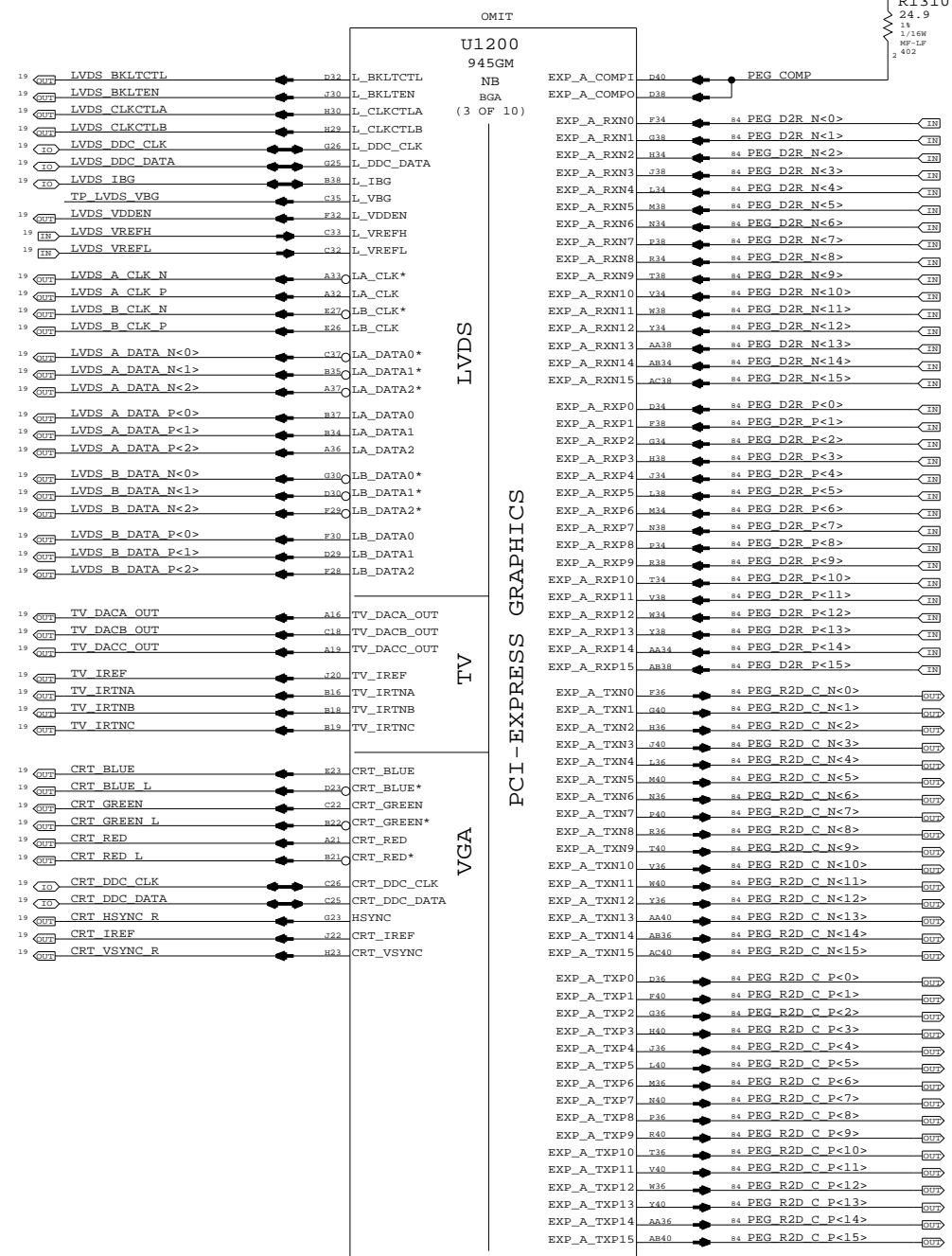
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

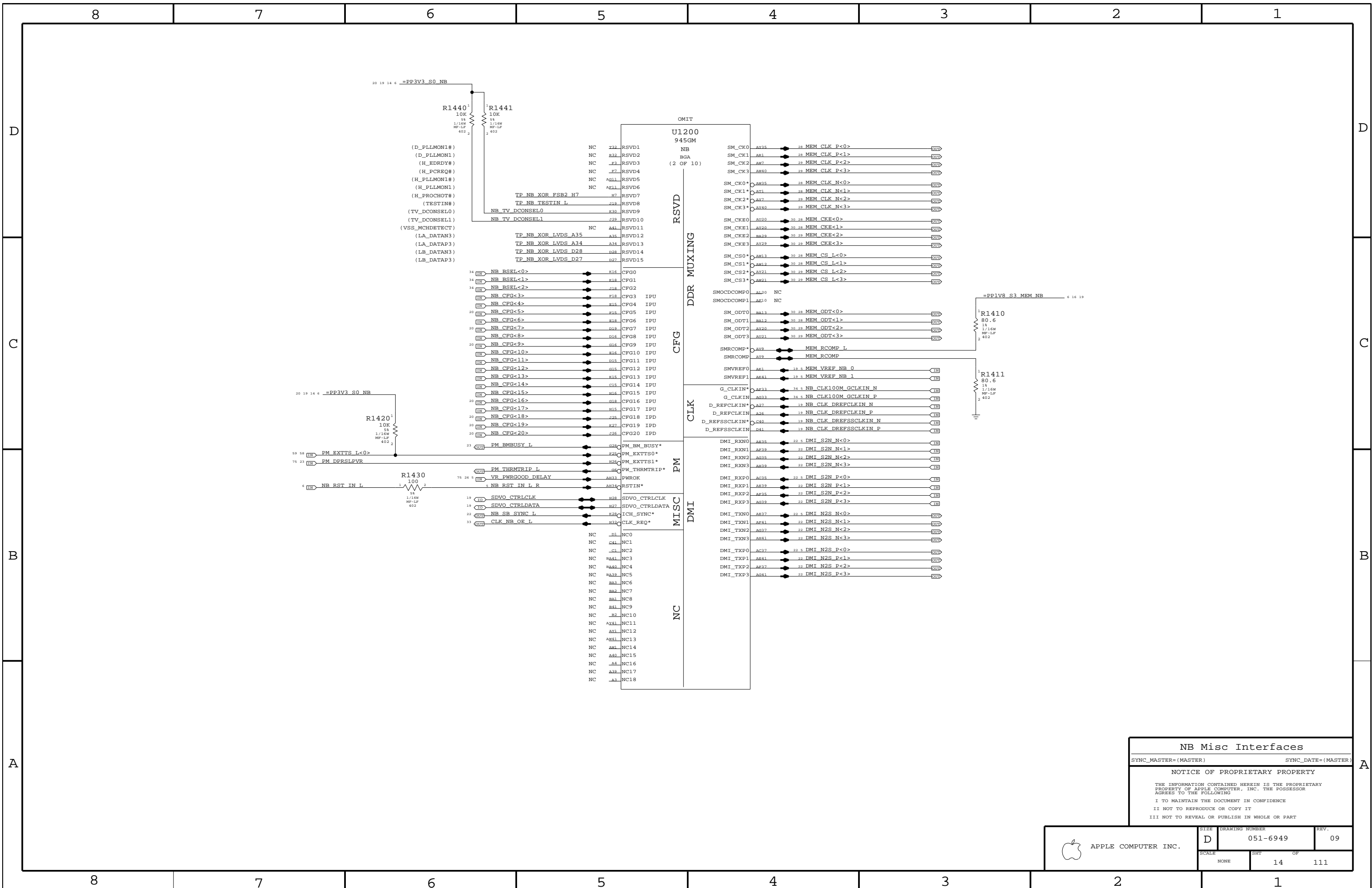
SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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| NONE | 13 OF | | 111 |



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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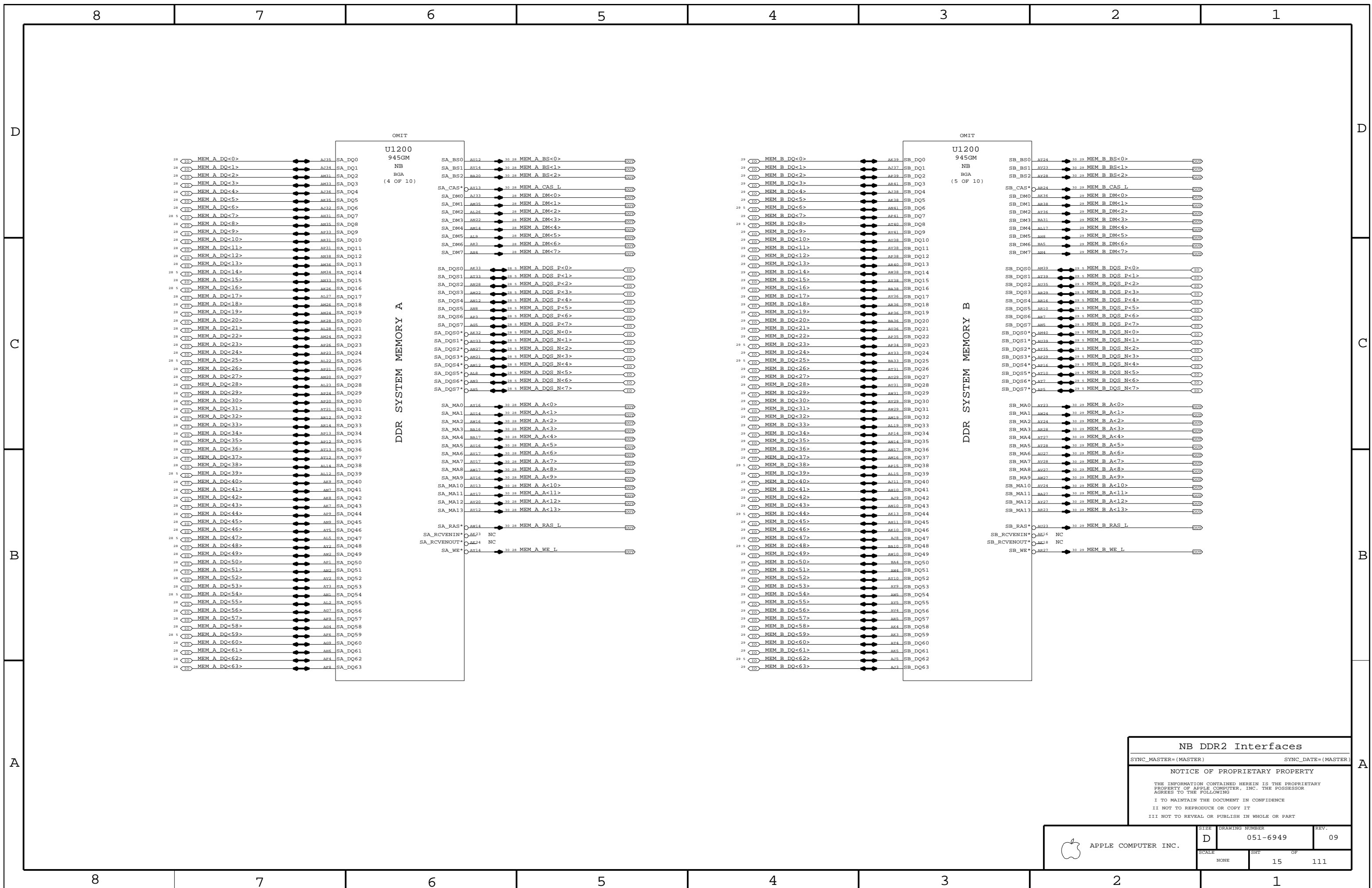
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NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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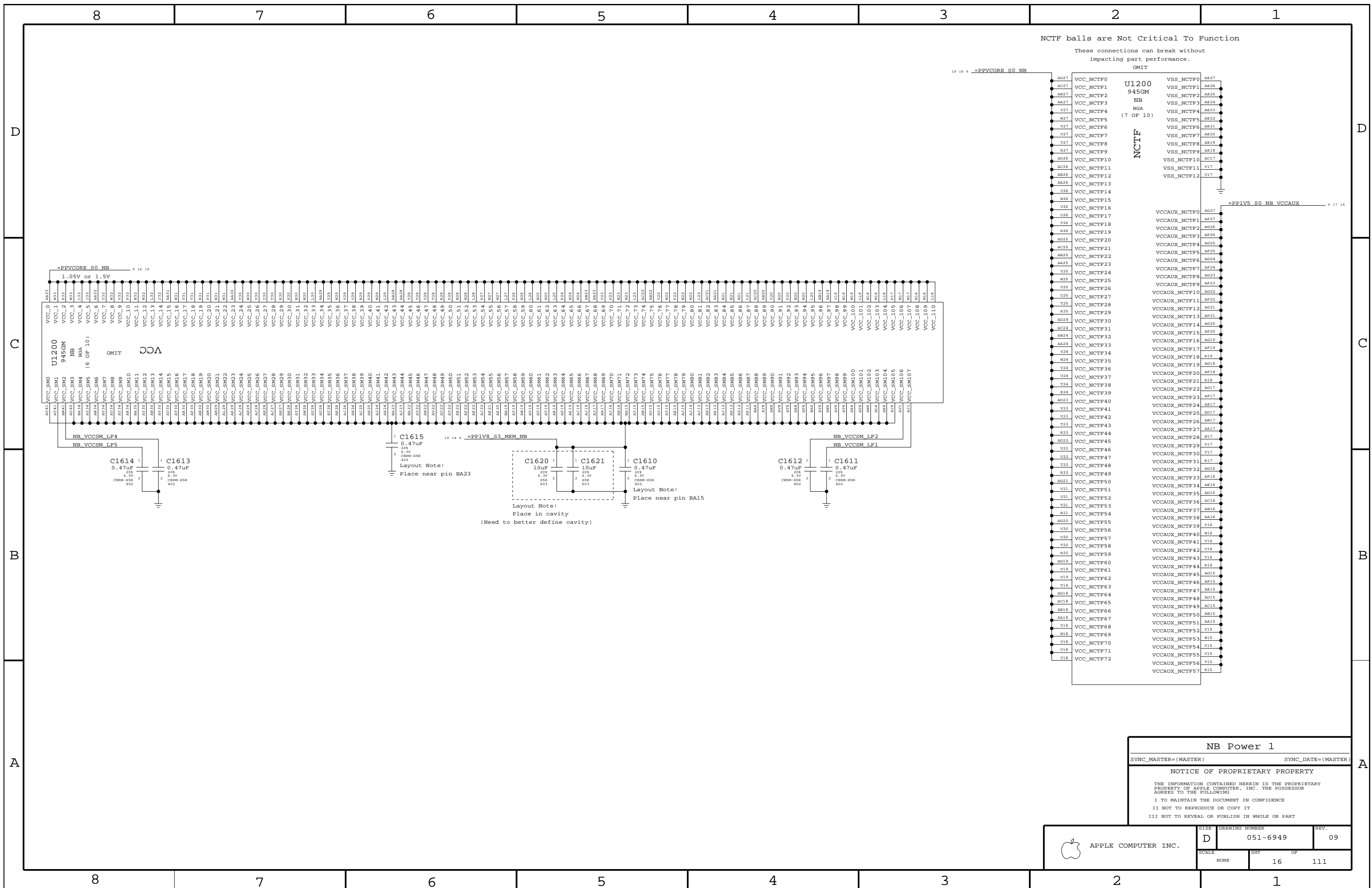
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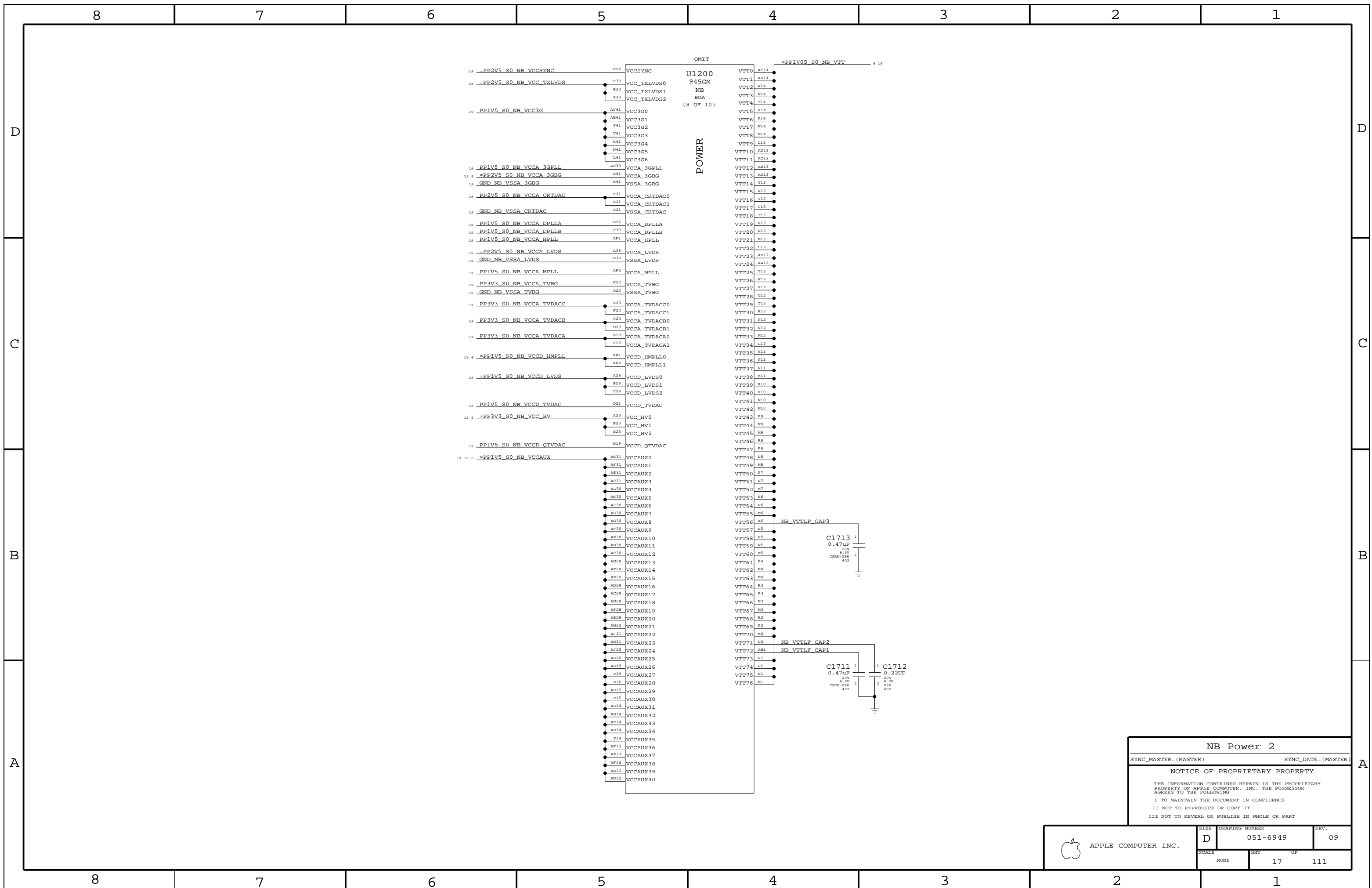
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NB Power 1
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

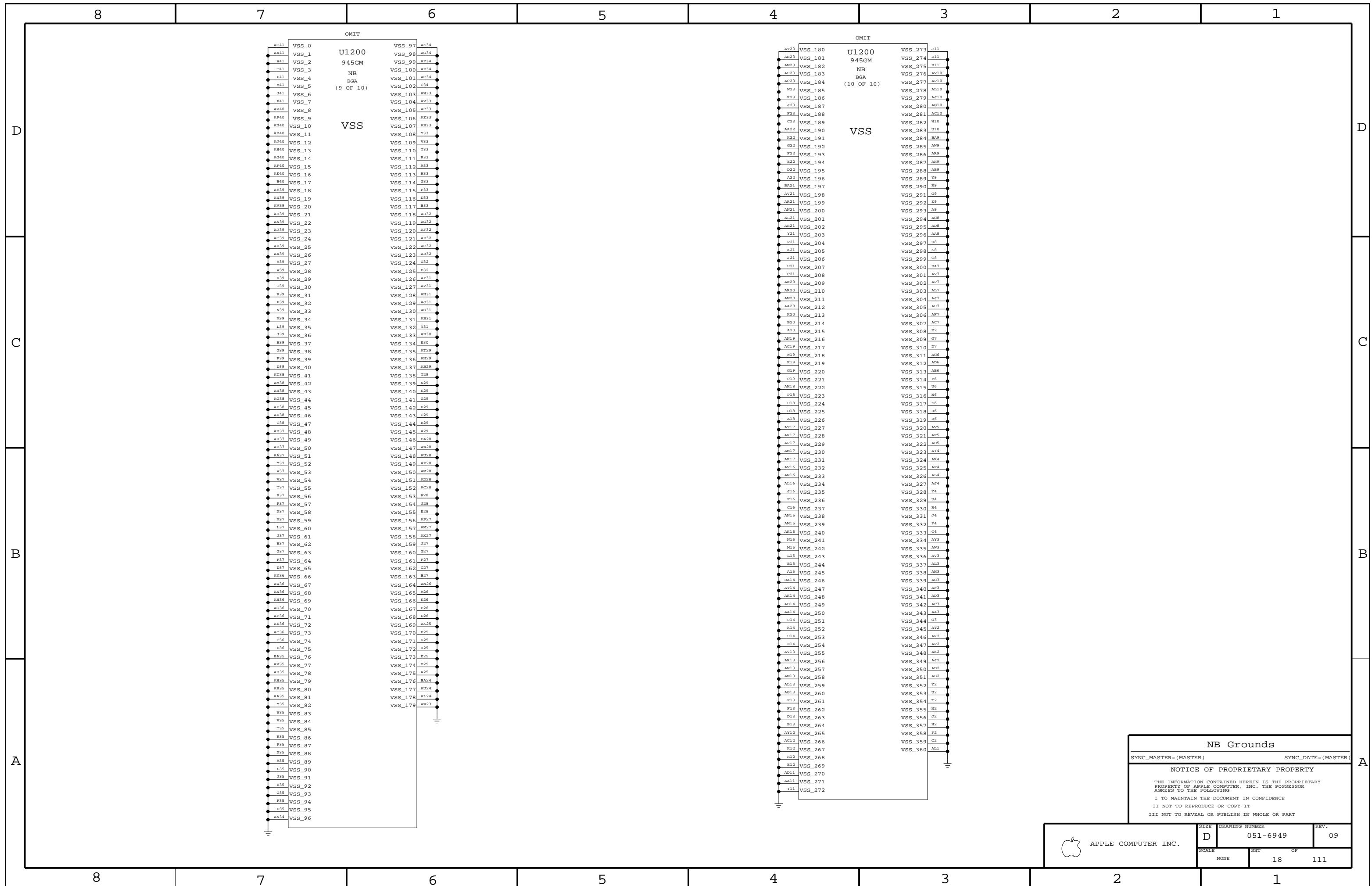
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| | SCALE: NONE | SHEET: 17 | OF: 111 |



NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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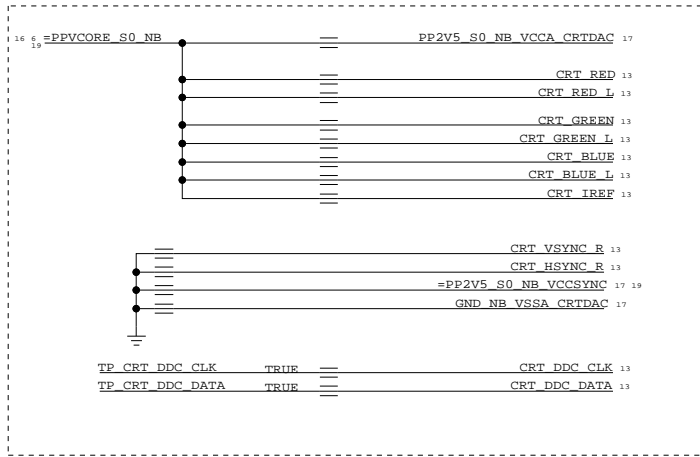
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| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 18 | OF 111 |

Power Interface

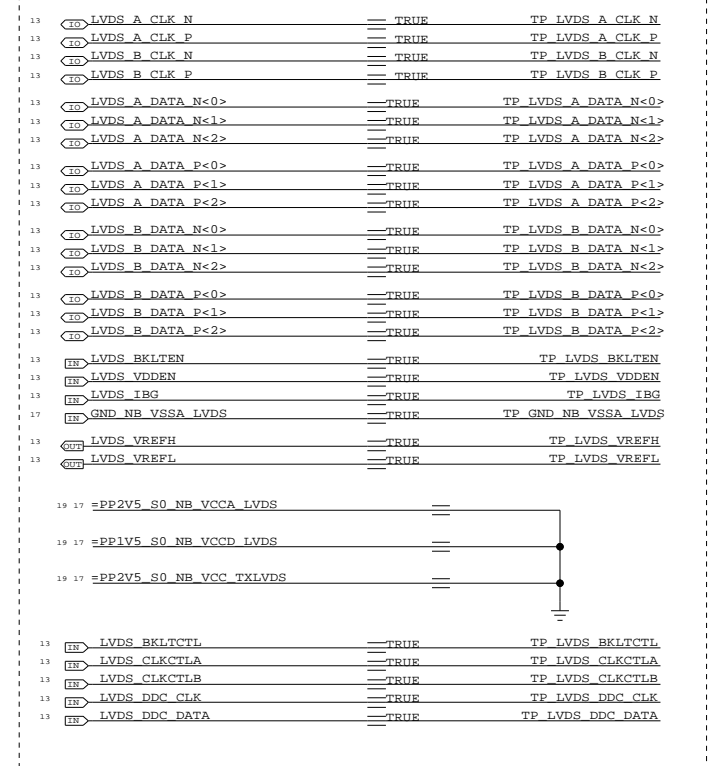
These are the power signals that leave the NB "block"

| | |
|------------------------|------------|
| PP1V05_S0_FSB_NB | 5 6 12 |
| PPVCORE_S0_NB | 6 16 19 |
| PP1V05_S0_NB | 6 |
| PP1V05_S0_NB_VTT | 6 17 19 |
| PP1V5_S0_NB | 6 19 |
| PP1V5_S0_NB_PCIE | 6 13 |
| PP1V5_S0_NB_PLL | 6 19 |
| PP1V5_S0_NB_TVDAC | 6 19 |
| PP1V5_S0_NB_VCCD_HMPLL | 6 17 |
| PP1V5_S0_NB_VCCD_LVDS | 17 19 |
| PP1V5_S0_NB_VCCAUX | 6 16 17 19 |
| PP1V8_S3_MEM_NB | 6 14 16 19 |
| PP2V5_S0_NB_VCCSYNCR | 17 19 |
| PP2V5_S0_NB_VCC_TXLVDS | 17 19 |
| PP2V5_S0_NB_VCCA_3GBG | 6 17 19 |
| PP2V5_S0_NB_VCCA_LVDS | 17 19 |
| PP3V3_S0_NB | 6 14 20 |
| PP3V3_S0_NB_TVDAC | 6 |
| PP3V3_S0_NB_VCC_HV | 6 17 19 |

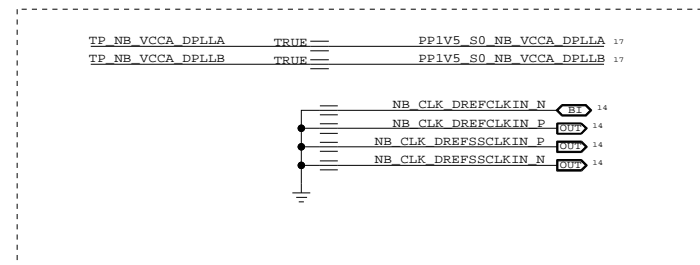
TVOUT DISABLE



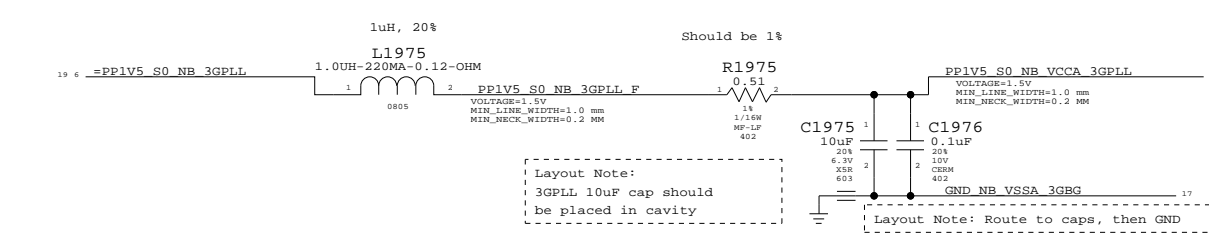
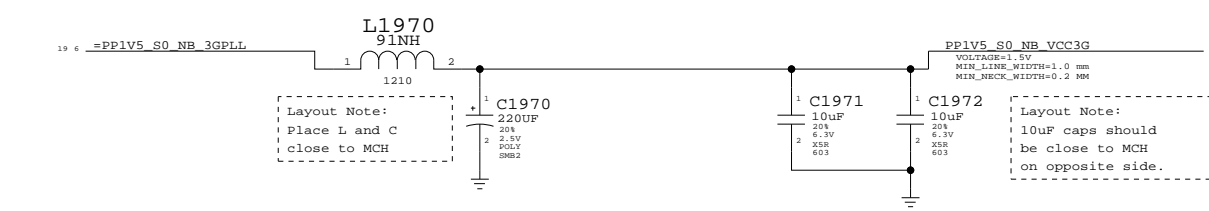
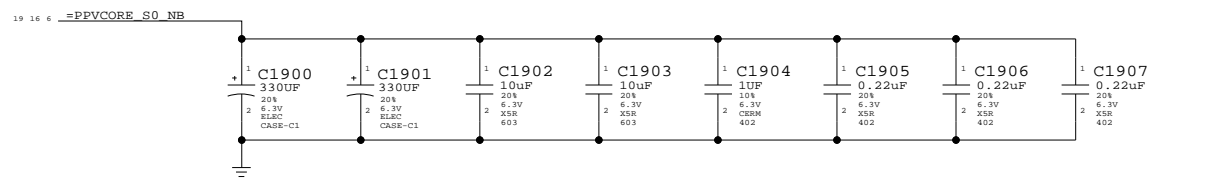
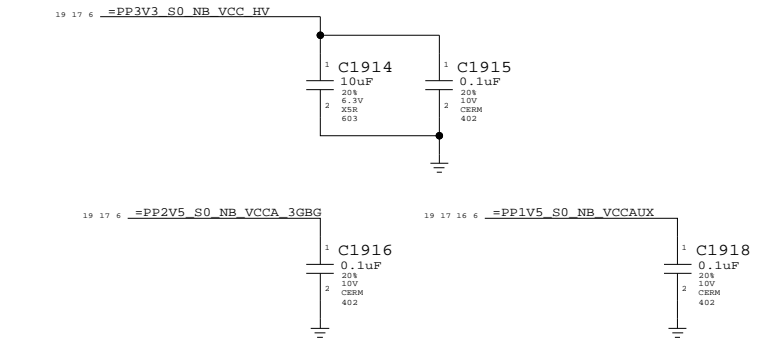
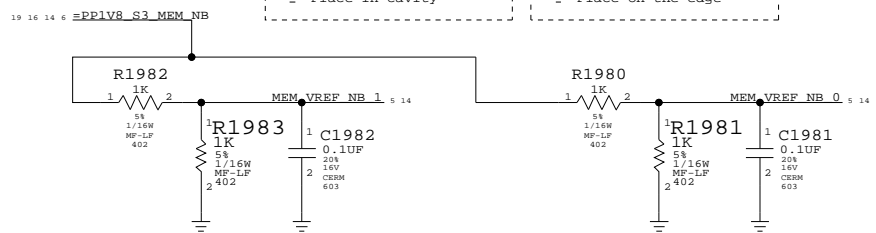
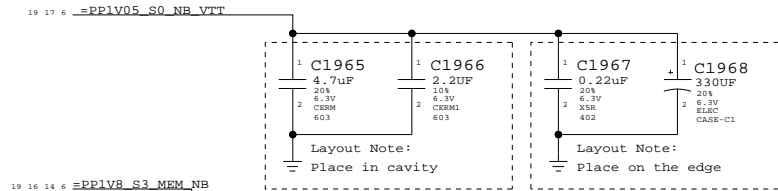
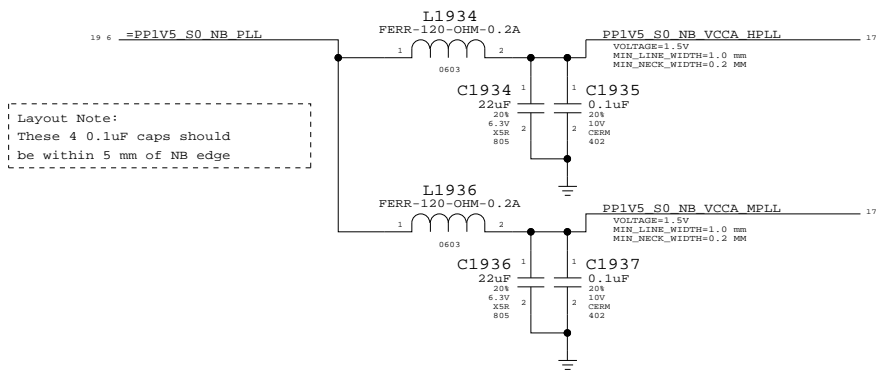
LVDS DISABLE



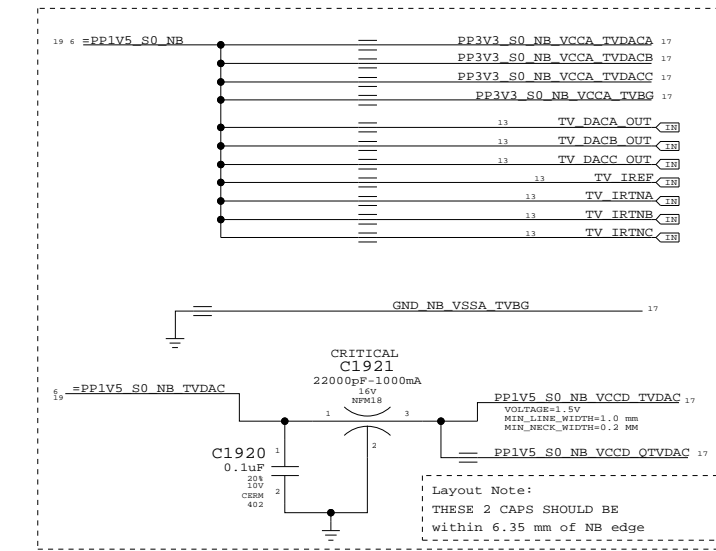
DISPLAY DISABLE



Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge

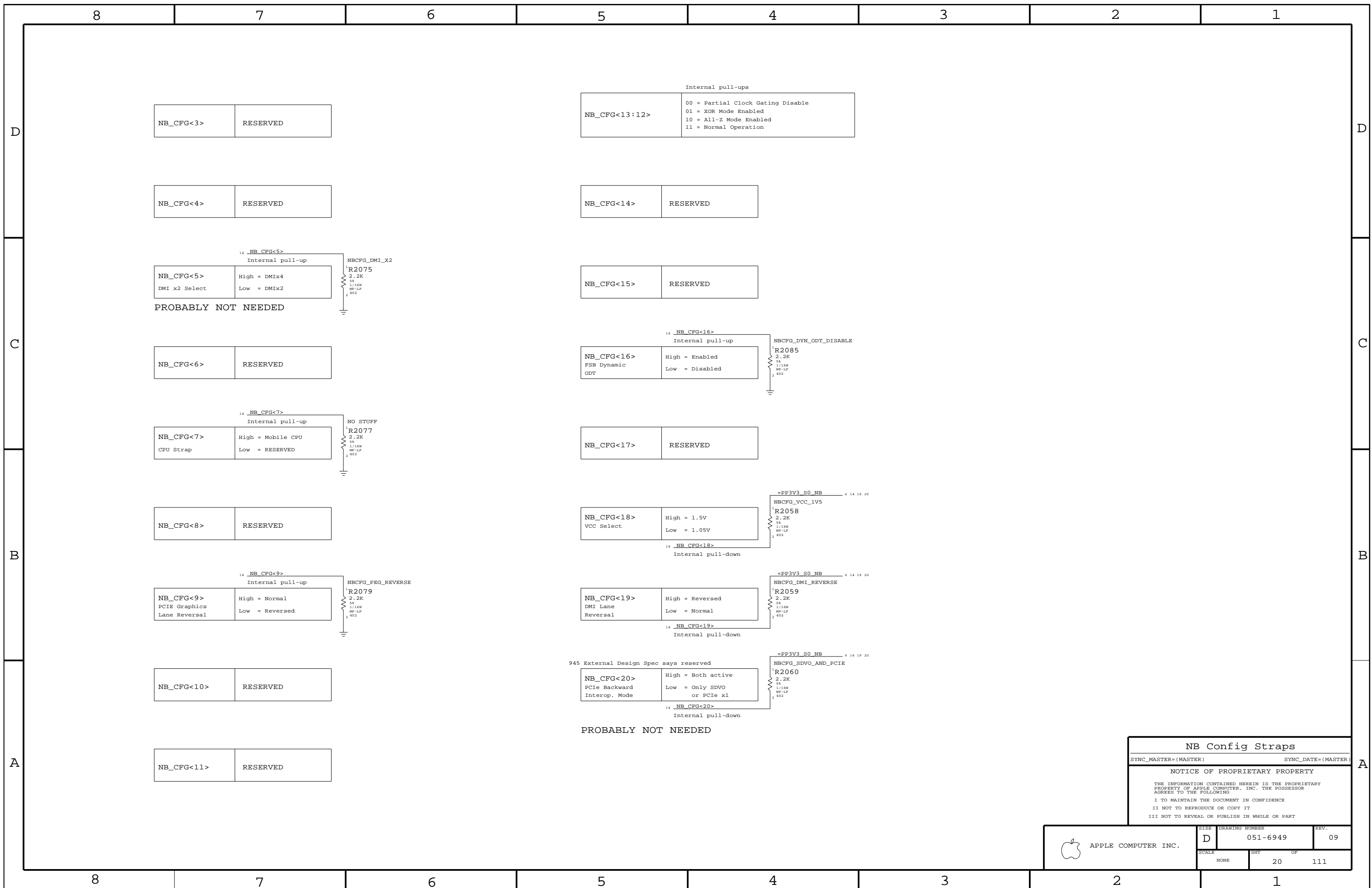


TVOUT DISABLE



Layout Note:
THESE 2 CAPS SHOULD BE WITHIN 6.35 mm OF NB EDGE

NB (GM) Decoupling
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| | |
|-----------|----------|
| NB_CFG<3> | RESERVED |
|-----------|----------|

| | |
|---------------|---|
| NB_CFG<13:12> | Internal pull-ups 00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation |
|---------------|---|

| | |
|-----------|----------|
| NB_CFG<4> | RESERVED |
|-----------|----------|

| | |
|------------|----------|
| NB_CFG<14> | RESERVED |
|------------|----------|

| | |
|----------------------------------|--|
| 14 NB_CFG<5> Internal pull-up | |
| NB_CFG<5> | High = DMIX4 DMI x2 Select Low = DMIX2 |

PROBABLY NOT NEEDED

| | |
|------------|----------|
| NB_CFG<15> | RESERVED |
|------------|----------|

| | |
|-----------|----------|
| NB_CFG<6> | RESERVED |
|-----------|----------|

| | |
|-----------------------------------|--|
| 14 NB_CFG<16> Internal pull-up | |
| NB_CFG<16> | High = Enabled FSB Dynamic ODT Low = Disabled |

| | |
|----------------------------------|--|
| 14 NB_CFG<7> Internal pull-up | |
| NB_CFG<7> | High = Mobile CPU CPU Strap Low = RESERVED |

| | |
|------------|----------|
| NB_CFG<17> | RESERVED |
|------------|----------|

| | |
|-----------|----------|
| NB_CFG<8> | RESERVED |
|-----------|----------|

| | |
|--|--|
| =PP3V3_S0_NB 6 14 19 20 NBCFG_VCC_LV5 | |
| NB_CFG<18> | High = 1.5V VCC Select Low = 1.05V |

14 NB_CFG<18>
Internal pull-down

| | |
|----------------------------------|---|
| 14 NB_CFG<9> Internal pull-up | |
| NB_CFG<9> | High = Normal PCIe Graphics Lane Reversal Low = Reversed |

| | |
|--|---|
| =PP3V3_S0_NB 6 14 19 20 NBCFG_DMI_REVERSE | |
| NB_CFG<19> | High = Reversed DMI Lane Reversal Low = Normal |

14 NB_CFG<19>
Internal pull-down

| | |
|------------|----------|
| NB_CFG<10> | RESERVED |
|------------|----------|

| | |
|--|---|
| 945 External Design Spec says reserved =PP3V3_S0_NB 6 14 19 20 NBCFG_SDVO_AND_PCIE | |
| NB_CFG<20> | High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1 |

14 NB_CFG<20>
Internal pull-down

| | |
|------------|----------|
| NB_CFG<11> | RESERVED |
|------------|----------|

PROBABLY NOT NEEDED

NB Config Straps

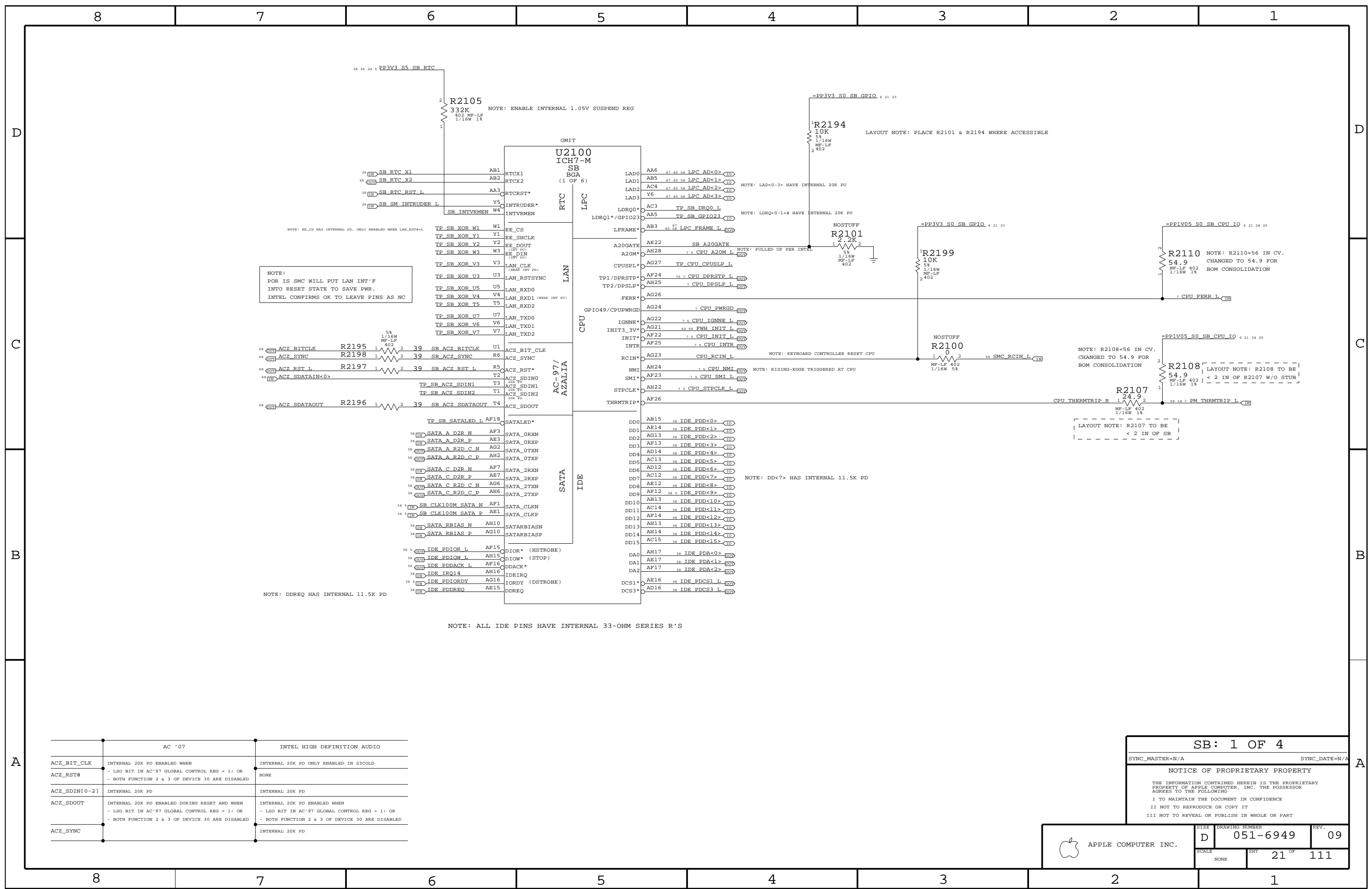
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| NONE | 20 | 111 | |



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

| AC '07 | INTEL HIGH DEFINITION AUDIO |
|---------------|---|
| ACZ_BIT_CLK | INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR |
| ACZ_RST# | NONE |
| ACZ_SDIN[0-2] | INTERNAL 20K PD |
| ACZ_SDOUT | INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED |
| ACZ_SYNC | INTERNAL 20K PD |

SB: 1 OF 4

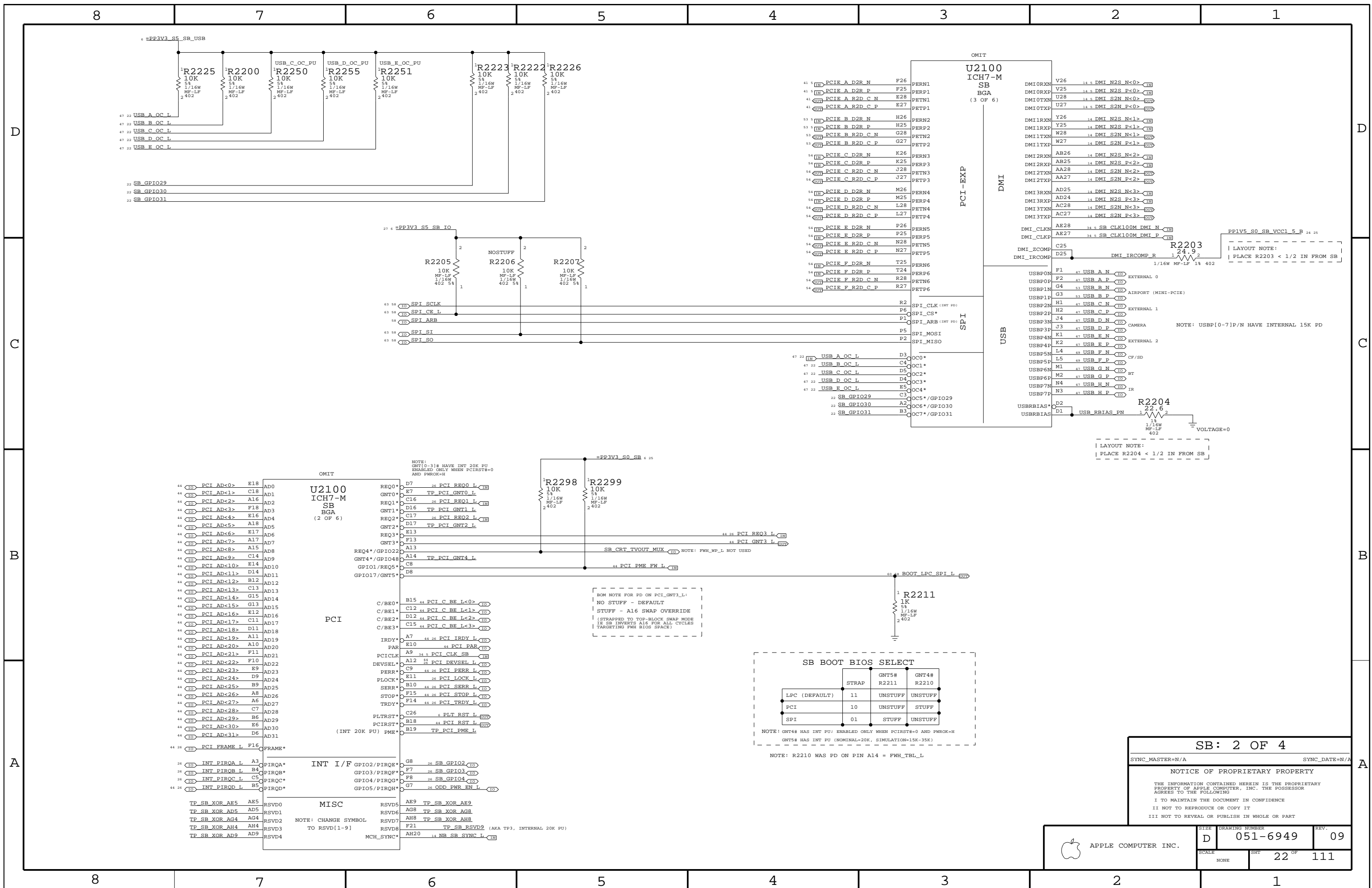
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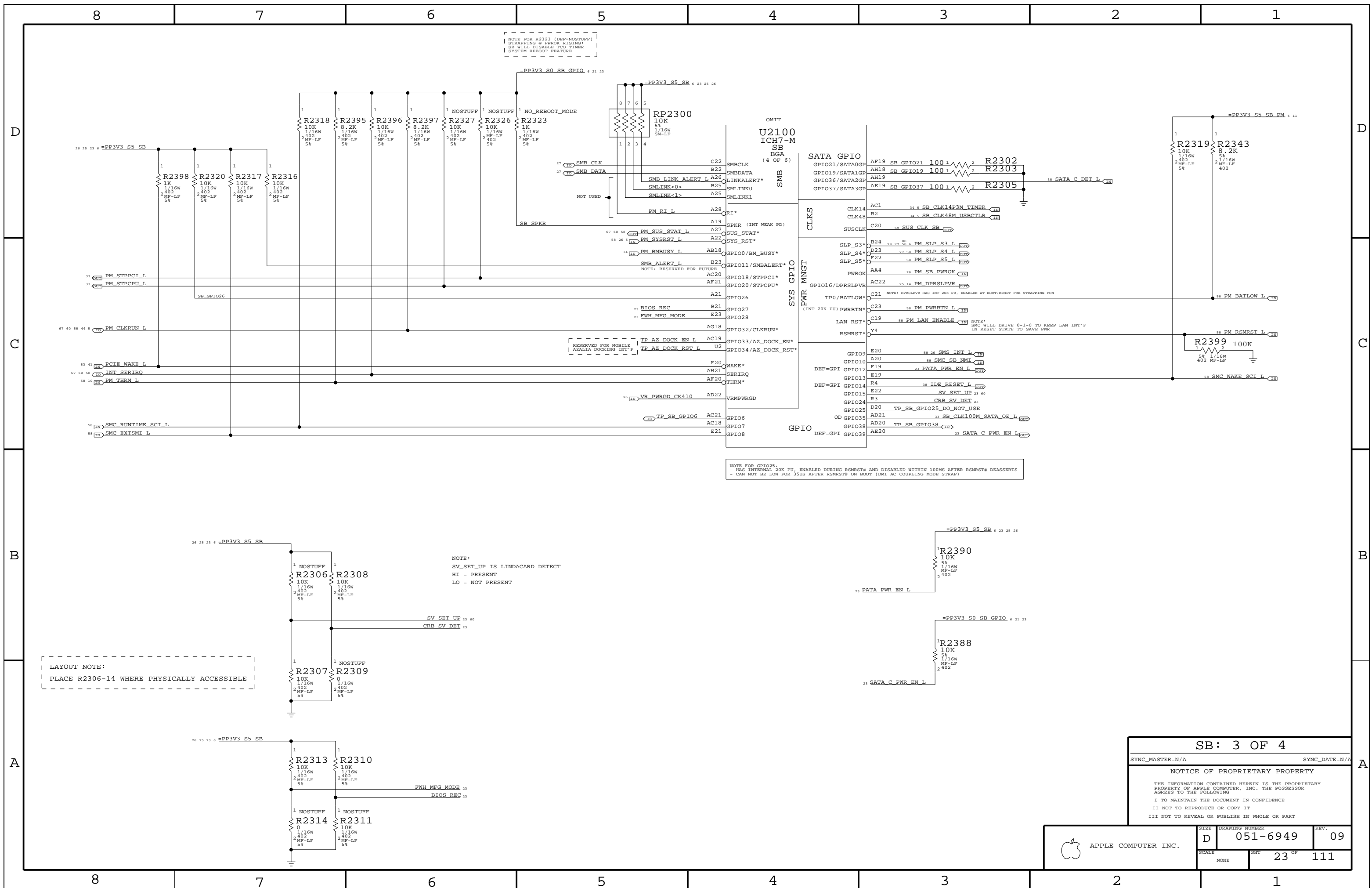
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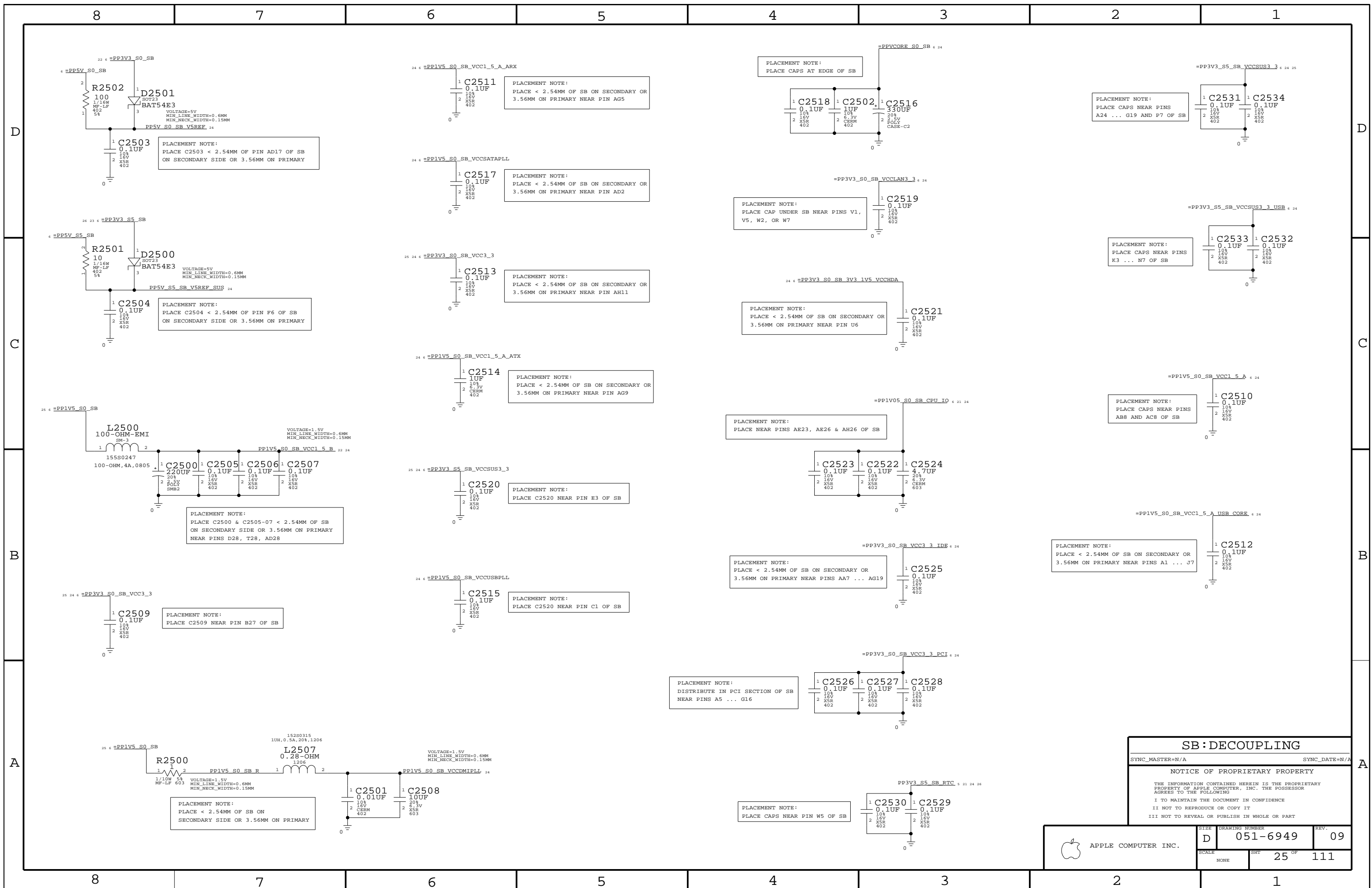
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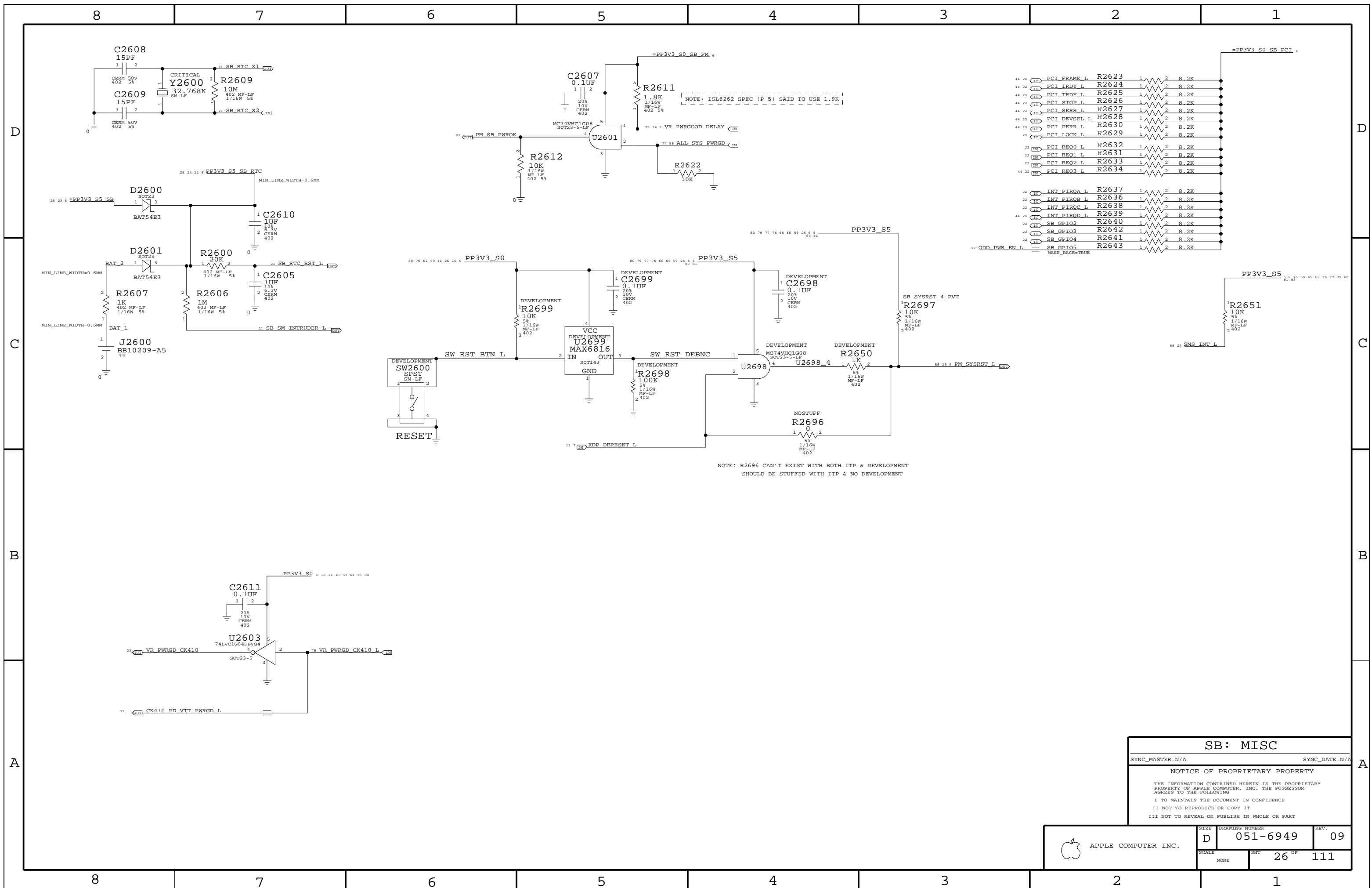


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SB: MISC

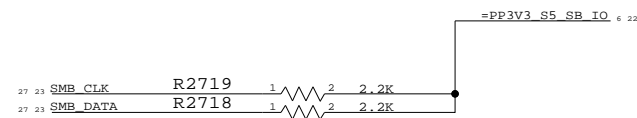
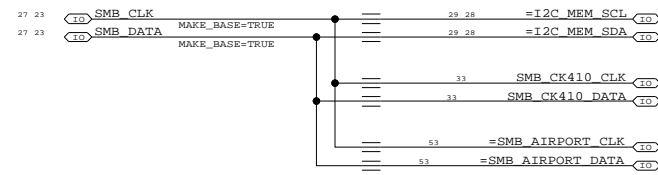
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SB I2C BUSSES



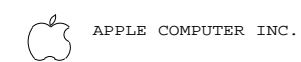
SB: SMB HUB

SYNC_MASTER=N/A SYNC_DATE=N/A

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Page Notes

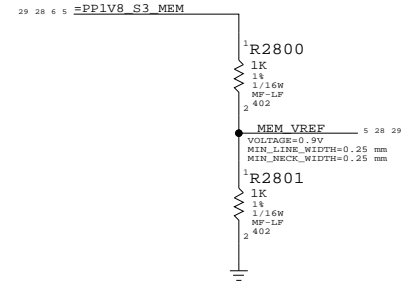
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

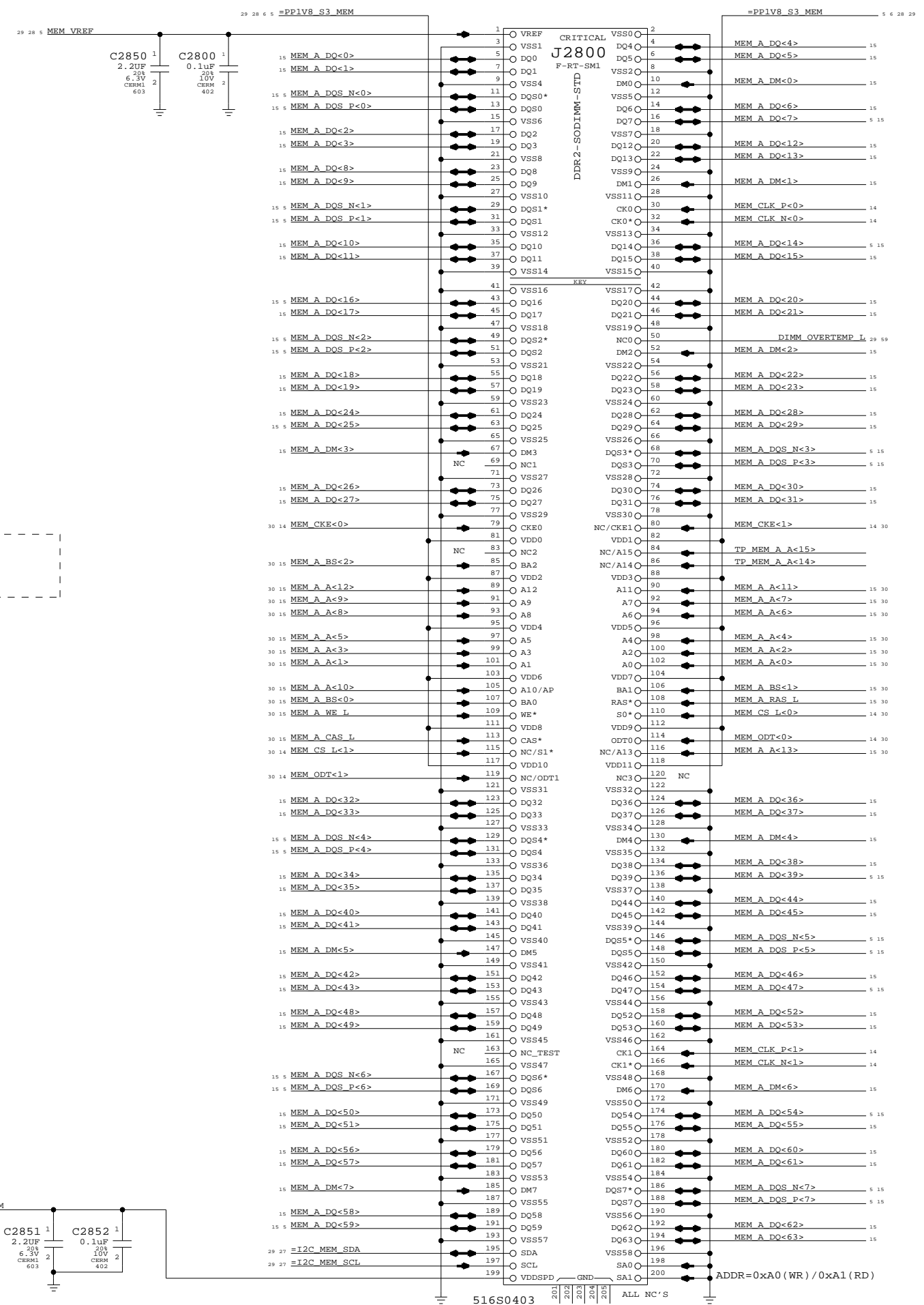
BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector

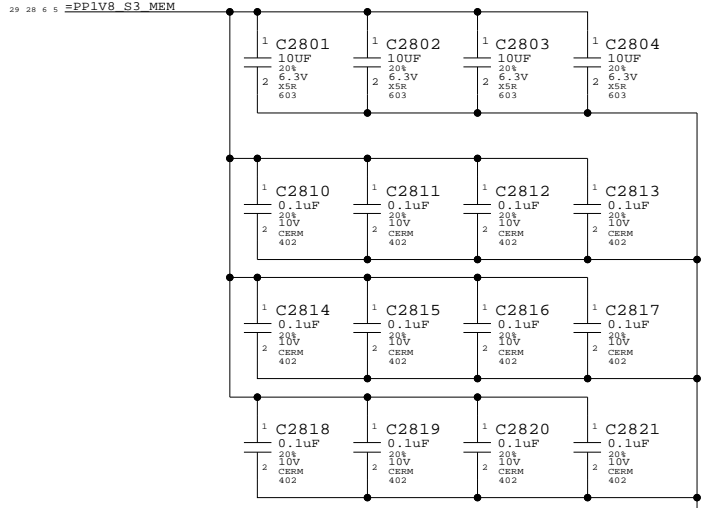


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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| NONE | 28 | 111 | |

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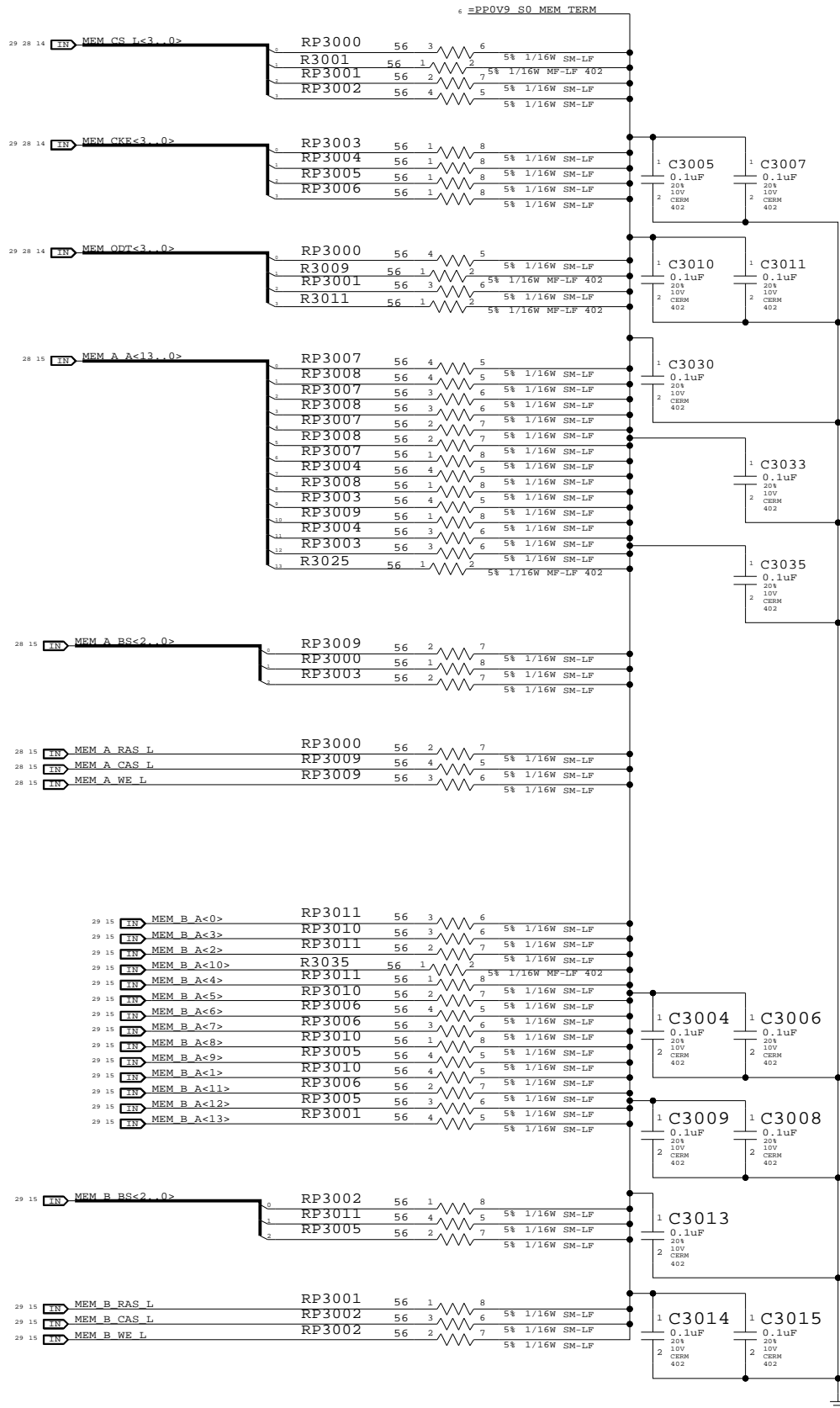
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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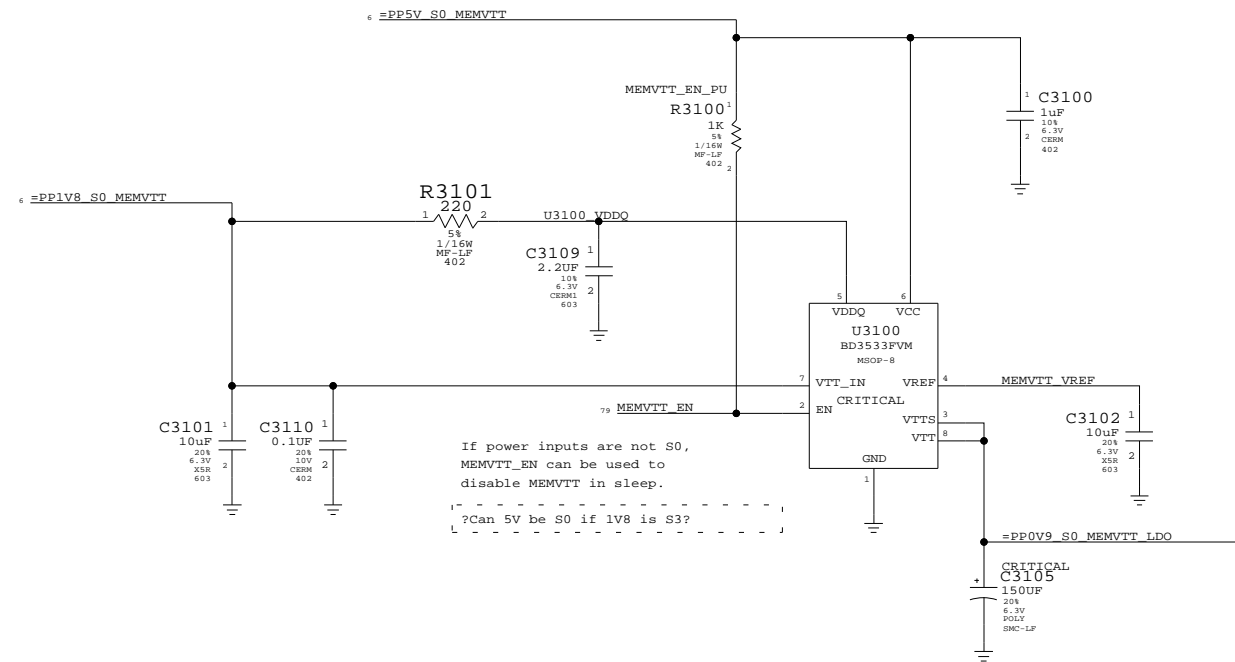
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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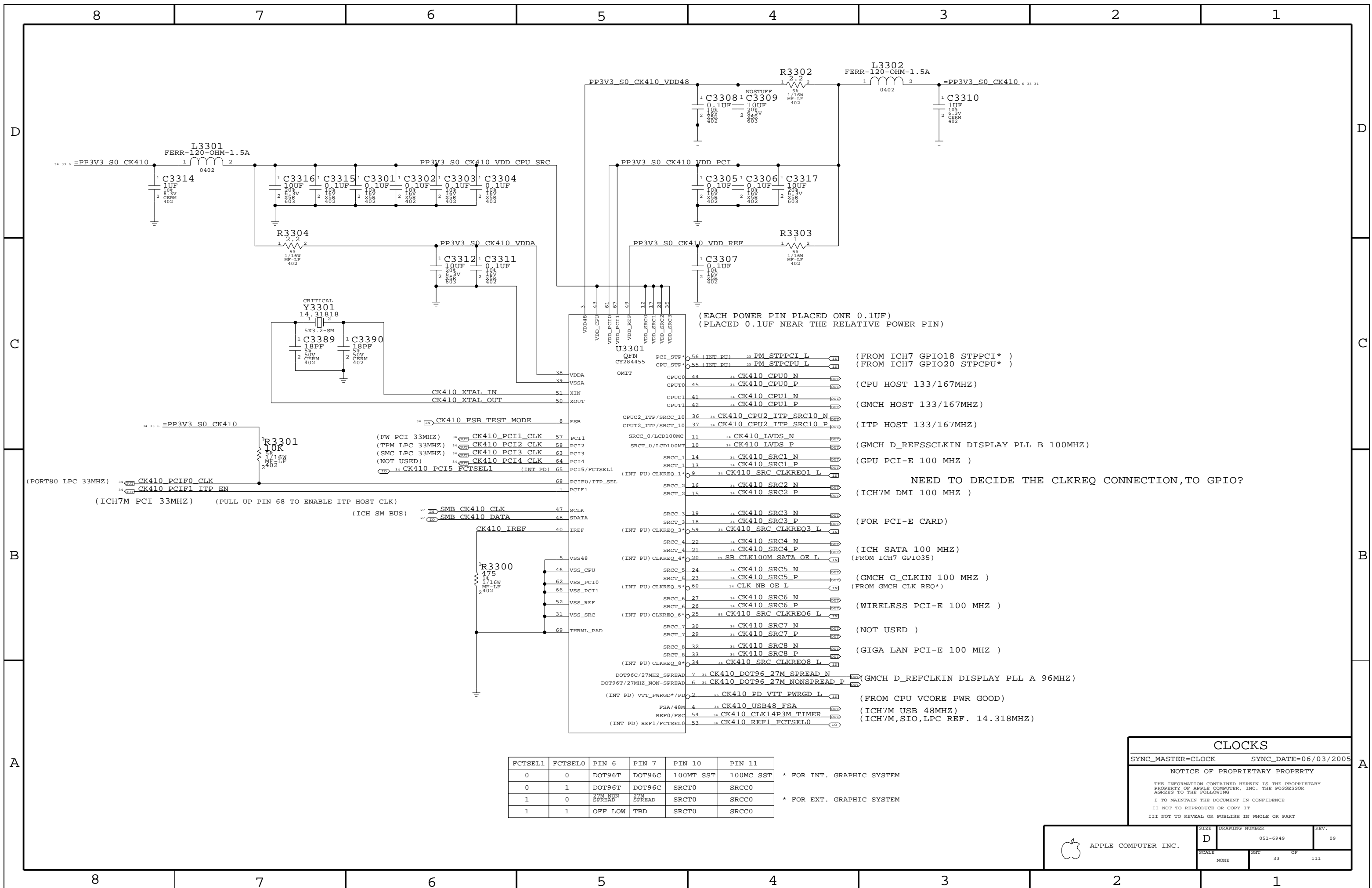
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(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)

(FROM ICH7 GPIO35)

(GMCH G_CLKIN 100 MHZ)

(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

| FCTSEL1 | FCTSEL0 | PIN 6 | PIN 7 | PIN 10 | PIN 11 |
|---------|---------|----------------|------------|-----------|-----------|
| 0 | 0 | DOT96T | DOT96C | 100MT_SST | 100MC_SST |
| 0 | 1 | DOT96T | DOT96C | SRCT0 | SRCC0 |
| 1 | 0 | 27M NON SPREAD | 27M SPREAD | SRCT0 | SRCC0 |
| 1 | 1 | OFF LOW | TBD | SRCT0 | SRCC0 |

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

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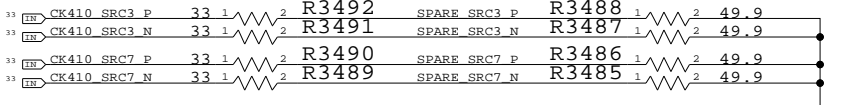
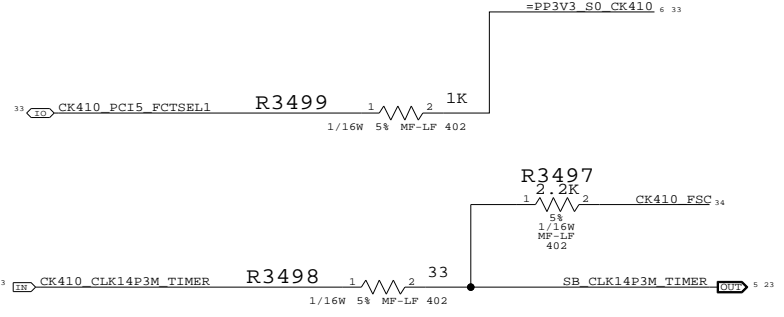
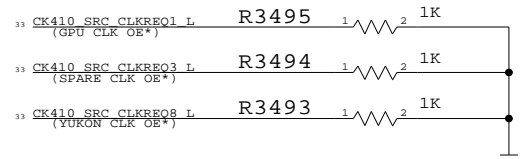
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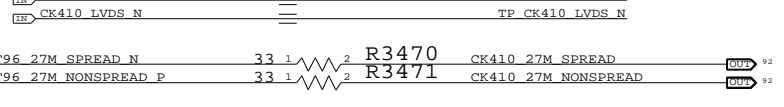
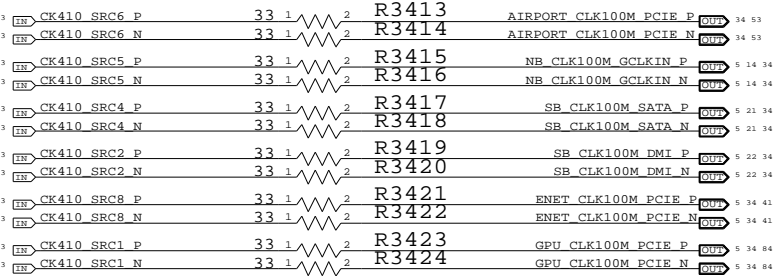
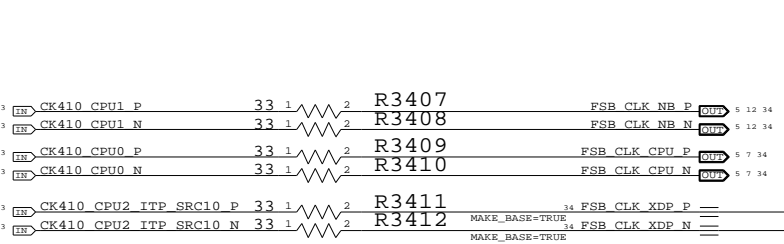
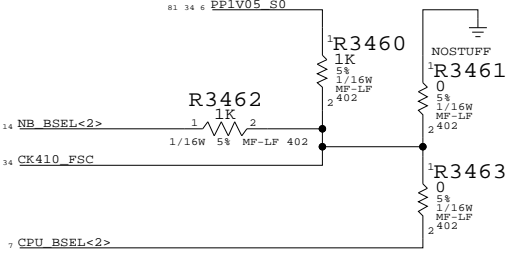
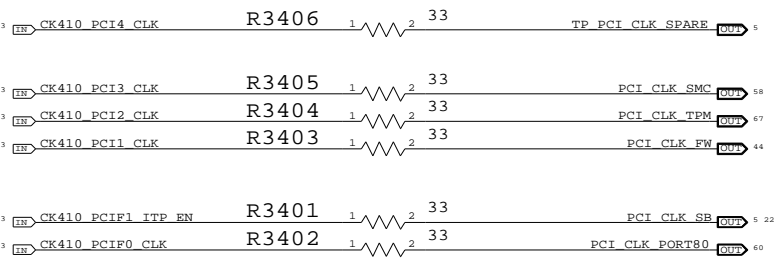
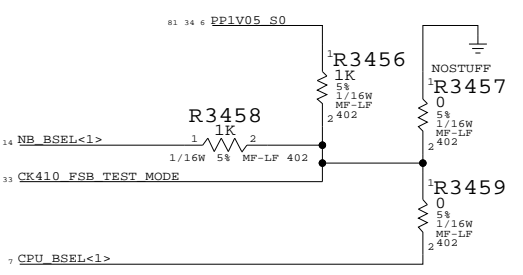
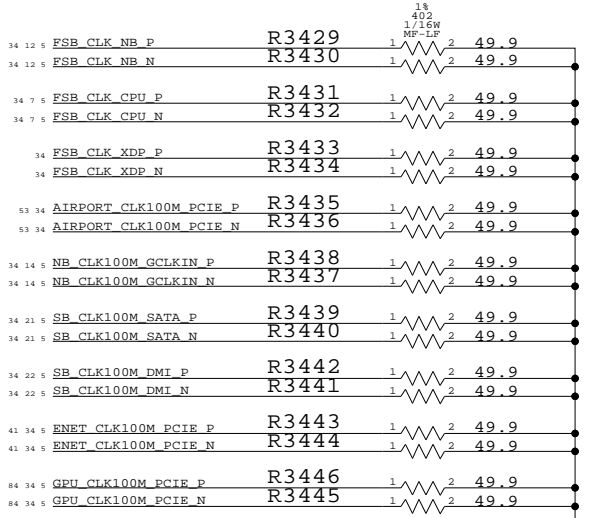
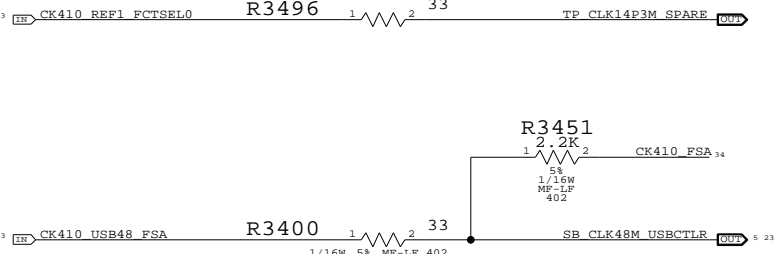
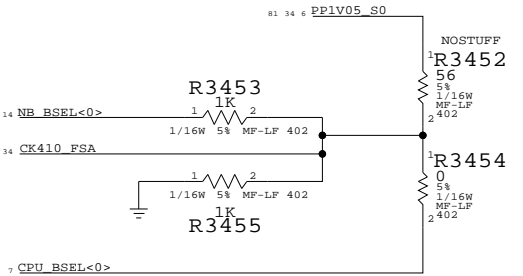
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|-------|----------------|------|
| SCALE | DRAWING NUMBER | REV. |
| NONE | D 051-6949 | 09 |
| SHT | OF | 111 |
| 33 | | |

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

| | STUFF | NO STUFF |
|----------------------------|-------------------------|----------------|
| CPU DRIVEN | R3453 R3454 R3455 | R3456 R3457 |
| 533MHZ (133MHZ CPU CLK) | R3452 R3461 | R3458 R3459 |
| 667MHZ (166MHZ CPU CLK) | R3452 R3461 | R3458 R3459 |



CLOCKS: TERMINATIONS

SYNC_MASTER=N/A SYNC_DATE=N/A

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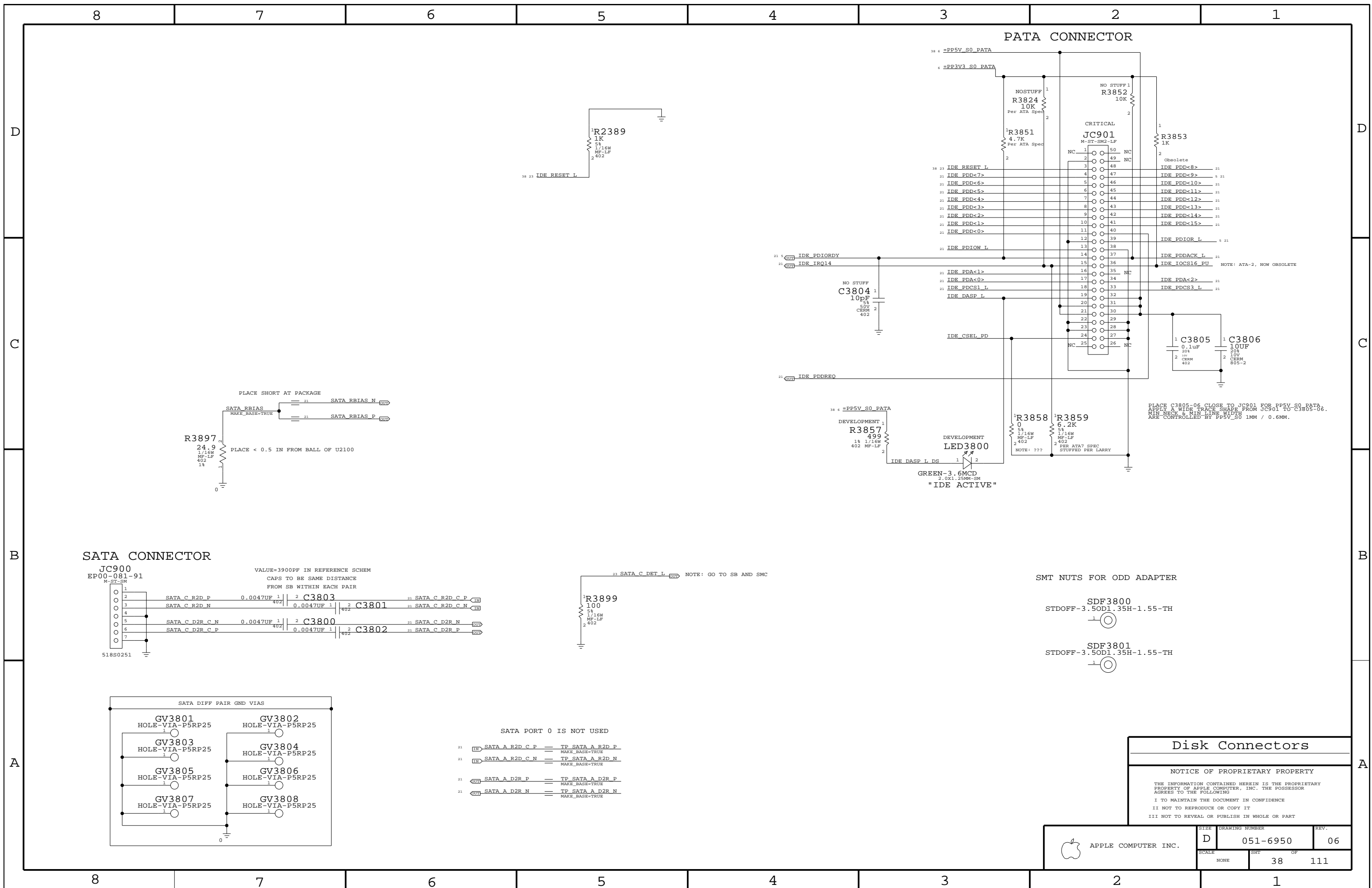
II NOT TO REPRODUCE OR COPY IT

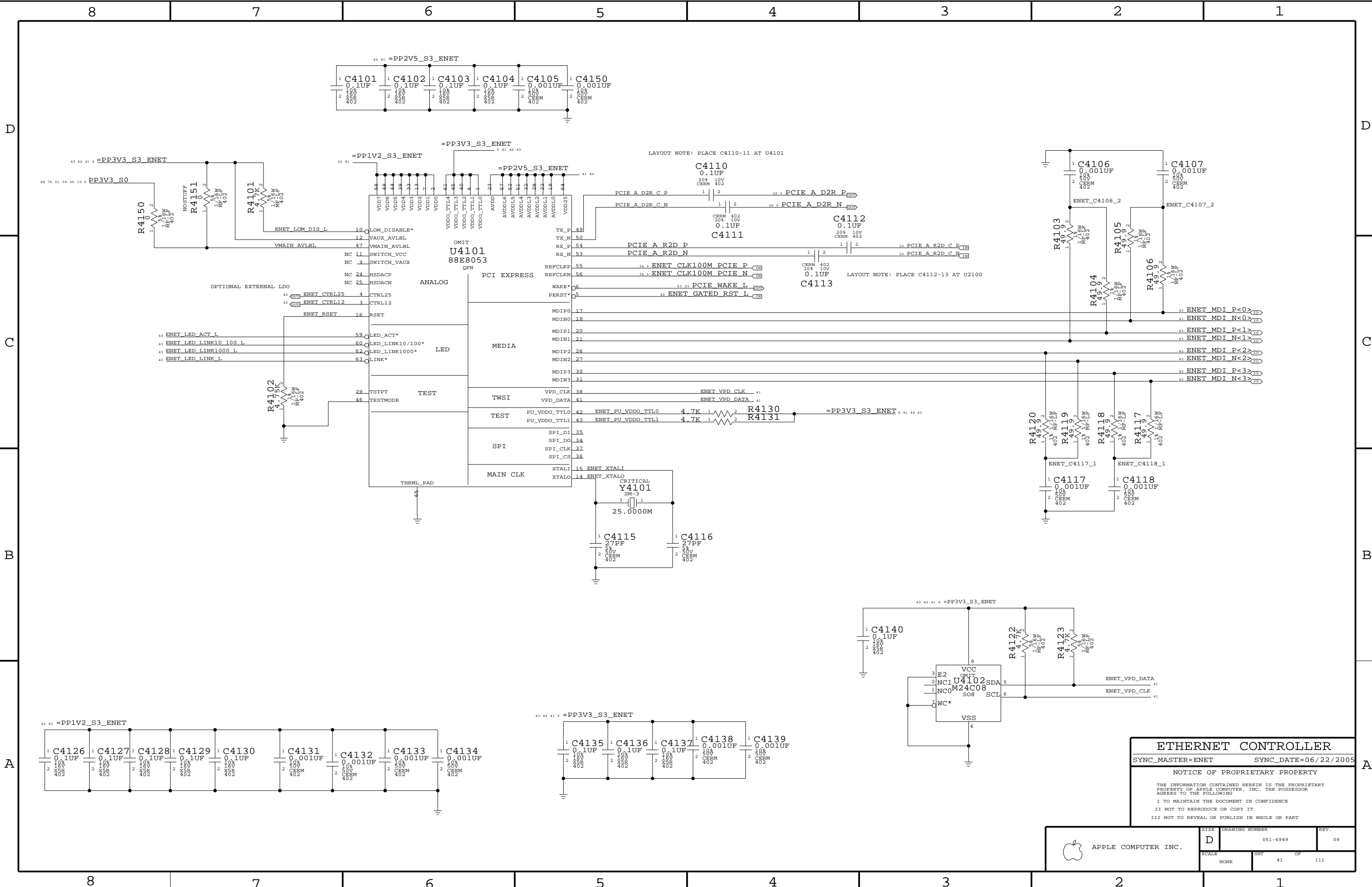
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SCALE: NONE SHEET: 34 OF 111

SIZE: D DRAWING NUMBER: 051-6949 REV: 09





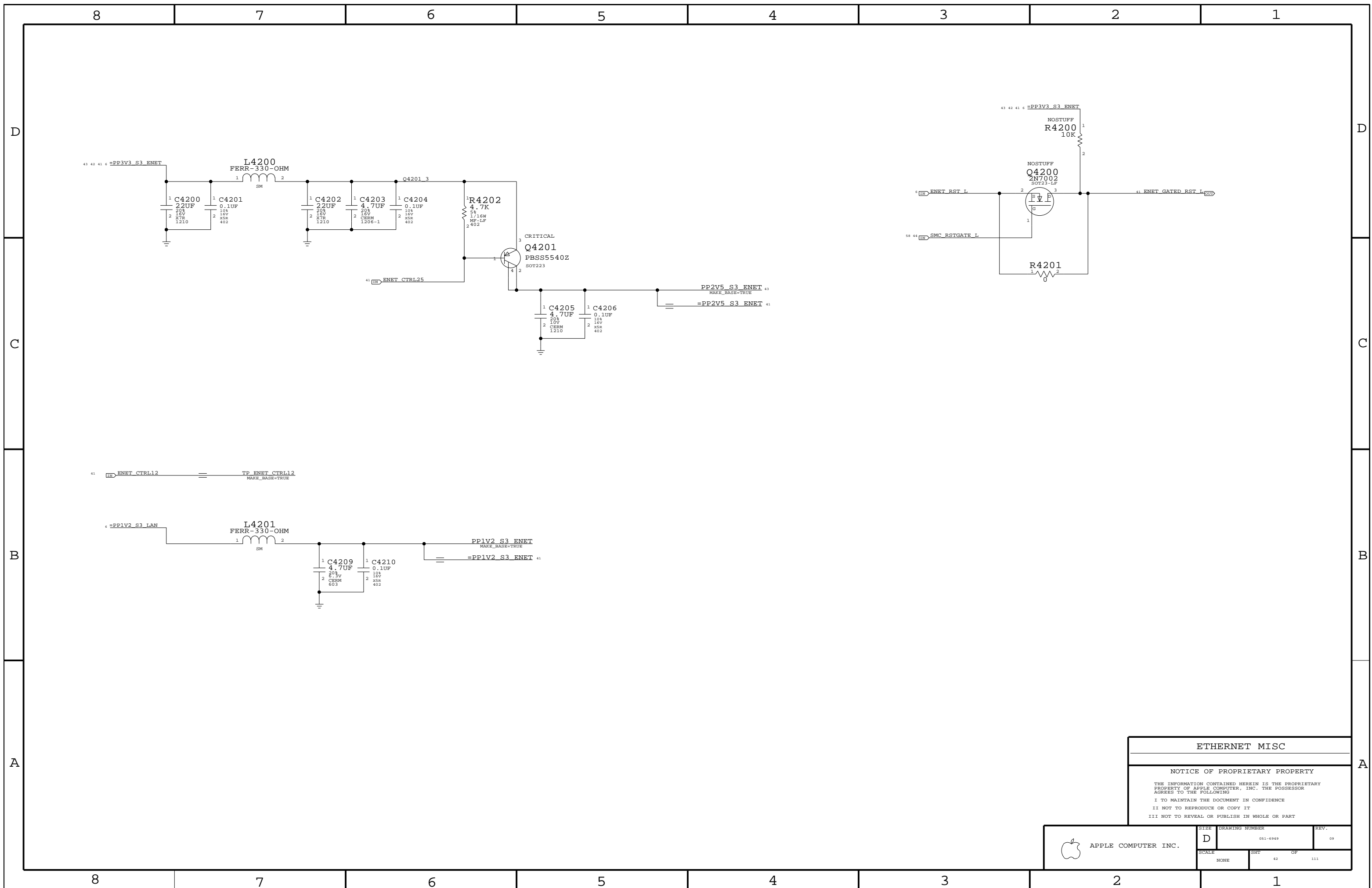
ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=06/22/2005

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| | SCALE | DRAWING NUMBER | | REV. |
| | NONE | D | 051-6949 | 09 |
| | | SHT | OF | |
| | | 41 | 111 | |



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

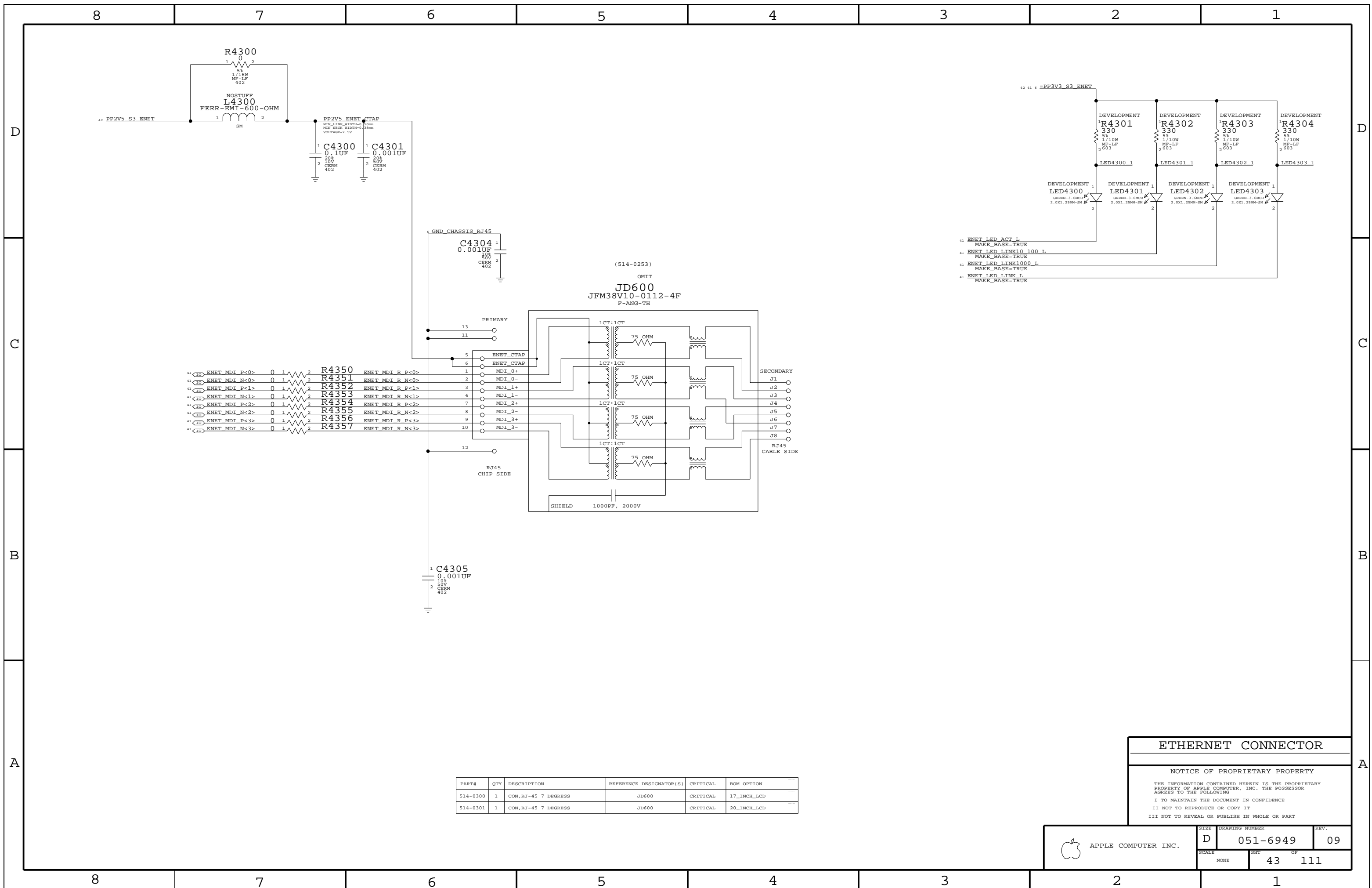
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|---------------------|------------------|----------------------------|------------|
| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 42 | OF 111 |



| | | | | | |
|---------------|---|---|---|-------|-----------------|
| ENET MDI P<0> | 0 | 1 | 2 | R4350 | ENET MDI R P<0> |
| ENET MDI N<0> | 0 | 1 | 2 | R4351 | ENET MDI R N<0> |
| ENET MDI P<1> | 0 | 1 | 2 | R4352 | ENET MDI R P<1> |
| ENET MDI N<1> | 0 | 1 | 2 | R4353 | ENET MDI R N<1> |
| ENET MDI P<2> | 0 | 1 | 2 | R4354 | ENET MDI R P<2> |
| ENET MDI N<2> | 0 | 1 | 2 | R4355 | ENET MDI R N<2> |
| ENET MDI P<3> | 0 | 1 | 2 | R4356 | ENET MDI R P<3> |
| ENET MDI N<3> | 0 | 1 | 2 | R4357 | ENET MDI R N<3> |

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---------------------|-------------------------|----------|-------------|
| 514-0300 | 1 | CON,RJ-45 7 DEGRESS | JD600 | CRITICAL | 17_INCH_LCD |
| 514-0301 | 1 | CON,RJ-45 7 DEGRESS | JD600 | CRITICAL | 20_INCH_LCD |

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

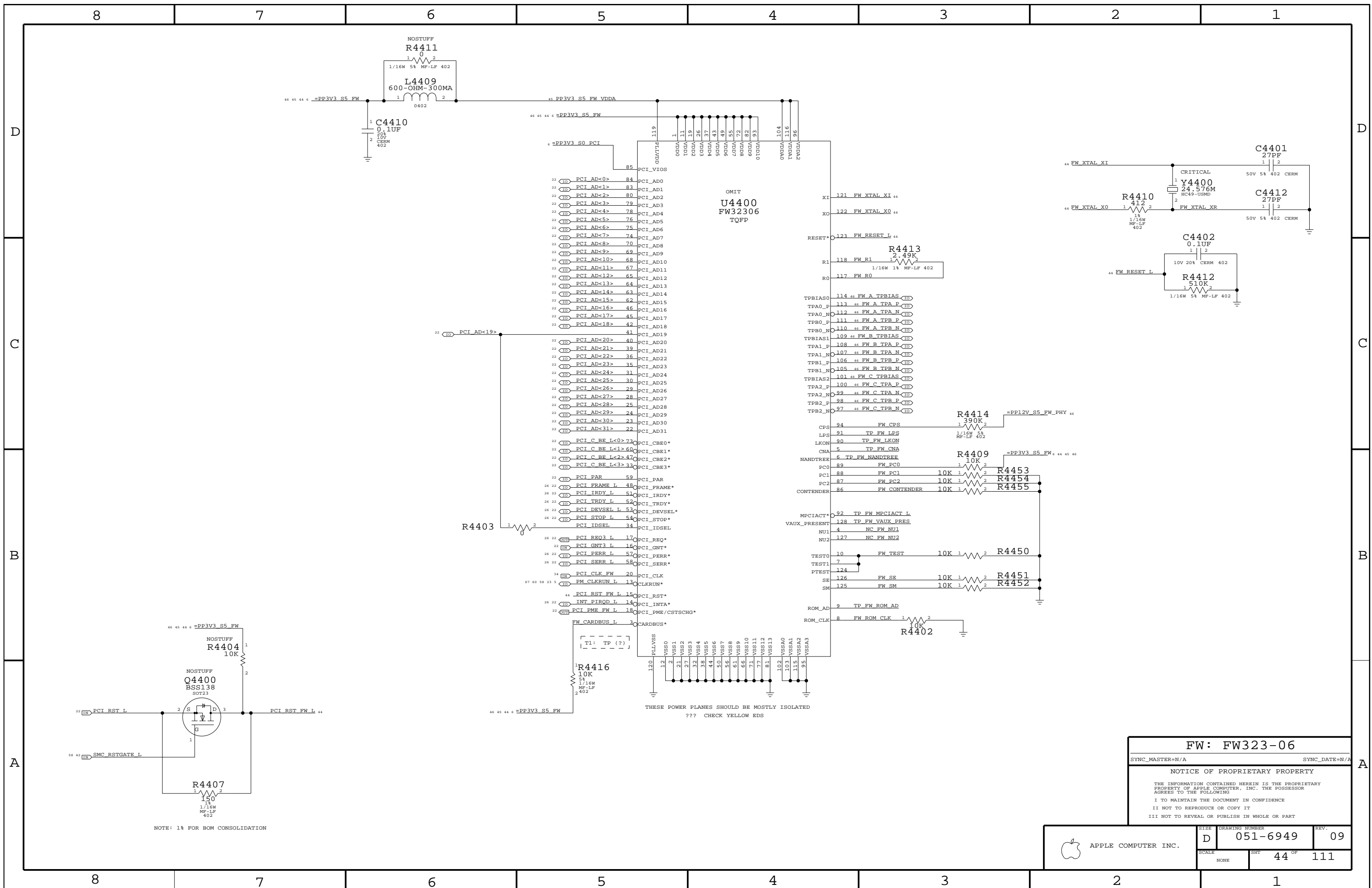
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | | OF |
| NONE | 43 | | 111 |



THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
 ??? CHECK YELLOW EDS

NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06

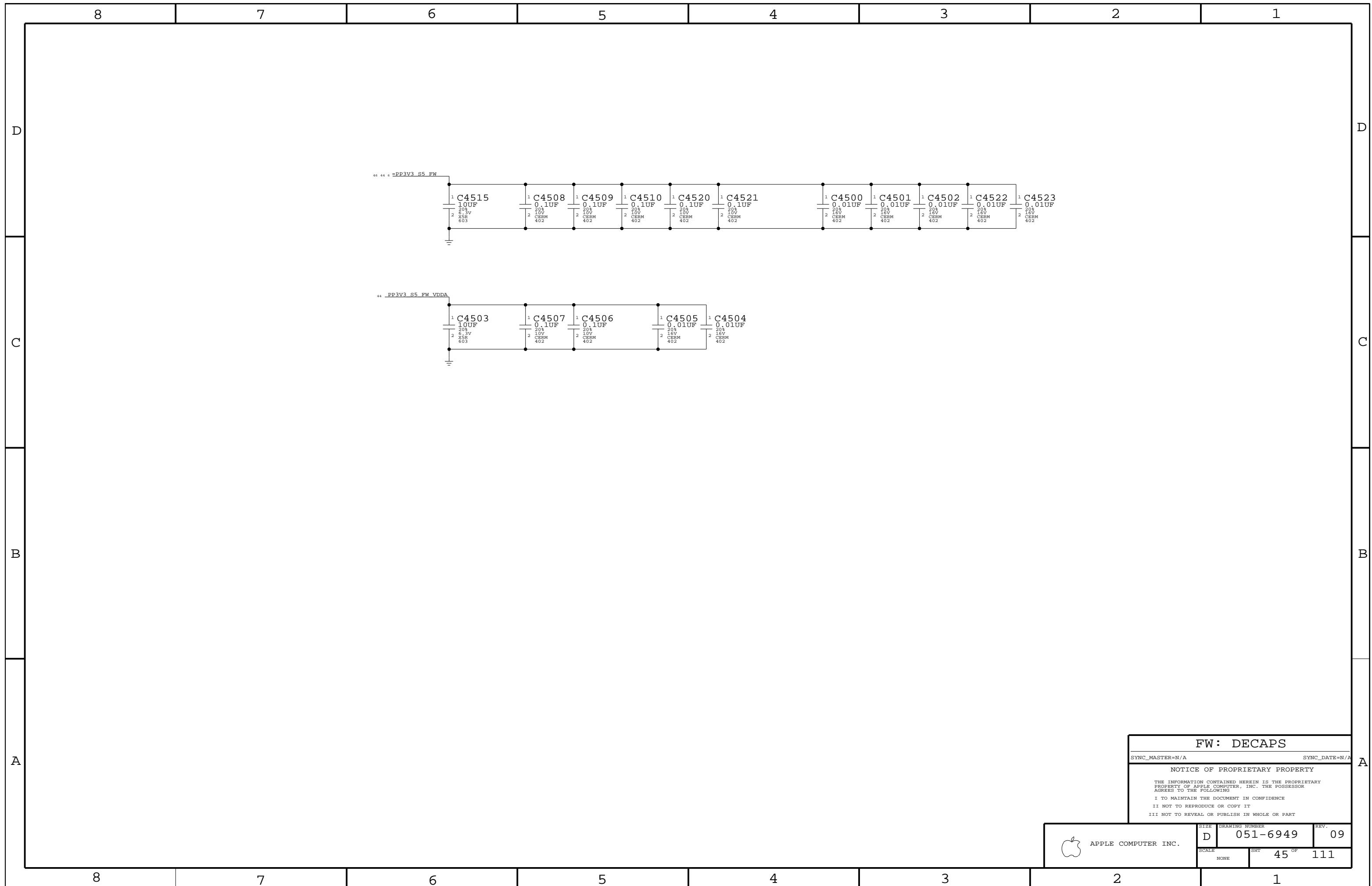
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| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 44 OF 111 | |



FW: DECAPS

SYNC_MASTER=N/A SYNC_DATE=N/A

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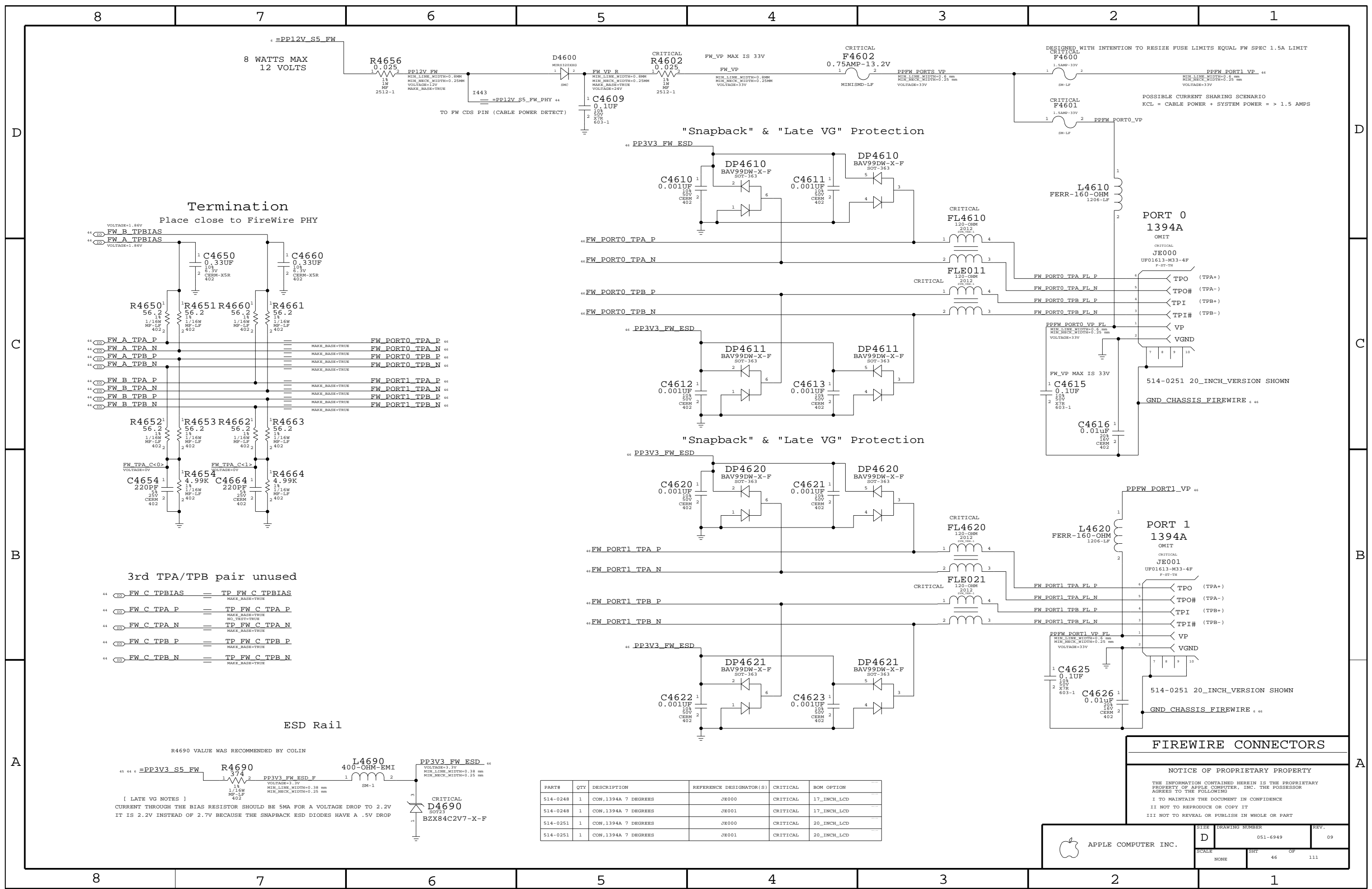
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| | SCALE | SHT | OF |
| | NONE | 45 | 111 |



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail

R4690 VALUE WAS RECOMMENDED BY COLIN

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------------|-------------------------|----------|-------------|
| 514-0248 | 1 | CON, 1394A 7 DEGREES | JE000 | CRITICAL | 17_INCH_LCD |
| 514-0248 | 1 | CON, 1394A 7 DEGREES | JE001 | CRITICAL | 17_INCH_LCD |
| 514-0251 | 1 | CON, 1394A 7 DEGREES | JE000 | CRITICAL | 20_INCH_LCD |
| 514-0251 | 1 | CON, 1394A 7 DEGREES | JE001 | CRITICAL | 20_INCH_LCD |

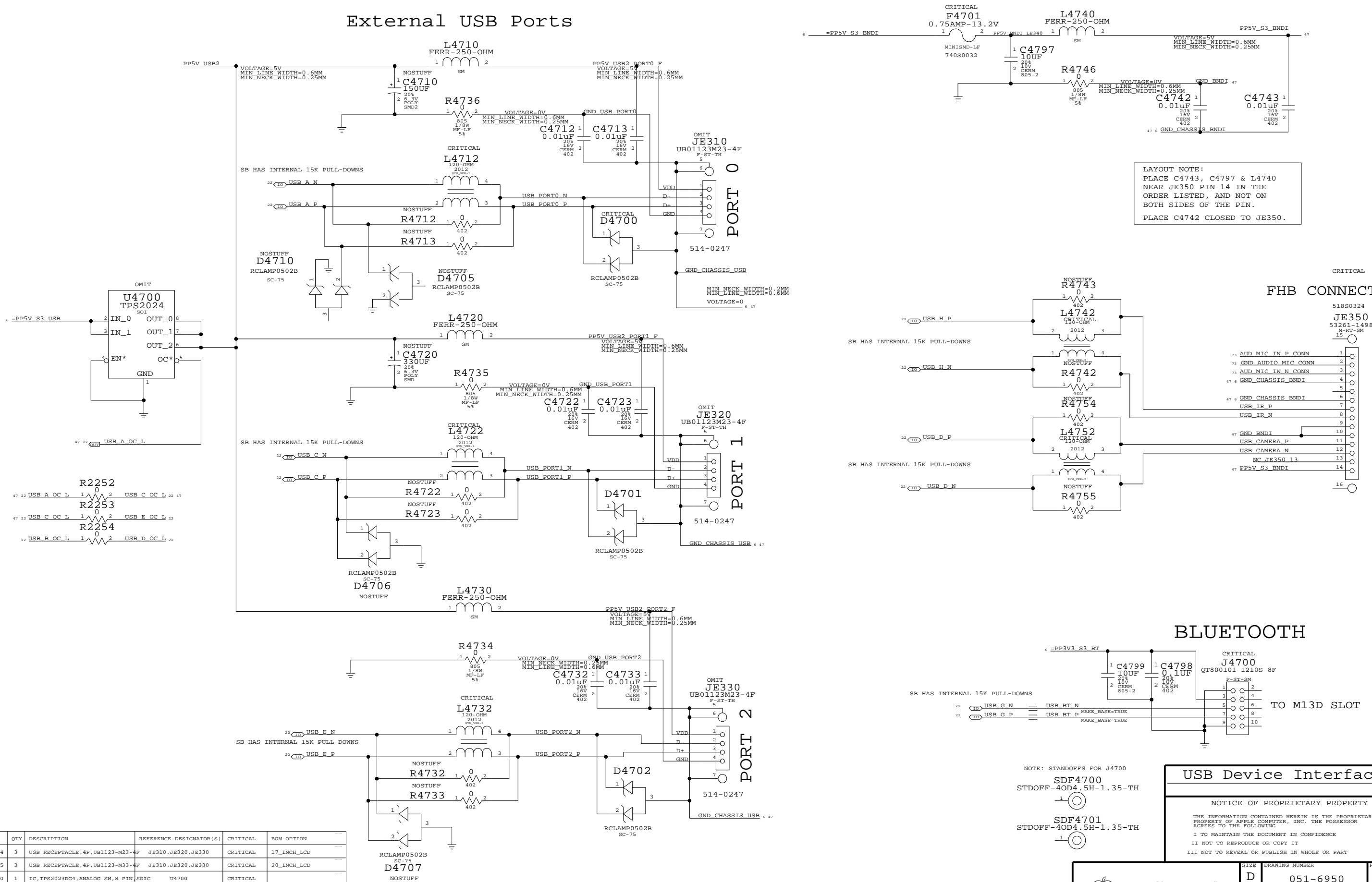
FIREWIRE CONNECTORS

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|---------------------|-------------|--------------------------|----------|
| APPLE COMPUTER INC. | SIZE: D | DRAWING NUMBER: 051-6949 | REV.: 09 |
| | SCALE: NONE | SHEET: 46 | OF: 111 |

External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE350 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE350.

NOTE: STANDOFFS FOR J4700
 SDF4700
 STDOFF-40D4.5H-1.35-TH
 SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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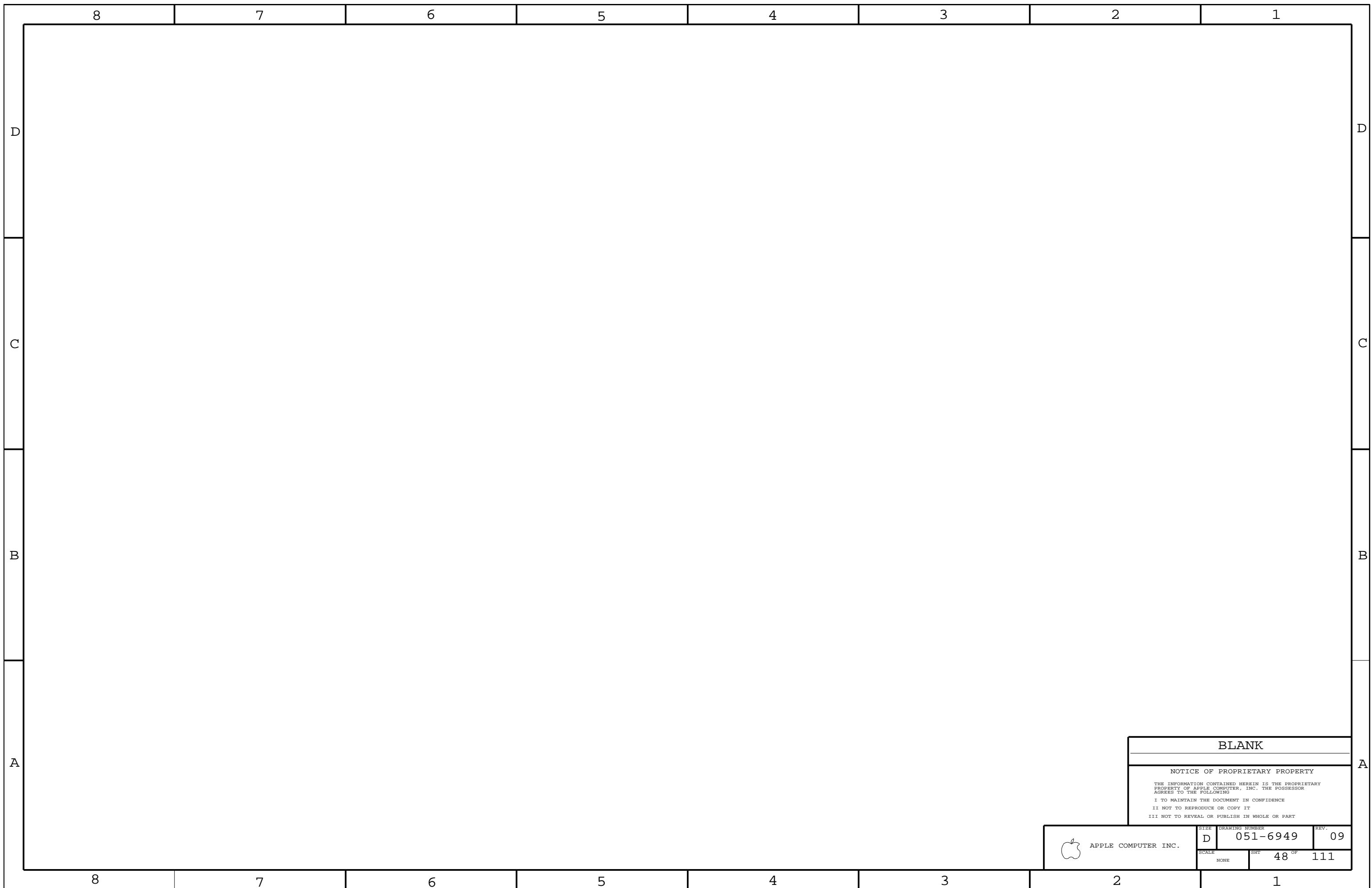
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
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| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|------------------------------------|-------------------------|----------|-------------|
| 514-0294 | 3 | USB RECEPTACLE,4P,UB1123-M23-4F | JE310,JE320,JE330 | CRITICAL | 17_INCH_LCD |
| 514-0295 | 3 | USB RECEPTACLE,4P,UB1123-M33-4F | JE310,JE320,JE330 | CRITICAL | 20_INCH_LCD |
| 353S1370 | 1 | IC,TPS2023DG4,ANALOG SW,8 PIN,SOIC | U4700 | CRITICAL | |

APPLE COMPUTER INC.

DRAWING NUMBER: D 051-6950 REV. 06

SCALE: NONE SHEET 47 OF 111



8

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NOTICE OF PROPRIETARY PROPERTY

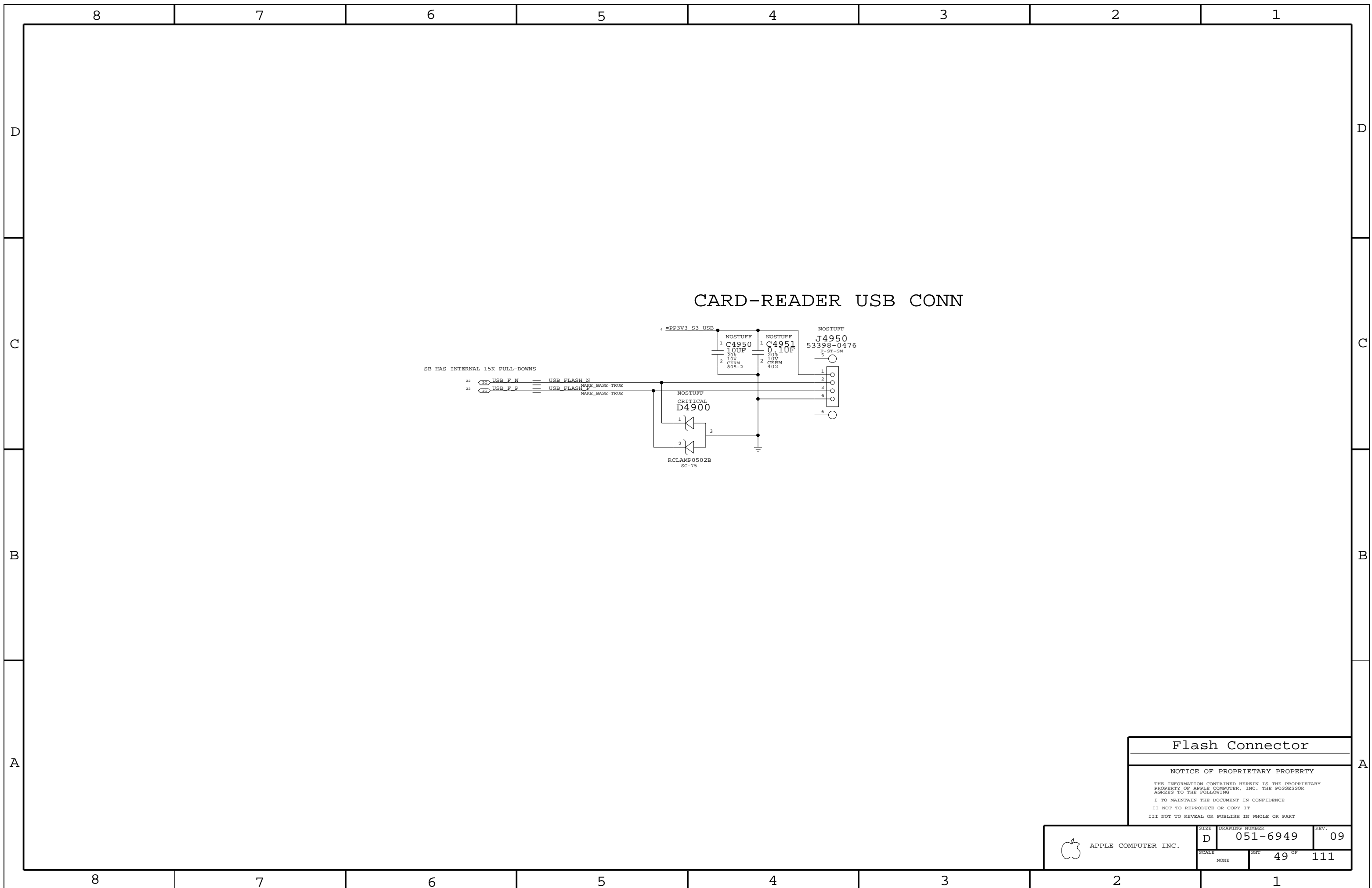
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|  APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 48 OF | TOTAL SHEETS 111 |



CARD-READER USB CONN

Flash Connector

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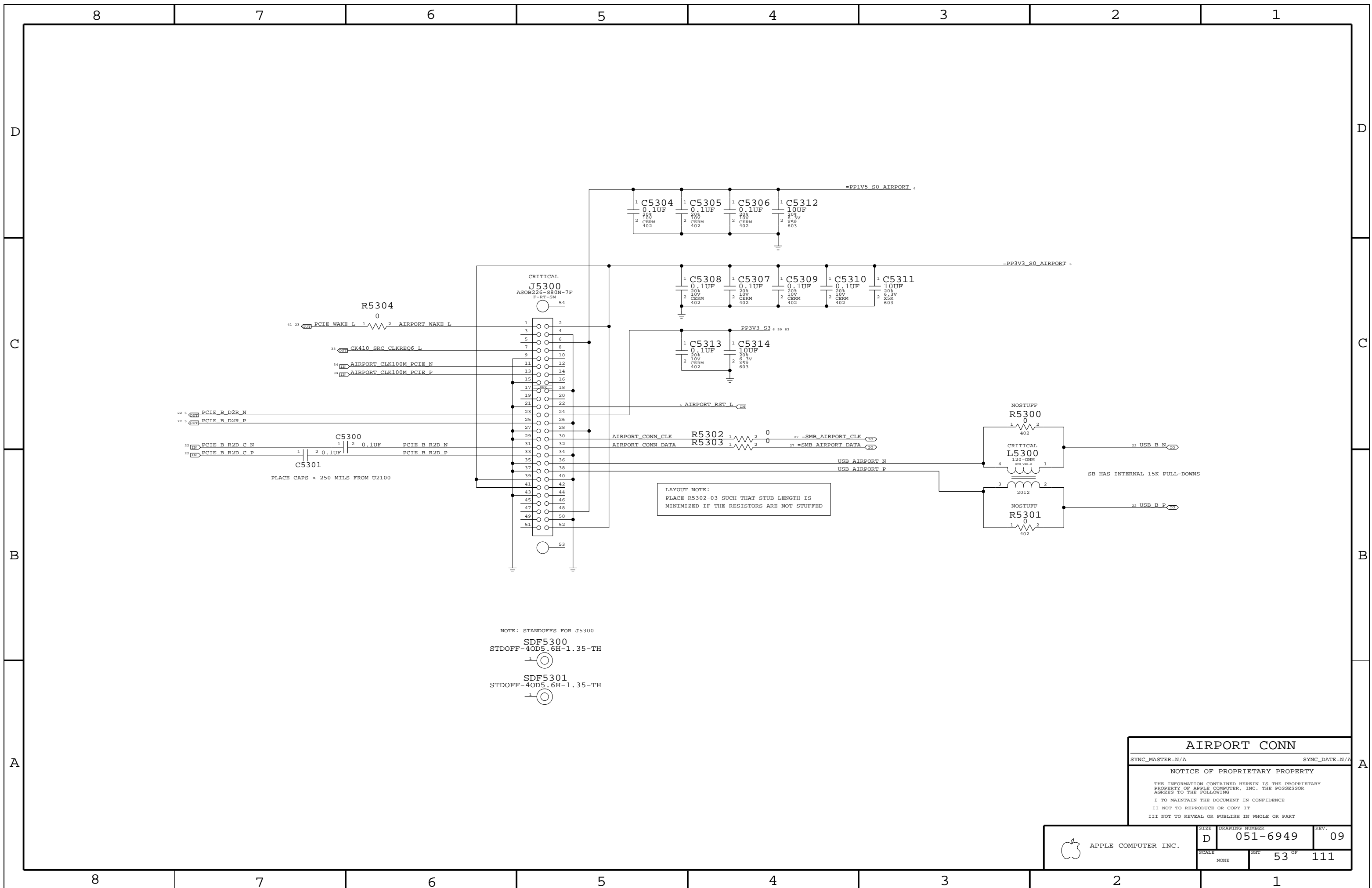
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| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 49 OF 111 | |



LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300

SDF5300
 STDOFF-4OD5.6H-1.35-TH

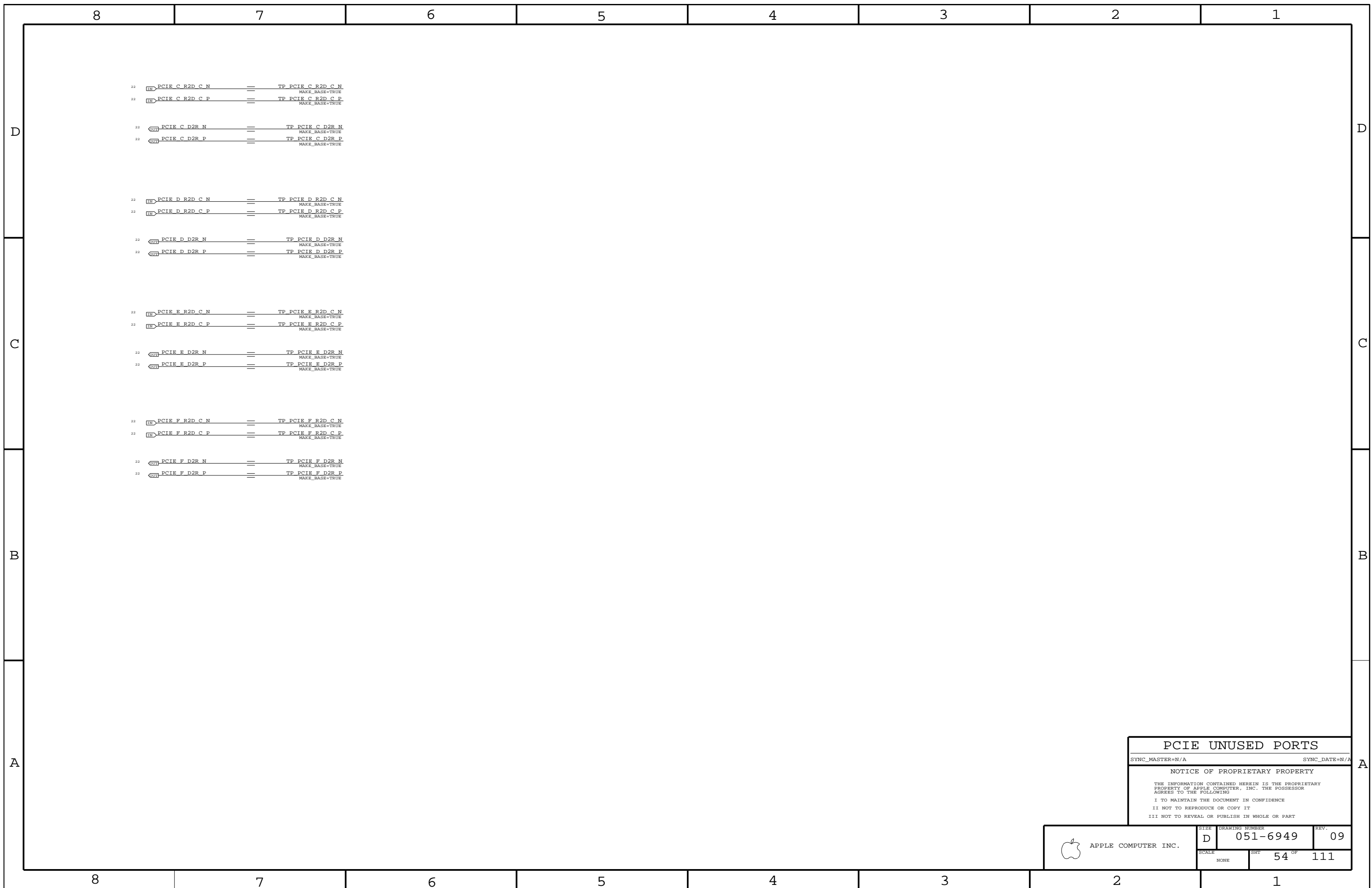


SDF5301
 STDOFF-4OD5.6H-1.35-TH



AIRPORT CONN
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | OF | |
| NONE | 53 | 111 | |



22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE

22 PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE

22 PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE

22 PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22 PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22 PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

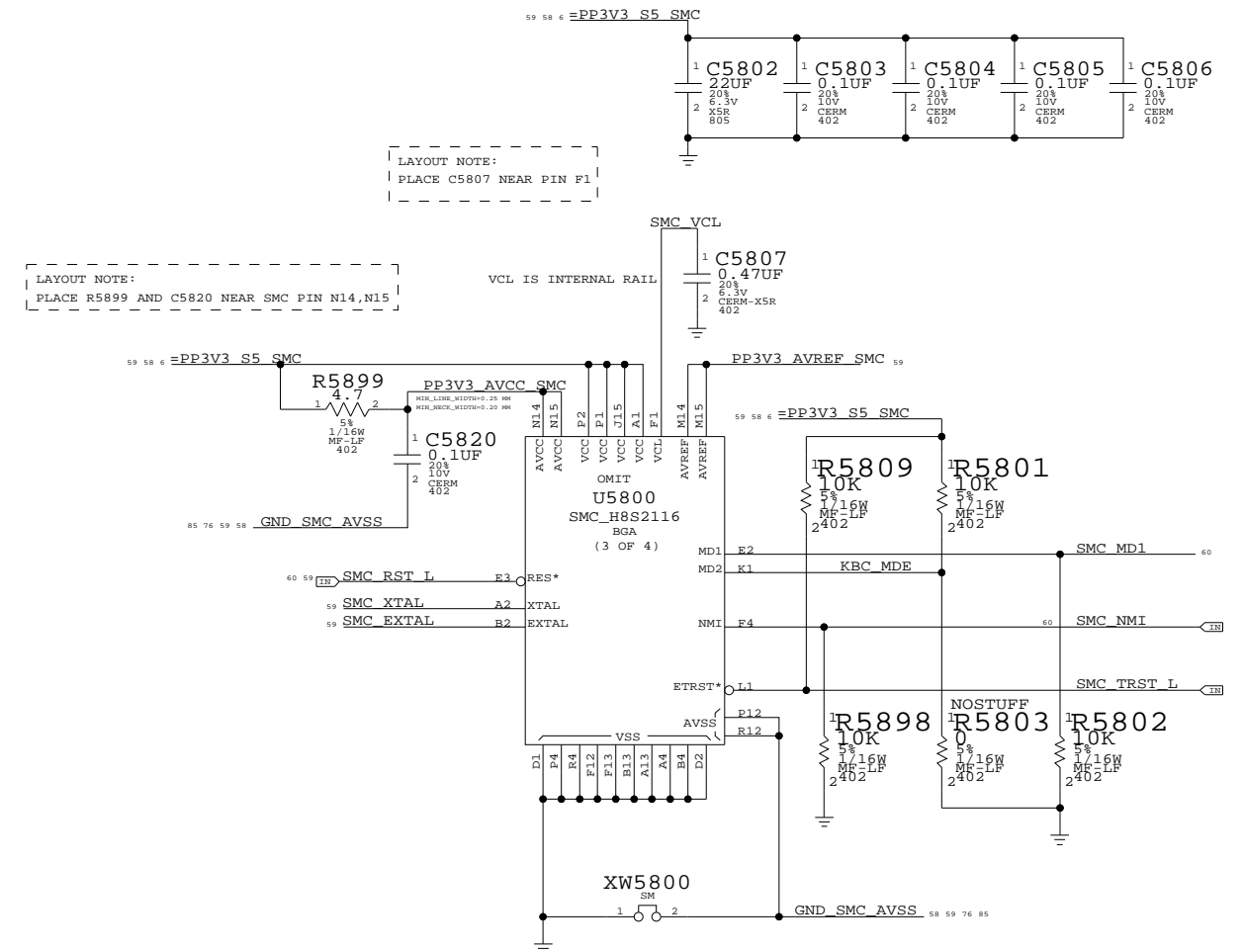
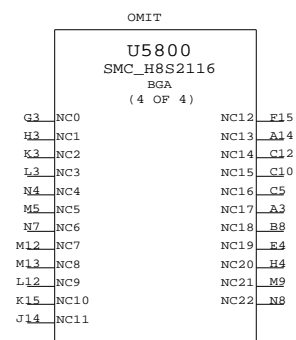
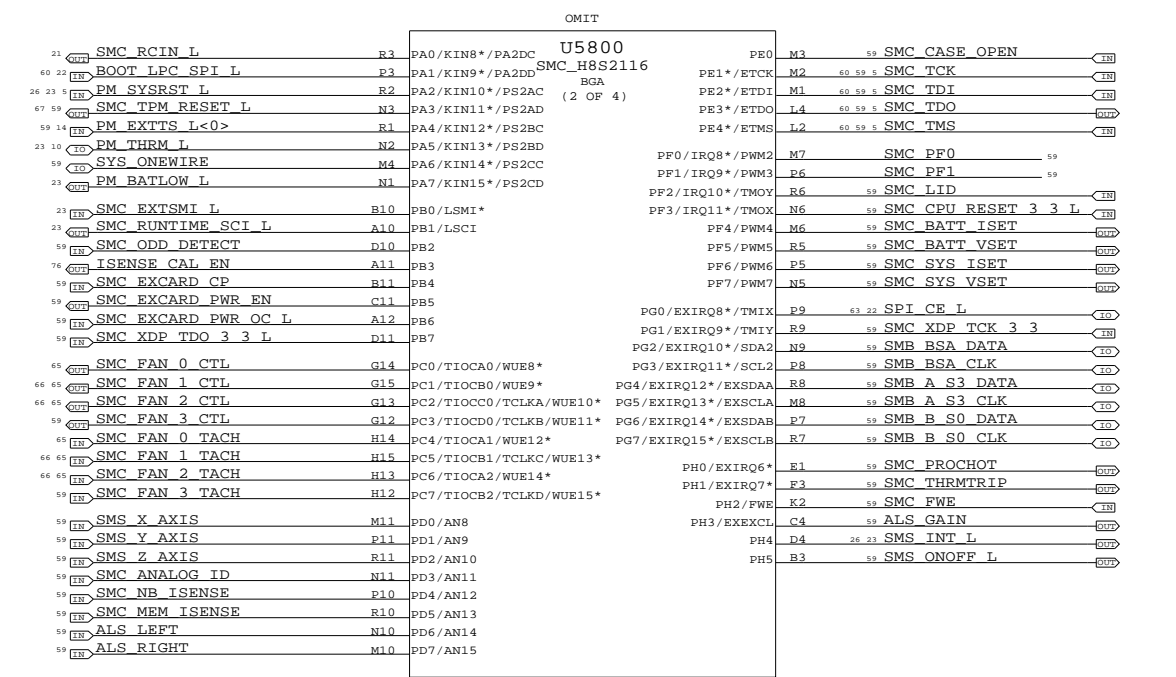
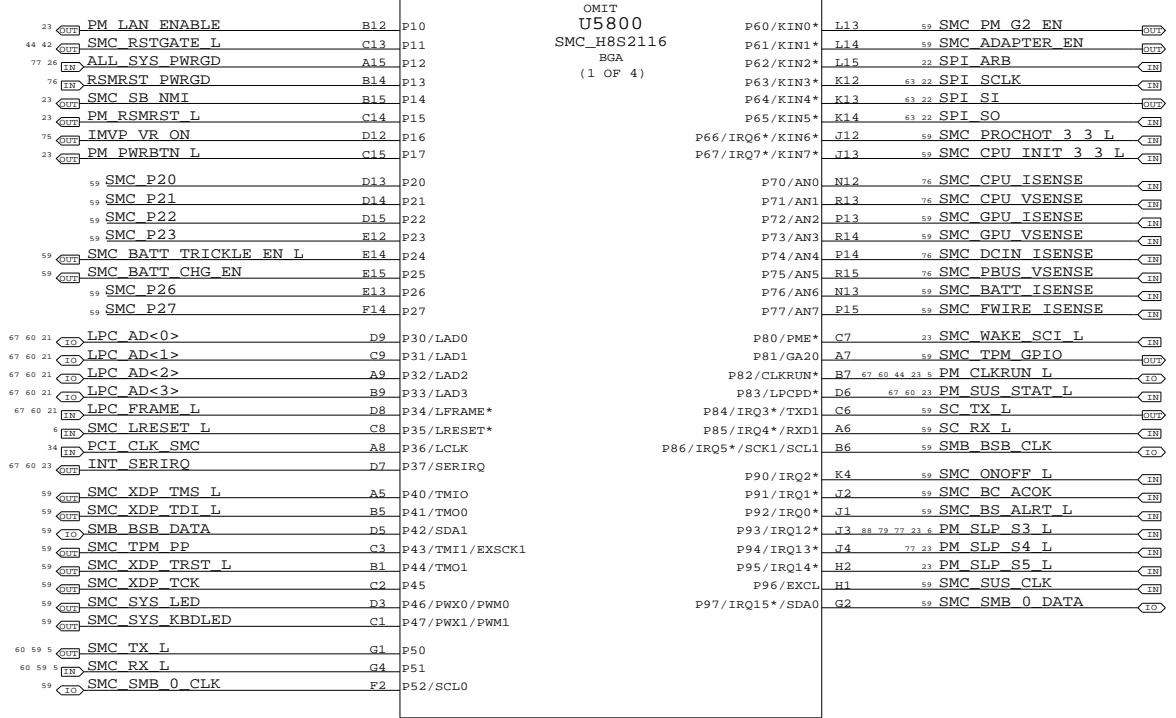
22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

PCIE UNUSED PORTS
 SYNC_MASTER=N/A SYNC_DATE=N/A
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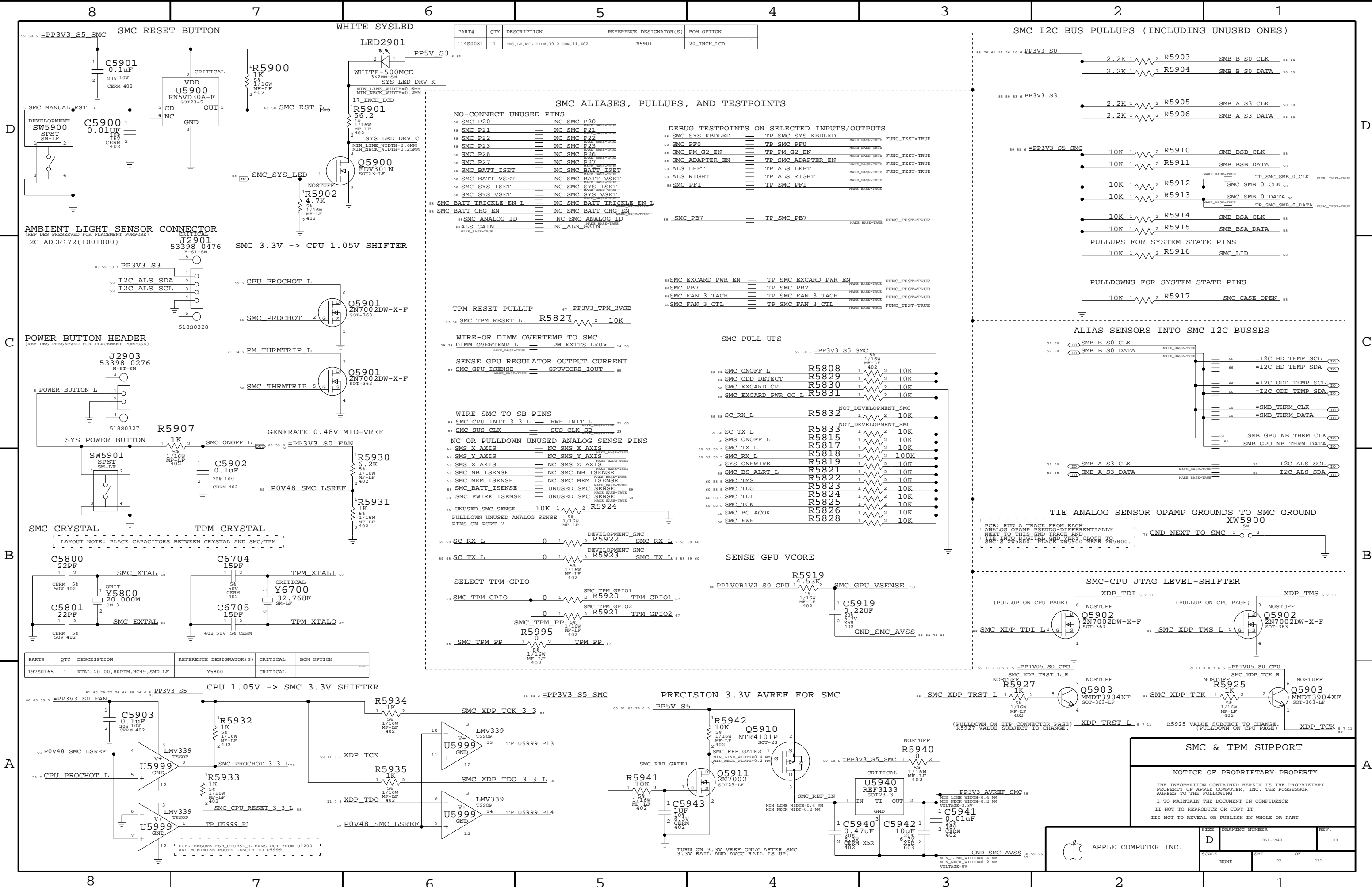
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| | D | 051-6949 | 09 |
| SCALE | SHT | | OF |
| NONE | 54 | | 111 |

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC
 SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC. DRAWING NUMBER 051-6949 REV. 09
 SCALE NONE SHEET 58 OF 111



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|----------|-----|---------------------------------|-------------------------|-------------|
| 11450081 | 1 | RES,LP,WTL FILM,39.2 OHM,14,402 | R5901 | 20_INCH_LCD |

SMC ALIASES, PULLUPS, AND TESTPOINTS

| NO-CONNECT UNUSED PINS | DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS |
|--|--|
| 58 SMC P20 == NC SMC P20 | 58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE |
| 58 SMC P21 == NC SMC P21 | 58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE |
| 58 SMC P22 == NC SMC P22 | 58 SMC PM_G2_EN == TP_PM_G2_EN MAKE_BASE=TRUE |
| 58 SMC P23 == NC SMC P23 | 58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE |
| 58 SMC P26 == NC SMC P26 | 58 ALS_LEFT == TP_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE |
| 58 SMC P27 == NC SMC P27 | 58 ALS_RIGHT == TP_ALS_RIGHT MAKE_BASE=TRUE FUNC_TEST=TRUE |
| 58 SMC_BATT_ISET == NC SMC_BATT_ISET | 58 SMC_PF1 == TP_SMC_PF1 MAKE_BASE=TRUE |
| 58 SMC_BATT_VSET == NC SMC_BATT_VSET | |
| 58 SMC_SYS_ISET == NC SMC_SYS_ISET | |
| 58 SMC_SYS_VSET == NC SMC_SYS_VSET | |
| 58 SMC_BATT_TRICKLE_EN_L == NC SMC_BATT_TRICKLE_EN_L | 59 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE |
| 58 SMC_BATT_CHG_EN == NC SMC_BATT_CHG_EN | |
| 58 SMC_ANALOG_ID == NC SMC_ANALOG_ID | |
| 58 ALS_GAIN == NC ALS_GAIN | |

SMC PULL-UPS

| | | |
|------------------------|-------|------|
| 58 SMC_ONOFF_L | R5808 | 10K |
| 58 SMC_ODD_DETECT | R5829 | 10K |
| 58 SMC_EXCARD_CP | R5830 | 10K |
| 58 SMC_EXCARD_PWR_OC_L | R5831 | 10K |
| 58 SC_RX_L | R5832 | 10K |
| 58 SC_TX_L | R5833 | 10K |
| 58 SMS_ONOFF_L | R5815 | 10K |
| 58 SMC_TX_L | R5817 | 10K |
| 58 SMC_RX_L | R5818 | 100K |
| 58 SYS_ONEWIRE | R5819 | 10K |
| 58 SMC_BS_ALERT_L | R5821 | 10K |
| 58 SMC_TMS | R5822 | 10K |
| 58 SMC_TDO | R5823 | 10K |
| 58 SMC_TDI | R5824 | 10K |
| 58 SMC_TCK | R5825 | 10K |
| 58 SMC_BC_ACOK | R5826 | 10K |
| 58 SMC_FWE | R5828 | 10K |

WIRE SMC TO SB PINS

| | |
|-----------------------|------------------------------|
| 58 SMC_CPU_INIT_3_3_L | FWH_INIT_L |
| 58 SMC_SUS_CLK | SUS_CLK_SB |
| 58 SMC_TPM_GPIO | SMC_TPM_GPIO1, SMC_TPM_GPIO2 |
| 58 SMC_TPM_PP | SMC_TPM_PP |

SELECT TPM GPIO

| | | |
|------------------|-------|-----------|
| 58 SMC_TPM_GPIO1 | R5920 | TPM_GPIO1 |
| 58 SMC_TPM_GPIO2 | R5921 | TPM_GPIO2 |
| 58 SMC_TPM_PP | R5995 | TPM_PP |

WIRE SMC TO SB PINS (continued)

| | |
|-----------------------|------------------------------|
| 58 SMC_CPU_INIT_3_3_L | FWH_INIT_L |
| 58 SMC_SUS_CLK | SUS_CLK_SB |
| 58 SMC_TPM_GPIO | SMC_TPM_GPIO1, SMC_TPM_GPIO2 |
| 58 SMC_TPM_PP | SMC_TPM_PP |

WIRE SMC TO SB PINS (continued)

| | |
|-----------------------|------------------------------|
| 58 SMC_CPU_INIT_3_3_L | FWH_INIT_L |
| 58 SMC_SUS_CLK | SUS_CLK_SB |
| 58 SMC_TPM_GPIO | SMC_TPM_GPIO1, SMC_TPM_GPIO2 |
| 58 SMC_TPM_PP | SMC_TPM_PP |

WIRE SMC TO SB PINS (continued)

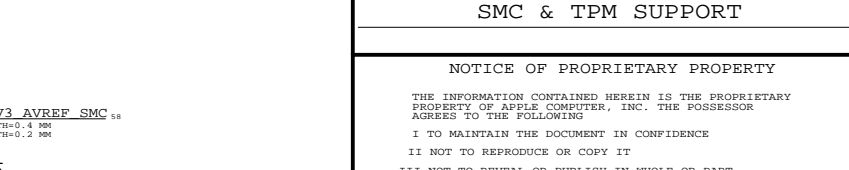
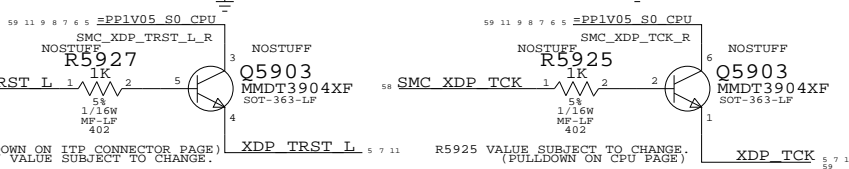
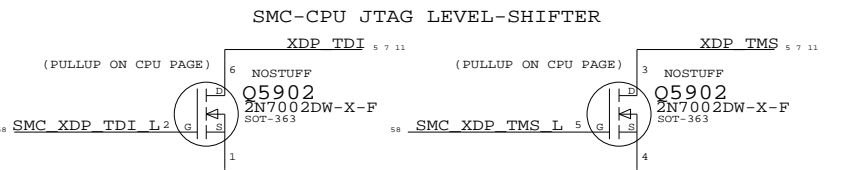
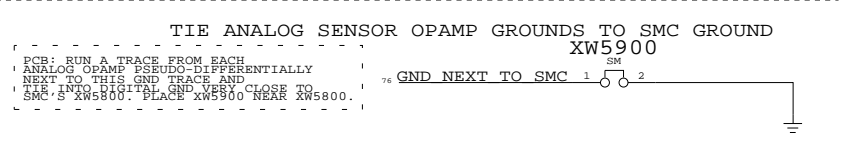
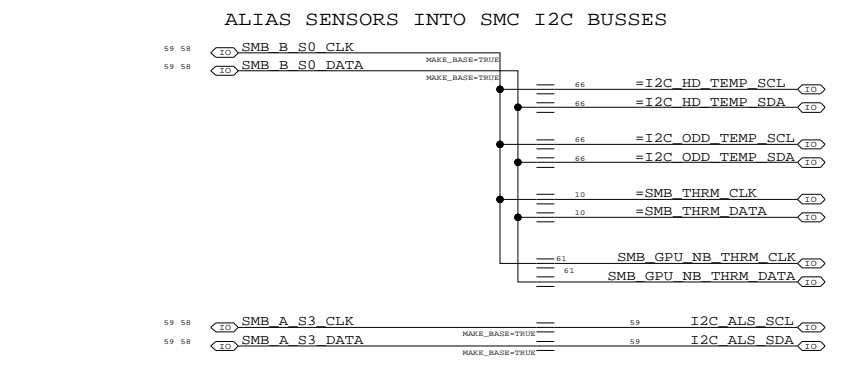
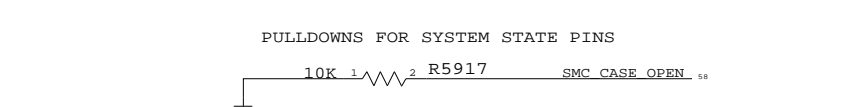
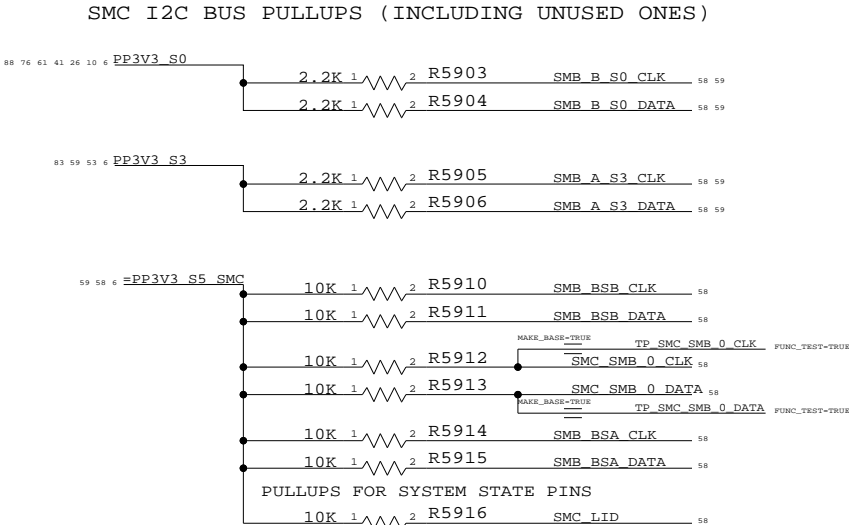
| | |
|-----------------------|------------------------------|
| 58 SMC_CPU_INIT_3_3_L | FWH_INIT_L |
| 58 SMC_SUS_CLK | SUS_CLK_SB |
| 58 SMC_TPM_GPIO | SMC_TPM_GPIO1, SMC_TPM_GPIO2 |
| 58 SMC_TPM_PP | SMC_TPM_PP |

WIRE SMC TO SB PINS (continued)

| | |
|-----------------------|------------------------------|
| 58 SMC_CPU_INIT_3_3_L | FWH_INIT_L |
| 58 SMC_SUS_CLK | SUS_CLK_SB |
| 58 SMC_TPM_GPIO | SMC_TPM_GPIO1, SMC_TPM_GPIO2 |
| 58 SMC_TPM_PP | SMC_TPM_PP |

WIRE SMC TO SB PINS (continued)

| | |
|-----------------------|------------------------------|
| 58 SMC_CPU_INIT_3_3_L | FWH_INIT_L |
| 58 SMC_SUS_CLK | SUS_CLK_SB |
| 58 SMC_TPM_GPIO | SMC_TPM_GPIO1, SMC_TPM_GPIO2 |
| 58 SMC_TPM_PP | SMC_TPM_PP |

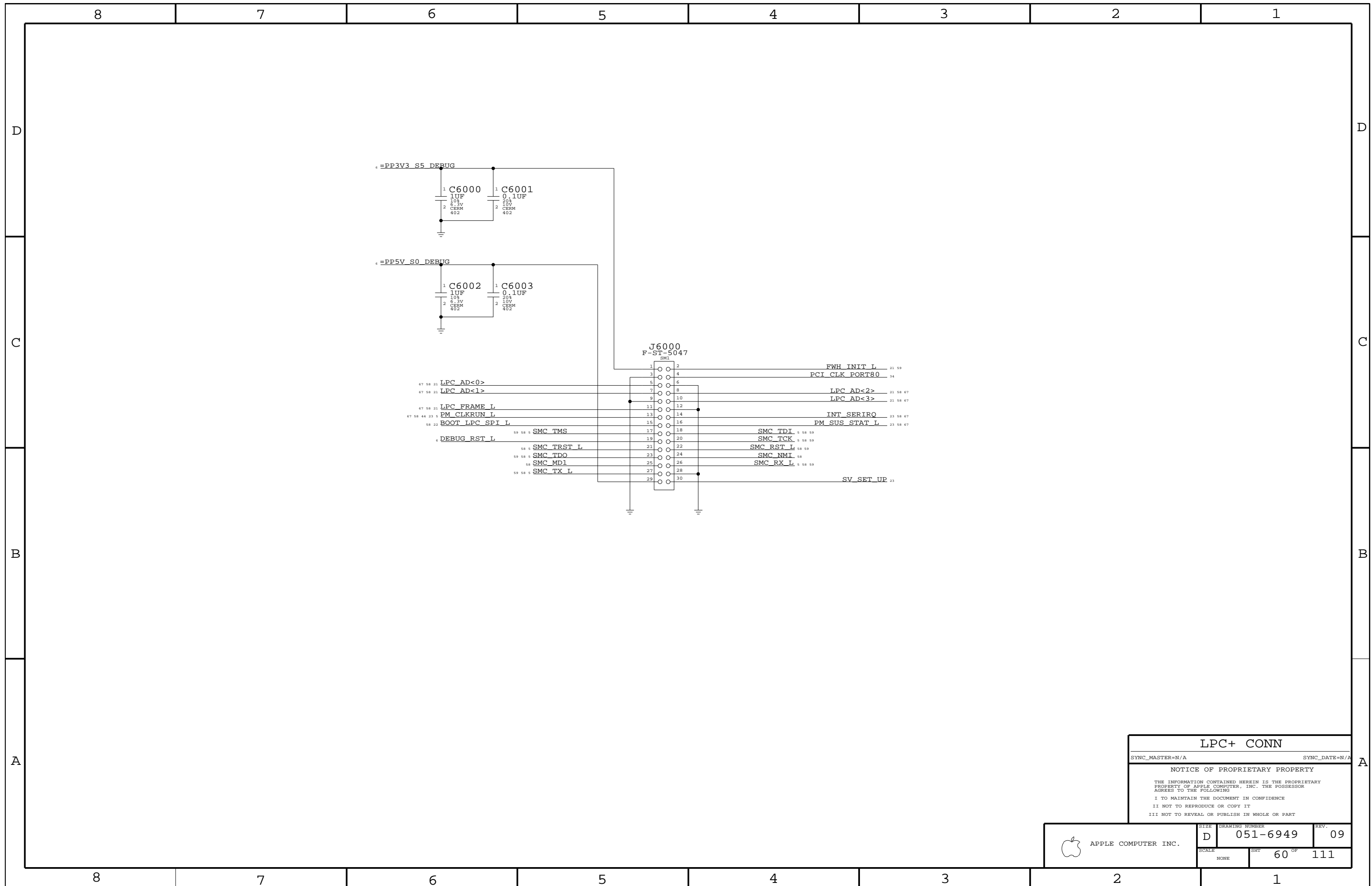


| SIZE | DRAWING NUMBER | REV. |
|------|----------------|------|
| D | 051-6949 | 09 |

SCALE: NONE

SHEET: 59 OF 111

APPLE COMPUTER INC.



LPC+ CONN

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

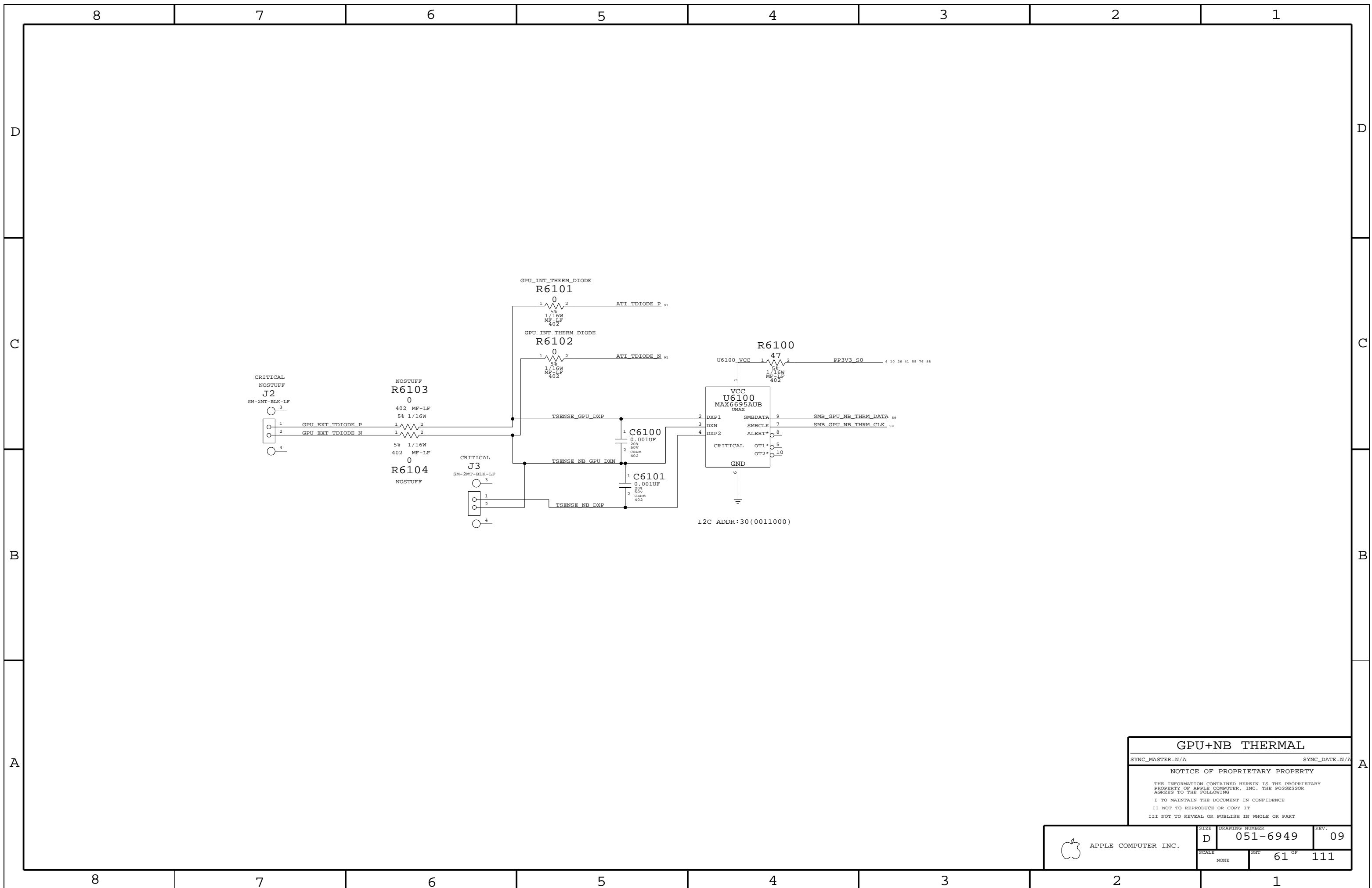
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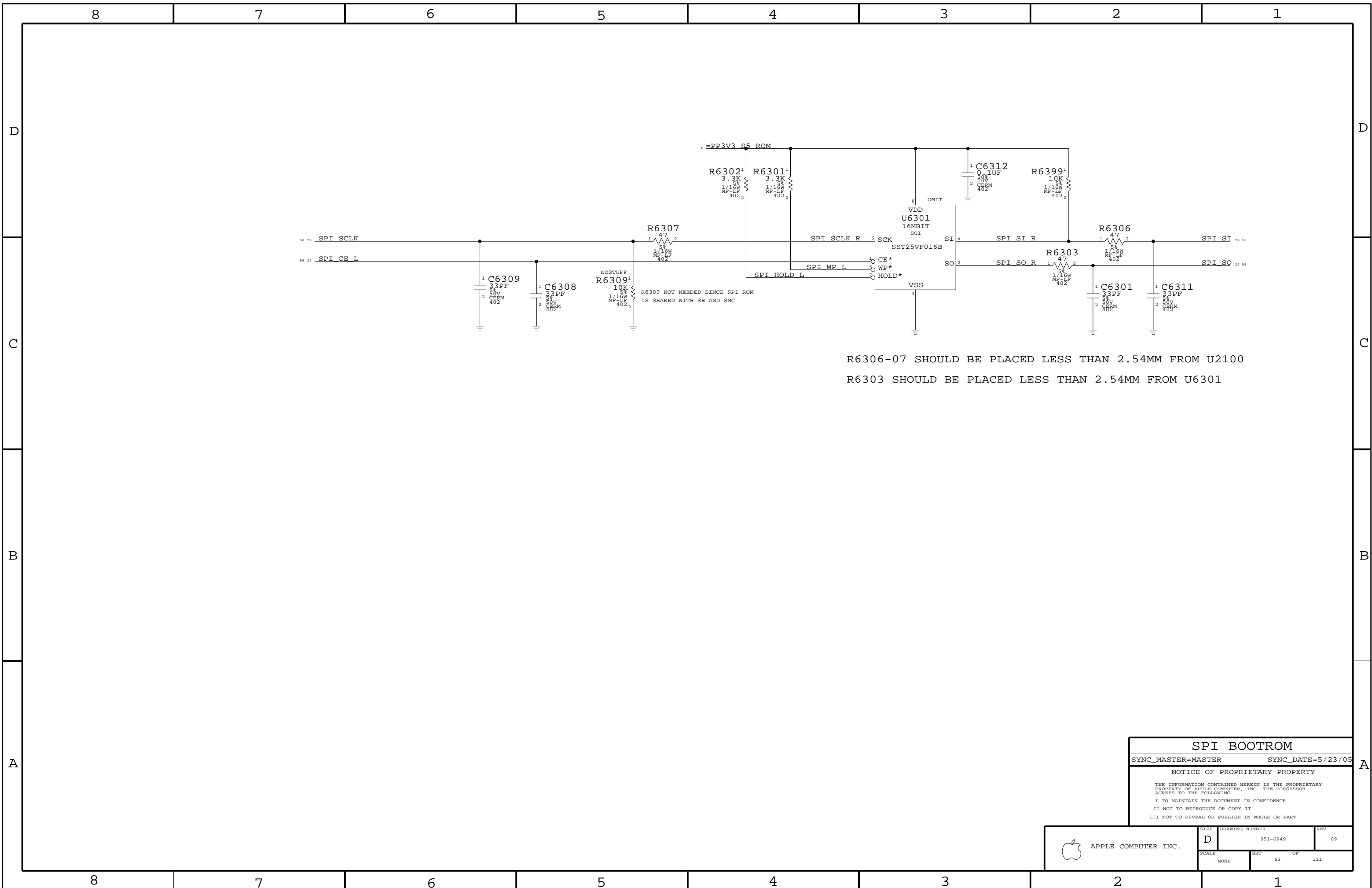
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

| | | | |
|---------------------|------------------|-----------------------------------|-------------------|
| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 60 OF 111 | |



GPU+NB THERMAL
 SYNC_MASTER=N/A SYNC_DATE=N/A
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | 61 OF | 111 |
| NONE | | | |



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

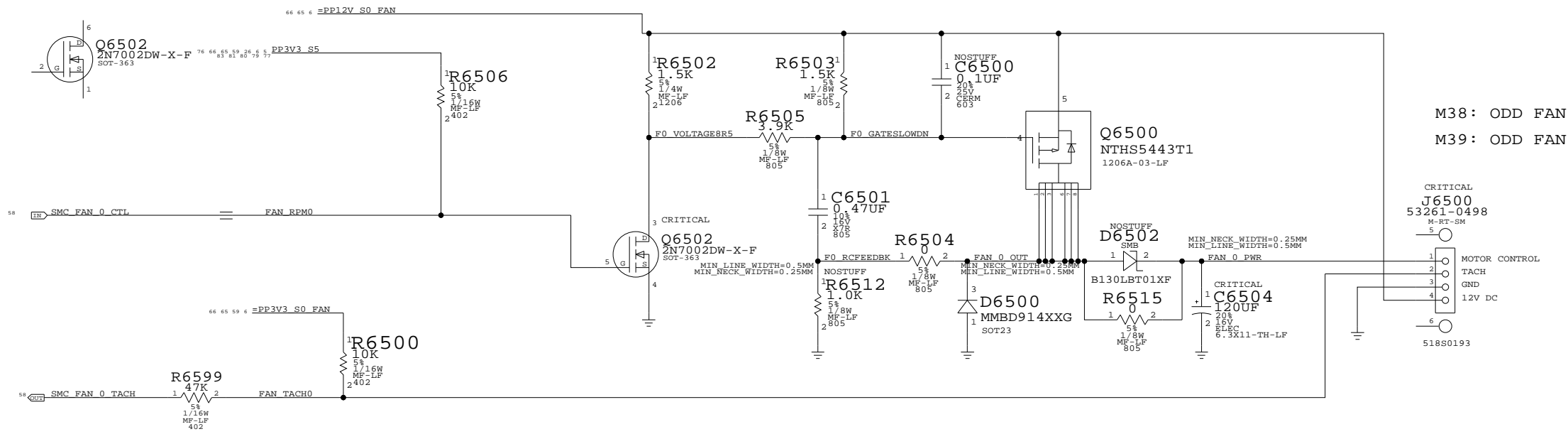
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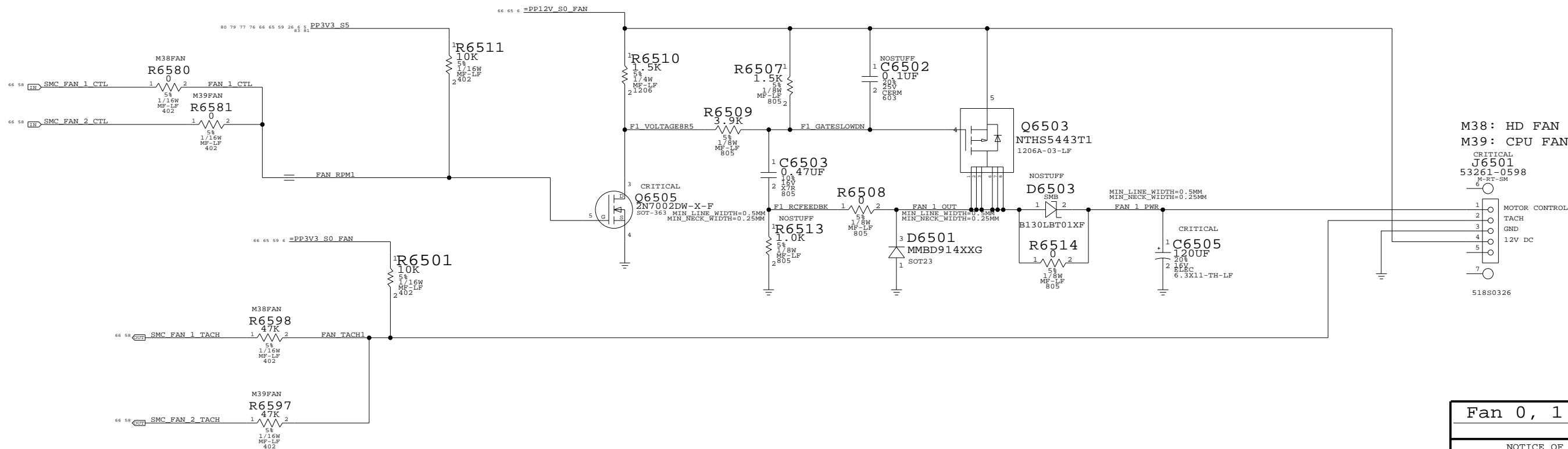
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| | | | |
|---------------------|------------------|----------------------------|------------|
| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 63 | OF 111 |

FAN 0



FAN 1

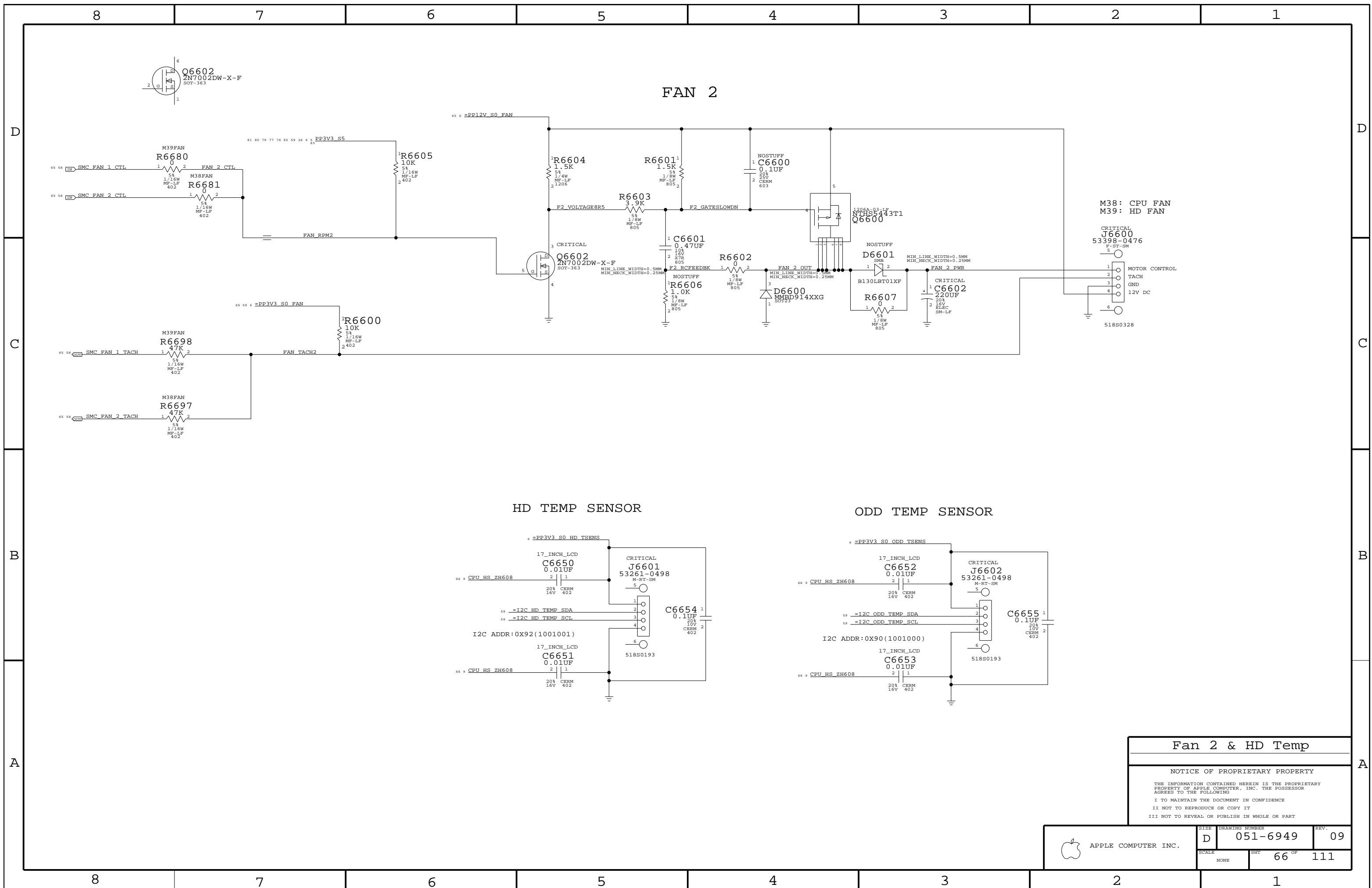


Fan 0, 1 & System Temp

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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | NONE | SHT | OF |
| | | 65 | 111 |



FAN 2

HD TEMP SENSOR

ODD TEMP SENSOR

Fan 2 & HD Temp

NOTICE OF PROPRIETARY PROPERTY

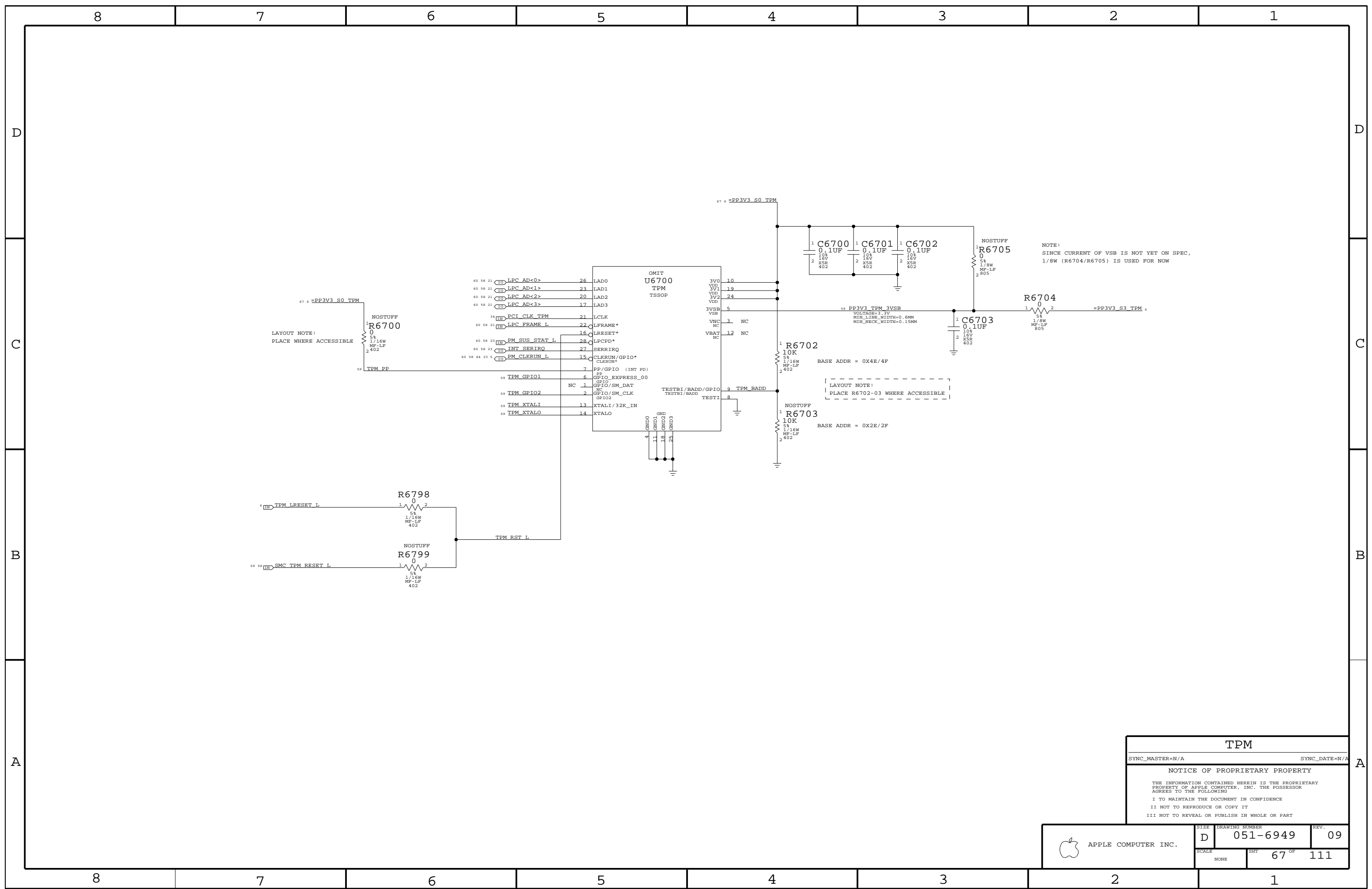
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|---------------------|---------------|-----------------------------------|-------------------|
| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 66 OF 111 | |



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=N/A SYNC_DATE=N/A

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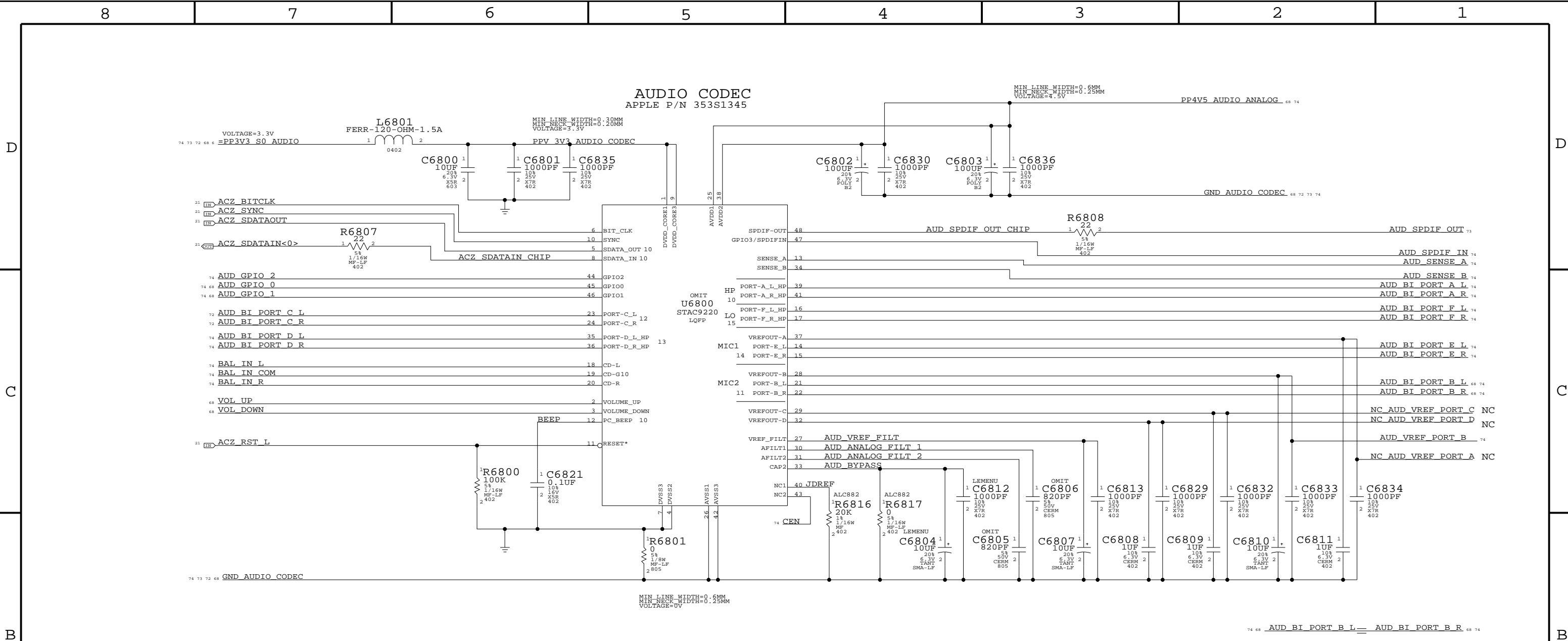
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | 67 OF | 111 |
| NONE | | | |

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

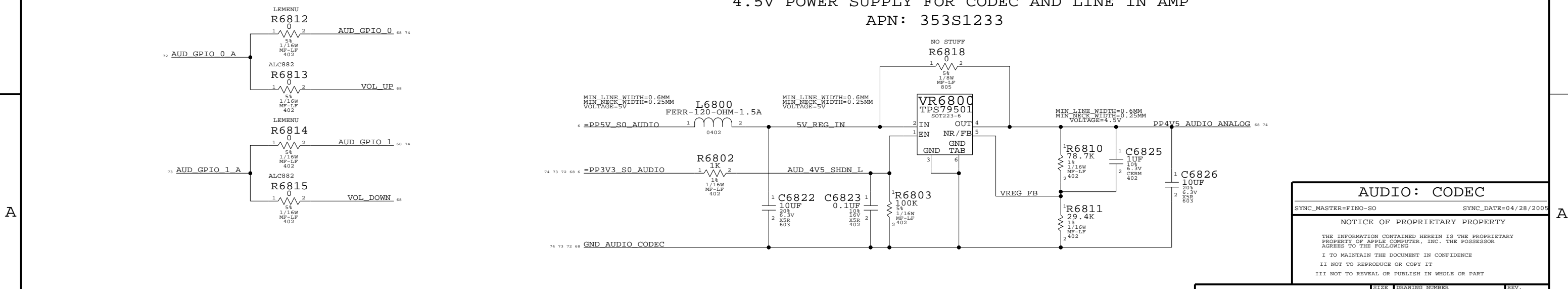
D
C
B
A

D
C
B
A



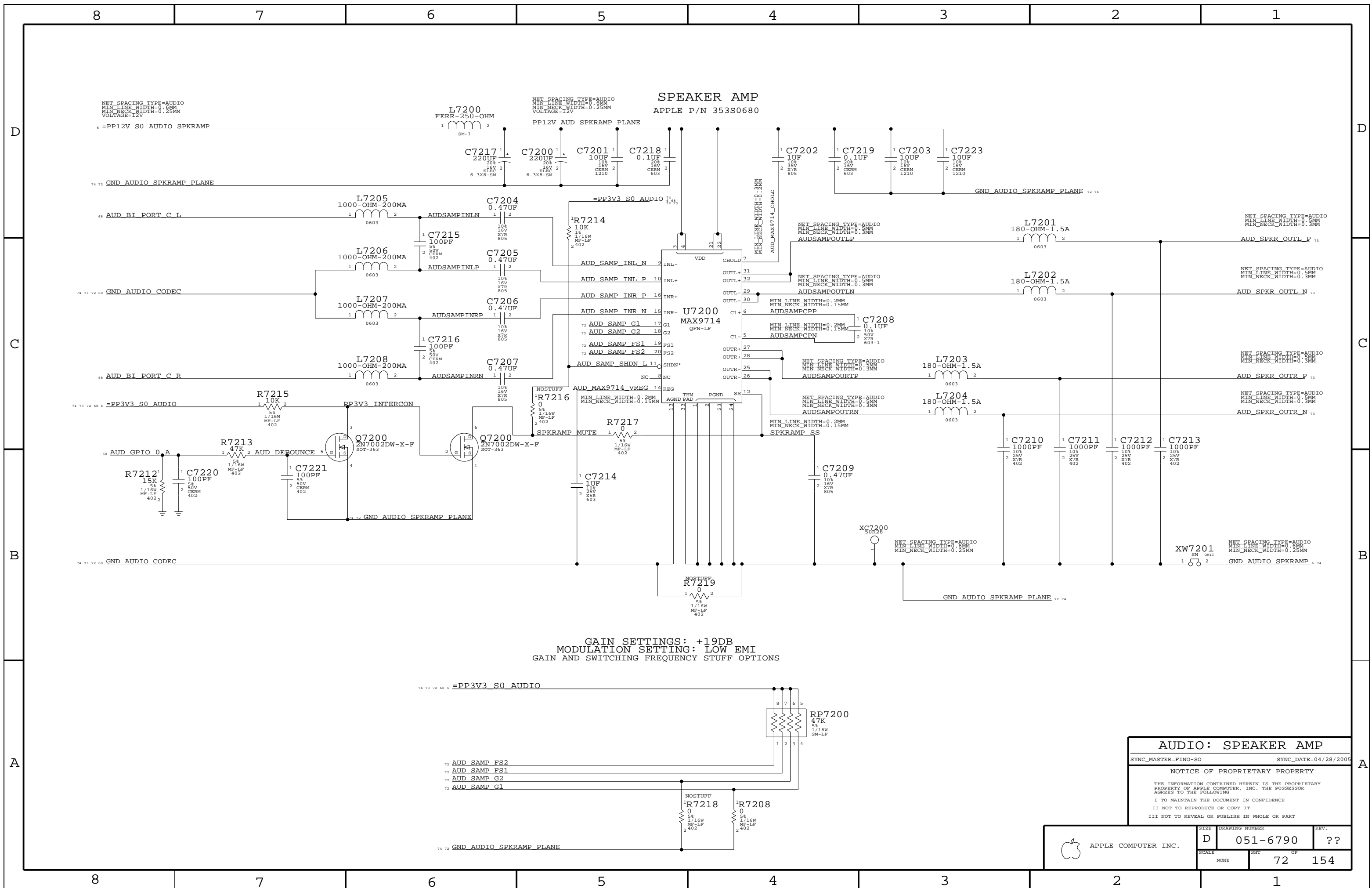
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

MIC INPUT TO BOTH L&R



| | |
|--|----------------------|
| AUDIO: CODEC | |
| SYNC_MASTER=FINO-SO | SYNC_DATE=04/28/2005 |
| NOTICE OF PROPRIETARY PROPERTY | |
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| | | | |
|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6790 | ?? |
| SCALE | SHT | OF | |
| NONE | 68 | 154 | |



SPEAKER AMP
APPLE P/N 353S0680

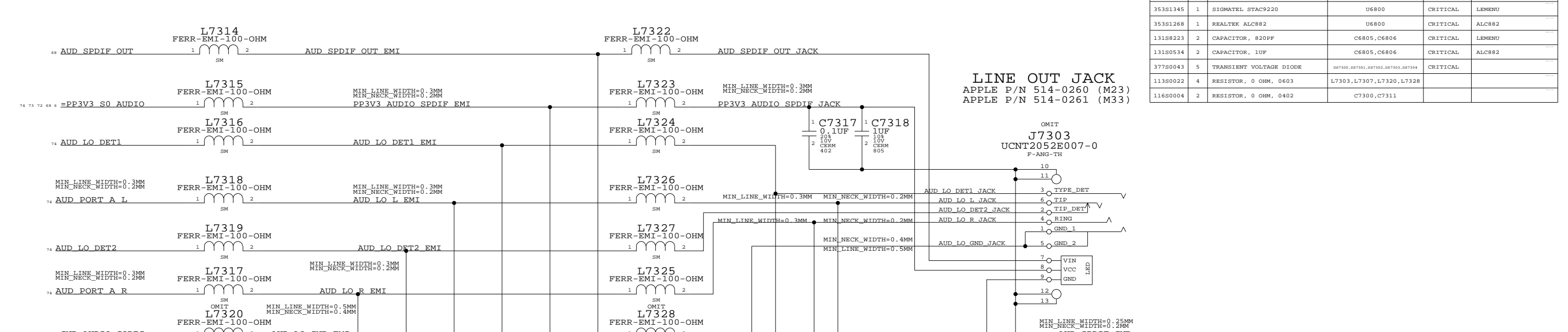
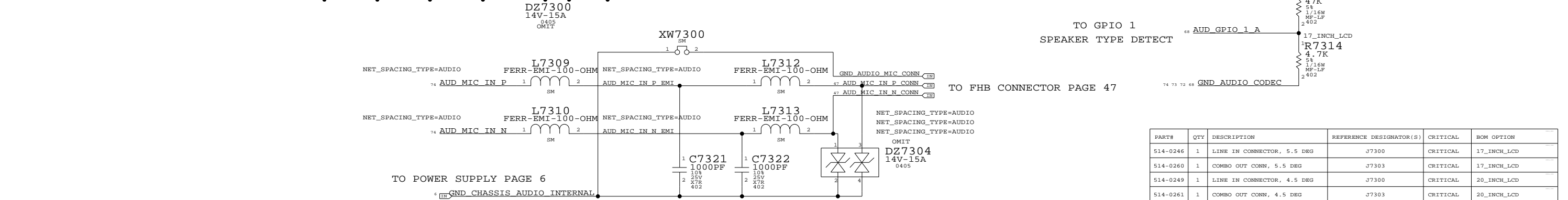
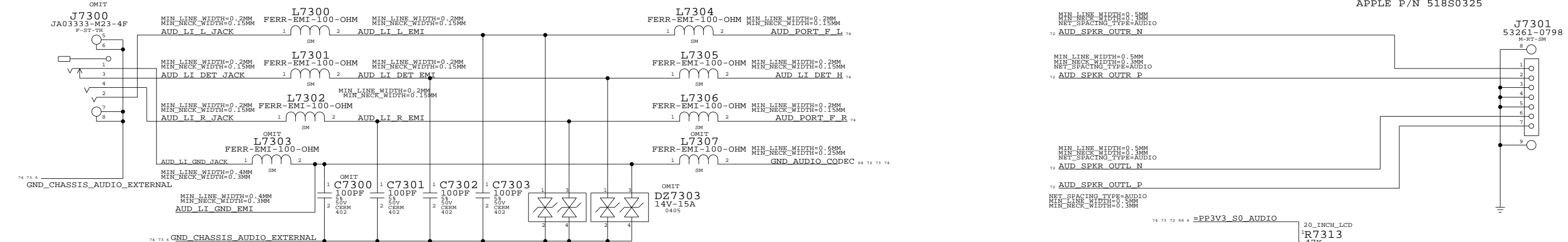
GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
 SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005
 NOTICE OF PROPRIETARY PROPERTY
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6790 | ?? |
| SCALE | NONE | SHT | OF |
| | | 72 | 154 |

LINE IN JACK
APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------------------|------------------------------------|----------|-------------|
| 514-0246 | 1 | LINE IN CONNECTOR, 5.5 DEG | J7300 | CRITICAL | 17_INCH_LCD |
| 514-0260 | 1 | COMBO OUT CONN, 5.5 DEG | J7303 | CRITICAL | 17_INCH_LCD |
| 514-0249 | 1 | LINE IN CONNECTOR, 4.5 DEG | J7300 | CRITICAL | 20_INCH_LCD |
| 514-0261 | 1 | COMBO OUT CONN, 4.5 DEG | J7303 | CRITICAL | 20_INCH_LCD |
| 353S1345 | 1 | SIGMATEL STAC9220 | U6800 | CRITICAL | LEMENU |
| 353S1268 | 1 | REALTEK ALC882 | U6800 | CRITICAL | ALC882 |
| 131S8223 | 2 | CAPACITOR, 820PF | C6805,C6806 | CRITICAL | LEMENU |
| 131S0534 | 2 | CAPACITOR, 1UF | C6805,C6806 | CRITICAL | ALC882 |
| 377S0043 | 5 | TRANSIENT VOLTAGE DIODE | DZ7300,DZ7301,DZ7302,DZ7303,DZ7304 | CRITICAL | |
| 113S0022 | 4 | RESISTOR, 0 OHM, 0603 | L7303,L7307,L7320,L7328 | | |
| 116S0004 | 2 | RESISTOR, 0 OHM, 0402 | C7300,C7311 | | |



AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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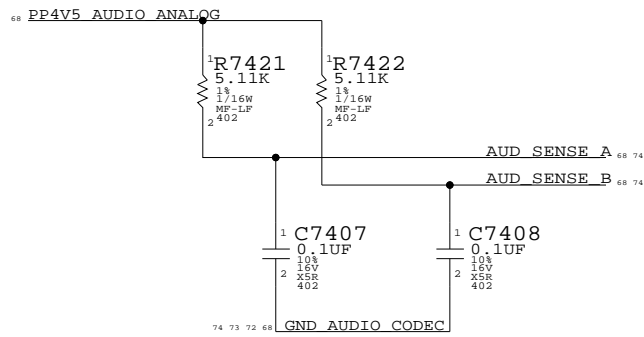
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SCALE: NONE SHEET: 73 OF 154

SIZE: DRAWING NUMBER: REV. D 051-6790 ??

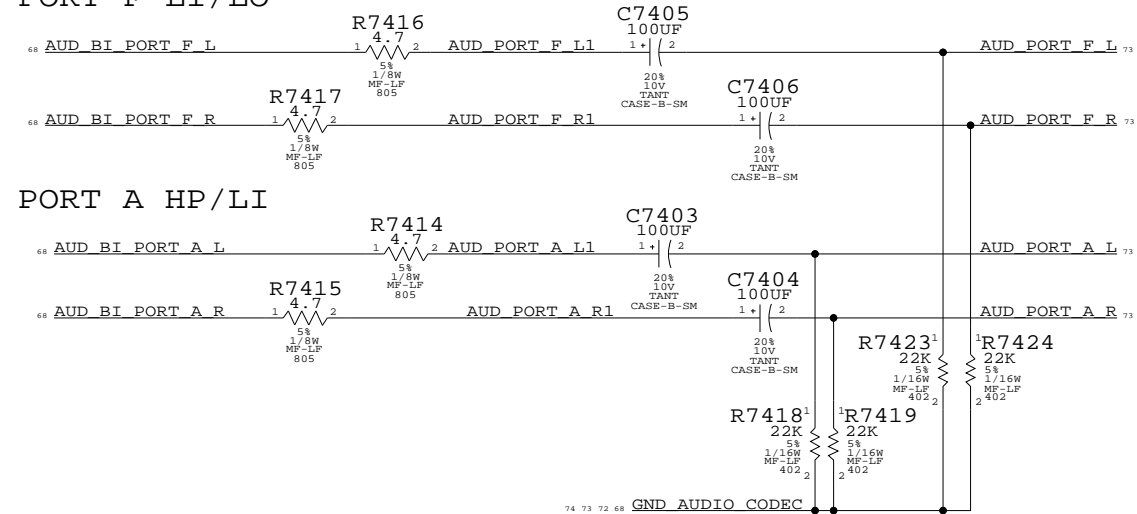
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



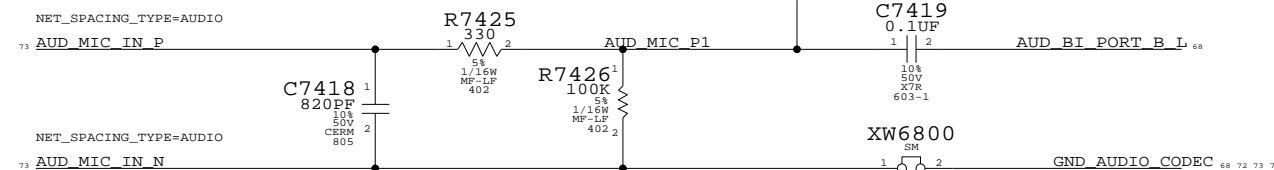
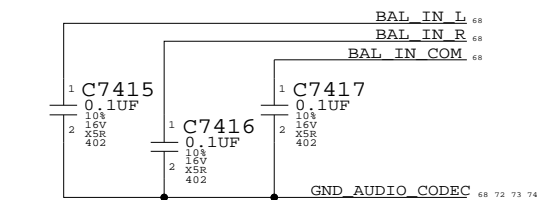
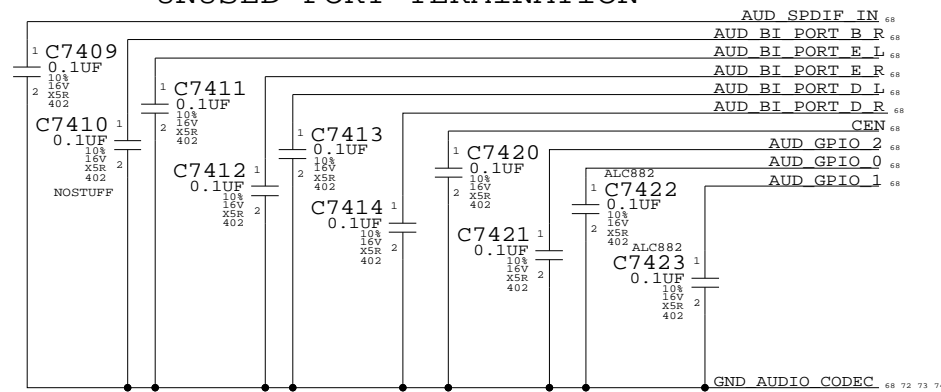
USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

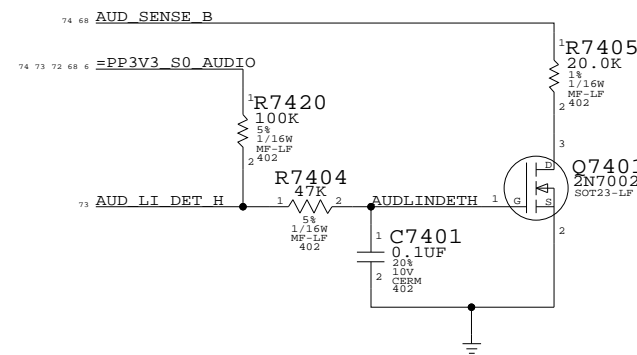
PORT F LI/LO



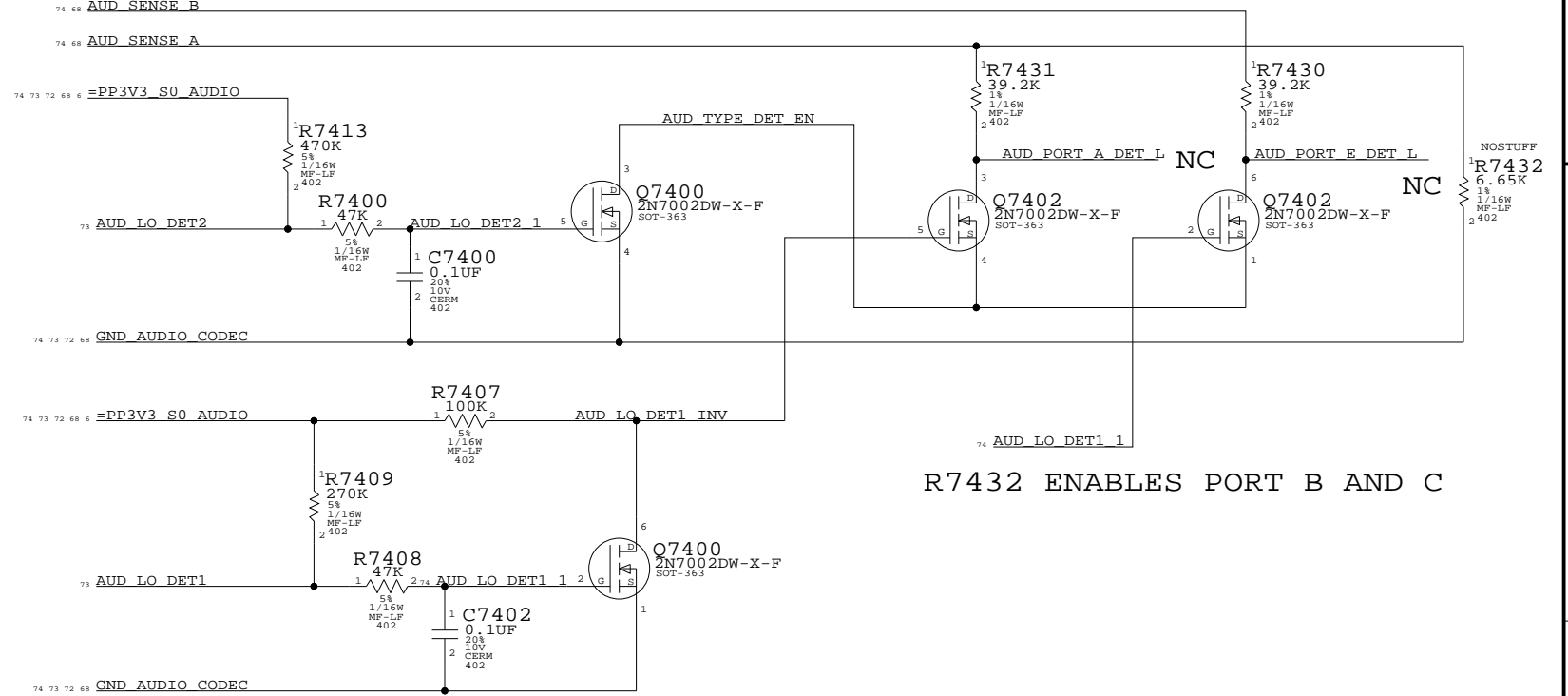
UNUSED PORT TERMINATION



PORT F (LI/LO) PLUG DETECT

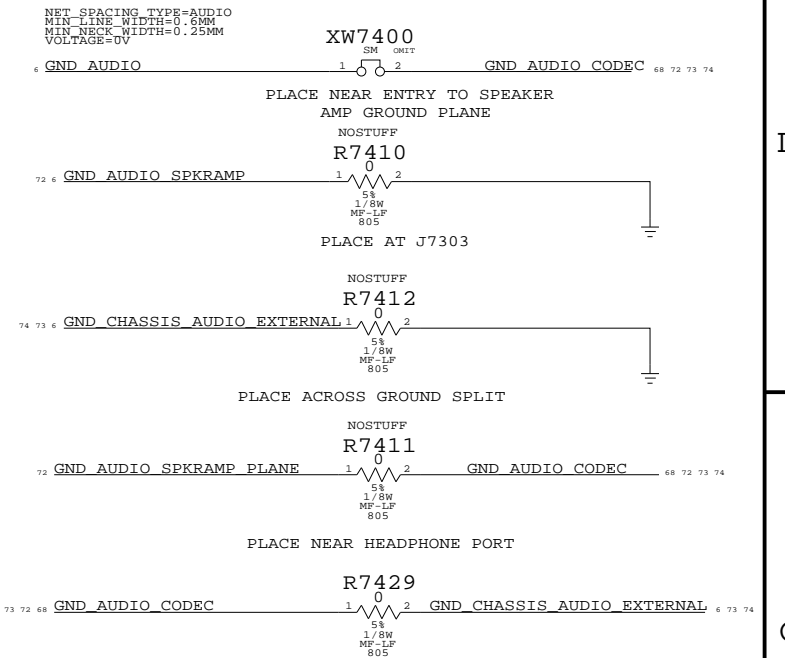


PORT A/H (HP/LI/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



R7432 ENABLES PORT B AND C

AUDIO GROUND RETURNS



MICROPHONE IMPEDANCE MATCHING CIRCUIT

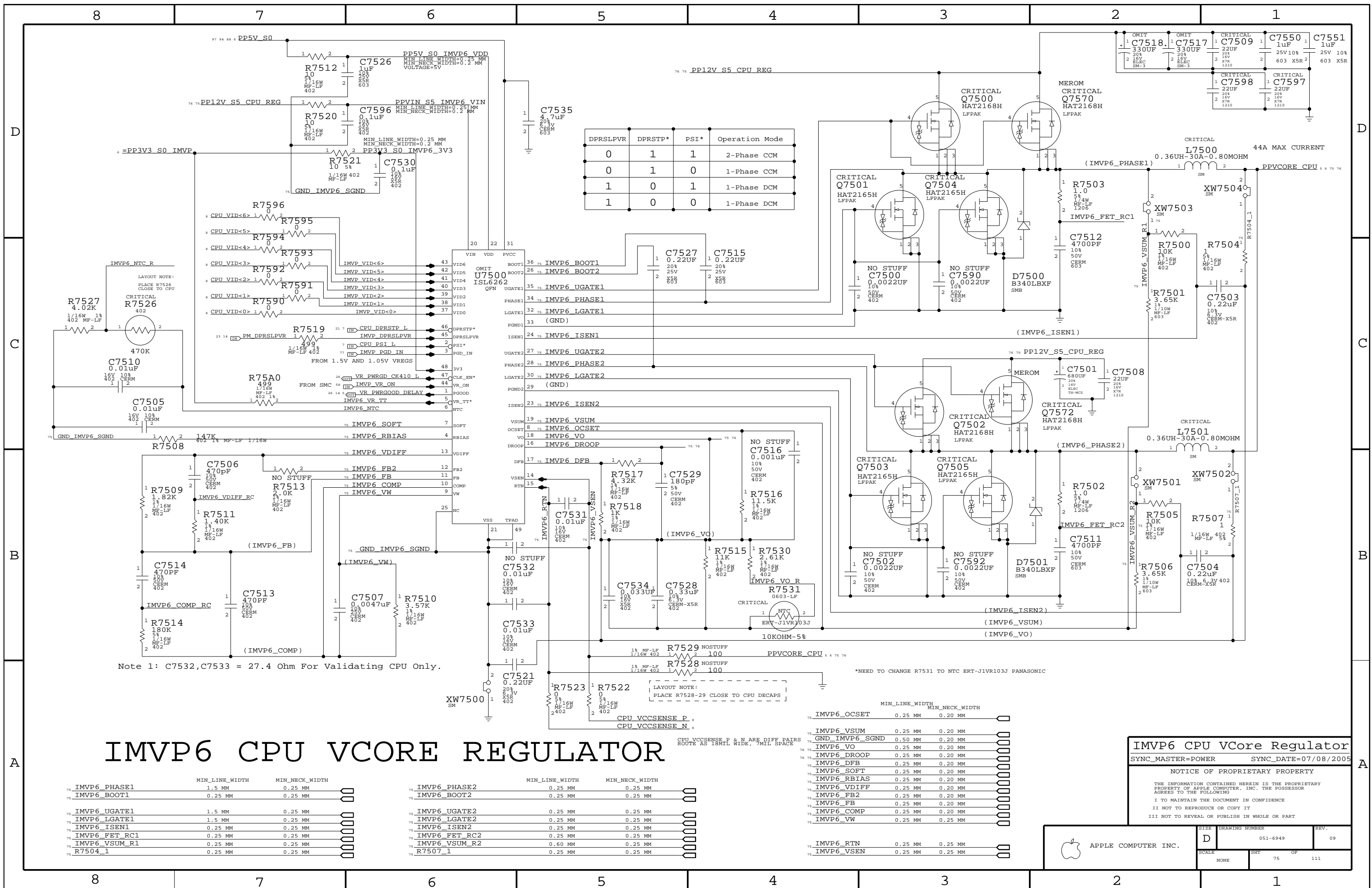
AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=04/28/2005

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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6790 | ?? |
| SCALE | NONE | SHT | OF |
| | | 74 | 154 |



| DPRSLPVR | DPRSTP* | PSI* | Operation Mode |
|----------|---------|------|----------------|
| 0 | 1 | 1 | 2-Phase CCM |
| 0 | 1 | 0 | 1-Phase CCM |
| 1 | 0 | 1 | 1-Phase DCM |
| 1 | 0 | 0 | 1-Phase DCM |

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

| | MIN_LINE_WIDTH | MIN_NECK_WIDTH |
|------------------|----------------|----------------|
| 75 IMVP6_PHASE1 | 1.5 MM | 0.25 MM |
| 75 IMVP6_BOOT1 | 0.25 MM | 0.25 MM |
| 75 IMVP6_UGATE1 | 1.5 MM | 0.25 MM |
| 75 IMVP6_LGATE1 | 1.5 MM | 0.25 MM |
| 75 IMVP6_ISEN1 | 0.25 MM | 0.25 MM |
| 75 IMVP6_FET_RC1 | 0.25 MM | 0.25 MM |
| 75 IMVP6_VSUM_R1 | 0.25 MM | 0.25 MM |
| 75 R7504_1 | 0.25 MM | 0.25 MM |

| | MIN_LINE_WIDTH | MIN_NECK_WIDTH |
|------------------|----------------|----------------|
| 75 IMVP6_PHASE2 | 0.25 MM | 0.25 MM |
| 75 IMVP6_BOOT2 | 0.25 MM | 0.25 MM |
| 75 IMVP6_UGATE2 | 0.25 MM | 0.25 MM |
| 75 IMVP6_LGATE2 | 0.25 MM | 0.25 MM |
| 75 IMVP6_ISEN2 | 0.25 MM | 0.25 MM |
| 75 IMVP6_FET_RC2 | 0.25 MM | 0.25 MM |
| 75 IMVP6_VSUM_R2 | 0.60 MM | 0.25 MM |
| 75 R7507_1 | 0.25 MM | 0.25 MM |

| | MIN_LINE_WIDTH | MIN_NECK_WIDTH |
|-------------------|----------------|----------------|
| 75 IMVP6_OCSET | 0.25 MM | 0.20 MM |
| 75 IMVP6_VSUM | 0.25 MM | 0.20 MM |
| 75 GND_IMVP6_SGND | 0.50 MM | 0.20 MM |
| 75 IMVP6_VO | 0.25 MM | 0.20 MM |
| 75 IMVP6_DROOP | 0.25 MM | 0.20 MM |
| 75 IMVP6_DFB | 0.25 MM | 0.20 MM |
| 75 IMVP6_SOFT | 0.25 MM | 0.20 MM |
| 75 IMVP6_RBIAS | 0.25 MM | 0.20 MM |
| 75 IMVP6_VDIFF | 0.25 MM | 0.20 MM |
| 75 IMVP6_FB2 | 0.25 MM | 0.20 MM |
| 75 IMVP6_FB | 0.25 MM | 0.20 MM |
| 75 IMVP6_COMP | 0.25 MM | 0.20 MM |
| 75 IMVP6_VW | 0.25 MM | 0.25 MM |
| 75 IMVP6_RTIN | 0.25 MM | 0.25 MM |
| 75 IMVP6_VSEN | 0.25 MM | 0.25 MM |

IMVP6 CPU VCore Regulator
 SYNC_MASTER=POWER SYNC_DATE=07/08/2005

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| SCALE | DRAWING NUMBER | REV. |
| NONE | D 051-6949 | 09 |
| SHEET | 75 | OF 111 |

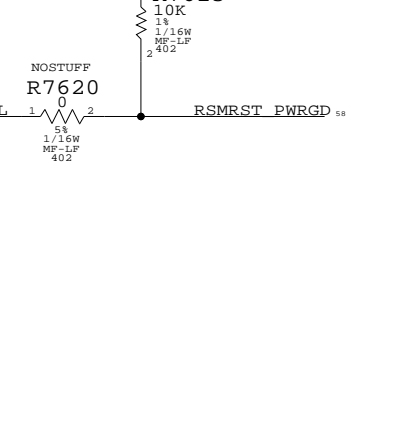
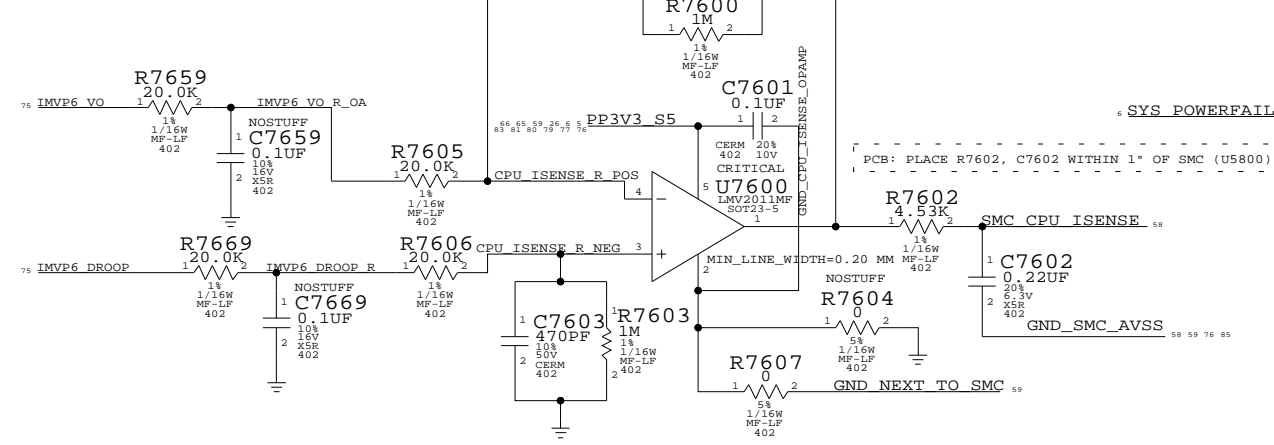
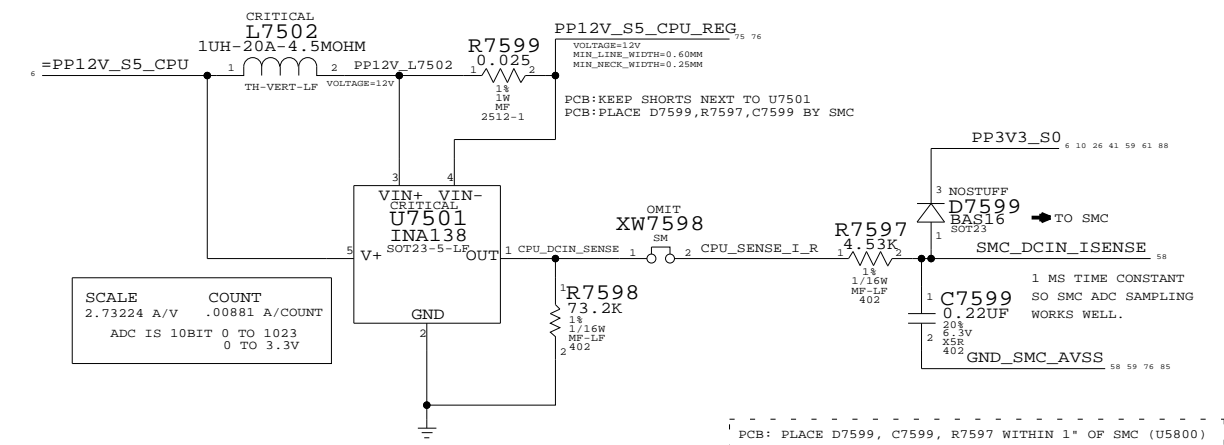


APPLE COMPUTER INC.

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

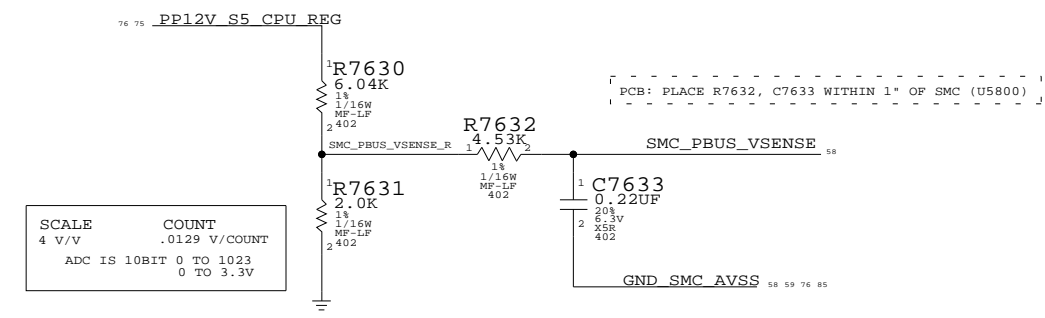
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

SMC PWRGD PULLUP

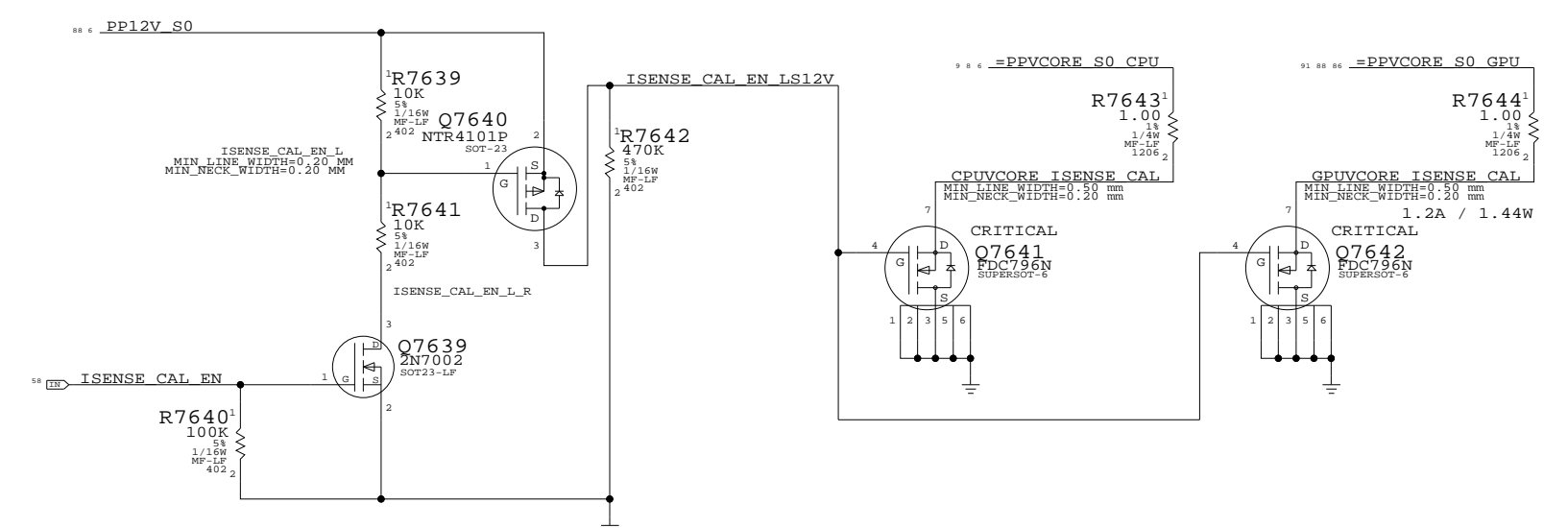


PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

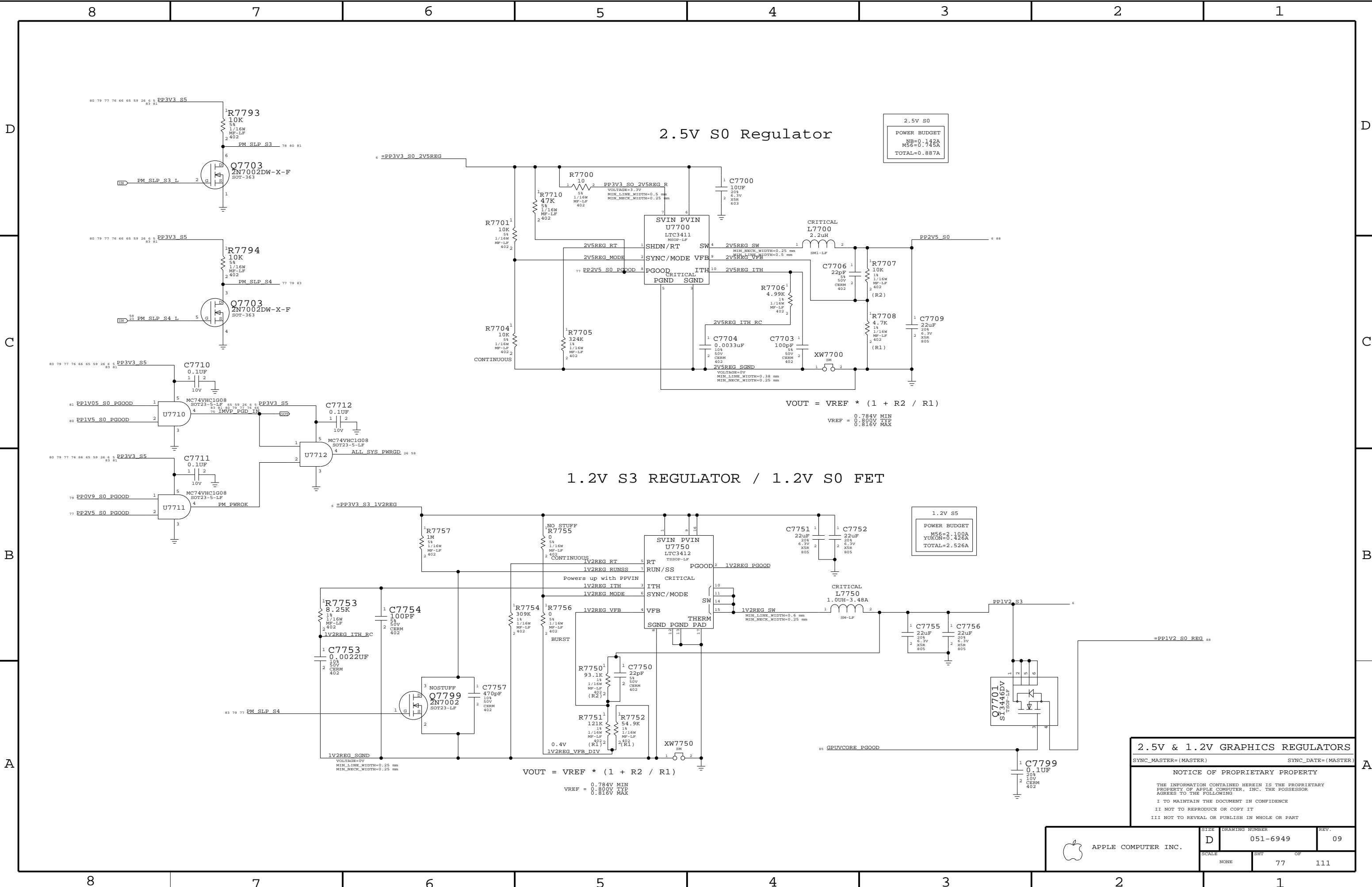
PROCESSOR VCORE SENSE



Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits



CPU SENSE CIRCUITRIES
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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2.5V S0 Regulator

2.5V S0
POWER BUDGET
MSE=1.42A
MBS=0.745A
TOTAL=0.887A

$V_{OUT} = V_{REF} * (1 + R2 / R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

1.2V S3 REGULATOR / 1.2V S0 FET

1.2V S5
POWER BUDGET
MSE=1.408A
YUSEN=0.108A
TOTAL=2.526A

$V_{OUT} = V_{REF} * (1 + R2 / R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $V_{REF} = 0.800V \text{ TYP}$
 $V_{REF} = 0.816V \text{ MAX}$

2.5V & 1.2V GRAPHICS REGULATORS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

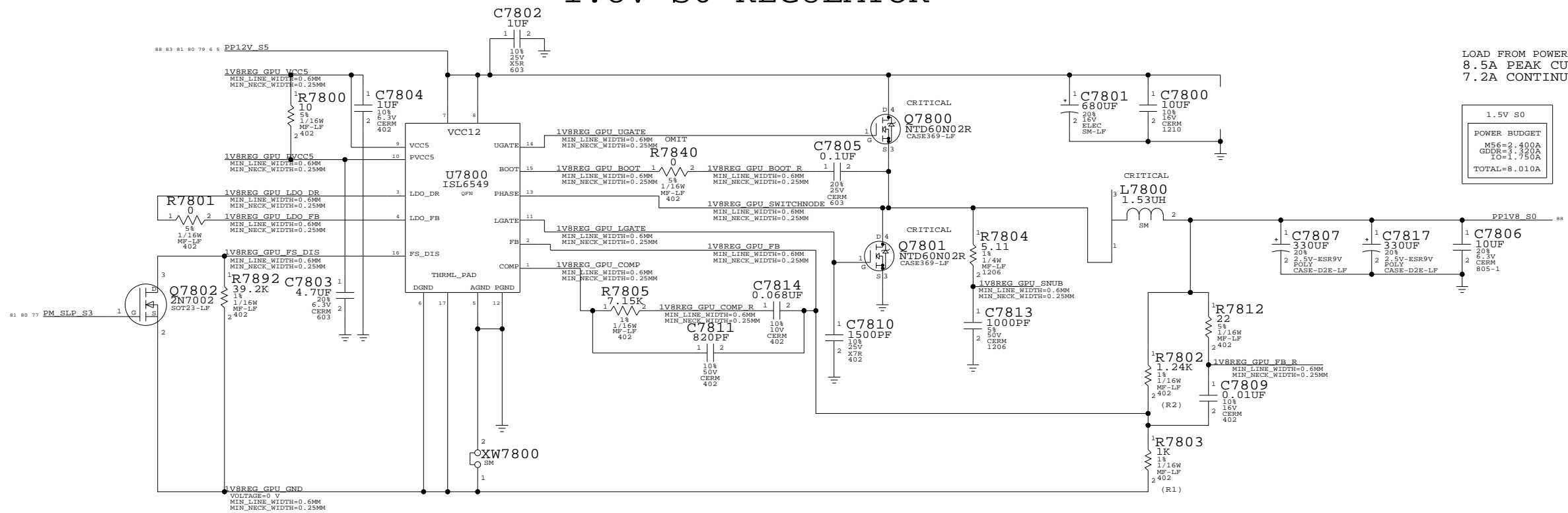
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| | D | 051-6949 | 09 |
| SCALE | SHT | OF | |
| NONE | 77 | 111 | |

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---------------------------|-------------------------|----------|------------|
| 11480514 | 1 | 5.11 OHM 0402 1% 1/16W LF | R7840 | | |

1.8V S0 REGULATOR



LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.5V S0
POWER BUDGET
M56=2.400A
GDDR=3.300A
IO=1.700A
TOTAL=8.010A

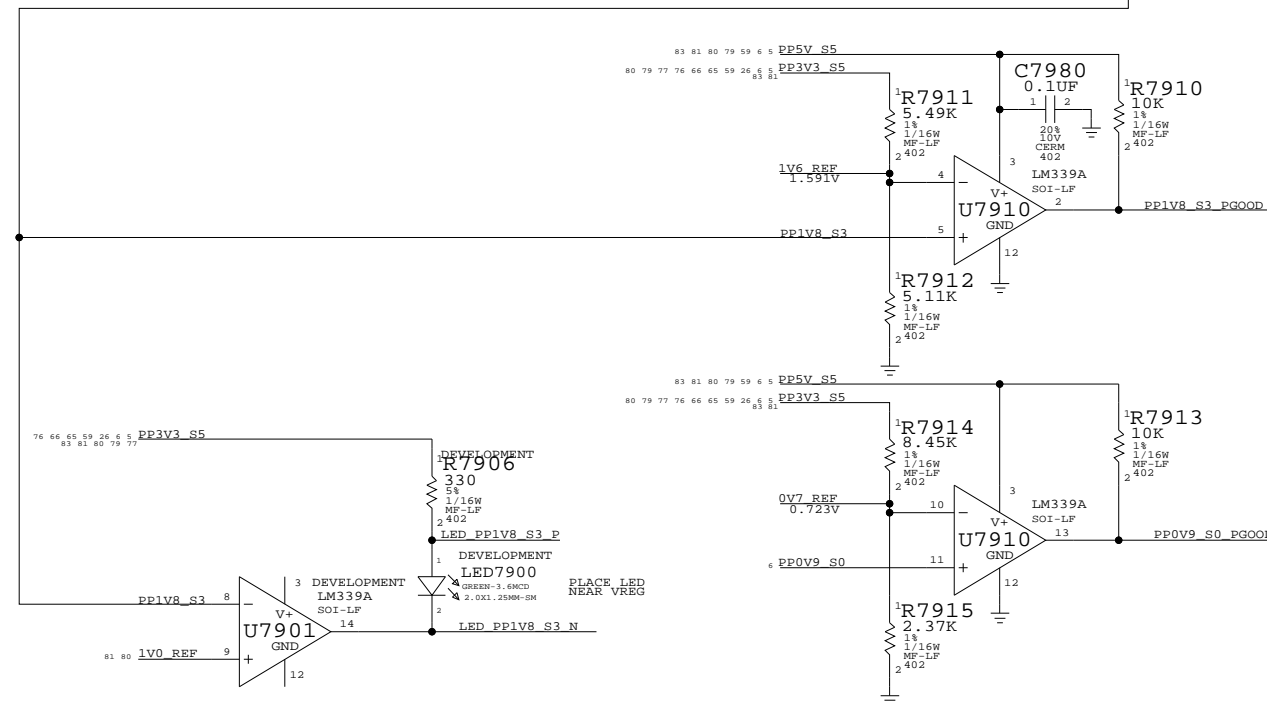
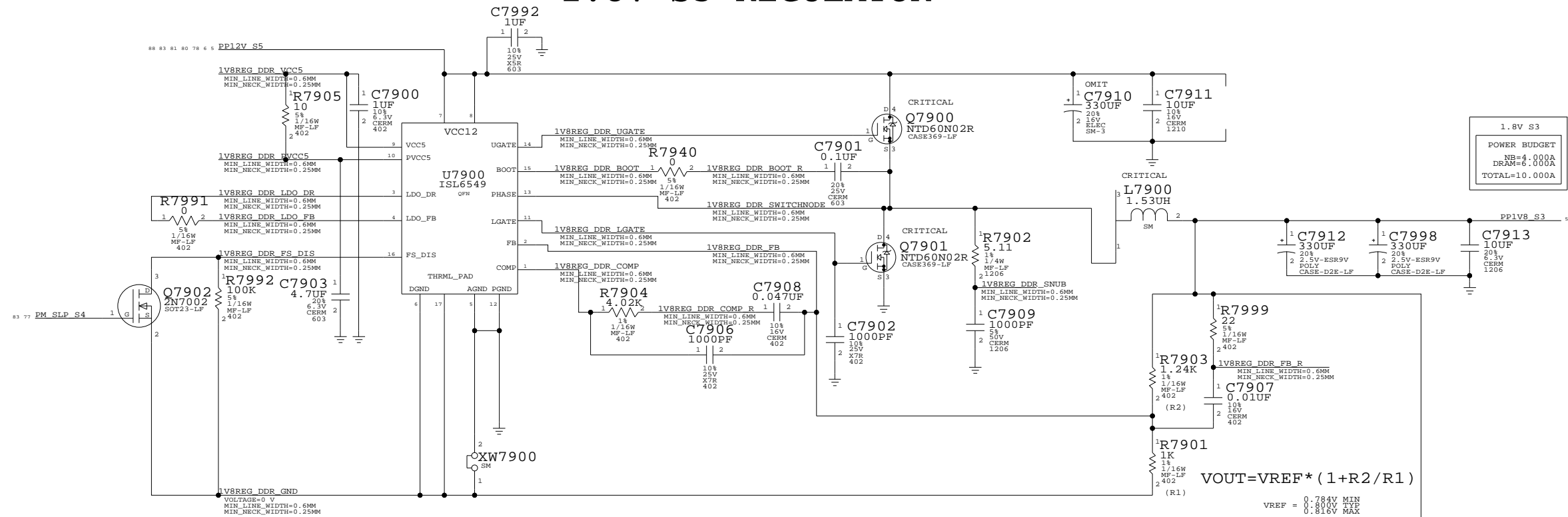
$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

VREF = 0.784V MIN
0.800V TYP
0.816V MAX

1.8V GDDR REGULATOR
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | 78 OF 111 | |
| NONE | | | |

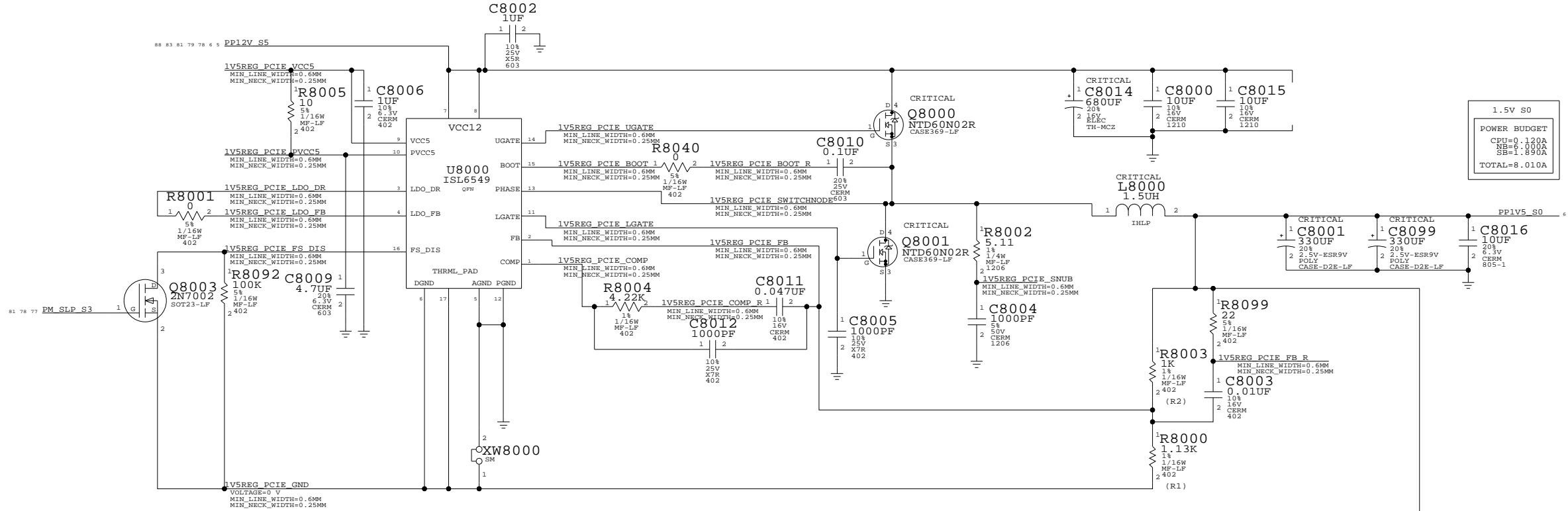
1.8V S3 REGULATOR



1.8V Vreg
 SYNC_MASTER=M23-PC SYNC_DATE=04/12/2005
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| | D | 051-6949 | 09 |
| SCALE | SHT | 79 OF | 111 |
| NONE | | | |

1.5V S0 REGULATOR

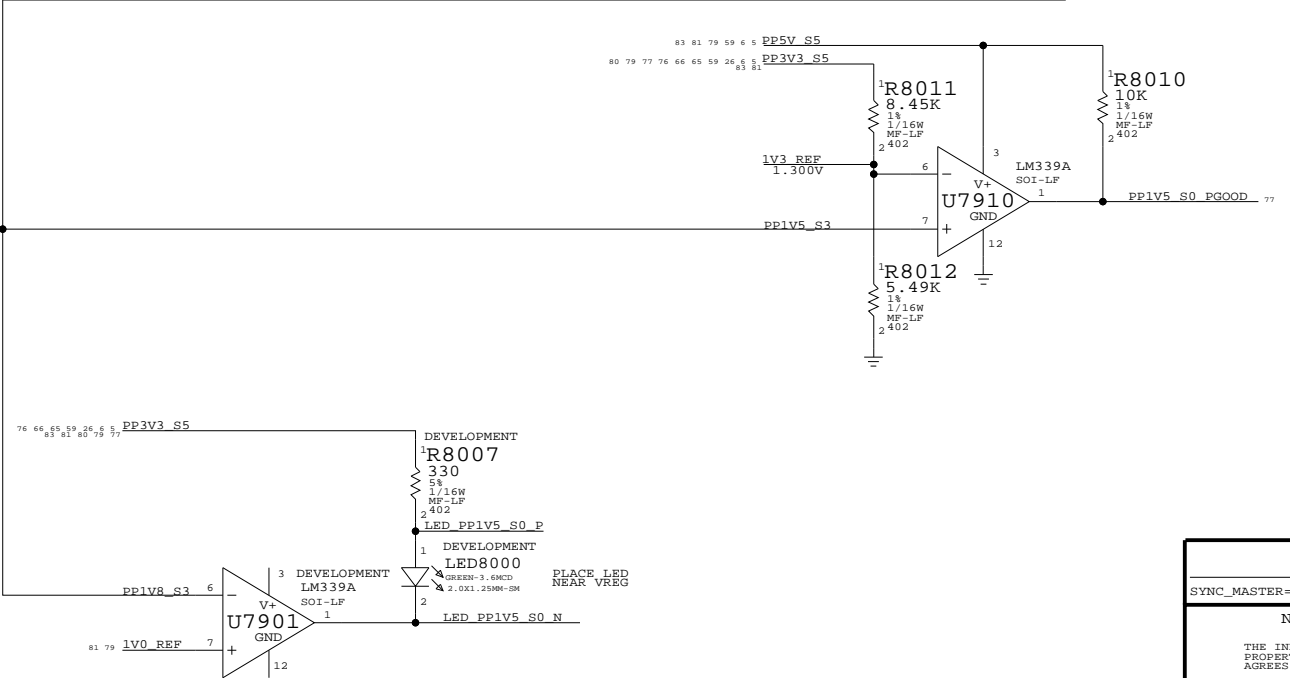


$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$V_{REF} = 0.800V \text{ TYP}$$

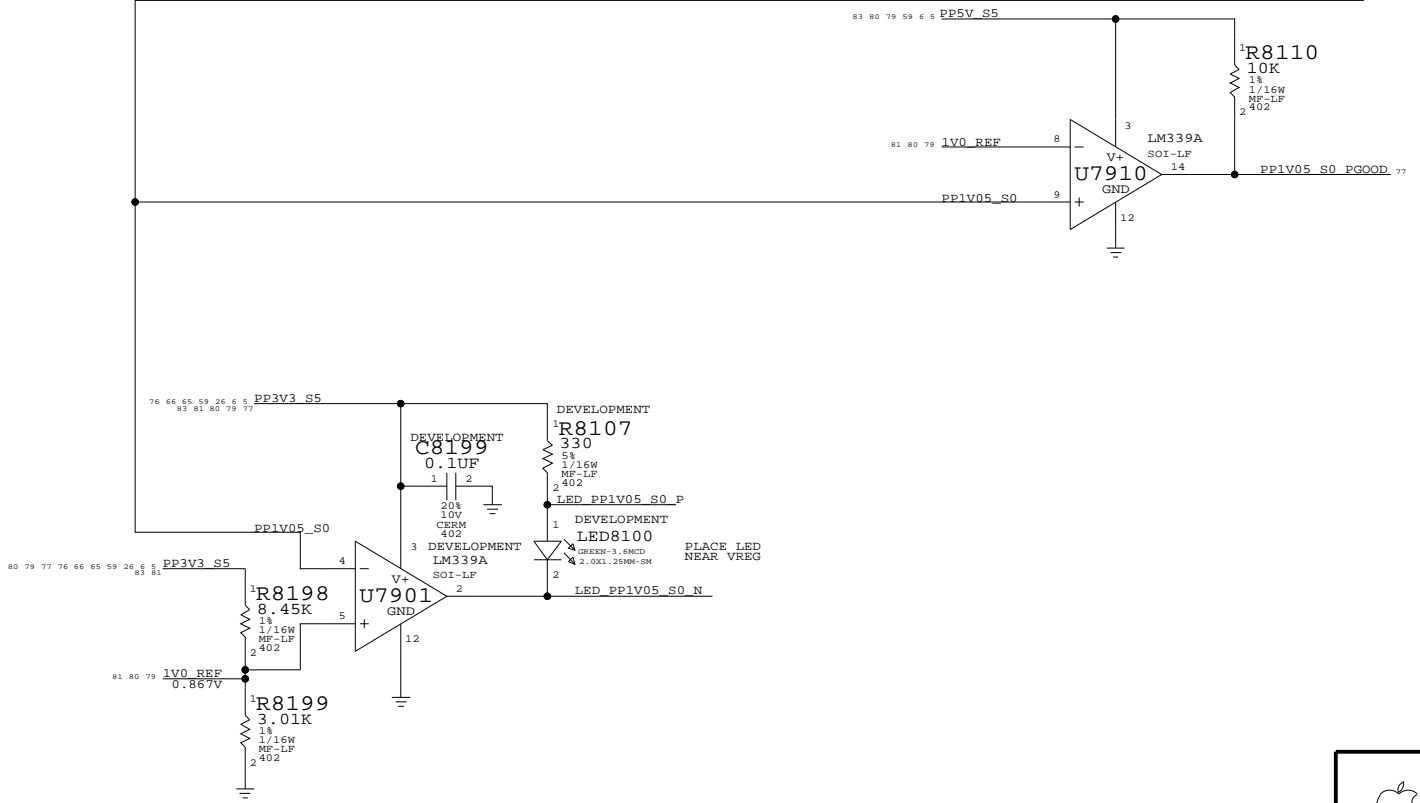
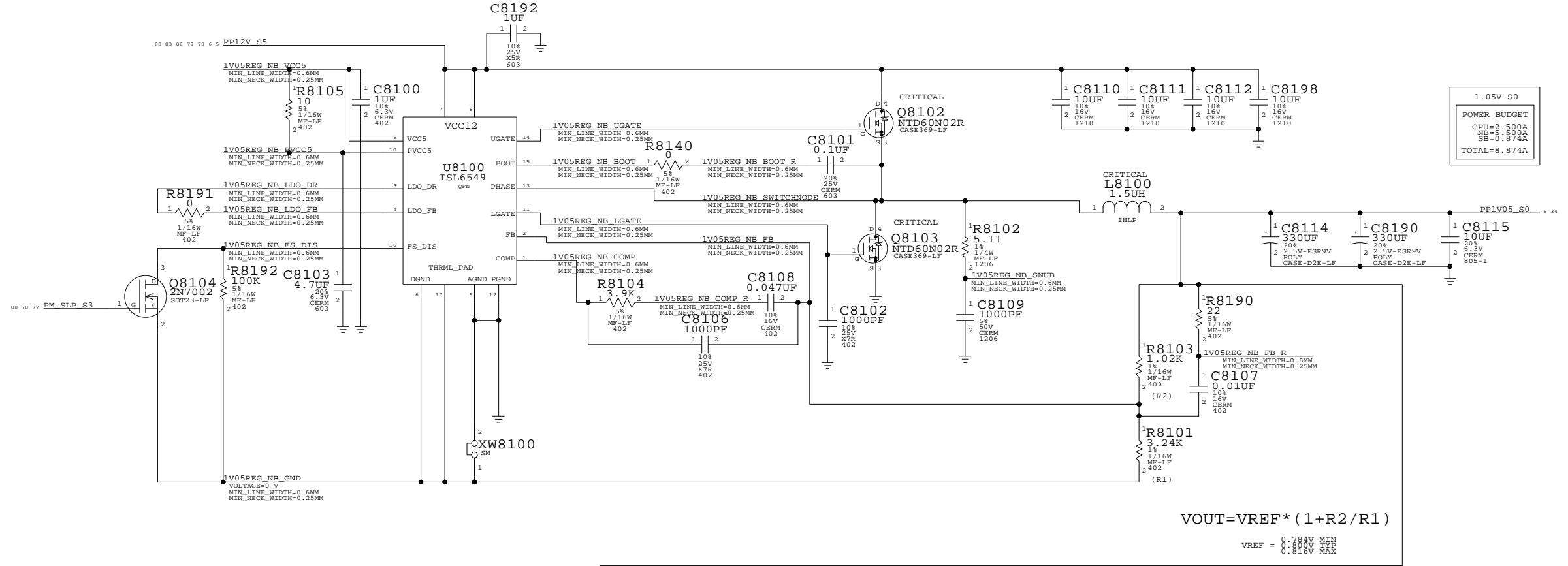
$$V_{REF} = 0.816V \text{ MAX}$$



1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/18/2005
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| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6950 | 06 |
| SCALE | SHT | 80 OF | 111 |
| NONE | | | |

1.05V S0 REGULATOR



1.05V VREG

SYNC_MASTER=M38-RT SYNC_DATE=05/18/2005

NOTICE OF PROPRIETARY PROPERTY

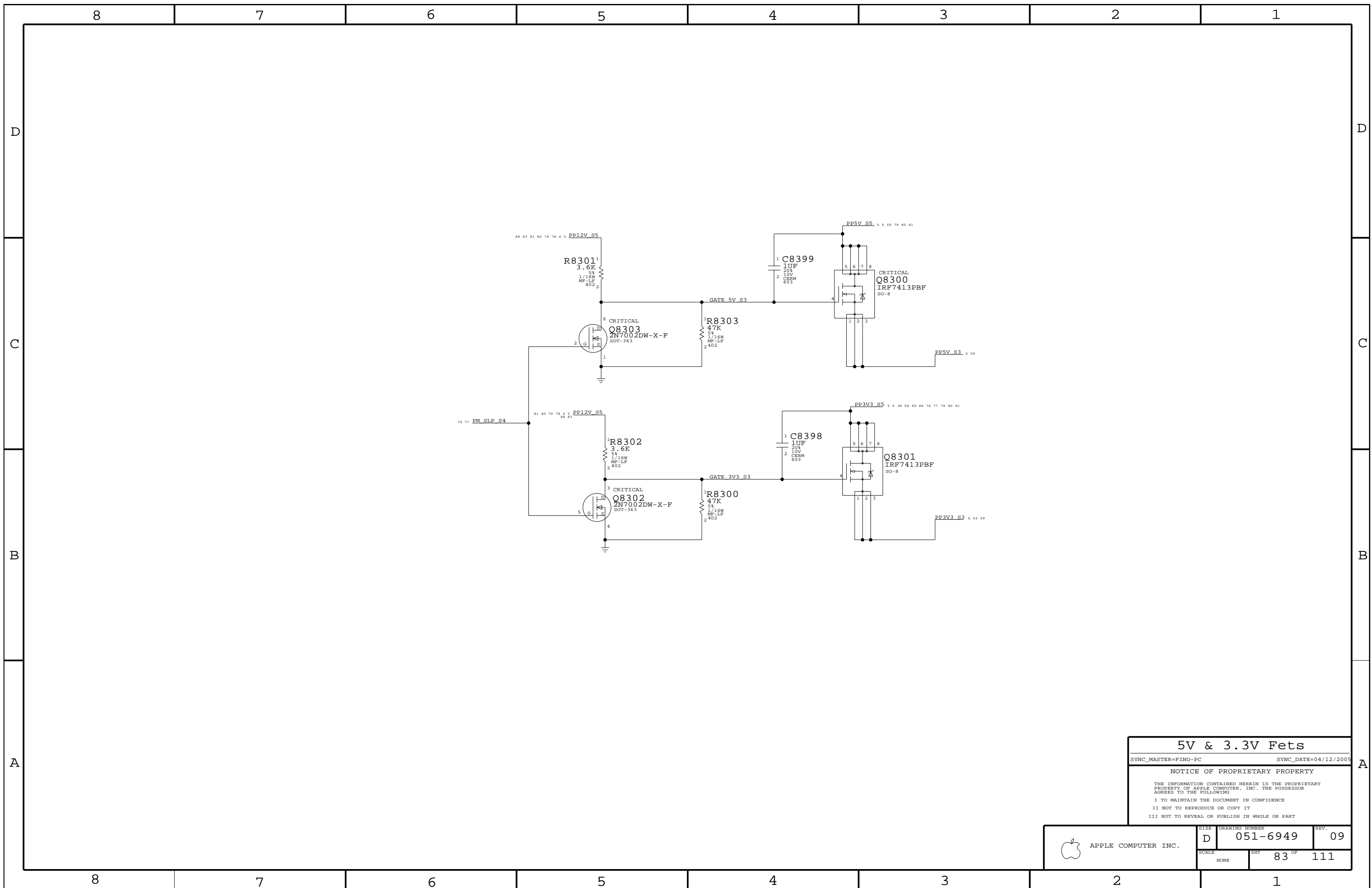
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| | D | 051-6949 | 09 |
| SCALE | SHT | 81 OF | 111 |
| NONE | | | |



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=04/12/2005

NOTICE OF PROPRIETARY PROPERTY

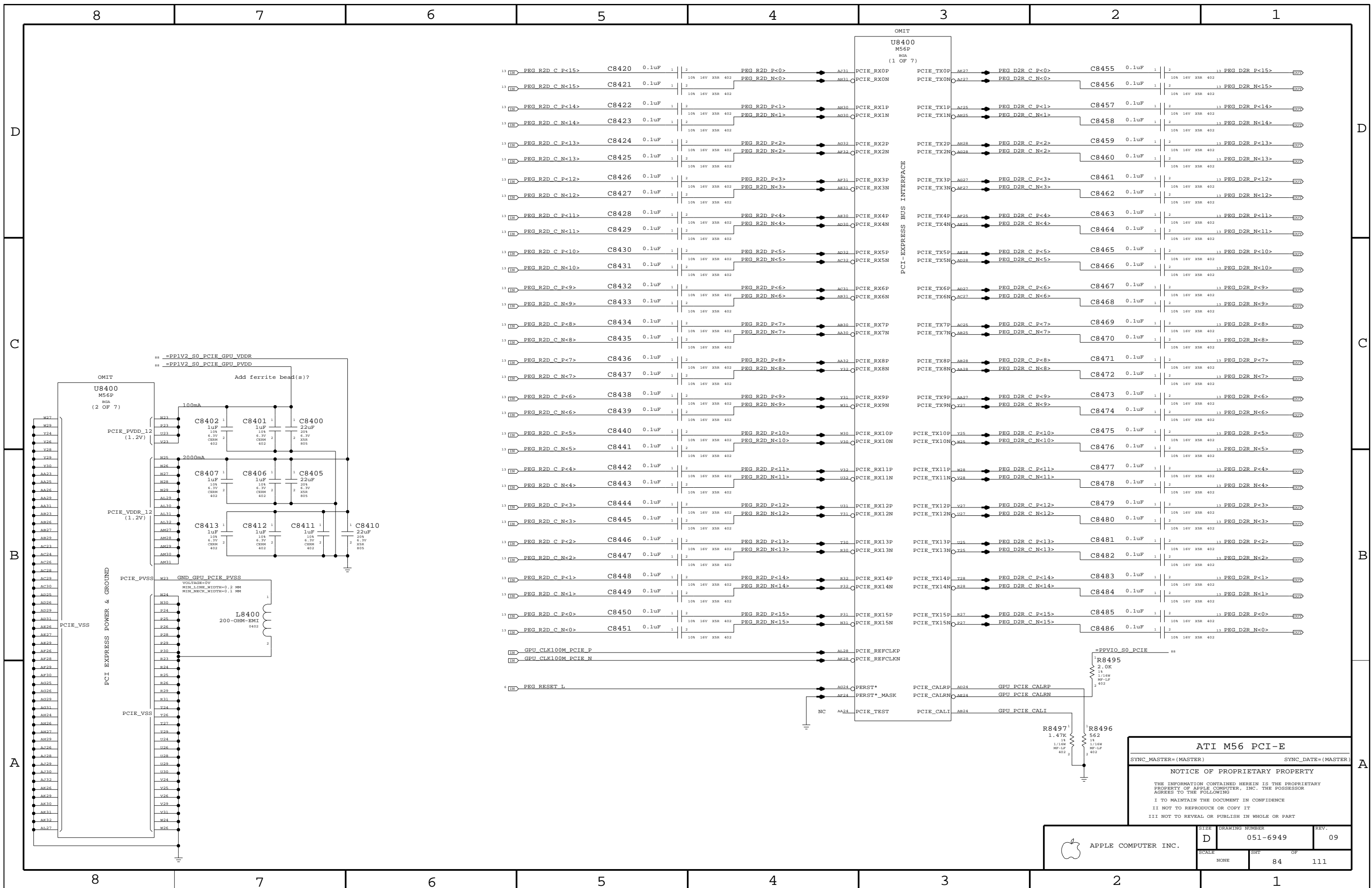
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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | 83 OF 111 | |
| NONE | | | |



ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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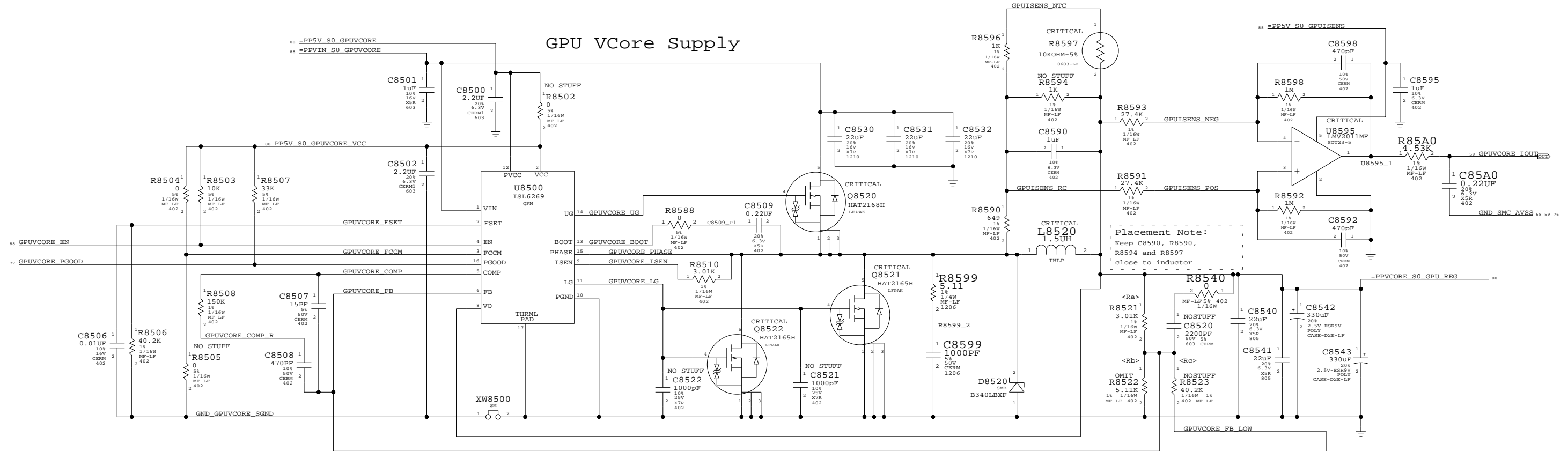
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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| | | | |
|---------------------|---------------|----------------------------|------------|
| APPLE COMPUTER INC. | SIZE D | DRAWING NUMBER 051-6949 | REV. 09 |
| | SCALE NONE | SHEET 84 | OF 111 |

GPU VCore Current Sense



Placement Note:
 Keep C8590, R8590, R8594 and R8597 close to inductor

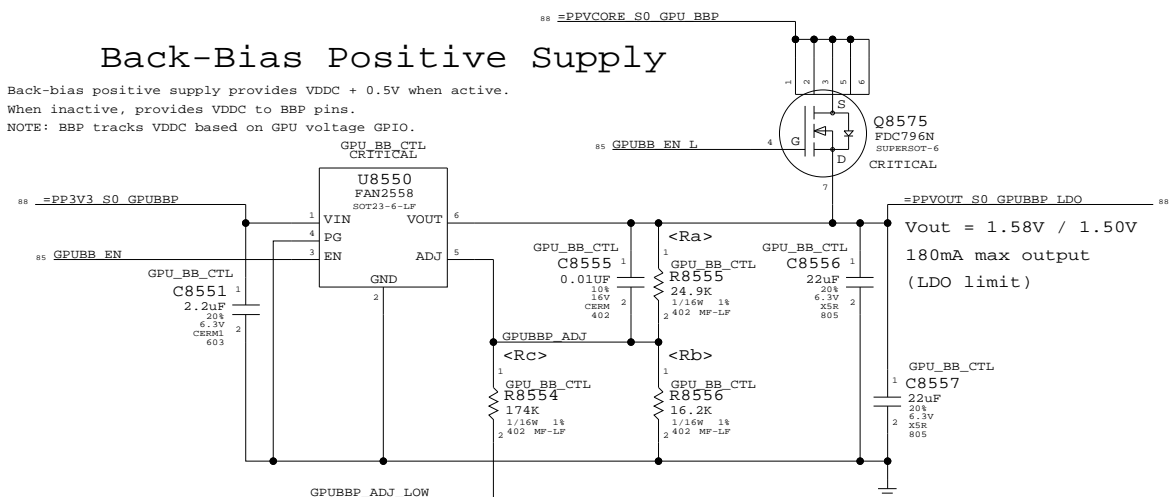
$$V_{out}(low) = 0.6V * (1 + R_a/R_b)$$

$$V_{out}(high) = 0.6V * (1 + R_a/Req)$$

$$Req = R_b || R_c$$

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to BBP pins.
 NOTE: BBP tracks VDDC based on GPU voltage GPIO.



$$V_{out} = 1.58V / 1.50V$$

180mA max output (LDO limit)

$$V_{out}(low) = 0.59V * (1 + R_a/R_b)$$

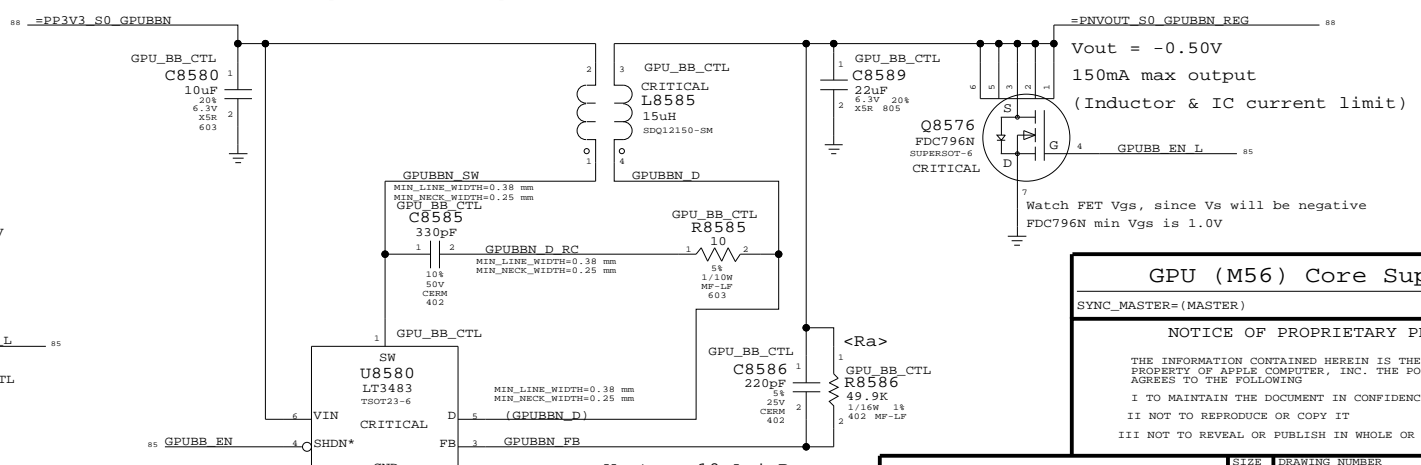
$$V_{out}(high) = 0.59V * (1 + R_a/Req)$$

$$Req = R_b || R_c$$

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
 FDC796N max Vgs is 3.0V
 Vin must be > 4.2V

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active. When inactive, provides VSS to BBN pins.



$$V_{out} = -0.50V$$

150mA max output (Inductor & IC current limit)

$$V_{out} = -10\mu A * R_a$$

GPU (M56) Core Supplies
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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| | D | 051-6949 | 09 |
| SCALE | SHT | OF | |
| NONE | 85 | 111 | |

Page Notes

Power aliases required by this page:
 - =PP1V5_GPU_VDD15
 - =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

8 7 6 5 4 3 2 1

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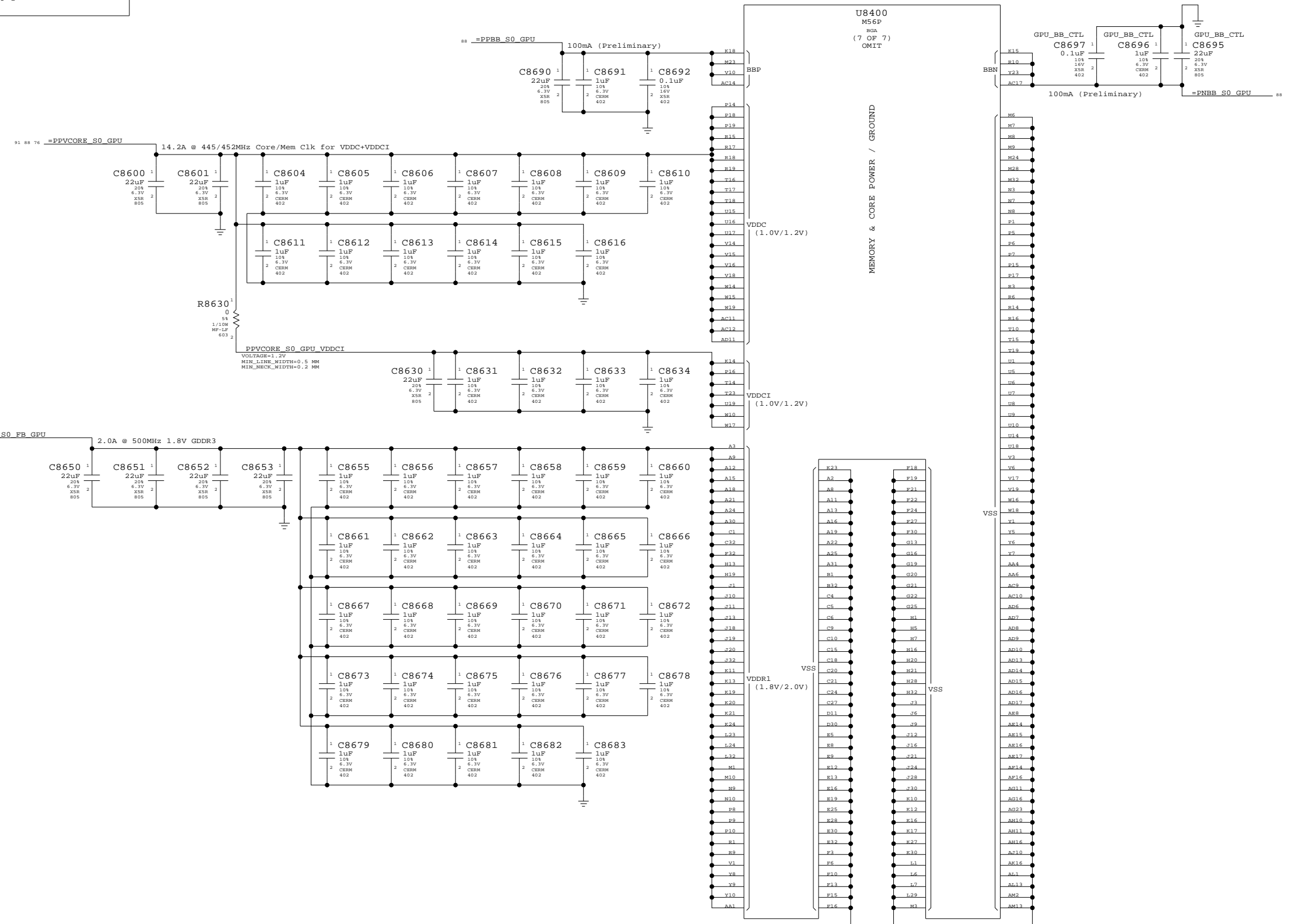
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8 7 6 5 4 3 2 1



ATI M56 Core Power

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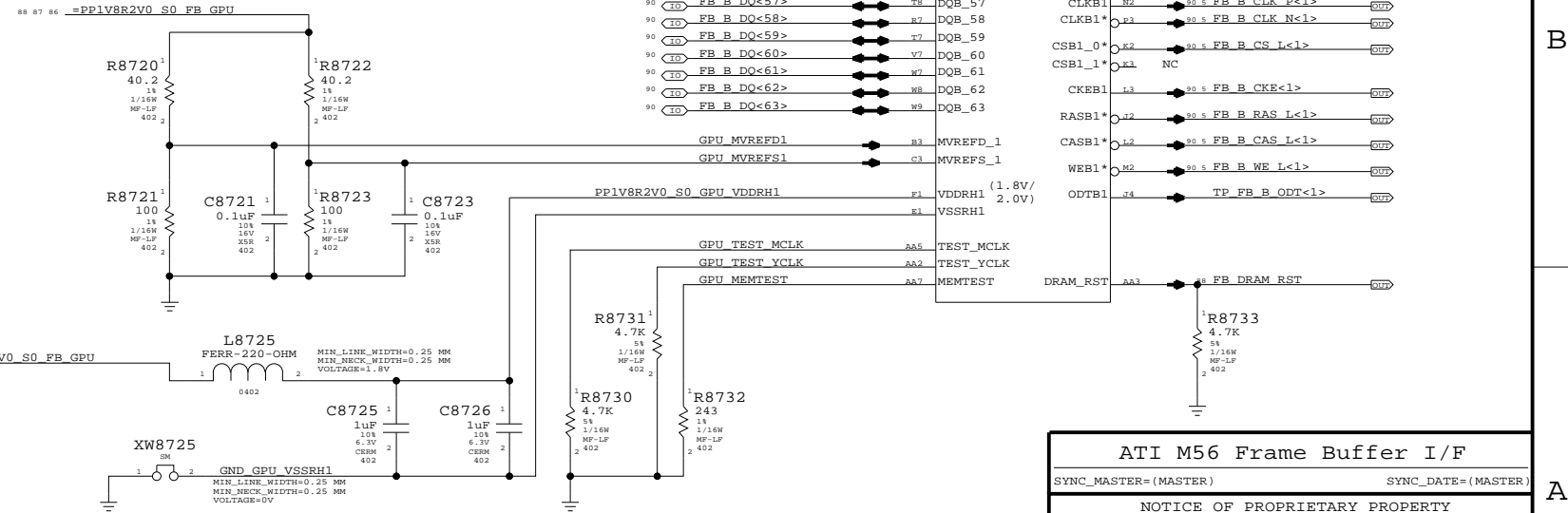
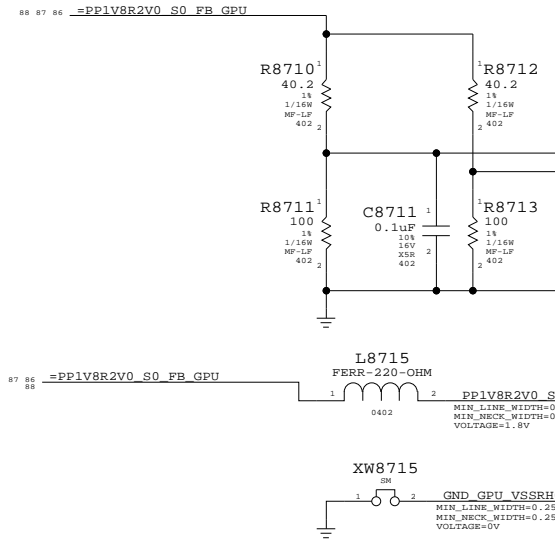
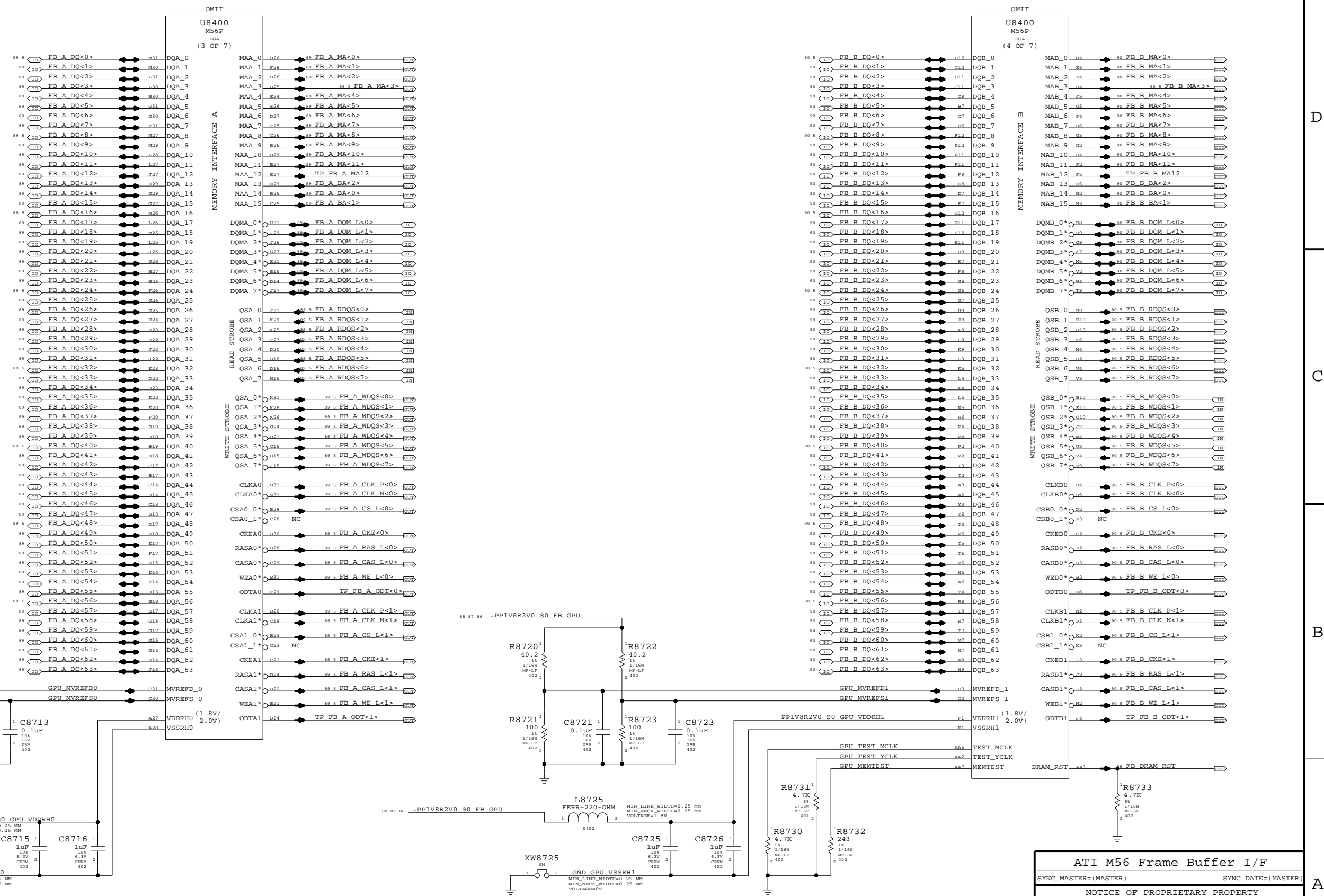
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | NONE | SHT | OF |
| | | 86 | 111 |

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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"S0" GPU RAILS

ONLY ON IN RUN

M56 GPIOs

=PP3V3_S0_GPU_VDDR3 #8 #1

59 EP1V0R1V2_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

85 PP5V_S0_GPUVCORE_VCC
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

PP1V2_GPU_IO_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PPBB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PPNB_S0_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=0V

76 61 59 41 26 10 6 PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

77 6 PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

PP1V8R2V0_S0_FB_GPU
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.8V

83 81 80 79 78 6 5 PP12V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

76 6 PP12V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=1.2V

97 94 76 6 PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

85 GPUVCORE_EN
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

87 FB_DRAM_RST
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

94 91 GPU_GPIO_0
GPIO 0 = TRANSMITTER POWER SAVINGS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_1
GPIO 1 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_2
GPIO 2 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_3
GPIO 3 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_4
GPIO 4 = DEBUG SIGNALS OUT

91 GPU_GPIO_5
GPIO 5 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_6
GPIO 6 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

TP_GPU_GPIO_7
MAKE_BASE=TRUE

91 GPU_GPIO_8
GPIO 8 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

NC_GPU_GPIO_10
MAKE_BASE=TRUE

91 GPU_GPIO_9
GPIO 9 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_13
GPIO 13 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_12
GPIO 12 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_11
GPIO 11 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_24
GPIO 24 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_27
GPIO 27 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_28
GPIO 28 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

91 GPU_GPIO_29
GPIO 29 = TRANSMITTER DE-EMPHASIS ENABLE
INTERNAL PULL DOWN, ATI RECOMMENDS HIGH

85 GPU_VCORE_LOW
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

85 GPUVCORE_EN
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.125MM
VOLTAGE=5V

GPU MISC

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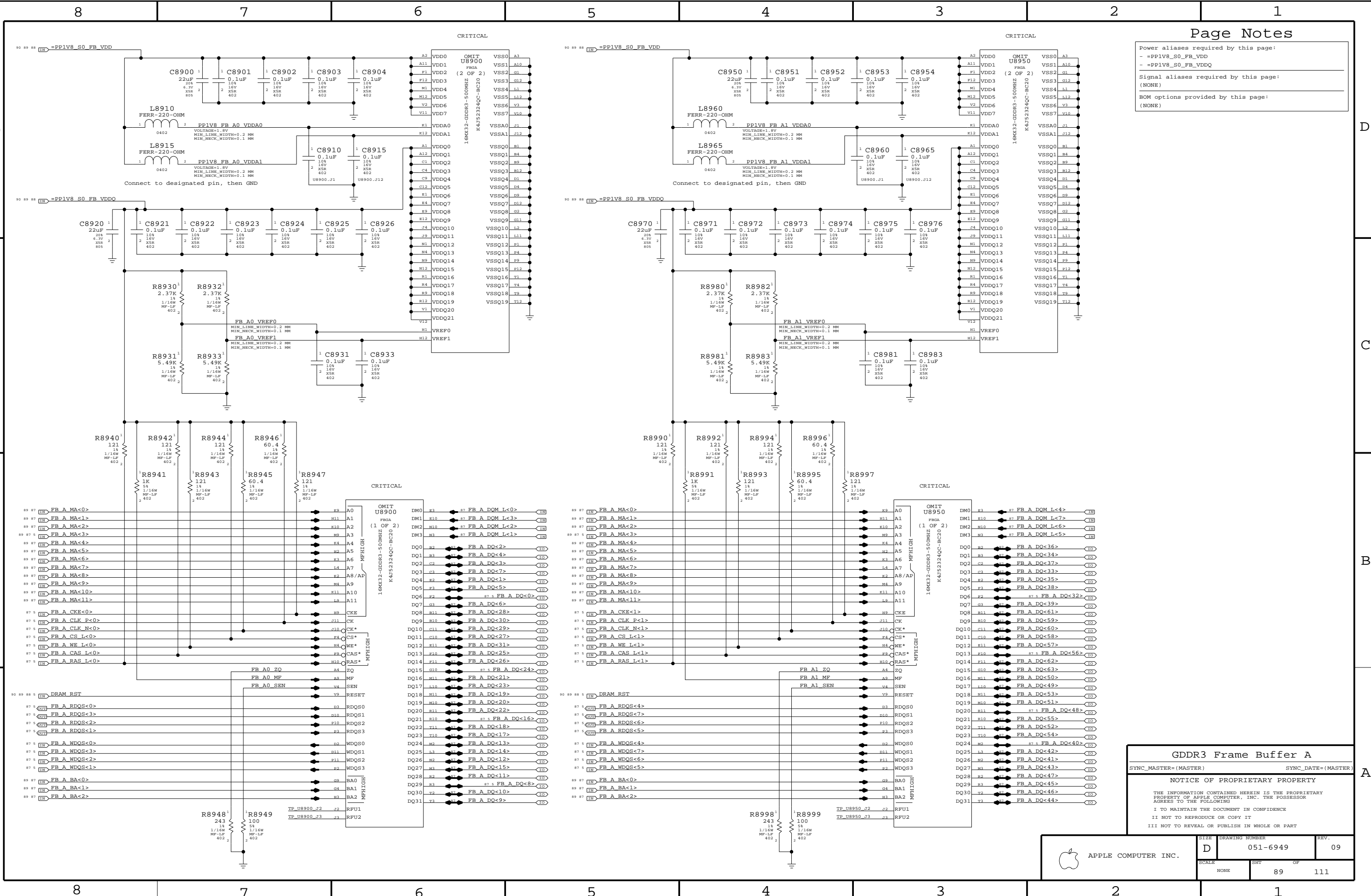
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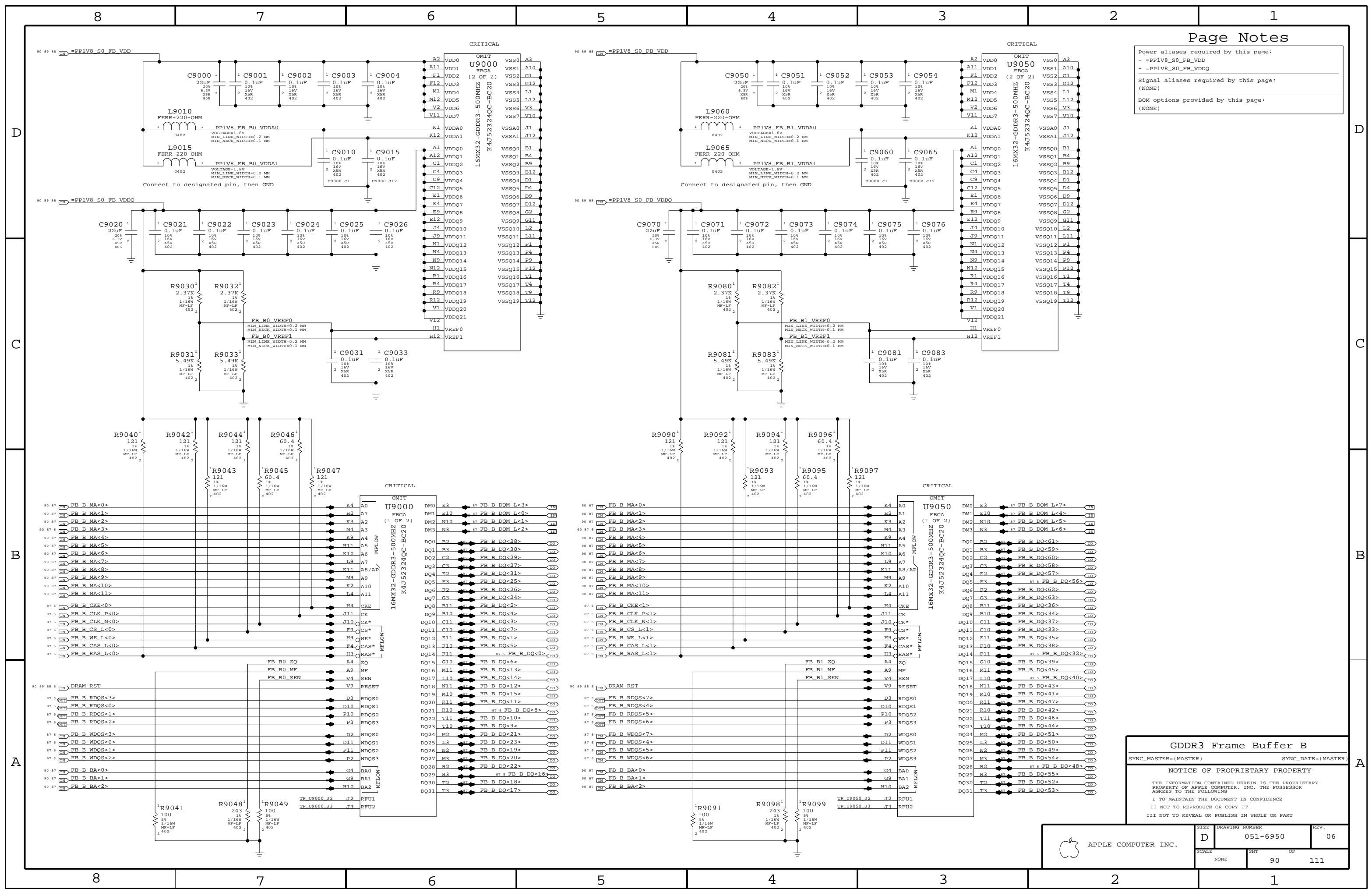
A

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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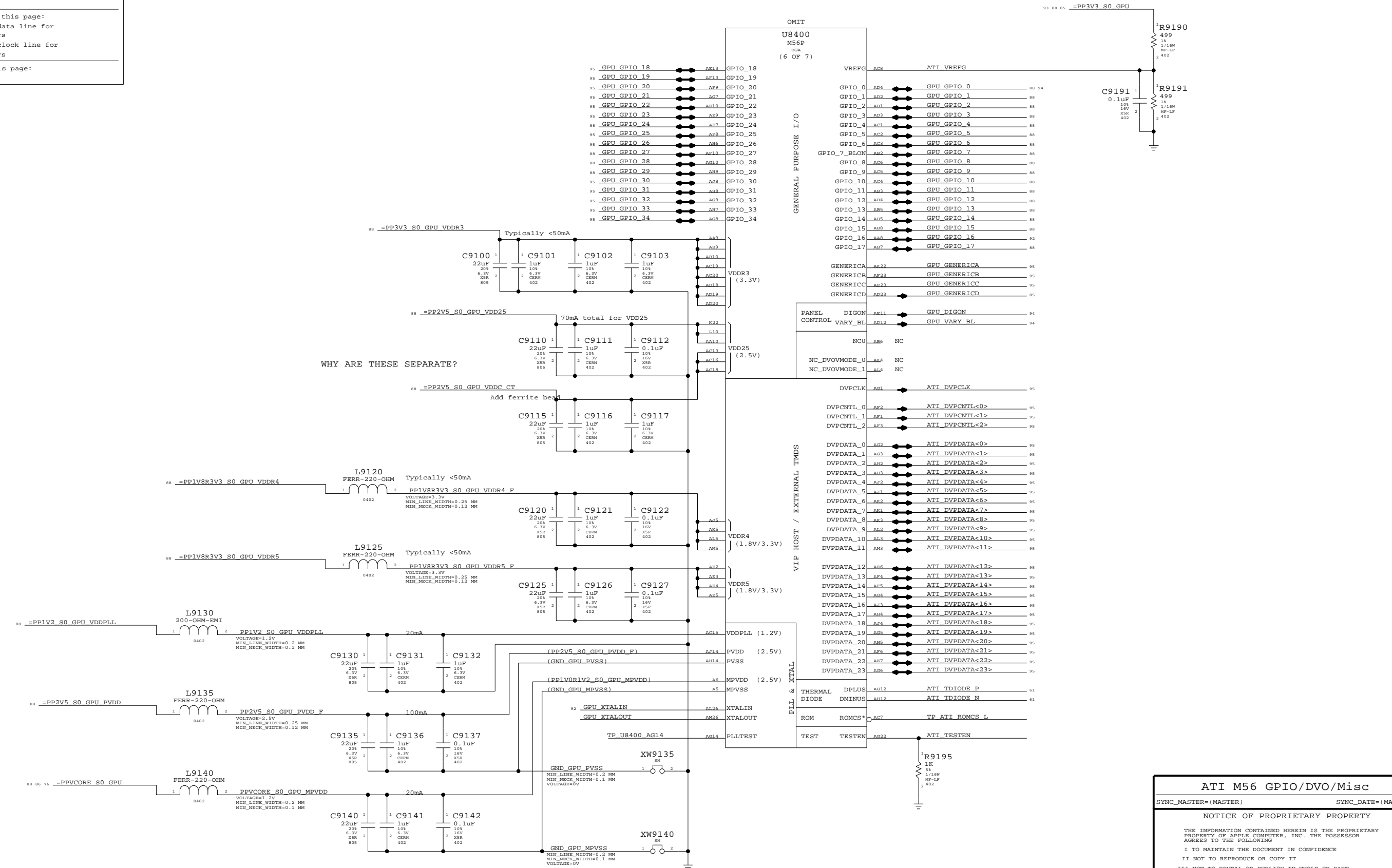
Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

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| SCALE | SHT | OF | |
| NONE | 91 | 111 | |

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Page Notes

Power aliases required by this page:

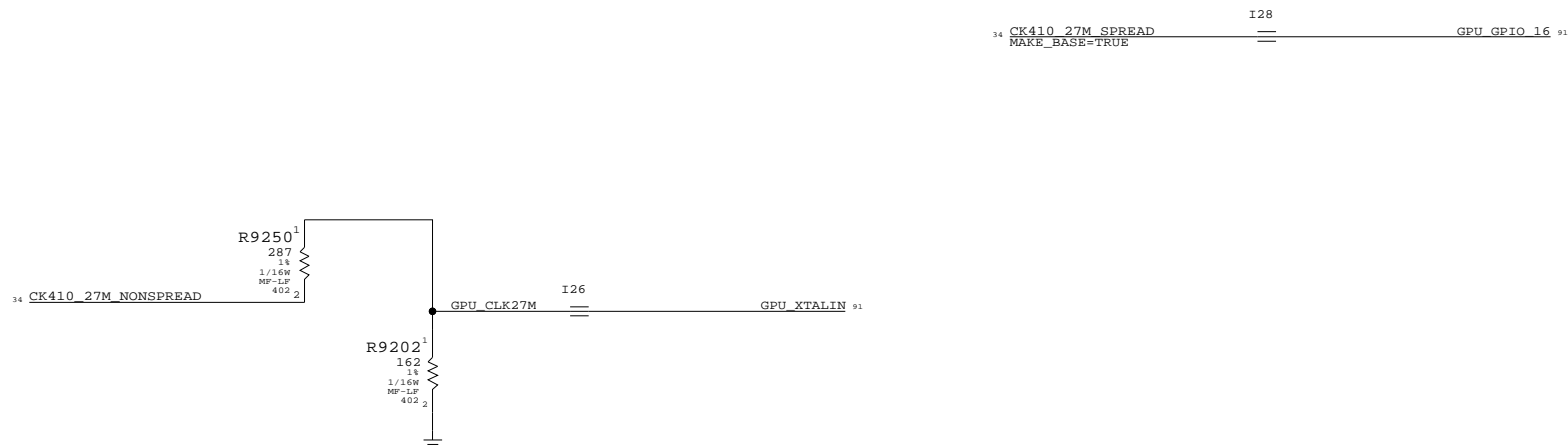
- =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
- =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
- =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- GPU_SS - GPU_LVDDR_2V8



GPU CLOCKS

SYNC_MASTER=BOZEMAN SYNC_DATE=05/21/2005

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| | D | 051-6949 | 09 |
| SCALE | SHT | OF | |
| NONE | 92 | 111 | |

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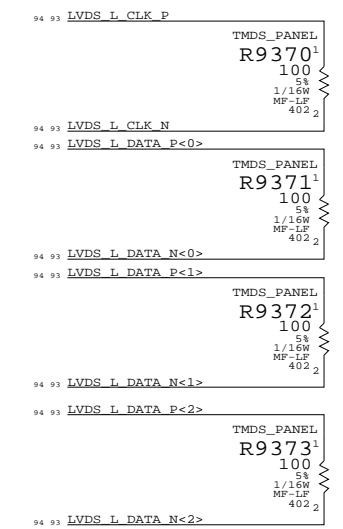
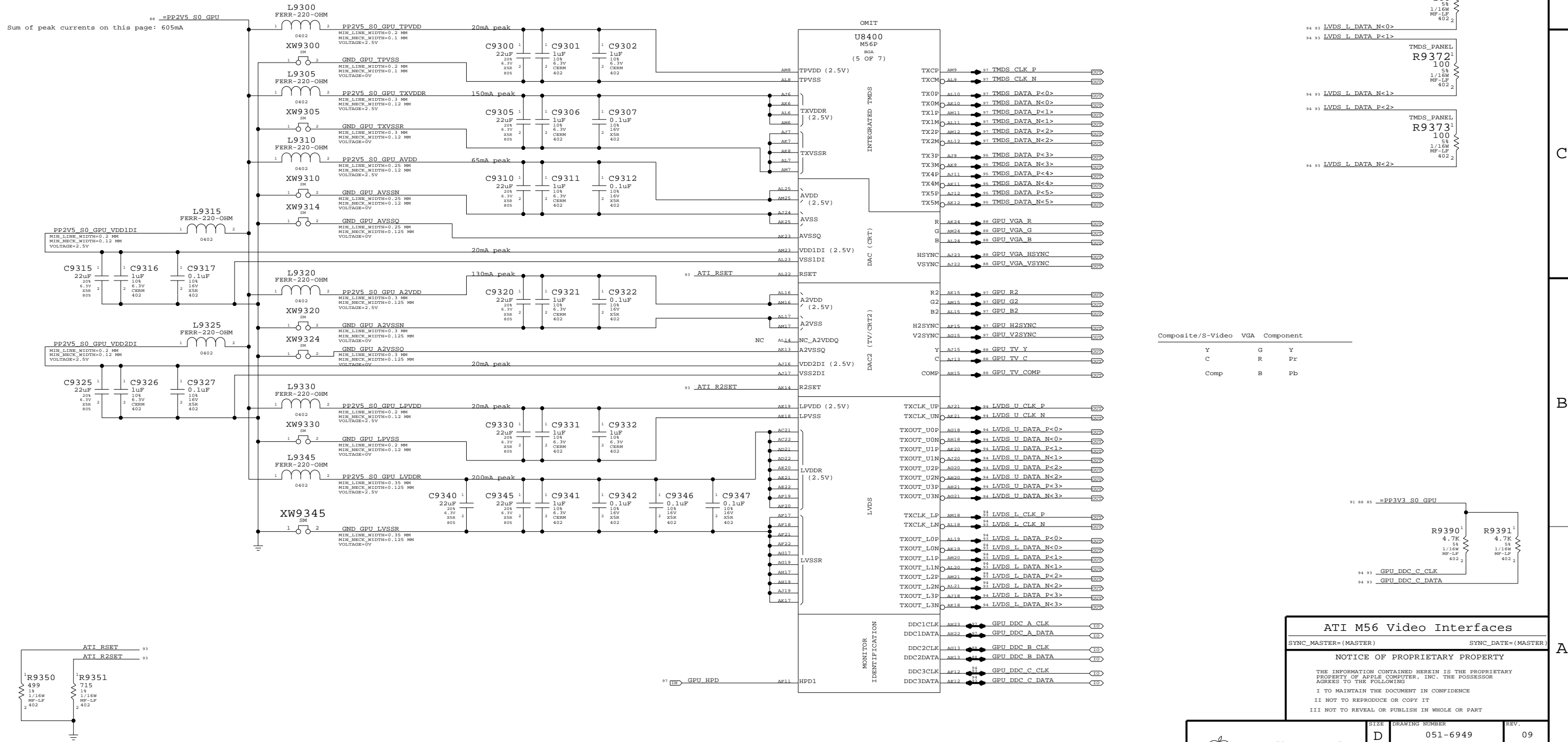
Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

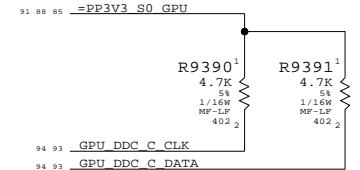
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

TERMINATION FOR TMDS USAGE OF LVDS PINS
 PLACE CLOSE TO GPU (U8400)



| Composite/S-Video | VGA | Component |
|-------------------|-----|-----------|
| Y | G | Y |
| C | R | Pr |
| Comp | B | Pb |



ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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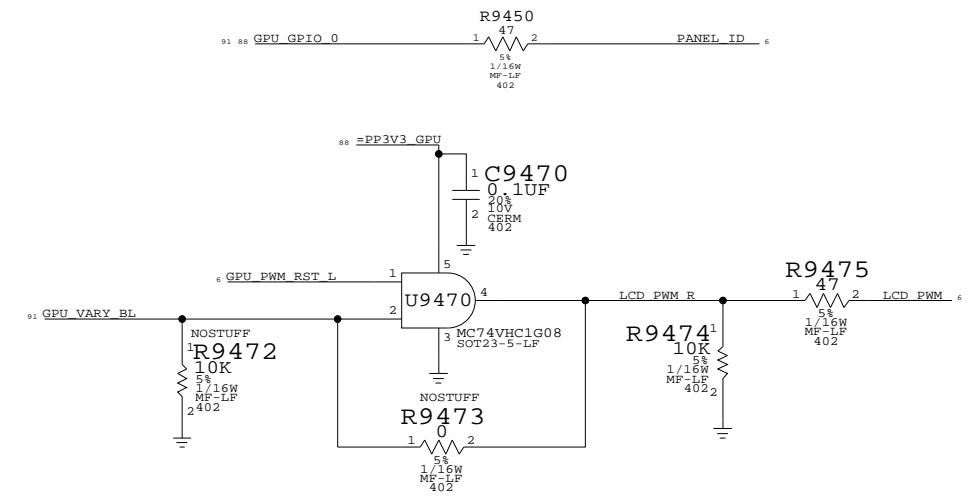
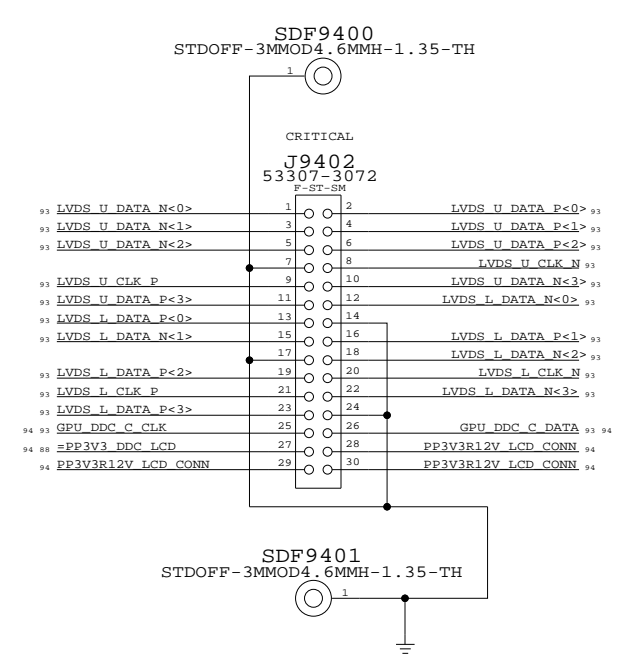
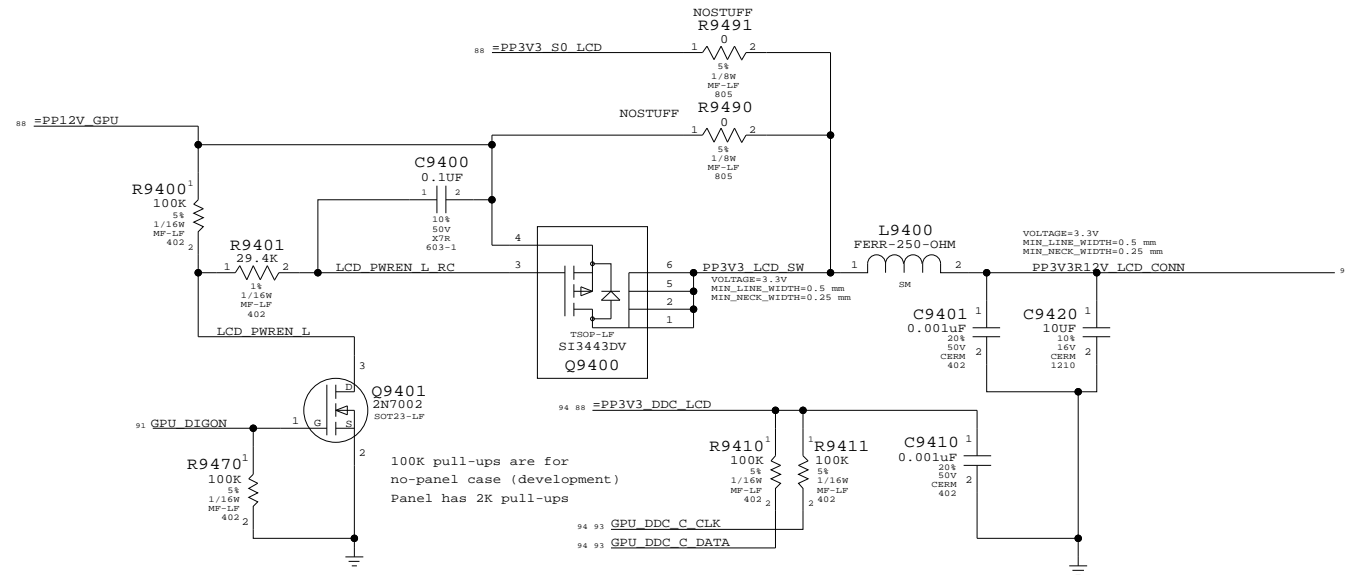
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|-----------------------------------|
| 338S0302 | 338S0266 | | U8400 | IC,ATI,M560,GRAFIX CTLR,88P8GA,LF |

INVERTER INTERFACE

LCD (LVDS) INTERFACE



Internal Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/27/2005
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| | D | 051-6950 | 06 |
| SCALE | SHT | OF | |
| NONE | 94 | 111 | |

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TP TMSD DATA P<3> == TMSD DATA P<3> 91
 MAKE_BASE=TRUE

TP TMSD DATA N<3> == TMSD DATA N<3> 91
 MAKE_BASE=TRUE

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 MAKE_BASE=TRUE

TP TMSD DATA N<4> == TMSD DATA N<4> 91
 MAKE_BASE=TRUE

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 MAKE_BASE=TRUE

TP TMSD DATA N<5> == TMSD DATA N<5> 91
 MAKE_BASE=TRUE

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 MAKE_BASE=TRUE

TP ATI DVDPDATA<22> == ATI DVDPDATA<22> 91
 MAKE_BASE=TRUE

TP ATI DVDPDATA<21> == ATI DVDPDATA<21> 91
 MAKE_BASE=TRUE

TP ATI DVDPDATA<20> == ATI DVDPDATA<20> 91
 MAKE_BASE=TRUE

TP ATI DVDPDATA<19> == ATI DVDPDATA<19> 91
 MAKE_BASE=TRUE

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C

C

B

B

A

A

8

7

6

5

4

3

2

1

M56 TPS

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APPLE COMPUTER INC.

| | | |
|-------|----------------|------|
| SIZE | DRAWING NUMBER | REV. |
| D | 051-6949 | 09 |
| SCALE | SHT 95 OF 111 | |
| NONE | | |

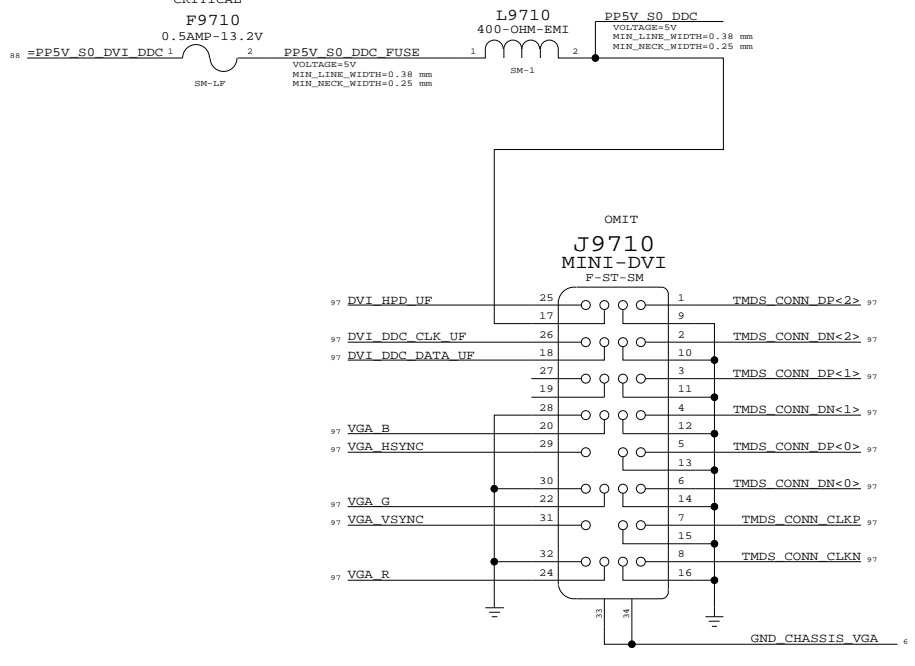
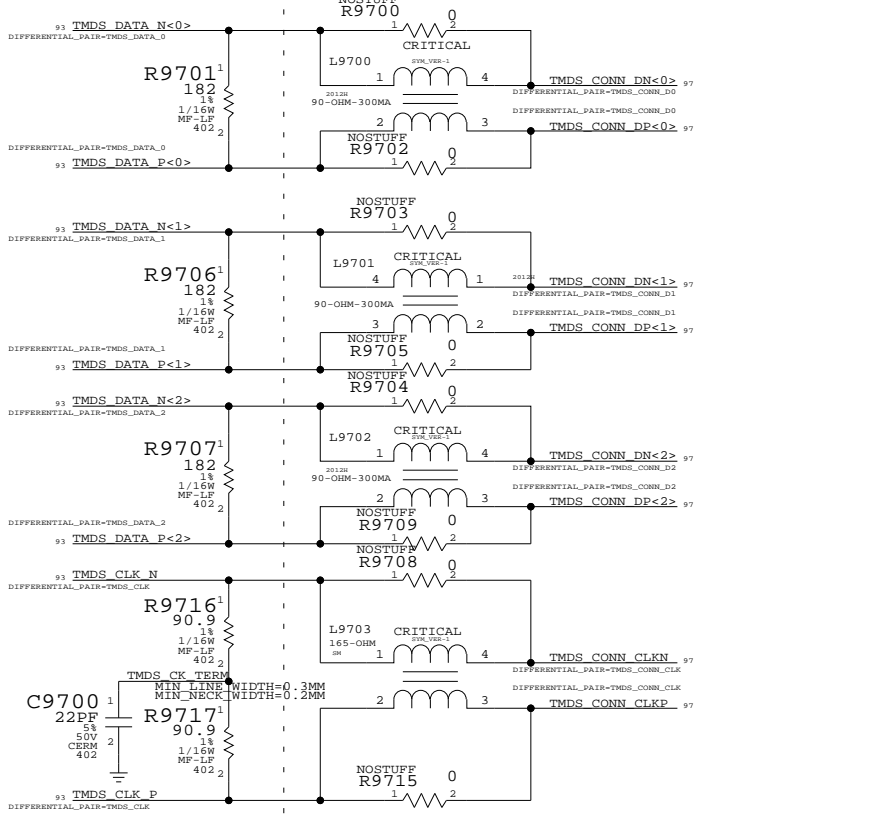
8 7 6 5 4 3 2 1

PLACE LEFT SIDE
AS CLOSE TO GPU (U8400)
AS POSSIBLE

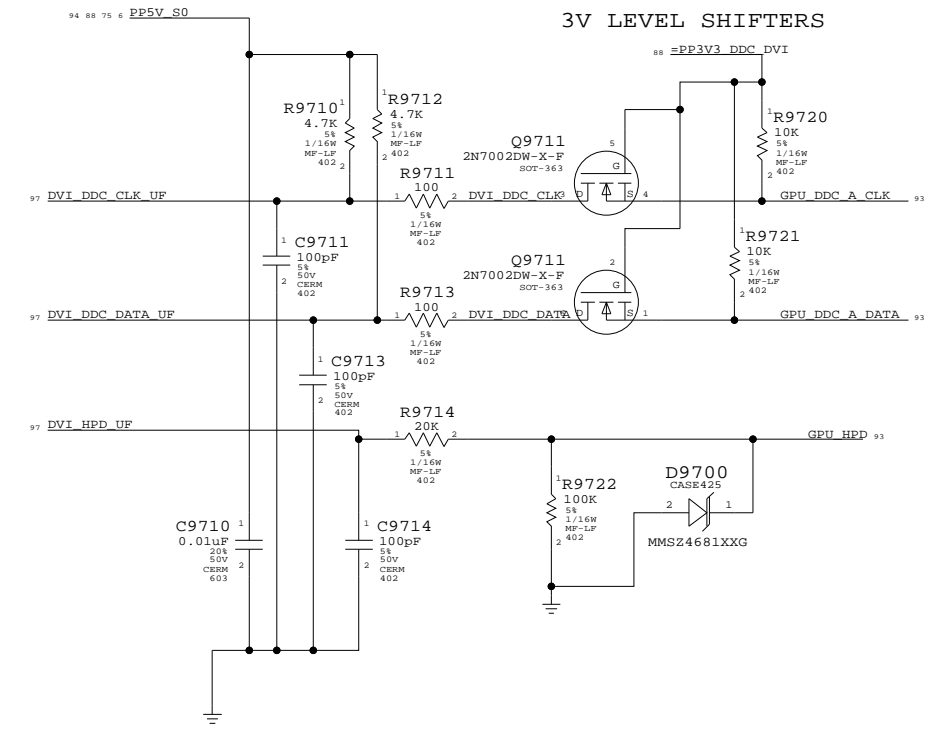
PLACE FILTER CLOSE
TO TMD5 CONNECTOR

DVI DDC CURRENT LIMIT DVI INTERFACE

(55mA requirement per DVI spec)

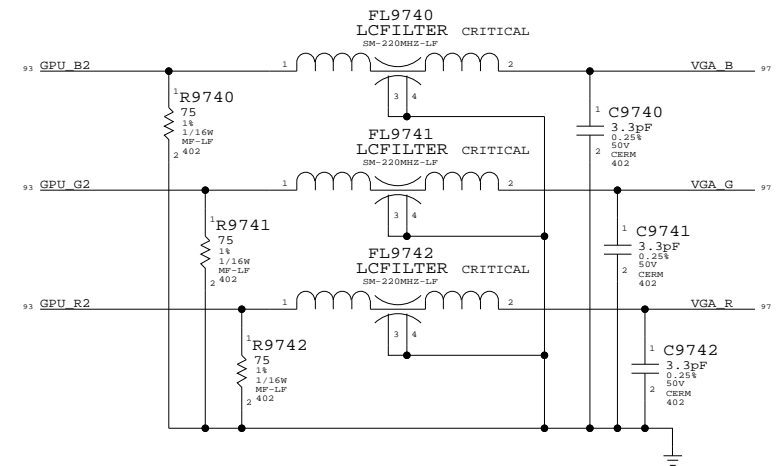


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|---------------------------------|-------------------------|----------|-------------|
| 51480114 | 1 | CONN, 32-P MINI-DVI RCPT MG3,LF | J9710 | CRITICAL | 17_INCH_LCD |
| 51480116 | 1 | CONN, 32-P MINI-DVI RCPT MG3,LF | J9710 | CRITICAL | 20_INCH_LCD |

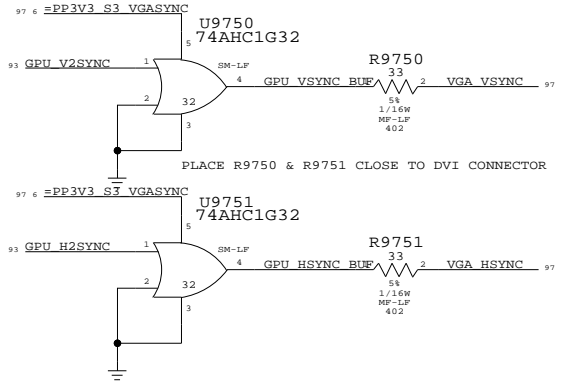


ANALOG FILTERING

PLACE CLOSE TO CONNECTOR



VGA SYNC BUFFERS



External Display Conns
 SYNC_MASTER=BOZEMAN SYNC_DATE=04/14/2005
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| | | | |
|---------------------|------|----------------|------|
| APPLE COMPUTER INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-6949 | 09 |
| SCALE | SHT | OF | |
| NONE | 97 | 111 | |

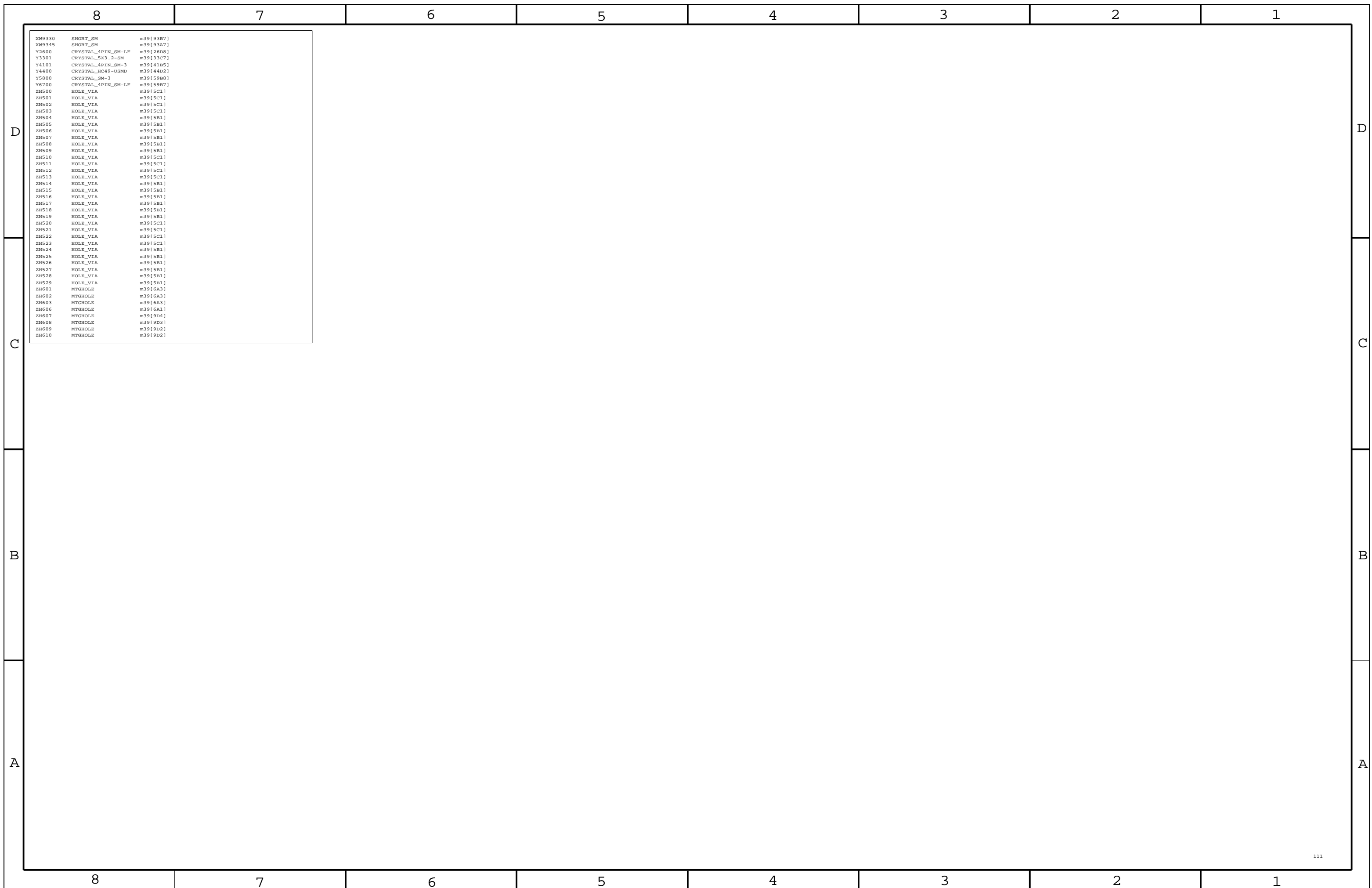
8 7 6 5 4 3 2 1

| | | | | | | | | | | | | | | |
|----------------|-------------------------------|------|-----------|-----------------|--------------------------------|------|------|-----------------------|--------------------------------------|--------------------------|---------------------|---|------|-----------|
| 8 | 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | |
| D | C | B | A | D | C | B | A | | | | | | | |
| PCI_AD<3> | PCI_AD<3> - @m39.lib.M39 | 2287 | 44D5 | PEG_R2D_C_N<3> | PEG_R2D_C_N<3> - @m39.lib.M39 | 1383 | 84B5 | PP1V8_FB_A0_VDDA0 | PP1V8_FB_A0_VDDA0 - @m39.lib.M39 | 89D7 | SB_RTC_X2 | SB_RTC_X2 - @m39.lib.M39 | 21D6 | 26D7 |
| PCI_AD<4> | PCI_AD<4> - @m39.lib.M39 | 2287 | 44D5 | PEG_R2D_C_N<4> | PEG_R2D_C_N<4> - @m39.lib.M39 | 1383 | 84B5 | PP1V8_FB_A1_VDDA0 | PP1V8_FB_A1_VDDA0 - @m39.lib.M39 | 89D7 | SB_SM_INTRUDER_L | SB_SM_INTRUDER_L - @m39.lib.M39 | 21D6 | 26C7 |
| PCI_AD<5> | PCI_AD<5> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<5> | PEG_R2D_C_N<5> - @m39.lib.M39 | 1383 | 84B5 | PP1V8_FB_A1_VDDA1 | PP1V8_FB_A1_VDDA1 - @m39.lib.M39 | 89D4 | SB_SPKR | SB_SPKR - @m39.lib.M39 | 23C5 | |
| PCI_AD<6> | PCI_AD<6> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<6> | PEG_R2D_C_N<6> - @m39.lib.M39 | 1383 | 84C5 | PP1V8_FB_B0_VDDA0 | PP1V8_FB_B0_VDDA0 - @m39.lib.M39 | 90D7 | SC_RX_L | SC_RX_L - @m39.lib.M39 | 58C5 | 59B6 59C4 |
| PCI_AD<7> | PCI_AD<7> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<7> | PEG_R2D_C_N<7> - @m39.lib.M39 | 1383 | 84C5 | PP1V8_FB_B0_VDDA1 | PP1V8_FB_B0_VDDA1 - @m39.lib.M39 | 90D7 | SC_TX_L | SC_TX_L - @m39.lib.M39 | 58C5 | 59B4 59B6 |
| PCI_AD<8> | PCI_AD<8> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<8> | PEG_R2D_C_N<8> - @m39.lib.M39 | 1383 | 84C5 | PP1V8_FB_B1_VDDA0 | PP1V8_FB_B1_VDDA0 - @m39.lib.M39 | 90D4 | SDVO_CTRLCLK | SDVO_CTRLCLK - @m39.lib.M39 | 14B6 | 19A2 |
| PCI_AD<9> | PCI_AD<9> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<9> | PEG_R2D_C_N<9> - @m39.lib.M39 | 1383 | 84C5 | PP1V8_FB_B1_VDDA1 | PP1V8_FB_B1_VDDA1 - @m39.lib.M39 | 90D4 | TP_SDVO_CTRLCLK | TP_SDVO_CTRLCLK - @m39.lib.M39 | 571 | 59C1 |
| PCI_AD<10> | PCI_AD<10> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<10> | PEG_R2D_C_N<10> - @m39.lib.M39 | 1383 | 84C5 | PP1V8_S3_PGOOD | PP1V8_S3_PGOOD - @m39.lib.M39 | 79A2 | SMB_ALERT_L | SMB_ALERT_L - @m39.lib.M39 | 23C5 | |
| PCI_AD<11> | PCI_AD<11> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<11> | PEG_R2D_C_N<11> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 77B8 77C5 | SMB_BSA_CLK | SMB_BSA_CLK - @m39.lib.M39 | 58B5 | 59C1 |
| PCI_AD<12> | PCI_AD<12> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<12> | PEG_R2D_C_N<12> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_BSA_DATA | SMB_BSA_DATA - @m39.lib.M39 | 58B5 | 59C1 |
| PCI_AD<13> | PCI_AD<13> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<13> | PEG_R2D_C_N<13> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_BSA_CLK | SMB_BSA_CLK - @m39.lib.M39 | 58C5 | 59D1 |
| PCI_AD<14> | PCI_AD<14> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<14> | PEG_R2D_C_N<14> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_BSA_DATA | SMB_BSA_DATA - @m39.lib.M39 | 58C7 | 59D1 |
| PCI_AD<15> | PCI_AD<15> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_N<15> | PEG_R2D_C_N<15> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_BSA_CLK | SMB_BSA_CLK - @m39.lib.M39 | 58C5 | 59D1 |
| PCI_AD<16> | PCI_AD<16> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<0> | PEG_R2D_C_P<0> - @m39.lib.M39 | 1383 | 84B5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_BSA_DATA | SMB_BSA_DATA - @m39.lib.M39 | 58C7 | 59D1 |
| PCI_AD<17> | PCI_AD<17> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<1> | PEG_R2D_C_P<1> - @m39.lib.M39 | 1383 | 84B5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_LINK_ALERT_L | SMB_LINK_ALERT_L - @m39.lib.M39 | 23D5 | |
| PCI_AD<18> | PCI_AD<18> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<2> | PEG_R2D_C_P<2> - @m39.lib.M39 | 1383 | 84B5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMB_ADAPTER_EN | SMB_ADAPTER_EN - @m39.lib.M39 | 58D5 | 59D5 |
| PCI_AD<19> | PCI_AD<19> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<3> | PEG_R2D_C_P<3> - @m39.lib.M39 | 1383 | 84B5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | TP_SMC_ADAPTER_EN | TP_SMC_ADAPTER_EN - @m39.lib.M39 | 59D3 | |
| PCI_AD<20> | PCI_AD<20> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<4> | PEG_R2D_C_P<4> - @m39.lib.M39 | 1383 | 84B5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | SMC_ANALOG_ID | SMC_ANALOG_ID - @m39.lib.M39 | 571 | 59C6 |
| PCI_AD<21> | PCI_AD<21> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<5> | PEG_R2D_C_P<5> - @m39.lib.M39 | 1383 | 84B5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C7 | NC_SMC_ANALOG_ID | NC_SMC_ANALOG_ID - @m39.lib.M39 | 59C5 | |
| PCI_AD<22> | PCI_AD<22> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<6> | PEG_R2D_C_P<6> - @m39.lib.M39 | 1383 | 84C5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | SMC_BATT_CHG_EN | SMC_BATT_CHG_EN - @m39.lib.M39 | 58D7 | 59D6 |
| PCI_AD<23> | PCI_AD<23> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<7> | PEG_R2D_C_P<7> - @m39.lib.M39 | 1383 | 84C5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | NC_SMC_BATT_CHG_EN | NC_SMC_BATT_CHG_EN - @m39.lib.M39 | 59D5 | |
| PCI_AD<24> | PCI_AD<24> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<8> | PEG_R2D_C_P<8> - @m39.lib.M39 | 1383 | 84C5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | SMC_BATT_ISENSE | SMC_BATT_ISENSE - @m39.lib.M39 | 58D5 | 59B6 |
| PCI_AD<25> | PCI_AD<25> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<9> | PEG_R2D_C_P<9> - @m39.lib.M39 | 1383 | 84C5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | UNUSED_SMC_SENSE | UNUSED_SMC_SENSE - @m39.lib.M39 | 59B5 | 59B6 |
| PCI_AD<26> | PCI_AD<26> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<10> | PEG_R2D_C_P<10> - @m39.lib.M39 | 1383 | 84C5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | SMC_FWIRE_ISENSE | SMC_FWIRE_ISENSE - @m39.lib.M39 | 58D5 | 59B6 |
| PCI_AD<27> | PCI_AD<27> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<11> | PEG_R2D_C_P<11> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | UNUSED_SMC_SENSE | UNUSED_SMC_SENSE - @m39.lib.M39 | 59B5 | 59B6 |
| PCI_AD<28> | PCI_AD<28> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<12> | PEG_R2D_C_P<12> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | SMC_FWIRE_ISENSE | SMC_FWIRE_ISENSE - @m39.lib.M39 | 58D5 | 59B6 |
| PCI_AD<29> | PCI_AD<29> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<13> | PEG_R2D_C_P<13> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | SMC_BATT_ISET | SMC_BATT_ISET - @m39.lib.M39 | 58B5 | 59B6 |
| PCI_AD<30> | PCI_AD<30> - @m39.lib.M39 | 2287 | 44C5 | PEG_R2D_C_P<14> | PEG_R2D_C_P<14> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | NC_SMC_BATT_ISET | NC_SMC_BATT_ISET - @m39.lib.M39 | 59D5 | |
| PCI_AD<31> | PCI_AD<31> - @m39.lib.M39 | 2287 | 44B5 | PEG_R2D_C_P<15> | PEG_R2D_C_P<15> - @m39.lib.M39 | 1383 | 84D5 | PP2V5_S0_PGOOD | PP2V5_S0_PGOOD - @m39.lib.M39 | 93C8 | SMC_BATT_TRICKLE_EN | SMC_BATT_TRICKLE_EN - @m39.lib.M39 | 58D7 | 59D6 |
| PCI_CLK_FW | PCI_CLK_FW - @m39.lib.M39 | 34C4 | 44B5 | PEG_R2D_N<0> | PEG_R2D_N<0> - @m39.lib.M39 | 84D4 | | PP3V3_VFW_RSD | PP3V3_VFW_RSD - @m39.lib.M39 | 46A7 | L | NC_SMC_BATT_TRICKLE_EN_L - @m39.lib.M39 | 59D5 | |
| PCI_CLK_PORT80 | PCI_CLK_PORT80 - @m39.lib.M39 | 34B4 | 60C3 | PEG_R2D_N<1> | PEG_R2D_N<1> - @m39.lib.M39 | 84D4 | | PP3V3_VFW_RSD_F | PP3V3_VFW_RSD_F - @m39.lib.M39 | 46A7 | SMC_BC_ACOK | SMC_BC_ACOK - @m39.lib.M39 | 58C5 | 59B4 |
| PCI_CLK_SB | PCI_CLK_SB - @m39.lib.M39 | 5C8 | 22A6 34B4 | PEG_R2D_N<2> | PEG_R2D_N<2> - @m39.lib.M39 | 84D4 | | PP3V3_AVCC_SMC | PP3V3_AVCC_SMC - @m39.lib.M39 | 58D3 | SMC_BS_ALERT_L | SMC_BS_ALERT_L - @m39.lib.M39 | 58C5 | 59B4 |
| PCI_CLK_SMC | PCI_CLK_SMC - @m39.lib.M39 | 34C4 | 58C7 | PEG_R2D_N<3> | PEG_R2D_N<3> - @m39.lib.M39 | 84D4 | | PP3V3_AVREF_SMC | PP3V3_AVREF_SMC - @m39.lib.M39 | 58D2 59A3 | SMC_CS_ALIGN | SMC_CS_ALIGN - @m39.lib.M39 | 58C5 | 59B6 |
| PCI_CLK_TPM | PCI_CLK_TPM - @m39.lib.M39 | 34C4 | 67C6 | PEG_R2D_N<4> | PEG_R2D_N<4> - @m39.lib.M39 | 84D4 | | PP3V3_AVREF_SMC | PP3V3_AVREF_SMC - @m39.lib.M39 | 58D2 59A3 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 76D2 |
| PCI_C_BE_L<0> | PCI_C_BE_L<0> - @m39.lib.M39 | 22B6 | 44B5 | PEG_R2D_N<5> | PEG_R2D_N<5> - @m39.lib.M39 | 84C4 | | PP3V3_FW_RSD | PP3V3_FW_RSD - @m39.lib.M39 | 46A5 46A6 46B5 46C5 46D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_C_BE_L<1> | PCI_C_BE_L<1> - @m39.lib.M39 | 22B6 | 44B5 | PEG_R2D_N<6> | PEG_R2D_N<6> - @m39.lib.M39 | 84C4 | | PP3V3_FW_RSD_F | PP3V3_FW_RSD_F - @m39.lib.M39 | 46A7 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_C_BE_L<2> | PCI_C_BE_L<2> - @m39.lib.M39 | 22B6 | 44B5 | PEG_R2D_N<7> | PEG_R2D_N<7> - @m39.lib.M39 | 84C4 | | PP3V3_INTERCON | PP3V3_INTERCON - @m39.lib.M39 | 46C7 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_C_BE_L<3> | PCI_C_BE_L<3> - @m39.lib.M39 | 22B6 | 44B5 | PEG_R2D_N<8> | PEG_R2D_N<8> - @m39.lib.M39 | 84C4 | | PP3V3_LCDC_SW | PP3V3_LCDC_SW - @m39.lib.M39 | 94C6 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_DEVSSEL_L | PCI_DEVSSEL_L - @m39.lib.M39 | 22A6 | 26D2 44B5 | PEG_R2D_N<9> | PEG_R2D_N<9> - @m39.lib.M39 | 84B4 | | PP3V3_LCDC_SW | PP3V3_LCDC_SW - @m39.lib.M39 | 94C6 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_FRAME_L | PCI_FRAME_L - @m39.lib.M39 | 22A7 | 26D2 44B5 | PEG_R2D_N<10> | PEG_R2D_N<10> - @m39.lib.M39 | 84B4 | | PP3V3_S0_CK410_VDDA0 | PP3V3_S0_CK410_VDDA0 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_GNT3_L | PCI_GNT3_L - @m39.lib.M39 | 22B4 | 44B5 | PEG_R2D_N<11> | PEG_R2D_N<11> - @m39.lib.M39 | 84B4 | | PP3V3_S0_CK410_VDDA1 | PP3V3_S0_CK410_VDDA1 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_IDSEL | PCI_IDSEL - @m39.lib.M39 | 44B5 | | PEG_R2D_N<12> | PEG_R2D_N<12> - @m39.lib.M39 | 84B4 | | PP3V3_S0_CK410_VDDA2 | PP3V3_S0_CK410_VDDA2 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_IRDY_L | PCI_IRDY_L - @m39.lib.M39 | 22A6 | 26D2 44B5 | PEG_R2D_N<13> | PEG_R2D_N<13> - @m39.lib.M39 | 84B4 | | PP3V3_S0_CK410_VDDA3 | PP3V3_S0_CK410_VDDA3 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_LOCK_L | PCI_LOCK_L - @m39.lib.M39 | 22A6 | 26D2 | PEG_R2D_N<14> | PEG_R2D_N<14> - @m39.lib.M39 | 84B4 | | PP3V3_S0_CK410_VDDA4 | PP3V3_S0_CK410_VDDA4 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_PAR | PCI_PAR - @m39.lib.M39 | 22A6 | 44B5 | PEG_R2D_N<15> | PEG_R2D_N<15> - @m39.lib.M39 | 84B4 | | PP3V3_S0_CK410_VDDA5 | PP3V3_S0_CK410_VDDA5 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_PERR_L | PCI_PERR_L - @m39.lib.M39 | 22A6 | 26D2 44B5 | PEG_R2D_P<0> | PEG_R2D_P<0> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA6 | PP3V3_S0_CK410_VDDA6 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_RST_FWL | PCI_RST_FWL - @m39.lib.M39 | 44A7 | 44B5 | PEG_R2D_P<1> | PEG_R2D_P<1> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA7 | PP3V3_S0_CK410_VDDA7 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_RST_L | PCI_RST_L - @m39.lib.M39 | 22A6 | 44A8 | PEG_R2D_P<2> | PEG_R2D_P<2> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA8 | PP3V3_S0_CK410_VDDA8 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_SERR_L | PCI_SERR_L - @m39.lib.M39 | 22A6 | 26D2 44B5 | PEG_R2D_P<3> | PEG_R2D_P<3> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA9 | PP3V3_S0_CK410_VDDA9 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_STOP_L | PCI_STOP_L - @m39.lib.M39 | 22A6 | 26D2 44B5 | PEG_R2D_P<4> | PEG_R2D_P<4> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA10 | PP3V3_S0_CK410_VDDA10 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_TRDY_L | PCI_TRDY_L - @m39.lib.M39 | 22A6 | 26D2 44B5 | PEG_R2D_P<5> | PEG_R2D_P<5> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA11 | PP3V3_S0_CK410_VDDA11 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PCI_COMP | PCI_COMP - @m39.lib.M39 | 13D3 | | PEG_R2D_P<6> | PEG_R2D_P<6> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA12 | PP3V3_S0_CK410_VDDA12 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PEG_D2R_C_N<0> | PEG_D2R_C_N<0> - @m39.lib.M39 | 84D3 | | PEG_R2D_P<7> | PEG_R2D_P<7> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA13 | PP3V3_S0_CK410_VDDA13 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PEG_D2R_C_N<1> | PEG_D2R_C_N<1> - @m39.lib.M39 | 84D3 | | PEG_R2D_P<8> | PEG_R2D_P<8> - @m39.lib.M39 | 84D4 | | PP3V3_S0_CK410_VDDA14 | PP3V3_S0_CK410_VDDA14 - @m39.lib.M39 | 33D5 | SMC_CPU_ISENSE | SMC_CPU_ISENSE - @m39.lib.M39 | 58B5 | 59A7 |
| PEG_D2R_C_N<2> | PEG_D2R_C_N<2> - @m39.lib.M39 | | | | | | | | | | | | | |

| 8 | | | 7 | | | 6 | | | 5 | | | 4 | | | 3 | | | 2 | | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|-------|---------|-----------|-------|---------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|----------|-----------|-------|---------|-----------|-------|----------|-----------|-------|------------|-----------|-------|---------|-----------|-------|----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|--------------------|-----------|-------|--------------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|--------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|----------|-----------|-------|----------|-----------|-------|--------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|--------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|--------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|----------------|-----------|-------|----------|-----------|-------|---------|-----------|-------|----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|----------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------------|-----------|-------|-----------------|-----------|-------|-----------------|-----------|-------|-----------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|-----------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|--------------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|---------|-----------|-------|----------|-----------|-------|----------|-----------|-------|---------|-----------|-------|---------|-----------|
| Title: Cref Part Report Design: m39 Date: Dec 6 19:54:16 2005 | | | C2515 | CAP_402 | m39[25B6] | C2516 | CAP_P_CASE-C2 | m39[25D3] | C2517 | CAP_402 | m39[25D6] | C2518 | CAP_402 | m39[25D4] | C2519 | CAP_402 | m39[25D3] | C2520 | CAP_402 | m39[25B6] | C2521 | CAP_402 | m39[25C3] | C2522 | CAP_402 | m39[25B3] | C2523 | CAP_402 | m39[25B4] | C2524 | CAP_603 | m39[25B3] | C2525 | CAP_402 | m39[25B3] | C2526 | CAP_402 | m39[25A4] | C2527 | CAP_402 | m39[25A3] | C2528 | CAP_402 | m39[25A3] | C2529 | CAP_402 | m39[25A3] | C2530 | CAP_402 | m39[25A3] | C2531 | CAP_402 | m39[25D1] | C2532 | CAP_402 | m39[25C1] | C2533 | CAP_402 | m39[25C1] | C2534 | CAP_402 | m39[25D1] | C2605 | CAP_402 | m39[26C7] | C2607 | CAP_402 | m39[26D5] | C2608 | CAP_402 | m39[26D8] | C2609 | CAP_402 | m39[26D8] | C2610 | CAP_402 | m39[26C7] | C2611 | CAP_402 | m39[26B7] | C2698 | CAP_402 | m39[26C4] | C2699 | CAP_402 | m39[26C5] | C2800 | CAP_402 | m39[28D6] | C2801 | CAP_603 | m39[28B2] | C2802 | CAP_603 | m39[28B2] | C2803 | CAP_603 | m39[28B1] | C2804 | CAP_603 | m39[28B1] | C2810 | CAP_402 | m39[28B2] | C2811 | CAP_402 | m39[28B2] | C2812 | CAP_402 | m39[28B1] | C2813 | CAP_402 | m39[28B1] | C2814 | CAP_402 | m39[28B1] | C2815 | CAP_402 | m39[28B2] | C2816 | CAP_402 | m39[28B1] | C2817 | CAP_402 | m39[28B1] | C2818 | CAP_402 | m39[28B2] | C2819 | CAP_402 | m39[28B2] | C2820 | CAP_402 | m39[28B1] | C2821 | CAP_402 | m39[28B1] | C2850 | CAP_603 | m39[28D6] | C2851 | CAP_603 | m39[28A6] | C2852 | CAP_402 | m39[28A6] | C2900 | CAP_402 | m39[29D6] | C2908 | CAP_402 | m39[29B2] | C2909 | CAP_402 | m39[29B2] | C2910 | CAP_402 | m39[29B1] | C2911 | CAP_402 | m39[29B1] | C2912 | CAP_402 | m39[29B2] | C2913 | CAP_402 | m39[29B2] | C2914 | CAP_402 | m39[29B1] | C2915 | CAP_402 | m39[29B1] | C2916 | CAP_402 | m39[29B2] | C2917 | CAP_402 | m39[29B2] | C2918 | CAP_402 | m39[29B1] | C2919 | CAP_402 | m39[29B1] | C2920 | CAP_402 | m39[29B2] | C2921 | CAP_402 | m39[29B2] | C2922 | CAP_402 | m39[29B1] | C2923 | CAP_402 | m39[29B1] | C2950 | CAP_603 | m39[29D6] | C2951 | CAP_402 | m39[29A7] | C2952 | CAP_402 | m39[29A6] | C3004 | CAP_402 | m39[30B4] | C3005 | CAP_402 | m39[30D4] | C3006 | CAP_402 | m39[30B3] | C3007 | CAP_402 | m39[30D3] | C3008 | CAP_402 | m39[30A3] | C3009 | CAP_402 | m39[30A4] | C3010 | CAP_402 | m39[30D4] | C3011 | CAP_402 | m39[30D3] | C3013 | CAP_402 | m39[30A4] | C3014 | CAP_402 | m39[30A4] | C3015 | CAP_402 | m39[30A3] | C3030 | CAP_402 | m39[30C4] | C3033 | CAP_402 | m39[30C3] | C3035 | CAP_402 | m39[30C3] | C3100 | CAP_402 | m39[31C4] | C3101 | CAP_603 | m39[31B6] | C3102 | CAP_603 | m39[31B4] | C3105 | CAP_402 | m39[31B4] | C3109 | CAP_603 | m39[31C5] | C3110 | CAP_402 | m39[31B6] | C3301 | CAP_402 | m39[33D6] | C3302 | CAP_402 | m39[33D6] | C3303 | CAP_402 | m39[33D6] | C3304 | CAP_402 | m39[33D6] | C3305 | CAP_402 | m39[33D4] | C3306 | CAP_402 | m39[33D4] | C3307 | CAP_402 | m39[33C4] | C3308 | CAP_402 | m39[33D4] | C3309 | CAP_603 | m39[33D4] | C3310 | CAP_402 | m39[33D3] | C3311 | CAP_402 | m39[33C6] | C3312 | CAP_603 | m39[33C6] | C3314 | CAP_402 | m39[33D8] | C3315 | CAP_402 | m39[33D7] | C3316 | CAP_603 | m39[33D7] | C3317 | CAP_603 | m39[33D4] | C3389 | CAP_402 | m39[33C7] | C3390 | CAP_402 | m39[33C7] | C3800 | CAP_402 | m39[38B7] | C3801 | CAP_402 | m39[38B7] | C3802 | CAP_402 | m39[38B7] | C3803 | CAP_402 | m39[38B7] | C3804 | CAP_402 | m39[38C3] | C3805 | CAP_402 | m39[38C2] | C3806 | CAP_805-2 | m39[38C1] | C4101 | CAP_402 | m39[41D7] | C4102 | CAP_402 | m39[41D6] | C4103 | CAP_402 | m39[41D6] | C4104 | CAP_402 | m39[41D6] | C4105 | CAP_402 | m39[41D5] | C4106 | CAP_402 | m39[41D2] | C4107 | CAP_402 | m39[41D2] | C4110 | CAP_402 | m39[41D4] | C4111 | CAP_402 | m39[41D4] | C4112 | CAP_402 | m39[41C4] | C4113 | CAP_402 | m39[41C4] | C4115 | CAP_402 | m39[41B5] | C4116 | CAP_402 | m39[41B5] | C4117 | CAP_402 | m39[41B2] | C4118 | CAP_402 | m39[41B2] | C4126 | CAP_402 | m39[41A8] | C4127 | CAP_402 | m39[41A8] | C4128 | CAP_402 | m39[41A8] | C4129 | CAP_402 | m39[41A8] | C4130 | CAP_402 | m39[41A7] | C4131 | CAP_402 | m39[41A7] | C4132 | CAP_402 | m39[41A7] | C4133 | CAP_402 | m39[41A6] | C4134 | CAP_402 | m39[41A6] | C4135 | CAP_402 | m39[41A5] | C4136 | CAP_402 | m39[41A5] | C4137 | CAP_402 | m39[41A5] | C4138 | CAP_402 | m39[41A4] | C4139 | CAP_402 | m39[41A4] | C4140 | CAP_402 | m39[41B3] | C4150 | CAP_402 | m39[41D5] | C4200 | CAP_1210 | m39[42D8] | C4201 | CAP_402 | m39[42D7] | C4202 | CAP_1210 | m39[42D7] | C4203 | CAP_1206-1 | m39[42D6] | C4204 | CAP_402 | m39[42D6] | C4205 | CAP_1210 | m39[42C5] | C4206 | CAP_402 | m39[42C5] | C4209 | CAP_603 | m39[42B7] | C4210 | CAP_402 | m39[42B6] | C4300 | CAP_402 | m39[43D7] | C4301 | CAP_402 | m39[43D6] | C4304 | CAP_402 | m39[43C6] | C4305 | CAP_402 | m39[43B6] | C4401 | CAP_402 | m39[44D1] | C4402 | CAP_402 | m39[44C1] | C4410 | CAP_402 | m39[44D6] | C4412 | CAP_402 | m39[44D1] | C4500 | CAP_402 | m39[45D4] | C4501 | CAP_402 | m39[45D3] | C4502 | CAP_402 | m39[45D3] | C4503 | CAP_603 | m39[45C6] | C4504 | CAP_402 | m39[45C4] | C4505 | CAP_402 | m39[45C5] | C4506 | CAP_402 | m39[45C5] | C4507 | CAP_402 | m39[45C5] | C4508 | CAP_402 | m39[45D5] | C4509 | CAP_402 | m39[45D5] | C4510 | CAP_402 | m39[45D5] | C4515 | CAP_603 | m39[45D6] | C4520 | CAP_402 | m39[45D5] | C4521 | CAP_402 | m39[45D4] | C4522 | CAP_402 | m39[45D3] | C4523 | CAP_402 | m39[45D3] | C4609 | CAP_603-1 | m39[46D5] | C4610 | CAP_402 | m39[46D4] | C4611 | CAP_402 | m39[46D4] | C4612 | CAP_402 | m39[46C4] | C4613 | CAP_402 | m39[46C4] | C4615 | CAP_603-1 | m39[46C2] | C4616 | CAP_402 | m39[46B2] | C4620 | CAP_402 | m39[46B4] | C4621 | CAP_402 | m39[46B4] | C4622 | CAP_402 | m39[46A4] | C4623 | CAP_402 | m39[46A4] | C4625 | CAP_603-1 | m39[46A2] | C4626 | CAP_402 | m39[46A2] | C4650 | CAP_402 | m39[46C7] | C4654 | CAP_402 | m39[46B8] | C4660 | CAP_402 | m39[46C7] | C4664 | CAP_402 | m39[46B7] | C4710 | CAP_P_SMB2 | m39[47D6] | C4712 | CAP_402 | m39[47D5] | C4713 | CAP_402 | m39[47D5] | C4720 | CAP_P_SMBD | m39[47C6] | C4722 | CAP_402 | m39[47C5] | C4723 | CAP_402 | m39[47C5] | C4732 | CAP_402 | m39[47A5] | C4733 | CAP_402 | m39[47A5] | C4742 | CAP_402 | m39[47D2] | C4743 | CAP_402 | m39[47D1] | C4797 | CAP_805-2 | m39[47D3] | C4798 | CAP_402 | m39[47A2] | C4799 | CAP_805-2 | m39[47A2] | C4950 | CAP_805-2 | m39[49C4] | C4951 | CAP_402 | m39[49C4] | C5300 | CAP_402 | m39[53B7] | C5301 | CAP_402 | m39[53B7] | C5304 | CAP_402 | m39[53D5] | C5305 | CAP_402 | m39[53D5] | C5306 | CAP_402 | m39[53D4] | C5307 | CAP_402 | m39[53C4] | C5308 | CAP_402 | m39[53C5] | C5309 | CAP_402 | m39[53C4] | C5310 | CAP_402 | m39[53C3] | C5311 | CAP_603 | m39[53D4] | C5312 | CAP_603 | m39[53D4] | C5313 | CAP_402 | m39[53C5] | C5314 | CAP_603 | m39[53C4] | C5800 | CAP_402 | m39[58B8] | C5801 | CAP_402 | m39[58B8] | C5802 | CAP_805 | m39[58D3] | C5803 | CAP_402 | m39[58D2] | C5804 | CAP_402 | m39[58D2] | C5805 | CAP_402 | m39[58D2] | C5806 | CAP_402 | m39[58D1] | C5807 | CAP_402 | m39[58D2] | C5820 | CAP_402 | m39[58C3] | C5900 | CAP_402 | m39[59D8] | C5901 | CAP_402 | m39[59D8] | C5902 | CAP_402 | m39[59B7] | C5903 | CAP_402 | m39[59A8] | C5919 | CAP_402 | m39[59B4] | C5940 | CAP_402 | m39[59A4] | C5941 | CAP_402 | m39[59A3] | C5942 | CAP_603 | m39[59A3] | C5943 | CAP_402 | m39[59A5] | C6000 | CAP_402 | m39[60D6] | C6001 | CAP_402 | m39[60D6] | C6002 | CAP_402 | m39[60C6] | C6003 | CAP_402 | m39[60C6] | C6100 | CAP_402 | m39[61B5] | C6101 | CAP_402 | m39[61B5] | C6301 | CAP_402 | m39[63C2] | C6308 | CAP_402 | m39[63C5] | C6309 | CAP_402 | m39[63C6] | C6311 | CAP_402 | m39[63C2] | C6312 | CAP_402 | m39[63D3] | C6500 | CAP_603 | m39[65D5] | C6501 | CAP_805 | m39[65D5] | C6502 | CAP_603 | m39[65B4] | C6503 | CAP_805 | m39[65B5] | C6504 | CAP_P_6_3X11-TH-LF | m39[65C4] | C6505 | CAP_P_6_3X11-TH-LF | m39[65B3] | C6600 | CAP_603 | m39[66D4] | C6601 | CAP_805 | m39[66C5] | C6602 | CAP_P_SMA-LF | m39[66C3] | C6650 | CAP_402 | m39[66B5] | C6651 | CAP_402 | m39[66A5] | C6652 | CAP_402 | m39[66B3] | C6653 | CAP_402 | m39[66A3] | C6654 | CAP_402 | m39[66B4] | C6700 | CAP_402 | m39[67C4] | C6701 | CAP_402 | m39[67C4] | C6702 | CAP_402 | m39[67C3] | C6703 | CAP_402 | m39[67C3] | C6704 | CAP_402 | m39[59B7] | C6705 | CAP_402 | m39[59B7] | C6800 | CAP_603 | m39[68D6] | C6801 | CAP_402 | m39[68D6] | C6802 | CAP_P_B2 | m39[68D4] | C6803 | CAP_P_B2 | m39[68D3] | C6804 | CAP_P_SMA-LF | m39[68B4] | C6805 | CAP_805 | m39[68B3] | C6806 | CAP_805 | m39[68B3] | C6807 | CAP_P_SMA-LF | m39[68B3] | C6808 | CAP_402 | m39[68B3] | C6809 | CAP_402 | m39[68B2] | C6810 | CAP_P_SMA-LF | m39[68B2] | C6811 | CAP_402 | m39[68B2] | C6812 | CAP_402 | m39[68A7] | C6813 | CAP_402 | m39[68B3] | C6821 | CAP_402 | m39[68C6] | C6822 | CAP_603 | m39[68A5] | C6823 | CAP_402 | m39[68A4] | C6825 | CAP_402 | m39[68A3] | C6826 | CAP_603 | m39[68A3] | C6829 | CAP_402 | m39[68B3] | C6830 | CAP_402 | m39[68D4] | C6832 | CAP_402 | m39[68B2] | C6833 | CAP_402 | m39[68B3] | C6834 | CAP_402 | m39[68B2] | C6835 | CAP_402 | m39[68D6] | C6836 | CAP_402 | m39[68D3] | C7200 | CAP_P_6_3X8-SM | m39[72D5] | C7201 | CAP_1210 | m39[72D5] | C7202 | CAP_805 | m39[72D4] | C7203 | CAP_1210 | m39[72D3] | C7204 | CAP_805 | m39[72D6] | C7205 | CAP_805 | m39[72C6] | C7206 | CAP_805 | m39[72C6] | C7207 | CAP_805 | m39[72C6] | C7208 | CAP_603-1 | m39[72C4] | C7209 | CAP_805 | m39[72B4] | C7210 | CAP_402 | m39[72B3] | C7211 | CAP_402 | m39[72B2] | C7212 | CAP_402 | m39[72B2] | C7213 | CAP_402 | m39[72B2] | C7214 | CAP_603 | m39[72B5] | C7215 | CAP_402 | m39[72C6] | C7216 | CAP_402 | m39[72C6] | C7217 | CAP_P_6_3X8-SM | m39[72D6] | C7218 | CAP_603 | m39[72D5] | C7219 | CAP_603 | m39[72D4] | C7220 | CAP_402 | m39[72B7] | C7221 | CAP_402 | m39[72B7] | C7223 | CAP_1210 | m39[72D3] | C7300 | CAP_402 | m39[73D7] | C7301 | CAP_402 | m39[73D6] | C7302 | CAP_402 | m39[73D6] | C7303 | CAP_402 | m39[73D6] | C7311 | CAP_402 | m39[73A7] | C7312 | CAP_402 | m39[73A6] | C7313 | CAP_402 | m39[73A6] | C7314 | CAP_402 | m39[73A7] | C7315 | CAP_402 | m39[73A6] | C7317 | CAP_402 | m39[73B4] | C7318 | CAP_805 | m39[73B4] | C7321 | CAP_402 | m39[73C5] | C7322 | CAP_402 | m39[73C6] | C7323 | CAP_402 | m39[73A6] | C7324 | CAP_402 | m39[73A5] | C7400 | CAP_402 | m39[74B4] | C7401 | CAP_402 | m39[74C4] | C7402 | CAP_402 | m39[74A4] | C7403 | CAP_P_CASE-B-SM | m39[74B7] | C7404 | CAP_P_CASE-B-SM | m39[74B6] | C7405 | CAP_P_CASE-B-SM | m39[74C7] | C7406 | CAP_P_CASE-B-SM | m39[74C6] | C7407 | CAP_402 | m39[74D8] | C7408 | CAP_402 | m39[74D7] | C7409 | CAP_402 | m39[74B8] | C7410 | CAP_402 | m39[74A8] | C7411 | CAP_402 | m39[74B8] | C7412 | CAP_402 | m39[74A8] | C7413 | CAP_402 | m39[74A8] | C7414 | CAP_402 | m39[74A7] | C7415 | CAP_402 | m39[74A8] | C7416 | CAP_402 | m39[74A8] | C7417 | CAP_402 | m39[74A8] | C7418 | CAP_805 | m39[74A5] | C7419 | CAP_603-1 | m39[74A4] | C7420 | CAP_402 | m39[74A7] | C7421 | CAP_402 | m39[74A7] | C7422 | CAP_402 | m39[74A7] | C7423 | CAP_402 | m39[74A7] | C7500 | CAP_402 | m39[75C4] | C7501 | CAP_P_TH-MCZ | m39[75C2] | C7502 | CAP_603 | m39[75C2] | C7503 | CAP_402 | m39[75C1] | C7504 | CAP_402 | m39[75B1] | C7505 | CAP_402 | m39[75C8] | C7506 | CAP_402 | m39[75B7] | C7507 | CAP_402 | m39[75B7] | C7508 | CAP_1210 | m39[75C2] | C7509 | CAP_1210 | m39[75D1] | C7510 | CAP_402 | m39[75C8] | C7511 | CAP_603 | m39[75B2] |

| | 8 | | | 7 | | | 6 | | | 5 | | | 4 | | | 3 | | | 2 | | | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | J600 | CON_M14RT_D_THA_RT-M | m39[507] | L7500 | IND_SM | m39[75D1] | PP627 | PROBEPOINT_SM | m39[5C8] | PP8908 | PROBEPOINT_SM | m39[5B5] | PP8914 | PROBEPOINT_SM | m39[5A5] | PP8920 | PROBEPOINT_SM | m39[5A5] | PP8926 | PROBEPOINT_SM | m39[5A5] | PP8932 | PROBEPOINT_SM | m39[5A5] | PP8938 | PROBEPOINT_SM | m39[5A5] | PP8944 | PROBEPOINT_SM | m39[5A5] | PP8950 | PROBEPOINT_SM | m39[5A5] | PP8956 | PROBEPOINT_SM | m39[5A5] | PP8962 | PROBEPOINT_SM | m39[5A5] | PP8968 | PROBEPOINT_SM | m39[5A5] | PP8974 | PROBEPOINT_SM | m39[5A5] | PP8980 | PROBEPOINT_SM | m39[5A5] | PP8986 | PROBEPOINT_SM | m39[5A5] | PP8992 | PROBEPOINT_SM | m39[5A5] | PP8998 | PROBEPOINT_SM | m39[5A5] | PP9004 | PROBEPOINT_SM | m39[5A5] | PP9010 | PROBEPOINT_SM | m39[5A5] | PP9016 | PROBEPOINT_SM | m39[5A5] | PP9022 | PROBEPOINT_SM | m39[5A5] | PP9028 | PROBEPOINT_SM | m39[5A5] | PP9034 | PROBEPOINT_SM | m39[5A5] | PP9040 | PROBEPOINT_SM | m39[5A5] | PP9046 | PROBEPOINT_SM | m39[5A5] | PP9052 | PROBEPOINT_SM | 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| m39[66D8] | 66C5] | Q7200 | TRA_2N7002DM_SOT-363 | m39[72B6] | 72B7] | Q7400 | TRA_2N7002DM_SOT-363 | m39[74B3] | 74B3] | Q7401 | TRA_2N7002_SOT23-LF | m39[74C3] | Q7402 | TRA_2N7002DM_SOT-363 | m39[74B2] | 74B2] | Q7500 | TRA_HAT2165H_LFPACK | m39[75D3] | Q7501 | TRA_HAT2165H_LFPACK | m39[75D3] | Q7502 | TRA_HAT2165H_LFPACK | m39[75C3] | Q7503 | TRA_HAT2165H_LFPACK | m39[75B3] | Q7504 | TRA_HAT2165H_LFPACK | m39[75D3] | Q7505 | TRA_HAT2165H_LFPACK | m39[75B3] | Q7570 | TRA_HAT2165H_LFPACK | m39[75D2] | Q7572 | TRA_HAT2165H_LFPACK | m39[75C3] | Q7639 | TRA_2N7002_SOT23-LF | m39[76A7] | Q7640 | TRA_SINGLE_MOSFET_PC | m39[76A6] | HN_SOT-23 | Q7641 | TRA_FDC796N_SUPERSOT | m39[76A5] | -6 | Q7642 | TRA_FDC796N_SUPERSOT | m39[76A4] | -6 | Q7701 | TRA_S13446DV_TSOP-LF | m39[77A3] | Q7703 | TRA_2N7002DM_SOT-363 | m39[77D7] | 77C7] | Q7799 | TRA_2N7002_SOT23-LF | m39[77A6] | Q7800 | TRA_NTD60N02R_CASE36 | m39[78C4] | 9-LF | Q7801 | TRA_NTD60N02R_CASE36 | m39[78B4] | 9-LF | Q7802 | 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| | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
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| C | | | | | | | | |
| B | | | | | | | | |
| A | | | | | | | | |



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|--------|--------------------|-----------|
| XW9330 | SHORT_SM | m39[93B7] |
| XW9345 | SHORT_SM | m39[93A7] |
| Y2600 | CRYSTAL_4PIN_SM-LF | m39[26D8] |
| Y3301 | CRYSTAL_5X3.2-SM | m39[33C7] |
| Y4101 | CRYSTAL_4PIN_SM-3 | m39[41B5] |
| Y4400 | CRYSTAL_HC49-USMD | m39[44D2] |
| Y5800 | CRYSTAL_SM-3 | m39[59B8] |
| Y6700 | CRYSTAL_4PIN_SM-LF | m39[59B7] |
| ZH500 | HOLE_VIA | m39[5C1] |
| ZH501 | HOLE_VIA | m39[5C1] |
| ZH502 | HOLE_VIA | m39[5C1] |
| ZH503 | HOLE_VIA | m39[5C1] |
| ZH504 | HOLE_VIA | m39[5B1] |
| ZH505 | HOLE_VIA | m39[5B1] |
| ZH506 | HOLE_VIA | m39[5B1] |
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| ZH509 | HOLE_VIA | m39[5B1] |
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| ZH529 | HOLE_VIA | m39[5B1] |
| ZH601 | MTGHOLE | m39[6A3] |
| ZH602 | MTGHOLE | m39[6A3] |
| ZH603 | MTGHOLE | m39[6A3] |
| ZH606 | MTGHOLE | m39[6A1] |
| ZH607 | MTGHOLE | m39[9D4] |
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