

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

FINO M33

5/19/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
07		381758	ENGINEERING RELEASED	DATE	DATE
				05/19/05	?

D

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B

PDF	CSA	CONTENTS	SYNC MASTER	DATE
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89	154	AUDIO: POWER SUPPLIES	FINO-SO	05/19/2005

A

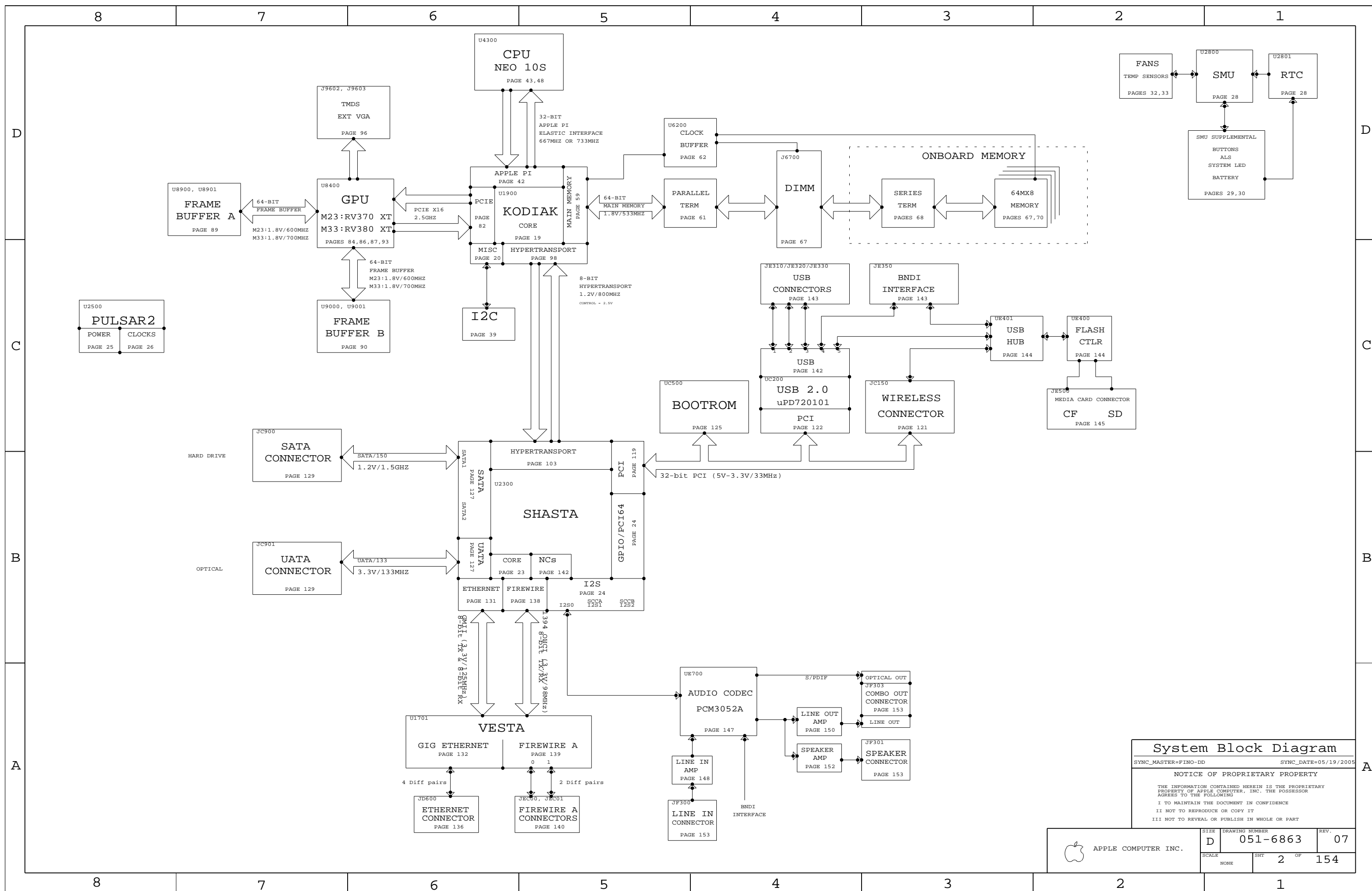
<p style="font-size: small;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <div style="text-align: center;"> <p style="font-size: x-small;">THIRD ANGLE PROJECTION</p> </div>	<p>METRIC</p>	<p>Apple Computer Inc.</p>
<p style="font-size: x-small;">DRAPTER</p> <p style="font-size: x-small;">ENG APPD</p> <p style="font-size: x-small;">QA APPD</p> <p style="font-size: x-small;">RELEASE</p>		<p>DESIGN CK</p> <p>MFG APPD</p> <p>DESIGNER</p> <p>SCALE</p> <p>NONE</p>
<p style="font-size: x-small;">MATERIAL/FINISH NOTED AS APPLICABLE</p> <p style="font-size: x-small;">SIZE D</p>		<p>NOTICE OF PROPRIETARY PROPERTY</p> <p>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</p> <p>II NOT TO REPRODUCE OR COPY IT</p> <p>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="font-size: large; font-weight: bold;">SCH, MLB, FINO, M33</p> <p style="font-size: x-small;">DRAWING NUMBER 051-6863 REV. 07</p> <p style="font-size: x-small; text-align: right;">SHT 1 OF 154</p>

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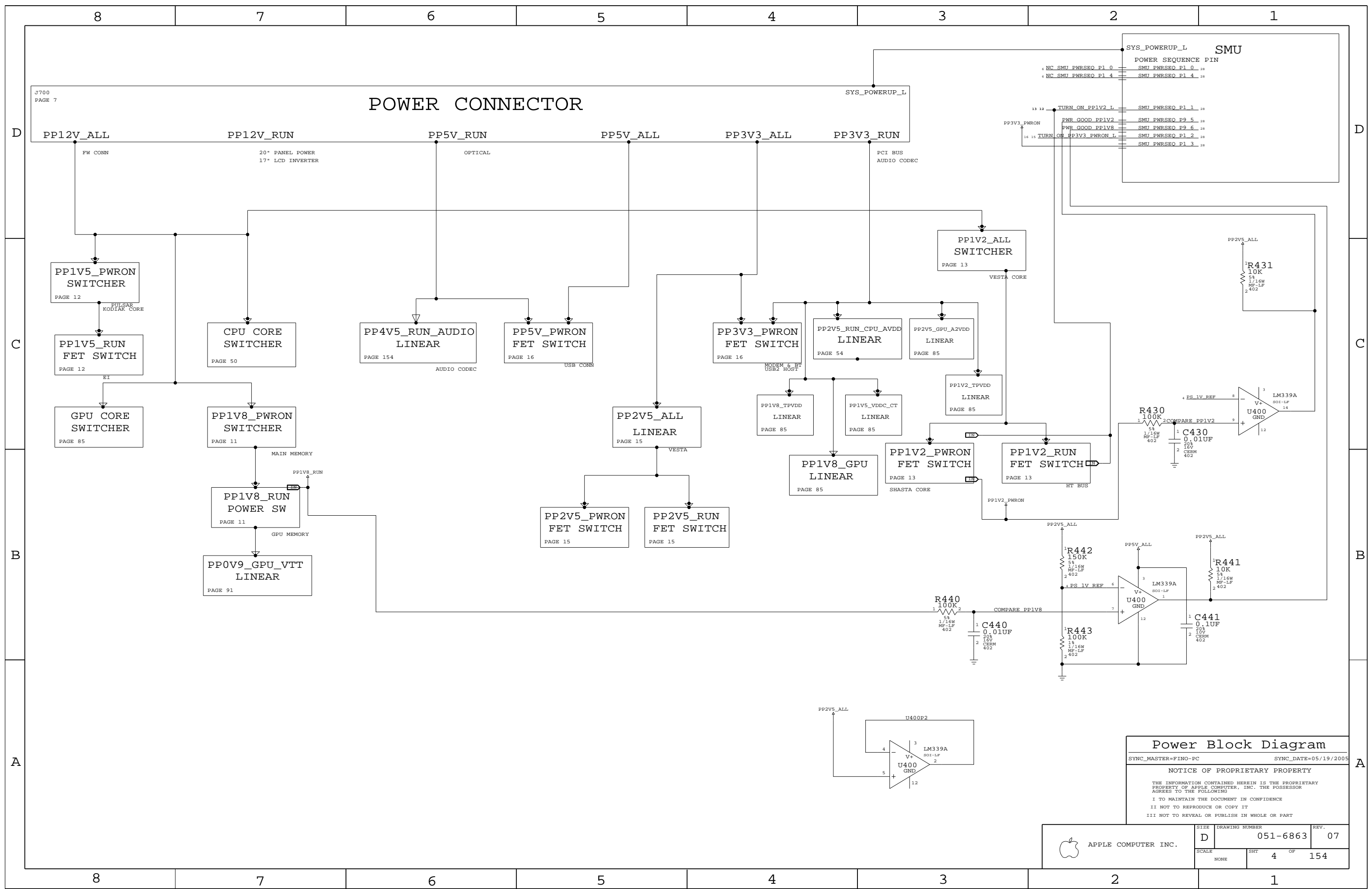
System Block Diagram

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

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NONE			



Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
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NONE	4	154	

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2

1

PROCESSORS

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3158	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.0G,85C,CQA	2.0GHZ	1.15V	46W	50MV	U4300	CPU_2_0GHZ
337S3157	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.2G,85C,FQA	2.2GHZ	1.15V	51W	50MV	U4300	CPU_2_2GHZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
337S3165	337S3158	CPU_2_0GHZ	U4300	IC,DD3.1,2.0G,CJA	1.20V
337S3164	337S3157	CPU_2_2GHZ	U4300	IC,DD3.1,2.0G,FJA	1.20V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0371	1	IC,KODIAK,V1.1,PBGA,200MM	U1900	
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	
343S0324	1	IC,ASIC,VESTA,V1.3	U1701	
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500	

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6790	1	PCB,SCHM,MLB,M23	SCH1	17_INCH_LCD
051-6863	1	PCB,SCHM,MLB,M33	SCH1	20_INCH_LCD
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
825-6447	1	BARCODE LABEL, MLB	LBL1	
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500	
341T1752	1	PURCH ASSY, SMU BIG	U2800	
603-7318	1	M23 CPU HEATSINK	MECH1	17_INCH_LCD
603-7321	1	M33 CPU HEATSINK	MECH1	20_INCH_LCD
603-7322	1	M33 GPU HEATSINK	MECH2	20_INCH_LCD
875-1614	1	CPU GAP FILLER	GAP1	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702	KINGBRIGHT LED
376S0204	376S0130		Q5010,Q5020	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q5011,Q5021	MOSFET,N-CH,VISHAY

Table Items

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

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NONE	5	154

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6

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4

3

2

1

NO TEST XW NETS

Table of test points for NO TEST XW NETS, columns 8 and 7.

Table of test points for NO TEST XW NETS, columns 6 and 5.

Table of test points for NO TEST XW NETS, columns 4 and 3.

EE IDENTIFIED NO TEST NETS

Table of test points for EE IDENTIFIED NO TEST NETS, columns 8 and 7.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 6 and 5.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 4 and 3.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 8 and 7.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 6 and 5.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 4 and 3.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 8 and 7.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 6 and 5.

Table of test points for EE IDENTIFIED NO TEST NETS, columns 4 and 3.

Table of test points for FUNC TEST NETS, columns 4 and 3.

FUNC TEST NETS

NOTES FROM TOM FUSSELMAN
PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

Table of test points for FUNC TEST NETS, columns 2 and 1.

Table of test points for FUNC TEST NETS, columns 2 and 1.

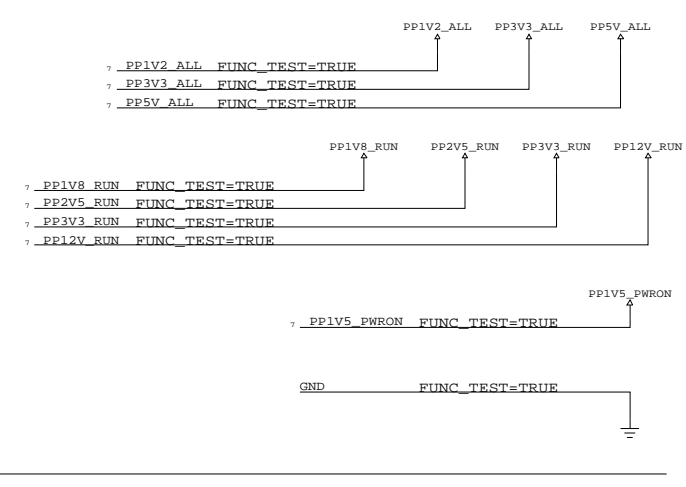


Table of test points for FUNC TEST NETS, columns 2 and 1.

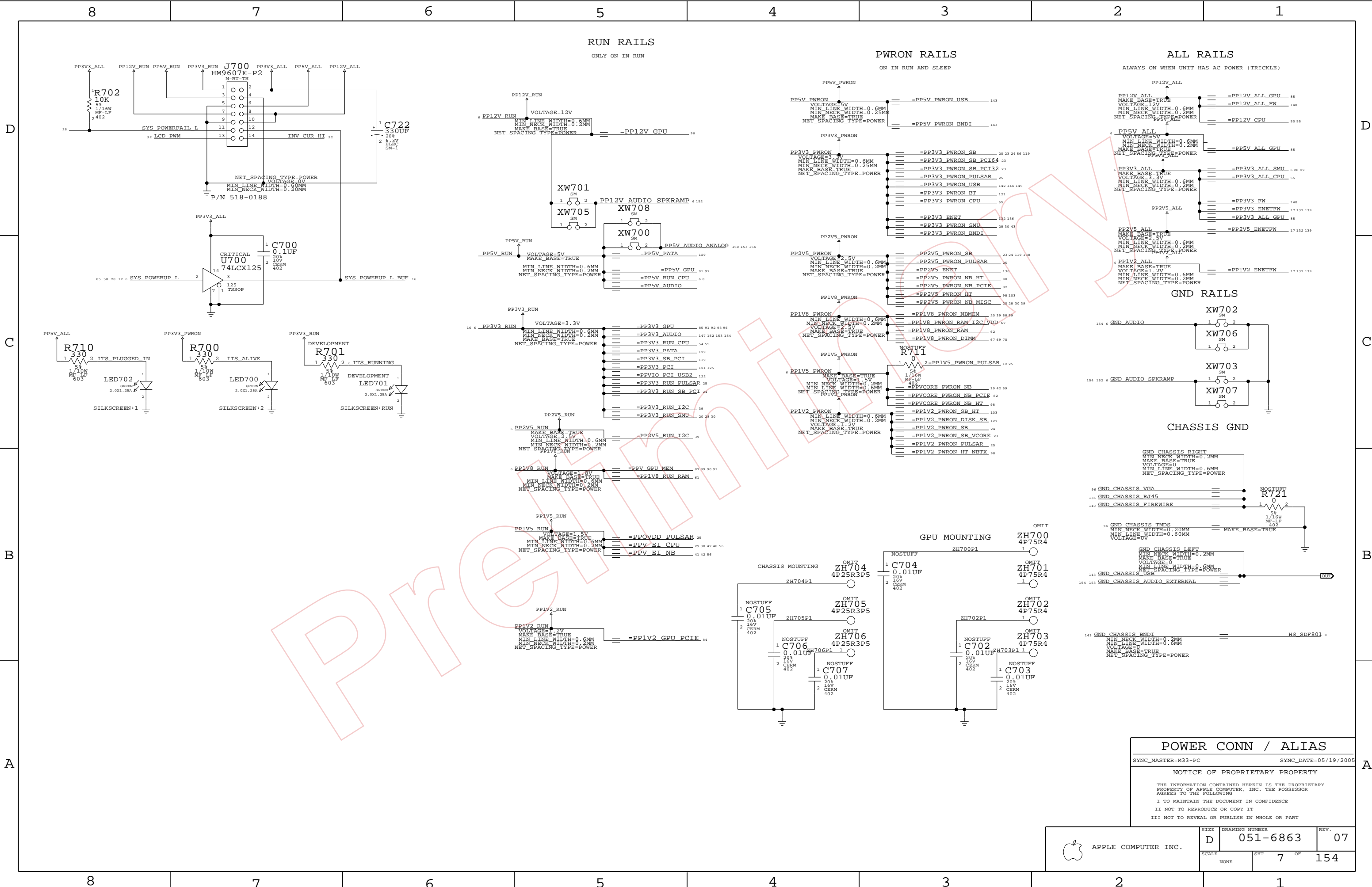
FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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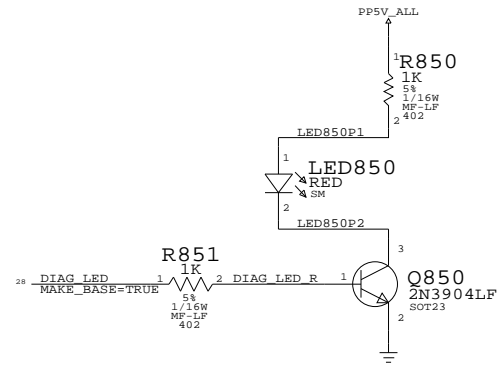
Apple logo, APPLE COMPUTER INC., DRAWING NUMBER 051-6863, REV. 07, SCALE NONE, SHEET 6 OF 154.



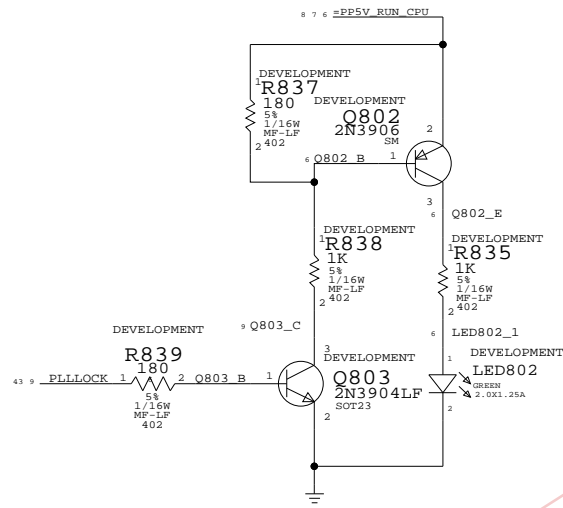
POWER CONN / ALIAS
 SYNC_MASTER=M33-PC SYNC_DATE=05/19/2005
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NONE			

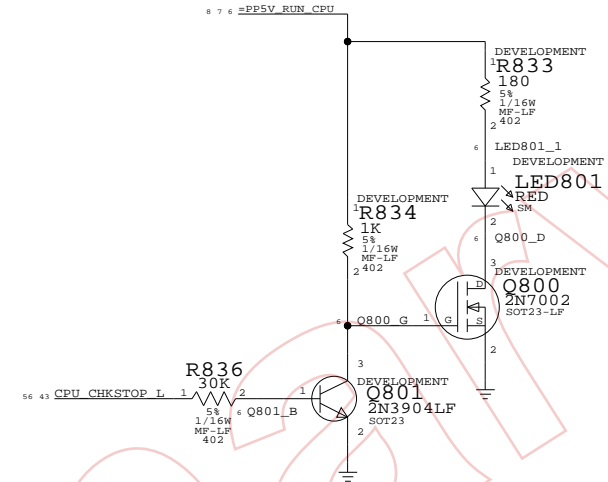
DIAG LED (OVERTEMP LED)



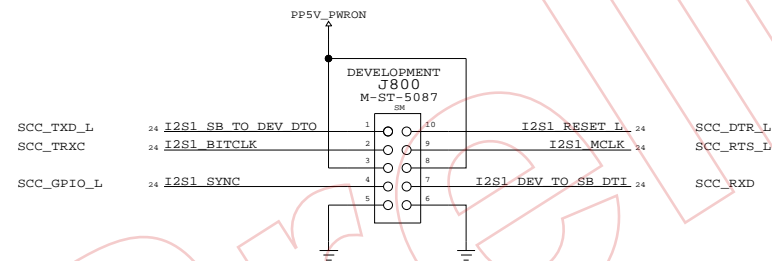
PLL LOCK LED



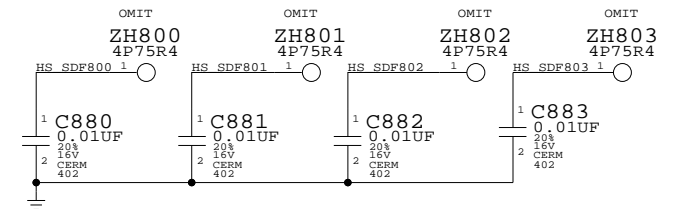
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005

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SCALE	SHT	OF	
NONE	8	154	

8	7	6	5	4	3	2	1				
<p>THE FOLLOWING NETS ARE USED ONLY WHEN THE DEVELOPMENT BOM OPTION IS ENABLED</p> <pre> NO_TEST=YES ENET_TXD_R<7> 130 131 NO_TEST=YES ENET_TXD_R<6> 130 131 NO_TEST=YES ENET_TXD_R<5> 130 131 NO_TEST=YES ENET_TXD_R<4> 130 131 NO_TEST=YES ENET_TXD_R<3> 130 131 NO_TEST=YES ENET_TXD_R<2> 130 131 NO_TEST=YES ENET_TXD_R<1> 130 131 NO_TEST=YES ENET_TXD_R<0> 130 131 NO_TEST=YES ENET_TXD<7> 130 131 132 NO_TEST=YES ENET_TXD<6> 130 131 132 NO_TEST=YES ENET_TXD<5> 130 131 132 NO_TEST=YES ENET_TXD<4> 130 131 132 NO_TEST=YES ENET_TXD<3> 130 131 132 NO_TEST=YES ENET_TXD<2> 130 131 132 NO_TEST=YES ENET_TXD<1> 130 131 132 NO_TEST=YES ENET_TXD<0> 130 131 132 NO_TEST=YES ENET_RXD_R<7> 130 131 132 NO_TEST=YES ENET_RXD_R<6> 130 131 132 NO_TEST=YES ENET_RXD_R<5> 130 131 132 NO_TEST=YES ENET_RXD_R<4> 130 131 132 NO_TEST=YES ENET_RXD_R<3> 130 131 132 NO_TEST=YES ENET_RXD_R<2> 130 131 132 NO_TEST=YES ENET_RXD_R<1> 130 131 132 NO_TEST=YES ENET_RXD_R<0> 130 131 132 NO_TEST=YES ENET_RXD<7> 130 131 132 NO_TEST=YES ENET_RXD<6> 130 131 132 NO_TEST=YES ENET_RXD<5> 130 131 132 NO_TEST=YES ENET_RXD<4> 130 131 132 NO_TEST=YES ENET_RXD<3> 130 131 132 NO_TEST=YES ENET_RXD<2> 130 131 132 NO_TEST=YES ENET_RXD<1> 130 131 132 NO_TEST=YES ENET_RXD<0> 130 131 132 NO_TEST=YES ENET_TX_EN_R 130 131 NO_TEST=YES ENET_TX_ER_R 130 131 NO_TEST=YES ENET_TX_EN 130 131 132 NO_TEST=YES ENET_TX_ER 130 131 132 NO_TEST=YES TP_HT_MB_TO_NB_CLK_N<1> 101 NO_TEST=YES TP_HT_MB_TO_NB_CLK_P<1> 101 NO_TEST=YES NC_CPU_AFN 56 NO_TEST=YES NC_I2C_SMU_CPU_SCL_IN 31 NO_TEST=YES NC_PSRO 56 NO_TEST=YES NC_PSRO_ENABLE 56 NO_TEST=YES NC_SLOT_TOTAL_PWR 31 NO_TEST=YES NC_SMU_CPU_VID_LE0 31 NO_TEST=YES NC_SMU_CPU_VID_LE1 31 NO_TEST=YES NC_SMU_FAN_RPM3 31 NO_TEST=YES NC_SMU_FAN_RPM4 31 NO_TEST=YES NC_SMU_FAN_RPM5 31 NO_TEST=YES NC_SMU_FAN_TACH3 31 NO_TEST=YES NC_SMU_FAN_TACH4 31 NO_TEST=YES NC_SMU_FAN_TACH5 31 NO_TEST=YES NC_SMU_FAN_TACH7 31 NO_TEST=YES NC_SMU_SER_SEL 31 NO_TEST=YES NC_SYS_DOOR_AJAR_L 31 NO_TEST=YES TP_VESTA_2_5V_EN 17 NO_TEST=YES TP_VESTA_AN_EN 132 NO_TEST=YES TP_VESTA_DNC_C9 17 NO_TEST=YES TP_VESTA_DNC_E9 17 NO_TEST=YES TP_VESTA_EN_10B 132 NO_TEST=YES TP_VESTA_ER 132 NO_TEST=YES TP_VESTA_F1000 132 NO_TEST=YES TP_VESTA_FDX 132 NO_TEST=YES TP_VESTA_FDXLED_L 132 NO_TEST=YES TP_VESTA_HUB 132 NO_TEST=YES TP_VESTA_LINK1_L 132 NO_TEST=YES TP_VESTA_LINK2_L 132 NO_TEST=YES TP_VESTA_MANMS 132 NO_TEST=YES TP_VESTA_PHYA<0> 132 NO_TEST=YES TP_VESTA_PHYA<1> 132 NO_TEST=YES TP_VESTA_PHYA<2> 132 NO_TEST=YES TP_VESTA_PHYA<3> 132 NO_TEST=YES TP_VESTA_PHYA<4> 132 NO_TEST=YES TP_VESTA_RBC0 132 NO_TEST=YES TP_VESTA_RBC1 132 NO_TEST=YES TP_VESTA_REGCTL1 17 NO_TEST=YES TP_VESTA_REGCTL2 17 NO_TEST=YES TP_VESTA_REGSEN1 17 NO_TEST=YES TP_VESTA_REGSEN2 17 NO_TEST=YES TP_VESTA_REGSUP1 17 NO_TEST=YES TP_VESTA_REGSUP2 17 NO_TEST=YES TP_VESTA_RGMIIEN 132 NO_TEST=YES TP_VESTA_SPD0 132 NO_TEST=YES TP_VESTA_TDBL<0> 139 NO_TEST=YES TP_VESTA_TDBL<1> 139 NO_TEST=YES TP_VESTA_TDBL<2> 139 NO_TEST=YES TP_VESTA_TEST<0> 132 NO_TEST=YES TP_VESTA_TEST<1> 132 NO_TEST=YES TP_VESTA_TEST_1394<0> 139 NO_TEST=YES TP_VESTA_TEST_1394<1> 139 NO_TEST=YES TP_VESTA_TVCO 132 NO_TEST=YES CARD_READER_ACTIVITY_R 144 NO_TEST=YES TP_VESTA_FAVDDL 139 NO_TEST=YES TP_NB_A_TRIGGER_OUT 56 NO_TEST=YES TP_NB_B_TRIGGER_OUT 56 </pre>				<p>THE FOLLOWING NETS DO NOT HAVE TEST POINT BECAUSE OF ROUTING DENSITY AND SIGNAL INTEGRITY. TEST COVERAGE WILL BE BY FCT NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS</p> <pre> NO_TEST=YES Q803_C 8 NO_TEST=YES FLLLOCK 8 43 NO_TEST=YES LED_PPIV8_RUN_P 11 NO_TEST=YES LED_PPIV8_RUN_N 11 NO_TEST=YES PPIV5_RUN_FOR_LED 12 NO_TEST=YES LED_PPIV5_RUN_N 12 NO_TEST=YES LED_PPIV5_RUN_P 12 NO_TEST=YES PULSAR_1V5_RUN_SWITCH 12 NO_TEST=YES PPIV2_RUN_FOR_LED 13 NO_TEST=YES LED_PPIV2_RUN_N 13 NO_TEST=YES LED_PPIV2_RUN_P 13 NO_TEST=YES KP_V<1> 65 NO_TEST=YES KP_V<2> 65 NO_TEST=YES CPU_SENSE_KP_V 65 NO_TEST=YES NB_PLL_OUT_TRG_R 59 NO_TEST=YES NB_PLL_OUT_TRG 59 NO_TEST=YES PP5V_T555 92 NO_TEST=YES T555_DISC 92 NO_TEST=YES T555_THRES 92 NO_TEST=YES T555_OUT 92 NO_TEST=YES T555_PWM 92 NO_TEST=YES PP3V3_GPU_TSENSE 93 NO_TEST=YES TSENSE_GPU_OVERTEMP_L 93 NO_TEST=YES TSENSE_GPU_ADD0 93 NO_TEST=YES TSENSE_GPU_ADD1 93 NO_TEST=YES GPU_DIODE_PLUS 93 NO_TEST=YES GPU_DIODE_MINUS 93 NO_TEST=YES LED8700_P 136 NO_TEST=YES LED8701_P 136 NO_TEST=YES CPU_A_TBN_CLK_R 26 NO_TEST=YES CPU_B_TBN_CLK_R 26 NO_TEST=YES CPU_A_APSYNC_R 26 NO_TEST=YES CPU_B_APSYNC_R 26 NO_TEST=YES NB_APSYNC_R 26 NO_TEST=YES HT_SB_REFCLK_R 26 NO_TEST=YES HT_NB_REFCLK_H0_R 26 NO_TEST=YES HT_NB_REFCLK_L0_R 26 NO_TEST=YES CLK_RAIREF_200M_P_R 26 NO_TEST=YES CLK_RAIREF_200M_N_R 26 NO_TEST=YES NB_PMR_CLK_P_R 26 NO_TEST=YES NB_PMR_CLK_N_R 26 NO_TEST=YES NB_PCIE_REFCLK_P_C 26 NO_TEST=YES NB_PCIE_REFCLK_N_C 26 NO_TEST=YES GFX_SLOT_PCIE_REFCLK_P_C 26 NO_TEST=YES GFX_SLOT_PCIE_REFCLK_N_C 26 NO_TEST=YES PCIE_A_REFCLKIN_P_C 26 NO_TEST=YES PCIE_A_REFCLKIN_N_C 26 NO_TEST=YES PCIE_B_REFCLKIN_P_C 26 NO_TEST=YES PCIE_B_REFCLKIN_N_C 26 NO_TEST=YES PCIE_C_REFCLKIN_P_C 26 NO_TEST=YES PCIE_C_REFCLKIN_N_C 26 NO_TEST=YES NB_DDR_REFCLK_P_R 26 NO_TEST=YES NB_DDR_REFCLK_N_R 26 NO_TEST=YES CLK_RAI_GIGE_25MHZ_R 26 NO_TEST=YES QUA0_REF_25MHZ_R 26 NO_TEST=YES SB_CLK25M_SATA_R 26 NO_TEST=YES QUA1_REF_25MHZ_R 26 NO_TEST=YES PCI_CLK33M_SB_EXT_R 26 NO_TEST=YES SB_AIRPRT_CLK_33MHZ_R 26 NO_TEST=YES CLK_RAI_REFCLK_66M_R 26 NO_TEST=YES SB_USB2_CLK_33MHZ_R 26 NO_TEST=YES 100M_N<0> 82 97 NO_TEST=YES 100M_P<0> 82 97 NO_TEST=YES CKA_N<0> 84 97 NO_TEST=YES CKA_P<0> 84 97 NO_TEST=YES HT_NB_N<0> 98 101 NO_TEST=YES HT_NB_P<0> 98 101 NO_TEST=YES HT_NB_REFCLK_NF<0> 98 101 NO_TEST=YES HT_NB_REFCLK_PF<0> 98 101 NO_TEST=YES HT_NB_TO_SB_CAD_N<0..7> 101 NO_TEST=YES HT_NB_TO_SB_CAD_P<0..7> 101 NO_TEST=YES HT_NB_TO_SB_CLK_P<0> 101 NO_TEST=YES HT_NB_TO_SB_CLK_N<0> 101 NO_TEST=YES HT_SB_TO_NB_CAD_N<0..7> 101 NO_TEST=YES HT_SB_TO_NB_CAD_P<0..7> 101 NO_TEST=YES HT_SB_TO_NB_CLK_P<0> 101 NO_TEST=YES HT_SB_TO_NB_CLK_N<0> 101 NO_TEST=YES PCIE_SLOT_A_TO_NB_N<0..15> 82 84 97 NO_TEST=YES PCIE_SLOT_A_TO_NB_P<0..15> 82 84 97 NO_TEST=YES UATA_DA<0> 127 129 NO_TEST=YES UATA_DD<1> 127 129 NO_TEST=YES UATA_DD<14> 127 129 NO_TEST=YES PCIE_NB_TO_SLOT_A_N<0> 82 84 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_N<3> 82 84 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_NF<13> 82 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_NF<7> 82 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_P<1> 82 84 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_P<13> 82 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_PF<14> 82 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_NF<12> 82 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_PF<10> 82 97 NO_TEST=YES PCIE_NB_TO_SLOT_A_PF<4> 82 97 NO_TEST=YES HT_MB_TO_NB_CTL_N<1> 98 NO_TEST=YES HT_MB_TO_NB_CTL_P<1> 98 NO_TEST=YES HT_NB_TO_MB_CTL_P<1> 98 NO_TEST=YES HT_NB_TO_MB_CTL_N<0> 101 NO_TEST=YES HT_SB_TO_NB_CTL_P<0> 101 NO_TEST=YES CLK_KOD_100M_NF<0> 82 97 NO_TEST=YES CLK_KOD_100M_PF<0> 82 97 NO_TEST=YES EI_CPU_TO_NB_CLK_N 43 56 NO_TEST=YES EI_CPU_TO_NB_SR_N<1> 43 56 NO_TEST=YES EI_CPU_TO_NB_SR_P<1> 43 56 NO_TEST=YES EI_NB_TO_CPU_CLK_N 43 56 NO_TEST=YES EI_NB_TO_CPU_CLK_P 43 56 NO_TEST=YES EI_NB_TO_CPU_SR_N<0> 43 56 NO_TEST=YES EI_NB_TO_CPU_SR_P<0> 43 56 </pre>				<p>JTAG TEST POINTS NEED TO BE ON THE BOTTOM OF THE BOARD ADDING FUNC_TEST=TRUE TO THESE NETS</p> <pre> FUNC_TEST=TRUE TP_JTAG_SB_TCK 20 FUNC_TEST=TRUE TP_JTAG_SB_TDI 20 FUNC_TEST=TRUE TP_JTAG_SB_TDO 20 FUNC_TEST=TRUE TP_JTAG_SB_TMS 20 FUNC_TEST=TRUE JTAG_SB_TRST_L 20 24 FUNC_TEST=TRUE JTAG_NB_TCK 20 30 FUNC_TEST=TRUE JTAG_NB_TDI 20 30 FUNC_TEST=TRUE JTAG_NB_TDO 20 30 FUNC_TEST=TRUE JTAG_NB_TMS 20 30 FUNC_TEST=TRUE JTAG_NB_TRST_L 20 30 FUNC_TEST=TRUE TP_JTAG_VESTA_TDI 30 43 FUNC_TEST=TRUE TP_JTAG_VESTA_TDO 30 43 FUNC_TEST=TRUE TP_JTAG_VESTA_TCK 30 43 FUNC_TEST=TRUE TP_JTAG_VESTA_TMS 30 43 FUNC_TEST=TRUE TP_JTAG_VESTA_TRST_L 30 43 FUNC_TEST=TRUE JTAG_CPU_TCK 30 43 FUNC_TEST=TRUE JTAG_CPU_TDI 30 43 FUNC_TEST=TRUE JTAG_CPU_TDO 30 43 47 FUNC_TEST=TRUE JTAG_CPU_TMS 30 43 47 FUNC_TEST=TRUE JTAG_CPU_TRST_L 43 47 </pre>			
8	7	6	5	4	3	2	1				

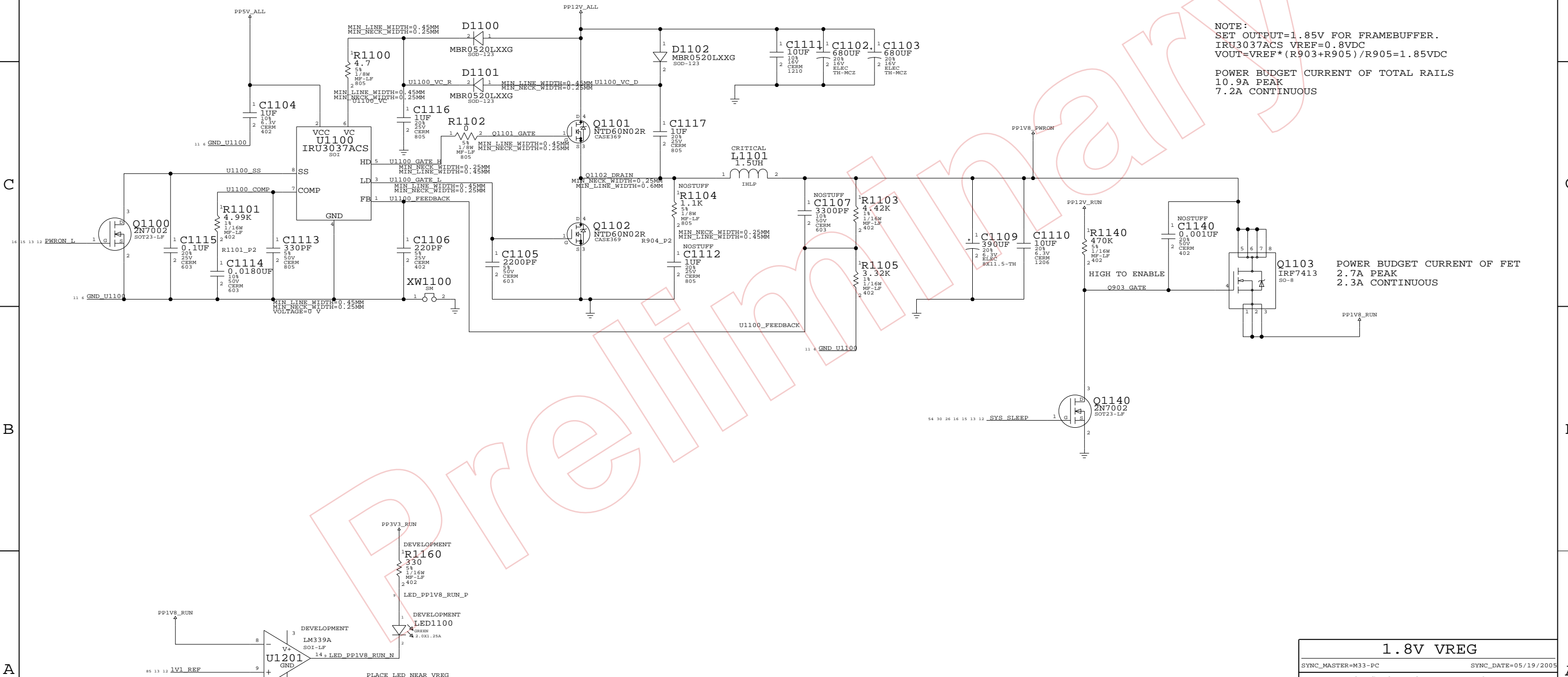
PROPRIETARY

FUNC TEST 2 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. 07
	SCALE NONE	SHEET 9	OF 154

1.8V VOLTAGE REGULATOR



NOTE:
 SET OUTPUT=1.85V FOR FRAMEBUFFER.
 IRU3037ACS VREF=0.8VDC
 $V_{OUT} = V_{REF} * (R_{903} + R_{905}) / R_{905} = 1.85VDC$
 POWER BUDGET CURRENT OF TOTAL RAILS
 10.9A PEAK
 7.2A CONTINUOUS

POWER BUDGET CURRENT OF FET
 2.7A PEAK
 2.3A CONTINUOUS

1.8V VREG		
SYNC_MASTER=M33-PC	SYNC_DATE=05/19/2005	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT	11 OF	154
NONE			

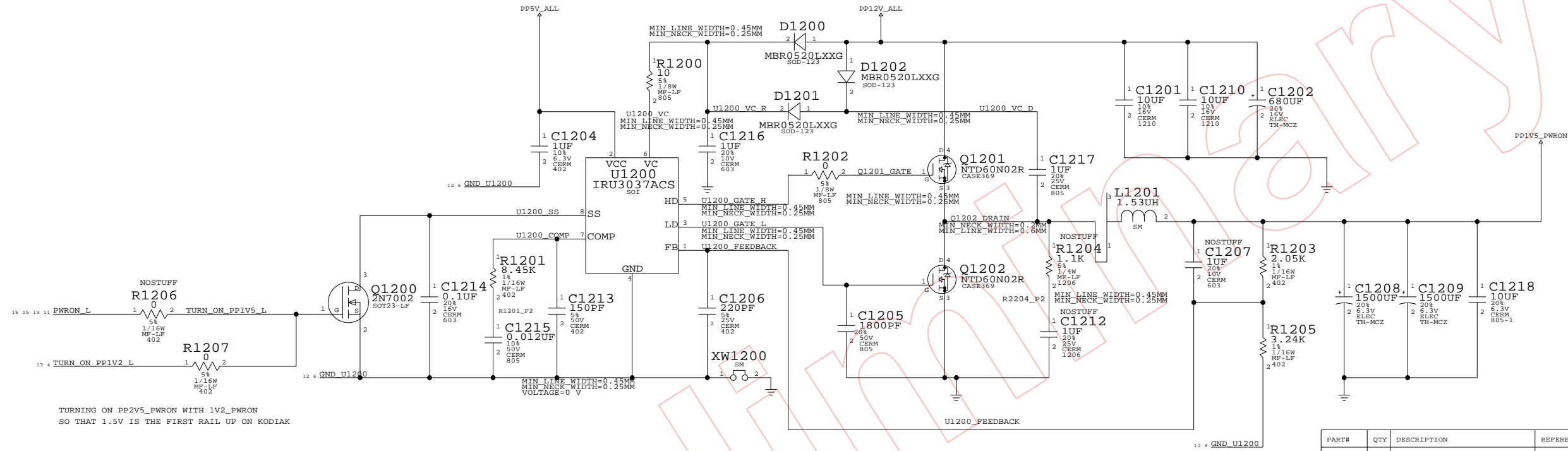
KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
 $V_{OUT}=V_{REF} \cdot (R_{1203}+R_{1205})/R_{1205}=1.30VDC$

LOAD FROM POWER BUDGET
 8.5A PEAK CURRENT DRAW
 7.2A CONTINUOUS CURRENT DRAW

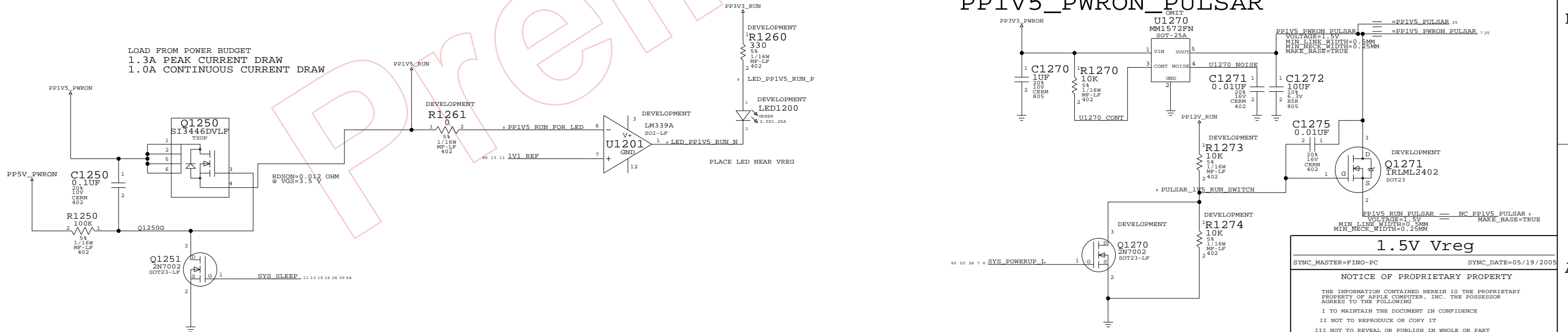
1.35V R1205=2.87K
 1.30V R1205=3.24K
 1.25V R1205=4.02K



TURNING ON PP2V5_PWRON WITH V2_PWRON
 SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
3538L145	1	MM1571FN	U1270	CRITICAL	

PP1V5_PWRON_PULSAR



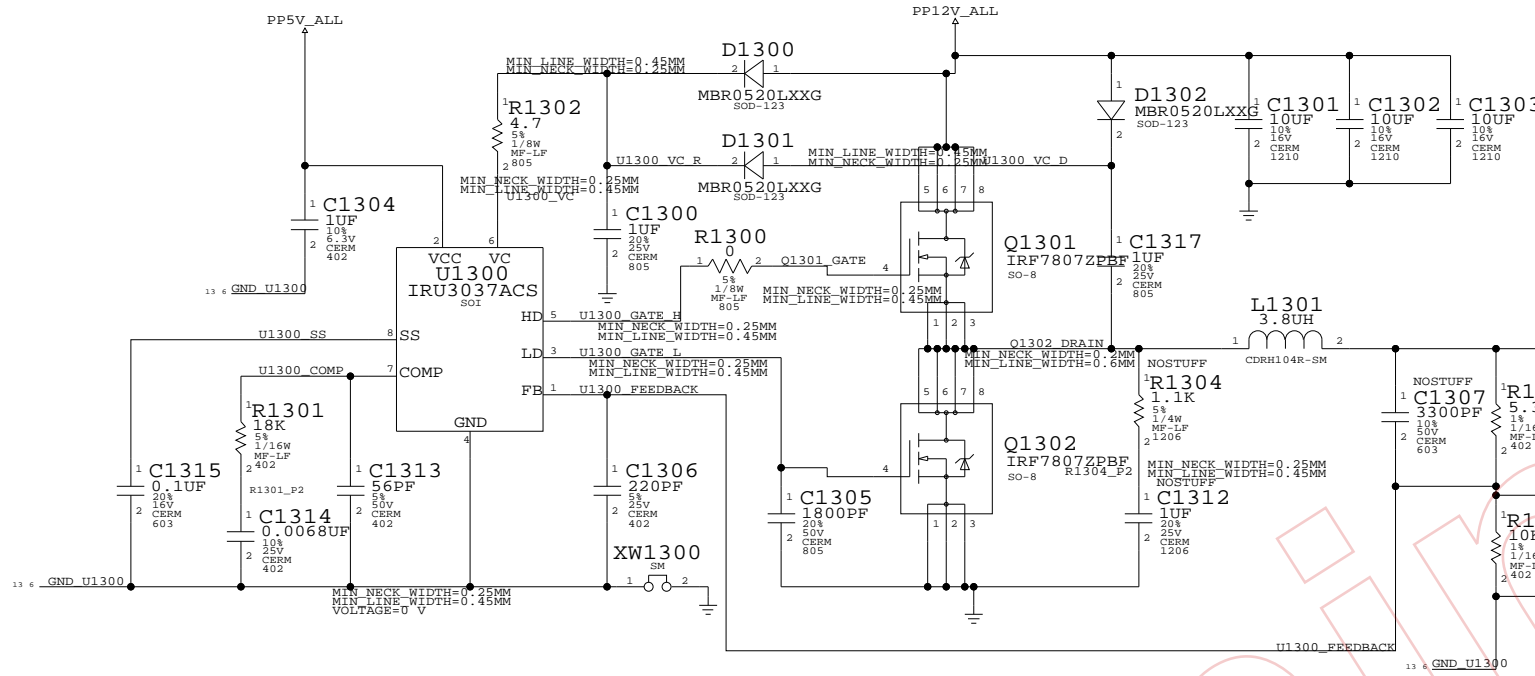
LOAD FROM POWER BUDGET
 1.3A PEAK CURRENT DRAW
 1.0A CONTINUOUS CURRENT DRAW

1.5V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

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	D	051-6863	07
SCALE	SHT	12 OF	154
NONE			

PP1V2_ALL VOLTAGE REGULATOR

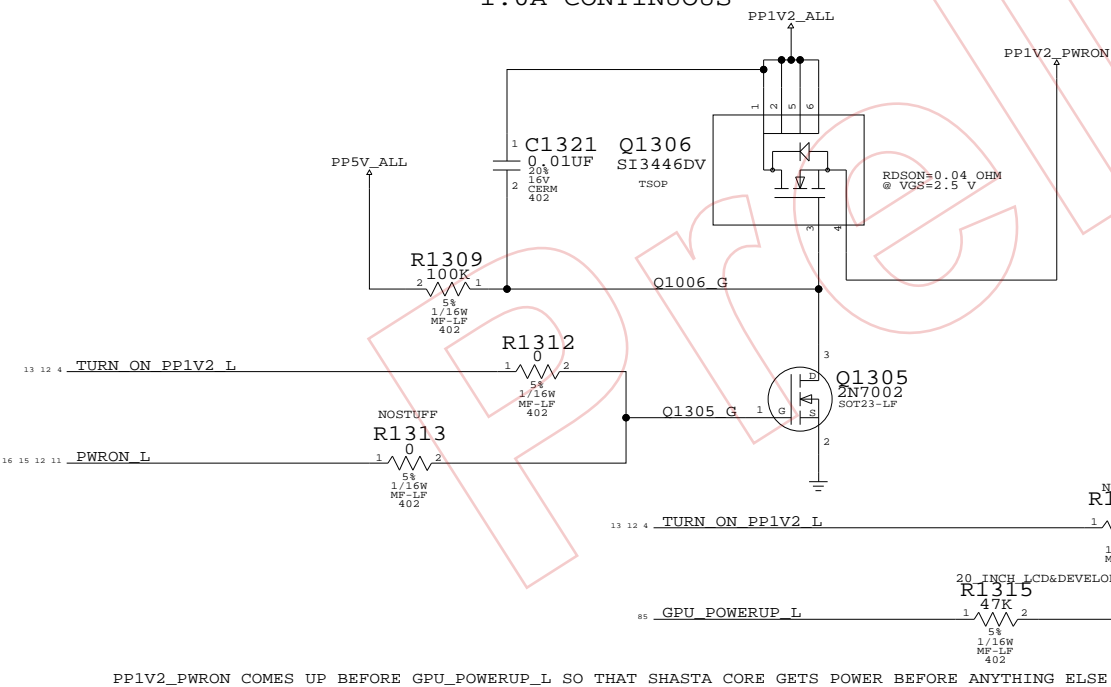


NOTE:
 SET OUTPUT=1.22-1.23V
 IRU3037ACS VREF=0.8VDC
 $V_{OUT}=V_{REF} * (R1003+R1005)/R1005=1.22-1.23VDC$

POWER BUDGET CURRENT OF TOTAL RAILS
 3.2A PEAK
 2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

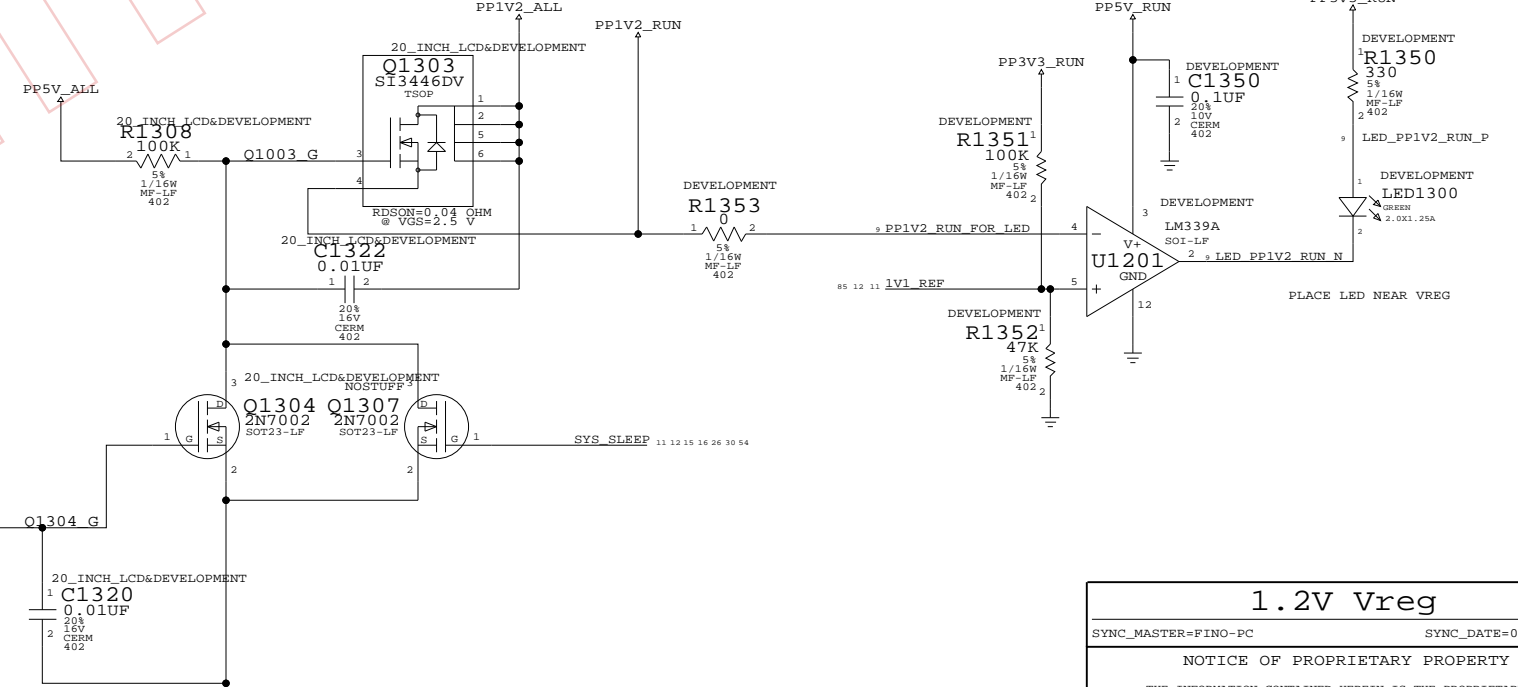
PEAK CURRENT 1.3A
 1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg
 SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

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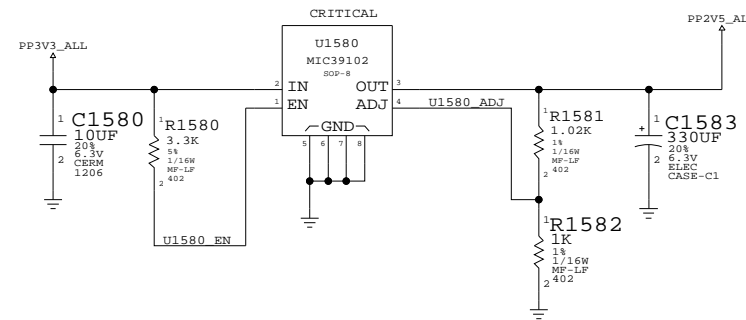
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SCALE	SHT	13 OF 154	
NONE			

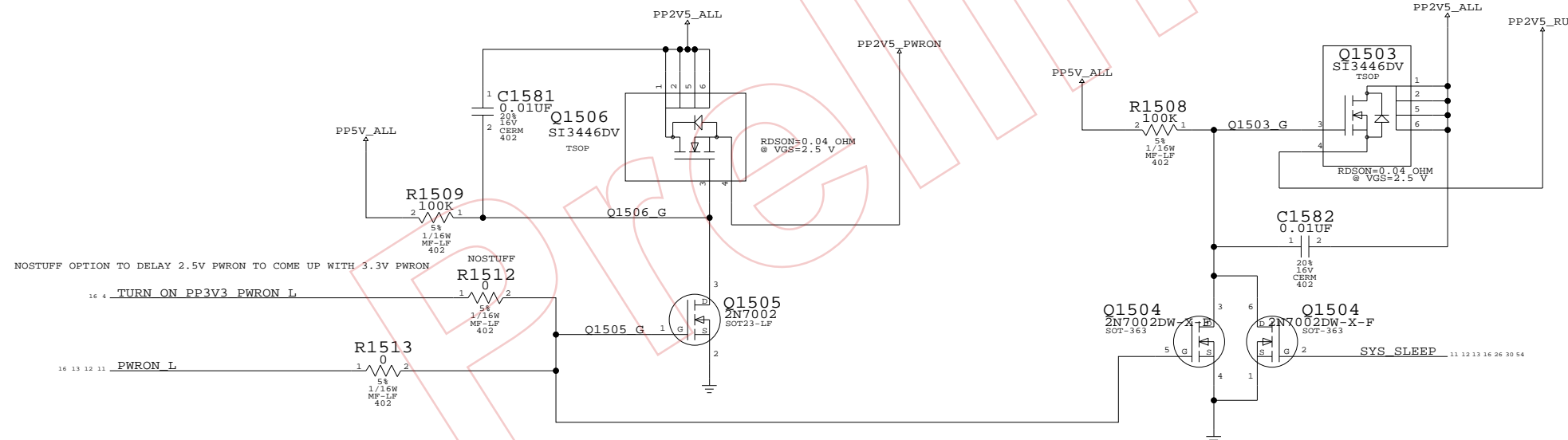
PP2V5_ALL VOLTAGE REGULATOR

NOTE:
 SET OUTPUT=2.5V
 IRU3037CS VREF=1.24VDC
 $V_{OUT} = V_{REF} * (R_{1581} + R_{1582}) + 1 = 5.505VDC$
 POWER BUDGET CURRENT OF TOTAL RAILS
 0.2A PEAK
 0.1A CONTINUOUS



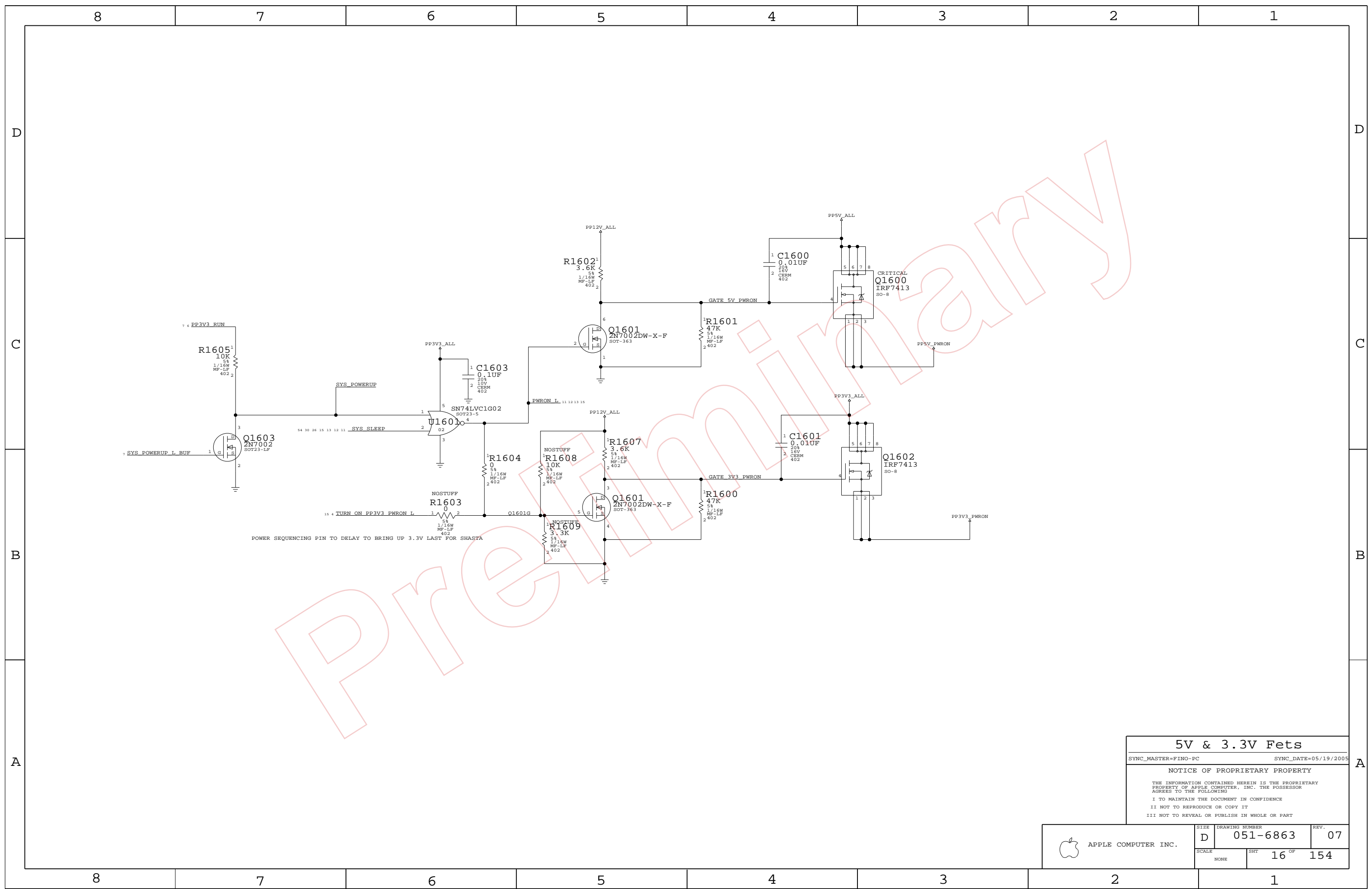
PP2V5_PWRON FET SWITCH PEAK CURRENT 0.1A

PP2V5_RUN FET SWITCH PEAK CURRENT 0.1A



2.5V Vreg
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	D	051-6863	07
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NONE			




5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

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SCALE	SHT	16 OF 154	
NONE			

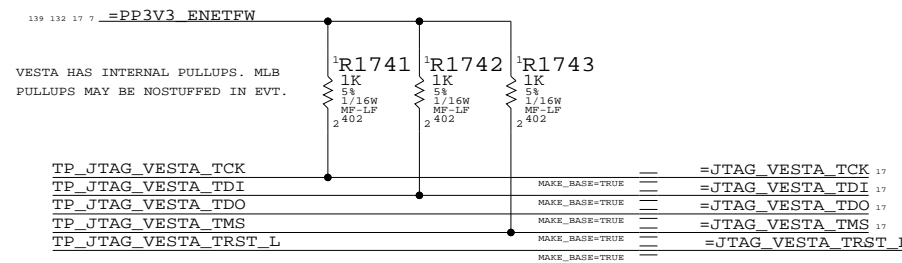
Page Notes

Power aliases required by this page:

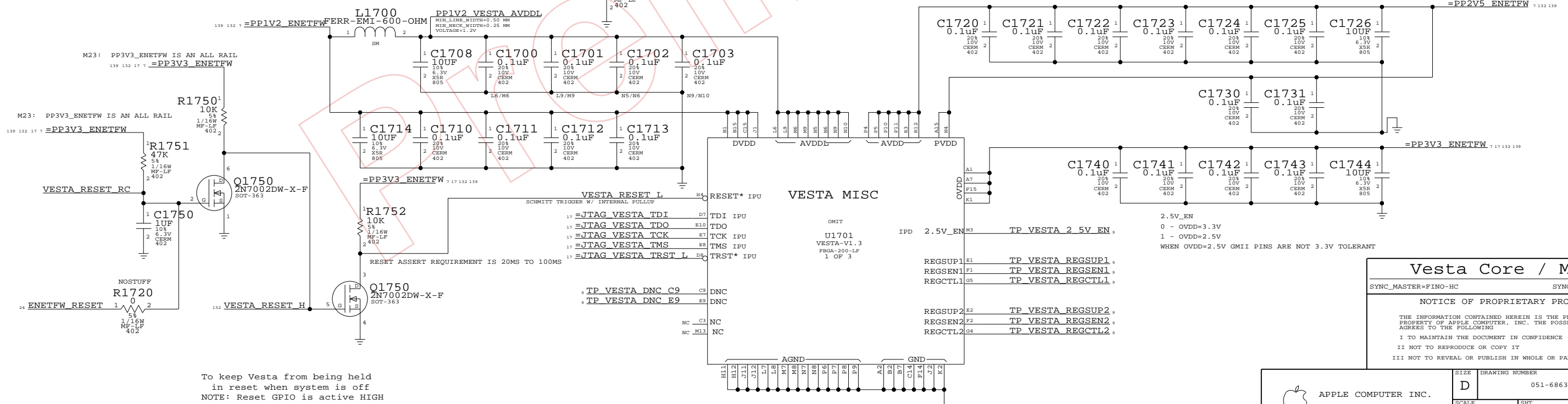
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG



M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS



To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

Vesta Core / Misc		
SYNC_MASTER=FINO-HC	SYNC_DATE=05/19/2005	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT	OF	
NONE	17	154	

D

D

C

C

B

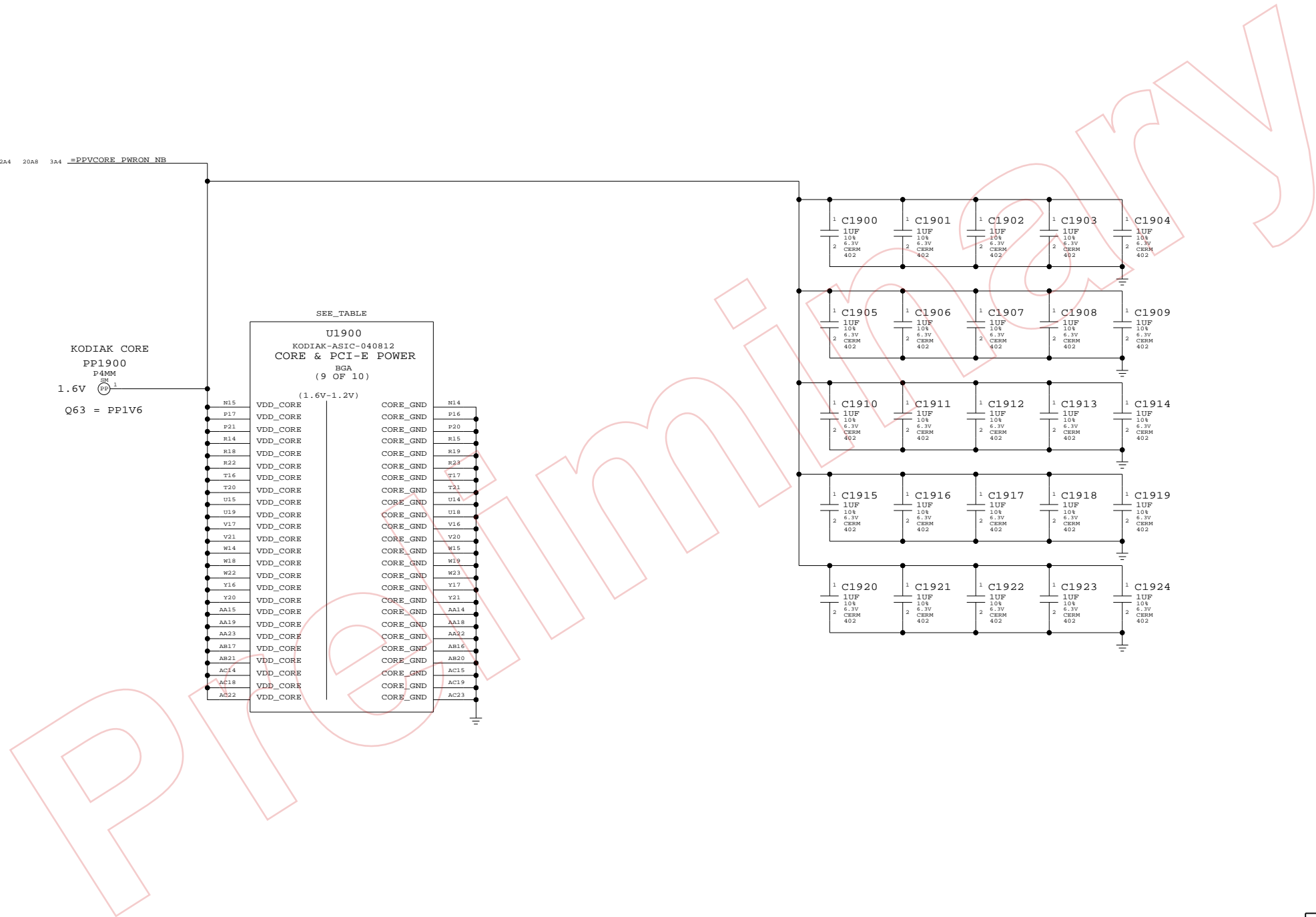
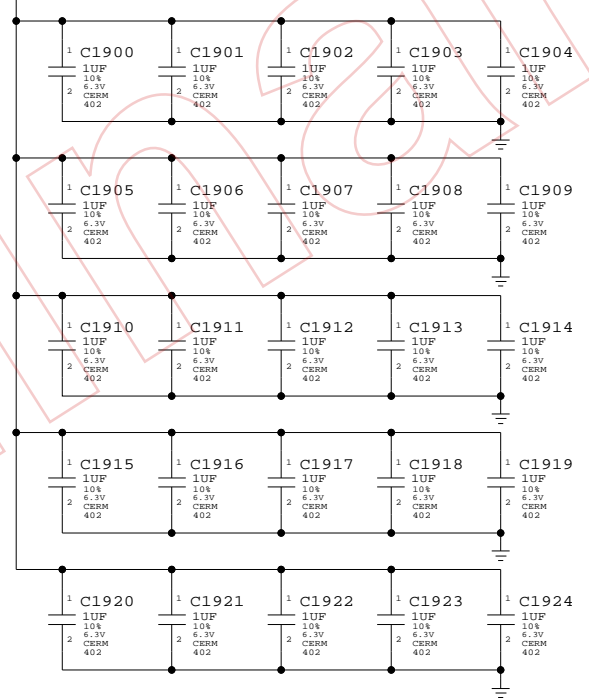
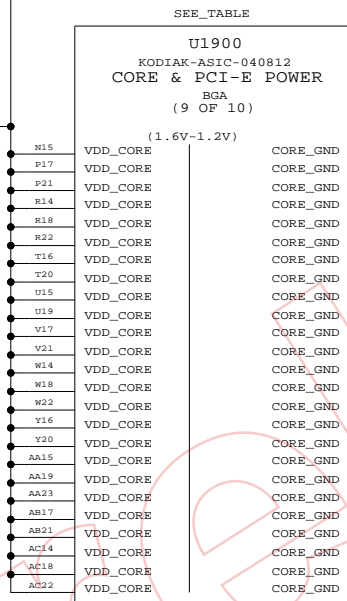
B

A

A

59A6 42A4 20A8 3A4 =PPVCORE_PWRON_NB

KODIAK CORE
PP1900
P4MM
3K
1.6V
Q63 = PP1V6



DRAWING

KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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LAST MODIFIED=Thu May 19 14:26:38 2005
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PAGE 19

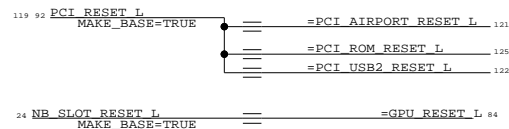
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE		SHT	OF
NONE		19	154

D
C
B
A

D
C
B
A

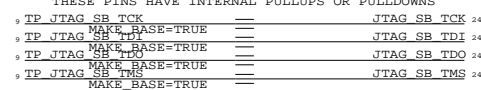
SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

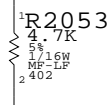
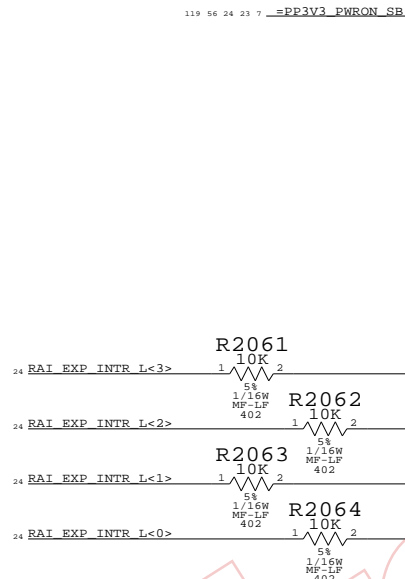


SHASTA JTAG

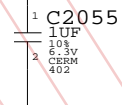
THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS



SHASTA GPIO TERMINATIONS
(SOME OF THESE ARE NOSTUFF
ON PAGE 24)

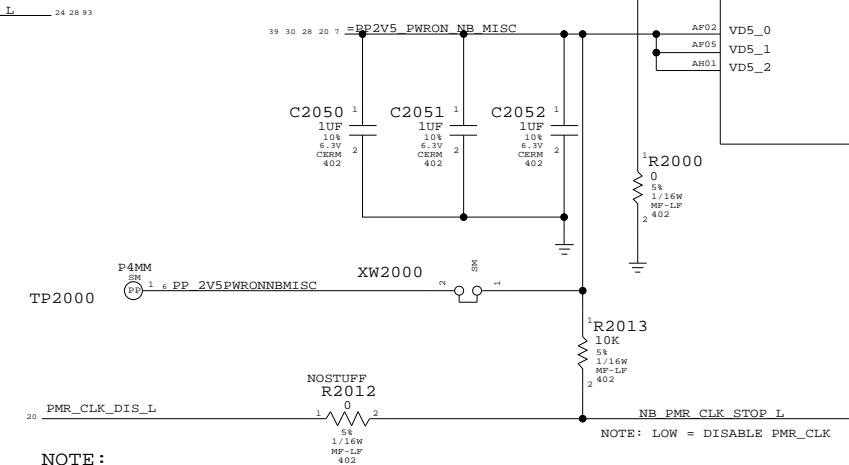
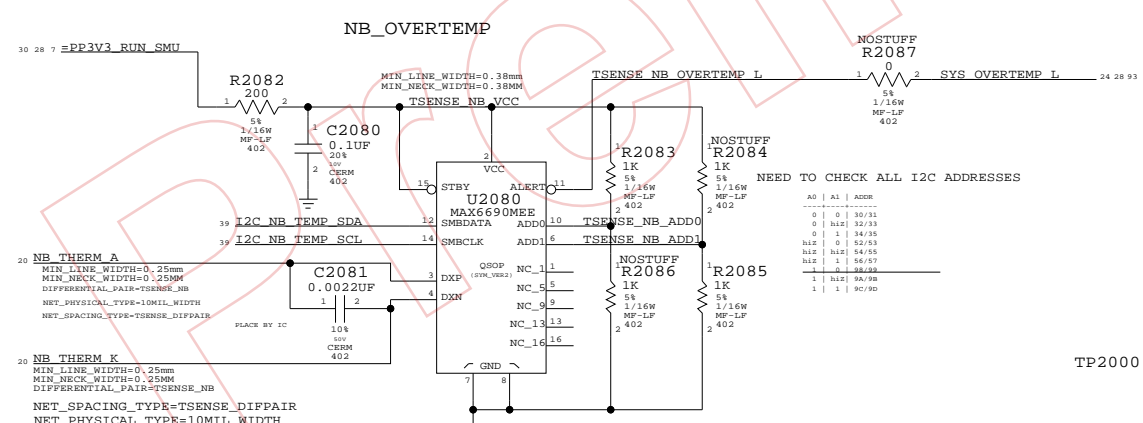
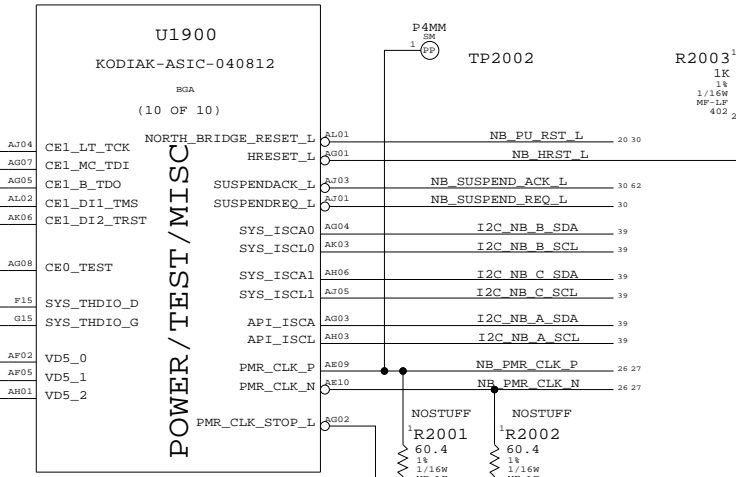
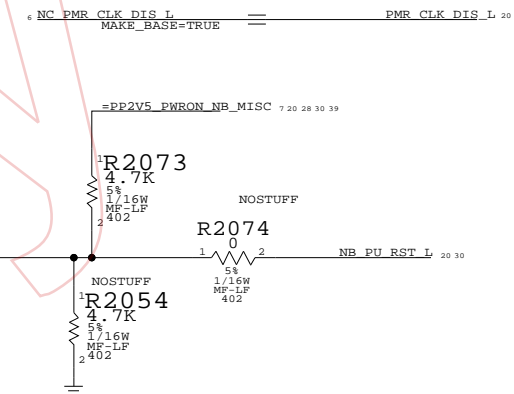


C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP



KODIAK ALIASES

KODIAK JTAG_TRST PULLED HIGH
TO ALLOW SMU DEBUG ACCESS



NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

KODIAK & SHASTA MISC
SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005
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	D	051-6863	07
SCALE	SHEET OF		
NONE	20		154

Page Notes

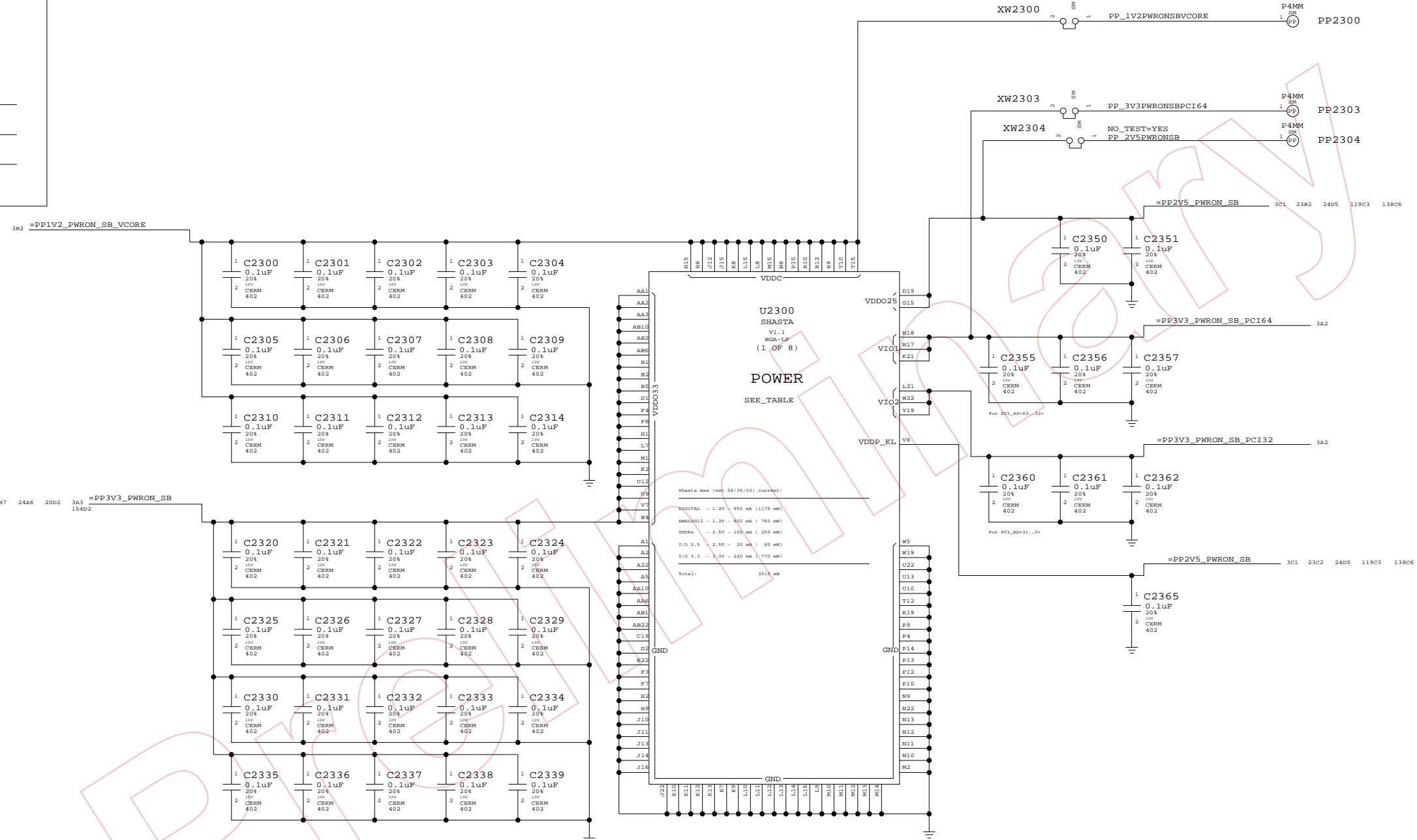
Power aliases required by this page:
 - =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
 - =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
 - =PP3V3_PWRON_SB
 - =PP2V5_PWRON_SB
 - =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Power Sequencing:
 Must power Shasta VCore rail before any other Shasta supplies.



Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

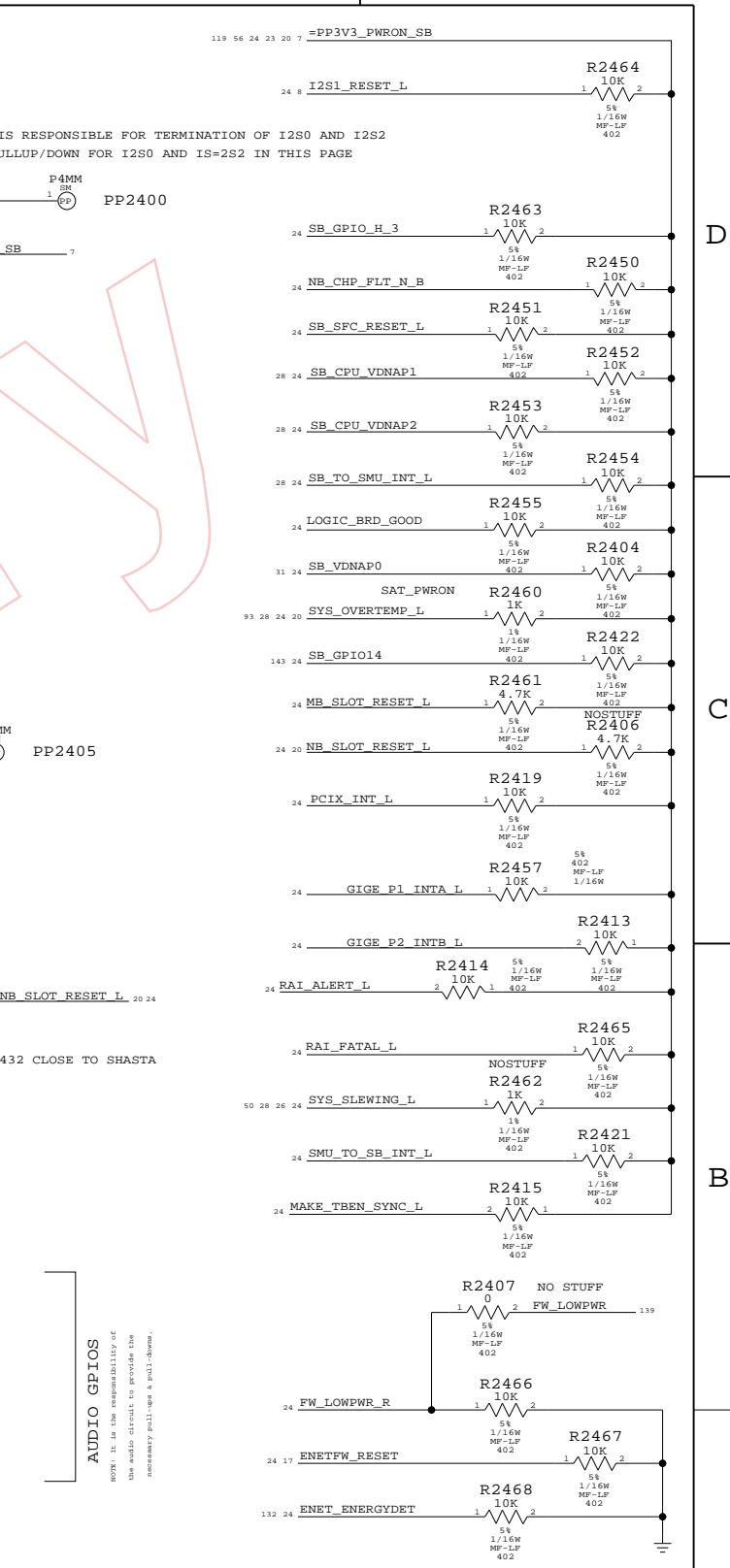
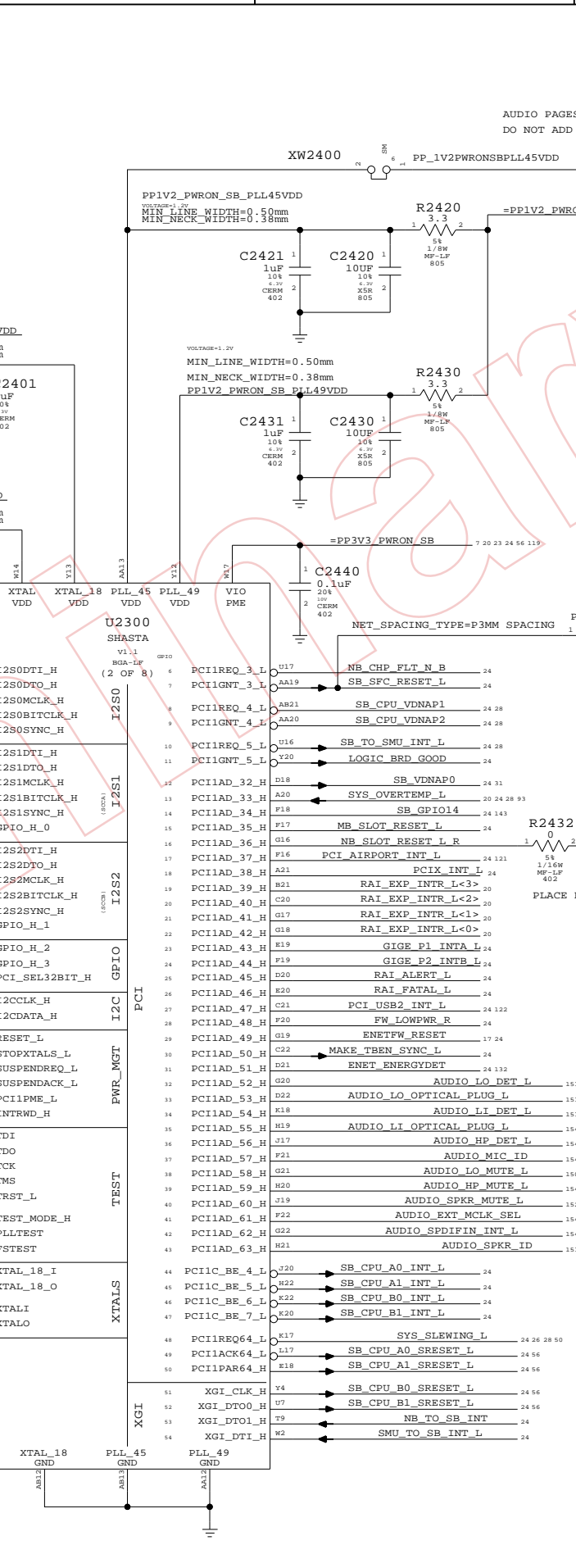
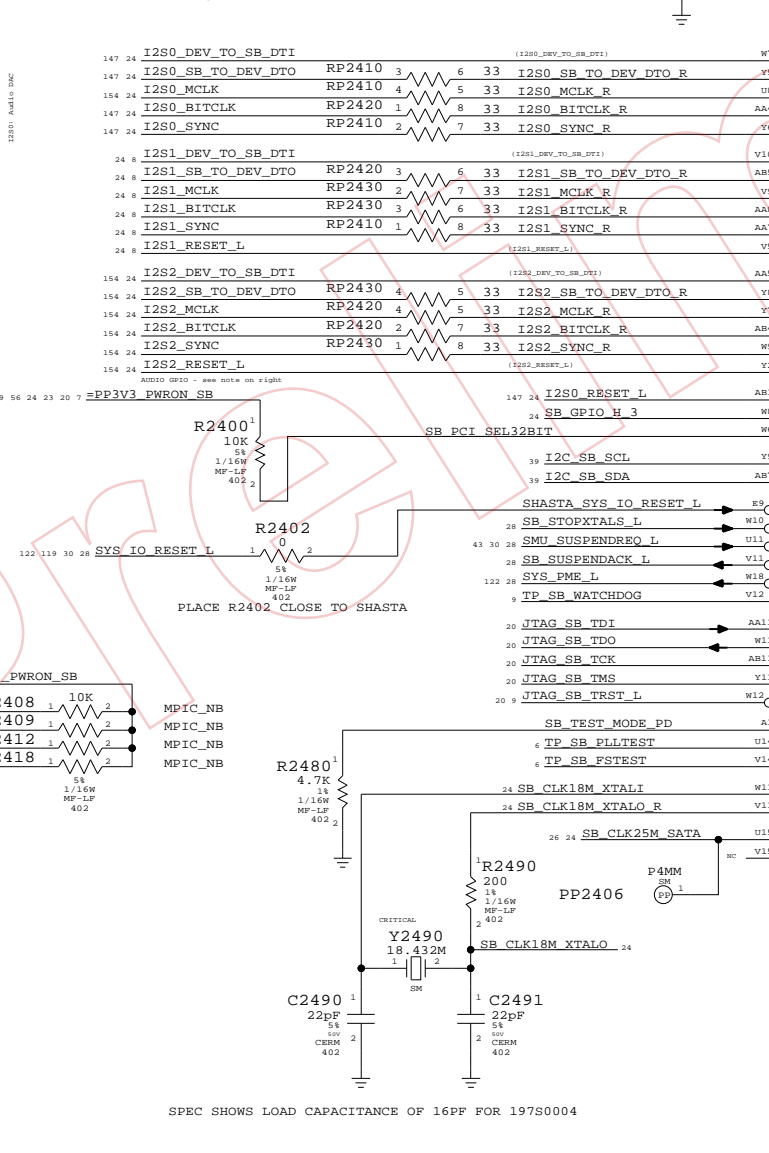
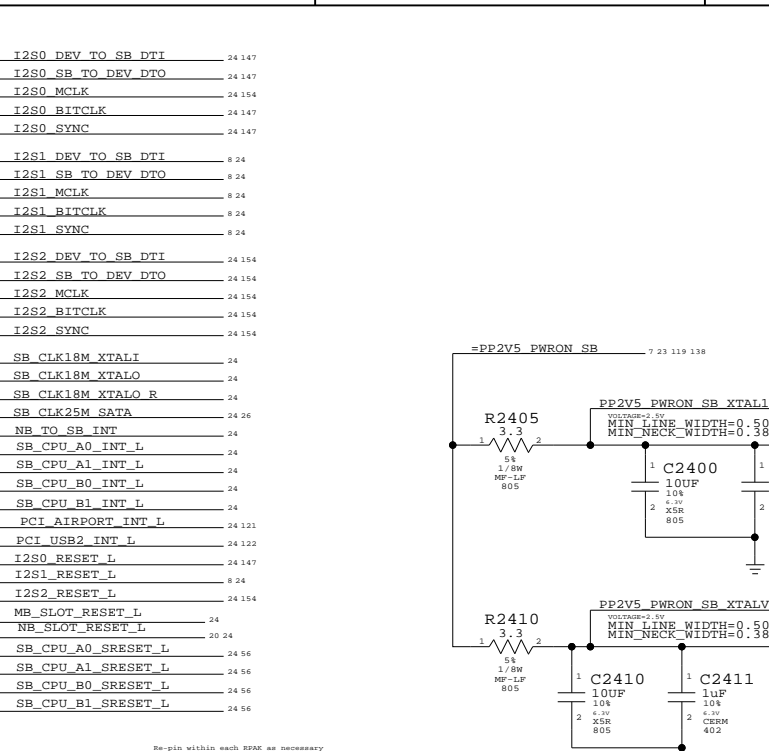
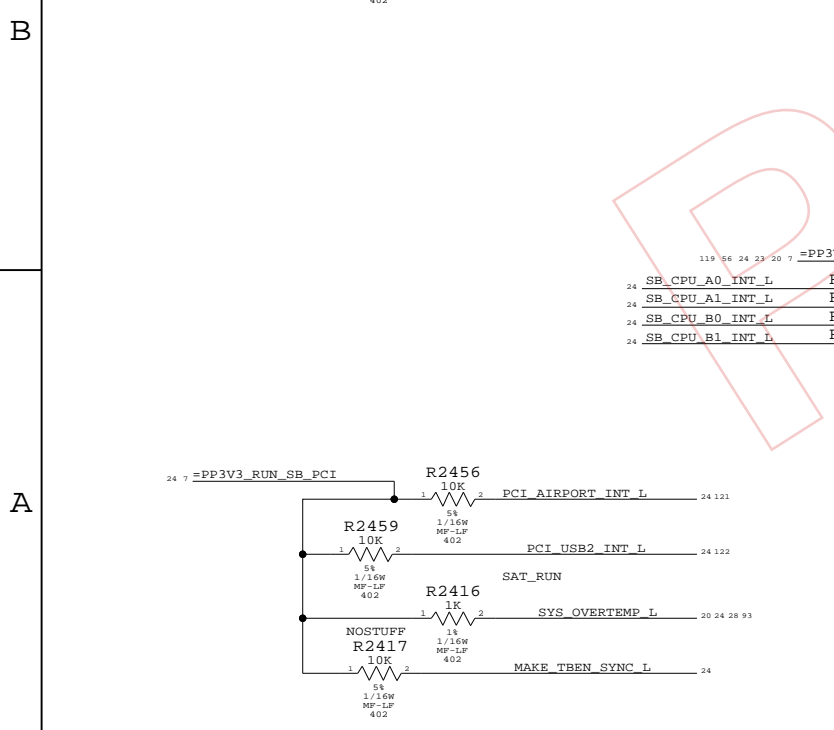
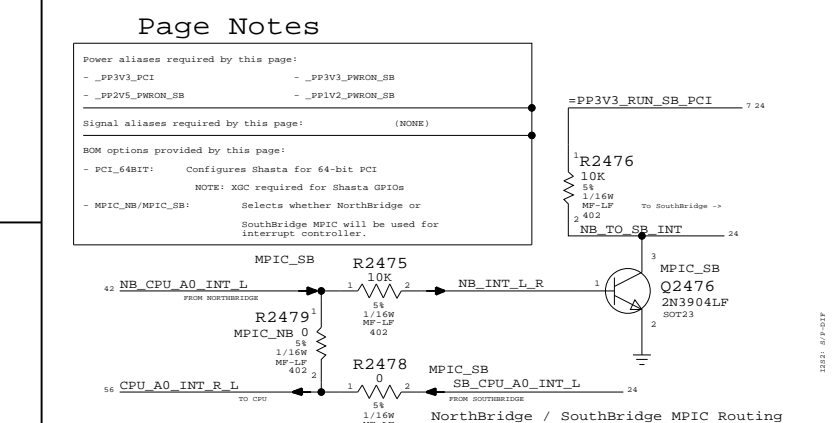
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SCALE	SHT OF		
NONE	23		154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		I2S0_DEV_TO_SB_DTI 24 147
I2S0_TO_DEV		I2S0_SB_TO_DEV_DTO 24 147
I2S0_TO_DEV	AUDIO	I2S0_MCLK 24 154
I2S0_BIDIR		I2S0_BITCLK 24 147
I2S0_BIDIR		I2S0_SYNC 24 147
I2S1_TO_SB		I2S1_DEV_TO_SB_DTI 8 24
I2S1_TO_DEV		I2S1_SB_TO_DEV_DTO 8 24
I2S1_TO_DEV	0.25mm SPACING	I2S1_MCLK 8 24
I2S1_BIDIR		I2S1_BITCLK 8 24
I2S1_BIDIR		I2S1_SYNC 8 24
I2S2_TO_SB		I2S2_DEV_TO_SB_DTI 24 154
I2S2_TO_DEV		I2S2_SB_TO_DEV_DTO 24 154
I2S2_TO_DEV	0.25mm SPACING	I2S2_MCLK 24 154
I2S2_BIDIR		I2S2_BITCLK 24 154
I2S2_BIDIR		I2S2_SYNC 24 154
SB_CLK18M_XTAL	0.38mm SPACING	SB_CLK18M_XTALI 24
SB_CLK18M_XTAL	0.38mm SPACING	SB_CLK18M_XTALO 24
SB_CLK18M_XTAL	0.38mm SPACING	SB_CLK18M_XTALO R 24
SB_CLK25M_ATA	0.38mm SPACING	SB_CLK25M_SATA 24 26
	P3MM SPACING	NB_TO_SB_INT 24
	P3MM SPACING	SB_CPU_A0_INT_L 24
	P3MM SPACING	SB_CPU_A1_INT_L 24
	P3MM SPACING	SB_CPU_B0_INT_L 24
	P3MM SPACING	SB_CPU_B1_INT_L 24
	P3MM SPACING	PCI_AIRPORT_INT_L 24 131
	P3MM SPACING	PCI_USB2_INT_L 24 132
	P3MM SPACING	I2S0_RESET_L 24 147
	P3MM SPACING	I2S1_RESET_L 8 24
	P3MM SPACING	I2S2_RESET_L 24 154
	P3MM SPACING	MB_SLOT_RESET_L 24
	P3MM SPACING	NB_SLOT_RESET_L 20 24
	P3MM SPACING	SB_CPU_A0_SRESET_L 24 56
	P3MM SPACING	SB_CPU_A1_SRESET_L 24 56
	P3MM SPACING	SB_CPU_B0_SRESET_L 24 56
	P3MM SPACING	SB_CPU_B1_SRESET_L 24 56



Shasta Serial / Misc

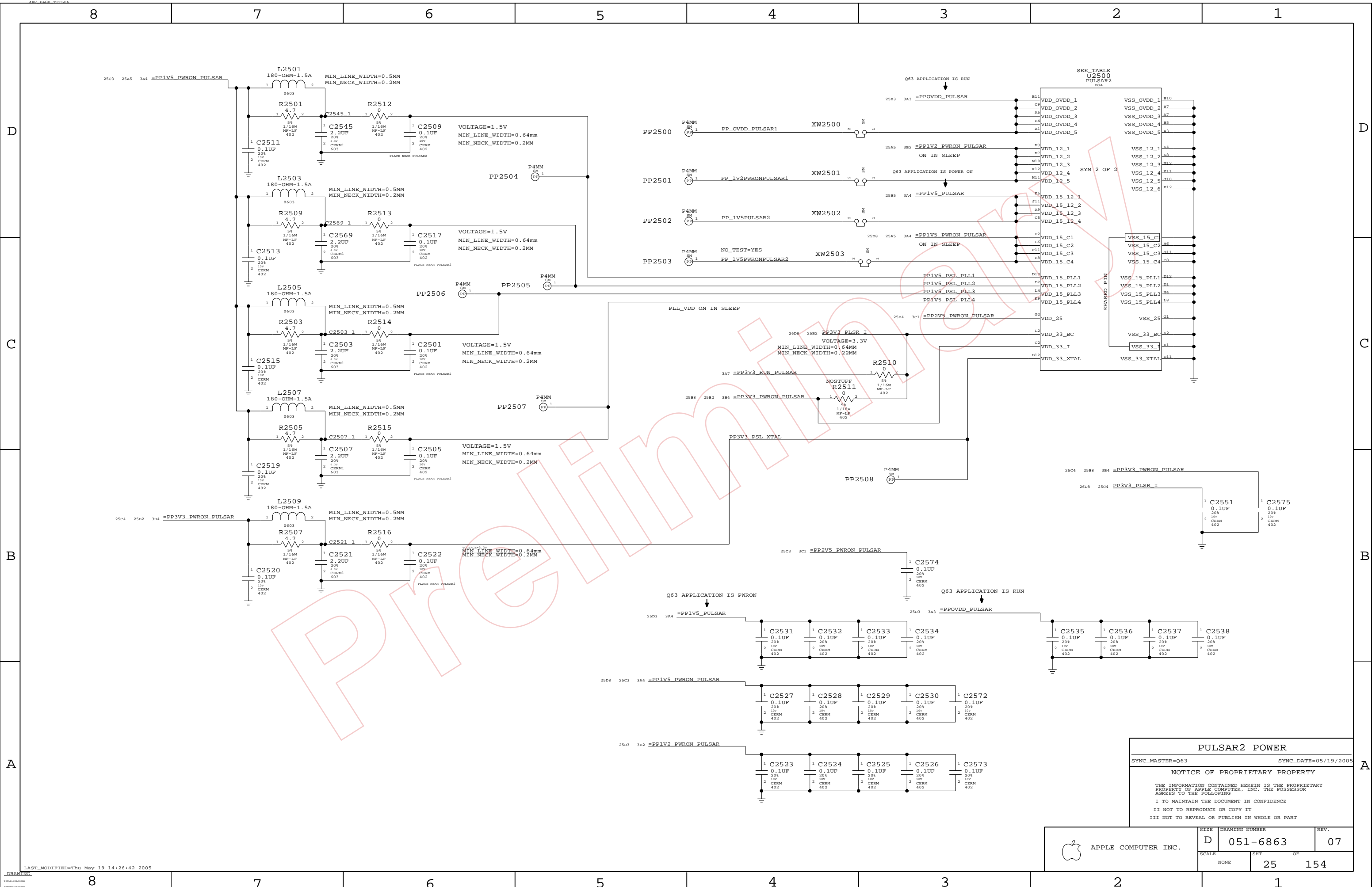
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D	051-6863	07
SCALE	SHT	OF
NONE	24	154



PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

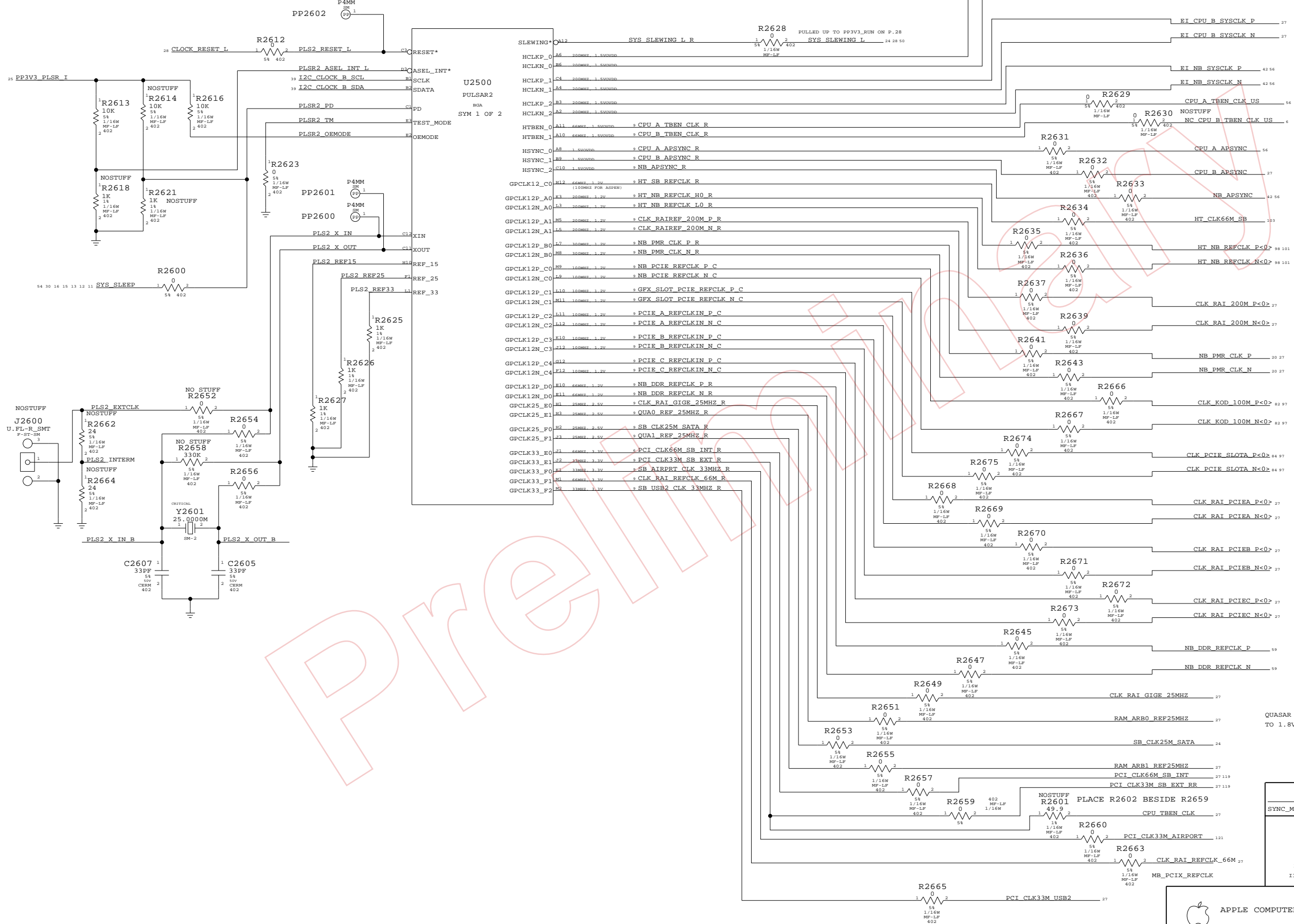
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. 07
	SCALE NONE	SHEET 25	OF 154

PLACE ALL 0-OHM SERIES RESISTORS ON THIS PAGE NEAR PULSAR



QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN TO 1.8V ON QUASAR PAGES
LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS
 SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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	D	051-6863	07
SCALE	NONE	SHT	OF
		26	154

N/C ALIASES

N/C RAINIER CLOCKS

NC_CLK_RAI_REFCLK_66M == CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

NC_CLK_RAI_GIGE_25MHZ == CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

NC_CLK_RAI_200M_P<0> == CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_200M_N<0> == CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEA_P<0> == CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEA_N<0> == CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEB_P<0> == CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEB_N<0> == CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEC_P<0> == CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

NC_CLK_RAI_PCIEC_N<0> == CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

NC_CPU_TBEN_CLK == CPU_TBEN_CLK 26
MAKE_BASE=TRUE

NC_EI_CPU_B_SYSCLK_P == EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

NC_EI_CPU_B_SYSCLK_N == EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

NC_CPU_B_APSYNC == CPU_B_APSYNC 26
MAKE_BASE=TRUE

CPU_TBEN_CLK IS FOR Q63 ONLY
IT IS THE INPUT TO THE AND GATE WHICH
GENERATES CPUA AND CPUB_TBEN_CLK

N/C QUASAR CLOCKS

NC_RAM_ARB0_REF25MHZ == RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

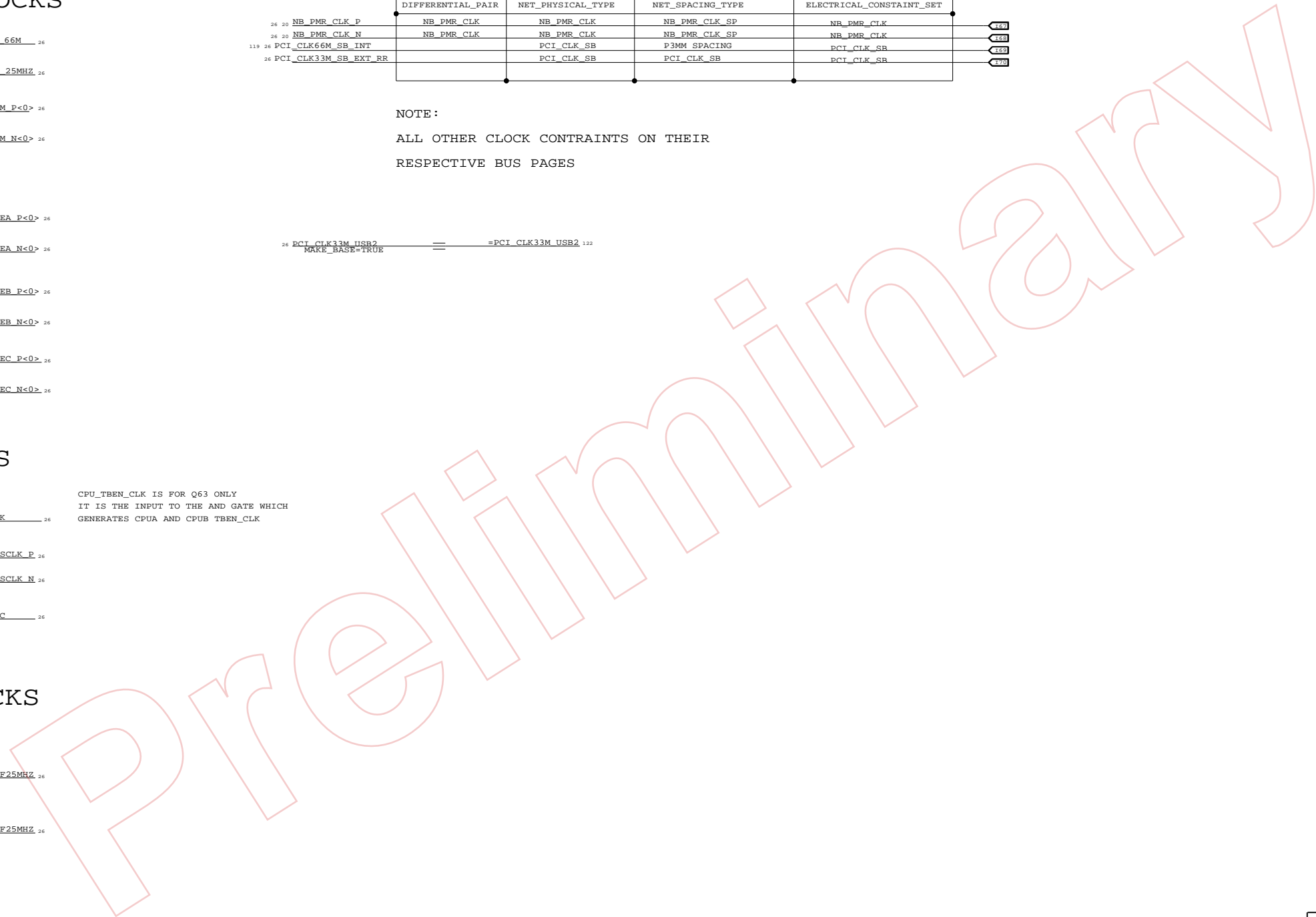
NC_RAM_ARB1_REF25MHZ == RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTRAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	499
26 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	499
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM_SPACING	PCI_CLK_SB	499
26 PCI_CLK33M_SB_EXT RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB	499

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 == PCI_CLK33M_USB2 122
MAKE_BASE=TRUE



Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=05/19/2005

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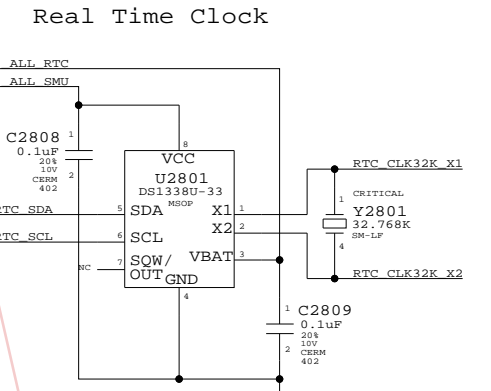
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	D	051-6863	07
SCALE	NONE	SHT	27 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_CLK10M_XTAL	0.38MM SPACING	
SMU_CLK10M_XOUT	0.38MM SPACING	
SMU_CLK10M_XOUT_R	0.38MM SPACING	
RTC_CLK32K_XTAL	0.38MM SPACING	
RTC_CLK32K_X1	0.38MM SPACING	
RTC_CLK32K_X2	0.38MM SPACING	
SMU_IO_RESET_L	P3MM SPACING	
SYS_NORTH_RESET_L	0.25MM SPACING	

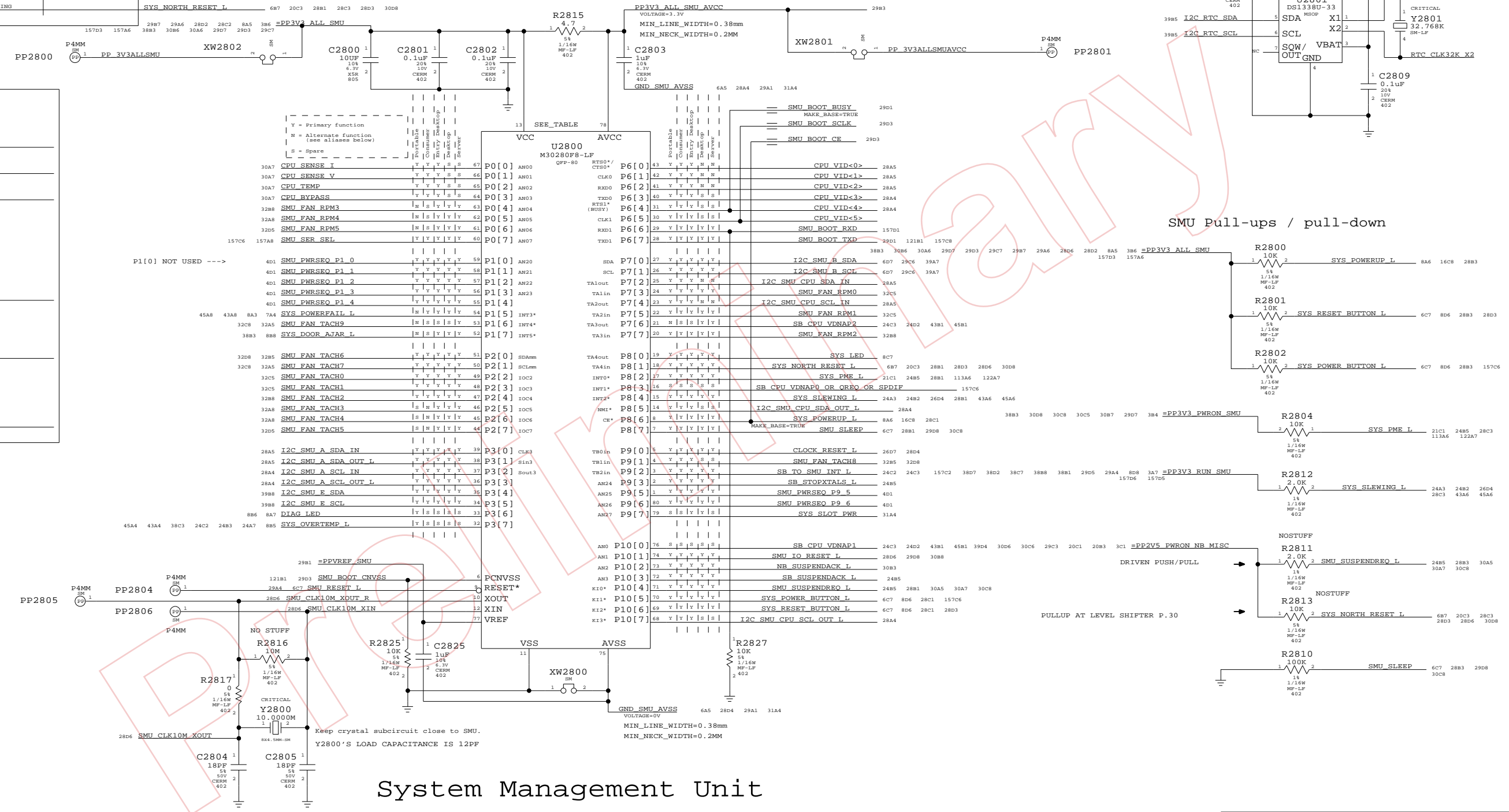
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
SMU_RESET	0.25MM SPACING	
SMU_RESET	0.25MM SPACING	
SMU_RESET	P3MM SPACING	
SMU_RESET	P3MM SPACING	

SYS_NORTH_RESET_L	687	20C3	28B1	28C3	28D6	30D8
SYS_IO_RESET_L	21C5	24B7	29D6	119A4	122A7	29D7
CLOCK_RESET_L	26D7	28B3				
SYS_RESET_BUTTON_L	6C7	8D6	28B3	28C1		



Page Notes

- Power aliases required by this page:
- =PP3V3_ALL_SMU
 - =PP3V3_ALL_RTC
 - =PP3V3_PWRON_SMU
 - =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)
- Signal aliases required by this page:
- (NONE)
- BOM options provided by this page:
- (NONE)
- NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.
- NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.
- NOTE: Some primary and alternate functions require pull-ups that are not provided on this page. Please review the latest SMU specification to ensure missing pull-ups are provided on another page.
- NOTE: Pinout matches SMU pinout v1.51.



System Management Unit

Alternate Functions

Tower & Server			
Port	Signal	Port	Signal
28C3	CPU VID<0>	6.0	SAT MRESET_L
28C3	CPU VID<1>	6.1	CPU_A_INSERTED_L
28C3	CPU VID<2>	6.2	CPU_B_INSERTED_L
28C3	I2C SMU CPU SDA IN	7.2	SMU_FAN_PWM8
28C3	I2C SMU CPU SCL IN	7.4	SMU_FAN_PWM9
28B6	I2C SMU A SDA IN	3.0	I2C SMU A SDA
28B6	I2C SMU A SDA OUT_L	3.1	I2C SMU A SCL
28A5	CPU VID<3>	6.3	SMU_FAN_RPM6
28C3	CPU VID<4>	6.4	SMU_FAN_RPM7
28B6	I2C SMU A SCL IN	3.2	NB_TDI
28B6	I2C SMU A SCL OUT_L	3.3	NB_TCK
28B3	I2C SMU CPU SDA OUT_L	8.6	NB_TMS
28B3	I2C SMU CPU SCL OUT_L	16.7	NB_TDO_SMU

System Management Unit

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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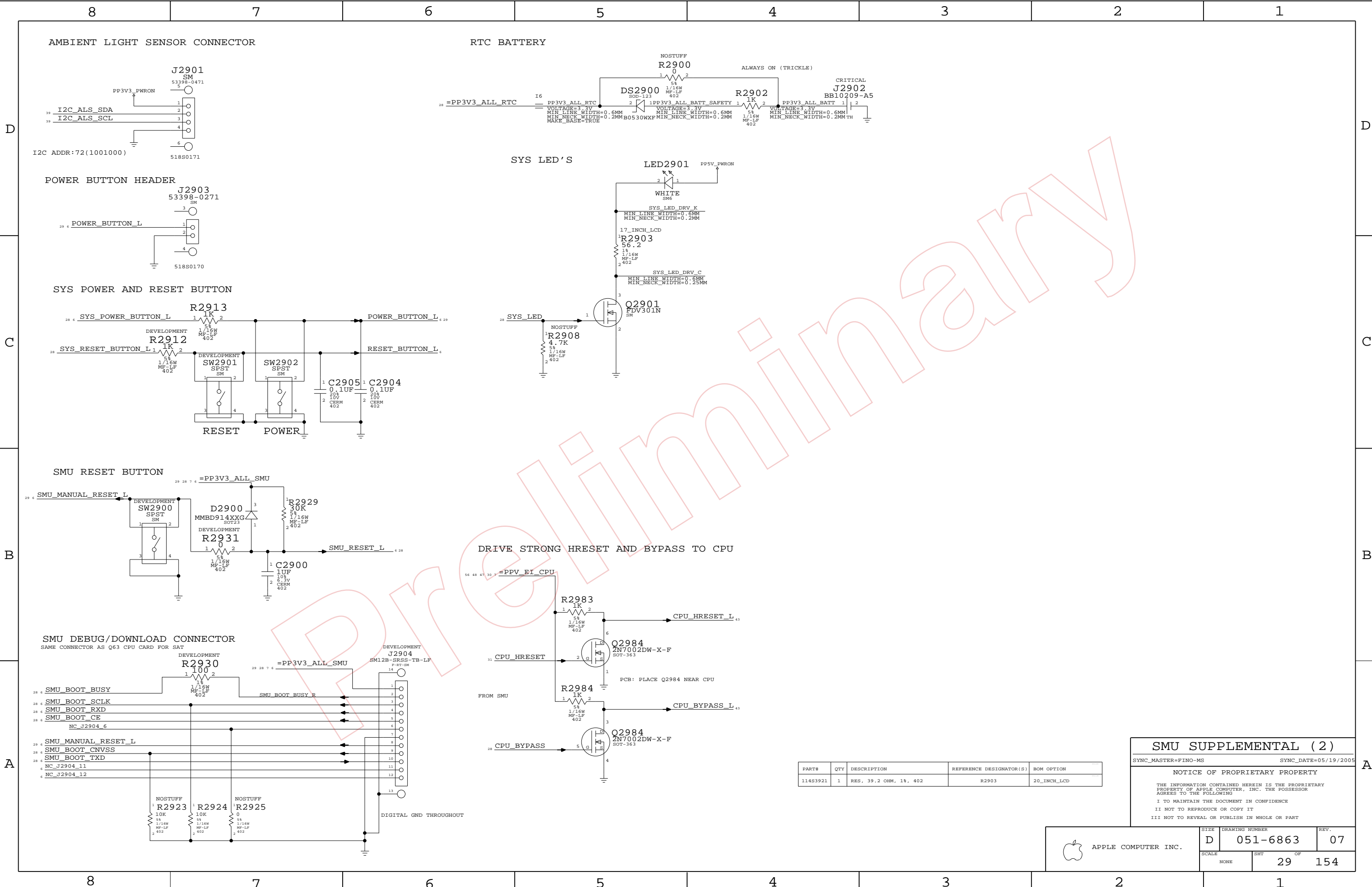
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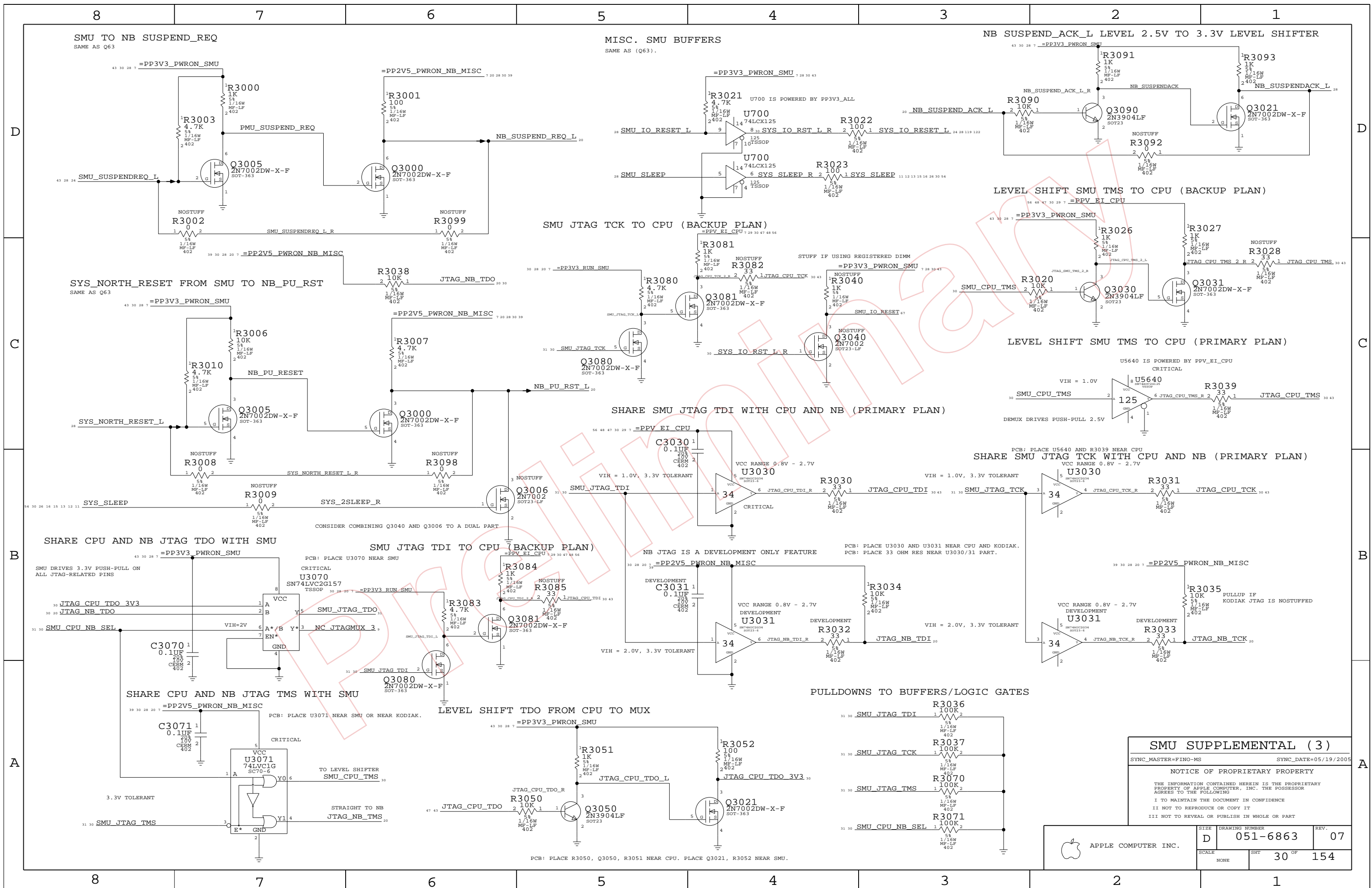
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	D	051-6863	07
SCALE	NONE	SHT	OF
		28	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11483921	1	RES, 39.2 OHM, 1%, 402	R2903	20_INCH_LCD

SMU SUPPLEMENTAL (2)
 SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005
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SCALE	NONE	SHT OF	29 OF 154



SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

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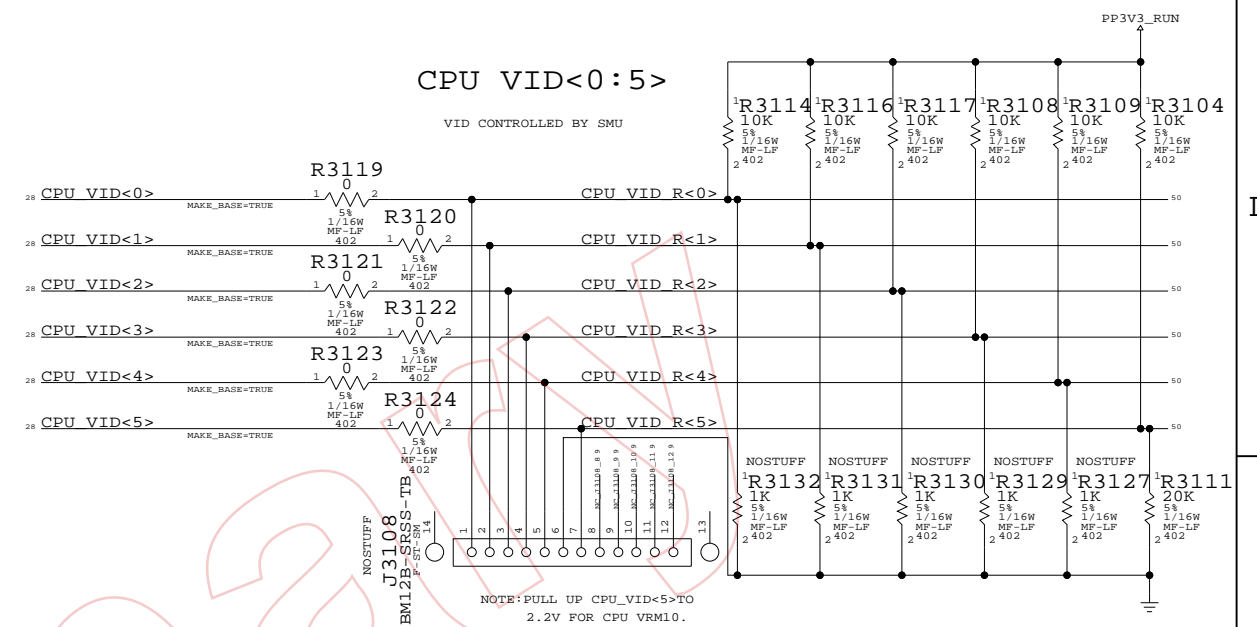
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT	30 OF 154	
NONE			

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION	Q63 NET NAME (SHARED PAGE)
Q63 NC'S THESE AS IT USES A SAT.		CPU_SENSE_I0 P0.0	
		CPU_SENSE_V0 P0.1	
		CPU_TEMP0 P0.2	
		CPU_BYPASS P0.3	
M23/M33 DOESN'T HAVE THOSE FANS.	NC_SMU_FAN_RPM3	FAN_CNTRL0_4 P0.4	SMU_FAN_RPM3 28
	NC_SMU_FAN_RPM4	FAN_CNTRL0_5 P0.5	SMU_FAN_RPM4 28
	NC_SMU_FAN_RPM5	FAN_CNTRL0_6 P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE. M23/M33 DOESN'T USE. P1.0 NC ON PG 7.	NC_SMU_SER_SEL	SMU_SCCL_SEL P0.7	SMU_SER_SEL 28
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_SENSE_I1 P1.1	
		CPU_SENSE_V1 P1.2	
		CPU_TEMP1 P1.3	
		PS1_3 P1.3	
		PS1_4 P1.4	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		POWERFAIL* P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE. CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR? CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE. M23/M33 DOESN'T HAVE THIS FAN.	NC_SMU_CPU_VID_LE0	CPU_VID_LE0 P1.6	SMU_FAN_TACH9 28
	NC_SYS_DOOR_AJAR_L	DOOR_AJAR* P1.7	SYS_DOOR_AJAR_L 28
	NC_SMU_CPU_VID_LE1	CPU_VID_LE1 P2.5	SMU_FAN_TACH6 28
	NC_SMU_FAN_TACH7	FAN_TACH2_1 P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2 P2.2	
		FAN_TACH2_3 P2.3	
		FAN_TACH2_4 P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7. M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	NC_SMU_FAN_TACH3	FAN_TACH2_5 P2.5	SMU_FAN_TACH3 28
	NC_SMU_FAN_TACH4	FAN_TACH2_6 P2.6	SMU_FAN_TACH4 28
	NC_SMU_FAN_TACH5	FAN_TACH2_7 P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	I2C_SMU_A_SDA	IIC_A_DAT P3.0	I2C_SMU_A_SDA_IN 28
	I2C_SMU_A_SCL	IIC_A_CLK P3.1	I2C_SMU_A_SDA_OUT_L 28
	SMU_JTAG_TDI	TDI P3.2	I2C_SMU_A_SCL_IN 28
	SMU_JTAG_TCK	TCK P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT P3.4	
		IIC_E_CLK P3.5	
		DIAG_LED P3.6	
		OVERTEMP* P3.7	
		CPU_VID[0] P6.0	
		CPU_VID[1] P6.1	
		CPU_VID[2] P6.2	
		CPU_VID[3] P6.3	
		CPU_VID[4] P6.4	
		CPU_VID[5] P6.5	
		DEBUG_RXD P6.6	
		DEBUG_TXD P6.7	
		IIC_B_DAT P7.0	
		IIC_B_CLK P7.1	
Q63 USE OF P7.2 IS PWM FAN SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	SMU_CPU_NB_SEL	CPU_TMS P7.2	I2C_SMU_CPU_SDA_IN 28
M23/M33 DOESN'T HAVE THIS FAN (P7.4) M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.	NC_I2C_SMU_CPU_SCL_IN	FAN_CNTRL7_3 P7.3	I2C_SMU_CPU_SCL_IN 28
		FAN_CNTRL7_4 P7.4	
		FAN_CNTRL7_5 P7.5	
		VDNAP2 P7.6	
		FAN_CNTRL7_7 P7.7	
		SYSTEM_LED P8.0	
		NB_RESET* P8.1	
		PME* P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	SB_VDNAP0	VDNAP0 P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING* P8.4	
	SMU_JTAG_TMS	NR_TMS P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP* P8.6	
		SLEEP P8.7	
		CLK_RESET* P9.0	
Q63 USE OF P9.1 IS TACH 8.	CPU_HRESET	CPU_HRESET P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL* P9.2	
		STOP_XTAL* P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7. M23/M33 HAS NO SLOTS.	NC_SLOT_TOTAL_PWR	PS9_5 P9.5	SYS_SLOT_PWR 28
		PS9_6 P9.6	
		VDNAP1 P10.0	
		IO_RESET* P10.1	
		SUSPEND_ACK* P10.2	
		SUSPEND_IO_ACK* P10.3	
		SUSPEND_REQ* P10.4	
		PWR_BUTTON* P10.5	
		RST_BUTTON* P10.6	
	SMU_JTAG_TDO	TDO P10.7	I2C_SMU_CPU_SCL_OUT_L 28



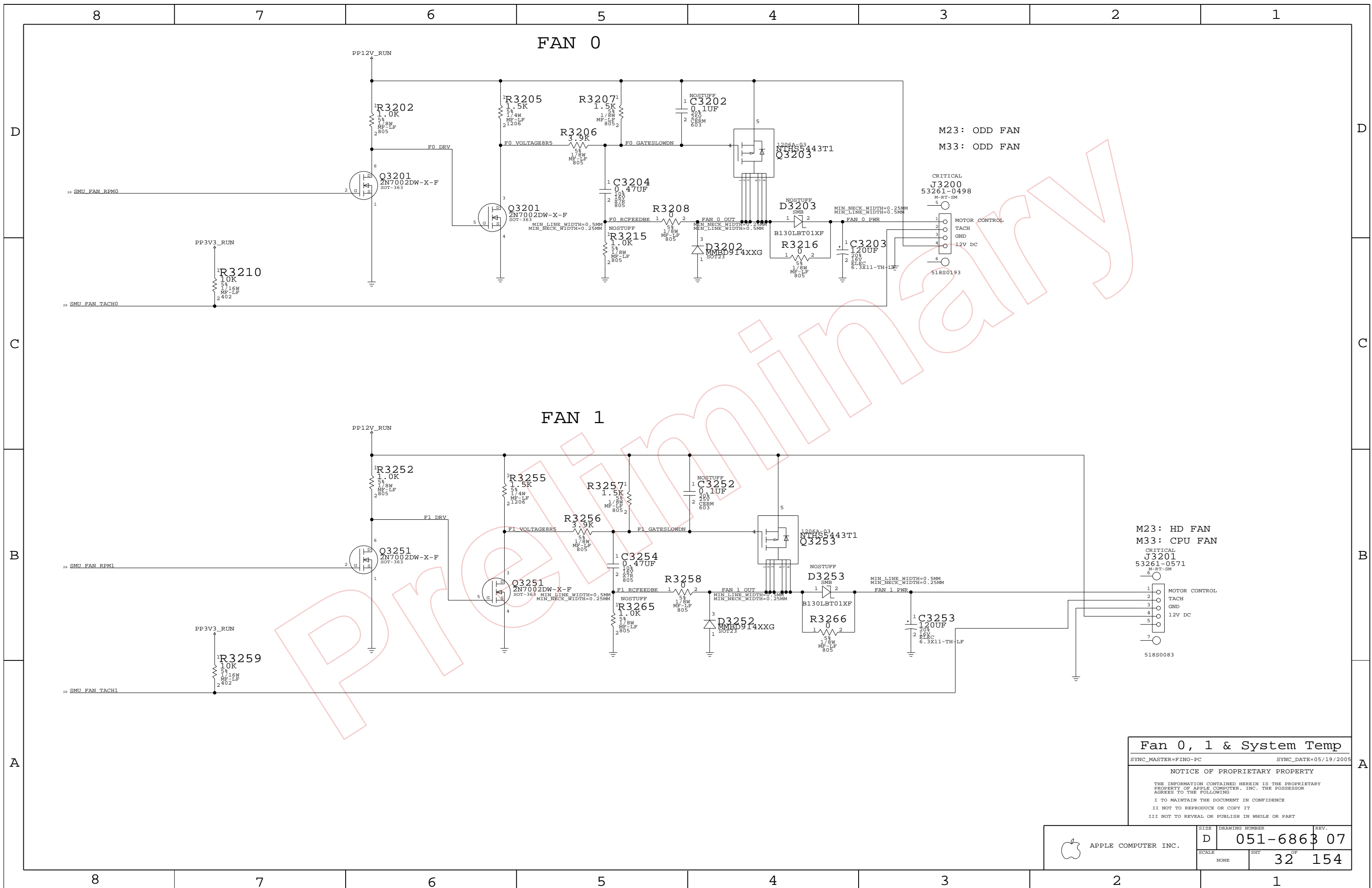
SMU SUPPLEMENTAL (4)

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FAN 0

FAN 1

M23: ODD FAN
M33: ODD FAN

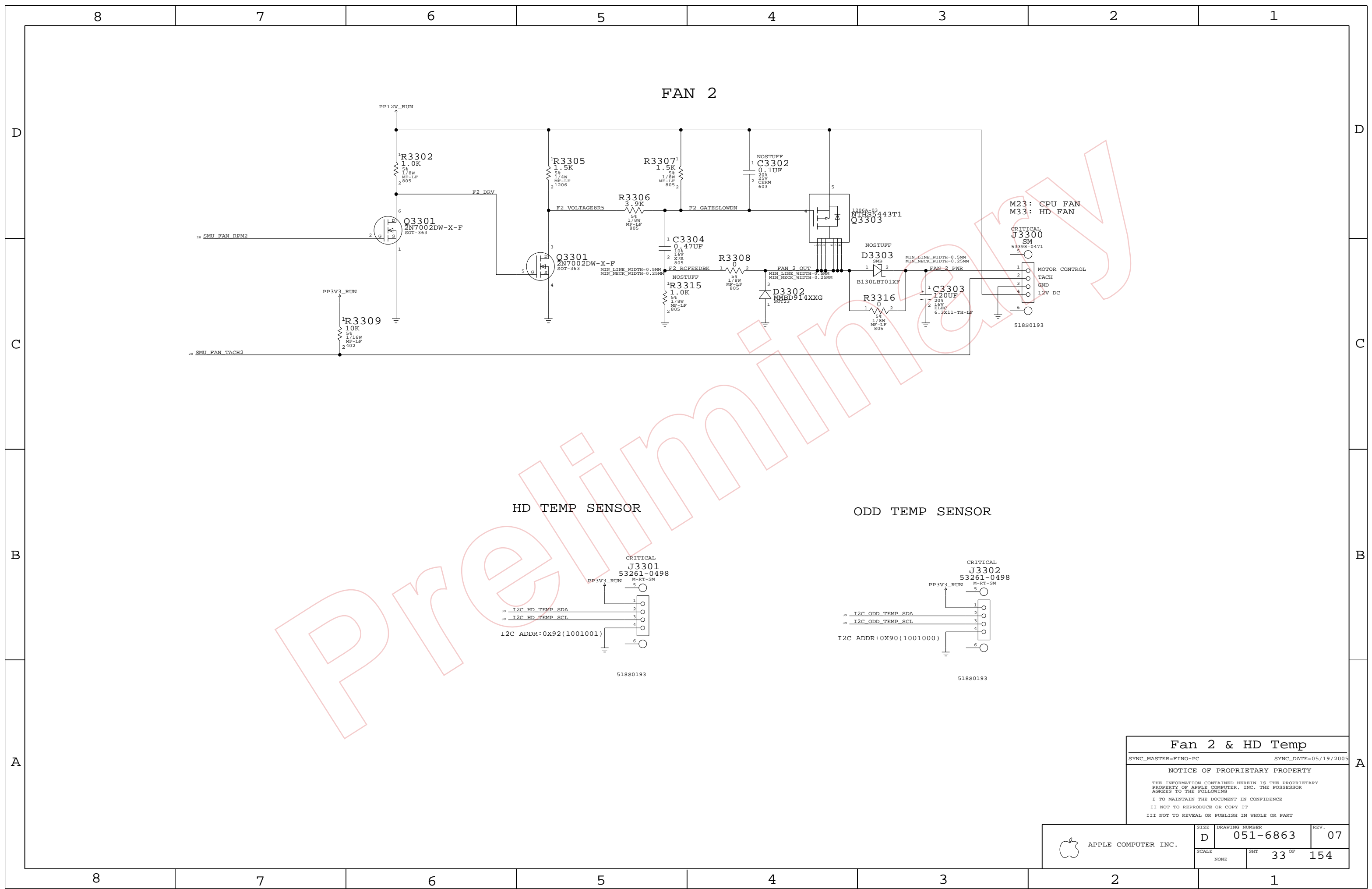
M23: HD FAN
M33: CPU FAN

Fan 0, 1 & System Temp

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Fan 2 & HD Temp

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SMU AND NB I2C A BUS

SB I2C BUS

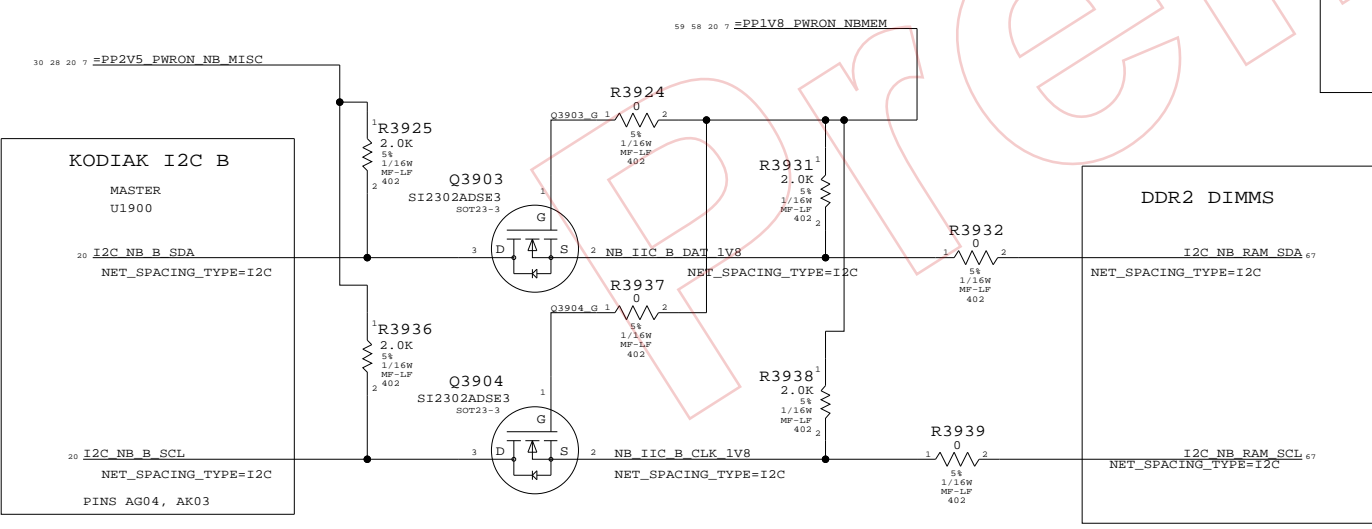
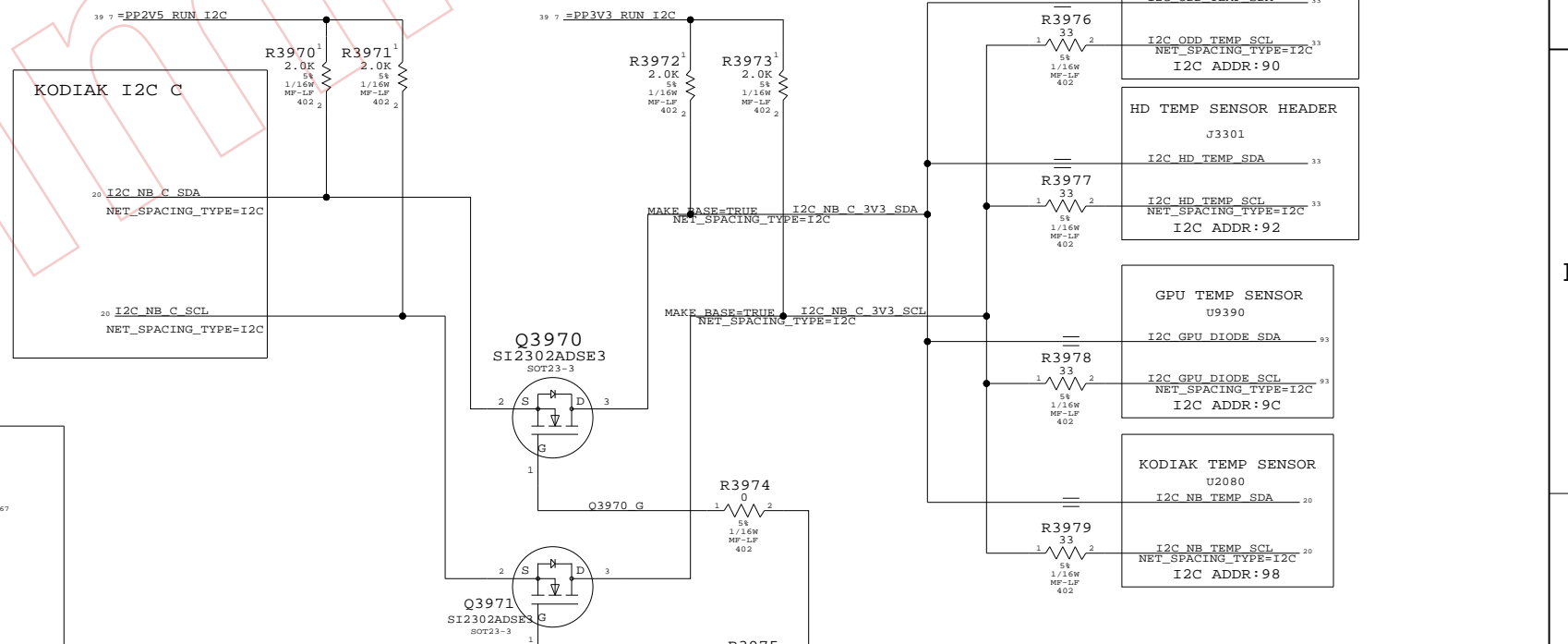
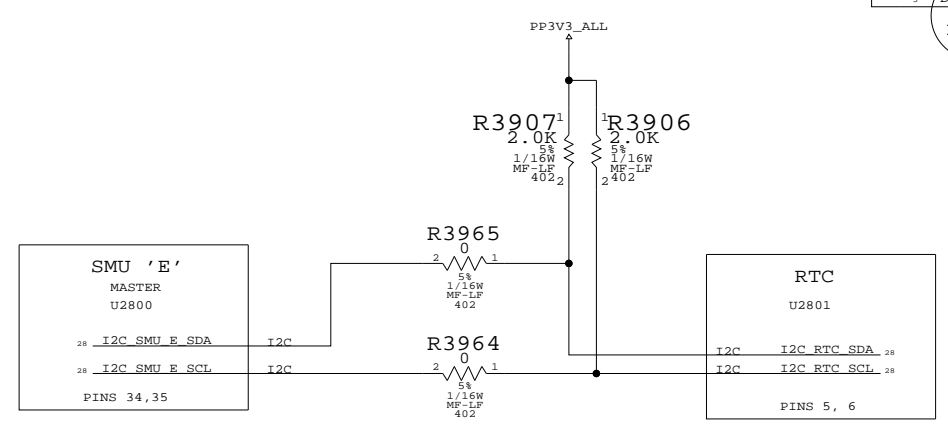
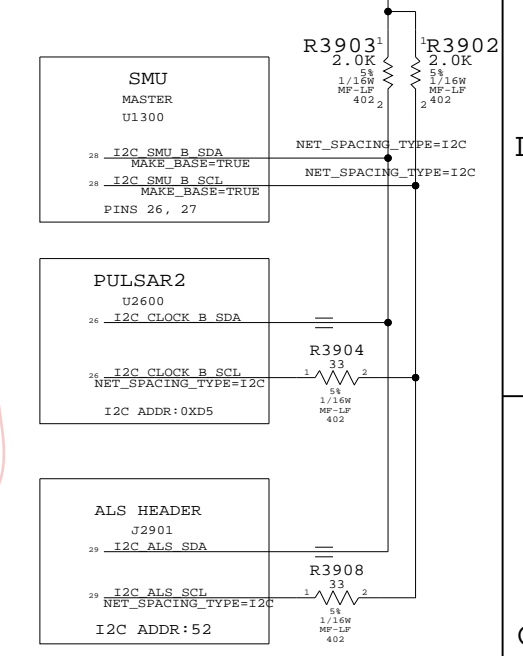
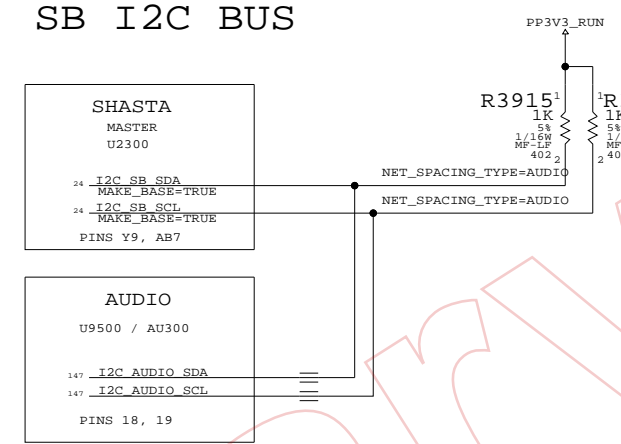
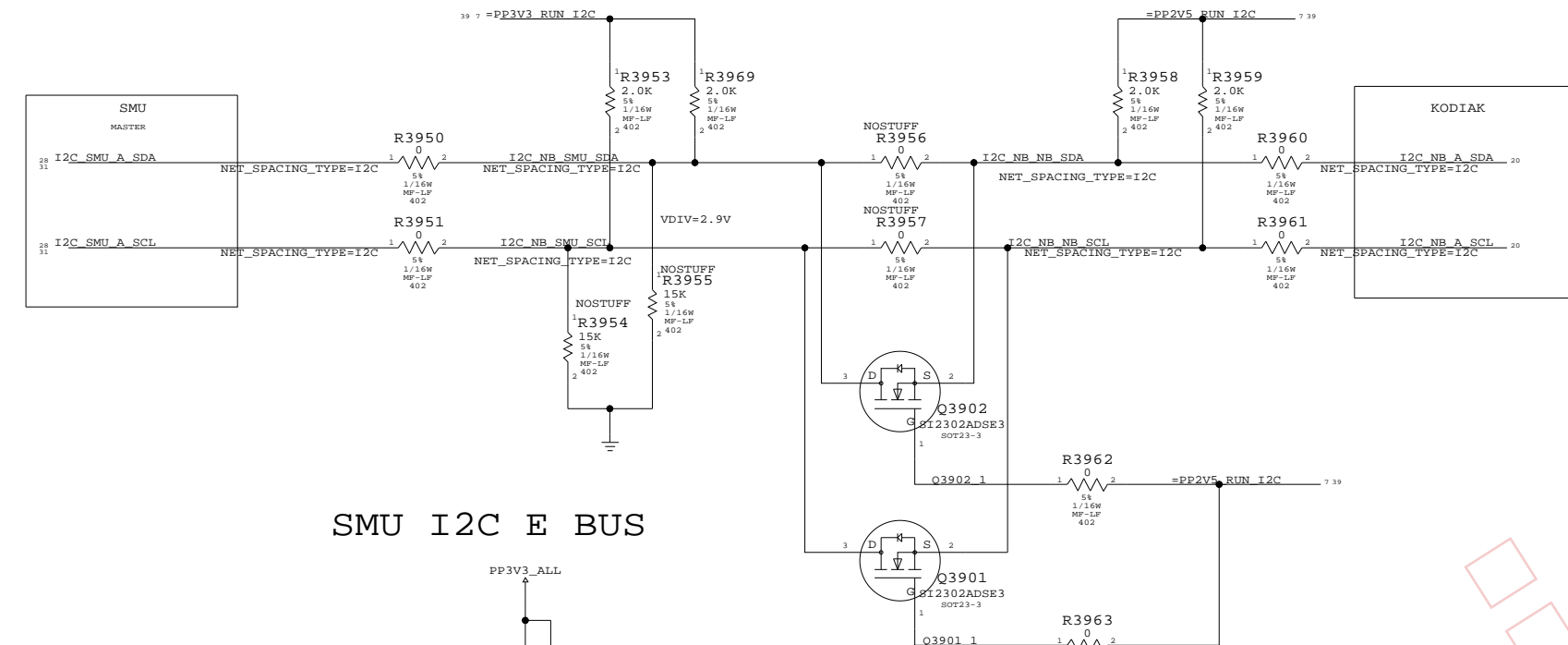
SMU I2C B BUS

SMU I2C E BUS

NB I2C C BUS

NB I2C B BUS

I2C Connections



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U1900
BGA
(7 OF 10)
PART 0
PWR/GND

KODIAK-ASIC-040B1.2

KODIAK EI PWR & CAPS
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D

D

C

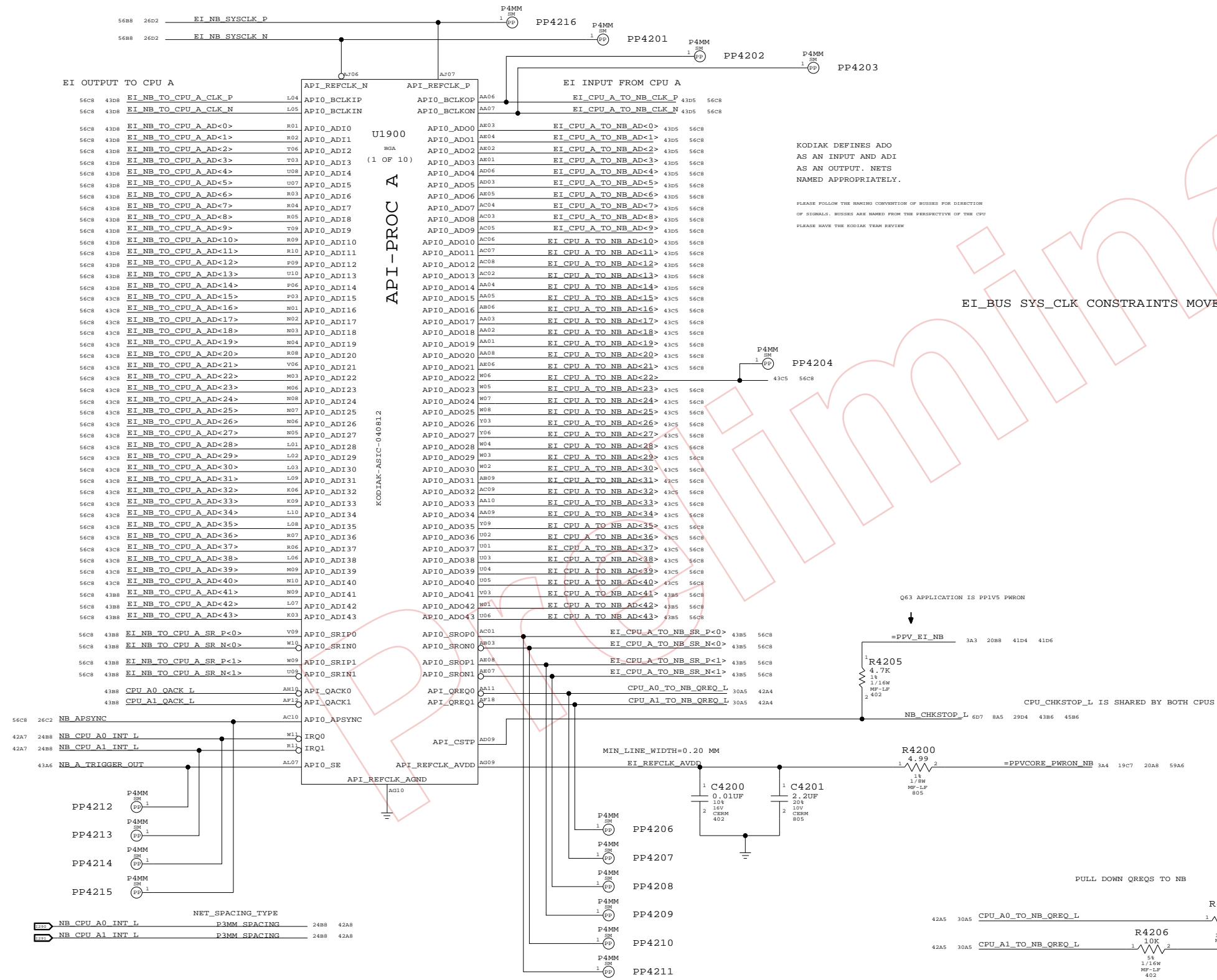
C

B

B

A

A



EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

KODIAK EI A

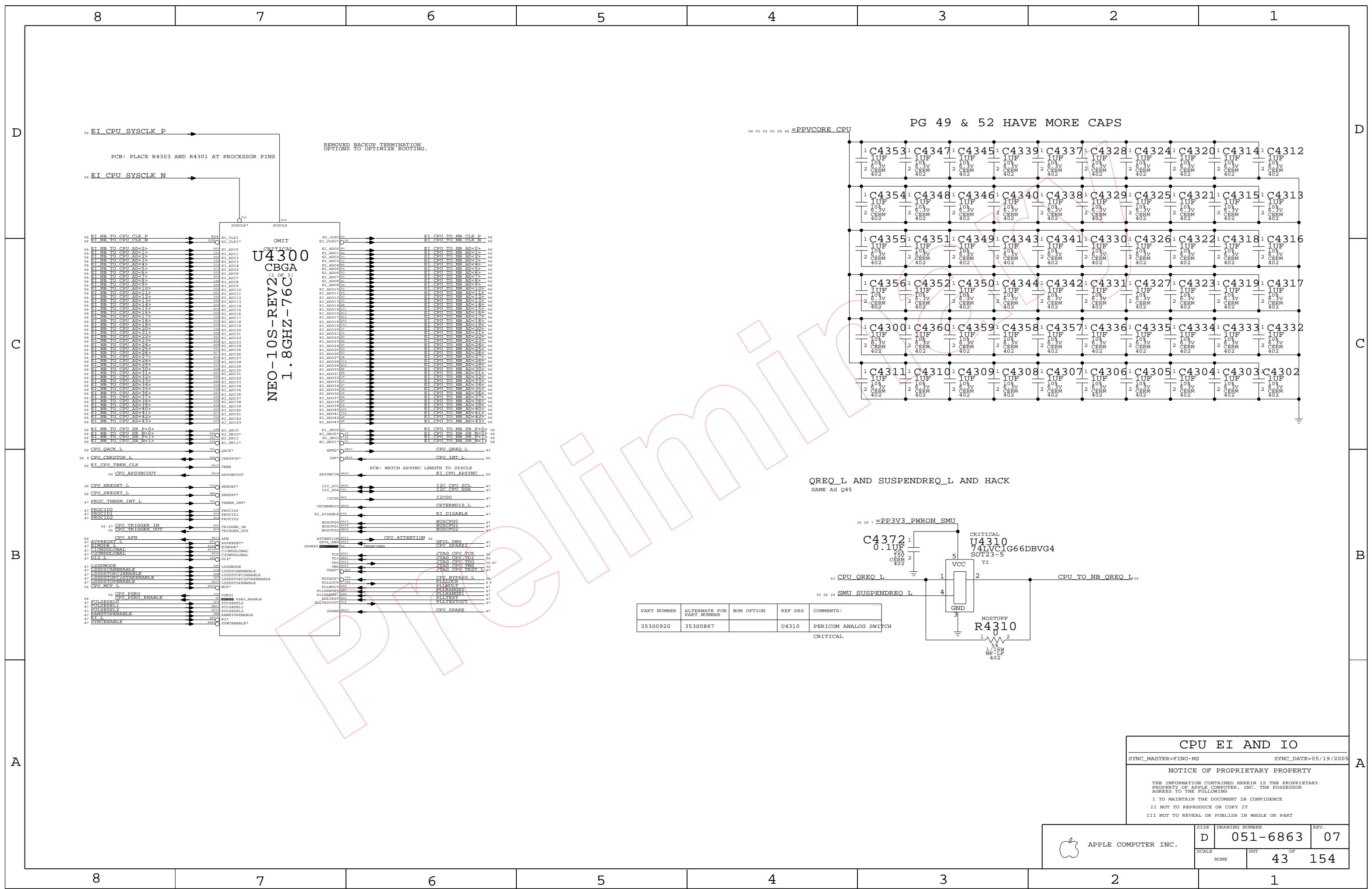
SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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PG 49 & 52 HAVE MORE CAPS

CRITICAL
U4300
 CBGA
 (1 OF 3)
 NEO-10S-REV2
 1.8GHZ-76C

QREQ_L AND SUSPENDREQ_L AND HACK
 SAME AS Q45

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0920	353S0867		U4310	PERICOM ANALOG SWITCH CRITICAL

CPU EI AND IO

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PLEASE FOLLOW THE NAMING CONVENTION OF BUSES FOR DIRECTION OF SIGNALS. BUSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU. PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI INPUT FROM CPU B

5688	45d8	EI_NB_TO_CPU_B_CLK_P	AT08	API1_BCLKIP	API1_BCLKOP	AT16	EI_CPU_B_TO_NB_CLK_P	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_CLK_N	AR08	API1_BCLKIN	API1_BCLKON	AR16	EI_CPU_B_TO_NB_CLK_N	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<0>	AM12	API1_ADI0	API1_ADO0	AP20	EI_CPU_B_TO_NB_AD<0>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<1>	AM12	API1_ADI1	API1_ADO1	AR20	EI_CPU_B_TO_NB_AD<1>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<2>	AL12	API1_ADI2	API1_ADO2	AR20	EI_CPU_B_TO_NB_AD<2>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<3>	AK12	API1_ADI3	API1_ADO3	AR20	EI_CPU_B_TO_NB_AD<3>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<4>	AP11	API1_ADI4	API1_ADO4	AL19	EI_CPU_B_TO_NB_AD<4>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<5>	AL11	API1_ADI5	API1_ADO5	AP19	EI_CPU_B_TO_NB_AD<5>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<6>	AP12	API1_ADI6	API1_ADO6	AM20	EI_CPU_B_TO_NB_AD<6>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<7>	AR12	API1_ADI7	API1_ADO7	AM18	EI_CPU_B_TO_NB_AD<7>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<8>	AT12	API1_ADI8	API1_ADO8	AL18	EI_CPU_B_TO_NB_AD<8>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<9>	AM12	API1_ADI9	API1_ADO9	AM18	EI_CPU_B_TO_NB_AD<9>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<10>	AG12	API1_ADI10	API1_ADO10	AP18	EI_CPU_B_TO_NB_AD<10>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<11>	AM11	API1_ADI11	API1_ADO11	AR18	EI_CPU_B_TO_NB_AD<11>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<12>	AG12	API1_ADI12	API1_ADO12	AT18	EI_CPU_B_TO_NB_AD<12>	45d6	5688
5688	45d8	EI_NB_TO_CPU_B_AD<13>	AG14	API1_ADI13	API1_ADO13	AR18	EI_CPU_B_TO_NB_AD<13>	45d6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<14>	AM10	API1_ADI14	API1_ADO14	AP17	EI_CPU_B_TO_NB_AD<14>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<15>	AL10	API1_ADI15	API1_ADO15	AL17	EI_CPU_B_TO_NB_AD<15>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<16>	AM10	API1_ADI16	API1_ADO16	AM20	EI_CPU_B_TO_NB_AD<16>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<17>	AP10	API1_ADI17	API1_ADO17	AT20	EI_CPU_B_TO_NB_AD<17>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<18>	AR10	API1_ADI18	API1_ADO18	AK20	EI_CPU_B_TO_NB_AD<18>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<19>	AT10	API1_ADI19	API1_ADO19	AM19	EI_CPU_B_TO_NB_AD<19>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<20>	AK10	API1_ADI20	API1_ADO20	AG20	EI_CPU_B_TO_NB_AD<20>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<21>	AL10	API1_ADI21	API1_ADO21	AL20	EI_CPU_B_TO_NB_AD<21>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<22>	AM08	API1_ADI22	API1_ADO22	AM16	EI_CPU_B_TO_NB_AD<22>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<23>	AM08	API1_ADI23	API1_ADO23	AM16	EI_CPU_B_TO_NB_AD<23>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<24>	AL08	API1_ADI24	API1_ADO24	AL16	EI_CPU_B_TO_NB_AD<24>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<25>	AP07	API1_ADI25	API1_ADO25	AK16	EI_CPU_B_TO_NB_AD<25>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<26>	AT06	API1_ADI26	API1_ADO26	AP15	EI_CPU_B_TO_NB_AD<26>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<27>	AR06	API1_ADI27	API1_ADO27	AL15	EI_CPU_B_TO_NB_AD<27>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<28>	AP08	API1_ADI28	API1_ADO28	AP16	EI_CPU_B_TO_NB_AD<28>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<29>	AT04	API1_ADI29	API1_ADO29	AM14	EI_CPU_B_TO_NB_AD<29>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<30>	AR04	API1_ADI30	API1_ADO30	AL14	EI_CPU_B_TO_NB_AD<30>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<31>	AP05	API1_ADI31	API1_ADO31	AM14	EI_CPU_B_TO_NB_AD<31>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<32>	AM06	API1_ADI32	API1_ADO32	AP14	EI_CPU_B_TO_NB_AD<32>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<33>	AR06	API1_ADI33	API1_ADO33	AR14	EI_CPU_B_TO_NB_AD<33>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<34>	AP06	API1_ADI34	API1_ADO34	AT14	EI_CPU_B_TO_NB_AD<34>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<35>	AP04	API1_ADI35	API1_ADO35	AR14	EI_CPU_B_TO_NB_AD<35>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<36>	AM03	API1_ADI36	API1_ADO36	AP13	EI_CPU_B_TO_NB_AD<36>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<37>	AN01	API1_ADI37	API1_ADO37	AL13	EI_CPU_B_TO_NB_AD<37>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<38>	AL06	API1_ADI38	API1_ADO38	AM16	EI_CPU_B_TO_NB_AD<38>	45c6	5688
5688	45c8	EI_NB_TO_CPU_B_AD<39>	AL05	API1_ADI39	API1_ADO39	AM15	EI_CPU_B_TO_NB_AD<39>	45c6	5688
5688	4588	EI_NB_TO_CPU_B_AD<40>	AL04	API1_ADI40	API1_ADO40	AT14	EI_CPU_B_TO_NB_AD<40>	4586	5688
5688	4588	EI_NB_TO_CPU_B_AD<41>	AL03	API1_ADI41	API1_ADO41	AM14	EI_CPU_B_TO_NB_AD<41>	4586	5688
5688	4588	EI_NB_TO_CPU_B_AD<42>	AN02	API1_ADI42	API1_ADO42	AM16	EI_CPU_B_TO_NB_AD<42>	4586	5688
5688	4588	EI_NB_TO_CPU_B_AD<43>	AM01	API1_ADI43	API1_ADO43	AM17	EI_CPU_B_TO_NB_AD<43>	4586	5688

KODIAK DEFINES ADO AS AN INPUT AND ADI AS AN OUTPUT. NETS NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT ELECTRICAL_CONSTRAINT_SET FOR CPU_A AND CPU_B.

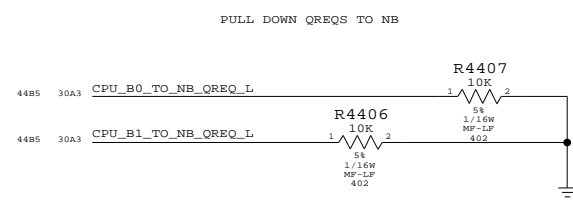
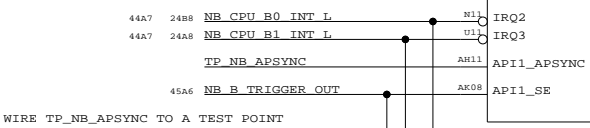
EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

API-PROC B (2 OF 10)

KODIAK-ASFC-040812

PP4413

PP4400, PP4401, PP4402, PP4403, PP4404, PP4405



KODIAK EI B

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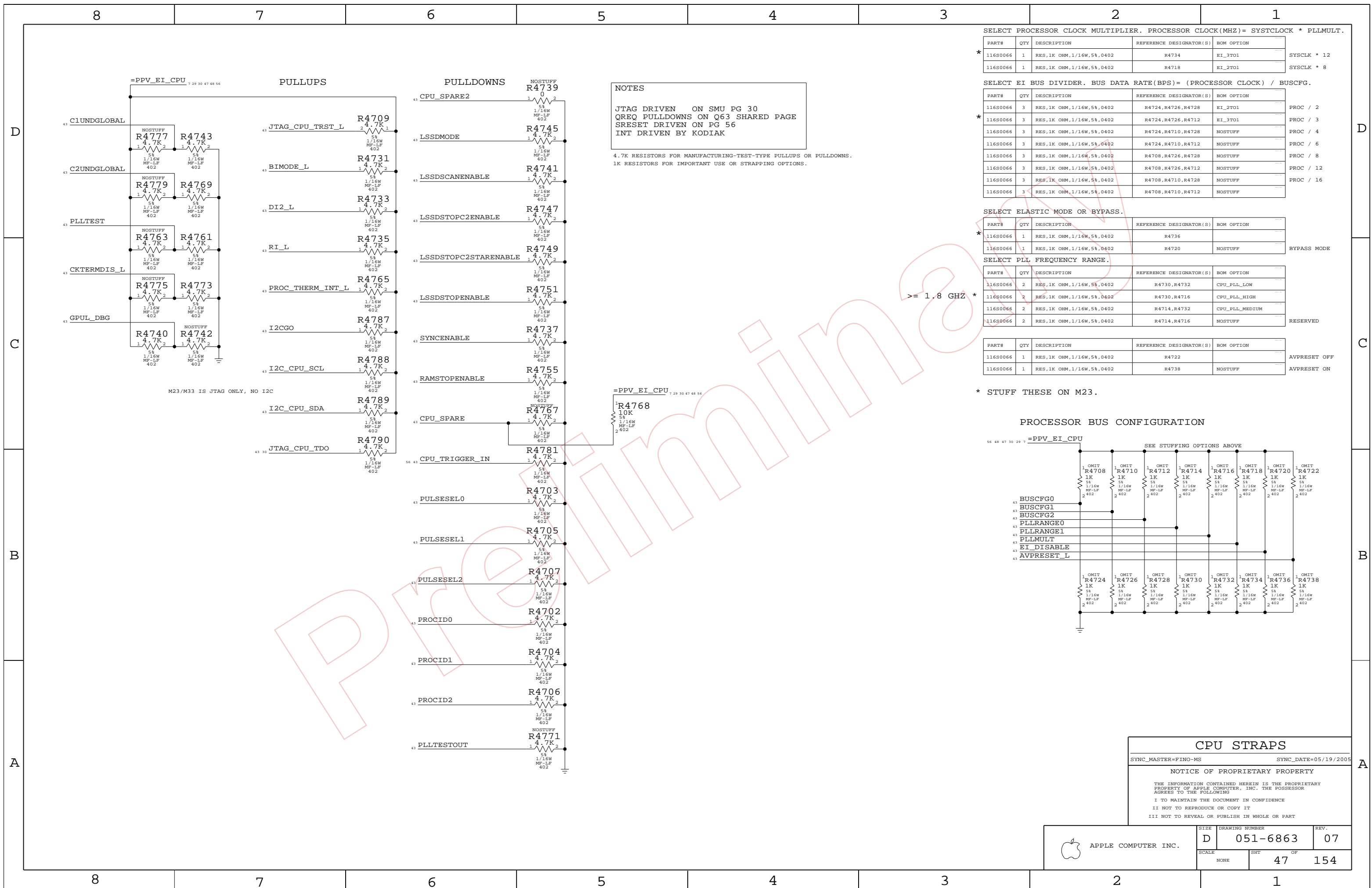
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		44	154



NOTES

JTAG DRIVEN ON SMU PG 30
 QREQ PULLDOWNS ON Q63 SHARED PAGE
 SRESET DRIVEN ON PG 56
 INT DRIVEN BY KODIAK

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
 1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

>= 1.8 GHZ *

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
* 116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3T01
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2T01

SYSCLK * 12
 SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2T01
* 116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3T01
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF
116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF

PROC / 2
 PROC / 3
 PROC / 4
 PROC / 6
 PROC / 8
 PROC / 12
 PROC / 16

SELECT ELASTIC MODE OR BYPASS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
* 116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736	
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF

BYPASS MODE

SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW
* 116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM
116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF

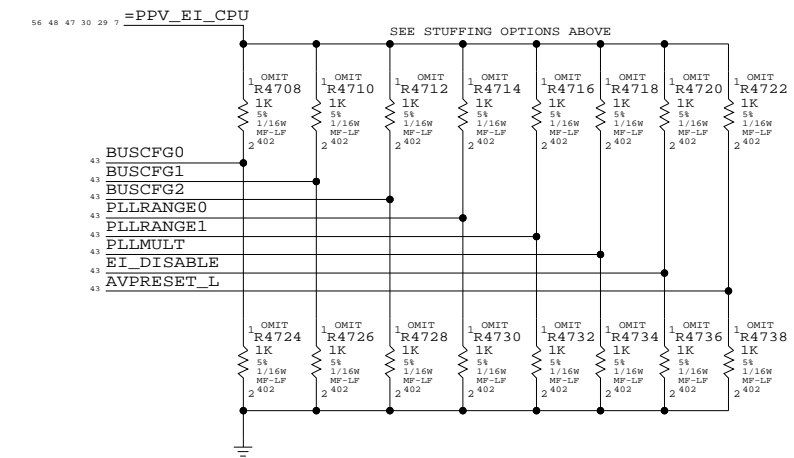
RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722	AVPRESET OFF
116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	AVPRESET ON

AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



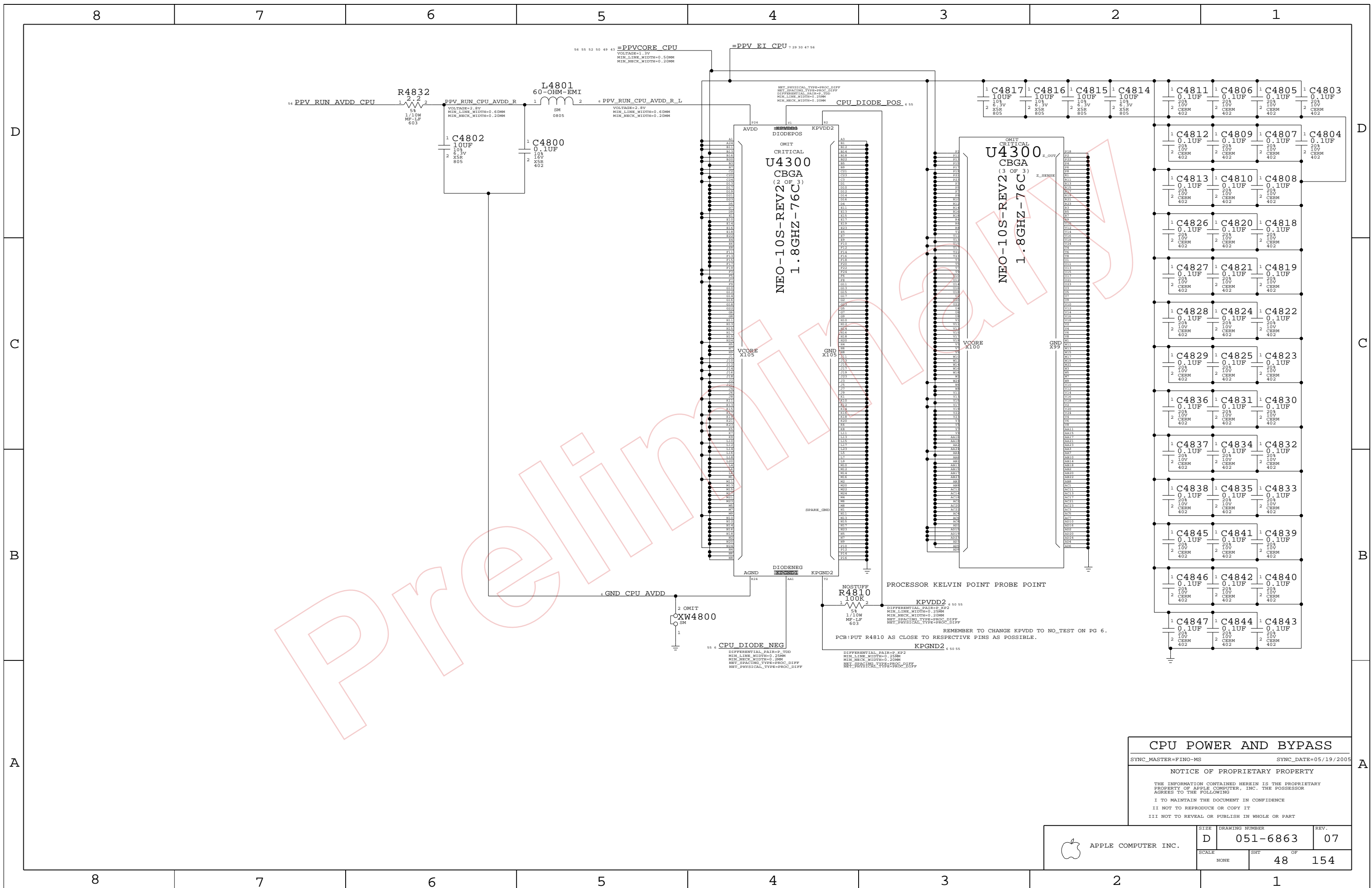
CPU STRAPS

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CPU POWER AND BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

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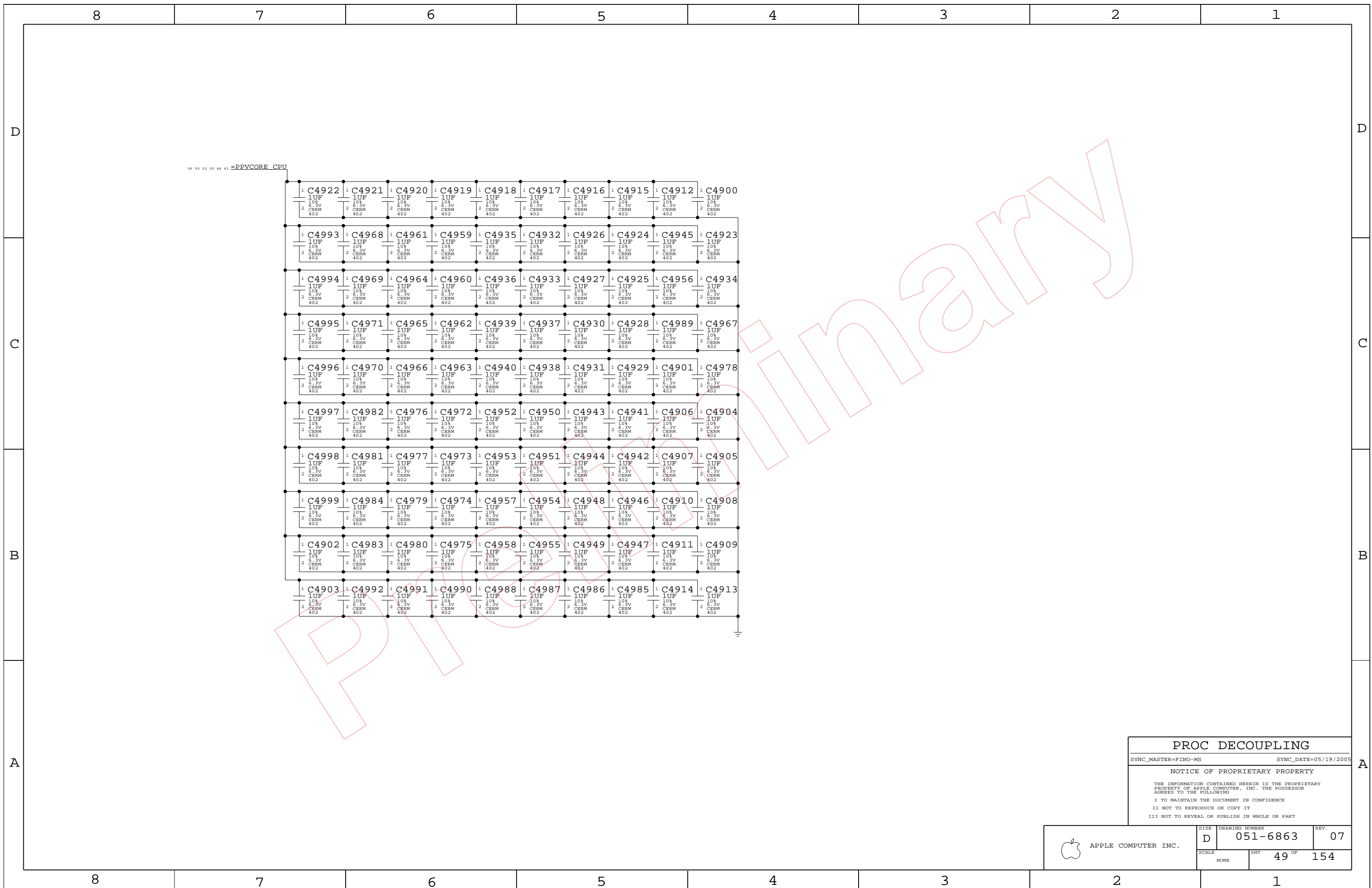
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	D	051-6863	07
SCALE	NONE	SHT	OF
		48	154



PROC DECOUPLING

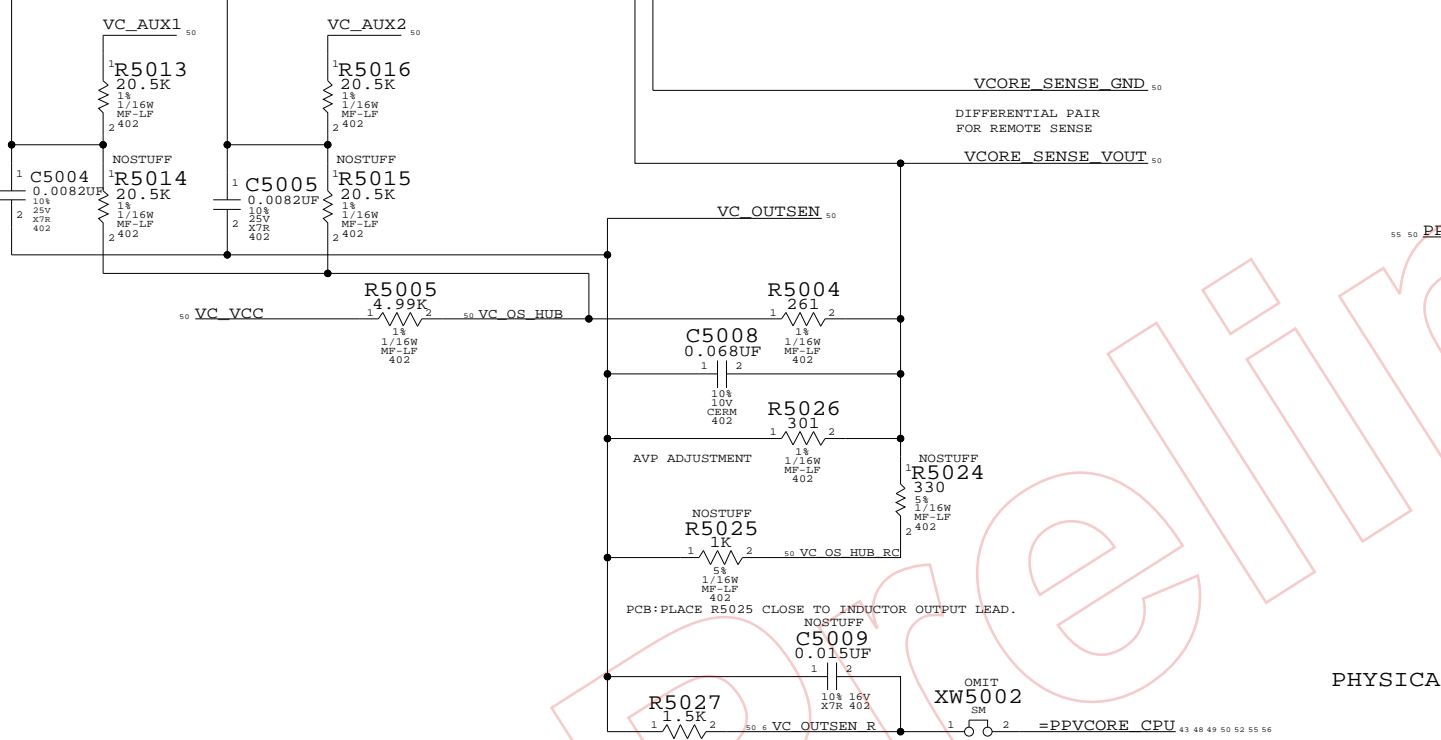
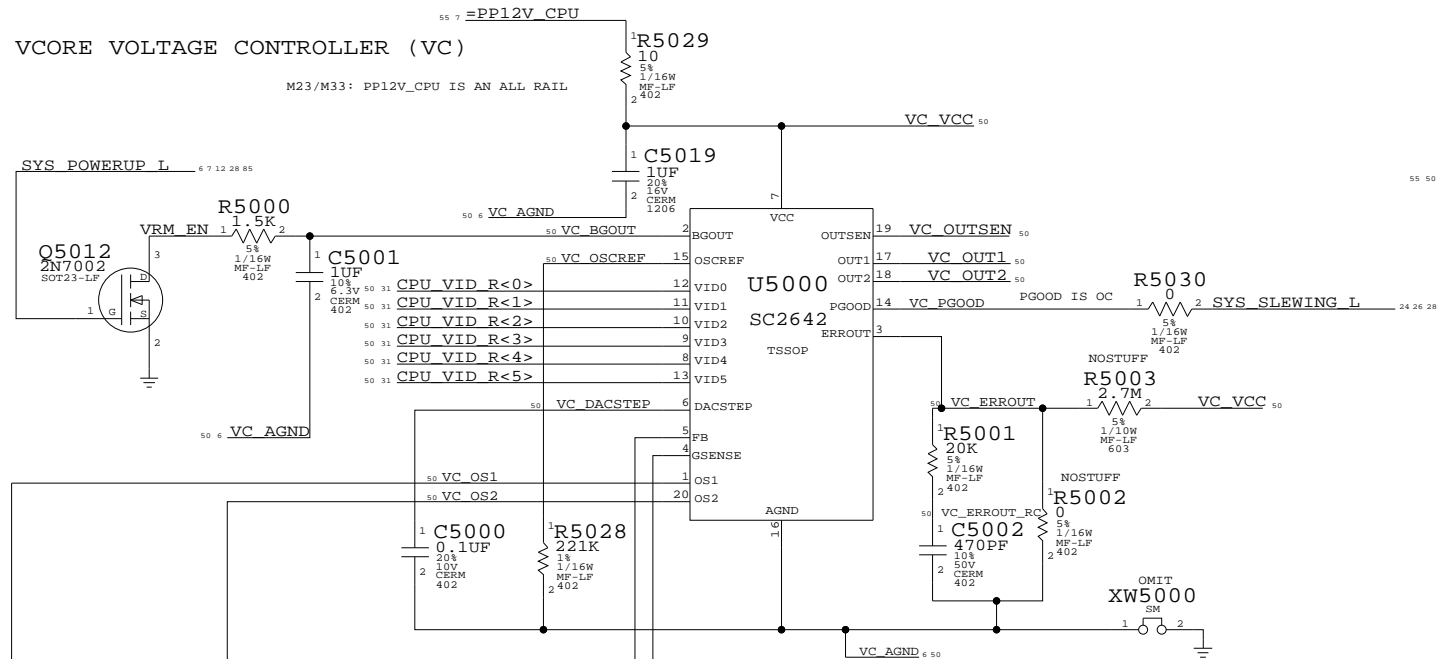
SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. 07
	SCALE NONE	SHT 49 OF	154

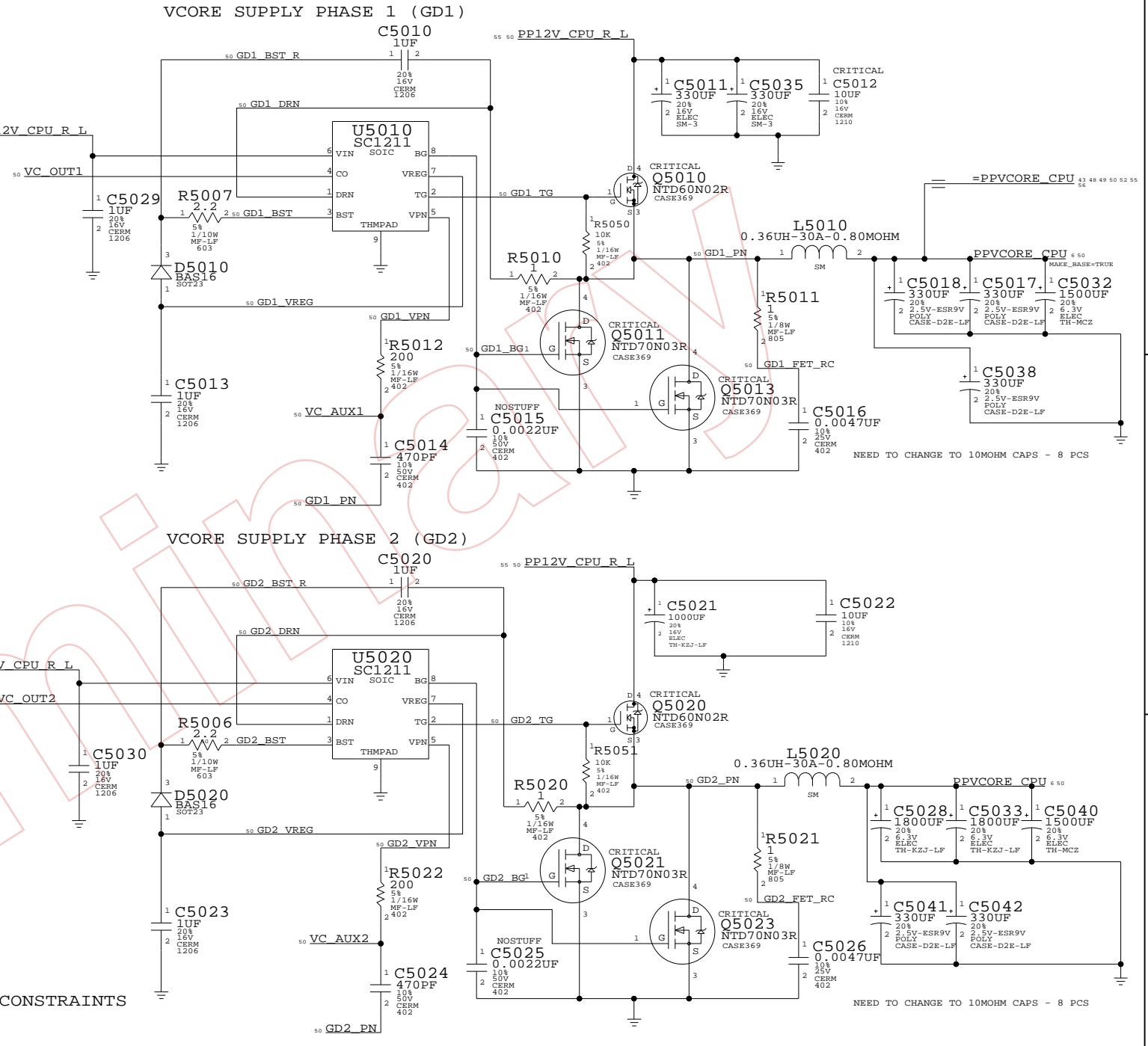


PHYSICAL CONSTRAINTS

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH	Constraint
VC_OSCREF	0.25 MM	0.20 MM	<439>
CPU_VID_R<0..5>	0.25 MM	0.20 MM	<440>
VC_DACSTEP	0.25 MM	0.20 MM	<441>
VC_AGNND	0.50 MM	0.20 MM	<442>
VC_BGOUT	0.25 MM	0.20 MM	<443>
VC_OS1	0.25 MM	0.20 MM	<444>
VC_OS2	0.25 MM	0.20 MM	<445>
VC_VCC	0.25 MM	0.25 MM	<446>
VC_OS_HUB	0.25 MM	0.20 MM	<447>
VC_OUTSEN	0.25 MM	0.20 MM	<448>
VC_OUTSEN_R	0.25 MM	0.20 MM	<449>
VCORE_SENSE_GND	0.25 MM	0.20 MM	<450>
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	<451>
VC_AUX1	0.25 MM	0.25 MM	<452>
VC_AUX2	0.25 MM	0.25 MM	<453>
VC_OUT1	0.45 MM	0.25 MM	<454>
VC_OUT2	0.45 MM	0.25 MM	<455>
VC_ERRROUT	0.25 MM	0.20 MM	<456>
VC_ERRROUT_RC	0.25 MM	0.20 MM	<457>
VC_OS_HUB_RC	0.25 MM	0.20 MM	<458>
EI_REFCLK_AVDD	0.20 MM	0.08 MM	<459>

MIN_LINE_WIDTH MIN_NECK_WIDTH

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH	Constraint
GD1_DRN	0.25 MM	0.25 MM	<460>
GD1_BST	0.25 MM	0.25 MM	<461>
GD1_VREG	0.25 MM	0.25 MM	<462>
GD1_VPN	0.25 MM	0.25 MM	<463>
GD1_TG	0.25 MM	0.25 MM	<464>
GD1_BG	0.25 MM	0.25 MM	<465>
GD1_FET_RC	0.25 MM	0.25 MM	<466>
GD1_PN	0.60 MM	0.25 MM	<467>
GD1_BST_R	0.25 MM	0.25 MM	<468>
GD2_DRN	0.25 MM	0.25 MM	<469>
GD2_BST	0.25 MM	0.25 MM	<470>
GD2_VREG	0.25 MM	0.25 MM	<471>
GD2_VPN	0.25 MM	0.25 MM	<472>
GD2_TG	0.25 MM	0.25 MM	<473>
GD2_BG	0.25 MM	0.25 MM	<474>
GD2_FET_RC	0.25 MM	0.25 MM	<475>
GD2_PN	0.60 MM	0.25 MM	<476>
GD2_BST_R	0.25 MM	0.25 MM	<477>



CPU VCORE VREG

SYNC_MASTER=M33-MS SYNC_DATE=05/19/2005

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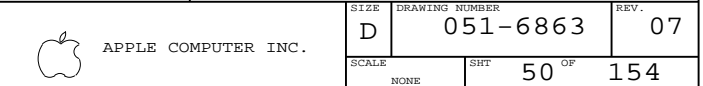
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

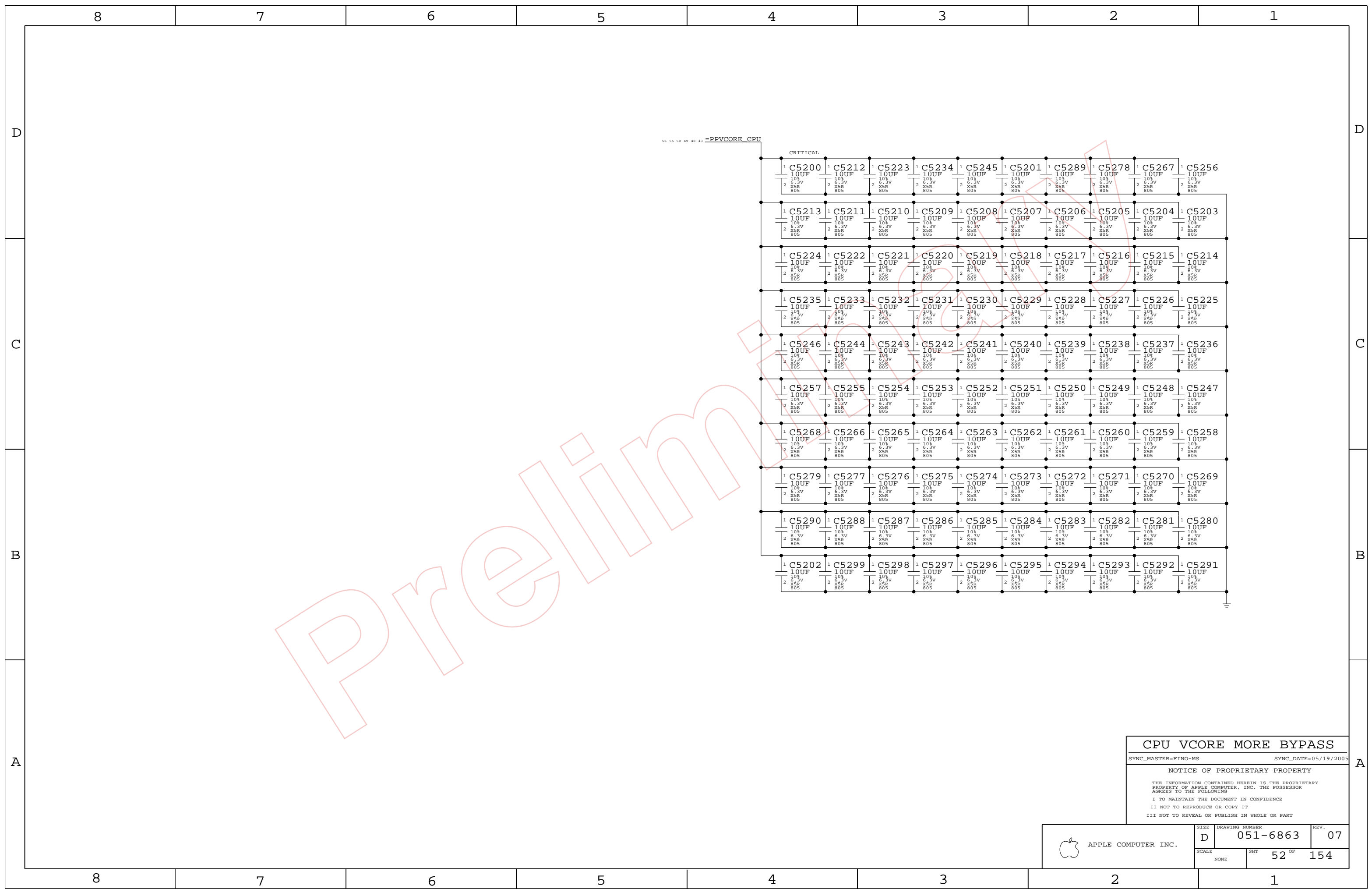
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SIZE	DRAWING NUMBER	REV.
D	051-6863	07

SCALE: NONE SHEET: 50 OF 154





CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

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	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT		OF
NONE	52		154

8

7

6

5

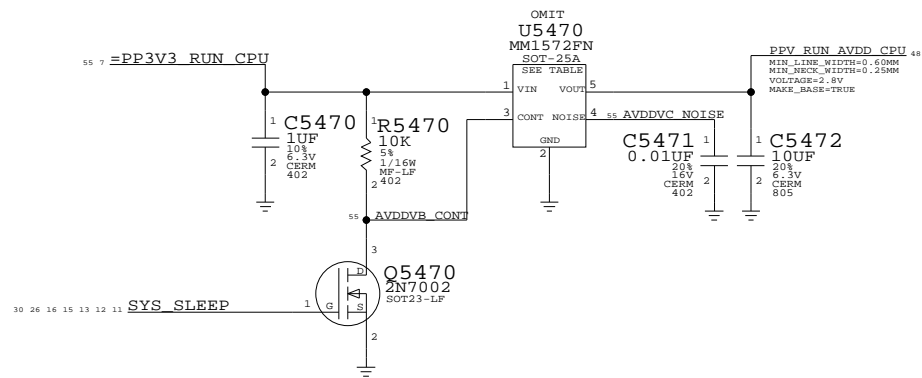
4

3

2

1

PROCESSOR AVDD VREG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0671	1	IIC,MM1572FN,2.5V,150MA,REG,5P SOT-25A	U5470	AVDD_2V5
353S0807	1	IIC,MM1572,2.8V,150MA,REG,5P SOT-25A	U5470	AVDD_2V8



CPU AVDD VREG

SYNC_MASTER=FINO-MS SYNC_DATE=05/19/2005

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	D	051-6863	07
SCALE	SHT	54 OF 154	
NONE			

8

7

6

5

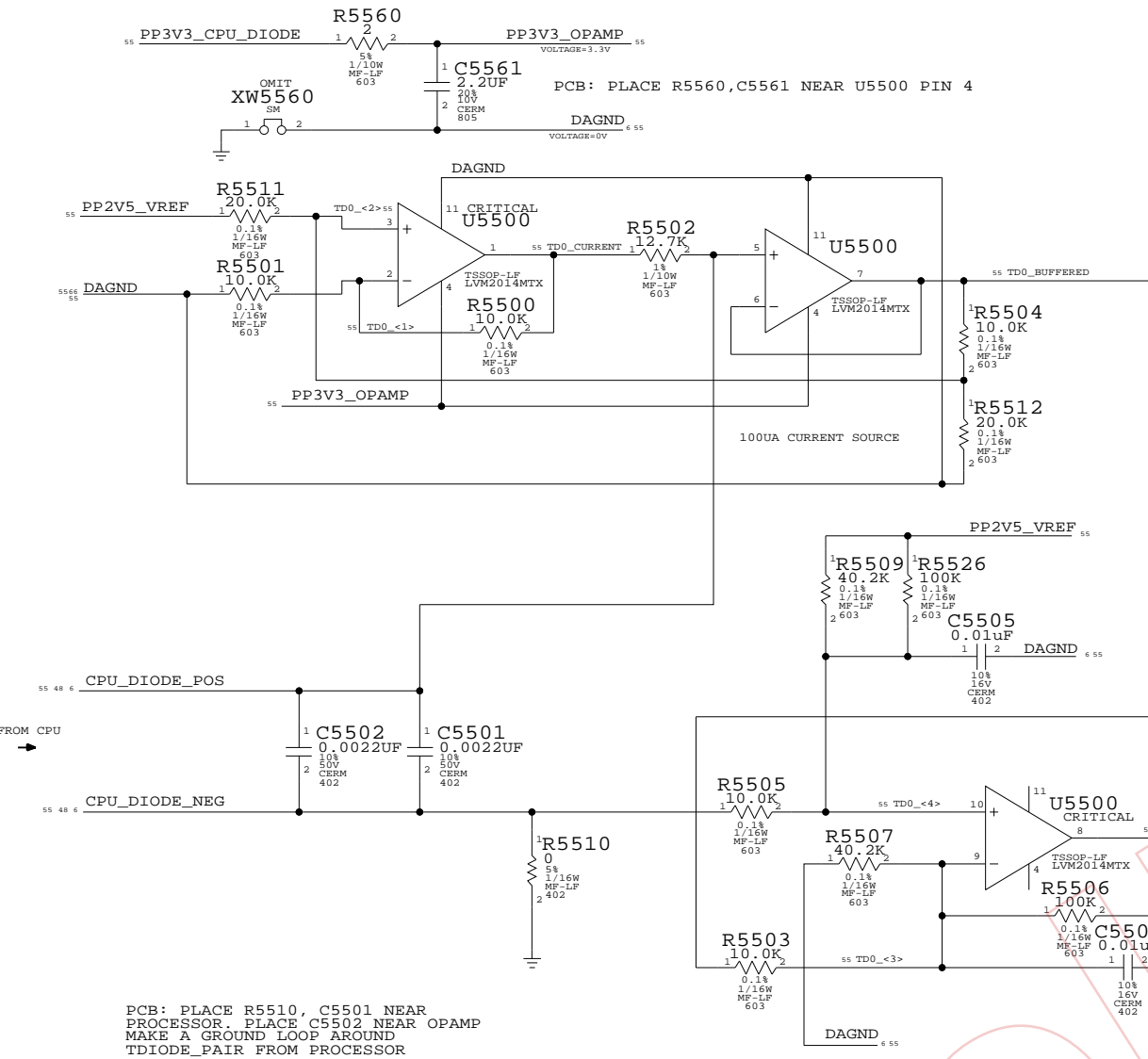
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3

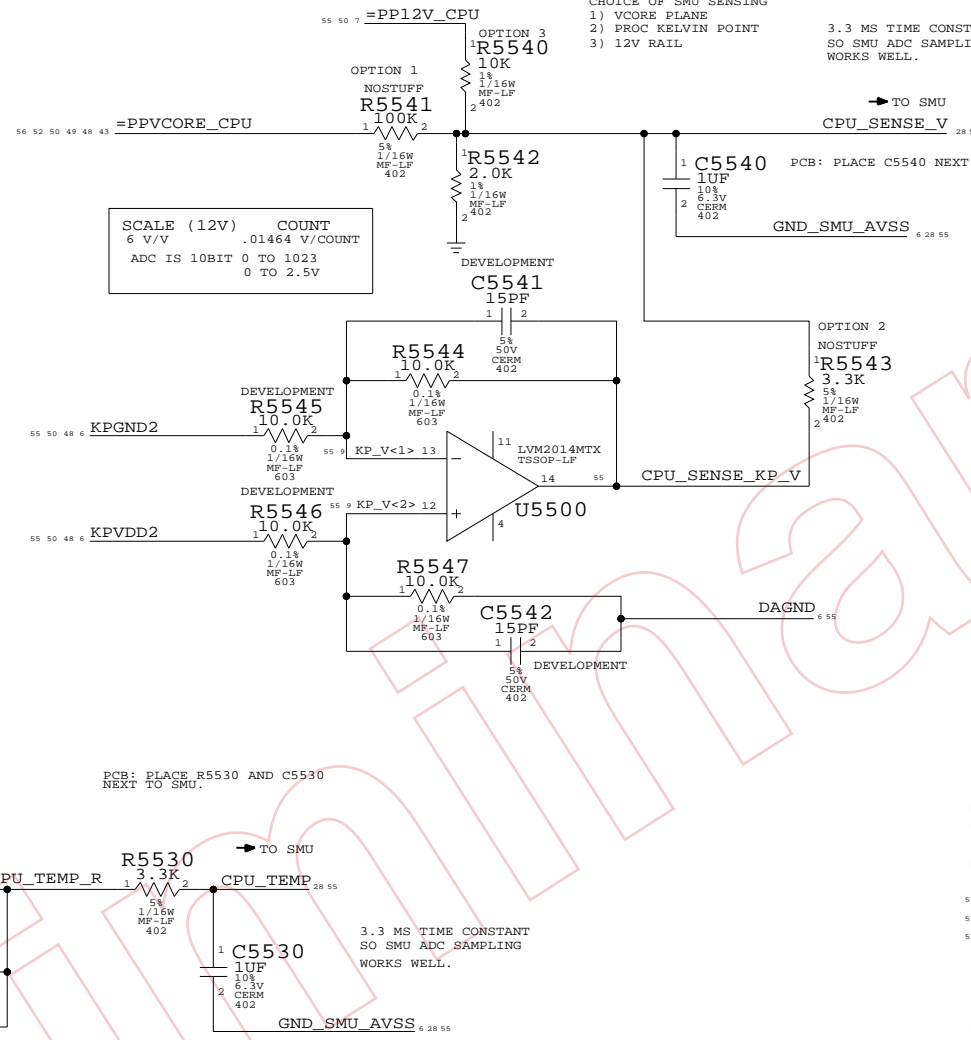
2

1

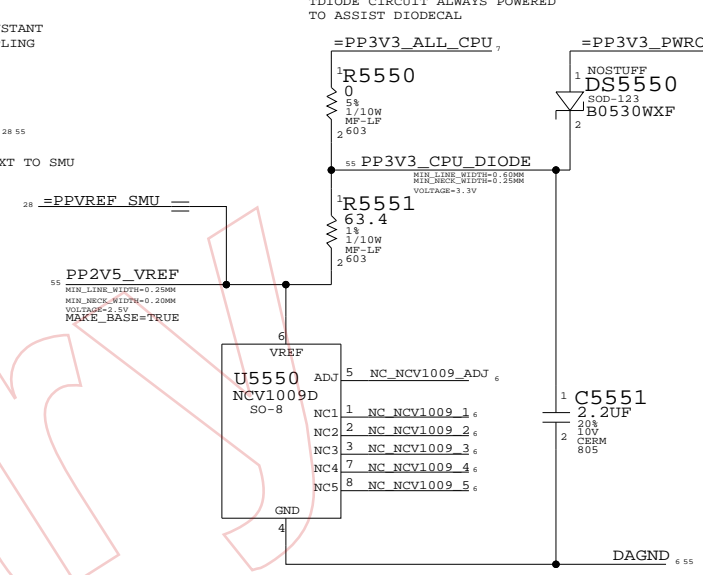
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



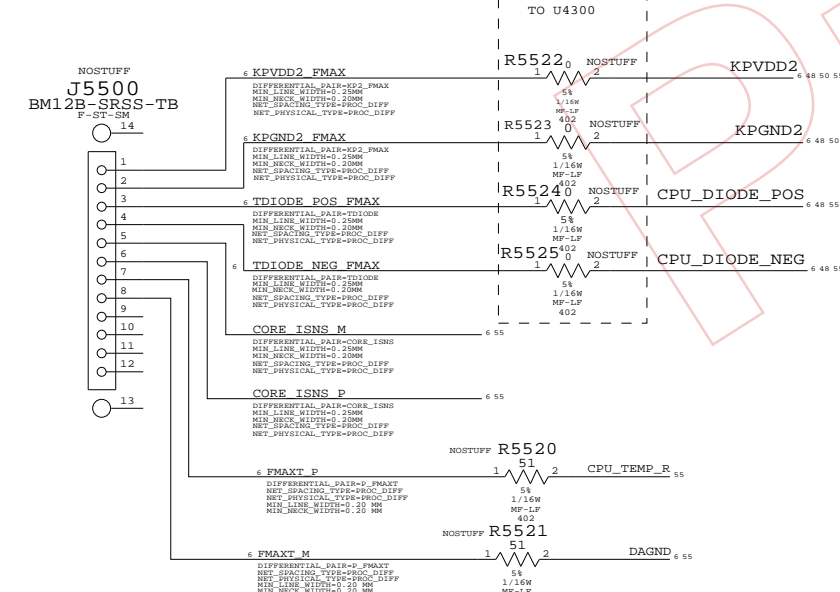
2.5V PRECISION VOLTAGE REFERENCE SOURCE



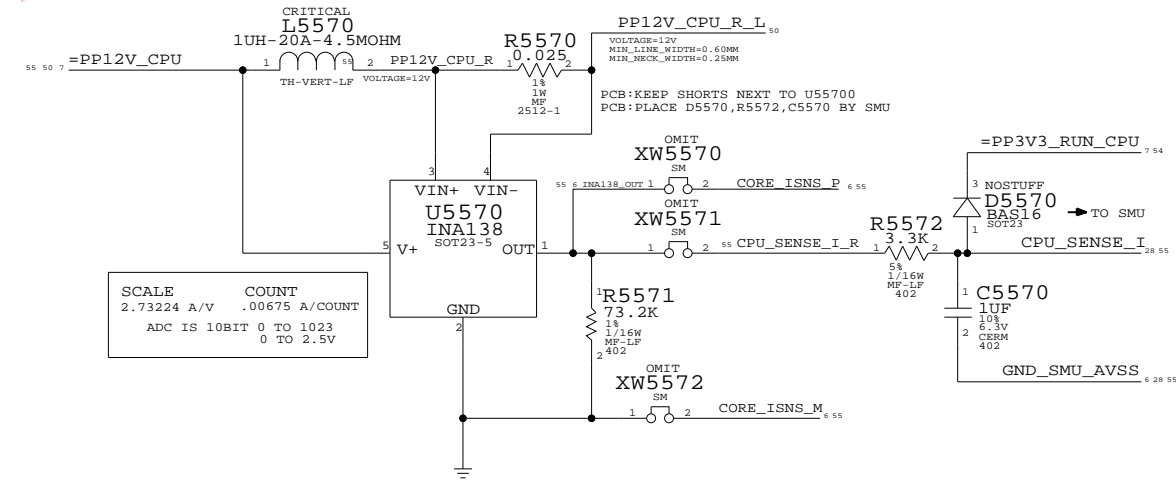
PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE (USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T, V, I SENSORS

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SCALE	SHEET	OF	
NONE	55	154	

CONNECT PULSAR CLKS TO CPU/NB

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for EI_CPU_SYSCLK_P, EI_CPU_SYSCLK_N, EI_CPU_APSYNC, EI_CPU_TREN_CLK, EI_NB_APSYNC.

CONNECT KODIAK EI A TO/FROM CPU

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for EI_NB_TO_CPU_CLK_P, EI_NB_TO_CPU_CLK_N, EI_NB_TO_CPU_AD<0..43>, EI_NB_TO_CPU_SR_P<0..1>, EI_NB_TO_CPU_SR_N<0..1>.

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for EI_CPU_TO_NB_CLK_P, EI_CPU_TO_NB_CLK_N, EI_CPU_TO_NB_AD<0..43>, EI_CPU_TO_NB_SR_P<0..1>, EI_CPU_TO_NB_SR_N<0..1>.

CONNECT CPU TO KODIAK QREQ A0

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes row for CPU_TO_NB_QREQ_L, CPU_A0_TO_NB_QREQ_L.

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for CPU_QACK_L, NC_CPU_A1_QACK_L, NC_CPU_B0_QACK_L, NC_CPU_B1_QACK_L.

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for CPU_INT_L, NC_NB_CPU_A1_INT_L, NC_NB_CPU_B0_INT_L, NC_NB_CPU_B1_INT_L.

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

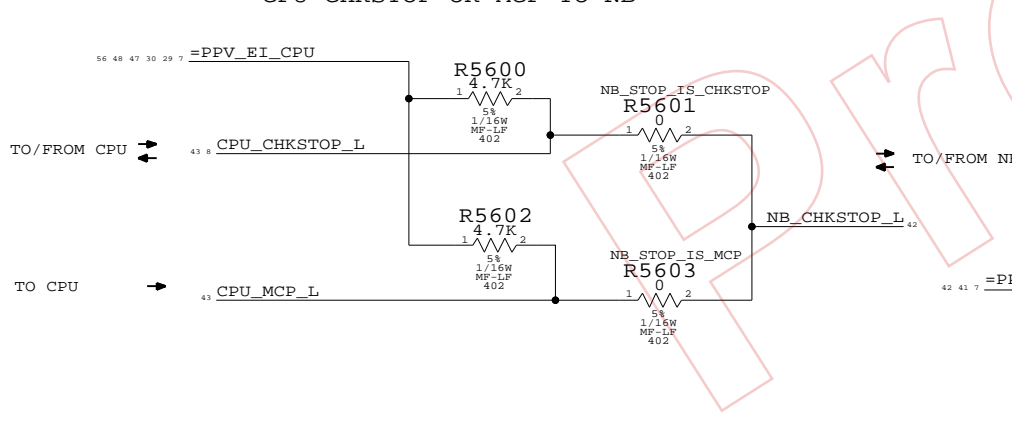
Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for CPU_SRESET_L_R, NOTUSED_CPU_A1_SRESET_L, NOTUSED_CPU_B0_SRESET_L, NOTUSED_CPU_B1_SRESET_L.

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Includes rows for TP_NB_B_TRIGGER_OUT, TP_NB_A_TRIGGER_OUT, TP_CPU_APSYNCOUT, TP_CPU_TRIGGER_IN, TP_CPU_TRIGGER_OUT, NC_PSR0, NC_PSR0_ENABLE, TP_CPU_ATTENTION, NC_CPU_AFN.

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU_CHKSTOP OR MCP TO NB



EI BUS AND SYSCLK CONSTRAINT LABELS

Table with 5 columns: Signal Name, Constraint, Signal Name, Signal Name, Signal Name. Lists various electrical constraints for EI bus and sysclk signals.

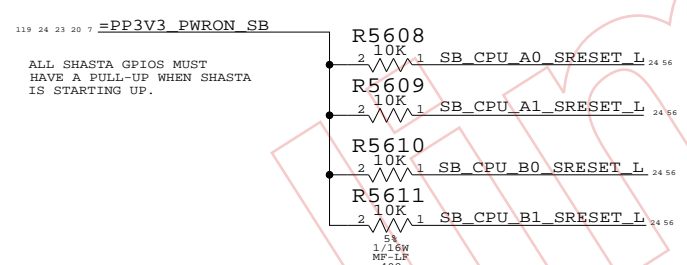
NC KODIAK EI B OUTPUT PORT

Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Lists constraints for NC KODIAK EI B output signals.

NC KODIAK EI B INPUT PORT

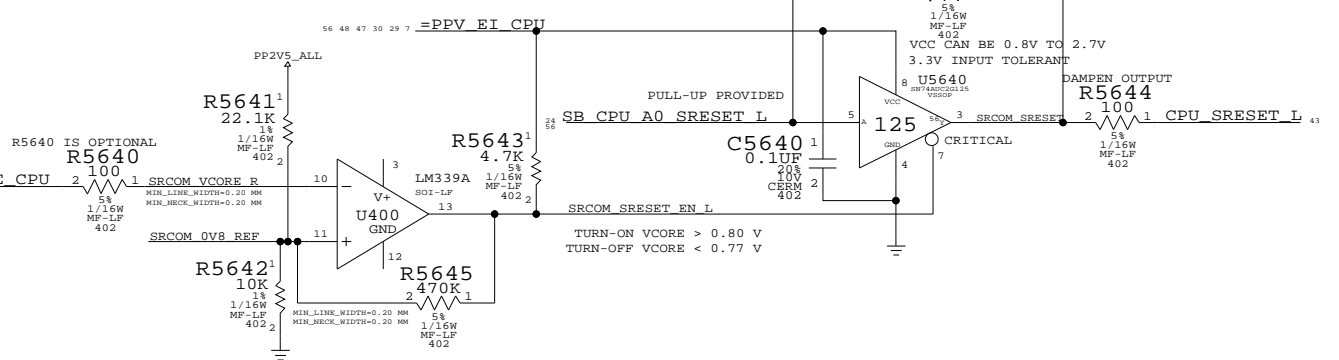
Table with 4 columns: Signal Name, Constraint, Signal Name, Constraint. Lists constraints for NC KODIAK EI B input signals.

PULLUPS FOR SRESET'S FROM SHASTA



SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVOID IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.

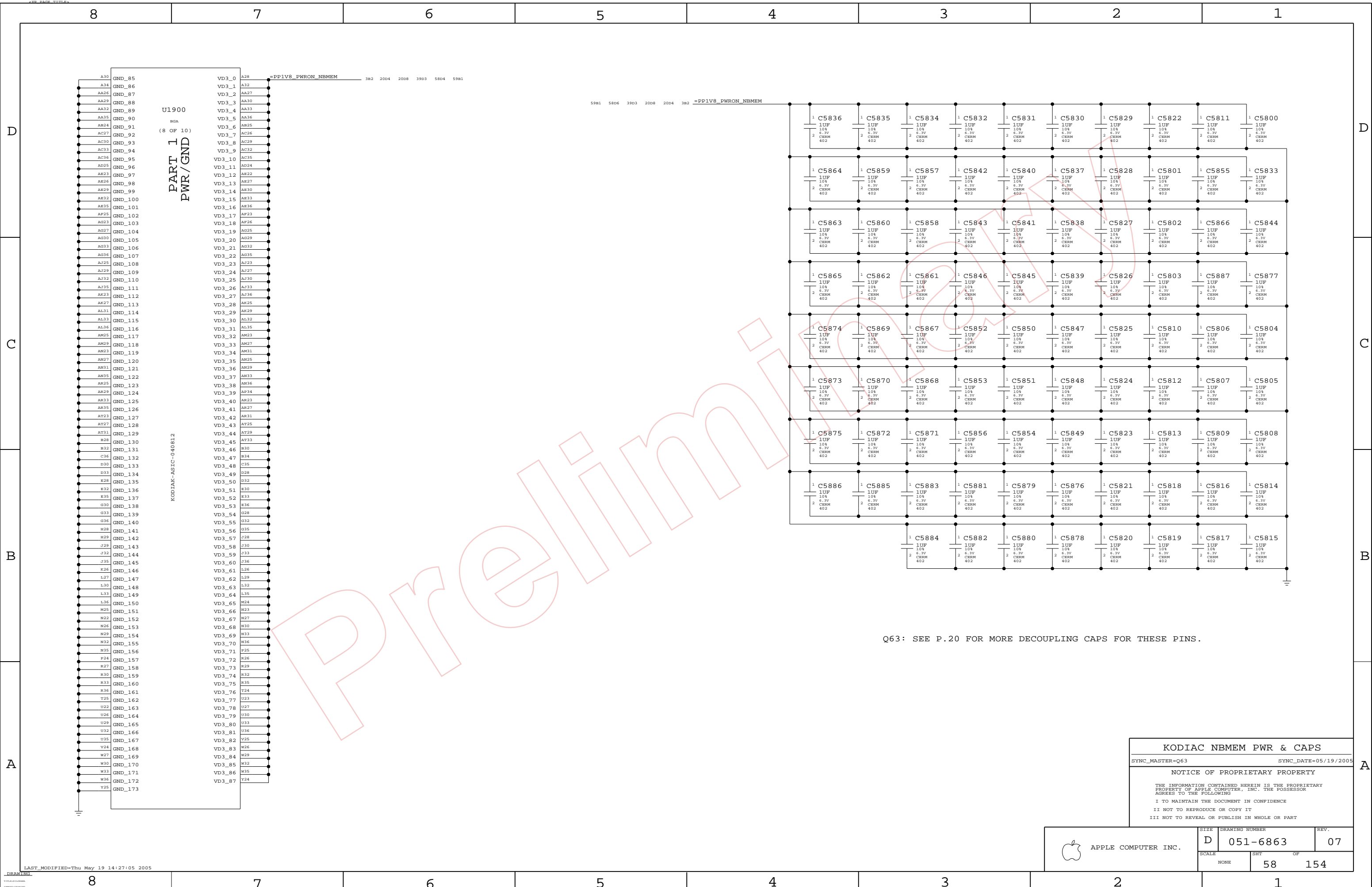


IF SHASTA SHOULD DRIVE OD WITH EI LEVEL PULLUP, STUFF R5612, NOSTUFF R5608, STUFF R5646

NOTE, NB UNUSED INTS DO NOT REQUIRE PULLUPS, ONLY SHASTA (SINCE ITS OUTPUTS ARE TEMPORARILY INPUTS ON BOOTUP). INT PULLUP IS SO INT PIN IS NOT FLOATING TO PROCESSOR BUT WEAK TO ALLOW KODIAK TO DRIVE PUSH-PULL STRONGLY

CPU ALIASES & MISC. SYNC_MASTER=FINO-MS, SYNC_DATE=05/19/2005. NOTICE OF PROPRIETARY PROPERTY. THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE, II NOT TO REPRODUCE OR COPY IT, III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART.

Apple Computer Inc. Drawing Number: D 051-6863 07. Scale: NONE. Sheet: 56 OF 154.



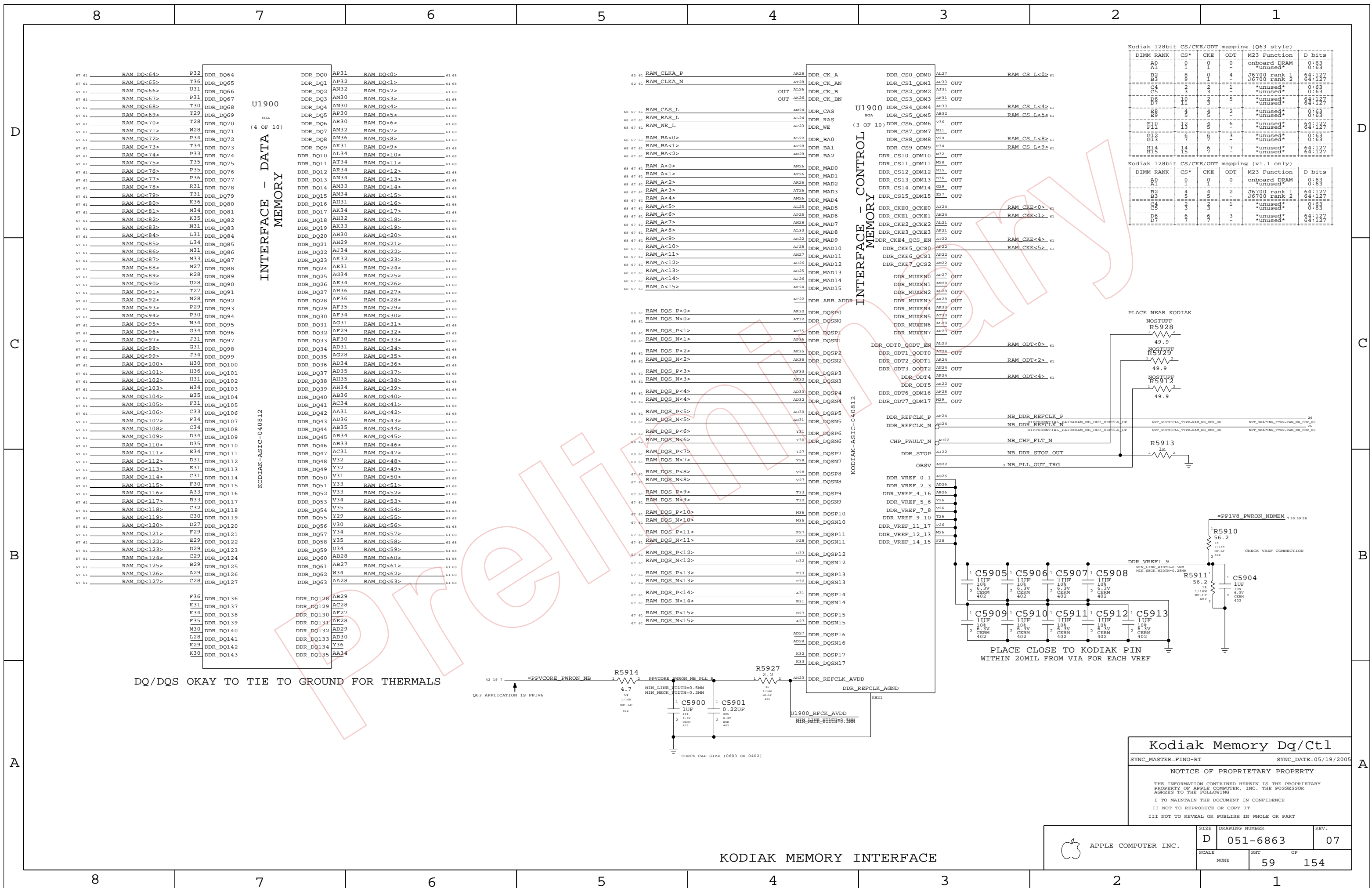
U1900
 (8 OF 10)
 PWR/GND

KODIAC-NBEM-040812

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBEM PWR & CAPS
 SYNC_MASTER=Q63 SYNC_DATE=05/19/2005
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SCALE	NONE	SHT	OF
		58	154



U1900
BGA
(4 OF 10)
INTERFACE - DATA MEMORY

U1900
BGA
(3 OF 10)
INTERFACE - CONTROL MEMORY

Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	1	0	onboard DRAM	0:63
A1	1	1	0	onboard DRAM	0:63
B2	8	0	4	U6700 rank 1	64:127
B3	9	1	4	U6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	2	1	*unused*	0:63
D6	10	3	3	*unused*	64:127
D7	11	3	3	*unused*	64:127
E8	5	5	5	*unused*	0:63
E9	6	5	5	*unused*	0:63
F10	13	4	6	*unused*	64:127
F11	14	4	6	*unused*	64:127
G12	7	7	3	*unused*	0:63
G13	8	7	3	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	6	7	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	0	onboard DRAM	0:63
B2	4	4	2	U6700 rank 1	64:127
B3	5	5	2	U6700 rank 2	64:127
C4	3	3	1	*unused*	0:63
C5	2	2	1	*unused*	0:63
D6	10	6	7	*unused*	64:127
D7	7	7	3	*unused*	64:127

DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

PLACE CLOSE TO KODIAK PIN WITHIN 20MIL FROM VIA FOR EACH VREF

Kodiak Memory Dq/Ctl

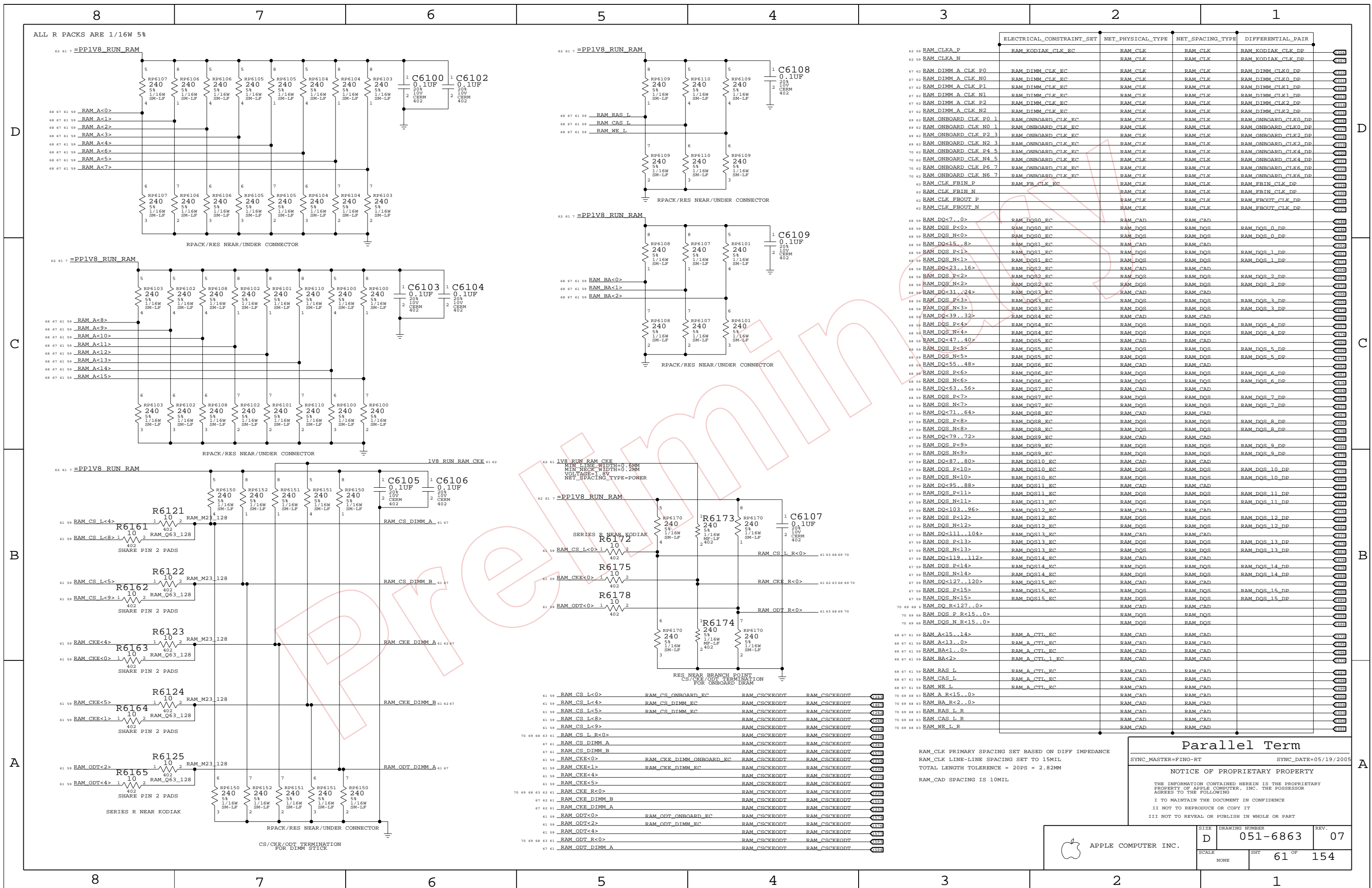
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SCALE	SHEET	OF	
NONE	59	154	

KODIAK MEMORY INTERFACE

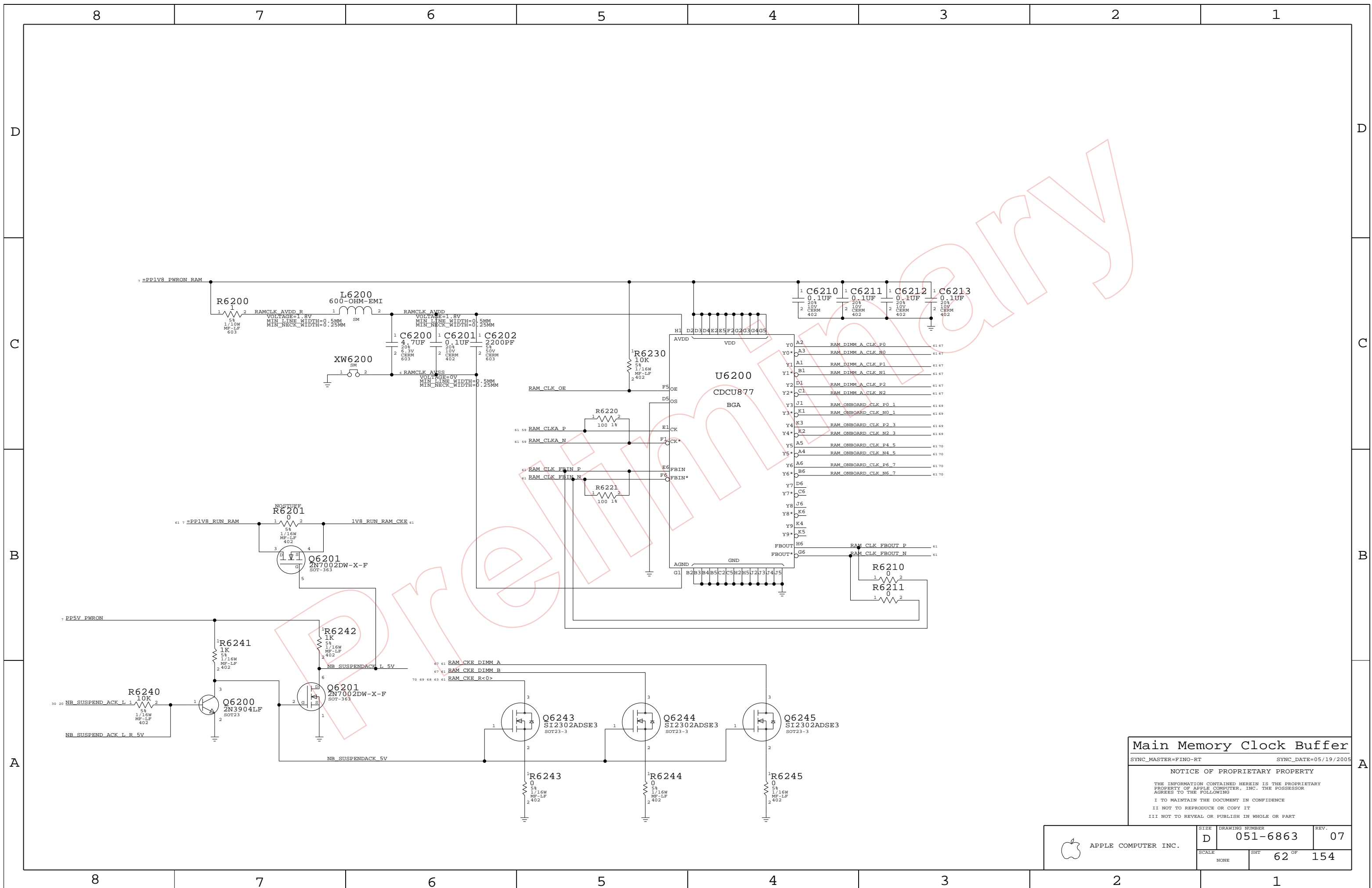


ALL R PACKS ARE 1/16W 5%

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
RAM_CLKA_P	RAM_CLK	RAM_CLK	RAM_CLK
RAM_CLKA_N	RAM_CLK	RAM_CLK	RAM_CLK
RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK0_DP
RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK0_DP
RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK1_DP
RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK1_DP
RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK2_DP
RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_DIMM_CLK_EC	RAM_DIMM_CLK2_DP
RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK0_DP
RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK0_DP
RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK2_DP
RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK2_DP
RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK4_DP
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RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK6_DP
RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK_EC	RAM_ONBOARD_CLK6_DP
RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBIN_CLK_DP
RAM_CLK_FBIN_N	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBIN_CLK_DP
RAM_CLK_FBOUT_P	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBOUT_CLK_DP
RAM_CLK_FBOUT_N	RAM_FB_CLK_EC	RAM_FB_CLK_EC	RAM_FBOUT_CLK_DP
RAM_DS0<7..0>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<0>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<0>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<15..8>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<1>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<1>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<23..16>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<2>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<2>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<31..24>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<3>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<3>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<39..32>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
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RAM_DS0<47..40>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
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RAM_DS0<55..48>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
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RAM_DS0<63..56>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<7>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<7>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<71..64>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<8>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<8>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<79..72>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<9>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<9>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<87..80>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<10>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<10>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<95..88>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<11>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<11>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<103..96>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<12>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<12>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<111..104>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<13>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<13>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<119..112>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<14>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<14>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<127..120>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P<15>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0_N<15>	RAM_DS0_EC	RAM_DS0	RAM_DS0_DP
RAM_DS0<127..0>	RAM_DS0_EC	RAM_CAD	RAM_DS0_DP
RAM_DS0_P_R<15..0>	RAM_DS0	RAM_DS0	RAM_DS0_DP
RAM_DS0_N_R<15..0>	RAM_DS0	RAM_DS0	RAM_DS0_DP
RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_A_CTL_DP
RAM_BAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_A_CTL_DP
RAM_A_R<15..0>	RAM_CAD	RAM_CAD	RAM_CAD
RAM_BA_R<2..0>	RAM_CAD	RAM_CAD	RAM_CAD
RAM_RAS_L_R	RAM_CAD	RAM_CAD	RAM_CAD
RAM_CAS_L_R	RAM_CAD	RAM_CAD	RAM_CAD
RAM_WE_L_R	RAM_CAD	RAM_CAD	RAM_CAD

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
 RAM_CLK LINE-LINE SPACING SET TO 15MIL
 TOTAL LENGTH TOLERANCE = 20PS = 2.82MM
 RAM_CAD SPACING IS 10MIL

Parallel Term
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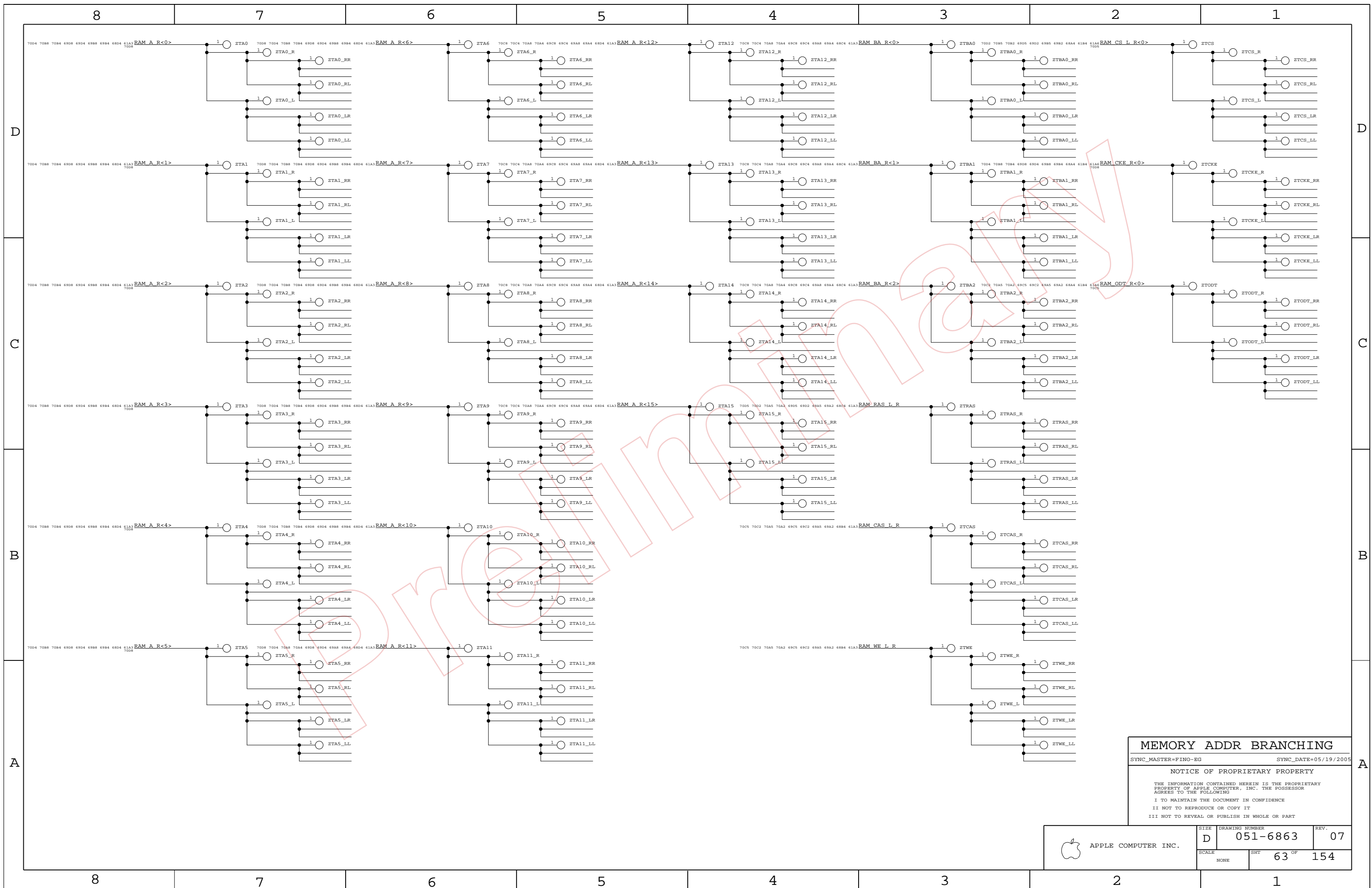
Main Memory Clock Buffer

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	SCALE NONE	SHEET 62 OF	TOTAL SHEETS 154




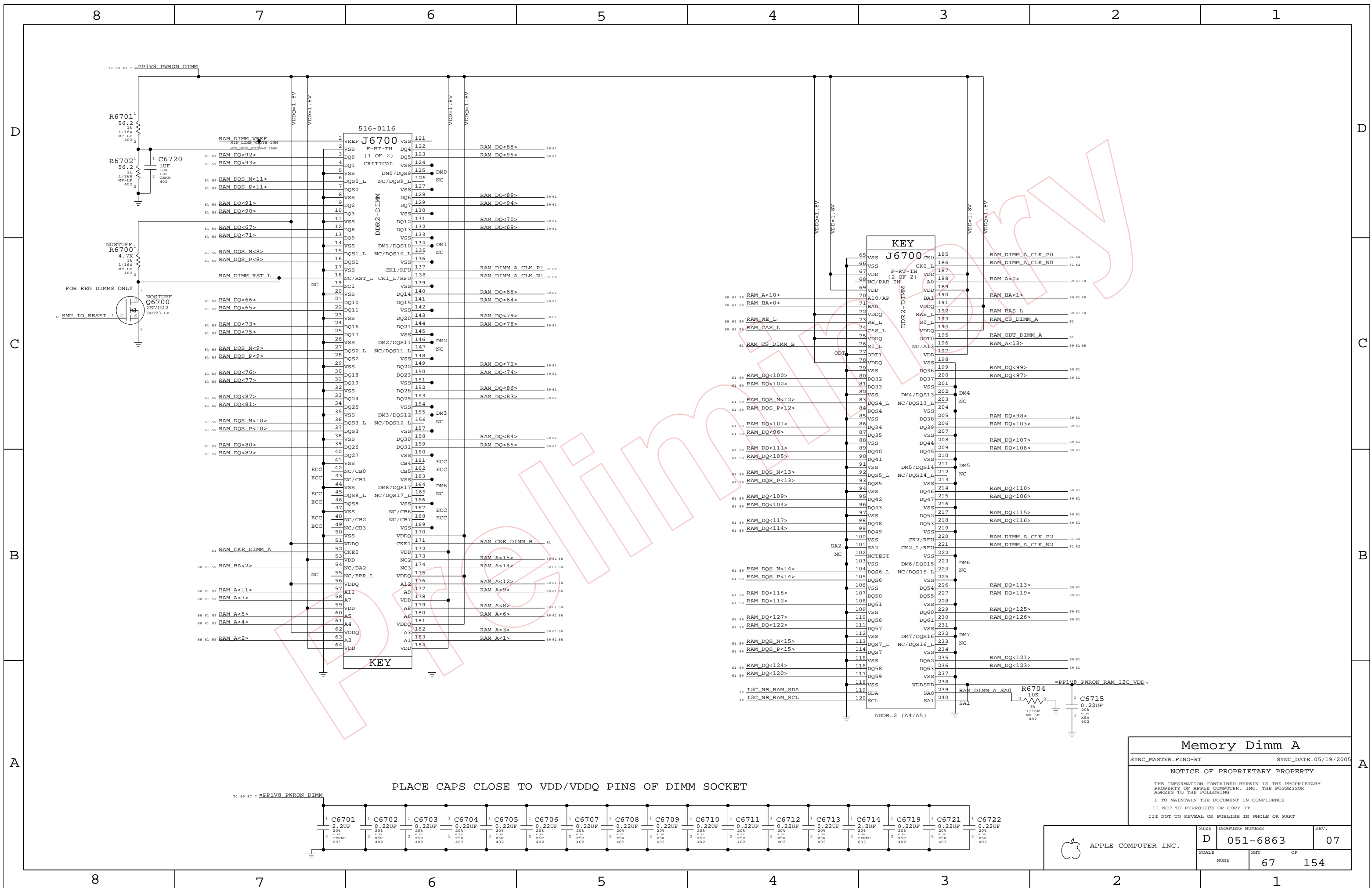
MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT	63 OF 154	
NONE			



PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET

1	C6701	2.2UF	20%	CSRM1	609	2	C6702	0.22UF	20%	X5R	402	3	C6703	0.22UF	20%	X5R	402	4	C6704	0.22UF	20%	X5R	402	5	C6705	0.22UF	20%	X5R	402	6	C6706	0.22UF	20%	X5R	402	7	C6707	0.22UF	20%	X5R	402	8	C6708	0.22UF	20%	X5R	402	9	C6709	0.22UF	20%	X5R	402	10	C6710	0.22UF	20%	X5R	402	11	C6711	0.22UF	20%	X5R	402	12	C6712	0.22UF	20%	X5R	402	13	C6713	0.22UF	20%	X5R	402	14	C6714	2.2UF	20%	CSRM1	609	15	C6719	0.22UF	20%	X5R	402	16	C6721	0.22UF	20%	X5R	402	17	C6722	0.22UF	20%	X5R	402
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KEY

65	VSS	185	RAM_DIMM_A_CLK_P0	61 62
66	CK0_L	186	RAM_DIMM_A_CLK_N0	61 62
67	F-RT-TH VDD	187		
68	NC/PAR_IN A0	188	RAM_A<0>	59 61 68
69	VDD	189		
70	VDD	190	RAM_BA<1>	59 61 68
71	BA1	191		
72	VDDQ	192	RAM_RAS_L	59 61 68
73	RAS_L	193	RAM_CS_DIMM_A	61
74	SO_L	194		
75	VDDQ	195	RAM_ODT_DIMM_A	61
76	ODT0	196	RAM_A<13>	59 61 68
77	NC/A13	197		
78	VDD	198		
79	VDDQ	199	RAM_DQ<99>	59 61
80	DQ32	200	RAM_DQ<97>	59 61
81	DQ33	201		
82	VSS	202	DM4	DM4
83	DQS4_L	203	NC	NC
84	DQS4	204		
85	VSS	205	RAM_DQ<98>	59 61
86	DQ34	206	RAM_DQ<103>	59 61
87	DQ35	207		
88	VSS	208	RAM_DQ<107>	59 61
89	DQ40	209	RAM_DQ<108>	59 61
90	DQ41	210		
91	VSS	211	DM5	DM5
92	DM5/DQS14	212	NC	NC
93	NC/DQS14_L	213		
94	DQS5	214		
95	VSS	215	RAM_DQ<110>	59 61
96	DQ42	216	RAM_DQ<106>	59 61
97	DQ43	217		
98	VSS	218	RAM_DQ<115>	59 61
99	DQ52	219	RAM_DQ<116>	59 61
100	DQ53	220		
101	VSS	221	RAM_DIMM_A_CLK_P2	61 62
102	CK2_L/RFU	222	RAM_DIMM_A_CLK_N2	61 62
103	NC	223		
104	VSS	224	DM6	DM6
105	DM6/DQS15	225	NC	NC
106	NC/DQS15_L	226		
107	DQS6	227		
108	VSS	228	RAM_DQ<113>	59 61
109	DQ54	229	RAM_DQ<119>	59 61
110	DQ55	230		
111	VSS	231	RAM_DQ<125>	59 61
112	DQ60	232	RAM_DQ<126>	59 61
113	DQ61	233		
114	VSS	234	DM7	DM7
115	DM7/DQS16	235	NC	NC
116	NC/DQS16_L	236		
117	DQS7	237		
118	VSS	238	RAM_DQ<121>	59 61
119	DQ62	239	RAM_DQ<123>	59 61
120	DQ63	240		
121	VSS	241		
122	DQ59	242		
123	VSS	243		
124	VDDSPD	244		
125	SA0	245	RAM_DIMM_A_SA0	
126	SA1	246		
127	SA1	247		

Memory Dimm A

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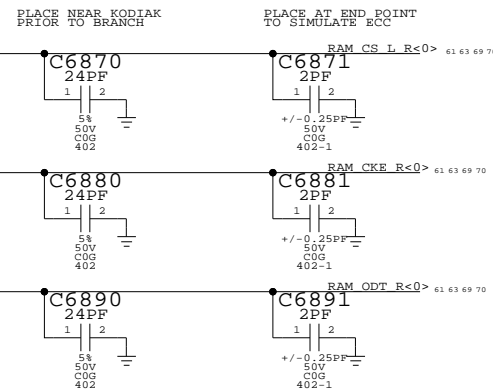
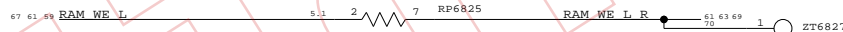
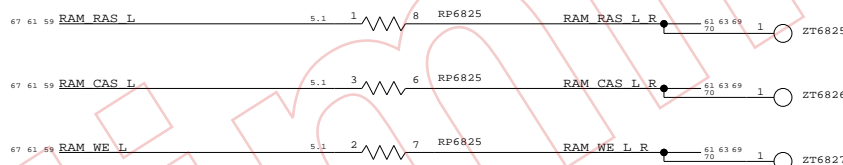
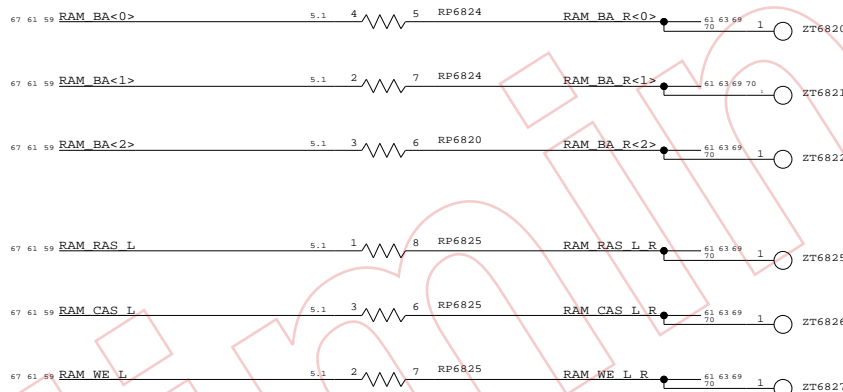
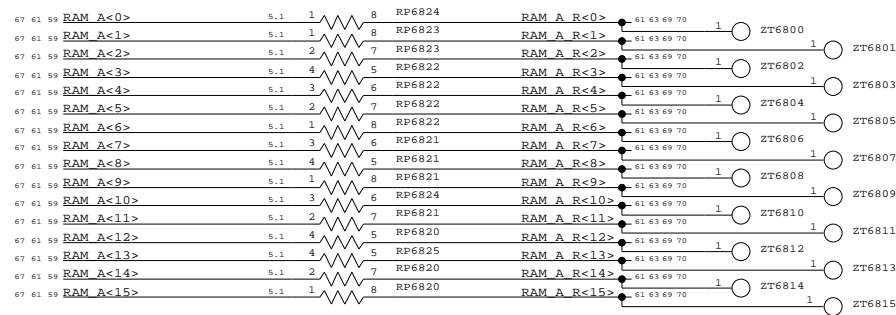
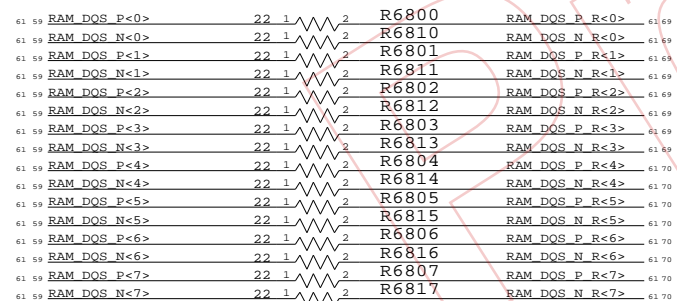
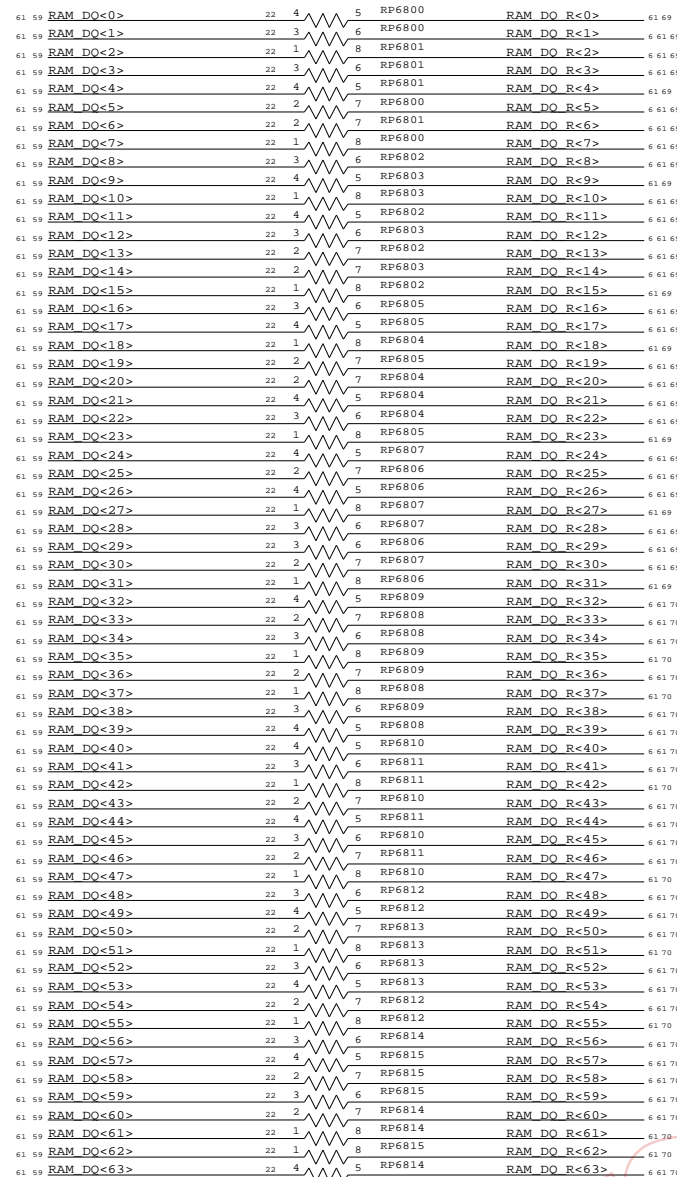
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SCALE	SHT	OF	
NONE	67	154	

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A



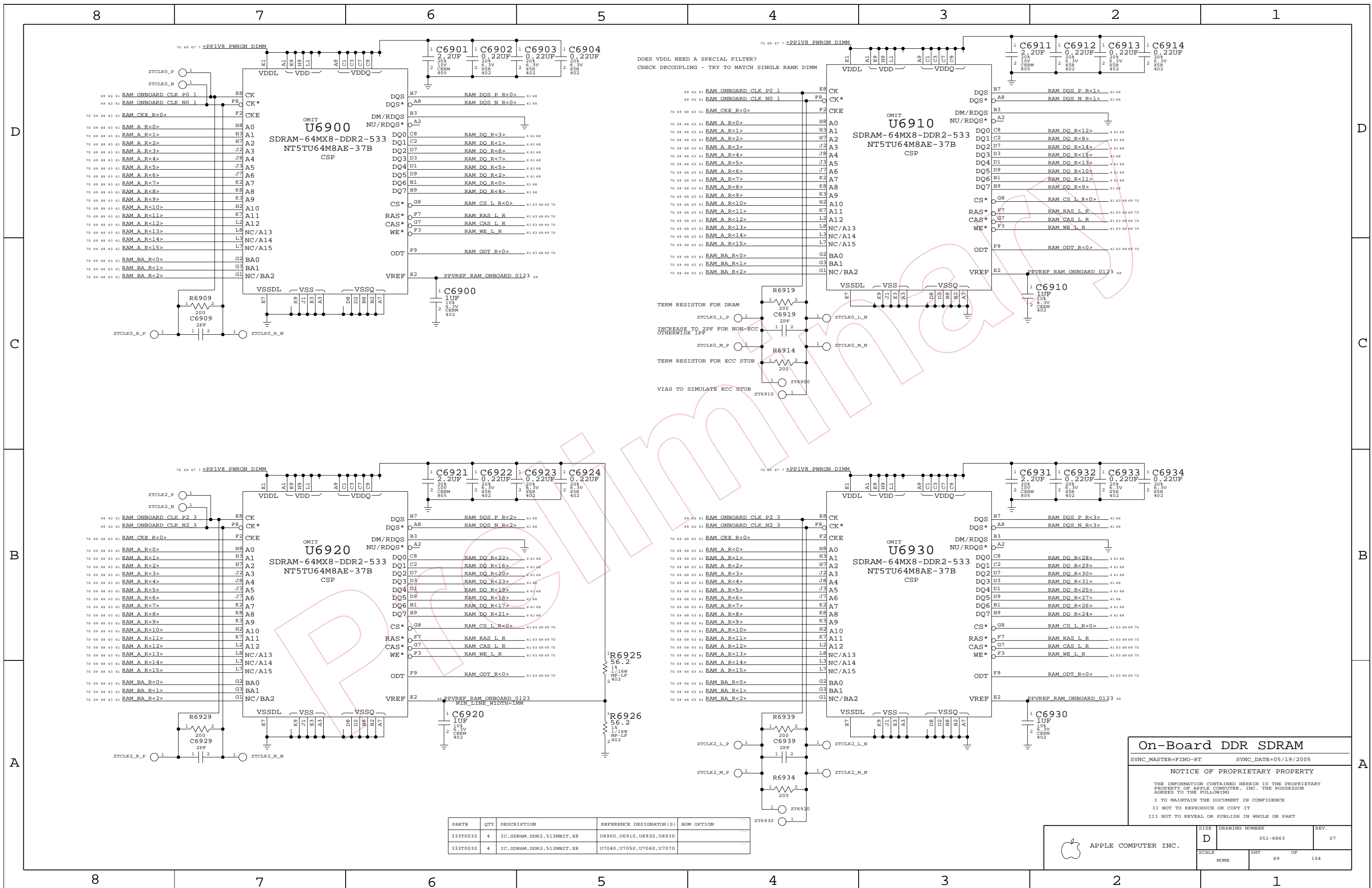
MLB Mem Series Term

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NONE	68	154	



DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM

On-Board DDR SDRAM

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U6900, U6910, U6920, U6930	
333T0032	4	IC, SDRAM, DDR2, 512MBIT, X8	U7040, U7050, U7060, U7070	

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6863	REV. 07
	SCALE NONE	SHEET 69	OF 154



DOES VDDL NEED A SPECIAL FILTER?
CHECK DECOUPLING - TRY TO MATCH SINGLE RANK DIMM

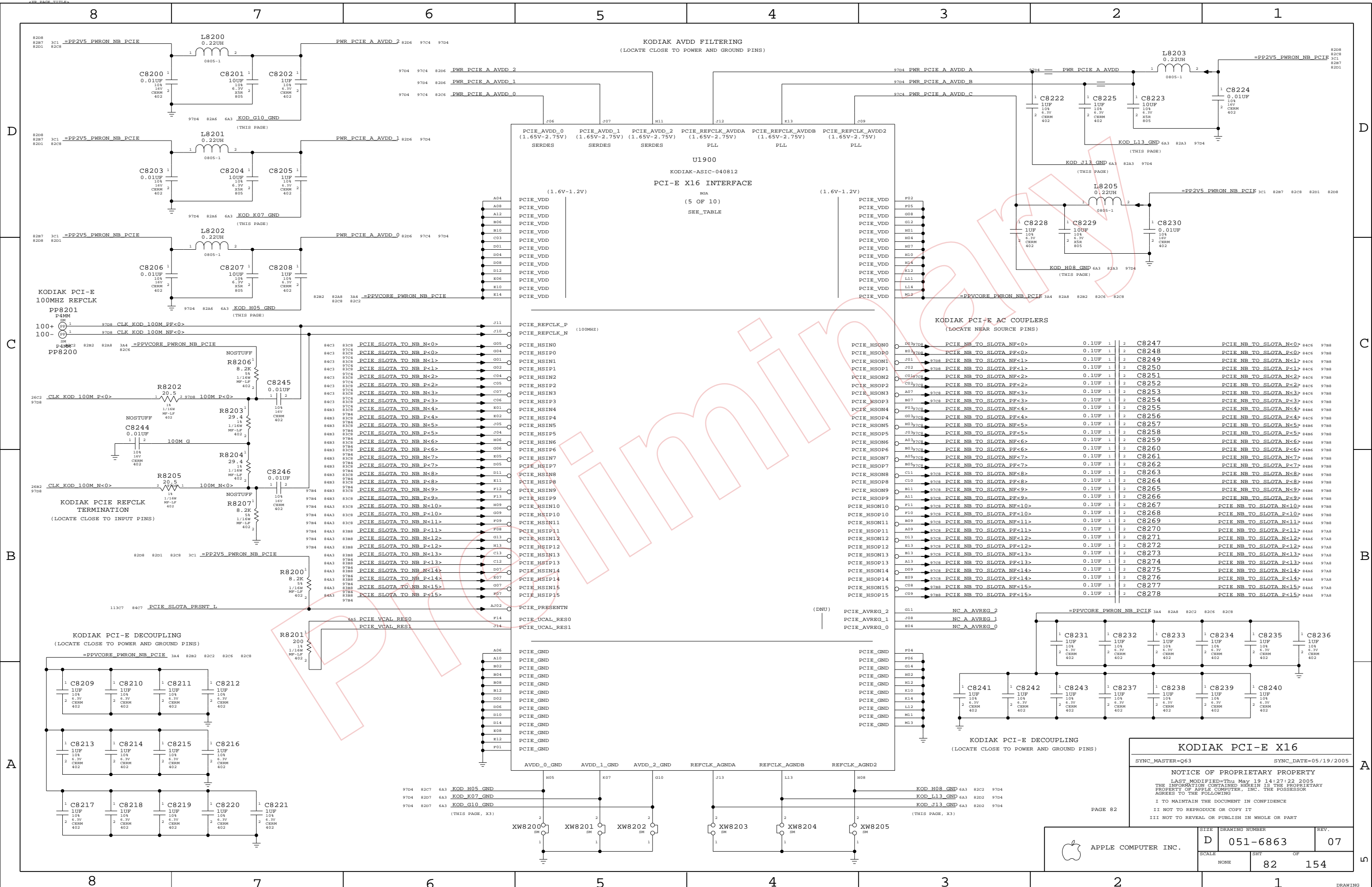
On-Board DDR SDRAM

SYNC_MASTER=FINO-RT SYNC_DATE=05/19/2005

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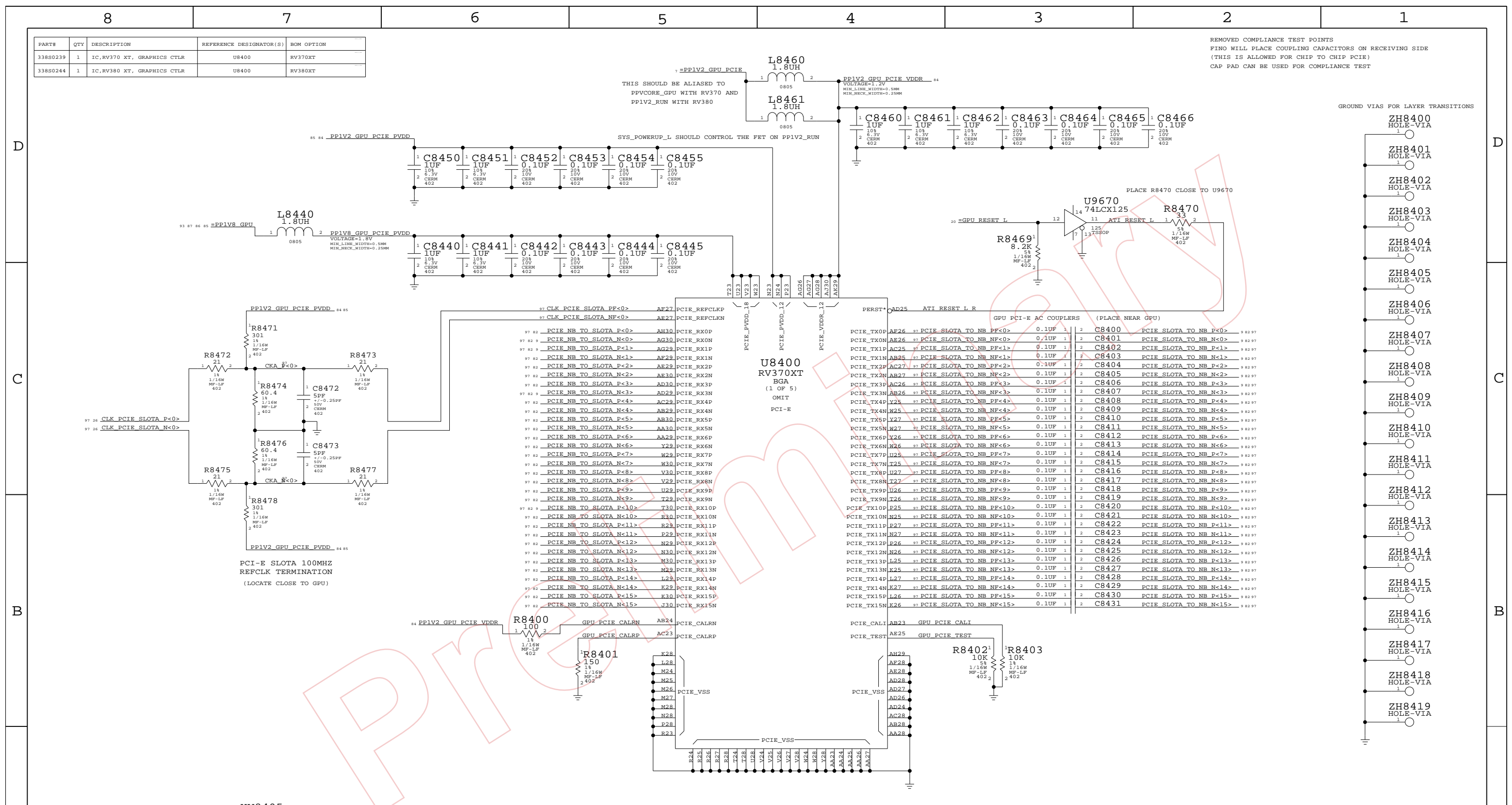
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	NONE	D 051-6863	07
SHEET 70 OF 154			



KODIAK PCI-E X16
 SYNC_MASTER=Q63 SYNC_DATE=05/19/2005
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
33880239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT
33880244	1	IC,RV380 XT, GRAPHICS CTLR	U8400	RV380XT

REMOVED COMPLIANCE TEST POINTS
 FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
 (THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
 CAP PAD CAN BE USED FOR COMPLIANCE TEST



GPU PCIe	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	NONE	SHT	OF
		84	154

A

A

D

D

C

C

B

B

8

7

6

5

4

3

2

1

8

7

6

5

4

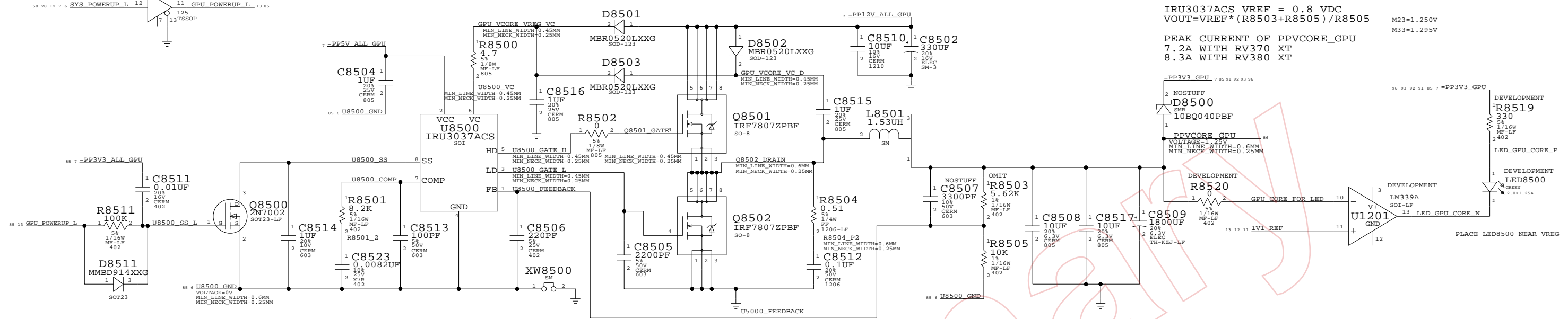
3

2

1

GPU VCORE VREG

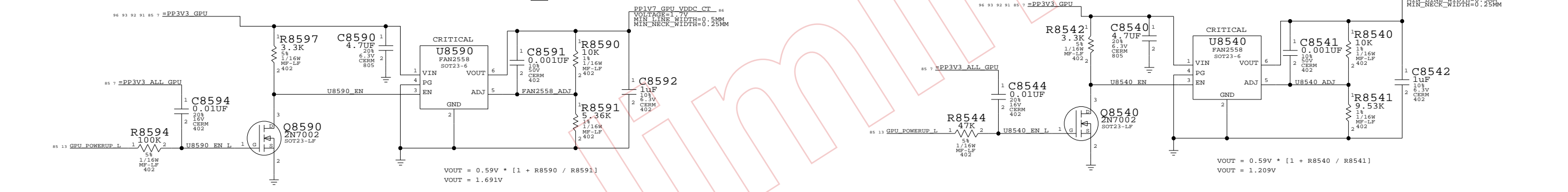
NOTE:
 SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
 1.30V +/- 2% FOR RV380 XT
 IRU3037ACS VREF = 0.8 VDC
 VOUT=VREF*(R8503+R8505)/R8505 M23=1.250V
 M33=1.295V
 PEAK CURRENT OF PPVCORE_GPU
 7.2A WITH RV370 XT
 8.3A WITH RV380 XT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11450291	1	RES, 5.62K OHM, 1/16W, 1%, 0402	R8503	RV370XT
11450295	1	RES, 6.19K OHM, 1/16W, 1%, 0402	R8503	RV380XT

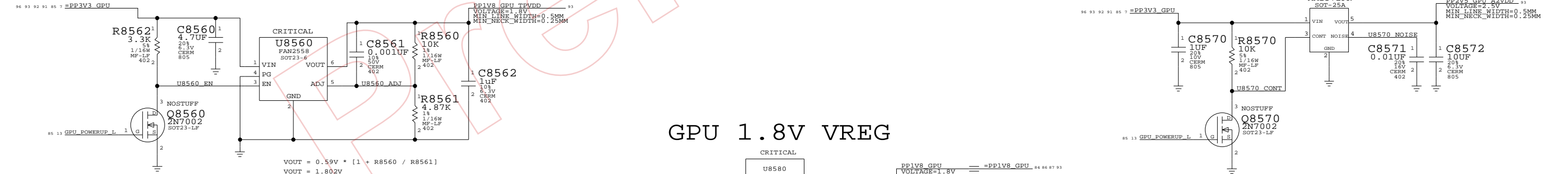
GPU 1.7V VDDC_CT

GPU 1.20V PCIE PVDD

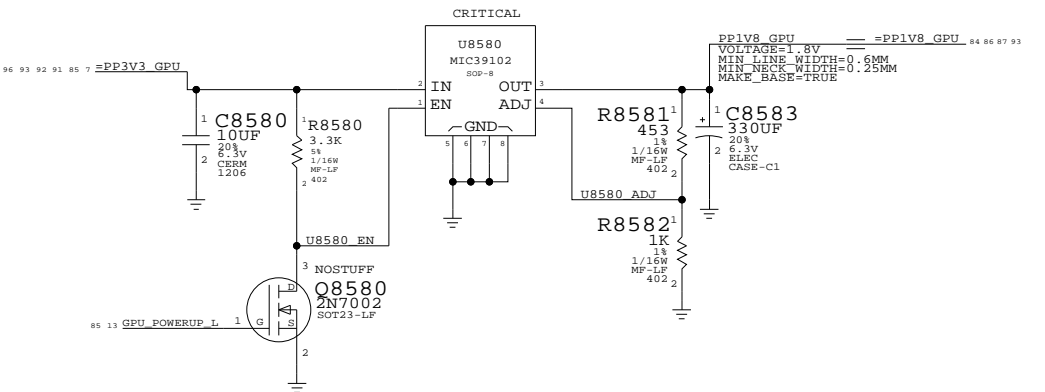


GPU 1.80V TPVDD

GPU 2.5V A2VDD



GPU 1.8V VREG



Graphics Vregs

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

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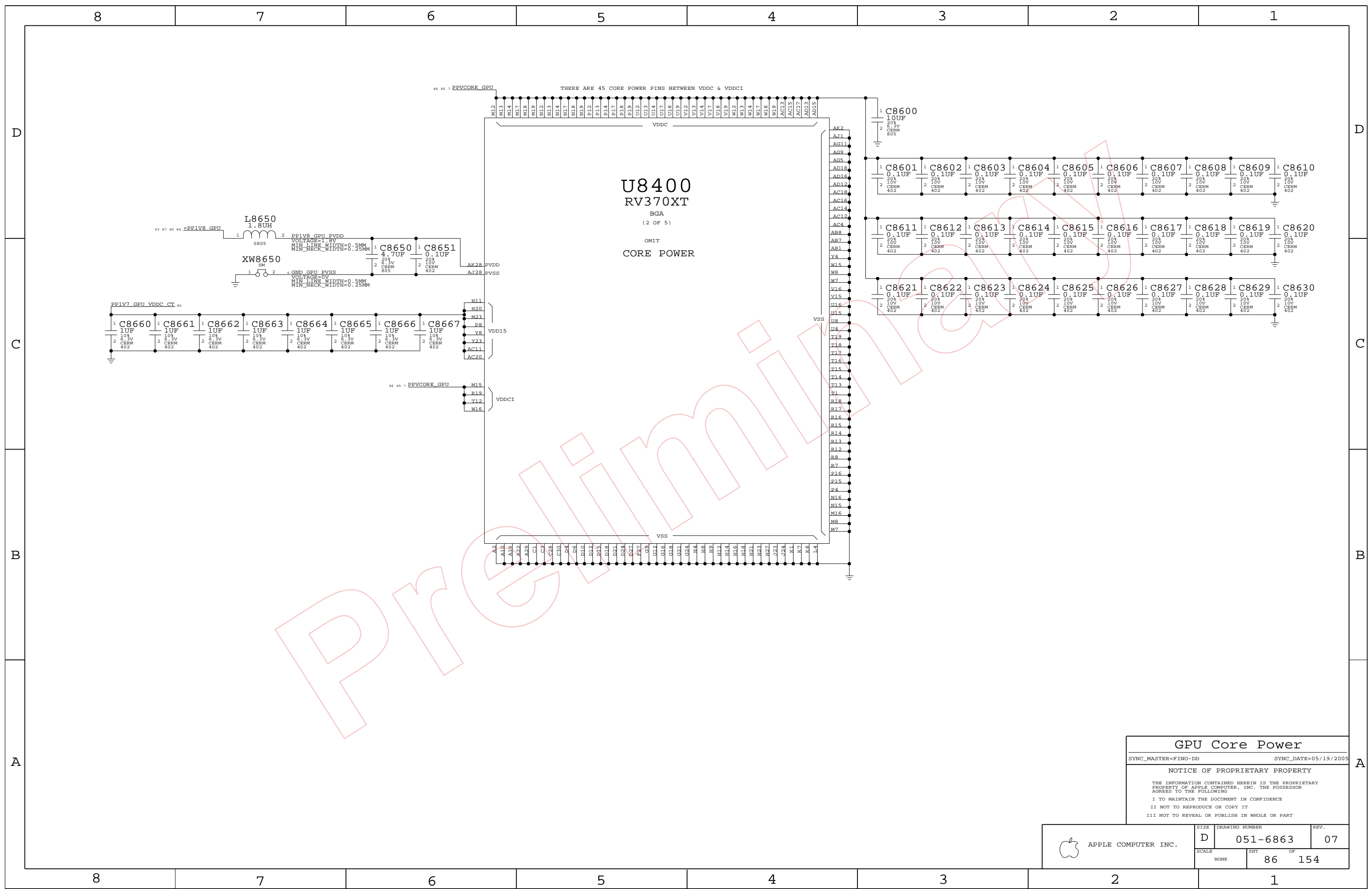
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POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
 PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
 HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
 POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

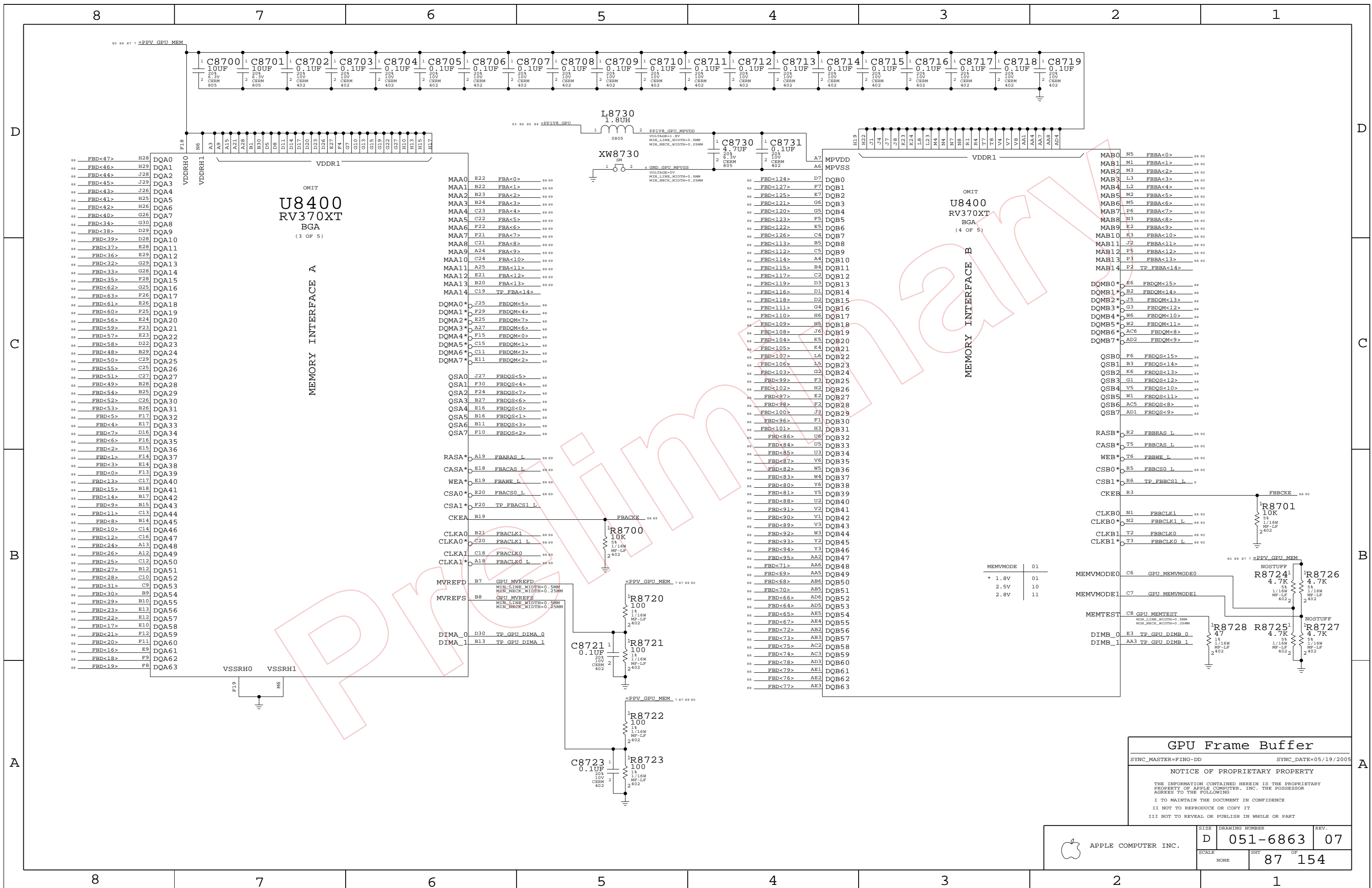
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	NONE	SHT	OF
		85	154



U8400
RV370XT
BGA
(2 OF 5)
OMIT
CORE POWER

GPU Core Power
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	D	051-6863	07
SCALE	SHT OF		
NONE	86 OF		154



OMIT
U8400
 RV370XT
 BGA
 (3 OF 5)

OMIT
U8400
 RV370XT
 BGA
 (4 OF 5)

MEMORY INTERFACE A

MEMORY INTERFACE B

MEMVMODE	01
* 1.8V	01
2.5V	10
2.8V	11

GPU Frame Buffer
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APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	87 OF 154	07

FRAME BUFFER A TERMINATION

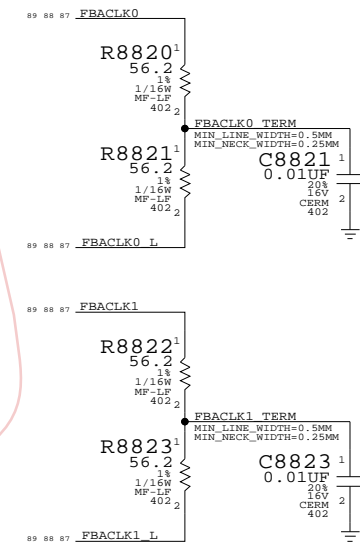
PLACE R'S CLOSE TO MEMORY

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

Table listing termination points for Frame Buffer A, including signals like FBD<31>, FBD<30>, FBD<29>, FBD<28>, FBD<27>, FBD<26>, FBD<25>, FBD<24>, FBD<0>, FBD<1>, FBD<2>, FBD<3>, FBD<17>, FBD<16>, FBD<18>, FBD<19>, FBD<15>, FBD<14>, FBD<13>, FBD<12>, FBD<10>, FBD<11>, FBD<9>, FBD<8>, FBD<5>, FBD<6>, FBD<4>, FBD<7>, FBD<20>, FBD<21>, FBD<22>, FBD<23>.

Table listing termination points for Frame Buffer A, including signals like FBD<32>, FBD<33>, FBD<34>, FBD<35>, FBD<36>, FBD<37>, FBD<38>, FBD<39>, FBD<40>, FBD<41>, FBD<42>, FBD<43>, FBD<44>, FBD<45>, FBD<46>, FBD<47>, FBD<48>, FBD<49>, FBD<50>, FBD<51>, FBD<52>, FBD<53>, FBD<54>, FBD<55>, FBD<56>, FBD<57>, FBD<58>, FBD<59>, FBD<60>, FBD<61>, FBD<62>, FBD<63>.

Table listing termination points for Frame Buffer A, including signals like FBDQS<0>, FBDQS<1>, FBDQS<2>, FBDQS<3>, FBDQS<4>, FBDQS<5>, FBDQS<6>, FBDQS<7>, FBDQM<0>, FBDQM<1>, FBDQM<2>, FBDQM<3>, FBDQM<4>, FBDQM<5>, FBDQM<6>, FBDQM<7>.



FRAME BUFFER B TERMINATION

Table listing termination points for Frame Buffer B, including signals like FBD<64>, FBD<65>, FBD<66>, FBD<67>, FBD<84>, FBD<85>, FBD<86>, FBD<87>, FBD<72>, FBD<73>, FBD<75>, FBD<74>, FBD<68>, FBD<70>, FBD<69>, FBD<71>, FBD<80>, FBD<81>, FBD<82>, FBD<83>, FBD<76>, FBD<77>, FBD<78>, FBD<79>, FBD<91>, FBD<90>, FBD<89>, FBD<88>, FBD<95>, FBD<94>, FBD<93>, FBD<92>.

Table listing termination points for Frame Buffer B, including signals like FBD<96>, FBD<97>, FBD<98>, FBD<99>, FBD<100>, FBD<101>, FBD<102>, FBD<103>, FBD<104>, FBD<105>, FBD<106>, FBD<107>, FBD<108>, FBD<109>, FBD<110>, FBD<111>, FBD<112>, FBD<113>, FBD<114>, FBD<115>, FBD<116>, FBD<117>, FBD<118>, FBD<119>, FBD<120>, FBD<121>, FBD<122>, FBD<123>, FBD<124>, FBD<125>, FBD<126>, FBD<127>.

Table listing termination points for Frame Buffer B, including signals like FBDQS<8>, FBDQS<9>, FBDQS<10>, FBDQS<11>, FBDQS<12>, FBDQS<13>, FBDQS<14>, FBDQS<15>, FBDQM<8>, FBDQM<9>, FBDQM<10>, FBDQM<11>, FBDQM<12>, FBDQM<13>, FBDQM<14>, FBDQM<15>.

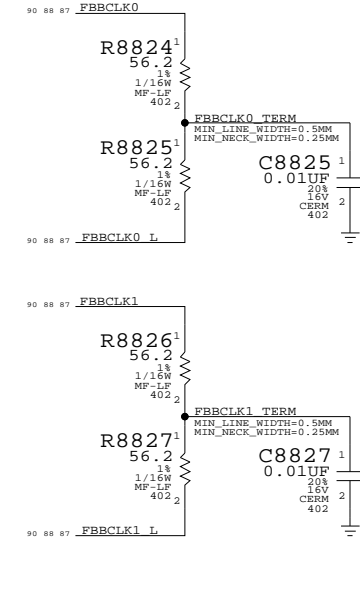
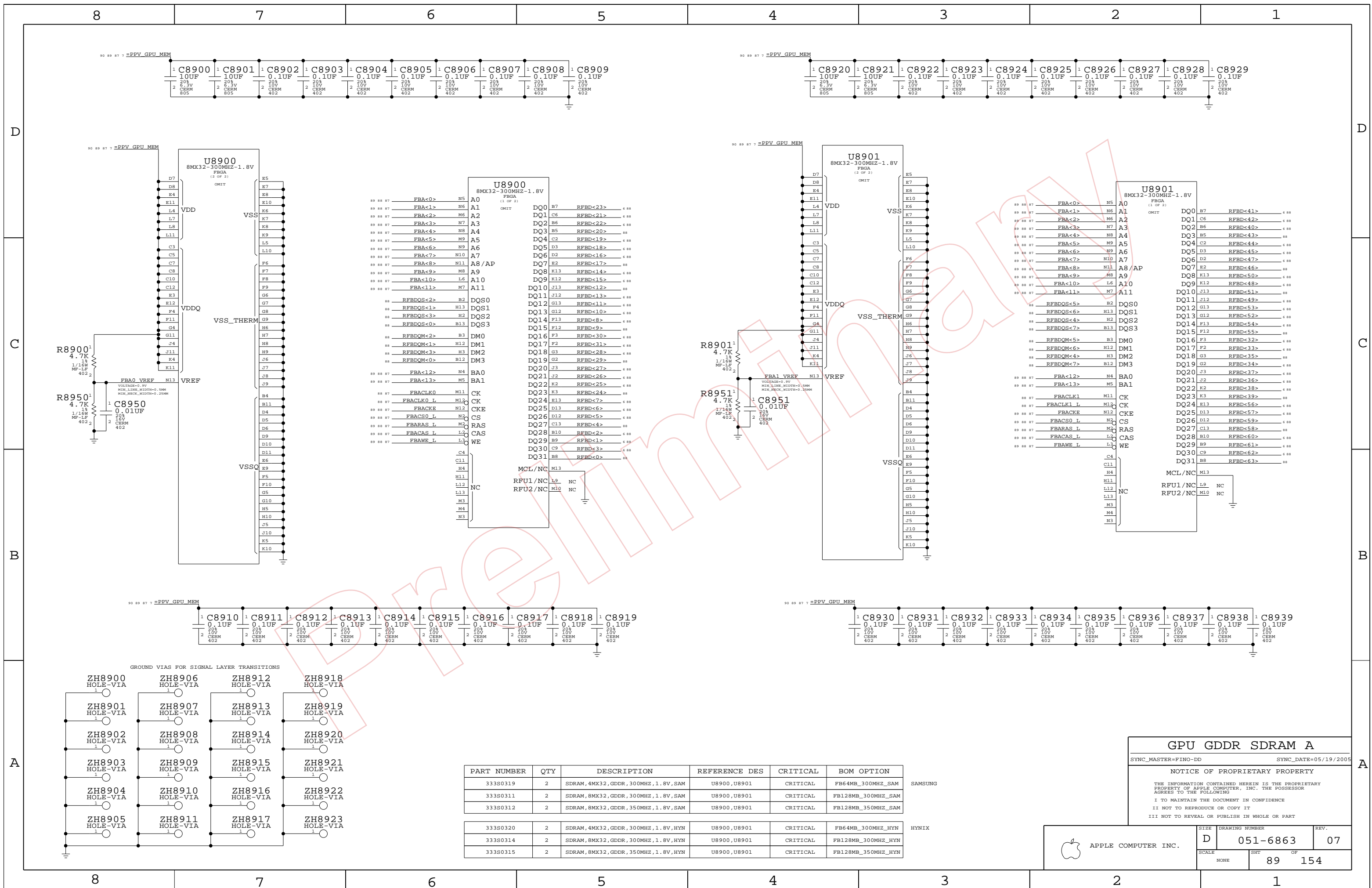


Table with columns: ELECTRICAL_CONSTRAINT_SET, NET_PHYSICAL_TYPE, NET_SPACING_TYPE, DIFFERENTIAL_PAIR. Lists various net names and their constraints.

Table with columns: ELECTRICAL_CONSTRAINT_SET, NET_PHYSICAL_TYPE, NET_SPACING_TYPE, DIFFERENTIAL_PAIR. Lists various net names and their constraints.

FB Series Termination
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DRAWING NUMBER: 051-6863
REV: 07
SCALE: NONE
SHEET: 88 OF 154

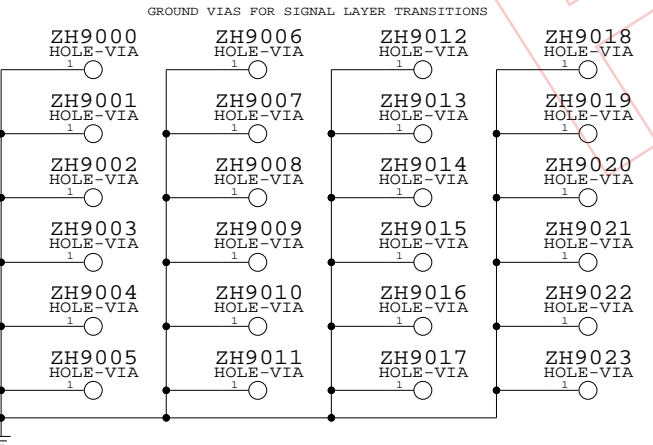
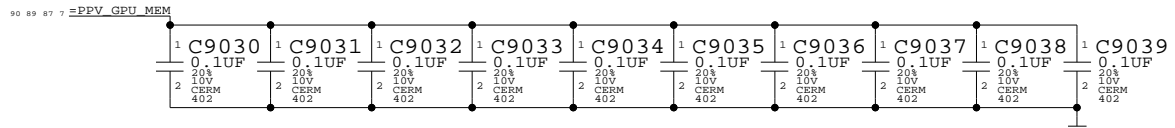
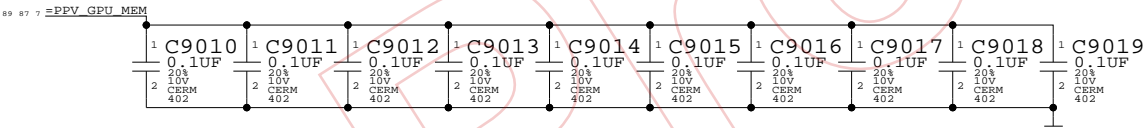
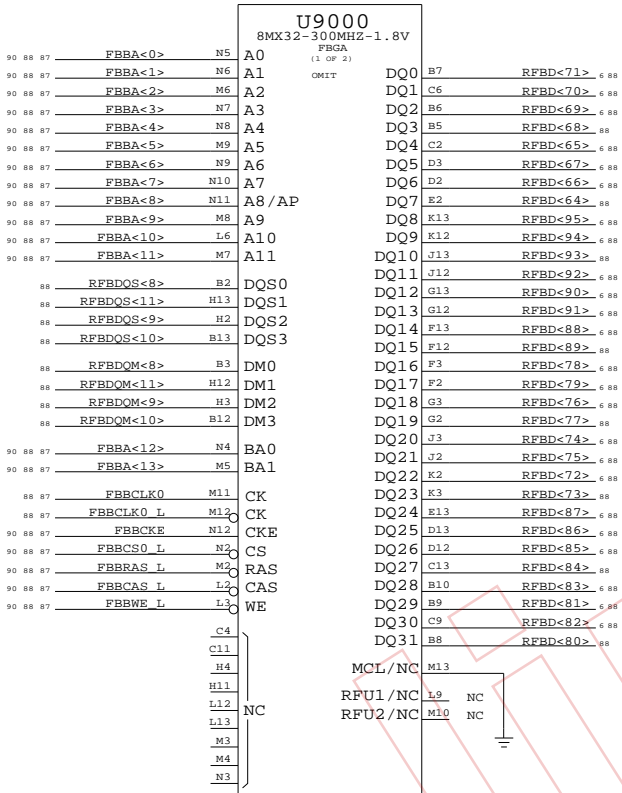
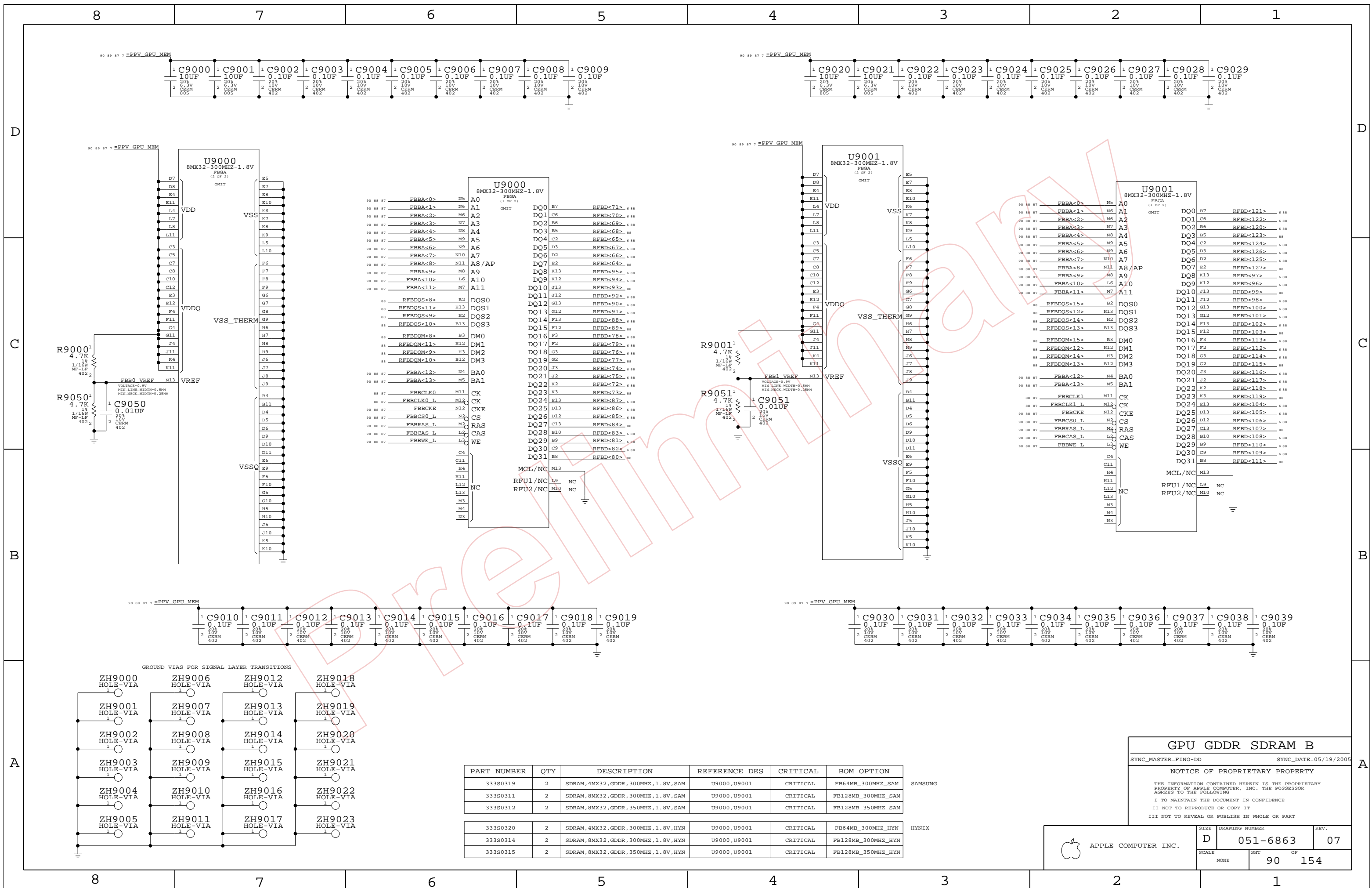


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB64MB_300MHZ_SAM
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_300MHZ_SAM
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U8900, U8901	CRITICAL	FB128MB_350MHZ_SAM
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB64MB_300MHZ_HYN
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_300MHZ_HYN
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U8900, U8901	CRITICAL	FB128MB_350MHZ_HYN

GPU GDDR SDRAM A
 SYNC_MASTER=FINO-DD SYNC_DATE=05/19/2005
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE	SHT	OF
NONE	89	154



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0319	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB64MB_300MHZ_SAM SAMSUNG
333S0311	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB128MB_300MHZ_SAM SAMSUNG
333S0312	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, SAM	U9000, U9001	CRITICAL	FB128MB_350MHZ_SAM SAMSUNG
333S0320	2	SDRAM, 4MX32, GDDR, 300MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB64MB_300MHZ_HYN HYNIX
333S0314	2	SDRAM, 8MX32, GDDR, 300MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB128MB_300MHZ_HYN HYNIX
333S0315	2	SDRAM, 8MX32, GDDR, 350MHZ, 1.8V, HYN	U9000, U9001	CRITICAL	FB128MB_350MHZ_HYN HYNIX

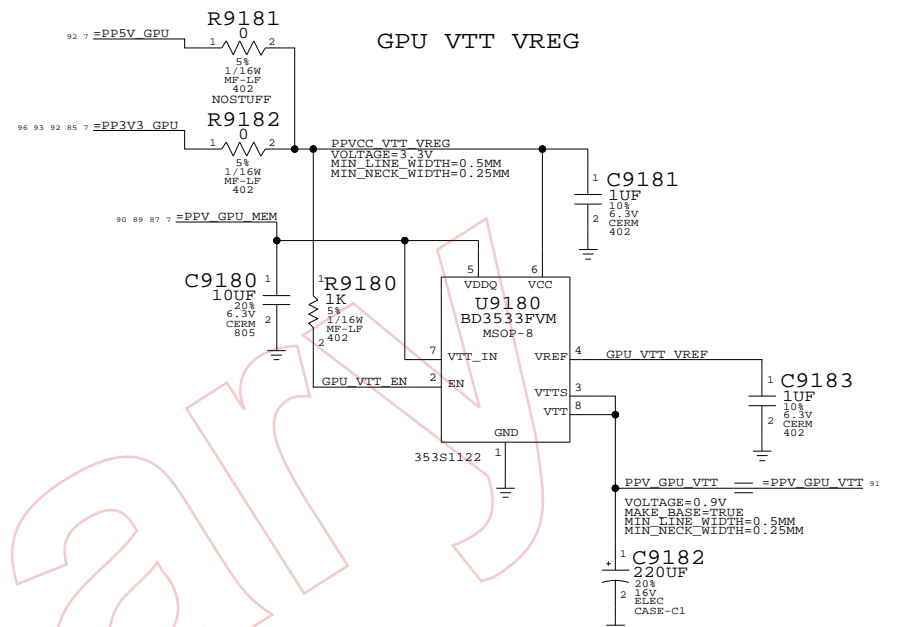
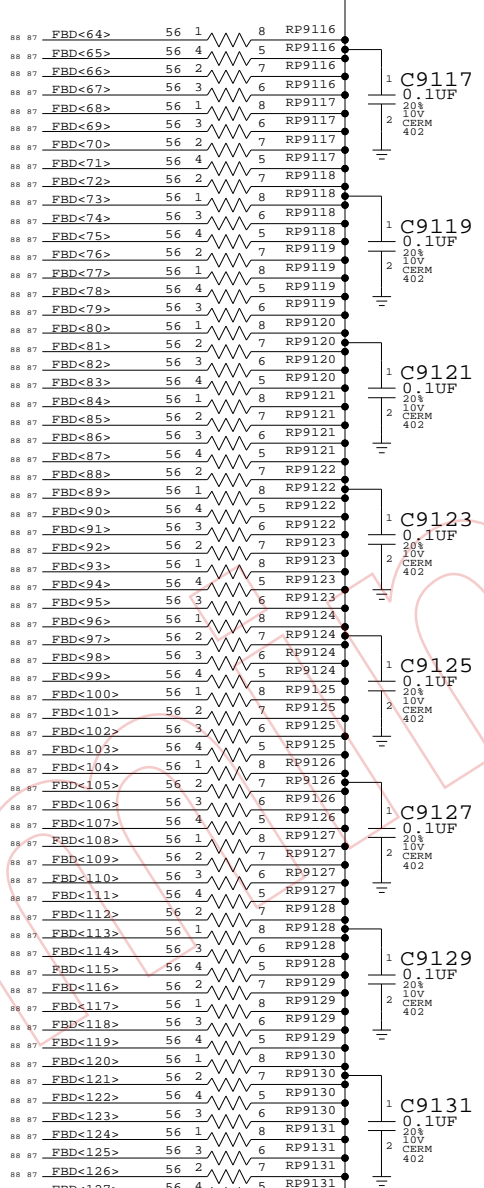
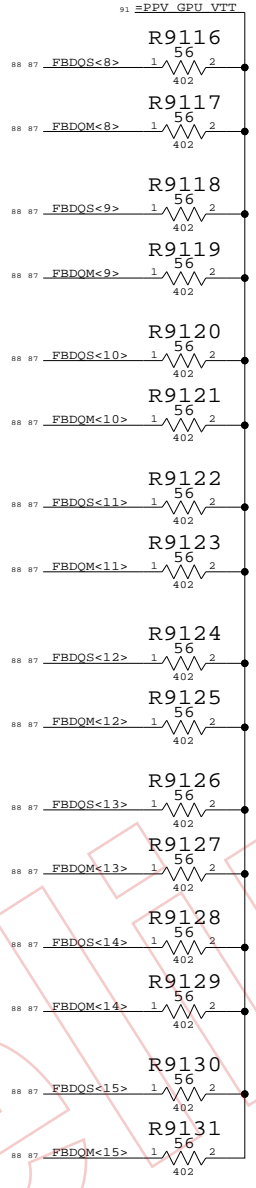
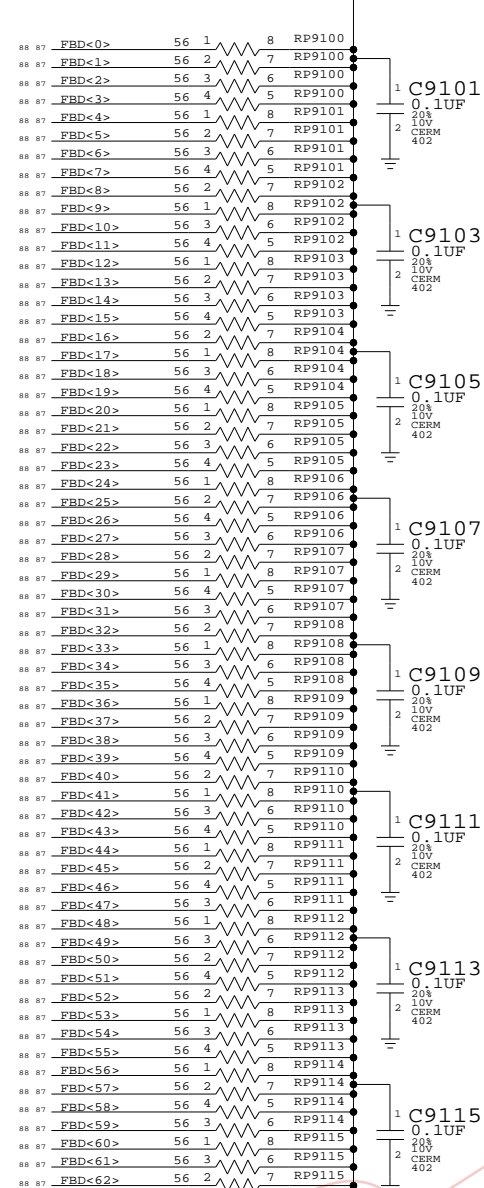
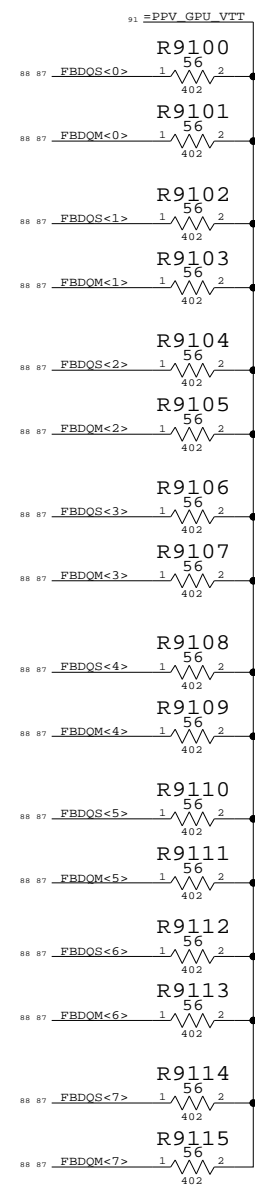
GPU GDDR SDRAM B
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SCALE	SHEET OF		
NONE	90		154

FRAME BUFFER A TERMINATION

FRAME BUFFER B TERMINATION

GPU VTT VREG



FB Parallel Termination

SYNC_MASTER=M33-DD SYNC_DATE=MASTER

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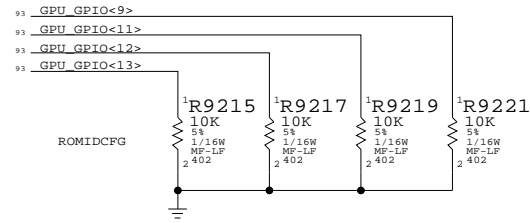
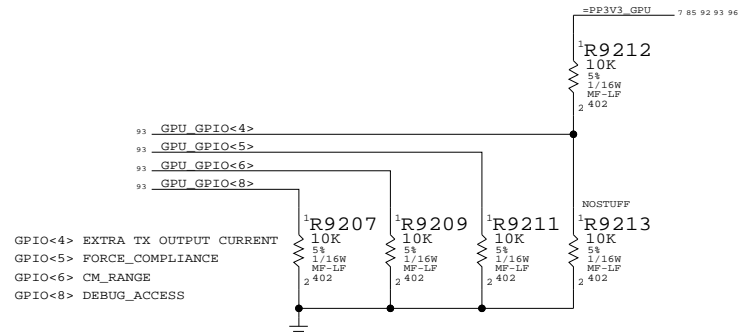
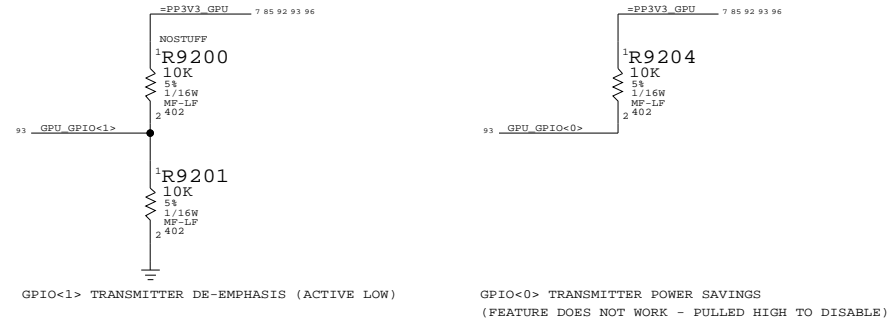
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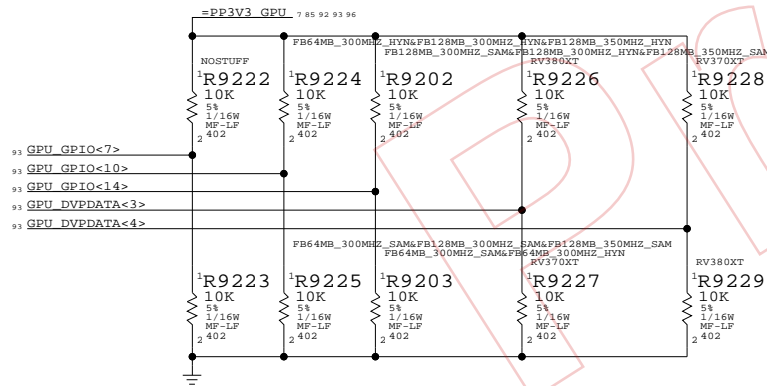
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	NONE	SHT	OF
		91	154

ATI STRAPS



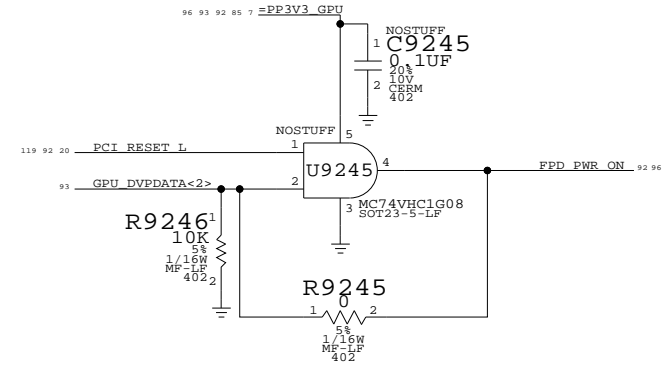
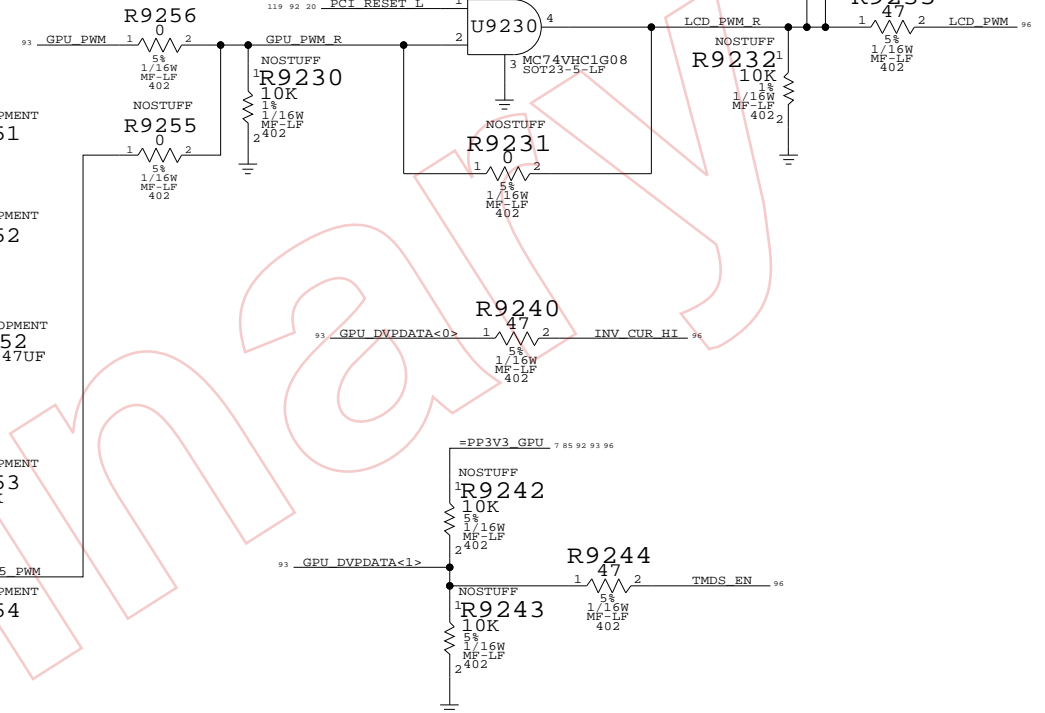
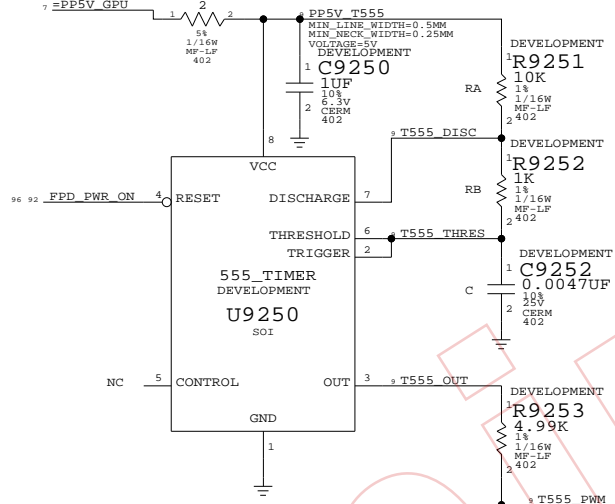
MEMORY STRAPS



GPIO<7> - MEMORY DIE REVISION
 0 - ORIGINAL DIE REVISION
 1 - NEW (FUTURE) DIE REV
 GPIO<10> - MEMORY VENDOR
 0 - SAMSUNG
 1 - HYNIX
 GPIO<14> - MEMORY DENSITY
 0 - 4MX32
 1 - 8MX32
 DVPPDATA<3,4> - SPEED
 00 - 325E / 200M
 01 - 400E / 300M
 10 - 500E / 350M
 11 - RESERVED FOR FUTURE USE

APPLE GPIOS

PROTOL HACK TO PROVIDE 91% DUTY CYCLE 25KHZ PWM
 DEVELOPMENT R9250



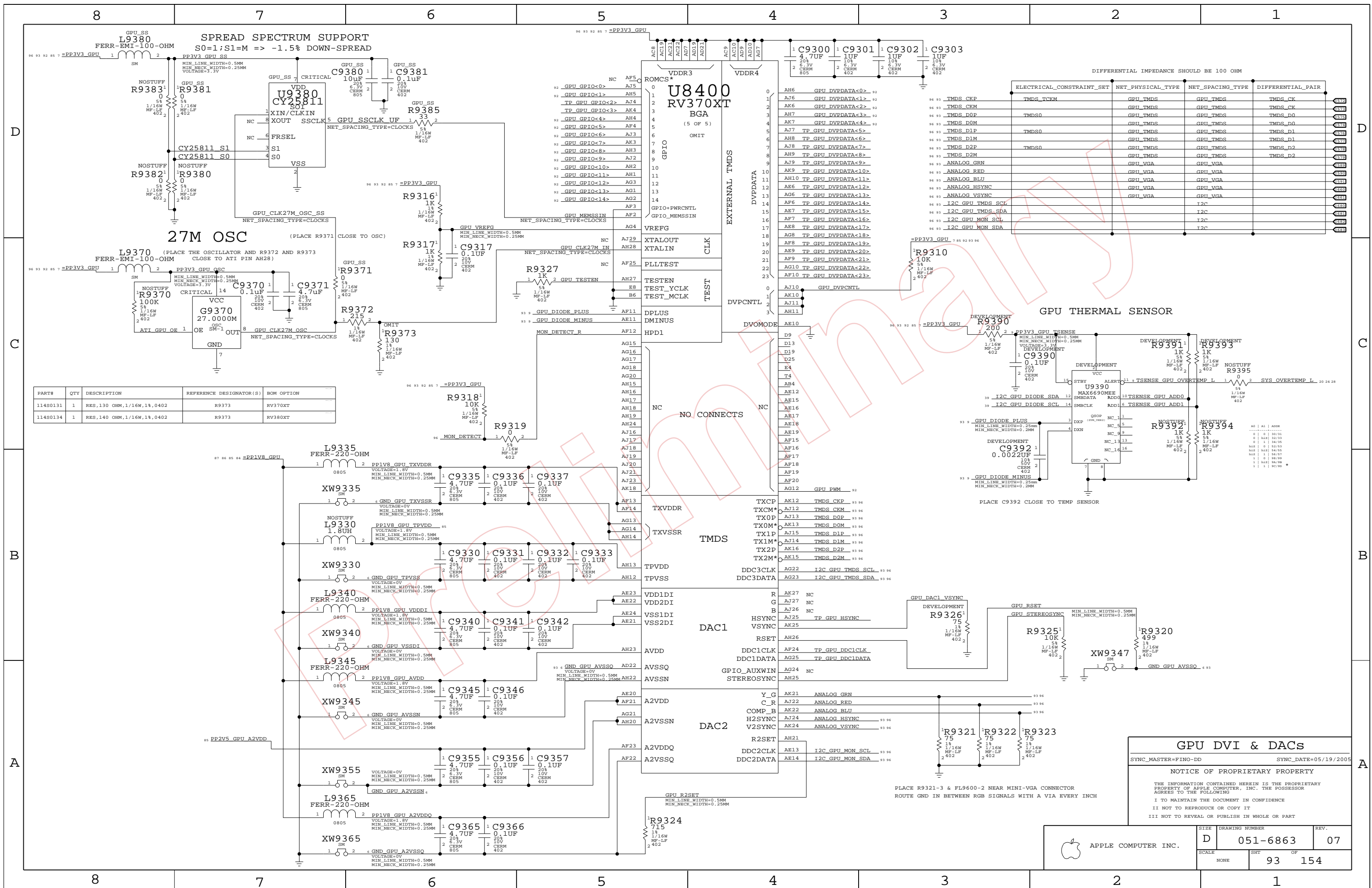
GPU Straps

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SCALE	NONE	SHT	OF
		92	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0131	1	RES,130 OHM,1/16W,1%,0402	R9373	RV370XT
114S0134	1	RES,140 OHM,1/16W,1%,0402	R9373	RV380XT

GPU DVI & DACs

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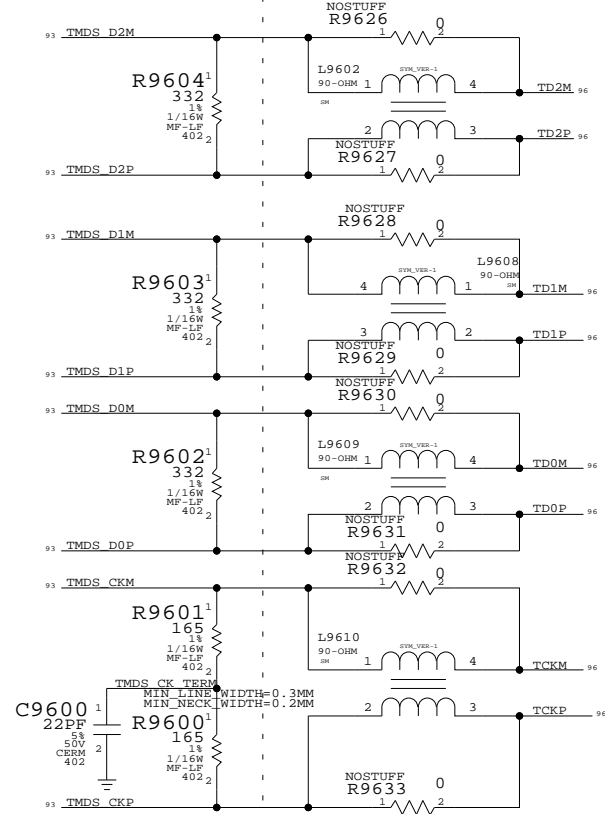
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHEET	OF	
NONE	93	154	

INTERNAL LCD

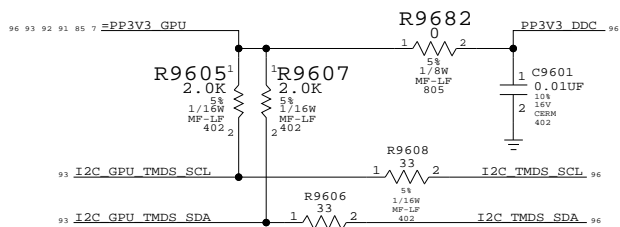
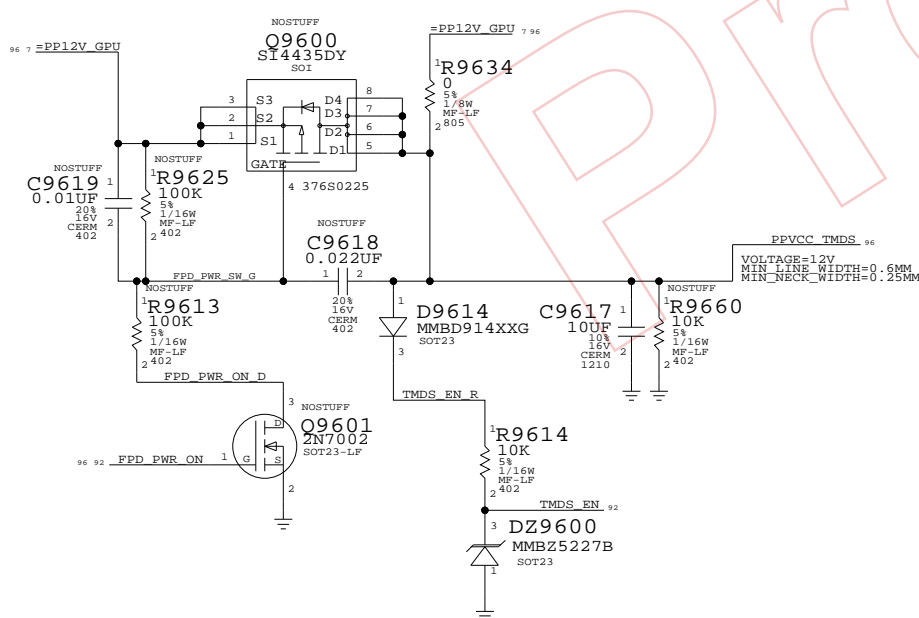
	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
96_TCKP	GPU_TMDS	GPU_TMDS	TCK
96_TCKM	GPU_TMDS	GPU_TMDS	TCK
96_TD0P	GPU_TMDS	GPU_TMDS	TD0
96_TD0M	GPU_TMDS	GPU_TMDS	TD0
96_TD1P	GPU_TMDS	GPU_TMDS	TD1
96_TD1M	GPU_TMDS	GPU_TMDS	TD1
96_TD2P	GPU_TMDS	GPU_TMDS	TD2
96_TD2M	GPU_TMDS	GPU_TMDS	TD2

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

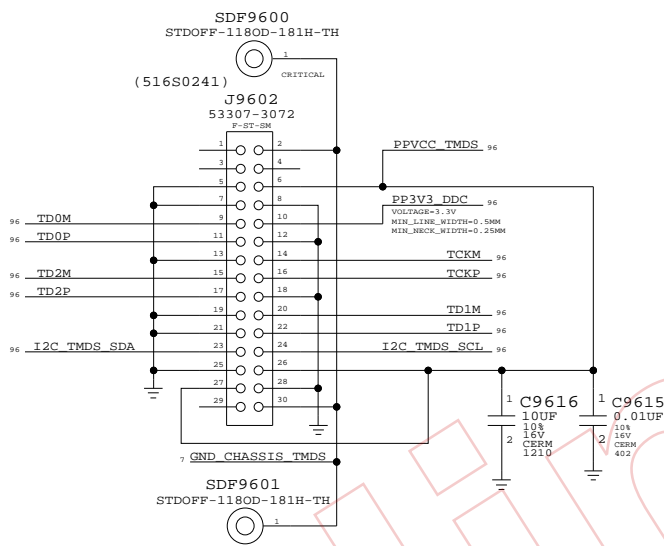
PLACE FILTER CLOSE TO TMD5 CONNECTOR



PANEL POWER SEQUENCING



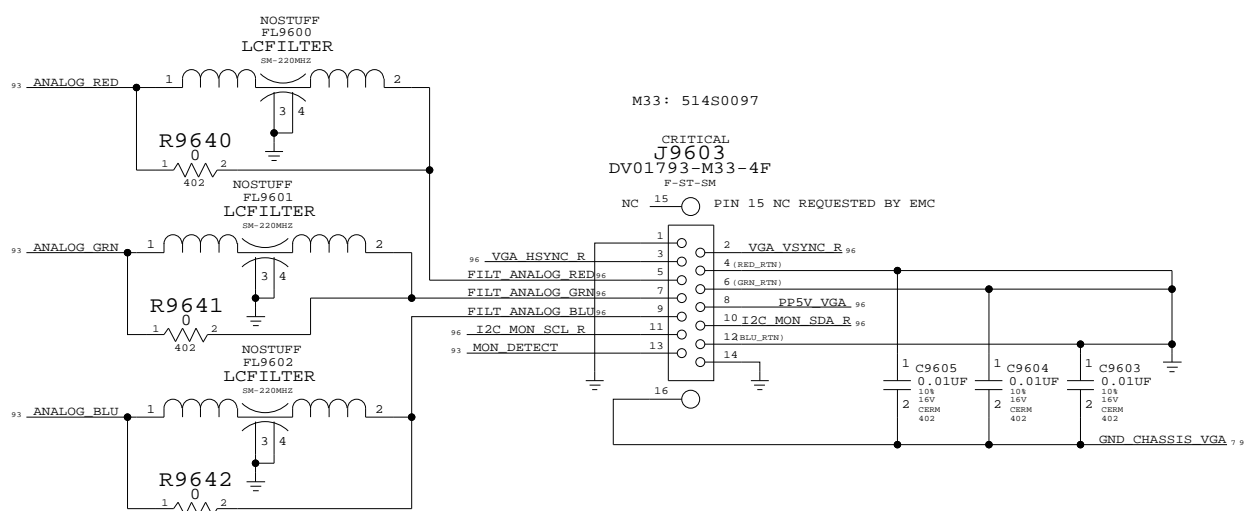
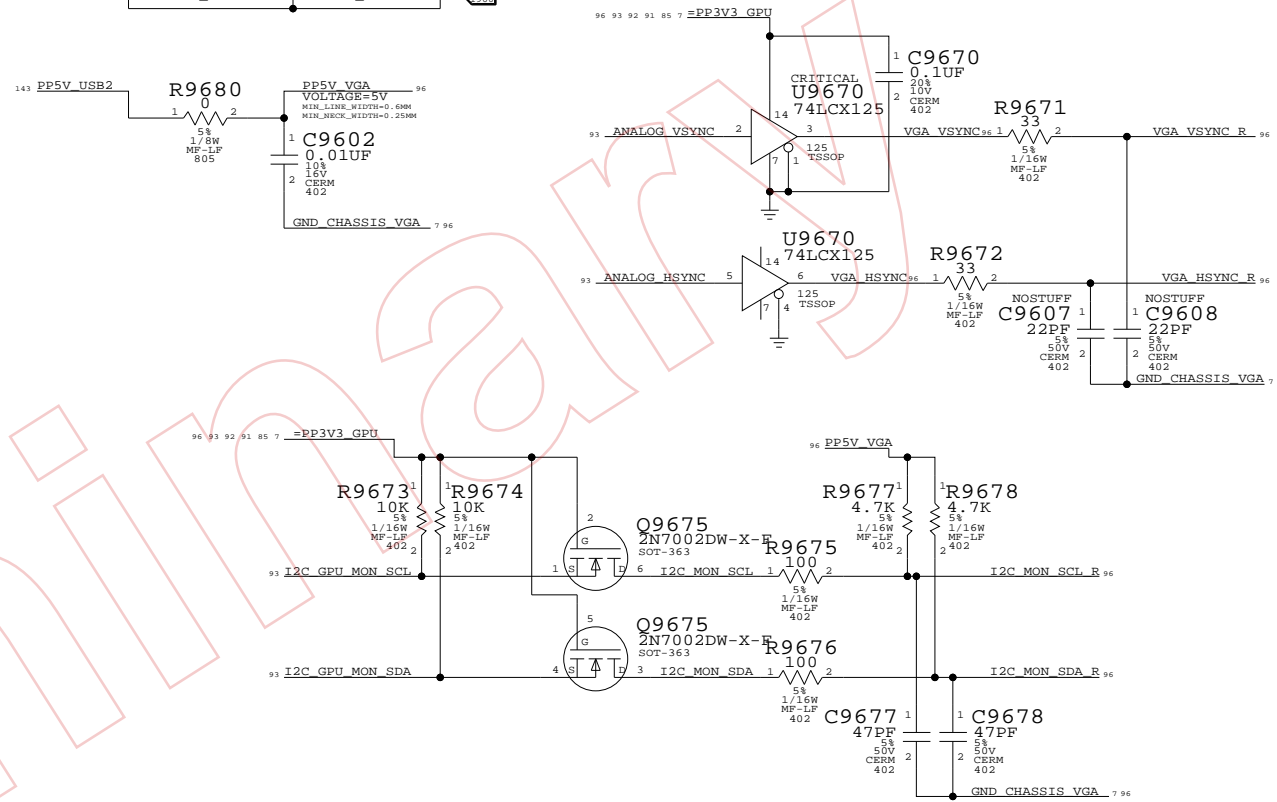
INTERNAL TMD5 CONNECTOR



SILKSCREEN: 3

EXTERNAL VGA CONNECTOR

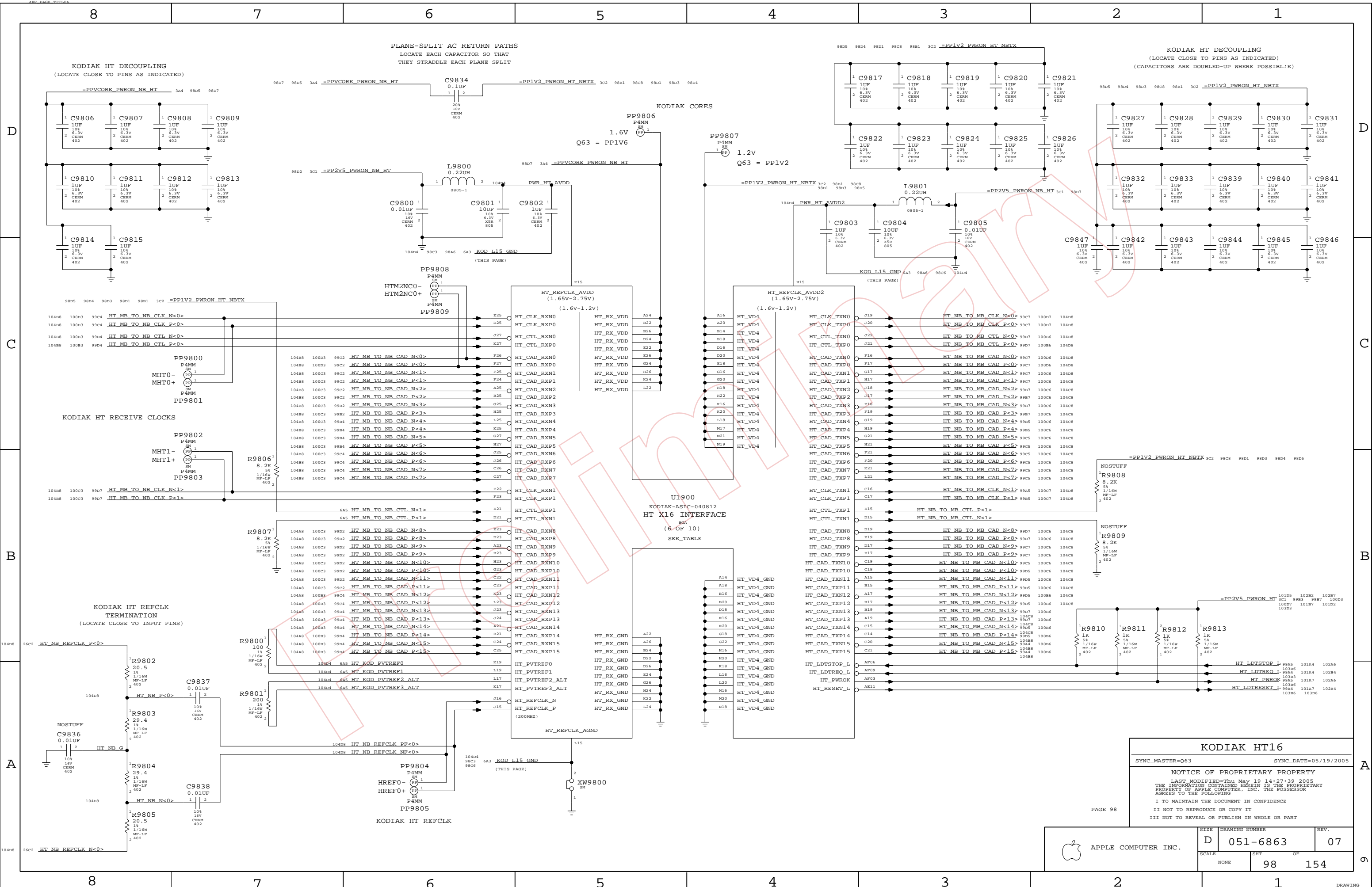
	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
96_FILT_ANALOG GRN	GPU_VGA	GPU_VGA
96_FILT_ANALOG RED	GPU_VGA	GPU_VGA
96_FILT_ANALOG BLU	GPU_VGA	GPU_VGA
96_VGA_VSYNC	GPU_VGA	GPU_VGA
96_VGA_VSYNC R	GPU_VGA	GPU_VGA
96_VGA_HSYNC	GPU_VGA	GPU_VGA
96_VGA_HSYNC R	GPU_VGA	GPU_VGA



PLACE R9321-3 & FL9600-2 CLOSE TO J9603

TMD5 / ExtVGA	
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		96	154



KODIAK HT16
 SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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	DRAWING NUMBER D 051-6863	REV. 07
	SCALE NONE	SHEET 98

D

D

C

C

B

B

A

A

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
9803 HT_NB_TO_MB_CLK_N<0>	HT_NB_TO_SB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD
9803 HT_NB_TO_MB_CLK_P<0>	HT_NB_TO_SB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD
9803 HT_NB_TO_MB_CAD_N<0>	HT_NB_TO_SB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD
9803 HT_NB_TO_MB_CAD_P<0>	HT_NB_TO_SB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD
9803 HT_NB_TO_MB_CAD_N<1>	HT_NB_TO_SB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD
9803 HT_NB_TO_MB_CAD_P<1>	HT_NB_TO_SB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD
9803 HT_NB_TO_MB_CAD_N<2>	HT_NB_TO_SB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD
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9803 NC_HT_MB_TO_NB_CAD_P<8..15>		TRUE			
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9803 TP_HT_MB_TO_NB_CLK_P<1>		TRUE			
9803 NC_HT_NB_TO_MB_CAD_P<8..15>		TRUE			
9803 NC_HT_NB_TO_MB_CAD_N<8..15>		TRUE			
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98A8 26C2 HT_NB_REFCLK_P<0>			HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK
98A8 26C2 HT_NB_REFCLK_N<0>			HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK
98A8 902 HT_NB_P<0>			HT_NB0		HT_CLK
98A8 902 HT_NB_N<0>			HT_NB0		HT_CLK
98A8 902 HT_NB_REFCLK_P<0>			HT_NB_REFCLK_F0		HT_CLK
98A8 902 HT_NB_REFCLK_N<0>			HT_NB_REFCLK_F0		HT_CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
9805 PWR_HT_AVDD	0.4MM	0.2MM	2.5
9804 PWR_HT_AVDD2	0.4MM	0.2MM	2.5
9806 9803 98A6 60C KOD_L15_GND	0.4MM	0.2MM	0
98A8 HT_NB_G			KEEP DIFF CLOCK FROM BEING A SINGLE XNET

HT ALIASES

FINO-EG 05/19/2005

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	D	051-6863	07
SCALE	SHT	101	154
NONE			

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
HT_CLK66M_SB_C	0.38mm SPACING	
HT_CLK66M_SB	0.38mm SPACING	
HT_LDRESET_L	P3MM SPACING	

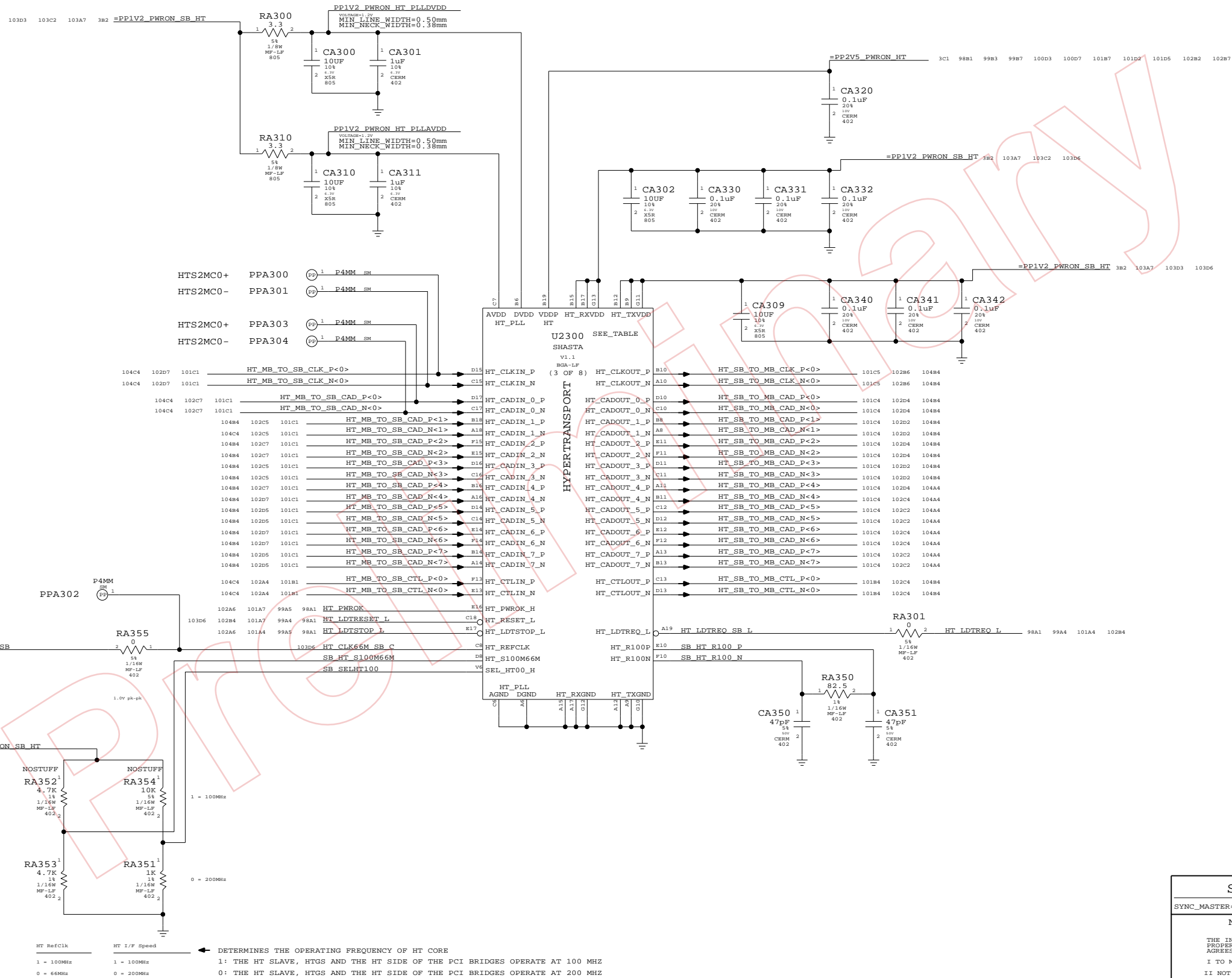
HT_CLK66M_SB_C	103B6
HT_CLK66M_SB	26C2 103B7
HT_LDRESET_L	98A1 99A4 101A7 102B4 103B6

Page Notes

Power aliases required by this page:
 =PP2V5_PWRON_HT
 =PP1V2_PWRON_HT

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - SB_HT_200M
 Stuffs resistor to select 200MHz HT I/F.



HT Refclk HT I/F Speed

1 = 100MHz 1 = 100MHz
 0 = 66MHz 0 = 200MHz

DETERMINES THE OPERATING FREQUENCY OF HT CORE

1: THE HT SLAVE, HTGS AND THE PCI BRIDGES OPERATE AT 100 MHZ
 0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE	SHT	OF
NONE	103	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
		PCI_AD<31..28>
		PCI_AD<27>
		PCI_AD<26..24>
		PCI_AD<23>
		PCI_AD<22>
		PCI_AD<21>
		PCI_AD<20>
		PCI_AD<19..18>
		PCI_AD<17>
		PCI_AD<16..0>
		PCI_CBE_L<3..0>
		PCI_PAR
		PCI_DEVSEL_L
		PCI_FRAME_L
		PCI_IRDY_L
		PCI_TRDY_L
		PCI_STOP_L
	P3MM SPACING	PCI_CLK66M_SB_INT

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

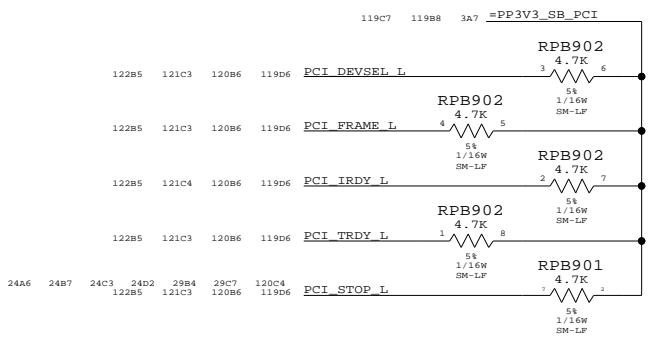
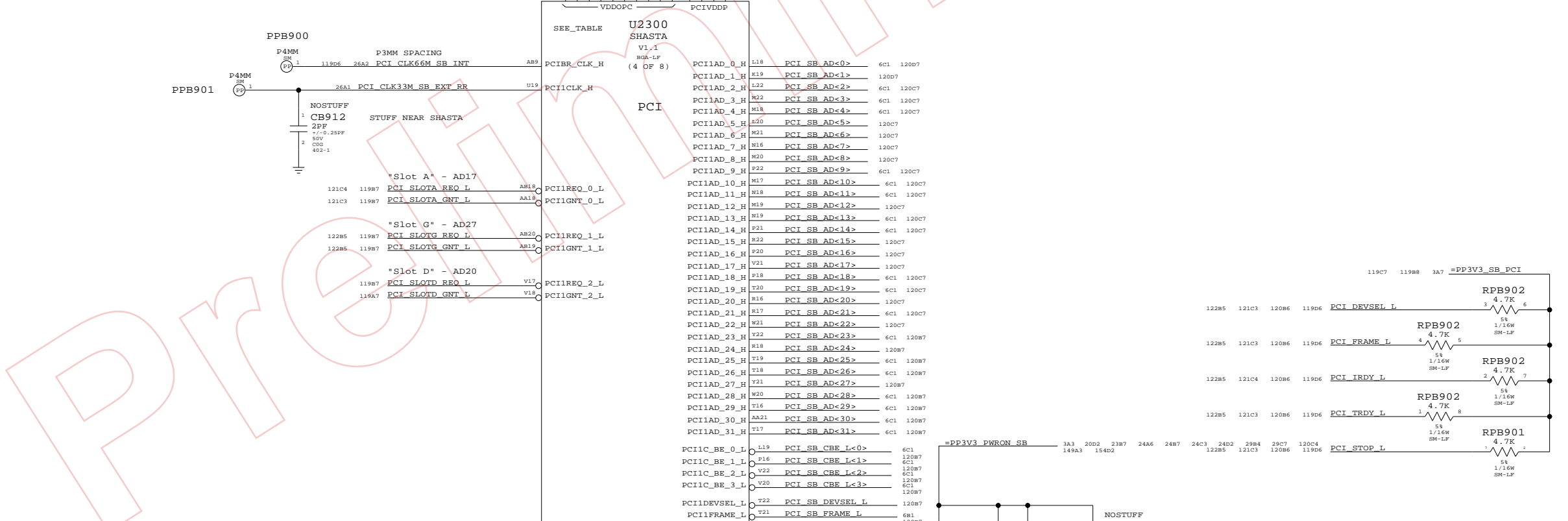
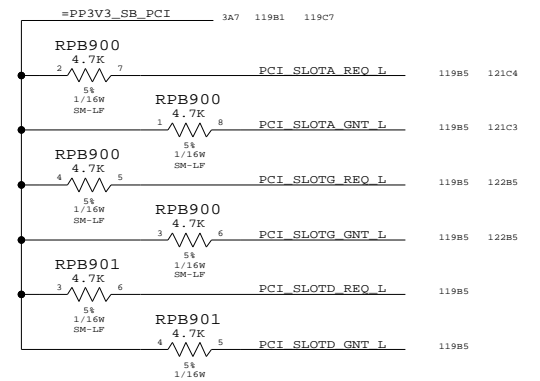
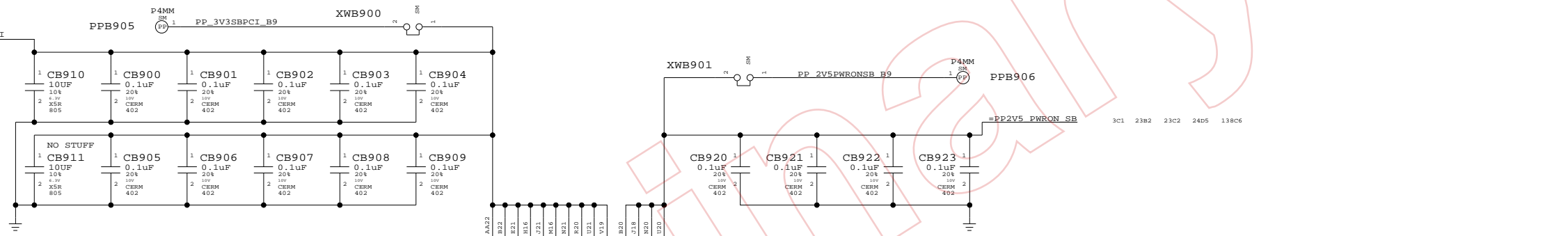
Page Notes

Power aliases required by this page:
 - PP3V3_PCI
 - PP3V3_SB_PCI (CAN BE PP3V3_PCI)
 - PP3V3_PWRON_SB
 - PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

ROM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD11 - PC10 (0x1068/0x0053)
 AD11 - PC11 (0x1068/0x0054)
 AD11 - PC12 (0x1068/0x0055)
 AD23 - KeyLargo (0x1068/0x004F, PC11)
 AD28 - SATA 150 (0x1166/0x0240, PC10 or 2)
 AD29 - UATA 133 (0x1068/0x0050, PC10 or 2)
 AD30 - FireWire (0x1068/0x0052, PC10 or 2)
 AD31 - Ethernet (0x1068/0x0051, PC10)



Shasta PCI Interface
 SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE	SHT	OF
NONE	119	154

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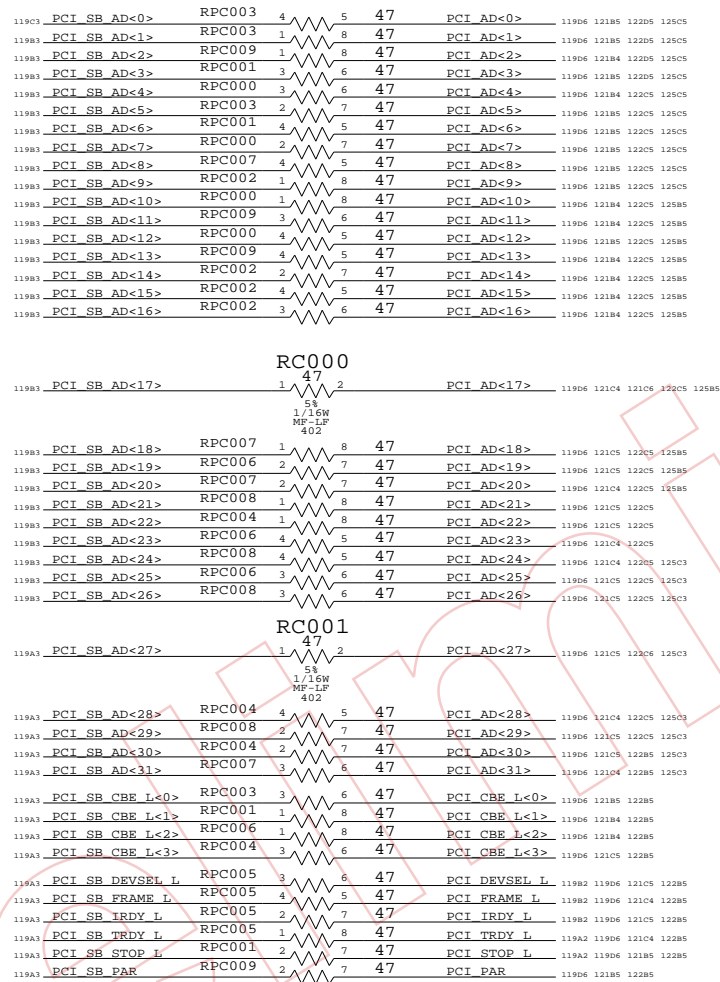
3

2

1

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)



PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	NONE	SHT	120 OF 154

8

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1

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
 - _PP3V3_PCI

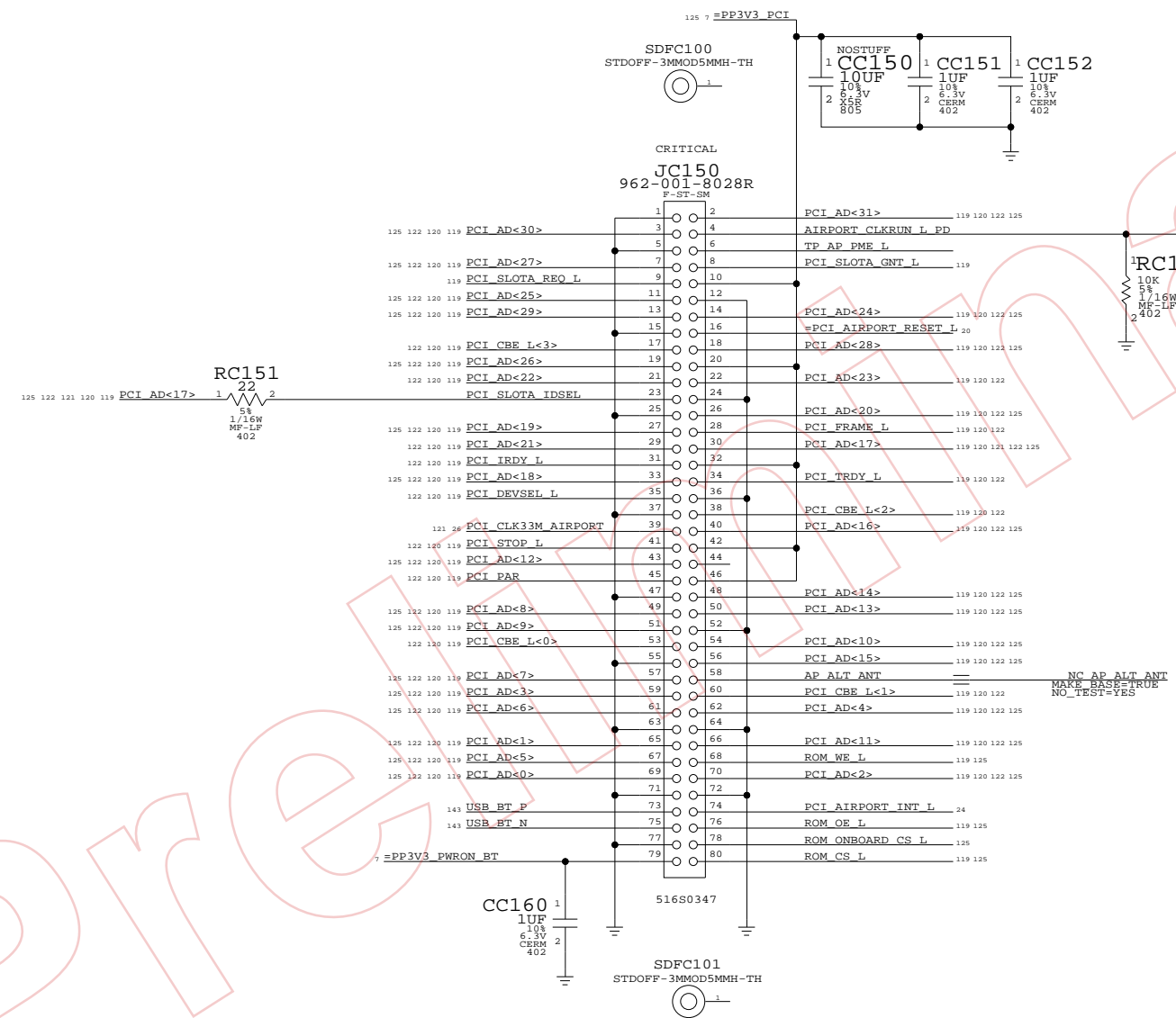
Signal aliases required by this page:
 - _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



D

D

C

C

B

B

A

A

AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-EG SYNC_DATE=05/19/2005

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	D	051-6863	07
SCALE		SHT	OF
NONE		121	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 120A3 122B5

Page Notes

Power aliases required by this page:
 - _PPVIO_PCI (to 3.3V or 5V)

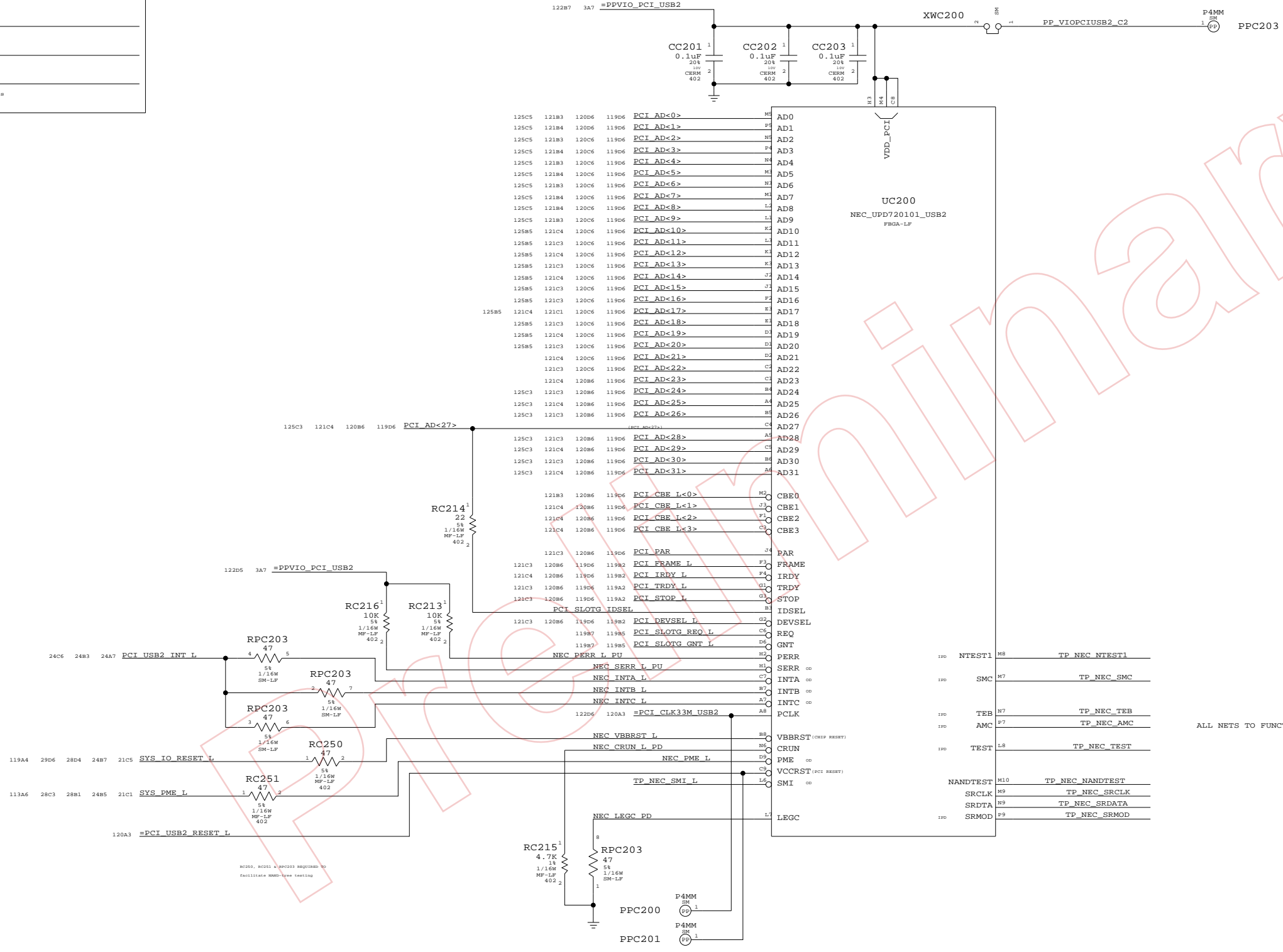
Signal aliases required by this page:
 - _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 AD27 (Slot "0") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

Q63 APPLICATION OF POWER NET "-PPVIO_PCI_USB2" IS PP3V3_RUN



ALL NETS TO FUNCTIONAL TEST PAGE

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	NONE	SHT	OF
		122	154

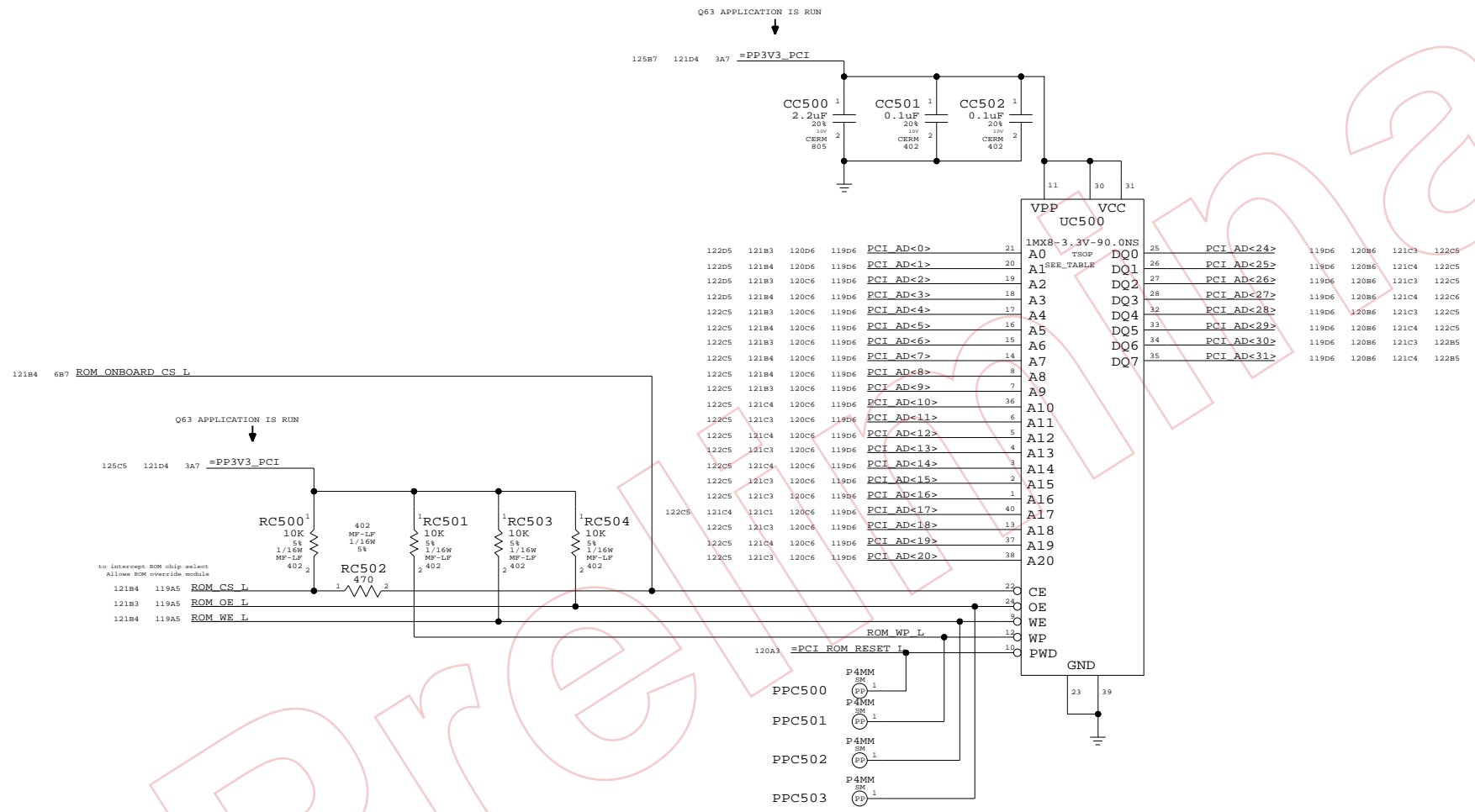
Page Notes

Power aliases required by this page:
 - PP3V3_PCI

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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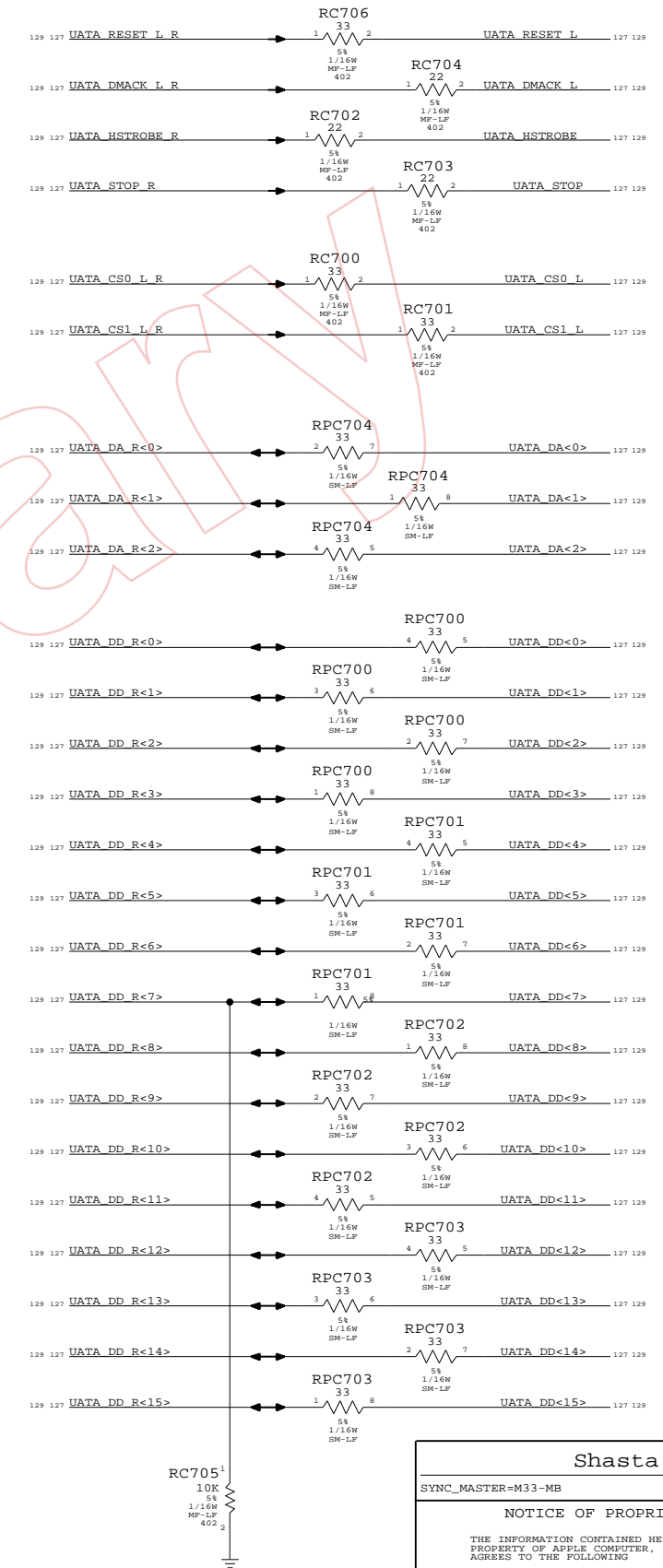
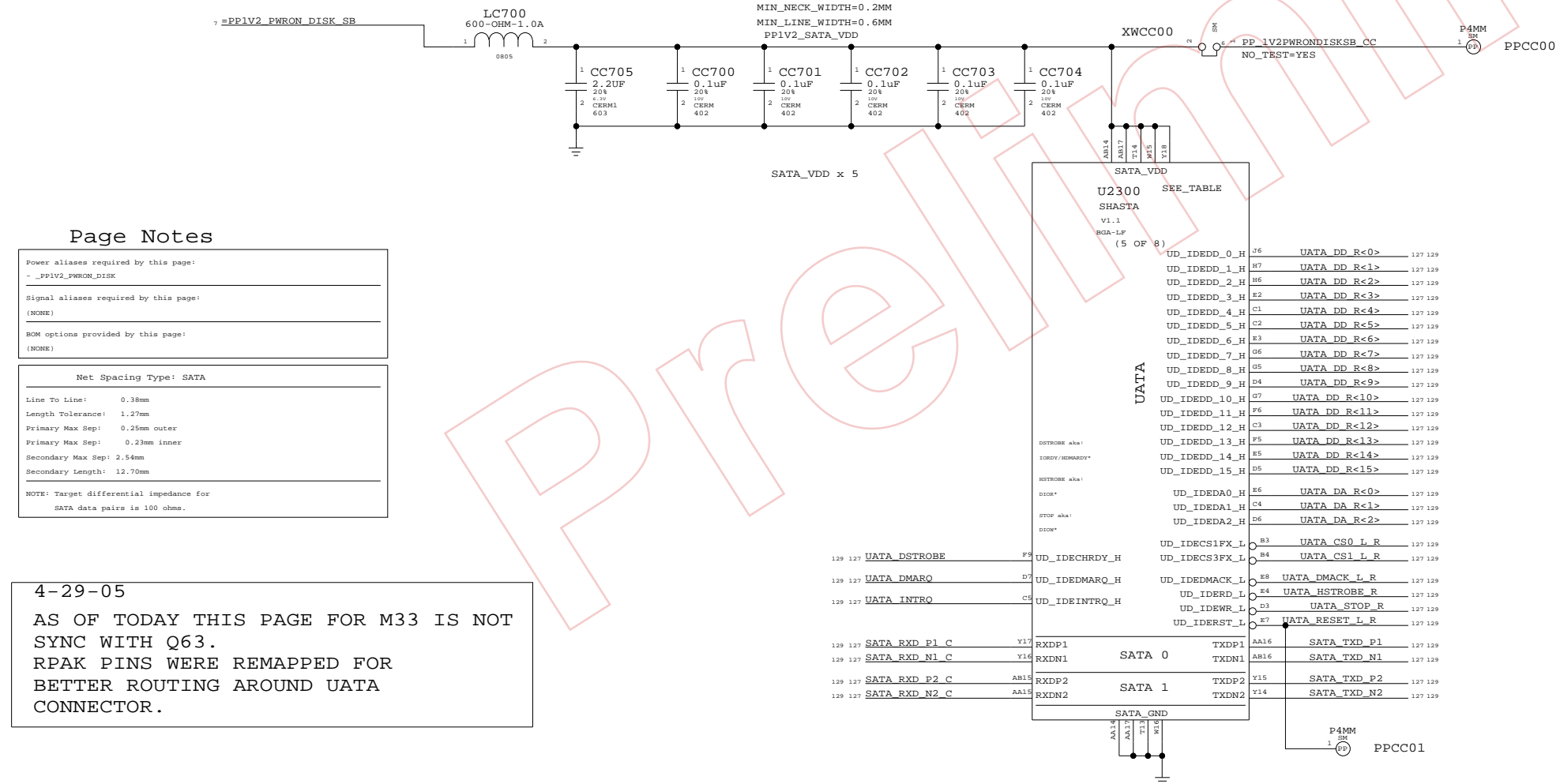
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE		SHT	OF
NONE		125	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	SATA	SATA	SATA_RXD1_C
	SATA	SATA	SATA_RXD1_C
	SATA	SATA	SATA_TXD1
	SATA	SATA	SATA_TXD1
	SATA	SATA	SATA_RXD2_C
	SATA	SATA	SATA_RXD2_C
	SATA	SATA	SATA_TXD2
	SATA	SATA	SATA_TXD2
			UATA_DD<15..8>
			UATA_DD<7>
			UATA_DD<6..0>
			UATA_DA<2..0>
			UATA_CS1_L
			UATA_CS1_L
			UATA_HSTROBE
			UATA_STOP
			UATA_DMACK_L
			UATA_RESET_L
			UATA_DSTROBE
			UATA_DMARQ
			UATA_INTRO
			UATA_DD_R<15..8>
			UATA_DD_R<7>
			UATA_DD_R<6..0>
			UATA_DA_R<2..0>
			UATA_CS0_L_R
			UATA_CS1_L_R
			UATA_DMACK_L_R
			UATA_HSTROBE_R
			UATA_STOP_R
			UATA_RESET_L_R

PLACE UATA TERMINATION RESISTORS NEAR JC901 CONNECTOR



Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.25mm outer
Primary Max Sep: 0.23mm inner
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

4-29-05
AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
RPAK PINS WERE REMAPPED FOR BETTER ROUTING AROUND UATA CONNECTOR.

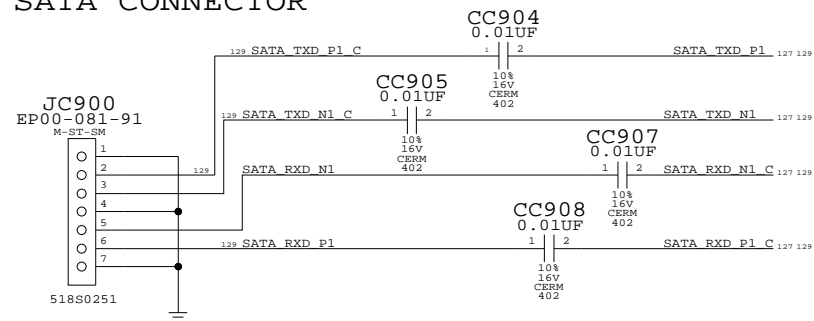
UATA	UATA	UATA
UD_IDEDD_0_H	U76	UATA_DD_R<0>
UD_IDEDD_1_H	H7	UATA_DD_R<1>
UD_IDEDD_2_H	H6	UATA_DD_R<2>
UD_IDEDD_3_H	E2	UATA_DD_R<3>
UD_IDEDD_4_H	C1	UATA_DD_R<4>
UD_IDEDD_5_H	C2	UATA_DD_R<5>
UD_IDEDD_6_H	E3	UATA_DD_R<6>
UD_IDEDD_7_H	O6	UATA_DD_R<7>
UD_IDEDD_8_H	O5	UATA_DD_R<8>
UD_IDEDD_9_H	D4	UATA_DD_R<9>
UD_IDEDD_10_H	O7	UATA_DD_R<10>
UD_IDEDD_11_H	F6	UATA_DD_R<11>
UD_IDEDD_12_H	C3	UATA_DD_R<12>
UD_IDEDD_13_H	F5	UATA_DD_R<13>
UD_IDEDD_14_H	E5	UATA_DD_R<14>
UD_IDEDD_15_H	O5	UATA_DD_R<15>
UD_IDEDA0_H	E6	UATA_DA_R<0>
UD_IDEDA1_H	C4	UATA_DA_R<1>
UD_IDEDA2_H	D6	UATA_DA_R<2>
UD_IDECS1FX_L	B3	UATA_CS0_L_R
UD_IDECS3FX_L	B4	UATA_CS1_L_R
UD_IDEDMACK_L	B8	UATA_DMACK_L_R
UD_IDERD_L	D3	UATA_HSTROBE_R
UD_IDEWR_L	D3	UATA_STOP_R
UD_IDERST_L	E7	UATA_RESET_L_R
RXDP1	AA16	SATA_TXD_P1
RXDN1	AA16	SATA_TXD_N1
RXDP2	Y15	SATA_TXD_P2
RXDN2	Y14	SATA_TXD_N2

Shasta Disk
SYNC_MASTER=M33-MB SYNC_DATE=05/19/2005

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	D	051-6863	07
SCALE	NONE	SHT	OF
		127	154

SATA CONNECTOR

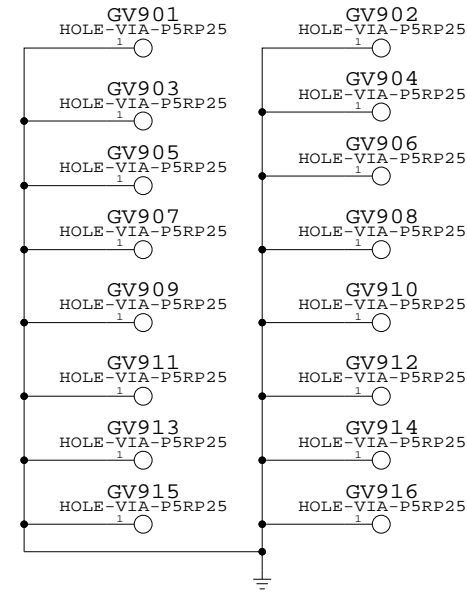


SATA PORT1 IS NOT USED IN M23/M33:NO TEST

- 127 SATA TXD P2 == NC_SATA_TXD_P2 6 MAKE_BASE=TRUE
- 127 SATA TXD N2 == NC_SATA_TXD_N2 6 MAKE_BASE=TRUE
- 127 SATA RXD N2 C == NC_SATA_RXD_N2_C 6 MAKE_BASE=TRUE
- 127 SATA RXD P2 C == NC_SATA_RXD_P2_C 6 MAKE_BASE=TRUE

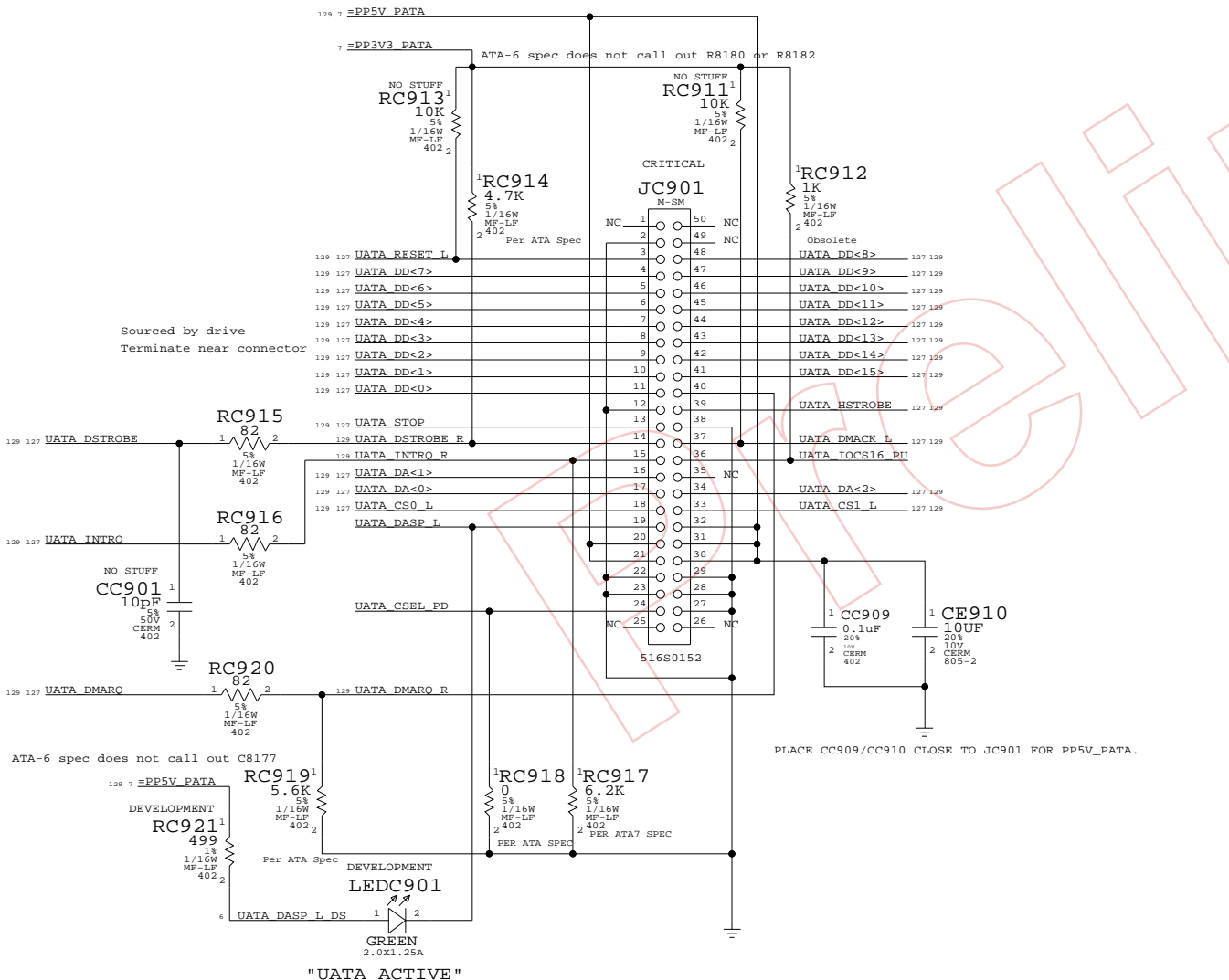
SATA & USB DIFF PAIR GND VIAS

ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA APPROXIMATELY 0.152MM AWAY FROM SIGNAL VIA.



M33 PATA CONNECTOR

4-12-05



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
129 127 UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_HSTROBE	UATA_DD	UATA_NETPH	UATA_NETSPA		
129 127 UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
129 127 UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DMARQ	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
129 127 UATA_INTRO_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM RPAKS TO JC901

127 UATA_DD R<15..8>	UATA_NETPH	UATA_NETSPA		
127 UATA_DD R<7>	UATA_NETPH	UATA_NETSPA		
127 UATA_DD R<6..0>	UATA_NETPH	UATA_NETSPA		
127 UATA_DA R<2..0>	UATA_NETPH	UATA_NETSPA		
127 UATA_CS0_L R	UATA_NETPH	UATA_NETSPA		
127 UATA_CS1_L R	UATA_NETPH	UATA_NETSPA		
127 UATA_HSTROBE_R	UATA_NETPH	UATA_NETSPA		
127 UATA_STOP_R	UATA_NETPH	UATA_NETSPA		
127 UATA_DMACK_L R	UATA_NETPH	UATA_NETSPA		
127 UATA_RESET_L R	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DSTROBE	UATA_NETPH	UATA_NETSPA		
129 127 UATA_DMARQ	UATA_NETPH	UATA_NETSPA		
129 127 UATA_INTRO	UATA_NETPH	UATA_NETSPA		

UATA FROM SHASTA U2300 TO RPAKS

129 127 SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
129 127 SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
129 127 SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
129 127 SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
129 127 SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
129 127 SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
129 127 SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
129 127 SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGNMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE. UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05

NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE FOR PP1V2_SATA_VDD AND THEN NECK DOWN TO THE DEFAULT VALUE WHEN NECESSARY. THE WIDTH/NECK PROPERTIES ON PAGE 127 ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.

PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL HELP MITIGATE THE LOSS ACROSS THE Q1306 FET SI3326DV.

4-12-05.

UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M33-MB SYNC_DATE=05/19/2005

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	D	051-6863	07
SCALE	SHEET	OF	
NONE	129	154	

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D

D

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA₈ -> VESTA

131	9	ENET_TXD_R<0>	159	MAKE_BASE=TRUE	ENET_TXD<0>	9	131	132
131	9	ENET_TXD_R<1>	160	MAKE_BASE=TRUE	ENET_TXD<1>	9	131	132
131	9	ENET_TXD_R<2>	161	MAKE_BASE=TRUE	ENET_TXD<2>	9	131	132
131	9	ENET_TXD_R<3>	162	MAKE_BASE=TRUE	ENET_TXD<3>	9	131	132
131	9	ENET_TXD_R<4>	163	MAKE_BASE=TRUE	ENET_TXD<4>	9	131	132
131	9	ENET_TXD_R<5>	164	MAKE_BASE=TRUE	ENET_TXD<5>	9	131	132
131	9	ENET_TXD_R<6>	165	MAKE_BASE=TRUE	ENET_TXD<6>	9	131	132
131	9	ENET_TXD_R<7>		MAKE_BASE=TRUE	ENET_TXD<7>	9	131	132
			166					
131	9	ENET_TX_EN_R	167	MAKE_BASE=TRUE	ENET_TX_EN	9	131	132
131	9	ENET_TX_ER_R		MAKE_BASE=TRUE	ENET_TX_ER	9	131	132
			168					
131	9	ENET_CLK125M_GTX_R		MAKE_BASE=TRUE	ENET_CLK125M_GTX	131	132	
			169					
131	9	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131	132	

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

			184					
132	ENET_CLK125M_GBE_REF_R		MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	132			
			170					
132	ENET_CLK25M_TX_R		MAKE_BASE=TRUE	ENET_CLK25M_TX	131			
			171					
132	ENET_CLK125M_RX_R		MAKE_BASE=TRUE	ENET_CLK125M_RX	131			
			172					
132	9	ENET_RXD_R<0>	173	MAKE_BASE=TRUE	ENET_RXD<0>	9	131	
132	9	ENET_RXD_R<1>	174	MAKE_BASE=TRUE	ENET_RXD<1>	9	131	
132	9	ENET_RXD_R<2>	175	MAKE_BASE=TRUE	ENET_RXD<2>	9	131	
132	9	ENET_RXD_R<3>	176	MAKE_BASE=TRUE	ENET_RXD<3>	9	131	
132	9	ENET_RXD_R<4>	177	MAKE_BASE=TRUE	ENET_RXD<4>	9	131	
132	9	ENET_RXD_R<5>	178	MAKE_BASE=TRUE	ENET_RXD<5>	9	131	
132	9	ENET_RXD_R<6>	179	MAKE_BASE=TRUE	ENET_RXD<6>	9	131	
132	9	ENET_RXD_R<7>		MAKE_BASE=TRUE	ENET_RXD<7>	9	131	
			180					
132	9	ENET_RX_DV_R	181	MAKE_BASE=TRUE	ENET_RX_DV	131		
132	9	ENET_RX_ER_R		MAKE_BASE=TRUE	ENET_RX_ER	131		
			182					
132	9	ENET_COL_R	183	MAKE_BASE=TRUE	ENET_COL	131		
132	9	ENET_CR_S_R		MAKE_BASE=TRUE	ENET_CR_S	131		

Preliminary

C

C

B

B

A

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ENET SERIES TERM

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT	OF	
NONE	130	154	

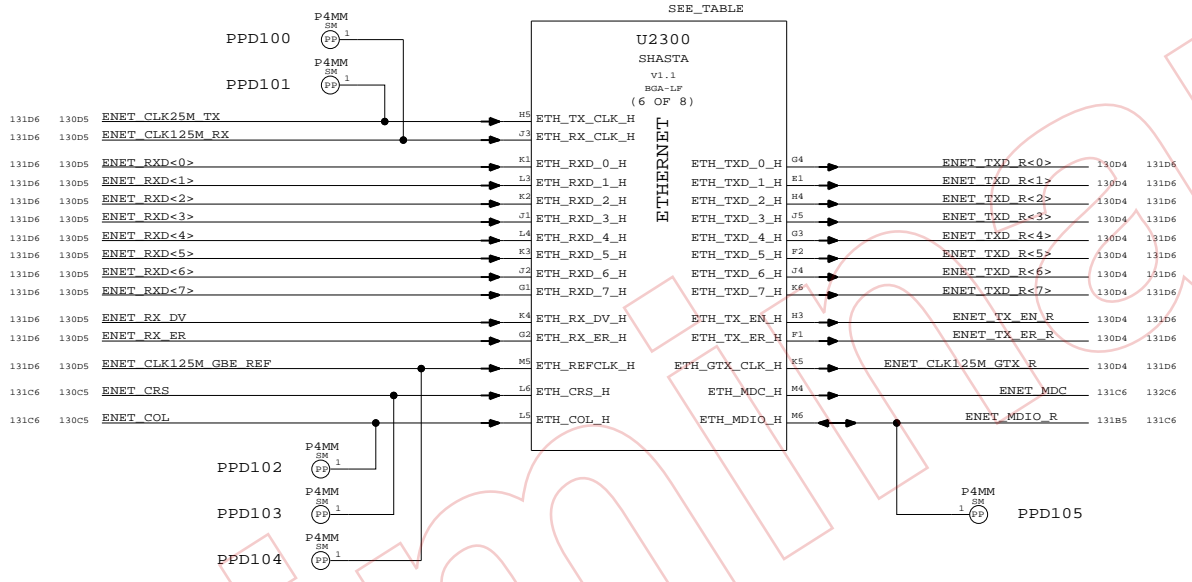
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR			
PPD100	0.38mm SPACING	ENET_CLK25M_TX	130D5	131C6	
PPD100	0.38mm SPACING	ENET_CLK125M_RX	130D5	131C6	
PPD100	0.38mm SPACING	ENET_CLK125M_GBE_REF	130D5	131C6	
PPD100	0.38mm SPACING	ENET_CLK125M_GTX	130B6	132C5	
PPD100	0.38mm SPACING	ENET_CLK125M_GTX_R	130D4	131C3	
PPD100	ENET_FW_2X	ENET_RXD R<7..0>	130B4	130C4	132C3
PPD100	ENET_FW_3X	ENET_RX_DV_R	130B4	132C3	
PPD100	ENET_FW_3X	ENET_RX_ER_R	130B4	132C3	
PPD100	ENET_FW_2X	ENET_RXD<7..0>	130D5	131C6	
PPD100	ENET_FW_3X	ENET_RX_DV	130D5	131C6	
PPD100	ENET_FW_3X	ENET_RX_ER	130D5	131C6	
PPD100	ENET_FW_2X	ENET_TXD R<7..0>	130D4	131C3	
PPD100	ENET_FW_3X	ENET_TX_EN_R	130D4	131C3	
PPD100	ENET_FW_3X	ENET_TX_ER_R	130D4	131C3	
PPD100	ENET_FW_2X	ENET_TXD<7..0>	130B6	130C6	132C5
PPD100	ENET_FW_3X	ENET_TX_EN	130B6	132C5	
PPD100	ENET_FW_3X	ENET_TX_ER	130B6	132C5	
PPD100	ENET_FW_3X	ENET_CRS_R	130B4	132C3	
PPD100	ENET_FW_3X	ENET_COL_R	130B4	132C3	
PPD100	ENET_FW_3X	ENET_CRS	130C5	131C6	
PPD100	ENET_FW_3X	ENET_COL	130C5	131C6	
PPD100	ENET_FW_3X	ENET_MDC	131C3	132C6	
PPD100	ENET_FW_3X	ENET_MDIO	131B3	132C6	
PPD100	ENET_FW_3X	ENET_MDIO_R	131B5	131C3	
PPD100	ENET_FW_3X	R8405_1	131B4		
PPD100	ENET_FW_3X	R8405_2	131B4		
PPD100	ENET_FW_3X	R8407_2	131A4		

Page Notes

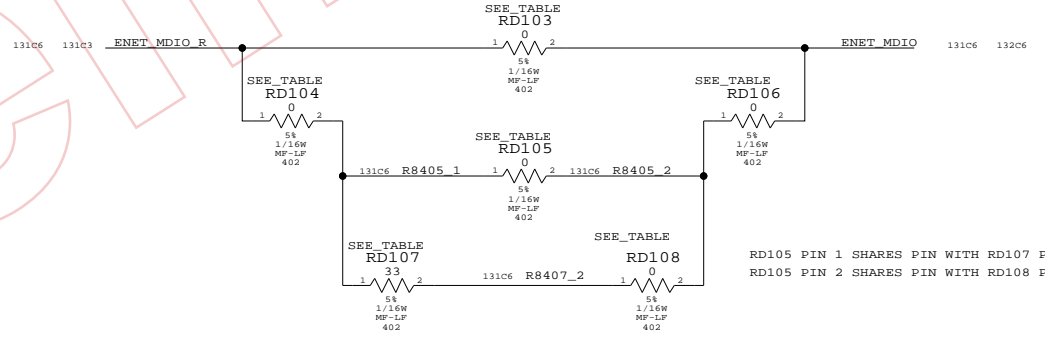
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES, 0-OHM, 402, 5%	RD103		ENET_MDIO_DELAY_0 *
116S0004	3	RES, 0-OHM, 402, 5%	RD104, RD105, RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES, 0-OHM, 402, 5%	RD104, RD108, RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES, 33-OHM, 402, 5%	RD107		ENET_MDIO_DELAY_4NS

Shasta Ethernet
 SYNC_MASTER=Q63 SYNC_DATE=05/19/2005
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	D	051-6863	07
SCALE	SHT OF		
NONE	131	154	

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET	PHYSICAL TYPE	VALUE	REF
ENET	ENET MDI P<0>	132 136	
ENET	ENET MDI N<0>	132 136	
ENET	ENET MDI P<1>	132 136	
ENET	ENET MDI N<1>	132 136	
ENET	ENET MDI P<2>	132 136	
ENET	ENET MDI N<2>	132 136	
ENET	ENET MDI P<3>	132 136	
ENET	ENET MDI N<3>	132 136	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

D

D

C

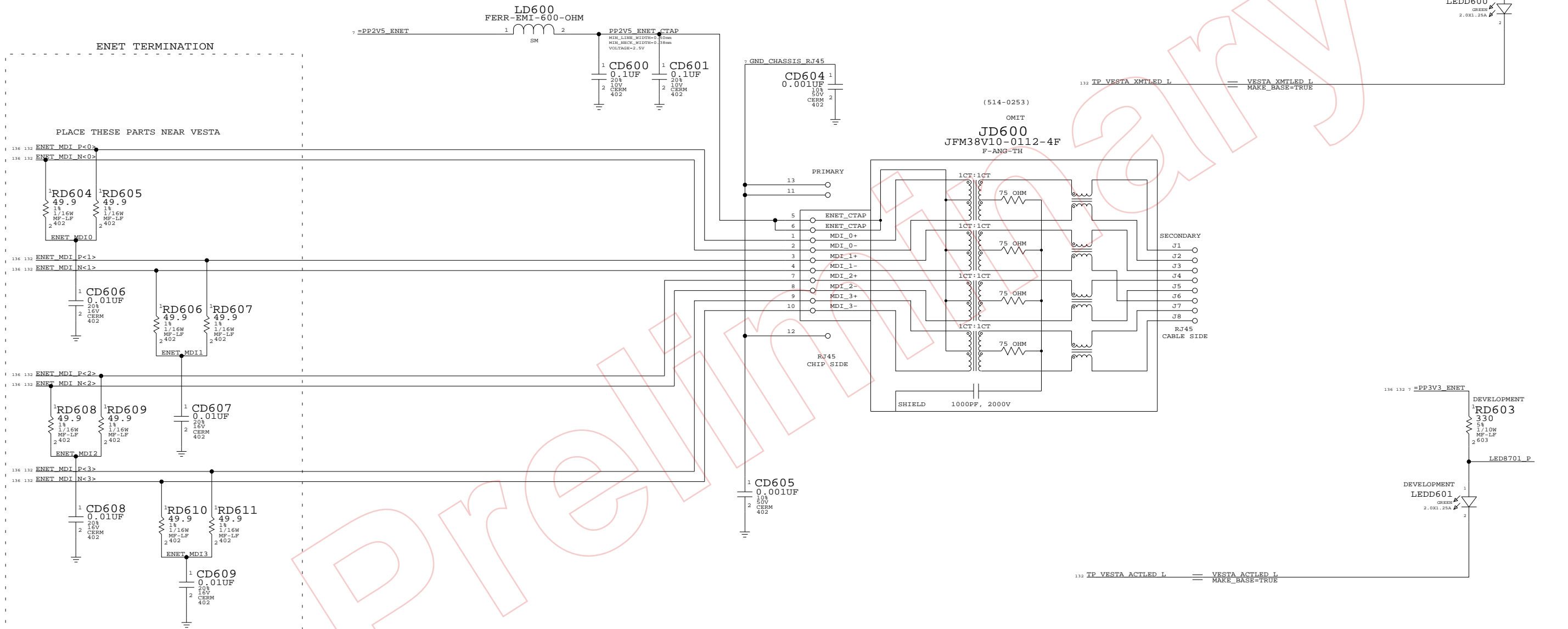
C

B

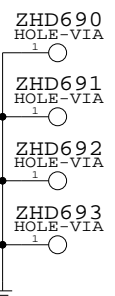
B

A

A



SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING



ETHERNET CONNECTOR
 SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005
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SCALE	NONE	SHT	OF
		136	154

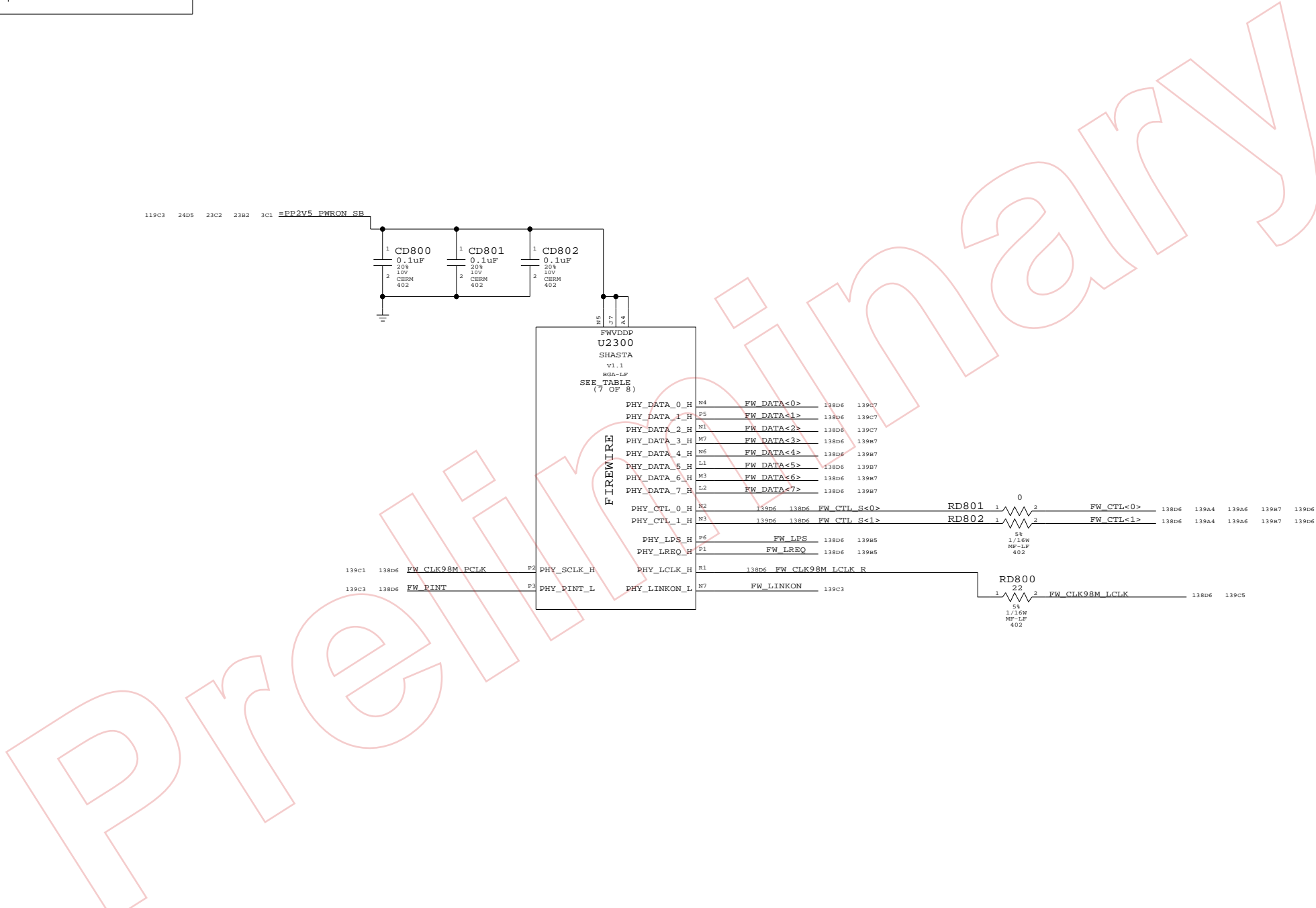
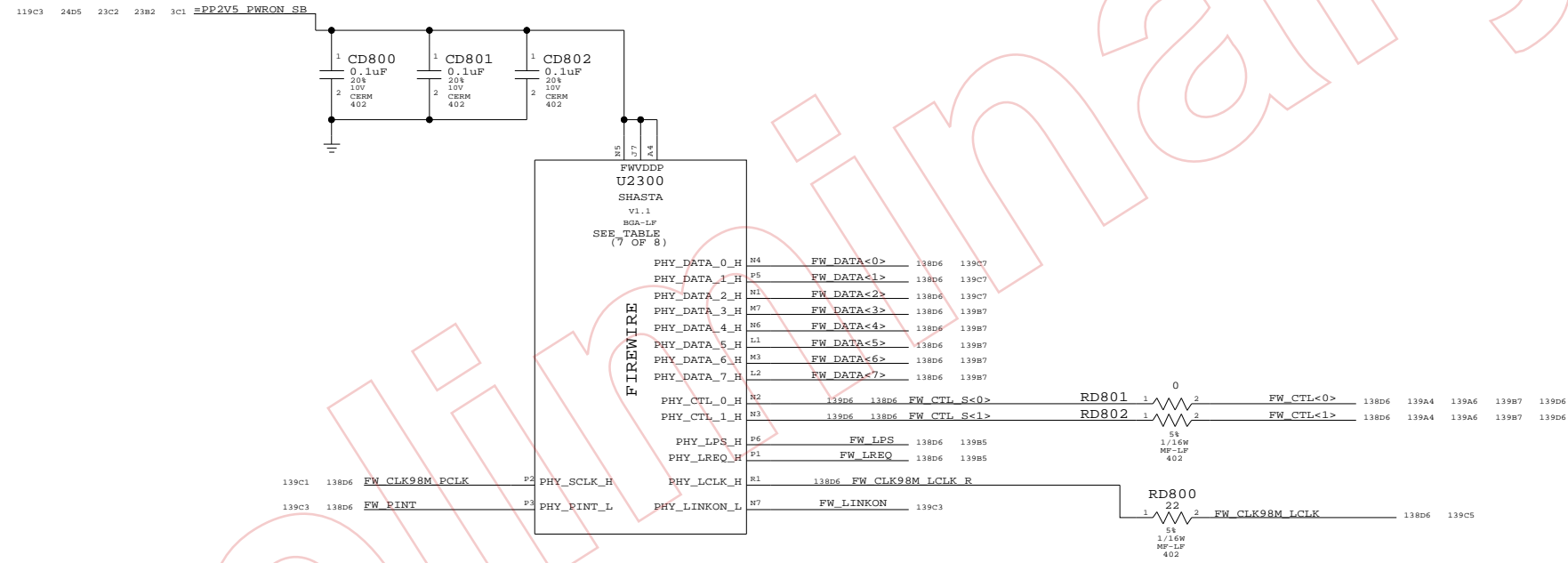
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	ENET_FW_2X	FW_DATA<7..0>
	ENET_FW_3X	FW_CTL_S<1..0>
	ENET_FW_3X	FW_CTL<1..0>
	ENET_FW_2X	FW_DATA_R<7..0>
	ENET_FW_3X	FW_CTL_R<1..0>
	ENET_FW_3X	FW_LPS
	ENET_FW_3X	FW_LREQ
	ENET_FW_3X	FW_PINT
	0.38mm SPACING	FW_CLK98M_LCLK
	0.38mm SPACING	FW_CLK98M_PCLK
	0.38mm SPACING	FW_CLK98M_LCLK_R

Page Notes

Power aliases required by this page:
 - _PP2V5_PWRON_SB

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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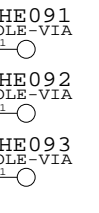
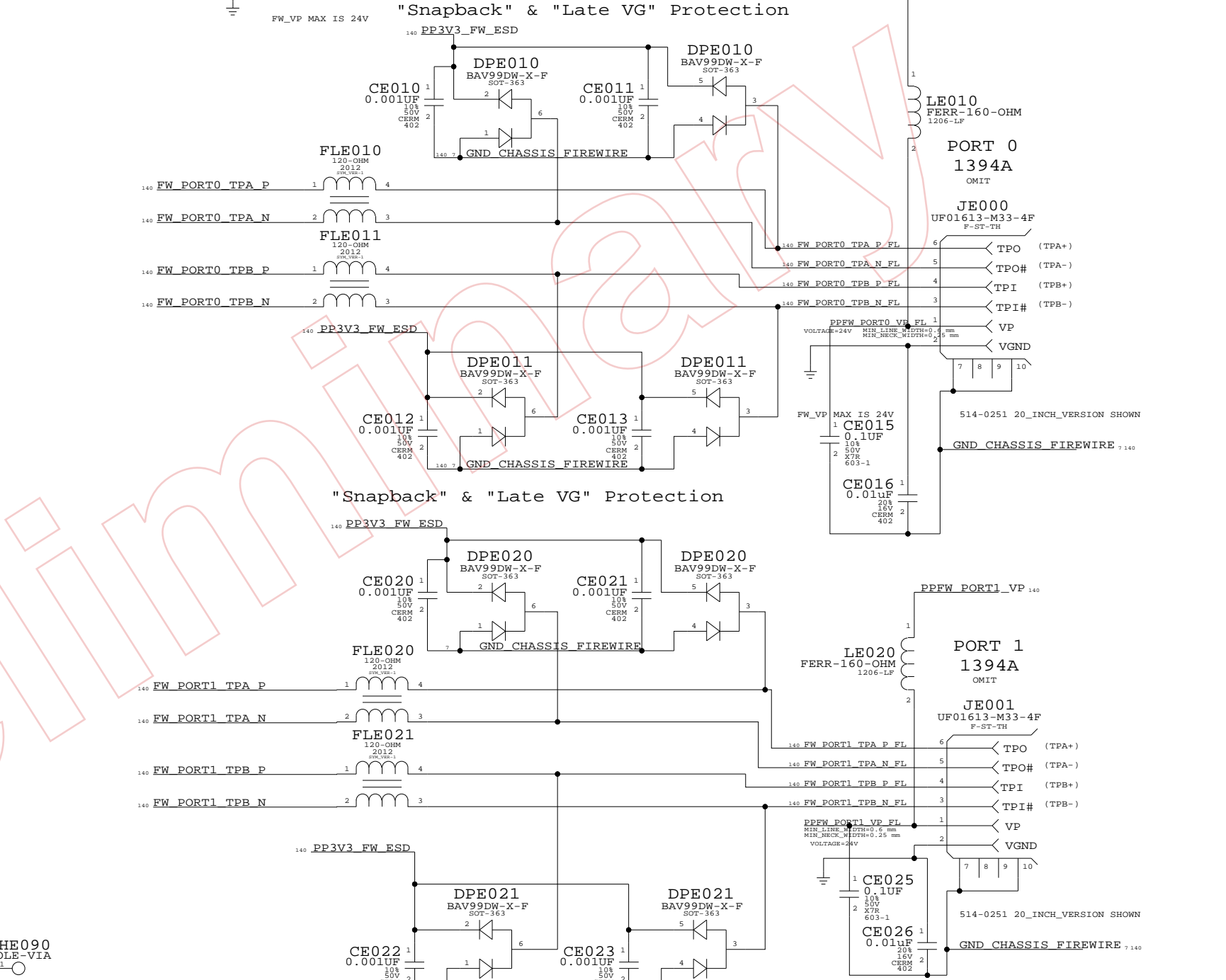
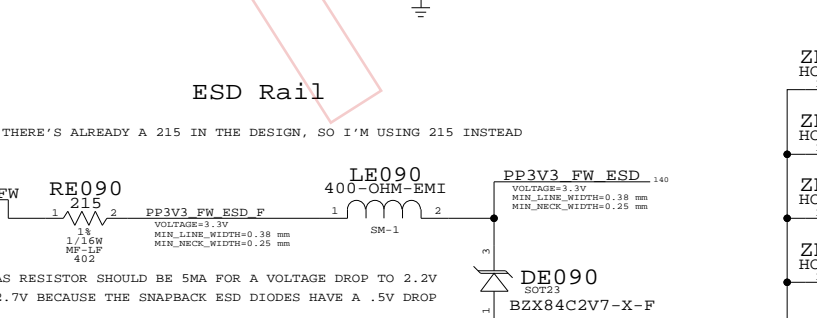
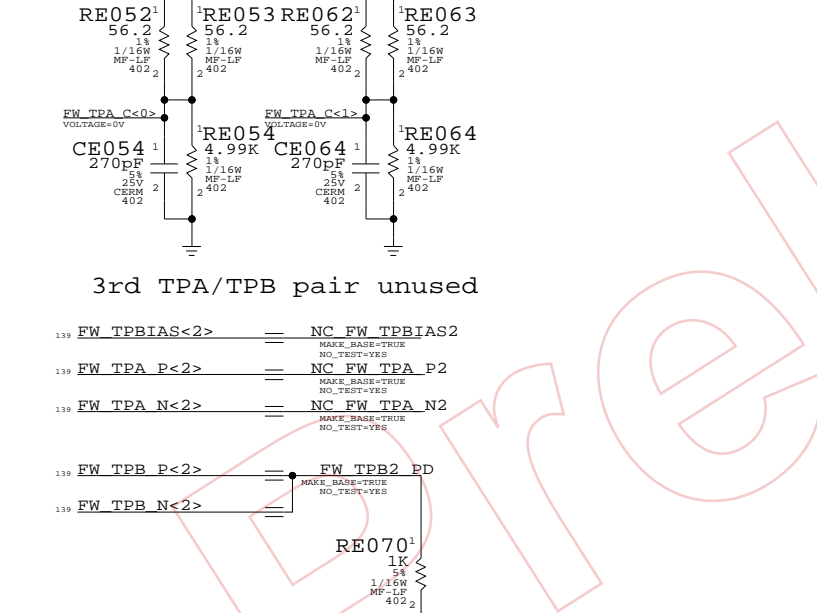
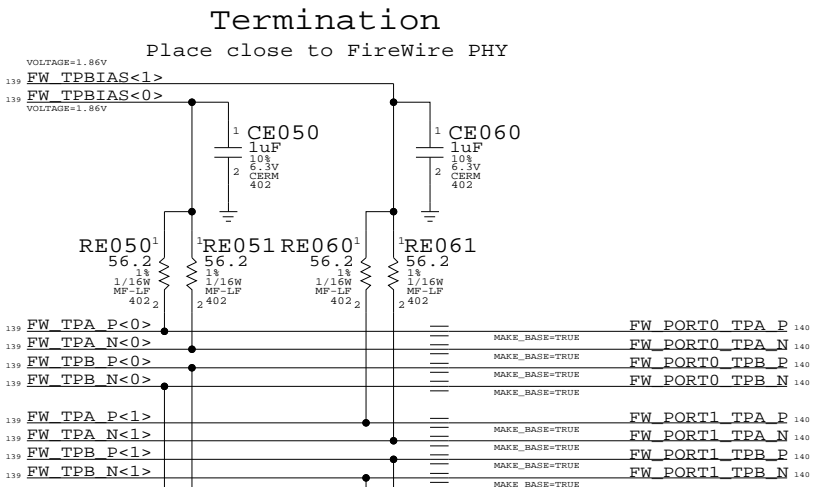
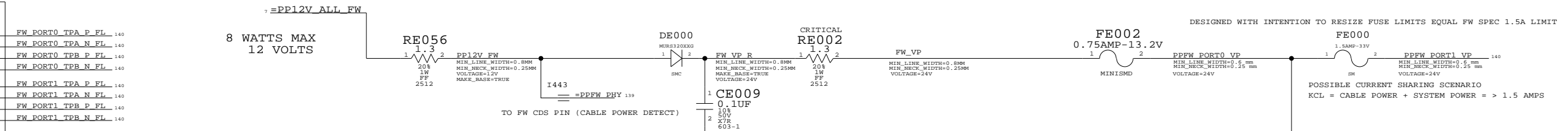
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SCALE		SHT	OF
NONE		138	154

NET_TYPE		
SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FW	FW	FW_TPA0_FL
FW	FW	FW_TPA0_FR
FW	FW	FW_TPB0_FL
FW	FW	FW_TPB0_FR
FW	FW	FW_TPA1_FL
FW	FW	FW_TPA1_FR
FW	FW	FW_TPB1_FL
FW	FW	FW_TPB1_FR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON, 1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-HC SYNC_DATE=05/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT	OF	154
NONE	140		

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_3
	USB2	USB2_S	USB2_3
	USB2	USB2_S	USB2_4
	USB2	USB2_S	USB2_4
	0.38mm SPACING		NEC_CLK30M_XT1
	0.38mm SPACING		NEC_CLK30M_XT2
	0.38mm SPACING		NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

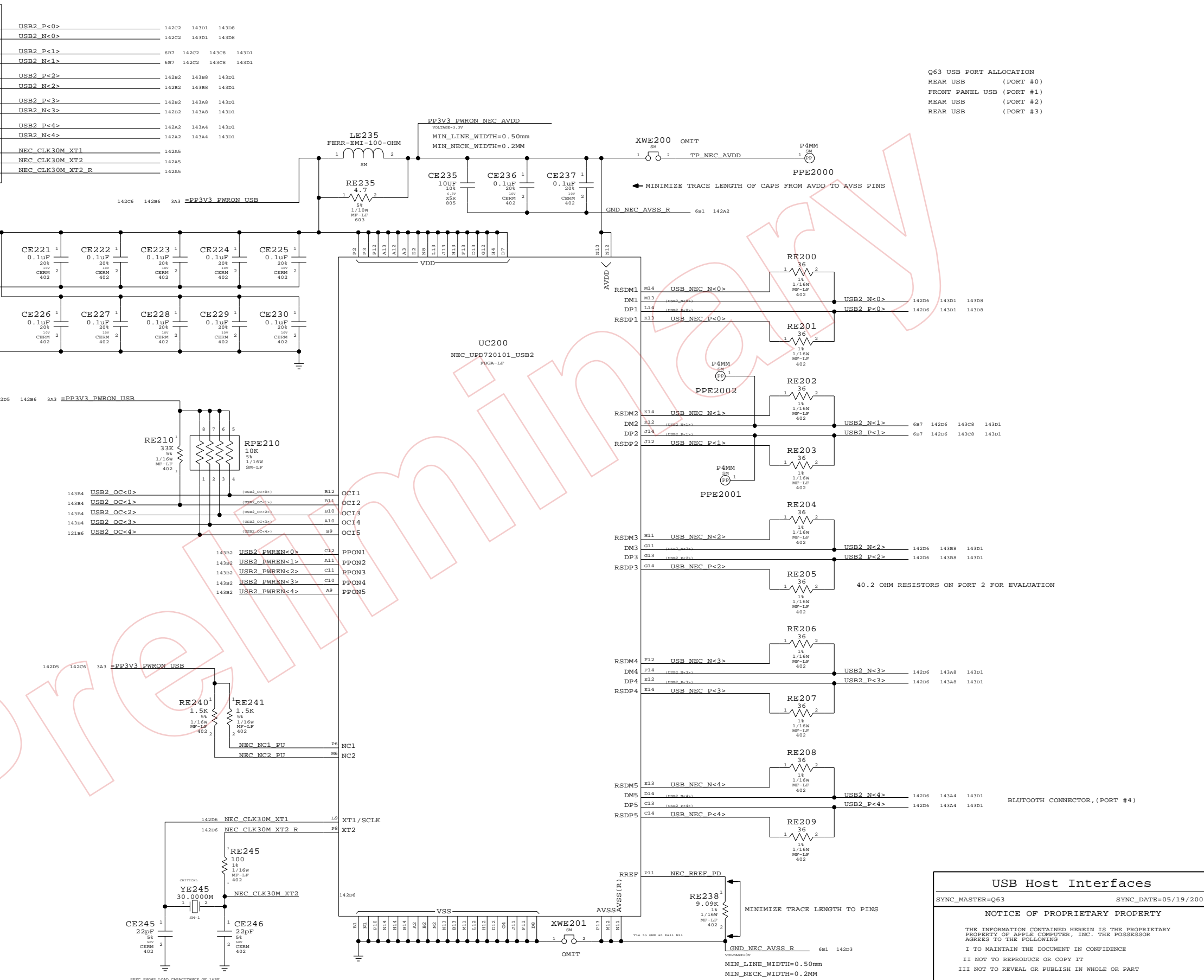
Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

U2300
SHASTA
V1.1
BGA-LF
(8 OF 8)

NC0	F7	TP_SB<0>
NC1	F8	TP_SB<1>
NC2	E3	TP_SB<2>
NC3	R4	TP_SB<3>
NC4	R5	TP_SB<4>
NC5	R6	TP_SB<5>
NC6	E7	TP_SB<6>
NC7	E8	TP_SB<7>
NC8	T1	TP_SB<8>
NC9	T2	TP_SB<9>
NC10	T3	TP_SB<10>
NC11	T4	TP_SB<11>
NC12	T5	TP_SB<12>
NC13	T6	TP_SB<13>
NC14	T7	TP_SB<14>
NC15	T8	TP_SB<15>
NC16	U1	TP_SB<16>
NC17	U2	TP_SB<17>
NC18	U3	TP_SB<18>
NC19	U4	TP_SB<19>
NC20	U5	TP_SB<20>
NC21	U6	TP_SB<21>
NC22	V1	TP_SB<22>
NC23	V2	TP_SB<23>
NC24	V3	TP_SB<24>
NC25	V4	TP_SB<25>
NC26	W1	TP_SB<26>
NC27	W3	TP_SB<27>
NC28	Y1	TP_SB<28>
NC29	Y3	TP_SB<29>



Q63 USB PORT ALLOCATION

REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

USB Host Interfaces

SYNC_MASTER=Q63 SYNC_DATE=05/19/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6863	07
SCALE	SHT	OF
NONE	142	154

Page Notes

Power aliases required by this page:

- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

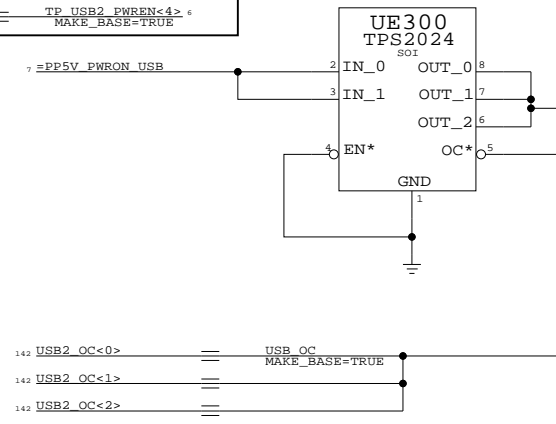
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

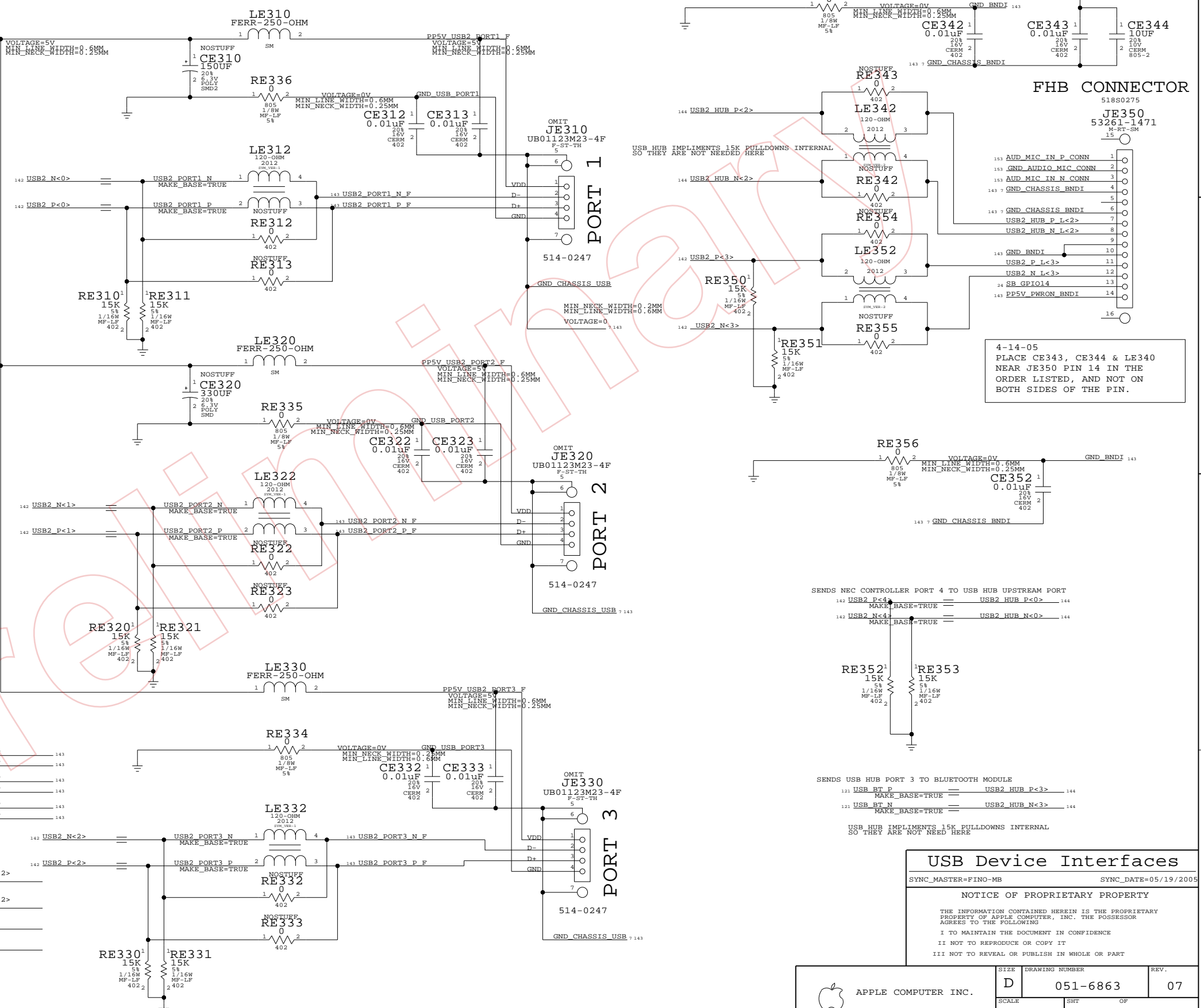
- 142 USB2_PWRN<0> == TP_USB2_PWRN<0> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<1> == TP_USB2_PWRN<1> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<2> == TP_USB2_PWRN<2> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<3> == TP_USB2_PWRN<3> 6 MAKE_BASE=TRUE
- 142 USB2_PWRN<4> == TP_USB2_PWRN<4> 6 MAKE_BASE=TRUE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0247	3	USB RECEPTACLE,4P,UB1123-M23-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0250	3	USB RECEPTACLE,4P,UB1123-M33-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE
PROVIDED	USB2	USB2_PORT1_F	USB2 USB2_PORT1_P_F 143
BY	USB2	USB2_PORT1_F	USB2 USB2_PORT1_N_F 143
USB	USB2	USB2_PORT2_F	USB2 USB2_PORT2_P_F 143
CONTROLLER	USB2	USB2_PORT2_F	USB2 USB2_PORT2_N_F 143
	USB2	USB2_PORT3_F	USB2 USB2_PORT3_P_F 143
	USB2	USB2_PORT3_F	USB2 USB2_PORT3_N_F 143
	USB2	USB2_HUB_F	USB2 USB2_HUB_P_L<2>
	USB2	USB2_HUB_F	USB2 USB2_HUB_N_L<2>
	USB2	USB2_BNDI_F	USB2 USB2_P_L<3>
	USB2	USB2_BNDI_F	USB2 USB2_N_L<3>

External USB Ports



USB Device Interfaces

SYNC_MASTER=FINO-MB SYNC_DATE=05/19/2005

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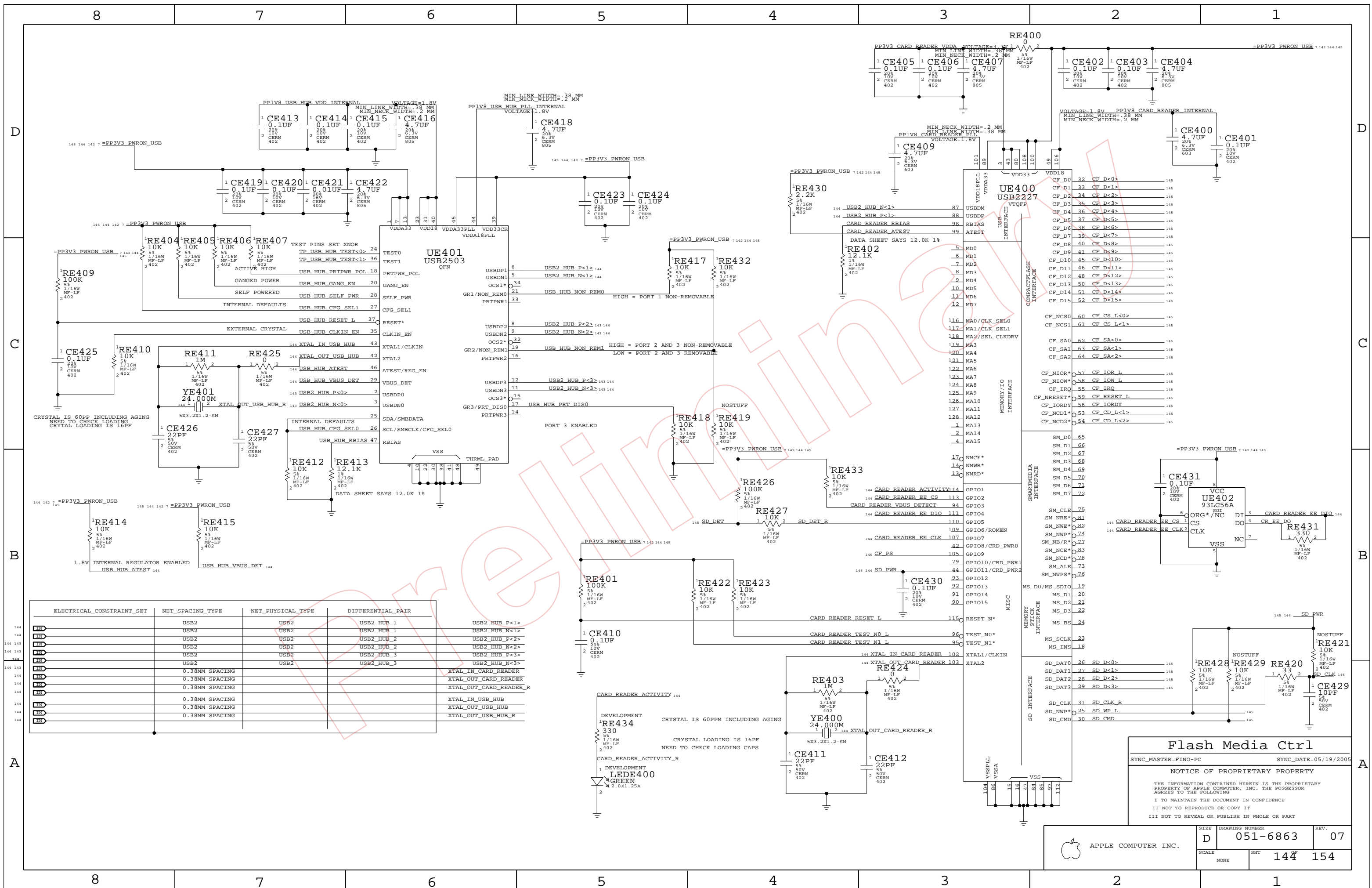
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	D	051-6863	07
SCALE	SHEET	OF	
NONE	143	154	



ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
MIN	USB2	USB2	USB2_HUB_1
MIN	USB2	USB2	USB2_HUB_2
MIN	USB2	USB2	USB2_HUB_3
MIN	0.38MM SPACING	USB2	XTAL_IN_CARD_READER
MIN	0.38MM SPACING	USB2	XTAL_OUT_CARD_READER
MIN	0.38MM SPACING	USB2	XTAL_OUT_CARD_READER_R
MIN	0.38MM SPACING	USB2	XTAL_IN_USB_HUB
MIN	0.38MM SPACING	USB2	XTAL_OUT_USB_HUB
MIN	0.38MM SPACING	USB2	XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

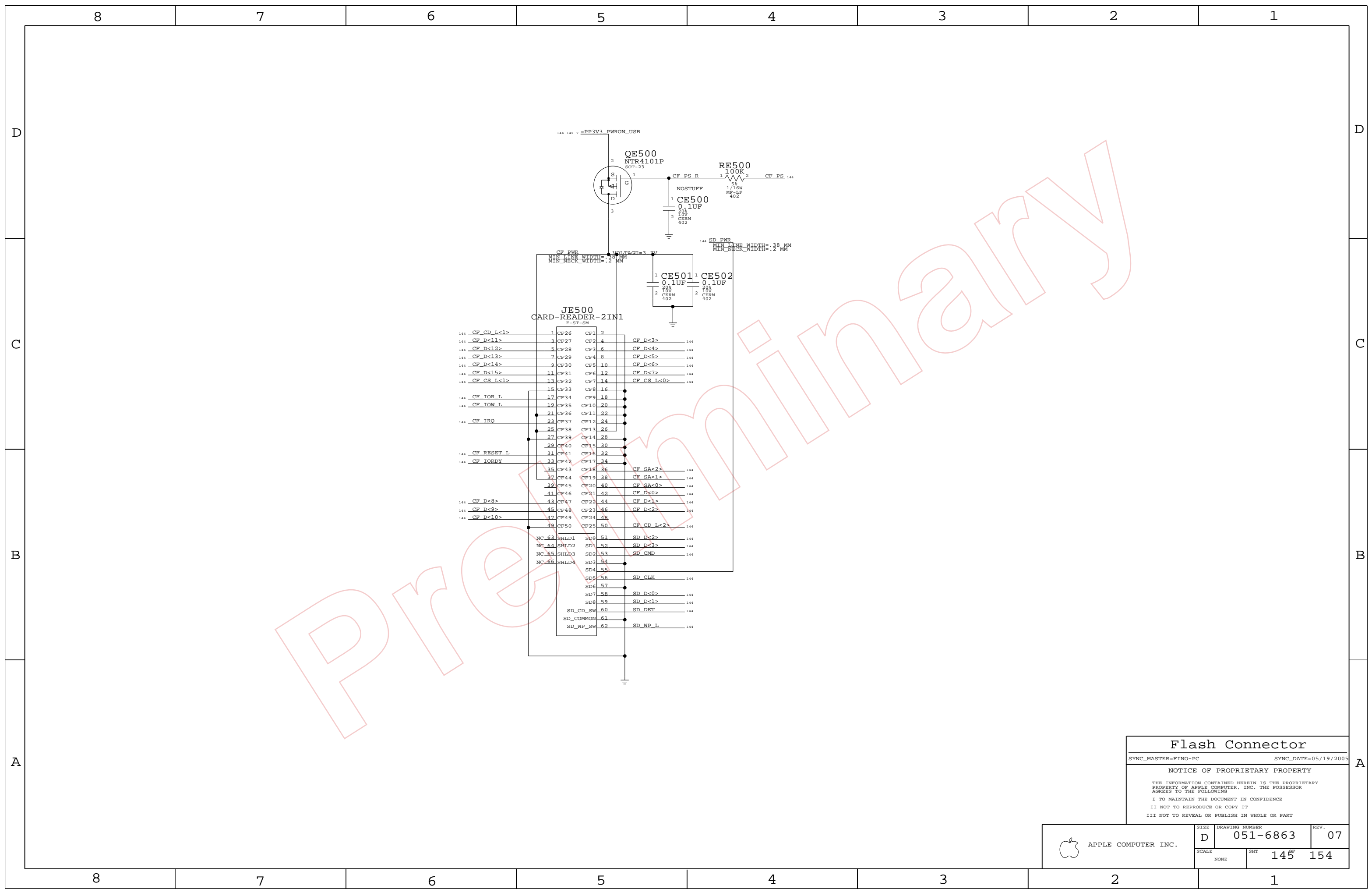
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Pre-ministry

Flash Connector

SYNC_MASTER=FINO-PC SYNC_DATE=05/19/2005

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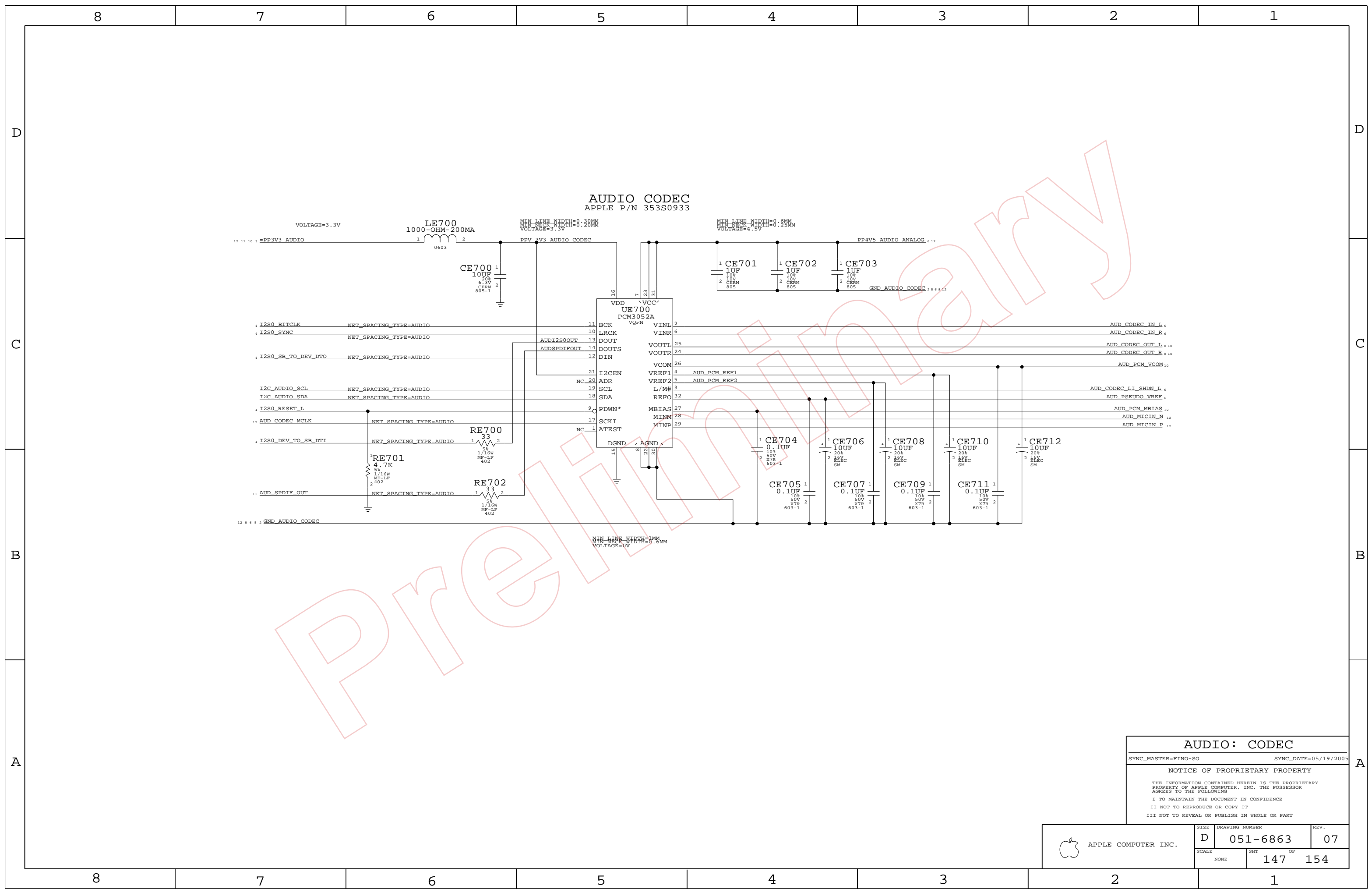
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	D	051-6863	07
SCALE		SHT	REV.
NONE		145	154



AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

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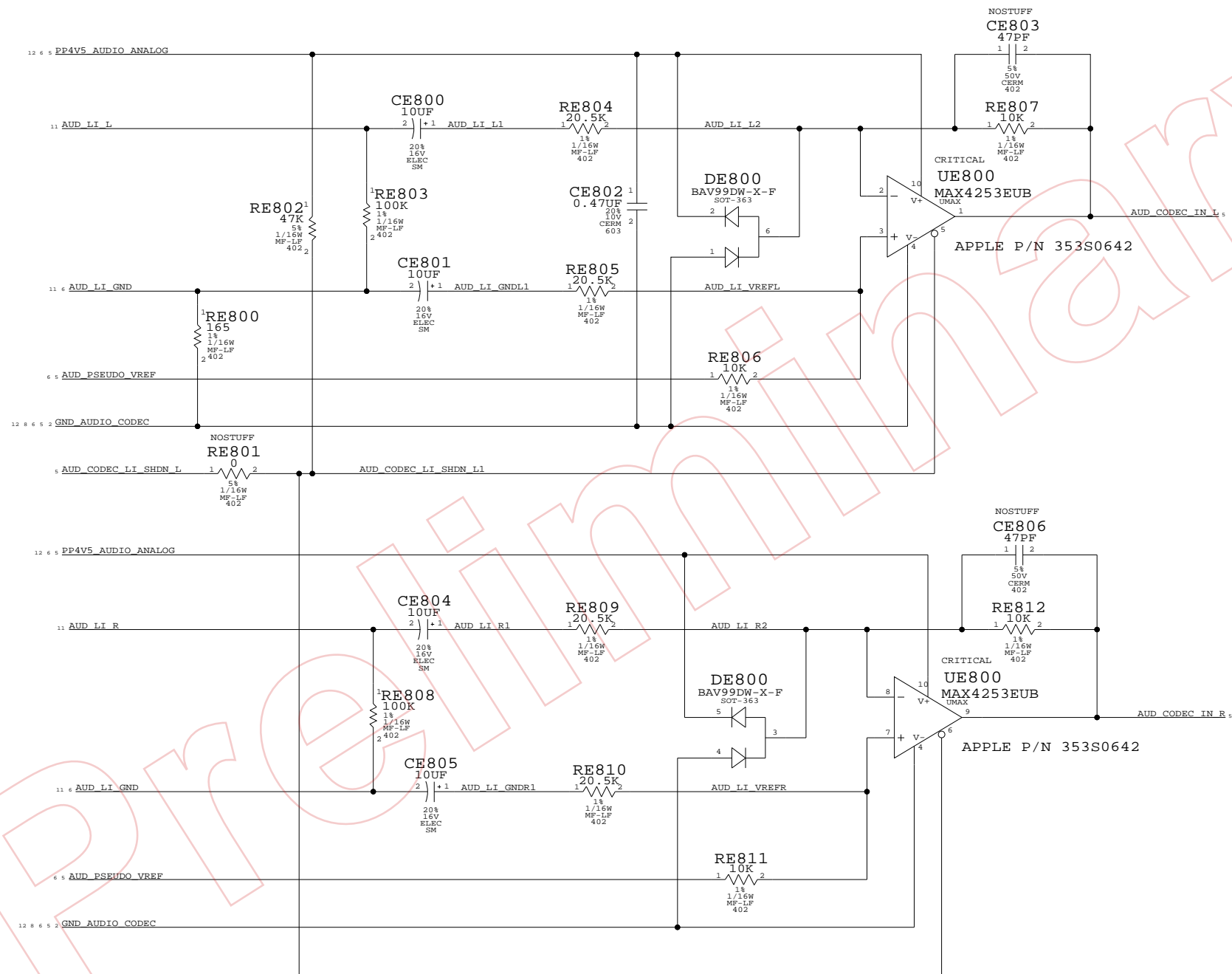
II NOT TO REPRODUCE OR COPY IT

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	SHT OF		
NONE	147	154	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49




AUDIO: LINE INPUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005

NOTICE OF PROPRIETARY PROPERTY

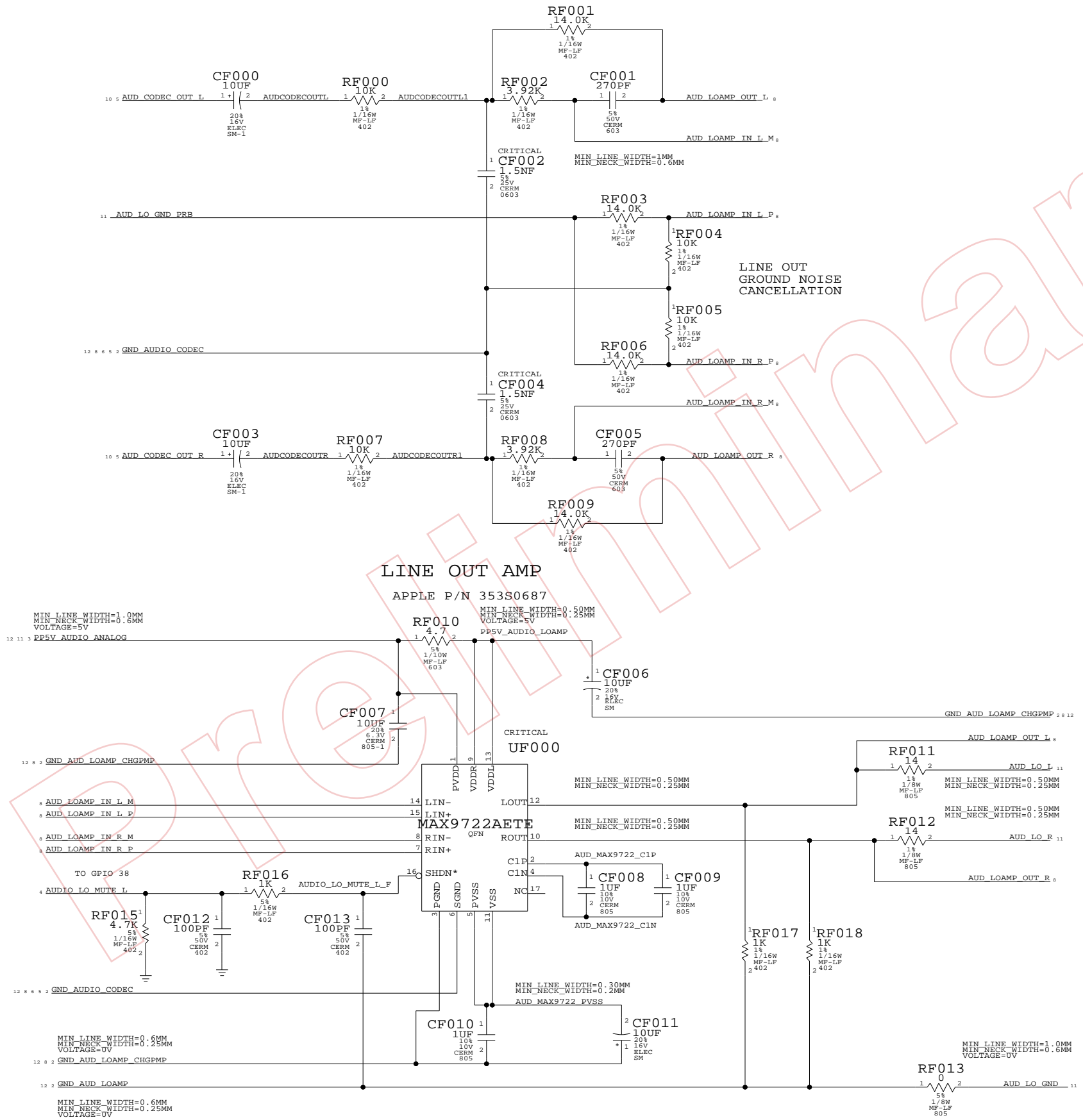
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	NONE	D 051-6863	07
SCALE		SHT	OF
NONE		148	154

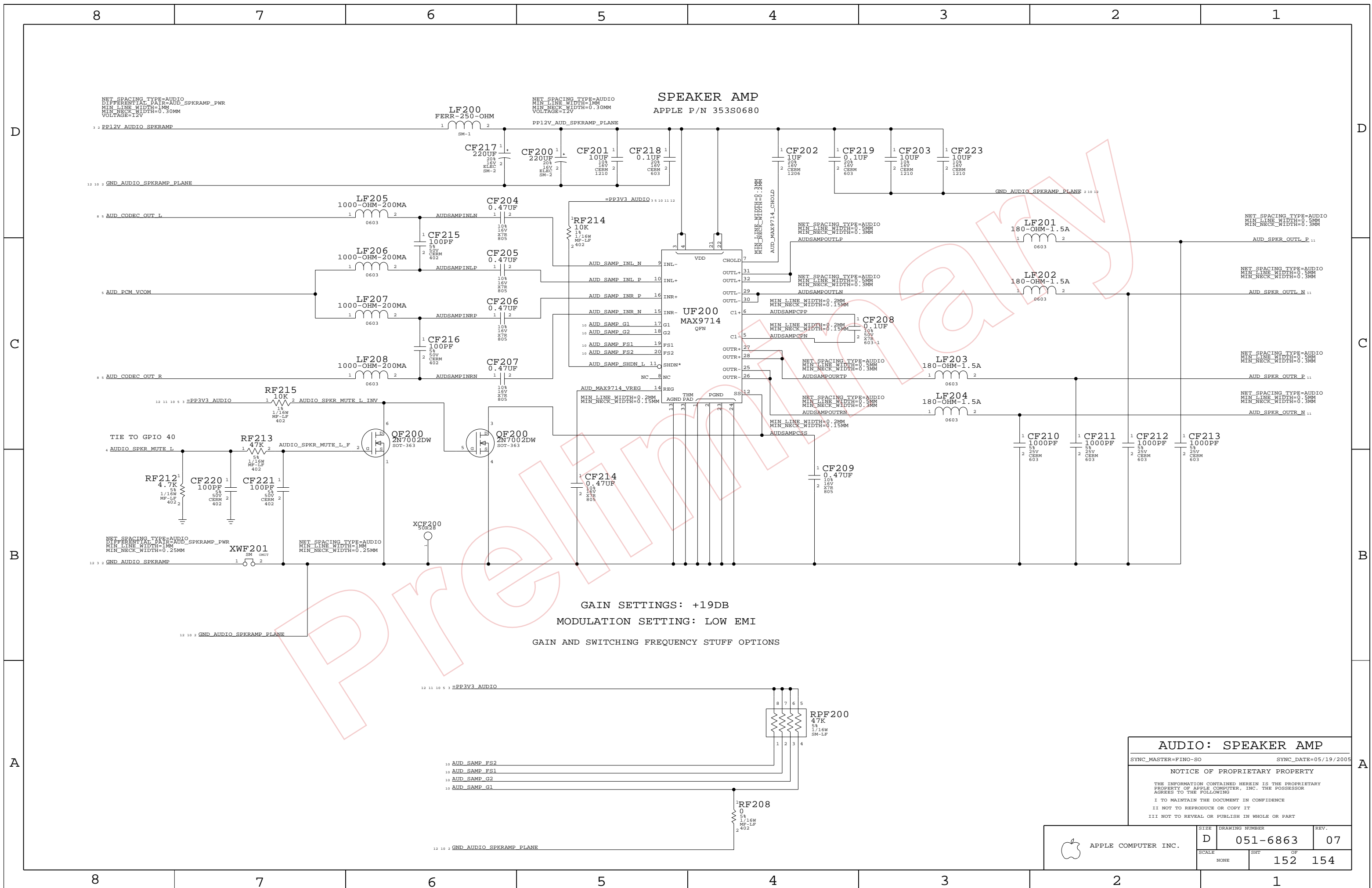
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



AUDIO: LINE OUT AMP
 SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005
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SCALE	SHT OF		
NONE	150		154

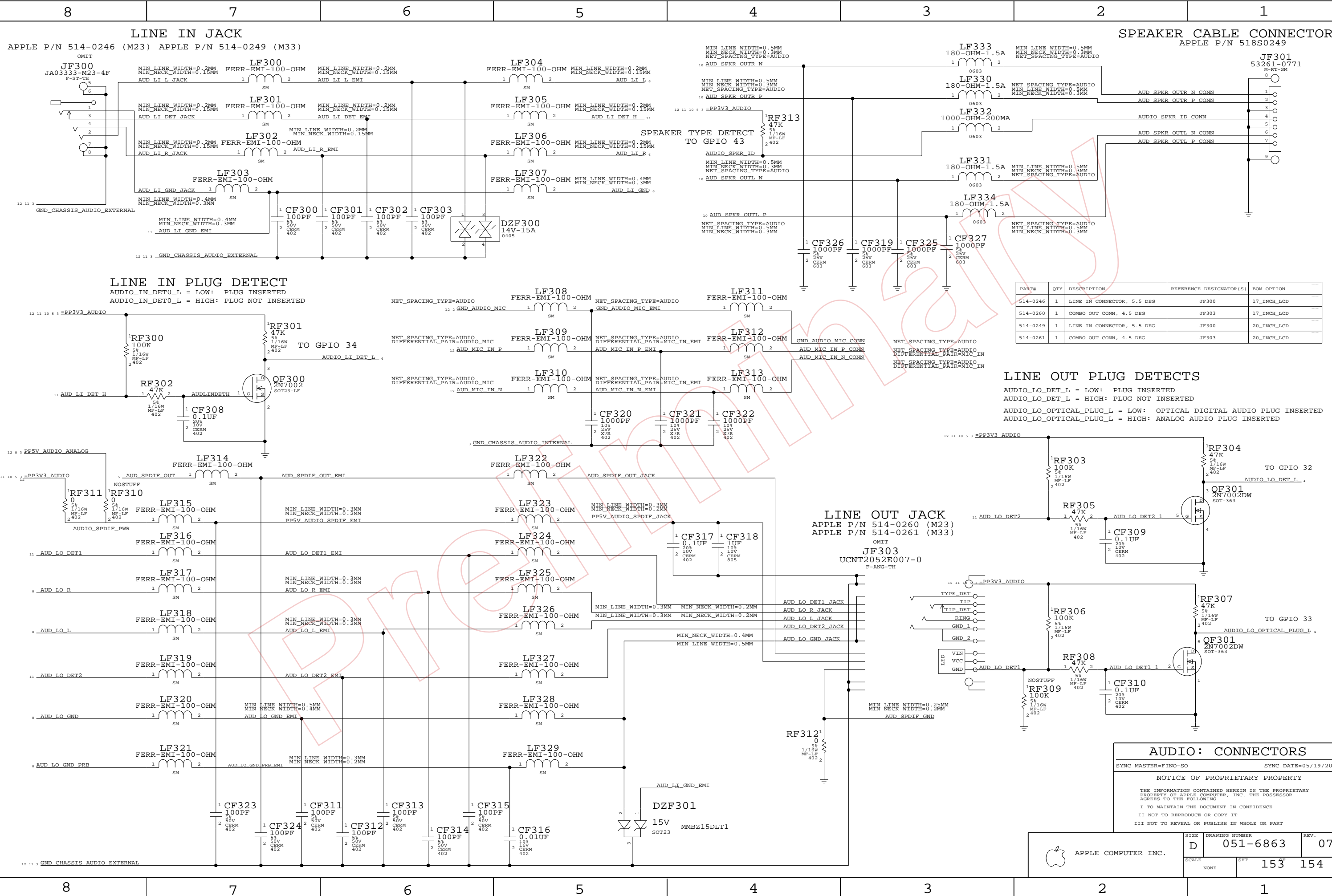


SPEAKER AMP
APPLE P/N 353S0680

GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6863	07
SCALE	NONE	SHT	OF
		152	154



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS
 AUDIO_LO_DET_L = LOW: PLUG INSERTED
 AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED
 AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
 AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

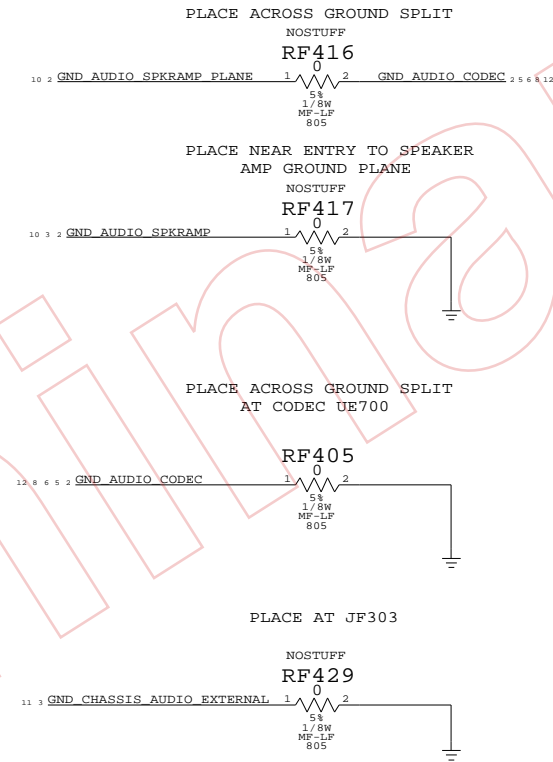
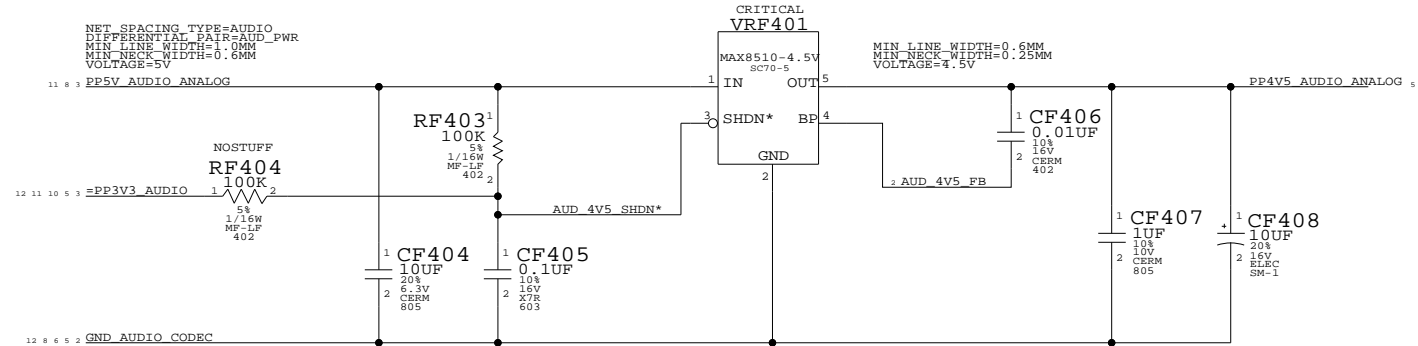
AUDIO: CONNECTORS
 SYNC_MASTER=FINO-SO SYNC_DATE=05/19/2005
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SCALE	SHT	153	154
NONE			

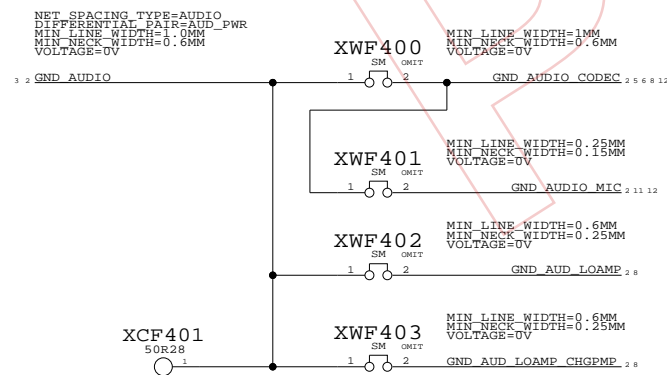
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35380655	35380933		U9500	PCM3052

UNUSED GPIO TERMINATIONS

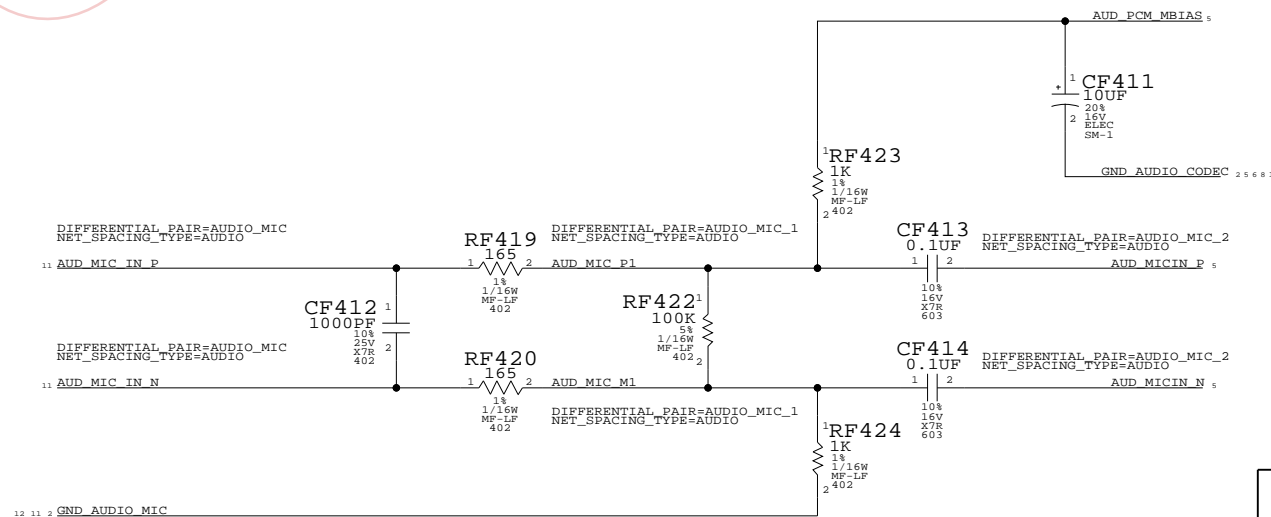
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APPLE P/N 353S0733



AUDIO GROUND RETURNS



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

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SCALE	NONE	SHT OF	154 OF 154