1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SEEDY
12/07/04

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
04		354713	ENGINEERING RELEASED	12/07/04	?

CSA	PDF	CIRCUIT	BLOCK
1	1	TABLE OF CONTENTS	TOP
2	2	SYSTEM BLOCK DIAGRAM	
3	3	POWER BLOCK DIAGRAM	
4	4	REVISION HISTORY	
5	5	TABLE ITEMS	
6	6	FUNC TEST	
7	7	POWER CONNECTOR / POWER ALIAS	
8	8	SIGNAL ALIAS	
9	9	2.5V VREG	
10	10	1.2V VREG	
11	11	3.3V/5V PWRON SWITCHING	
12	12	VESTA POWER	
13*	13	SMU	
14	14	CPU LOGIC ANALYZER CONNECTOR	
16	15	FAN 0, 1 AND SYSTEM TEMP SENSOR	
17	16	FAN 2 AND HARD DRIVE TEMP SENSOR	
18	17	I2C CONNECTIONS	
21	18	INDICATOR LED / AMBIENT LIGHT SENSOR	
22	19	1.5V VREG / U3LITE CORE	
23	20	SHASTA CORE	
24	21	U3LITE MISC	
25*	22	SHASTA SERIAL	
26	23	PULSAR POWER	
27	24	PULSAR CLOCKS	
28	25	U3LITE APPLE PI	PROCESSOR
29	26	NEO APPLE PI	
30	27	CPU STRAPS	
31	28	NEO POWER & BYPASS	
32	29	CPU BYPASS	
33	30	CPU VREG	
34	31	CPU VREG	
35	32	CPU VREG OUTPUT CAPS	
36	33	CPU DIODE CONDITIONER	
37	34	U3LITE MEMORY	MEMORY
38	35	SERIES TERMINATION	
40	36	DIMMS	
44	37	PARALLEL TERMINATION	
45	38	PARALLEL TERMINATION	
46	39	VTT VREG	
48	40	U3LITE AGP	GRAPHICS
49	41	GPU AGP	
50	42	GRAPHICS VREGS	

CSA	PDF	CIRCUIT	BLOCK
51	43	GPU CORE POWER	GRAPHICS
52	44	GPU FRAME BUFFER	
53	45	FRAME BUFFER TERMINATION	
54	46	GRAPHICS DDR SDRAM A	
55	47	GRAPHICS DDR SDRAM B	
56	48	GPU STRAPS	
58	49	GPU DVI & DACS	
59	50	EXT VGA & TMDS	
60	51	U3LITE HYPERTRANSPORT	HT
62*	52	SHASTA HYPERTRANSPORT	
64	53	HYPERTRANSPORT LA CONNECTORS	
73	54	PCI SERIES TERMINATION	PCI
74*	55	SHASTA PCI	
75*	56	BOOT ROM	
76	57	AIRPORT EXTREME & BLUETOOTH	
77*	58	USB2 PCI	
80*	59	SHASTA DISK	DISK
83	60	DISK CONNECTORS	
84*	61	SHASTA ETHERNET	ETHERNET
86*	62	VESTA ETHERNET PHY	
87	63	ETHERNET CONNECTOR	
88*	64	SHASTA FIREWIRE	FIREWIRE
89*	65	VESTA FIREWIRE PHY	
90	66	FIREWIRE CONNECTORS	
91*	67	USB HOST INTERFACE	USB
92	68	USB DEVICE INTERFACE	
94	69	MODEM CONNECTOR	MODEM
95*	70	PCM3052A AUDIO CODEC	AUDIO
96*	71	LINE IN AMP	
98*	72	LINE OUT AMP	
100*	73	SPEAKER AMP	
101*	74	AUDIO CONNECTORS	
102*	75	AUDIO POWER SUPPLIES	

* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK
ENG APPD | MFG APPD
QA APPD | DESIGNER
RELEASE | SCALE NONE
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

Apple Computer Inc.

TITLE: SCH,MLB,SEEDY

DRAWING NUMBER 051-6772 | REV. 04

SHT 1 OF 102

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE

U2900
CPU
NEO 10S
PAGE 29

32-BIT
APPLE PI
ELASTIC INTERFACE
1.2V/900MHZ

U1300
SMU
PAGE 13

U1301
RTC
PAGE 13

J5900, J5901
J5902, J5903
17",20" INVERTER
TMDS
EXT VGA
PAGE 59

U5400, U5401
FRAME
BUFFER A
PAGE 54

64-BIT
FRAME BUFFER
2.6V/400MHZ

U4900
GPU
RV351LE
PAGE 49

32-BIT
8X AGP
0.8V/533MHZ
4X = 1.5V
I/O = 1.5V

APPLE PI
PAGE 28

AGP
PAGE 48

U3
U3LITE
CORE
PAGE 22

MAIN MEMORY
PAGE 37

64/128-BIT
MAIN MEMORY
2.6V/400MHZ

SERIES
TERM
PAGE 38

J4000
J4001
DIMMS
PAGE 40

PARALLEL
TERM
PAGES 44&45

64-BIT
FRAME BUFFER
2.6V/400MHZ

U5500, U5501
FRAME
BUFFER B
PAGE 55

MISC
PAGE 24

HYPERTRANSPORT
PAGE 60

8-BIT
HYPERTRANSPORT
1.2V/800MHZ
CONTROL = 2.5V

J9210/J9220/J9230
USB
CONNECTORS
PAGE 92

U2600
PULSAR
POWER
PAGE 26
CLOCKS
PAGE 27

I2C
PAGE 18

J6400
J6401
J6402
HT
DEBUG
PAGE 64

J9240
BLUETOOTH
CONNECTOR
PAGE 92

1 2 3 4 5
USB
PAGE 91

U7700
USB 2.0
uPD720101
PCI
PAGE 77

U7500
BOOTROM
PAGE 75

J7600
AIRPORT
EXTREME
CONNECTOR
PAGE 76

HARD DRIVE

JXXXX
SATA
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

HYPERTRANSPORT
PAGE 62

SATA1
SATA
PAGE 80

U2300

PCI
PAGE 74

32-bit PCI (5V-3.3V/33MHz)

FOR DEVELOPMENT ONLY

J8302
SATA DEV
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA2

SHASTA

GPIO/PCI64
PAGE 25

OPTICAL

J8301
UATA
CONNECTOR
PAGE 83

UATA/133
3.3V/133MHZ

UATA
PAGE 80

CORE
PAGE 23

NCS
PAGE 91

J9401
CTL-LESS /
SOFT MODEM
CONNECTOR
PAGE 94

ETHERNET
PAGE 84

FIREWIRE
PAGE 88

I2S
PAGE 25
I2S0
SCCA
I2S1
SCCB
I2S2

GMII (3.3V/125MHz)
8-bit Tx
8-bit Rx

1394 PHY 8-bit (3.3V/98MHz)
Tx
Rx

U9500
AUDIO CODEC
PCM3052A
PAGE 95

S/PDIF

OPTICAL OUT
J9803
COMBO OUT
CONNECTOR
PAGE 98

LINE OUT
AMP
PAGE 97

LINE OUT

SPEAKER
AMP
PAGE 97

J9801
SPEAKER
CONNECTOR
PAGE 98

U8600
VESTA
GIG ETHERNET
PAGE 86
FIREWIRE A
PAGE 89
0 1

4 Diff pairs

2 Diff pairs

LINE IN
AMP
PAGE 97

J8700
ETHERNET
CONNECTOR
PAGE 87

J9000, J9001
FIREWIRE A
CONNECTORS
PAGE 90

J9800
LINE IN
CONNECTOR
PAGE 98

J9802
MIC
CONNECTOR
PAGE 98

SYSTEM BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 04

SCALE NONE | SHT 2 OF 102

POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP24V_RUN — FW CONN, 20" LCD INVERTER

PP12V_RUN — 20" PANEL POWER, 20" LCD INVERTER

PP5V_RUN — HDD & OPTICAL

PP5V_ALL

PP3V3_RUN — PCI BUS, AUDIO CODEC

SMU

SYS_POWERUP_L
POWER SEQUENCE PIN

PULSAR_POWER_DOWN
MAKE_BASE=TRUE
27 =PULSAR_POWER_DOWN

TP_SMU_PWRSEQ_P1_0
MAKE_BASE=TRUE

10 TURN_ON_PP1V2_PWRON_L

SMU_PWRSEQ_P1_4 13
SMU_PWRSEQ_P1_0 13
SMU_PWRSEQ_P1_1 13
SMU_PWRSEQ_P9_5 13 (PWR_GOOD_SB_CORE)
SMU_PWRSEQ_P9_6 13 (PWR_GOOD_PP2V5)
SMU_PWRSEQ_P1_2 13 (TURN_ON_VTT)

5V

PP5V_RUN_AUDIO LINEAR
PAGE 99
5V — HP/LINEOUT AMP

PP4V5_RUN_AUDIO LINEAR
PAGE 99
4.5V — AUDIO CODEC

CPU CORE SWITCHER
PAGE 33 SC1211 4
SC2643VX*1
0.8~1.2V — GPUL

=PP5V_RUN_CPU 6 7 8 31
ALIAS CPU_AVDD_EN 31

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 31
2.8V — CPU AVDD

PP5V_PWRON FET SWITCH
PAGE 11
5V — USB CONN

PP3V3_ALL LINEAR
PAGE 11
3.3V — FW PHY, SMU

PP3V3_PWRON FET SWITCH
PAGE 11
3.3V — ENET PHY, USB2 HOST, MODEM & BT

GPU CORE SWITCHER
PAGE 50 IRU3037ACS
1.20V — RV351

PP2V5_GPU_A2VDD LINEAR
PAGE 50 — GPU

PP1V2_ALL SWITCHER
PAGE 10 IRU3037ACS
1.2V — VESTA CORE

PP1V8_TPVDD LINEAR
PAGE 50 GPU

PP1V5_VDDC_CT LINEAR
PAGE 50 GPU

U3LITE CORE SWITCHER
PAGE 22 IRU3037CS
1.53V — U3LITE CORE

PP2V5_PWRON SWITCHER
PAGE 9 IRU3037CS
2.59V — SHASTA HT, DDR DIMM

PP2V5_PWRON

PP1V2_PWRON FET SWITCH
PAGE 10
SHASTA CORE
PWRON_SD
PWRON_DISK_SB
23 7 6 =PPVCORE_PWRON_SB

PP1V2_RUN FET SWITCH
PAGE 10
HT BUS

PP2V5_RUN FET SWITCH
PAGE 9
RAM TERM, GRAPHIC FB

PP1V25_RAM_VTT LINEAR
PAGE 46
1.3V — RAM VTT

PP1V5_PWRON LINEAR
PAGE 50
1.5V — PULSAR CORE

PP1V8_GPU LINEAR
PAGE 50
GPU

PP1V5_RUN POWER SW
PAGE 50
AGP BUS

46 TURN_ON_VTT

PP3V3_ALL
R331 10K 5% 1/16W MF-LF 402
PWR_GOOD_SB_CORE

11 RAIL_CTL_NEG
R330 100K 5% 1/10W MF-LF 402
COMPARE_SB_CORE
C330 0.01UF 20% 16V CERM 402
U1100 LM339A SOI

PP5V_ALL
R342 150K 5% 1/16W MF-LF 402
PS_2V_REF
R340 100K 5% 1/16W MF-LF 402
COMPARE_PP2V5
C340 0.01UF 20% 16V CERM 402
R343 100K 5% 1/16W MF-LF 402
U1100 LM339A SOI

PP3V3_ALL
R341 10K 5% 1/10W MF-LF 402
PWR_GOOD_PP2V5

POWER BLOCK DIAGRAM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT	OF
NONE	3	102

DATE	DESCRIPTION
10/20/04	CLONED DESIGN FROM GILA (Q45 A/B) REV G CHECKIN 00002
10/21/04	ADDED VESTA ADDED 1.2V REGULATOR FOR VESTA CORE ADDED 2.5V LDO FOR VESTA ADDED FW LATE VG PROTECTION REMOVED BCM5231 ETHERNET PHY REMOVED FW802A FW PHY REMOVED FW PORT POWER CIRCUITRY REMOVED MICRODASH CONNECTOR CHECKIN 00003
10/22/04	REMOVED NV18/34 GPU REMOVED AGP VREG (VR5001) REMOVED GPU VTT VREG ADDED 2.5V VREG FOR A2VDD REMOVED EXTERNAL TMDS TRANSMITTER ADDED RV351LE GPU CHECKIN 00004
10/26/04	GPU CORE POWER UPDATES ADDED VESTA ETHERNET LOWPWR CIRCUIT ADDED DEVELOPMENT LEDS FOR VESTA ENET CHECKIN 00005
10/28/04	CONNECTED FRAME BUFFER ADDED 1.8V GPU VREG CONNECTED GPU TMDS AND VGA CONNECTED GPU POWER AND POWER FILTERS CHECKIN 00006
11/01/04	ADDED VOLTAGE, LINE WIDTH, AND NECK WIDTH PROPERTIES FOR GRAPHICS (IN MM) TIED PPVCORE_NB DIRECTLY TO PP1V5_PWRON (REMOVED R707) REPLACED EMC FERRITES WITH 0 OHM RESISTORS FOR GRAPHICS AND FANS REMOVED VESTA CORE REGULATOR REPURPOSED 1.2V REGULATOR FOR VESTA AND SHASTA CHANGED FW LATE VG CIRCUITRY TO MATCH Q78 & Q86 CHECKIN 00007
11/03/04	<RADAR 3848831> MOVED SMU RESET BUTTON TO DEVELOPMENT BOM <RADAR 3849762> MOVED SMU DOWNLOAD CONNECTOR TO DEVELOPMENT BOM <RADAR 3849798> REDUCED CAPACITANCE OF C1100 & C1102 MASTER PAGE SYNC: FRAME BUFFER SWAPS FOR CLEANER ROUTING REMOVED VESTA ROM AUDIO COST REDUCTIONS <RADAR 3849747 & 3849751> AUDIO 3052A CODEC ADDED 1.55V VREG FOR GPU VDDC_CT MOVED VTT VREG TO 2.5V PWRON TO REDUCE CURRENT THROUGH Q903 CHANGED FETS IN GPU CORE FOR COST REDUCTION ADDED SPACING & PHYSICAL CONSTRAINTS TO FRAME BUFFER CHECKIN 00008
11/04/04	REMOVED 1.6GHZ PROCESSORS CHANGED VOLTAGE SETTING OF 2.5V VREG TO 2.588V FROM 2.62V 1.2V VREG COST REDUCTIONS - Q1002 TO NTD60N02R; C1002/3 TO 10UF CERM U2850 - REMOVED MAXIM AS AN ALTERNATE MOVED GPU ZENER DIODES TO VREG PAGE SINCE THEY SHOULD BE PLACED NEAR THE VREGS ADDED 8MX32 GRAPHICS MEMORY ADDED GIGABIT ETHERNET CONNECTOR CHECKIN 00009
11/06/04	ADDED GPU STRAPS CONNECTED GPU GPIOS REMOVED ON BOARD POWER SUPPLY TEMP SENSOR ADDED AMBIENT LIGHT SENSOR CONNECTOR CONNECTED GPU TEMP SENSOR REMOVED CPU VREG 4TH PHASE ADDED DEVELOPMENT LEDS TO REGULATORS CHECKIN 00010
11/07/04	ADDED MORE GPU CONSTRAINTS <RADAR 3616348, 3621390> CHANGED FLS900-2 TO 220 OHM <RADAR 3848846> 2.5V RUN FET COST REDUCTION <RADAR 3848859> 1.2V, 1.5V RUN FET COST REDUCTIONS <RADAR 3848887> 5V & 3.3V PWRON FET COST REDUCTIONS <RADAR 3849622> STUFFED AROUND TMDS FILTERS <RADAR 3849656> STUFFED AROUND RGB FILTERS <RADAR 3849806> CHEAPER SMU CRYSTAL <RADAR 3849857> CHEAPER USB2 CRYSTAL BOM RELEASE REV 01
11/08/04	FRAME BUFFER PIN SWAPS <RADAR 3848846> UPDATE OF 2.5V RUN FET COST REDUCTION <RADAR 3849743> ADDED RESISTORS TO STUFF AROUND USB FILTERS CHECKIN 01001
11/09/04	<RADAR 3848850> REGULATOR COST REDUCTIONS <RADAR 3849767> 2.5V VREG COST REDUCTIONS <RADAR 3849772> REMOVED OUTPUT CAP ON 1.2V_ALL VREG <RADAR 3849820> SHASTA FILTER COST REDUCTION <RADAR 3849854> GPU CORE VREG COST REDUCTION <RADAR 3865344> SET GPU VDDC_CT VREG TO 1.55V CHECKIN 01002
11/10/04	CHANGED SOURCE OF Q1003 TO PP1V2_ALL RGB TERMINATION NOW CONNECTED TO DIGITAL GROUND WHITE LED - CHANGED INDUCTORS TO 0 OHM RESISTORS UPDATED POWER BLOCK DIAGRAM CHECKIN 01003 <RADAR 3848850> 2.5V VREG COST REDUCTION CHECKIN 01004
11/15/04	ADDED REGULATOR FOR GPU TPVDD ADDED POWER SEQUENCING FOR GRAPHICS REGULATORS ADDED TEST POINTS TO GRAPHICS FOR EXOR TESTING REMOVED EXTERNAL S/PDIF TRANSMITTER CHECKIN 01005
11/16/04	REMOVED P50 AIRPORT AND Q23 BLUETOOTH CONNECTORS, HOLES, & STANDOFFS ADDED Q85 AIRPORT & BLUETOOTH CONNECTOR CHECKIN 01006 (PP 16,17) REPLACED FAN CONTROL WITH NEW CIRCUIT (P 76) FINISHED CONNECTING Q85 CONNECTOR (P 7) ADDED PLATED HOLE ZH710 FOR TMDS GROUNDING (P 7) TIED BOTH EI RAILS TO 1.5V (P 5) NEW BOOTROM P/N (P 9) ADDED EXTRA 10UF INPUT CAP (P 12) VESTA_ENET_LOWPWR UPDATE (P 18) <RADAR 3878118> MOVED SMU I2C E BUS (P 22) CHANGED Q2250 TO 376S0143 (P 46) SLEEP SIGNAL TURNS OFF VTT VREG (P 58) REPLACED THERMAL SENSOR WITH LM63 (P 59) TIED UNUSED BUFFER ENABLE PINS HIGH (P 90) FIXED FW PORT NAMING (P 90) CHANGED R9090 TO 665 OHM (P 91) CHANGED USB2 CHIP GROUNDING (P 8) ALIASED VESTA JTAG TO TEST POINT NETS (P 9) <RADAR 3848846> ADDED PAD FOR 1NF CAP TO GATE OF Q903 CHECKIN 01007 / BOM RELEASE REV 02
11/18/04	ADDED PHYSICAL CONSTRAINTS AUDIO STUFFING CHANGES CHECKIN 02001
11/20/04	(P 36) CONNECTED NEW CPU DIODE REFERENCE (P 77) USB2 IDESEL - NOW FROM USB2 SIDE (P 56) ADDED BOMOPTIONS FOR MEMORY STRAPS (PP 56, 58) CONNECTED PWM FROM RV351LEP & PUT IN PROTO WORKAROUND (P 25) <RADAR 3849835> NEW SHASTA XTAL (P 62) <RADAR 3849855> SHASTA HT_PLL FILTER COST REDUCTION (P 91) <RADAR 3849858> USB CAP COST REDUCTION (P 76) ADDED STANDOFFS FOR Q85 CARD (PP 16,17) NEW FAN CIRCUIT CAPS (C1603, C1653, C1703) (P 50) <RADAR 3865344> VDDC_CT SET TO 1.50V (P 50) <RADAR 3877855> TP_VDD SET TO 1.80V (P 12) VESTA_ENET_LOWPWR UPDATE (PP 10, 22, 34, 50) USED COMPARATOR FOR LOW VOLTAGE RAIL LEDS CHECKIN 02002
11/22/04	(P 49) CONNECTED AGPTEST RESISTOR TO VDDP (P 56) ADDED PADS FOR STRAPPING RESISTORS TO GPU_GPIO<14> (P 58) ADDED CONSTRAINT SETS (P 59) STUFFED AROUND Q5900 PANEL PWR SEQUENCING (P 59) LED 3 NOW DRIVEN FROM FPD_PWR_ON (P 3) CONNECTED SHASTA CORE POWER FOR POWER SEQUENCING (P 76) FIXED PCI_CBE_L<1> CONNECTION MORE PHYSICAL & SPACING UPDATES (P 83) <RADAR 3890225> OPTICAL DRIVE CONNECTOR CHANGED TO 516S0235 CHECKIN 02003 (P 56) ADDED OPTION OF USING PWM FROM SHASTA <RADAR 3849718, 3849767, 3849854> MADE ON & VISHAY FETS TRUE ALTERNATES (P5) ADDED U3L W/ NEW LAMINATE AS ALTERNATE (P 16) C1653 - REPLACED WITH LOWER HEIGHT CAP CHECKIN 02004
11/23/04	(P 76) TABLED IN NEW STANDOFFS FOR Q85 CARD PROTO RELEASE (REV 3)
12/02/04	(P 90) FIXED ALIAS PROBLEM WITH FW_TPB2_PD (P 90) FIXED FW_CPS SHORT (P 35) REMOVED DS3500 & DS3501 (P 83) REMOVED SECOND SATA CONNECTOR CHECKIN 03001 CONVERTED DISCRETES TO LEAD FREE CHECKIN 03002
12/07/04	CHANGED U7700 BACK TO LEADED PART (P 5) REMOVED ORIGINAL U3LITE (NEW LAMINATE ONLY FOR C/D) (P 49) CHANGED GPU TO RV351LEP (338S0231) (P 76) NOW HAVE CORRECT SYMBOL FOR STANDOFFS (P 76) J7650 - NEW TO ALLOW 5MM CONNECTED HEIGHT BOM RELEASE REV 04

REVISION HISTORY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT	OF
NONE	4	102

PROCESSORS

QUALIFIED

	PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
WAVE3	337S2969	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.8G,85C,BPA	1.8GHZ	1.20V	42W	?	U2900	CPU_DD30_1_8GHZ

	PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
WAVE3	337S2970	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BRA	1.25V
WAVE5	337S2981	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BPL	1.20V
WAVE5	337S2982	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BRL	1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0320	1	IC,U3LITE,NEW LAM,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0321	343S0320		U3	U3L,NEW LAM,200MM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0324	1	IC,ASIC,VESTA,V1.3	U8600	

MISC PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
	062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
	820-1747	1	PCB,FAB,MLB	MLB1	
	825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
	051-6772	1	PCB,SCHEM,MLB	SCH1	
	341T1667	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
	341T1395	1	PURCH ASSY, SMU BIG	U1300	
CRITICAL	603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL	603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114		LED700,LED702,LED5900	RINGBRIGHT LED
376S0204	376S0130		Q3310,Q3320,Q3410	MOSFET,N-CH,VISHAY
376S0207	376S0146		Q3311,Q3321,Q3411	MOSFET,N-CH,VISHAY

TABLE ITEMS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 04

SCALE NONE | SHT 5 OF 102

L80	NO_TEST=YES	TP_FBBCS1_L	52	
L33	NO_TEST=YES	TP_AGP_MB_AGP8X_DET_L	48	
L33	NO_TEST=YES	TP_ATTENTION	29	
L34	NO_TEST=YES	TP_AFN	29	
L34	NO_TEST=YES	TP_PSRO1	29	
L34	NO_TEST=YES	TP_PSRO2	29	
L34	NO_TEST=YES	TP_PSYNCOUT	29	
L34	NO_TEST=YES	TP_USB2_PWREN<2>	92	
L35	NO_TEST=YES	TP_USB2_PWREN<3>	92	
L34	NO_TEST=YES	TP_USB2_PWREN<4>	92	
L35	NO_TEST=YES	TP_NEC_AMC	77	
L35	NO_TEST=YES	TP_NEC_NANDTEST	77	
L35	NO_TEST=YES	TP_NEC_NTEST1	77	
L35	NO_TEST=YES	TP_NEC_SMC	77	
L35	NO_TEST=YES	TP_NEC_SMI_L	77	
L36	NO_TEST=YES	TP_NEC_SRCLK	77	
L35	NO_TEST=YES	TP_NEC_SRDATA	77	
L36	NO_TEST=YES	TP_NEC_SRMOD	77	
L36	NO_TEST=YES	TP_NEC_TEB	77	
L36	NO_TEST=YES	TP_NEC_TEST	77	
L36	NO_TEST=YES	TP_PLS_CLK_66M_0	27	
L36	NO_TEST=YES	TP_PLS_CLK_66M_1	27	
L37	NO_TEST=YES	TP_PLS_REF_CML	27	
L37	NO_TEST=YES	TP_PLS_TEST1	27	
L37	NO_TEST=YES	TP_PLS_TEST2	27	
L37	NO_TEST=YES	TP_PLS_TEST3	27	
L37	NO_TEST=YES	TP_SB_FSTEST	25	
L37	NO_TEST=YES	TP_SB_PLLTEST	25	
L37	NO_TEST=YES	TP_VREF_CG	48	
L37	NO_TEST=YES	TP_SB_NC_P7	91	
L38	NO_TEST=YES	TP_SB_NC_P8	91	
L37	NO_TEST=YES	TP_SB_NC_R3	91	
L38	NO_TEST=YES	TP_SB_NC_R4	91	
L38	NO_TEST=YES	TP_SB_NC_R5	91	
L38	NO_TEST=YES	TP_SB_NC_R6	91	
L38	NO_TEST=YES	TP_SB_NC_R7	91	
L38	NO_TEST=YES	TP_SB_NC_R8	91	
L38	NO_TEST=YES	TP_SB_NC_T1	91	
L38	NO_TEST=YES	TP_SB_NC_T2	91	
L38	NO_TEST=YES	TP_SB_NC_T3	91	
L39	NO_TEST=YES	TP_SB_NC_T4	91	
L38	NO_TEST=YES	TP_SB_NC_T5	91	
L39	NO_TEST=YES	TP_SB_NC_T6	91	
L39	NO_TEST=YES	TP_SB_NC_T7	91	
L39	NO_TEST=YES	TP_SB_NC_T8	91	
L39	NO_TEST=YES	TP_SB_NC_U1	91	
L39	NO_TEST=YES	TP_SB_NC_U2	91	
L39	NO_TEST=YES	TP_SB_NC_U3	91	
L39	NO_TEST=YES	TP_SB_NC_U4	91	
L39	NO_TEST=YES	TP_SB_NC_U5	91	
L39	NO_TEST=YES	TP_SB_NC_U6	91	
L40	NO_TEST=YES	TP_SB_NC_V1	91	
L40	NO_TEST=YES	TP_SB_NC_V2	91	
L40	NO_TEST=YES	TP_SB_NC_V3	91	
L40	NO_TEST=YES	TP_SB_NC_V4	91	
L40	NO_TEST=YES	TP_SB_NC_W1	91	
L40	NO_TEST=YES	TP_SB_NC_W3	91	
L40	NO_TEST=YES	TP_SB_NC_Y1	91	
L40	NO_TEST=YES	TP_SB_NC_Y3	91	
L40	NO_TEST=YES	TP_SATA_CLK25M	27	
L42	NO_TEST=YES	TP_USB2_PWREN<0>	92	
L42	NO_TEST=YES	TP_USB2_PWREN<1>	92	
L43	NO_TEST=YES	TP_DUMMY_A	24	
L43	NO_TEST=YES	TP_DUMMY_B	24	
L43	NO_TEST=YES	TP_RAM_CKE_R<2>	8	
L43	NO_TEST=YES	TP_RAM_CKE_R<3>	8	
L43	NO_TEST=YES	TP_RAM_CKE_R<6>	8	
L43	NO_TEST=YES	TP_RAM_CKE_R<7>	8	
L43	NO_TEST=YES	TP_RAM_CS_L_R<10>	8	
L43	NO_TEST=YES	TP_RAM_CS_L_R<11>	8	
L43	NO_TEST=YES	TP_RAM_CS_L_R<2>	8	
L43	NO_TEST=YES	TP_RAM_CS_L_R<3>	8	
L44	NO_TEST=YES	TP_RAM_MUXEN0	8	
L44	NO_TEST=YES	TP_RAM_MUXEN4	8	
L44	NO_TEST=YES	TP_NB_PM_SLEEP0	24	
L44	NO_TEST=YES	TP_J4000_SJRESET_L	40	
L44	NO_TEST=YES	TP_J4001_SJRESET_L	40	
L78	NO_TEST=YES	U2100_UNUSED	21	
L80	NO_TEST=YES	PLS_CLK_66M_0_R	27	
L81	NO_TEST=YES	PLS_CLK_66M_1_R	27	

GENZ SHOULD USE J1400 FOR THE FOLLOWING NETS:

L85	NO_TEST=TRUE	EI_CPU_TO_NB_AD<0..43>	14 28 29
L84	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	14 28 29
L85	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	14 28 29
L85	NO_TEST=TRUE	EI_CPU_TO_NB_SR_N<0..1>	14 28 29
L87	NO_TEST=TRUE	EI_CPU_TO_NB_SR_P<0..1>	14 28 29
L86	NO_TEST=TRUE	EI_NB_TO_CPU_AD<0..43>	14 28 29
L88	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	14 28 29
L90	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	14 28 29
L92	NO_TEST=TRUE	EI_NB_TO_CPU_SR_N<0..1>	14 28 29
L93	NO_TEST=TRUE	EI_NB_TO_CPU_SR_P<0..1>	14 28 29
L95	NO_TEST=YES	CHKSTOP_L	8 14 29
L95	NO_TEST=YES	CPU_HRESET_L	14 29 30
L95	NO_TEST=YES	CPU_INT_L	14 25 29 30
L96	NO_TEST=YES	CPU1_HTBEN	14
L97	NO_TEST=YES	EI_CPU1_CLK_N	14 27
L98	NO_TEST=YES	EI_CPU1_CLK_P	14 27
L99	NO_TEST=YES	EI_QACK_L	14 28 29
L100	NO_TEST=YES	EI_QREQ_L	14 28 29 30
L101	NO_TEST=YES	EI_SE	14 28 29 30
L102	NO_TEST=YES	I2C_SMU_A_SCL_OUT_L	13 14 18
L103	NO_TEST=YES	I2C_SMU_A_SDA_OUT_L	13 14 18
L104	NO_TEST=YES	MCP_L	14 29
L105	NO_TEST=YES	RI_L	14 29 30
L106	NO_TEST=YES	SYNCENABLE	14 29 30
L107	NO_TEST=YES	TP_PROC_TRIGGER_OUT	14 29
L108	NO_TEST=YES	EI_CPU1_SYNC	14 27

101	IN	AUD_MIC_IN_N_CONN		FUNC_TEST=TRUE
101	IN	AUD_MIC_IN_P_CONN		FUNC_TEST=TRUE
90	IN	FW_VP		FUNC_TEST=TRUE
101	IN	GND_AUDIO_MIC_CONN		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SCL		FUNC_TEST=TRUE
18 17	IN	I2C_HD_TEMP_SDA		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SCL		FUNC_TEST=TRUE
25 18	IN	I2C_SB_SDA		FUNC_TEST=TRUE
36 33 31	IN	KPGND2		FUNC_TEST=TRUE
36 33 31	IN	KPVDD2		FUNC_TEST=TRUE
	IN	TMDS_DCC_CLK		FUNC_TEST=TRUE
	IN	TMDS_DCC_DAT		FUNC_TEST=TRUE
77 76 75 74 73	IN	PCI_AD<31..0>		FUNC_TEST=TRUE
77 76 74 73	IN	PCI_CBE_L<3..0>		FUNC_TEST=TRUE
8	IN	PCI_CLK33M_AIRPORT		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_REQ_L		FUNC_TEST=YES
76 74	IN	PCI_SLOTA_GNT_L		FUNC_TEST=YES
76 25	IN	PCI_SLOTA_INT_L		FUNC_TEST=YES
74 56 8	IN	PCI_RESET_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_FRAME_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_TRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_IRDY_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_STOP_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_DEVSEL_L		FUNC_TEST=YES
77 76 74 73	IN	PCI_PAR		FUNC_TEST=YES
76	IN	PCI_SLOTA_IDSEL		FUNC_TEST=YES
76 75 74	IN	ROM_CS_L		FUNC_TEST=YES
76 75 74	IN	ROM_OE_L		FUNC_TEST=YES
76 75 74	IN	ROM_WE_L		FUNC_TEST=YES
76 75	IN	ROM_ONBOARD_CS_L		FUNC_TEST=YES
76	IN	AIRPORT_CLKRUN_L_PD		FUNC_TEST=YES
76	IN	USB_BT_N		FUNC_TEST=YES
76	IN	USB_BT_P		FUNC_TEST=YES
92	IN	USB2_PORT1_N_F		FUNC_TEST=YES
92	IN	USB2_PORT1_P_F		FUNC_TEST=YES
92	IN	USB2_PORT2_N_F		FUNC_TEST=YES
92	IN	USB2_PORT2_P_F		FUNC_TEST=YES
92	IN	USB2_PORT3_N_F		FUNC_TEST=YES
92	IN	USB2_PORT3_P_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT1_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT2_F		FUNC_TEST=YES
92	IN	PP5V_USB2_PORT3_F		FUNC_TEST=YES
94 25	IN	I2S1_DEV_TO_SB_DTI	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SYNC	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_BITCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_MCLK	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_SB_TO_DEV_DTO	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	I2S1_RESET_L	2 TEST POINTS	FUNC_TEST=YES
94 25	IN	MODEM_RING2SYS_L	2 TEST POINTS	FUNC_TEST=YES
92 91	IN	USB2_P<3>		FUNC_TEST=YES
92 91	IN	USB2_N<3>		FUNC_TEST=YES
25	IN	UDASH_SDOWN		FUNC_TEST=YES
25	IN	UDASH_RESET_L		FUNC_TEST=YES
59	IN	PPVCC_TMDS		FUNC_TEST=YES
59	IN	PP3V3_DDC		FUNC_TEST=YES
59	IN	TD0M		FUNC_TEST=YES
59	IN	TD0P		FUNC_TEST=YES
59	IN	TD1M		FUNC_TEST=YES
59	IN	TD1P		FUNC_TEST=YES
59	IN	TD2M		FUNC_TEST=YES
59	IN	TD2P		FUNC_TEST=YES
59	IN	TCKM		FUNC_TEST=YES
59	IN	TCKP		FUNC_TEST=YES
59	IN	I2C_TMDS_SDA		FUNC_TEST=YES
59	IN	I2C_TMDS_SCL		FUNC_TEST=YES
59 7	IN	GND_CHASSIS_TMDS		FUNC_TEST=YES
59	IN	FILT_ANALOG_RED		FUNC_TEST=YES
59	IN	FILT_ANALOG_GRN		FUNC_TEST=YES
59	IN	FILT_ANALOG_BLU		FUNC_TEST=YES
59 58	IN	MON_DETECT		FUNC_TEST=YES
59	IN	PP24V_INV		FUNC_TEST=YES
59	IN	GND_20_INV		FUNC_TEST=YES
59	IN	INV_20_LCD_PWM		FUNC_TEST=YES
59	IN	INV_20_CUR_HI_F		FUNC_TEST=YES
59	IN	PP12V_INV		FUNC_TEST=YES
59	IN	GND_17_INV		FUNC_TEST=YES
59	IN	PP5V_AGP_RL		FUNC_TEST=YES
59	IN	INV_17_LCD_PWM_F		FUNC_TEST=YES
59	IN	INV_17_CUR_HI_F		FUNC_TEST=YES
33 8	IN	CPU_VID_R<5..0>		FUNC_TEST=TRUE
36	IN	KPVDD2_FMAX		FUNC_TEST=YES
36	IN	KPGND2_FMAX		FUNC_TEST=YES
36	IN	TDIODE_POS_FMAX		FUNC_TEST=YES
36	IN	TDIODE_NEG_FMAX		FUNC_TEST=YES
36 33	IN	CORE_ISNS_M		FUNC_TEST=YES
36 33	IN	CORE_ISNS_P		FUNC_TEST=YES

PP12V_RUN PP5V_RUN PP24V_RUN PP5V_ALL PP3V3_RUN

IN	PP12V_RUN	10 TEST POINTS	FUNC_TEST=YES
11 7 IN	PP5V_ALL	5 TEST POINTS	FUNC_TEST=YES
18 11 10 7 IN	PP5V_RUN	5 TEST POINTS	FUNC_TEST=YES
50 34 22 18 11 10 7 IN	PP3V3_RUN	5 TEST POINTS	FUNC_TEST=YES
IN	PP24V_RUN	5 TEST POINTS	FUNC_TEST=YES
83 7 IN	=PP5V_DISK	5 TEST POINTS	FUNC_TEST=YES
83 7 IN	=PP12V_DISK	5 TEST POINTS	FUNC_TEST=YES
IN	GND	12 TEST POINTS	FUNC_TEST=YES

PP2V5_RUN PP5V_PWRON PP1V2_PWRON PP1V5_RUN PP3V3_PWRON

IN	PP2V5_RUN		FUNC_TEST=YES
IN	PP1V5_RUN		FUNC_TEST=YES
18 13 IN	PP5V_PWRON		FUNC_TEST=YES
58 27 18 13 IN	PP3V3_PWRON		FUNC_TEST=YES
IN	PP1V2_PWRON		FUNC_TEST=YES
IN	=PPVCORE_PWRON_SB		FUNC_TEST=YES
13 8 7 IN	=PP3V3_ALL_SMU		FUNC_TEST=TRUE
31 8 7 3 IN	=PP5V_RUN_CPU		FUNC_TEST=YES
22 IN	PPVCORE_NB		FUNC_TEST=YES
35 34 33 7 IN	PPVCORE_CPU		FUNC_TEST=YES
34 33 IN	PP12V_CPU		FUNC_TEST=YES
33 IN	VCORE_SENSE_GND		FUNC_TEST=YES
33 IN	VCORE_SENSE_VOUT		FUNC_TEST=YES
8 7 IN	SMU_MANUAL_RESET_L	2 TEST POINTS	FUNC_TEST=YES
13 7 IN	SYS_POWER_BUTTON_L	2 TEST POINTS	FUNC_TEST=YES
7 IN	POWER_BUTTON_L		FUNC_TEST=YES
7 IN	RESET_BUTTON_L		FUNC_TEST=YES
13 8 IN	SMU_RESET_L		FUNC_TEST=YES
33 13 11 10 7 IN	SYS_POWERUP_L		FUNC_TEST=YES
46 22 11 10 9 8 IN	SYS_SLEEP		FUNC_TEST=YES
13 8 IN	SYS_POWERFAIL_L		FUNC_TEST=YES
9 IN	U900_FEEDBACK		FUNC_TEST=YES
22 IN	U2200_FEEDBACK		FUNC_TEST=YES
59 58 IN	ANALOG_RED		FUNC_TEST=YES
59 58 IN	ANALOG_GRN		FUNC_TEST=YES
59 58 IN	ANALOG_BLU		FUNC_TEST=YES
101 25 IN	AUDIO_LO_DET_L		FUNC_TEST=YES
75 IN	ROM_WP_L		FUNC_TEST=YES
83 80 IN	UATA_DD<15..0>		FUNC_TEST=TRUE
83 80 IN	UATA_DA<2..0>		FUNC_TEST=TRUE
83 80 IN	UATA_CS0_L		FUNC_TEST=YES
83 80 IN	UATA_CS1_L		FUNC_TEST=YES
83 80 IN	UATA_RESET_L		FUNC_TEST=YES
83 IN	UATA_DSTROBE_R		FUNC_TEST=YES
83 80 IN	UATA_HSTROBE		FUNC_TEST=YES
83 80 66 IN	UATA_STOP		FUNC_TEST=YES
83 IN	UATA_DMARQ_R		FUNC_TEST=YES
83 80 IN	UATA_DMACK_L		FUNC_TEST=YES
83 IN	UATA_INTRQ_R		FUNC_TEST=YES
83 IN	UATA_IOCS16_PU		FUNC_TEST=YES
83 IN	UATA_CSEL_PD		FUNC_TEST=YES
83 IN	UATA_DASP_L		FUNC_TEST=TRUE
36 31 IN	TDIODE_NEG		FUNC_TEST=YES

FUNC TEST

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

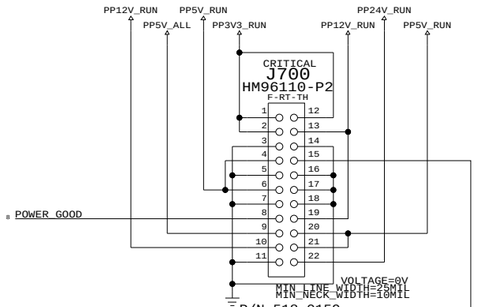
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

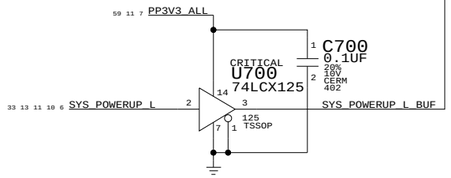
II NOT TO REPRODUCE OR COPY IT

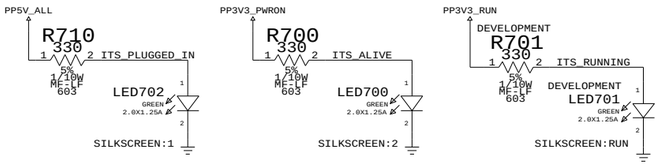
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

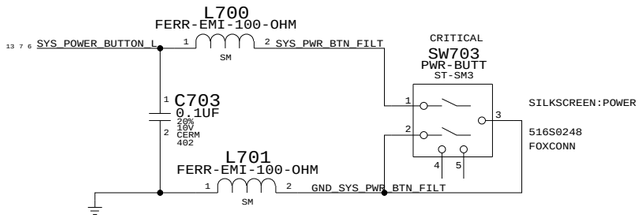
APPLE COMPUTER INC.

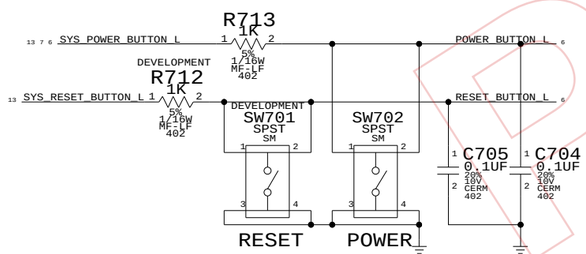
SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 6 OF 102	

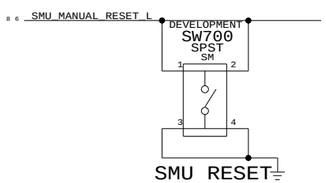






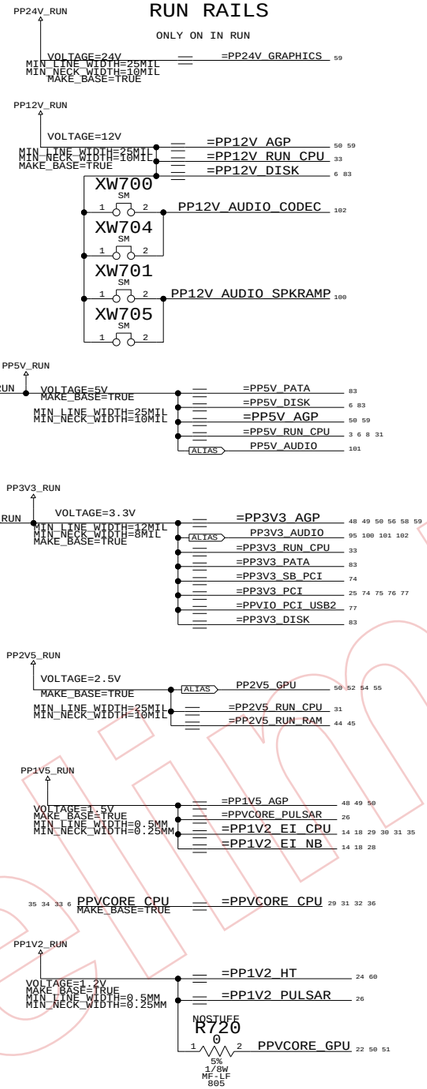






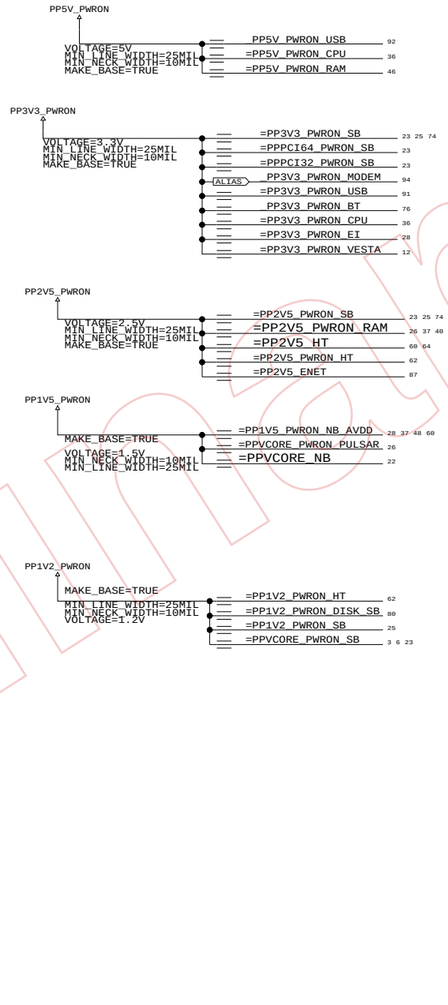
RUN RAILS

ONLY ON IN RUN



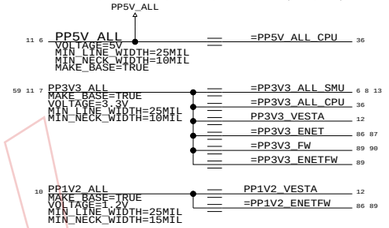
PWRON RAILS

ON IN RUN AND SLEEP

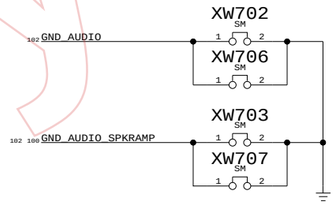


ALL RAILS

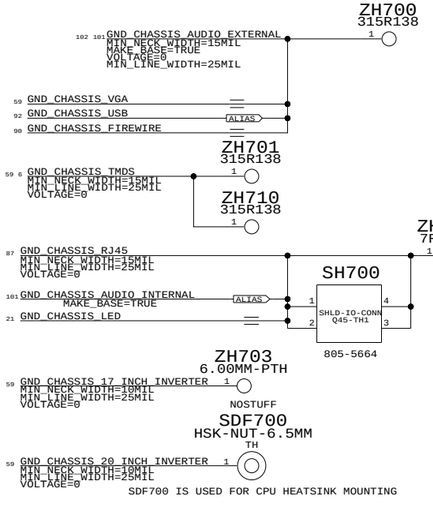
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



GND RAILS

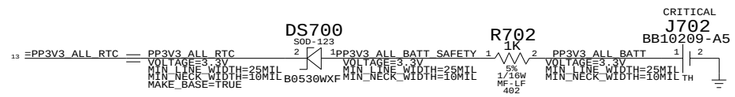


CHASSIS GND



RTC BATTERY

ALWAYS ON (TRICKLE)



POWER CONN / ALIAS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE: NONE

SHT 7 OF 102

PCI CLOCKS

TP_NB_THMI MAKE_BASE=TRUE ALIAS NB_THMI 24
TP_THMO MAKE_BASE=TRUE ALIAS NB_THMO 24
6 TP_RAM_CKE_R<2> MAKE_BASE=TRUE ALIAS RAM_CKE_R<2> 37
6 TP_RAM_CKE_R<3> MAKE_BASE=TRUE ALIAS RAM_CKE_R<3> 37
6 TP_RAM_CKE_R<6> MAKE_BASE=TRUE ALIAS RAM_CKE_R<6> 37
6 TP_RAM_CKE_R<7> MAKE_BASE=TRUE ALIAS RAM_CKE_R<7> 37
6 TP_RAM_MUXEN0 MAKE_BASE=TRUE ALIAS RAM_MUXEN0 37
6 TP_RAM_MUXEN4 MAKE_BASE=TRUE ALIAS RAM_MUXEN4 37
6 TP_RAM_CS_L_R<2> MAKE_BASE=TRUE ALIAS RAM_CS_L_R<2> 37
6 TP_RAM_CS_L_R<3> MAKE_BASE=TRUE ALIAS RAM_CS_L_R<3> 37
6 TP_RAM_CS_L_R<10> MAKE_BASE=TRUE ALIAS RAM_CS_L_R<10> 37
6 TP_RAM_CS_L_R<11> MAKE_BASE=TRUE ALIAS RAM_CS_L_R<11> 37

PCI_CLK33M_USB2 MAKE_BASE=TRUE — PCI_CLK_GP0 27
=PCI_CLK33M_USB2 77
TP_PCI_CLK_GP1 MAKE_BASE=TRUE ALIAS PCI_CLK_GP1 27
6 PCI_CLK33M_AIRPORT MAKE_BASE=TRUE — PCI_CLK_P3 27
PCI_CLK33M_AIRPORT 76
TP_PCI_CLK_P4 MAKE_BASE=TRUE ALIAS PCI_CLK_P4 27
74 27 PCI_CLK33M_SB_EXT MAKE_BASE=TRUE ALIAS PCI_CLK_P1 27

SMU

TP_ALS0_OUT MAKE_BASE=TRUE ALIAS ALS0_OUT 13
TP_ALS1_OUT MAKE_BASE=TRUE ALIAS ALS1_OUT 13
TP_ALS_GAIN_BOOST MAKE_BASE=TRUE ALIAS ALS_GAIN_BOOST 13
TP_SMU_ONEWIRE MAKE_BASE=TRUE ALIAS SMU_ONEWIRE 13
TP_SYS_SLOT_PWR MAKE_BASE=TRUE ALIAS SYS_SLOT_PWR 13
TP_SMU_PWRSEQ_P1_3 MAKE_BASE=TRUE ALIAS SMU_PWRSEQ_P1_3 13
TP_SYS_DOOR_AJAR_L MAKE_BASE=TRUE ALIAS SYS_DOOR_AJAR_L 13
TP_FAN_PWM8 MAKE_BASE=TRUE ALIAS FAN_PWM8 13
TP_SYS_DRIVE_BAY_INT_L MAKE_BASE=TRUE ALIAS SYS_DRIVE_BAY_INT_L 13
13 8 SMU_WARM_RESET_L MAKE_BASE=TRUE ALIAS NB_WARM_RESET_L 24

74 56 6 PCI_RESET_L MAKE_BASE=TRUE — PCI_AIRPORT_RESET_L 76
GPU_RESET_L 49
=PCI_ROM_RESET_L 75
=PCI_USB2_RESET_L 77

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
16486 SMU_RESET	10 MIL SPACING		SYS_COLD_RESET_L 13 24
16487 SMU_RESET	10 MIL SPACING		SYS_WARM_RESET_L 8 25 74 77

PP2V5_PWRON
R870 4.7K 5% 1/16W MF-LF 402
13 8 SMU_WARM_RESET_L
U700 74LCX125 TSSOP
SYS_WARM_RESET_L 8 25 74 77
13 SMU_SLEEP
SYS_SLEEP 6 9 10 11 22 46
24 NB_SUSPEND_ACK_L
NB_SUSPENDACK_L 13

DEVELOPMENT
J800 U.FL-R-SMT F-ST-SM
24 NB_PMR_OBSV
518S0104

PP5V_ALL
DIAG LED
R850 180 5% 1/16W MF-LF 402
LED850P1
LED850 RED SM
LED850P2
13 DIAG_LED MAKE_BASE=TRUE
R851 1K 5% 1/16W MF-LF 402
DIAG_LED_R
Q850 2N3904LF SOT23

CPU VID<0:5>

VID CONTROLLED BY SMU

PP3V3_RUN
R814 R816 R817 R808 R809 R804 10K 5% 1/16W MF-LF 402
13 CPU_VID<0> R819 0 5% 1/16W MF-LF 402 CPU_VID_R<0> 6 33
13 CPU_VID<1> R820 0 CPU_VID_R<1> 6 33
13 CPU_VID<2> R821 0 CPU_VID_R<2> 6 33
13 CPU_VID<3> R822 0 CPU_VID_R<3> 6 33
13 CPU_VID<4> R823 0 CPU_VID_R<4> 6 33
13 CPU_VID<5> R824 0 CPU_VID_R<5> 6 33
NOSTUFF J803 BM12B-SRSS-TB
R832 R831 R830 R829 R827 1K 5% 1/16W MF-LF 402
R811 20K 5% 1/16W MF-LF 402
NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

DOWNLOAD CONNECTOR

PP3V3_ALL
DEVELOPMENT J802 HC17051 M-ST-TH
DEVELOPMENT R826 100 5% 1/16W MF-LF 402
J802_2 2 1 SMU_BOOT_BUSY 13
13 SMU_BOOT_SCLK 3 4 SMU_BOOT_RXD 13
13 SMU_BOOT_CE 5 6 (SMU_BOOT_EPM) J802_6
7 8 SMU_MANUAL_RESET_L 6 7 8
13 SMU_BOOT_CNVSS 9 10 SMU_BOOT_TXD 13
518-0158
R806 R807 10K 5% 1/16W MF-LF 402
NOSTUFF R805 0 5% 1/16W MF-LF 402
R803 10K 5% 1/16W MF-LF 402
J802 & R826 CAN MOVE TO DEVELOPMENT BOM POST RAMP

SMU ANALOG VREF

13 PP3V3_ALL_SMU_AVCC
NOSTUFF R818 200 1% 1/16W MF-LF 402
PPVREF_SMU MAKE_BASE=TRUE =PPVREF_SMU 13
R802 0 5% 1/16W MF-LF 603 PPVREF_SMU_ADC_REF 36
NOSTUFF C801 2.2UF 20% 10V CERM 805
NOSTUFF VR801 2.5V SOT-23
NOSTUFF C802 0.47UF 20% 16V CERM 603
GND_SMU_AVSS 13 33 36
NOSTUFF R828 0 5% 1/16W MF-LF 402 GND_SMU_AVSS_DAGND 36

POWER_FAIL_L CONNECTION

7 POWER_GOOD
PP3V3_ALL
R813 430 5% 1/16W MF-LF 402
NOSTUFF R812 10K 5% 1/16W MF-LF 402
SYS_POWERFAIL_L 6 13
R860 4.7K 5% 1/16W MF-LF 402
POWER_GOOD IS A 5V DRIVEN SIGNAL FROM POWER SUPPLY
2K PULLUP INSIDE P/S

PLL LOCK LED

31 8 7 6 3 =PP5V_RUN_CPU
DEVELOPMENT R837 180 5% 1/16W MF-LF 402
DEVELOPMENT Q802 2N3906 SM
Q802_B
Q802_E
DEVELOPMENT R838 1K 5% 1/16W MF-LF 402
DEVELOPMENT R835 180 5% 1/16W MF-LF 402
LED802_1
DEVELOPMENT LED802 GREEN 2.0X1.25A
Q803_C
DEVELOPMENT R839 180 5% 1/16W MF-LF 402
29 PLLLOCK_L
Q803_B
DEVELOPMENT Q803 2N3904LF SOT23

CHKSTOP LED

31 8 7 6 3 =PP5V_RUN_CPU
DEVELOPMENT R833 180 5% 1/16W MF-LF 402
LED801_1
DEVELOPMENT LED801 RED SM
Q800_D
DEVELOPMENT R834 180 5% 1/16W MF-LF 402
Q800_G
DEVELOPMENT Q800 2N7002 SOT23-LF
DEVELOPMENT R836 180 5% 1/16W MF-LF 402
29 14 6 CHKSTOP_L
Q801_B
DEVELOPMENT Q801 2N3904LF SOT23

CPU HEATSINK SMT NUTS

NOSTUFF SDF800 HSK-NUT-6.5MM TH
NOSTUFF SDF801 HSK-NUT-6.5MM TH
NOSTUFF SDF802 HSK-NUT-6.5MM TH
HS_SDF800 1 C880 0.01UF 20% 16V CERM 402
HS_SDF801 1 C881 0.01UF 20% 16V CERM 402
HS_SDF802 1 C882 0.01UF 20% 16V CERM 402
NOSTUFF SDF803 HSK-NUT-6.5MM TH
OMIT ZH804 6P15R5P4
HS_SDF803 1 C883 0.01UF 20% 16V CERM 402
HS_SDF804 1 C884 0.01UF 20% 16V CERM 402
SDF700 IS ALSO USED FOR HEATSINK MOUNTING

BACKUP SMU RESET CIRCUIT

13 7 6 =PP3V3_ALL_SMU
NOSTUFF C800 0.1UF 20% 10V CERM 402
VCC
U890 SM
NOSTUFF R890 1K 5% 1/16W MF-LF 402
8 7 6 SMU_MANUAL_RESET_L
DELAY NOSTUFF RESET
SMU_RESET_L 6 13
VOLTAGE DETECTOR MC33465N_30ATR
GND
NOSTUFF C890 0.01UF 10% 16V CERM 402
NOSTUFF C891 1UF 10% 6.3V CERM 402
R810 0 5% 1/16W MF-LF 402

PULSAR ERROR_L LED

PP3V3_RUN
DEVELOPMENT R801 4.7K 5% 1/16W MF-LF 402
DEVELOPMENT R800 330 5% 1/16W MF-LF 402
ERROR_LED
DEVELOPMENT D810 RED SM
27 CLOCK_ERROR_L

VESTA JTAG

JTAG_VESTA_TRST_L MAKE_BASE=TRUE ALIAS =JTAG_VESTA_TRST_L 12
TP_JTAG_VESTA_TCK MAKE_BASE=TRUE ALIAS =JTAG_VESTA_TCK 12
TP_JTAG_VESTA_TDI MAKE_BASE=TRUE ALIAS =JTAG_VESTA_TDI 12
TP_JTAG_VESTA_TDO MAKE_BASE=TRUE ALIAS =JTAG_VESTA_TDO 12
TP_JTAG_VESTA_TMS MAKE_BASE=TRUE ALIAS =JTAG_VESTA_TMS 12
R840 10K 5% 1/16W MF-LF 402

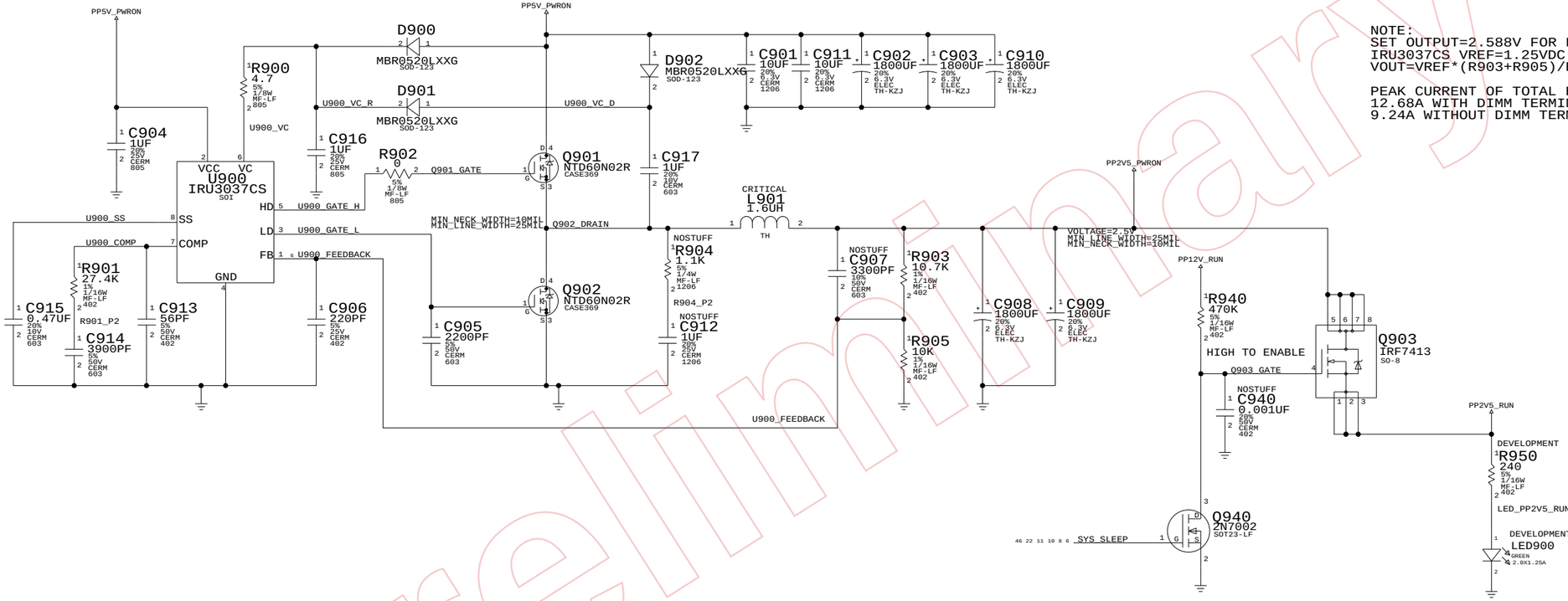
SHASTA JTAG PULL DOWN

THESE PINS HAVE INTERNAL PULLUPS
25 JTAG_SB_TRST_L
TP_JTAG_SB_TCK MAKE_BASE=TRUE ALIAS JTAG_SB_TCK 25
TP_JTAG_SB_TDI MAKE_BASE=TRUE ALIAS JTAG_SB_TDI 25
TP_JTAG_SB_TDO MAKE_BASE=TRUE ALIAS JTAG_SB_TDO 25
TP_JTAG_SB_TMS MAKE_BASE=TRUE ALIAS JTAG_SB_TMS 25
R825 10K 5% 1/16W MF-LF 402

SIGNAL ALIAS

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6772 | REV. 04
SCALE NONE | SHT 8 OF 102

2.5V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=2.588V FOR FRAMEBUFFER.
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R903+R905)/R905=2.588VDC

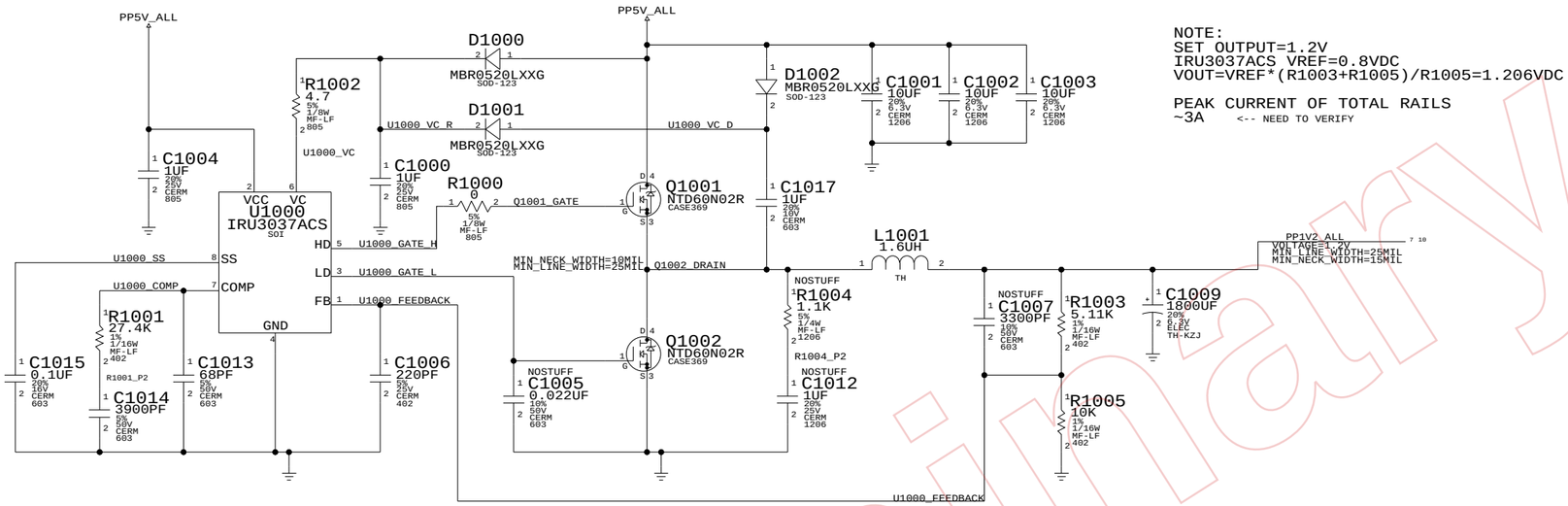
PEAK CURRENT OF TOTAL RAILS
12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

2.5V VREG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 9 OF 102	

PP1V2_ALL VOLTAGE REGULATOR

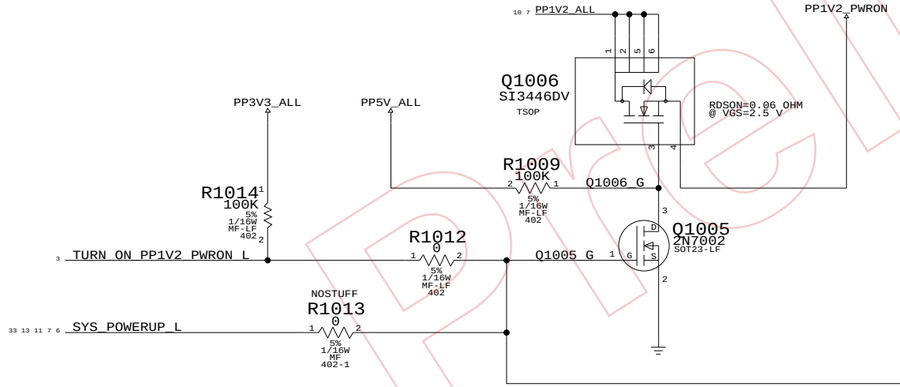


NOTE:
SET OUTPUT=1.2V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.206VDC

PEAK CURRENT OF TOTAL RAILS
~3A <-- NEED TO VERIFY

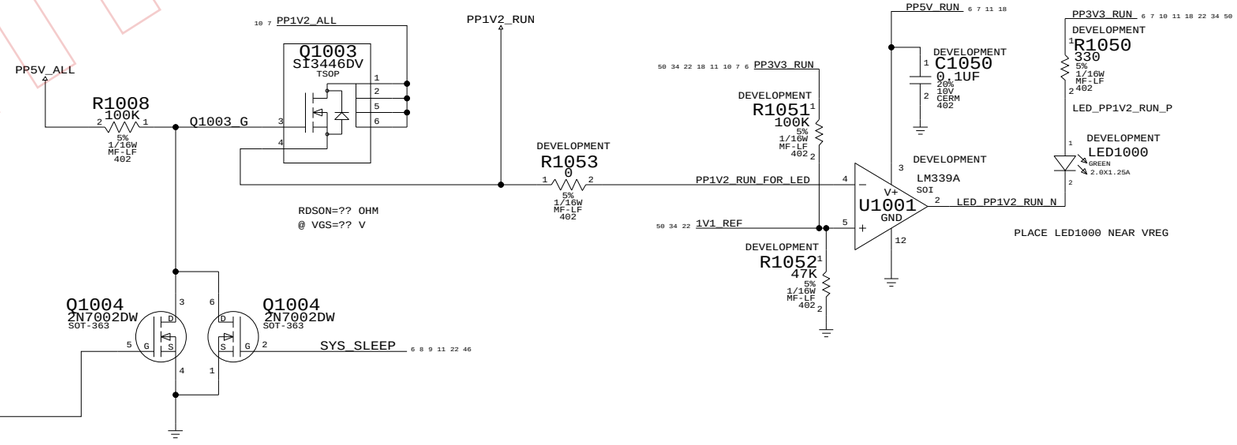
PP1V2_PWRON FET SWITCH

PEAK CURRENT ??A



PP1V2_RUN FET SWITCH

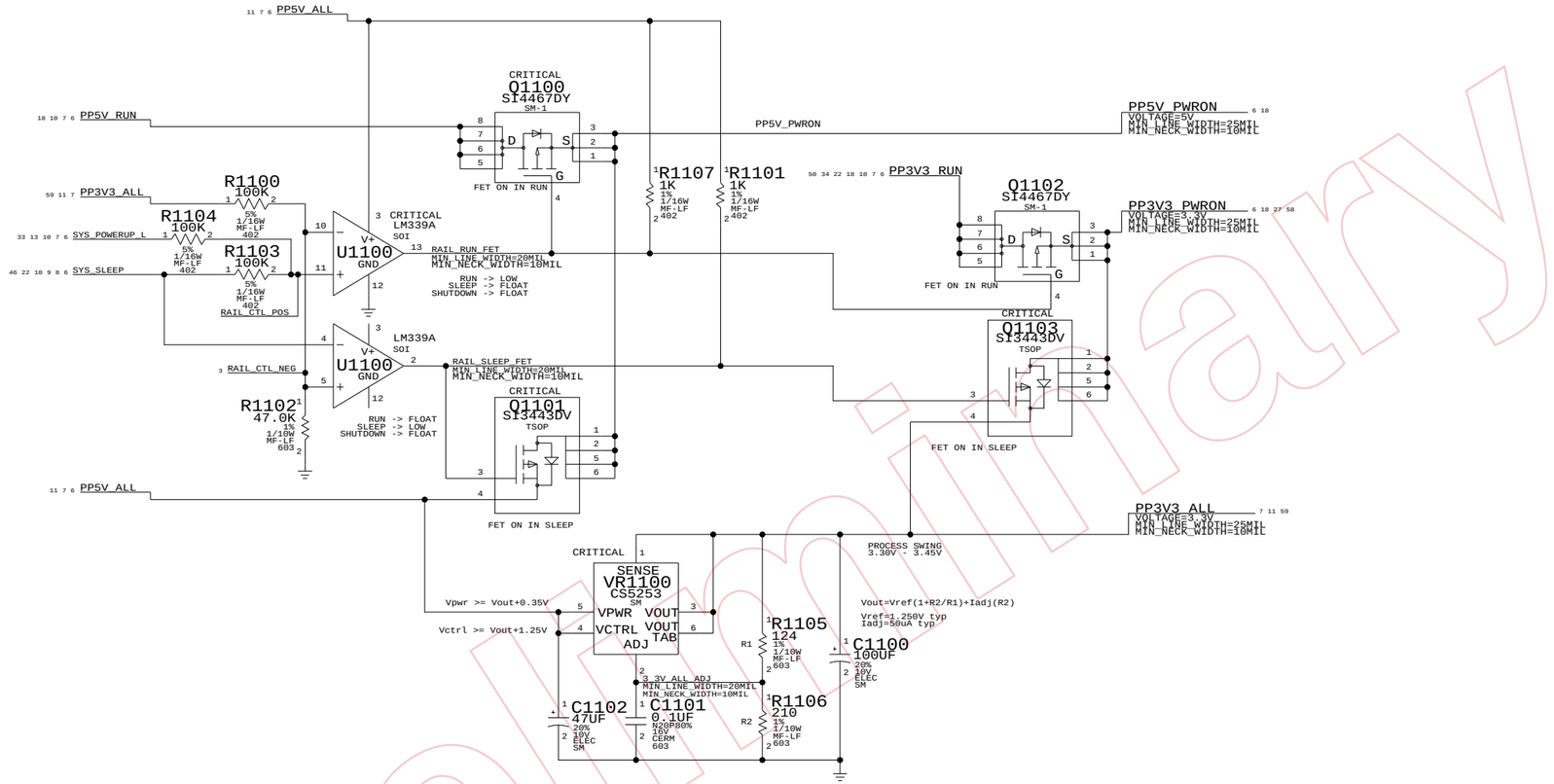
PEAK CURRENT ??A



1.2V VREG

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 10 OF 102	



5V & 3.3V VREGS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 11 OF 102	

Page Notes

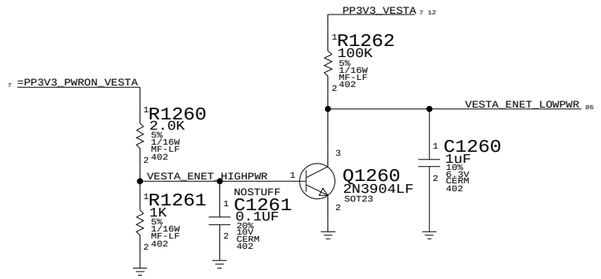
Power aliases required by this page:

Signal aliases required by this page:
(NONE)

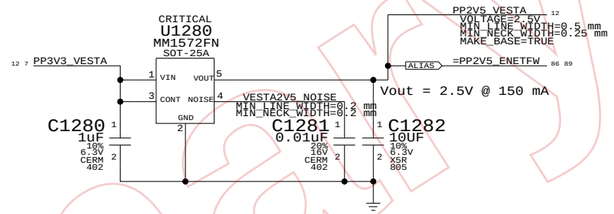
BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

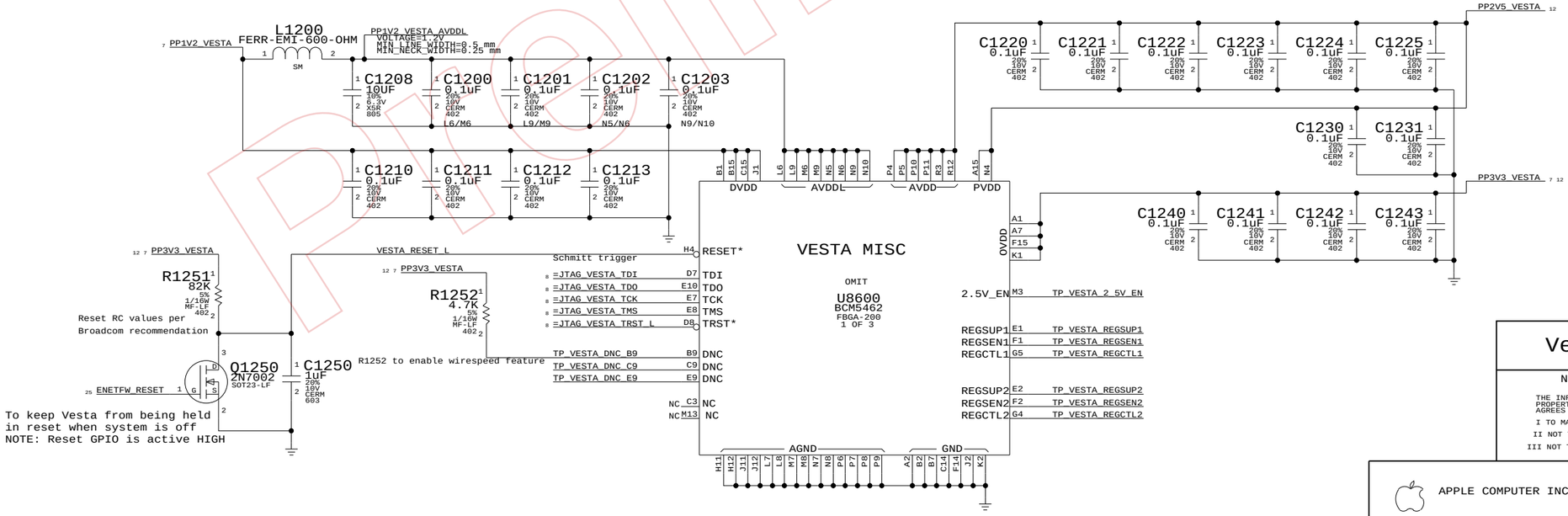
Ethernet LowPwr

ETHERNET PORTION IN LOW POWER MODE
WHEN NOT IN RUN MODE.



2.5V LDO





Vesta Core / Misc

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE: NONE

SHT 12 OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	15 MIL SPACING		SMU_CLK10M_XIN
	15 MIL SPACING		SMU_CLK10M_XOUT
	15 MIL SPACING		SMU_CLK10M_XOUT_R
RTC_CLK32K_XTAL	15 MIL SPACING		RTC_CLK32K_X1
	15 MIL SPACING		RTC_CLK32K_X2

Page Notes

Power aliases required by this page:
- _P3V3_ALL_SMU
- _P3V3_ALL_RTC
- _P3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

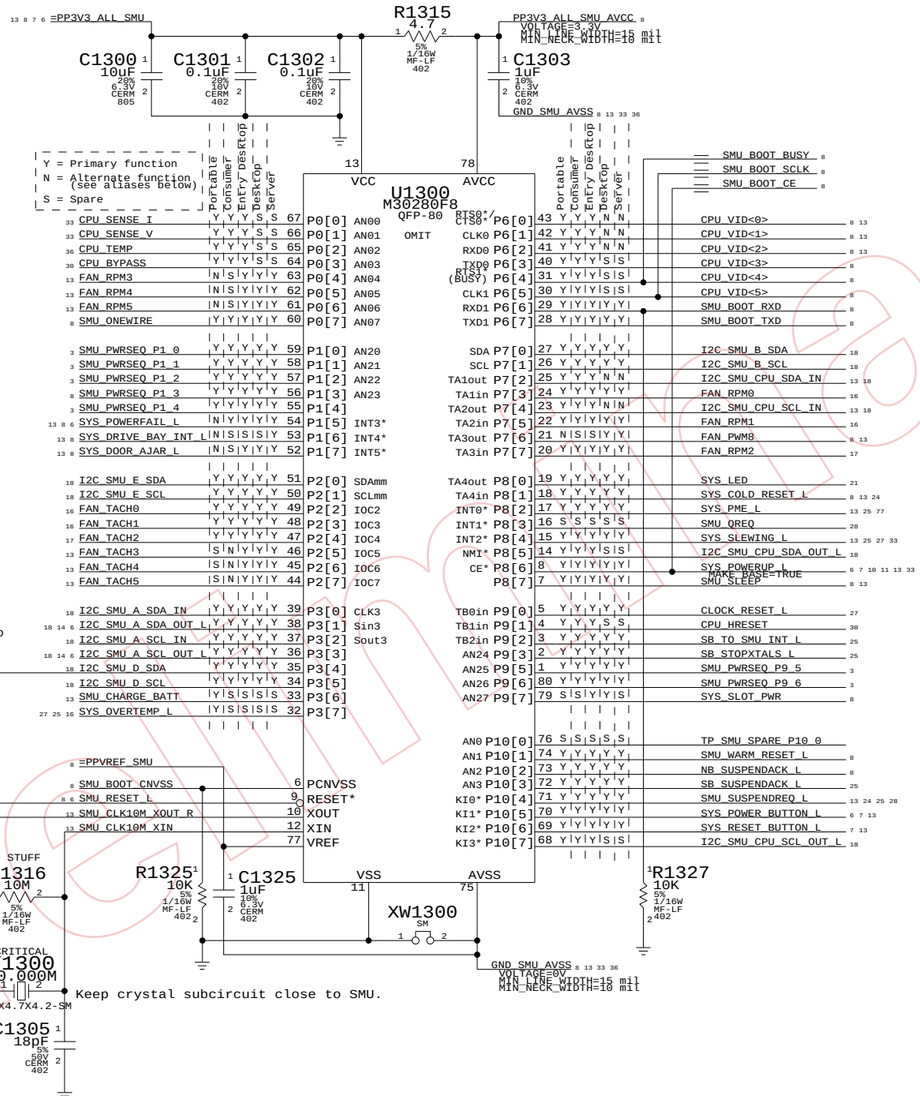
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

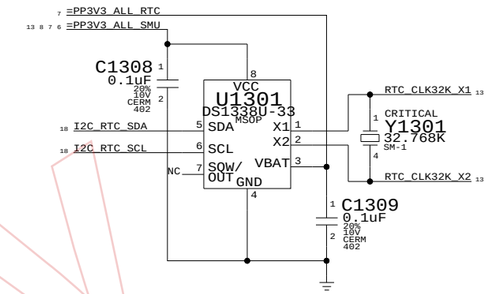
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

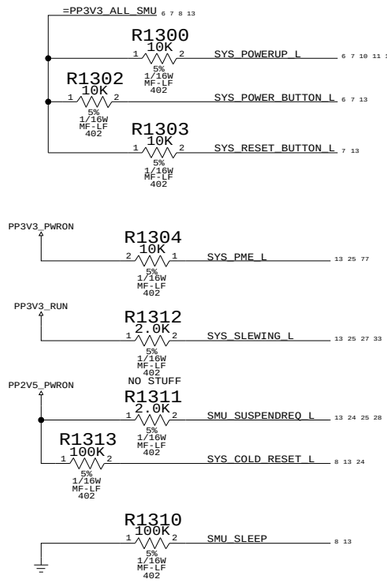
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4	—	ALS0_OUT
FAN_RPM4	0.5	—	ALS1_OUT
FAN_RPM5	0.6	—	ALS_GAIN_BOOST
SYS_POWERFAIL_L	1.5	—	SMU_ACIN
SYS_DRIVE_BAY_INT_L	1.6	—	SMU_BATT_DET_L
SYS_DOOR_AJAR_L	1.7	—	SYS_LID_OPEN
FAN_PWM8	7.6	—	SYS_KBDLED

Consumer

	Port		
FAN_TACH3	2.5	—	SYS_LED_RED
FAN_TACH4	2.6	—	SYS_LED_GREEN
FAN_TACH5	2.7	—	SYS_LED_BLUE
SMU_CHARGE_BATT	3.6	—	DIAG_LED

Tower & Server

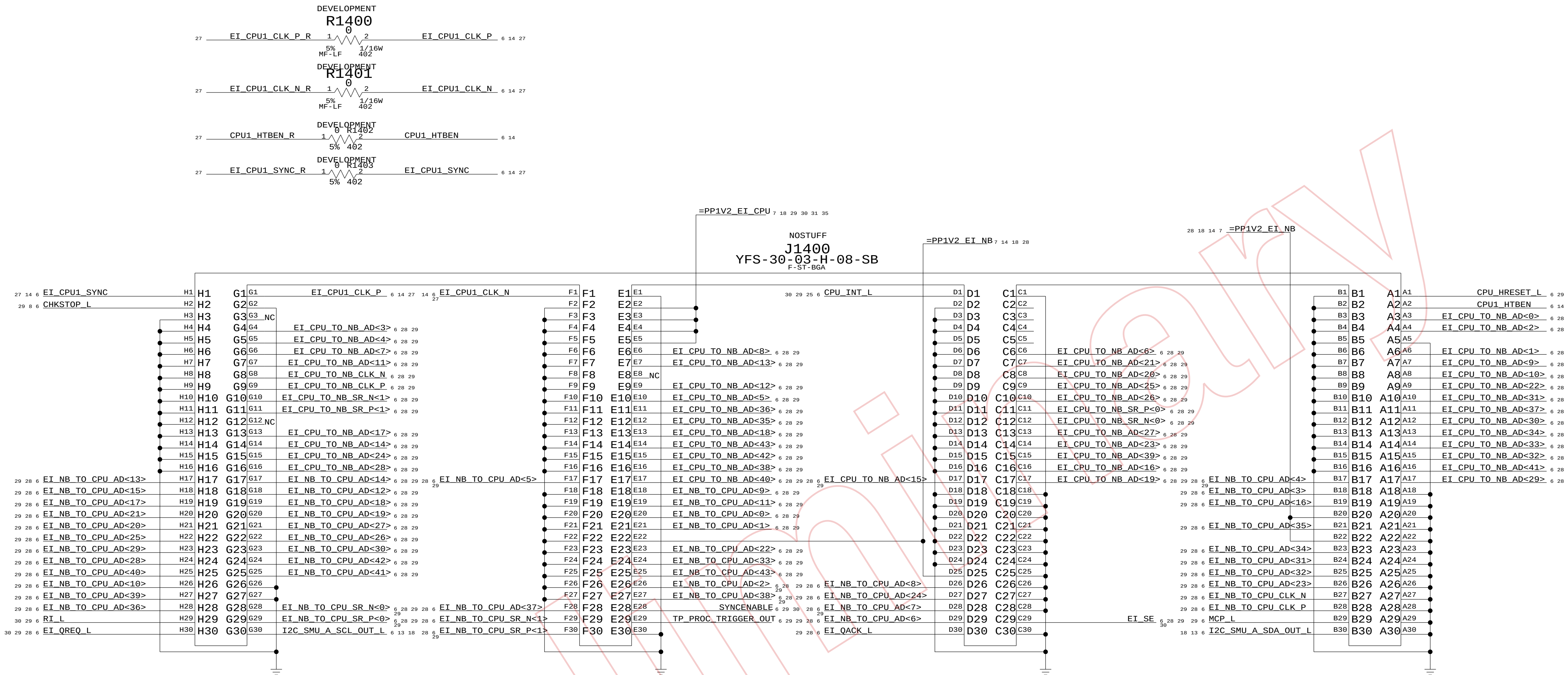
	Port		
CPU_VID<0>	6.0	—	FAN_TACH6
CPU_VID<1>	6.1	—	FAN_TACH7
CPU_VID<2>	6.2	—	FAN_TACH8
I2C_SMU_CPU_SDA_IN	7.2	—	FAN_PWM6
I2C_SMU_CPU_SCL_IN	7.4	—	FAN_PWM7

MASTER: SEEDY

System Management Unit

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 13 OF 102	

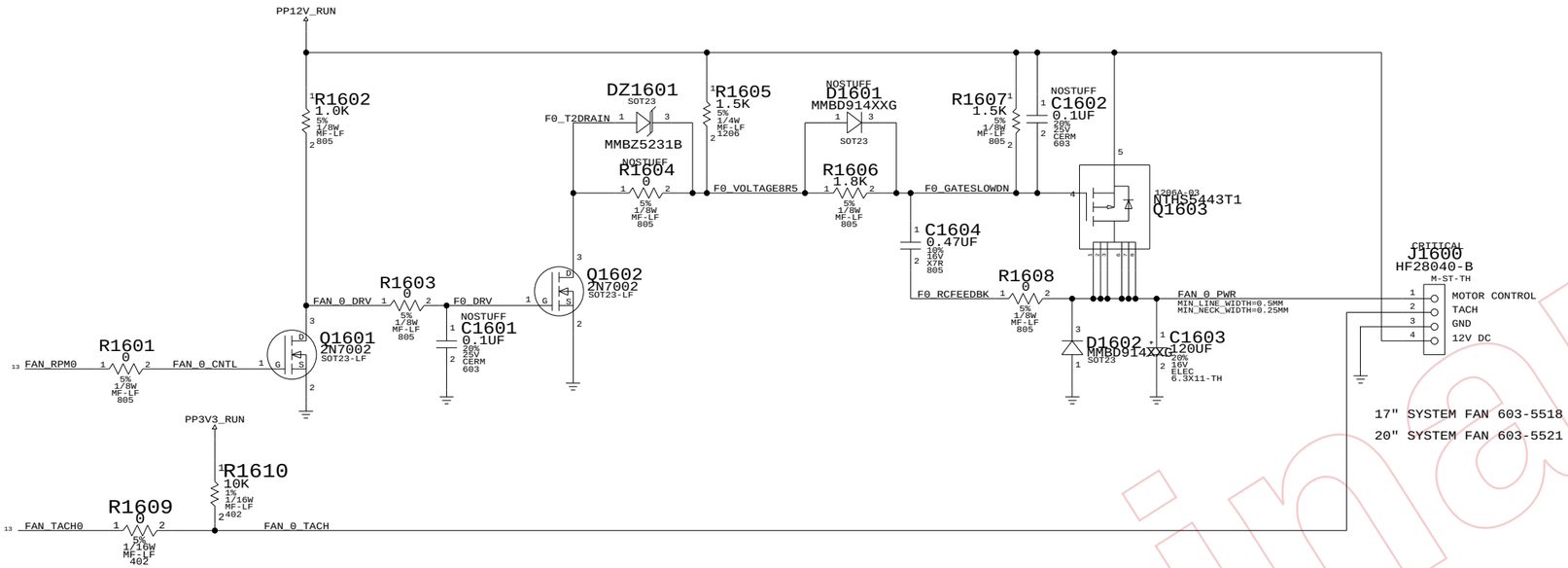


CPU LOGIC ANALYZER

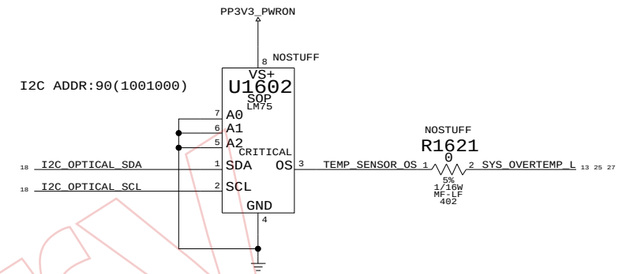
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE NONE	SHT 14 OF 102	

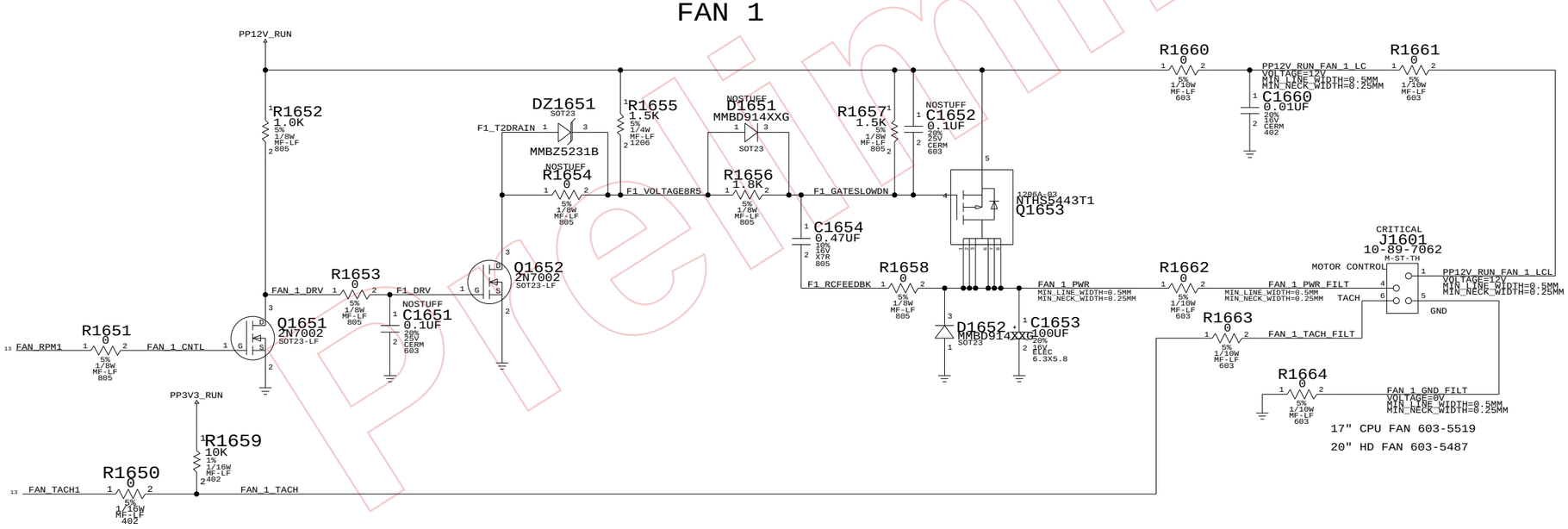
FAN 0



OPTICAL TEMP SENSOR



FAN 1

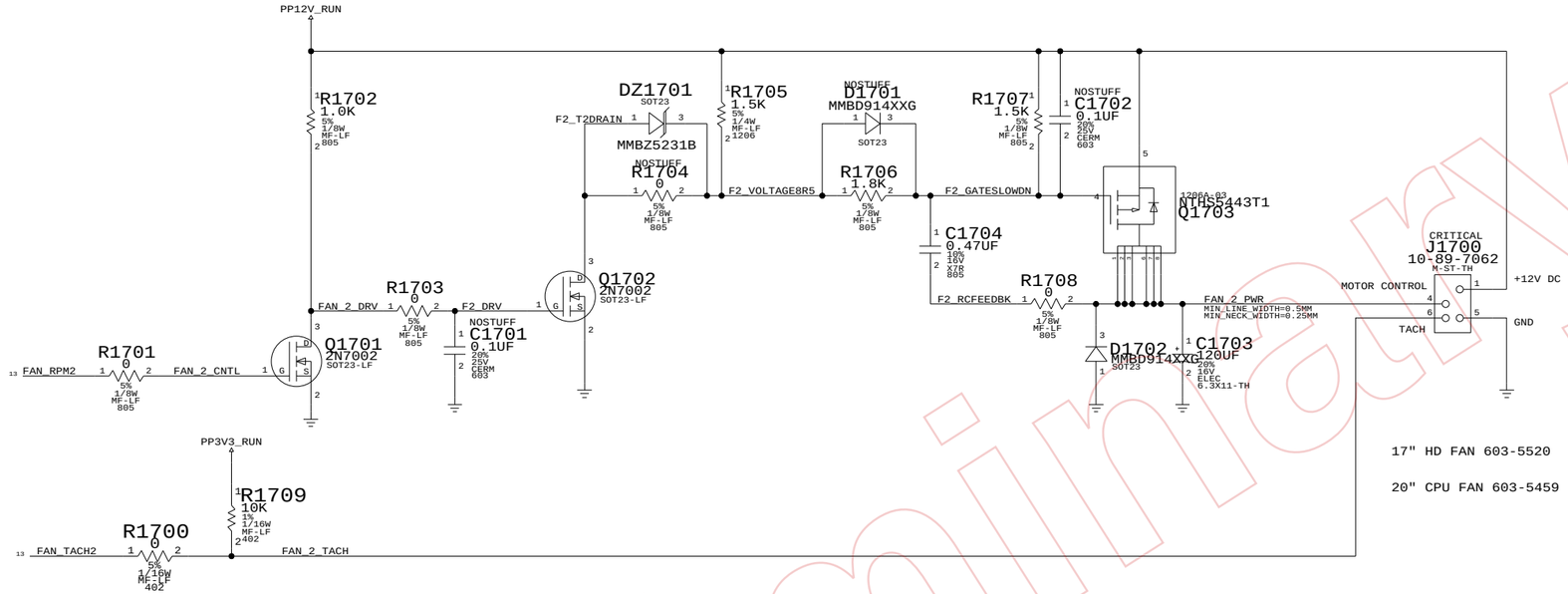


FAN 0, 1 & SYSTEM TEMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 16 OF 102	

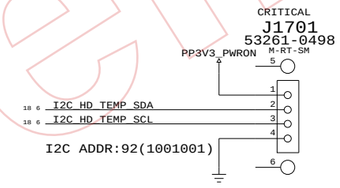
FAN 2



17" HD FAN 603-5520

20" CPU FAN 603-5459

REMOTE HARD DRIVE TEMP SENSOR



518S0193

FAN 2 & HD TEMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 17 OF 102	

I2C A BUS

R1832 0 603 NOSTUFF — 11 6 PP5V_PWRON — PP5V_U1800 — MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL
R1833 0 603 NOSTUFF — 11 10 7 6 PP5V_RUN

50 34 22 11 10 7 6 PP3V3_RUN — 58 27 18 11 6 PP3V3_PWRON

C1800 0.1UF 20% 10V CERM 402 — NOSTUFF R1809 4.7K 5% 1/16W MF-LF 402 — R1828 4.7K 5% 1/16W MF-LF 402 — C1802 0.1UF 20% 10V CERM 402 — R1808 200 5% 1/16W MF-LF 402 — R1810 200 5% 1/16W MF-LF 402 — =PP1V2_EI_NB 7 14 28

NOSTUFF R1830 2.0K 5% 1/16W MF-LF 402 — NOSTUFF R1831 2.0K 5% 1/16W MF-LF 402 — R1800 2.0K 5% 1/16W MF-LF 402 — R1801 2.0K 5% 1/16W MF-LF 402

SMU
MASTER
U1300
13 I2C_SMU_A_SDA_IN MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
14 13 6 I2C_SMU_A_SDA_OUT_L MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
13 I2C_SMU_A_SCL_IN MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
14 13 6 I2C_SMU_A_SCL_OUT_L MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 36-39

LM339A SOI U1800 GND — Q1800 2N7002DW SOT-363

U3LITE
U3
I2C_NB_A_SDA 24
I2C_NB_A_SCL 24
PINS A20, B20

NOSTUFF R1820 0 5% 1/16W MF-LF 402 — NOSTUFF R1821 0 5% 1/16W MF-LF 402

58 27 18 11 6 PP3V3_PWRON — R1819 2.0K 5% 1/16W MF-LF 402 — R1818 2.0K 5% 1/16W MF-LF 402

=PP1V2_EI_CPU 7 14 29 30 31 35 — R1816 200 5% 1/16W MF-LF 402 — R1817 200 5% 1/16W MF-LF 402

SMU
MASTER
U1300
13 I2C_SMU_CPU_SCL_IN MAKE_BASE=TRUE — I2C
13 I2C_SMU_CPU_SCL_OUT_L MAKE_BASE=TRUE — I2C
13 I2C_SMU_CPU_SDA_IN MAKE_BASE=TRUE — I2C
13 I2C_SMU_CPU_SDA_OUT_L MAKE_BASE=TRUE — I2C
PINS 14,25,23,68

RP1800 0 5% SM-LF
SMU_CPU_JTAG_OR_I2C — NET_SPACING_TYPE=I2C
I2C_CPU_A_SCL — NET_SPACING_TYPE=I2C
I2C_CPU_A_SDA_TO_SMU
I2C_CPU_A_SDA_TO_CPU

CPU
U2900
I2C_CPU_A_SCL 29
I2C_CPU_A_SDA 29
PINS AA20, Y21

LM339A SOI U1800 GND — Q1801 2N7002DW SOT-363 — I2C_CPU_SCL_LS

NOSTUFF RP1801 0 5% SM-LF — CPU JTAG
JTAG_CPU_TDO 29 30
JTAG_CPU_TDI 29 30
JTAG_CPU_TMS 29 30
JTAG_CPU_TCK 29 30

I2C_0V6_REF — C1801 0.1UF 20% 10V CERM 402 — R1811 4.7K 5% 1/16W MF-LF 402
USE 576 OHM FOR R1811 IF 5V RAIL IS USED FOR REFERENCE

I2C B BUS

PP3V3_PWRON — R1803 2.0K 5% 1/16W MF-LF 402 — R1802 2.0K 5% 1/16W MF-LF 402

SMU
MASTER
U1300
13 I2C_SMU_B_SDA MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
13 I2C_SMU_B_SCL MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 26, 27

PULSAR
U2600
27 I2C_CLOCK_SDA — ALIAS
27 I2C_CLOCK_SCL — ALIAS
PINS C1, B1

OPTICAL TEMP SENSOR
U1602
16 I2C_OPTICAL_SDA — ALIAS
16 I2C_OPTICAL_SCL — ALIAS
PINS 1, 2
I2C ADDR:90

AMBIENT LIGHT SENSOR
J2100
21 I2C_ALS_SDA — ALIAS
21 I2C_ALS_SCL — ALIAS
PINS 2, 3
I2C ADDR:94??
J2100 CAN BE USED AS A SECOND TEMP SENSOR

HD TEMP SENSOR
U1702
17 6 I2C_HD_TEMP_SDA — ALIAS
17 6 I2C_HD_TEMP_SCL — ALIAS
PINS 2, 3
I2C ADDR:92

GPU TEMP SENSOR
U5890
58 I2C_GPU_DIODE_SDA — ALIAS
58 I2C_GPU_DIODE_SCL — ALIAS
PINS 7, 8
I2C ADDR:98

I2C C BUS

PP2V5_PWRON — R1805 2.0K 5% 1/16W MF-LF 402 — R1804 2.0K 5% 1/16W MF-LF 402

NET_SPACING_TYPE=I2C — U3LITE MASTER U3 — I2C_NB_C_SDA MAKE_BASE=TRUE 24 — I2C_NB_C_SCL MAKE_BASE=TRUE 24 — PINS C21, E21
NET_SPACING_TYPE=I2C

DIMMS
J4000 = A0
J4001 = A2
ALIAS — I2C_DIMM_SDA 40
ALIAS — I2C_DIMM_SCL 40
PINS 91, 92
OF EACH DIMM

I2C D & E BUS

PP2V5_PWRON — R1812 2.0K 5% 1/16W MF-LF 402 — R1813 2.0K 5% 1/16W MF-LF 402
PP3V3_ALL — R1807 2.0K 5% 1/16W MF-LF 402 — R1806 2.0K 5% 1/16W MF-LF 402

U3LITE 'B'
U3
24 I2C_NB_B_SDA — I2C
24 I2C_NB_B_SCL — I2C
PINS C20, B21

RTC
U1301
I2C — I2C_RTC_SDA 13
I2C — I2C_RTC_SCL 13
PINS 5, 6

NOSTUFF R1822 0 5% 1/16W MF-LF 402 — NOSTUFF R1823 0 5% 1/16W MF-LF 402

NOSTUFF R1824 0 5% 1/16W MF-LF 402 — R1826 0 5% 1/16W MF-LF 402
NOSTUFF R1825 0 5% 1/16W MF-LF 402 — R1827 0 5% 1/16W MF-LF 402

SMU OLD 'E'
MASTER
U1300
13 I2C_SMU_E_SDA — I2C
13 I2C_SMU_E_SCL — I2C
PINS 50, 51

SMU NEW 'E'
MASTER
U1300
I2C — I2C_SMU_D_SDA 13
I2C — I2C_SMU_D_SCL 13
PINS 34, 35

I2C SB BUS

PP3V3_RUN — R1815 1K 5% 1/16W MF-LF 402 — R1814 1K 5% 1/16W MF-LF 402

SHASTA
MASTER
U2300
25 6 I2C_SB_SDA MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
25 6 I2C_SB_SCL MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS Y9, AB7

AUDIO
U9500 / AU300
95 I2C_AUDIO_SDA — ALIAS
95 I2C_AUDIO_SCL — ALIAS
PINS 18, 19

I2C CONNECTIONS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 18 OF 102	

TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS

PLACE THESE PARTS CLOSE TO SMU IC

SYS_LED_GREEN
MAKE_BASE=TRUE
PWM INPUT FROM SMU

R2101 0 5% 1/10W MF-LF 402
G_PWM_IN_H
R2109 953K 1% 1/10W MF-LF 402
R2104 953K 1% 1/10W MF-LF 402
R2105 200K 1% 1/10W MF-LF 402
C2106 0.47UF 20% 10V CERM 603
U2100 LP324 TSSOP
G_BASE_DRV
C2104 0.022UF 20% 16V CERM 402
G_PWM_DC
PP5V_PWRON
G_IN_OFFSET
5MV INPUT OFFSET
R2112 1K 1% 1/10W MF-LF 402

100% DUTY CYCLE OF 3V-PP PWM = 0.5V

C2105 220PF 5% 25V CERM 402 — GND_CHASSIS_LED
G_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2100 400-OHM-EMI SM-1
G_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
Q2102 2N3904LF SOT23
G_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2100 25.5 1% 1/16W MF-LF 402 <-- 17 INCH
CHANGE R2100 VALUE TO SET LED CURRENT
MAX LED CURRENT = 0.5 / R

LED2100 LATBG66B AMB-GRN-BLUE PLCC
AMB
GRN
BLUE
L2104 400-OHM-EMI SM-1
C2107 220PF 5% 25V CERM 402
C2108 220PF 5% 25V CERM 402
C2109 220PF 5% 25V CERM 402

PLACE THESE PARTS CLOSE TO SMU IC

SYS_LED_RED
MAKE_BASE=TRUE
PWM INPUT FROM SMU

R2115 0 5% 1/10W MF-LF 402
R_PWM_IN_H
R2102 953K 1% 1/10W MF-LF 402
R2110 953K 1% 1/10W MF-LF 402
R2111 200K 1% 1/10W MF-LF 402
C2112 0.47UF 20% 10V CERM 603
U2100 LP324 TSSOP
R_BASE_DRV
C2101 0.022UF 20% 16V CERM 402
R_PWM_DC
PP5V_PWRON
R_IN_OFFSET
R2114 1K 1% 1/10W MF-LF 402

R_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2101 400-OHM-EMI SM-1
R_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
Q2108 2N3904LF SOT23
R_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2113 25.5 1% 1/16W MF-LF 402 <-- 17 INCH

PLACE THESE PARTS CLOSE TO SMU IC

SYS_LED_BLUE
MAKE_BASE=TRUE
PWM INPUT FROM SMU

R2130 0 5% 1/10W MF-LF 402
B_PWM_IN_H
R2118 953K 1% 1/10W MF-LF 402
R2116 953K 1% 1/10W MF-LF 402
R2117 200K 1% 1/10W MF-LF 402
C2118 0.47UF 20% 10V CERM 603
U2100 LP324 TSSOP
B_BASE_DRV
C2102 0.022UF 20% 16V CERM 402
B_PWM_DC
PP5V_PWRON
B_IN_OFFSET
R2127 1K 1% 1/10W MF-LF 402

B_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2102 400-OHM-EMI SM-1
B_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
Q2114 2N3904LF SOT23
B_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2126 25.5 1% 1/16W MF-LF 402 <-- 17 INCH

RGB_LED_A MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2104 400-OHM-EMI SM-1 — PP5V_PWRON

PP3V3_PWRON
PP5V_PWRON
C2103 0.1UF 20% 10V CERM 402
U2100 LP324 TSSOP
U2100_UNUSED

PLACE THESE PARTS CLOSE TO SMU IC

PP3V3_PWRON
NOSTUFF Q2100 FDV302P SOT-23
NOSTUFF R2119 953K 1% 1/10W MF-LF 402
SYS_LED_H
WHITE_LED R2129 4.7K 5% 1/10W MF-LF 402
WHITE_LED R2106 1K 5% 1/10W MF-LF 402
SYS_GATE
NOSTUFF R2132 1K 5% 1/10W MF-LF 402
SYS_LED
PWM INPUT FROM SMU
SYS_LED_IN
WHITE_LED R2107 0 5% 1/10W MF-LF 402

(STUFF WHEN SYS_LED_L = ACTIVE HIGH)
(AND NO STUFF R2132, R2119 & Q2100)

AMBIENT LIGHT SENSOR

CRITICAL
J2100 53261-0498 M-RT-SM
PP3V3_PWRON
I2C_ALS_SDA
I2C_ALS_SCL
518S0193

J2100 CAN BE USED AS A SECOND TEMP SENSOR

LED2101
WHITE SM6
SYS_DRV_A MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
PP5V_PWRON
WHITE_LED R2120 0 5% 1/10W MF-LF 603
WHITE_LED C2111 220PF 5% 25V CERM 402
WHITE_LED C2110 220PF 5% 25V CERM 402 — GND_CHASSIS_LED
WHITE_LED R2121 0 5% 1/10W MF-LF 603
SYS_LED_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2103 56.2 1% 1/10W MF-LF 402
20_INCH_LCD
SYS_LED_DRV_C MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
WHITE_LED Q2101 FDV301N SM

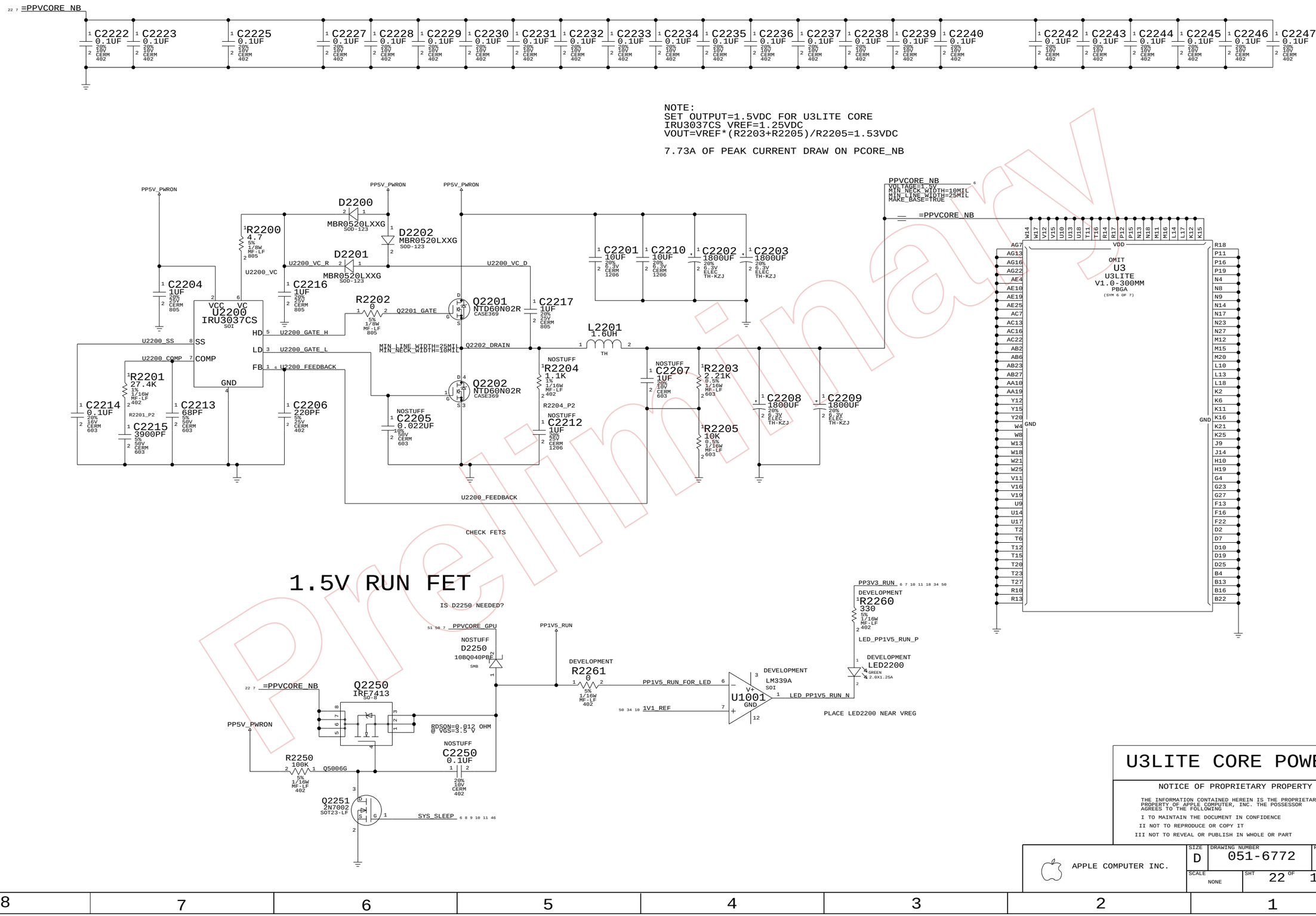
20 INCH -->

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
114S1821	3	RES, 18.2 OHM, 1%, 402	R2100,R2113,R2126	NOSTUFF

INDICATOR LED

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 21 OF 102	


=PPVCORE_NB
C2222 0.1UF 20% 10V CERM 402
C2223 0.1UF 20% 10V CERM 402
C2225 0.1UF 20% 10V CERM 402
C2227 0.1UF 20% 10V CERM 402
C2228 0.1UF 20% 10V CERM 402
C2229 0.1UF 20% 10V CERM 402
C2230 0.1UF 20% 10V CERM 402
C2231 0.1UF 20% 10V CERM 402
C2232 0.1UF 20% 10V CERM 402
C2233 0.1UF 20% 10V CERM 402
C2234 0.1UF 20% 10V CERM 402
C2235 0.1UF 20% 10V CERM 402
C2236 0.1UF 20% 10V CERM 402
C2237 0.1UF 20% 10V CERM 402
C2238 0.1UF 20% 10V CERM 402
C2239 0.1UF 20% 10V CERM 402
C2240 0.1UF 20% 10V CERM 402
C2242 0.1UF 20% 10V CERM 402
C2243 0.1UF 20% 10V CERM 402
C2244 0.1UF 20% 10V CERM 402
C2245 0.1UF 20% 10V CERM 402
C2246 0.1UF 20% 10V CERM 402
C2247 0.1UF 20% 10V CERM 402
NOTE:
SET OUTPUT=1.5VDC FOR U3LITE CORE
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R2203+R2205)/R2205=1.53VDC
7.73A OF PEAK CURRENT DRAW ON PCORE_NB
PP5V_PWRON
D2200 MBR0520LXXG SOD-123
D2202 MBR0520LXXG SOD-123
D2201 MBR0520LXXG SOD-123
R2200 4.7 5% 1/8W MF-LF 805
U2200_VC
U2200_VC_R
U2200_VC_D
C2204 1UF 20% 25V CERM 805
C2216 1UF 20% 25V CERM 805
U2200 IRU3037CS SOI
VCC_VC
SS
COMP
GND
HD
LD
FB
U2200_SS
U2200_COMP
U2200_GATE_H
U2200_GATE_L
U2200_FEEDBACK
R2202 0 5% 1/8W MF-LF 805
Q2201_GATE
Q2201 NTD60N02R CASE369
Q2202 NTD60N02R CASE369
C2217 1UF 20% 25V CERM 805
Q2202_DRAIN
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL
L2201 1.6UH TH
C2201 10UF 20% 6.3V CERM 1206
C2210 10UF 20% 6.3V CERM 1206
C2202 1800UF 20% 6.3V ELEC TH-KZJ
C2203 1800UF 20% 6.3V ELEC TH-KZJ
R2201 27.4K 1% 1/16W MF-LF 402
R2201_P2
C2214 0.1UF 20% 10V CERM 603
C2215 3900PF 5% 50V CERM 603
C2213 68PF 5% 50V CERM 603
C2206 220PF 5% 50V CERM 402
C2205 NOSTUFF 0.022UF 10% 50V CERM 603
R2204 1.1K 1% 1/16W MF-LF 402
R2204_P2
C2212 NOSTUFF 1UF 20% 25V CERM 1206
C2207 NOSTUFF 1UF 20% 10V CERM 603
R2203 2.21K 0.5% 1/16W MF-LF 603
R2205 10K 0.5% 1/16W MF-LF 603
C2208 1800UF 20% 6.3V ELEC TH-KZJ
C2209 1800UF 20% 6.3V ELEC TH-KZJ
PPVCORE_NB
VOLTAGE=1.5V
MIN_NECK_WIDTH=10MIL
MIN_LINE_WIDTH=25MIL
MAKE_BASE=TRUE
=PPVCORE_NB
OMIT
U3
U3LITE
V1.0-300MM
PBGA
(SYM 6 OF 7)
VDD
GND
AG7 AG13 AG16 AG22 AE4 AE10 AE19 AE25 AC7 AC13 AC16 AC22 AB2 AB6 AB23 AB27 AA10 AA19 Y12 Y15 Y20 W4 W8 W13 W18 W21 W25 V11 V16 V19 U9 U14 U17 T2 T6 T12 T15 T20 T23 T27 R10 R13
R18 P11 P16 P19 N4 N8 N9 N14 N17 N23 N27 M12 M15 M20 L10 L13 L18 K2 K6 K11 K16 K21 K25 J9 J14 H10 H19 G4 G23 G27 F13 F16 F22 D2 D7 D10 D19 D25 B4 B13 B16 B22
CHECK FETS
1.5V RUN FET
IS D2250 NEEDED?
PPVCORE_GPU
NOSTUFF D2250 10BQ040PBF SMB
PP1V5_RUN
DEVELOPMENT R2261 0 5% 1/16W MF-LF 402
PP1V5_RUN_FOR_LED
1V1_REF
DEVELOPMENT U1001 LM339A SOI
LED_PP1V5_RUN_N
PP3V3_RUN
DEVELOPMENT R2260 330 5% 1/16W MF-LF 402
LED_PP1V5_RUN_P
DEVELOPMENT LED2200 GREEN 2.0X1.25A
PLACE LED2200 NEAR VREG
=PPVCORE_NB
Q2250 IRF7413 SO-8
RDSON=0.012 OHM @ VGS=3.5 V
NOSTUFF C2250 0.1UF 20% 10V CERM 402
R2250 100K 5% 1/16W MF-LF 402
Q5006G
Q2251 2N7002 SOT23-LF
SYS_SLEEP
U3LITE CORE POWER
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6772
REV. 04
SCALE NONE
SHT 22 OF 102

Page Notes

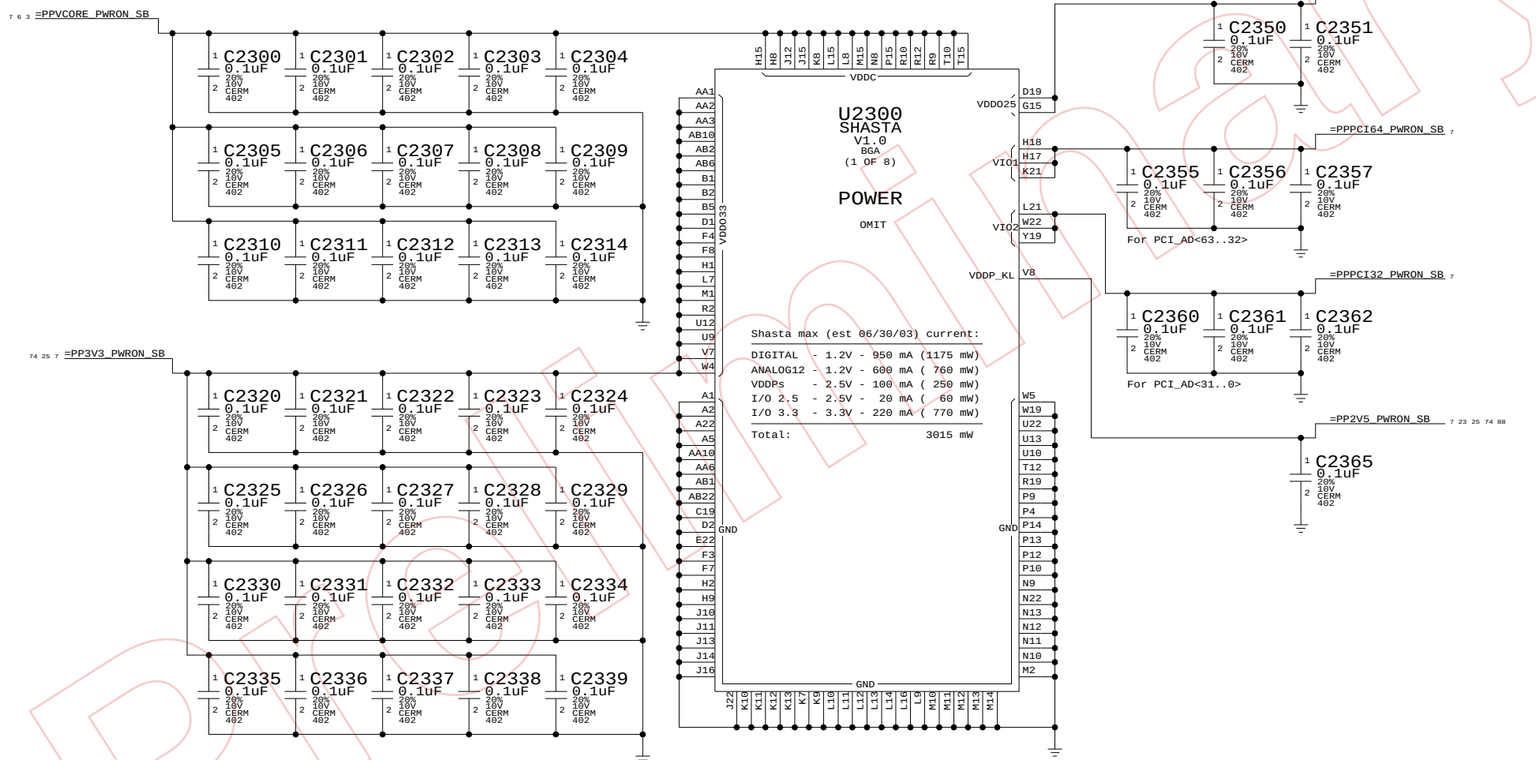
Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

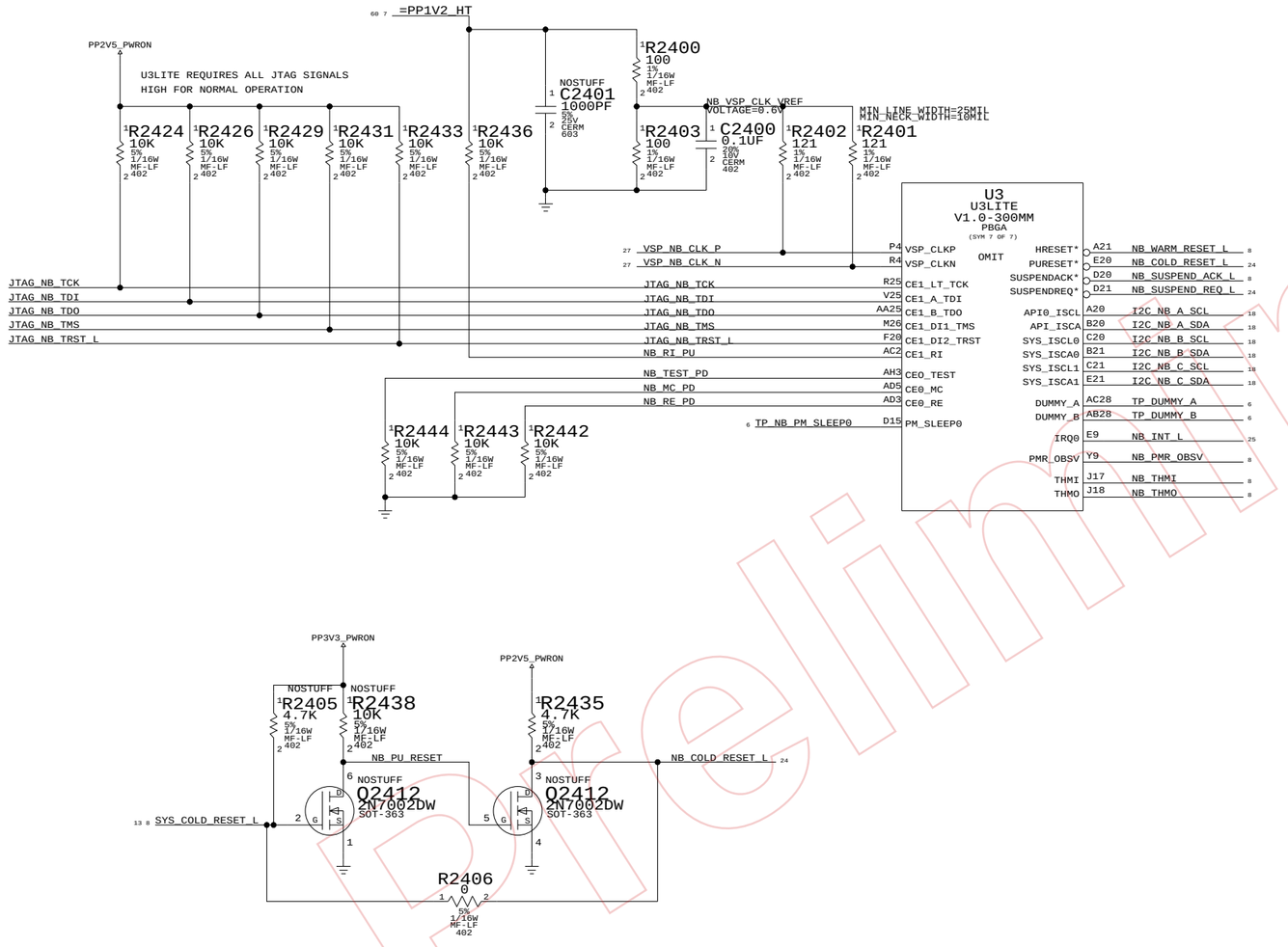


Master: Link

Shasta Core Power

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 23 OF 102	



MASTER: GILA
LAST MODIFIED: JUNE 10, 04

U3LITE MISC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 24 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI	25 95
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO	25 95
I2S0_TO_DEV	AUDIO		I2S0_MCLK	25 102
I2S0_BIDIR			I2S0_BITCLK	25 102
I2S0_BIDIR			I2S0_SYNC	25 95
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI	6 25 94
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO	6 25 94
I2S1_TO_DEV	10 MIL SPACING		I2S1_MCLK	6 25 94
I2S1_BIDIR			I2S1_BITCLK	6 25 94
I2S1_BIDIR			I2S1_SYNC	6 25 94
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI	25 102
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO	25 102
I2S2_TO_DEV	10 MIL SPACING		I2S2_MCLK	25 102
I2S2_BIDIR			I2S2_BITCLK	25 102
I2S2_BIDIR			I2S2_SYNC	25 102
SB_CLK18M_XTAL	15 MIL SPACING		SB_CLK18M_XTALI	25
	15 MIL SPACING		SB_CLK18M_XTALO	25
	15 MIL SPACING		SB_CLK18M_XTALO_R	25
SB_CLK25M_ATA	15 MIL SPACING		SB_CLK25M_ATA	25 27

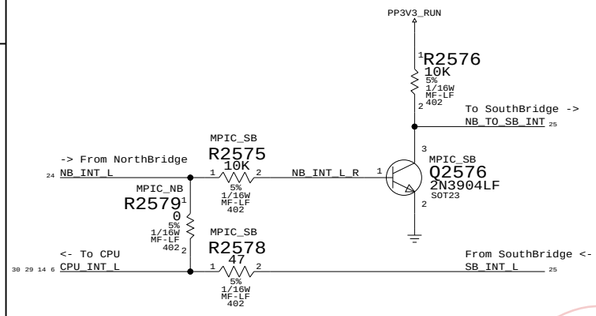
Page Notes

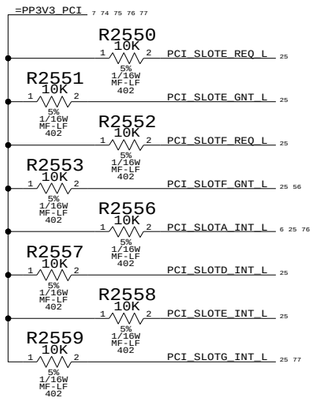
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

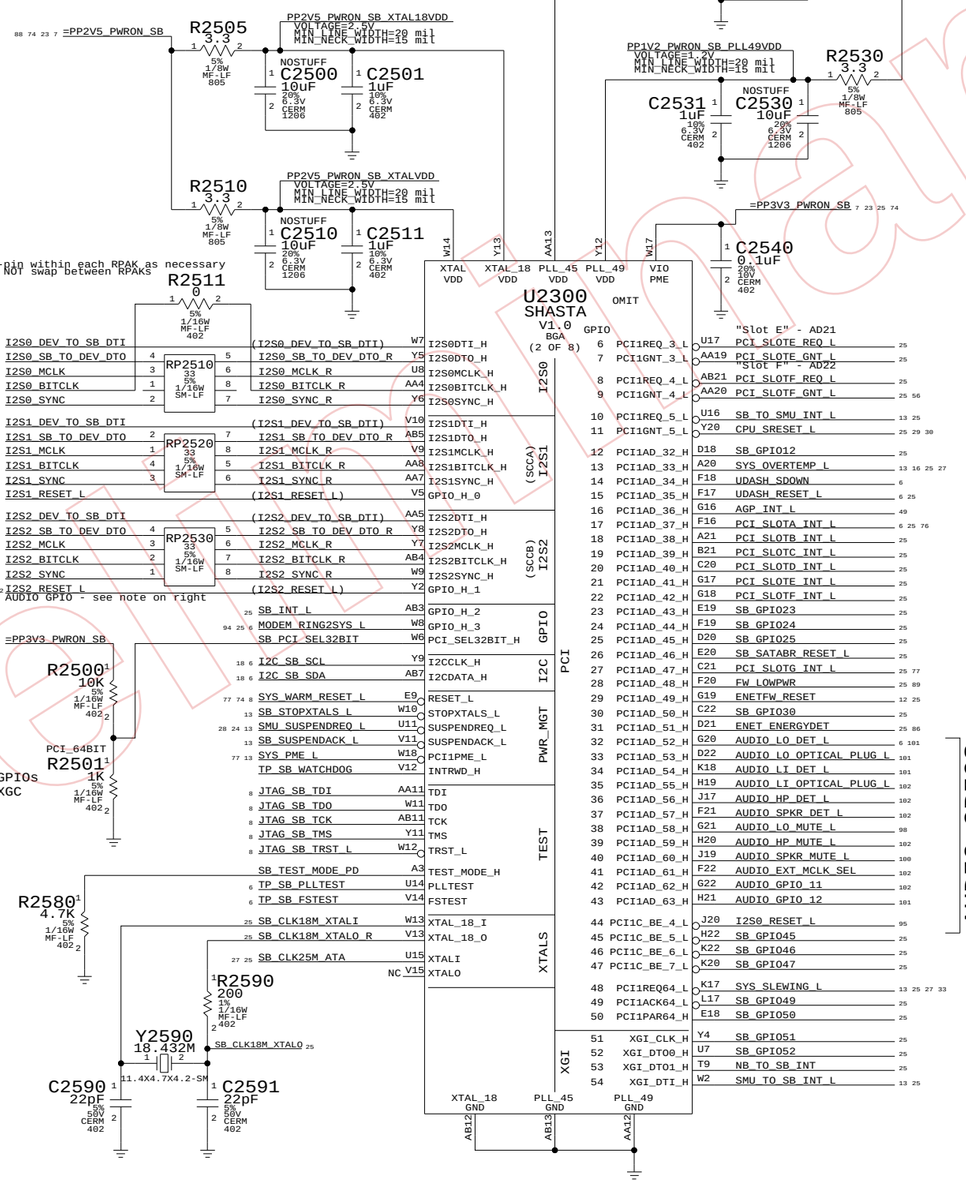
Signal aliases required by this page:
(NONE)

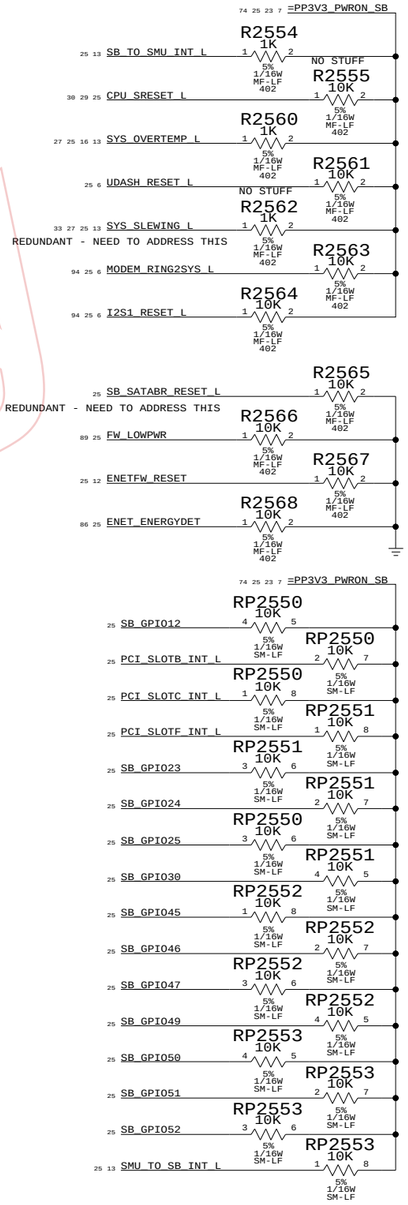
BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing









AUDIO GPIOS

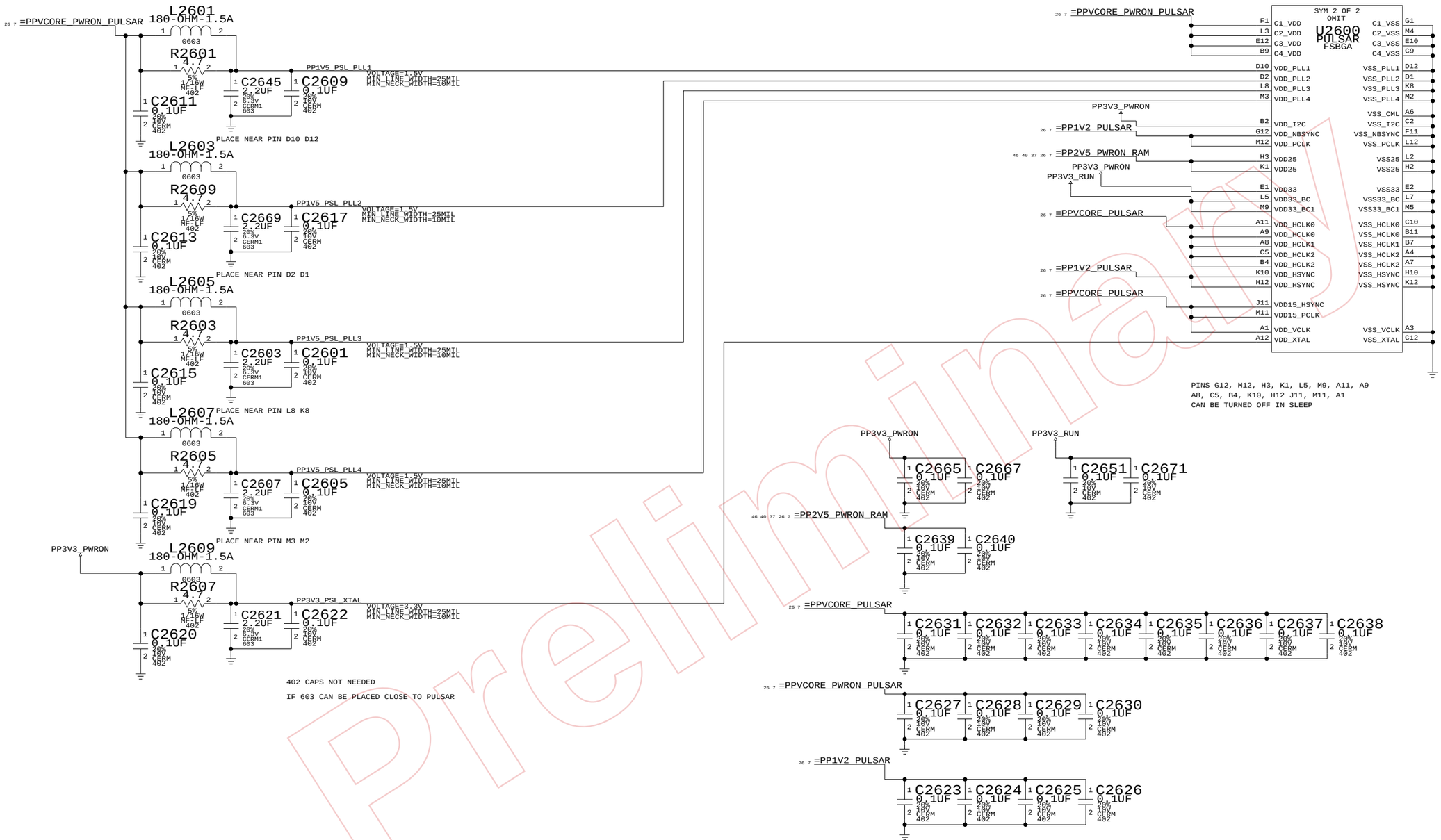
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

MASTER: SEEDY

Shasta Serial / Misc

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 25 OF 102	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

MASTER: GILA
LAST MODIFIED: APR 09, 04

PULSAR POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 26 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK
EI_CPU_SYNC	EI_SYNC	CLOCKS	
EI_NB_SYNC		CLOCKS	
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS	
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS	
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS	
HT_CLK66M_NB	HT_NB_CLK	CLOCKS	
HT_CLK66M_SB	HT_SB_CLK	CLOCKS	
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS	
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS	
PLS_EXTCLK	PLS_XTAL	CLOCKS	
CPU_HTBEN		CLOCKS	

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

NET SPACING TYPE

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS	
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS	
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS	
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS	
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS	
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS 14	
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS	
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS	
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS 14	
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS	
GPCLK25_0	J3	6 PLS_CLK_66M_0_R	CLOCKS	
GPCLK25_1	J1	6 PLS_CLK_66M_1_R	CLOCKS	
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS	
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS	
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS	
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS	
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS	
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS	
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS	
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS	
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS 14	
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS	
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS	
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS 14	
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS	
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS	
SLEWING*	K9	SLEWING_L_R	CLOCKS	
ERROR*	M8	CLOCK_ERROR_L 8		
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS	
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS	

SCLK	C1	18 I2C_CLOCK_SCL		
SDATA	B1	18 I2C_CLOCK_SDA		
RESET*	D3	PLS_RESET_L	13 CLOCK_RESET_L	R2704 0 5% 402
XIN	C11	PLS_X_IN		
XOUT	B12	PLS_X_OUT		
ADDRSEL	E3	PLS_X_ADDRSEL		NOSTUFF R2738 1K 5% 402
TEST1	K3	6 TP_PLS_TEST1		
TEST2	E11	6 TP_PLS_TEST2		
TEST3	D11	6 TP_PLS_TEST3		
SCAN_MODE	M1	PLS_SCAN_MODE		R2706 249 1%
REF15	G11	PLS_REF15		R2744 681 1%
REF25	J2	PLS_REF25		R2740 1K 1%
REF33	M6	PLS_REF33		R2746 1K 1%
REF_CML	A5	6 TP_PLS_REF_CML		
PRES_CML	B6	PLS_PRES_CML		R2742 806 1%
FORCESPO*	F2	PLS_FORCE_P0_L_R	25 16 13 SYS_OVERTEMP_L	R2748 0 5% 1/16W MF-LF 402 NOSTUFF; R2722 1K 5% 1/16W MF-LF 402; 58 18 11 6 PP3V3_PWRON
PD	C3	PLS_POWER_DOWN_R	3 =PULSAR_POWER_DOWN	R2750 47 5%
				R2724 1K 5% NOSTUFF

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

J2700 U.FL-R_SMT F-ST-SM; NOSTUFF R2762 24 5% 1/16W MF-LF 402; NOSTUFF R2764 24 5% 1/16W MF-LF 402; PLS_INTERM; 17 PLS_EXTCLK; NO STUFF R2752 0 5% 1/16W MF-LF 402; NO STUFF R2758 330K 5% 1/16W MF-LF 402; R2754 0 5% 1/16W MF-LF 402; R2756 0 5% 1/16W MF-LF 402; CRITICAL Y2701 25.0000M 8X4.5MM-SM; PLS_X_IN_B; PLS_X_OUT_B; C2707 33PF 5% 50V CERM 402; C2705 33PF 5% 50V CERM 402

PCI_CLK_GP0	8	3.3V	33MHZ	R2701 0 5%
PCI_CLK_GP1	8	3.3V	33MHZ	R2761 0 5% 402
VSP_NB_CLK_P	24 27			C2708 0.001UF 50V 10% 2CERM 402
VSP_NB_CLK_N	24 27			C2710 0.001UF 50V 10% 2CERM 402
EI_CPU_CLK_P	27 29			C2713 0.001UF 50V 10% 2CERM 402
EI_CPU_CLK_N	27 29			C2715 0.001UF 50V 10% 2CERM 402
EI_NB_CLK_P	27 28			C2700 0.001UF 50V 10% 2CERM 402
EI_NB_CLK_N	27 28			C2702 0.001UF 50V 10% 2CERM 402
TP_PLS_CLK_66M_0	6	2.5V	66MHZ	NOSTUFF R2775 0 5% 402
TP_PLS_CLK_66M_1	6	2.5V	66MHZ	R2776 0 5% 402
HT_CLK66M_NB	27 60	2.5V	66MHZ	20 R2703 5% 402
RAM_CLK66M_NB	37	2.5V	66MHZ	20 R2709 5% 402
PCI_CLK66M_SB_INT	27 74	3.3V	66MHZ	R2705 0 5% 402
PCI_CLK_P1	8	3.3V	33MHZ	R2711 0 5% 402
AGP_CLK66M_GPU	27 49	3.3V	66MHZ	R2707 0 5% 402
PCI_CLK_P3	8	3.3V	33MHZ	R2702 0 5% 402
PCI_CLK_P4	8			R2779 0 5% 402
CPU_HTBEN	27 29 30	1.2V	33MHZ	R2715 0 5% 402
EI_NB_SYNC	27 28	1.2V		R2768 0 5% 402
EI_CPU_SYNC	27 29	1.2V		R2772 0 5% 402
SB_CLK25M_ATA	25	2.5V	25MHZ	NOSTUFF 20 R2770 5% 402
TP_SATA_CLK25M	6	2.5V	25MHZ	22 R2700 5% 402
SYS_SLEWING_L	13 25 33			R2720 0 5% 402
HT_CLK66M_SB	27 62	1.2V	66MHZ	R2717 0 5% 402
AGP_CLK66M_NB	27 48	1.5V	66MHZ	R2719 0 5% 402

MASTER: SEEDY
LAST MODIFIED: NOV 22, 04

PULSAR CLOCKS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 27 OF 102	

=PP1V2_EI_NB 7 14 18 28

C2800 0.1UF 20% 10V CERM 402
C2801 0.1UF 20% 10V CERM 402
C2802 0.1UF 20% 10V CERM 402
C2803 0.1UF 20% 10V CERM 402
C2804 0.1UF 20% 10V CERM 402
C2805 0.1UF 20% 10V CERM 402
C2806 0.1UF 20% 10V CERM 402
C2807 0.1UF 20% 10V CERM 402
C2808 0.1UF 20% 10V CERM 402
C2809 0.1UF 20% 10V CERM 402
C2810 0.1UF 20% 10V CERM 402
C2811 0.1UF 20% 10V CERM 402
C2812 0.1UF 20% 10V CERM 402
C2813 0.1UF 20% 10V CERM 402
C2814 0.1UF 20% 10V CERM 402
C2815 0.1UF 20% 10V CERM 402
C2816 0.1UF 20% 10V CERM 402
C2817 0.1UF 20% 10V CERM 402

60 48 37 7 =PP1V5_PWRON_NB_AVDD

R2800 2.2 5% 1/10W MF-LF 603

PP1V5_PWRON_EI_NB_AVDD
VOLTAGE=1.5V
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL

C2818 1UF 10% 6.3V CERM 402
C2819 0.1UF 20% 10V CERM 402

=PP1V2_EI_NB 7 14 18 28

U3
U3LITE
V1.0-300MM
PBGA
(SYN 1 OF 7)

OMIT

APPLE PI INTERFACE

	EI_NB_TO_CPU_CLK_P	F15	API0_BCLKIP
	EI_NB_TO_CPU_CLK_N	E15	API0_BCLKIN
	EI_NB_TO_CPU_AD<0>	F11	API0_ADI0
	EI_NB_TO_CPU_AD<1>	F12	API0_ADI1
	EI_NB_TO_CPU_AD<2>	G11	API0_ADI2
	EI_NB_TO_CPU_AD<3>	H11	API0_ADI3
	EI_NB_TO_CPU_AD<4>	G12	API0_ADI4
	EI_NB_TO_CPU_AD<5>	H12	API0_ADI5
	EI_NB_TO_CPU_AD<6>	H14	API0_ADI6
	EI_NB_TO_CPU_AD<7>	G14	API0_ADI7
	EI_NB_TO_CPU_AD<8>	D9	API0_ADI8
	EI_NB_TO_CPU_AD<9>	C9	API0_ADI9
	EI_NB_TO_CPU_AD<10>	D11	API0_ADI10
	EI_NB_TO_CPU_AD<11>	E11	API0_ADI11
	EI_NB_TO_CPU_AD<12>	A10	API0_ADI12
	EI_NB_TO_CPU_AD<13>	A9	API0_ADI13
	EI_NB_TO_CPU_AD<14>	A8	API0_ADI14
	EI_NB_TO_CPU_AD<15>	B9	API0_ADI15
	EI_NB_TO_CPU_AD<16>	C11	API0_ADI16
	EI_NB_TO_CPU_AD<17>	B11	API0_ADI17
	EI_NB_TO_CPU_AD<18>	A11	API0_ADI18
	EI_NB_TO_CPU_AD<19>	A12	API0_ADI19
	EI_NB_TO_CPU_AD<20>	B12	API0_ADI20
	EI_NB_TO_CPU_AD<21>	C12	API0_ADI21
	EI_NB_TO_CPU_AD<22>	D12	API0_ADI22
	EI_NB_TO_CPU_AD<23>	E12	API0_ADI23
	EI_NB_TO_CPU_AD<24>	A13	API0_ADI24
	EI_NB_TO_CPU_AD<25>	A14	API0_ADI25
	EI_NB_TO_CPU_AD<26>	B14	API0_ADI26
	EI_NB_TO_CPU_AD<27>	C14	API0_ADI27
	EI_NB_TO_CPU_AD<28>	A16	API0_ADI28
	EI_NB_TO_CPU_AD<29>	A15	API0_ADI29
	EI_NB_TO_CPU_AD<30>	B15	API0_ADI30
	EI_NB_TO_CPU_AD<31>	C15	API0_ADI31
	EI_NB_TO_CPU_AD<32>	H15	API0_ADI32
	EI_NB_TO_CPU_AD<33>	G15	API0_ADI33
	EI_NB_TO_CPU_AD<34>	F17	API0_ADI34
	EI_NB_TO_CPU_AD<35>	G17	API0_ADI35
	EI_NB_TO_CPU_AD<36>	G18	API0_ADI36
	EI_NB_TO_CPU_AD<37>	H18	API0_ADI37
	EI_NB_TO_CPU_AD<38>	F18	API0_ADI38
	EI_NB_TO_CPU_AD<39>	E18	API0_ADI39
	EI_NB_TO_CPU_AD<40>	A17	API0_ADI40
	EI_NB_TO_CPU_AD<41>	A18	API0_ADI41
	EI_NB_TO_CPU_AD<42>	B17	API0_ADI42
	EI_NB_TO_CPU_AD<43>	C17	API0_ADI43
	EI_NB_TO_CPU_SR_P<0>	D17	API0_SRIP0
	EI_NB_TO_CPU_SR_N<0>	A19	API0_SRIN0
	EI_NB_TO_CPU_SR_P<1>	E17	API0_SRIP1
	EI_NB_TO_CPU_SR_N<1>	B18	API0_SRIN1
	EI_QACK_L	D14	API_QACK0
		E8	API0_APSYNC
		H17	API0_SE

	API_BCLKOP	D6	EI_CPU_TO_NB_CLK_P
	API_BCLKON	E6	EI_CPU_TO_NB_CLK_N
	API0_AD0	J2	EI_CPU_TO_NB_AD<0>
	API0_AD1	H1	EI_CPU_TO_NB_AD<1>
	API0_AD2	J1	EI_CPU_TO_NB_AD<2>
	API0_AD3	K1	EI_CPU_TO_NB_AD<3>
	API0_AD4	E1	EI_CPU_TO_NB_AD<4>
	API0_AD5	F2	EI_CPU_TO_NB_AD<5>
	API0_AD6	J4	EI_CPU_TO_NB_AD<6>
	API0_AD7	H4	EI_CPU_TO_NB_AD<7>
	API0_AD8	G1	EI_CPU_TO_NB_AD<8>
	API0_AD9	H2	EI_CPU_TO_NB_AD<9>
	API0_AD10	F1	EI_CPU_TO_NB_AD<10>
	API0_AD11	H5	EI_CPU_TO_NB_AD<11>
	API0_AD12	H3	EI_CPU_TO_NB_AD<12>
	API0_AD13	J3	EI_CPU_TO_NB_AD<13>
	API0_AD14	J5	EI_CPU_TO_NB_AD<14>
	API0_AD15	J6	EI_CPU_TO_NB_AD<15>
	API0_AD16	E3	EI_CPU_TO_NB_AD<16>
	API0_AD17	F4	EI_CPU_TO_NB_AD<17>
	API0_AD18	E2	EI_CPU_TO_NB_AD<18>
	API0_AD19	F5	EI_CPU_TO_NB_AD<19>
	API0_AD20	H6	EI_CPU_TO_NB_AD<20>
	API0_AD21	J7	EI_CPU_TO_NB_AD<21>
	API0_AD22	F3	EI_CPU_TO_NB_AD<22>
	API0_AD23	J8	EI_CPU_TO_NB_AD<23>
	API0_AD24	F6	EI_CPU_TO_NB_AD<24>
	API0_AD25	E5	EI_CPU_TO_NB_AD<25>
	API0_AD26	D5	EI_CPU_TO_NB_AD<26>
	API0_AD27	E4	EI_CPU_TO_NB_AD<27>
	API0_AD28	D8	EI_CPU_TO_NB_AD<28>
	API0_AD29	A5	EI_CPU_TO_NB_AD<29>
	API0_AD30	C2	EI_CPU_TO_NB_AD<30>
	API0_AD31	C3	EI_CPU_TO_NB_AD<31>
	API0_AD32	C5	EI_CPU_TO_NB_AD<32>
	API0_AD33	C6	EI_CPU_TO_NB_AD<33>
	API0_AD34	B2	EI_CPU_TO_NB_AD<34>
	API0_AD35	D1	EI_CPU_TO_NB_AD<35>
	API0_AD36	B1	EI_CPU_TO_NB_AD<36>
	API0_AD37	C1	EI_CPU_TO_NB_AD<37>
	API0_AD38	A6	EI_CPU_TO_NB_AD<38>
	API0_AD39	C8	EI_CPU_TO_NB_AD<39>
	API0_AD40	A2	EI_CPU_TO_NB_AD<40>
	API0_AD41	B3	EI_CPU_TO_NB_AD<41>
	API0_AD42	A7	EI_CPU_TO_NB_AD<42>
	API0_AD43	B8	EI_CPU_TO_NB_AD<43>
	API0_SROP0	A3	EI_CPU_TO_NB_SR_P<0>
	API0_SRON0	A4	EI_CPU_TO_NB_SR_N<0>
	API0_SROP1	B5	EI_CPU_TO_NB_SR_P<1>
	API0_SRON1	B6	EI_CPU_TO_NB_SR_N<1>
	API_QREQ0	E14	
	API_APCLKP	D18	EI_NB_CLK_P
	API_APCLKN	C18	EI_NB_CLK_N
	API_CSTP	F14	CPU_CHKSTOP_L

	EI_CPU_TO_NB_CLK_P	EI_CLK	EI_CPU_TO_NB_CLK
	EI_CPU_TO_NB_CLK_N	EI_CLK	EI_CPU_TO_NB_CLK
	EI_NB_TO_CPU_CLK_P	EI_CLK	EI_NB_TO_CPU_CLK
	EI_NB_TO_CPU_CLK_N	EI_CLK	EI_NB_TO_CPU_CLK
	EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD
	EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD
	EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
	EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
	EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
	EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK
	EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK
	EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK
	EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK
	EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK

	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	
	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	
	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	
	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	
	EI_CPU_TO_NB_CAD		
	EI_NB_TO_CPU_CAD		
	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	
	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	
	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	
	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	
	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	
	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	
	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	
	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	

ZT2847 ZT2857 ZT2867 ZT2807 ZT2817 ZT2827 ZT2837
ZT2848 ZT2858 ZT2868 ZT2808 ZT2818 ZT2828 ZT2838
ZT2849 ZT2859 ZT2869 ZT2809 ZT2819 ZT2829 ZT2839
ZT2850 ZT2860 ZT2800 ZT2810 ZT2820 ZT2830 ZT2840
ZT2851 ZT2861 ZT2801 ZT2811 ZT2821 ZT2831 ZT2841
ZT2852 ZT2862 ZT2802 ZT2812 ZT2822 ZT2832 ZT2842
ZT2853 ZT2863 ZT2803 ZT2813 ZT2823 ZT2833 ZT2843
ZT2854 ZT2864 ZT2804 ZT2814 ZT2824 ZT2834 ZT2844
ZT2855 ZT2865 ZT2805 ZT2815 ZT2825 ZT2835 ZT2845
ZT2806 ZT2816 ZT2826 ZT2836
ZT2846 ZT2856 ZT2866

OMIT HOLE-VIA-20R10

=PP1V2_EI_NB 7 14 18 28

R2802 100 1% 1/10W MF-LF 402

NOSTUFF C2821 0.001UF 10% 50V CERM 402

EI_APCLK_VREF
VOLTAGE=0.6V

NOSTUFF R2801 100 1% 1/10W MF-LF 402

NOSTUFF C2820 0.1UF 20% 10V CERM 402

NOSTUFF R2803 121 1% 1/10W MF-LF 402

NOSTUFF R2804 121 1% 1/10W MF-LF 402

MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL

EI_NB_CLK_P 27
EI_NB_CLK_N 27

PLACE R2805 AND R2806 NEAR U3LITE

R2805 0 402

27 EI_NB_SYNC — NB_APSYNC

NOSTUFF R2806 0 402

29 EI_SYNC_FROM_NB
30 29 14 6 EI_SE

API_APCLK_AVSS

G20

QREQ_L HACK

28 7 =PP3V3_PWRON_EI

C2850 0.1UF 20% 10V CERM 402

CRITICAL
U2850
74LVC1G66DBVG4
SOT23-5
TI

VCC
GND

30 29 14 6 EI_QREQ_L
25 24 13 SMU_SUSPENDREQ_L

EI_NB_QREQ_L

NOSTUFF R2850 0 5% 1/16W MF-LF 402

R2851 10K 5% 1/16W MF-LF 402

NOSTUFF R2899 180 5% 1/10W MF-LF 402

EI_NB_QREQ_L_R

QREQ TO SMU

28 7 =PP3V3_PWRON_EI

NOSTUFF R2898 10K 5% 1/16W MF-LF 402

SMU_QREQ 13

NOSTUFF Q2899 2N3904LF SOT23

POST-RAMP QUAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
353S0920	353S0867		U2850	PERICOM ANALOG SWITCH	CRITICAL

PLACE QREQ CIRCUITS BETWEEN CPU AND U3LITE

MASTER: SEEDY
LAST MODIFIED: NOV 4, 04

U3LITE APPLE PI

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 28 OF 102	

PLACE AT PROCESSOR PINS.

PLACE NEAR PROCESSOR.

27 EI_CPU_CLK_P

27 EI_CPU_CLK_N

NOSTUFF R2903 46.4 1% 1/10W MF-LF 402

NOSTUFF R2901 46.4 1% 1/10W MF-LF 402

NOSTUFF C2901 0.22UF 20% 6.3V X5R 402

SYSCLK_TERM VOLTAGE=0.6V

35 31 30 29 18 14 7 =PP1V2_EI_CPU

NOSTUFF R2909 100 1% 1/16W MF-LF 402

NOSTUFF R2907 100 1% 1/16W MF-LF 402

SYSCLK* SYSCLK

OMIT CRITICAL

U2900 CBGA (1 OF 3)

NEO-10S-REV2 1.8GHZ-76C

28 14 6 EI_NB_TO_CPU_CLK_P
28 14 6 EI_NB_TO_CPU_CLK_N

28 14 6 EI_NB_TO_CPU_AD<0>
28 14 6 EI_NB_TO_CPU_AD<1>
28 14 6 EI_NB_TO_CPU_AD<2>
28 14 6 EI_NB_TO_CPU_AD<3>
28 14 6 EI_NB_TO_CPU_AD<4>
28 14 6 EI_NB_TO_CPU_AD<5>
28 14 6 EI_NB_TO_CPU_AD<6>
28 14 6 EI_NB_TO_CPU_AD<7>
28 14 6 EI_NB_TO_CPU_AD<8>
28 14 6 EI_NB_TO_CPU_AD<9>
28 14 6 EI_NB_TO_CPU_AD<10>
28 14 6 EI_NB_TO_CPU_AD<11>
28 14 6 EI_NB_TO_CPU_AD<12>
28 14 6 EI_NB_TO_CPU_AD<13>
28 14 6 EI_NB_TO_CPU_AD<14>
28 14 6 EI_NB_TO_CPU_AD<15>
28 14 6 EI_NB_TO_CPU_AD<16>
28 14 6 EI_NB_TO_CPU_AD<17>
28 14 6 EI_NB_TO_CPU_AD<18>
28 14 6 EI_NB_TO_CPU_AD<19>
28 14 6 EI_NB_TO_CPU_AD<20>
28 14 6 EI_NB_TO_CPU_AD<21>
28 14 6 EI_NB_TO_CPU_AD<22>
28 14 6 EI_NB_TO_CPU_AD<23>
28 14 6 EI_NB_TO_CPU_AD<24>
28 14 6 EI_NB_TO_CPU_AD<25>
28 14 6 EI_NB_TO_CPU_AD<26>
28 14 6 EI_NB_TO_CPU_AD<27>
28 14 6 EI_NB_TO_CPU_AD<28>
28 14 6 EI_NB_TO_CPU_AD<29>
28 14 6 EI_NB_TO_CPU_AD<30>
28 14 6 EI_NB_TO_CPU_AD<31>
28 14 6 EI_NB_TO_CPU_AD<32>
28 14 6 EI_NB_TO_CPU_AD<33>
28 14 6 EI_NB_TO_CPU_AD<34>
28 14 6 EI_NB_TO_CPU_AD<35>
28 14 6 EI_NB_TO_CPU_AD<36>
28 14 6 EI_NB_TO_CPU_AD<37>
28 14 6 EI_NB_TO_CPU_AD<38>
28 14 6 EI_NB_TO_CPU_AD<39>
28 14 6 EI_NB_TO_CPU_AD<40>
28 14 6 EI_NB_TO_CPU_AD<41>
28 14 6 EI_NB_TO_CPU_AD<42>
28 14 6 EI_NB_TO_CPU_AD<43>

28 14 6 EI_NB_TO_CPU_SR_P<0>
28 14 6 EI_NB_TO_CPU_SR_N<0>
28 14 6 EI_NB_TO_CPU_SR_P<1>
28 14 6 EI_NB_TO_CPU_SR_N<1>

28 14 6 EI_QACK_L
29 14 8 6 CHKSTOP_L
30 29 27 CPU_HTBEN
6 TP_PSYNCOUT
30 14 6 CPU_HRESET_L
30 25 CPU_SRESET_L
30 PROC_THERM_INT_L
30 PROCID0
30 PROCID1
30 PROCID2
30 28 14 6 EI_SE
14 6 TP_PROC_TRIGGER_OUT
6 TP_AFN
30 AVPRESET_L
30 BIMODE_L
30 C1UNDGLOBAL
30 C2UNDGLOBAL
30 DI2_L
30 LSSDMODE
30 LSSDSCANENABLE
30 LSSDSTOPC2ENABLE
30 LSSDSTOPC2STARENABLE
30 LSSDSTOPENABLE
29 14 6 MCP_L
6 TP_PSRO1
6 TP_PSRO2
30 PULSESEL0
30 PULSESEL1
30 PULSESEL2
30 RAMSTOPENABLE
30 14 6 RI_L
30 14 6 SYNCENABLE

EI_CLKI EI_CLKI*

EI_AD10 EI_AD11 EI_AD12 EI_AD13 EI_AD14 EI_AD15 EI_AD16 EI_AD17 EI_AD18 EI_AD19 EI_AD110 EI_AD111 EI_AD112 EI_AD113 EI_AD114 EI_AD115 EI_AD116 EI_AD117 EI_AD118 EI_AD119 EI_AD120 EI_AD121 EI_AD122 EI_AD123 EI_AD124 EI_AD125 EI_AD126 EI_AD127 EI_AD128 EI_AD129 EI_AD130 EI_AD131 EI_AD132 EI_AD133 EI_AD134 EI_AD135 EI_AD136 EI_AD137 EI_AD138 EI_AD139 EI_AD140 EI_AD141 EI_AD142 EI_AD143

EI_SR10 EI_SR10* EI_SR11 EI_SR11*

QACK*
CHKSTOP*
TBEN
APSYNCOUT
HRESET*
SRESET*
THERM_INT*
PROCID0
PROCID1
PROCID2
TRIGGER_IN
TRIGGER_OUT
AVPRESET*
BIMODE*
C1UNDGLOBAL
C2UNDGLOBAL
DI2*
LSSDMODE
LSSDSCANENABLE
LSSDSTOPC2ENABLE
LSSDSTOPC2STARENABLE
LSSDSTOPENABLE
MCP*
PSRO1
PSRO2
PULSESEL0
PULSESEL1
PULSESEL2
RAMSTOPENABLE
RI*
SYNCENABLE*

EI_CLKO EI_CLKO*

EI_AD00 EI_AD01 EI_AD02 EI_AD03 EI_AD04 EI_AD05 EI_AD06 EI_AD07 EI_AD08 EI_AD09 EI_AD010 EI_AD011 EI_AD012 EI_AD013 EI_AD014 EI_AD015 EI_AD016 EI_AD017 EI_AD018 EI_AD019 EI_AD020 EI_AD021 EI_AD022 EI_AD023 EI_AD024 EI_AD025 EI_AD026 EI_AD027 EI_AD028 EI_AD029 EI_AD030 EI_AD031 EI_AD032 EI_AD033 EI_AD034 EI_AD035 EI_AD036 EI_AD037 EI_AD038 EI_AD039 EI_AD040 EI_AD041 EI_AD042 EI_AD043

EI_SR00 EI_SR00* EI_SR01 EI_SR01*

QREQ*
INT*
APSYNCIN
IIC_SCL IIC_SDA
I2CGO
CKTERMDIS
EI_DISABLE
BUSCFG0 BUSCFG1 BUSCFG2
ATTENTION GPUL_DBG JTAGMODE
TCK TDI TDO TMS TRST*
BYPASS* PLLLOCK
PLLMULT PLLRANGE0 PLLRANGE1 PLLTEST PLLTESTOUT
SPARE

EI_CPU_TO_NB_CLK_P 6 14 28
EI_CPU_TO_NB_CLK_N 6 14 28

EI_CPU_TO_NB_AD<0> 6 14 28
EI_CPU_TO_NB_AD<1> 6 14 28
EI_CPU_TO_NB_AD<2> 6 14 28
EI_CPU_TO_NB_AD<3> 6 14 28
EI_CPU_TO_NB_AD<4> 6 14 28
EI_CPU_TO_NB_AD<5> 6 14 28
EI_CPU_TO_NB_AD<6> 6 14 28
EI_CPU_TO_NB_AD<7> 6 14 28
EI_CPU_TO_NB_AD<8> 6 14 28
EI_CPU_TO_NB_AD<9> 6 14 28
EI_CPU_TO_NB_AD<10> 6 14 28
EI_CPU_TO_NB_AD<11> 6 14 28
EI_CPU_TO_NB_AD<12> 6 14 28
EI_CPU_TO_NB_AD<13> 6 14 28
EI_CPU_TO_NB_AD<14> 6 14 28
EI_CPU_TO_NB_AD<15> 6 14 28
EI_CPU_TO_NB_AD<16> 6 14 28
EI_CPU_TO_NB_AD<17> 6 14 28
EI_CPU_TO_NB_AD<18> 6 14 28
EI_CPU_TO_NB_AD<19> 6 14 28
EI_CPU_TO_NB_AD<20> 6 14 28
EI_CPU_TO_NB_AD<21> 6 14 28
EI_CPU_TO_NB_AD<22> 6 14 28
EI_CPU_TO_NB_AD<23> 6 14 28
EI_CPU_TO_NB_AD<24> 6 14 28
EI_CPU_TO_NB_AD<25> 6 14 28
EI_CPU_TO_NB_AD<26> 6 14 28
EI_CPU_TO_NB_AD<27> 6 14 28
EI_CPU_TO_NB_AD<28> 6 14 28
EI_CPU_TO_NB_AD<29> 6 14 28
EI_CPU_TO_NB_AD<30> 6 14 28
EI_CPU_TO_NB_AD<31> 6 14 28
EI_CPU_TO_NB_AD<32> 6 14 28
EI_CPU_TO_NB_AD<33> 6 14 28
EI_CPU_TO_NB_AD<34> 6 14 28
EI_CPU_TO_NB_AD<35> 6 14 28
EI_CPU_TO_NB_AD<36> 6 14 28
EI_CPU_TO_NB_AD<37> 6 14 28
EI_CPU_TO_NB_AD<38> 6 14 28
EI_CPU_TO_NB_AD<39> 6 14 28
EI_CPU_TO_NB_AD<40> 6 14 28
EI_CPU_TO_NB_AD<41> 6 14 28
EI_CPU_TO_NB_AD<42> 6 14 28
EI_CPU_TO_NB_AD<43> 6 14 28

EI_CPU_TO_NB_SR_P<0> 6 14 28
EI_CPU_TO_NB_SR_N<0> 6 14 28
EI_CPU_TO_NB_SR_P<1> 6 14 28
EI_CPU_TO_NB_SR_N<1> 6 14 28

EI_QREQ_L 6 14 28 30
CPU_INT_L 6 14 25 30

MATCH TO SYSCLK

CPU_APSYNC 30
I2C_CPU_A_SCL 18
I2C_CPU_A_SDA 18
I2CGO 30
CKTERMDIS_L 30
EI_DISABLE 30
BUSCFG0 30
BUSCFG1 30
BUSCFG2 30
TP_ATTENTION 6
GPUL_DBG 30
JTAGMODE_SPARE2 30
JTAG_CPU_TCK 18 30
JTAG_CPU_TDI 18 30
JTAG_CPU_TDO 18 30
JTAG_CPU_TMS 18 30
JTAG_CPU_TRST_L 18 30
CPU_BYPASS_L 30
PLLLOCK 8
PLLMULT 30
PLLRANGE0 30
PLLRANGE1 30
PLLTEST 30
PLLTESTOUT 30
CPU_SPARE 30

R2910 0 5% 1/16W MF-LF 402 — EI_CPU_SYNC 27

NOSTUFF R2911 0 5% 1/16W MF-LF 402 — EI_SYNC_FROM_NB 28

PROCESSOR IIC ADDRESS:
80,84

MORE PROCESSOR DECOUPLING ON PAGES 31 & 32

36 32 31 7 =PPVCORE_CPU

C2953 C2947 C2945 C2939 C2937 C2928 C2924 C2920 C2914 C2912
C2954 C2948 C2946 C2940 C2938 C2929 C2925 C2921 C2915 C2913
C2955 C2951 C2949 C2943 C2941 C2930 C2926 C2922 C2918 C2916
C2956 C2952 C2950 C2944 C2942 C2931 C2927 C2923 C2919 C2917
C2900 C2960 C2959 C2958 C2957 C2936 C2935 C2934 C2933 C2932
C2911 C2910 C2909 C2908 C2907 C2906 C2905 C2904 C2903 C2902

1UF 10% 6.3V CERM 402

NOSTUFF R2905 49.9 1% 1/10W MF-LF 402 — 30 29 27 CPU_HTBEN

PLACE BY PROCESSOR PIN.

35 31 30 29 18 14 7 =PP1V2_EI_CPU

R2906 1K 5% 1/16W MF-LF 402

R2908 1K 5% 1/16W MF-LF 402

R2902 0 5% 1/16W MF-LF 402 — 28 CPU_CHKSTOP_L

CHKSTOP_L 6 8 14 29

NOSTUFF R2904 0 5% 1/16W MF-LF 402

MCP_L 6 14 29

PROCESSOR LOGIC I/O

MASTER: GILA
LAST MODIFIED: APR 09, 04

NEO APPLE PI

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

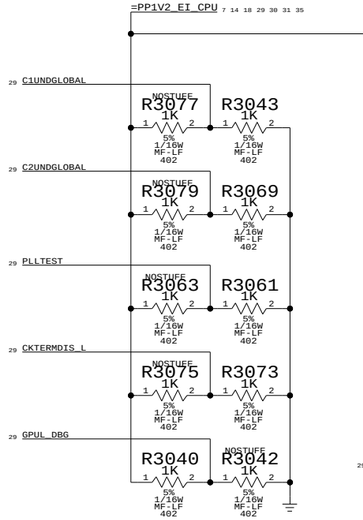
II NOT TO REPRODUCE OR COPY IT

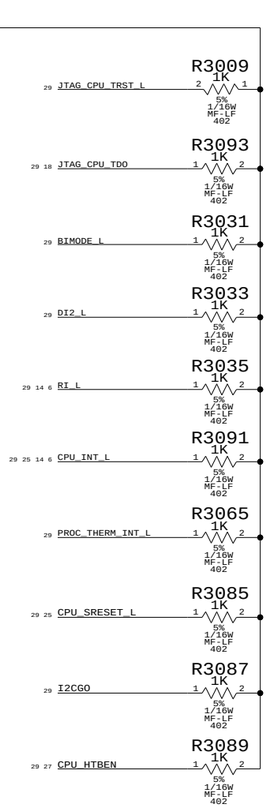
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

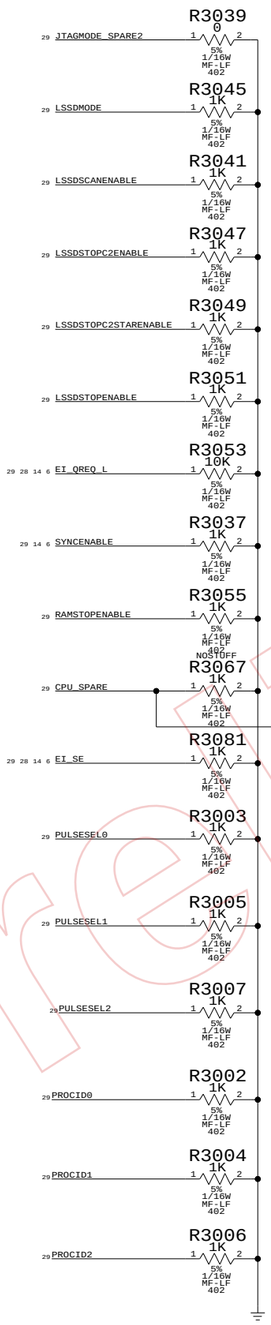
APPLE COMPUTER INC.

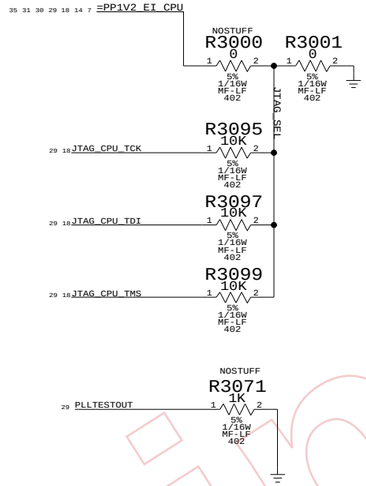
SIZE	DRAWING NUMBER	REV.
D	051-6772	04

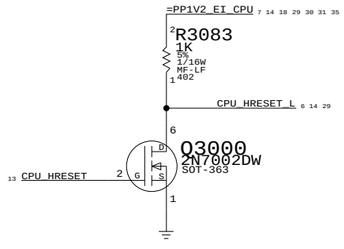
SCALE	SHT	OF
NONE	29	102

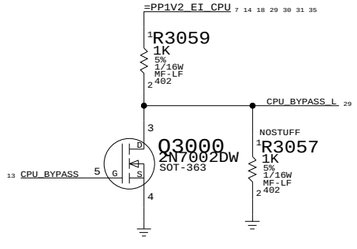


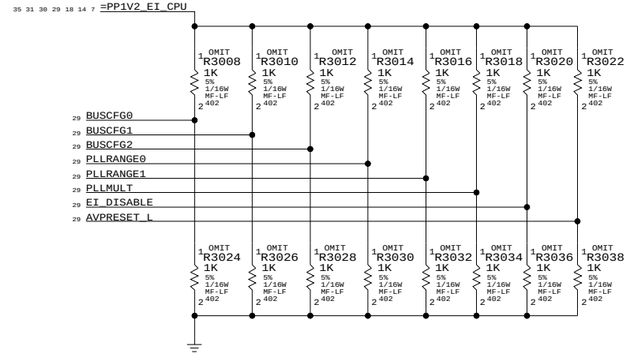












SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	>= 1.8 GHZ *
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	<= 1.6 GHZ *
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION

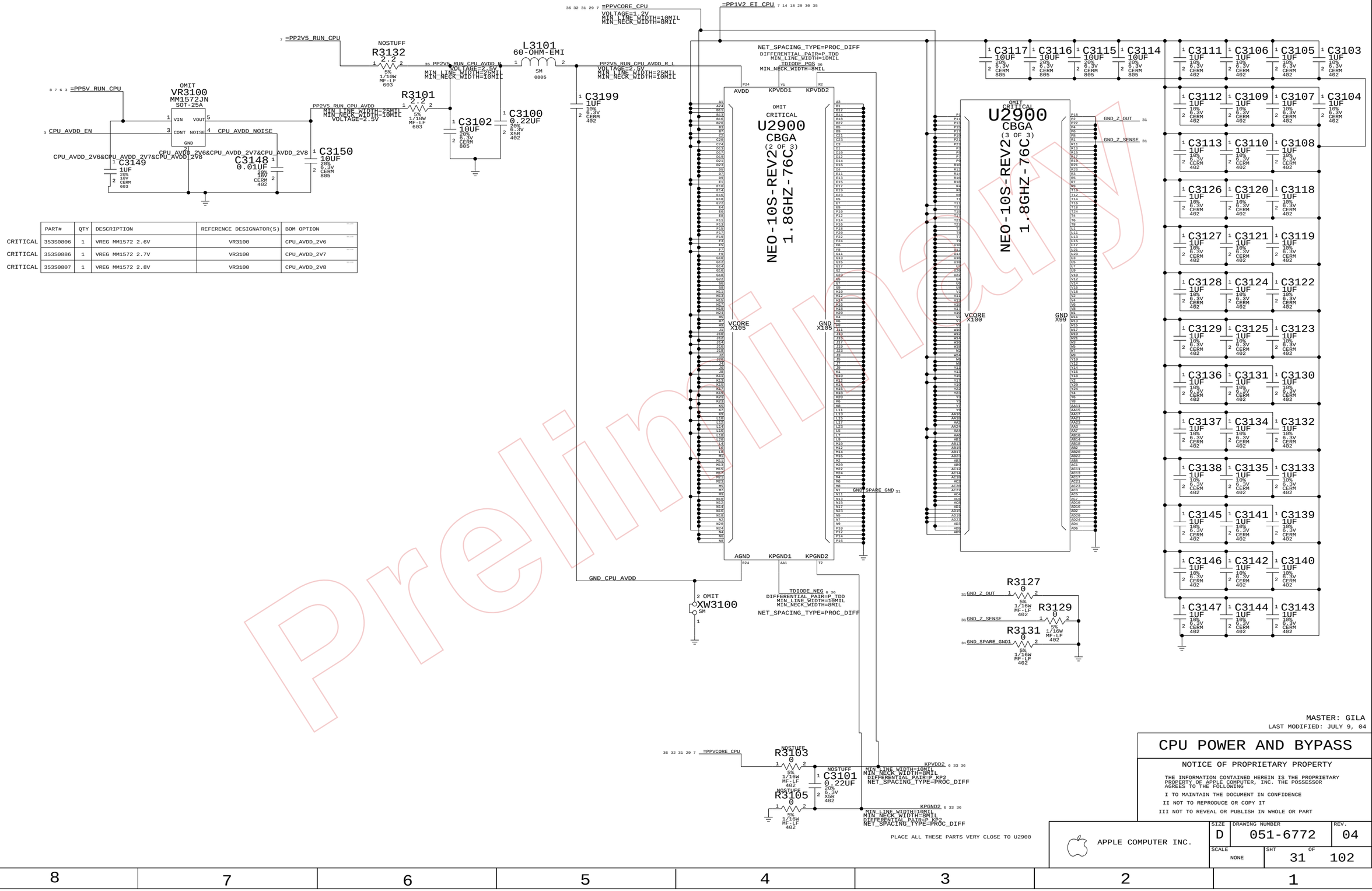
MASTER: GILA
LAST MODIFIED: APR 27, 04

CPU STRAPS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 04

SCALE NONE | SHT 30 OF 102



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0886	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL	353S0807	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

MASTER: GILA
LAST MODIFIED: JULY 9, 04

CPU POWER AND BYPASS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT	OF
NONE	31	102

36 31 29 7 =PPVCORE_CPU

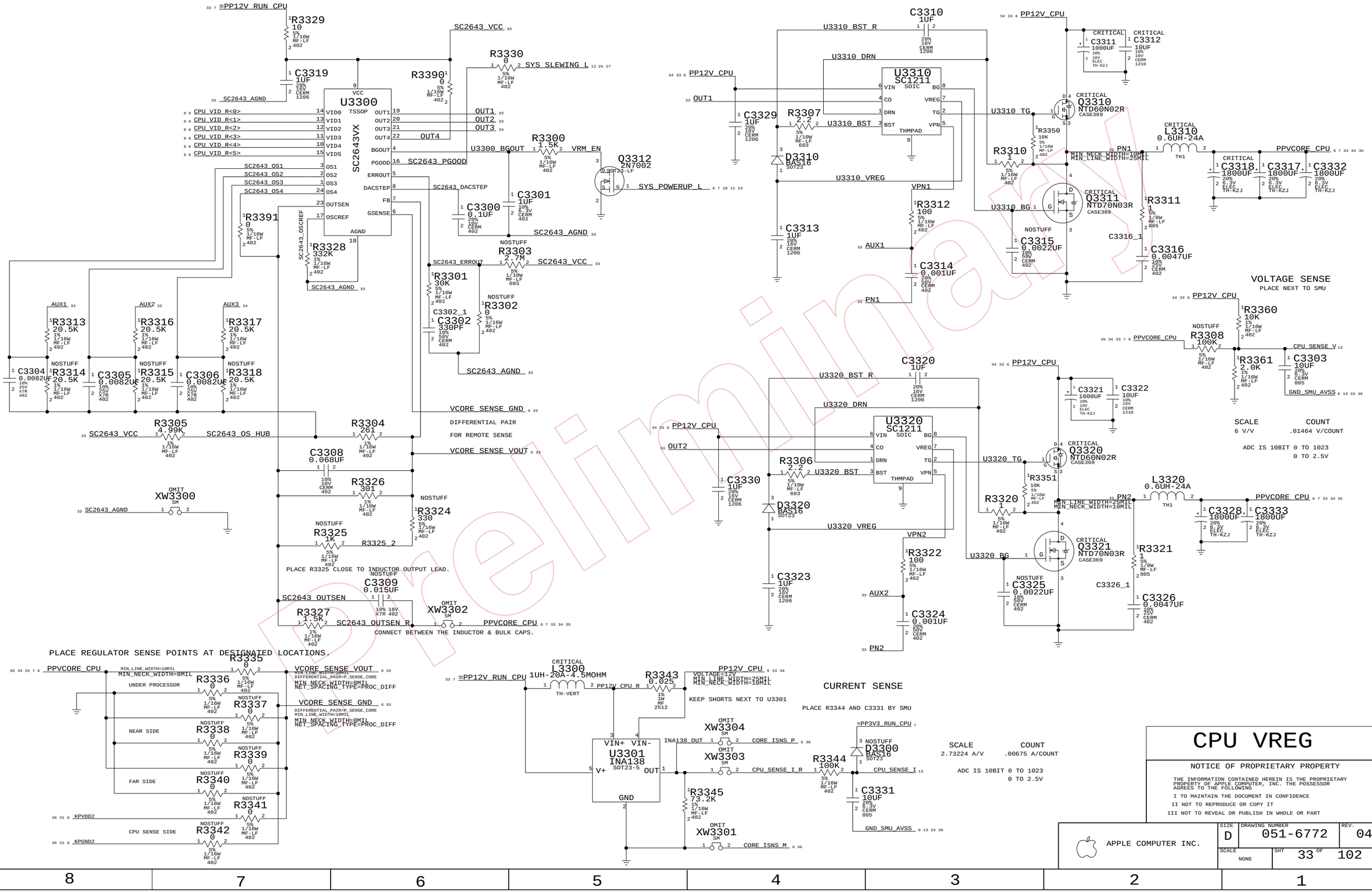
C3222 1UF 10% 6.3V CERM 402	C3221 1UF 10% 6.3V CERM 402	C3220 1UF 10% 6.3V CERM 402	C3219 1UF 10% 6.3V CERM 402	C3218 1UF 10% 6.3V CERM 402	C3217 1UF 10% 6.3V CERM 402	C3216 1UF 10% 6.3V CERM 402	C3215 1UF 10% 6.3V CERM 402	C3212 1UF 10% 6.3V CERM 402	C3200 1UF 10% 6.3V CERM 402
C3293 1UF 10% 6.3V CERM 402	C3268 1UF 10% 6.3V CERM 402	C3261 1UF 10% 6.3V CERM 402	C3259 1UF 10% 6.3V CERM 402	C3235 1UF 10% 6.3V CERM 402	C3232 1UF 10% 6.3V CERM 402	C3226 1UF 10% 6.3V CERM 402	C3224 1UF 10% 6.3V CERM 402	C3245 1UF 10% 6.3V CERM 402	C3223 1UF 10% 6.3V CERM 402
C3294 1UF 10% 6.3V CERM 402	C3269 1UF 10% 6.3V CERM 402	C3264 1UF 10% 6.3V CERM 402	C3260 1UF 10% 6.3V CERM 402	C3236 1UF 10% 6.3V CERM 402	C3233 1UF 10% 6.3V CERM 402	C3227 1UF 10% 6.3V CERM 402	C3225 1UF 10% 6.3V CERM 402	C3256 1UF 10% 6.3V CERM 402	C3234 1UF 10% 6.3V CERM 402
C3295 1UF 10% 6.3V CERM 402	C3271 1UF 10% 6.3V CERM 402	C3265 1UF 10% 6.3V CERM 402	C3262 1UF 10% 6.3V CERM 402	C3239 1UF 10% 6.3V CERM 402	C3237 1UF 10% 6.3V CERM 402	C3230 1UF 10% 6.3V CERM 402	C3228 1UF 10% 6.3V CERM 402	C3289 1UF 10% 6.3V CERM 402	C3267 1UF 10% 6.3V CERM 402
C3296 1UF 10% 6.3V CERM 402	C3270 1UF 10% 6.3V CERM 402	C3266 1UF 10% 6.3V CERM 402	C3263 1UF 10% 6.3V CERM 402	C3240 1UF 10% 6.3V CERM 402	C3238 1UF 10% 6.3V CERM 402	C3231 1UF 10% 6.3V CERM 402	C3229 1UF 10% 6.3V CERM 402	C3201 1UF 10% 6.3V CERM 402	C3278 1UF 10% 6.3V CERM 402
C3297 1UF 10% 6.3V CERM 402	C3282 1UF 10% 6.3V CERM 402	C3276 1UF 10% 6.3V CERM 402	C3272 1UF 10% 6.3V CERM 402	C3252 1UF 10% 6.3V CERM 402	C3250 1UF 10% 6.3V CERM 402	C3243 1UF 10% 6.3V CERM 402	C3241 1UF 10% 6.3V CERM 402	C3206 1UF 10% 6.3V CERM 402	C3204 1UF 10% 6.3V CERM 402
C3298 1UF 10% 6.3V CERM 402	C3281 1UF 10% 6.3V CERM 402	C3277 1UF 10% 6.3V CERM 402	C3273 1UF 10% 6.3V CERM 402	C3253 1UF 10% 6.3V CERM 402	C3251 1UF 10% 6.3V CERM 402	C3244 1UF 10% 6.3V CERM 402	C3242 1UF 10% 6.3V CERM 402	C3207 1UF 10% 6.3V CERM 402	C3205 1UF 10% 6.3V CERM 402
C3299 1UF 10% 6.3V CERM 402	C3284 1UF 10% 6.3V CERM 402	C3279 1UF 10% 6.3V CERM 402	C3274 1UF 10% 6.3V CERM 402	C3257 1UF 10% 6.3V CERM 402	C3254 1UF 10% 6.3V CERM 402	C3248 1UF 10% 6.3V CERM 402	C3246 1UF 10% 6.3V CERM 402	C3210 1UF 10% 6.3V CERM 402	C3208 1UF 10% 6.3V CERM 402
C3202 1UF 10% 6.3V CERM 402	C3283 1UF 10% 6.3V CERM 402	C3280 1UF 10% 6.3V CERM 402	C3275 1UF 10% 6.3V CERM 402	C3258 1UF 10% 6.3V CERM 402	C3255 1UF 10% 6.3V CERM 402	C3249 1UF 10% 6.3V CERM 402	C3247 1UF 10% 6.3V CERM 402	C3211 1UF 10% 6.3V CERM 402	C3209 1UF 10% 6.3V CERM 402
C3203 1UF 10% 6.3V CERM 402	C3292 1UF 10% 6.3V CERM 402	C3291 1UF 10% 6.3V CERM 402	C3290 1UF 10% 6.3V CERM 402	C3288 1UF 10% 6.3V CERM 402	C3287 1UF 10% 6.3V CERM 402	C3286 1UF 10% 6.3V CERM 402	C3285 1UF 10% 6.3V CERM 402	C3214 1UF 10% 6.3V CERM 402	C3213 1UF 10% 6.3V CERM 402

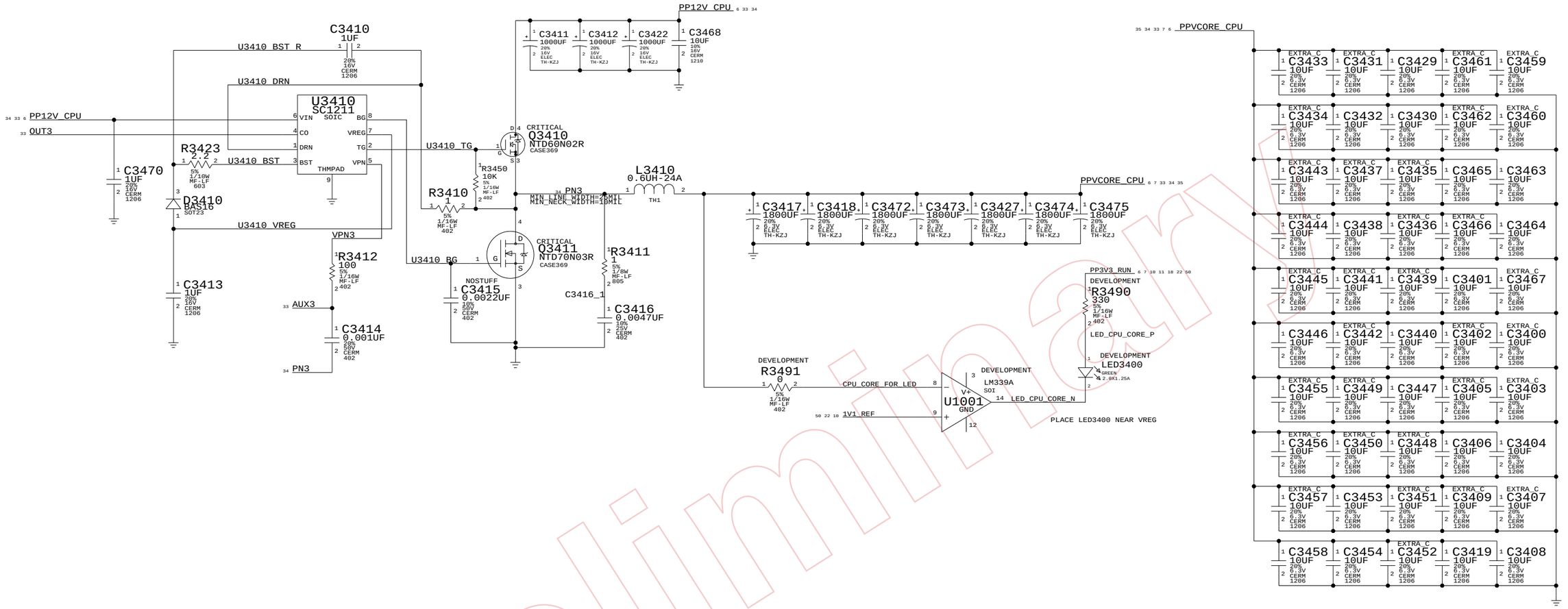
MASTER: GILA
LAST MODIFIED: APR 09, 04

PROC DECOUPLING

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 32 OF 102	


=PP12V_RUN_CPU
R3329 10
C3319 1UF
SC2643_AGND
SC2643_VCC
R3330 0
SYS_SLEWING_L
R3390 0
U3300
SC2643VX
VCC
TSSOP
CPU_VID_R<0>
CPU_VID_R<1>
CPU_VID_R<2>
CPU_VID_R<3>
CPU_VID_R<4>
CPU_VID_R<5>
VID0
VID1
VID2
VID3
VID4
VID5
OUT1
OUT2
OUT3
OUT4
BGOUT
PGOOD
ERROUT
DACSTEP
FB
GSENSE
OUTSEN
OSCREF
AGND
SC2643_OS1
SC2643_OS2
SC2643_OS3
SC2643_OS4
SC2643_OSCREF
R3328 332K
R3391 0
R3300 1.5K
U3300_BGOUT
VRM_EN
SC2643_PGOOD
Q3312 2N7002
SOT23-LF
SYS_POWERUP_L
C3300 0.1UF
C3301 1UF
R3303 2.7M
SC2643_ERROUT
R3301 30K
R3302 0
NOSTUFF
C3302_1
C3302 330PF
VCORE_SENSE_GND
DIFFERENTIAL PAIR
FOR REMOTE SENSE
VCORE_SENSE_VOUT
AUX1
AUX2
AUX3
R3313 20.5K
R3316 20.5K
R3317 20.5K
C3304 0.0082UF
R3314 20.5K
C3305 0.0082UF
R3315 20.5K
C3306 0.0082UF
R3318 20.5K
R3305 4.99K
R3304 261
C3308 0.068UF
R3326 301
R3324 330
R3325 1K
R3325_2
PLACE R3325 CLOSE TO INDUCTOR OUTPUT LEAD.
C3309 0.015UF
SC2643_OUTSEN
R3327 1.5K
SC2643_OUTSEN_R
OMIT
XW3300
XW3302
PPVCORE_CPU
CONNECT BETWEEN THE INDUCTOR & BULK CAPS.
C3310 1UF
U3310_BST_R
U3310_DRN
U3310 SC1211
SOIC
VIN
CO
DRN
BST
BG
VREG
TG
VPN
THMPAD
PP12V_CPU
OUT1
C3329 1UF
R3307 2.2
U3310_BST
D3310 BAS16
SOT23
U3310_VREG
C3313 1UF
U3310_TG
U3310_BG
Q3310 NTD60N02R
CASE369
Q3311 NTD70N03R
R3350 10K
R3310 1
R3312 100
VPN1
AUX1
C3314 0.001UF
PN1
C3315 0.0022UF
NOSTUFF
R3311 1
C3316_1
C3316 0.0047UF
CRITICAL
C3311 1000UF
C3312 10UF
L3310 0.6UH-24A
TH1
MIN_NECK_WIDTH=10MIL
MIN_LINE_WIDTH=25MIL
C3318 1800UF
C3317 1800UF
C3332 1800UF
PPVCORE_CPU
VOLTAGE SENSE
PLACE NEXT TO SMU
R3360 10K
R3308 100K
R3361 2.0K
C3303 10UF
CPU_SENSE_V
GND_SMU_AVSS
SCALE
6 V/V
COUNT
.01464 V/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
U3320_BST_R
U3320_DRN
U3320 SC1211
U3320_TG
U3320_BG
Q3320 NTD60N02R
Q3321 NTD70N03R
R3351 10K
R3320 1
R3322 100
C3324 0.001UF
C3323 1UF
C3321 1000UF
C3322 10UF
L3320 0.6UH-24A
C3328 1800UF
C3333 1800UF
R3321 1
C3325 0.0022UF
C3326_1
C3326 0.0047UF
OUT2
R3306 2.2
D3320 BAS16
C3330 1UF
C3320 1UF
PLACE REGULATOR SENSE POINTS AT DESIGNATED LOCATIONS.
PPVCORE_CPU
MIN_NECK_WIDTH=8MIL
UNDER PROCESSOR
NEAR SIDE
FAR SIDE
CPU SENSE SIDE
R3335 0
R3336 0
R3337 0
R3338 0
R3339 0
R3340 0
R3341 0
R3342 0
KPVDD2
KPGND2
VCORE_SENSE_VOUT
VCORE_SENSE_GND
DIFFERENTIAL_PAIR=P_SENSE_CORE
MIN_NECK_WIDTH=8MIL
NET_SPACING_TYPE=PROC_DIFF
CURRENT SENSE
PLACE R3344 AND C3331 BY SMU
L3300 1UH-20A-4.5MOHM
TH-VERT
R3343 0.025
PP12V_CPU_R
KEEP SHORTS NEXT TO U3301
U3301 INA138
SOT23-5
VIN+
VIN-
V+
OUT
GND
INA138_OUT
CORE_ISNS_P
CORE_ISNS_M
CPU_SENSE_I_R
CPU_SENSE_I
R3345 73.2K
R3344 100K
D3300 BAS16
C3331 10UF
=PP3V3_RUN_CPU
SCALE
2.73224 A/V
COUNT
.00675 A/COUNT
ADC IS 10BIT 0 TO 1023
0 TO 2.5V
CPU VREG
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6772
REV. 04
SCALE NONE
SHT 33 OF 102



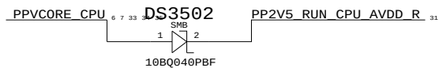
CPU VREG

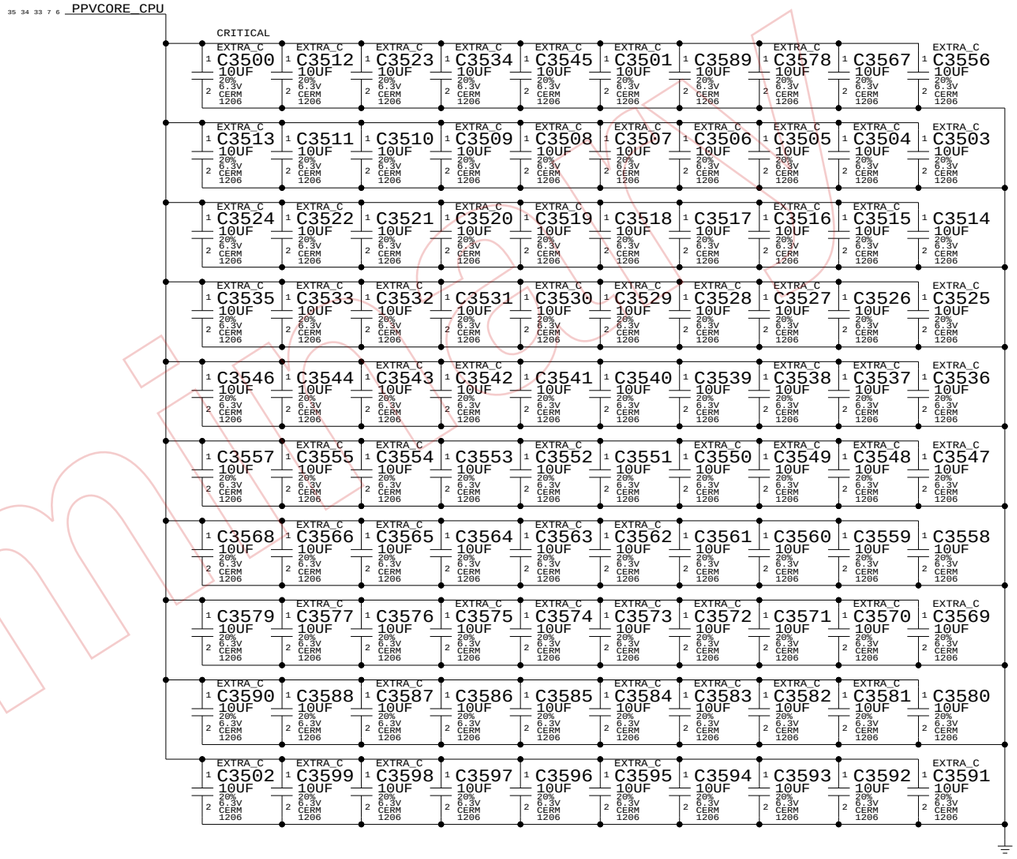
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE NONE

SHT 34 OF 102

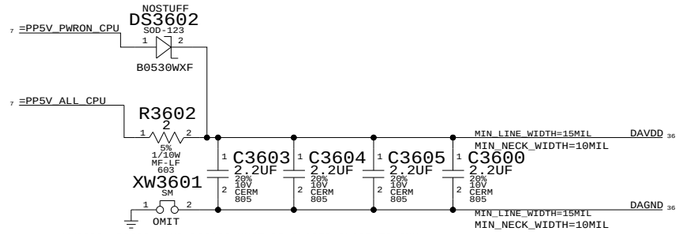


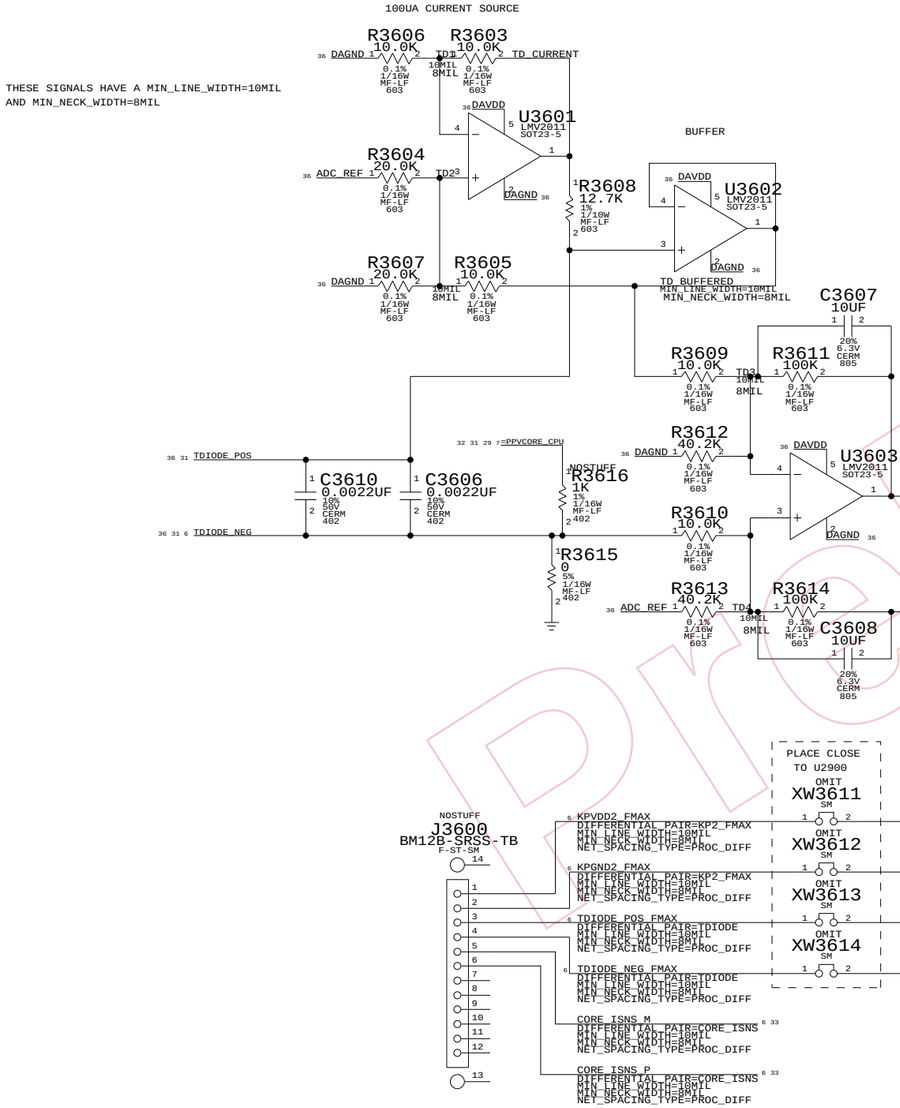


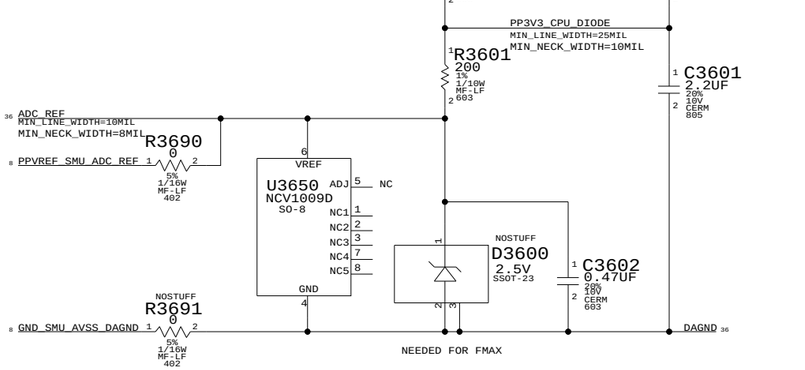
CPU VREG OUTPUT CAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 35 OF 102	







CPU DIODE CONDITIONER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 36 OF 102	

U3TWINS DO NOT HAVE MASKS

=PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT — MEMORY DATA INTERFACE

RAM_DQ_R<0>	AF20	DDR_DQ0	DDR_DQ64 AG27 RAM_DQ_R<64>
RAM_DQ_R<1>	AH22	DDR_DQ1	DDR_DQ65 AF24 RAM_DQ_R<65>
RAM_DQ_R<2>	AH21	DDR_DQ2	DDR_DQ66 AE24 RAM_DQ_R<66>
RAM_DQ_R<3>	AG21	DDR_DQ3	DDR_DQ67 AG26 RAM_DQ_R<67>
RAM_DQ_R<4>	AB20	DDR_DQ4	DDR_DQ68 AF26 RAM_DQ_R<68>
RAM_DQ_R<5>	AC21	DDR_DQ5	DDR_DQ69 AD24 RAM_DQ_R<69>
RAM_DQ_R<6>	AD23	DDR_DQ6	DDR_DQ70 AD25 RAM_DQ_R<70>
RAM_DQ_R<7>	AD21	DDR_DQ7	DDR_DQ71 AG28 RAM_DQ_R<71>
RAM_DQ_R<8>	AH26	DDR_DQ8	DDR_DQ72 AF28 RAM_DQ_R<72>
RAM_DQ_R<9>	AH25	DDR_DQ9	DDR_DQ73 AE28 RAM_DQ_R<73>
RAM_DQ_R<10>	AH24	DDR_DQ10	DDR_DQ74 AD26 RAM_DQ_R<74>
RAM_DQ_R<11>	AH23	DDR_DQ11	DDR_DQ75 AF27 RAM_DQ_R<75>
RAM_DQ_R<12>	AH27	DDR_DQ12	DDR_DQ76 AC26 RAM_DQ_R<76>
RAM_DQ_R<13>	AG24	DDR_DQ13	DDR_DQ77 AC25 RAM_DQ_R<77>
RAM_DQ_R<14>	AF23	DDR_DQ14	DDR_DQ78 AC27 RAM_DQ_R<78>
RAM_DQ_R<15>	AH28	DDR_DQ15	DDR_DQ79 AD27 RAM_DQ_R<79>
RAM_DQ_R<16>	U25	DDR_DQ16	DDR_DQ80 AA27 RAM_DQ_R<80>
RAM_DQ_R<17>	AA23	DDR_DQ17	DDR_DQ81 AA26 RAM_DQ_R<81>
RAM_DQ_R<18>	Y22	DDR_DQ18	DDR_DQ82 AA24 RAM_DQ_R<82>
RAM_DQ_R<19>	AA22	DDR_DQ19	DDR_DQ83 AA28 RAM_DQ_R<83>
RAM_DQ_R<20>	U24	DDR_DQ20	DDR_DQ84 Y26 RAM_DQ_R<84>
RAM_DQ_R<21>	V23	DDR_DQ21	DDR_DQ85 Y25 RAM_DQ_R<85>
RAM_DQ_R<22>	V22	DDR_DQ22	DDR_DQ86 Y28 RAM_DQ_R<86>
RAM_DQ_R<23>	U22	DDR_DQ23	DDR_DQ87 Y24 RAM_DQ_R<87>
RAM_DQ_R<24>	P25	DDR_DQ24	DDR_DQ88 V26 RAM_DQ_R<88>
RAM_DQ_R<25>	R22	DDR_DQ25	DDR_DQ89 V27 RAM_DQ_R<89>
RAM_DQ_R<26>	R21	DDR_DQ26	DDR_DQ90 V24 RAM_DQ_R<90>
RAM_DQ_R<27>	U23	DDR_DQ27	DDR_DQ91 W28 RAM_DQ_R<91>
RAM_DQ_R<28>	P26	DDR_DQ28	DDR_DQ92 U27 RAM_DQ_R<92>
RAM_DQ_R<29>	R24	DDR_DQ29	DDR_DQ93 V28 RAM_DQ_R<93>
RAM_DQ_R<30>	P24	DDR_DQ30	DDR_DQ94 T28 RAM_DQ_R<94>
RAM_DQ_R<31>	P23	DDR_DQ31	DDR_DQ95 U26 RAM_DQ_R<95>
RAM_DQ_R<32>	M25	DDR_DQ32	DDR_DQ96 R27 RAM_DQ_R<96>
RAM_DQ_R<33>	M23	DDR_DQ33	DDR_DQ97 R26 RAM_DQ_R<97>
RAM_DQ_R<34>	P21	DDR_DQ34	DDR_DQ98 R28 RAM_DQ_R<98>
RAM_DQ_R<35>	P22	DDR_DQ35	DDR_DQ99 P27 RAM_DQ_R<99>
RAM_DQ_R<36>	M24	DDR_DQ36	DDR_DQ100 M28 RAM_DQ_R<100>
RAM_DQ_R<37>	L22	DDR_DQ37	DDR_DQ101 N28 RAM_DQ_R<101>
RAM_DQ_R<38>	L23	DDR_DQ38	DDR_DQ102 L28 RAM_DQ_R<102>
RAM_DQ_R<39>	J23	DDR_DQ39	DDR_DQ103 P28 RAM_DQ_R<103>
RAM_DQ_R<40>	D23	DDR_DQ40	DDR_DQ104 L25 RAM_DQ_R<104>
RAM_DQ_R<41>	D24	DDR_DQ41	DDR_DQ105 L26 RAM_DQ_R<105>
RAM_DQ_R<42>	C26	DDR_DQ42	DDR_DQ106 L27 RAM_DQ_R<106>
RAM_DQ_R<43>	C27	DDR_DQ43	DDR_DQ107 K28 RAM_DQ_R<107>
RAM_DQ_R<44>	A22	DDR_DQ44	DDR_DQ108 H27 RAM_DQ_R<108>
RAM_DQ_R<45>	A25	DDR_DQ45	DDR_DQ109 H28 RAM_DQ_R<109>
RAM_DQ_R<46>	C24	DDR_DQ46	DDR_DQ110 J27 RAM_DQ_R<110>
RAM_DQ_R<47>	C23	DDR_DQ47	DDR_DQ111 L24 RAM_DQ_R<111>
RAM_DQ_R<48>	B24	DDR_DQ48	DDR_DQ112 J25 RAM_DQ_R<112>
RAM_DQ_R<49>	B23	DDR_DQ49	DDR_DQ113 J24 RAM_DQ_R<113>
RAM_DQ_R<50>	A23	DDR_DQ50	DDR_DQ114 J26 RAM_DQ_R<114>
RAM_DQ_R<51>	A24	DDR_DQ51	DDR_DQ115 G28 RAM_DQ_R<115>
RAM_DQ_R<52>	A27	DDR_DQ52	DDR_DQ116 H25 RAM_DQ_R<116>
RAM_DQ_R<53>	A28	DDR_DQ53	DDR_DQ117 H24 RAM_DQ_R<117>
RAM_DQ_R<54>	B28	DDR_DQ54	DDR_DQ118 F27 RAM_DQ_R<118>
RAM_DQ_R<55>	A26	DDR_DQ55	DDR_DQ119 H26 RAM_DQ_R<119>
RAM_DQ_R<56>	F24	DDR_DQ56	DDR_DQ120 E28 RAM_DQ_R<120>
RAM_DQ_R<57>	J22	DDR_DQ57	DDR_DQ121 E27 RAM_DQ_R<121>
RAM_DQ_R<58>	E23	DDR_DQ58	DDR_DQ122 F26 RAM_DQ_R<122>
RAM_DQ_R<59>	H23	DDR_DQ59	DDR_DQ123 E26 RAM_DQ_R<123>
RAM_DQ_R<60>	J21	DDR_DQ60	DDR_DQ124 D28 RAM_DQ_R<124>
RAM_DQ_R<61>	H21	DDR_DQ61	DDR_DQ125 C28 RAM_DQ_R<125>
RAM_DQ_R<62>	G21	DDR_DQ62	DDR_DQ126 E25 RAM_DQ_R<126>
RAM_DQ_R<63>	H22	DDR_DQ63	DDR_DQ127 E24 RAM_DQ_R<127>

=PP1V5_PWRON_NB_AVDD — R3702 2.2 5% 1/10W MF-LF 603 — PP1V5_PWRON_RAM_NB_AVDD (VOLTAGE=1.5V) — C3745 1UF 10% 6.3V CERM 402 — C3744 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

=PP2V5_PWRON_RAM

DDR CLK_AVDD (AB21) — DDR_CLK_AVSS (AA20)

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT — MEMORY CONTROL INTERFACE

RAM_CLK66M_NB	AC20	DDR_CLKP	
RAM_CLK_A_P_R	AA12	DDR_CK_A	
RAM_CLK_A_N_R	AB12	DDR_CK_AN	
RAM_CLK_B_P_R	AB14	DDR_CK_B	
RAM_CLK_B_N_R	AA14	DDR_CK_BN	
RAM_CLK_C_P_R	AE15	DDR_CK_C	
RAM_CLK_C_N_R	AE14	DDR_CK_CN	
RAM_CLK_D_P_R	AC14	DDR_CK_D	
RAM_CLK_D_N_R	AD14	DDR_CK_DN	
RAM_CLK_E_P_R	AD15	DDR_CK_E	
RAM_CLK_E_N_R	AC15	DDR_CK_EN	
RAM_CLK_F_P_R	AA15	DDR_CK_F	
RAM_CLK_F_N_R	AB15	DDR_CK_FN	
RAM_CKE_R<0>	AC17	DDR_CKE0	
RAM_CKE_R<1>	AD17	DDR_CKE1	
RAM_CKE_R<2>	AE17	DDR_CKE2	
RAM_CKE_R<3>	AF17	DDR_CKE3	
RAM_CKE_R<4>	AB17	DDR_CKE4	
RAM_CKE_R<5>	AA17	DDR_CKE5	
RAM_CKE_R<6>	AB18	DDR_CKE6	
RAM_CKE_R<7>	AA18	DDR_CKE7	
	Y21	DDR_VREF0	
	U21	DDR_VREF1	
	L21	DDR_VREF2	
	H20	DDR_VREF3	
	AA21	DDR_VREF4	
	M21	DDR_VREF5	
	V21	DDR_VREF6	
	J20	DDR_VREF7	
	AE21	DDR_RAS	RAM_RAS_L_R
	AD20	DDR_CAS	RAM_CAS_L_R
	AC23	DDR_WE	RAM_WE_L_R
	AF21	DDR_BA0	RAM_BA_R<0>
	AE20	DDR_BA1	RAM_BA_R<1>
	AH16	DDR_MUXEN0	RAM_MUXEN0
	AH18	DDR_MUXEN4	RAM_MUXEN4
	AG12	DDR_MAD0	RAM_A_R<0>
	AH13	DDR_MAD1	RAM_A_R<1>
	AH14	DDR_MAD2	RAM_A_R<2>
	AH15	DDR_MAD3	RAM_A_R<3>
	AF12	DDR_MAD4	RAM_A_R<4>
	AE12	DDR_MAD5	RAM_A_R<5>
	AD12	DDR_MAD6	RAM_A_R<6>
	AC12	DDR_MAD7	RAM_A_R<7>
	AG15	DDR_MAD8	RAM_A_R<8>
	AF15	DDR_MAD9	RAM_A_R<9>
	AF14	DDR_MAD10	RAM_A_R<10>
	AG14	DDR_MAD11	RAM_A_R<11>
	AH17	DDR_MAD12	RAM_A_R<12>
	AG17	DDR_MAD13	RAM_A_R<13>
	AF18	DDR_CS0	RAM_CS_L_R<0>
	AE18	DDR_CS1	RAM_CS_L_R<1>
	AG20	DDR_CS2	RAM_CS_L_R<2>
	AH20	DDR_CS3	RAM_CS_L_R<3>
	AC18	DDR_CS8	RAM_CS_L_R<8>
	AD18	DDR_CS9	RAM_CS_L_R<9>
	AG18	DDR_CS10	RAM_CS_L_R<10>
	AH19	DDR_CS11	RAM_CS_L_R<11>
	AC24	DDR_DQSP0	RAM_DQS_R<0>
	AG23	DDR_DQSP1	RAM_DQS_R<1>
	Y23	DDR_DQSP2	RAM_DQS_R<2>
	R23	DDR_DQSP3	RAM_DQS_R<3>
	M22	DDR_DQSP4	RAM_DQS_R<4>
	B26	DDR_DQSP5	RAM_DQS_R<5>
	B27	DDR_DQSP6	RAM_DQS_R<6>
	F23	DDR_DQSP7	RAM_DQS_R<7>
	AE23	DDR_DQSP8	RAM_DQS_R<8>
	AD28	DDR_DQSP9	RAM_DQS_R<9>
	Y27	DDR_DQSP10	RAM_DQS_R<10>
	U28	DDR_DQSP11	RAM_DQS_R<11>
	M27	DDR_DQSP12	RAM_DQS_R<12>
	J28	DDR_DQSP13	RAM_DQS_R<13>
	F28	DDR_DQSP14	RAM_DQS_R<14>
	F25	DDR_DQSP15	RAM_DQS_R<15>

=PP2V5_PWRON_RAM — R3700 1K 1% 1/10W MF-LF 402 — R3701 1K 1% 1/10W MF-LF 402 — PP1V25_PWRON_RAM_VREF_NB (VOLTAGE=1.25V) — C3730 C3746 C3747 C3748 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

=PP2V5_PWRON_RAM — C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 0.1UF 20% 10V CERM 402

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 C3740 C3739 C3738 0.1UF 20% 10V CERM 402

MASTER: GILA
LAST MODIFIED: APR 12, 04

U3LITE MEMORY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE: NONE — SHT 37 OF 102

ALL R PACKS ARE 1/16W 5%

RAM_DQ_R<7>	RP3836	4	5	22	RAM_DQ<7>	38 40 44
RAM_DQ_R<2>	RP3836	1	8	22	RAM_DQ<2>	38 40 44
RAM_DQ_R<0>	RP3836	3	6	22	RAM_DQ<0>	38 40 44
RAM_DQ_R<3>	RP3836	2	7	22	RAM_DQ<3>	38 40 44
RAM_DQ_R<1>	RP3816	1	8	22	RAM_DQ<1>	38 40 44
RAM_DQ_R<4>	RP3816	2	7	22	RAM_DQ<4>	38 40 44
RAM_DQ_R<6>	RP3816	4	5	22	RAM_DQ<6>	38 40 44
RAM_DQ_R<5>	RP3816	3	6	22	RAM_DQ<5>	38 40 44
RAM_DQ_R<9>	RP3835	4	5	22	RAM_DQ<9>	38 40 44
RAM_DQ_R<10>	RP3801	1	8	22	RAM_DQ<10>	38 40 44
RAM_DQ_R<11>	RP3801	3	6	22	RAM_DQ<11>	38 40 44
RAM_DQ_R<14>	RP3801	4	5	22	RAM_DQ<14>	38 40 44
RAM_DQ_R<12>	RP3835	2	7	22	RAM_DQ<12>	38 40 44
RAM_DQ_R<13>	RP3801	2	7	22	RAM_DQ<13>	38 40 44
RAM_DQ_R<15>	RP3835	1	8	22	RAM_DQ<15>	38 40 44
RAM_DQ_R<8>	RP3835	3	6	22	RAM_DQ<8>	38 40 44
RAM_DQ_R<17>	RP3822	1	8	22	RAM_DQ<17>	38 40 44
RAM_DQ_R<22>	RP3822	4	5	22	RAM_DQ<22>	38 40 44
RAM_DQ_R<19>	RP3822	2	7	22	RAM_DQ<19>	38 40 44
RAM_DQ_R<18>	RP3822	3	6	22	RAM_DQ<18>	38 40 44
RAM_DQ_R<20>	RP3823	3	6	22	RAM_DQ<20>	38 40 44
RAM_DQ_R<16>	RP3823	4	5	22	RAM_DQ<16>	38 40 44
RAM_DQ_R<21>	RP3823	2	7	22	RAM_DQ<21>	38 40 44
RAM_DQ_R<23>	RP3823	1	8	22	RAM_DQ<23>	38 40 44
RAM_DQ_R<30>	RP3808	3	6	22	RAM_DQ<30>	38 40 44
RAM_DQ_R<26>	RP3824	2	7	22	RAM_DQ<26>	38 40 44
RAM_DQ_R<24>	RP3808	1	8	22	RAM_DQ<24>	38 40 44
RAM_DQ_R<27>	RP3824	1	8	22	RAM_DQ<27>	38 40 44
RAM_DQ_R<28>	RP3808	4	5	22	RAM_DQ<28>	38 40 44
RAM_DQ_R<31>	RP3808	2	7	22	RAM_DQ<31>	38 40 44
RAM_DQ_R<29>	RP3824	4	5	22	RAM_DQ<29>	38 40 44
RAM_DQ_R<25>	RP3824	3	6	22	RAM_DQ<25>	38 40 44
RAM_DQ_R<32>	RP3826	4	5	22	RAM_DQ<32>	38 40 44
RAM_DQ_R<35>	RP3807	2	7	22	RAM_DQ<35>	38 40 44
RAM_DQ_R<38>	RP3826	2	7	22	RAM_DQ<38>	38 40 44
RAM_DQ_R<37>	RP3807	4	5	22	RAM_DQ<37>	38 40 44
RAM_DQ_R<39>	RP3826	3	6	22	RAM_DQ<39>	38 40 44
RAM_DQ_R<33>	RP3807	3	6	22	RAM_DQ<33>	38 40 44
RAM_DQ_R<34>	RP3807	1	8	22	RAM_DQ<34>	38 40 44
RAM_DQ_R<36>	RP3826	1	8	22	RAM_DQ<36>	38 40 44
RAM_DQ_R<47>	RP3811	2	7	22	RAM_DQ<47>	38 40 44
RAM_DQ_R<46>	RP3811	1	8	22	RAM_DQ<46>	38 40 44
RAM_DQ_R<43>	RP3814	2	7	22	RAM_DQ<43>	38 40 44
RAM_DQ_R<41>	RP3814	1	8	22	RAM_DQ<41>	38 40 44
RAM_DQ_R<45>	RP3811	4	5	22	RAM_DQ<45>	38 40 44
RAM_DQ_R<42>	RP3814	3	6	22	RAM_DQ<42>	38 40 44
RAM_DQ_R<40>	RP3814	4	5	22	RAM_DQ<40>	38 40 44
RAM_DQ_R<44>	RP3811	3	6	22	RAM_DQ<44>	38 40 44
RAM_DQ_R<51>	RP3830	4	5	22	RAM_DQ<51>	38 40 44
RAM_DQ_R<50>	RP3830	2	7	22	RAM_DQ<50>	38 40 44
RAM_DQ_R<49>	RP3830	1	8	22	RAM_DQ<49>	38 40 44
RAM_DQ_R<48>	RP3830	3	6	22	RAM_DQ<48>	38 40 44
RAM_DQ_R<52>	RP3812	2	7	22	RAM_DQ<52>	38 40 44
RAM_DQ_R<53>	RP3812	3	6	22	RAM_DQ<53>	38 40 44
RAM_DQ_R<54>	RP3812	4	5	22	RAM_DQ<54>	38 40 44
RAM_DQ_R<55>	RP3812	1	8	22	RAM_DQ<55>	38 40 44
RAM_DQ_R<56>	RP3813	1	8	22	RAM_DQ<56>	38 40 44
RAM_DQ_R<63>	RP3831	4	5	22	RAM_DQ<63>	38 40 44
RAM_DQ_R<59>	RP3813	2	7	22	RAM_DQ<59>	38 40 44
RAM_DQ_R<61>	RP3831	2	7	22	RAM_DQ<61>	38 40 44
RAM_DQ_R<57>	RP3831	3	6	22	RAM_DQ<57>	38 40 44
RAM_DQ_R<60>	RP3831	1	8	22	RAM_DQ<60>	38 40 44
RAM_DQ_R<58>	RP3813	3	6	22	RAM_DQ<58>	38 40 44
RAM_DQ_R<62>	RP3813	4	5	22	RAM_DQ<62>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>	38 40 45
RAM_CKE_R<5>	RP3841	4	5	15	RAM_CKE<5>	38 40 45
RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>	38 40 44
RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>	38 40 44
RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>	38 40 45
RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>	38 40 45
RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>	38 40 44
RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>	38 40 44
RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>	38 40 44
RAM_A_R<10>	RP3832	2	7	15	RAM_A<10>	38 40 45
RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L	38 40 45
RAM_A_R<4>	RP3833	3	6	15	RAM_A<4>	38 40 44
RAM_A_R<6>	RP3833	2	7	15	RAM_A<6>	38 40 44
RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>	38 40 44
	RP3834	1	8	15		
RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>	38 40 44
RAM_A_R<2>	RP3834	2	7	15	RAM_A<2>	38 40 44
RAM_A_R<0>	RP3833	4	5	15	RAM_A<0>	38 40 44
RAM_A_R<5>	RP3832	1	8	15	RAM_A<5>	38 40 44
RAM_A_R<13>	RP3800	2	7	15	RAM_A<13>	38 40 44
RAM_A_R<3>	RP3800	1	8	15	RAM_A<3>	38 40 44
RAM_CAS_L_R	RP3804	1	8	15	RAM_CAS_L	38 40 45
RAM_BA_R<0>	RP3804	4	5	15	RAM_BA<0>	38 40 45
RAM_BA_R<1>	RP3804	2	7	15	RAM_BA<1>	38 40 45
RAM_RAS_L_R	RP3804	3	6	15	RAM_RAS_L	38 40 45
RAM_A_R<9>	RP3834	3	6	15	RAM_A<9>	38 40 44
RAM_A_R<8>	RP3834	4	5	15	RAM_A<8>	38 40 44

RAM_DQ_R<68>	RP3818	2	7	22	RAM_DQ<68>	38 40 45
RAM_DQ_R<65>	RP3805	2	7	22	RAM_DQ<65>	38 40 45
RAM_DQ_R<70>	RP3818	4	5	22	RAM_DQ<70>	38 40 45
RAM_DQ_R<66>	RP3805	1	8	22	RAM_DQ<66>	38 40 45
RAM_DQ_R<71>	RP3818	3	6	22	RAM_DQ<71>	38 40 45
RAM_DQ_R<64>	RP3805	4	5	22	RAM_DQ<64>	38 40 45
RAM_DQ_R<67>	RP3805	3	6	22	RAM_DQ<67>	38 40 45
RAM_DQ_R<69>	RP3818	1	8	22	RAM_DQ<69>	38 40 45
RAM_DQ_R<74>	RP3817	3	6	22	RAM_DQ<74>	38 40 45
RAM_DQ_R<73>	RP3802	4	5	22	RAM_DQ<73>	38 40 45
RAM_DQ_R<72>	RP3817	2	7	22	RAM_DQ<72>	38 40 45
RAM_DQ_R<75>	RP3817	4	5	22	RAM_DQ<75>	38 40 45
RAM_DQ_R<78>	RP3802	2	7	22	RAM_DQ<78>	38 40 45
RAM_DQ_R<79>	RP3817	1	8	22	RAM_DQ<79>	38 40 45
RAM_DQ_R<77>	RP3802	1	8	22	RAM_DQ<77>	38 40 45
RAM_DQ_R<76>	RP3802	3	6	22	RAM_DQ<76>	38 40 45
RAM_DQ_R<87>	RP3806	2	7	22	RAM_DQ<87>	38 40 45
RAM_DQ_R<86>	RP3821	1	8	22	RAM_DQ<86>	38 40 45
RAM_DQ_R<81>	RP3821	4	5	22	RAM_DQ<81>	38 40 45
RAM_DQ_R<80>	RP3821	2	7	22	RAM_DQ<80>	38 40 45
RAM_DQ_R<84>	RP3806	1	8	22	RAM_DQ<84>	38 40 45
RAM_DQ_R<85>	RP3806	3	6	22	RAM_DQ<85>	38 40 45
RAM_DQ_R<83>	RP3821	3	6	22	RAM_DQ<83>	38 40 45
RAM_DQ_R<82>	RP3806	4	5	22	RAM_DQ<82>	38 40 45
RAM_DQ_R<91>	RP3819	3	6	22	RAM_DQ<91>	38 40 45
RAM_DQ_R<93>	RP3819	1	8	22	RAM_DQ<93>	38 40 45
RAM_DQ_R<94>	RP3803	2	7	22	RAM_DQ<94>	38 40 45
RAM_DQ_R<90>	RP3819	4	5	22	RAM_DQ<90>	38 40 45
RAM_DQ_R<88>	RP3803	4	5	22	RAM_DQ<88>	38 40 45
RAM_DQ_R<89>	RP3819	2	7	22	RAM_DQ<89>	38 40 45
RAM_DQ_R<92>	RP3803	3	6	22	RAM_DQ<92>	38 40 45
RAM_DQ_R<95>	RP3803	1	8	22	RAM_DQ<95>	38 40 45
RAM_DQ_R<98>	RP3820	4	5	22	RAM_DQ<98>	38 40 45
RAM_DQ_R<96>	RP3820	3	6	22	RAM_DQ<96>	38 40 45
RAM_DQ_R<103>	RP3820	2	7	22	RAM_DQ<103>	38 40 45
RAM_DQ_R<97>	RP3820	1	8	22	RAM_DQ<97>	38 40 45
RAM_DQ_R<100>	RP3825	2	7	22	RAM_DQ<100>	38 40 45
RAM_DQ_R<99>	RP3825	3	6	22	RAM_DQ<99>	38 40 45
RAM_DQ_R<102>	RP3825	1	8	22	RAM_DQ<102>	38 40 45
RAM_DQ_R<101>	RP3825	4	5	22	RAM_DQ<101>	38 40 45
RAM_DQ_R<111>	RP3809	1	8	22	RAM_DQ<111>	38 40 45
RAM_DQ_R<106>	RP3809	3	6	22	RAM_DQ<106>	38 40 45
RAM_DQ_R<105>	RP3809	2	7	22	RAM_DQ<105>	38 40 45
RAM_DQ_R<108>	RP3829	2	7	22	RAM_DQ<108>	38 40 45
RAM_DQ_R<107>	RP3829	4	5	22	RAM_DQ<107>	38 40 45
RAM_DQ_R<110>	RP3829	3	6	22	RAM_DQ<110>	38 40 45
RAM_DQ_R<104>	RP3809	4	5	22	RAM_DQ<104>	38 40 45
RAM_DQ_R<109>	RP3829	1	8	22	RAM_DQ<109>	38 40 45
RAM_DQ_R<119>	RP3828	4	5	22	RAM_DQ<119>	38 40 45
RAM_DQ_R<112>	RP3815	2	7	22	RAM_DQ<112>	38 40 45
RAM_DQ_R<117>	RP3815	1	8	22	RAM_DQ<117>	38 40 45
RAM_DQ_R<118>	RP3828	1	8	22	RAM_DQ<118>	38 40 45
RAM_DQ_R<113>	RP3815	3	6	22	RAM_DQ<113>	38 40 45
RAM_DQ_R<115>	RP3828	3	6	22	RAM_DQ<115>	38 40 45
RAM_DQ_R<116>	RP3828	2	7	22	RAM_DQ<116>	38 40 45
RAM_DQ_R<114>	RP3815	4	5	22	RAM_DQ<114>	38 40 45
RAM_DQ_R<121>	RP3827	3	6	22	RAM_DQ<121>	38 40 45
RAM_DQ_R<124>	RP3827	2	7	22	RAM_DQ<124>	38 40 45
RAM_DQ_R<120>	RP3827	4	5	22	RAM_DQ<120>	38 40 45
RAM_DQ_R<123>	RP3810	2	7	22	RAM_DQ<123>	38 40 45
RAM_DQ_R<125>	RP3827	1	8	22	RAM_DQ<125>	38 40 45
RAM_DQ_R<122>	RP3810	4	5	22	RAM_DQ<122>	38 40 45
RAM_DQ_R<126>	RP3810	1	8	22	RAM_DQ<126>	38 40 45
RAM_DQ_R<127>	RP3810	3	6	22	RAM_DQ<127>	38 40 45

THE FOLLOWING ARE 0402 5% RESISTORS

RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P	38 40
RAM_CLK_A_N_R	R3817	1	2	15	RAM_CLK_A_N	38 40
RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P	38 40
RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N	38 40
RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P	38 40
RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N	38 40
RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P	38 40
RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N	38 40
RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P	38 40
RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N	38 40
RAM_CLK_F_P_R	R3826	1	2	15	RAM_CLK_F_P	38 40
RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N	38 40

RAM_DQS_R<0>	R3800	1	2	15	RAM_DQS<0>	38 40 44
RAM_DQS_R<1>	R3801	1	2	15	RAM_DQS<1>	38 40 44
RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>	38 40 44
RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>	38 40 44
RAM_DQS_R<4>	R3804	1	2	15	RAM_DQS<4>	38 40 44
RAM_DQS_R<5>	R3805	1	2	15	RAM_DQS<5>	38 40 44
RAM_DQS_R<6>	R3806	1	2	15	RAM_DQS<6>	38 40 44
RAM_DQS_R<7>	R3807	1	2	15	RAM_DQS<7>	38 40 44
RAM_DQS_R<8>	R3808	1	2	15	RAM_DQS<8>	38 40 45
RAM_DQS_R<9>	R3809	1	2	15	RAM_DQS<9>	38 40 45
RAM_DQS_R<10>	R3810	1	2	15	RAM_DQS<10>	38 40 45
RAM_DQS_R<11>	R3811	1	2	15	RAM_DQS<11>	38 40 45
RAM_DQS_R<12>	R3812	1	2	15	RAM_DQS<12>	38 40 45
RAM_DQS_R<13>	R3813	1	2	15	RAM_DQS<13>	38 40 45
RAM_DQS_R<14>	R3814	1	2	15	RAM_DQS<14>	38 40 45
RAM_DQS_R<15>	R3815	1	2	15	RAM_DQS<15>	38 40 45

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
RAM_CLK_A_P_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	2506
RAM_CLK_A_N_R		RAM_CLK	RAM_CLK	RAM_CLK_A_R	2507
RAM_CLK_B_P_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	2508
RAM_CLK_B_N_R		RAM_CLK	RAM_CLK	RAM_CLK_B_R	2509
RAM_CLK_C_P_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	2510
RAM_CLK_C_N_R		RAM_CLK	RAM_CLK	RAM_CLK_C_R	2511
RAM_CLK_D_P_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	2512
RAM_CLK_D_N_R		RAM_CLK	RAM_CLK	RAM_CLK_D_R	2513
RAM_CLK_E_P_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	2514
RAM_CLK_E_N_R		RAM_CLK	RAM_CLK	RAM_CLK_E_R	2515
RAM_CLK_F_P_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	2516
RAM_CLK_F_N_R		RAM_CLK	RAM_CLK	RAM_CLK_F_R	2517
RAM_CLK_A_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	2518
RAM_CLK_A_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_A	2519
RAM_CLK_B_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	2520
RAM_CLK_B_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_B	2521
RAM_CLK_C_P	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	2522
RAM_CLK_C_N	RAM_CLK0	RAM_CLK	RAM_CLK	RAM_CLK_C	2523
RAM_CLK_D_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	2524
RAM_CLK_D_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_D	2525
RAM_CLK_E_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	2526
RAM_CLK_E_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_E	2527
RAM_CLK_F_P	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	2528
RAM_CLK_F_N	RAM_CLK1	RAM_CLK	RAM_CLK	RAM_CLK_F	2529
RAM_CKE_R<1..0>		RAM_CAD	RAM_CAD		2530
RAM_CKE_R<5..4>		RAM_CAD	RAM_CAD		2531
RAM_CKE<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		2534
RAM_CKE<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		2535
RAM_CKE<4>	RAM_CKECS1	RAM_CAD	RAM_CAD		2536
RAM_CKE<5>	RAM_CKECS1	RAM_CAD	RAM_CAD		2537
RAM_CS_L_R<1..0>		RAM_CAD	RAM_CAD		2538
RAM_CS_L_R<9..8>		RAM_CAD	RAM_CAD		2541
RAM_CS_L<0>	RAM_CKECS0	RAM_CAD	RAM_CAD		2543
RAM_CS_L<1>	RAM_CKECS0	RAM_CAD	RAM_CAD		2542
RAM_CS_L<8>	RAM_CKECS1	RAM_CAD	RAM_CAD		2540
RAM_CS_L<9>	RAM_CKECS1	RAM_CAD	RAM_CAD		2544
RAM_DQS_R<15..0>		RAM_CAD	RAM_CAD		2505
RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		2504
RAM_DQ<127..0>		RAM_CAD	RAM_CAD		2503
RAM_DQS<0>	RAM_DQS0	RAM_CAD	RAM_CAD		2546
RAM_DQ<7..0>	RAM_DQS0	RAM_CAD	RAM_CAD		2545
RAM_DQS<1>	RAM_DQS1	RAM_CAD	RAM_CAD		2551
RAM_DQ<15..8>	RAM_DQS1	RAM_CAD	RAM_CAD		2552
RAM_DQS<2>	RAM_DQS2	RAM_CAD	RAM_CAD		2553
RAM_DQ<23..16>	RAM_DQS2	RAM_CAD	RAM_CAD		2554
RAM_DQS<3>	RAM_DQS3	RAM_CAD	RAM_CAD		2555
RAM_DQ<31..24>	RAM_DQS3	RAM_CAD	RAM_CAD		2556
RAM_DQS<4>	RAM_DQS4	RAM_CAD	RAM_CAD		2557
RAM_DQ<39..32>	RAM_DQS4	RAM_CAD	RAM_CAD		2558
RAM_DQS<5>	RAM_DQS5	RAM_CAD	RAM_CAD		2559
RAM_DQ<47..40>	RAM_DQS5	RAM_CAD	RAM_CAD		2560
RAM_DQS<6>	RAM_DQS6	RAM_CAD	RAM_CAD		2561
RAM_DQ<55..48>	RAM_DQS6	RAM_CAD	RAM_CAD		2562
RAM_DQS<7>	RAM_DQS7	RAM_CAD	RAM_CAD		2563
RAM_DQ<63..56>	RAM_DQS7	RAM_CAD	RAM_CAD		2564
RAM_DQS<8>	RAM_DQS8	RAM_CAD	RAM_CAD		2565
RAM_DQ<71..64>	RAM_DQS8	RAM_CAD	RAM_CAD		2567
RAM_DQS<9>	RAM_DQS9	RAM_CAD	RAM_CAD		2566
RAM_DQ<79..72>	RAM_DQS9	RAM_CAD	RAM_CAD		2568
RAM_DQS<10>	RAM_DQS10	RAM_CAD	RAM_CAD		2570
RAM_DQ<87..80>	RAM_DQS10	RAM_CAD	RAM_CAD		2569
RAM_DQS<11>	RAM_DQS11	RAM_CAD	RAM_CAD		2572
RAM_DQ<95..88>	RAM_DQS11	RAM_CAD	RAM_CAD		2571
RAM_DQS<12>	RAM_DQS12	RAM_CAD	RAM_CAD		2573
RAM_DQ<103..96>	RAM_DQS12	RAM_CAD	RAM_CAD		2575
RAM_DQS<13>	RAM_DQS13	RAM_CAD	RAM_CAD		2574
RAM_DQ<111..104>	RAM_DQS13	RAM_CAD	RAM_CAD		2577
RAM_DQS<14>	RAM_DQS14	RAM_CAD	RAM_CAD		2576
RAM_DQ<119..112>	RAM_DQS14	RAM_CAD	RAM_CAD		2578
RAM_DQS<15>	RAM_DQS15	RAM_CAD	RAM_CAD		2580
RAM_DQ<127..120>	RAM_DQS15	RAM_CAD	RAM_CAD		2579
RAM_A_R<13..0>		RAM_CAD	RAM_CAD		2596
RAM_BA_R<1..0>		RAM_CAD	RAM_CAD		2595
RAM_RAS_L_R		RAM_CAD	RAM_CAD		2597
RAM_CAS_L_R		RAM_CAD	RAM_CAD		2598
RAM_WE_L_R		RAM_CAD	RAM_CAD		2599
RAM_A<13..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		2600
RAM_BA<1..0>	RAM_A_CTL	RAM_CAD	RAM_CAD		2594
RAM_RAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		2593
RAM_CAS_L	RAM_A_CTL	RAM_CAD	RAM_CAD		2592
RAM_WE_L	RAM_A_CTL	RAM_CAD	RAM_CAD		2591

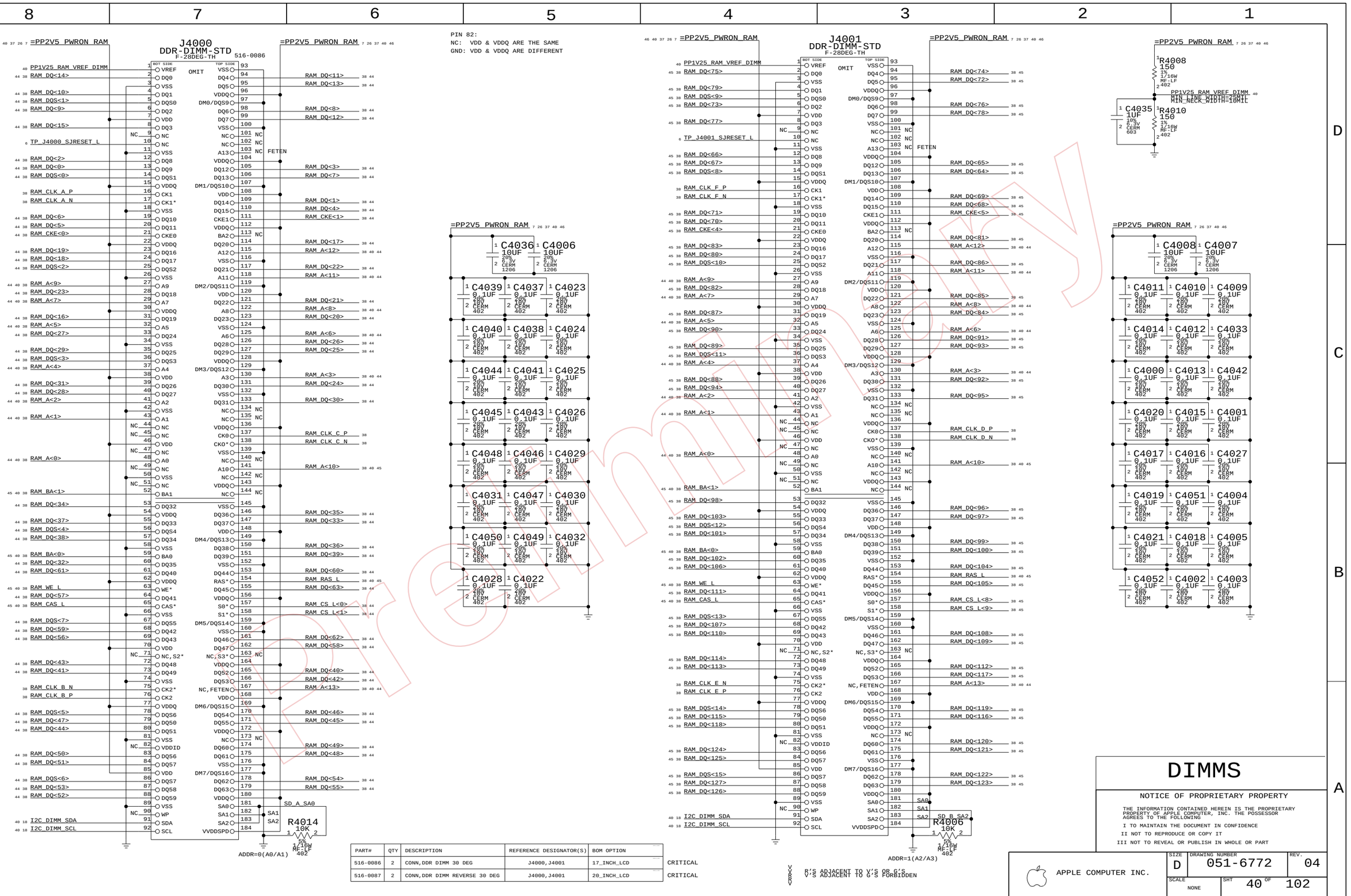
RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

SERIES TERM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 38 OF 102	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
516-0086	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD
516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD

CRITICAL

CRITICAL

V V V V D'S ADJACENT TO V'S OR G'S
V V V V V'S ADJACENT TO G'S FORBIDDEN

DIMMS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

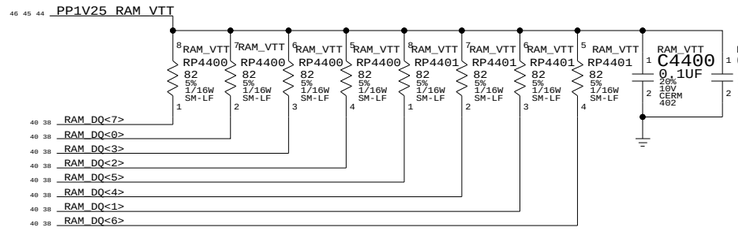
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

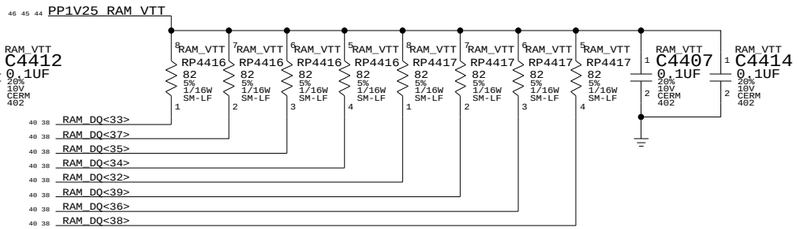
II NOT TO REPRODUCE OR COPY IT

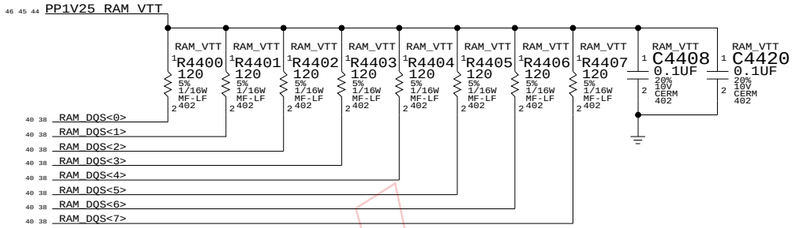
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

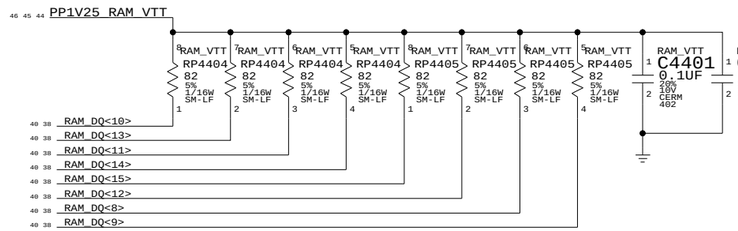
APPLE COMPUTER INC.

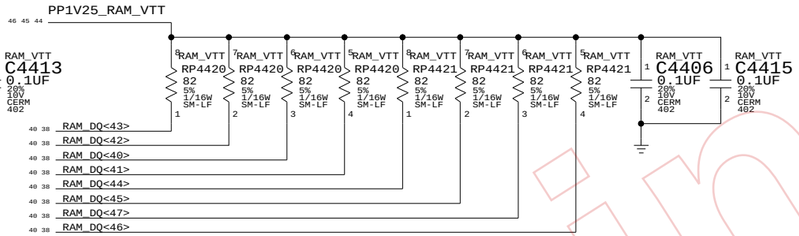
SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 40 OF 102	

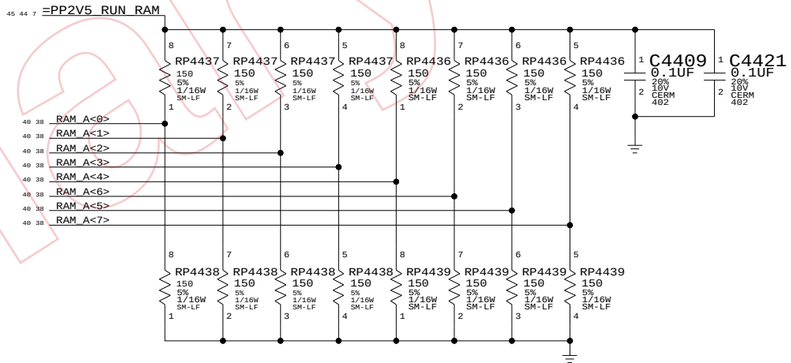


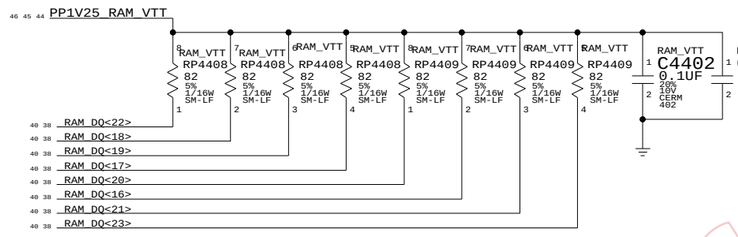


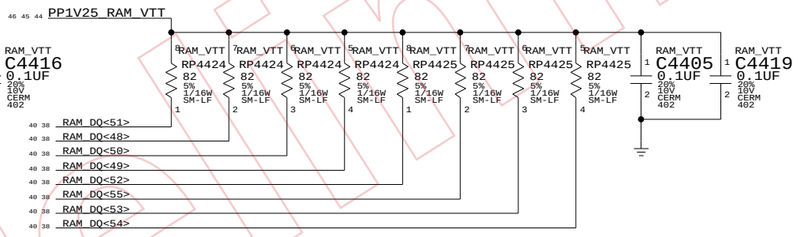


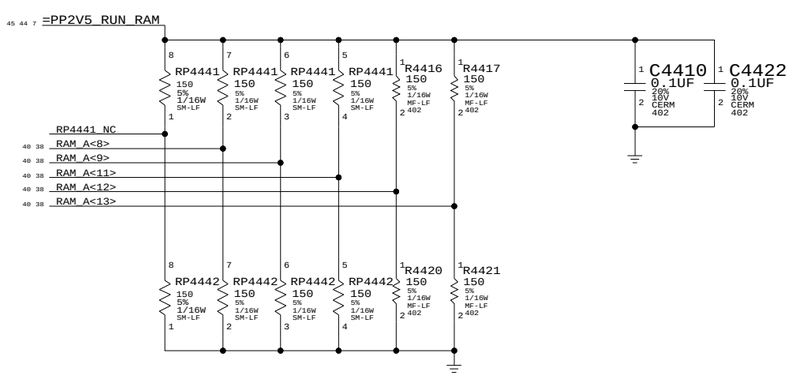


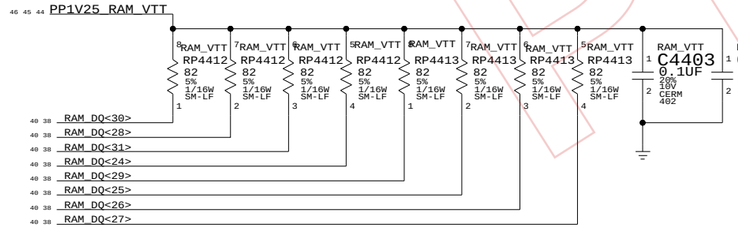


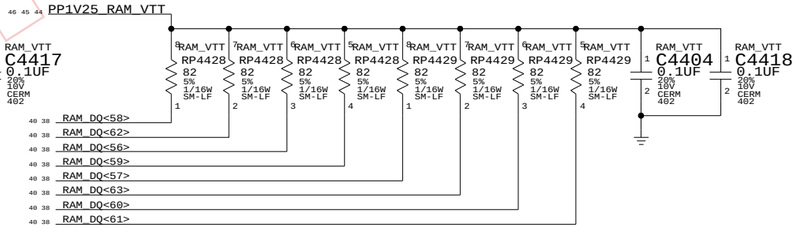


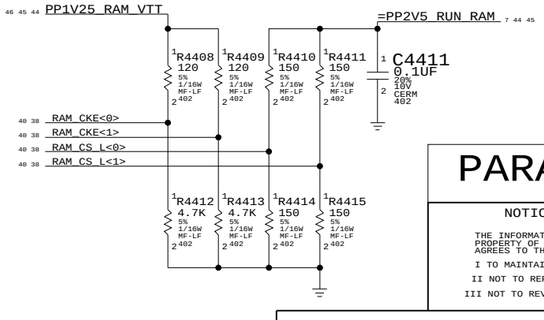








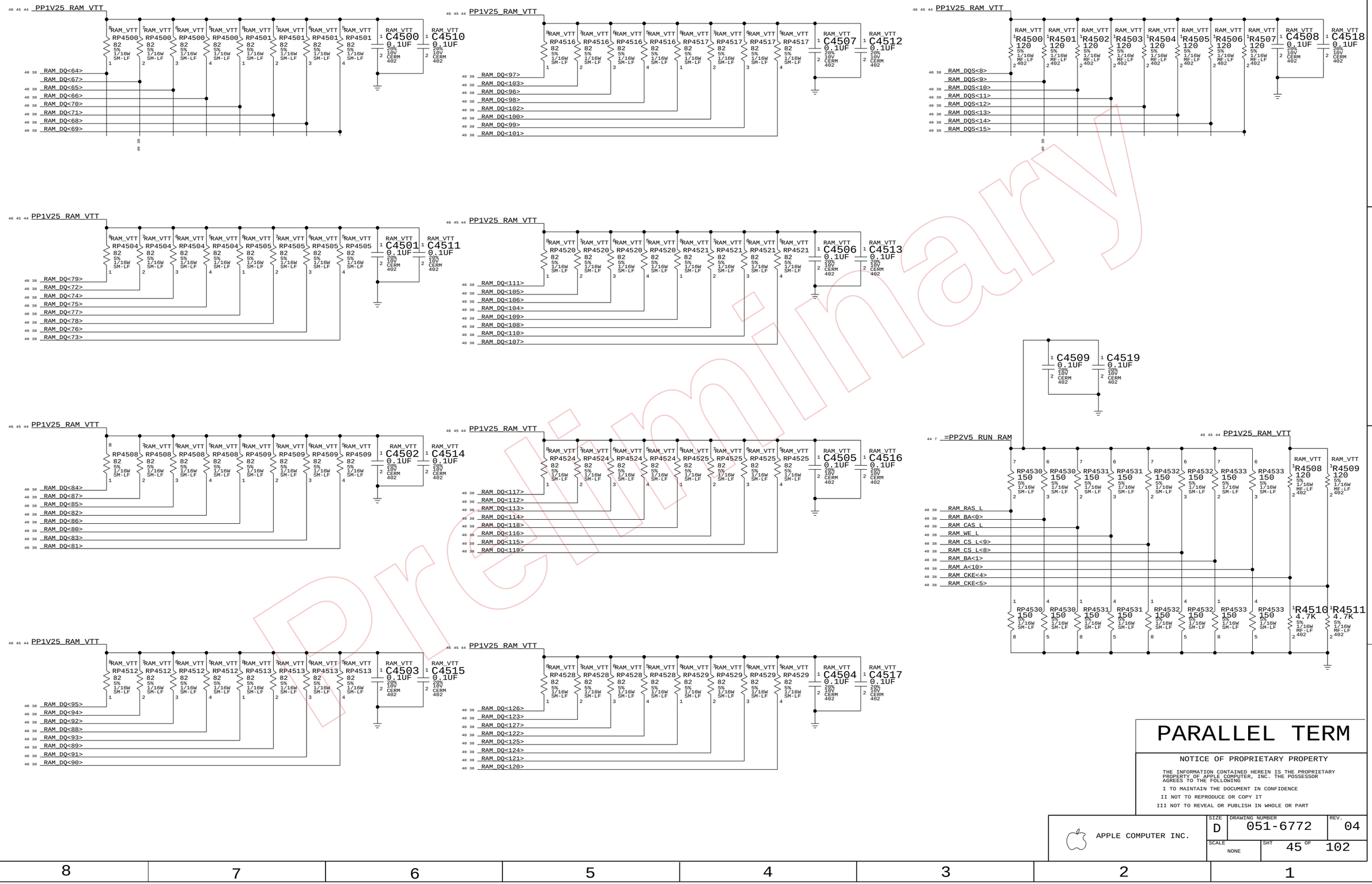




PARALLEL TERM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 44 OF 102	

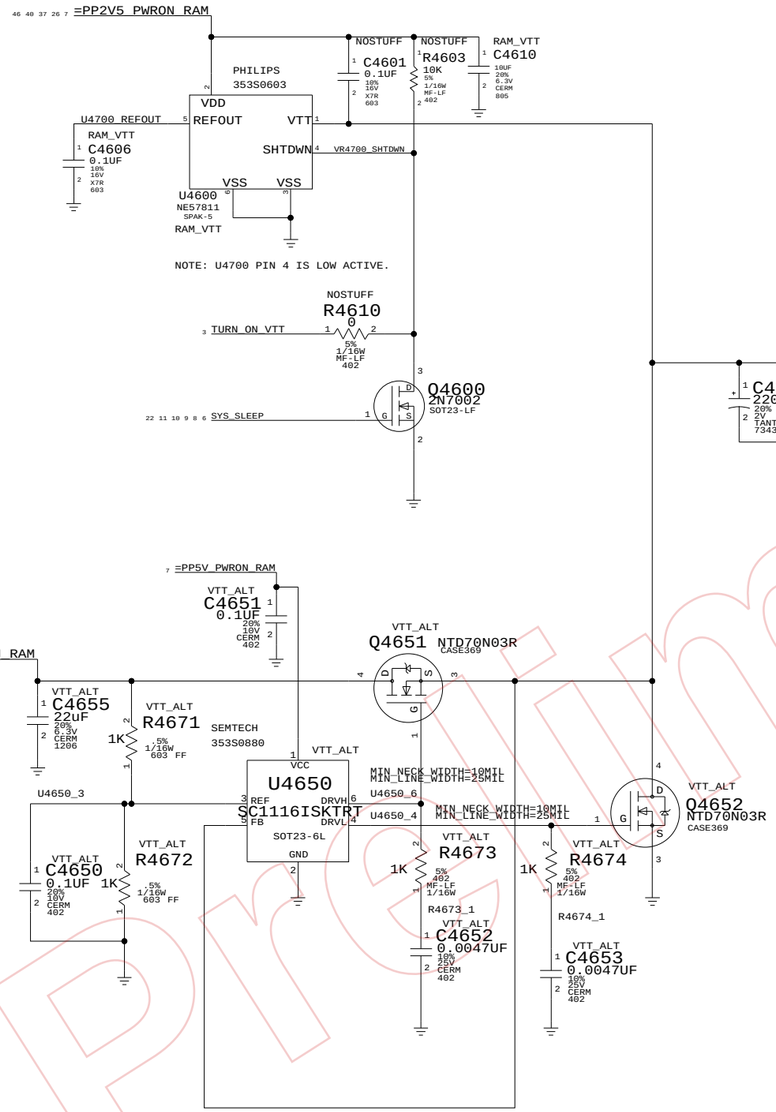


PARALLEL TERM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 45 OF 102	

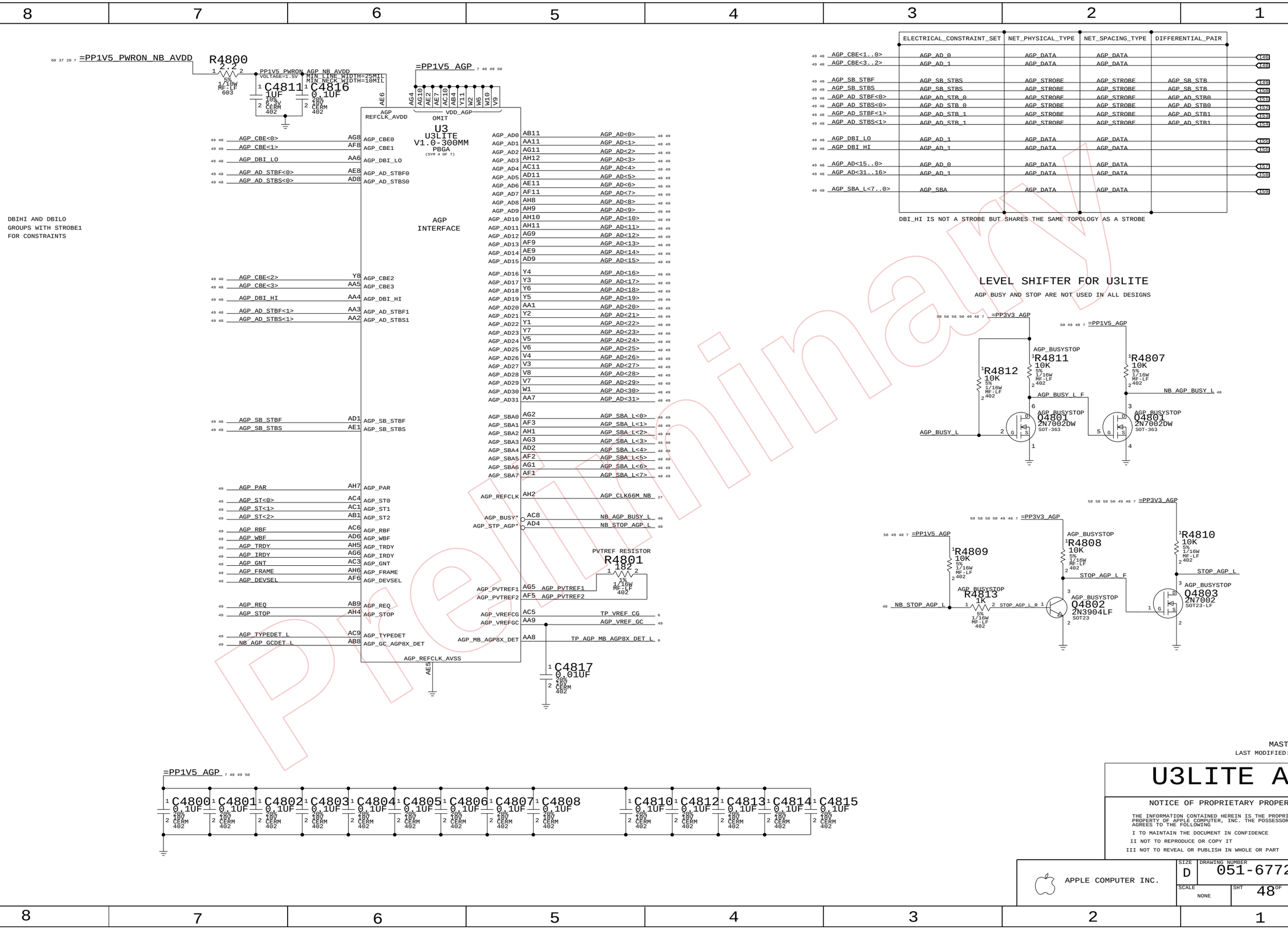
ONLY STUFF ONE VTT VREG



MEM TERM VREGS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 46 OF 102	



MASTER: SEEDY
LAST MODIFIED: NOV 18, 04

U3LITE AGP

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6772	04
	SCALE NONE	SHT 48 OF 102	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0231	1	IC,RV351LEP, GRAPHICS CTLR	U4900	

U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)

50 49 48 7 =PP1V5_AGP

R4914 3.32K 1% 1/16W MF-LF 402

AGP_VREF_GC 48

R4940 1.02K 1% 1/16W MF-LF 402

C4940 0.01UF 20% 16V CERM 402

VOLTAGE=0.35V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

GPU AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALLS)

50 49 48 7 =PP1V5_AGP

R4906 3.32K 1% 1/16W MF-LF 402

AGP 3.0
0.233 * VDDP
0.35V

GPU_AGP_VREF 49

VOLTAGE=0.35V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM

R4907 1.02K 1% 1/16W MF-LF 402

C4957 0.01UF 20% 16V CERM 402

DO WE NEED THE SERIES R?

8 GPU_RESET_L — R4912 0 5% 1/16W MF-LF 402 — ATI_PCIRST_L AG28

50 49 48 7 =PP1V5_AGP

C4900 1UF 10% 6.3V CERM 402

C4901 1UF 10% 6.3V CERM 402

C4902 0.01UF 20% 16V CERM 402

C4903 0.01UF 20% 16V CERM 402

C4904 0.01UF 20% 16V CERM 402

C4905 0.01UF 20% 16V CERM 402

AA23 AA24 P27 T24 T30 U27 V23 V24 W30 Y27 AB30 AC23 AC27 AE30 AF27 J30 M23 M24 N30 P23 T23

VDDP

OMIT

U4900
RV351
BGA
(1 OF 5)

AGP

27 AGP_CLK66M_GPU	AG30	PCICLK
48 AGP_AD<0>	H29	AD0
48 AGP_AD<1>	H28	AD1
48 AGP_AD<2>	J29	AD2
48 AGP_AD<3>	J28	AD3
48 AGP_AD<4>	K29	AD4
48 AGP_AD<5>	K28	AD5
48 AGP_AD<6>	L29	AD6
48 AGP_AD<7>	L28	AD7
48 AGP_AD<8>	N28	AD8
48 AGP_AD<9>	P29	AD9
48 AGP_AD<10>	P28	AD10
48 AGP_AD<11>	R29	AD11
48 AGP_AD<12>	R28	AD12
48 AGP_AD<13>	T29	AD13
48 AGP_AD<14>	T28	AD14
48 AGP_AD<15>	U29	AD15
48 AGP_AD<16>	N25	AD16
48 AGP_AD<17>	R26	AD17
48 AGP_AD<18>	P25	AD18
48 AGP_AD<19>	R27	AD19
48 AGP_AD<20>	R25	AD20
48 AGP_AD<21>	T25	AD21
48 AGP_AD<22>	T26	AD22
48 AGP_AD<23>	U25	AD23
48 AGP_AD<24>	V27	AD24
48 AGP_AD<25>	W26	AD25
48 AGP_AD<26>	W25	AD26
48 AGP_AD<27>	Y26	AD27
48 AGP_AD<28>	Y25	AD28
48 AGP_AD<29>	AA26	AD29
48 AGP_AD<30>	AA25	AD30
48 AGP_AD<31>	AA27	AD31
48 AGP_SBA_L<0>	AD28	SBA0
48 AGP_SBA_L<1>	AD29	SBA1
48 AGP_SBA_L<2>	AC28	SBA2
48 AGP_SBA_L<3>	AC29	SBA3
48 AGP_SBA_L<4>	AA28	SBA4
48 AGP_SBA_L<5>	AA29	SBA5
48 AGP_SBA_L<6>	Y28	SBA6
48 AGP_SBA_L<7>	Y29	SBA7
	AG28	RST*
48 AGP_ST<0>	AF29	ST0
48 AGP_ST<1>	AD27	ST1
48 AGP_ST<2>	AE28	ST2
48 AGP_REQ	AF28	REQ*
48 AGP_GNT	AD26	GNT*
48 AGP_STOP	N26	STOP*
48 AGP_DEVSEL	V29	DEVSEL*
48 AGP_TRDY	V28	TRDY*
48 AGP_IRDY	W29	IRDY*
48 AGP_FRAME	W28	FRAME*
48 AGP_WBF	AC26	WBF*
48 AGP_RBF	AE29	RBF*

GPU_AGP_VREF 49

C4910 0.01UF 20% 16V CERM 402

PLACE C4910 CLOSE TO BALL M26

AGPREF	M26	
CBE0*	N29	AGP_CBE<0> 48
CBE1*	U28	AGP_CBE<1> 48
DBI_LO	AB26	AGP_DBI_LO 48
AD_STBF_0	M28	AGP_AD_STBF<0> 48
AD_STBS_0*	M29	AGP_AD_STBS<0> 48
CBE2*	P26	AGP_CBE<2> 48
CBE3*	U26	AGP_CBE<3> 48
DBI_HI	AB25	AGP_DBI_HI 48
AD_STBF_1	V25	AGP_AD_STBF<1> 48
AD_STBS_1*	V26	AGP_AD_STBS<1> 48
SB_STBF	AB29	AGP_SB_STBF 48
SB_STBS*	AB28	AGP_SB_STBS 48
PAR	M25	AGP_PAR 48
INTA*	AE26	
AGPTEST*	M27	GPU_AGPTEST_L — R4910 47 1% 1/16W MF-LF 402 — =PP1V5_AGP 7 48 49 50
AGP8X_DET*	AC25	

=PP3V3_AGP 7 48 50 56 58 59

R4908 10K 5% 1/16W MF-LF 402

AGP_INT_L 25

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

U3LITE SIGNALS

48 NB_AGP_GCDET_L

48 AGP_TYPEDET_L

R4913 0 5% 1/16W MF-LF 402

R4909 10k 5% 1/16W MF-LF 402

GPU AGP

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

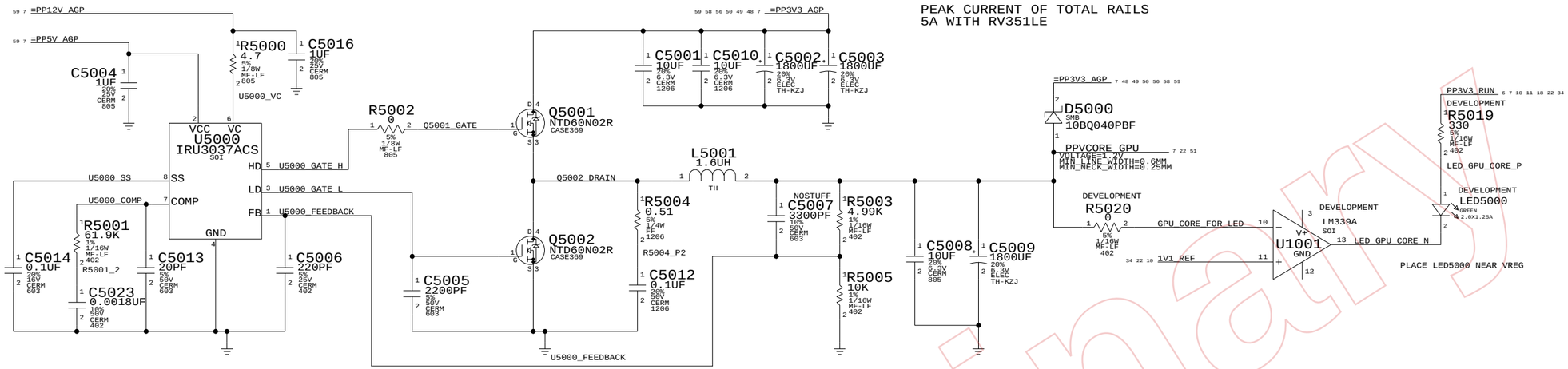
SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 49 OF 102	

GPU VCORE VREG

NOTE:
SET OUTPUT = 1.20V +/- 5% FOR RV351LE

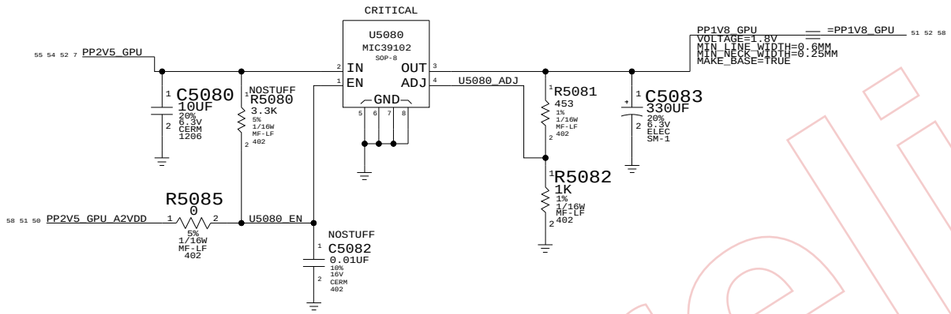
IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R5003+R5005)/R5005 = 1.199 VDC

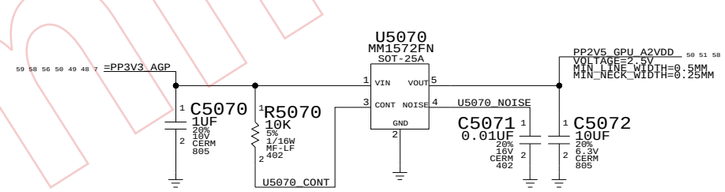
PEAK CURRENT OF TOTAL RAILS
5A WITH RV351LE



GPU 1.8V VREG

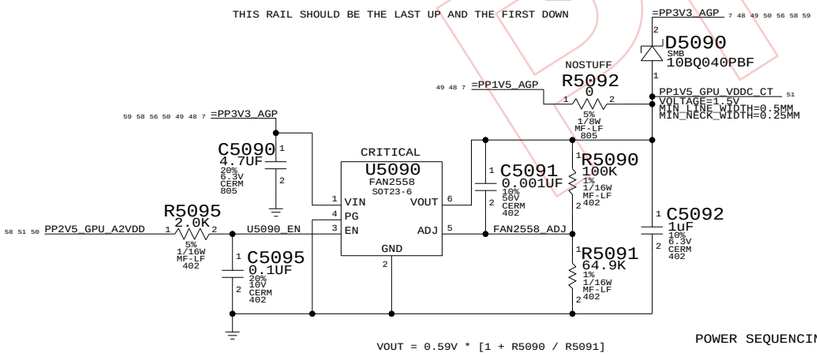
GPU 2.5V A2VDD





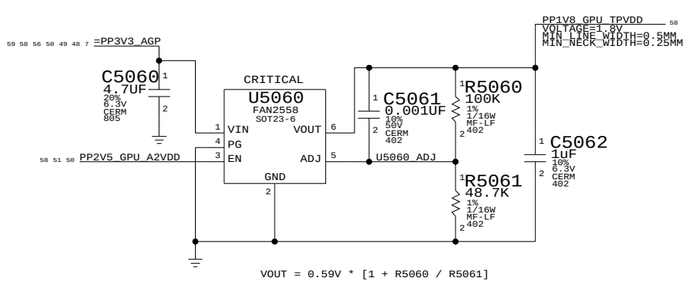
GPU 1.50V VDDC_CT

THIS RAIL SHOULD BE THE LAST UP AND THE FIRST DOWN



VOUT = 0.59V * [1 + R5090 / R5091]
VOUT = 1.50V

GPU 1.80V TPVDD



VOUT = 0.59V * [1 + R5060 / R5061]
VOUT = 1.80V

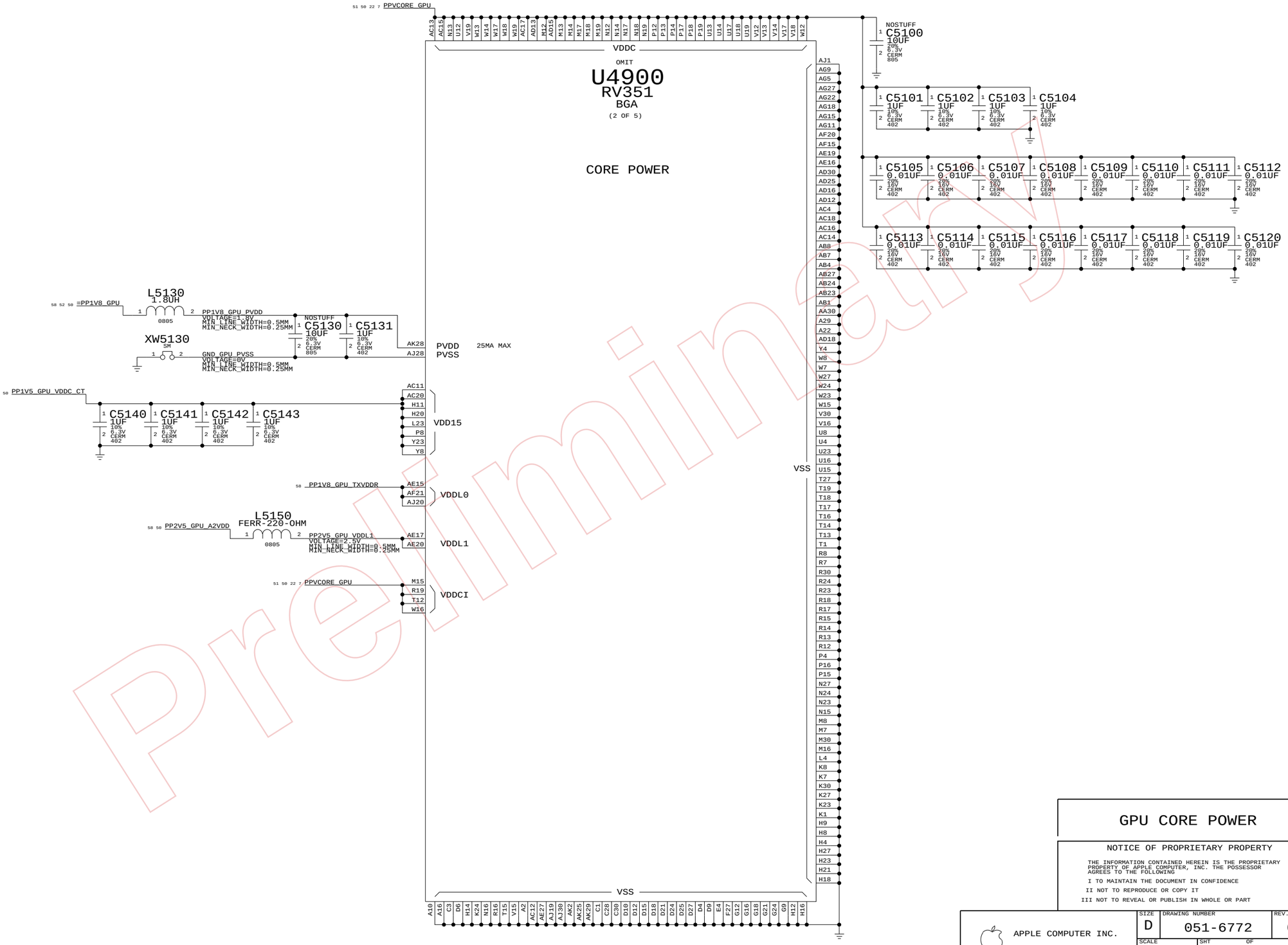
POWER SEQUENCING FOR RV351: =PP3V3_AGP > PP2V5_GPU > PPVCORE_GPU > VDDC_CT
PP2V5_GPU_A2VDD > PP1V8_GPU
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER

POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

GRAPHICS VREGS

APPLE COMPUTER INC.

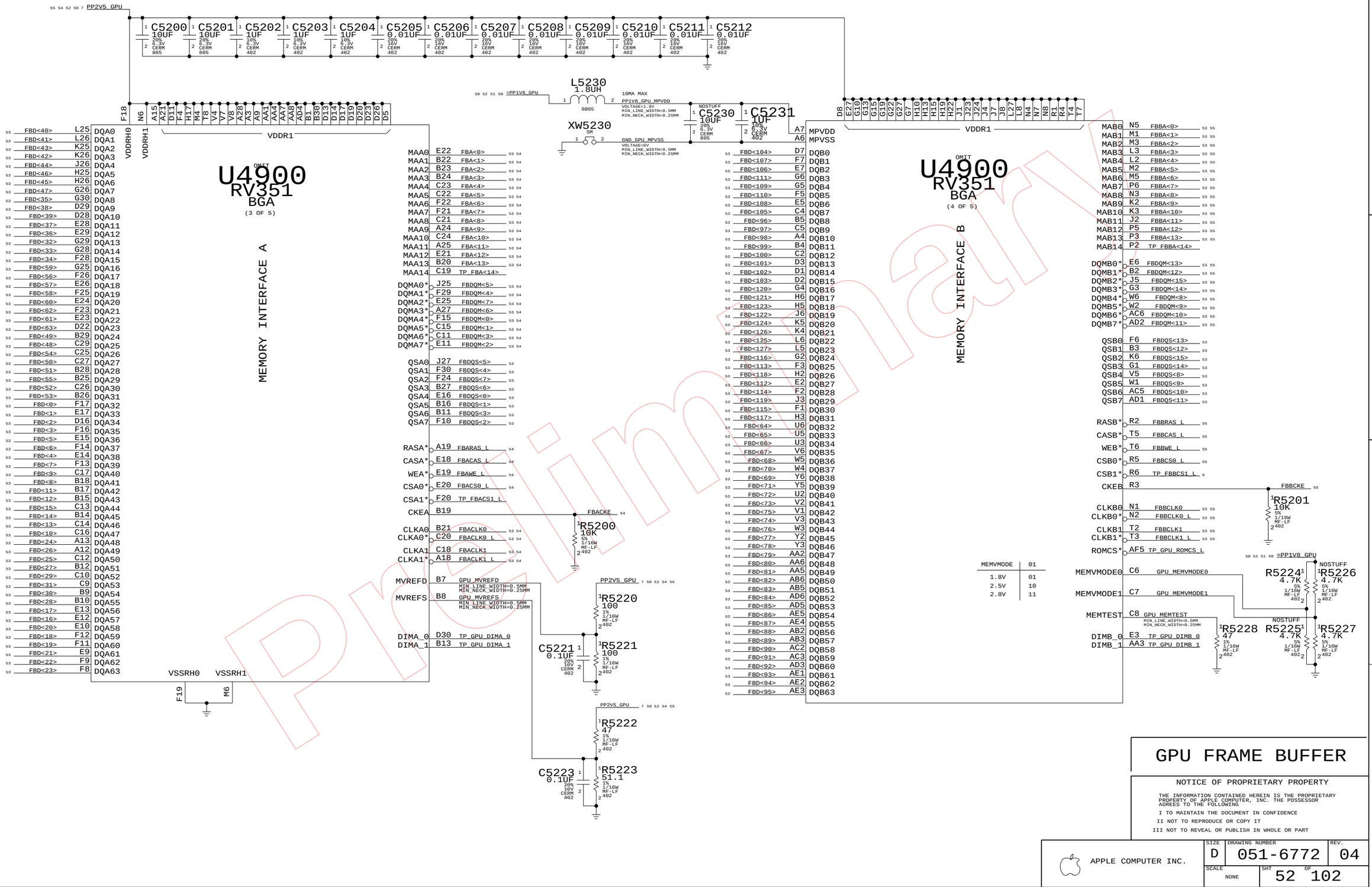
SIZE D | DRAWING NUMBER 051-6772 | REV. 04
SCALE NONE | SHT 50 OF 102



GPU CORE POWER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 51	OF 102


PP2V5_GPU
C5200 10UF 20% 6.3V CERM 805
C5201 10UF 20% 6.3V CERM 805
C5202 1UF 10% 6.3V CERM 402
C5203 1UF 10% 6.3V CERM 402
C5204 1UF 10% 6.3V CERM 402
C5205 0.01UF 20% 16V CERM 402
C5206 0.01UF 20% 16V CERM 402
C5207 0.01UF 20% 16V CERM 402
C5208 0.01UF 20% 16V CERM 402
C5209 0.01UF 20% 16V CERM 402
C5210 0.01UF 20% 16V CERM 402
C5211 0.01UF 20% 16V CERM 402
C5212 0.01UF 20% 16V CERM 402
L5230 1.8UH 10MA MAX 0805
=PP1V8_GPU
PP1V8_GPU_MPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
C5230 10UF NOSTUFF 20% 6.3V CERM 805
C5231 1UF 10% 6.3V CERM 402
XW5230 SM
GND_GPU_MPVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
VDDR1
VSSRH0
VSSRH1
U4900 RV351 BGA (3 OF 5) OMIT
MEMORY INTERFACE A
DQA0 DQA1 DQA2 DQA3 DQA4 DQA5 DQA6 DQA7 DQA8 DQA9 DQA10 DQA11 DQA12 DQA13 DQA14 DQA15 DQA16 DQA17 DQA18 DQA19 DQA20 DQA21 DQA22 DQA23 DQA24 DQA25 DQA26 DQA27 DQA28 DQA29 DQA30 DQA31 DQA32 DQA33 DQA34 DQA35 DQA36 DQA37 DQA38 DQA39 DQA40 DQA41 DQA42 DQA43 DQA44 DQA45 DQA46 DQA47 DQA48 DQA49 DQA50 DQA51 DQA52 DQA53 DQA54 DQA55 DQA56 DQA57 DQA58 DQA59 DQA60 DQA61 DQA62 DQA63
MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14
DQMA0* DQMA1* DQMA2* DQMA3* DQMA4* DQMA5* DQMA6* DQMA7*
QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
RASA* CASA* WEA* CSA0* CSA1* CKEA
CLKA0 CLKA0* CLKA1 CLKA1*
MVREFD MVREFS
DIMA_0 DIMA_1
R5200 10K 5% 1/16W MF-LF 402
R5220 100 1% 1/16W MF-LF 402
R5221 100 1% 1/16W MF-LF 402
R5222 47 1% 1/16W MF-LF 402
R5223 51.1 1% 1/16W MF-LF 402
C5221 0.1UF 20% 10V CERM 402
C5223 0.1UF 20% 10V CERM 402
U4900 RV351 BGA (4 OF 5) OMIT
MEMORY INTERFACE B
MPVDD MPVSS
DQB0 DQB1 DQB2 DQB3 DQB4 DQB5 DQB6 DQB7 DQB8 DQB9 DQB10 DQB11 DQB12 DQB13 DQB14 DQB15 DQB16 DQB17 DQB18 DQB19 DQB20 DQB21 DQB22 DQB23 DQB24 DQB25 DQB26 DQB27 DQB28 DQB29 DQB30 DQB31 DQB32 DQB33 DQB34 DQB35 DQB36 DQB37 DQB38 DQB39 DQB40 DQB41 DQB42 DQB43 DQB44 DQB45 DQB46 DQB47 DQB48 DQB49 DQB50 DQB51 DQB52 DQB53 DQB54 DQB55 DQB56 DQB57 DQB58 DQB59 DQB60 DQB61 DQB62 DQB63
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13 MAB14
DQMB0* DQMB1* DQMB2* DQMB3* DQMB4* DQMB5* DQMB6* DQMB7*
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
RASB* CASB* WEB* CSB0* CSB1* CKEB
CLKB0 CLKB0* CLKB1 CLKB1*
ROMCS*
MEMVMODE0 MEMVMODE1
MEMTEST
DIMB_0 DIMB_1
R5201 10K 5% 1/16W MF-LF 402
R5224 4.7K 5% 1/16W MF-LF 402
R5226 4.7K 5% 1/16W MF-LF 402
R5225 4.7K 5% 1/16W MF-LF 402
R5227 4.7K 5% 1/16W MF-LF 402
R5228 47 1% 1/16W MF-LF 402
MEMVMODE 01
1.8V 01
2.5V 10
2.8V 11
GPU FRAME BUFFER
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6772
REV. 04
SCALE NONE
SHT 52 OF 102

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

FBD<31>	22	1	8	RP5320	RFBD<31>	53 52	53 54
FBD<30>	22	2	7	RP5320	RFBD<30>	53 52	53 54
FBD<29>	22	3	6	RP5320	RFBD<29>	53 52	53 54
FBD<28>	22	4	5	RP5320	RFBD<28>	53 52	53 54
FBD<27>	22	1	8	RP5321	RFBD<27>	53 52	53 54
FBD<26>	22	2	7	RP5321	RFBD<26>	53 52	53 54
FBD<25>	22	3	6	RP5321	RFBD<25>	53 52	53 54
FBD<24>	22	4	5	RP5321	RFBD<24>	53 52	53 54
FBD<0>	22	1	8	RP5322	RFBD<0>	53 52	53 54
FBD<1>	22	2	7	RP5322	RFBD<1>	53 52	53 54
FBD<2>	22	3	6	RP5322	RFBD<2>	53 52	53 54
FBD<3>	22	4	5	RP5322	RFBD<3>	53 52	53 54
FBD<17>	22	1	8	RP5323	RFBD<17>	53 52	53 54
FBD<16>	22	2	7	RP5323	RFBD<16>	53 52	53 54
FBD<18>	22	3	6	RP5323	RFBD<18>	53 52	53 54
FBD<19>	22	4	5	RP5323	RFBD<19>	53 52	53 54
FBD<15>	22	1	8	RP5324	RFBD<15>	53 52	53 54
FBD<14>	22	2	7	RP5324	RFBD<14>	53 52	53 54
FBD<13>	22	3	6	RP5324	RFBD<13>	53 52	53 54
FBD<12>	22	4	5	RP5324	RFBD<12>	53 52	53 54
FBD<10>	22	1	8	RP5325	RFBD<10>	53 52	53 54
FBD<11>	22	2	7	RP5325	RFBD<11>	53 52	53 54
FBD<9>	22	3	6	RP5325	RFBD<9>	53 52	53 54
FBD<8>	22	4	5	RP5325	RFBD<8>	53 52	53 54
FBD<5>	22	1	8	RP5326	RFBD<5>	53 52	53 54
FBD<6>	22	2	7	RP5326	RFBD<6>	53 52	53 54
FBD<4>	22	3	6	RP5326	RFBD<4>	53 52	53 54
FBD<7>	22	4	5	RP5326	RFBD<7>	53 52	53 54
FBD<20>	22	1	8	RP5327	RFBD<20>	53 52	53 54
FBD<21>	22	2	7	RP5327	RFBD<21>	53 52	53 54
FBD<22>	22	3	6	RP5327	RFBD<22>	53 52	53 54
FBD<23>	22	4	5	RP5327	RFBD<23>	53 52	53 54

FBD<32>	22	3	6	RP5328	RFBD<32>	53 52	53 54
FBD<33>	22	4	5	RP5328	RFBD<33>	53 52	53 54
FBD<34>	22	1	8	RP5328	RFBD<34>	53 52	53 54
FBD<35>	22	2	7	RP5328	RFBD<35>	53 52	53 54
FBD<36>	22	4	5	RP5316	RFBD<36>	53 52	53 54
FBD<37>	22	3	6	RP5316	RFBD<37>	53 52	53 54
FBD<38>	22	2	7	RP5316	RFBD<38>	53 52	53 54
FBD<39>	22	1	8	RP5316	RFBD<39>	53 52	53 54
FBD<40>	22	2	7	RP5329	RFBD<40>	53 52	53 54
FBD<41>	22	1	8	RP5329	RFBD<41>	53 52	53 54
FBD<42>	22	3	6	RP5329	RFBD<42>	53 52	53 54
FBD<43>	22	4	5	RP5329	RFBD<43>	53 52	53 54
FBD<44>	22	1	8	RP5330	RFBD<44>	53 52	53 54
FBD<45>	22	2	7	RP5330	RFBD<45>	53 52	53 54
FBD<46>	22	4	5	RP5330	RFBD<46>	53 52	53 54
FBD<47>	22	3	6	RP5330	RFBD<47>	53 52	53 54
FBD<48>	22	4	5	RP5331	RFBD<48>	53 52	53 54
FBD<49>	22	3	6	RP5331	RFBD<49>	53 52	53 54
FBD<50>	22	1	8	RP5331	RFBD<50>	53 52	53 54
FBD<51>	22	2	7	RP5331	RFBD<51>	53 52	53 54
FBD<52>	22	4	5	RP5300	RFBD<52>	53 52	53 54
FBD<53>	22	3	6	RP5300	RFBD<53>	53 52	53 54
FBD<54>	22	2	7	RP5300	RFBD<54>	53 52	53 54
FBD<55>	22	1	8	RP5300	RFBD<55>	53 52	53 54
FBD<56>	22	1	8	RP5301	RFBD<56>	53 52	53 54
FBD<57>	22	2	7	RP5301	RFBD<57>	53 52	53 54
FBD<58>	22	4	5	RP5301	RFBD<58>	53 52	53 54
FBD<59>	22	3	6	RP5301	RFBD<59>	53 52	53 54
FBD<60>	22	1	8	RP5302	RFBD<60>	53 52	53 54
FBD<61>	22	3	6	RP5302	RFBD<61>	53 52	53 54
FBD<62>	22	2	7	RP5302	RFBD<62>	53 52	53 54
FBD<63>	22	4	5	RP5302	RFBD<63>	53 52	53 54

FBDQS<0>	MAKE_BASE=TRUE	RFBDQS<0>	53 52 54
FBDQS<1>	MAKE_BASE=TRUE	RFBDQS<1>	53 52 54
FBDQS<2>	MAKE_BASE=TRUE	RFBDQS<2>	53 52 54
FBDQS<3>	MAKE_BASE=TRUE	RFBDQS<3>	53 52 54
FBDQS<4>	MAKE_BASE=TRUE	RFBDQS<4>	53 52 54
FBDQS<5>	MAKE_BASE=TRUE	RFBDQS<5>	53 52 54
FBDQS<6>	MAKE_BASE=TRUE	RFBDQS<6>	53 52 54
FBDQS<7>	MAKE_BASE=TRUE	RFBDQS<7>	53 52 54

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

54 53 52 FBACLK0
R5320 56.2 1% 1/10W MF-LF 402
FBACLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R5321 56.2 1% 1/10W MF-LF 402
C5321 0.01UF 20% 16V CERM 402
54 53 52 FBACLK0_L

54 53 52 FBACLK1
R5322 56.2 1% 1/10W MF-LF 402
FBACLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R5323 56.2 1% 1/10W MF-LF 402
C5323 0.01UF 20% 16V CERM 402
54 53 52 FBACLK1_L

FRAME BUFFER B TERMINATION

FBD<64>	GPU128BIT	22	1	8	RP5310	RFBD<64>	53 52	53 55
FBD<65>	GPU128BIT	22	2	7	RP5310	RFBD<65>	53 52	53 55
FBD<66>	GPU128BIT	22	3	6	RP5310	RFBD<66>	53 52	53 55
FBD<67>	GPU128BIT	22	4	5	RP5310	RFBD<67>	53 52	53 55
FBD<84>	GPU128BIT	22	1	8	RP5309	RFBD<84>	53 52	53 55
FBD<85>	GPU128BIT	22	2	7	RP5309	RFBD<85>	53 52	53 55
FBD<86>	GPU128BIT	22	3	6	RP5309	RFBD<86>	53 52	53 55
FBD<87>	GPU128BIT	22	4	5	RP5309	RFBD<87>	53 52	53 55
FBD<72>	GPU128BIT	22	4	5	RP5319	RFBD<72>	53 52	53 55
FBD<73>	GPU128BIT	22	3	6	RP5319	RFBD<73>	53 52	53 55
FBD<75>	GPU128BIT	22	2	7	RP5319	RFBD<75>	53 52	53 55
FBD<74>	GPU128BIT	22	1	8	RP5319	RFBD<74>	53 52	53 55
FBD<68>	GPU128BIT	22	1	8	RP5308	RFBD<68>	53 52	53 55
FBD<70>	GPU128BIT	22	2	7	RP5308	RFBD<70>	53 52	53 55
FBD<69>	GPU128BIT	22	3	6	RP5308	RFBD<69>	53 52	53 55
FBD<71>	GPU128BIT	22	4	5	RP5308	RFBD<71>	53 52	53 55
FBD<80>	GPU128BIT	22	1	8	RP5307	RFBD<80>	53 52	53 55
FBD<81>	GPU128BIT	22	2	7	RP5307	RFBD<81>	53 52	53 55
FBD<82>	GPU128BIT	22	3	6	RP5307	RFBD<82>	53 52	53 55
FBD<83>	GPU128BIT	22	4	5	RP5307	RFBD<83>	53 52	53 55
FBD<76>	GPU128BIT	22	4	5	RP5317	RFBD<76>	53 52	53 55
FBD<77>	GPU128BIT	22	3	6	RP5317	RFBD<77>	53 52	53 55
FBD<78>	GPU128BIT	22	2	7	RP5317	RFBD<78>	53 52	53 55
FBD<79>	GPU128BIT	22	1	8	RP5317	RFBD<79>	53 52	53 55
FBD<91>	GPU128BIT	22	1	8	RP5318	RFBD<91>	53 52	53 55
FBD<90>	GPU128BIT	22	2	7	RP5318	RFBD<90>	53 52	53 55
FBD<89>	GPU128BIT	22	3	6	RP5318	RFBD<89>	53 52	53 55
FBD<88>	GPU128BIT	22	4	5	RP5318	RFBD<88>	53 52	53 55
FBD<95>	GPU128BIT	22	1	8	RP5303	RFBD<95>	53 52	53 55
FBD<94>	GPU128BIT	22	2	7	RP5303	RFBD<94>	53 52	53 55
FBD<93>	GPU128BIT	22	3	6	RP5303	RFBD<93>	53 52	53 55
FBD<92>	GPU128BIT	22	4	5	RP5303	RFBD<92>	53 52	53 55

FBD<96>	GPU128BIT	22	4	5	RP5315	RFBD<96>	53 52	53 55
FBD<97>	GPU128BIT	22	3	6	RP5315	RFBD<97>	53 52	53 55
FBD<98>	GPU128BIT	22	2	7	RP5315	RFBD<98>	53 52	53 55
FBD<99>	GPU128BIT	22	1	8	RP5315	RFBD<99>	53 52	53 55
FBD<100>	GPU128BIT	22	4	5	RP5314	RFBD<100>	53 52	53 55
FBD<101>	GPU128BIT	22	3	6	RP5314	RFBD<101>	53 52	53 55
FBD<102>	GPU128BIT	22	2	7	RP5314	RFBD<102>	53 52	53 55
FBD<103>	GPU128BIT	22	1	8	RP5314	RFBD<103>	53 52	53 55
FBD<104>	GPU128BIT	22	1	8	RP5312	RFBD<104>	53 52	53 55
FBD<105>	GPU128BIT	22	2	7	RP5312	RFBD<105>	53 52	53 55
FBD<106>	GPU128BIT	22	3	6	RP5312	RFBD<106>	53 52	53 55
FBD<107>	GPU128BIT	22	4	5	RP5312	RFBD<107>	53 52	53 55
FBD<108>	GPU128BIT	22	1	8	RP5313	RFBD<108>	53 52	53 55
FBD<109>	GPU128BIT	22	2	7	RP5313	RFBD<109>	53 52	53 55
FBD<110>	GPU128BIT	22	3	6	RP5313	RFBD<110>	53 52	53 55
FBD<111>	GPU128BIT	22	4	5	RP5313	RFBD<111>	53 52	53 55
FBD<112>	GPU128BIT	22	4	5	RP5311	RFBD<112>	53 52	53 55
FBD<113>	GPU128BIT	22	3	6	RP5311	RFBD<113>	53 52	53 55
FBD<114>	GPU128BIT	22	2	7	RP5311	RFBD<114>	53 52	53 55
FBD<115>	GPU128BIT	22	1	8	RP5311	RFBD<115>	53 52	53 55
FBD<116>	GPU128BIT	22	4	5	RP5306	RFBD<116>	53 52	53 55
FBD<117>	GPU128BIT	22	3	6	RP5306	RFBD<117>	53 52	53 55
FBD<118>	GPU128BIT	22	2	7	RP5306	RFBD<118>	53 52	53 55
FBD<119>	GPU128BIT	22	1	8	RP5306	RFBD<119>	53 52	53 55
FBD<120>	GPU128BIT	22	1	8	RP5304	RFBD<120>	53 52	53 55
FBD<121>	GPU128BIT	22	2	7	RP5304	RFBD<121>	53 52	53 55
FBD<122>	GPU128BIT	22	4	5	RP5304	RFBD<122>	53 52	53 55
FBD<123>	GPU128BIT	22	3	6	RP5304	RFBD<123>	53 52	53 55
FBD<124>	GPU128BIT	22	1	8	RP5305	RFBD<124>	53 52	53 55
FBD<125>	GPU128BIT	22	3	6	RP5305	RFBD<125>	53 52	53 55
FBD<126>	GPU128BIT	22	2	7	RP5305	RFBD<126>	53 52	53 55
FBD<127>	GPU128BIT	22	4	5	RP5305	RFBD<127>	53 52	53 55

FBDQS<8>	MAKE_BASE=TRUE	RFBDQS<8>	53 52 55
FBDQS<9>	MAKE_BASE=TRUE	RFBDQS<9>	53 52 55
FBDQS<10>	MAKE_BASE=TRUE	RFBDQS<10>	53 52 55
FBDQS<11>	MAKE_BASE=TRUE	RFBDQS<11>	53 52 55
FBDQS<12>	MAKE_BASE=TRUE	RFBDQS<12>	53 52 55
FBDQS<13>	MAKE_BASE=TRUE	RFBDQS<13>	53 52 55
FBDQS<14>	MAKE_BASE=TRUE	RFBDQS<14>	53 52 55
FBDQS<15>	MAKE_BASE=TRUE	RFBDQS<15>	53 52 55

55 53 52 FBBCLK0
R5324 56.2 1% 1/10W MF-LF 402
FBBCLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R5325 56.2 1% 1/10W MF-LF 402
C5325 0.01UF 20% 16V CERM 402
55 53 52 FBBCLK0_L

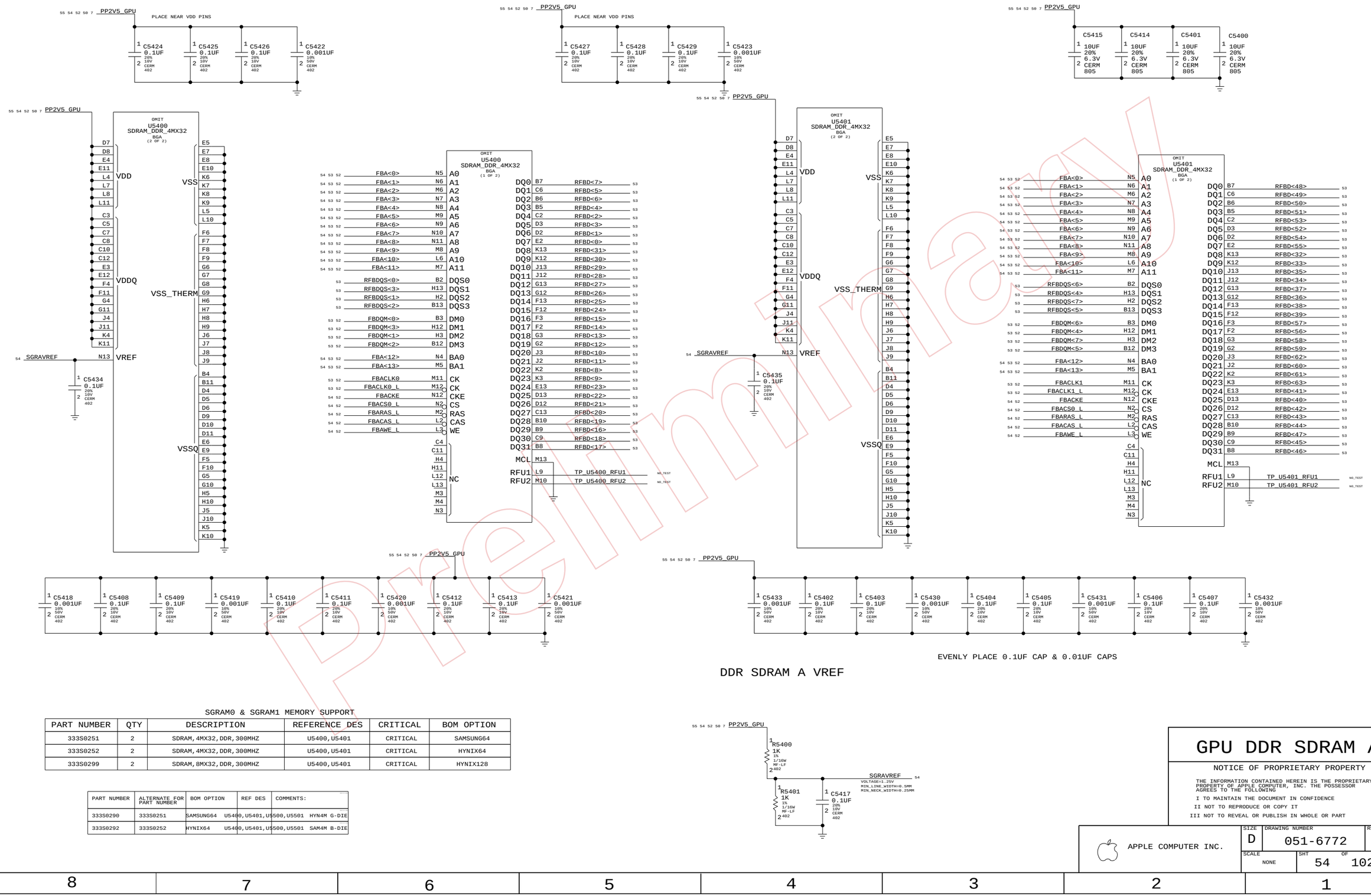
55 53 52 FBBCLK1
R5326 56.2 1% 1/10W MF-LF 402
FBBCLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R5327 56.2 1% 1/10W MF-LF 402
C5327 0.01UF 20% 16V CERM 402
55 53 52 FBBCLK1_L

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
53 52 FBD<127..0>		GPU_FB	GPU_FB		<434>
55 54 53 RFBD<127..0>		GPU_FB	GPU_FB		<435>
54 52 FBA<13..0>		GPU_FB	GPU_FB		<436>
55 52 FBBA<13..0>		GPU_FB	GPU_FB		<437>
55 54 52 FBDQM<15..0>		GPU_FB	GPU_FB		<438>
53 52 FBDQS<15..0>		GPU_FB	GPU_FB		<439>
54 53 52 FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0	<440>
54 53 52 FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0	<440>
54 53 52 FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1	<441>
54 53 52 FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1	<441>
55 53 52 FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0	<443>
55 53 52 FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0	<443>
55 53 52 FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1	<444>
55 53 52 FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1	<444>

FB TERMINATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 53 OF 102	



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX64
333S0299	2	SDRAM,8MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX128

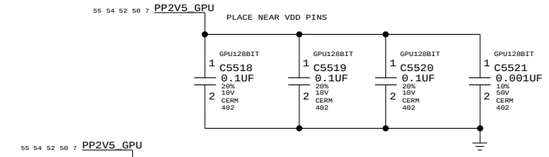
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0290	333S0251	SAMSUNG64	U5400,U5401,U5500,U5501	HYN4M G-DIE
333S0292	333S0252	HYNIX64	U5400,U5401,U5500,U5501	SAM4M B-DIE

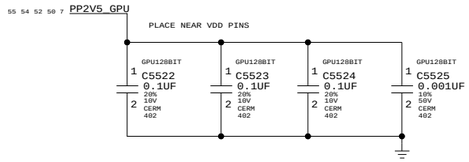
GPU DDR SDRAM A

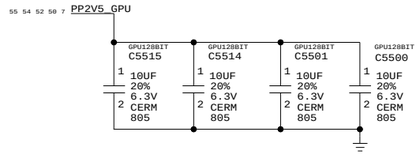
APPLE COMPUTER INC.

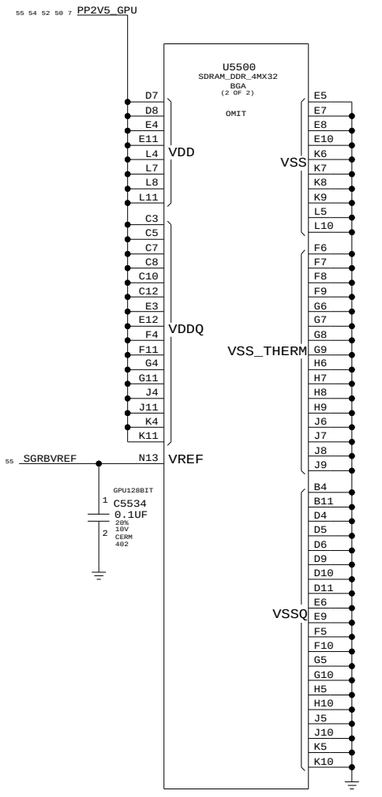
SIZE	DRAWING NUMBER	REV.
D	051-6772	04

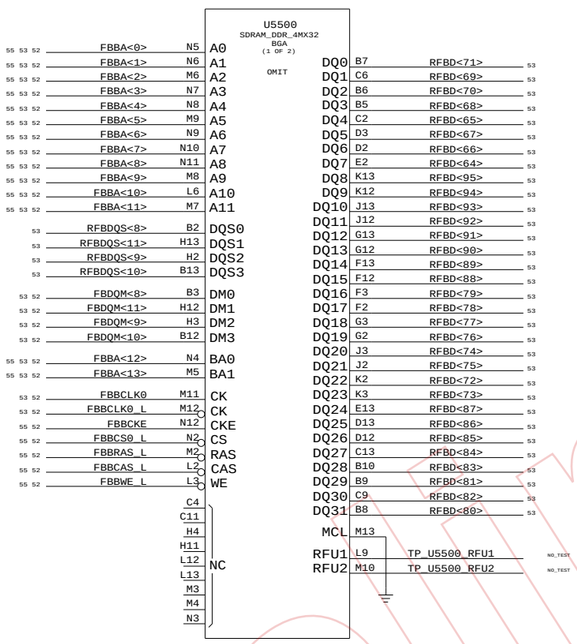
SCALE	SHT	OF
NONE	54	102

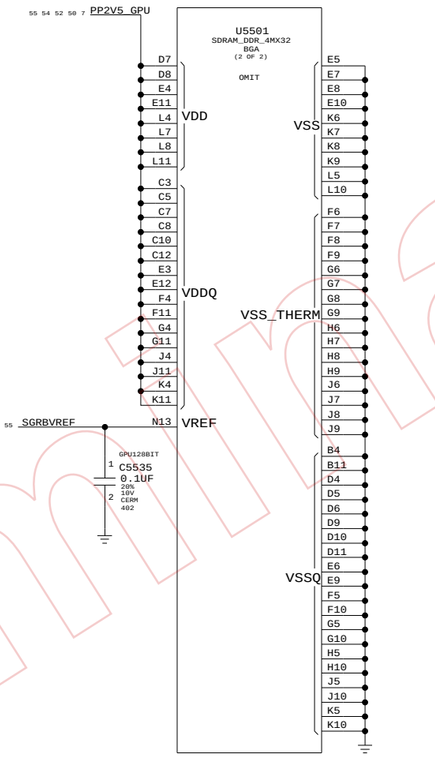


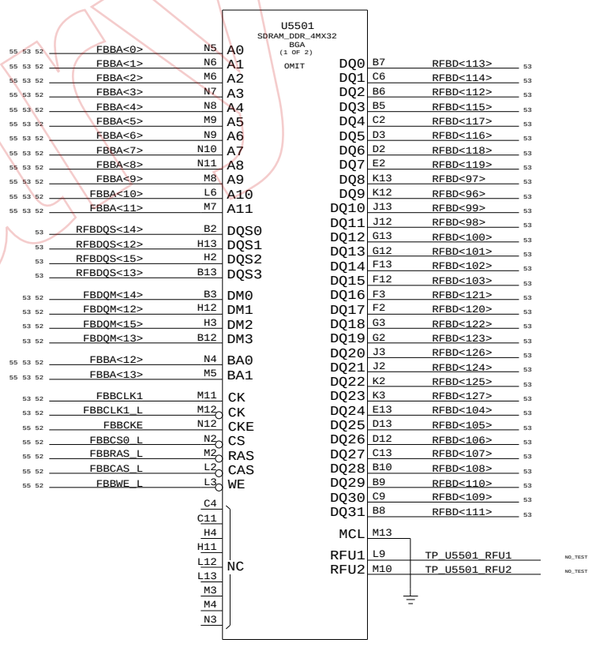


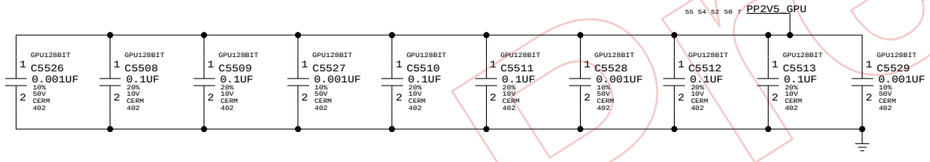




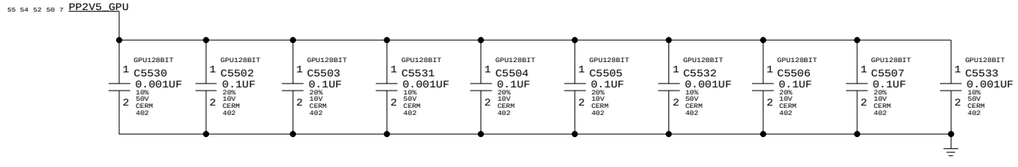




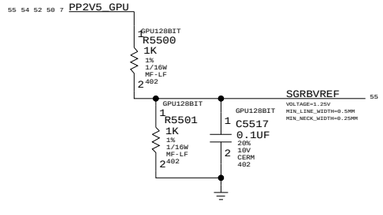




DDR SDRAM B VREF



EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	SAMSUNG64
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX64
333S0299	2	SDRAM,8MX32,DDR,300MHZ	U5500,U5501	CRITICAL	HYNIX128

GPU DDR SDRAM B

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

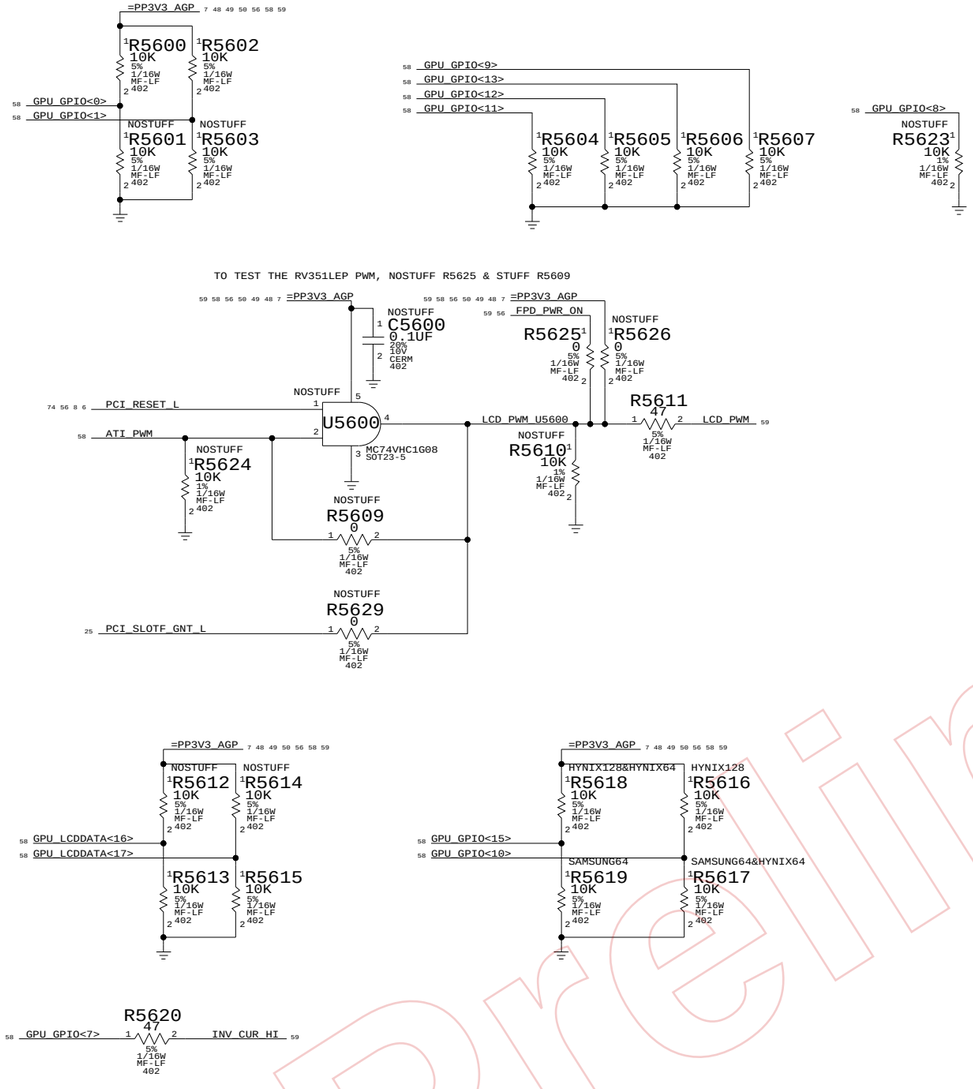
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 55 OF 102	



APPLE GPIO	ATI STRAP	PIN	DESCRIPTION	DEFAULT
	AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK) 00 - REFCLK SLIGHTLY EARLIER THEN FEEDBACK 01 - REFCLK 1 TAP EARLIER THEN FEEDBACK 10 - REFCLK 1 TAP LATER THEN FEEDBACK 11 - REFCLK 2 TAPS EARLIER THEN FEEDBACK CLOCK (ATI RECOMMENDED)	00 INTERNAL PULL-DOWN
	X1CLK_SKWE(1:0)	GPIO(3:2)	CLOCK PHASE ADJUSTMENT BETWEEN X1 CLK AND X2CLK 00 - 0 TAP DELAY	00 INTERNAL PULL-DOWN
	ROMIDCFG(3:0)	GPIO(9,13:11)	IF NO ROM ATTACHED, CONTROLS CHIP IDS. IF ROM- IDENTIFIES TYPE 0X0X - NO ROM, CHG_ID=0	
	ID_DISABLE	GPIO(8)	STRAP 0 - NORMAL OPERATION 1 - SHUTS THE CHIP DOWN BY NOT RESPONDING TO ANY CONFIG CYCLES	0 INTERNAL PULL-DOWN
	BUSCFG(2:0)	GPIO(6:4)	AGP8X_DETB: 0 — BUSCFG[2:0]: 000 — AGPMODE: AGP8X — SIGNALING: 0.8V — IDSEL: AD16	000 INTERNAL PULL-DOWN
	MULTIFUNC(1:0)	LCDDATA(17:16)	MULTI-FUNCTION DEVICE SELECT 00 - SINGLE FUNCTION DEVICE. 01 - TWO FUNCTION DEVICE. NO AGP IN EITHER FUNCTION 10 - TWO FUNCTION DEVICE. AGP ONLY IN FUNCTION 0 11 - TWO FUNCTION DEVICE. AGP IN BOTH FUNCTIONS IF BUSCFG PIN BASED STRAPS ARE SET TO PCI, THEN AGP WILL NOT BE ENABLED IN ANY FUNCTION.	00
	MEMSTRAP(1:0)	GPU_GPIO<15,10>	00 - SAMSUNG 4MX32 01 - UNDEFINED 10 - HYNIX 4MX32 11 - HYNIX 8MX32	
INV_CUR_HI		GPIO<7>	OUTPUT: GPU READS PANEL ID AND SETS THIS BIT ACCORDINGLY FOR REFERENCE ONLY, ACTIONS COME FROM BOOTROM SYSTEM / PANEL ID / INV_CUR_HI Q45 A / 0X9C27 / 1 0X9C38 / 0 Q45 B / 0X9C3A / 1 0X9C39 / 0 Q45 C / TBD / 1 TBD / 0 Q45 D / 0X9C3A / 1 Q45 A/B SUPPORT IS FOR DEVELOPMENT	
FPD_PWR_ON		GPIO<16>	OUTPUT: PANEL POWER SEQUENCING	
TMDS_EN		GPIO<14>	INPUT: PANEL POWER SEQUENCING	

GPU STRAPS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 56 OF 102	

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
ANALOG_GRN	GPU_VGA_37P5	GPU_VGA_37P5	
ANALOG_RED	GPU_VGA_37P5	GPU_VGA_37P5	
ANALOG_BLU	GPU_VGA_37P5	GPU_VGA_37P5	

=PP3V3_AGP

U4900 RV351 BGA (5 OF 5)

VDDR3 OMIT

0	AC19	
1	AC21	
2	AC22	
3	AC8	
4	AD19	
5	AD21	
6	AD22	
7	AD7	

VDDR4

8	AC10	
9	AC9	
10	AD10	
11	AD9	
12	AG7	

NOSTUFF C5800 10UF 20% 6.3V CERM 805; C5801 1UF 10% 6.3V CERM 402; C5802 1UF 10% 6.3V CERM 402; C5803 1UF 10% 6.3V CERM 402

GPIO

0	AJ5	GPU_GPIO<0>
1	AH5	GPU_GPIO<1>
2	AJ4	TP_GPU_GPIO<2>
3	AK4	TP_GPU_GPIO<3>
4	AH4	TP_GPU_GPIO<4>
5	AF4	TP_GPU_GPIO<5>
6	AJ3	TP_GPU_GPIO<6>
7	AK3	GPU_GPIO<7>
8	AH3	GPU_GPIO<8>
9	AJ2	GPU_GPIO<9>
10	AH2	GPU_GPIO<10>
11	AH1	GPU_GPIO<11>
12	AG3	GPU_GPIO<12>
13	AG1	GPU_GPIO<13>
14	AG2	GPU_GPIO<14>
15	AF3	GPU_GPIO<15>
16	AF2	GPU_GPIO<16>

EXTERNAL TMDS LCDDATA

0	AH6	TP_GPU_LCDDATA<0>
1	AJ6	TP_GPU_LCDDATA<1>
2	AK6	TP_GPU_LCDDATA<2>
3	AH7	TP_GPU_LCDDATA<3>
4	AK7	TP_GPU_LCDDATA<4>
5	AJ7	TP_GPU_LCDDATA<5>
6	AH8	TP_GPU_LCDDATA<6>
7	AJ8	TP_GPU_LCDDATA<7>
8	AH9	TP_GPU_LCDDATA<8>
9	AJ9	TP_GPU_LCDDATA<9>
10	AK9	TP_GPU_LCDDATA<10>
11	AH10	TP_GPU_LCDDATA<11>
12	AE6	TP_GPU_LCDDATA<12>
13	AG6	TP_GPU_LCDDATA<13>
14	AF6	TP_GPU_LCDDATA<14>
15	AE7	TP_GPU_LCDDATA<15>
16	AF7	GPU_LCDDATA<16>
17	AE8	GPU_LCDDATA<17>
18	AG8	TP_GPU_LCDDATA<18>
19	AF8	TP_GPU_LCDDATA<19>
20	AE9	TP_GPU_LCDDATA<20>
21	AF9	TP_GPU_LCDDATA<21>
22	AG10	TP_GPU_LCDDATA<22>
23	AF10	TP_GPU_LCDDATA<23>

LCDCNTL

0	AJ10	GPU_LCDCNTL<0>
1	AK10	GPU_LCDCNTL<1>
2	AJ11	GPU_LCDCNTL<2>
3	AH11	GPU_LCDCNTL<3>

DVOMODE AE10

HPD1 AF12 MON_DETECT_R

=PP3V3_AGP

RP5810 4.7K 5% 1/16W SM-LF; RP5810 4.7K 5% 1/16W SM-LF; RP5810 4.7K 5% 1/16W SM-LF; RP5810 4.7K 5% 1/16W SM-LF; R5818 10K 5% 1/16W MF-LF 402

R5819 0 5% 1/16W MF-LF 402

MON_DETECT

Y5800 SM-3 27.000M

C5814 22PF 5% 50V CERM 603; C5815 22PF 5% 50V CERM 603

R5815 0 5% 1/16W MF-LF 402

R5814 1M 5% 1/16W MF-LF 402

GPU_CLK27M_XOUT_R

XTALIN AH28 GPU_CLK27M_XIN

XTALOUT AJ29 GPU_CLK27M_XOUT

CLK

TEST

TEST_MCLK	B6	
TEST_YCLK	E8	
PLLTEST	NC	AE25
TESTEN		AH27

=PP3V3_AGP

R5816 1K 1% 1/16W MF-LF 402; R5817 1K 1% 1/16W MF-LF 402; C5817 0.1UF 20% 10V CERM 402

DPLUS AF11 GPU_DIODE_PLUS

DMINUS AE11 GPU_DIODE_MINUS

RSTB_MSK AG29

VREFG AG4 GPU_VREFG

MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

ATI_PWM

NC NO CONNECTS

NC	AF17	
	AF18	
	AG12	
	AG16	
	AG17	
	AG19	
	AG20	
	AH16	
	AH17	
	AH19	
	AH20	
	AH29	

NC

AE12	
AE18	
AH18	
AH30	
AJ16	
AJ17	
AJ18	
AJ25	
AK16	
AK19	
AF16	

THE FREQUENCY OF THE 20" PIXEL CLOCK IS 119 MHZ

TXVDDR AF13; TXVSSR AF14 AG13 AG14 AH12

TMDS

TXCP	AK13	TMDS_CKP
TXCM*	AH13	TMDS_CKM
TX0P	AH14	TMDS_D0P
TX0M*	AJ13	TMDS_D0M
TX1P	AH15	TMDS_D1P
TX1M*	AJ14	TMDS_D1M
TX2P	AK15	TMDS_D2P
TX2M*	AJ15	TMDS_D2M

TPVDD AK12 75MA MAX

TPVSS AJ12

DDC2CLK AE13 I2C_GPU_TMDS_SCL

DDC2DATA AE14 I2C_GPU_TMDS_SDA

VDD1DI AE24; VDD2DI AE22; VSS1DI AE23; VSS2DI AE21

DAC1

R	AK27	NC
G	AJ27	NC
B	AJ26	NC
HSYNC	AG25	NC
VSYNC	AH25	
RSET	AH26	
DDC1CLK	AF24	NC
DDC1DATA	AF25	NC
AUXWIN	AF26	NC
STEREOSYNC	AG26	

GPU_DAC1_VSYNC NO_TEST=TRUE

DEVELOPMENT R5826 75 1% 1/16W MF-LF 402

GPU_RSET

GPU_STEREOSYNC

R5825 10K 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

R5820 499 1% 1/16W MF-LF 402

XW5847 SM GND_GPU_AVSSQ

AVDD AH24; AVSSQ AD24 GND_GPU_AVSSQ; AVSSN AH23

A2VDD AG21 AH21; A2VSSN AH22 AJ21

DAC2

Y_G	AJ22	ANALOG_GRN
C_R	AJ23	ANALOG_RED
COMP_B	AK22	ANALOG_BLU
H2SYNC	AJ24	ANALOG_HSYNC
V2SYNC	AK24	ANALOG_VSYNC
R2SET	AK21	
DDC3CLK	AG23	I2C_GPU_MON_SCL
DDC3DATA	AG24	I2C_GPU_MON_SDA

ROUTE SIGNALS AT 37.5 OHMS

R5821 75 1% 1/16W MF-LF 402; R5822 75 1% 1/16W MF-LF 402; R5823 75 1% 1/16W MF-LF 402

PLACE R5821-3 & FL5900-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

A2VDDQ AF22; A2VSSQ AF23

GPU_R2SET MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

R5824 715 1% 1/16W MF-LF 402

=PP1V8_GPU

L5835 FERR-220-OHM 0805 — PP1V8_GPU_TXVDDR VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5835 10UF 20% 6.3V CERM 805; C5836 1UF 10% 6.3V CERM 402; C5837 0.1UF 20% 10V CERM 402

XW5835 SM — GND_GPU_TXVSSR VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF L5830 1.8UH 0805 — PP1V8_GPU_TPVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5830 10UF 20% 6.3V CERM 805; C5831 1UF 10% 6.3V CERM 402; C5832 0.1UF 20% 10V CERM 402; C5833 0.1UF 20% 10V CERM 402

XW5830 SM — GND_GPU_TPVSS VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5840 FERR-220-OHM 0805 — PP1V8_GPU_VDDDI VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5840 10UF 20% 6.3V CERM 805; C5841 1UF 10% 6.3V CERM 402

XW5840 SM — GND_GPU_VSSDI VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5845 FERR-220-OHM 0805 — PP1V8_GPU_AVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5845 10UF 20% 6.3V CERM 805; C5846 1UF 10% 6.3V CERM 402

XW5845 SM — GND_GPU_AVSSN VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

=PP2V5_GPU_A2VDD

NOSTUFF C5855 10UF 20% 6.3V CERM 805; C5856 1UF 10% 6.3V CERM 402

XW5855 SM — GND_GPU_A2VSSN VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

L5865 FERR-220-OHM 0805 — PP1V8_GPU_A2VDDQ VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

NOSTUFF C5865 10UF 20% 6.3V CERM 805; C5866 1UF 10% 6.3V CERM 402

XW5865 SM — GND_GPU_A2VSSQ VOLTAGE=0V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

GPU THERMAL SENSOR

PP3V3_PWRON

DEVELOPMENT C5890 0.1UF 20% 10V CERM 402; DEVELOPMENT C5891 100PF 5% 50V CERM 402; DEVELOPMENT R5891 10K 5% 1/16W MF-LF 402; DEVELOPMENT R5892 10K 5% 1/16W MF-LF 402

U5890 LM63CIMA SOI

VDD; DEVELOPMENT ALERT*/TACH — U5890_ALERT_L; PWM — U5890_PWM; SMBCLK — I2C_GPU_DIODE_SCL; SMBDA — I2C_GPU_DIODE_SDA; GND

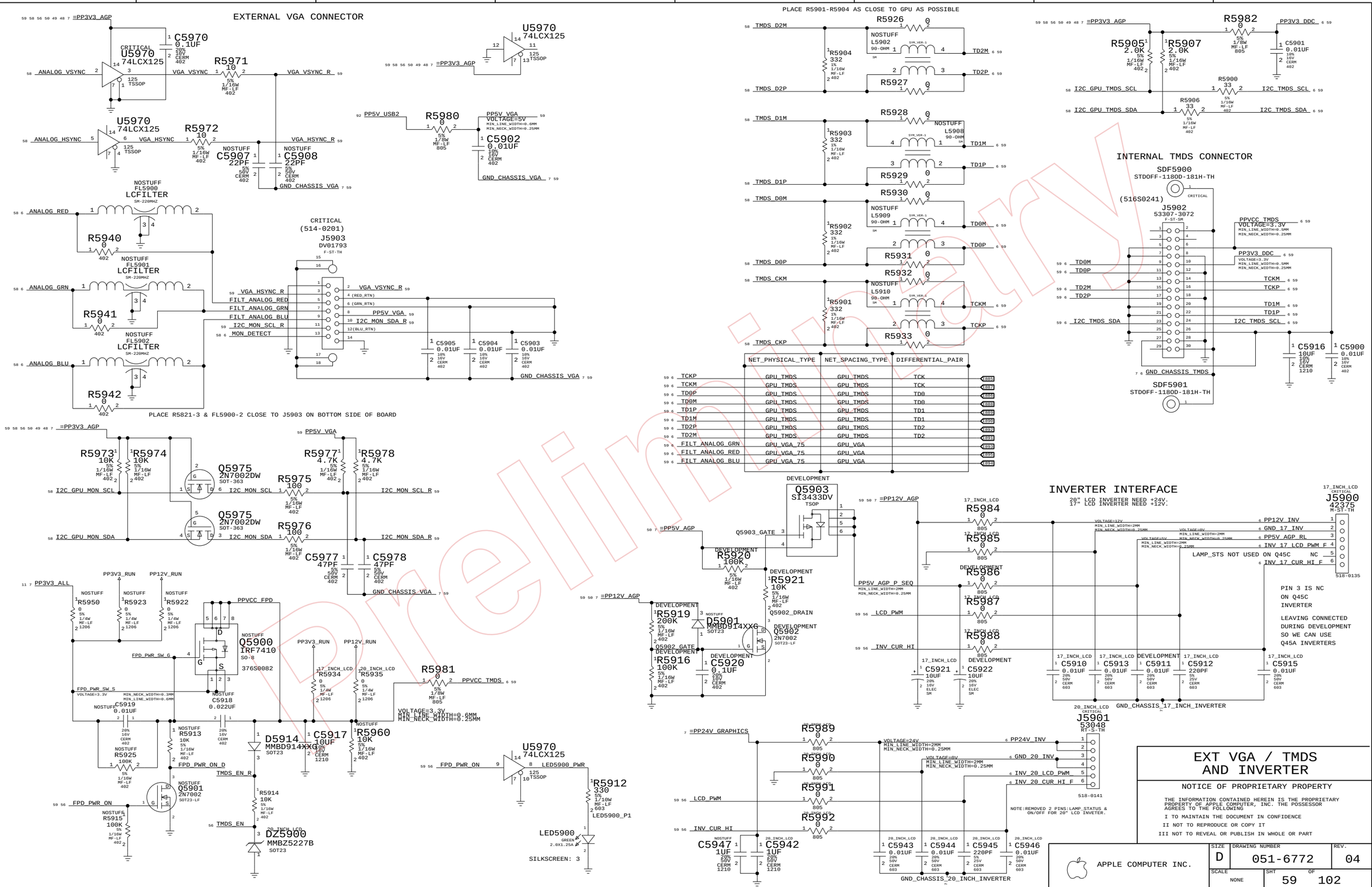
GPU_DIODE_PLUS — D+; GPU_DIODE_MINUS — D-

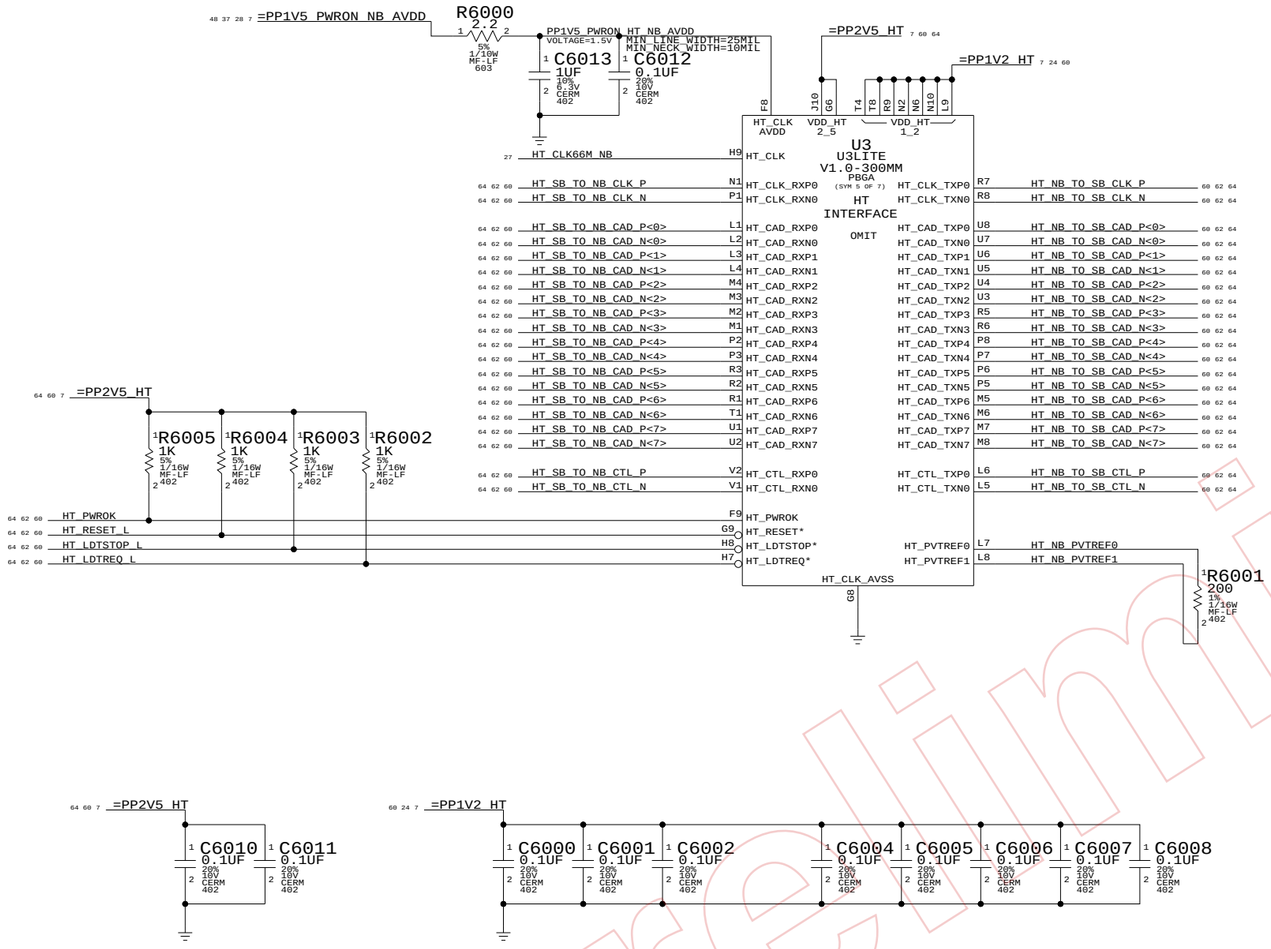
DEVELOPMENT C5892 2200PF 5% 50V CERM 603

GPU DVI & DACS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 58 OF 102	


EXTERNAL VGA CONNECTOR
=PP3V3_AGP
U5970
74LCX125
C5970
0.1UF
R5971
10
VGA_VSYNC
VGA_VSYNC_R
R5972
10
VGA_HSYNC
VGA_HSYNC_R
NOSTUFF
C5907
22PF
C5908
22PF
GND_CHASSIS_VGA
PP5V_USB2
R5980
0
PP5V_VGA
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
C5902
0.01UF
NOSTUFF
FL5900
LCFILTER
SM-220MHZ
ANALOG_RED
R5940
ANALOG_GRN
R5941
ANALOG_BLU
R5942
NOSTUFF
FL5901
NOSTUFF
FL5902
CRITICAL
(514-0201)
J5903
DV01793
F-ST-TH
VGA_HSYNC_R
VGA_VSYNC_R
FILT_ANALOG_RED
FILT_ANALOG_GRN
FILT_ANALOG_BLU
I2C_MON_SCL_R
I2C_MON_SDA_R
MON_DETECT
PP5V_VGA
C5905
0.01UF
C5904
0.01UF
C5903
0.01UF
GND_CHASSIS_VGA
PLACE R5821-3 & FL5900-2 CLOSE TO J5903 ON BOTTOM SIDE OF BOARD
R5973
10K
R5974
10K
Q5975
2N7002DW
SOT-363
I2C_GPU_MON_SCL
I2C_GPU_MON_SDA
I2C_MON_SCL
I2C_MON_SDA
R5975
100
R5976
100
R5977
4.7K
R5978
4.7K
C5977
47PF
C5978
47PF
PP3V3_ALL
PP3V3_RUN
PP12V_RUN
R5950
R5923
R5922
PPVCC_FPD
Q5900
IRF7410
SO-8
376S0082
FPD_PWR_SW_G
FPD_PWR_SW_S
C5919
0.01UF
C5918
0.022UF
R5925
100K
R5913
10K
D5914
MMBD914XXG
SOT23
C5917
10UF
R5960
10K
R5934
R5935
R5981
0
PPVCC_TMDS
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
Q5901
2N7002
SOT23-LF
FPD_PWR_ON
R5915
100K
TMDS_EN_R
R5914
10K
TMDS_EN
DZ5900
MMBZ5227B
SOT23
U5970
74LCX125
LED5900_PWR
R5912
330
LED5900_P1
LED5900
GREEN
2.0X1.25A
SILKSCREEN: 3
PLACE R5901-R5904 AS CLOSE TO GPU AS POSSIBLE
TMDS_D2M
TMDS_D2P
TMDS_D1M
TMDS_D1P
TMDS_D0M
TMDS_D0P
TMDS_CKM
TMDS_CKP
R5926
R5927
R5928
R5929
R5930
R5931
R5932
R5933
R5904
R5903
R5902
R5901
NOSTUFF
L5902
L5908
L5909
L5910
90-OHM
SYM_VER-1
TD2M
TD2P
TD1M
TD1P
TD0M
TD0P
TCKM
TCKP
NET_PHYSICAL_TYPE | NET_SPACING_TYPE | DIFFERENTIAL_PAIR
TCKP GPU_TMDS GPU_TMDS TCK
TCKM GPU_TMDS GPU_TMDS TCK
TD0P GPU_TMDS GPU_TMDS TD0
TD0M GPU_TMDS GPU_TMDS TD0
TD1P GPU_TMDS GPU_TMDS TD1
TD1M GPU_TMDS GPU_TMDS TD1
TD2P GPU_TMDS GPU_TMDS TD2
TD2M GPU_TMDS GPU_TMDS TD2
FILT_ANALOG_GRN GPU_VGA_75 GPU_VGA
FILT_ANALOG_RED GPU_VGA_75 GPU_VGA
FILT_ANALOG_BLU GPU_VGA_75 GPU_VGA
DEVELOPMENT
Q5903
SI3433DV
TSOP
Q5903_GATE
R5920
100K
R5921
10K
Q5902_DRAIN
R5919
200K
D5901
MMBD914XXG
SOT23
Q5902_GATE
R5916
100K
C5920
0.1UF
Q5902
2N7002
SOT23-LF
=PP12V_AGP
=PP5V_AGP
=PP24V_GRAPHICS
R5989
R5990
R5991
R5992
LCD_PWM
INV_CUR_HI
C5947
1UF
C5942
1UF
C5943
0.01UF
C5944
0.01UF
C5945
220PF
C5946
0.01UF
GND_CHASSIS_20_INCH_INVERTER
PP24V_INV
GND_20_INV
INV_20_LCD_PWM
INV_20_CUR_HI_F
NOTE:REMOVED 2 PINS:LAMP_STATUS & ON/OFF FOR 20" LCD INVETER.
R5982
0
PP3V3_DDC
C5901
0.01UF
R5905
2.0K
R5907
2.0K
R5900
33
R5906
33
I2C_GPU_TMDS_SCL
I2C_GPU_TMDS_SDA
I2C_TMDS_SCL
I2C_TMDS_SDA
INTERNAL TMDS CONNECTOR
SDF5900
STDOFF-118OD-181H-TH
(516S0241)
J5902
53307-3072
F-ST-SM
PPVCC_TMDS
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
PP3V3_DDC
TCKM
TCKP
TD1M
TD1P
TD2M
TD2P
TD0M
TD0P
I2C_TMDS_SDA
I2C_TMDS_SCL
C5916
10UF
C5900
0.01UF
GND_CHASSIS_TMDS
SDF5901
STDOFF-118OD-181H-TH
INVERTER INTERFACE
20" LCD INVERTER NEED +24V.
17" LCD INVERTER NEED +12V.
J5900
42375
M-ST-TH
518-0135
PP12V_INV
GND_17_INV
PP5V_AGP_RL
INV_17_LCD_PWM_F
INV_17_CUR_HI_F
LAMP_STS NOT USED ON Q45C
PIN 3 IS NC
ON Q45C
INVERTER
LEAVING CONNECTED
DURING DEVELOPMENT
SO WE CAN USE
Q45A INVERTERS
PP5V_AGP_P_SEQ
LCD_PWM
INV_CUR_HI
R5984
R5985
R5986
R5987
R5988
C5910
0.01UF
C5913
0.01UF
C5911
0.01UF
C5912
220PF
C5915
0.01UF
GND_CHASSIS_17_INCH_INVERTER
J5901
53048
RT-S-TH
518-0141
EXT VGA / TMDS AND INVERTER
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6772
REV. 04
SCALE NONE
SHT 59 OF 102



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5	HT_2V5		189

HT_NB_TO_SB HT_SB_TO_NB
5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5
4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE CAN BE LOOSE
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

MASTER: GILA
LAST MODIFIED: APR 12, 04

U3LITE HT

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 60 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	15 MIL SPACING	

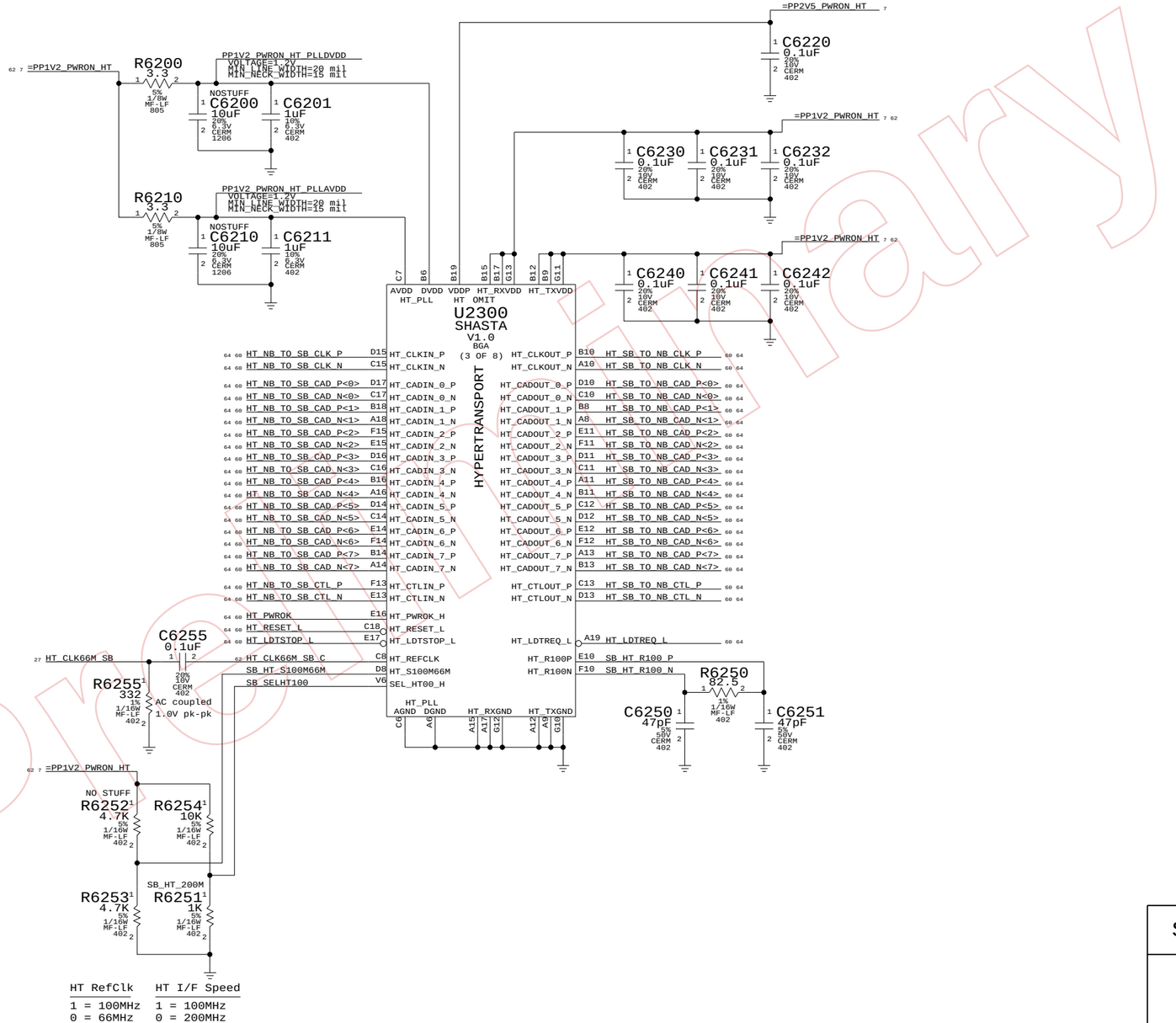
HT_CLK66M_SB_C 62

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



MASTER: SEEDY

Shasta HyperTransport

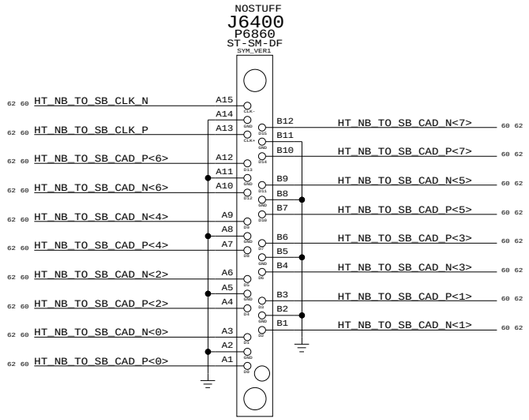
APPLE COMPUTER INC.

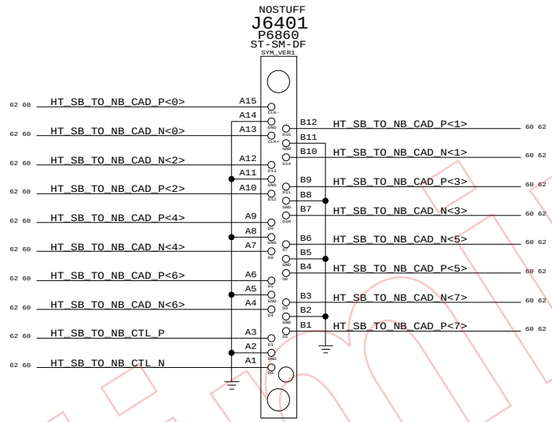
SIZE	DRAWING NUMBER	REV.
D	051-6772	04

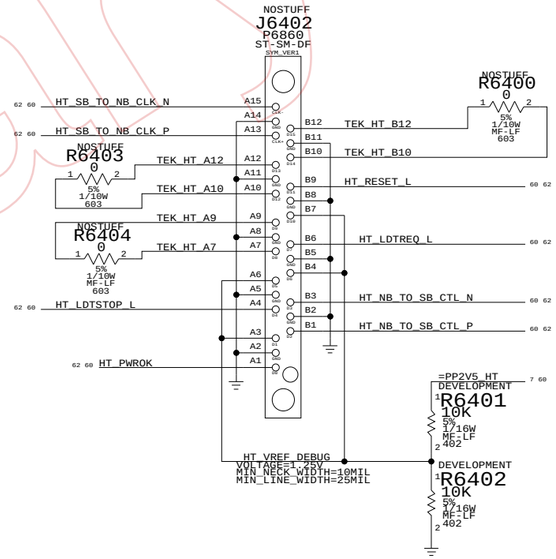
SCALE	SHT	OF
NONE	62	102

SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2







MASTER: GILA
LAST MODIFIED: APR 12, 04

HT DEBUG CONN

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT
NONE	64 OF 102

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

74	PCI_SB_AD<0>	RP7300	2	7	47	PCI_AD<0>	6 74 75 76 77
74	PCI_SB_AD<1>	RP7303	1	8	47	PCI_AD<1>	6 74 75 76 77
74	PCI_SB_AD<2>	RP7303	2	7	47	PCI_AD<2>	6 74 75 76 77
74	PCI_SB_AD<3>	RP7303	4	5	47	PCI_AD<3>	6 74 75 76 77
74	PCI_SB_AD<4>	RP7309	2	7	47	PCI_AD<4>	6 74 75 76 77
74	PCI_SB_AD<5>	RP7300	1	8	47	PCI_AD<5>	6 74 75 76 77
74	PCI_SB_AD<6>	RP7300	3	6	47	PCI_AD<6>	6 74 75 76 77
74	PCI_SB_AD<7>	RP7309	4	5	47	PCI_AD<7>	6 74 75 76 77
74	PCI_SB_AD<8>	RP7300	4	5	47	PCI_AD<8>	6 74 75 76 77
74	PCI_SB_AD<9>	RP7301	2	7	47	PCI_AD<9>	6 74 75 76 77
74	PCI_SB_AD<10>	RP7301	1	8	47	PCI_AD<10>	6 74 75 76 77
74	PCI_SB_AD<11>	RP7301	4	5	47	PCI_AD<11>	6 74 75 76 77
74	PCI_SB_AD<12>	RP7309	1	8	47	PCI_AD<12>	6 74 75 76 77
74	PCI_SB_AD<13>	RP7309	3	6	47	PCI_AD<13>	6 74 75 76 77
74	PCI_SB_AD<14>	RP7301	3	6	47	PCI_AD<14>	6 74 75 76 77
74	PCI_SB_AD<15>	RP7307	1	8	47	PCI_AD<15>	6 74 75 76 77
74	PCI_SB_AD<16>	RP7308	1	8	47	PCI_AD<16>	6 74 75 76 77

R7300
47
5%
1/16W
MF-LF
402

74	PCI_SB_AD<17>		1	2		PCI_AD<17>	6 74 75 76 77

74	PCI_SB_AD<18>	RP7307	2	7	47	PCI_AD<18>	6 74 75 76 77
74	PCI_SB_AD<19>	RP7306	3	6	47	PCI_AD<19>	6 74 75 76 77
74	PCI_SB_AD<20>	RP7305	1	8	47	PCI_AD<20>	6 74 75 76 77
74	PCI_SB_AD<21>	RP7305	2	7	47	PCI_AD<21>	6 74 76 77
74	PCI_SB_AD<22>	RP7302	1	8	47	PCI_AD<22>	6 74 76 77
74	PCI_SB_AD<23>	RP7302	3	6	47	PCI_AD<23>	6 74 76 77
74	PCI_SB_AD<24>	RP7304	1	8	47	PCI_AD<24>	6 74 75 76 77
74	PCI_SB_AD<25>	RP7306	4	5	47	PCI_AD<25>	6 74 75 76 77
74	PCI_SB_AD<26>	RP7305	3	6	47	PCI_AD<26>	6 74 75 76 77

R7301
47
5%
1/16W
MF-LF
402

74	PCI_SB_AD<27>		1	2		PCI_AD<27>	6 74 75 76 77

74	PCI_SB_AD<28>	RP7302	2	7	47	PCI_AD<28>	6 74 75 76 77
74	PCI_SB_AD<29>	RP7304	4	5	47	PCI_AD<29>	6 74 75 76 77
74	PCI_SB_AD<30>	RP7302	4	5	47	PCI_AD<30>	6 74 75 76 77
74	PCI_SB_AD<31>	RP7304	2	7	47	PCI_AD<31>	6 74 75 76 77
74	PCI_SB_CBE_L<0>	RP7303	3	6	47	PCI_CBE_L<0>	6 74 76 77
74	PCI_SB_CBE_L<1>	RP7306	2	7	47	PCI_CBE_L<1>	6 74 76 77
74	PCI_SB_CBE_L<2>	RP7305	4	5	47	PCI_CBE_L<2>	6 74 76 77
74	PCI_SB_CBE_L<3>	RP7304	3	6	47	PCI_CBE_L<3>	6 74 76 77
74	PCI_SB_DEVSEL_L	RP7306	1	8	47	PCI_DEVSEL_L	6 74 76 77
74	PCI_SB_FRAME_L	RP7307	4	5	47	PCI_FRAME_L	6 74 76 77
74	PCI_SB_IRDY_L	RP7307	3	6	47	PCI_IRDY_L	6 74 76 77
74	PCI_SB_TRDY_L	RP7308	3	6	47	PCI_TRDY_L	6 74 76 77
74	PCI_SB_STOP_L	RP7308	4	5	47	PCI_STOP_L	6 74 76 77
74	PCI_SB_PAR	RP7308	2	7	47	PCI_PAR	6 74 76 77

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT
NONE	73 OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_AD		PCI_AD<31..28>
PCI_AD27		PCI_AD<27>
PCI_AD		PCI_AD<26..24>
PCI_AD23		PCI_AD<23>
PCI_AD22		PCI_AD<22>
PCI_AD21		PCI_AD<21>
PCI_AD20		PCI_AD<20>
PCI_AD		PCI_AD<19..18>
PCI_AD17		PCI_AD<17>
PCI_AD		PCI_AD<16..0>
PCI		PCI_CBE_L<3..0>
PCI		PCI_PAR
PCI_CTL		PCI_DEVSEL_L
PCI_CTL		PCI_FRAME_L
PCI_CTL		PCI_IRDY_L
PCI_CTL		PCI_TRDY_L
PCI_CTL		PCI_STOP_L

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

=PP3V3_SB_PCI

NO_STUFF C7410 10uF 20% 6.3V CERM 805
C7400 0.1uF 20% 10V CERM 402
C7401 0.1uF 20% 10V CERM 402
C7402 0.1uF 20% 10V CERM 402
C7403 0.1uF 20% 10V CERM 402
C7404 0.1uF 20% 10V CERM 402

NO_STUFF C7411 10uF 20% 6.3V CERM 805
C7405 0.1uF 20% 10V CERM 402
C7406 0.1uF 20% 10V CERM 402
C7407 0.1uF 20% 10V CERM 402
C7408 0.1uF 20% 10V CERM 402
C7409 0.1uF 20% 10V CERM 402

=PP2V5_PWRON_SB

C7420 0.1uF 20% 10V CERM 402
C7421 0.1uF 20% 10V CERM 402
C7422 0.1uF 20% 10V CERM 402
C7423 0.1uF 20% 10V CERM 402

U2300 SHASTA V1.0 BGA (4 OF 8) OMIT

VDDOPC: AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19
PCIVDDP: B20 J18 N20 U20

PCI

PCI_CLK66M_SB_INT	AB9	PCIBR_CLK_H
PCI_CLK33M_SB_EXT	U19	PCI1CLK_H

"Slot A" - AD17
PCI_SLOTA_REQ_L AB18 PCI1REQ_0_L
PCI_SLOTA_GNT_L AA18 PCI1GNT_0_L

"Slot G" - AD27
PCI_SLOTG_REQ_L AB20 PCI1REQ_1_L
PCI_SLOTG_GNT_L AB19 PCI1GNT_1_L

"Slot D" - AD20
PCI_SLOTD_REQ_L V17 PCI1REQ_2_L
PCI_SLOTD_GNT_L V18 PCI1GNT_2_L

ROM_CS_L	AB8	ROMCS_L
ROM_OE_L	AA9	ROMOE_L
ROM_WE_L	Y10	ROMRW_L

PCI1AD_0_H	L18	PCI_SB_AD<0>
PCI1AD_1_H	K19	PCI_SB_AD<1>
PCI1AD_2_H	L22	PCI_SB_AD<2>
PCI1AD_3_H	M22	PCI_SB_AD<3>
PCI1AD_4_H	M18	PCI_SB_AD<4>
PCI1AD_5_H	L20	PCI_SB_AD<5>
PCI1AD_6_H	M21	PCI_SB_AD<6>
PCI1AD_7_H	N16	PCI_SB_AD<7>
PCI1AD_8_H	M20	PCI_SB_AD<8>
PCI1AD_9_H	P22	PCI_SB_AD<9>
PCI1AD_10_H	M17	PCI_SB_AD<10>
PCI1AD_11_H	N18	PCI_SB_AD<11>
PCI1AD_12_H	M19	PCI_SB_AD<12>
PCI1AD_13_H	N19	PCI_SB_AD<13>
PCI1AD_14_H	P21	PCI_SB_AD<14>
PCI1AD_15_H	R22	PCI_SB_AD<15>
PCI1AD_16_H	P20	PCI_SB_AD<16>
PCI1AD_17_H	V21	PCI_SB_AD<17>
PCI1AD_18_H	P18	PCI_SB_AD<18>
PCI1AD_19_H	T20	PCI_SB_AD<19>
PCI1AD_20_H	R16	PCI_SB_AD<20>
PCI1AD_21_H	R17	PCI_SB_AD<21>
PCI1AD_22_H	W21	PCI_SB_AD<22>
PCI1AD_23_H	Y22	PCI_SB_AD<23>
PCI1AD_24_H	R18	PCI_SB_AD<24>
PCI1AD_25_H	T19	PCI_SB_AD<25>
PCI1AD_26_H	T18	PCI_SB_AD<26>
PCI1AD_27_H	Y21	PCI_SB_AD<27>
PCI1AD_28_H	W20	PCI_SB_AD<28>
PCI1AD_29_H	T16	PCI_SB_AD<29>
PCI1AD_30_H	AA21	PCI_SB_AD<30>
PCI1AD_31_H	T17	PCI_SB_AD<31>
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L
PCI1FRAME_L	T21	PCI_SB_FRAME_L
PCI1IRDY_L	R21	PCI_SB_IRDY_L
PCI1TRDY_L	P19	PCI_SB_TRDY_L
PCI1STOP_L	P17	PCI_SB_STOP_L
PCI1PAR_H	N17	PCI_SB_PAR
PCI1RST_L	U18	SB_PCI_RESET_L

=PP3V3_PCI
RP7400 4.7K 5% 1/16W SM-LF: PCI_SLOTA_REQ_L
RP7400 4.7K 5% 1/16W SM-LF: PCI_SLOTA_GNT_L
RP7400 4.7K 5% 1/16W SM-LF: PCI_SLOTG_REQ_L
RP7400 4.7K 5% 1/16W SM-LF: PCI_SLOTG_GNT_L
RP7401 4.7K 5% 1/16W SM-LF: PCI_SLOTD_REQ_L
RP7401 4.7K 5% 1/16W SM-LF: PCI_SLOTD_GNT_L

=PP3V3_PWRON_SB
R7455 4.7K 5% 1/16W MF-LF 402
C7450 0.1uF 20% 10V CERM 402
R7450 4.7K 5% 1/16W MF-LF 402
U7450 NC74VHC1G08 SOT23-5

SYS_WARM_RESET_L
Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.
PCI_RESET_L

=PP3V3_PCI
RP7402 4.7K 5% 1/16W SM-LF: PCI_DEVSEL_L
RP7402 4.7K 5% 1/16W SM-LF: PCI_FRAME_L
RP7402 4.7K 5% 1/16W SM-LF: PCI_IRDY_L
RP7402 4.7K 5% 1/16W SM-LF: PCI_TRDY_L
RP7401 4.7K 5% 1/16W SM-LF: PCI_STOP_L

Master: Link

Shasta PCI Interface

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6772 | REV. 04
SCALE NONE | SHT 74 OF 102

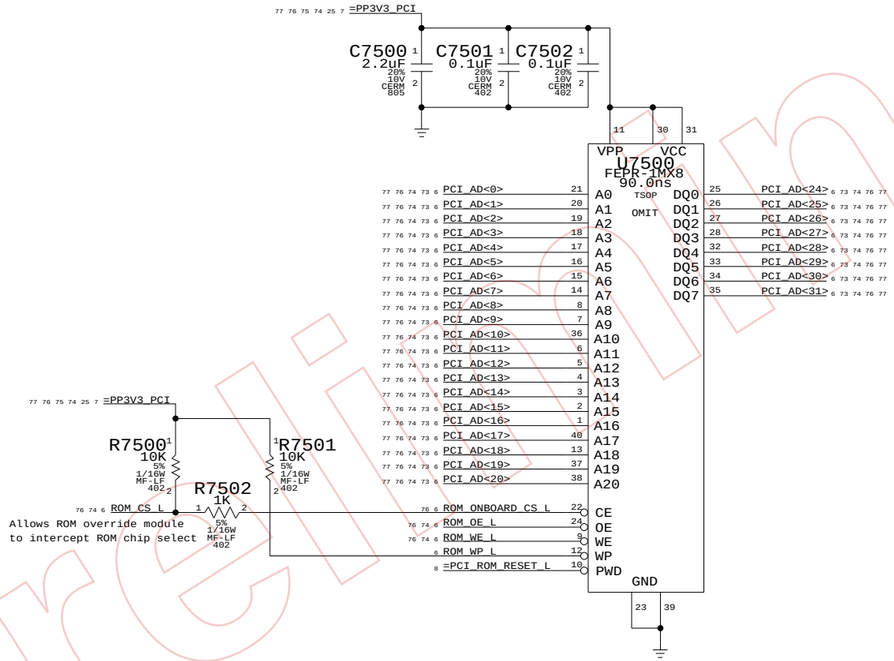
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



Master: Link

BootROM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 75 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

_PCI_CLK33M_AIRPORT 8 76

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR

77 75 74 25 7 =PP3V3_PCI

SDF7600
STDOFF-3MMOD5MMH-TH

NOSTUFF C7650 10UF 20% 6.3V CERM 1206
C7651 1UF 10% 6.3V CERM 402
C7652 1UF 10% 6.3V CERM 402

CRITICAL
J7650
20-5602-080-041-829
F-ST-SM

	1	2	PCI_AD<31> 6 73 74 75 77
77 75 74 73 6 PCI_AD<30>	3	4	AIRPORT_CLKRUN_L_PD 6
	5	6	TP_AP_PME_L
77 75 74 73 6 PCI_AD<27>	7	8	PCI_SLOTA_GNT_L 6 74
74 6 PCI_SLOTA_REQ_L	9	10	
77 75 74 73 6 PCI_AD<25>	11	12	
77 75 74 73 6 PCI_AD<29>	13	14	PCI_AD<24> 6 73 74 75 77
	15	16	PCI_AIRPORT_RESET_L 8
77 74 73 6 PCI_CBE_L<3>	17	18	PCI_AD<28> 6 73 74 75 77
77 75 74 73 6 PCI_AD<26>	19	20	
77 74 73 6 PCI_AD<22>	21	22	PCI_AD<23> 6 73 74 77
6 PCI_SLOTA_IDSEL	23	24	
	25	26	PCI_AD<20> 6 73 74 75 77
77 75 74 73 6 PCI_AD<19>	27	28	PCI_FRAME_L 6 73 74 77
77 74 73 6 PCI_AD<21>	29	30	PCI_AD<17> 6 73 74 75 76 77
77 74 73 6 PCI_IRDY_L	31	32	
77 75 74 73 6 PCI_AD<18>	33	34	PCI_TRDY_L 6 73 74 77
77 74 73 6 PCI_DEVSEL_L	35	36	
	37	38	PCI_CBE_L<2> 6 73 74 77
76 8 _PCI_CLK33M_AIRPORT	39	40	PCI_AD<16> 6 73 74 75 77
77 74 73 6 PCI_STOP_L	41	42	
77 75 74 73 6 PCI_AD<12>	43	44	
77 74 73 6 PCI_PAR	45	46	
	47	48	PCI_AD<14> 6 73 74 75 77
77 75 74 73 6 PCI_AD<8>	49	50	PCI_AD<13> 6 73 74 75 77
77 75 74 73 6 PCI_AD<9>	51	52	
77 74 73 6 PCI_CBE_L<0>	53	54	PCI_AD<10> 6 73 74 75 77
	55	56	PCI_AD<15> 6 73 74 75 77
77 75 74 73 6 PCI_AD<7>	57	58	AP_ALT_ANT
77 75 74 73 6 PCI_AD<3>	59	60	PCI_CBE_L<1> 6 73 74 77
77 75 74 73 6 PCI_AD<6>	61	62	PCI_AD<4> 6 73 74 75 77
	63	64	
77 75 74 73 6 PCI_AD<1>	65	66	PCI_AD<11> 6 73 74 75 77
77 75 74 73 6 PCI_AD<5>	67	68	ROM_WE_L 6 74 75
77 75 74 73 6 PCI_AD<0>	69	70	PCI_AD<2> 6 73 74 75 77
	71	72	
	73	74	PCI_SLOTA_INT_L 6 25
	75	76	ROM_OE_L 6 74 75
	77	78	ROM_ONBOARD_CS_L 6 75
7 _PP3V3_PWRON_BT	79	80	ROM_CS_L 6 74 75

516S0285

R7650 10K 5% 1/16W MF-LF 402

R7651 22 5% 1/16W MF-LF 402
77 76 75 74 73 6 PCI_AD<17>

91 USB2_P<4> ALIAS 6 USB_BT_P
91 USB2_N<4> ALIAS 6 USB_BT_N
MAKE_BASE=TRUE
MAKE_BASE=TRUE

R7660 15K 5% 1/16W MF-LF 402
R7661 15K 5% 1/16W MF-LF 402

7 _PP3V3_PWRON_BT
91 USB2_OC<4> ALIAS

C7660 1UF 10% 6.3V CERM 402

SDF7601
STDOFF-3MMOD5MMH-TH

AIRPORT & BLUETOOTH

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 76 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

=PCI_CLK33M_USB2 8 77

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

7 =PPVIO_PCI_USB2

C7703 0.1uF 20% 10V CERM 402 1 2

H1 H3 M4 C8 VDD_PCI

CRITICAL
U7700
NEC_UPD720101_USB2
FBGA

76 75 74 73 6 PCI_AD<0>	M5	AD0			
76 75 74 73 6 PCI_AD<1>	P5	AD1			
76 75 74 73 6 PCI_AD<2>	N5	AD2			
76 75 74 73 6 PCI_AD<3>	P4	AD3			
76 75 74 73 6 PCI_AD<4>	N4	AD4			
76 75 74 73 6 PCI_AD<5>	M3	AD5			
76 75 74 73 6 PCI_AD<6>	N3	AD6			
76 75 74 73 6 PCI_AD<7>	M1	AD7			
76 75 74 73 6 PCI_AD<8>	L2	AD8			
76 75 74 73 6 PCI_AD<9>	L1	AD9			
76 75 74 73 6 PCI_AD<10>	K2	AD10			
76 75 74 73 6 PCI_AD<11>	L3	AD11			
76 75 74 73 6 PCI_AD<12>	K1	AD12			
76 75 74 73 6 PCI_AD<13>	K3	AD13			
76 75 74 73 6 PCI_AD<14>	J2	AD14			
76 75 74 73 6 PCI_AD<15>	J1	AD15			
76 75 74 73 6 PCI_AD<16>	F2	AD16			
76 75 74 73 6 PCI_AD<17>	E3	AD17			
76 75 74 73 6 PCI_AD<18>	E1	AD18			
76 75 74 73 6 PCI_AD<19>	D3	AD19			
76 75 74 73 6 PCI_AD<20>	D1	AD20			
76 74 73 6 PCI_AD<21>	D2	AD21			
76 74 73 6 PCI_AD<22>	C2	AD22			
76 74 73 6 PCI_AD<23>	C1	AD23			
76 75 74 73 6 PCI_AD<24>	B4	AD24			
76 75 74 73 6 PCI_AD<25>	A4	AD25			
76 75 74 73 6 PCI_AD<26>	B5	AD26			
(PCI_AD<27>)	C4	AD27			
76 75 74 73 6 PCI_AD<28>	A5	AD28			
76 75 74 73 6 PCI_AD<29>	C5	AD29			
76 75 74 73 6 PCI_AD<30>	B6	AD30			
76 75 74 73 6 PCI_AD<31>	A6	AD31			
76 74 73 6 PCI_CBE_L<0>	M2	CBE0			
76 74 73 6 PCI_CBE_L<1>	J3	CBE1			
76 74 73 6 PCI_CBE_L<2>	F1	CBE2			
76 74 73 6 PCI_CBE_L<3>	C3	CBE3			
76 74 73 6 PCI_PAR	J4	PAR			
76 74 73 6 PCI_FRAME_L	F3	FRAME			
76 74 73 6 PCI_IRDY_L	F4	IRDY			
76 74 73 6 PCI_TRDY_L	G1	TRDY			
76 74 73 6 PCI_STOP_L	G3	STOP			
PCI_SLOTG_IDSEL	B3	IDSEL			
76 74 73 6 PCI_DEVSEL_L	G2	DEVSEL			
74 PCI_SLOTG_REQ_L	C6	REQ			
74 PCI_SLOTG_GNT_L	D6	GNT			
NEC_PERR_L_PU	H2	PERR			
NEC_SERR_L_PU	H1	SERR OD			
NEC_INTA_L	C7	INTA OD	IPD	NTEST1	M8 TP_NEC_NTEST1 6
NEC_INTB_L	B7	INTB OD	IPD	SMC	M7 TP_NEC_SMC 6
NEC_INTC_L	A7	INTC OD			
77 8 =PCI_CLK33M_USB2	A8	PCLK	IPD	TEB	N7 TP_NEC_TEB 6
			IPD	AMC	P7 TP_NEC_AMC 6
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)	IPD	TEST	L8 TP_NEC_TEST 6
NEC_CRUN_L_PD	N6	CRUN			
NEC_PME_L	D9	PME OD			
NEC_VCCRST_L	C9	VCCRST(PCI RESET)			
6 TP_NEC_SMI_L	L6	SMI OD	NANDTEST		M10 TP_NEC_NANDTEST 6
				SRCLK	M9 TP_NEC_SRCLK 6
NEC_LEGC_PD	L7	LEGC		SRDTA	N9 TP_NEC_SRDATA 6
			IPD	SRMOD	P9 TP_NEC_SRMOD 6

R7714 22 5% 1/16W MF-LF 402

76 75 74 25 7 =PP3V3_PCI

R7716 10K 5% 1/16W MF-LF 402

R7713 10K 5% 1/16W MF-LF 402

25 PCI_SLOTG_INT_L

RP7703 47 5% 1/16W SM-LF

RP7703 47 5% 1/16W SM-LF

RP7703 47 5% 1/16W SM-LF

74 25 8 SYS_WARM_RESET_L

RP7702 47 5% 1/16W SM-LF

25 13 SYS_PME_L

RP7702 47 5% 1/16W SM-LF

8 =PCI_USB2_RESET_L

RP7702 47 5% 1/16W SM-LF

RP7702 & RP7703 required to facilitate NAND-tree testing

R7715 4.7K 5% 1/16W MF-LF 402

RP7703 47 5% 1/16W SM-LF

USB 2.0 PCI Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 77 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C 80 83
SATA_RXD1	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C 80 83
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_P1 80 83
SATA_TXD1	SATA	SATA	SATA_TXD1	SATA_TXD_N1 80 83
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C 80 83
SATA_RXD2	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C 80 83
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_P2 80 83
SATA_TXD2	SATA	SATA	SATA_TXD2	SATA_TXD_N2 80 83
UATA_DD				UATA_DD<15..8> 6 80 83
UATA_DD7				UATA_DD<7> 6 80 83
UATA_DD				UATA_DD<6..0> 6 80 83
UATA_HOST				UATA_DA<2..0> 6 80 83
UATA_HOST				UATA_CS0_L 6 80 83
UATA_HOST				UATA_CS1_L 6 80 83
UATA_HOST				UATA_HSTROBE 6 80 83
UATA_HOST				UATA_STOP 6 80 83
UATA_HOST_R				UATA_DMACK_L 6 80 83
UATA_HOST_R				UATA_RESET_L 6 80 83
UATA_DEV_R_C				UATA_DSTROBE 80 83
UATA_DEV_R				UATA_DMARQ 80 83
UATA_DEV_R				UATA_INTRQ 80 83

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

=PP1V2_PWRON_DISK_SB

SATA_VDD x 5

C8000 0.1uF 20% 10V CERM 402
C8001 0.1uF 20% 10V CERM 402
C8002 0.1uF 20% 10V CERM 402
C8003 0.1uF 20% 10V CERM 402
C8004 0.1uF 20% 10V CERM 402

AB14 AB17 T14 W15 Y18 SATA_VDD

U2300 OMIT
SHASTA
V1.0
BGA
(5 OF 8)

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>
UD_IDEDD_1_H	H7	UATA_DD_R<1>
UD_IDEDD_2_H	H6	UATA_DD_R<2>
UD_IDEDD_3_H	E2	UATA_DD_R<3>
UD_IDEDD_4_H	C1	UATA_DD_R<4>
UD_IDEDD_5_H	C2	UATA_DD_R<5>
UD_IDEDD_6_H	E3	UATA_DD_R<6>
UD_IDEDD_7_H	G6	UATA_DD_R<7>
UD_IDEDD_8_H	G5	UATA_DD_R<8>
UD_IDEDD_9_H	D4	UATA_DD_R<9>
UD_IDEDD_10_H	G7	UATA_DD_R<10>
UD_IDEDD_11_H	F6	UATA_DD_R<11>
UD_IDEDD_12_H	C3	UATA_DD_R<12>
UD_IDEDD_13_H	F5	UATA_DD_R<13>
UD_IDEDD_14_H	E5	UATA_DD_R<14>
UD_IDEDD_15_H	D5	UATA_DD_R<15>
UD_IDEDA0_H	E6	UATA_DA_R<0>
UD_IDEDA1_H	C4	UATA_DA_R<1>
UD_IDEDA2_H	D6	UATA_DA_R<2>
UD_IDECS1FX_L	B3	UATA_CS0_L_R
UD_IDECS3FX_L	B4	UATA_CS1_L_R
UD_IDEDMACK_L	E8	UATA_DMACK_L_R
UD_IDERD_L	E4	UATA_HSTROBE_R
UD_IDEWR_L	D3	UATA_STOP_R
UD_IDERST_L	E7	UATA_RESET_L_R
UD_IDECHRDY_H	F9	UATA_DSTROBE
UD_IDEDMARQ_H	D7	UATA_DMARQ
UD_IDEINTRQ_H	C5	UATA_INTRQ

DSTROBE aka: IORDY/HDMARDY*
HSTROBE aka: DIOR*
STOP aka: DIOW*

SATA 0

RXDP1	SATA_RXD_P1_C	Y17	TXDP1 AA16 SATA_TXD_P1
RXDN1	SATA_RXD_N1_C	Y16	TXDN1 AB16 SATA_TXD_N1

SATA 1

RXDP2	SATA_RXD_P2_C	AB15	TXDP2 Y15 SATA_TXD_P2
RXDN2	SATA_RXD_N2_C	AA15	TXDN2 Y14 SATA_TXD_N2

SATA_GND
AA14 AA17 T13 W16

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

UATA Termination

R8005 10K 5% 1/16W MF-LF 402

RP8000 33 5% 1/16W SM-LF	UATA_DD_R<0>	UATA_DD<0>
RP8000 33 5% 1/16W SM-LF	UATA_DD_R<1>	UATA_DD<1>
RP8000 33 5% 1/16W SM-LF	UATA_DD_R<2>	UATA_DD<2>
RP8003 33 5% 1/16W SM-LF	UATA_DD_R<3>	UATA_DD<3>
RP8001 33 5% 1/16W SM-LF	UATA_DD_R<4>	UATA_DD<4>
RP8001 33 5% 1/16W SM-LF	UATA_DD_R<5>	UATA_DD<5>
RP8003 33 5% 1/16W SM-LF	UATA_DD_R<6>	UATA_DD<6>
RP8002 33 5% 1/16W SM-LF	UATA_DD_R<7>	UATA_DD<7>
RP8002 33 5% 1/16W SM-LF	UATA_DD_R<8>	UATA_DD<8>
RP8003 33 5% 1/16W SM-LF	UATA_DD_R<9>	UATA_DD<9>
RP8000 33 5% 1/16W SM-LF	UATA_DD_R<10>	UATA_DD<10>
RP8002 33 5% 1/16W SM-LF	UATA_DD_R<11>	UATA_DD<11>
RP8001 33 5% 1/16W SM-LF	UATA_DD_R<12>	UATA_DD<12>
RP8002 33 5% 1/16W SM-LF	UATA_DD_R<13>	UATA_DD<13>
RP8004 33 5% 1/16W SM-LF	UATA_DD_R<14>	UATA_DD<14>
RP8003 33 5% 1/16W SM-LF	UATA_DD_R<15>	UATA_DD<15>
RP8004 33 5% 1/16W SM-LF	UATA_DA_R<0>	UATA_DA<0>
RP8001 33 5% 1/16W SM-LF	UATA_DA_R<1>	UATA_DA<1>
RP8004 33 5% 1/16W SM-LF	UATA_DA_R<2>	UATA_DA<2>
RP8004 33 5% 1/16W SM-LF	UATA_RESET_L_R	UATA_RESET_L
R8000 33 5% 1/16W MF-LF 402	UATA_CS0_L_R	UATA_CS0_L
R8001 33 5% 1/16W MF-LF 402	UATA_CS1_L_R	UATA_CS1_L
R8002 22 5% 1/16W MF-LF 402	UATA_HSTROBE_R	UATA_HSTROBE
R8003 22 5% 1/16W MF-LF 402	UATA_STOP_R	UATA_STOP
R8004 22 5% 1/16W MF-LF 402	UATA_DMACK_L_R	UATA_DMACK_L

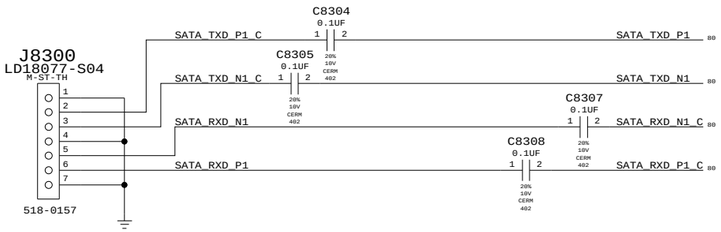
Shasta Disk

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 80 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
UATA_DD<15..8>	UATA_DD		
UATA_DD<7>	UATA_DD7		
UATA_DD<6..0>	UATA_DD		
UATA_DA<2..0>	UATA_HOST		
UATA_CS0_L	UATA_HOST		
UATA_CS1_L	UATA_HOST		
UATA_HSTROBE	UATA_HOST		
UATA_STOP	UATA_HOST		
UATA_DMACK_L	UATA_HOST_R		
UATA_RESET_L	UATA_HOST_R		
UATA_DSTROBE	UATA_DEV_R_C		
UATA_DMARQ	UATA_DEV_R		
UATA_INTRQ	UATA_DEV_R		

SATA CONNECTORS



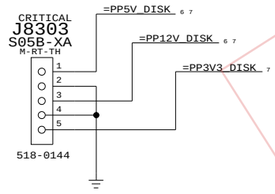
SATA_TXD_P2 80 — TP_SATA_TXD_P2 MAKE_BASE=TRUE

SATA_TXD_N2 80 — TP_SATA_TXD_N2 MAKE_BASE=TRUE

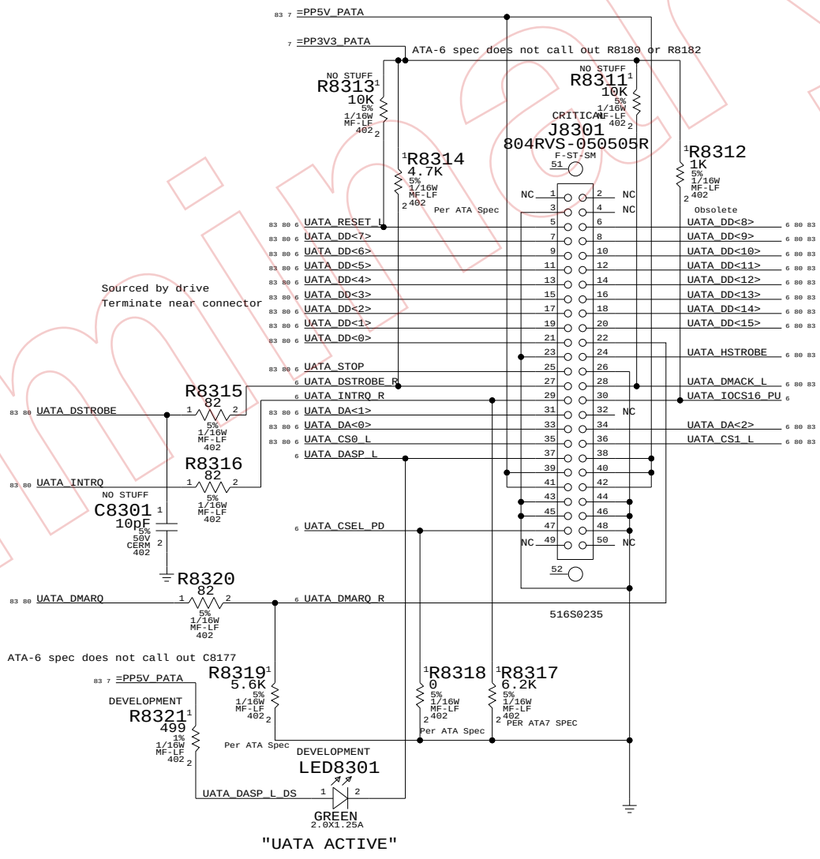
80 SATA_RXD_N2_C — 80 TP_SATA_RXD_N2_C MAKE_BASE=TRUE

80 SATA_RXD_P2_C — 80 TP_SATA_RXD_P2_C MAKE_BASE=TRUE

HD POWER



PATA CONNECTOR



DISK CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT: 83	OF: 102

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
ENET_RX_CLK		P25MM	
ENET_RX_CLK		P25MM	
ENET_GBE_REF		P25MM	
ENET_TX_CLK		P25MM	
ENET_RX			
ENET_RX_CTL			
ENET_RX_CTL			
ENET_TX			
ENET_TX_CTL			
ENET_TX_CTL			
ENET_RX_CTL			
ENET_RX_CTL			
ENET_MDC			
ENET_MDIO			

ENET_CLK25M_TX 84 86
ENET_CLK125M_RX 84 86
ENET_CLK125M_GBE_REF 84 86
ENET_CLK125M_GTX 84 86
ENET_CLK125M_GTX_R 84
ENET_RXD<7..0> 84 86
ENET_RX_DV 84 86
ENET_RX_ER 84 86
ENET_TXD<7..0> 84 86
ENET_TX_EN 84 86
ENET_TX_ER 84 86
ENET_CRS 84 86
ENET_COL 84 86
ENET_MDC 84 86
ENET_MDIO 84 86

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT

U2300
SHASTA
V1.0
BGA
(6 OF 8)

ETHERNET

86 84 ENET_CLK25M_TX	H5	ETH_TX_CLK_H			
86 84 ENET_CLK125M_RX	J3	ETH_RX_CLK_H			
86 84 ENET_RXD<0>	K1	ETH_RXD_0_H	ETH_TXD_0_H	G4	ENET_TXD_R<0>
86 84 ENET_RXD<1>	L3	ETH_RXD_1_H	ETH_TXD_1_H	E1	ENET_TXD_R<1>
86 84 ENET_RXD<2>	K2	ETH_RXD_2_H	ETH_TXD_2_H	H4	ENET_TXD_R<2>
86 84 ENET_RXD<3>	J1	ETH_RXD_3_H	ETH_TXD_3_H	J5	ENET_TXD_R<3>
86 84 ENET_RXD<4>	L4	ETH_RXD_4_H	ETH_TXD_4_H	G3	ENET_TXD_R<4>
86 84 ENET_RXD<5>	K3	ETH_RXD_5_H	ETH_TXD_5_H	F2	ENET_TXD_R<5>
86 84 ENET_RXD<6>	J2	ETH_RXD_6_H	ETH_TXD_6_H	J4	ENET_TXD_R<6>
86 84 ENET_RXD<7>	G1	ETH_RXD_7_H	ETH_TXD_7_H	K6	ENET_TXD_R<7>
86 84 ENET_RX_DV	K4	ETH_RX_DV_H	ETH_TX_EN_H	H3	ENET_TX_EN_R
86 84 ENET_RX_ER	G2	ETH_RX_ER_H	ETH_TX_ER_H	F1	ENET_TX_ER_R
86 84 ENET_CLK125M_GBE_REF	M5	ETH_REFCLK_H	ETH_GTX_CLK_H	K5	84 ENET_CLK125M_GTX_R
86 84 ENET_CRS	L6	ETH_CRS_H	ETH_MDC_H	M4	ENET_MDC 84 86
86 84 ENET_COL	L5	ETH_COL_H	ETH_MDIO_H	M6	ENET_MDIO 84 86

RP8400 0 — 2 — 7 — 5% 1/16W SM-LF — ENET_TXD<0> 84 86
RP8400 0 — 4 — 5 — 5% 1/16W SM-LF — ENET_TXD<1> 84 86
RP8400 0 — 1 — 8 — 5% 1/16W SM-LF — ENET_TXD<2> 84 86
RP8400 0 — 3 — 6 — 5% 1/16W SM-LF — ENET_TXD<3> 84 86
RP8401 0 — 2 — 7 — 5% 1/16W SM-LF — ENET_TXD<4> 84 86
RP8401 0 — 4 — 5 — 5% 1/16W SM-LF — ENET_TXD<5> 84 86
RP8401 0 — 1 — 8 — 5% 1/16W SM-LF — ENET_TXD<6> 84 86
RP8401 0 — 3 — 6 — 5% 1/16W SM-LF — ENET_TXD<7> 84 86
R8400 0 — 1 — 2 — 5% 1/16W MF-LF 402 — ENET_TX_EN 84 86
R8401 0 — 1 — 2 — 5% 1/16W MF-LF 402 — ENET_TX_ER 84 86
R8402 0 — 1 — 2 — 5% 1/16W MF-LF 402 — ENET_CLK125M_GTX 84 86

Master: Link

Shasta Ethernet

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 84 OF 102	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	P25MM			ENET_CLK125M_GBE_REF_R
	P25MM			ENET_CLK125M_RX_R
	P25MM			ENET_CLK25M_TX_R
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_P<0>
ENET_MDI	ENET	ENET	ENET_MDI0	ENET_MDI_N<0>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_P<1>
ENET_MDI	ENET	ENET	ENET_MDI1	ENET_MDI_N<1>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_P<2>
ENET_MDI	ENET	ENET	ENET_MDI2	ENET_MDI_N<2>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_P<3>
ENET_MDI	ENET	ENET	ENET_MDI3	ENET_MDI_N<3>
VESTA_CLK25M_XTALI	P25MM			VESTA_CLK25M_XTALI
	P25MM			VESTA_CLK25M_XTALO
	P25MM			VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- _PP3V3_ENET
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38 mms
Length Tolerance: 50 mils
Primary Max Sep: 5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

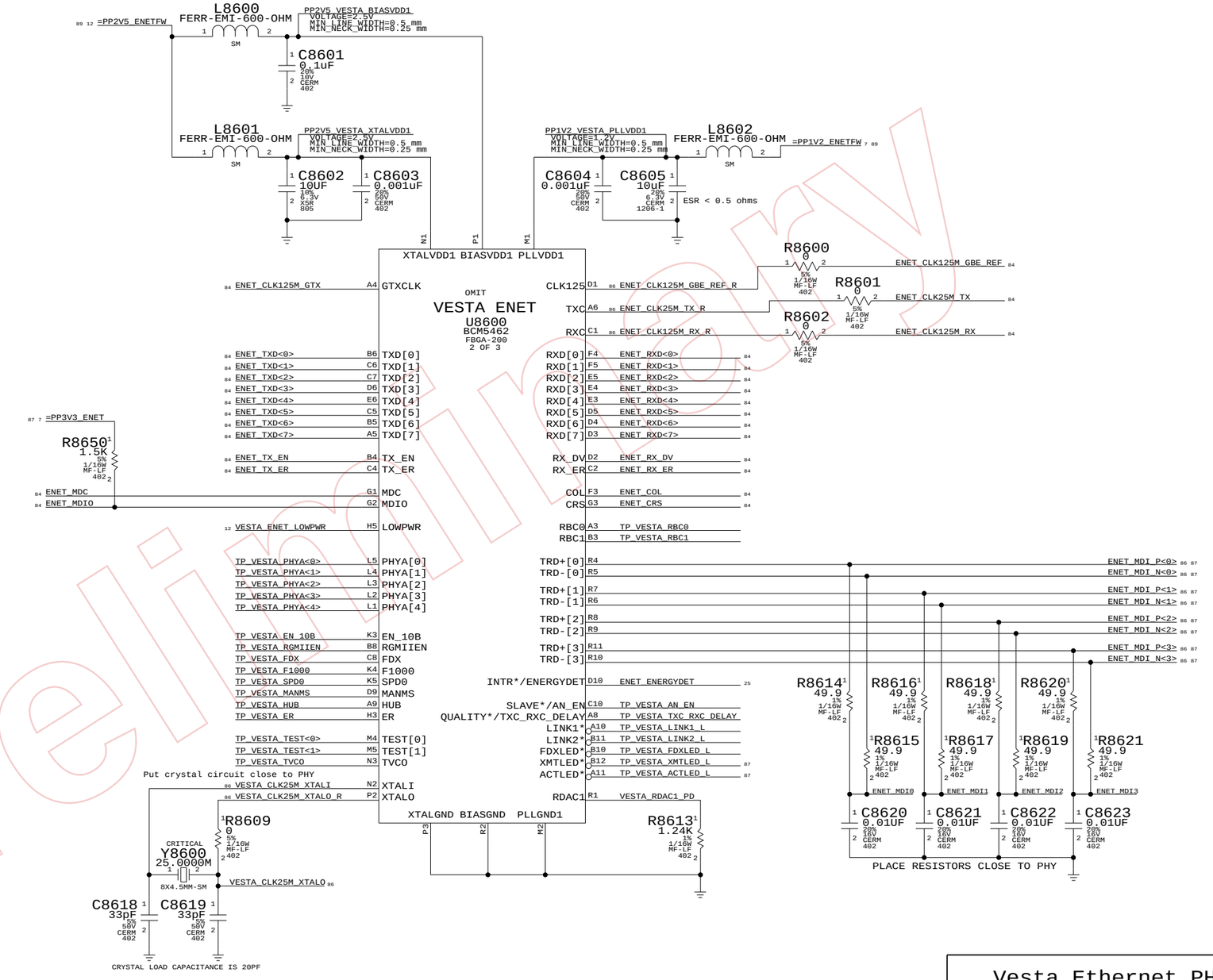
HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T



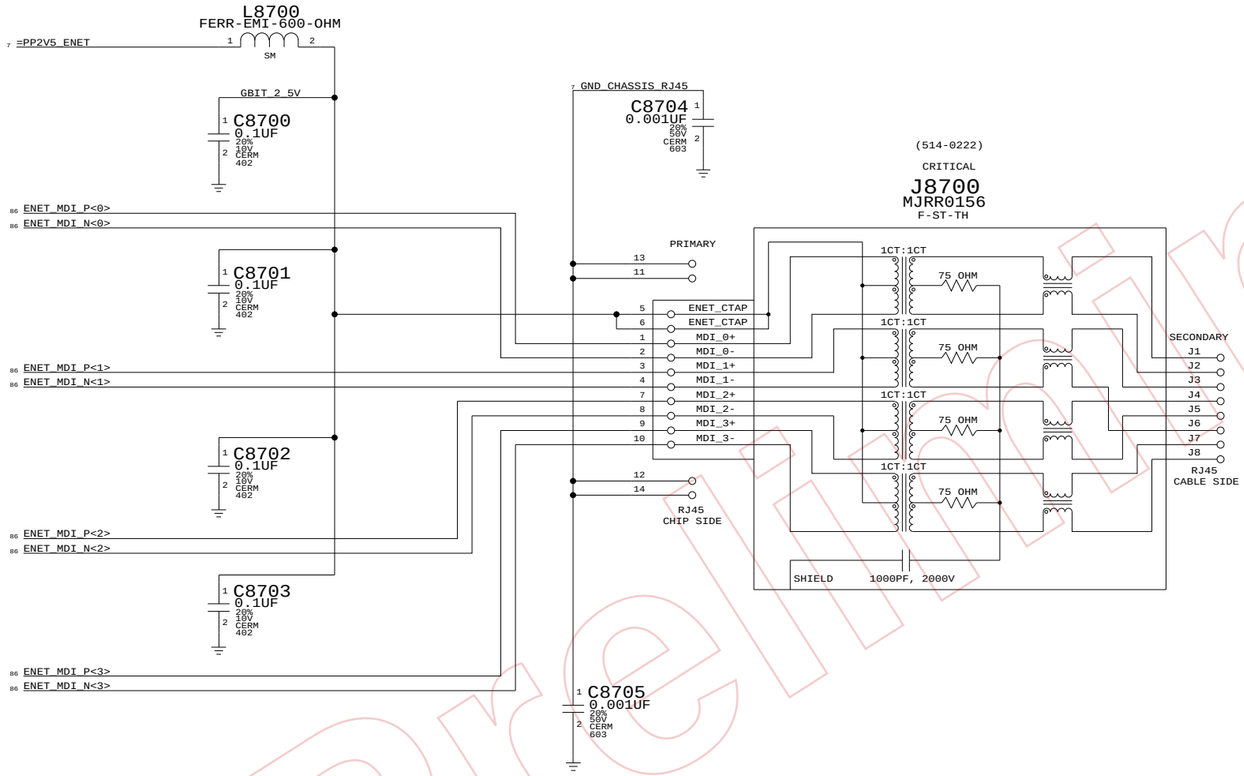
Vesta Ethernet PHY

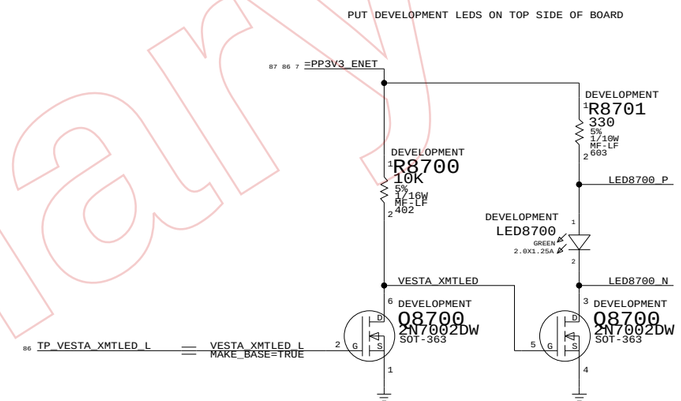
NOTICE OF PROPRIETARY PROPERTY

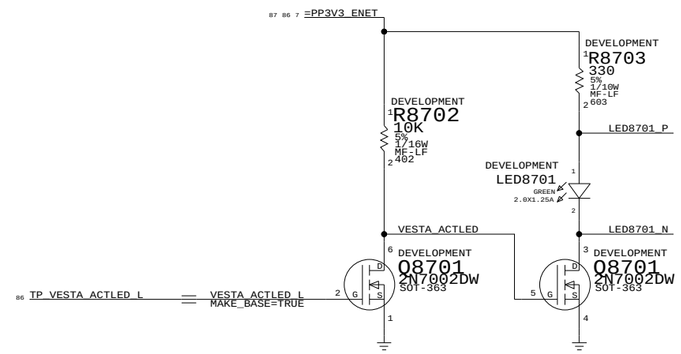
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 86 OF 102	







ETHERNET CONNECTOR

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 87 OF 102	

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FW			
FW			
FW_LPS			
FW_LREQ			
FW_PINT			
FW_LCLK		15_MIL_SPACING	
FW_PCLK		15_MIL_SPACING	
		15_MIL_SPACING	

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

74 25 23 7 =PP2V5_PWRON_SB

C8800 0.1uF 20% 10V CERM 402
C8801 0.1uF 20% 10V CERM 402
C8802 0.1uF 20% 10V CERM 402

U2300 OMIT
SHASTA
V1.0
BGA
(7 OF 8)
FWVDDP: N5, J7, A4

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	88 89
PHY_DATA_1_H	P5	FW_DATA<1>	88 89
PHY_DATA_2_H	N1	FW_DATA<2>	88 89
PHY_DATA_3_H	M7	FW_DATA<3>	88 89
PHY_DATA_4_H	N6	FW_DATA<4>	88 89
PHY_DATA_5_H	L1	FW_DATA<5>	88 89
PHY_DATA_6_H	M3	FW_DATA<6>	88 89
PHY_DATA_7_H	L2	FW_DATA<7>	88 89
PHY_CTL_0_H	N2	FW_CTL<0>	88 89
PHY_CTL_1_H	N3	FW_CTL<1>	88 89
PHY_LPS_H	P6	FW_LPS	88 89
PHY_LREQ_H	P1	FW_LREQ	88 89
PHY_LCLK_H	R1	FW_CLK98M_LCLK_R	88
PHY_LINKON_L	N7	FW_LINKON	89
PHY_SCLK_H	P2	FW_CLK98M_PCLK	89 88
PHY_PINT_L	P3	FW_PINT	89 88

R8800 22 5% 1/16W MF-LF 402
FW_CLK98M_LCLK — 88 89

Master: Link

Shasta FireWire

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 88 OF 102	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	P38MM	CLOCKS		FW_CLK98M_PCLK_R
FW_TPA1	FW	FW	FW_TPA0	FW_TPA_P<0>
FW_TPA1	FW	FW	FW_TPA0	FW_TPA_N<0>
FW_TPB1	FW	FW	FW_TPB0	FW_TPB_P<0>
FW_TPB1	FW	FW	FW_TPB0	FW_TPB_N<0>
FW_TPA2	FW	FW	FW_TPA1	FW_TPA_P<1>
FW_TPA2	FW	FW	FW_TPA1	FW_TPA_N<1>
FW_TPB2	FW	FW	FW_TPB1	FW_TPB_P<1>
FW_TPB2	FW	FW	FW_TPB1	FW_TPB_N<1>
FW_TPA3	FW	FW	FW_TPA2	FW_TPA_P<2>
FW_TPA3	FW	FW	FW_TPA2	FW_TPA_N<2>
FW_TPB3	FW	FW	FW_TPB2	FW_TPB_P<2>
FW_TPB3	FW	FW	FW_TPB2	FW_TPB_N<2>
VESTA_CLK24M_XTALI	P38MM	CRYSTAL		VESTA_CLK24M_XTALI
	P38MM	CRYSTAL		VESTA_CLK24M_XTALO
	P38MM	CRYSTAL		VESTA_CLK24M_XTALO_R

Page Notes

Power aliases required by this page:
- _PPFW_PHY
- _PP3V3_FW
- _PP3V3_ENETFW
- _PP2V5_ENETFW
- _PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

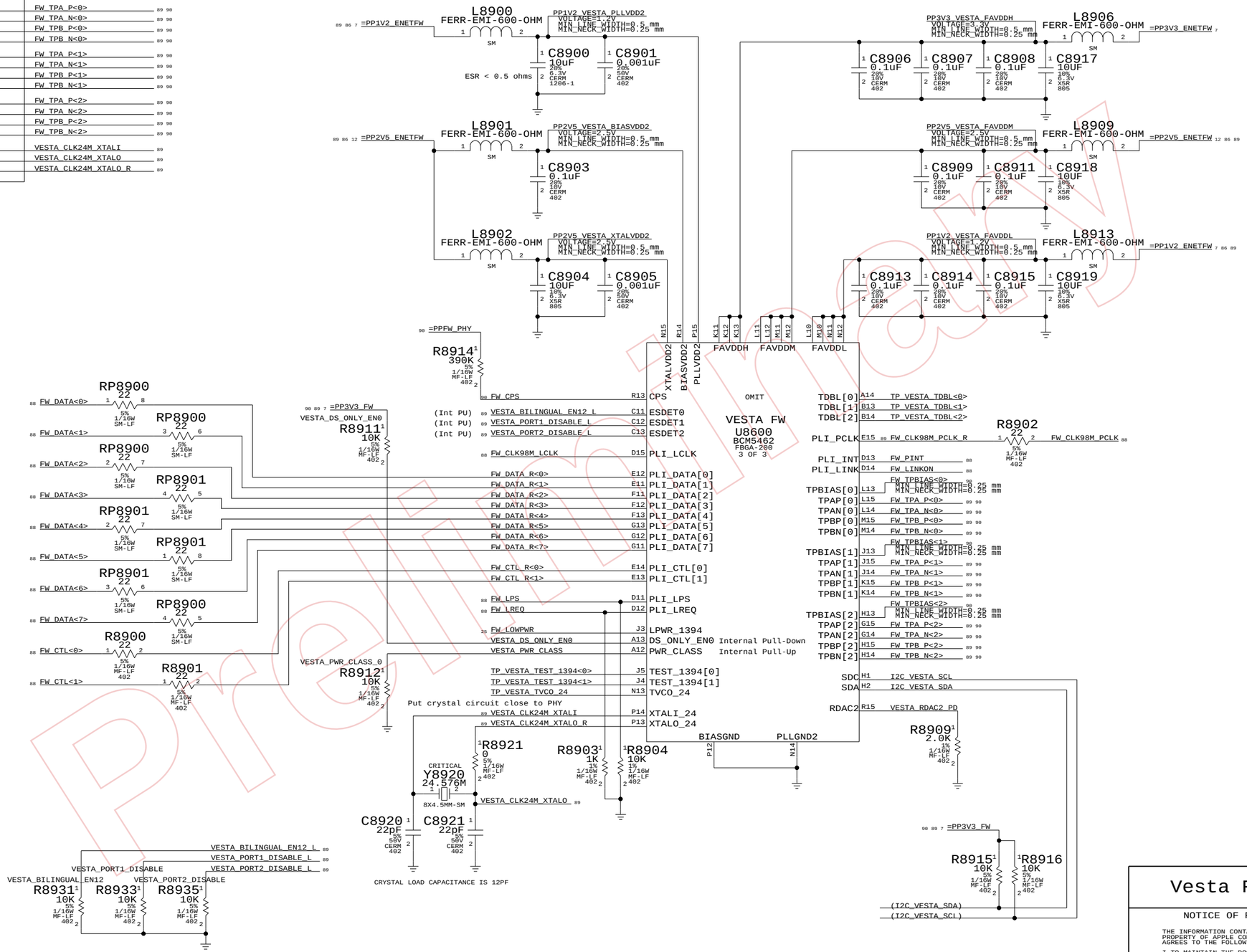
Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)



Vesta FireWire PHY

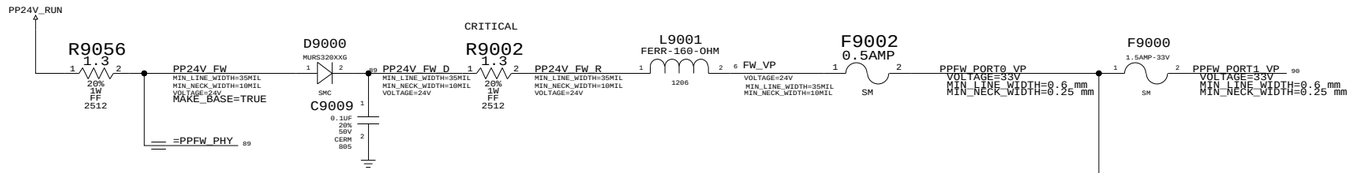
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 89 OF 102	

NET_TYPE				
SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	90
FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	90
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	90
FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	90
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	90
FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	90
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	90
FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	90

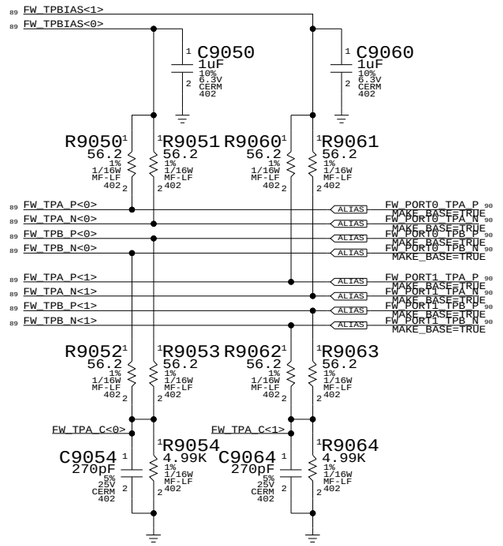
8 WATTS MAX

24 VOLTS

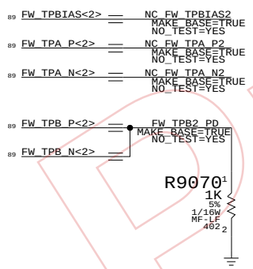


Termination

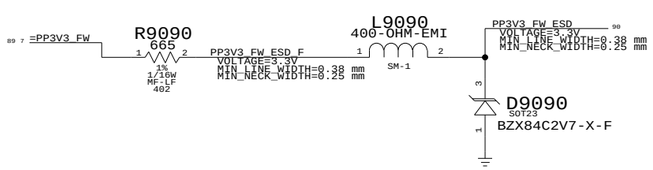
Place close to FireWire PHY



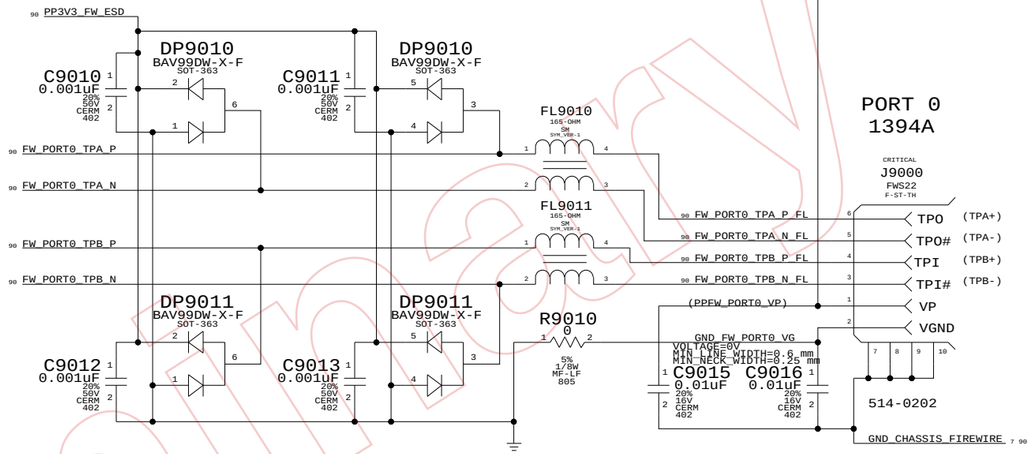
3rd TPA/TPB pair unused



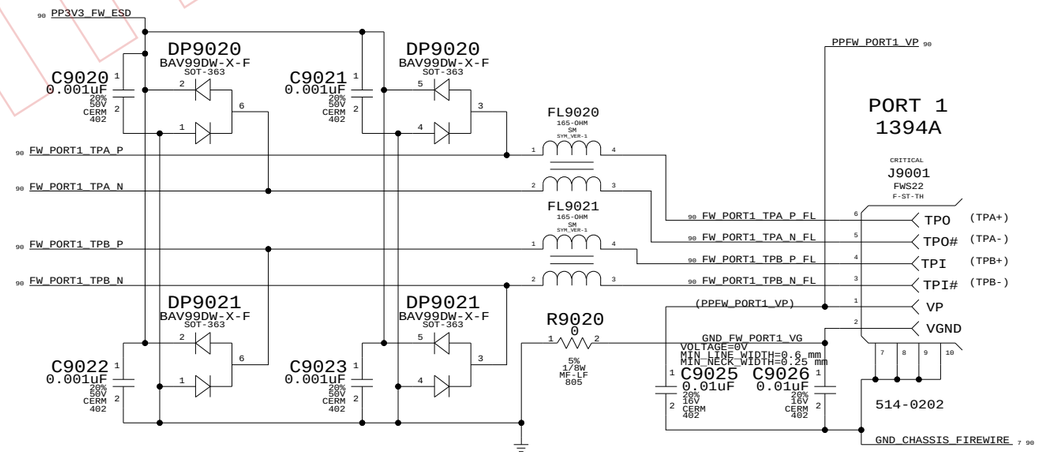
ESD Rail



"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection



FIREWIRE CONNECTORS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT	OF
NONE	90	102

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0> 91 92
USB2_0	USB2	USB2	USB2_0	USB2_N<0> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_P<1> 91 92
USB2_1	USB2	USB2	USB2_1	USB2_N<1> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_P<2> 91 92
USB2_2	USB2	USB2	USB2_2	USB2_N<2> 91 92
USB2_3	USB2	USB2	USB2_3	USB2_P<3> 6 91 92
USB2_3	USB2	USB2	USB2_3	USB2_N<3> 6 91 92
USB2_4	USB2	USB2	USB2_4	USB2_P<4> 76 91
USB2_4	USB2	USB2	USB2_4	USB2_N<4> 76 91
USB2_NEC_XTAL		15_MIL_SPACING		NEC_CLK30M_XT1 91
		15_MIL_SPACING		NEC_CLK30M_XT2 91
		15_MIL_SPACING		NEC_CLK30M_XT2_R 91

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

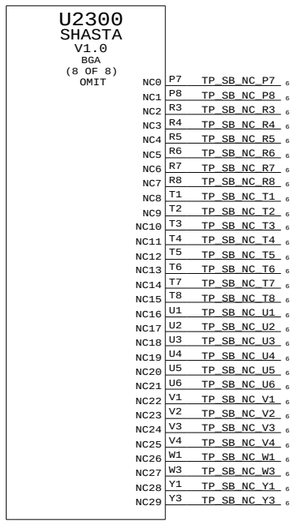
Signal aliases required by this page:
(NONE)

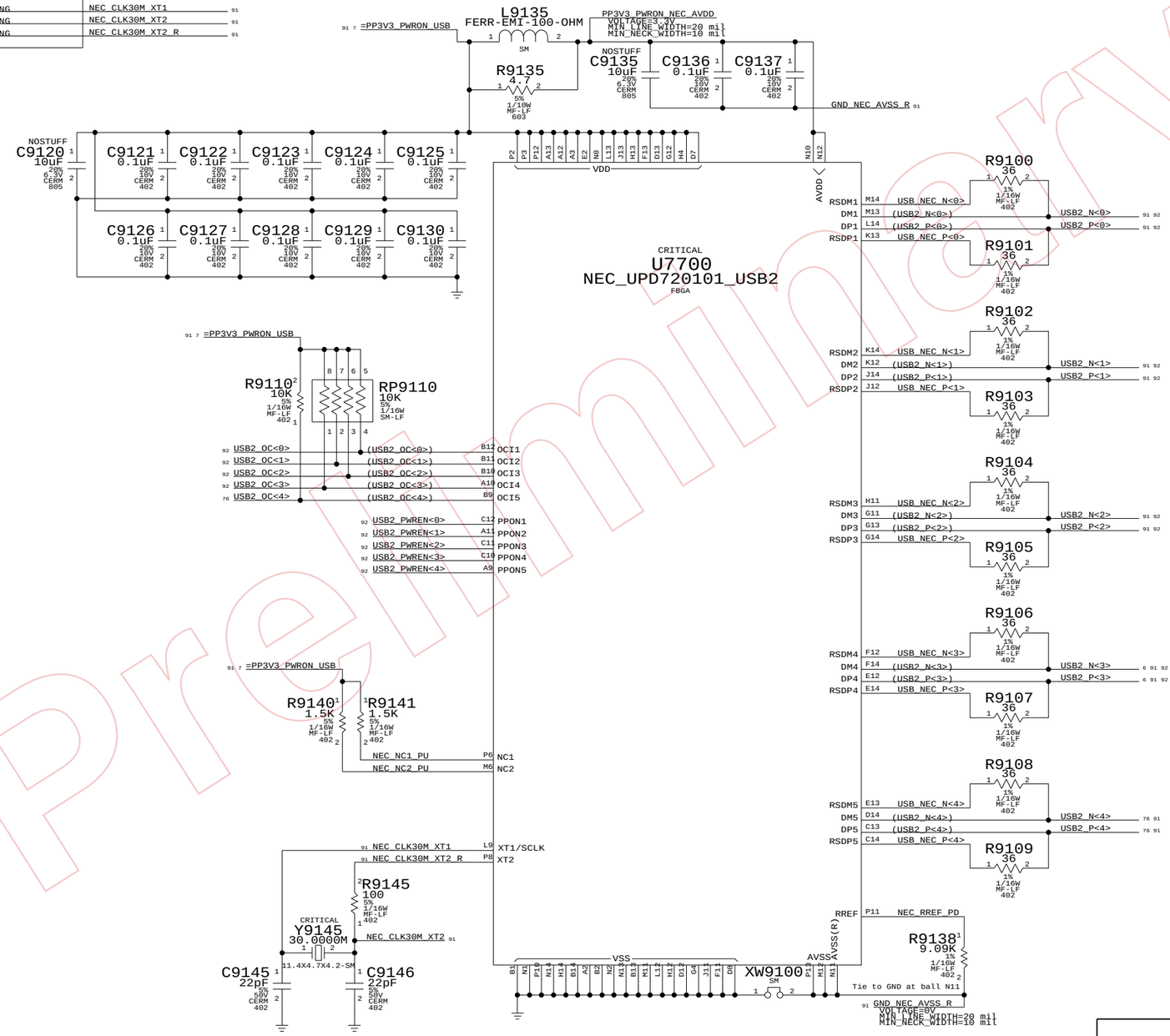
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





MASTER: SEEDY

USB Host Interfaces

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 04

SCALE NONE | SHT 91 OF 102

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2_PORT1_P_F
	USB2	USB2_PORT1_F	USB2_PORT1_N_F
	USB2	USB2_PORT2_F	USB2_PORT2_P_F
	USB2	USB2_PORT2_F	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2_PORT3_N_F

External USB Ports

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

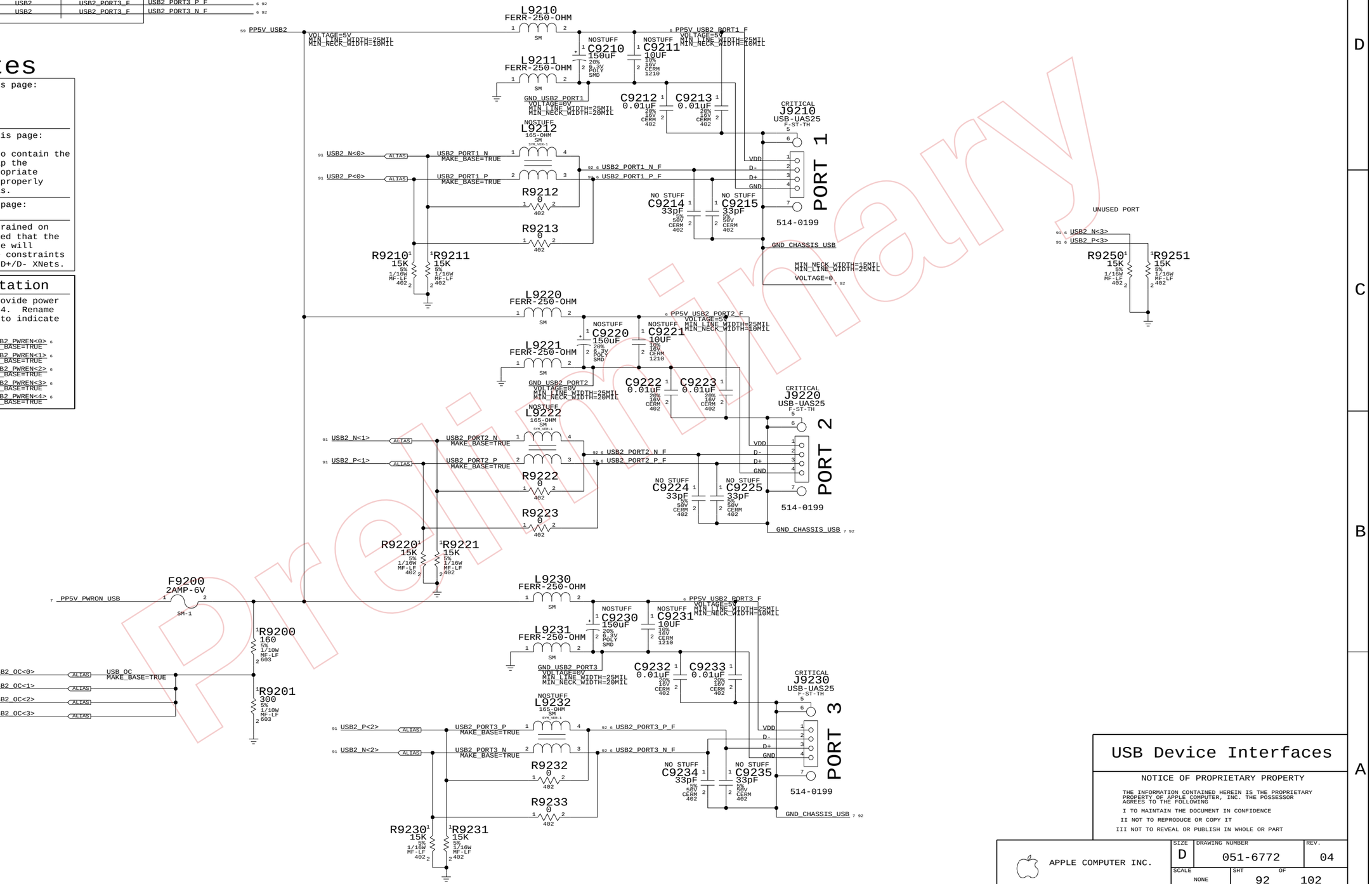
BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- USB2_PWREN<0> → TP_USB2_PWREN<0>
- USB2_PWREN<1> → TP_USB2_PWREN<1>
- USB2_PWREN<2> → TP_USB2_PWREN<2>
- USB2_PWREN<3> → TP_USB2_PWREN<3>
- USB2_PWREN<4> → TP_USB2_PWREN<4>



USB Device Interfaces

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 92 OF 102	

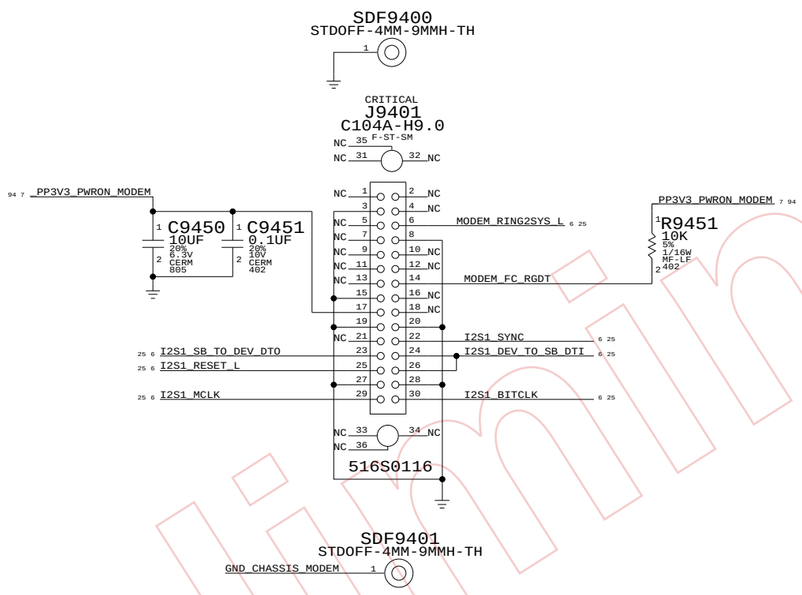
Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Q52 Modem Connector



From Intel Mobile Audio/Modem
Daughter Card Specification
Rev 1.0, February 22, 1999

1 - MONO_OUT/PC_BEEP	2 - AUDIO_PWRON
3 - GND	4 - MONO_PHONE
5 - AUXA_RIGHT	6 - RESERVED
7 - AUXA_LEFT	8 - GND
9 - CD_GND	10 - 5Vmain
11 - CD_RIGHT	12 - RESERVED
13 - CD_LEFT	14 - RESERVED
15 - GND	16 - PRIMARY_DN
17 - 3.3Vaux	18 - 5Vd
19 - GND	20 - GND
21 - 3.3Vmain	22 - AC97_SYNC
23 - AC97_SDATA_OUT	24 - AC97_SDATA_INB
25 - AC97_RESET#	26 - AC97_SDATA_INA
27 - GND	28 - GND
29 - AC97_MSTRCLK	30 - AC97_BITCLK

RJ11 CONNECTOR

STUFFED AT FATP
SYMBOL USED FOR PLACEMENT

OMIT

J9402
RJ11-HGT27.5
ST-TH

514-0205

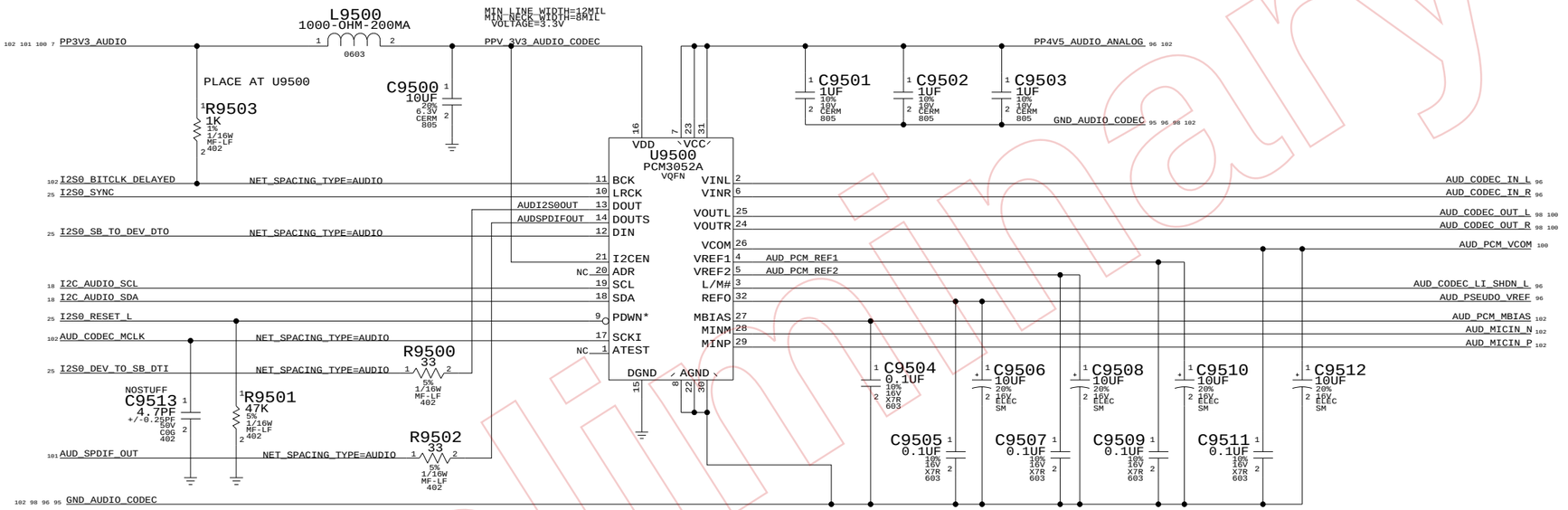
Modem Interface

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04

SCALE	SHT	OF
NONE	94	102

AUDIO CODEC
APPLE P/N 353S0933



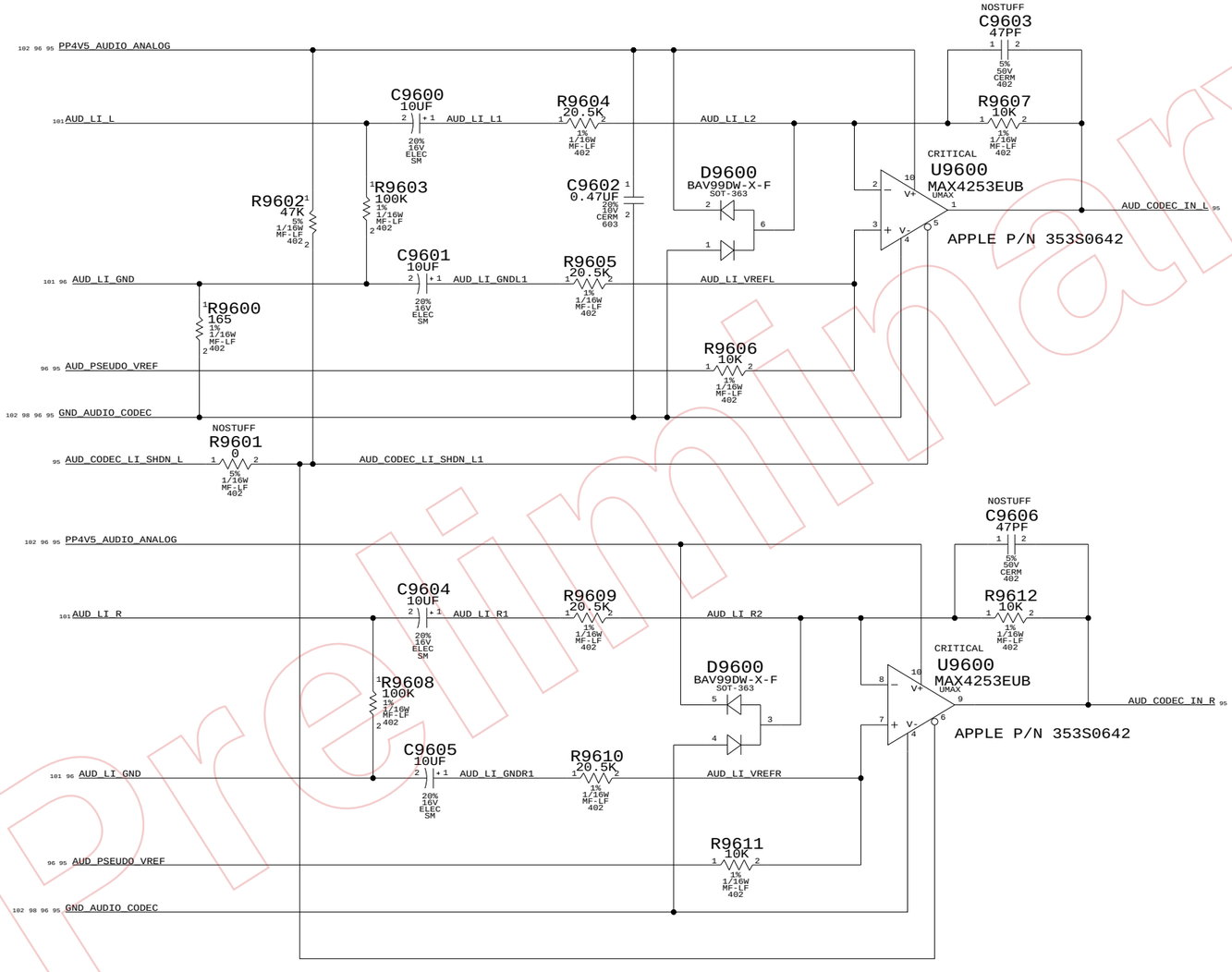
AUDIO: CODEC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 95 OF 102	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



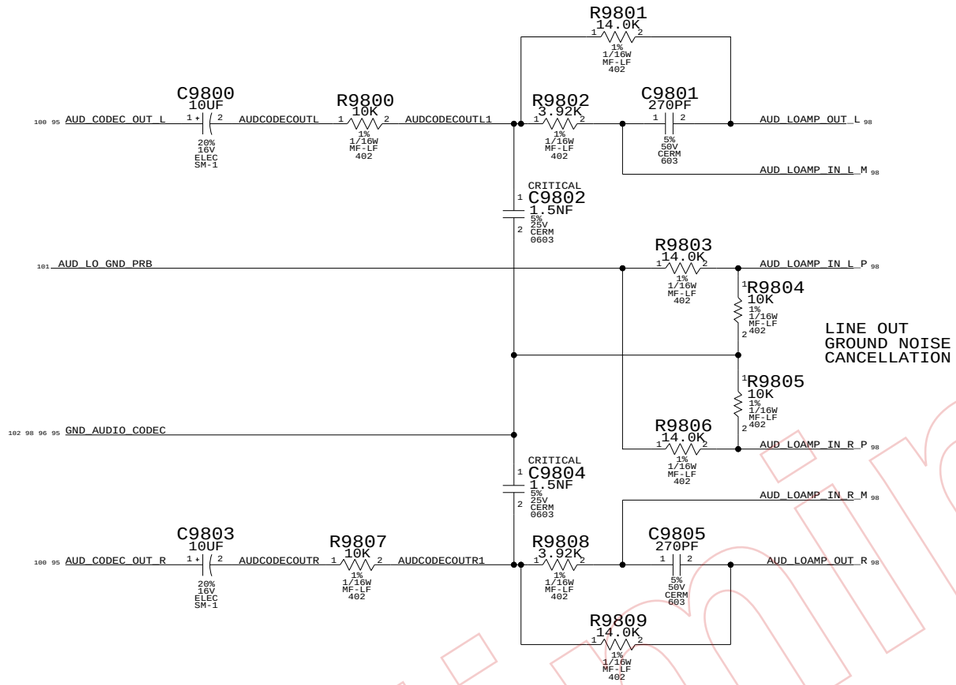
AUDIO: LINE INPUT AMP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 96 OF 102	

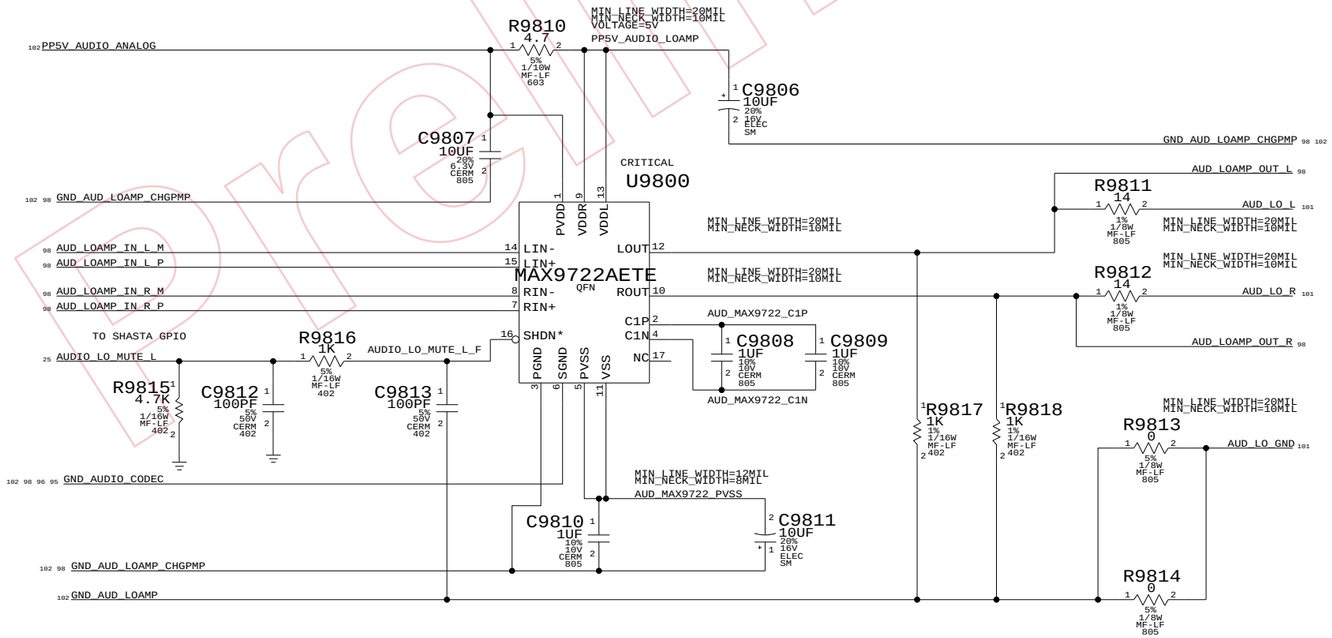
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

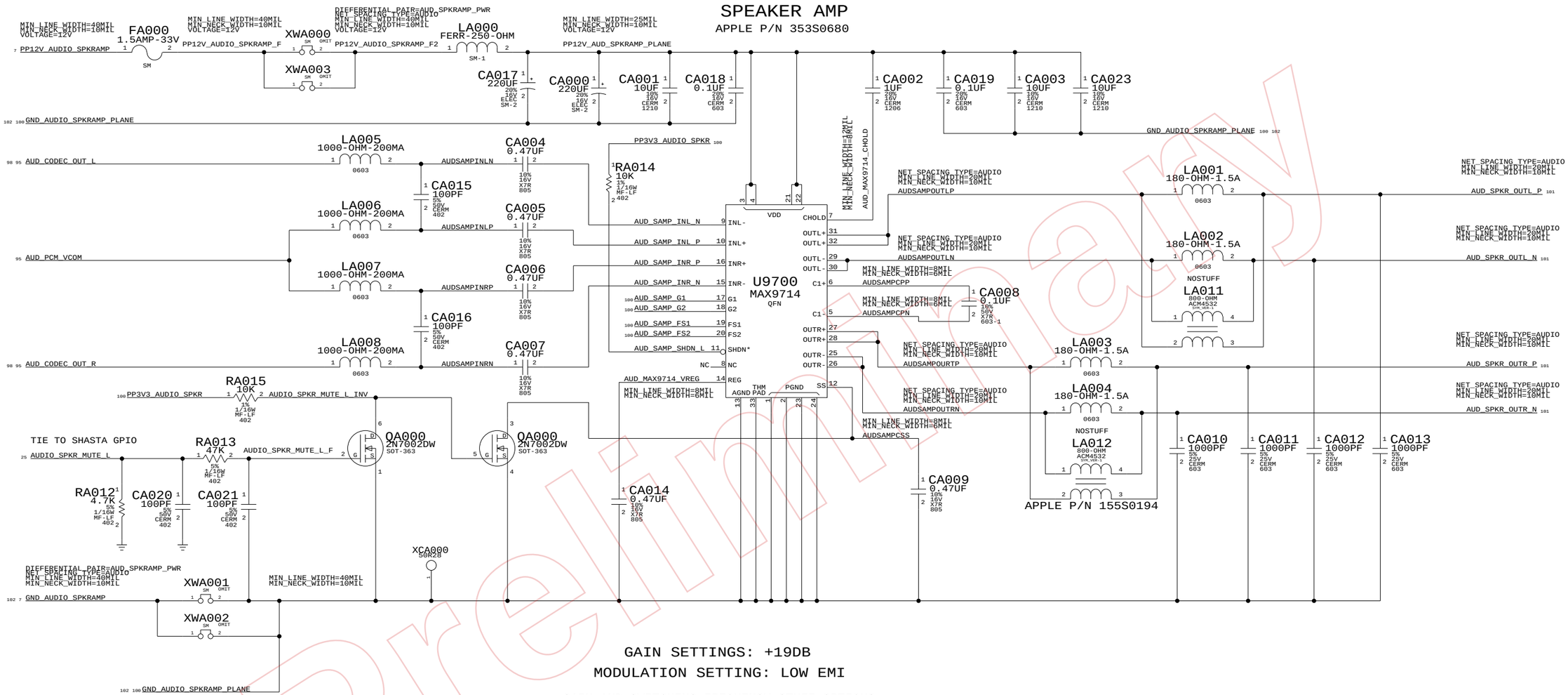
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6772 | REV. 04

SCALE NONE | SHT 98 OF 102

SPEAKER AMP

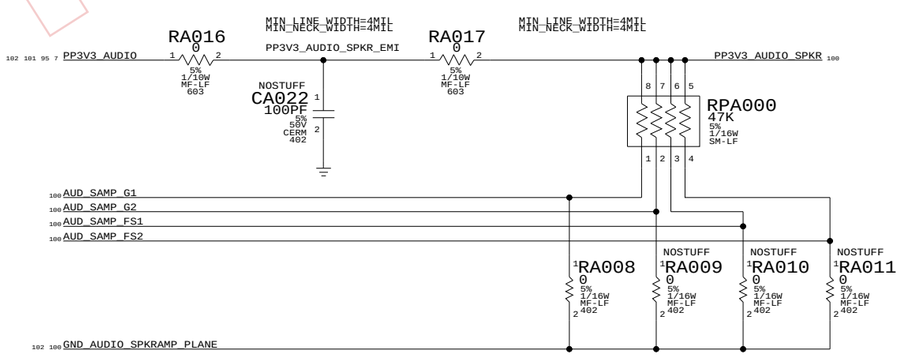
APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

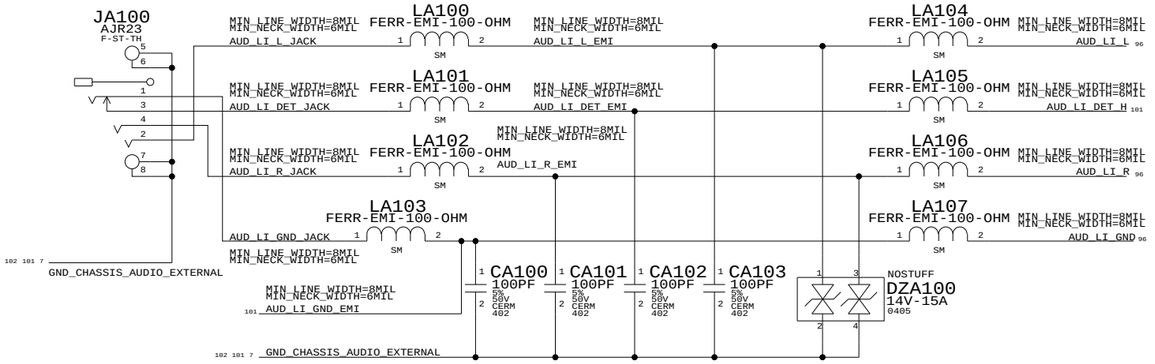
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 100 OF 102	

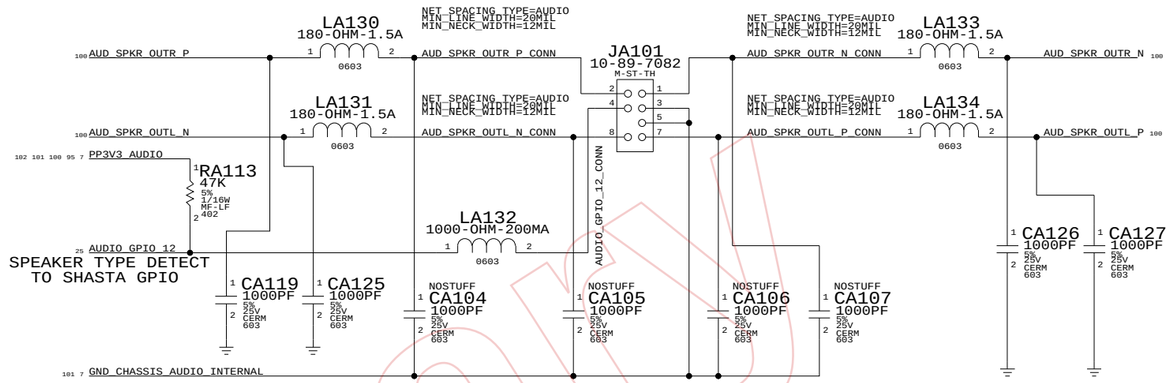
LINE IN JACK

APPLE P/N 514-0203



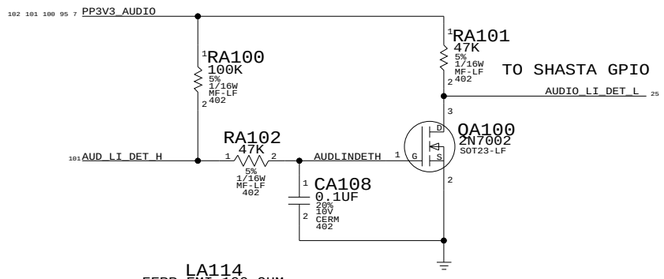
SPEAKER CABLE CONNECTOR

APPLE P/N 518-0138



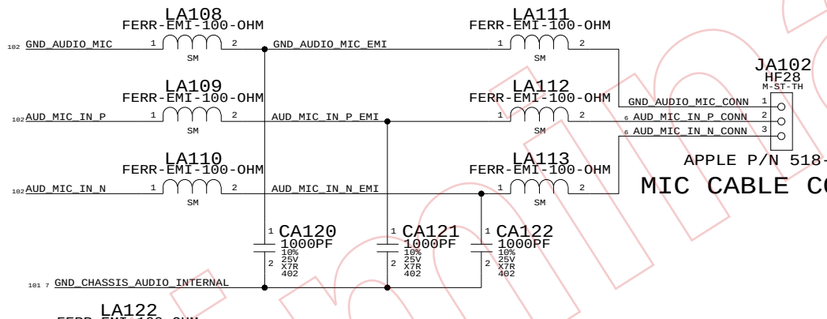
LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED



MIC CABLE CONNECTOR

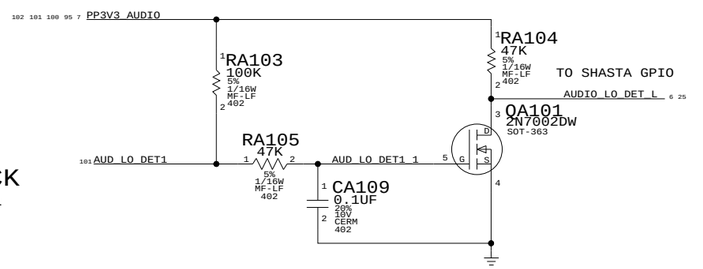
APPLE P/N 518-0034



LINE OUT PLUG DETECTS

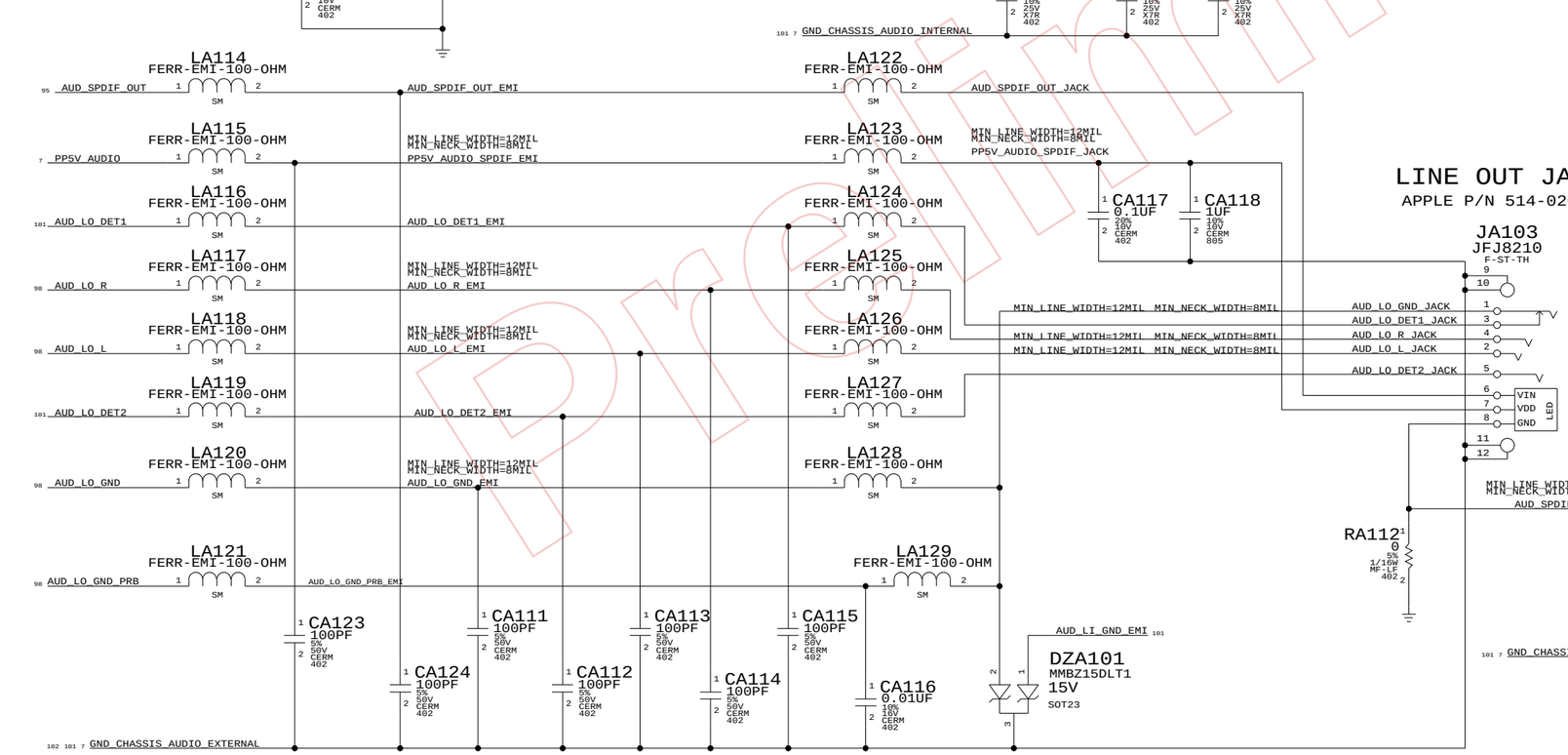
AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK

APPLE P/N 514-0204



PLACE NEAR J9801 XCA100 50H28

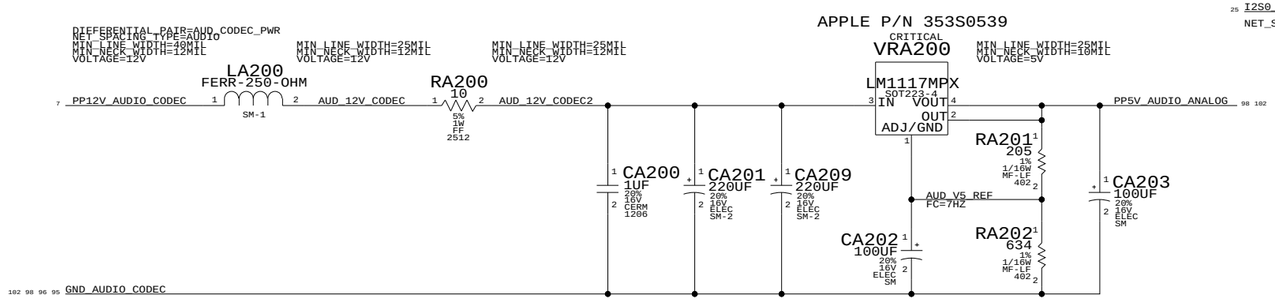
PLACE NEAR J700 XCA101 50H28

AUDIO: Q45 CONNECTORS

APPLE COMPUTER INC.

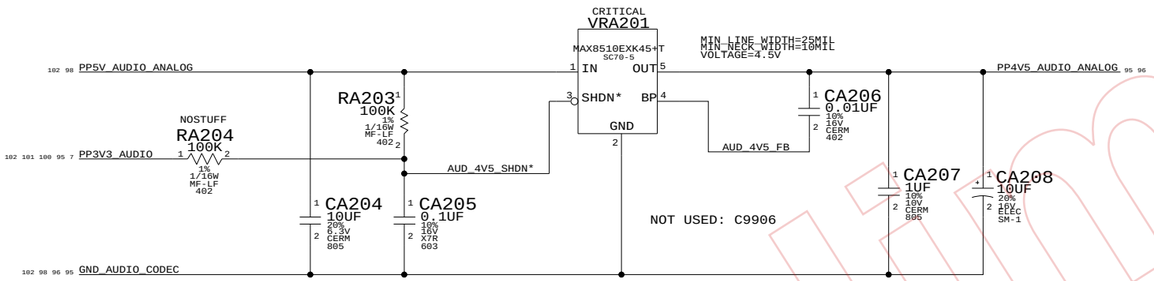
SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 101 OF 102	

5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP

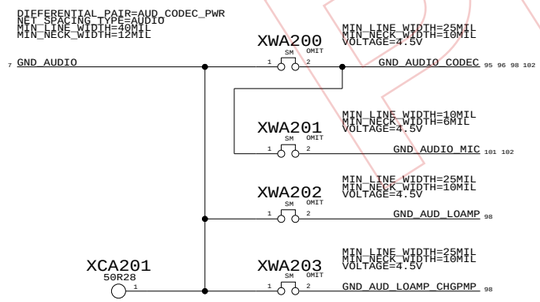


4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

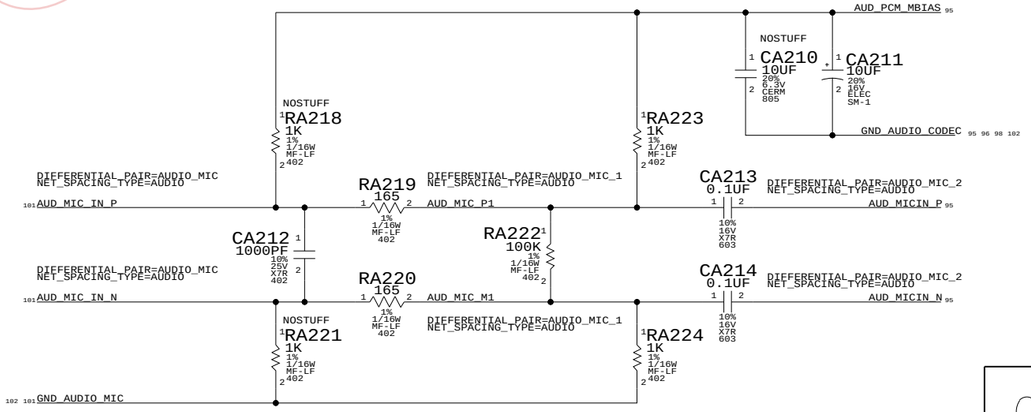
APPLE P/N 353S0733



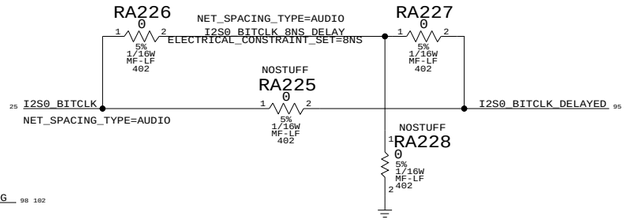
AUDIO GROUND RETURNS



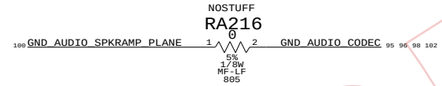
MICROPHONE IMPEDANCE MATCHING CIRCUIT



5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP



PLACE ACROSS GROUND SPLIT
AT RIGHT SIDE OF CA007

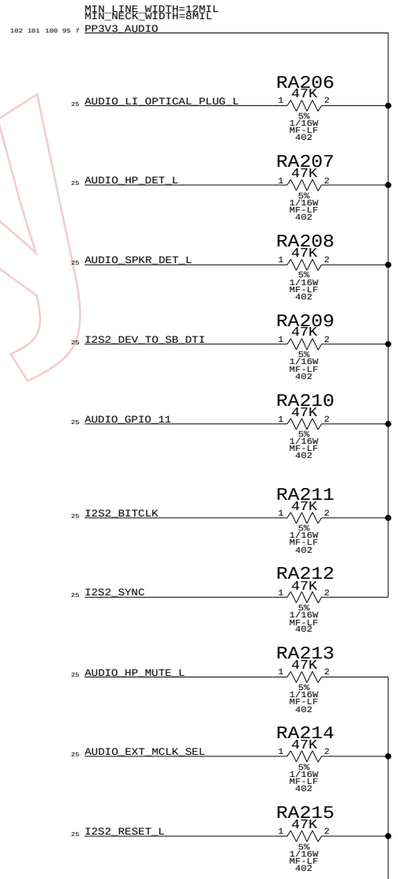


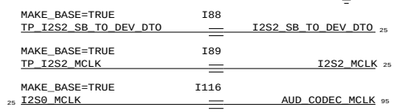
PLACE NEAR ENTRY TO SPEAKER
AMP GROUND PLANE

PLACE ACROSS GROUND SPLIT
AT CODEC U9500

PLACE AT J5903

UNUSED GPIO TERMINATIONS





AUDIO: Q45 POWER SUPPLIES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6772	04
SCALE: NONE	SHT 102 OF 102	