

M50 - DVT

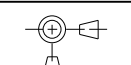
04/05/06

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
13		405954	ENGINEERING RELEASED	10/18/05	06/22/04

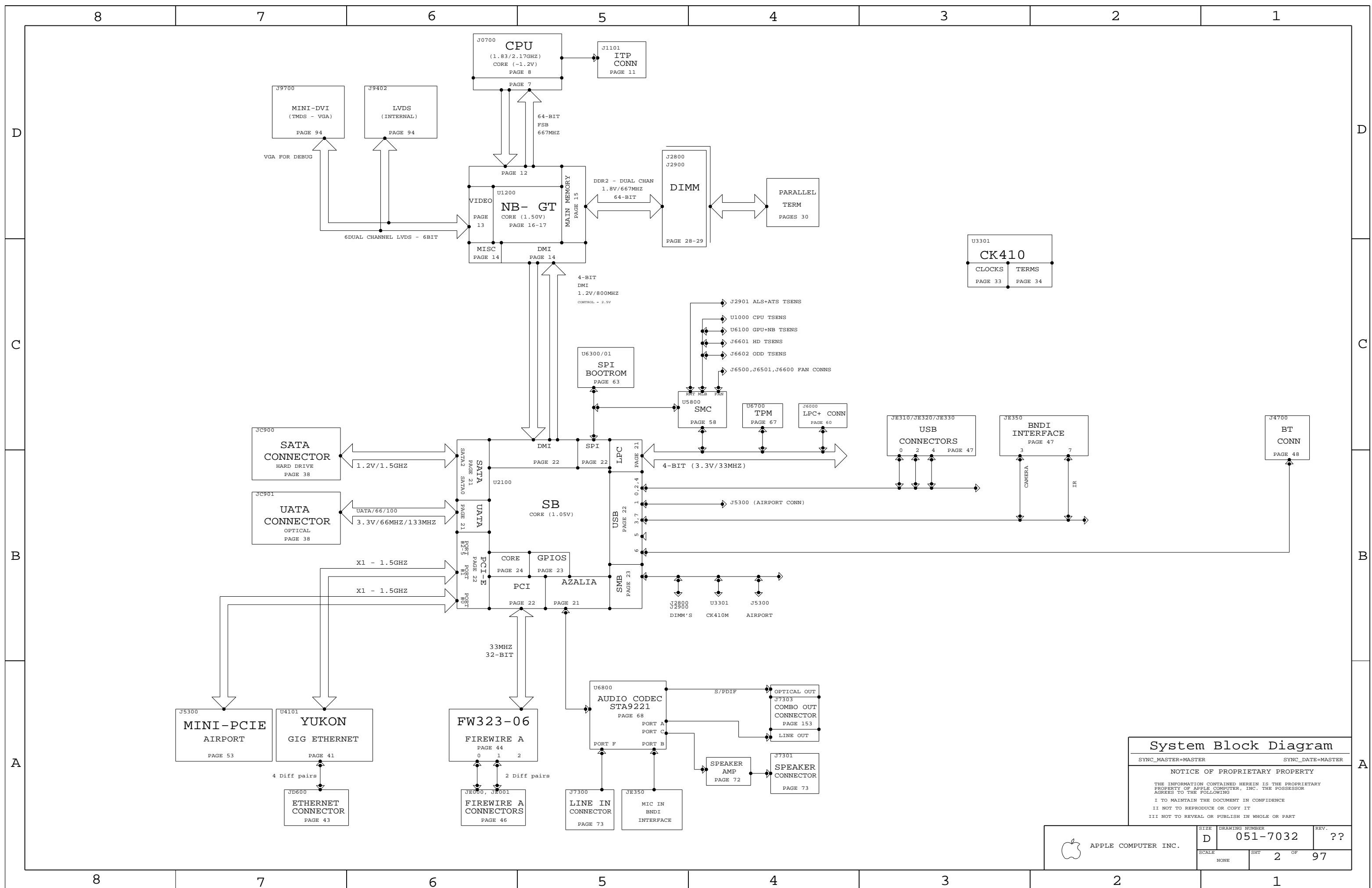
PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
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7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006	
12	12	NB CPU Interface	M1	01/05/2006	
13	13	NB PEG / Video Interfaces	M1	01/05/2006	
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1	01/05/2006	
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40	01/05/2006	
18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER	
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	03/30/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	03/30/2006	
54	73	AUDIO: CONNECTORS	AUDIO	03/30/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	03/30/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUI	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMD5	MASTER	MASTER	
66	96	TMD5/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTR	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7032	REV. ??
SHT 1 OF 97					

D
C
B
A

D
C
B
A



System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

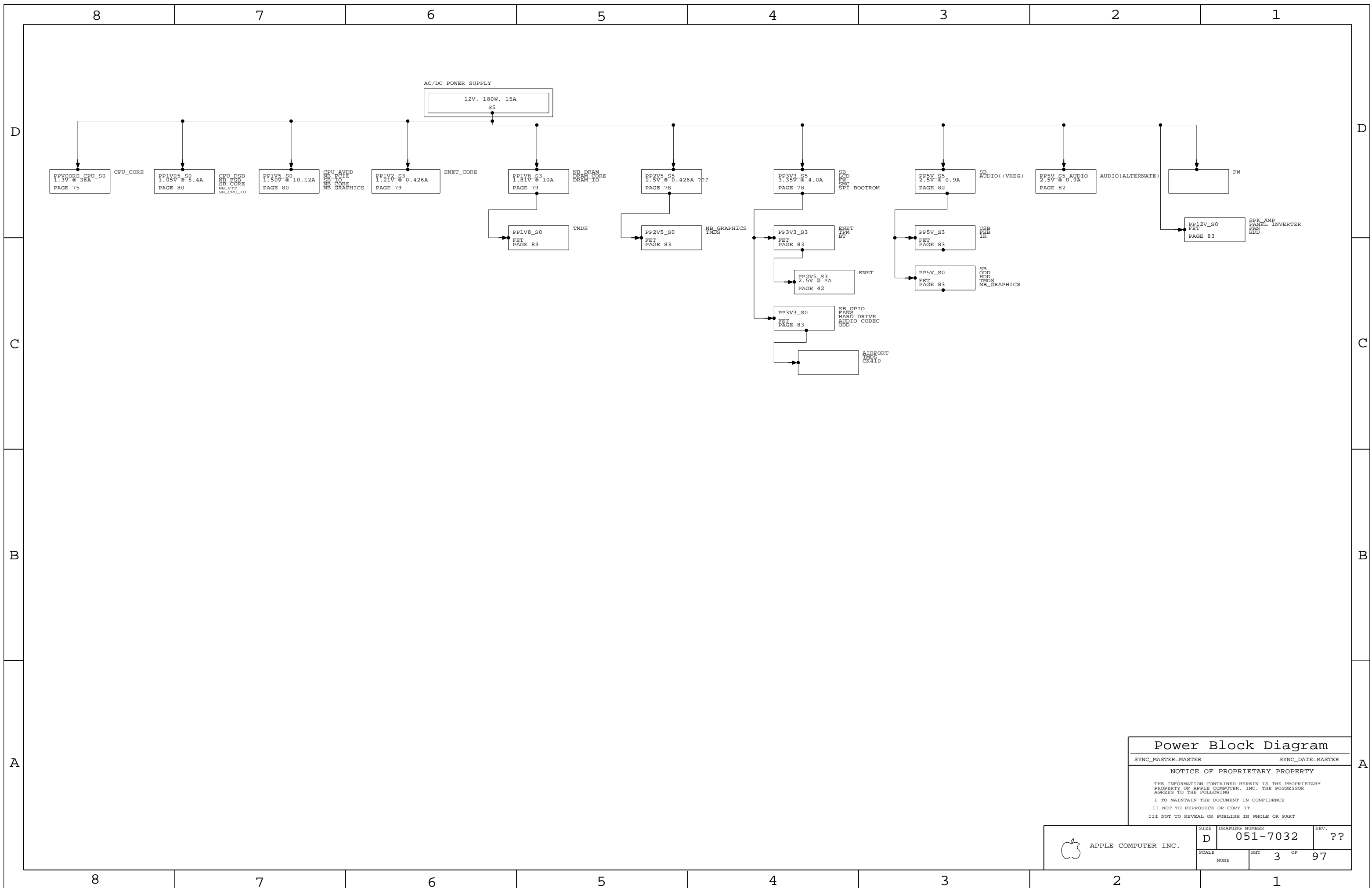
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	D	051-7032	??
SCALE	SHT	OF	REV.
NONE	2	97	




Power Block Diagram

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	D	051-7032	??
SCALE	SHT	OF	REV.
NONE	3	97	

8

7

6

5

4

3

2

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
338S0270	1	IC,888053,1GIGABIT ENET XCVR,64P QFN,MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1235	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHEM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0021	1	EFI ROM,M50	U6301	CRITICAL	
337S3244	1	M50 1.66G CPU (C0)	CPU	CRITICAL	YONAH
337S3242	1	M38 CPU (C0)	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		0628	FACTORY SHORTAGE
353S1381	353S1278		U5940	SMC VREF
378S0140	378S0141		LXD601,LXD602,LXD603	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:V3M]	CRITICAL	

Table Items

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D	051-7032	??
SCALE	SHT	OF
NONE	4	97

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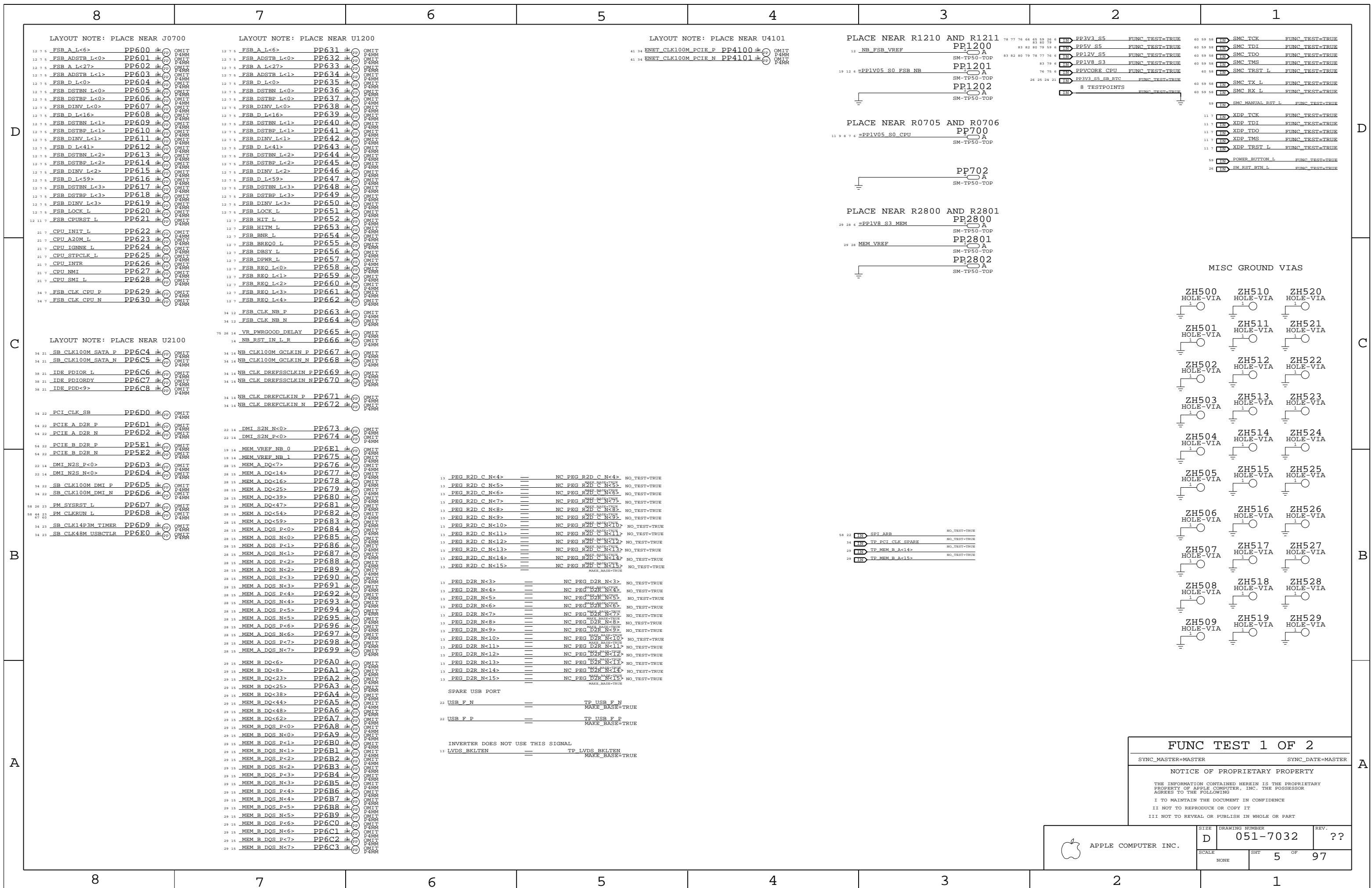
5

4

3

2

1



LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

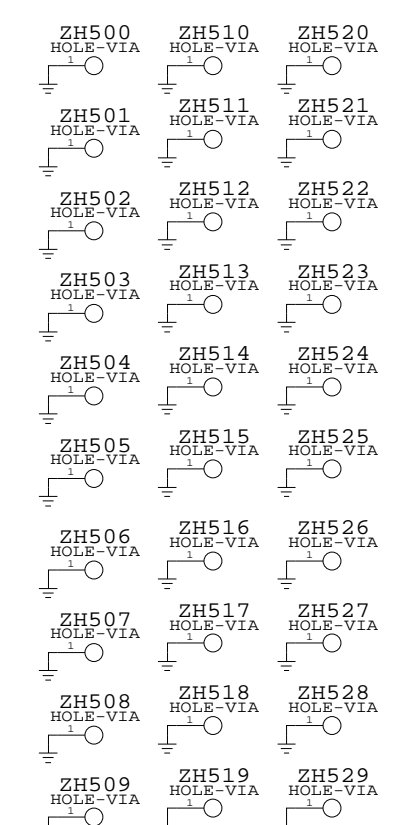
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

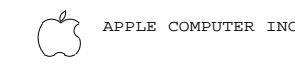
MISC GROUND VIAS



FUNC TEST 1 OF 2

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SCALE NONE	DRAWING NUMBER D 051-7032	REV. ??



"S0" RAILS

ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

82 78 76 SYS POWERFAIL L I632 POWER_GOOD

PP0V9_S0 =PP0V9_S0_MEMVTT_LDO =PP0V9_S0_MEM_TERM

PP1V2_S3 =PP1V2_S3_LAN

PP3V3_S5 =PP3V3_S5_SB =PP3V3_S5_SB_USB =PP3V3_S5_SB_PM =PP3V3_S5_SB_VCCSUS3_3 =PP3V3_S5_SB_VCCSUS3_3_USB =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA =PP3V3_S5_SB_IO =PP3V3_S5_SB_FW =PP3V3_S5_SMC =PP3V3_S5_2V5_LDO =PP3V3_S5_DEBUG =PP3V3_S5_ROM =PP3V3_S5_LCD

PPVCORE_CPU =PPVCORE_S0_CPU

PP1V8_S3 =PP1V8_S3_MEM_NB =PP1V8_S3_MEM =PP1V8_S3_1V2_LDO

PP5V_S5 =PP5V_S5_SB =PP5V_S5_AUDIO_LDO XW604 SM OMIT PP5V_S5_AUDIO =PP5V_S5_AUDIO

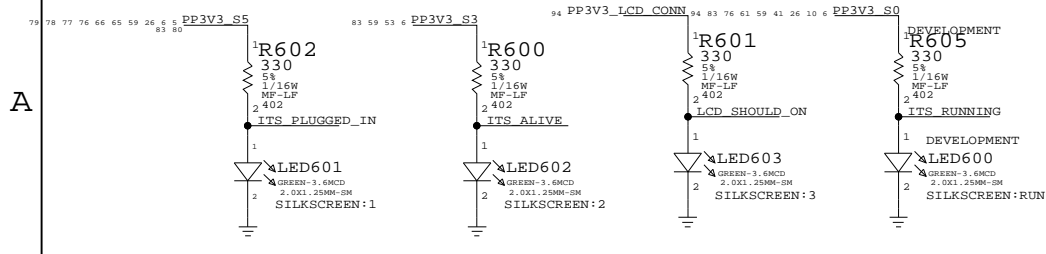
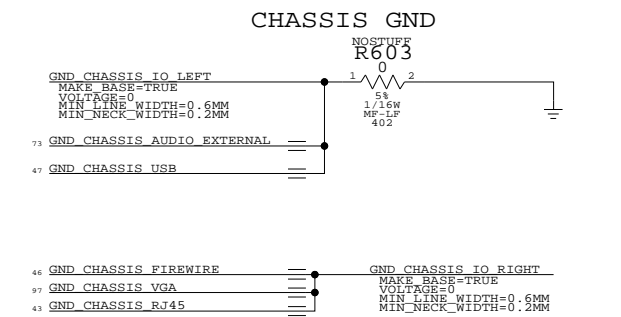
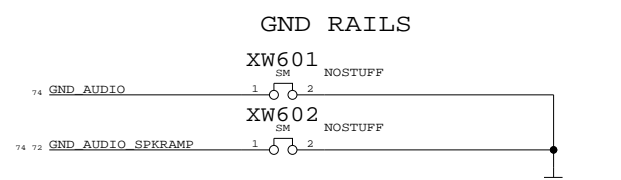
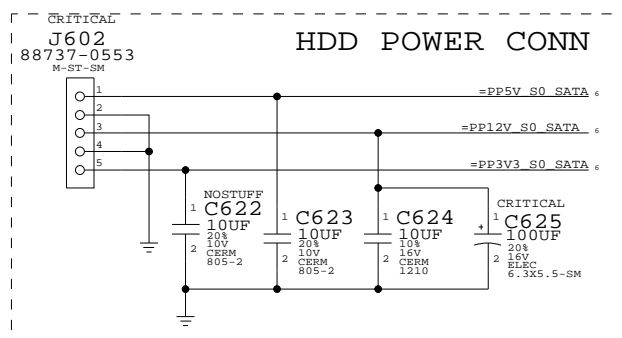
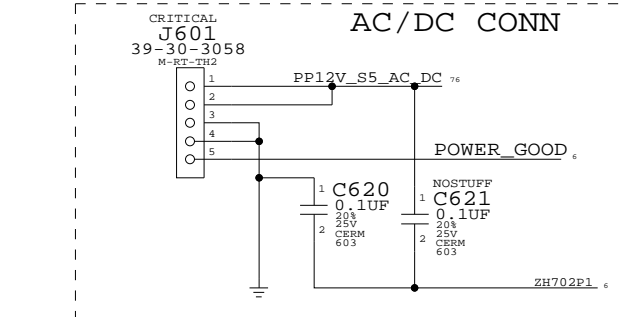
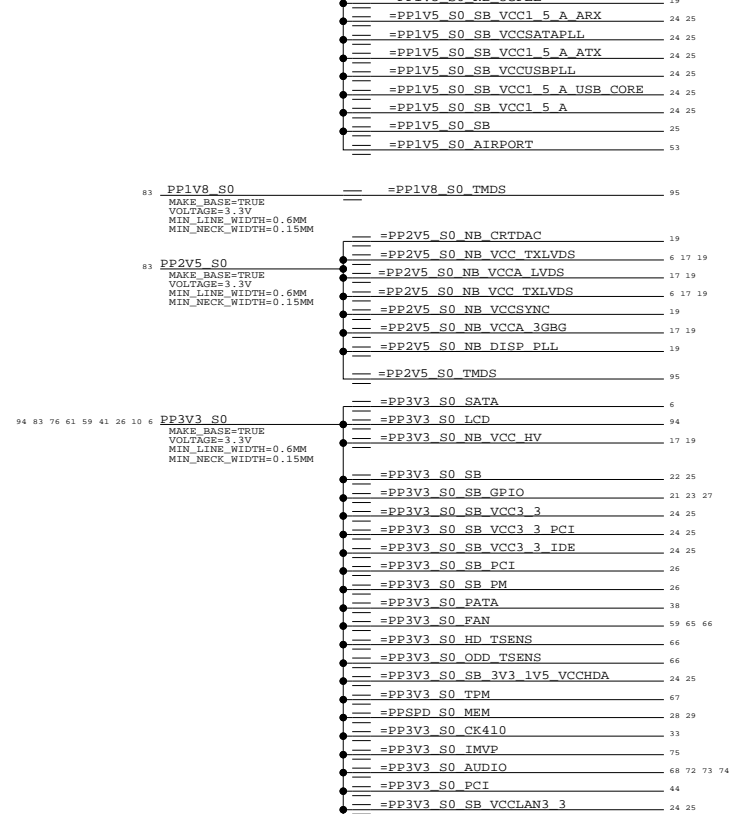
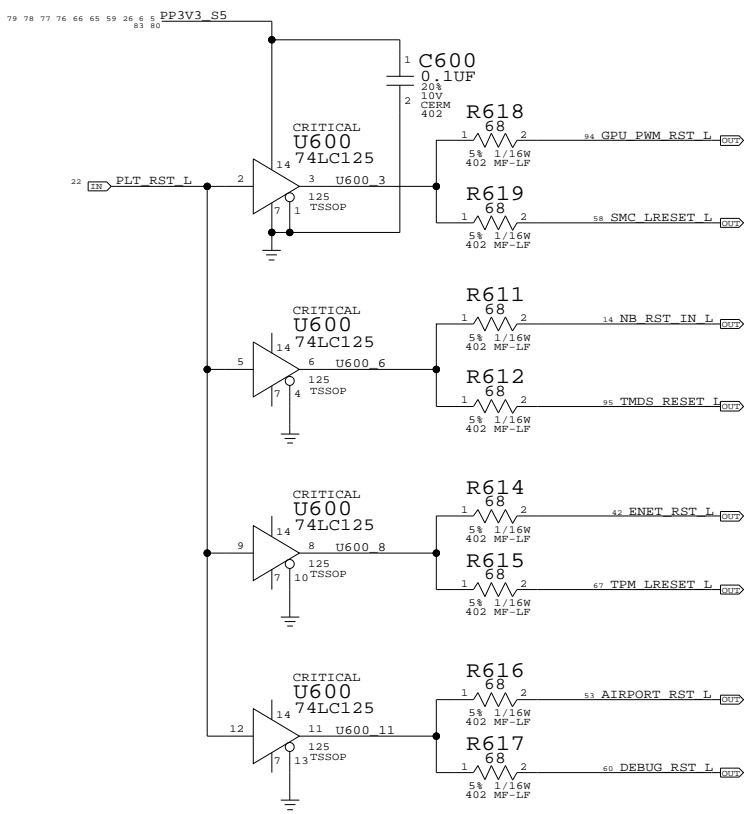
PP1V05_S0 =PP1V05_S0_CPU =PP1V05_S0_FSB_NB =PP1V05_S0_NB_VTT =PP1V05_S0_SB_CPU_IO =PPVCORE_S0_SB

PP3V3_S3 =PP3V3_S3_ENET =PP3V3_S3_TPM =PP3V3_S3_BT

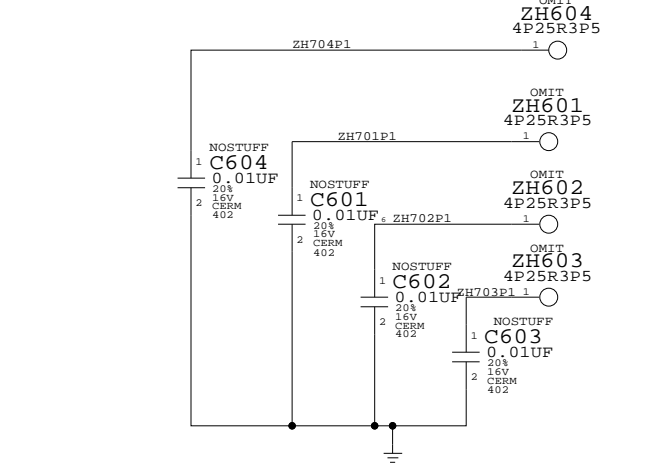
PP1V5_S0 =PPVCORE_S0_NB =PP1V5_S0_CPU =PP1V5_S0_NB_PCIE =PP1V5_S0_NB_TVDAC =PP1V5_S0_NB_VCCD_HMPLL =PP1V5_S0_NB_VCCD_LVDS =PP1V5_S0_NB_VCCD_LVDS =PP1V5_S0_NB_VCCAUX =PP1V5_S0_NB_PLL =PP1V5_S0_NB =PP1V5_S0_NB_TVDAC =PP1V5_S0_NB_3GPLL =PP1V5_S0_SB_VCC1_5_A_ARX =PP1V5_S0_SB_VCCSATAPLL =PP1V5_S0_SB_VCC1_5_A_ATX =PP1V5_S0_SB_VCCSUSBLL =PP1V5_S0_SB_VCC1_5_A_USB_CORE =PP1V5_S0_SB_VCC1_5_A =PP1V5_S0_SB =PP1V5_S0_AIRPORT

PP5V_S3 =PP5V_S3_USB =PP5V_S3_BNDI =PP5V_S0_MEMVTT USING S3 TO DRIVE S0 OK IN THIS CASE

PP12V_S5 =PP12V_S5_FW =PP12V_S5_CPU



PP4V5_S0_AUDIO_ANALOG =PP4V5_S0_AUDIO_ANALOG



PP5V_S0 =PP5V_S0_SB =PP5V_S0_PATA =PP5V_S0_NBISENSE =PP5V_S0_DEBUG =PP5V_S0_SATA =PP5V_S0_TMSD =PP5V_S0_NB_TVDAC

PP12V_S0 =PP12V_S0_FAN XW605 SM OMIT PP12V_S0_AUDIO_SPKRAMP =PP12V_S0_AUDIO_SPKRAMP PP12V_INVERTER =PP12V_S0_SATA

Power Conn / Alias

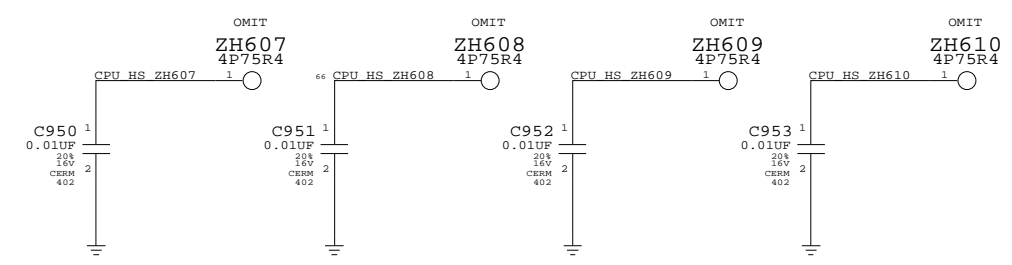
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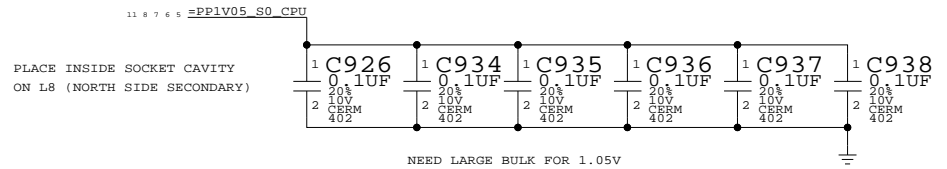
Table with columns: SCALE (NONE), SHEET (6 OF 97), DRAWING NUMBER (051-7032), REV. (??), and APPLE COMPUTER INC. logo.

CPU HEATSINK MOUNTING HOLES



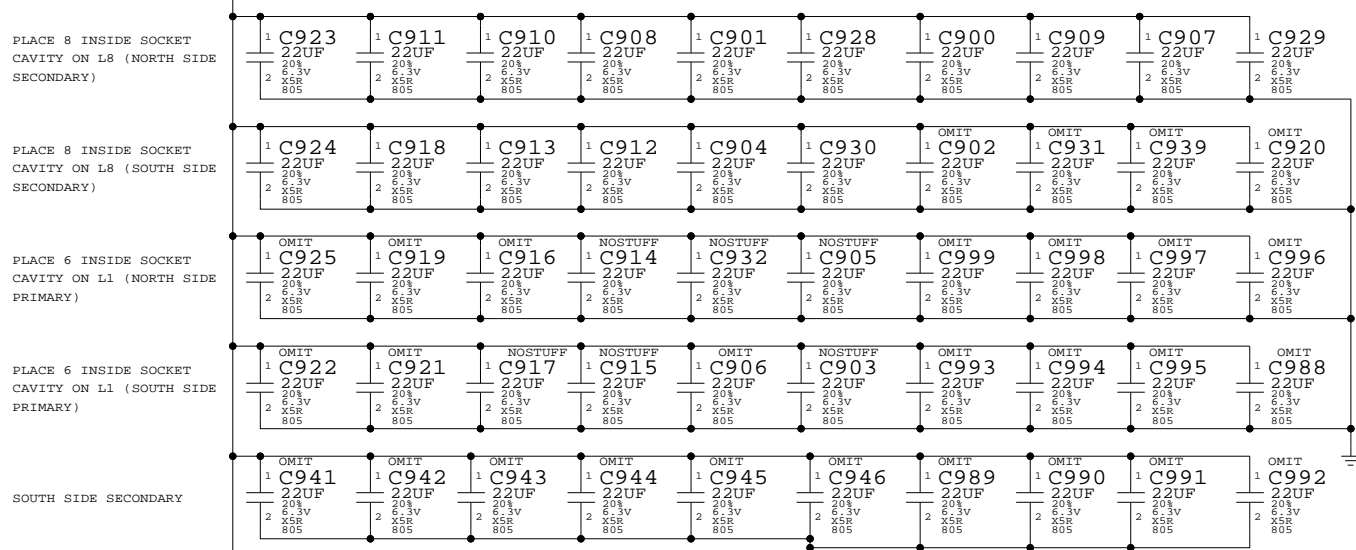
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



VCC CORE COUPLING CAPS USES DIFFERENT VALUES FOR MEROME VS. YONAH. SEE BOM TABLE.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

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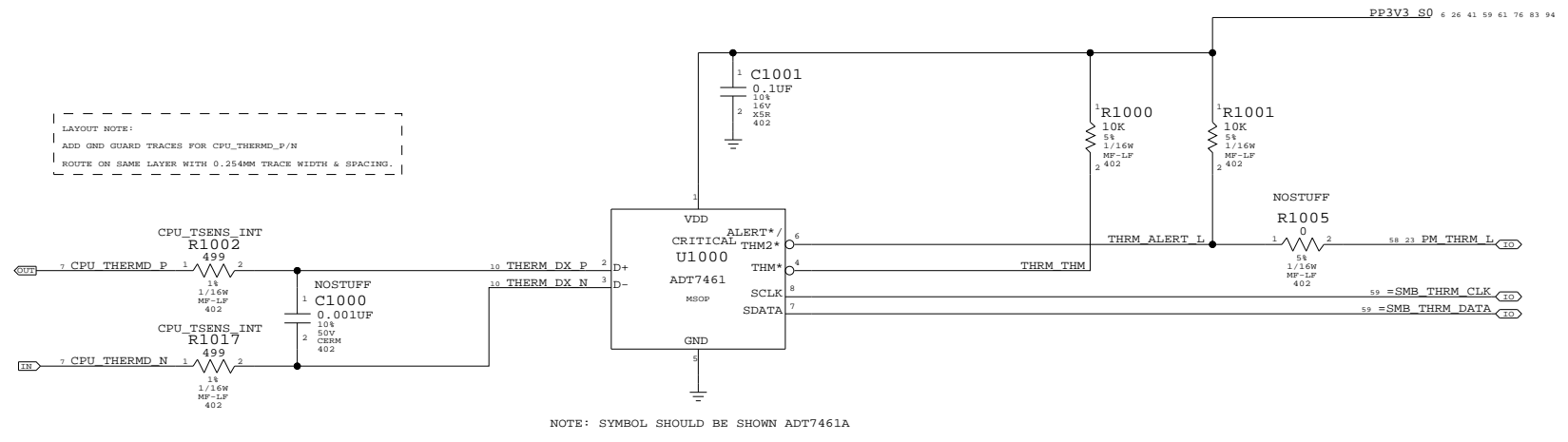
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	D	051-7032	??
SCALE	SHT	9 OF	97
NONE			

CPU THERMAL SENSOR

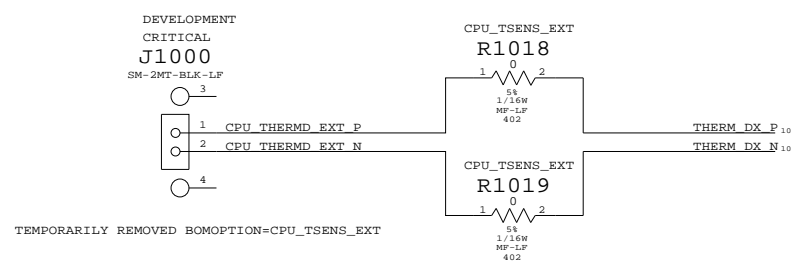
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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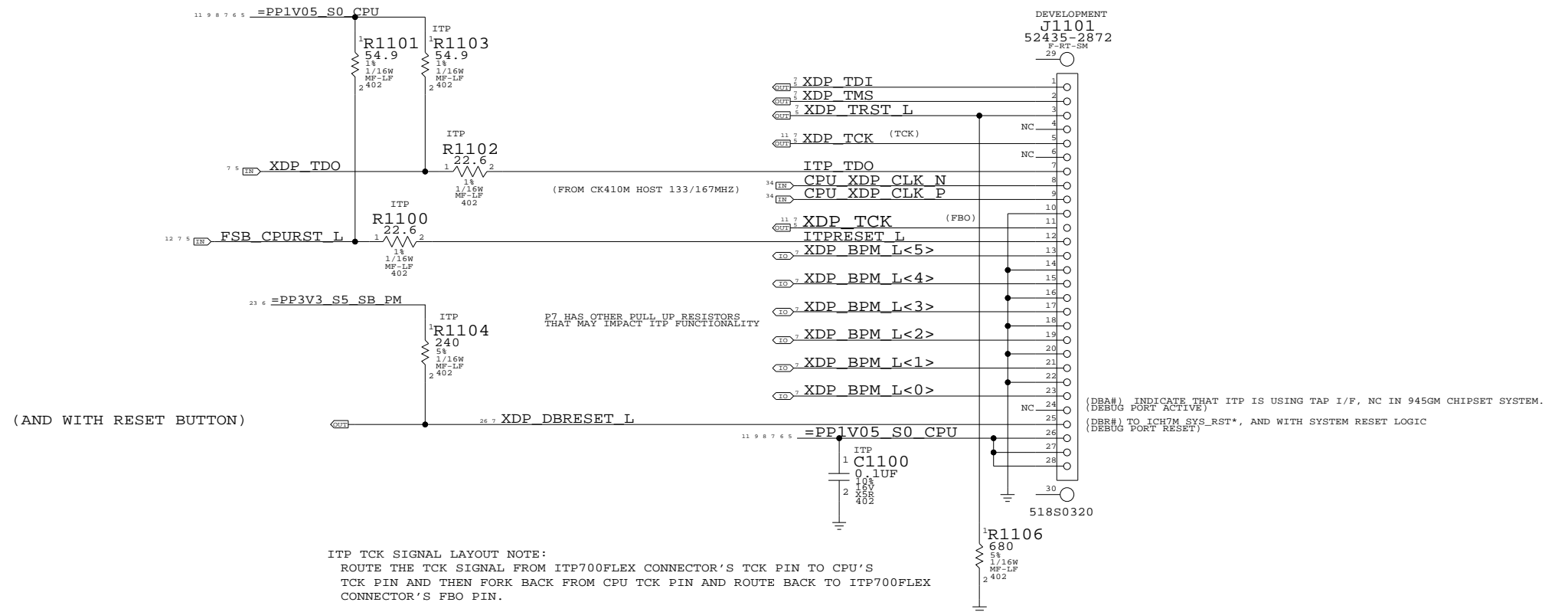
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	D	051-7032	??
SCALE	SHT	10 OF 97	
NONE			

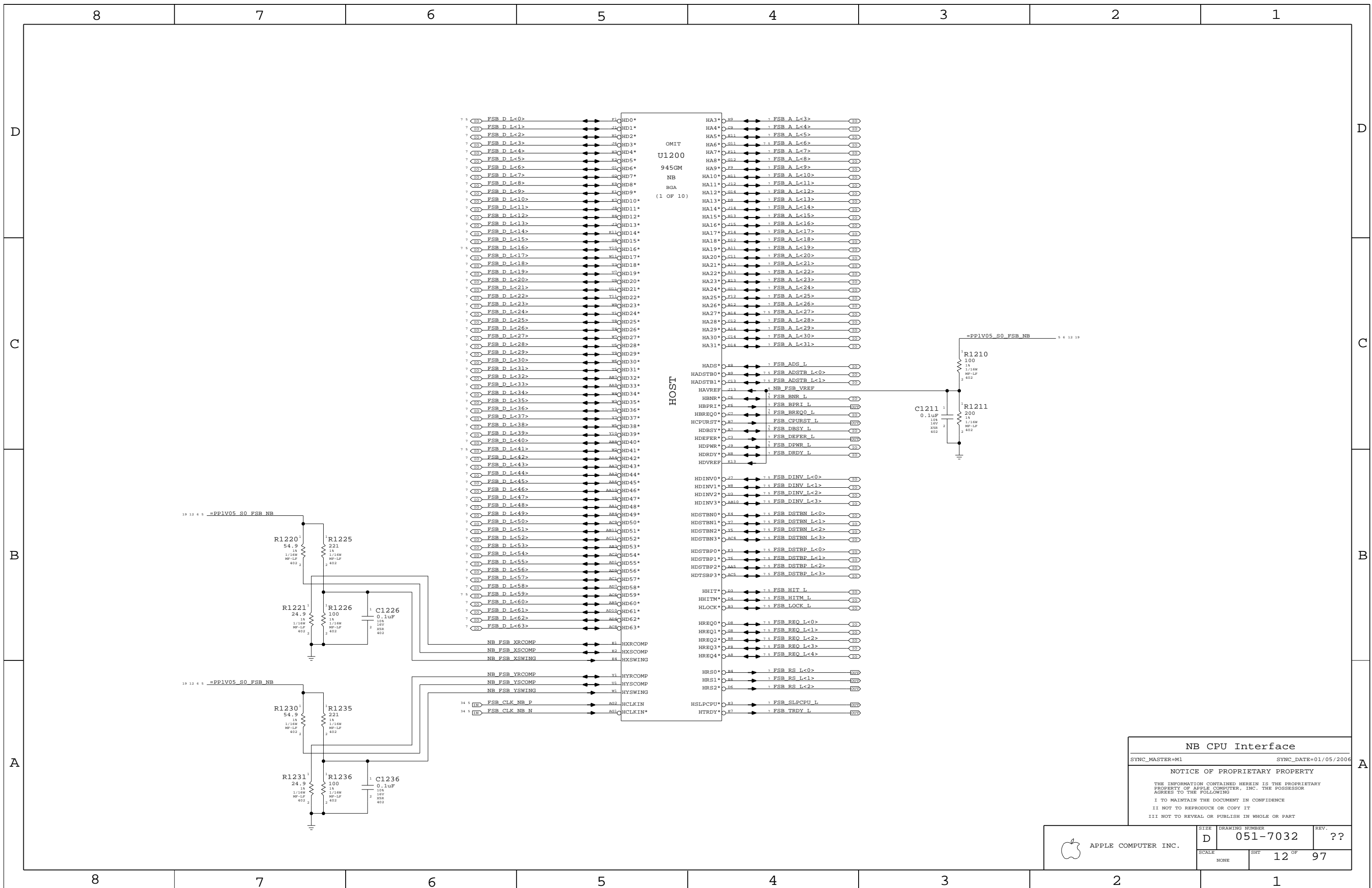
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

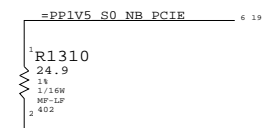
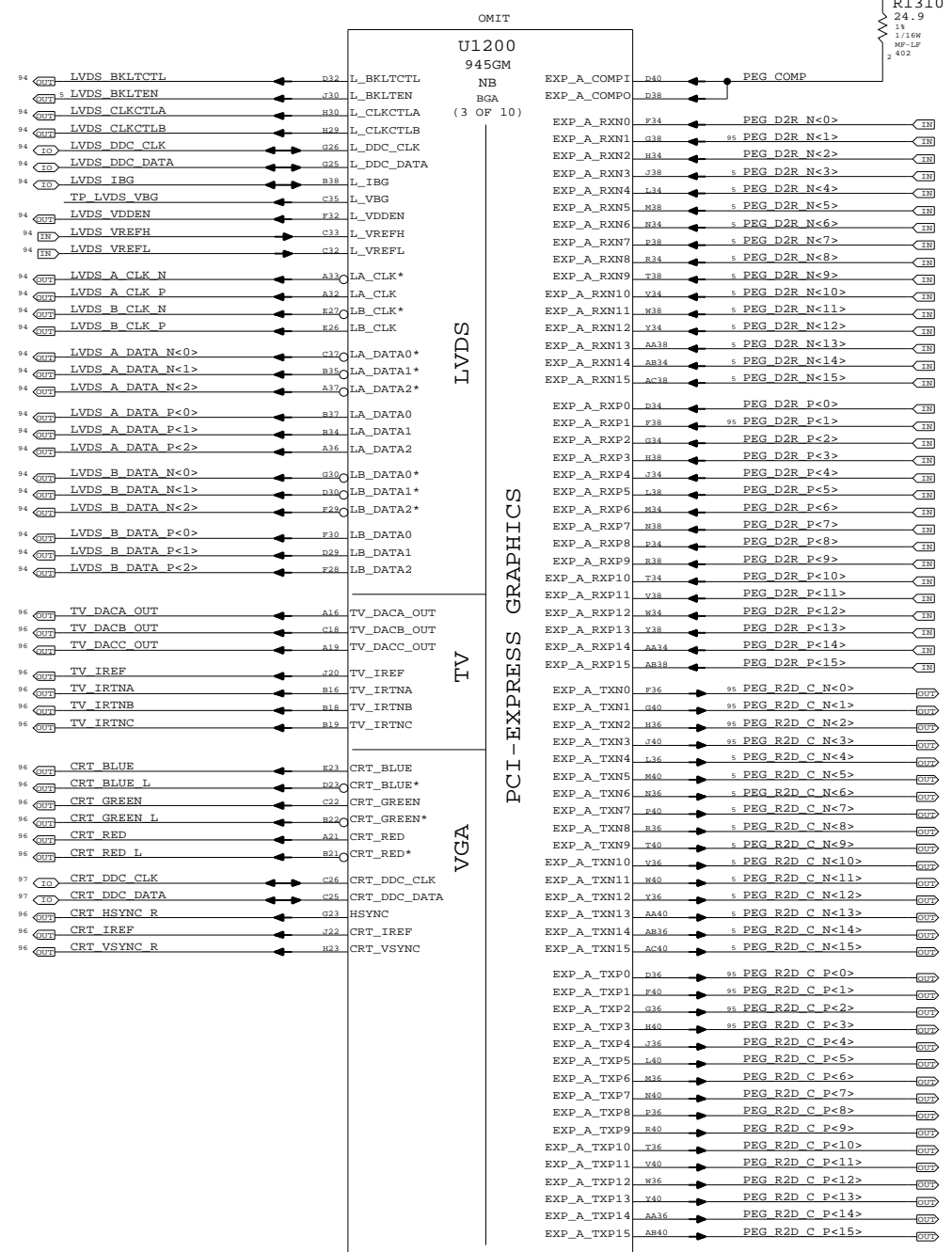
LVDS Disable
Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable
Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

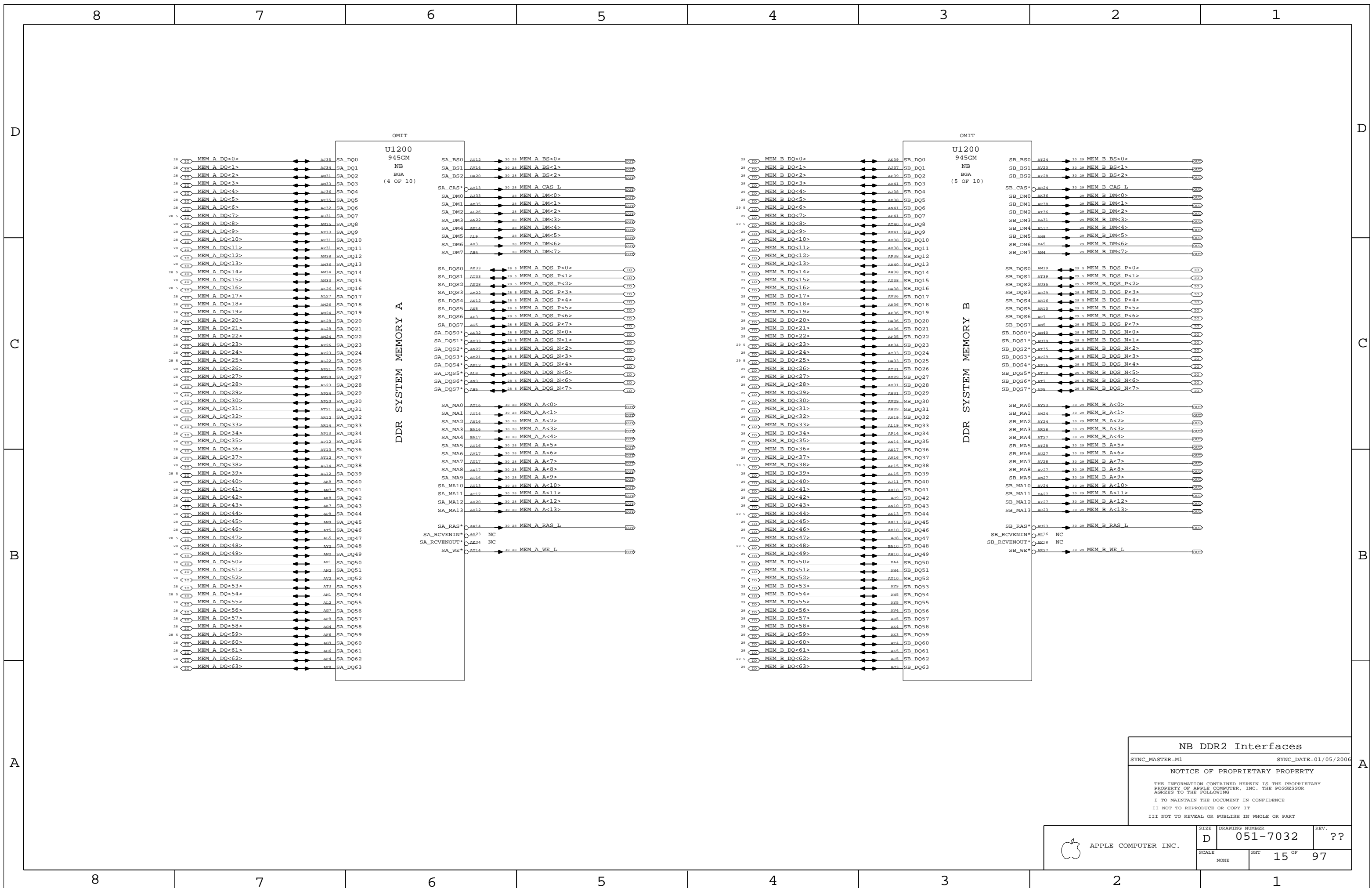
SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces
SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	13 OF 97	
NONE			



NB DDR2 Interfaces

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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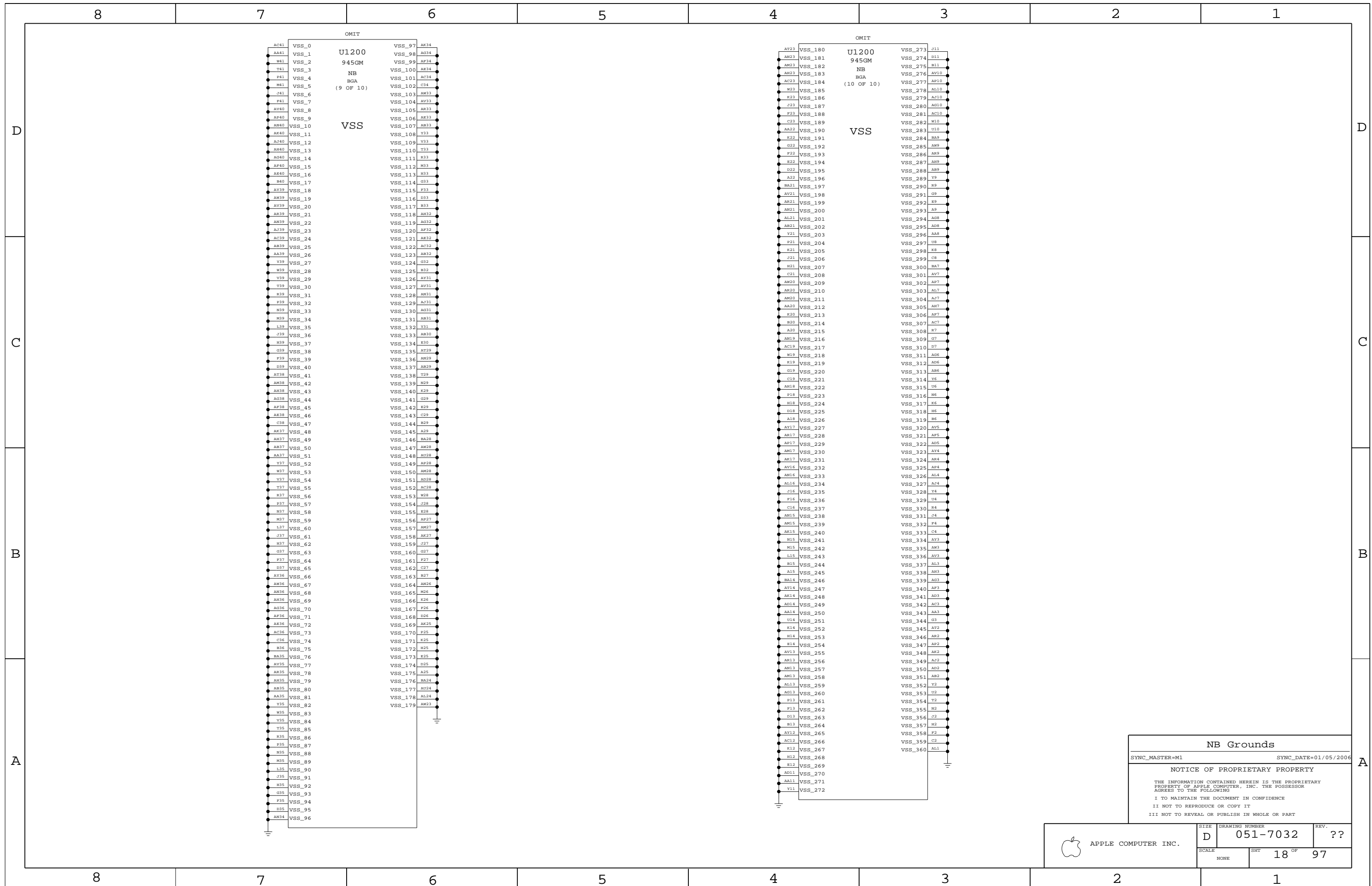
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	SCALE NONE	SHEET 15 OF 97	



NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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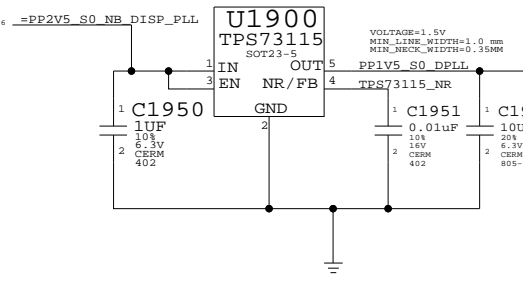
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 18 OF 97	

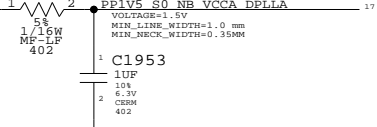
Power Interface
These are the power signals that leave the NB "block"

- =PP1V05_S0_FSB_NB 5 6 12
- =PPVCORE_S0_NB 6 16 19
- =PP1V05_S0_NB_VTT 6 17 19
- =PP1V5_S0_NB 6 19
- =PP1V5_S0_NB_PCIE 6 13
- =PP1V5_S0_NB_PLL 6 19
- =PP1V5_S0_NB_TVDAC 6 19
- =PP1V5_S0_NB_VCCD_HMPLL 6 17
- =PP1V5_S0_NB_VCCD_LVDS 6 17 19
- =PP1V5_S0_NB_VCCAUX 6 19
- =PP1V8_S3_MEM_NB 6 14 16 19
- =PP2V5_S0_NB_VCCSYNC 19 6
- =PP2V5_S0_NB_VCC_TLXVDS 6 17 19
- =PP2V5_S0_NB_VCCA_3GBG 6 17 19
- =PP2V5_S0_NB_VCCA_LVDS 6 17 19
- =PP3V3_S0_NB 6 14 20
- =PP3V3_S0_NB_VCC_HV 6 17 19
- =PP5V_S0_NB_TVDAC 6 19

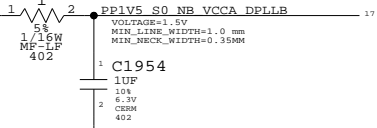
MCH DISPLAY PLL POWER LDO



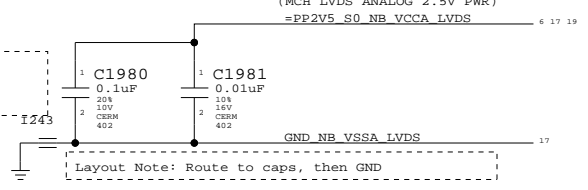
MCH VCCA_DPLL FILTER (MCH DISPLAY A PLL 1.5V PWR)



GMCH VCCA_DPLL_B FILTER (MCH DISPLAY B PLL 1.5V PWR)



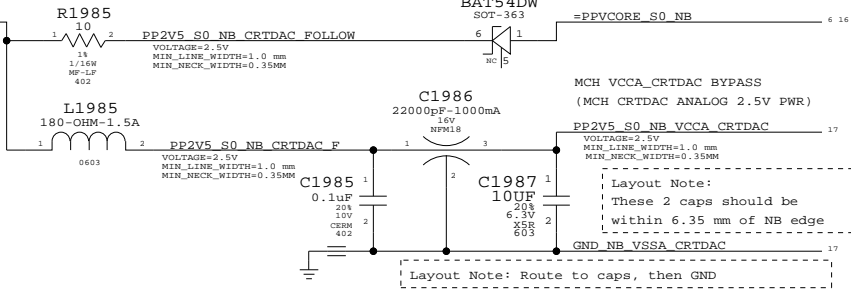
MCH VCCA_LVDS FILTER (MCH LVDS ANALOG 2.5V PWR)



Layout Note:
This 0.1uF cap should be within 5 mm of NB edge

Layout Note: Route to caps, then GND

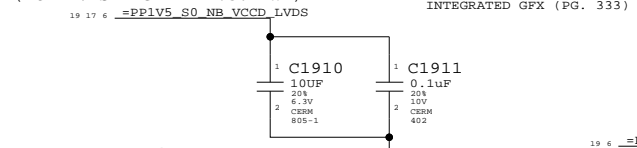
MCH VCCA_CRDACC BYPASS (MCH CRDACC ANALOG 2.5V PWR)



Layout Note:
These 2 caps should be within 6.35 mm of NB edge

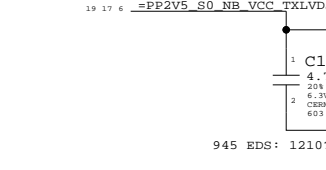
Layout Note: Route to caps, then GND

GMCH VCCD_LVDS BYPASS (MCH LVDS DIGITAL 1.5V PWR)

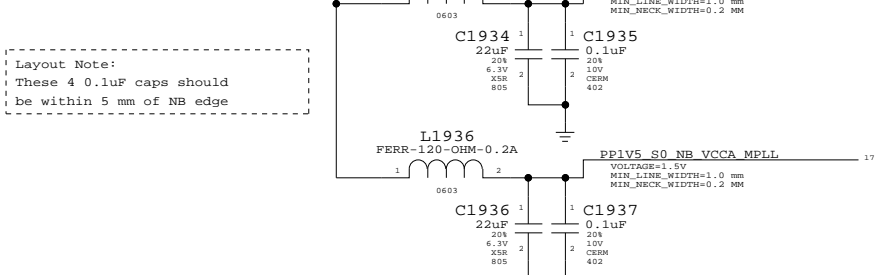


FILTERING REQUIRED FOR INTEGRATED GFX (PG. 333)

GMCH VCCD_TVDS BYPASS (MCH LVDS DIGITAL TX 2.5V PWR)

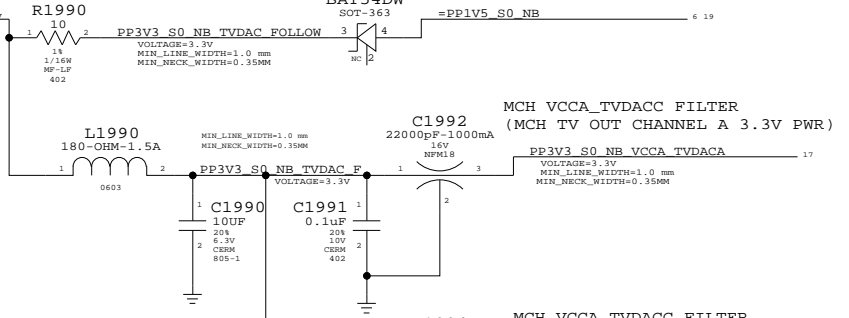


PP1V5_S0_NB_VTT



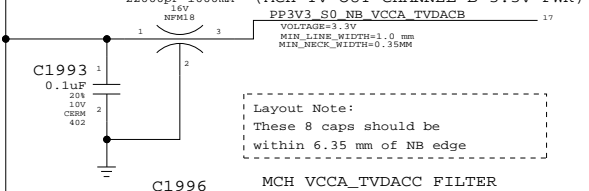
Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge

MCH VCCA_TVDACC FILTER (MCH TV OUT CHANNEL A 3.3V PWR)



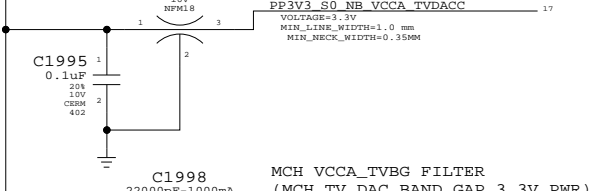
Layout Note:
These 2 caps should be within 6.35 mm of NB edge

MCH VCCA_TVDACC FILTER (MCH TV OUT CHANNEL B 3.3V PWR)

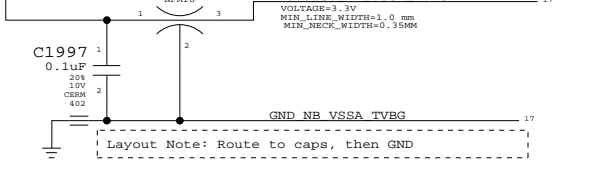


Layout Note:
These 8 caps should be within 6.35 mm of NB edge

MCH VCCA_TVDACC FILTER (MCH TV OUT CHANNEL C 3.3V PWR)

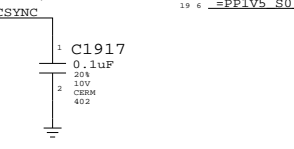


MCH VCCA_TVDBG FILTER (MCH TV DAC BAND GAP 3.3V PWR)

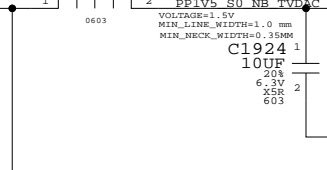


Layout Note: Route to caps, then GND

MCH VCCSYNC BYPASS (MCH H/V SYNC 2.5V PWR)

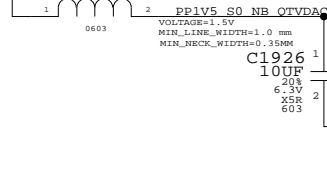


GMCH VCCD_TVDS FILTER (MCH TVDAC DEDICATED PWR 1.5V)



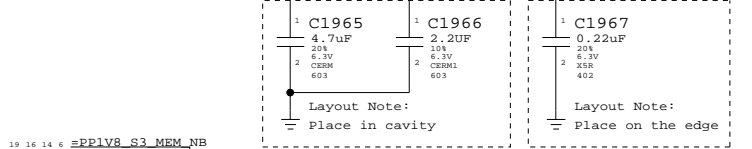
Layout Note:
PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR)



Layout Note:
10uF caps should be close to MCH on opposite side.

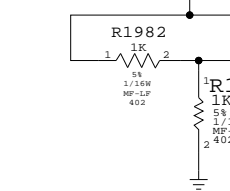
PP1V05_S0_NB_VTT



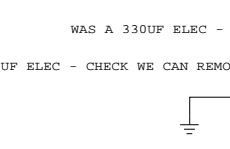
Layout Note:
Place in cavity

Layout Note:
Place on the edge

PP1V8_S3_MEM_NB



PPVCORE_S0_NB



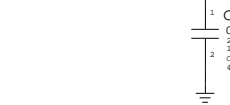
WAS A 330UF ELEC - CHECK WE CAN REMOVE

Layout Note:
Place L and C close to MCH

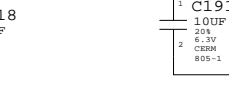
PP2V5_S0_NB_VCCA_3GBG



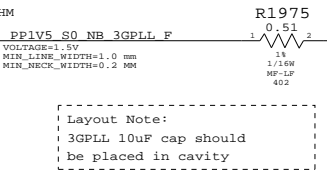
PP1V5_S0_NB_VCCAUX



PP3V3_S0_NB_VCC_HV

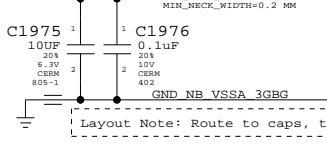


PP1V5_S0_NB_VCC3G



Layout Note:
3GPLL 10uF cap should be placed in cavity

PP1V5_S0_NB_VCCA_3GPLL



Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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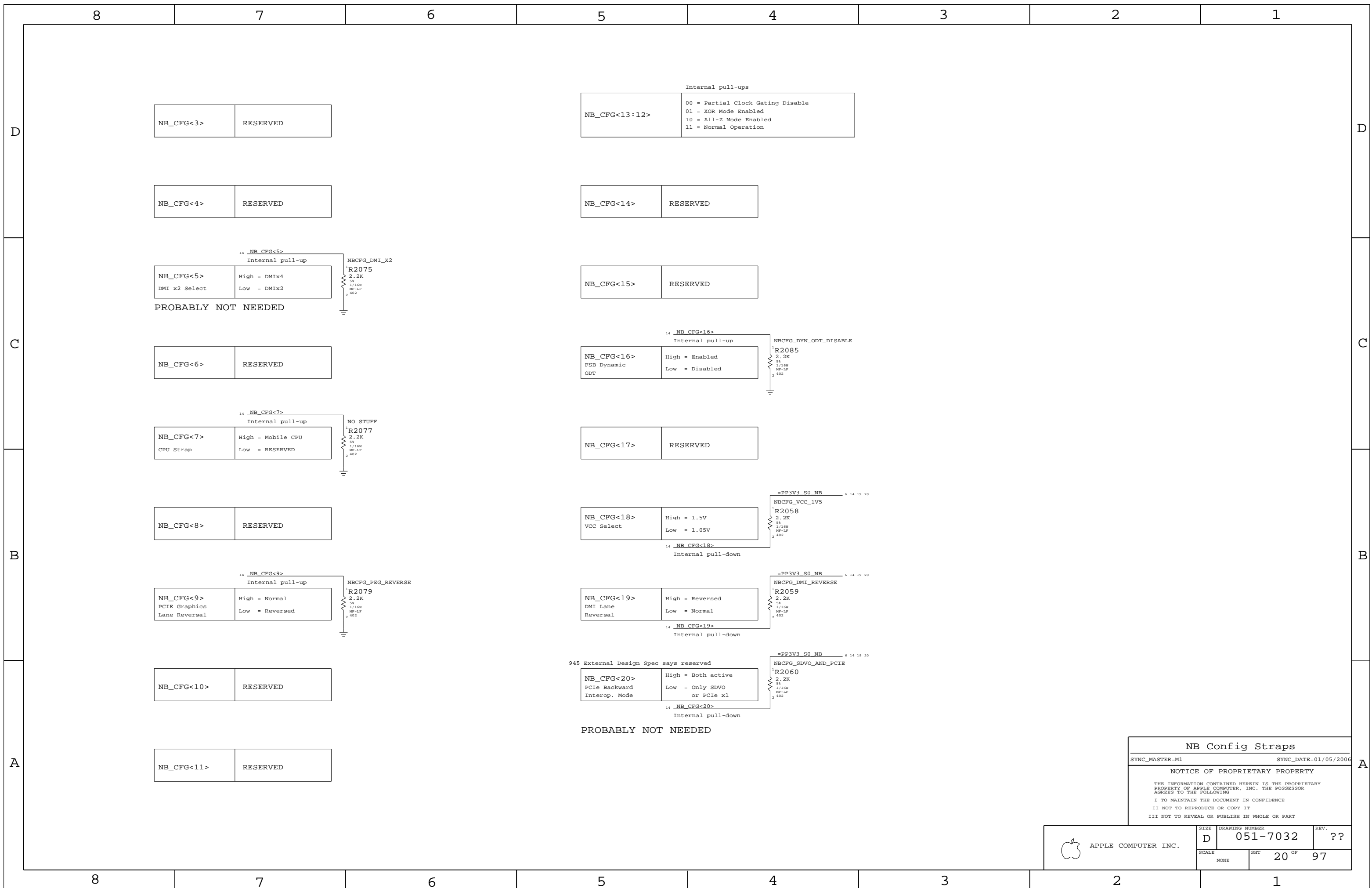
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SCALE NONE	SHT 19 OF 97	REV. ??
		D 051-7032



APPLE COMPUTER INC.



NB Config Straps

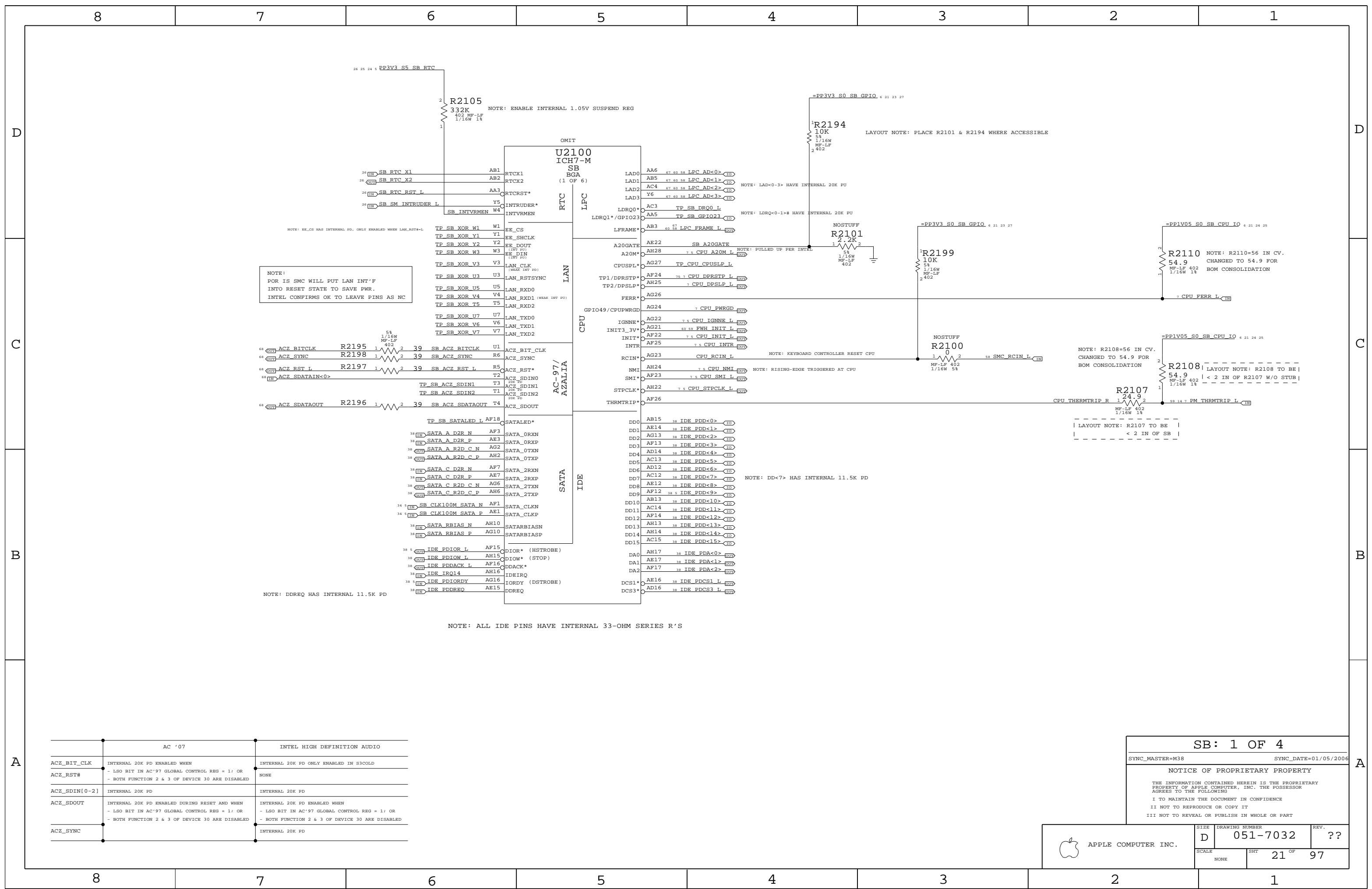
SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHT 20 OF	97



NOTE:
 POR IS SMC WILL PUT LAN INT'F
 INTO RESET STATE TO SAVE PWR.
 INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

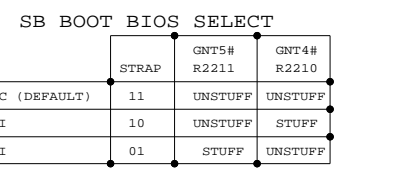
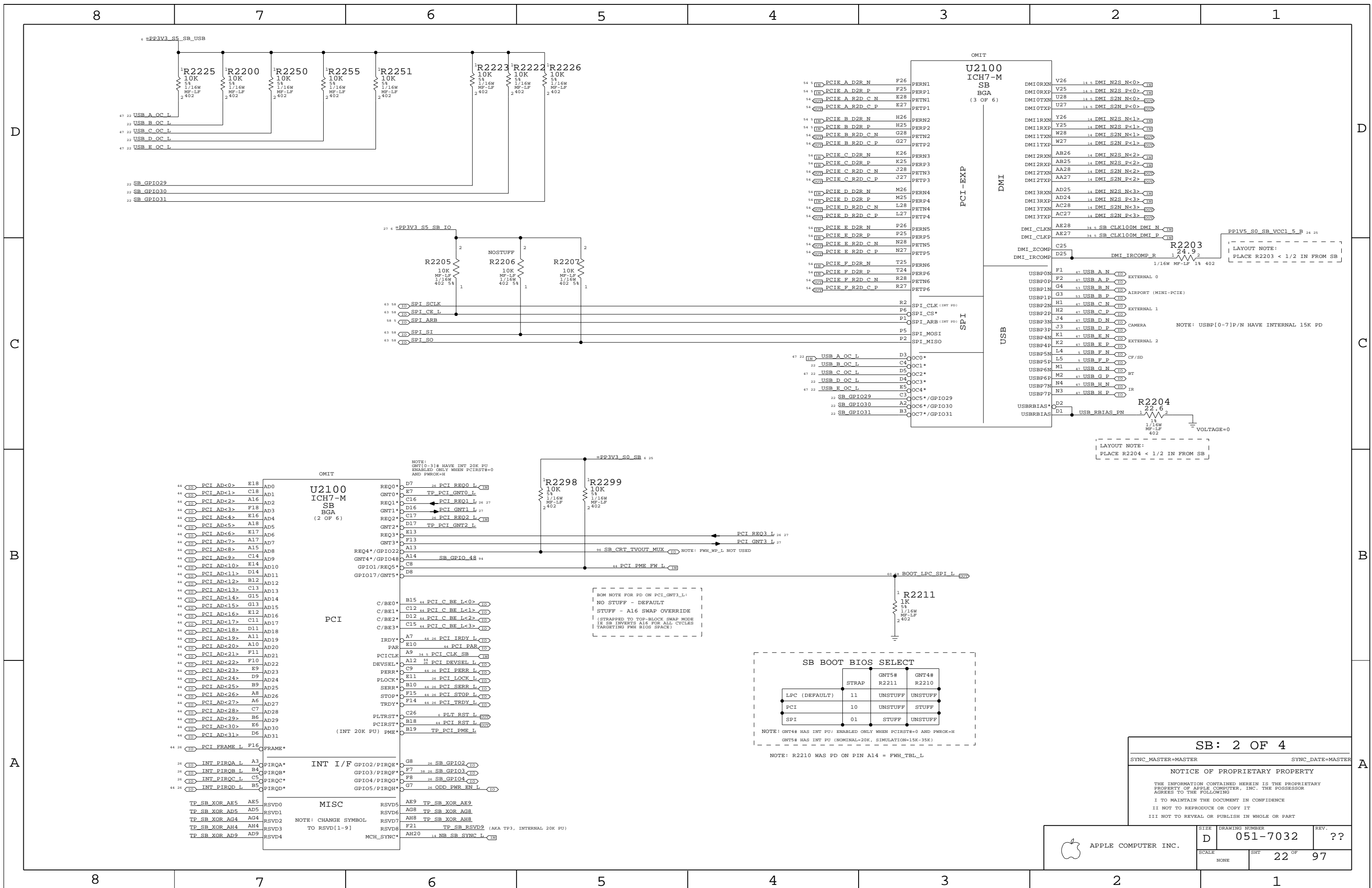
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7032	??
SCALE	SHT	21 OF 97	
NONE			



SB: 2 OF 4

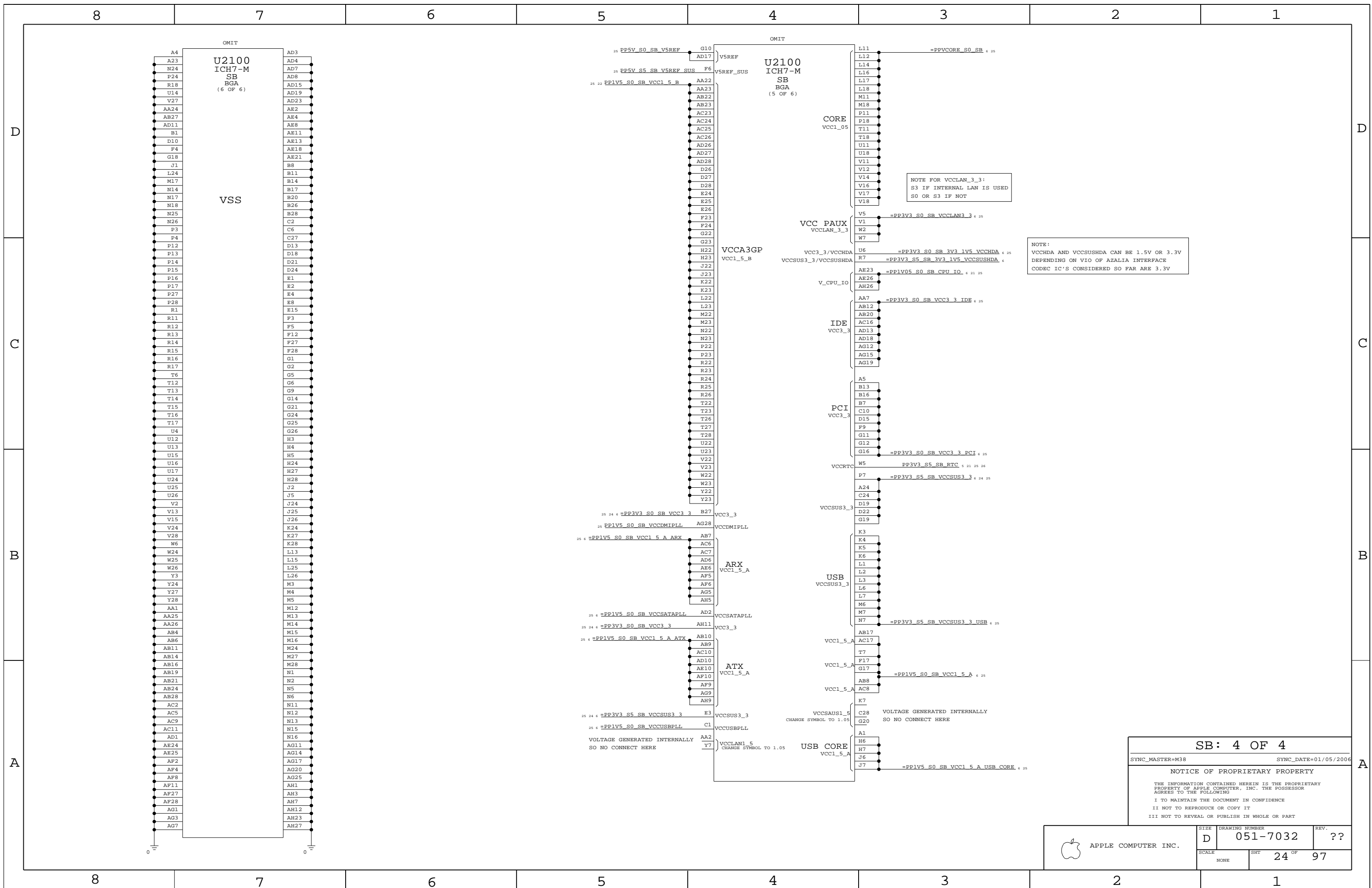
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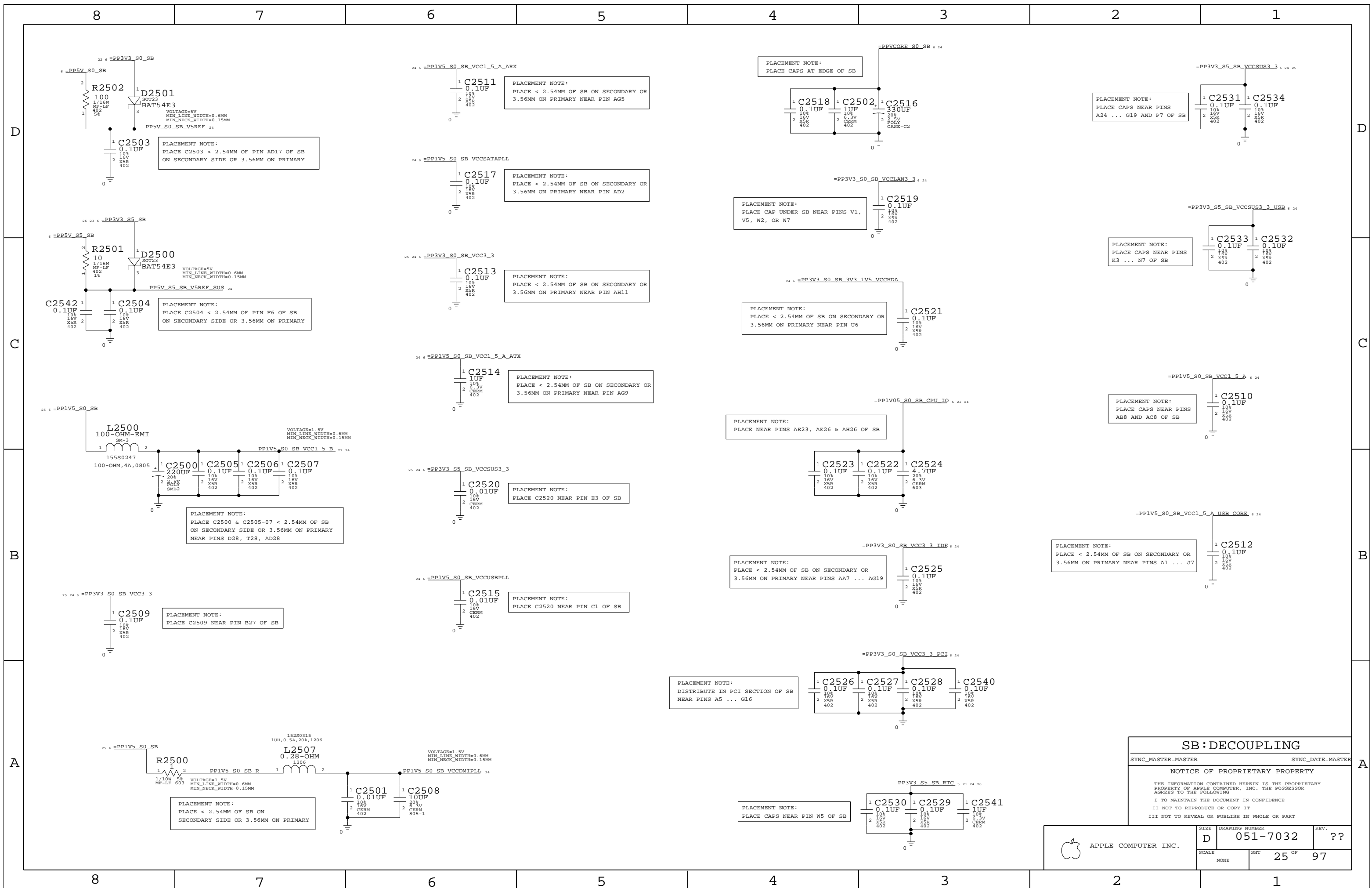
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	NONE	051-7032	??
SIZE		SHEET	
D		22 OF 97	





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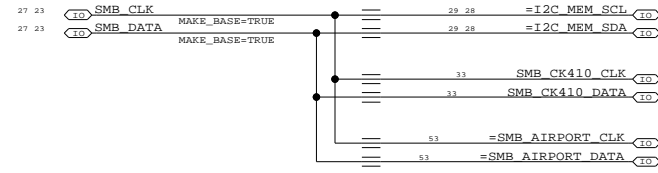
2

1

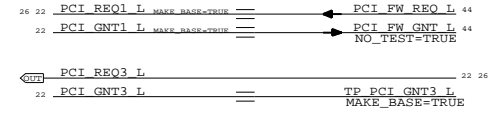
D

D

SB I2C BUSSES

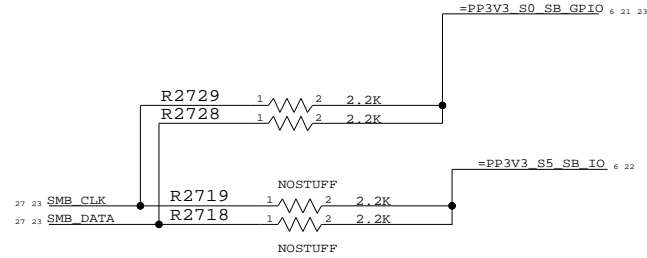


PCI CONTROL



C

C



B

B

A

A

SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	??
SCALE	SHT	27 OF 97	
NONE			

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Page Notes

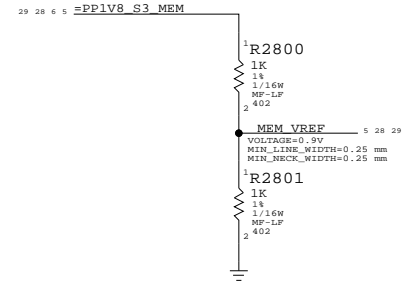
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

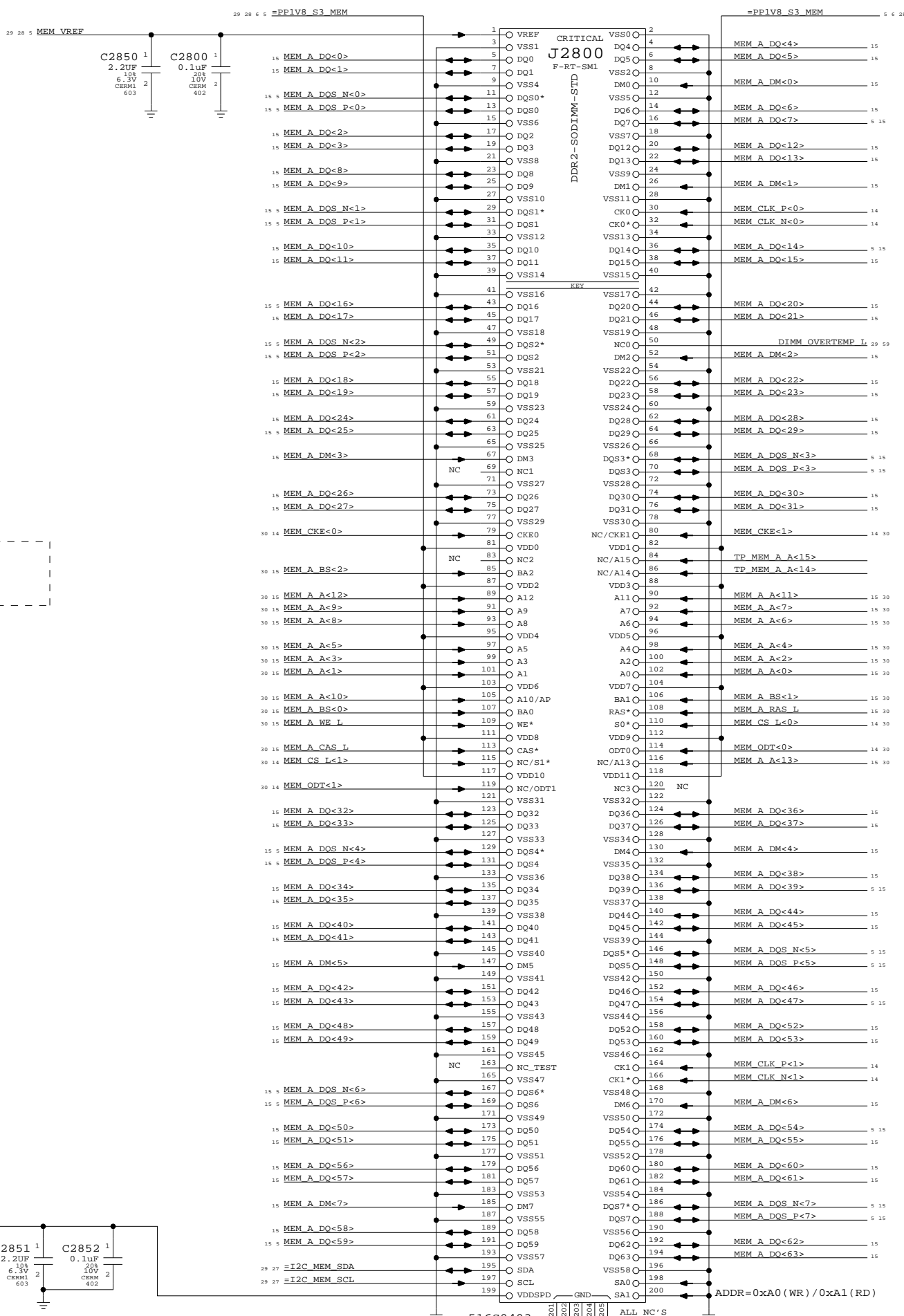
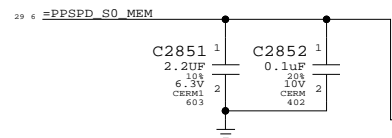
BOM options provided by this page:
 (NONE)

DDR2 VRef

One 0.1uF per connector

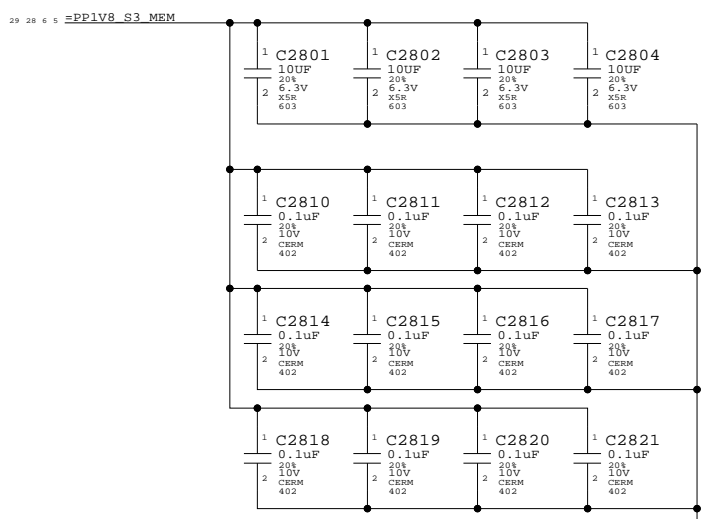


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
 (See Capell Valley pg 47)



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	28 OF 97	
NONE			

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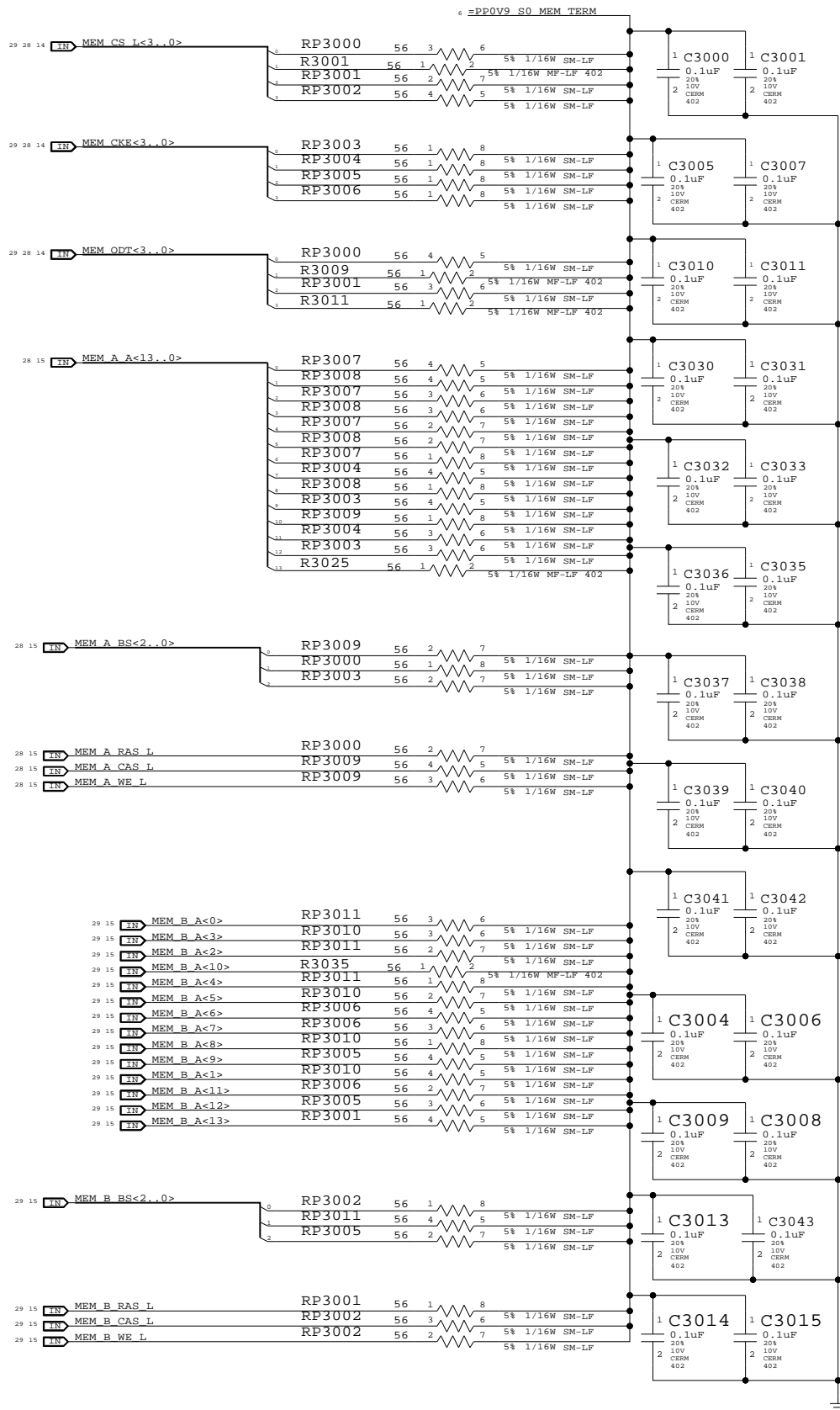
4

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1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	OF	
NONE	30	97	

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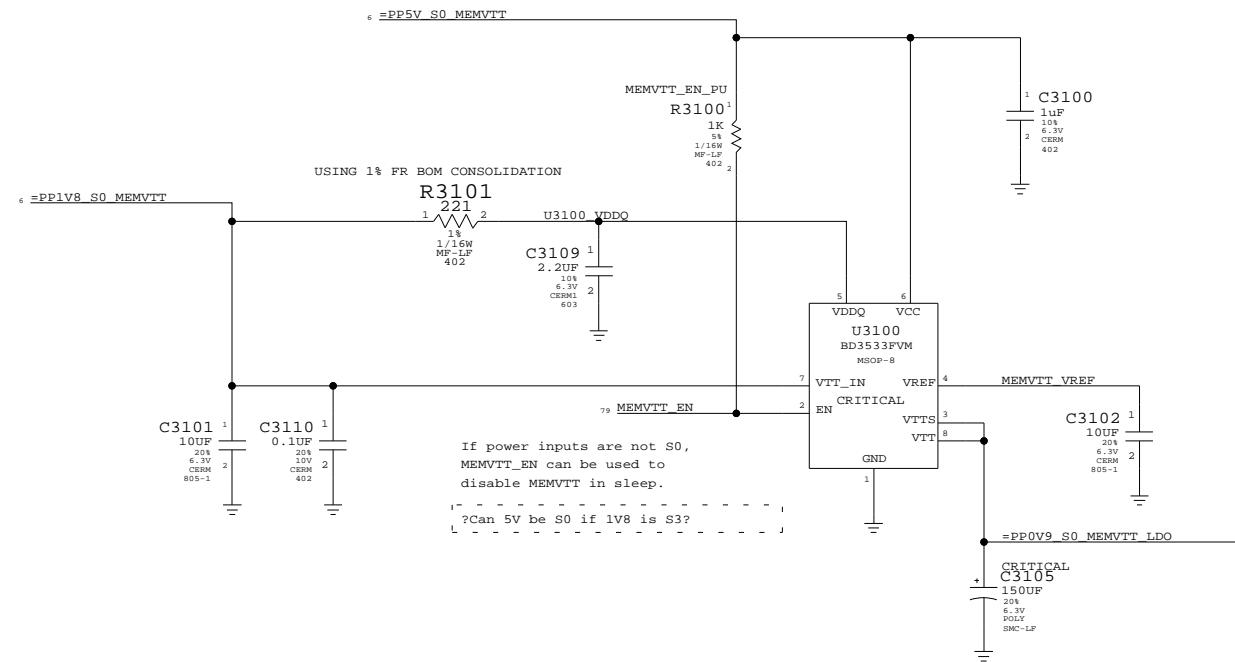
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

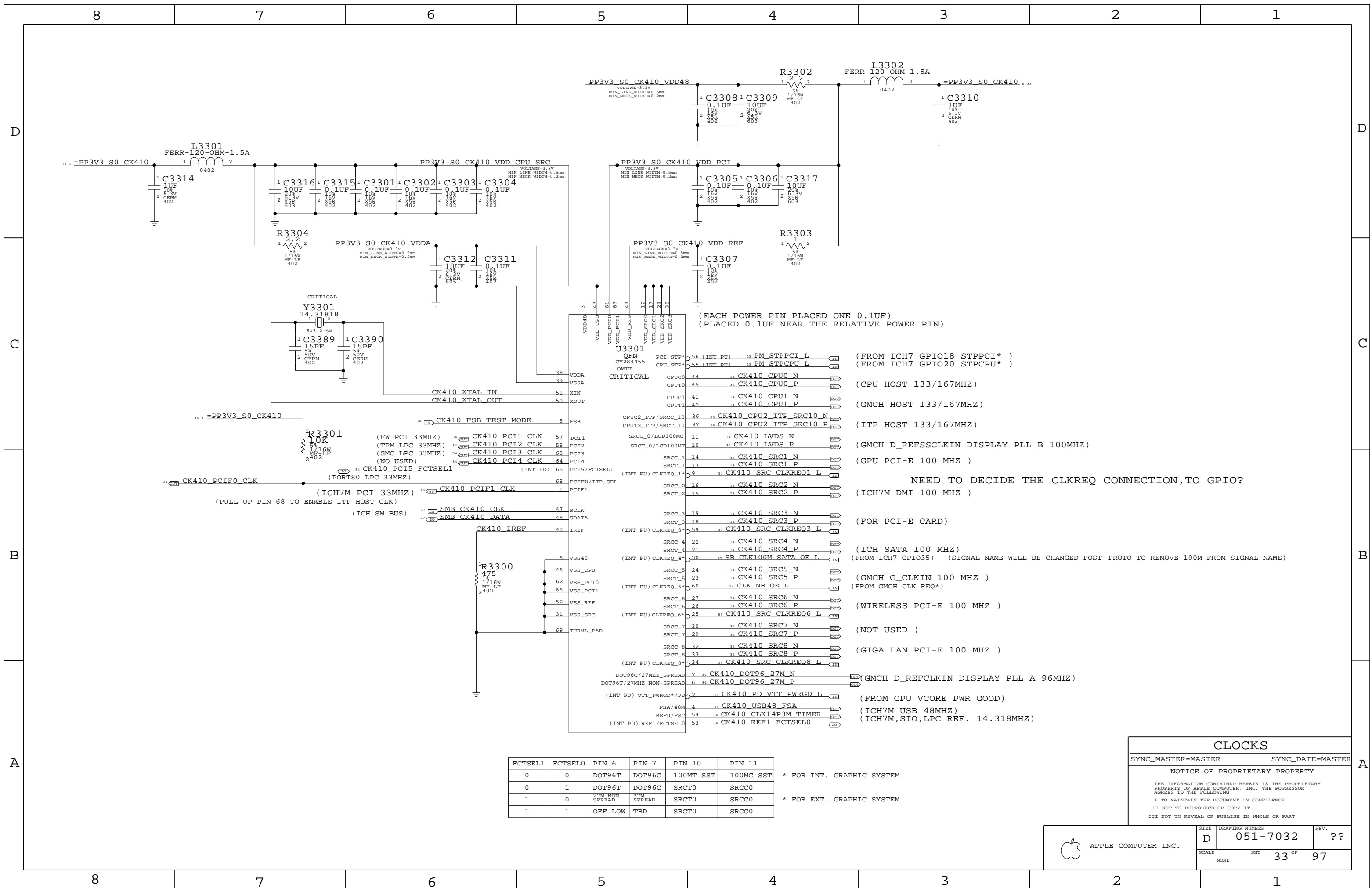
SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	??
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI*)
(FROM ICH7 GPIO20 STPCPU*)

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ)

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

(ICH7M DMI 100 MHZ)

(FOR PCI-E CARD)

(ICH SATA 100 MHZ)

(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G_CLKIN 100 MHZ)

(FROM GMCH CLK_REQ*)

(WIRELESS PCI-E 100 MHZ)

(NOT USED)

(GIGA LAN PCI-E 100 MHZ)

(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

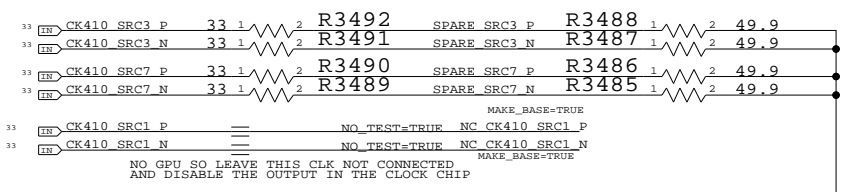
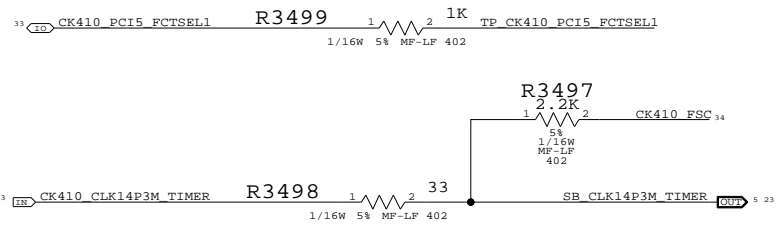
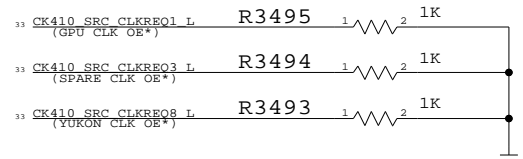
* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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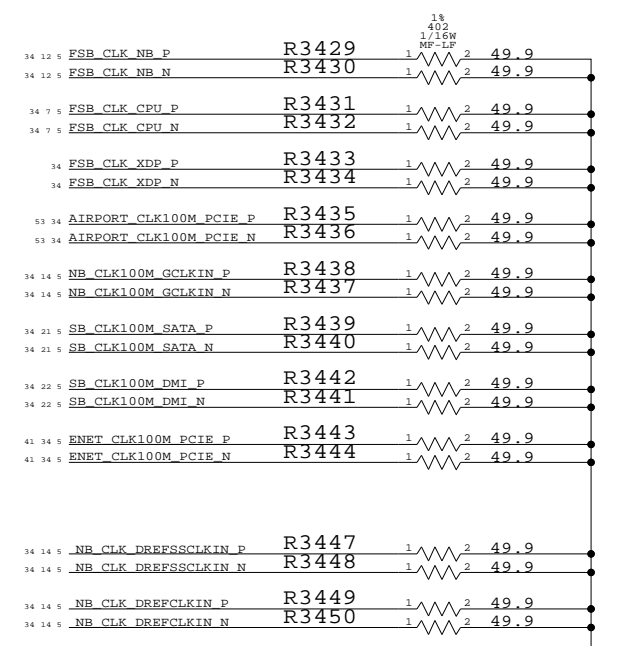
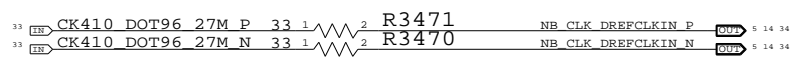
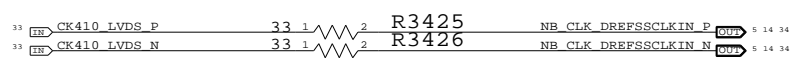
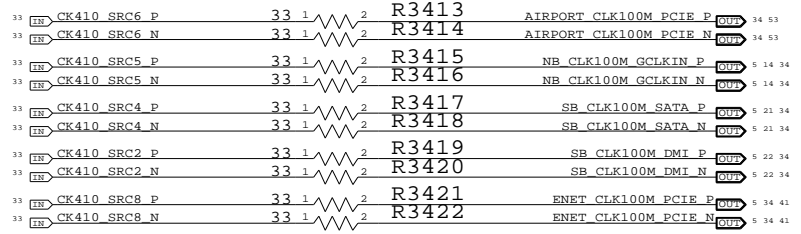
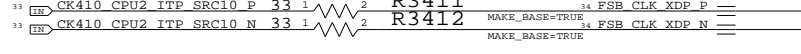
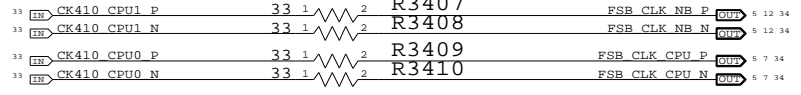
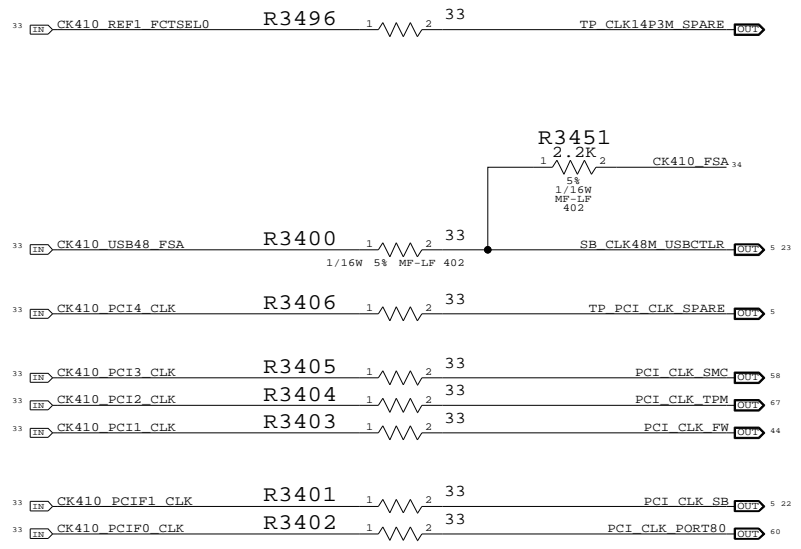
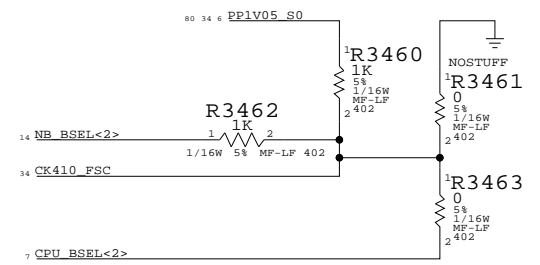
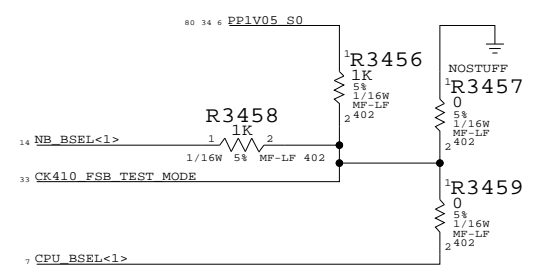
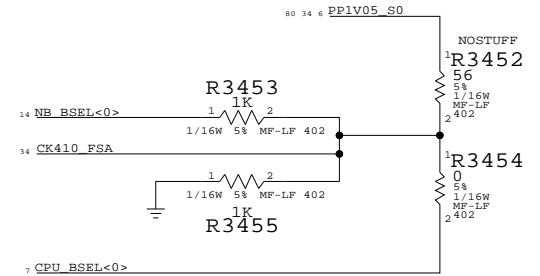
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	33 OF 97	
NONE			

NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457
533MHZ (133MHZ CPU CLK)	R3452 R3461	R3458 R3459
667MHZ (166MHZ CPU CLK)	R3452 R3461	R3458 R3459



CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

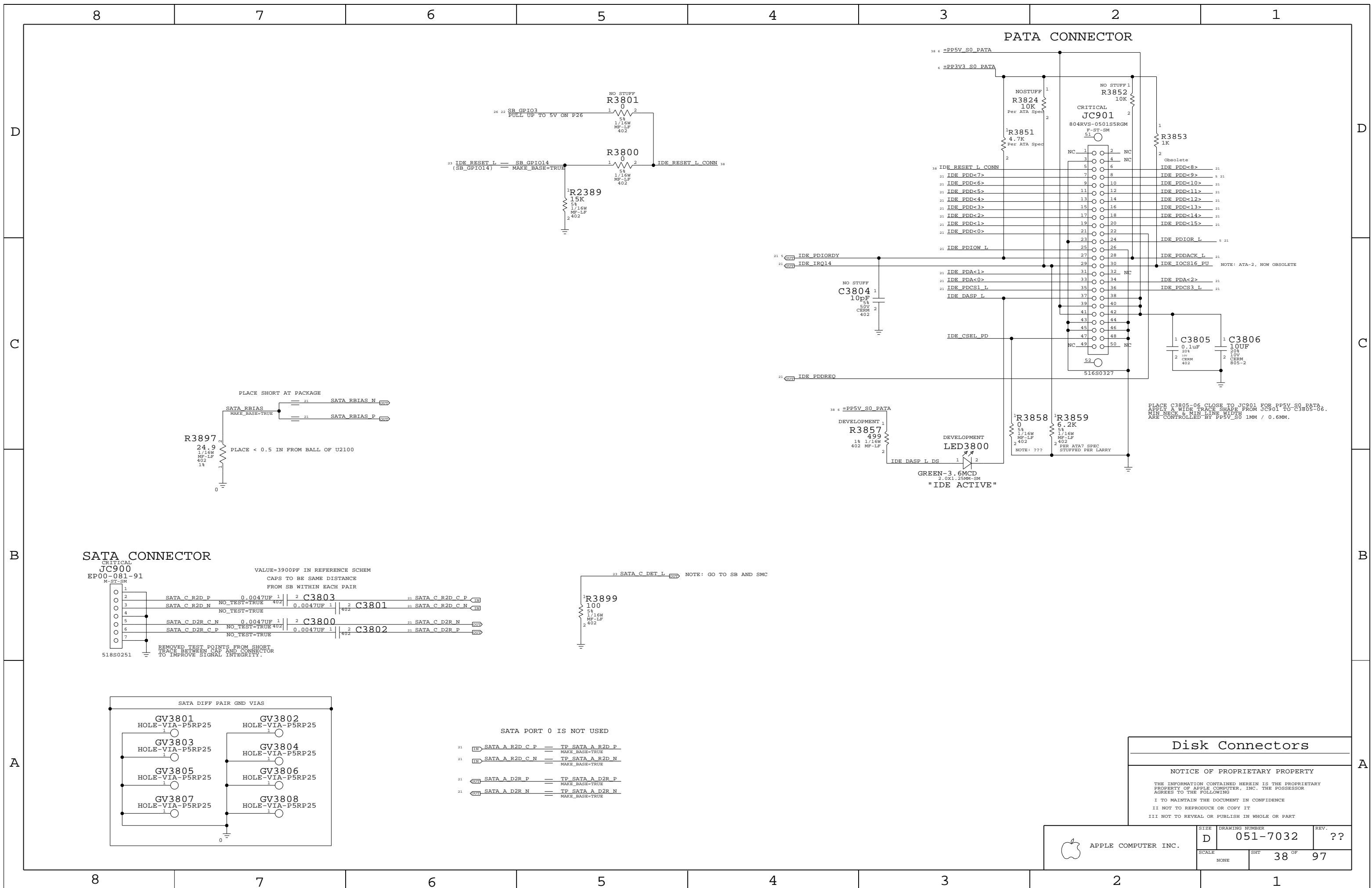
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	34 OF 97	
NONE			



PATA CONNECTOR

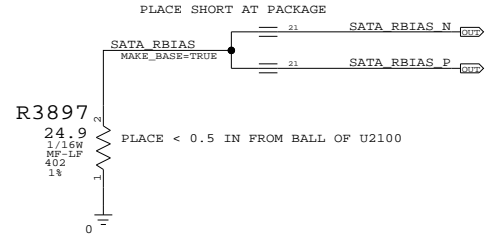
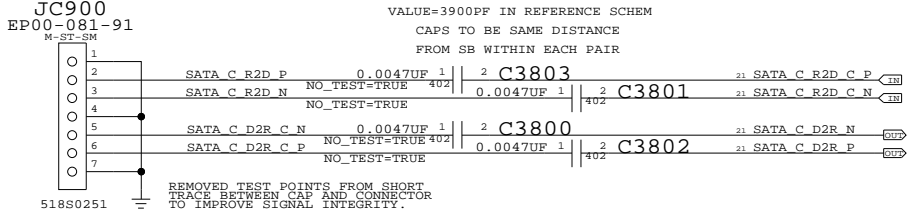
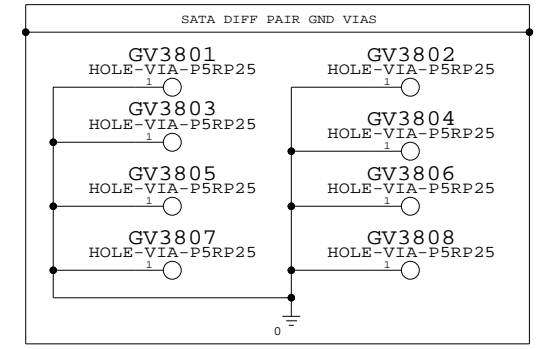
Disk Connectors

SATA CONNECTOR

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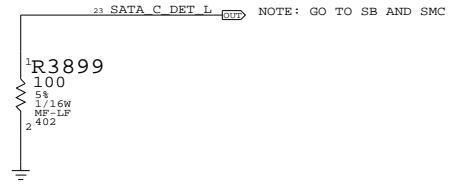
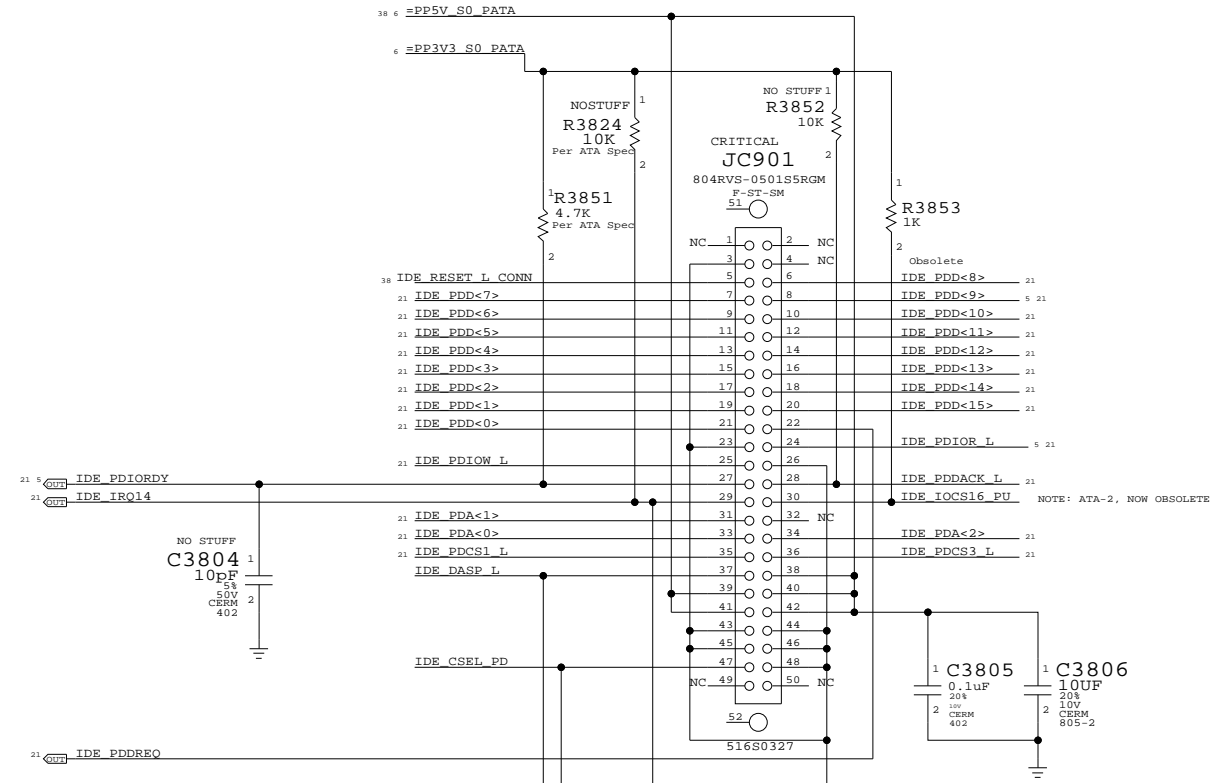
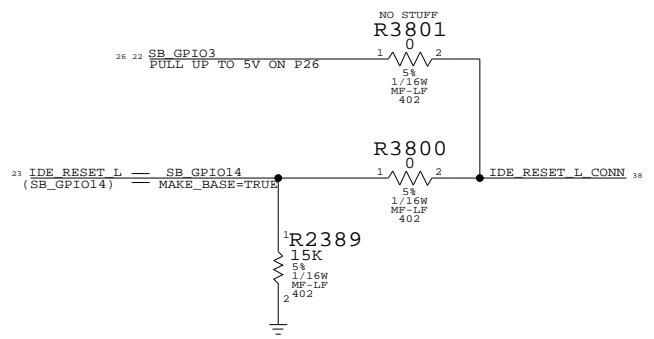
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	38 OF 97	
NONE			

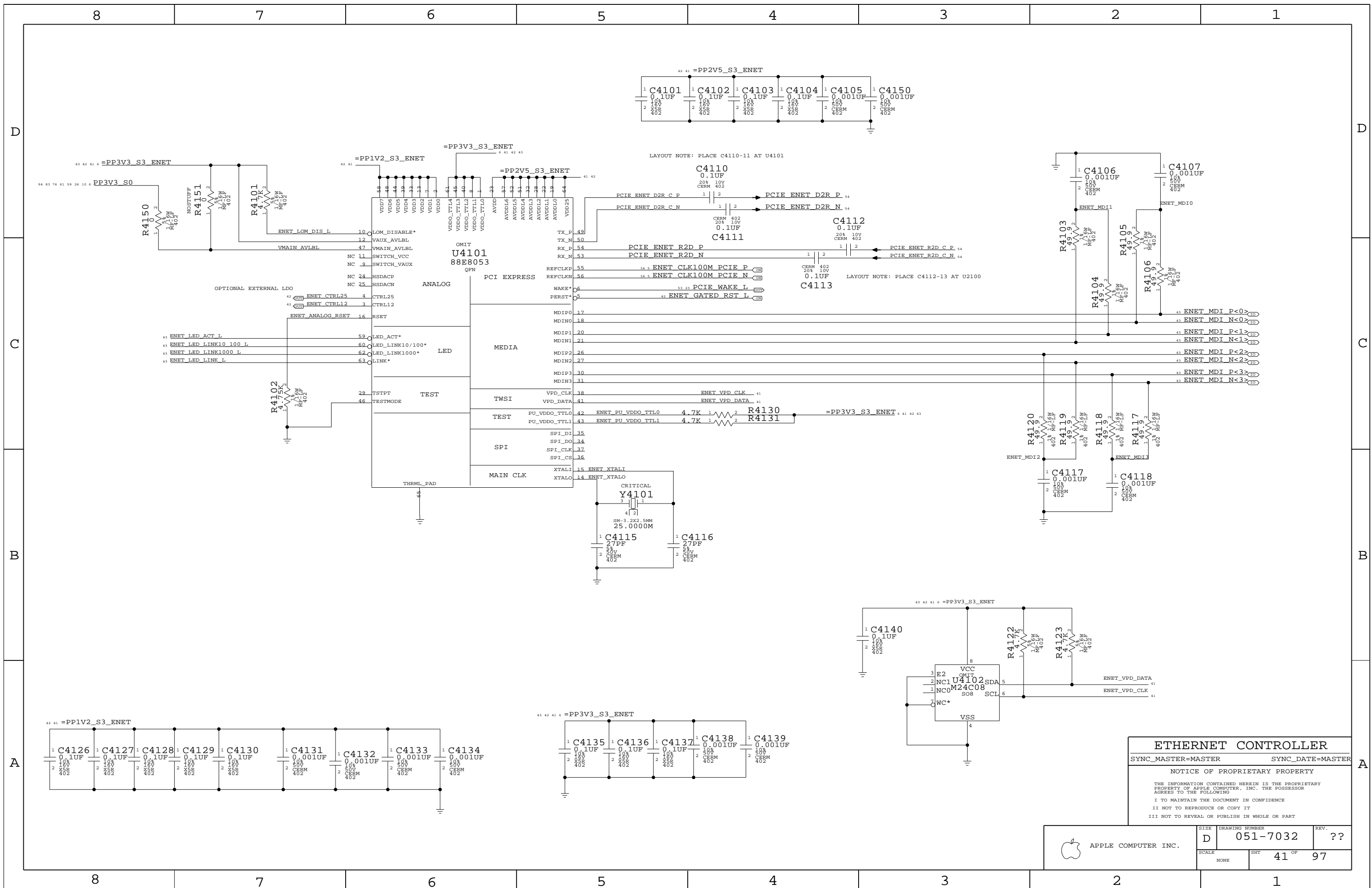
- SATA PORT 0 IS NOT USED
- TP SATA A R2D C P == MAKE_BASE=TRUE
 - TP SATA A R2D C N == MAKE_BASE=TRUE
 - TP SATA A D2R P == MAKE_BASE=TRUE
 - TP SATA A D2R N == MAKE_BASE=TRUE



PLACE C3805-06 CLOSE TO JC901 FOR PP5V_S0_PATA. APPLY A WIDE TRACE SHAPE FROM JC901 TO C3805-06. MIN NECK & MIN LINE WIDTHS ARE CONTROLLED BY PP5V_S0 1MM / 0.6MM.

DEVELOPMENT LED3800 GREEN-3.6MCD 2.0X1.25MM-SM "IDE ACTIVE"





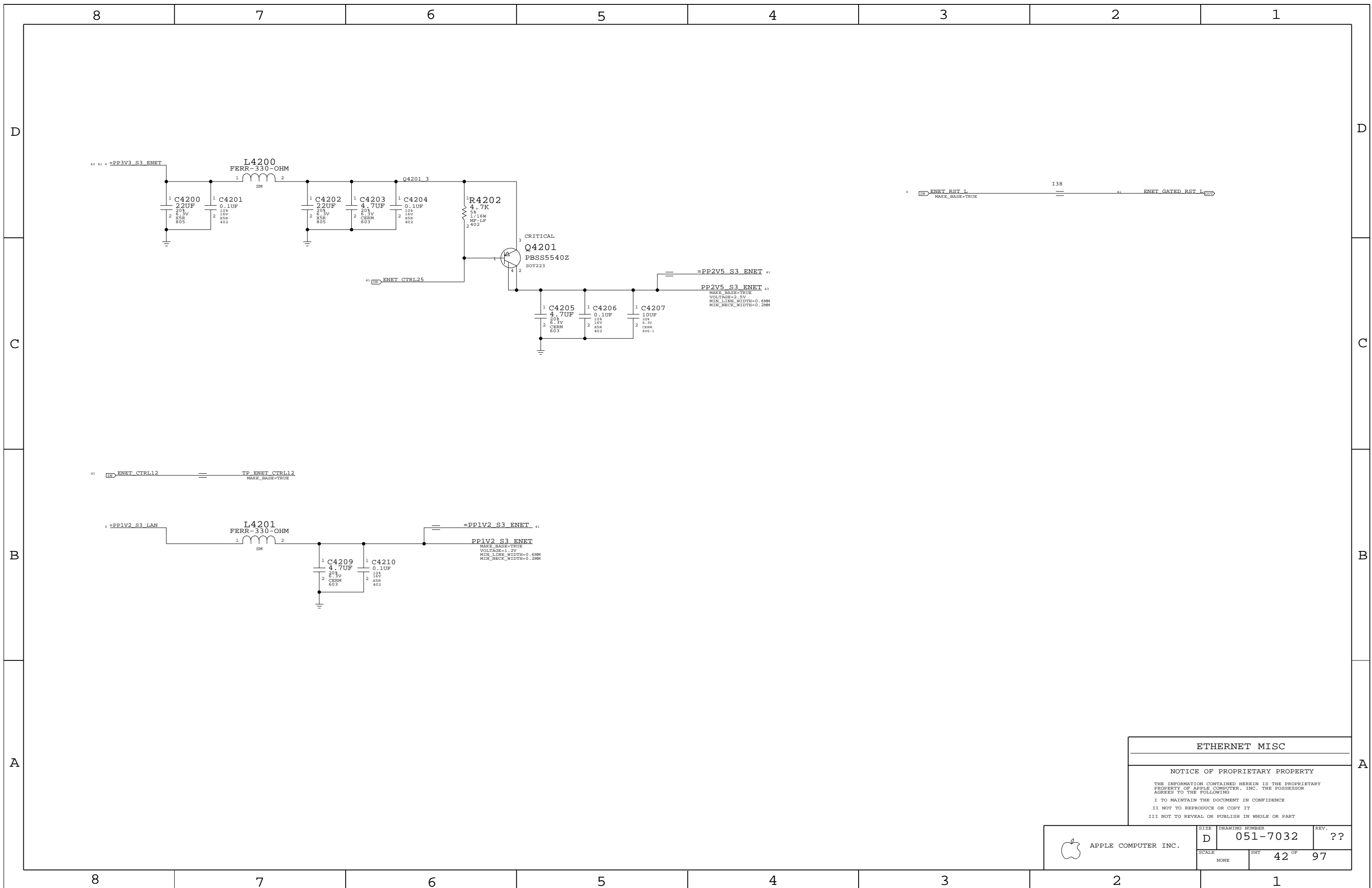
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 41 OF 97	



ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

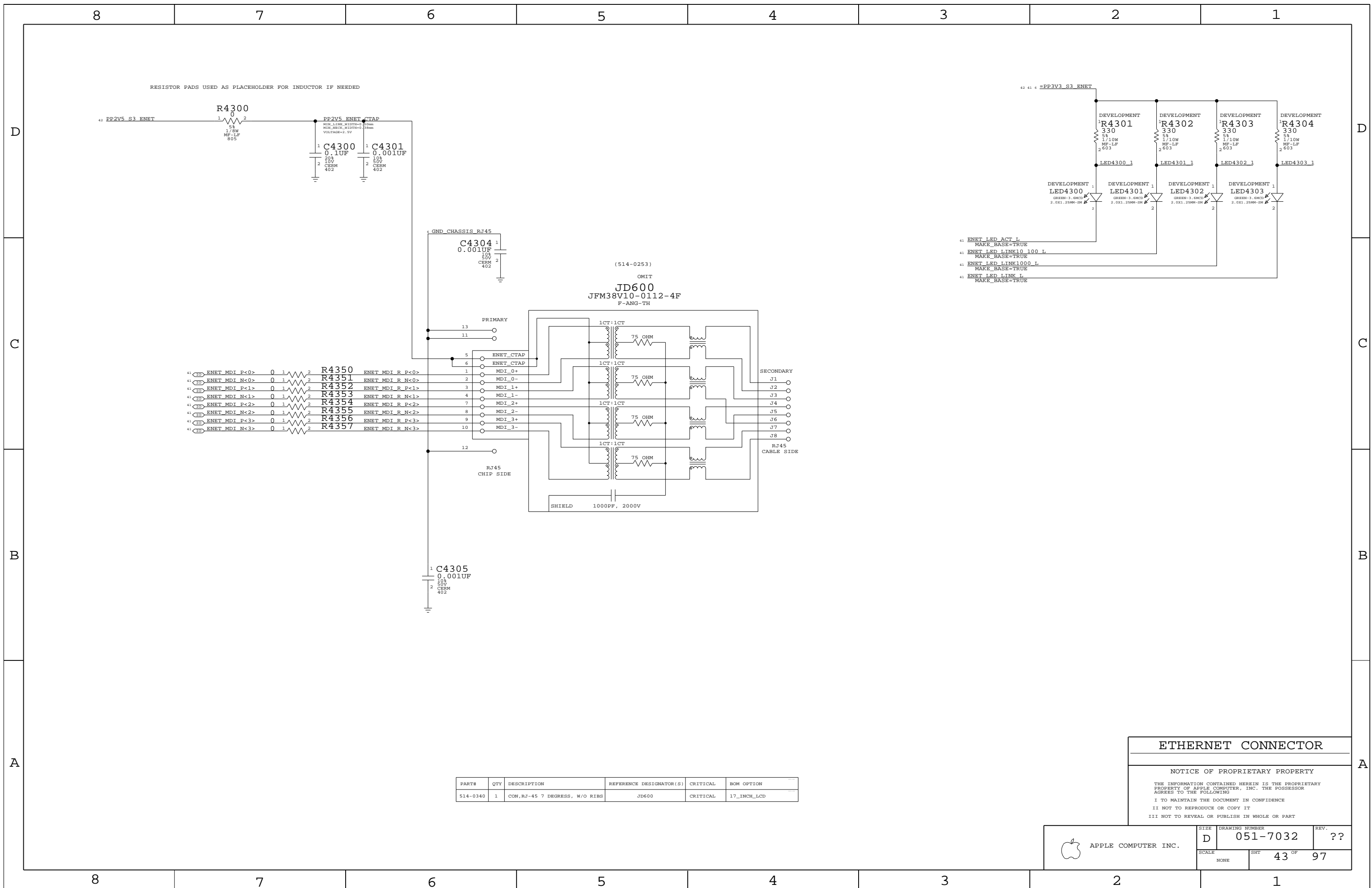
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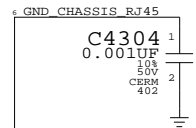
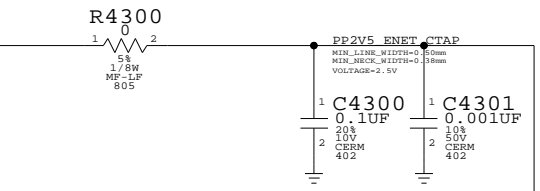
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

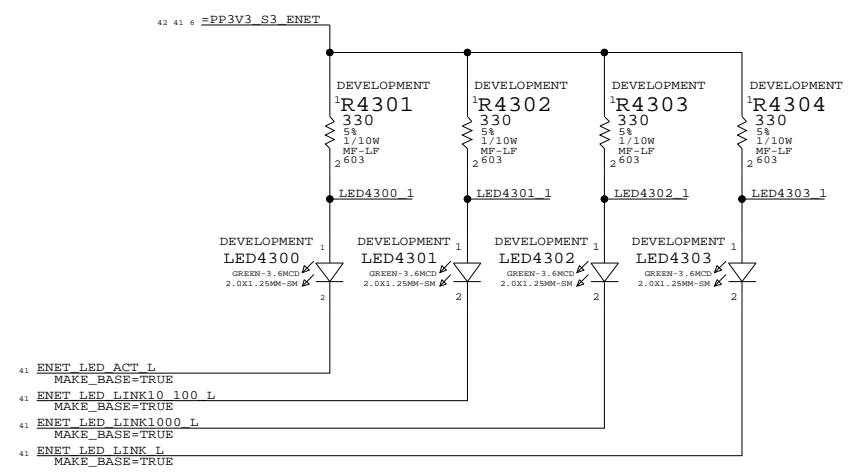
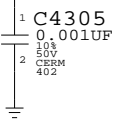
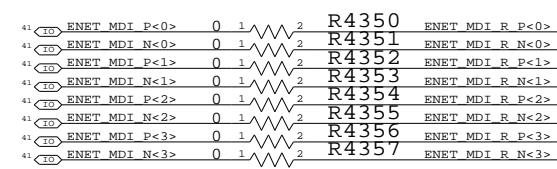
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 42 OF 97	



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0340	1	CON,RJ-45 7 DEGRESS, W/O RIBS	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

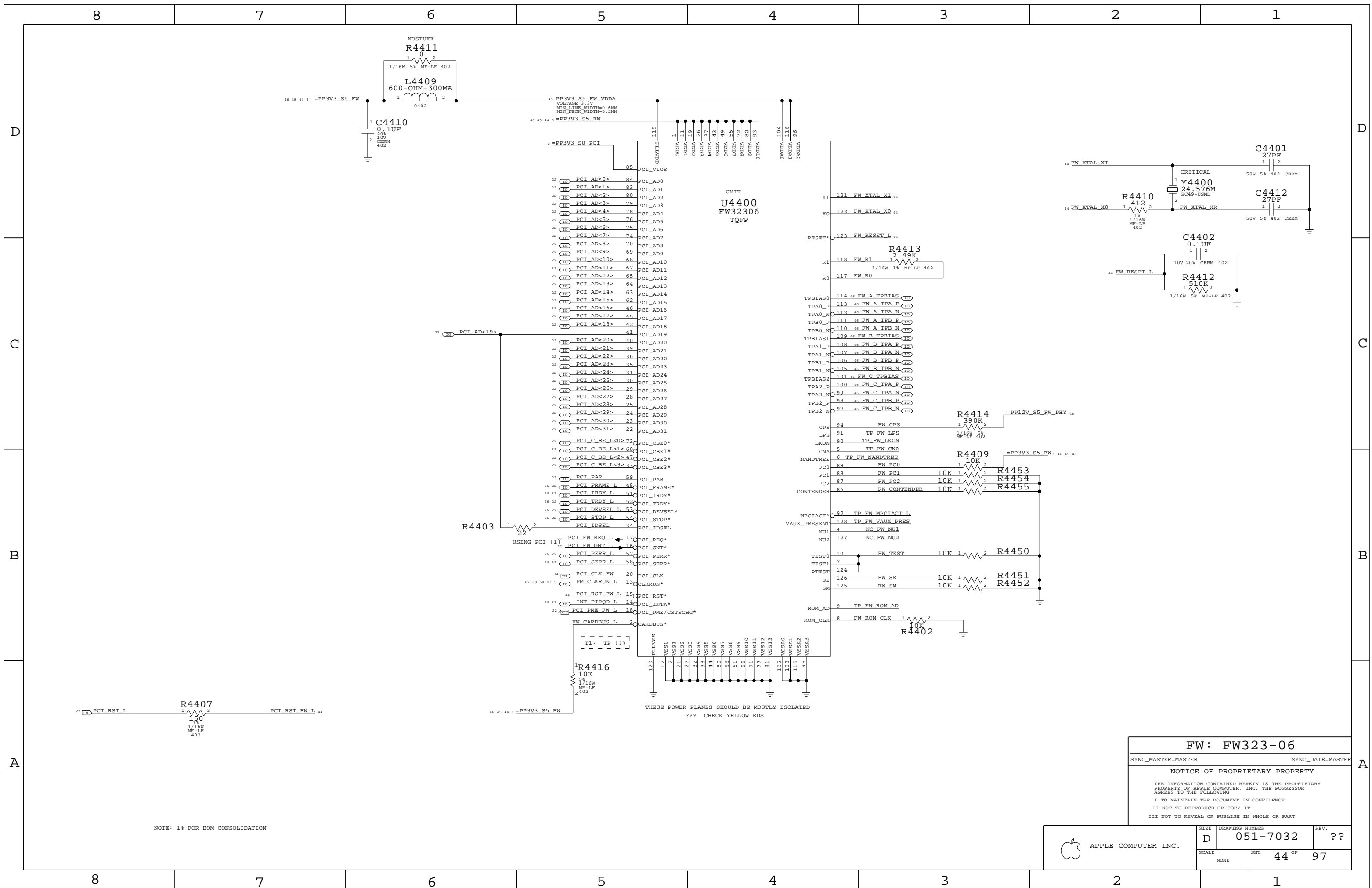
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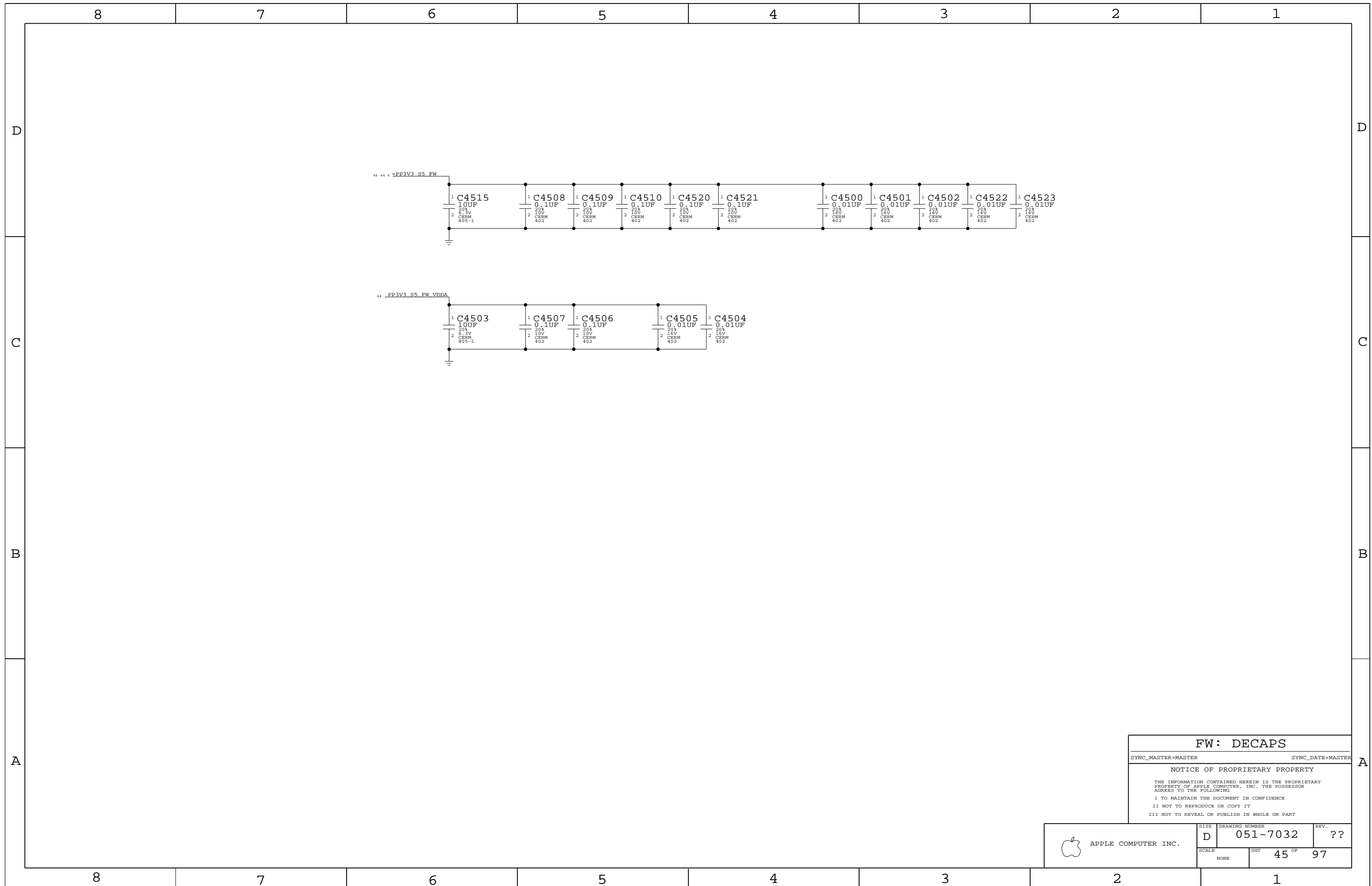
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	43 OF 97	
NONE			



NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	NONE	SHT	44 OF 97



FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER


NOTICE OF PROPRIETARY PROPERTY

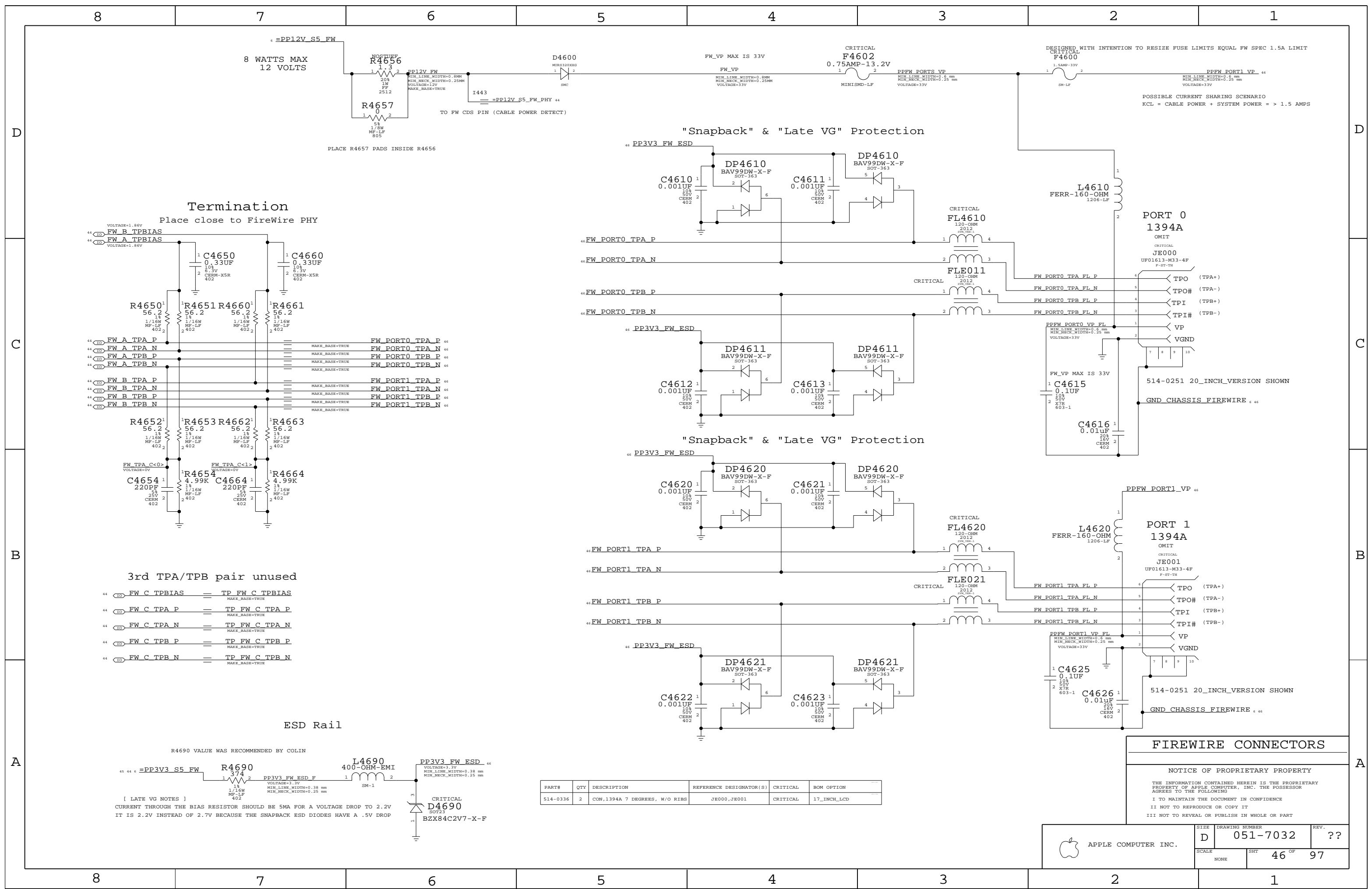
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	45 OF 97	
NONE			



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

FIREWIRE CONNECTORS

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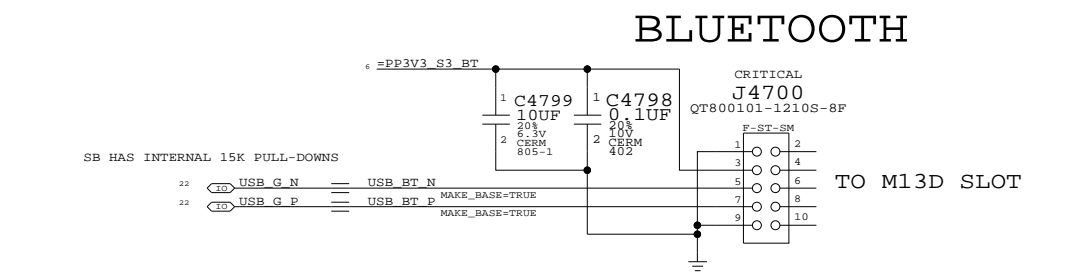
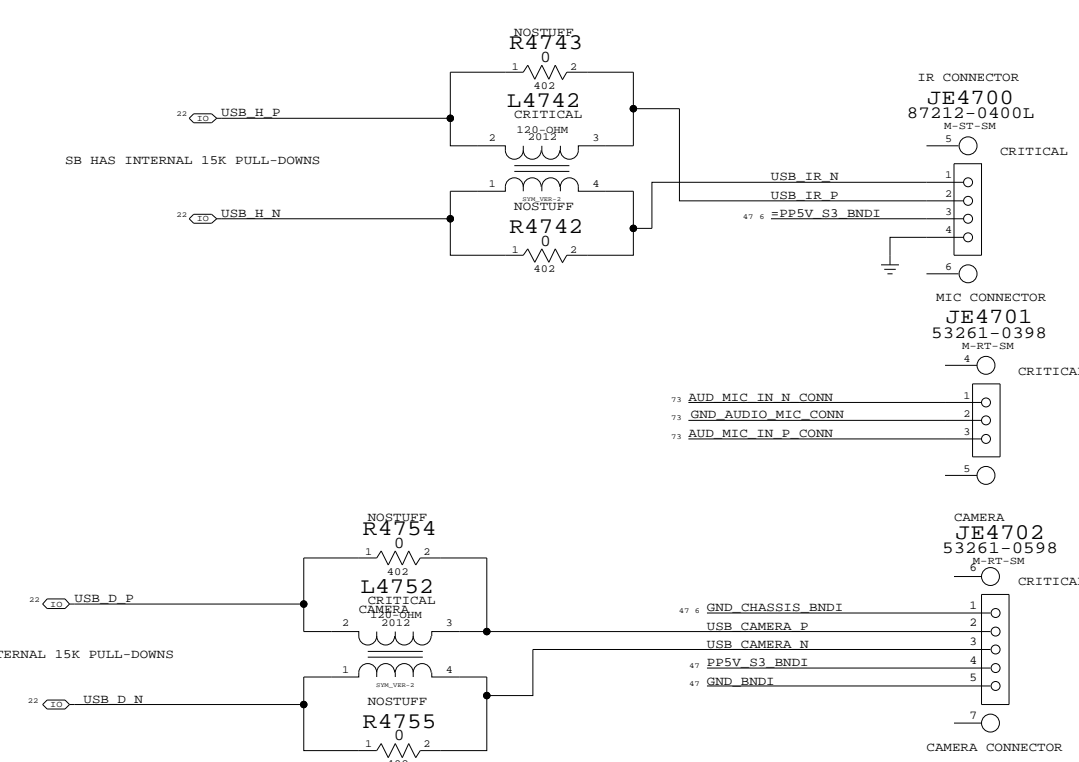
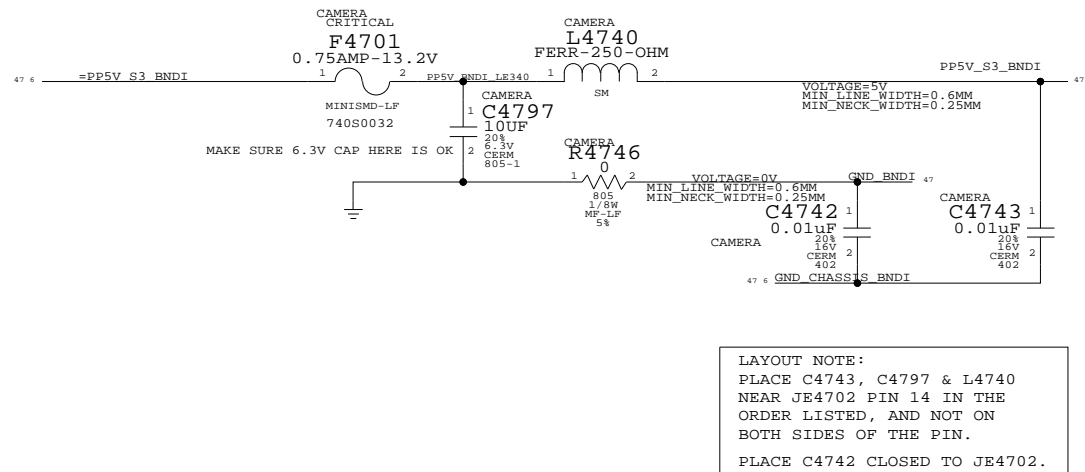
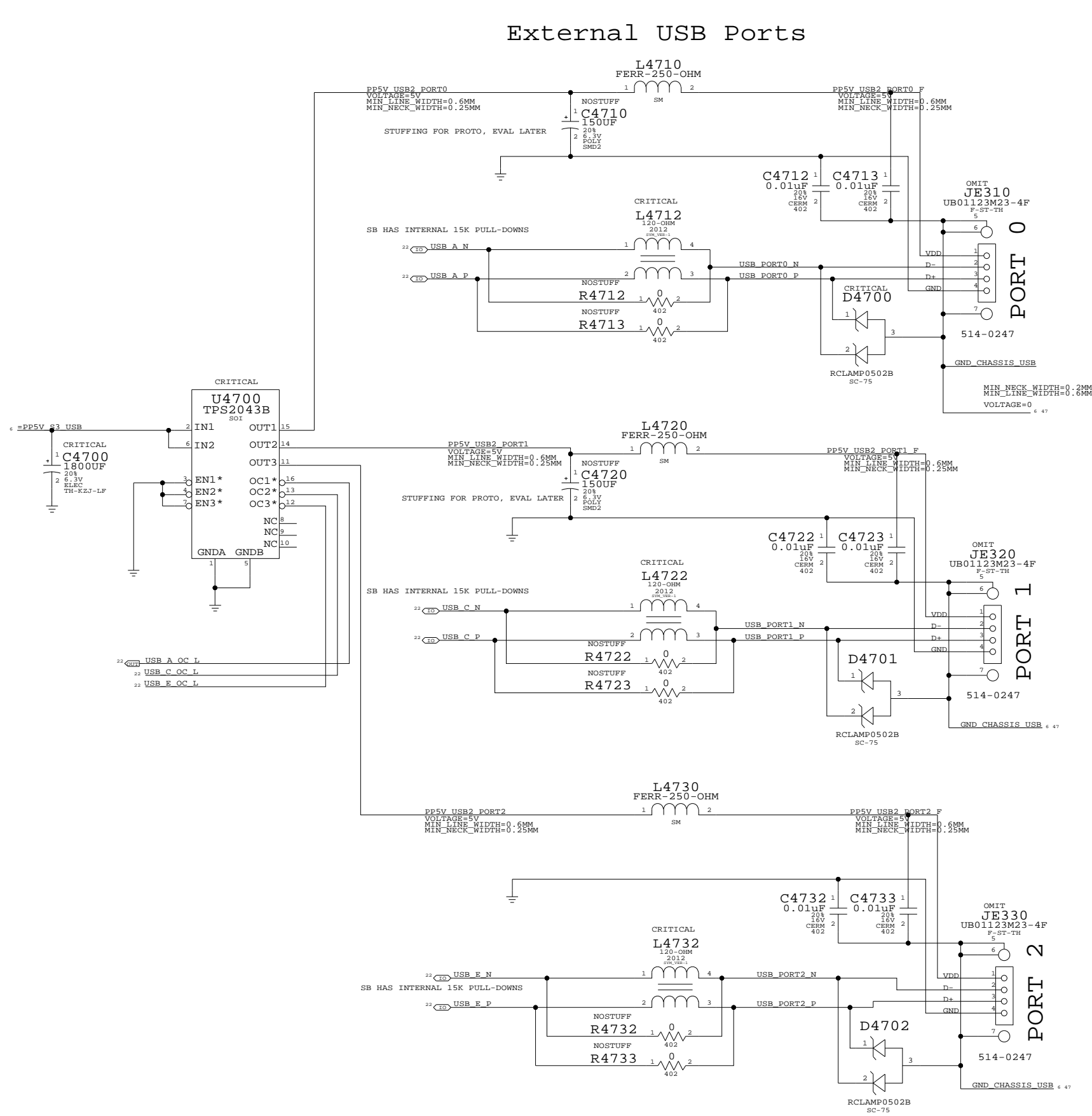
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 46	OF 97

External USB Ports



NOTE: STANDOFFS FOR J4700
 SDF4700
 STDOFF-40D4.5H-1.35-TH
 SDF4701
 STDOFF-40D4.5H-1.35-TH

USB Device Interfaces

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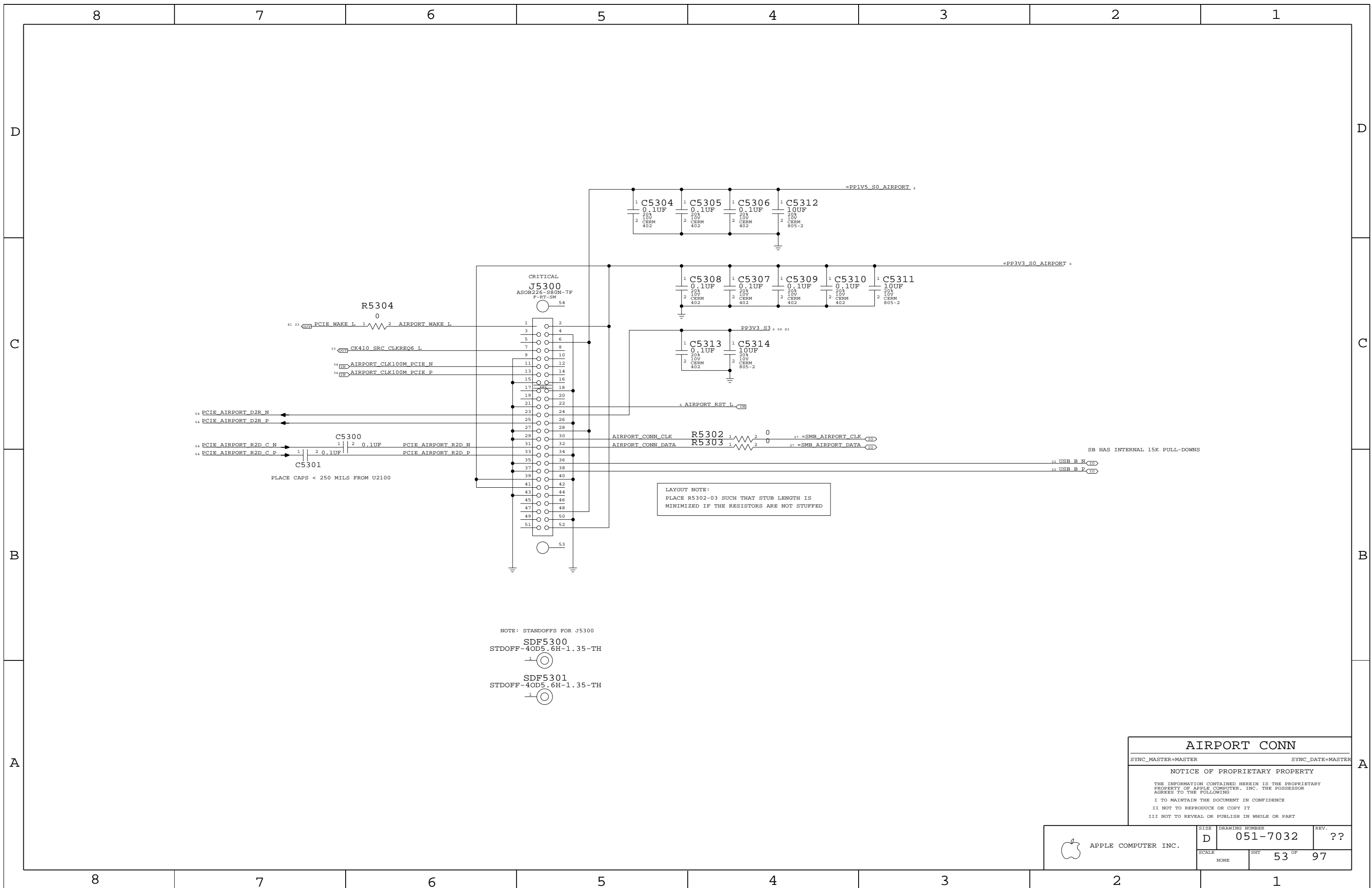
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7032	REV.	??
	SCALE	NONE	SHT	47 OF 97		



LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH
 SDF5301
 STDOFF-40D5.6H-1.35-TH

SB HAS INTERNAL 15K PULL-DOWNS

AIRPORT CONN
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	53 OF 97	
NONE			

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

22 PCIE C R2D C N == TP PCIE C R2D C N
MAKE_BASE=TRUE

22 PCIE C R2D C P == TP PCIE C R2D C P
MAKE_BASE=TRUE

22 PCIE C D2R N == TP PCIE C D2R N
MAKE_BASE=TRUE

22 PCIE C D2R P == TP PCIE C D2R P
MAKE_BASE=TRUE

22 PCIE D R2D C N == TP PCIE D R2D C N
MAKE_BASE=TRUE

22 PCIE D R2D C P == TP PCIE D R2D C P
MAKE_BASE=TRUE

22 PCIE D D2R N == TP PCIE D D2R N
MAKE_BASE=TRUE

22 PCIE D D2R P == TP PCIE D D2R P
MAKE_BASE=TRUE

22 PCIE E R2D C N == TP PCIE E R2D C N
MAKE_BASE=TRUE

22 PCIE E R2D C P == TP PCIE E R2D C P
MAKE_BASE=TRUE

22 PCIE E D2R N == TP PCIE E D2R N
MAKE_BASE=TRUE

22 PCIE E D2R P == TP PCIE E D2R P
MAKE_BASE=TRUE

22 PCIE F R2D C N == TP PCIE F R2D C N
MAKE_BASE=TRUE

22 PCIE F R2D C P == TP PCIE F R2D C P
MAKE_BASE=TRUE

22 PCIE F D2R N == TP PCIE F D2R N
MAKE_BASE=TRUE

22 PCIE F D2R P == TP PCIE F D2R P
MAKE_BASE=TRUE

USED PCIE PORTS

22 PCIE A R2D C N == PCIE AIRPORT R2D C N 53
MAKE_BASE=TRUE

22 PCIE A R2D C P == PCIE AIRPORT R2D C P 53
MAKE_BASE=TRUE

22 5 PCIE A D2R N == PCIE AIRPORT D2R N 53
MAKE_BASE=TRUE

22 5 PCIE A D2R P == PCIE AIRPORT D2R P 53
MAKE_BASE=TRUE

22 PCIE B R2D C N == PCIE ENET R2D C N 41
MAKE_BASE=TRUE

22 PCIE B R2D C P == PCIE ENET R2D C P 41
MAKE_BASE=TRUE

22 5 PCIE B D2R N == PCIE ENET D2R N 41
MAKE_BASE=TRUE

22 5 PCIE B D2R P == PCIE ENET D2R P 41
MAKE_BASE=TRUE

PCIE PORT ALIASES		
SYNC_MASTER=MASTER	SYNC_DATE=MASTER	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	54 OF 97	
NONE			

8

7

6

5

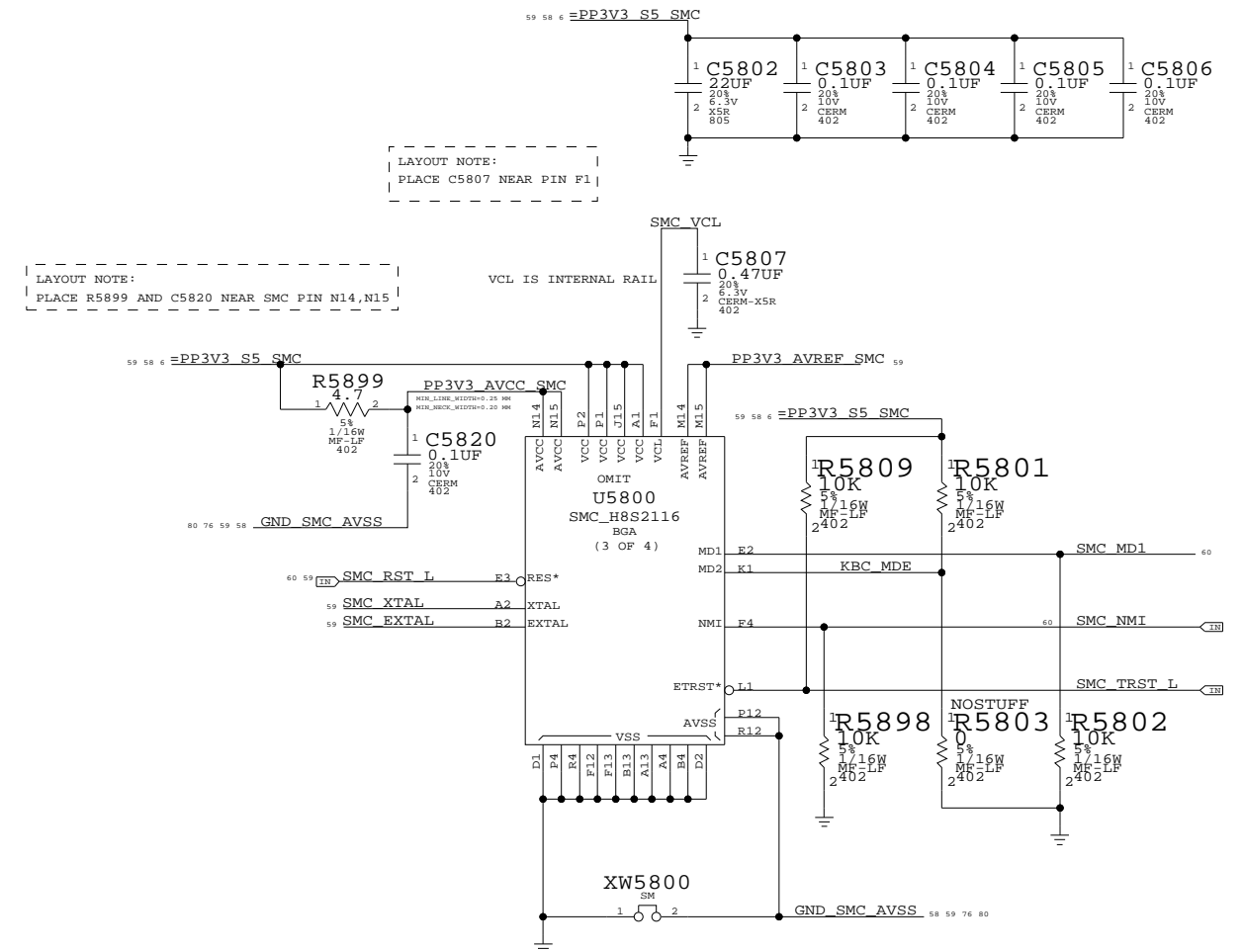
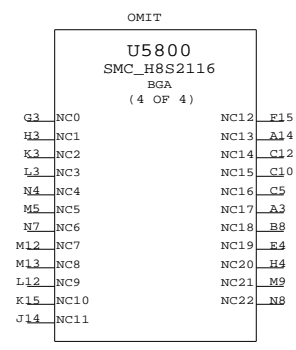
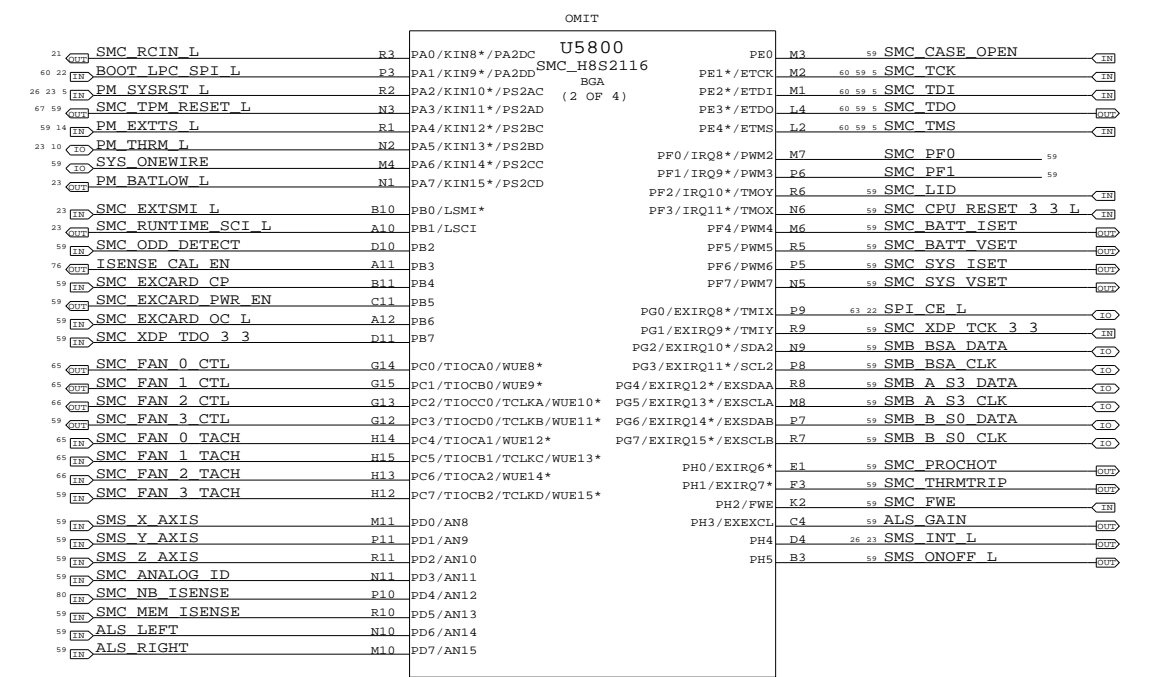
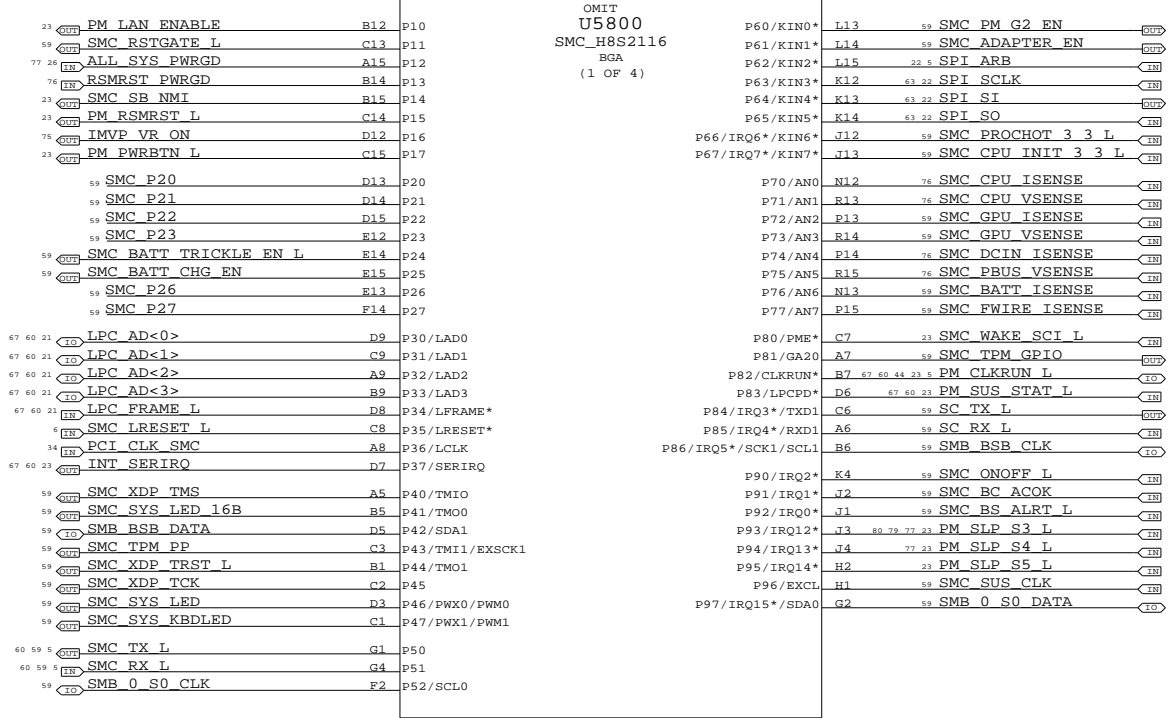
4

3

2

1

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

NOTICE OF PROPRIETARY PROPERTY

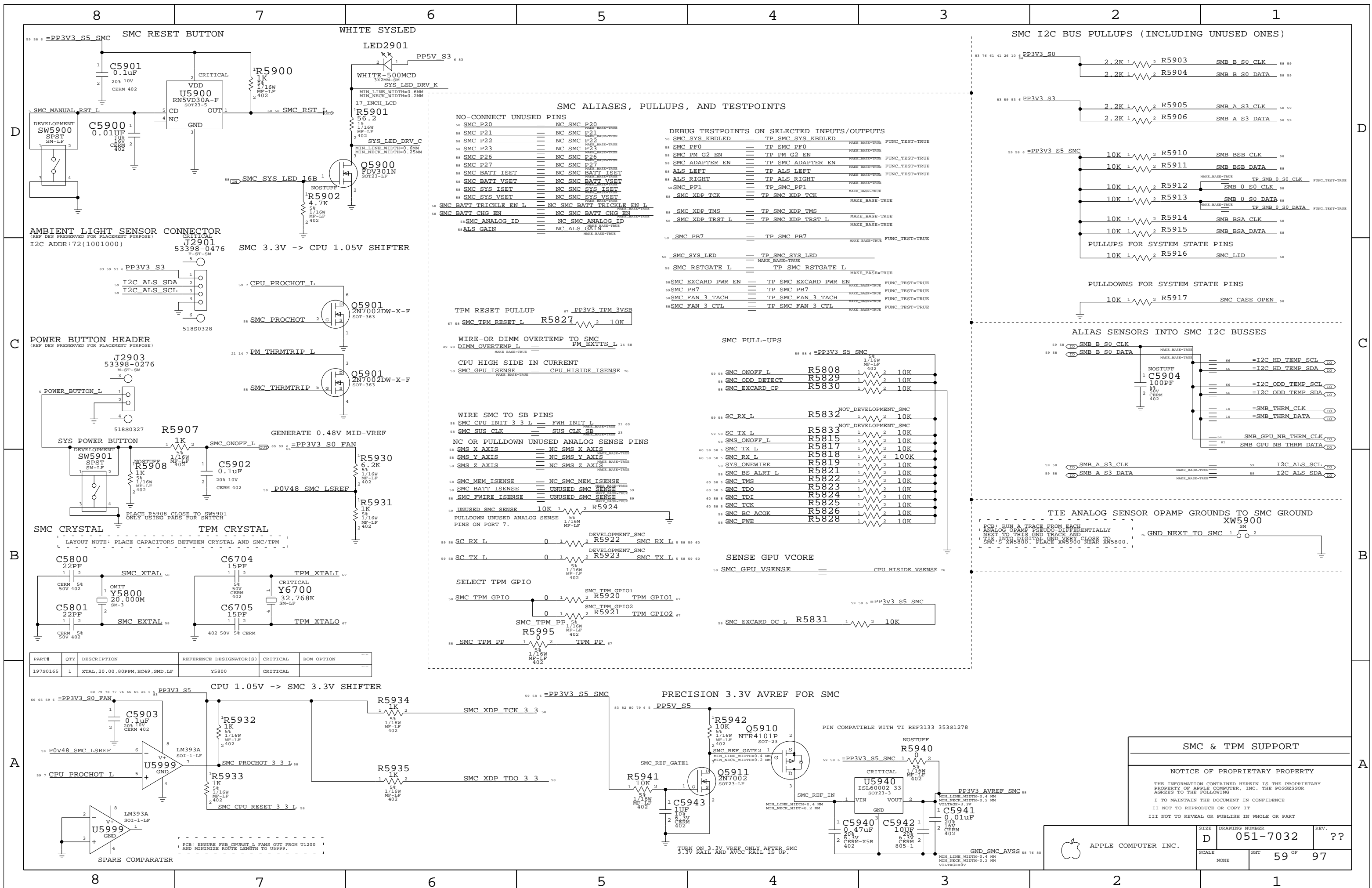
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	<p>SCALE</p> <p>NONE</p>	<p>SHT</p> <p>58 OF 97</p>	



SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
SMC P20 = NC SMC P20	SMC SYS_KBDLED = TP_SMC_SYS_KBDLED
SMC P21 = NC SMC P21	SMC PF0 = TP_SMC_PF0
SMC P22 = NC SMC P22	SMC PM_G2_EN = TP_PM_G2_EN
SMC P23 = NC SMC P23	SMC_ADAPTER_EN = TP_SMC_ADAPTER_EN
SMC P26 = NC SMC P26	ALS_LEFT = TP_ALS_LEFT
SMC P27 = NC SMC P27	ALS_RIGHT = TP_ALS_RIGHT
SMC_BATT_ISET = NC SMC_BATT_ISET	SMC_PFI = TP_SMC_PFI
SMC_BATT_VSET = NC SMC_BATT_VSET	SMC_XDP_TCK = TP_SMC_XDP_TCK
SMC_SYS_ISET = NC SMC_SYS_ISET	SMC_XDP_TMS = TP_SMC_XDP_TMS
SMC_SYS_VSET = NC SMC_SYS_VSET	SMC_XDP_TRST_L = TP_SMC_XDP_TRST_L
SMC_BATT_TRICKLE_EN_L = NC SMC_BATT_TRICKLE_EN_L	SMC_PB7 = TP_SMC_PB7
SMC_BATT_CHG_EN = NC SMC_BATT_CHG_EN	SMC_SYS_LED = TP_SMC_SYS_LED
SMC_ANALOG_ID = NC SMC_ANALOG_ID	SMC_RSTGATE_L = TP_SMC_RSTGATE_L
ALS_GAIN = NC ALS_GAIN	SMC_EXCARD_PWR_EN = TP_SMC_EXCARD_PWR_EN
	SMC_PB7 = TP_SMC_PB7
	SMC_FAN_3_TACH = TP_SMC_FAN_3_TACH
	SMC_FAN_3_CTL = TP_SMC_FAN_3_CTL

SMC PULL-UPS

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SMC_EXCARD_CP	R5830	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALRT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K

SMC CPU 1.05V -> SMC 3.3V SHIFTER

SMC_CPU_INIT_3_3_L	FWH_INIT_L
SMC_SUS_CLK	SUS_CLK_SB
SMC_CPU_ISENSE	CPU_HISIDE_ISENSE
SMC_GPU_ISENSE	CPU_HISIDE_ISENSE
SMC_TPM_GPIO	SMC_TPM_GPIO1
SMC_TPM_PP	SMC_TPM_PP

PRECISION 3.3V AVREF FOR SMC

SMC_XDP_TCK_3_3	R5934
SMC_XDP_TDO_3_3	R5935
SMC_REF_GATE1	R5941
SMC_REF_GATE2	R5942
SMC_REF_IN	R5943

SMC CRystals and TPM Crystals

Part#	Qty	Description	Reference Designator(s)	Critical	BOM Option
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

SMC I2C BUS PULLUPS (INCLUDING UNUSED ONES)

SMB_B_S0_CLK	R5903	2.2K
SMB_B_S0_DATA	R5904	2.2K
SMB_A_S3_CLK	R5905	2.2K
SMB_A_S3_DATA	R5906	2.2K
SMB_BSB_CLK	R5910	10K
SMB_BSB_DATA	R5911	10K
SMB_0_S0_CLK	R5912	10K
SMB_0_S0_DATA	R5913	10K
SMB_BSA_CLK	R5914	10K
SMB_BSA_DATA	R5915	10K
SMC_CASE_OPEN	R5917	10K

ALIAS SENSORS INTO SMC I2C BUSES

I2C_HD_TEMP_SCL	
I2C_HD_TEMP_SDA	
I2C_ODD_TEMP_SCL	
I2C_ODD_TEMP_SDA	
SMB_THRM_CLK	
SMB_THRM_DATA	
SMB_GPU_NB_THRM_CLK	
SMB_GPU_NB_THRM_DATA	
I2C_ALS_SCL	
I2C_ALS_SDA	

TIE ANALOG SENSOR OPAMP GROUNDS TO SMC GROUND

PCB: RUN A TRACE FROM EACH ANALOG OPAMP PSEUDO-DIFFERENTIALLY NEXT TO THIS GND TRACE AND TIE INTO DIGITAL GND VERY CLOSE TO SMC'S XW5800. PLACE XW5900 NEAR XW5800.

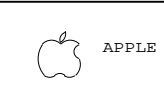
SMC & TPM SUPPORT

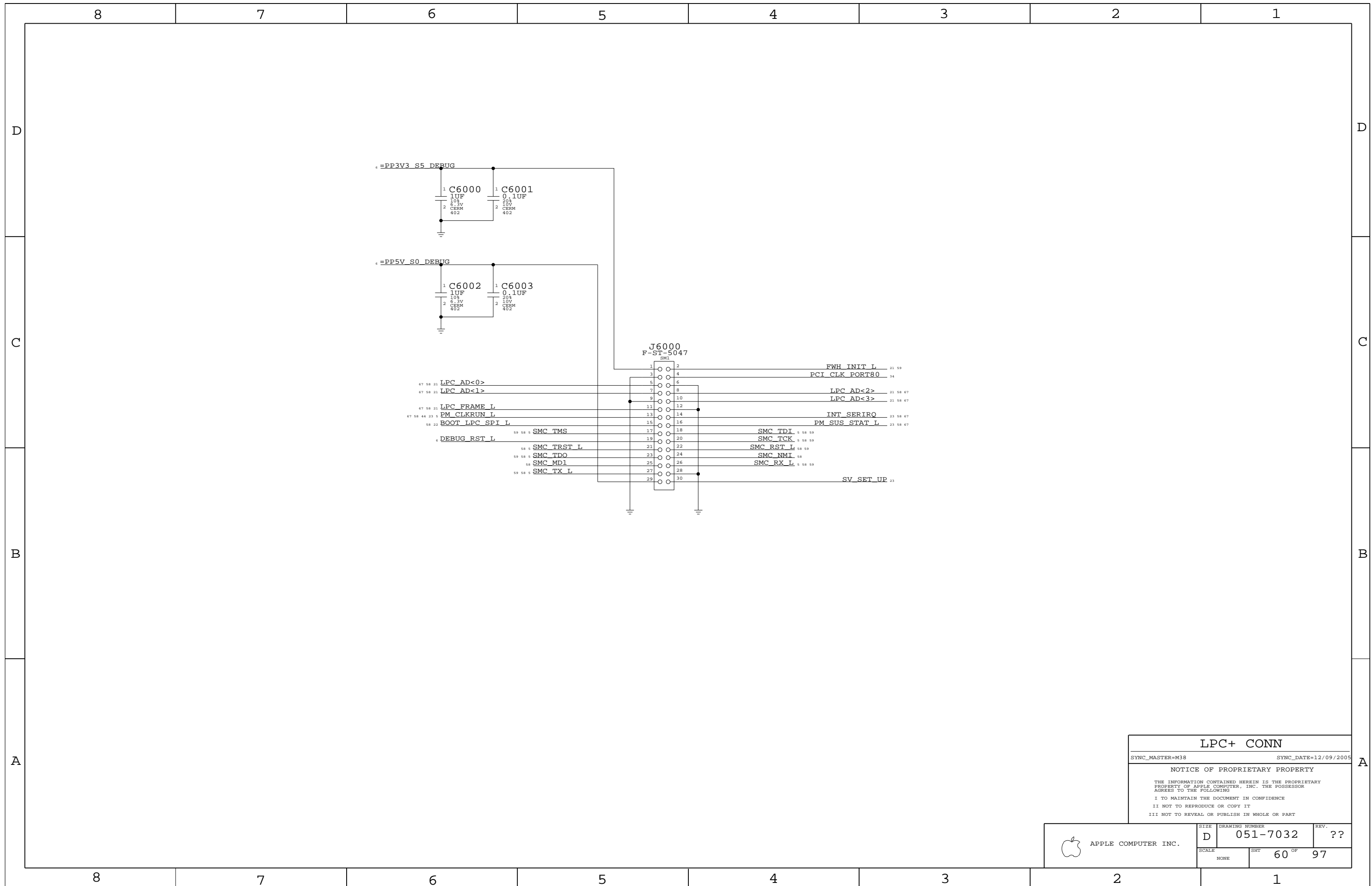
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SIZE	DRAWING NUMBER	REV.
D	051-7032	??
SCALE	SHT	59 OF 97
NONE		





LPC+ CONN

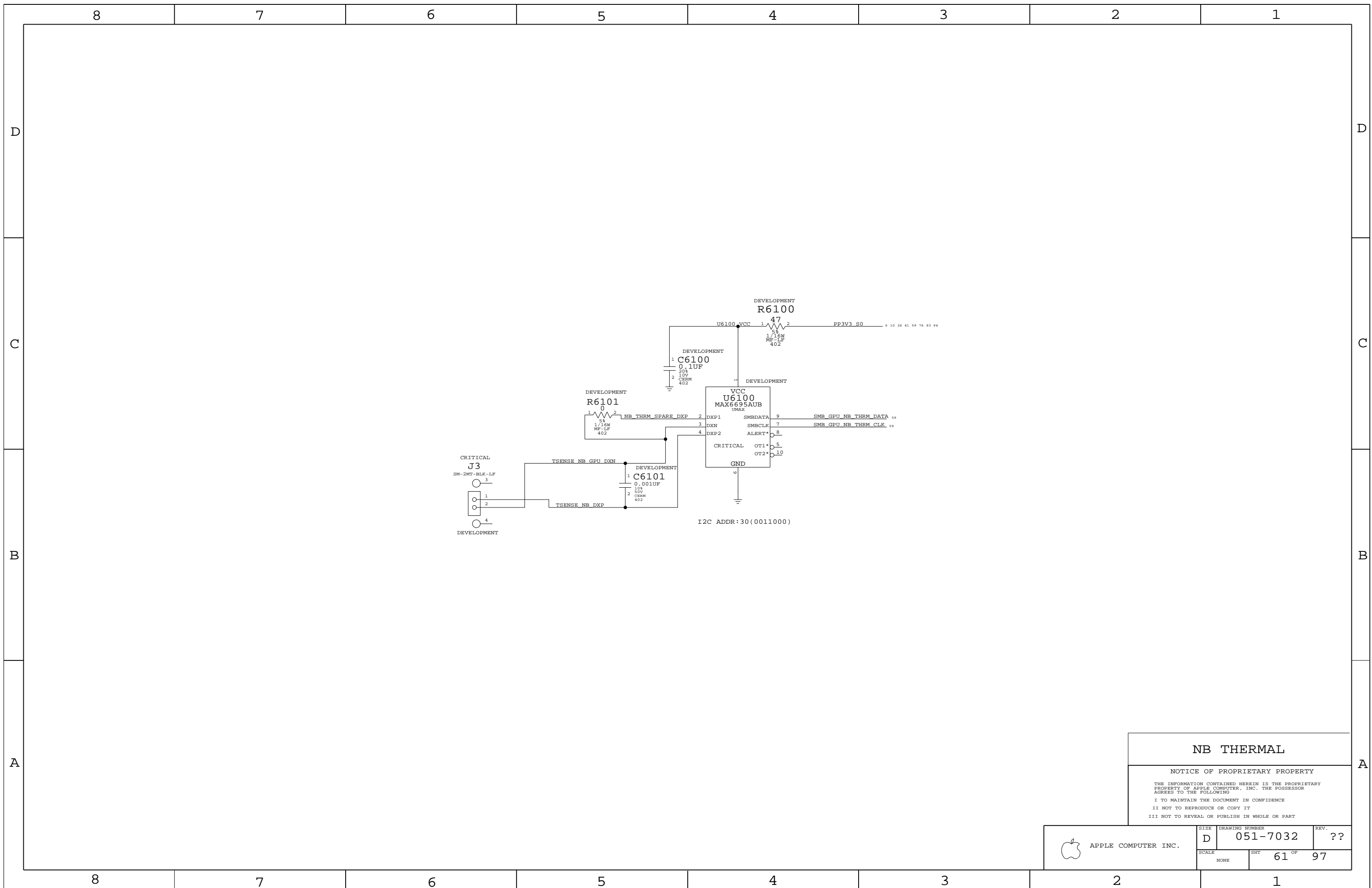
SYNC_MASTER=M38 SYNC_DATE=12/09/2005

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	D	051-7032	??
SCALE	SHT	60 OF 97	
NONE			

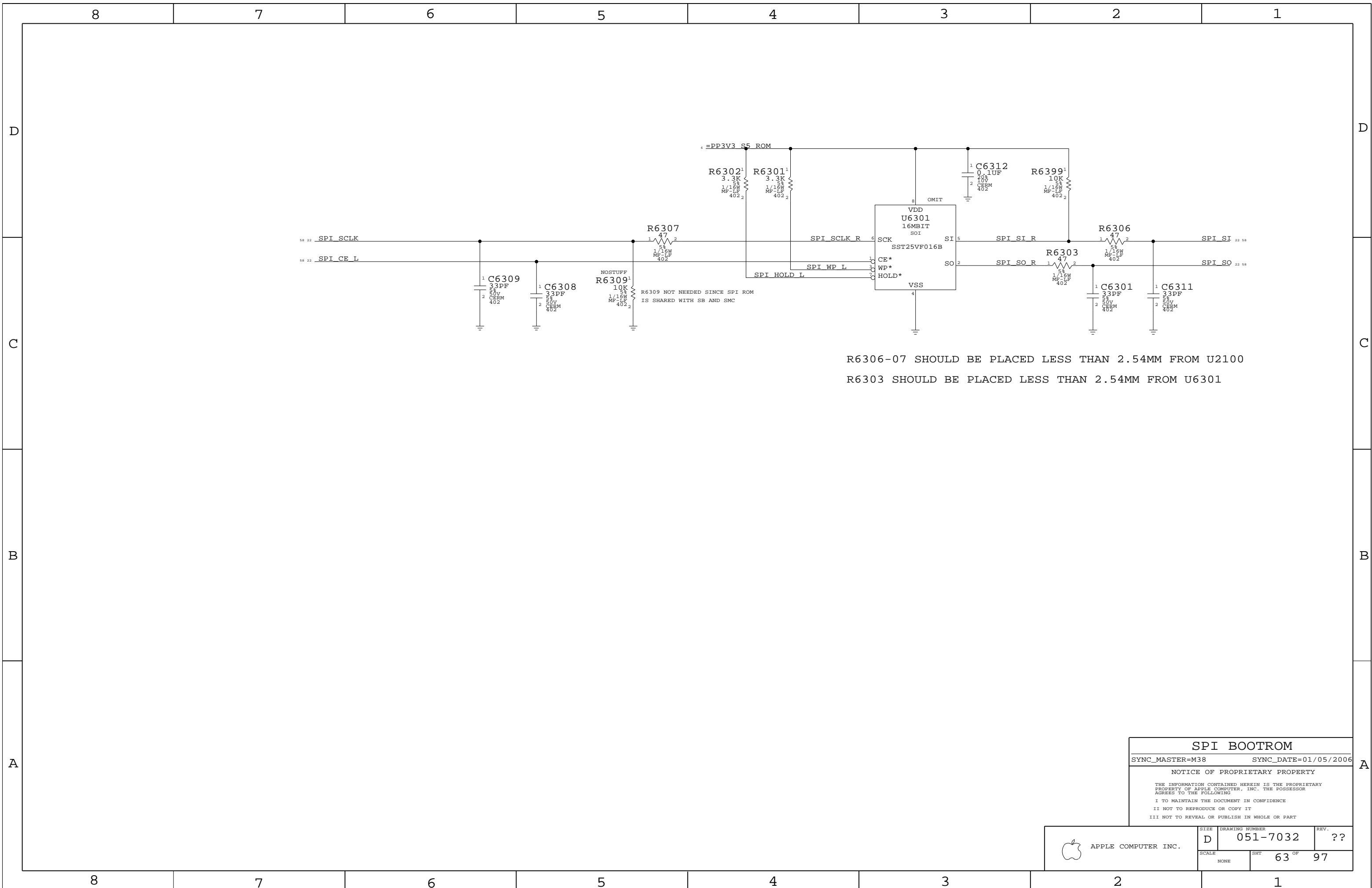


NB THERMAL

NOTICE OF PROPRIETARY PROPERTY

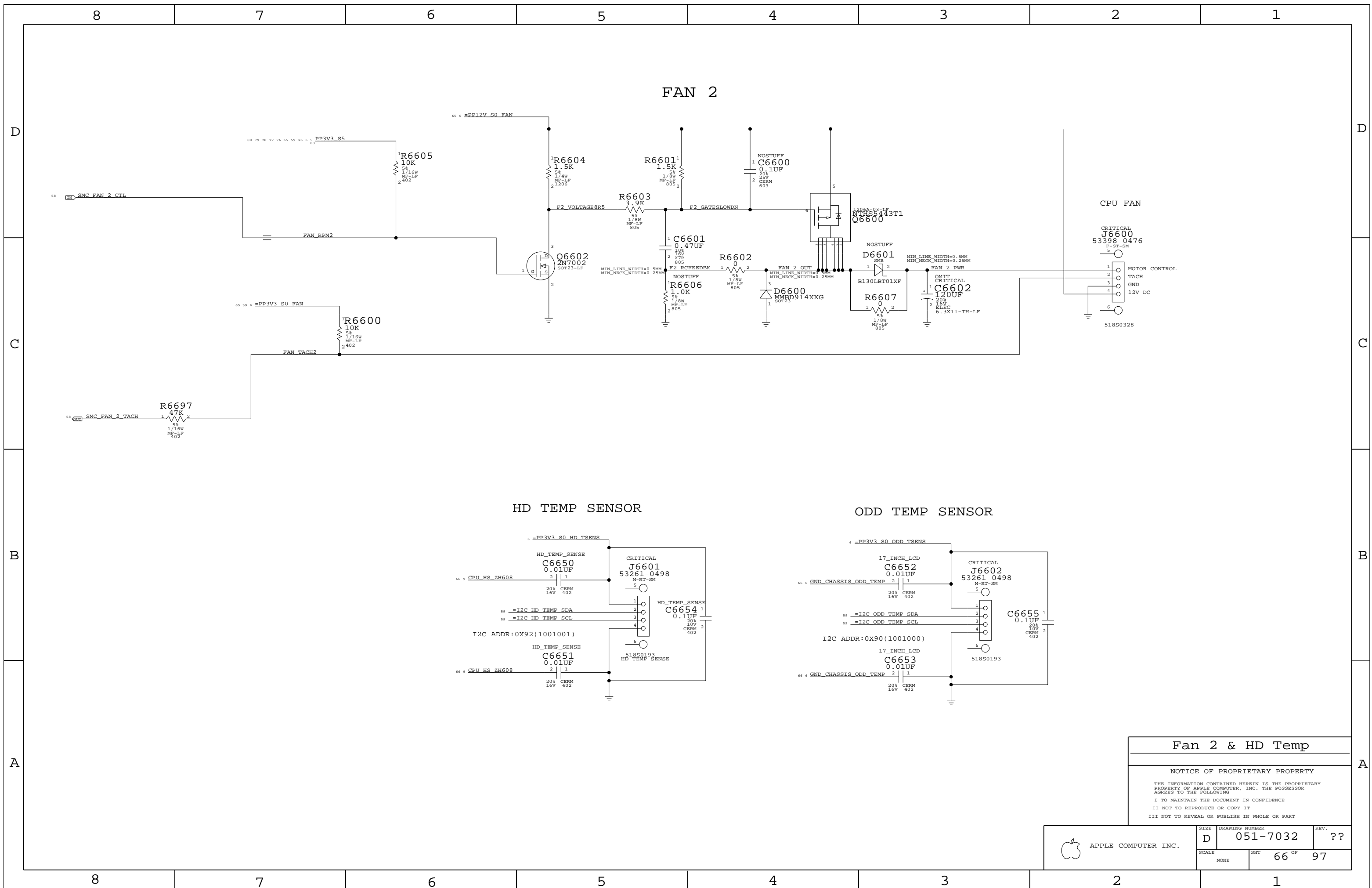
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 61	OF 97



SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 63 OF 97	REV.



FAN 2

HD TEMP SENSOR

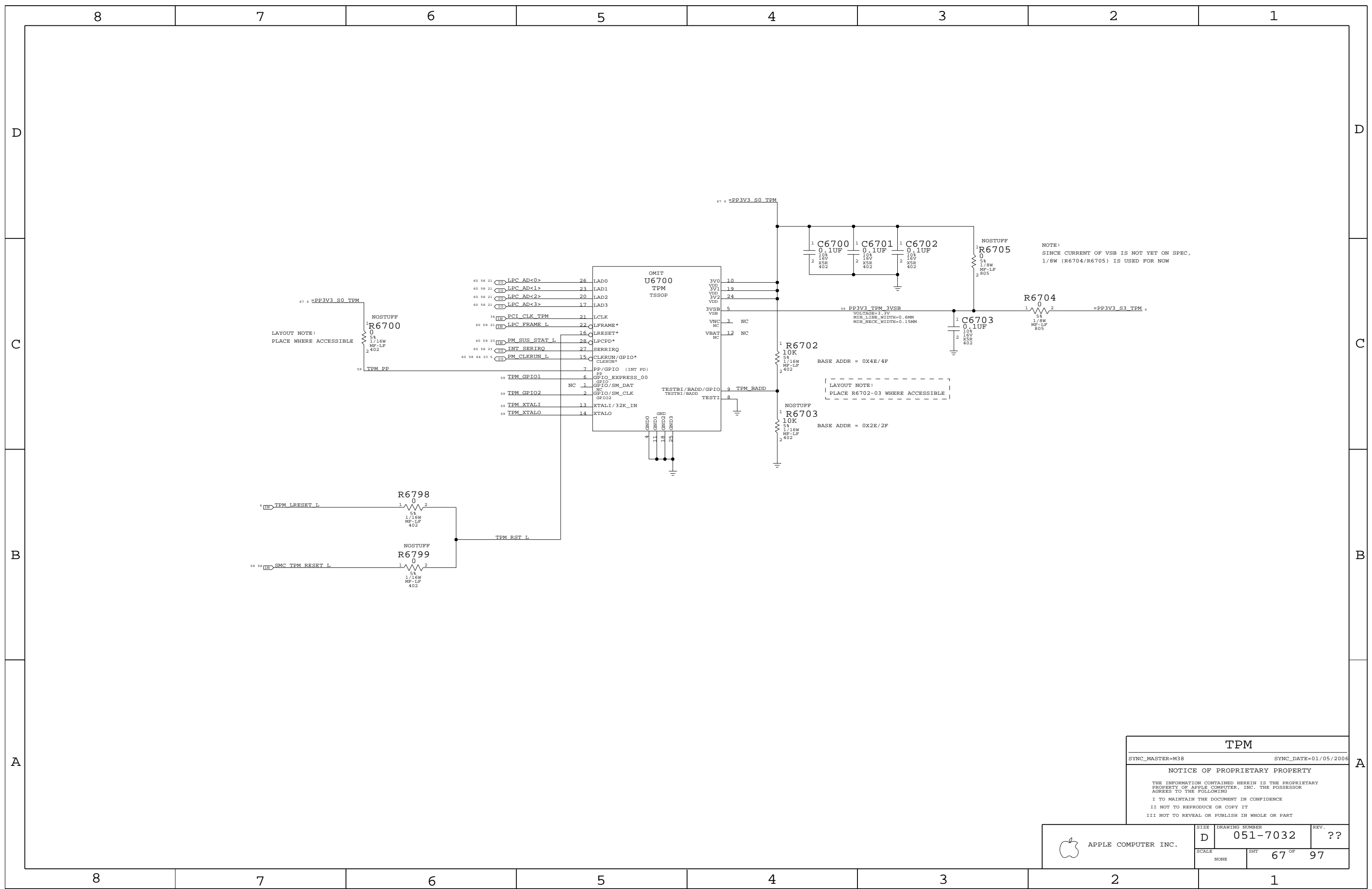
ODD TEMP SENSOR

Fan 2 & HD Temp

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	66 OF	97
NONE			



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHT 67 OF 97	

8 7 6 5 4 3 2 1

D

C

B

A

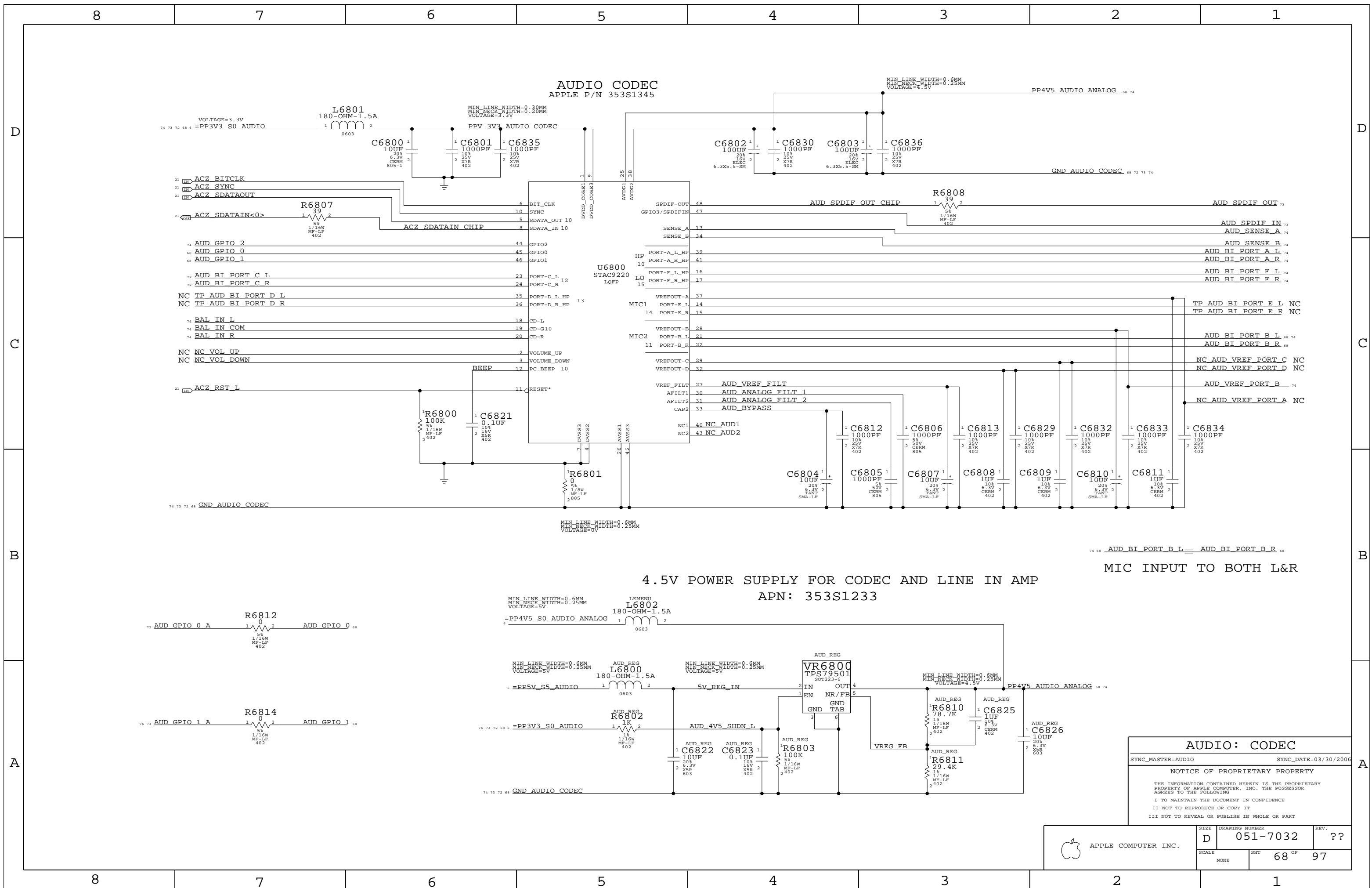
D

C

B

A

8 7 6 5 4 3 2 1



AUDIO CODEC
APPLE P/N 353S1345

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP
APN: 353S1233

AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

NOTICE OF PROPRIETARY PROPERTY

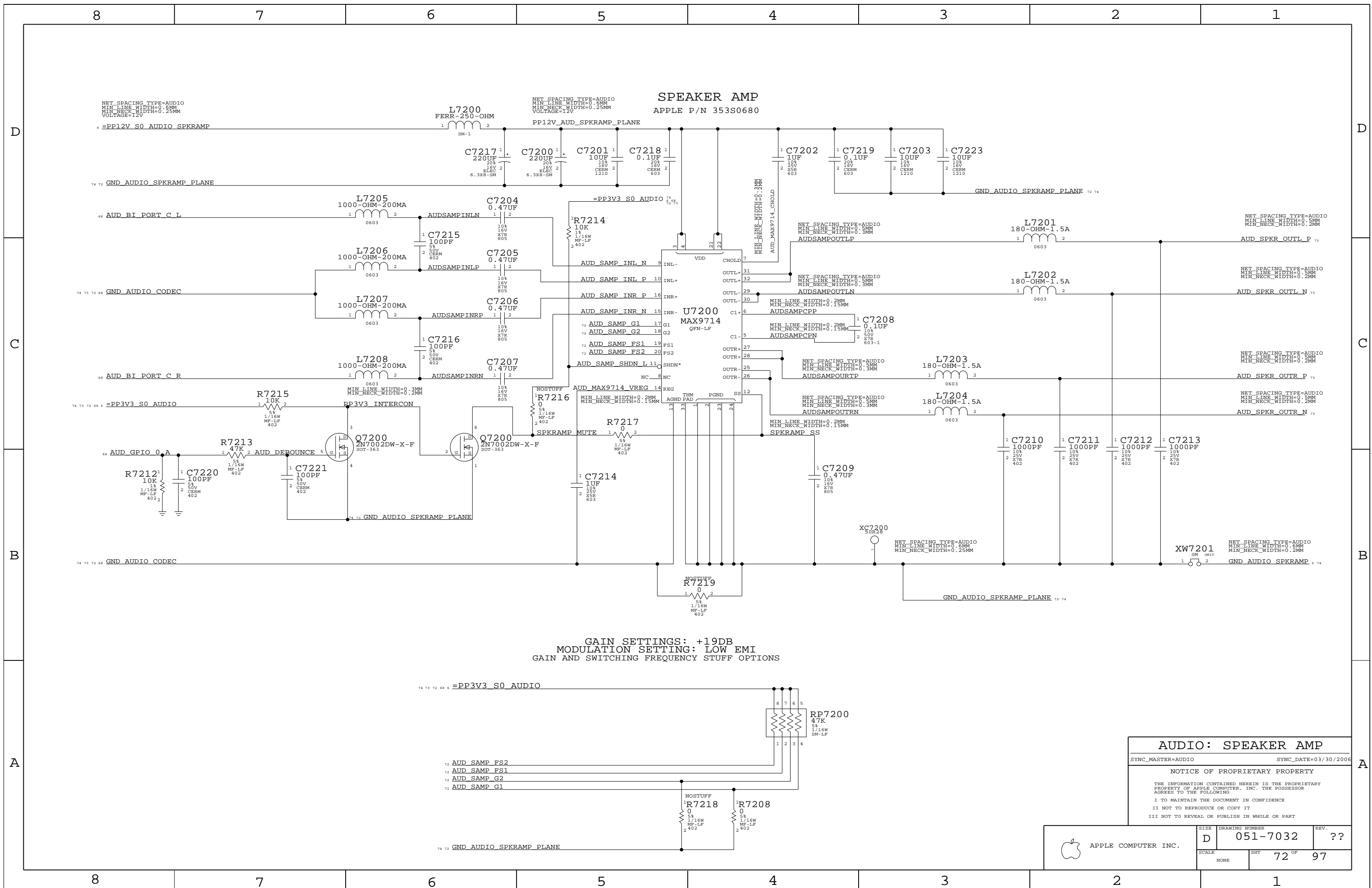
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 68 OF 97	



SPEAKER AMP
APPLE P/N 353S0680

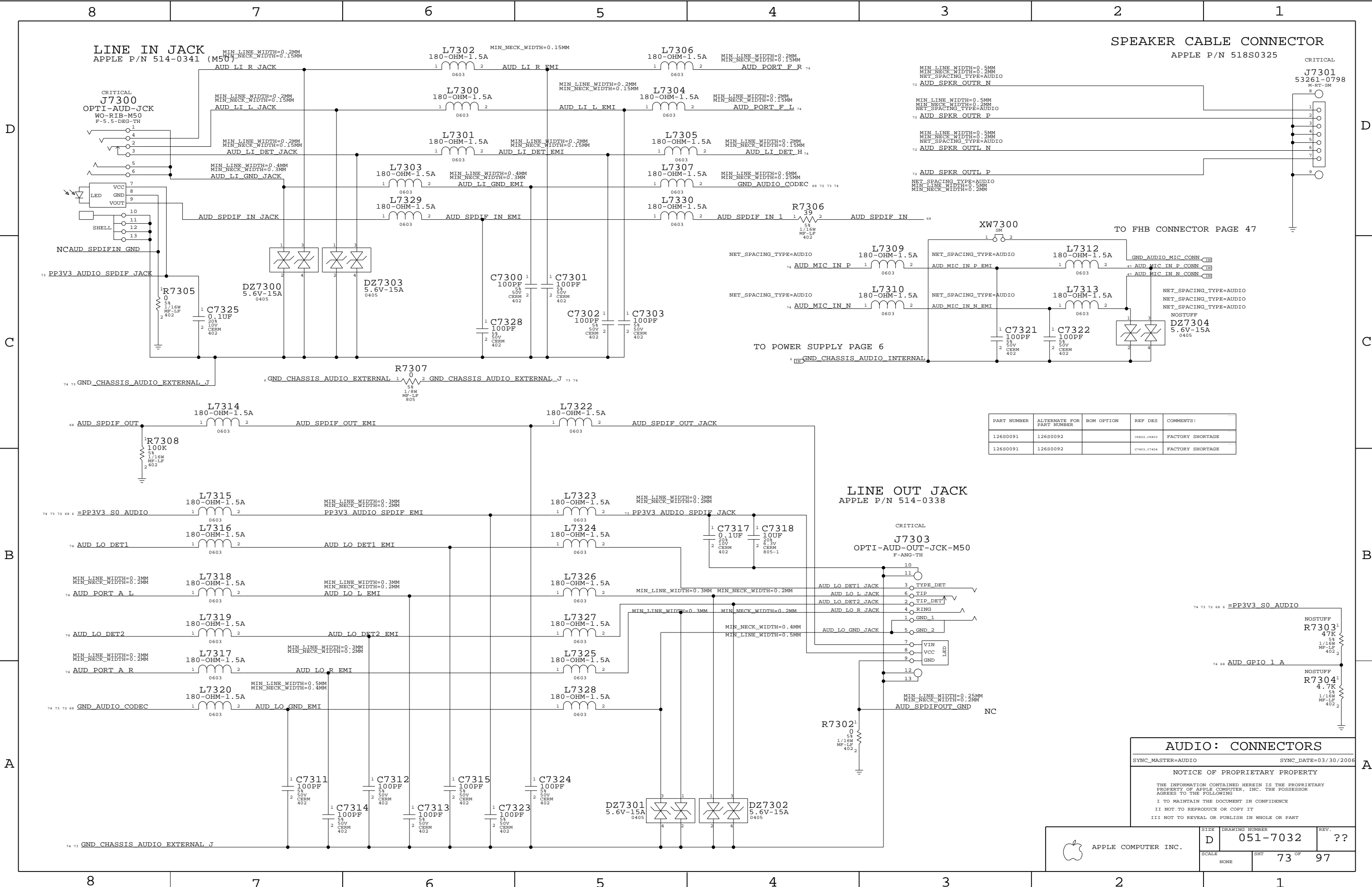
GAIN SETTINGS: +19DB
MODULATION SETTING: LOW EMI
GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

AUDIO: SPEAKER AMP
SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	72 OF	97
NONE			

LINE IN JACK
APPLE P/N 514-0341 (M50)

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		C8802, C8803	FACTORY SHORTAGE
126S0091	126S0092		C7453, C7454	FACTORY SHORTAGE

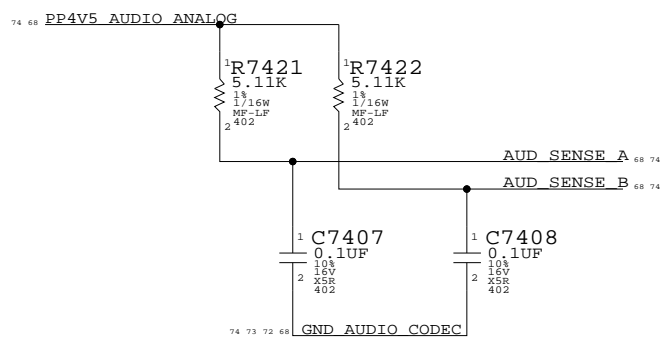
LINE OUT JACK
APPLE P/N 514-0338

AUDIO: CONNECTORS
SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	73 OF	97
NONE			

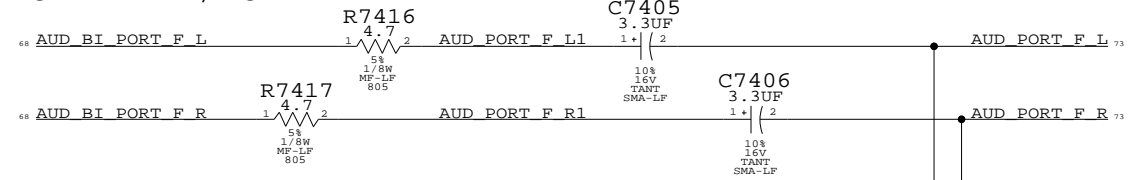
JACK SENSE PULL UPS (PLACE NEXT TO CODEC)



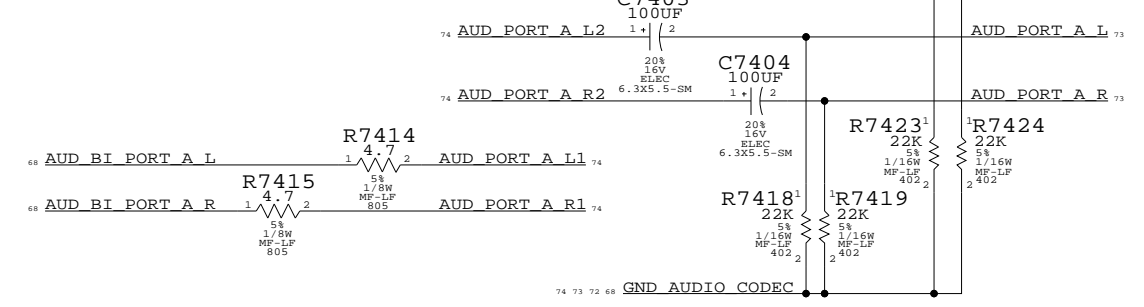
USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

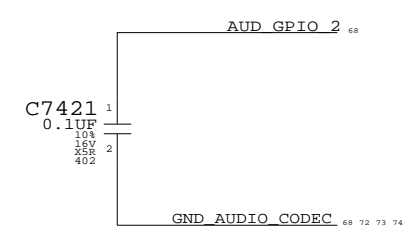
PORT F LI/LO



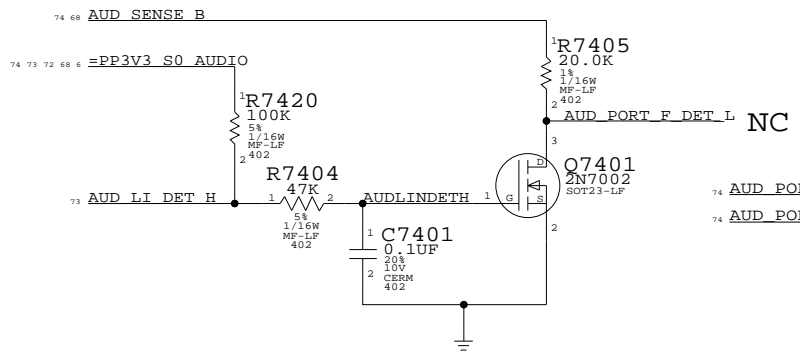
PORT A HP/LI



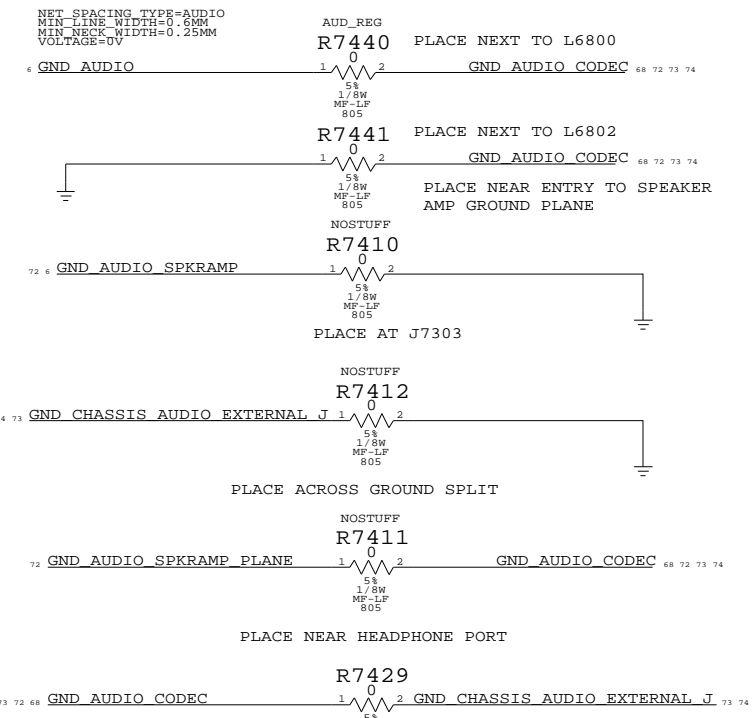
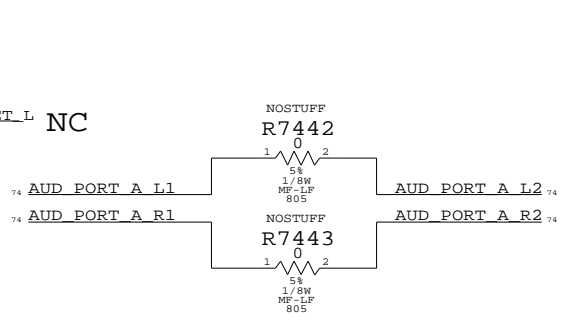
UNUSED PORT TERMINATION



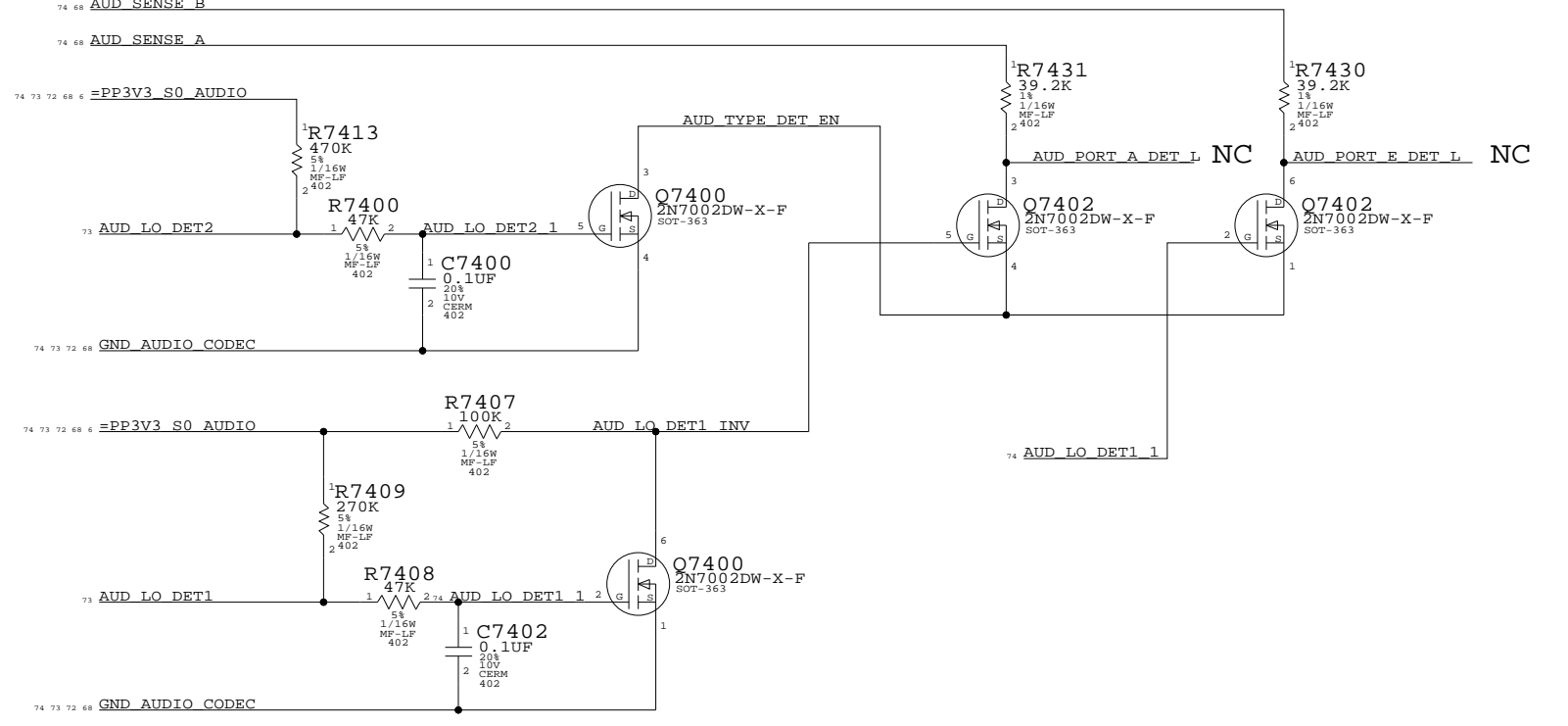
PORT F (LI) PLUG DETECT



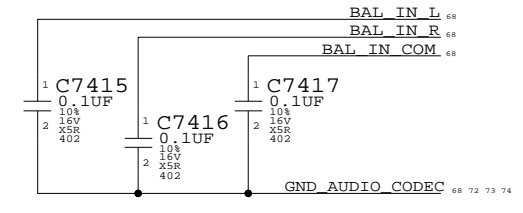
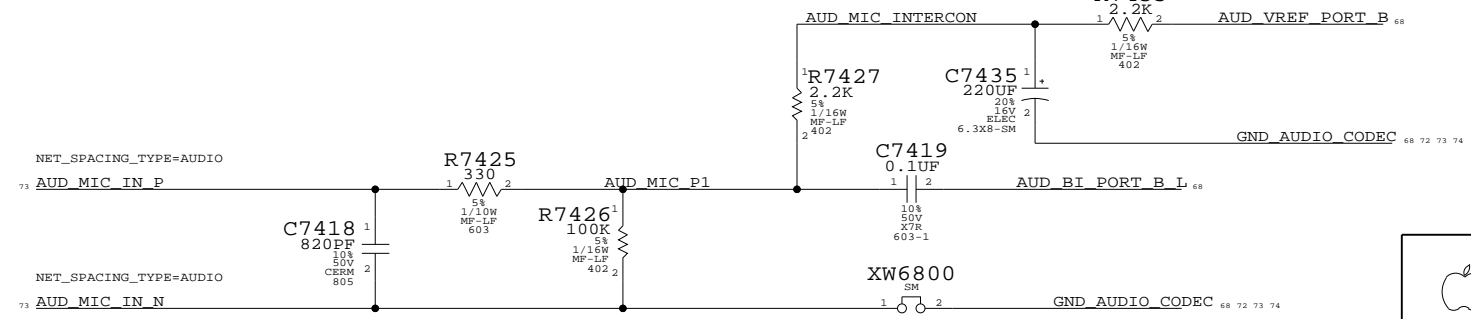
AUDIO GROUND RETURNS



PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)



MICROPHONE IMPEDANCE MATCHING CIRCUIT



AUDIO: POWER SUPPLIES

SYNC_MASTER=AUDIO SYNC_DATE=03/30/2006

NOTICE OF PROPRIETARY PROPERTY

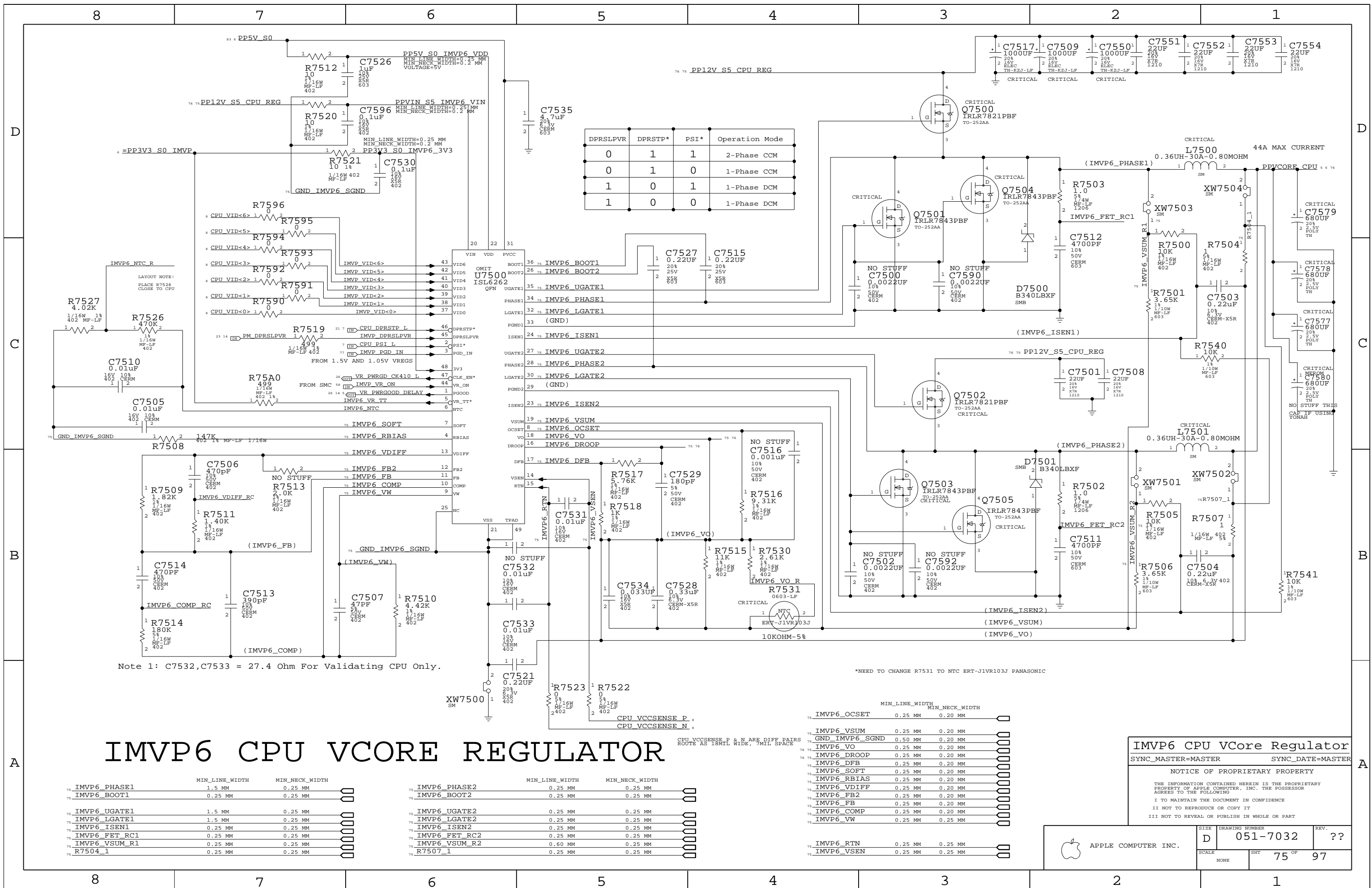
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	74 OF	97
NONE			



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

*NEED TO CHANGE R7531 TO NTC ERT-J1VR103J PANASONIC

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE1	1.5 MM	0.25 MM
75 IMVP6_BOOT1	0.25 MM	0.25 MM
75 IMVP6_UGATE1	1.5 MM	0.25 MM
75 IMVP6_LGATE1	1.5 MM	0.25 MM
75 IMVP6_ISEN1	0.25 MM	0.25 MM
75 IMVP6_FET_RC1	0.25 MM	0.25 MM
75 IMVP6_VSUM_R1	0.25 MM	0.25 MM
75 R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_PHASE2	0.25 MM	0.25 MM
75 IMVP6_BOOT2	0.25 MM	0.25 MM
75 IMVP6_UGATE2	0.25 MM	0.25 MM
75 IMVP6_LGATE2	0.25 MM	0.25 MM
75 IMVP6_ISEN2	0.25 MM	0.25 MM
75 IMVP6_FET_RC2	0.25 MM	0.25 MM
75 IMVP6_VSUM_R2	0.60 MM	0.25 MM
75 R7507_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75 IMVP6_OCSET	0.25 MM	0.20 MM
75 IMVP6_VSUM	0.25 MM	0.20 MM
75 GND_IMVP6_SGND	0.50 MM	0.20 MM
75 IMVP6_VO	0.25 MM	0.20 MM
75 IMVP6_DROOP	0.25 MM	0.20 MM
75 IMVP6_DFB	0.25 MM	0.20 MM
75 IMVP6_SOFT	0.25 MM	0.20 MM
75 IMVP6_VDIFF	0.25 MM	0.20 MM
75 IMVP6_FB2	0.25 MM	0.20 MM
75 IMVP6_FB	0.25 MM	0.20 MM
75 IMVP6_COMP	0.25 MM	0.20 MM
75 IMVP6_VW	0.25 MM	0.25 MM
75 IMVP6_RTIN	0.25 MM	0.25 MM
75 IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

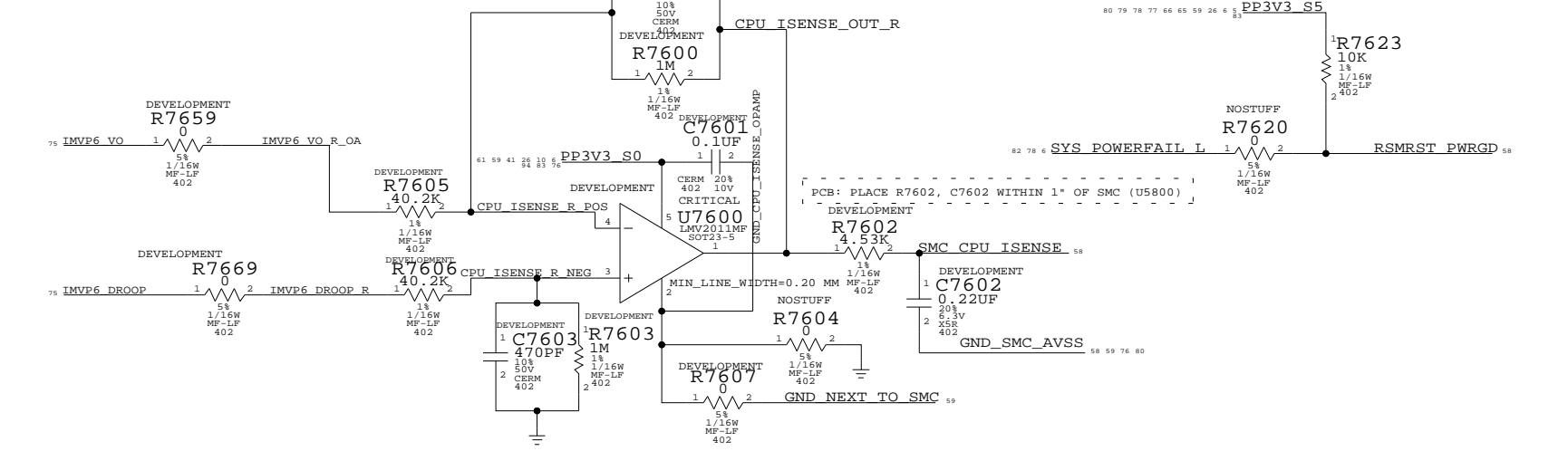
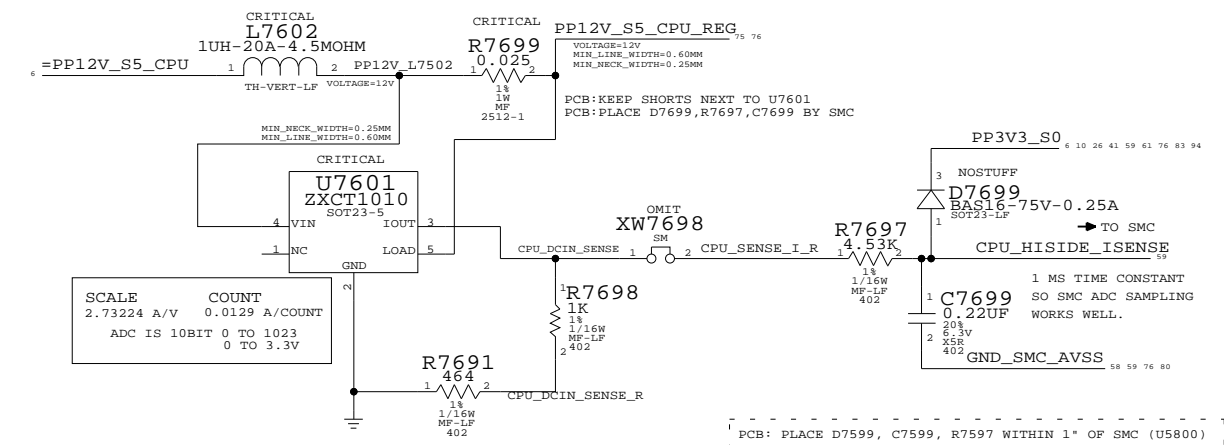
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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7032	??
	SHEET	75 OF 97	

PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

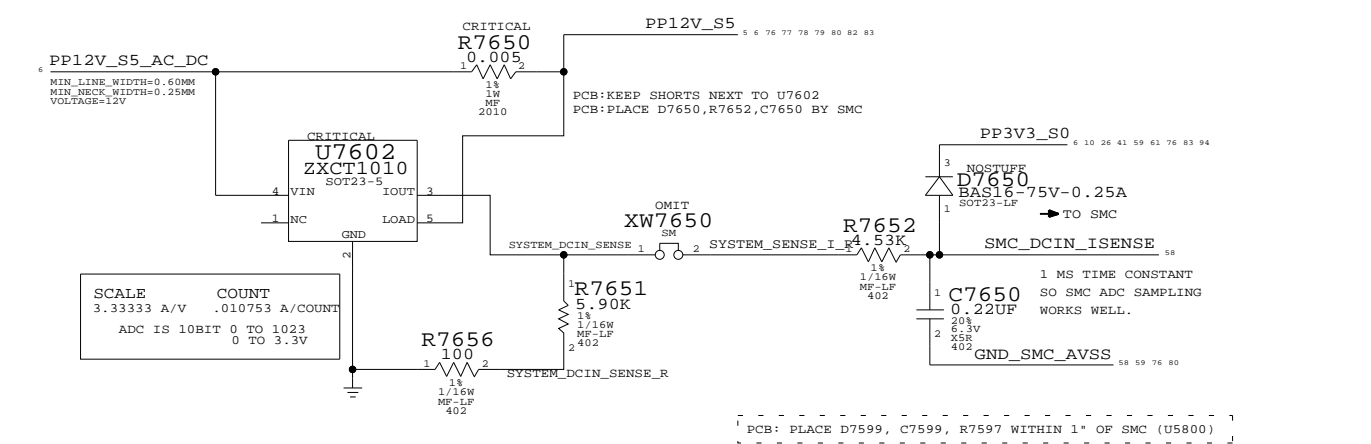
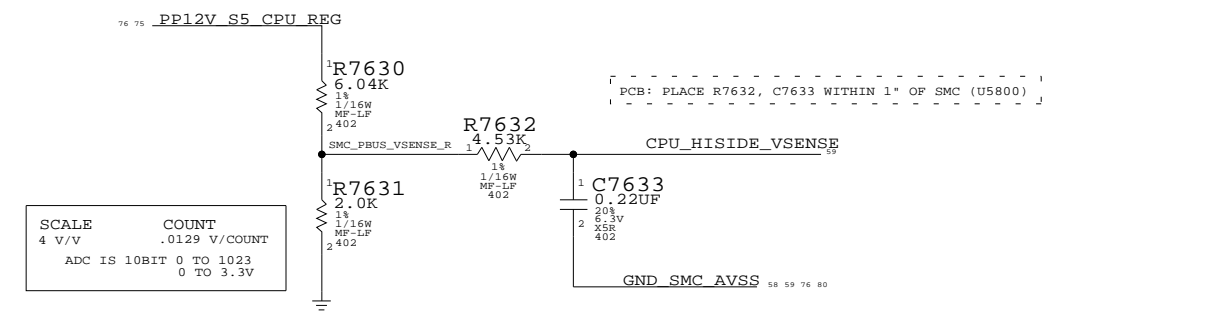
PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

SMC PWRGD PULLUP



PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

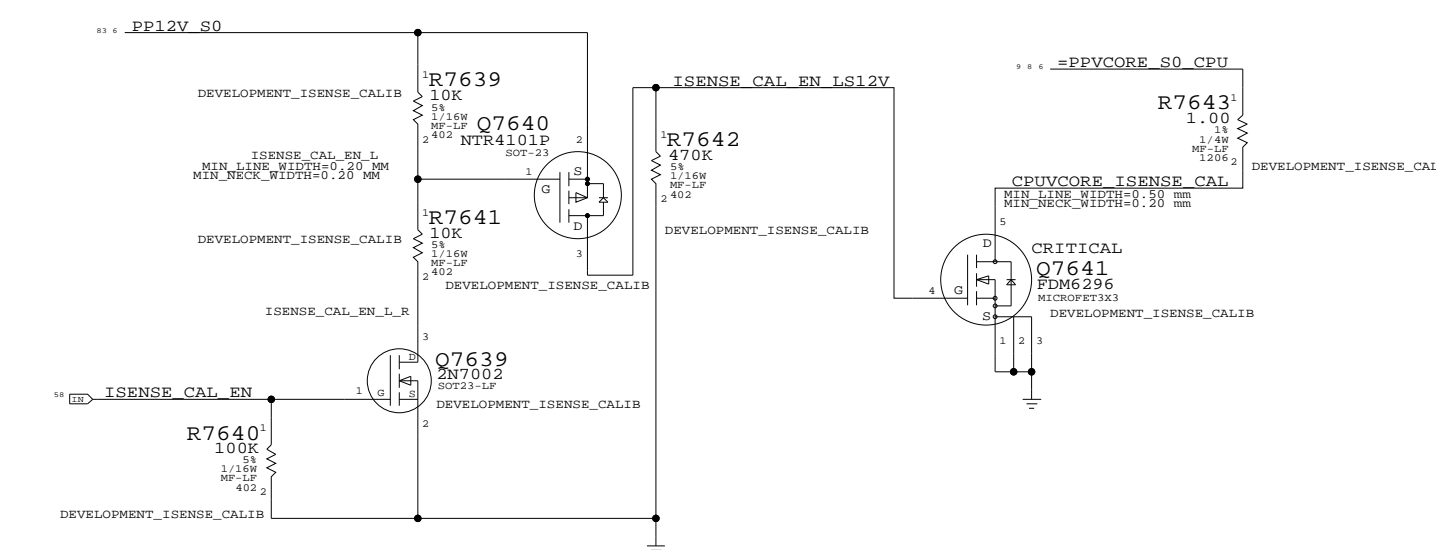
SYSTEM CURRENT SENSE



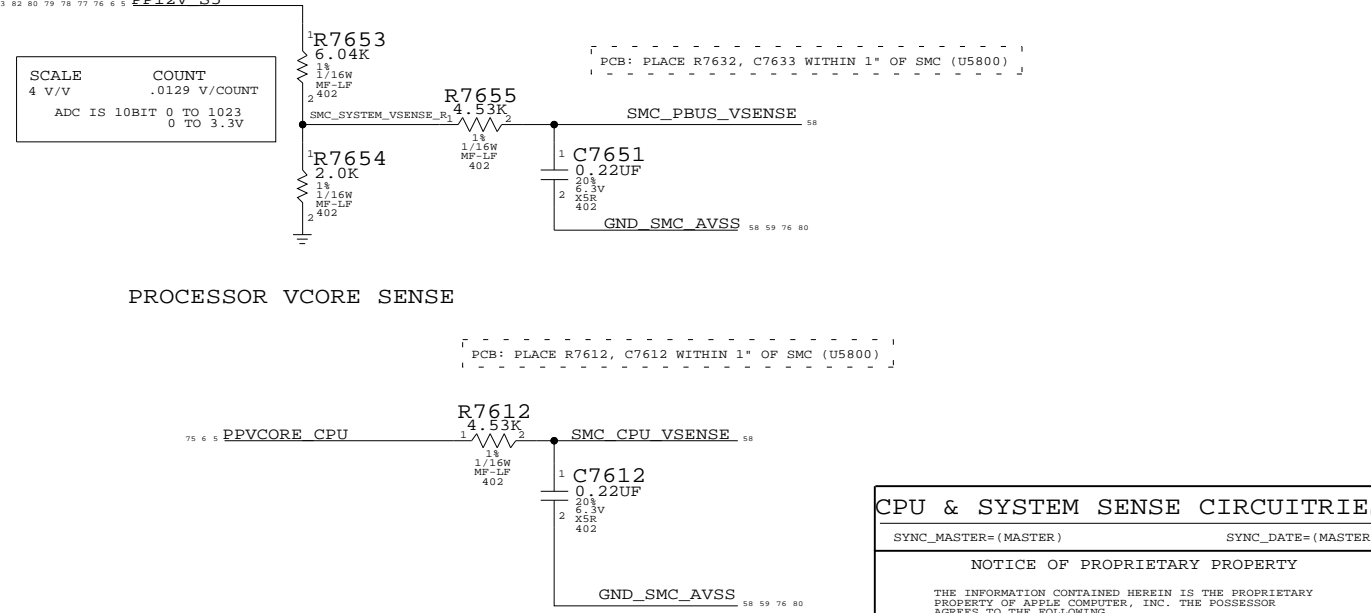
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



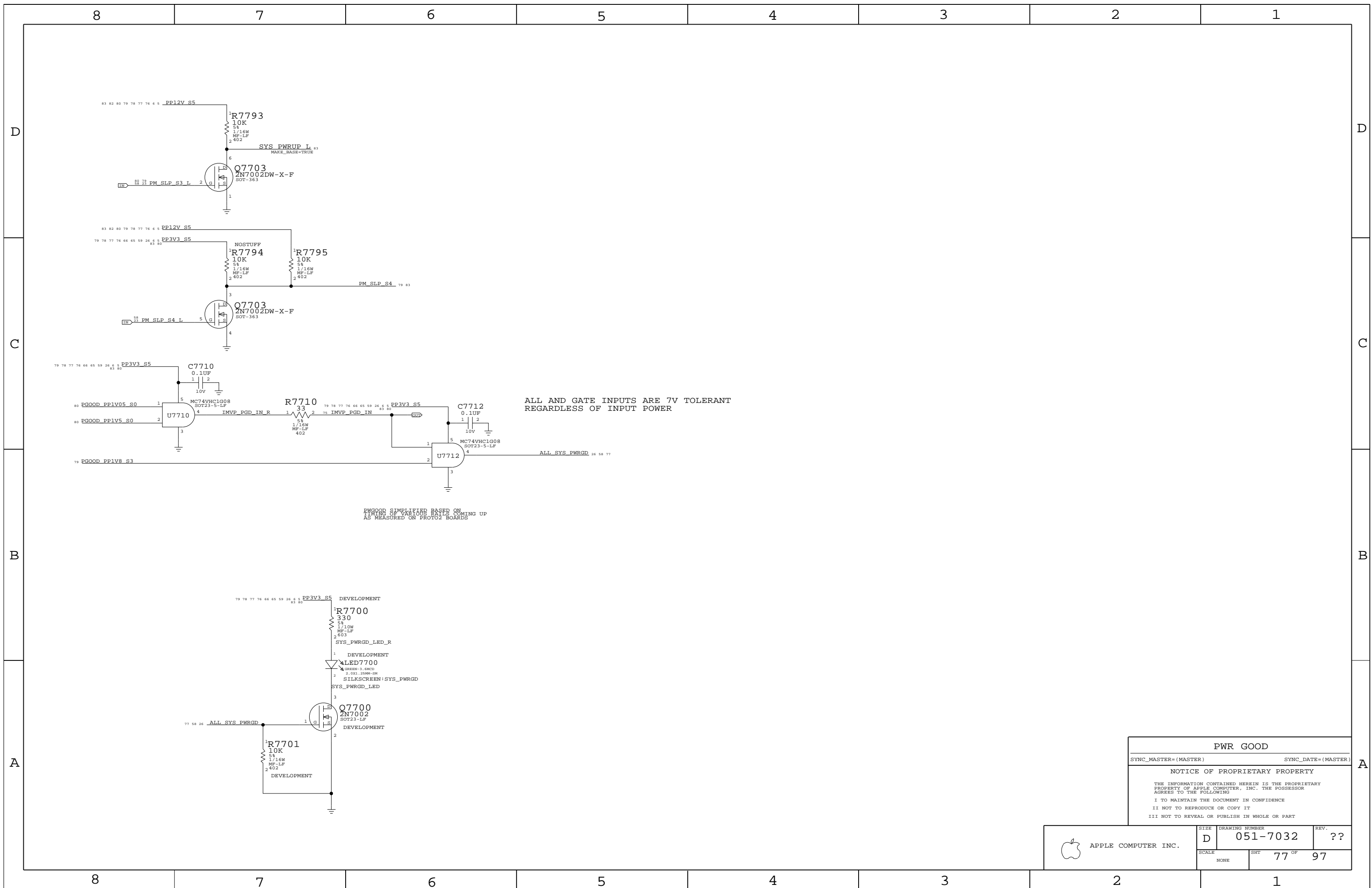
PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	76 OF	97
NONE			



ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWR GOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS


PWR GOOD

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

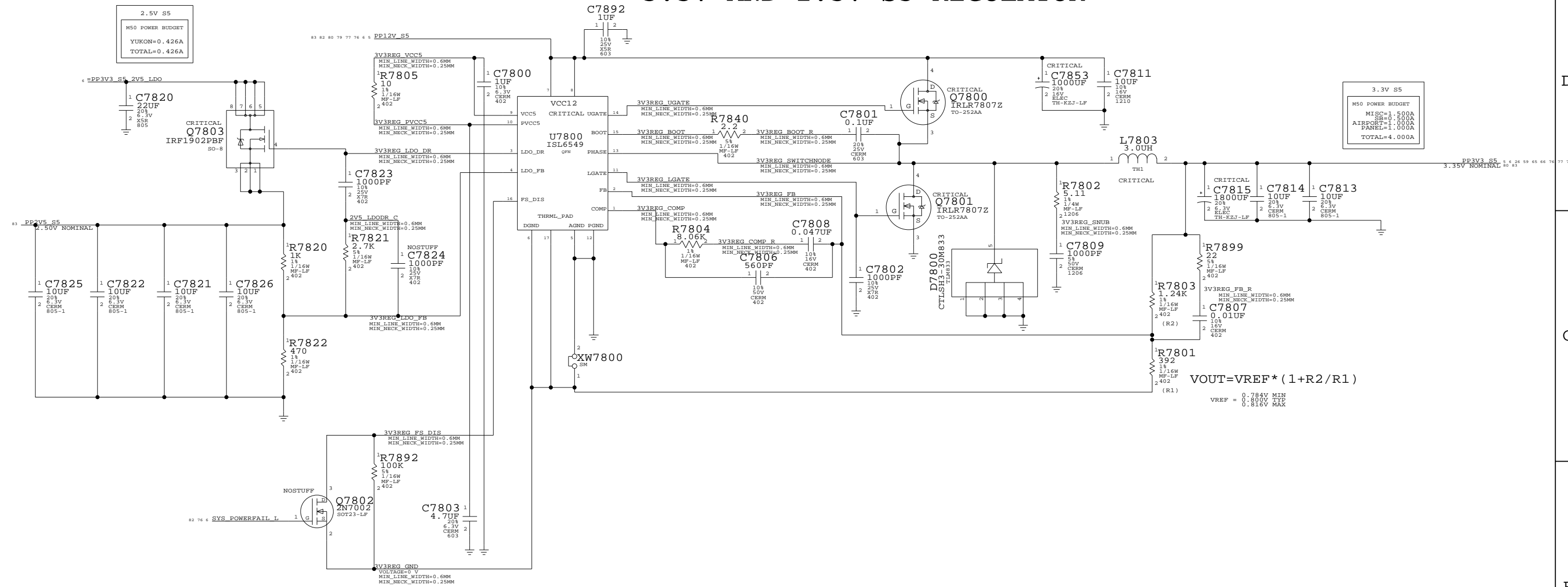
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	D	051-7032	??
SCALE	SHT	77 OF	97
NONE			

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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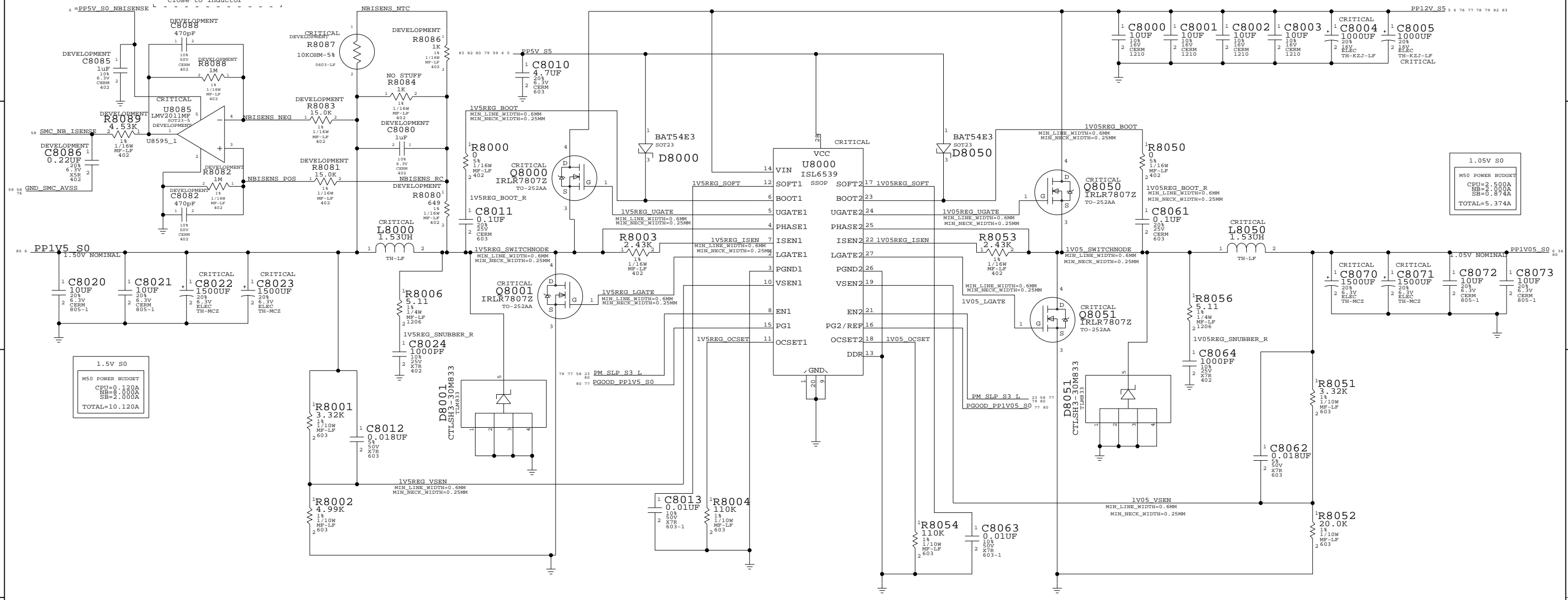
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	78 OF 97	
NONE			

TRUE

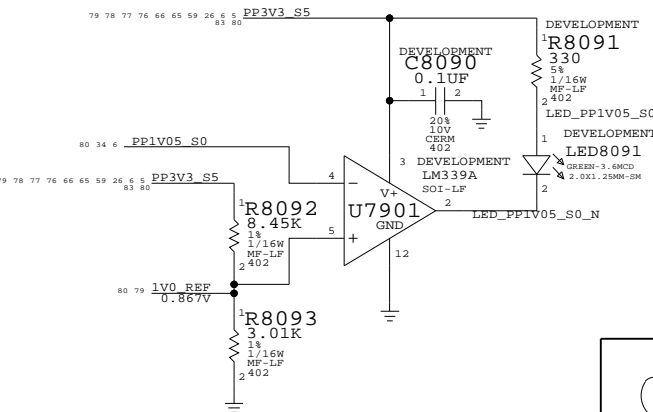
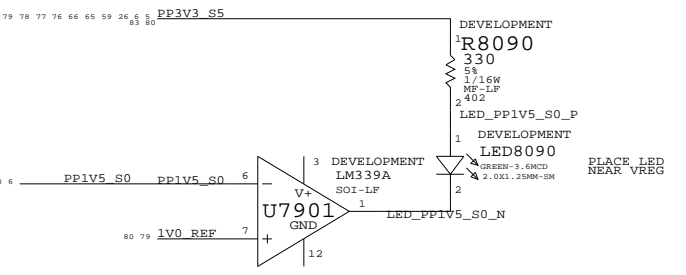
1.5V S0 AND 1.05V S0 RAILS

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V S0
M50 POWER BUDGET
CPU=0.120A
NB=0.000A
SB=2.000A
TOTAL=10.120A

1.05V S0
M50 POWER BUDGET
CPU=2.500A
NB=0.000A
SB=0.874A
TOTAL=5.374A



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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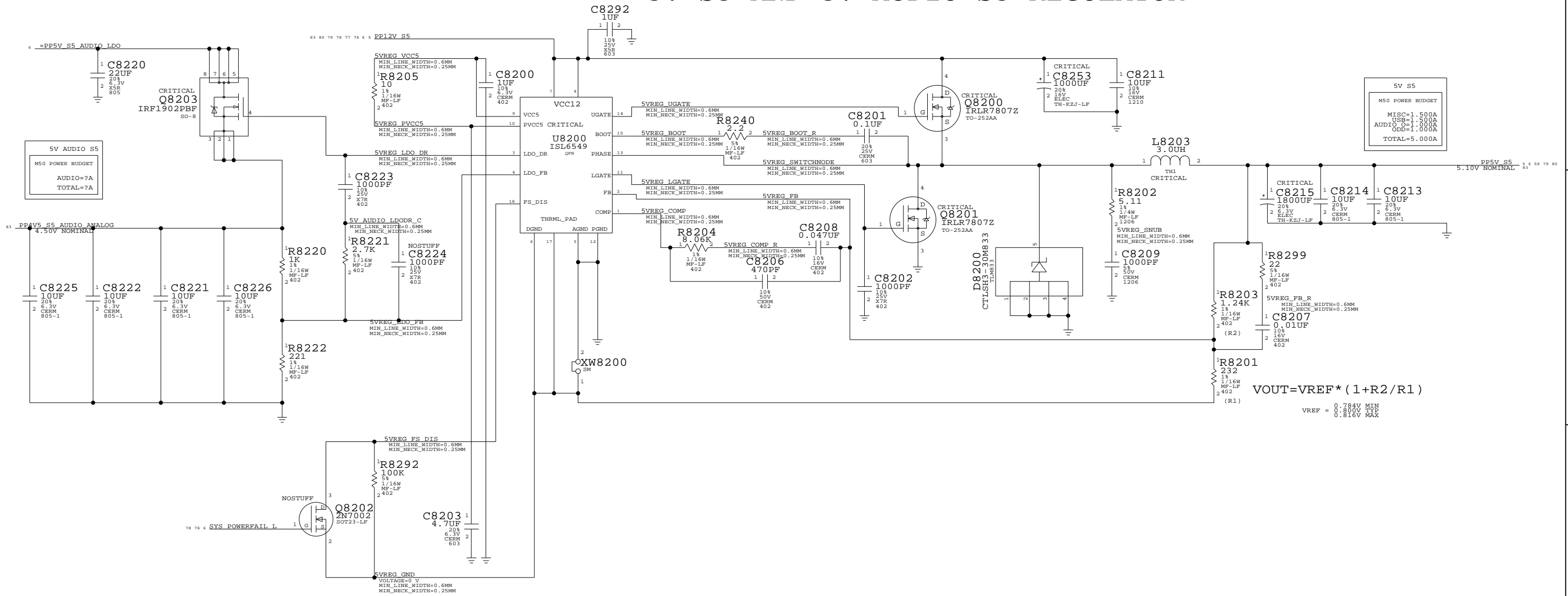
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	80 OF	97
NONE			

5V S5 AND 5V AUDIO S5 REGULATOR



$$V_{OUT} = V_{REF} * (1 + R2/R1)$$

$$V_{REF} = 0.784V \text{ MIN}$$

$$V_{REF} = 0.800V \text{ TYP}$$

$$V_{REF} = 0.816V \text{ MAX}$$

POWER SUPPLY 3.3V/5V MAIN SWITCH

5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

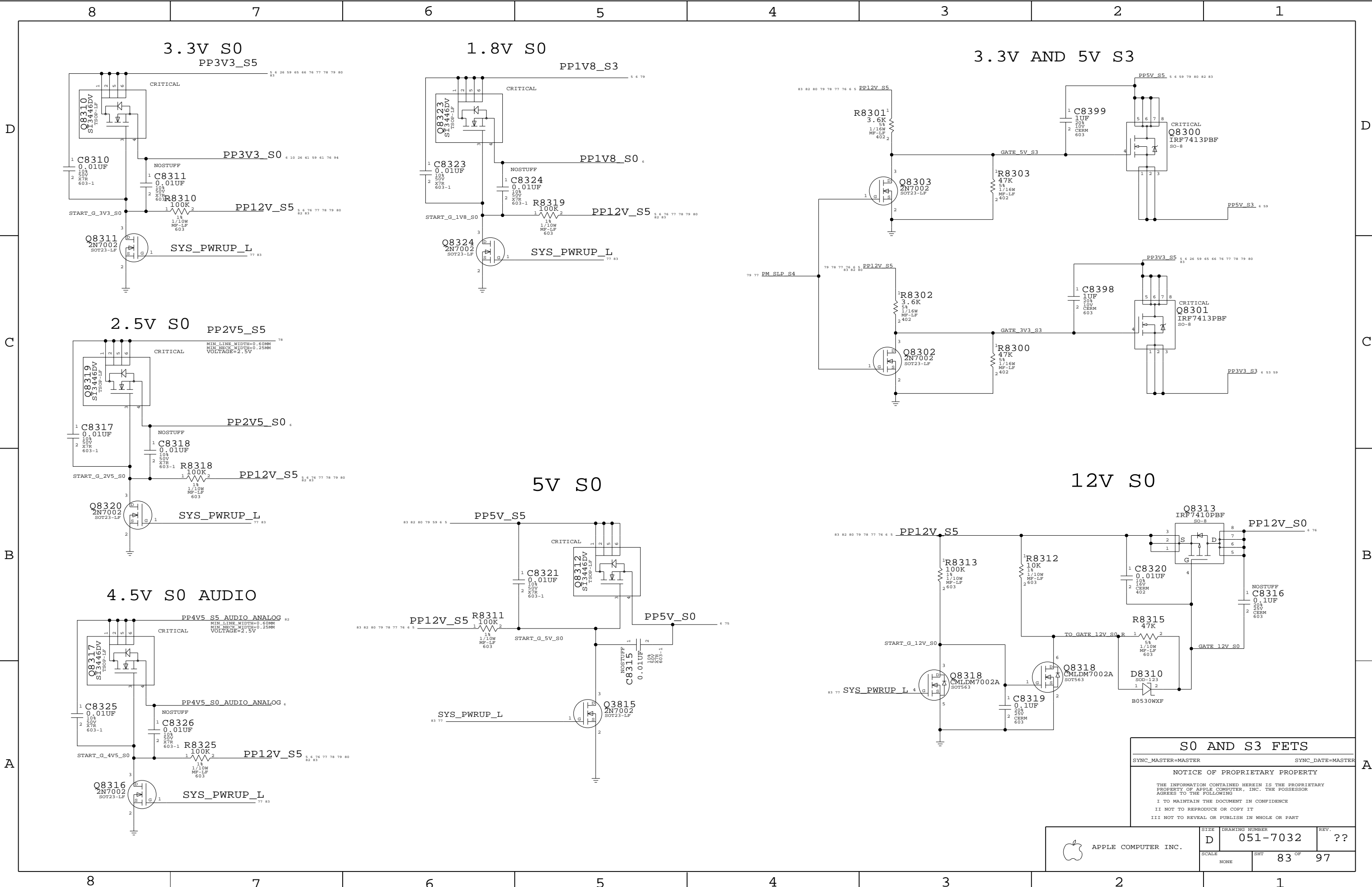
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

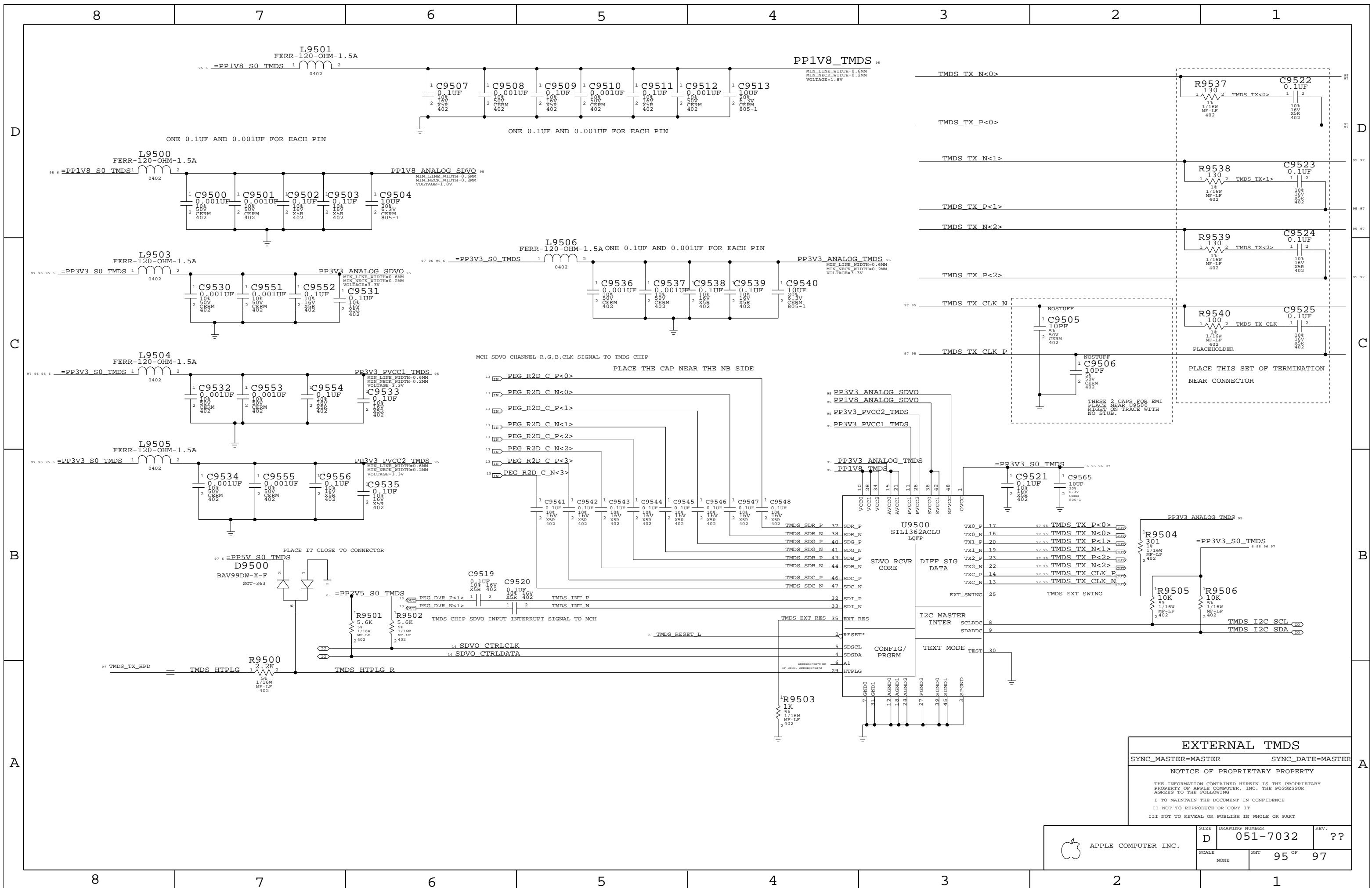
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. ??
	SCALE NONE	SHEET 83 OF 97	



EXTERNAL TMSD

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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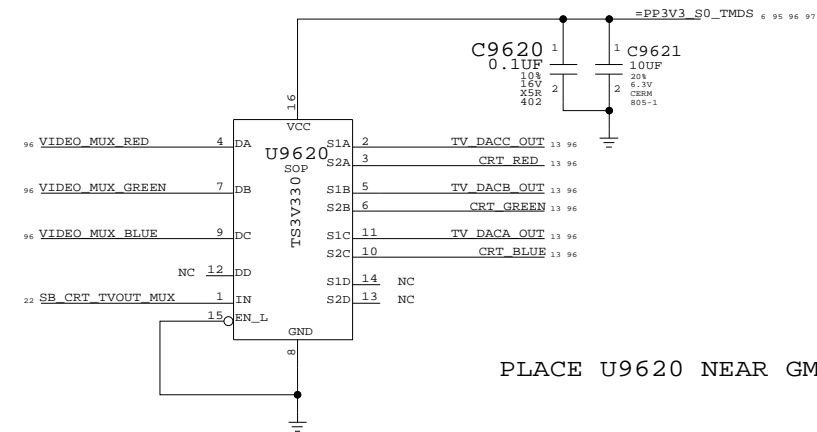
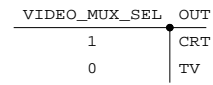
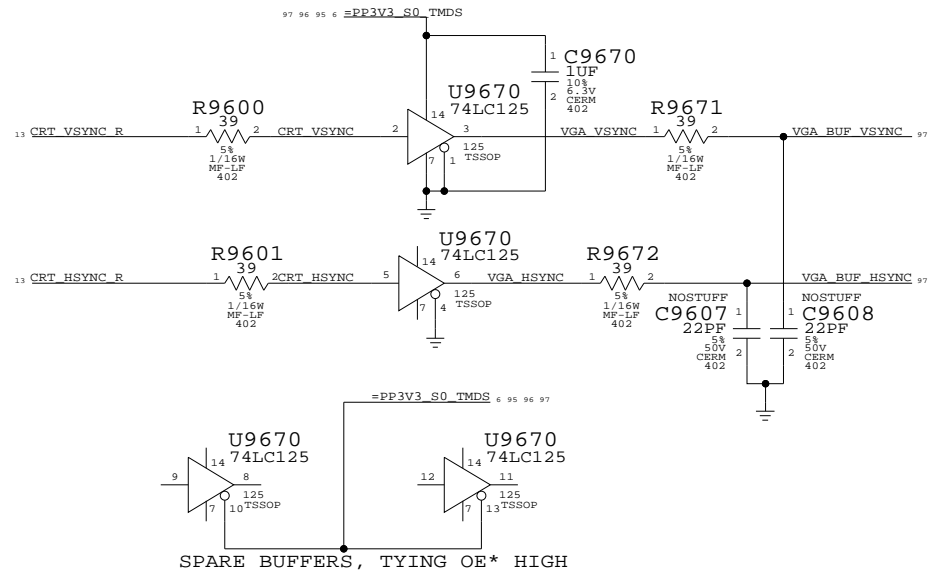
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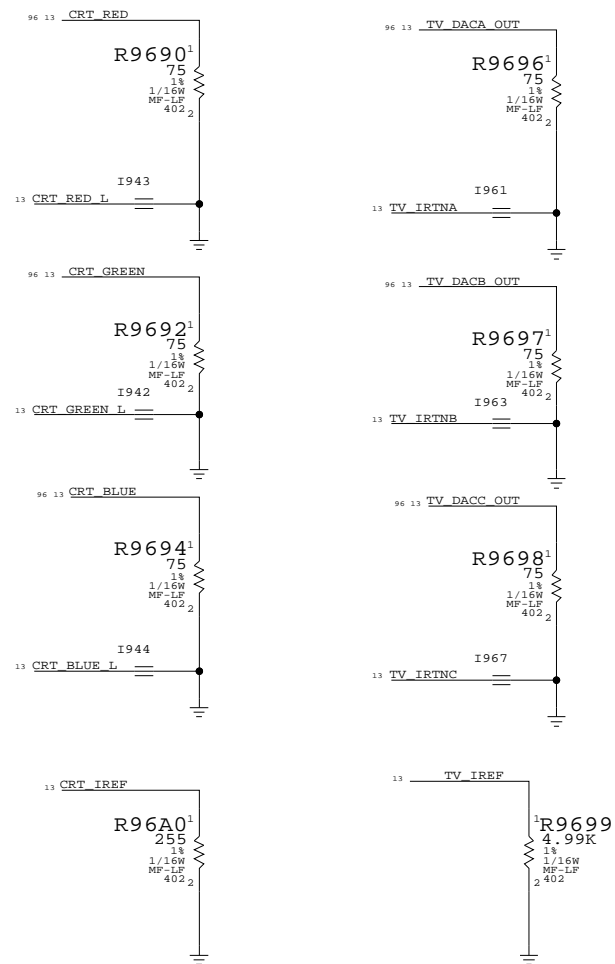
 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	??
SCALE	SHT	95 OF	97
NONE			

VGA SYNC BUFFERS

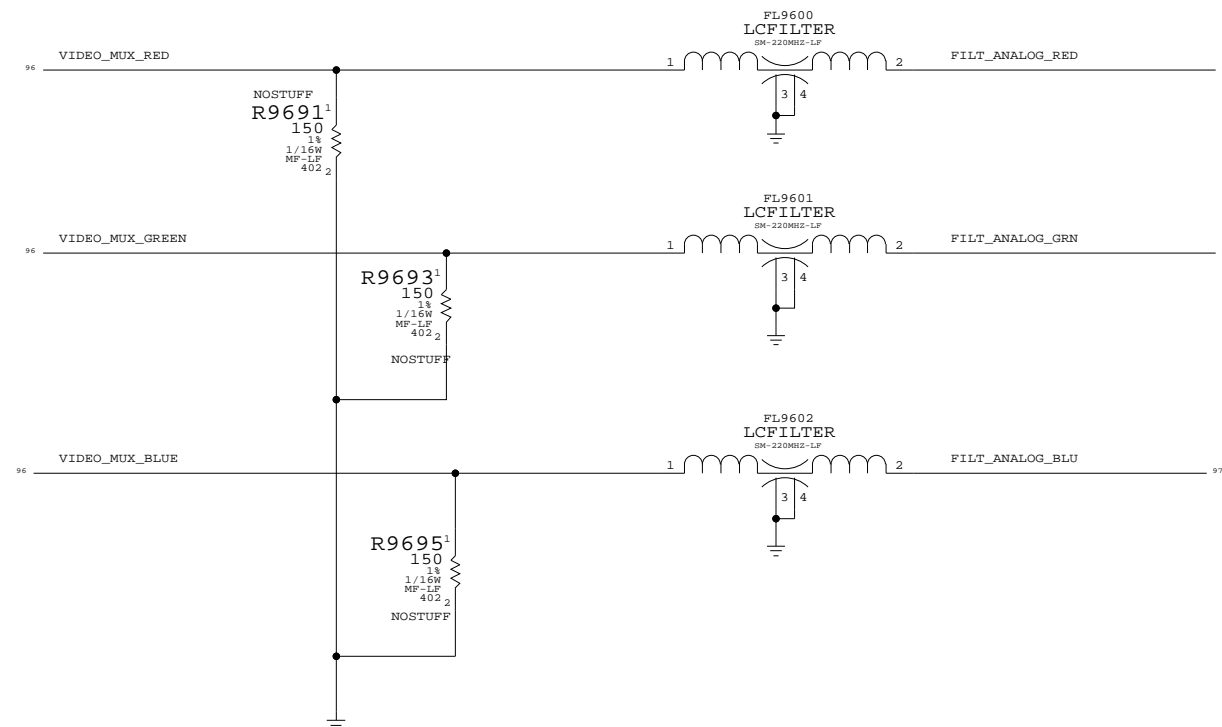


PLACE U9620 NEAR GMCH

PLACE RESISTORS AT NORTHBRIDGE



ANALOG FILTERING PLACE BY CONNECTOR

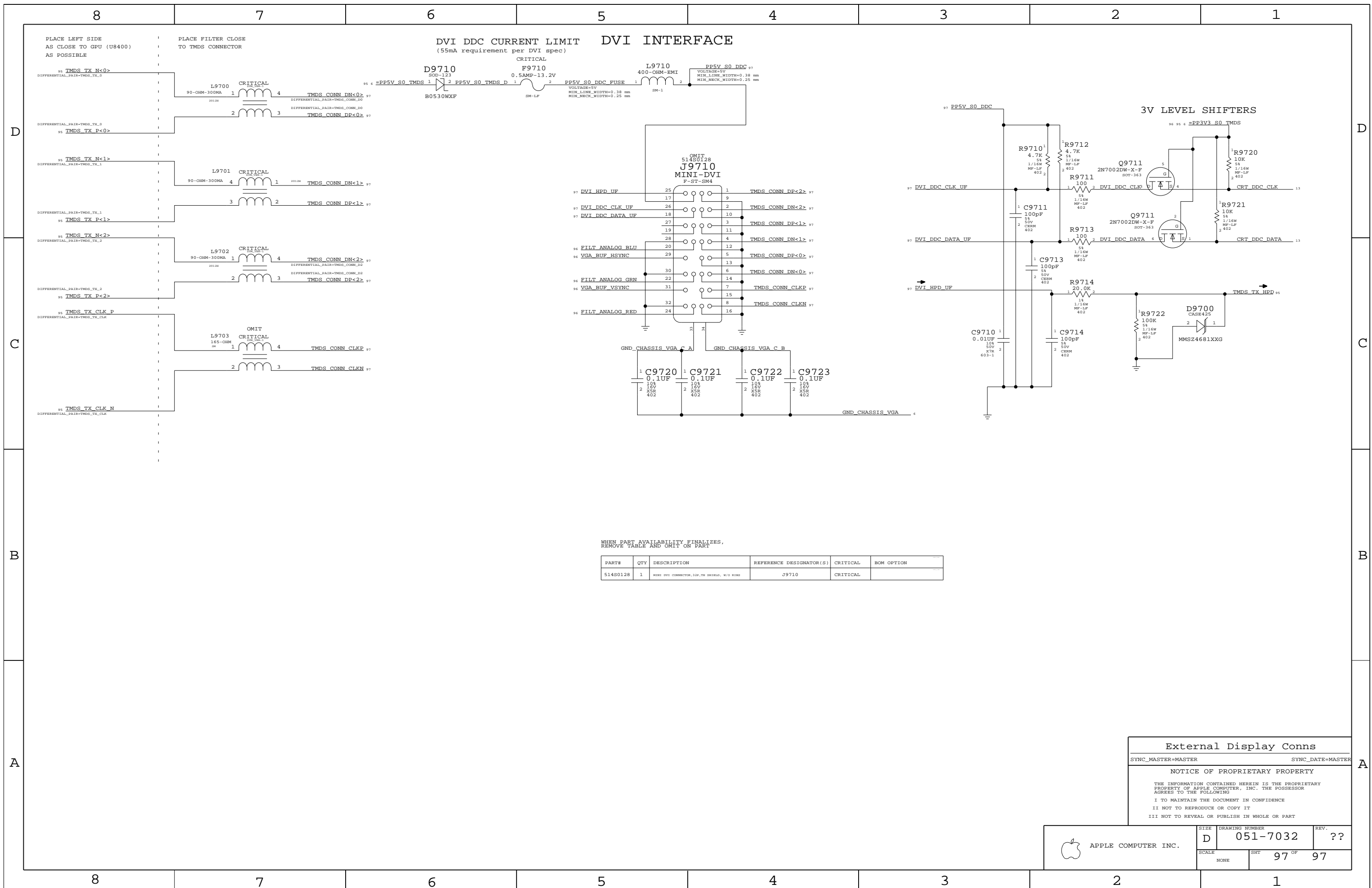


TMD5/Inverter/ExtVGA
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SCALE	SHT	96 OF	97
NONE			



DVI DDC CURRENT LIMIT DVI INTERFACE
(55mA requirement per DVI spec)

CRITICAL
514S0128
J9710
MINI-DVI
F-ST-SM4

WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 32P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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