

8

7

6

5

4

3

2

1

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

10/15/2004

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
B		328536	PRODUCTION RELEASED	DATE	DATE
				05/19/04	

PAGE

CONTENTS

1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL1162 TMDS TRANSMITTER
21	M10 ANALOG, POWER, GND

PAGE

CONTENTS

22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
30	PMU (POWER MANAGEMENT UNIT)
31	BATTERY CHARGER AND CONNECTOR
32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
33	3.3V / 5V SYSTEM POWER SUPPLIES
34	CPU CORE VOLTAGE POWER SUPPLY
35	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
37	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
38	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
39	FUNCTIONAL TEST POINTS
40	REVISION HISTORY (1 OF 1)
41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

SCHEM, SAPPHIRE, Q41B

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	cto	✓
INT_TMDS	✓	cto
NO_4XVCORE	✓	
INT_CLK	✓	
EXT_CLK		✓

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM, SAPPHIRE, Q41B	SCH1	
820-1688	1	PCBF, SAPPHIRE, Q41B	PCB1	

DIMENSIONS ARE IN MILLIMETERS

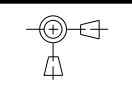
XX : _____

X.XX : _____

X.XXX : _____

ANGLES : _____

DO NOT SCALE DRAWING




THIRD ANGLE PROJECTION

METRIC

DRAPPER	DESIGN CR
ENG APPD	MFG APPD
QA APPD	DESIGNER
RELEASE	SCALE
	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D



Apple Computer Inc.

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SCHEM, SAPPHIRE, Q41B

DRAWING NUMBER 051-6694 REV. 02

SHT 1 OF 45

8

7

6

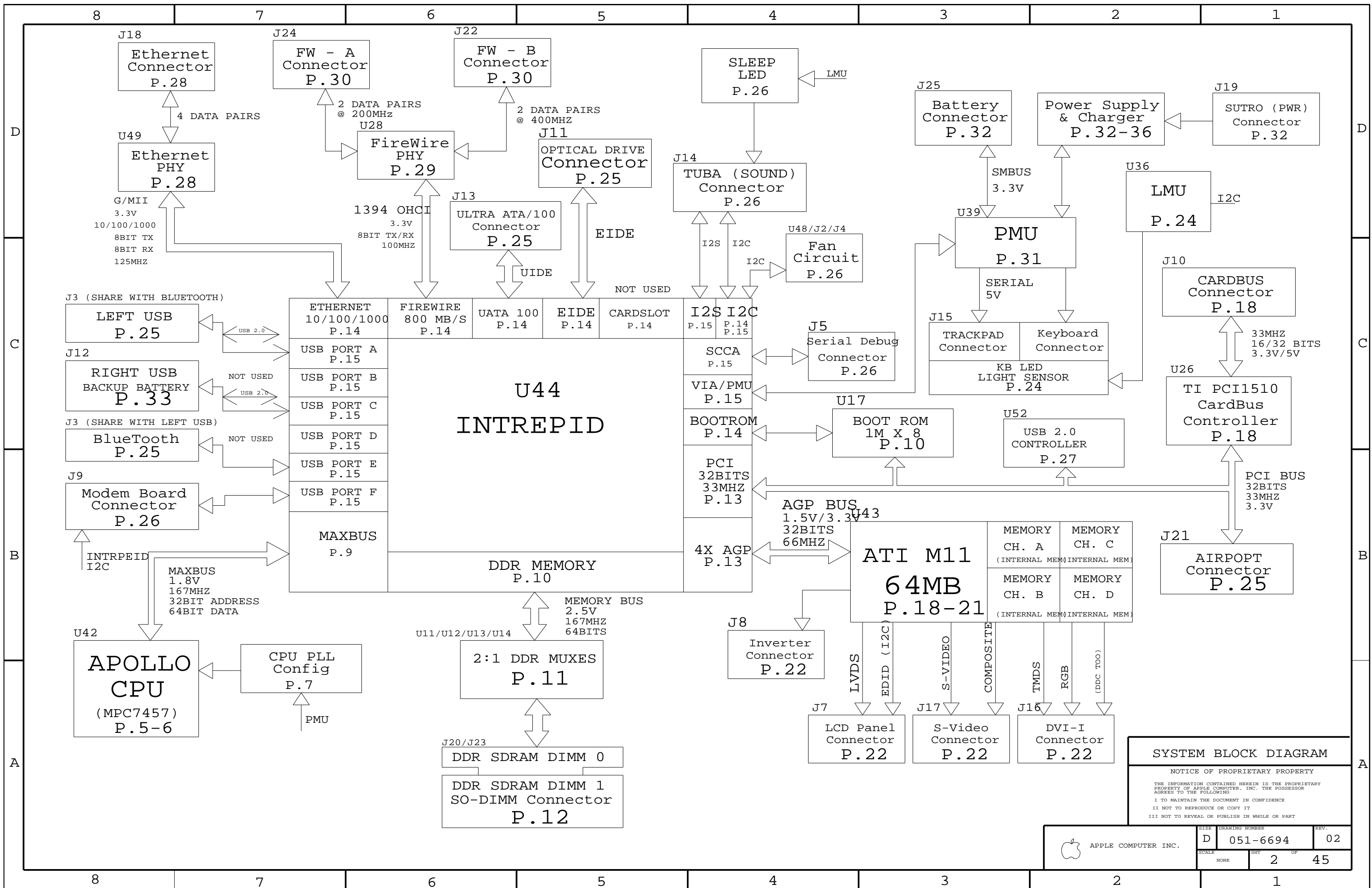
5

4

3

2

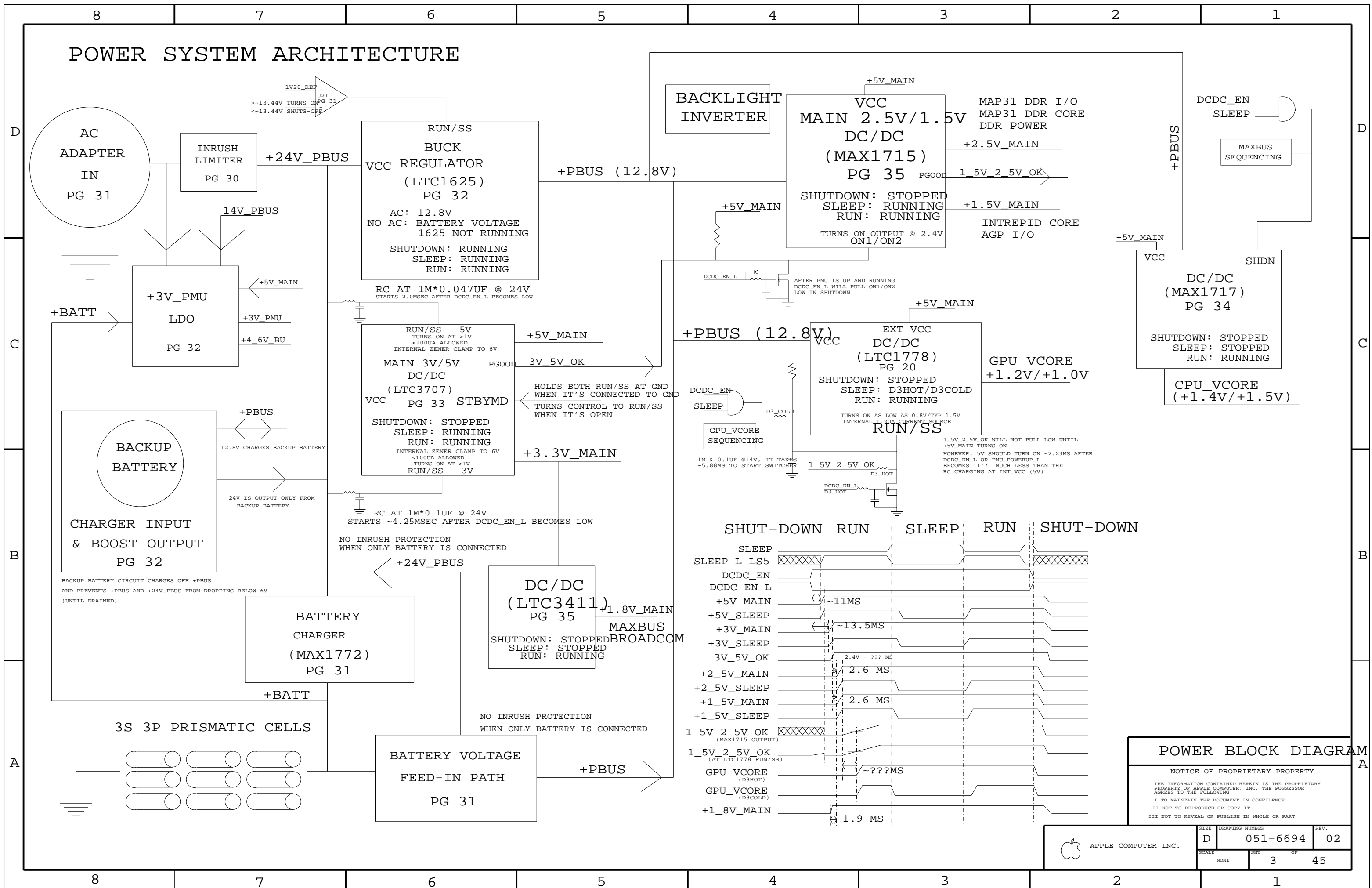
1



SYSTEM BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	NONE	SHT	OF
		3	45

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
 1/2 OZ CU THICKNESS: 0.7 MILS
 1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
 DIELECTRIC: FR-4
 LAYER COUNT: 12
 SIGNAL TRACE WIDTH: 4 MILS
 SIGNAL TRACE SPACING: 4 MILS
 PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

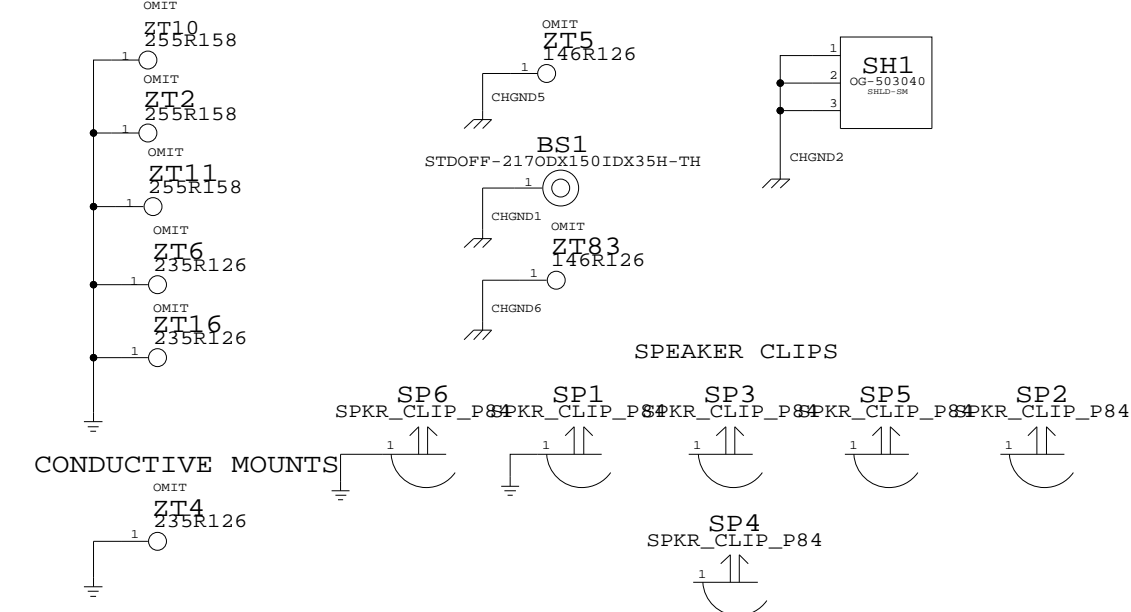
BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

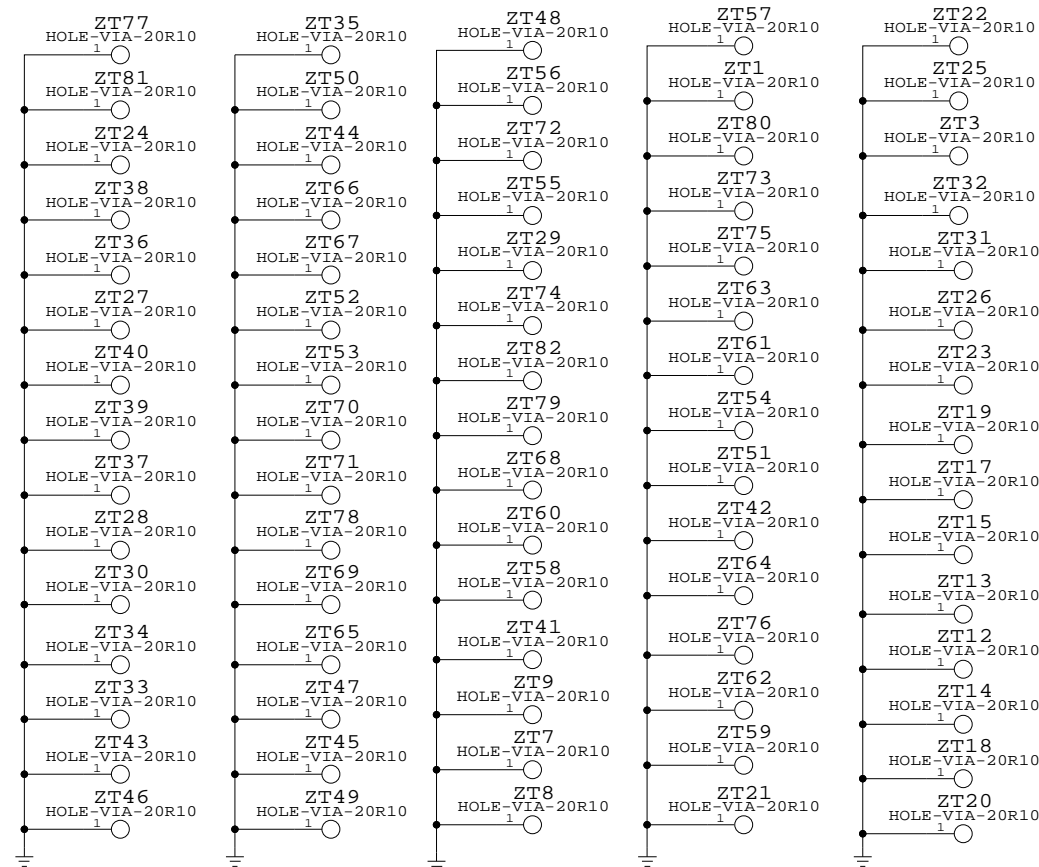
1	SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL) GROUND (1/2 OZ)
3	LAMINATE (4MIL) SIGNAL (1/2 OZ)
4	PREPREG (3MIL) SIGNAL (1/2 OZ)
5	LAMINATE (4MIL) GROUND (1/2 OZ)
6	PREPREG (2MIL) CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL) CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL) GROUND (1/2 OZ)
9	LAMINATE (4MIL) SIGNAL (1/2 OZ)
10	PREPREG (3MIL) SIGNAL (1/2 OZ)
11	LAMINATE (4MIL) GROUND (1/2 OZ)
12	PREPREG (3MIL) SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

ASICS HEATSINK MOUNTS
 CHASSIS MOUNTS
 SI/O AREA
 INVERTER



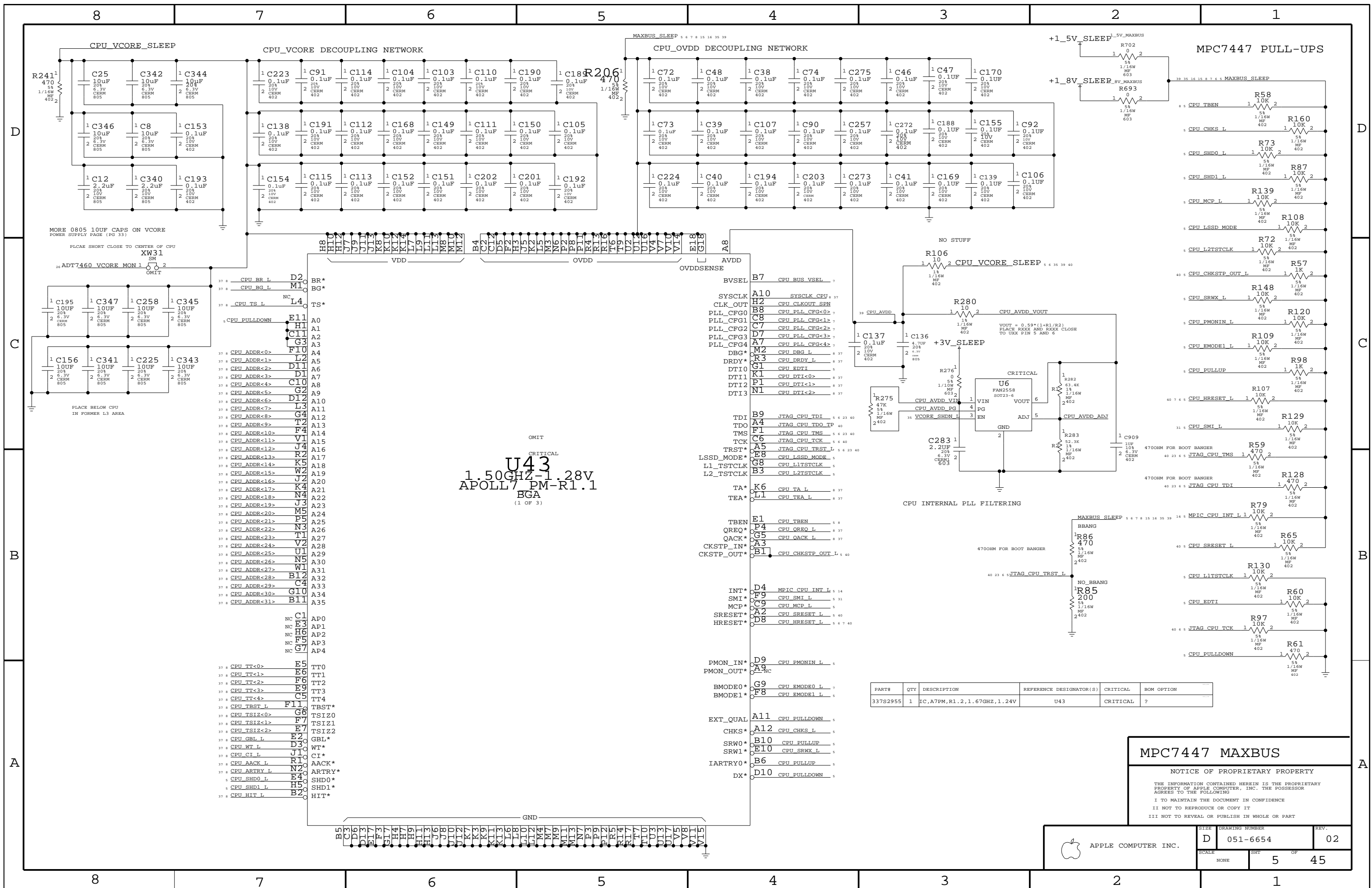
GROUND VIAS



BOARD INFORMATION

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	NONE	SHT	OF
		4	45



U43
1.50GHZ-1.28V
APOLL7 PM-R1.1
BGA
(1 OF 3)

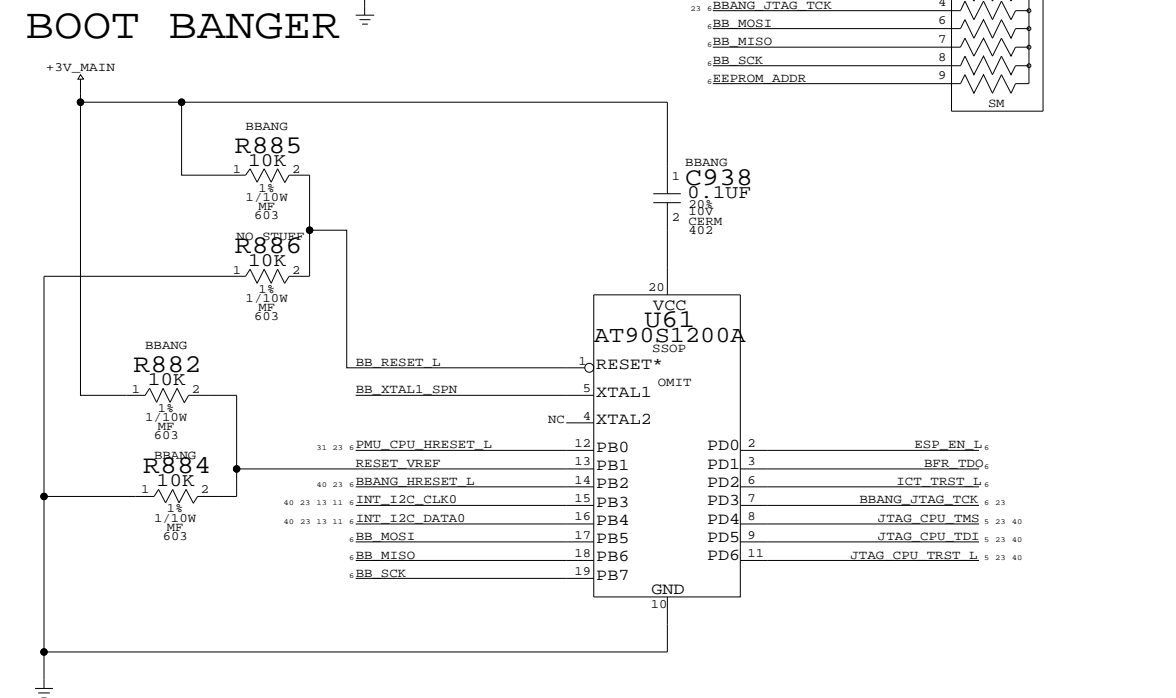
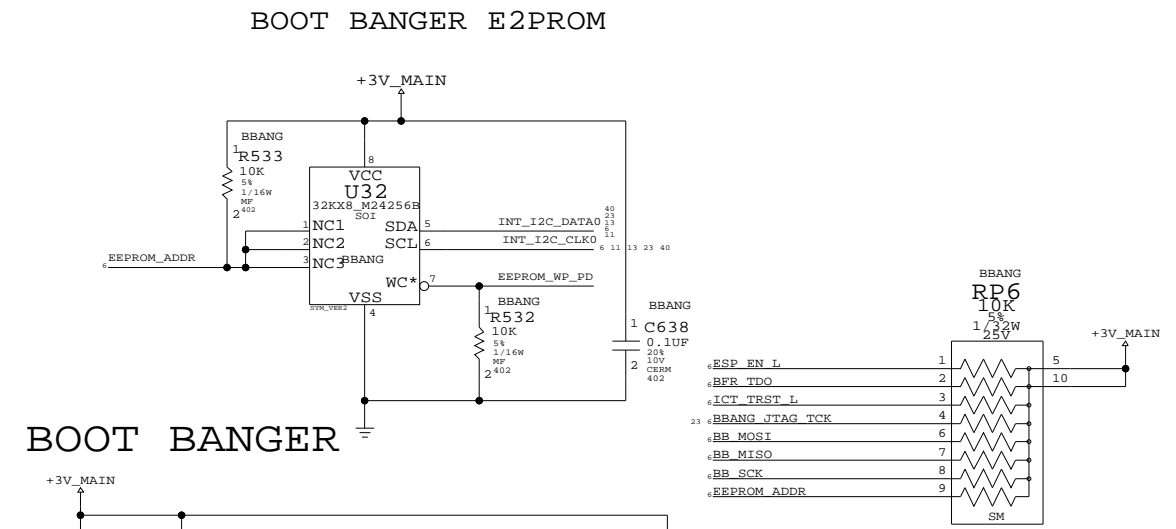
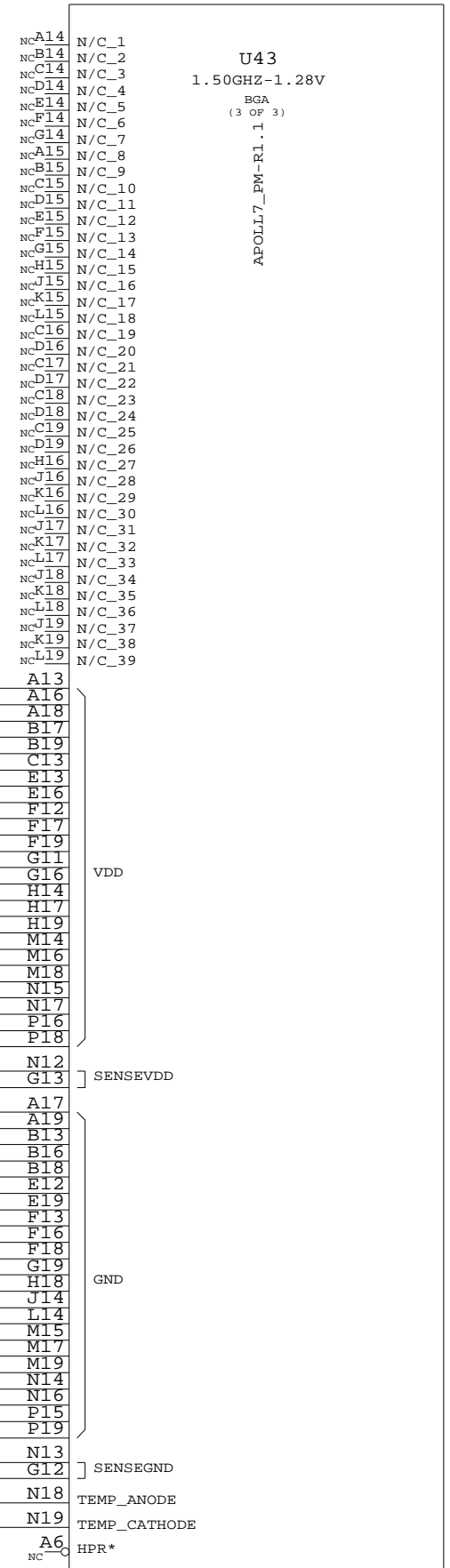
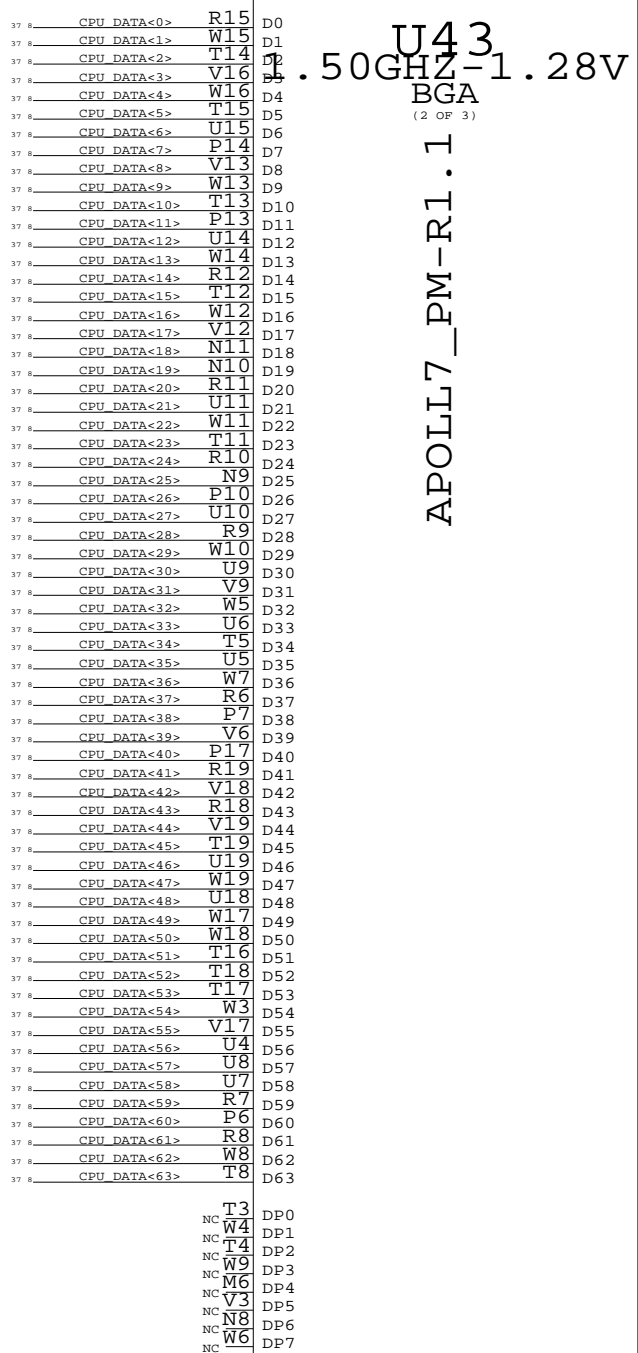
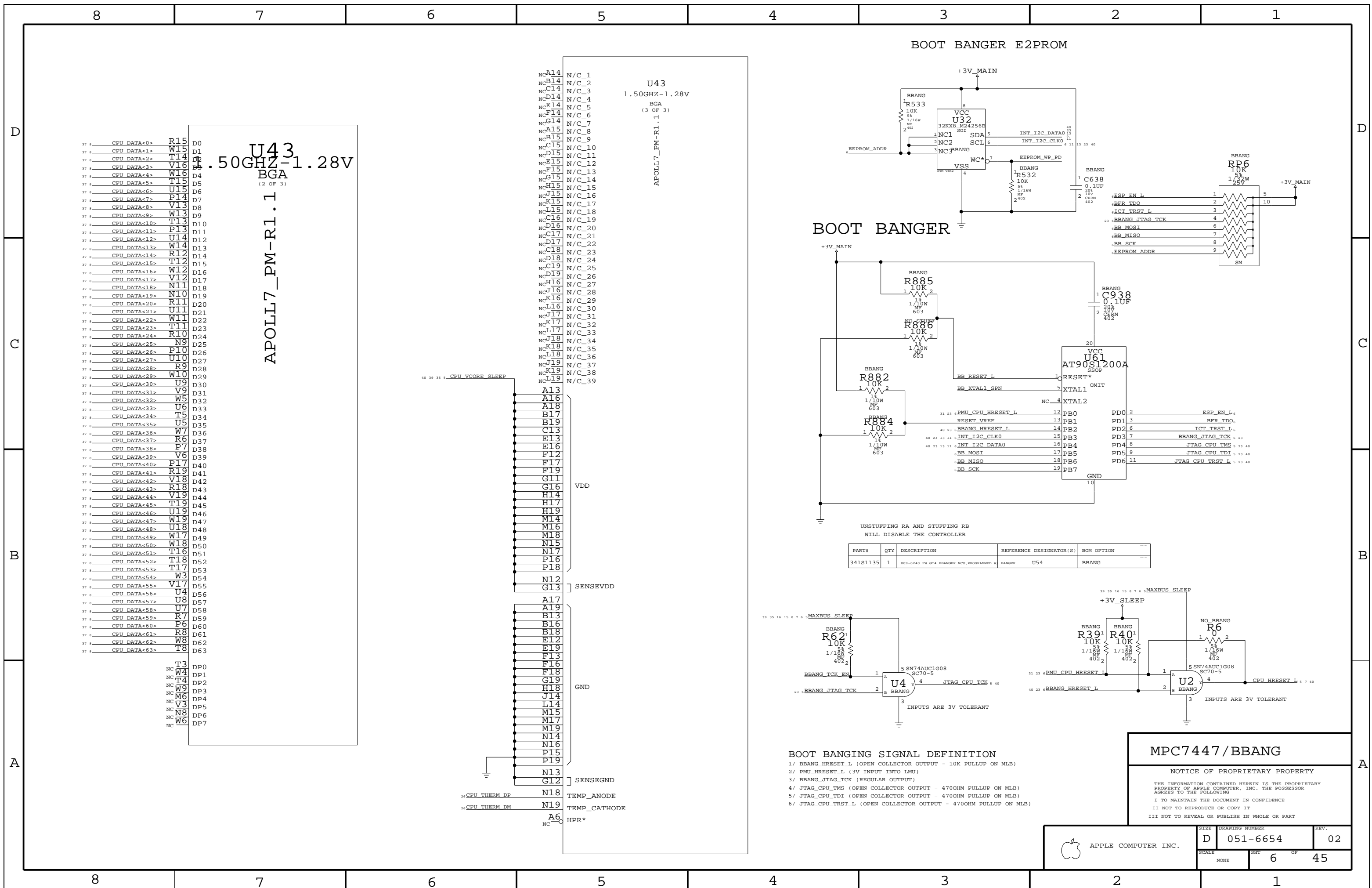
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,R1.2,1.67GHZ,1.24V	U43	CRITICAL	?

MPC7447 MAXBUS

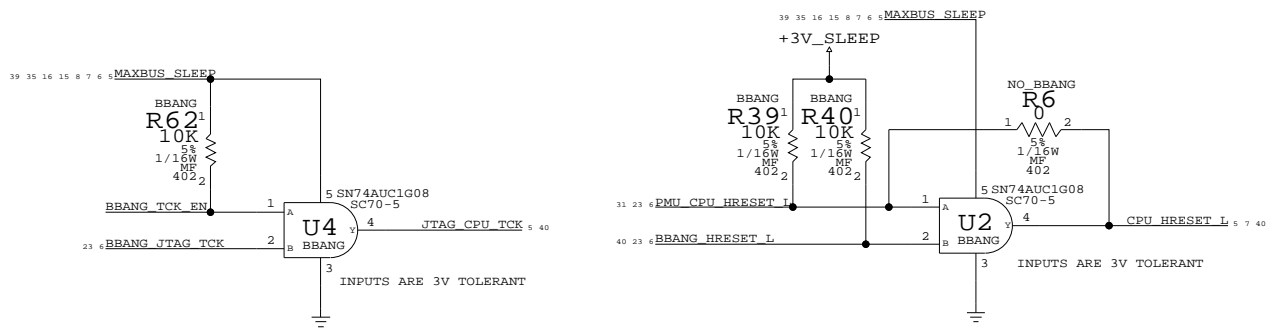
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6654	02
	SHEET	OF	
	5	45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	609-6240 PW QTA BBANGER MCU, PROGRAMMED W/BBANGER	U54	BBANG



- BOOT BANGING SIGNAL DEFINITION**
- 1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
 - 2/ PMU_HRESET_L (3V INPUT INTO LMU)
 - 3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
 - 4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
 - 5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
 - 6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

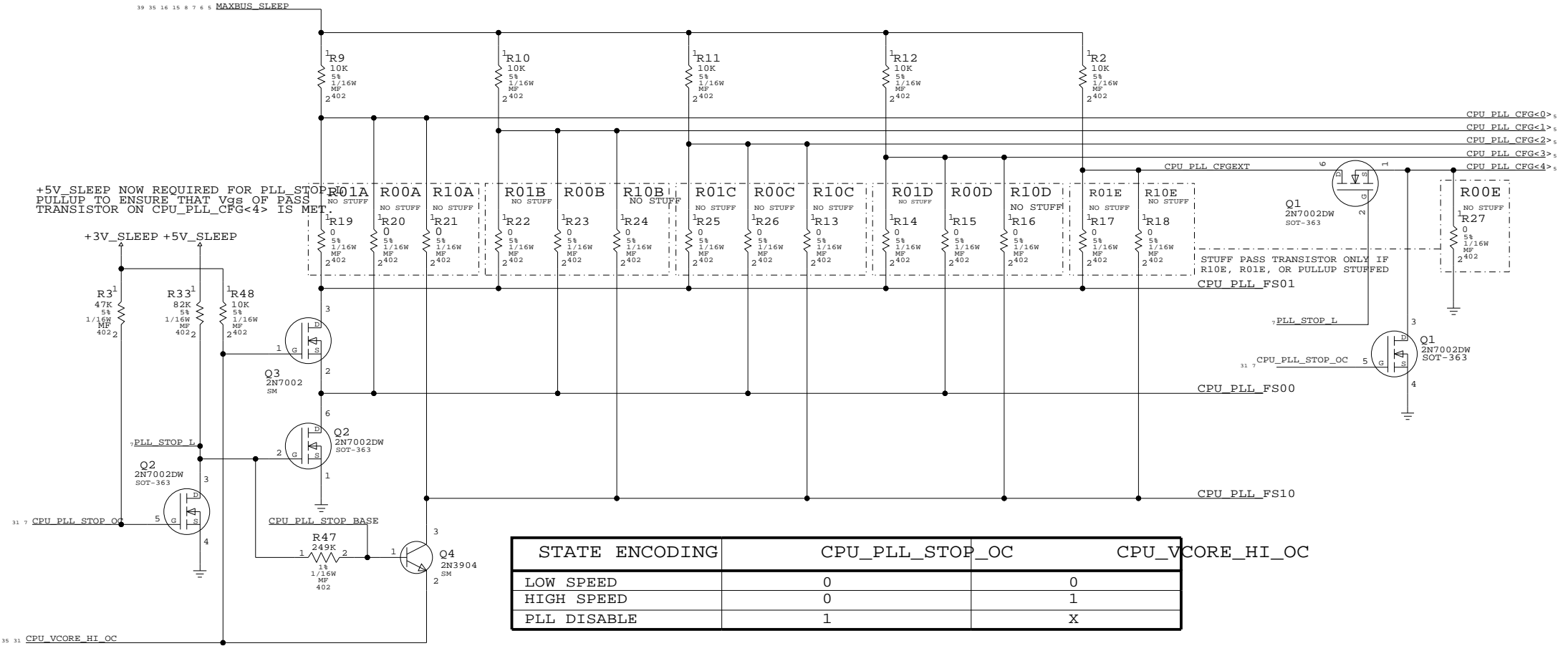
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ 133MHZ		CPU_PLL_CFG			
	(MHZ)		4	0123	HEX	
0.0X	PLL OFF		0	1111	0F	
1.0X	PLL BYPASS		0	0011	03	
2.0X	333	267	0	0100	04	
3.0X	500	400	0	1000	08	
4.0X	667	533	0	1010	0A	
5.0X	833	667	0	1011	0B	
5.5X	917	733	0	1001	09	
6.0X	1000	800	0	1101	0D	
6.5X	1083	867	0	0101	05	
7.0X	1167	933	0	0010	02	
7.5X	1250	1000	0	0001	01	
8.0X	1333	1067	0	1100	0C	
8.5X	1417	1133	0	0110	06	
9.0X	1500	1200	1	0111	07	
9.5X	1583	1267	0	0111	07	
10.0X	1667	1333	1	1010	1A	
10.5X	1750	1400	1	1000	18	
11.0X	1833	1467	1	1001	19	
11.5X	1917	1533	0	0000	00	
12.0X	2000	1600	1	1011	1B	
12.5X	2083	1667	1	1111	1F	
13.0X	2167	1733	1	0101	15	
13.5X	2250	1800	0	1110	0E	
14.0X	2333	1867	1	1100	1C	
15.0X	2500	2000	1	0001	11	
16.0X	2667	2133	1	1101	1D	
17.0X	2833	2267	1	0000	10	
18.0X	3000	2400	1	0010	12	
20.0X	3333	2667	1	0011	13	
21.0X	3500	2800	1	0100	14	
24.0X	4000	3200	1	0110	16	
28.0X	4667	3733	1	1110	1E	

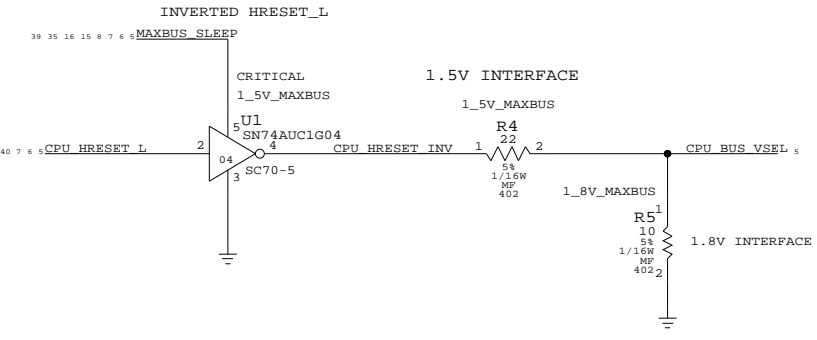
CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

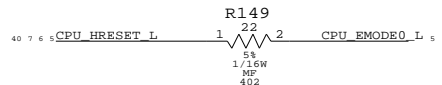
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC. DRAWING NUMBER: D 051-6694 REV. 02
SCALE: NONE SHEET 7 OF 45

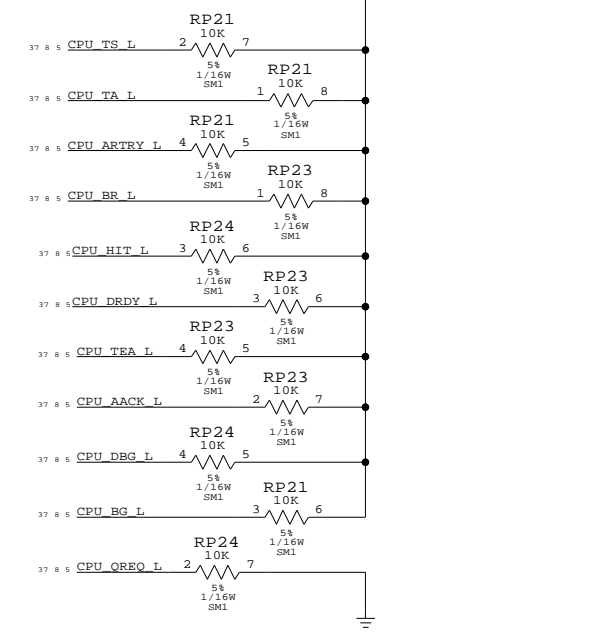
INTREPID BOOT STRAPS

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

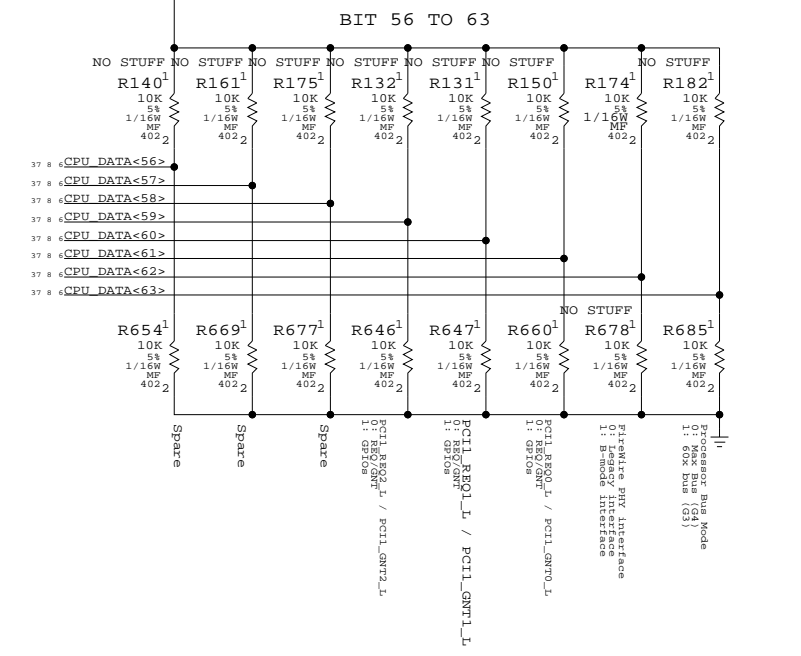
- 1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D46 - SELPCILSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS



INTREPID BOOT STRAPS



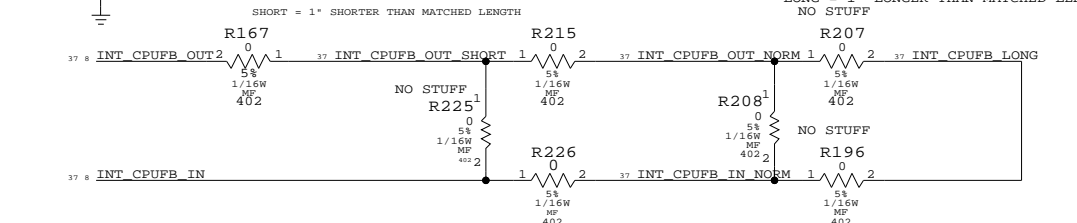
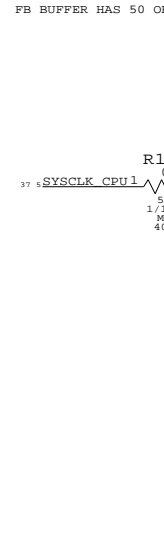
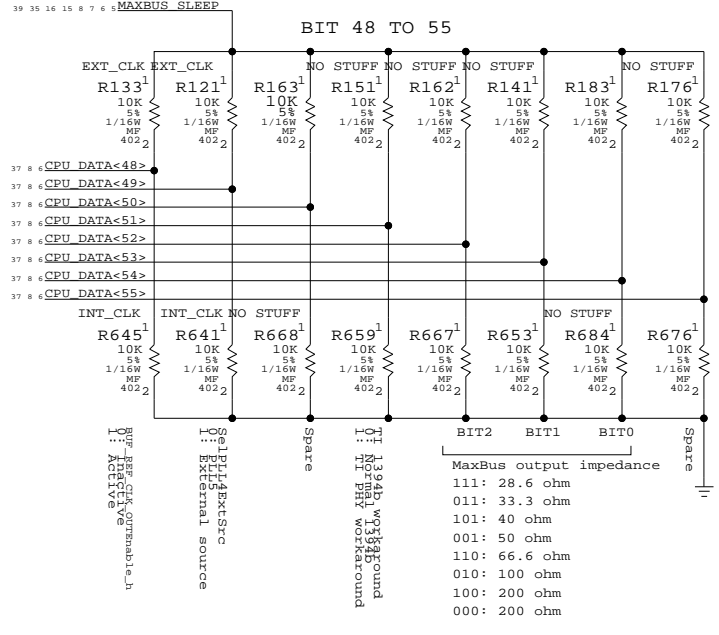
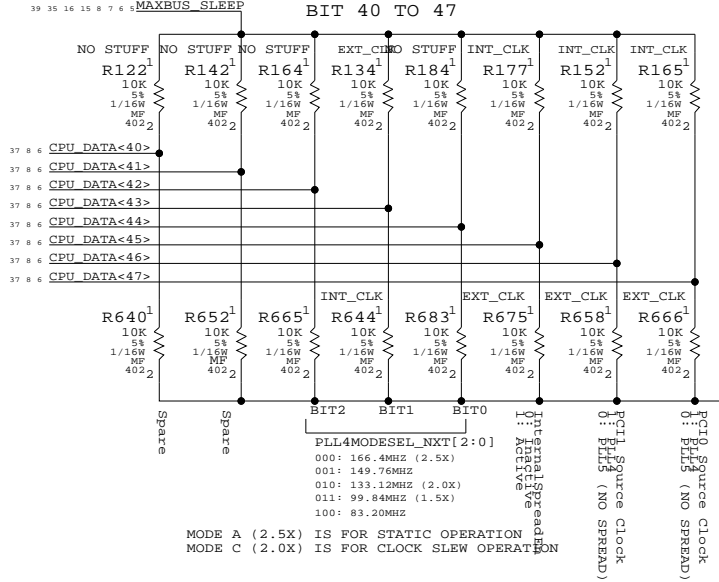
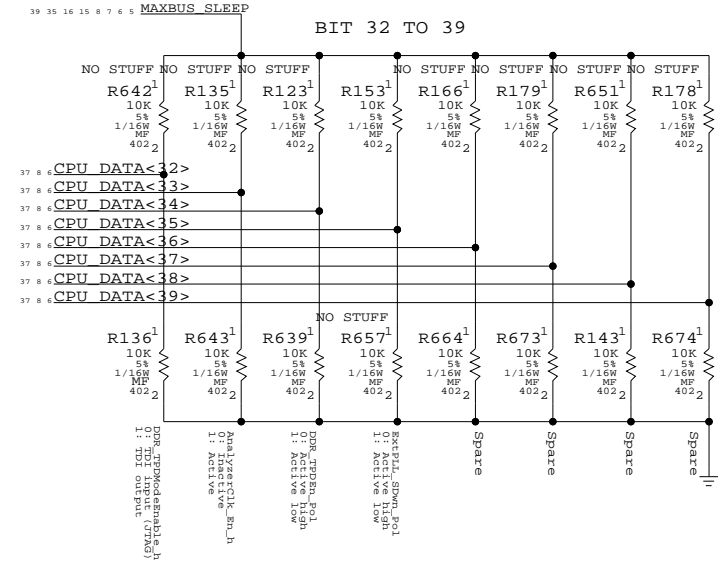
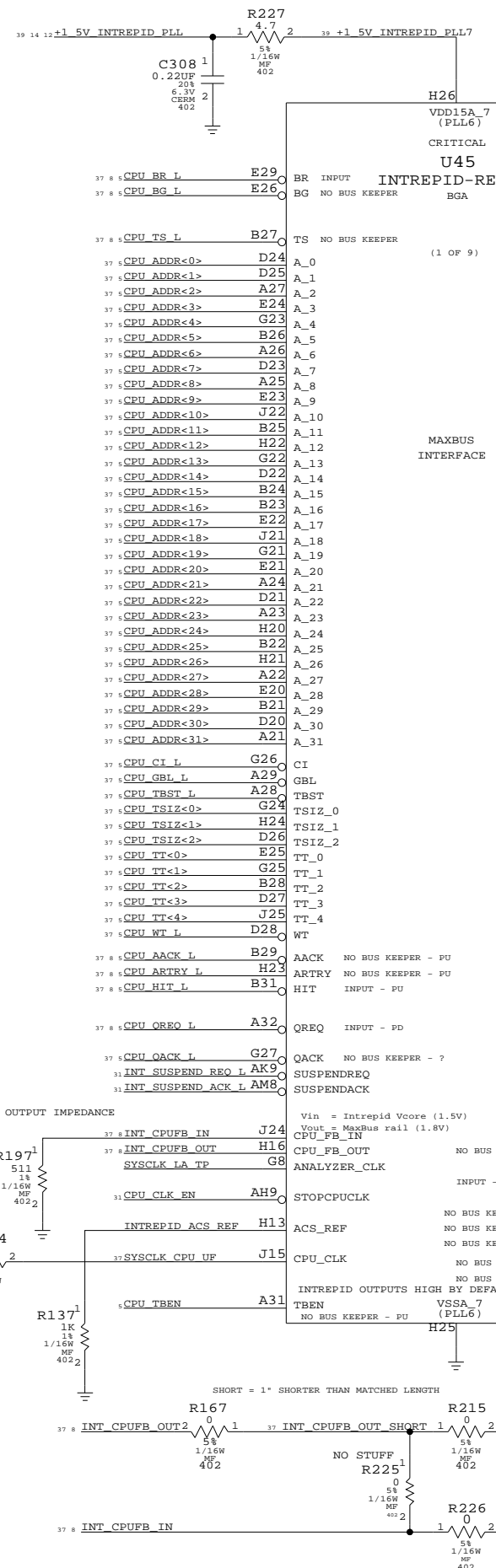
Intrepid MaxBus

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

- TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- NOT TO REPRODUCE OR COPY IT
- NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6694	02
SHEET		OF	
8		45	



MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW RATE REDUCTION

MaxBus output impedance

111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

D

C

B

A

D

C

B

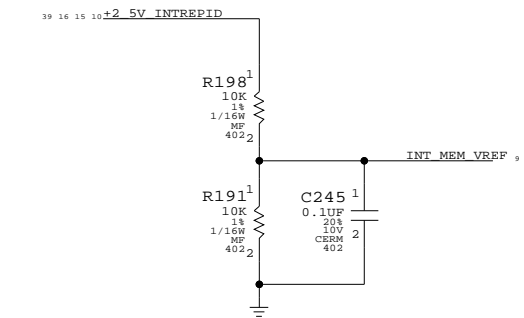
A

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

37 10 MEM_DATA<0>	AK32	DDR_DATA_0	H35	MEM_ADDR<0>	37
37 10 MEM_DATA<1>	AK33	DDR_DATA_1	G35	MEM_ADDR<1>	37
37 10 MEM_DATA<2>	AK31	DDR_DATA_2	G36	MEM_ADDR<2>	37
37 10 MEM_DATA<3>	AK35	DDR_DATA_3	F36	MEM_ADDR<3>	37
37 10 MEM_DATA<4>	AK36	DDR_DATA_4	F35	MEM_ADDR<4>	37
37 10 MEM_DATA<5>	AJ32	DDR_DATA_5	E35	MEM_ADDR<5>	37
37 10 MEM_DATA<6>	AJ35	DDR_DATA_6	E36	MEM_ADDR<6>	37
37 10 MEM_DATA<7>	AJ36	DDR_DATA_7	G32	MEM_ADDR<7>	37
37 10 MEM_DATA<8>	AG33	DDR_DATA_8	D36	MEM_ADDR<8>	37
37 10 MEM_DATA<9>	AG35	DDR_DATA_9	H36	MEM_ADDR<9>	37
37 10 MEM_DATA<10>	AH35	DDR_DATA_10	G33	MEM_ADDR<10>	37
37 10 MEM_DATA<11>	AG36	DDR_DATA_11	H33	MEM_ADDR<11>	37
37 10 MEM_DATA<12>	AH36	DDR_DATA_12	D35	MEM_ADDR<12>	37
37 10 MEM_DATA<13>	AH32	DDR_DATA_13	L30	MEM_BA<0>	37
37 10 MEM_DATA<14>	AG32	DDR_DATA_14	M29	MEM_BA<1>	37
37 10 MEM_DATA<15>	AG31	DDR_DATA_15	DDRCS_0	AN34	MEM_CS L<0>
37 10 MEM_DATA<16>	AE32	DDR_DATA_16	DDRCS_1	AN36	MEM_CS L<1>
37 10 MEM_DATA<17>	AF35	DDR_DATA_17	DDRCS_2	AL35	MEM_CS L<2>
37 10 MEM_DATA<18>	AF36	DDR_DATA_18	DDRCS_3	AL33	MEM_CS L<3>
37 10 MEM_DATA<19>	AE36	DDR_DATA_19	DDR_DQS_0	AJ31	MEM_DQS<0>
37 10 MEM_DATA<20>	AE35	DDR_DATA_20	DDR_DQS_1	AH31	MEM_DQS<1>
37 10 MEM_DATA<21>	AE33	DDR_DATA_21	DDR_DQS_2	AD32	MEM_DQS<2>
37 10 MEM_DATA<22>	AD36	DDR_DATA_22	DDR_DQS_3	AB30	MEM_DQS<3>
37 10 MEM_DATA<23>	AD35	DDR_DATA_23	DDR_DQS_4	V30	MEM_DQS<4>
37 10 MEM_DATA<24>	AA36	DDR_DATA_24	DDR_DQS_5	OP32	MEM_DQS<5>
37 10 MEM_DATA<25>	AA35	DDR_DATA_25	DDR_DQS_6	N29	MEM_DQS<6>
37 10 MEM_DATA<26>	AA33	DDR_DATA_26	DDR_DQS_7	L32	MEM_DQS<7>
37 10 MEM_DATA<27>	AB36	DDR_DATA_27	DDR_DM_0	AJ33	MEM_DQM<0>
37 10 MEM_DATA<28>	AB35	DDR_DATA_28	DDR_DM_1	AH33	MEM_DQM<1>
37 10 MEM_DATA<29>	AC36	DDR_DATA_29	DDR_DM_2	AD33	MEM_DQM<2>
37 10 MEM_DATA<30>	AA32	DDR_DATA_30	DDR_DM_3	AC35	MEM_DQM<3>
37 10 MEM_DATA<31>	AB33	DDR_DATA_31	DDR_DM_4	T35	MEM_DQM<4>
37 10 MEM_DATA<32>	V36	DDR_DATA_32	DDR_DM_5	OT33	MEM_DQM<5>
37 10 MEM_DATA<33>	U33	DDR_DATA_33	DDR_DM_6	N32	MEM_DQM<6>
37 10 MEM_DATA<34>	U32	DDR_DATA_34	DDR_DM_7	L33	MEM_DQM<7>
37 10 MEM_DATA<35>	V35	DDR_DATA_35	DDRRAS	L29	MEM_RAS L
37 10 MEM_DATA<36>	T30	DDR_DATA_36	DDRCAS	H32	MEM_CAS L
37 10 MEM_DATA<37>	U36	DDR_DATA_37	DDRWE	K30	MEM_WE L
37 10 MEM_DATA<38>	U35	DDR_DATA_38	DDRCKE0	AN35	MEM_CKE<0>
37 10 MEM_DATA<39>	T36	DDR_DATA_39	DDRCKE1	AM35	MEM_CKE<1>
37 10 MEM_DATA<40>	P33	DDR_DATA_40	DDRCKE2	AM36	MEM_CKE<2>
37 10 MEM_DATA<41>	R30	DDR_DATA_41	DDRCKE3	AL36	MEM_CKE<3>
37 10 MEM_DATA<42>	P35	DDR_DATA_42	DDR_SELHI_0	AB32	MEM_MUXSEL H<0>
37 10 MEM_DATA<43>	P36	DDR_DATA_43	DDR_SELHI_1	AE29	MEM_MUXSEL H<1>
37 10 MEM_DATA<44>	R36	DDR_DATA_44	DDR_SELLO_0	N30	MEM_MUXSEL L<0>
37 10 MEM_DATA<45>	R35	DDR_DATA_45	DDR_SELLO_1	T32	MEM_MUXSEL L<1>
37 10 MEM_DATA<46>	R33	DDR_DATA_46	DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK A0 UF
37 10 MEM_DATA<47>	R32	DDR_DATA_47	DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK A0 L UF
37 10 MEM_DATA<48>	N35	DDR_DATA_48	DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK A1 UF
37 10 MEM_DATA<49>	M36	DDR_DATA_49	DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK A1 L UF
37 10 MEM_DATA<50>	L35	DDR_DATA_50	DDR_MCLK_2_P	Y30	INT_DDRCLK2 P TP
37 10 MEM_DATA<51>	M35	DDR_DATA_51	DDR_MCLK_2_N	W30	INT_DDRCLK2 N TP
37 10 MEM_DATA<52>	M33	DDR_DATA_52	DDR_MCLK_3_P	W32	SYSCLK_DDRCLK B0 UF
37 10 MEM_DATA<53>	L36	DDR_DATA_53	DDR_MCLK_3_N	W33	SYSCLK_DDRCLK B0 L UF
37 10 MEM_DATA<54>	N33	DDR_DATA_54	DDR_MCLK_4_P	V32	SYSCLK_DDRCLK B1 UF
37 10 MEM_DATA<55>	M30	DDR_DATA_55	DDR_MCLK_4_N	V32	SYSCLK_DDRCLK B1 L UF
37 10 MEM_DATA<56>	J32	DDR_DATA_56	DDR_MCLK_5_P	W35	INT_DDRCLK5 P TP
37 10 MEM_DATA<57>	J33	DDR_DATA_57	DDR_MCLK_5_N	W36	INT_DDRCLK5 N TP
37 10 MEM_DATA<58>	J35	DDR_DATA_58	DDR_REF	AA22	INT MEM VREF H
37 10 MEM_DATA<59>	K32	DDR_DATA_59	DDR_VREF_0	Y22	INT MEM VREF
37 10 MEM_DATA<60>	K33	DDR_DATA_60	DDR_VREF_1	T22	
37 10 MEM_DATA<61>	J36	DDR_DATA_61			
37 10 MEM_DATA<62>	K36	DDR_DATA_62			
37 10 MEM_DATA<63>	K35	DDR_DATA_63			

MEM_VREF



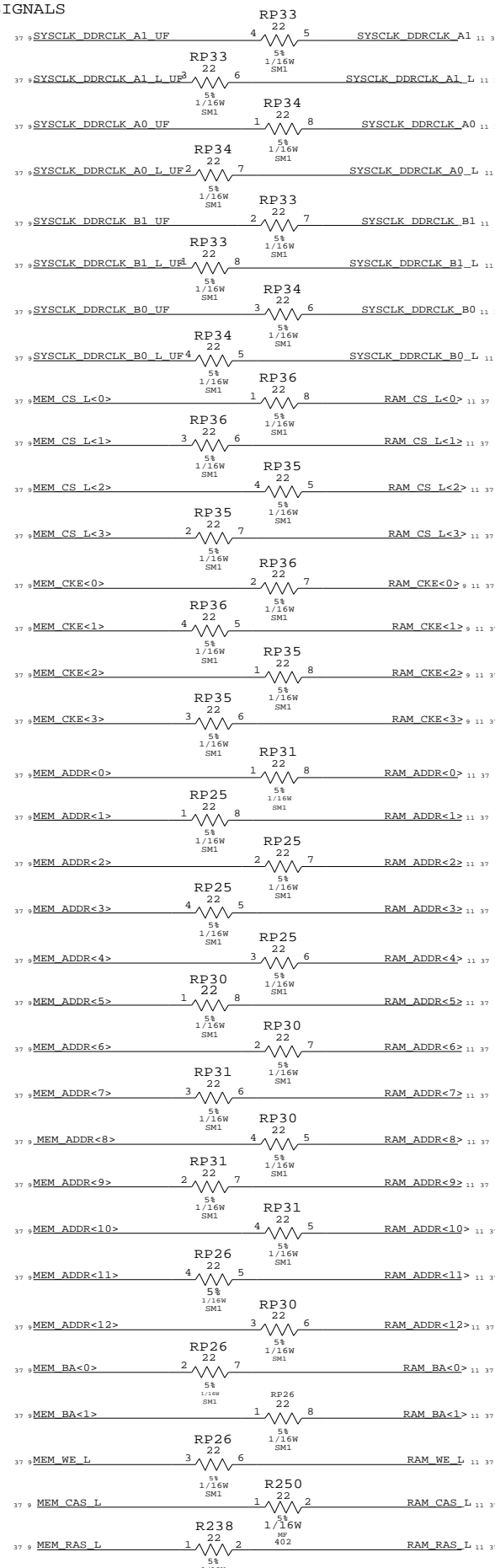
CLOCKS

CS

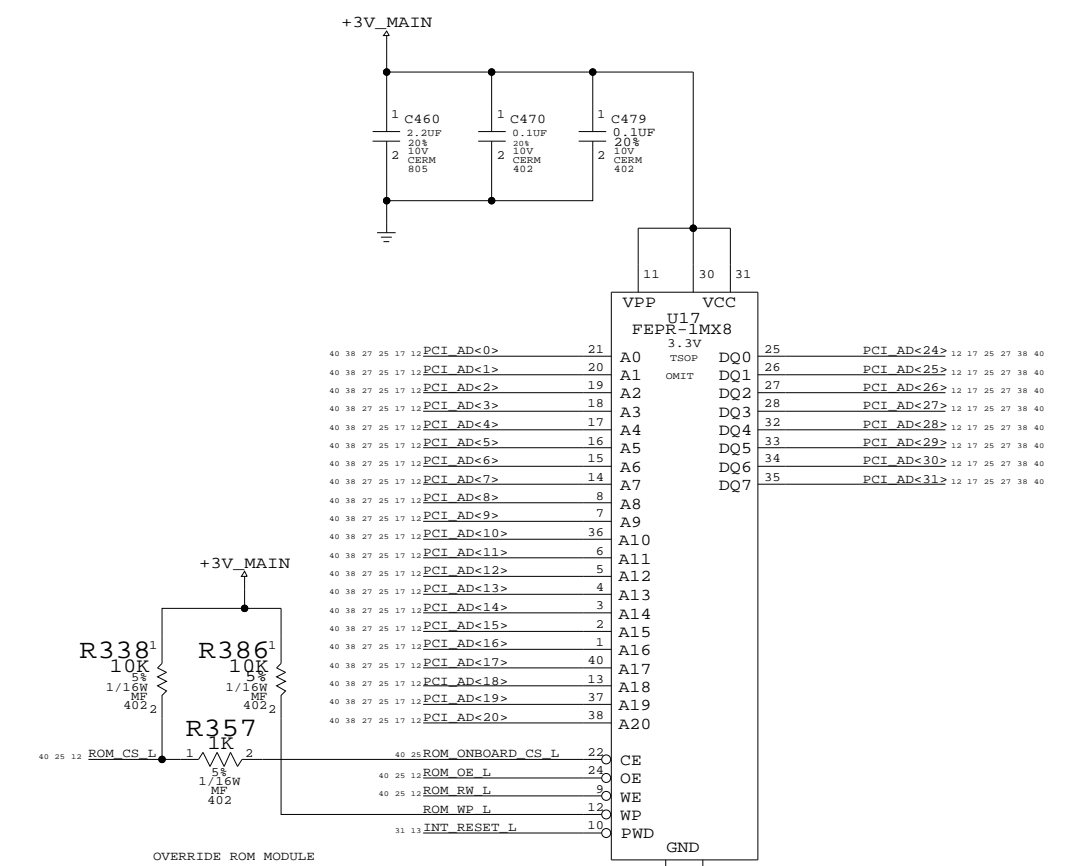
CKE

ADDR

CNTL BA

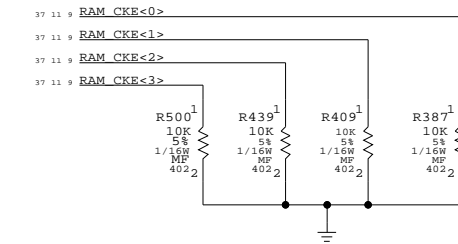


1MB BOOT ROM



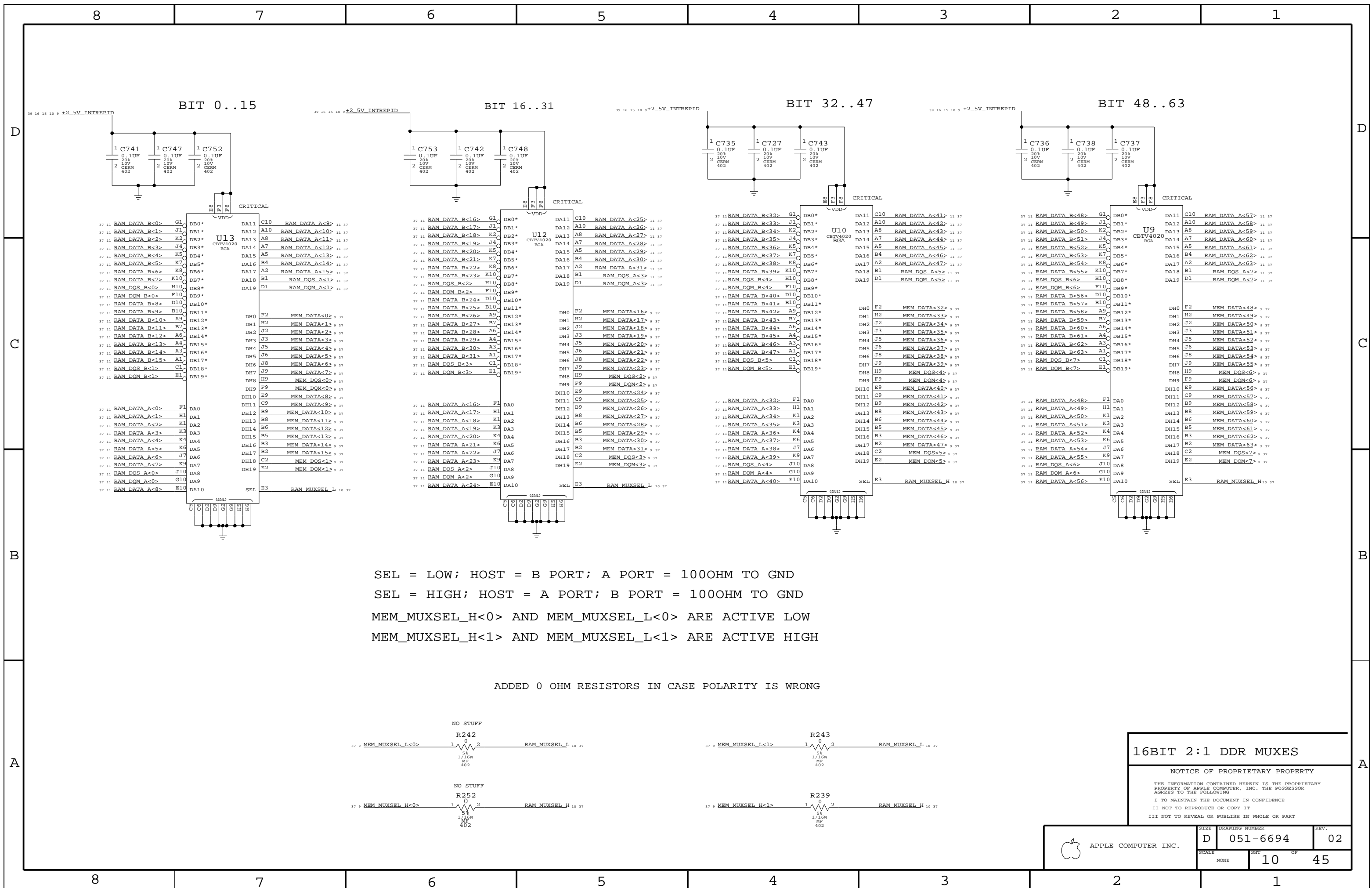
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1556	1	IC,BOOTROM,Q41B	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE CKE STAYS LOW AFTER INTREPID 2.5V I/O SHUTS OFF



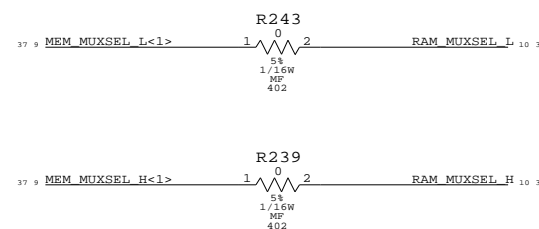
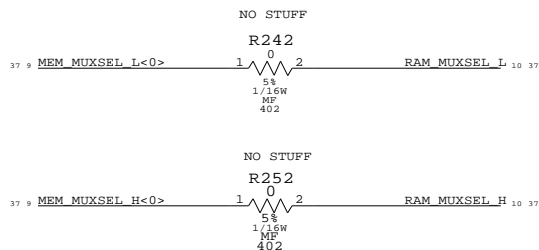
INT - DDR/BOOTROM

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
 SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
 MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
 MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

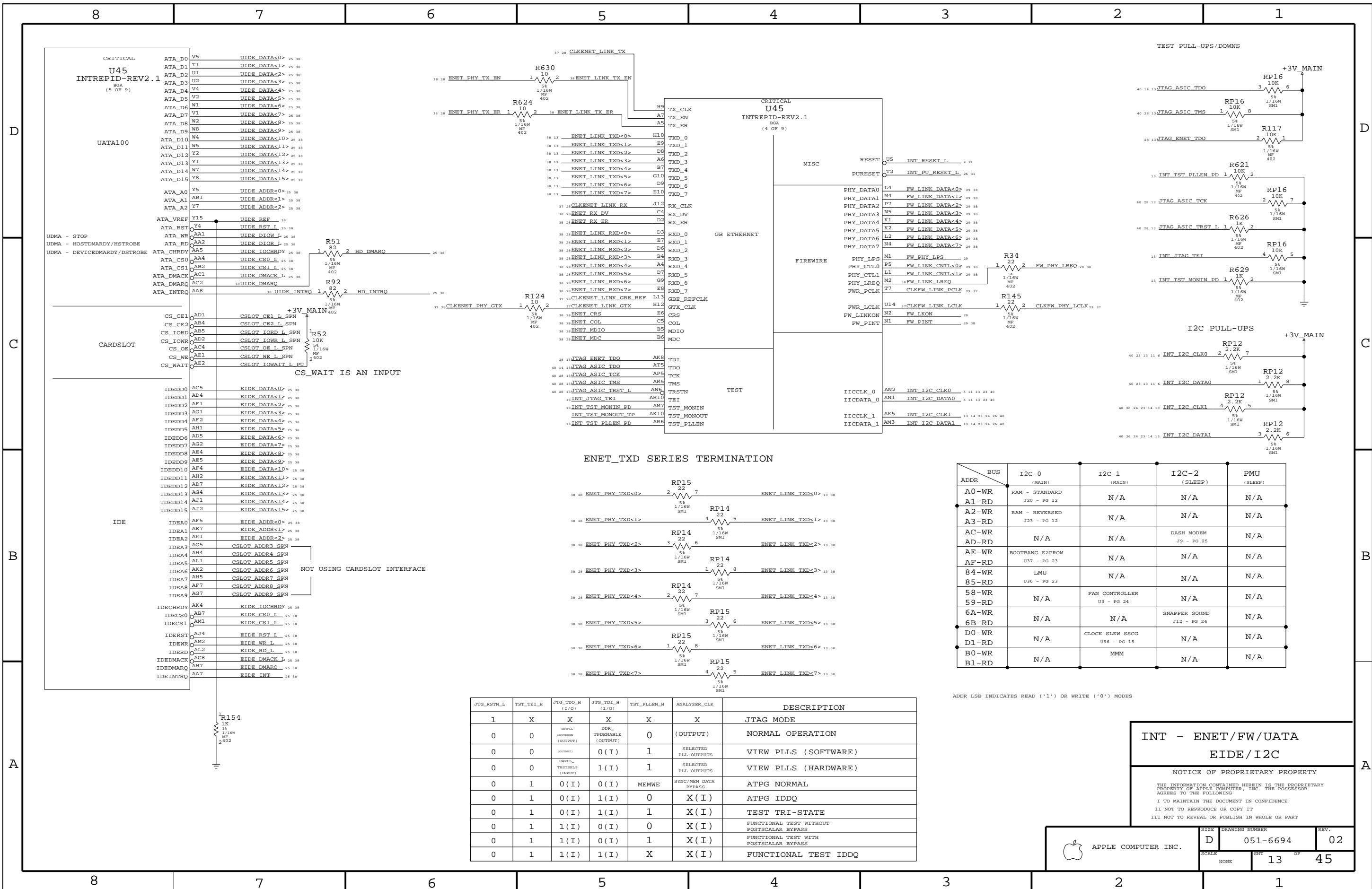
ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG



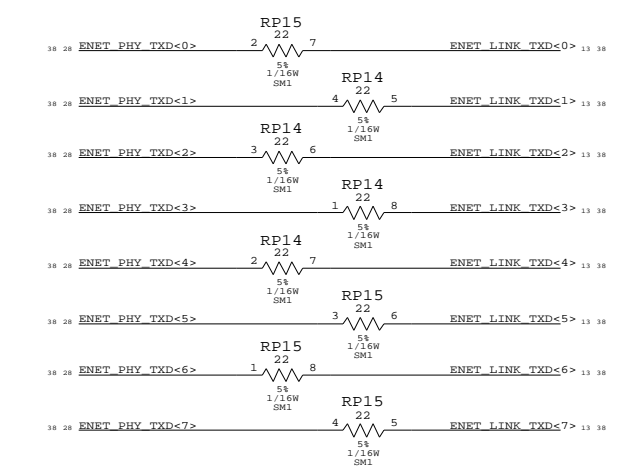
16BIT 2:1 DDR MUXES

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6694	02
SHEET		OF	
10		45	



ENET_TXD SERIES TERMINATION



JTAG_RSTN_L	TST_TDI_H	JTAG_TDO_H (I/O)	JTAG_TDI_H (I/O)	TST_PLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	0	0	0	(OUTPUT)	NORMAL OPERATION
0	0	0	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	0	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

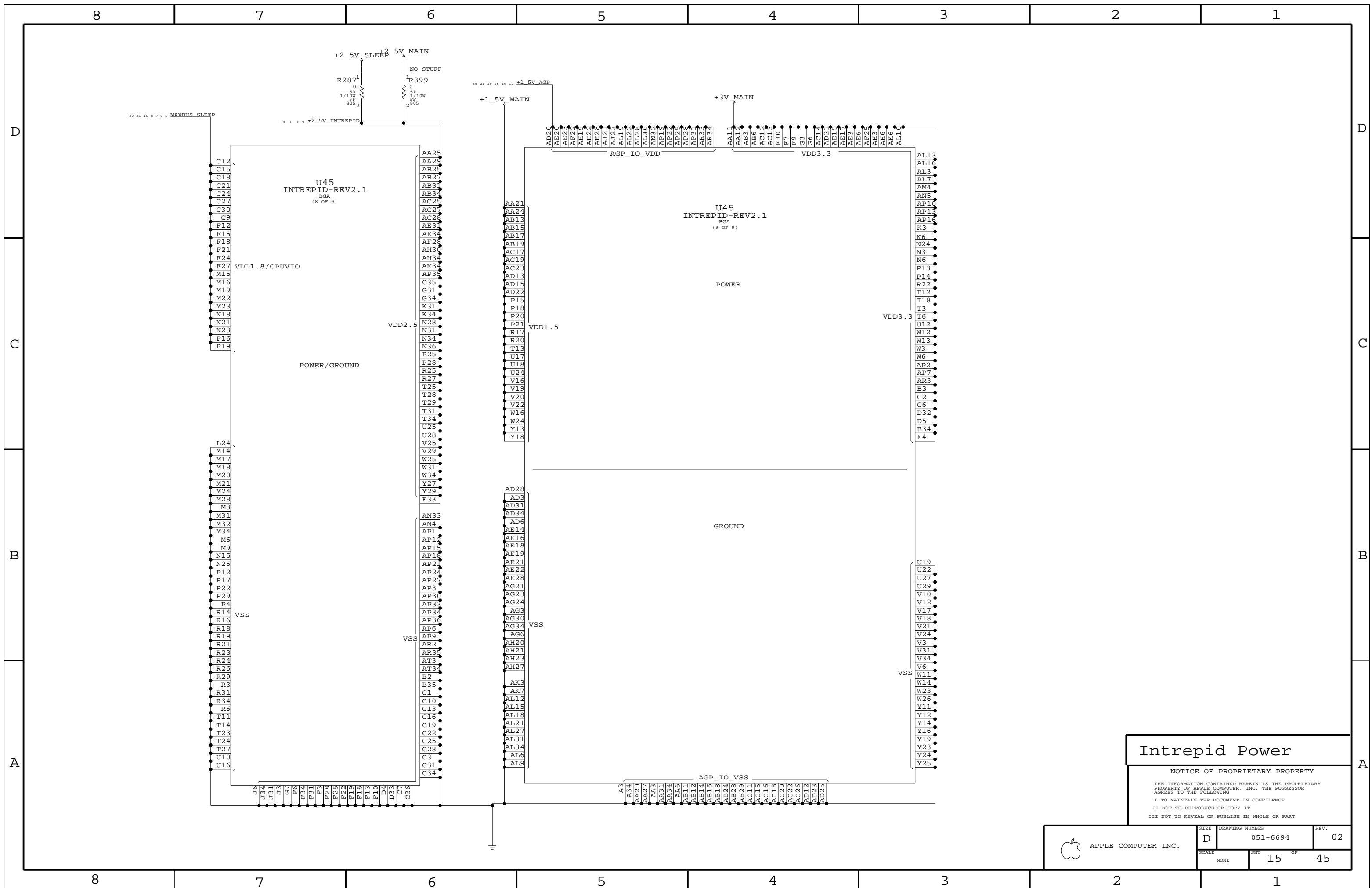
ADDR	BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR		RAM - STANDARD	N/A	N/A	N/A
A1-RD		J20 - PG 12	N/A	N/A	N/A
A2-WR		RAM - REVERSED	N/A	N/A	N/A
A3-RD		J23 - PG 12	N/A	N/A	N/A
AC-WR		N/A	N/A	DASH MODEM	N/A
AD-RD		N/A	N/A	J9 - PG 25	N/A
AE-WR		BOOTBANG E2PROM	N/A	N/A	N/A
AF-RD		U37 - PG 23	N/A	N/A	N/A
84-WR		LMU	N/A	N/A	N/A
85-RD		U36 - PG 23	N/A	N/A	N/A
58-WR		N/A	FAN CONTROLLER	N/A	N/A
59-RD		N/A	U3 - PG 24	N/A	N/A
6A-WR		N/A	N/A	SNAPPER SOUND	N/A
6B-RD		N/A	N/A	J12 - PG 24	N/A
D0-WR		N/A	CLOCK SLEW SSCG	N/A	N/A
D1-RD		N/A	U56 - PG 15	N/A	N/A
B0-WR		N/A	MMM	N/A	N/A
B1-RD		N/A	N/A	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA
EIDE/I2C

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

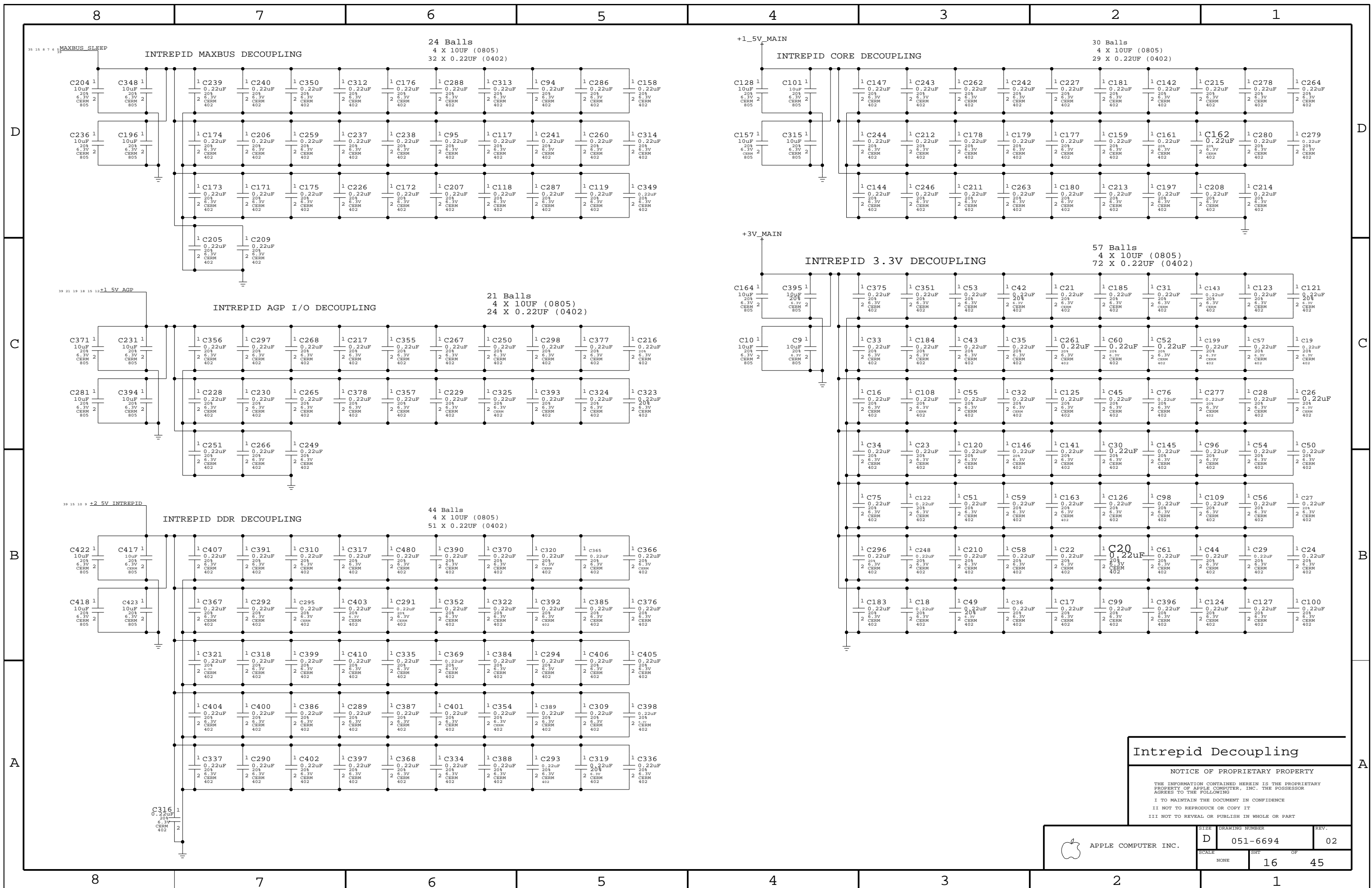
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	SHT	OF	
NONE	13	45	



Intrepid Power

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	SHT		OF
NONE	15		45

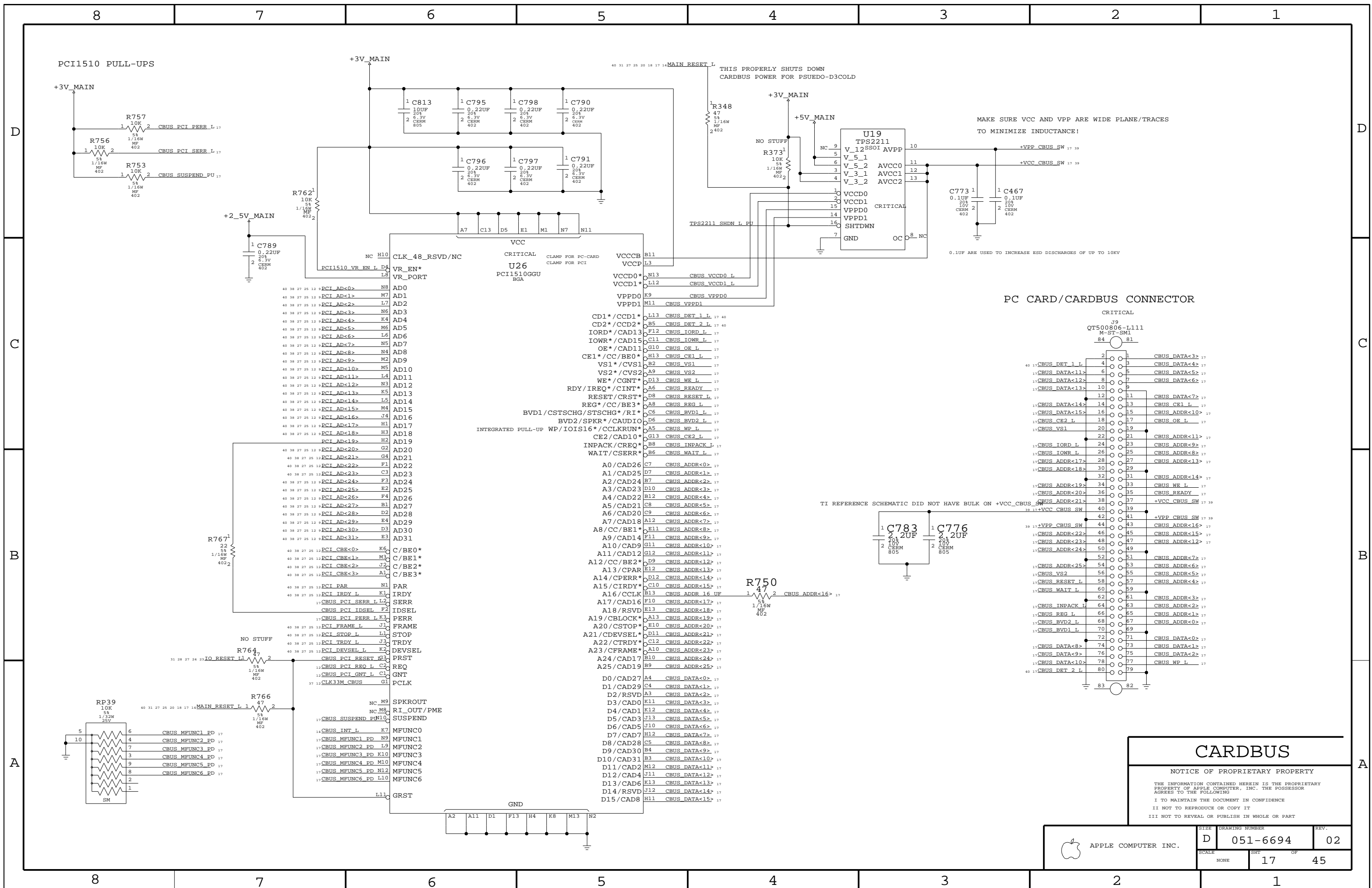


Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE: D DRAWING NUMBER: 051-6694 SCALE: NONE	REV.: 02 SHEET: 16 OF 45
---------------------	--	-----------------------------

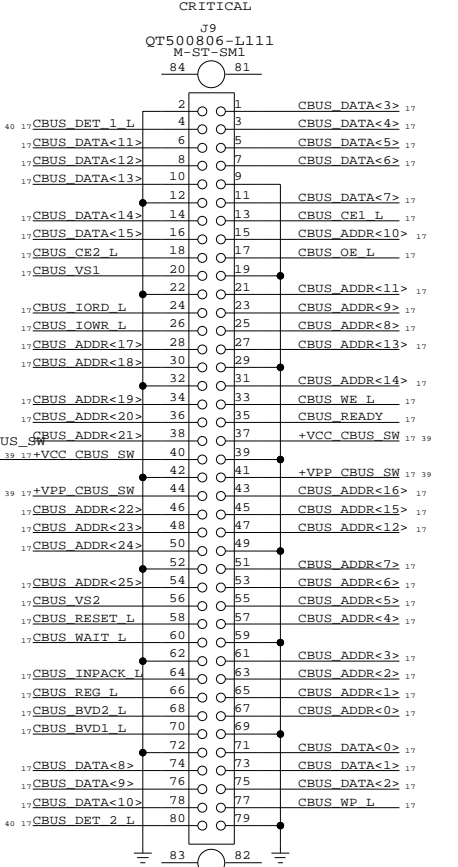


THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSEUDO-D3COLD

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

PC CARD/CARDBUS CONNECTOR



CARDBUS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	NONE	SHT	OF
		17	45

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTRL,667BGA	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHSCTRL,667BGA	U44	CRITICAL	M11_CSP64

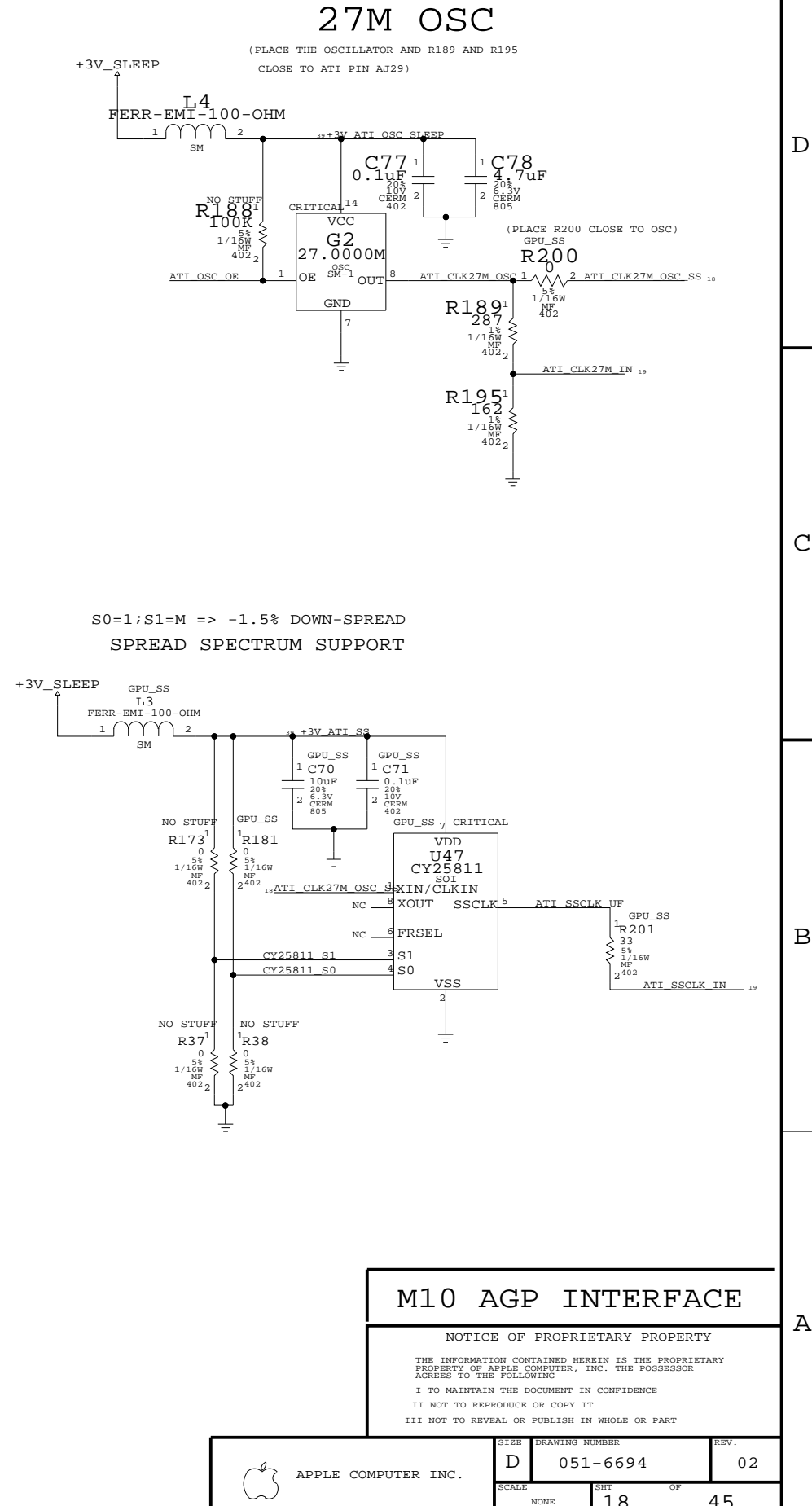
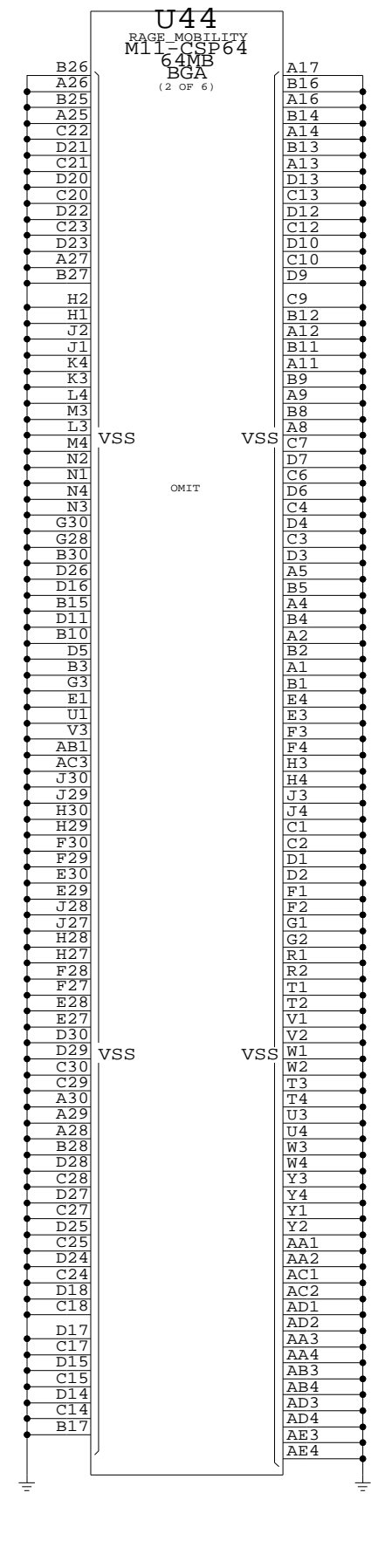
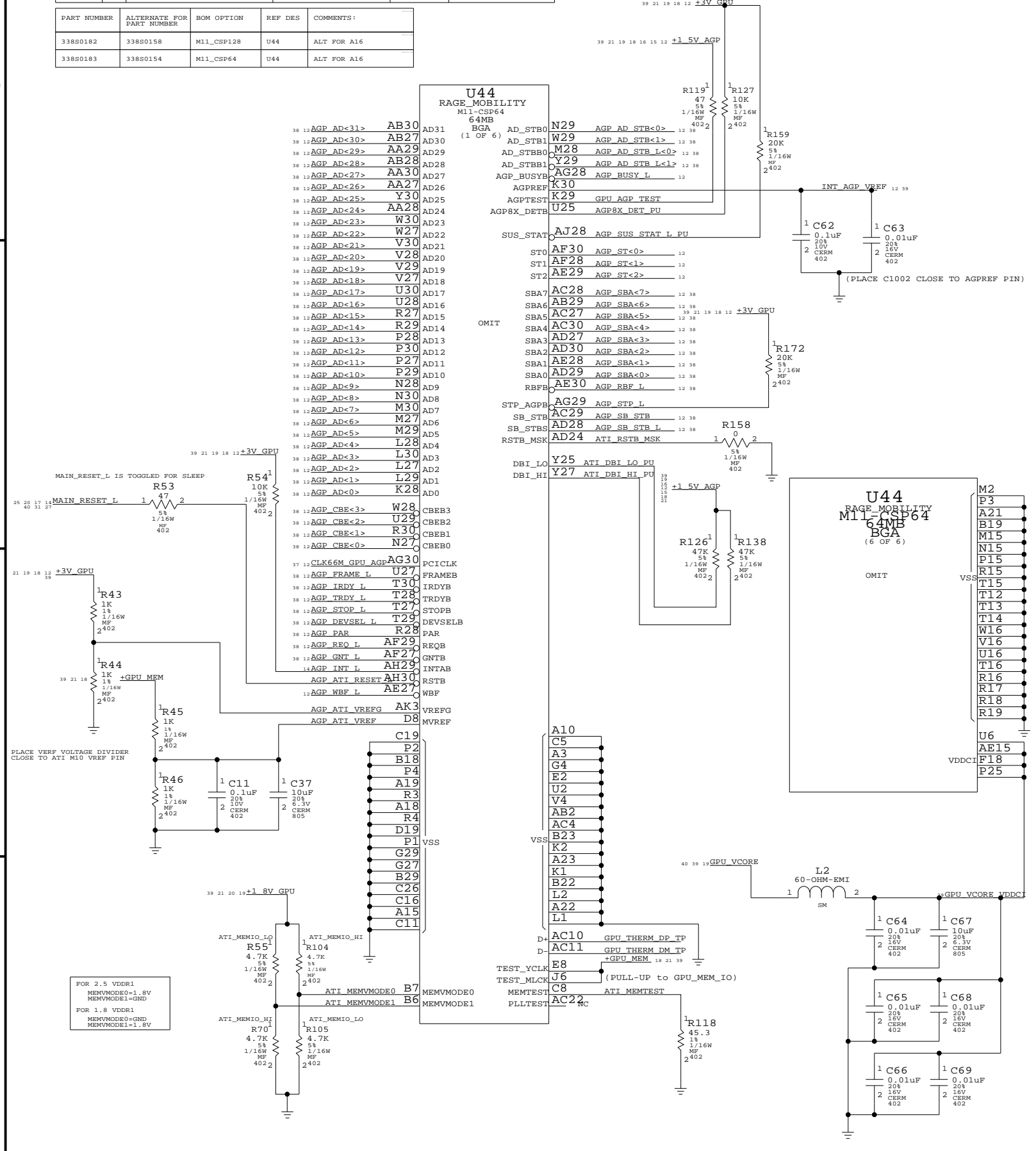
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
338S0182	338S0158	M11_CSP128	U44	ALT FOR A16
338S0183	338S0154	M11_CSP64	U44	ALT FOR A16

D

C

B

A

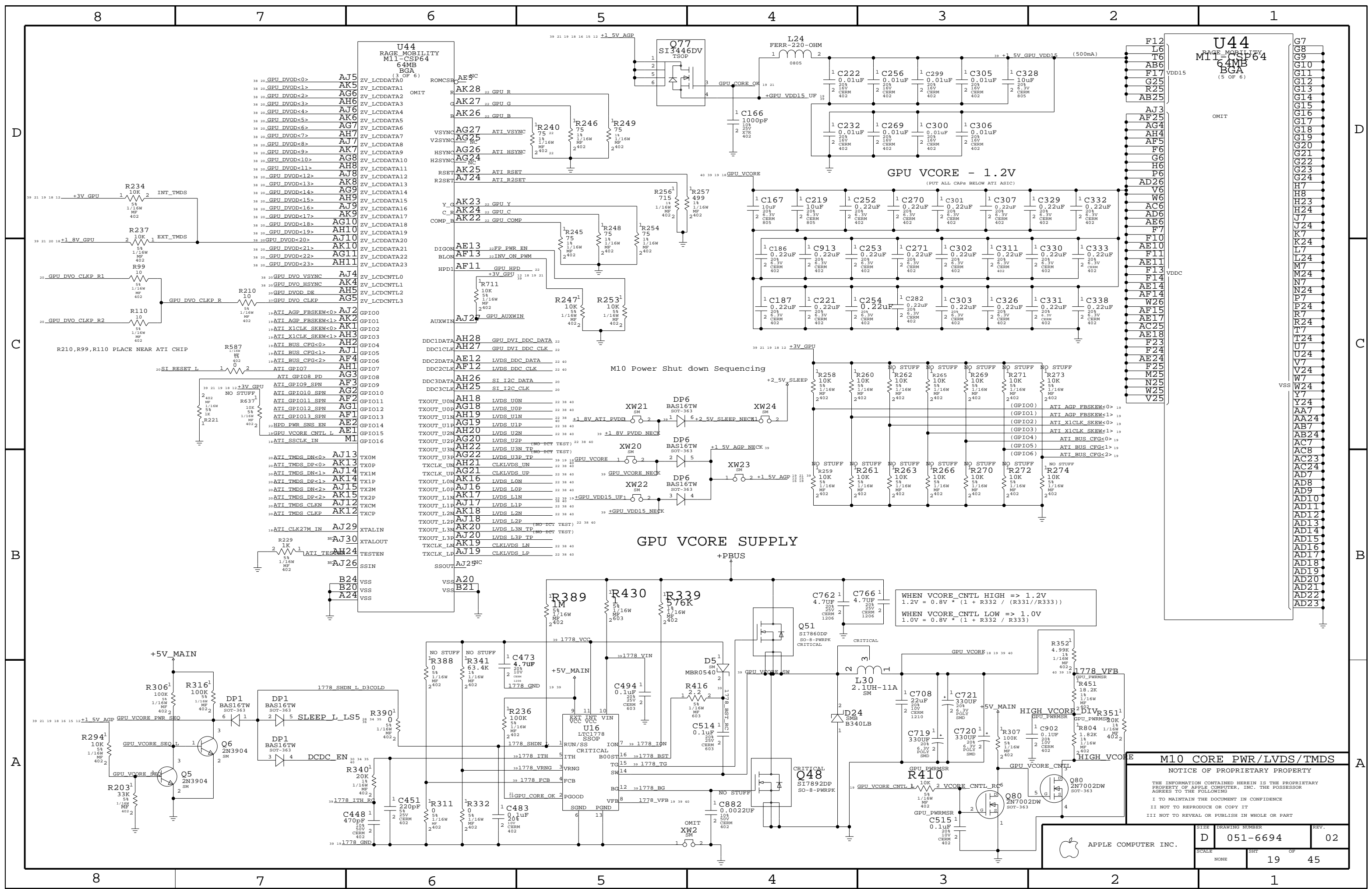


D

C

B

A



U44 RAGE MOBILITY M11-CSP64 64MB BGA (3 OF 6)

38 GPU_DVOD<0>	AJ5	ZV_LCDATA0	ROMCSB<0>	AF5C
38 GPU_DVOD<1>	AK9	ZV_LCDATA1	ROMCSB<1>	AK28
38 GPU_DVOD<2>	AG6	ZV_LCDATA2	OMIT	AK27
38 GPU_DVOD<3>	AH6	ZV_LCDATA3		AK26
38 GPU_DVOD<4>	AJ6	ZV_LCDATA4		AG27
38 GPU_DVOD<5>	AK6	ZV_LCDATA5		AG25
38 GPU_DVOD<6>	AG7	ZV_LCDATA6		AG26
38 GPU_DVOD<7>	AH7	ZV_LCDATA7		AG24
38 GPU_DVOD<8>	AJ7	ZV_LCDATA8		AK25
38 GPU_DVOD<9>	AK7	ZV_LCDATA9		AJ24
38 GPU_DVOD<10>	AG8	ZV_LCDATA10		
38 GPU_DVOD<11>	AH8	ZV_LCDATA11		
38 GPU_DVOD<12>	AJ8	ZV_LCDATA12		
38 GPU_DVOD<13>	AK8	ZV_LCDATA13		
38 GPU_DVOD<14>	AG9	ZV_LCDATA14		
38 GPU_DVOD<15>	AH9	ZV_LCDATA15		
38 GPU_DVOD<16>	AJ9	ZV_LCDATA16		
38 GPU_DVOD<17>	AK9	ZV_LCDATA17		
38 GPU_DVOD<18>	AG10	ZV_LCDATA18		
38 GPU_DVOD<19>	AH10	ZV_LCDATA19		
38 GPU_DVOD<20>	AJ10	ZV_LCDATA20		
38 GPU_DVOD<21>	AK10	ZV_LCDATA21		
38 GPU_DVOD<22>	AG11	ZV_LCDATA22		
38 GPU_DVOD<23>	AH11	ZV_LCDATA23		
38 GPU_DVO_VSYNC	AJ4	ZV_LDCNTL0	DDC1DATA	AH28
38 GPU_DVO_HSYNC	AK4	ZV_LDCNTL1	DDC1CLK	AH27
38 GPU_DVO_DE	AH5	ZV_LDCNTL2	DDC2DATA	AE12
38 GPU_DVO_CLKP	AG5	ZV_LDCNTL3	DDC2CLK	AF12
38 ATI_AGP_FBSKEW<0>	AJ2	GPIO0	DDC3DATA	AH26
38 ATI_AGP_FBSKEW<1>	AK2	GPIO1	DDC3CLK	AH25
38 ATI_X1CLK_SKEW<0>	AK1	GPIO2	TXOUT_U0<0>	AH18
38 ATI_X1CLK_SKEW<1>	AH3	GPIO3	TXOUT_U0<1>	AG18
38 ATI_BUS_CFG<0>	AH2	GPIO4	TXOUT_U1<0>	AH19
38 ATI_BUS_CFG<1>	AJ1	GPIO5	TXOUT_U1<1>	AG19
38 ATI_BUS_CFG<2>	AF4	GPIO6	TXOUT_U2<0>	AH20
38 ATI_GPI0<0>	AH1	GPIO7	TXOUT_U2<1>	AG20
38 ATI_GPI0<1>	AG3	GPIO8	TXOUT_U3<0>	AH22
38 ATI_GPI0<2>	AF3	GPIO9	TXOUT_U3<1>	AG22
38 ATI_GPI0<3>	AG2	GPIO10	TXCLK_UN	AH21
38 ATI_GPI0<4>	AF2	GPIO11	TXCLK_UP	AG21
38 ATI_GPI0<5>	AG1	GPIO12	TXOUT_L0N	AK16
38 ATI_GPI0<6>	AF1	GPIO13	TXOUT_L0P	AJ16
38 ATI_GPI0<7>	AE2	GPIO14	TXOUT_L1N	AK17
38 ATI_GPI0<8>	AE1	GPIO15	TXOUT_L1P	AJ17
38 ATI_GPI0<9>	AE1	GPIO16	TXOUT_L2N	AK18
38 ATI_GPI0<10>	AE1	GPIO16	TXOUT_L2P	AJ18
38 ATI_GPI0<11>	AE1	GPIO16	TXOUT_L3N	AK20
38 ATI_GPI0<12>	AE1	GPIO16	TXOUT_L3P	AJ20
38 ATI_GPI0<13>	AE1	GPIO16	TXCLK_LN	AK19
38 ATI_GPI0<14>	AE1	GPIO16	TXCLK_LP	AJ19
38 ATI_GPI0<15>	AE1	GPIO16	SSOUT	AJ25C
38 ATI_GPI0<16>	AE1	GPIO16	SSIN	A20
38 ATI_GPI0<17>	AE1	GPIO16	SSIN	B21
38 ATI_GPI0<18>	AE1	GPIO16	SSIN	B24
38 ATI_GPI0<19>	AE1	GPIO16	SSIN	B20
38 ATI_GPI0<20>	AE1	GPIO16	SSIN	A24
38 ATI_GPI0<21>	AE1	GPIO16	SSIN	
38 ATI_GPI0<22>	AE1	GPIO16	SSIN	
38 ATI_GPI0<23>	AE1	GPIO16	SSIN	
38 ATI_GPI0<24>	AE1	GPIO16	SSIN	
38 ATI_GPI0<25>	AE1	GPIO16	SSIN	
38 ATI_GPI0<26>	AE1	GPIO16	SSIN	
38 ATI_GPI0<27>	AE1	GPIO16	SSIN	
38 ATI_GPI0<28>	AE1	GPIO16	SSIN	
38 ATI_GPI0<29>	AE1	GPIO16	SSIN	
38 ATI_GPI0<30>	AE1	GPIO16	SSIN	
38 ATI_GPI0<31>	AE1	GPIO16	SSIN	
38 ATI_GPI0<32>	AE1	GPIO16	SSIN	
38 ATI_GPI0<33>	AE1	GPIO16	SSIN	
38 ATI_GPI0<34>	AE1	GPIO16	SSIN	
38 ATI_GPI0<35>	AE1	GPIO16	SSIN	
38 ATI_GPI0<36>	AE1	GPIO16	SSIN	
38 ATI_GPI0<37>	AE1	GPIO16	SSIN	
38 ATI_GPI0<38>	AE1	GPIO16	SSIN	
38 ATI_GPI0<39>	AE1	GPIO16	SSIN	
38 ATI_GPI0<40>	AE1	GPIO16	SSIN	
38 ATI_GPI0<41>	AE1	GPIO16	SSIN	
38 ATI_GPI0<42>	AE1	GPIO16	SSIN	
38 ATI_GPI0<43>	AE1	GPIO16	SSIN	
38 ATI_GPI0<44>	AE1	GPIO16	SSIN	
38 ATI_GPI0<45>	AE1	GPIO16	SSIN	
38 ATI_GPI0<46>	AE1	GPIO16	SSIN	
38 ATI_GPI0<47>	AE1	GPIO16	SSIN	
38 ATI_GPI0<48>	AE1	GPIO16	SSIN	
38 ATI_GPI0<49>	AE1	GPIO16	SSIN	
38 ATI_GPI0<50>	AE1	GPIO16	SSIN	
38 ATI_GPI0<51>	AE1	GPIO16	SSIN	
38 ATI_GPI0<52>	AE1	GPIO16	SSIN	
38 ATI_GPI0<53>	AE1	GPIO16	SSIN	
38 ATI_GPI0<54>	AE1	GPIO16	SSIN	
38 ATI_GPI0<55>	AE1	GPIO16	SSIN	
38 ATI_GPI0<56>	AE1	GPIO16	SSIN	
38 ATI_GPI0<57>	AE1	GPIO16	SSIN	
38 ATI_GPI0<58>	AE1	GPIO16	SSIN	
38 ATI_GPI0<59>	AE1	GPIO16	SSIN	
38 ATI_GPI0<60>	AE1	GPIO16	SSIN	
38 ATI_GPI0<61>	AE1	GPIO16	SSIN	
38 ATI_GPI0<62>	AE1	GPIO16	SSIN	
38 ATI_GPI0<63>	AE1	GPIO16	SSIN	
38 ATI_GPI0<64>	AE1	GPIO16	SSIN	
38 ATI_GPI0<65>	AE1	GPIO16	SSIN	
38 ATI_GPI0<66>	AE1	GPIO16	SSIN	
38 ATI_GPI0<67>	AE1	GPIO16	SSIN	
38 ATI_GPI0<68>	AE1	GPIO16	SSIN	
38 ATI_GPI0<69>	AE1	GPIO16	SSIN	
38 ATI_GPI0<70>	AE1	GPIO16	SSIN	
38 ATI_GPI0<71>	AE1	GPIO16	SSIN	
38 ATI_GPI0<72>	AE1	GPIO16	SSIN	
38 ATI_GPI0<73>	AE1	GPIO16	SSIN	
38 ATI_GPI0<74>	AE1	GPIO16	SSIN	
38 ATI_GPI0<75>	AE1	GPIO16	SSIN	
38 ATI_GPI0<76>	AE1	GPIO16	SSIN	
38 ATI_GPI0<77>	AE1	GPIO16	SSIN	
38 ATI_GPI0<78>	AE1	GPIO16	SSIN	
38 ATI_GPI0<79>	AE1	GPIO16	SSIN	
38 ATI_GPI0<80>	AE1	GPIO16	SSIN	
38 ATI_GPI0<81>	AE1	GPIO16	SSIN	
38 ATI_GPI0<82>	AE1	GPIO16	SSIN	
38 ATI_GPI0<83>	AE1	GPIO16	SSIN	
38 ATI_GPI0<84>	AE1	GPIO16	SSIN	
38 ATI_GPI0<85>	AE1	GPIO16	SSIN	
38 ATI_GPI0<86>	AE1	GPIO16	SSIN	
38 ATI_GPI0<87>	AE1	GPIO16	SSIN	
38 ATI_GPI0<88>	AE1	GPIO16	SSIN	
38 ATI_GPI0<89>	AE1	GPIO16	SSIN	
38 ATI_GPI0<90>	AE1	GPIO16	SSIN	
38 ATI_GPI0<91>	AE1	GPIO16	SSIN	
38 ATI_GPI0<92>	AE1	GPIO16	SSIN	
38 ATI_GPI0<93>	AE1	GPIO16	SSIN	
38 ATI_GPI0<94>	AE1	GPIO16	SSIN	
38 ATI_GPI0<95>	AE1	GPIO16	SSIN	
38 ATI_GPI0<96>	AE1	GPIO16	SSIN	
38 ATI_GPI0<97>	AE1	GPIO16	SSIN	
38 ATI_GPI0<98>	AE1	GPIO16	SSIN	
38 ATI_GPI0<99>	AE1	GPIO16	SSIN	
38 ATI_GPI0<100>	AE1	GPIO16	SSIN	

M10 CORE PWR/LVDS/TMDS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

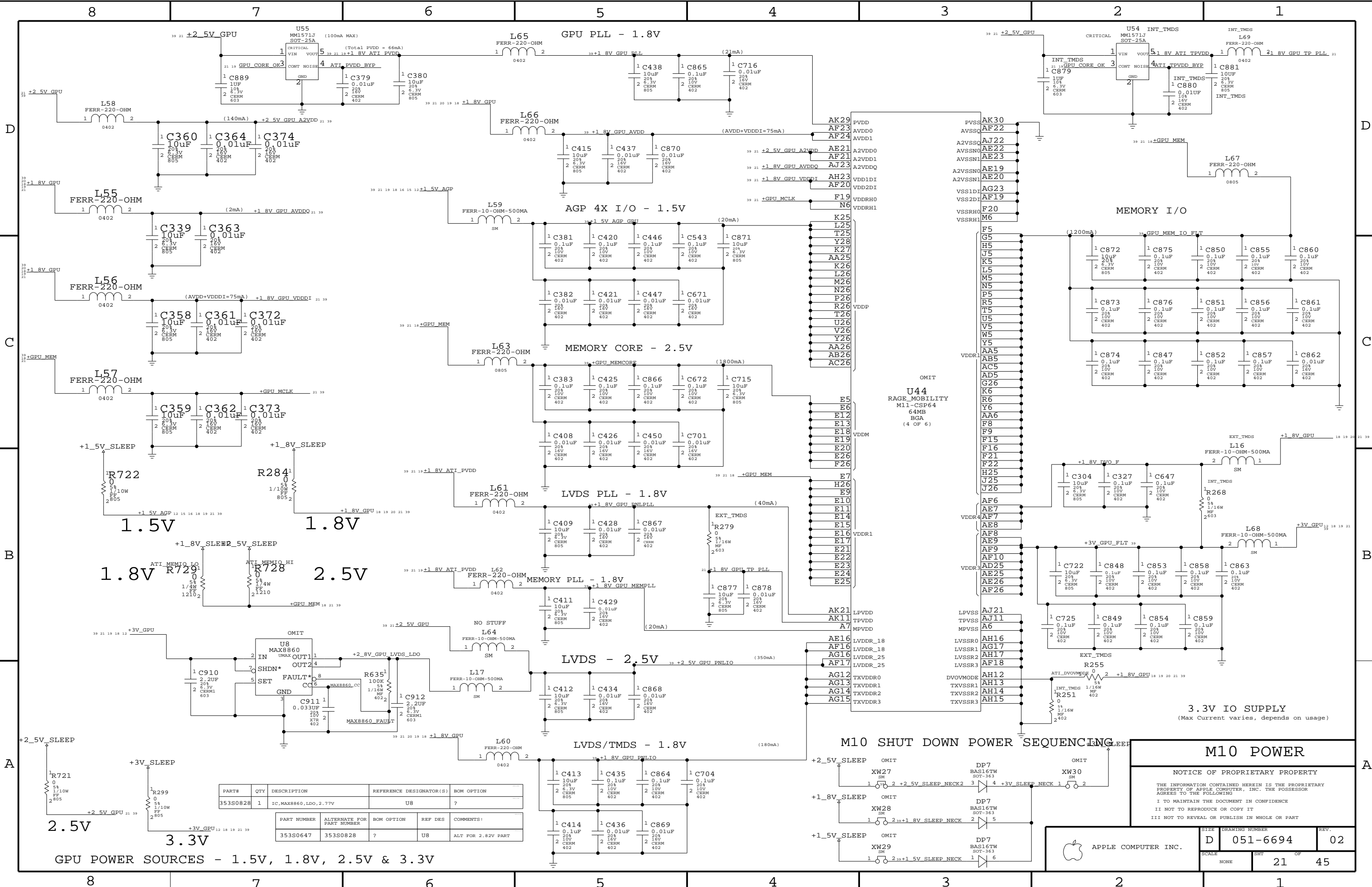
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

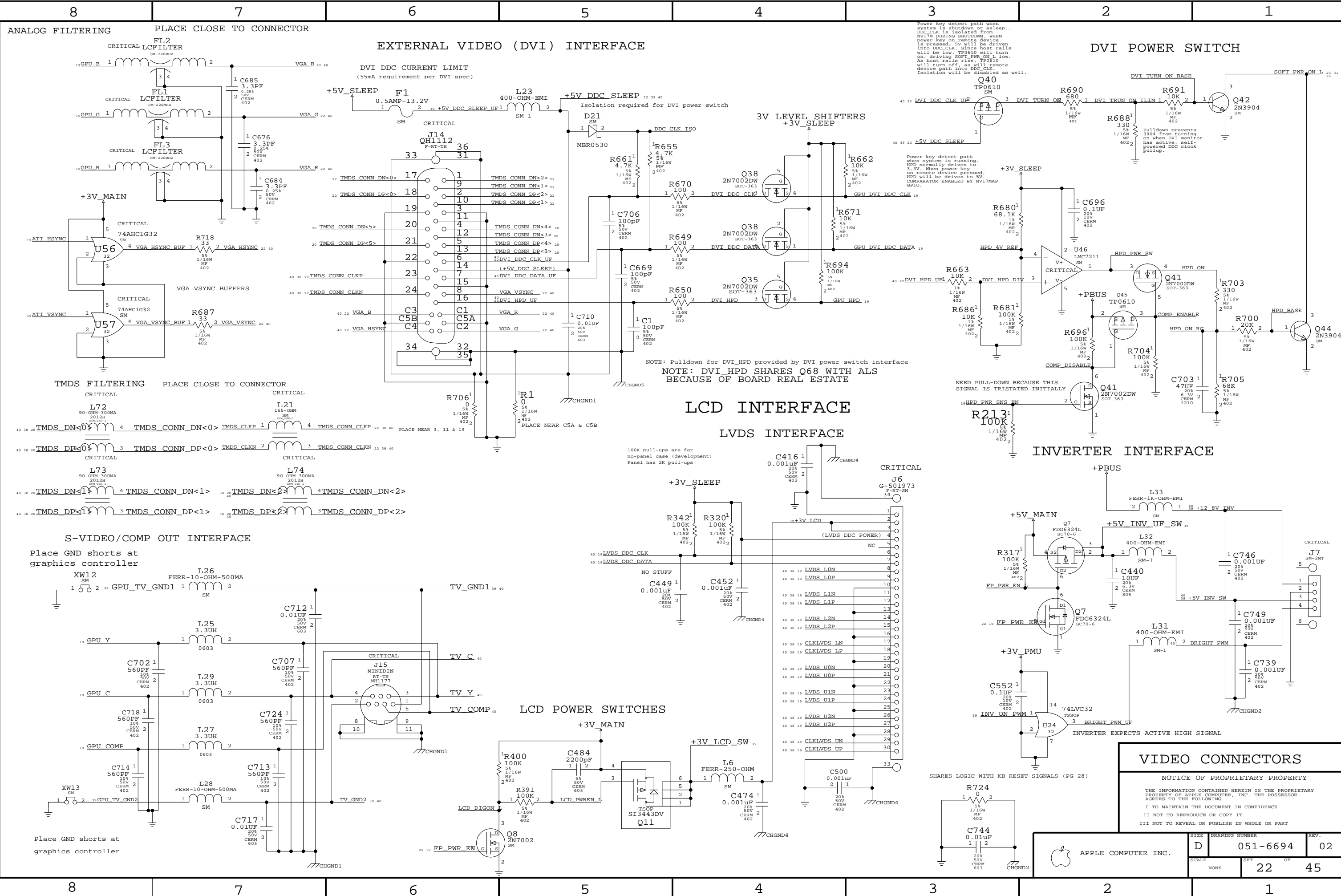
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE	SHEET	OF
NONE	19	45





NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



Power key detect path when system is shutdown or asleep. DDC_CLK is isolated from NV17M during shutdown. When power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GP10.

NOTE: Pull-down for DVI_HPD provided by DVI power switch interface
 NOTE: DVI HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

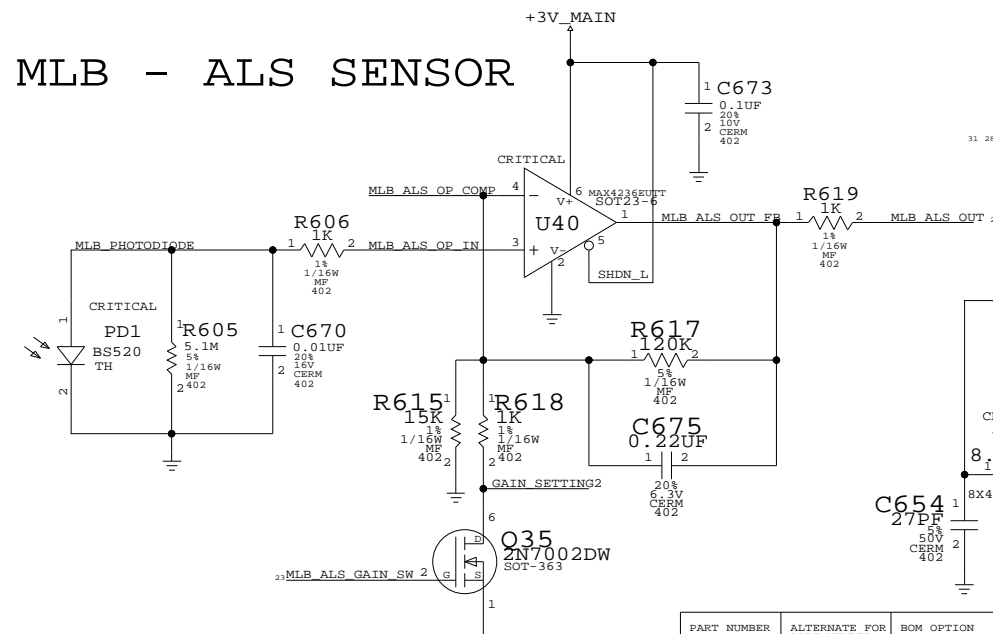
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)

VIDEO CONNECTORS

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE NONE	DRAWING NUMBER D 051-6694	REV. 02
	SCALE NONE	SHEET 22	OF 45

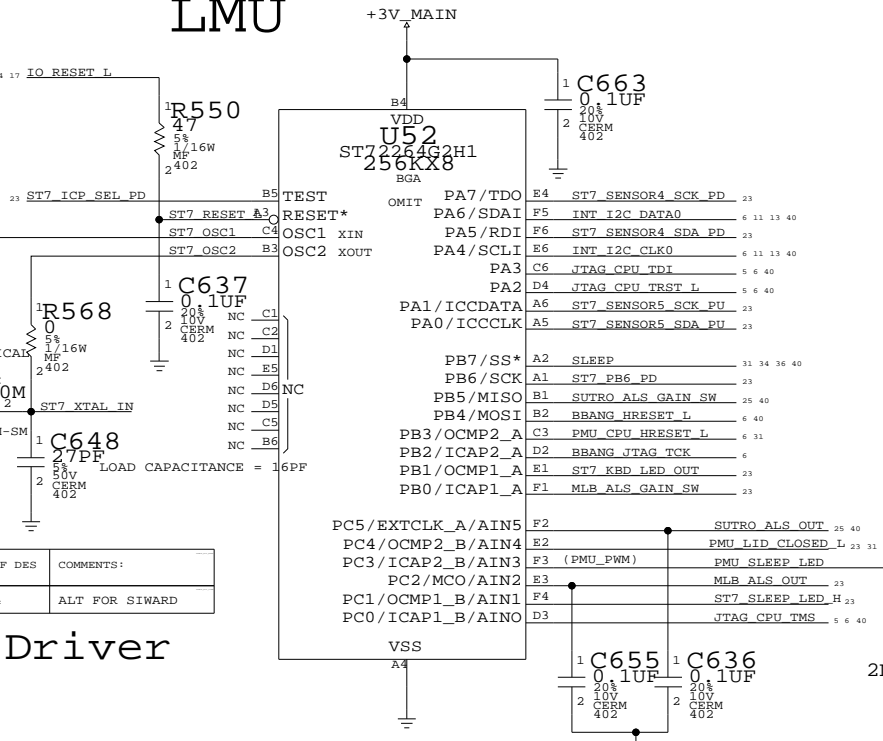
MLB - ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC, LMU, P84	U52	CRITICAL	?

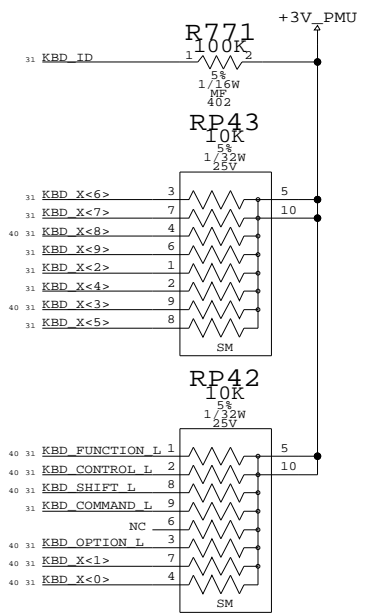
LMU



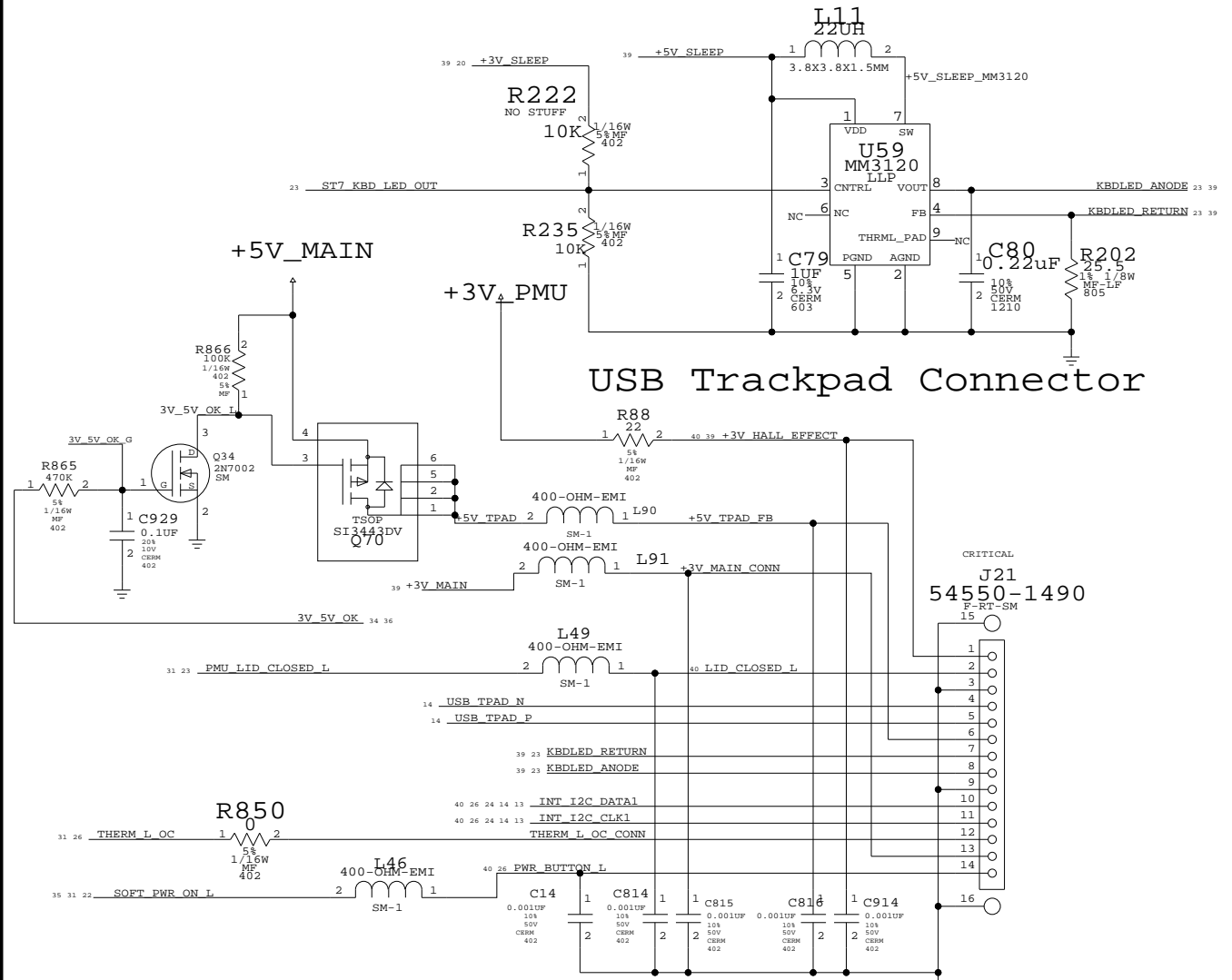
Keyboard LED Driver

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

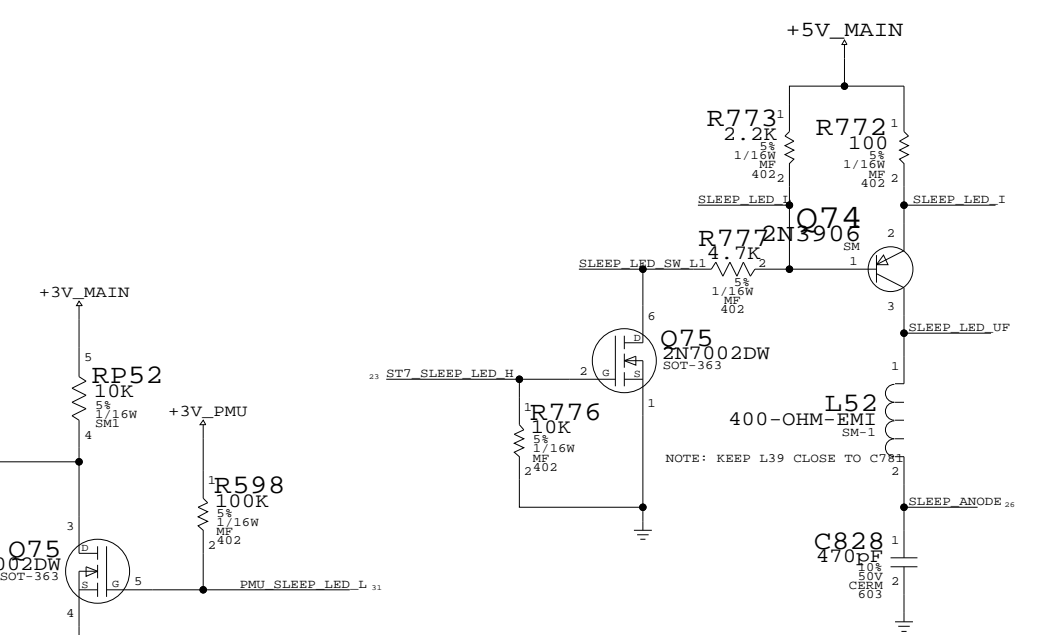
KEYBOARD PULLUPS



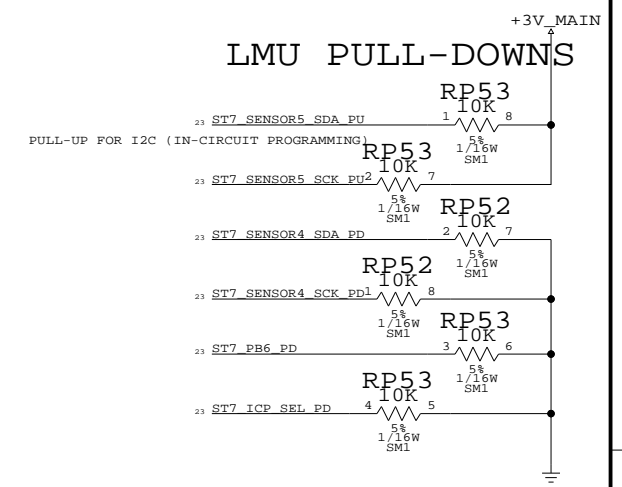
USB Trackpad Connector



SLEEP LED



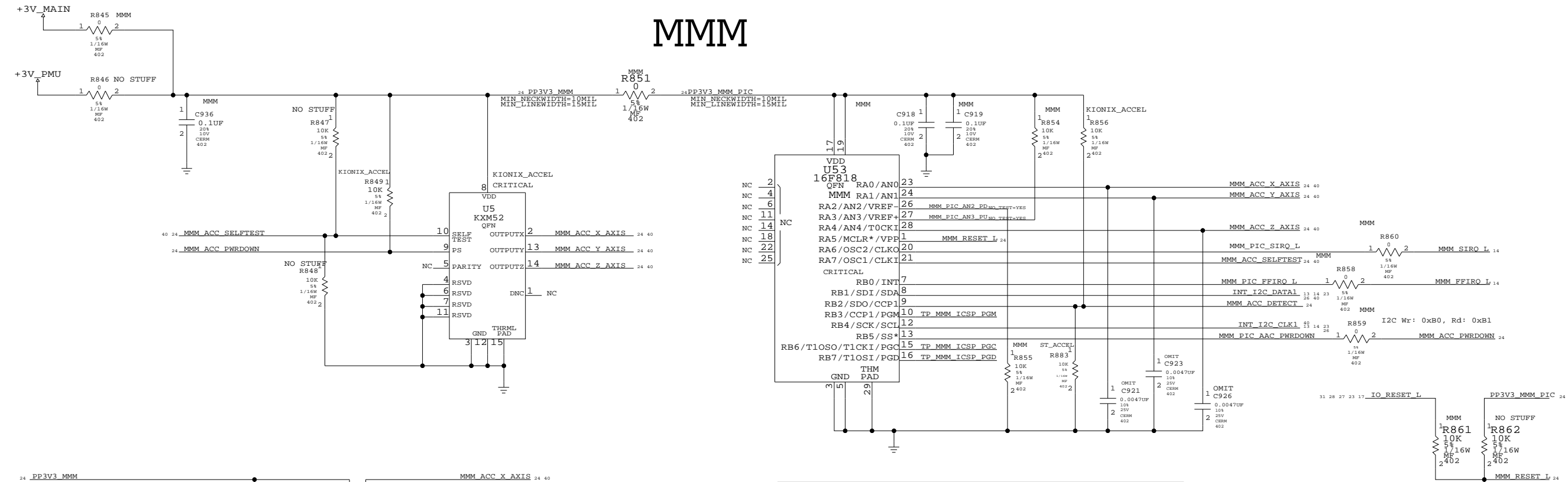
LMU PULL-DOWNS



LMU/BOOTBANGER/SPIDEY

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

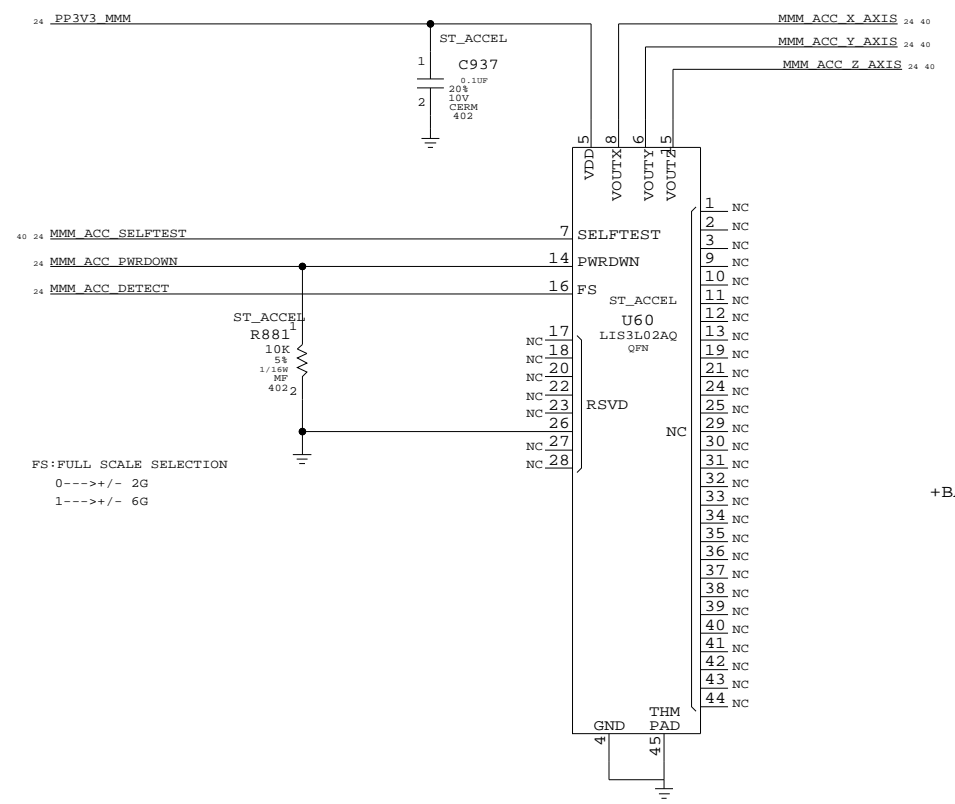
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	?	02
SCALE	NONE	SHT	23 OF 45



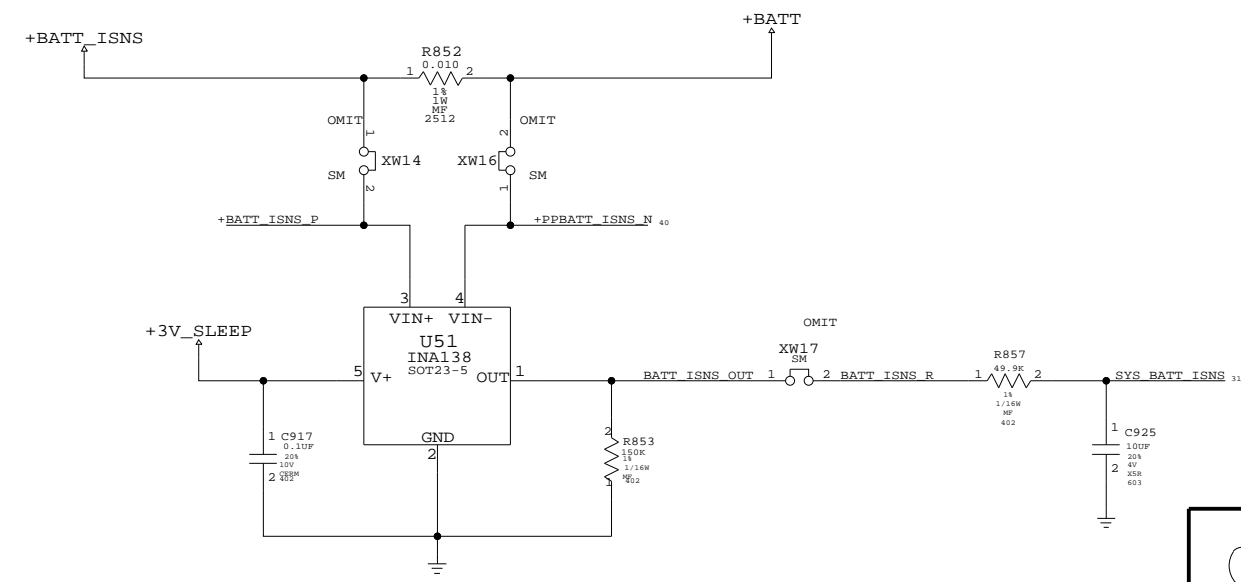
MMM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP CER .0047UF,10%,25V,X7R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

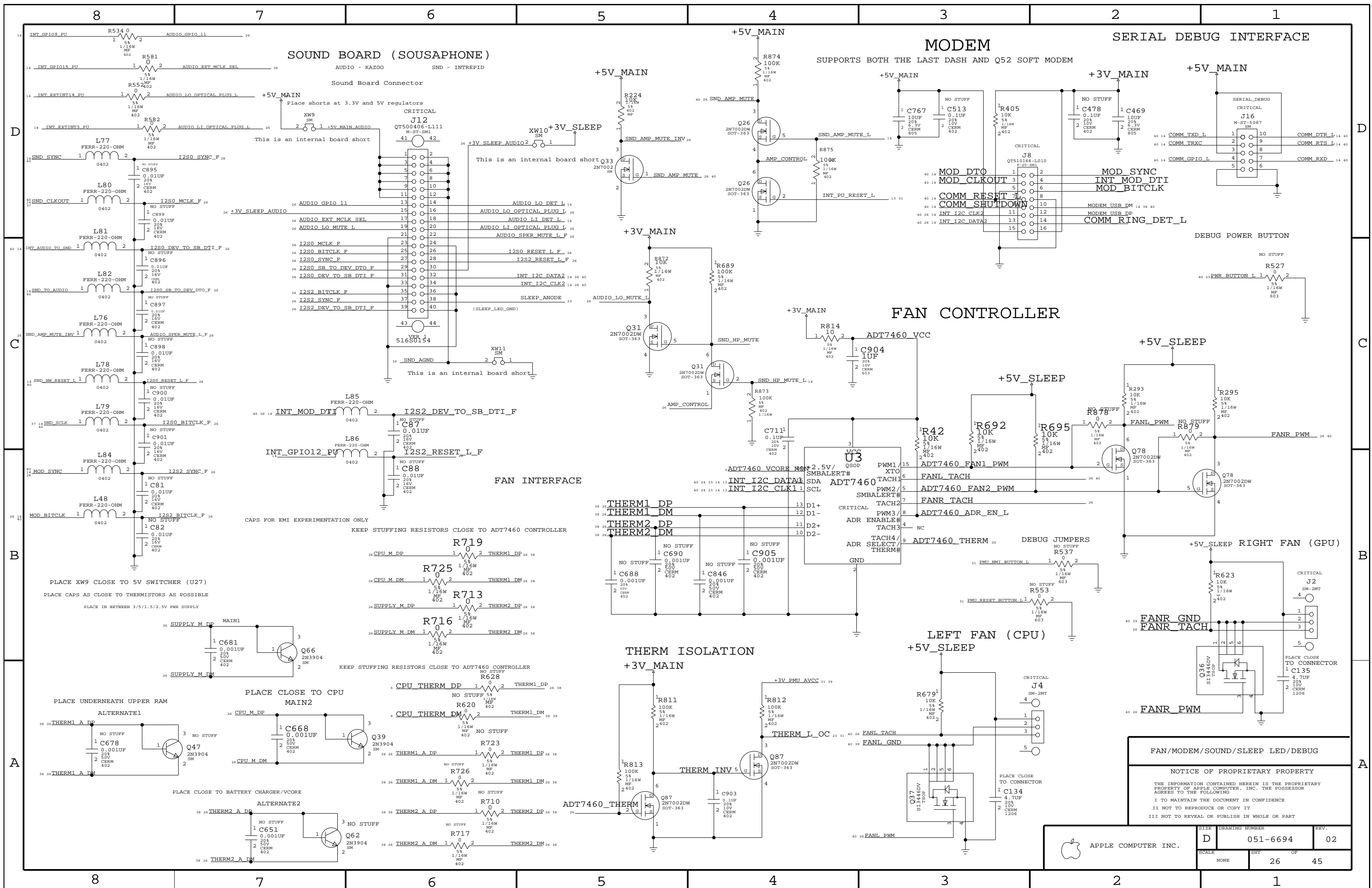


BATTERY CURRENT SENSE



NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	?	02
SCALE	SHT	24	OF 45
NONE			



SOUND BOARD (SOUSAPHONE)

MODEM

SERIAL DEBUG INTERFACE

FAN CONTROLLER

FAN INTERFACE

THERM ISOLATION

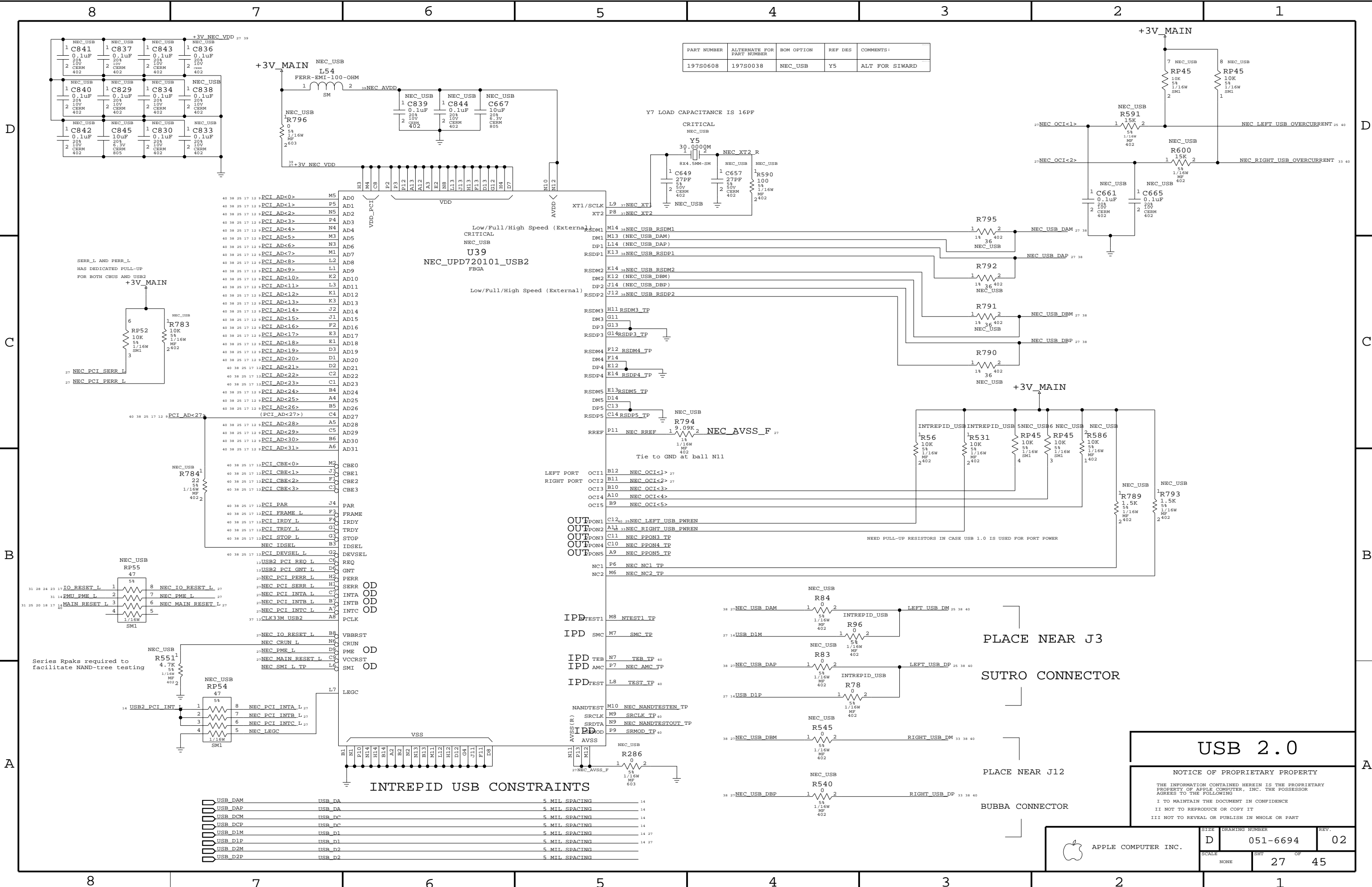
LEFT FAN (CPU)

FAN/MODEM/SOUND/SLEEP LED/DEBUG

NOTICE OF PROPRIETARY PROPERTY

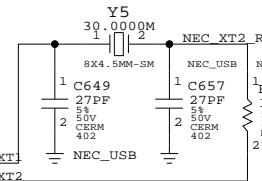
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO MAINTAIN THE DOCUMENT IN CONFIDENCE I I NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	SHEET	OF	REV.
	NONE	26	45	02



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

Y7 LOAD CAPACITANCE IS 16PF
CRITICAL



U39
NEC_UPD720101_USB2
FBGA

Pin	Signal	Component
40	PCI AD<0>	M5
40	PCI AD<1>	P5
40	PCI AD<2>	N5
40	PCI AD<3>	P4
40	PCI AD<4>	N4
40	PCI AD<5>	M3
40	PCI AD<6>	N3
40	PCI AD<7>	M1
40	PCI AD<8>	L2
40	PCI AD<9>	L1
40	PCI AD<10>	K2
40	PCI AD<11>	L3
40	PCI AD<12>	K1
40	PCI AD<13>	K3
40	PCI AD<14>	J2
40	PCI AD<15>	J1
40	PCI AD<16>	F2
40	PCI AD<17>	E3
40	PCI AD<18>	E1
40	PCI AD<19>	D3
40	PCI AD<20>	D1
40	PCI AD<21>	D2
40	PCI AD<22>	C2
40	PCI AD<23>	C1
40	PCI AD<24>	B4
40	PCI AD<25>	A4
40	PCI AD<26>	B5
40	PCI AD<27>	C4
40	PCI AD<28>	A5
40	PCI AD<29>	C5
40	PCI AD<30>	B6
40	PCI AD<31>	A6
40	PCI CBE<0>	M2
40	PCI CBE<1>	J3
40	PCI CBE<2>	F1
40	PCI CBE<3>	C3
40	PCI PAR	J4
40	PCI FRAME L	F3
40	PCI TRDY L	F4
40	PCI TRDY L	G1
40	PCI STOP L	G2
40	PCI IDSEL	B3
40	PCI DEVSEL L	G2
12	USB2 PCI REQ L	C6
12	USB2 PCI GNT L	D6
12	NEC PCI PERR L	H7
12	NEC PCI SERR L	H1
12	NEC PCI INTA L	C7
12	NEC PCI INTB L	B7
12	NEC PCI INTC L	A7
12	CLK33M USB2	A8
27	NEC IO RESET L	B8
27	NEC CRUN L	N6
27	NEC PME L	D9
27	NEC MAIN RESET L	C9
27	NEC SMI L TP	L6
14	USB2 PCI INT	L7
14	NEC PCI INTA L	1
14	NEC PCI INTB L	2
14	NEC PCI INTC L	3
14	NEC LEGC	4

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 27
USB_D1P	USB_D1	5 MIL SPACING	14 27
USB_D2M	USB_D2	5 MIL SPACING	14
USB_D2P	USB_D2	5 MIL SPACING	14

LEFT PORT OC11
RIGHT PORT OC12
OC13
OC14
OC15

OUTP0N1
OUTP0N2
OUTP0N3
OUTP0N4
OUTP0N5

IPD TEST1
IPD SMC
IPD TEB
IPD AMC
IPD TEST

NANDTEST
SRCLK
SRDTA
SRDOD
AVSS(R)
AVSS

INTREPID_USB
LEFT USB_DM
LEFT USB_DP
RIGHT USB_DM
RIGHT USB_DP

USB 2.0

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

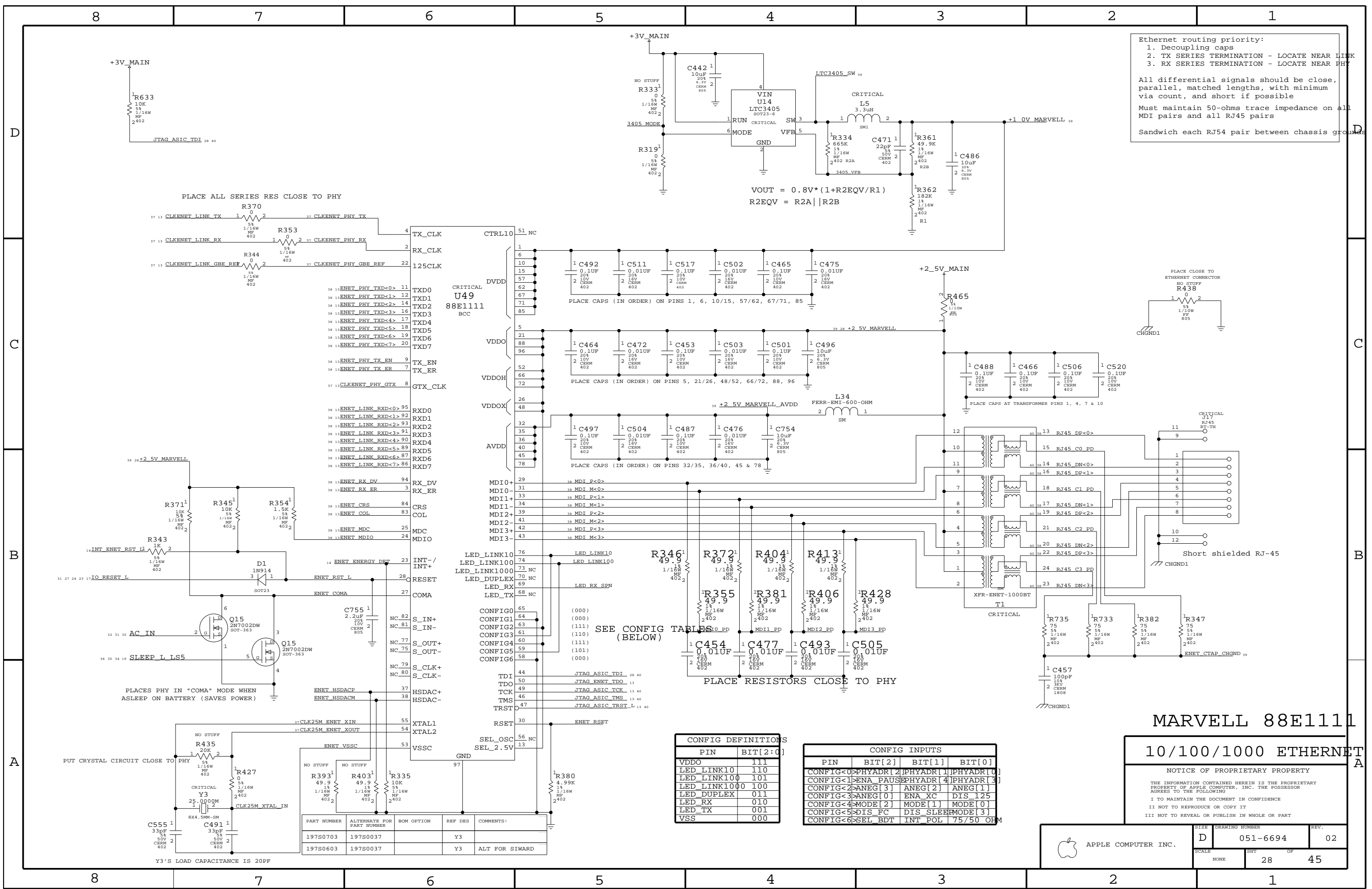
APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	27	45	02

Ethernet routing priority:
 1. Decoupling caps
 2. TX SERIES TERMINATION - LOCATE NEAR LINK
 3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis ground



PLACE ALL SERIES RES CLOSE TO PHY

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

PLACE CLOSE TO ETHERNET CONNECTOR

SEE CONFIG TABLES (BELOW)

PLACE RESISTORS CLOSE TO PHY

MARVELL 88E1111

10/100/1000 ETHERNET

NOTICE OF PROPRIETARY PROPERTY

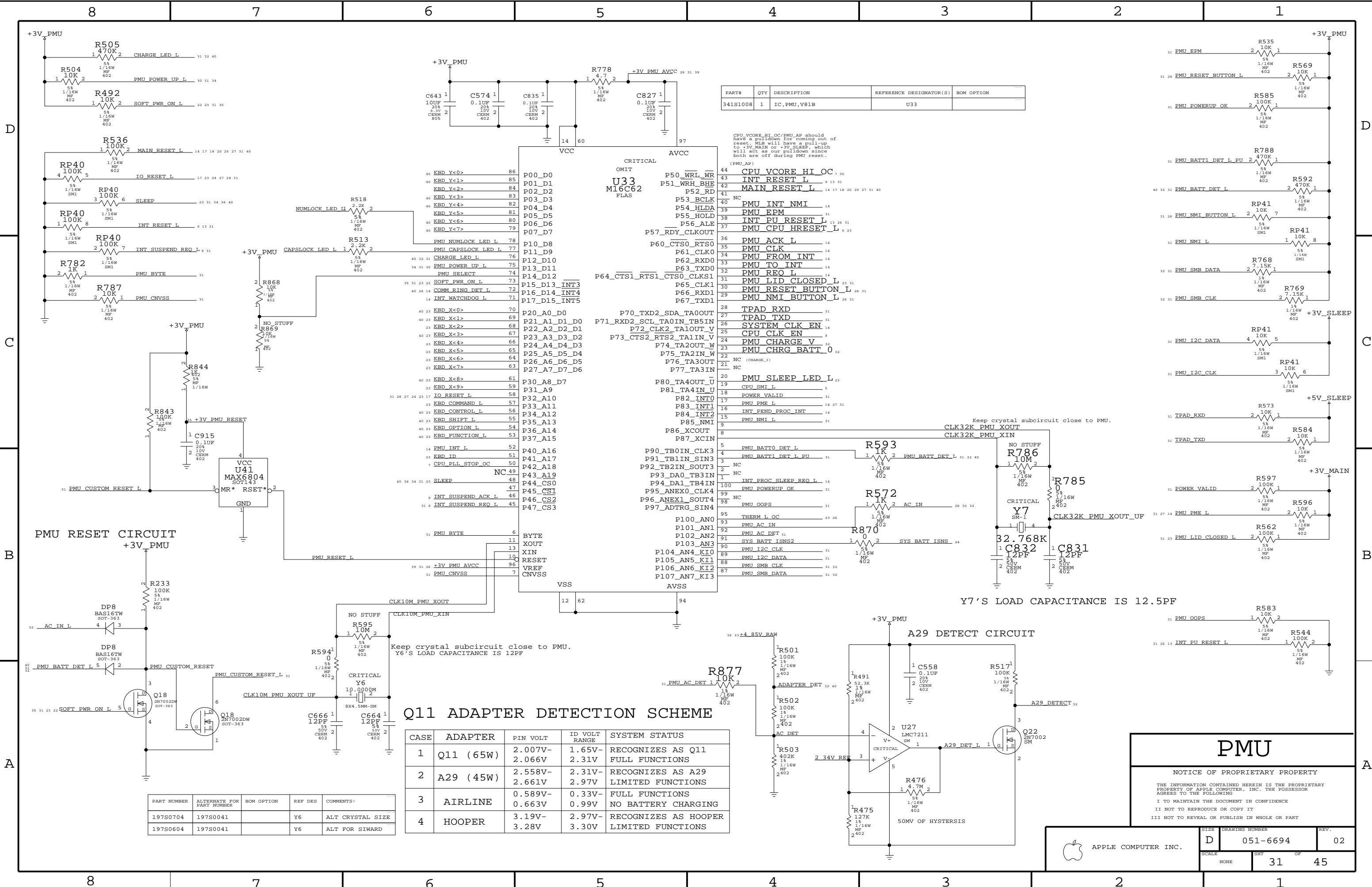
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037		Y3	
197S0603	197S0037		Y3	ALT FOR SIWARD

APPLE COMPUTER INC.	SIZE: D DRAWING NUMBER: 051-6694 SCALE: NONE	REV.: 02 SHEET: 28 OF 45
---------------------	--	-----------------------------



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

CPU_VCORE_HI_OC/PMU_AP should have a pull-down for coming out of reset. MIB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pull-down since both are off during PMU reset.

VCC		CRITICAL		AVCC		
40	KBD_Y<0>	86	P00_D0	44	CPU_VCORE_HI_OC	
40	KBD_Y<1>	85	P01_D1	43	INT_RESET_L	
40	KBD_Y<2>	84	P02_D2	42	MAIN_RESET_L	
40	KBD_Y<3>	83	P03_D3	41	NC	
40	KBD_Y<4>	82	P04_D4	40	PMU_INT_NMI	
40	KBD_Y<5>	81	P05_D5	39	PMU_EPM	
40	KBD_Y<6>	80	P06_D6	38	INT_PU_RESET_L	
40	KBD_Y<7>	79	P07_D7	37	PMU_CPU_HRESET_L	
40	PMU_NUMLOCK_LED_L	78	P10_D8	36	PMU_ACK_L	
40	PMU_CAPSLOCK_LED_L	77	P11_D9	35	PMU_CLK	
40	CHARGE_LED_L	76	P12_D10	34	PMU_FROM_INT	
34	31	30	P13_D11	33	PMU_TO_INT	
34	31	30	P14_D12	32	PMU_REQ_L	
35	31	23	P15_D13_INT3	31	PMU_LID_CLOSED_L	
40	26	14	P16_D14_INT4	30	PMU_RESET_BUTTON_L	
14	14	72	P17_D15_INT5	29	PMU_NMI_BUTTON_L	
40	KBD_X<0>	70	P20_A0_D0	28	TPAD_RXD	
40	KBD_X<1>	69	P21_A1_D1_D0	27	TPAD_TXD	
40	KBD_X<2>	68	P22_A2_D2_D1	26	SYSTEM_CLK_EN	
40	KBD_X<3>	67	P23_A3_D3_D2	25	CPU_CLK_EN	
40	KBD_X<4>	66	P24_A4_D4_D3	24	PMU_CHARGE_V	
23	KBD_X<5>	65	P25_A5_D5_D4	23	PMU_CHRG_BATT_0	
23	KBD_X<6>	64	P26_A6_D6_D5	22	NC (CHARGE_1)	
23	KBD_X<7>	63	P27_A7_D7_D6	21	NC	
40	KBD_X<8>	61	P30_A8_D7	20	PMU_SLEEP_LED_L	
40	KBD_X<9>	59	P31_A9	19	CPU_SMI_L	
31	28	27	24	23	18	POWER_VALID
40	IO_RESET_L	58	P32_A10	17	PMU_PME_L	
40	KBD_COMMAND_L	57	P33_A11	16	INT_PEND_PROC_INT	
40	KBD_CONTROL_L	56	P34_A12	15	PMU_NMI_L	
40	KBD_SHIFT_L	55	P35_A13	9	NC	
40	KBD_OPTION_L	54	P36_A14	8	NC	
40	KBD_FUNCTION_L	53	P37_A15	5	PMU_BATT0_DET_L	
14	PMU_INT_L	52	P40_A16	4	PMU_BATT1_DET_L_PU	
23	KBD_ID	51	P41_A17	3	NC	
7	CPU_PIL_STOP_OC	50	P42_A18	2	NC	
40	36	34	31	23	1	INT_PROC_SLEEP_REQ_L
40	SLEEP	48	P43_A19	100	PMU_POWERUP_OK	
40	NC	49	P44_A20	99	NC	
40	INT_SUSPEND_ACK_L	46	P45_A21	98	PMU_OOPS	
31	8	8	P46_CS2	95	THERM_L_OC	
31	8	8	P47_CS3	93	PMU_AC_IN	
6	BYTE	11	XOUT	92	PMU_AC_DEPT	
11	XIN	13	RESET	91	SYS_BATT_ISNS2	
10	RESET	10	VREF	90	PMU_I2C_CLK	
96	VREF	96	PMU_I2C_DATA	89	PMU_SMB_CLK	
7	PMU_CNVS	7	PMU_SMB_DATA	88	PMU_SMB_DATA	
12	VSS	62	AVSS	87	PMU_SMB_DATA	

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V-2.066V	1.65V-2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V-2.661V	2.31V-2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V-0.663V	0.33V-0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V-3.28V	2.97V-3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

Y7'S LOAD CAPACITANCE IS 12.5PF

PMU

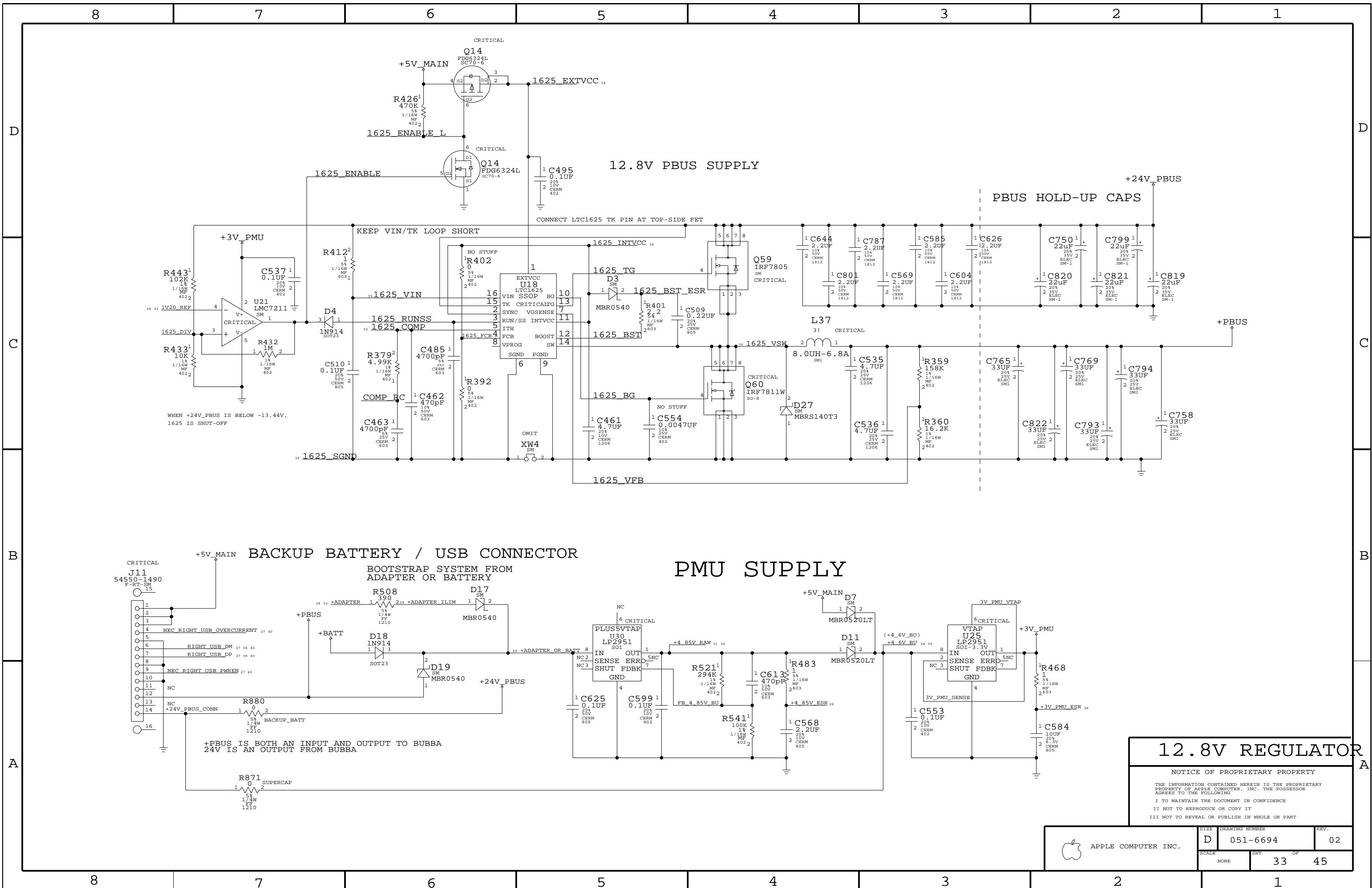
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



12.8V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

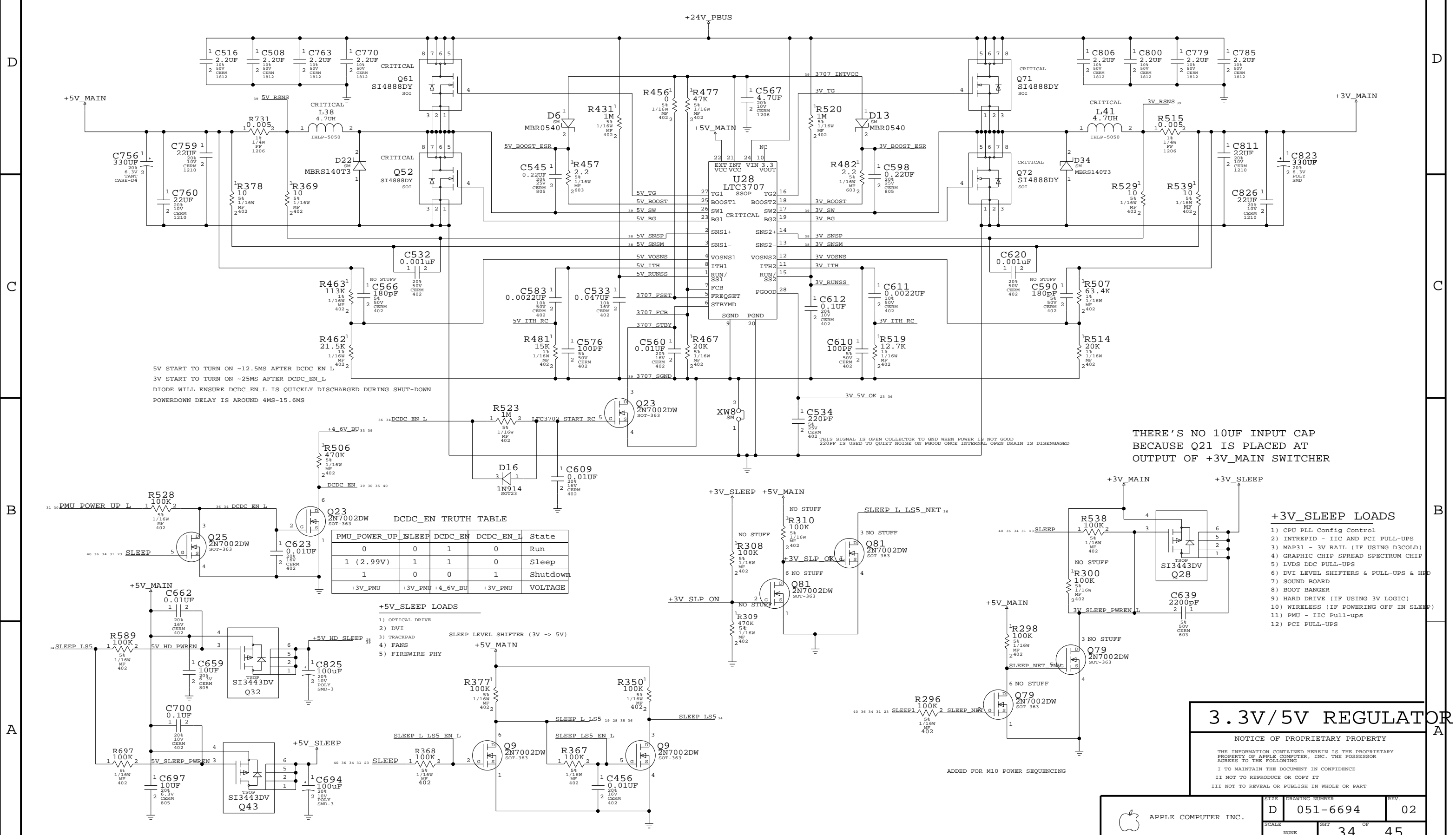
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	NONE		SHT OF
	33		45

3.3V/5V MAIN SUPPLY



THERE'S NO 10UF INPUT CAP BECAUSE Q21 IS PLACED AT OUTPUT OF +3V_MAIN SWITCHER

3.3V/5V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	NONE	SHT	OF
		34	45

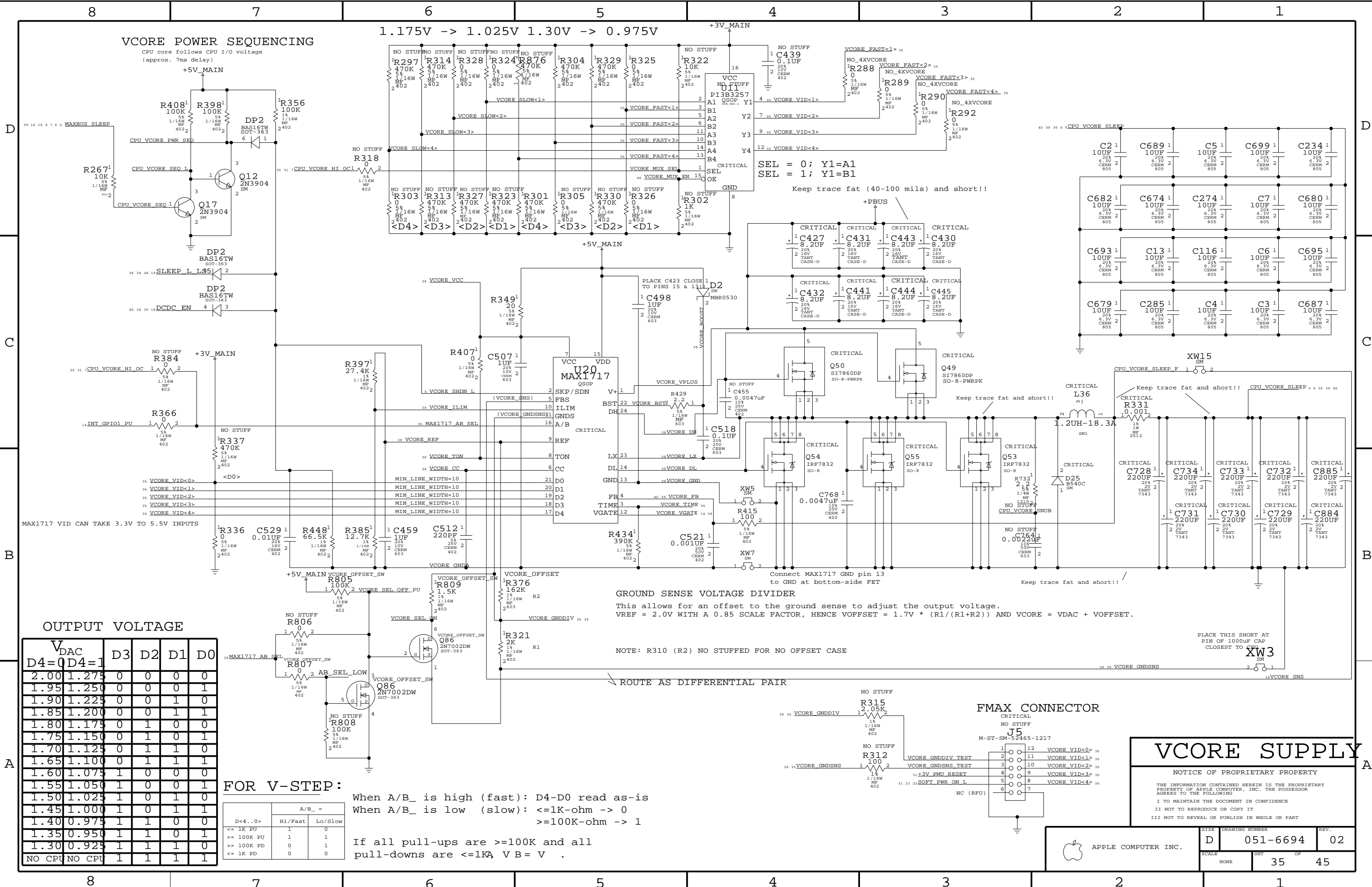
VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 0.975V

D
C
B
A

D
C
B
A



OUTPUT VOLTAGE

V _{DAC}	D3	D2	D1	D0
2.00	1.275	0	0	0
1.95	1.250	0	0	1
1.90	1.225	0	0	1
1.85	1.200	0	1	1
1.80	1.175	0	1	0
1.75	1.150	0	1	0
1.70	1.125	0	1	0
1.65	1.100	0	1	1
1.60	1.075	1	0	0
1.55	1.050	1	0	1
1.50	1.025	1	0	1
1.45	1.000	1	0	1
1.40	0.975	1	1	0
1.35	0.950	1	1	0
1.30	0.925	1	1	0
NO CPU	NO CPU	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

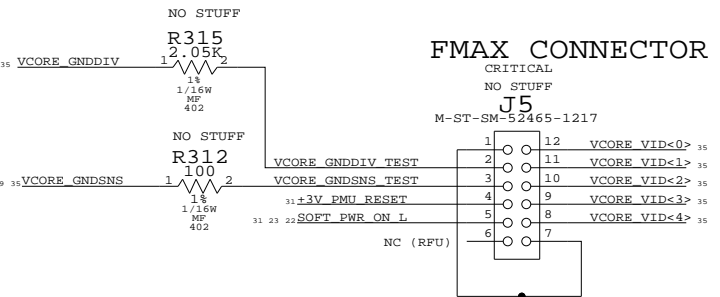
If all pull-ups are >=100K and all pull-downs are <=1K, V_B = V

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
V_{REF} = 2.0V WITH A 0.85 SCALE FACTOR, HENCE V_{OFFSET} = 1.7V * (R1/(R1+R2)) AND V_{VCORE} = V_{DAC} + V_{OFFSET}.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

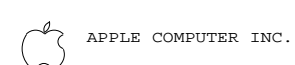


FMAX CONNECTOR

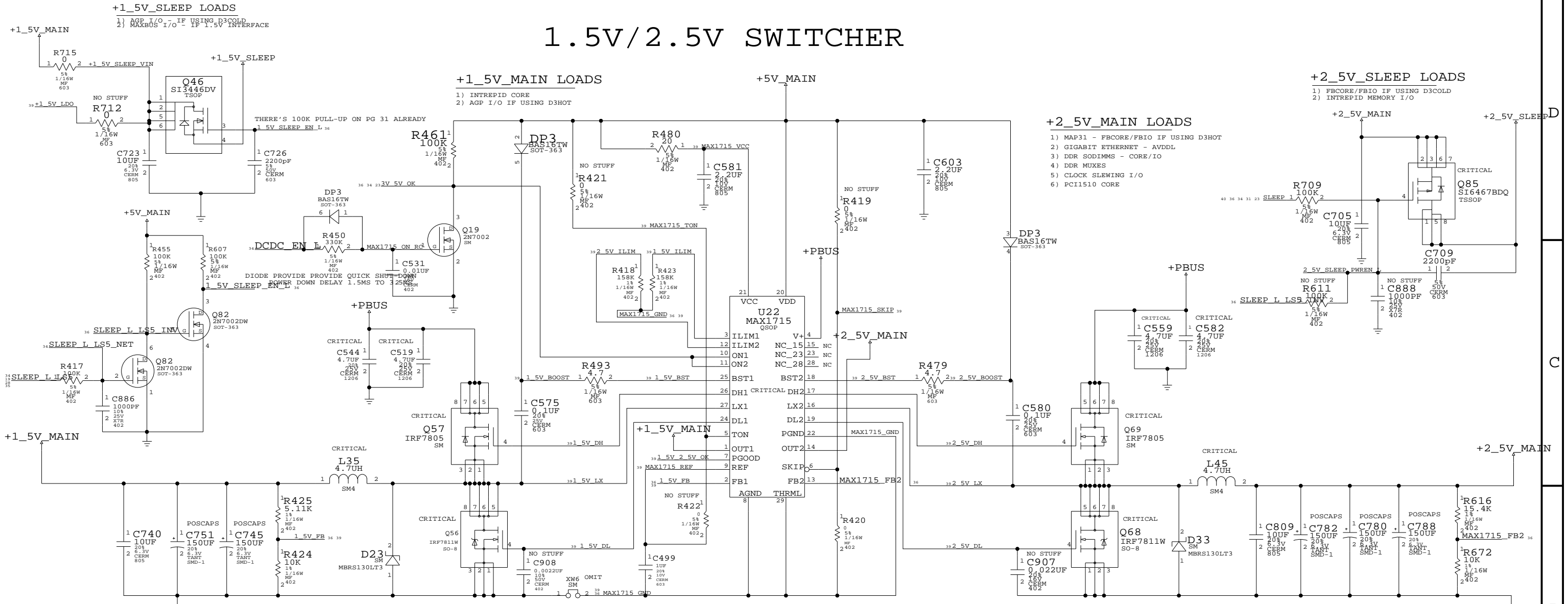
VCORE SUPPLY

NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

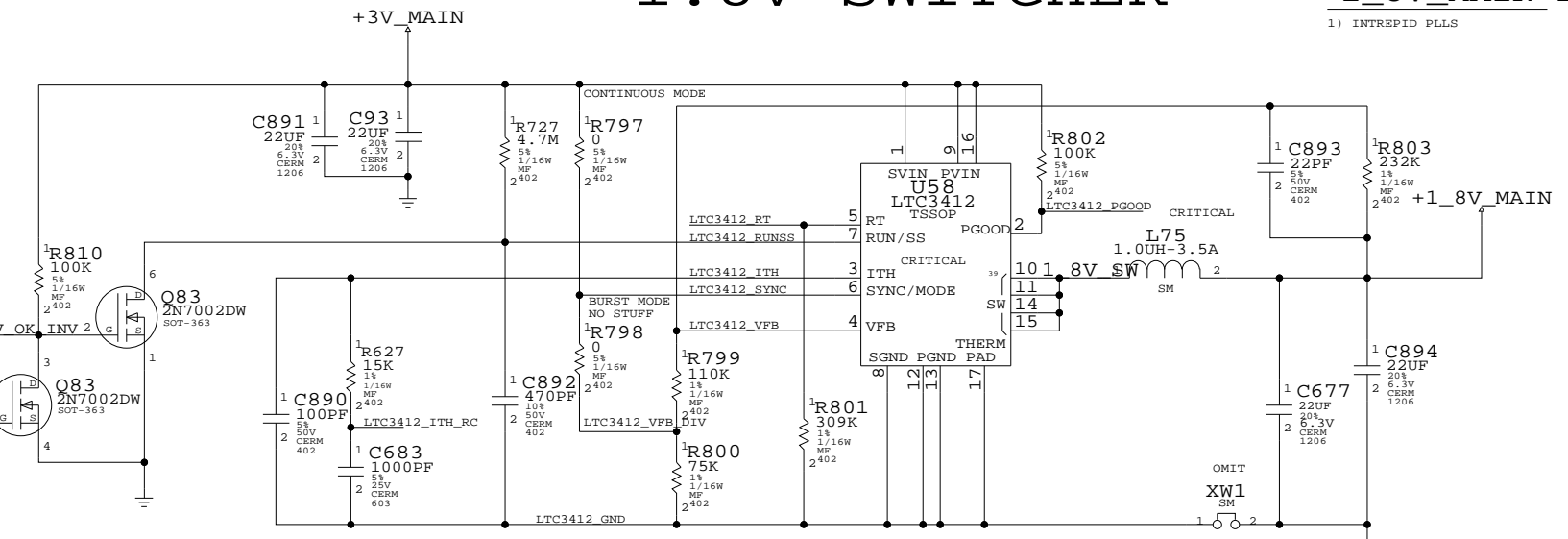
SCALE	DRAWING NUMBER	REV.
NONE	D 051-6694	02
SHEET	OF	
35	45	



1.5V/2.5V SWITCHER



1.8V SWITCHER



1.5V/1.8V/2.5V SUPPLIES

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6694	02
SCALE	SHT	OF	
NONE	36	45	

	8	7	6	5	4	3	2	1			
DIGITAL SIGNALS	MAXBUS	GROUP	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING	TYPE	PULSE_PARAM		
		CPU_AACK_L			250.0000	10 MIL SPACING					
		CPU_ADDR<0..31>	5		250				83 MHZ		
		CPU_ARTRY_L			250.0000	10 MIL SPACING					
		CPU_BG_L			250.0000	10 MIL SPACING					
		CPU_BR_L			250.0000	10 MIL SPACING					
		CPU_CI_L	5		250.0000				83 MHZ		
		CPU_DATA<0..31>	5		250				83 MHZ		
		CPU_DATA<32..63>	5		250				83 MHZ		
		CPU_DBG_L	5		250.0000	10 MIL SPACING					
		CPU_DTI<0..2>	5		250						
		CPU_DRDY_L_UF				10 MIL SPACING					
		CPU_DRDY_L			250.0000	10 MIL SPACING					
		CPU_GBL_L	5		250.0000						
		CPU_HIT_L			250.0000	10 MIL SPACING					
		CPU_OACK_L	5		250.0000	10 MIL SPACING					
		CPU_QREQ_L			250.0000	10 MIL SPACING					
		CPU_TA_L			250.0000	10 MIL SPACING					
		CPU_TBST_L	5		250.0000	10 MIL SPACING					
		CPU_TEA_L			250.0000						
		CPU_TS_L			250.0000	10 MIL SPACING					
		CPU_TSI<0..2>	5		250						
		CPU_TT<0..4>	5		250						
		CPU_WT_L	5		250.0000						
		GROUP 0	MEM_DATA<7..0>	4		200				167 MHZ	
	RAM_DATA_A<7..0>		4		200				167 MHZ		
	RAM_DATA_B<7..0>		4		200				167 MHZ		
	MEM_DQS<0>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200						
	RAM_DQS_A<0>		4		200						
	RAM_DQS_B<0>		4		200						
	MEM_DQM<0>		4		200						
	RAM_DQM_A<0>		4		200						
	RAM_DQM_B<0>		4		200						
	MEM_DATA<15..8>		4		200					167 MHZ	
	RAM_DATA_A<15..8>		4		200					167 MHZ	
	RAM_DATA_B<15..8>		4		200					167 MHZ	
	MEM_DQS<1>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200						
	RAM_DQS_A<1>		4		200						
	RAM_DQS_B<1>		4		200						
	MEM_DQM<1>		4		200						
	RAM_DQM_A<1>		4		200						
	RAM_DQM_B<1>		4		200						
	MEM_DATA<31..16>		4		200					167 MHZ	
	RAM_DATA_A<31..16>		4		200					167 MHZ	
	RAM_DATA_B<31..16>		4		200					167 MHZ	
	MEM_DQS<3..2>		4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200						
	RAM_DQS_A<3..2>		4		200					167 MHZ	
	RAM_DQS_B<3..2>		4		200					167 MHZ	
	MEM_DQM<3..2>		4		200						
	RAM_DQM_A<3..2>	4		200					167 MHZ		
	RAM_DQM_B<3..2>	4		200					167 MHZ		
	MEM_DATA<47..32>	4		200					167 MHZ		
	RAM_DATA_A<47..32>	4		200					167 MHZ		
	RAM_DATA_B<47..32>	4		200					167 MHZ		
	MEM_DQS<5..4>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200							
	RAM_DQS_A<5..4>	4		200					167 MHZ		
	RAM_DQS_B<5..4>	4		200					167 MHZ		
	MEM_DQM<5..4>	4		200							
	RAM_DQM_A<5..4>	4		200					167 MHZ		
	RAM_DQM_B<5..4>	4		200					167 MHZ		
	MEM_DATA<55..48>	4		200					167 MHZ		
	RAM_DATA_A<55..48>	4		200					167 MHZ		
	RAM_DATA_B<55..48>	4		200					167 MHZ		
	MEM_DQS<6>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200							
	RAM_DQS_A<6>	4		200							
	RAM_DQS_B<6>	4		200							
	MEM_DQM<6>	4		200							
	RAM_DQM_A<6>	4		200							
	RAM_DQM_B<6>	4		200							
	MEM_DATA<63..56>	4		200					167 MHZ		
	RAM_DATA_A<63..56>	4		200					167 MHZ		
	RAM_DATA_B<63..56>	4		200					167 MHZ		
	MEM_DQS<7>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200							
	RAM_DQS_A<7>	4		200							
	RAM_DQS_B<7>	4		200							
	MEM_DQM<7>	4		200							
	RAM_DQM_A<7>	4		200							
	RAM_DQM_B<7>	4		200							
	MEM_ADDR<12..0>	4							83 MHZ		
	RAM_ADDR<12..0>	6		200							
	MEM_BA<1..0>	4									
	RAM_BA<1..0>	6		200							
	MEM_CS_L<3..0>	4									
	RAM_CS_L<3..0>	6		200							
	MEM_CKE<3..0>	4									
	RAM_CKE<3..0>	6		200							
	MEM_RAS_L	4									
	RAM_RAS_L	4		200.0000							
	MEM_CAS_L	4									
	RAM_CAS_L	4		200.0000							
	MEM_WE_L	4									
	RAM_WE_L	4		200.0000							
	MEM_MUXSEL_H<1..0>	3									
	MEM_MUXSEL_L<1..0>	3									
	RAM_MUXSEL_H	5									
	RAM_MUXSEL_L	5									
	CLOCK LINE CONSTRAINTS	INTREPID CLOCKS	GROUP	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING	TYPE	PULSE_PARAM	
			SYSCLK_CPU_UF							10 MIL SPACING	
			SYSCLK_CPU	4			200.0000			10 MIL SPACING	
			INT_CPUFB_OUT	3						10 MIL SPACING	
INT_CPUFB_OUT_SHORT			3						10 MIL SPACING		
INT_CPUFB_OUT_NORM			3						10 MIL SPACING		
INT_CPUFB_IN_NORM			3						10 MIL SPACING		
INT_CPUFB_LONG			3						10 MIL SPACING		
INT_CPUFB_IN			3						10 MIL SPACING		
SYSCLK_DDRCLK_A0_UF							200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A0_L_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A1_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A1_L_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B0_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B0_L_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B1_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B1_L_UF			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A0							200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A0_L							200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A1			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_A1_L							200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B0			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B0_L							200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B1			3				200.0000			10 MIL SPACING	
SYSCLK_DDRCLK_B1_L							200.0000			10 MIL SPACING	
INT_REF_CLK_OUT		3				200.0000			10 MIL SPACING		
INT_REF_CLK_IN						200.0000			10 MIL SPACING		
CLK66M_GPU_AGP_UF						200.0000			10 MIL SPACING		
CLK66M_GPU_AGP		4				200.0000			10 MIL SPACING		
INT_AGP_FB_OUT						200.0000			10 MIL SPACING		
INT_AGP_FB_IN		4				200.0000			10 MIL SPACING		
CLK33M_CBUS_UF						200.0000			10 MIL SPACING		
CLK33M_CBUS						200.0000		SHOULD BE AT MOST 4 VIAS FOR CLK	10 MIL SPACING		
CLK33M_AIRPORT_UF						200.0000			10 MIL SPACING		
CLK33M_AIRPORT						200.0000		SHOULD BE AT MOST 4 VIAS FOR CLK	10 MIL SPACING		
CLK33M_USB2_UF						200.0000			10 MIL SPACING		
CLK33M_USB2						200.0000		SHOULD BE AT MOST 4 VIAS FOR CLK	10 MIL SPACING		
INT_PCI_FB_OUT						200.0000			10 MIL SPACING		
INT_PCI_FB_IN		3				200.0000			10 MIL SPACING		
MAP31		GPU_CLK27M_OUT							10 MIL SPACING		
		GPU_CLK27M_UF							10 MIL SPACING		
		GPU_SSCLK_UF							10 MIL SPACING		
		GPU_SSCLK_IN							10 MIL SPACING		
		GPU_FBCLK0							10 MIL SPACING		
		GPU_FBCLK0_L							10 MIL SPACING		
		GPU_FBCLK1							10 MIL SPACING		
		GPU_FBCLK1_L							10 MIL SPACING		
		GPU_DVO_CLKP							10 MIL SPACING		
		CRYSTALS	CLK27M_GPU_XOUT							10 MIL SPACING	
CLK27M_XTAL_IN									10 MIL SPACING		
CLK27M_GPU_XIN									10 MIL SPACING		
CLK18M_INT_XIN									10 MIL SPACING		
CLK18M_INT_XOUT									10 MIL SPACING		
CLK18M_XTAL_IN									10 MIL SPACING		
CLK18M_INT_EXT									10 MIL SPACING		
CLK25M_ENET_XIN									10 MIL SPACING		
CLK25M_ENET_XOUT									10 MIL SPACING		
NEC_XT1									10 MIL SPACING		
NEC_XT2							THERE'S ANOTHER 280MIL LEG	10 MIL SPACING			
SOUND		SND_SCLK	7						200.0000	10 MIL SPACING	
		SND_CLKOUT							200.0000	10 MIL SPACING	
ETHERNET MARVELL		CLKENET_PHY_RX							200.0000		
		CLKENET_LINK_RX	3						200.0000	10 MIL SPACING	
		CLKENET_PHY_GBE_REF							200.0000		
		CLKENET_LINK_GBE_REF	3						200.0000	10 MIL SPACING	
		CLKENET_PHY_TX							200.0000		
CLKENET_LINK_TX		5						200.0000	10 MIL SPACING		
CLKENET_LINK_GTX								200.0000			
CLKENET_PHY_GTX		3						200.0000	10 MIL SPACING		
FIREWIRE		CLKFW_PHY_PCLK							200.0000		
		CLKFW_LINK_PCLK	3						200.0000	10 MIL SPACING	
		CLKFW_PHY_LCLK	3						200.0000	10 MIL SPACING	
		CLKFW_LINK_LCLK							200.0000		
		FW_XI							200.0000	10 MIL SPACING	
FW_OSC								200.0000	10 MIL SPACING		

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHZ	
	AGP_CBE<1..0>		5	100				66 MHZ	
	AGP_AD_STB<0>		5	100		8 MIL SPACING			
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			
	AGP_AD<31..16>		5	100				66 MHZ	
	AGP_CBE<3..2>		5	100				66 MHZ	
	AGP_AD_STB<1>		5	100		8 MIL SPACING			
	AGP_AD_STB_L<1>		5	100		8 MIL SPACING			
	AGP_SBA<7..0>		5	100				66 MHZ	
	AGP_SB_STB		100.0000			8 MIL SPACING			
AGP_SB_STB_L		100.0000			8 MIL SPACING				
AGP CONTROL	AGP_FRAME_L			250.0000					
	AGP_IRDY_L			250.0000					
	AGP_TRDY_L		6	250.0000					
	AGP_DEVSEL_L			250.0000					
	AGP_STOP_L		6	250.0000					
	AGP_PAR		6	250.0000					
	AGP_REQ_L			285.0000					
	AGP_GNT_L			250.0000					
	AGP_RBF_L			250.0000					
	GPU_DVDD<0..23>		5	250					
GPU_DVO_HSYNC									
GPU_DVO_VSYNC									
PCI	PCI_AD<31..0>					MIN DAISY CHAIN		33 MHZ	
	PCI_CBE<3..0>					MIN DAISY CHAIN		33 MHZ	
	PCI_FRAME_L					MIN DAISY CHAIN			
	PCI_IRDY_L					MIN DAISY CHAIN			
	PCI_TRDY_L					MIN DAISY CHAIN			
	PCI_DEVSEL_L					MIN DAISY CHAIN			
	PCI_STOP_L					MIN DAISY CHAIN			
	PCI_PAR					MIN DAISY CHAIN			
	ULTRA ATA-100	UIDE_DATA<15..8>			200				100 MHZ
	UIDE_DATA<7>				200				100 MHZ
UIDE_DATA<6..0>				200				100 MHZ	
UIDE_ADDR<2..0>				200				100 MHZ	
UIDE_RST_L				200.0000					
UIDE_DIOW_L				200.0000					
UIDE_DIOR_L				200.0000		10 MIL SPACING			
UIDE_DMACK_L				200.0000					
UIDE_CS0_L				200.0000					
UIDE_CS1_L				200.0000					
UIDE_DMARQ				200.0000					
UIDE_IOCHRDY				200.0000		10 MIL SPACING			
UIDE_INTRO				200.0000					
HD_DATA<15..0>				200				100 MHZ	
HD_ADDR<2..0>				200				100 MHZ	
HD_RESET_L				200.0000					
HD_DIOW_L				200.0000					
HD_DIOR_L				200.0000		10 MIL SPACING			
HD_DMACK_L				200.0000					
HD_CS0_L				200.0000					
HD_CS1_L				200.0000					
HD_DMARQ				200.0000					
HD_IOCHRDY				200.0000		10 MIL SPACING			
HD_INTRO				200.0000					
EIDE	EIDE_DATA<15..0>			200				100 MHZ	
	EIDE_ADDR<2..0>			200				100 MHZ	
	EIDE_CS0_L			200.0000					
	EIDE_CS1_L			200.0000					
	EIDE_RD_L			200.0000					
	EIDE_WR_L			200.0000					
	EIDE_IOCHRDY			200.0000		10 MIL SPACING			
	EIDE_INT			200.0000					
	EIDE_RST_L			200.0000					
	EIDE_DMACK_L			200.0000					
OPTICAL	UIDE_OPTICAL_DATA<15..0>			200				100 MHZ	
	UIDE_OPTICAL_ADDR<2..0>			200				100 MHZ	
	EIDE_OPTICAL_CS0_L			200.0000					
	EIDE_OPTICAL_CS1_L			200.0000					
	EIDE_OPTICAL_RD_L			200.0000					
	EIDE_OPTICAL_WR_L			200.0000					
	EIDE_OPTICAL_IOCHRDY			200.0000		10 MIL SPACING			
	EIDE_OPTICAL_INT			200.0000					
	EIDE_OPTICAL_RST_L			200.0000					
	EIDE_OPTICAL_DMAACK_L			200.0000					
ETHERNET MI	ENET_LINK_RXD<7..0>		5						
	ENET_RX_DV								
	ENET_RX_ER								
	ENET_PHY_TXD<7..0>		5						
	ENET_LINK_TXD<7..0>								
	ENET_PHY_TX_ER		5						
	ENET_LINK_TX_ER								
	ENET_PHY_TX_EN		5						
	ENET_LINK_TX_EN								
	ENET_MDIO								
FIREWIRE MI	FW_LINK_DATA<7..0>		5						
	FW_PHY_DATA<7..0>		5						
	FW_LINK_CNTL<1..0>								
	FW_PHY_CNTL<1..0>								
	FW_LINK_LREQ								
	FW_PHY_LREQ								
	FW_PINT								

GROUP	SIG_NAME	DIFFERENTIAL PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
ETHERNET MI	MDI M<0>	ENET_MD10			
	MDI P<0>	ENET_MD10			
	MDI M<1>	ENET_MD11		SPACING DELETED BECAUSE OF PHYSICAL CONSTRAINTS AROUND MARVELL PHY	
	MDI P<1>	ENET_MD11			
	MDI M<2>	ENET_MD12			
	MDI P<2>	ENET_MD12			
	MDI M<3>	ENET_MD13			
	MDI P<3>	ENET_MD13			
	RJ45 DN<0>	RJ45_DP0		10 MIL SPACING	
	RJ45 DP<0>	RJ45_DP0		10 MIL SPACING	
FIREWIRE	FW_TPA0N	FW_TPA0		MIN LINE WIDTH=3.4	
	FW_TPA0P	FW_TPA0		MIN LINE WIDTH=3.4	
	FW_TPB0N	FW_TPB0		MIN LINE WIDTH=3.4	
	FW_TPB0P	FW_TPB0		MIN LINE WIDTH=3.4	
	FW_TPI0N	FW_TPI0		MIN LINE WIDTH=3.4	
	FW_TPI0P	FW_TPI0		MIN LINE WIDTH=3.4	
	FW_TPO0N	FW_TPO0		MIN LINE WIDTH=3.4	
	FW_TPO0P	FW_TPO0		MIN LINE WIDTH=3.4	
	FW_TPA1N	FW_TPA1	500.0000	MIN LINE WIDTH=3.4	
	FW_TPA1P	FW_TPA1	500.0000	MIN LINE WIDTH=3.4	
LVDS LOWER	CLKLVDS LN	CLKLVDS_L		10 MIL SPACING	4
	CLKLVDS LP	CLKLVDS_L		10 MIL SPACING	4
	LVDS LON	LVDS_L0		10 MIL SPACING	
	LVDS LOP	LVDS_L0		10 MIL SPACING	
	LVDS LIN	LVDS_L1		10 MIL SPACING	
	LVDS LIP	LVDS_L1		10 MIL SPACING	
	LVDS L2N	LVDS_L2		10 MIL SPACING	
	LVDS L2P	LVDS_L2		10 MIL SPACING	
	CLKLVDS UN	CLKLVDS_U		10 MIL SPACING	4
	CLKLVDS UP	CLKLVDS_U		10 MIL SPACING	4
LVDS UPPER	LVDS UON	LVDS_U0		10 MIL SPACING	
	LVDS UOP	LVDS_U0		10 MIL SPACING	
	LVDS U1N	LVDS_U1		10 MIL SPACING	
	LVDS U1P	LVDS_U1		10 MIL SPACING	
	LVDS U2N	LVDS_U2		10 MIL SPACING	
	LVDS U2P	LVDS_U2		10 MIL SPACING	
	CLKCONN_TMD0	CLKCONN_TMD0		10 MIL SPACING	4
	CLKCONN_TMD1	CLKCONN_TMD1		10 MIL SPACING	4
	TMD0_CLKN	CLKTMD0		10 MIL SPACING	4
	TMD0_CLKP	CLKTMD0		10 MIL SPACING	4
TMDS	TMDS DN<0>	TMDS_D0		10 MIL SPACING	
	TMDS DP<0>	TMDS_D0		10 MIL SPACING	
	TMDS DN<1>	TMDS_D1		10 MIL SPACING	
	TMDS DP<1>	TMDS_D1		10 MIL SPACING	
	TMDS DN<2>	TMDS_D2		10 MIL SPACING	
	TMDS DP<2>	TMDS_D2		10 MIL SPACING	
	NEC_USB_DAM	NEC_USB_DA		MIN LINE WIDTH=5	10 MIL SPACING
	NEC_USB_DAP	NEC_USB_DA		MIN LINE WIDTH=5	10 MIL SPACING
	USB_DEM	USB_DE		5 MIL SPACING	
	USB_DEP	USB_DE		5 MIL SPACING	
USB	NEC_USB_DBM	NEC_USB_DB		MIN LINE WIDTH=5	10 MIL SPACING
	NEC_USB_DBP	NEC_USB_DB		MIN LINE WIDTH=5	10 MIL SPACING
	USB_DFM	USB_DF		5 MIL SPACING	
	USB_DFP	USB_DF		5 MIL SPACING	
	BT_USB_DM	BT_USB_D		5 MIL SPACING	
	BT_USB_DP	BT_USB_D		5 MIL SPACING	
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN LINE WIDTH=5	10 MIL SPACING
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN LINE WIDTH=5	10 MIL SPACING
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN LINE WIDTH=5	10 MIL SPACING
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN LINE WIDTH=5	10 MIL SPACING
POWER SUPPLIES	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING	
	LEFT_USB_DM	LEFT_USB		MIN LINE WIDTH=5	10 MIL SPACING
	LEFT_USB_DP	LEFT_USB		MIN LINE WIDTH=5	10 MIL SPACING
	RIGHT_USB_DM	RIGHT_USB		MIN LINE WIDTH=5	10 MIL SPACING
	RIGHT_USB_DP	RIGHT_USB		MIN LINE WIDTH=5	10 MIL SPACING
	1772_CSSN	1772_CSS			DIFF
	1772_CSSP	1772_CSS			DIFF
	1772_CSIN	1772_CSI			DIFF
	1772_CSIP	1772_CSI			DIFF
3V_SNSM	3V_SNS			DIFF	
3V_SNSP	3V_SNS			DIFF	
5V_SNSM	5V_SNS			DIFF	
5V_SNSP	5V_SNS			DIFF	
THERMOSTATS	THERM1_DM	THERM1			DIFF
	THERM1_DP	THERM1			DIFF
	THERM2_DM	THERM2			DIFF
	THERM2_DP	THERM2			DIFF
	THERM1_M_DM	THERM1_MAIN			DIFF
	THERM1_M_DP	THERM1_MAIN			DIFF
	THERM2_M_DM	THERM2_MAIN			DIFF
	THERM2_M_DP	THERM2_MAIN			DIFF
	THERM1_A_DM	THERM1_ALT			DIFF
	THERM1_A_DP	THERM1_ALT			DIFF
THERM2_A_DM	THERM2_ALT			DIFF	
THERM2_A_DP	THERM2_ALT			DIFF	

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.50HM (USB 1.1)/ 46.20HM (USB 2.0)
ZDIFF = 89.30HM (USB 1.1)/ 89.40HM (USB 2.0)

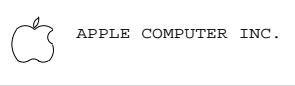
SIGNAL CONSTRAINTS - PAGE 2

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE	SHT	OF
NONE	38	45



POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2.5V MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2.5V SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.8V MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.8V SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+1.5V SLEEP VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	1772 DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	1772 LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	
	1772 LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	1772 DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
1772 GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6		
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+4.85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+4.6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+4.85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
	TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
VIDEO	+12.8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_INV_UP_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+5V_DDC_SLEEP_UP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
KB LED	KBLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	KBLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	

I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
INVERTER	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
TRACKPAD	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
LVDS	CHGND7	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	CHGND8	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
I/O AREA	CHGND9	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	CHGND10	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
I/O AREA	CHGND11	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12
	CHGND12	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	DDR VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	+2.5V INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V INTREPID USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	+1.5V INTREPID PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
REFERENCE	INT MEM VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	INT AGP VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
CARDBUS	INT MEM REF H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	UIIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
ATI M10	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	+GPU MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	+3V GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V GPU FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.5V AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU MEM IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU MEM IO FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+GPU MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1.8V GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2.5V GPU PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	+1.8V ATI_VDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	+1.5V AGP GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	+1.5V GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
+1.8V GPU PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+1.8V GPU_VDD1	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+1.2V GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+2.5V GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+1.8V GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+1.8V GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+1.8V GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10		
+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+1.8V GPU_AVDDO	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+1.8V GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+3V ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+3V ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+GPU_VDD15_UP	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10		
+2.5V SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+3V SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+1.5V AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+1.8V PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+2.5V SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+1.8V SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+1.5V SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
+2.5V SLEEP_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10		
SILICON	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	
	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	
	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	
	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	
	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	
	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	
	88E1111	+2.5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+2.5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+1.0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8
		LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8
		LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
		+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12
+FW_PWR_OR		VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+FW_VPO		VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+FW_PWR_PORTA		VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+FW_VP1		VOLTAGE=3.3V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
+3V_FW		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_UP		VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+1.95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12		
FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12		
FW_TPOOR	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10		
+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8		
+2.5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8		
FW					
USB 2.0					
INTREPID SSCG					

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10
		5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10
		3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
MAX1715 2.5V SWITCHER	2.5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=5	MIN_NECK_WIDTH=10	
	2.5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	2.5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	2.5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	2.5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
1.5V SWITCHER	1.5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	1.5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=5	MIN_NECK_WIDTH=10	
	1.5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	1.5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	1.5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	1.5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	CONTROL	1.5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
		2.5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
		MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
		MAX1715_SRP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6
MAX1715_KEP		VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10		
MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10		
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	VCORE_DH	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	VCORE_DL	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	
	VCORE_ILIM	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	VCORE_REF	VOLT			

FUNCTIONAL TEST POINTS

8	7	6	5	4	3	2	1
FUNC_TEST=YES JTAG_ASIC_TMS 13 28	FUNC_TEST=YES TMDS_CONN_CLKP 22 38	FUNC_TEST=YES TV_C 22	FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38	FUNC_TEST=YES PCI_PAR 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38	FUNC_TEST=YES +5V_INV_SW 22 39	FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES JTAG_ASIC_TDI 28	FUNC_TEST=YES VGA_R 22	FUNC_TEST=YES TV_Y 22	FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38	FUNC_TEST=YES KBD_Y<0> 31	FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES JTAG_ASIC_TDO 13 14	FUNC_TEST=YES VGA_G 22	FUNC_TEST=YES TV_COMP 22	FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38	FUNC_TEST=YES KBD_Y<1> 31	FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES JTAG_ASIC_TCK 13 28	FUNC_TEST=YES VGA_B 22	FUNC_TEST=YES SND_TO_AUDIO 14 26	FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38	FUNC_TEST=YES FW_TP01P 30 38	FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28	FUNC_TEST=YES VGA_VSYNC 22	FUNC_TEST=YES SND_SYNC 14 26	FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38	FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_IOCHRDRY 25 38	FUNC_TEST=YES KBD_Y<3> 31	FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5	FUNC_TEST=YES VGA_HSYNC 22	FUNC_TEST=YES SND_CLKOUT 14 26 37	FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38	FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25	FUNC_TEST=YES EIDE_OPTICAL_INT 25 38	FUNC_TEST=YES KBD_Y<4> 31	FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES CPU_SRESET_L 5	FUNC_TEST=YES DVI_DDC_CLK_UF 22		FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38	FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25	FUNC_TEST=YES TPAD_F_TXD	FUNC_TEST=YES CHARGE_LED_L 31 32	FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES CPU_HRESET_L 5 6 7	FUNC_TEST=YES DVI_DDC_DATA_UF 22		FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38	FUNC_TEST=YES AIRPORT_PCI_INT_L 14 26	FUNC_TEST=YES TPAD_F_RXD	FUNC_TEST=YES ADAPTER_DET 31 32	FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES JTAG_CPU_TMS 5 6 23	FUNC_TEST=YES LVDS_HPD_UF 22	FUNC_TEST=YES INT_AUDIO_TO_SND 14 26	FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38	FUNC_TEST=YES LID_CLOSED_L 23	FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25	FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES JTAG_CPU_TDI 5 6 23	FUNC_TEST=YES LVDS_L0N 19 22 38	FUNC_TEST=YES SND_SCLK 14 26 37	FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38	FUNC_TEST=YES COMM_RESET_L 14 26	FUNC_TEST=YES SUTRO_ALS_OUT 23 25	FUNC_TEST=YES DDDC_EN 19 30 34 35
FUNC_TEST=YES JTAG_CPU_TDO_TP 5	FUNC_TEST=YES LVDS_L0P 19 22 38	FUNC_TEST=YES SND_HW_RESET_L 14 26	FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38	FUNC_TEST=YES COMM_SHUTDOWN 14 26	FUNC_TEST=YES +BATT_POS 32 39	FUNC_TEST=YES BRANG_HRESET_L 6 23
FUNC_TEST=YES JTAG_CPU_TCK 5 6	FUNC_TEST=YES LVDS_L1N 19 22 38	FUNC_TEST=YES SND_HP_SENSE_L	FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38	FUNC_TEST=YES COMM_RING_DET_L 14 26 31	FUNC_TEST=YES BATT_CLK 32	
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 23 40	FUNC_TEST=YES LVDS_L1P 19 22 38	FUNC_TEST=YES SND_LIN_SENSE_L	FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38	FUNC_TEST=YES COMM_RING_DET_L 14 26 31	FUNC_TEST=YES BATT_DATA 32	FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
	FUNC_TEST=YES LVDS_L2N 19 22 38	FUNC_TEST=YES INT_I2C_DATA2 14 26	FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38	FUNC_TEST=YES +5V_TPAD_SLEEP	FUNC_TEST=YES BATT_NEG 32 39	FUNC_TEST=YES RF_DISABLE_L_SPN 25
	FUNC_TEST=YES LVDS_L2P 19 22 38	FUNC_TEST=YES INT_I2C_CLK2 14 26	FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38	FUNC_TEST=YES +3V_HALL_EFFECT 23 39	FUNC_TEST=YES PMU_BATT_DET_L 31 32	FUNC_TEST=YES AIRPORT_CLKRUN_L 25
	FUNC_TEST=YES CLKLVDS_LN 19 22 38	FUNC_TEST=YES CHGND4 39	FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38	FUNC_TEST=YES KBD_CAPSLOCK_LED	FUNC_TEST=YES FANR_GND 26 39	FUNC_TEST=YES ROM_RW_L 9 12 25
	FUNC_TEST=YES CLKLVDS_LP 19 22 38	FUNC_TEST=YES SLEEP_LED	FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38	FUNC_TEST=YES KBD_FUNCTION_L 23 31	FUNC_TEST=YES COMM_DTR_L 14 26	FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23	FUNC_TEST=YES LVDS_U0N 19 22 38		FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38	FUNC_TEST=YES KBD_CONTROL_L 23 31	FUNC_TEST=YES COMM_RXD 14 26	FUNC_TEST=YES ROM_CS_L 9 12 25
FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23	FUNC_TEST=YES LVDS_U0P 19 22 38		FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38	FUNC_TEST=YES +PPBATT_ISSNS_N 24	FUNC_TEST=YES FANL_TACH 26	FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26	FUNC_TEST=YES LVDS_U1N 19 22 38	FUNC_TEST=YES BT_USB_DM 14 25 38	FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38	FUNC_TEST=YES KBD_OPTION_L 23 31	FUNC_TEST=YES FANR_PWM 26	FUNC_TEST=YES AIRPORT_IDSEL 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26	FUNC_TEST=YES LVDS_U1P 19 22 38	FUNC_TEST=YES BT_USB_DP 14 25 38	FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38	FUNC_TEST=YES KBD_SHIFT_L 23 31	FUNC_TEST=YES FANL_PWM 26	FUNC_TEST=YES ROM_OE_L 9 12 25
FUNC_TEST=YES CBUS_DET_1_L 17	FUNC_TEST=YES LVDS_U2N 19 22 38	FUNC_TEST=YES MODEM_USB_DM 14 26 38	FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38	FUNC_TEST=YES KBD_X<0> 23 31	FUNC_TEST=YES RJ45_DP<0> 28 38	FUNC_TEST=YES INT_MOD_DTI 14 26
FUNC_TEST=YES CBUS_DET_2_L 17	FUNC_TEST=YES LVDS_U2P 19 22 38	FUNC_TEST=YES MODEM_USB_DP 14 26 38	FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38	FUNC_TEST=YES KBD_X<1> 23 31	FUNC_TEST=YES RJ45_DP<1> 28 38	FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 23 40
FUNC_TEST=YES TMDS_DN<0> 20 22 38	FUNC_TEST=YES CLKLVDS_UN 19 22 38	FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38	FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38	FUNC_TEST=YES KBD_X<3> 23 31	FUNC_TEST=YES RJ45_DP<2> 28 38	FUNC_TEST=YES GPU_VCORE 18 19 39
FUNC_TEST=YES TMDS_DP<0> 20 22 38	FUNC_TEST=YES CLKLVDS_UP 19 22 38	FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38	FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38	FUNC_TEST=YES MMM_ACC_SELPTST 24	FUNC_TEST=YES RJ45_DP<3> 28 38	FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
FUNC_TEST=YES TMDS_DN<1> 20 22 38	FUNC_TEST=YES LVDS_DDC_CLK 19 22	FUNC_TEST=YES PCI_AD<32> 9 12 17 25 27 38	FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38	FUNC_TEST=YES MMM_ACC_X_AXIS 24	FUNC_TEST=YES RJ45_DP<4> 28 38	FUNC_TEST=YES MOD_BITCLK 14 26
FUNC_TEST=YES TMDS_DP<1> 20 22 38	FUNC_TEST=YES LVDS_DDC_DATA 19 22	FUNC_TEST=YES PCI_AD<33> 9 12 17 25 27 38	FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38	FUNC_TEST=YES MMM_ACC_Y_AXIS 24	FUNC_TEST=YES RJ45_DP<5> 28 38	FUNC_TEST=YES MOD_CLKOUT 14 26
FUNC_TEST=YES TMDS_DN<2> 20 22 38	FUNC_TEST=YES BRIGHT_PWM 22	FUNC_TEST=YES PCI_IRDY<4> 9 12 17 25 27 38	FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38	FUNC_TEST=YES MMM_ACC_Z_AXIS 24	FUNC_TEST=YES RJ45_DP<6> 28 38	FUNC_TEST=YES VCORE_FB 35 39
FUNC_TEST=YES TMDS_DP<2> 20 22 38	FUNC_TEST=YES TV_GND1 22 39	FUNC_TEST=YES PCI_AD<5> 9 12 17 25 27 38	FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38	FUNC_TEST=YES FW_TPOUR 30 39	FUNC_TEST=YES RJ45_DP<7> 28 38	FUNC_TEST=YES +1_8V_MAIN 39
FUNC_TEST=YES TMDS_CONN_CLKN 22 38	FUNC_TEST=YES TV_GND2 22 39	FUNC_TEST=YES PCI_AD<6> 9 12 17 25 27 38	FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38	FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38	FUNC_TEST=YES VCORE_VID0	FUNC_TEST=YES +3V_PMU 39	FUNC_TEST=YES SLEEP 23 31 34 36
				FUNC_TEST=NO KBD_X<8> 23 31	FUNC_TEST=NO KBD_X<8> 23 31	FUNC_TEST=YES +5V_DDC_SLEEP 22 39	FUNC_TEST=YES 1778_VFB 19 39
				FUNC_TEST=YES SRCLK_TP 27	FUNC_TEST=YES SRCLK_TP 27	FUNC_TEST=YES +12_8V_INV 22 39	
				FUNC_TEST=YES SRMOD_TP 27	FUNC_TEST=YES SRMOD_TP 27	FUNC_TEST=YES VCORE_MUX_EN 35	
				FUNC_TEST=YES TEB_TP 27	FUNC_TEST=YES TEB_TP 27	FUNC_TEST=YES VCORE_VID1	
				FUNC_TEST=YES TEST_TP 27	FUNC_TEST=YES TEST_TP 27	FUNC_TEST=YES VCORE_VID2	
						FUNC_TEST=YES VCORE_VID3	
						FUNC_TEST=YES VCORE_VID4	

NOTICE OF PROPRIETARY PROPERTY
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
 II NOT TO REPRODUCE OR COPY IT
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-6694	02
	SHEET	OF	
	40	45	

REVISION HISTORY

12/11/03

- 1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
- 2) CHANGED CPU (U43) TO A7PM
- 3) CHANGED PLL CONFIG STEERING FOR NEW CPU
- 4) CHANGED U44 TO 1884 SYMBOL
- 5) ADDED CPU_AVDD_LDO (U6)
- 6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
- 7) ADDED R608 TO DISCONNECT INT_GP100 FROM OC_FSEL
- 8) CHANGED JTAG_ASIC_TDO TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
- 9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

- 10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
- 11) CHANGED PIN 11 OF J11 TO NC

12/16/03

- 12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
- 13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
- 14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
- 15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
- 16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
- 17) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
- 18) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

- 18) CHANGED R657 (EXTPLL_SDNV_POL_BOOT_STRAP) TO NO STUFF AND REMOVED NO STUFF FROM R153
- 19) UPDATE DIFF NET SPACING TYPE PROPERTY ON POWER SUPPLY SENSE AND THERMAL DIODE DIFF PAIRS
- 20) CHANGED FIREWIRE_OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

- 21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

- 22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
- 23) CHANGED R657 TO STUFFE AND R153 TO NO STUFF
- 24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

- 25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

- 26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
- 27) ADDED ALTERNATES FOR 120M AND 64M A16 M11'S
- 28) CHANGED TMS SERIES RPAKS TO 0 OHMS (RP57,RP27,RP32,RP28)
- 29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

- 30) CHANGED TMS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

- 1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
- 2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
- 3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
- 4) ADD C935 (0.1UF)
- 5) ADD R867 (0 OHM) FOR IPOD ACTION
- 6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
- 7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
- 8) ADD R869 (10K OHM) PULL DOWN TO GND
- 9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
- 10) ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
- 11) ADD U51 (INA138)
- 12) ADD R852 (0.010 OHM), R853 (150K OHM) AND R857 (49.9 OHM)
- 13) ADD C917 (0.1UF) AND C925 (10UF)
- 14) ADD DESCRIPTION FOR MMM I2C BUS
- 15) MMM I2C BUS LINK TO INTREPID : INT_I2C_CLK1 AND INT_I2C_DATA1
- 16) CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
- 17) CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
- 18) ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L & MMM_SIRQ_L PULL UP TO +3V_MAIN
- 19) ADD U53 (16F818) AND U5 (KXM52)
- 20) ADD R845 (0 OHM), R846 (0 OHM; NO_STUFF), R847 (10K OHM; NO_STUFF), R848 (10K OHM; NO_STUFF)
- 21) ADD R849 (10K OHM), R850 (10K OHM; NO_STUFF), R851 (0 OHM), R854 (10K OHM), R856 (10K OHM)
- 22) ADD R860 (0 OHM), R858 (0 OHM), R859 (0 OHM), R855 (10K OHM), R861 (10K OHM), R862 (10K OHM; NO_STUFF)
- 23) ADD C936 (0.1UF), C918 (0.1UF), C919 (0.1UF), C921 (0.0047UF), C923 (0.0047UF), C926 (0.0047UF), C927 (0.1UF)
- 24) DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
- 25) ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
- 26) ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80; 5.5V; ELEC; 0.33F)
- 27) J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
- 28) J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
- 29) J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
- 30) C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%, 50V, 0603)
- 31) U59 FROM MP1518DJ CHANGE TO MM3120
- 32) L11 CHANGE TO 152S0235 (22UH; 3.8*3.8*1.5MM)
- 33) DEL D31
- 34) R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
- 35) C79 VALUE FROM 2.2UF CHANGE TO 1UF
- 36) ADD Q70 (SI3443), Q34 (2N7002)
- 37) ADD R866 (100K OHM), R865 (4.7 OHM), C929 (0.022UF)

09/20/2004

- 1) ADD R877 (10K OHM)
- 2) ADD R876 (470K OHM; NO_STUFF)

09/21/2004

- 1) ADD R878 AND R879 (0 OHM; NO_STUFF) [ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

- 1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

- 1) ADD NC NETNAME AT U59 PIN6 AND PIN9
- 2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
- 3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

- 1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
- 2) ADD R880 AND R871 (0 OHM; BOM_OPTION; FOR SUPERCAP AND BACKUP BATTERY SWITCH)
- 3) ADD U60 (LIS3L02AQ; ST SENSOR)
- 4) ADD R881 (10K OHM), R882 (10K OHM), R883 (10K OHM)
- 5) ADD C937 (0.1UF, 10V, 20%, 0402)
- 6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

- 1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
- 2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD, MMM_PIC_AN3_PU)

10/05/2004

- 1) ADD R850 (0 OHM)

QUANTA EE, PLEASE ADD SCHEMATIC UPDATE DETAILS HERE.

10/15/2004

- 1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	02
SCALE	SHT	OF
NONE	41	45

	8	7	6	5	4	3	2	1
D	R210 RES 24 R311 RES 19 R312 RES 35 R313 RES 35 R314 RES 35 R315 RES 35 R316 RES 19 R317 RES 22 R318 RES 35 R319 RES 28 R320 RES 22 R321 RES 35 R322 RES 35 R323 RES 35 R324 RES 35 R325 RES 35 R326 RES 35 R327 RES 35 R328 RES 35 R329 RES 35 R330 RES 35 R331 RES 35 R332 RES 19 R333 RES 28 R334 RES 28 R335 RES 28 R336 RES 35 R337 RES 35 R338 RES 9 R339 RES 19 R340 RES 19 R341 RES 19 R342 RES 22 R343 RES 28 R344 RES 28 R345 RES 28 R346 RES 28 R347 RES 28 R348 RES 17 R349 RES 35 R350 RES 14 R351 RES 19 R352 RES 19 R353 RES 28 R354 RES 28 R355 RES 28 R356 RES 35 R357 RES 9 R358 RES 12 R359 RES 33 R360 RES 33 R361 RES 28 R362 RES 28 R363 RES 32 R364 RES 32 R365 RES 32 R366 RES 35 R367 RES 34 R368 RES 34 R369 RES 34 R370 RES 28 R371 RES 28 R372 RES 28 R373 RES 17 R374 RES 32 R375 RES 32 R376 RES 35 R377 RES 14 R378 RES 34 R379 RES 33 R380 RES 28 R381 RES 28 R382 RES 28 R383 RES 32 R384 RES 35 R385 RES 35 R386 RES 9 R387 RES 9 R388 RES 19 R389 RES 19 R390 RES 19 R391 RES 22 R392 RES 32 R393 RES 28 R394 RES 32 R395 RES 32 R396 RES 35 R397 RES 15 R398 RES 22 R400 RES 22 R401 RES 33 R402 RES 33 R403 RES 28 R404 RES 28 R405 RES 26 R406 RES 28 R407 RES 35 R408 RES 35 R409 RES 9 R410 RES 19 R411 RES 25 R412 RES 33 R413 RES 28 R414 RES 32 R415 RES 35 R416 RES 19 R417 RES 36 R418 RES 36 R419 RES 36 R420 RES 36 R421 RES 36 R422 RES 36 R423 RES 36 R424 RES 36 R425 RES 36 R426 RES 33 R427 RES 28 R428 RES 28 R429 RES 35 R430 RES 19 R431 RES 34 R432 RES 33 R433 RES 33 R434 RES 35 R435 RES 28 R436 RES 28 R437 RES 29 R438 RES 28 R439 RES 9 R440 RES 11 R441 RES 25 R442 RES 25 R443 RES 33 R444 RES 29 R445 RES 29 R446 RES 29 R447 RES 35 R448 RES 35 R449 RES 11 R450 RES 16 R451 RES 19 R452 RES 25 R453 RES 29 R454 RES 32 R455 RES 14 R456 RES 14 R457 RES 34 R458 RES 25 R459 RES 34 R460 RES 32 R461 RES 34 R462 RES 14 R463 RES 34 R464 RES 29 R465 RES 28 R466 RES 32 R467 RES 34 R468 RES 14 R469 RES 29 R470 RES 14 R471 RES 29 R472 RES 30 R473 RES 32 R474 RES 32 R475 RES 31 R476 RES 31 R477 RES 34	R476 RES 29 R480 RES 36 R481 RES 36 R482 RES 34 R483 RES 33 R484 RES 19 R485 RES 29 R486 RES 29 R487 RES 28 R488 RES 32 R489 RES 32 R490 RES 32 R491 RES 31 R492 RES 31 R493 RES 36 R494 RES 29 R495 RES 29 R496 RES 29 R497 RES 32 R498 RES 32 R499 RES 32 R500 RES 9 R501 RES 31 R502 RES 31 R503 RES 31 R504 RES 31 R505 RES 31 R506 RES 34 R507 RES 34 R508 RES 19 R509 RES 29 R510 RES 29 R511 RES 32 R512 RES 32 R513 RES 31 R514 RES 34 R515 RES 34 R516 RES 34 R517 RES 31 R518 RES 31 R519 RES 34 R520 RES 34 R521 RES 33 R522 RES 28 R523 RES 34 R524 RES 29 R525 RES 9 R526 RES 32 R527 RES 26 R528 RES 34 R529 RES 34 R530 RES 14 R531 RES 27 R532 RES 6 R533 RES 6 R534 RES 26 R535 RES 31 R536 RES 31 R537 RES 26 R538 RES 34 R539 RES 34 R540 RES 27 R541 RES 33 R542 RES 28 R543 RES 32 R544 RES 31 R545 RES 27 R546 RES 29 R547 RES 29 R548 RES 26 R549 RES 32 R550 RES 23 R551 RES 27 R552 RES 26 R553 RES 26 R554 RES 9 R555 RES 29 R556 RES 29 R557 RES 29 R558 RES 32 R559 RES 32 R560 RES 32 R561 RES 32 R562 RES 31 R563 RES 29 R564 RES 29 R565 RES 32 R566 RES 32 R567 RES 32 R568 RES 23 R569 RES 33 R570 RES 32 R571 RES 32 R572 RES 28 R573 RES 31 R574 RES 29 R575 RES 29 R576 RES 29 R577 RES 29 R578 RES 32 R579 RES 32 R580 RES 32 R581 RES 26 R582 RES 26 R583 RES 35 R584 RES 31 R585 RES 31 R586 RES 27 R587 RES 19 R588 RES 32 R589 RES 34 R590 RES 27 R591 RES 27 R592 RES 31 R593 RES 31 R594 RES 31 R595 RES 31 R596 RES 31 R597 RES 31 R598 RES 19 R599 RES 32 R600 RES 27 R601 RES 25 R602 RES 25 R603 RES 26 R604 RES 14 R605 RES 23 R606 RES 23 R607 RES 36 R608 RES 14 R609 RES 14 R610 RES 36 R611 RES 36 R612 RES 29 R613 RES 25 R614 RES 14 R615 RES 29 R616 RES 36 R617 RES 23 R618 RES 36 R619 RES 23 R620 RES 31 R621 RES 30 R622 RES 14 R623 RES 26 R624 RES 13 R625 RES 14 R626 RES 13 R627 RES 29 R628 RES 26 R629 RES 13 R630 RES 14 R631 RES 14 R632 RES 14 R633 RES 28 R634 RES 14 R635 RES 14 R636 RES 19 R637 RES 19 R638 RES 14 R639 RES 8 R640 RES 8 R641 RES 8 R642 RES 8 R643 RES 8 R644 RES 8 R645 RES 8	R646 RES 8 R648 RES 8 R649 RES 20 R650 RES 22 R651 RES 8 R652 RES 8 R653 RES 8 R654 RES 8 R655 RES 22 R656 RES 14 R657 RES 8 R658 RES 8 R659 RES 8 R660 RES 8 R661 RES 22 R662 RES 22 R663 RES 22 R664 RES 8 R665 RES 8 R666 RES 8 R667 RES 8 R668 RES 8 R669 RES 8 R670 RES 22 R671 RES 22 R672 RES 36 R673 RES 8 R674 RES 8 R675 RES 8 R676 RES 8 R677 RES 8 R678 RES 28 R679 RES 26 R680 RES 22 R681 RES 22 R682 RES 14 R683 RES 8 R684 RES 8 R685 RES 8 R686 RES 22 R687 RES 22 R688 RES 22 R689 RES 26 R690 RES 26 R691 RES 22 R692 RES 26 R693 RES 5 R694 RES 22 R695 RES 26 R696 RES 26 R697 RES 34 R698 RES 14 R699 RES 14 R700 RES 22 R701 RES 14 R702 RES 5 R703 RES 22 R704 RES 22 R705 RES 22 R706 RES 22 R707 RES 14 R708 RES 14 R709 RES 36 R710 RES 28 R711 RES 19 R712 RES 36 R713 RES 26 R714 RES 20 R715 RES 36 R716 RES 26 R717 RES 26 R718 RES 26 R719 RES 26 R720 RES 14 R721 RES 21 R722 RES 21 R723 RES 26 R724 RES 22 R725 RES 26 R726 RES 26 R727 RES 36 R728 RES 21 R729 RES 14 R730 RES 25 R731 RES 35 R732 RES 28 R733 RES 32 R734 RES 28 R735 RES 28 R736 RES 30 R737 RES 31 R738 RES 32 R739 RES 29 R740 RES 29 R741 RES 30 R742 RES 28 R743 RES 30 R744 RES 32 R745 RES 32 R746 RES 32 R747 RES 32 R748 RES 32 R749 RES 32 R750 RES 17 R751 RES 30 R752 RES 30 R753 RES 17 R754 RES 32 R755 RES 32 R756 RES 17 R757 RES 17 R758 RES 29 R759 RES 29 R760 RES 29 R761 RES 29 R762 RES 17 R763 RES 32 R764 RES 17 R765 RES 20 R766 RES 17 R767 RES 17 R768 RES 31 R769 RES 31 R770 RES 14 R771 RES 23 R772 RES 23 R773 RES 23 R774 RES 32 R775 RES 29 R776 RES 23 R777 RES 23 R778 RES 31 R779 RES 30 R780 RES 14 R781 RES 29 R782 RES 31 R783 RES 27 R784 RES 27 R785 RES 31 R786 RES 31 R787 RES 31 R788 RES 31 R789 RES 30 R790 RES 27 R791 RES 27 R792 RES 27 R793 RES 27 R794 RES 27 R795 RES 27 R796 RES 27 R797 RES 36 R798 RES 36 R799 RES 36 R800 RES 36 R801 RES 36 R802 RES 36 R803 RES 36 R804 RES 19 R805 RES 35 R806 RES 35 R807 RES 35 R808 RES 35 R809 RES 35 R810 RES 35 R811 RES 26 R812 RES 26 R813 RES 26	R814 RES 26 R815 RES 20 R816 RES 20 R817 RES 20 R818 RES 20 R819 RES 14 R820 RES 8 R821 RES 20 R822 RES 20 R823 RES 22 R824 RES 14 R825 RES 14 R826 RES 8 R827 RES 20 R828 RES 20 R829 RES 20 R830 RES 20 R831 RES 20 R832 RES 20 R833 RES 20 R834 RES 20 R835 RES 20 R836 RES 20 R837 RES 20 R838 RES 20 R839 RES 20 R840 RES 20 R841 RES 8 R842 RES 20 R843 RES 31 R844 RES 31 R845 RES 24 R846 RES 24 R847 RES 24 R848 RES 24 R849 RES 24 R850 RES 23 R851 RES 24 R852 RES 24 R853 RES 24 R854 RES 24 R855 RES 24 R856 RES 24 R857 RES 24 R858 RES 24 R859 RES 24 R860 RES 24 R861 RES 5 R862 RES 24 R863 RES 14 R864 RES 14 R865 RES 24 R866 RES 23 R867 RES 14 R868 RES 31 R869 RES 14 R870 RES 22 R871 RES 33 R872 RES 26 R873 RES 26 R874 RES 26 R875 RES 26 R876 RES 35 R877 RES 31 R878 RES 28 R879 RES 26 R880 RES 33 R881 RES 24 R882 RES 6 R883 RES 24 R884 RES 6 R885 RES 6 R886 RES 6 R887 RES 30 R888 RES 30 R889 RES 30 R890 RES 21 R891 RES 30 R892 RES 30 R893 RES 26 R894 RES 14 R895 RES 14 R896 RES 14 R897 RES 14 R901 RES 14 R902 RES 25 R903 RES 25 R904 RES 25 R905 RES 25 R906 RES 25 R907 RES 14 R908 RES 14 R909 RES 25 R910 RES 25 R911 RES 13 R912 RES 25 R913 RES 25 R914 RES 13 R915 RES 13 R916 RES 13 R917 RES 13 R918 RES 13 R919 RES 25 R920 RES 25 R921 RES 12 R922 RES 25 R923 RES 13 R924 RES 13 R925 RES 13 R926 RES 12 R927 RES 12 R928 RES 12 R929 RES 12 R930 RES 12 R931 RES 12 R932 RES 12 R933 RES 12 R934 RES 12 R935 RES 12 R936 RES 12 R937 RES 12 R938 RES 12 R939 RES 12 R940 RES 12 R941 RES 12 R942 RES 12 R943 RES 12 R944 RES 12 R945 RES 12 R946 RES 12 R947 RES 12 R948 RES 12 R949 RES 12 R950 RES 12 R951 RES 12 R952 RES 12 R953 RES 12 R954 RES 12 R955 RES 12 R956 RES 12 R957 RES 12 R958 RES 12 R959 RES 12 R960 RES 12 R961 RES 12 R962 RES 12 R963 RES 12 R964 RES 12 R965 RES 12 R966 RES 12 R967 RES 12 R968 RES 12 R969 RES 12 R970 RES 12 R971 RES 12 R972 RES 12 R973 RES 12 R974 RES 12 R975 RES 12 R976 RES 12 R977 RES 12 R978 RES 12 R979 RES 12 R980 RES 12 R981 RES 12 R982 RES 12 R983 RES 12 R984 RES 12 R985 RES 12 R986 RES 12 R987 RES 12 R988 RES 12 R989 RES 12 R990 RES 12 R991 RES 12 R992 RES 12 R993 RES 12 R994 RES 12 R995 RES 12 R996 RES 12 R997 RES 12 R998 RES 12 R999 RES 12 R1000 RES 12	U19 SWR_CTRL_T9S2211 17 U20 MAX1717 35 U21 COMPANATOR_LMC7211 33 U22 MAX1715 36 U23 AMP_MAX4172 32 U24 7412 22 U25 VREG_L2P5V1 33 U26 PCII5100GV 17 U27 COMPANATOR_LMC7211 31 U28 LTC1707 34 U29 TS881BA3A 29 U30 VREG_L2P5V1 33 U31 MAX1712 32 U32 KEPPROM_32KX8_M242568 6 U33 M16C62 31 U34 VREG_L2P5V1 33 U35 SILL78 20 U36 LTC1761 29 U37 VREG_L2P5V1 33 U38 COMPANATOR_LMC7211 32 U39 UP9720101_P8GA 27 U40 OSAMP_MAX4138EITTT 23 U41 MAX804 31 U42 CLK_GEN_CV28512 14 U43 ANPLL4_M07474_360 5 6 U44 RAGE_MBL2V_M11_CSP64_667 18 19 21 U45 INTREFID 8 9 12 13 14 15 U46 COMPANATOR_LMC7211 22 U47 CLK_GEN_CV28511 18 U48 SILL78 20 U49 TRANSDUCER_H81111 28 U50 OSAMP_LMC7111 32 U51 IMX130 24 U52 FEPR_256KX8_ST72264_BGA 23 U53 PIC16F818_QFN 24 U54 VREG_M015712 21 U55 VREG_M015712 21 U56 741032 22 U57 741032 22 U58 LTC1412 36 U59 MM120 23 U60 LISI20A2 24 U61 AT90E1200 6 U62 COMPANATOR_LMC7211 30 X01 SHORT 19 X02 SHORT 19 X03 SHORT 35 X04 SHORT 33 X05 SHORT 35 X06 SHORT 36 X07 SHORT 35 X08 SHORT 34 X09 SHORT 26 X10 SHORT 26 X11 SHORT 26 X12 SHORT 22 X13 SHORT 22 X14 SHORT 24 X15 SHORT 35 X16 SHORT 24 X17 SHORT 24 X18 SHORT 32 X19 SHORT 19 X20 SHORT 19 X21 SHORT 19 X22 SHORT 21 X23 SHORT 21 X24 SHORT 5 Y1 CRYSTAL 4 Y3 CRYSTAL 28 Y4 CRYSTAL 23 Y5 CRYSTAL 27 Y6 CRYSTAL 31 Y7 CRYSTAL_4P18 31 T71 HOLE_VIA 4 T72 MTHOLE 4 T73 HOLE_VIA 4 T74 MTHOLE 4 T75 MTHOLE 4 T76 MTHOLE 4 T77 HOLE_VIA 4 T78 HOLE_VIA 4 T79 HOLE_VIA 4 T80 MTHOLE 4 T81 MTHOLE 4 T82 HOLE_VIA 4 T83 HOLE_VIA 4 T84 HOLE_VIA 4 T85 HOLE_VIA 4 T86 HOLE_VIA 4 T87 HOLE_VIA 4 T88 HOLE_VIA 4 T89 HOLE_VIA 4 T90 HOLE_VIA 4 T91 HOLE_VIA 4 T92 HOLE_VIA 4 T93 HOLE_VIA 4 T94 HOLE_VIA 4 T95 HOLE_VIA 4 T96 HOLE_VIA 4 T97 HOLE_VIA 4 T98 HOLE_VIA 4 T99 HOLE_VIA 4 T100 HOLE_VIA 4 T101 HOLE_VIA 4 T102 HOLE_VIA 4 T103 HOLE_VIA 4 T104 HOLE_VIA 4 T105 HOLE_VIA 4 T106 HOLE_VIA 4 T107 HOLE_VIA 4 T108 HOLE_VIA 4 T109 HOLE_VIA 4 T110 HOLE_VIA 4 T111 HOLE_VIA 4 T112 HOLE_VIA 4 T113 HOLE_VIA 4 T114 HOLE_VIA 4 T115 HOLE_VIA 4 T116 HOLE_VIA 4 T117 HOLE_VIA 4 T118 HOLE_VIA 4 T119 HOLE_VIA 4 T120 HOLE_VIA 4 T121 HOLE_VIA 4 T122 HOLE_VIA 4 T123 HOLE_VIA 4 T124 HOLE_VIA 4 T125 HOLE_VIA 4 T126 HOLE_VIA 4 T127 HOLE_VIA 4 T128 HOLE_VIA 4 T129 HOLE_VIA 4 T130 HOLE_VIA 4 T131 HOLE_VIA 4 T132 HOLE_VIA 4 T133 HOLE_VIA 4 T134 HOLE_VIA 4 T135 HOLE_VIA 4 T136 HOLE_VIA 4 T137 HOLE_VIA 4 T138 HOLE_VIA 4 T139 HOLE_VIA 4 T140 HOLE_VIA 4 T141 HOLE_VIA 4 T142 HOLE_VIA 4 T143 HOLE_VIA 4 T144 HOLE_VIA 4 T145 HOLE_VIA 4 T146 HOLE_VIA 4 T147 HOLE_VIA 4 T148 HOLE_VIA 4 T149 HOLE_VIA 4 T150 HOLE_VIA 4 T151 HOLE_VIA 4 T152 HOLE_VIA 4 T153 HOLE_VIA 4 T154 HOLE_VIA 4 T155 HOLE_VIA 4 T156 HOLE_VIA 4 T157 HOLE_VIA 4 T158 HOLE_VIA 4 T159 HOLE_VIA 4 T160 HOLE_VIA 4 T161 HOLE_VIA 4 T162 HOLE_VIA 4 T163 HOLE_VIA 4 T164 HOLE_VIA 4 T165 HOLE_VIA 4 T166 HOLE_VIA 4 T167 HOLE_VIA 4 T168 HOLE_VIA 4 T169 HOLE_VIA 4 T170 HOLE_VIA 4 T171 HOLE_VIA 4 T172 HOLE_VIA 4 T173 HOLE_VIA 4 T174 HOLE_VIA 4 T175 HOLE_VIA 4 T176 HOLE_VIA 4 T177 HOLE_VIA 4 T178 HOLE_VIA 4 T179 HOLE_VIA 4 T180 HOLE_VIA 4 T181 HOLE_VIA 4 T182 HOLE_VIA 4 T183 HOLE_VIA 4 T184 HOLE_VIA 4 T185 HOLE_VIA 4 T186 HOLE_VIA 4 T187 HOLE_VIA 4 T188 HOLE_VIA 4 T189 HOLE_VIA 4 T190 HOLE_VIA 4 T191 HOLE_VIA 4 T192 HOLE_VIA 4 T193 HOLE_VIA 4 T194 HOLE_VIA 4 T195 HOLE_VIA 4 T196 HOLE_VIA 4 T197 HOLE_VIA 4 T198 HOLE_VIA 4 T199 HOLE_VIA 4 T200 HOLE_VIA 4	B	C	D
A	8	7	6	5	4	3	2	1