

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
C	0000734528	PRODUCTION RELEASED		2009-06-04

K24 MLB SCHEMATIC

6/12/2009

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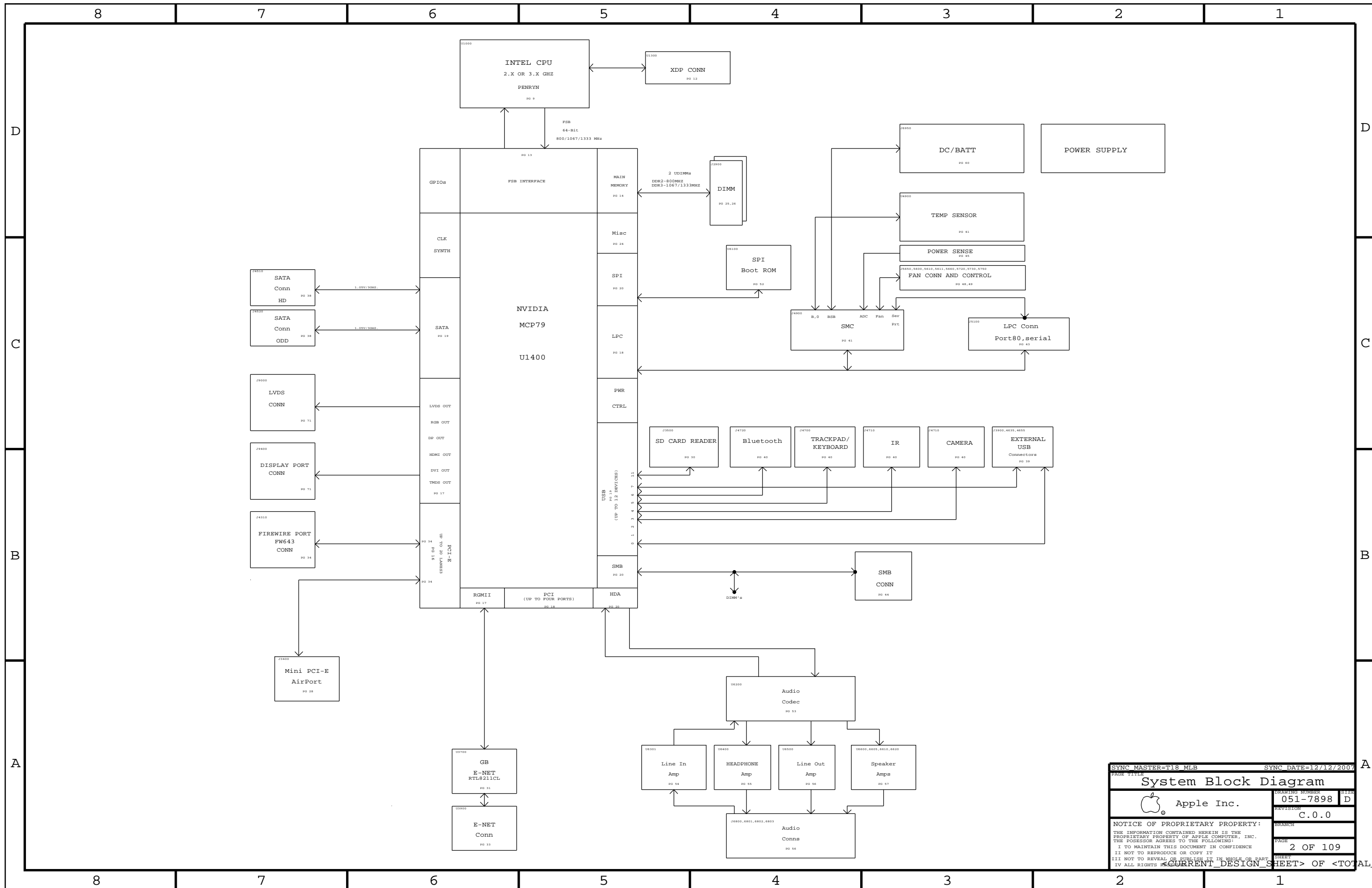
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46	Thermal Sensors	YUNWU	03/20/2008
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74	Memory Constraints	T18_MLB	01/04/2008
75	MCP Constraints 1	T18_MLB	01/04/2008
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Schematic / PCB #'s

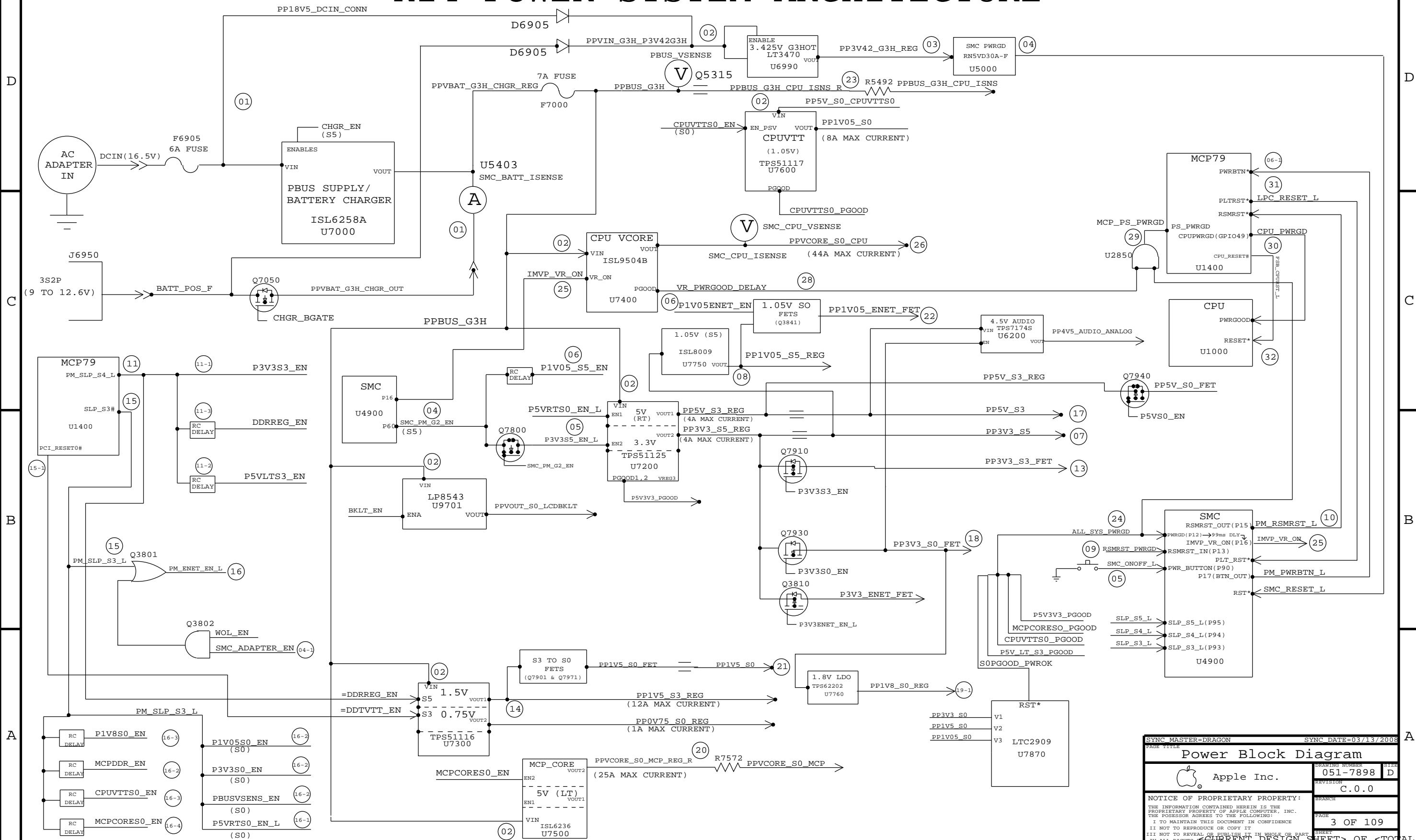
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7898	1	SCHEM,MLB,K24	SCH	CRITICAL	
820-2530	1	PCBF,MLB,K24	PCB	CRITICAL	

DRAWING TITLE		SCHEM,MLB,K24	
Apple Inc.	DRAWING NUMBER	051-7898	SIZE
	REVISION	C.0.0	D
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SYNC MASTER=T18 MLB		SYNC DATE=12/12/2007	
System Block Diagram			
Apple Inc.		CREATION NUMBER	051-7898 D
		REVISION	C.0.0
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K24 POWER SYSTEM ARCHITECTURE



PAGE TITLE		SYNC DATE=03/13/2008	
Power Block Diagram			
Apple Inc.		DRAWING NUMBER	051-7898 D
		REVISION	C.0.0
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LHL,F/N LABEL,PCB,28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LHL,F/N LABEL,PCB,28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LHL,F/N LABEL,PCB,28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM GROUP	BOM OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROD,SMC_PROD,IR_PROD,WELLSPRING_PROD
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3646	1	PDC,SIGSE,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC,SIGSE,PRQ,2.26,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SL4M,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3756	1	PDC,SIGPU,PRQ,2.53,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC,SIGLA,PRQ,2.66,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710	1	IC,OMCP,MCP79,35X35MM,BGA1437,B03	U1400	CRITICAL	MCP_B03

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0563	1	IC,SMC,MS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2445	1	IC,SMC,K24	U4900	CRITICAL	SMC_PROD
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441	1	IC,PRGM,EFI,BOOTROM,UNLOCK,K24	U6100	CRITICAL	BOOTROM_PROD
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROD
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC,PRGM,WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROD

LOCKED BOOTROM APN IS 341S2443

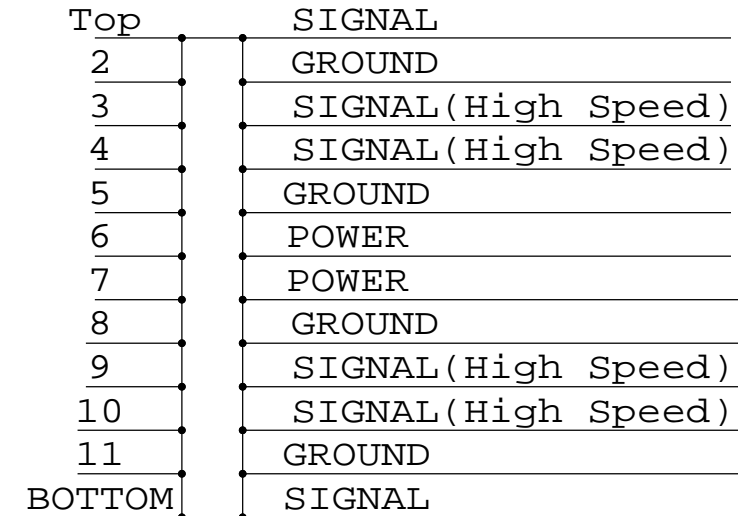
Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYRTEC AS ALTERNATE
152S0796	152S0685		ALL	CYRTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	EMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7930 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERTEL AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K24 BOARD STACK-UP



SYNC MASTER=M97 MLB

BOM Configuration

Apple Inc. 051-7898 D

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Revision History

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SYNC MASTER=M97 MLB	
Revision History	
Apple Inc.	051-7898 D
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Functional Test Points

Fan Connectors

(NEED 3 TP)
TRUE PP5V_S0 603 705
TRUE FAN_RT_PWM 4784
TRUE FAN_RT_TACH 4704
(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

TRUE BI_MIC_LO 5602 5781
TRUE BI_MIC_HI 5602 5781
TRUE BI_MIC_SHIELD 5602 5781

SPEAKER FUNC_TEST

TRUE SPKRAMP_L_N_OUT 5542 5682
TRUE SPKRAMP_L_P_OUT 5582 5682
TRUE SPKRAMP_R_N_OUT 5582 5682
TRUE SPKRAMP_R_P_OUT 5582 5682
TRUE SPKRAMP_SUB_N_OUT 5582 5682
TRUE SPKRAMP_SUB_P_OUT 5582 5682

THERMAL FUNC_TEST

TRUE MCPTHMSNS_D2_P 4685 8003
TRUE MCPTHMSNS_D2_N 4685 8003

LVDS FUNC_TEST

TRUE PP3V3_LCDVDD_SW_F 603 6802
TRUE PP3V3_S0_LCD_F 6803
TRUE PPVOUT_S0_LCDBKLT 603 6882 7101
TRUE LVDS_IG_DDC_CLK 1783 6805
TRUE LVDS_IG_DDC_DATA 1783 6805
TRUE LVDS_IG_A_DATA_N<0> 1783 6802 7583
TRUE LVDS_IG_A_DATA_P<0> 1783 6802 7583
TRUE LVDS_IG_A_DATA_N<1> 1783 6802 7583
TRUE LVDS_IG_A_DATA_P<1> 1783 6802 7583
TRUE LVDS_IG_A_DATA_N<2> 1783 6802 7583
TRUE LVDS_IG_A_DATA_P<2> 1783 6802 7583
TRUE LVDS_IG_A_CLK_F_N 6802 7583
TRUE LVDS_IG_A_CLK_F_P 6802 7583
TRUE LED_RETURN_1 6883 7181
TRUE LED_RETURN_2 6883 7181
TRUE LED_RETURN_3 6883 7181
TRUE LED_RETURN_4 6883 7181
TRUE LED_RETURN_5 6883 7181
TRUE LED_RETURN_6 6883 7181
TRUE TP_BKL_SYNC 6802
(NEED TO ADD 5 GND TP)

SATA ODD CONN

TRUE PP5V_SW_ODD (NEED 4 TP) 603 3703
TRUE SMC_ODD_DETECT 3707 4088
TRUE SATA_ODD_D2R_C_P 3706 75A3
TRUE SATA_ODD_D2R_C_N 3706 75A3
TRUE SATA_ODD_R2D_P 3706 75A3
TRUE SATA_ODD_R2D_N 6A7 3706 75A3
(NEED TO ADD 4 GND TP)

SATA HDD/IR/SIL

(NEED 4 TP)
TRUE PP5V_S0_HDD_FLT 603 3786
TRUE SATA_HDD_R2D_P 37A5 75A3
TRUE SATA_HDD_R2D_N 37A5 75A3
TRUE SATA_HDD_D2R_C_P 37B5 75A3
TRUE SATA_HDD_D2R_C_N 37B5 75A3
TRUE SYS_LED_ANODE_R 37A7
TRUE IR_RX_OUT 37A7 3904
TRUE PP5V_S3_IR_R 37A7
(NEED TO ADD 4 GND TP)

BATT POWER CONN

TRUE SMBUS_SMC_BSA_SCL 6A7 4305 7903
TRUE SMBUS_SMC_BSA_SDA 4305 7903
TRUE SYS_DETECT_L 58A4
TRUE BATT_POS_F (NEED 3 TP) 58A7 5888 59A3
(NEED TO ADD 3 GND TP)

BATT SIGNAL CONN

(NEED 3 TP)
TRUE PP3V42_G3H 685 603 701
TRUE SMBUS_SMC_BSA_SCL 6A7 4305 7903
TRUE SMBUS_SMC_BSA_SCL 6A7 4305 7903
TRUE SMC_BIL_BUTTON_L 4005 5804
TRUE SMC_LID_R 5802
(NEED TO ADD 5 GND TP)

RIGHT CLUTCH CONN

TRUE PP5V_S3_BTCAMERA_F 2907
TRUE PCIE_MINI_D2R_P 1886 2907 75D3
TRUE PCIE_MINI_D2R_N 1886 2907 75D3
TRUE PCIE_MINI_R2D_P 2907 75D3
TRUE PCIE_MINI_R2D_N 2907 75D3
TRUE PCIE_CLK100M_MINI_CONN_P 2907 75D3
TRUE PCIE_CLK100M_MINI_CONN_N 2907 75D3
TRUE USB_CAMERA_CONN_P 2987 7603
TRUE USB_CAMERA_CONN_N 2987 7603
TRUE PP5V_WLAN 603 (NEED 2 TP)
TRUE PCIE_WAKE_L 1886 2907
TRUE SMBUS_SMC_A_S3_SCL 605 4302 7903
TRUE SMBUS_SMC_A_S3_SDA 605 4302 7903
TRUE CONN_USB2_BT_P 2987 7603
TRUE CONN_USB2_BT_N 2987 76A3
TRUE MINI_CLKREQ_O_L 2907
TRUE MINI_RESET_CONN_L 29A7
(NEED TO ADD 6 GND TP)

IPD_FLEX CONN

TRUE PP3V3_S3_LDO 603 4984 4903
TRUE PP18V5_S3 603 4901 4903
TRUE Z2_CS_L 4808 4903
TRUE Z2_DEBUG3 4808 4903
TRUE Z2_MOS1 4808 4903
TRUE Z2_MISO 4808 4903
TRUE Z2_SCLK 4808 4903
TRUE Z2_BOOST_EN 4903 4905
TRUE Z2_HOST_INTN 4808 4903
TRUE Z2_CLKIN 4806 4903
TRUE Z2_KEY_ACT_L 4808 4901
TRUE Z2_RESET 4808 4901
TRUE PSOC_MISO 4808 4901
TRUE PSOC_MOSI 4808 4901
TRUE PSOC_SCLK 4808 4901
TRUE SMBUS_SMC_A_S3_SDA 605 4302 7903
TRUE SMBUS_SMC_A_S3_SCL 605 4302 7903
TRUE PSOC_F_CS_L 4808 4901
TRUE PICKB_L 4806 4901

KEYBOARD CONN

TRUE PP3V3_S3 603 703
TRUE PP3V42_G3H 6A7 603 701
TRUE WS_KBD1 4806 4802
TRUE WS_KBD2 4806 4802
TRUE WS_KBD3 4806 4802
TRUE WS_KBD4 4806 4802
TRUE WS_KBD5 4806 4802
TRUE WS_KBD6 4806 4802
TRUE WS_KBD7 4806 4802
TRUE WS_KBD8 4806 4802
TRUE WS_KBD9 4806 4802
TRUE WS_KBD10 4806 4802
TRUE WS_KBD11 4806 4802
TRUE WS_KBD12 4806 4802
TRUE WS_KBD13 4806 4802
TRUE WS_KBD14 4806 4802
TRUE WS_KBD15_CAP 4802 4806
TRUE WS_KBD16_NUM 4802
TRUE WS_KBD17 4802 4806
TRUE WS_KBD18 4802 4807
TRUE WS_KBD19 4802 4807
TRUE WS_KBD20 4802 4807
TRUE WS_KBD21 4802 4807
TRUE WS_KBD22 4802 4807
TRUE WS_KBD23 4802 4807
TRUE WS_KBD_ONOFF_L 4802
TRUE WS_LEFT_SHIFT_KBD 4883 4885 4802
TRUE WS_LEFT_OPTION_KBD 4883 4885 4802
TRUE WS_CONTROL_KBD 4883 4885 4802
(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

TRUE KBDLED_ANODE (NEED 2 TP) 49A4
TRUE SMC_KDBLED_PRESENT_L 49A4 49A6
(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

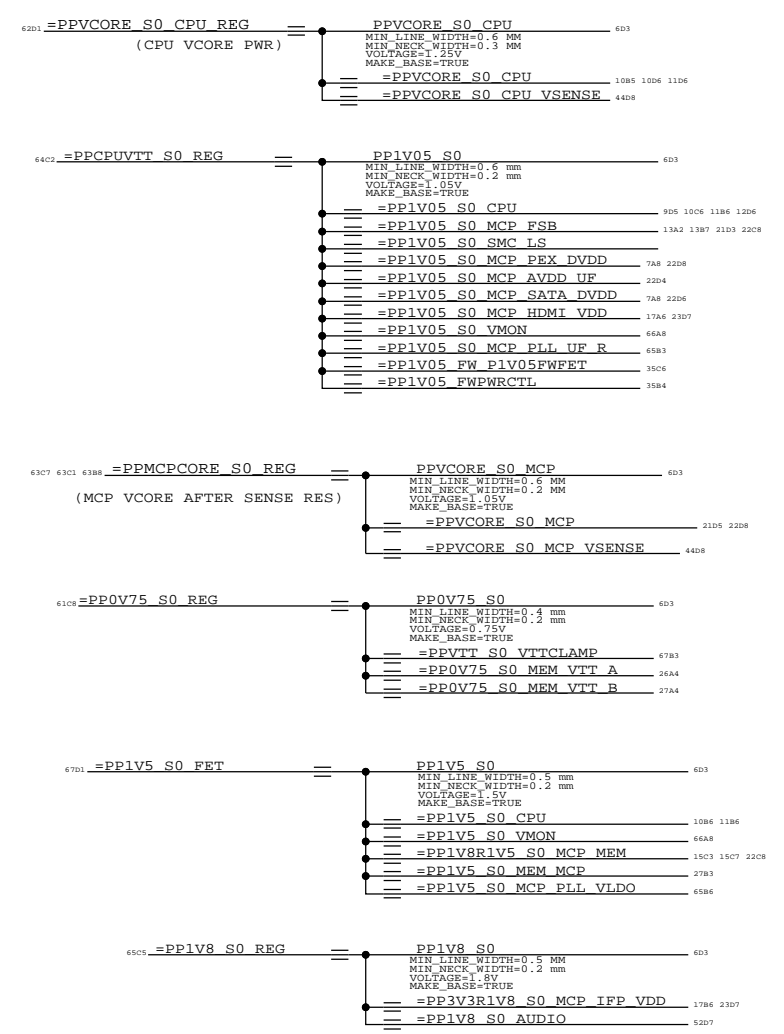
TRUE PPVCORE_S0_CPU 707
TRUE PPVCORE_S0_MCP 707
TRUE PP0V75_S0 707
TRUE PP1V05_S0 707
TRUE PP1V5_S0 706
TRUE PP1V8_S0 706
TRUE PP5V_S0 607 705
TRUE PP3V3_S0 705
TRUE PP1V5_S3 703
TRUE PP3V3_S3 685 703
TRUE PP5V_S3 703
TRUE PP1V1R1V05_S5 783
TRUE PP3V3_S5 783
TRUE PP3V42_G3H 6A7 685 701
TRUE PPBUS_G3H 701
TRUE PP3V3_ENET_PHY 785
TRUE PP1V2R1V05_ENET 785
TRUE PP3V3_G3_RTC 2008 21A5 24D4
TRUE PP5V_WLAN 605 2905
TRUE PP5V_SW_ODD 687 37D3
TRUE PP5V_S0_HDD_FLT 687 3786
TRUE PP3V3_S5_AVREF_SMC 4004 4106
TRUE PP18V5_S3 605 4901 4903
TRUE PP3V3_S3_LDO 605 4984 4903
TRUE PP3V3_LCDVDD_SW_F 607 6802
TRUE PPVOUT_S0_LCDBKLT 607 6882 7101
TRUE PP4V5_AUDIO_ANALOG 42A5 6205 6207
TRUE SMC_PM_G2_EN 4005 6205 6208
TRUE PM_SLP_S4_L 2003 4005 41A2 6608
TRUE PM_SLP_S3_L 2003 32A7 35A5 4005 6605 7008
(NEED TO ADD 4 GND TP)

DC POWER CONN

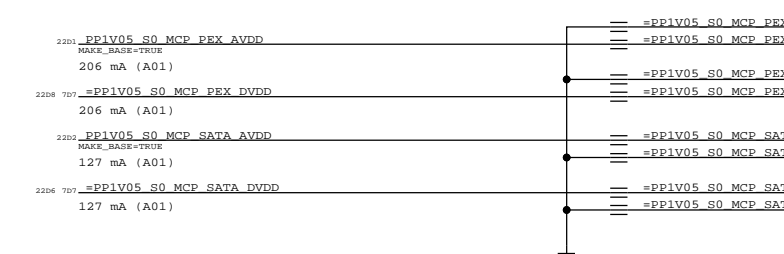
TRUE PP18V5_DCIN_FUSE (NEED 3 TP) 5806
TRUE ADAPTER_SENSE 5807
(NEED TO ADD 4 GND TP)

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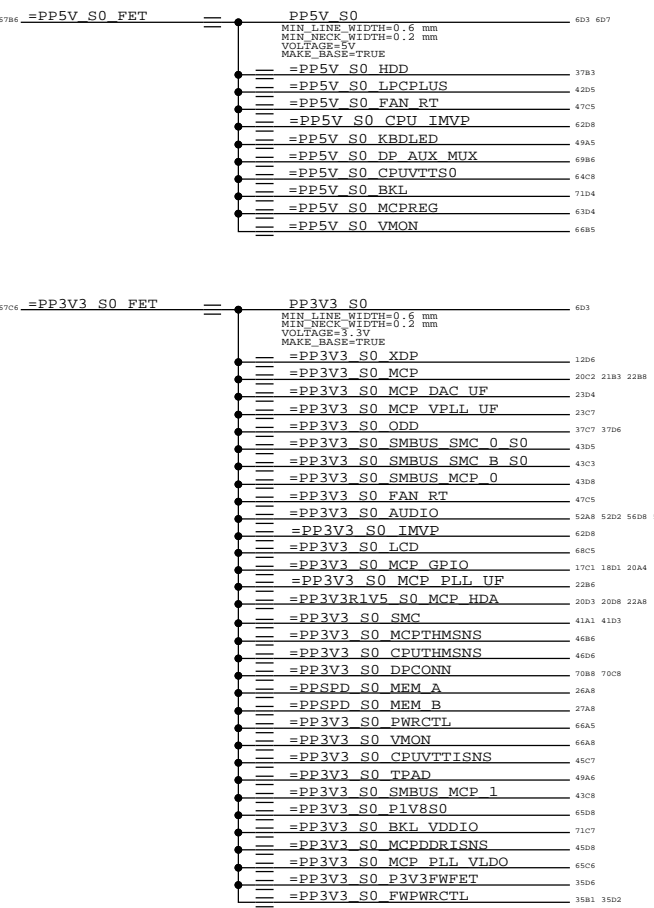
"S0,S0M" RAILS



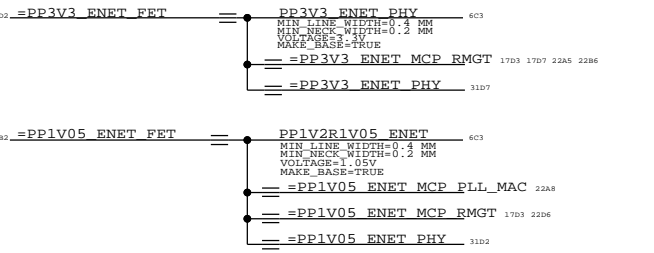
PEX & SATA AVDD/DVDD aliases



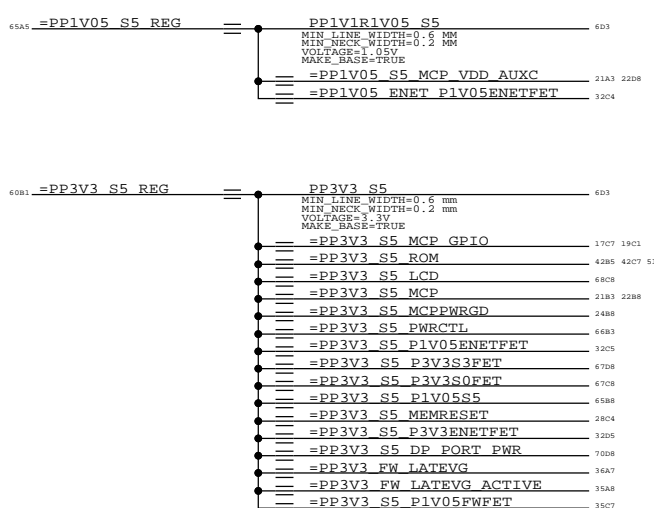
"S3" RAILS



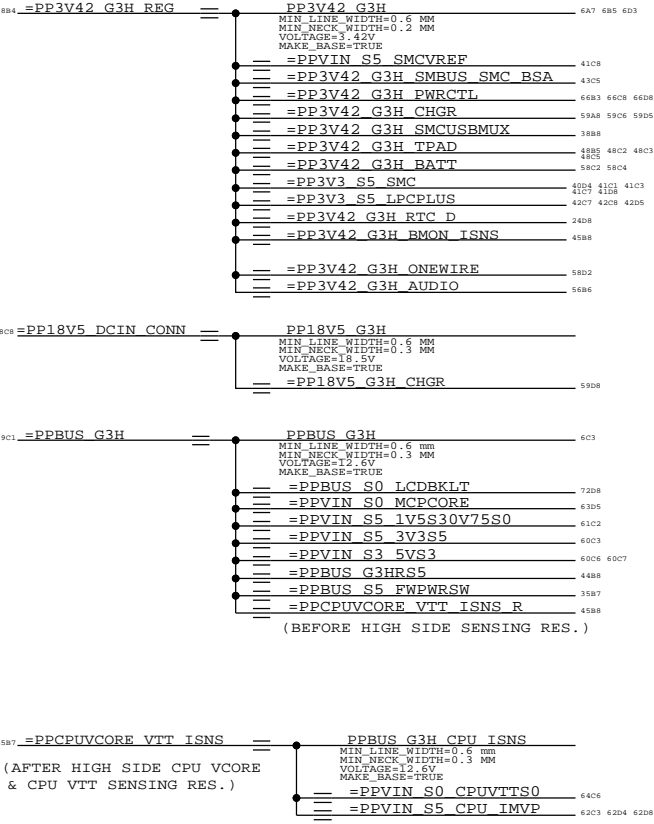
"ENET" RAILS



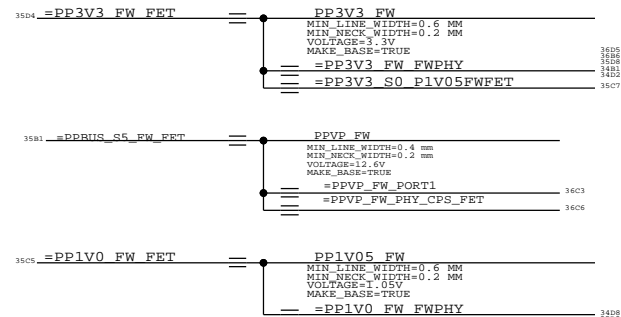
"S5" RAILS



"G3H" RAILS



"FIREWIRE" RAILS



SYNC MASTER=BEN SYNC DATE=04/21/2008

Power Aliases

Apple Inc.

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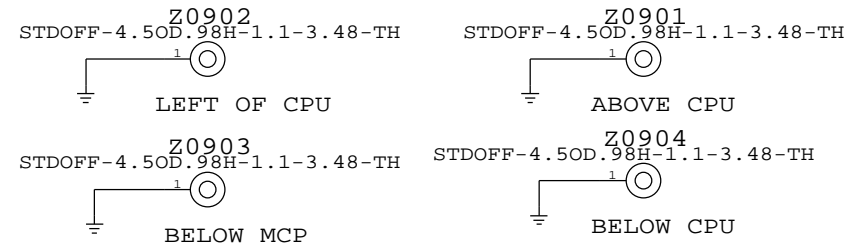
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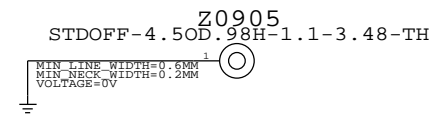
2

1

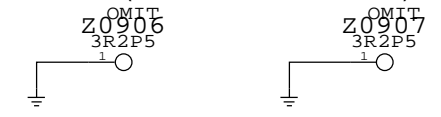
HEATSINK STANDOFFS



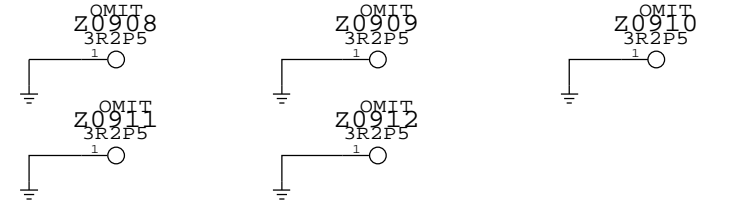
FAN STANDOFF



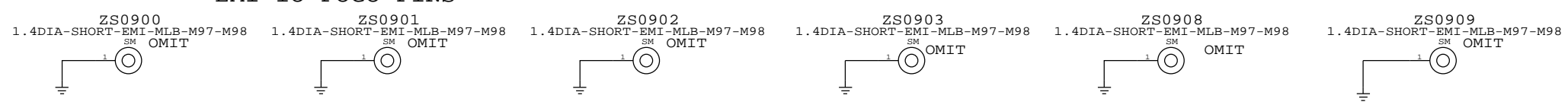
MLB MOUNTING (TO C. BRACKET) SCREW HOLES



MLB MOUNTING (TO TOPCASE) SCREW HOLES

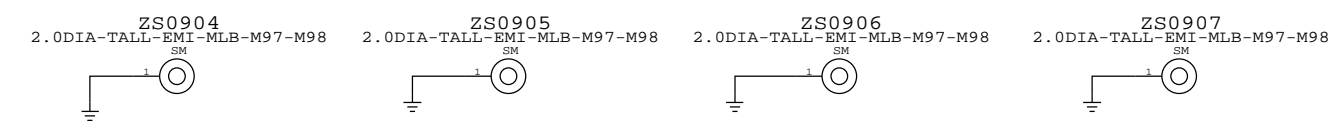


EMI IO POGO PINS

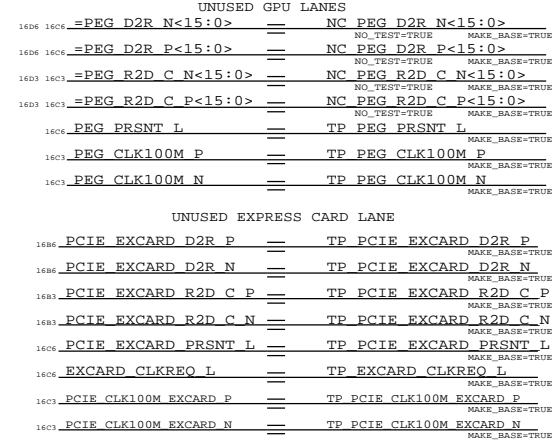


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
870-1801	6	POGO PIN, SHORT, EMI, MLB, K19/K24	88990, 88991, 88992, 88993, 88994, 88995	CRITICAL	

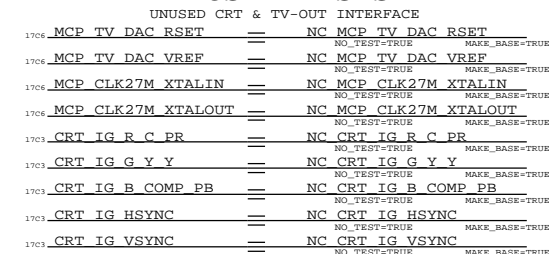
EMI POGO PINS



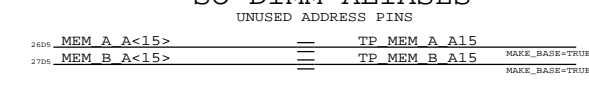
PCI-E ALIASES



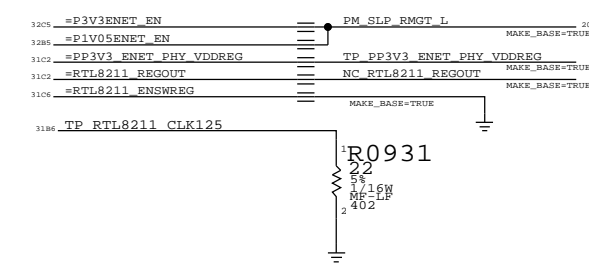
DACS ALIASES



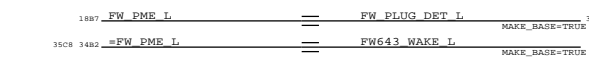
SO-DIMM ALIASES



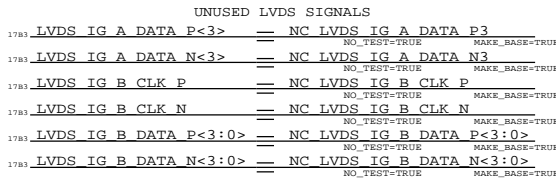
ETHERNET ALIASES



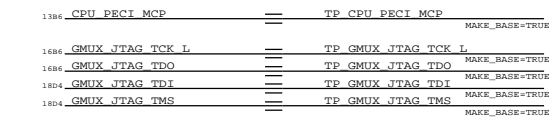
FW ALIASES



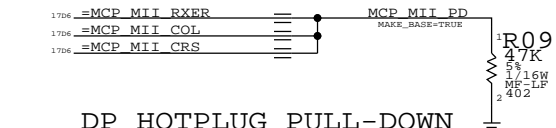
LVDS ALIASES



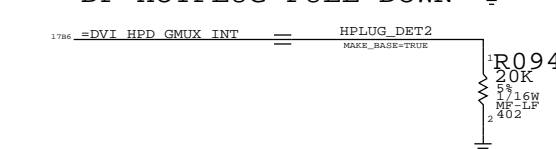
MISC MCP79 ALIASES



LAN ALIASES



DP HOTPLUG PULL-DOWN



CPU FSB FREQUENCY STRAPS



SYNC MASTER=M97_MLB

PAGE TITLE

SIGNAL ALIAS

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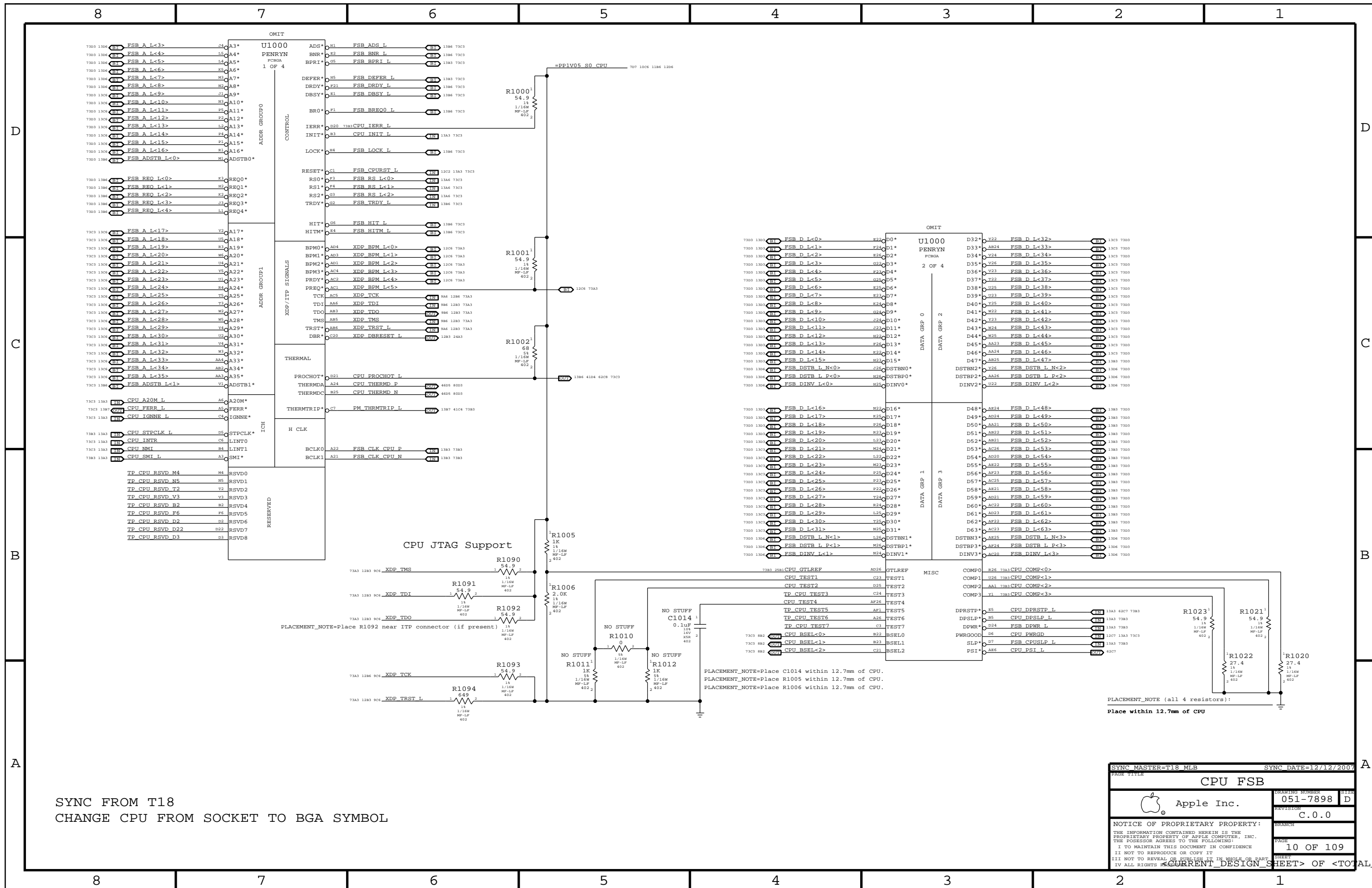
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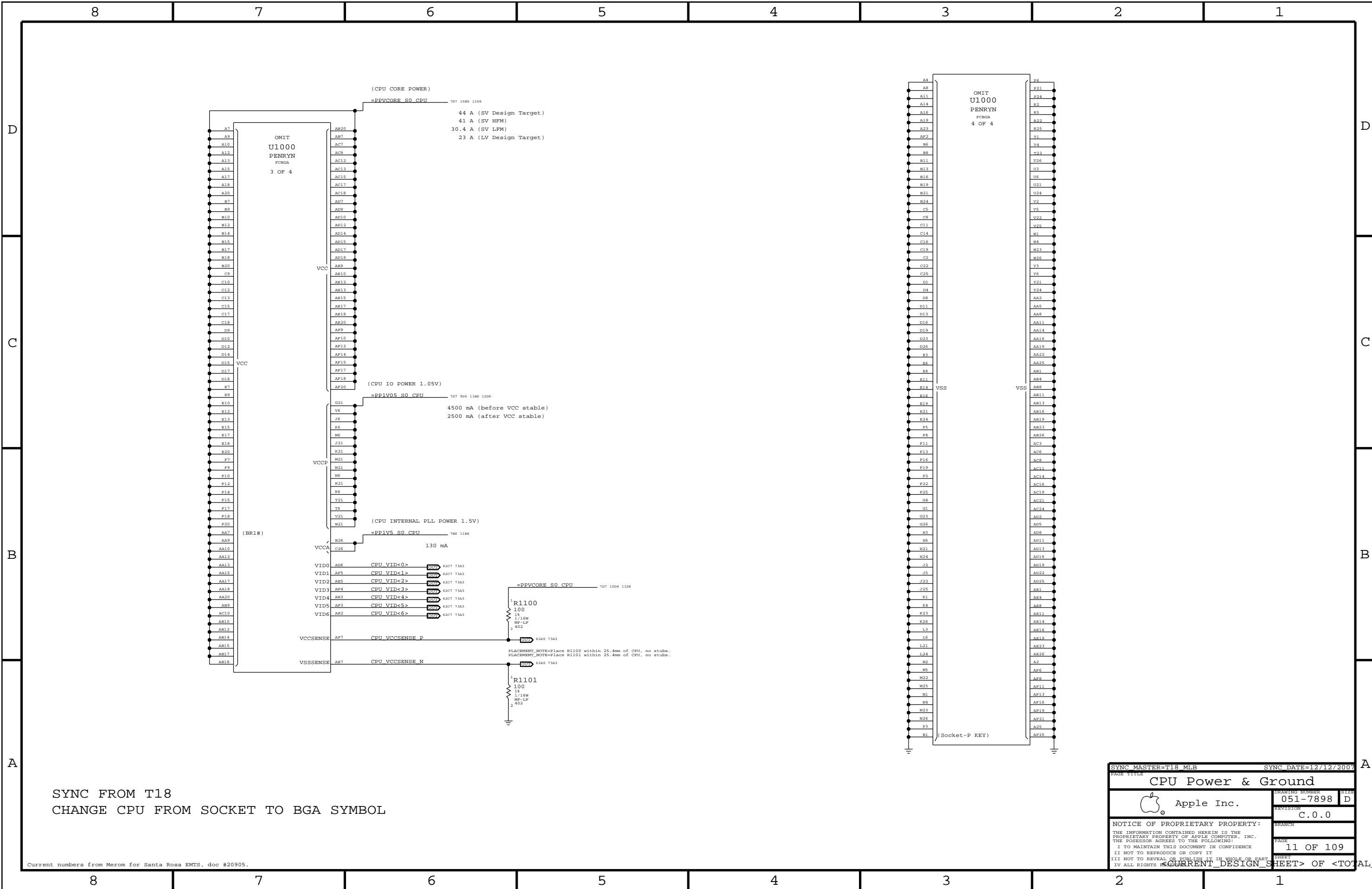


SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=T18 MLB SYNC DATE=12/12/2007

CPU FSB	
Apple Inc.	DRAWING NUMBER 051-7898
REVISION C.0.0	
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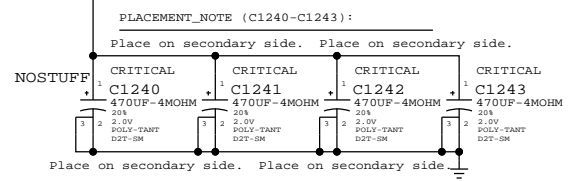
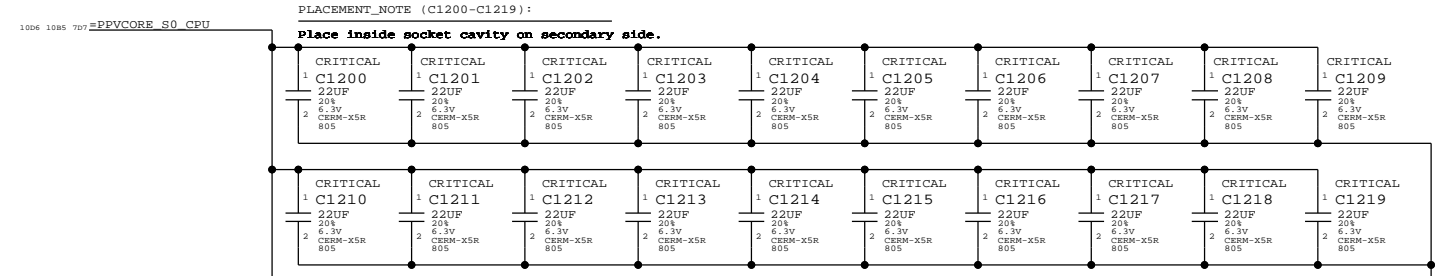
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC MASTER=T18 MLB		SYNC DATE=12/12/2007	
CPU Power & Ground			
Apple Inc.		051-7898	D
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Current numbers from Merom for Santa Rosa EMTS, doc #20905.

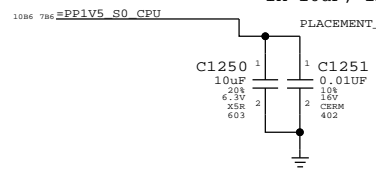
CPU VCore HF and Bulk Decoupling

4X 330UF, 20X 22UF 0805



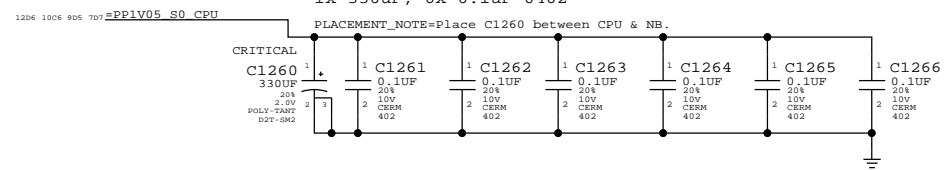
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



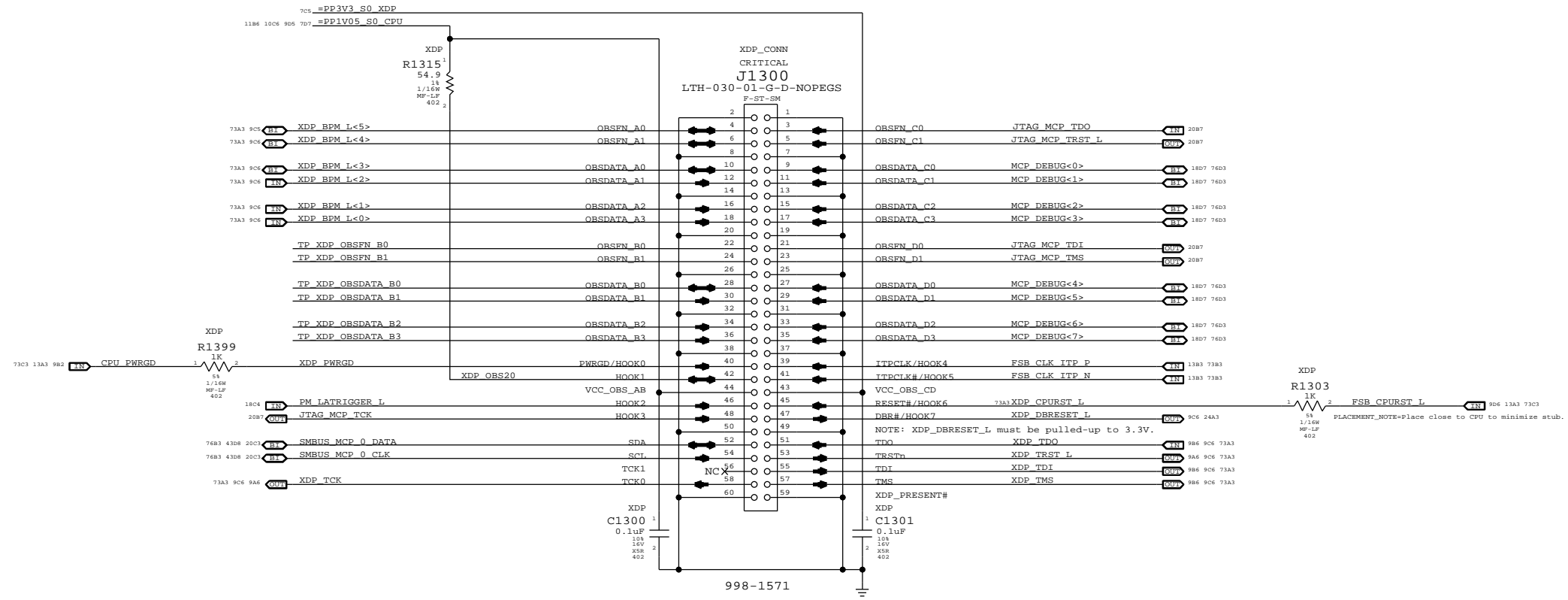
SYNC FROM T18
 REMOVE NO STUFF CAPS C1220 TO C1231
 REMOVE C1244 & C1245
 CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC MASTER=RAYMOND		SYNC DATE=03/31/2008	
CPU Decoupling			
Apple Inc.		051-7898	D
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Mini-XDP Connector

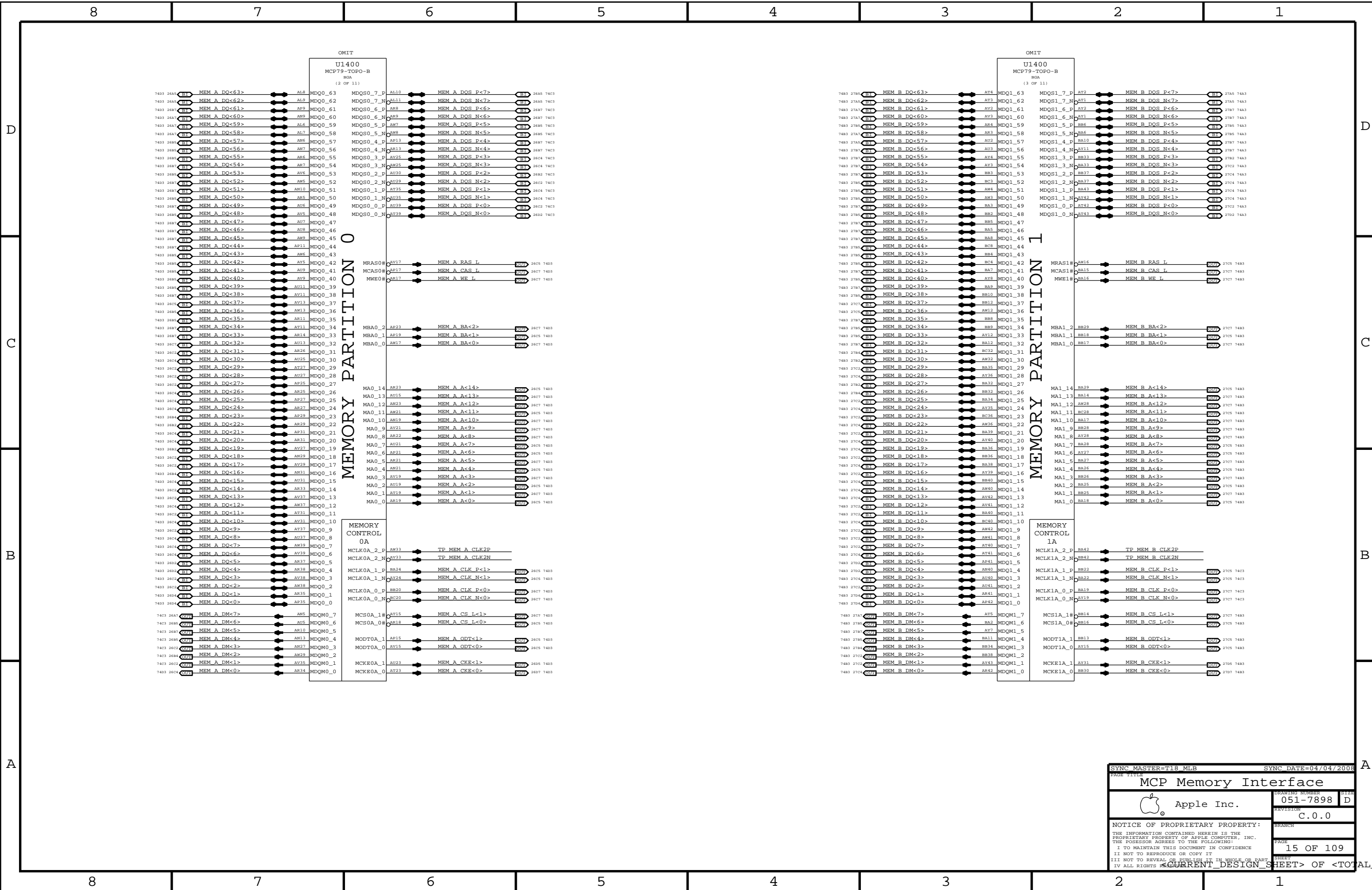
NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



← Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

SYNC MASTER=K19 MLB		SYNC DATE=11/07/2008	
PAGE TITLE eXtended Debug Port (MiniXDP)			
DRAWING NUMBER 051-7898		REVISION D	
DRAWING NUMBER 051-7898		REVISION C.0.0	
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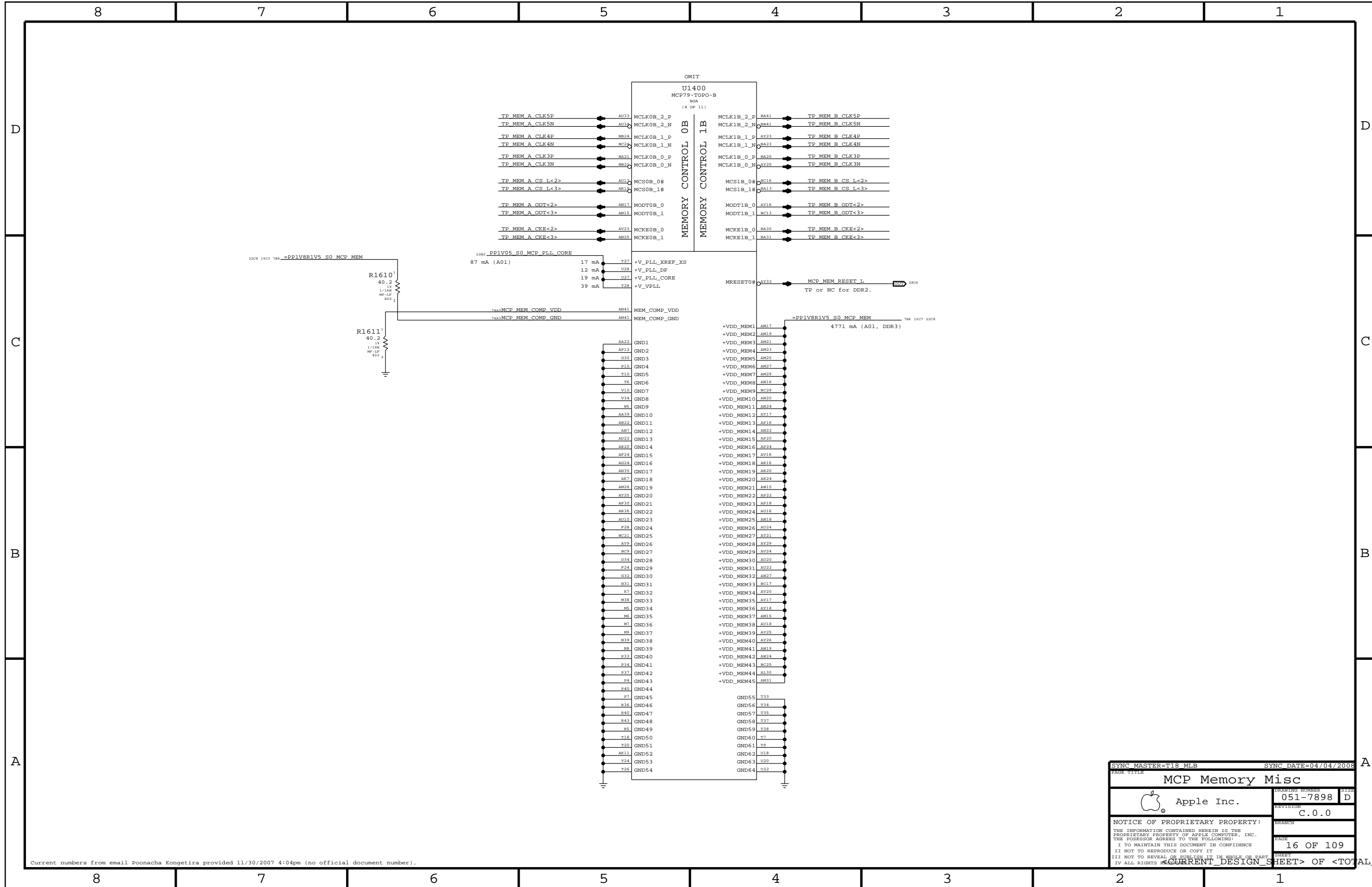


SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

MCP Memory Interface

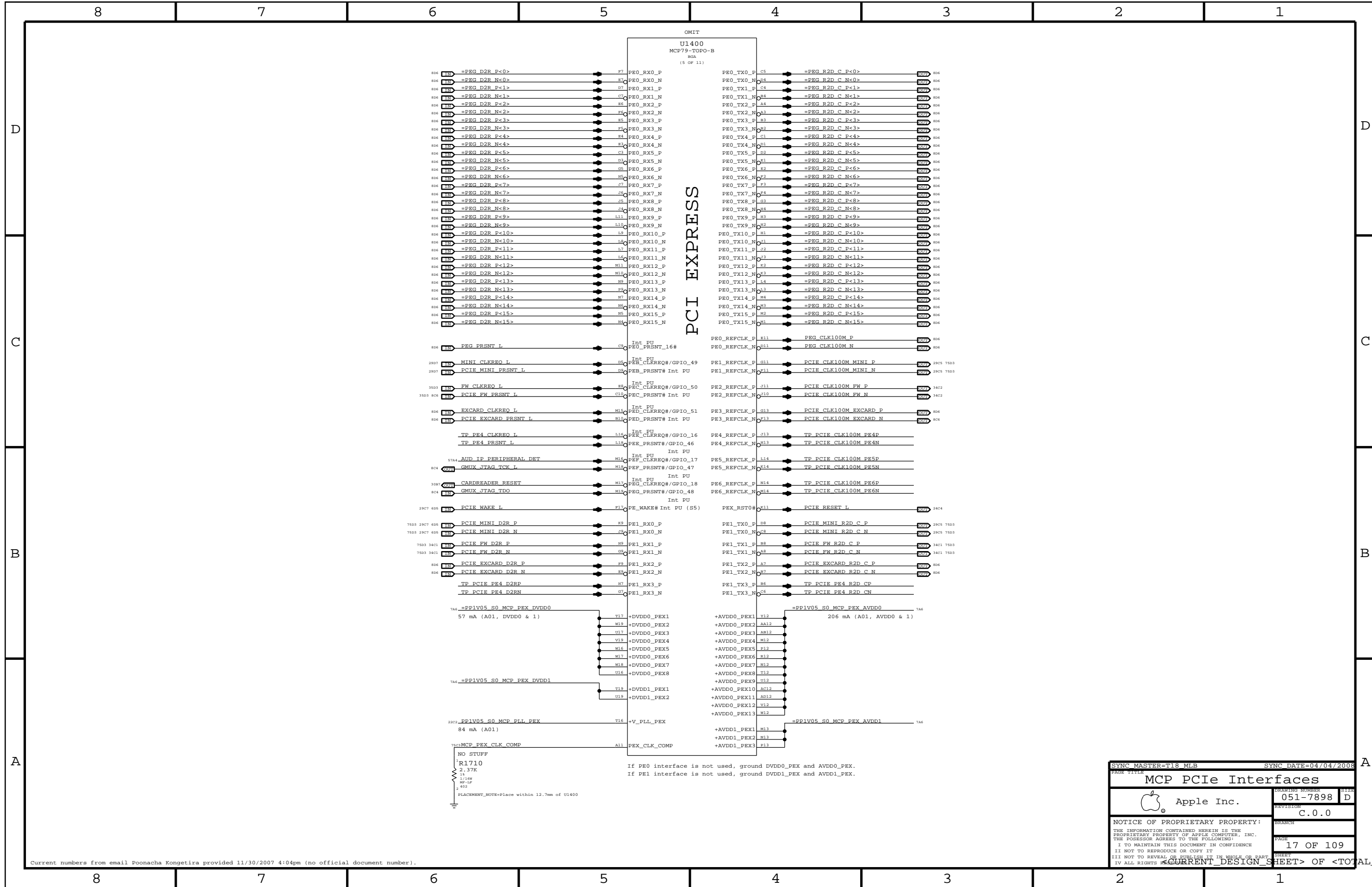
Apple Inc.
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 REVISION: C.0.0

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PAGE TITLE			
MCP Memory Misc			
		DRAWING NUMBER 051-7898	SHEET D
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SYNC MASTER=T18 MLB		SYNC DATE=04/04/2008	
MCP PCIe Interfaces			
Apple Inc.		DRAWING NUMBER	051-7898 D
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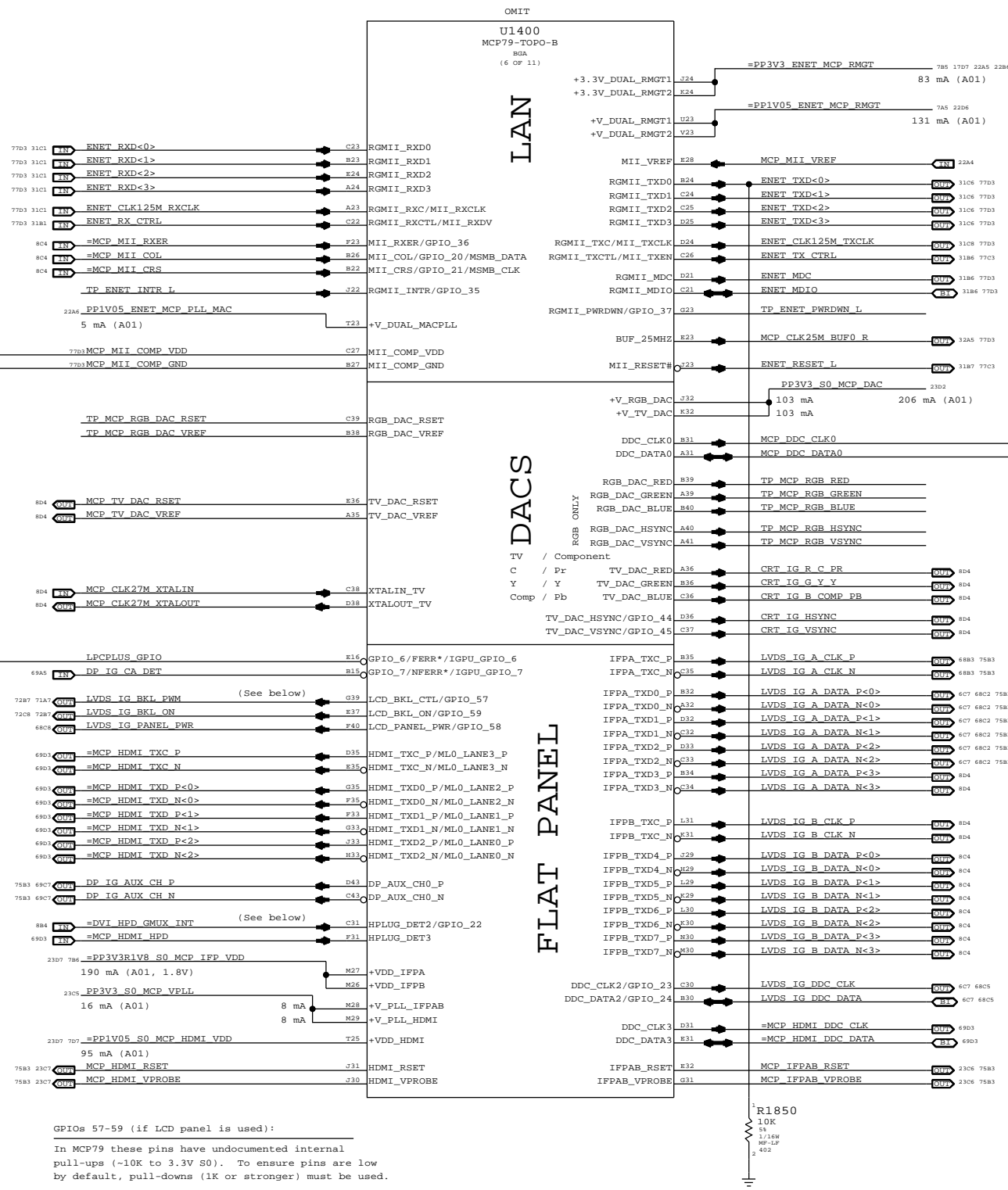
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Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
 Okay to float all TV_DAC signals.
 Okay to float XTALIN_TV and XTALOUT_TV.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
 NOTE: 20K pull-down required on DP_HPD_DET.
 NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
 Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):
 In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
 Alias to DVI_HPD for systems using IFP for DVI.
 Alias to GMUX_INT for systems with GMUX.
 Alias to HPLUG_DET2 for other systems.
 Pull-down (20k) required in all cases.

SYNC MASTER=T18 MLB SYNC DATE=04/04/2008

MCP Ethernet & Graphics

Apple Inc.

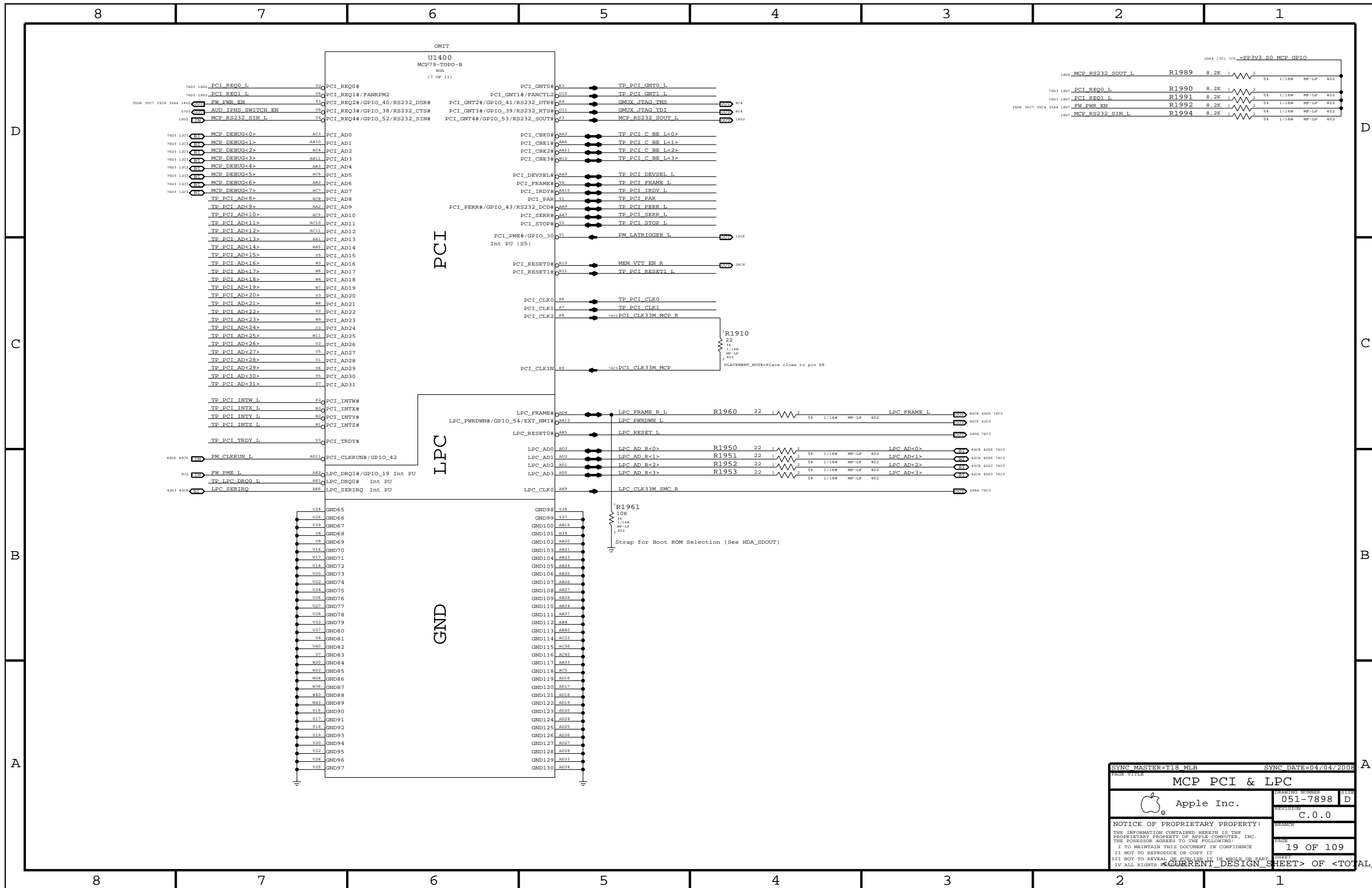
051-7898 D

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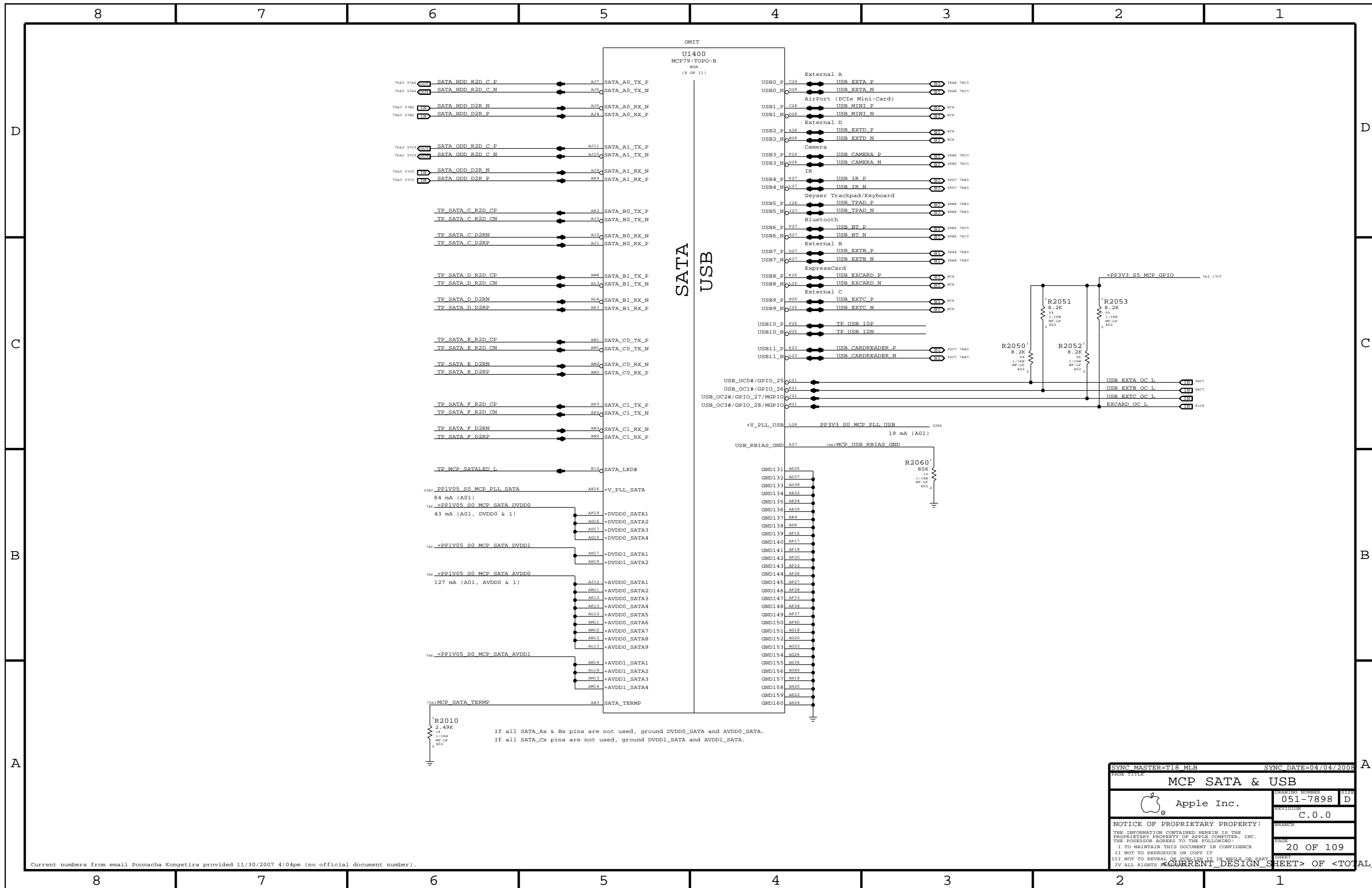
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MCP PCI & LPC			
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MCP SATA & USB			
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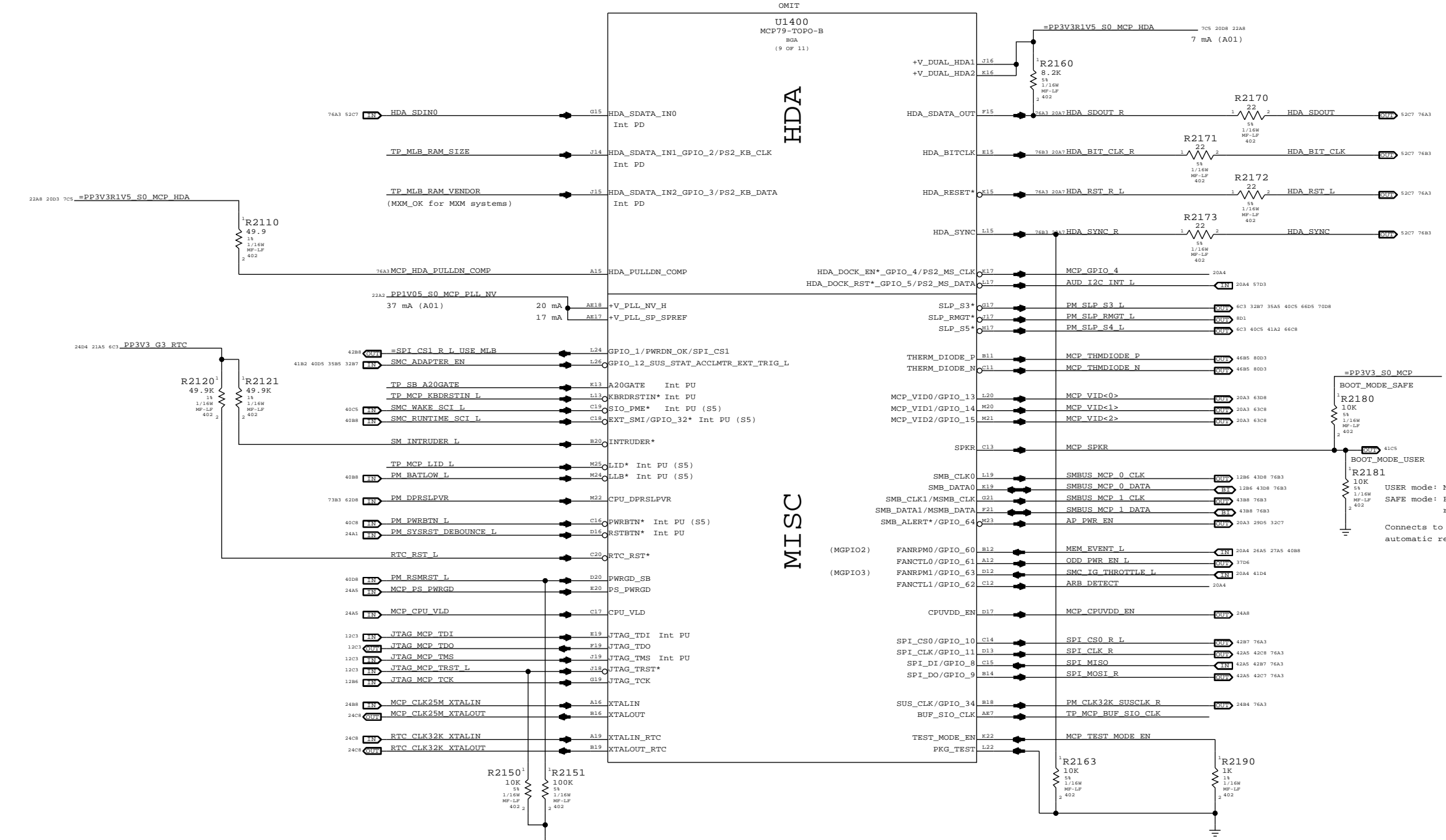
B

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U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

MISC



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

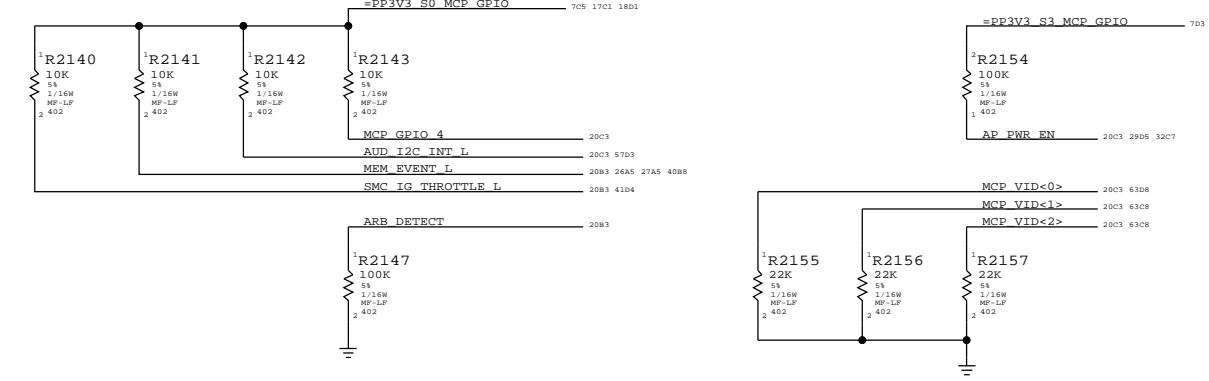
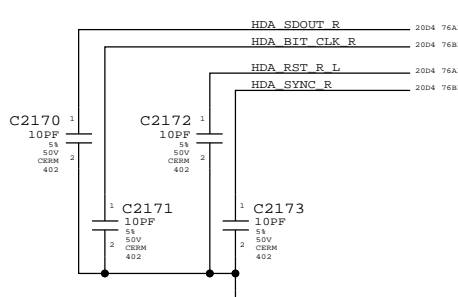
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



SYNC MASTER=T18_MLB SYNC DATE=06/26/2008

MCP HDA & MISC

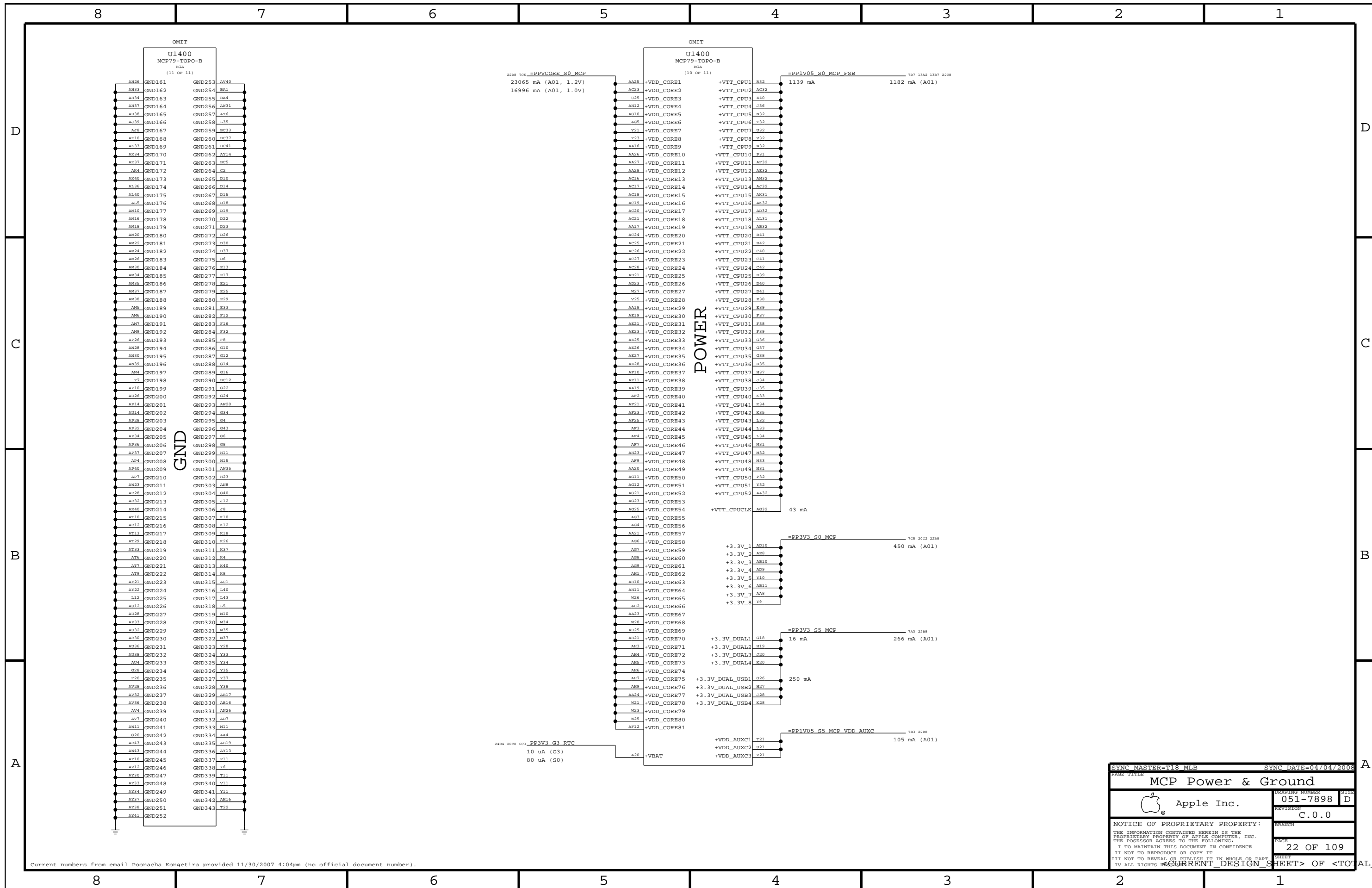
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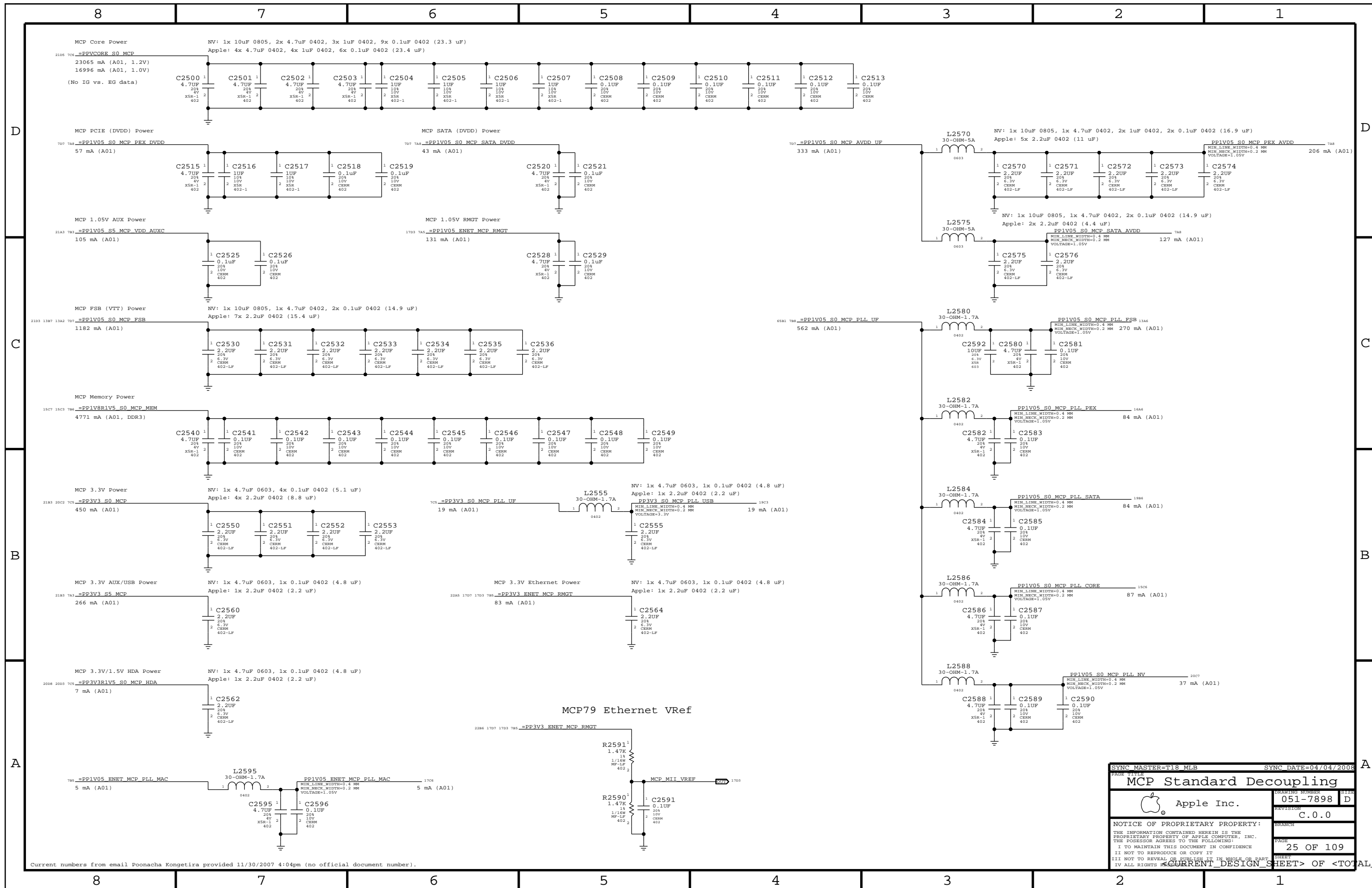
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MCP Standard Decoupling					
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		REVISION	C.0.0		
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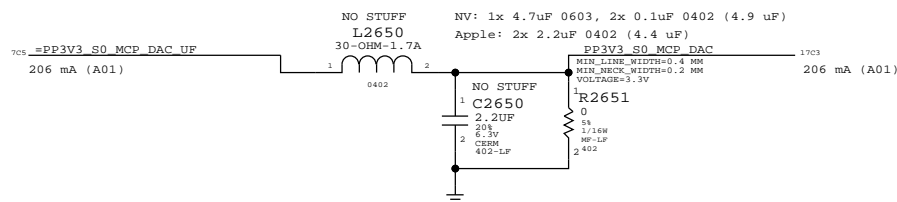
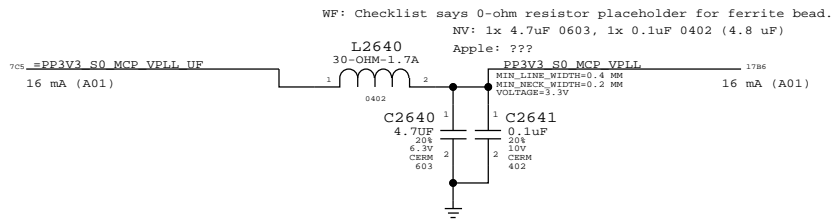
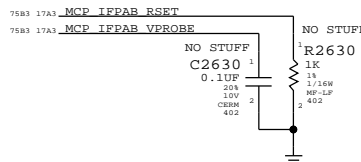
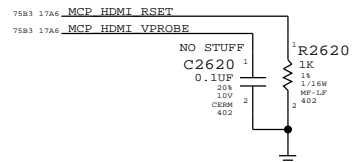
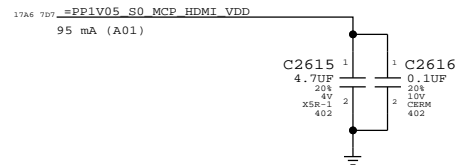
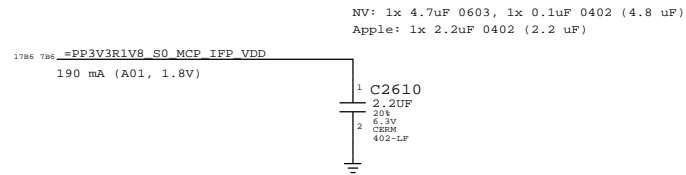
D

C

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WF: Checklist says 0-ohm resistor placeholder for ferrite bead.



D

C

B

A

SYNC FROM T18
 REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
 REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
 NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
 CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
 REMOVE HDCP ROMS

SYNC MASTER=T18 MLB		SYNC DATE=12/12/2007	
MCP Graphics Support			
Apple Inc.		051-7898	D
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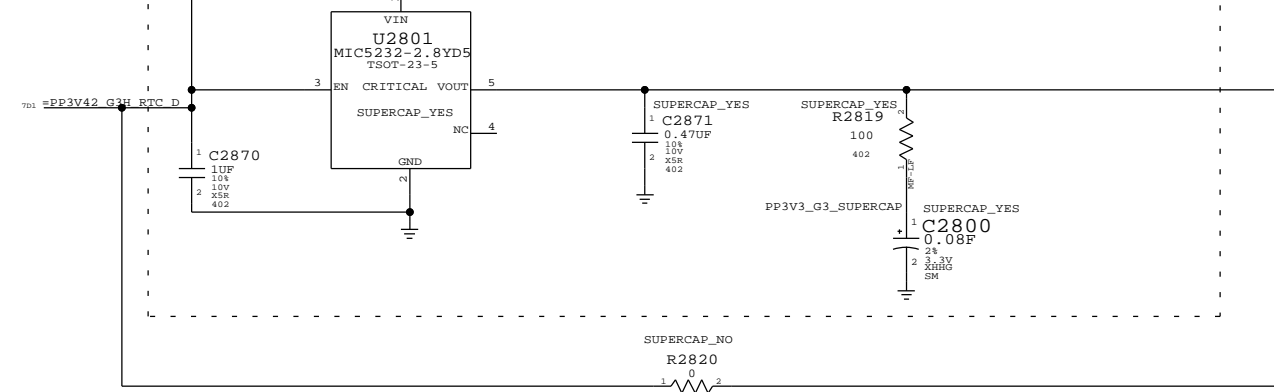
4

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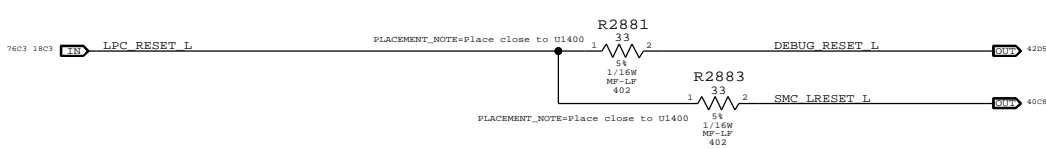
1

RTC Power Sources

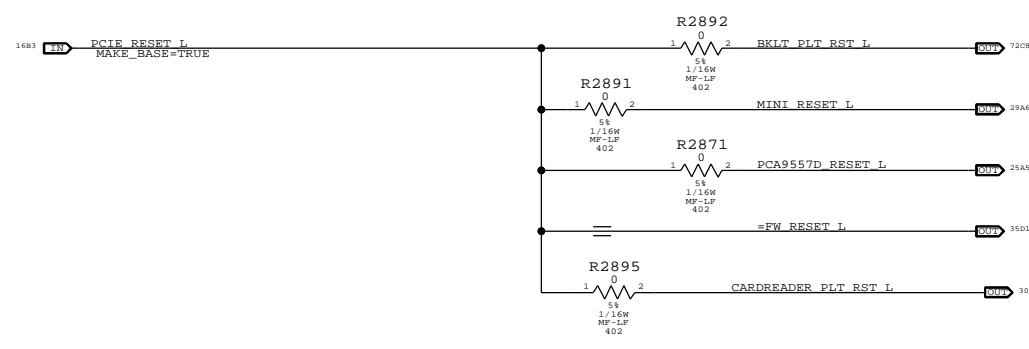


Platform Reset Connections

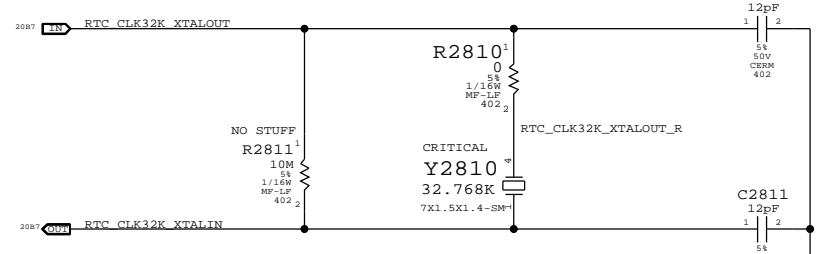
LPC Reset (Unbuffered)



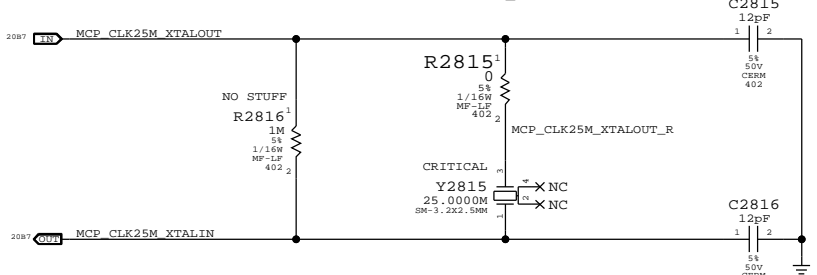
PCIE Reset (Unbuffered)



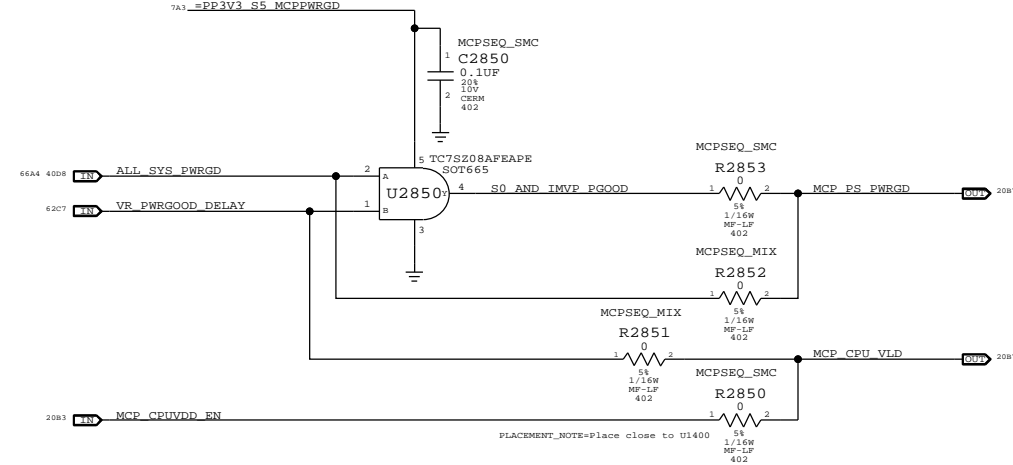
RTC Crystal



MCP 25MHz Crystal



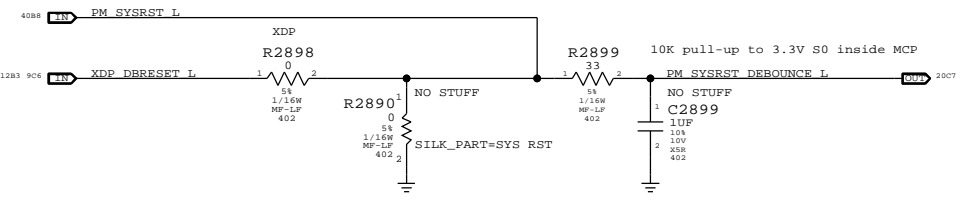
MCP S0 PWRGD & CPU_VLD



PP3V3_G3_RTC 6C3 20C8 21A5
 MIN_LINK_WIDTH=0.3 mm
 MIN_BACK_WIDTH=0.2 mm
 VOLTAGE=3.3V

PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79
 PLACE C2819 CLOSE TO MCP79
 PLACE C2800 AT COOLEST SPOT ON MLB

Reset Button



SYNC FROM T18
 CHANGE RESET BUTTON TO RESET PADS
 REMOVE UNUSED PCIE RESET SIGNALS
 REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
 CHANGE RTC COIN CELL TO LDO & SUPERCAP
 ALIAS MEM_VTT_EN TO =DDRVTT_EN
 CHANGE Y2810 AND U2850 TO SMALLER PARTS

SYNC MASTER=RAYMOND SYNC DATE=04/05/2008
 PAGE TITLE SB Misc

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Page Notes

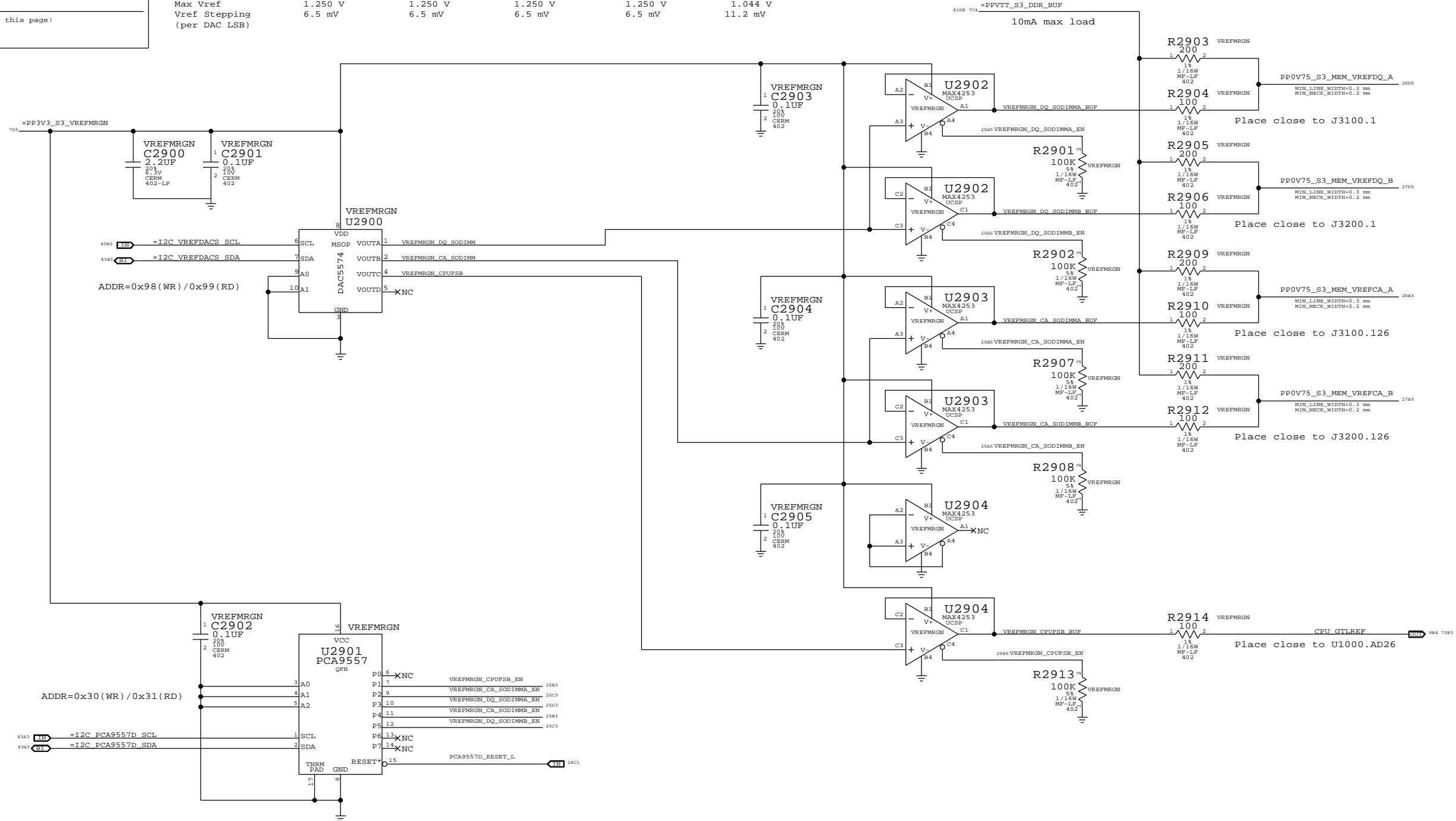
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN
 NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC MASTER=BEN SYNC DATE=03/31/2008

FSB/DDR3 Vref Margining

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 CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

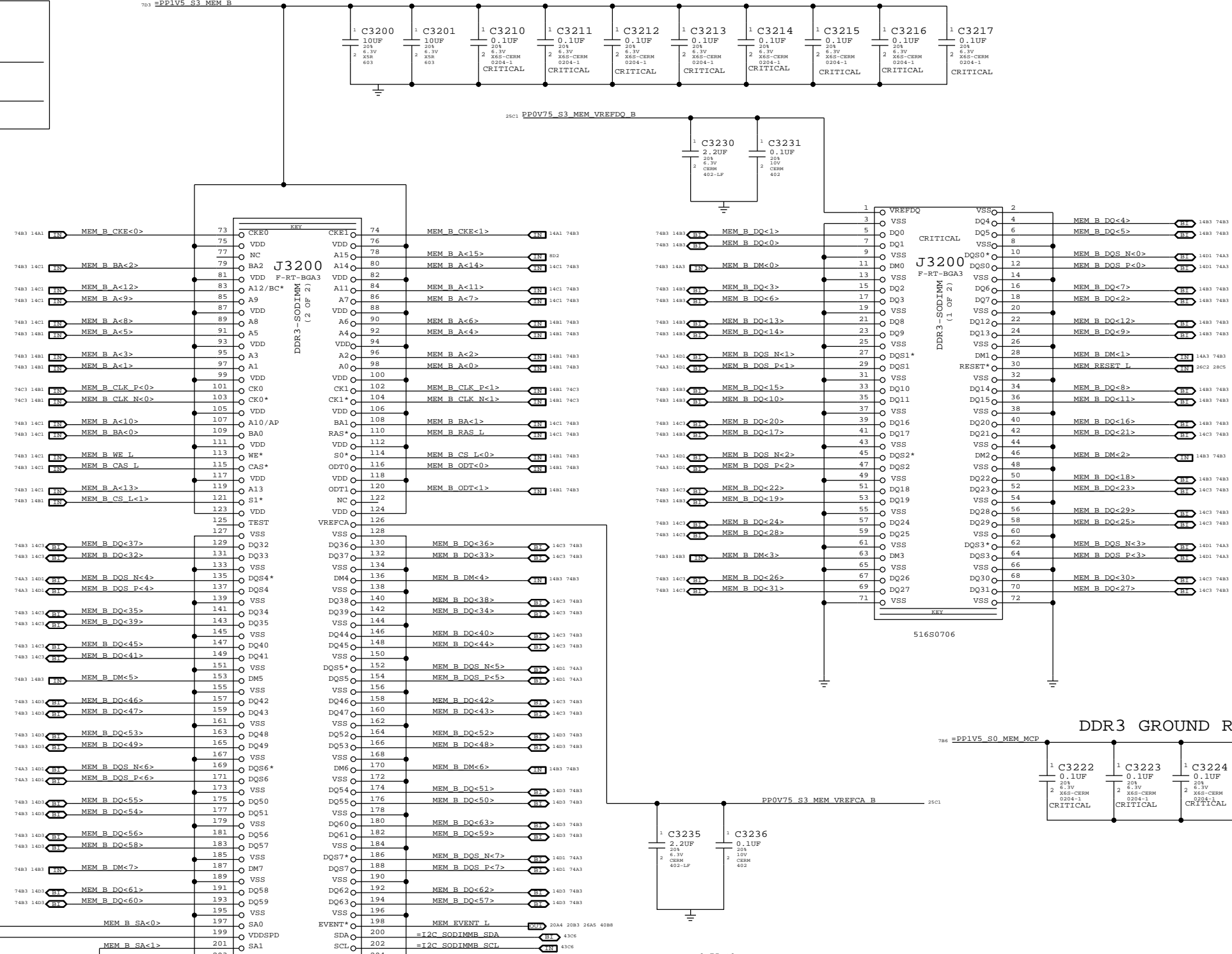
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_B
 - =PP1V5_S3_MEM_B
 - =PP0V75_S0_MEM_VTT_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)

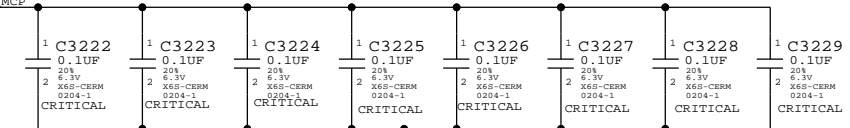
Signal aliases required by this page:
 - =I2C_S0DIMMB_SCL
 - =I2C_S0DIMMB_SDA

ROM options provided by this page:
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 GROUND RETURN CAPS (MCP SIDE)



"Expansion" (bottom) slot

SYNC MASTER=BEN SYNC DATE=05/09/2008

DDR3 SO-DIMM Connector B

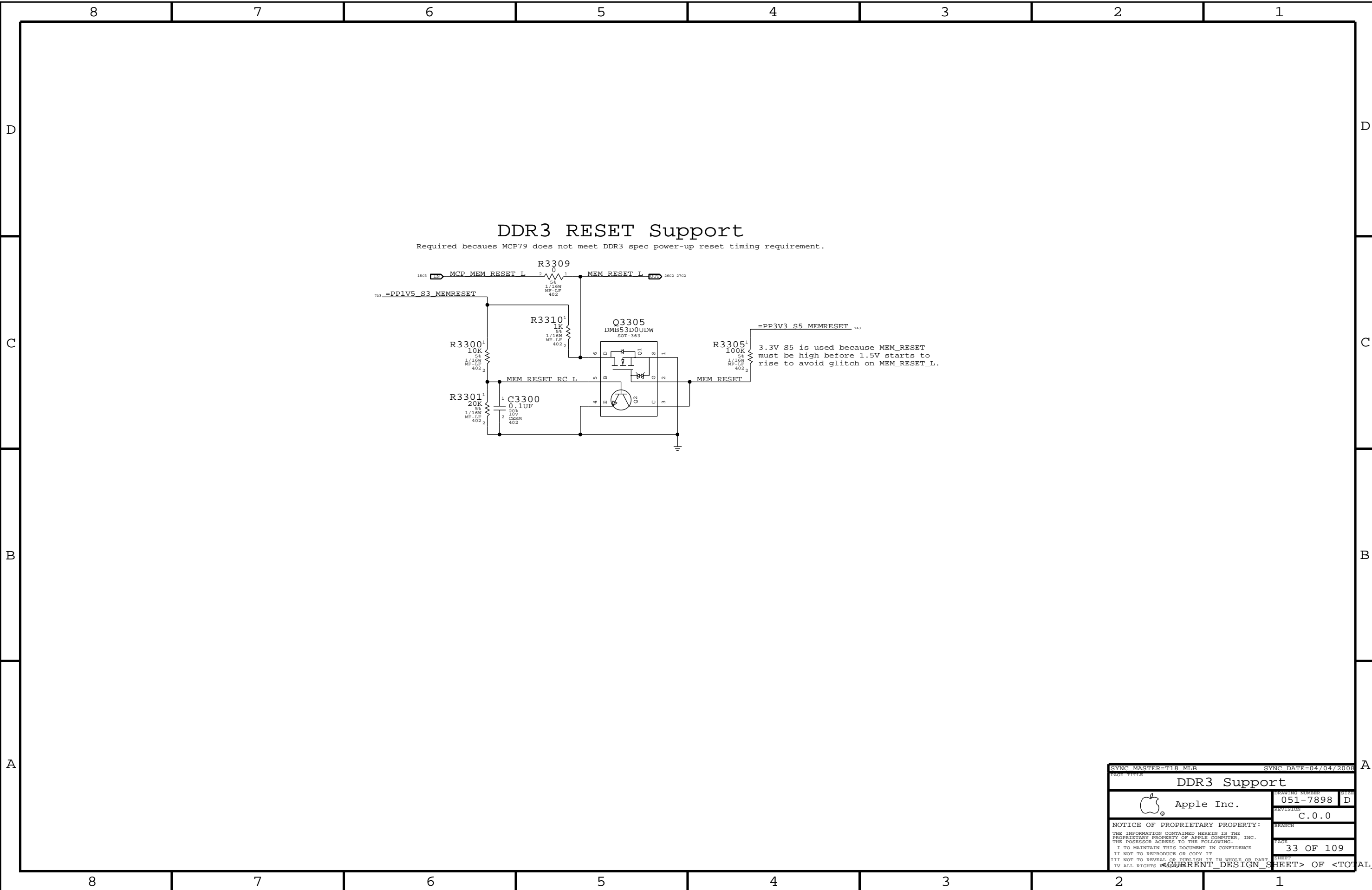
Apple Inc.

051-7898 D

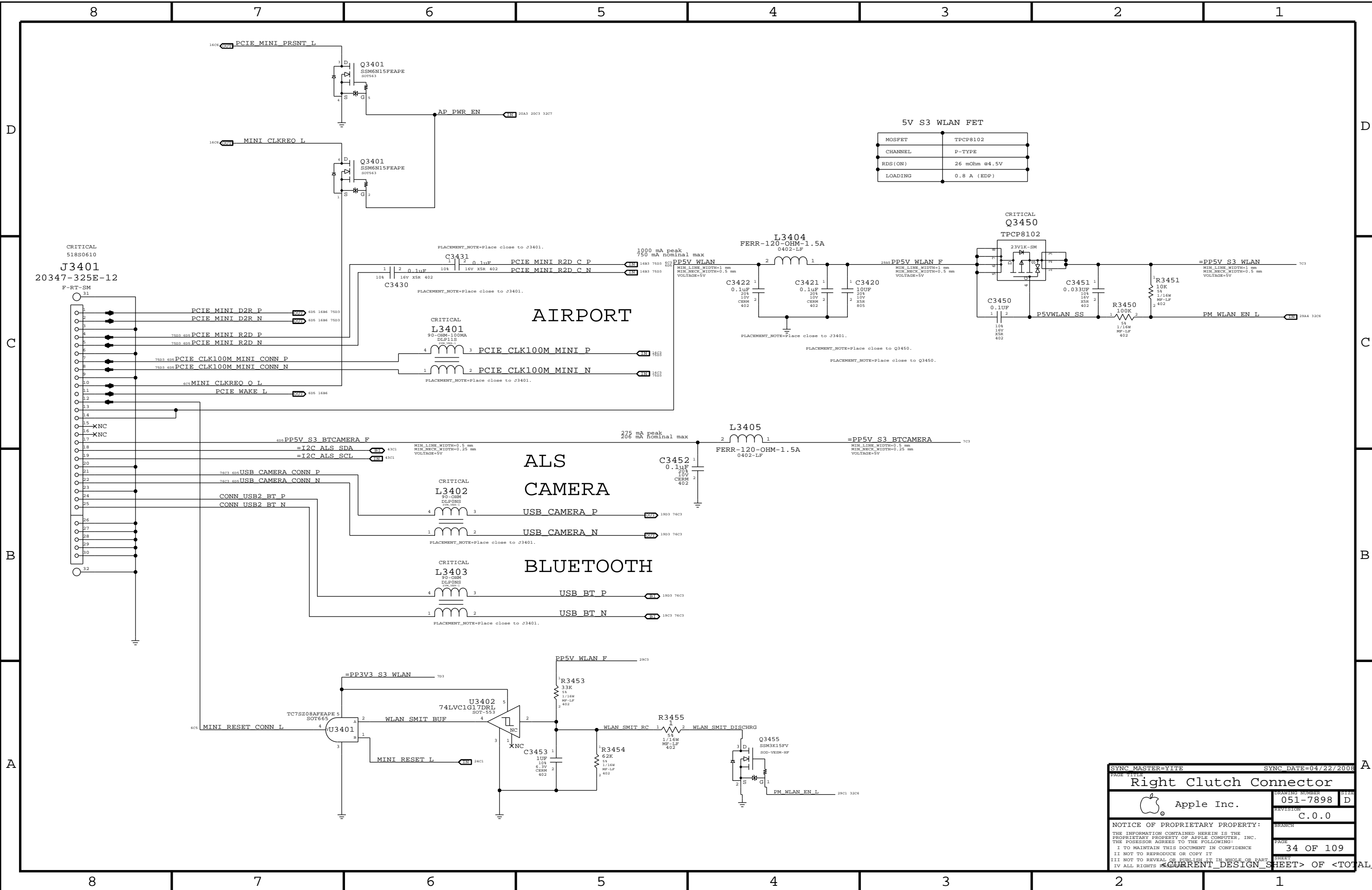
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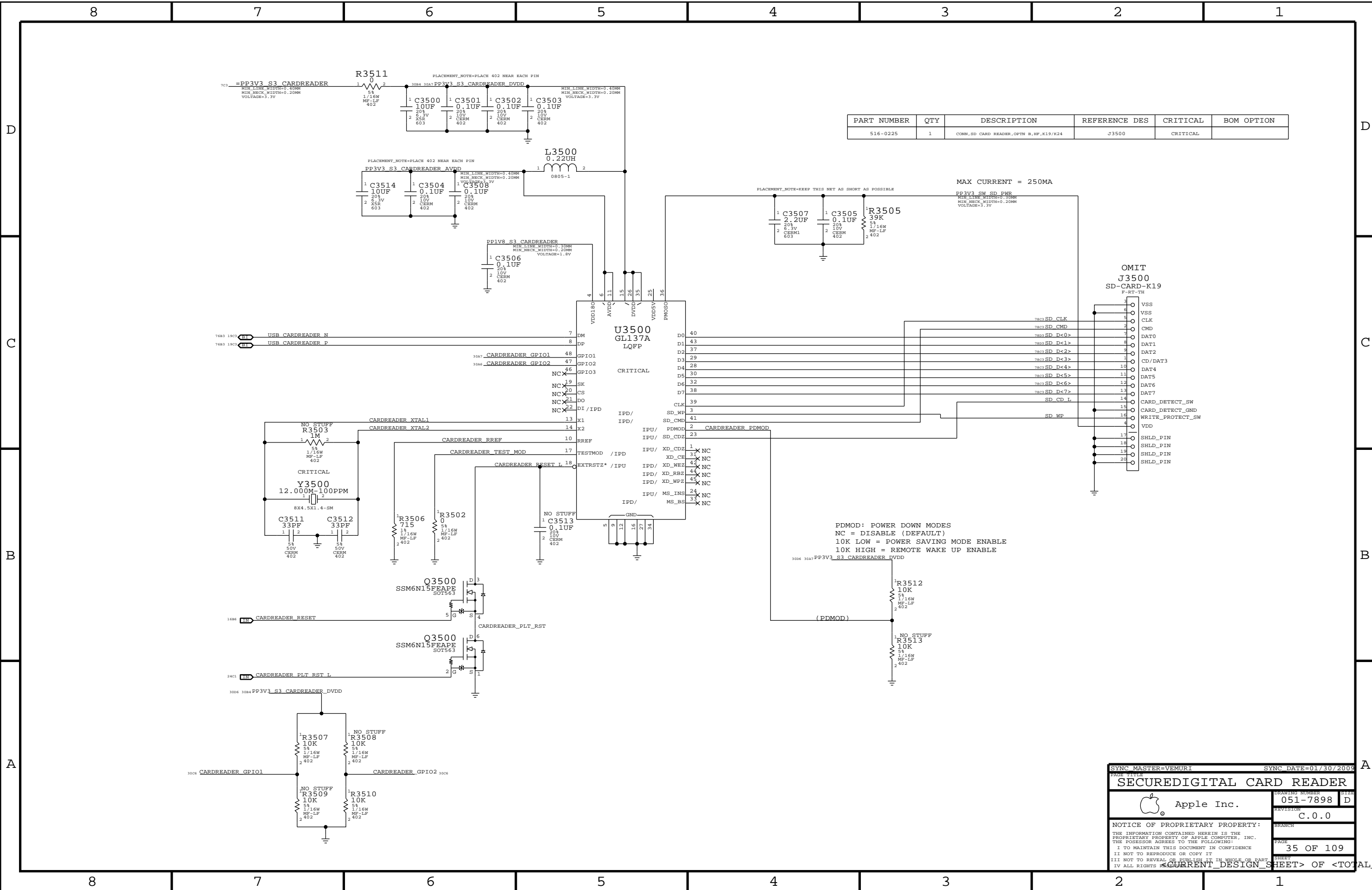
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SYNC MASTER=T18 MLB		SYNC DATE=04/04/2008	
DDR3 Support			
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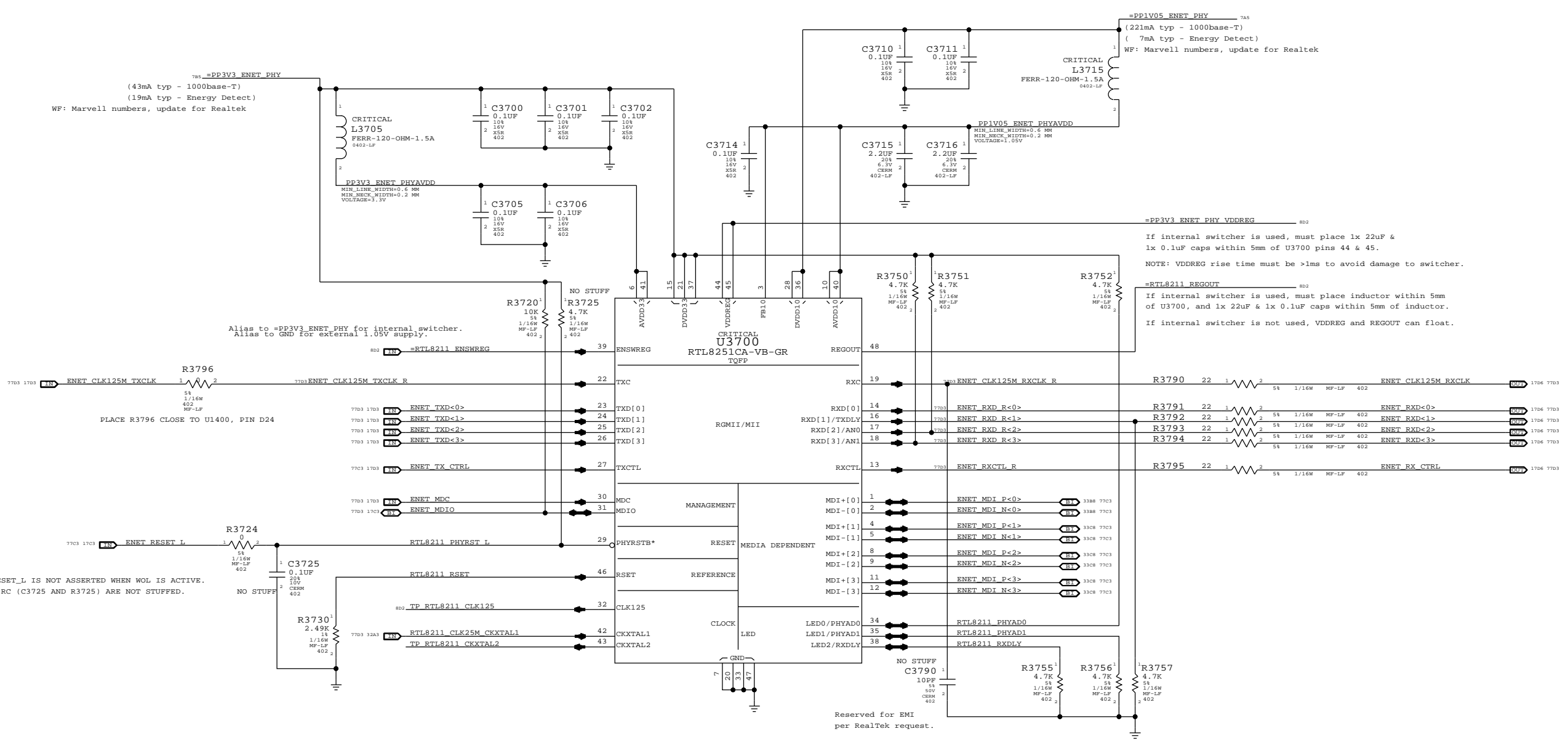
PAGE TITLE		SYNC DATE=04/22/2008	
Right Clutch Connector			
Apple Inc.		DRAWING NUMBER	051-7898 D
		REVISION	C.0.0
		BRANCH	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTM B,HP,K19/K24	J3500	CRITICAL	

SYNC MASTER=VEMURI SYNC DATE=01/30/2009
 PAGE TITLE
SECUREDIGITAL CARD READER

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7A5 =PP3V3_ENET_PHY
(43mA typ - 1000base-T)
(19mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek

=PP1V05_ENET_PHY 7A5
(22mA typ - 1000base-T)
(7mA typ - Energy Detect)
WF: Marvell numbers, update for Realtek

Alias to =PP3V3_ENET_PHY for internal switcher.
Alias to GND for external 1.05V supply.

=PP3V3_ENET_PHY_VDDREG 8D2
If internal switcher is used, must place 1x 22uF &
1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

=RTL8211_REGOUT 8D2
If internal switcher is used, must place inductor within 5mm
of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
If internal switcher is not used, VDDREG and REGOUT can float.

PLACE R3796 CLOSE TO U1400, PIN D24

ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.
HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.

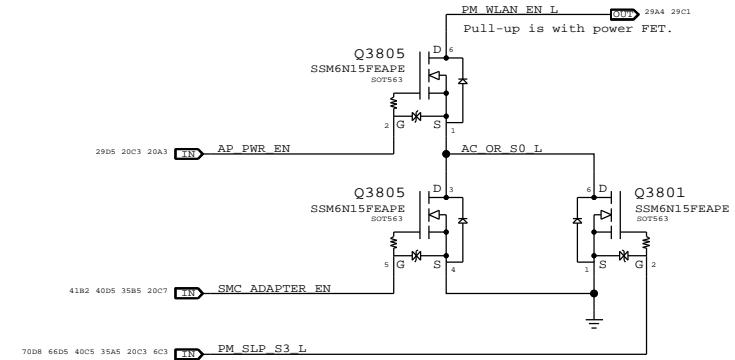
Reserved for EMI
per RealTek request.

Configuration Settings:
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

SYNC MASTER=SUMA		SYNC DATE=05/23/2008	
Ethernet PHY (RTL8211CL)			
Apple Inc.		DRAWING NUMBER	051-7898 D
		REVISION	C.0.0
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		PAGE	37 OF 109
		SHEET	

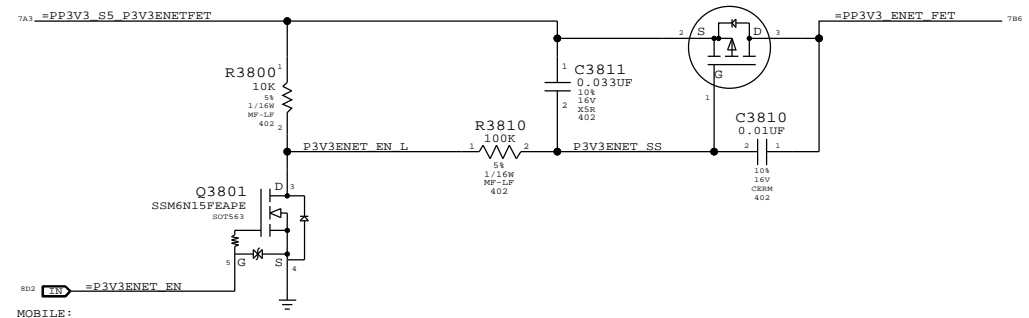
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
 NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

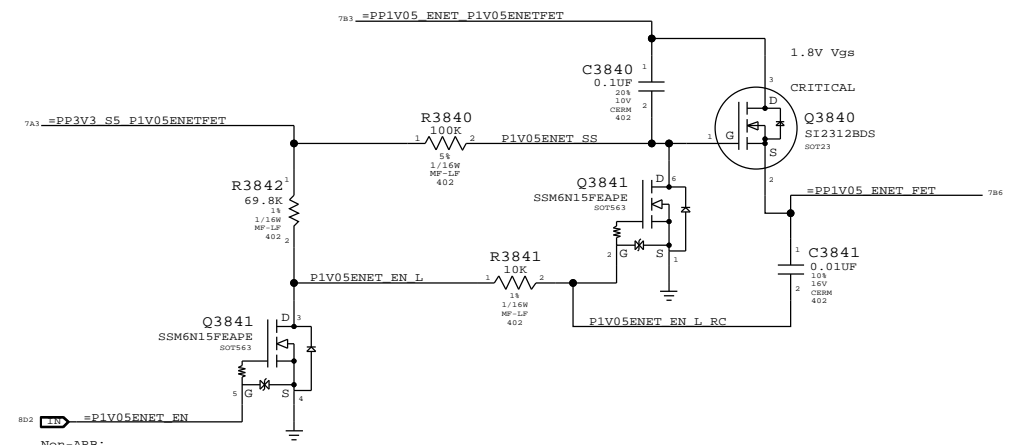
@ 2.5V Vgs:
 Rds(on) = 90mOhm max
 I(max) = 1.7A (85C)
 CRITICAL
 Q3810
 NTR4101P
 SOT-23-BF



MOBILE:
 Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

1.05V ENET FET

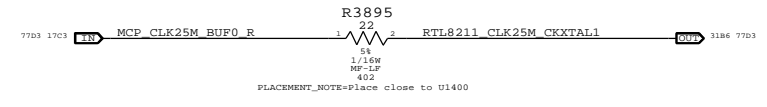
1.8V Vgs
 CRITICAL
 Q3840
 SI2312BDS
 SOT23



Non-ARB:
 Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNC MASTER=SUMA	SYNC DATE=07/01/2008
Ethernet & AirPort Support	
Apple Inc.	051-7898 D
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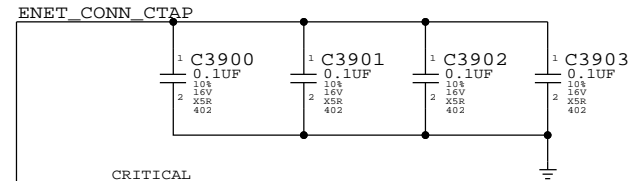
B

B

A

A

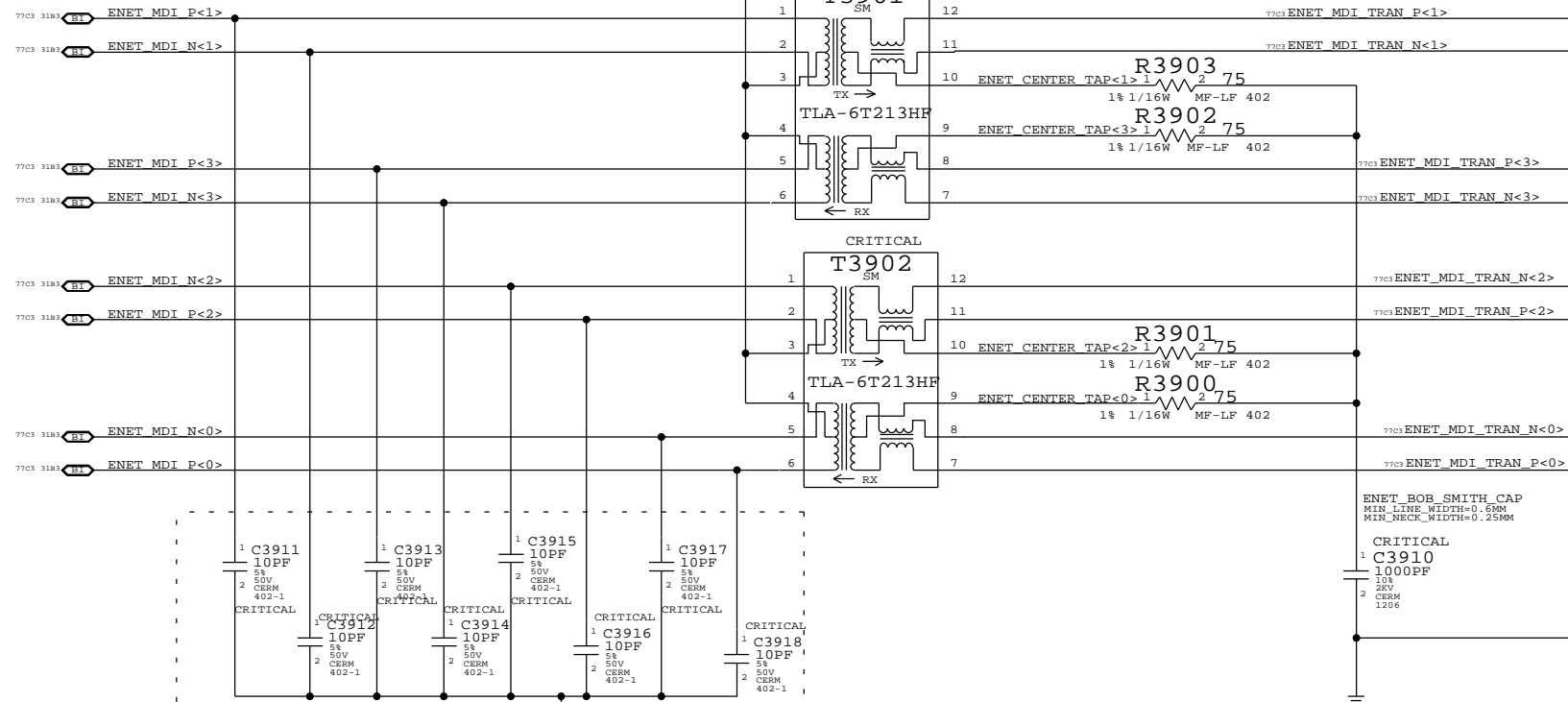
PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902



ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-M97-3
F-RT-TH

514-0636



SYNC MASTER=SUMA SYNC DATE=04/04/2008

ETHERNET CONNECTOR

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0558	1	RES,0.68 OHM,1%,0402,SMD	R4100	CRITICAL	

D

D

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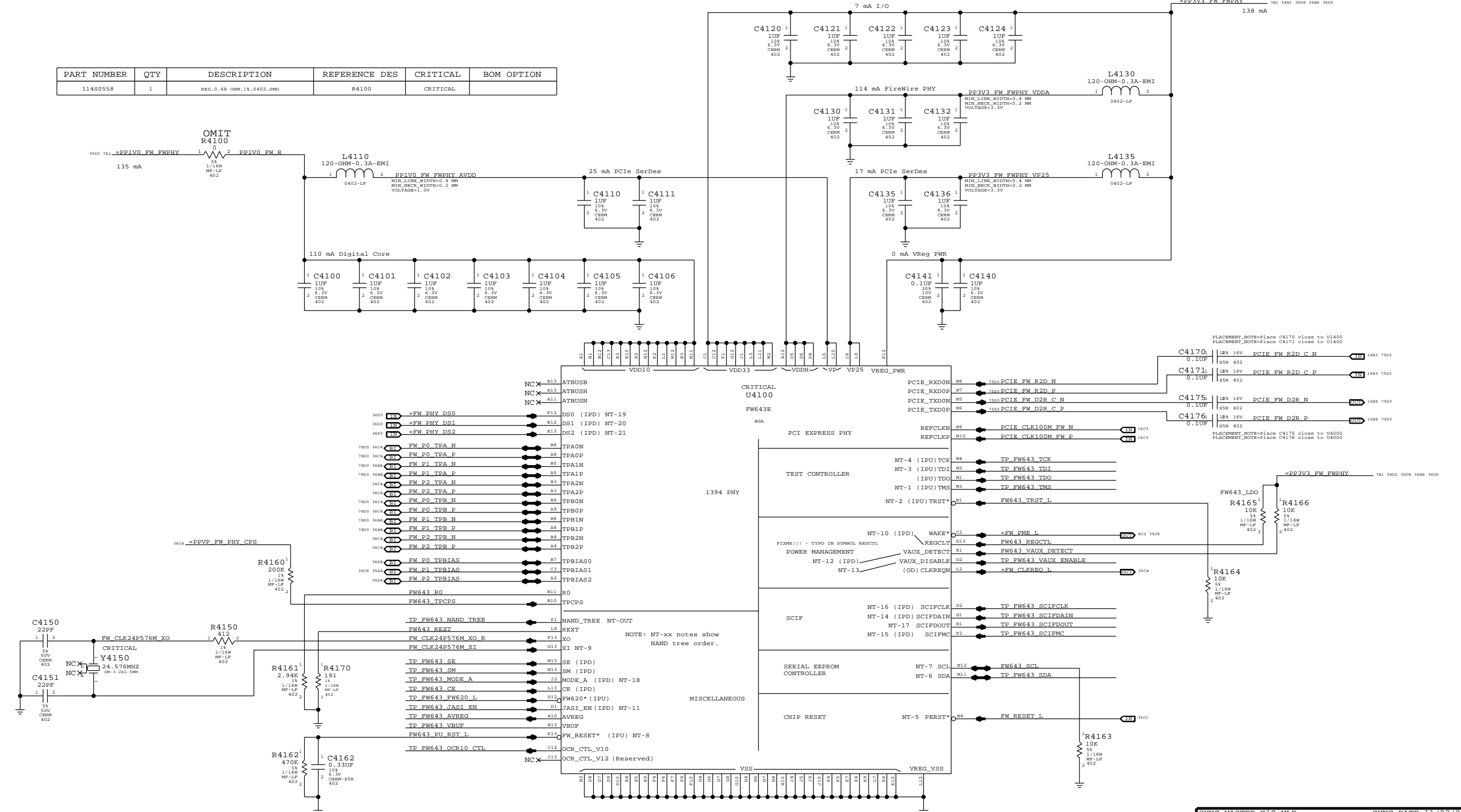
C

B

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A



SYNC MASTER=K19 MLB SYNC DATE=11/02/2008

FireWire LLC/PHY (FW643)

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Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PP3V3_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
 (NONE)

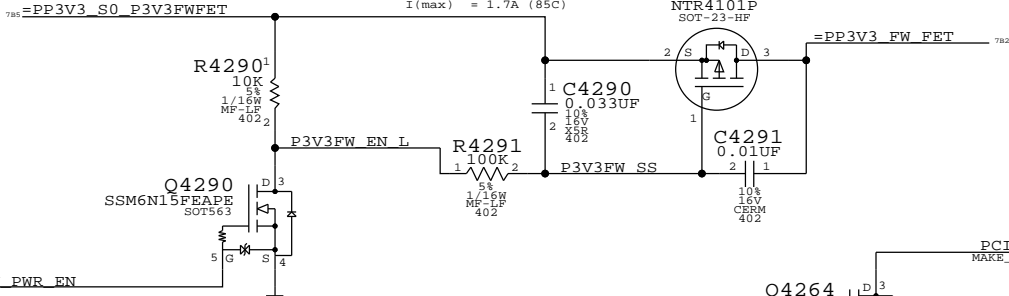
BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:

Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

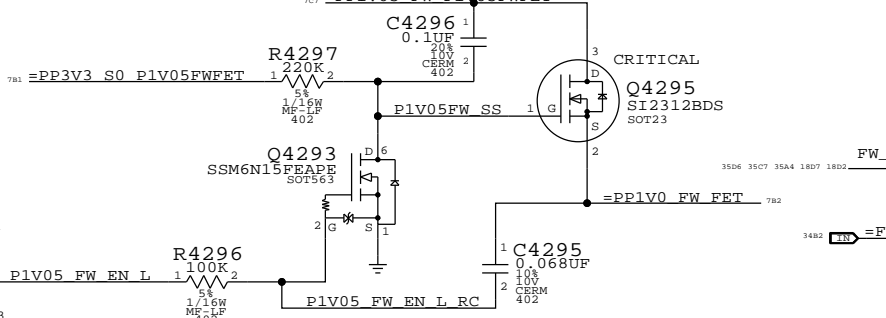
CRITICAL
Q4291
NTR4101P
SOT-23-HF



1.05V FW FET

=PP1V05_FW_P1V05FWFET

CRITICAL
Q4295
SI2312BDS
SOT23

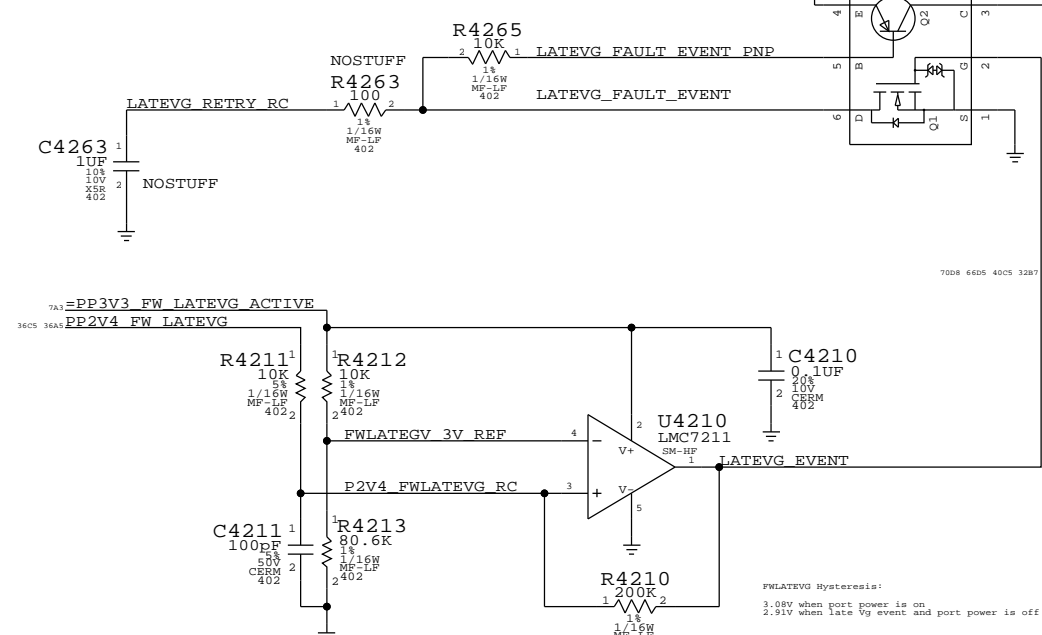


FireWire Port Power Switch

FireWire Port Power Switch

FireWire Port Power Switch

Late-VG Event Detection



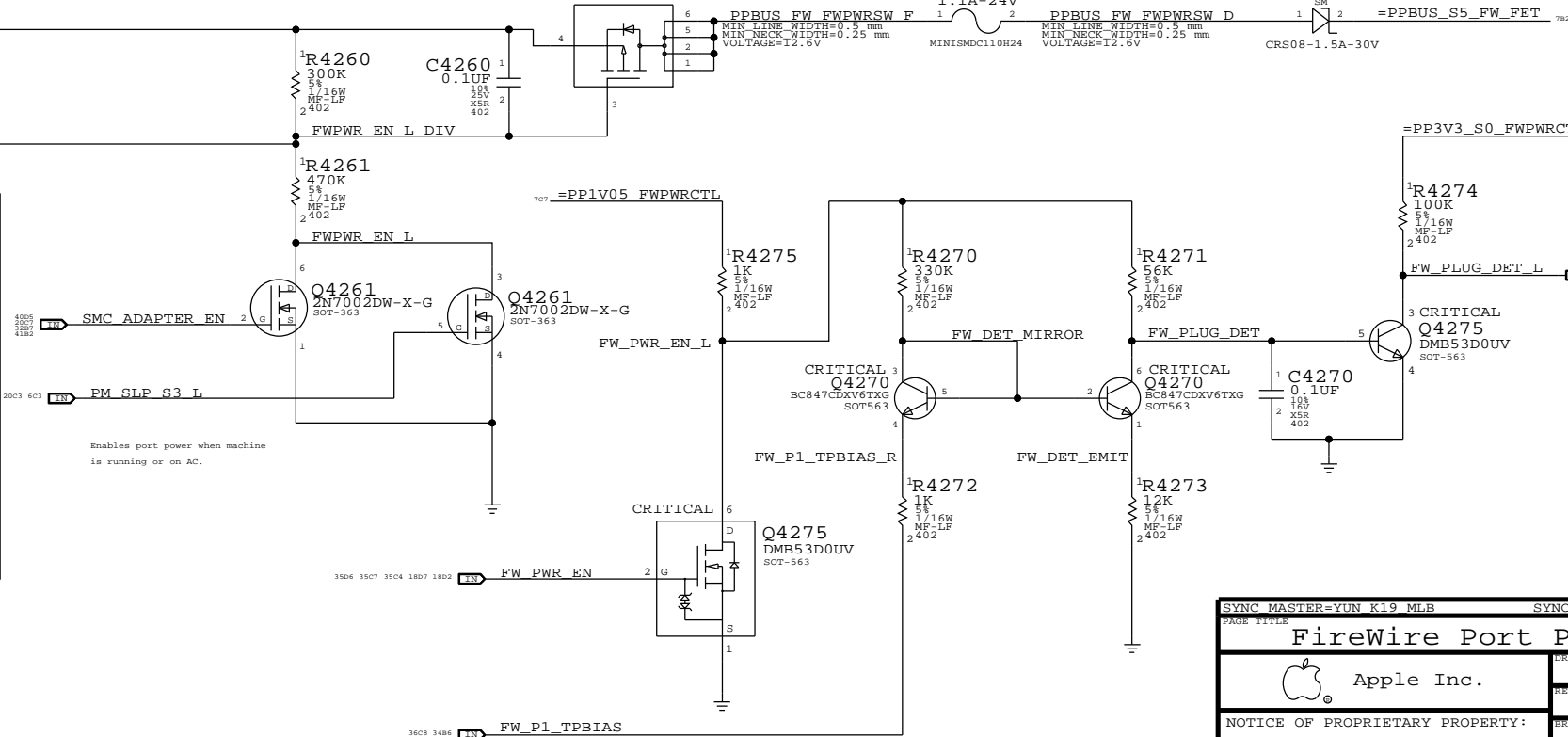
FWLATEGV Hysteresis:
3.0V when port power is on
2.9V when late Vg event and port power is off

Enables port power when machine is running or on AC.

CRITICAL
Q4260
FDC638P_G
SM

CRITICAL
F4260
1.1A-24V

CRITICAL
D4260
CRS08-1.5A-30V



SYNC MASTER=YUN K19 MLB SYNC DATE=12/22/2008

FireWire Port Power

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Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

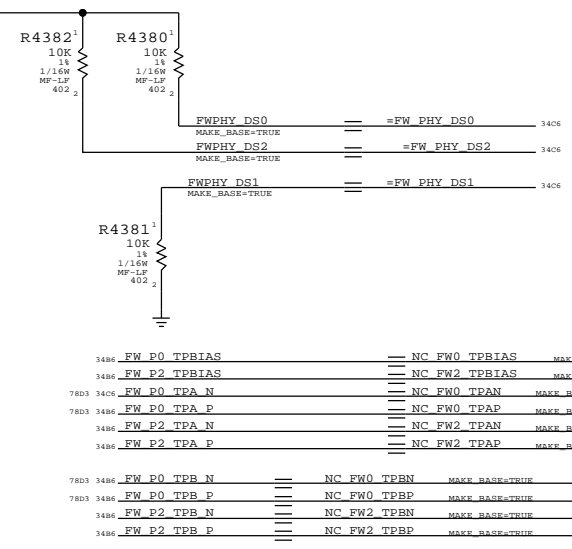
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

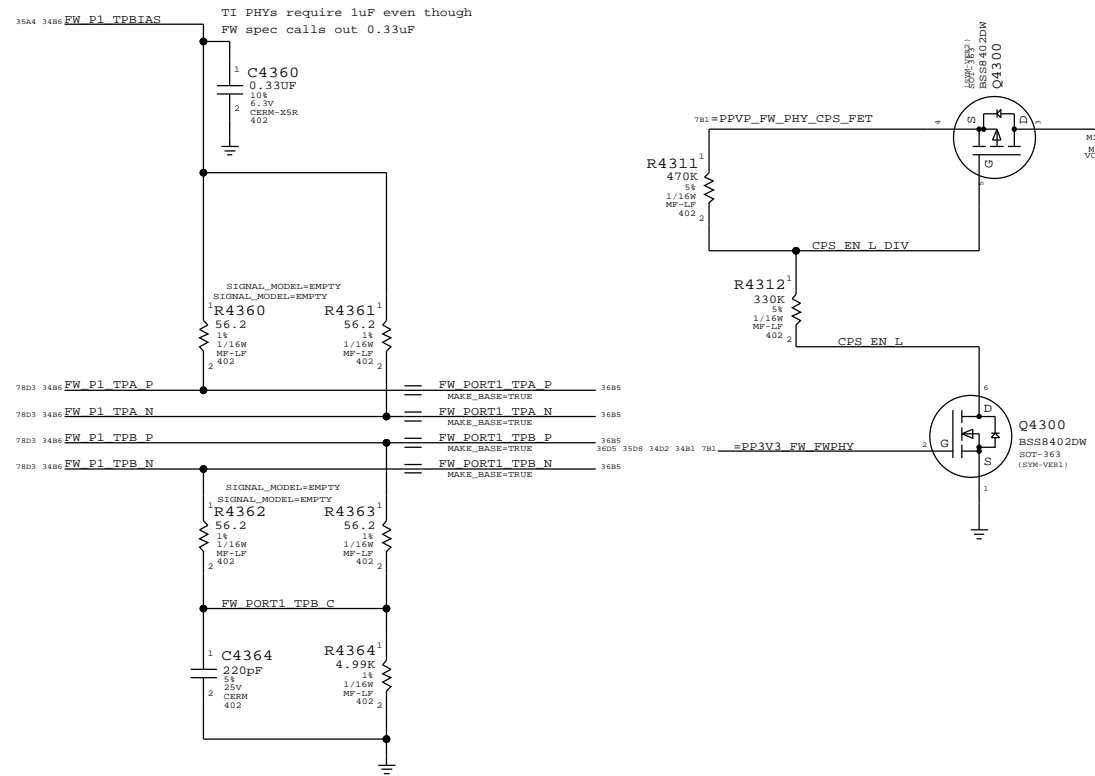
FireWire PHY Config Straps

Configures PHY for:
 - 1-port Portable Power Class (0)
 - Port "1" Bilingual (1394B)

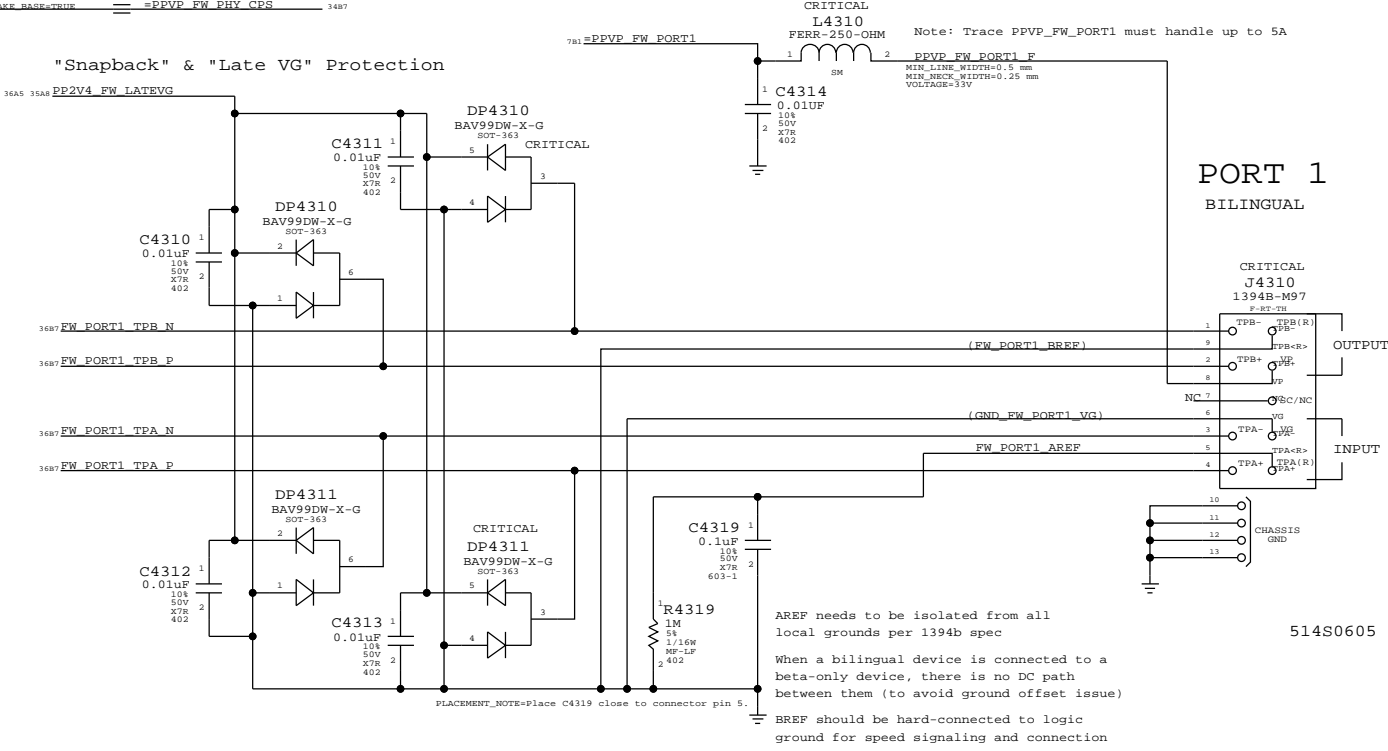


Termination

Place close to FireWire PHY

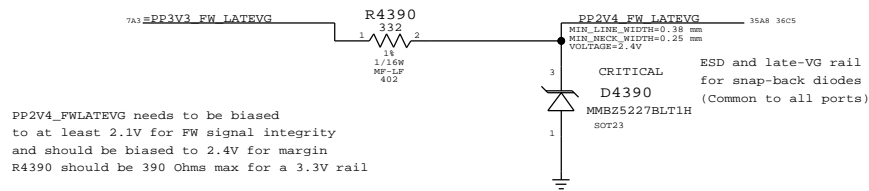


Cable Power



PORT 1 BILINGUAL

Late-VG Protection Power



SYNC MASTER=K19 MLB SYNC DATE=11/02/2008

FireWire Ports

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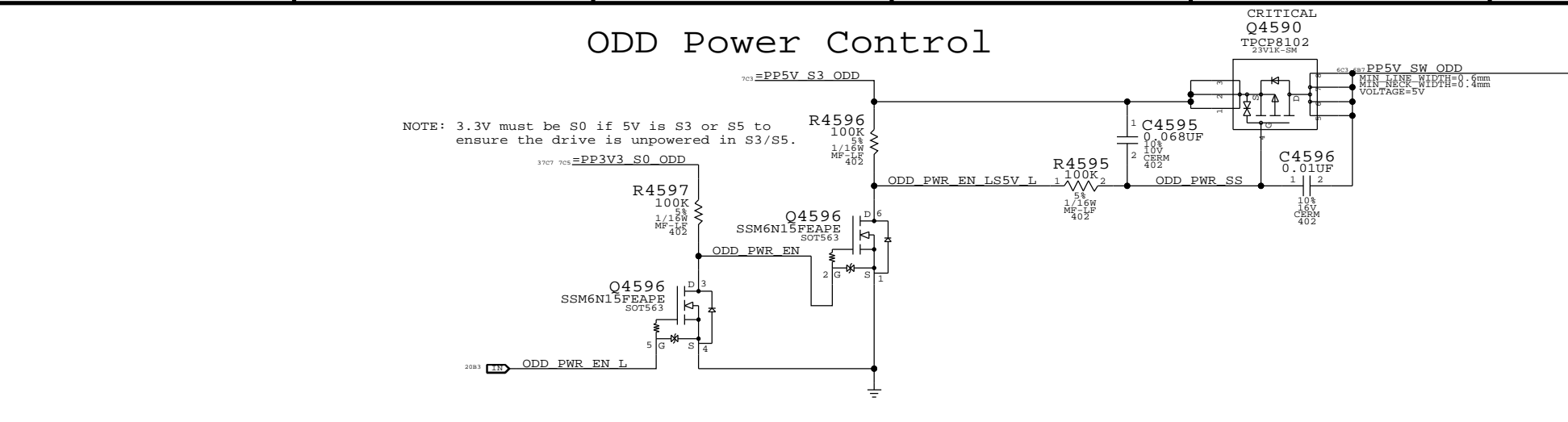
IV ALL RIGHTS RESERVED

43 OF 109 SHEETS

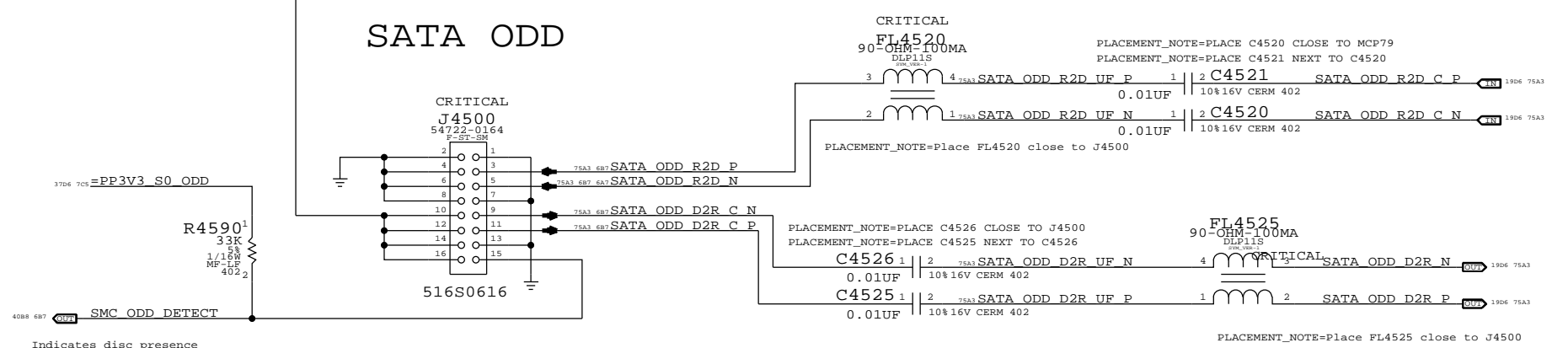
CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

ODD Power Control

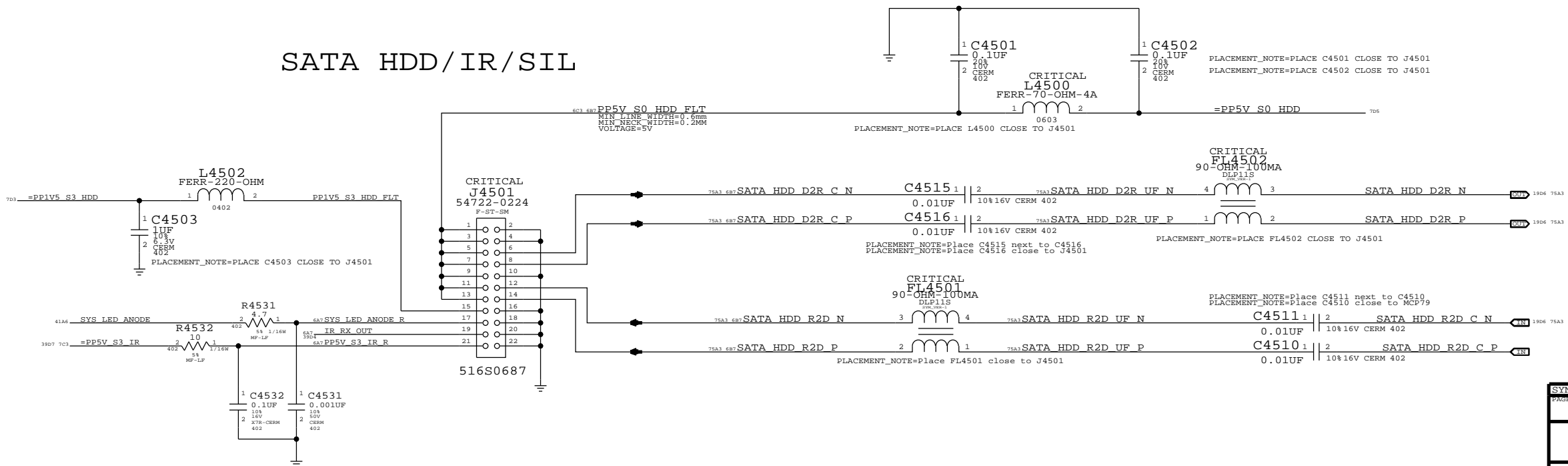
NOTE: 3.3V must be S0 if 5V is S3 or S5 to ensure the drive is unpowered in S3/S5.



SATA ODD



SATA HDD/IR/SIL



SYNC MASTER=K19 MLB SYNC DATE=12/04/2008

PAGE TITLE		DRAWING NUMBER	
SATA Connectors		051-7898 D	
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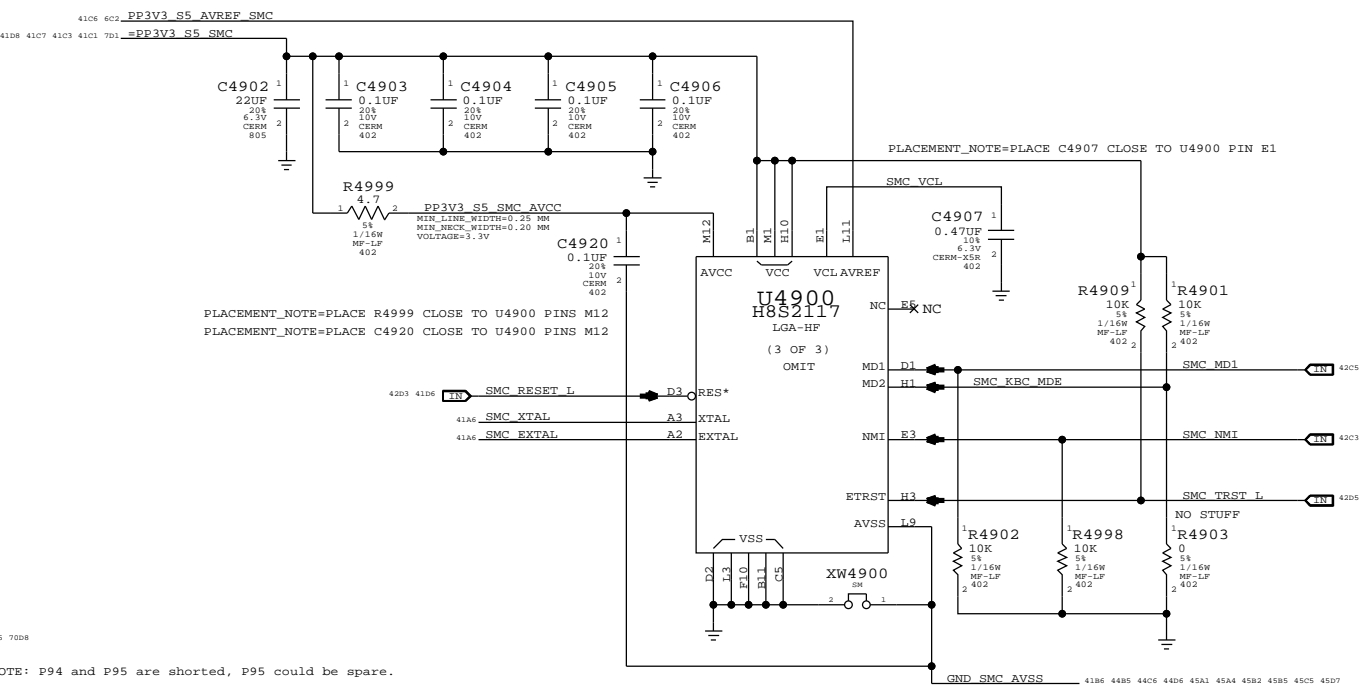
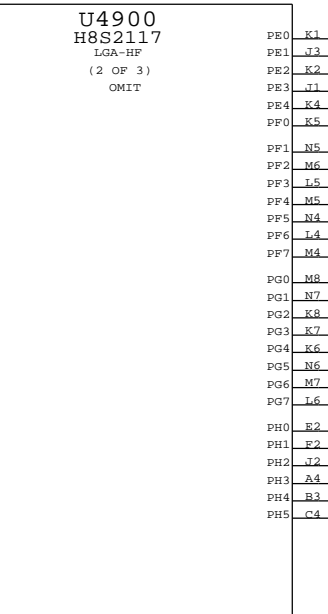
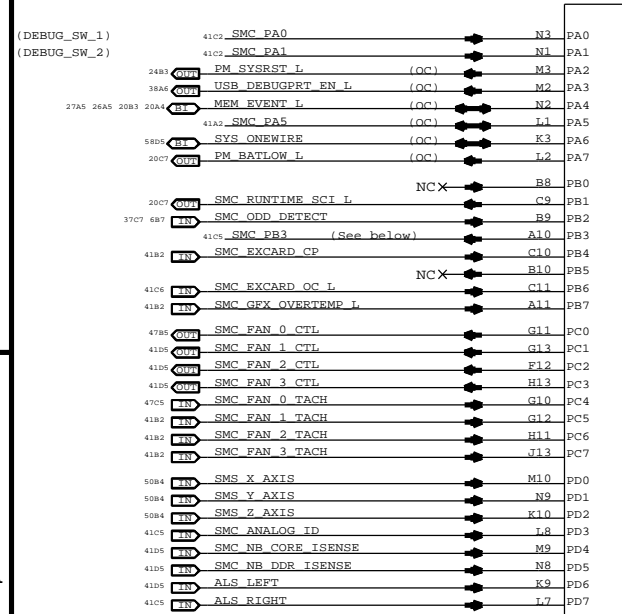
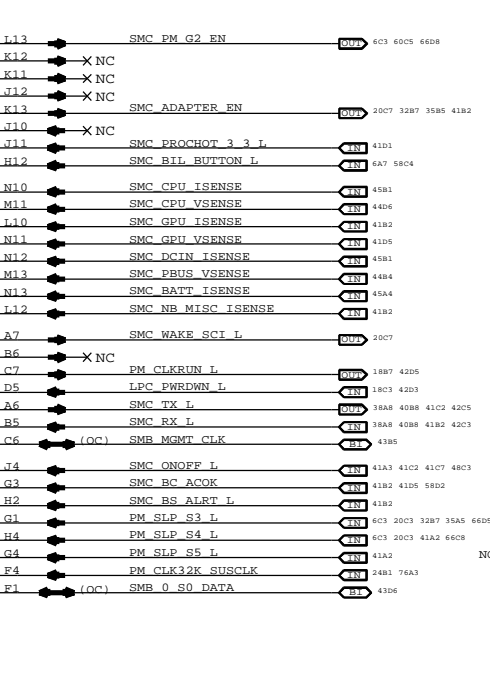
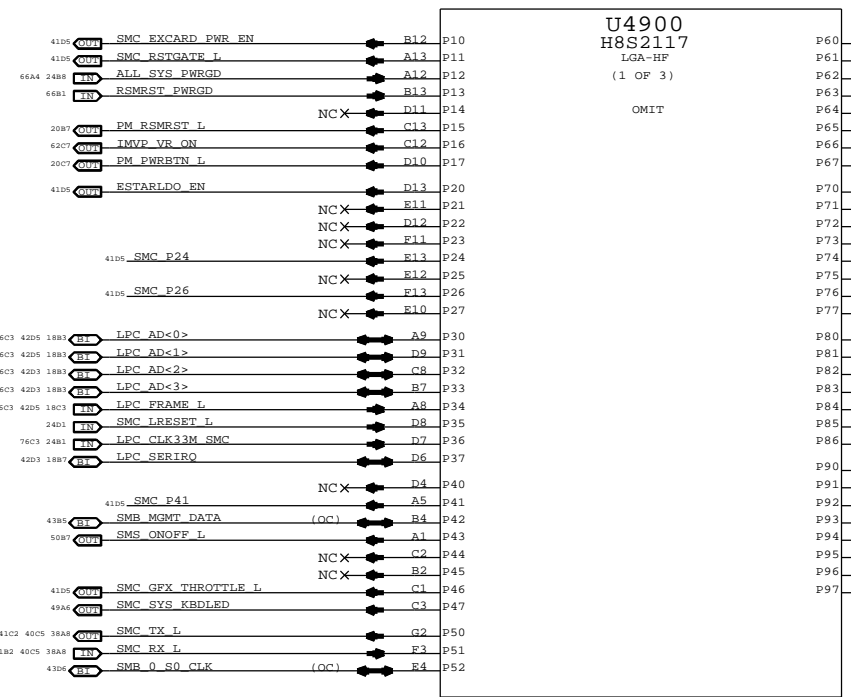
4

3

2

1

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC_PB3: SMC_IG_THROTTLE_L for MG systems. Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SYNC MASTER=T18 MLB SYNC DATE=06/26/2008

SMC		DATE	06/26/2008
Apple Inc.		DESIGN NUMBER	051-7898
		REVISION	C.0.0
		BATCH	
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8

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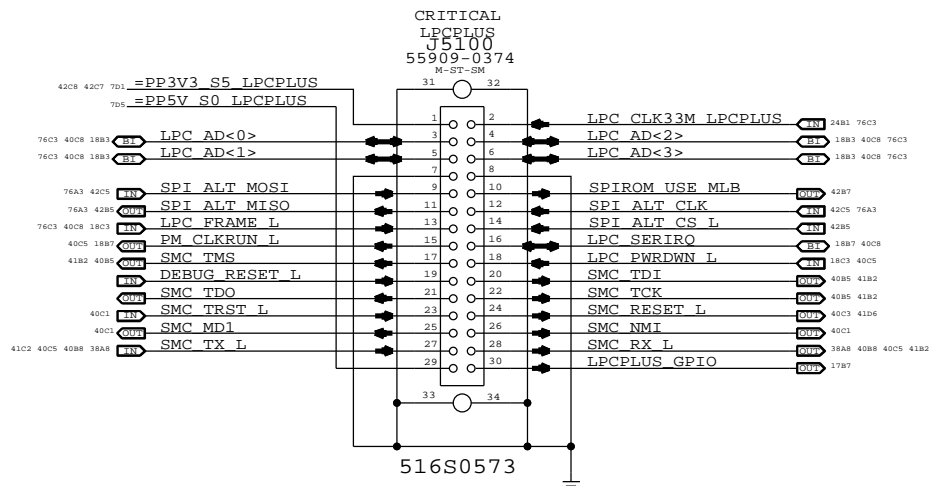
3

2

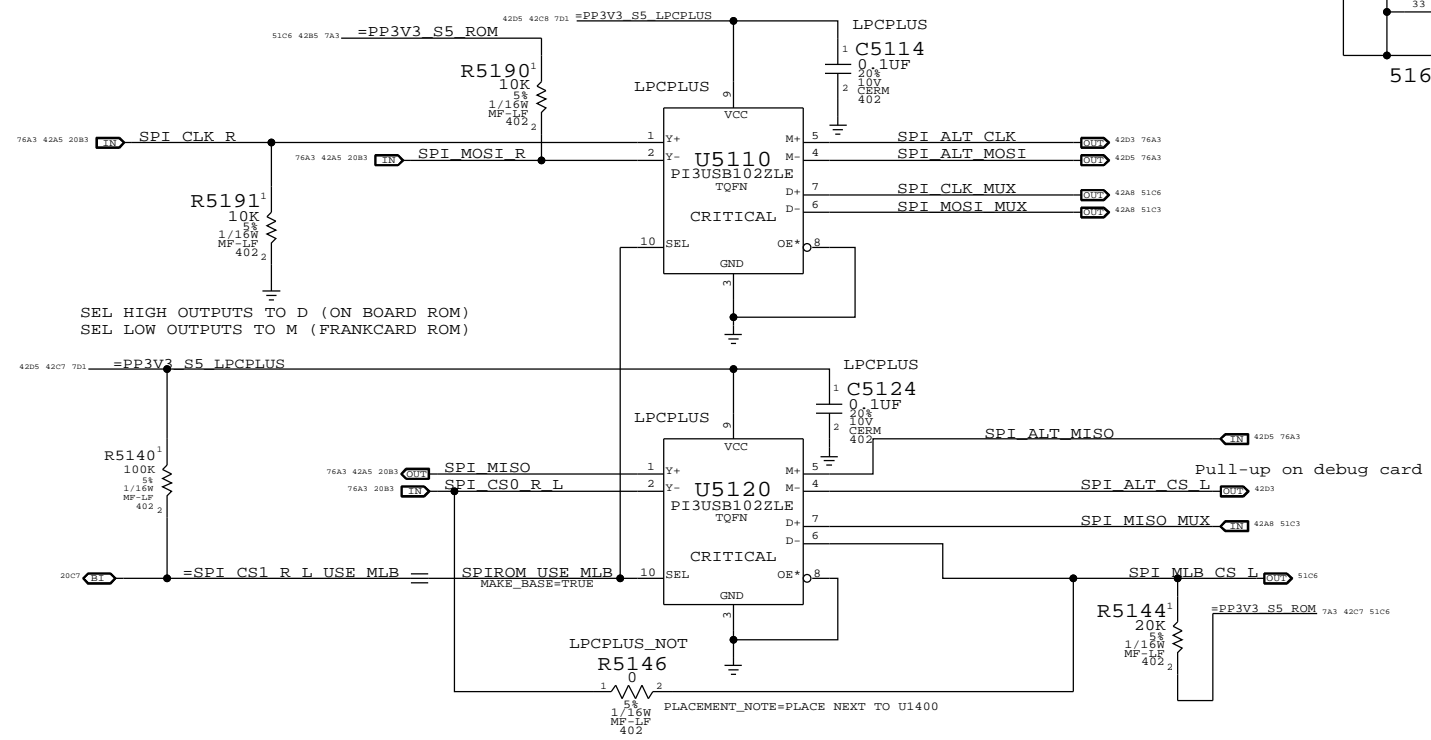
1

SHEET <CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>

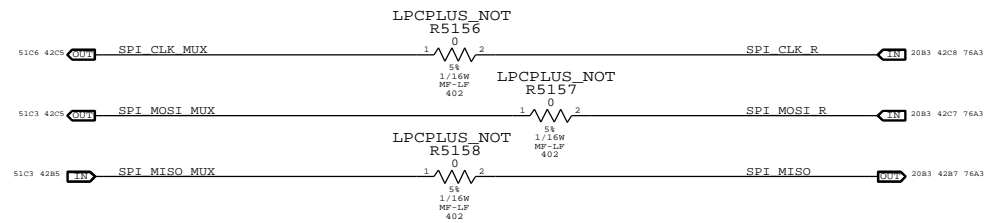
LPC+SPI Connector



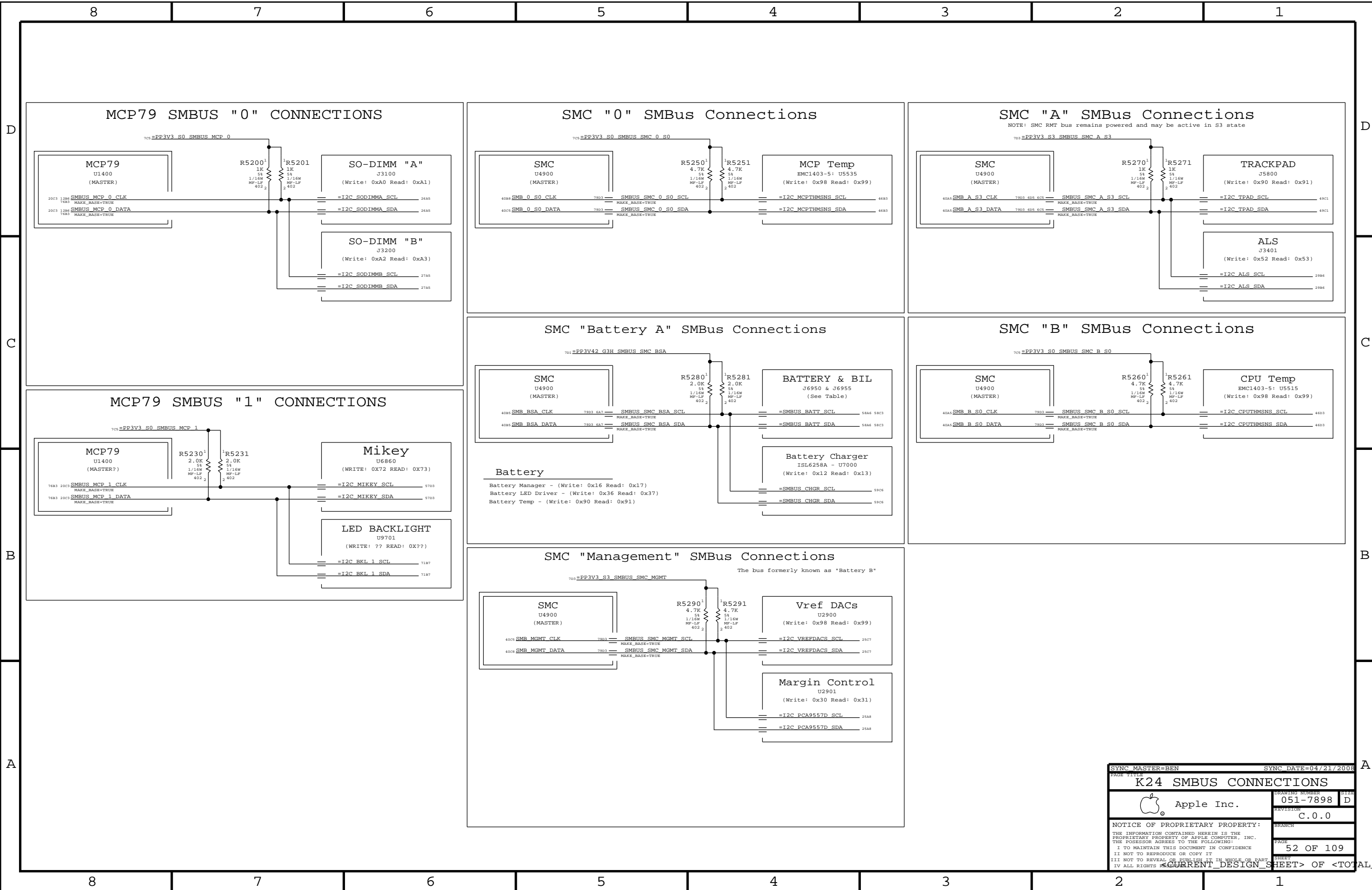
Alternate SPI ROM Support



SPI MUX BYPASS

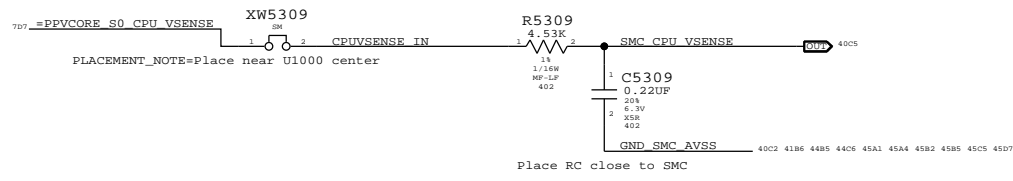


SYNC MASTER=CHANGZHANG		SYNC DATE=05/09/2008	
LPC+SPI Debug Connector			
Apple Inc.		DRAWING NUMBER	051-7898 D
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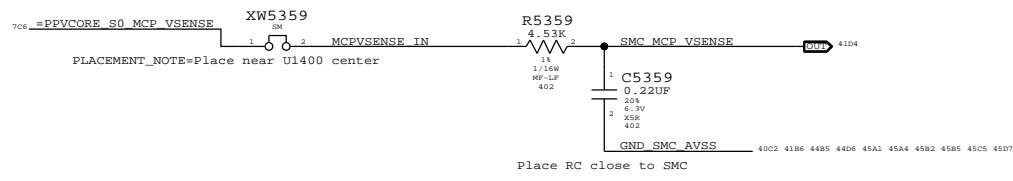


SYNC MASTER=BEN		SYNC DATE=04/21/2008	
K24 SMBUS CONNECTIONS			
Apple Inc.		DRAWING NUMBER	051-7898
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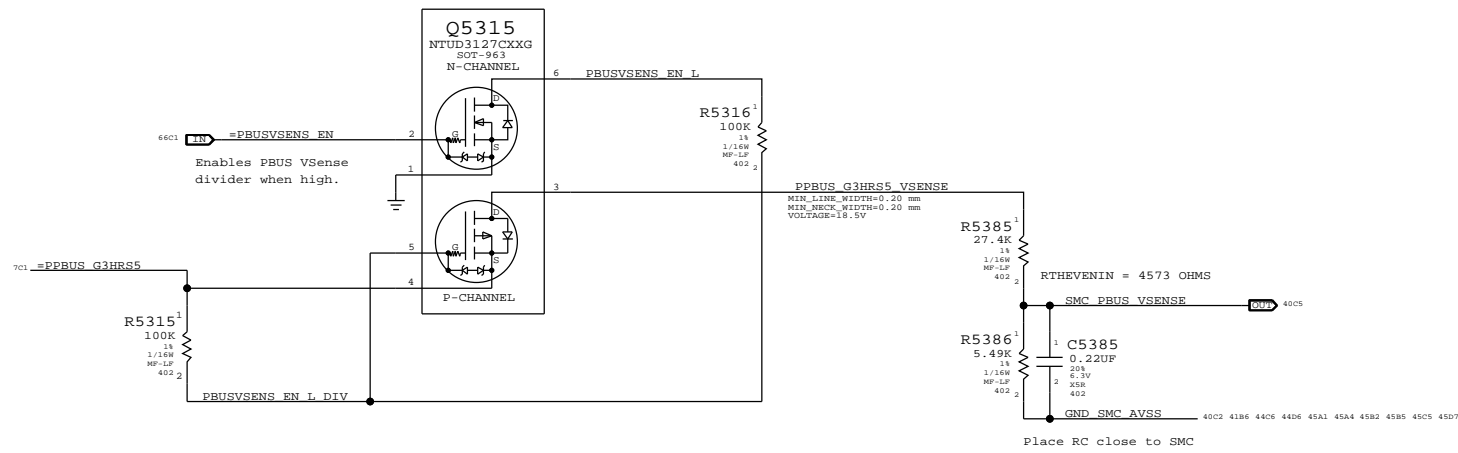
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter

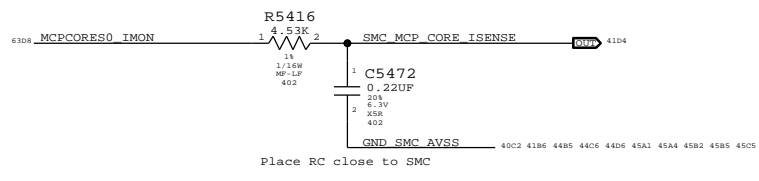


PBUS VOLTAGE SENSE ENABLE & FILTER

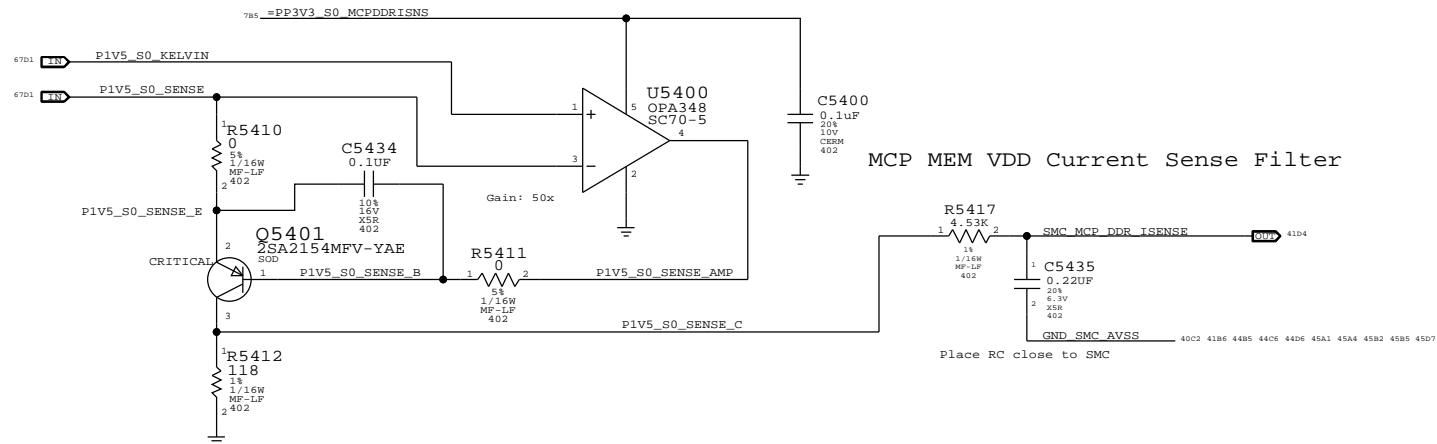


SYNC MASTER=YUNWU		SYNC DATE=02/04/2008	
PAGE TITLE			
VOLTAGE SENSING			
Apple Inc.		DRAWING NUMBER	051-7898
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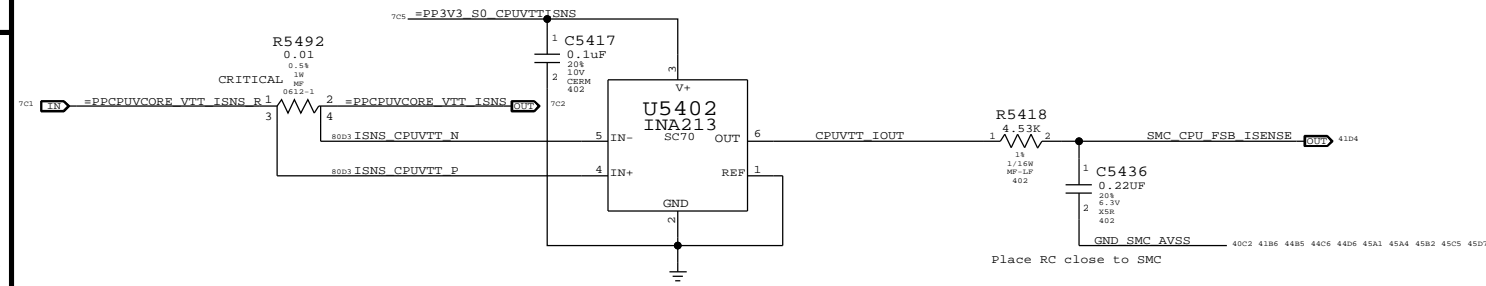
MCP VCore Current Sense Filter



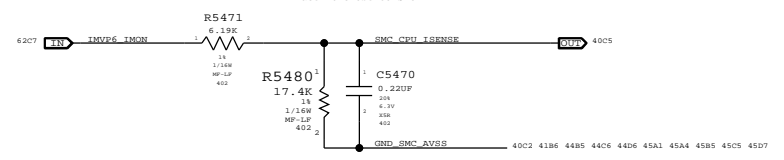
MCP MEM VDD Current Sense



CPU 1.05V AND CPU VCore HIGH SIDE CURRENT SENSE

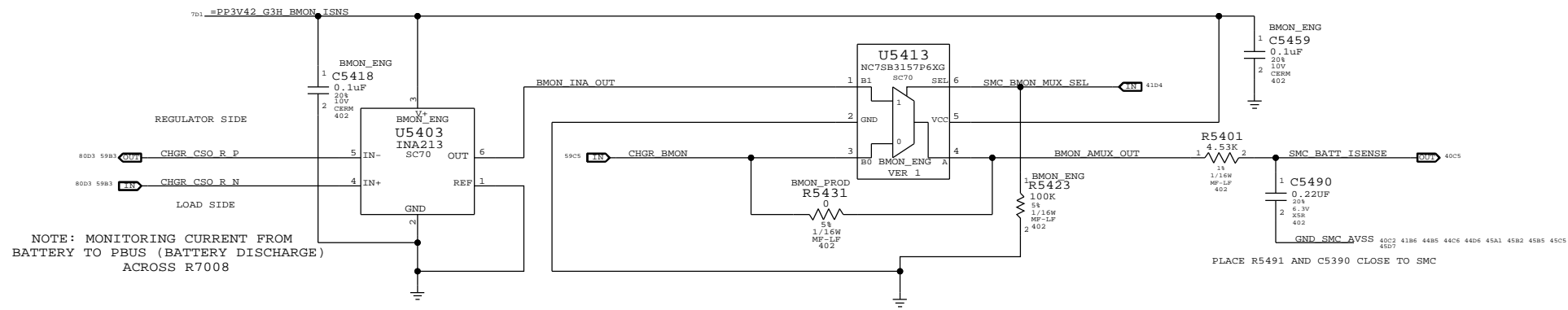


CPU VCore Load Side Current Sense / Filter



BMON CURRENT SENSE

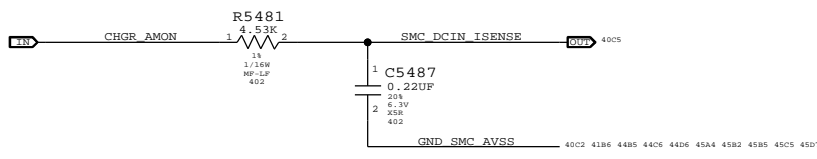
PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)



NOTE: MONITORING CURRENT FROM BATTERY TO PBUS (BATTERY DISCHARGE) ACROSS R7008
 PLACE U5403 AND C5418 NEAR R7008
 INA213 has gain of 50V/V

For engineering, stuff U5313 and unstuff R5330
 For production, stuff R5330 and unstuff U5313

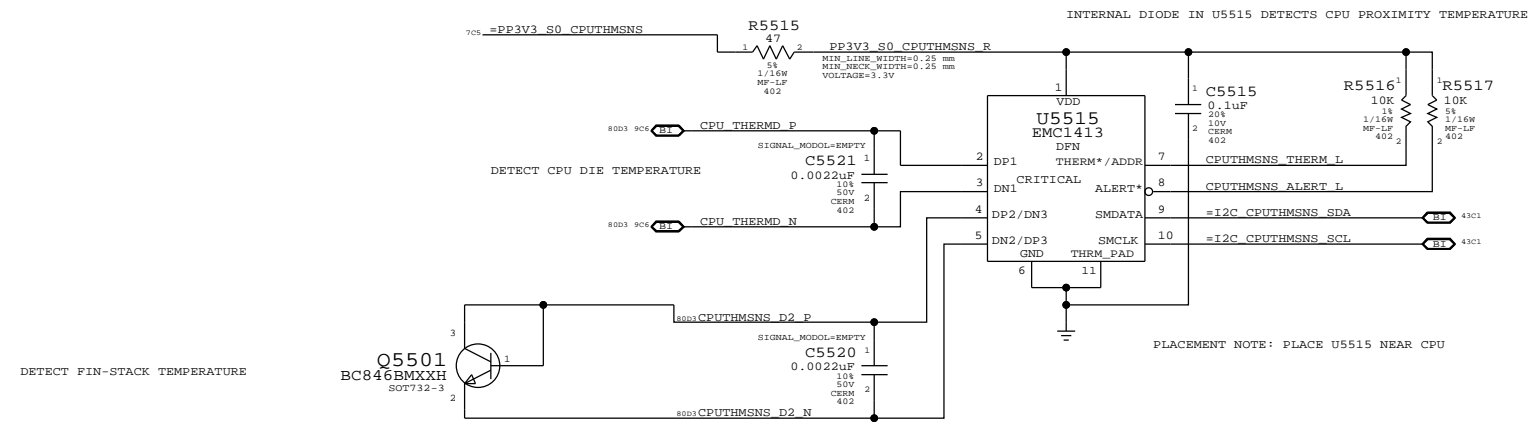
DC-IN (AMON) CURRENT SENSE



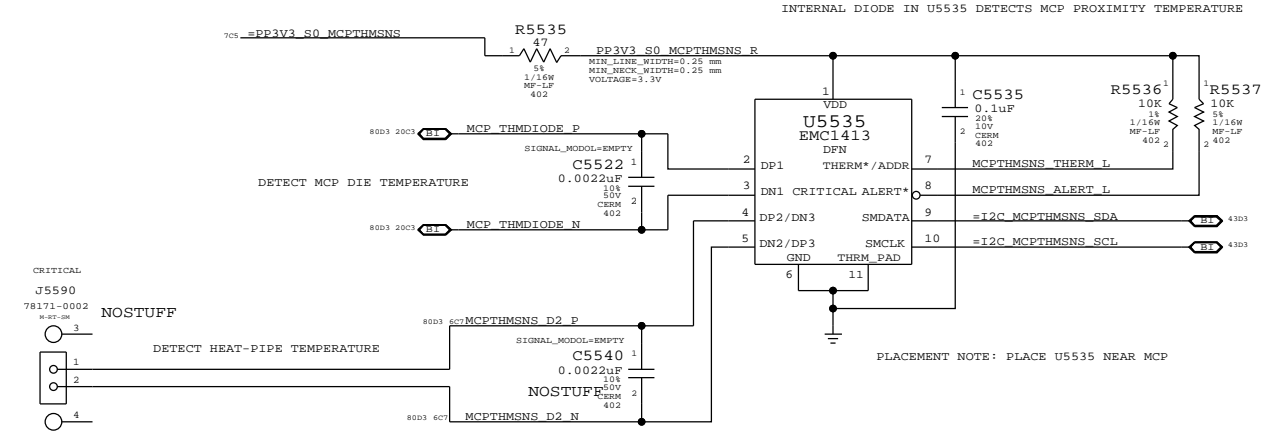
SYNC MASTER=YUNWU SYNC DATE=12/17/2008

Current Sensing	
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CPU T-Diode Thermal Sensor



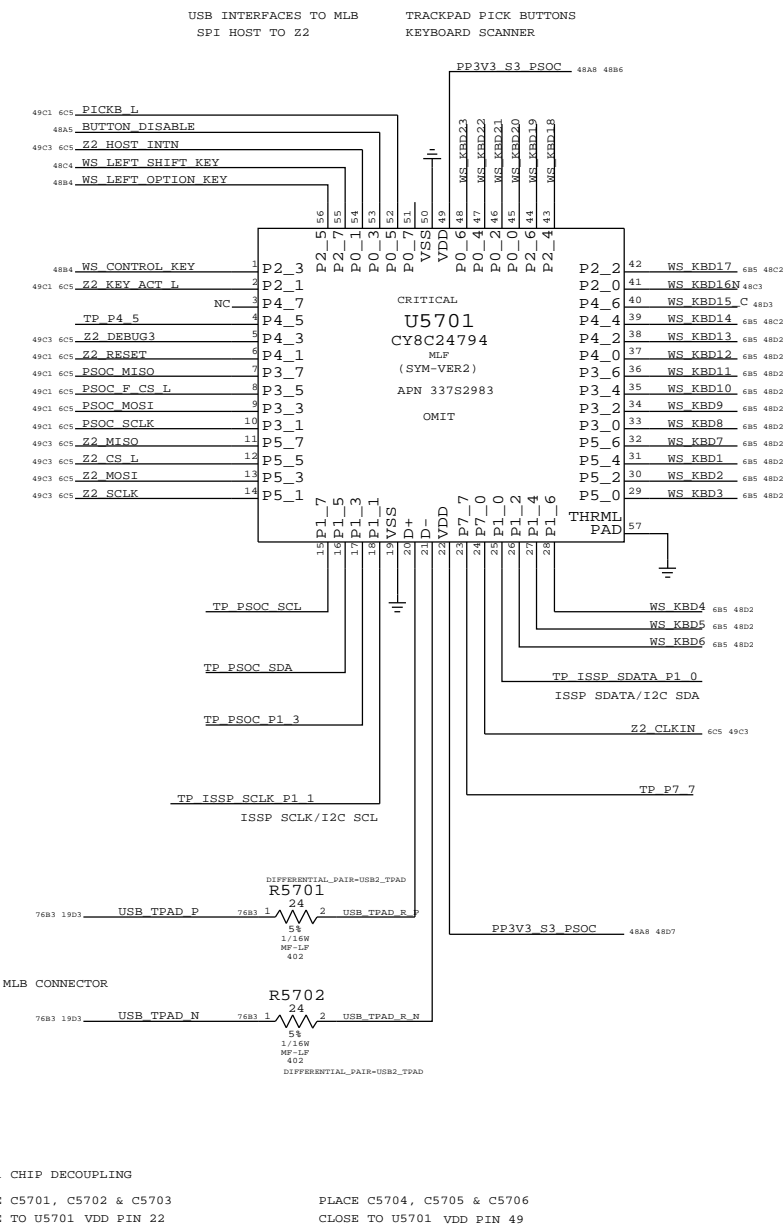
MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

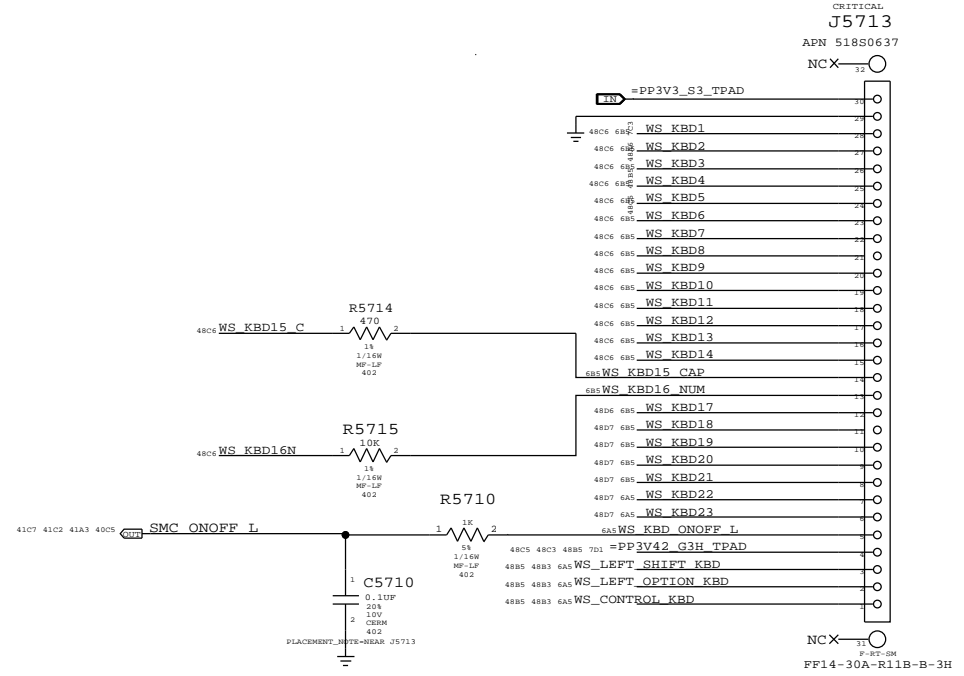
SYNC MASTER=YUNWU		SYNC DATE=03/20/2008	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-7898 D
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		BRANCH	
		PAGE	55 OF 109
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PSOC USB CONTROLLER

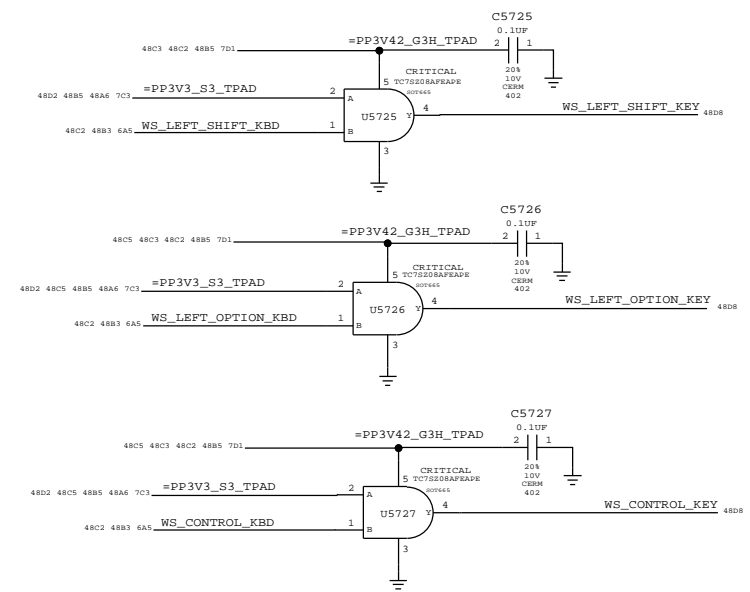


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V-	100A	2.55 KOHM	0.0255 V	0.255E-6 W
3V3 LDO	VDD	800A		0.204 V	16.32E-6 W
	VOUT	60MA MAX	10 OHM	0.6 V	36E-3 W
	VDD	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
	VDD	14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

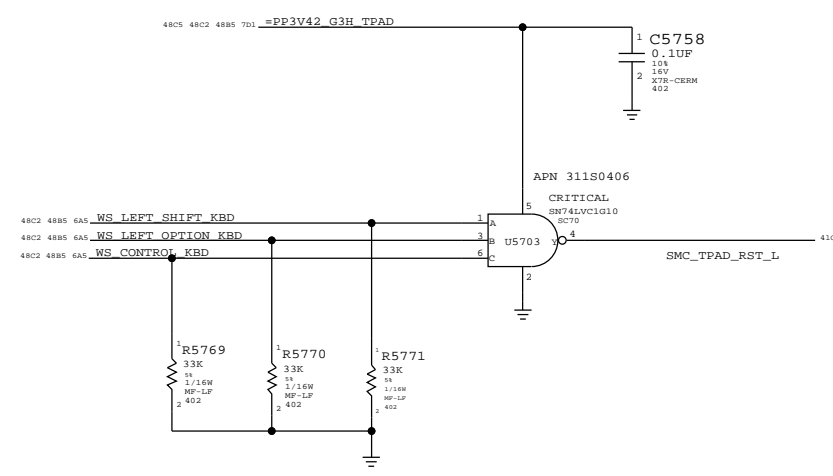
KEYBOARD CONNECTOR



ISOLATION CIRCUIT



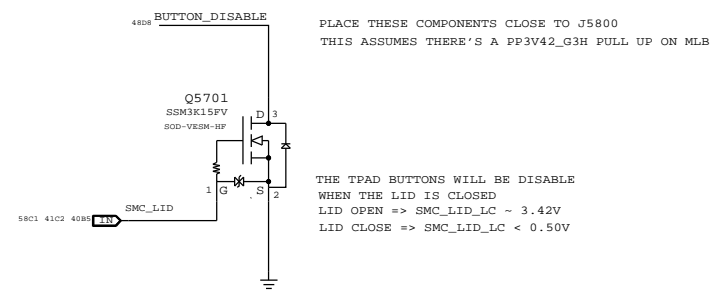
SMC_MANUAL_RESET LOGIC



Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0406	311S0447		ALL	NXP PART AS ALTERNATE

TPAD BUTTONS DISABLE



SYNC MASTER=YUAN.MA SYNC DATE=04/22/2008

WELLSPRING 1

Apple Inc.

051-7898 D

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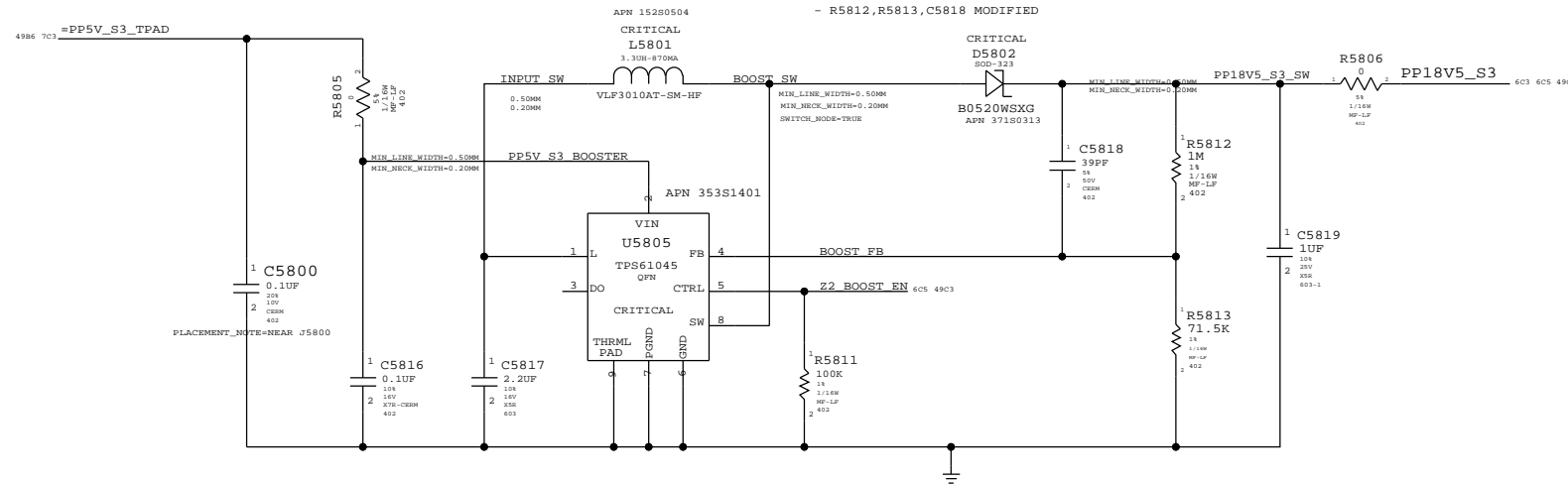
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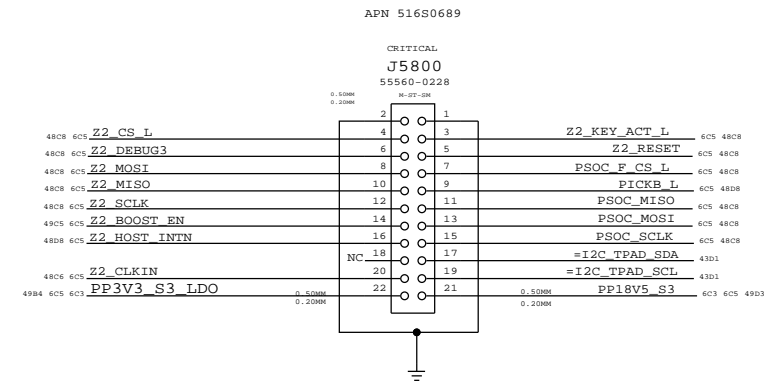
CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

BOOSTER +18.5VDC FOR SENSORS

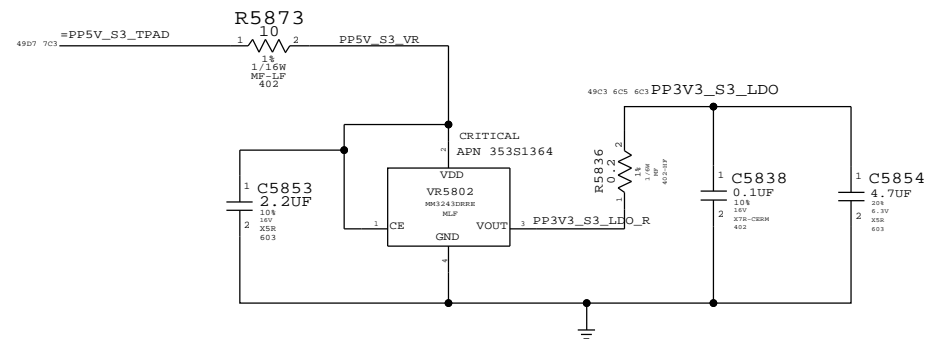
- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812, R5813, C5818 MODIFIED



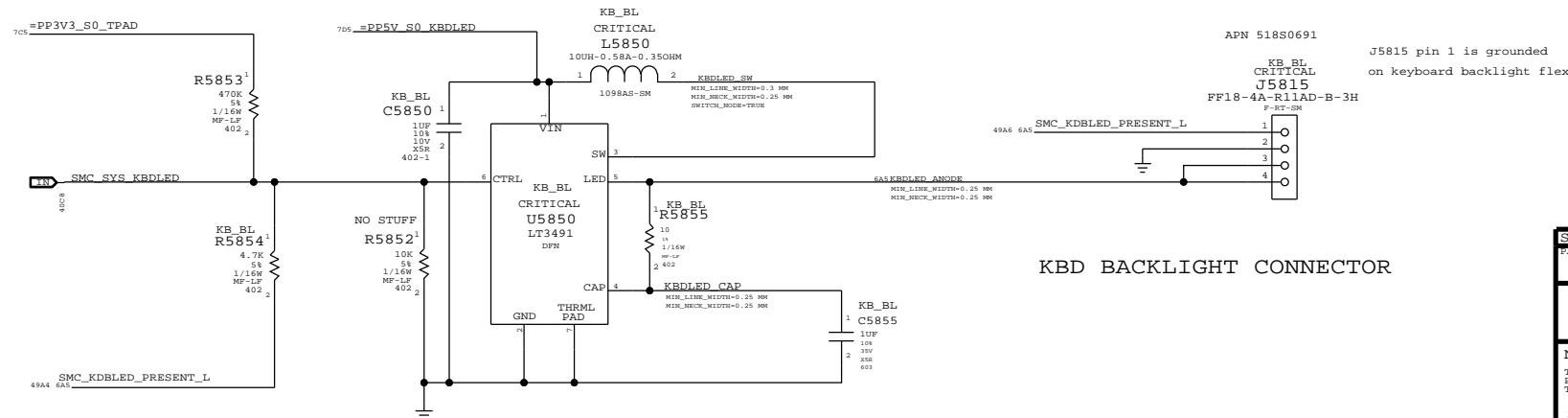
IPD FLEX CONNECTOR



3V3 LDO FOR IPD



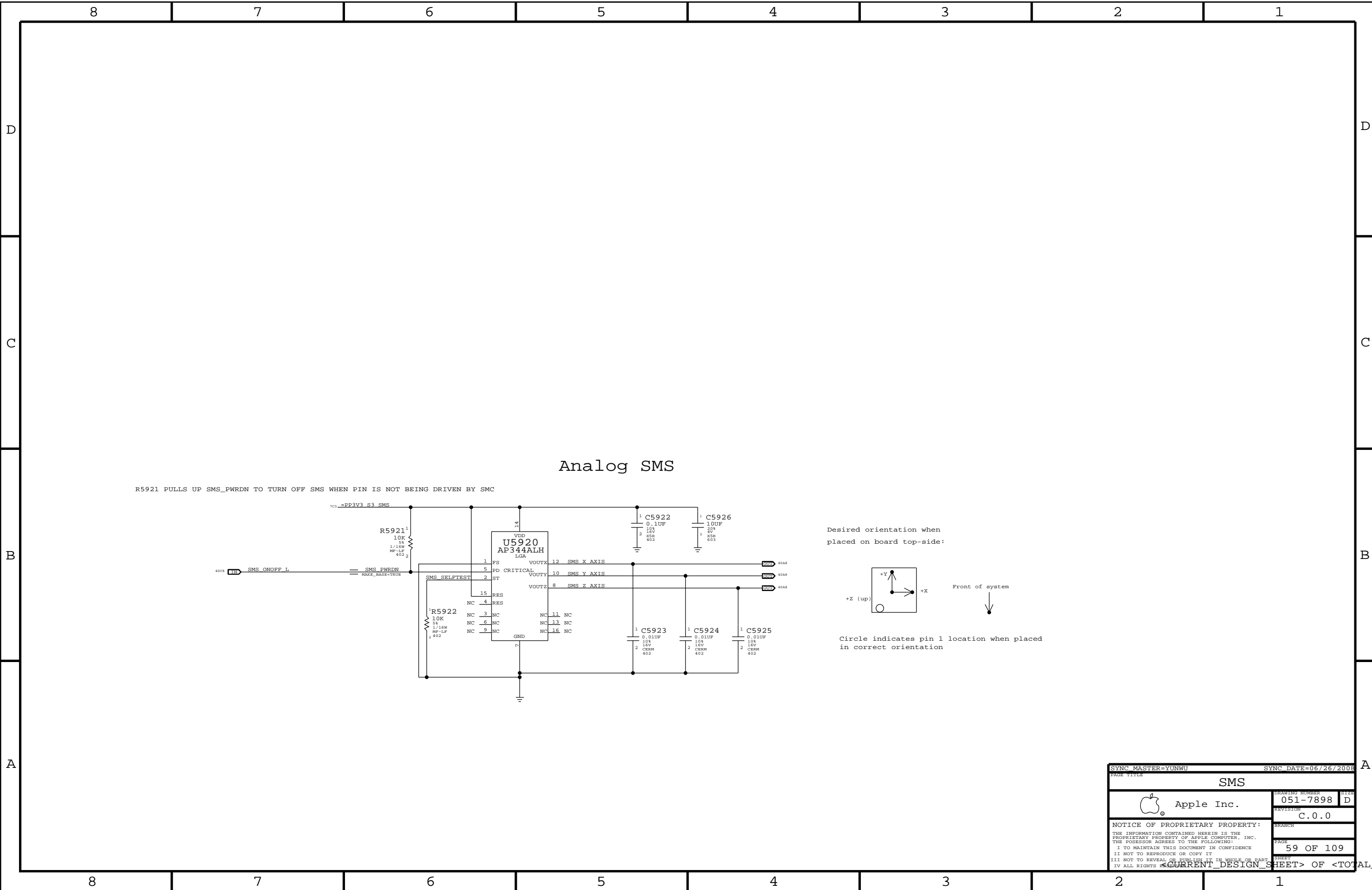
KEYBOARD BACKLIGHT DRIVING AND DETECTION



To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
 LOW = keyboard backlight present
 HIGH = keyboard backlight not present
 BOM OPTION: KBDLED_YES
 TURNED ON FOR BEST MLB CONFIG
 R5853 ALWAYS PRESENT

KBD BACKLIGHT CONNECTOR

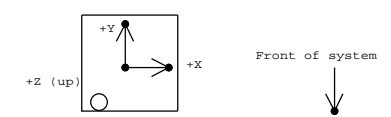
SYNC MASTER=YUAN.MA		SYNC DATE=05/09/2008	
PAGE TITLE			
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Analog SMS

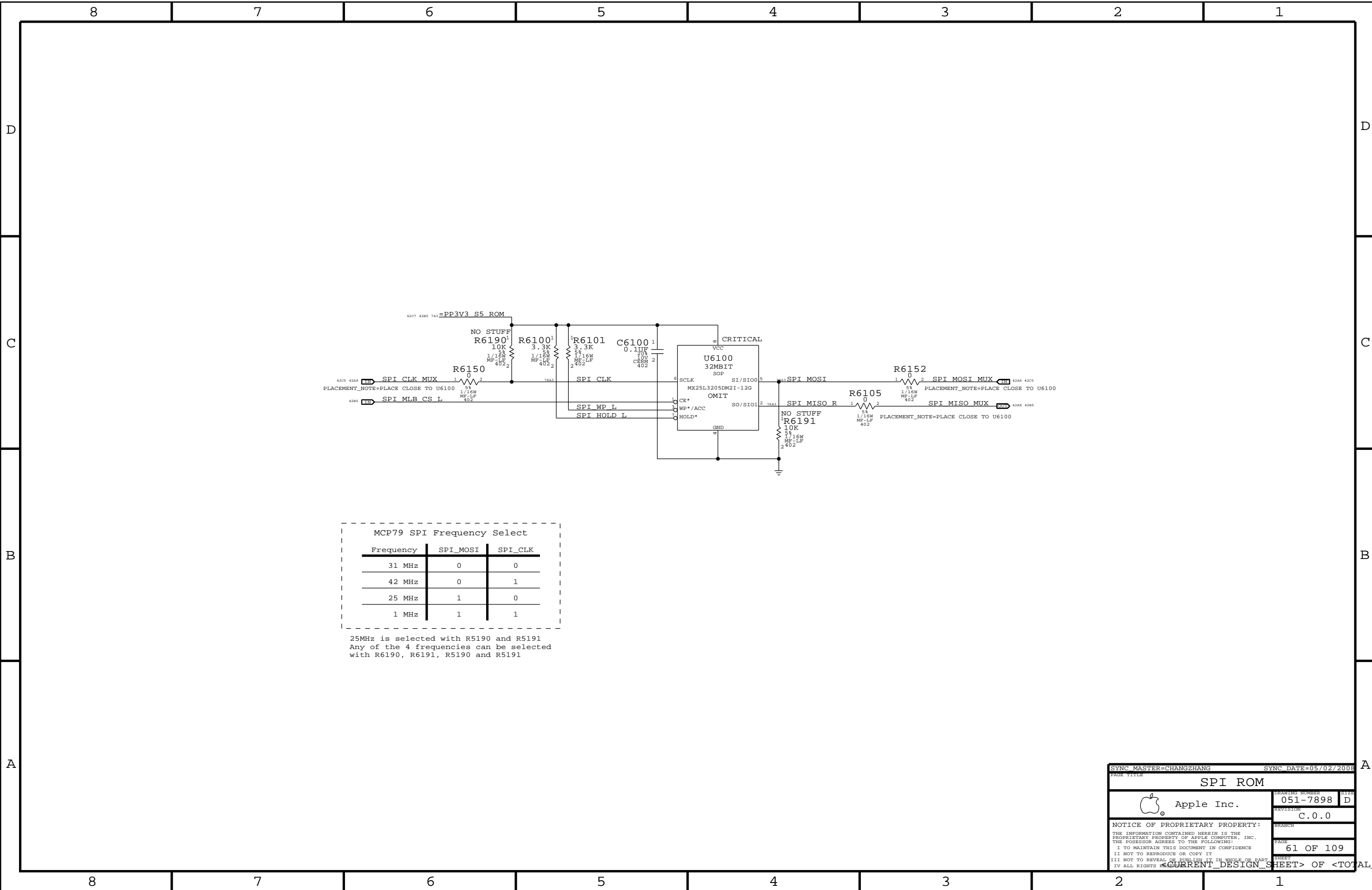
R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=YUNWU		SYNC DATE=06/26/2008	
SMS			
Apple Inc.		DRAWING NUMBER 051-7898	SIZE D
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		PAGE 59 OF 109	SHEET

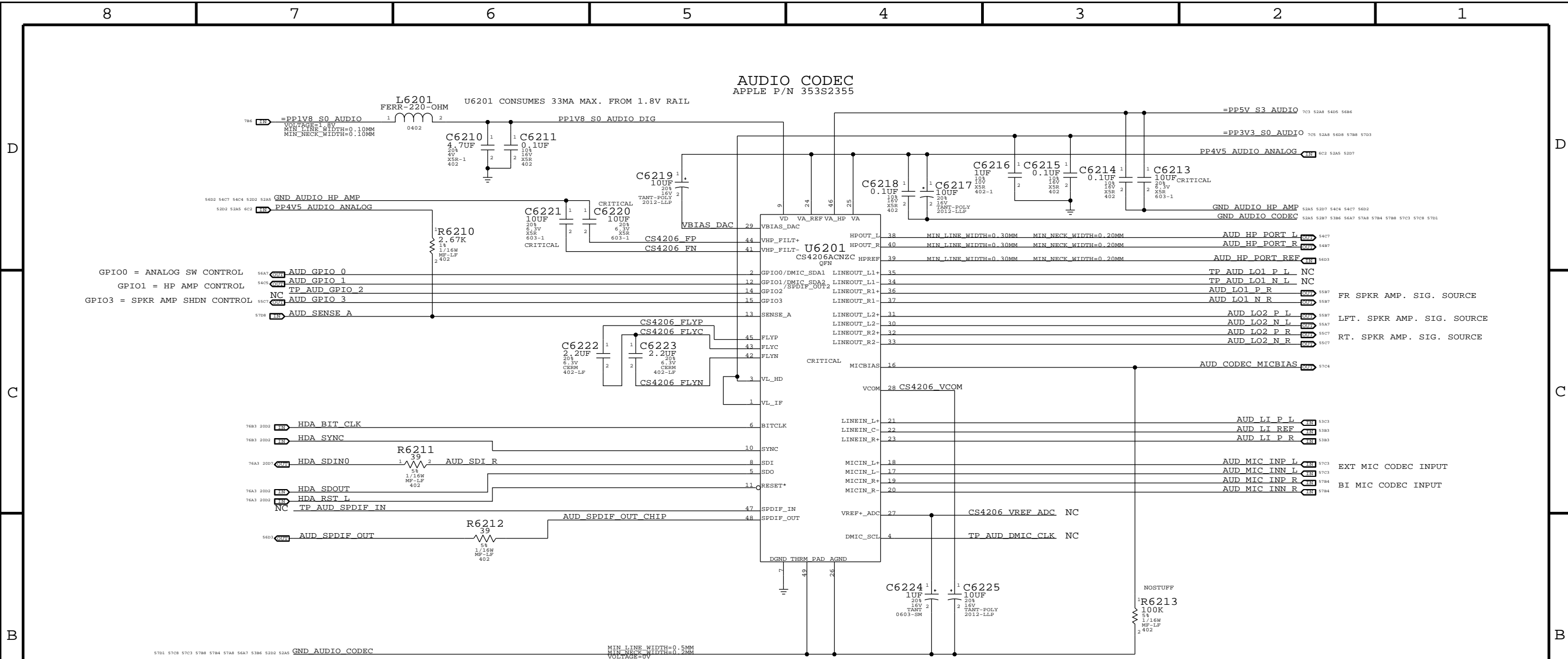


MCP79 SPI Frequency Select

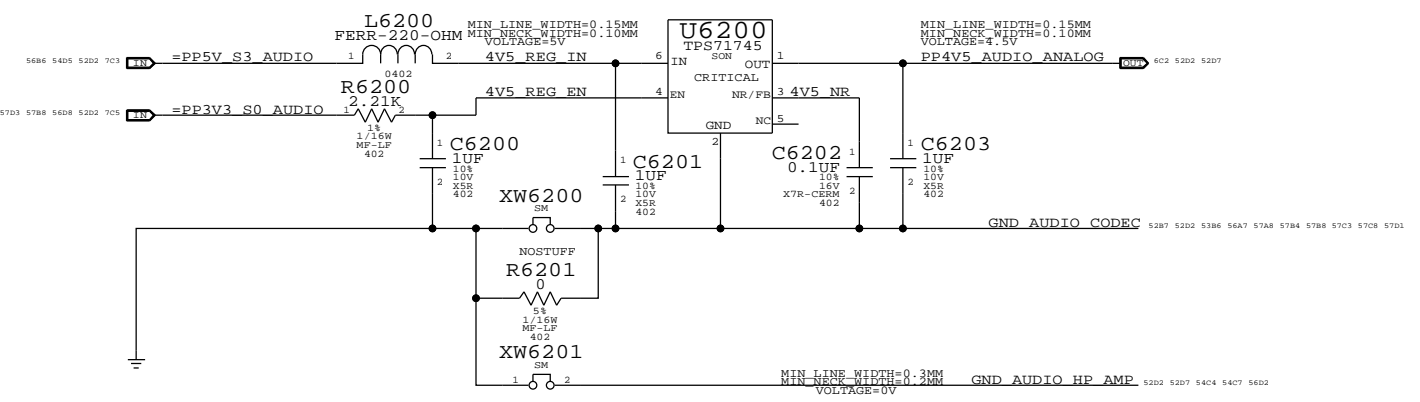
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
 Any of the 4 frequencies can be selected
 with R6190, R6191, R5190 and R5191

SYNC MASTER=CHANGZHANG		SYNC DATE=05/02/2008	
SPI ROM			
Apple Inc.		DRAWING NUMBER 051-7898	SIZE D
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4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2456



NOTES ON CODEC I/O
 DIFF FSINPUT= 2.45VRMS
 SE FSINPUT= 1.22VRMS
 DAC1 FSOUTPUT= 1.34VRMS
 DAC2/3 FSOUTPUTDIFF= 2.67VRMS
 DAC2/3 FSOUTPUTSE= 1.34VRMS

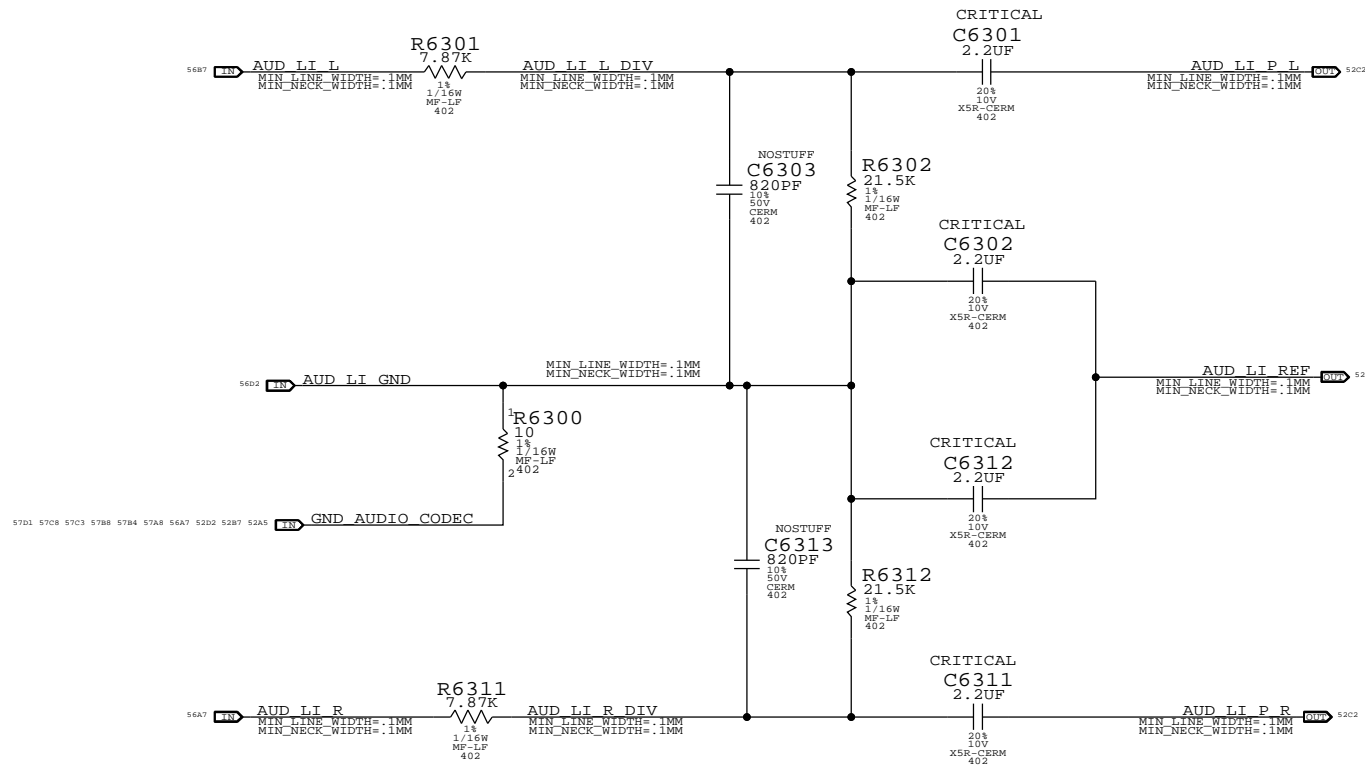
SYNC MASTER=AUDIO		SYNC DATE=03/04/2009	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
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SHEET		SHEET	

8 7 6 5 4 3 2 1

D
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A

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



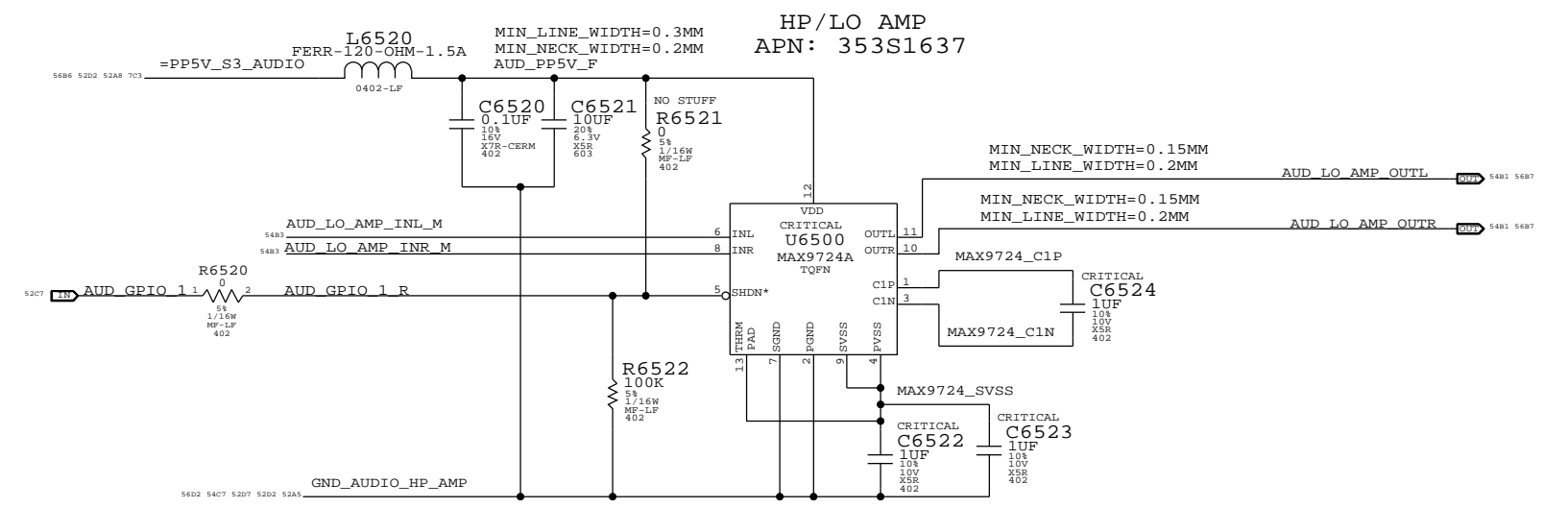
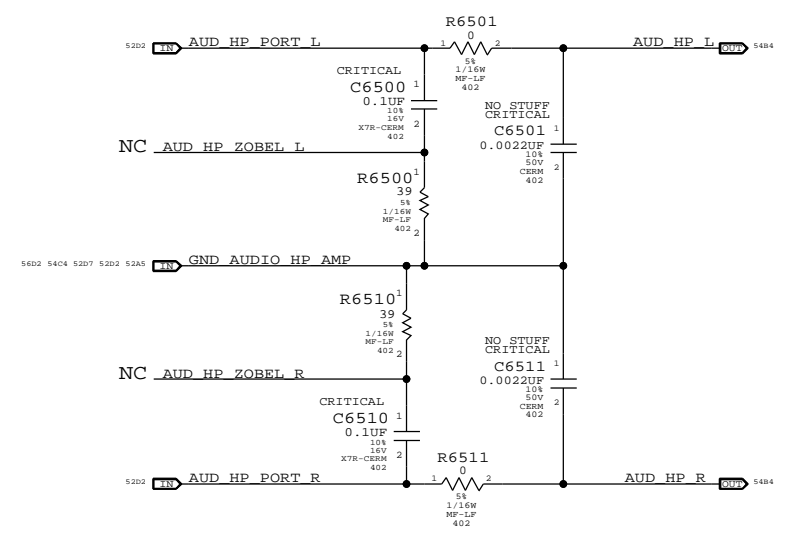
SYNC MASTER=AUDIO		SYNC DATE=01/31/2009	
PAGE TITLE AUDIO: LINE INPUT FILTER			
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8 7 6 5 4 3 2 1

D
C
B
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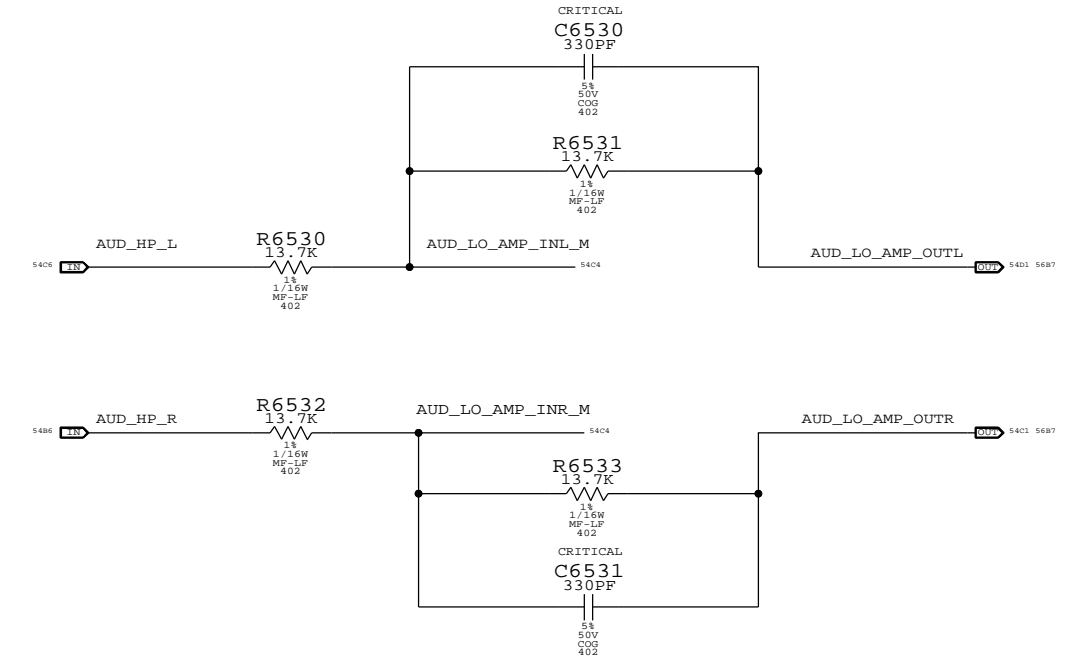
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



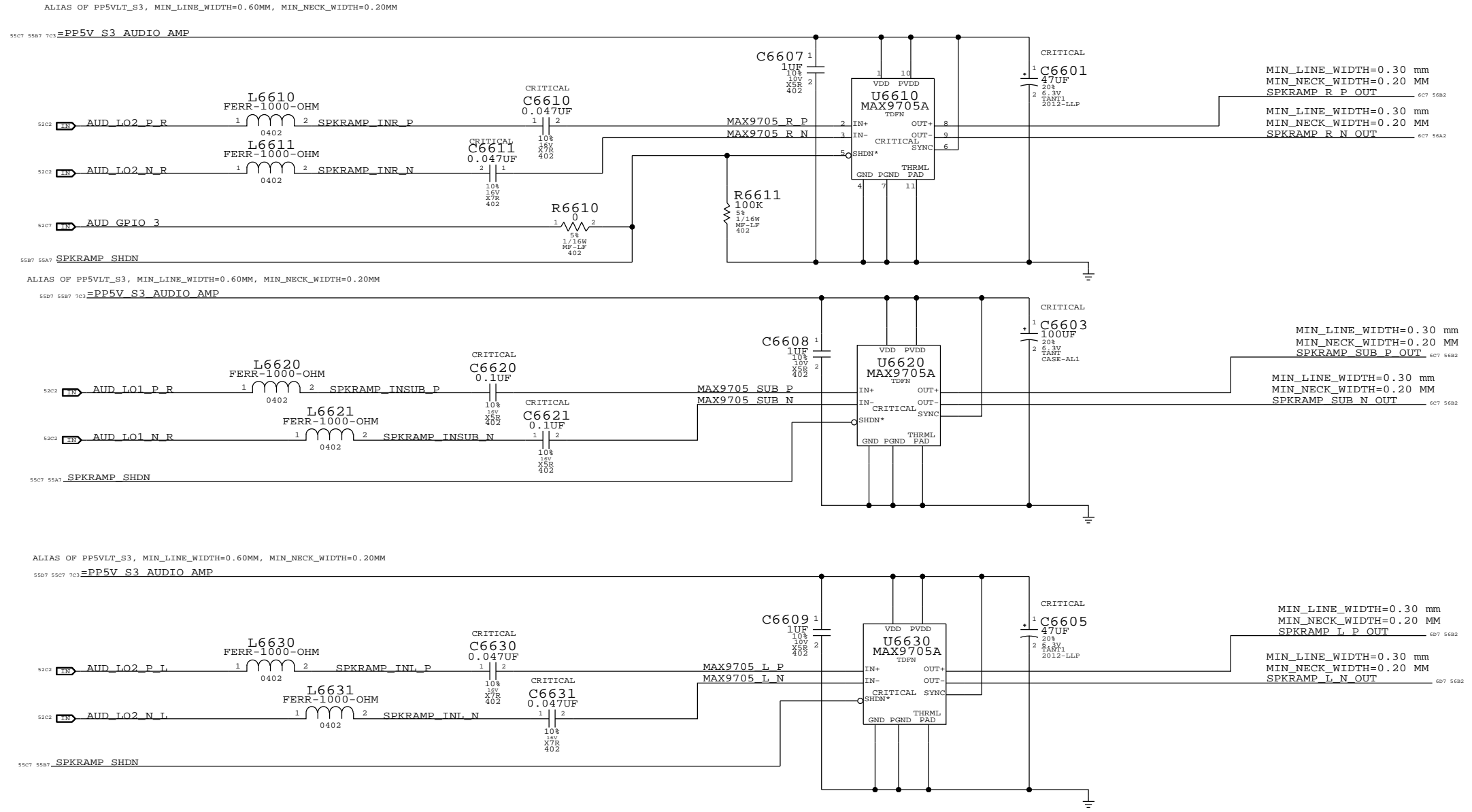
SYNC MASTER=AUDIO SYNC DATE=02/03/2009

PAGE TITLE		AUDIO: HEADPHONE FILTER	
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SATELLITE & SUB TWEETER AMPLIFIER

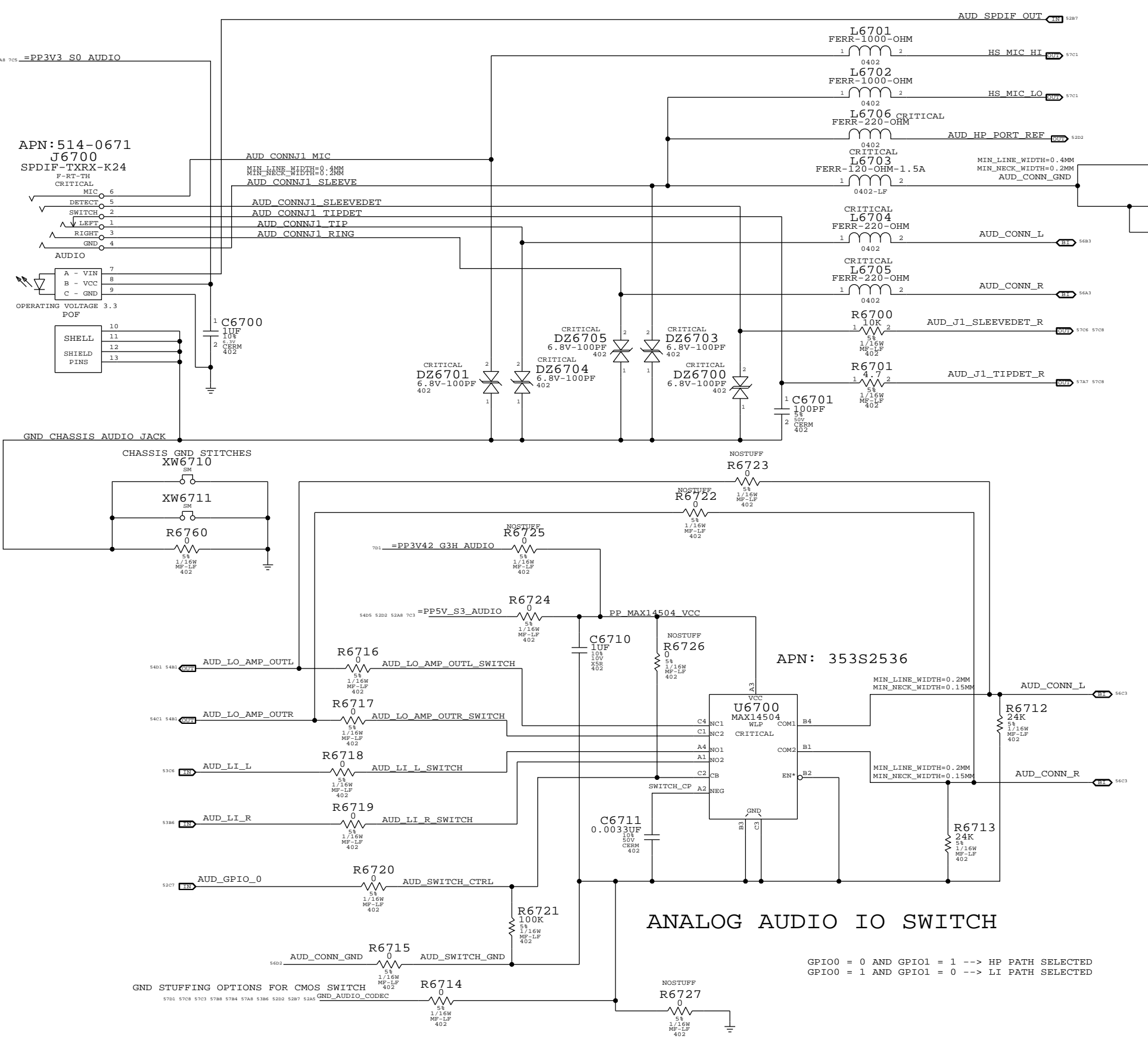
APN:353S2524

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 6DB

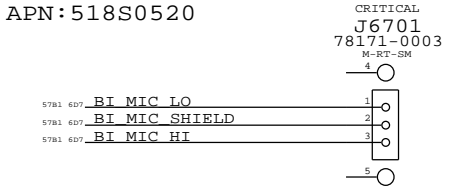


SYNC MASTER=AUDIO		SYNC DATE=12/18/2008	
PAGE TITLE			
AUDIO: SPEAKER AMP			
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SHEET			

AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX

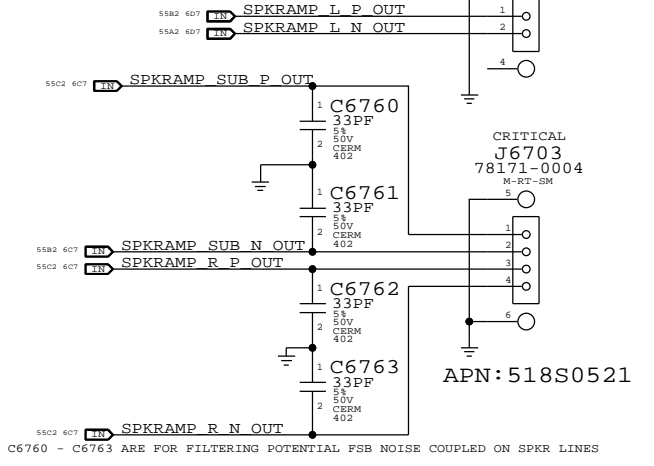


MIC CONNECTOR
APN: 518S0520



SPEAKER CONNECTOR

APN: 518S0519



ANALOG AUDIO IO SWITCH

GPIO0 = 0 AND GPIO1 = 1 --> HP PATH SELECTED
 GPIO0 = 1 AND GPIO1 = 0 --> LI PATH SELECTED

SYNC MASTER=AUDIO		SYNC DATE=03/20/2009	
PAGE TITLE: AUDIO: JACK			
Apple Inc.		DRAWING NUMBER: 051-7898	SIZE: D
		REVISION: C.0.0	
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		PAGE: 67 OF 109	SHEET: 1

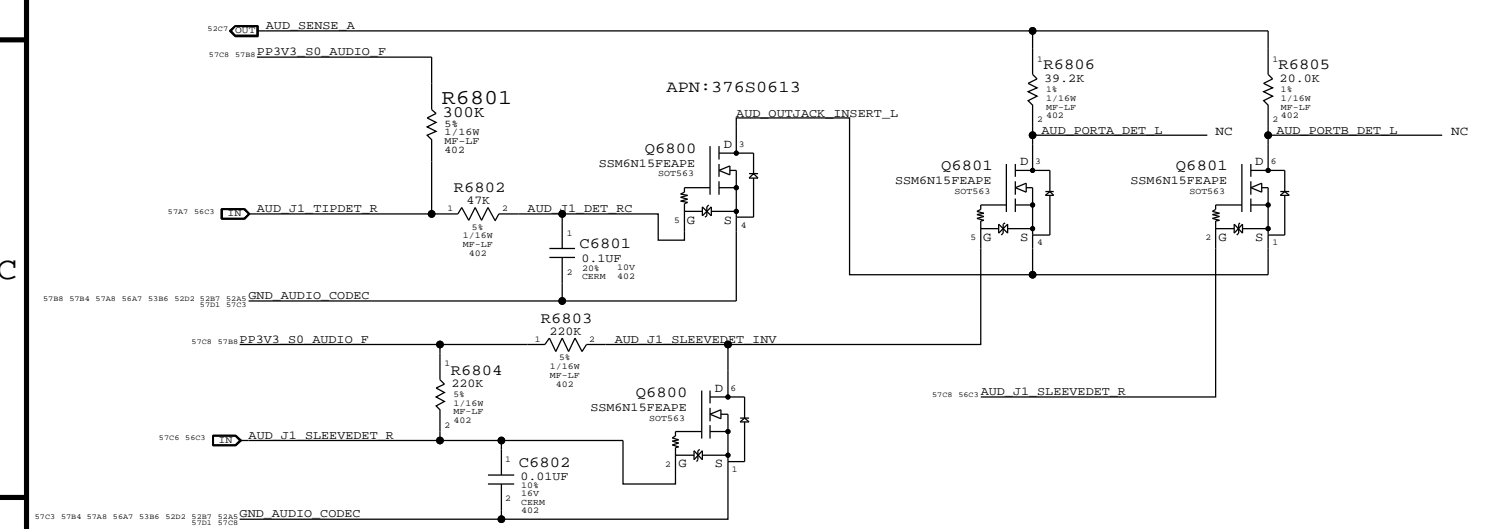
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A) AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

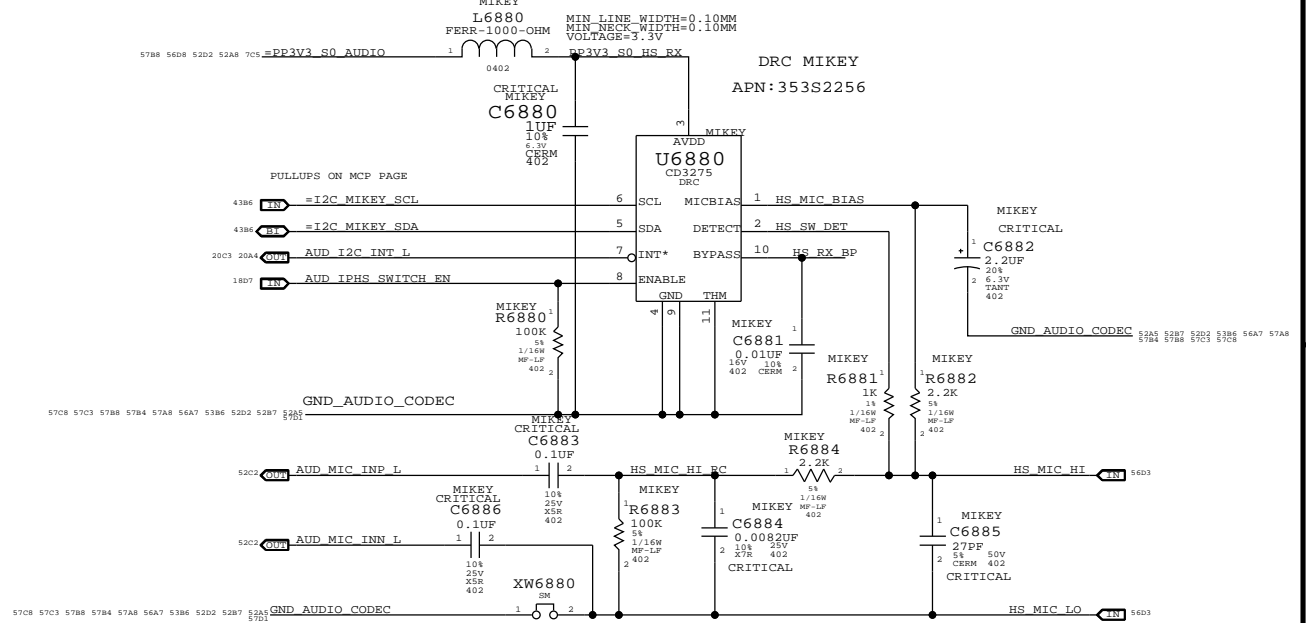
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

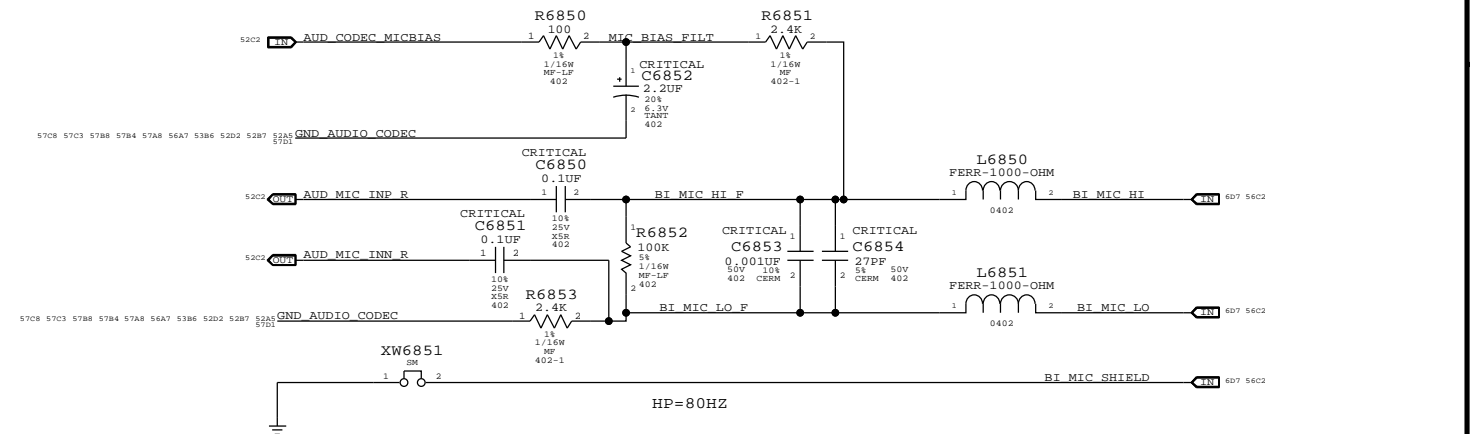
PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)



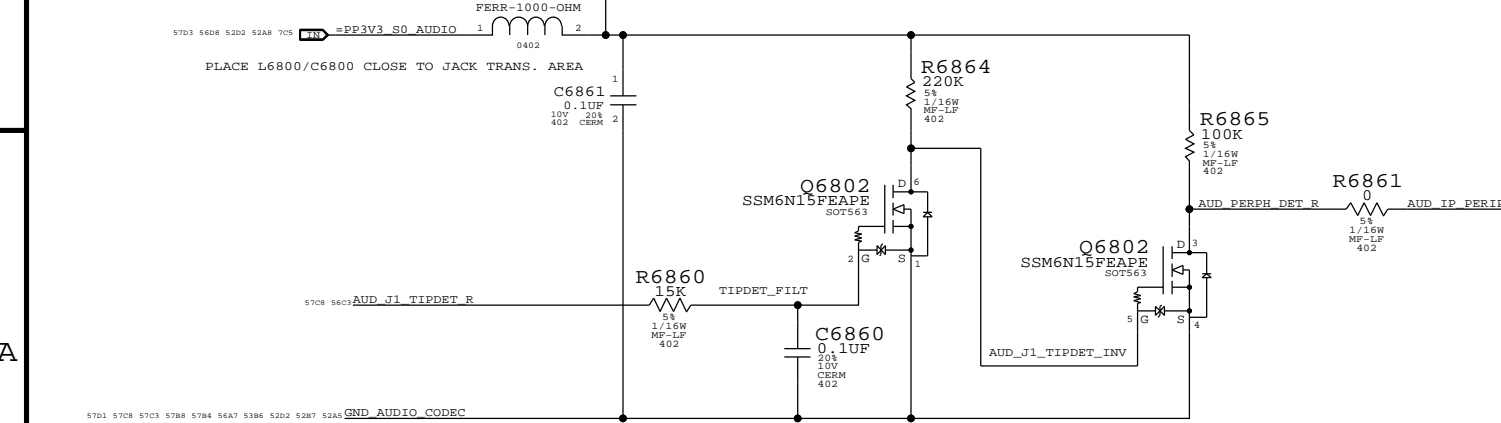
PORT B LEFT (HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT (BUILT-IN MIC)



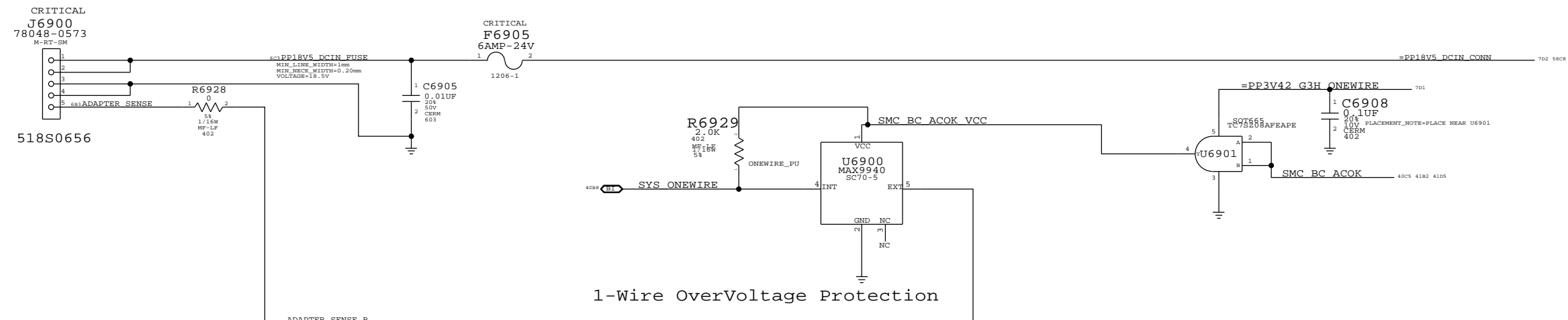
EXTRACTION NOTIFICATION CKT



SYNC MASTER=AUDIO SYNC DATE=03/20/2009
PAGE TITLE: AUDIO: JACK TRANSLATORS

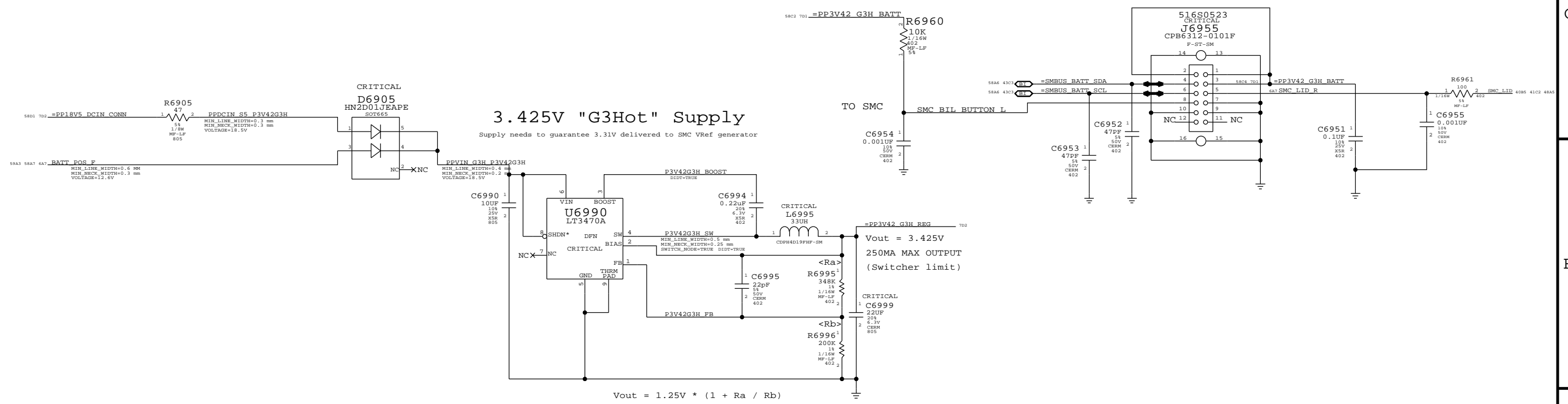
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PAGE: 68 OF 109	SHEET: 1

MagSafe DC Power Jack



1-Wire OverVoltage Protection

BIL CONNECTOR

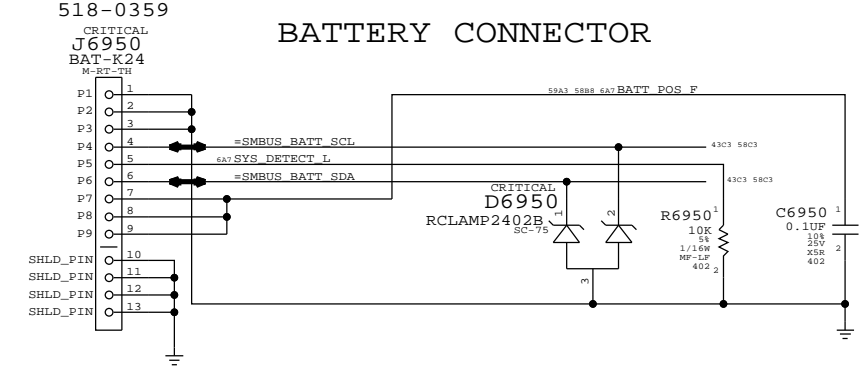


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

BATTERY CONNECTOR

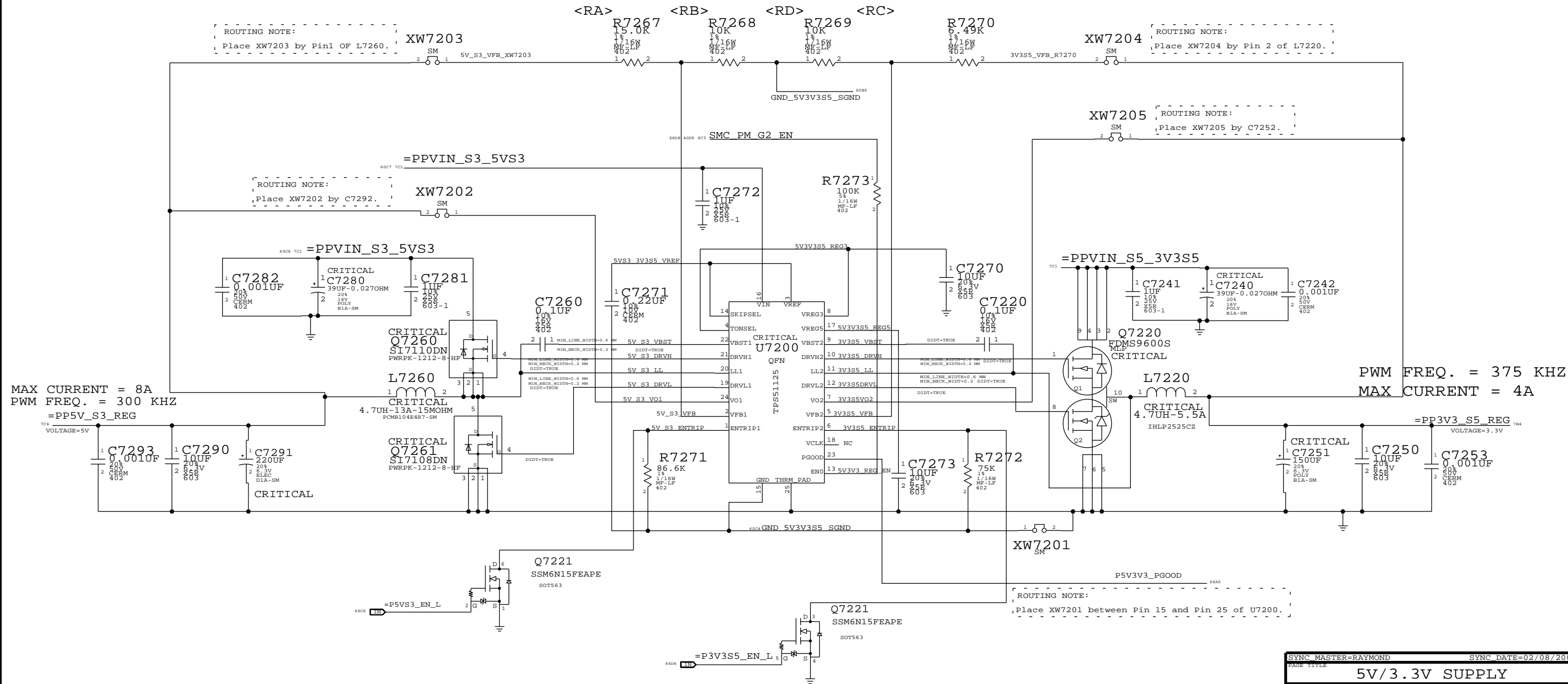


SYNC MASTER=YUNWU		SYNC DATE=12/11/2008	
DC-In & Battery Connectors			
Apple Inc.		051-7898	D
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5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



MAX CURRENT = 8A
 PWM FREQ. = 300 KHZ
 =PP5V_S3_REG

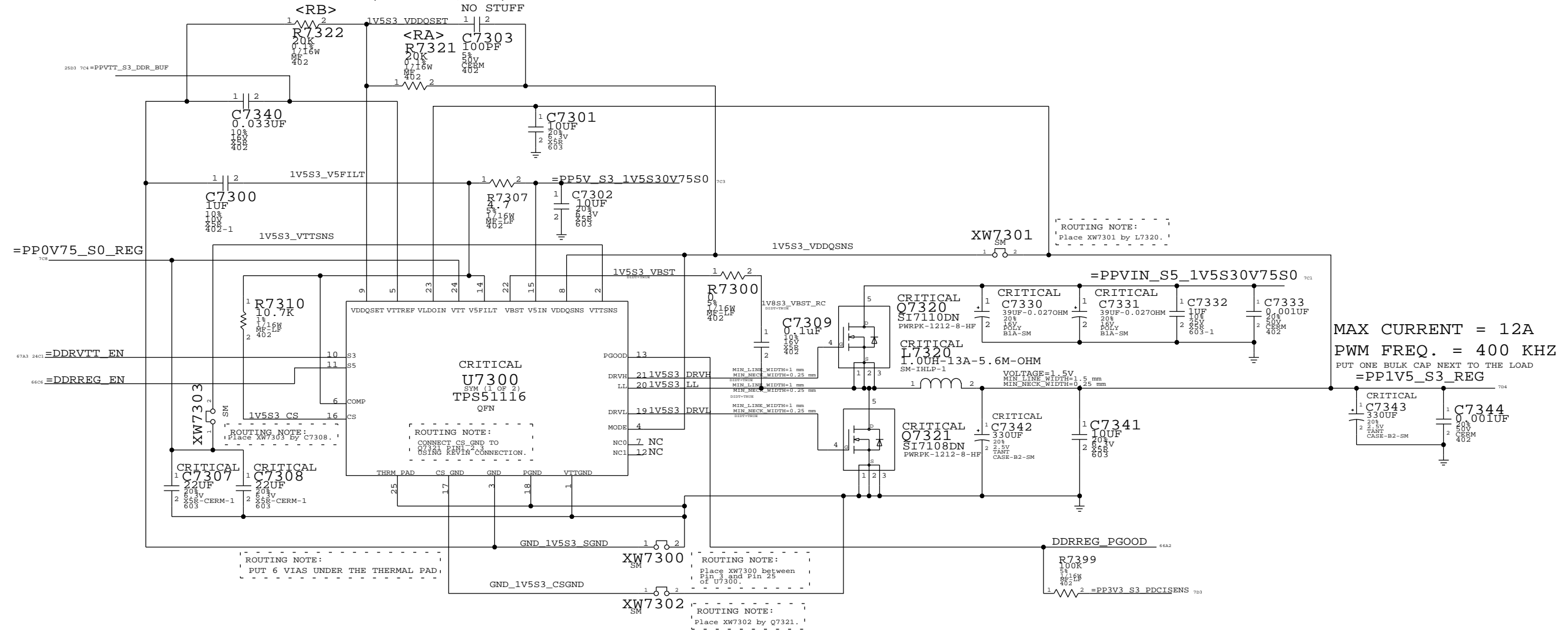
PWM FREQ. = 375 KHZ
 MAX CURRENT = 4A

SEPARATED MASTER PGOOD FOR BOTH 5V AND 3V3.

SYNC MASTER=RAYMOND		SYNC DATE=02/08/2008	
5V/3.3V SUPPLY			
Apple Inc.		DRAWING NUMBER	051-7898 D
		REVISION	C.0.0
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1.5V/0.75V (DDR3) POWER SUPPLY

$$V_{OUT} = 0.75V * (1 + R_A / R_B)$$



STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC MASTER=RAYMOND SYNC DATE=01/31/2008

1.5V/0.75V DDR3 SUPPLY



Apple Inc.

DRAWING NUMBER
051-7898 D

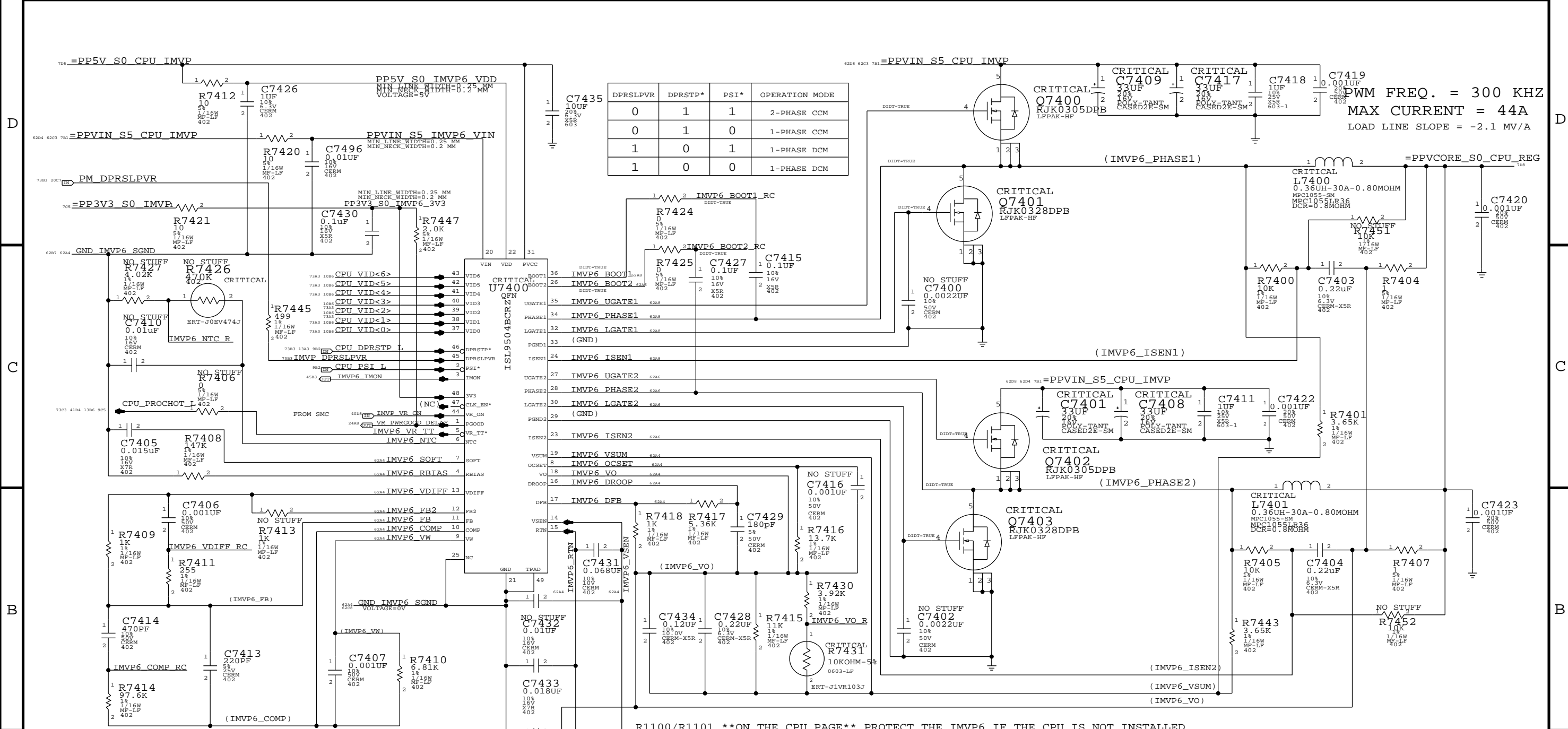
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73 OF 109

SHEET
<CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>



NOTE 1: C7432, C7433 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCore Regulator

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIA	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

SYNC MASTER=RAYMOND SYNC DATE=01/31/2008

IMVP6 CPU VCore Regulator

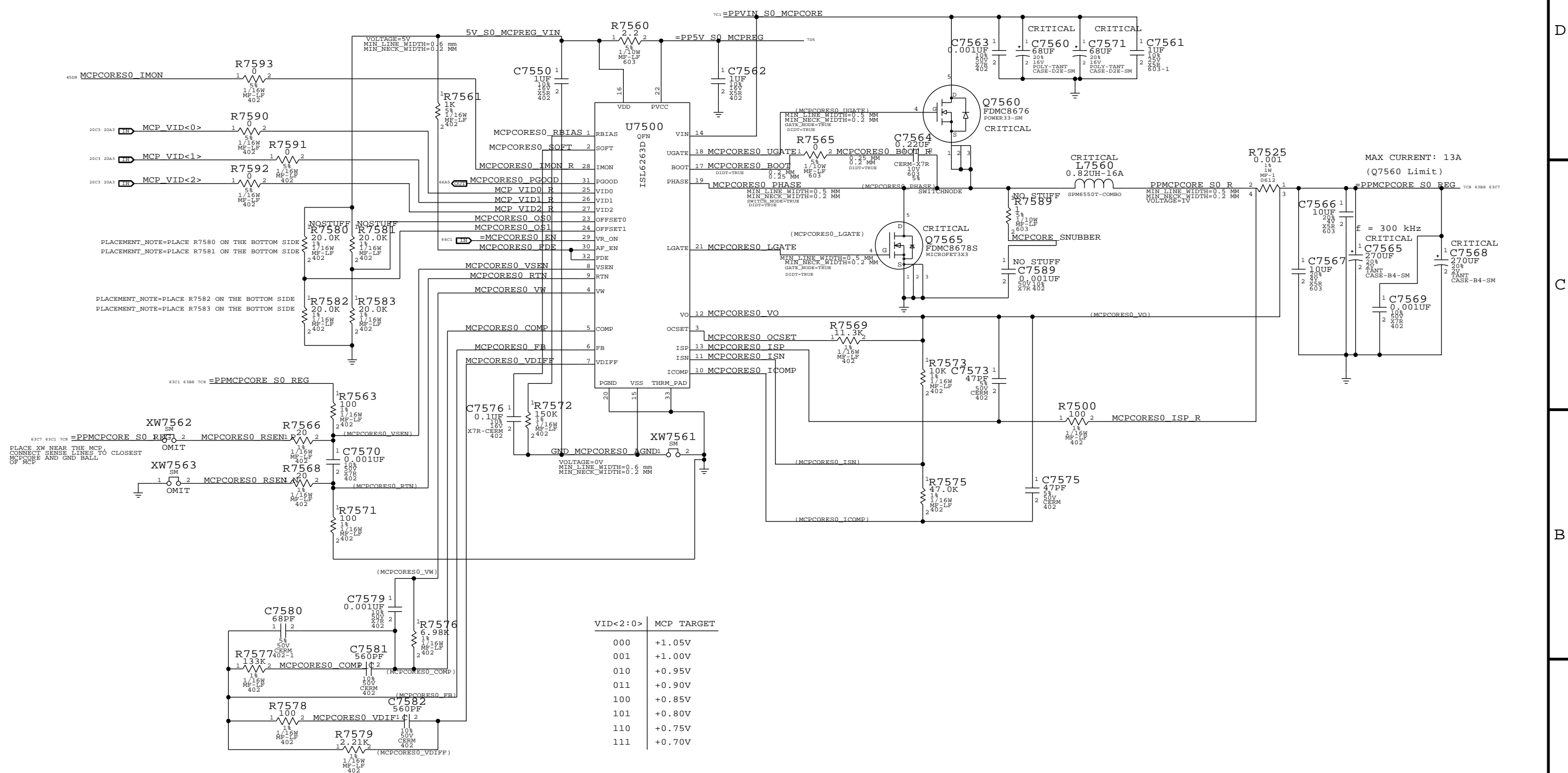
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MCP VCORE POWER SUPPLY



SYNC MASTER=K19 MLB SYNC DATE=12/10/2008

MCP CORE REGULATOR

Apple Inc.

051-7898 D

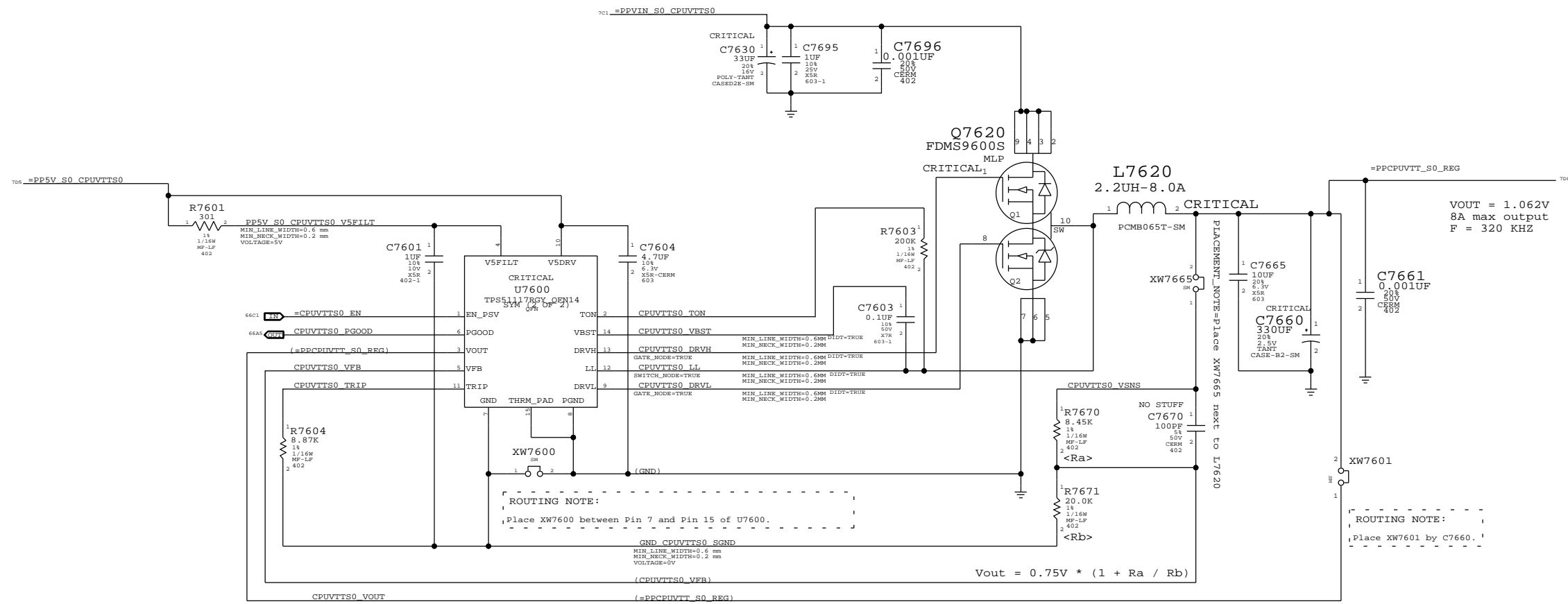
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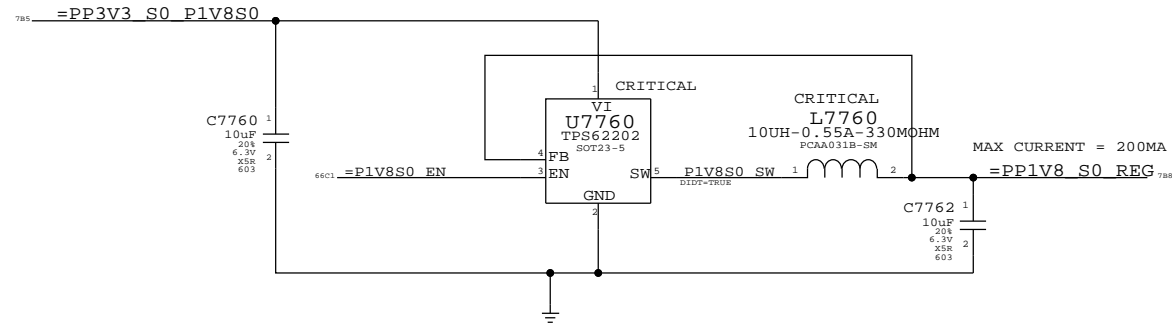
CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

CPUVTT POWER SUPPLY

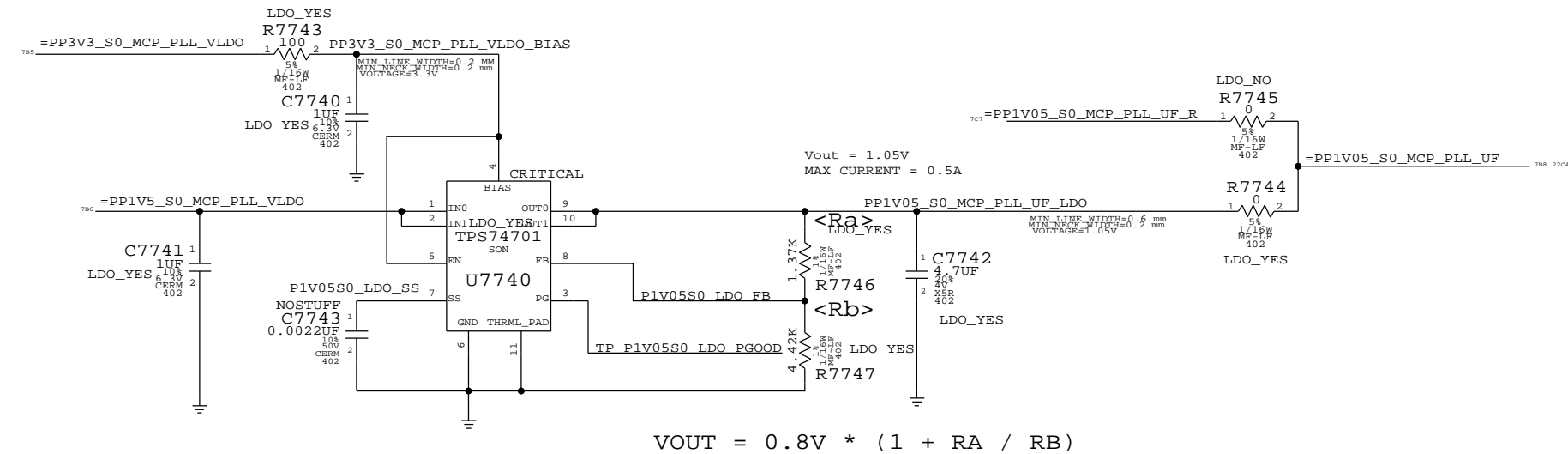


SYNC MASTER=RAYMOND		SYNC DATE=02/08/2008	
CPU VTT(1.05V) SUPPLY			
Apple Inc.		051-7898	D
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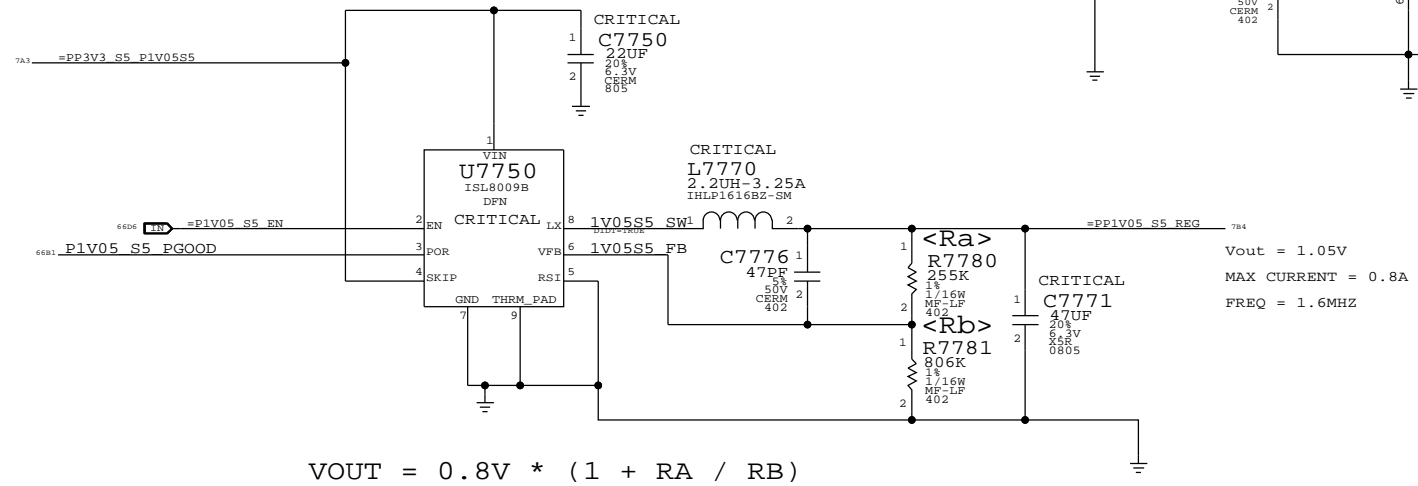
1.8V S0 SWITCHER



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY

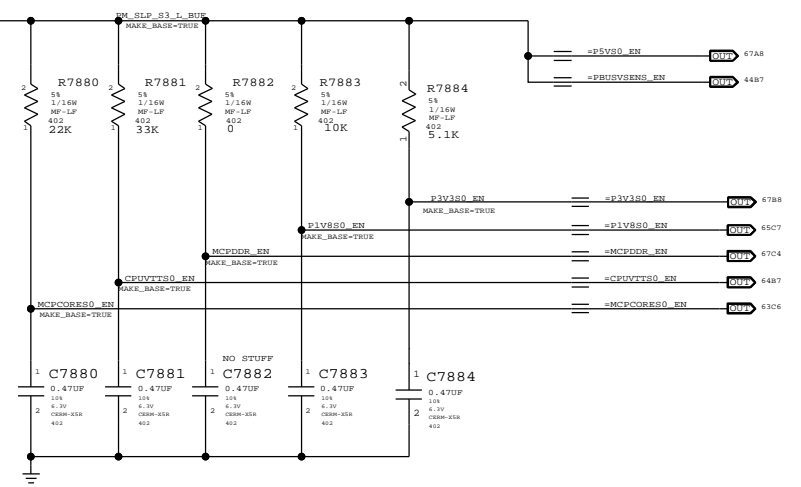
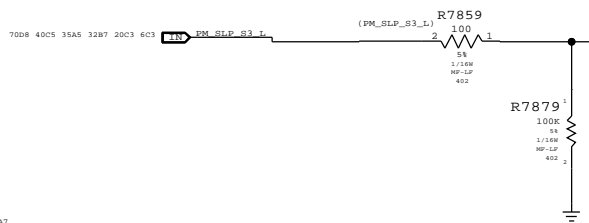
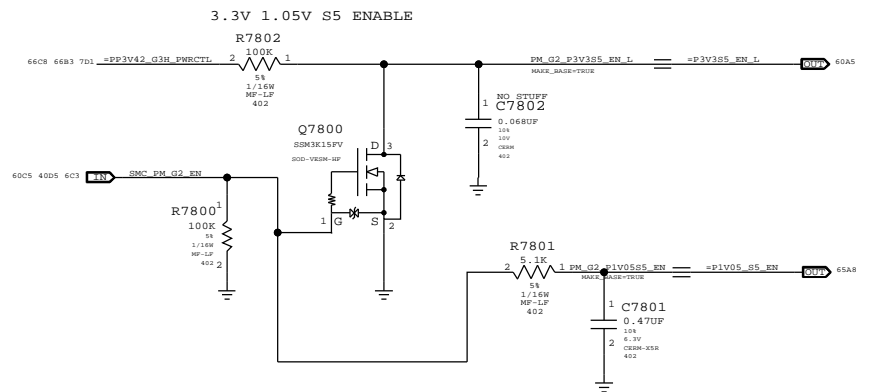


SYNC MASTER=RAYMOND		SYNC DATE=01/23/2008	
PAGE TITLE			
MISC POWER SUPPLIES			
Apple Inc.		DRAWING NUMBER	051-7898 D
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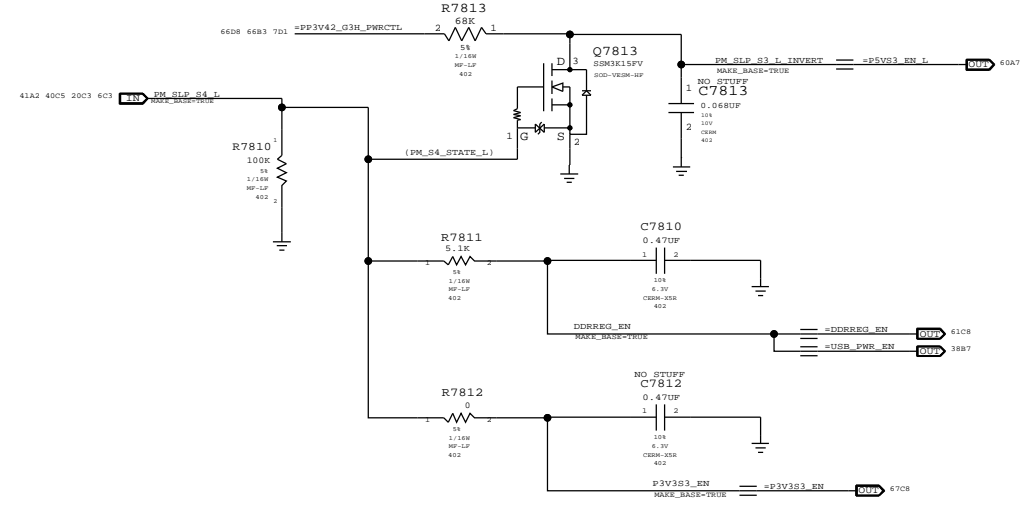
Power Control Signals

State	PMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

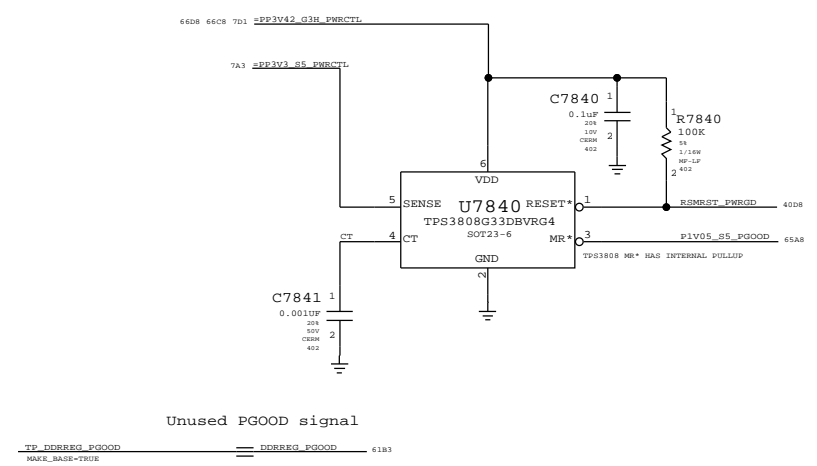
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT, MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



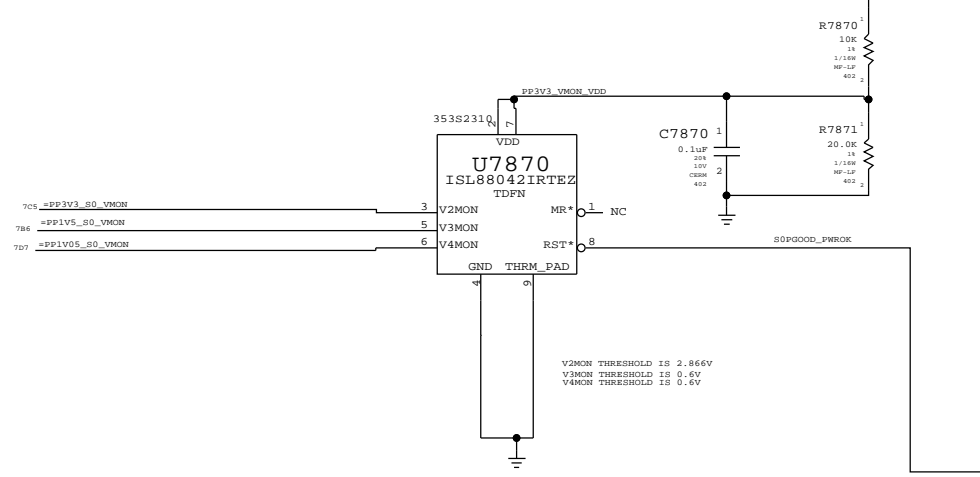
S3 ENABLE



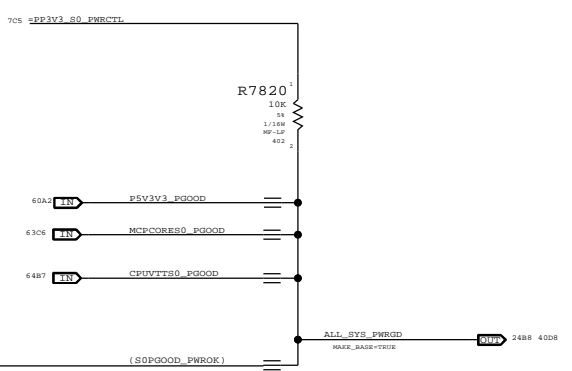
VOLTAGE MONITOR



3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



OTHER S0 RAILS PGOOD



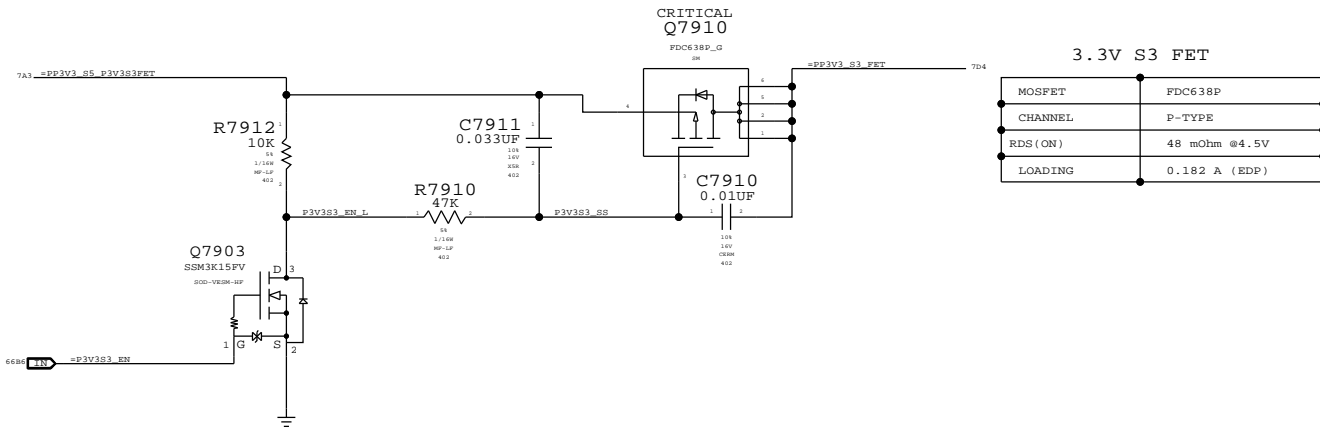
SYNC MASTER=YUAN.MA SYNC DATE=12/11/2008

POWER SEQUENCING

Apple Inc.	DRAWING NUMBER 051-7898
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	PAGE 78 OF 109
	SHEET

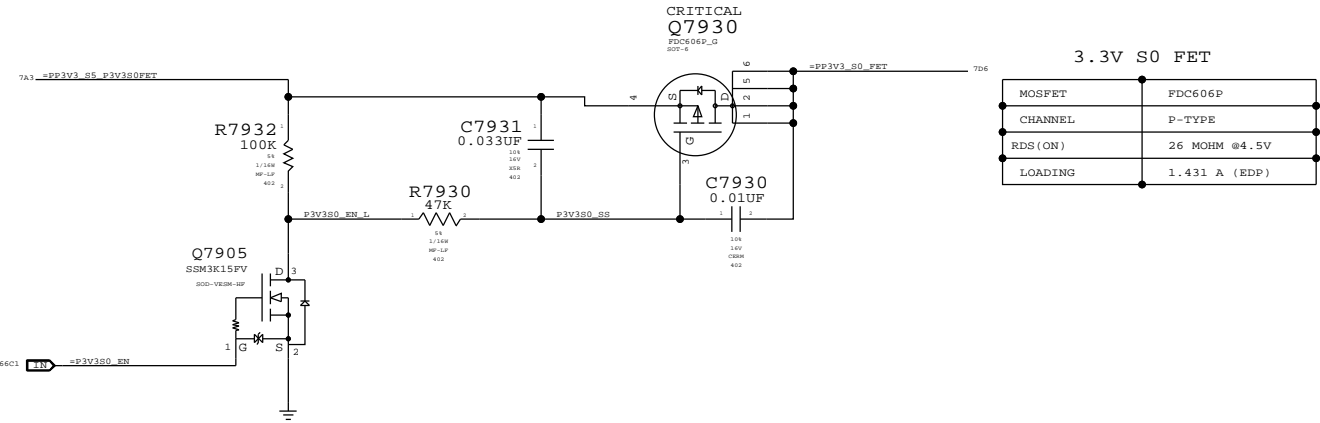
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3.3V S3 FET



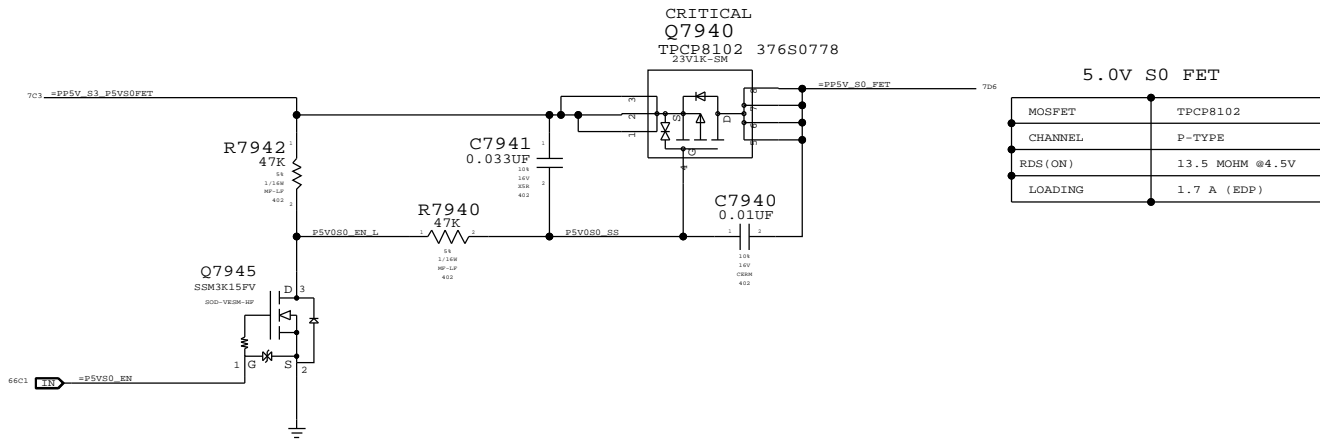
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

3.3V S0 FET



3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

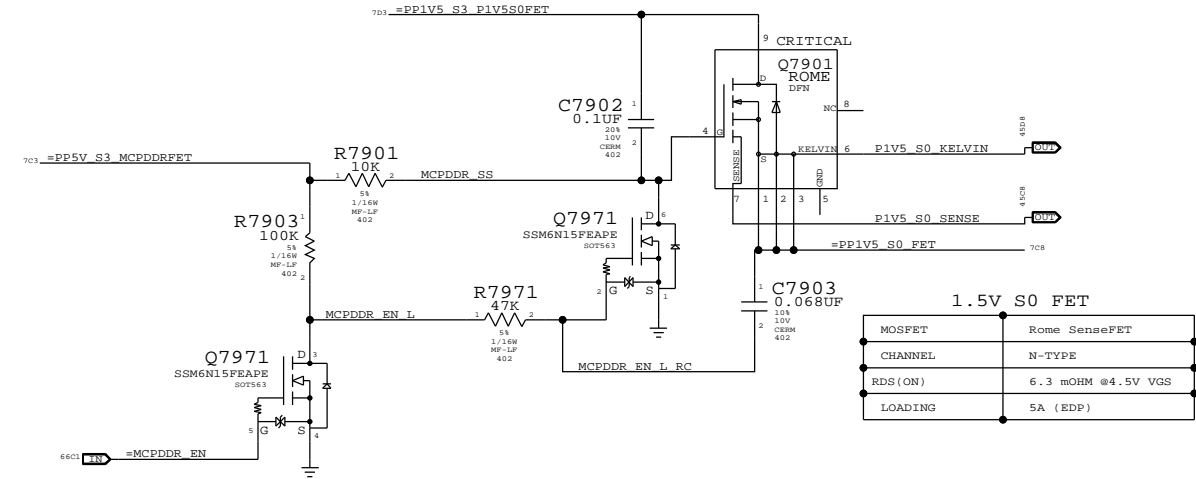
5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	13.5 MOHM @4.5V
LOADING	1.7 A (EDP)

1.5V S0 FET

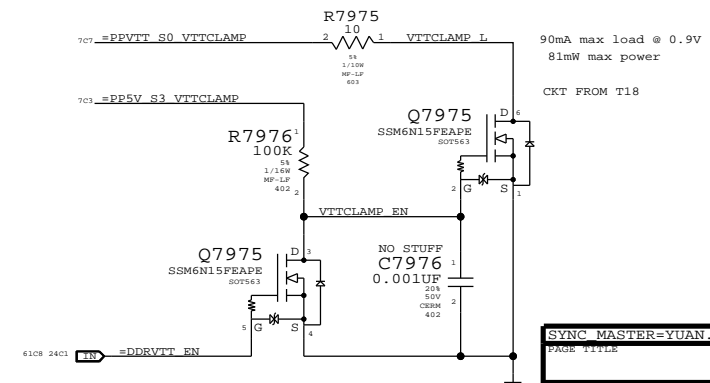
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 MOHM @4.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



90mA max load @ 0.9V
81mW max power
CKT FROM T18

SYNC MASTER=YUAN.MA SYNC DATE=12/11/2008

POWER FETS

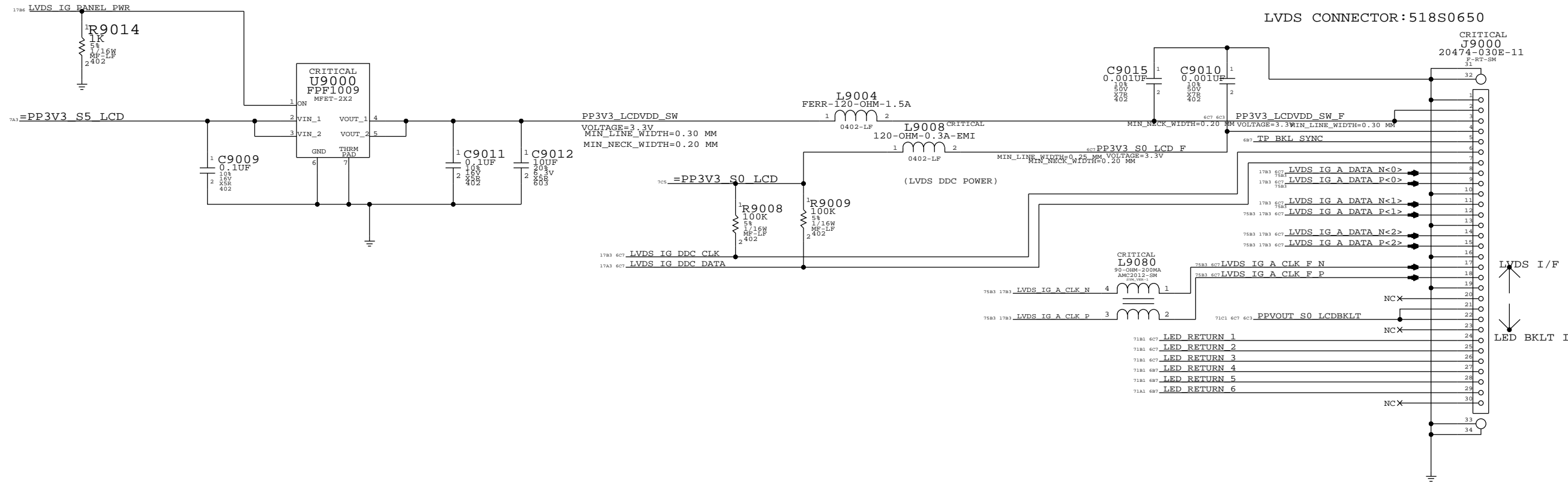
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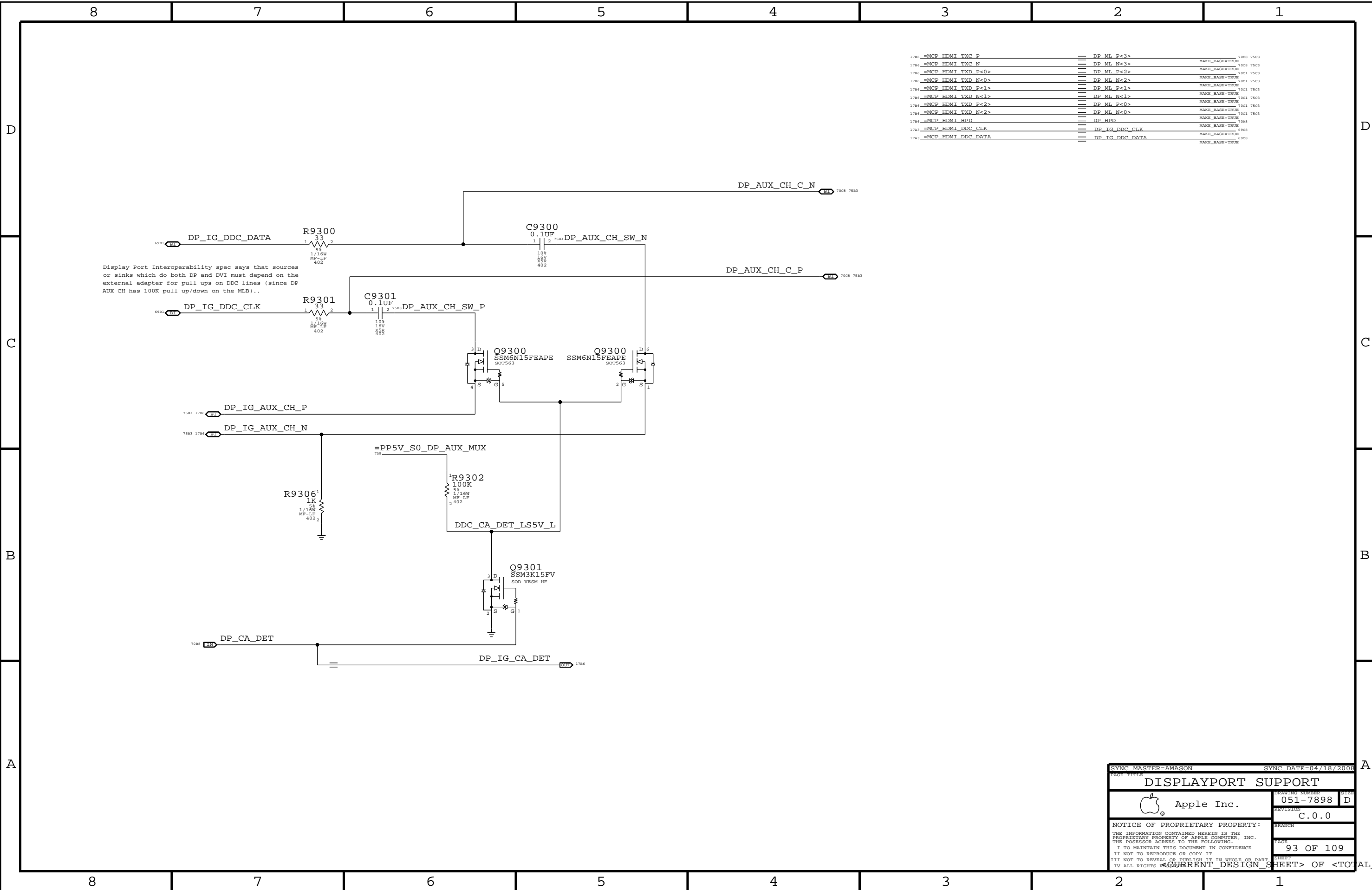
79 OF 109 SHEETS
CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

LCD CONNECTOR
LVDS CONNECTOR: 518S0650



SYNC MASTER=NMARTIN		SYNC DATE=04/04/2008	
LVDS CONNECTOR			
Apple Inc.		DESIGN NUMBER	SIZE
		051-7898	D
		REVISION	
		C.0.0	
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		PAGE	
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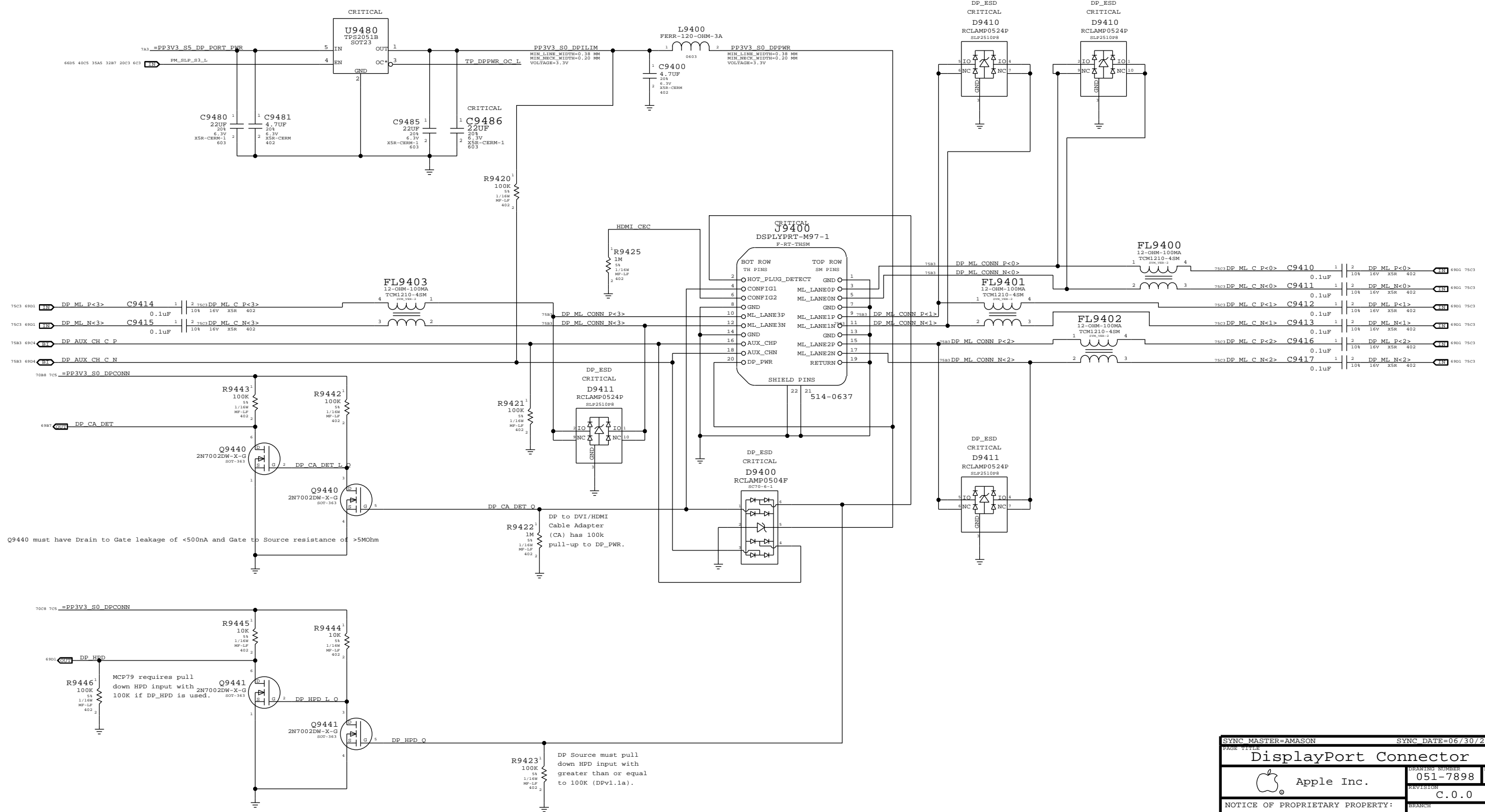
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1786 =MCP HDMI TXC P == DP ML P<3> MAKE_BASE=TRUE 70C8 75C3
1786 =MCP HDMI TXC N == DP ML N<3> MAKE_BASE=TRUE 70C8 75C3
1786 =MCP HDMI TXD P<0> == DP ML P<2> MAKE_BASE=TRUE 70C1 75C3
1786 =MCP HDMI TXD N<0> == DP ML N<2> MAKE_BASE=TRUE 70C1 75C3
1786 =MCP HDMI TXD P<1> == DP ML P<1> MAKE_BASE=TRUE 70C1 75C3
1786 =MCP HDMI TXD N<1> == DP ML N<1> MAKE_BASE=TRUE 70C1 75C3
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1786 =MCP HDMI TXD N<2> == DP ML N<0> MAKE_BASE=TRUE 70C1 75C3
1786 =MCP HDMI HPD == DP HPD MAKE_BASE=TRUE 70A8
17A3 =MCP HDMI DDC CLK == DP IG_DDC_CLK MAKE_BASE=TRUE 69C8
17A3 =MCP HDMI DDC DATA == DP IG_DDC_DATA MAKE_BASE=TRUE 69C8

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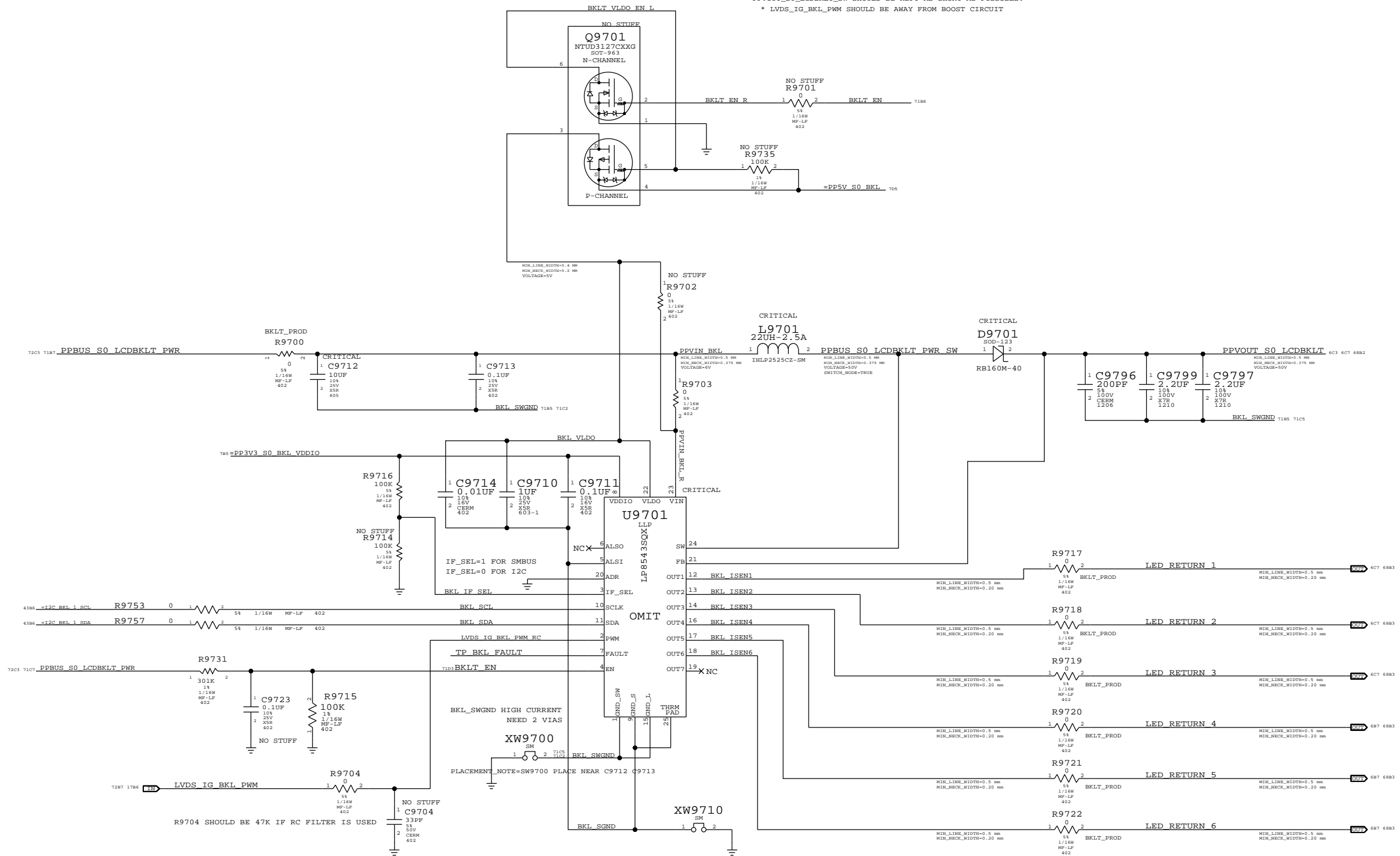
SYNC MASTER=AMASON		SYNC DATE=04/18/2008	
DISPLAYPORT SUPPORT			
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		SHEET <CURRENT DESIGN SHEET> OF <TOTAL DESIGN SHEETS>	

Port Power Switch



SYNC MASTER=AMASON		SYNC DATE=06/30/2008	
DisplayPort Connector			
Apple Inc.		DRAWING NUMBER	051-7898 D
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		PAGE	94 OF 109

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
 *PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
 * LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	6	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		BKLT_ENG
116S0005	1	RES,1/16W,0.1 OHM,1%,0402,SM	R9700		BKLT_ENG

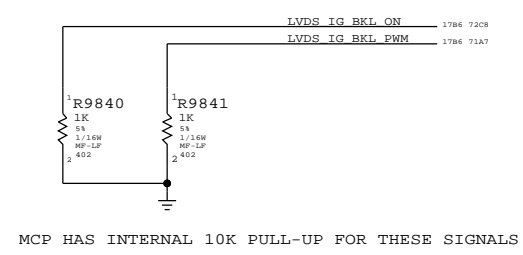
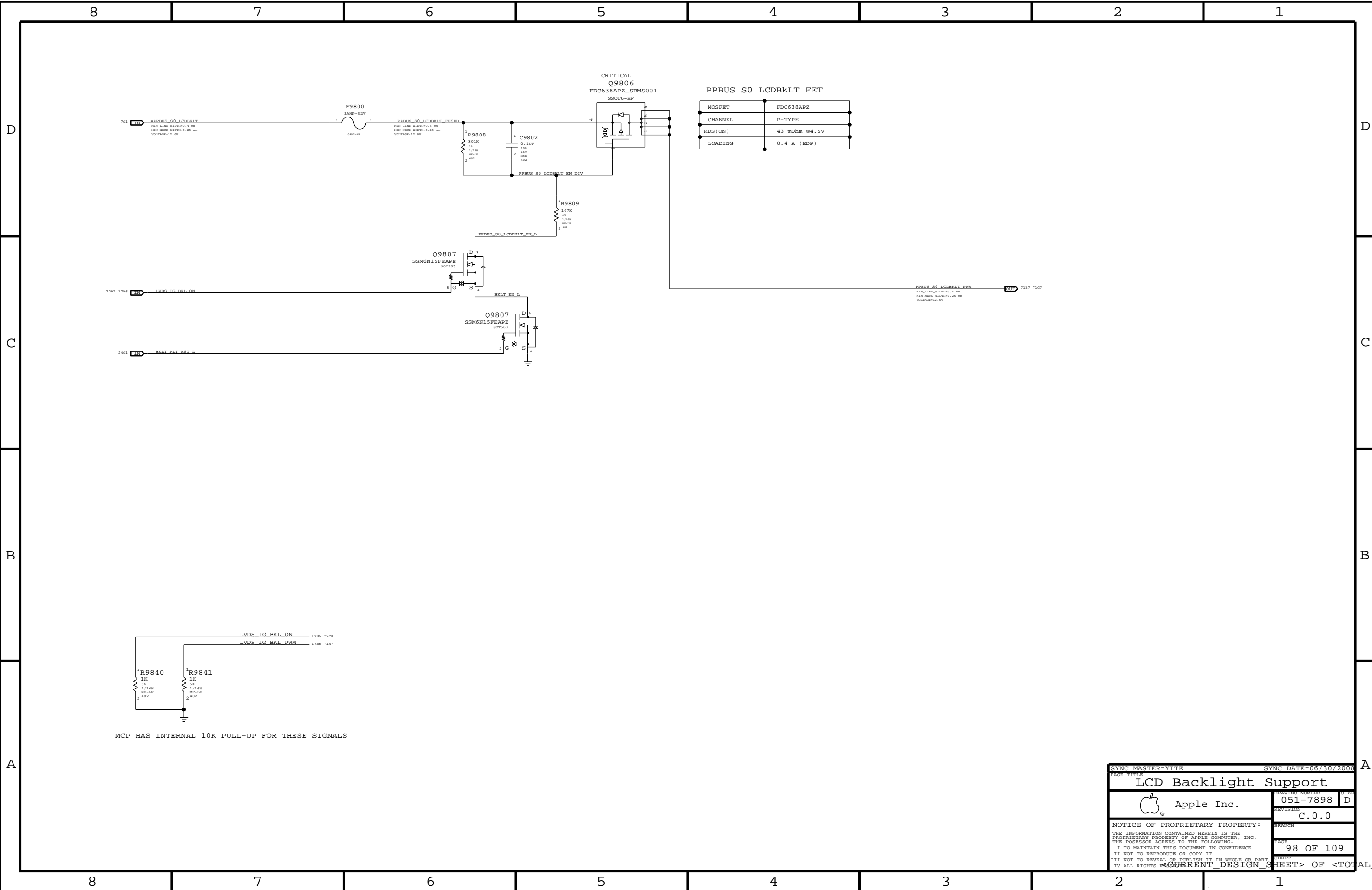
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,MIT LED BKLT CTRLR,QFN24,PROD	U9701	CRITICAL	

SYNC MASTER=KIRAN SYNC DATE=12/05/2008

LCD BACKLIGHT DRIVER

Apple Inc.
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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFPPAIR	=1:1_DIFPPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2k_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4k_DIELECTRIC	?
FSB_DSTB	*	=3k_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5k_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3k_DIELECTRIC	?
FSB_ADSTB	*	=2k_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4k_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3k_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right. Signals within each 4x group should be matched within 5 ps of strobe. DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps. Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s. DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right. Signals within each 2x group should be matched within 20 ps. ADTSTB#s should be matched +/- 300 ps. Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSTB#.

FSB 1X signals shown in signal table on right. Signals within each 1x group should be matched to CPU clock, +/-1000 mils. Design Guide recommends each strobe/signal group is routed on the same layer. Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2k_DIELECTRIC	?
CPU_BMIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFPPAIR PRIMARY GAP	DIFPPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP	=100_OHM_DIFP

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3k_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4k_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	904 1303
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	904 1306
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	904 1306
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	904 1306
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	984 904 1303 1303
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	984 1306
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	984 1306
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	984 1306
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	902 1303 1303
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	902 1306
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	902 1306
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	902 1306
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	982 902 1303
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	982 1306
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	982 1306
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	982 1306
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	908 1306 1306
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	908 1386
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	908 1386
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	908 908 1306
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	908 1386
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	906 1386
FSB_BREQ0	FSB_50S	FSB_1X	FSB BREQ0 L	906 1386
FSB_BREQ1	FSB_50S	FSB_1X	FSB BREQ1 L	1386
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	906 1386
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	906 1383
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	906 1386
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	906 1383
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	906 1386
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	906 1386
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	906 1386
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	906 1386
FSB_CPURST	FSB_50S	FSB_1X	FSB CPURST L	906 1202 13A3
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	906 13A6
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	906 1386
CPU_ASYM	CPU_50S	CPU_AGTL	CPU A20M L	908 13A3
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	882 984
CPU_FERR	CPU_50S	CPU_BMIL	CPU FERR L	908 1387
CPU_ASYM	CPU_50S	CPU_AGTL	CPU IGNE L	908 13A3
CPU_INIT	CPU_50S	CPU_AGTL	CPU INIT L	906 13A3
CPU_ASYM	CPU_50S	CPU_AGTL	CPU INTR	908 13A3
CPU_ASYM	CPU_50S	CPU_AGTL	CPU NMI	988 13A3
CPU_PROCHOT	CPU_50S	CPU_AGTL	CPU PROCHOT L	905 1386 4104 6208
CPU_PERR0	CPU_50S	CPU_AGTL	CPU PWRGD	982 1207 13A3
CPU_ASYM	CPU_50S	CPU_AGTL	CPU SMI L	988 13A3
CPU_ASYM	CPU_50S	CPU_AGTL	CPU STPCLK L	908 13A3
PM_THRMTRIP	CPU_50S	CPU_BMIL	PM THRMTRIP L	906 1387 4104
FSB_CPUSLP	CPU_50S	CPU_AGTL	FSB CPUSLP L	982 13A3
CPU_FSB_SB	CPU_50S	CPU_AGTL	CPU DESLP L	982 13A3
CPU_DPRSTP	CPU_50S	CPU_AGTL	CPU DPRSTP L	982 13A3 6207
CPU_ASYM	CPU_50S	CPU_AGTL	FSB DPWR L	982 13A3
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	13A6
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	13A6
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	986 1383
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	986 1383
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	1203 1383
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	1203 1383
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	13A4
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	13A4
CPU_IERR	CPU_50S		CPU IERR L	906
PM DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	2007 6208
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	6207
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	984 2881
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	983
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	983
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	983
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	983
XDP_TDI	CPU_50S	CPU_TTP	XDP TDI	986 908 1283
XDP_TDO	CPU_50S	CPU_TTP	XDP TDO	986 908 1283
XDP_TMS	CPU_50S	CPU_TTP	XDP TMS	986 908 1283
XDP_TCK	CPU_50S	CPU_TTP	XDP TCK	9A6 908 1286
XDP_TRST	CPU_50S	CPU_TTP	XDP TRST L	9A6 908 1283
XDP_BPM	CPU_50S	CPU_TTP	XDP BPM L<4..0>	906 1206
XDP_BPM	CPU_50S	CPU_TTP	XDP BPM L<5>	906 1206
(FSB_CPURST L)	CPU_50S	CPU_TTP	XDP CPURST L	1204
	CPU_50S	CPU_BMIL	CPU VID<6..0>	1086 6207
	CPU_50S	CPU_BMIL	IMVP6 VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	10A5 62A5
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	10A5 62A5
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	

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CPU/FSB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SR	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SR	=40_OHM_SE	=40_OHM_SR	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20THER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20THER
MEM_CTRL	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_DATA	*	*	MEM_20THER
MEM_DQS	*	*	MEM_20THER

Need to support MEM*-style wildcards!

DDR2:
 DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
 DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_TYPE	
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	1485 2605 2607
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	1485 2605 2607
MEM_A_CKE	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	1445 2606 2607
MEM_A_CS	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>	1485 2605 2607
MEM_A_ODT	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	1485 2605
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	1485 1405 2605 2607
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	1405 2605 2607
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L	1405 2605
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L	1405 2607
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L	1405 2607
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<7..0>	1487 2602 2604 2602 2604
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<15..8>	1487 2602 2604
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<23..16>	1487 1407 2682 2684 2602 2604
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<31..24>	1407 2602 2604
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<39..32>	1407 2685 2687 2605 2607
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<47..40>	1407 1407 2685 2687
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<55..48>	1407 2685 2687
MEM_A_DQ	MEM_40S	MEM_DATA	MEM A DQ<63..56>	1407 26A5 26A7 2685 2687
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<0>	14A7 2604
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<1>	14A7 2602
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<2>	1487 2684
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<3>	1487 2602
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<4>	1487 2685
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<5>	1487 2687
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<6>	1487 2685
MEM_A_DM	MEM_40S	MEM_DATA	MEM A DM<7>	1487 26A7
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<0>	1405 2602
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<0>	1405 2602
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<1>	1405 2604
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<1>	1405 2604
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<2>	1405 2682
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<2>	1405 2602
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<3>	1405 2604
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<3>	1405 2604
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<4>	1405 2687
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<4>	1405 2687
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<5>	1405 2685
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<5>	1405 2685
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<6>	1405 2687
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<6>	1405 2687
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS P<7>	1405 26A5
MEM_A_DQS	MEM_70D	MEM_DQS	MEM A DQS N<7>	1405 26A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	1481 2705 2707
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	1481 2705 2707
MEM_B_CKE	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	14A1 2706 2707
MEM_B_CS	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>	1481 2705 2707
MEM_B_ODT	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	1481 2705
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	1481 1401 2705 2707
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	1401 2705 2707
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L	1401 2705
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L	1401 2707
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L	1401 2707
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<7..0>	1483 2702 2704 2702 2704
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<15..8>	1483 2702 2704
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<23..16>	1483 1403 2702 2704
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<31..24>	1403 2782 2784 2702 2704
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<39..32>	1403 2785 2787 2705 2707
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<47..40>	1403 1403 2785 2787
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<55..48>	1403 2785 2787
MEM_B_DQ	MEM_40S	MEM_DATA	MEM B DQ<63..56>	1403 27A5 27A7 2785 2787
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<0>	14A3 2704
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<1>	14A3 2702
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<2>	1483 2702
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<3>	1483 2784
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<4>	1483 2785
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<5>	1483 2787
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<6>	1483 2785
MEM_B_DM	MEM_40S	MEM_DATA	MEM B DM<7>	1483 27A7
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<0>	1401 2702
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<0>	1401 2702
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<1>	1401 2704
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<1>	1401 2704
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<2>	1401 2704
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<2>	1401 2704
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<3>	1401 2782
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<3>	1401 2702
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<4>	1401 2787
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<4>	1401 2787
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<5>	1401 2785
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<5>	1401 2785
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<6>	1401 2787
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<6>	1401 2787
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS P<7>	1401 27A5
MEM_B_DQS	MEM_70D	MEM_DQS	MEM B DQS N<7>	1401 27A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_VDD	1506
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP_GND	1506

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Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	*	=3X_DIELECTRIC	?	PCI_E	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCI_E	*	20 MIL	?				
MCP_PEX_COMP	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_90D_HDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?	SATA	TOP,BOTTOM	=3X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	PCI_E_90D	PCI_E	PCI_E MINI R2D P	405 2907
	PCI_E_90D	PCI_E	PCI_E MINI R2D N	405 2907
	PCI_E_90D	PCI_E	PCI_E MINI R2D C P	1683 2905
	PCI_E_90D	PCI_E	PCI_E MINI R2D C N	1683 2905
	PCI_E_90D	PCI_E	PCI_E MINI D2R P	405 1686 2907
	PCI_E_90D	PCI_E	PCI_E MINI D2R N	405 1686 2907
	PCI_E_90D	PCI_E	PCI_E FW R2D P	3403
	PCI_E_90D	PCI_E	PCI_E FW R2D N	3403
	PCI_E_90D	PCI_E	PCI_E FW R2D C P	1683 3401
	PCI_E_90D	PCI_E	PCI_E FW R2D C N	1683 3401
	PCI_E_90D	PCI_E	PCI_E FW D2R P	1686 3401
	PCI_E_90D	PCI_E	PCI_E FW D2R N	1686 3401
	PCI_E_90D	PCI_E	PCI_E FW D2R C P	3403
	PCI_E_90D	PCI_E	PCI_E FW D2R C N	3403
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI P	1603 2905
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI N	1603 2905
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI CONN P	405 2907
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M MINI CONN N	405 2907
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M FC P	
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E CLK100M FC N	
	MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP PEX CLK COMP	1646
	DP_100D	DISPLAYPORT	TMDS IG TXC P	
	DP_100D	DISPLAYPORT	TMDS IG TXC N	
	DP_100D	DISPLAYPORT	TMDS IG TXD P<2..0>	
	DP_100D	DISPLAYPORT	TMDS IG TXD N<2..0>	
	DP_ML	DISPLAYPORT	DP ML P<3..0>	4903 7001 7008
	DP_ML	DISPLAYPORT	DP ML C P<3..0>	7002 7007
	DP_ML	DISPLAYPORT	DP ML N<3..0>	4903 7001 7008
	DP_ML	DISPLAYPORT	DP ML C N<3..0>	7002 7007
	DP_AUX_CH	DISPLAYPORT	DP IG AUX CH P	1786 6907
	DP_AUX_CH	DISPLAYPORT	DP IG AUX CH N	1786 6907
	DP_AUX_CH	DISPLAYPORT	DP AUX CH SW P	6906
	DP_AUX_CH	DISPLAYPORT	DP AUX CH SW N	6905
	DP_AUX_CH	DISPLAYPORT	DP AUX CH C P	6904 7008
	DP_AUX_CH	DISPLAYPORT	DP AUX CH C N	6904 7008
	MCP_HDMI_RSET	MCP_DV_COMP	MCP HDMI RSET	1746 2307
	MCP_HDMI_VPROBE	MCP_DV_COMP	MCP HDMI VPROBE	1746 2307
	LVDS_IG_A_CLK	LVDS_100D	LVDS IG A CLK P	1783 6883
	LVDS_IG_A_CLK	LVDS_100D	LVDS IG A CLK F P	607 6802
	LVDS_IG_A_CLK	LVDS_100D	LVDS IG A CLK N	1783 6883
	LVDS_IG_A_CLK	LVDS_100D	LVDS IG A CLK F N	607 6802
	LVDS_IG_A_DATA	LVDS_100D	LVDS IG A DATA P<2..0>	607 1783 6802
	LVDS_IG_A_DATA	LVDS_100D	LVDS IG A DATA N<2..0>	607 1783 6802
	DP_ML	DISPLAYPORT	DP ML CONN P<3..0>	7003 7004 7005
	DP_ML	DISPLAYPORT	DP ML CONN N<3..0>	7003 7004 7005
	MCP_IFPAB_RSET	MCP_DV_COMP	MCP IFPAB RSET	1743 2306
	MCP_IFPAB_VPROBE	MCP_DV_COMP	MCP IFPAB VPROBE	1743 2306
	SATA_HDD_R2D	SATA_90D_HDD	SATA HDD R2D C P	1906 3762
	SATA_HDD_R2D	SATA_90D_HDD	SATA HDD R2D C N	1906 3762
	SATA_HDD_R2D	SATA_90D_HDD	SATA HDD R2D P	687 3765
	SATA_HDD_R2D	SATA_90D_HDD	SATA HDD R2D N	687 3765
	SATA_HDD_R2D	SATA_90D_HDD	SATA HDD R2D UF P	3764
	SATA_HDD_R2D	SATA_90D_HDD	SATA HDD R2D UF N	3764
	SATA_HDD_D2R	SATA_90D_HDD	SATA HDD D2R P	1906 3782
	SATA_HDD_D2R	SATA_90D_HDD	SATA HDD D2R N	1906 3782
	SATA_HDD_D2R	SATA_90D_HDD	SATA HDD D2R C P	687 3785
	SATA_HDD_D2R	SATA_90D_HDD	SATA HDD D2R C N	687 3785
	SATA_HDD_D2R	SATA_90D_HDD	SATA HDD D2R UF P	3784
	SATA_HDD_D2R	SATA_90D_HDD	SATA HDD D2R UF N	3784
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D C P	1906 3703
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D C N	1906 3703
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D P	687 3706
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D N	687 3706
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D UF P	3704
	SATA_ODD_R2D	SATA_100D	SATA ODD R2D UF N	3704
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R P	1906 3703
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R N	1906 3703
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R C P	687 3706
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R C N	687 3706
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R UF P	3704
	SATA_ODD_D2R	SATA_100D	SATA ODD D2R UF N	3704
	MCP_SATA_TERM	SATA_TERM	MCP SATA TERM	1946

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MCP Constraints 1

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HDA Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	1203 1807
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	
PCI_AD	PCI_55S	PCI	PCI_PAR	
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L	
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L	
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	1802 1807
PCI_REQ0_L	PCI_55S	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	1802 1807
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK PCI_55S	CLK PCI	PCI_CLK33M MCP_R	1805
MCP_PCI_CLK2	CLK PCI_55S	CLK PCI	PCI_CLK33M MCP	1805
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	1883 4008 4203 4205
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	1803 4008 4205
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	1803 2404
MCP_LPC_CLK0	CLK LPC_55S	CLK LPC	LPC_CLK33M SMC_R	1883 2484
MCP_LPC_CLK0	CLK LPC_55S	CLK LPC	LPC_CLK33M SMC	2481 4008
MCP_LPC_CLK0	CLK LPC_55S	CLK LPC	LPC_CLK33M LPCPLUS	2481 4203
USB_EXTA	USB_90D	USB	USB_EXTA_P	1903 38A8
USB_EXTA	USB_90D	USB	USB_EXTA_N	1903 38A8
USB_EXTA	USB_90D	USB	USB_EXTA_MUXED_P	3804
USB_EXTA	USB_90D	USB	USB_EXTA_MUXED_N	3804
CONN_USB_EXTA_P	USB_90D	USB	CONN_USB_EXTA_P	3803
CONN_USB_EXTA_N	USB_90D	USB	CONN_USB_EXTA_N	3803
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	1903 2985
USB_CAMERA	USB_90D	USB	USB_CAMERA_N	1903 2985
USB_CAMERA	USB_90D	USB	USB_CAMERA_CONN_P	605 2987
USB_CAMERA	USB_90D	USB	USB_CAMERA_CONN_N	605 2987
USB_BT	USB_90D	USB	USB_BT_P	1903 2985
USB_BT	USB_90D	USB	USB_BT_N	1903 2985
CONN_USB2_BT_P	USB_90D	USB	CONN_USB2_BT_P	605 2987
CONN_USB2_BT_N	USB_90D	USB	CONN_USB2_BT_N	605 2987
USB_TPAD	USB_90D	USB	USB_TPAD_P	1903 4888
USB_TPAD	USB_90D	USB	USB_TPAD_N	1903 4888
USB_TPAD	USB_90D	USB	USB_TPAD_R_P	4887
USB_TPAD	USB_90D	USB	USB_TPAD_R_N	4887
USB_IR	USB_90D	USB	USB_IR_P	1903 3907
USB_IR	USB_90D	USB	USB_IR_N	1903 3907
USB_EXTB	USB_90D	USB	USB_EXTB_P	1903 38A4
USB_EXTB	USB_90D	USB	USB_EXTB_N	1903 38A4
CONN_USB_EXTB_P	USB_90D	USB	CONN_USB_EXTB_P	3883
CONN_USB_EXTB_N	USB_90D	USB	CONN_USB_EXTB_N	3883
USB_CARDREADER_P	USB_90D	USB	USB_CARDREADER_P	1903 3007
USB_CARDREADER_N	USB_90D	USB	USB_CARDREADER_N	1903 3007
MCP_USB_BIAS	MCP_USB_BIAS		MCP_USB_BIAS_GND	1904
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	1286 2003 4308
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	1286 2003 4308
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	2003 4388
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	2003 4388
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	2002 5207
HDA_BIT_CLK_R	HDA_55S	HDA	HDA_BIT_CLK_R	20A7 2004
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	2002 5207
HDA_SYNC_R	HDA_55S	HDA	HDA_SYNC_R	20A7 2004
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	20A7 2004
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	2002 5207
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	2007 5207
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	2002 5207
HDA_SDOUT_R	HDA_55S	HDA	HDA_SDOUT_R	20A7 2004
MCP_HDA_PULLDN_COMP	MCP_HDA_PULLDN_COMP		MCP_HDA_PULLDN_COMP	2007
MCP_SIO_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K SUSCLK_R	2083 2484
MCP_SIO_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K SUSCLK	2481 4005
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	2083 42A5 4208
SPI_CLK	SPI_55S	SPI	SPI_CLK	4105
SPI_ALT_CLK	SPI_55S	SPI	SPI_ALT_CLK	4205 4203
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	2083 42A5 4207
SPI_MOSI	SPI_55S	SPI	SPI_MOSI	5104
SPI_ALT_MOSI	SPI_55S	SPI	SPI_ALT_MOSI	4205 4205
SPI_MISO	SPI_55S	SPI	SPI_MISO	2083 42A5 4287
SPI_MISO	SPI_55S	SPI	SPI_MISO_R	5104
SPI_ALT_MISO	SPI_55S	SPI	SPI_ALT_MISO	4285 4205
SPI_CS0_L	SPI_55S	SPI	SPI_CS0_L	2083 4287
SPI_CS0_L	SPI_55S	SPI	SPI_CS0_L	
SPI_CS1_R_L	SPI_55S	SPI	SPI_CS1_R_L	
SPI_CS1_R_L	SPI_55S	SPI	SPI_CS1_R_L_USE_MLR	

SYNC MASTER=T18 MLB SYNC DATE=12/14/2007

MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SR	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD	1706
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND	1706
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M_BUF0_R	1703 32A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1	3186 32A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO	1703 3186
ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC	1703 3186
ENET_PWDWN_L	ENET_MII_55S	ENET_MII	ENET_PWDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	3104
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	1706 3101
	ENET_MII_55S	ENET_MII	ENET_RXD R<3..0>	3104
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	1706 3101
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	1706 3101
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	1706 3181
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	3184
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R	3104
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	1703 3108
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	1703 3106
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	1703 3106
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	1703 3186
	ENET_MII_55S	ENET_MII	ENET_RESET_L	1703 3187
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0>	3183 3388 3308
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0>	3183 3388 3308
	ENET_MDI_100D	ENET_MDI	ENET MDI TRAN P<3..0>	3384 3304 3305
	ENET_MDI_100D	ENET_MDI	ENET MDI TRAN N<3..0>	3384 3304 3305

SYNC MASTER=T18 MLB SYNC DATE=03/19/2008

Ethernet Constraints

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_1100	*	+110_00M_DIFF	+110_00M_DIFF	+110_00M_DIFF	+110_00M_DIFF	+110_00M_DIFF	+110_00M_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_00	*	+112_00M_DIFF	7

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_550	*	+55_00M_SE	+55_00M_SE	+55_00M_SE	+55_00M_SE	+STANDARD	+STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	+3M_SELECTRIC	7

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
FW_P0_TPA_P	FW_1100	FW_TP		FW P0 TPA P	3486 3604
FW_P0_TPA_N	FW_1100	FW_TP		FW P0 TPA N	3486 3604
FW_P0_TPB_P	FW_1100	FW_TP		FW P0 TPB P	3486 3604
FW_P0_TPB_N	FW_1100	FW_TP		FW P0 TPB N	3486 3604
FW_P1_TPA_P	FW_1100	FW_TP		FW P1 TPA P	3486 3688
FW_P1_TPA_N	FW_1100	FW_TP		FW P1 TPA N	3486 3688
FW_P1_TPB_P	FW_1100	FW_TP		FW P1 TPB P	3486 3688
FW_P1_TPB_N	FW_1100	FW_TP		FW P1 TPB N	3486 3688
Port 2 Not Used					

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
SD_D<0>	SD_550	SD_INTERFACE		SD D<0>	3002
SD_D<1>	SD_550	SD_INTERFACE		SD D<1>	3002
SD_D<2>	SD_550	SD_INTERFACE		SD D<2>	3002
SD_D<3>	SD_550	SD_INTERFACE		SD D<3>	3002
SD_D<4>	SD_550	SD_INTERFACE		SD D<4>	3002
SD_D<5>	SD_550	SD_INTERFACE		SD D<5>	3002
SD_D<6>	SD_550	SD_INTERFACE		SD D<6>	3002
SD_D<7>	SD_550	SD_INTERFACE		SD D<7>	3002
SD_CLK	SD_550	SD_INTERFACE		SD CLK	3002
SD_CMD	SD_550	SD_INTERFACE		SD CMD	3002

SYNC MASTER=K19 MLB SYNC DATE=12/01/2008

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS SMC A S3 SCL	SMB 550	5MM	SMBUS SMC A S3 SCL	605 605 4302
SMBUS SMC A S3 SDA	SMB 550	5MM	SMBUS SMC A S3 SDA	605 605 4302
SMBUS SMC B S0 SCL	SMB 550	5MM	SMBUS SMC B S0 SCL	4302
SMBUS SMC B S0 SDA	SMB 550	5MM	SMBUS SMC B S0 SDA	4302
SMBUS SMC O S0 SCL	SMB 550	5MM	SMBUS SMC O S0 SCL	4305
SMBUS SMC O S0 SDA	SMB 550	5MM	SMBUS SMC O S0 SDA	4305
SMBUS SMC BSA SCL	SMB 550	5MM	SMBUS SMC BSA SCL	6A7 4305
SMBUS SMC BSA SDA	SMB 550	5MM	SMBUS SMC BSA SDA	6A7 4305
SMBUS SMC MGMT SCL	SMB 550	5MM	SMBUS SMC MGMT SCL	43B5
SMBUS SMC MGMT SDA	SMB 550	5MM	SMBUS SMC MGMT SDA	43B5


SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR CSI	1T01 DIFFPAIR		CHGR CSI P	
			CHGR CSI N	
CHGR CSO	1T01 DIFFPAIR		CHGR CSO P	
			CHGR CSO N	

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SYNC MASTER=T18 MLB		SYNC DATE=01/04/2008	
SMC Constraints			
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

K24 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DIFFPAIR			CHGR CSO R P	45A8 59B3
DIFFPAIR			CHGR CSO R N	45A8 59B3
DIFFPAIR			CPUTHMSNS D2 P	46C5
DIFFPAIR			CPUTHMSNS D2 N	46C5
DIFFPAIR			CPU THERMD P	9C6 46D5
DIFFPAIR			CPU THERMD N	9C6 46D5
DIFFPAIR			ISNS CPUVTT P	45B7
DIFFPAIR			ISNS CPUVTT N	45B7
DIFFPAIR			ISNS P1V5S0MCP P	
DIFFPAIR			ISNS P1V5S0MCP N	
DIFFPAIR			ISNS P1V5S0MCP P	
DIFFPAIR			ISNS P1V5S0MCP N	
DIFFPAIR			MCP THMSNS D2 P	6C7 46B5
DIFFPAIR			MCP THMSNS D2 N	6C7 46B5
DIFFPAIR			MCP THMDIODE P	20C3 46B5
DIFFPAIR			MCP THMDIODE N	20C3 46B5

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SYNC MASTER=M97 MLB

K24 SPECIAL CONSTRAINTS

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K24 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS			BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM			NO_TYPE, BGA_P1MM				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	0.224 MM	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.350 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

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K24 RULE DEFINITIONS

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