

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K36 MLB SCHEMATIC

REFERENCED FROM M70
8/9/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
?		?	?	DATE	DATE
				?	?

Page	(.csa)	Contents	Sync	Date
1	1	Table of Contents	RX	09/05/2006
2	2	System Block Diagram	RX	05/11/2006
3	3	Power Block Diagram	MK	06/30/2005
4	4	CONFIGURATION OPTIONS	RX	07/18/2005
5	5	Revision History	RX	N/A
6	7	FUNC TEST 1 OF 2	RX	07/25/2005
7	8	Power Aliases	MK	06/15/2006
8	9	SIGNAL ALIAS /RESET	RX	07/17/2006
9	10	CPU FSB	RX	11/12/2006
10	11	CPU Power & Ground	RX	T9_MLB_NOME
11	12	CPU Decoupling & VID	RX	MSARWAR
12	13	CPU ITP700FLEX DEBUG	ES	MASTER
13	14	NB CPU Interface	ES	T9_MLB
14	15	NB PEG / Video Interfaces	ES	T9_MLB
15	16	NB Misc Interfaces	ES	T9_MLB
16	17	NB DDR2 Interfaces	ES	T9_MLB
17	18	NB Power 1	ES	T9_MLB
18	19	NB Power 2	ES	T9_MLB
19	20	NB Grounds	ES	T9_MLB
20	21	NB Standard Decoupling	ES	WFERRY
21	22	NB Graphics Decoupling	ES	WFERRY
22	23	SB Enet, Disk, FSB, LPC	RX	T9_MLB
23	24	SB PCI, PCIe, DMI, USB	RX	T9_MLB
24	25	SB Pwr Mgt, GPIO, Clink	RX	T9_MLB
25	26	SB Power & Ground	RX	T9_MLB
26	27	SB Decoupling	RX	WFERRY
27	28	SB Misc	RX	NB
28	29	Clock (CK505)	DK	DSIMON
29	30	Clock Termination	DK	DSIMON-WF
30	31	DDR2 SO-DIMM Connector A	LD	MEMORY
31	32	DDR2 SO-DIMM Connector B	LD	MEMORY
32	33	Memory Active Termination	LD	MEMORY
33	34		LT	ENET
34	37	Ethernet (Yukon)	LT	USB
35	38	Yukon Power Control	LT	USB
36	39	ETHERNET CONNECTOR	LT	USB
37	40	FIREWIRE CONTROLLER	LT	ENET
38	43	FIREWIRE PORT	LT	GPU
39	44	PATA CONNECTOR	DK	GPU
40	45	SATA CONNECTOR	RX	GPU
41	46	USB EXTERNAL CONNECTORS	LT	USB
42	47	CONNECTOR MISC	LT	USB
43	48	IR CONTROLLER & BT INTERFACE	LT	USB
44	49	SMC	LD	T9_MLB
45	50	SMC SUPPORT	LD	GPU

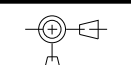
Page	(.csa)	Contents	Sync	Date
46	51	LPC+ Debug Connector	LD	WFERRY
47	52	SMBUS CONNECTIONS	LD	WFERRY
48	53	CPU Current & Voltage Sense	ES	GPU
49	55	TEMPERATURE SENSE	ES	GPU
50	56	Fan	LD	ENET
51	59	SMS	MK	SMC
52	61	SPI ROMs	RX	WFERRY
53	62	AUDIO: CODEC	RX	M70AUDIO
54	66	AUDIO: SPEAKER AMP	RX	M70AUDIO
55	67	AUDIO: JACK	RX	M70AUDIO
56	68	AUDIO: JACK TRANSLATORS	RX	M70AUDIO
57	69	DC-In & Battery Connectors	RX	POWER
58	70	S0 FETS & Power Sequencing	MK	DSIMON-WF
59	71	IMVP6 CPU VCore Regulator	MK	POWER
60	72	Render VCore Supplies	MK	GPU
61	73	1.5V / 1.05V Supplies	MK	POWER
62	75	1.8V/0.9V Supplies	MK	POWER
63	76	5V/3.3V Supplies	MK	POWER
64	77	3.42V/1.25V Switcher	MK	ENET
65	78	S3 FET & S3/S5 Control	MK	DSIMON-WF
66	79	PBUS Supply/Battery Charger	MK	SMC
67	90	INVERTER, LVDS, TMS	MK	GPU
68	92	EXTERNAL TMS	ES	GRAPHIC
69	94	MINI-DVI CONNECTOR	ES	EUGENE
70	100	CPU/FSB Constraints	ES	WFERRY
71	101	NB Constraints	RX	WFERRY
72	102	Memory Constraints	ES	WFERRY
73	103	SB Constraints (1 of 2)	LD	WFERRY
74	104	SB Constraints (2 of 2)	RX	WFERRY
75	105	Clock Constraints	RX	WFERRY
76	106	FireWire & SMC Constraints	DK	WFERRY

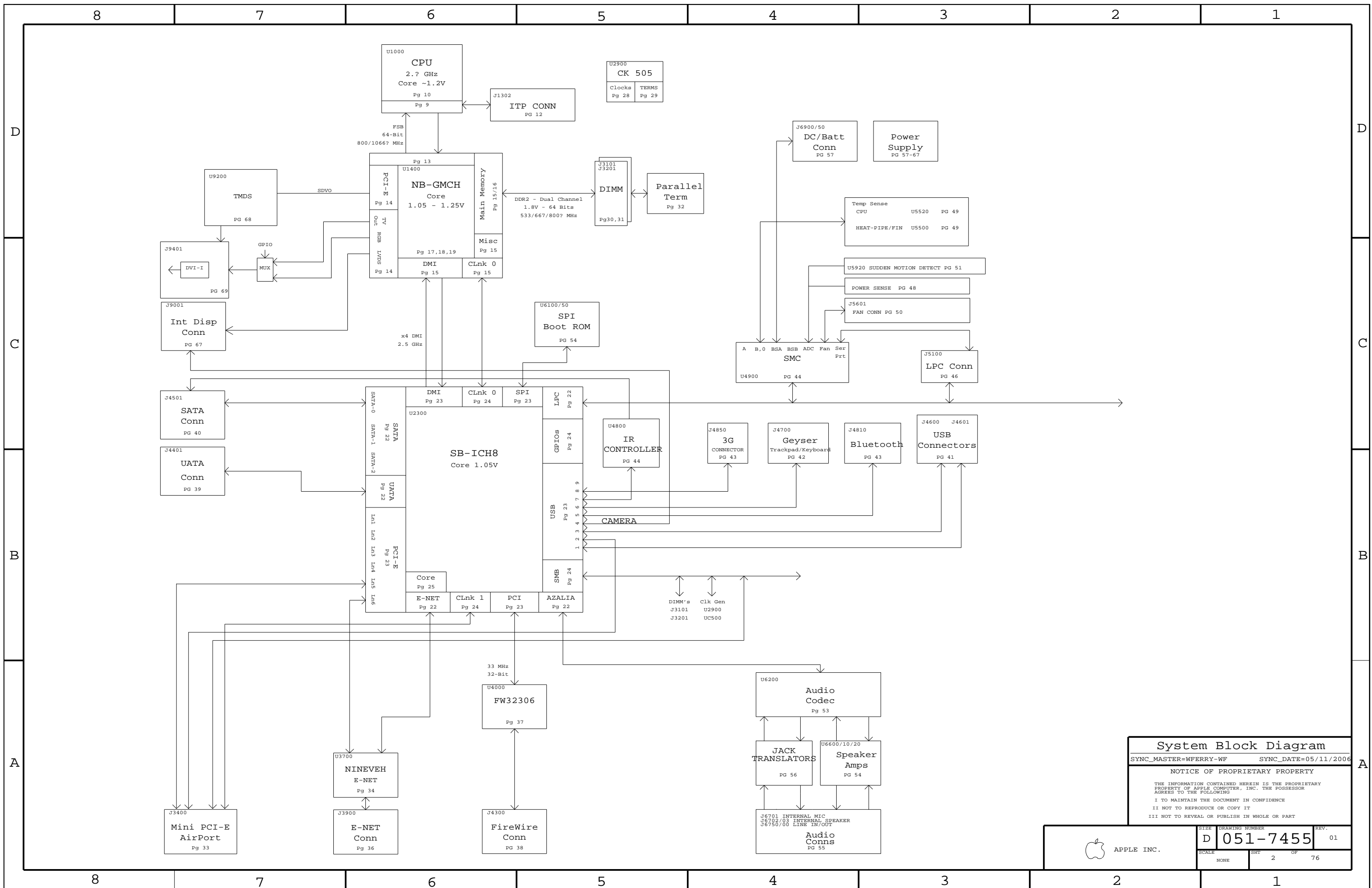
K36 EE DRIS:
RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFER
LT-LAWRENCE TAN
LD-LINDA DUNN
MM-MARY(YUAN) MA

DVT BUILD

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7455	1	SCHEM, MLB, K36	SCH	CRITICAL	
820-2279	1	PCBF, MLB, K36	PCB	CRITICAL	

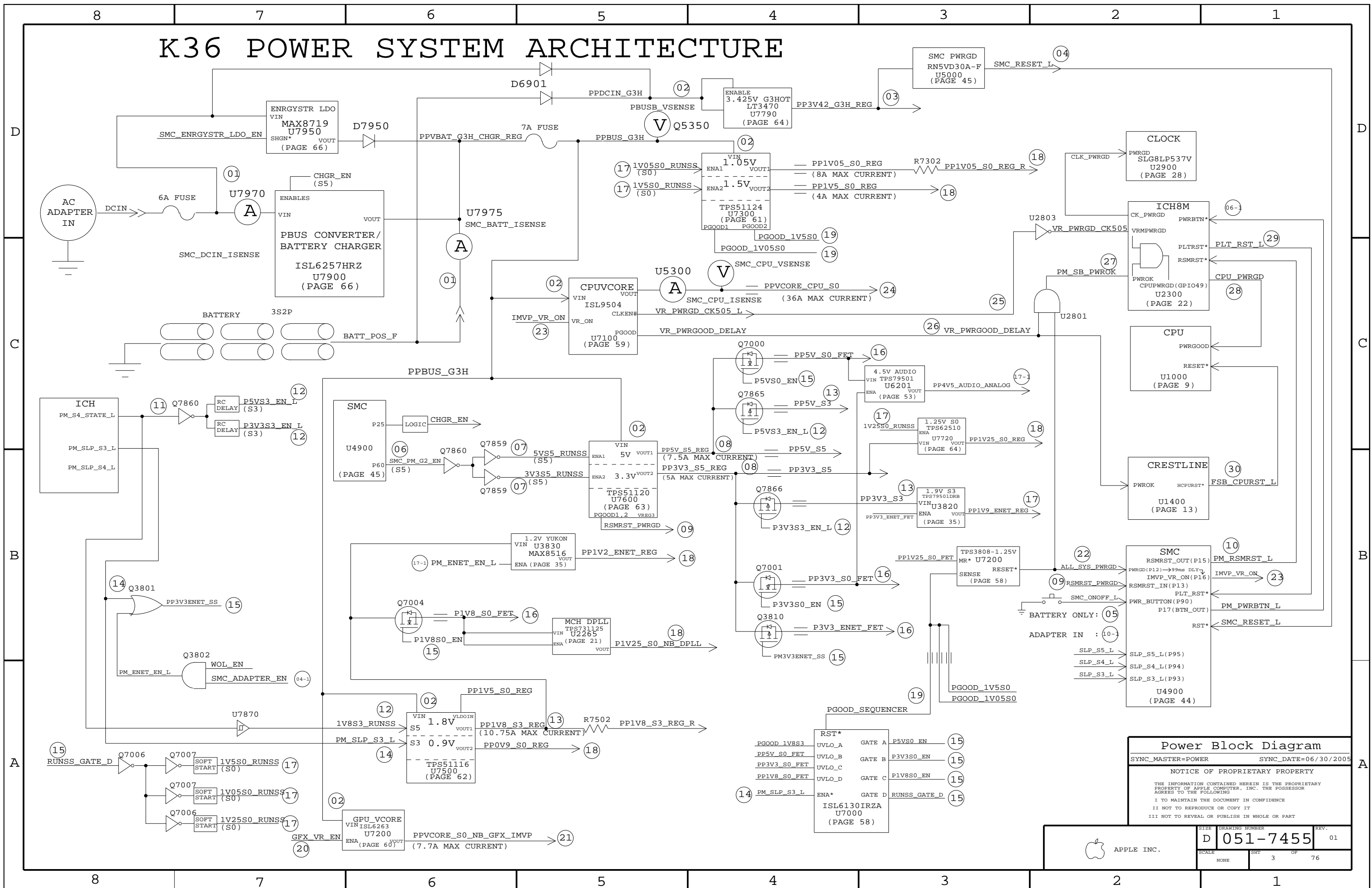
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DO NOT SCALE DRAWING		WRAPPER	DESIGN CR	TITLE	
		ENG APPD	MFG APPD	SCHEM, MLB, K36	
		QA APPD	DESIGNER	DRAWING NUMBER 051-7455	
		RELEASE	SCALE NONE	REV. 01	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	SHT 1 OF 76	



System Block Diagram
 SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		2	76

K36 POWER SYSTEM ARCHITECTURE



Power Block Diagram
 SYNC_MASTER=POWER SYNC_DATE=06/30/2005
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

BOMOPTION	K36 GOOD 630-9104 EVT	K36 BETTER 630-9105 EVT	K36 BEST 630-9106 EVT	M70 GOOD 630-7935 CONCEPT
COMMON	V	V	V	V
ALTERNATE	V	V	V	V
ARB_ONLY				
K36	V	V	V	V
LPCPLUS	V	V	V	V
INVERTER_BUF	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V
INVERTER_UNBUF	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V
ITP	V	V	V	V
NO_REBOOT_MODE				
NBCFG_DMI_REVERSE				
NBCFG_DMI_X2				
NBCFG_DYN_ODT_DISABLE				
NBCFG_PEG_REVERSE				
NBCFG_SDVO_AND_PCIE				
GOOD	V			V
BETTER		V		V
BEST			V	V
K36_PGM	V	V	V	V
YUKON_EC				V
YUKON_ULTRA	V	V	V	V
NORMAL	V	V		V
FANCY			V	V
STANDOFF	V	V	V	V
ODD_PWR_CORE	V	V	V	V
ODD_PWR_RESUME				V
ISL6126	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	
ISL6130	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

BOM TABLE FOR HF POSCAPS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0147	4	HF VERSION OF 128S0057	C4610,C4611,C6830,C6831	CRITICAL	K36
128S0164	3	HF VERSION OF 128S0073	C2130,C2716,C7543	CRITICAL	K36
128S0148	1	HF VERSION OF 128S0085	C6605	CRITICAL	K36
128S0169	3	HF VERSION OF 128S0111	C7220,C7352,C7542	CRITICAL	K36
128S0160	2	HF VERSION OF 128S0113	C2173,C2700	CRITICAL	K36
128S0150	6	HF VERSION OF 128S0115	C6204,C6205,C7651,C7652,C7691,C7692	CRITICAL	K36
128S0157	1	HF VERSION OF 128S0122	C2220	CRITICAL	K36
128S0162	1	HF VERSION OF 128S0123	C2140	CRITICAL	K36
128S0135	2	HF VERSION OF 128S0129	C6601,C6603	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3463	1	IC,MDC,SR,E1.2.GG,800PFB,4M,BGA	U1000	CRITICAL	GOOD
337S3500	1	IC,MDC,SR,GG.2.2G,800PFB,4M,BGA	U1000	CRITICAL	BETTER
337S3500	1	IC,MDC,SR,GG.2.2G,800PFB,4M,BGA	U1000	CRITICAL	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0448	1	IC,CRESTLINE,GM965,667	U1400	CRITICAL	K36
338S0434	1	IC,ICHS,BGA	U2300	CRITICAL	K36
516-0162	2	IN-LINE SOD1MM CONNECTOR	J3101,J3201	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2196	1	IC,16MBIT 8PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	K36_PGM
341S2060	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	K36_PGM
341S2198	1	IC,SMC,H58/2116	U4900	CRITICAL	K36_PGM
341S2093	1	IC,CYPRESS,CY7C63833,ENCORE_II,USB_CNTR	U4800	CRITICAL	K36_PGM

LOCKED BOOTROM PN 341S2197


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:Z55	CRITICAL	GOOD
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:Z56	CRITICAL	BETTER
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:Z57	CRITICAL	BEST

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	SHT	OF	76
NONE	4		

Revision History

M70 PROTO TO EVT CHANGES

- WAKE-ON-WIRELESS SUPPORT - RADAR: 4954357
- ADD ISOLATION BUFFER FOR ODD_RESET_L SIGNAL...
- ADD 270K PULL-DOWN RESISTOR ON HTPLG - RADAR: 4888755
- LOWER RDS(ON) MOSFET (FDC606P - APN: 376S0552) FOR ODD AND LCD POWER - RADAR: TBD
- HIGH-PRECISION 0.1% RESISTORS TO INCREASE OUTPUT VOLTAGE REGULATION (5V, 3.3V, PBUS_LDO) ACCURACY - RADAR:4972500
- FIX LINDA CARD POWER ALIAS (NEED TO CONNECT TO PP3V42_G3HOT INSTEAD OF PP3V3_S5) - RADAR: 4927858
- FIX MOJO-CARD SMC TX, RX REVERSAL - RADAR: 4910888
- NO STUFF 3G CONNECTOR CIRCUITRY
- CHANGE BOM STUFFING TO SPEED UP PORT POWER SHUT-OFF RESPONSE TIME DURING ACTIVE LATE-VG EVENT (RADAR: 4985252)
- CHANGE BOM STUFFING TO ENABLE ON-BOARD MICROPHONE CONNECTOR (M42/M42A SOLUTION) INSTEAD OF ROUTING MICROPHONE THROUGH LVDS CABLE
- CHANGE LOAD CAP STUFFING OPTION FOR RTC AND ETHERNET CRYSTALS TO MEET 5XESR (-R) REQUIREMENT
- CHANGE 10UF, 16V CPU VCORE CAPS TO 10UF, 6.3V CAPS - RADAR: 4952553
- MOVE SMC RESET BUTTON PAD TO TOP SIDE OF MLB - RADAR: 4920913
- MODIFY FIREWIRE CONNECTOR SYMBOL TO SUPPORT MINI-DVI CONNECTOR WITH TAB
- TEST POINT MOVEMENTS REQUESTED BY ICT AND MAC-1 GROUPS - RADAR: 4924481

M70 EVT TO DVT CHANGES

3/5/2007
CSA PAGE 8:
- 4954357 ADD =PP3V3_S3_AIRPORT_AUX BACK TO PP3V3_S3 ALIAS.
CSA PAGE 34:
- 4954357 BREAK OUT =PP3V3_S3_AIRPORT_AUX(J3400.PIN 24) FROM PP3V3_S3_AP_AUX AGAIN.
- 4954357 MOVE C3409 AND C3410 FROM PP3V3_S3_AP_AUX RAIL TO =PP3V3_S3_AIRPORT_AUX RAIL.
CSA PAGE 49:
- 5040728 STUFF C9421 FOR EMI.
CSA PAGE 62,66,67,68:
- SYNC FROM AUDIO TEAM.
CSA PAGE 94:
- 4996074 SWAP PIN 2 AND PIN 3 OF MIC CONNECTOR, BACK TO M42 PIN OUT.
CSA PAGE 99:
- 5029811 CHANGE Q7940 FROM 376S0326 TO 376S0558.

3/8/2007
CSA PAGE 22:
- 4996074 CHANGE L2205 TO R2205(1000HM,5%,1/10W,0603).
CSA PAGE 25:
- 4924443 CHANGE R2514 FROM 100K PULL-DOWN TO 10K PULL-UP TO 3.3V_S5.
CSA PAGE 77:
- 5040817 SYNC LP25V REGULATOR CIRCUIT FROM M82 CHANGE R AND C TO Q402 CHANGE =PP3V3_S5_P1V25S0 TO =PP3V3_S5_1V25S0,
- C172 FROM 100UF TO 100UF C172B FROM 22UF TO 100UF,
- AND REVERT REFERENCE DESIGNATORS. (CHANGE FROM TPS62510 TO LTC3412A)

3/12/2007
CSA PAGE 25:
- 4924443 CHANGE R2514 FROM 100K PULL-UP TO 47K PULL-UP.
CSA PAGE 45:
- UPDATE SYMBOL FOR J4501.
CSA PAGE 62,66,67,68:
- SYNC FROM AUDIO TEAM.
CSA PAGE 94:
- 4996074 CHANGE R9469 FOR CRT_TVO_IREF FROM 1.3K TO 1.21K.

3/14/2007
CSA PAGE 47:
- ADD TEXT NOTE TO UPDATE J4700 FROM 516S0251 TO 516S0588 WHEN SYMBOL IS READY.
CSA PAGE 49:
- ADD TEXT NOTE TO UPDATE J6900 FROM 518S0287 TO 518S0526 WHEN SYMBOL IS READY.
CSA PAGE 90:
- DELETE LVDS_VREFH AND LVDS_VREFL TO GROUND TO FIX LVDS GLITCH.
CSA PAGE 94:
- ADD TEXT NOTE TO CHANGE L9404 FROM 155S0303 TO 155S0348 WHEN SYMBOL IS READY.

M70 DVT TO K36 CHANGES

6/29/2007
CSA PAGE 4:
- CHANGE GOOD CPU FROM 337S3471(1.8G) TO 337S3463(2.0G)
- CHANGE BETTER CPU FROM 337S3456(2.0G) TO 337S3464(2.2G)
- CHANGE BEST CPU FROM 337S3464(2.2G) TO 337S3465(2.4G)
- CHANGE NB FROM 338S0426(500M) TO 343S0448(667M)
- CHANGE NB FROM 338S0427 TO 338S0434.
CSA PAGE 16:
- DISCONNECT GFX_VID<0> TO GND
- CONNECT GFX_VID<0> TO GFX_VID<3> ON NB
- ADD R1600 (0OHM, 0402) TO CONNECT GFX_VID<4> TO GND.
CSA PAGE 22:
- 5282976 ADD C2207 (0_LUP, 0402)
- SIZING DOWN R2205 FROM 0603 TO 0402 FOR PLACEMENT.
- CHANGE GFX_VID<1:4> TO GFX_VID<0:3>
- CHANGE TRAPPING FROM 0010 ON GFX_VID<1:4> TO 0001 ON GFX_VID<0:3>.
CSA PAGE 39:
- CHANGE J3900 FROM 514S0143 TO 514-0443.
- EPII BOM OPTION TABLE.
CSA PAGE 46:
- CHANGE J4600 FROM 353S1245 TO 353S1728.
- REMOVE MIN_NECK_WIDTH=0.3MM FROM PP5V_S3_USB2_EXTR/A.
- ADD NOSTUFF R4650 AND R4651.
CSA PAGE 47:
- CHANGE J4700 FROM 516S0251 TO 516S0588.
CSA PAGE 48:
- CHANGE J4800 FROM 518S0287 TO 518S0526.
- REPLACE BATTERY INTERFACE CIRCUIT WITH THE ONE ON M42B ESTAR.
CSA PAGE 94:
- 5040728 CHANGE L9404 FROM 155S0303 TO 155S0348.

7/5/2006
CSA PAGE 4:
- REPLACE ALL M70 WITH K36 (TEXT, BOM OPTIONS, 630 NUMBERS).
CSA PAGE 21:
- CHANGE C2173 FROM 128S0051 TO 128S0113 PER CE.
CSA PAGE 22:
- CHANGE C2700 FROM 128S0051 TO 128S0113 PER CE.
CSA PAGE 28:
- CHANGE R2800 FROM 518S0487 TO 518S0519.
CSA PAGE 46:
- REMOVE R4660 AND R4601 (U4675 BYPASS RESISTORS).
CSA PAGE 48:
- CHANGE R4810 FROM 518S0369 TO 518S0521.
CSA PAGE 49:
- CHANGE R4900 FROM M70 EMC1033 CIRCUIT TO M71 EMC1043 CIRCUIT.
- J5550 CHANGES FROM 2PIN TO 4PIN.
CSA PAGE 55:
- CHANGE J5501 FROM 518S0369 TO 518S0521.
CSA PAGE 56:
- CHANGE J5602 FROM 518S0487 TO 518S0519.
- CHANGE J5603 FROM 518S0369 TO 518S0521.
CSA PAGE 59:
- CHANGE J9000 FROM 518S0369 TO 518S0521.

7/6/2006
CSA PAGE 8:
- REMOVE NO_TEST=TRUE FOR LV833 COMP, LV833 FSET, 3V3S5 COMP, 3V3S5 FSET, 1V0S50 COMP, 1V0S50 FSET, IMVP6 BIAS, IMVP6 COMP, 5V3S5 RUNSS, 1V5S0_RUNSS.
- ADD FUNC TEST=TRUE FOR TRM_INSTACK_P7N.
- ADD FUNC TEST=TRUE FOR PP1V05_S0_P.
CSA PAGE 9:
- REMOVE ALIASES FOR GND CHASSIS_AUDIO_SPKRCOONN,GND_CHASSIS_AUDIO_SHIELD1,GND_CHASSIS_AUDIO_SHIELD2,GND_CHASSIS_AUDIO_SHIELD3,MIC_SHIELD_LVDS_R,MIC_SHLD_CONN.
- REMOVE ALIAS FOR =FWPWR_PRRON
- ADD SPN ALIASES FOR TP_CK505_SRC7_N/P.
- ADD SPN ALIASES FOR CK505_PCT2/4_CLK.
CSA PAGE 11:
- REMOVE R1290 TO R1296 ON CPU_VID<0:6>.
CSA PAGE 12:
- DELETE TEXT NOTE AND WITH RESET BUTTON.
CSA PAGE 13:
- RENAME LVDS_VREFH/L TO TP_LVDS_VREFH/L.
CSA PAGE 59:
- Add R2596 and R2596 FOR 10K PU ON GPIO6 AND GPIO17(EXTGPU_RST_L).
- CHANGE R2514 TO 100K.
CSA PAGE 59:
- CHANGE L2902 AND L2903 FROM 155S0302 TO 0OHM R2906 AND R2907.
- NOSTUFF C2907, C2910, C2914, C2911, C2914.
- CHANGE R2900, R2901 FROM 2.2OHM TO 0OHM.
- CHANGE R2902 FROM 10HM TO 0OHM.
CSA PAGE 61:
- REMOVE TEXT NOTE WILL CHANGE TO 606P.
CSA PAGE 62:
- RE-DRAW CPU VOLTAGE SENSE RC FILTERING.
CSA PAGE 62:
- RE-CONNECTED /SHDN INPUT OF U6801 SO THAT IT'S CONTROLLED BY U6200 PORTA VREF. - DISCONNECTED GPIO1 AND TERMINATED IT WITH A 10K PULL DOWN.
- ADDED A NO STUFF PULL-UP TO CODEC DVDV AT GPIO1.
- ADDED SMALL 15PF COMPENSATION CAP. TO U6201 FEEDBACK NETWORK (C6224).
CSA PAGE 67:
- CHANGED ALL TRANSIENT SUPPRESSORS TO 6.8V/100PF DEVICES (WERE ORIGINALLY 8V/100PF DEVICES).
- ADDED L6771 AND L6773 TO MIC INPUT EMI FILTER.
- REMOVED DZ672.
- ADDED R6740 NO STUFF.
CSA PAGE 68:
- CONNECTED MIC_SHLD_CONN TO GND_CHASSIS_AUDIO_MIC THROUGH R6854.
- ADDED R6895 NO STUFF.
CSA PAGE 71:
- RENAME CPU_VID_R<6:0> TO CPU_VID<6:0>.

7/10/2007
CSA PAGE 4:
- BOTH PART NUMBER CHANGES FROM 341S2085 TO 341S2196.
- SMC PART NUMBER CHANGES FROM 541S2088 TO 341S2198.
- UPDATE BEE CODES, Z55 FOR GOOD, Z56 FOR BETTER, Z57 FOR BEST.
CSA PAGE 8:
- ADD R4675 =PP3V3_S3_SMBUS_SMC_MGMT TO PP3V3_S3.
CSA PAGE 19:
- ADD CRITICAL TO U2900.
- ADD CRITICAL TO U4401.
CSA PAGE 41:
- CHANGE U4675 FROM APN 353S1505 TO APN 353S1742. (SMALL PACKAGE)
- ADD R4676 & R4671. (USB BYPASS ROUTING).
CSA PAGE 49:
- REMOVE ALIAS FOR =SMC_SMS_INT TO SMC_PG1 - SIGNAL SHOULD JUST BE CALLED SMC_SMS_INT.
- CHANGE R5077 FROM PULL-UP TO A PULL-DOWN RESISTOR AND NAME IT SMC_SMS_INT.
CSA PAGE 49:
- REMOVE CLK AND SMB_ME DATA ON SOUTHRIDGE DISCONNECTED FROM SMB_MGMT_CLK AND SMB_MGMT_DATA FROM SMC.B
- THE 10K PULL-UP RESISTORS (R5230 AND R5231), AND STILL REMAIN CONNECTED TO PP3V3_S3_SMBUS_SB_ME AND STAY ON THE SB SIDE.
- SMC MANAGEMENT SMBUS CONNECTOR:
- ADD TWO NEW 10K PULL-UP RESISTOR (R5232 & R5233) TO =PP3V3_S3_SMBUS_SMC_MGMT.B
- THE PULL-UP RESISTORS SHOULD BE CONNECTED BETWEEN SMB_MGMT_CLK AND SMB_MGMT_DATA TO =I2C_SMS_SCL AND =I2C_SMS_SDA OF THE NEW ACCELEROMETER.
CSA PAGE 53:
- ADD 2ND SMS (U5930).
CSA PAGE 62:
- CHANGED C6210 FROM A CASE-S LOUF TANT CAP TO A SMA-LF 3.3UF TANT CAP.
- MADE NO TEST ATTRIBUTE VISIBLE FOR NET_NCL_VRP CONNECTED TO PIN 37 OF U6200.
CSA PAGE 67:
- REMOVED NO STUFF RESISTORS R6730, R6731, AND R6732. ALSO REMOVED L6774.
- STUFFED R6740.
- MADE DZ6702, DZ6703, DZ6704, DZ6705, DZ6752, DZ6753, DZ6754, DZ6755, DZ6770, DZ6771B CRITICAL.
CSA PAGE 68:
- NO STUFFED R6854
CSA PAGE 74:
- CHANGE R7208 FROM 8.66K TO 15.8K.

7/11/2007
CSA PAGE 9:
- CHANGE Z0901 AND Z0906 FROM 998-1178 TO 998-1186 (NON-PLATED).
CSA PAGE 11:
- STUFF C3110 AND C3111.
CSA PAGE 12:
- STUFF C3210 AND C3211.
CSA PAGE 39:
- UPDATE PN FOR FANCY RJ45 CONNECTOR, 514-0475.
CSA PAGE 59:
- UPDATE PN FOR FANCY RJ45 CONNECTOR, 514-0475.
CSA PAGE 59:
- REMOVE R5907 (BECOMES R5931).
CSA PAGE 59:
- ADD R5931 (WAS R5077 BEFORE), 10K PD ON SMC_SMS_INIT.
- STUFF U5930 (DIGITAL ACCELEROMETER) CIRCUIT.

7/12/2007
CSA PAGE 43:
- CHANGE J4300 FROM 514-0289 TO 514-0456 (SAME JEDEC).
- UPDATE BOM OPTION TABLE FOR J4300.
- NORMAL CHANGES FROM 514-0359 TO 514-0456, FANCY CHANGES FROM 514-0316 TO 514-0476.
CSA PAGE 45:
- CHANGE J4600 AND J4601 FROM 514-0288 TO 514-0457 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J4600 AND J4601.
- NORMAL CHANGES FROM 514-0288 TO 514-0457, FANCY CHANGES FROM 514-0315 TO 514-0477.
CSA PAGE 67:
- ADD J4601 TITLE AUDIO: CODEC.
CSA PAGE 67:
- CHANGE J6700 FROM 514-0409 TO 514-0459 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J6700.
- NORMAL CHANGES FROM 514-0409 TO 514-0459, FANCY CHANGES FROM 514-0411 TO 514-0479.
- CHANGE J6750 FROM 514-0408 TO 514-0458 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J6750.
- NORMAL CHANGES FROM 514-0408 TO 514-0458, FANCY CHANGES FROM 514-0410 TO 514-0478.
CSA PAGE 75:
- CHANGE L7900 FROM 152S0302 TO 152S0670 FOR CORRECT AVL.
CSA PAGE 94:
- UPDATE BOM OPTION TABLE FOR J9401.
- NORMAL CHANGES FROM 514-0375 TO 514-0480, FANCY CHANGES FROM 514-0376 TO 514-0481.

7/13/2007
CSA PAGE 4:
- CHANGE BEST CPU FROM 337S3465(2.4GHZ) TO 337S3464(2.2GHZ).
CSA PAGE 38:
- CHANGE C3831 AND C3832 FROM 138S0582 TO 138S0554 (DON'T NEED LOW-PROFILE PARTS).

7/17/2007
CSA PAGE 59:
- UPDATE SYMBOL FOR U5930, VENDOR PART NUMBER CHANGES FROM SMB380 TO BMA150.

7/24/2007
CSA PAGE 4:
- CHANGE BETTER AND BEST CPU TO G0 STEPPING PARTS (FROM 337S3464 TO 337S3500).
CSA PAGE 38:
- STUFF R2242 AND NOSTUFF R2247.
CSA PAGE 49:
- CHANGE R5201 AND R5202 FROM 5.23K TO 2.94K.
- CHANGE R5211 AND R5212 FROM 16.5K TO 9.09K.

M70 EVT TO DVT CHANGES

8/9/2007
PER CE ALL SANYO POSCAPS HAVE NEW HF PART NUMBERS.
- ALL 128S0057 BECOME 128S0147.
- ALL 128S0073 BECOME 128S0164.
- ALL 128S0111 BECOME 128S0169.
- ALL 128S0113 BECOME 128S0160.
- ALL 128S0115 BECOME 128S0160.
- ALL 128S0123 BECOME 128S0160.
- ALL 128S0124 BECOME 128S0162.
- ALL 128S0129 BECOME 128S0135.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.
CSA PAGE 4:
- ADD BOM OPTION TABLE FOR ALL SANYO POSCAP TO USE HF PARTS.

Revision History

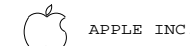
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SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE NONE SHEET 5 OF 76

Functional Test Points

Power Supply NO_TESTS

NO_TEST		
1E33	IMVP6_RBIAS	59A4 59B7
1E34	IMVP6_COMP	59A4 59B7
1E35	5VS5_RUNSS	63B5 65C5
1E36	1V5S0_RUNSS	58B1 61B5

Fan Connectors Battery Digital Connector

FUNC_TEST		
1E37	=PP5V_S0_FAN_RT	7A7 5004
1E38	FAN_RT_PWM	50B3
1E39	FAN_RT_TACH	50C3
1E40	=PP3V3_S0_FAN_RT	704 5004
1E41	SMC_FAN_1_CTL	44A8 50B4
1E42	SMC_FAN_1_TACH	44A8 5004

LPC+ Debug Connector

FUNC_TEST		
1E43	=PP3V42_G3H_LPCPLUS	781 46C6
1E44	=PP5V_S0_LPCPLUS	7A7 46C6
1E45	LPC_AD<0>	32D4 44C8 46C6
1E46	LPC_AD<1>	32D4 44C8 46C6
1E47	LPC_FRAME_L	32D4 44C8 46B6
1E48	PM_CLKRUN_L	24C8 37A5 44C5 46B6
1E49	BOOT_LPC_SPI_L	23B5 46B6
1E50	SMC_TMS	44B5 45C5 46B6
1E51	DEBUG_RESET_L	27D1 46B6
1E52	SMC_TRST_L	44C1 46B6
1E53	SMC_TDO	44B5 45C5 46B6
1E54	SMC_MD1	44C1 46B6
1E55	SMC_TX_L	43A8 44B8 44C5 45D5
1E56	FWH_INIT_L	46B6
1E57	PCI_CLK33M_LPCPLUS	46C5
1E58	LPC_AD<2>	29B3 46C4 75C3
1E59	LPC_AD<3>	32D4 44C8 46C4
1E60	INT_SERIRO	32D4 44C8 46C4
1E61	PM_SUS_STAT_L	24D5 44C5 46B4
1E62	SMC_TDI	44B5 45C5 46B4
1E63	SMC_TCK	44B5 45C5 46B4
1E64	SMC_RESET_L	44C1 45D7 46B4
1E65	SMC_NMI	44C1 46B4
1E66	SMC_RX_L	43A8 44B8 44C5 45D5
1E67	LINDACARD_GPIO	24A7 24D5 46B4

Other Func Test Points

FUNC_TEST		
1E68	=PP1V05_S0_REG	7D8 61B8
1E69	SMBUS_SMC_B_S0_SCL	47C5 76C3
1E70	SMBUS_SMC_B_S0_SDA	47C5 76C3
1E71	PPFW_SWITCH	38D3
1E72	SYS_LED_ANODE	40C5 45A3
1E73	SMC_LID	42C3 44B5 45C5 57A8
1E74	SMC_MANUAL_RST_L	45D8
1E75	SMC_CPU_VSENSE	44C5 46B1
1E76	ALL_SYS_PWRGD	27A5 44D8 58A3
1E77	PPVCORE_S0_CPU	7D7
1E78	PP1V05_S0_R	7D7
1E79	PP1V05_S0	7D7 45D2
1E80	PP1V8_S0	7D7
1E81	PP3V3_S0	7B7
1E82	PP5V_S0	7D4 45D1
1E83	PP1V2_ENET_S0	7A7
1E84	PP1V8_S3	7B5
1E85	PP3V3_S3	7A4
1E86	PP5V_S3	7A4
1E87	PP3V3_S5	7D1
1E88	PP5V_S5	7C1
1E89	PP3V42_G3H	701
1E90	PPBUS_G3H	7B1
1E91	PP18V5_G3H	7B1
1E92	PP0V9_S0	7D7
1E93	PP3V3_S3_BT_F	43D3
1E94	GND_BT_F	43C2

CLOCK NO_TESTS

NO_TEST		
1E37	CK505_CPU0_N	28C4 29D6 75D3
1E38	CK505_CPU0_P	28C4 29D6 75D3
1E39	CK505_CPU1_N	28C4 29D6 75D3
1E40	CK505_CPU1_P	28C4 29D6 75D3
1E41	CK505_CPU2_ITP_SRC10_N	28C4 29D6 75D3
1E42	CK505_CPU2_ITP_SRC10_P	28C4 29D6 75D3
1E43	CK505_DOT96_27M_N	28A4 29B6 75D3
1E44	CK505_DOT96_27M_P	28A4 29B6 75D3
1E45	CK505_LVDS_N	28B4 29C6 75C3
1E46	CK505_LVDS_P	28B4 29C6 75C3
1E47	CK505_PCIF1_CLK	28B6 29B6 75D3
1E48	CK505_SRC2_N	28B4 29C6 75C3
1E49	CK505_SRC2_P	28B4 29C6 75C3
1E50	CK505_SRC4_N	28B4 29C6 75C3
1E51	CK505_SRC4_P	28B4 29C6 75C3
1E52	CK505_SRC5_N	28B4 29C6 75C3
1E53	CK505_SRC5_P	28B4 29C6 75C3
1E54	CK505_SRC6_N	28B4 29B6 75C3
1E55	CK505_SRC6_P	28B4 29C6 75C3
1E56	CK505_SRC8_N	28A4 29B6 75C3
1E57	CK505_SRC8_P	28A4 29B6 75C3

FIREWARE NO_TESTS

NO_TEST		
1E58	FW_B_TPA_N_SPN	8D1
1E59	FW_B_TPA_P_SPN	8D1
1E60	FW_B_TPBIAS_SPN	8D1
1E61	FW_B_TPB_N_SPN	8D1
1E62	FW_B_TPB_P_SPN	8D1
1E63	FW_C_TPA_N_SPN	8D1
1E64	FW_C_TPA_P_SPN	8D1
1E65	FW_C_TPBIAS_SPN	8D1
1E66	FW_C_TPB_N_SPN	8D1
1E67	FW_C_TPB_P_SPN	8D1

LVDS NO_TESTS

NO_TEST		
1E68	LVDS_B_CLK_N_SPN	8D5
1E69	LVDS_B_CLK_P_SPN	8D5
1E70	LVDS_B_DATA_N0_SPN	8D5
1E71	LVDS_B_DATA_N1_SPN	8D5
1E72	LVDS_B_DATA_N2_SPN	8D5
1E73	LVDS_B_DATA_P1_SPN	8D5
1E74	LVDS_B_DATA_P2_SPN	8D5

NO_TEST

1E95	SMC_FAN_3_TACH	44A4 44A8
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Audio FUNC TEST

FUNC_TEST		
1E96	=PP5V_S0_AUDIO_AMP	7A7 54B8 54C8 54D8
1E97	=PP5V_S0_AUDIO	7A7 53A7 56C4
1E98	GND_AUDIO_AMP	8A4
1E99	GND_AUDIO_CODEC	8B4
1E100	ACZ_SDATIN<0>	8A5 53C7
1E101	ACZ_SDATOUT	8A5 53C7
1E102	ACZ_BITCLK	8A5 53C7
1E103	ACZ_RST_L	8A5 53B7
1E104	ACZ_SYNC	8A5 53C7

Battery FUNC TEST

FUNC_TEST		
1E105	SMC_BATT_ISET	44B5 66A8
1E106	SMC_BATT_CHG_EN	44C8 45B6 66A4
1E107	SMC_BC_AOK	66A5 45B6 57C3
1E108	SMC_ADAPTER_EN	45B3 57C4 38C6
1E109	SMC_BATT_TRICKLE_EN_L	44C8 45D5 45D6
1E110	SYS_ONEWIRE	44B8 45D5 57C8

USB FUNC TEST

FUNC_TEST		
1E111	TP_USB_EXCARD_P	8B2
1E112	TP_USB_EXCARD_N	8B2
1E113	TP_USB_EXTC_P	8B2
1E114	TP_USB_EXTC_N	8B2
1E115	USB2_BT_F_P	43C2
1E116	USB2_BT_F_N	43C2
1E117	USB2_3G_F_N	43A4
1E118	USB2_3G_F_P	43A4

DC-JACK FUNC TEST

1E119	ACIN_ENABLE_GATE	57C3 66A6
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Battery charger FUNC TEST

1E120	PPVBAT_G3H_CHGR_OUT	66B5 66C2
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INVERTER CONNECTOR FUNC TEST

FUNC_TEST		
1E121	PPBUS_ALL_INV_CONN	67D3
1E122	INV_GND	67D2
1E123	PP5V_INV_F	67D3
1E124	INV_BKLIGHT_PWM_L	67D2

MIC FUNC TEST

FUNC_TEST		
1E125	MIC_HI	55B3 56A6
1E126	MIC_LO	55B3 56A6
1E127	MIC_SHIELD	
1E128	MIC_HI_CONN	55B1 55D3
1E129	MIC_LO_CONN	55B1 55D3
1E130	MIC_SHLD_CONN	55A1 55D3 56A6

SPEAKER FUNC TEST

FUNC_TEST		
1E131	SPKRCONN_L_N_OUT	54C1 55C2
1E132	SPKRCONN_L_P_OUT	54C1 55C2
1E133	SPKRCONN_R_N_OUT	54C1 55C2
1E134	SPKRCONN_R_P_OUT	54C1 55C2
1E135	SPKRCONN_SUB_N_OUT	54B1 55C2
1E136	SPKRCONN_SUB_P_OUT	54B1 55C2

THERMAL FUNC TEST

FUNC_TEST		
1E137	THRM_HEATPIPE_P	49D6
1E138	THRM_HEATPIPE_N	49D6
1E139	THRM_DIMM_DX_F_N	49B6
1E140	THRM_DIMM_DX_F_P	49B6
1E141	THRM_FINSTACK_P	49C6
1E142	THRM_FINSTACK_N	49C6

FUNC TEST 1 OF 2

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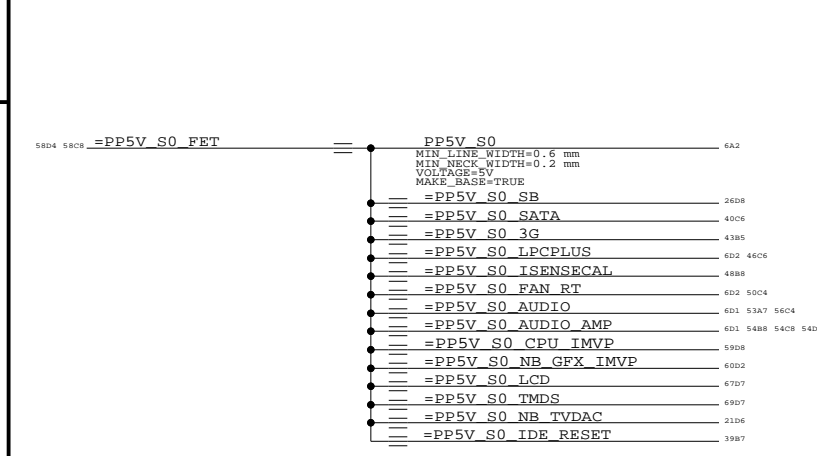
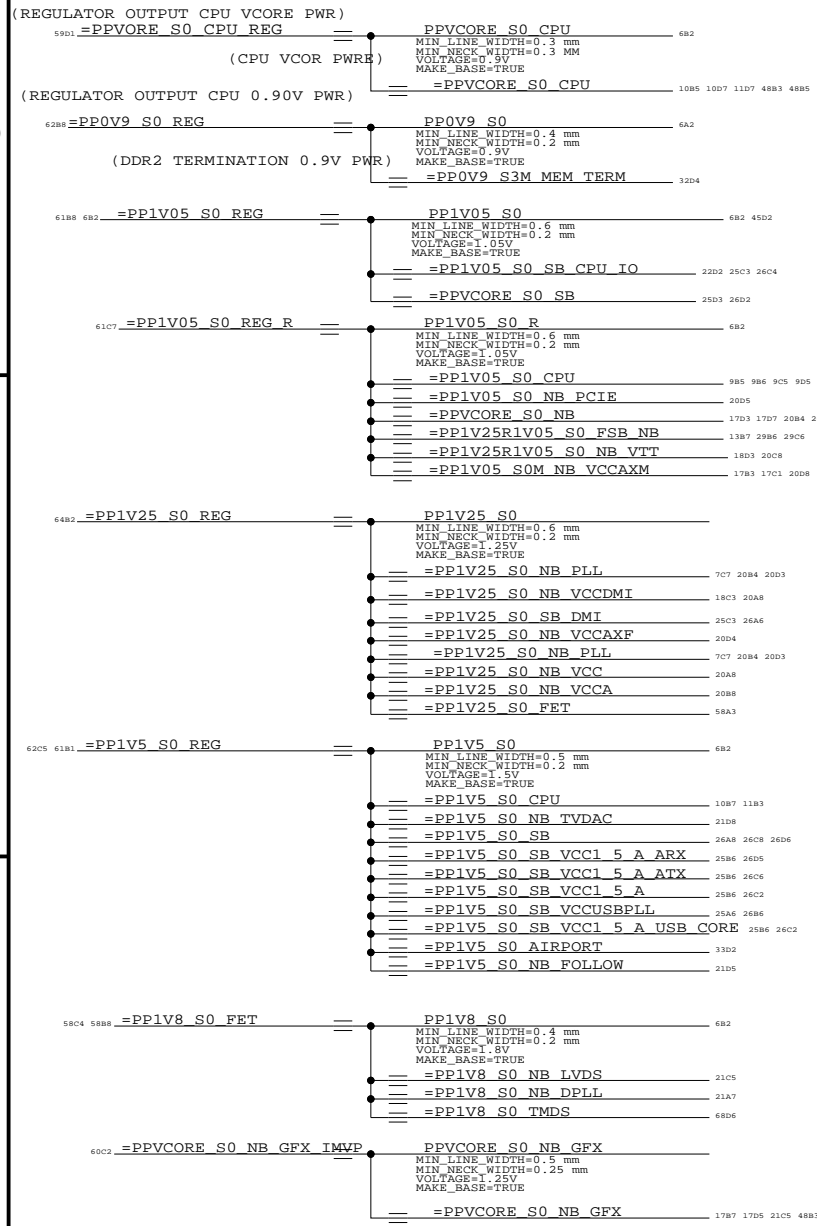
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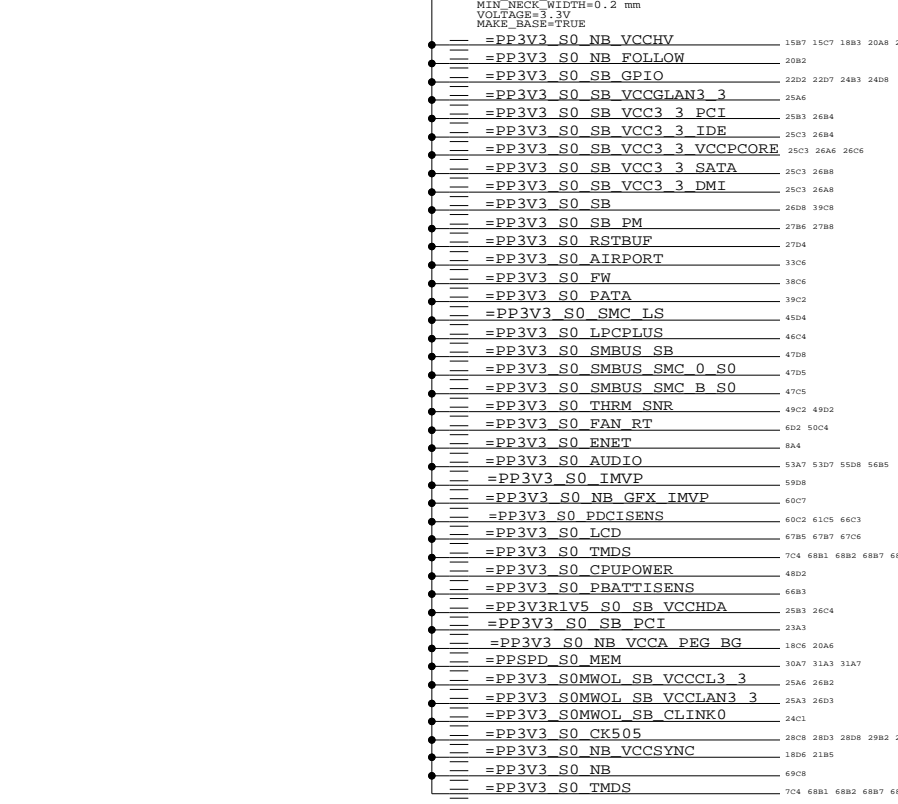
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NONE SHEET 6 OF 76

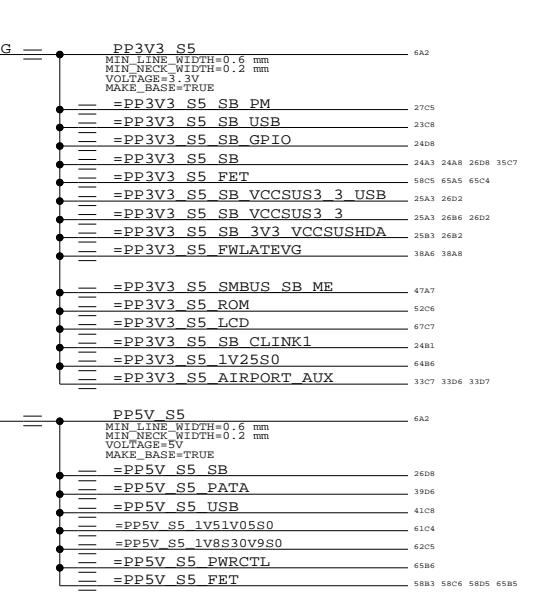
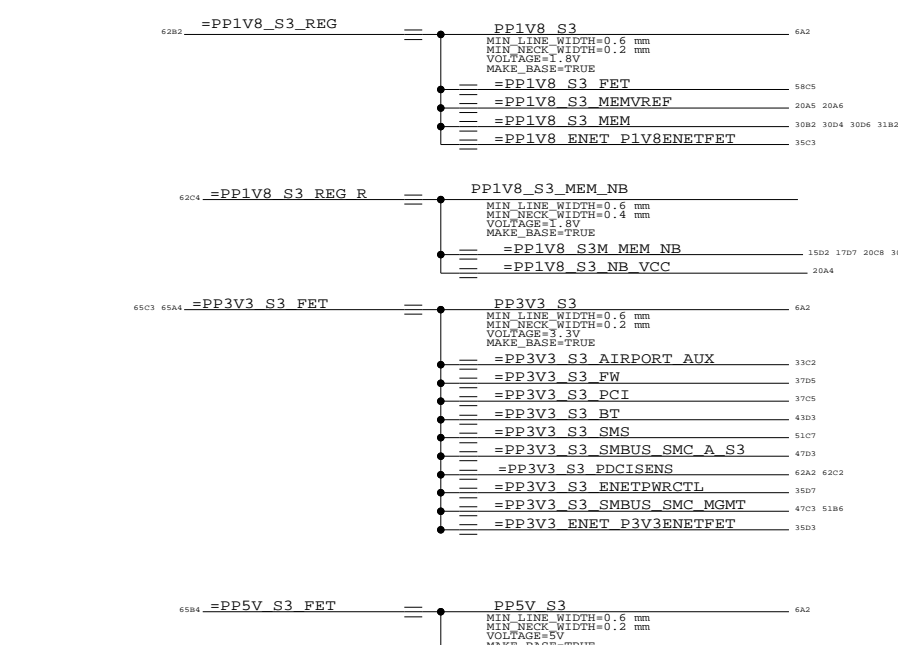
"S0,S0M" RAILS



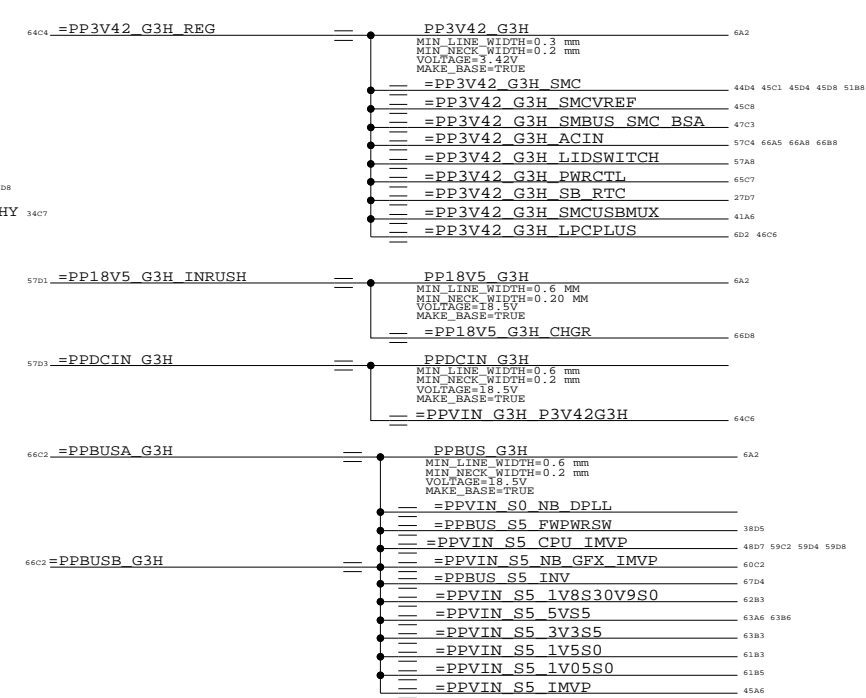
"S5" RAILS



"S3" RAILS



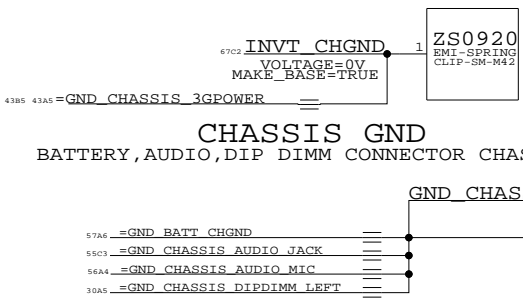
"G3H" RAILS



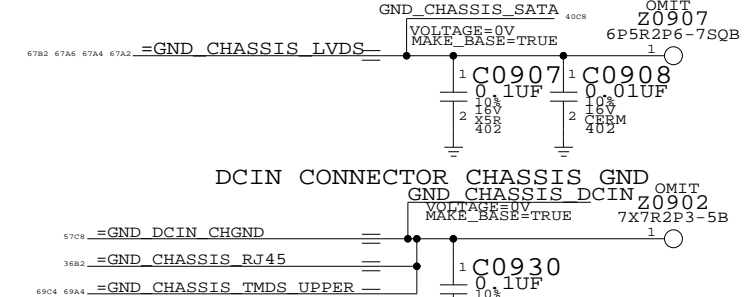
Power Aliases
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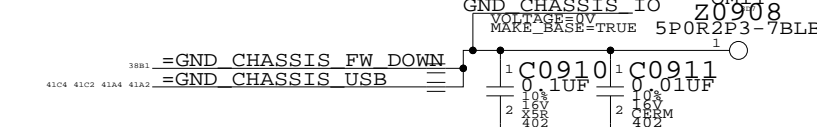
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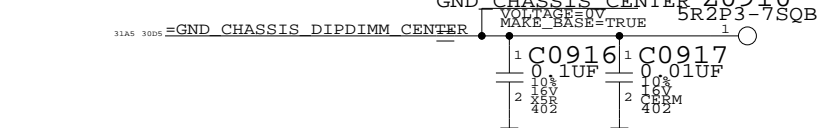
SATA, LVDS CONNECTOR CHASSIS GND



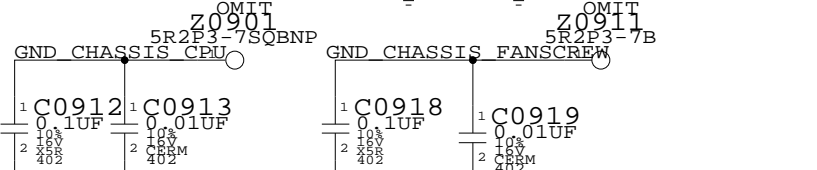
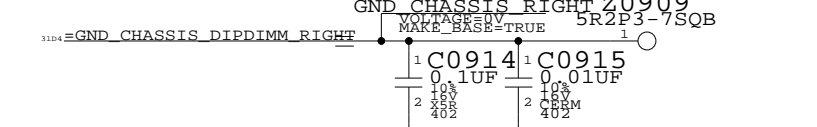
I/O CONNECTOR CHASSIS GND



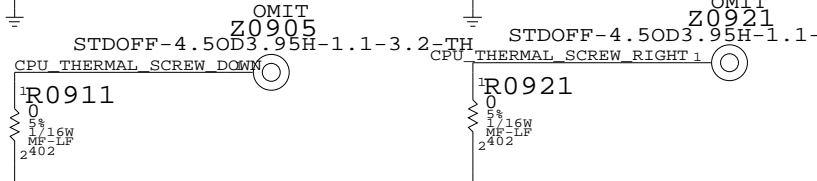
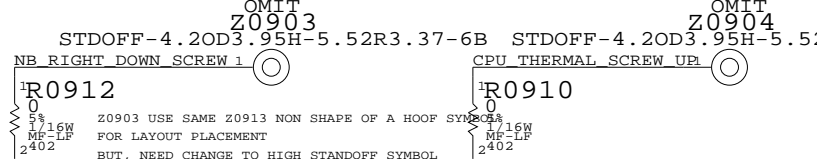
DIP DIMM CONNECTOR CHASSIS GND



DIP DIMM CONNECTOR CHASSIS GND



CPU HEATSINK STANDOFF SCREW HOLE



LVDS ALIASES

Table listing LVDS aliases such as LVDS B_CLK_N, LVDS B_CLK_P, LVDS B_DATA_N<0>, etc.

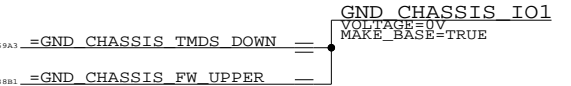
PCI_EXPRESS GRAPHICS ALIASES

Table listing PCI Express Graphics aliases such as PEG D2R N<0>, PEG D2R N<1>, PEG D2R N<2>, etc.

Table listing HDA aliases such as HDA_BIT_CLK, HDA_SYNC, HDA_RST_L, etc.

NB CFG ALIASES

Table listing NB CFG aliases such as NB_CFG<3>, NB_CFG<4>, NB_CFG<6>, etc.



SATA ALIASES

Table listing SATA aliases such as SATA B_D2R_N, SATA B_D2R_P, SATA B_R2D_C_N, etc.

PCI_EXP ALIASES

Table listing PCI Express aliases such as TP_PCIE_A_D2R_N, TP_PCIE_A_D2R_P, TP_PCIE_A_R2D_C_N, etc.

CLOCK ALIASES

Table listing Clock aliases such as TP_CK505_SRC1_N, TP_CK505_SRC1_P, TP_CK505_SRC3_N, etc.

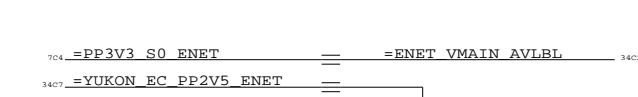
SB ALIASES

Table listing SB aliases such as VR_PWRGD_CLKEN, SB_CLINK_MPWRK, SB_SATA_CLKREQ_L, etc.

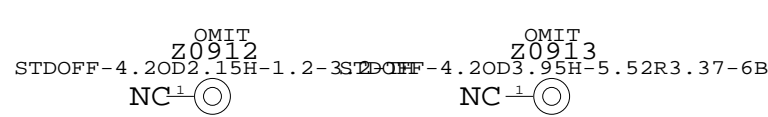
SO-DIMM ALIASES

Table listing SO-DIMM aliases such as MEM_A_A<15>, MEM_B_A<15>, TP_MEM_CLKP2, etc.

Ethernet ALIASES



AIRPORT CARD STANDOFF SCREW HOLE



FIREWIRE ALIASES

Table listing FireWire aliases such as FW_B_TPBIAS, FW_B_TPA_P, FW_B_TPA_N, etc.

USB PORT [0] = External USB2.0 Port A

Table listing USB aliases for Port 0 such as USB2_EXTN_P, USB2_EXTN_N, EXTUSB_OC_L, etc.

USB PORT [1] = PCI-E Mini Card

Table listing USB aliases for Port 1 such as USB2_AIRPORT_P, USB2_AIRPORT_N, USB2_AIRPORT_N, etc.

USB PORT [2] = 3G USB

Table listing USB aliases for Port 2 such as USB2_3G_P, USB2_3G_N, USB_EXTD_P, etc.

USB PORT [3] = CAMERA

Table listing USB aliases for Port 3 such as USB2_CAMERA_P, USB2_CAMERA_N, USB_CAMERA_P, etc.

USB PORT [4] = IR CONTROLLER

Table listing USB aliases for Port 4 such as USB2_IR_P, USB2_IR_N, USB_IR_P, etc.

USB PORT [5] = Trackpad(Geyser)

Table listing USB aliases for Port 5 such as USB2_GEYSER_P, USB2_GEYSER_N, USB_TPAD_P, etc.

USB PORT [6] = BLUETOOTH

Table listing USB aliases for Port 6 such as USB2_BT_P, USB2_BT_N, USB_BT_P, etc.

USB PORT [7] = External USB2.0 Port B

Table listing USB aliases for Port 7 such as USB2_EXTP_P, USB2_EXTP_N, USB2_EXTB_P, etc.

USB PORT [8] = Unused

Table listing USB aliases for Port 8 such as TP_USB_EXCARD_P, TP_USB_EXCARD_N, USB_EXCARD_P, etc.

USB PORT [9] = Unused

Table listing USB aliases for Port 9 such as TP_USB_EXTC_P, TP_USB_EXTC_N, USB_EXTC_P, etc.

ANALOG SWITCH GPIO

Table listing analog switch GPIO aliases such as PM_EXTTTS_L<0>, PM_EXTTTS_L<1>, etc.

NB ALIASES

Table listing NB aliases such as GFX_VR_EN, NB_CLKMPWRK, NB_CLK96M_DOT_P, etc.

Table with columns: PART#, QTY, DESCRIPTION, REFERENCE DESIGNATOR(S), BOM OPTION. Lists thermal standoffs.

SIGNAL ALIAS /RESET

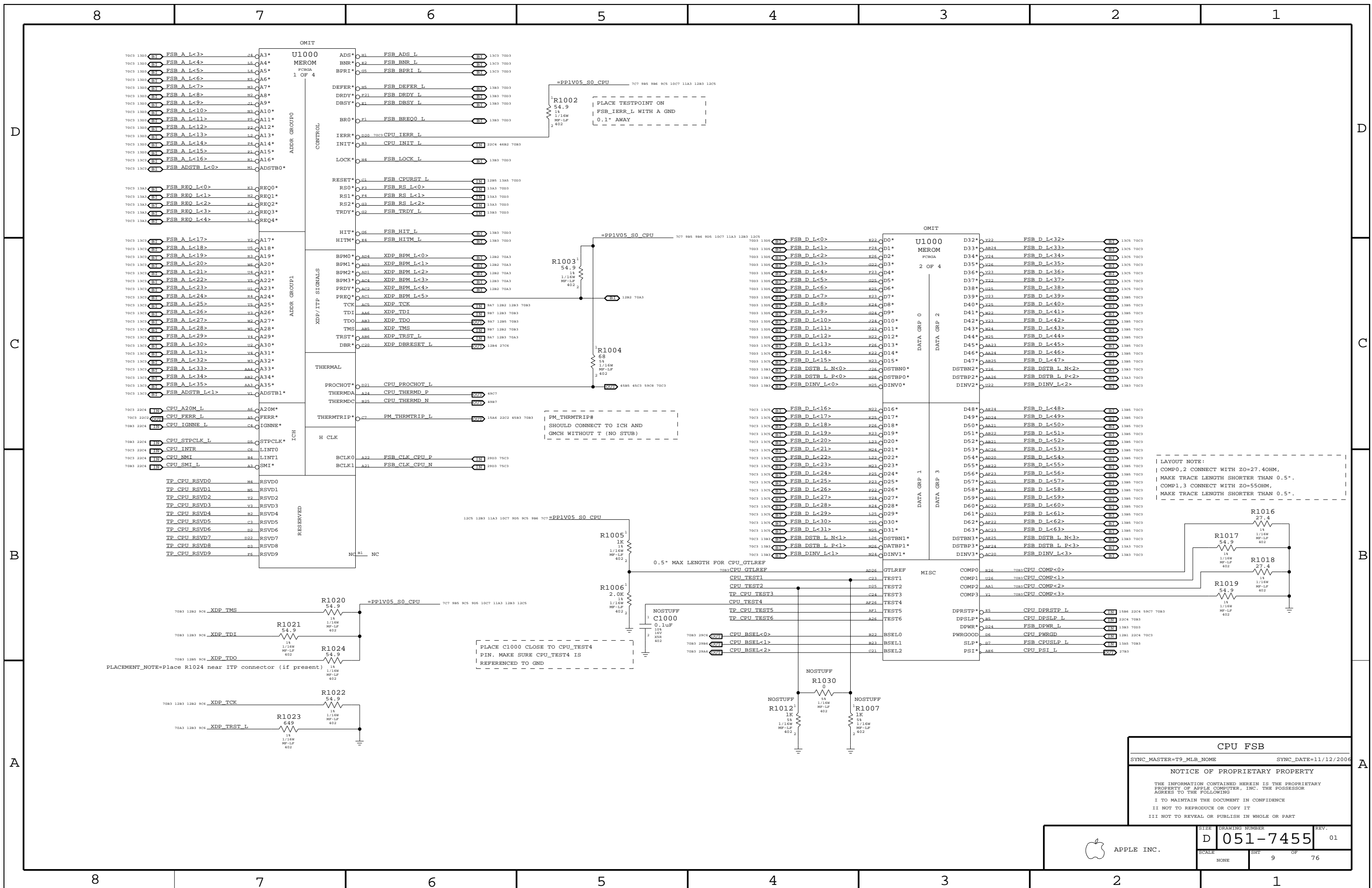
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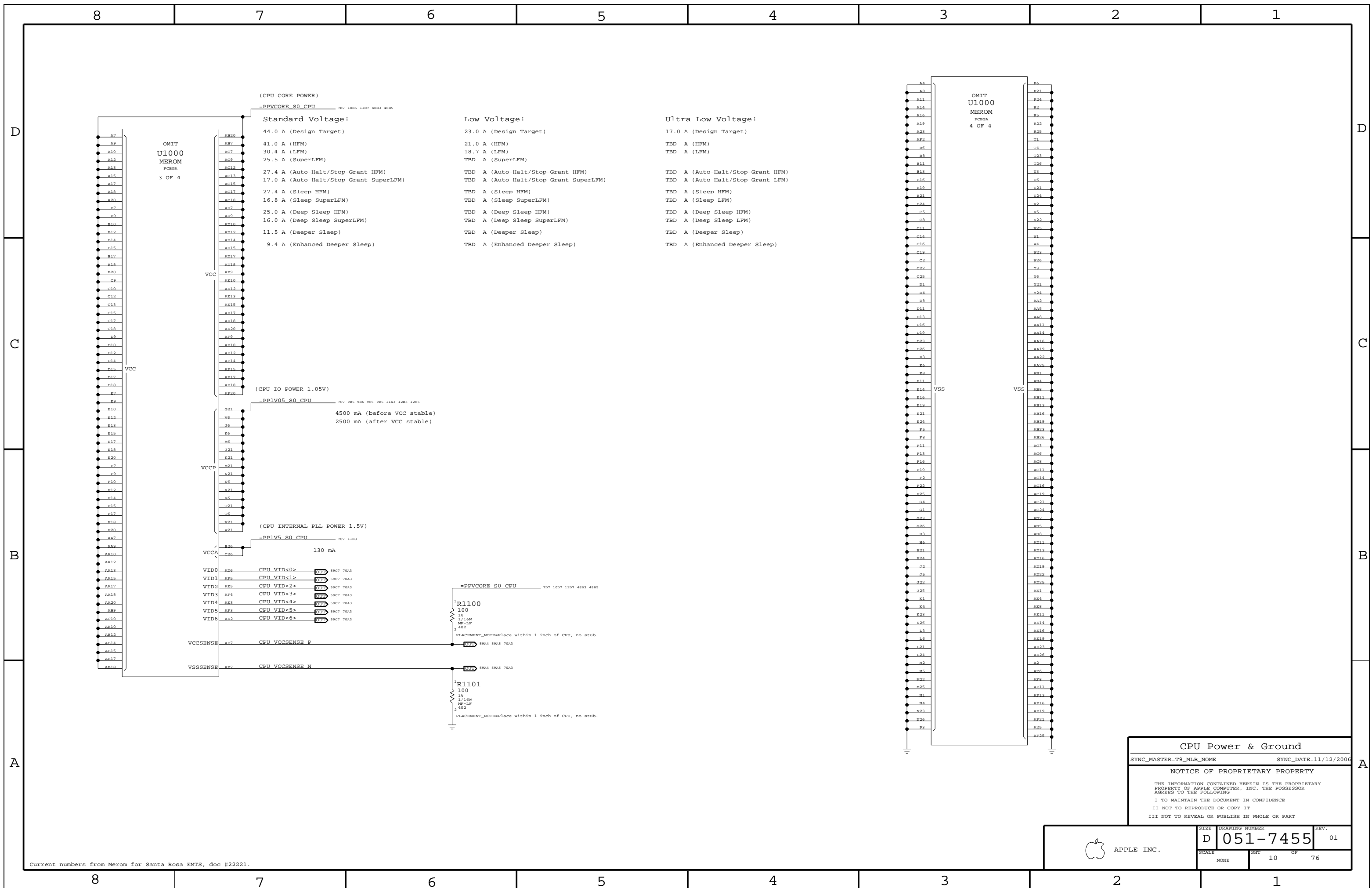
Table with columns: SIZE, DRAWING NUMBER, REV. Drawing number: D 051-7455, Rev: 01. Scale: NONE, Sheet: 8 OF 76.



LAYOUT NOTE:
 COMP0,2 CONNECT WITH Z0=27.4OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMP1,3 CONNECT WITH Z0=55OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB
 SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/12/2006
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APPLE INC.	DRAWING NUMBER D 051-7455	REV. 01
	SCALE NONE	SHEET 9 OF 76



CPU Power & Ground

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/12/2006

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		10	76

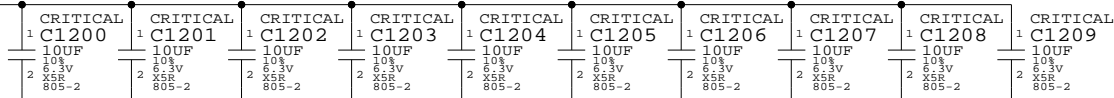
Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU VCORE HF AND BULK DECOUPLING

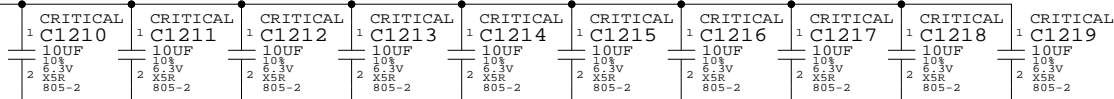
4x 330uF, 20x 10uF 0805

4885 4883 1007 1085 707 PPVCORE_S0_CPU

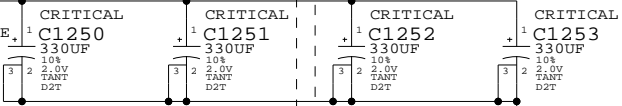
LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)



LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)



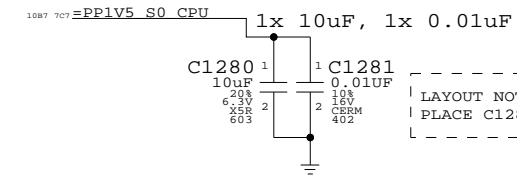
LAYOUT NOTE:
PLACE ON BOTTOMSIDE



LAYOUT NOTE:
PLACE ON BOTTOMSIDE

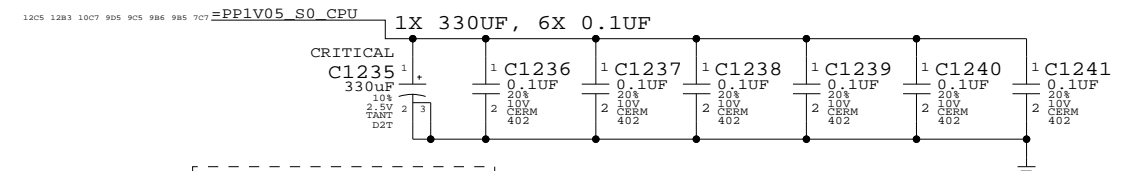
C1250, C1251, C1252 AND C1253 NEED TO USE 6mOHM CAPS.

VCCA (CPU AVdd) DECOUPLING



LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING



LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

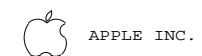
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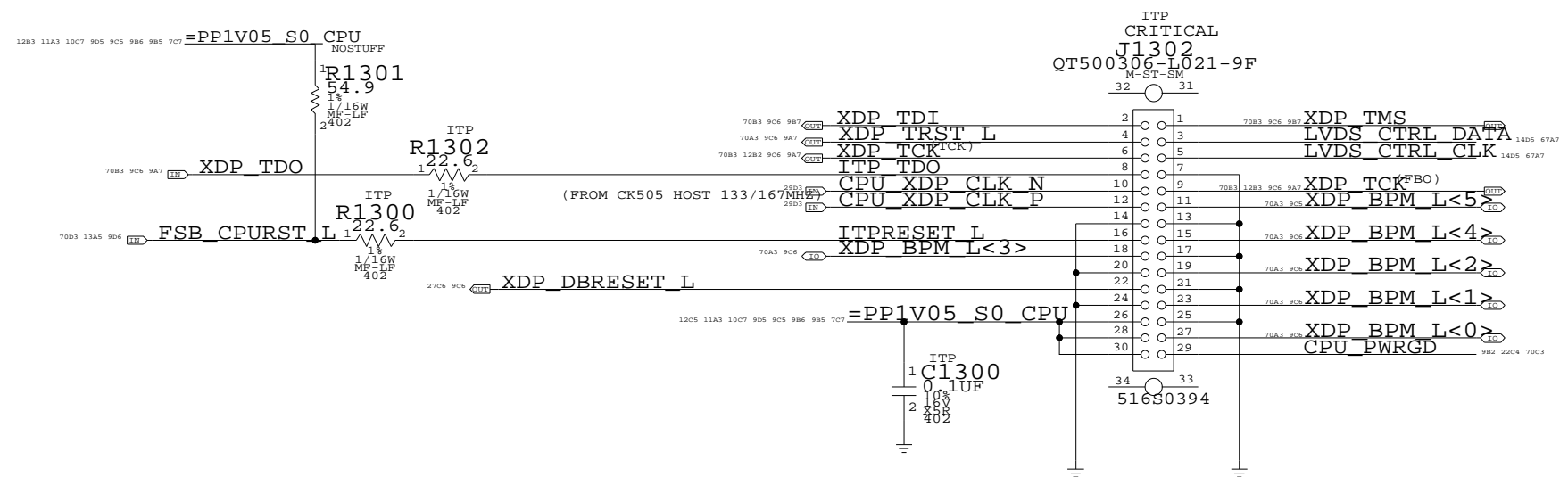
APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE SHEET OF 76

CPU ITP700FLEX DEBUG SUPPORT



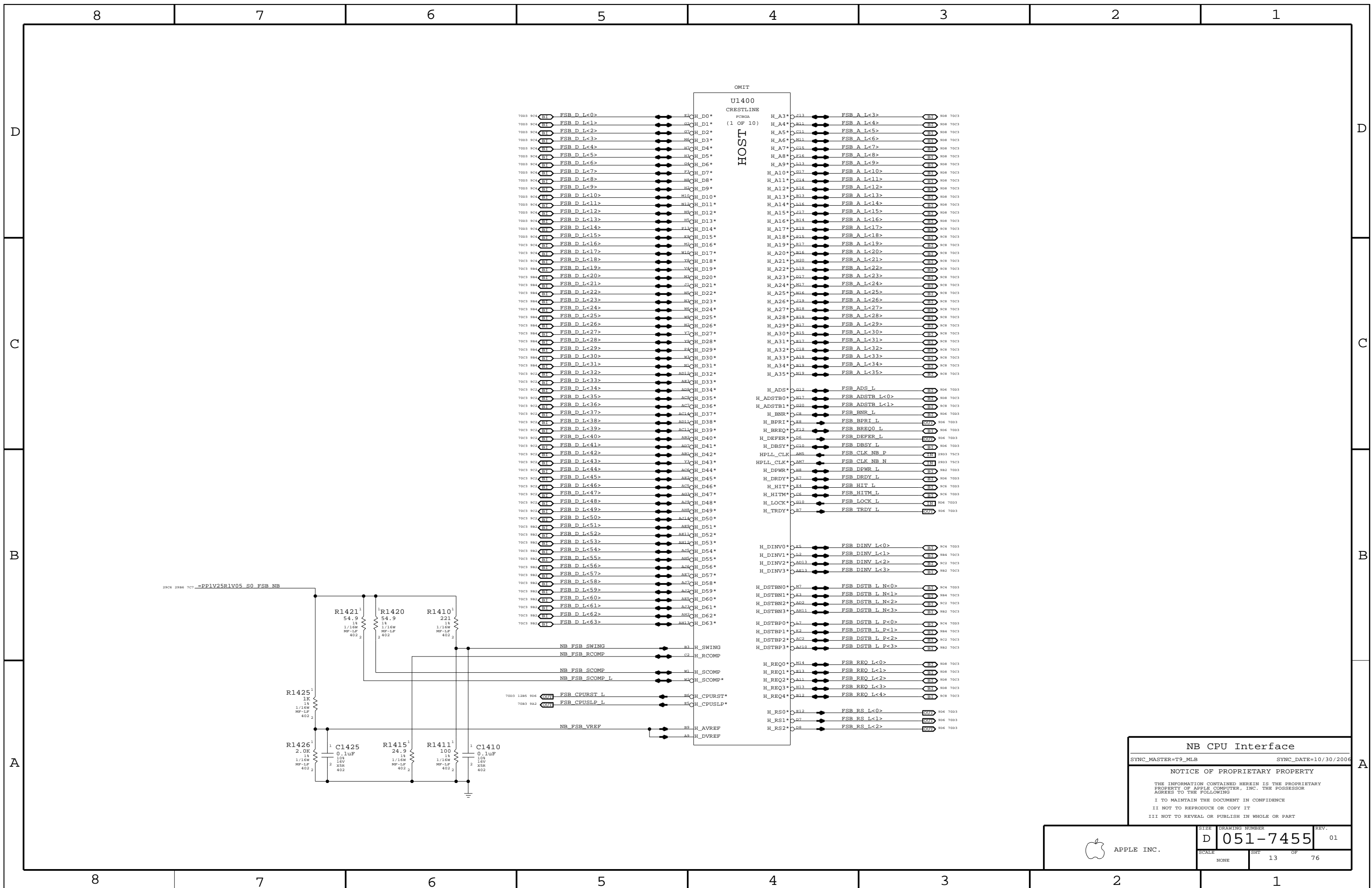
(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 965GM CHIPSET SYSTEM.
 (DEBUG PORT ACTIVE)
 (DBR# TO ICH8M SYS_RST*, AND WITH SYSTEM RESET LOGIC
 (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
 CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7455	REV. 01
	SCALE NONE	SHEETS 12 OF 76	



NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7455	REV.: 01
	SCALE: NONE	SHEET: 13	OF: 76

LVDS Disable
 Can leave all signals NC if LVDS is not implemented.
 Tie VCC_TX_LVDS and VCCA_LVDS to GND.
 If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC
 Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

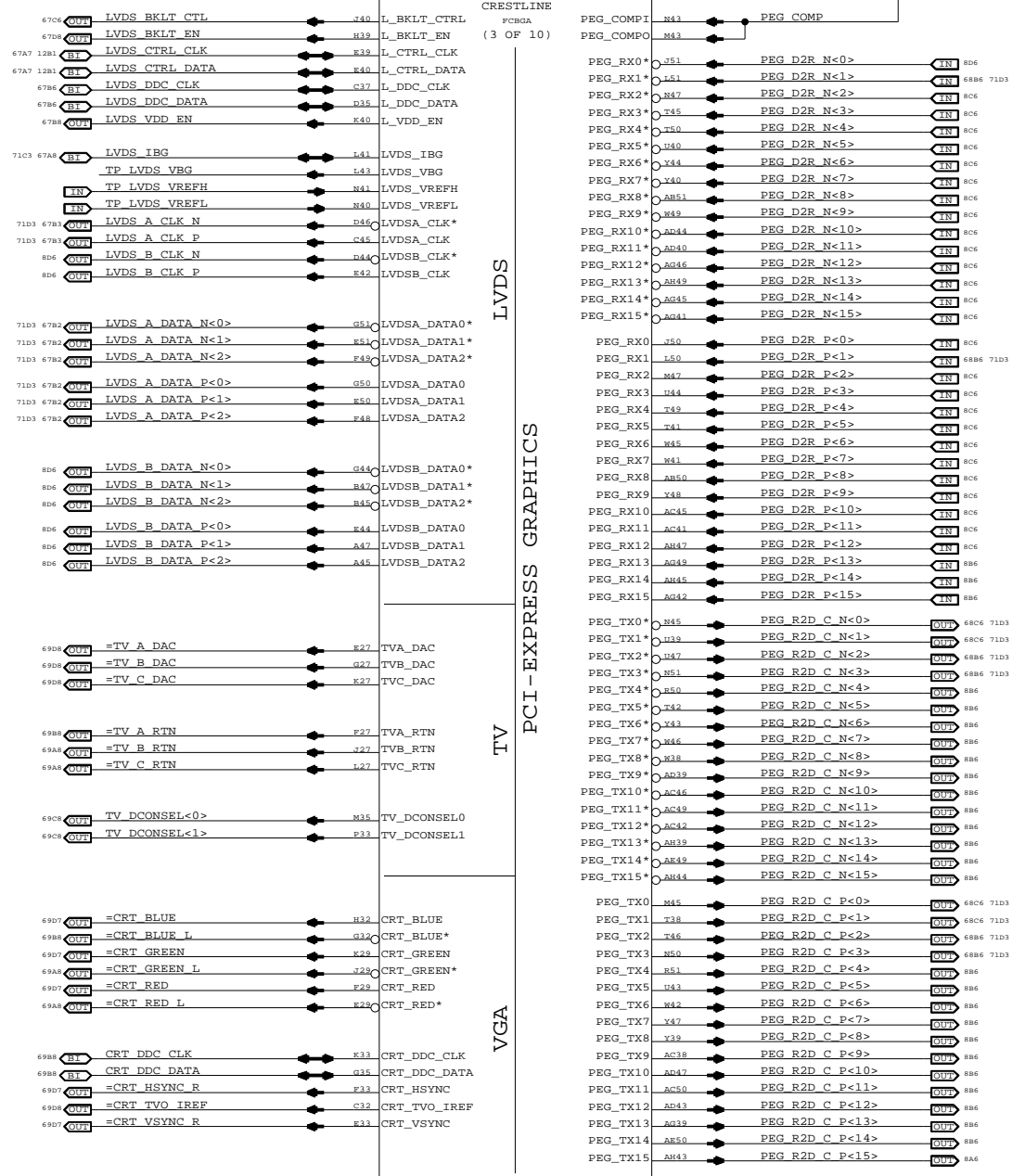
TV-Out Disable / CRT Enable
 Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_CRT_DAC can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable
 Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable
 Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
 Can tie the following rails to GND:
 VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCCD_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable
 Follow instructions for LVDS and CRT & TV-Out Disable above.
 Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
 Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
 Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
 Tie VCCA_DPLL and VCCA_DPLL to VCC (VCore).
 Tie VCC_AXG and VCC_AXG_NCTF to GND.
 Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function
 SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

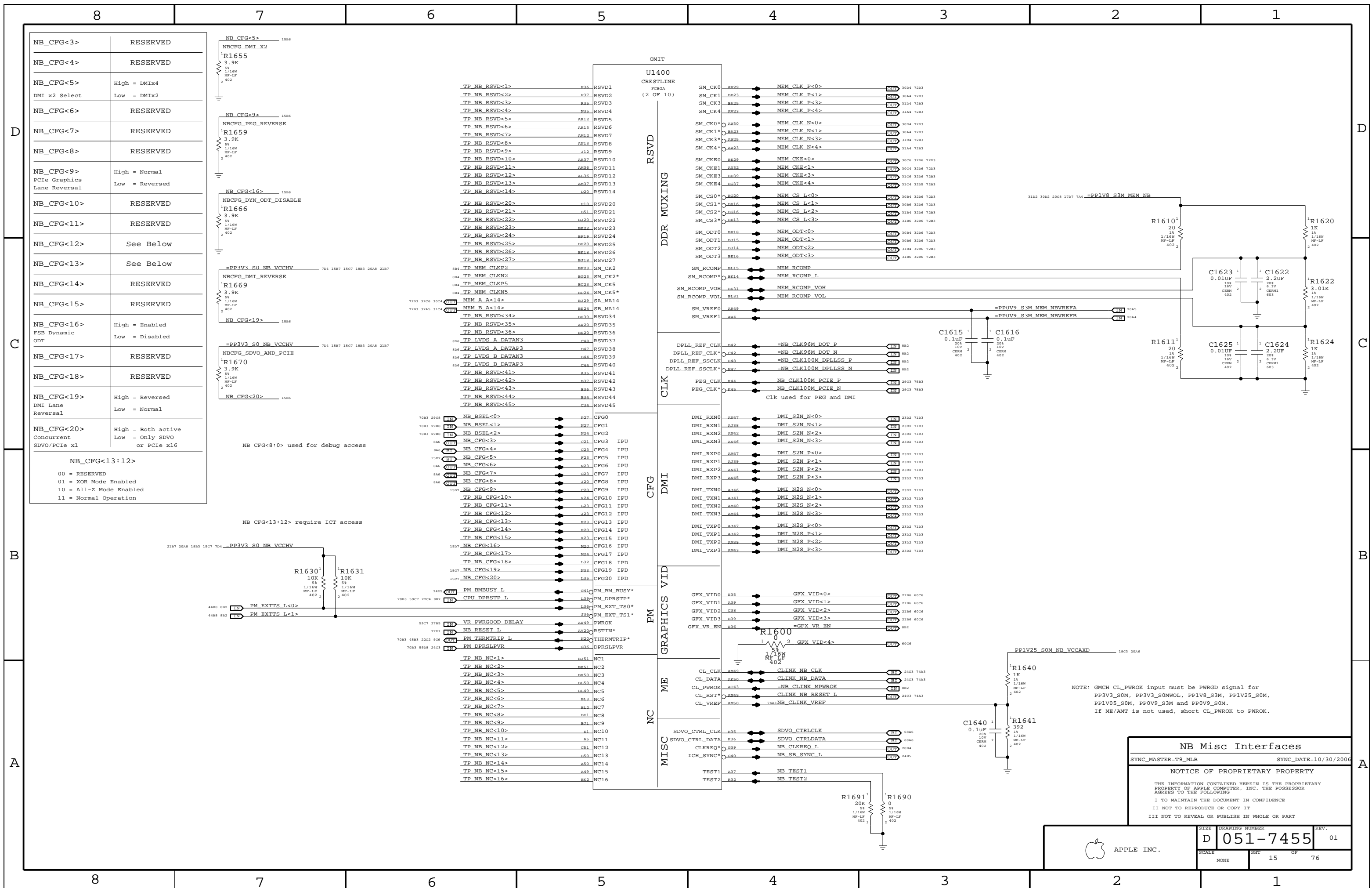
SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006
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APPLE INC. DRAWING NUMBER: D 051-7455 REV. 01
 SCALE: NONE SHEET: 14 OF 76



NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIX4 Low = DMIX2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed Low = Normal
NB_CFG<20>	High = Both active Low = Only SDVO or PCIe x1

NB_CFG<13:12>
 00 = RESERVED
 01 = XOR Mode Enabled
 10 = All-Z Mode Enabled
 11 = Normal Operation

NB_CFG<8:0> used for debug access

NB_CFG<13:12> require ICT access

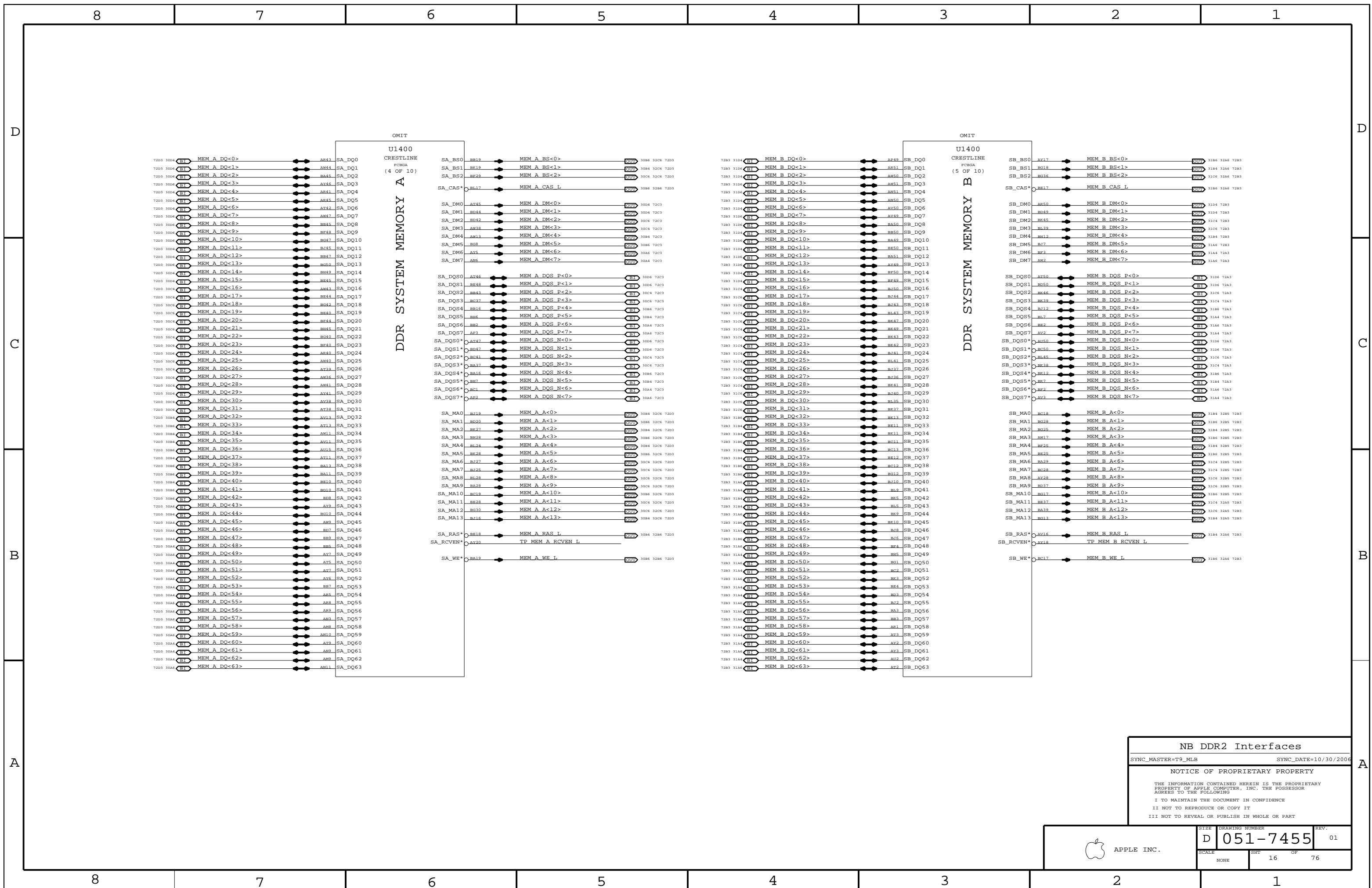
NB Misc Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

NOTICE OF PROPRIETARY PROPERTY

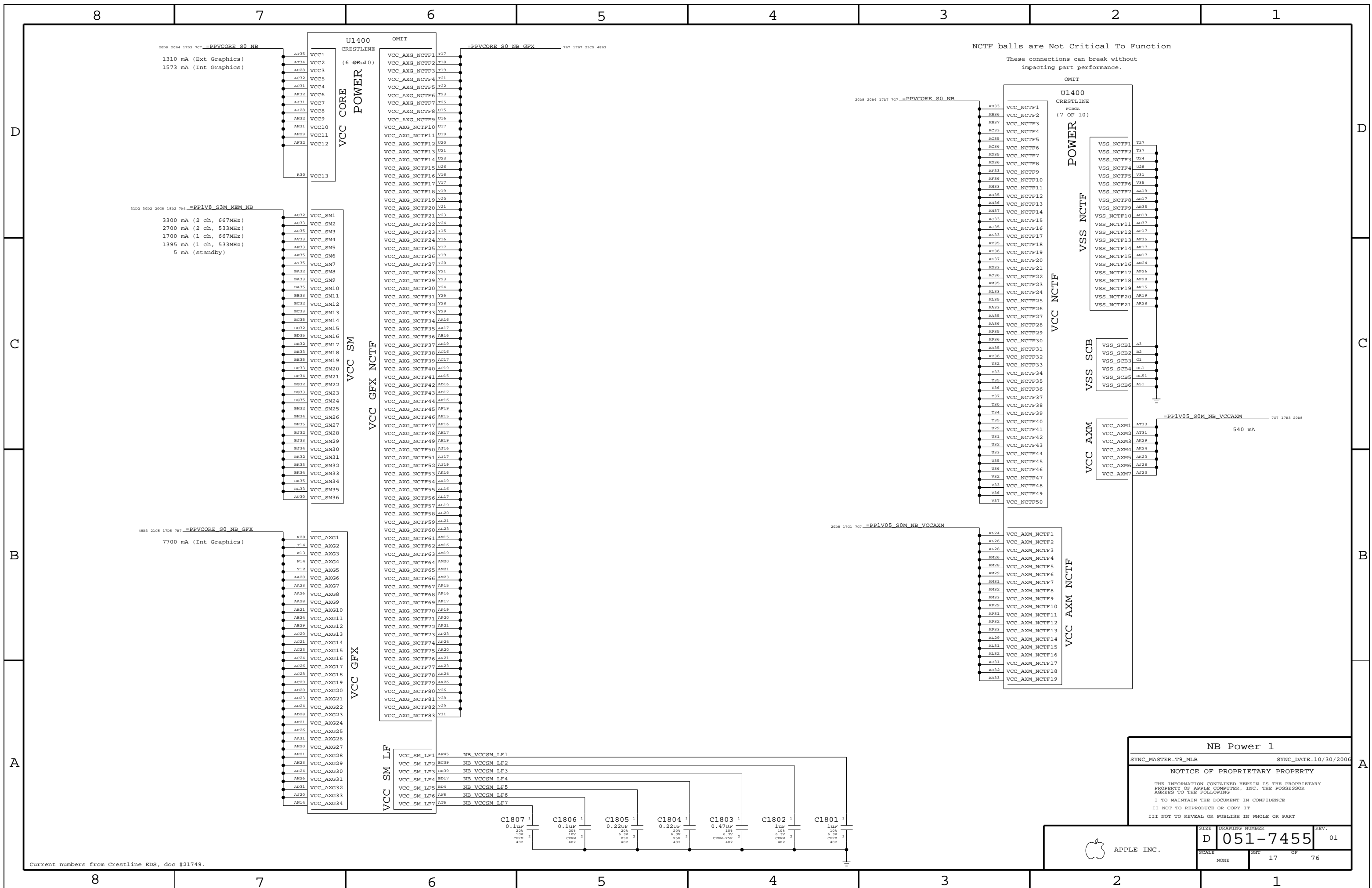
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APPLE INC.	SCALE	SHEET	OF	REV.
	NONE	15	76	01



NB DDR2 Interfaces
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APPLE INC.	DRAWING NUMBER D 051-7455	REV. 01
SCALE NONE	SHEET 16	OF 76



NCTF balls are Not Critical To Function
 These connections can break without impacting part performance.

2008 2084 1703 707 =PPVCORE_S0_NB
 1310 mA (Ext Graphics)
 1573 mA (Int Graphics)

3102 3002 2008 1502 744 =PPIV8_S3M_MEM_NB
 3300 mA (2 ch, 667MHz)
 2700 mA (2 ch, 533MHz)
 1700 mA (1 ch, 667MHz)
 1395 mA (1 ch, 533MHz)
 5 mA (standby)

4883 2105 1705 787 =PPVCORE_S0_NB_GFX
 7700 mA (Int Graphics)

2008 2084 1707 707 =PPVCORE_S0_NB

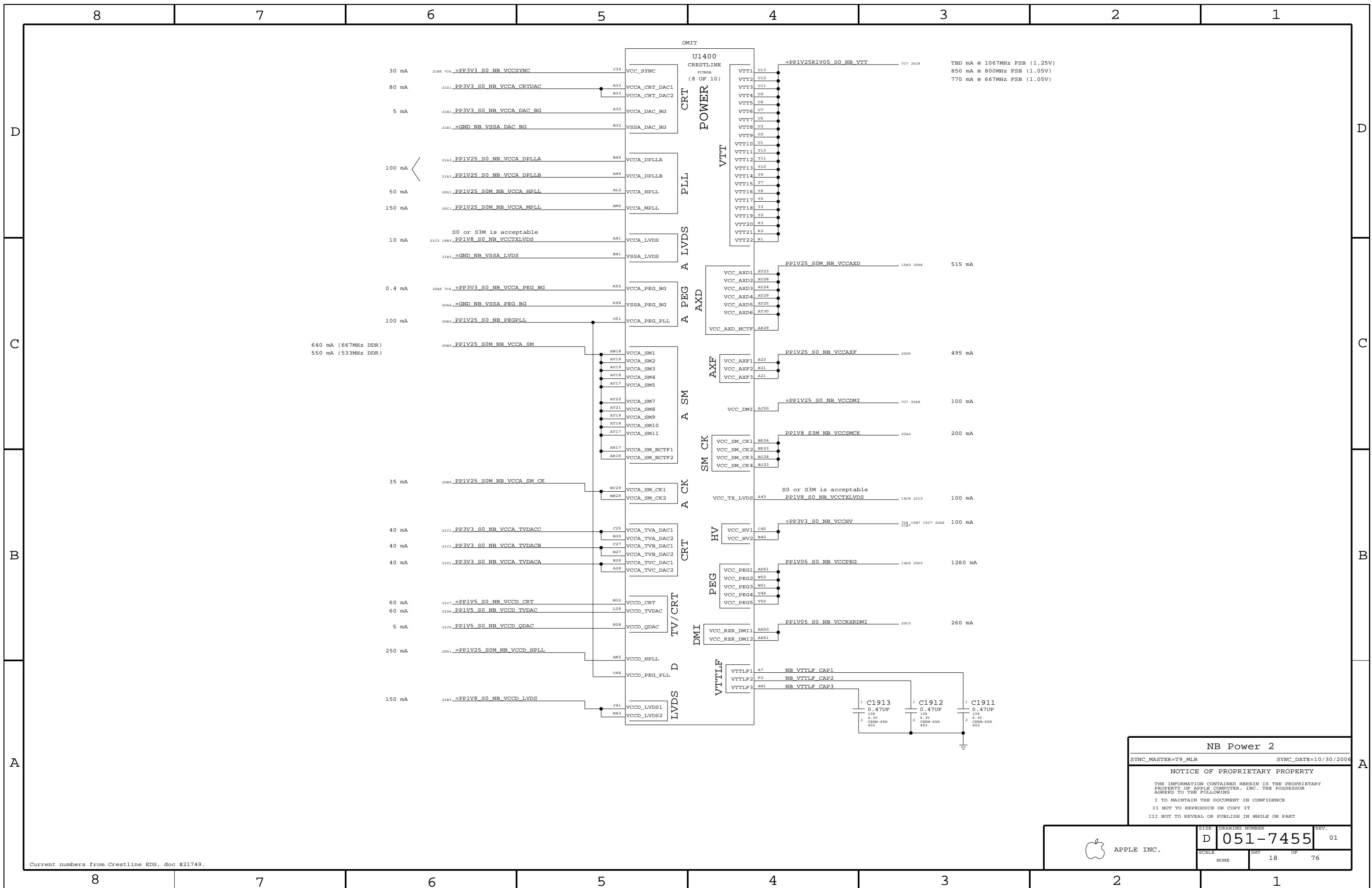
2008 1701 707 =PPIV05_S0M_NB_VCCAXM

NB Power 1
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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APPLE INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
		SHT	OF
		17	76

Current numbers from Crestline EDS, doc #21749.

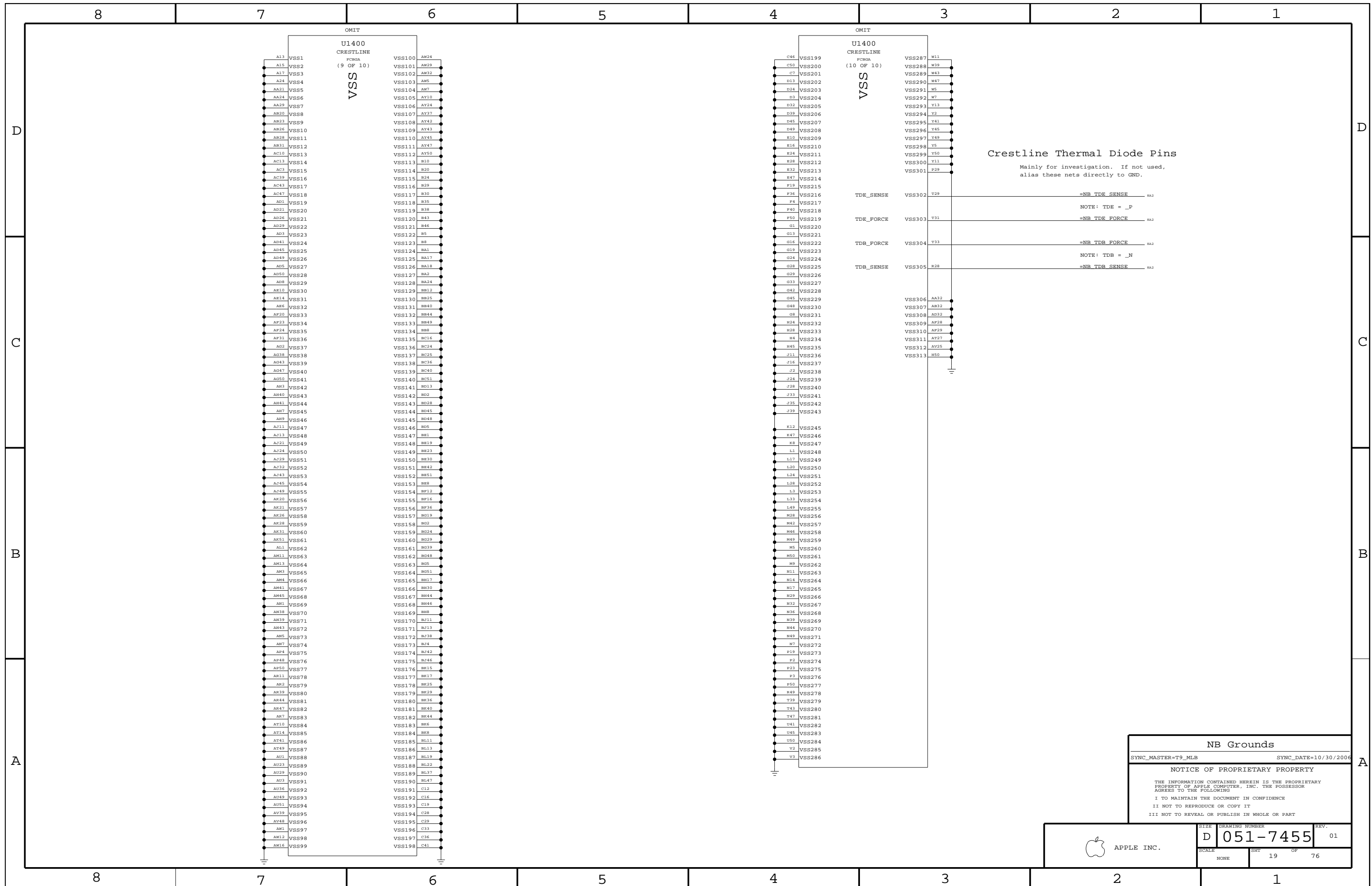


NB Power 2
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-7455	01
SCALE		SHT	OF
		18	76

Current numbers from Crestline EDS, doc #21749.

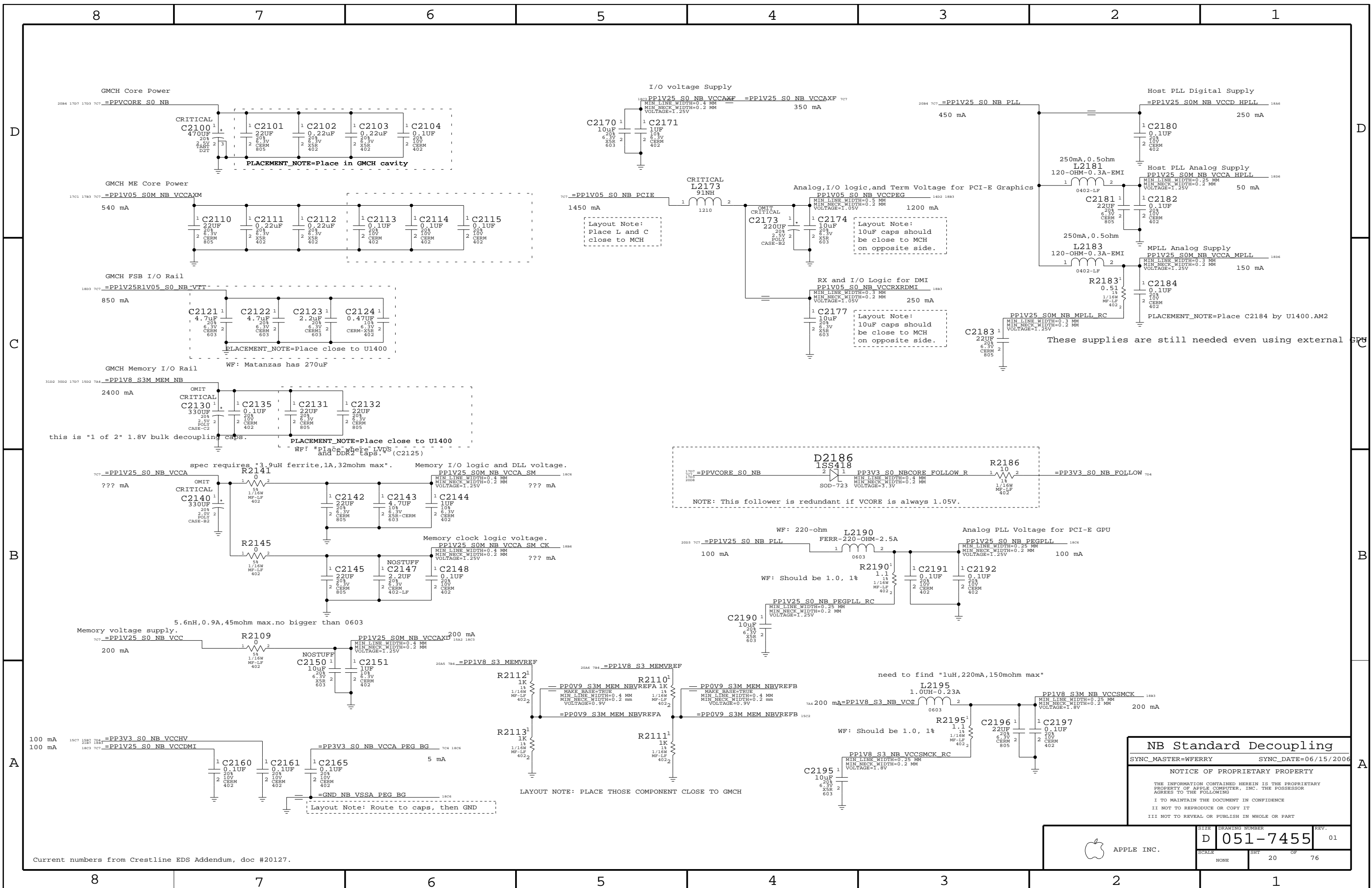


Crestline Thermal Diode Pins
 Mainly for investigation. If not used,
 alias these nets directly to GND.

TDE_SENSE VSS302 =NB TDE_SENSE BA.2
 NOTE: TDE = _P
 TDE_FORCE VSS303 =NB TDE_FORCE BA.2
 TDB_FORCE VSS304 =NB TDB_FORCE BA.2
 NOTE: TDB = _N
 TDB_SENSE VSS305 =NB TDB_SENSE BA.2

NB Grounds
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006
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 APPLE INC.	SIZE DRAWING NUMBER D 051-7455	REV. 01
	SCALE NONE	SHEET 19 OF 76



NB Standard Decoupling

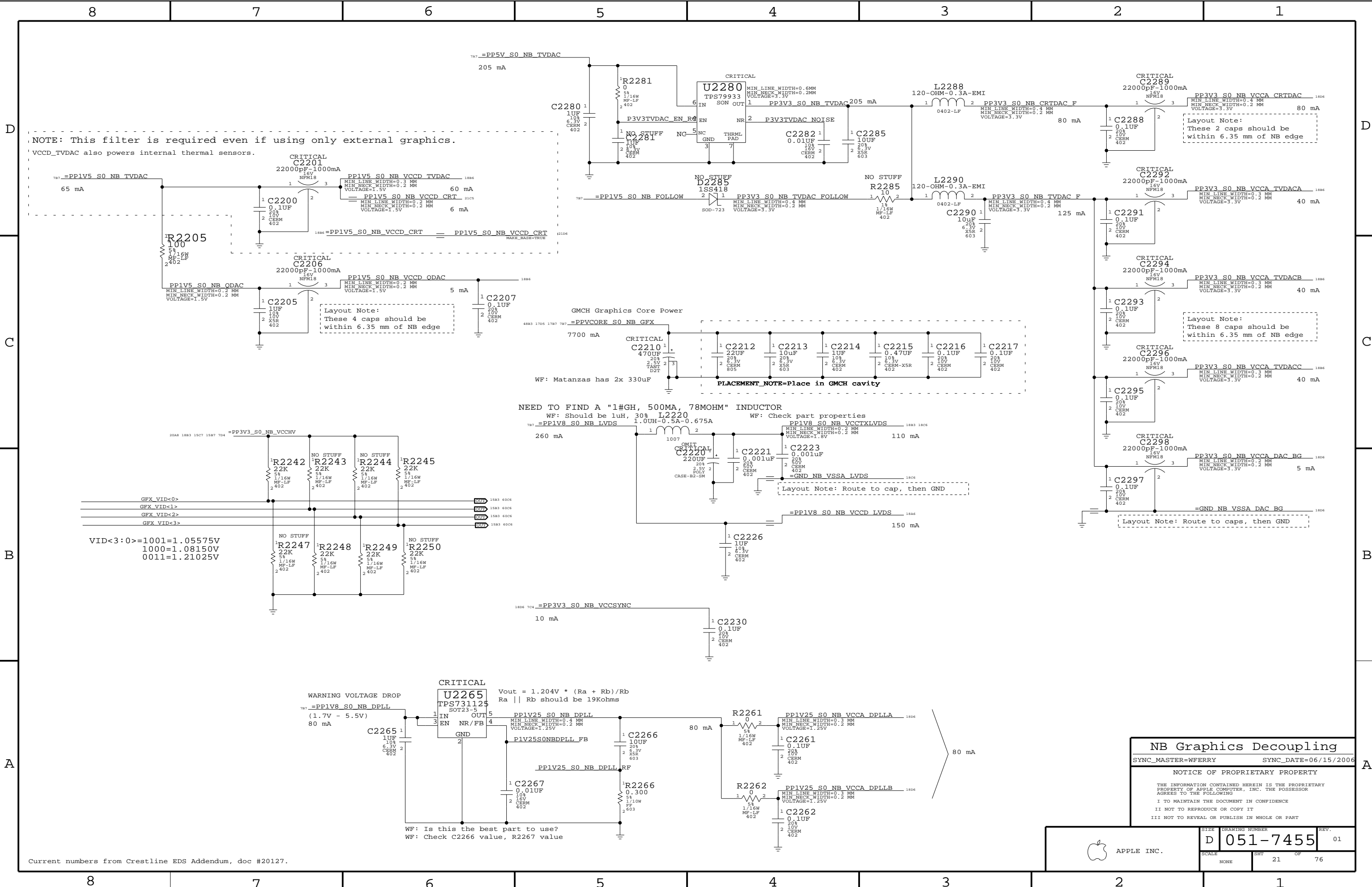
SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	SHT	OF	76
NONE	20		

Current numbers from Crestline EDS Addendum, doc #20127.



NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

Layout Note:
These 8 caps should be
within 6.35 mm of NB edge

Layout Note: Route to cap, then GND

Layout Note: Route to caps, then GND

NEED TO FIND A "1GH, 500MA, 78MOHM" INDUCTOR
WF: Should be 1uH, 30% L2220

WF: Is this the best part to use?
WF: Check C2266 value, R2267 value

NB Graphics Decoupling

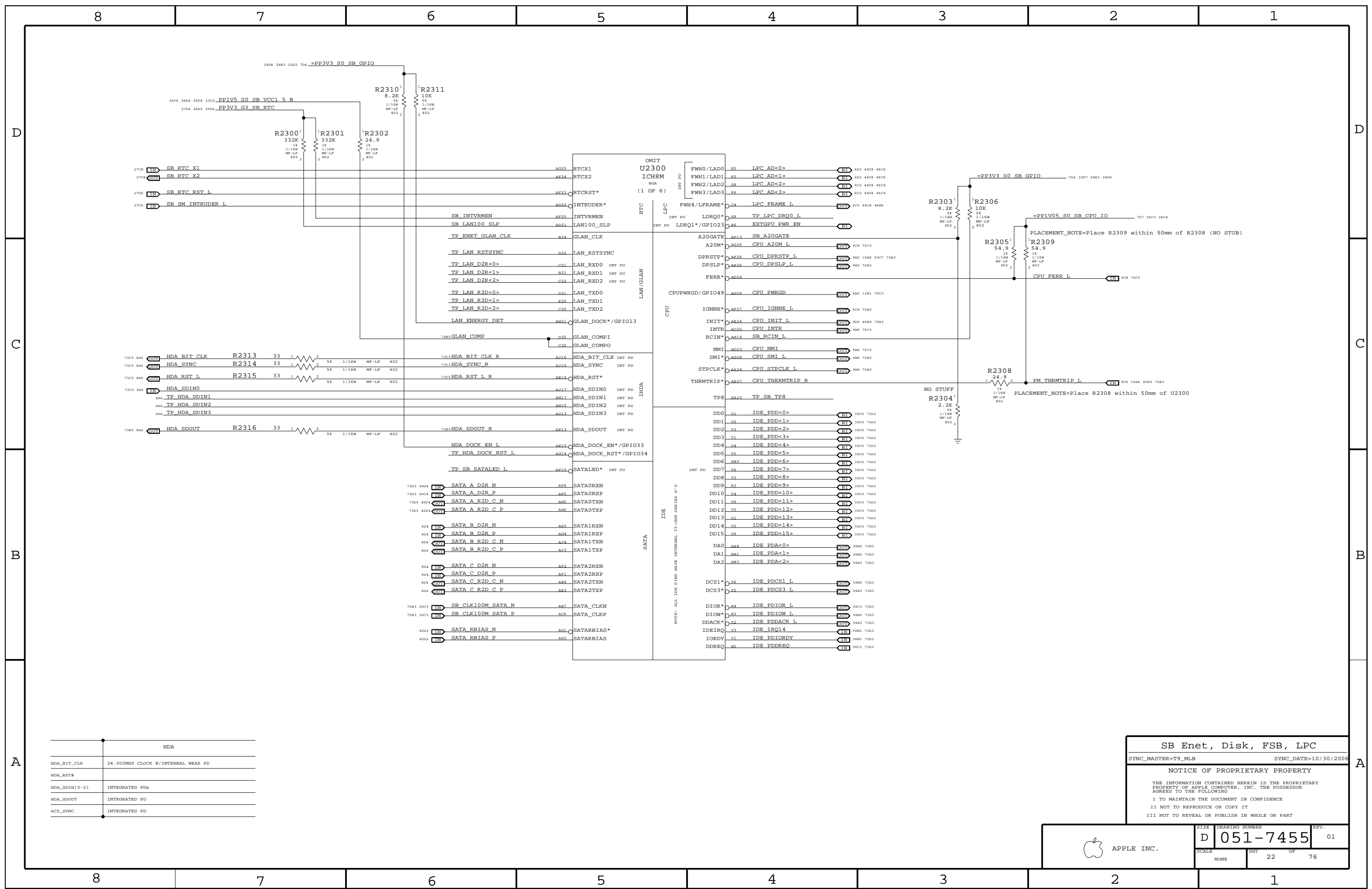
SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

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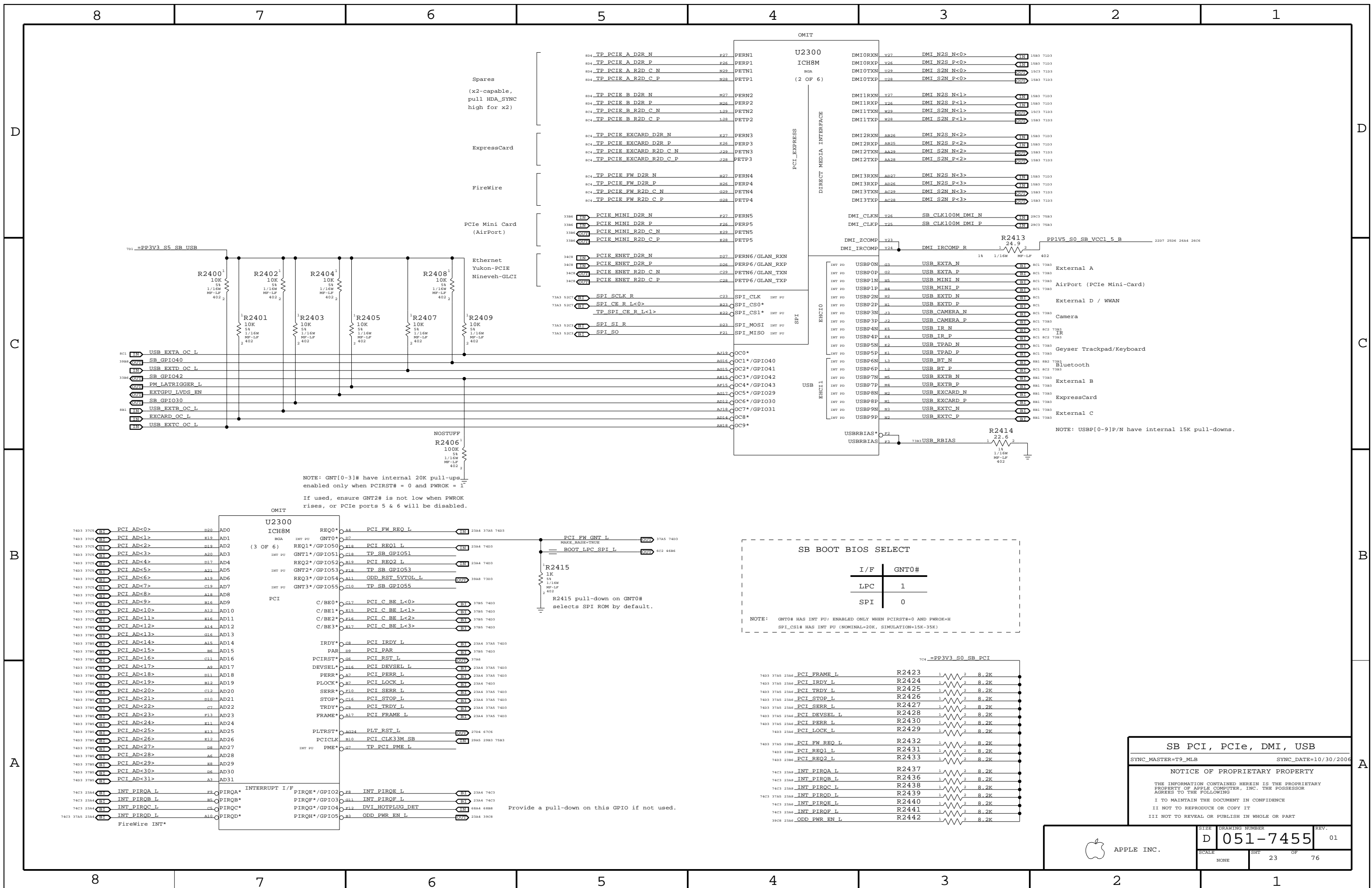
SIZE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
SCALE	SHT	OF
	21	76



HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDS
HDA_SDOUT	INTEGRATED PD
AC2_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006
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APPLE INC.	SIZE DRAWING NUMBER D 051-7455	REV. 01
	SCALE NONE	SHEET 22 OF 76



Spares
(x2-capable,
pull HDA_SYNC
high for x2)

ExpressCard

FireWire

PCIe Mini Card
(AirPort)

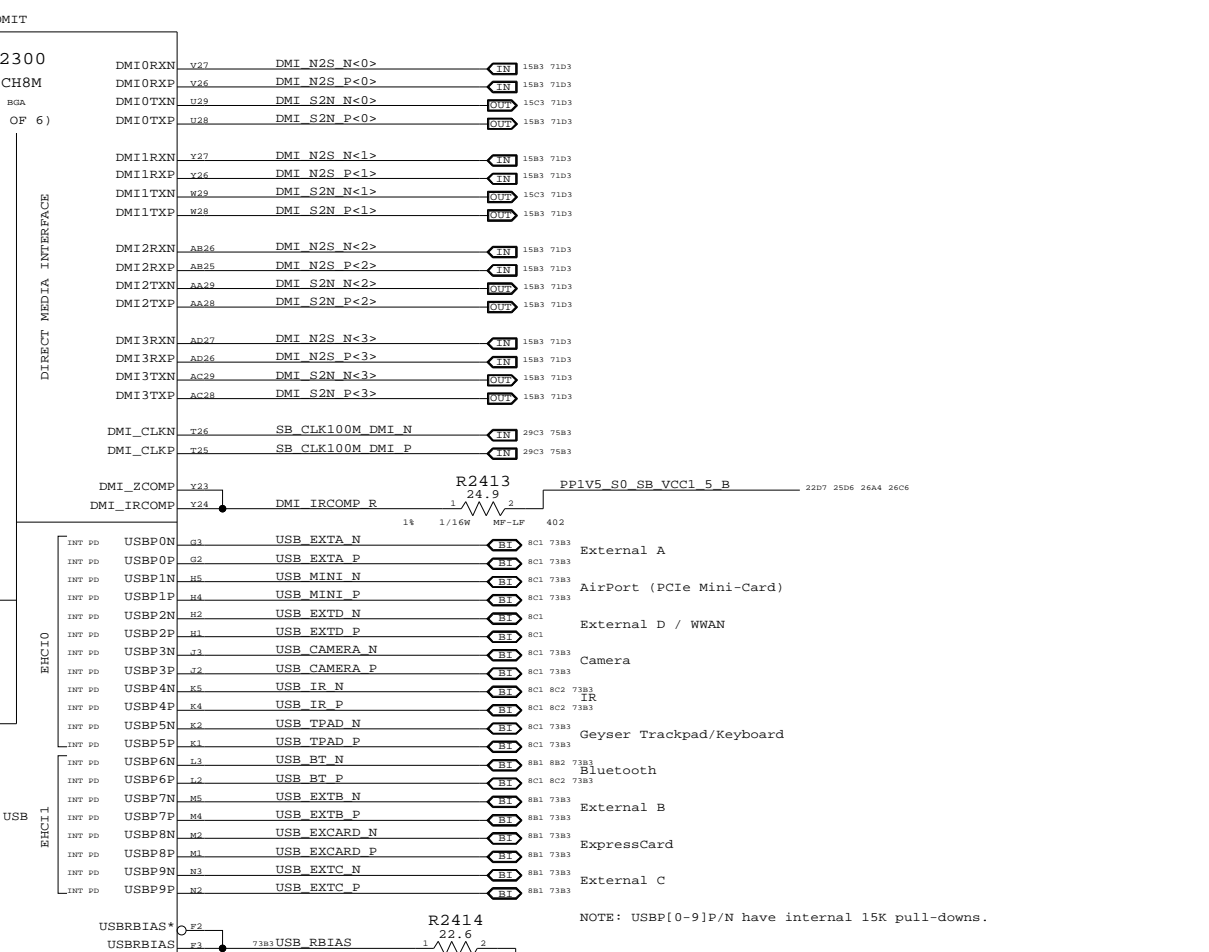
Ethernet
Yukon-PCI
Nineveh-GLCI

USB EXTA OC L
SB GPIO40
USB EXTD OC L
SB GPIO42
PM LATRIGGER L
EXTGPU LVDS EN
SB GPIO30
USB EXTB OC L
EXCARD OC L
USB EXTC OC L

U2300 ICH8M (2 OF 6)	PERN1	DMI N2S N<0>
	PERP1	DMI N2S P<0>
	PETN1	DMI S2N N<0>
	PETP1	DMI S2N P<0>
	PERN2	DMI N2S N<1>
	PERP2	DMI N2S P<1>
	PETN2	DMI S2N N<1>
	PETP2	DMI S2N P<1>
	PERN3	DMI N2S N<2>
	PERP3	DMI N2S P<2>
	PETN3	DMI S2N N<2>
	PETP3	DMI S2N P<2>
	PERN4	DMI N2S N<3>
	PERP4	DMI N2S P<3>
	PETN4	DMI S2N N<3>
	PETP4	DMI S2N P<3>
	PERN5	SB_CLK100M DMI N
	PERP5	SB_CLK100M DMI P
	PETN5	
	PETP5	
	PERN6/GLAN_RXN	
	PERP6/GLAN_RXP	
	PETN6/GLAN_TXN	
	PETP6/GLAN_TXP	

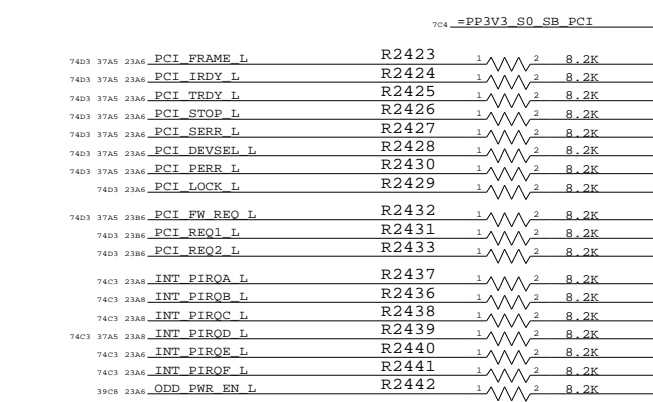
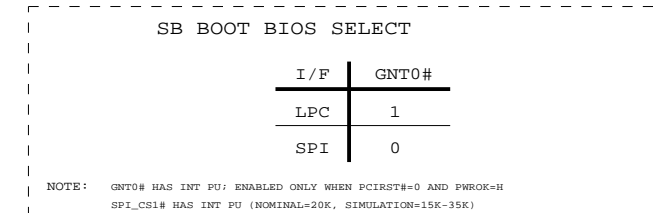
3386	PCIE MINI D2R N	F27	SPI_CLK	INT PU
3386	PCIE MINI D2R P	F26	SPI_CS0*	INT PU
3386	PCIE MINI R2D C N	E29	SPI_CS1*	INT PU
3386	PCIE MINI R2D C P	E28	SPI_MISO	INT PU
3408	PCIE ENET D2R N	D27	SPI_MOSI	INT PU
3408	PCIE ENET D2R P	D26	SPI_SO	INT PU
3408	PCIE ENET R2D C N	C29		
3408	PCIE ENET R2D C P	C28		

OC0*	OC1*/GPIO40
OC1*/GPIO40	OC2*/GPIO41
OC2*/GPIO41	OC3*/GPIO42
OC3*/GPIO42	OC4*/GPIO43
OC4*/GPIO43	OC5*/GPIO29
OC5*/GPIO29	OC6*/GPIO30
OC6*/GPIO30	OC7*/GPIO31
OC7*/GPIO31	OC8*
OC8*	OC9*



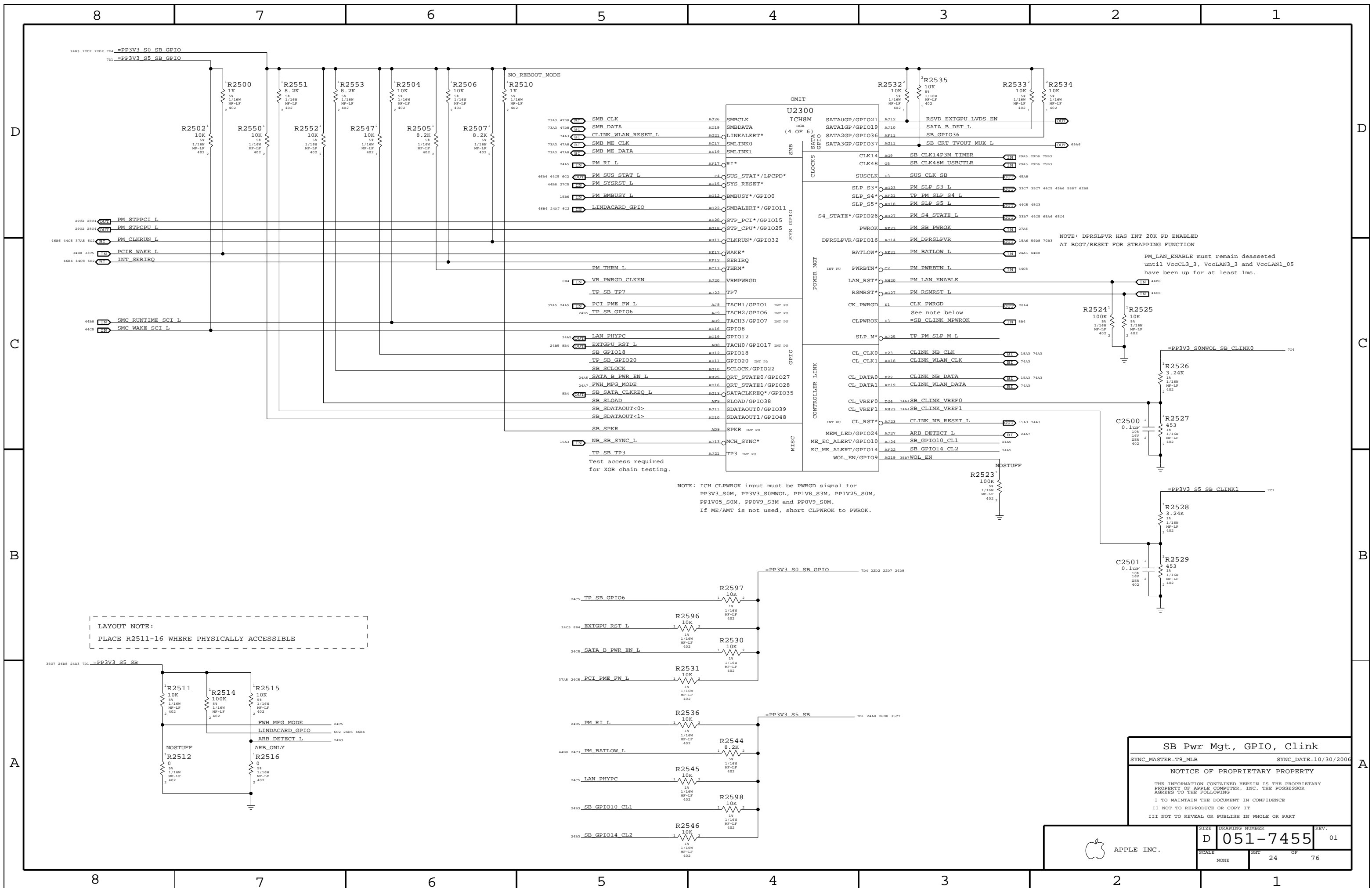
USB EXTA N	USB EXTA P	USB MINI N	USB MINI P	USB EXTD N	USB EXTD P	USB CAMERA N	USB CAMERA P	USB IR N	USB IR P	USB TPAD N	USB TPAD P	USB BT N	USB BT P	USB EXTB N	USB EXTB P	USB EXCARD N	USB EXCARD P	USB EXTC N	USB EXTC P
------------	------------	------------	------------	------------	------------	--------------	--------------	----------	----------	------------	------------	----------	----------	------------	------------	--------------	--------------	------------	------------

NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.



SB PCI, PCIe, DMI, USB
SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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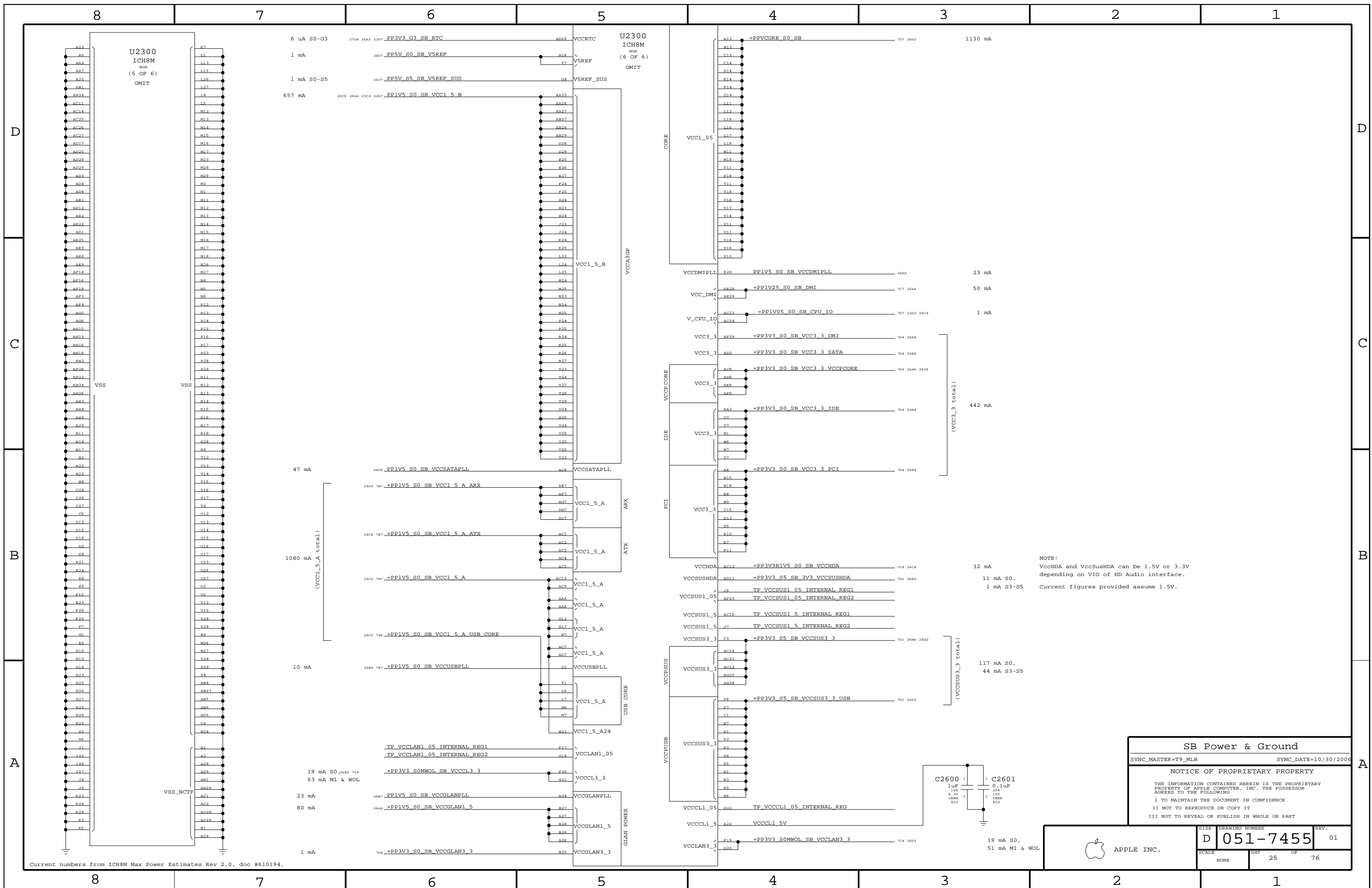
U2300 Pin	Signal Name	Function
73A3 4708	SMB_CLK	SMBCLK
73A3 4709	SMB_DATA	SMBDATA
74A3	CLINK_WLAN RESET L	LINKALERT*
73A3 47A8	SMB_MF_CLK	SMLINK0
73A3 47A9	SMB_MF_DATA	SMLINK1
24A5	PM_RI_L	RI*
46B4 44C5 6C2	PM_SUS_STAT_L	SUS_STAT*/LPCPD*
4488 27C5	PM_SYSRST_L	SYS_RESET*
15B6	PM_BMBUSY_L	BMBUSY*/GPIO0
46B4 24A7 6C2	LINDACARD_GPIO	SMBALERT*/GPIO11
	TP_SB_TP7	TP7
8B4	VR_PWRGD_CLKEN	VRMPWRGD
37A5 24A5	PCI_PME_FW_L	TACH1/GPIO1 INT PU
24B5	TP_SB_GPIO6	TACH2/GPIO6 INT PU
	LAN_PHYPC	TACH3/GPIO7 INT PU
24B5 8B4	EXTGPU_RST_L	GPI08
	SB_GPIO18	TACH0/GPIO17 INT PU
	TP_SB_GPIO20	GPI018
	SB_SCLK	GPI020 INT PU
24A5	SATA_B_PWR_EN_L	SCLK/GPIO22
24A7	FWH_MFG_MODE	QRT_STATE0/GPIO27
8B4	SB_SATA_CLKREQ_L	QRT_STATE1/GPIO28
	SB_SLOAD	SATACLKREQ*/GPIO35
	SB_SDATAOUT<0>	SLOAD/GPIO38
	SB_SDATAOUT<1>	SDATAOUT0/GPIO39
	SB_SPKR	SATAOUT1/GPIO48
15A3	NB_SB_SYNC_L	SPKR INT PU
	TP_SB_TP3	MCH_SYNC*

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_SOM, PP3V3_SOMWOL, PP1V8_S3M, PP1V25_SOM, PP1V05_SOM, PPOV9_S3M and PPOV9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

LAYOUT NOTE:
PLACE R2511-16 WHERE PHYSICALLY ACCESSIBLE

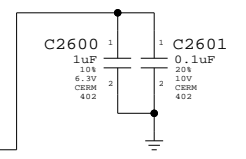
SB Pwr Mgt, GPIO, Clink
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006
NOTICE OF PROPRIETARY PROPERTY
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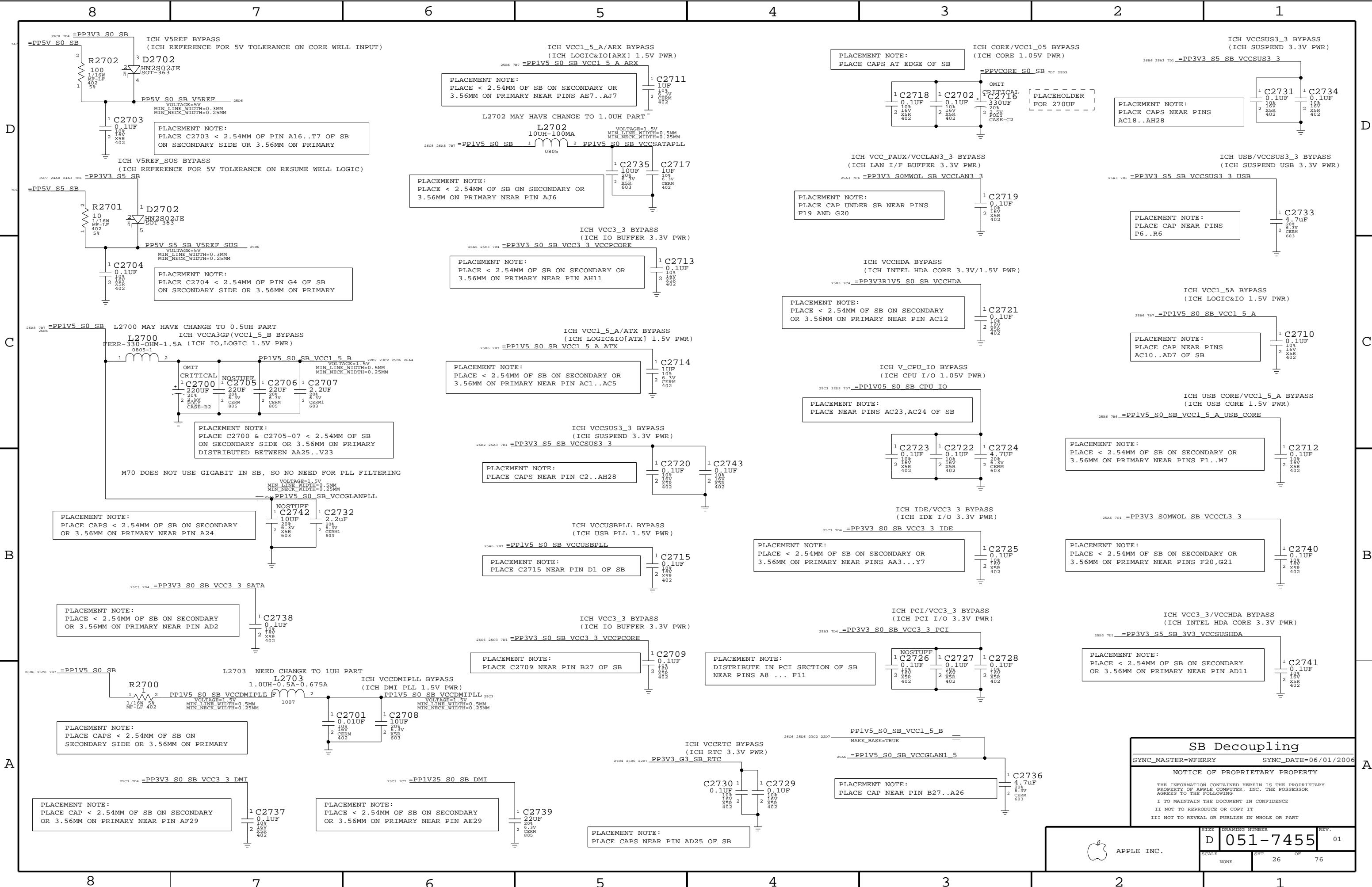
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		24	76



Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

NOTE:
 VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
 Current figures provided assume 1.5V.





SB Decoupling

SYNC_MASTER=WERRY SYNC_DATE=06/01/2006

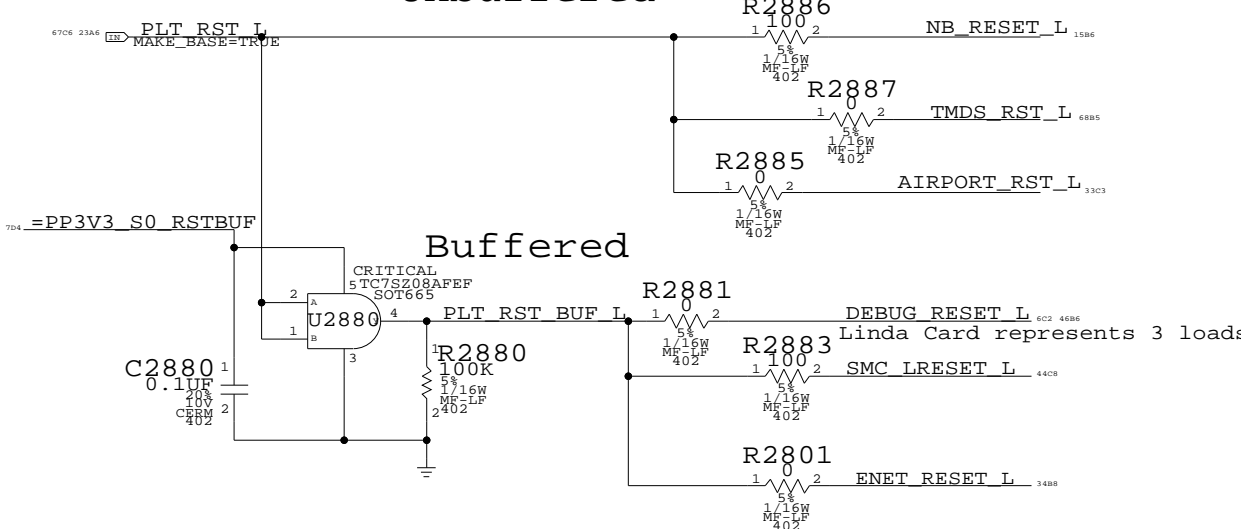
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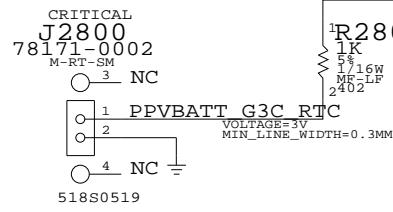
Platform Reset Connections

Unbuffered

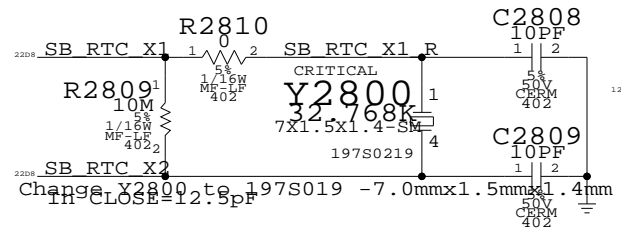


Buffered

RTC Battery Connector



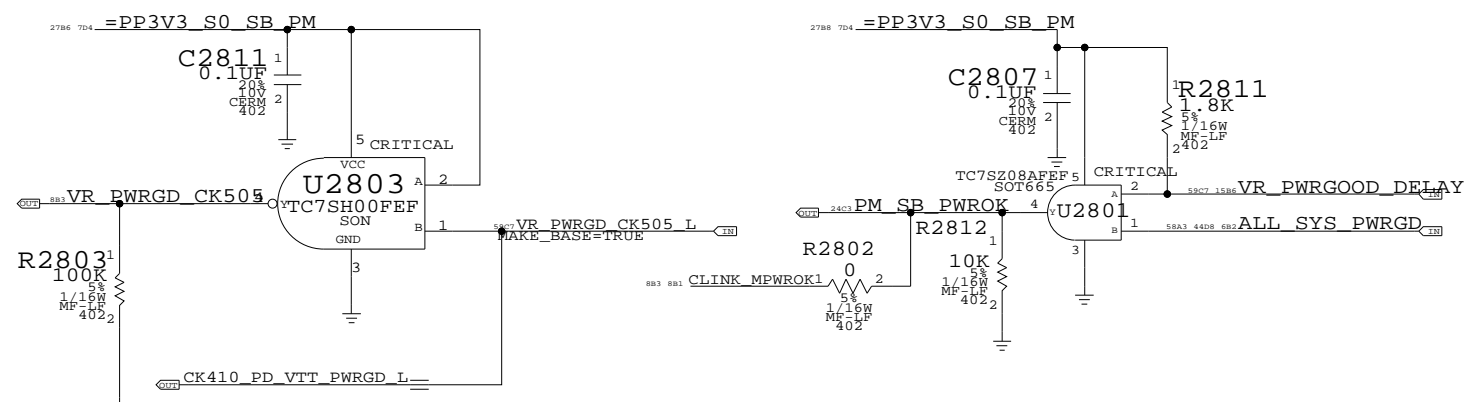
SB RTC Crystal Circuit



This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

CPU VCORE PSI



Pulled a new APN for U2803(0.6mm max 2-input NAND gate-APN:311S0304 It may take a few days before this is done through This will allow us to sequence this part under wireless card

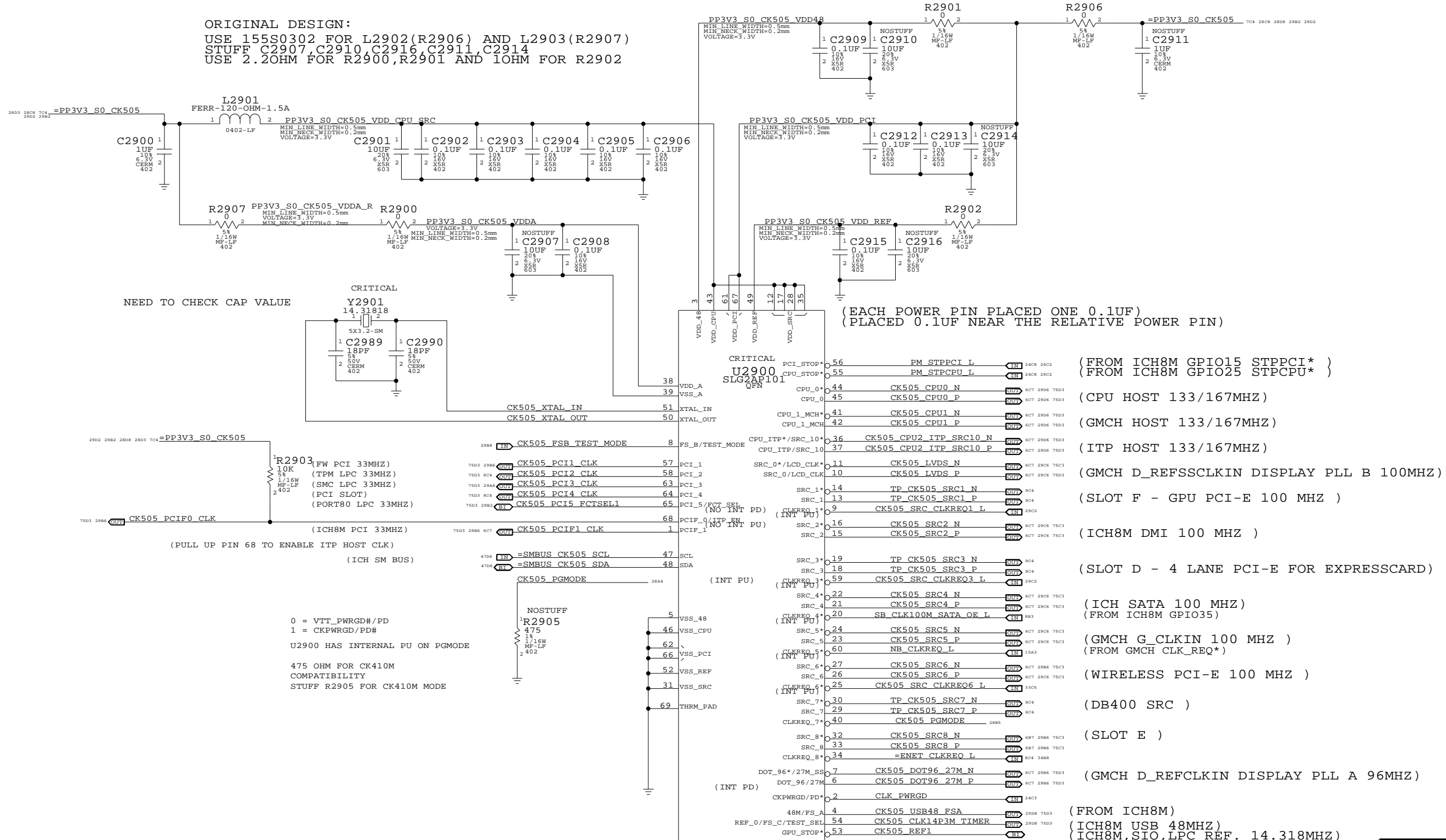
Initial resistor values are based on CRB, but may change after characterization.

SB Misc		
SYNC_MASTER=NB	SYNC_DATE=07/26/2005	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-7455	01
SCALE		SHT	OF
NONE		27	76

SELIGO RECOMMEND TO REMOVE L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

ORIGINAL DESIGN:
USE 155S0302 FOR L2902(R2906) AND L2903(R2907)
STUFF C2907,C2910,C2916,C2911,C2914
USE 2.2OHM FOR R2900,R2901 AND 1OHM FOR R2902



NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)
(ICH8M PCI 33MHZ)
(ICH SM BUS)

0 = VTT_PWRGD#/PD
1 = CKPWRGD/PD#
U2900 HAS INTERNAL PU ON PGMODE
475 OHM FOR CK410M
COMPATIBILITY
STUFF R2905 FOR CK410M MODE

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

- (FROM ICH8M GPIO15 STPPCI*)
- (FROM ICH8M GPIO25 STPCPU*)
- (CPU HOST 133/167MHZ)
- (GMCH HOST 133/167MHZ)
- (ITP HOST 133/167MHZ)
- (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- (SLOT F - GPU PCI-E 100 MHZ)
- (ICH8M DMI 100 MHZ)
- (SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
- (ICH SATA 100 MHZ)
(FROM ICH8M GPIO35)
- (GMCH G_CLKIN 100 MHZ)
(FROM GMCH CLK_REQ*)
- (WIRELESS PCI-E 100 MHZ)
- (DB400 SRC)
- (SLOT E)
- (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- (FROM ICH8M)
- (ICH8M USB 48MHZ)
- (ICH8M,SIO,LPC REF. 14.318MHZ)

Clock (CK505)

SYNC_MASTER=DSIMON SYNC_DATE=06/06/2006

NOTICE OF PROPRIETARY PROPERTY

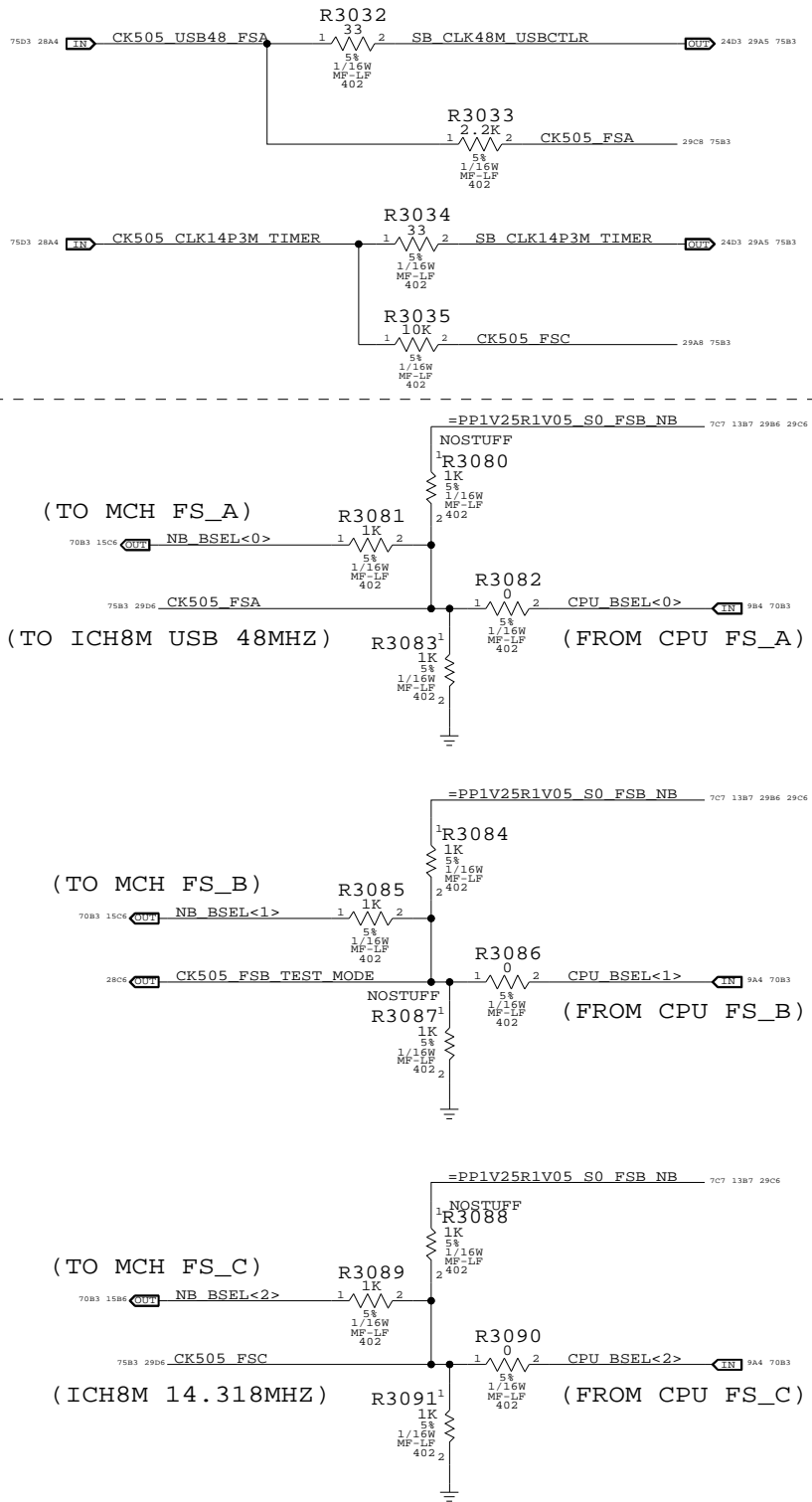
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APPLE INC.

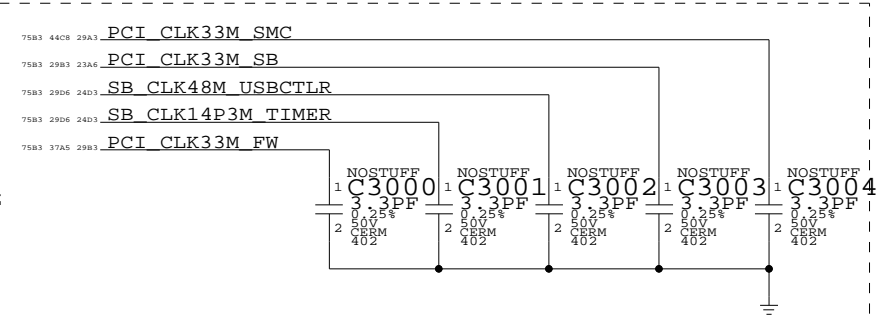
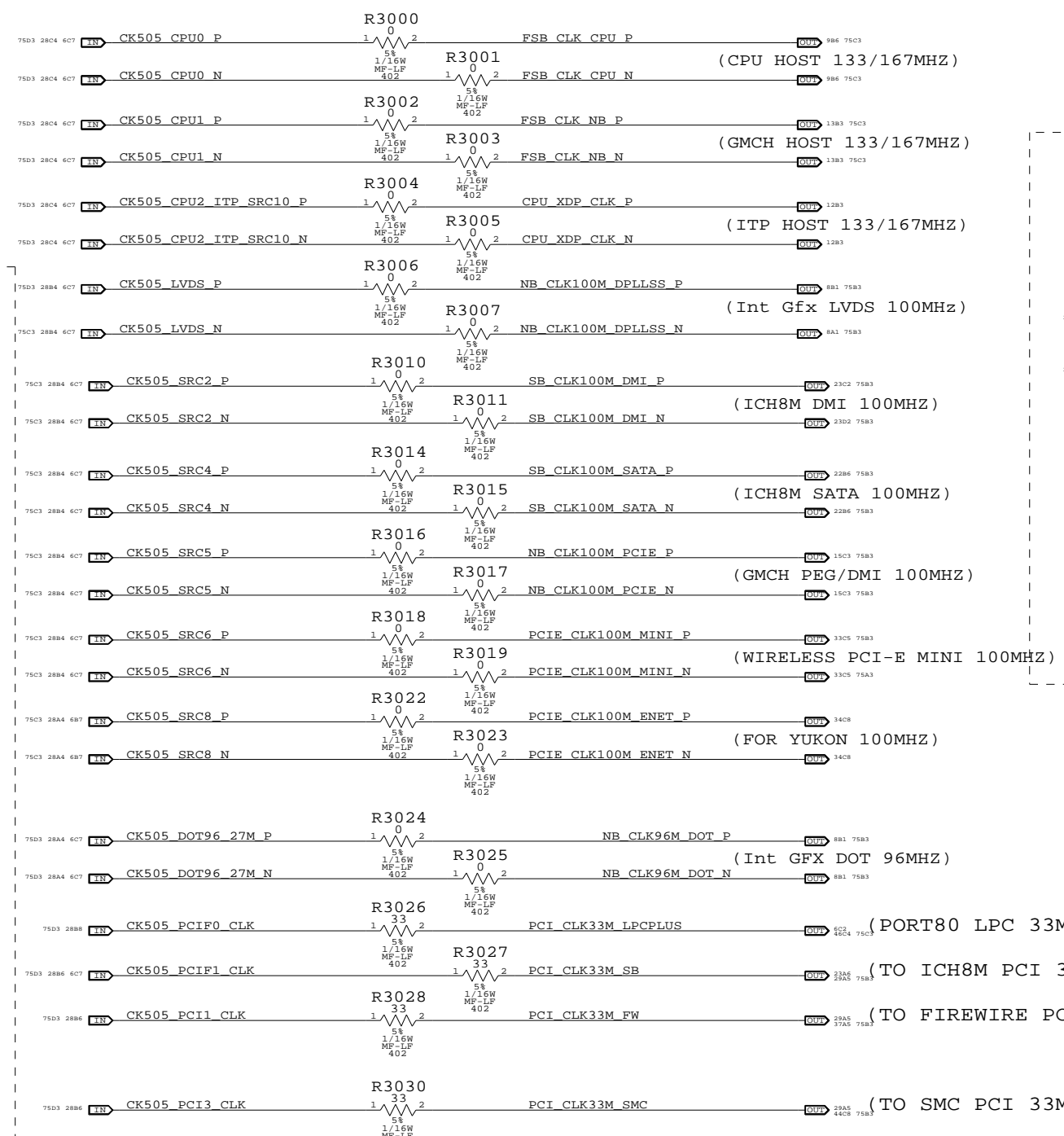
SCALE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
	SHEET	OF
	28	76

CLK Termination



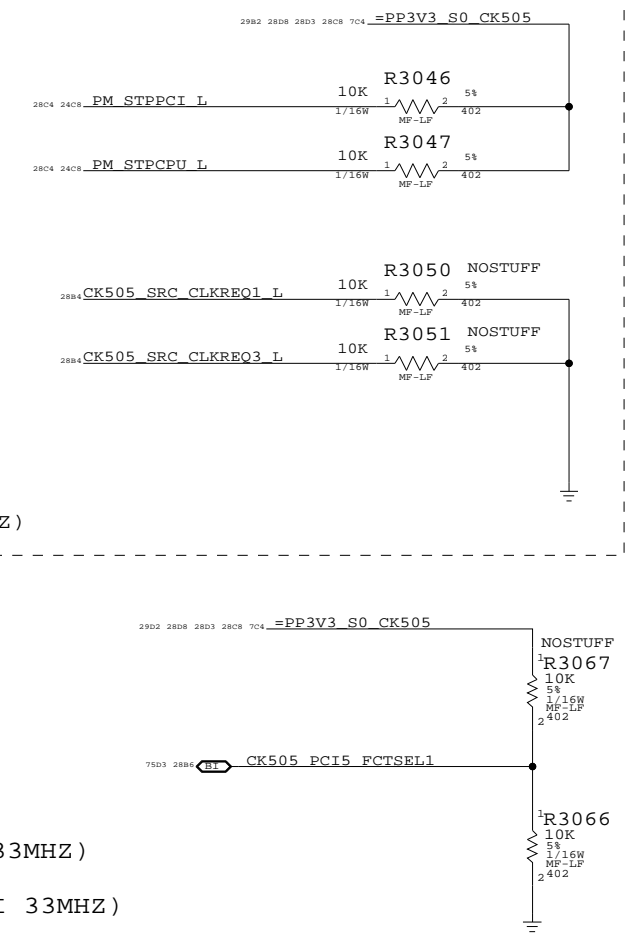
FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	1	166M
0	1	0	200M
1	1	0	400M
1	1	1	Resrvd
1	0	1	100M
1	0	0	333M

NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY
CPU speed is currently set to 200MHZ



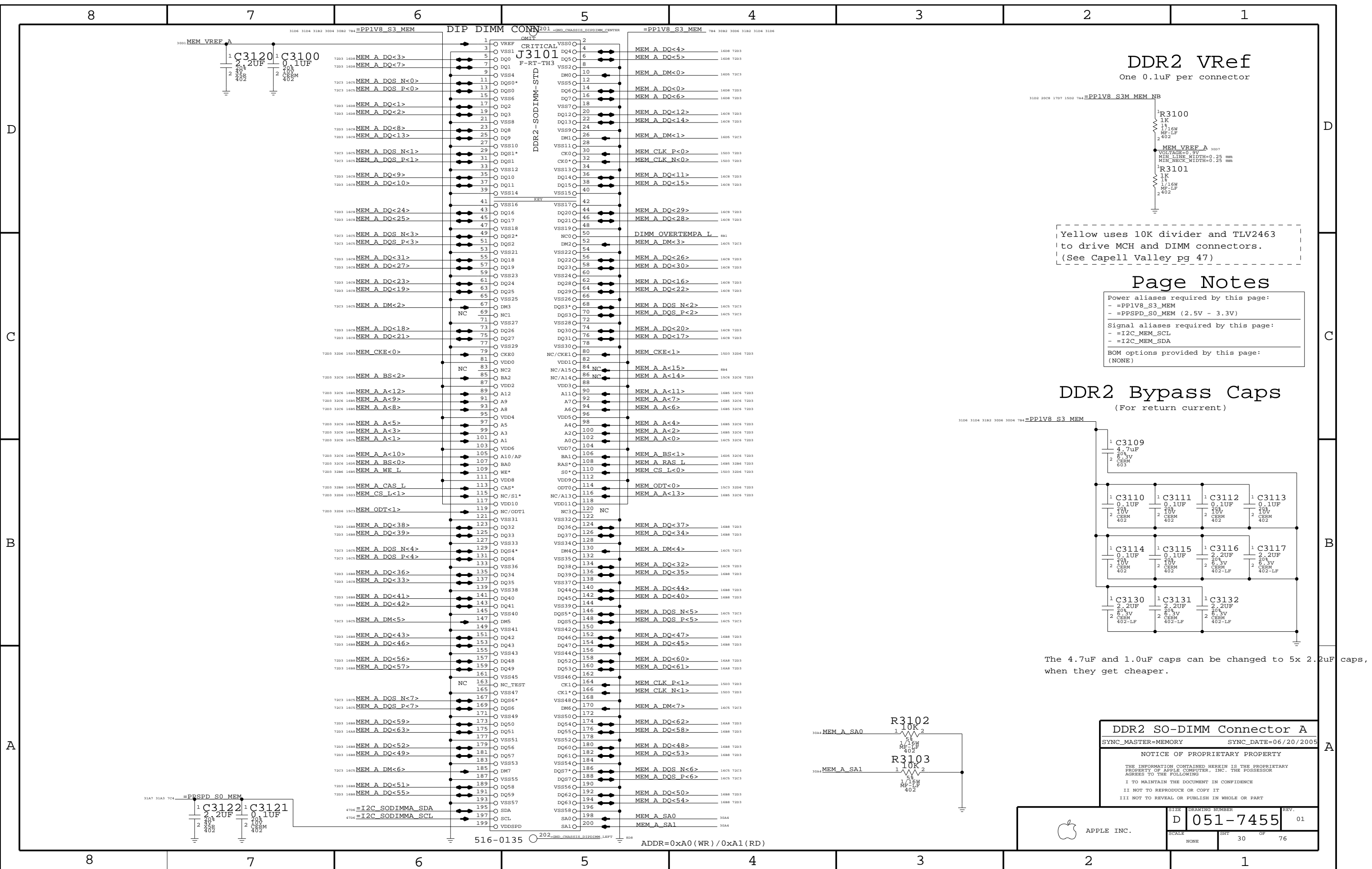
Place close to CLK Gen
For reducing noise coupling to wireless frequencies

CLKREQ Controls

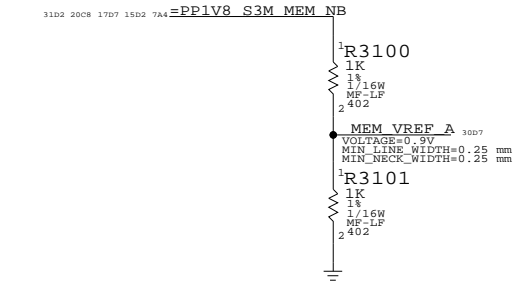


Clock Termination
 SYNC_MASTER=DSIMON-WF SYNC_DATE=06/06/2006
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APPLE INC. DRAWING NUMBER: D 051-7455 REV. 01
 SCALE: NONE SHEET: 29 OF 76



DDR2 VRef
One 0.1uF per connector

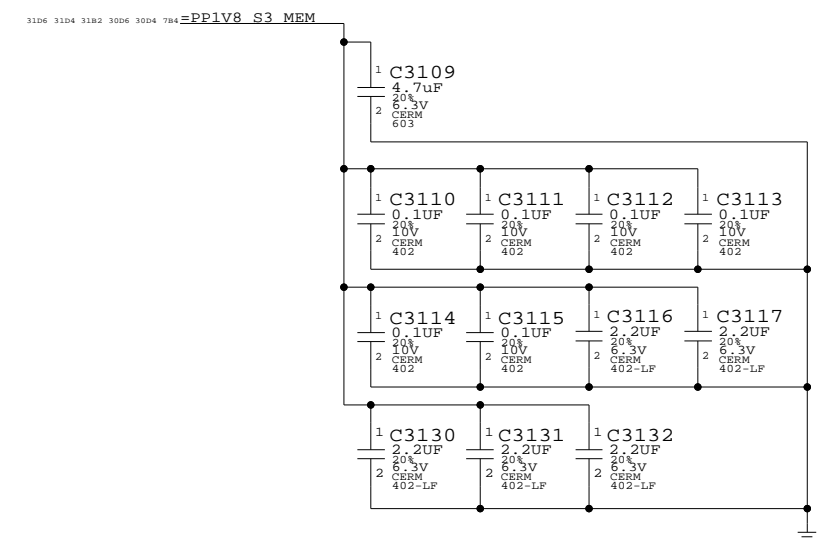


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

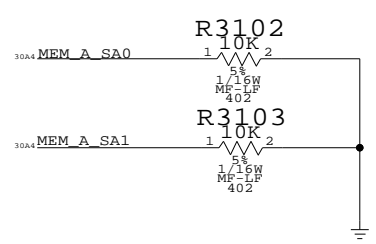
Page Notes

- Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA
- BOM options provided by this page: (NONE)

DDR2 Bypass Caps
(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



DDR2 SO-DIMM Connector A
 SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	SHT	OF	REV.
NONE	30	76	

ADDR=0xA0 (WR) / 0xA1 (RD)

8

7

6

5

4

3

2

1

D

D

C

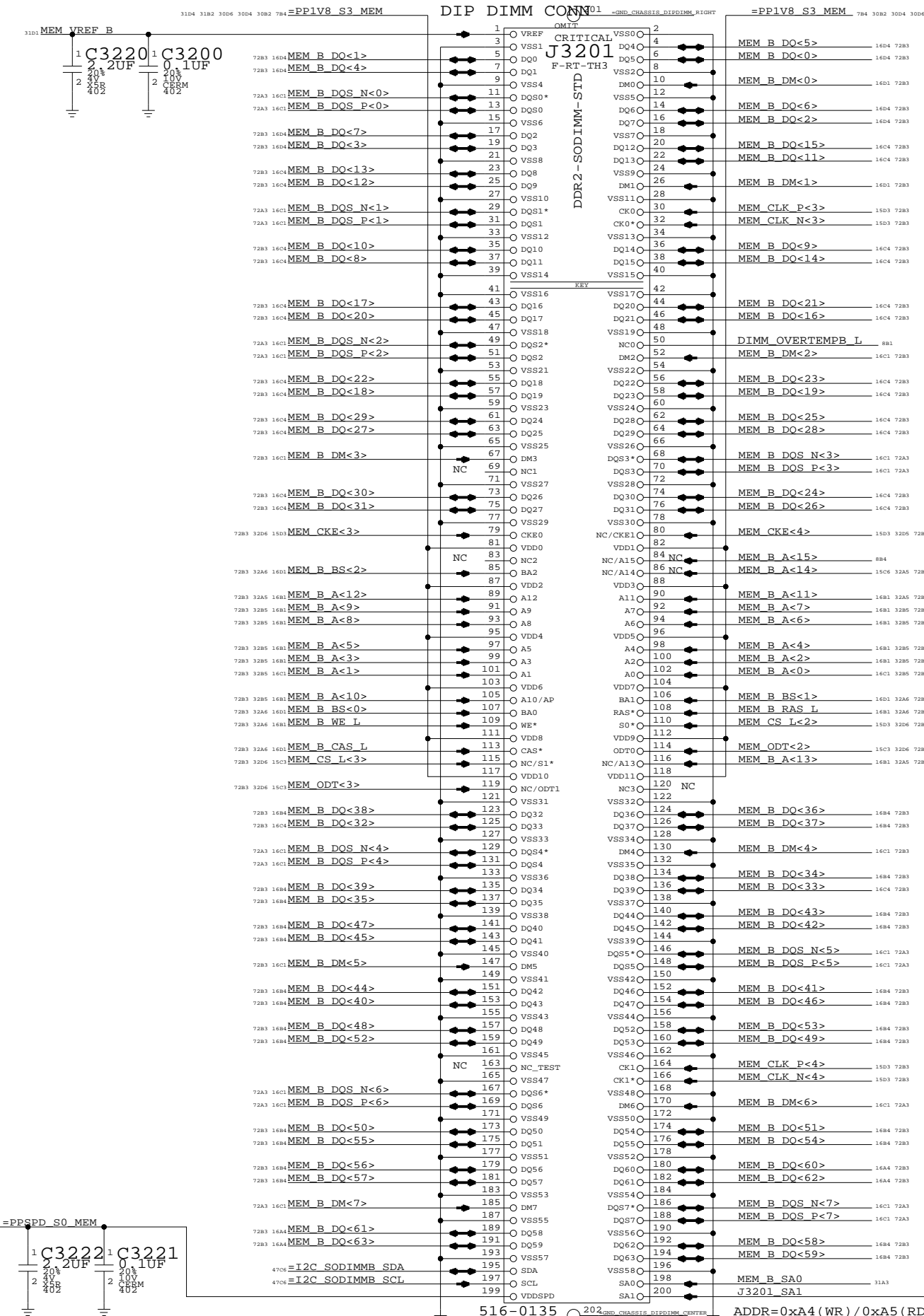
C

B

B

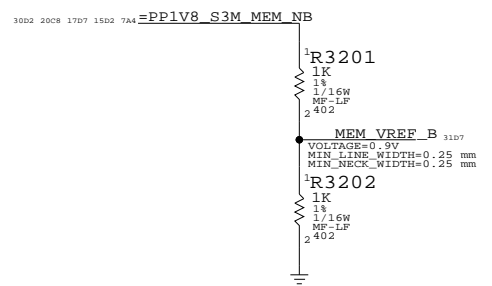
A

A



DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector

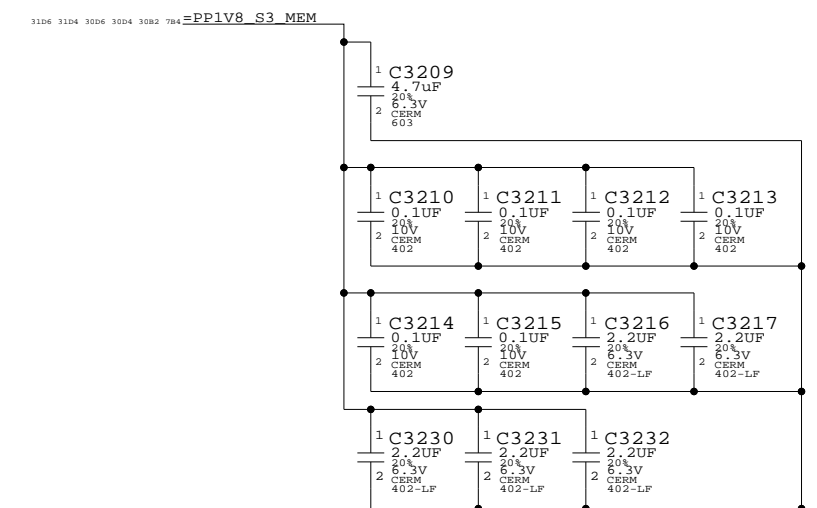


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

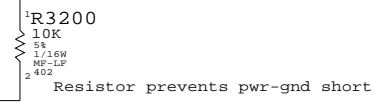
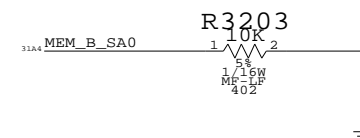
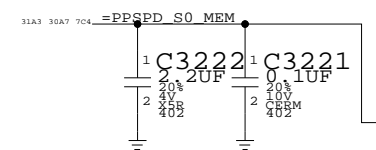
Page Notes

- Power aliases required by this page:
- =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
- =I2C_MEM_SCL
 - =I2C_MEM_SDA
- BOM options provided by this page:
- (NONE)
- NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



DDR2 SO-DIMM Connector B			
SYNC_MASTER=MEMORY		SYNC_DATE=06/20/2005	
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 APPLE INC.	SIZE: D DRAWING NUMBER: 051-7455 SCALE: NONE	REV. 01 SHT 31 OF 76	

8

7

6

5

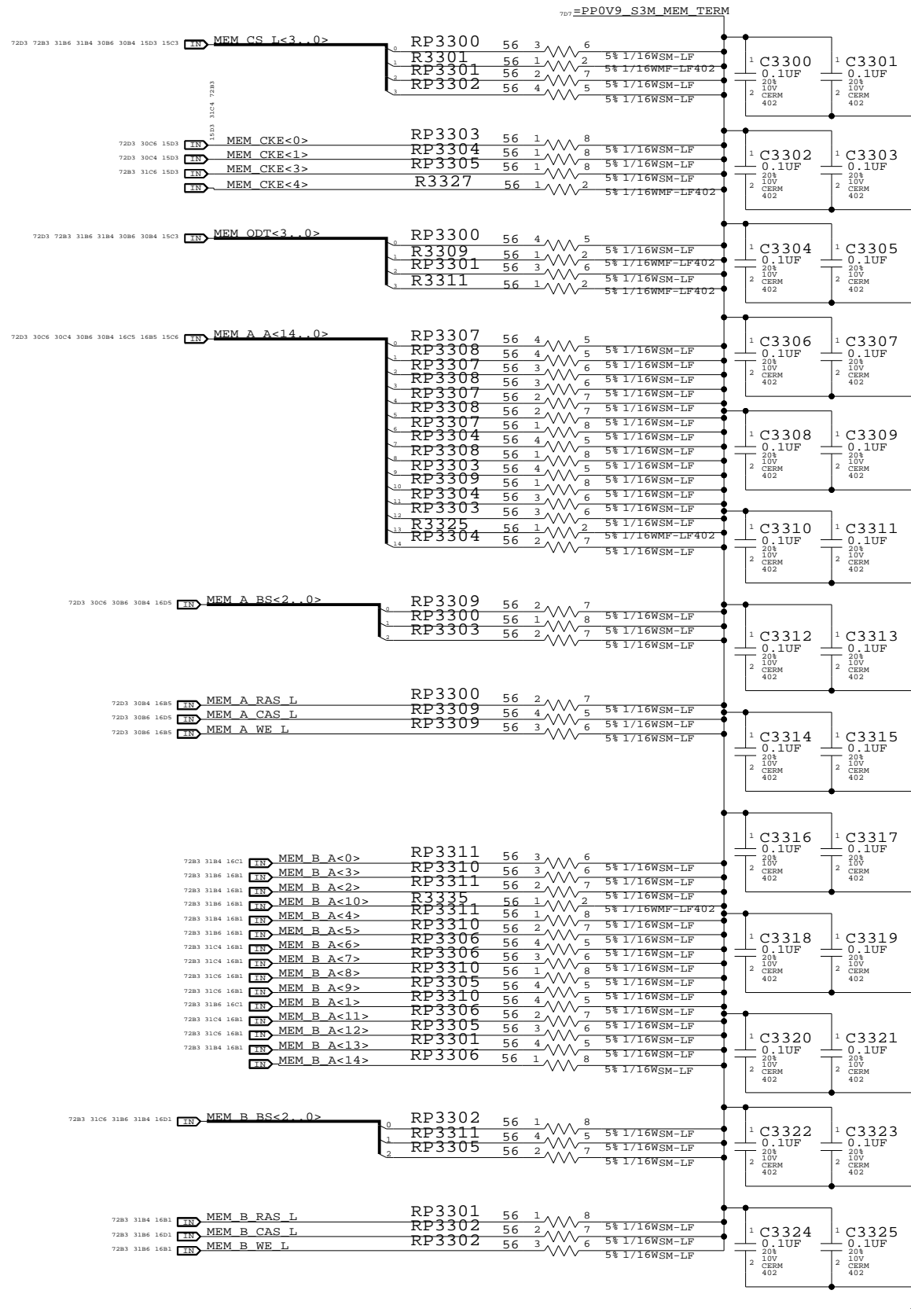
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

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I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

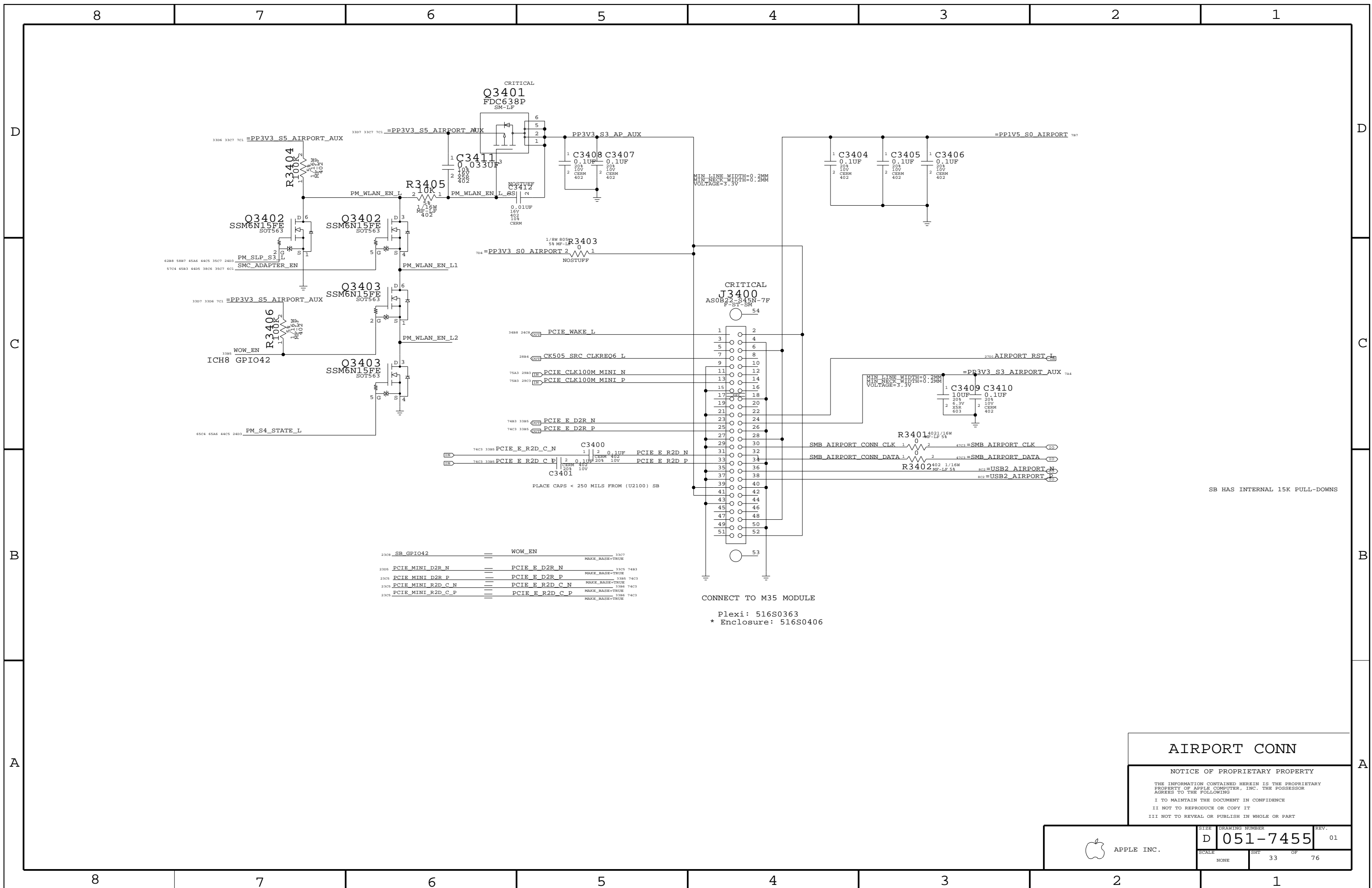
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	32	76



AIRPORT CONN

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	33	76

Page Notes

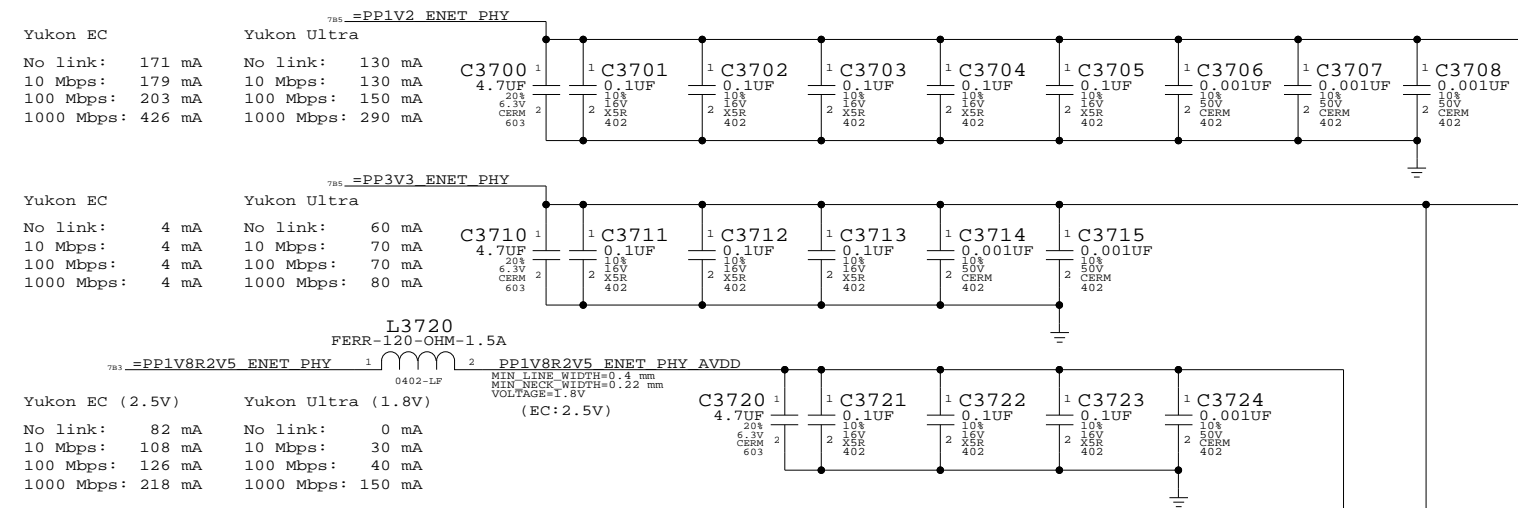
Power aliases required by this page:
 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY

Signal aliases required by this page:
 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBL

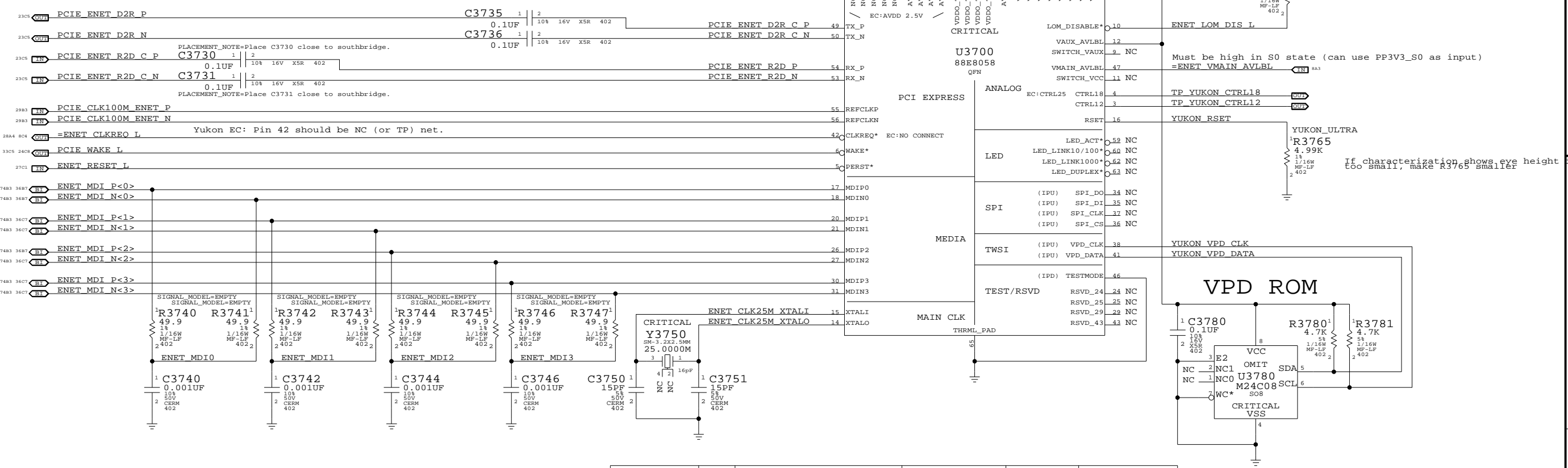
BOM options provided by this page:
 YUKON_EC - Selects Yukon EC RSET value.
 YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: Yukon IC and EEPROM are OMITTED on this page. Proper part numbers must be called out elsewhere.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



8A4 =YUKON_EC_PP2V5_ENET
 Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:
 - Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
 - Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY
 - Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
 - Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)
 SYNC_MASTER=USB SYNC_DATE=10/07/2006

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APPLE INC.

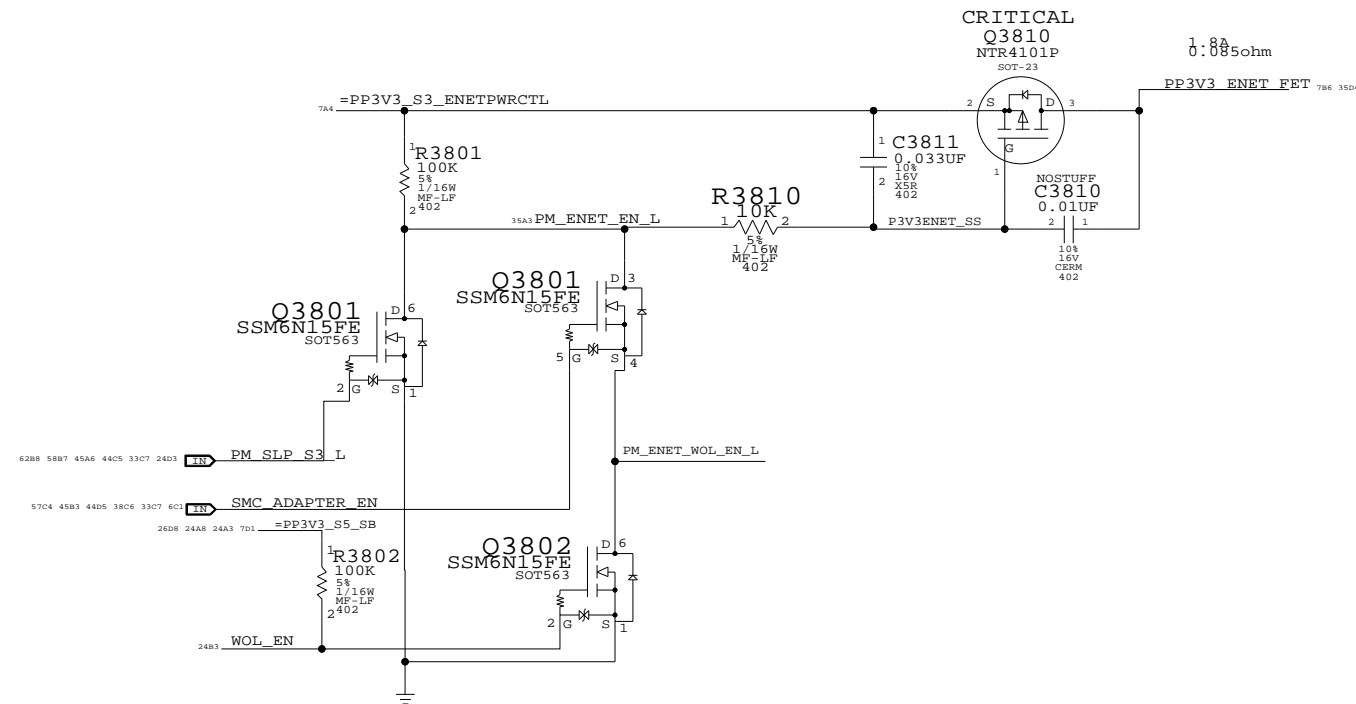
SIZE DRAWING NUMBER REV. 01
D 051-7455

SCALE NONE SHEET 34 OF 76

ENET Enable Generation

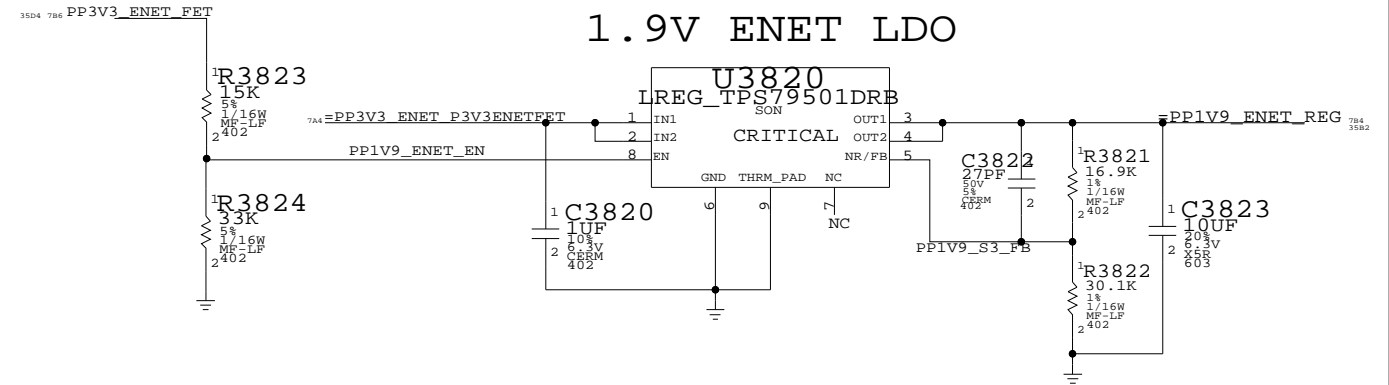
"ENET" = "S0" || AC

3.3V ENET FET



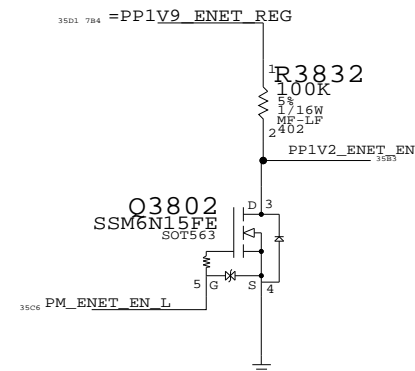
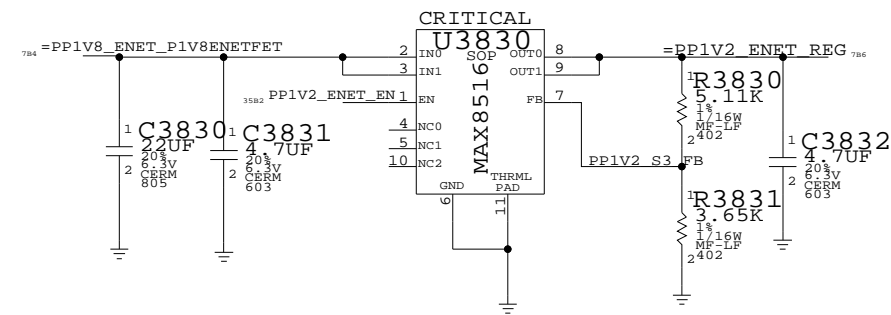
Name	PM_SLP_S3_L	SMC_ADAPTER_EN	PM_ENET_EN_L	PM_ENET_EN	Yukon Power
Logic	S0	AC			Powered by S3
S0 on Battery	High (3.3V)	Low (0V)	Low (0V)	High (3.3V)	Power
S3 on Battery	Low (0V)	Low (0V)	High (3.3V)	Low (0V)	Power
S0 on AC	High (3.3V)	High (3.3V)	Low (0V)	High (3.3V)	Power
S3 on AC	Low (0V)	High (3.3V)	Low (0V)	High (3.3V)	Power
S5 on anything	N/A	N/A	N/A	N/A	No Power

1.9V ENET LDO



$$V_{out} = 1.2246V * (1 + R3821 / R3822)$$

1.2V ENET LDO



Yukon Power Control

SYNC_MASTER=USB SYNC_DATE=10/07/2006

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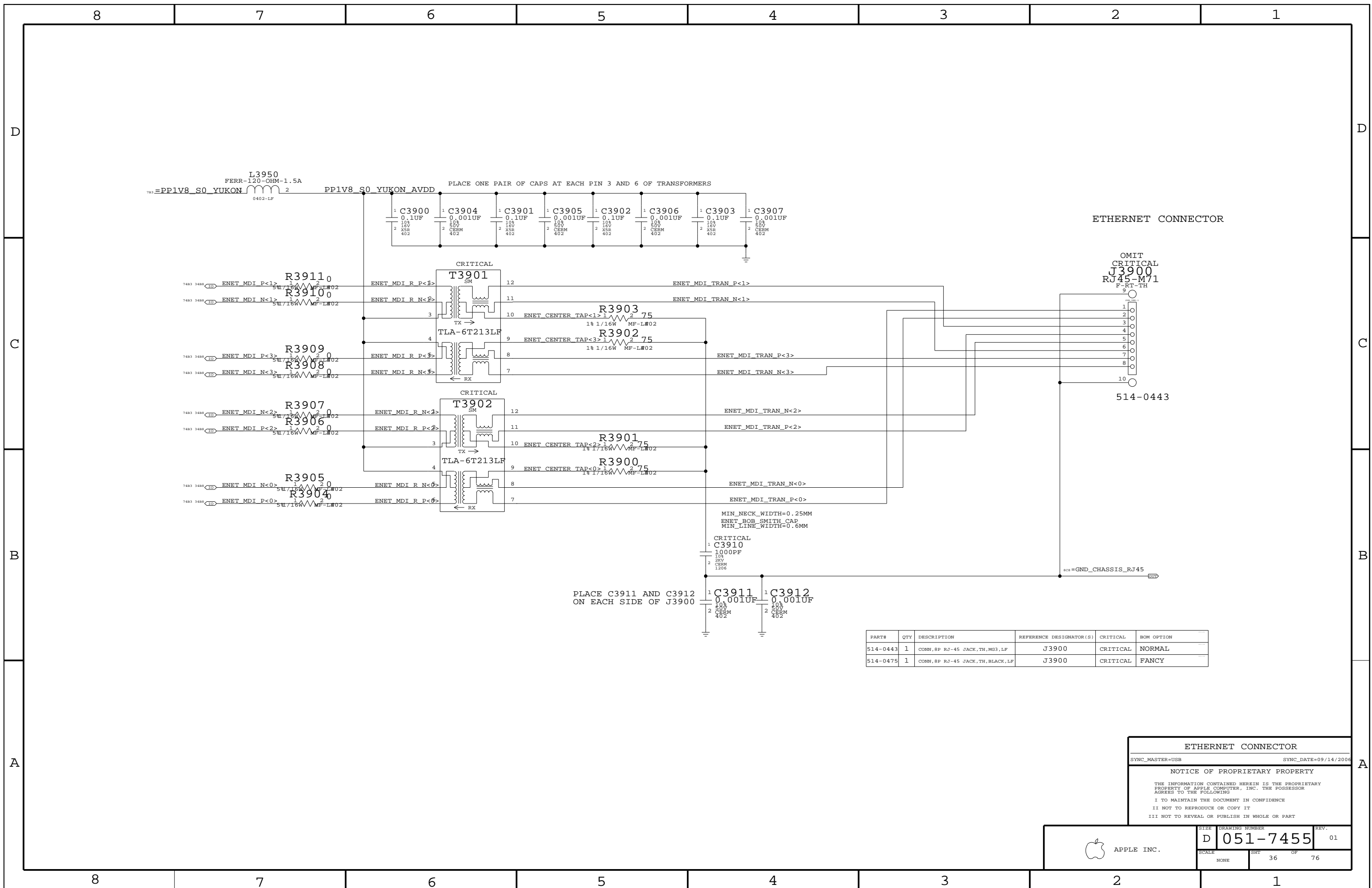


APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE SHEET OF 76



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0443	1	CONN, 8P RJ-45 JACK, TH, MG3, LF	J3900	CRITICAL	NORMAL
514-0475	1	CONN, 8P RJ-45 JACK, TH, BLACK, LF	J3900	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC_MASTER=USB SYNC_DATE=09/14/2006

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APPLE INC.

SCALE NONE

SHT 36 OF 76

SIZE D

DRAWING NUMBER 051-7455

REV. 01

PAGE NOTES

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT
PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

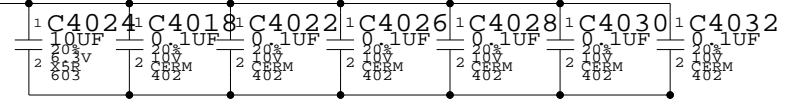
PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/21/2005 - CHANGED FROM INT_PIRQD TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED FROM FW_PC0 TO FW_PC0_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED FROM FW_A_TPA_P/N TO FW_A_TPA_P AND FW_A_TPB_P/N TO FW_A_TPB_P (PER ARCHITECTURAL DEFINITION)
6/21/2005 - ADDED 10K PULL-DOWN ON SB_A3 AND REMOVED CONNECTION TO PLT_RST_L
6/21/2005 - REMOVED CONSTRAINTS AS THEY WILL BE MANAGED ON BOARD SIDE
6/21/2005 - REMOVED CONSTRAINTS AS THEY WILL BE MANAGED ON BOARD SIDE
7/26/2005 - BEING OUT FOR CONNECTION TO BE CONNECTED ON PORT PAGE
CONNECTED PIN E10 TO GND

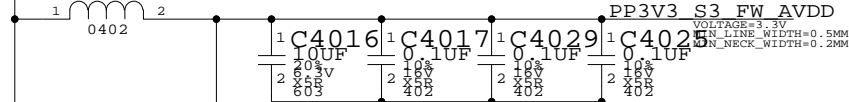
MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

744 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4024 ON VDD0



600-OHM-300MA PLACE ONE CAP PER TWO PINS STARTING WITH C4016 ON VDDA0



PP3V3_S3_FW_AVDD

VOLTAGE=3.3V
LINE_WIDTH=0.5MM
NECK_WIDTH=0.2MM

D
C
B
A

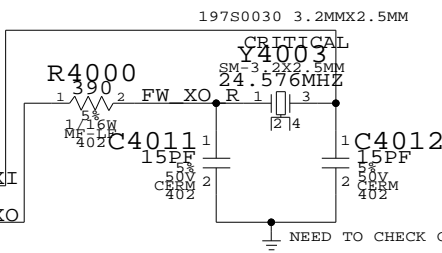
D
C
B
A

744 =PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

Table of PCI pins and their functions, including PCI_AD<0> to PCI_AD<31>, PCI_C_BE_L<0> to PCI_C_BE_L<3>, PCI_PAR, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L, PCI_DEVSEL_L, PCI_STOP_L, FW_PCI_IDSEL, PCI_FW_REQ_L, PCI_FW_GNT_L, PCI_PERR_L, PCI_SERR_L, PCI_CLK33M, PM_CLKRUN_L, PCI_RST_L, INT_PIRQD_L, PCI_PME_FW_L.

CRITICAL
U4000
FW32306
BGA



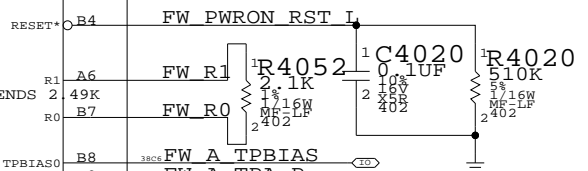
197S0030 3.2MMX2.5MM

OPTICAL

SM-3 2X2.5MM

24.576MHZ

NEED TO CHECK CRYSTAL LOAD CAPACITANCE



SPEC RECOMMENDS

FW A TPBIAS, FW A TPA P, FW A TPA N, FW A TPB P, FW A TPB N, FW B TPBIAS, FW B TPA P, FW B TPA N, FW B TPB P, FW B TPB N, FW C TPBIAS, FW C TPA P, FW C TPA N, FW C TPB P, FW C TPB N

MODE_420, MODE_A

FW_PC0

LOW = NOT BUS MANAGER, LOW = PCI OPERATION

FW TEST0, FW TEST1, FW PTEST, FW SE

MANUFACTURING TEST PINS

R4033, R4034, R4035, R4036, R4037

R4032
THIS IS FROM ICH-8
PLACE R4032 VERY CLOSE TO SB

FIREWIRE CONTROLLER
SYNC_MASTER=ENESYNC_DATE=08/30/2005

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Table with columns: SIZE, DRAWING NUMBER, REV. D, 051-7455, 01. Row 2: SCALE NONE, SHEET 37 OF 76.

Page Notes

INPUT:
 =PPBUS_FW - PORT POWER
 =PP3V3_S5_FW - DIGITAL POWER
 =GND_CHASSIS_FW_PORT0 - CHASSIS GROUND
 =FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:
 FW_TPA0_P/N,FW_TPBO_P/N,FW_TPBIAS0 - FIREWIRE DIFF PAIRS

OUTPUT:
 FW_PCO - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

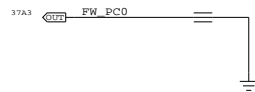
PAGE HISTORY

5/19/05 - INITIAL REVISION
 6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
 6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
 6/26/05 - CONNECTED FW_PCO FOR SINGLE PORT
 6/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
 7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
 7/26/05 - SWITCHED TO 514-014 FOR PRE-PROD CONNECTOR
 7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
 7/26/05 - CHANGED FL4590 TO 1.1A VERSION
 7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
 7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

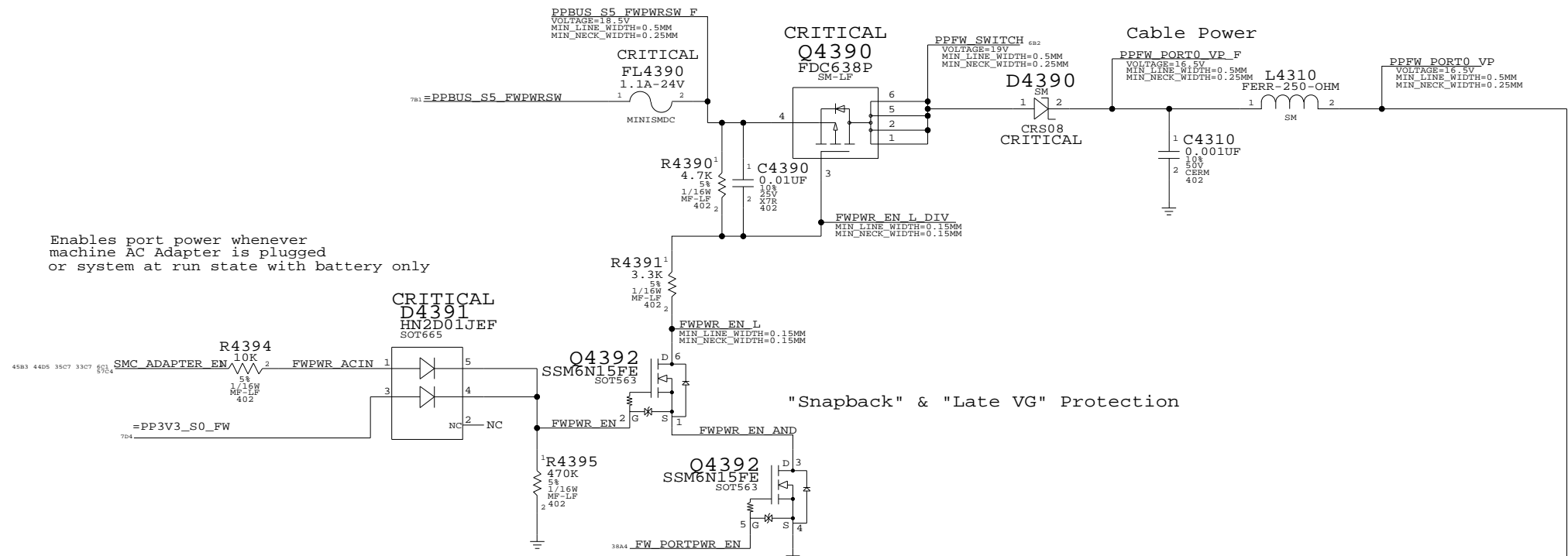
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

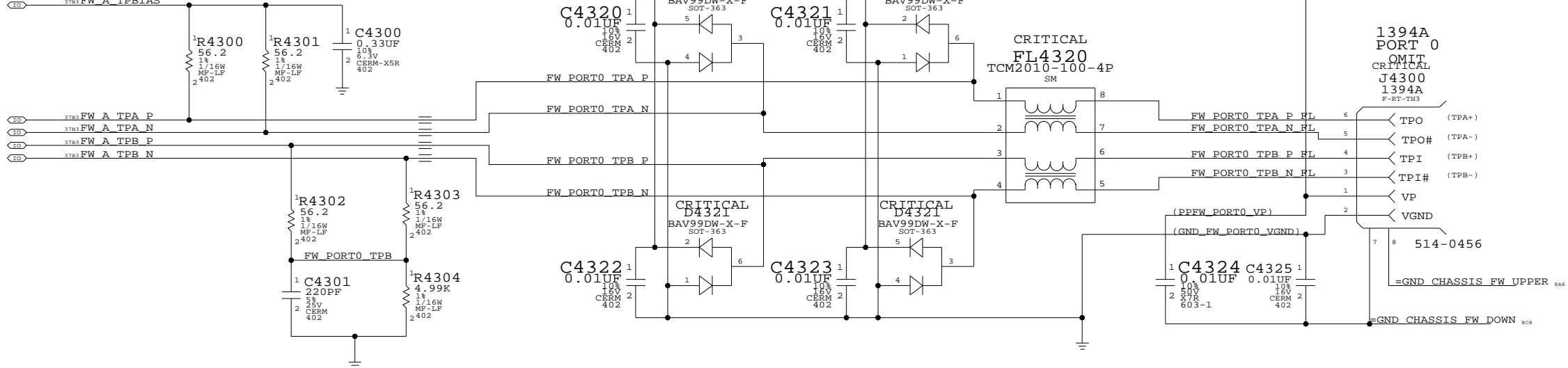
0 FOR SINGLE PORT
 1 FOR DUAL PORT



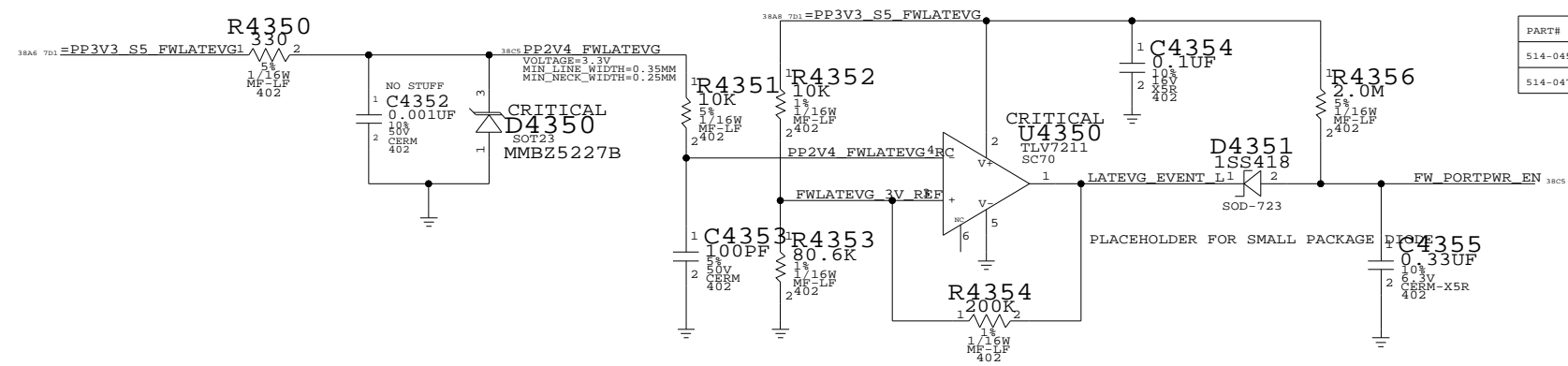
Enables port power whenever machine AC Adapter is plugged or system at run state with battery only



[LATE VG NOTES]
 CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP



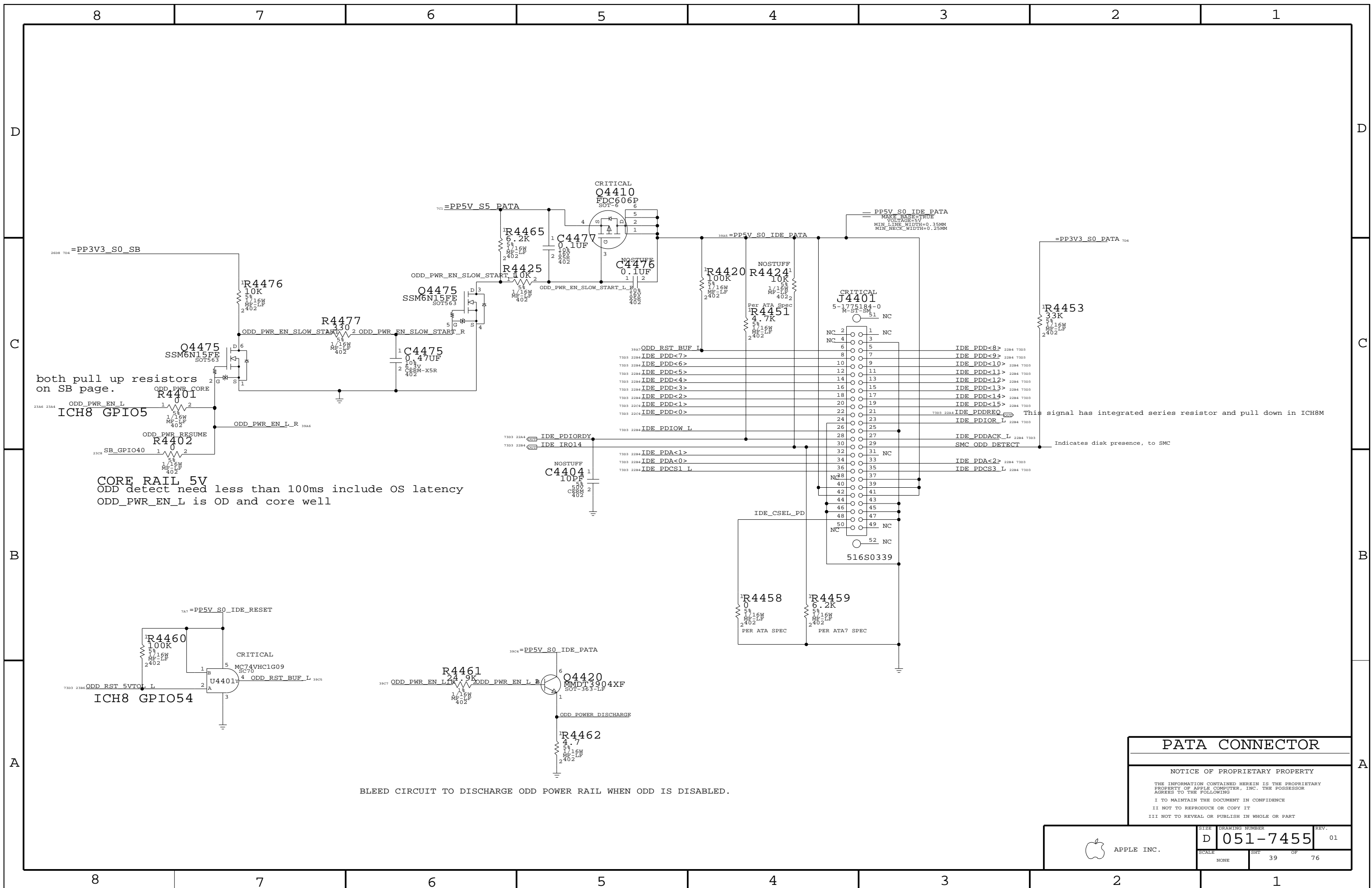
LATE-VG DETECTION CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0456	1	CONN, 6P 1394A RCPT, MIDPLANE, IN3, LP	J4300	CRITICAL	NORMAL
514-0476	1	CONN, 6P 1394A RCPT, MIDPLANE, BLACK, LP	J4300	CRITICAL	FANCY

FIREWIRE PORT
 SYNC_MASTER=GPU SYNC_DATE=07/17/2006
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APPLE INC. DRAWING NUMBER: D 051-7455 REV. 01
 SCALE: NONE SHEET: 38 OF 76



both pull up resistors on SB page.

CORE RAIL 5V
 ODD detect need less than 100ms include OS latency
 ODD_PWR_EN_L is OD and core well

This signal has integrated series resistor and pull down in ICH8M

Indicates disk presence, to SMC

BLEED CIRCUIT TO DISCHARGE ODD POWER RAIL WHEN ODD IS DISABLED.

PATA CONNECTOR

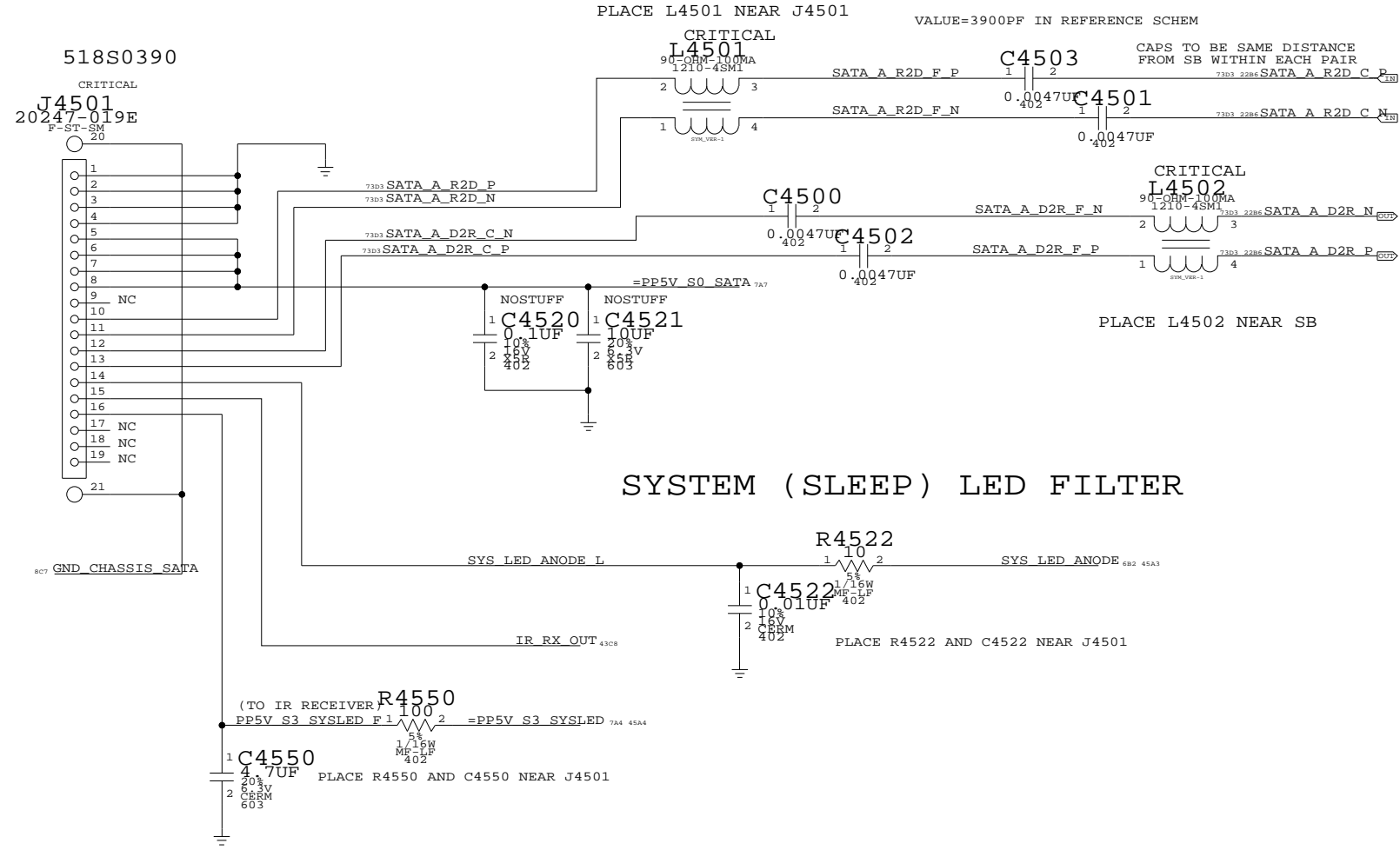
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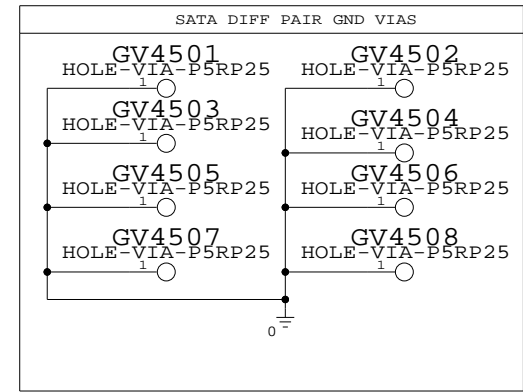
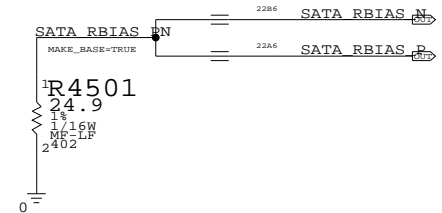
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APPLE INC.	SIZE: DRAWING NUMBER: D 051-7455	REV: 01
	SCALE: NONE	SHEET: 39 OF 76

SATA CONNECTOR



PLACE NEAR ICH8 PIN



SATA CONNECTOR

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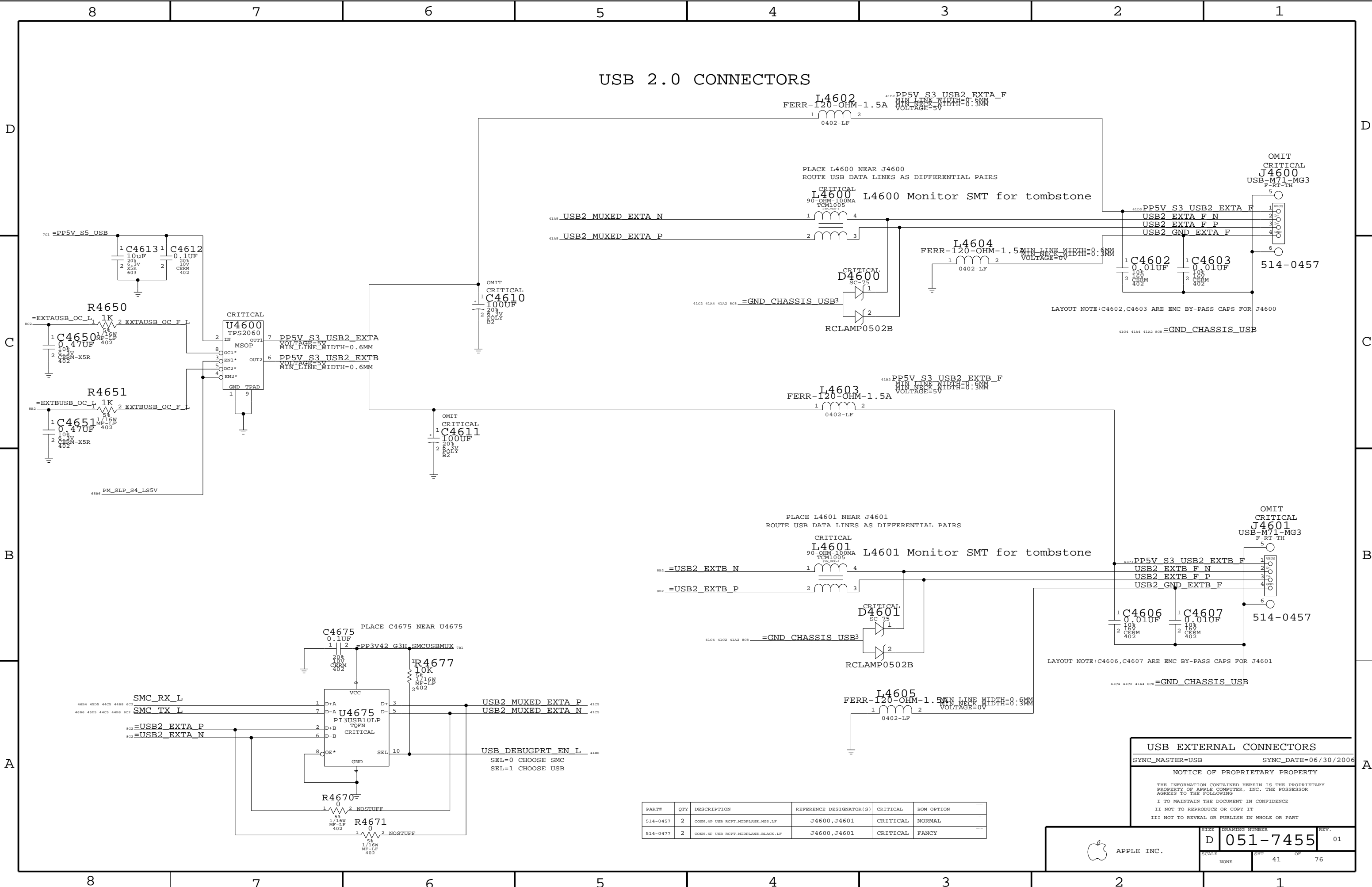
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7455	REV.: 01
	SCALE: NONE	SHEET: 40	OF: 76

USB 2.0 CONNECTORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0457	2	CONN, 4P USB RCPT, MIDPLANE, MG3, LF	J4600, J4601	CRITICAL	NORMAL
514-0477	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J4600, J4601	CRITICAL	FANCY

USB EXTERNAL CONNECTORS

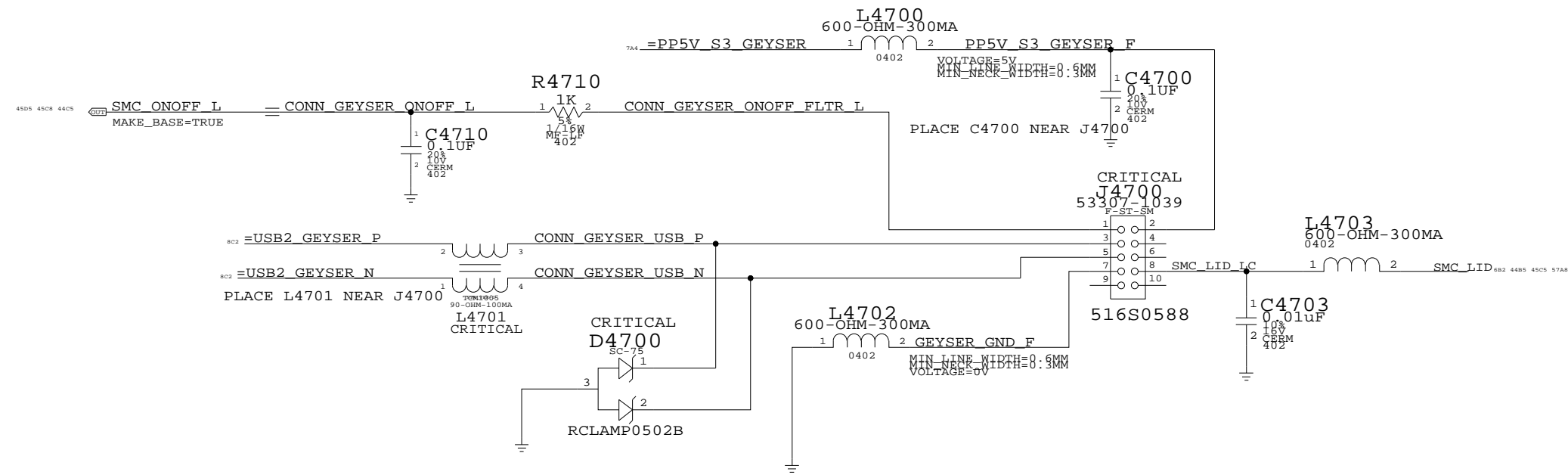
SYNC_MASTER=USB SYNC_DATE=06/30/2006

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APPLE INC.	SCALE	DRAWING NUMBER		REV.
	NONE	D	051-7455	01
		SHT	OF	
		41	76	

GEYSER AND DIMMO REMOTE TEMP SENSORS

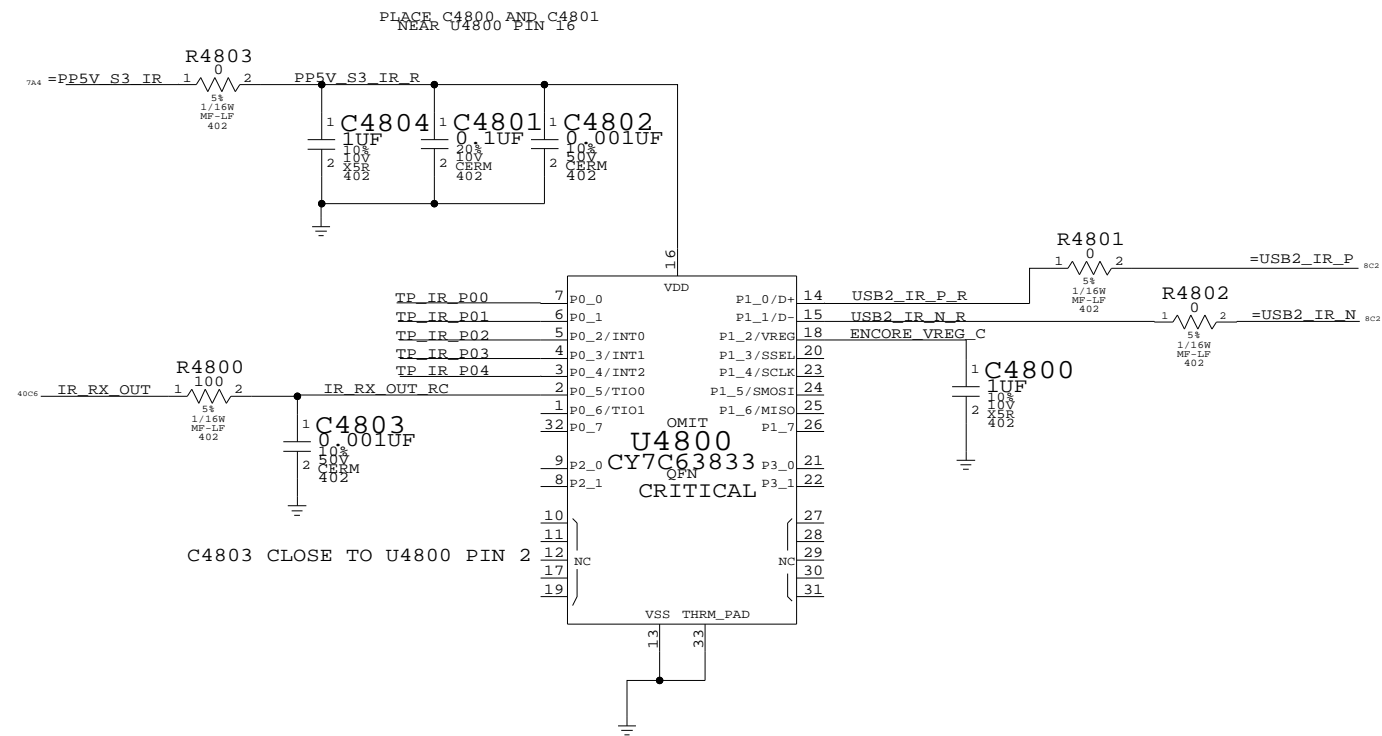


CONNECTOR MISC
 SYNC_MASTER=USB SYNC_DATE=06/29/2006

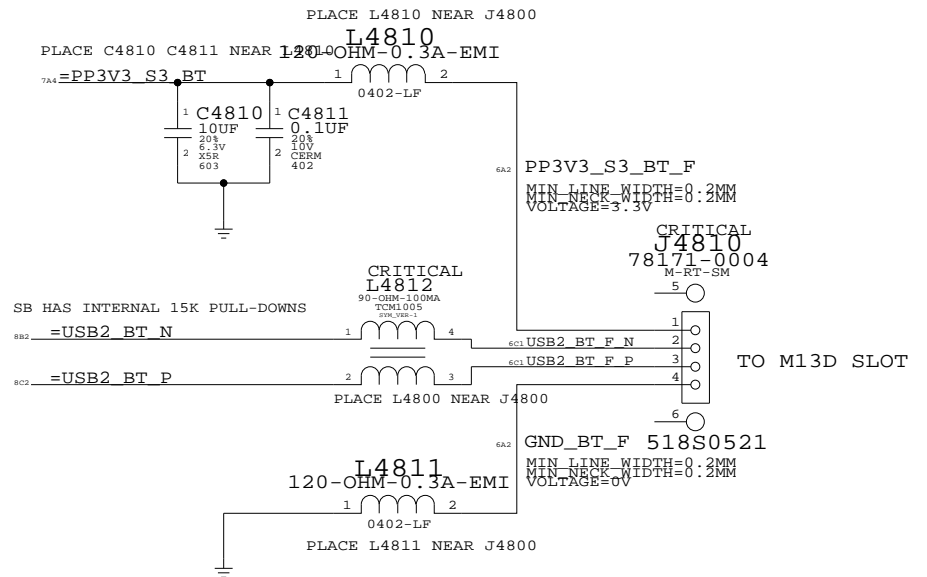
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APPLE INC.	SIZE DRAWING NUMBER REV. D 051-7455 01
	SCALE NONE SHEET 42 OF 76

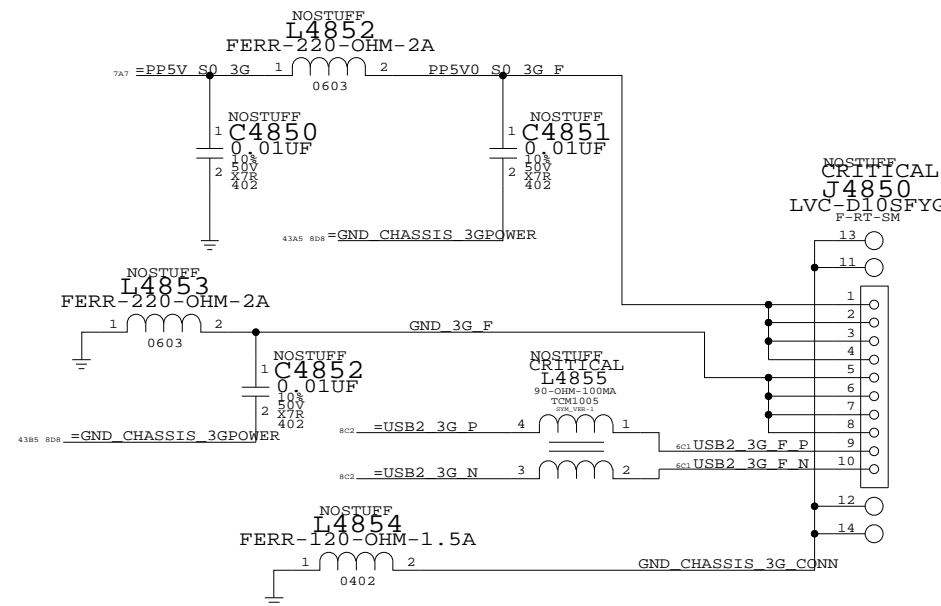
IR CYPRESS ENCORE II USB CONTROLLER



BLUETOOTH



3G CONNECTOR



IR CONTROLLER & BT INTERFACE

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		43	76

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designated as outputs can be left floating, those designated as inputs require pull-ups.

D

D

C

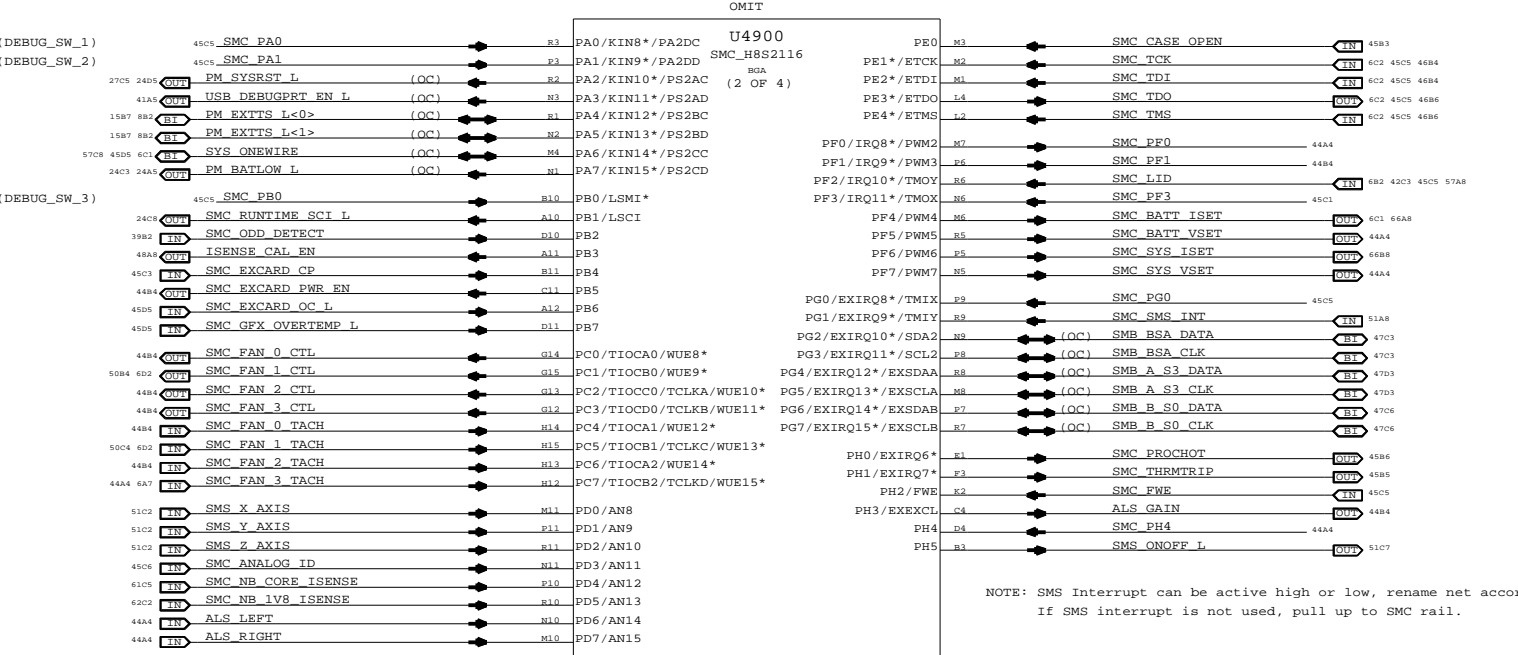
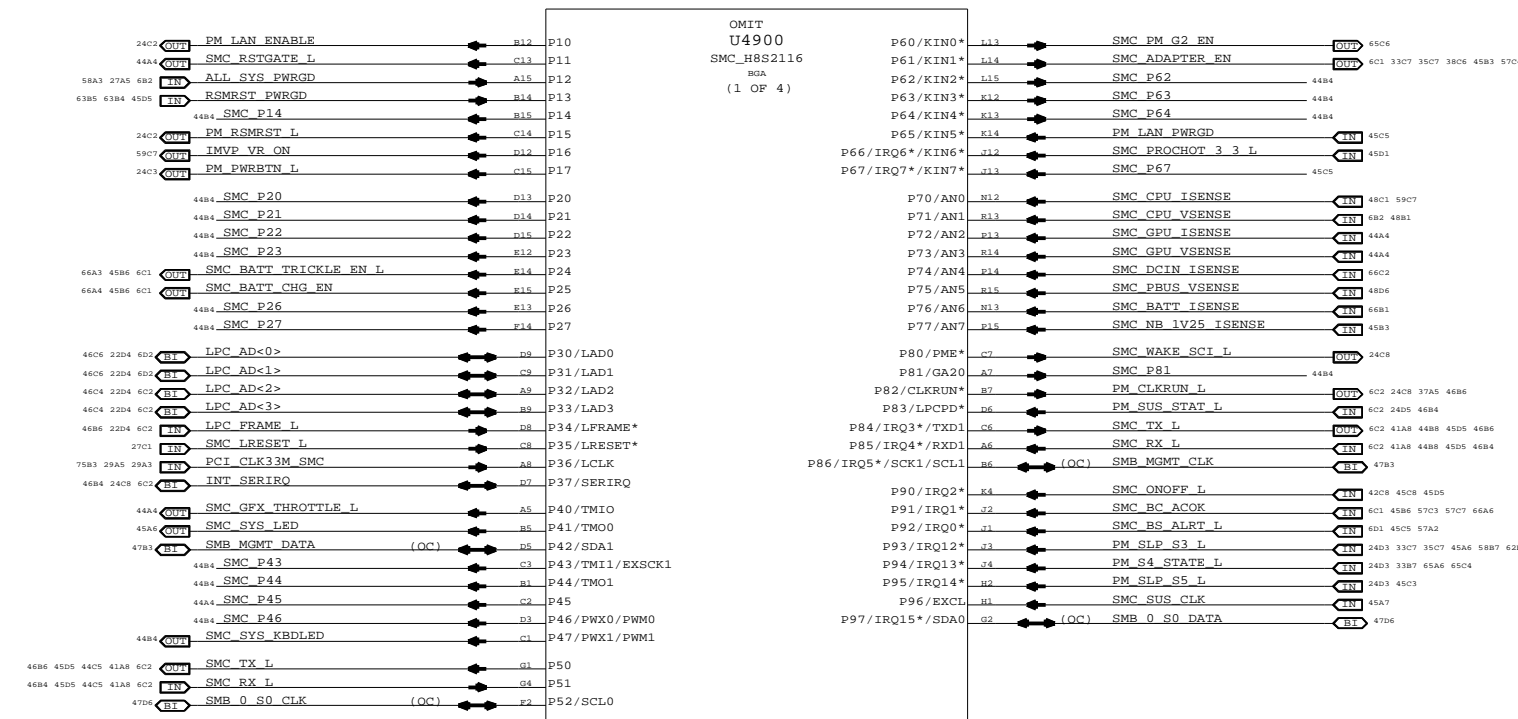
C

B

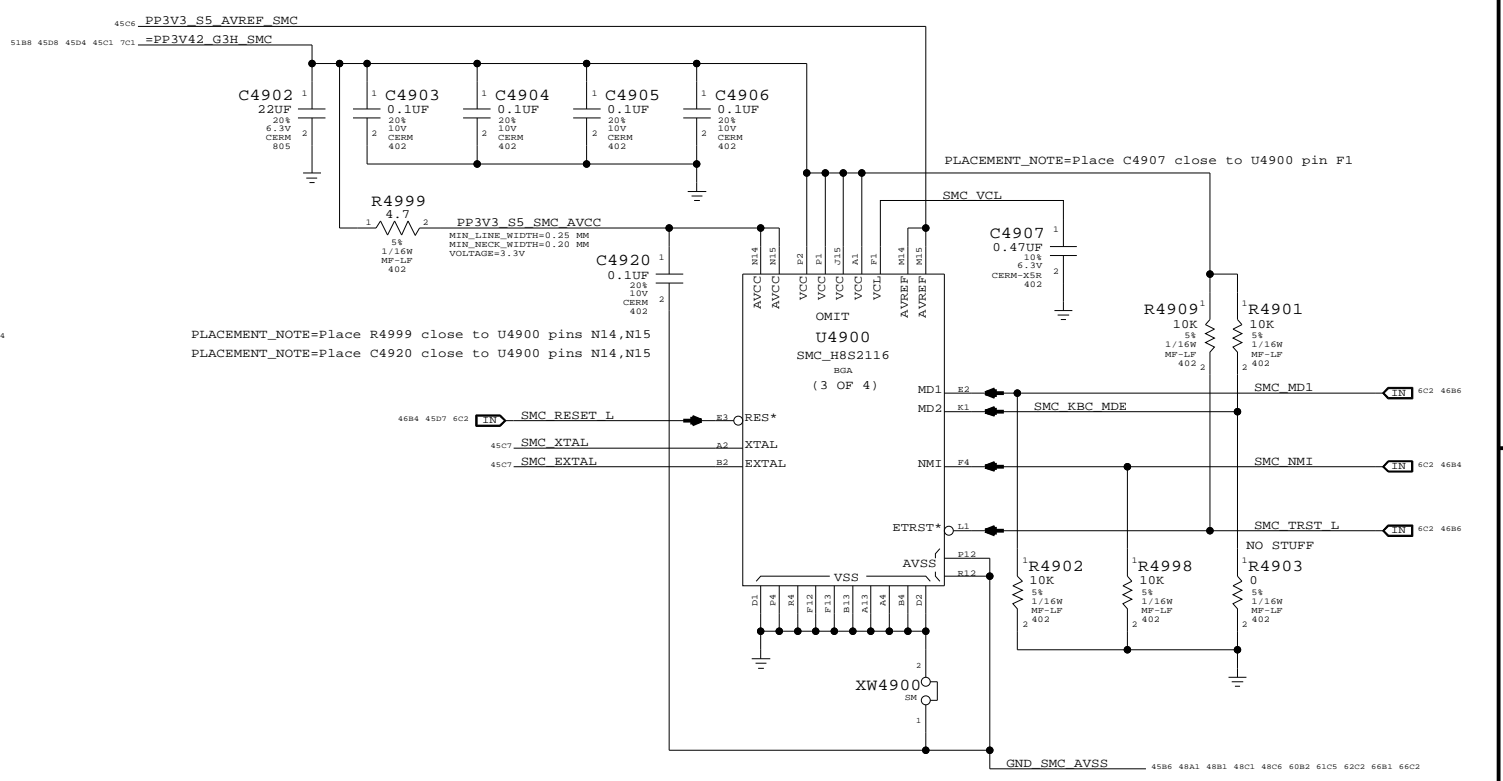
B

A

A



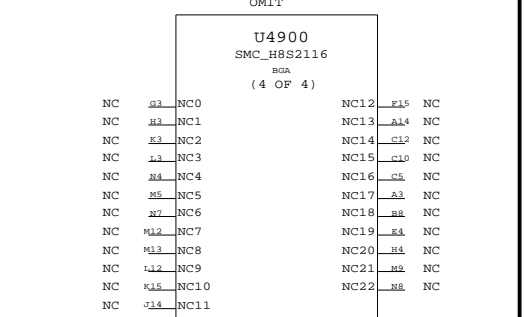
NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.



SMC P14	MAKE_BASE=TRUE	NC	SMC P14
SMC P20	MAKE_BASE=TRUE	NC	SMC P20
SMC P21	MAKE_BASE=TRUE	NC	SMC P21
SMC P22	MAKE_BASE=TRUE	NC	SMC P22
SMC P23	MAKE_BASE=TRUE	NC	SMC P23
SMC P26	MAKE_BASE=TRUE	NC	SMC P26
SMC P27	MAKE_BASE=TRUE	NC	SMC P27
SMC P46	MAKE_BASE=TRUE	NC	SMC P46
SMC P44	MAKE_BASE=TRUE	NC	SMC P44
SMC P43	MAKE_BASE=TRUE	NC	SMC P43
SMC P62	MAKE_BASE=TRUE	NC	SMC P62
SMC P63	MAKE_BASE=TRUE	NC	SMC P63
SMC P64	MAKE_BASE=TRUE	NC	SMC P64
SMC P81	MAKE_BASE=TRUE	NC	SMC P81
SMC PF1	MAKE_BASE=TRUE	NC	SMC PF1

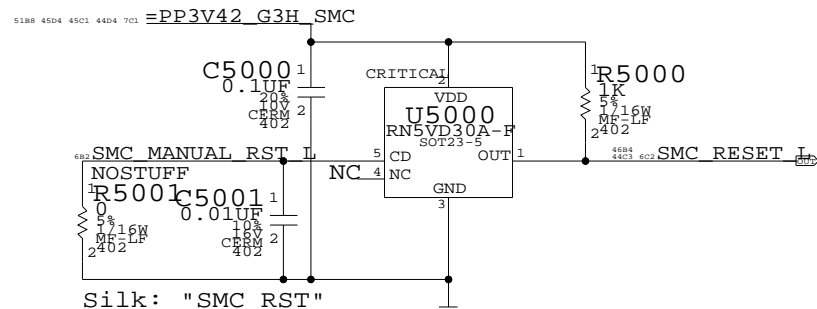
SMC SYS_KBDLED	MAKE_BASE=TRUE	NC	SMC SYS_KBDLED
ALS_GAIN	MAKE_BASE=TRUE	NC	ALS_GAIN
SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	NC	SMC_EXCARD_PWR_EN
SMC_FAN_0_CTL	MAKE_BASE=TRUE	NC	SMC_FAN_0_CTL
SMC_FAN_2_CTL	MAKE_BASE=TRUE	NC	SMC_FAN_2_CTL
SMC_FAN_3_CTL	MAKE_BASE=TRUE	NC	SMC_FAN_3_CTL
SMC_FAN_0_TACH	MAKE_BASE=TRUE	NC	SMC_FAN_0_TACH
SMC_FAN_2_TACH	MAKE_BASE=TRUE	NC	SMC_FAN_2_TACH
SMC_FAN_3_TACH	MAKE_BASE=TRUE	NC	SMC_FAN_3_TACH
ALS_LEFT	MAKE_BASE=TRUE	NC	ALS_LEFT
ALS_RIGHT	MAKE_BASE=TRUE	NC	ALS_RIGHT
SMC_PF0	MAKE_BASE=TRUE	NC	SMC_PF0
SMC_BATT_VSET	MAKE_BASE=TRUE	NC	SMC_BATT_VSET
SMC_SYS_VSET	MAKE_BASE=TRUE	NC	SMC_SYS_VSET
SMC_RSTGATE_L	MAKE_BASE=TRUE	NC	SMC_RSTGATE_L
SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NC	SMC_GFX_THROTTLE_L

SMC_GPU_ISENSE	MAKE_BASE=TRUE	SMC_GPU1_ISENSE	6082 60C7
SMC_GPU_VSENSE	MAKE_BASE=TRUE	SMC_GPU1_VSENSE	4881
SMC_P45	MAKE_BASE=TRUE	SMC_ENRGYSTR_LDO_EN	66D3
SMC_PH4	MAKE_BASE=TRUE	SMC_ENRGYSTR_LDO_PGOOD	45C5 66C1

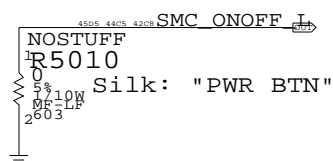


SMC
 SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006
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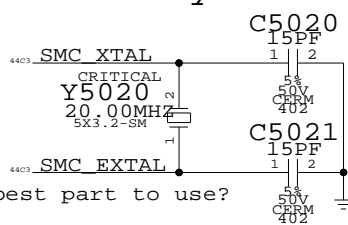
SMC Reset Button / Brownout Detect



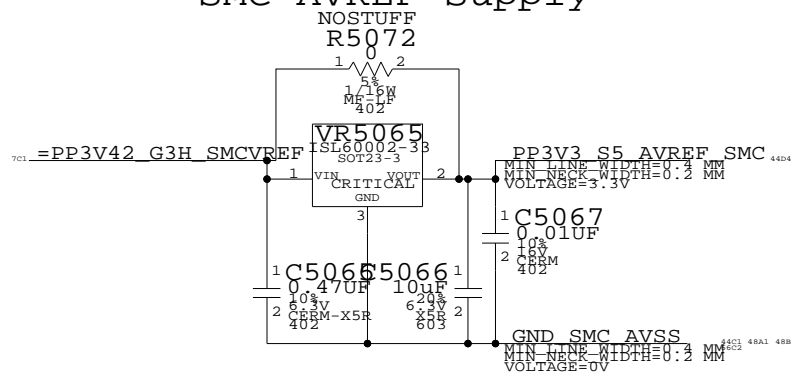
Debug Power Button



SMC Crystal Circuit

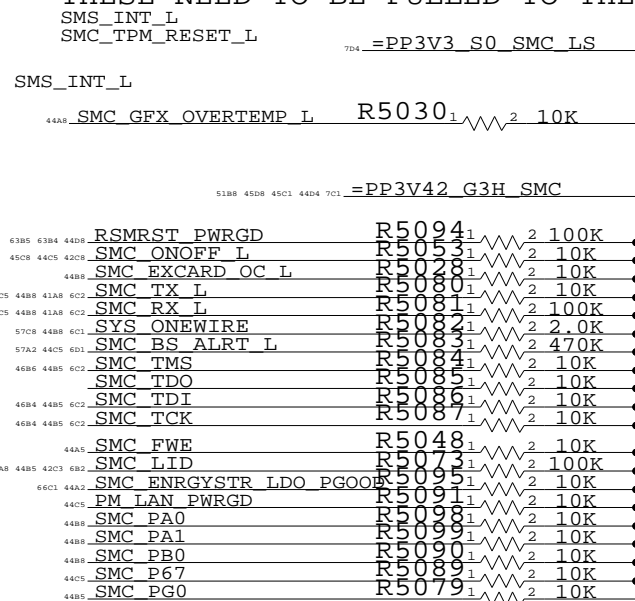


SMC AVREF Supply

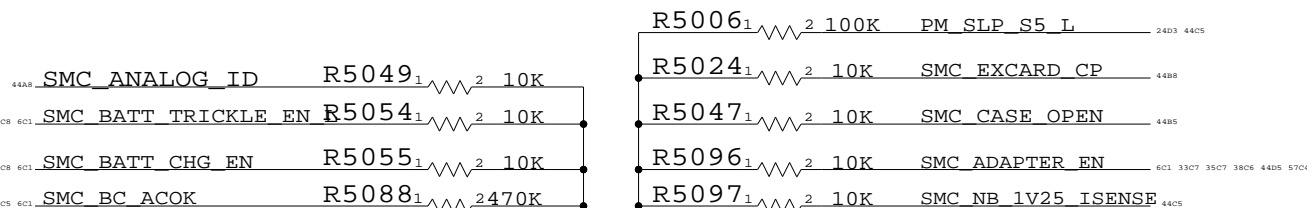
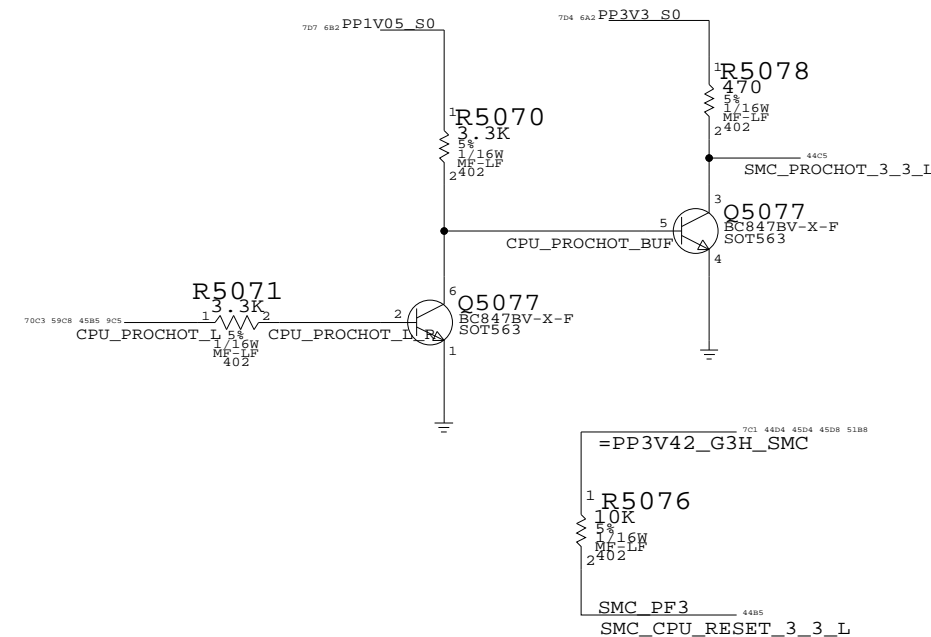


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5065	TI REF3133

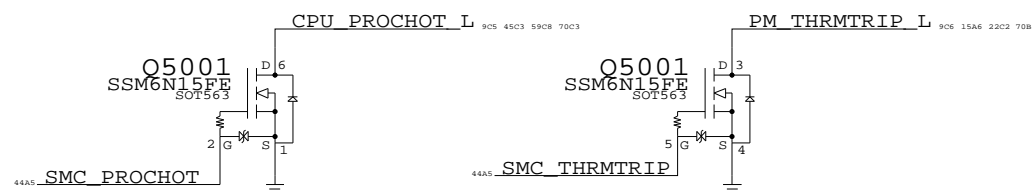
THESE NEED TO BE PULLED TO THE PROPER RAIL:



SMC 1.05V to 3.3V Level Shifting

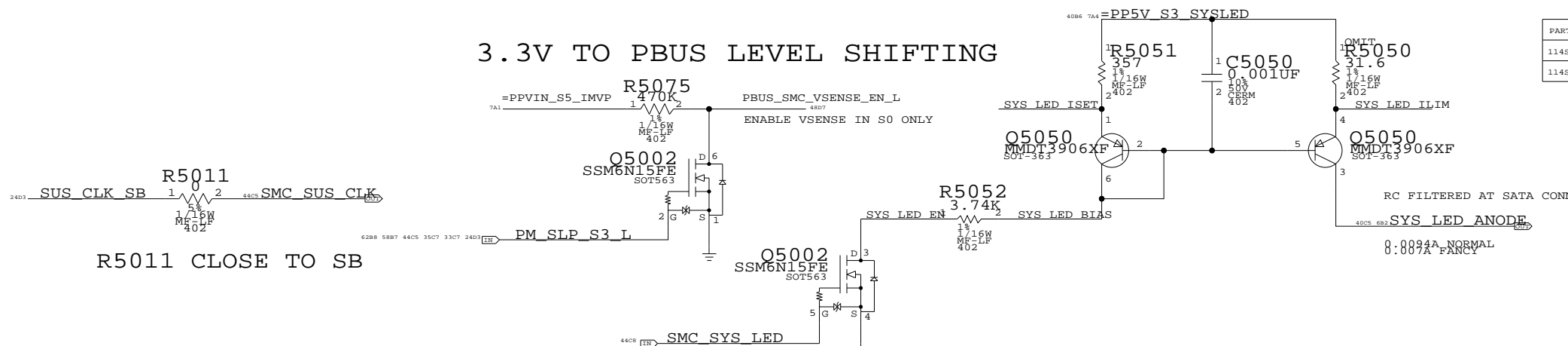


SMC 3.3V to 1.05V Level Shifting



SYSTEM (SLEEP) LED CURRENT DRIVER

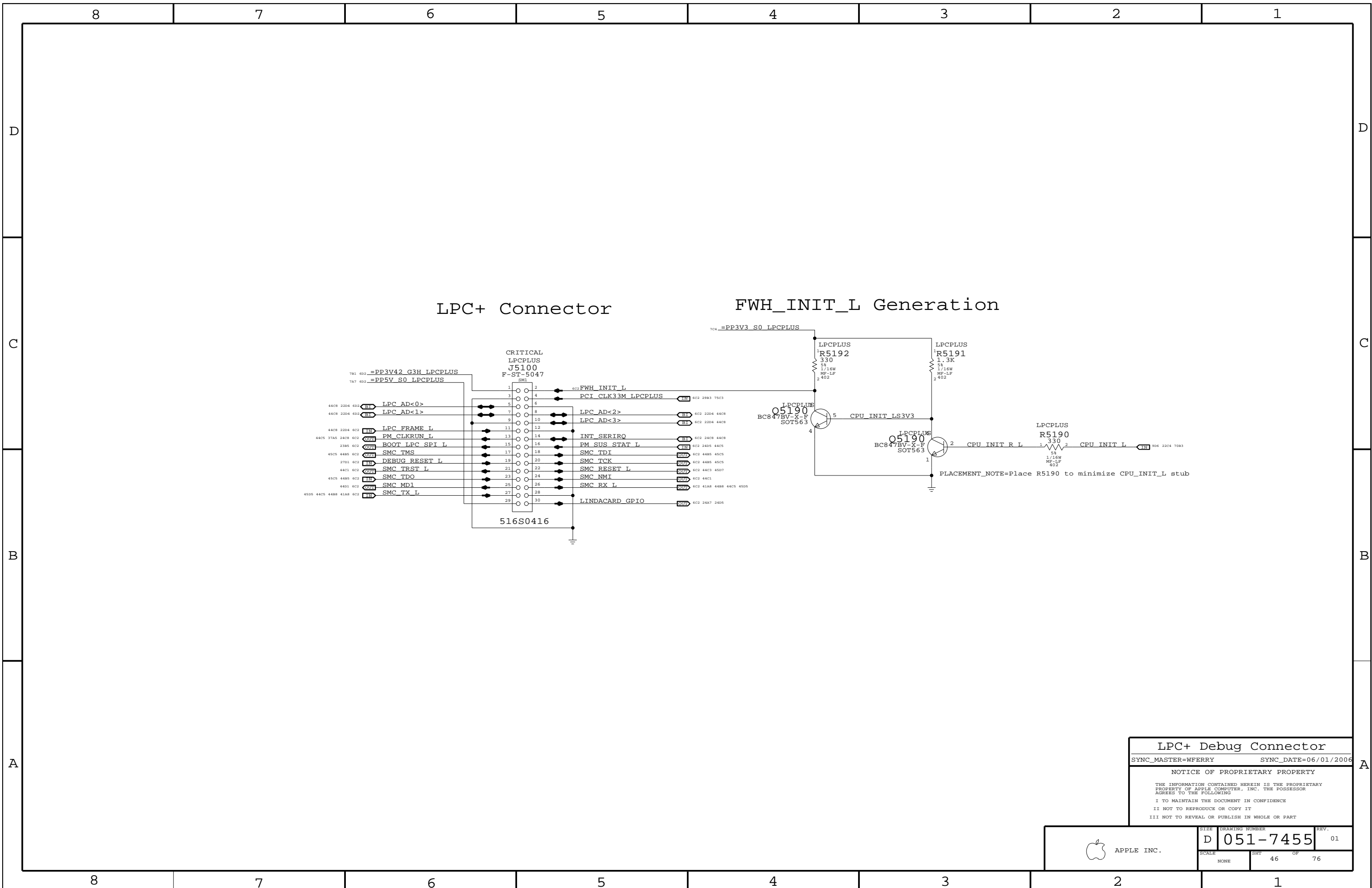
3.3V TO PBUS LEVEL SHIFTING



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0071	1	31.6, 1%, 1/16W, MF-LF, 402	R5050	NORMAL
114S0086	1	44.2, 1%, 1/16W, MF-LF, 402	R5050	FANCY

SMC SUPPORT
 SYNC_MASTER=GPU SYNC_DATE=07/17/2006
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	NONE	45		76	01



LPC+ Connector

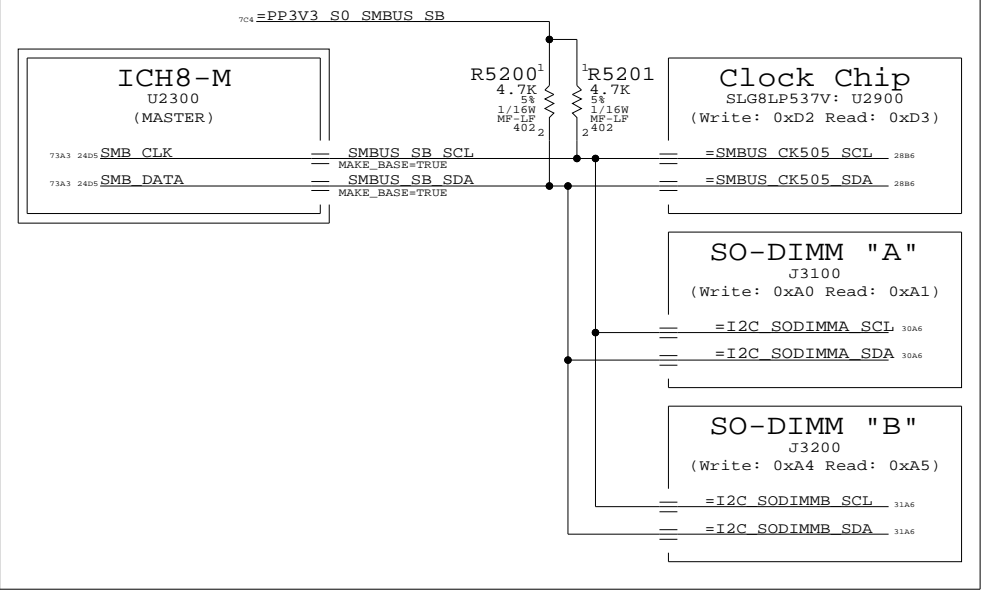
FWH_INIT_L Generation

LPC+ Debug Connector
 SYNC_MASTER=WFERRY SYNC_DATE=06/01/2006
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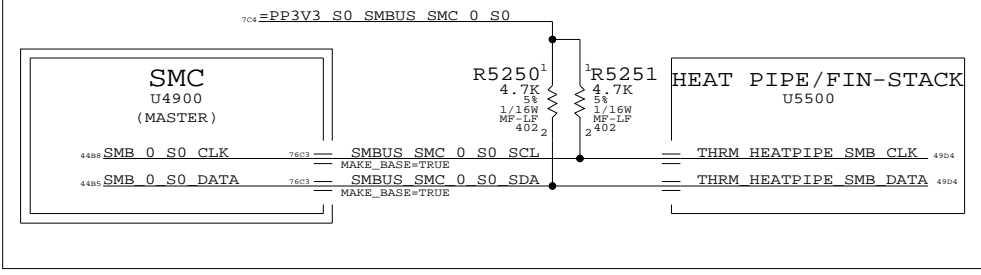
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SCALE		SHT	OF
NONE		46	76

8 7 6 5 4 3 2 1

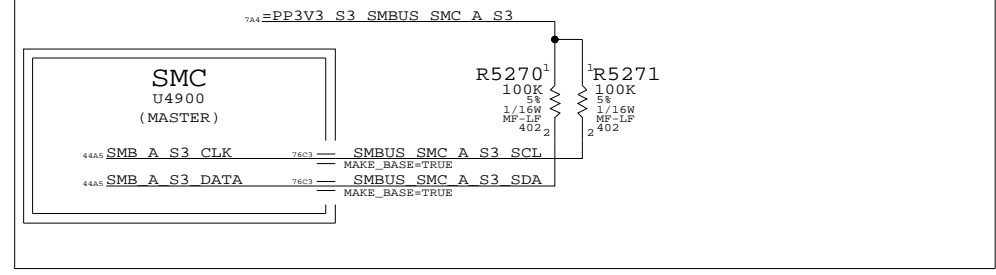
ICH8-M SMBus Connections



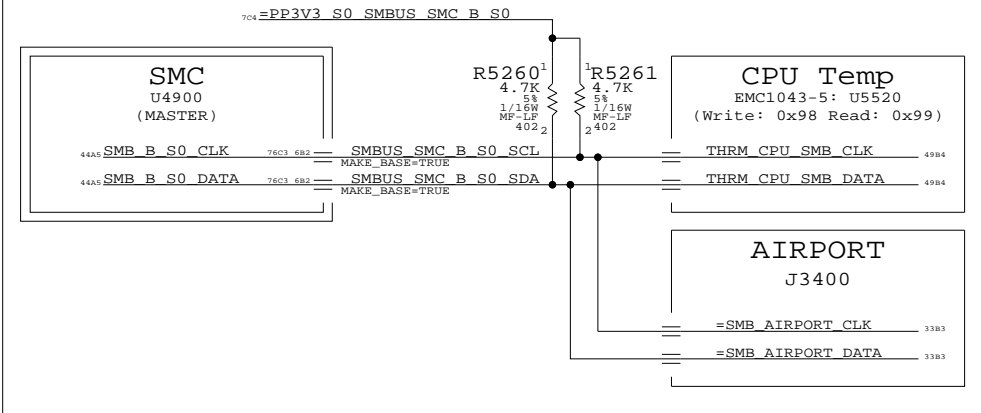
SMC "0" SMBus Connections



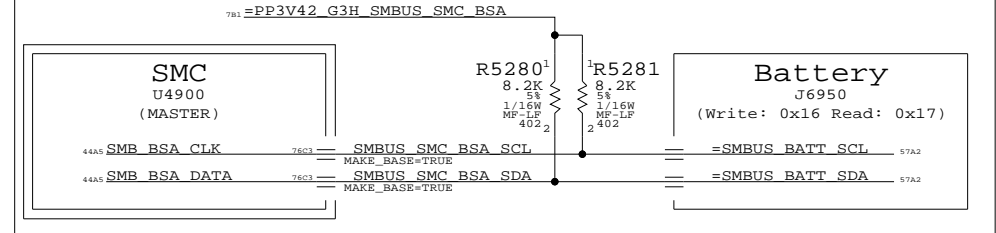
SMC "A" SMBus Connections



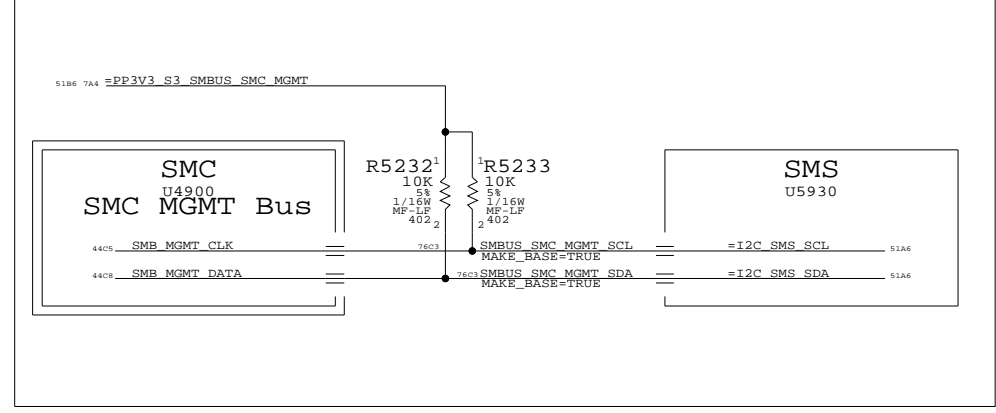
SMC "B" SMBus Connections



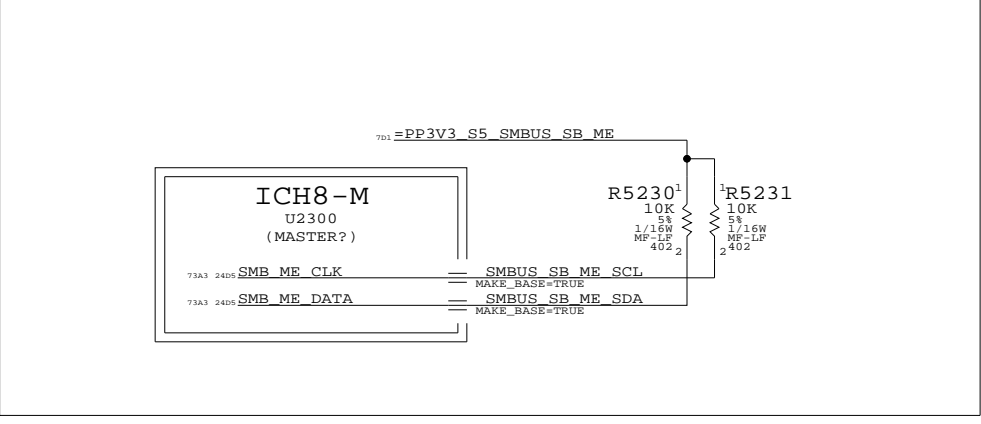
SMC "Battery A" SMBus Connections



SMC "MANAGEMENT" SMBUS CONNECTIONS



ICH8-M ME SMBus Connections



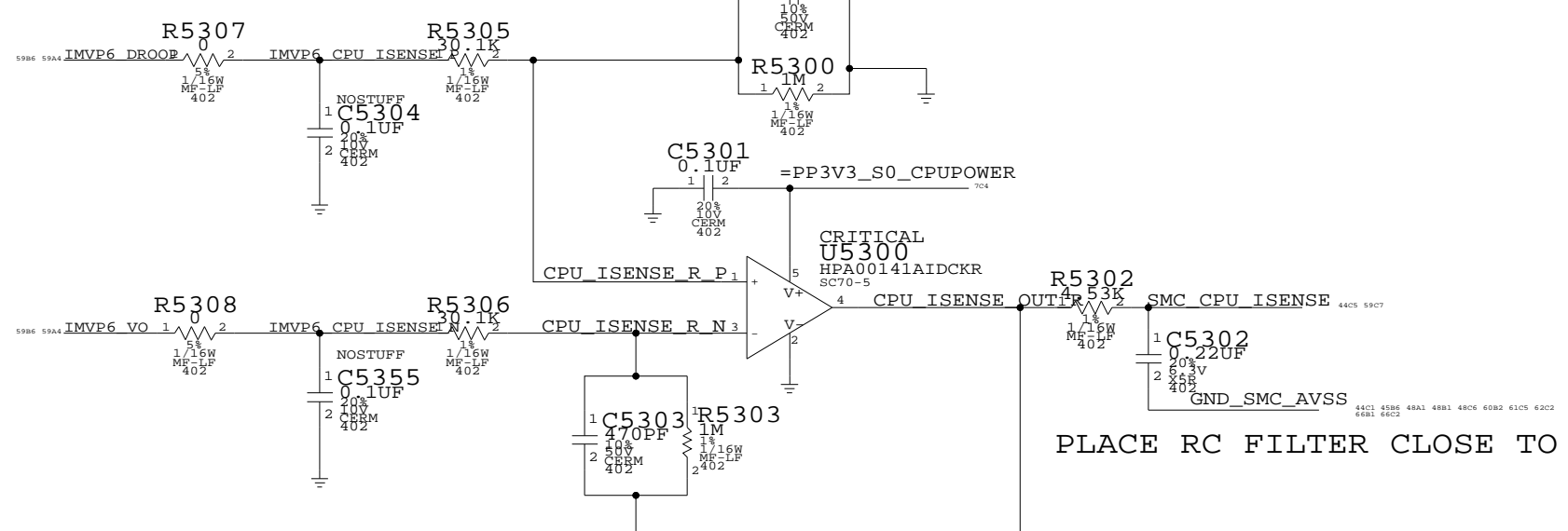
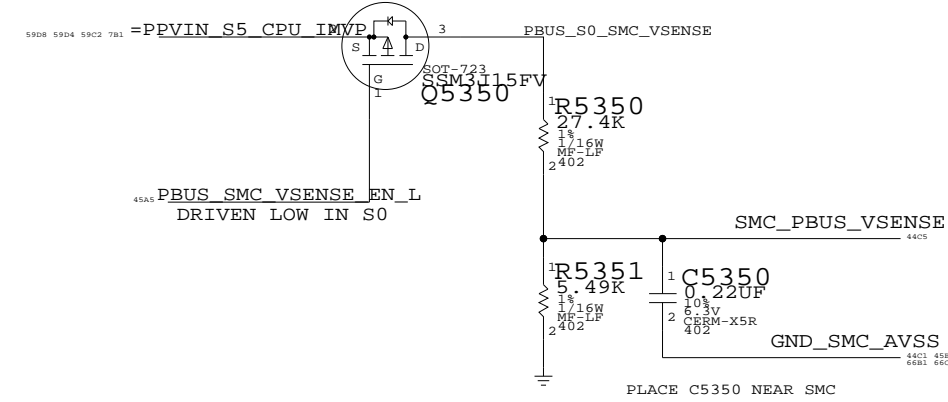
SMBUS CONNECTIONS
 SYNC_MASTER=WFERRY SYNC_DATE=06/01/2006
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	D	051-7455	01
SCALE	SHEET		OF
NONE	47		76

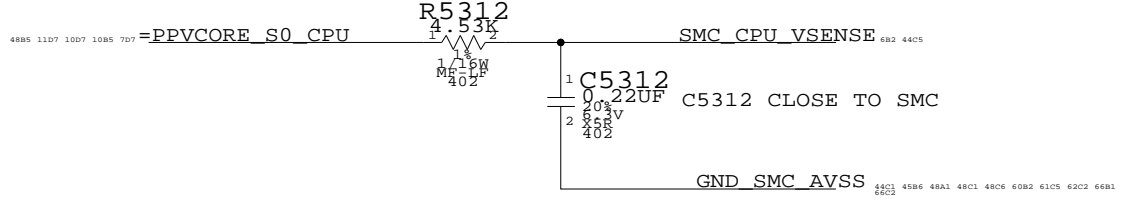
8 7 6 5 4 3 2 1

PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

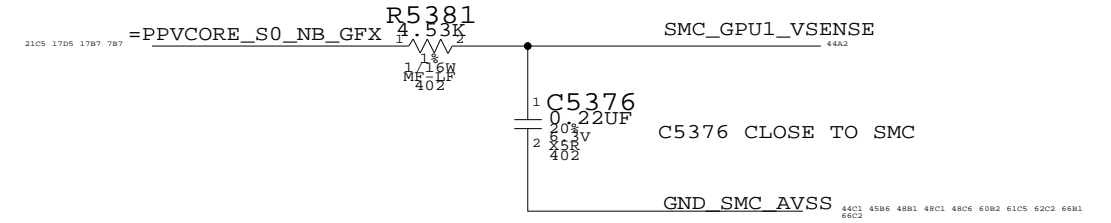
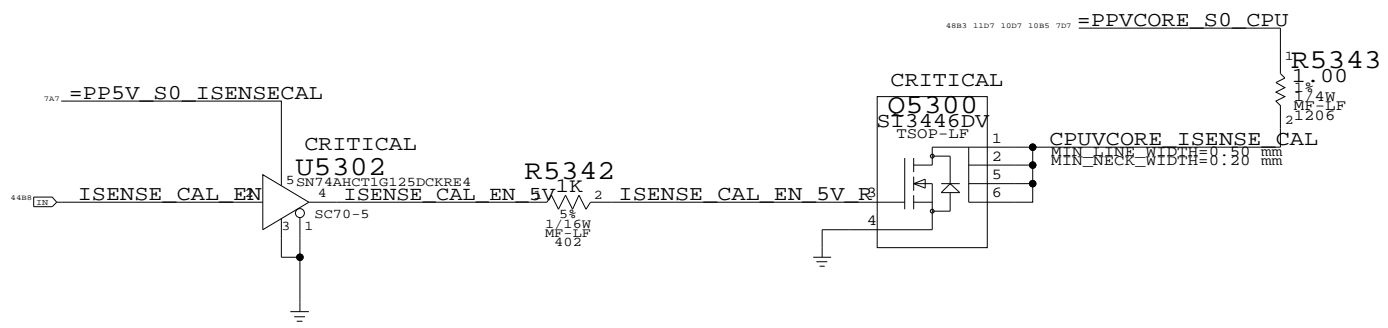


CPU VOLTAGE SENSE



Current Sense Calibration Circuit
Switches in fixed load on power supplies to calibrate current sense circuits

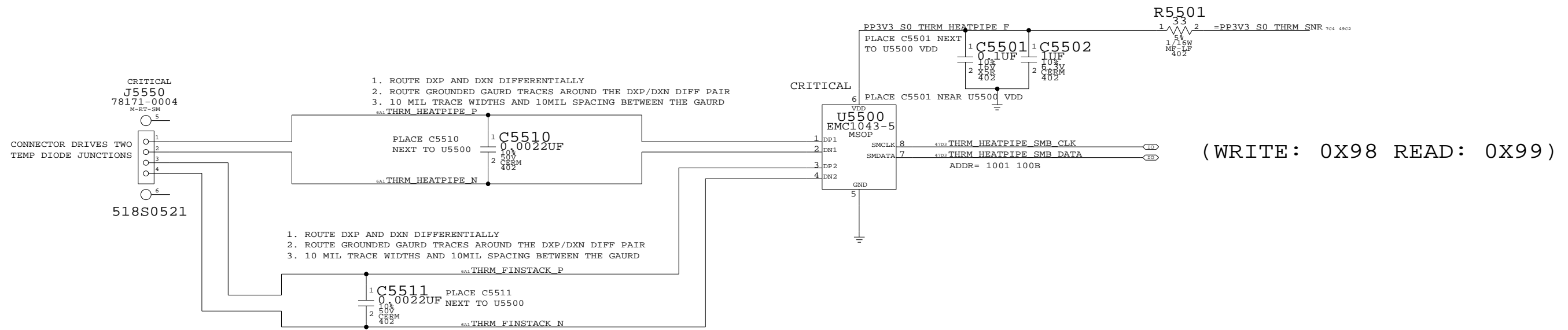
GPU VOLTAGE SENSE



CPU Current & Voltage Sense
 SYNC_MASTER=GPU SYNC_DATE=07/17/2006
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	SHT	OF	REV.
NONE	48	76	

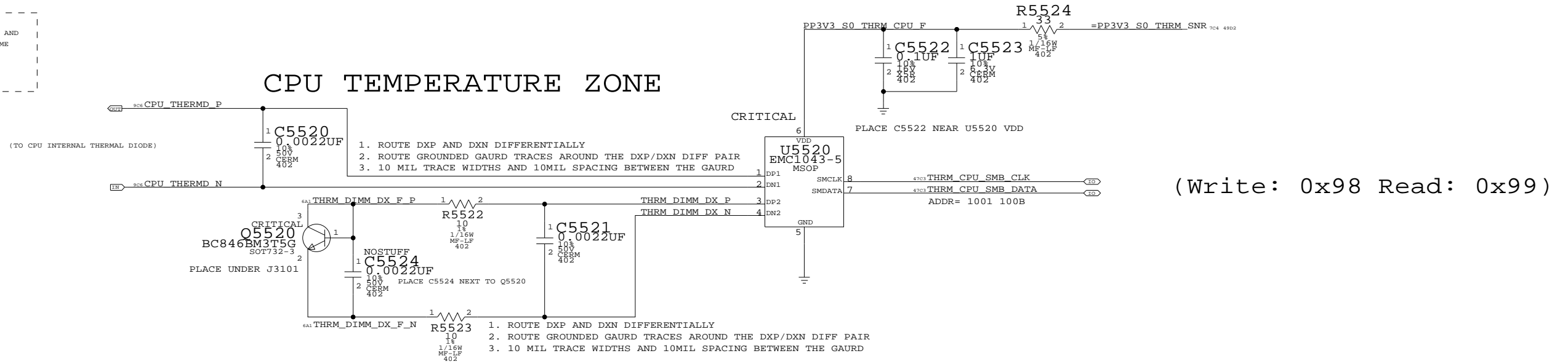
HEAT-PIPE/FIN-STACK TEMPERATURE ZONE



LAYOUT NOTE:
ADD GND GUARD TRACE FOR CPU_THERMD_P AND CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND CPU_THERMD_N ON SAME LAYER.
10 MIL TRACE
10 MIL SPACING

CPU TEMPERATURE ZONE



TEMPERATURE SENSE

SYNC_MASTER=GPU SYNC_DATE=06/21/2006

NOTICE OF PROPRIETARY PROPERTY

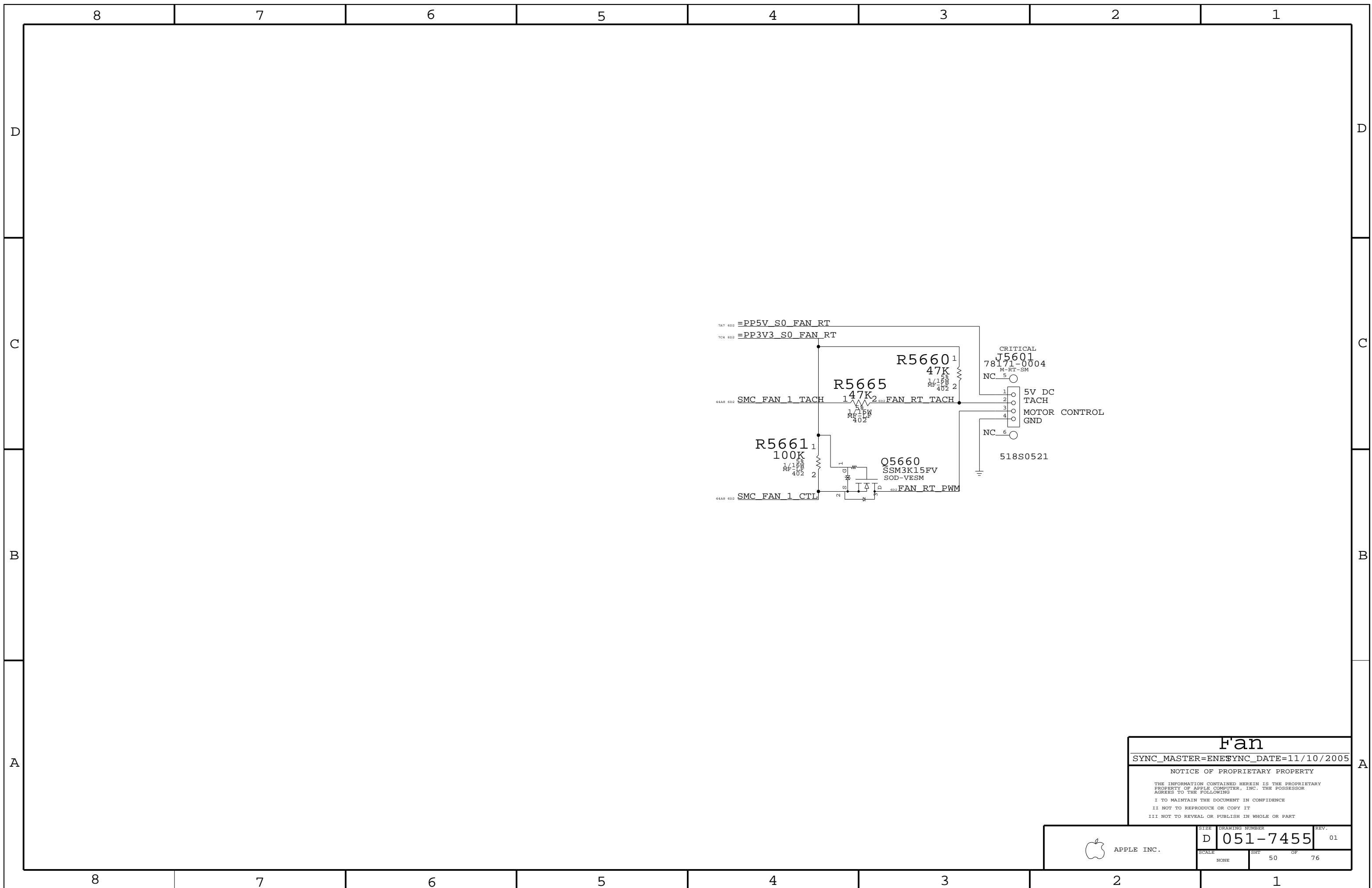
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	NONE	051-7455	01
SCALE		SHT	OF
NONE		49	76



F'an

SYNC_MASTER=ENESYNC_DATE=11/10/2005

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APPLE INC.	SIZE DRAWING NUMBER REV. D 051-7455 01
	SCALE SHEET OF NONE 50 OF 76

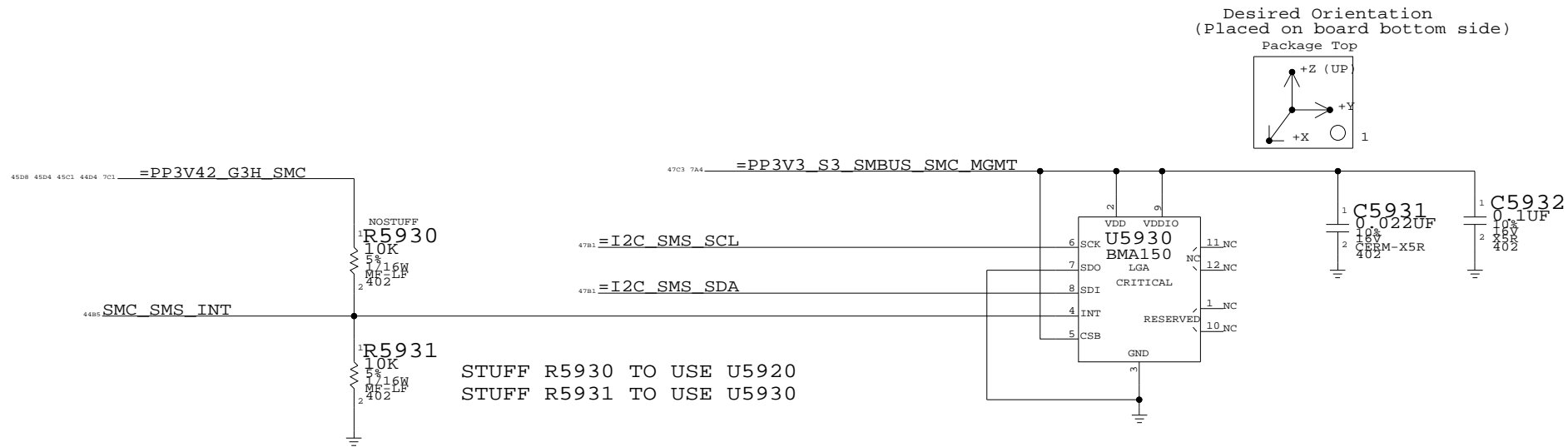
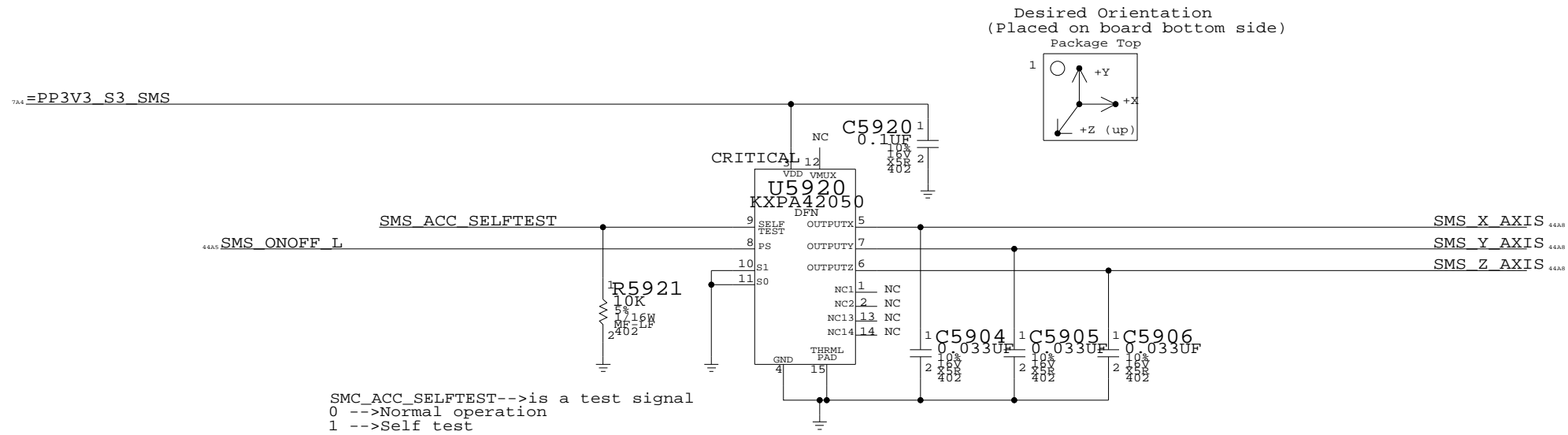
PAGE NOTES

INPUT
 =PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
 SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT
 SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
 7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
 7/28/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L



SMS

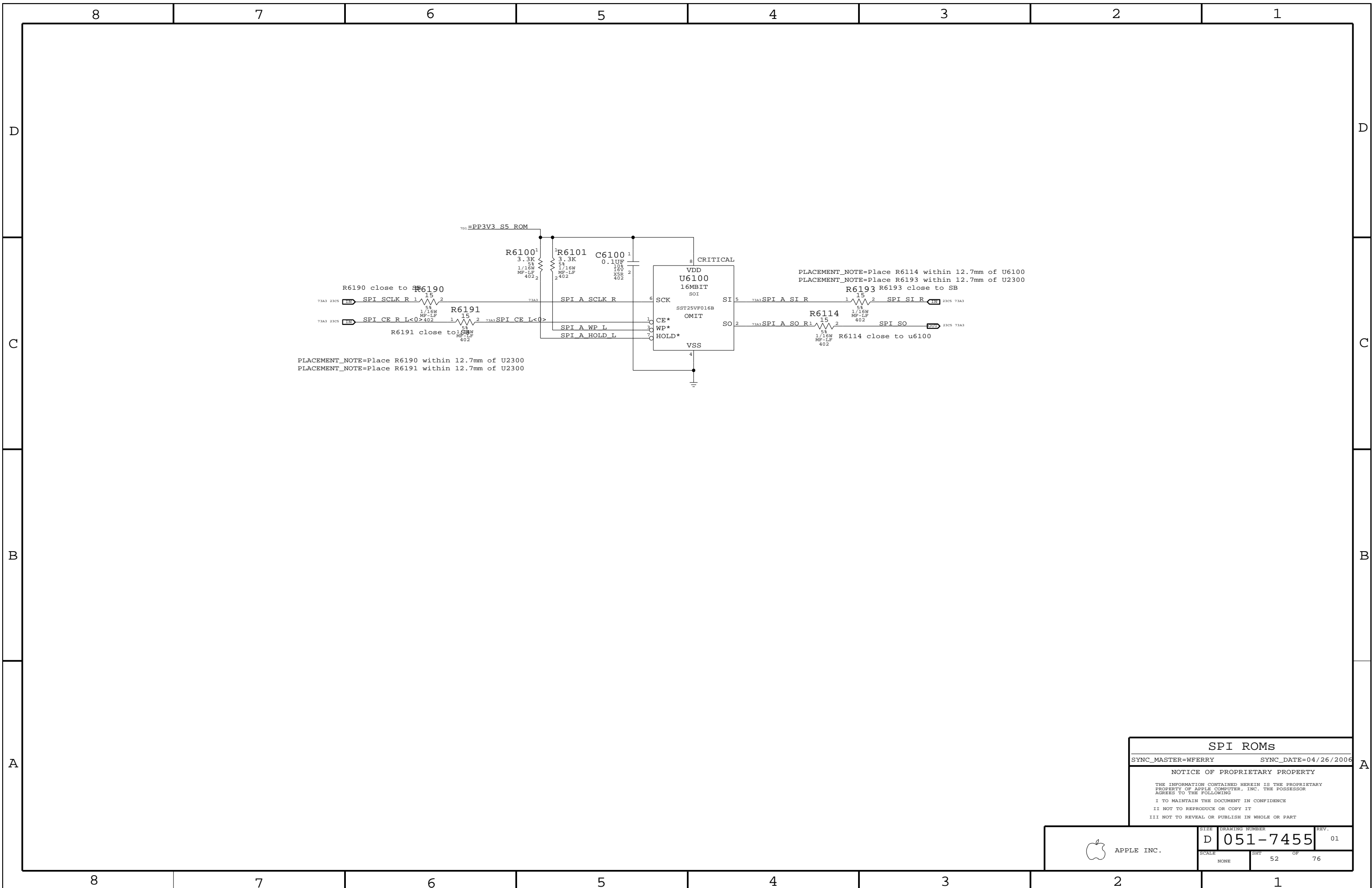
SYNC_MASTER=SMC SYNC_DATE=08/23/2005

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	DRAWING NUMBER		REV.
	D	051-7455	01
SCALE		SHT	OF
NONE		51	76



SPI ROMs

SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

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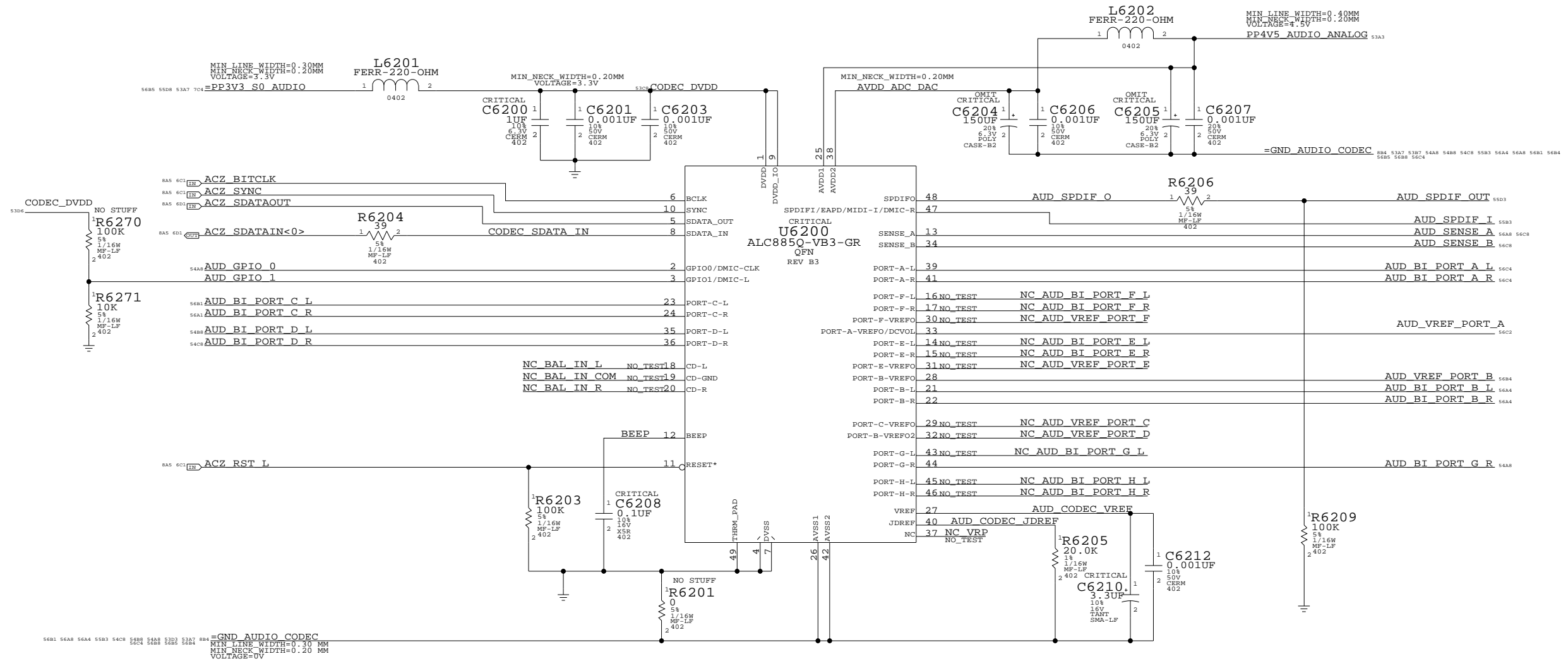
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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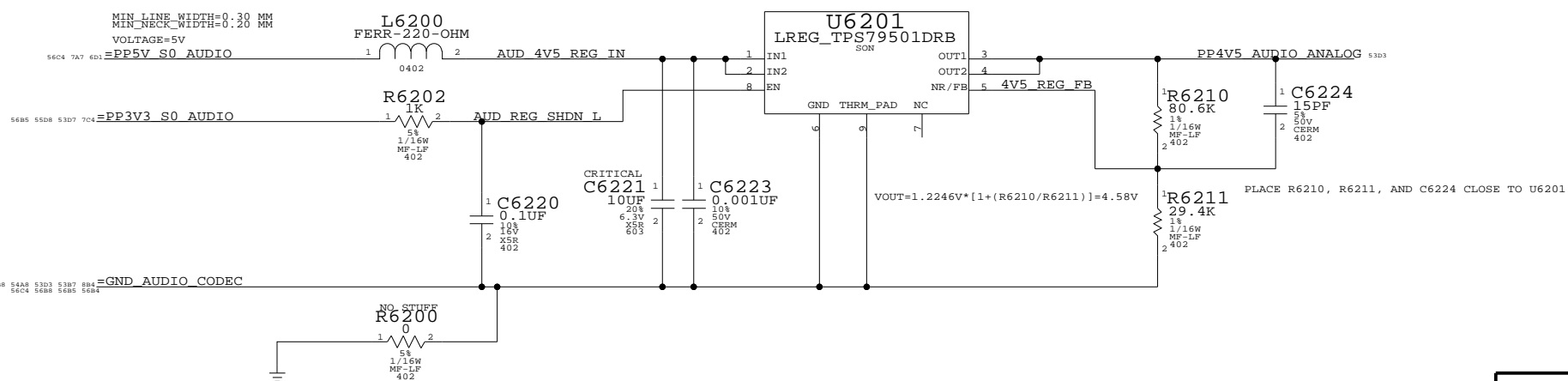
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		52	76

AUDIO CODEC
APPLE P/N 353S1538



AUDIO 4.5V REGULATOR
APPLE P/N 353S1576



AUDIO: CODEC

SYNC_MASTER=M70AUDIO

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	NONE	D 051-7455	01
SCALE		SHT	OF
		53	76

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ
 SUB 80 HZ < FC < 132 HZ
 GAIN 12DB

VOLTAGE=5V
 MIN_LINE_WIDTH=0.60 MM
 MIN_NECK_WIDTH=0.20 MM
 5408 5488 7A7 6D1 =PP5V_S0_AUDIO_AMP

VOLTAGE=5V
 MIN_LINE_WIDTH=0.30 MM
 MIN_NECK_WIDTH=0.20 MM

MIN_LINE_WIDTH=0.30 mm MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm
 5404 SPKRAMP_R_P_OUT R6660 SPKRCONN_R_P_OUT

MIN_LINE_WIDTH=0.30 mm MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm
 5404 SPKRAMP_R_N_OUT R6661 SPKRCONN_R_N_OUT

RIGHT SATELLITE

MIN_LINE_WIDTH=0.30 mm MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm
 5404 SPKRAMP_L_P_OUT R6670 SPKRCONN_L_P_OUT

MIN_LINE_WIDTH=0.30 mm MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm
 5404 SPKRAMP_L_N_OUT R6671 SPKRCONN_L_N_OUT

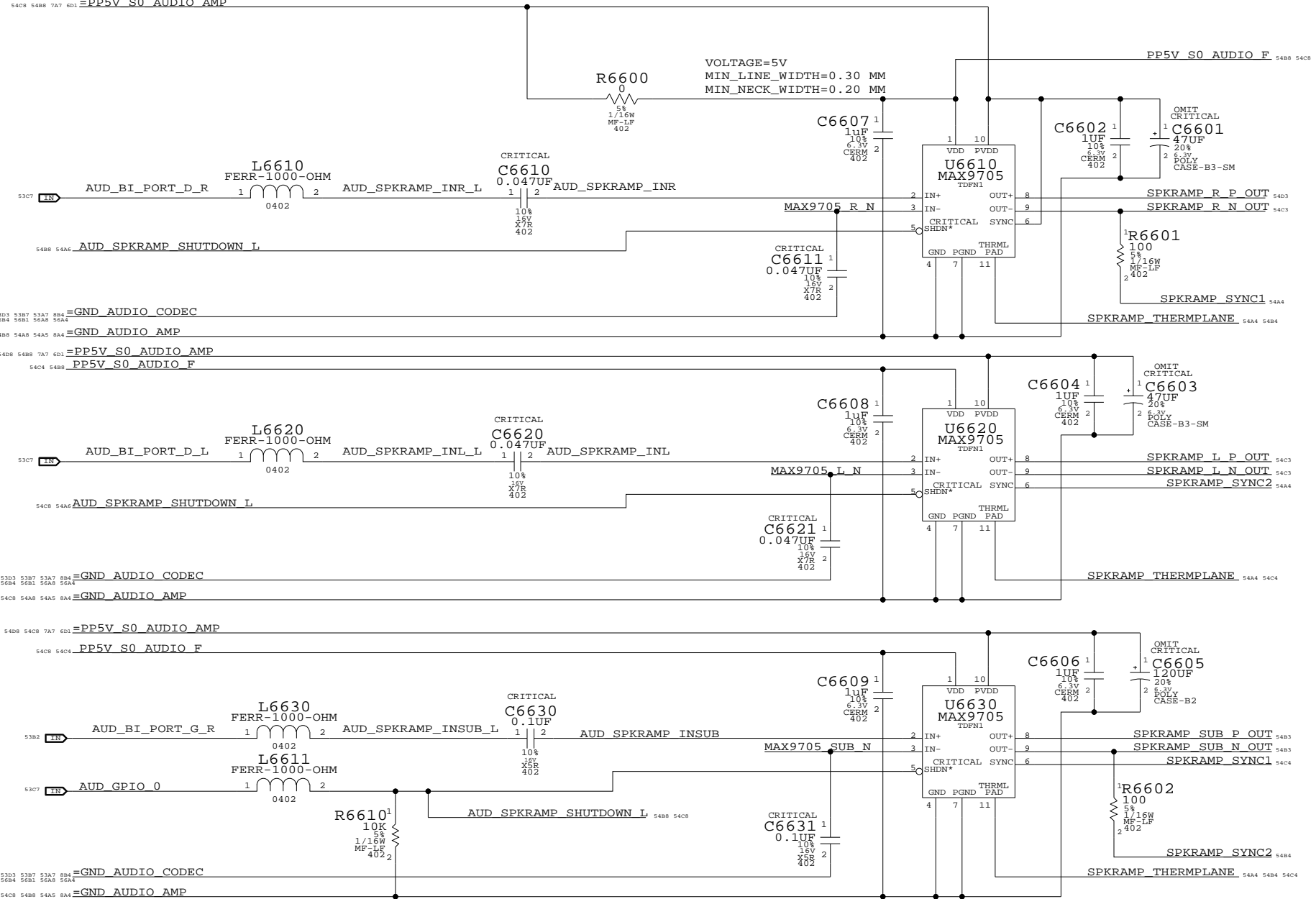
LEFT SATELLITE

MIN_LINE_WIDTH=0.30 mm MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm
 5404 SPKRAMP_SUB_P_OUT R6680 SPKRCONN_SUB_P_OUT

MIN_LINE_WIDTH=0.30 mm MIN_LINE_WIDTH=0.30 mm
 MIN_NECK_WIDTH=0.20 mm MIN_NECK_WIDTH=0.20 mm
 5404 SPKRAMP_SUB_N_OUT R6681 SPKRCONN_SUB_N_OUT

SUB-TWEETER

MIN_LINE_WIDTH=0.60 MM XW6600
 MIN_NECK_WIDTH=0.20 MM SM
 5408 5488 54A5 8A4 =GND_AUDIO_AMP 1 0 2 SPKRAMP_THERMPLANE 54A4 54B4 54C4



AUDIO: SPEAKER AMP

SYNC_MASTER=M70AUDIO SYNC_DATE=03/12/2007

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	NONE	051-7455	01
SCALE		SHT	OF
NONE		54	76

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR

APN:518S0392

CRITICAL
J6701
48227-0301
M-RT-SM

SPEAKER CONNECTOR

APN:518S0519

CRITICAL
J6702
78171-0002
M-RT-SM

CRITICAL
J6703
78171-0004
M-RT-SM

APN:518S0521

XW6705

MIC EMI FILTER

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

AUDIO: JACK

SYNC_MASTER=M70AUDIO SYNC_DATE=03/12/2007

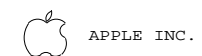
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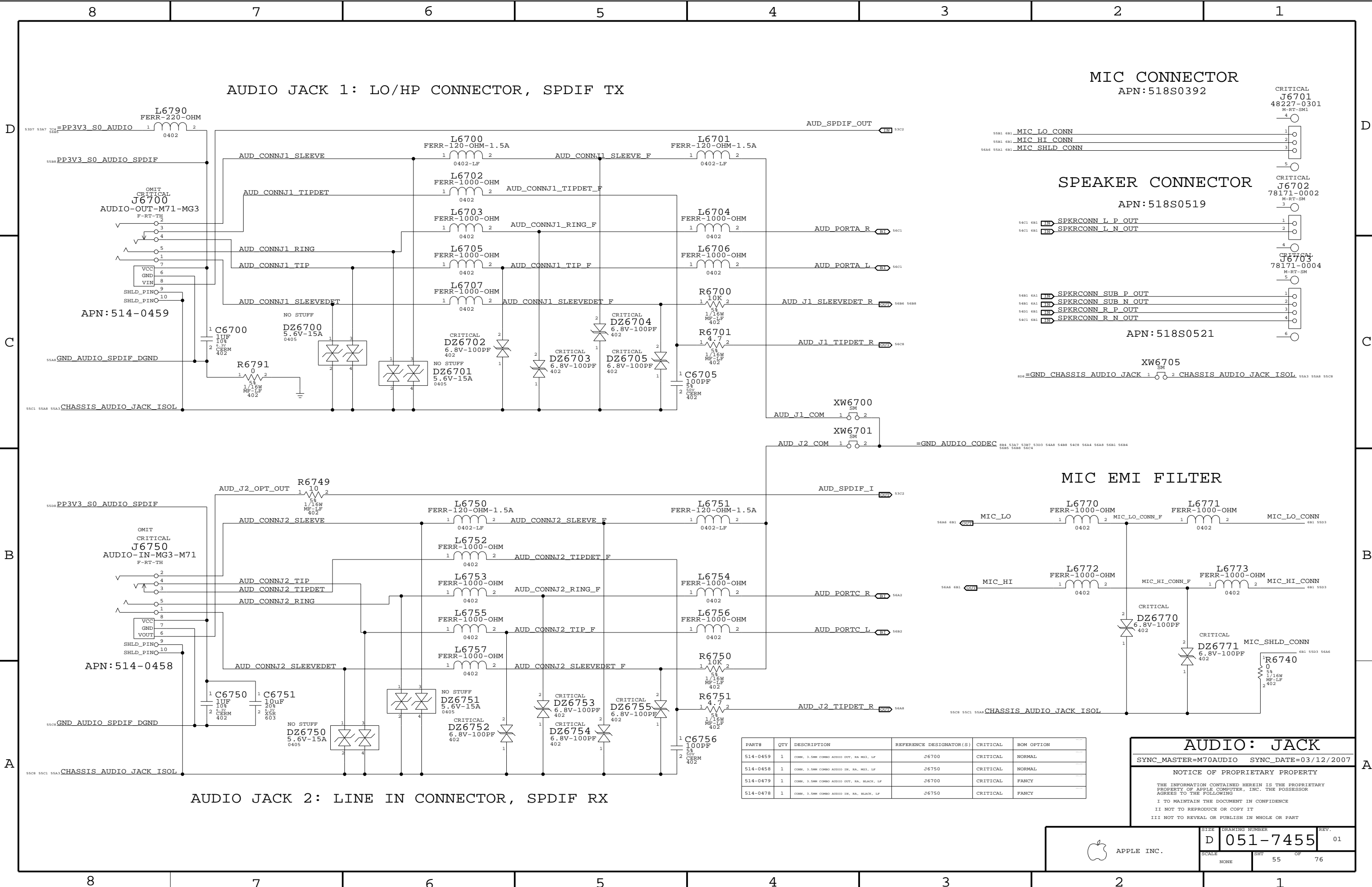
APPLE INC.

SCALE DRAWING NUMBER REV.

D 051-7455 01

SCALE NONE SHEET 55 OF 76

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0459	1	CONN, 3.5MM COMBO AUDIO OUT, RA, NEG, LP	J6700	CRITICAL	NORMAL
514-0458	1	CONN, 3.5MM COMBO AUDIO IN, RA, NEG, LP	J6750	CRITICAL	NORMAL
514-0479	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LP	J6700	CRITICAL	FANCY
514-0478	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LP	J6750	CRITICAL	FANCY



CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

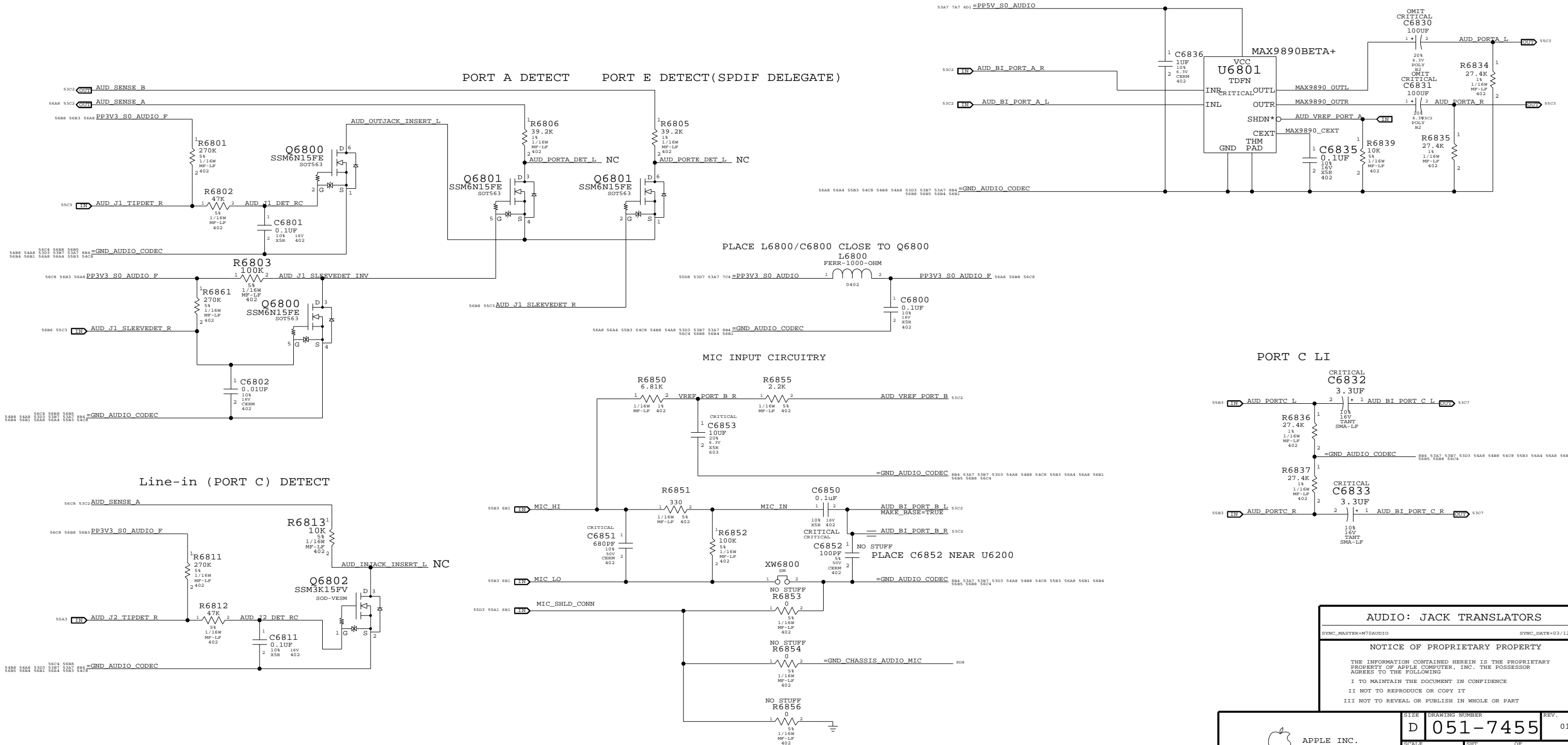
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

HP/LO DE-POP SWITCH
APN:353S1459

PORT A HP/LO

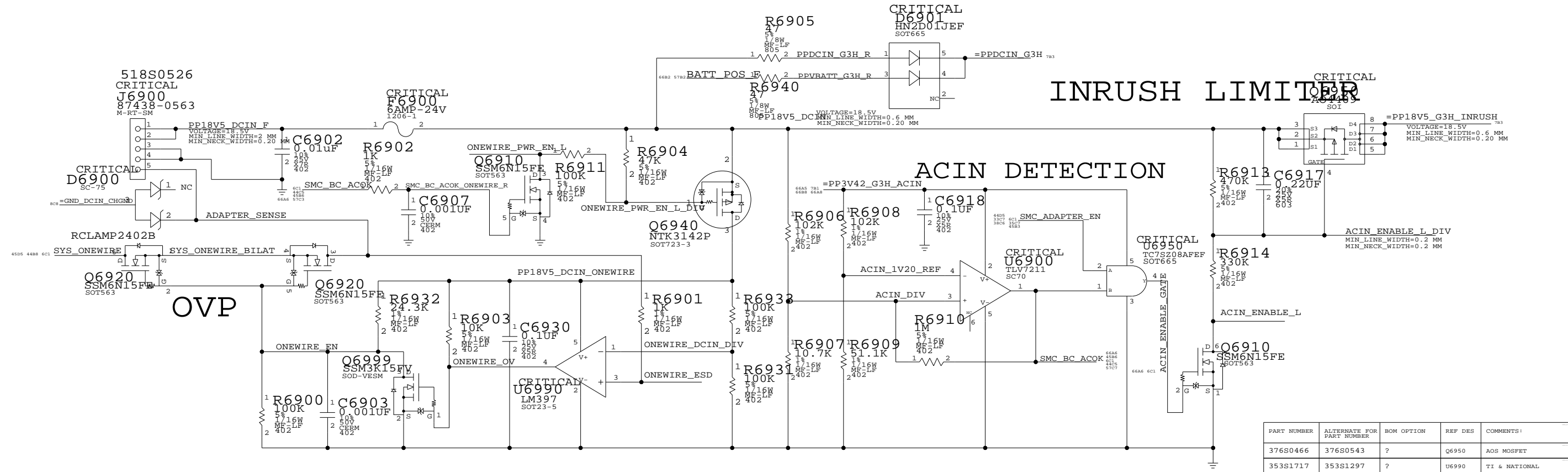
PORT A DETECT PORT E DETECT (SPDIF DELEGATE)



AUDIO: JACK TRANSLATORS
 SYNC_MASTER=M7AUDIO SYNC_DATE=03/12/2007
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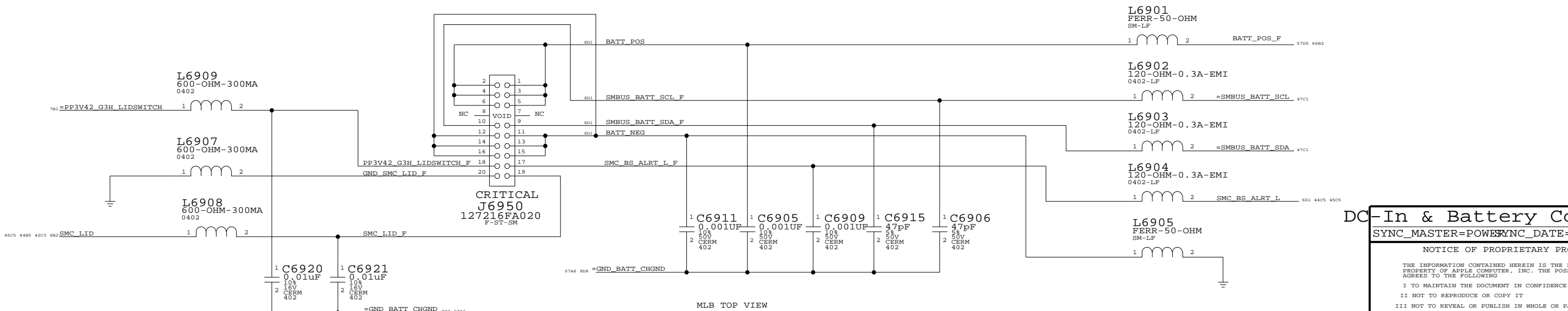
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	SCALE	56	01

DC-JACK INTERFACE



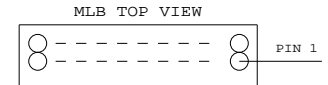
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0466	376S0543	?	Q6950	AOS MOSFET
353S1717	353S1297	?	U6990	TI & NATIONAL

BATTERY INTERFACE



DC-In & Battery Connectors
 SYNC_MASTER=POWER_NG_DATE=07/13/2005

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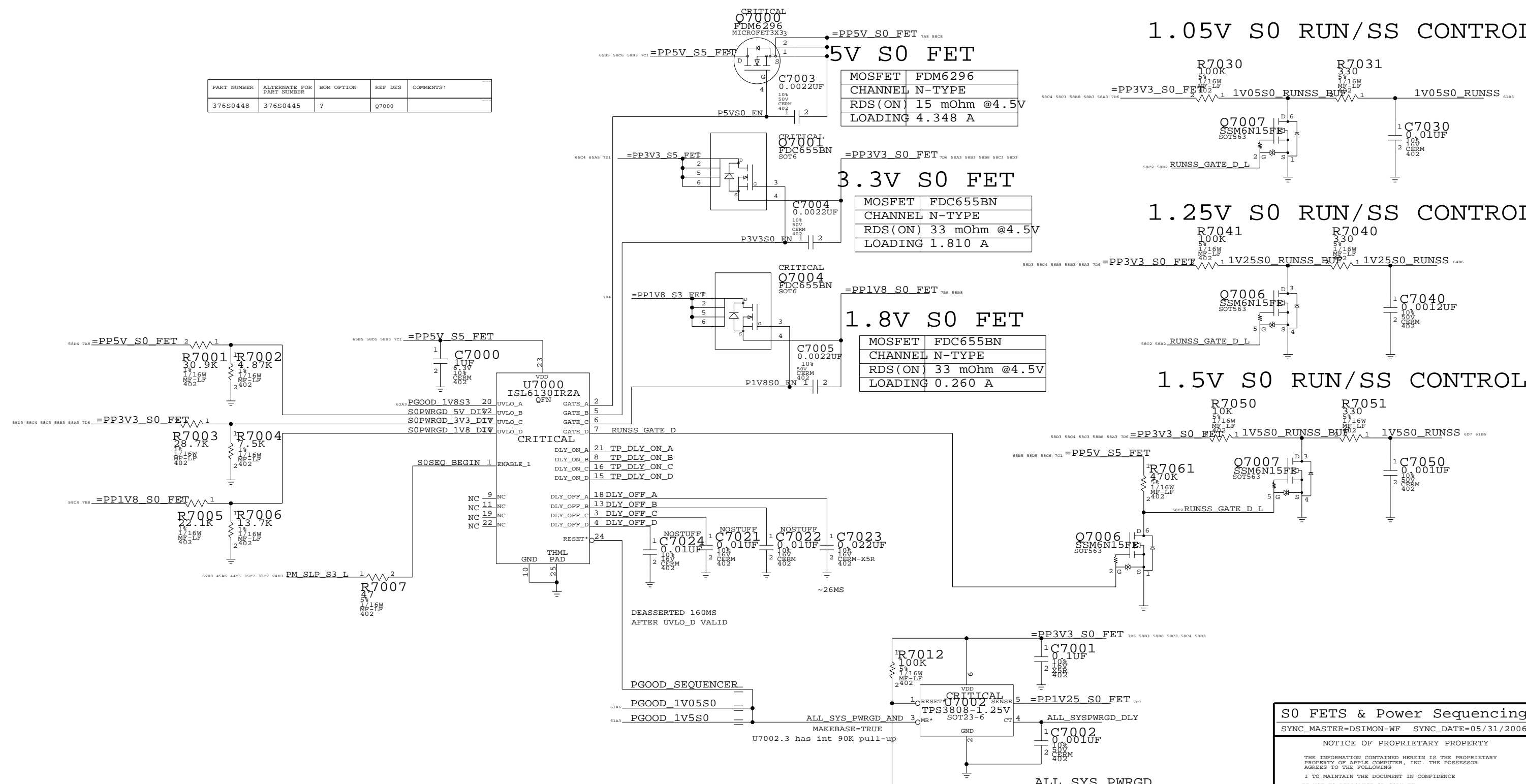
LID HALL EFFECT SENSOR

APPLE INC.

SIZE	D	DRAWING NUMBER	051-7455	REV.	01
SCALE	NONE	SHT	57	OF	76

S0 FETS & POWER SEQUENCING & PGOOD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q7000	

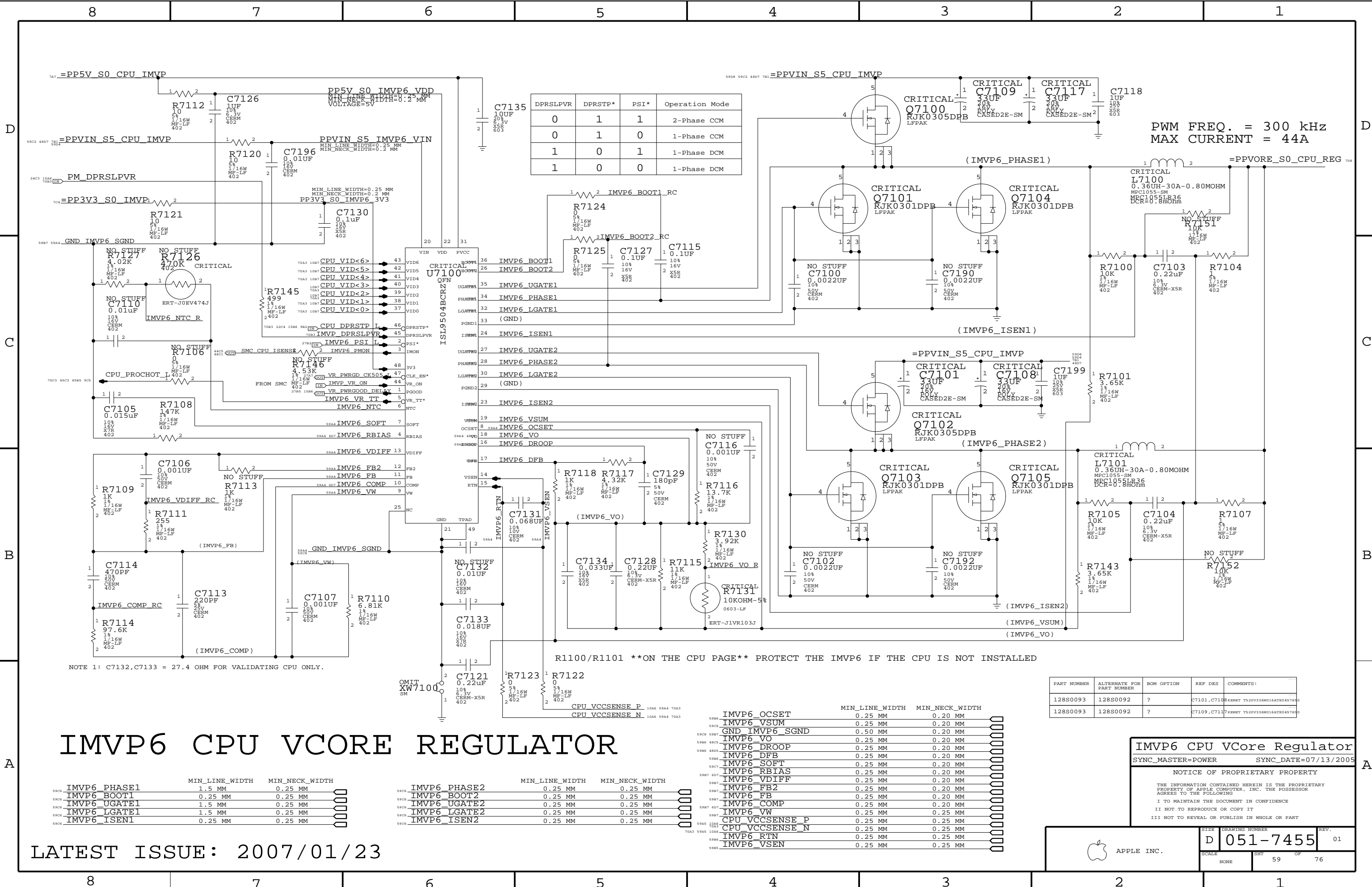


S0 FETS & Power Sequencing
 SYNC_MASTER=DSIMON-WF SYNC_DATE=05/31/2006

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DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

PWM FREQ. = 300 kHz
MAX CURRENT = 44A

NOTE 1: C7132, C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5986 IMVP6_PHASE1	1.5 MM	0.25 MM
5987 IMVP6_BOOT1	0.25 MM	0.25 MM
5988 IMVP6_UGATE1	1.5 MM	0.25 MM
5989 IMVP6_LGATE1	1.5 MM	0.25 MM
5990 IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5991 IMVP6_PHASE2	0.25 MM	0.25 MM
5992 IMVP6_BOOT2	0.25 MM	0.25 MM
5993 IMVP6_UGATE2	0.25 MM	0.25 MM
5994 IMVP6_LGATE2	0.25 MM	0.25 MM
5995 IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5996 IMVP6_OCSET	0.25 MM	0.20 MM
5997 IMVP6_VSUM	0.25 MM	0.20 MM
5998 GND_IMVP6_SGND	0.50 MM	0.20 MM
5999 IMVP6_VO	0.25 MM	0.20 MM
5986 48C5 IMVP6_DROOP	0.25 MM	0.20 MM
5986 48D5 IMVP6_DFB	0.25 MM	0.20 MM
5986 IMVP6_SOFT	0.25 MM	0.20 MM
5987 IMVP6_RBIAS	0.25 MM	0.20 MM
5987 6D7 IMVP6_VDIFF	0.25 MM	0.20 MM
5987 IMVP6_FB2	0.25 MM	0.20 MM
5987 IMVP6_FB	0.25 MM	0.20 MM
5987 IMVP6_COMP	0.25 MM	0.20 MM
5987 6D7 IMVP6_VW	0.25 MM	0.25 MM
5987 CPU_VCCSENSE_P	0.25 MM	0.25 MM
5987 CPU_VCCSENSE_N	0.25 MM	0.25 MM
5987 10A5 IMVP6_RTN	0.25 MM	0.25 MM
5987 10A5 IMVP6_VSEN	0.25 MM	0.25 MM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7101, C7108	KEMET T520V336M016ATE0457690
128S0093	128S0092	?	C7109, C7117	KEMET T520V336M016ATE0457690

IMVP6 CPU VCore Regulator

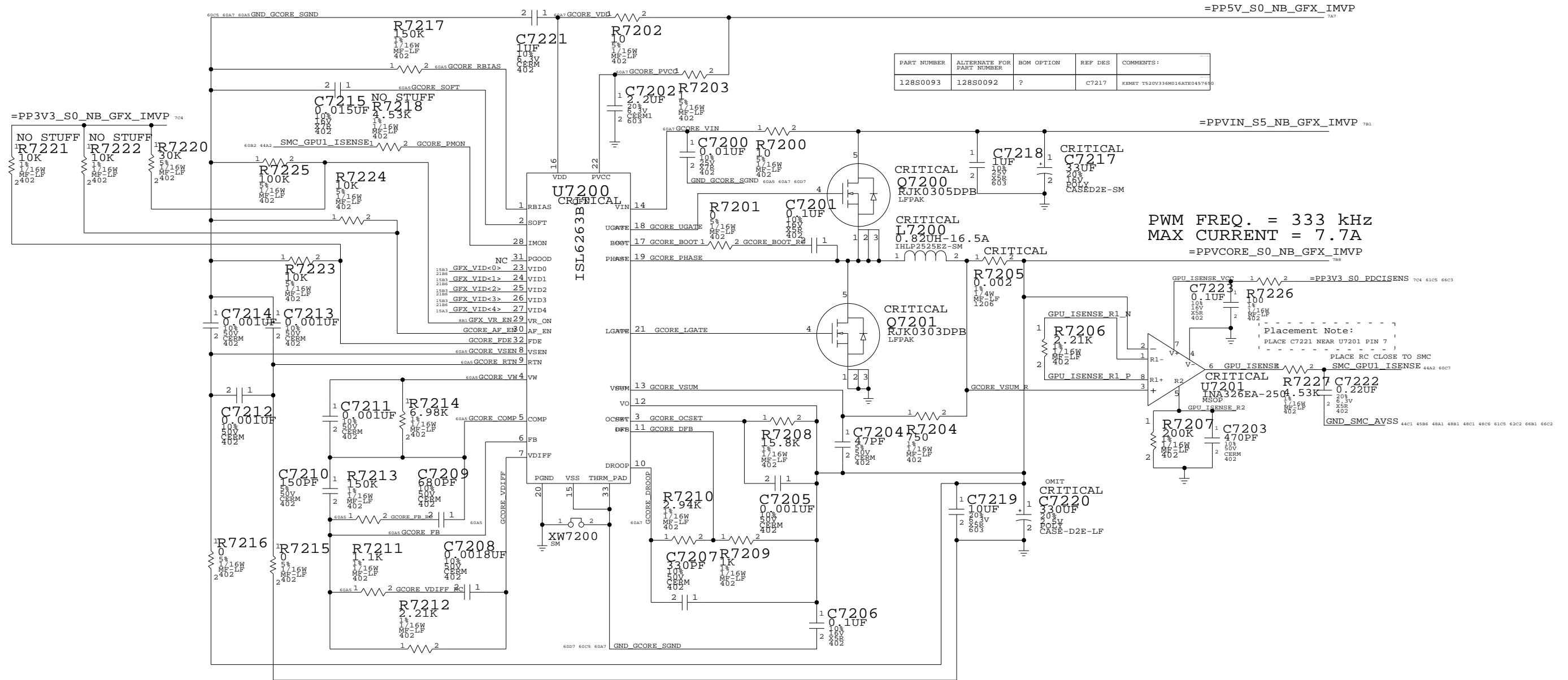
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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LATEST ISSUE: 2007/01/23

APPLE INC. DRAWING NUMBER: D 051-7455 REV. 01
SCALE: NONE SHEET: 59 OF 76

RENDER VCORE POWER SUPPLY



	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
60C5 GCORE_PHASE	1 MM	0.25 MM	489
60C5 GCORE_BOOT	0.3 MM	0.25 MM	494
60C5 GCORE_UGATE	1 MM	0.25 MM	495
60C5 GCORE_LGATE	1 MM	0.25 MM	496
60C5 GCORE_BOOT_RC	0.3 MM	0.25 MM	497
60C5 GND_CORE_SGND	0.6 MM	0.25 MM	498
60C5 GCORE_VDD	0.3 MM	0.25 MM	499
60D5 GCORE_PVCC	0.3 MM	0.25 MM	500
60C5 GCORE_VIN	0.3 MM	0.25 MM	501
60C5 GCORE_DROOP	0.3 MM	0.25 MM	502
60B5 GCORE_VSUM	0.3 MM	0.25 MM	503
60B5 GCORE_DFB	0.3 MM	0.25 MM	504

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
60B5 GCORE_OCSET	0.3 MM	0.25 MM	505
60B5 GCORE_VW	0.3 MM	0.25 MM	506
60B5 GCORE_RTN	0.3 MM	0.25 MM	507
60C5 GCORE_VSEN	0.3 MM	0.25 MM	508
60C5 GCORE_RBIAS	0.3 MM	0.25 MM	509
60C5 GCORE_SOFT	0.3 MM	0.25 MM	510
60C5 GCORE_COMP	0.3 MM	0.25 MM	511
60C5 GCORE_FB	0.3 MM	0.25 MM	512
60B5 GCORE_VDIFF	0.3 MM	0.25 MM	513
60B5 GCORE_FB_RC	0.3 MM	0.25 MM	514
60B5 GCORE_VDIFF_RC	0.3 MM	0.25 MM	515

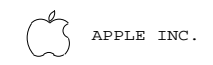
Render VCore Supplies

SYNC_MASTER=GPU SYNC_DATE=06/29/2006

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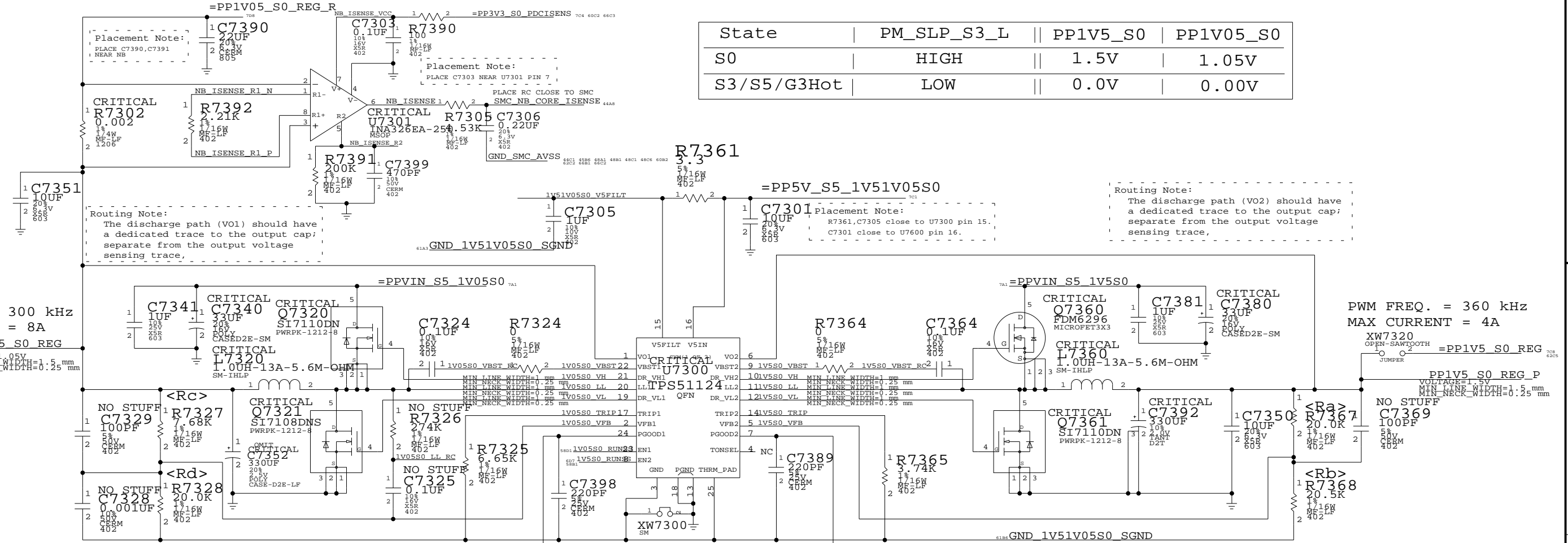
LATEST ISSUE: 2006/12/22



SCALE	SHT	OF	REV.
NONE	60	76	01

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



PWM FREQ. = 300 kHz
MAX CURRENT = 8A

PWM FREQ. = 360 kHz
MAX CURRENT = 4A

$$V_{out} = 0.758V * (1 + R_c / R_d)$$

$$V_{out} = 0.758V * (1 + R_a / R_b)$$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7380, C7340	KEMET T820V336M016AT8045740

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q7360	

LATEST ISSUE: 2006/12/22

APPLE INC.		DRAWING NUMBER D 051-7455	REV. 01
		SCALE NONE	SHEET 61 OF 76

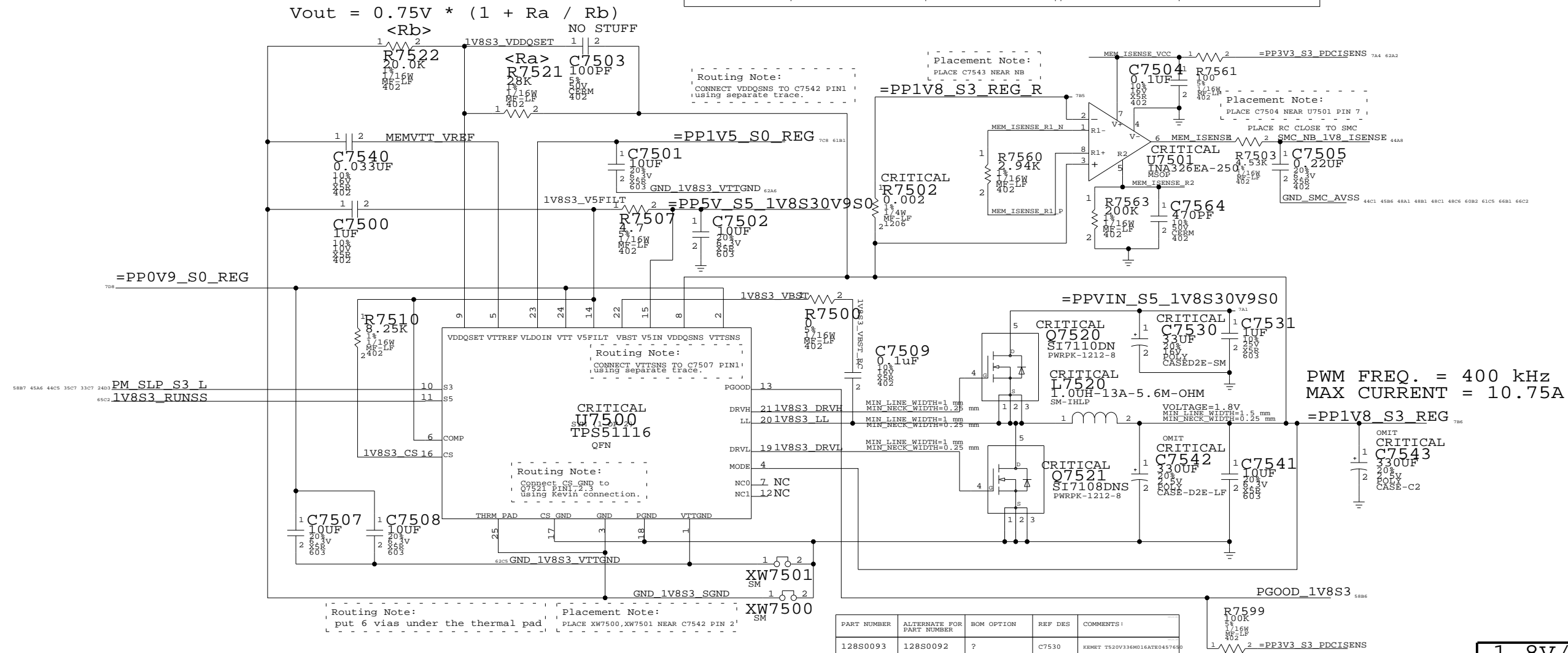
1.5V / 1.05V Supplies
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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1.8V/0.9V POWER SUPPLY

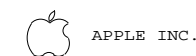
State	PM_SLP_S4	IPM_SLP_S3	IPP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V

$$V_{out} = 0.75V * (1 + \frac{R_a}{R_b})$$



PWM FREQ. = 400 kHz
MAX CURRENT = 10.75A

LATEST ISSUE: 2006/12/22



APPLE INC.

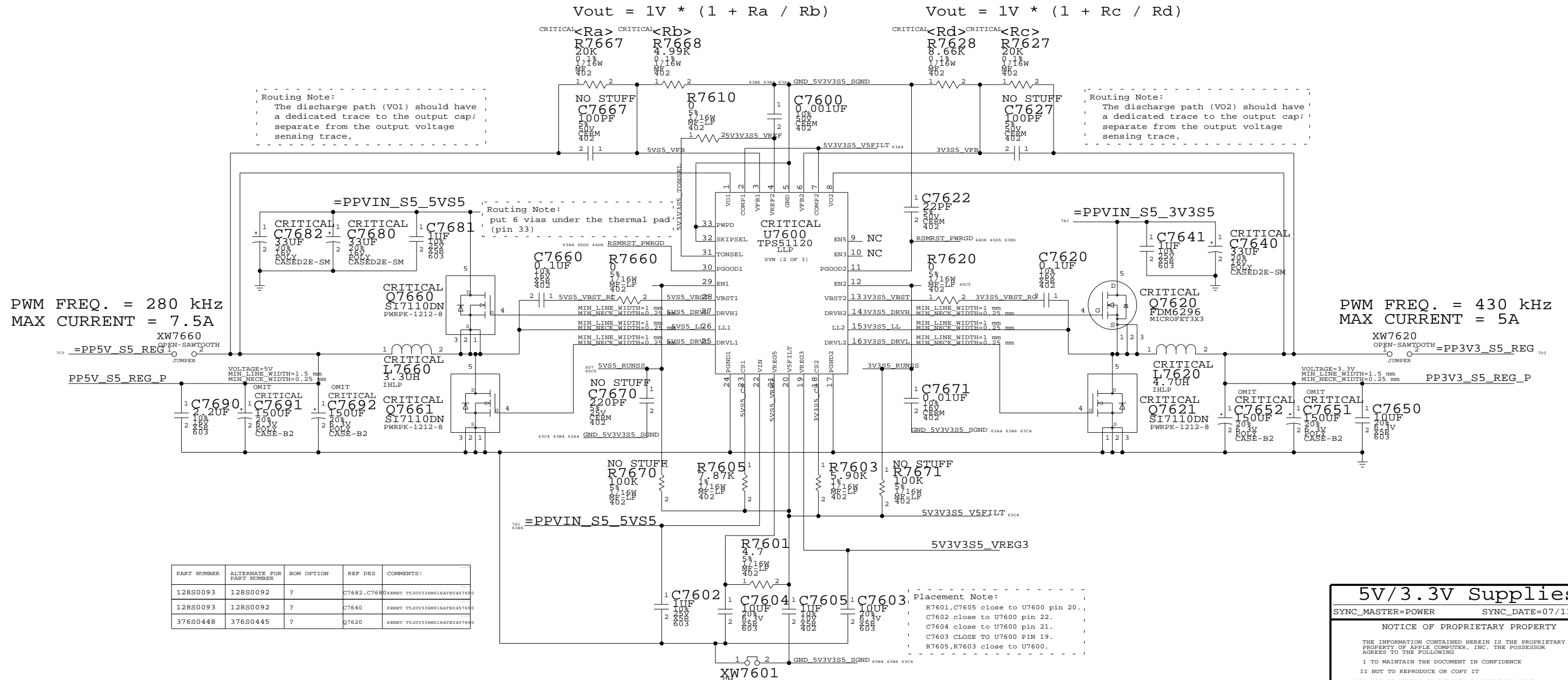
1.8V/0.9V Supplies		
SYNC_MASTER=POWER SYNC_DATE=07/13/2005		
NOTICE OF PROPRIETARY PROPERTY		
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SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	62	76

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

$$V_{out} = 1V * (1 + R_a / R_b)$$

$$V_{out} = 1V * (1 + R_c / R_d)$$



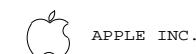
PWM FREQ. = 280 kHz
MAX CURRENT = 7.5A

PWM FREQ. = 430 kHz
MAX CURRENT = 5A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682, C7680	KEMET T520V336M016AT0457610
128S0093	128S0092	?	C7640	KEMET T520V336M016AT0457610
376S0448	376S0445	?	Q7620	KEMET T520V336M016AT0457610

Placement Note:
R7601, C7605 close to U7600 pin 20.
C7602 close to U7600 pin 22.
C7604 close to U7600 pin 21.
C7603 close to U7600 pin 19.
R7605, R7603 close to U7600.

LATEST ISSUE: 2006/12/22

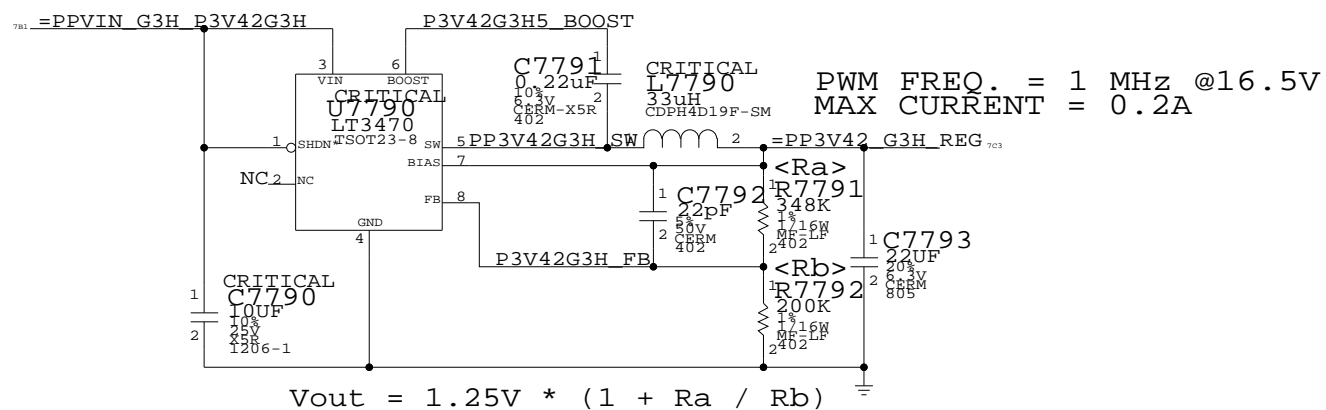


5V/3.3V Supplies
 SYNC_MASTER=POWER SYNC_DATE=07/13/2005
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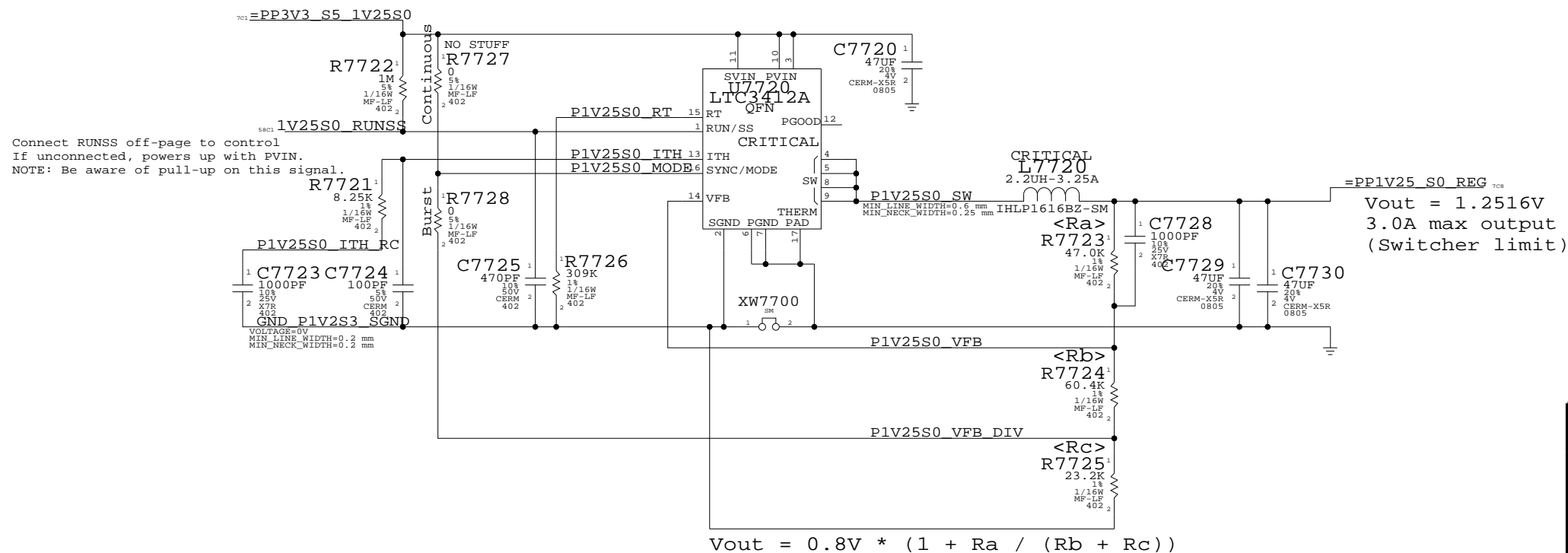
SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	63	76

3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.25V S0 REGULATOR



3.42V/1.25V Switcher

SYNC_MASTER=ENESYNC_DATE=12/06/2005

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LATEST ISSUE: 2007/3/8



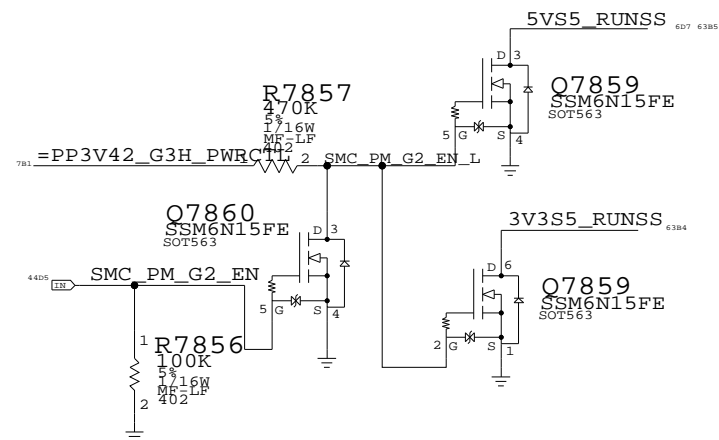
SIZE DRAWING NUMBER REV.

D 051-7455 01

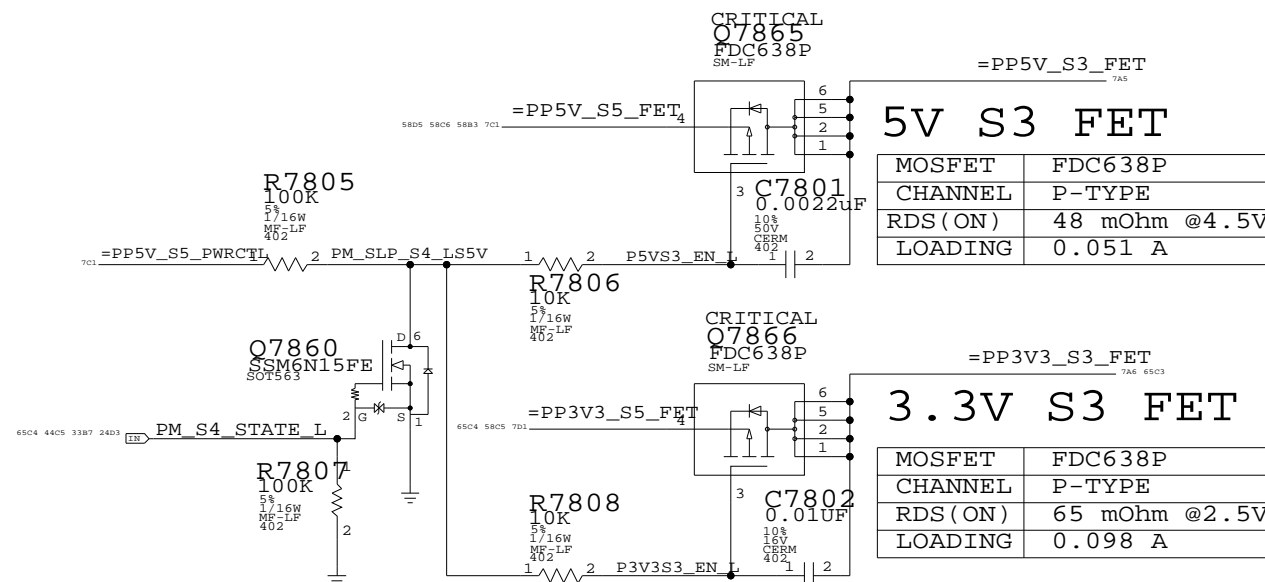
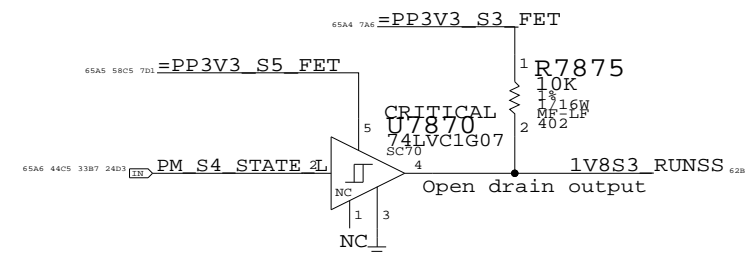
SCALE SHEET OF 64 OF 76

S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL



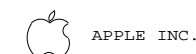
1.8V S3 RUN/SS CONTROL



S3 FET & S3/S5 Control
 SYNC_MASTER=DSIMON DATE=06/12/2006

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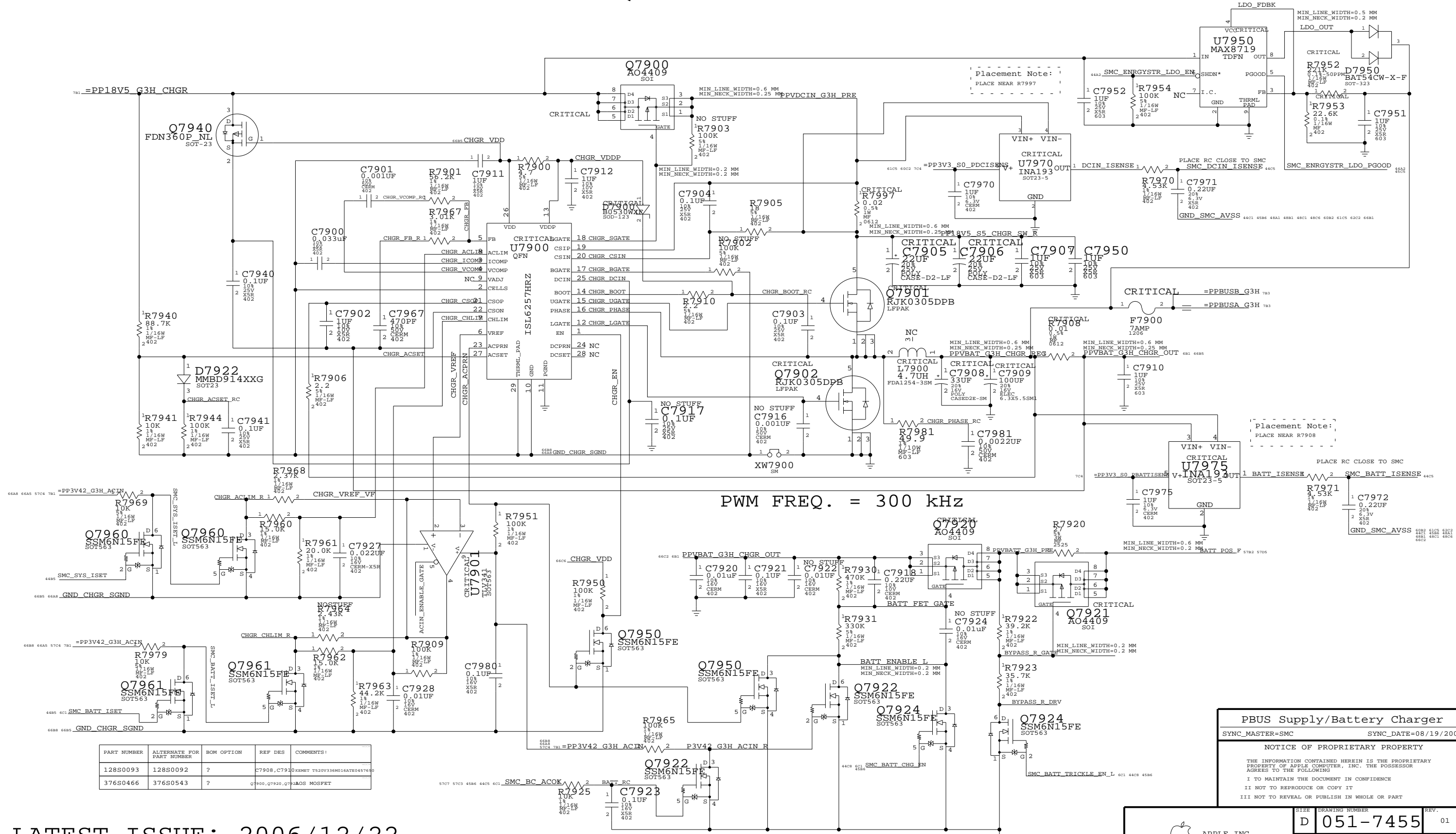
LATEST ISSUE: 2006/12/22



APPLE INC.

SIZE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
SCALE	SHT	OF
	65	76

PBUS SUPPLY / BATTERY CHARGER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7908, C7910	KEMET T520V336016ATE045760
376S0466	376S0543	?	Q7900, Q7920, Q7925	AOSS MOSFET

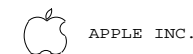
PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

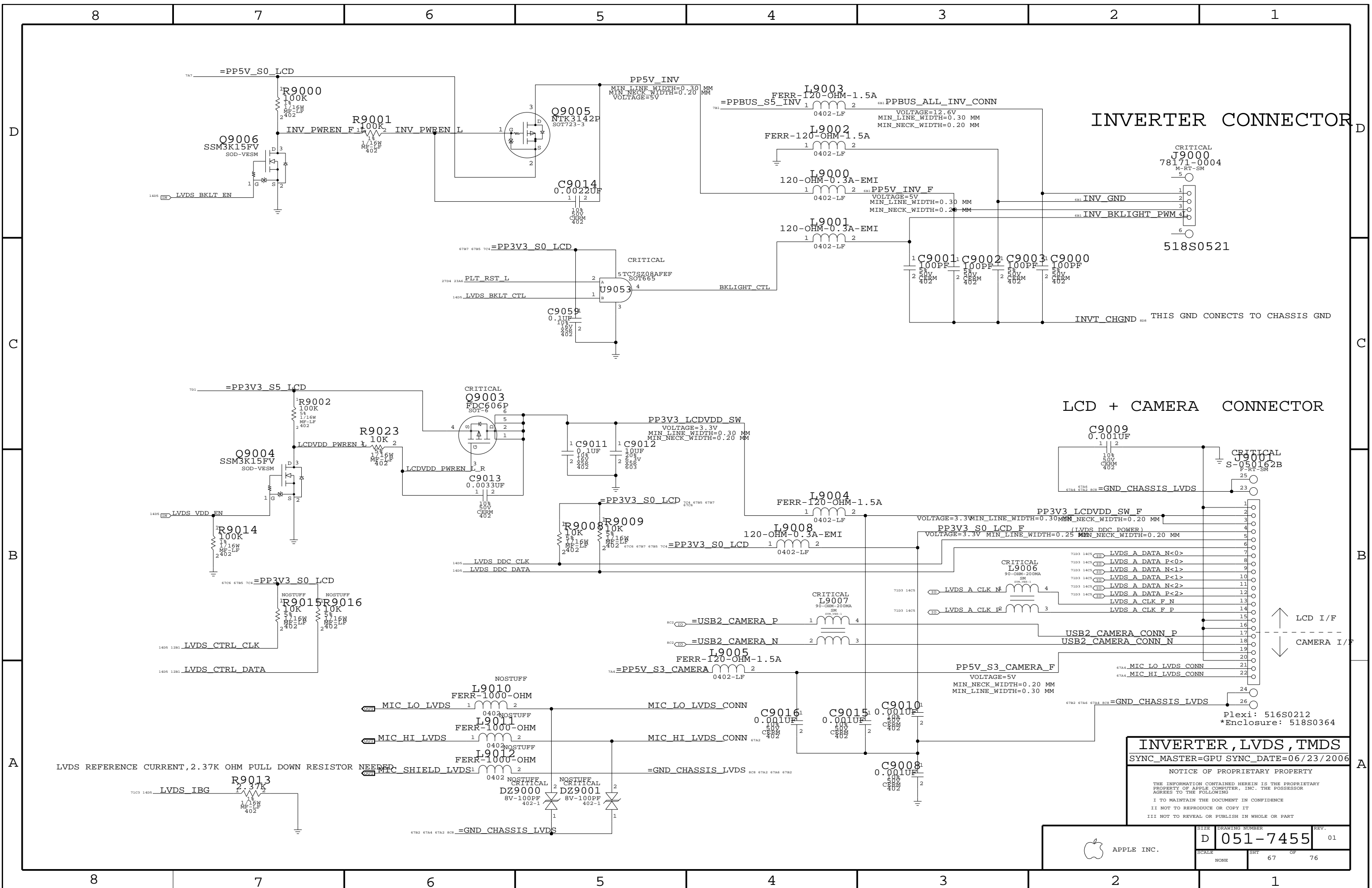
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LATEST ISSUE: 2006/12/22



SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHEET	OF
NONE	66	76



INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

INVERTER, LVDS, TMDS

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

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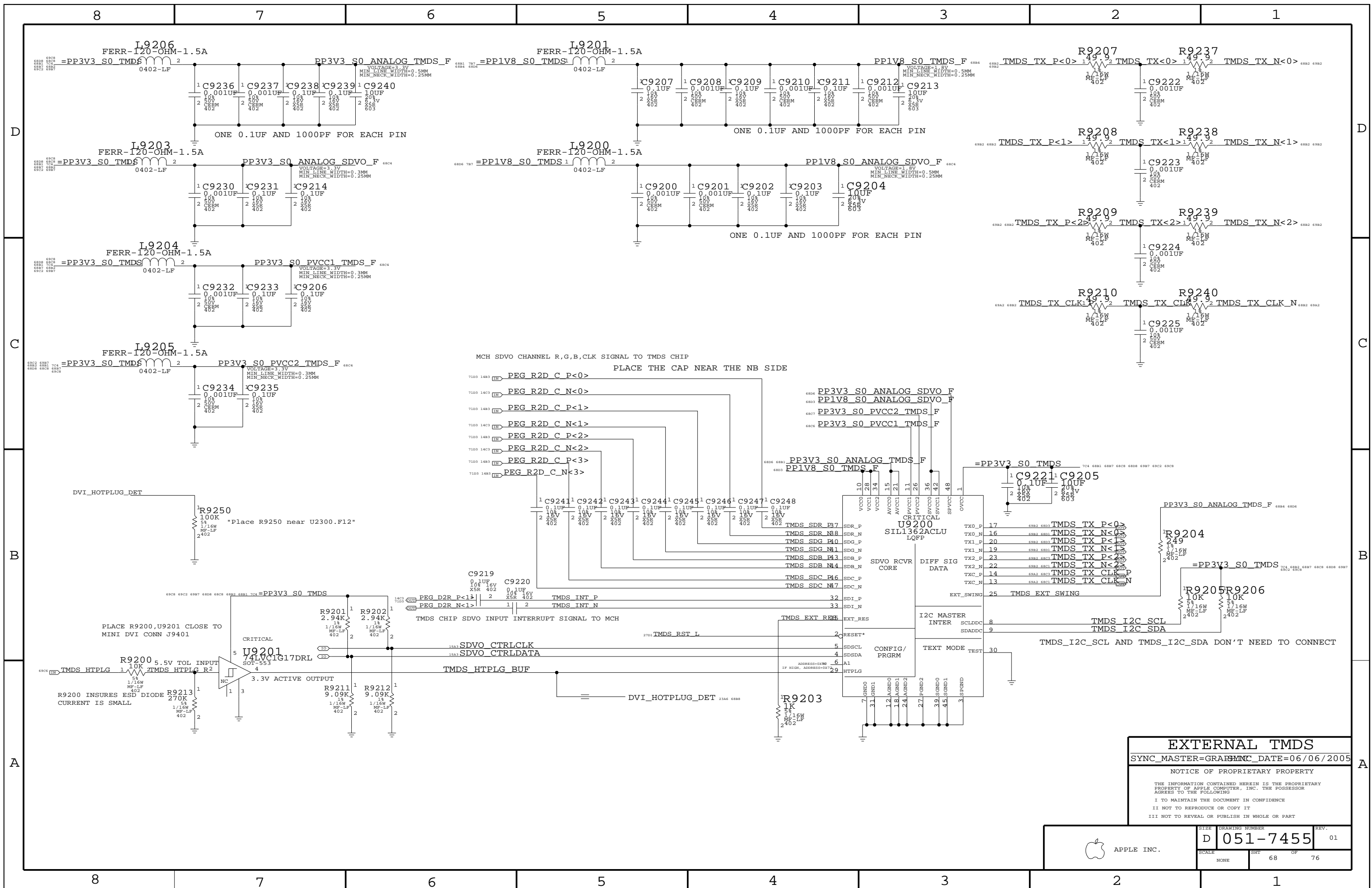
APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7455	REV.: 01
	SCALE: NONE	SHT: 67	OF: 76

LVDS REFERENCE CURRENT, 2.37K OHM PULL DOWN RESISTOR NEEDED

Plexi: 516S0212
*Enclosure: 518S0364

INVT_CHGND THIS GND CONNECTS TO CHASSIS GND

LCD I/F
CAMERA I/F



EXTERNAL TMSD
 SYNC_MASTER=GRABMNC_DATE=06/06/2005

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APPLE INC.	SCALE	SHEET	OF	REV.
	NONE	68	76	01

NB VIDEO ALIASES

1445	=CRT_TVO_IREF	CRT_TVO_IREF	1489 71C3	=CRT_BLUE	CRT_BLUE	6988 71C3
1445	=TV_A_DAC	TV_A_DAC	MAKE_BASE=TRUE 6988 71C3			
1485	=TV_B_DAC	TV_B_DAC	MAKE_BASE=TRUE 6988 71C3	=CRT_GREEN	CRT_GREEN	6988 71C3
1485	=TV_C_DAC	TV_C_DAC	MAKE_BASE=TRUE 6988 71C3			
1485	=CRT_RED	CRT_RED	MAKE_BASE=TRUE 6988 71C3			
1485	=CRT_HSYNC_R	CRT_HSYNC_R	69C3 71C3			
1445	=CRT_VSYNC_R	CRT_VSYNC_R	69C3 71C3			

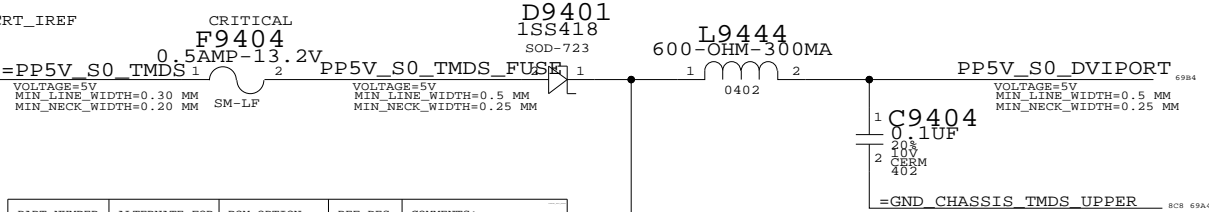
Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

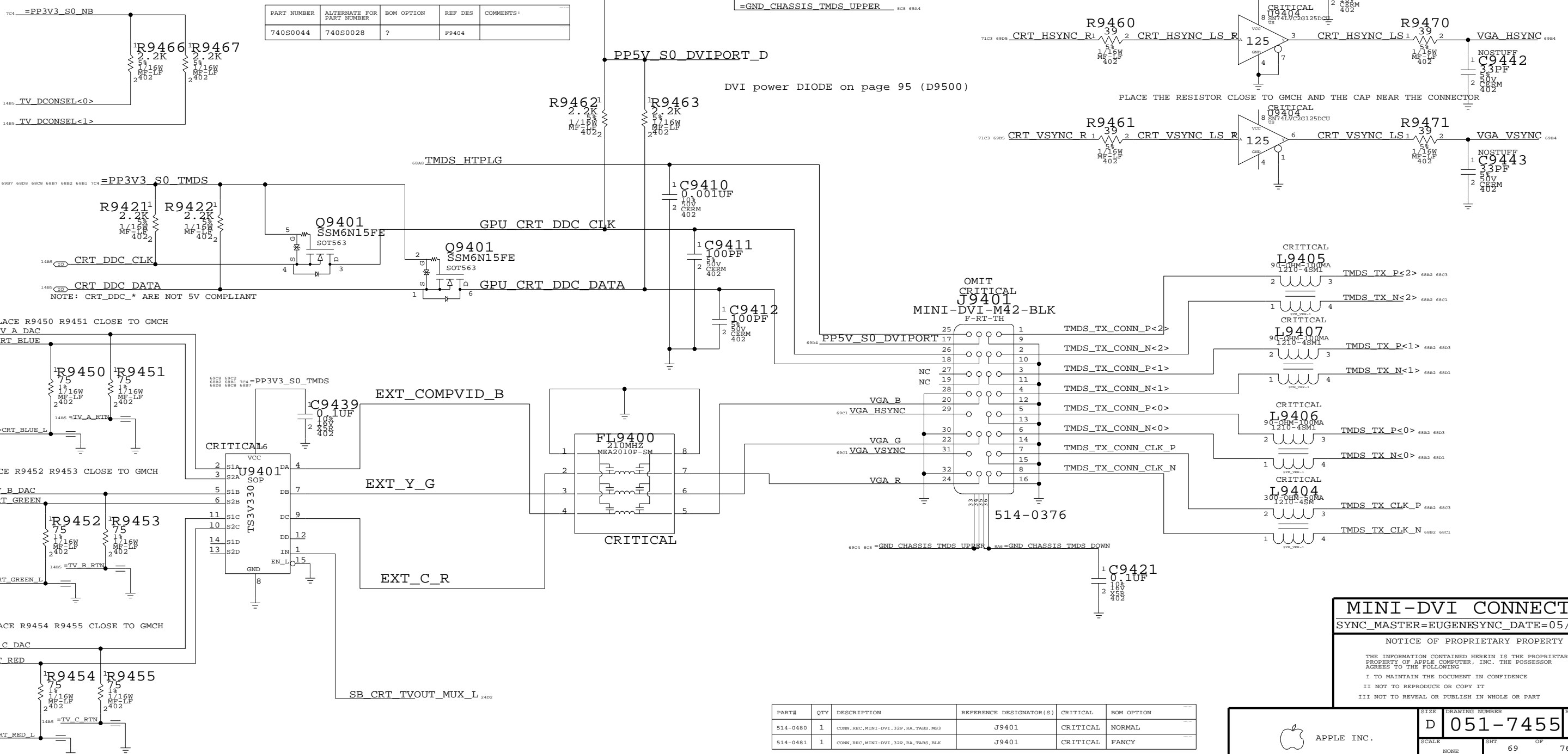
TMDS (MINI DVI) INTERFACE

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND



PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR



MINI-DVI CONNECTOR

SYNC_MASTER=EUGENESYNC_DATE=05/21/05

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SCALE	SHEET	OF	REV.
NONE	69	76	01

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BREQ0 L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	982 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	906 1303
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	906 1303
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	906 1286 1303
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	904 1305 1305
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	904 1303
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	904 1303
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	904 1303
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	984 904 1305
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	984 1303
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	984 1303
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	984 1303
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	902 1305 1305
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	902 1303
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	902 1303
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	902 1303
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	982 902 1305
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	982 1303
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	982 1303
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	982 1303
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	908 1303 1303
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	908 908 1303
FSB_ADSTR0	FSB_55S	FSB_ADSTR	FSB ADSTB L<0>	908 1303
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	908 1303
FSB_ADSTR1	FSB_55S	FSB_ADSTR	FSB ADSTB L<1>	908 1303
CPU_IERR_L	CPU_55S		CPU IERR L	906
CPU_FERR_L	CPU_55S		CPU FERR L	906 2202
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	906 4585 4503 5908
CPU_PWRGD	CPU_55S		CPU PWRGD	982 1281 2204
CPU_FROM_SB	CPU_55S		CPU INTR	988 2204
CPU_FROM_SB	CPU_55S		CPU NMI	988 2204
CPU_FROM_SB	CPU_55S		CPU A20M L	908 2204
CPU_FROM_SB	CPU_55S		CPU DPSLP L	982 2204
CPU_FROM_SB	CPU_55S		CPU IGNE L	908 2204
CPU_INIT_L	CPU_55S		CPU INIT L	906 2204 4682
CPU_FROM_SB	CPU_55S		CPU SMI L	988 2204
CPU_FROM_SB	CPU_55S		CPU_STPOLK L	988 2204
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	906 1506 2202 4583
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	902 1305
PM DPRSLPVR	CPU_55S	CPU_2T01	PM DPRSLPVR	1506 2403 5908
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	5907
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	984 2906
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	1506 2908
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	984 2906
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	1506 2908
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	984 2906
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	1506 2908
CPU DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	982 1506 2204 5907
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	984
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	983
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	983
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	983
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	983
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	987 906 1283
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	987 906 1285
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	987 906 1282
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	987 906 1282 1283
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	987 906 1283
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	906 1282 1283
XDP_BPM_LS	CPU_55S	CPU_ITP	XDP BPM L<5>	906 1282
CLK_FSB_1000	CLK_FSB_1000	CLK_FSB	XDP CLK P	7503
CLK_FSB_1000	CLK_FSB_1000	CLK_FSB	XDP CLK N	7503
(FSB_CPURST_L)	CPU_55S	CPU_ITP	ITP CPURST L	
CPU_55S	CPU_2T01	CPU_2T01	CPU VID<6..0>	1087 5907
CPU_55S	CPU_2T01	CPU_2T01	IMVP6_VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	1006 5904 5905
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	1006 5904 5905
CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE	IMVP6_VSEN P	
CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE	IMVP6_VSEN N	

CPU/FSB Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/08/2006

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SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE NONE SHEET 70 OF 76

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
 CRT & TVDAC signal single-ended impedance varies by location:
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.
 - 50-ohm +/- 15% from first to second termination resistor.
 - 55-ohm +/- 15% from second termination resistor to connector.
 CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG D2R N<1>	1403 6886
	PCIE_100D	PCIE	PEG D2R P<1>	1403 6886
	PCIE_100D	PCIE	PEG R2D_C P<3..0>	1403 6886 680C
	PCIE_100D	PCIE	PEG R2D_C N<3..0>	1403 1403 6886 680C
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>	1503 2302
	DMI_100D	DMI	DMI N2S N<3..0>	1503 2302
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>	1503 2302
	DMI_100D	DMI	DMI S2N N<3..0>	1503 1503 2302
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P	1405 6783
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N	1405 6783
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>	1405 6782
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>	1405 6782
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>	
LVDS_IBG		LVDS	LVDS_IBG	1405 6788
CRT_TVO_IREF		CRT	CRT TVO IREF	6907 6908
CRT_RED	CRT_50S	CRT	CRT RED	6908 6905
CRT_GREEN	CRT_50S	CRT	CRT GREEN	6908 6905
CRT_BLUE	CRT_50S	CRT	CRT BLUE	6908 6905
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R	6903 6905
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R	6903 6905
TV_A_DAC	CRT_50S	TVDAC	TV A DAC	6908 6907
TV_B_DAC	CRT_50S	TVDAC	TV B DAC	6908 6907
TV_C_DAC	CRT_50S	TVDAC	TV C DAC	6908 6907

NB Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK P<2..0>	1503 3004 3004
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK N<2..0>	1503 3004 3004
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	1503 3004 3006 3206
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_CS L<1..0>	1503 3004 3086 3206
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	1503 3004 3086 3206
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A A<14..0>	1506 1605 1605 3084 3086 3004 3006 3206
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A BS<2..0>	1605 3084 3086 3006 3206
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A RAS L	1605 3084 3206
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A CAS L	1605 3086 3206
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A WE L	1605 3086 3206
MEM_A_DO_BYTE0	MEM_55S	MEM_DATA	MEM_A DQ<7..0>	1608 3004 3006
MEM_A_DO_BYTE1	MEM_55S	MEM_DATA	MEM_A DQ<15..8>	1608 3004 3006
MEM_A_DO_BYTE2	MEM_55S	MEM_DATA	MEM_A DQ<23..16>	1608 3004 3006
MEM_A_DO_BYTE3	MEM_55S	MEM_DATA	MEM_A DQ<31..24>	1608 3004 3006 3004 3006
MEM_A_DO_BYTE4	MEM_55S	MEM_DATA	MEM_A DQ<39..32>	1608 1608 3084 3086
MEM_A_DO_BYTE5	MEM_55S	MEM_DATA	MEM_A DQ<47..40>	1608 3004 3006 3084 3086
MEM_A_DO_BYTE6	MEM_55S	MEM_DATA	MEM_A DQ<55..48>	1608 3004 3006
MEM_A_DO_BYTE7	MEM_55S	MEM_DATA	MEM_A DQ<63..56>	1608 1608 3004 3006
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A DM<0>	1605 3004
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A DM<1>	1605 3004
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A DM<2>	1605 3006
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A DM<3>	1605 3004
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A DM<4>	1605 3004
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A DM<5>	1605 3086
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A DM<6>	1605 3006
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A DM<7>	1605 3004
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A DQS P<0>	1605 3006
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A DQS N<0>	1605 3006
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DQS P<1>	1605 3006
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A DQS N<1>	1605 3006
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DQS P<2>	1605 3004
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A DQS N<2>	1605 3004
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DQS P<3>	1605 3006
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A DQS N<3>	1605 3006
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DQS P<4>	1605 3086
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A DQS N<4>	1605 3086
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DQS P<5>	1605 3084
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A DQS N<5>	1605 3084
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DQS P<6>	1605 3004
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A DQS N<6>	1605 3004
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DQS P<7>	1605 3006
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A DQS N<7>	1605 3006
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK P<5..3>	1503 3104 3104
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK N<5..3>	1503 3104 3104
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	1503 3104 3106 3206 3206
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_CS L<3..2>	1503 1503 3184 3186 3206
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	1503 3184 3186 3206
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B A<14..0>	1506 1601 1601 3184 3186 3104 3106 3206 3206
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B BS<2..0>	1601 3184 3186 3106 3206
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B RAS L	1601 3184 3206
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B CAS L	1601 3186 3206
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B WE L	1601 3186 3206
MEM_B_DO_BYTE0	MEM_55S	MEM_DATA	MEM_B DQ<7..0>	1604 3104 3106
MEM_B_DO_BYTE1	MEM_55S	MEM_DATA	MEM_B DQ<15..8>	1604 3104 3106
MEM_B_DO_BYTE2	MEM_55S	MEM_DATA	MEM_B DQ<23..16>	1604 3104 3106
MEM_B_DO_BYTE3	MEM_55S	MEM_DATA	MEM_B DQ<31..24>	1604 3104 3106
MEM_B_DO_BYTE4	MEM_55S	MEM_DATA	MEM_B DQ<39..32>	1604 1604 3184 3186
MEM_B_DO_BYTE5	MEM_55S	MEM_DATA	MEM_B DQ<47..40>	1604 3104 3106 3184 3186
MEM_B_DO_BYTE6	MEM_55S	MEM_DATA	MEM_B DQ<55..48>	1604 3104 3106
MEM_B_DO_BYTE7	MEM_55S	MEM_DATA	MEM_B DQ<63..56>	1604 1604 3104 3106
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B DM<0>	1601 3104
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B DM<1>	1601 3104
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B DM<2>	1601 3104
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B DM<3>	1601 3106
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B DM<4>	1601 3184
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B DM<5>	1601 3106
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B DM<6>	1601 3104
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B DM<7>	1601 3106
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B DQS P<0>	1601 3106
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B DQS N<0>	1601 3106
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DQS P<1>	1601 3106
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B DQS N<1>	1601 3106
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DQS P<2>	1601 3106
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B DQS N<2>	1601 3106
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DQS P<3>	1601 3104
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B DQS N<3>	1601 3104
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DQS P<4>	1601 3186
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B DQS N<4>	1601 3186
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DQS P<5>	1601 3104
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B DQS N<5>	1601 3104
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DQS P<6>	1601 3106
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B DQS N<6>	1601 3106
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DQS P<7>	1601 3104
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B DQS N<7>	1601 3104

Memory Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/08/2006

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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	2284 2204 3903 3905
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	2284 3983 3985
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L	2284 3986
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3 L	2284 3987
IDE_PDIOW	IDE_55S	IDE	IDE_PDIOW L	2284 3988
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR L	2284 3989
IDE_PDDACK	IDE_55S	IDE	IDE_PDDACK L	2284 3993
IDE_PDDRQ	IDE_55S	IDE	IDE_PDDRQ	2284 3993
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	2284 3995
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	2284 3995
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L	2286 39A8
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	2286 40D4
SATA_100D	SATA_100D	SATA	SATA_A_R2D_C_N	2286 40D4
SATA_100D	SATA_100D	SATA	SATA_A_R2D_P	40C7
SATA_100D	SATA_100D	SATA	SATA_A_R2D_N	40D7
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	2286 40D4
SATA_100D	SATA_100D	SATA	SATA_A_D2R_N	2286 40D4
SATA_100D	SATA_100D	SATA	SATA_A_D2R_C_P	40C7
SATA_100D	SATA_100D	SATA	SATA_A_D2R_C_N	40D7
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	8A6 2208
HDA_55S	HDA_55S	HDA	HDA_BIT_CLK_R	2208
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	8A6 2208
HDA_55S	HDA_55S	HDA	HDA_SYNC_R	2208
HDA_RST_L	HDA_55S	HDA	HDA_RST L	8A6 2208
HDA_55S	HDA_55S	HDA	HDA_RST L R	2208
HDA_SDINO	HDA_55S	HDA	HDA_SDINO	8A6 2208
HDA_SDOUPT	HDA_55S	HDA	HDA_SDOUPT	8A6 2288
HDA_55S	HDA_55S	HDA	HDA_SDOUPT_R	2288
USB_EXT_A	USB_90D	USB	USB_EXT_A_P	8C1 2302
USB_90D	USB_90D	USB	USB_EXT_A_N	8C1 2302
USB_90D	USB_90D	USB	USB_EXT_A_MUXED_P	
USB_90D	USB_90D	USB	USB_EXT_A_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	8C1 2302
USB_90D	USB_90D	USB	USB_MINI_N	8C1 2302
USB_3G	USB_90D	USB	USB_3G_P	
USB_90D	USB_90D	USB	USB_3G_N	
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	8C1 2302
USB_90D	USB_90D	USB	USB_CAMERA_N	8C1 2302
USB_BT	USB_90D	USB	USB_BT_P	8C1 8C2 2302
USB_90D	USB_90D	USB	USB_BT_N	883 882 2302
USB_TPAD	USB_90D	USB	USB_TPAD_P	8C1 2302
USB_90D	USB_90D	USB	USB_TPAD_N	8C1 2302
USB_IR	USB_90D	USB	USB_IR_P	8C1 8C2 2302
USB_90D	USB_90D	USB	USB_IR_N	8C1 8C2 2302
USB_EXTB	USB_90D	USB	USB_EXTB_P	881 2302
USB_90D	USB_90D	USB	USB_EXTB_N	881 2302
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	881 2302
USB_90D	USB_90D	USB	USB_EXCARD_N	881 2302
USB_EXTC	USB_90D	USB	USB_EXTC_P	881 2302
USB_90D	USB_90D	USB	USB_EXTC_N	881 2302
USB_RBIA5	USB_60S	USB	USB_RBIA5	23A3
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	2405 47D8
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	2405 47D8
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	2405 47A8
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	2405 47A8
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	2305 52C7
SPI_55S	SPI_55S	SPI	SPI_A_SCLK_R	52C5
SPI_ST	SPI_55S	SPI	SPI_ST_R	2305 52C3
SPI_55S	SPI_55S	SPI	SPI_A_ST_R	52C4
SPI_SO	SPI_55S	SPI	SPI_SO	2305 52C3
SPI_55S	SPI_55S	SPI	SPI_A_SO_R	52C4
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	2305 52C7
SPI_55S	SPI_55S	SPI	SPI_CE_L<0>	52C5
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	Y	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	23A8 23B8 37B5 37C5
PCI_AD19	PCI_55S	PCI	PCI AD<19>	23A8 37B6
PCI_AD20	PCI_55S	PCI	PCI AD<20>	23A8 37B5
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	23A8 37B5
PCI_AD	PCI_55S	PCI	PCI PAR	23A6 37B5
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	23B6 37B5
PCI_CNTL	PCI_55S	PCI	PCI IRDY_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI DEVSEL_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI PERR_L	23A4 23A6 37A5
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	23A4 23A6
PCI_CNTL	PCI_55S	PCI	PCI SERR_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI STOP_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI TRDY_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI FRAME_L	23A4 23A6 37A5
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	23A4 23B6 37A5
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	23B5 37A5
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	23A4 23B6
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	23A4 23B6
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	
INT_PIROA_L	PCI_55S	PCI	INT PIROA_L	23A4 23A8
INT_PIROB_L	PCI_55S	PCI	INT PIROB_L	23A4 23A8
INT_PIROC_L	PCI_55S	PCI	INT PIROC_L	23A4 23A8
INT_PIROD_L	PCI_55S	PCI	INT PIROD_L	23A4 23A8 37A5
INT_PIROE_L	PCI_55S	PCI	INT PIROE_L	23A4 23A6
INT_PIROF_L	PCI_55S	PCI	INT PIROF_L	23A4 23A6
PCIE_E_R2D	PCIE_100D	PCIE	PCIE_E R2D C P	33B5 33B6
PCIE_E_R2D	PCIE_100D	PCIE	PCIE_E R2D C N	33B5 33B6
PCIE_E_D2R	PCIE_100D	PCIE	PCIE_E D2R P	33B5
PCIE_E_D2R	PCIE_100D	PCIE	PCIE_E D2R N	33B5 33C5
GLAN_COMP			GLAN_COMP	22C5
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC	
ENET_LAN	LAN_55S	ENET_LAN	LAN R2D<2..0>	
ENET_LAN	LAN_55S	ENET_LAN	LAN D2R<2..0>	
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK R	
LAN_55S	ENET_CLK		ENET_GLAN_CLK	
ENET_MDI0	ENET_100D	ENET_MDI	ENET MDI P<0>	34B8 36B7
ENET_100D	ENET_MDI		ENET MDI N<0>	34B8 36B7
ENET_MDI1	ENET_100D	ENET_MDI	ENET MDI P<1>	34B8 36C7
ENET_100D	ENET_MDI		ENET MDI N<1>	34B8 36C7
ENET_MDI2	ENET_100D	ENET_MDI	ENET MDI P<2>	34B8 36B7
ENET_100D	ENET_MDI		ENET MDI N<2>	34B8 36C7
ENET_MDI3	ENET_100D	ENET_MDI	ENET MDI P<3>	34B8 36C7
ENET_100D	ENET_MDI		ENET MDI N<3>	34B8 36C7
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	15A3 24C3
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	15A3 24C3
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET L	15A3 24C3
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	24C3
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	24C3
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET L	24C3
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	15A4
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	24C3
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	24C3

SB Constraints (2 of 2)

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

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SCALE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
SHEET	74	OF 76

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

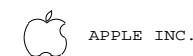
ELECTRICAL_CONSTRAINT_SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	6C7 28C4 29D6
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	6C7 28C4 29D6
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	6C7 28C4 29D6
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	6C7 28C4 29D6
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	6C7 28C4 29D6
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	6C7 28C4 29D6
CK505_PCIE0	CLK_MED_55S	CLK_MED	CK505_PCIE0_CLK	2886 2986
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	6C7 2886 2986
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	2886 2986
CK505_PCIE2	CLK_MED_55S	CLK_MED	CK505_PCIE2_CLK	8C4 2886
CK505_PCIE3	CLK_MED_55S	CLK_MED	CK505_PCIE3_CLK	2886 2986
CK505_PCIE4	CLK_MED_55S	CLK_MED	CK505_PCIE4_CLK	8C4 2886
CK505_PCIE5	CLK_MED_55S	CLK_MED	CK505_PCIE5_FCTSEL1	2886 2982
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_USB48_FSA	28A4 29D8
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_CLK14P3M_TIMER	28A4 29D8
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	6C7 28A4 2986
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	6C7 28A4 2986
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	6C7 2884 29C6
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	6C7 2884 29C6
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	6C7 2884 29C6
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	6C7 2884 29C6
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	6C7 2884 29C6
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	6C7 2884 29C6
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	6C7 2884 29C6
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	6C7 2884 29C6
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	6C7 2884 29C6
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	6C7 2884 2986
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	6B7 28A4 2986
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	6B7 28A4 2986
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	986 29D3
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	986 29D3
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	1383 29D3
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	1383 29D3
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	70A3
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	70A3
(CK505_PCIE0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6C2 29B3 46C4
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	21A6 29A5 29B3
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	29A5 29B3 37A5
(CK505_PCIE2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCIE3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	29A3 29A5 44C8
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_PCI4 is project-specific	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	24D3 29A5 29D6
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	24D3 29A5 29D6
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	29C8 29D6
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	29A8 29D6
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	8B1 29B3
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	8B1 29B3
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	8B1 29C3
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	8A1 29C3
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	23C2 29C3
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	23D2 29C3
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	2286 29C3
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	2286 29C3
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	15C3 29C3
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	15C3 29C3
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29C3 33C5
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29A3 33C5
			CK505_SRC7 is project-specific	
			CK505_SRC8 is project-specific	

Clock Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

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NONE	051-7455	01
SCALE	SHT	OF
NONE	75	76

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
EW_D_CTL	EW_55S	FW	FW LINK<7..0>
EW_D_CTL	EW_55S	FW	FW CTL<1..0>
EW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
EW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK
EW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK
EW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK
EW_LKON	EW_55S	FW	FW LKON
EW_LKON	EW_55S	FW	FW LKON R
EW_LPS	EW_55S	FW	FW LPS
EW_LREQ	EW_55S	FW	FW LREQ
EW_PINT	EW_55S	FW	FW PINT
EWPHY_CLK98P304M_XT	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
EWPHY_CLK98P304M_XT	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
EW_0_TPA	EW_110D	EW_TP	FW 0 TPA P
EW_0_TPA	EW_110D	EW_TP	FW 0 TPA N
EW_0_TPB	EW_110D	EW_TP	FW 0 TPB P
EW_0_TPB	EW_110D	EW_TP	FW 0 TPB N
EW_1_TPA	EW_110D	EW_TP	FW 1 TPA P
EW_1_TPA	EW_110D	EW_TP	FW 1 TPA N
EW_1_TPB	EW_110D	EW_TP	FW 1 TPB P
EW_1_TPB	EW_110D	EW_TP	FW 1 TPB N
Port 2 Not Used			

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 4702
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 4702
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 682 4705
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 682 4705
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 4705
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 4705
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 4702
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 4702
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 4782
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 4782

FireWire & SMC Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

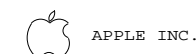
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