

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Sully

M9 MLB
3/3/2006

DVT
(6.0.0)

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

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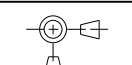
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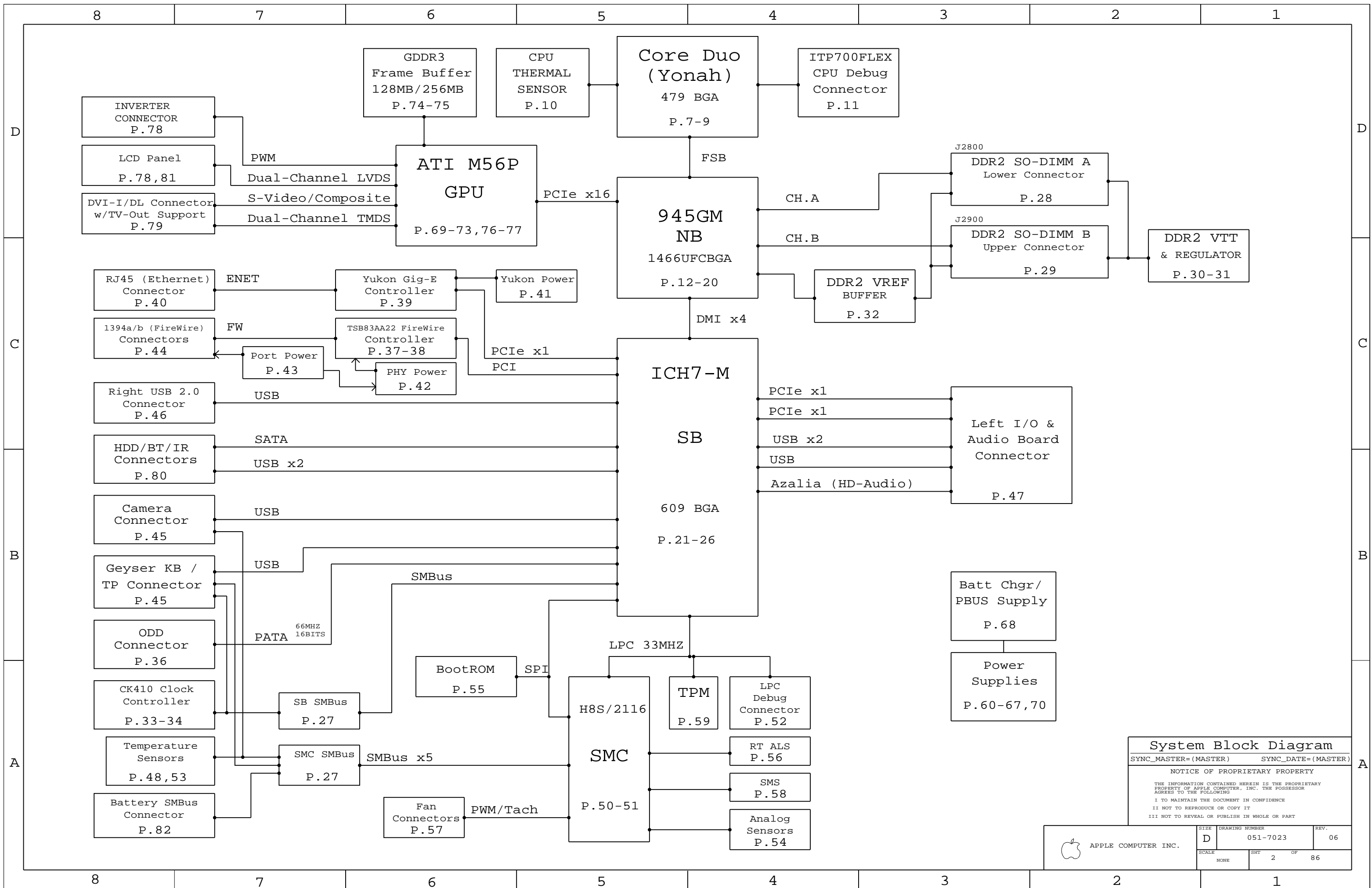
ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7023	1	SCHEM, SULLY, M9	SCH	CRITICAL	
820-2023	1	PCBF, SULLY, FINAL, M9	PCB	CRITICAL	

DRAWING
TITLE=SULLY
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 3 17:59:45 2006

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	
 THIRD ANGLE PROJECTION		DRAWING NUMBER		REV.	
		051-7023		06	
		SHT 1		OF 86	

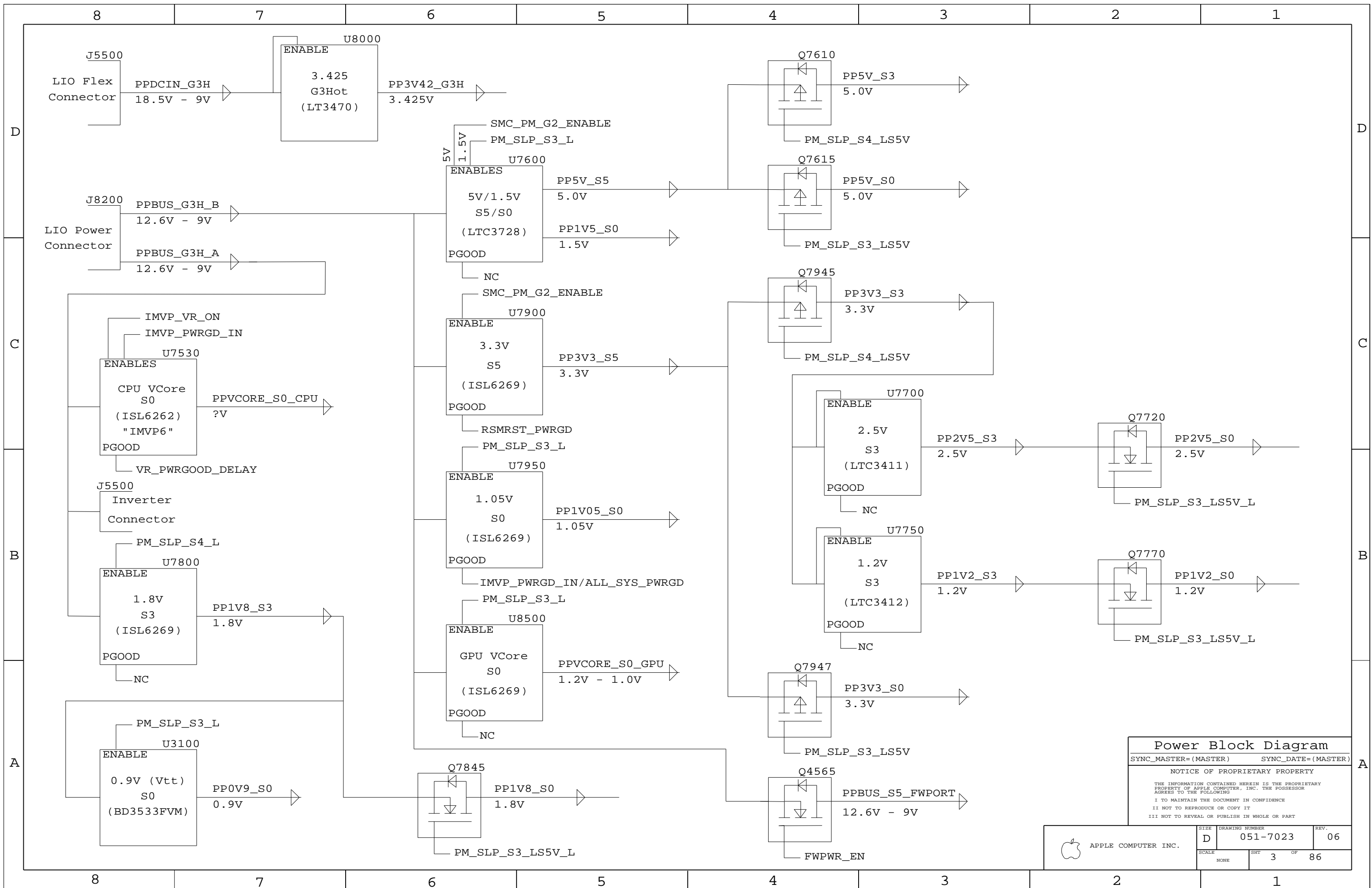


System Block Diagram

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT		OF
NONE	2		86



Power Block Diagram
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NONE	3	86	

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7404	PCBA, SULLY, 2.0GHz, M9	VRAM_256SAM, M9_COMMON, CPU_2_0GHZ, EEE_UNZ
630-7406	PCBA, SULLY, 2.16GHz, M9	VRAM_256SAM, M9_COMMON, CPU_2_16GHZ, EEE_UP1

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M, VRAM_256_SAMSUNG
VRAM_128HY	GPU_MEM_HYNIX, VRAM_128_HYNIX
VRAM_256HY	GPU_MEM_HYNIX, GPU_MEM_256M, VRAM_256_HYNIX

BOM GROUP	BOM OPTIONS
M9_COMMON	ALTERNATE, COMMON, M9_COMMON1, M9_COMMON2, M9_COMMON3, M9_COMMON4, M9_DEBUG
M9_COMMON1	ENET_LOM_DISABLE, ENETPWR_S3AC, GPUTHM_A_GPU, GPU_BB_CTL, HSTHMSNS_HAS, INVERTER_BUF, ONEWIRE_PU
M9_COMMON2	KBDLED_HAS, MEMVREF_S3, MEMVTT_EN_PU, RTUSB_ESD, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU
M9_COMMON3	LVDS_PD, M56_REV_B24_LP, FW_B_BILINGUAL, FW_A_DS_ONLY, FW_PORT_FAULT_PU, FW_PLTRST_UNGATED
M9_COMMON4	LIO_TEMP, BOOTROM_DEVEL, SMC_DEVEL
M9_DEBUG	ITP, ITPCONN, LPCPLUS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC, 8888053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC, SMC, HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1876	1	IC, SMC, PRGRM, M9	U5800	CRITICAL	SMC_DEVEL
341S1876	1	IC, SMC, PRGRM, M9	U5800	CRITICAL	SMC_FINAL
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL	
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1828	1	IC, EFI, BOOTROM DEVELOPMENT, M9	U6301	CRITICAL	BOOTROM_DEVEL
341S1829	1	IC, EFI, BOOTROM FINAL, M9	U6301	CRITICAL	BOOTROM_FINAL
353S1235	1	IC, CPU VOLTAGE REGULATOR, IMVP, TWO PHASE	U7530	CRITICAL	
359S0101	1	IC, CY28445-5, CLOCK GEN, 68PIN QFN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3282	1	IC, CPU, 479 BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC, CPU, 479 BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC, CPU, 479 BGA	U0700	CRITICAL	CPU_2_16GHZ
338S0269	1	IC, 945GM, SOUTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC, SB, 652BGA	U2100	CRITICAL	

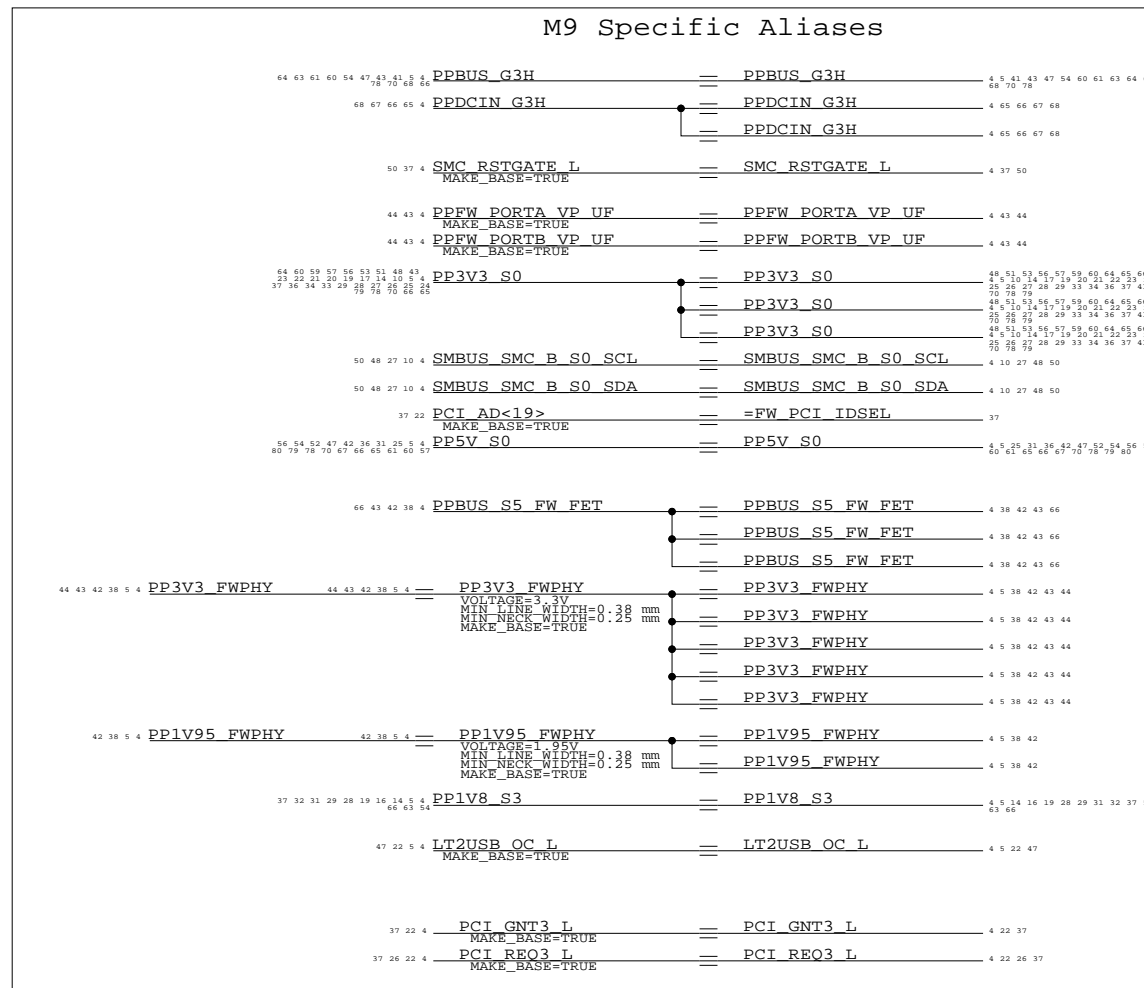
Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:UNZ]	CRITICAL	EEE_UNZ
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:UP0]	CRITICAL	EEE_UP0
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:UP1]	CRITICAL	EEE_UP1
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:UP2]	CRITICAL	EEE_UP2
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:UYU]	CRITICAL	EEE_UYU

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0266	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF	U8400	CRITICAL	M56_REV_B24_LL
338S0302	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF	U8400	CRITICAL	M56_REV_B24_HL
338S0309	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF	U8400	CRITICAL	M56_REV_B24_LP
338S0315	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF	U8400	CRITICAL	M56_REV_B26_LP
338S0316	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LF	U8400	CRITICAL	M56_REV_B26_P
333S0354	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0309	338S0266	M56_REV_B24_LL	U8400	LP is alt to LL
338S0266	338S0309	M56_REV_B24_LP	U8400	LL is alt to LP
338S0315	338S0309	M56_REV_B24_LP	U8400	B26_LP is alt to B24_LP
376S0448	376S0445		ALL	Vishay 2nd source
128S0083	128S0073		C2516	1.86 max alt to 1.9 max
128S0093	128S0092		ALL	Kemet is alt to Sanyo
128S0060	128S0094		ALL	Sanyo is alt to Panasonic
128S0095	128S0094		ALL	330uF, 2V, 6MOHM, D2
128S0081	128S0061		ALL	C2 package is alt to C3



BOM Configuration

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE	SHT	OF
NONE	4	86

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA
TRUE	IMVP6_RBIAS
TRUE	P5VS5_RUNSS
TRUE	P1V5S0_RUNSS
TRUE	P2V5S3_MODE
TRUE	P2V5S3_SHDNRT
TRUE	P1V2S3_RT
TRUE	P1V2S3_RUNSS
TRUE	P1V8S3_COMP
TRUE	P1V8S3_FSET
TRUE	P3V3S5_COMP
TRUE	P3V3S5_FSET
TRUE	P1V0S0_COMP
TRUE	P1V0S0_FSET
TRUE	P3V42G3H_FB
TRUE	GPUVCORE_COMP
TRUE	GPUVCORE_FSET
TRUE	GPUBBP_ADJ

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA
TRUE	FSB_A_L<31..3>
TRUE	FSB_ADS_L
TRUE	FSB_ADSTB_L<1..0>
TRUE	FSB_BNR_L
TRUE	FSB_BREQ0_L
TRUE	FSB_D_L<63..0>
TRUE	FSB_DBSY_L
TRUE	FSB_DINV_L<3..0>
TRUE	FSB_DRDY_L
TRUE	FSB_DSTBN_L<3..0>
TRUE	FSB_DSTBP_L<3..0>
TRUE	FSB_HIT_L
TRUE	FSB_HITM_L
TRUE	FSB_LOCK_L
TRUE	FSB_REQ_L<4..0>

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA	
TRUE	DMI_N2S_P<1..0>
TRUE	DMI_N2S_N<1..0>
TRUE	SB_CLK100M_SATA_P
TRUE	SB_CLK100M_SATA_N

Power Nets

FUNC_TEST	
TRUE	PP0V9_S0
TRUE	PP1V05_S0
TRUE	PP1V2_S0
TRUE	PP1V2_S3
TRUE	PP1V5_S0
TRUE	PP1V8_S0
TRUE	PP1V8_S3
TRUE	PP2V5_S0
TRUE	PP2V5_S3
TRUE	PP3V3_S0
TRUE	PP3V3_S3
TRUE	PP3V3_S5
TRUE	PP5V_S0
TRUE	PP5V_S5
TRUE	PPBUS_G3H
TRUE	GND

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST	
TRUE	IMVP_VR_ON
TRUE	IMVP_DPRSLEVR
TRUE	PM_SLP_S3_L
TRUE	PM_SLP_S3BATT
TRUE	PM_SLP_S4_L
TRUE	PM_SLP_S5_L
TRUE	P1V5P1V05S0_PGOOD
TRUE	CPU_DPRSTP_L
TRUE	IMVP6_VID<6..0>
TRUE	FSB_CLK_CPU_N
TRUE	FSB_CLK_CPU_P
TRUE	PLT_RST_L
TRUE	PLT_RST_L
TRUE	PEG_RESET_L
TRUE	SMC_LRESET_L
TRUE	TPM_LRESET_L
TRUE	CPU_STPCLK_L
TRUE	FSB_CLK_NB_P
TRUE	FSB_CLK_NB_N
TRUE	CLK_NB_OE_L
TRUE	NB_CLK100M_GCLKIN_P
TRUE	NB_CLK100M_GCLKIN_N
TRUE	GND
TRUE	GND
TRUE	GND
TRUE	CPU_THERMTRIP_R
TRUE	TP_SB_SUS_CLK

MAC-1 TPs

FUNC_TEST	
TRUE	CPU_PWRGD
TRUE	TP_CPU_CPUSLP_L
TRUE	PM_DPRSLEVR
TRUE	CPU_DPSLP_L
TRUE	PM_LAN_ENABLE
TRUE	PCI_RST_L
TRUE	PM_RSMRST_L
TRUE	PM_SB_PWROK
TRUE	SB_RTC_RST_L
TRUE	PM_STPCPU_L
TRUE	PM_STPPCI_L
TRUE	VR_PWRGD_CK410
TRUE	VR_PWRGD_DELAY
TRUE	FSB_CPURST_L
TRUE	FSB_SLP_CPU_L
TRUE	FSB_DPWR_L
TRUE	NB_SB_SYNC_L
TRUE	PP2V5_S0_GPU_TPVDD
TRUE	PP2V5_S0_GPU_TXVDDR
TRUE	PP2V5_S0_GPU_AVDD
TRUE	PP2V5_S0_GPU_A2VDD
TRUE	PP2V5_S0_GPU_LPVDD
TRUE	PP2V5_S0_GPU_LVDDR
TRUE	PP3V3_S0
TRUE	PP3V3_S0_CK410_VDD48
TRUE	PP3V3_S0_CK410_VDD_PCI
TRUE	PP3V3_S0_CK410_VDD_REF
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC
TRUE	PP3V3_S0_CK410_VDDA
TRUE	PP3V3_FWPHY
TRUE	PP3V3_FWPHY_AVDD
TRUE	PP3V3_FWPHY_PLLVDD
TRUE	PP1V95_FWPHY
TRUE	PP1V95_FWPHY_PLLVDD
TRUE	PP1V2_S3
TRUE	PP3V3_S3AC
TRUE	PP2V5_S3
TRUE	PP2V5_S3_ENET_AVDD

Fan Connectors

FUNC_TEST	
TRUE	PP5V_S0
TRUE	FAN_LT_PWM
TRUE	FAN_LT_TACH
TRUE	FAN_RT_PWM
TRUE	FAN_RT_TACH

LPC+ Debug Connector

FUNC_TEST	
TRUE	PP3V42_G3H
TRUE	PP5V_S0
TRUE	LPC_AD<0>
TRUE	LPC_AD<1>
TRUE	LPC_FRAME_L
TRUE	PM_CLKRUN_L
TRUE	BOOT_LPC_SPI_L
TRUE	SMC_TMS
TRUE	DEBUG_RST_L
TRUE	SMC_TRST_L
TRUE	SMC_TDO
TRUE	SMC_MDI
TRUE	SMC_TX_L
TRUE	FWH_INIT_L
TRUE	PCI_CLK_PORT80_LPC
TRUE	LPC_AD<2>
TRUE	LPC_AD<3>
TRUE	INT_SERIRO
TRUE	PM_SUS_STAT_L
TRUE	SMC_TDI
TRUE	SMC_TCK
TRUE	SMC_RST_L
TRUE	SMC_NMI
TRUE	SMC_RX_L
TRUE	SV_SET_UP

Resistor Calibration

FUNC_TEST	
TRUE	PP5V_S0
TRUE	PP1V8_S3
TRUE	PP1V05_S0
TRUE	PPVCORE_S0_CPU
TRUE	PPVCORE_S0_GPU
TRUE	ISENSE_CAL_EN
TRUE	GND

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST	
TRUE	PP5V_S3
TRUE	USB2_CAMERA_N
TRUE	USB2_CAMERA_P
TRUE	SMBUS_SMC_0_S0_SDA
TRUE	SMBUS_SMC_0_S0_SCL

Thermal Sensors

FUNC_TEST	
TRUE	HSTHMSNS_DX_P
TRUE	HSTHMSNS_DX_N
TRUE	RSFSTHMSNS_D_P
TRUE	RSFSTHMSNS_D_N

SMC TPs

FUNC_TEST	
TRUE	PM_SYSRST_L
TRUE	SMC_ONOFF_L

Battery Connector

FUNC_TEST	
TRUE	BATT_POS
TRUE	BATT_NEG
TRUE	SMC_BS_ALERT_L
TRUE	SMBUS_SMC_BSA_SCL
TRUE	SMBUS_SMC_BSA_SDA

Left I/O Data Connector

FUNC_TEST	
TRUE	PP1V5_S0
TRUE	PPBUS_G3H
TRUE	PP3V42_G3H
TRUE	PP5V_S0_AUDIO
TRUE	GND_AUDIO
TRUE	ALS_GAIN
TRUE	LTALS_OUT
TRUE	ACZ_SDATAIN<0>
TRUE	ACZ_SDATAOUT
TRUE	ACZ_BITCLK
TRUE	ACZ_RST_L
TRUE	EXCARD_OC_L
TRUE	LTUSB_OC_L
TRUE	LT2USB_OC_L
TRUE	PM_SLP_S3_LS5V
TRUE	PM_SLP_S4_L
TRUE	SYS_ONEWIRE
TRUE	MINI_CLKREO_L
TRUE	SMC_EXCARD_CP
TRUE	EXCARD_CLKREO_L
TRUE	SMC_EXCARD_PWR_EN
TRUE	LIO_PLT_RESET_L
TRUE	ACZ_SYNC
TRUE	USB2_LT_N
TRUE	USB2_LT_P
TRUE	USB2_EXCARD_N
TRUE	USB2_EXCARD_P
TRUE	PCIE_EXCARD_R2D_C_N
TRUE	PCIE_EXCARD_R2D_C_P
TRUE	PCIE_EXCARD_D2R_P
TRUE	PCIE_CLK100M_EXCARD_P
TRUE	PCIE_CLK100M_EXCARD_N
TRUE	USB2_LT2_N
TRUE	USB2_LT2_P
TRUE	PCIE_MINI_R2D_C_N
TRUE	PCIE_MINI_R2D_C_P
TRUE	PCIE_MINI_D2R_N
TRUE	PCIE_MINI_D2R_P
TRUE	PCIE_CLK100M_MINI_P
TRUE	PCIE_CLK100M_MINI_N
TRUE	SMBUS_SB_SCL
TRUE	SMBUS_SB_SDA
TRUE	PCIE_WAKE_L
TRUE	SMC_BC_ACOK

Left I/O Power Connector

FUNC_TEST	
TRUE	PP1V8V_DCI_N
TRUE	PP5V_S5
TRUE	PP5V_S0_AUDIO_PWR
TRUE	GND_AUDIO_PWR
TRUE	GND

Request for at least 10 GND test points

Functional / ICT Test

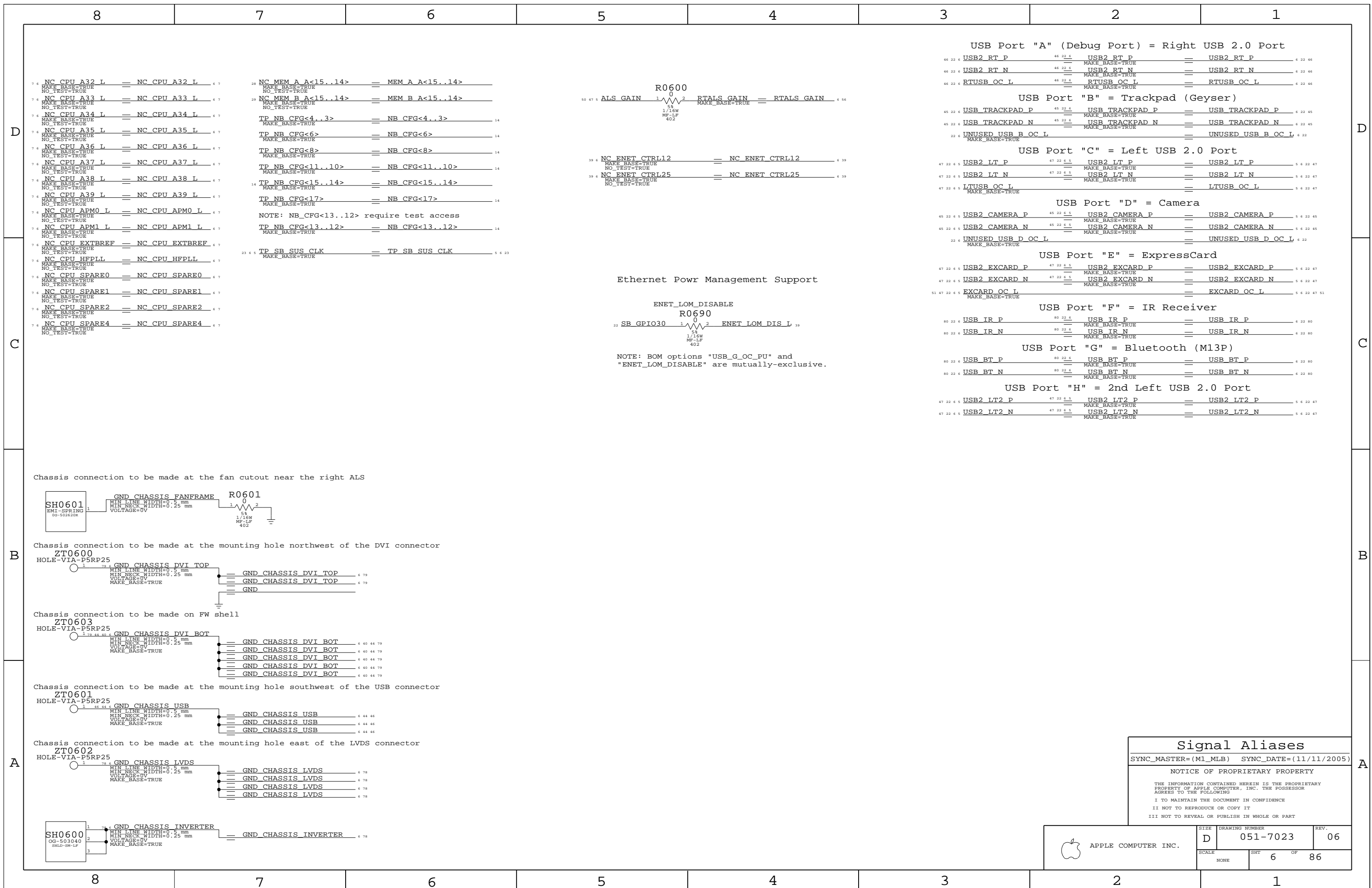
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	5	86



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USB Port "A" (Debug Port) = Right USB 2.0 Port

46 22 6	USB2_RT_P	46 22 6	USB2_RT_P	==	USB2_RT_P	6 22 46
46 22 6	USB2_RT_N	46 22 6	USB2_RT_N	==	USB2_RT_N	6 22 46
46 22 6	RTUSB_OC_L	46 22 6	RTUSB_OC_L	==	RTUSB_OC_L	6 22 46

USB Port "B" = Trackpad (Geyser)

45 22 6	USB_TRACKPAD_P	45 22 6	USB_TRACKPAD_P	==	USB_TRACKPAD_P	6 22 45
45 22 6	USB_TRACKPAD_N	45 22 6	USB_TRACKPAD_N	==	USB_TRACKPAD_N	6 22 45
22 6	UNUSED_USB_B_OC_L			==	UNUSED_USB_B_OC_L	6 22

USB Port "C" = Left USB 2.0 Port

47 22 6 5	USB2_LT_P	47 22 6 5	USB2_LT_P	==	USB2_LT_P	5 6 22 47
47 22 6 5	USB2_LT_N	47 22 6 5	USB2_LT_N	==	USB2_LT_N	5 6 22 47
47 22 6 5	LTUSB_OC_L			==	LTUSB_OC_L	5 6 22 47

USB Port "D" = Camera

45 22 6 5	USB2_CAMERA_P	45 22 6 5	USB2_CAMERA_P	==	USB2_CAMERA_P	5 6 22 45
45 22 6 5	USB2_CAMERA_N	45 22 6 5	USB2_CAMERA_N	==	USB2_CAMERA_N	5 6 22 45
22 6	UNUSED_USB_D_OC_L			==	UNUSED_USB_D_OC_L	6 22

USB Port "E" = ExpressCard

47 22 6 5	USB2_EXCARD_P	47 22 6 5	USB2_EXCARD_P	==	USB2_EXCARD_P	5 6 22 47
47 22 6 5	USB2_EXCARD_N	47 22 6 5	USB2_EXCARD_N	==	USB2_EXCARD_N	5 6 22 47
51 47 22 6 5	EXCARD_OC_L			==	EXCARD_OC_L	5 6 22 47 51

USB Port "F" = IR Receiver

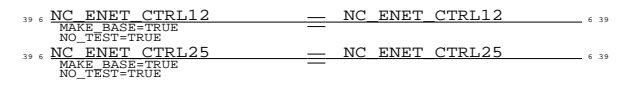
80 22 6	USB_IR_P	80 22 6	USB_IR_P	==	USB_IR_P	6 22 80
80 22 6	USB_IR_N	80 22 6	USB_IR_N	==	USB_IR_N	6 22 80

USB Port "G" = Bluetooth (M13P)

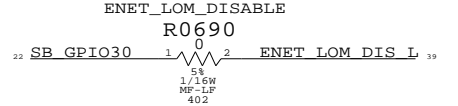
80 22 6	USB_BT_P	80 22 6	USB_BT_P	==	USB_BT_P	6 22 80
80 22 6	USB_BT_N	80 22 6	USB_BT_N	==	USB_BT_N	6 22 80

USB Port "H" = 2nd Left USB 2.0 Port

47 22 6 5	USB2_LT2_P	47 22 6 5	USB2_LT2_P	==	USB2_LT2_P	5 6 22 47
47 22 6 5	USB2_LT2_N	47 22 6 5	USB2_LT2_N	==	USB2_LT2_N	5 6 22 47

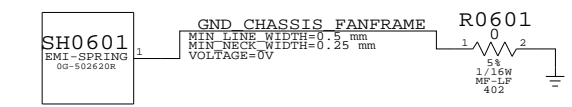


Ethernet Powr Management Support

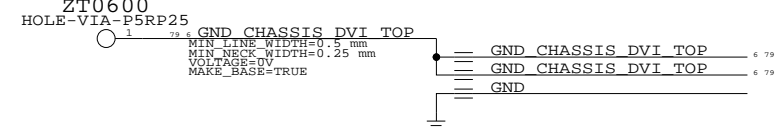


NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

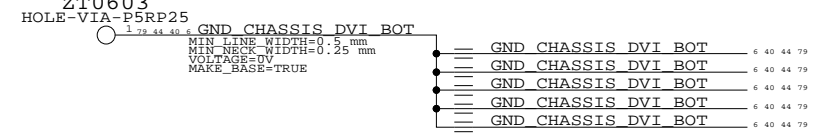
Chassis connection to be made at the fan cutout near the right ALS



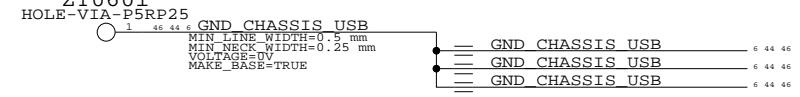
Chassis connection to be made at the mounting hole northwest of the DVI connector



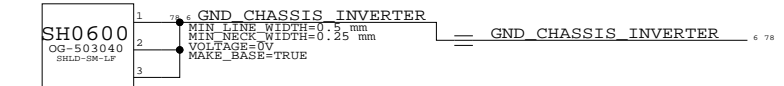
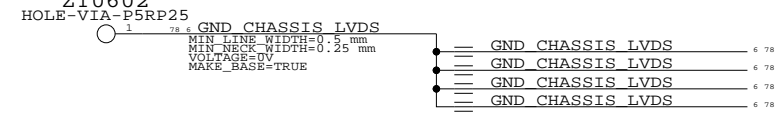
Chassis connection to be made on FW shell



Chassis connection to be made at the mounting hole southwest of the USB connector

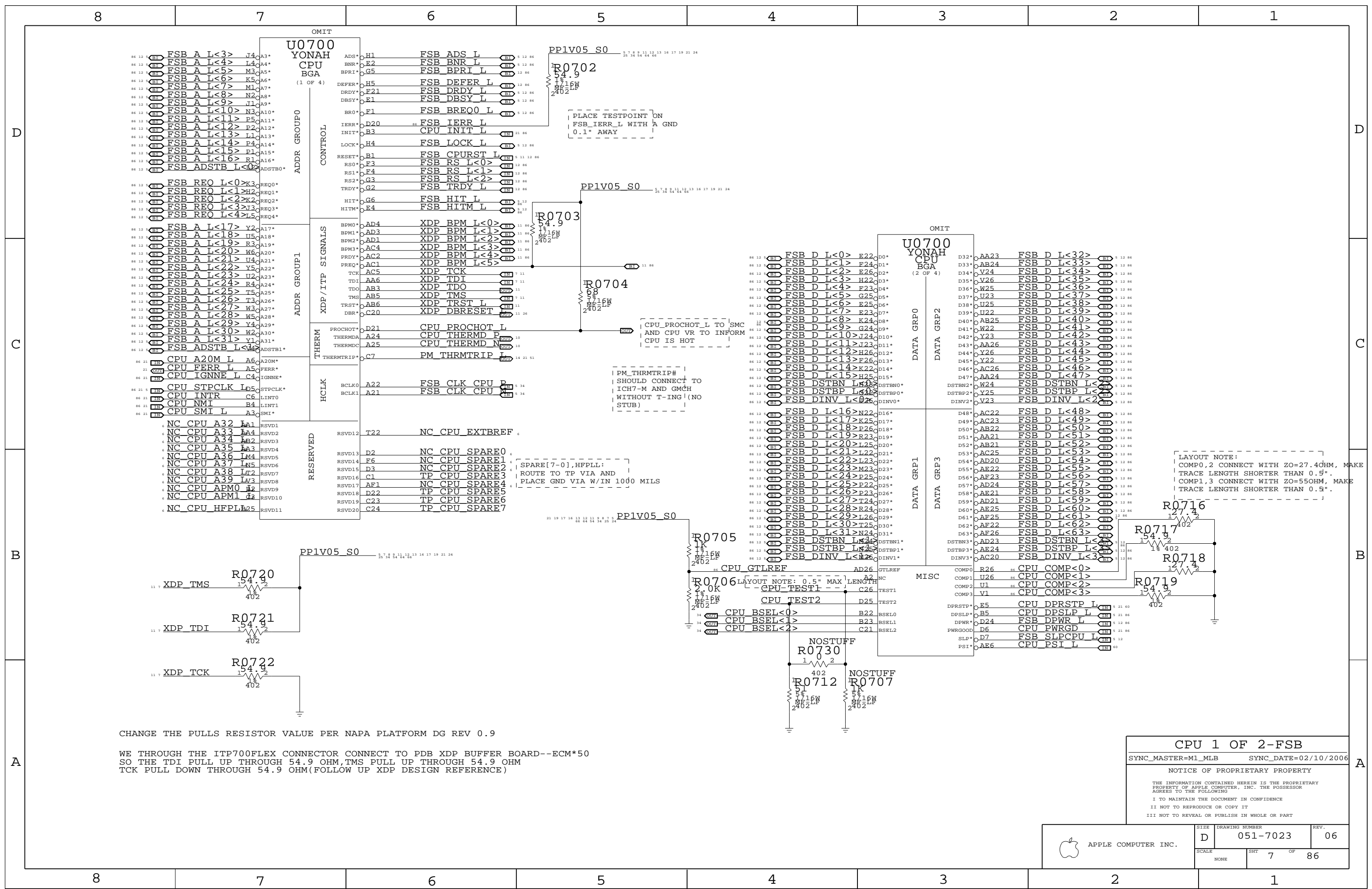


Chassis connection to be made at the mounting hole east of the LVDS connector



Signal Aliases		
SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/11/2005)		
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NONE	6	86	



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM#50
 SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM
 TCK PULL DOWN THROUGH 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

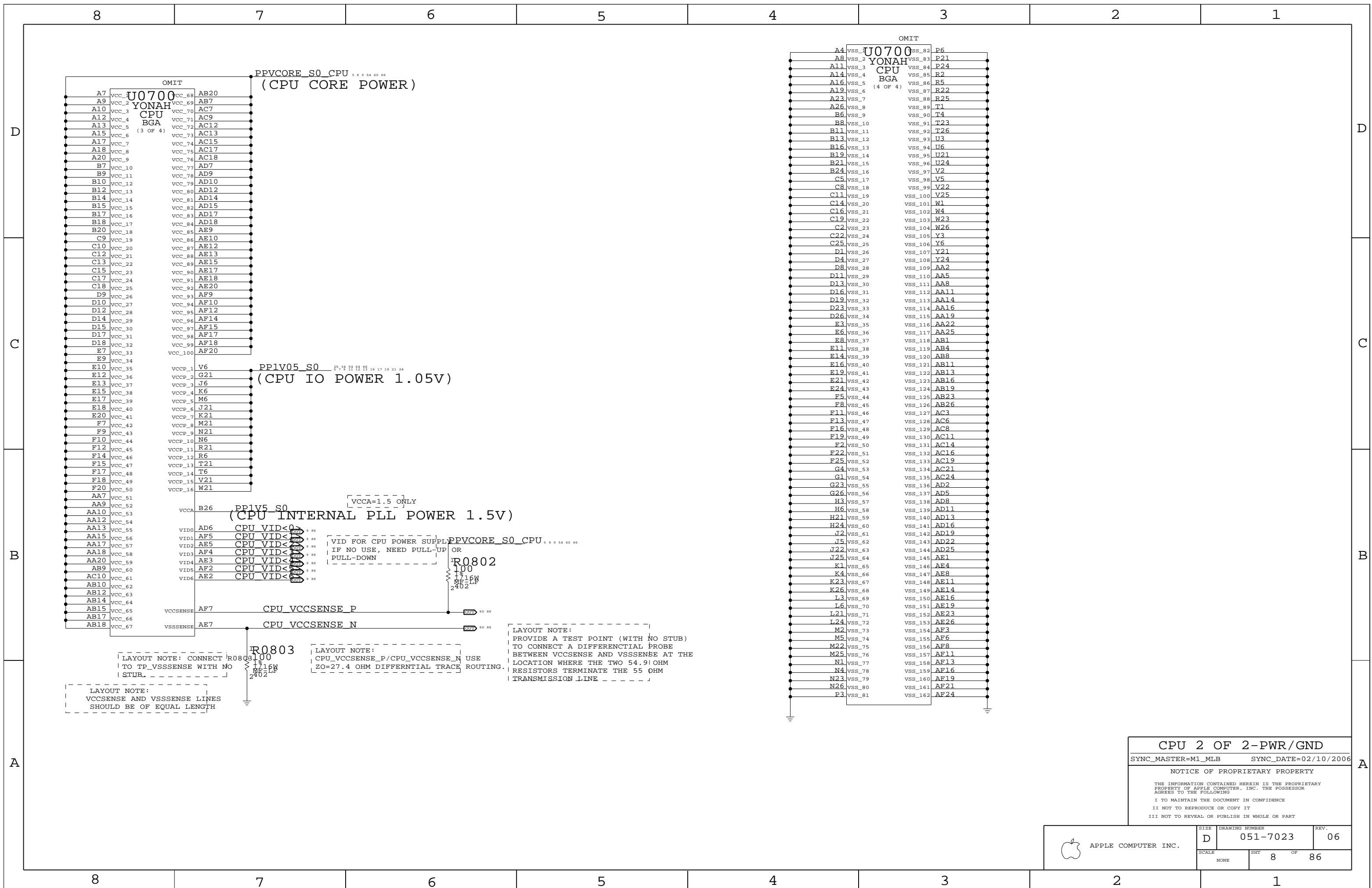
CPU 1 OF 2-FSB
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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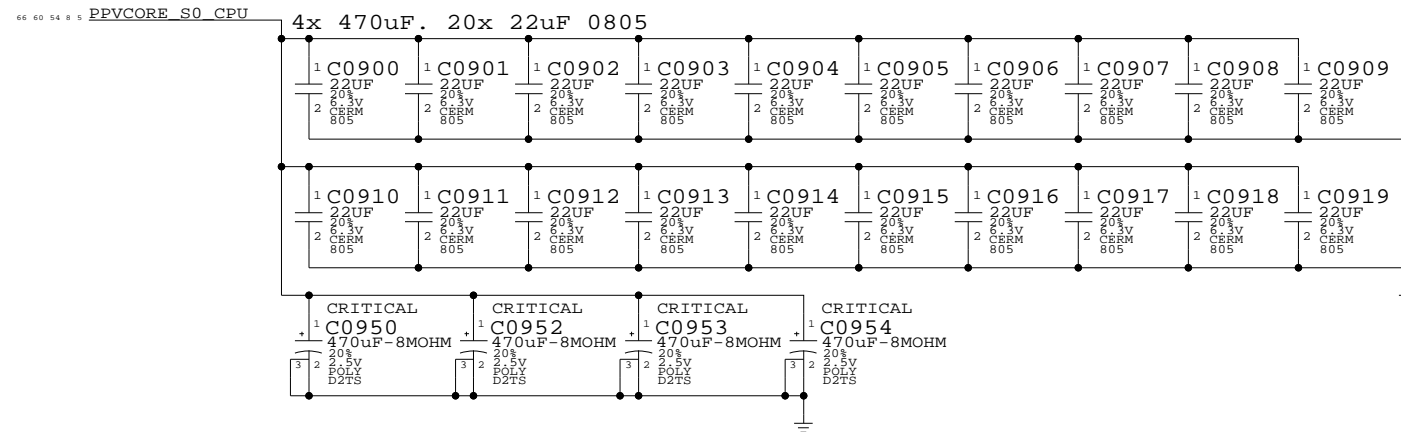


CPU 2 OF 2-PWR/GND
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

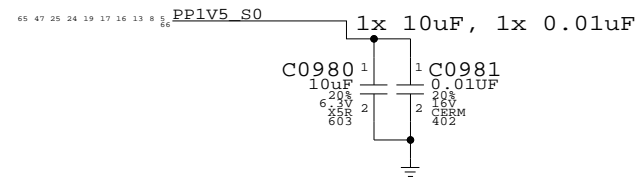
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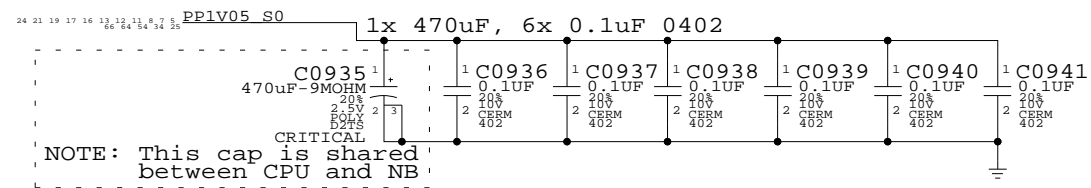
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

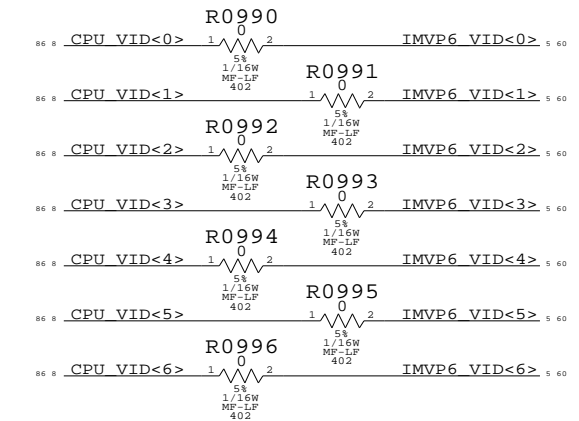


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



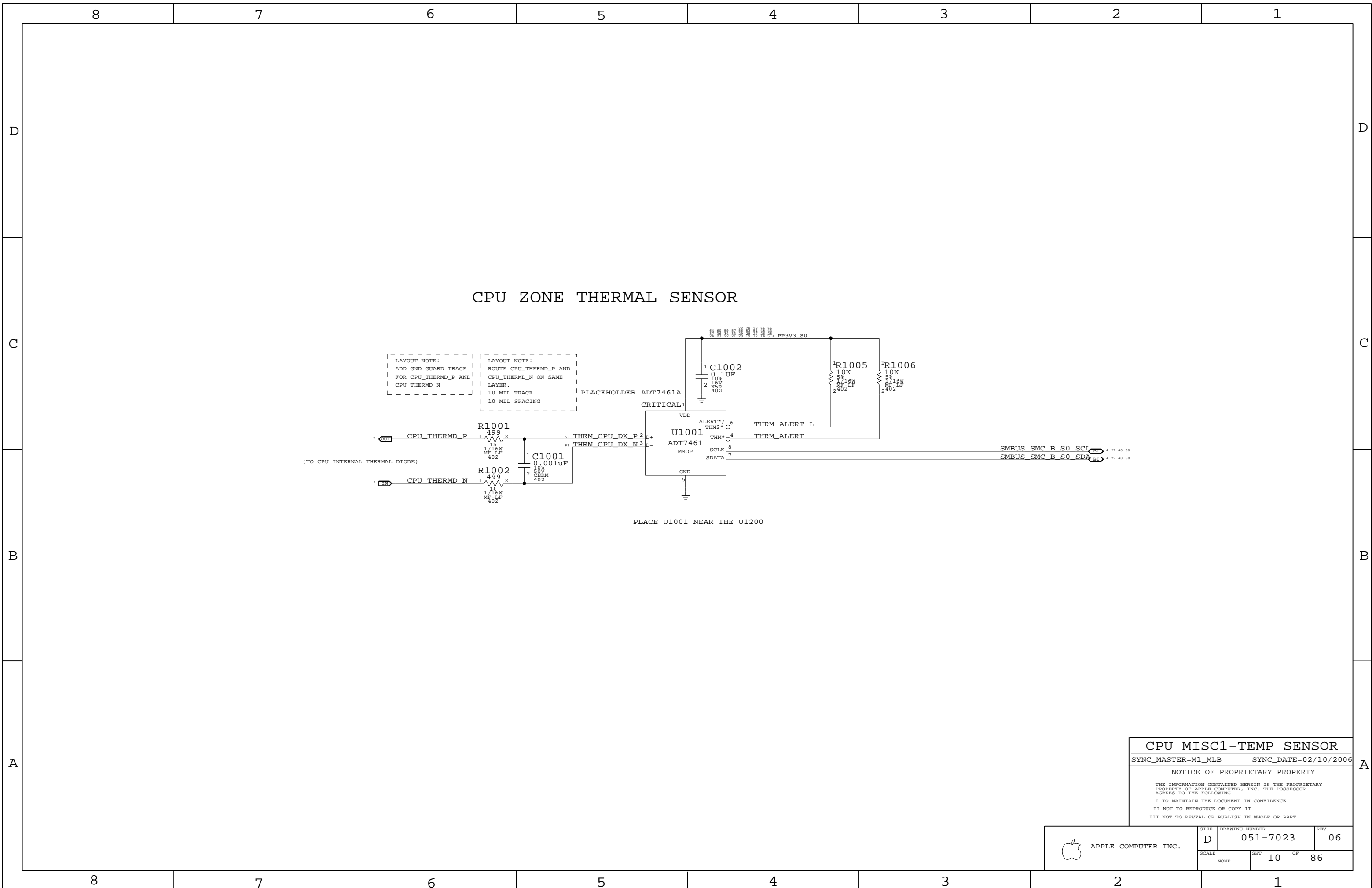
CPU Decoupling & VID

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

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CPU MISC1-TEMP SENSOR

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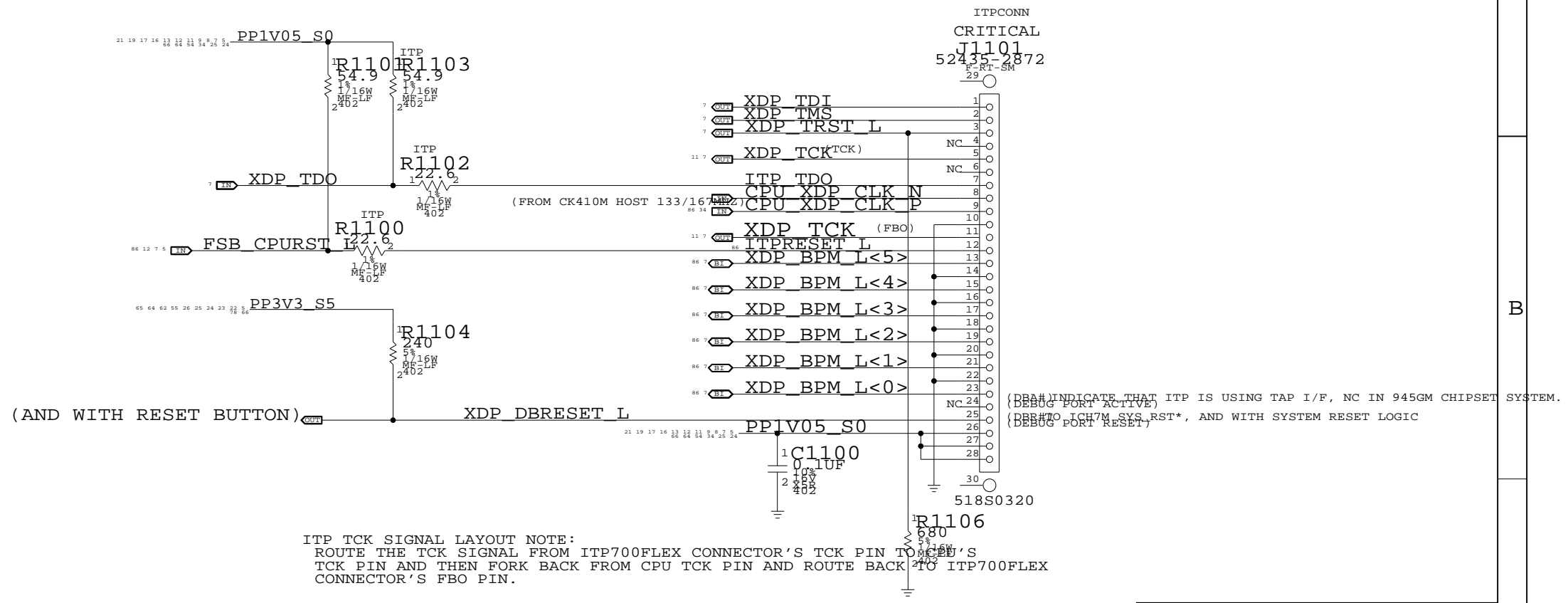
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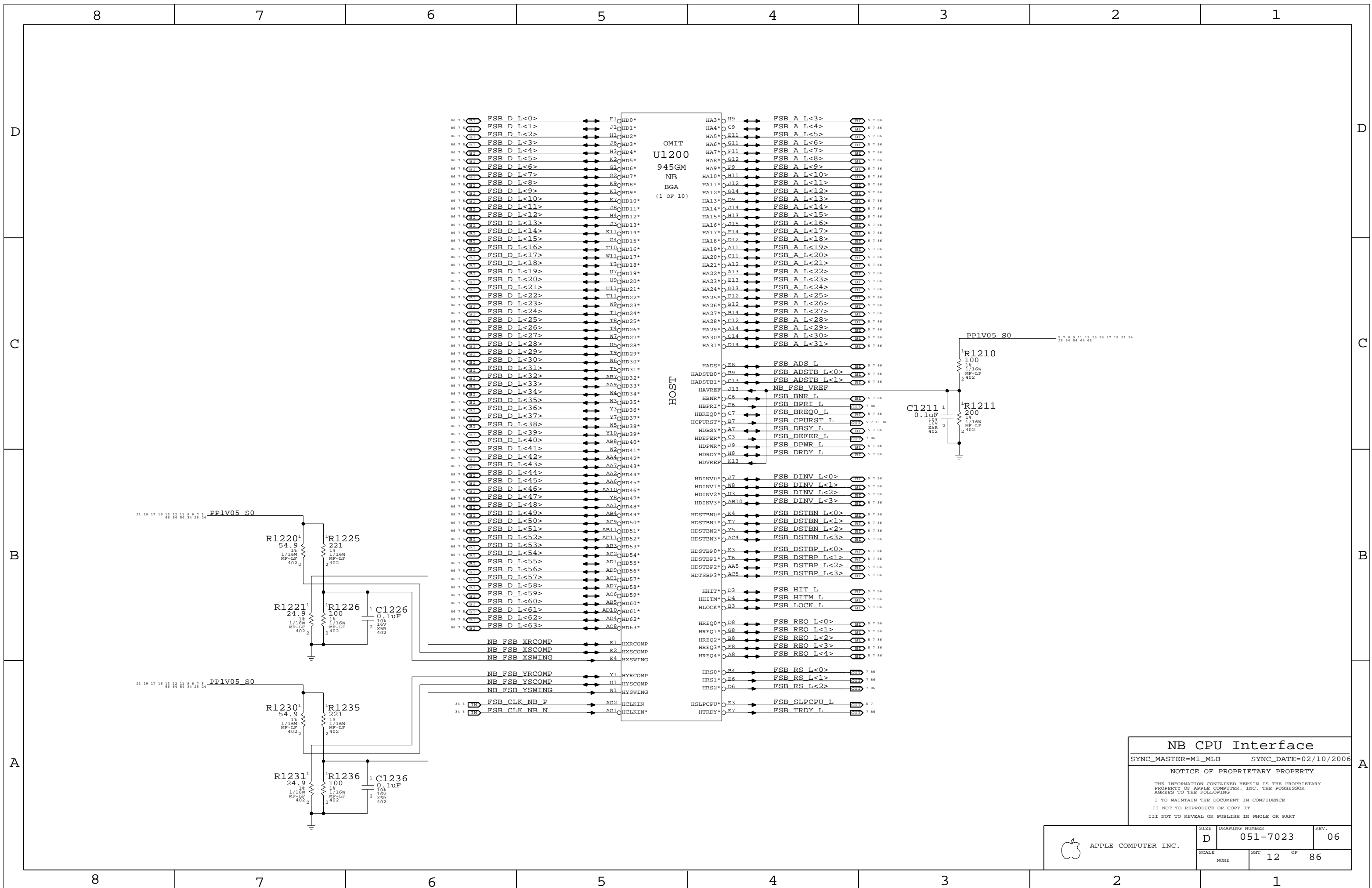
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO
 CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG
 SYNC_MASTER=MSYNCBDATE=02/10/2006
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NB CPU Interface
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NONE	12		86

LVDS Disable

Can leave all signals NC if LVDS is not implemented Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only S-Video: DACB & DACC only Component: DACA, DACB & DACC

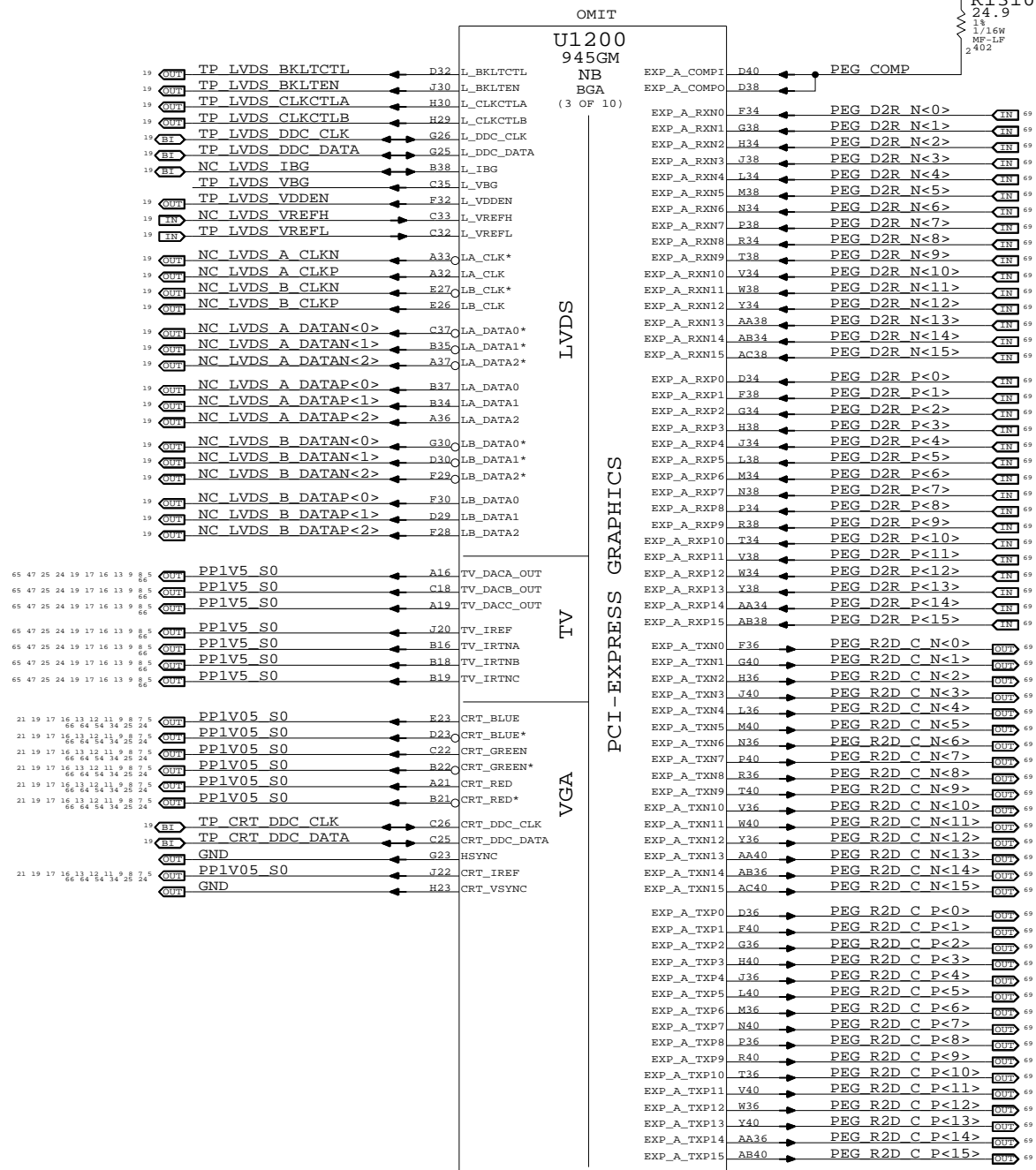
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TV DAC, VCCD_QTV DAC, VCCA_TV DACx, and VCCA_TV BG to 1.5V power rail. Tie VSSA_TV BG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRT DAC to VCC Core rail, and tie VSSA_CRT DAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN# SDVO_INT# SDVO_FLDSTALL#

SDVO_TVCLKIN SDVO_INT SDVO_FLDSTALL

SDVOB_RED# SDVOB_GREEN# SDVOB_BLUE# SDVOB_CLKN SDVOC_RED# SDVOC_GREEN# SDVOC_BLUE# SDVOC_CLKN

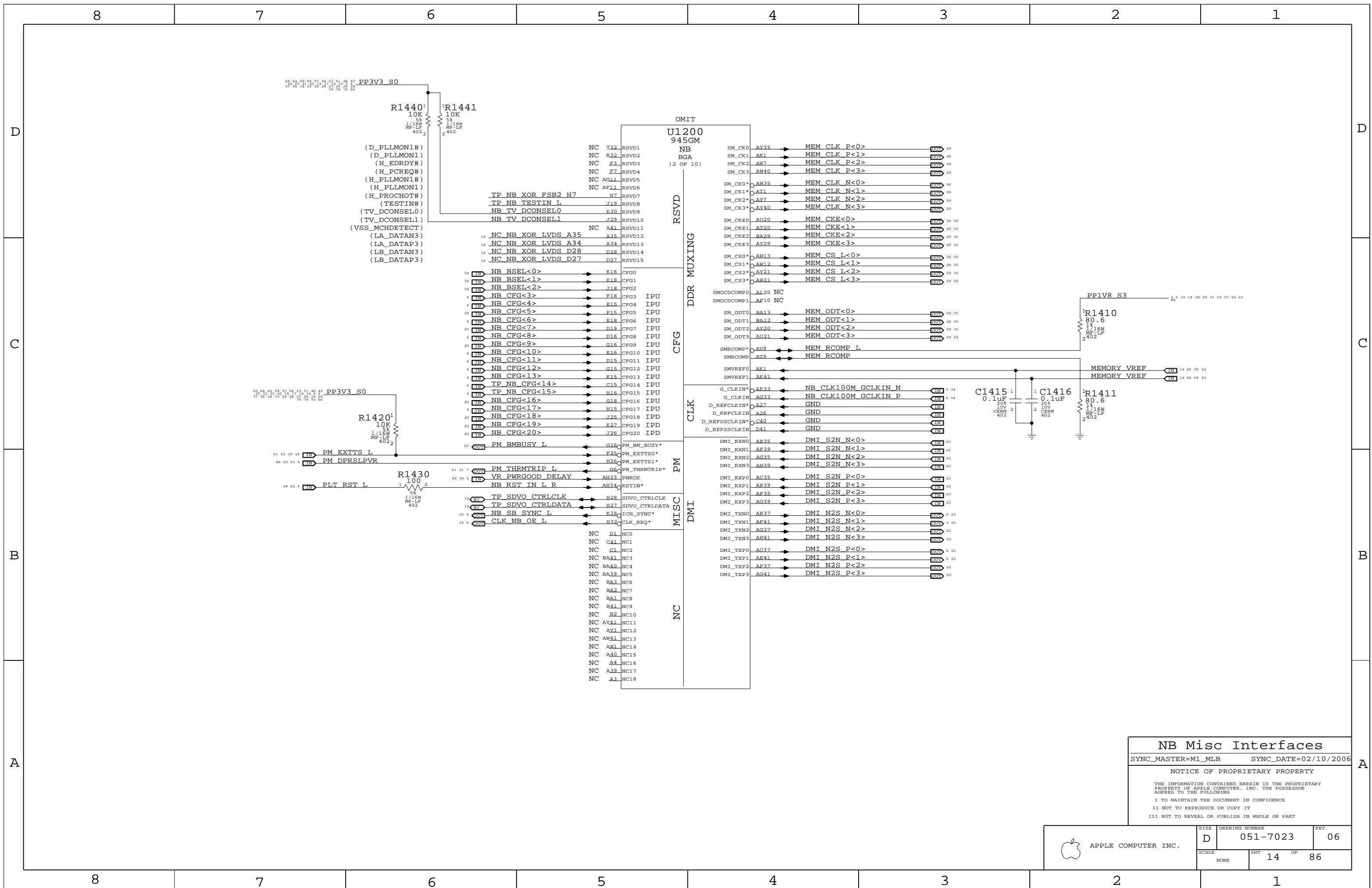
SDVOB_RED SDVOB_GREEN SDVOB_BLUE SDVOB_CLKP SDVOC_RED SDVOC_GREEN SDVOC_BLUE SDVOC_CLKP

NB PEG / Video Interfaces SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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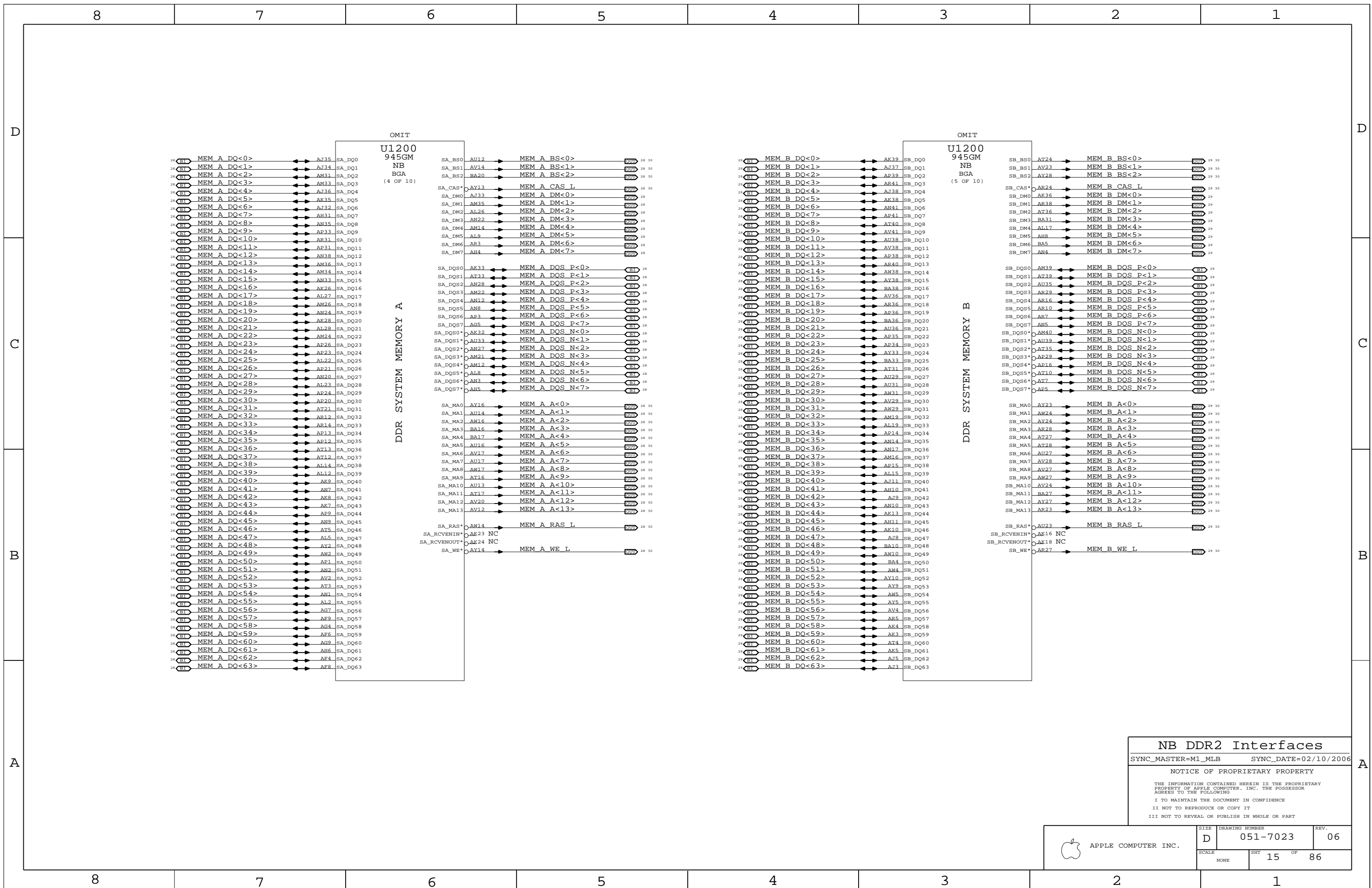
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NB Misc Interfaces
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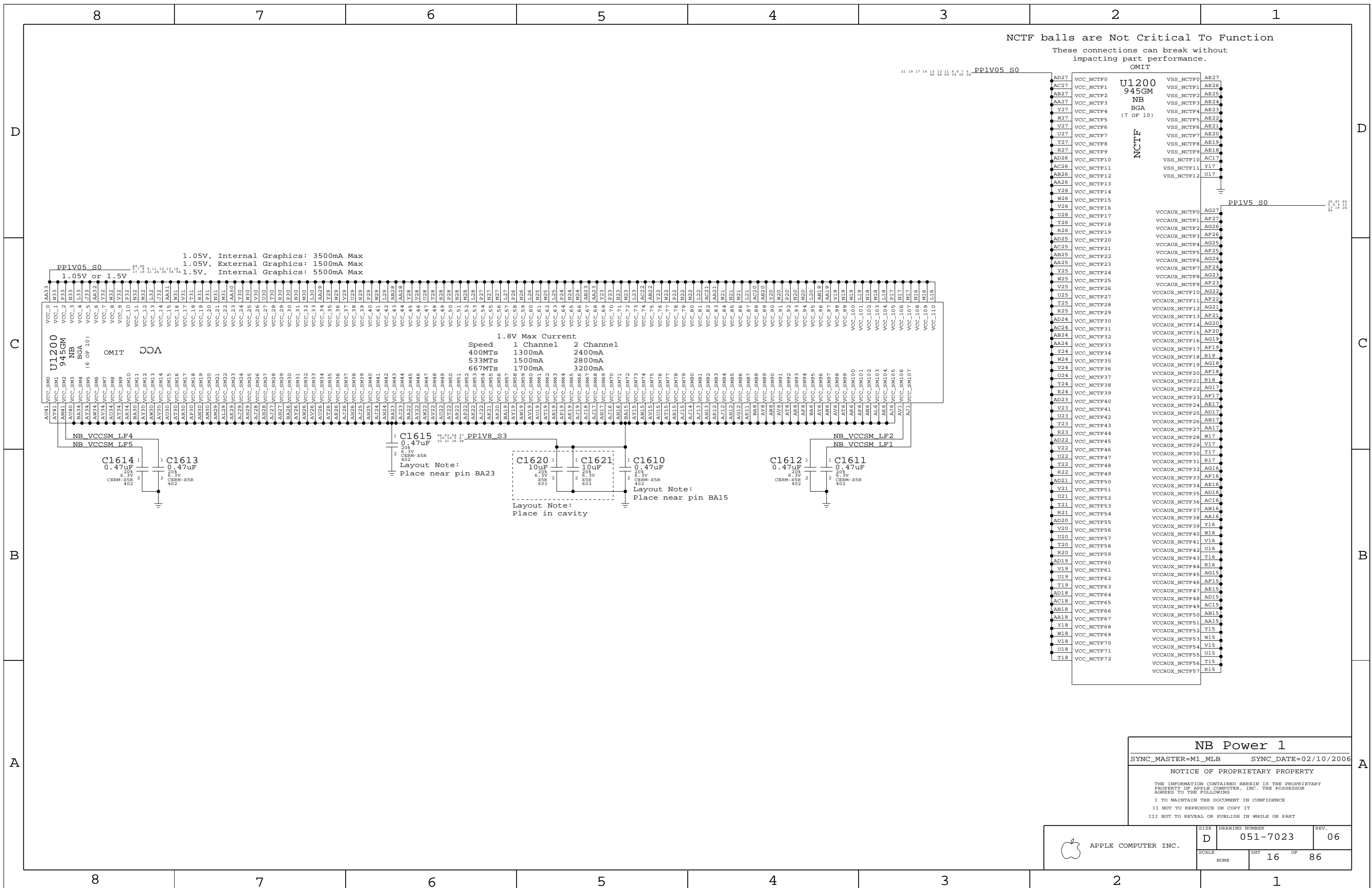
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NB DDR2 Interfaces
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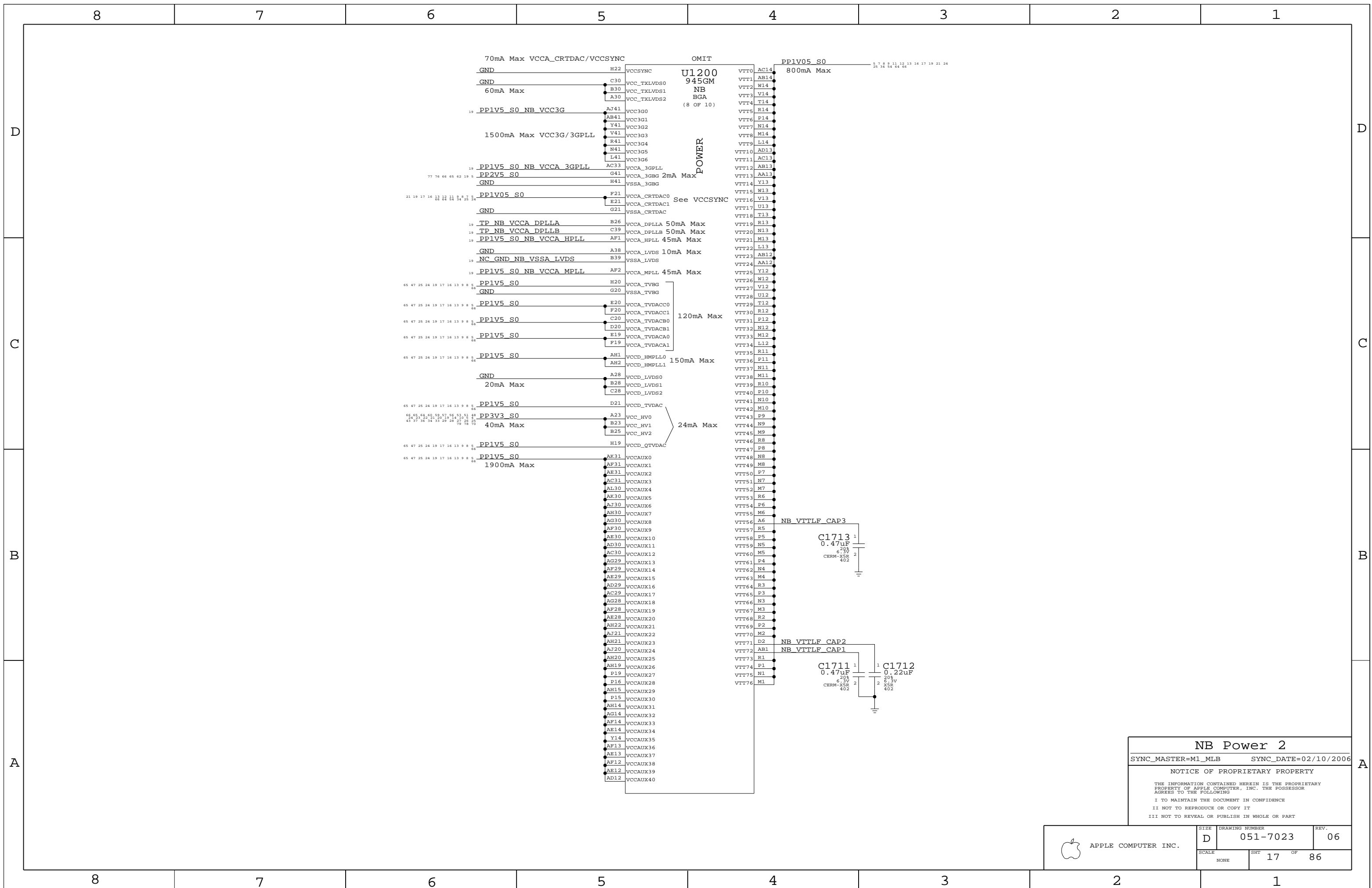
NB Power 1
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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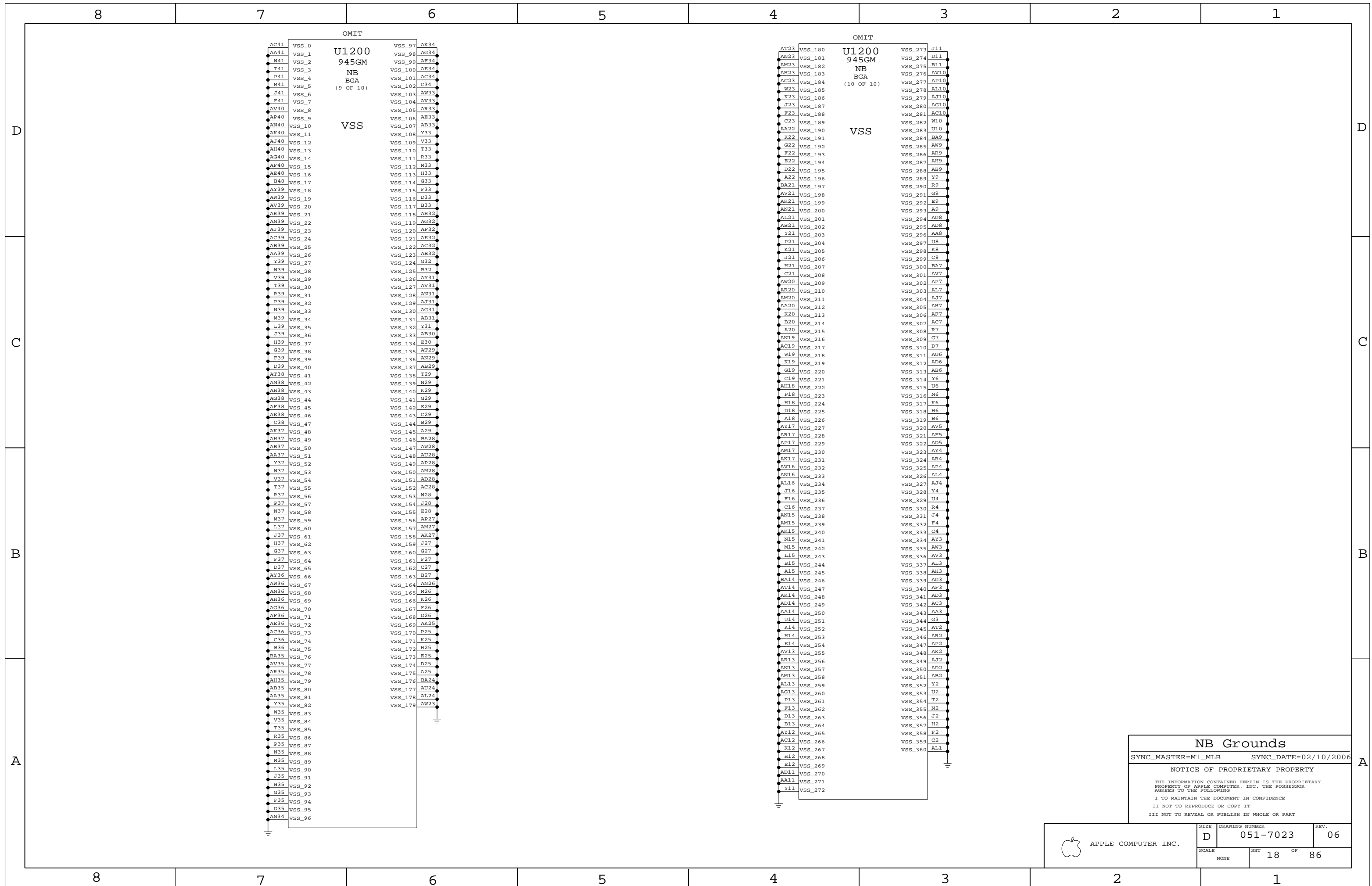
NB Power 2
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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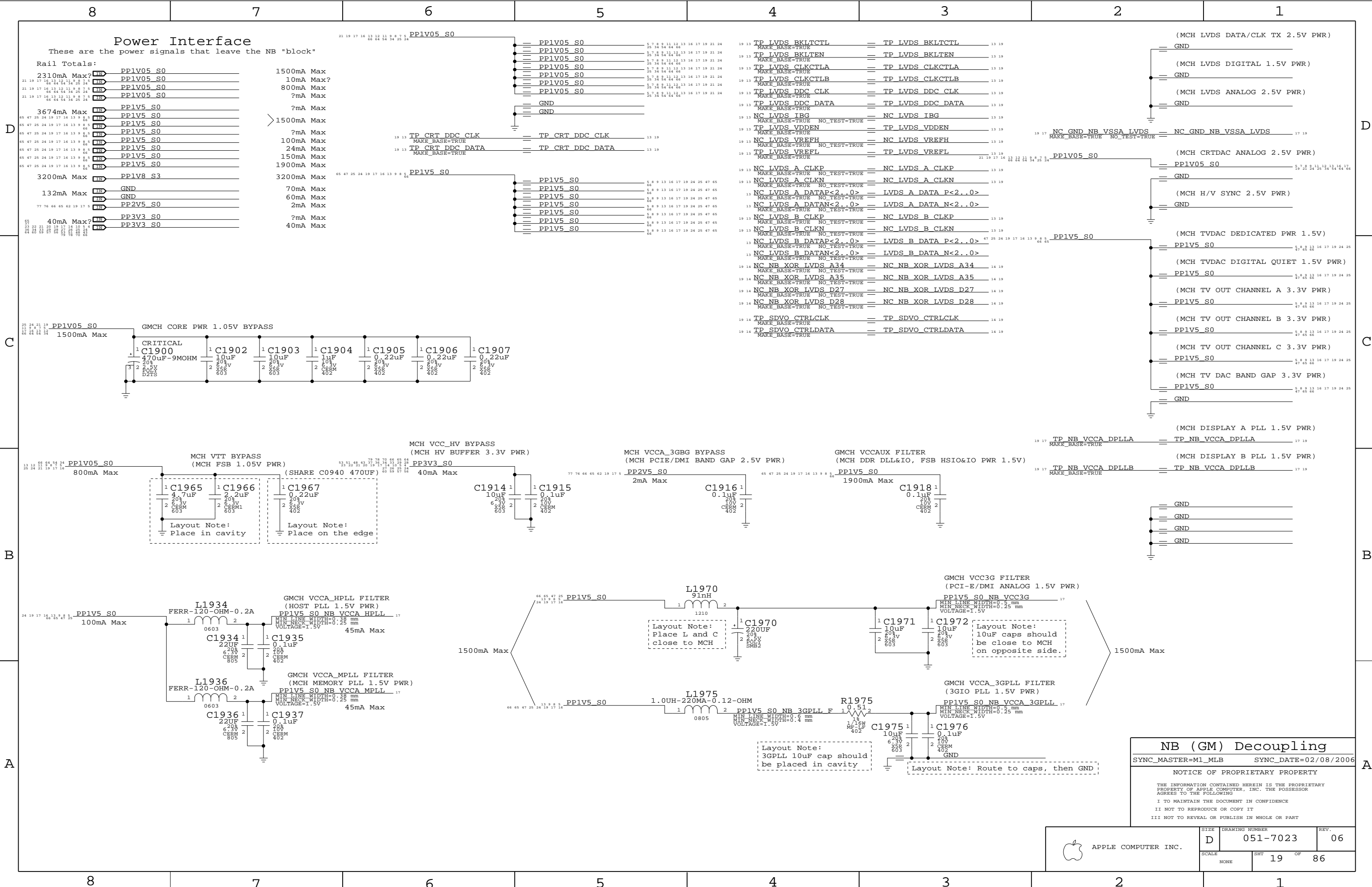
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	SCALE NONE	SHEET 17 OF 86	



NB Grounds
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SCALE	SHT 18 OF 86		
NONE			



Power Interface

These are the power signals that leave the NB "block"

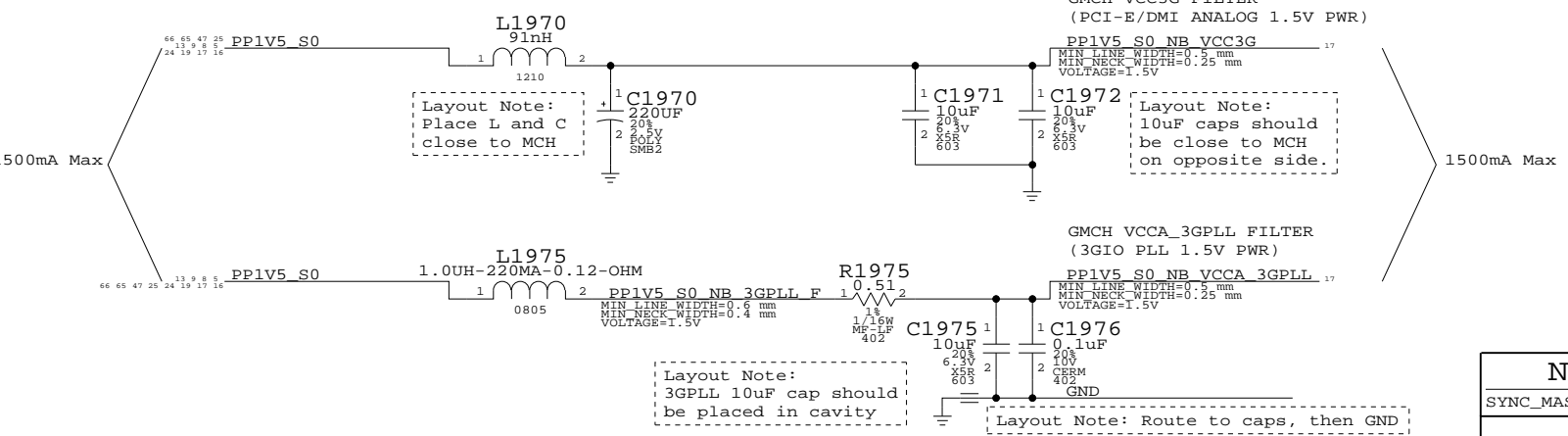
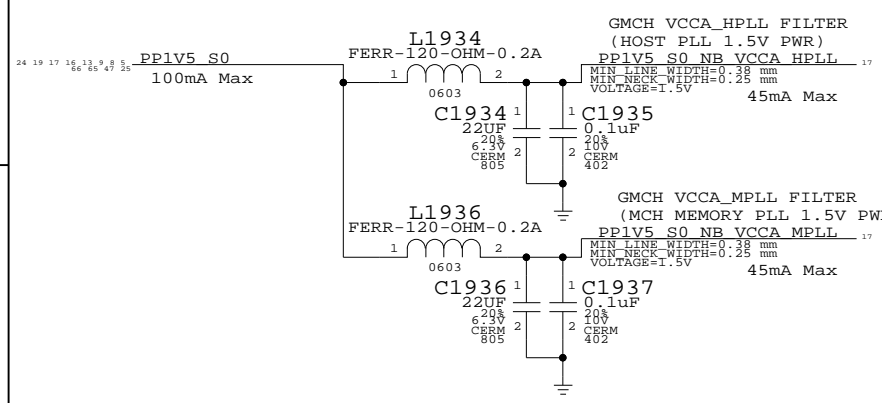
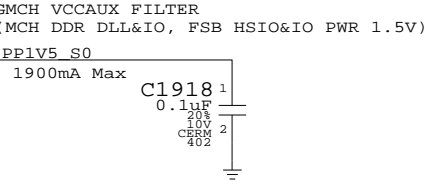
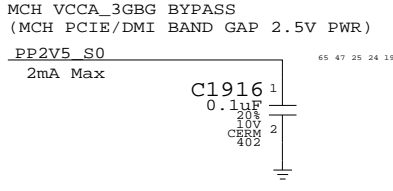
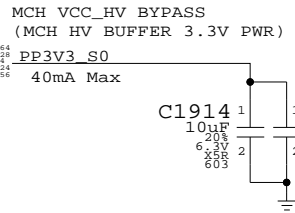
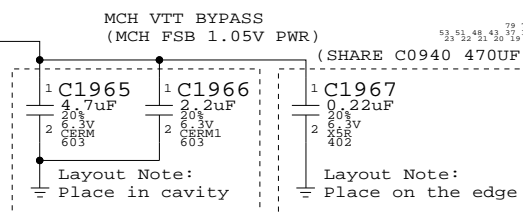
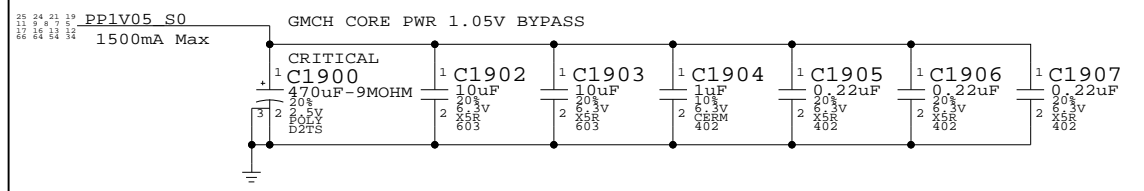
Rail Totals:

2310mA Max?	PP1V05_S0	1500mA Max
10mA Max?	PP1V05_S0	10mA Max?
800mA Max	PP1V05_S0	800mA Max
?	PP1V05_S0	?mA Max
3674mA Max	PP1V5_S0	?mA Max
1500mA Max	PP1V5_S0	>1500mA Max
?	PP1V5_S0	?mA Max
100mA Max	PP1V5_S0	100mA Max
24mA Max	PP1V5_S0	24mA Max
150mA Max	PP1V5_S0	150mA Max
1900mA Max	PP1V5_S0	1900mA Max
3200mA Max	PP1V8_S3	3200mA Max
70mA Max	GND	70mA Max
60mA Max	GND	60mA Max
2mA Max	PP2V5_S0	2mA Max
?	PP3V3_S0	?mA Max
40mA Max?	PP3V3_S0	40mA Max

21 19 17 16 13 12 11 9 8 7 5	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24
66 64 64 64 66	PP1V05_S0	25 34 54 64 66
	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24
	PP1V05_S0	25 34 54 64 66
	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24
	PP1V05_S0	25 34 54 64 66
	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24
	PP1V05_S0	25 34 54 64 66
	GND	
	GND	
19 13	TP CRT DDC CLK	TP CRT DDC CLK 13 19
	MAKE_BASE=TRUE	
19 13	TP CRT DDC DATA	TP CRT DDC DATA 13 19
	MAKE_BASE=TRUE	
65 47 25 24 19 17 16 13 9 8 6	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65
	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65

19 13	TP LVDS BKLCTCTL	TP LVDS BKLCTCTL 13 19
	MAKE_BASE=TRUE	
19 13	TP LVDS BKLCTEN	TP LVDS BKLCTEN 13 19
	MAKE_BASE=TRUE	
19 13	TP LVDS CLKCTLA	TP LVDS CLKCTLA 13 19
	MAKE_BASE=TRUE	
19 13	TP LVDS CLKCTLB	TP LVDS CLKCTLB 13 19
	MAKE_BASE=TRUE	
19 13	TP LVDS DDC CLK	TP LVDS DDC CLK 13 19
	MAKE_BASE=TRUE	
19 13	TP LVDS DDC DATA	TP LVDS DDC DATA 13 19
	MAKE_BASE=TRUE	
19 13	NC LVDS IBG	NC LVDS IBG 13 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 13	TP LVDS VDDEN	TP LVDS VDDEN 13 19
	MAKE_BASE=TRUE	
19 13	NC LVDS VREFH	NC LVDS VREFH 13 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 13	TP LVDS VREFL	TP LVDS VREFL 13 19
	MAKE_BASE=TRUE	
19 13	NC LVDS A CLKP	NC LVDS A CLKP 13 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 13	NC LVDS A CLKN	NC LVDS A CLKN 13 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
13	NC LVDS A DATAP<2..0>	LVDS A DATA P<2..0>
	MAKE_BASE=TRUE NO_TEST=TRUE	
13	NC LVDS A DATAN<2..0>	LVDS A DATA N<2..0>
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 13	NC LVDS B CLKP	NC LVDS B CLKP 13 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 13	NC LVDS B CLKN	NC LVDS B CLKN 13 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
13	NC LVDS B DATAP<2..0>	LVDS B DATA P<2..0>
	MAKE_BASE=TRUE NO_TEST=TRUE	
13	NC LVDS B DATAN<2..0>	LVDS B DATA N<2..0>
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 14	NC NB XOR LVDS A34	NC NB XOR LVDS A34 14 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 14	NC NB XOR LVDS A35	NC NB XOR LVDS A35 14 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 14	NC NB XOR LVDS D27	NC NB XOR LVDS D27 14 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 14	NC NB XOR LVDS D28	NC NB XOR LVDS D28 14 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
19 14	TP SDVO CTRLCLK	TP SDVO CTRLCLK 14 19
	MAKE_BASE=TRUE	
19 14	TP SDVO CTRLDATA	TP SDVO CTRLDATA 14 19
	MAKE_BASE=TRUE	

	(MCH LVDS DATA/CLK TX 2.5V PWR)	
	GND	
	(MCH LVDS DIGITAL 1.5V PWR)	
	GND	
	(MCH LVDS ANALOG 2.5V PWR)	
	GND	
19 17	NC_GND_NB_VSSA_LVDS	NC_GND_NB_VSSA_LVDS 17 19
	MAKE_BASE=TRUE NO_TEST=TRUE	
	(MCH CRTDAC ANALOG 2.5V PWR)	
	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24
	GND	
	(MCH H/V SYNC 2.5V PWR)	
	GND	
	(MCH TVDAC DEDICATED PWR 1.5V)	
	PP1V5_S0	5 8 9 13 16 17 19 24 25
	(MCH TVDAC DIGITAL QUIET 1.5V PWR)	
	PP1V5_S0	5 8 9 13 16 17 19 24 25
	(MCH TV OUT CHANNEL A 3.3V PWR)	
	PP1V5_S0	5 8 9 13 16 17 19 24 25
	(MCH TV OUT CHANNEL B 3.3V PWR)	
	PP1V5_S0	5 8 9 13 16 17 19 24 25
	(MCH TV OUT CHANNEL C 3.3V PWR)	
	PP1V5_S0	5 8 9 13 16 17 19 24 25
	(MCH TV DAC BAND GAP 3.3V PWR)	
	PP1V5_S0	5 8 9 13 16 17 19 24 25
	GND	
	(MCH DISPLAY A PLL 1.5V PWR)	
19 17	TP_NB_VCCA_DPLLA	TP_NB_VCCA_DPLLA 17 19
	MAKE_BASE=TRUE	
	(MCH DISPLAY B PLL 1.5V PWR)	
19 17	TP_NB_VCCA_DPLLB	TP_NB_VCCA_DPLLB 17 19
	MAKE_BASE=TRUE	
	GND	
	GND	
	GND	
	GND	



NB (GM) Decoupling

SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

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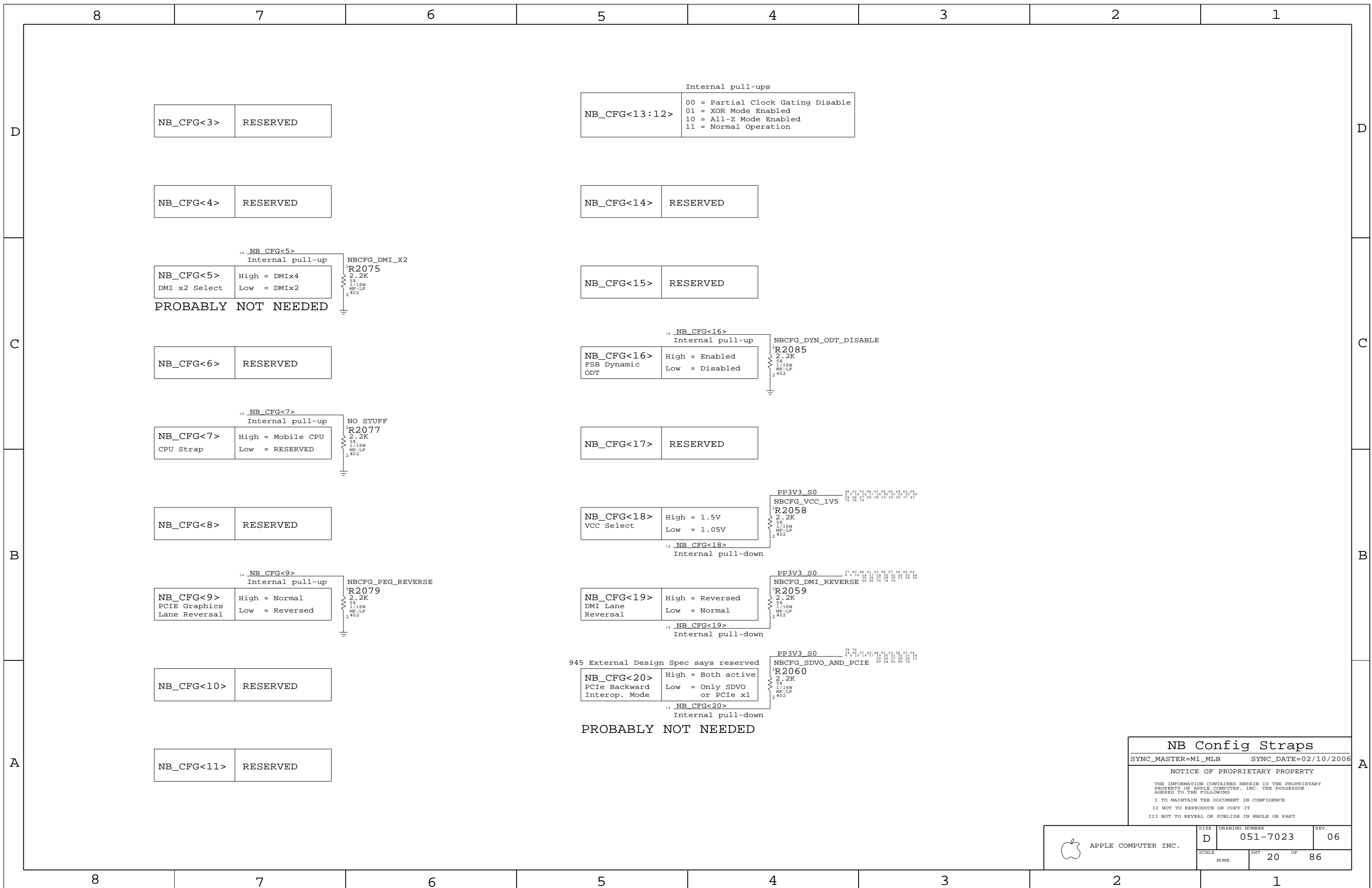
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	D	051-7023	06
SCALE	SHT	OF	
NONE	19	86	



NB_CFG<3> RESERVED

Internal pull-ups
 NB_CFG<13:12> 00 = Partial Clock Gating Disable
 01 = XOR Mode Enabled
 10 = All-Z Mode Enabled
 11 = Normal Operation

NB_CFG<4> RESERVED

NB_CFG<14> RESERVED

14 NB_CFG<5> Internal pull-up
 NBCFG_DMI_X2
 R2075 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<5> High = DMIx4
 DMI x2 Select Low = DMIx2
 PROBABLY NOT NEEDED

NB_CFG<15> RESERVED

NB_CFG<6> RESERVED

14 NB_CFG<16> Internal pull-up
 NBCFG_DYN_ODT_DISABLE
 R2085 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<16> High = Enabled
 FSB Dynamic ODT Low = Disabled

14 NB_CFG<7> Internal pull-up
 NO STUFF
 R2077 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<7> High = Mobile CPU
 CPU Strap Low = RESERVED

NB_CFG<17> RESERVED

NB_CFG<8> RESERVED

PP3V3_S0 48, 51, 93, 96, 97, 98, 65, 64, 63, 66, 4
 NBCFG_VCC_1V5 70, 26, 27, 28, 29, 33, 34, 36, 37, 43
 R2058 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<18> High = 1.5V
 VCC Select Low = 1.05V
 14 NB_CFG<18> Internal pull-down

14 NB_CFG<9> Internal pull-up
 NBCFG_PEG_REVERSE
 R2079 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<9> High = Normal
 PCIe Graphics Lane Reversal Low = Reversed

PP3V3_S0 37, 41, 48, 51, 53, 56, 57, 59, 60, 64
 NBCFG_DMI_REVERSE 4, 5, 10, 11, 13, 17, 20, 21, 22, 23, 24
 R2059 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<19> High = Reversed
 DMI Lane Reversal Low = Normal
 14 NB_CFG<19> Internal pull-down

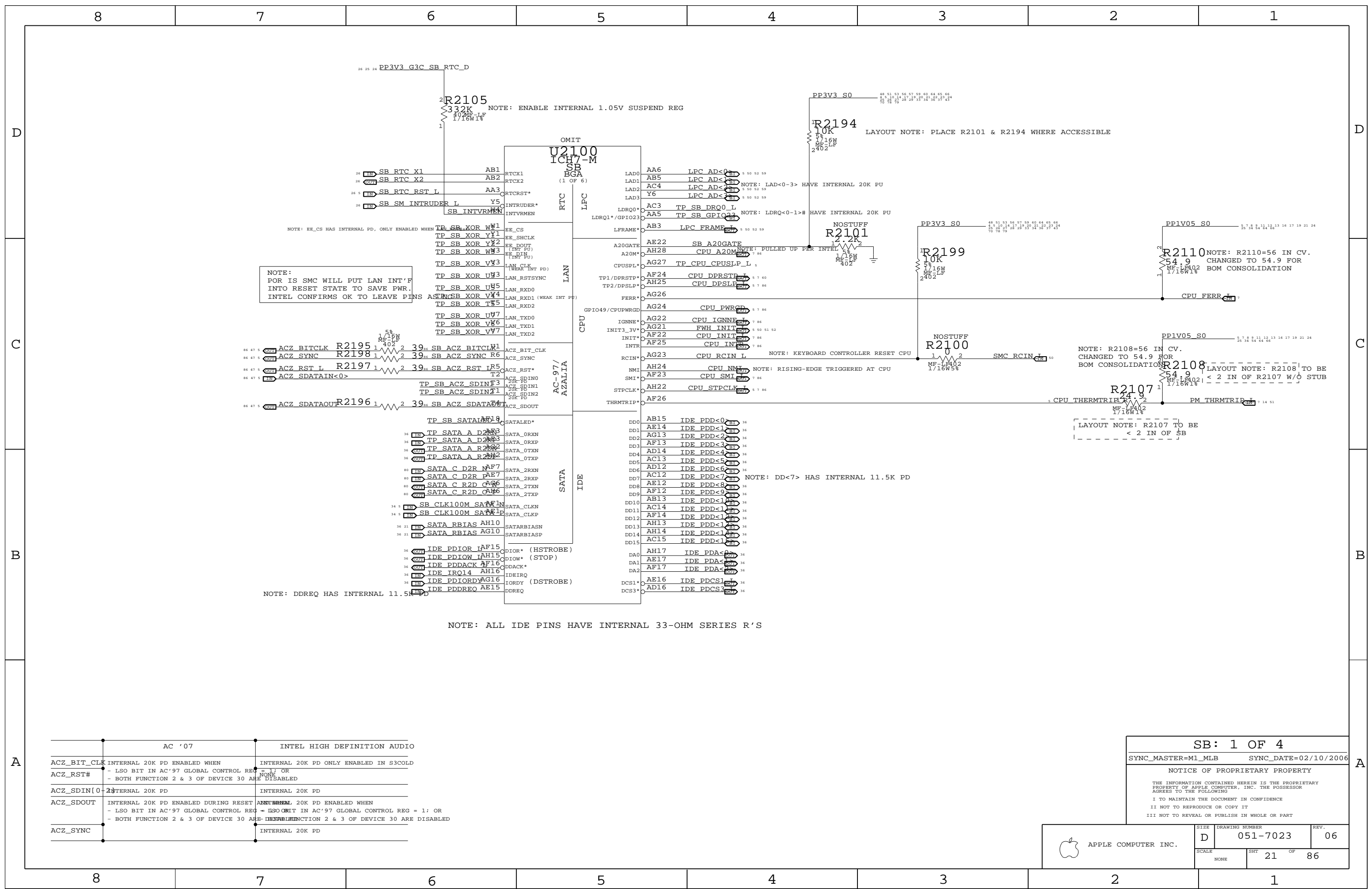
NB_CFG<10> RESERVED

945 External Design Spec says reserved
 PP3V3_S0 78, 79
 NBCFG_SDVO_AND_PCIE 24, 30, 31, 41, 48, 51, 53, 56, 57, 59
 R2060 2.2K
 5% 1/16W MF-LP
 2 402
 NB_CFG<20> High = Both active
 PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1
 14 NB_CFG<20> Internal pull-down
 PROBABLY NOT NEEDED

NB_CFG<11> RESERVED

NB Config Straps
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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	D	051-7023	06
SCALE	SHT	OF	REV.
NONE	20	86	



NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_RST#	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_SDIN[0:2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND INTERNAL 20K PD ENABLED WHEN LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

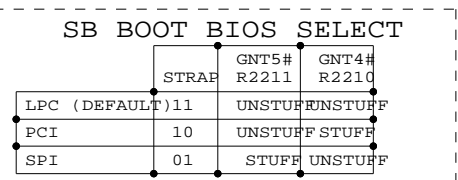
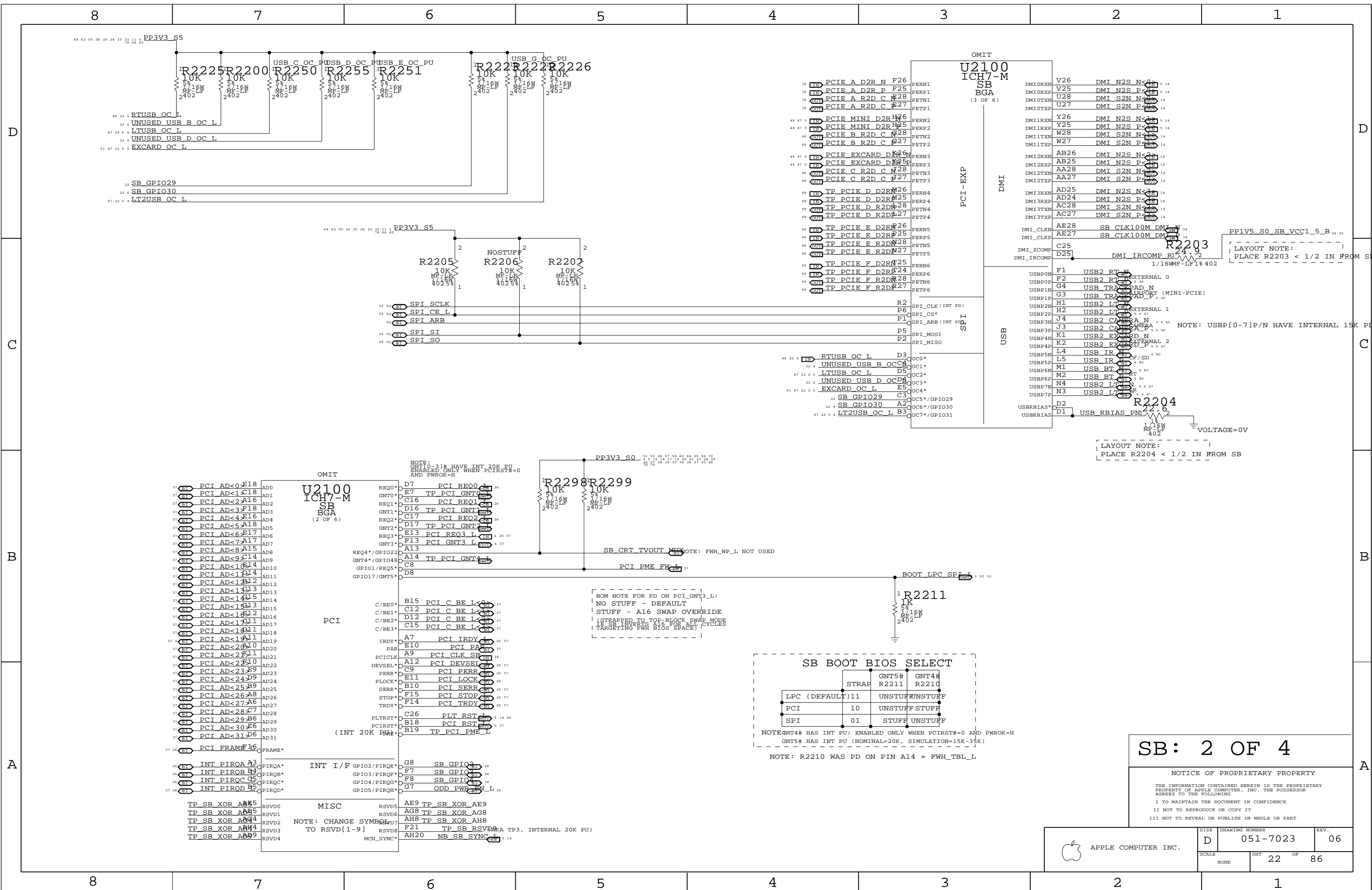
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	06
SCALE	SHT	OF	
NONE	21	86	

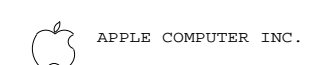


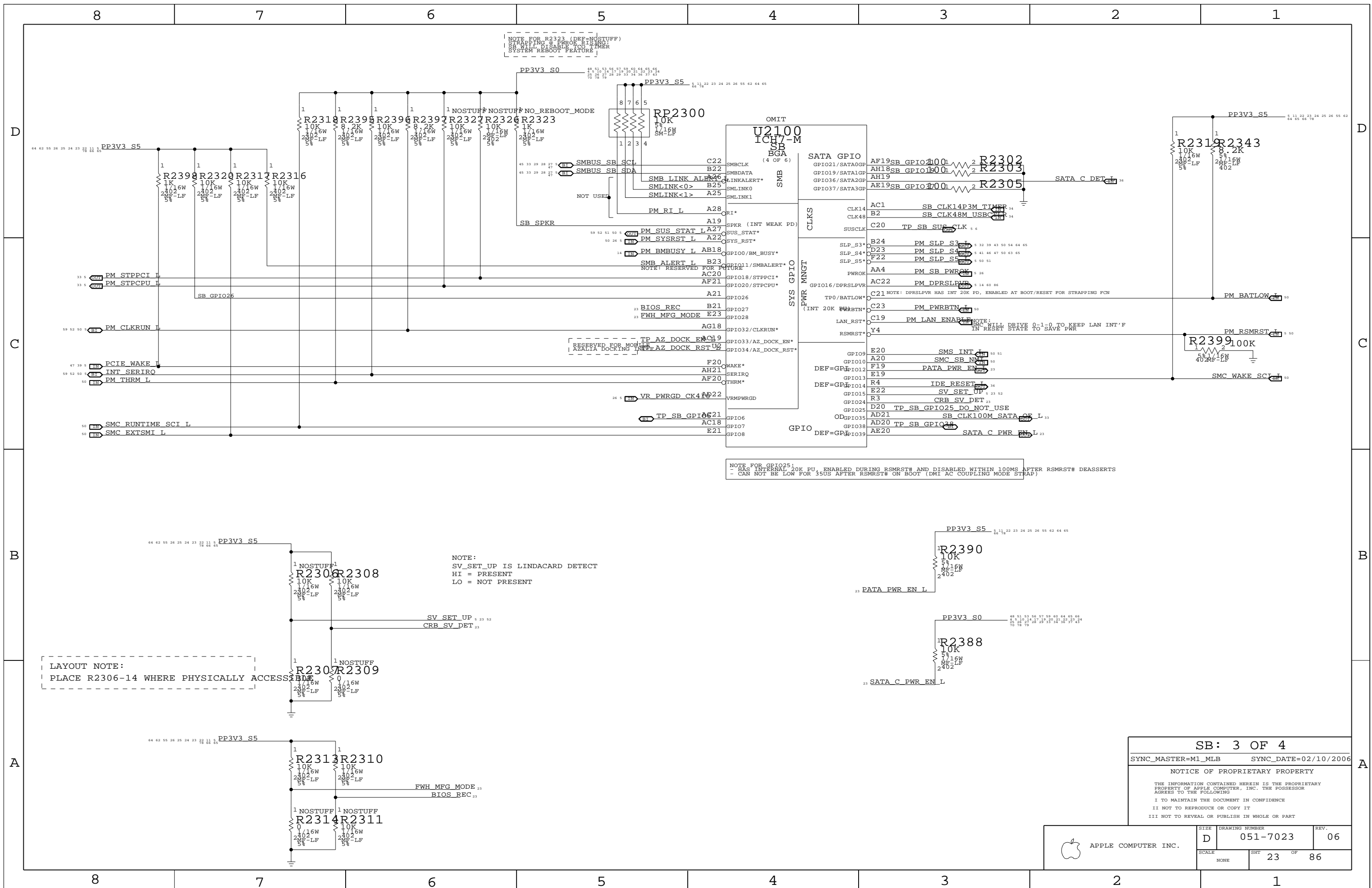
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST# = 0 AND PWROK = 1
 GNT5# HAS INT PU (NOMINAL = 20K, SIMULATION = 15K-35K)
 NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

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SCALE NONE	SHT 22	OF 86	SIZE	DRAWING NUMBER	REV.
			D	051-7023	06





NOTE FOR R2323 (DEF=NOSTUFF)
 STRAPPING @ PWRK RISING:
 SE WILL DISABLE TCO TIMER
 SYSTEM REBOOT FEATURE

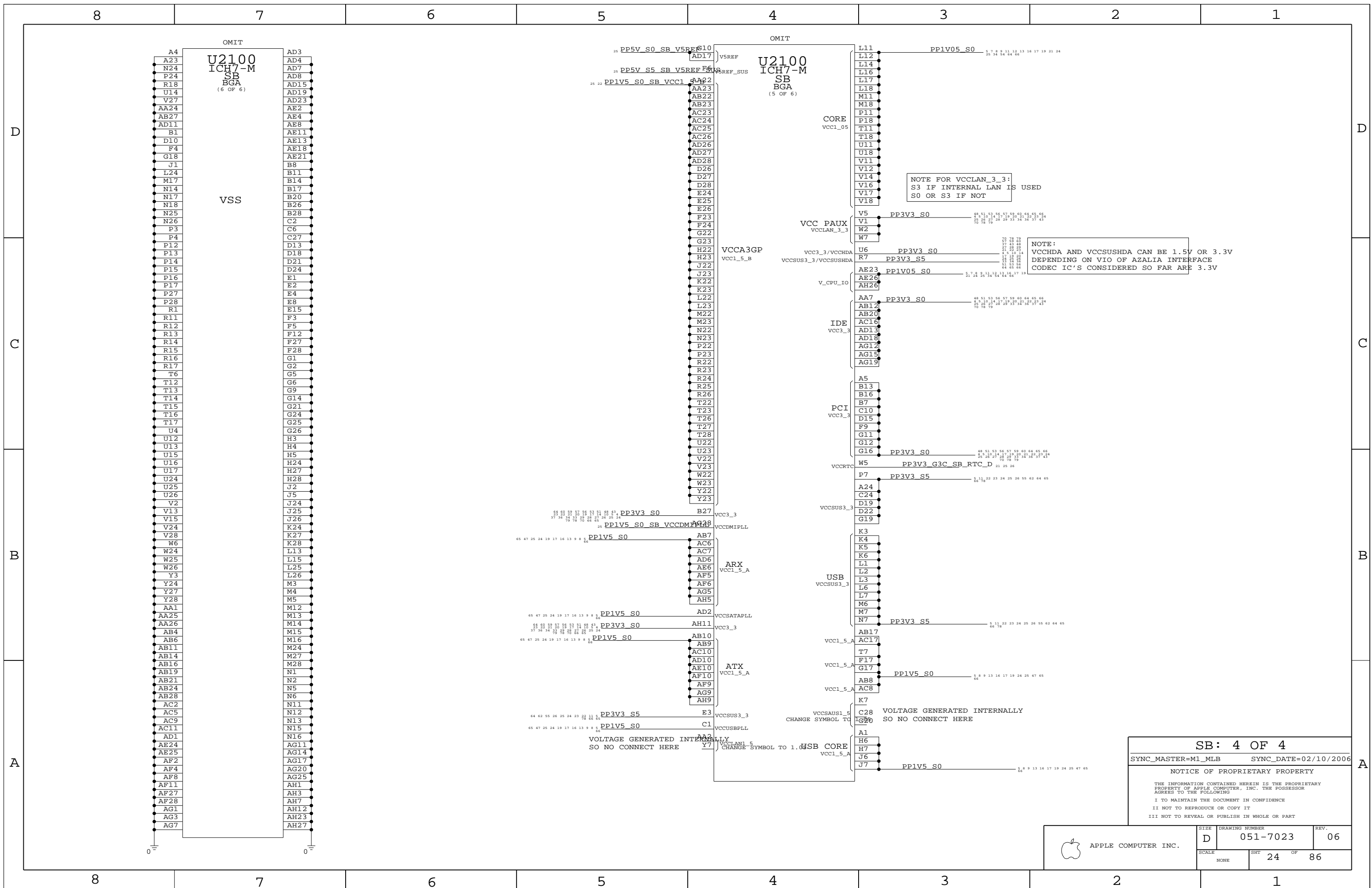
NOTE FOR GPIO25:
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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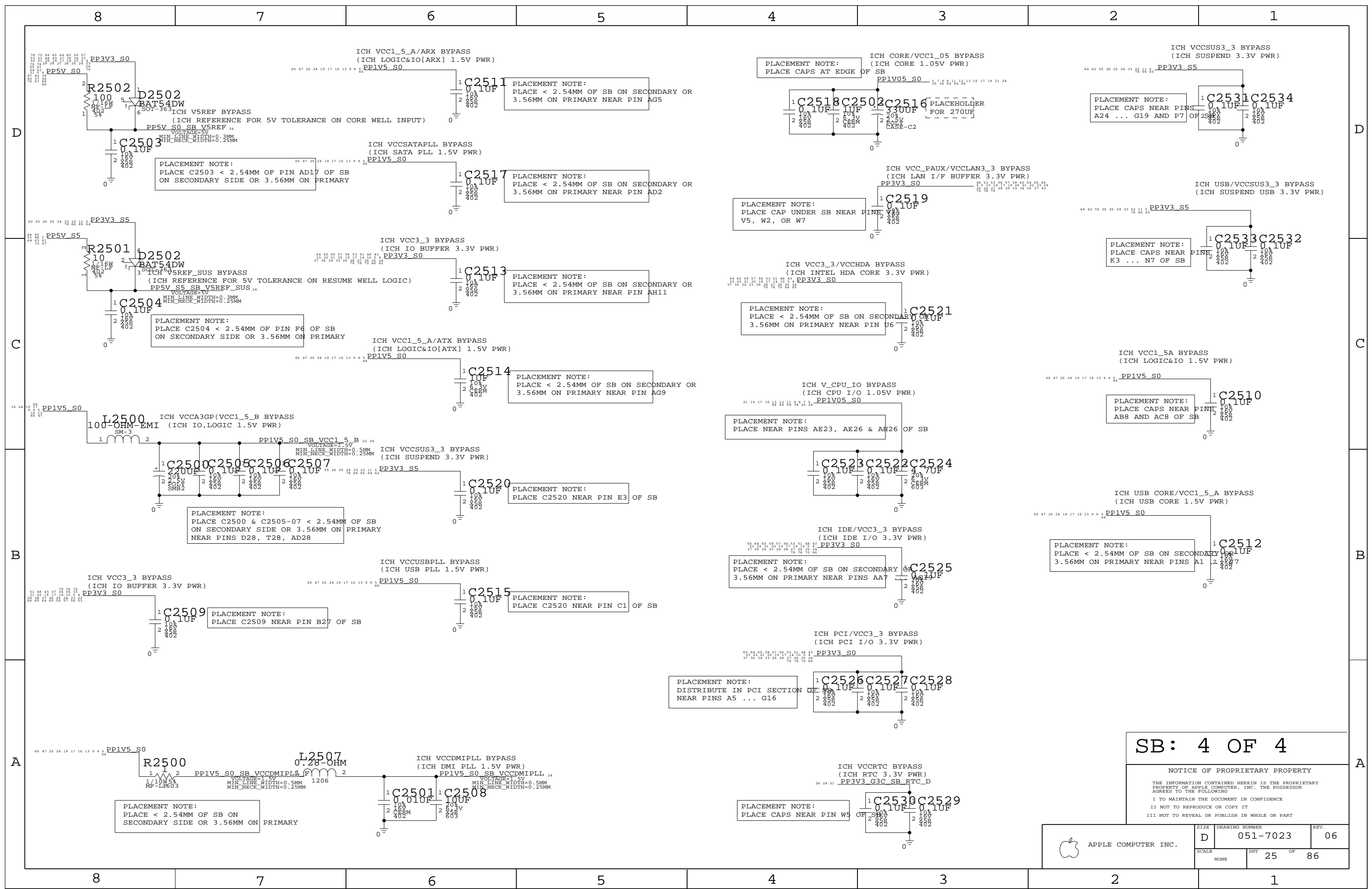
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	NONE	SHT	23 OF 86



SB: 4 OF 4
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	06
SCALE	SHT	OF	
NONE	24	86	

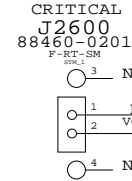


SB: 4 OF 4

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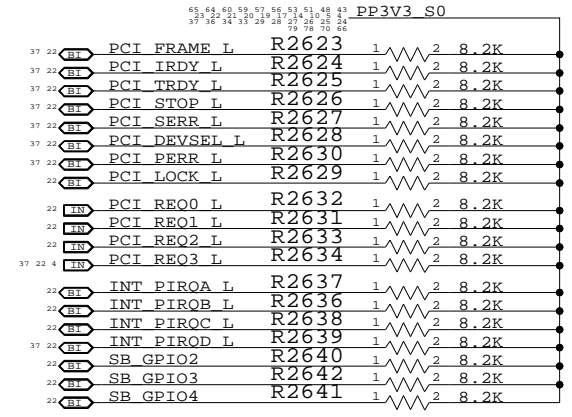
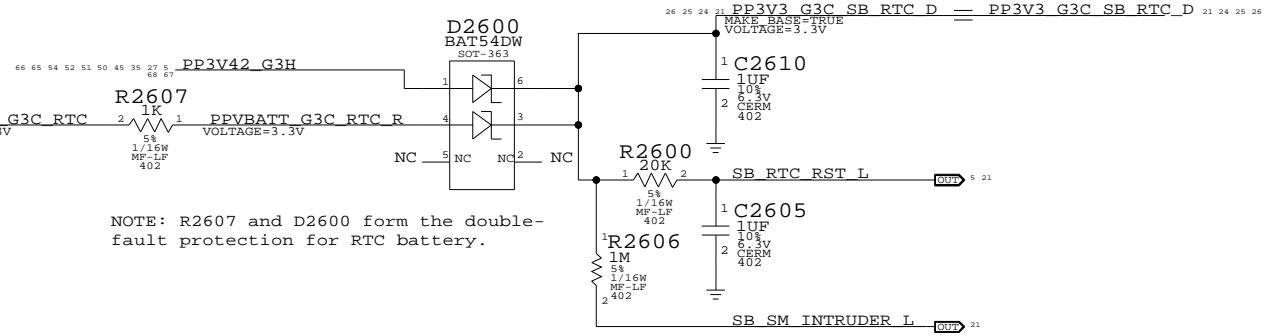
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	25	86	

RTC Battery Connector

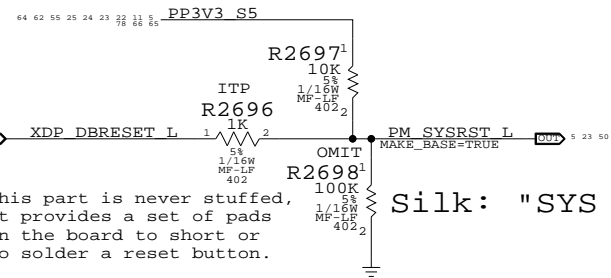
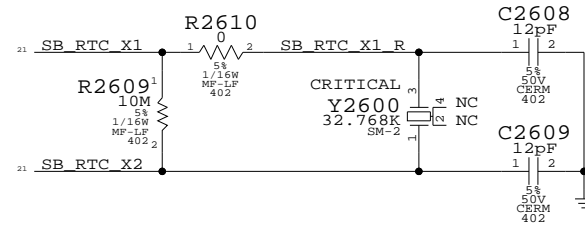


518S0226

NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit

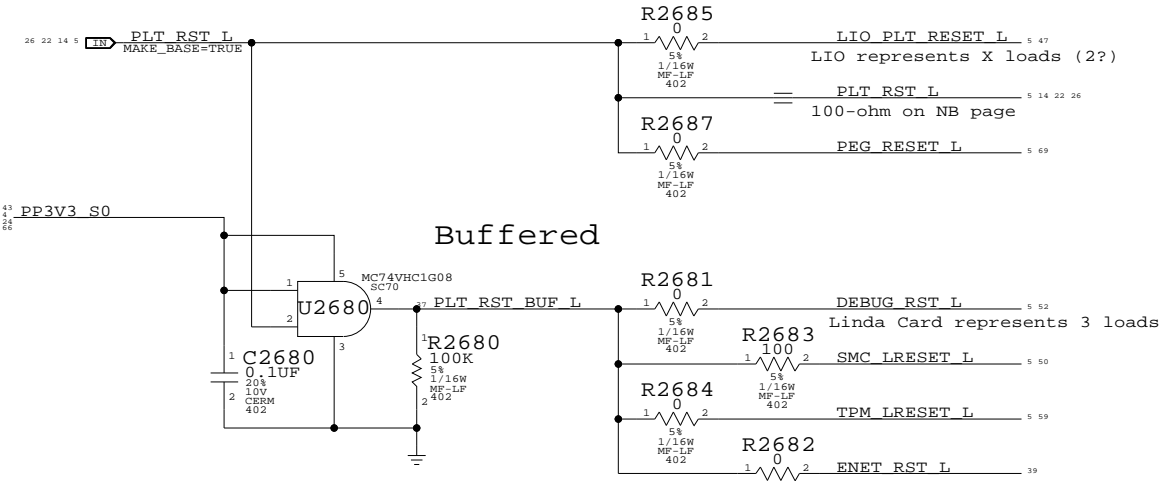


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

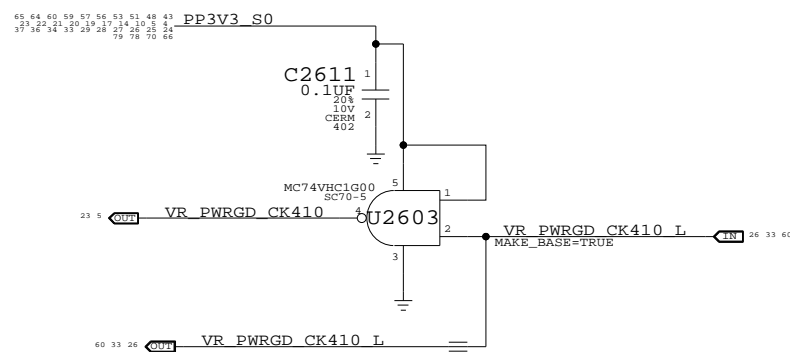
Silk: "SYS RST"

Platform Reset Connections

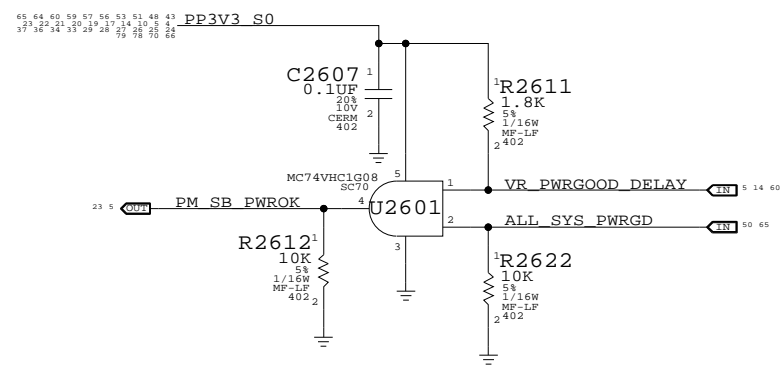
Unbuffered



Initial resistor values are based on CRB, but may change after characterization.

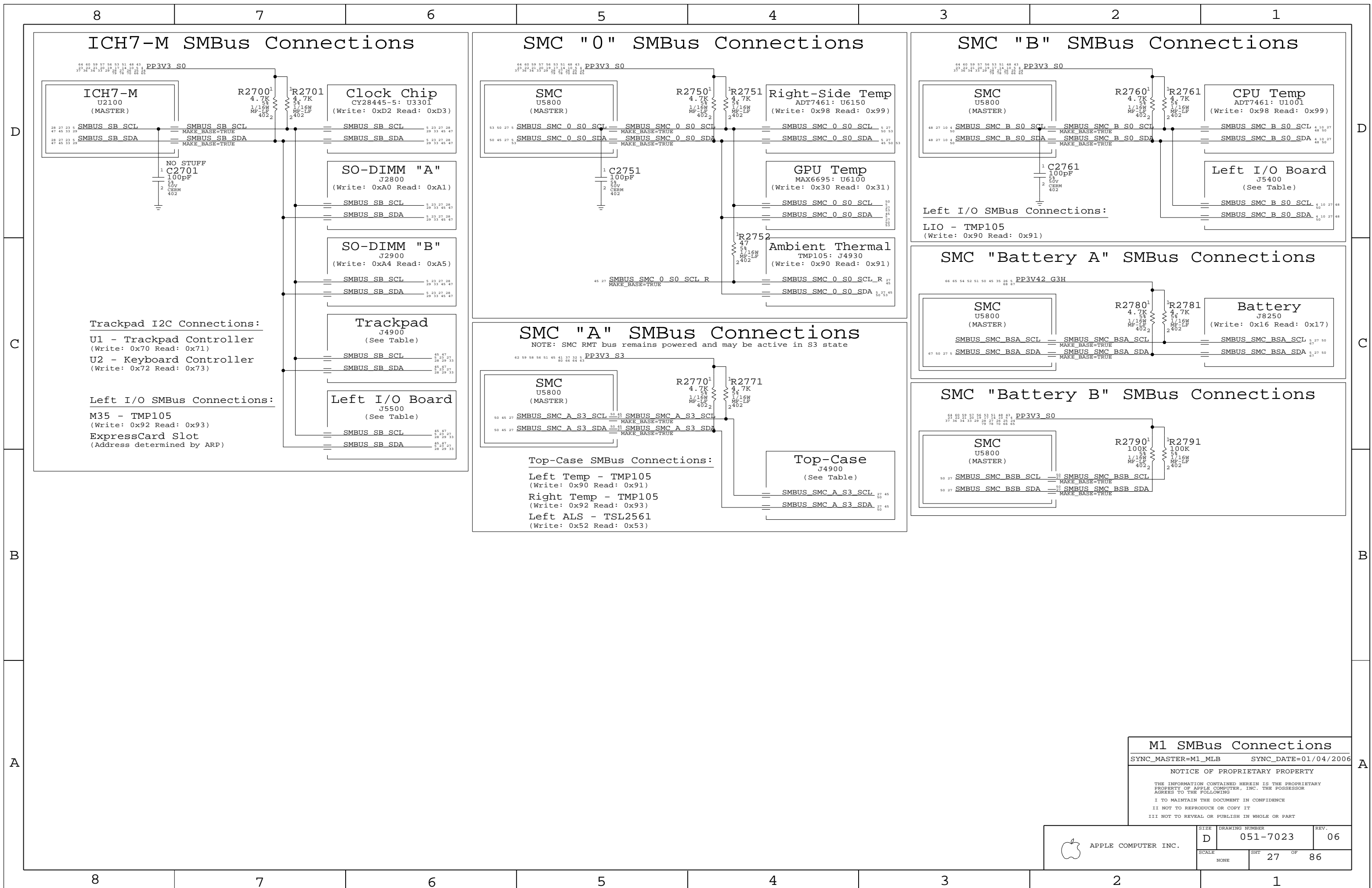


1G00 used as small & cheap inverter



SB Misc		
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006	
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	D	051-7023	06
SCALE	SHT	OF	
NONE	26	86	



M1 SMBus Connections

SYNC_MASTER=M1_MLB SYNC_DATE=01/04/2006

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	D	051-7023	06
SCALE	SHT	OF	
NONE	27	86	

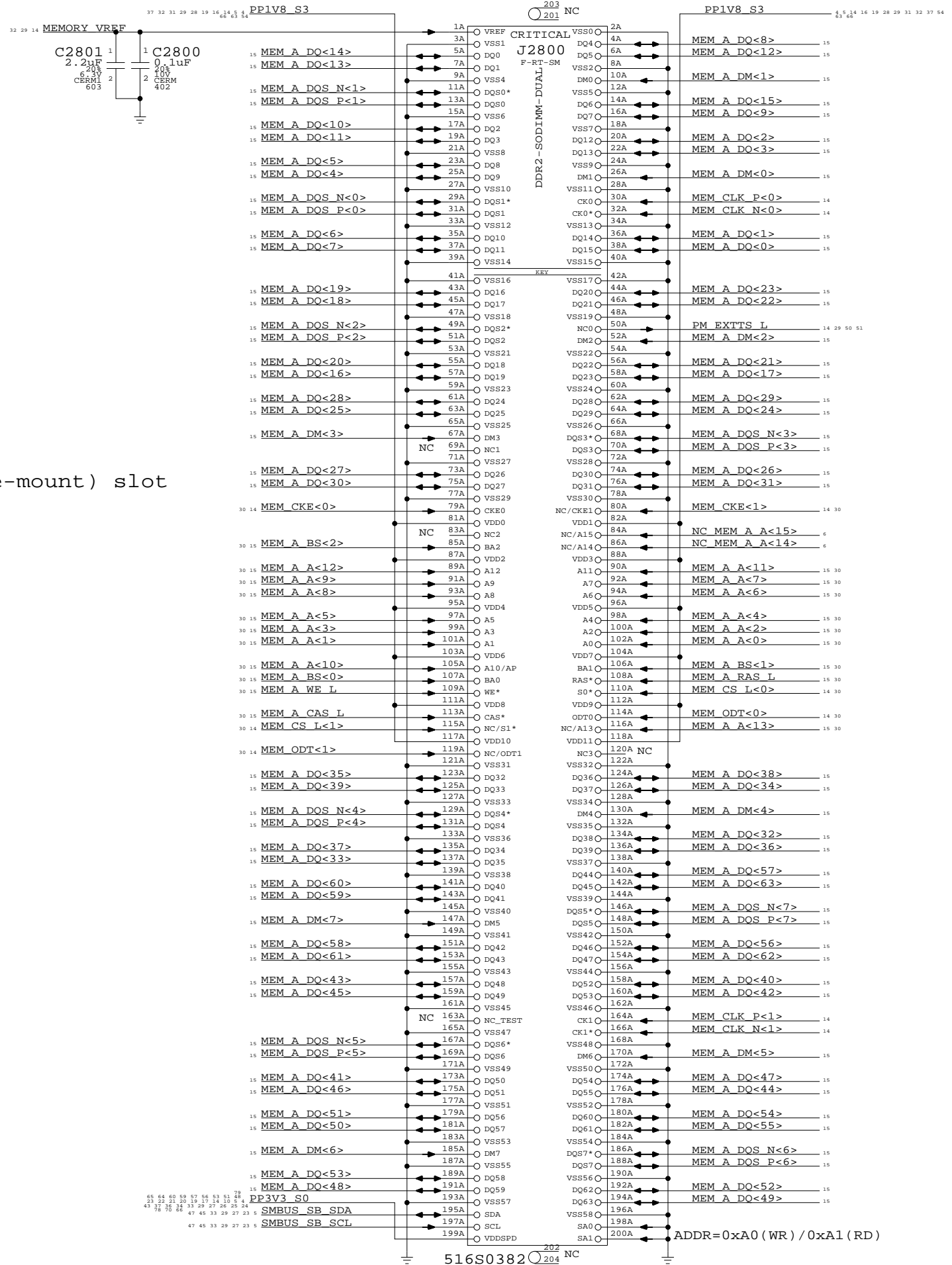
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

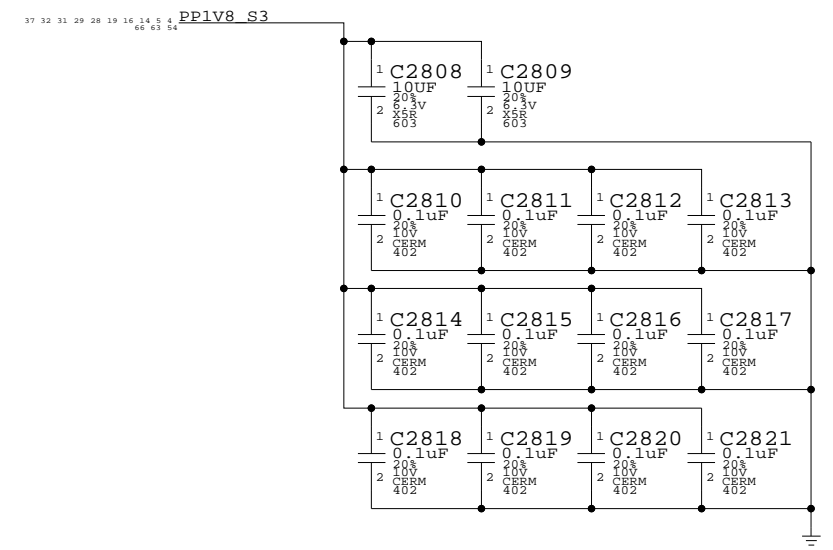
NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



"Lower" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	28	86	06

Page Notes

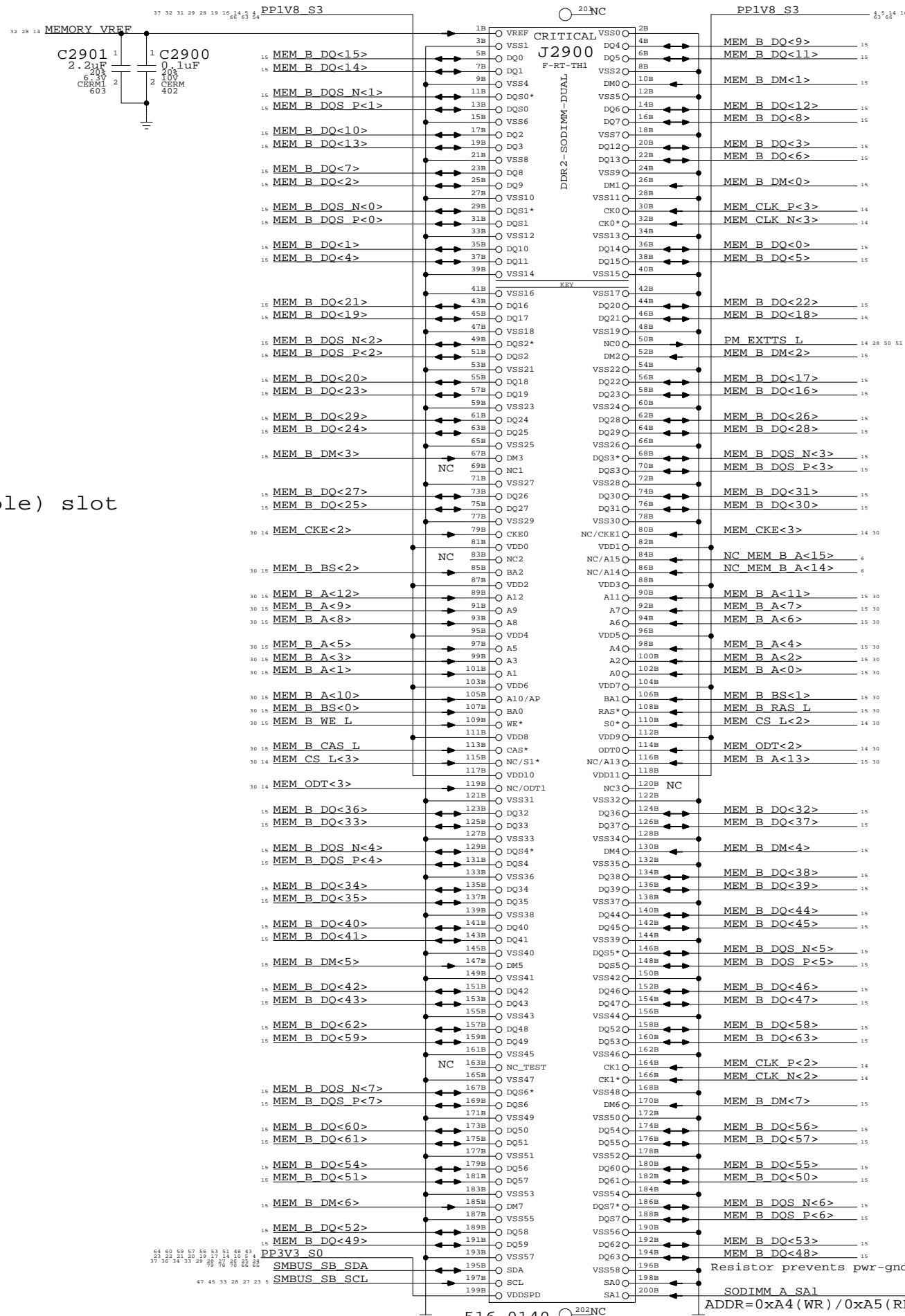
Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

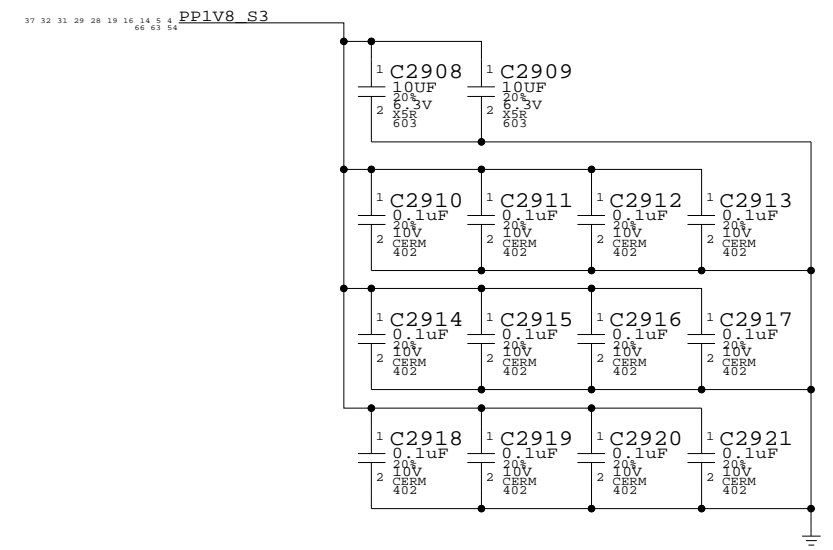
BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.

"Upper" (thru-hole) slot



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. 06
	SCALE NONE	SHT 29	OF 86

8

7

6

5

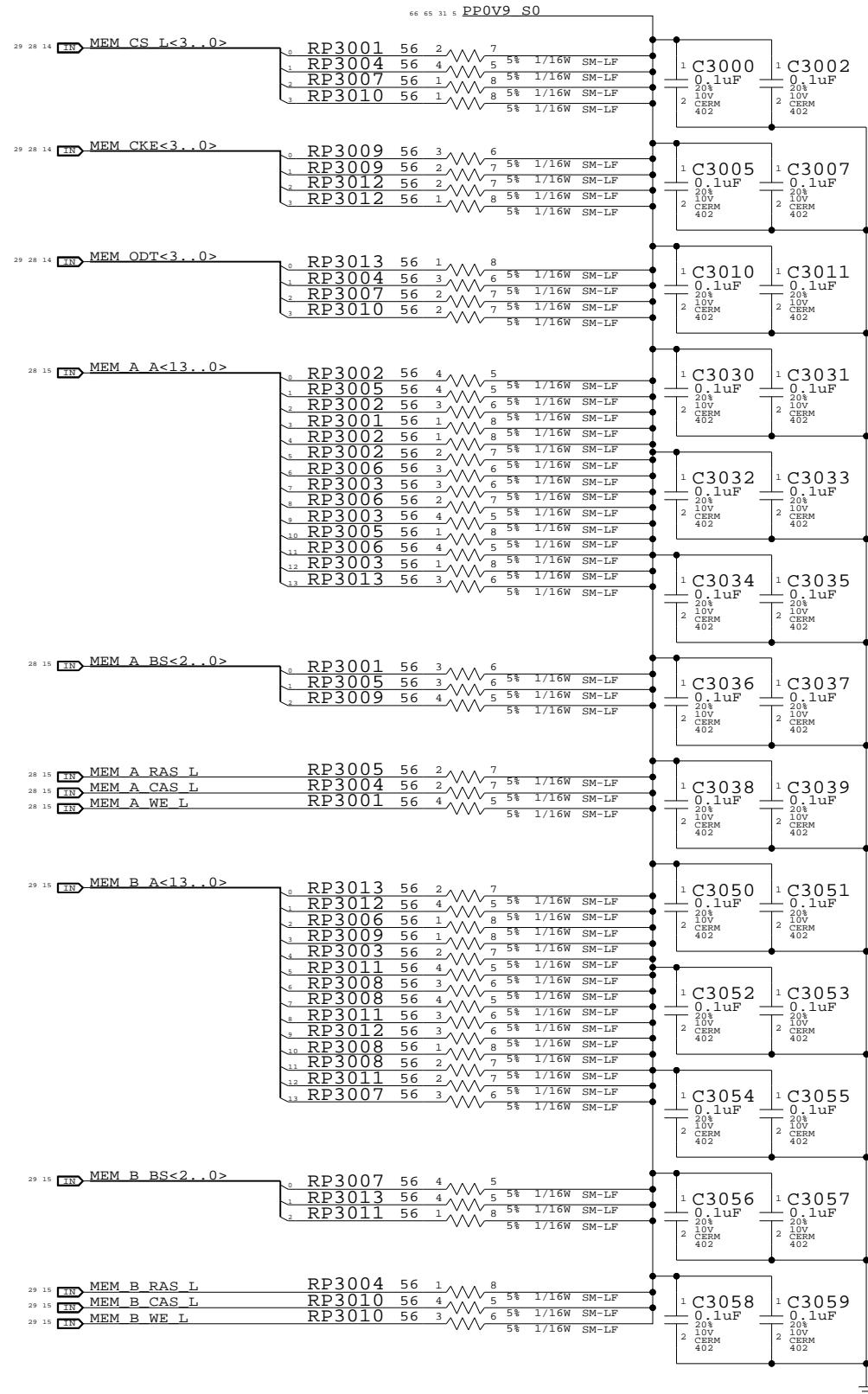
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/07/2006)

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	D	051-7023	06
SCALE	SHT		OF
NONE	30		86

8

7

6

5

4

3

2

1

Page Notes

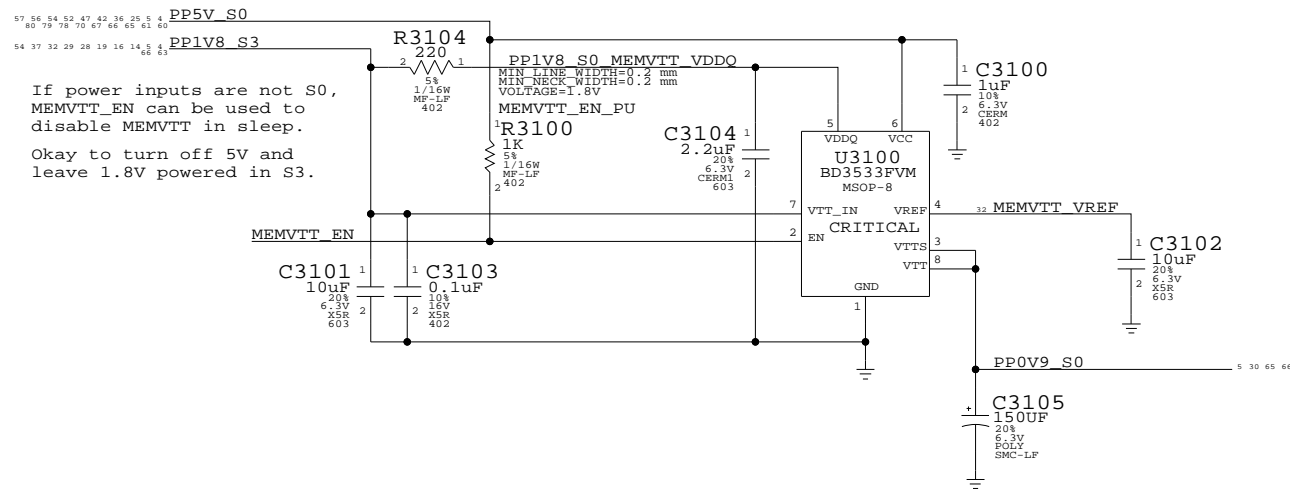
Power aliases required by this page:

- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

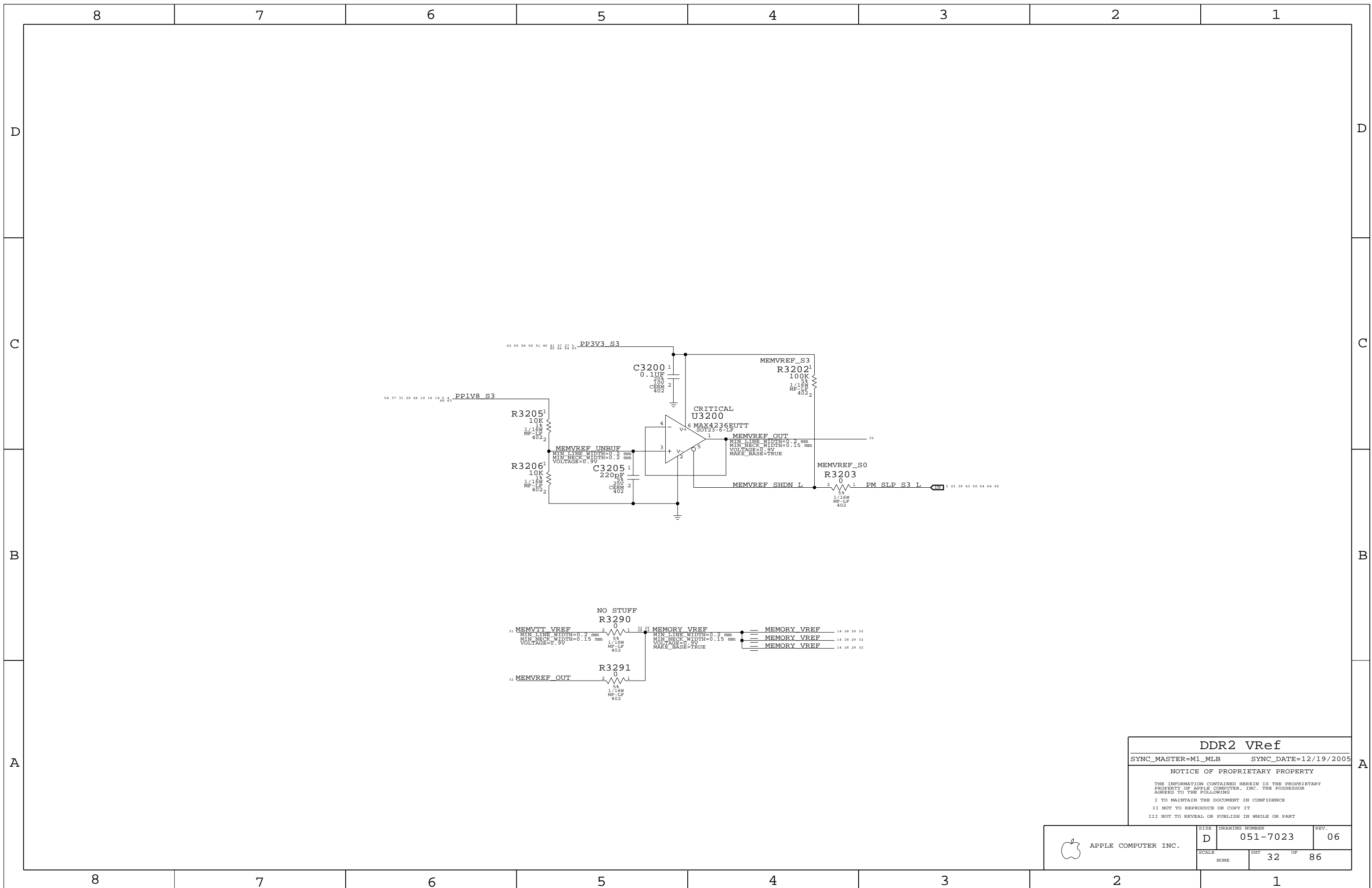
DDR2 Vtt Regulator



If power inputs are not S0,
MEMVTT_EN can be used to
disable MEMVTT in sleep.
Okay to turn off 5V and
leave 1.8V powered in S3.

Memory Vtt Supply
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	31	86	



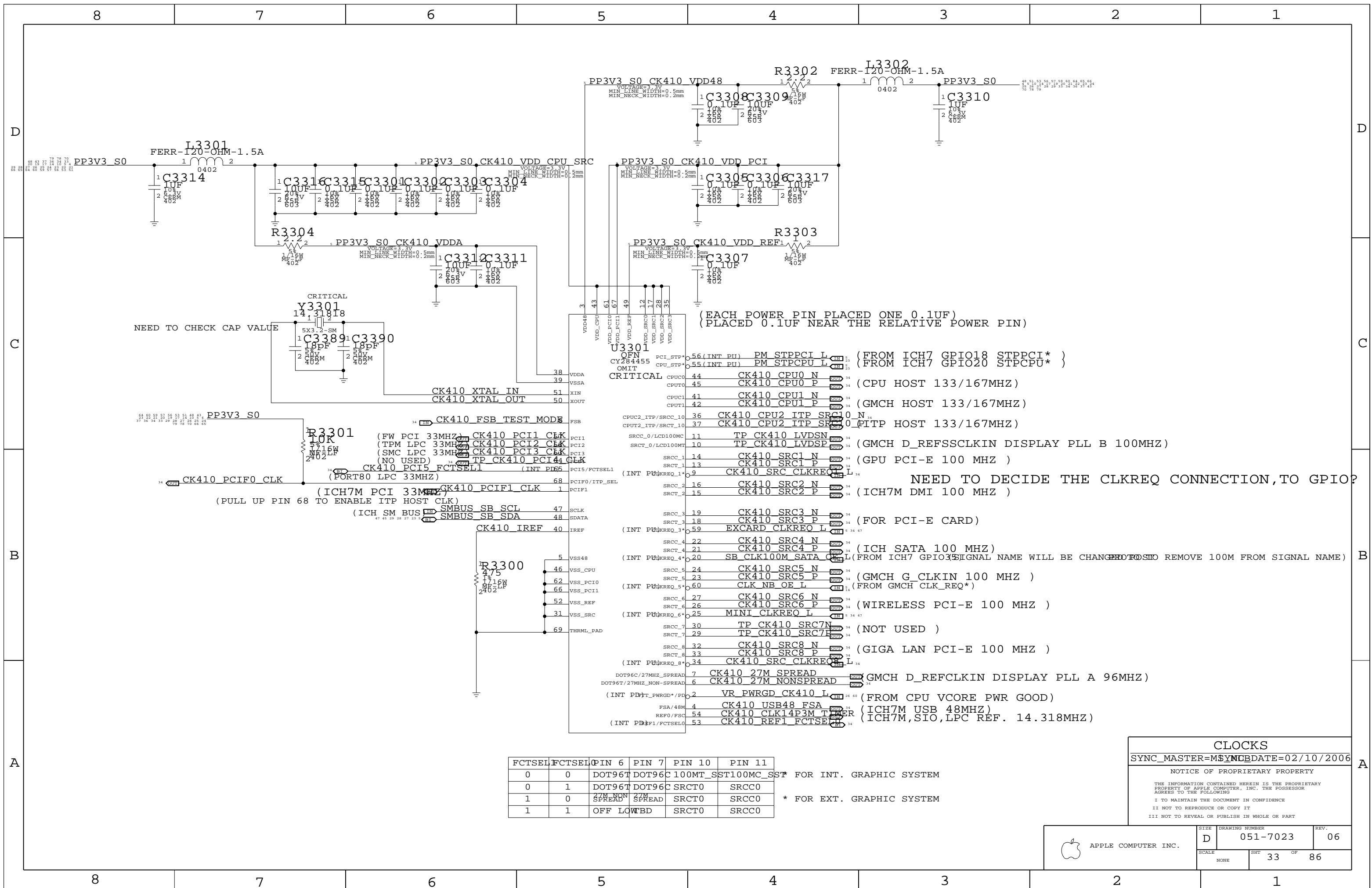
DDR2 Vref
 SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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	SCALE NONE	SHT 32	OF 86



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

NEED TO CHECK CAP VALUE

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?

FCTSEL	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST100MC_SST*		* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON_SPREAD	27M_SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	SRCT0	SRCC0	

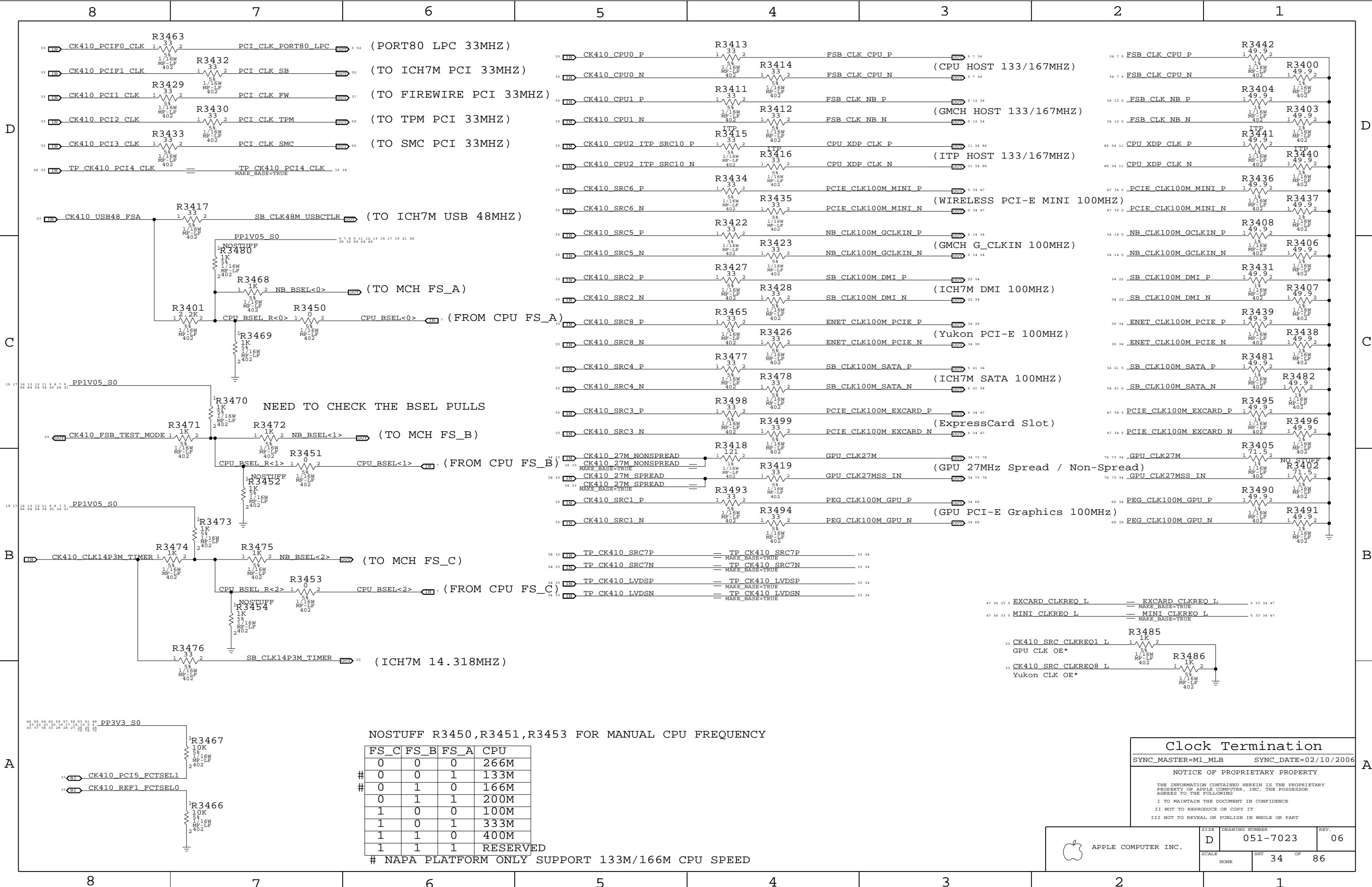
CLOCKS

SYNC_MASTER=MSYNC
DATE=02/10/2006

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NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
0	0	0	0	266M
0	0	1	0	133M
0	1	0	0	166M
0	1	1	0	200M
1	0	0	0	100M
1	0	1	0	333M
1	1	0	0	400M
1	1	1	0	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	34	86	

8

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D

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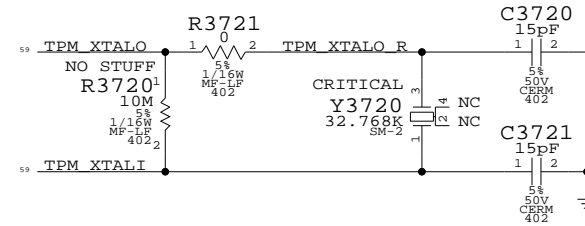
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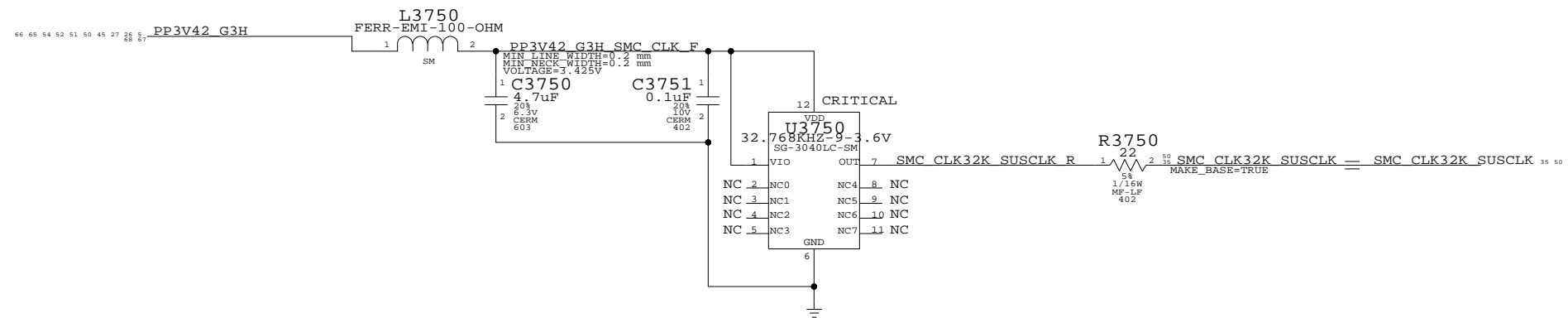
2

1

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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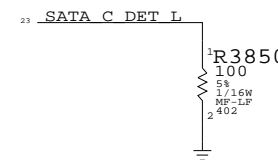
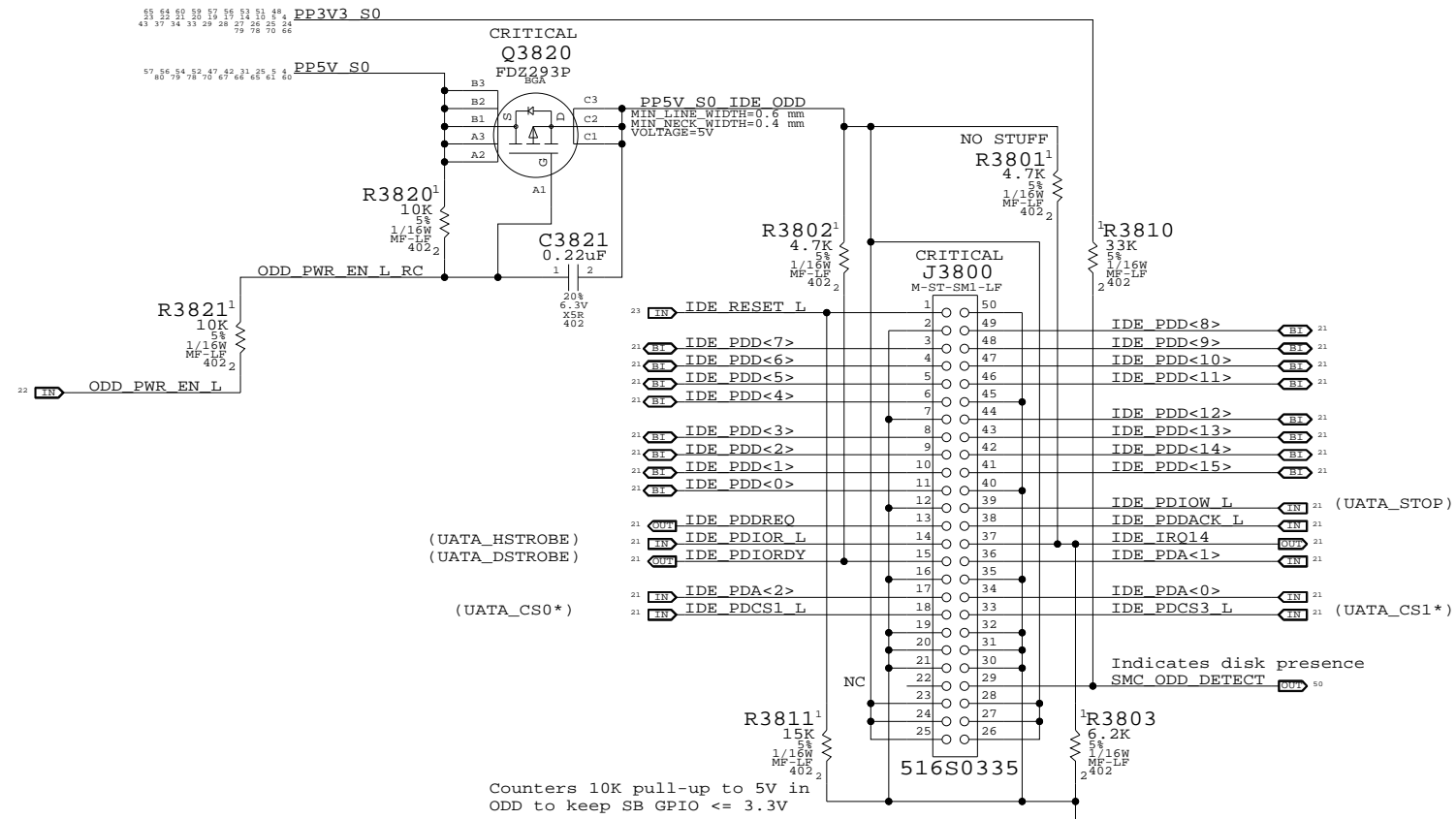
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

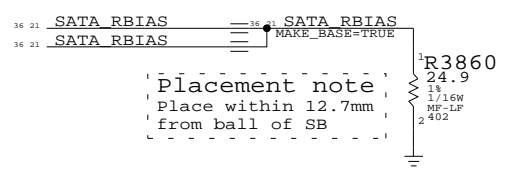
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	NONE	SHT	35 OF 86

IDE (ODD) Connector



- 36 21 TP SATA A R2DP == TP SATA A R2DP 21 36
MAKE_BASE=TRUE
- 36 21 TP SATA A R2DN == TP SATA A R2DN 21 36
MAKE_BASE=TRUE
- 36 21 TP SATA A D2RP == TP SATA A D2RP 21 36
MAKE_BASE=TRUE
- 36 21 TP SATA A D2RN == TP SATA A D2RN 21 36
MAKE_BASE=TRUE



PATA Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

NOTICE OF PROPRIETARY PROPERTY

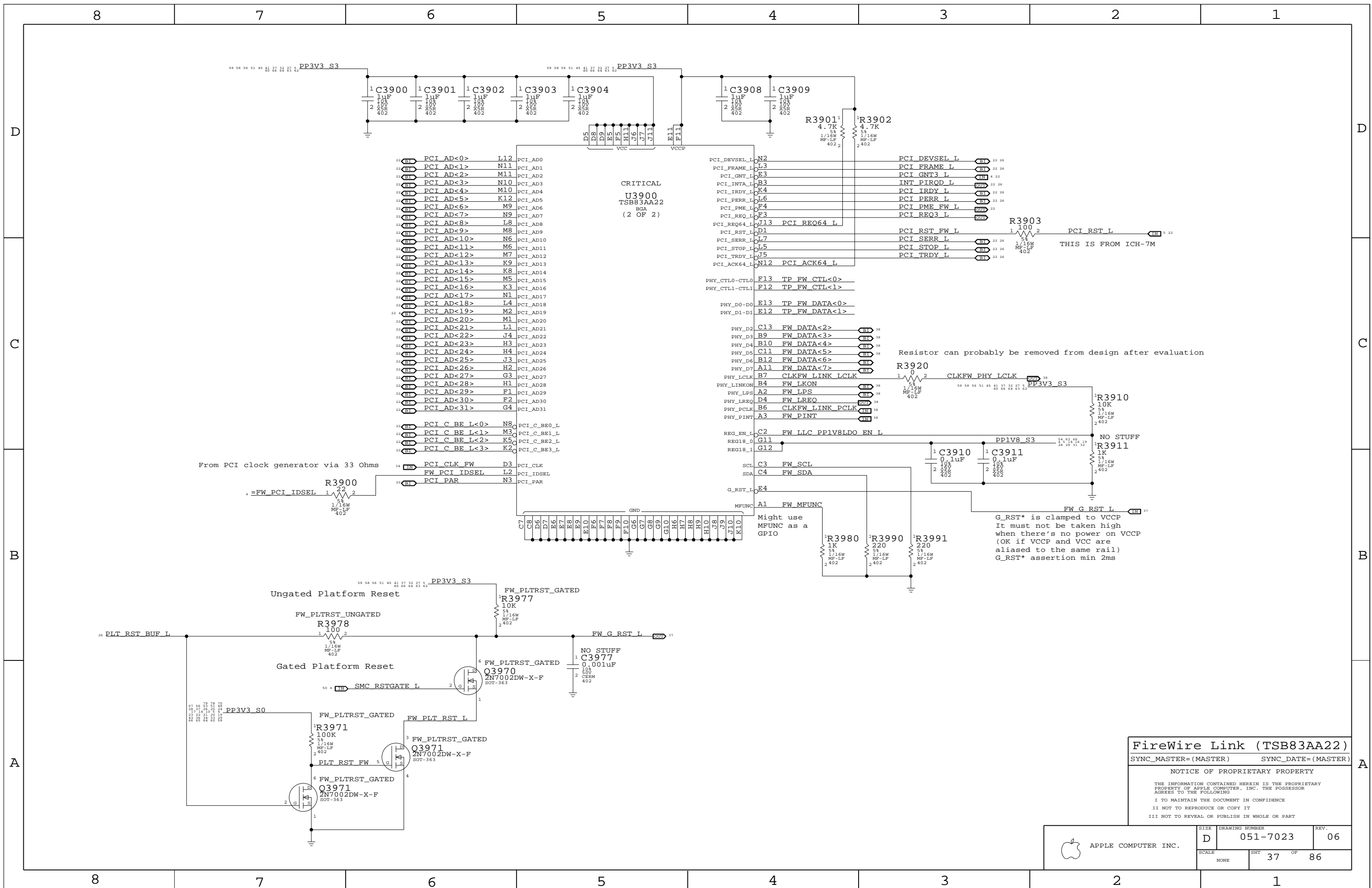
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	D	051-7023	06
SCALE	SHT	OF	REV.
NONE	36	86	



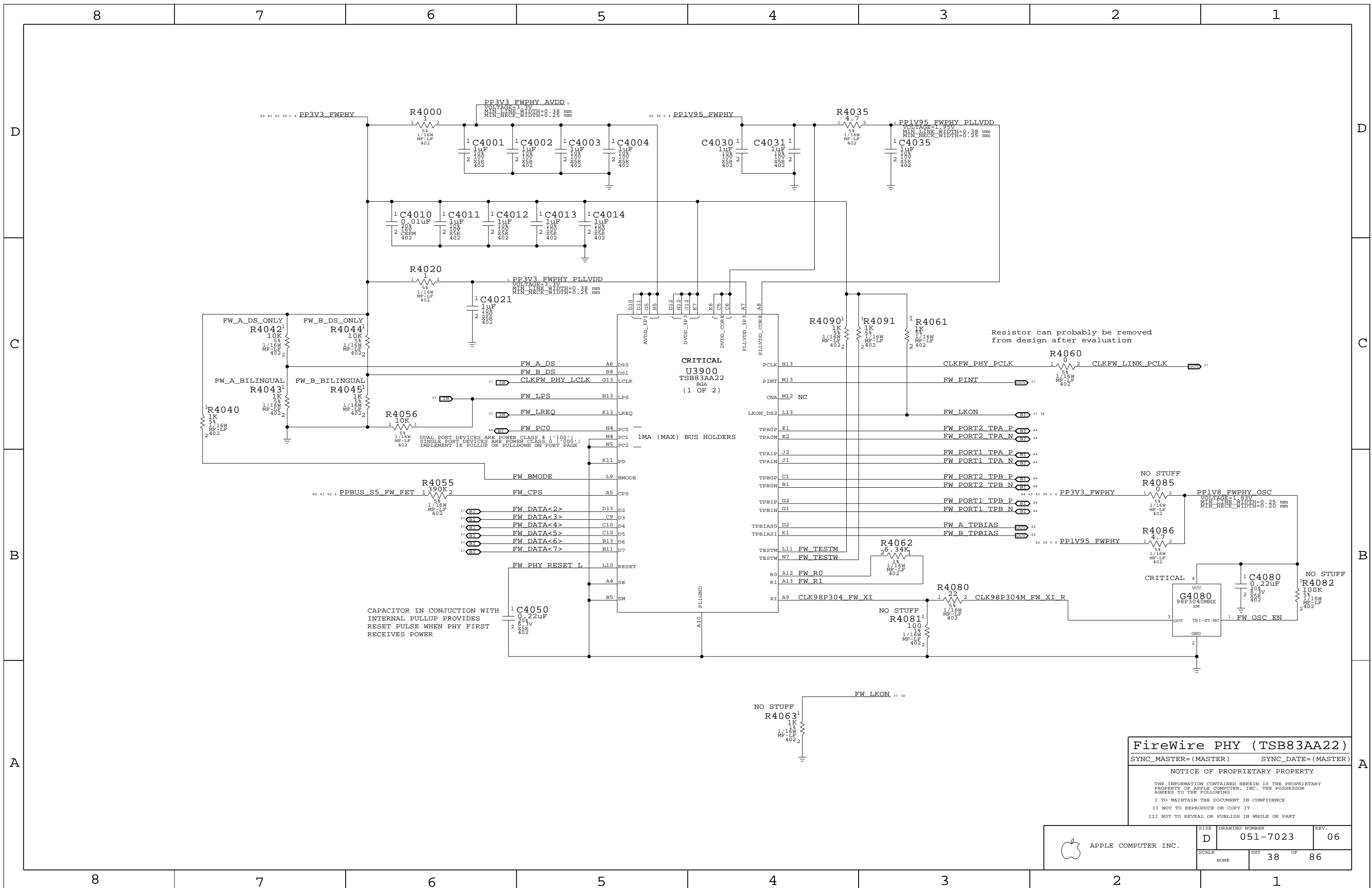
FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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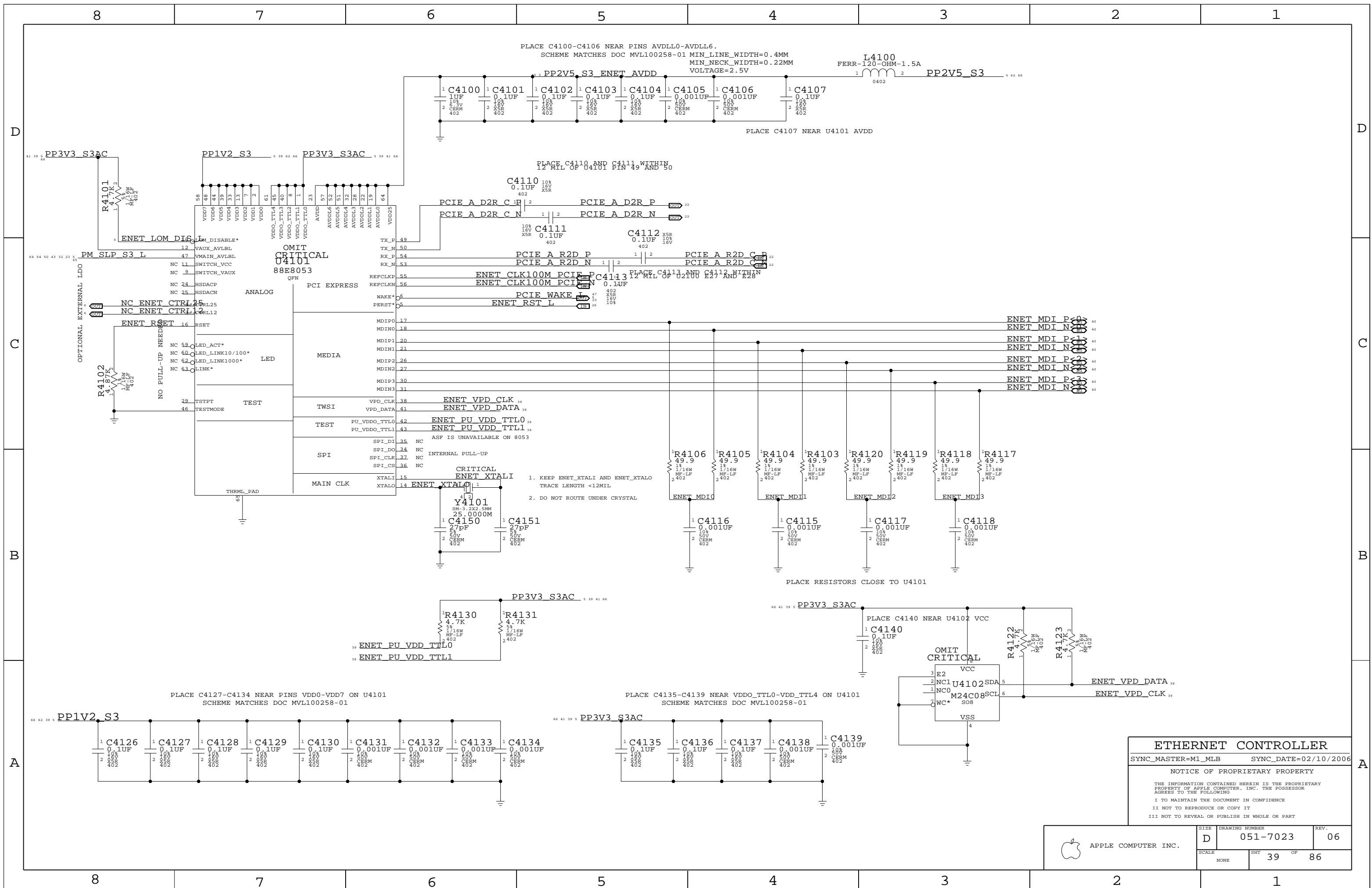
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT 37 OF 86		
NONE			



FireWire PHY (TSB83AA22)
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7023	06
SCALE	NONE	SHT	38 OF 86



ETHERNET CONTROLLER
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. 06
	SCALE NONE	SHEET 39	OF 86

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	SPACING	PHYSICAL
PROVIDED	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
BY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
ETHERNET	ENETCONN	ENET_100D
	ENETCONN	ENET_100D
PHY	ENETCONN	ENET_100D
	ENETCONN	ENET_100D

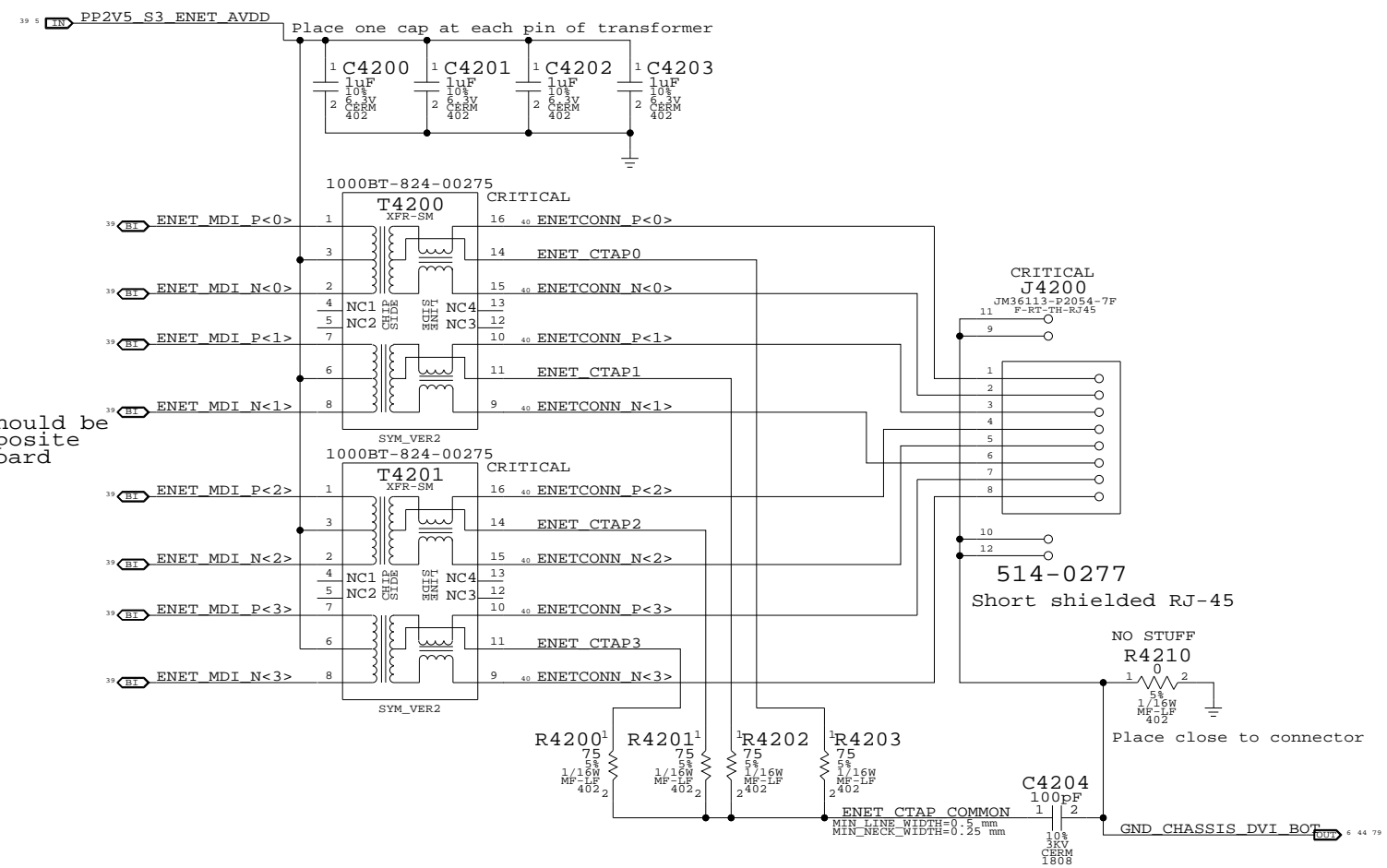
Page Notes

Power aliases required by this page:
 - =PP2V5_ENET
 - =GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

NOTICE OF PROPRIETARY PROPERTY

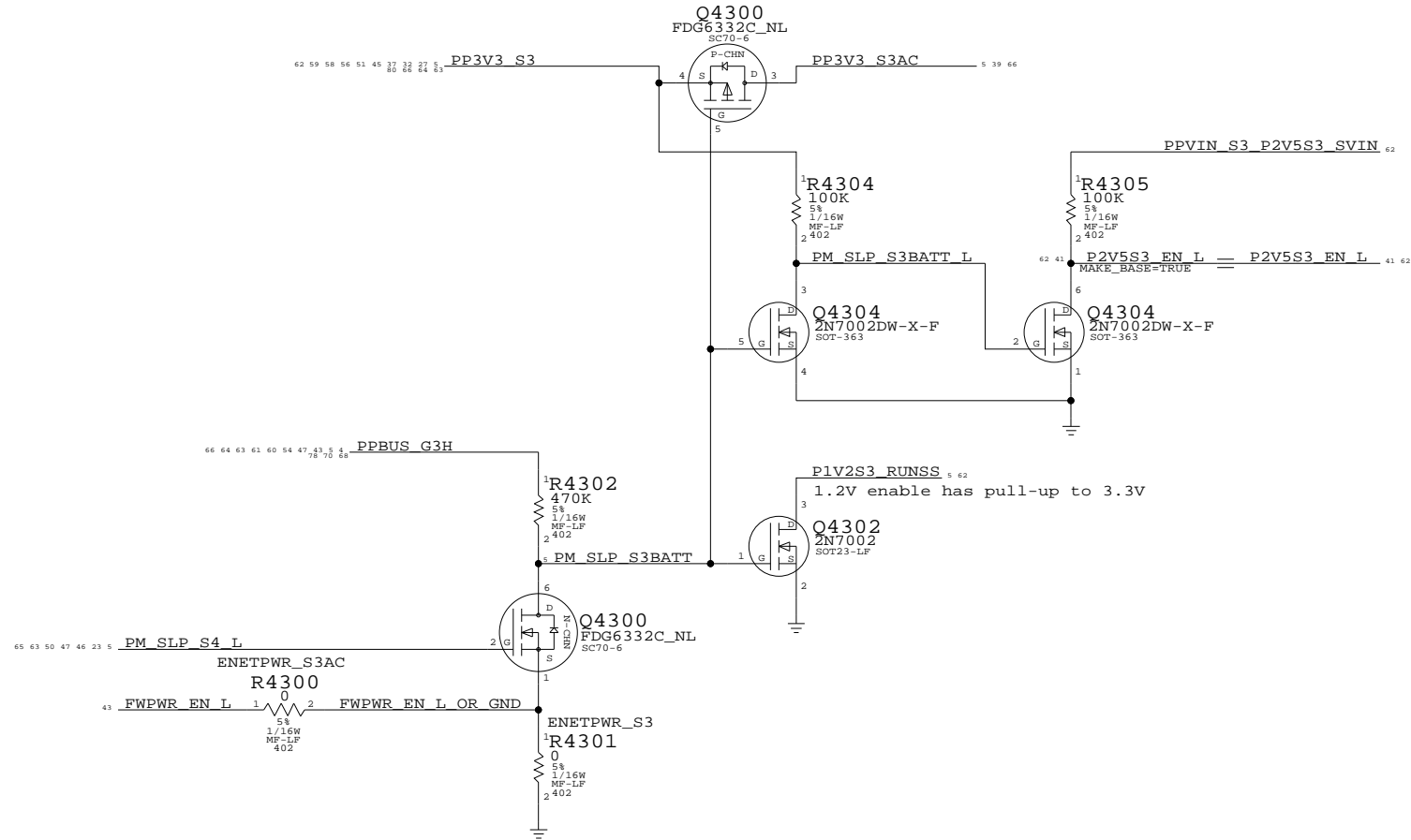
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	D	051-7023	06
SCALE	SHT	OF	
NONE	40	86	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

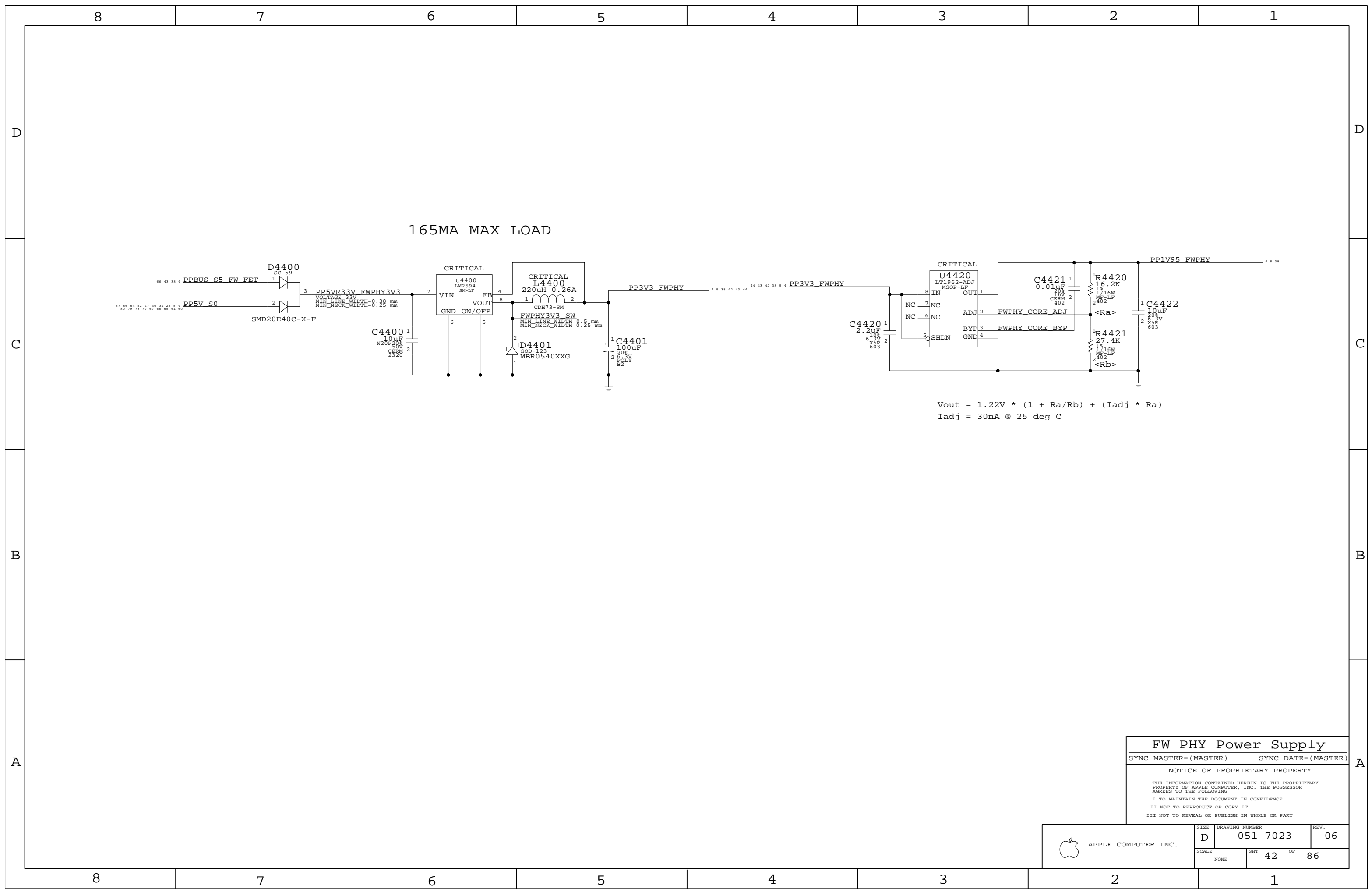
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	06
SCALE	SHT	OF	
NONE	41	86	



$$V_{out} = 1.22V * (1 + R_a/R_b) + (I_{adj} * R_a)$$

$$I_{adj} = 30nA @ 25 \text{ deg C}$$

FW PHY Power Supply
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	42	86	

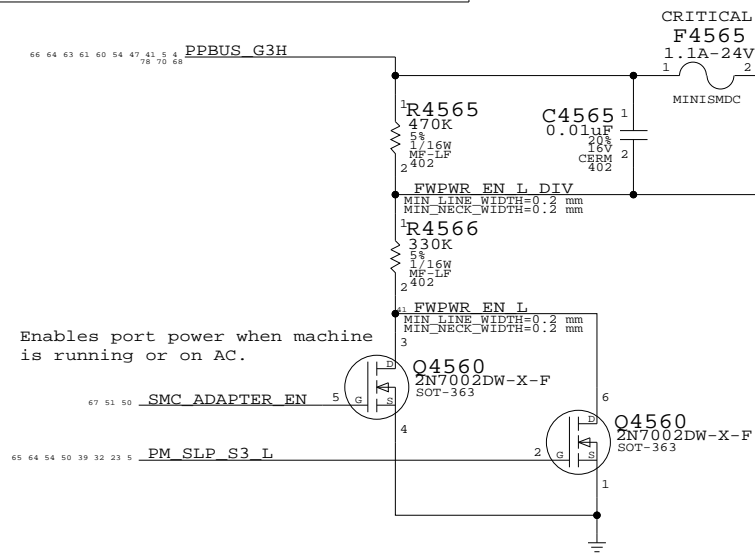
Page Notes

Power aliases required by this page:
 - =PPBUS_S0_FWPWRSW (system supply for bus power)
 - =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
 - =FWPWR_PWRON (see related text note below)

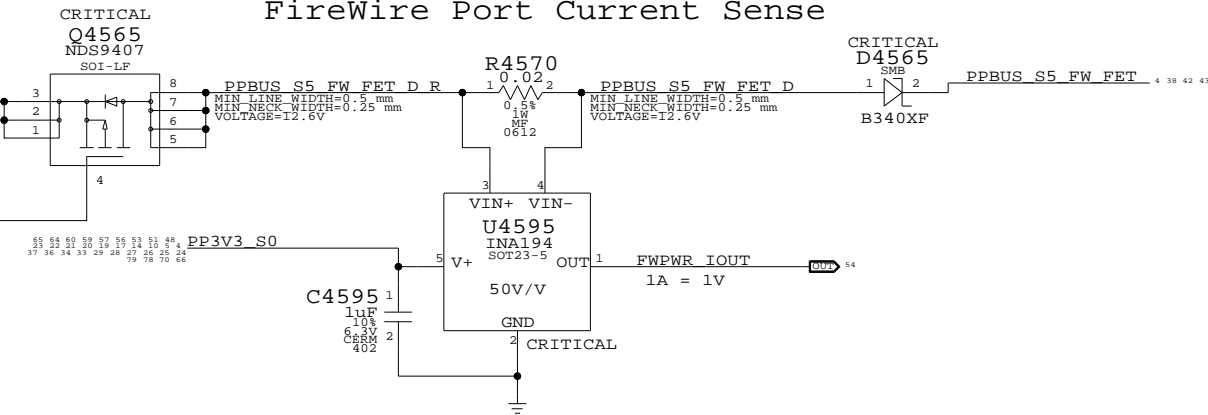
BOM options provided by this page:
 (NONE)

Port Power Switch



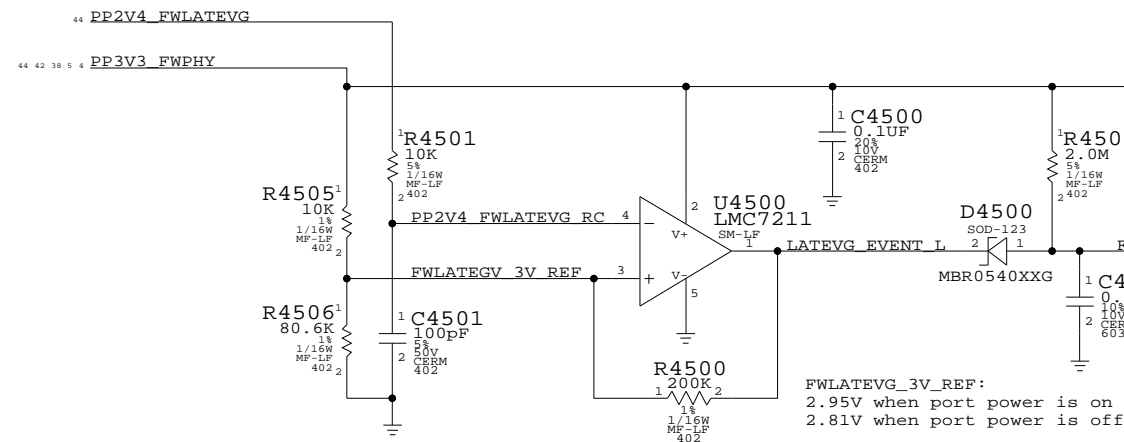
Enables port power when machine is running or on AC.

FireWire Port Current Sense

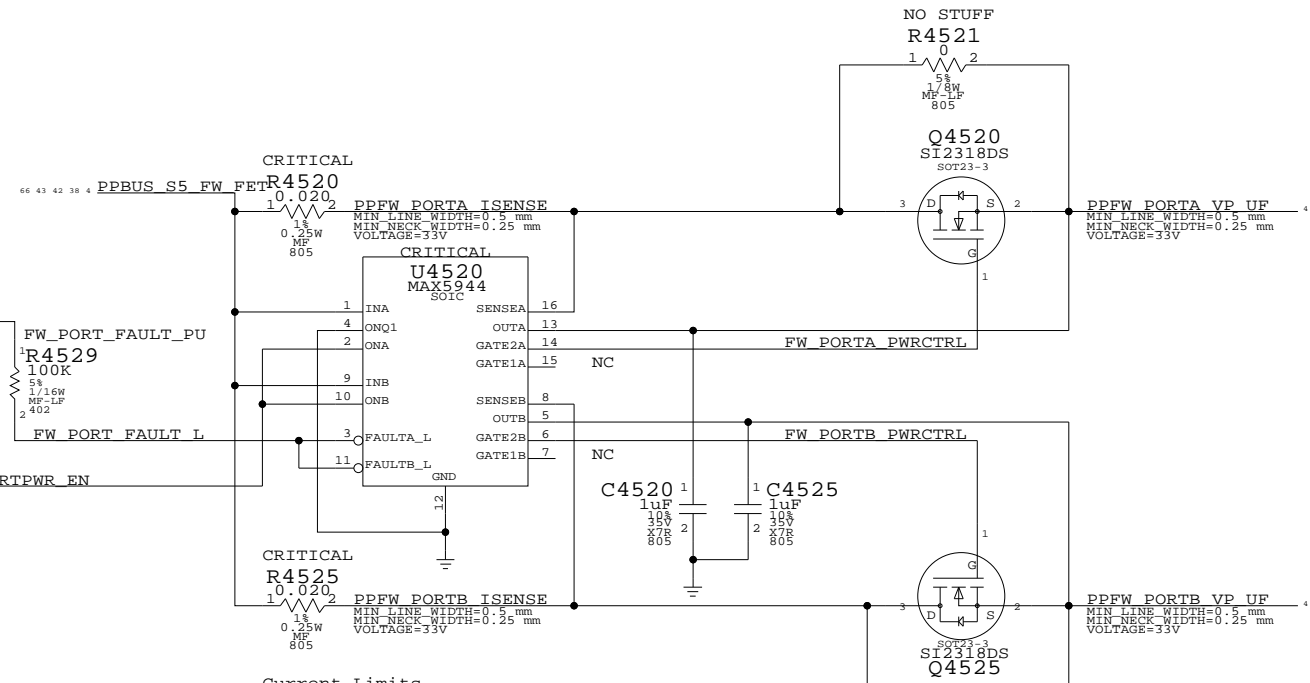


Current Limit/Active Late-VG Protection

Late-VG Event Detection



FWLATEVG_3V_REF:
 2.95V when port power is on
 2.81V when port power is off



Current Limits

- 0.020 ohm => 2.4A
- 0.025 ohm => 2A
- 0.030 ohm => 1.66A (Ideal)
- 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/03/2005)

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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	43	86	06

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
PROVIDED	FW	FW_110D
BY	FW	FW_110D
PHY	FW	FW_110D
PAGE	FW	FW_110D

Page Notes

Power aliases required by this page:
 - =PPFW_PORT1
 - =PP3V3_S5_FWLATEVG
 - =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

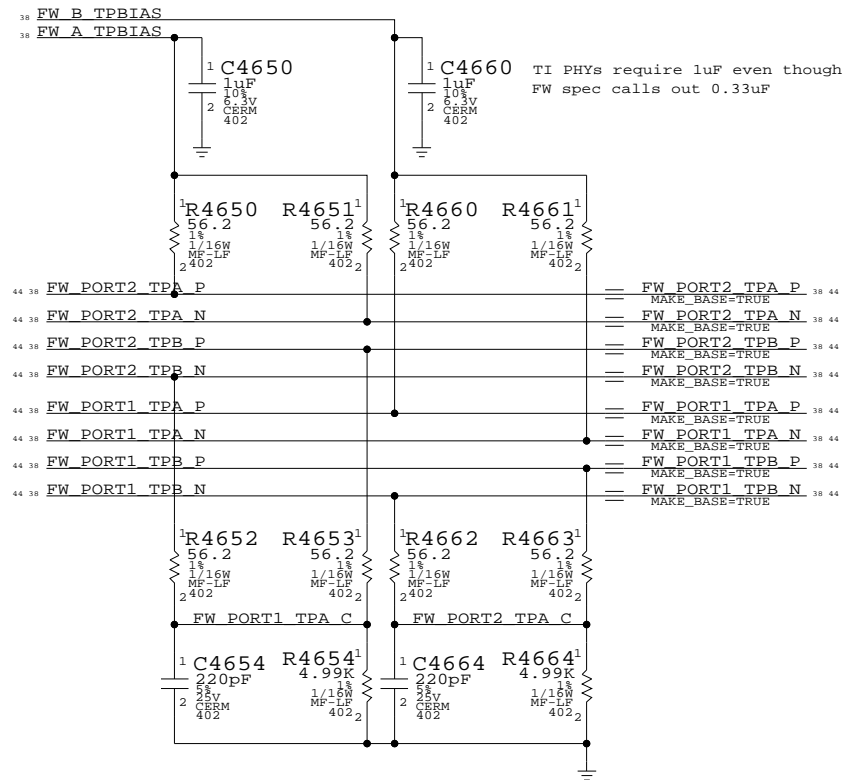
AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

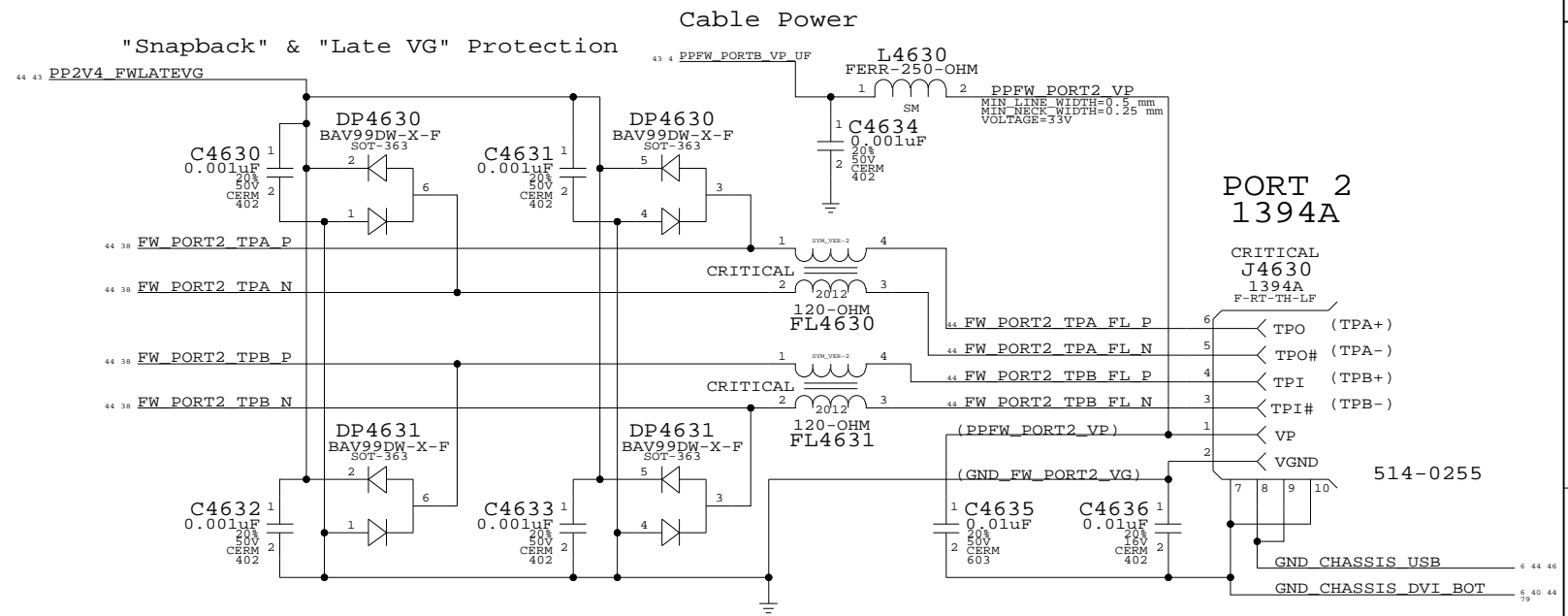
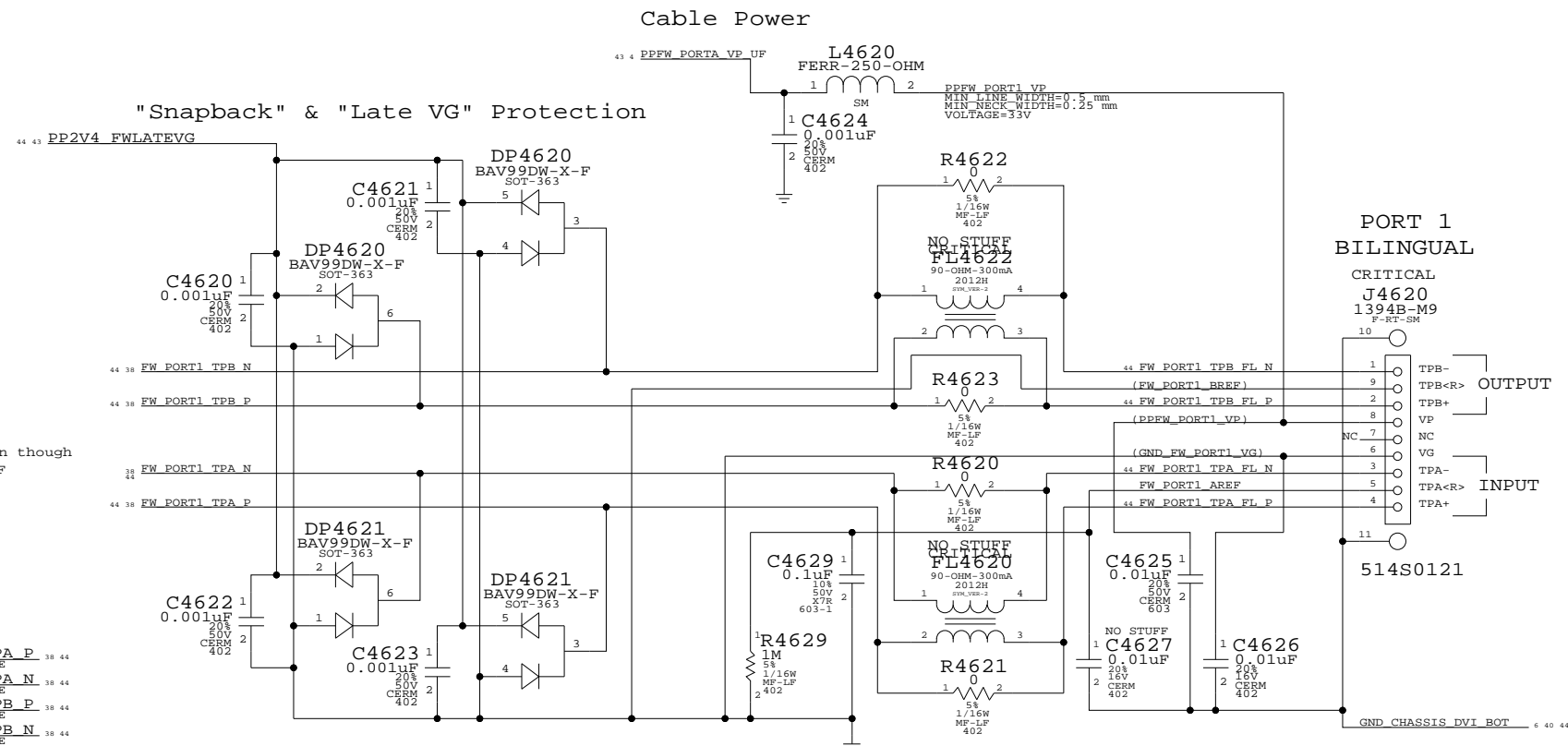
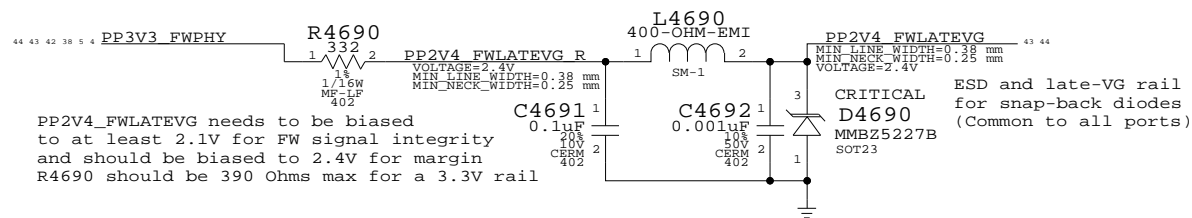
BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Termination

Place close to FireWire PHY



Late-VG Protection Power



FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

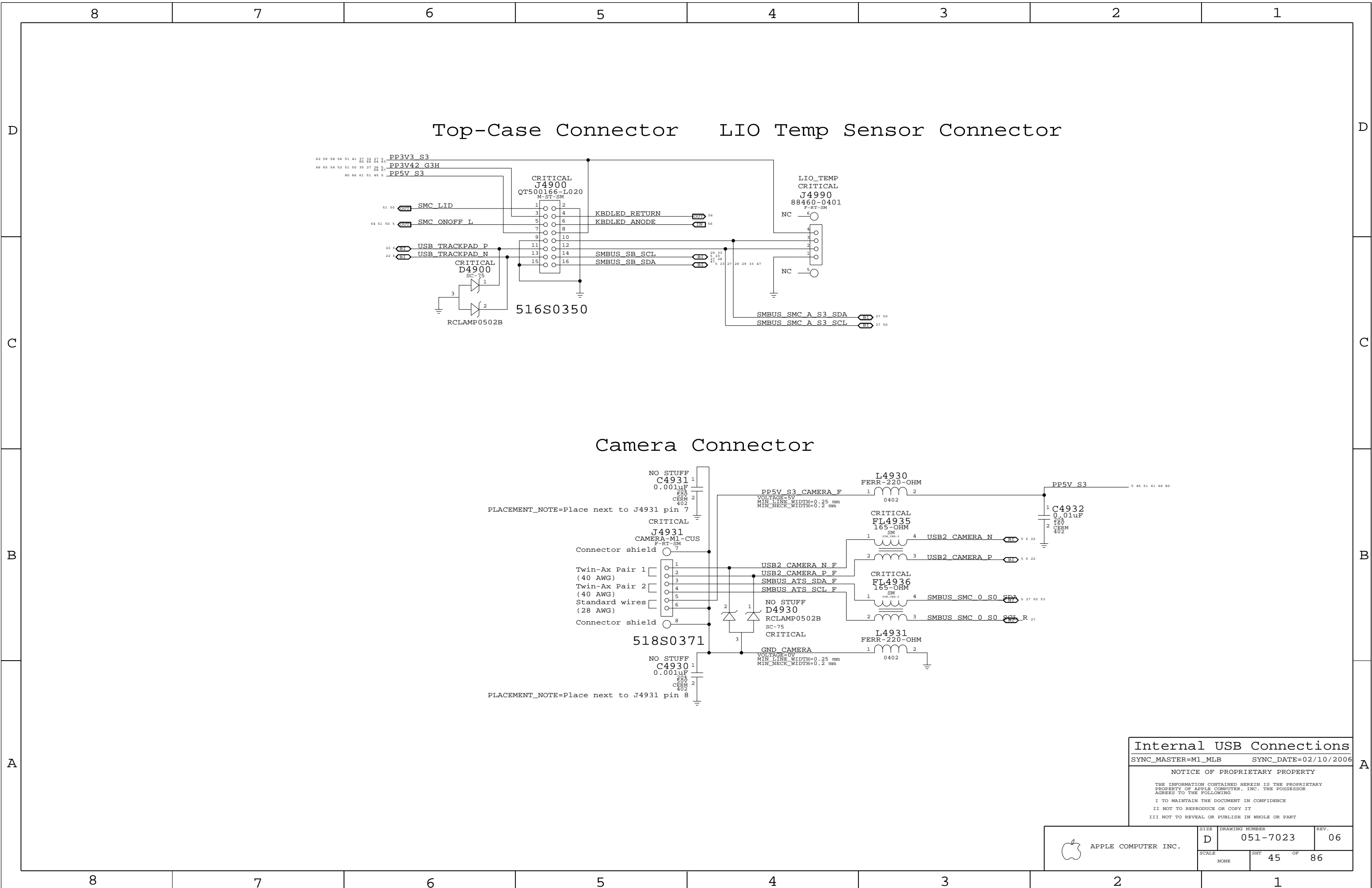
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	D	051-7023	06
SCALE	NONE	SHT	44 OF 86



Internal USB Connections

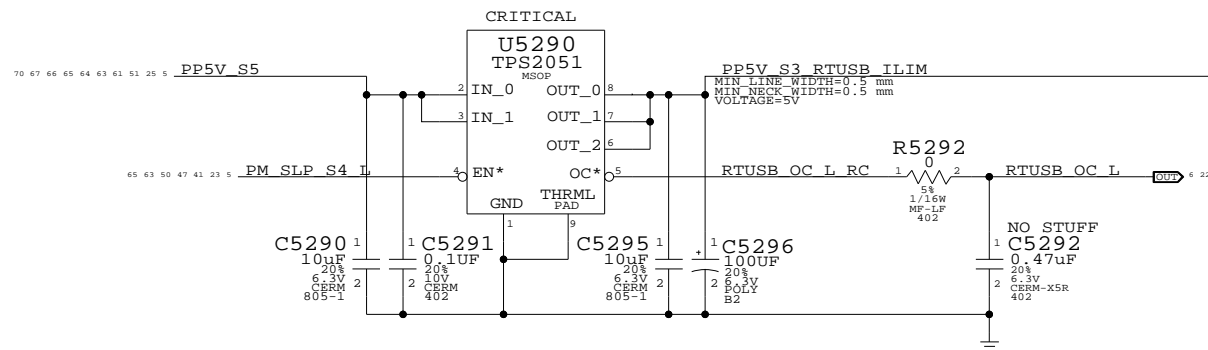
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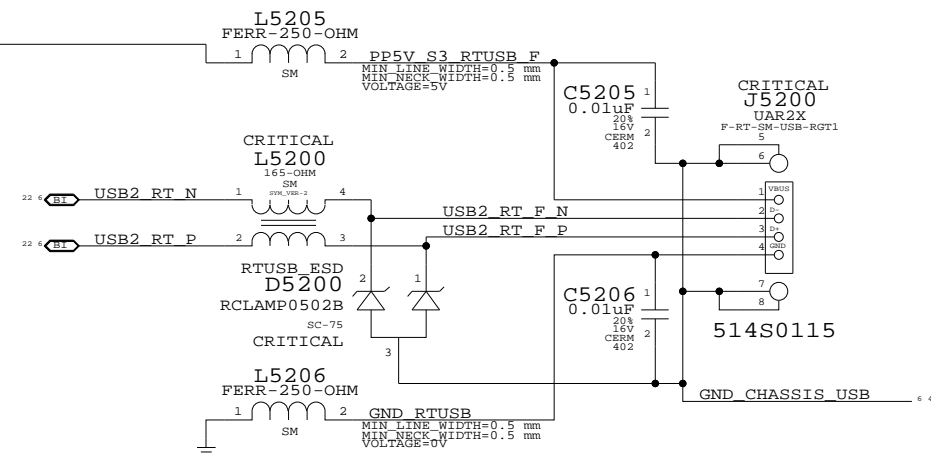
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	D	051-7023	06
SCALE	SHT	OF	
NONE	45	86	

Port Power Switch



Right USB Port

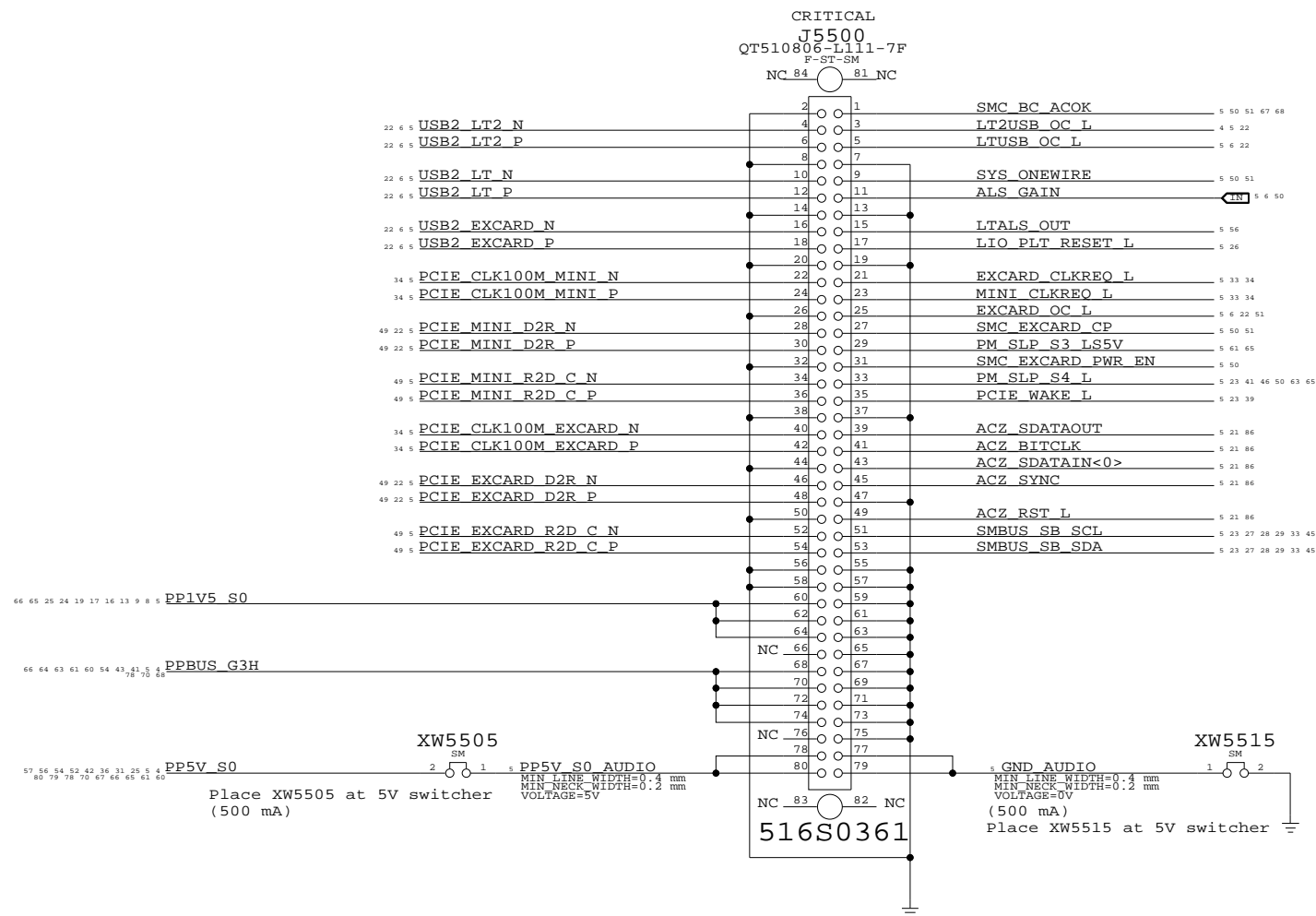


Place L5200, L5205 and L5206 across moat

External USB Connector
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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	D	051-7023	06
SCALE	SHT	OF	REV.
NONE	46	86	

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

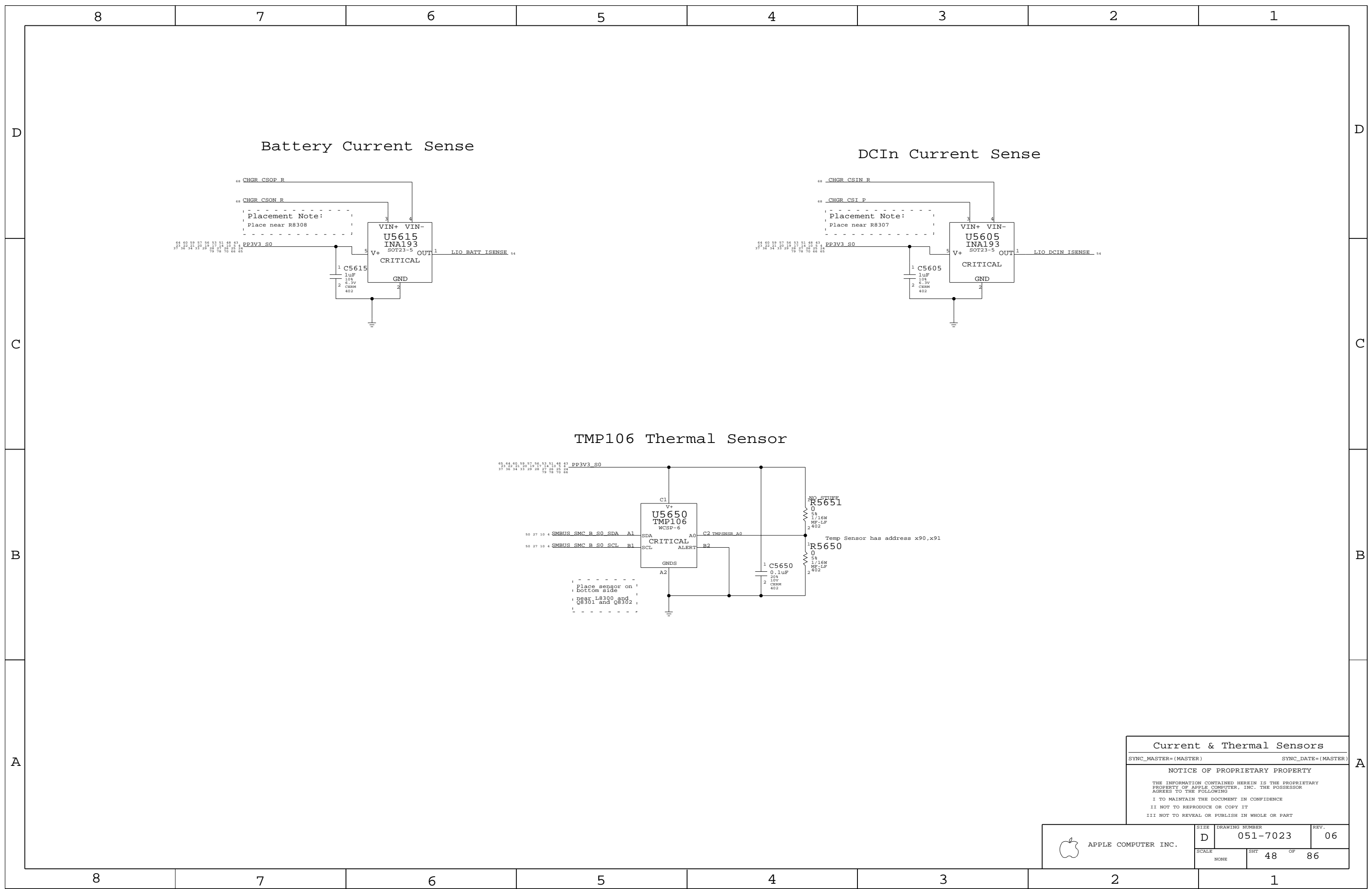
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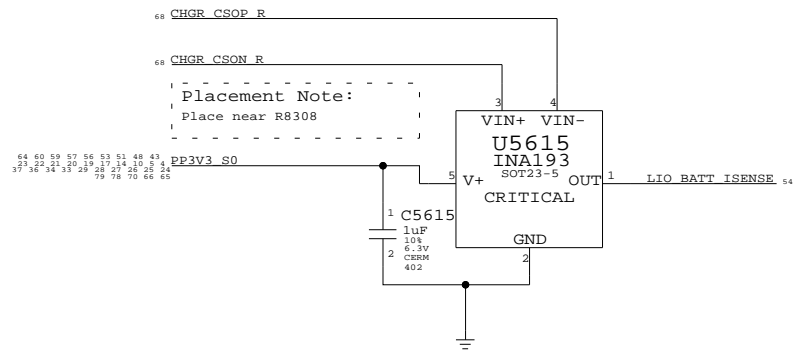
II NOT TO REPRODUCE OR COPY IT

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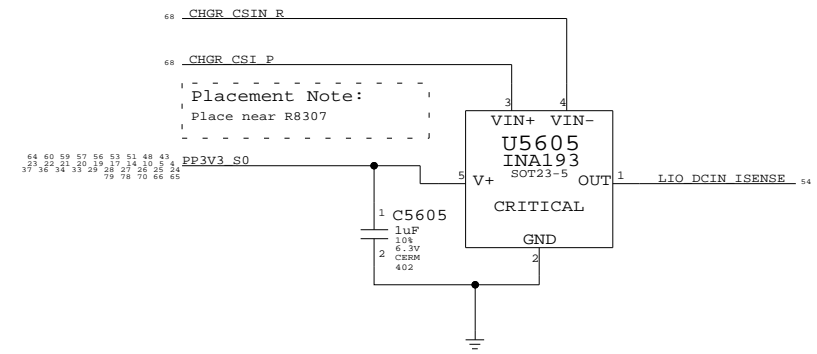
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT		OF
NONE	47		86



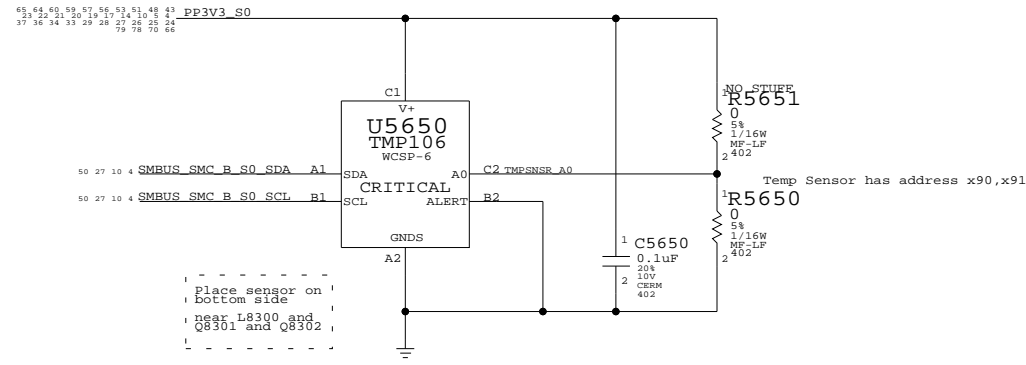
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	D	051-7023	06
SCALE	SHT	OF	
NONE	48	86	

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D

C

C

B

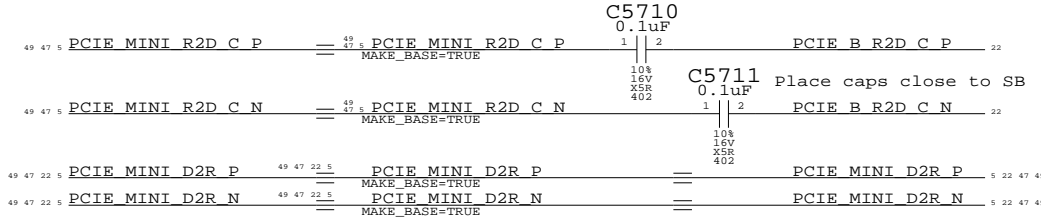
B

A

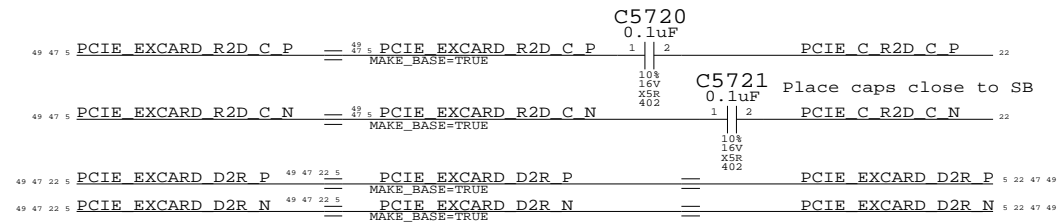
A

PCI-E x1 Port "A" = Ethernet (Yukon)

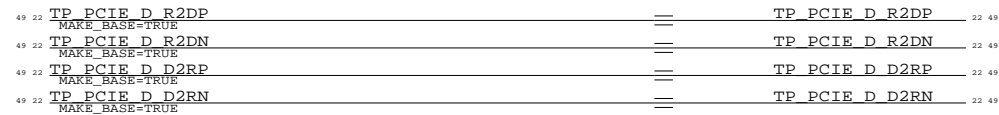
PCI-E x1 Port "B" = PCI-E Mini Card



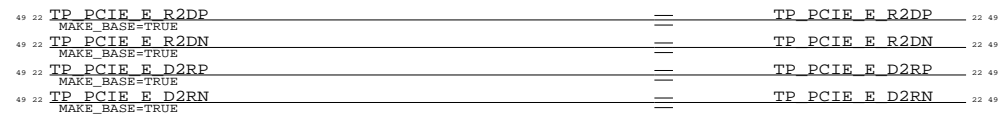
PCI-E x1 Port "C" = ExpressCard



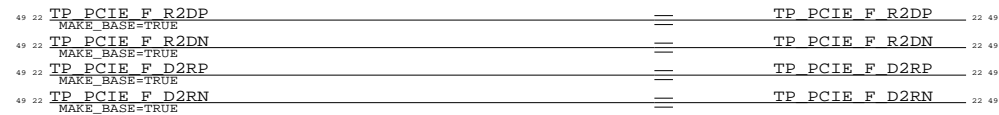
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF	
NONE	49	86	

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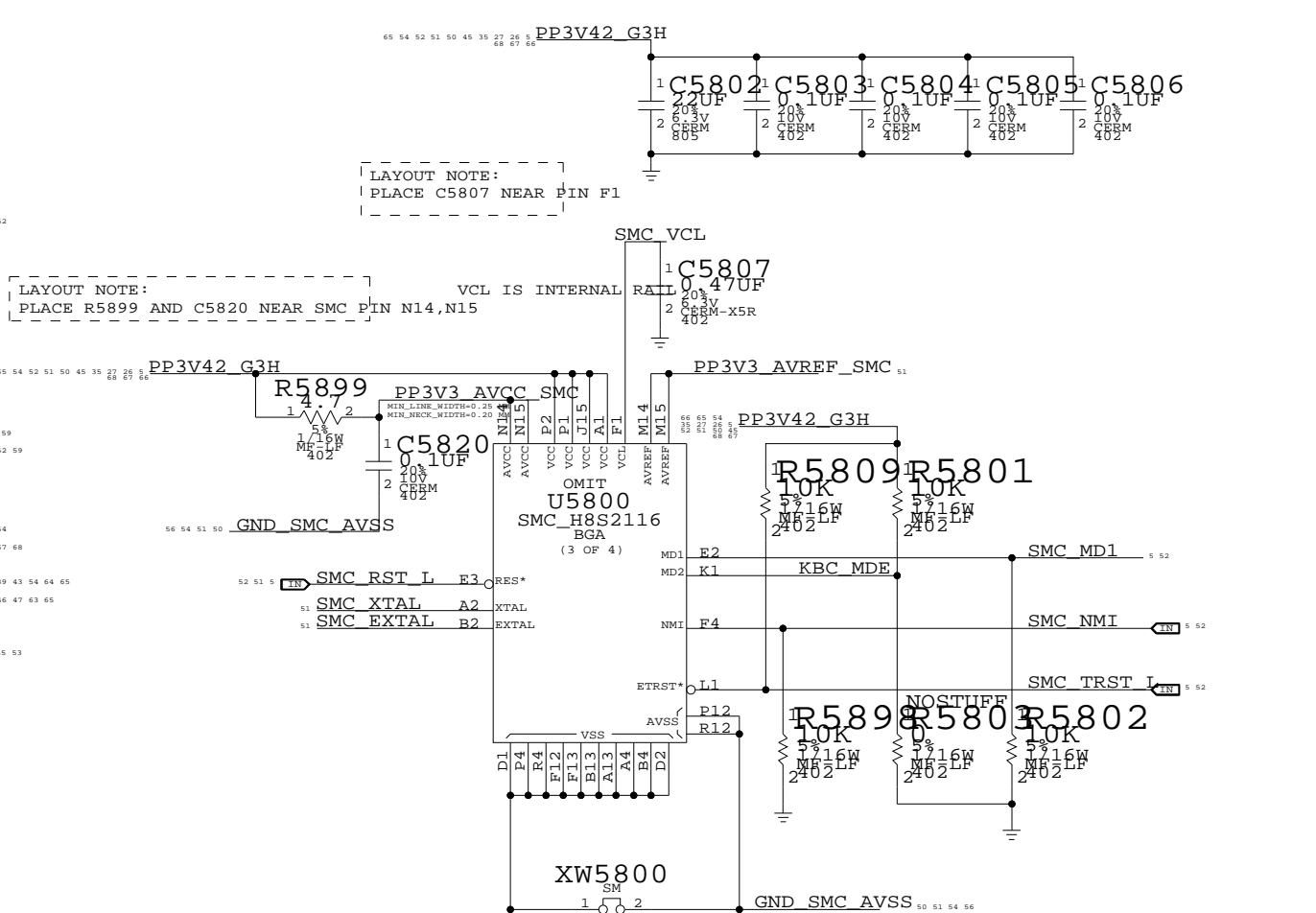
3

2

1

UNUSED PINS HAVE THE FORMAT
 THEY ARE WHERE THEY ARE BY SOFTWARE. THEY
 CAN BE LEFT NO-CONNECTED.

37 5 37 4 65 26 61 14 23 23 5 60 5 23		PM LAN ENABLE B12 SMC_RSTGATE L C13 ALL_SYS_PWRGD A15 RSMRST_PWRGD B14 SMC_SB_NMI B15 PM_RSMRST L C14 IMVP_VR_ON D12 PM_PWRBTN L C15	P10 P11 P12 P13 P14 P15 P16 P17	OMIT U5800 SMC_H8S2116 BGA (1 OF 4)	P60/KIN0* L13 P61/KIN1* L14 P62/KIN2* L15 P63/KIN3* K12 P64/KIN4* K13 P65/KIN5* K14 P66/IRQ6*/KIN6* J12 P67/IRQ7*/KIN7* J13	SMC_PM_G2_EN 65 SMC_ADAPTER_EN 43 51 67 SPI_ARB 22 SPI_SCLK 22 55 SPI_SI 22 55 SPI_SO 22 55 SMC_PROCHOT_3 3 51 FWH_INIT L 51 21 51 52	P70/AN0 N12 P71/AN1 R13 P72/AN2 P13 P73/AN3 R14 P74/AN4 P14 P75/AN5 R15 P76/AN6 N13 P77/AN7 P15	SMC_CPU_ISENSE 54 SMC_CPU_VSENSE 54 SMC_GPU_ISENSE 54 SMC_GPU_VSENSE 54 SMC_DCIN_ISENSE 54 SMC_PBUS_VSENSE 54 SMC_BATT_ISENSE 54 SMC_FWIRE_ISENSE 54
59 52 21 5 59 52 21 5 59 52 21 5 59 52 21 5 26 5 34 59 52 23 5 51 51 27 51 51 51 56		LPC_AD<0> D9 LPC_AD<1> C9 LPC_AD<2> A9 LPC_AD<3> B9 LPC_FRAME L D8 SMC_LRESET L C8 PCI_CLK_SMC A8 INT_SERIRQ D7 TP_SMC_XDP_TMS A5 SMC_SYS_LED_16B B5 SMBUS_SMC_BSB_SDA D5 SMC_TPM_PP C3 TP_SMC_XDP_TRST L B1 TP_SMC_XDP_TCK C2 TP_SMC_SYS_LED D3 SMC_SYS_KBDLED C1	P30/LAD0 P31/LAD1 P32/LAD2 P33/LAD3 P34/LFRAME* P35/LRESET* P36/LCLK P37/SERIRQ P40/TMIO P41/TMO0 P42/SDA1 P43/TMI1/EXSCK1 P44/TMO1 P45 P46/PWX0/PWM0 P47/PWX1/PWM1	OMIT U5800 SMC_H8S2116 BGA (2 OF 4)	P80/PME* C7 P81/GA20 A7 P82/CLKRUN* B7 P83/LPCPD* D6 P84/IRQ3*/TXD1 C6 P85/IRQ4*/RXD1 A6 P86/IRQ5*/SCK1/SCL1 B6	SMC_WAKE_SCI L 23 SMC_TPM_GPIO 51 67 PM_CLKRUN L 5 23 52 59 PM_SUS_STAT L 51 52 59 SC_TX L 51 SC_RX L 51 SMBUS_SMC_BSB_SDA 27	P90/IRQ2* K4 P91/IRQ1* J2 P92/IRQ0* J1 P93/IRQ12* J3 P94/IRQ13* J4 P95/IRQ14* H1 P96/EXCL C2 P97/IRQ15*/SDA0 G2	SMC_ONOFF L 45 51 54 SMC_BC_ACOK 5 47 51 67 68 SMC_BS_ALERT L 51 67 PM_SLP_S3 L 5 23 32 39 43 54 65 PM_SLP_S4 L 5 23 41 46 47 63 65 PM_SLP_S5 L 5 23 51 SMC_CLK32K_SUSC 35 SMBUS_SMC_0_S0 5 27 45 53
52 51 5 52 51 5 53 27 5		SMC_TX L G1 SMC_RX L G4 SMBUS_SMC_0_S0_SCL F2	P50 P51 P52/SCL0	OMIT U5800 SMC_H8S2116 BGA (3 OF 4)	P98/IRQ8*/PMM2 M7 P99/IRQ9*/PMM3 P6 PF2/IRQ10*/TMOY R6 PF3/IRQ11*/TMOX N6 PF4/PMM4 M6 PF5/PMM5 R5 PF6/PMM6 P5 PF7/PMM7 N5	SMC_CASE_OPEN 51 SMC_TCK 5 51 52 SMC_TDI 5 51 52 SMC_TDO 5 51 52 SMC_TMS 5 51 52 TP_SMC_PF0 51 TP_SMC_PF1 51 SMC_LID 45 51 SMC_CPU_RESET_3 3 51 SMC_BATT_ISET 68 TP_SMC_BATT_VSET 51 SMC_SYS_ISET 68 TP_SMC_SYS_VSET 51	PG0/EXIRQ8*/TMIX P9 PG1/EXIRQ9*/TMIY R9 PG2/EXIRQ10*/SDA2 N9 PG3/EXIRQ11*/SCL2 P8 PG4/EXIRQ12*/EXSDAA R8 PG5/EXIRQ13*/EXSCLA M8 PG6/EXIRQ14*/EXSDAB P7 PG7/EXIRQ15*/EXSCLB R7	
56 56 56 51 54 51 56		SMC_RCIN L R3 BOOT_LPC_SPI L P3 PM_SYSRST L R2 SMC_TPM_RESET L N3 PM_EXTS L R1 PM_THRM L N2 SYS_ONEWIRE M4 PM_BATLOW L N1 SMC_EXTSMI L B10 SMC_RUNTIME_SCI L A10 SMC_ODD_DETECT D10 ISENSE_CAL_EN A11 SMC_EXCARD_CP B11 SMC_EXCARD_PWR_EN C11 SMC_EXCARD_OC L A12 SMC_XDP_TDO_3_3 D11 SMC_FAN_0_CTL G14 SMC_FAN_1_CTL G15 TP_SMC_FAN_2_CTL G13 TP_SMC_FAN_3_CTL G12 SMC_FAN_0_TACH H14 SMC_FAN_1_TACH H15 TP_SMC_FAN_2_TACH H13 TP_SMC_FAN_3_TACH H12 SMS_X_AXIS M11 SMS_Y_AXIS P11 SMS_Z_AXIS R11 TP_SMC_ANALOG_ID N11 SMC_P1V05S0_ISENSE P10 SMC_P1V8S3_ISENSE R10 ALS_LEFT N10 ALS_RIGHT M10	PA0/KIN8*/PA2CC PA1/KIN9*/PA2BD PA2/KIN10*/PS2AC PA3/KIN11*/PS2AD PA4/KIN12*/PS2BC PA5/KIN13*/PS2BD PA6/KIN14*/PS2CC PA7/KIN15*/PS2CD PB0/LSMI* PB1/LSCI PB2 PB3 PB4 PB5 PB6 PB7 PC0/TIOCA0/WUE8* PC1/TIOCB0/WUE9* PC2/TIOCC0/TCLKA/WUE10* PC3/TIOCD0/TCLKB/WUE11* PC4/TIOCA1/WUE12* PC5/TIOCB1/TCLKC/WUE13* PC6/TIOCA2/WUE14* PC7/TIOCB2/TCLKD/WUE15* PD0/AN8 PD1/AN9 PD2/AN10 PD3/AN11 PD4/AN12 PD5/AN13 PD6/AN14 PD7/AN15	OMIT U5800 SMC_H8S2116 BGA (4 OF 4)	PH0/EXIRQ6* E1 PH1/EXIRQ7* F3 PH2/FWE K2 PH3/EXEXCL C4 PH4 D4 PH5 B3	SMC_PROCHOT 51 SMC_THRMTRIP 51 SMC_FWE 51 ALS_GAIN 5 6 47 SMS_INT L 23 51 SMS_ONOFF L 58		



OMIT

U5800
 SMC_H8S2116
 BGA
 (4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

SMC

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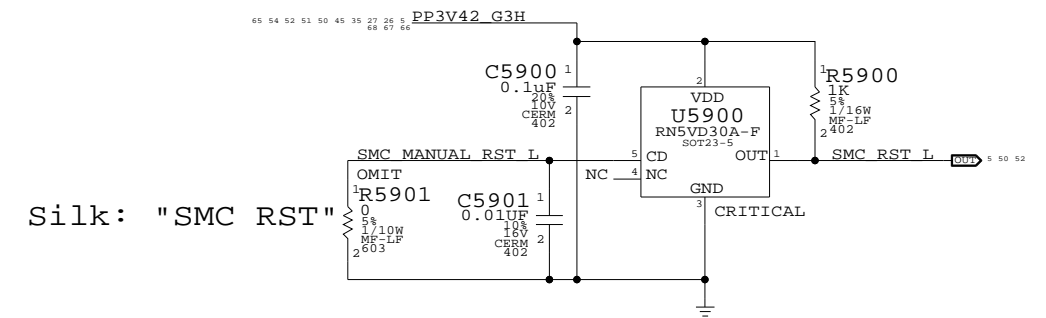
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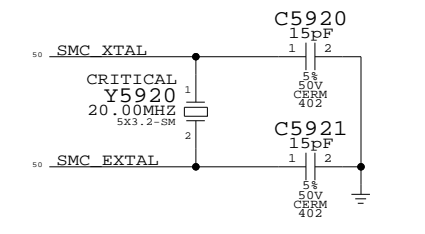
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7023	REV. 06
	SCALE NONE	SHEETS 50	OF 86

SMC Reset Button / Brownout Detect

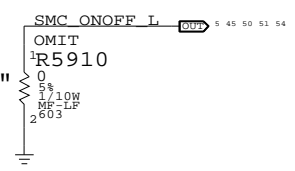


Silk: "SMC_RST"

SMC Crystal Circuit

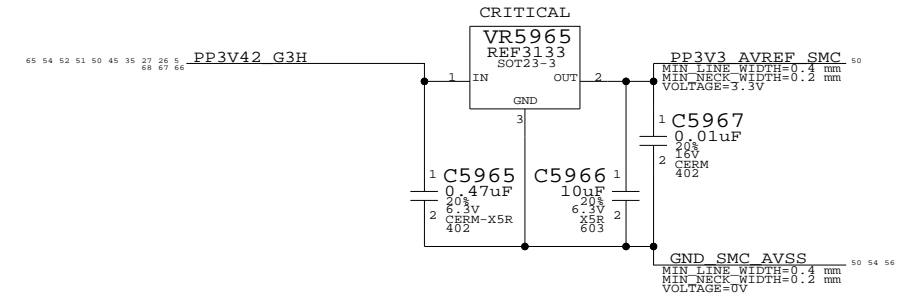


Debug Power Button

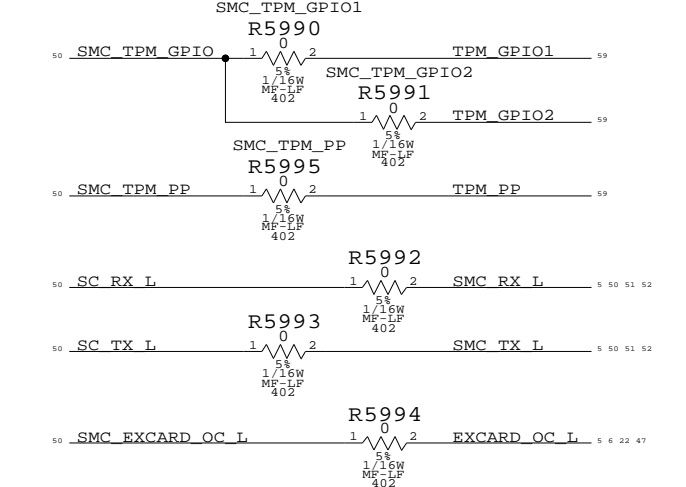


Silk: "PWR_BTN"

SMC AVREF Supply

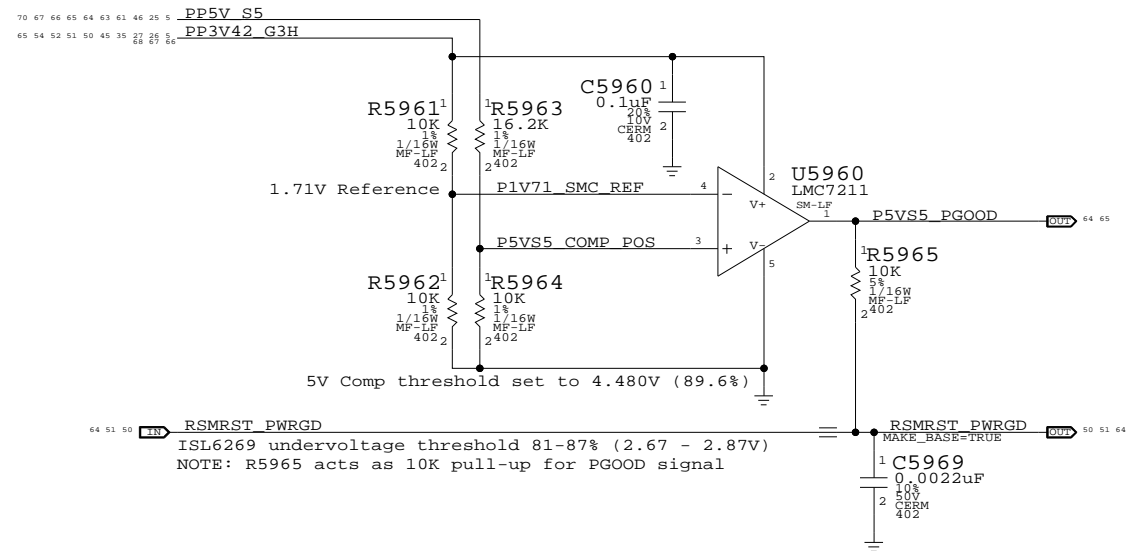


FWH_INIT_L	=	FWH_INIT_L	5 21 50 51 52
SMC_P1V05S0_ISENSE	=	SMC_P1V05S0_ISENSE	48 43 22 21 10 15 13 14 15 14 24 24 50 51 54
SMC_P1V8S3_ISENSE	=	SMC_P1V8S3_ISENSE	50 51 54
PM_EXTTTS_L	=	PM_EXTTTS_L	14 28 29 50 51
TP_SMC_SYS_LED	=	TP_SMC_SYS_LED	50 51
TP_SMC_ANALOG_ID	=	TP_SMC_ANALOG_ID	50 51
TP_SMC_BATT_VSET	=	TP_SMC_BATT_VSET	50 51
TP_SMC_SYS_VSET	=	TP_SMC_SYS_VSET	50 51
TP_SMC_FAN_2_CTL	=	TP_SMC_FAN_2_CTL	50 51
TP_SMC_FAN_2_TACH	=	TP_SMC_FAN_2_TACH	50 51
TP_SMC_FAN_3_CTL	=	TP_SMC_FAN_3_CTL	50 51
TP_SMC_FAN_3_TACH	=	TP_SMC_FAN_3_TACH	50 51
TP_SMC_XDP_TCK	=	TP_SMC_XDP_TCK	50 51
TP_SMC_XDP_TDO_L	=	TP_SMC_XDP_TDO_L	51
TP_SMC_XDP_TMS	=	TP_SMC_XDP_TMS	50 51
TP_SMC_XDP_TRST_L	=	TP_SMC_XDP_TRST_L	50 51
TP_SMC_P20	=	TP_SMC_P20	50 51
TP_SMC_P21	=	TP_SMC_P21	50 51
TP_SMC_P22	=	TP_SMC_P22	50 51
TP_SMC_P23	=	TP_SMC_P23	50 51
TP_SMC_P26	=	TP_SMC_P26	50 51
TP_SMC_P27	=	TP_SMC_P27	50 51
TP_SMC_PFO	=	TP_SMC_PFO	50 51
TP_SMC_PFI	=	TP_SMC_PFI	50 51



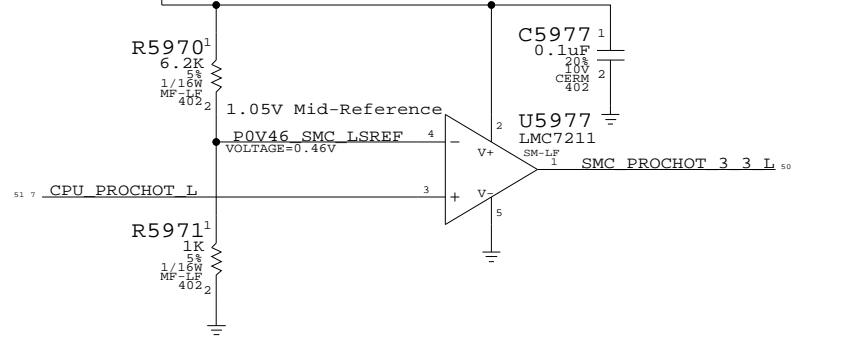
SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation

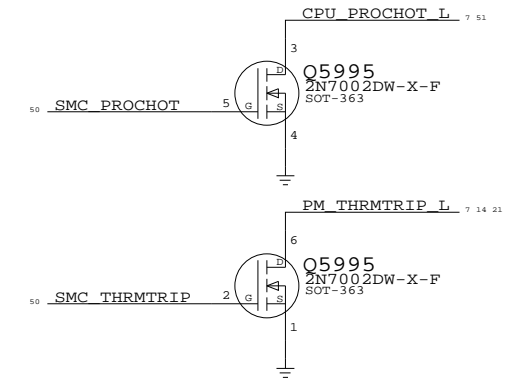


RSMRST_PWRGD ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal

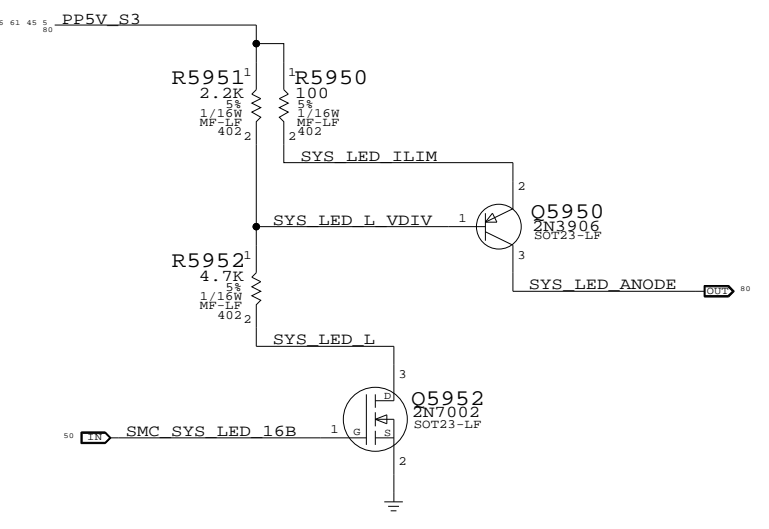
SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



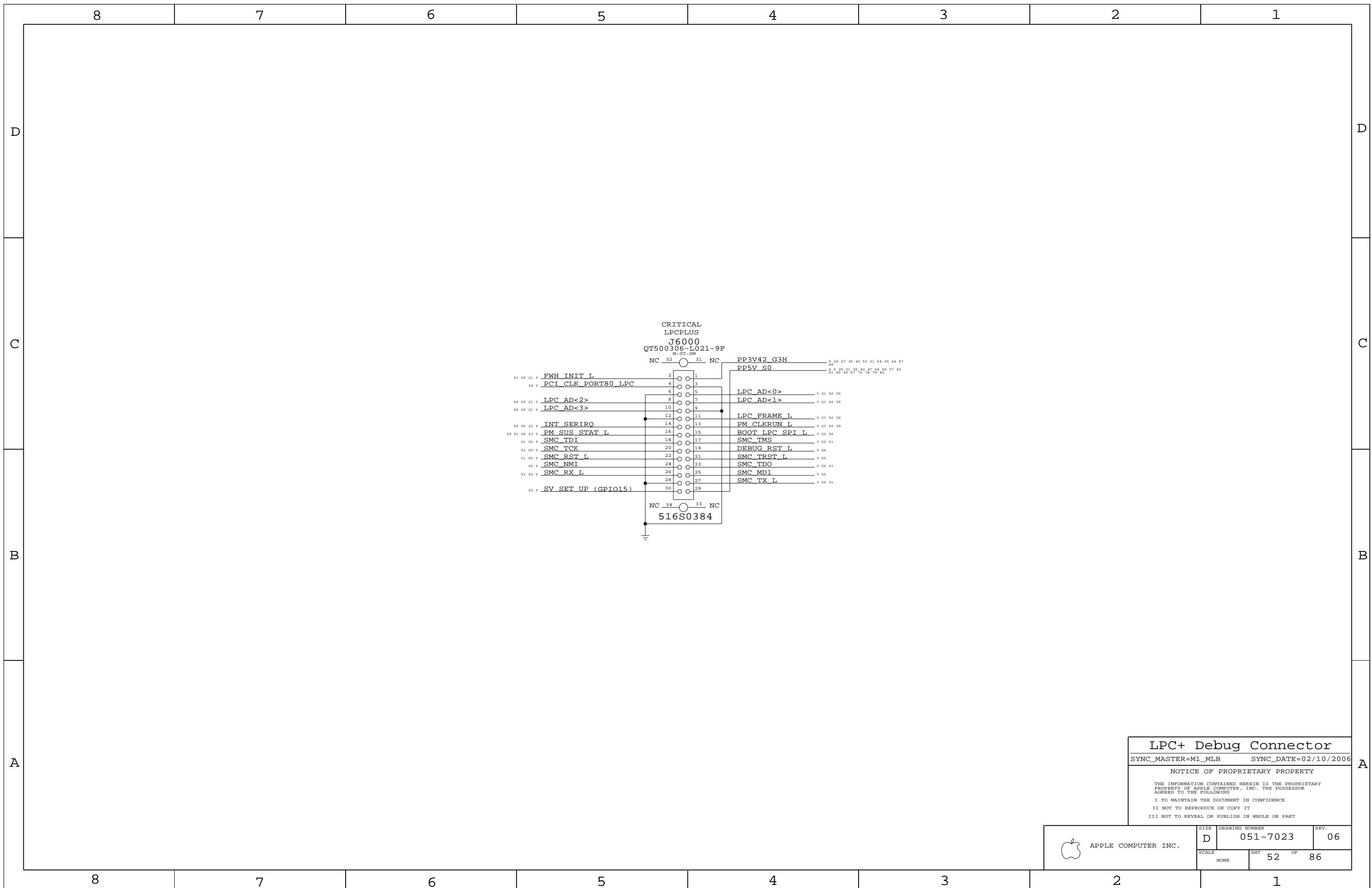
System (Sleep) LED Circuit



SMS_INT_L	R5930	10K	1	2	5%	1/16W	MF-LF	402
SMC_TPM_RESET_L	R5931	10K	1	2	5%	1/16W	MF-LF	402
SMC_ONOFF_L	R5932	10K	1	2	5%	1/16W	MF-LF	402
SMC_LID	R5933	100K	1	2	5%	1/16W	MF-LF	402
SMC_FWE	R5934	10K	1	2	5%	1/16W	MF-LF	402
SMC_TX_L	R5935	10K	1	2	5%	1/16W	MF-LF	402
SMC_RX_L	R5936	100K	1	2	5%	1/16W	MF-LF	402
SYN_ONEWIRE	R5937	2.0K	1	2	5%	1/16W	MF-LF	402
SMC_BS_ALERT_L	R5938	100K	1	2	5%	1/16W	MF-LF	402
SMC_TMS	R5939	10K	1	2	5%	1/16W	MF-LF	402
SMC_TDO	R5940	10K	1	2	5%	1/16W	MF-LF	402
SMC_TDI	R5941	10K	1	2	5%	1/16W	MF-LF	402
SMC_TCK	R5942	10K	1	2	5%	1/16W	MF-LF	402
SMC_CPU_RESET_3_3_L	R5980	10K	1	2	5%	1/16W	MF-LF	402
SMC_XDP_TCK_3_3	R5981	10K	1	2	5%	1/16W	MF-LF	402
SMC_XDP_TDO_3_3	R5982	10K	1	2	5%	1/16W	MF-LF	402
SMC_BATT_TRICKLE_EN_L	R5943	10K	1	2	5%	1/16W	MF-LF	402
SMC_BATT_CHG_EN	R5944	10K	1	2	5%	1/16W	MF-LF	402
SMC_ADAPTER_EN	R5945	10K	1	2	5%	1/16W	MF-LF	402
SMC_CASE_OPEN	R5946	10K	1	2	5%	1/16W	MF-LF	402
SMC_BC_ACOK	R5947	470K	1	2	5%	1/16W	MF-LF	402
SMC_EXCARD_CP	R5948	10K	1	2	5%	1/16W	MF-LF	402
PM_SUS_STAT_L	R5983	100K	1	2	5%	1/16W	MF-LF	402
PM_SLP_S5_L	R5984	100K	1	2	5%	1/16W	MF-LF	402

SMC Support
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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SCALE	SHT	OF	
NONE	51	86	



LPC+ Debug Connector

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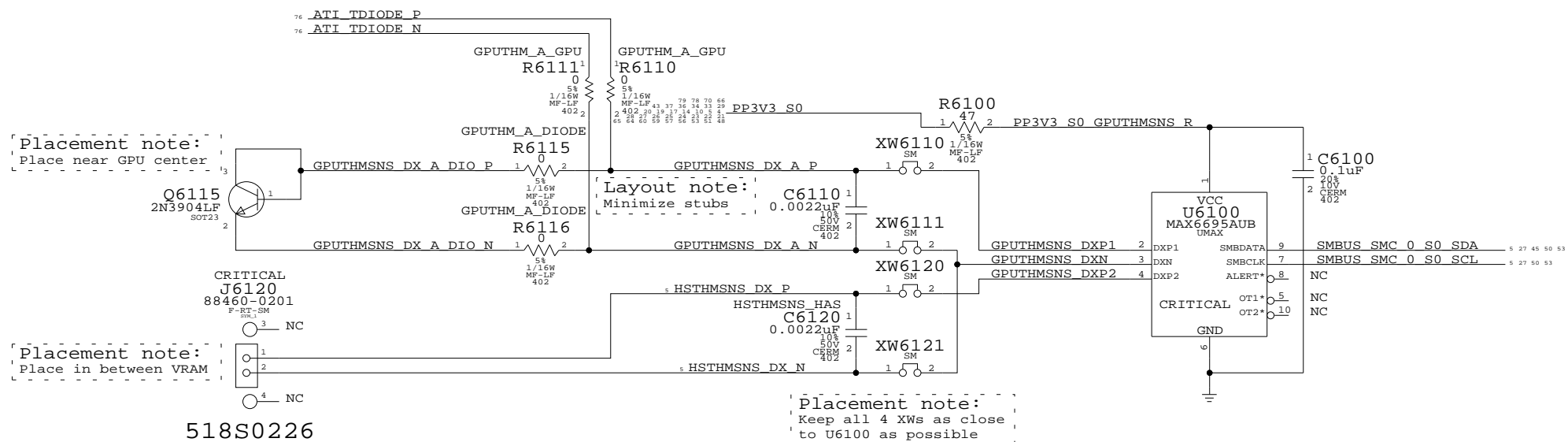
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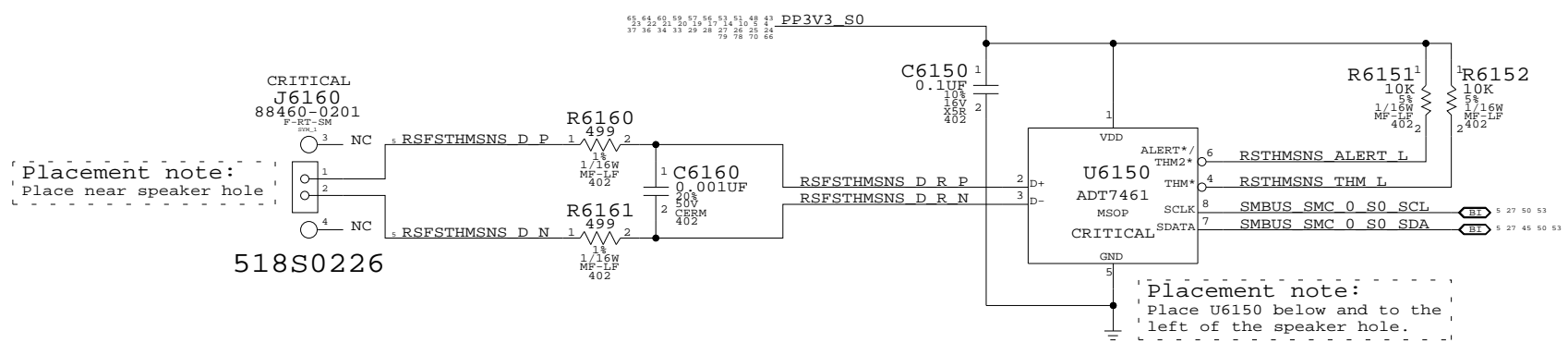
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GPU / Heat Pipe Thermal Sensor

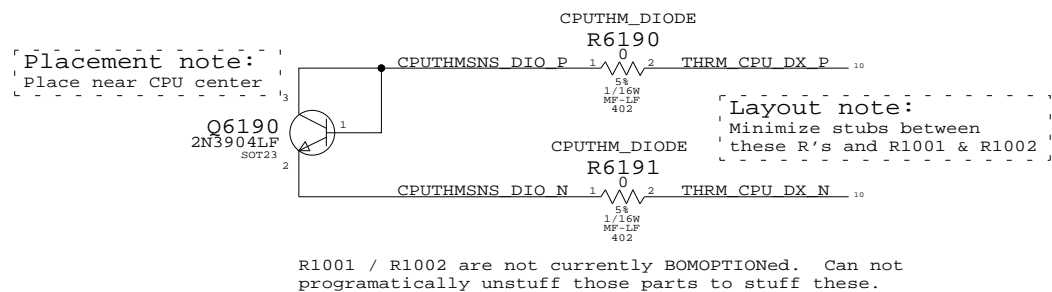


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



Thermal Sensors
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

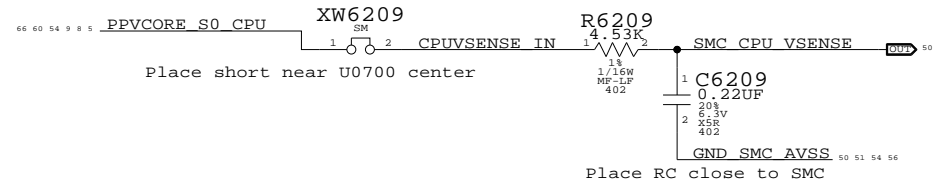
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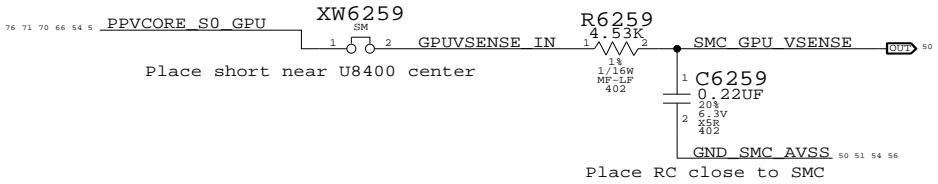
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	D	051-7023	06
SCALE	SHT 53 OF 86		
NONE			

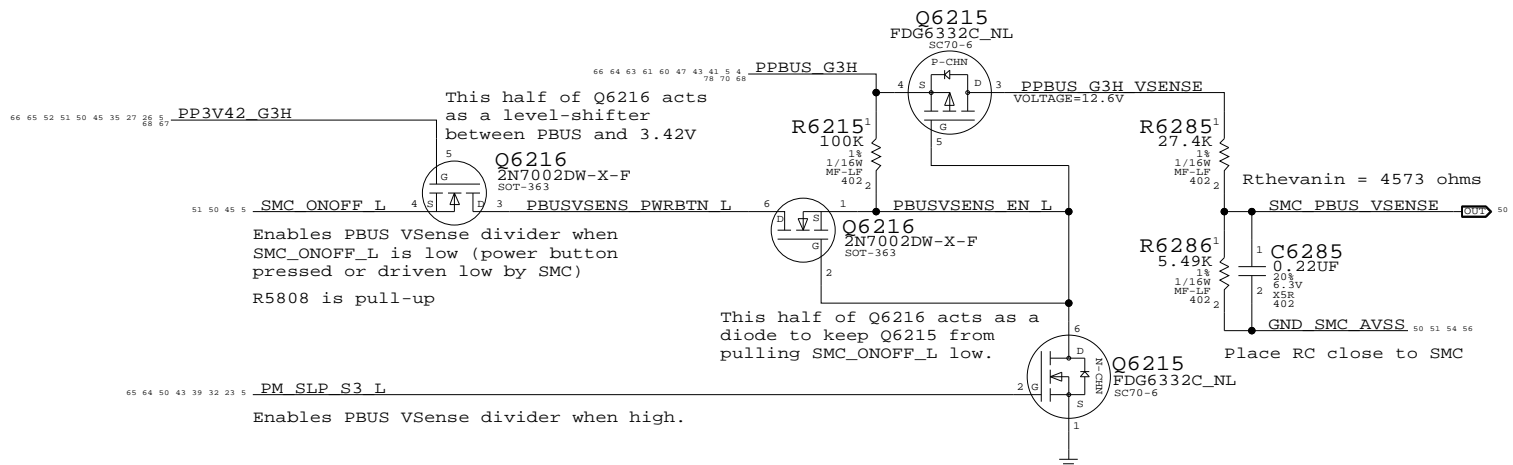
CPU Voltage Sense / Filter



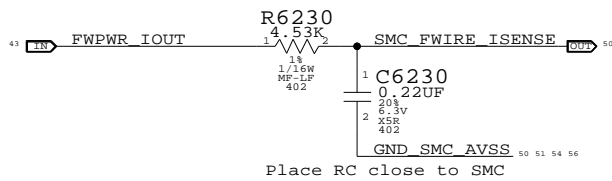
GPU Voltage Sense / Filter



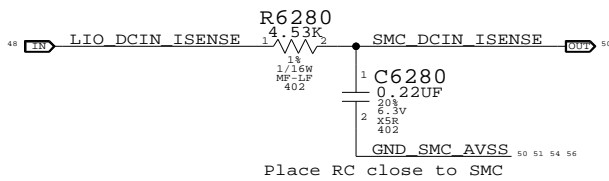
PBUS Voltage Sense Enable & Filter



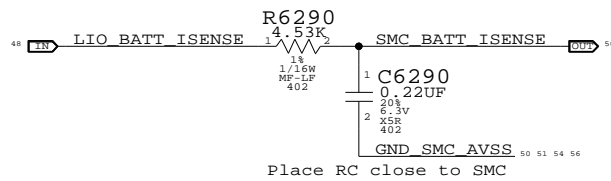
FireWire Current Sense Filter



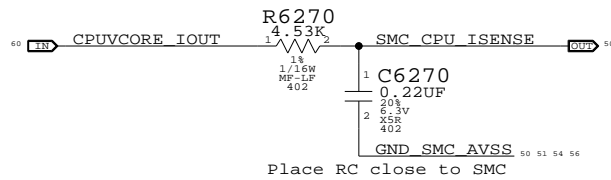
DCIN Current Sense Filter



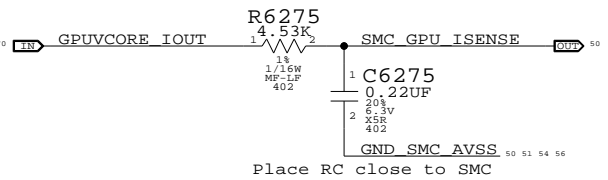
Battery Current Sense Filter



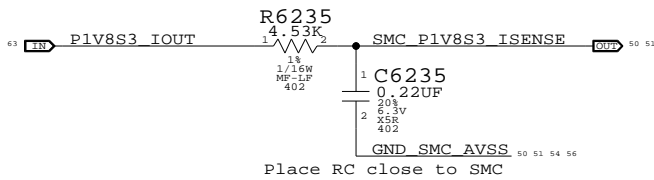
CPU Current Sense Filter



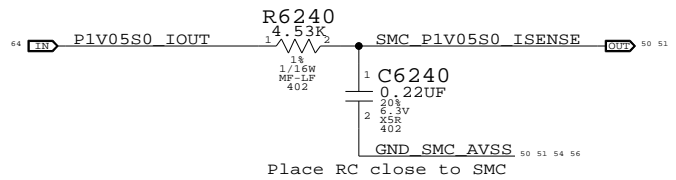
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

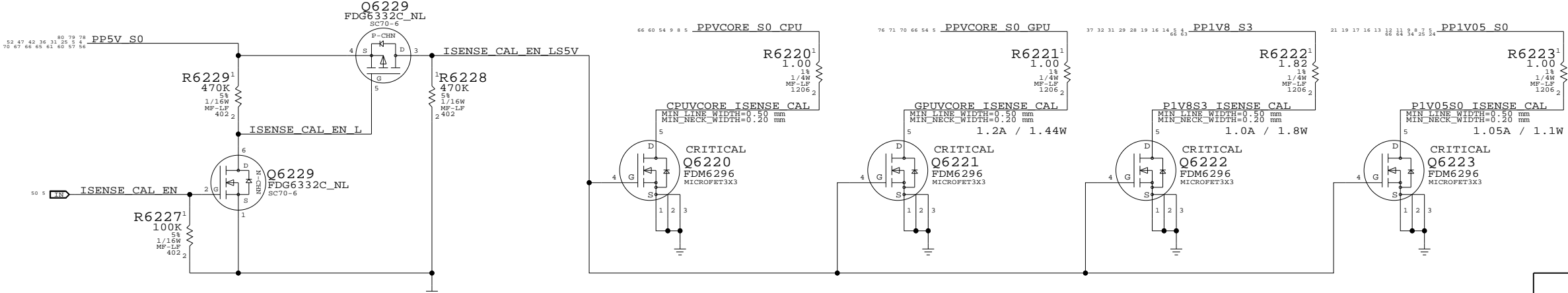


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



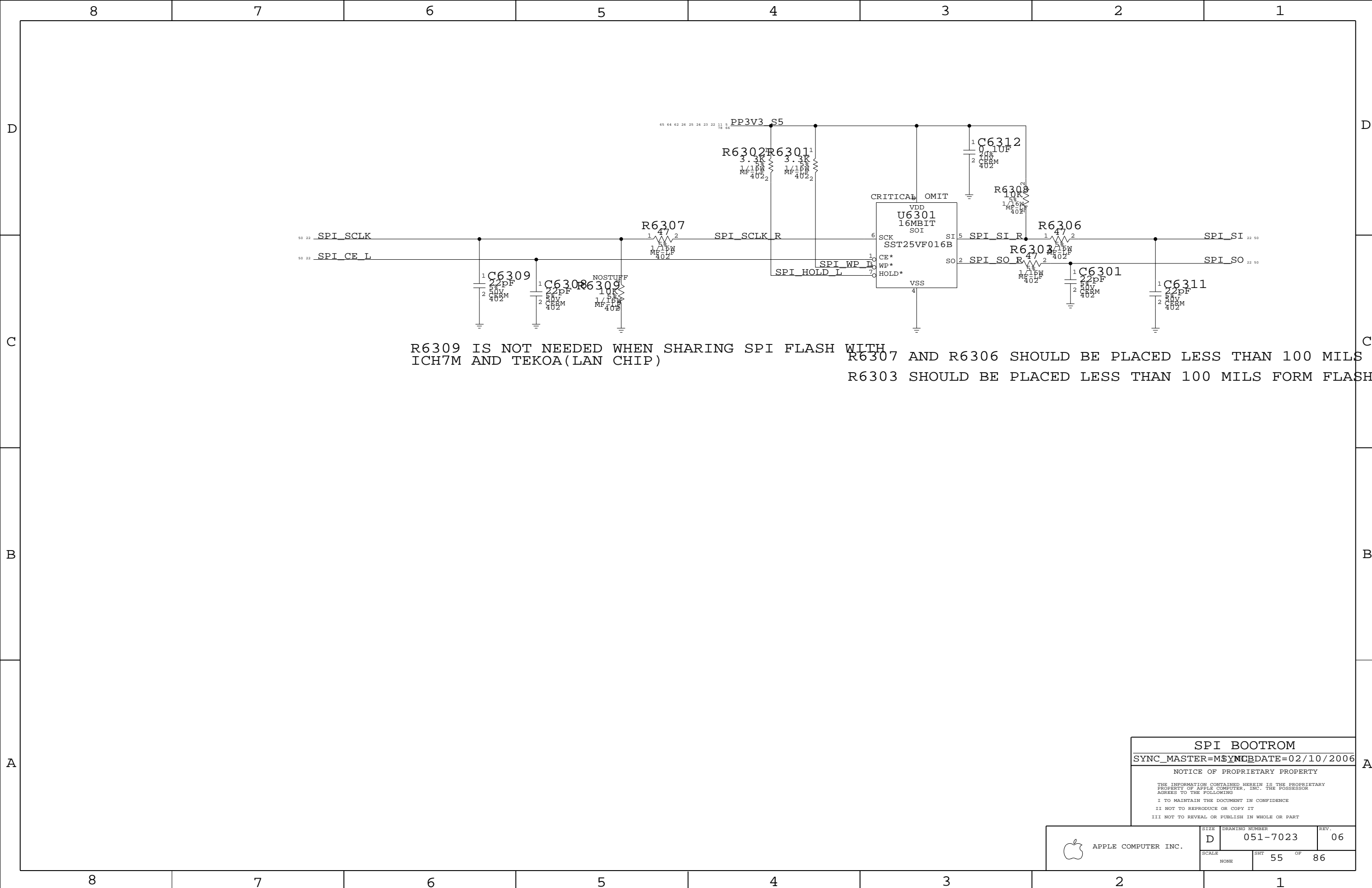
Current & Voltage Sensing

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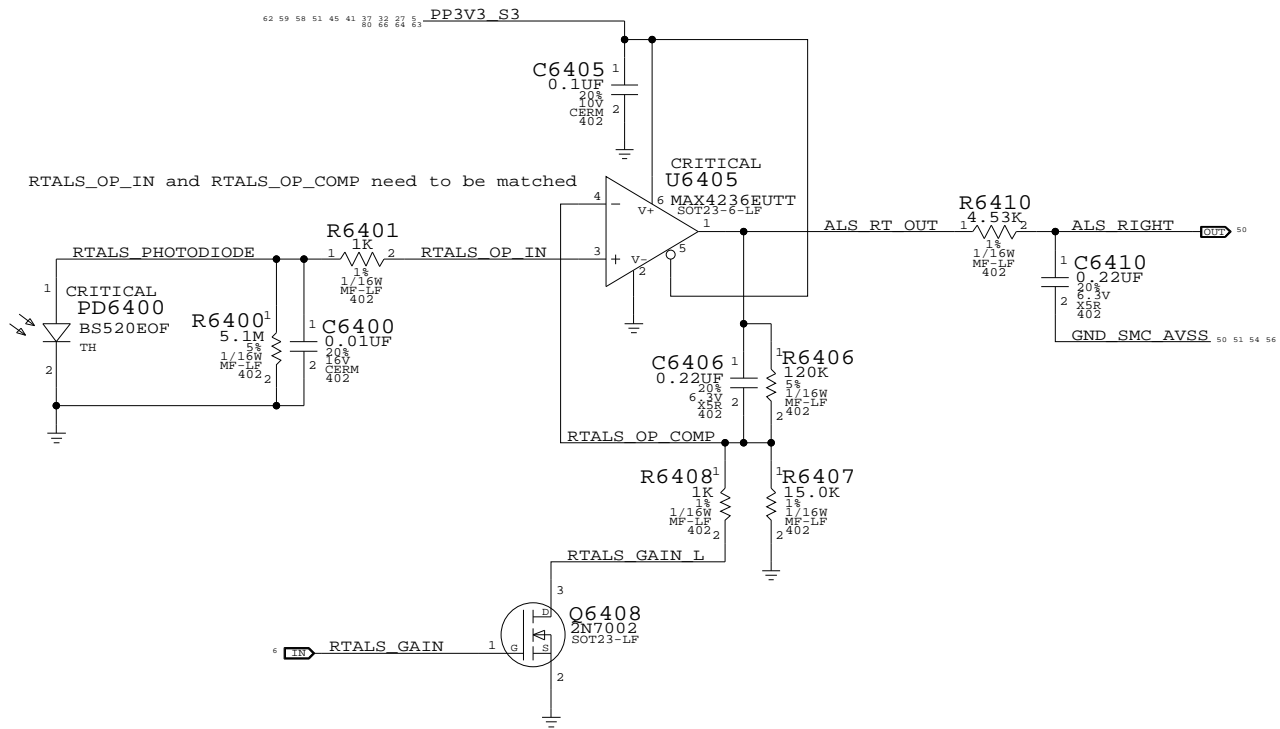


R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)
 R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
 R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

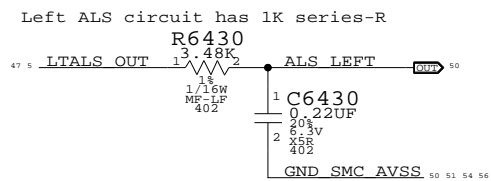
SPI BOOTROM
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	SCALE NONE	SHIT 55	OF 86

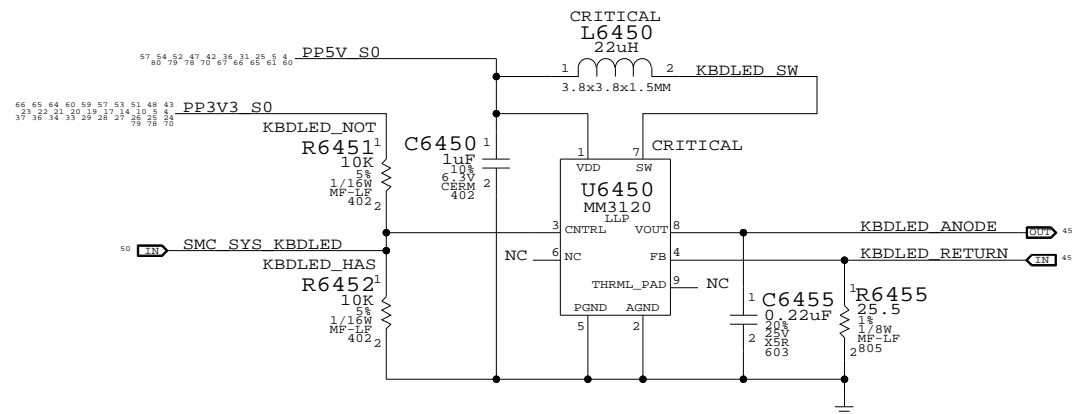
Right ALS Circuit



Left ALS Filter



Keyboard LED Driver



ALS Support

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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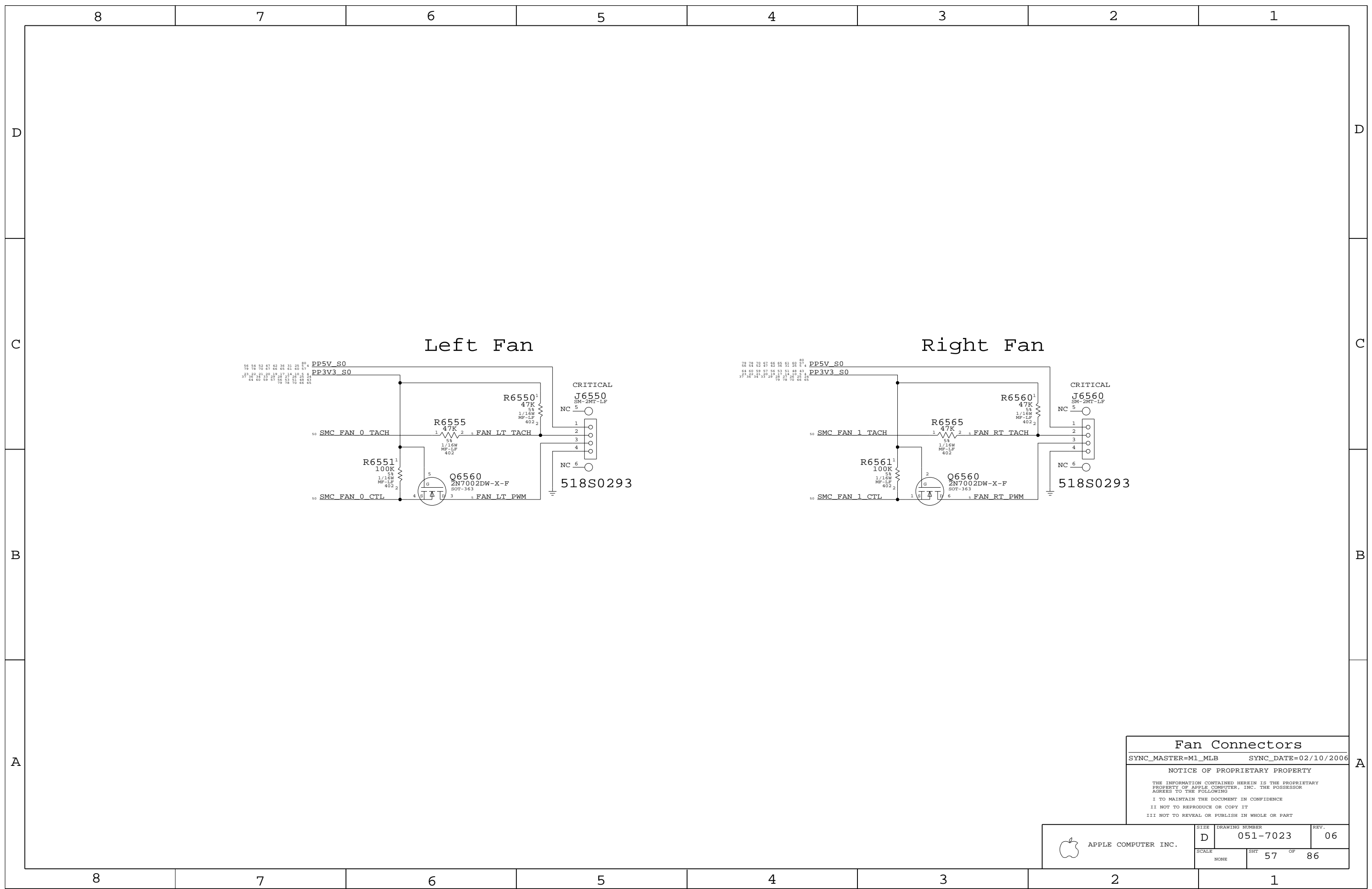
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SCALE	SHT	OF	
NONE	56	86	



Fan Connectors

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	SCALE NONE	SHT 57	OF 86

8 7 6 5 4 3 2 1

D

D

C

C

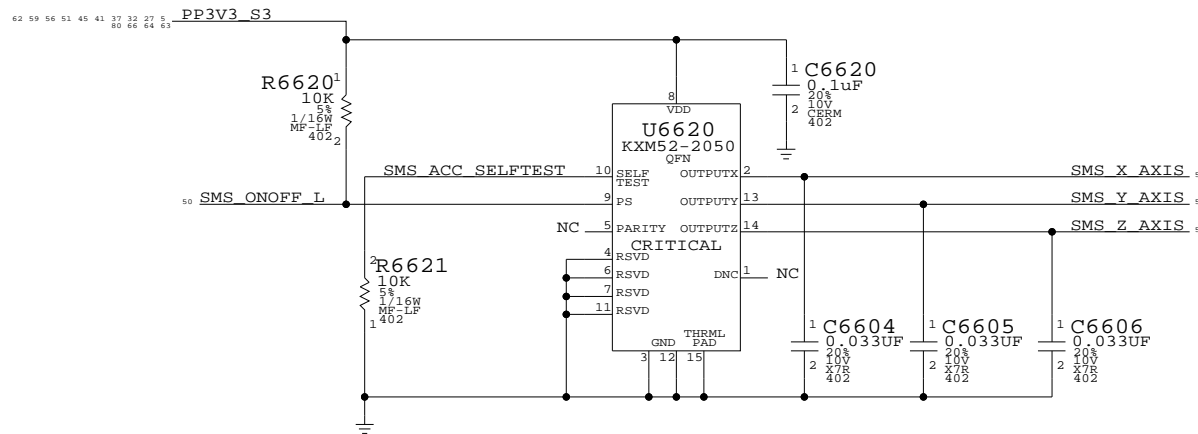
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A

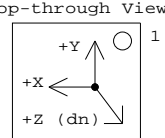
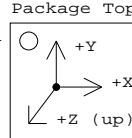
A

8 7 6 5 4 3 2 1



Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

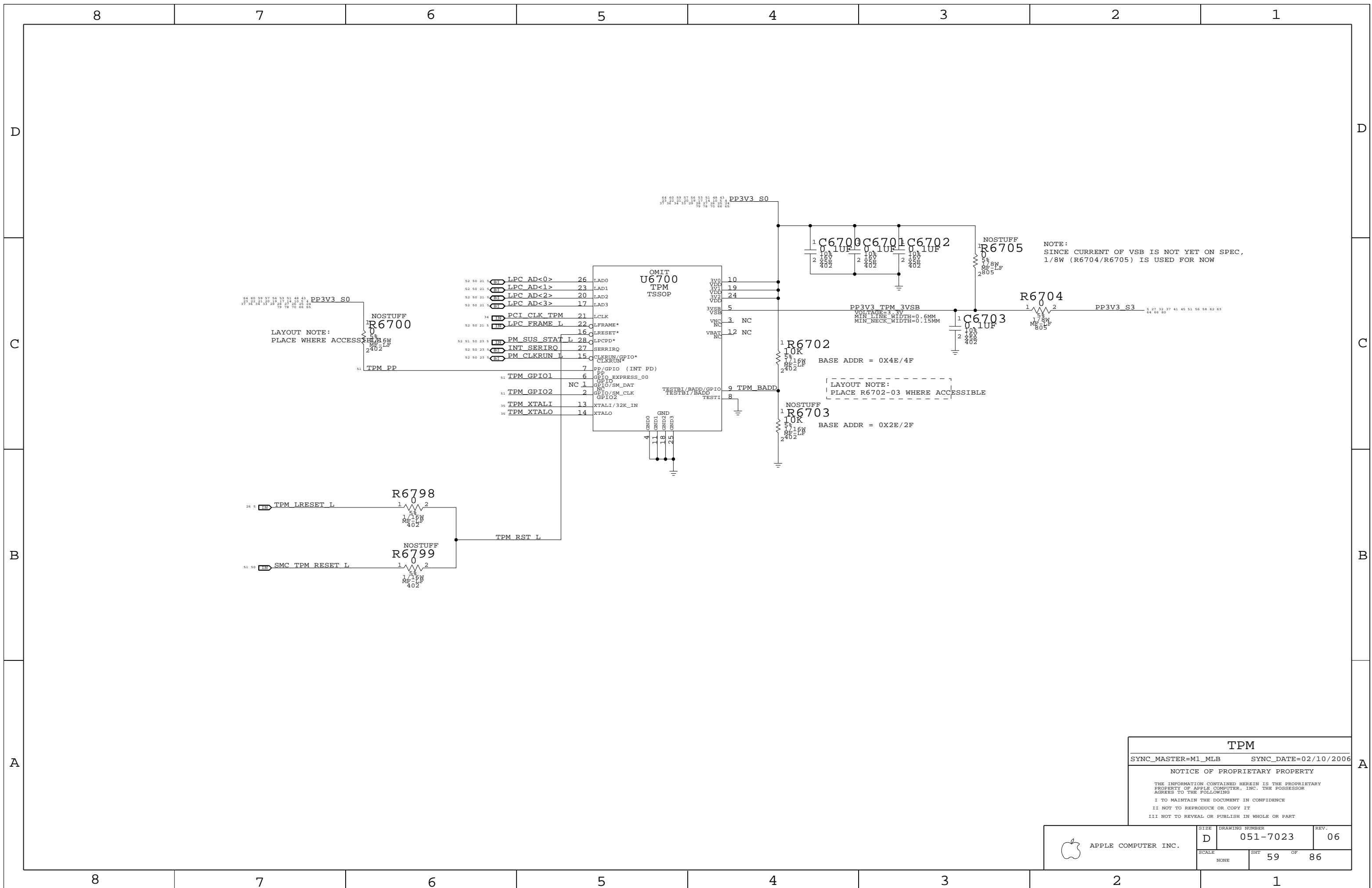


M1 placement: Bottom-side

Sudden Motion Sensor (SMS)
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT		OF
NONE	58		86



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

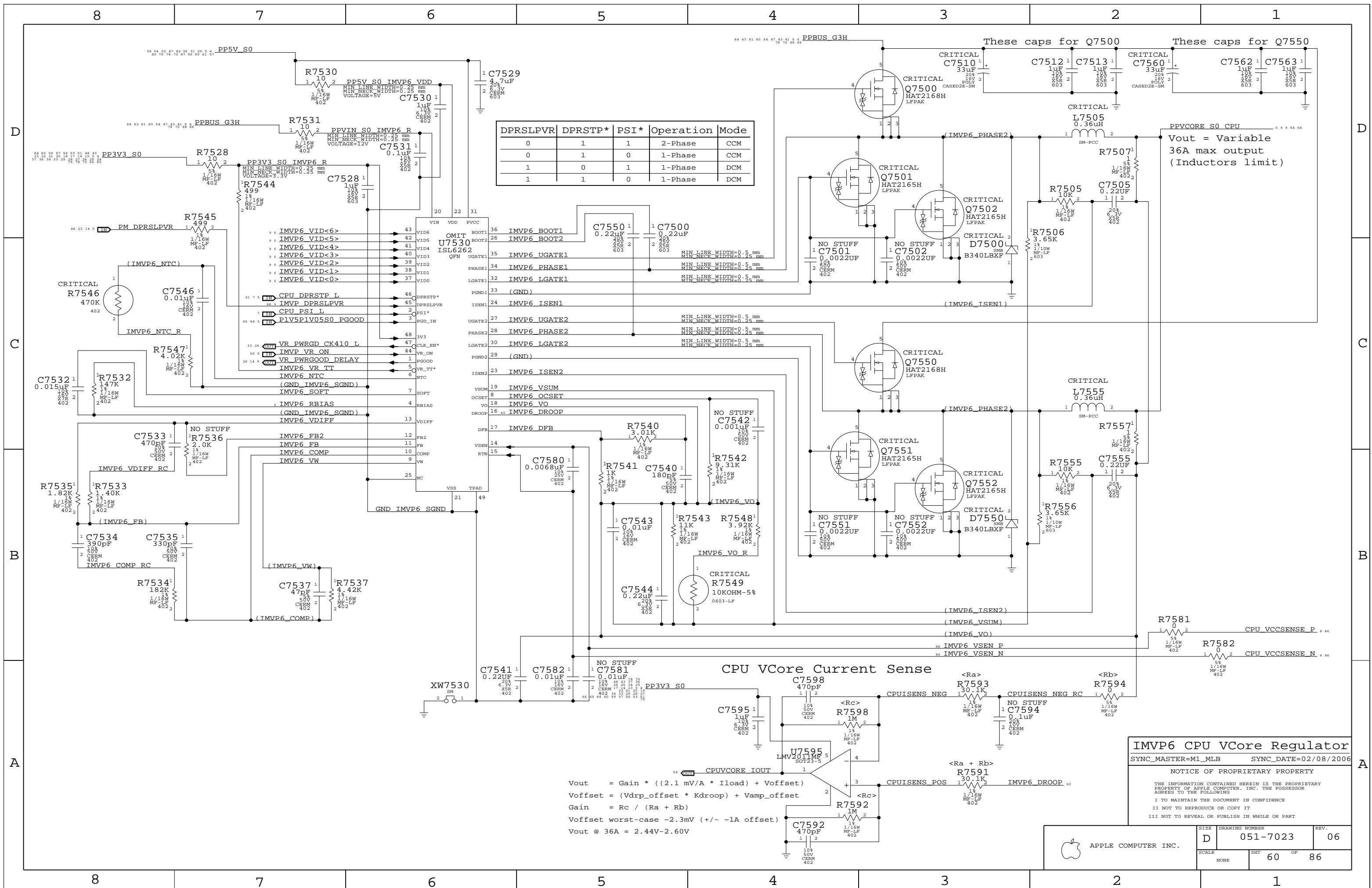
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	SCALE NONE	SHT 59	OF 86



$$V_{out} = Gain * ((2.1 \text{ mV/A} * I_{load}) + V_{offset})$$

$$V_{offset} = (V_{drp_offset} * K_{droop}) + V_{amp_offset}$$

$$Gain = R_c / (R_a + R_b)$$

$$V_{offset \text{ worst-case}} \sim 2.3 \text{ mV (+/- } \sim 1 \text{ A offset)}$$

$$V_{out @ 36A} = 2.44 \text{ V} - 2.60 \text{ V}$$

IMVP6 CPU VCore Regulator
 SYNC_MASTER=M1_MLB SYNC_DATE=02/08/2006

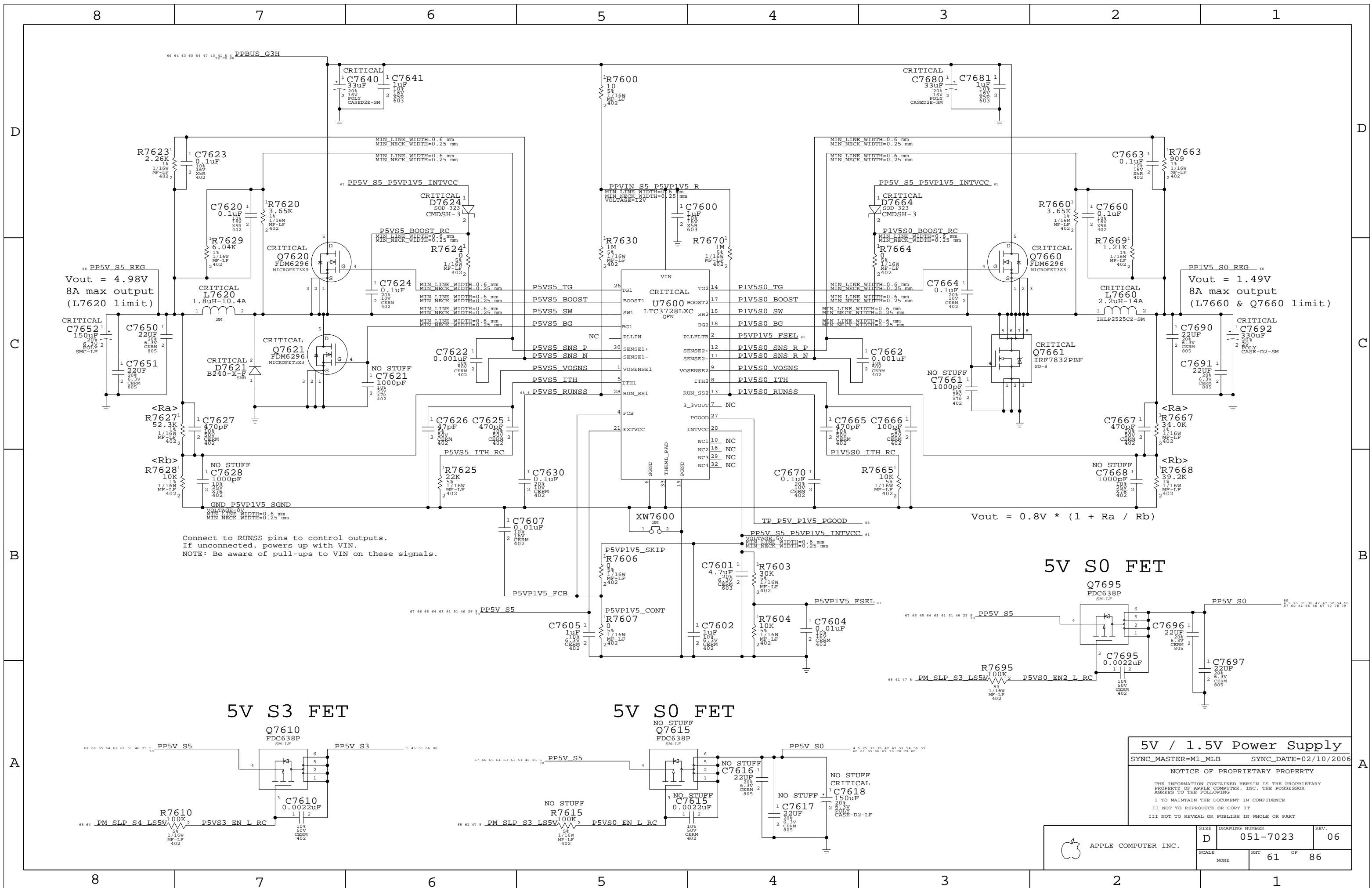
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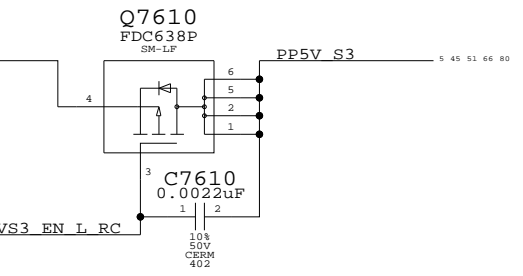
PP5V_S5_REG
 Vout = 4.98V
 8A max output
 (L7620 limit)

PP1V5_S0_REG
 Vout = 1.49V
 8A max output
 (L7660 & Q7661 limit)

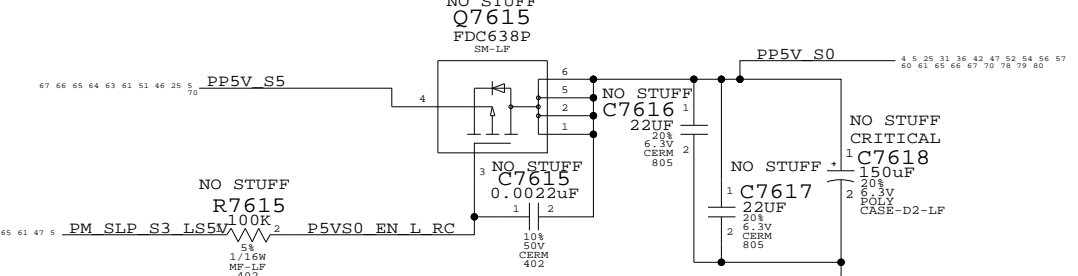
$$Vout = 0.8V * (1 + Ra / Rb)$$

Connect to RUNSS pins to control outputs.
 If unconnected, powers up with VIN.
 NOTE: Be aware of pull-ups to VIN on these signals.

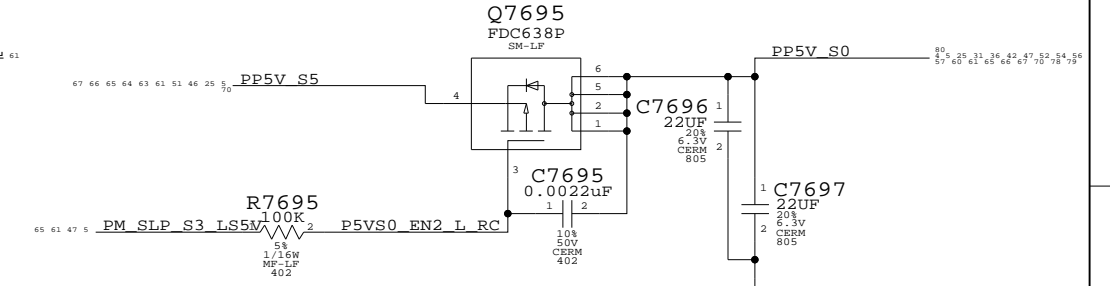
5V S3 FET



5V S0 FET



5V S0 FET

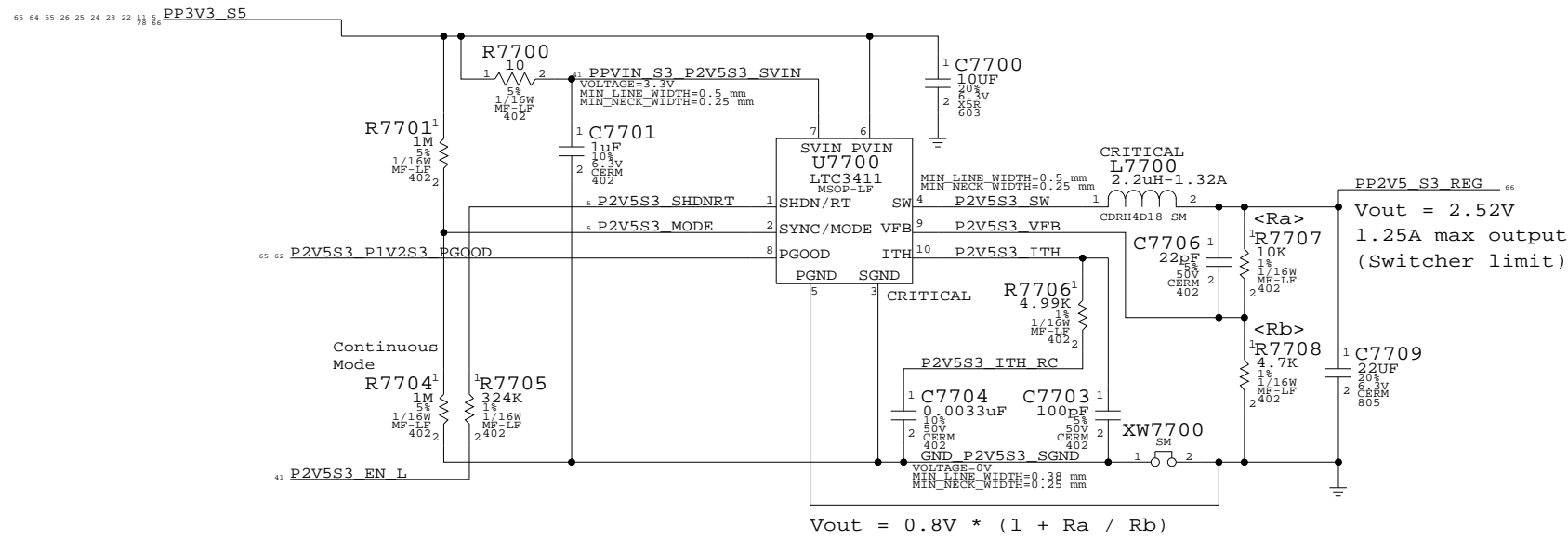


5V / 1.5V Power Supply
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

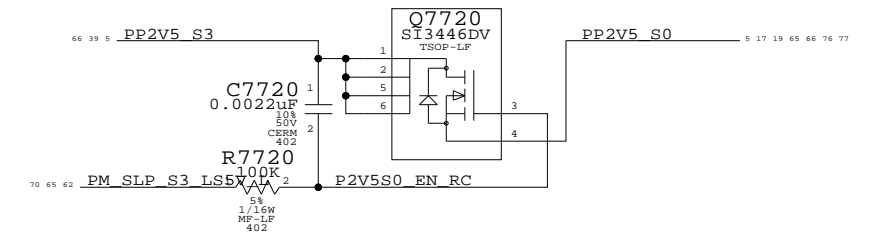
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	D	051-7023	06
SCALE	SHT 61 OF 86		

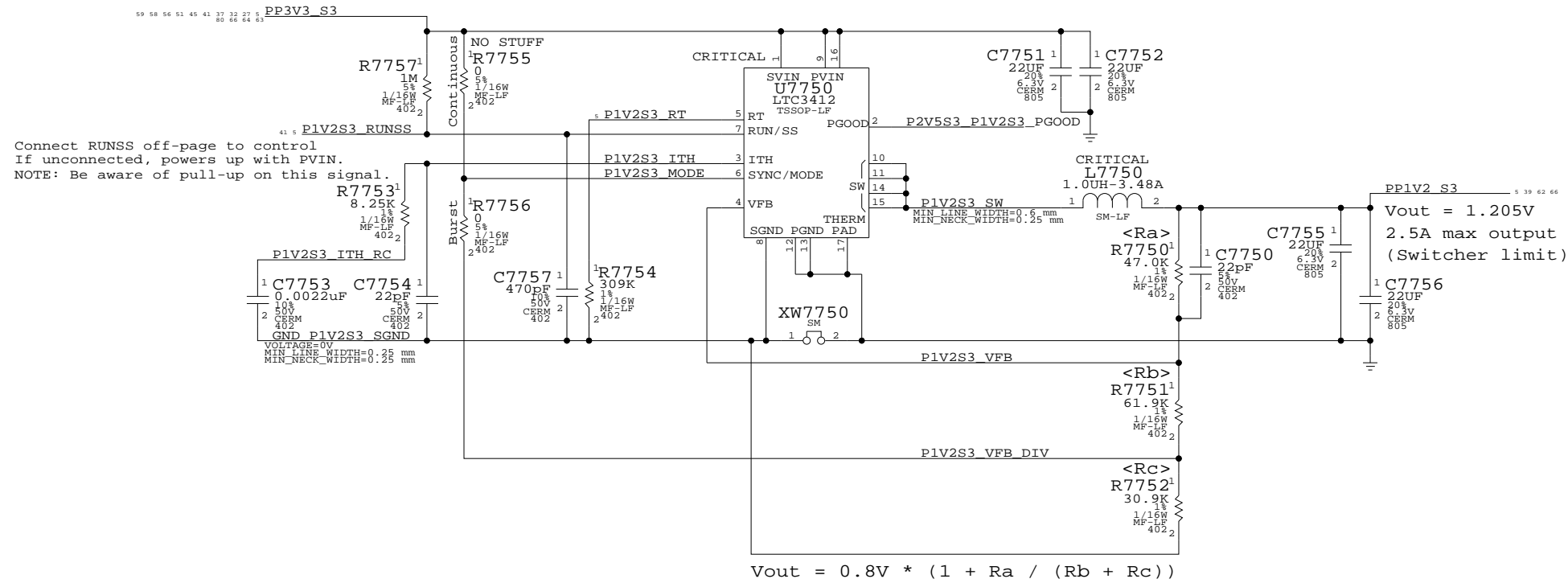
2.5V S3 Regulator



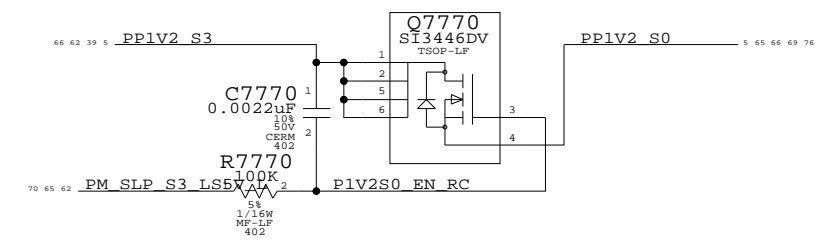
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

NOTICE OF PROPRIETARY PROPERTY

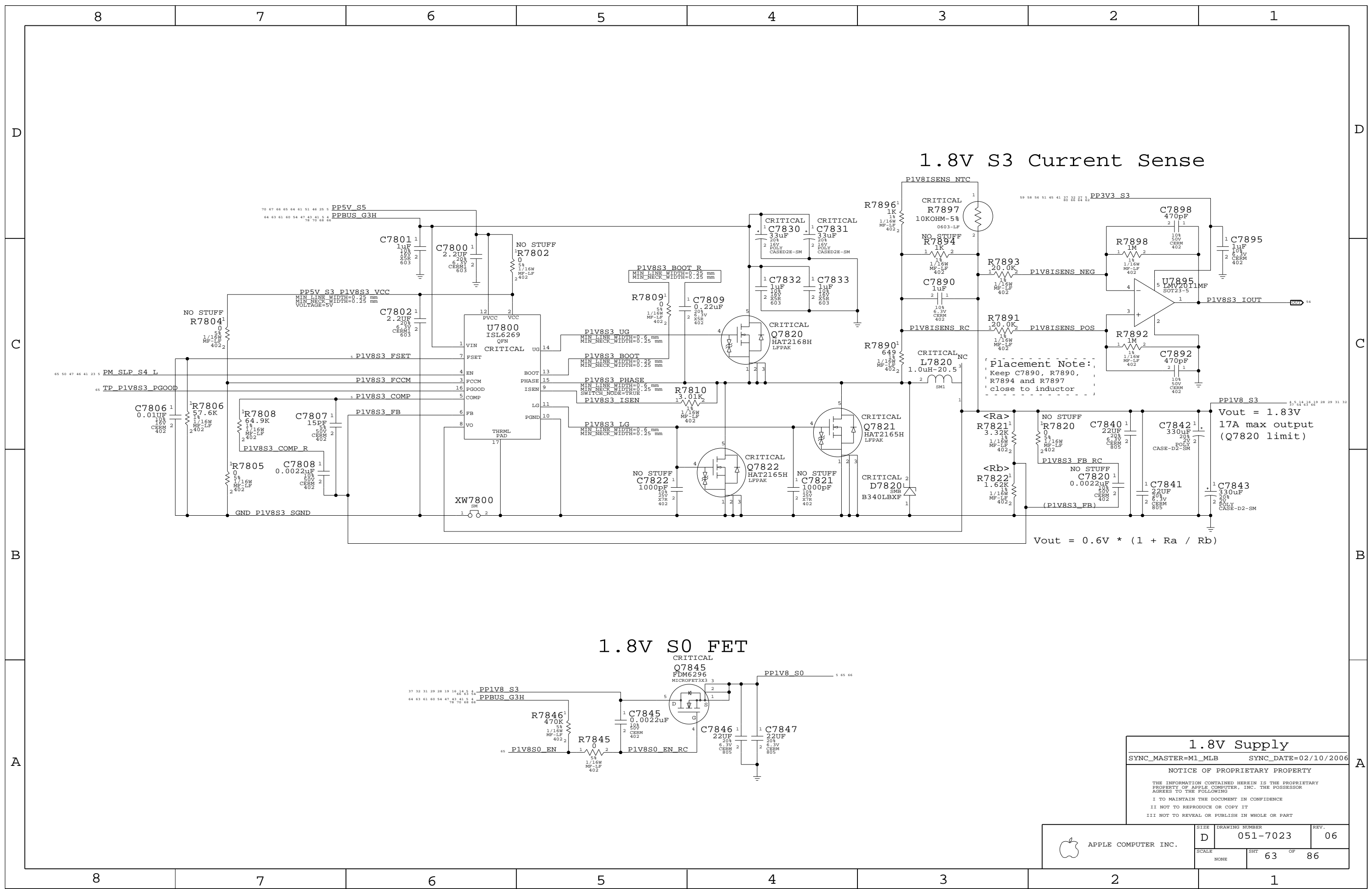
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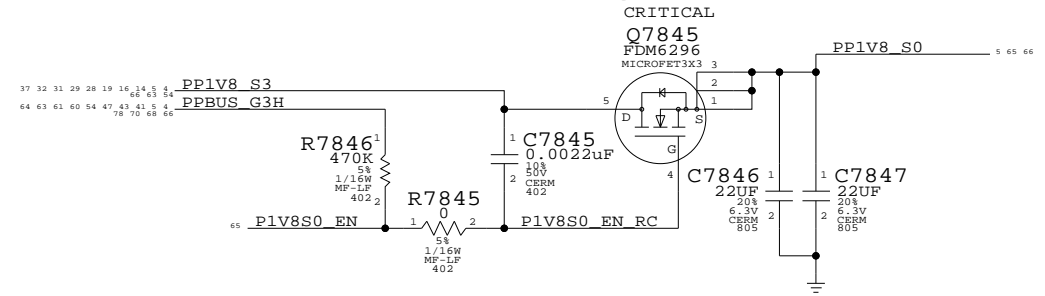
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	NONE	SHT	62 OF 86

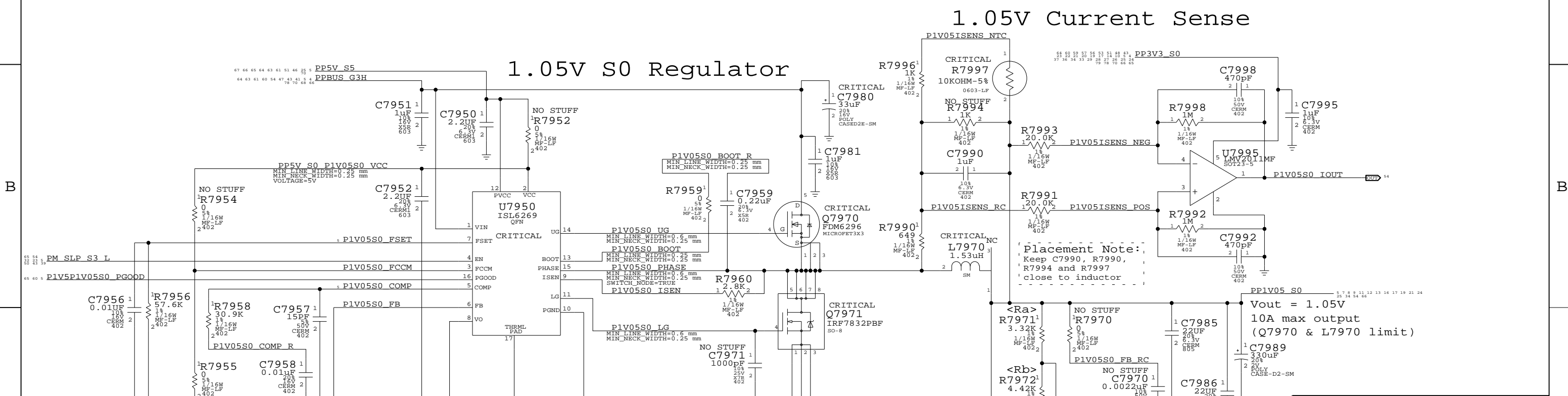
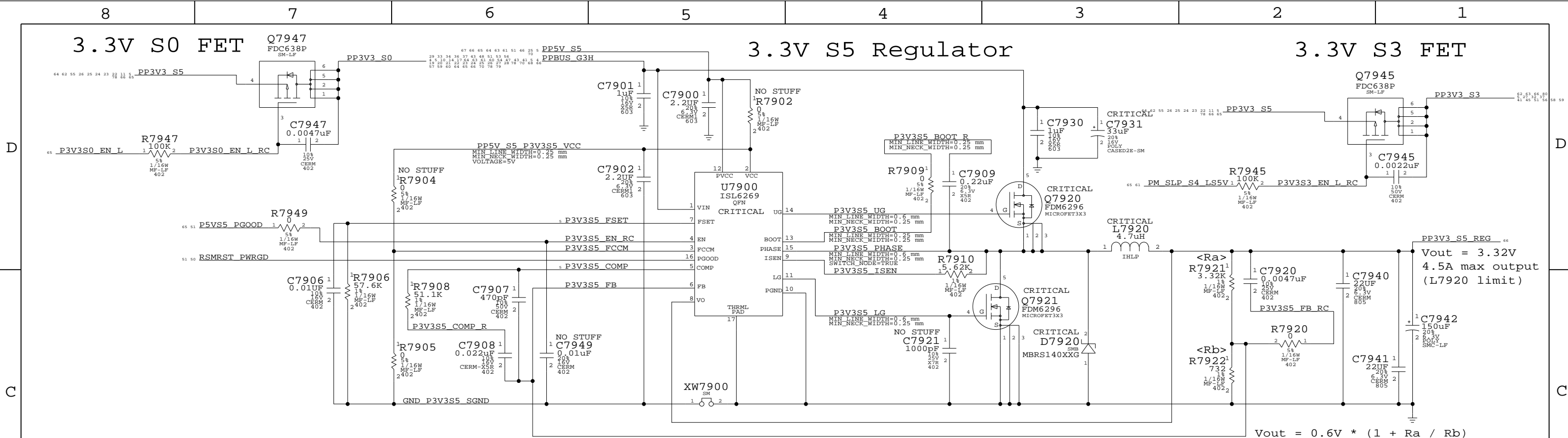


1.8V S0 FET



1.8V Supply
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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	SCALE NONE	SHEET 63	OF 86

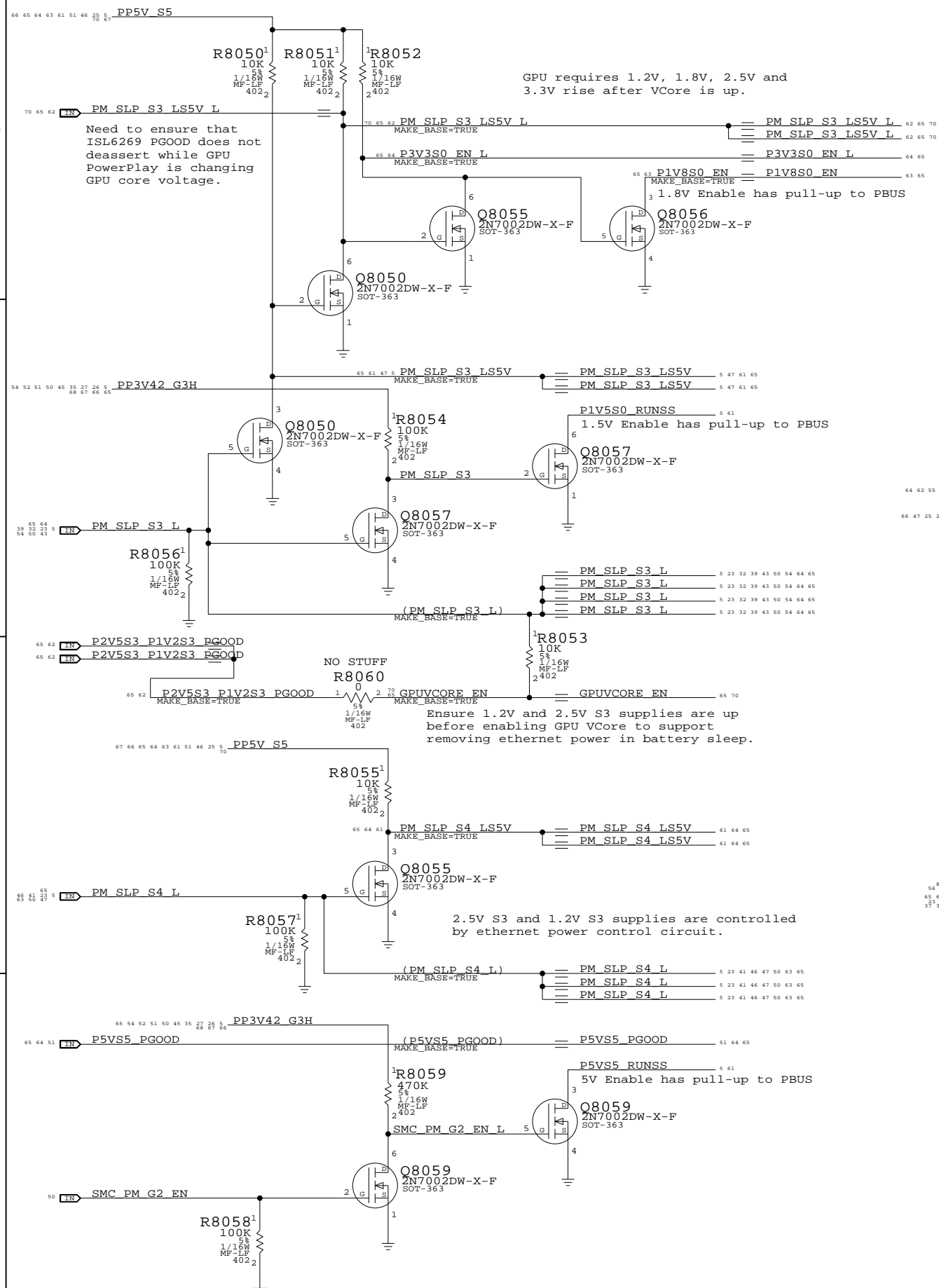


3.3V / 1.05V Power Supplies
SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF	
NONE	64	86	

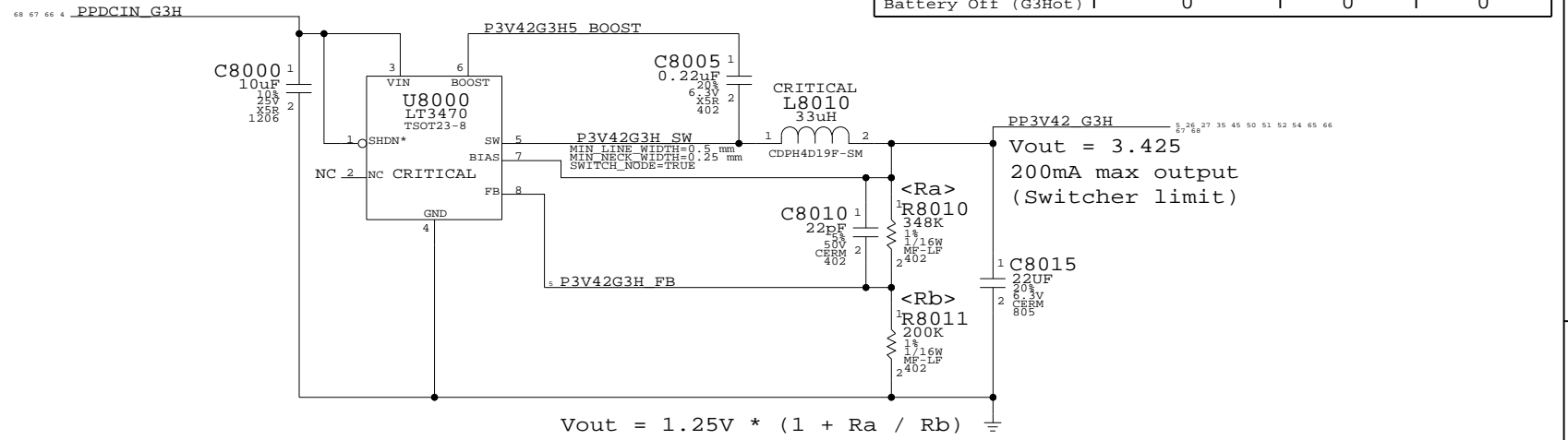
Power Control Signals



3.425V "G3Hot" Supply

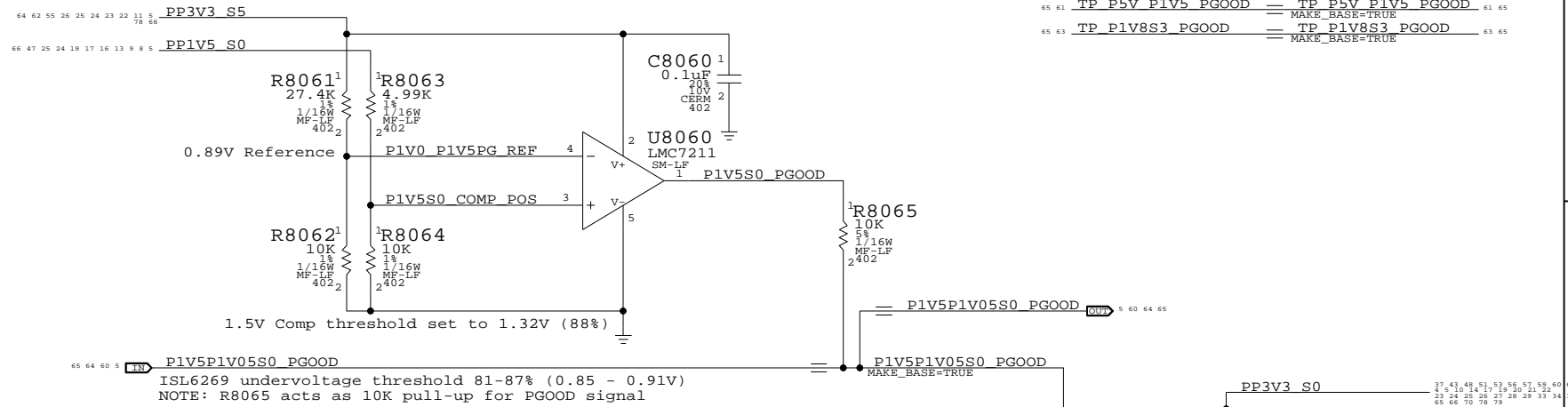
Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

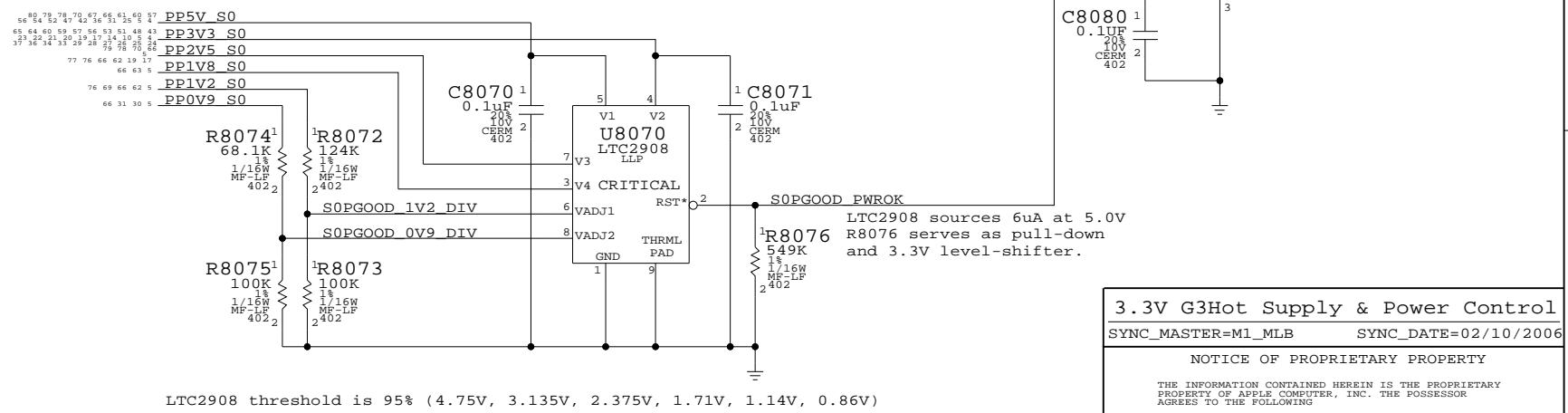


Unused PGOOD Signals

TP_P5V_P1V5_PGOOD	=	TP_P5V_P1V5_PGOOD
TP_P1V8S3_PGOOD	=	TP_P1V8S3_PGOOD

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



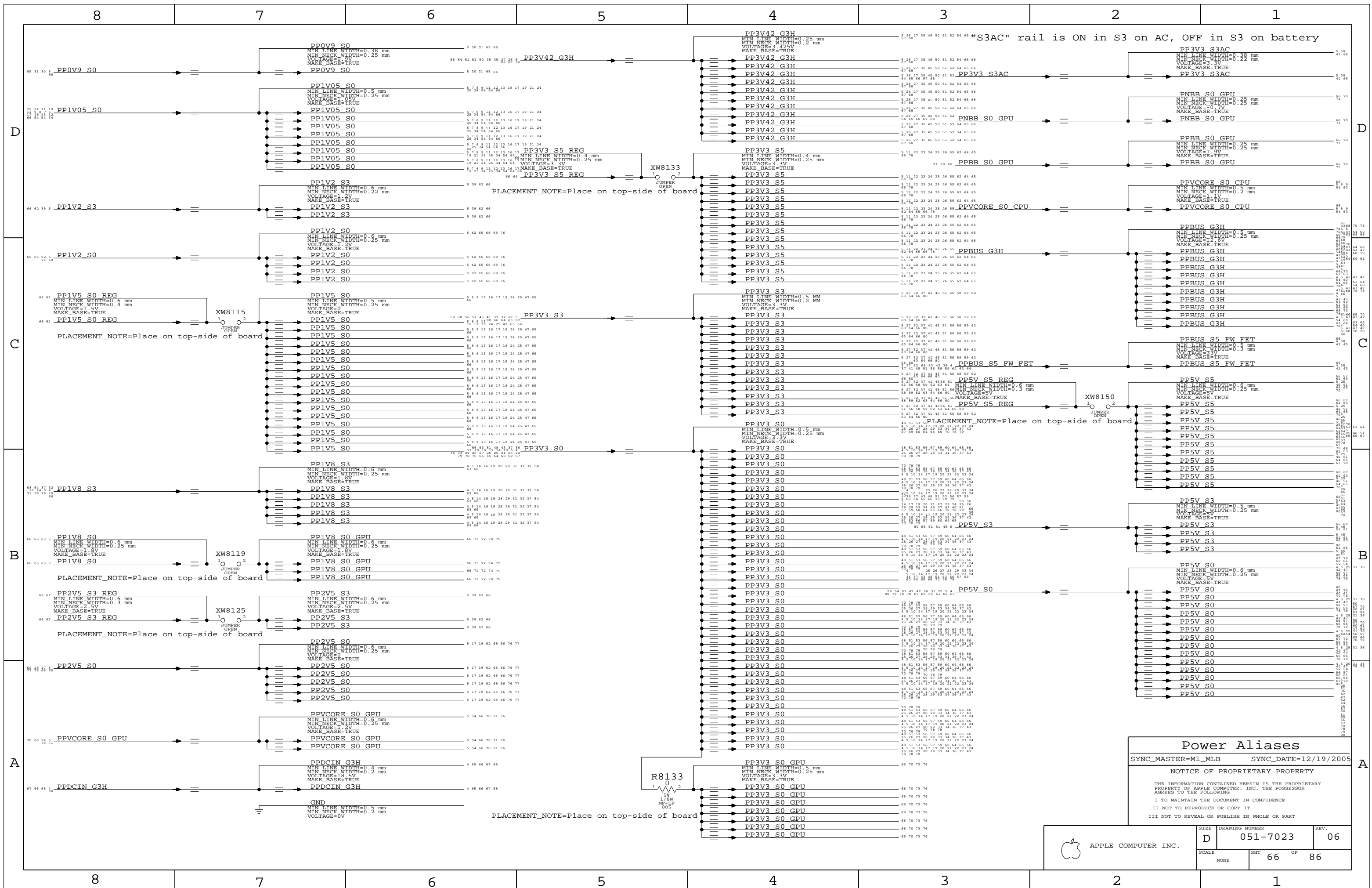
3.3V G3Hot Supply & Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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NONE	65	86	



"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PLACEMENT_NOTE=Place on top-side of board

PLACEMENT_NOTE=Place on top-side of board

PLACEMENT_NOTE=Place on top-side of board

PLACEMENT_NOTE=Place on top-side of board

Power Aliases

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

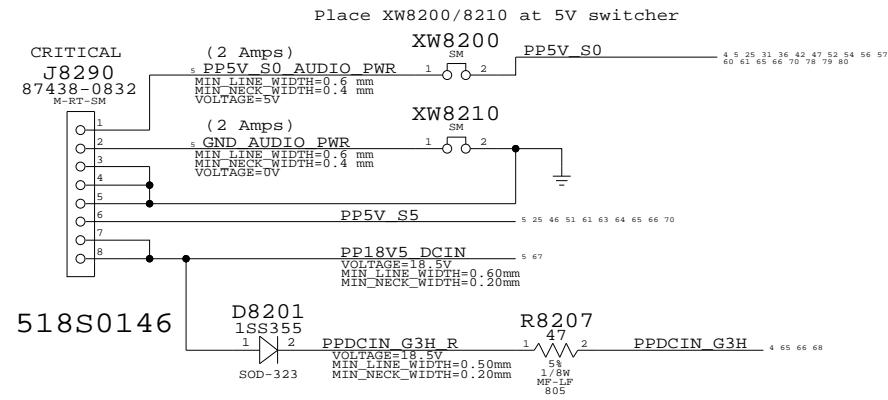
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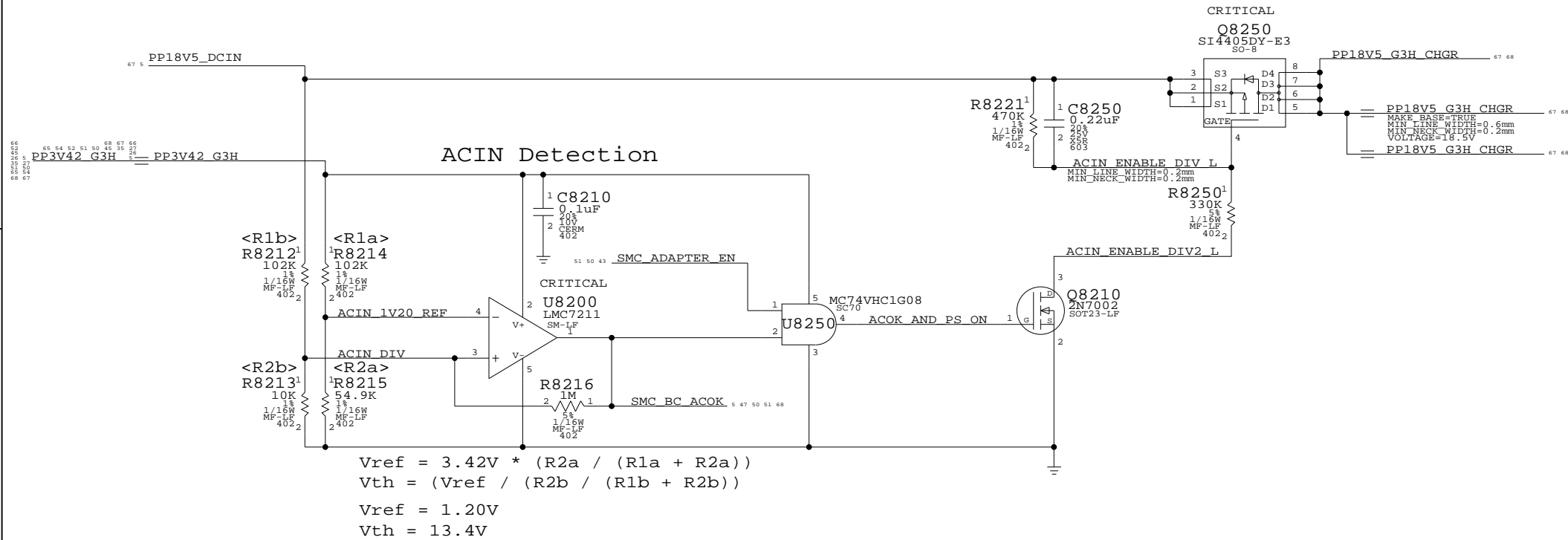
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	D	051-7023	06
SCALE	SHT	OF	
NONE	66	86	

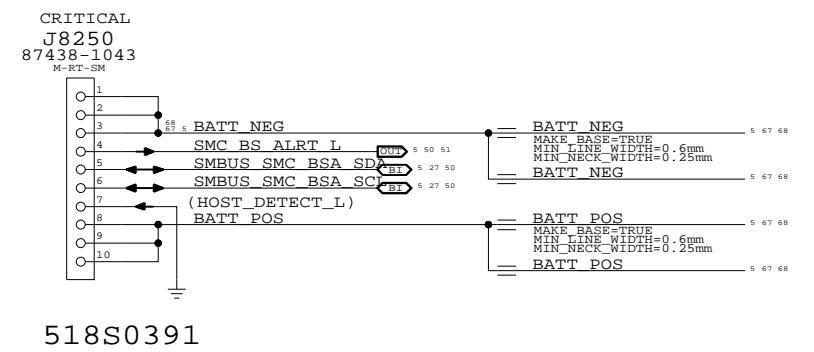
DC-In Connector



Inrush Limiter



Battery Connector



DC-In & Battery Connectors
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	67	86	

PBUS SUPPLY

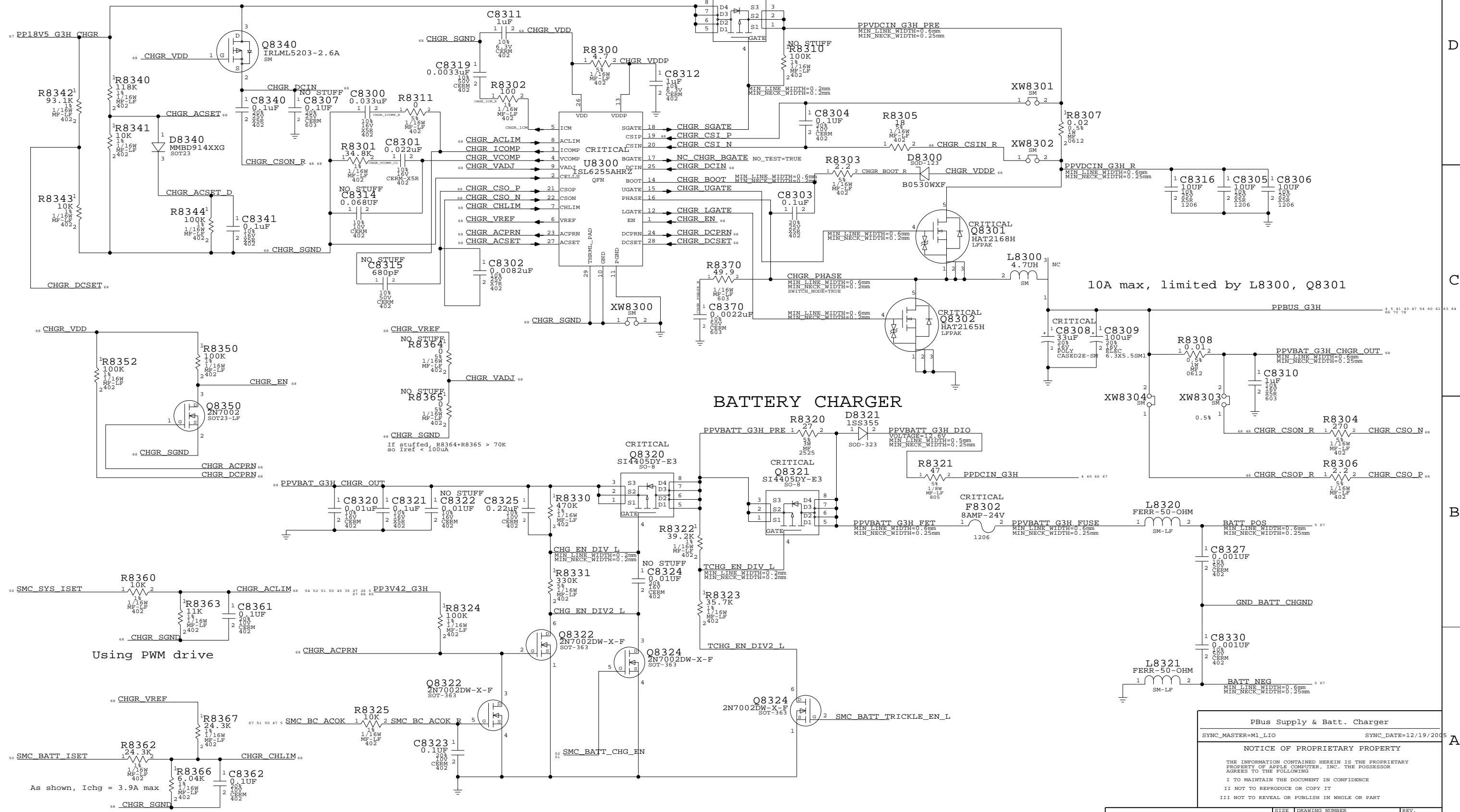
CRITICAL
Q8300
SI4405DY-E3
SO-8

BATTERY CHARGER

CRITICAL
Q8320
SI4405DY-E3
SO-8

CRITICAL
Q8321
SI4405DY-E3
SO-8

CRITICAL
F8302
8AMP-24V



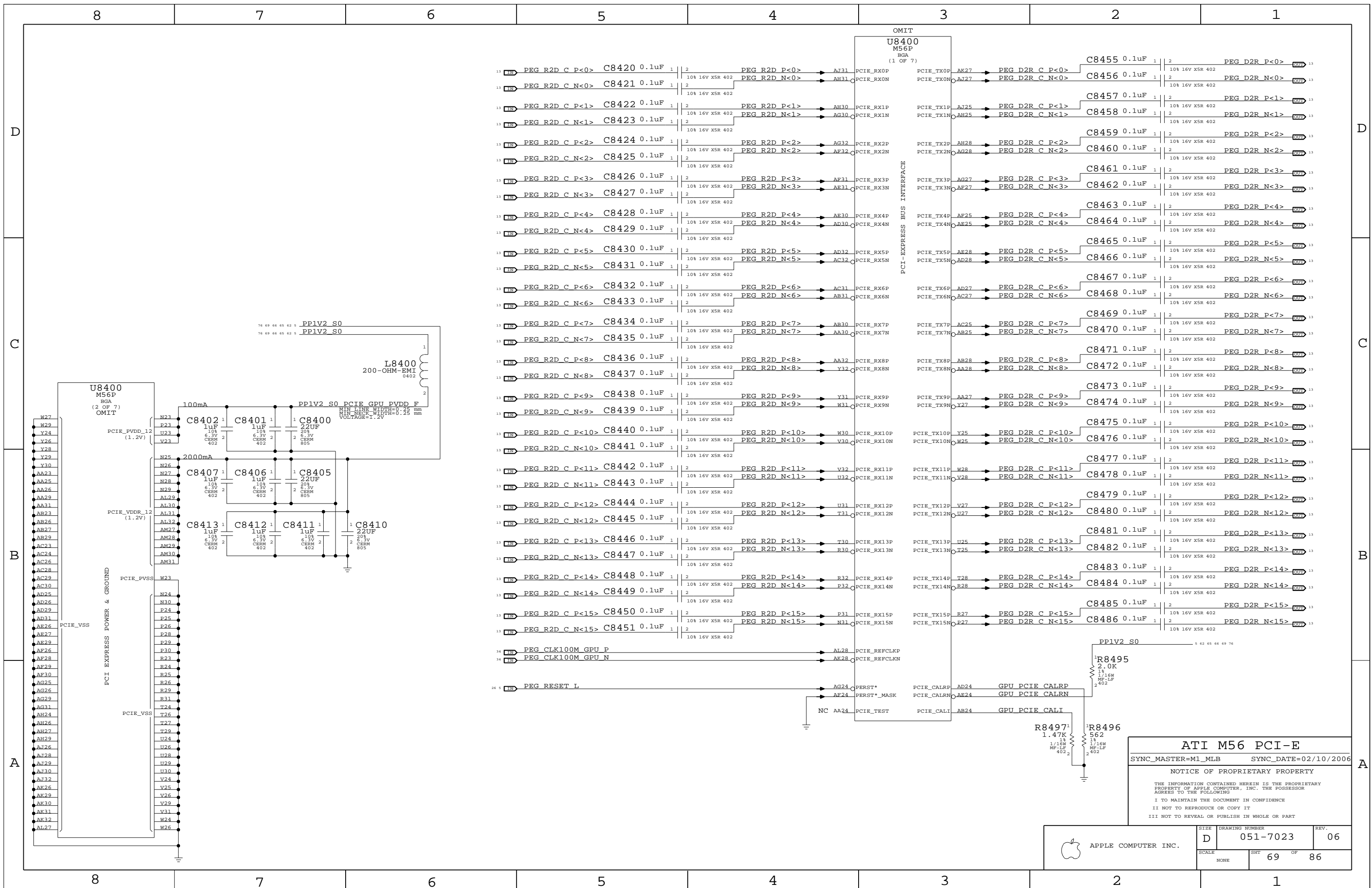
Using PWM drive

Using PWM drive

PBUS Supply & Batt. Charger
SYNC_MASTER=M1_LIO SYNC_DATE=12/19/2005

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SCALE	SHT	OF	
NONE	68	OF	86



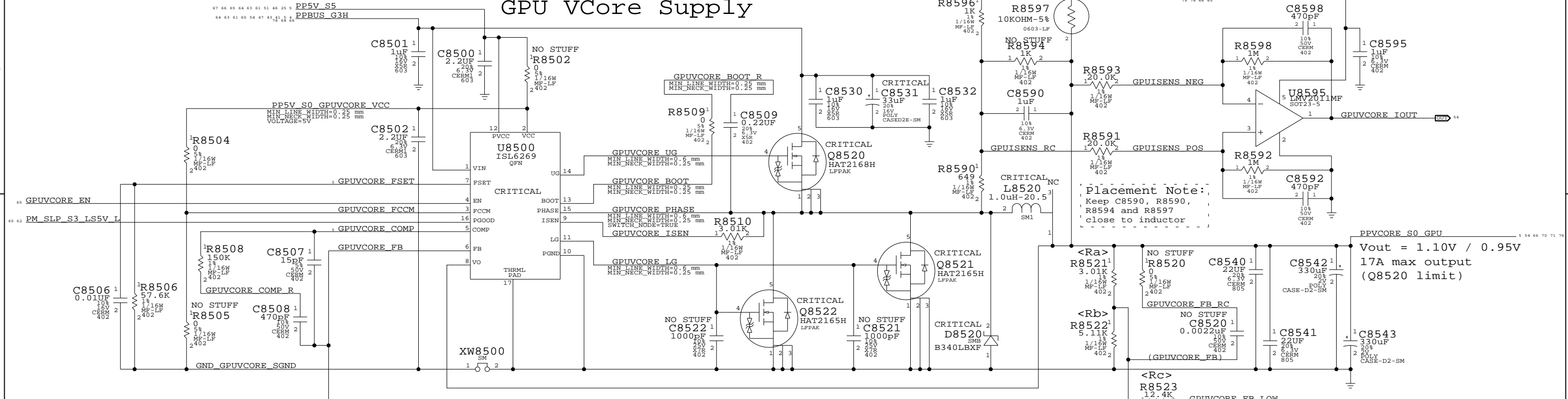
Component	Value	Pin 1	Pin 2	Signal	Pin 1	Pin 2	Signal
C8420	0.1uF	1	2	PEG R2D C P<0>	AW31	PCIE_RX0P	PEG D2R C P<0>
C8421	0.1uF	1	2	PEG R2D C N<0>	AH31	PCIE_RX0N	PEG D2R C N<0>
C8422	0.1uF	1	2	PEG R2D C P<1>	AH30	PCIE_RX1P	PEG D2R C P<1>
C8423	0.1uF	1	2	PEG R2D C N<1>	AG30	PCIE_RX1N	PEG D2R C N<1>
C8424	0.1uF	1	2	PEG R2D C P<2>	AG32	PCIE_RX2P	PEG D2R C P<2>
C8425	0.1uF	1	2	PEG R2D C N<2>	AF32	PCIE_RX2N	PEG D2R C N<2>
C8426	0.1uF	1	2	PEG R2D C P<3>	AF31	PCIE_RX3P	PEG D2R C P<3>
C8427	0.1uF	1	2	PEG R2D C N<3>	AE31	PCIE_RX3N	PEG D2R C N<3>
C8428	0.1uF	1	2	PEG R2D C P<4>	AE30	PCIE_RX4P	PEG D2R C P<4>
C8429	0.1uF	1	2	PEG R2D C N<4>	AD30	PCIE_RX4N	PEG D2R C N<4>
C8430	0.1uF	1	2	PEG R2D C P<5>	AD32	PCIE_RX5P	PEG D2R C P<5>
C8431	0.1uF	1	2	PEG R2D C N<5>	AC32	PCIE_RX5N	PEG D2R C N<5>
C8432	0.1uF	1	2	PEG R2D C P<6>	AC31	PCIE_RX6P	PEG D2R C P<6>
C8433	0.1uF	1	2	PEG R2D C N<6>	AB31	PCIE_RX6N	PEG D2R C N<6>
C8434	0.1uF	1	2	PEG R2D C P<7>	AB30	PCIE_RX7P	PEG D2R C P<7>
C8435	0.1uF	1	2	PEG R2D C N<7>	AA30	PCIE_RX7N	PEG D2R C N<7>
C8436	0.1uF	1	2	PEG R2D C P<8>	AA32	PCIE_RX8P	PEG D2R C P<8>
C8437	0.1uF	1	2	PEG R2D C N<8>	Y32	PCIE_RX8N	PEG D2R C N<8>
C8438	0.1uF	1	2	PEG R2D C P<9>	Y31	PCIE_RX9P	PEG D2R C P<9>
C8439	0.1uF	1	2	PEG R2D C N<9>	W31	PCIE_RX9N	PEG D2R C N<9>
C8440	0.1uF	1	2	PEG R2D C P<10>	W30	PCIE_RX10P	PEG D2R C P<10>
C8441	0.1uF	1	2	PEG R2D C N<10>	V30	PCIE_RX10N	PEG D2R C N<10>
C8442	0.1uF	1	2	PEG R2D C P<11>	V32	PCIE_RX11P	PEG D2R C P<11>
C8443	0.1uF	1	2	PEG R2D C N<11>	U32	PCIE_RX11N	PEG D2R C N<11>
C8444	0.1uF	1	2	PEG R2D C P<12>	U31	PCIE_RX12P	PEG D2R C P<12>
C8445	0.1uF	1	2	PEG R2D C N<12>	T31	PCIE_RX12N	PEG D2R C N<12>
C8446	0.1uF	1	2	PEG R2D C P<13>	T30	PCIE_RX13P	PEG D2R C P<13>
C8447	0.1uF	1	2	PEG R2D C N<13>	R30	PCIE_RX13N	PEG D2R C N<13>
C8448	0.1uF	1	2	PEG R2D C P<14>	R32	PCIE_RX14P	PEG D2R C P<14>
C8449	0.1uF	1	2	PEG R2D C N<14>	P32	PCIE_RX14N	PEG D2R C N<14>
C8450	0.1uF	1	2	PEG R2D C P<15>	P31	PCIE_RX15P	PEG D2R C P<15>
C8451	0.1uF	1	2	PEG R2D C N<15>	N31	PCIE_RX15N	PEG D2R C N<15>

ATI M56 PCI-E
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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SCALE	NONE	SHT	69 OF 86

GPU VCore Current Sense

GPU VCore Supply



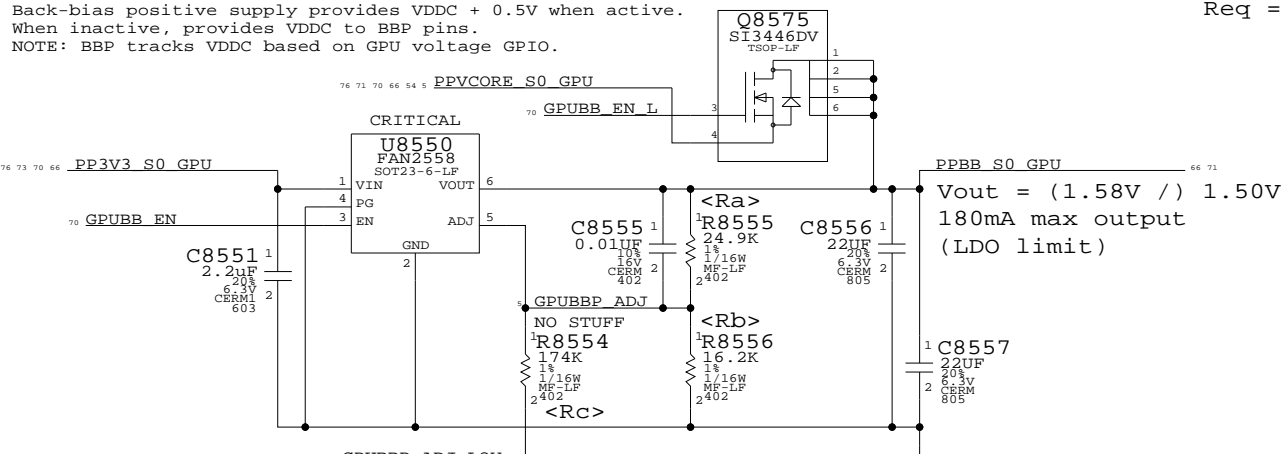
Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active. When inactive, provides VDDC to GPU pins.
NOTE: BBP tracks VDDC based on BBP voltage GPIO.

$$V_{out}(low) = 0.6V * (1 + R_a / R_b)$$

$$V_{out}(high) = 0.6V * (1 + R_a / R_{eq})$$

$$R_{eq} = R_b || R_c$$

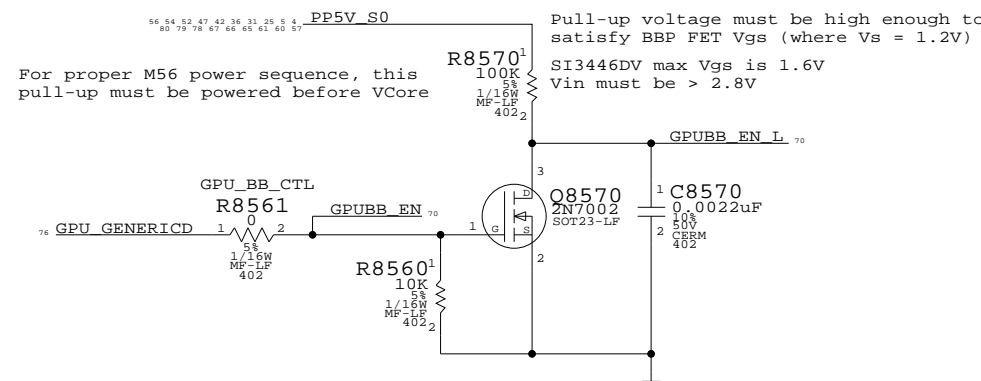
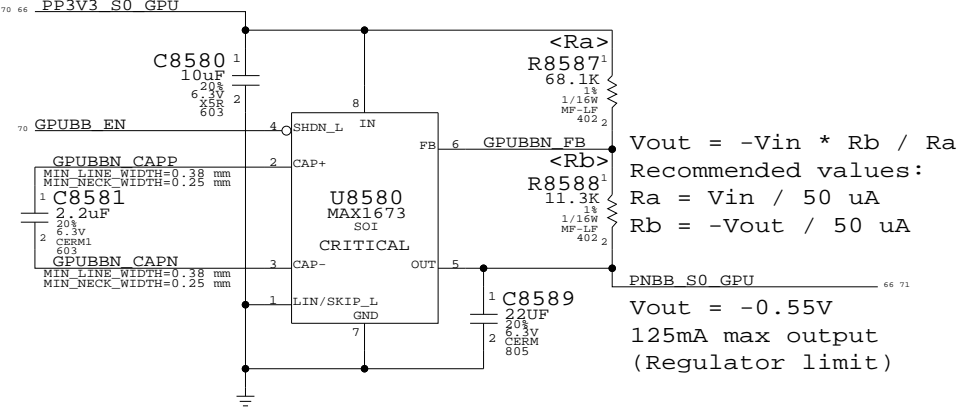


Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active. When inactive, provides VSS to BBN pins.

$$V_{out} = -V_{in} * R_b / R_a$$

Recommended values:
 $R_a = V_{in} / 50 \mu A$
 $R_b = -V_{out} / 50 \mu A$



GPU (M56) Core Supplies

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	06
SCALE	NONE	SHT 70 OF 86	

Page Notes

Power aliases required by this page:

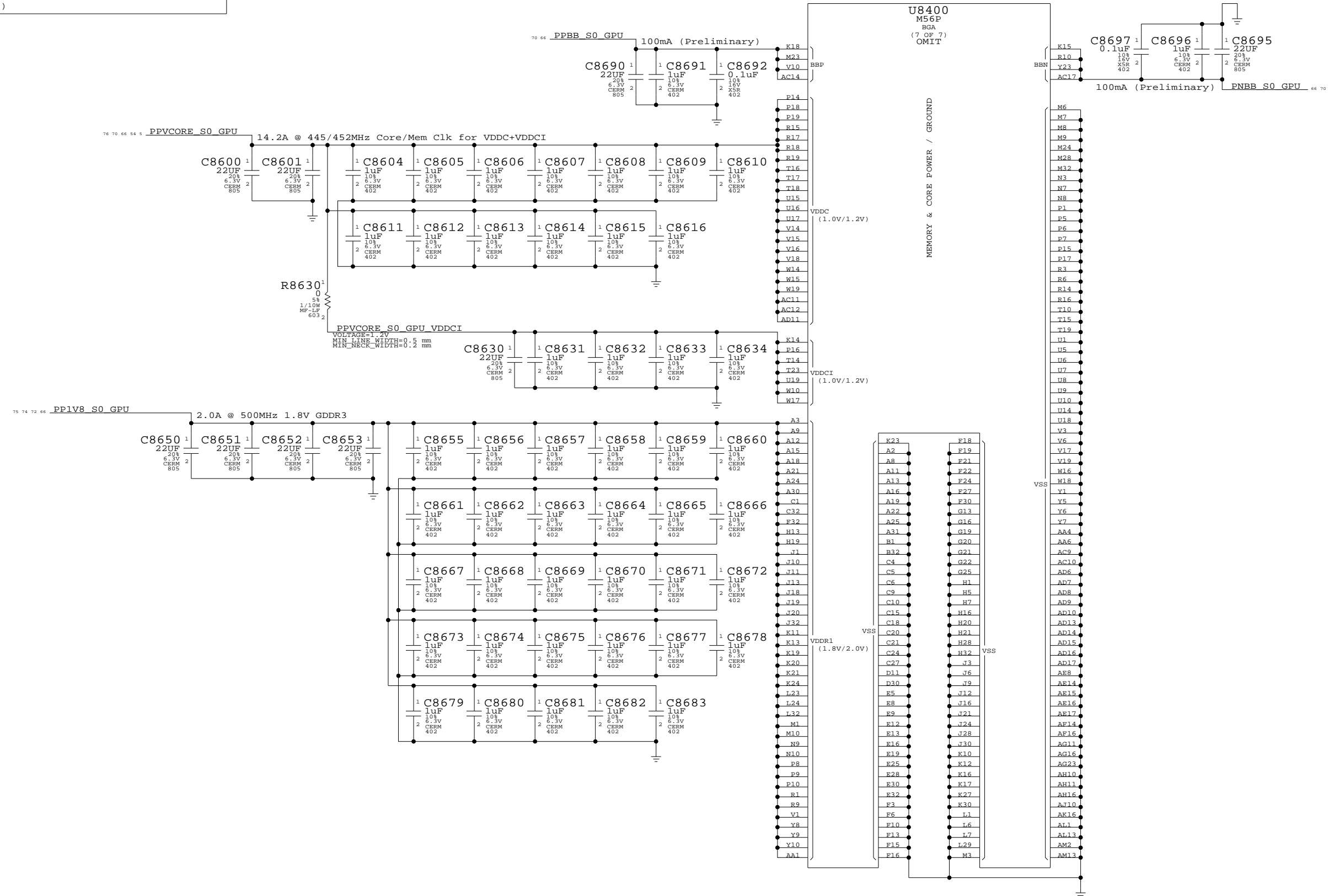
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



ATI M56 Core Power
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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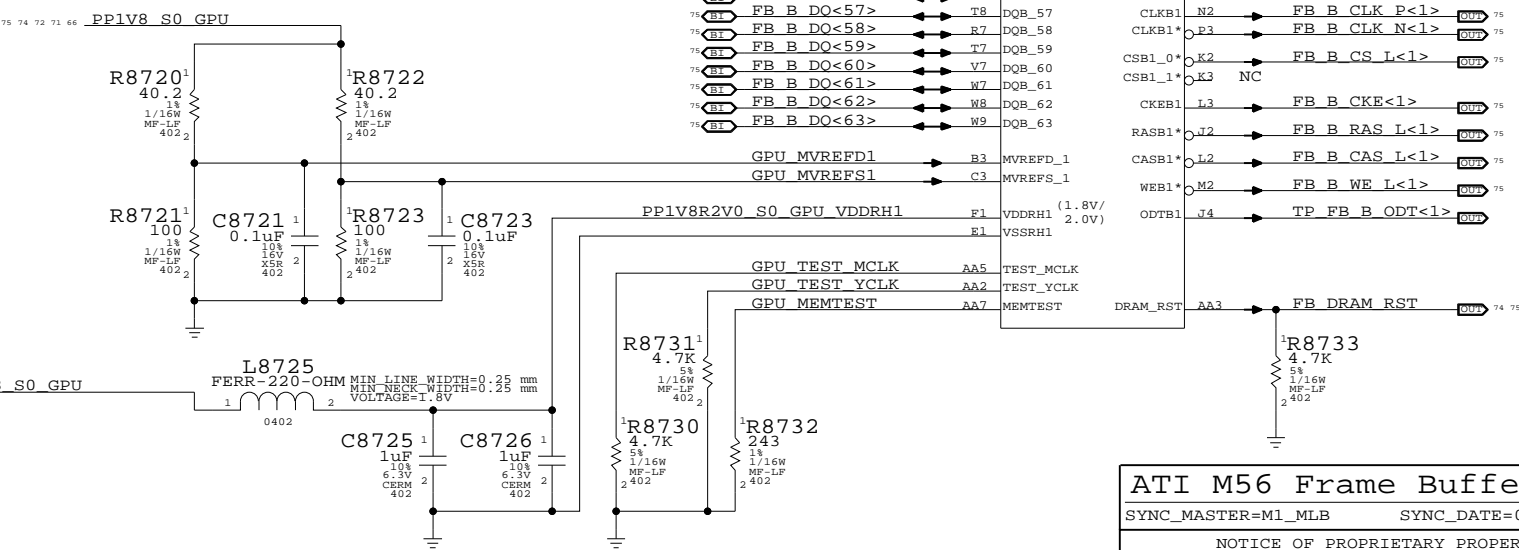
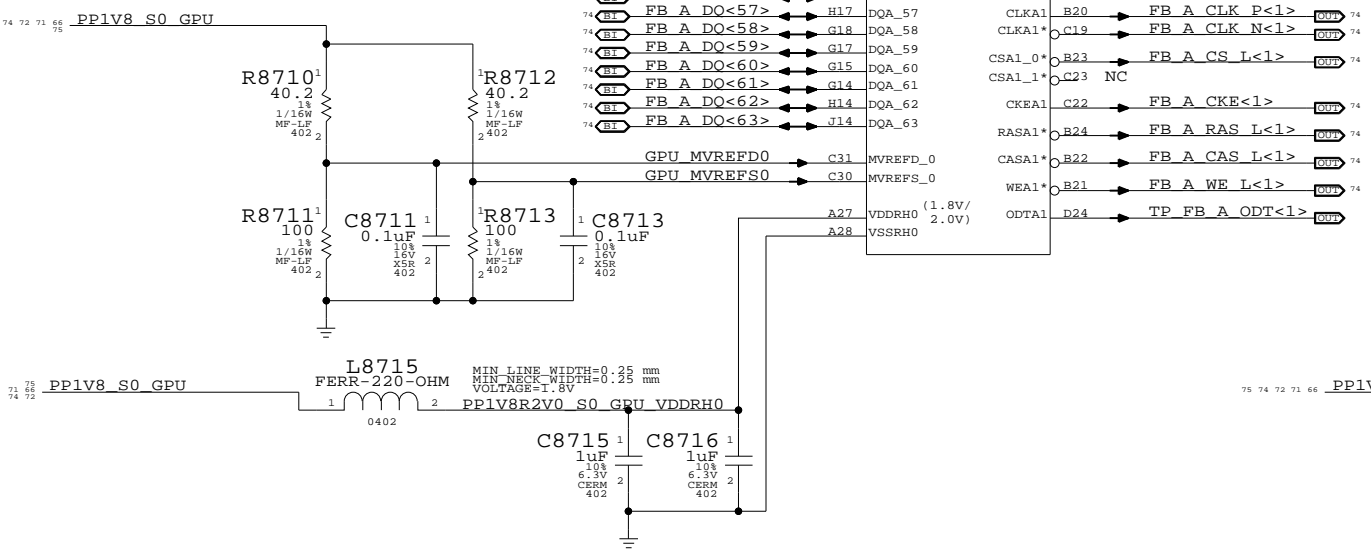
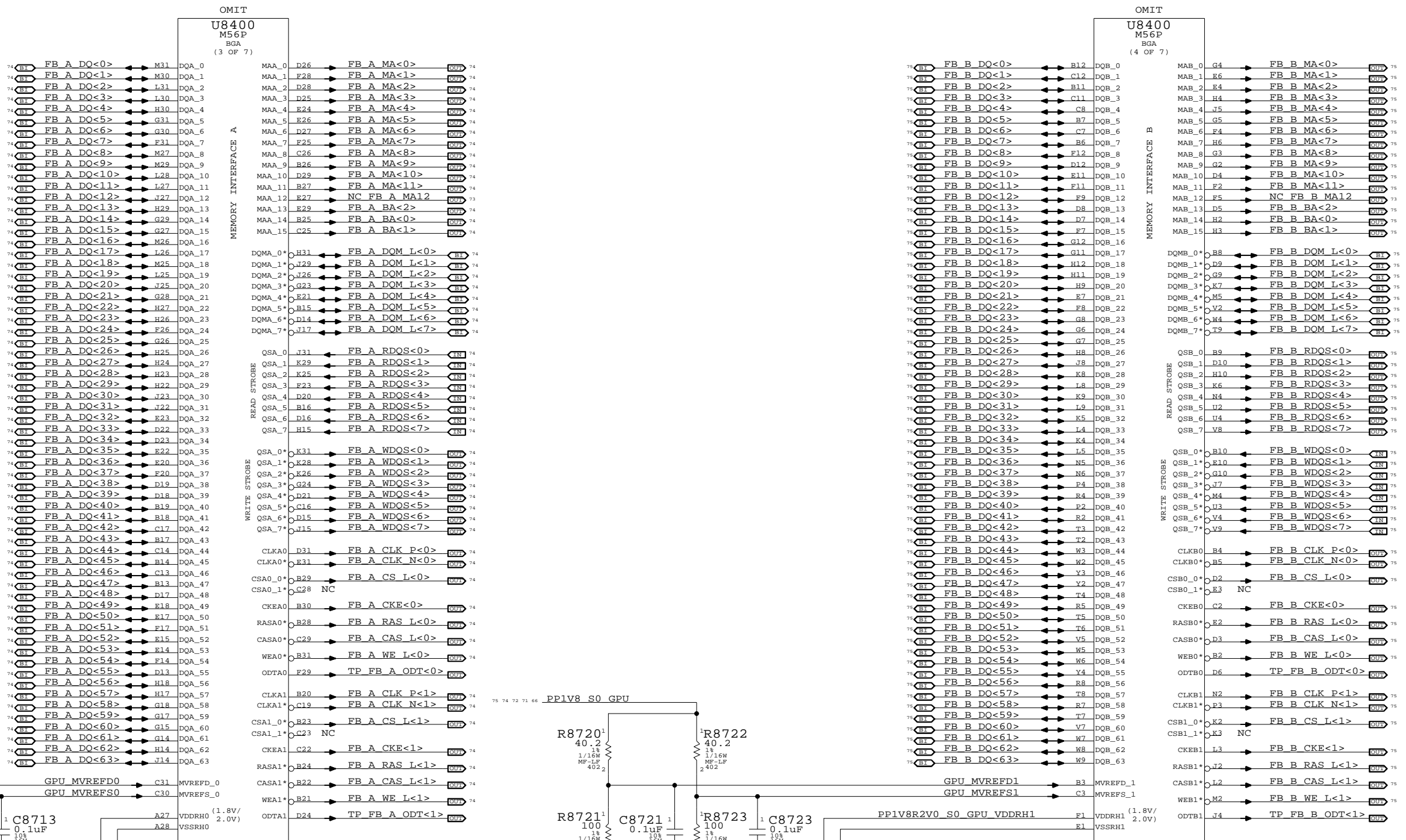
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	NONE	SHT	71 OF 86

Page Notes

Power aliases required by this page:
 - =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
 (NONE)

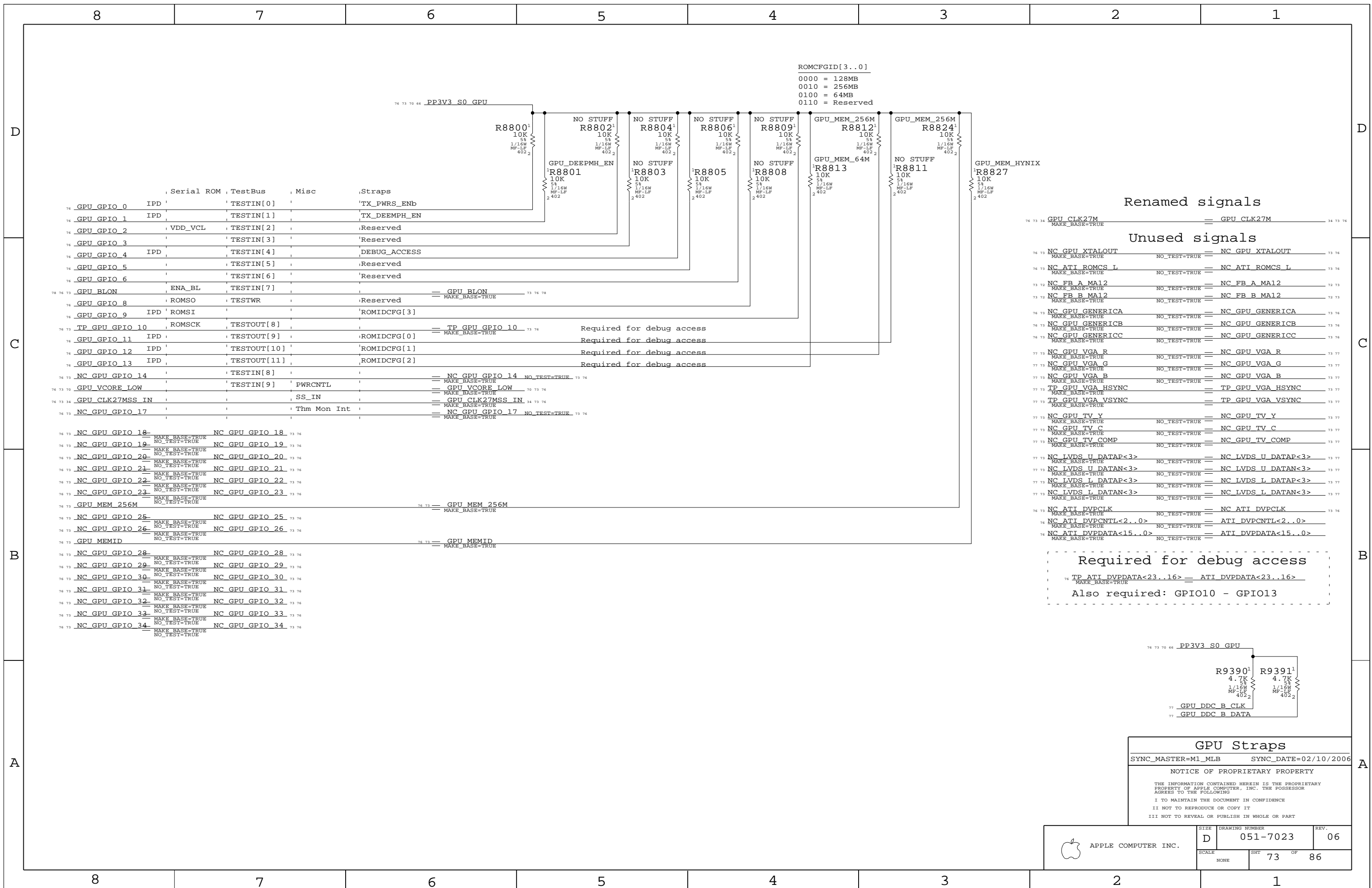
BOM options provided by this page:
 (NONE)



ATI M56 Frame Buffer I/F
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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	D	051-7023	06
SCALE	SHT	OF	
NONE	72	86	



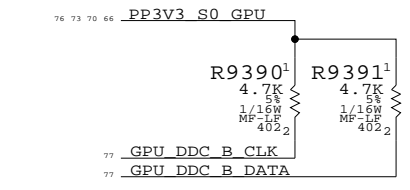
ROMCFGID[3..0]
 0000 = 128MB
 0010 = 256MB
 0100 = 64MB
 0110 = Reserved

Renamed signals

76 73 34	GPU_CLK27M	==	GPU_CLK27M	34 73 76
76 73	NC_GPU_XTALOUT	==	NC_GPU_XTALOUT	73 76
76 73	NC_ATI_ROMCS_L	==	NC_ATI_ROMCS_L	73 76
73 72	NC_FB_A_MAl2	==	NC_FB_A_MAl2	72 73
73 72	NC_FB_B_MAl2	==	NC_FB_B_MAl2	72 73
76 73	NC_GPU_GENERICA	==	NC_GPU_GENERICA	73 76
76 73	NC_GPU_GENERICB	==	NC_GPU_GENERICB	73 76
76 73	NC_GPU_GENERICC	==	NC_GPU_GENERICC	73 76
73 72	NC_GPU_VGA_R	==	NC_GPU_VGA_R	73 77
73 72	NC_GPU_VGA_G	==	NC_GPU_VGA_G	73 77
73 72	NC_GPU_VGA_B	==	NC_GPU_VGA_B	73 77
73 72	TP_GPU_VGA_HSYNC	==	TP_GPU_VGA_HSYNC	73 77
73 72	TP_GPU_VGA_VSYNC	==	TP_GPU_VGA_VSYNC	73 77
73 72	NC_GPU_TV_Y	==	NC_GPU_TV_Y	73 77
73 72	NC_GPU_TV_C	==	NC_GPU_TV_C	73 77
73 72	NC_GPU_TV_COMP	==	NC_GPU_TV_COMP	73 77
73 72	NC_LVDS_U_DATAP<3>	==	NC_LVDS_U_DATAP<3>	73 77
73 72	NC_LVDS_U_DATAN<3>	==	NC_LVDS_U_DATAN<3>	73 77
73 72	NC_LVDS_L_DATAP<3>	==	NC_LVDS_L_DATAP<3>	73 77
73 72	NC_LVDS_L_DATAN<3>	==	NC_LVDS_L_DATAN<3>	73 77
76 73	NC_ATI_DVPCCLK	==	NC_ATI_DVPCCLK	73 76
76 73	NC_ATI_DVPCNTL<2..0>	==	ATI_DVPCNTL<2..0>	73 76
76 73	NC_ATI_DVPPDATA<15..0>	==	ATI_DVPPDATA<15..0>	73 76

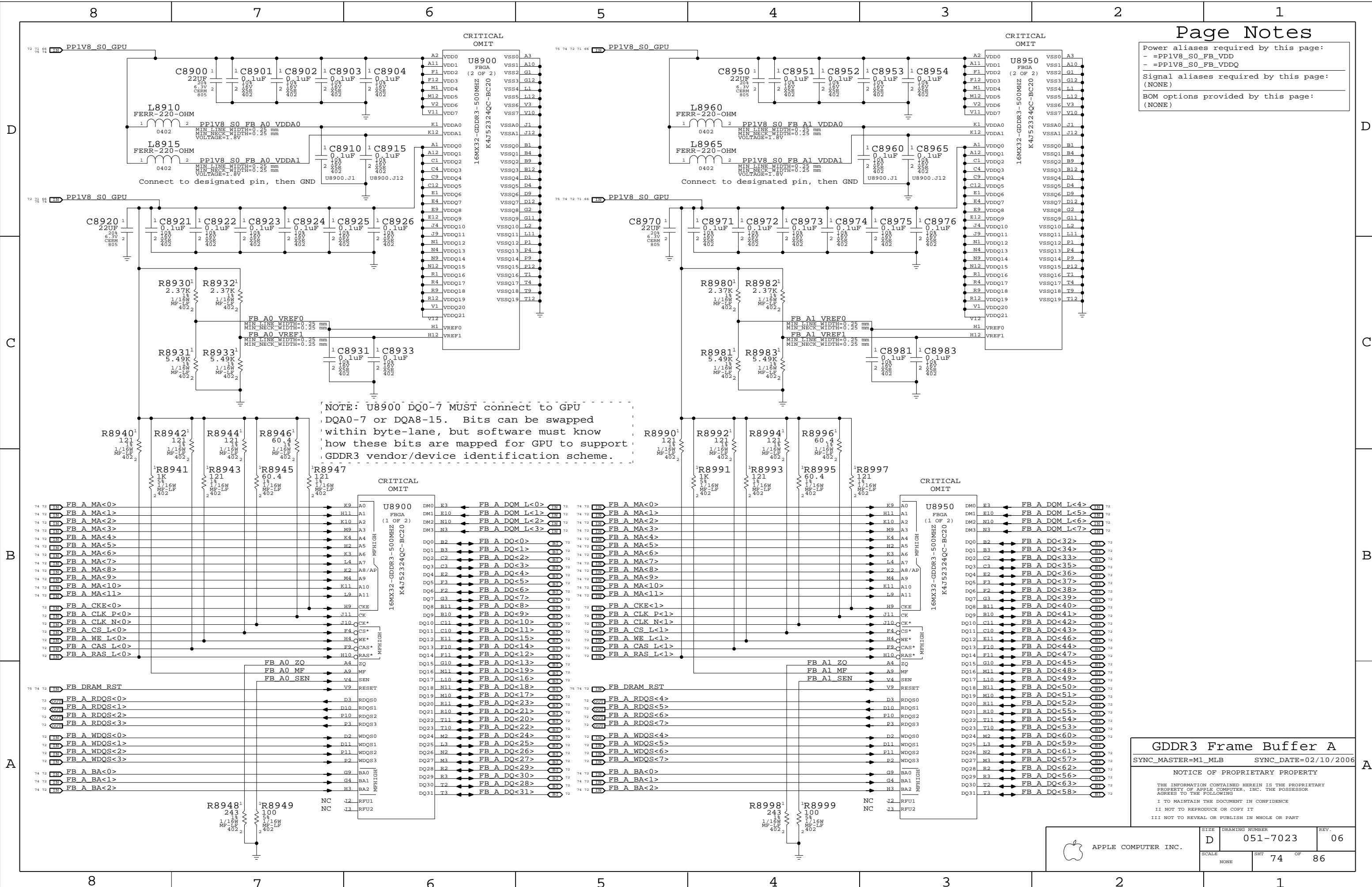
Required for debug access

TP_ATI_DVPPDATA<23..16> == ATI_DVPPDATA<23..16>
 Also required: GPIO10 - GPIO13



GPU Straps
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

GDDR3 Frame Buffer A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

NOTICE OF PROPRIETARY PROPERTY

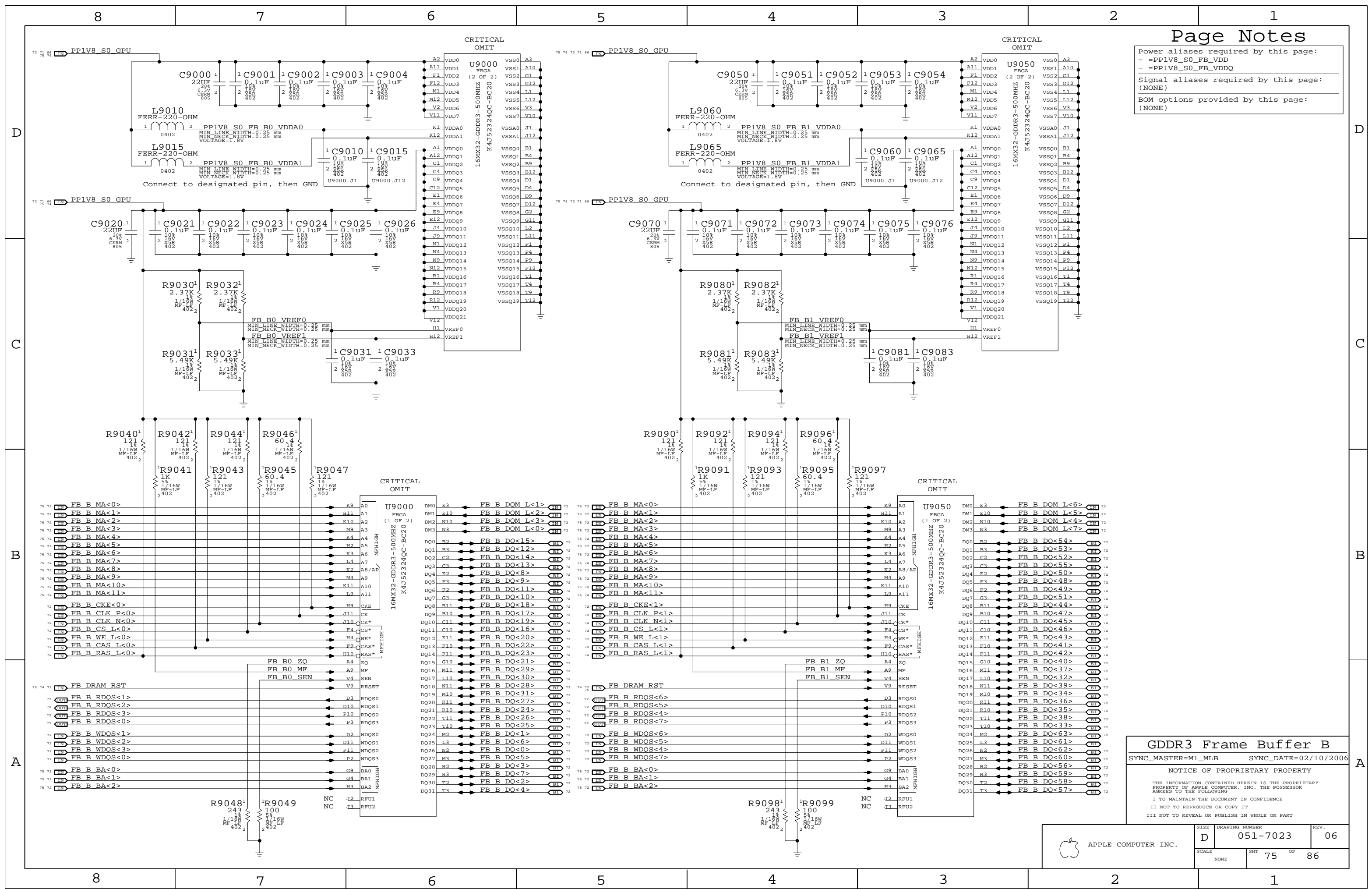
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D	051-7023	06
SCALE	SHT	OF
NONE	74	86



APPLE COMPUTER INC.

Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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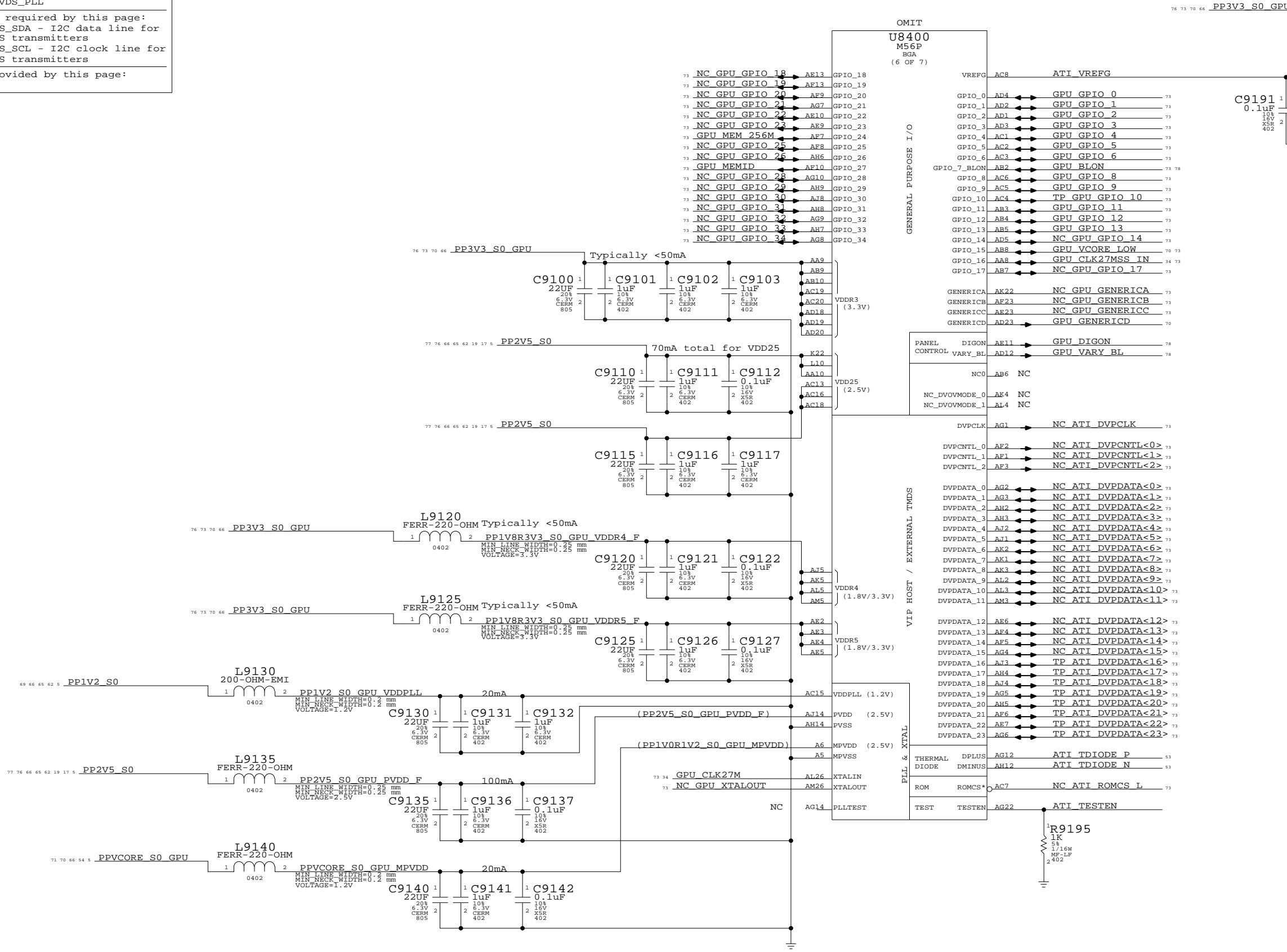
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	75	86	

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)



ATI M56 GPIO/DVO/Misc
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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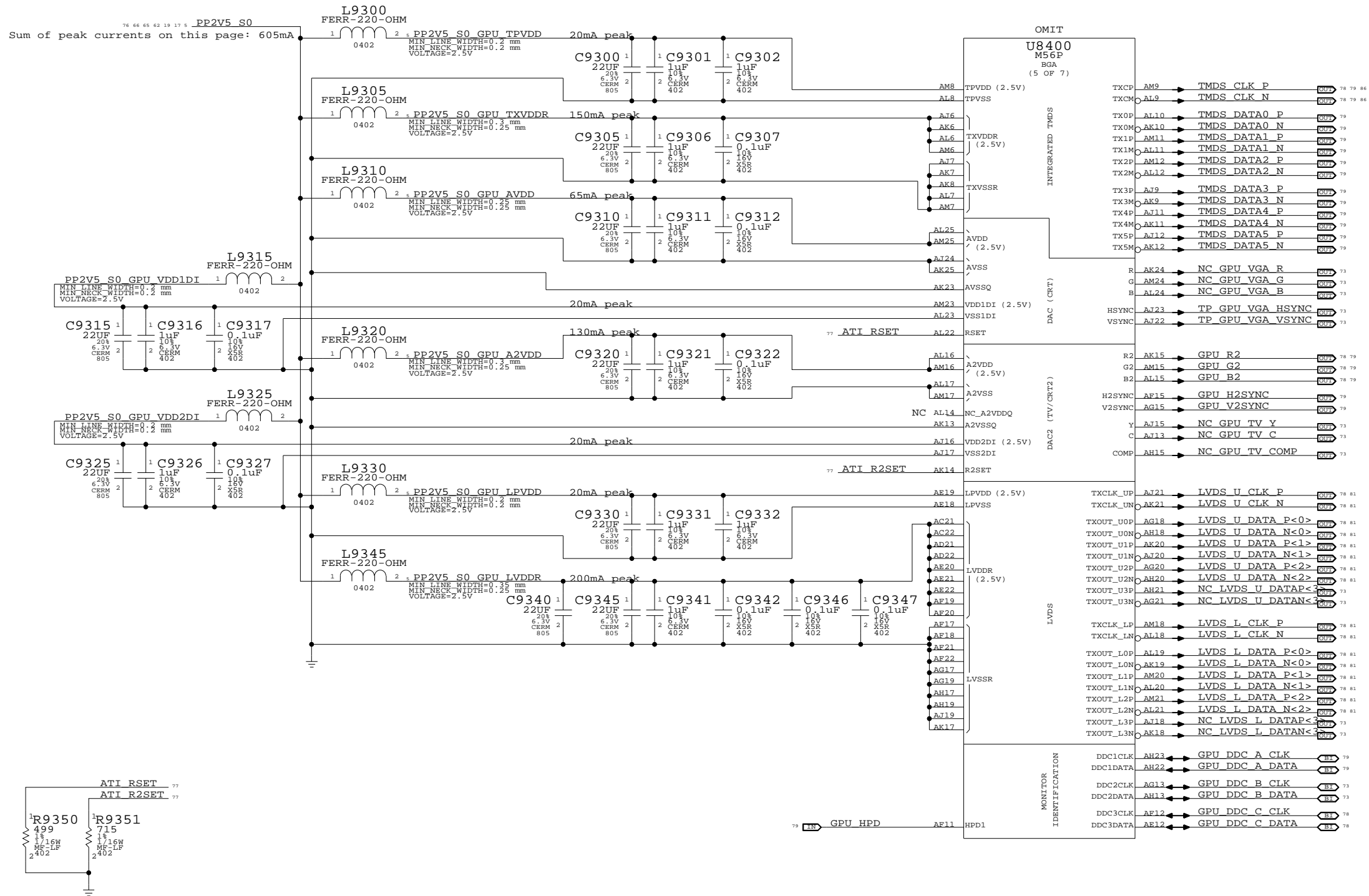
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	76	86	

Page Notes

Power aliases required by this page:
 - =PP2V5_S0_GPU
 - =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

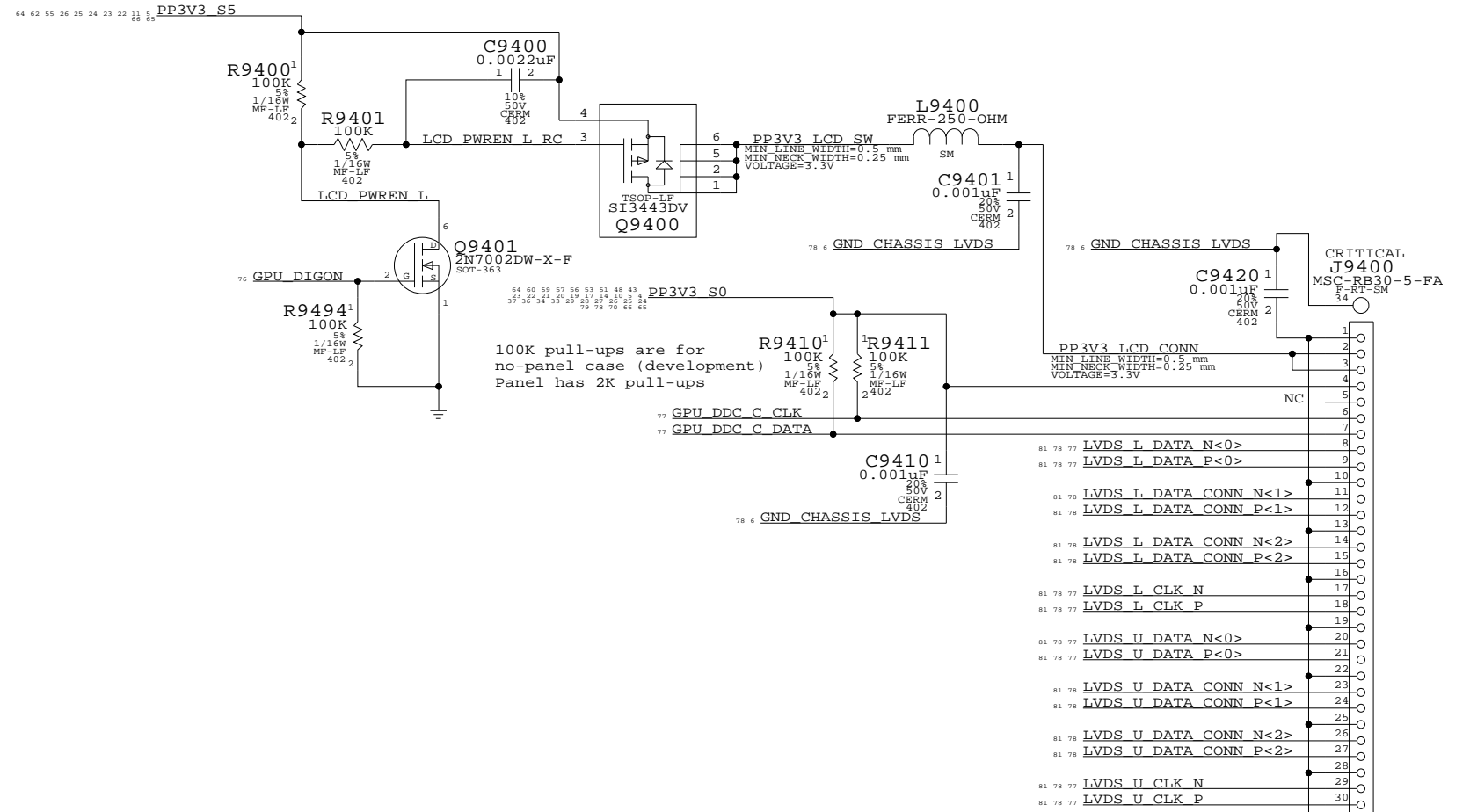
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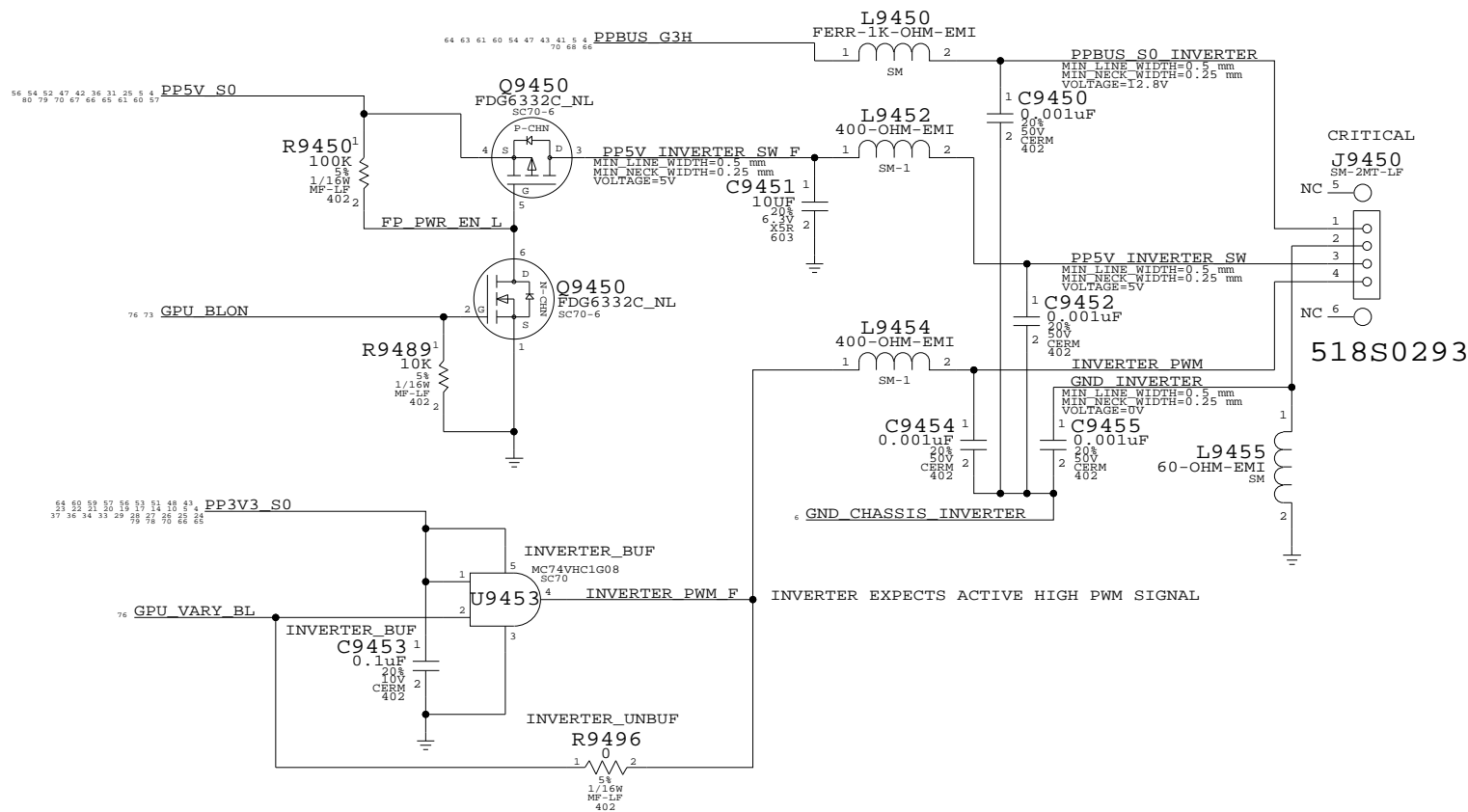
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	NONE	SHT	77 OF 86

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL		
	VGA	VGA	GPU_R2	77 79
	VGA	VGA	GPU_G2	77 79
	VGA	VGA	GPU_B2	77 79
	LVDS	LVDS	LVDS_U_CLK_P	77 78 81
	LVDS	LVDS	LVDS_U_CLK_N	77 78 81
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	77 78 81
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	77 78 81
	LVDS	LVDS	LVDS_L_CLK_P	77 78 81
	LVDS	LVDS	LVDS_L_CLK_N	77 78 81
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	77 78 81
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	77 78 81
	LVDS	LVDS	LVDS_U_CLK_P	77 78 81
	LVDS	LVDS	LVDS_U_CLK_N	77 78 81
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	78 81
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	78 81
	LVDS	LVDS	LVDS_L_CLK_P	77 78 81
	LVDS	LVDS	LVDS_L_CLK_N	77 78 81
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	78 81
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	78 81
	TMDS	TMDS	TMDS_CLK_P	77 79 86
	TMDS	TMDS	TMDS_CLK_N	77 79 86
	TMDS	TMDS	TMDS_DATA_P<5..3>	86
	TMDS	TMDS	TMDS_DATA_N<5..3>	86
	TMDS	TMDS	TMDS_DATA_P<2..0>	86
	TMDS	TMDS	TMDS_DATA_N<2..0>	86



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=01/09/2006

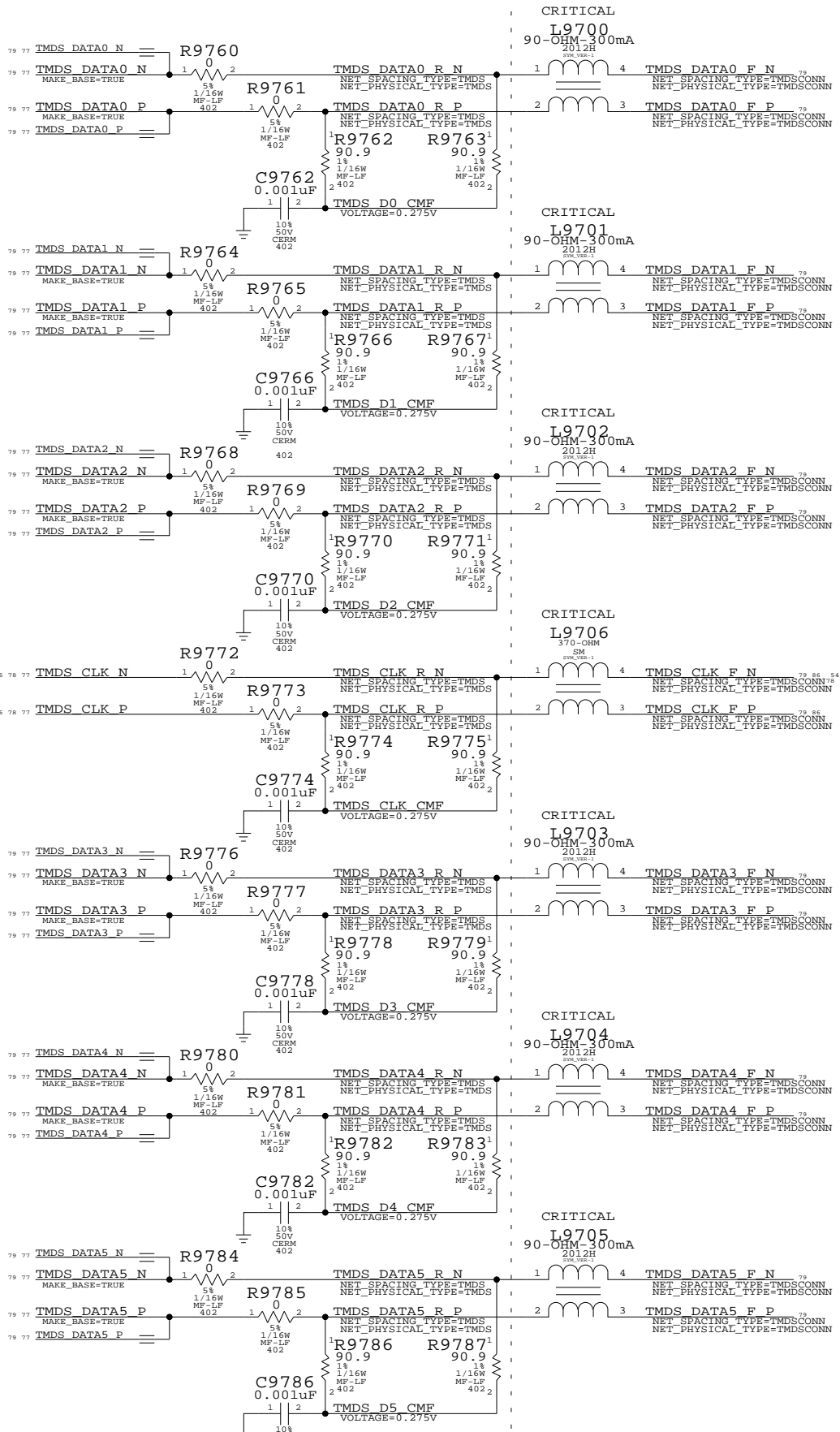
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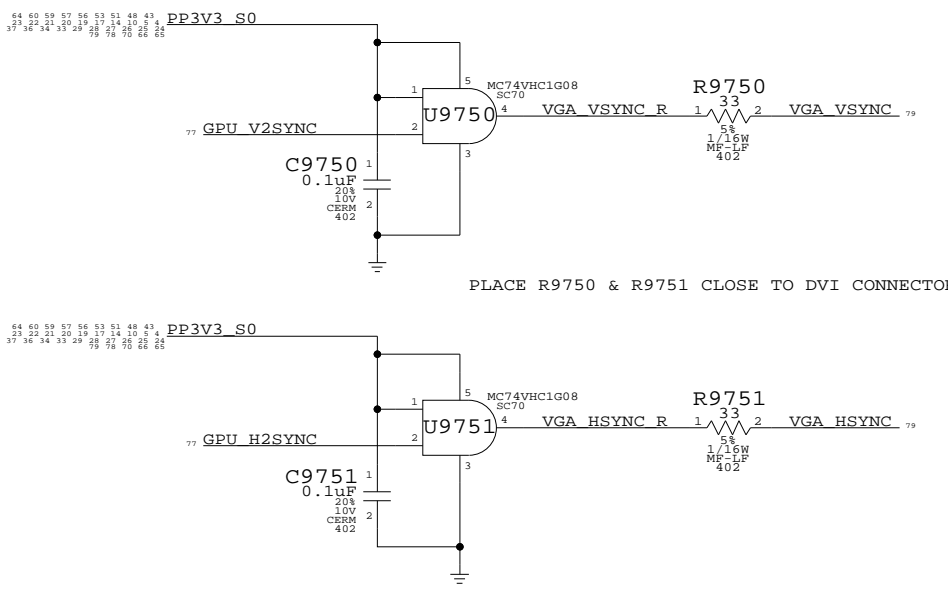
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	NONE	SHT	78 OF 86

TMDS Filtering

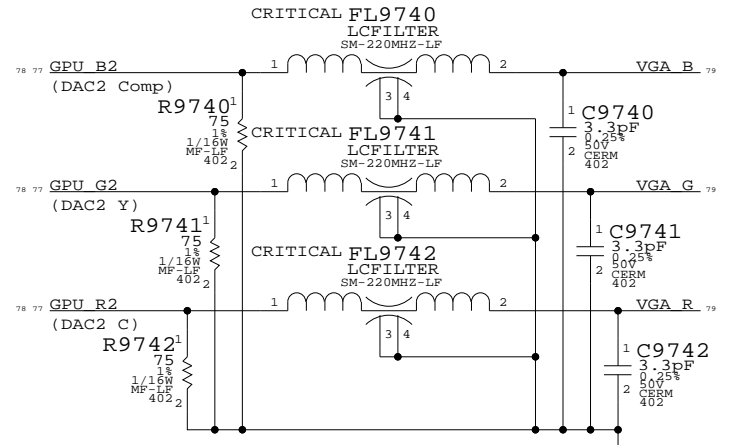
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS

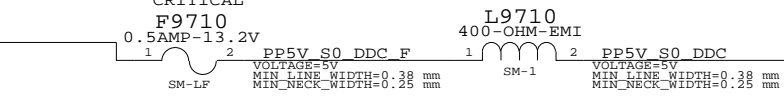


ANALOG FILTERING PLACE CLOSE TO CONNECTOR

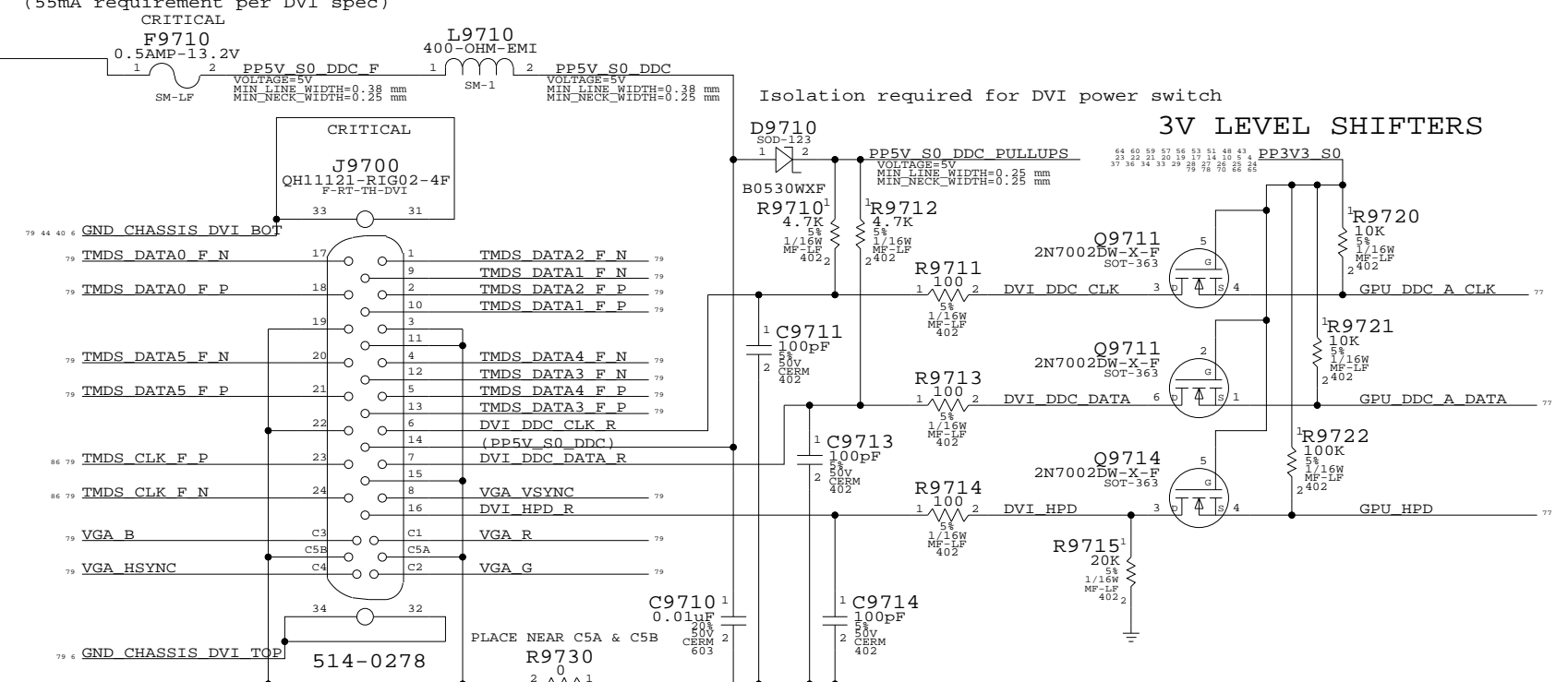


DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)



DVI INTERFACE



External Display Connector
SYNC_MASTER=M1_MLB SYNC_DATE=11/18/2005

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	D	051-7023	06
SCALE	SHT	OF	
NONE	79	OF	86

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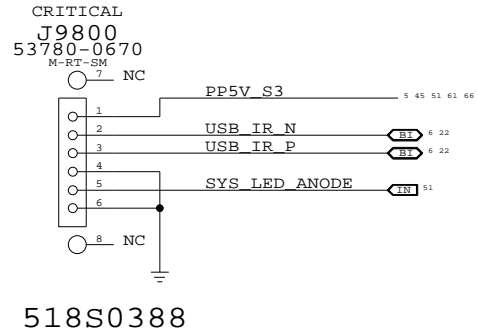
2

1

D

D

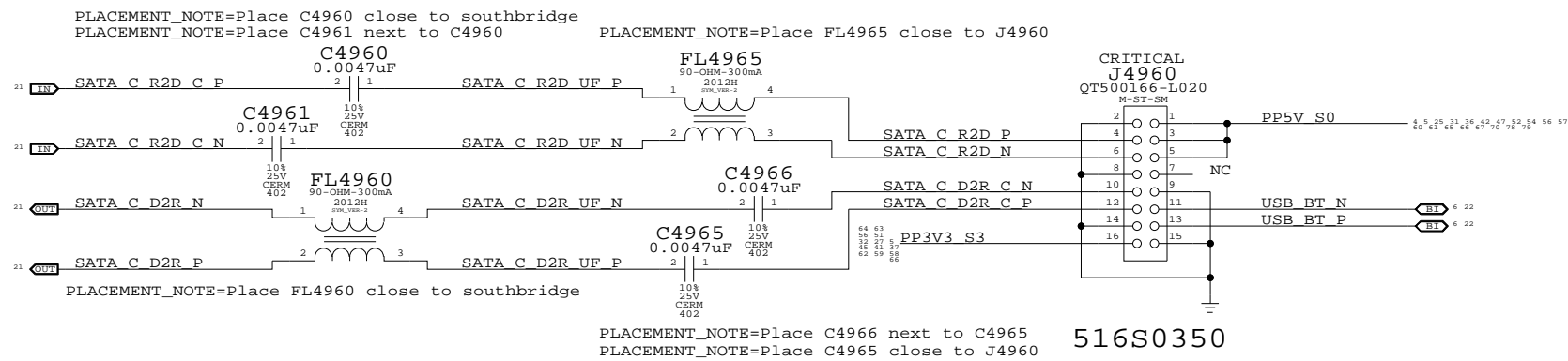
IR & Sleep LED Connector



C

C

Bluetooth (M13P) & SATA HDD Flex Connector



B

B

A

A

8

7

6

5

4

3

2

1

M9 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT 80 OF 86		
NONE			

8

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D

D

C

C

B

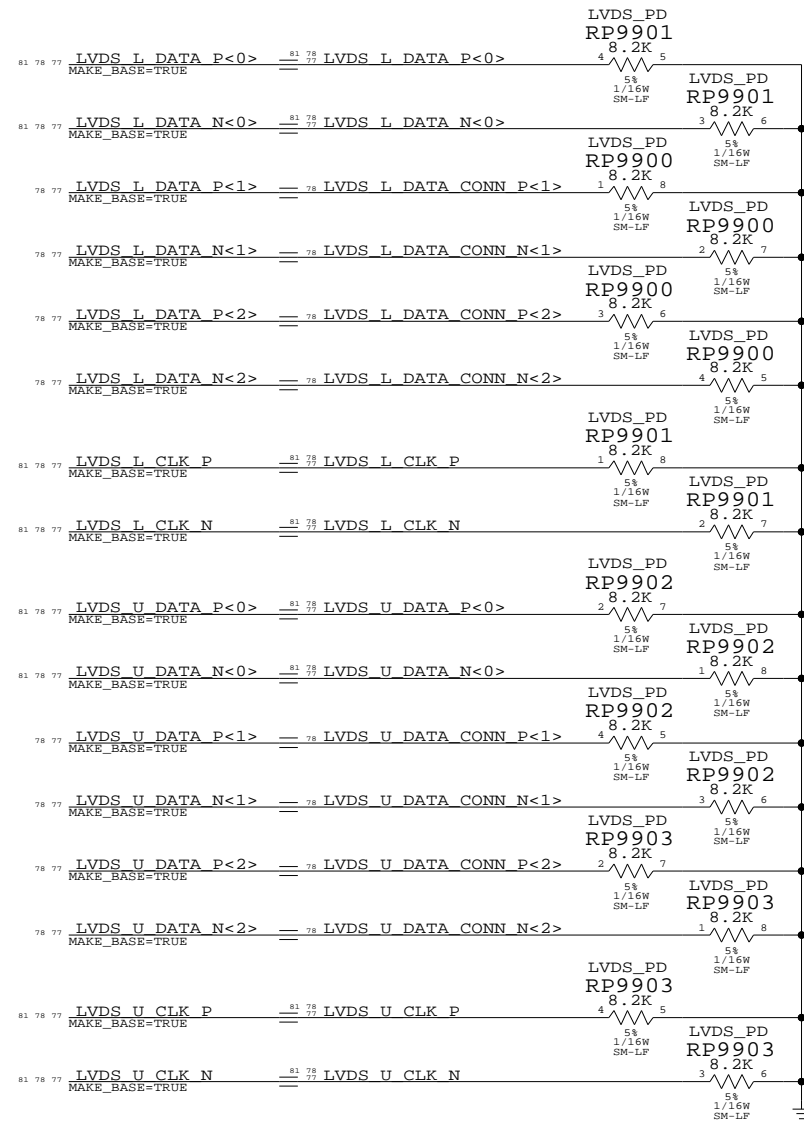
B

A

A

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs
 SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7023	06
SCALE	SHT	OF	
NONE	81	86	

8

7

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5

4

3

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1

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4

3

2

1

Revision History

Proto

11-29-05: -Release for Proto
 11-30-05: -Turned on M56_REV_B24 BOMOPTION
 12-01-05: -Added CRITICAL property to 3-pin caps, ESD diodes, and FW chokes
 -Added ITPCONN_BOMOPTION
 -RC value changes on CPU Core current sense
 -Changed IDE reset pulldown to 15K

EVT

12-01-05: -Changed L4400 to Pb-free part
 -Changed V4620 to M9 part
 -Added ESD/EMI protection to camera connector
 -Removed dual voltage support for trackpad
 -Added PM_SUS_STAT_H and PM_SLP_S5_L pulldowns

D

D

C

C

B

B

A

A

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Revision History	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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	D	051-7023	06
SCALE	SHT	OF	
NONE	82	86	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CTRL2MEM
MEM_CLK	MEM_CMD	*	MEM_CMD2MEM
MEM_CLK	MEM_DATA	*	MEM_DATA2MEM
MEM_CLK	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

Need to support MEM*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	DG says

minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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APPLE COMPUTER INC.

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D	051-7023	06
SCALE	SHEET	OF
NONE	83	86

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedance.
DQ/DQM/DQS lines are 40-ohm single-ended impedance.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedance.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedance as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF	REV.
NONE	84	86	

M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MILS OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.2
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM	
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP, BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP, BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2, ISL11	0.1 MM	?
1.8:1_SPACING	ISL2, ISL11	0.1 MM	?
2:1_SPACING	ISL2, ISL11	0.1 MM	?
2.5:1_SPACING	ISL2, ISL11	0.1 MM	?
3:1_SPACING	ISL2, ISL11	0.1 MM	?
4:1_SPACING	ISL2, ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2, ISL11	0.1 MM	?
CLK_PCIE	ISL2, ISL11	0.1 MM	?
CLK_MED	ISL2, ISL11	0.1 MM	?
CLK_SLOW	ISL2, ISL11	0.1 MM	?
CPU_COMP	ISL2, ISL11	0.1 MM	?
CPU_GTLREF	ISL2, ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2, ISL11	0.1 MM	?
DMI	ISL2, ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	?
MEM_2OTHER	ISL2, ISL11	0.1 MM	?
PCIE	ISL2, ISL11	0.1 MM	?
SATA	ISL2, ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2, ISL11	0.1 MM	?
VGA	ISL2, ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR_OVERRIDE	*	=2:1_SPACING_OVERRIDE	?
FSB_ADDR2ADDR_OVERRIDE	*	=STANDARD_OVERRIDE	?
FSB_ADSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	?
FSB_ADDR2ADSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA_OVERRIDE	*	=2:1_SPACING_OVERRIDE	?
FSB_DATA2DATA_OVERRIDE	*	=STANDARD_OVERRIDE	?
FSB_DSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	?
FSB_DATA2DSTB_OVERRIDE	*	=2:1_SPACING_OVERRIDE	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER_OVERRIDE	*	0.5 MM_OVERRIDE	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI_OVERRIDE	*	0.1 MM_OVERRIDE	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI
PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S_OVERRIDE	*	Y	0.100 MM_OVERRIDE	0.100 MM_OVERRIDE	0.100 MM_OVERRIDE	0.200 MM_OVERRIDE	0.200 MM_OVERRIDE
MEM_70D_OVERRIDE	*	Y	0.100 MM_OVERRIDE	0.100 MM_OVERRIDE	0.100 MM_OVERRIDE	0.200 MM_OVERRIDE	0.200 MM_OVERRIDE
MEM_85D_OVERRIDE	*	Y	0.100 MM_OVERRIDE	0.100 MM_OVERRIDE	0.100 MM_OVERRIDE	0.200 MM_OVERRIDE	0.200 MM_OVERRIDE

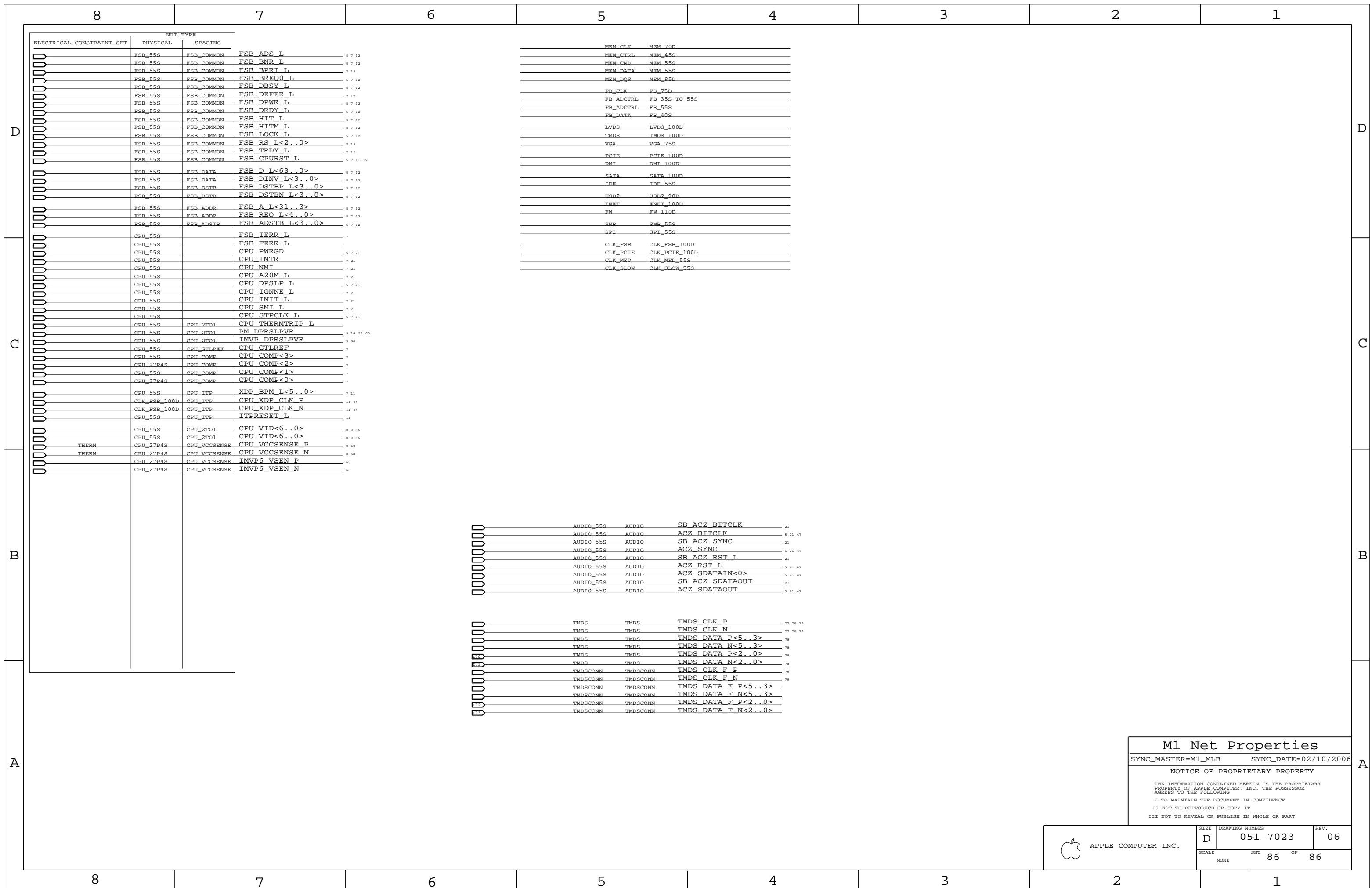
M1 Spacing & Physical Constraints
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF	
NONE	85	OF	86

D
C
B
A

D
C
B
A



ELECTRICAL_CONSTRAINT_SET	NET_TYPE	
	PHYSICAL	SPACING
FSB_55S	FSB_COMMON	FSB ADS L
FSB_55S	FSB_COMMON	FSB BNR L
FSB_55S	FSB_COMMON	FSB BPRI L
FSB_55S	FSB_COMMON	FSB BREQ0 L
FSB_55S	FSB_COMMON	FSB DBSY L
FSB_55S	FSB_COMMON	FSB DEFER L
FSB_55S	FSB_COMMON	FSB DPWR L
FSB_55S	FSB_COMMON	FSB DRDY L
FSB_55S	FSB_COMMON	FSB HIT L
FSB_55S	FSB_COMMON	FSB HITM L
FSB_55S	FSB_COMMON	FSB LOCK L
FSB_55S	FSB_COMMON	FSB RS L<2..0>
FSB_55S	FSB_COMMON	FSB TRDY L
FSB_55S	FSB_COMMON	FSB CPURST L
FSB_55S	FSB_DATA	FSB D L<63..0>
FSB_55S	FSB_DATA	FSB DINV L<3..0>
FSB_55S	FSB_DSTR	FSB DSTBP L<3..0>
FSB_55S	FSB_DSTR	FSB DSTBN L<3..0>
FSB_55S	FSB_ADDR	FSB A L<31..3>
FSB_55S	FSB_ADDR	FSB REQ L<4..0>
FSB_55S	FSB_ADSTR	FSB ADSTB L<3..0>
CPU_55S		FSB IERR L
CPU_55S		FSB FERR L
CPU_55S		CPU PWRGD
CPU_55S		CPU INTR
CPU_55S		CPU NMI
CPU_55S		CPU A20M L
CPU_55S		CPU DPSLP L
CPU_55S		CPU IGNE L
CPU_55S		CPU INIT L
CPU_55S		CPU SMI L
CPU_55S		CPU STPCLK L
CPU_55S	CPU_2T01	CPU THERMTRIP L
CPU_55S	CPU_2T01	PM DPRSLPVR
CPU_55S	CPU_2T01	IMVP DPRSLPVR
CPU_55S	CPU_GTLREF	CPU GTLREF
CPU_55S	CPU_COMP	CPU COMP<3>
CPU_27P4S	CPU_COMP	CPU COMP<2>
CPU_55S	CPU_COMP	CPU COMP<1>
CPU_27P4S	CPU_COMP	CPU COMP<0>
CPU_55S	CPU_ITP	XDP BPM L<5..0>
CLK_FSB_100D	CPU_ITP	CPU XDP CLK P
CLK_FSB_100D	CPU_ITP	CPU XDP CLK N
CPU_55S	CPU_ITP	ITPRESET L
CPU_55S	CPU_2T01	CPU VID<6..0>
CPU_55S	CPU_2T01	CPU VID<6..0>
THERM	CPU_27P4S	CPU VCCSENSE P
THERM	CPU_27P4S	CPU VCCSENSE N
	CPU_27P4S	IMVP6 VSEN P
	CPU_27P4S	IMVP6 VSEN N

MEM_CLK	MEM_70D
MEM_CTRL	MEM_45S
MEM_CMD	MEM_55S
MEM_DATA	MEM_55S
MEM_DQS	MEM_85D
FB_CLK	FB_75D
FB_ADCTRL	FB_35S_TO_55S
FB_ADCTRL	FB_55S
FB_DATA	FB_40S
LVDS	LVDS_100D
TMDS	TMDS_100D
VGA	VGA_75S
PCIE	PCIE_100D
DMI	DMI_100D
SATA	SATA_100D
IDE	IDE_55S
USB2	USB2_90D
ENET	ENET_100D
FW	FW_110D
SMB	SMB_55S
SPI	SPI_55S
CLK_FSB	CLK_FSB_100D
CLK_PCIE	CLK_PCIE_100D
CLK_MED	CLK_MED_55S
CLK_SLOW	CLK_SLOW_55S

AUDIO_55S	AUDIO	SB ACZ BITCLK	21
AUDIO_55S	AUDIO	ACZ BITCLK	5 21 47
AUDIO_55S	AUDIO	SB ACZ SYNC	21
AUDIO_55S	AUDIO	ACZ SYNC	5 21 47
AUDIO_55S	AUDIO	SB ACZ_RST_L	21
AUDIO_55S	AUDIO	ACZ_RST_L	5 21 47
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 47
AUDIO_55S	AUDIO	SB ACZ_SDATAOUT	21
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 47
TMDS	TMDS	TMDS_CLK_P	77 78 79
TMDS	TMDS	TMDS_CLK_N	77 78 79
TMDS	TMDS	TMDS_DATA_P<5..3>	78
TMDS	TMDS	TMDS_DATA_N<5..3>	78
TMDS	TMDS	TMDS_DATA_P<2..0>	78
TMDS	TMDS	TMDS_DATA_N<2..0>	78
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	79
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	79
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	79
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	79
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	79
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	79

M1 Net Properties
 SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006
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