1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB

Pansy Build - 08/10/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
03		394758	ENGINEERING RELEASE		08/10/05

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH		
820-1881	1	PCBF,MULLET,M1	PCB		
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TSQ]	CRITICAL	

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Wed Aug 10 08:42:29 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 03

SHT 1 OF 103

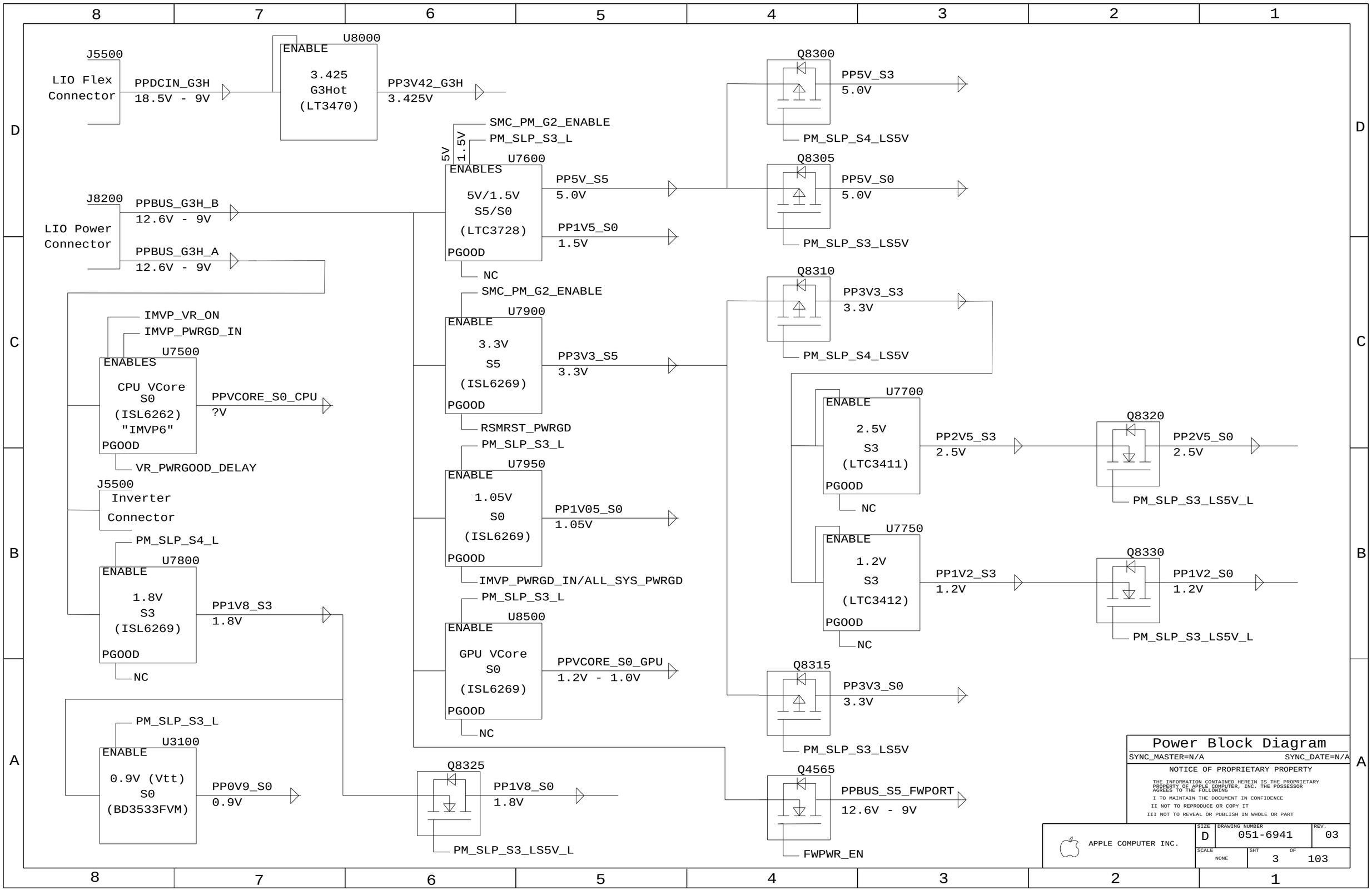
System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	2	103


J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
U7600
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
NC
PP5V_S5
5.0V
PP1V5_S0
1.5V
Q8300
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q8305
PP5V_S0
5.0V
PM_SLP_S3_LS5V
Q8310
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
U7900
SMC_PM_G2_ENABLE
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
NC
PP2V5_S3
2.5V
Q8320
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
NC
PP1V2_S3
1.2V
Q8330
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
U7500
IMVP_VR_ON
IMVP_PWRGD_IN
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
VR_PWRGOOD_DELAY
PPVCORE_S0_CPU
?V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
U8500
PM_SLP_S3_L
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
NC
PPVCORE_S0_GPU
1.2V - 1.0V
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
NC
PP1V8_S3
1.8V
U3100
PM_SLP_S3_L
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q8325
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q8315
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN
Power Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 03
SCALE NONE
SHT 3 OF 103

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7207	PCBA,MULLET_128,M1	075-0137,075-0139,075-0140
630-7254	PCBA,MULLET_256,M1	075-0138,075-0139,075-0140
075-0137	128,MULLET,M1	VRAM_128
075-0138	256,MULLET,M1	VRAM_256,GPU_MEM_256M
075-0139	PROJ_PTS,MULLET,M1	ALTERNATE,COMMON,M1_COMMON1,M1_COMMON2,M1_DEBUG
075-0140	LEMENU_PTS,MULLET,M1	LEMENU

BOM GROUP	BOM OPTIONS
M1_COMMON1	CAMERA_S3,CPUCORE_2PIN,GPU_BB_CTL,GPUTHM_A_GPU,INVERTER_BUF,KBDLED_HAS,LCD_CTL_GPU
M1_COMMON2	MEMVREF_S3,MEMVTT_EN_PU,PLTRST_GATE_STUFF,PROTO_ONLY,USB_C_OC_PU,USB_D_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0137	1	128,MULLET,M1	BOM1		075-0137
075-0138	1	256,MULLET,M1	BOM2		075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM3		075-0139
075-0140	1	LeMENU PTS,MULLET,M1	BOM4		075-0140

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
998-1175	128S0074	C0935,C0950,C0952,C0953,C0954,C1900	470uF,2.5V,7mOhm	

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	4	103

Functional Test Points

Power Supply NO_TESTs

NO_TEST

TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5VS5_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V05S0_COMP	60
TRUE	P1V05S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	7 12 76
TRUE	FSB_ADS_L	7 12 76
TRUE	FSB_ADSTB_L<1..0>	7 12 76
TRUE	FSB_BNR_L	7 12 76
TRUE	FSB_BREQ0_L	7 12 76
TRUE	FSB_D_L<63..0>	7 12 76
TRUE	FSB_DBSY_L	7 12 76
TRUE	FSB_DINV_L<3..0>	7 12 76
TRUE	FSB_DRDY_L	7 12 76
TRUE	FSB_DSTBN_L<3..0>	7 12 76
TRUE	FSB_DSTBP_L<3..0>	7 12 76
TRUE	FSB_HIT_L	7 12 76
TRUE	FSB_HITM_L	7 12 76
TRUE	FSB_LOCK_L	7 12 76
TRUE	FSB_REQ_L<4..0>	7 12 76

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST

	=PP5V_S0_FAN_LT	53 62
	FAN_LT_PWM	53
	FAN_LT_TACH	53
	FAN_RT_PWM	53
	FAN_RT_TACH	53

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 47 48
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORT80_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	50 60 62

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S3_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 76
TRUE	ACZ_SDATAOUT	21 44 76
TRUE	ACZ_BITCLK	21 44 76
TRUE	ACZ_RST_L	21 44 76
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_PS_ON	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 76
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUSA_G3H_LIO_CONN	62 63
TRUE	=PPBUSB_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	5	103

NC_CPU_A32_L — TP_CPU_A32_L
NC_CPU_A33_L — TP_CPU_A33_L
NC_CPU_A34_L — TP_CPU_A34_L
NC_CPU_A35_L — TP_CPU_A35_L
NC_CPU_A36_L — TP_CPU_A36_L
NC_CPU_A37_L — TP_CPU_A37_L
NC_CPU_A38_L — TP_CPU_A38_L
NC_CPU_A39_L — TP_CPU_A39_L
NC_CPU_APM0_L — TP_CPU_APM0_L
NC_CPU_APM1_L — TP_CPU_APM1_L
NC_CPU_EXTBREF — TP_CPU_EXTBREF
NC_CPU_HFPLL — TP_CPU_HFPLL
NC_CPU_SPARE0 — TP_CPU_SPARE0
NC_CPU_SPARE1 — TP_CPU_SPARE1
NC_CPU_SPARE2 — TP_CPU_SPARE2
NC_CPU_SPARE4 — TP_CPU_SPARE4

MAKE_BASE=TRUE
NO_TEST=TRUE

NC_MEM_A_A<15..14> — MEM_A_A<15..14>
NC_MEM_B_A<15..14> — MEM_B_A<15..14>
TP_NB_CFG<4..3> — NB_CFG<4..3>
TP_NB_CFG<6> — NB_CFG<6>
TP_NB_CFG<8> — NB_CFG<8>
TP_NB_CFG<11..10> — NB_CFG<11..10>
TP_NB_CFG<15..14> — NB_CFG<15..14>
TP_NB_CFG<17> — NB_CFG<17>

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12>

TP_SB_SUS_CLK — SUS_CLK_SB
NC_ENET_CTRL12 — ENET_CTRL12
NC_ENET_CTRL25 — ENET_CTRL25
NC_FWPWR_PWRON — =FWPWR_PWRON
FW_PC0

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P — USB2_RT_P — USB_A_P
=USB2_RT_N — USB2_RT_N — USB_A_N
=RTUSB_OC_L — RTUSB_OC_L — USB_A_OC_L

MAKE_BASE=TRUE

USB Port "B" = PCI-E Mini Card

=USB2_MINI_P — USB2_MINI_P — USB_B_P
=USB2_MINI_N — USB2_MINI_N — USB_B_N
UNUSED_USB_B_OC_L — USB_B_OC_L

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P — USB2_LT_P — USB_C_P
=USB2_LT_N — USB2_LT_N — USB_C_N
LTUSB_OC_L — USB_C_OC_L

USB Port "D" = Camera

=USB2_CAMERA_P — USB2_CAMERA_P — USB_D_P
=USB2_CAMERA_N — USB2_CAMERA_N — USB_D_N
UNUSED_USB_D_OC_L — USB_D_OC_L

USB Port "E" = ExpressCard

=USB2_EXCARD_P — USB2_EXCARD_P — USB_E_P
=USB2_EXCARD_N — USB2_EXCARD_N — USB_E_N
EXCARD_OC_L — USB_E_OC_L

USB Port "F" = Unused

TP_USBP_F — USB_F_P
TP_USBN_F — USB_F_N

USB Port "G" = Bluetooth (M13P)

=USB_BT_P — USB_BT_P — USB_G_P
=USB_BT_N — USB_BT_N — USB_G_N

USB Port "H" = Trackpad (Geyser)

=USB_TRACKPAD_P — USB_TRACKPAD_P — USB_H_P
=USB_TRACKPAD_N — USB_TRACKPAD_N — USB_H_N

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI2
=GND_CHASSIS_DVI3

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_DVI1
=GND_CHASSIS_DVI4
=GND_CHASSIS_ENET
=GND_CHASSIS_FW_EMI
=GND_CHASSIS_FW_PORT1
=GND_CHASSIS_RTUSB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_LCD1
=GND_CHASSIS_LCD2
=GND_CHASSIS_LCD3
=GND_CHASSIS_LCD4

SH0600
OG-503040
SHLD-SM-LF
GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
=GND_CHASSIS_INVERTER

Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	6	103

LEMENU

U0700
YONAH
CPU
BGA
(1 OF 4)

ADDR GROUP0
CONTROL
XDP/ITP SIGNALS
ADDR GROUP1
THERM
HCLK
RESERVED

FSB_A_L<3> J4 A3*
FSB_A_L<4> L4 A4*
FSB_A_L<5> M3 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M1 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L1 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> U2 ADSTB0*

FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L5 REQ4*

FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U2 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W3 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> W2 A30*
FSB_A_L<31> Y1 A31*
FSB_ADSTB_L<1> AB1 ADSTB1*

CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

TP_CPU_A32_L AA1 RSVD1
TP_CPU_A33_L AA4 RSVD2
TP_CPU_A34_L AB2 RSVD3
TP_CPU_A35_L AA3 RSVD4
TP_CPU_A36_L M4 RSVD5
TP_CPU_A37_L N5 RSVD6
TP_CPU_A38_L T2 RSVD7
TP_CPU_A39_L V3 RSVD8
TP_CPU_APM0_L R2 RSVD9
TP_CPU_APM1_L U3 RSVD10
TP_CPU_HFPLL B25 RSVD11

ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 FSB_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* B1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC A25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

RSVD12 T22 TP_CPU_EXTBREF
RSVD13 D2 TP_CPU_SPARE0
RSVD14 F6 TP_CPU_SPARE1
RSVD15 D3 TP_CPU_SPARE2
RSVD16 C1 TP_CPU_SPARE3
RSVD17 AF1 TP_CPU_SPARE4
RSVD18 D22 TP_CPU_SPARE5
RSVD19 C23 TP_CPU_SPARE6
RSVD20 C24 TP_CPU_SPARE7

SPARE[7-0],HFPLL:
ROUTE TO TP VIA AND
PLACE GND VIA W/IN 1000 MILS

=PP1V05_S0_CPU

R0702 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY

R0703 54.9 1% 1/16W MF-LF 402 NOSTUFF
R0704 68 5% 1/16W MF-LF 402
CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT

PM_THRMTRIP# SHOULD CONNECT TO ICH7-M AND GMCH WITHOUT T-ING (NO STUB)

R0705 1K 1% 1/16W MF-LF 402
R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH

CPU_GTLREF
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

R0712 54.9 5% 1/16W MF-LF 402 NOSTUFF
R0730 0 402 NOSTUFF
R0707 1K 5% 1/16W MF-LF 402

R0720 54.9 1% 402 XDP_TMS
R0721 54.9 1% 402 XDP_TDI
R0722 54.9 1% 402 XDP_TCK

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

LEMENU

U0700
YONAH
CPU
BGA
(2 OF 4)

DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC

FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> H22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H26 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H25 D15*
FSB_DSTBN_L<0> M26 DSTBN0*
FSB_DSTBP_L<0> M22 DSTBP0*
FSB_DINV_L<0> G26 DINV0*

FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L25 D20*
FSB_D_L<21> L22 D21*
FSB_D_L<22> L23 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P22 D25*
FSB_D_L<26> P23 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L26 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N24 D31*
FSB_DSTBN_L<1> M24 DSTBN1*
FSB_DSTBP_L<1> N25 DSTBP1*
FSB_DINV_L<1> G22 DINV1*

AD26 GTLREF

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 U1 CPU_COMP<2>
COMP3 V1 CPU_COMP<3>

DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_SLPCPU_L
PSI* AE6 CPU_PSI_L

D32* AA23 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* W25 FSB_D_L<36>
D37* U23 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U22 FSB_D_L<39>
D40* AB25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* AA26 FSB_D_L<43>
D44* Y26 FSB_D_L<44>
D45* Y22 FSB_D_L<45>
D46* AC26 FSB_D_L<46>
D47* AA24 FSB_D_L<47>
DSTBN2* W24 FSB_DSTBN_L<2>
DSTBP2* Y25 FSB_DSTBP_L<2>
DINV2* V23 FSB_DINV_L<2>

D48* AC22 FSB_D_L<48>
D49* AC23 FSB_D_L<49>
D50* AB22 FSB_D_L<50>
D51* AA21 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC25 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AD24 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AE25 FSB_D_L<60>
D61* AF25 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AF26 FSB_D_L<63>
DSTBN3* AD23 FSB_DSTBN_L<3>
DSTBP3* AE24 FSB_DSTBP_L<3>
DINV3* AC20 FSB_DINV_L<3>

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".

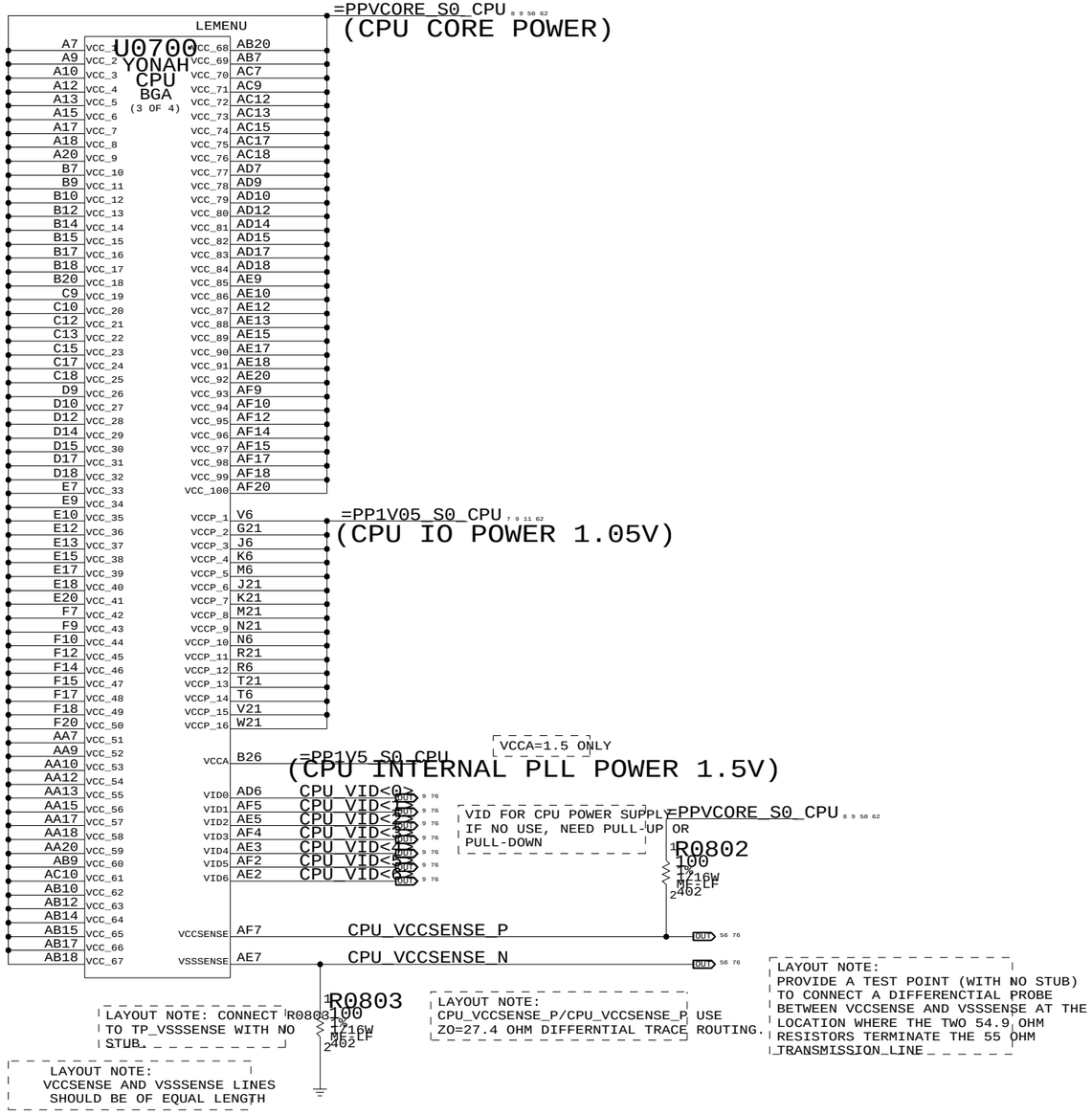
R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402

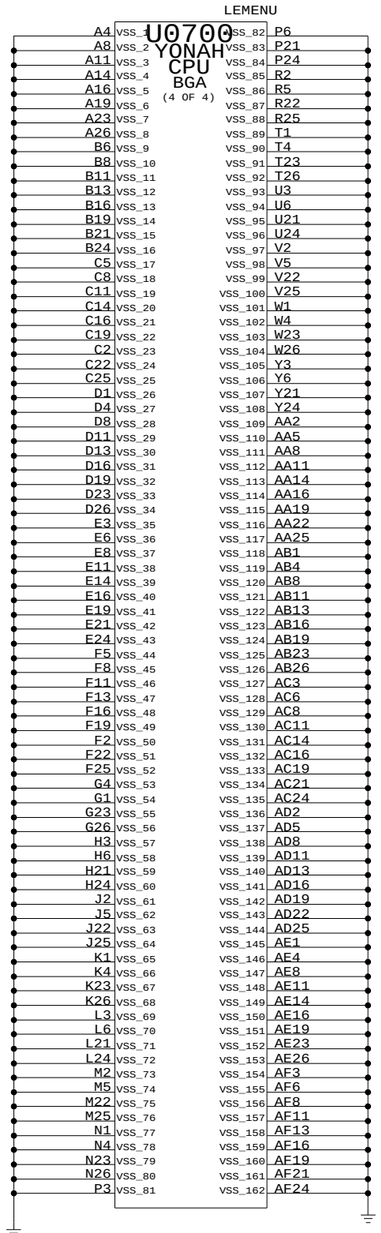
CPU 1 OF 2-FSB

SYNC_MASTER=M42 SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 7 OF 103	





CPU 2 OF 2-PWR/GND

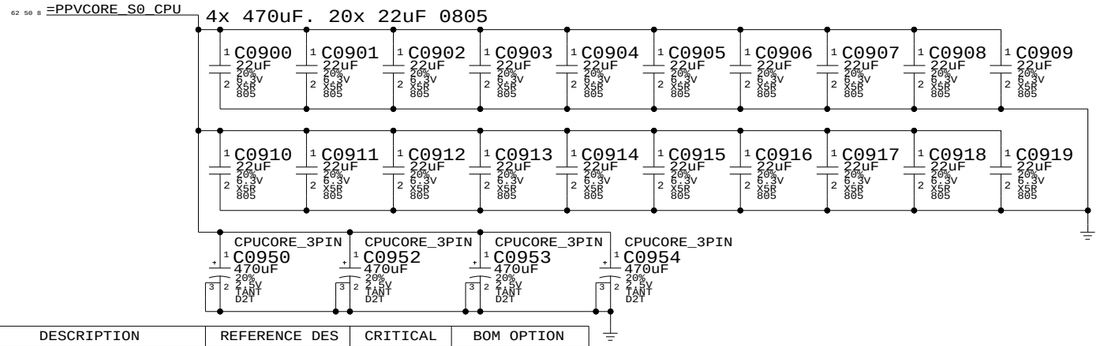
SYNC_MASTER=M42 SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	8	103

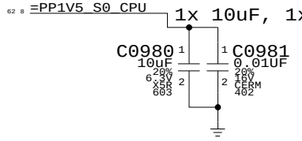
CPU VCORE HF AND BULK DECOUPLING



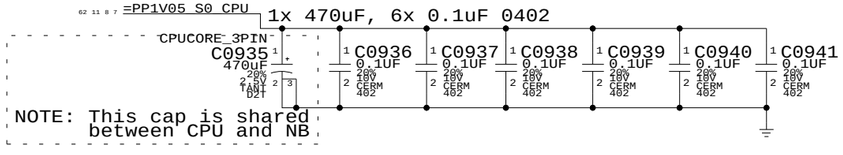
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	4	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C0950,C0952,C0953,C0954	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

VCCA (CPU AVdd) Decoupling



VCCP (CPU I/O) Decoupling

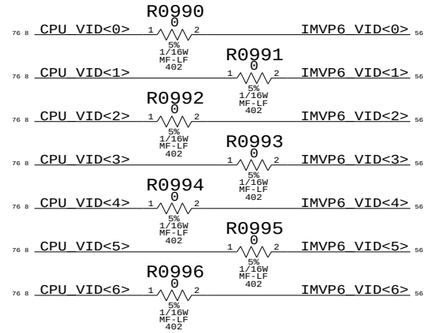


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	1	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C0935	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



CPU Decoupling & VID

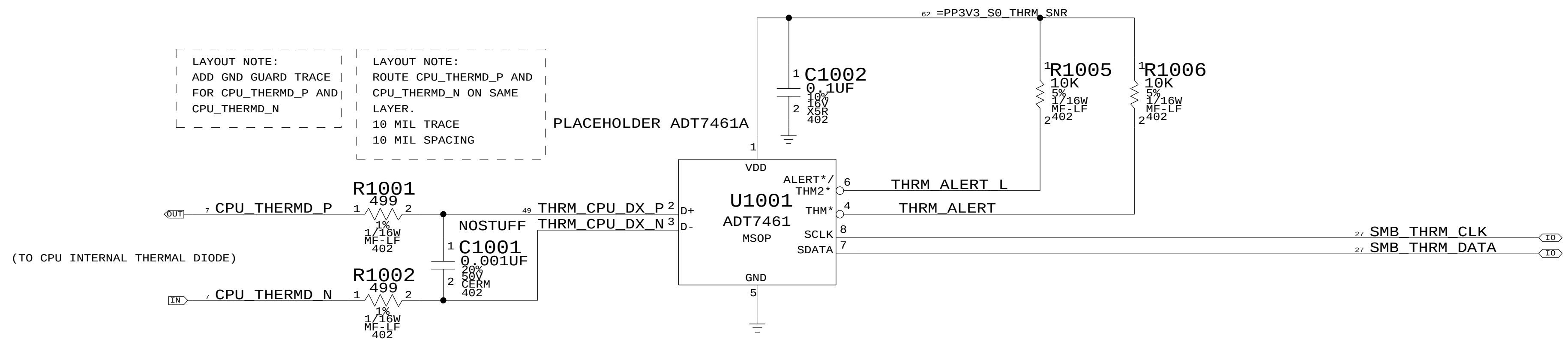
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	9	103

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE MCH

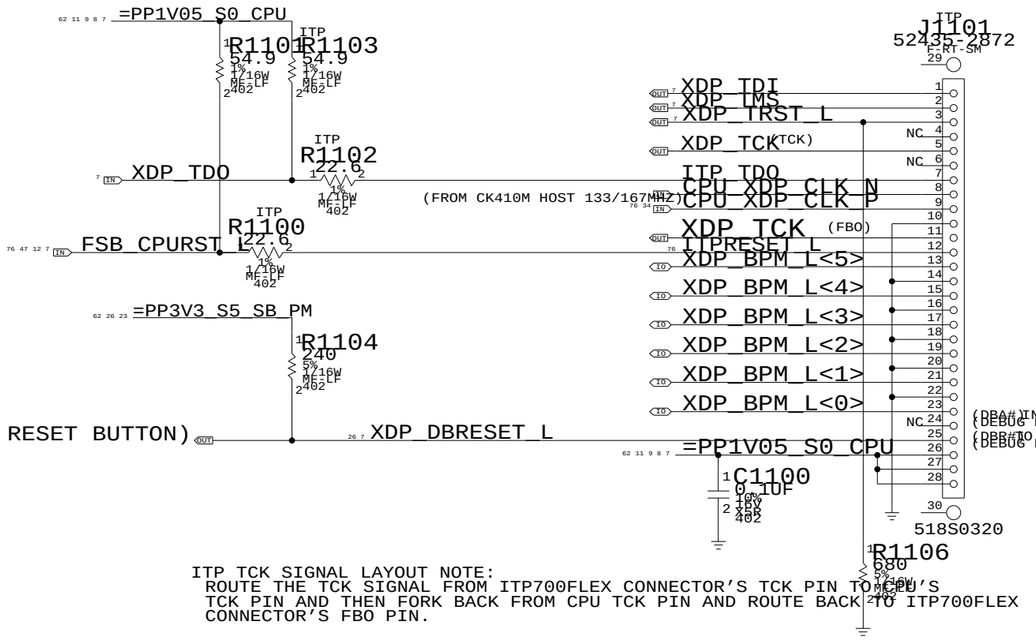
CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42 SYNC_DATE=08/04/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE NONE	SHT 10	OF 103

CPU ITP700FLEX DEBUG SUPPORT

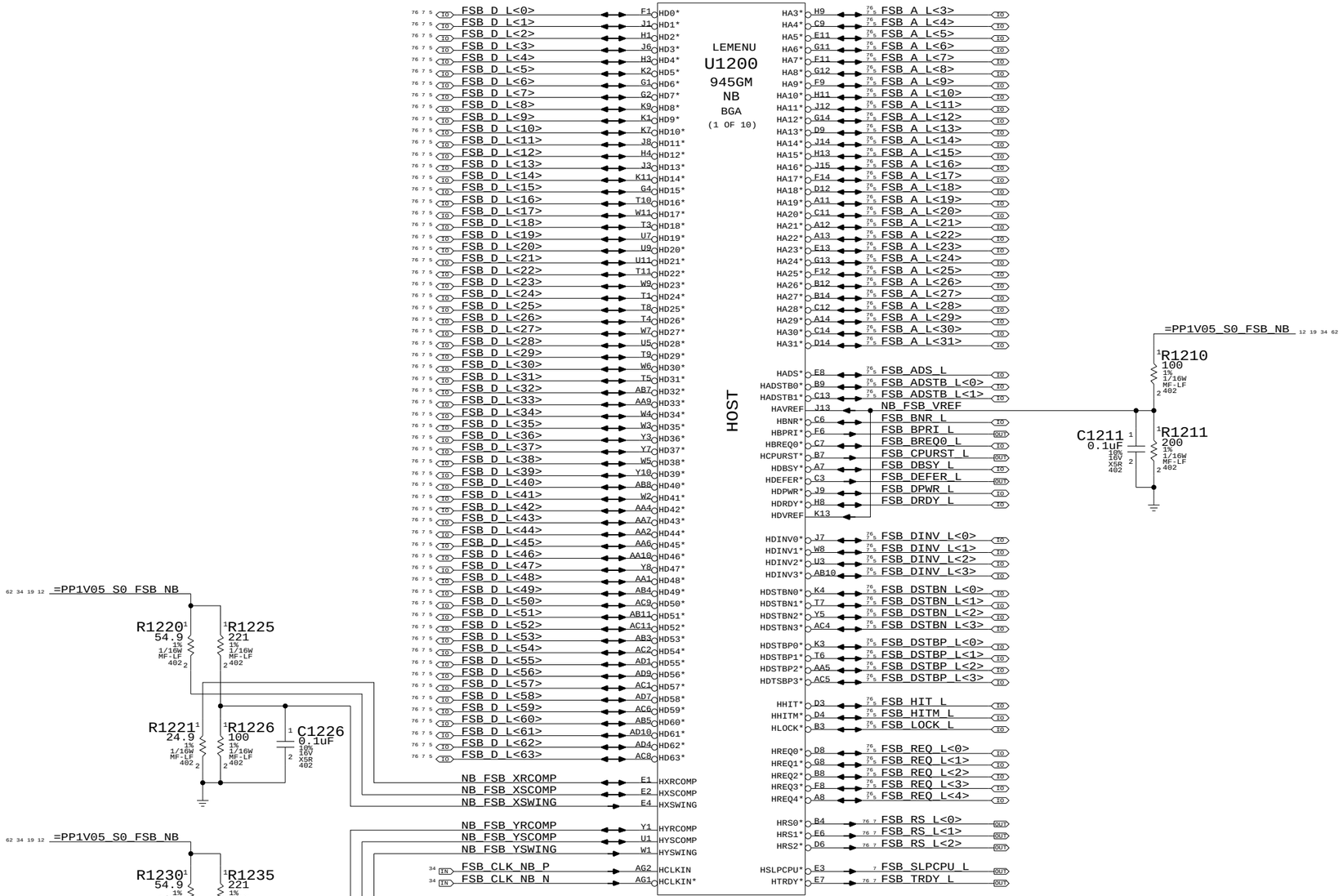


ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=07/26/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	03
	SCALE	SHT OF	
	NONE	11 103	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	12	103

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

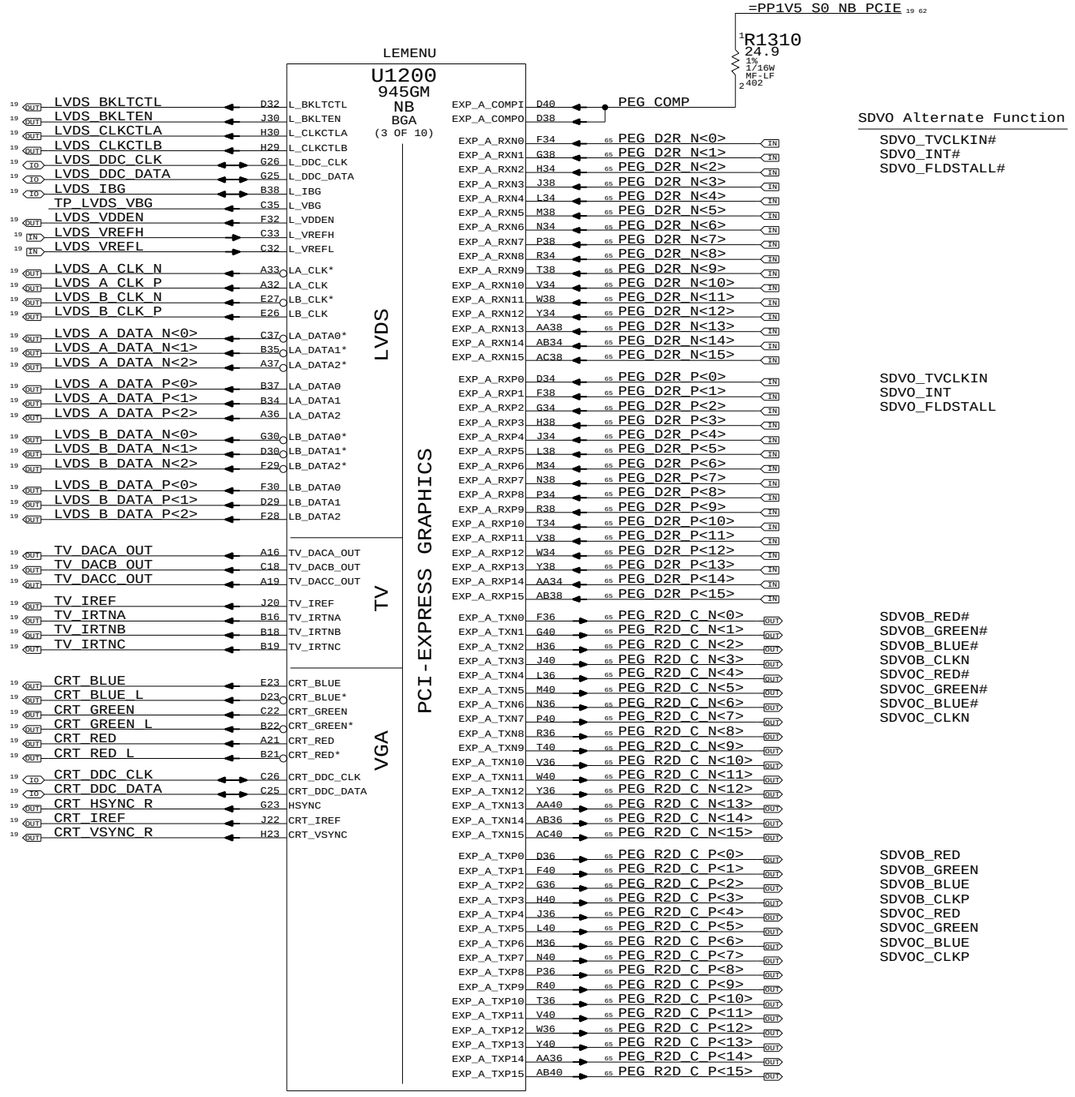
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

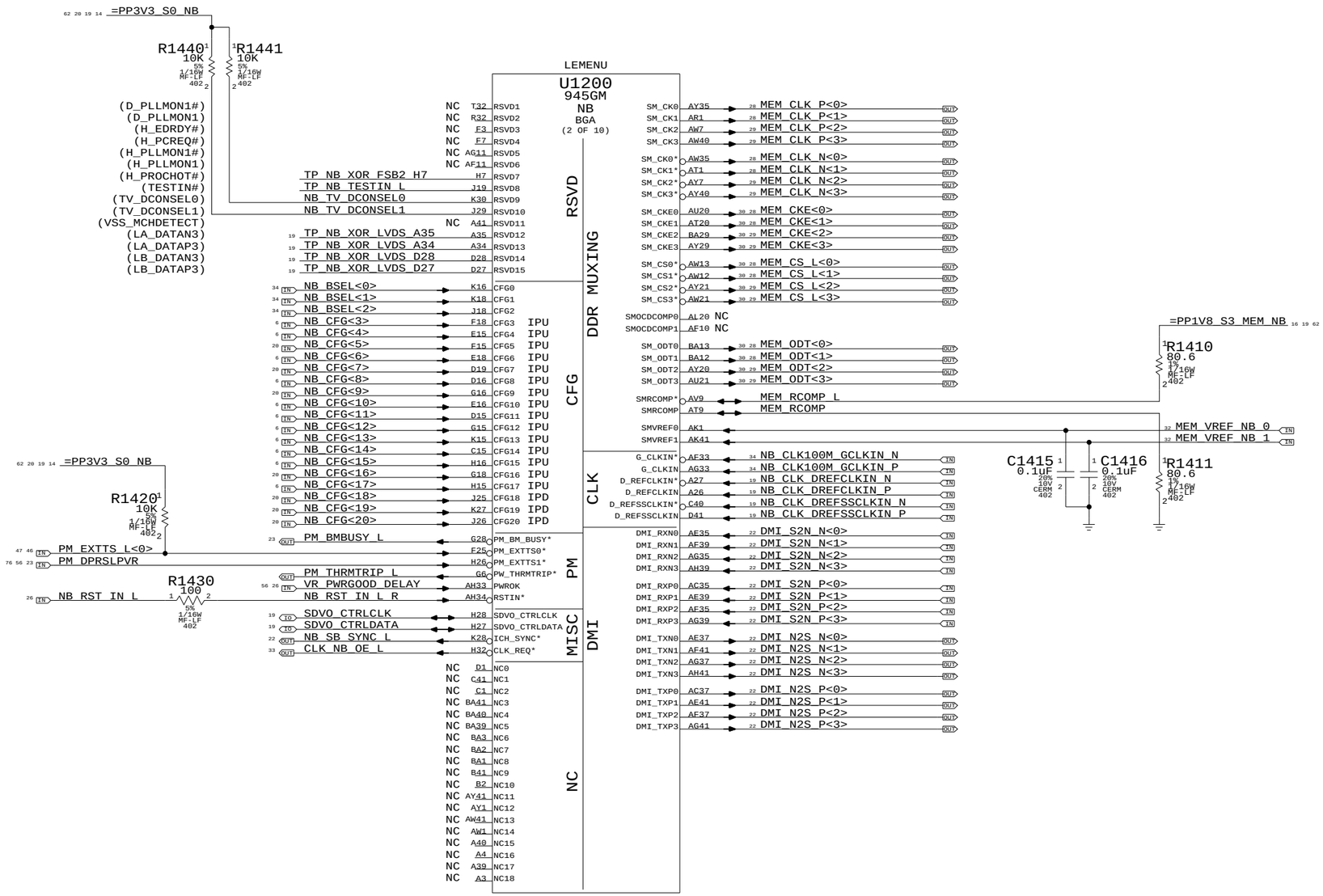
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	13	103



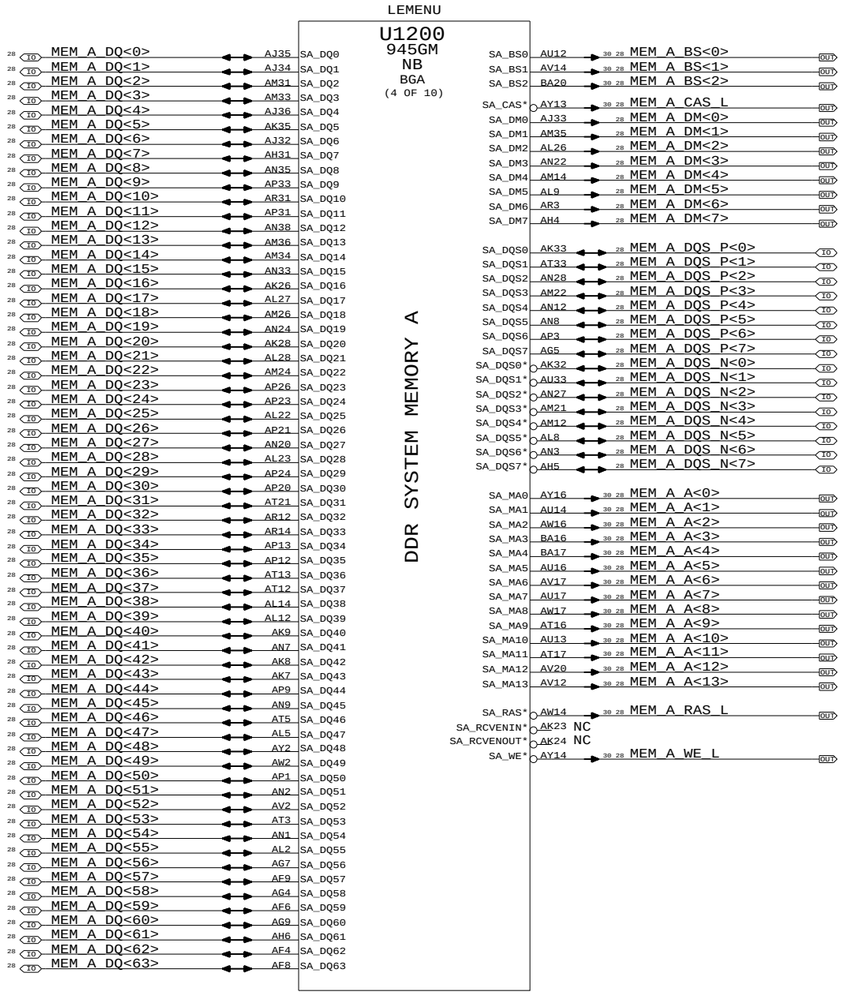
NB Misc Interfaces

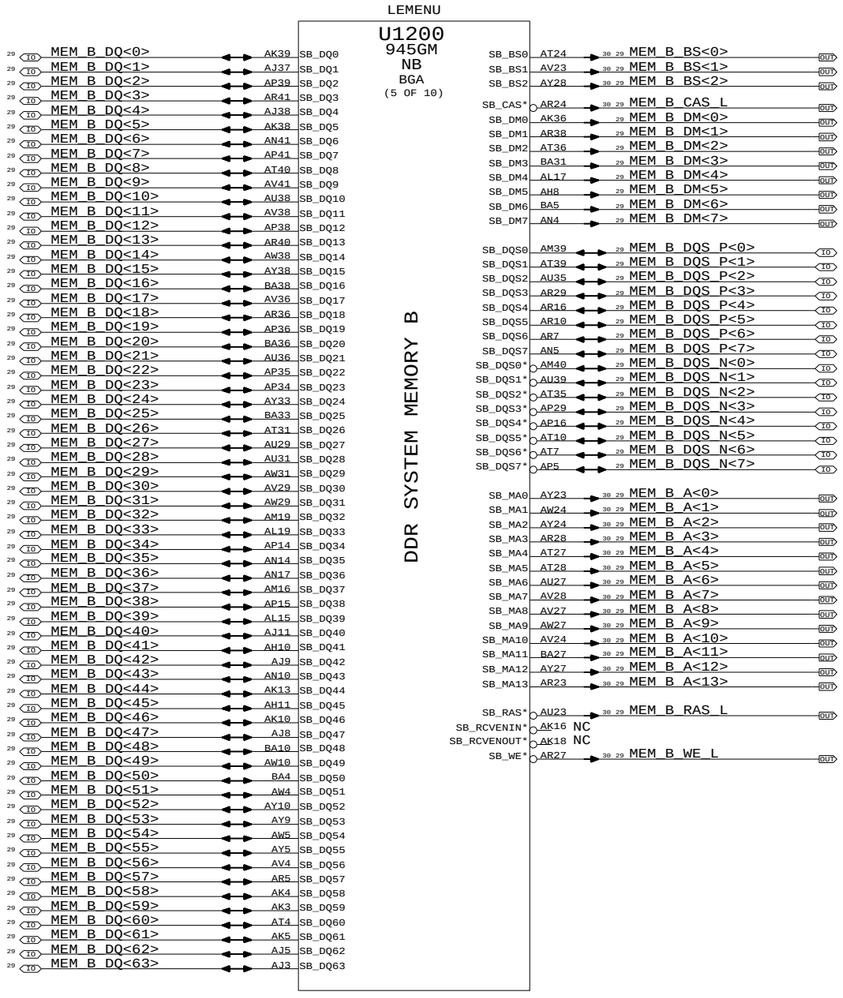
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	14	103





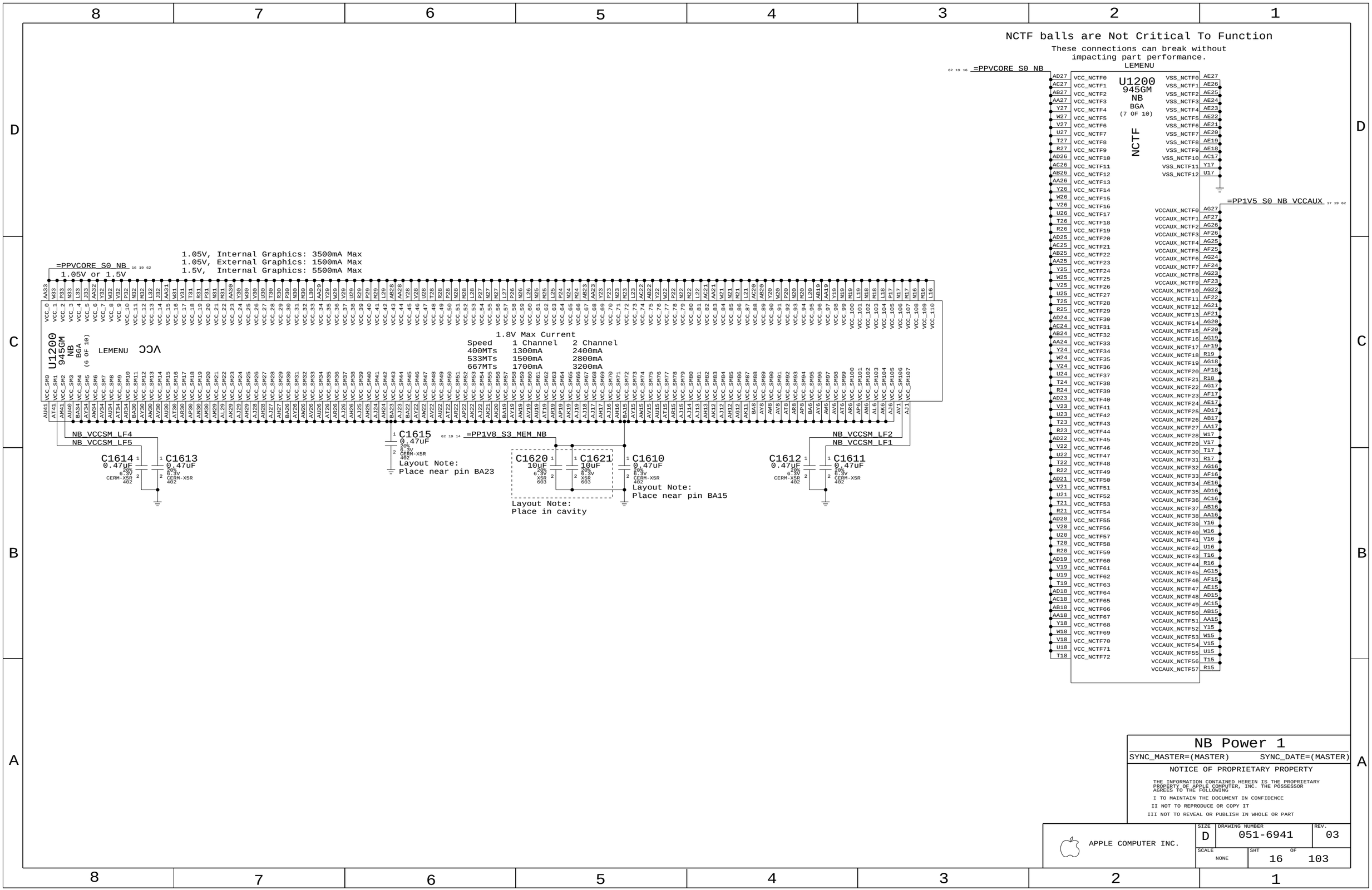
NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	15	103



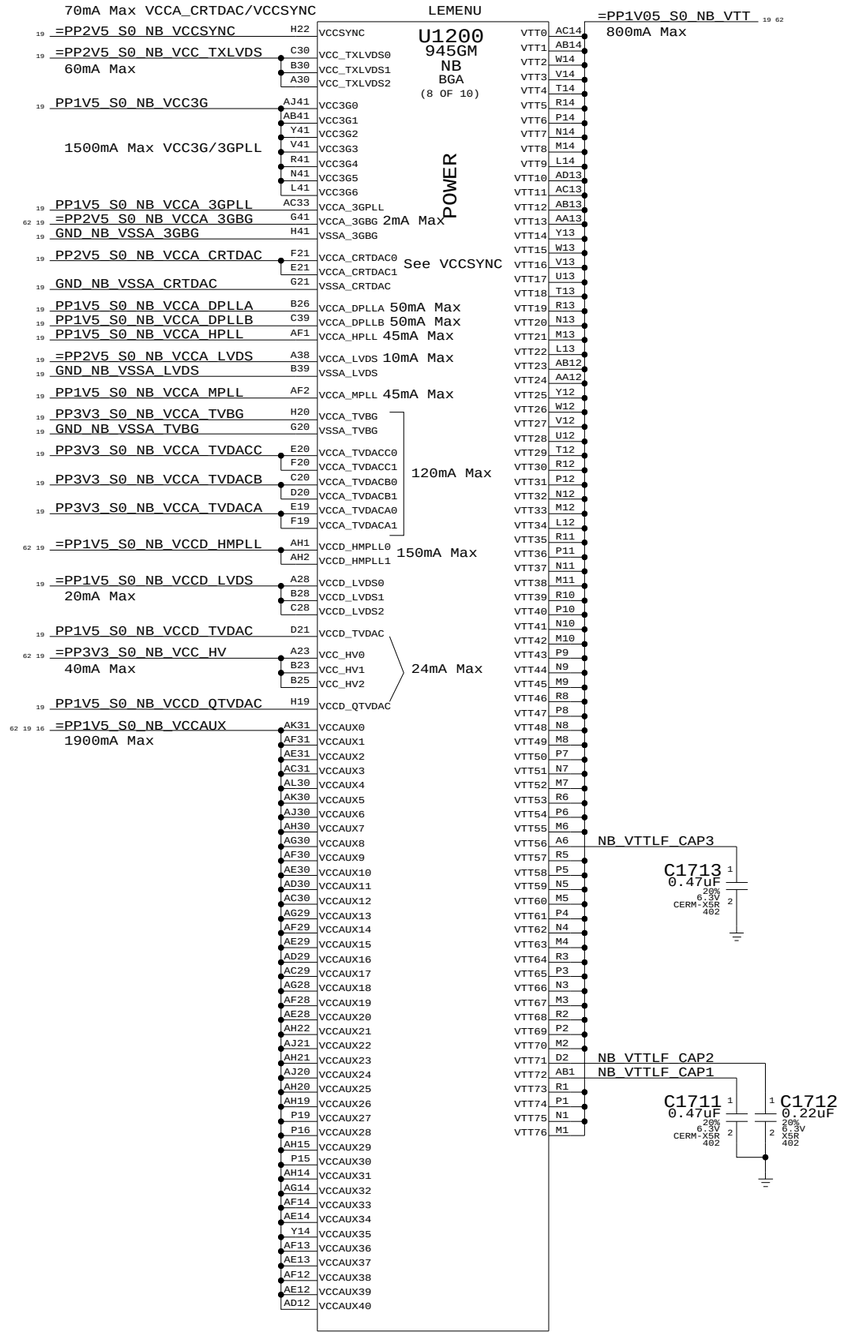
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	16	103



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	17	103

LEMENU

U1200
945GM
NB
BGA
(9 OF 10)

VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

LEMENU

U1200
945GM
NB
BGA
(10 OF 10)

VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	18	103

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16 19 62	1500mA Max
	=PP1V05_S0_FSB_NB	12 34 62	10mA Max?
	=PP1V05_S0_NB_VTT	17 19 62	800mA Max
	=PP1V05_S0_NB_CRT	19 62	?mA Max
3674mA Max	=PP1V5_S0_NB	62	?mA Max
	=PP1V5_S0_NB_3G	19 62	1500mA Max
	=PP1V5_S0_NB_3GPLL	19 62	
	=PP1V5_S0_NB_PCIE	13 62	?mA Max
	=PP1V5_S0_NB_PLL	19 62	100mA Max
	=PP1V5_S0_NB_TVDAC	19 62	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17 62	150mA Max
	=PP1V5_S0_NB_VCCAUX	16 17 19 62	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14 16 62	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	17 19	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	17 19	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17 19 62	2mA Max
	=PP3V3_S0_NB	14 20 62	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	17 19 62	40mA Max

=PP1V05_S0_NB_CRT (62 19)
- CRT_RED (13)
- CRT_GREEN (13)
- CRT_BLUE (13)
- CRT_RED_L (13)
- CRT_GREEN_L (13)
- CRT_BLUE_L (13)
- CRT_IREF (13)
- CRT_HSYNC_R (13)
- CRT_VSYNC_R (13)

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK (13)
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA (13)

=PP1V5_S0_NB_TVDAC (62 19)
- TV_DACA_OUT (13)
- TV_DACB_OUT (13)
- TV_DACC_OUT (13)
- TV_IREF (13)
- TV_IRTNA (13)
- TV_IRTNB (13)
- TV_IRTNC (13)

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL (13)
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN (13)
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA (13)
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB (13)
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK (13)
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA (13)
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG (13)
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN (13)
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH (13)
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL (13)
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P (13)
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N (13)
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> (13)
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> (13)
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P (13)
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N (13)
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> (13)
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> (13)
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 (14)
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 (14)
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 (14)
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 (14)
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK (14)
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA (14)

(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS (17 19)
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS (17)
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS (17)
NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS (17)

=PPVCORE_S0_NB (62 19 16)
- (MCH CRTDAC ANALOG 2.5V PWR) PP2V5_S0_NB_VCCA_CRTDAC (17)
- GND_NB_VSSA_CRTDAC (17)
- (MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC (17 19)

=PP1V5_S0_NB_TVDAC (62 19)
- (MCH TV OUT CHANNEL A 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACA (17)
- (MCH TV OUT CHANNEL B 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACB (17)
- (MCH TV OUT CHANNEL C 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACC (17)
- (MCH TV DAC BAND GAP 3.3V PWR) PP3V3_S0_NB_VCCA_TVBG (17)
- GND_NB_VSSA_TVBG (17)

(MCH DISPLAY A PLL 1.5V PWR) TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA (17)
(MCH DISPLAY B PLL 1.5V PWR) TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB (17)

- NB_CLK_DREFCLKIN_P (14)
- NB_CLK_DREFCLKIN_N (14)
- NB_CLK_DREFSSCLKIN_P (14)
- NB_CLK_DREFSSCLKIN_N (14)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0074	1	CAP,TANT,POLY,470UF,20%,2.5V,7MOHM,D2E	C1900	CRITICAL	CPUCORE_2PIN

Need to make sure we can do dual-footprint for 128S0068 & 128S0074!!!

=PPVCORE_S0_NB (62 19 16), 1500mA Max — GMCH CORE PWR 1.05V BYPASS
CPUCORE_3PIN
C1900 470UF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V X5R 402
C1905 0.22uF 20% 6.3V CERM 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

=PP1V05_S0_NB_VTT (62 19 17), 800mA Max — MCH VTT BYPASS (MCH FSB 1.05V PWR)
(SHARE C0940 470UF)
C1965 4.7uF 20% 6.3V CERM 603 — Layout Note: Place in cavity
C1966 2.2uF 20% 6.3V CERM1 603
C1967 0.22uF 20% 6.3V X5R 402 — Layout Note: Place on the edge

=PP3V3_S0_NB_VCC_HV (62 19 17), 40mA Max — MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG (62 19 17), 2mA Max — MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)
C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX (62 19 17 16), 1900mA Max — GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
C1918 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_TVDAC (62 19), 24mA Max
C1921 22000pF-1000mA 10V NPM18 — GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB_VCCD_TVDAC (17)
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
C1920 0.1uF 20% 10V CERM 402 — 24mA Max TVDAC/QTVDAC
Layout Note: These 4 caps should be within 6.35 mm of NB edge
L1922 180-OHM-1.5A 0603 — PP1V5_S0_NB_QTVDAC
C1923 22000pF-1000mA 10V NPM18 — GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB_VCCD_QTVDAC (17)
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
C1922 0.1uF 20% 10V CERM 402

1500mA Max

=PP1V5_S0_NB_3G (62 19), 1500mA Max
L1970 91nH 2010
C1970 220UF 20% 2.5V POLY SMB2 — Layout Note: Place L and C close to MCH
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603 — Layout Note: 10uF caps should be close to MCH on opposite side.
GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR) PP1V5_S0_NB_VCC3G (17)
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V

=PP1V5_S0_NB_3GPLL (62 19), 1.0UH-220MA-0.12-OHM 0805 — PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V
R1975 0.51 1% 1/10W ME-LF 402
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR) PP1V5_S0_NB_VCCA_3GPLL (17)
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V
GND_NB_VSSA_3GBG (17)
Layout Note: 3GPLL 10uF cap should be placed in cavity
Layout Note: Route to caps, then GND

1500mA Max

=PP1V5_S0_NB_PLL (62 19), 100mA Max
L1934 FERR-120-OHM-0.2A 0603
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402
GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR) PP1V5_S0_NB_VCCA_HPLL (17)
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
45mA Max
L1936 FERR-120-OHM-0.2A 0603
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402
GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR) PP1V5_S0_NB_VCCA_MPLL (17)
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
45mA Max

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 19 OF 103

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075
2.2K
5%
1/16W
MF-LF
2 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 62
NBCFG_VCC_1V5
1 R2058
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 62
NBCFG_DMI_REVERSE
1 R2059
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 62
NBCFG_SDVO_AND_PCIE
1 R2060
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

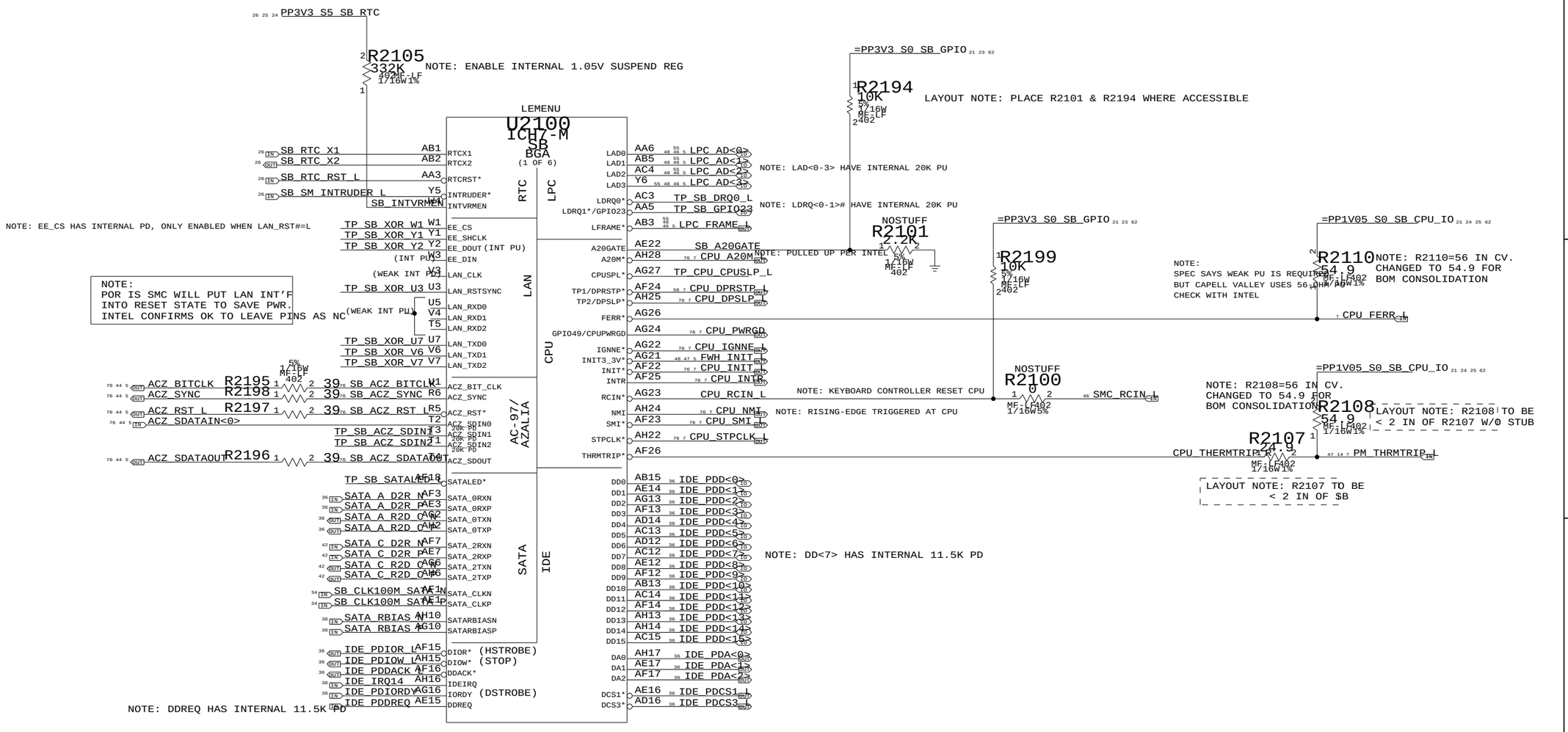
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 20 OF 103

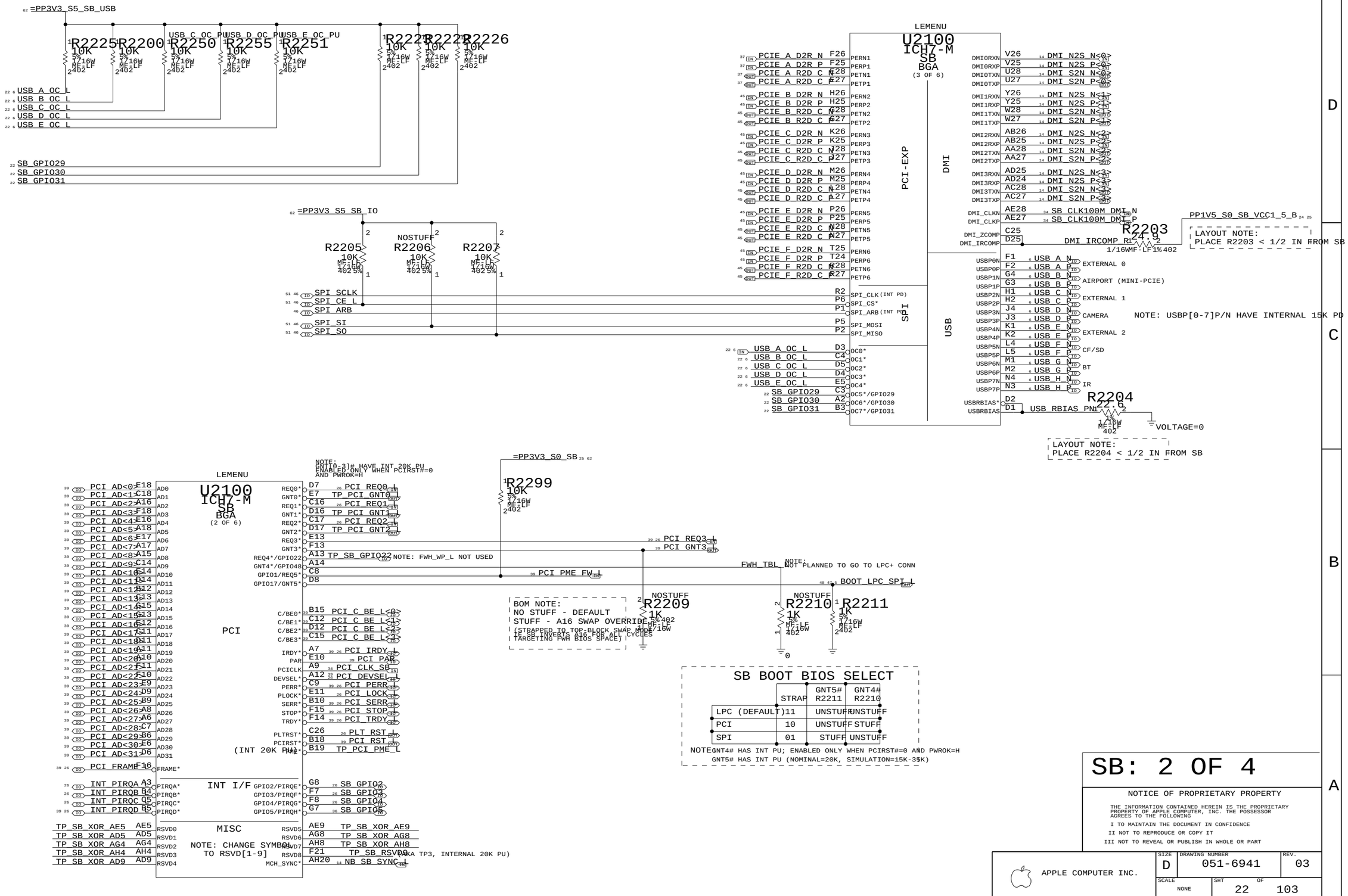


	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 21 OF 103	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2225 10K 5% 1/16W MF-LF 402
R2221 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K 1/16W 402 5%
NOSTUFF
R2206 10K 1/16W 402 5%
R2207 10K 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
LEMENU
U2100
ICH7-M
SB
BGA
(2 OF 6)
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
PCI
INT_PIRQA
INT_PIRQB
INT_PIRQC
INT_PIRQD
INT I/F
TP_SB_XOR_AE5
TP_SB_XOR_AD5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AD9
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
PCI_REQ0_L
TP_PCI_GNT0_L
PCI_REQ1_L
TP_PCI_GNT1_L
PCI_REQ2_L
TP_PCI_GNT2_L
PCI_REQ3_L
PCI_GNT3_L
TP_SB_GPIO22
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
(INT 20K PU)
SB_GPIO02
SB_GPIO03
SB_GPIO04
SB_GPIO06
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD8
(DNA TP3, INTERNAL 20K PU)
NB_SB_SYNC_L
=PP3V3_S0_SB
R2299 10K 5% 1/16W MF-LF 402
BOM NOTE:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
NOSTUFF
R2209 1K 5% 1/16W MF-LF 402
FWH_TBL_NOT
NOTE: NOT PLANNED TO GO TO LPC+ CONN
BOOT_LPC_SPI_L
NOSTUFF
R2210 1K 5% 1/16W MF-LF 402
R2211 1K 5% 1/16W MF-LF 402
0
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
LEMENU
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
PCI-EXP
SPI_CLK (INT PD)
SPI_CS*
SPI_ARB (INT PU)
SPI_MOSI
SPI_MISO
SPI
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
DMI
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
DMI_CLKN
DMI_CLKP
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
USB_A_N
USB_A_P
USB_B_N
USB_B_P
USB_C_N
USB_C_P
USB_D_N
USB_D_P
USB_E_N
USB_E_P
USB_F_N
USB_F_P
USB_G_N
USB_G_P
USB_H_N
USB_H_P
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
R2204 22.6 1/16W MF-LF 1% 402
USB_RBIAS_PN
VOLTAGE=0
LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB
SB: 2 OF 4
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 03
SCALE NONE
SHT 22 OF 103

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 62

=PP3V3_S5_SB 23 25 62

NO_REBOOT_MODE

R2318 10K 1/16W 2402 MF-LF 5%
R2395 8.2K 1/16W 2402 MF-LF 5%
R2396 10K 1/16W 2402 MF-LF 5%
R2397 8.2K 1/16W 2402 MF-LF 5%
R2327 10K 1/16W 2402 MF-LF 5%
R2326 10K 1/16W 2402 MF-LF 5%
R2323 1K 1/16W 2402 MF-LF 5%

NOSTUFF
RP2300 10K 5% 32 1/16W 5M-LF

=PP3V3_S5_SB 62 25 23

R2398 1K 1/16W 2402 MF-LF 5%
R2320 10K 1/16W 2402 MF-LF 5%
R2317 10K 1/16W 2402 MF-LF 5%
R2316 10K 1/16W 2402 MF-LF 5%

SMB_CLK 27 (IO) — C22 SMBCLK
SMB_DATA 27 (IO) — B22 SMBDATA
SMB_LINK_ALERT_L — A16 SMLINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L 55 48 46 5 (OUT) — A27 SUS_STAT*
PM_SYSRST_L 46 26 (IN) — A22 SYS_RST*
PM_BMBUSY_L 14 (IN) — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 (OUT) — AC20 GPIO18/STPPCI*
PM_STPCPU_L 33 (OUT) — AF21 GPIO20/STPCPU*
SB_GPIO26 (IN) — A21 GPIO26
BIOS_REC 23 — B21 GPIO27
FWH_MFG_MODE 23 — E23 GPIO28
PM_CLKRUN_L 55 48 46 39 5 (IO) — AG18 GPIO32/CLKRUN*
TP_AZ_DOCK_EN — AC19 GPIO33/AZ_DOCK_EN*
RESERVED FOR MOBILE AZALIA DOCKING INTF — AZ_DOCK_RST — U2 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L 44 37 5 (IN) — F20 WAKE*
INT_SERIRQ 55 48 46 5 (IO) — AH21 SERIRQ
PM_THRM_L 46 (IN) — AF20 THRM*
VR_PWRGD_CK410 26 (IN) — AD22 VRMPWRGD
TP_SB_GPIO6 (IO) — AG21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
SB_EXTSMI_L — E21 GPIO8

NOSTUFF
R2300 0 1/16W 2402 MF-LF 5%
SMC_RUNTIME_SCI 46 (IN)
SMC_EXTSMI_L 46 (IN)
R2301 0 1/16W 2402 MF-LF 5%

LEMENU
U2100
ICH7-M SB
BGA
(4 OF 6)

SMB
CLKS
SYS GPIO
PWR MNGT
GPIO

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

SB_GPIO21 — R2302 100 1/16W 2402 MF-LF 5%
SB_GPIO18 — R2303 100 1/16W 2402 MF-LF 5%
R2305 100 1/16W 2402 MF-LF 5%
SATA_C_DET_L 36 (IN)

AF19
AH18
AH19
AE19

CLK14 — AC1 — 34 SB_CLK14P3M_TIMER (IN)
CLK48 — B2 — 34 SB_CLK48M_USBCTLR (IN)
SUSCLK — C20 — 8 SUS_CLK_SB (OUT)

SLP_S3* — B24 — 64 46 PM_SLP_S3_L (OUT)
SLP_S4* — D23 — 64 46 PM_SLP_S4_L (OUT)
SLP_S5* — F22 — 46 PM_SLP_S5_L (OUT)
PWROK — AA4 — 26 PM_SB_PWROK (IN)
GPIO16/DPRSLPVR — AC22 — 76 56 14 PM_DPRSLPVR (OUT)
NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
TP0/BATLOW* — C21 — PM_BATLOW_L (IN)
PWRBTN* — C23 — 46 PM_PWRBTN_L (IN)
(INT 20K PU)
LAN_RST* — C19 — 46 PM_LAN_ENABLE (IN)
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4 — PM_RSMRST_L (IN)

GPIO9 — E20 — 47 46 SMS_INT_L (IN)
GPIO10 — A20 — 46 SMC_SB_NMI (IN)
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L (OUT)
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 36 23 IDE_RESET_L (OUT)
GPIO15 — E22 — SV_SET_UP 5 23 48
GPIO24 — R3 — CRB_SV_DET 23
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 33 SB_CLK100M_SATA_OE_L (OUT)
GPIO38 — AD20 — TP_SB_GPIO38 (NO)
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L (OUT)

=PP3V3_S5_SB_PM 11 26 62

R2319 10K 1/16W 2402 MF-LF 5%
R2343 8.2K 1/16W 2402 MF-LF 5%

R2399 100K 1/16W 402 MF-LF 5%

SMC_WAKE_SCI_L 46 (IN)

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S0_SB_GPIO 62 23 21

R2306 NOSTUFF 10K 1/16W 2402 MF-LF 5%
R2308 10K 1/16W 2402 MF-LF 5%

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SV_SET_UP 5 23 48
CRB_SV_DET 23

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 2402 MF-LF 5%
R2309 0 1/16W 2402 MF-LF 5%

=PP3V3_S5_SB 62 25 23

R2313 10K 1/16W 2402 MF-LF 5%
R2310 10K 1/16W 2402 MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

R2314 NOSTUFF 0 1/16W 2402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 2402 MF-LF 5%

=PP3V3_S0_SB_GPIO 21 23 62

R2390 10K 5% 1/16W MF-LF 2402
R2389 10K 5% 1/16W MF-LF 2402
R2388 10K 5% 1/16W MF-LF 2402

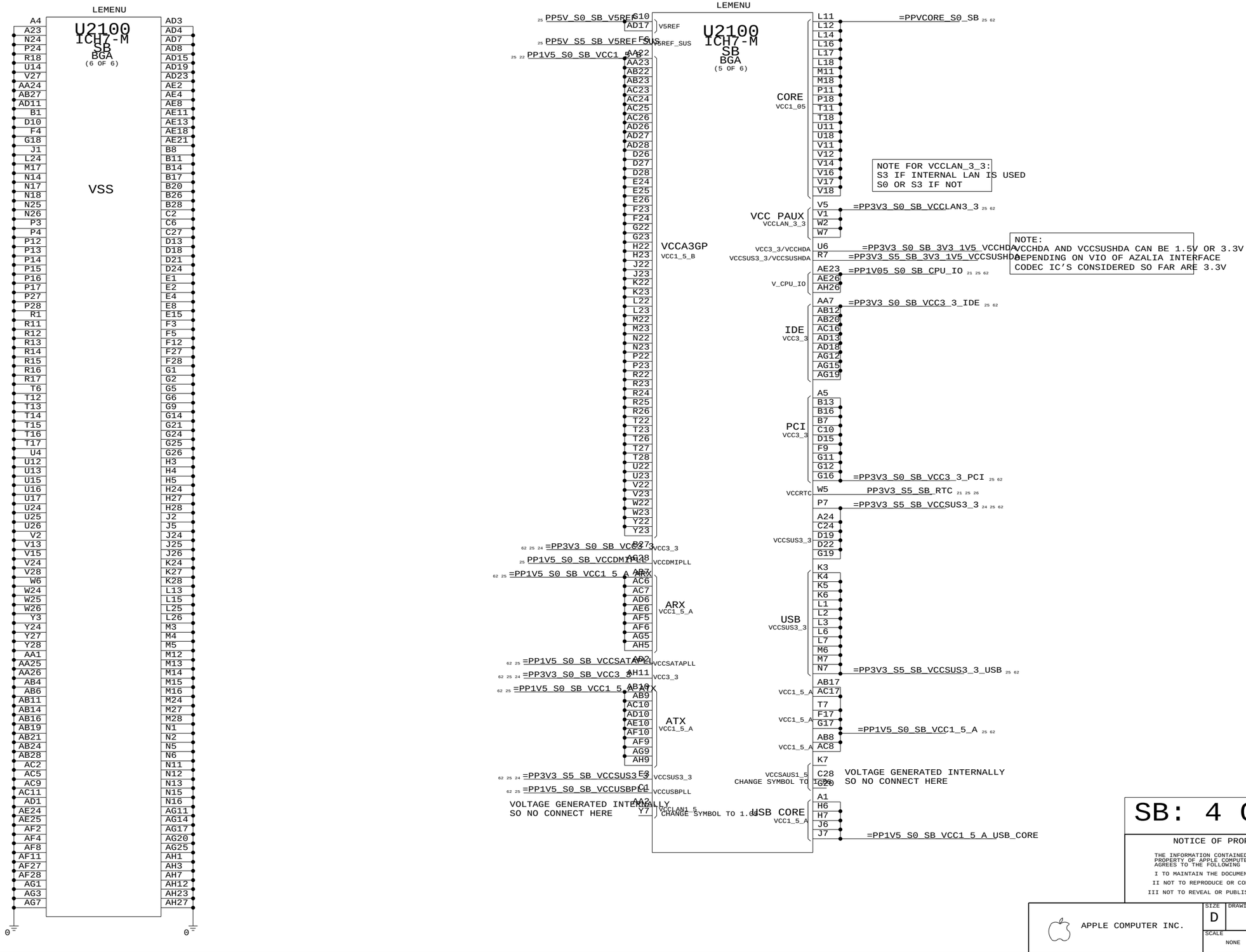
PATA_PWR_EN_L 23
IDE_RESET_L 36 23
SATA_C_PWR_EN_L 23

SB: 3 OF 4

APPLE COMPUTER INC.

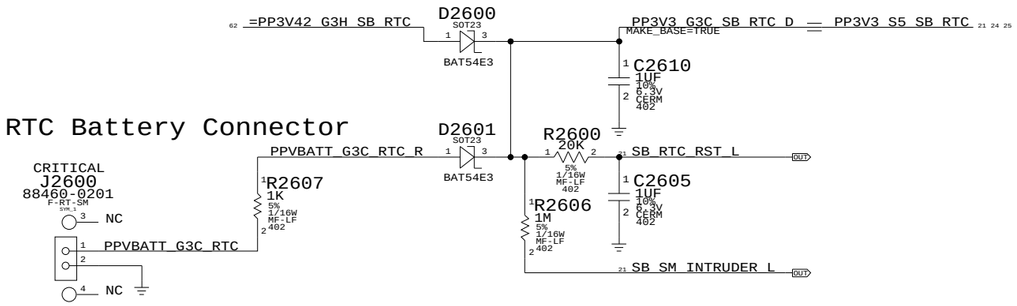
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	23	103

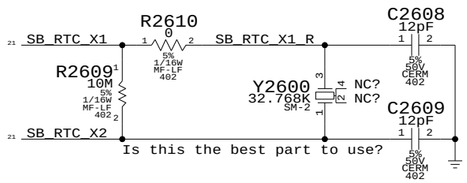

LEMENU
U2100
ICH7-M
SB
BGA
(6 OF 6)
VSS
LEMENU
U2100
ICH7-M
SB
BGA
(5 OF 6)
PP5V_S0_SB_V5REF
PP5V_S5_SB_V5REF_SUS
PP1V5_S0_SB_VCC1_5_A
V5REF
V5REF_SUS
VCCA3GP
VCC1_5_B
ARX
VCC1_5_A
ATX
VCC1_5_A
CORE
VCC1_05
VCC_PAUX
VCCLAN_3_3
IDE
VCC3_3
PCI
VCC3_3
USB
VCCSUS3_3
USB CORE
VCC1_5_A
=PPVCORE_S0_SB
=PP3V3_S0_SB_VCCLAN3_3
=PP3V3_S0_SB_3V3_1V5_VCCHDA
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
=PP1V05_S0_SB_CPU_IO
=PP3V3_S0_SB_VCC3_3_IDE
=PP3V3_S0_SB_VCC3_3_PCI
=PP3V3_S5_SB_RTC
=PP3V3_S5_SB_VCCSUS3_3
=PP3V3_S5_SB_VCCSUS3_3_USB
=PP1V5_S0_SB_VCC1_5_A
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
=PP3V3_S0_SB_VCC3_3
=PP1V5_S0_SB_VCCDMIPLL
=PP1V5_S0_SB_VCC1_5_A_ARX
=PP1V5_S0_SB_VCCSATAPLL
=PP3V3_S0_SB_VCC3_3
=PP1V5_S0_SB_VCC1_5_A_ATX
=PP3V3_S5_SB_VCCSUS3_3
=PP1V5_S0_SB_VCCUSBPLL
NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT
NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V
VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE
CHANGE SYMBOL TO 1.0u
VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE
SB: 4 OF 4
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 03
SCALE NONE
SHT 24 OF 103

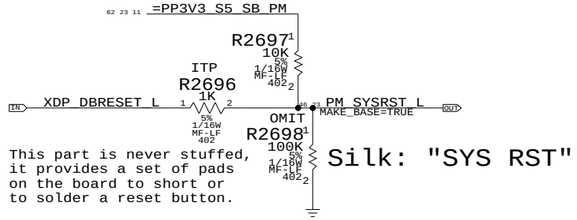

=PP3V3_S0_SB
=PP5V_S0_SB
R2502
100
1/10W
MF-LF
402
5%
D2501
SOT23
BAT54E3
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.15MM
PP5V_S0_SB_V5REF
C2503
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
=PP3V3_S5_SB
=PP5V_S5_SB
R2501
10
D2500
BAT54E3
PP5V_S5_SB_V5REF_SUS
C2504
0.1UF
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
=PP1V5_S0_SB
L2500
100-OHM-EMI
SM-3
155S0247
100-OHM,4A,0805
PP1V5_S0_SB_VCC1_5_B
C2500
220UF
20%
2.5V
SMB2
C2505
C2506
C2507
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
=PP3V3_S0_SB_VCC3_3
C2509
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
=PP1V5_S0_SB_VCC1_5_A_ARX
C2511
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
=PP1V5_S0_SB_VCCSATAPLL
C2517
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
=PP3V3_S0_SB_VCC3_3
C2513
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
=PP1V5_S0_SB_VCC1_5_A_ATX
C2514
1UF
20%
6.3V
CERM
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
=PP3V3_S5_SB_VCCSUS3_3
C2520
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
=PP1V5_S0_SB_VCCUSBPLL
C2515
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
=PPVCORE_S0_SB
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
C2518
C2502
330UF
20%
2.5V
POLY
CASE-C2
C2516
=PP3V3_S0_SB_VCCLAN3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V8,
V5, W2, OR W7
C2519
=PP3V3_S0_SB_3V3_1V5_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
C2521
=PP1V05_S0_SB_CPU_IO
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523
C2522
C2524
4.7UF
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
C2525
=PP3V3_S0_SB_VCC3_3_PCI
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526
C2527
C2528
=PP3V3_S5_SB_RTC
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530
C2529
=PP3V3_S5_SB_VCCSUS3_3
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531
C2534
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533
C2532
=PP1V5_S0_SB_VCC1_5_A
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1
C2512
=PP1V5_S0_SB
R2500
1/10W5%
MF-LF603
PP1V5_S0_SB_R
152S0315
1UH,0.5A,20%,1206
L2507
0.28-OHM
1206
PP1V5_S0_SB_VCCDMIPLL
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
C2501
0.01UF
C2508
10UF
6.3V
X6S
603
SB: 4 OF 4
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-6941
REV.
03
SCALE
NONE
SHT
25
OF
103

RTC Battery Connector



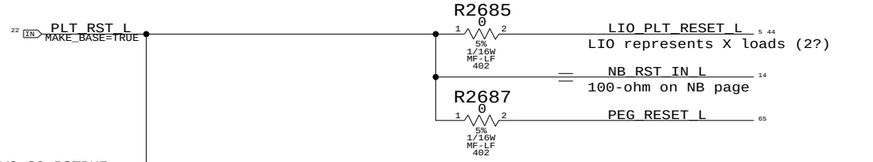
SB RTC Crystal Circuit



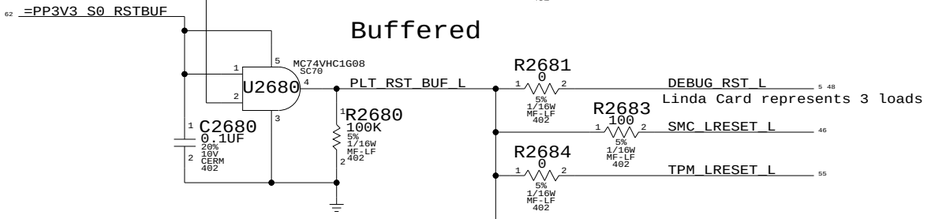


Platform Reset Connections

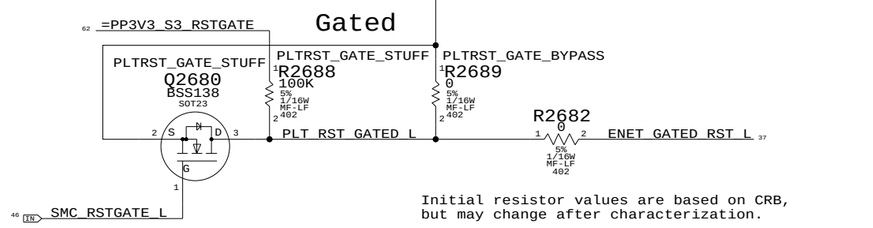
Unbuffered

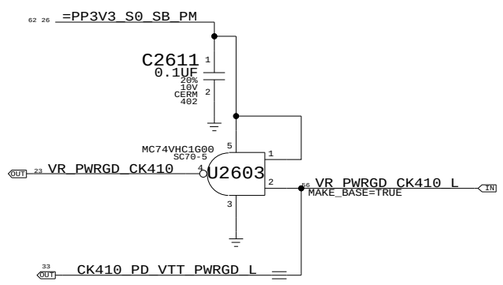


Buffered

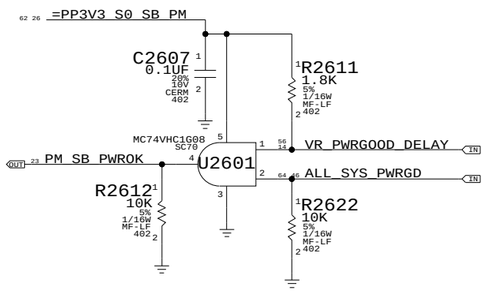


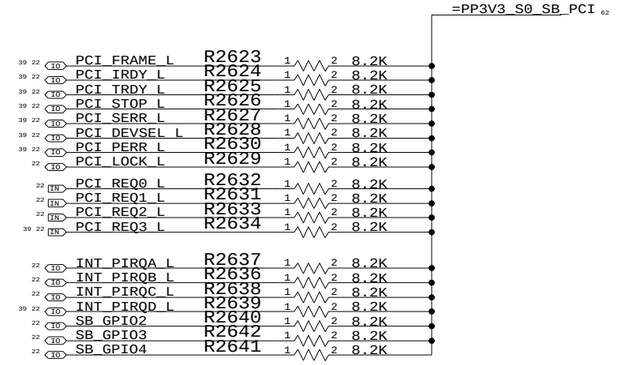
Gated





1G00 used as small & cheap inverter





SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE	SHT	OF
NONE	26	103

ICH7-M SMBus Connections

62 =PP3V3_S0_SMBUS_SB

ICH7-M
U2100
(MASTER)

23 SMB_CLK — SMBUS_SB_SCL (MAKE_BASE=TRUE)
23 SMB_DATA — SMBUS_SB_SDA (MAKE_BASE=TRUE)

R2700[1] 2.0K 5% 1/16W MF-LF 402[2]
R2701[1] 2.0K 5% 1/16W MF-LF 402[2]

Clock Chip
CY28445-5: U3301
(Write: 0xD2 Read: 0xD3)

SMB_CK410_CLK — 33
SMB_CK410_DATA — 33

SO-DIMM "A"
J2800
(Write: 0xA0 Read: 0xA1)

=I2C_SODIMMA_SCL — 28
=I2C_SODIMMA_SDA — 28

SO-DIMM "B"
J2900
(Write: 0xA4 Read: 0xA5)

=I2C_SODIMMB_SCL — 29
=I2C_SODIMMB_SDA — 29

Left I/O Board
J5500
(See Table)

=SMBUS_LIO_SB_SCL — 5 44
=SMBUS_LIO_SB_SDA — 5 44

Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections

62 =PP3V3_S0_SMBUS_SMC_0_S0

SMC
U5800
(MASTER)

46 SMB_0_S0_CLK — SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
46 SMB_0_S0_DATA — SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

R2750[1] 2.0K 5% 1/16W MF-LF 402[2]
R2751[1] 2.0K 5% 1/16W MF-LF 402[2]

Right-Side Temp
ADT7461: U6150
(Write: 0x98 Read: 0x99)

=SMBUS_RSTHMSNS_SCL — 49
=SMBUS_RSTHMSNS_SDA — 49

GPU Temp
MAX6695: U6100
(Write: 0x30 Read: 0x31)

=SMBUS_GPUTHMSNS_SCL — 49
=SMBUS_GPUTHMSNS_SDA — 49

Ambient Thermal
TMP105: J4930
(Write: 0x90 Read: 0x91)

=SMBUS_ATS_SCL — 42
=SMBUS_ATS_SDA — 42

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

62 =PP3V3_S3_SMBUS_SMC_A_S3

SMC
U5800
(MASTER)

46 SMB_A_S3_CLK — SMBUS_SMC_A_S3_SCL (MAKE_BASE=TRUE)
46 SMB_A_S3_DATA — SMBUS_SMC_A_S3_SDA (MAKE_BASE=TRUE)

R2770[1] 2.0K 5% 1/16W MF-LF 402[2]
R2771[1] 2.0K 5% 1/16W MF-LF 402[2]

Top-Case
J4900
(See Table)

=SMBUS_TOPCASE_SCL — 42
=SMBUS_TOPCASE_SDA — 42

Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

SMC "B" SMBus Connections

62 =PP3V3_S0_SMBUS_SMC_B_S0

SMC
U5800
(MASTER)

46 SMB_B_S0_CLK — SMBUS_SMC_B_S0_SCL (MAKE_BASE=TRUE)
46 SMB_B_S0_DATA — SMBUS_SMC_B_S0_SDA (MAKE_BASE=TRUE)

R2760[1] 2.0K 5% 1/16W MF-LF 402[2]
R2761[1] 2.0K 5% 1/16W MF-LF 402[2]

CPU Temp
ADT7461: U1001
(Write: 0x98 Read: 0x99)

SMB_THRM_CLK — 10
SMB_THRM_DATA — 10

Left I/O Board
J5400
(See Table)

=SMBUS_LIO_SMC_SCL — 5 44
=SMBUS_LIO_SMC_SDA — 5 44

Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections

62 =PP3V42_G3H_SMBUS_SMC_BSA

SMC
U5800
(MASTER)

SMB_BSA_CLK — SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
46 SMB_BSA_DATA — SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

R2780[1] 2.0K 5% 1/16W MF-LF 402[2]
R2781[1] 2.0K 5% 1/16W MF-LF 402[2]

Battery
J8250
(Write: 0x?? Read: 0x??)

=SMBUS_BATT_SCL — 5 63
=SMBUS_BATT_SDA — 5 63

SMC "Battery B" SMBus Connections

62 =PP3V3_S0_SMBUS_SMC_BSB

SMC
U5800
(MASTER)

46 SMB_BSB_CLK — SMBUS_SMC_BSB_SCL (MAKE_BASE=TRUE)
46 SMB_BSB_DATA — SMBUS_SMC_BSB_SDA (MAKE_BASE=TRUE)

R2790[1] 100K 5% 1/16W MF-LF 402[2]
R2791[1] 100K 5% 1/16W MF-LF 402[2]

M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 27 OF 103

Page Notes

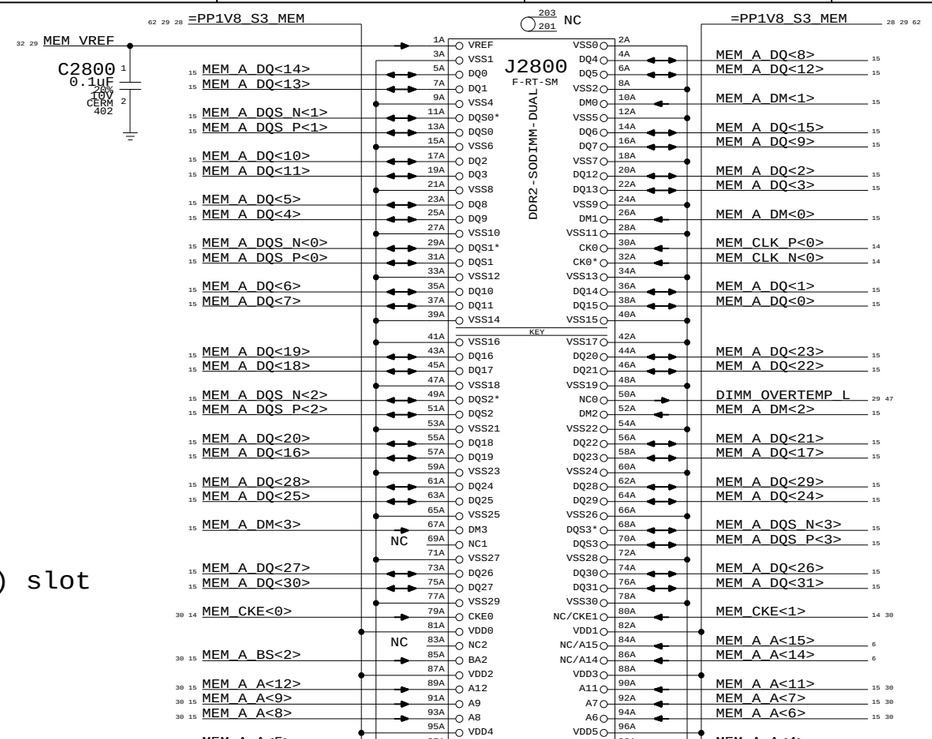
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

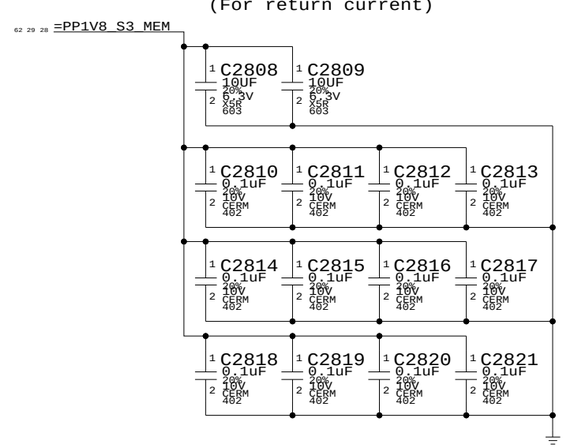
NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (surface-mount) slot



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 28 OF 103	

Page Notes

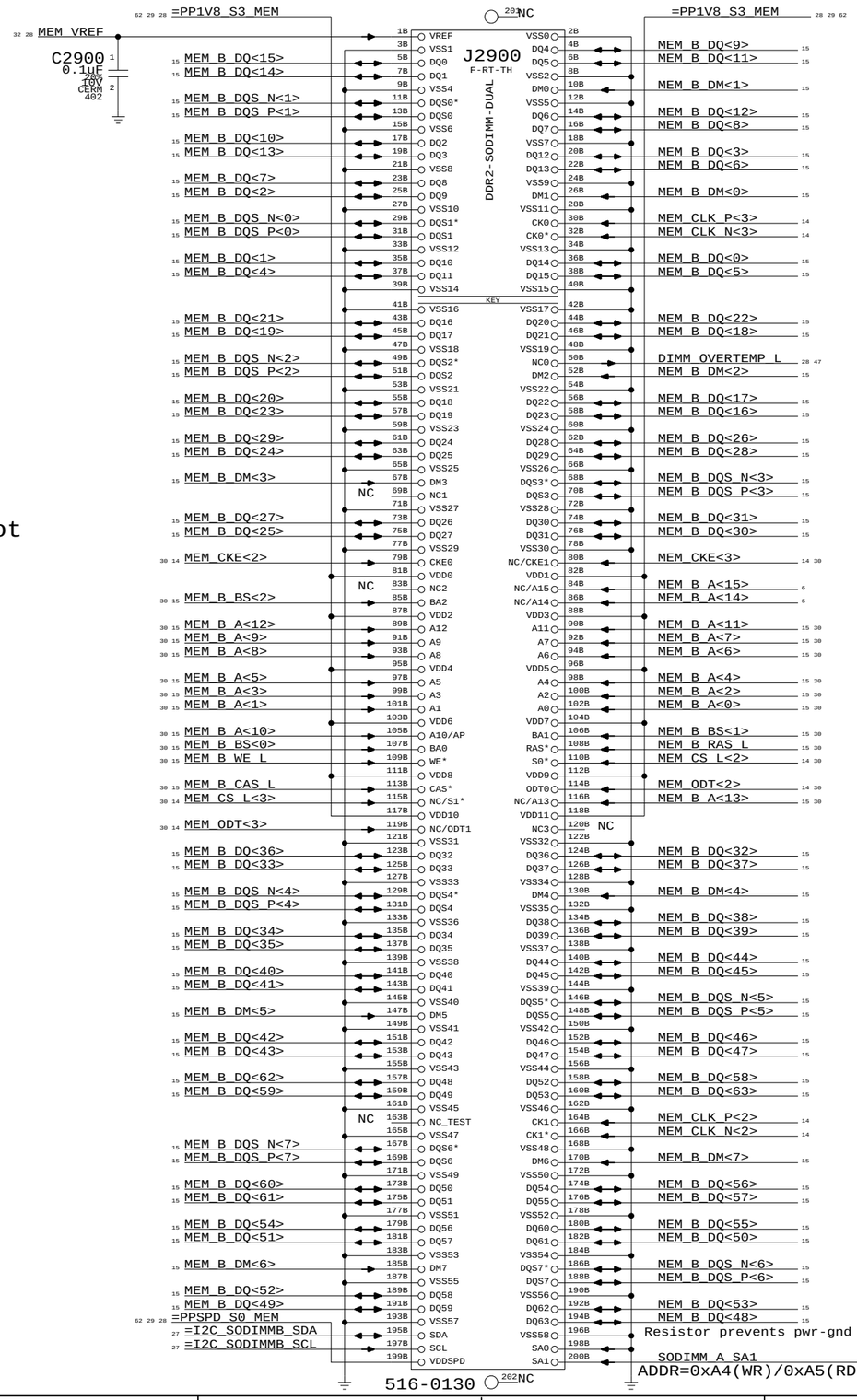
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

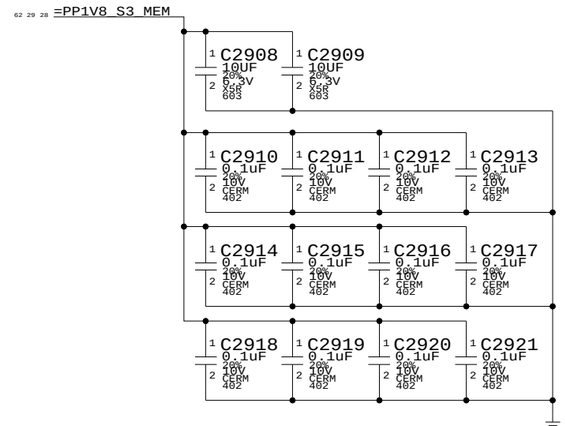
NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (thru-hole) slot



DDR2 Bypass Caps

(For return current)



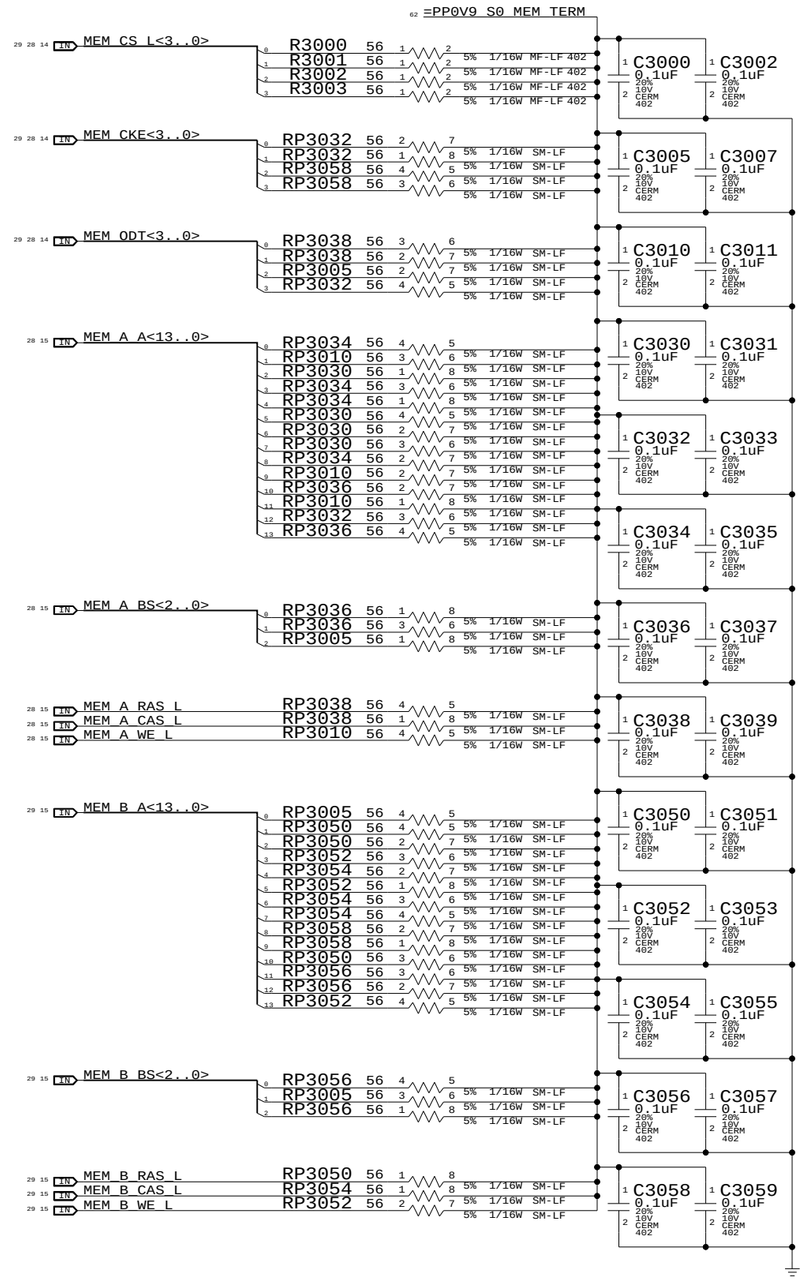
DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 29	OF 103

One cap for each side of every RPAK, one cap for every two discrete resistors



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	30	103

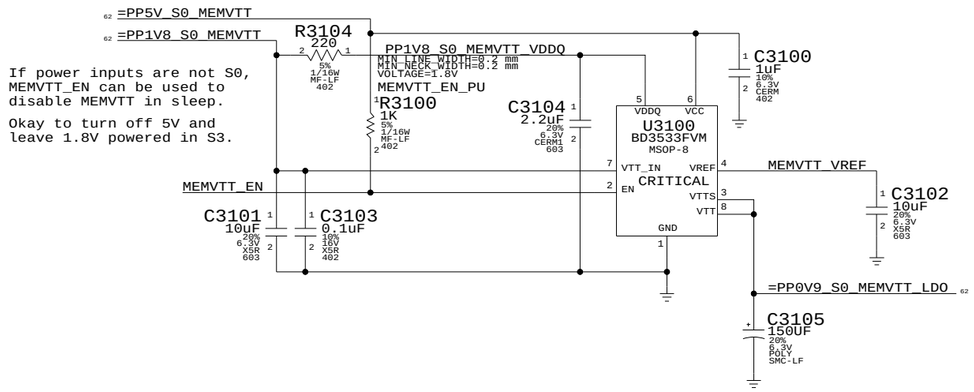
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



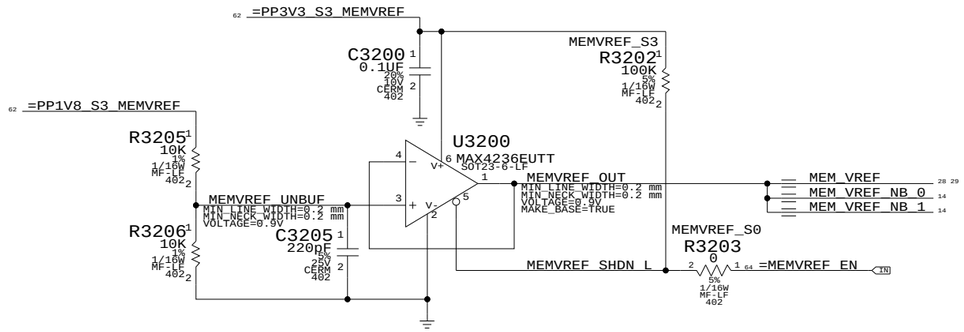
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	31	103



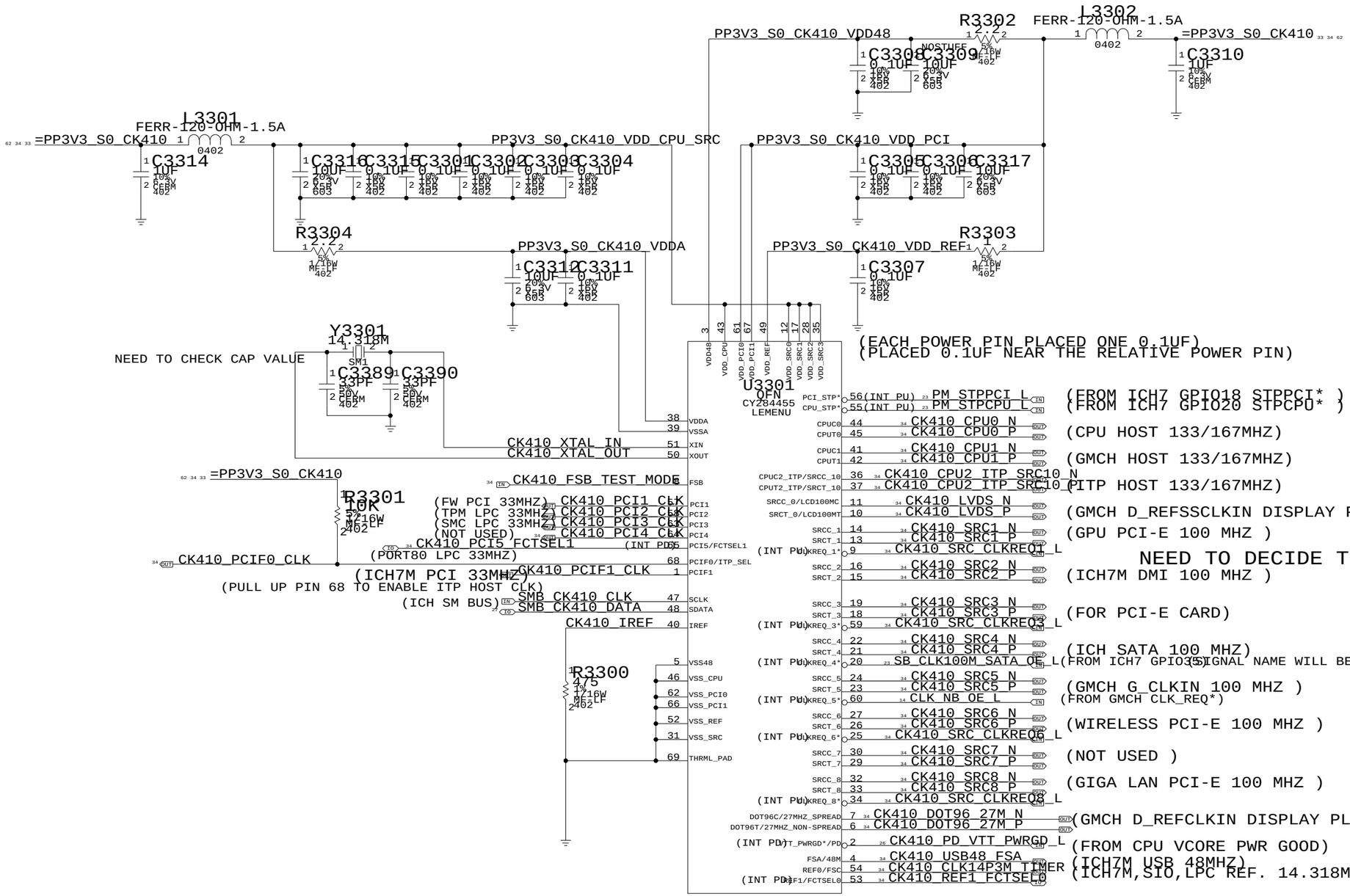
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	32	103



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	BD	SRCT0	SRCC0	

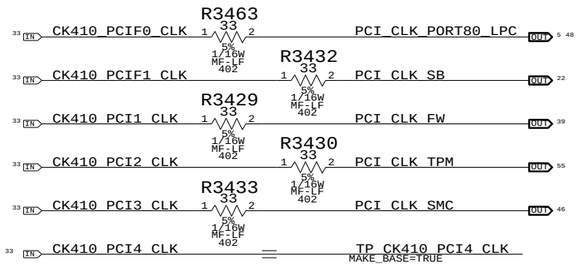
CLOCKS

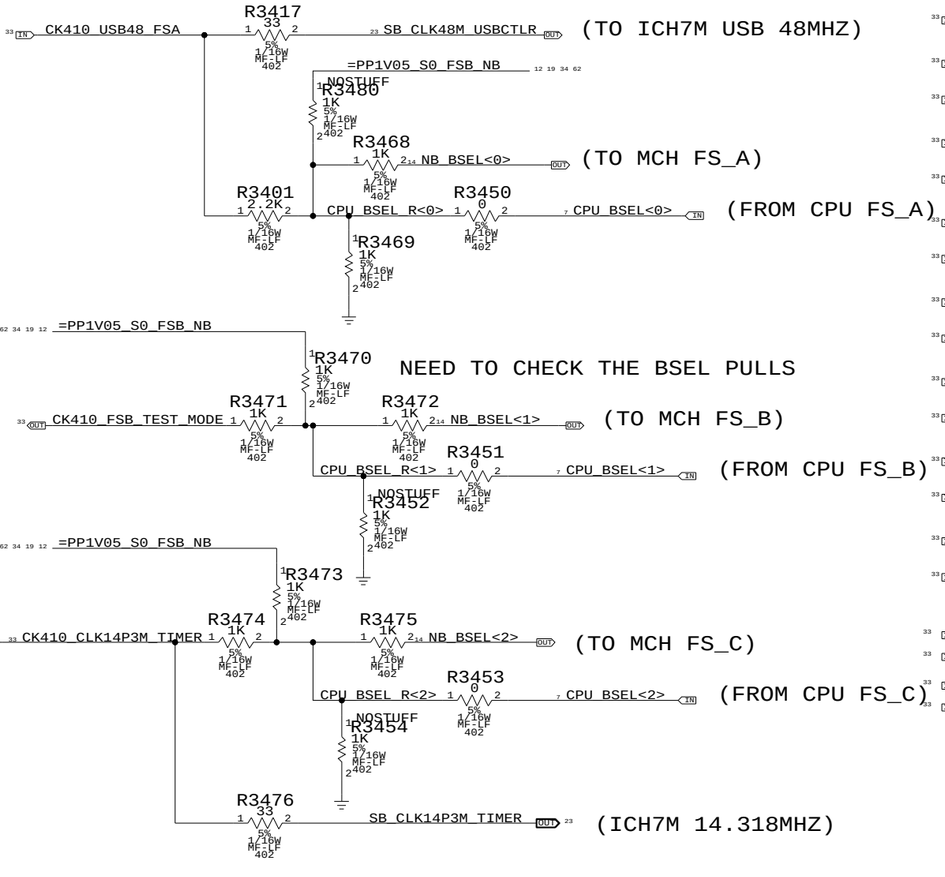
SYNC_MASTER=MBZ SYNC_DATE=08/04/2005

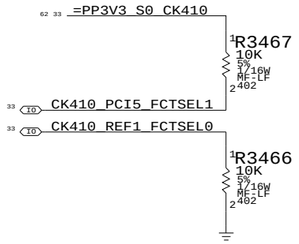
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	33	103



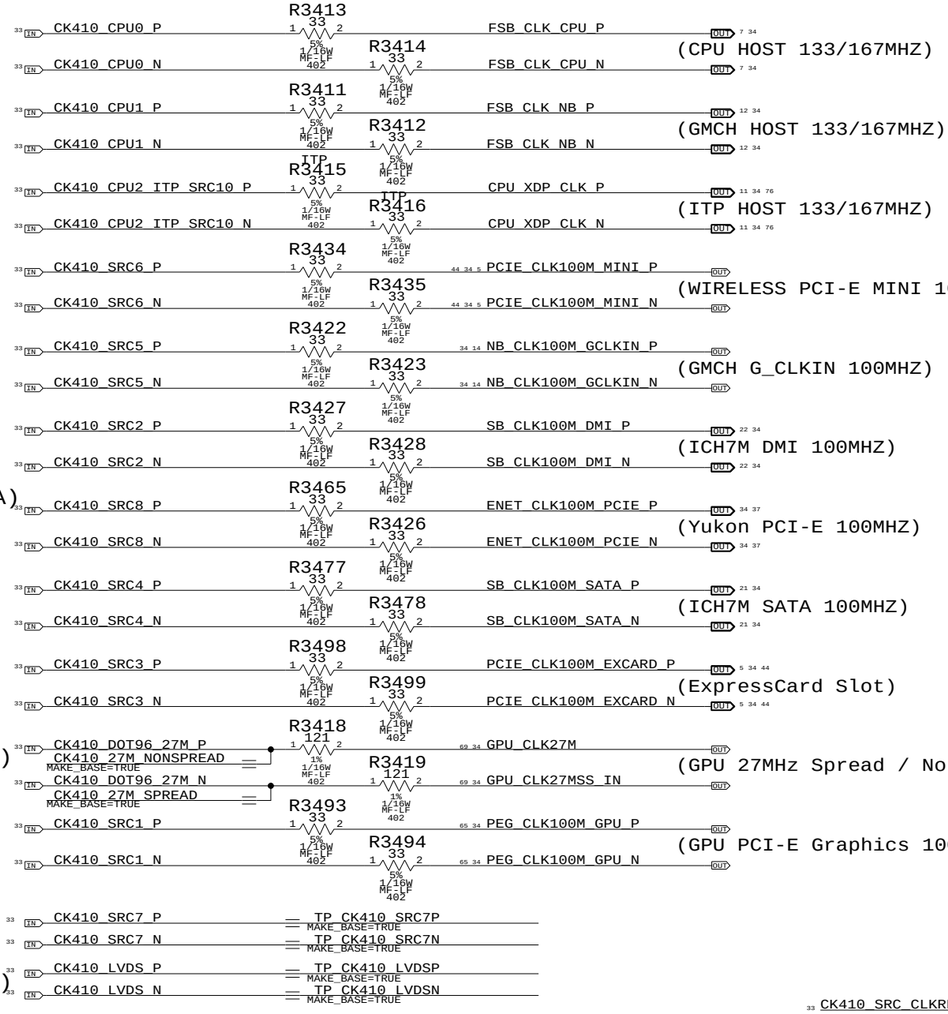


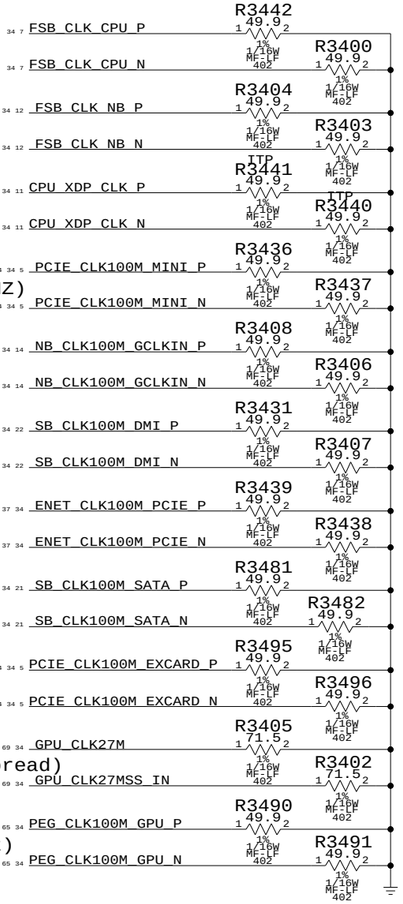


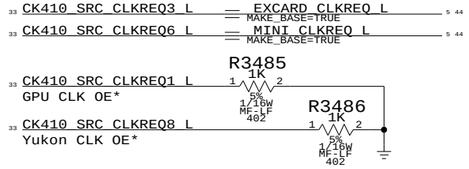
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







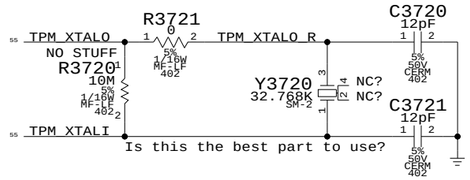
Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

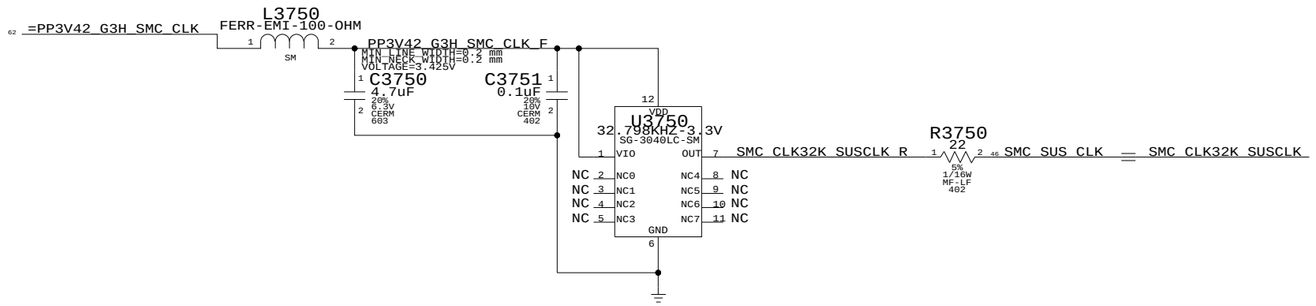
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE	SHT	OF
NONE	34	103

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

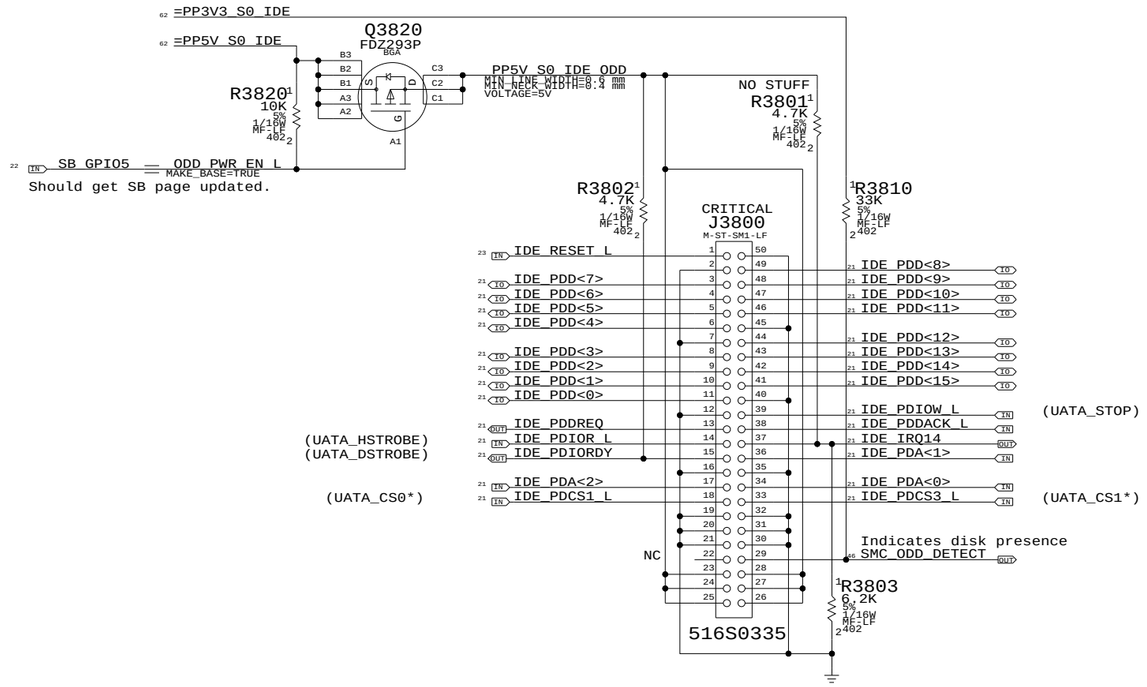
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

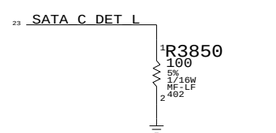
APPLE COMPUTER INC.

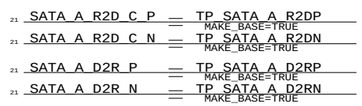
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

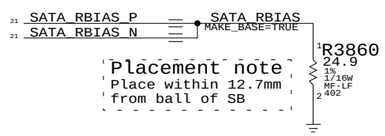
SCALE	SHT	OF
NONE	37	103

IDE (ODD) Connector









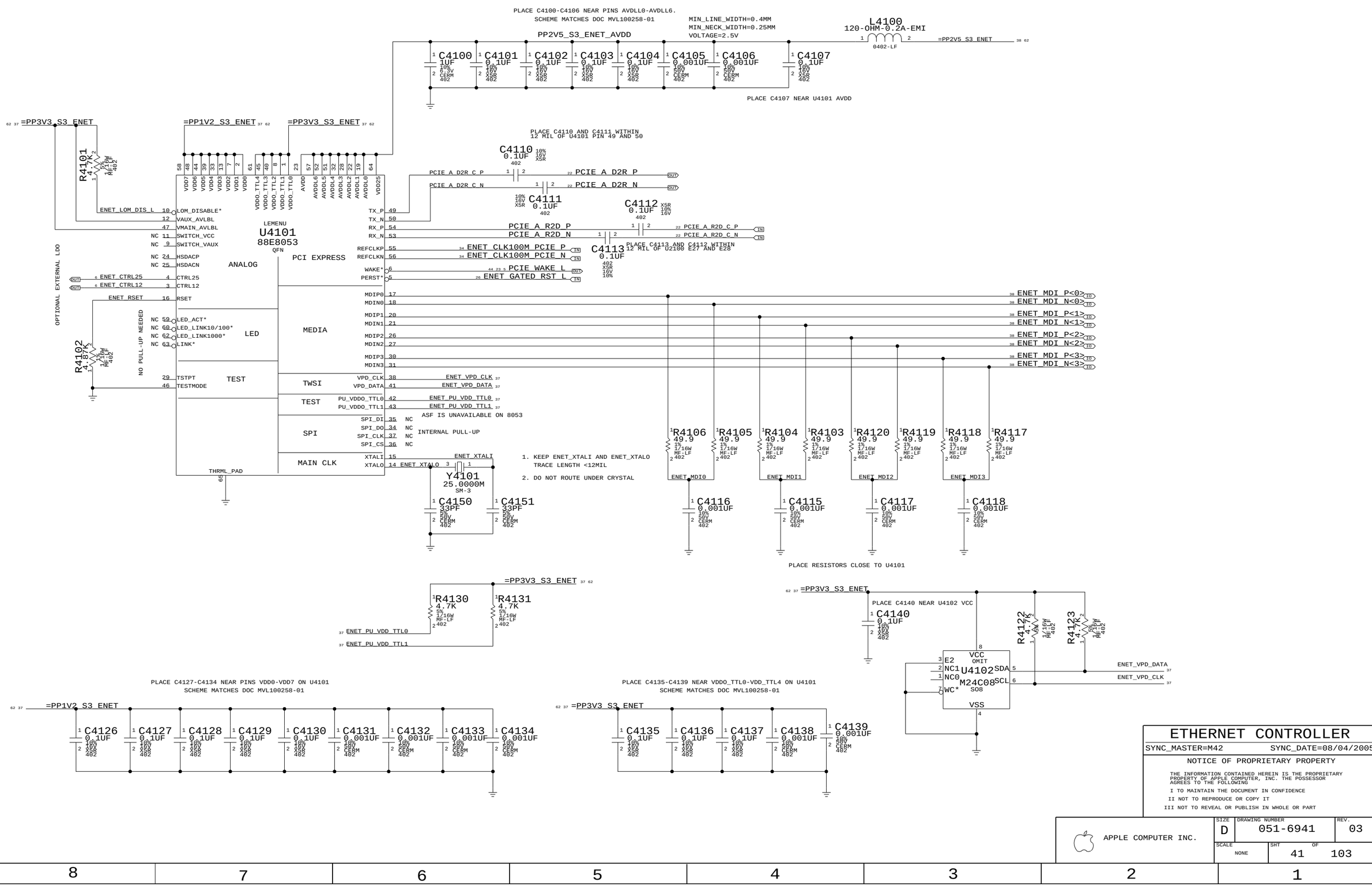
PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	38	103



ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=08/04/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	41	103

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

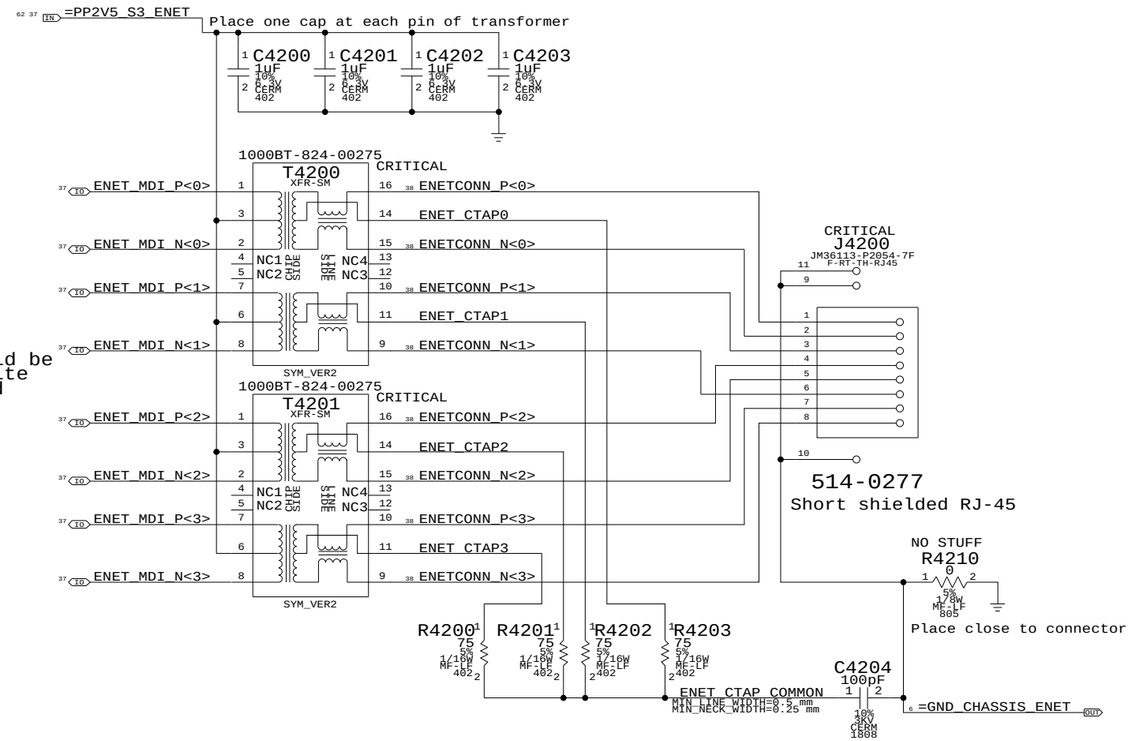
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	42	103

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23560 ADDED
6/21/2005 - CHANGED INT_PIRQD_L TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IDSEL TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT 0 TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW DIFF_PAIR_NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP

=PP3V3_S0_FW

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 10V X5R 402
C4422 0.1UF 10% 10V CERM 402
C4426 0.1UF 10% 10V CERM 402
C4428 0.1UF 10% 10V CERM 402
C4430 0.1UF 10% 10V CERM 402
C4432 0.1UF 10% 10V CERM 402

L4400
600-OHM-300MA
0402

PP3V3_S0_FW_AVDD

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 10V X5R 402
C4429 0.1UF 10% 10V X5R 402
C4425 0.1UF 10% 10V X5R 402

=PP3V3_S0_PCI

CONNECT TO VDD FOR 3.3V OPERATION

U4400
FW32306
BGA
LEMENU

	PCI_AD<0>	F10 PCI_AD0
	PCI_AD<1>	G10 PCI_AD1
	PCI_AD<2>	H10 PCI_AD2
	PCI_AD<3>	H12 PCI_AD3
	PCI_AD<4>	J13 PCI_AD4
	PCI_AD<5>	J12 PCI_AD5
	PCI_AD<6>	K13 PCI_AD6
	PCI_AD<7>	K10 PCI_AD7
	PCI_AD<8>	L12 PCI_AD8
	PCI_AD<9>	M13 PCI_AD9
	PCI_AD<10>	L11 PCI_AD10
	PCI_AD<11>	M12 PCI_AD11
	PCI_AD<12>	M11 PCI_AD12
	PCI_AD<13>	N12 PCI_AD13
	PCI_AD<14>	M10 PCI_AD14
	PCI_AD<15>	N11 PCI_AD15
	PCI_AD<16>	M4 PCI_AD16
	PCI_AD<17>	N5 PCI_AD17
	PCI_AD<18>	N4 PCI_AD18
	PCI_AD<19>	M3 PCI_AD19
	PCI_AD<20>	M2 PCI_AD20
	PCI_AD<21>	N3 PCI_AD21
	PCI_AD<22>	K4 PCI_AD22
	PCI_AD<23>	M1 PCI_AD23
	PCI_AD<24>	K2 PCI_AD24
	PCI_AD<25>	J4 PCI_AD25
	PCI_AD<26>	K1 PCI_AD26
	PCI_AD<27>	J2 PCI_AD27
	PCI_AD<28>	J1 PCI_AD28
	PCI_AD<29>	H2 PCI_AD29
	PCI_AD<30>	H4 PCI_AD30
	PCI_AD<31>	H1 PCI_AD31
	PCI_C_BE_L<0>	K12 PCI_CBE0*
	PCI_C_BE_L<1>	M9 PCI_CBE1*
	PCI_C_BE_L<2>	L3 PCI_CBE2*
	PCI_C_BE_L<3>	L1 PCI_CBE3*
	PCI_PAR	N10 PCI_PAR
	PCI_FRAME_L	N6 PCI_FRAME*
	PCI_IRDY_L	M6 PCI_IRDY*
	PCI_TRDY_L	N7 PCI_TRDY*
	PCI_DEVSEL_L	N8 PCI_DEVSEL*
	PCI_STOP_L	M7 PCI_STOP*
	FW_PCI_IDSEL	L2 PCI_IDSEL
OUT	PCI_REQ3_L	E2 PCI_REQ*
IN	PCI_GNT3_L	E1 PCI_GNT*
	PCI_PERR_L	M8 PCI_PERR*
	PCI_SERR_L	N9 PCI_SERR*
IN	PCI_CLK_FW	G2 PCI_CLK
IO	PM_CLKRUN_L	D1 CLKRUN*
IN	PCI_RST_L	F1 PCI_RST*
OUT	INT_PIRQD_L	D2 PCI_INTA*
OUT	PCI_PME_FW_L	F2 PCI_PME*

THIS IS FROM ICH-7M

R4431 22 5% 1/16W MF 402

197S0030 3.2MMX2.5MM

Y4403
24.576MHZ

R4400 390 1% 1/16W MF 402
C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0
TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

SPEC RECOMMENDS 2.49K

R4452 2.49K 1% 1/16W MF 402
C4420 0.1UF 10% 10V X5R 402
R4420 510K 5% 1/16W MF 402

MODE_420	M5	MODE FOR EXTERNAL LINK
MODE_A	B6	
PC0	E12	FW_PC0 — DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’) SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)
PC1	F13	
PC2	F12	
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

MANUFACTURING TEST PINS

TEST0	C2
TEST1	C1
PHYTEST	A4
SE	A3
SM	B3

VSS0 A1, VSS1 B2, VSS2 C3, VSS3 D4, VSS4 E4, VSS5 E5, VSS6 F4, VSS7 F6, VSS8 F7, VSS9 F8, VSS10 G1, VSS11 G6, VSS12 G7, VSS13 G8, VSS14 H6, VSS15 H7, VSS16 H8, VSS17 J5, VSS18 J9, VSS19 J10, VSS20 K8, VSS21 K9, VSS22 N13, VSSA0 E13, VSSA1 E9, VSSA2 D9, VSSA3 D7, VSSA4 D5

VDD0 G4, VDD1 N1, VDD2 N2, VDD3 K5, VDD4 K9, VDD5 K7, VDD6 L13, VDD7 H13, VDD8 A2, VDDA0 D10, VDDA1 A13, VDDA2 B13, VDDA3 A7, VDDA4 A8, VDDA5 D6

FIREWIRE CONTROLLER

SYNC_MASTER=MSX SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	44	103

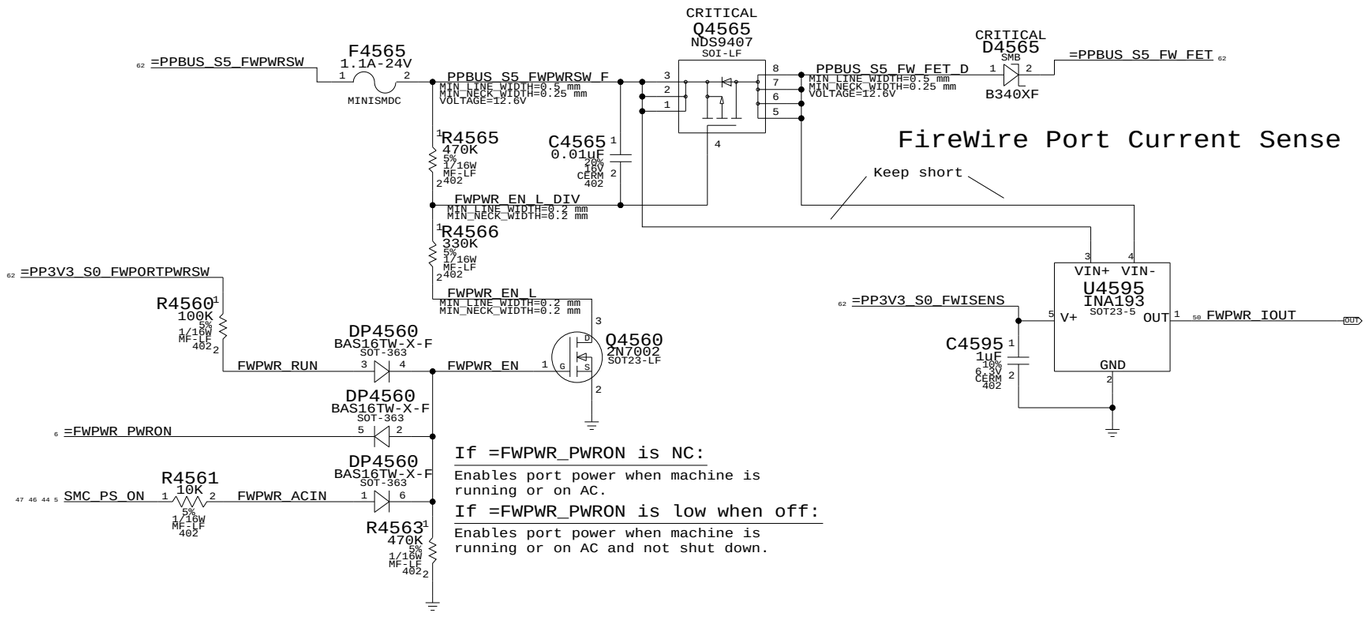
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 45 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 41
	FW	FW_110D	FW_PORT1_TPA_FL_N 41
	FW	FW_110D	FW_PORT1_TPB_FL_P 41
	FW	FW_110D	FW_PORT1_TPB_FL_N 41

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_FW
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

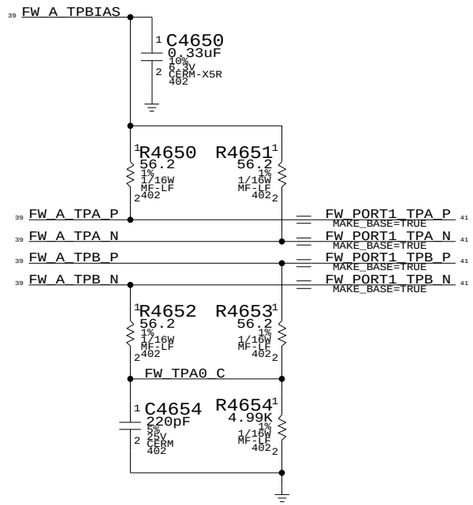
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

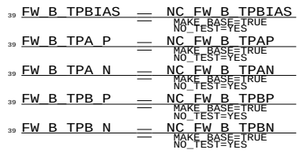
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

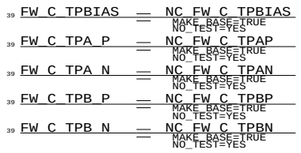
Place close to FireWire PHY



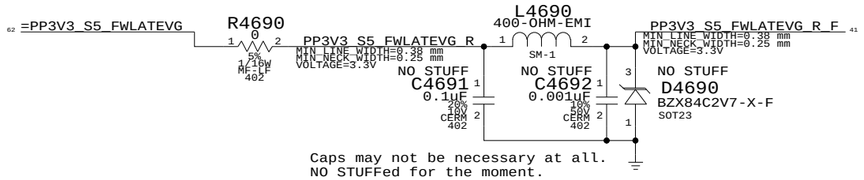
2nd TPA/TPB pair unused



3rd TPA/TPB pair unused

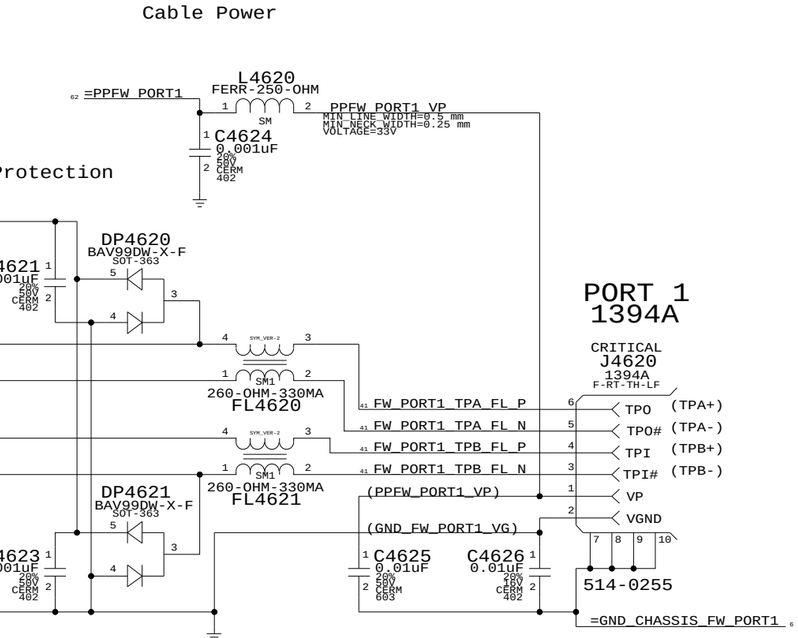


Late-VG Protection Power

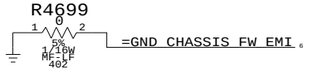


Caps may not be necessary at all.
NO STUFFed for the moment.

Cable Power



"Snapback" & "Late VG" Protection



FireWire Ports

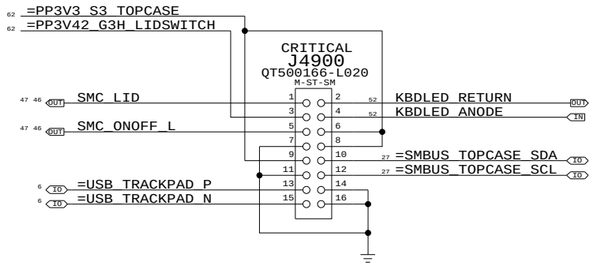
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

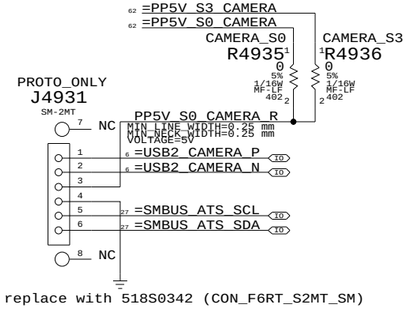
SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 46 OF 103	

Top-Case Connector

(Pinout is almost fixed)

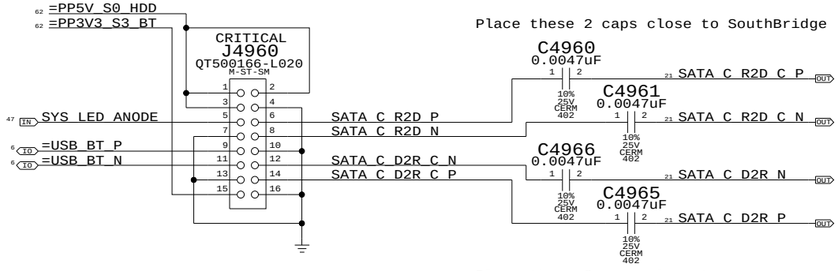


Camera Connector



Post-proto, replace with 518S0342 (CON_F6RT_S2MT_SM)

Bluetooth (M13P) & SATA HDD Flex Connector



Internal USB Connections

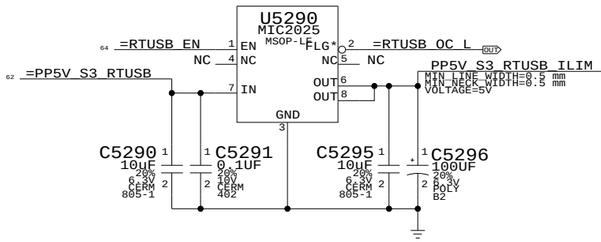
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

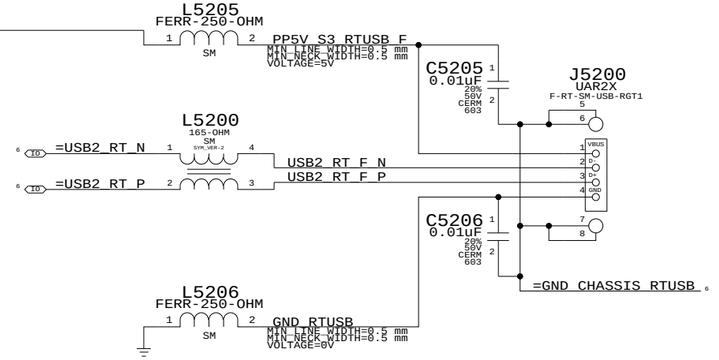
SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 49 OF 103

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

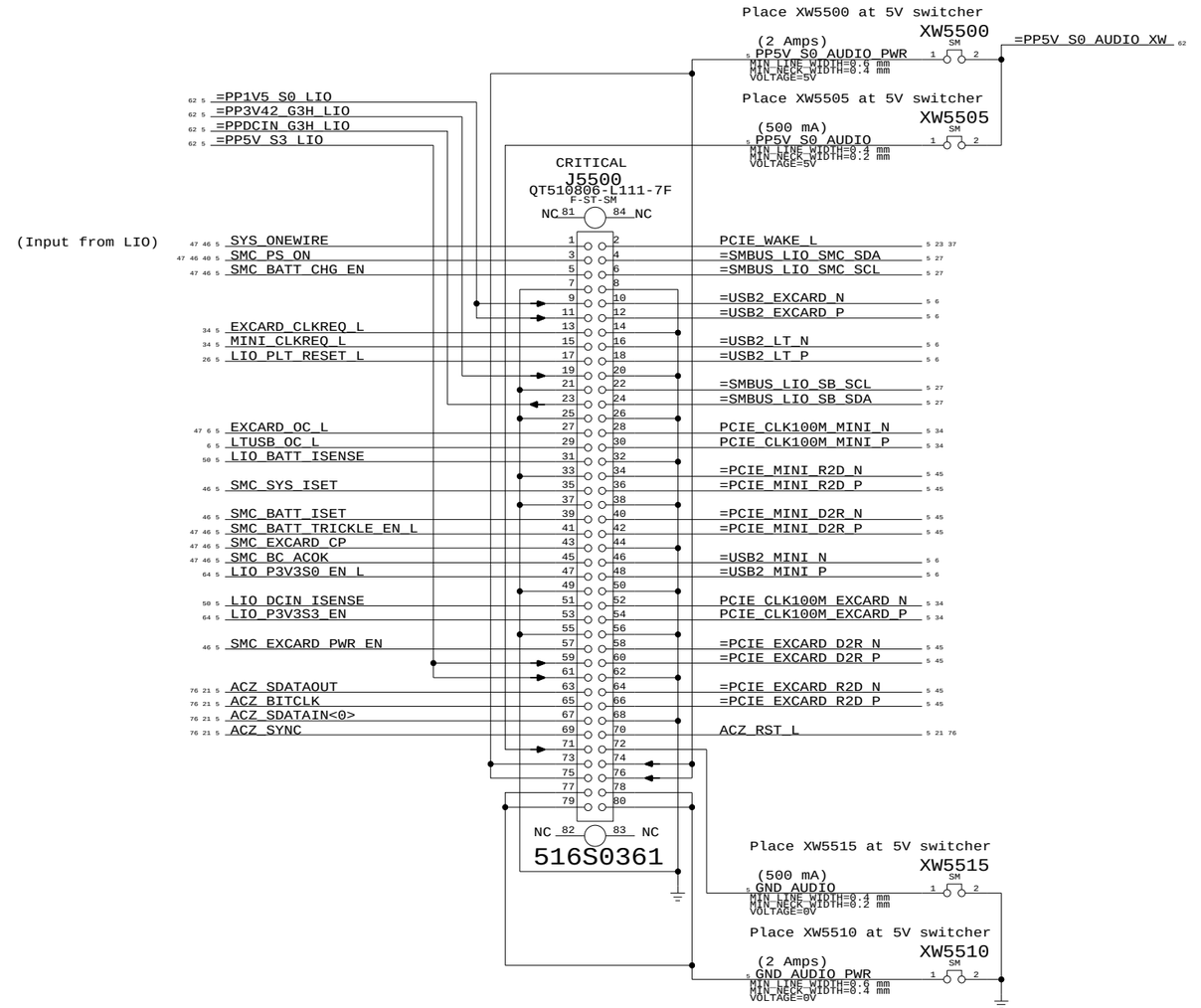
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	52	103

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	55	103

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_MINI_R2D_P	MAKE_BASE=TRUE	PCIE_MINI_R2D_C_P	PCIE_B_R2D_C_P	22
=PCIE_MINI_R2D_N	MAKE_BASE=TRUE	PCIE_MINI_R2D_C_N	PCIE_B_R2D_C_N	22
=PCIE_MINI_D2R_P	MAKE_BASE=TRUE	PCIE_MINI_D2R_P	PCIE_B_D2R_P	22
=PCIE_MINI_D2R_N	MAKE_BASE=TRUE	PCIE_MINI_D2R_N	PCIE_B_D2R_N	22

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_EXCARD_R2D_P	MAKE_BASE=TRUE	PCIE_EXCARD_R2D_C_P	PCIE_C_R2D_C_P	22
=PCIE_EXCARD_R2D_N	MAKE_BASE=TRUE	PCIE_EXCARD_R2D_C_N	PCIE_C_R2D_C_N	22
=PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	PCIE_EXCARD_D2R_P	PCIE_C_D2R_P	22
=PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	PCIE_EXCARD_D2R_N	PCIE_C_D2R_N	22

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP	MAKE_BASE=TRUE	PCIE_D_R2D_C_P	22
TP_PCIE_D_R2DN	MAKE_BASE=TRUE	PCIE_D_R2D_C_N	22
TP_PCIE_D_D2RP	MAKE_BASE=TRUE	PCIE_D_D2R_P	22
TP_PCIE_D_D2RN	MAKE_BASE=TRUE	PCIE_D_D2R_N	22

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP	MAKE_BASE=TRUE	PCIE_E_R2D_C_P	22
TP_PCIE_E_R2DN	MAKE_BASE=TRUE	PCIE_E_R2D_C_N	22
TP_PCIE_E_D2RP	MAKE_BASE=TRUE	PCIE_E_D2R_P	22
TP_PCIE_E_D2RN	MAKE_BASE=TRUE	PCIE_E_D2R_N	22

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP	MAKE_BASE=TRUE	PCIE_F_R2D_C_P	22
TP_PCIE_F_R2DN	MAKE_BASE=TRUE	PCIE_F_R2D_C_N	22
TP_PCIE_F_D2RP	MAKE_BASE=TRUE	PCIE_F_D2R_P	22
TP_PCIE_F_D2RN	MAKE_BASE=TRUE	PCIE_F_D2R_N	22

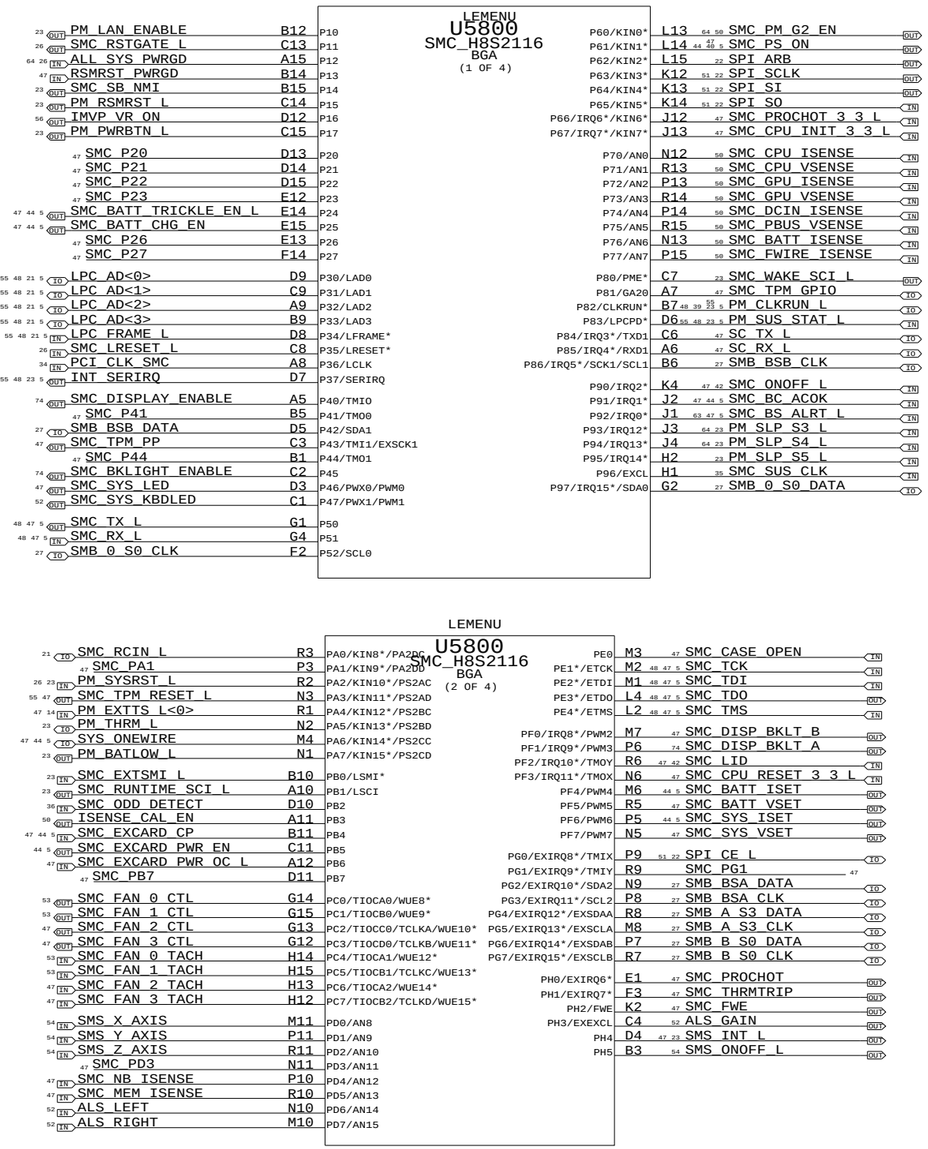
PCI-E Connections

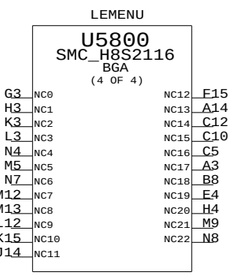
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

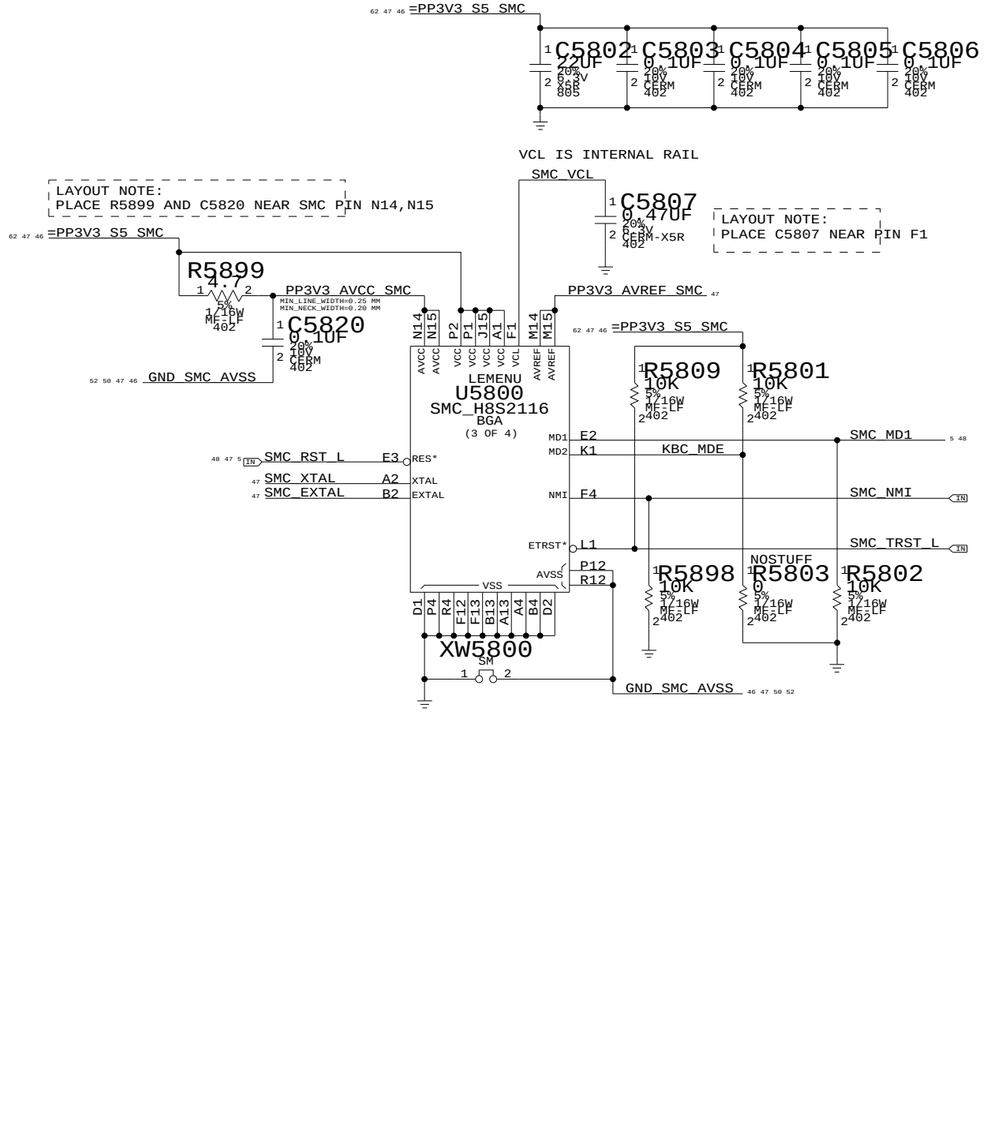
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 57 OF 103







SMC

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

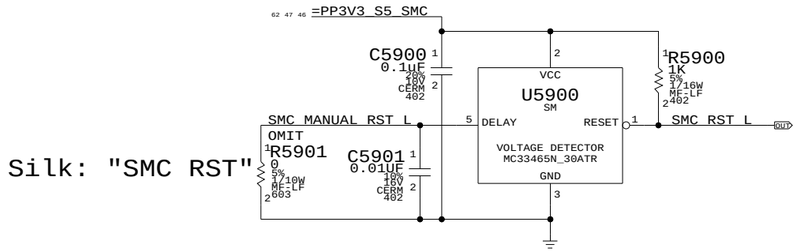
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

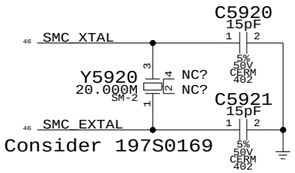
SCALE	SHT	OF
NONE	58	103

SMC Reset Button / Brownout Detect



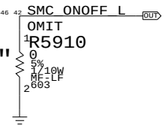
Silk: "SMC RST"

SMC Crystal Circuit



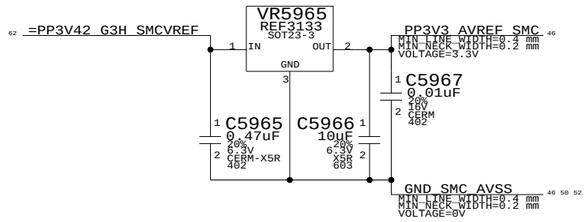
Post-Proto: Consider 197S0169

Debug Power Button

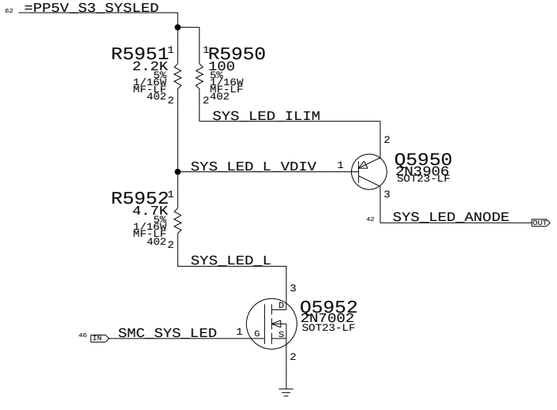


Silk: "PWR BTN"

SMC AVREF Supply

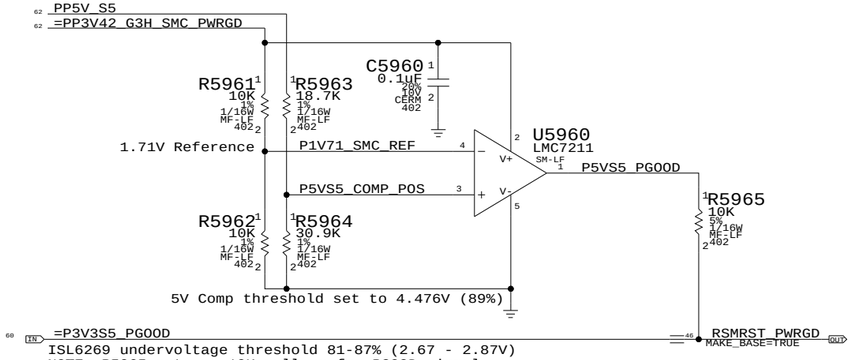


System (Sleep) LED Circuit



SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal

SMC_CPU_INIT_3_3_L — FWH_INIT_L

SMC_NB_ISENSE	SMC_P1V05S0_ISENSE	MAKE_BASE=TRUE
SMC_MEM_ISENSE	SMC_P1V8S3_ISENSE	MAKE_BASE=TRUE
SMC_PA1	BOOT_LPC_SPI_L	MAKE_BASE=TRUE
PM_EXTTS_L<0>	DIMM_OVERTEMP_L	MAKE_BASE=TRUE
SMC_BATT_VSET	TP_SMC_BATT_VSET	MAKE_BASE=TRUE
SMC_SYS_VSET	TP_SMC_SYS_VSET	MAKE_BASE=TRUE
SMC_DISP_BKLT_B	TP_SMC_DISP_BKLT_B	MAKE_BASE=TRUE
SMC_FAN_2_CTL	TP_SMC_FAN_2_CTL	MAKE_BASE=TRUE
SMC_FAN_2_TACH	TP_SMC_FAN_2_TACH	MAKE_BASE=TRUE
SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE
SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE
SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE
SMC_P21	TP_SMC_P21	MAKE_BASE=TRUE
SMC_P22	TP_SMC_P22	MAKE_BASE=TRUE
SMC_P23	TP_SMC_P23	MAKE_BASE=TRUE
SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE
SMC_P27	TP_SMC_P27	MAKE_BASE=TRUE
SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE
SMC_P44	TP_SMC_P44	MAKE_BASE=TRUE
SMC_PB7	TP_SMC_PB7	MAKE_BASE=TRUE
SMC_PD3	TP_SMC_PD3	MAKE_BASE=TRUE
SMC_PG1	TP_SMC_PG1	MAKE_BASE=TRUE

SMC_TPM_GPIO1
R5990 0 5% 1/16W MF-LF 402
SMC_TPM_GPIO — TPM_GPIO1

SMC_TPM_GPIO2
R5991 0 5% 1/16W MF-LF 402
TPM_GPIO2

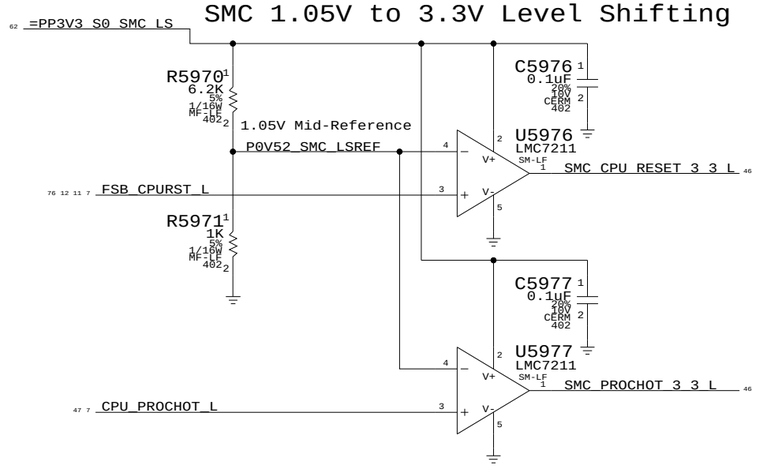
SMC_TPM_PP
R5995 0 5% 1/16W MF-LF 402
SMC_TPM_PP — TPM_PP

DEVELOPMENT
R5992 0 5% 1/16W MF-LF 402
SC_RX_L — SMC_RX_L

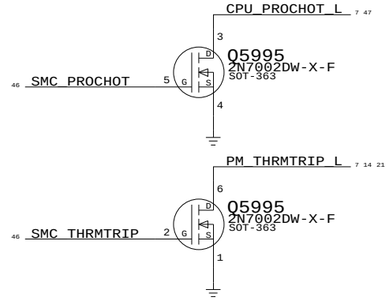
DEVELOPMENT
R5993 0 5% 1/16W MF-LF 402
SC_TX_L — SMC_TX_L

R5994 0 5% 1/16W MF-LF 402
SMC_EXCARD_PWR_OC_L — EXCARD_OC_L

SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting

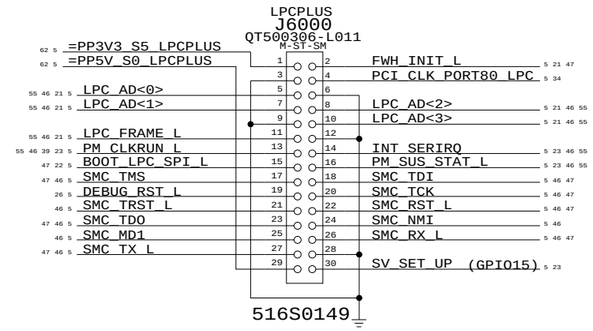


SMS_INT_L	R5829	10K	5% 1/16W MF-LF 402	
SMC_TPM_RESET_L	R5827	10K	5% 1/16W MF-LF 402	
SMC_ONOFF_L	R5808	10K	5% 1/16W MF-LF 402	
SMC_LID	R5814	100K	5% 1/16W MF-LF 402	
SMC_FWE	R5815	10K	5% 1/16W MF-LF 402	
SMC_TX_L	R5817	10K	5% 1/16W MF-LF 402	
SMC_RX_L	R5818	100K	5% 1/16W MF-LF 402	
SYS_ONEWIRE	R5819	2.0K	5% 1/16W MF-LF 402	
SMC_BS_ALRT_L	R5821	100K	5% 1/16W MF-LF 402	
SMC_TMS	R5822	10K	5% 1/16W MF-LF 402	
SMC_TDO	R5823	10K	5% 1/16W MF-LF 402	
SMC_TDI	R5824	10K	5% 1/16W MF-LF 402	
SMC_TCK	R5825	10K	5% 1/16W MF-LF 402	
SMC_BATT_TRICKLE_EN_L	R5810	10K	5% 1/16W MF-LF 402	
SMC_BATT_CHG_EN	R5811	10K	5% 1/16W MF-LF 402	
SMC_PS_ON	R5812	10K	5% 1/16W MF-LF 402	
SMC_CASE_OPEN	R5813	10K	5% 1/16W MF-LF 402	
SMC_BC_ACOK	R5826	470K	5% 1/16W MF-LF 402	
SMC_EXCARD_CP	R5828	10K	5% 1/16W MF-LF 402	

SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 03
	SCALE NONE	SHT 59 OF 103	



LPC+ Debug Connector

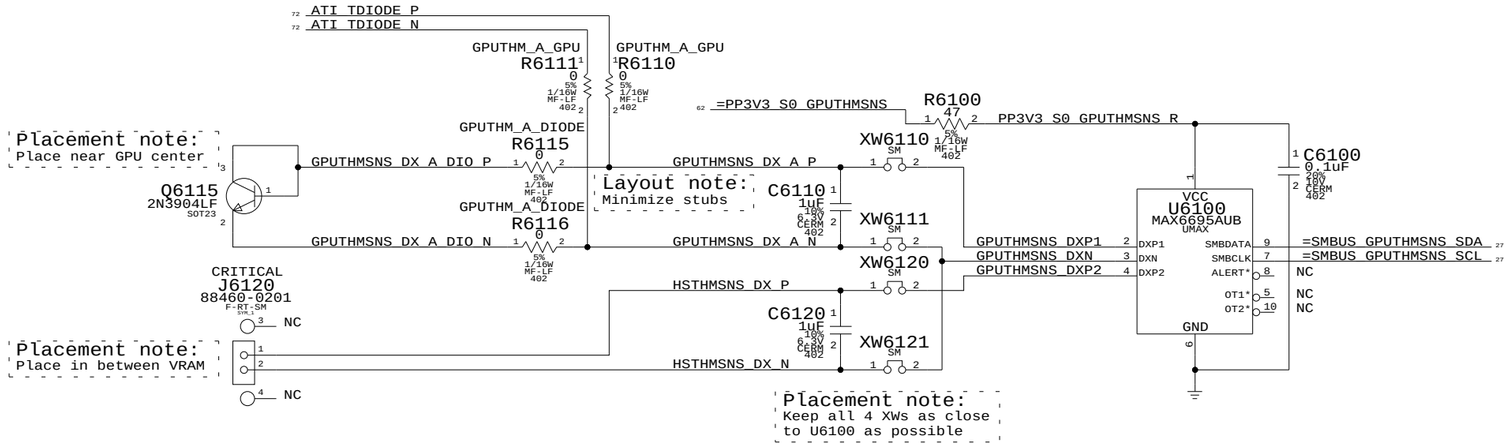
SYNC_MASTER=M42 SYNC_DATE=07/20/2005

APPLE COMPUTER INC.

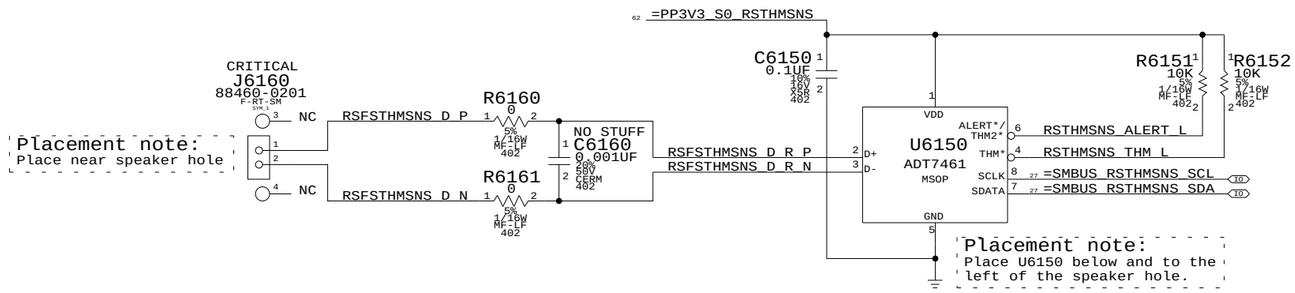
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	60	103

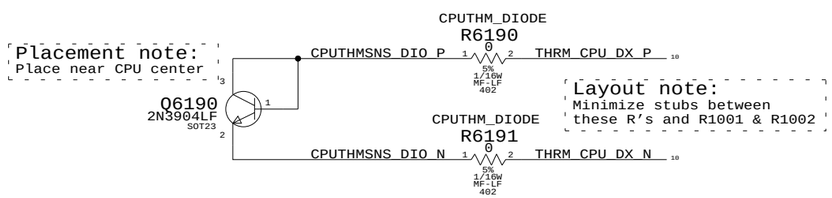
GPU / Heat Pipe Thermal Sensor



Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

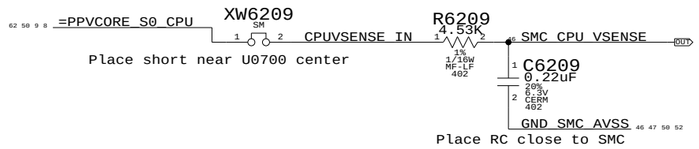
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

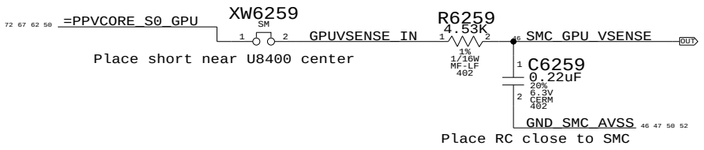
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 61 OF 103	

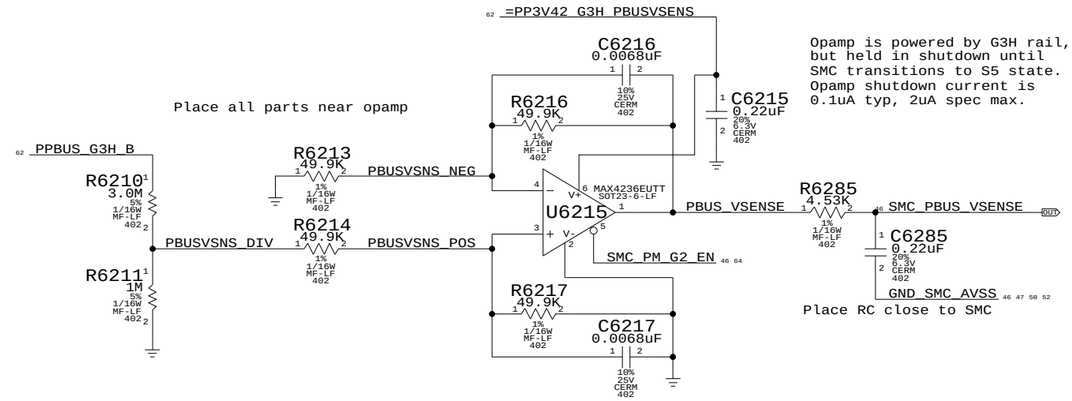
CPU Voltage Sense / Filter



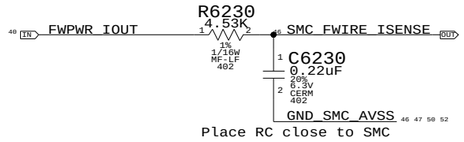
GPU Voltage Sense / Filter



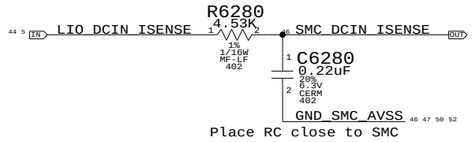
PBUS Voltage Sense Buffer & Filter



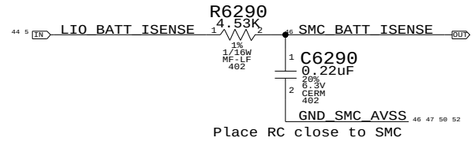
FireWire Current Sense Filter



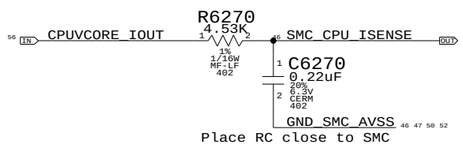
DCIN Current Sense Filter



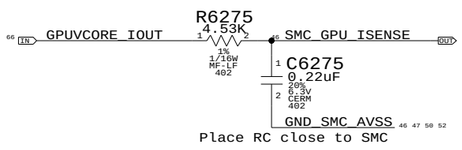
Battery Current Sense Filter



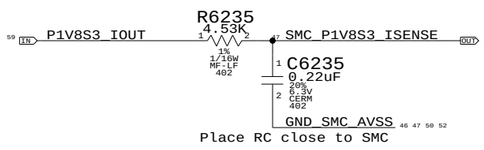
CPU Current Sense Filter



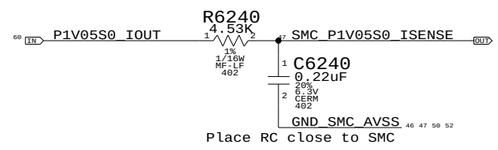
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

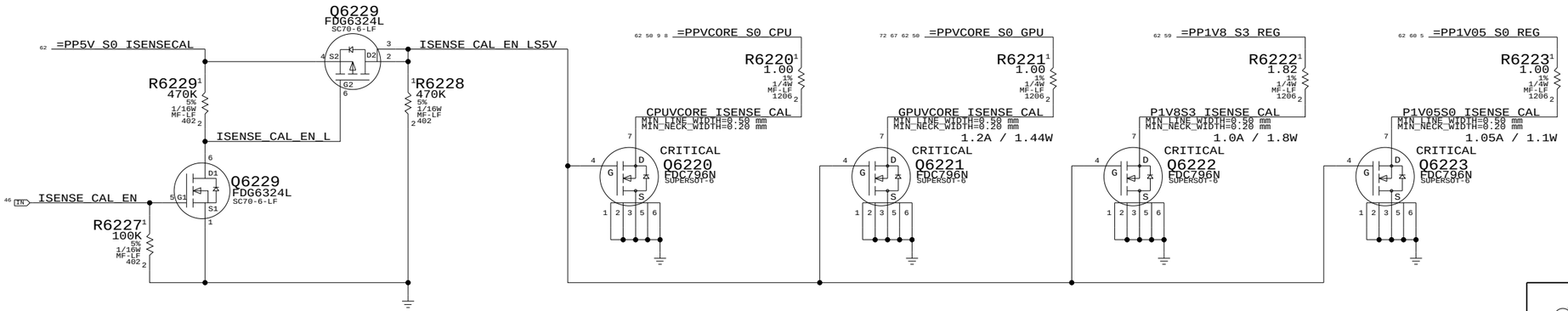


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing

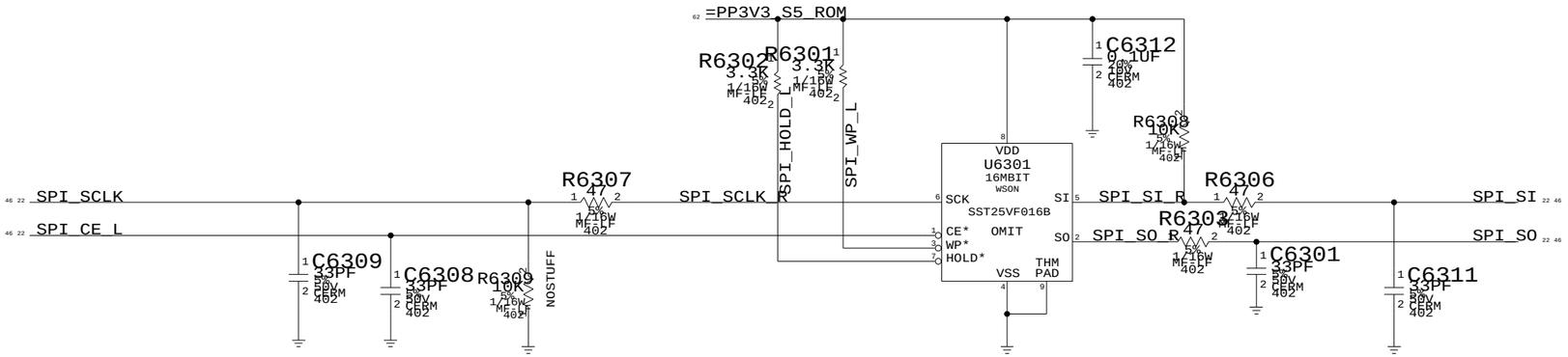
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	62	103

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0384	1	IC,16MBIT -PIN SPI SERIAL FLASH,SOIC8	U6301		LEMENU



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

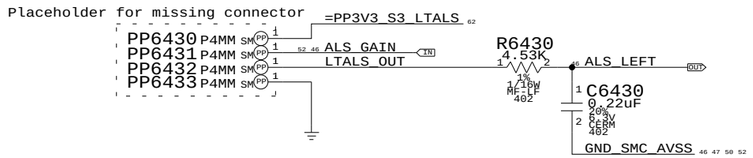
SYNC_MASTER=MSZ SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

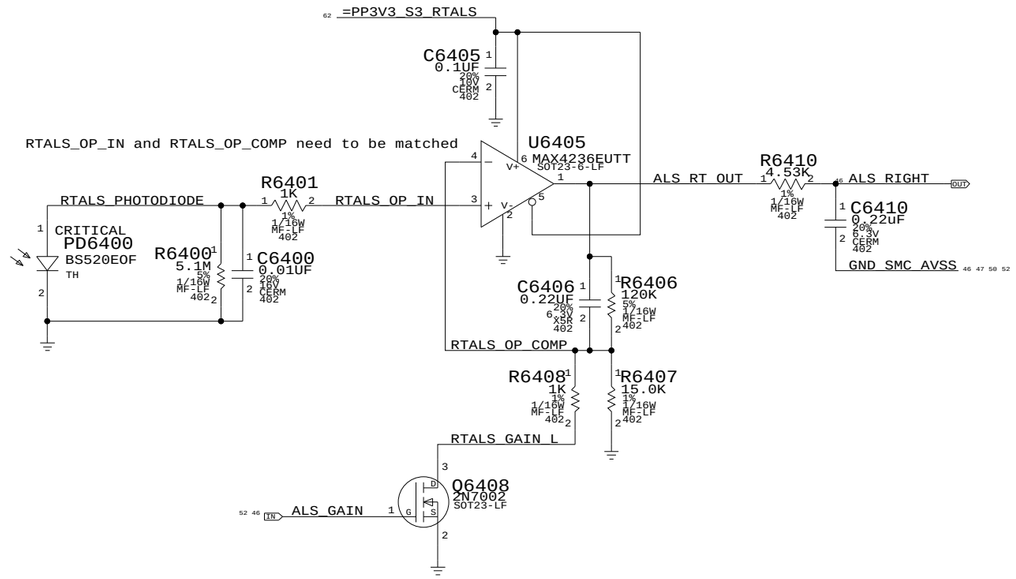
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	63	103

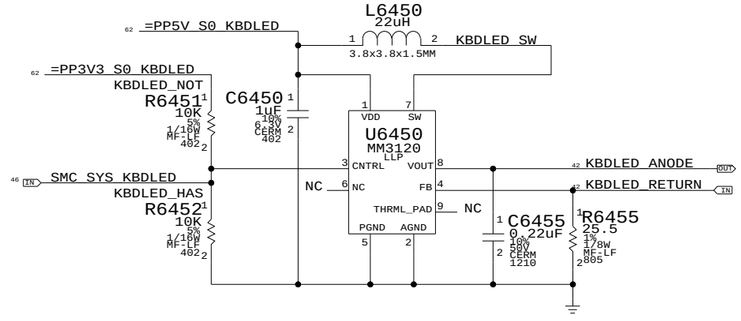
Left ALS "Connector"



Right ALS Circuit



Keyboard LED Driver



ALS Support

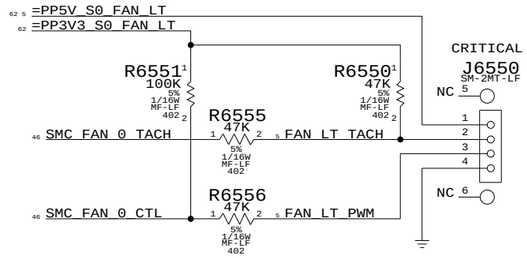
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

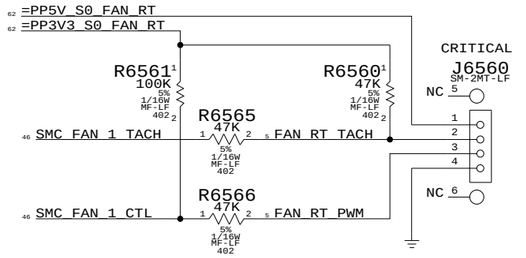
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	64	103

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	65	103

PAGE NOTES

INPUT

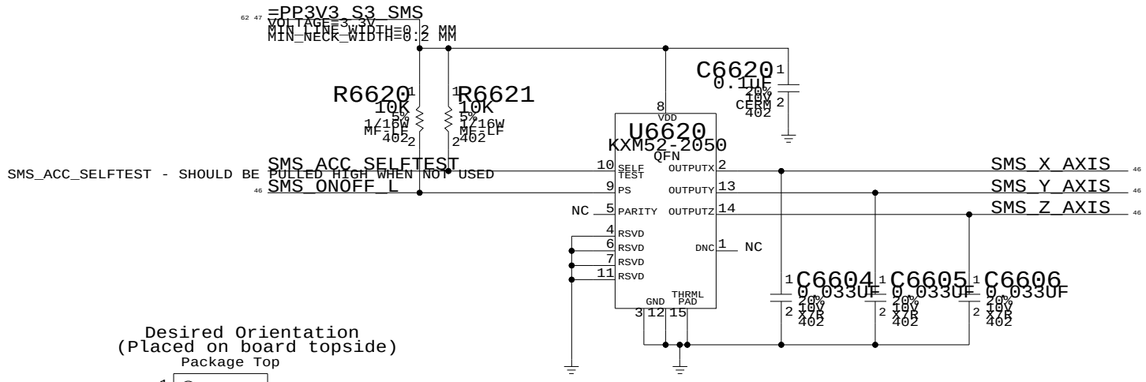
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

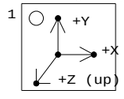
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



Desired Orientation
(Placed on board topside)

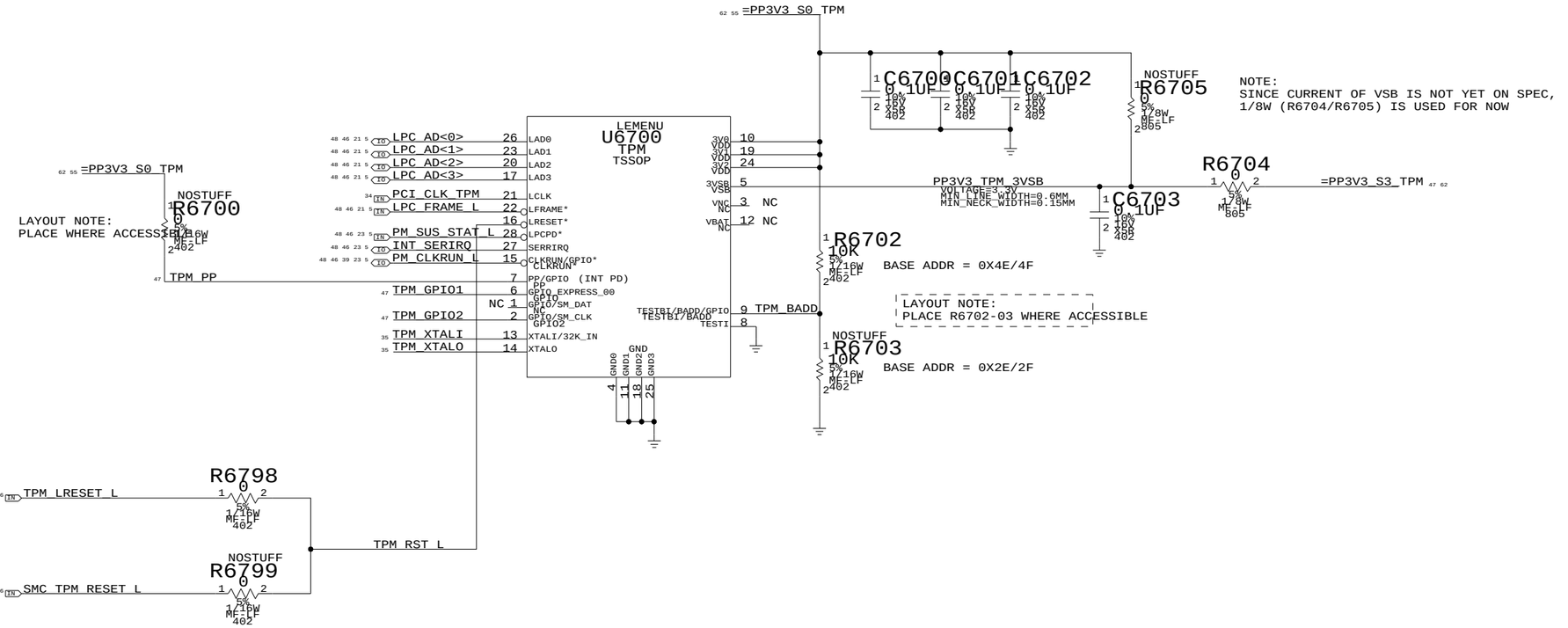


SMS
SYNC_MASTER=MSY SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	66	103



TPM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	67	103

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

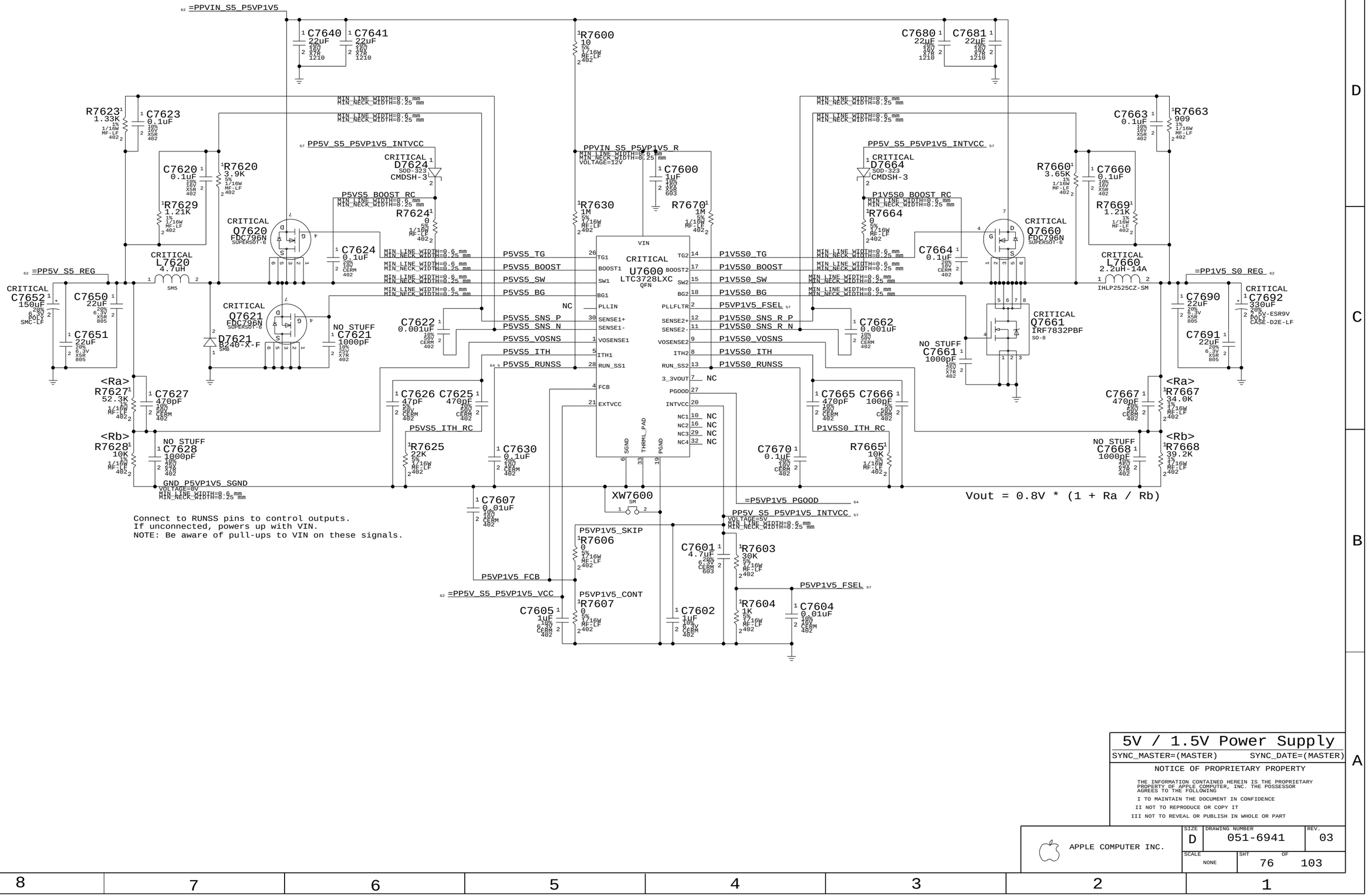
Placement Note:
Keep R7599 and R7596 close to inductor

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 75 OF 103	



5V / 1.5V Power Supply

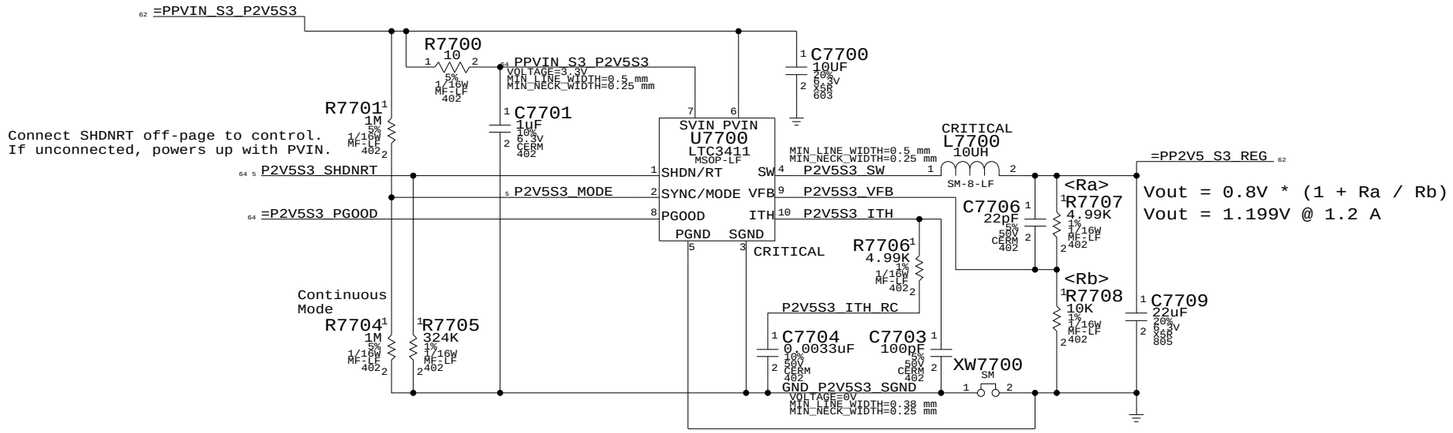
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

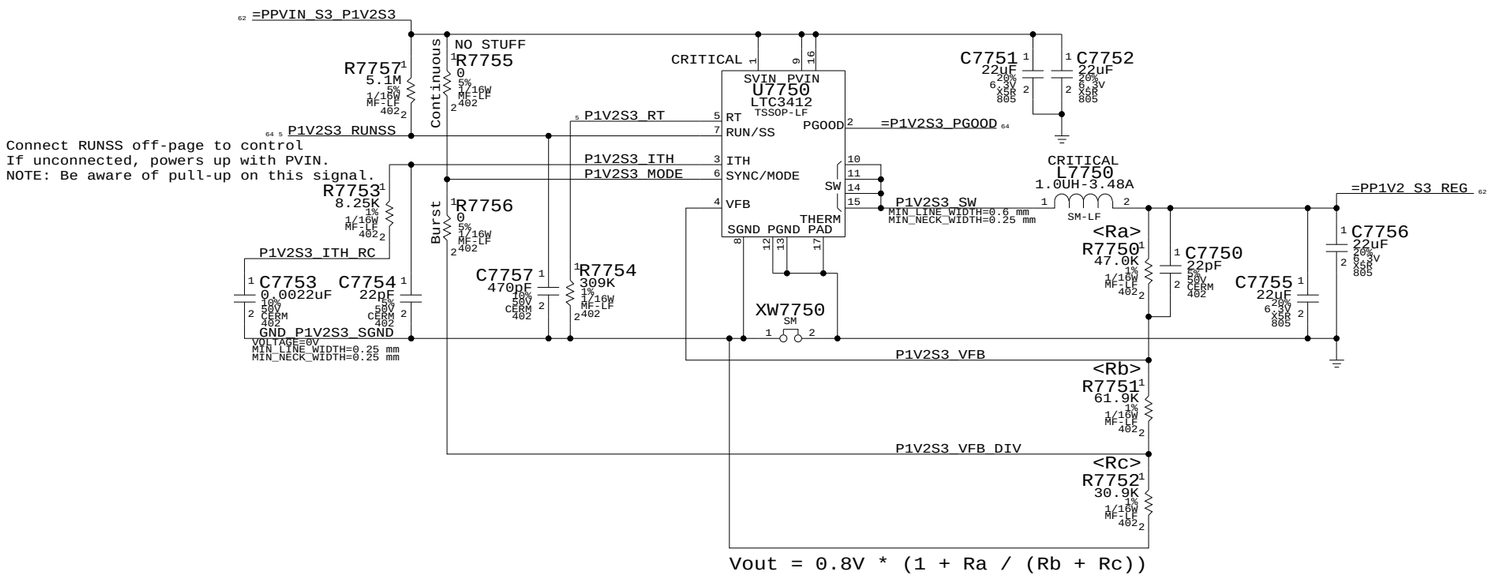
SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	76	103

2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

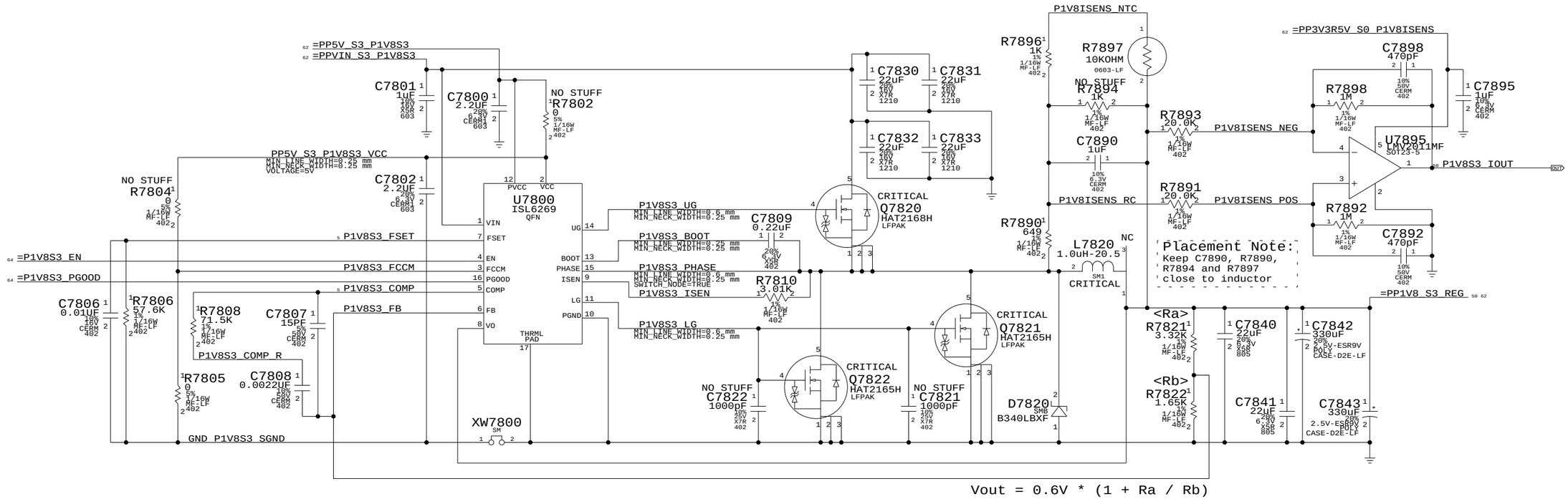
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	77	103

1.8V S3 Current Sense



Vout = 0.6V * (1 + Ra / Rb)

1.8V Supply

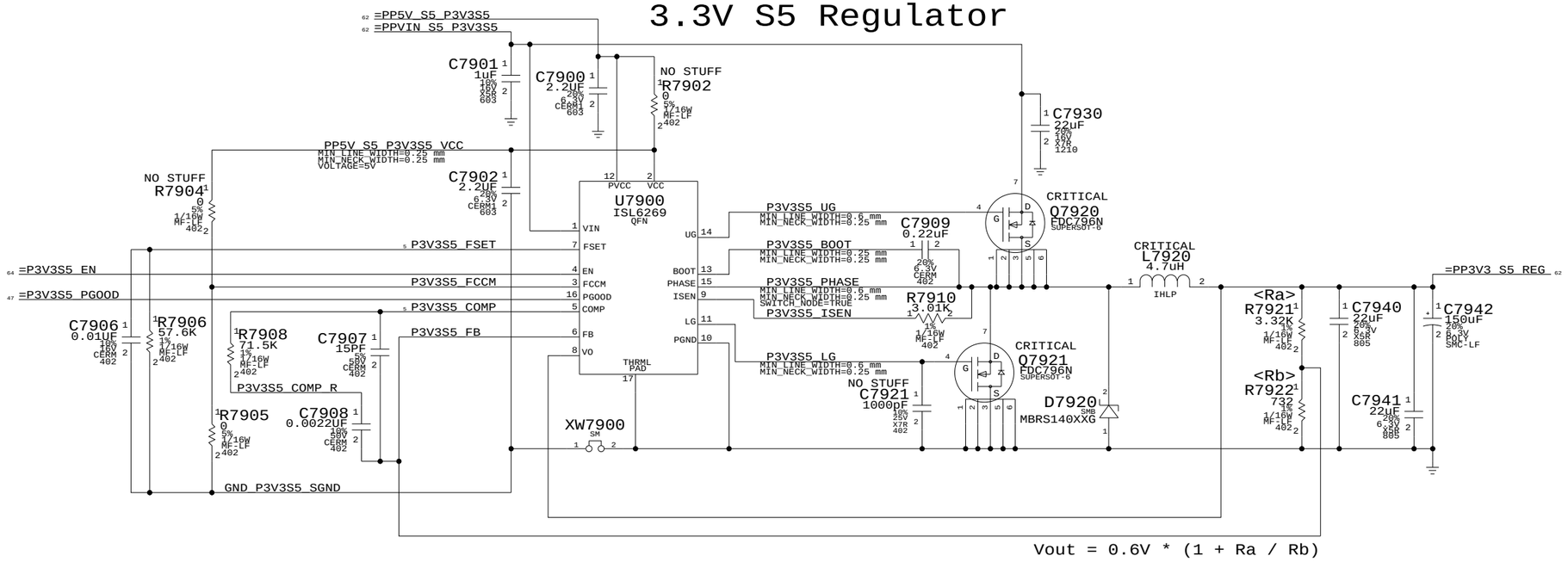
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

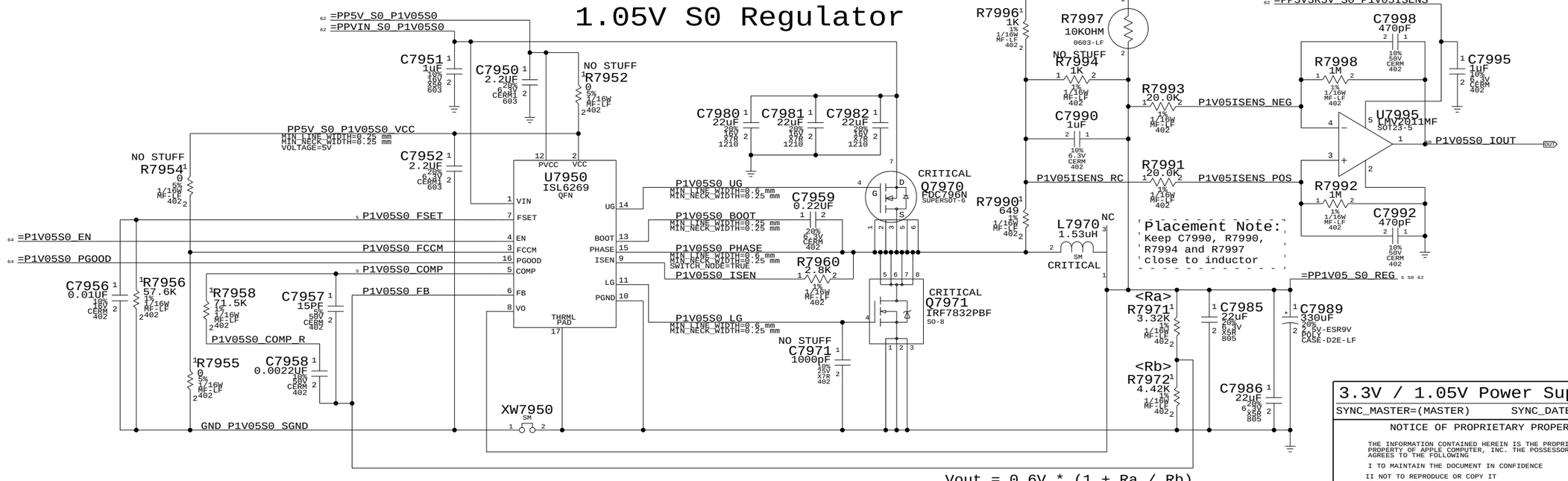
SCALE	SHT	OF
NONE	78	103

3.3V S5 Regulator



Vout = 0.6V * (1 + Ra / Rb)

1.05V S0 Regulator



Vout = 0.6V * (1 + Ra / Rb)

1.05V Current Sense

3.3V / 1.05V Power Supplies

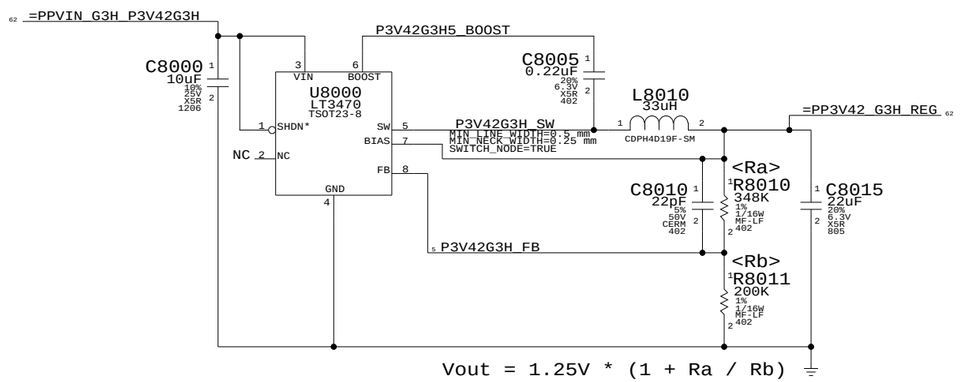
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE	SHT	OF
NONE	79	103

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

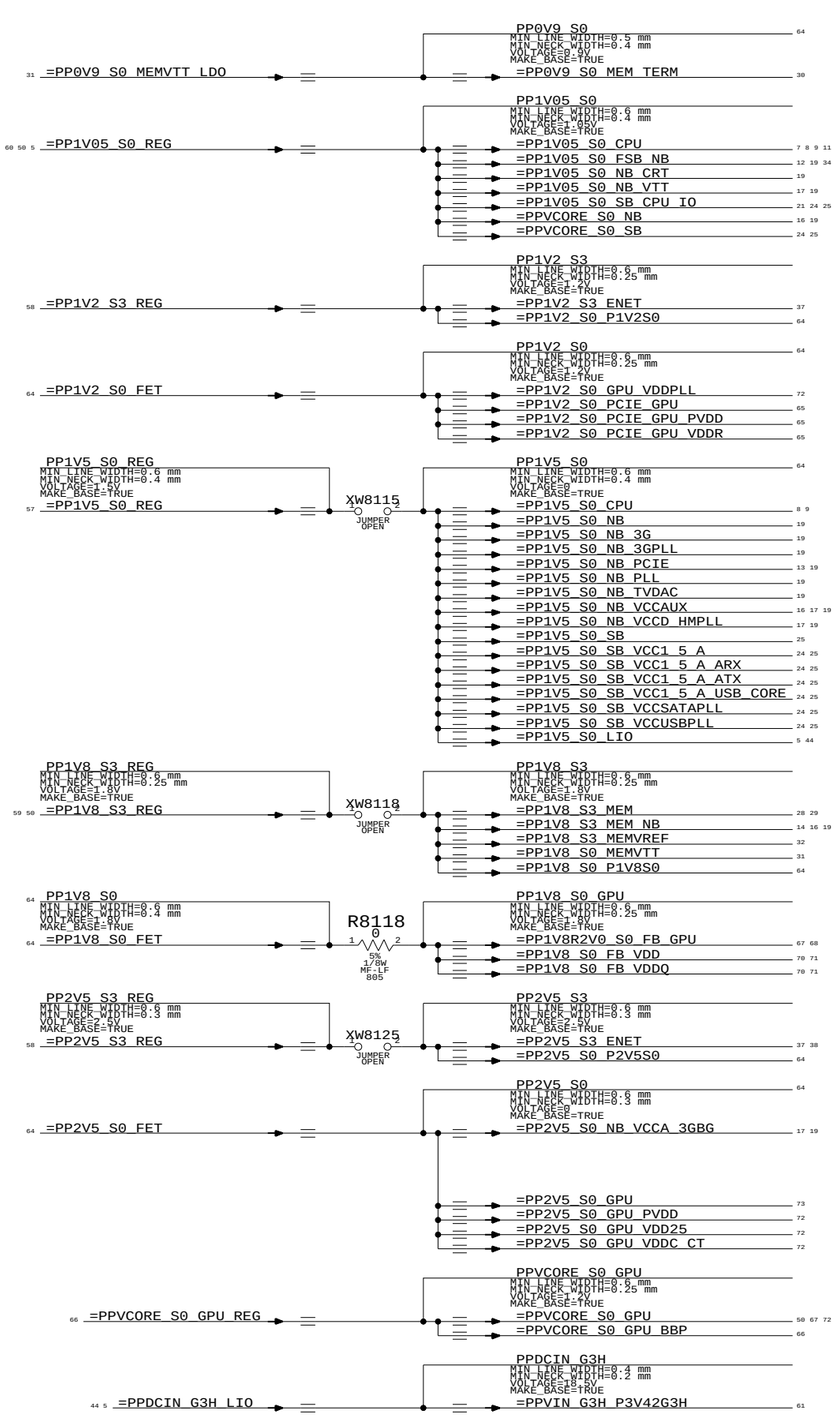


Vout = 1.25V * (1 + Ra / Rb)

3.3V G3Hot Supply	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 80 OF 103	



Note: Place all jumpers on top-side of MLB

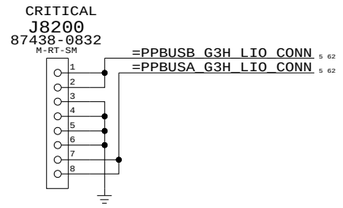
Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

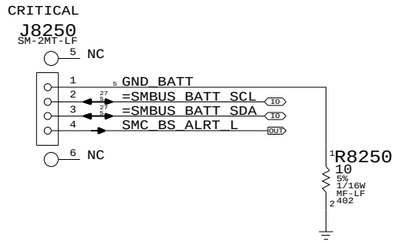
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 81 OF 103	

Left I/O Power Connector



Battery Connector (Digital Signals)



PBus-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	82	103

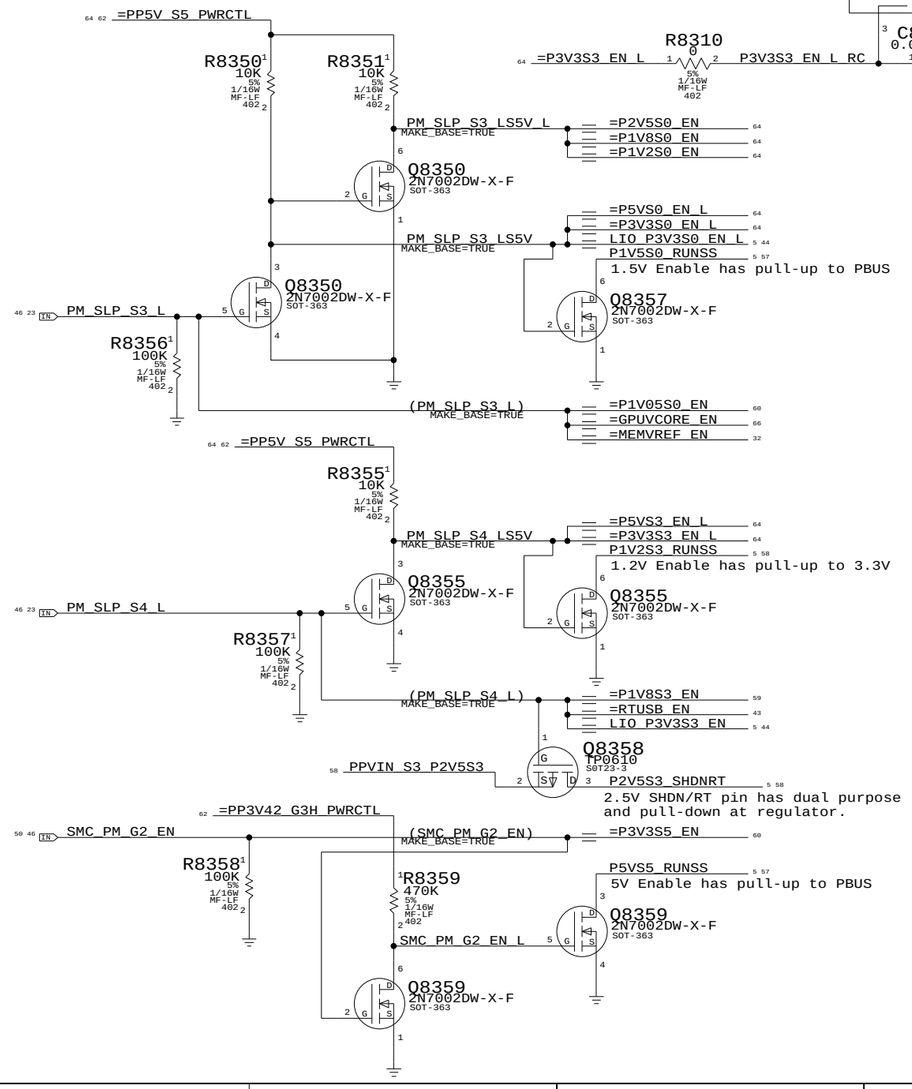
Unused PGOOD Signals

57 =P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)
58 =P2V5S3_PGOOD — TP_P2V5S3_PGOOD (MAKE_BASE=TRUE)
59 =P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)
58 =P1V2S3_PGOOD — TP_P1V2S3_PGOOD (MAKE_BASE=TRUE)

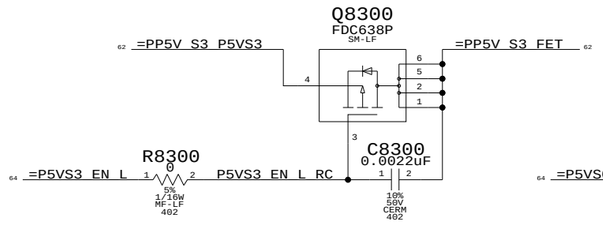
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

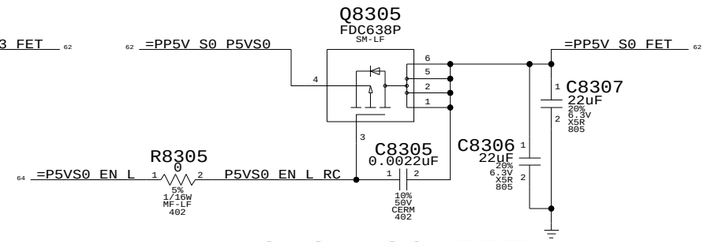
Power Control Signals



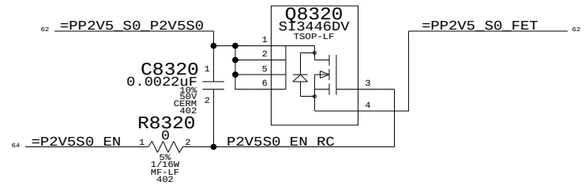
5V S3 FET



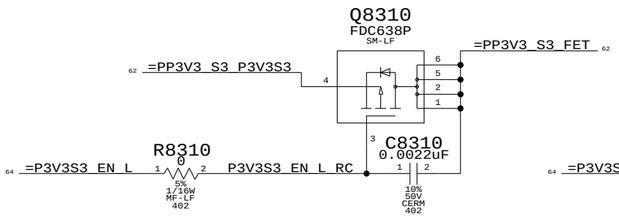
5V S0 FET



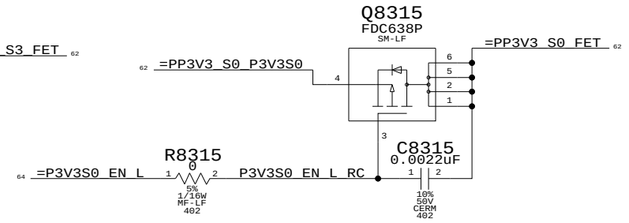
2.5V S0 FET



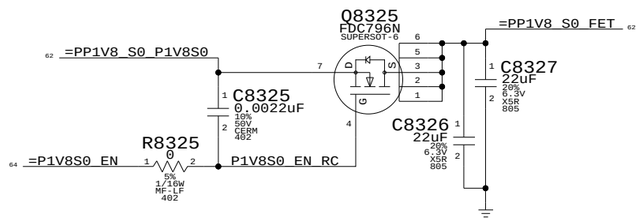
3.3V S3 FET



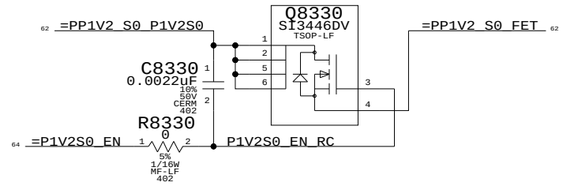
3.3V S0 FET



1.8V S0 FET



1.2V S0 FET

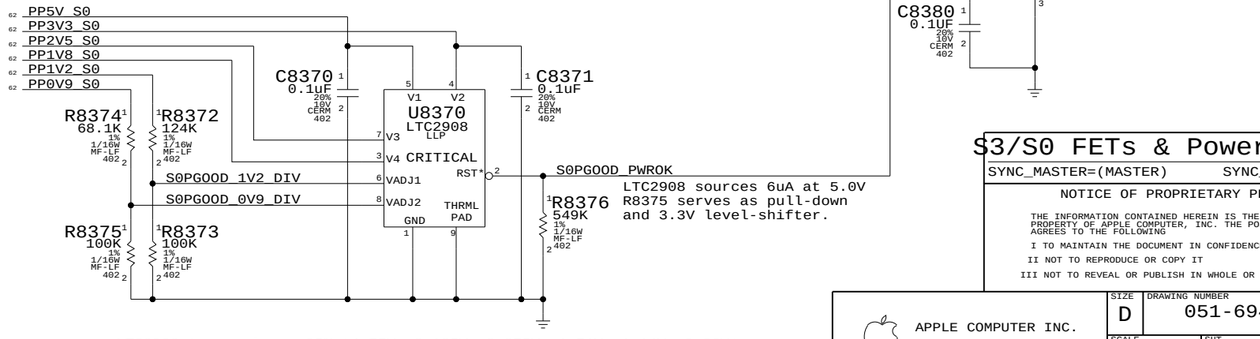


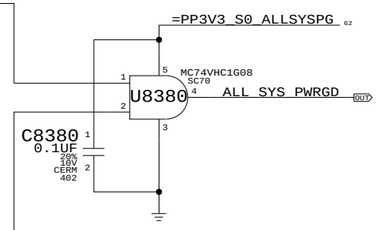
1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation





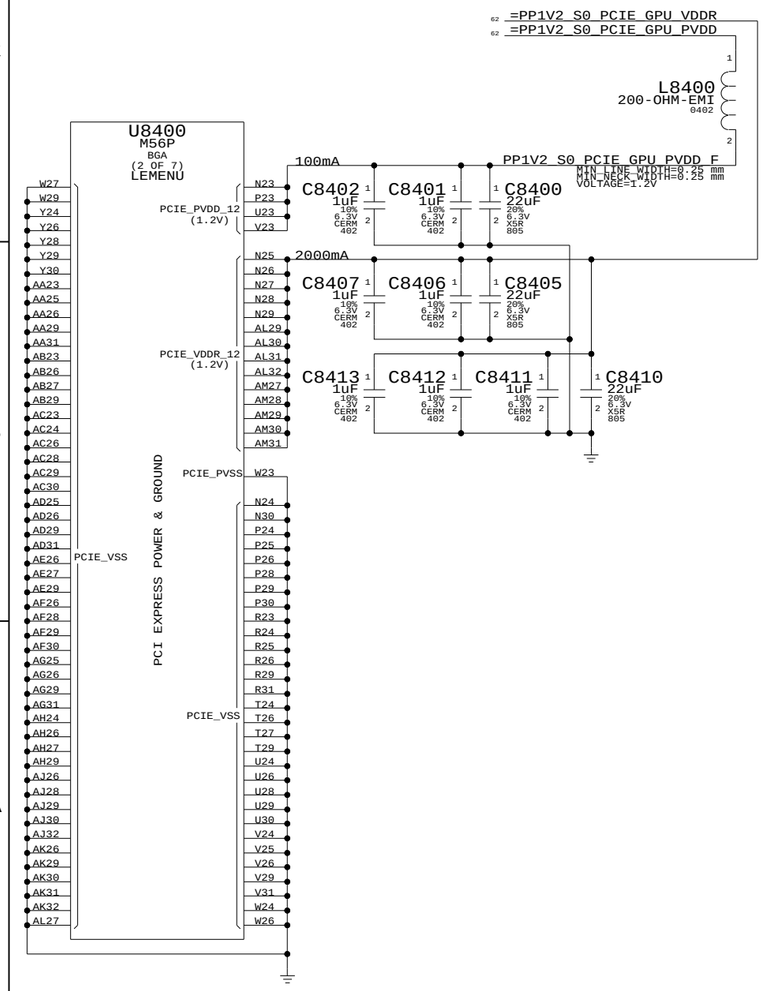
S3/S0 FETs & Power Control

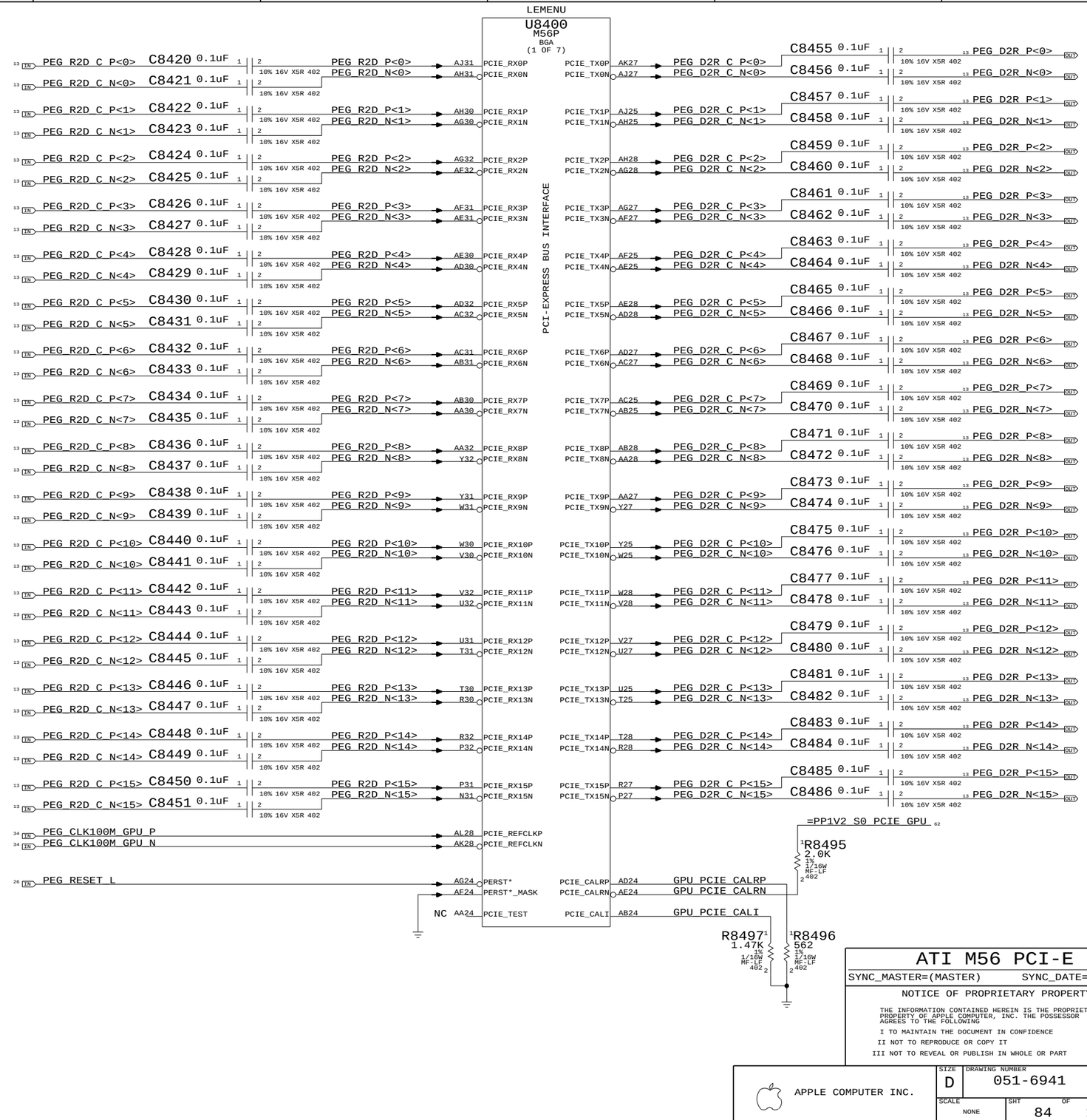
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	83	103





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 84 OF 103	

GPU VCore Supply

=PP5V_S0_GPUVCORE
=PPVIN_S0_GPUVCORE
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
NO STUFF R8504 0 5% 1/16W MF-LF 402
R8507 10K 1% 1/16W MF-LF 402
C8502 2.2UF 20% 6.3V CERM 603
U8500 ISL6269 QFN
PVCC VCC VIN FSET EN FCCM PGOOD COMP FB VO UG BOOT PHASE ISEN LG PGND THRML PAD
=GPUVCORE_EN
GPUVCORE_PGOOD
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
R8508 71.5K 1% 1/16W MF-LF 402
C8507 15PF 5% 50V CERM 402
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
GPUVCORE_COMP_R
R8505 0 5% 1/16W MF-LF 402
C8508 0.0022UF 10% 50V CERM 402
GND_GPUVCORE_SGND
XW8500 SM
GPUVCORE_UG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
GPUVCORE_BOOT
GPUVCORE_PHASE
SWITCH_NODE=TRUE
GPUVCORE_ISEN
GPUVCORE_LG
C8509 0.22UF 20% 25V CERM 402
R8510 3.01K 1% 1/16W MF-LF 402
C8530 22uF 20% 16V X7R 1210
C8531 22uF 20% 16V X7R 1210
C8532 22uF 20% 16V X7R 1210
CRITICAL Q8520 HAT2168H LFPAK
CRITICAL Q8521 HAT2165H LFPAK
CRITICAL Q8522 HAT2165H LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402
CRITICAL L8520 1.0uH-20.5 SM1
D8520 SME B340LBXF
GPUISENS_NTC
R8596 1K 1% 1/10W MF-LF 402
R8597 10KOHM 0603-LF
NO STUFF R8594 1K 1% 1/10W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
R8593 20.0K 1% 1/10W MF-LF 402
GPUISENS_NEG
GPUISENS_RC
R8591 20.0K 1% 1/10W MF-LF 402
GPUISENS_POS
R8590 649 1% 1/10W MF-LF 402
=PP3V3R5V_S0_GPUISENS
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
GPUVCORE_IOUT
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402
Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor
=PPVCORE_S0_GPU_REG
<Ra> R8521 10K 1% 1/16W MF-LF 402
<Rb> R8522 15.0K 1% 1/16W MF-LF 402
<Rc> R8523 60.4K 1% 1/16W MF-LF 402
C8540 22uF 20% 6.3V X5R 805
C8541 22uF 20% 6.3V X5R 805
C8542 330uF 20% 2.5V-ESR9V 2.5V-ESR CASE-D2E-LF
C8543 330uF 20% 2.5V-ESR9V 2.5V-ESR CASE-D2E-LF
GPUVCORE_FB_LOW
R8525 0 5% 1/16W MF-LF 402
GPU_VCORE_LOW
GPU_VCORE_LOW_RC
R8524 10K 5% 1/16W MF-LF 402
C8523 0.1uF 10% 16V X5R 402
Q8523 2N7002 SOT23-LF

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.7V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

=PPVCORE_S0_GPU_BBP
GPUBB_EN_L
Q8575 FDC796N SUPERSOT-6 CRITICAL
=PP3V3_S0_GPUBBP
GPUBB_EN
U8550 FAN2558 SOT23-6-LF CRITICAL
VIN PG EN GND VOUT ADJ
=PPVOUT_S0_GPUBBP_LDO
C8551 2.2uF 20% 6.3V CERM 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22uF 20% 6.3V X5R 805
GPUBBP_ADJ
<Rc> R8554 140K 1% 1/16W MF-LF 402
<Rb> R8556 13.3K 1% 1/16W MF-LF 402
C8557 22uF 20% 6.3V X5R 805
GPUBBP_ADJ_LOW
Q8554 2N7002 SOT23-LF
GPU_VCORE_LOW

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
FDC796N max Vgs is 3.0V
Vin must be > 4.2V
=PP5V_S0_GPUBBCTL
R8570 100K 5% 1/10W MF-LF 402
=PP3V3_S0_GPUBBCTL
GPU_BB_CTL
R8561 0 5% 1/16W MF-LF 402
GPU_GENERICD
GPU_BB_EN
U8560 MC74VHC1G08 SC70
GPUBB_EN
GPUBB_EN_L
R8560 10K 5% 1/16W MF-LF 402
C8560 1uF 10% 6.3V CERM 402
Q8570 2N7002 SOT23-LF
C8570 0.01uF 10% 16V CERM 402

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.7V when active.
When inactive, provides VSS to BBN pins.

=PP3V3_S0_GPUBBN
C8580 10uF 20% 6.3V X5R 603
CRITICAL L8585 15uH SDQ12150-SM
GPUBBN_SW
GPUBBN_D
C8585 330pF 10% 50V CERM 402
GPUBBN_D_RC
R8585 10 1% 1/16W MF-LF 603
U8580 LT3483 TSOT23-6 CRITICAL
VIN SHDN* GND SW FB
(GPUBBN_D)
GPUBB_EN
GPUBBN_FB
C8586 220pF 10% 25V CERM 402
<Ra> R8586 69.8K 1% 1/16W MF-LF 402
Vout = -10uA * Ra
C8589 22uF 20% 6.3V X5R 805
=PNVOUT_S0_GPUBBN_REG
Q8576 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
Watch FET Vgs, since Vs will be negative
FDC796N min Vgs is 1.0V

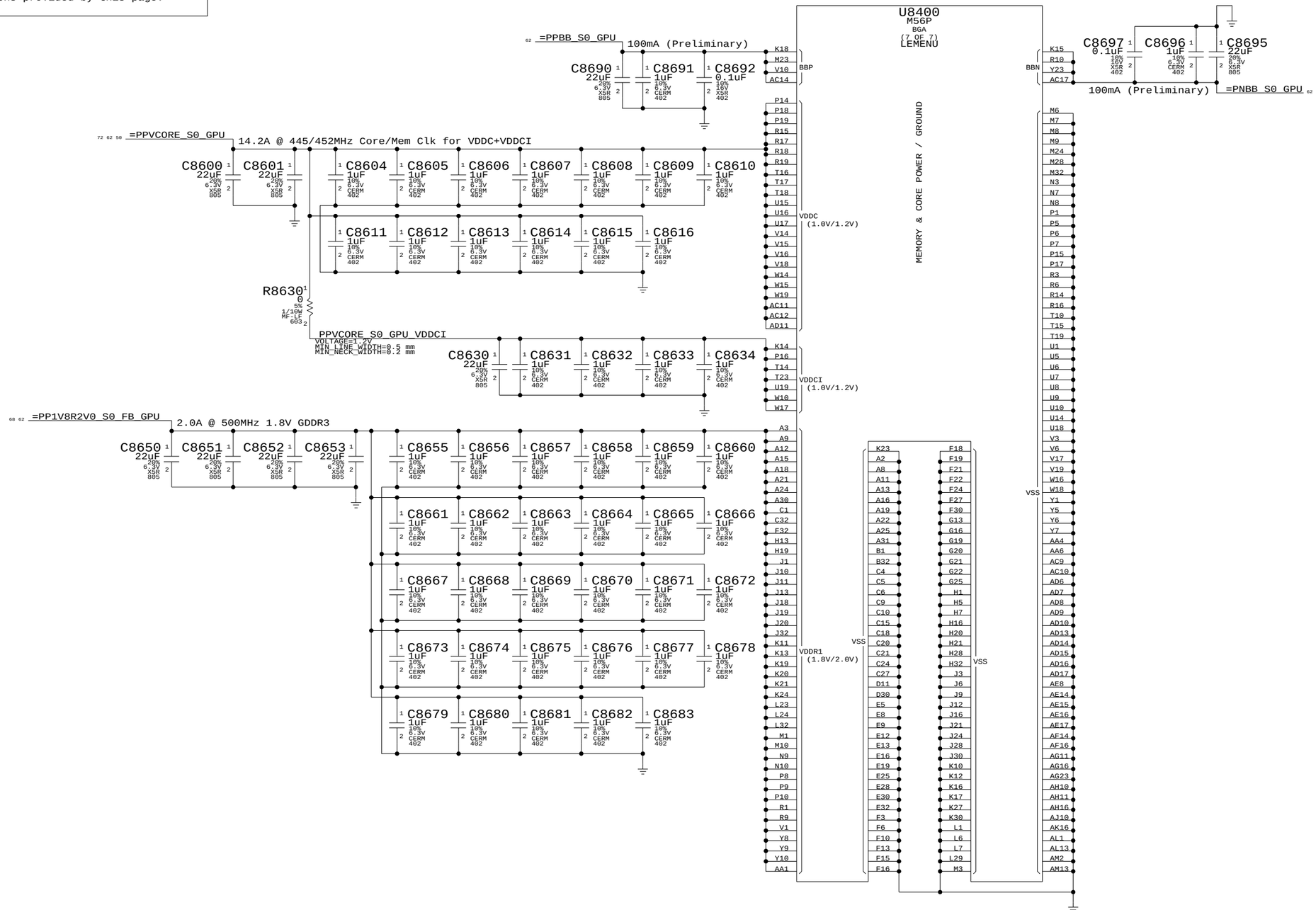
GPU (M56) Core Supplies		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941 / REV. 03
	SCALE NONE	SHT OF 85 103

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

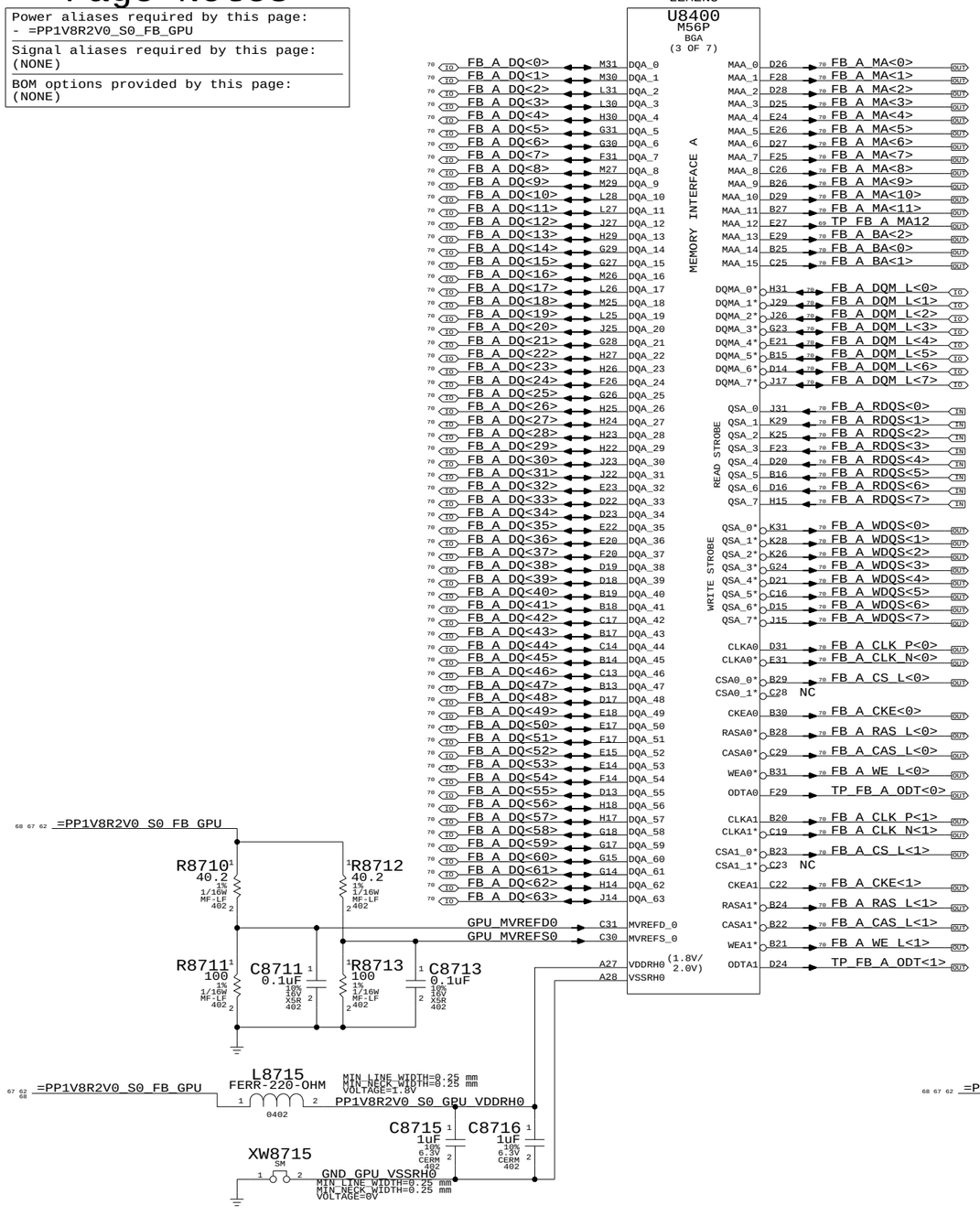
SCALE	SHT	OF
NONE	86	103

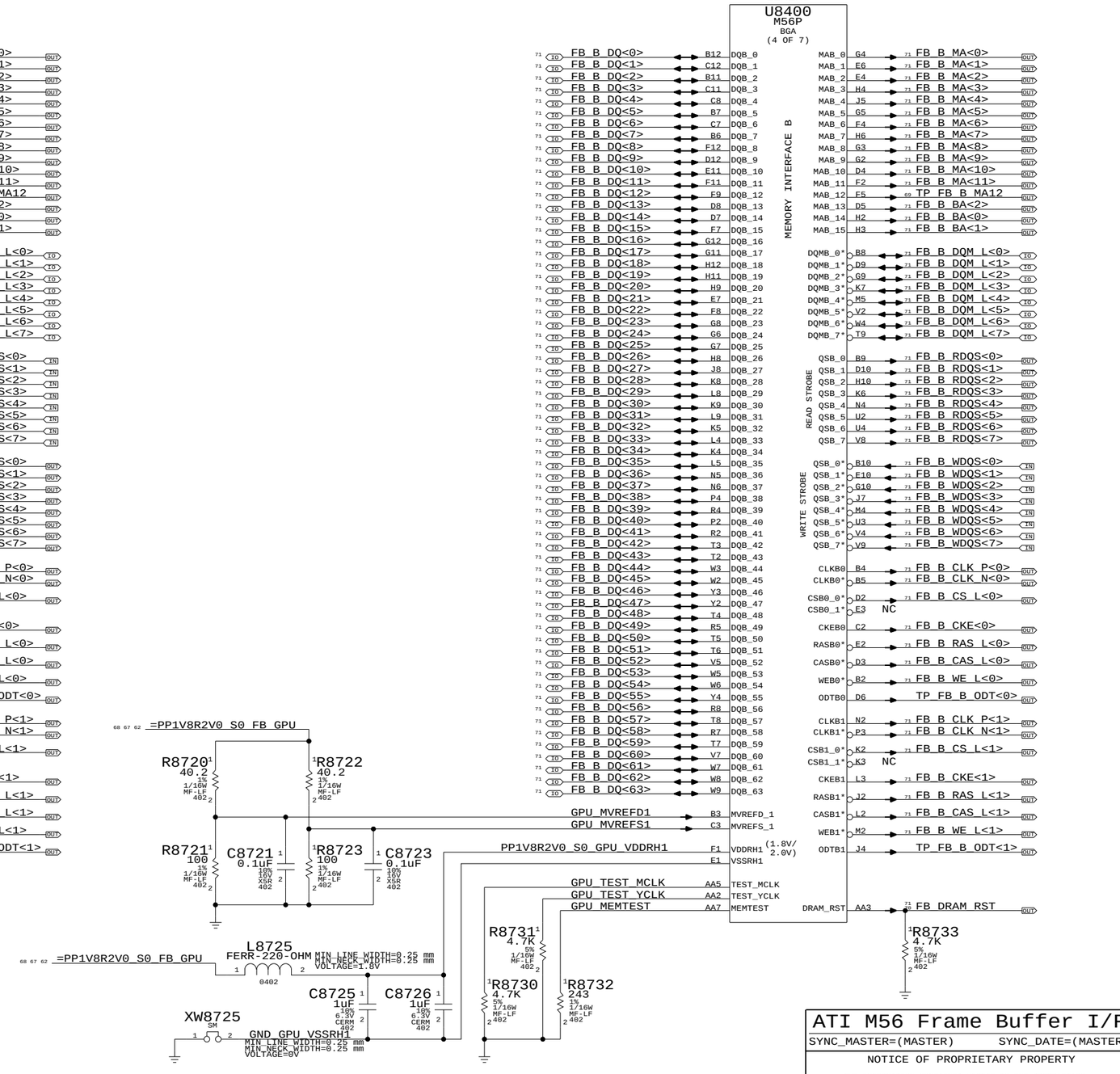
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





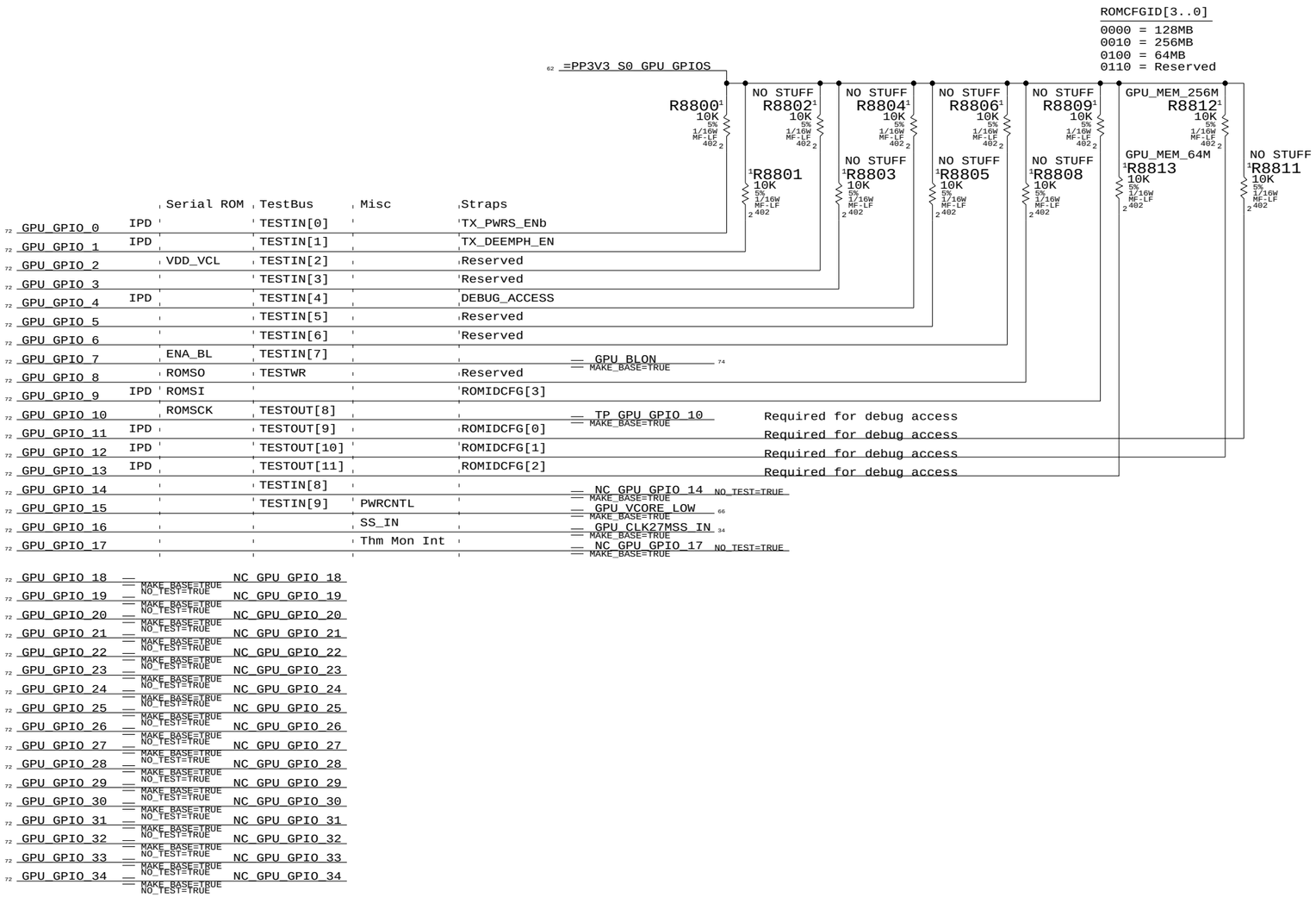
ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	87	103



Renamed signals

34 GPU_CLK27M — GPU_XTALIN 72

Unused signals

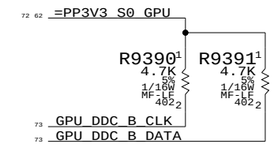
NC_GPU_XTALOUT — GPU_XTALOUT 72
NC_ATI_ROMCS_L — TP_ATI_ROMCS_L 72
NC_FB_A_MA12 — TP_FB_A_MA12 68
NC_FB_B_MA12 — TP_FB_B_MA12 68
NC_GPU_GENERICA — GPU_GENERICA 72
NC_GPU_GENERICB — GPU_GENERICB 72
NC_GPU_GENERICC — GPU_GENERICC 72
NC_GPU_VGA_R — GPU_VGA_R 73
NC_GPU_VGA_G — GPU_VGA_G 73
NC_GPU_VGA_B — GPU_VGA_B 73
NC_GPU_VGA_HSYNC — GPU_VGA_HSYNC 73
NC_GPU_VGA_VSYNC — GPU_VGA_VSYNC 73
NC_GPU_R2 — GPU_R2 73
NC_GPU_G2 — GPU_G2 73
NC_GPU_B2 — GPU_B2 73
NC_LVDS_U_DATAP<3> — LVDS_U_DATA_P<3> 73
NC_LVDS_U_DATAN<3> — LVDS_U_DATA_N<3> 73
NC_LVDS_L_DATAP<3> — LVDS_L_DATA_P<3> 73
NC_LVDS_L_DATAN<3> — LVDS_L_DATA_N<3> 73
NC_ATI_DVPCLK — ATI_DVPCLK 72
NC_ATI_DVPCNTL<2..0> — ATI_DVPCNTL<2..0> 72
NC_ATI_DVPDATA<15..0> — ATI_DVPDATA<15..0> 72

MAKE_BASE=TRUE NO_TEST=TRUE

Required for debug access

TP_ATI_DVPDATA<23..16> — ATI_DVPDATA<23..16> 72

Also required: GPIO10 - GPIO13



GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

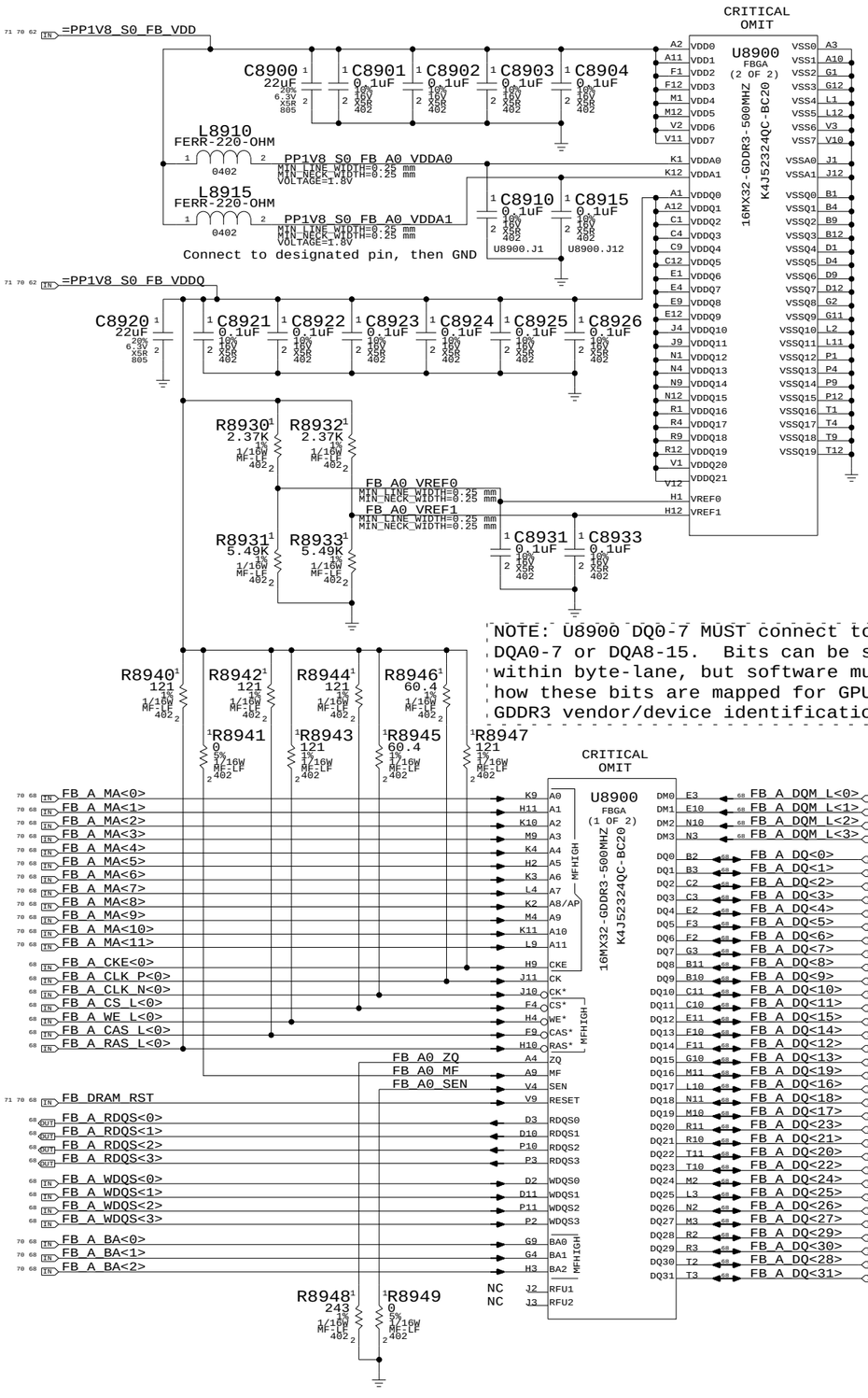
SCALE	SHT	OF
NONE	88	103

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

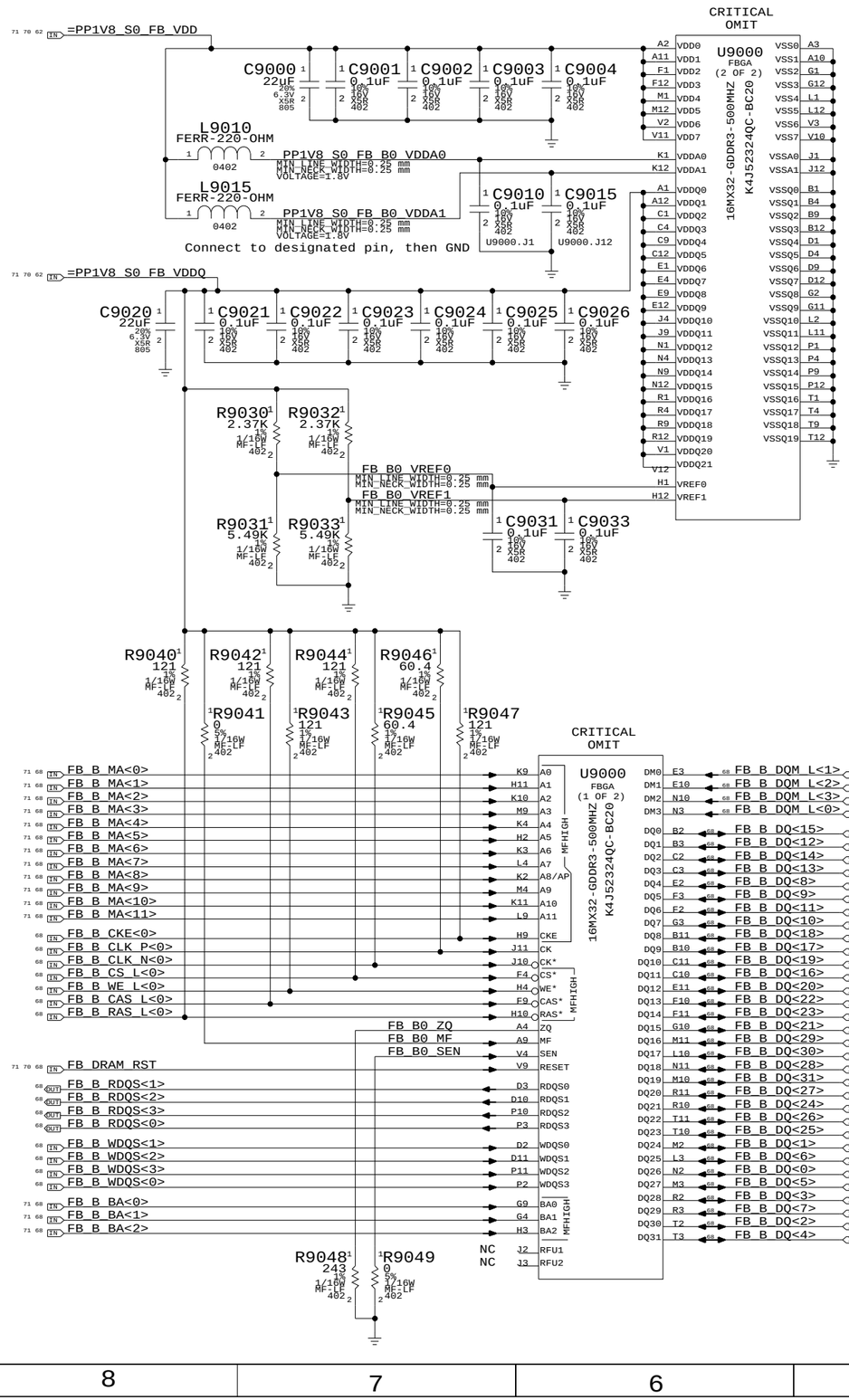


GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 89 OF 103	



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

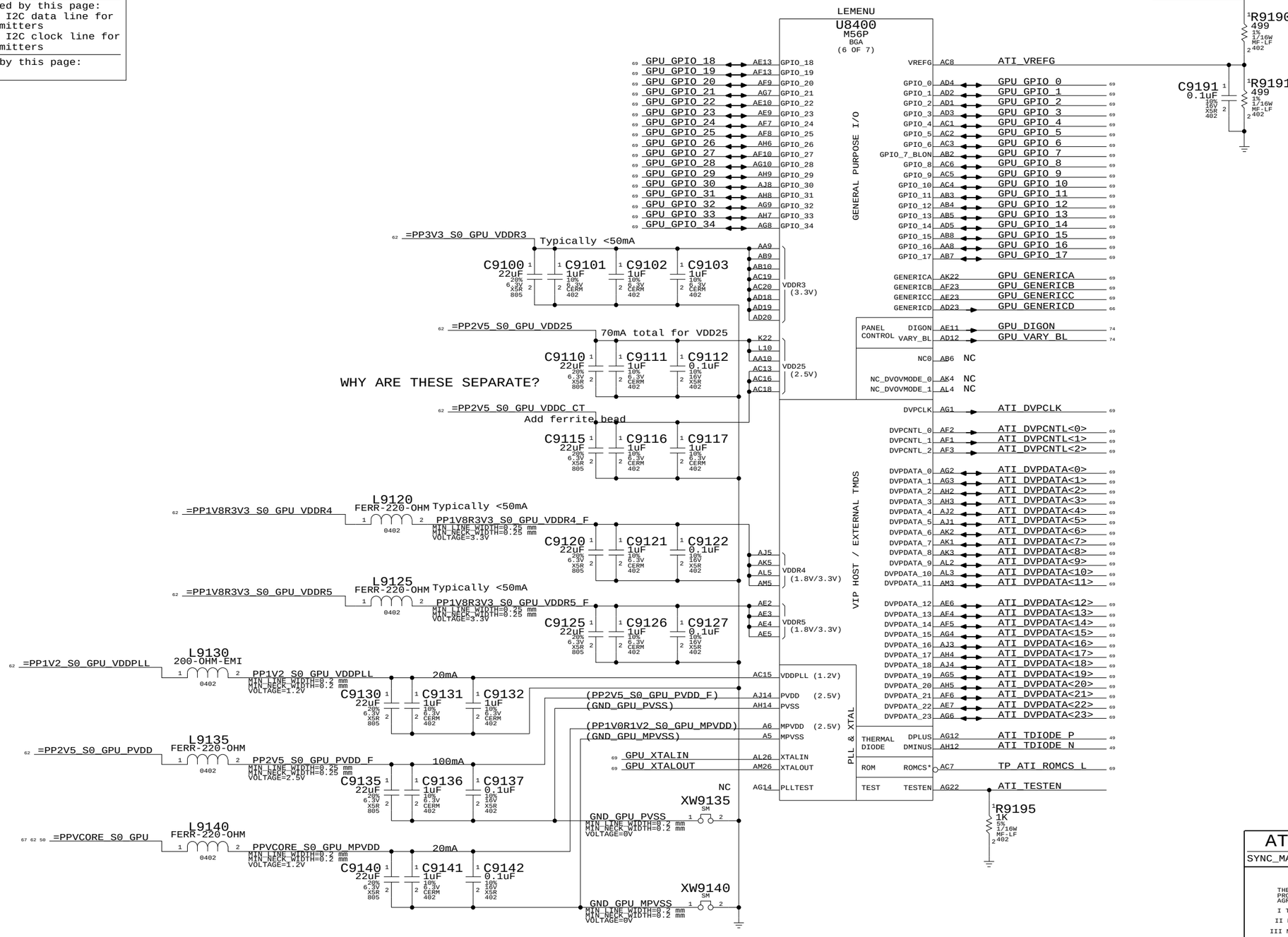
SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE	SHT	OF
NONE	90	103

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 91 OF 103	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

62 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 XW9300 SM — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9300 22uF 20% 6.3V X5R 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 XW9305 SM — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
C9305 22uF 20% 6.3V X5R 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 XW9310 SM — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
C9310 22uF 20% 6.3V X5R 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

XW9314 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22uF 20% 6.3V X5R 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 XW9320 SM — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
C9320 22uF 20% 6.3V X5R 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 XW9324 SM — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9325 22uF 20% 6.3V X5R 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

XW9324 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

L9330 FERR-220-OHM 0402 XW9330 SM — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9330 22uF 20% 6.3V X5R 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
C9340 22uF 20% 6.3V X5R 805; C9345 22uF 20% 6.3V X5R 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

ATI_RSET 73
ATI_R2SET 73
R9350 499 1% 1/16W MF-LF 402
R9351 715 1% 1/16W MF-LF 402

LEMENU
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
AM8 TPVDD (2.5V)
AL8 TPVSS
AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
AJ7, AK7, AK8, AL7, AM7 TXVSSR
AL25, AM25 AVDD (2.5V)
AJ24, AK25 AVSS
AK23 AVSSQ
AM23 VDD1DI (2.5V)
AL23 VSS1DI

DAC (CRT)
73 ATI_RSET AL22 RSET

DAC2 (TV/CRT2)
AL16, AM16 A2VDD (2.5V)
AL17, AM17 A2VSS
NC AL14 NC_A2VDDQ
AK13 A2VSSQ
AJ16 VDD2DI (2.5V)
AJ17 VSS2DI
73 ATI_R2SET AK14 R2SET

LVDS
AE19 LPVDD (2.5V)
AE18 LPVSS
AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
75 INT GPU_HPD AF11 HPD1

TMDS outputs:
TXCP AM9 — 76 75 74 TMDS_CLK_P
TXCM AL9 — 76 75 74 TMDS_CLK_N
TX0P AL10 — 76 75 74 TMDS_DATA_P<0>
TX0M AK10 — 76 75 74 TMDS_DATA_N<0>
TX1P AM11 — 76 75 74 TMDS_DATA_P<1>
TX1M AL11 — 76 75 74 TMDS_DATA_N<1>
TX2P AM12 — 76 75 74 TMDS_DATA_P<2>
TX2M AL12 — 76 75 74 TMDS_DATA_N<2>
TX3P AJ9 — 76 75 74 TMDS_DATA_P<3>
TX3M AK9 — 76 75 74 TMDS_DATA_N<3>
TX4P AJ11 — 76 75 74 TMDS_DATA_P<4>
TX4M AK11 — 76 75 74 TMDS_DATA_N<4>
TX5P AJ12 — 76 75 74 TMDS_DATA_P<5>
TX5M AK12 — 76 75 74 TMDS_DATA_N<5>

DAC (CRT) outputs:
R AK24 — 69 GPU_VGA_R
G AM24 — 69 GPU_VGA_G
B AL24 — 69 GPU_VGA_B
HSYNC AJ23 — 69 GPU_VGA_HSYNC
VSYNC AJ22 — 69 GPU_VGA_VSYNC

DAC2 (TV/CRT2) outputs:
R2 AK15 — 69 GPU_R2
G2 AM15 — 69 GPU_G2
B2 AL15 — 69 GPU_B2
H2SYNC AE15 — 78 GPU_H2SYNC
V2SYNC AG15 — 78 GPU_V2SYNC
Y AJ15 — 78 74 GPU_TV_Y
C AJ13 — 78 74 GPU_TV_C
COMP AH15 — 78 74 GPU_TV_COMP

LVDS outputs:
TXCLK_UP AJ21 — 74 LVDS_U_CLK_P
TXCLK_UN AK21 — 74 LVDS_U_CLK_N
TXOUT_U0P AG18 — 74 LVDS_U_DATA_P<0>
TXOUT_U0N AH18 — 74 LVDS_U_DATA_N<0>
TXOUT_U1P AK20 — 74 LVDS_U_DATA_P<1>
TXOUT_U1N AJ20 — 74 LVDS_U_DATA_N<1>
TXOUT_U2P AG20 — 74 LVDS_U_DATA_P<2>
TXOUT_U2N AH20 — 74 LVDS_U_DATA_N<2>
TXOUT_U3P AH21 — 69 LVDS_U_DATA_P<3>
TXOUT_U3N AG21 — 69 LVDS_U_DATA_N<3>
TXCLK_LP AM18 — 74 LVDS_L_CLK_P
TXCLK_LN AL18 — 74 LVDS_L_CLK_N
TXOUT_L0P AL19 — 74 LVDS_L_DATA_P<0>
TXOUT_L0N AK19 — 74 LVDS_L_DATA_N<0>
TXOUT_L1P AM20 — 74 LVDS_L_DATA_P<1>
TXOUT_L1N AL20 — 74 LVDS_L_DATA_N<1>
TXOUT_L2P AM21 — 74 LVDS_L_DATA_P<2>
TXOUT_L2N AL21 — 74 LVDS_L_DATA_N<2>
TXOUT_L3P AJ18 — 69 LVDS_L_DATA_P<3>
TXOUT_L3N AK18 — 69 LVDS_L_DATA_N<3>

MONITOR IDENTIFICATION outputs:
DDC1CLK AH23 — 75 GPU_DDC_A_CLK (I/O)
DDC1DATA AH22 — 75 GPU_DDC_A_DATA (I/O)
DDC2CLK AG13 — 69 GPU_DDC_B_CLK (I/O)
DDC2DATA AH13 — 69 GPU_DDC_B_DATA (I/O)
DDC3CLK AF12 — 74 GPU_DDC_C_CLK (I/O)
DDC3DATA AE12 — 74 GPU_DDC_C_DATA (I/O)

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

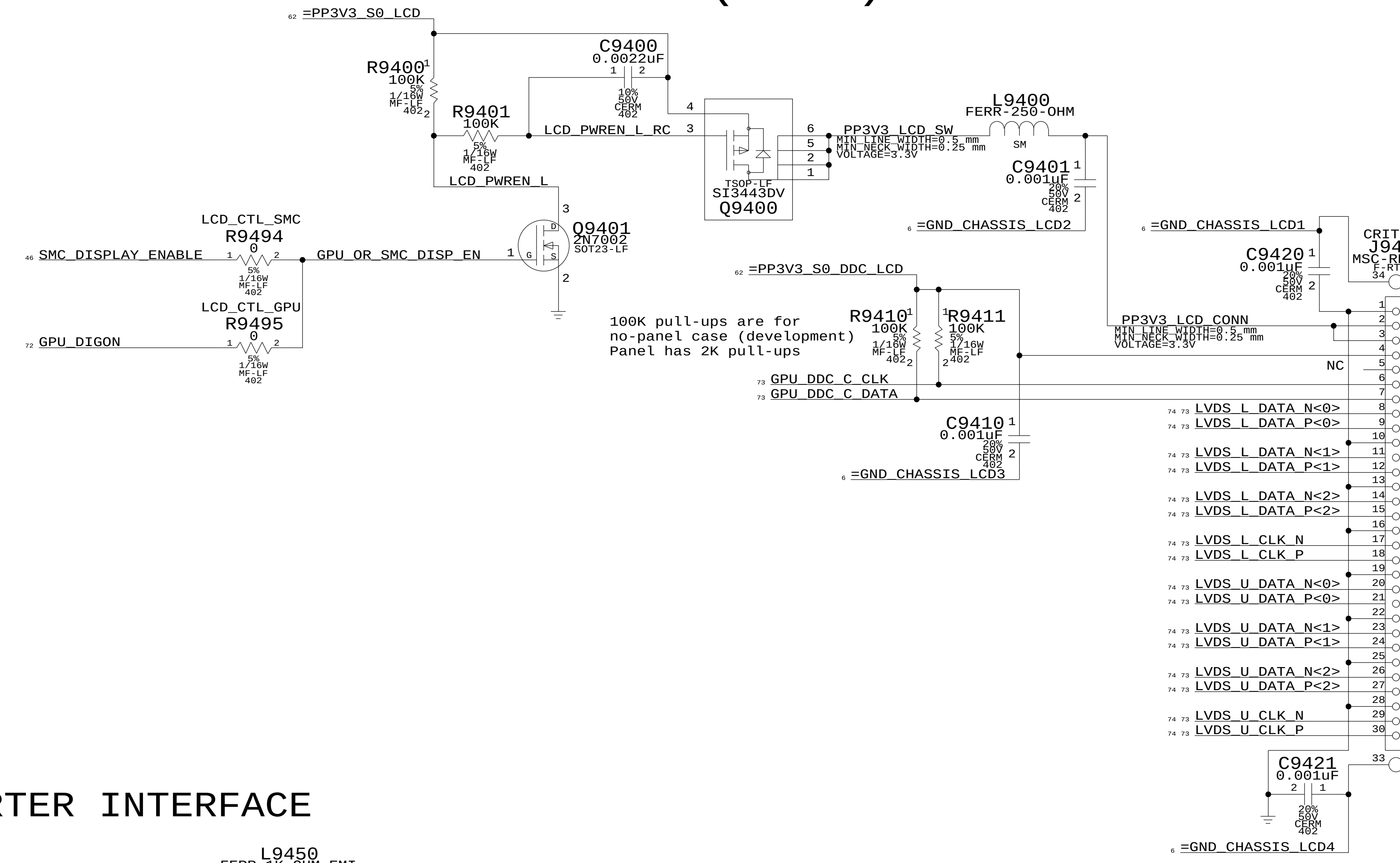
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 03

SCALE NONE | SHT 93 OF 103

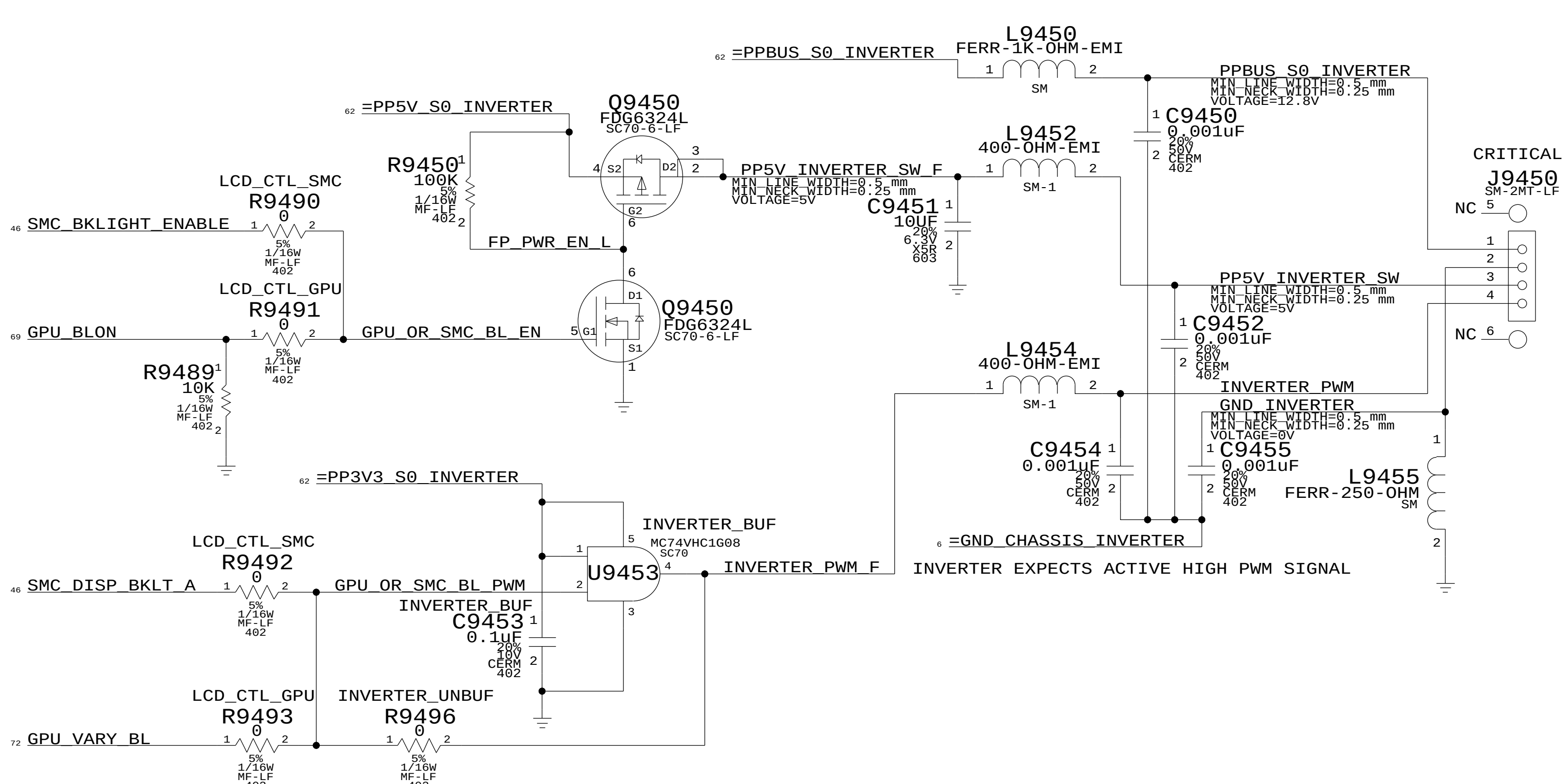
LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_TV_Y	73 75
	VGA	VGA	GPU_TV_C	73 75
	VGA	VGA	GPU_TV_COMP	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 74
	LVDS	LVDS	LVDS_U_CLK_N	73 74
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 74
	LVDS	LVDS	LVDS_L_CLK_P	73 74
	LVDS	LVDS	LVDS_L_CLK_N	73 74
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 74
	TMDS	TMDS	TMDS_CLK_P	73 75 76
	TMDS	TMDS	TMDS_CLK_N	73 75 76
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 76
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 76
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 76
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 76



=PP3V3_S0_LCD
R9400 100K 5% 1/16W MF-LF 402
C9400 0.0022uF 10% 50V CERM 402
R9401 100K 5% 1/16W MF-LF 402
LCD_PWREN_L_RC
LCD_PWREN_L
TSOP-LF SI3443DV Q9400
PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
L9400 FERR-250-OHM SM
C9401 0.001uF 20% 50V CERM 402
=GND_CHASSIS_LCD2
=GND_CHASSIS_LCD1
LCD_CTL_SMC
R9494 0
SMC_DISPLAY_ENABLE
GPU_OR_SMC_DISP_EN
Q9401 2N7002 SOT23-LF
LCD_CTL_GPU
R9495 0
GPU_DIGON
=PP3V3_S0_DDC_LCD
100K pull-ups are for
no-panel case (development)
Panel has 2K pull-ups
R9410 100K
R9411 100K
GPU_DDC_C_CLK
GPU_DDC_C_DATA
C9410 0.001uF
=GND_CHASSIS_LCD3
C9420 0.001uF
CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM
PP3V3_LCD_CONN
VOLTAGE=3.3V
NC
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_L_DATA_N<2>
LVDS_L_DATA_P<2>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<2>
LVDS_U_DATA_P<2>
LVDS_U_CLK_N
LVDS_U_CLK_P
C9421 0.001uF
=GND_CHASSIS_LCD4

INVERTER INTERFACE



=PPBUS_S0_INVERTER
L9450 FERR-1K-OHM-EMI SM
PPBUS_S0_INVERTER
VOLTAGE=12.6V
C9450 0.001uF
=PP5V_S0_INVERTER
Q9450 FDG6324L SC70-6-LF
R9450 100K
PP5V_INVERTER_SW_F
VOLTAGE=5V
L9452 400-OHM-EMI SM-1
C9451 10UF 20% 6.3V X5R 603
LCD_CTL_SMC
R9490 0
SMC_BKLIGHT_ENABLE
FP_PWR_EN_L
CRITICAL
J9450 SM-2MT-LF
NC
LCD_CTL_GPU
R9491 0
GPU_BLON
GPU_OR_SMC_BL_EN
PP5V_INVERTER_SW
C9452 0.001uF
R9489 10K
L9454 400-OHM-EMI SM-1
INVERTER_PWM
GND_INVERTER
VOLTAGE=0V
C9454 0.001uF
C9455 0.001uF
L9455 FERR-250-OHM SM
=PP3V3_S0_INVERTER
INVERTER_BUF
MC74VHC1G08 SC70
U9453
=GND_CHASSIS_INVERTER
LCD_CTL_SMC
R9492 0
SMC_DISP_BKLT_A
GPU_OR_SMC_BL_PWM
INVERTER_PWM_F
INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL
INVERTER_BUF
C9453 0.1uF 20% 10V CERM 402
LCD_CTL_GPU
R9493 0
GPU_VARY_BL
INVERTER_UNBUF
R9496 0

Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

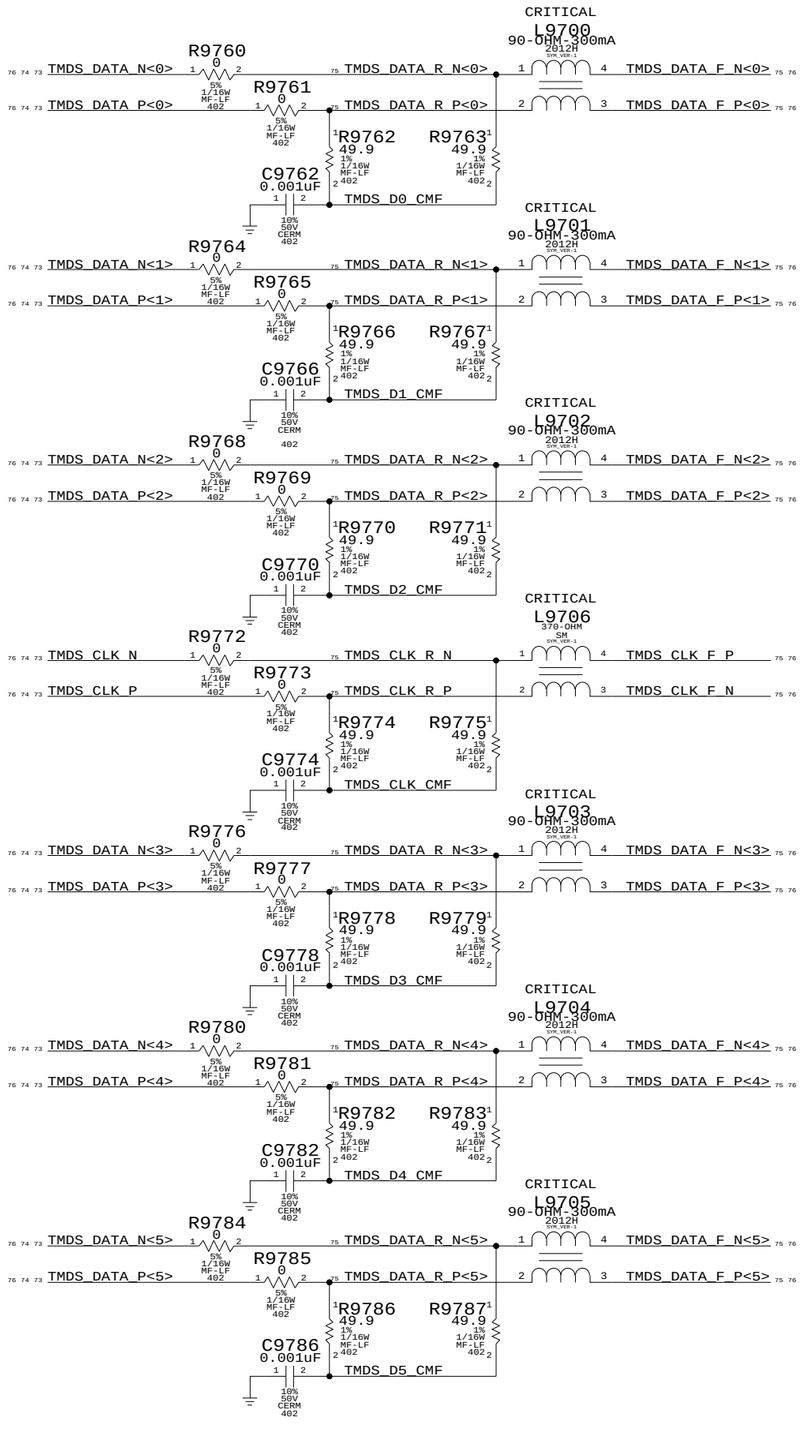
NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

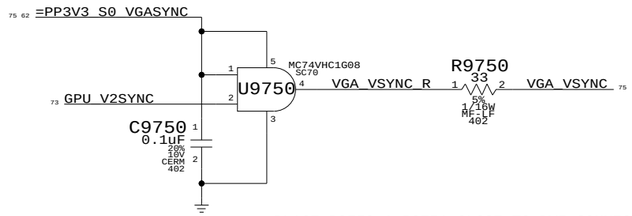
SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 94	OF 103

TMDS Filtering

Place series R's close to GPU, other parts near connector.



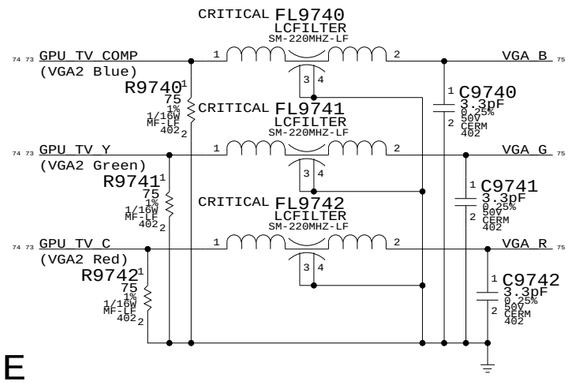
VGA SYNC BUFFERS



PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

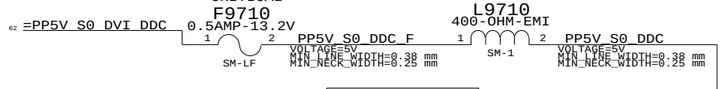
NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDS_DATA_F_N<5..0>

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

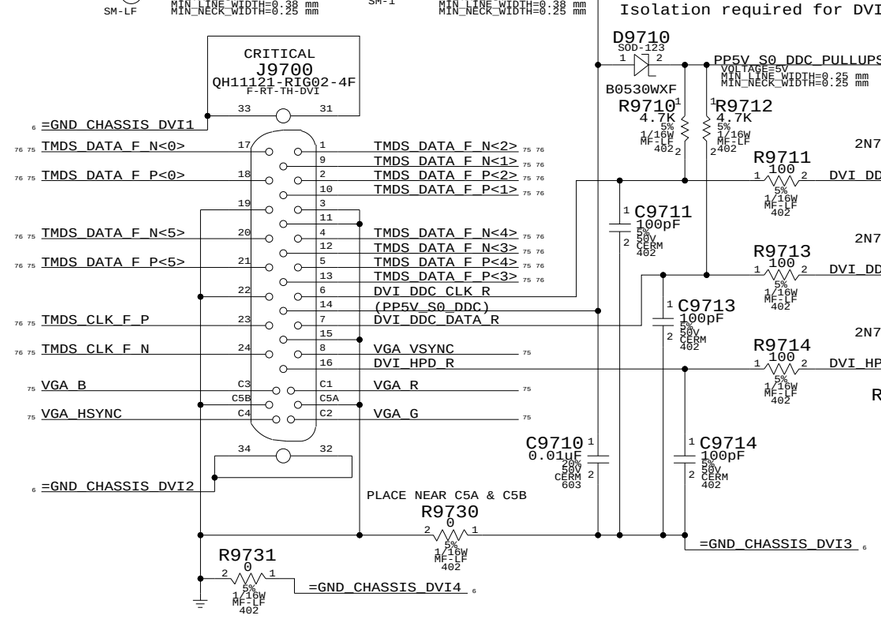


DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



Isolation required for DVI power switch



3V LEVEL SHIFTERS

External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03
SCALE: NONE	SHT 97 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12 47
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 56
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	56
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 76
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 76
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 56
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	56

	MEM_CLK	MEM_70D
	MEM_CTRL	MEM_45S
	MEM_CMD	MEM_55S
	MEM_DATA	MEM_55S
	MEM_DQS	MEM_85D
	FB_CLK	FB_75D
	FB_ADCTRL	FB_35S_TO_55S
	FB_ADCTRL	FB_55S
	FB_DATA	FB_40S
	LVDS	LVDS_100D
	TMDS	TMDS_100D
	VGA	VGA_75S
	PCIE	PCIE_100D
	DMI	DMI_100D
	SATA	SATA_100D
	IDE	IDE_55S
	USB2	USB2_90D
	FNET	FNET_100D
	FW	FW_110D
	SMB	SMB_55S
	SPI	SPI_55S
	CLK_FSB	CLK_FSB_100D
	CLK_PCIE	CLK_PCIE_100D
	CLK_MED	CLK_MED_55S
	CLK_SLOW	CLK_SLOW_55S

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 44
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	03

SCALE	SHT	OF
NONE	103	103