

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# K36 MLB SCHEMATIC

REFERENCED FROM M70  
8/9/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
?		?	?	DATE	DATE
				?	?

Page	(.csa)	Contents	Sync	Date
1	1	Table of Contents	RX	09/05/2006
2	2	System Block Diagram	RX	05/11/2006
3	3	Power Block Diagram	MK	06/30/2005
4	4	CONFIGURATION OPTIONS	RX	07/18/2005
5	5	Revision History	RX	N/A
6	7	FUNC TEST 1 OF 2	RX	07/25/2005
7	8	Power Aliases	MK	06/15/2006
8	9	SIGNAL ALIAS /RESET	RX	07/17/2006
9	10	CPU FSB	RX	11/12/2006
10	11	CPU Power & Ground	RX	T9_MLB_NOME
11	12	CPU Decoupling & VID	RX	MSARWAR
12	13	CPU ITP700FLEX DEBUG	ES	MASTER
13	14	NB CPU Interface	ES	T9_MLB
14	15	NB PEG / Video Interfaces	ES	T9_MLB
15	16	NB Misc Interfaces	ES	T9_MLB
16	17	NB DDR2 Interfaces	ES	T9_MLB
17	18	NB Power 1	ES	T9_MLB
18	19	NB Power 2	ES	T9_MLB
19	20	NB Grounds	ES	T9_MLB
20	21	NB Standard Decoupling	ES	WFERRY
21	22	NB Graphics Decoupling	ES	WFERRY
22	23	SB Enet, Disk, FSB, LPC	RX	T9_MLB
23	24	SB PCI, PCIe, DMI, USB	RX	T9_MLB
24	25	SB Pwr Mgt, GPIO, Clink	RX	T9_MLB
25	26	SB Power & Ground	RX	T9_MLB
26	27	SB Decoupling	RX	WFERRY
27	28	SB Misc	RX	NB
28	29	Clock (CK505)	DK	DSIMON
29	30	Clock Termination	DK	DSIMON-WF
30	31	DDR2 SO-DIMM Connector A	LD	MEMORY
31	32	DDR2 SO-DIMM Connector B	LD	MEMORY
32	33	Memory Active Termination	LD	MEMORY
33	34		LT	ENET
34	37	Ethernet (Yukon)	LT	USB
35	38	Yukon Power Control	LT	USB
36	39	ETHERNET CONNECTOR	LT	USB
37	40	FIREWIRE CONTROLLER	LT	ENET
38	43	FIREWIRE PORT	LT	GPU
39	44	PATA CONNECTOR	DK	GPU
40	45	SATA CONNECTOR	RX	GPU
41	46	USB EXTERNAL CONNECTORS	LT	USB
42	47	CONNECTOR MISC	LT	USB
43	48	IR CONTROLLER & BT INTERFACE	LT	USB
44	49	SMC	LD	T9_MLB
45	50	SMC SUPPORT	LD	GPU

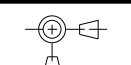
Page	(.csa)	Contents	Sync	Date
46	51	LPC+ Debug Connector	LD	WFERRY
47	52	SMBUS CONNECTIONS	LD	WFERRY
48	53	CPU Current & Voltage Sense	ES	GPU
49	55	TEMPERATURE SENSE	ES	GPU
50	56	Fan	LD	ENET
51	59	SMS	MK	SMC
52	61	SPI ROMs	RX	WFERRY
53	62	AUDIO: CODEC	RX	M70AUDIO
54	66	AUDIO: SPEAKER AMP	RX	M70AUDIO
55	67	AUDIO: JACK	RX	M70AUDIO
56	68	AUDIO: JACK TRANSLATORS	RX	M70AUDIO
57	69	DC-In & Battery Connectors	RX	POWER
58	70	S0 FETS & Power Sequencing	MK	DSIMON-WF
59	71	IMVP6 CPU VCore Regulator	MK	POWER
60	72	Render VCore Supplies	MK	GPU
61	73	1.5V / 1.05V Supplies	MK	POWER
62	75	1.8V/0.9V Supplies	MK	POWER
63	76	5V/3.3V Supplies	MK	POWER
64	77	3.42V/1.25V Switcher	MK	ENET
65	78	S3 FET & S3/S5 Control	MK	DSIMON-WF
66	79	PBUS Supply/Battery Charger	MK	SMC
67	90	INVERTER, LVDS, TMS	MK	GPU
68	92	EXTERNAL TMS	ES	GRAPHIC
69	94	MINI-DVI CONNECTOR	ES	EUGENE
70	100	CPU/FSB Constraints	ES	WFERRY
71	101	NB Constraints	RX	WFERRY
72	102	Memory Constraints	ES	WFERRY
73	103	SB Constraints (1 of 2)	LD	WFERRY
74	104	SB Constraints (2 of 2)	RX	WFERRY
75	105	Clock Constraints	RX	WFERRY
76	106	FireWire & SMC Constraints	DK	WFERRY

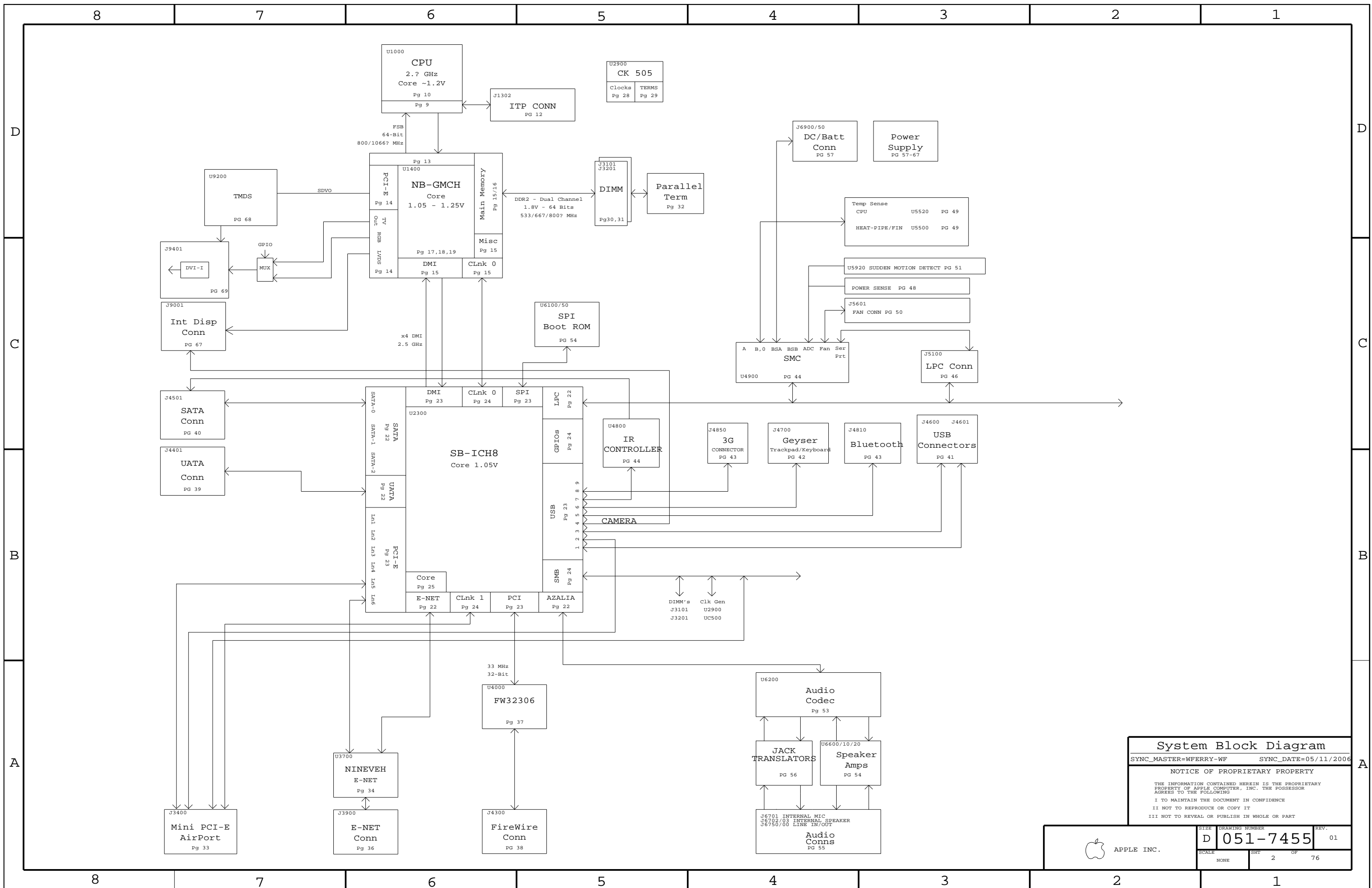
K36 EE DRIS:  
RX-RAYMOND XU  
DK-DINESH KUMAR  
RC-RAY CHANG  
MK-MARC KLINGELHOFER  
LT-LAWRENCE TAN  
LD-LINDA DUNN  
MM-MARY(YUAN) MA

## DVT BUILD

### Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7455	1	SCHEM, MLB, K36	SCH	CRITICAL	
820-2279	1	PCBF, MLB, K36	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
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DO NOT SCALE DRAWING				III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
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		QA APPD <input type="checkbox"/>	DESIGNER <input type="checkbox"/>	TITLE <input type="checkbox"/>	RELEASE <input type="checkbox"/>
		MATERIAL/FINISH NOTED AS APPLICABLE	SCALE NONE	SIZE D	DRAWING NUMBER <b>051-7455</b>
				REV. 01	SHEET 1 OF 76



**System Block Diagram**

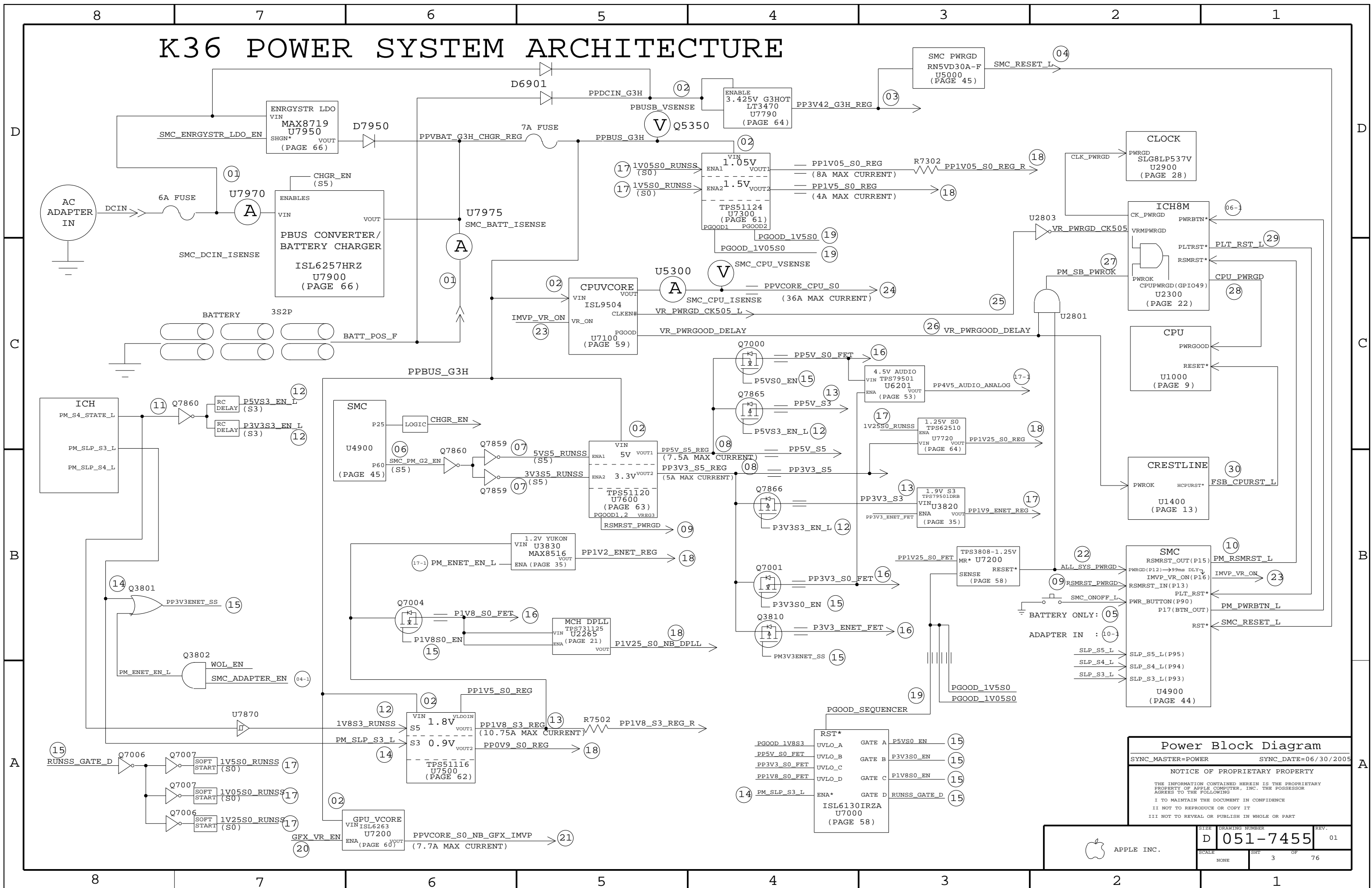
SYNC\_MASTER=WFERRY-WF SYNC\_DATE=05/11/2006

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APPLE INC.	SIZE DRAWING NUMBER <b>D 051-7455</b>	REV. 01
	SCALE NONE	SHEET 2 OF 76

# K36 POWER SYSTEM ARCHITECTURE



**Power Block Diagram**  
 SYNC\_MASTER=POWER SYNC\_DATE=06/30/2005

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Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

BOM OPTION

BOMOPTION	K36 GOOD 630-9104 EVT	K36 BETTER 630-9105 EVT	K36 BEST 630-9106 EVT	M70 GOOD 630-7935 CONCEPT
COMMON	V	V	V	V
ALTERNATE	V	V	V	V
ARB_ONLY				
K36	V	V	V	V
LPCPLUS	V	V	V	V
INVERTER_BUF	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V
INVERTER_UNBUF	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V
ITP	V	V	V	V
NO_REBOOT_MODE				
NBCFG_DMI_REVERSE				
NBCFG_DMI_X2				
NBCFG_DYN_ODT_DISABLE				
NBCFG_PEG_REVERSE				
NBCFG_SDVO_AND_PCIE				
GOOD	V			V
BETTER		V		V
BEST			V	V
K36_PGM	V	V	V	V
YUKON_EC				V
YUKON_ULTRA	V	V	V	V
NORMAL	V	V		V
FANCY			V	V
STANDOFF	V	V	V	V
ODD_PWR_CORE	V	V	V	V
ODD_PWR_RESUME				V
ISL6126	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	
ISL6130	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

MLB STACKUP		
LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

BOM TABLE FOR HF POSCAPS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0147	4	HF VERSION OF 128S0057	C4610,C4611,C6830,C6831	CRITICAL	K36
128S0164	3	HF VERSION OF 128S0073	C2130,C2716,C7543	CRITICAL	K36
128S0148	1	HF VERSION OF 128S0085	C6605	CRITICAL	K36
128S0169	3	HF VERSION OF 128S0111	C7220,C7352,C7542	CRITICAL	K36
128S0160	2	HF VERSION OF 128S0113	C2173,C2700	CRITICAL	K36
128S0150	6	HF VERSION OF 128S0115	C6204,C6205,C7651,C7652,C7691,C7692	CRITICAL	K36
128S0157	1	HF VERSION OF 128S0122	C2220	CRITICAL	K36
128S0162	1	HF VERSION OF 128S0123	C2140	CRITICAL	K36
128S0135	2	HF VERSION OF 128S0129	C6601,C6603	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3463	1	IC,MDC,SR,E1.2.GG,800PFB,4M,BGA	U1000	CRITICAL	GOOD
337S3500	1	IC,MDC,SR,GG.2.2G,800PFB,4M,BGA	U1000	CRITICAL	BETTER
337S3500	1	IC,MDC,SR,GG.2.2G,800PFB,4M,BGA	U1000	CRITICAL	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0448	1	IC,CRESTLINE,GM965,667	U1400	CRITICAL	K36
338S0434	1	IC,ICHS,BGA	U2300	CRITICAL	K36
516-0162	2	IN-LINE SOD1MM CONNECTOR	J3101,J3201	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2196	1	IC,16MBIT 8PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	K36_PGM
341S2060	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	K36_PGM
341S2198	1	IC,SMC,H58/2116	U4900	CRITICAL	K36_PGM
341S2093	1	IC,CYPRSS,CY7C63833,ENCORE_II,USB_CNTR	U4800	CRITICAL	K36_PGM

LOCKED BOOTROM PN 341S2197

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:Z55	CRITICAL	GOOD
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:Z56	CRITICAL	BETTER
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:Z57	CRITICAL	BEST

CONFIGURATION OPTIONS

SYNC\_MASTER=SMC SYNC\_DATE=07/18/2005

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	SHT	OF	REV.
NONE	4	76	

Revision History

M70 PROTO TO EVT CHANGES

- WAKE-ON-WIRELESS SUPPORT - RADAR: 4954357
- ADD ISOLATION BUFFER FOR ODD\_RESET\_L SIGNAL...
- ADD 270K PULL-DOWN RESISTOR ON HTPLG - RADAR: 4888755
- LOWER RDS(ON) MOSFET (FDC606P - APN: 376S0552) FOR ODD AND LCD POWER - RADAR: TBD
- HIGH-PRECISION 0.1% RESISTORS TO INCREASE OUTPUT VOLTAGE REGULATION (5V, 3.3V, PBUS\_LDO) ACCURACY - RADAR:4972500
- FIX LINDA CARD POWER ALIAS (NEED TO CONNECT TO PP3V42\_G3HOT INSTEAD OF PP3V3\_S5) - RADAR: 4927858
- FIX MOJO-CARD SMC TX, RX REVERSAL - RADAR: 4910888
- NO STUFF 3G CONNECTOR CIRCUITRY
- CHANGE BOM STUFFING TO SPEED UP PORT POWER SHUT-OFF RESPONSE TIME DURING ACTIVE LATE-VG EVENT (RADAR: 4985252)
- CHANGE BOM STUFFING TO ENABLE ON-BOARD MICROPHONE CONNECTOR (M42/M42A SOLUTION) INSTEAD OF ROUTING MICROPHONE THROUGH LVDS CABLE
- CHANGE LOAD CAP STUFFING OPTION FOR RTC AND ETHERNET CRYSTALS TO MEET 5XESR (-R) REQUIREMENT
- CHANGE 10UF, 16V CPU VCORE CAPS TO 10UF, 6.3V CAPS - RADAR: 4952553
- MOVE SMC RESET BUTTON PAD TO TOP SIDE OF MLB - RADAR: 4920913
- MODIFY FIREWIRE CONNECTOR SYMBOL TO SUPPORT MINI-DVI CONNECTOR WITH TAB
- TEST POINT MOVEMENTS REQUESTED BY ICT AND MAC-1 GROUPS - RADAR: 4924481

M70 EVT TO DVT CHANGES

3/5/2007
CSA PAGE 8:
- 4954357 ADD =PP3V3\_S3\_AIRPORT\_AUX BACK TO PP3V3\_S3 ALIAS.
CSA PAGE 34:
- 4954357 BREAK OUT =PP3V3\_S3\_AIRPORT\_AUX(J3400.PIN 24) FROM PP3V3\_S3\_AP\_AUX AGAIN.
- 4954357 MOVE C3409 AND C3410 FROM PP3V3\_S3\_AP\_AUX RAIL TO =PP3V3\_S3\_AIRPORT\_AUX RAIL.
CSA PAGE 49:
- 5040728 STUFF C9421 FOR EMI.
CSA PAGE 62,66,67,68:
- SYNC FROM AUDIO TEAM.
CSA PAGE 94:
- 4996074 SWAP PIN 2 AND PIN 3 OF MIC CONNECTOR, BACK TO M42 PIN OUT.
CSA PAGE 94:
- 5029811 CHANGE Q7940 FROM 376S0326 TO 376S0558.

3/8/2007
CSA PAGE 22:
- 4996074 CHANGE L2205 TO R2205(1000HM,5%,1/10W,0603).
CSA PAGE 25:
- 4924443 CHANGE R2514 FROM 100K PULL-DOWN TO 10K PULL-UP TO 3.3V\_S5.
CSA PAGE 77:
- 5040817 SYNC LP25V REGULATOR CIRCUIT FROM M82 CHANGE R AND C TO Q402 CHANGE =PP3V3\_S5\_P1V25S0 TO =PP3V3\_S5\_1V25S0,
- C172 FROM 100UF TO 100UF C172B FROM 2UF TO 1000PF,
- AND REVERT REFERENCE DESIGNATORS. (CHANGE FROM TPS62510 TO LTC3412A)

3/12/2007
CSA PAGE 25:
- 4924443 CHANGE R2514 FROM 100K PULL-UP TO 47K PULL-UP.
CSA PAGE 45:
- UPDATE SYMBOL FOR J4501.
CSA PAGE 62,66,67,68:
- SYNC FROM AUDIO TEAM.
CSA PAGE 94:
- 4996074 CHANGE R9469 FOR CRT\_TVO\_IREF FROM 1.3K TO 1.21K.

3/14/2007
CSA PAGE 47:
- ADD TEXT NOTE TO UPDATE J4700 FROM 516S0251 TO 516S0588 WHEN SYMBOL IS READY.
CSA PAGE 49:
- ADD TEXT NOTE TO UPDATE J6900 FROM 518S0287 TO 518S0526 WHEN SYMBOL IS READY.
CSA PAGE 90:
- DELETE LVDS\_VREFH AND LVDS\_VREFL TO GROUND TO FIX LVDS GLITCH.
CSA PAGE 94:
- ADD TEXT NOTE TO CHANGE L9404 FROM 155S0303 TO 155S0348 WHEN SYMBOL IS READY.

M70 DVT TO K36 CHANGES

6/29/2007
CSA PAGE 4:
- CHANGE GOOD CPU FROM 337S3471(1.8G) TO 337S3463(2.0G)
- CHANGE BETTER CPU FROM 337S3456(2.0G) TO 337S3464(2.2G)
- CHANGE BEST CPU FROM 337S3464(2.2G) TO 337S3465(2.4G)
- CHANGE NB FROM 338S0426(500M) TO 343S0448(667M)
- CHANGE NB FROM 338S0427 TO 338S0434.
CSA PAGE 16:
- DISCONNECT GFX\_VID<0> TO GND
- CONNECT GFX\_VID<0> TO GFX\_VID<3> ON NB
- ADD R1600 (0OHM, 0402) TO CONNECT GFX\_VID<4> TO GND.
CSA PAGE 22:
- 5282976 ADD C2207 (0.1UF, 0402)
- SIZING DOWN R2205 FROM 0603 TO 0402 FOR PLACEMENT.
- CHANGE GFX\_VID<1:4> TO GFX\_VID<0:3>
- CHANGE TRAPPING FROM 0010 ON GFX\_VID<1:4> TO 0001 ON GFX\_VID<0:3>.
CSA PAGE 39:
- CHANGE J3900 FROM 514S0143 TO 514-0443.
- EPII BOM
CSA PAGE 46:
- CHANGE 4600 FROM 353S1245 TO 353S1728.
- REMOVE MIN\_NECK\_WIDTH=0.3MM FROM PP5V\_S3\_USB2\_EXTR/A.
- ADD NOSTUFF R460 AND R461.
CSA PAGE 47:
- CHANGE 4700 FROM 516S0251 TO 516S0588.
CSA PAGE 48:
- CHANGE 4800 FROM 518S0287 TO 518S0526.
- REPLACE BATTERY INTERFACE CIRCUIT WITH THE ONE ON M42B ESTAR.
CSA PAGE 94:
- 5040728 CHANGE L9404 FROM 155S0303 TO 155S0348.

7/5/2006
CSA PAGE 4:
- REPLACE ALL M70 WITH K36 (TEXT, BOM OPTIONS, 630 NUMBERS).
CSA PAGE 21:
- CHANGE C2173 FROM 128S0051 TO 128S0113 PER CE.
CSA PAGE 22:
- CHANGE C2700 FROM 128S0051 TO 128S0113 PER CE.
CSA PAGE 28:
- CHANGE 2800 FROM 518S0487 TO 518S0519.
CSA PAGE 46:
- REMOVE R4660 AND R4601 (U4675 BYPASS RESISTORS).
CSA PAGE 48:
- CHANGE 4810 FROM 518S0369 TO 518S0521.
CSA PAGE 48:
- CHANGE 48500 FROM M70 EMC1033 CIRCUIT TO M71 EMC1043 CIRCUIT.
- J550 CHANGES FROM 2PIN TO 4PIN.
CSA PAGE 55:
- CHANGE J5601 FROM 518S0369 TO 518S0521.
CSA PAGE 56:
- CHANGE 56702 FROM 518S0487 TO 518S0519.
- CHANGE 56703 FROM 518S0369 TO 518S0521.
CSA PAGE 59:
- CHANGE J9000 FROM 518S0369 TO 518S0521.

7/6/2006
CSA PAGE 8:
- REMOVE NO\_TEST=TRUE FOR 1V8S3\_COMP, 1V8S3\_FSET, 3V3S5\_COMP, 3V3S5\_FSET, 1V0S50\_COMP, 1V0S50\_FSET, 1MV6P\_RBIAS, 1MV6P\_COMP, 5V3S5\_RUNSS, 1V5S0\_RUNSS.
- ADD FUNC TEST=TRUE FOR TRM\_INSTACK\_P7N.
- ADD FUNC TEST=TRUE FOR PP1V05\_S0\_P.
CSA PAGE 9:
- REMOVE ALIASES FOR GND CHASSIS\_AUDIO\_SPKRCONN,GND\_CHASSIS\_AUDIO\_SHIELD1,GND\_CHASSIS\_AUDIO\_SHIELD2,GND\_CHASSIS\_AUDIO\_SHIELD3,MIC\_SHIELD\_LVDS\_R,MIC\_SHLD\_CONN.
- REMOVE ALIAS FOR =FWPWR\_PBRON
- ADD SPN ALIASES FOR TP\_CK505\_SRC7\_N/P.
- ADD SPN ALIASES FOR CK505\_PCT2/4\_CLK.
CSA PAGE 11:
- REMOVE R1290 TO R1296 ON CPU\_VID<0:6>.
CSA PAGE 11:
- DELETE TEXT NOTE AND WITH RESET BUTTON.
CSA PAGE 15:
- RENAME LVDS\_VREFH/L TO TP\_LVDS\_VREFH/L.
CSA PAGE 59:
- Add L2592 and R2596 FOR 10K PU ON GPIO6 AND GPIO17(EXTGPU\_RST\_L).
- CHANGE R2514 TO 100K.
CSA PAGE 59:
- CHANGE L2902 AND L2903 FROM 155S0302 TO 0OHM R2906 AND R2907.
- NOSTUFF C2907, C2910, C2914, C2911, C2914.
- CHANGE R2900, R2901 FROM 2.2OHM TO 0OHM.
- CHANGE R2902 FROM 10HM TO 0OHM.
CSA PAGE 44:
- REMOVE TEXT NOTE WILL CHANGE TO 606P.
CSA PAGE 62:
- RE-DRAW CPU VOLTAGE SENSE RC FILTERING.
CSA PAGE 62:
- RE-CONNECTED /SHDN INPUT OF U6801 SO THAT IT'S CONTROLLED BY U6200 PORTA VREF. - DISCONNECTED GPIO1 AND TERMINATED IT WITH A 10K PULL DOWN.
- ADDED A NO STUFF PULL-UP TO CODEC DVDV AT GPIO1.
- ADDED SMALL 15PF COMPENSATION CAP. TO U6201 FEEDBACK NETWORK (C6224).
CSA PAGE 67:
- CHANGED ALL TRANSIENT SUPPRESSORS TO 6.8V/100PF DEVICES (WERE ORIGINALLY 8V/100PF DEVICES).
- ADDED L6771 AND L6773 TO MIC INPUT EMI FILTER.
- REMOVED DZ6772.
- ADDED R6740 NO STUFF.
CSA PAGE 68:
- CONNECTED MIC\_SHLD\_CONN TO GND\_CHASSIS\_AUDIO\_MIC THROUGH R6854.
- ADDED R6895 NO STUFF.
CSA PAGE 71:
- RENAME CPU\_VID\_R<6:0> TO CPU\_VID<6:0>.

7/10/2007
CSA PAGE 4:
- BOTH PART NUMBER CHANGES FROM 341S2085 TO 341S2196.
- SMC PART NUMBER CHANGES FROM 541S2088 TO 341S2198.
- UPDATE BEE CODES, Z55 FOR GOOD, Z56 FOR BETTER, Z57 FOR BEST.
CSA PAGE 8:
- ADD R4675 =PP3V3\_S3\_SMBUS\_SMC\_MGMT TO PP3V3\_S3.
CSA PAGE 19:
- ADD CRITICAL TO U2900.
- ADD CRITICAL TO U4401.
CSA PAGE 48:
- CHANGE U4675 FROM APN 353S1505 TO APN 353S1742. (SMALL PACKAGE)
- ADD R4676 & R4671. (USB BYPASS ROUTING).
CSA PAGE 49:
- REMOVE ALIAS FOR =SMC\_SMS\_INT TO SMC\_PG1 - SIGNAL SHOULD JUST BE CALLED SMC\_SMS\_INT.
- CHANGE R5077 FROM PULL-UP TO A PULL-DOWN RESISTOR AND NAME IT SMC\_SMS\_INT.
CSA PAGE 49:
- REMOVE CLK AND SMB\_ME\_DATA ON SOUTHRIDGE DISCONNECTED FROM SMB\_MGMT\_CLK AND SMB\_MGMT\_DATA FROM SMC.B
- THE 10K PULL-UP RESISTORS (R5230 AND R5231), AND STILL REMAIN CONNECTED TO PP3V3\_S3\_SMBUS\_SB\_ME AND STAY ON THE SB SIDE.
- SMC MANAGEMENT SMBUS CONNECTOR:
- ADD TWO NEW 10K PULL-UP RESISTOR (R5232 & R5233) TO =PP3V3\_S3\_SMBUS\_SMC\_MGMT.B
- THE PULL-UP RESISTORS SHOULD BE CONNECTED BETWEEN SMB\_MGMT\_CLK AND SMB\_MGMT\_DATA TO =I2C\_SMS\_SCL AND =I2C\_SMS\_SDA OF THE NEW ACCELEROMETER.
CSA PAGE 53:
- ADD 2ND SMS (U5930).
CSA PAGE 62:
- CHANGED C6210 FROM A CASE-5 10UF TANT CAP TO A SMA-LF 3.3UF TANT CAP.
- MADE NO TEST ATTRIBUTE VISIBLE FOR NET\_NCL\_VRP CONNECTED TO PIN 37 OF U6200.
CSA PAGE 67:
- REMOVED NO STUFF RESISTORS R6730, R6731, AND R6732. ALSO REMOVED L6774.
- STUFFED R6740.
- MADE DZ6702, DZ6703, DZ6704, DZ6705, DZ6752, DZ6753, DZ6754, DZ6755, DZ6770, DZ6771B CRITICAL.
CSA PAGE 68:
- NO STUFFED R6854
CSA PAGE 74:
- CHANGE R7208 FROM 8.66K TO 15.8K.

7/11/2007
CSA PAGE 9:
- CHANGE Z0901 AND Z0906 FROM 998-1178 TO 998-1186 (NON-PLATED).
CSA PAGE 11:
- STUFF C3110 AND C3111.
CSA PAGE 11:
- STUFF C3210 AND C3211.
CSA PAGE 39:
- UPDATE FB FOR FANCY RJ45 CONNECTOR, 514-0475.
CSA PAGE 59:
- UPDATE FB FOR FANCY RJ45 CONNECTOR, 514-0475.
CSA PAGE 59:
- REMOVE R5077 (BECOMES R5931).
CSA PAGE 59:
- ADD R5931 (WAS R5077 BEFORE), 10K PD ON SMC\_SMS\_INIT.
- STUFF U5930 (DIGITAL ACCELEROMETER) CIRCUIT.

7/12/2007
CSA PAGE 43:
- CHANGE J4300 FROM 514-0289 TO 514-0456 (SAME JEDEC).
- UPDATE BOM OPTION TABLE FOR J4300.
- NORMAL CHANGES FROM 514-0359 TO 514-0456, FANCY CHANGES FROM 514-0316 TO 514-0476.
CSA PAGE 45:
- CHANGE J4600 AND J4601 FROM 514-0288 TO 514-0457 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J4600 AND J4601.
- NORMAL CHANGES FROM 514-0288 TO 514-0457, FANCY CHANGES FROM 514-0315 TO 514-0477.
CSA PAGE 67:
- ADD 2ND TITLE AUDIO: CODEC.
CSA PAGE 67:
- CHANGE J6700 FROM 514-0409 TO 514-0459 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J6700.
- NORMAL CHANGES FROM 514-0409 TO 514-0459, FANCY CHANGES FROM 514-0411 TO 514-0479.
- CHANGE J6750 FROM 514-0408 TO 514-0458 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J6750.
- NORMAL CHANGES FROM 514-0408 TO 514-0458, FANCY CHANGES FROM 514-0410 TO 514-0478.
CSA PAGE 78:
- CHANGE L7900 FROM 152S0302 TO 152S0670 FOR CORRECT AVL.
CSA PAGE 94:
- UPDATE BOM OPTION TABLE FOR J9401.
- NORMAL CHANGES FROM 514-0375 TO 514-0480, FANCY CHANGES FROM 514-0376 TO 514-0481.

7/13/2007
CSA PAGE 4:
- CHANGE BEST CPU FROM 337S3465(2.4GHZ) TO 337S3464(2.2GHZ).
CSA PAGE 38:
- CHANGE C3831 AND C3832 FROM 138S0582 TO 138S0554 (DON'T NEED LOW-PROFILE PARTS).

7/17/2007
CSA PAGE 59:
- UPDATE SYMBOL FOR U5930, VENDOR PART NUMBER CHANGES FROM SMB380 TO BMA150.

7/24/2007
CSA PAGE 4:
- CHANGE BETTER AND BEST CPU TO G0 STEPPING PARTS (FROM 337S3464 TO 337S3500).
CSA PAGE 38:
- STUFF R2242 AND NOSTUFF R2247.
CSA PAGE 48:
- CHANGE R5201 AND R5202 FROM 5.23K TO 2.94K.
- CHANGE R5211 AND R5212 FROM 16.5K TO 9.09K.

M70 EVT TO DVT CHANGES

8/9/2007
PER CE ALL SANYO POSCAPS HAVE NEW HF PART NUMBERS.
- ALL 128S0057 BECOME 128S0147.
- ALL 128S0073 BECOME 128S0164.
- ALL 128S0111 BECOME 128S0169.
- ALL 128S0113 BECOME 128S0160.
- ALL 128S0115 BECOME 128S0160.
- ALL 128S0123 BECOME 128S0160.
- ALL 128S0124 BECOME 128S0162.
- ALL 128S0129 BECOME 128S0135.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.
CSA PAGE 4:
- ADD BOM OPTION TABLE FOR ALL SANYO POSCAP TO USE HF PARTS.

Revision History

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE NONE SHEET 5 OF 76

# Functional Test Points

## Power Supply NO\_TESTS

NO_TEST		
1E33	IMVP6_RBIAS	59A4 59B7
1E34	IMVP6_COMP	59A4 59B7
1E35	5VS5_RUNSS	63B5 65C5
1E36	1V5S0_RUNSS	58B1 61B5

## Fan Connectors Battery Digital Connector

FAN CONNECTORS		BATTERY		DIGITAL CONNECTOR	
FUNC_TEST		FUNC_TEST		FUNC_TEST	
1E37	TRUE =PP5V_S0_FAN_RT	7A7 5004	1E37	TRUE SMC_BS_ALRT_L	44C5 45C5 57A2
1E38	TRUE FAN_RT_PWM	50B3	1E38	TRUE SMBUS_BATT_SCL_F	57A5
1E39	TRUE FAN_RT_TACH	50C3	1E39	TRUE SMBUS_BATT_SDA_F	57A5
1E40	TRUE =PP3V3_S0_FAN_RT	704 5004	1E40	TRUE BATT_POS	57B5
1E41	TRUE SMC_FAN_1_CTL	44A8 50B4	1E41	TRUE BATT_NEG	57A5
1E42	TRUE SMC_FAN_1_TACH	44A8 5004			

## CLOCK NO\_TESTS

NO_TEST		
1E3A	TRUE CK505_CPU0_N	28C4 29D6 75D3
1E3B	TRUE CK505_CPU0_P	28C4 29D6 75D3
1E3C	TRUE CK505_CPU1_N	28C4 29D6 75D3
1E3D	TRUE CK505_CPU1_P	28C4 29D6 75D3
1E3E	TRUE CK505_CPU2_ITP_SRC10_N	28C4 29D6 75D3
1E3F	TRUE CK505_CPU2_ITP_SRC10_P	28C4 29D6 75D3
1E43	TRUE CK505_DOT96_27M_N	28A4 29B6 75D3
1E44	TRUE CK505_DOT96_27M_P	28A4 29B6 75D3
1E45	TRUE CK505_LVDS_N	28B4 29C6 75C3
1E46	TRUE CK505_LVDS_P	28B4 29C6 75C3
1E47	TRUE CK505_PCIF1_CLK	28B6 29B6 75D3
1E48	TRUE CK505_SRC2_N	28B4 29C6 75C3
1E49	TRUE CK505_SRC2_P	28B4 29C6 75C3
1E4A	TRUE CK505_SRC4_N	28B4 29C6 75C3
1E4B	TRUE CK505_SRC4_P	28B4 29C6 75C3
1E4C	TRUE CK505_SRC5_N	28B4 29C6 75C3
1E4D	TRUE CK505_SRC5_P	28B4 29C6 75C3
1E4E	TRUE CK505_SRC6_N	28B4 29B6 75C3
1E4F	TRUE CK505_SRC6_P	28B4 29C6 75C3
1E50	TRUE CK505_SRC8_N	28A4 29B6 75C3
1E51	TRUE CK505_SRC8_P	28A4 29B6 75C3

## LPC+ Debug Connector

FUNC_TEST	
1E52	TRUE =PP3V42_G3H_LPCPLUS
1E53	TRUE =PP5V_S0_LPCPLUS
1E54	TRUE LPC_AD<0>
1E55	TRUE LPC_AD<1>
1E56	TRUE LPC_FRAME_L
1E57	TRUE PM_CLKRUN_L
1E58	TRUE BOOT_LPC_SPI_L
1E59	TRUE SMC_TMS
1E5A	TRUE DEBUG_RESET_L
1E5B	TRUE SMC_TRST_L
1E5C	TRUE SMC_TDO
1E5D	TRUE SMC_MD1
1E5E	TRUE SMC_TX_L
1E5F	TRUE FW_H_INIT_L
1E60	TRUE PCI_CLK33M_LPCPLUS
1E61	TRUE LPC_AD<2>
1E62	TRUE LPC_AD<3>
1E63	TRUE INT_SERIRO
1E64	TRUE PM_SUS_STAT_L
1E65	TRUE SMC_TDI
1E66	TRUE SMC_TCK
1E67	TRUE SMC_RESET_L
1E68	TRUE SMC_NMI
1E69	TRUE SMC_RX_L
1E6A	TRUE LINDACARD_GPIO

## Audio FUNC TEST

FUNC_TEST	
1E6B	TRUE =PP5V_S0_AUDIO_AMP
1E6C	TRUE =PP5V_S0_AUDIO
1E6D	TRUE GND_AUDIO_AMP
1E6E	TRUE GND_AUDIO_CODEC
1E6F	TRUE ACZ_SDATAIN<0>
1E70	TRUE ACZ_SDATOUT
1E71	TRUE ACZ_BITCLK
1E72	TRUE ACZ_RST_L
1E73	TRUE ACZ_SYNC

## Battery FUNC TEST

FUNC_TEST	
1E74	TRUE SMC_BATT_ISET
1E75	TRUE SMC_BATT_CHG_EN
1E76	TRUE SMC_BC_AOK
1E77	TRUE SMC_ADAPTER_EN
1E78	TRUE SMC_BATT_TRICKLE_EN_L
1E79	TRUE SYS_ONEWIRE

## USB FUNC TEST

FUNC_TEST	
1E7A	TRUE TP_USB_EXCARD_P
1E7B	TRUE TP_USB_EXCARD_N
1E7C	TRUE TP_USB_EXTC_P
1E7D	TRUE TP_USB_EXTC_N
1E7E	TRUE USB2_BT_F_P
1E7F	TRUE USB2_BT_F_N
1E80	TRUE USB2_3G_F_N
1E81	TRUE USB2_3G_F_P

## FIREWARE NO\_TESTS

NO_TEST		
1E52	TRUE FW_B_TPA_N_SPN	8D1
1E53	TRUE FW_B_TPA_P_SPN	8D1
1E54	TRUE FW_B_TPBIAS_SPN	8D1
1E55	TRUE FW_B_TPB_N_SPN	8D1
1E56	TRUE FW_B_TPB_P_SPN	8D1
1E57	TRUE FW_C_TPA_N_SPN	8D1
1E58	TRUE FW_C_TPA_P_SPN	8D1
1E59	TRUE FW_C_TPBIAS_SPN	8D1
1E5A	TRUE FW_C_TPB_N_SPN	8D1
1E5B	TRUE FW_C_TPB_P_SPN	8D1

## LVDS NO\_TESTS

NO_TEST		
1E5C	TRUE LVDS_B_CLK_N_SPN	8D5
1E5D	TRUE LVDS_B_CLK_P_SPN	8D5
1E5E	TRUE LVDS_B_DATA_N0_SPN	8D5
1E5F	TRUE LVDS_B_DATA_N1_SPN	8D5
1E60	TRUE LVDS_B_DATA_N2_SPN	8D5
1E61	TRUE LVDS_B_DATA_P1_SPN	8D5
1E62	TRUE LVDS_B_DATA_P2_SPN	8D5

## Other Func Test Points

FUNC_TEST	
1E52	TRUE =PP1V05_S0_REG
1E53	TRUE SMBUS_SMC_B_S0_SCL
1E54	TRUE SMBUS_SMC_B_S0_SDA
1E55	TRUE PPFW_SWITCH
1E56	TRUE SYS_LED_ANODE
1E57	TRUE SMC_LID
1E58	TRUE SMC_MANUAL_RST_L
1E59	TRUE SMC_CPU_VSENSE
1E5A	TRUE ALL_SYS_PWRGD
1E5B	TRUE PPVCORE_S0_CPU
1E5C	TRUE PP1V05_S0_R
1E5D	TRUE PP1V05_S0
1E5E	TRUE PP1V8_S0
1E5F	TRUE PP3V3_S0
1E60	TRUE PP5V_S0
1E61	TRUE PP1V2_ENET_S0
1E62	TRUE PP1V8_S3
1E63	TRUE PP3V3_S3
1E64	TRUE PP5V_S3
1E65	TRUE PP3V3_S5
1E66	TRUE PP5V_S5
1E67	TRUE PP3V42_G3H
1E68	TRUE PPBUS_G3H
1E69	TRUE PP18V5_G3H
1E6A	TRUE PP0V9_S0
1E6B	TRUE PP3V3_S3_BT_F
1E6C	TRUE GND_BT_F

## DC-JACK FUNC TEST

1E52	TRUE ACIN_ENABLE_GATE
------	-----------------------

## Battery charger FUNC TEST

1E53	TRUE PPVBAT_G3H_CHGR_OUT
------	--------------------------

## INVERTER CONNECTOR FUNC TEST

1E54	TRUE PPBUS_ALL_INV_CONN
1E55	TRUE INV_GND
1E56	TRUE PP5V_INV_F
1E57	TRUE INV_BKLIGHT_PWM_L

## MIC FUNC TEST

1E58	TRUE MIC_HI
1E59	TRUE MIC_LO
1E5A	TRUE MIC_SHIELD
1E5B	TRUE MIC_HI_CONN
1E5C	TRUE MIC_LO_CONN
1E5D	TRUE MIC_SHLD_CONN

## SPEAKER FUNC TEST

1E5E	TRUE SPKRCONN_L_N_OUT
1E5F	TRUE SPKRCONN_L_P_OUT
1E60	TRUE SPKRCONN_R_N_OUT
1E61	TRUE SPKRCONN_R_P_OUT
1E62	TRUE SPKRCONN_SUB_N_OUT
1E63	TRUE SPKRCONN_SUB_P_OUT

## THERMAL FUNC TEST

1E64	TRUE THRM_HEATPIPE_P
1E65	TRUE THRM_HEATPIPE_N
1E66	TRUE THRM_DIMM_DX_F_N
1E67	TRUE THRM_DIMM_DX_F_P
1E68	TRUE THRM_FINSTACK_P
1E69	TRUE THRM_FINSTACK_N

FUNC TEST 1 OF 2

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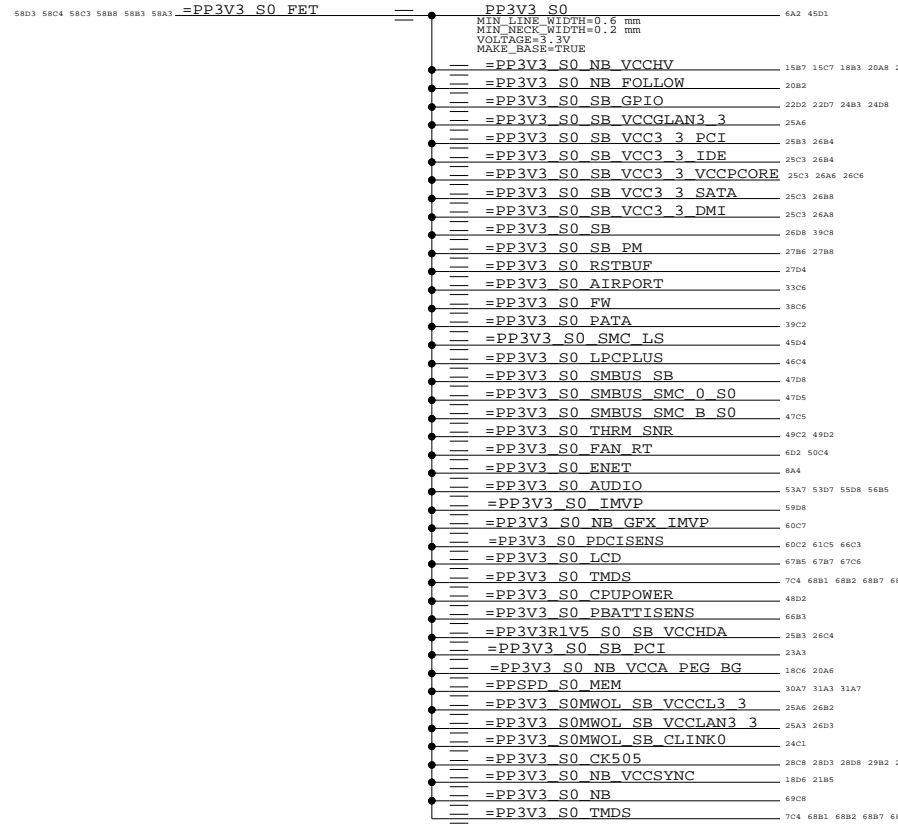
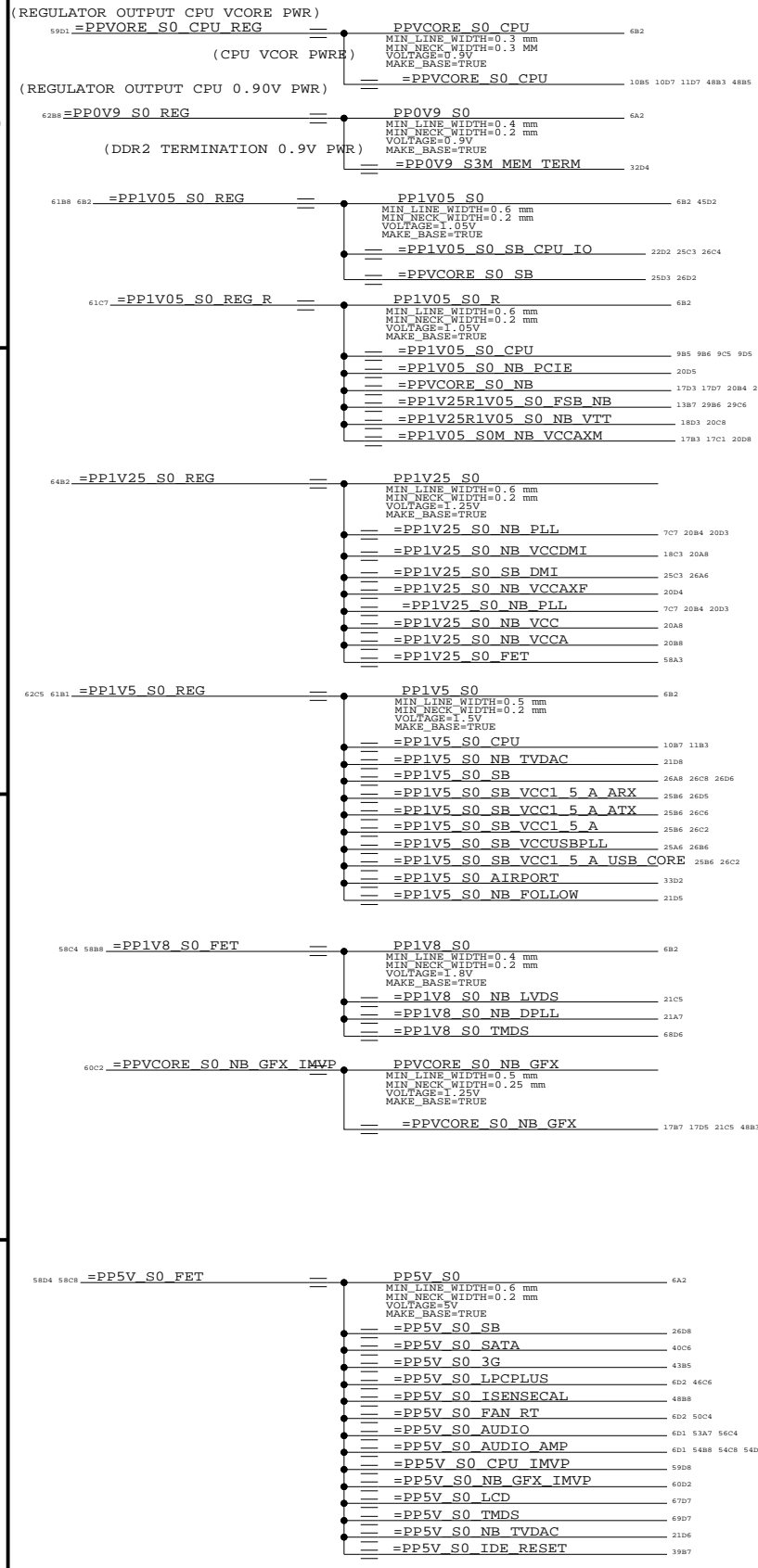
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SCALE DRAWING NUMBER REV.

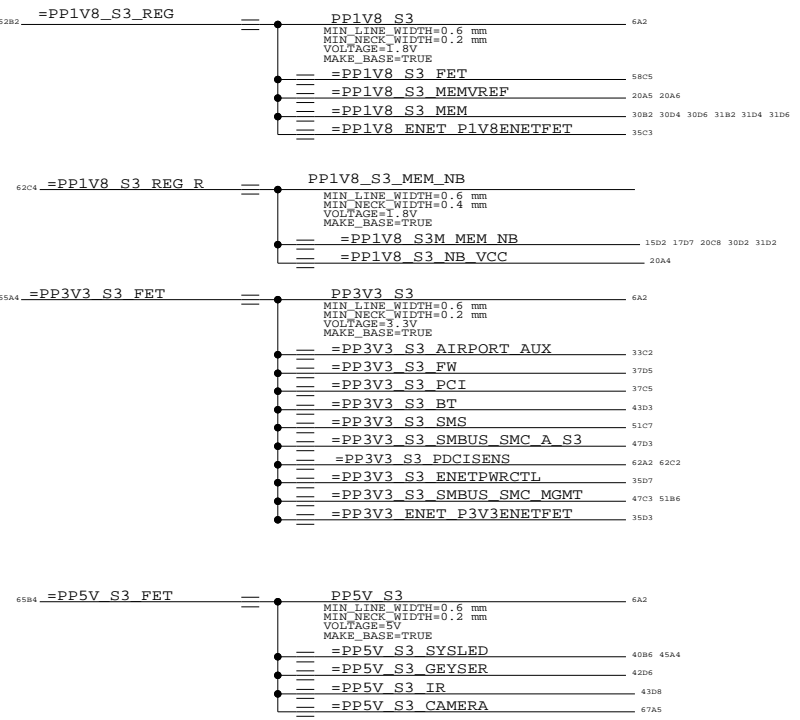
D 051-7455 01

SHEET 6 OF 76

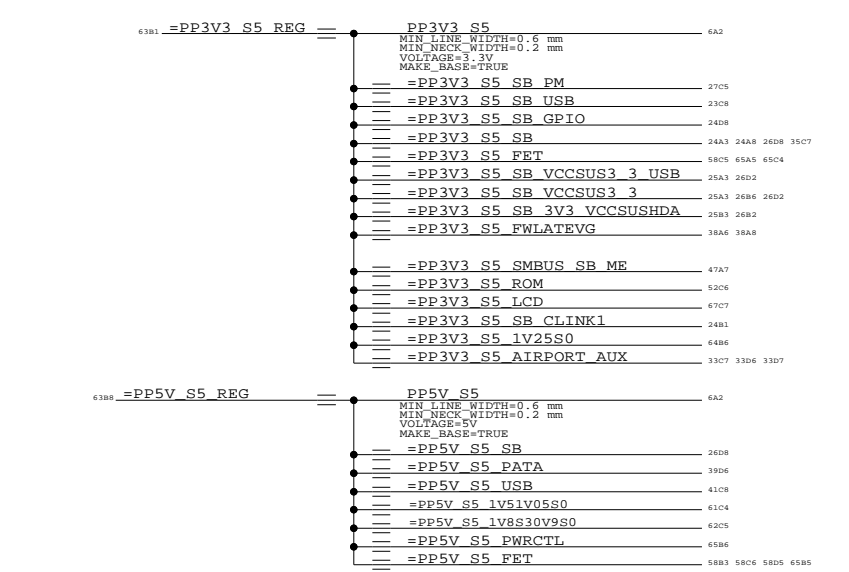
"S0,S0M" RAILS



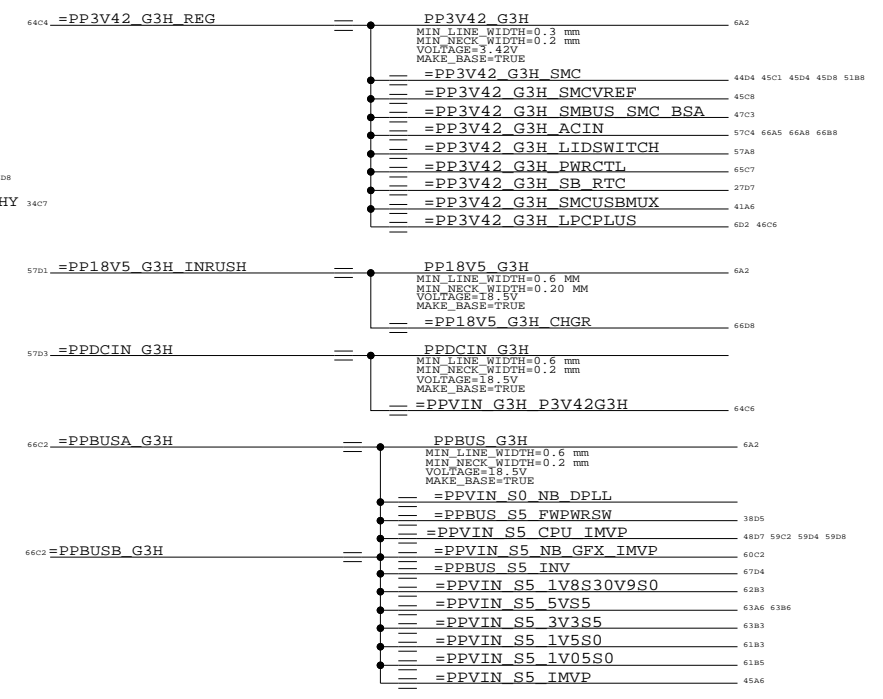
"S3" RAILS



"S5" RAILS



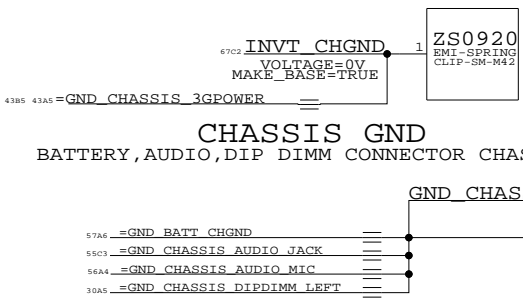
"G3H" RAILS



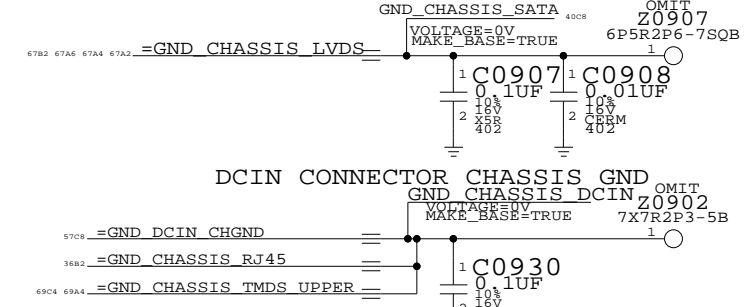
Power Aliases  
 SYNC\_MASTER=WFERRY SYNC\_DATE=06/15/2006  
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 SCALE NONE SHEET 7 OF 76

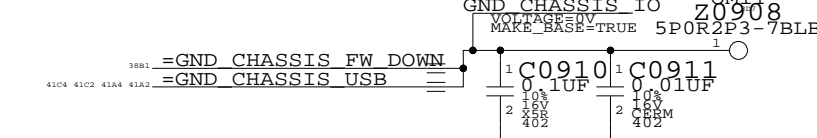
(EMI PAD FOR INVERTER GONNECTOR)



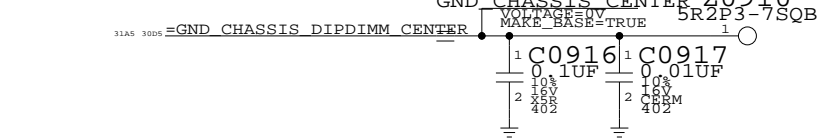
SATA, LVDS CONNECTOR CHASSIS GND



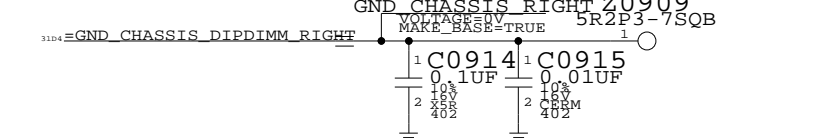
I/O CONNECTOR CHASSIS GND



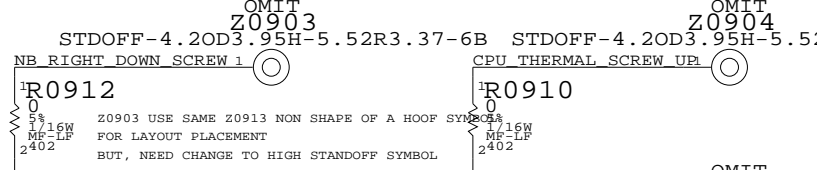
DIP DIMM CONNECTOR CHASSIS GND



DIP DIMM CONNECTOR CHASSIS GND



CPU HEATSINK STANDOFF SCREW HOLE



LVDS ALIASES

Table of LVDS aliases including NO-CONNECT UNUSED LVDS INTERFACE PORTS and LVDS B CLK N, LVDS B CLK P, etc.

PCI EXPRESS GRAPHICS ALIASES

Table of PCI EXPRESS GRAPHICS aliases including NO-CONNECT UNUSED SDVO INTERFACE PORTS and PEG D2R N<0>, PEG D2R N<1>, etc.

NB CFG ALIASES

Table of NB CFG aliases including TP NB CFG<3>, TP NB CFG<4>, etc.

SATA ALIASES

Table of SATA aliases including NO-CONNECT UNUSED SATA INTERFACE PORTS and SATA B D2R N, SATA B D2R P, etc.

PCI\_EXP ALIASES

Table of PCI\_EXP aliases including NO-CONNECT UNUSED PCI\_EXP INTERFACE PORTS and TP\_PCIE A D2R N, TP\_PCIE A D2R P, etc.

CLOCK ALIASES

Table of CLOCK aliases including NO-CONNECT UNUSED CLOCK INTERFACE PORTS and TP\_CK505 SRC1 N, TP\_CK505 SRC1 P, etc.

SB ALIASES

Table of SB aliases including NO-CONNECT UNUSED CLOCK INTERFACE PORTS and VR\_PWRGD\_CLKEN, SB\_CLINK\_MPWRK, etc.

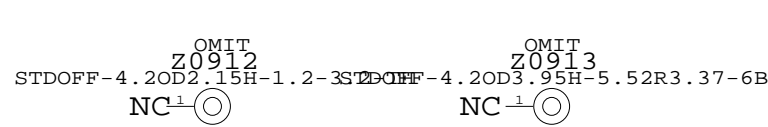
SO-DIMM ALIASES

Table of SO-DIMM aliases including NO-CONNECT UNUSED ADDRESS INTERFACE PORTS and MEM\_A A<15>, MEM\_B A<15>, etc.

Ethernet ALIASES

Table of Ethernet aliases including =PP3V3 S0 ENET, =YUKON\_EC PP2V5 ENET, etc.

AIRPORT CARD STANDOFF SCREW HOLE



FIREWIRE ALIASES

Table of FIREWIRE aliases including NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS and FW\_B\_TPBIAS, FW\_B\_TPA P, etc.

USB PORT [0] = External USB2.0 Port A

Table for USB PORT [0] aliases including USB2\_EXTN\_P, USB2\_EXTN\_N, etc.

USB PORT [1] = PCI-E Mini Card

Table for USB PORT [1] aliases including USB2\_AIRPORT\_P, USB2\_AIRPORT\_N, etc.

USB PORT [2] = 3G USB

Table for USB PORT [2] aliases including USB2\_3G\_P, USB2\_3G\_N, etc.

USB PORT [3] = CAMERA

Table for USB PORT [3] aliases including USB2\_CAMERA\_P, USB2\_CAMERA\_N, etc.

USB PORT [4] = IR CONTROLLER

Table for USB PORT [4] aliases including USB2\_IR\_P, USB2\_IR\_N, etc.

USB PORT [5] = Trackpad(Geyser)

Table for USB PORT [5] aliases including USB2\_GEYSER\_P, USB2\_GEYSER\_N, etc.

USB PORT [6] = BLUETOOTH

Table for USB PORT [6] aliases including USB2\_BT\_P, USB2\_BT\_N, etc.

USB PORT [7] = External USB2.0 Port B

Table for USB PORT [7] aliases including USB2\_EXTNB\_P, USB2\_EXTNB\_N, etc.

USB PORT [8] = Unused

Table for USB PORT [8] aliases including TP\_USB\_EXCARD\_P, TP\_USB\_EXCARD\_N, etc.

USB PORT [9] = Unused

Table for USB PORT [9] aliases including TP\_USB\_EXTC\_P, TP\_USB\_EXTC\_N, etc.

ANALOG SWITCH GPIO

Table for ANALOG SWITCH GPIO aliases including PM\_EXTTTS\_L<0>, PM\_EXTTTS\_L<1>, etc.

NB ALIASES

Table of NB aliases including =GFX\_VR\_EN, =NB\_CLKMPWRK, etc.

Table with columns: PART#, QTY, DESCRIPTION, REFERENCE DESIGNATOR(S), BOM OPTION. Includes items like 860-0876 THERMAL STANDOFF.

SIGNAL ALIAS /RESET

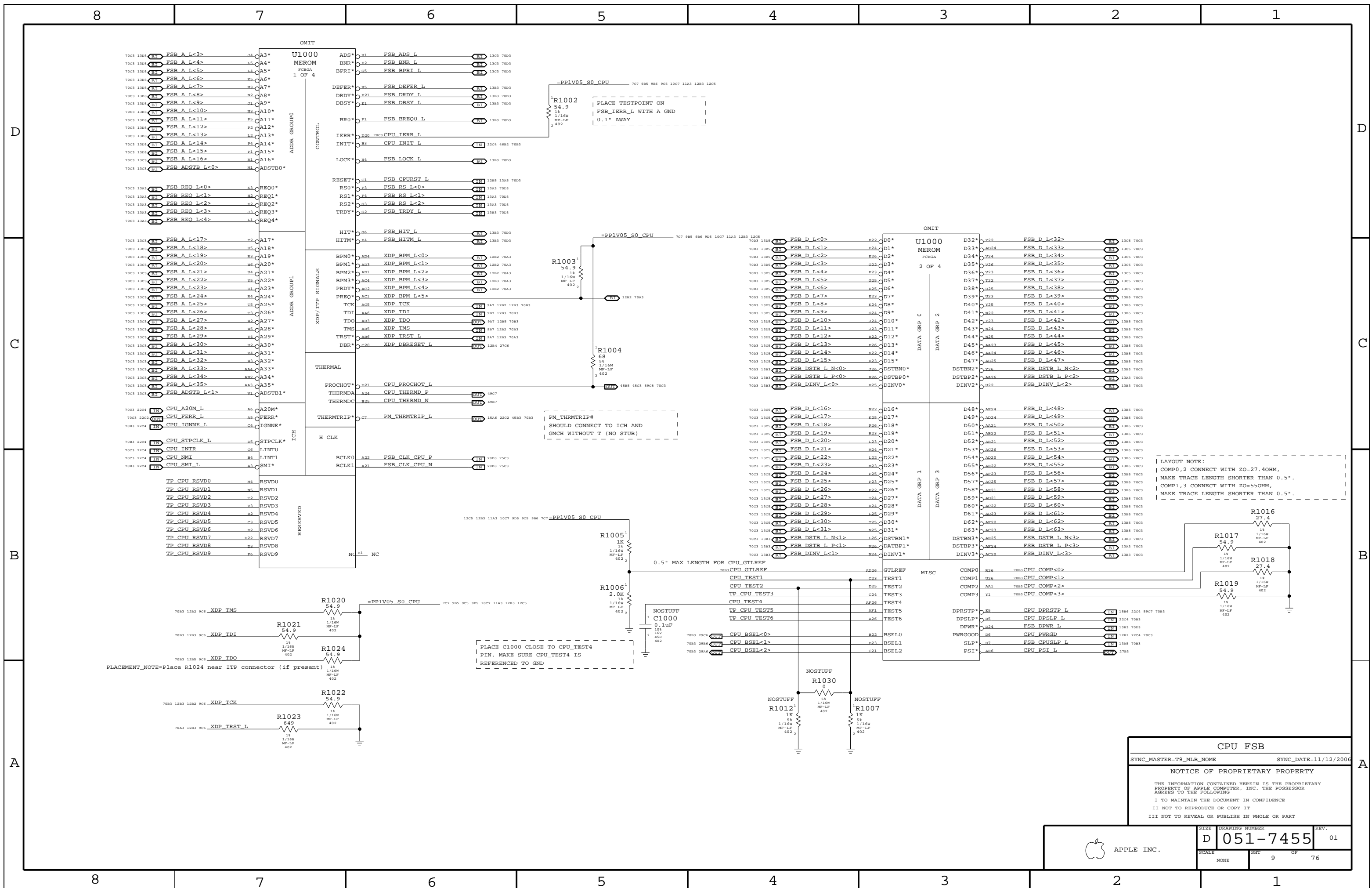
SYNC\_MASTER=GPU SYNC\_DATE=07/17/2006

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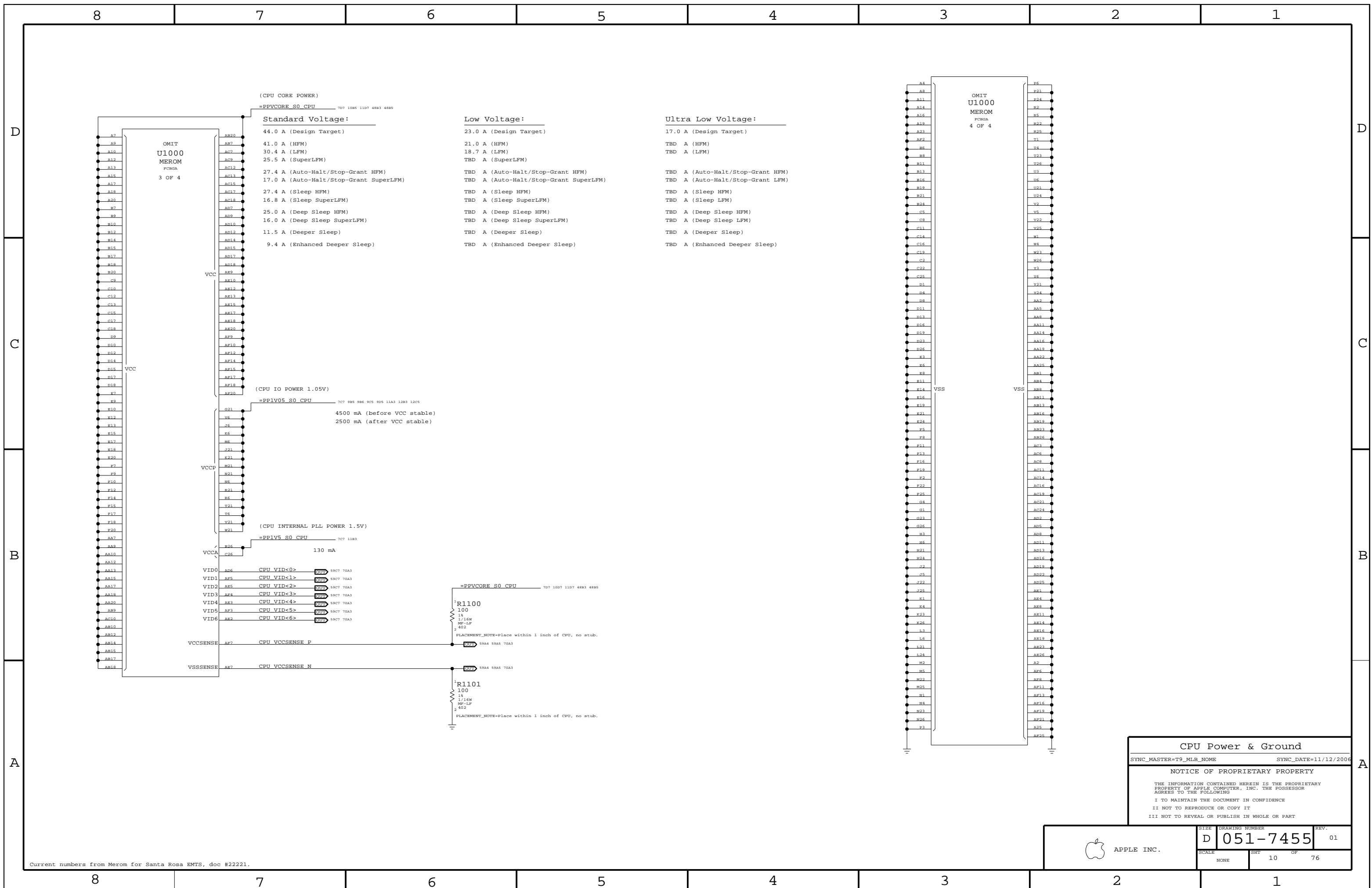
LAYOUT NOTE:  
 COMP0, 2 CONNECT WITH Z0=27.4OHM,  
 MAKE TRACE LENGTH SHORTER THAN 0.5".  
 COMP1, 3 CONNECT WITH Z0=55OHM,  
 MAKE TRACE LENGTH SHORTER THAN 0.5".

PLACE C1000 CLOSE TO CPU\_TEST4  
 PIN. MAKE SURE CPU\_TEST4 IS  
 REFERENCED TO GND

PM\_THRMTRIP#  
 SHOULD CONNECT TO ICH AND  
 GND WITHOUT T (NO STUB)

**CPU FSB**  
 SYNC\_MASTER=T9\_MLB\_NOME SYNC\_DATE=11/12/2006  
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	NONE	D	051-7455	01
		SHT	9	OF 76



**CPU Power & Ground**

SYNC\_MASTER=T9\_MLB\_NOME SYNC\_DATE=11/12/2006

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	SCALE NONE	SHEET 10 OF 76

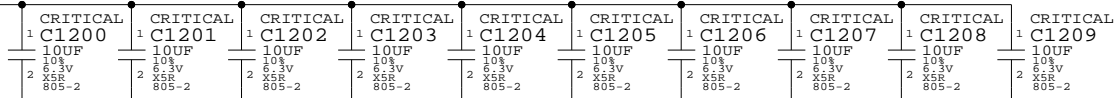
Current numbers from Merom for Santa Rosa EMTS, doc #22221.

# CPU VCORE HF AND BULK DECOUPLING

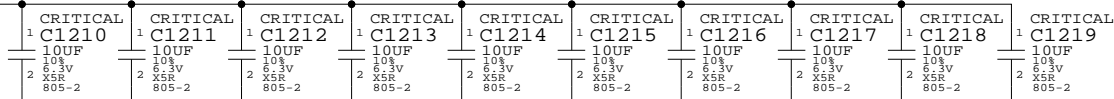
4x 330uF, 20x 10uF 0805

4885 4883 1007 1085 707 PPVCORE\_S0\_CPU

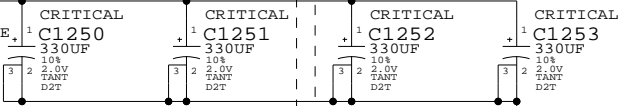
LAYOUT NOTE:  
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)



LAYOUT NOTE:  
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)



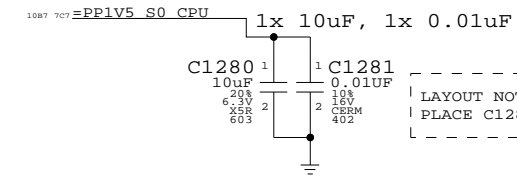
LAYOUT NOTE:  
PLACE ON BOTTOMSIDE



LAYOUT NOTE:  
PLACE ON BOTTOMSIDE

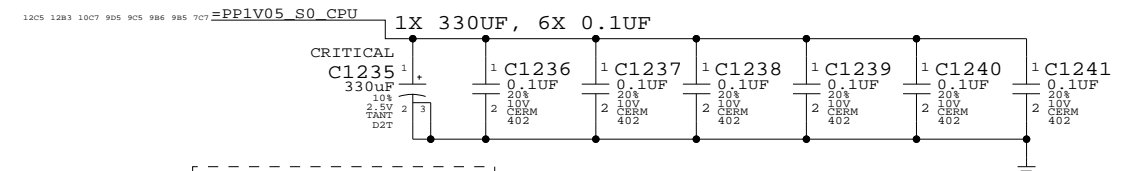
C1250, C1251, C1252 AND C1253 NEED TO USE 6mOHM CAPS.

## VCCA (CPU AVdd) DECOUPLING



LAYOUT NOTE:  
PLACE C1281 NEAR PIN B26 OF U1000

## VCCP (CPU I/O) DECOUPLING



LAYOUT NOTE:  
PLACE C1235 CLOSE TO CPU

### CPU Decoupling & VID

SYNC\_MASTER=MSARWAR SYNC\_DATE=04/26/2006

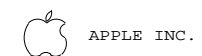
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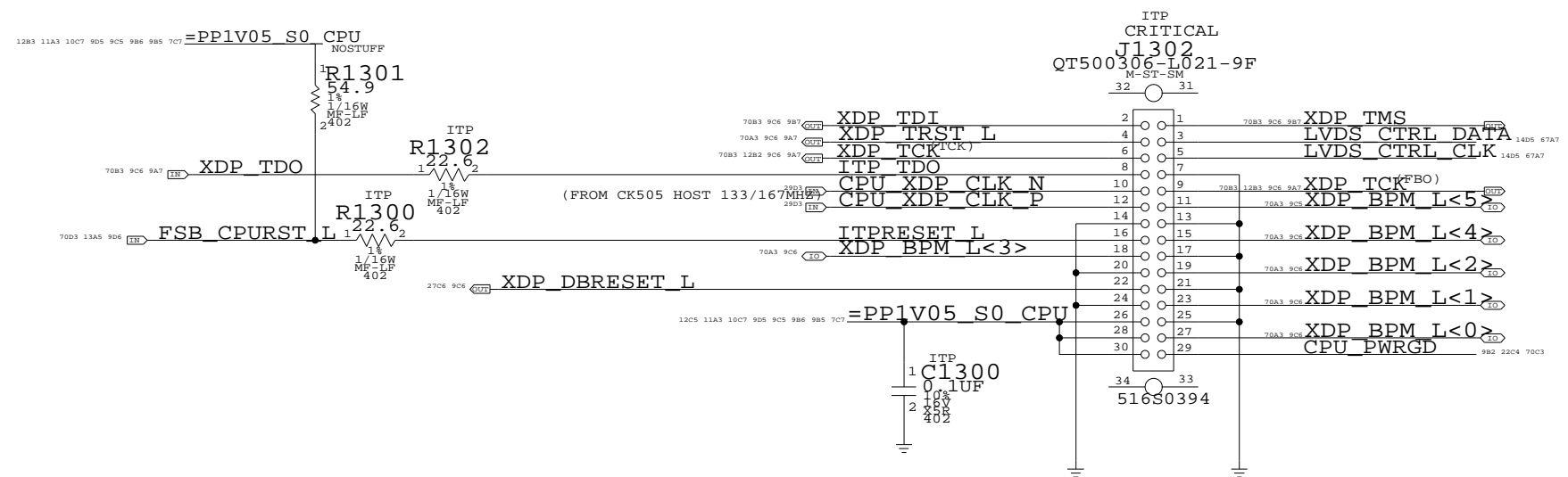


SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE SHEET OF 11 76

# CPU ITP700FLEX DEBUG SUPPORT



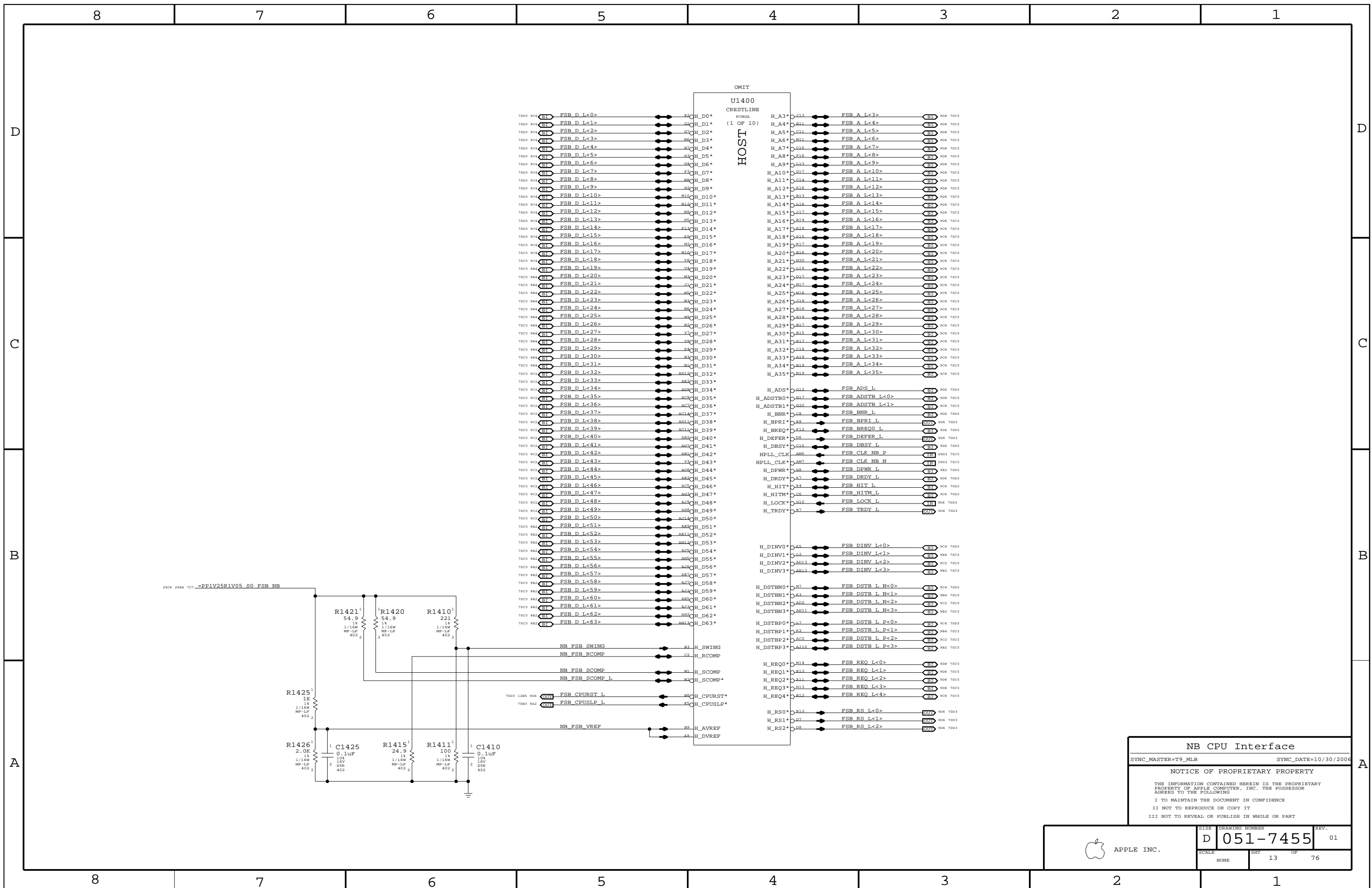
(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 965GM CHIPSET SYSTEM.  
 (DEBUG PORT ACTIVE)  
 (DBR# TO ICH8M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
 (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:  
 ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
 TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
 CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG  
 SYNC\_MASTER=MASTER SYNC\_DATE=5/23/05

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	SCALE NONE	SHEETS 12 OF 76	



**NB CPU Interface**

SYNC\_MASTER=T9\_MLB      SYNC\_DATE=10/30/2006

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APPLE INC.	SIZE: <b>D</b>	DRAWING NUMBER: <b>051-7455</b>	REV.: <b>01</b>
	SCALE: NONE	SHEET: 13	OF: 76

**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented.  
 Tie VCC\_TX\_LVDS and VCCA\_LVDS to GND.  
 If SDVO is used, VCCD\_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**  
 Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC  
 Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

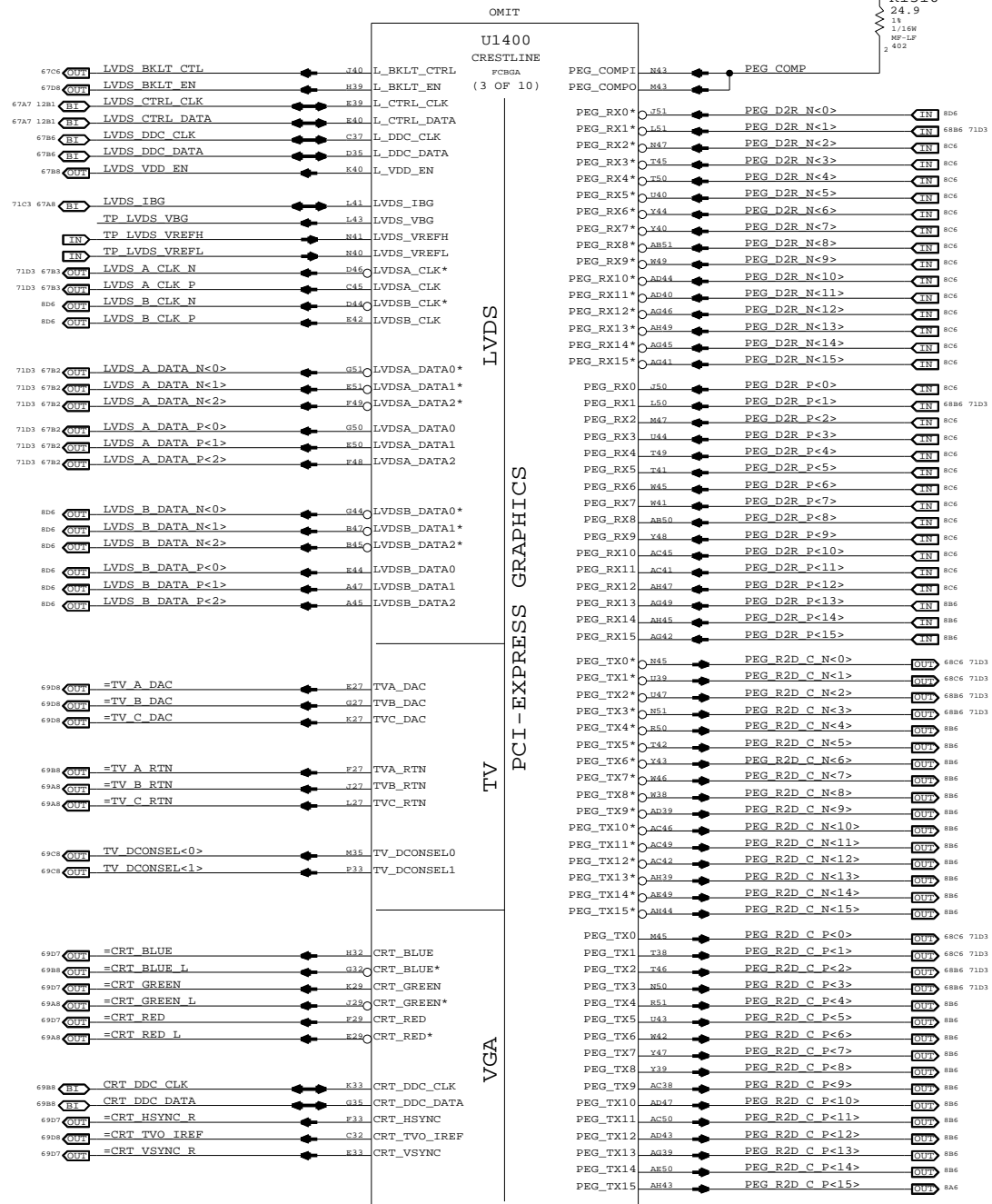
**TV-Out Disable / CRT Enable**  
 Tie TVx\_DAC and TVx\_RTN to GND. Must power all TVDAC rails. VCCA\_TVx\_DAC and VCCA\_CRT\_DAC can share filtering with VCCA\_CRT\_DAC.

**CRT Disable / TV-Out Enable**  
 Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA\_CRT.

**CRT & TV-Out Disable**  
 Tie TVx\_DAC, TVx\_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT\_TVO\_IREF to GND.  
 Can tie the following rails to GND:  
 VCCA\_CRT\_DAC, VCCA\_DAC\_BG, VCCA\_TVx\_DAC, VCCD\_CRT, VCCD\_QDAC and VCC\_SYNC.

**NOTE:** Must keep VDDC\_TVDAC powered and filtered at all times!

**Internal Graphics Disable**  
 Follow instructions for LVDS and CRT & TV-Out Disable above.  
 Can also tie CRT\_DDC\_\*, L\_CTRL\_\*, L\_DDC\_\*, SDVO\_CTRL\_\* and TV\_DCONSELx to GND.  
 Tie DPLL\_REF\_CLK and DPLL\_REF\_SSCLK to GND.  
 Tie DPLL\_REF\_CLK\* and DPLL\_REF\_SSCLK\* to VCC (VCore).  
 Tie VCCA\_DPLL and VCCA\_DPLL\_B to VCC (VCore).  
 Tie VCC\_AXG and VCC\_AXG\_NCTF to GND.  
 Leave GFX\_VID<3..0> and GFX\_VR\_EN as NC.



**SDVO Alternate Function**  
 SDVO\_TVCLKIN#  
 SDVO\_INT#  
 SDVO\_FLDSTALL#

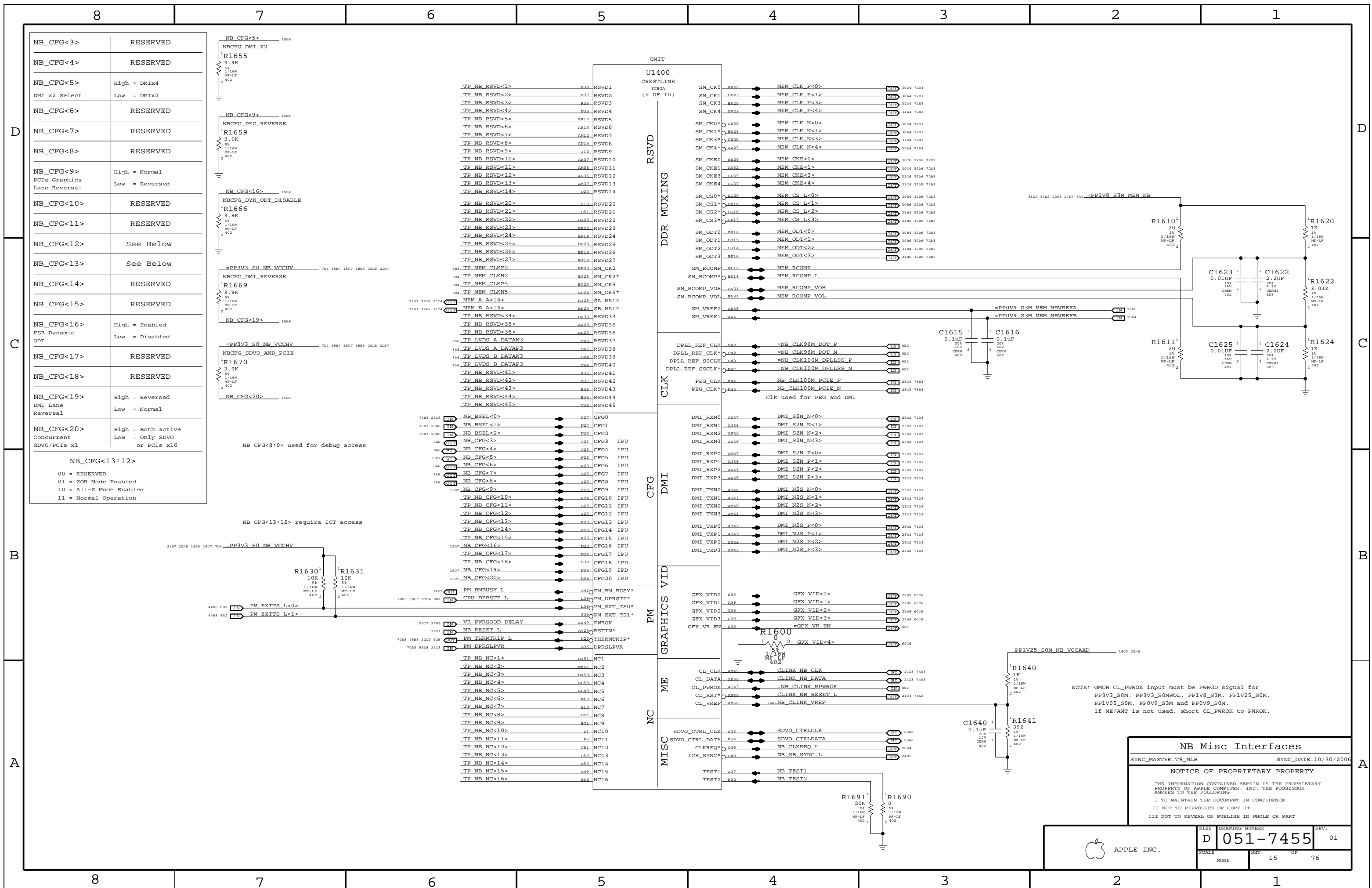
SDVO\_TVCLKIN  
 SDVO\_INT  
 SDVO\_FLDSTALL

SDVOB\_RED#  
 SDVOB\_GREEN#  
 SDVOB\_BLUE#  
 SDVOB\_CLKN  
 SDVOC\_RED#  
 SDVOC\_GREEN#  
 SDVOC\_BLUE#  
 SDVOC\_CLKN

SDVOB\_RED  
 SDVOB\_GREEN  
 SDVOB\_BLUE  
 SDVOB\_CLKP  
 SDVOC\_RED  
 SDVOC\_GREEN  
 SDVOC\_BLUE  
 SDVOC\_CLKP

**NB PEG / Video Interfaces**  
 SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006  
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APPLE INC. DRAWING NUMBER: D 051-7455 REV. 01  
 SCALE: NONE SHEET: 14 OF 76



NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIX4 DMI x2 Select Low = DMIX2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent Low = Only SDVO or PCIe x16

**NB\_CFG<13:12>**  
 00 = RESERVED  
 01 = XOR Mode Enabled  
 10 = All-Z Mode Enabled  
 11 = Normal Operation

NB\_CFG<8:0> used for debug access

NB\_CFG<13:12> require ICT access

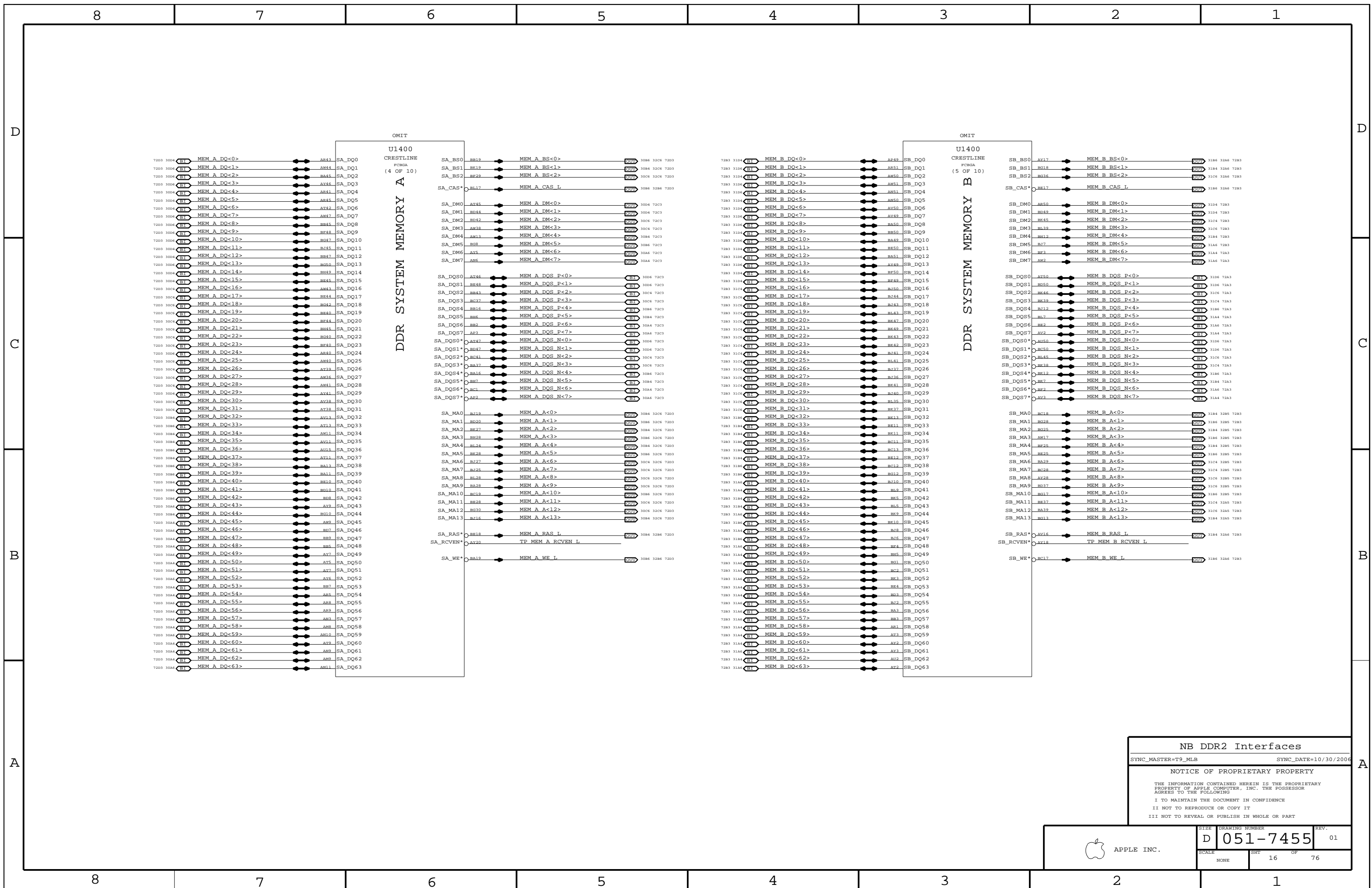
**NB Misc Interfaces**

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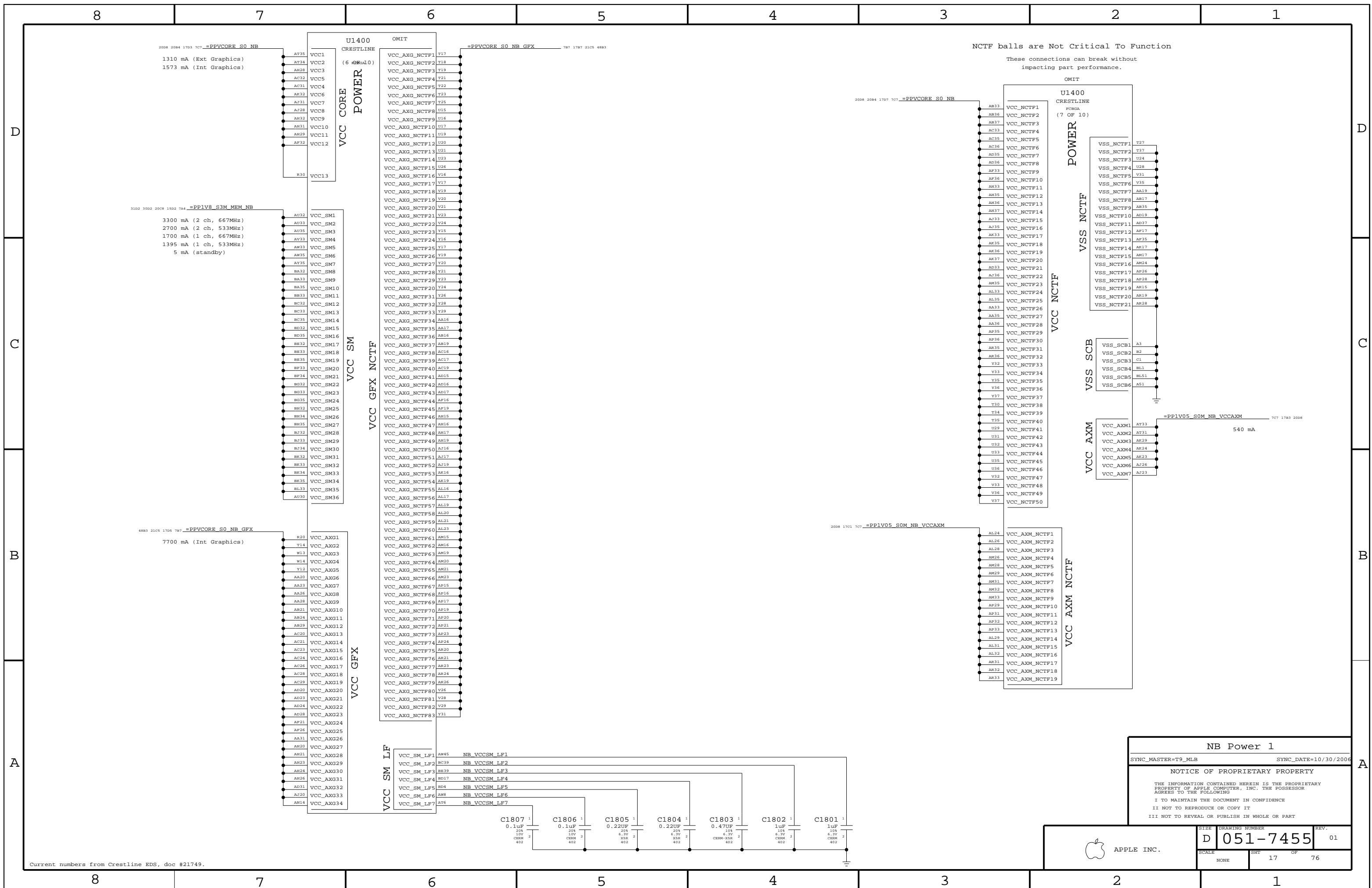
APPLE INC.	SCALE	SHEET	OF	REV.
	NONE	15	76	01



**NB DDR2 Interfaces**  
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APPLE INC.	DRAWING NUMBER <b>D 051-7455</b> 01 SCALE NONE SHT 16 OF 76
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NCTF balls are Not Critical To Function  
 These connections can break without impacting part performance.

2008 2084 1703 707 =PPVCORE\_S0\_NB  
 1310 mA (Ext Graphics)  
 1573 mA (Int Graphics)

3102 3002 2008 1502 744 =PP1V8\_S3M\_MEM\_NB  
 3300 mA (2 ch, 667MHz)  
 2700 mA (2 ch, 533MHz)  
 1700 mA (1 ch, 667MHz)  
 1395 mA (1 ch, 533MHz)  
 5 mA (standby)

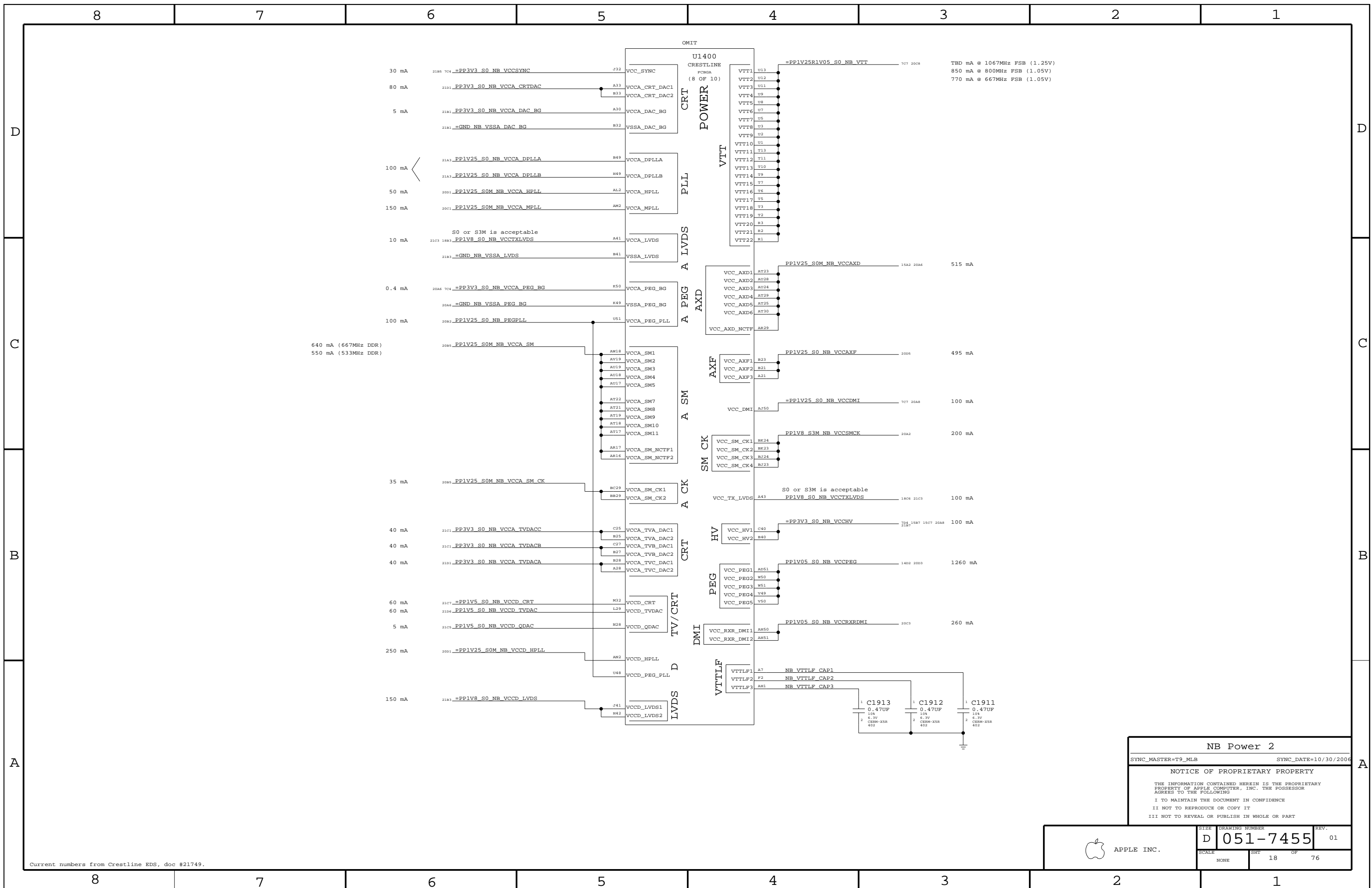
4883 2105 1705 787 =PPVCORE\_S0\_NB\_GFX  
 7700 mA (Int Graphics)

NB Power 1  
 SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006

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	NONE	D 051-7455	01
		SHEET	OF
		17	76

Current numbers from Crestline EDS, doc #21749.

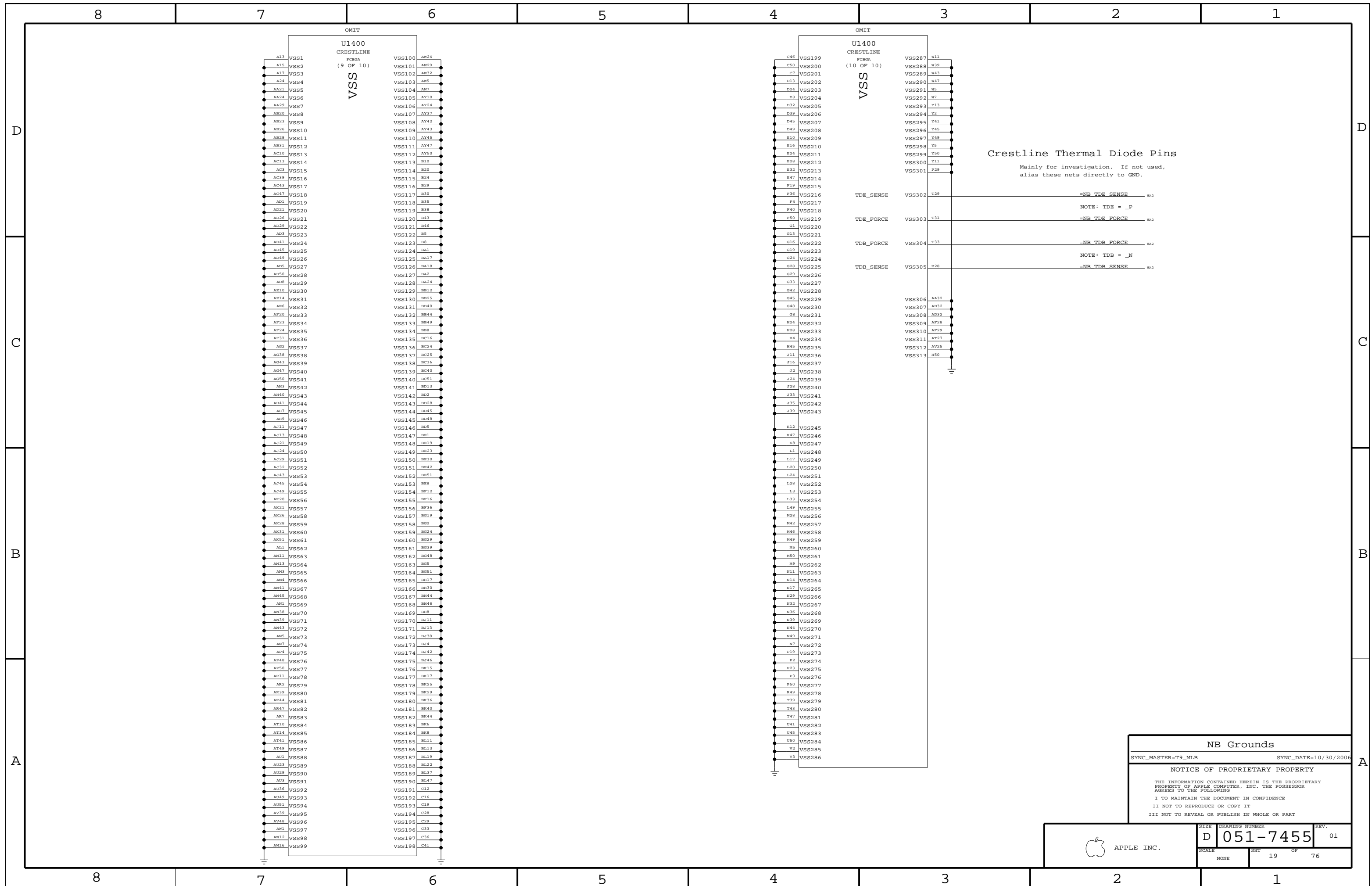


NB Power 2  
 SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006

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	D	051-7455	01
SCALE	SHT	OF	REV.
NONE	18	76	

Current numbers from Crestline EDS, doc #21749.



**Crestline Thermal Diode Pins**

Mainly for investigation. If not used,  
alias these nets directly to GND.

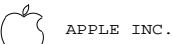
TDE\_SENSE VSS302 T29 =NB TDE\_SENSE BA2  
NOTE: TDE = \_P  
TDE\_FORCE VSS303 T31 =NB TDE\_FORCE BA2  
TDB\_FORCE VSS304 T33 =NB TDB\_FORCE BA2  
NOTE: TDB = \_N  
TDB\_SENSE VSS305 R28 =NB TDB\_SENSE BA2

**NB Grounds**

SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006

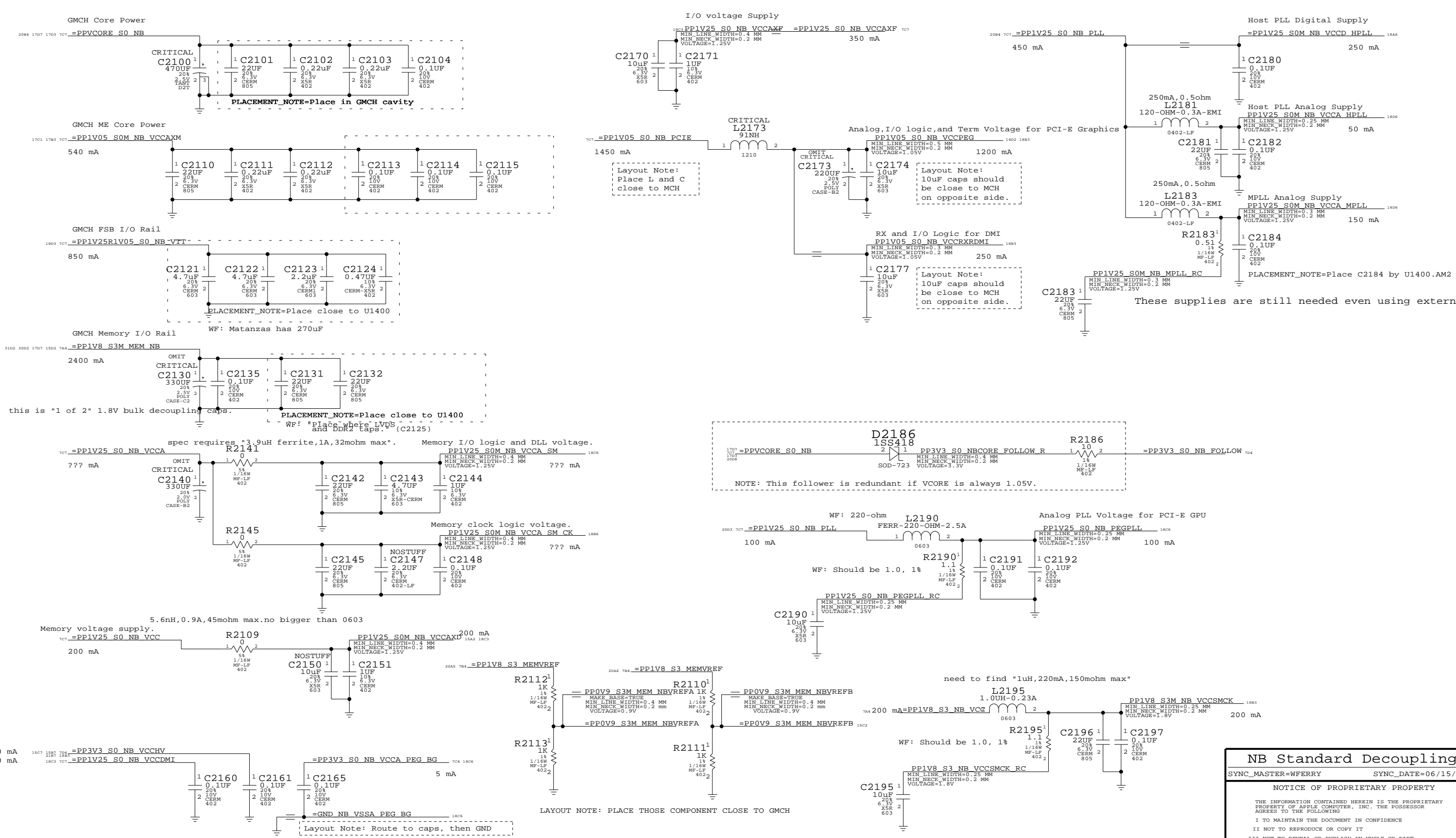
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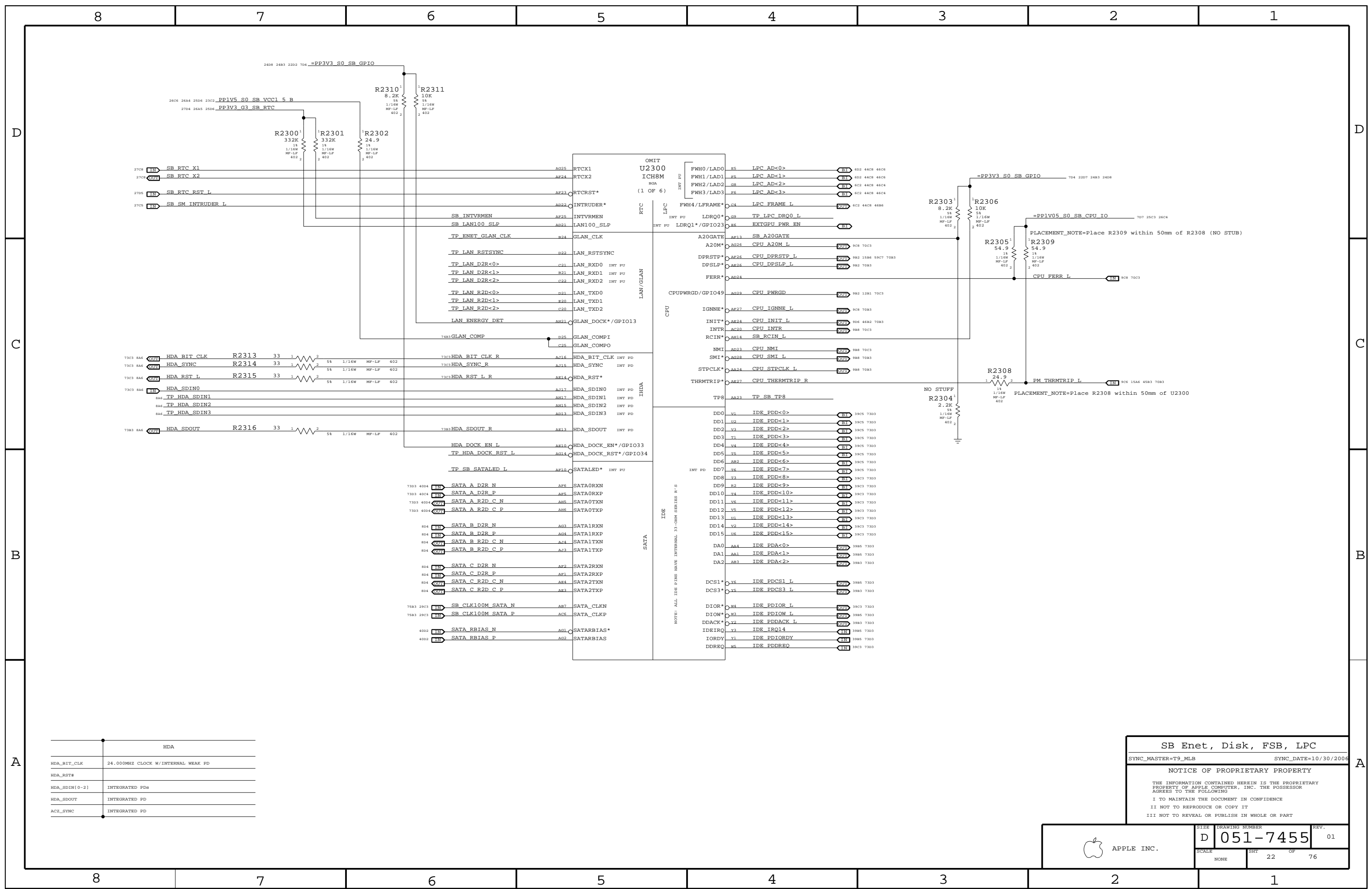
SIZE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
SCALE	SHEET	OF
NONE	19	76



<b>NB Standard Decoupling</b>			
SYNC_MASTER=WFERRY		SYNC_DATE=06/15/2006	
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SCALE NONE		SHT 20 OF 76	

Current numbers from Crestline EDS Addendum, doc #20127.



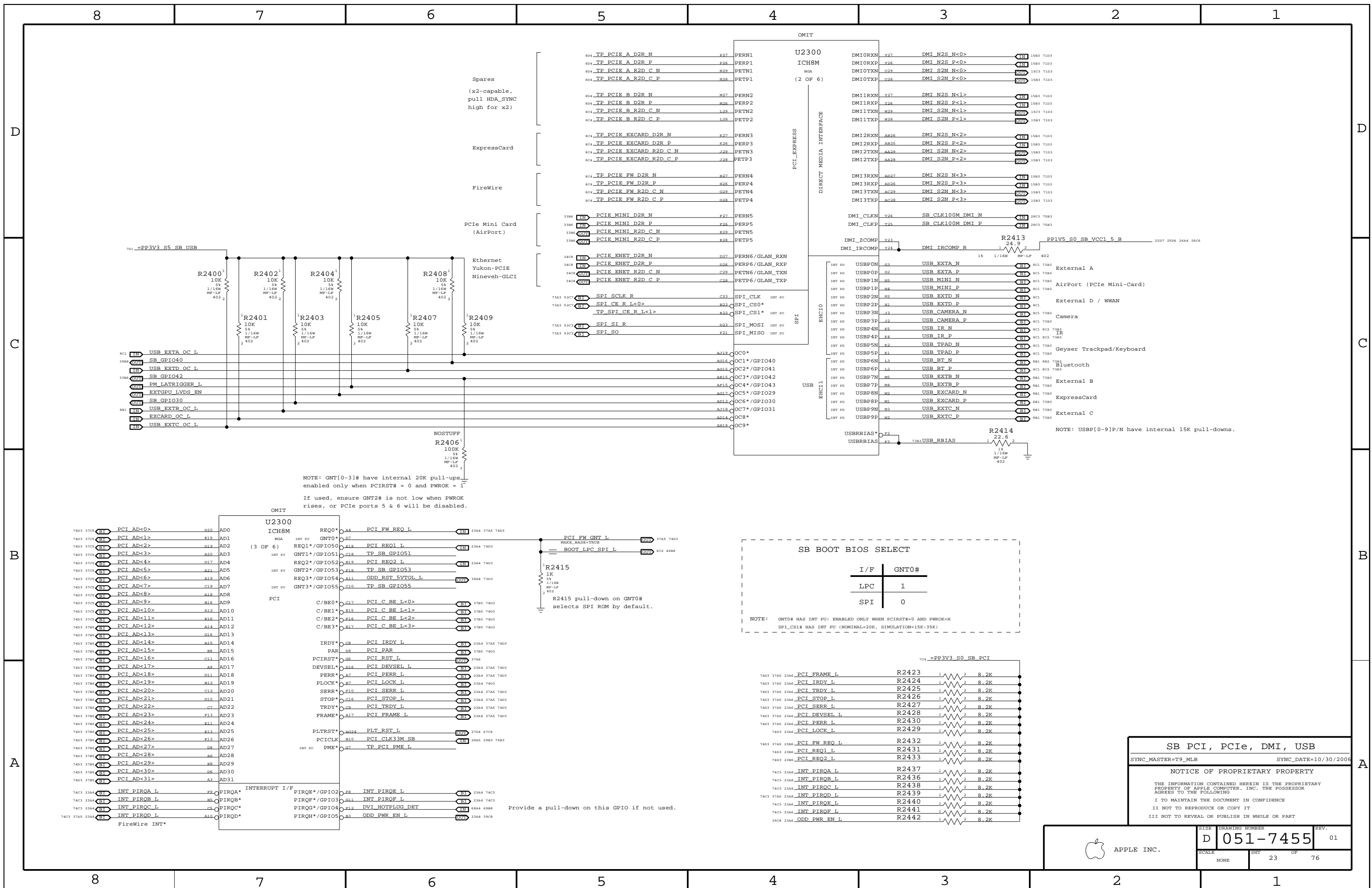


Signal	Pin	Component	Value	Notes
SB RTC X1	27C8	R2310	8.2K	
SB RTC X2	27C8	R2311	10K	
SB RTC RST L	27D4	R2300	332K	
SB SM INTRUDER L	27C8	R2301	332K	
SB INTVRMEN	AE25	R2302	24.9	
SB LAN100_SLP	AE21			
TP ENET GLAN_CLK	B24			
TP LAN_RSTSYNC	D22			
TP LAN_D2R<0>	C21			
TP LAN_D2R<1>	B21			
TP LAN_D2R<2>	C22			
TP LAN_R2D<0>	D21			
TP LAN_R2D<1>	E20			
TP LAN_R2D<2>	C20			
LAN ENERGY_DET	AE21			
HDA BIT_CLK	AE16	R2313	33	
HDA SYNC	AE15	R2314	33	
HDA_RST L	AE14	R2315	33	
HDA SDIN0	AE17			
TP HDA SDIN1	AE17			
TP HDA SDIN2	AE15			
TP HDA SDIN3	AE13			
HDA_SDOUT	AE13	R2316	33	
HDA_DOCK_EN L	AE10			
TP HDA_DOCK_RST L	AG14			
TP_SB_SATALED L	AE10			
SATA A D2R N	AF6			
SATA A D2R F	AE5			
SATA A R2D C N	AH5			
SATA A R2D C P	AH6			
SATA B D2R N	AG3			
SATA B D2R F	AG4			
SATA B R2D C N	AT4			
SATA B R2D C P	AT3			
SATA C D2R N	AF2			
SATA C D2R F	AF1			
SATA C R2D C N	AE4			
SATA C R2D C P	AE3			
SB_CLK100M SATA N	AB7			
SB_CLK100M SATA P	AC6			
SATA_BIAS_N	AG1			
SATA_BIAS_P	AG2			

HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDS
HDA_SDOUT	INTEGRATED PD
AC2_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC  
 SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006  
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	NONE	051-7455	01
SCALE		SHT	OF
NONE		22	76



Spares  
(x2-capable,  
pull HDA\_SYNC  
high for x2)

ExpressCard

FireWire

PCIe Mini Card  
(AirPort)

Ethernet  
Yukon-PCI  
Nineveh-GLCI

USB EXTA OC L  
SB GPIO40  
USB EXTD OC L  
SB GPIO42  
PM LATRIGGER L  
EXTGPU LVDS EN  
SB GPIO30  
USB EXTB OC L  
EXCARD OC L  
USB EXTC OC L

NOTE: GNT[0-3]# have internal 20K pull-ups  
enabled only when PCIRST# = 0 and PWROK = 1  
If used, ensure GNT2# is not low when PWROK  
rises, or PCIe ports 5 & 6 will be disabled.

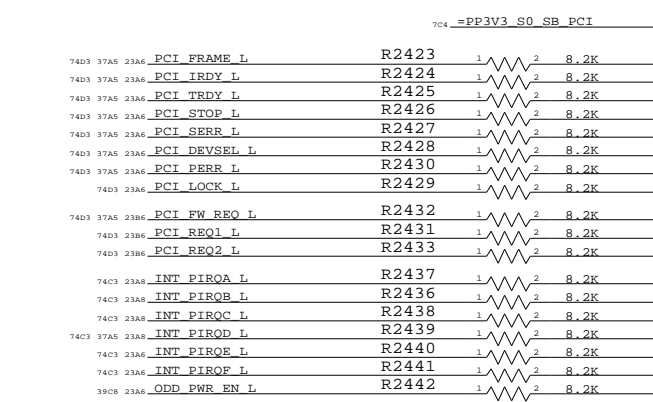
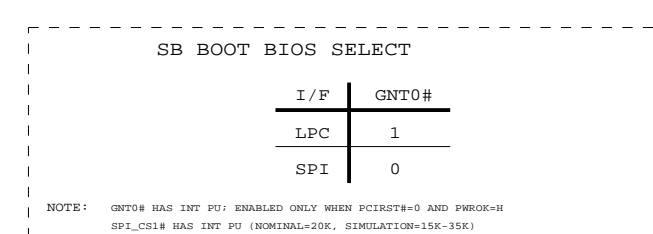
U2300 ICH8M	REQ0*	AA	PCI_FW_REQ_L	INT	2344 3745 7403
BGA	GNT0*	A7	GNT0*	INT	3745 7403
INT PU	REQ1*/GPIO50	A18	TP_SB_GPIO51	INT	3344 7403
INT PU	GNT1*/GPIO51	C18	TP_SB_GPIO51	INT	3344 7403
INT PU	REQ2*/GPIO52	B19	PCI_REQ2_L	INT	2344 7403
INT PU	GNT2*/GPIO53	F18	TP_SB_GPIO53	INT	3344 7403
INT PU	REQ3*/GPIO54	A11	ODD_RST_5VTOL_L	INT	19A8 7303
INT PU	GNT3*/GPIO55	C10	TP_SB_GPIO55	INT	3344 7403

PCI	C/BE0*	C17	PCI_C_BE_L<0>	INT	3785 7403
	C/BE1* <th>E15</th> <th>PCI_C_BE_L&lt;1&gt;</th> <th>INT</th> <th>3785 7403</th>	E15	PCI_C_BE_L<1>	INT	3785 7403
	C/BE2* <th>F14</th> <th>PCI_C_BE_L&lt;2&gt;</th> <th>INT</th> <th>3785 7403</th>	F14	PCI_C_BE_L<2>	INT	3785 7403
	C/BE3* <th>B17</th> <th>PCI_C_BE_L&lt;3&gt;</th> <th>INT</th> <th>3785 7403</th>	B17	PCI_C_BE_L<3>	INT	3785 7403

IRDY*	C8	PCI_IRDY_L	INT	2344 3745 7403
PAR	B9	PCI_PAR	INT	3785 7403
PCIRST* <th>B6</th> <th>PCI_RST_L</th> <th>INT</th> <th>3746</th>	B6	PCI_RST_L	INT	3746
DEVSEL* <th>A14</th> <th>PCI_DEVSEL_L</th> <th>INT</th> <th>2344 3745 7403</th>	A14	PCI_DEVSEL_L	INT	2344 3745 7403
PERR* <th>A7</th> <th>PCI_PERR_L</th> <th>INT</th> <th>2344 3745 7403</th>	A7	PCI_PERR_L	INT	2344 3745 7403
PLOCK* <th>B7</th> <th>PCI_LOCK_L</th> <th>INT</th> <th>2344 7403</th>	B7	PCI_LOCK_L	INT	2344 7403
SERR* <th>F10</th> <th>PCI_SERR_L</th> <th>INT</th> <th>2344 3745 7403</th>	F10	PCI_SERR_L	INT	2344 3745 7403
STOP* <th>D16</th> <th>PCI_STOP_L</th> <th>INT</th> <th>2344 3745 7403</th>	D16	PCI_STOP_L	INT	2344 3745 7403
TRDY* <th>C9</th> <th>PCI_TRDY_L</th> <th>INT</th> <th>2344 3745 7403</th>	C9	PCI_TRDY_L	INT	2344 3745 7403
FRAME* <th>A17</th> <th>PCI_FRAME_L</th> <th>INT</th> <th>2344 3745 7403</th>	A17	PCI_FRAME_L	INT	2344 3745 7403
PLTRST* <th>A24</th> <th>PLT_RST_L</th> <th>INT</th> <th>3704 6706</th>	A24	PLT_RST_L	INT	3704 6706
PCICKL <th>B10</th> <th>PCI_CLK33M_SB</th> <th>INT</th> <th>29A5 29B3 75B3</th>	B10	PCI_CLK33M_SB	INT	29A5 29B3 75B3
INT PU	A7	TP_PCI_PME_L	INT	29A5 29B3 75B3

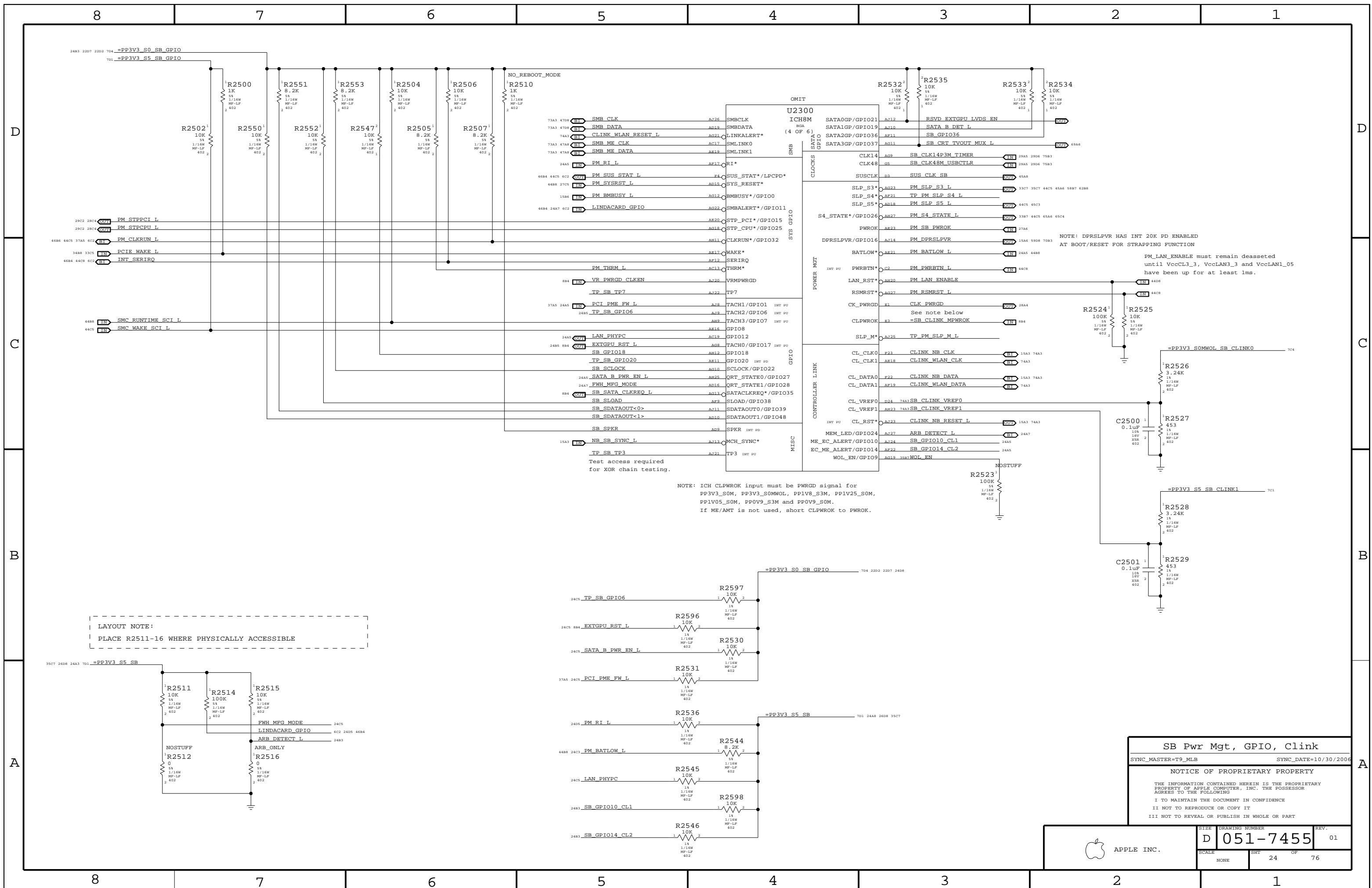
INTERRUPT I/F	PIRQA*	F9	INT_PIROA_L	INT	2344 7403
	BS	PIRQB*	INT_PIROB_L	INT	2344 7403
	CS	PIROC*	INT_PIROC_L	INT	68A4 68B8
	A10	PIROD*	INT_PIROD_L	INT	2344 39C8
	F8	INT_PIROE_L	INT	2344 7403	
	A11	INT_PIROF_L	INT	2344 7403	
	A12	DVI_HOTPLUG_DET	INT	68A4 68B8	
	A13	ODD_PWR_EN_L	INT	2344 39C8	

Provide a pull-down on this GPIO if not used.



SB PCI, PCIe, DMI, USB  
SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006

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U2300 Pin	Signal	U2300 Pin	Signal
73A3 4708	SMB_CLK	AJ26	SMBCLK
73A3 4708	SMB_DATA	AD19	SMBDATA
74A3	CLINK_WLAN_RESET_L	AG21	LINKALERT*
73A3 47A8	SMB_MF_CLK	AC17	SMLINK0
73A3 47A8	SMB_MF_DATA	AE19	SMLINK1
24A5	PM_RI_L	AF17	RI*
46B4 44C5 6C2	PM_SUS_STAT_L	E4	SUS_STAT*/LPCPD*
4488 27C5	PM_SYSRST_L	AD18	SYS_RESET*
15B6	PM_BMBUSY_L	AG12	BMBUSY*/GPIO0
46B4 24A7 6C2	LINDACARD_GPIO	AG22	SMBALERT*/GPIO11
		AE20	STP_PCI*/GPIO15
		AG18	STP_CPU*/GPIO25
		AM14	CLKRUN*/GPIO32
		AE12	WAKE*
		AE12	SERIRQ
		AC13	THRM*
8B4	VR_PWRGD_CLKEN	AJ20	VRMPWRGD
		AJ22	TP7
37A5 24A5	PCI_PME_FW_L	AJ8	TACH1/GPIO1 INT PU
24B5	TP_SB_GPIO6	AJ9	TACH2/GPIO6 INT PU
		AM9	TACH3/GPIO7 INT PU
		AE16	GPIO8
24A5 8B4	LAN_PHYPC	AC19	GPIO12
24B5 8B4	EXTGPU_RST_L	AG8	TACH0/GPIO17 INT PU
		AM12	GPIO18
		AE11	GPIO20 INT PU
		AG10	SCLOCK/GPIO22
24A5	SATA_B_PWR_EN_L	AD25	QRT_STATE0/GPIO27
24A7	FWH_MFG_MODE	AD16	QRT_STATE1/GPIO28
8B4	SB_SATA_CLKREQ_L	AG13	SATACLKREQ*/GPIO35
		AE9	SLOAD/GPIO38
		AD11	SDATAOUT0/GPIO39
		AD10	SDATAOUT1/GPIO48
		AD9	SPKR INT PU
15A3	NB_SB_SYNC_L	AJ13	MCH_SYNC*
		AJ21	TP3 INT PU

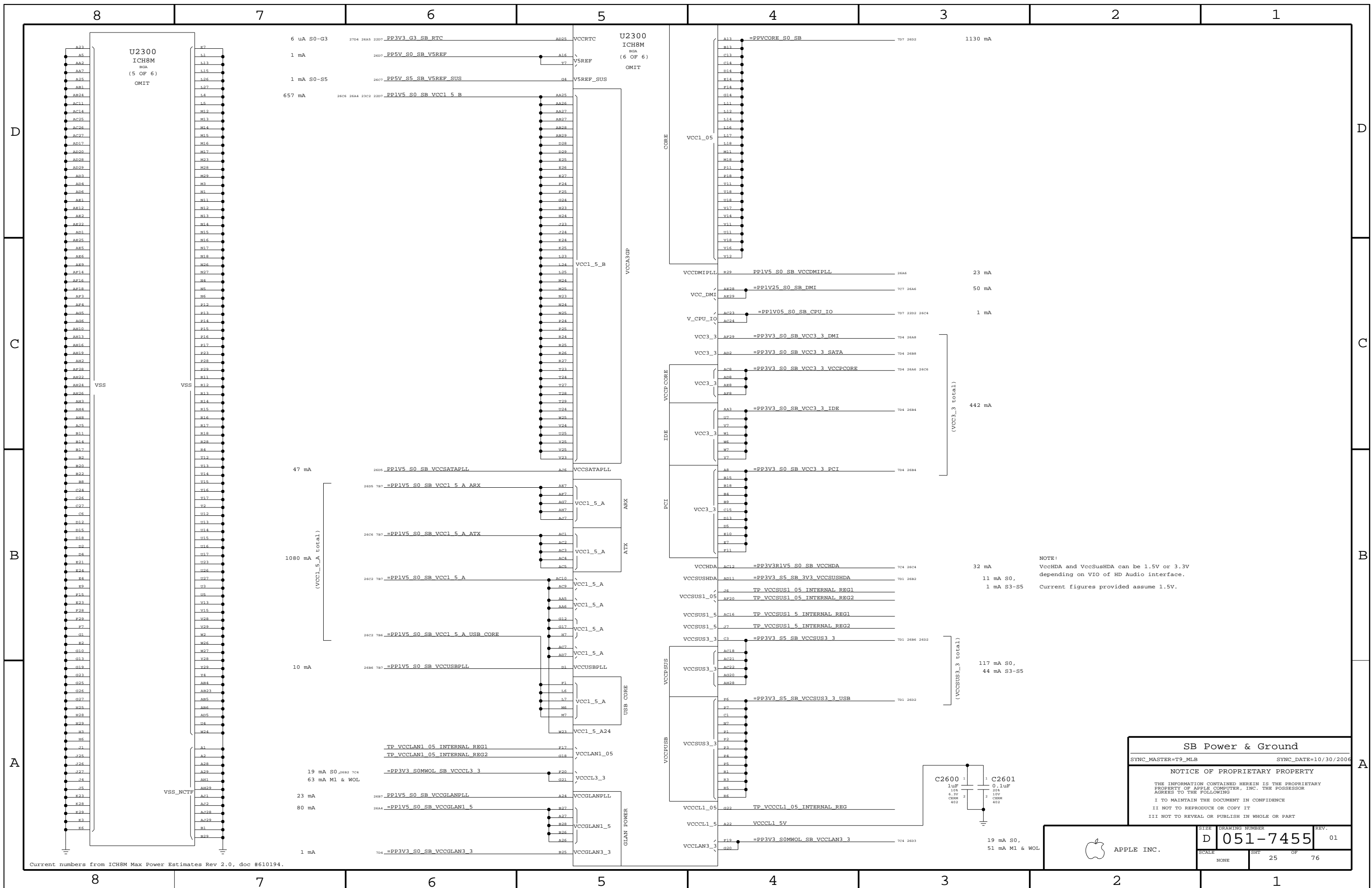
NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3\_SOM, PP3V3\_SOMWOL, PP1V8\_S3M, PP1V25\_SOM, PP1V05\_SOM, PPOV9\_S3M and PPOV9\_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

LAYOUT NOTE:  
PLACE R2511-16 WHERE PHYSICALLY ACCESSIBLE

**SB Pwr Mgt, GPIO, Clink**  
 SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006  
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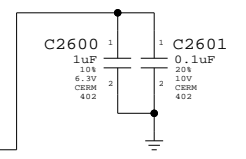
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	SHT	OF	76
NONE	24		

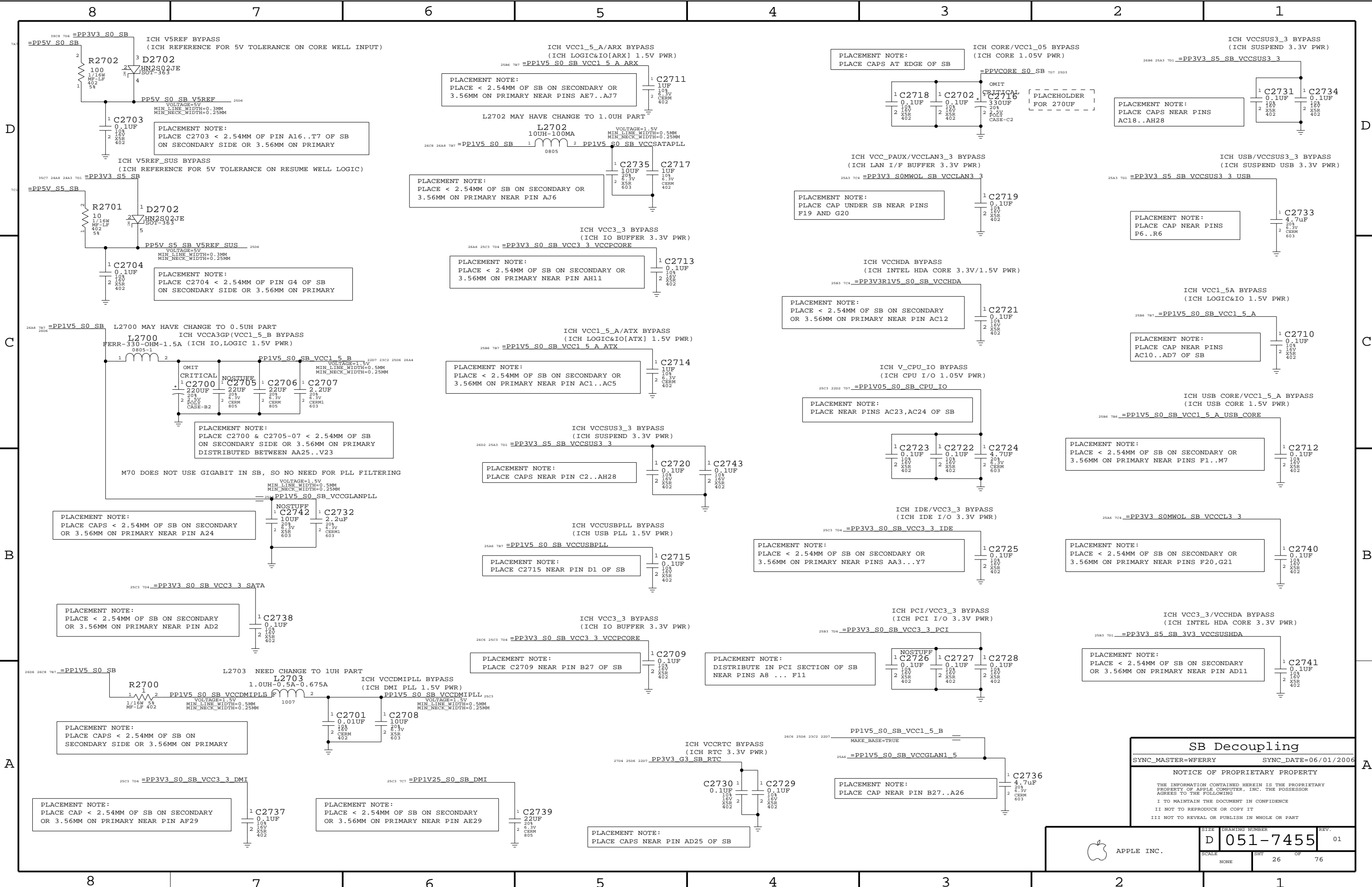




Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

NOTE:  
 VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.  
 Current figures provided assume 1.5V.





**SB Decoupling**

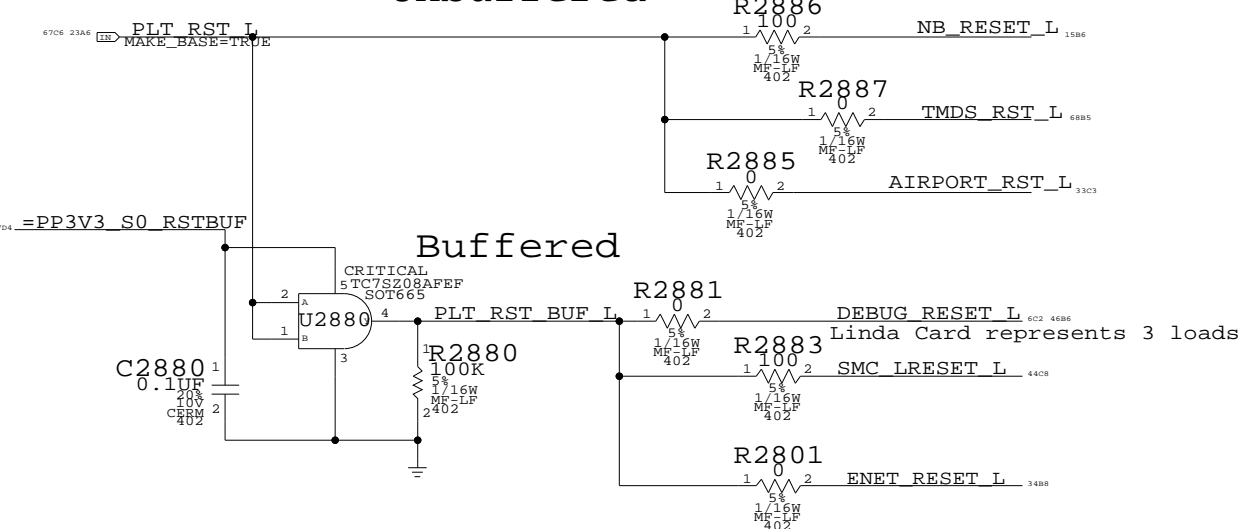
SYNC\_MASTER=WFERRY SYNC\_DATE=06/01/2006

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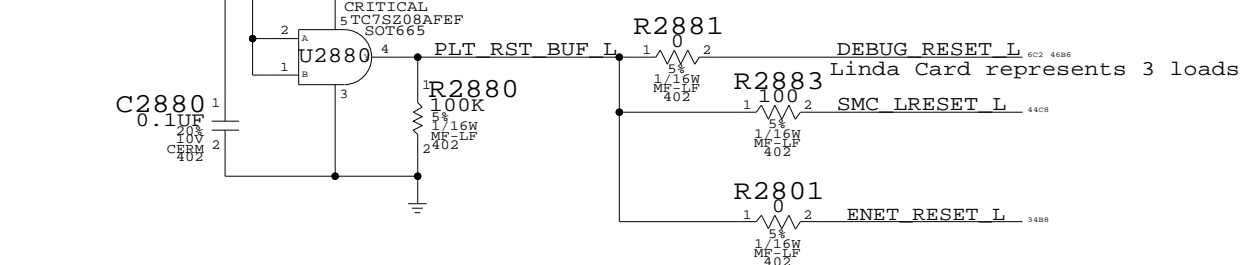
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
		26	76

# Platform Reset Connections

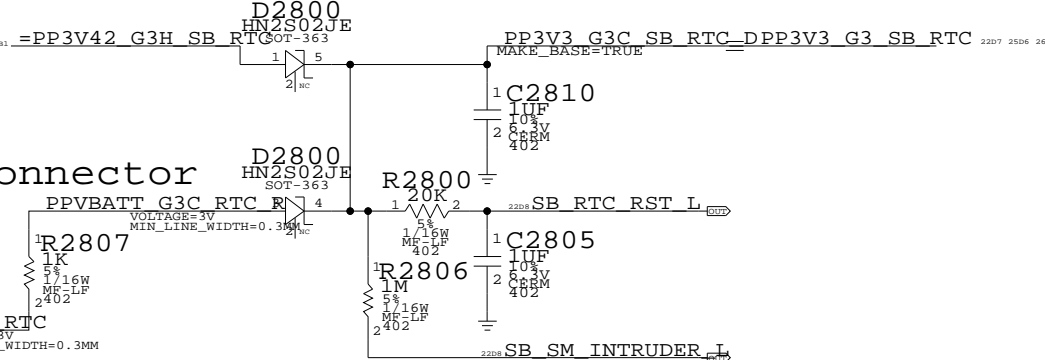
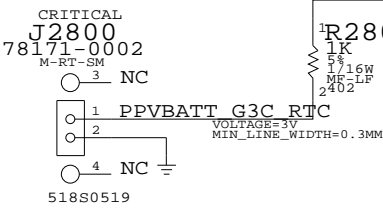
## Unbuffered



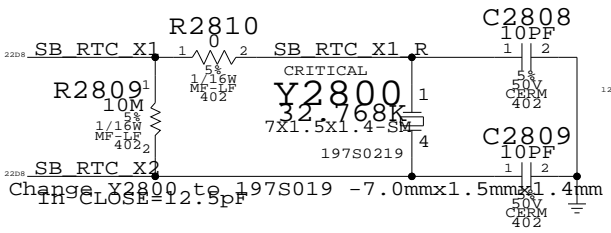
## Buffered



## RTC Battery Connector

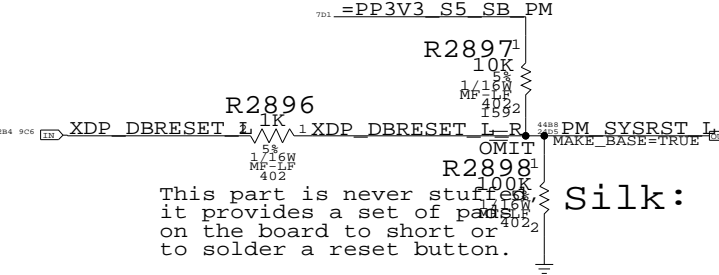


## SB RTC Crystal Circuit

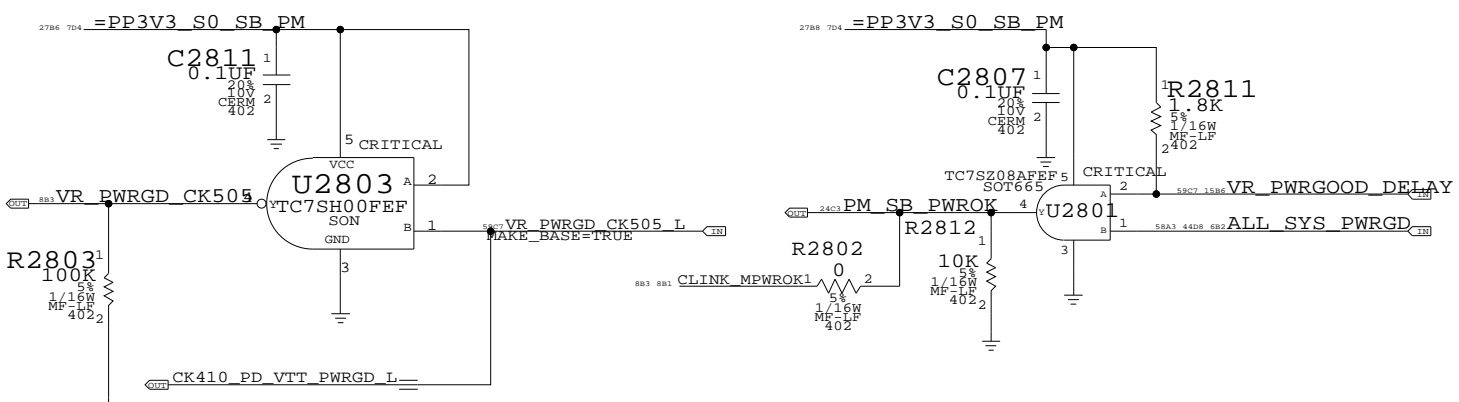
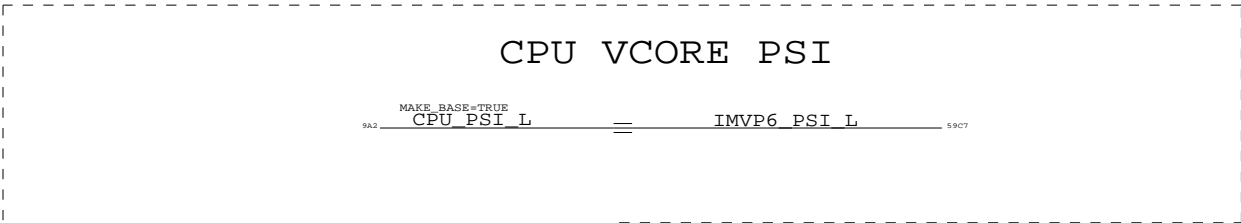


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"



## CPU VCORE PSI



Pulled a new APN for U2803(0.6mm max 2-input NAND gate-APN:311S0304 It may take a few days before this is done through This will allow us to sequence this part under wireless card

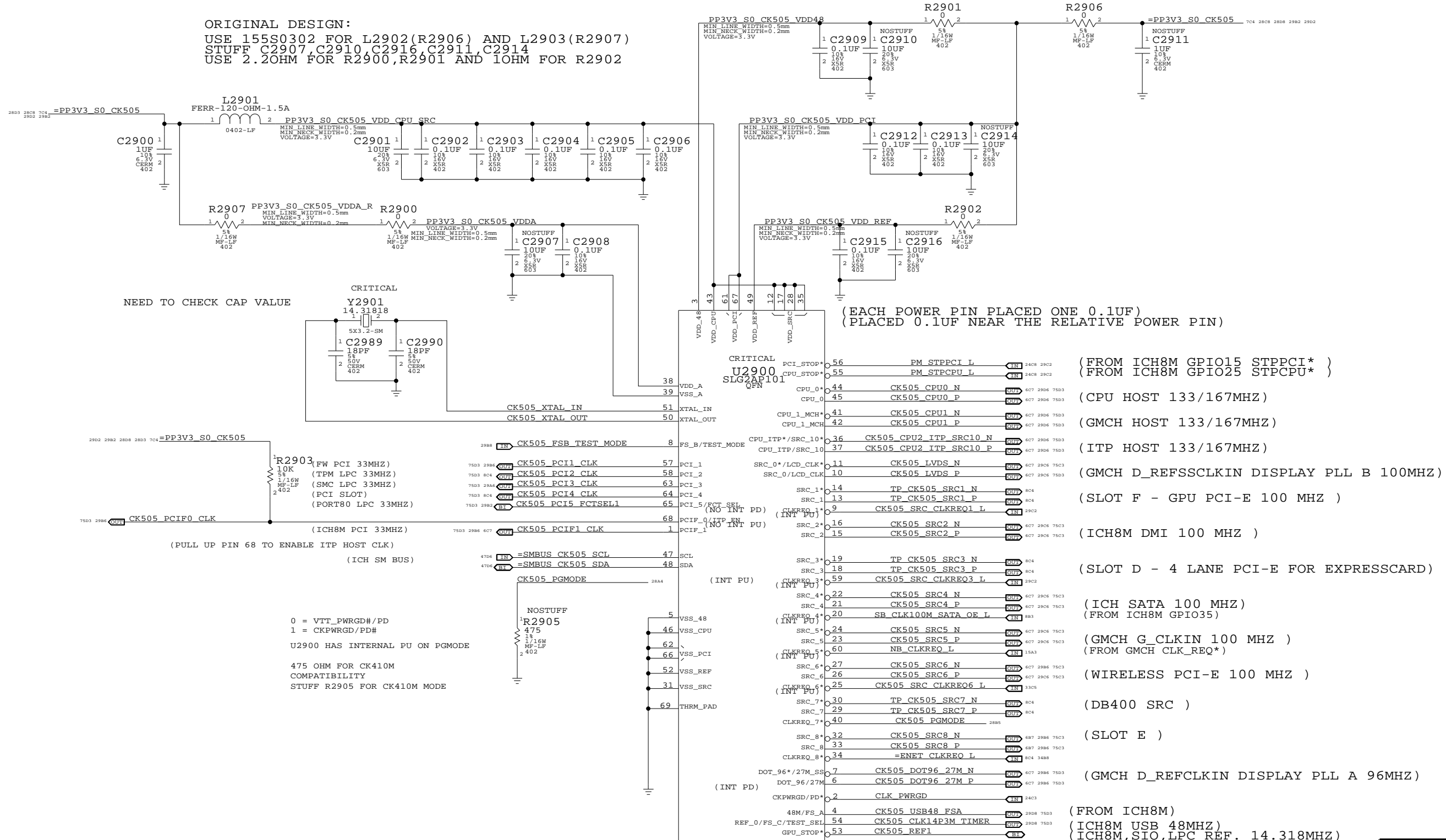
Initial resistor values are based on CRB, but may change after characterization.

<b>SB Misc</b>	
SYNC_MASTER=NB	SYNC_DATE=07/26/2005
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	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		27	76

SELIGO RECOMMEND TO REMOVE L2903,R2900,C2907,C2910  
R2901,L2902,C2916,C2911,C2914 and R2902

ORIGINAL DESIGN:  
USE 155S0302 FOR L2902(R2906) AND L2903(R2907)  
STUFF C2907,C2910,C2916,C2911,C2914  
USE 2.2OHM FOR R2900,R2901 AND 1OHM FOR R2902



NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)  
(ICH8M PCI 33MHZ)  
(ICH SM BUS)

0 = VTT\_PWRGD#/PD  
1 = CKPWRGD/PD#  
U2900 HAS INTERNAL PU ON PGMODE  
475 OHM FOR CK410M  
COMPATIBILITY  
STUFF R2905 FOR CK410M MODE

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM  
\* FOR EXT. GRAPHIC SYSTEM

- (FROM ICH8M GPIO15 STPPCI\* )
- (FROM ICH8M GPIO25 STPCPU\* )
- (CPU HOST 133/167MHZ)
- (GMCH HOST 133/167MHZ)
- (ITP HOST 133/167MHZ)
- (GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)
- (SLOT F - GPU PCI-E 100 MHZ )
- (ICH8M DMI 100 MHZ )
- (SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
- (ICH SATA 100 MHZ)  
(FROM ICH8M GPIO35)
- (GMCH G\_CLKIN 100 MHZ )  
(FROM GMCH CLK\_REQ\*)
- (WIRELESS PCI-E 100 MHZ )
- (DB400 SRC )
- (SLOT E )
- (GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)
- (FROM ICH8M)
- (ICH8M USB 48MHZ)
- (ICH8M,SIO,LPC REF. 14.318MHZ)

**Clock (CK505)**

SYNC\_MASTER=DSIMON      SYNC\_DATE=06/06/2006

NOTICE OF PROPRIETARY PROPERTY

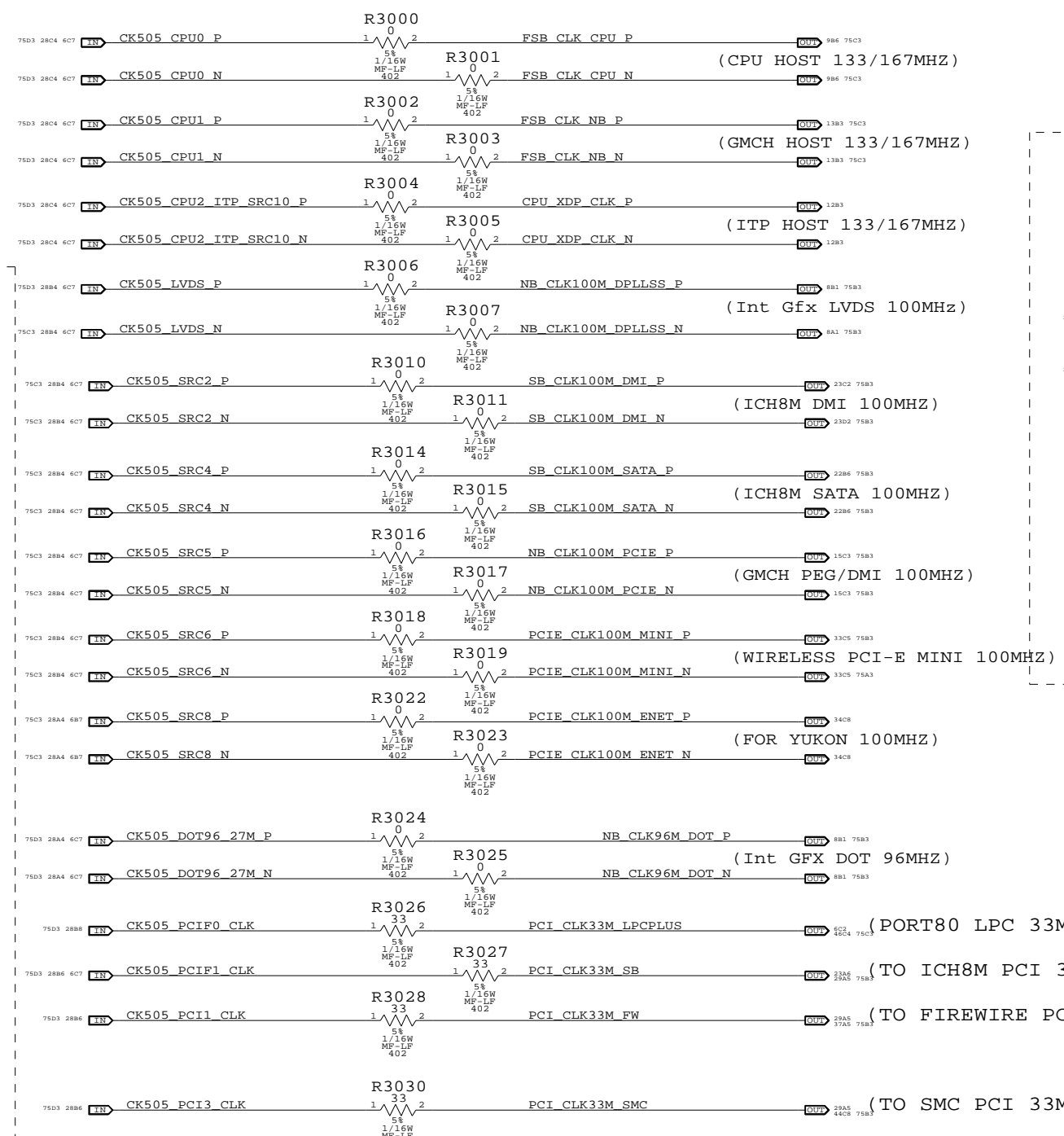
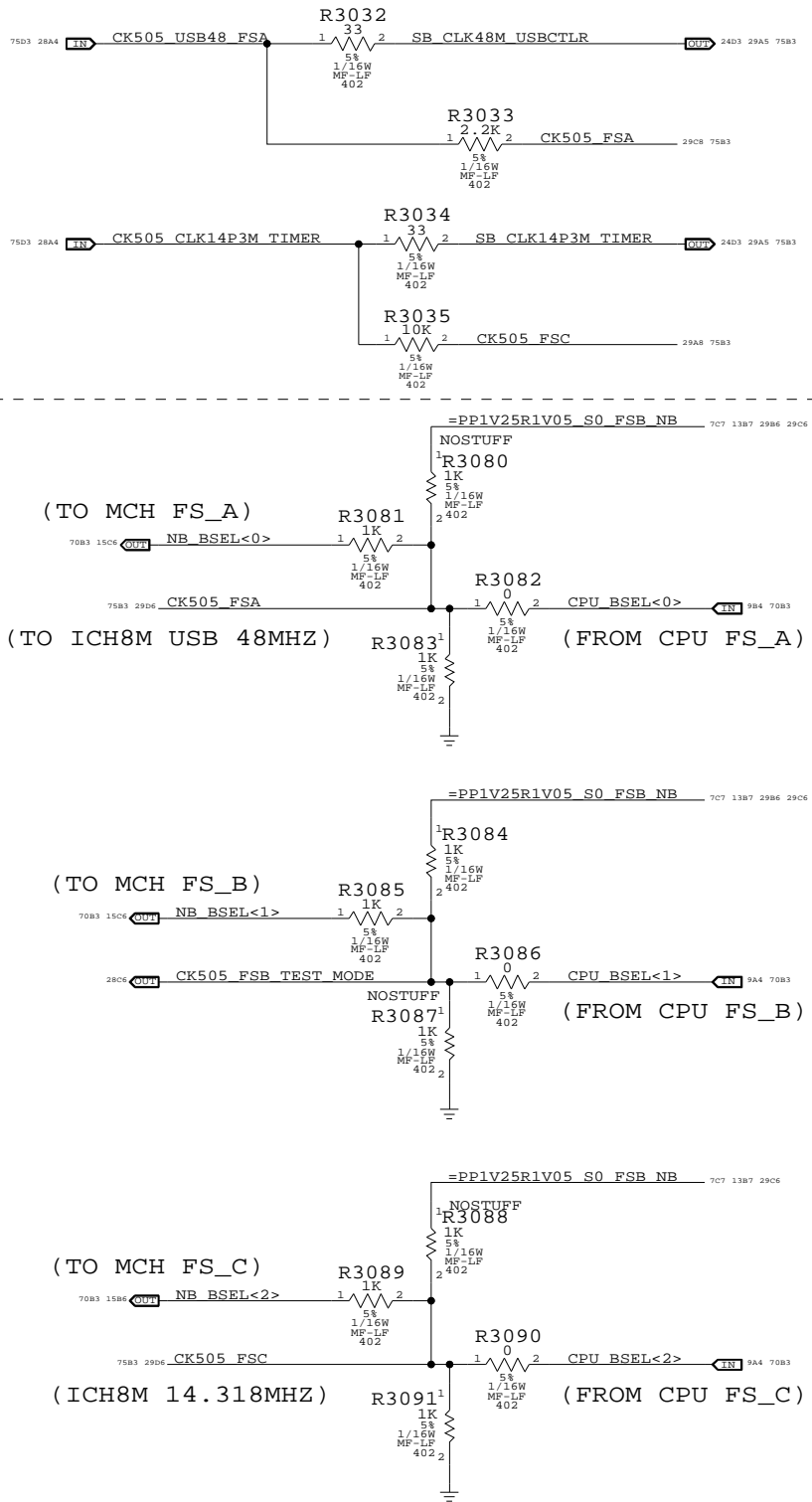
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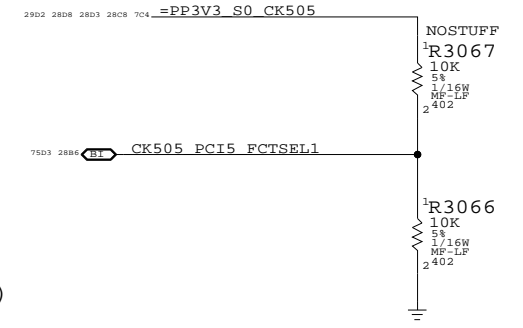
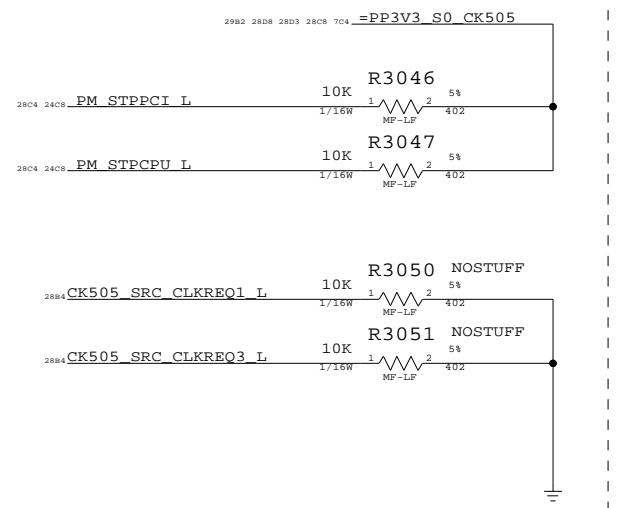
APPLE INC.

SCALE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
SHEET	28	OF 76

# CLK Termination

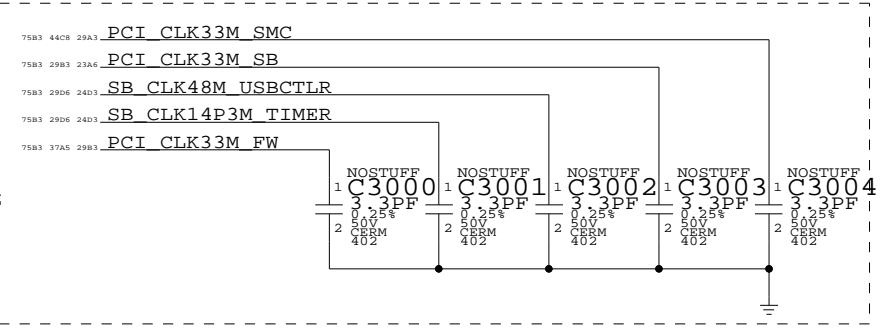


# CLKREQ Controls



FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	1	166M
0	1	0	200M
1	1	0	400M
1	1	1	Resrvd
1	0	1	100M
1	0	0	333M

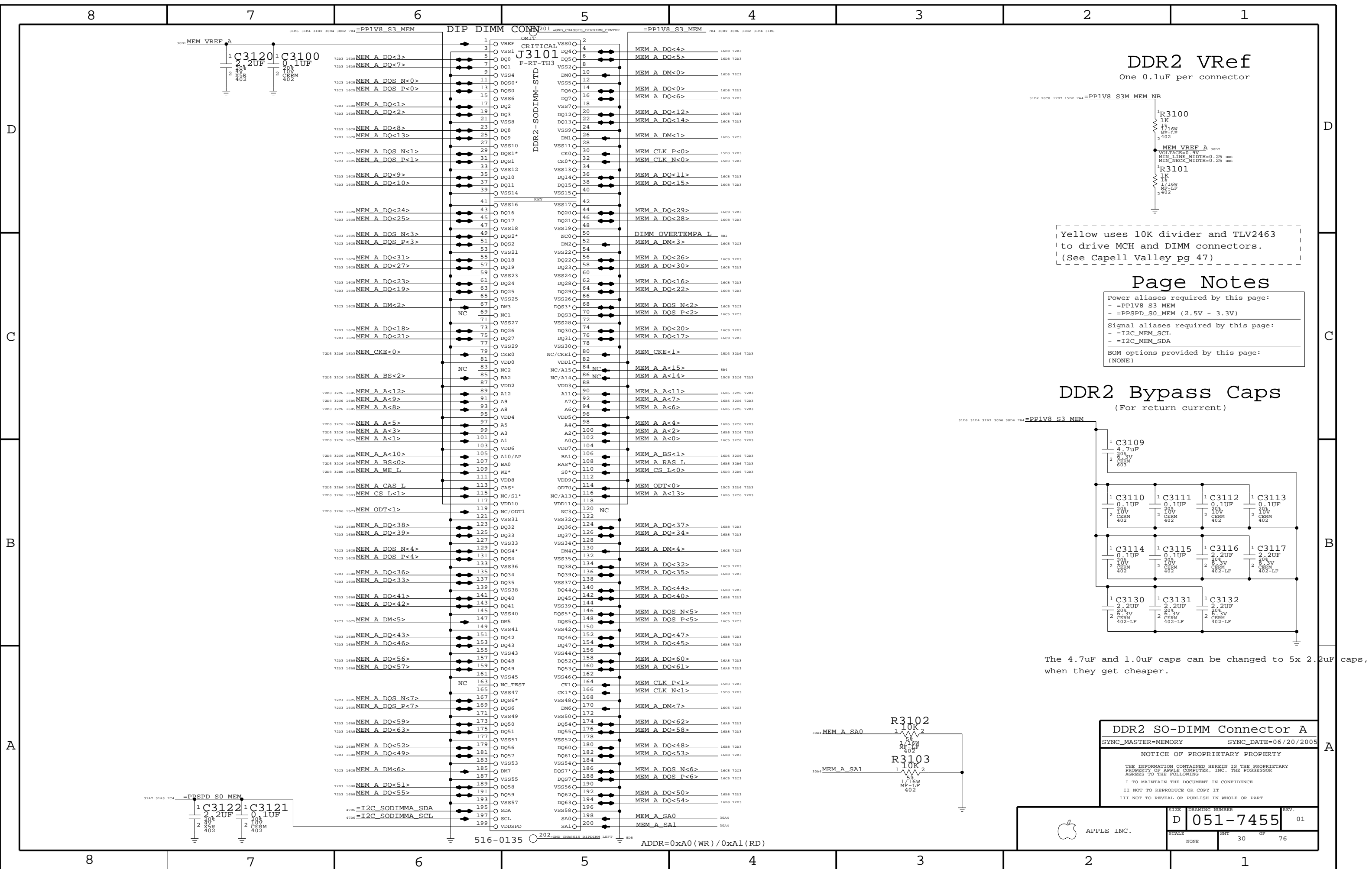
NOSTUFF R3082, R3086, R3090  
FOR MANUAL CPU FREQUENCY  
CPU speed is currently set to 200MHZ



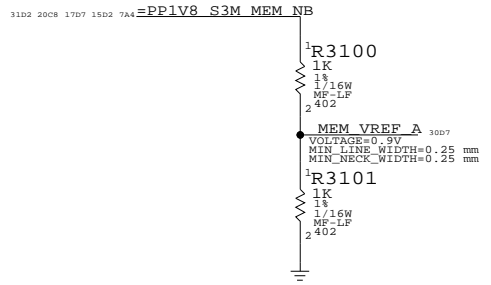
Place close to CLK Gen  
For reducing noise coupling to wireless frequencies

**Clock Termination**  
 SYNC\_MASTER=DSIMON-WF      SYNC\_DATE=06/06/2006  
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APPLE INC.      DRAWING NUMBER: D 051-7455      REV. 01  
 SCALE: NONE      SHEET: 29 OF 76



DDR2 VRef  
One 0.1uF per connector

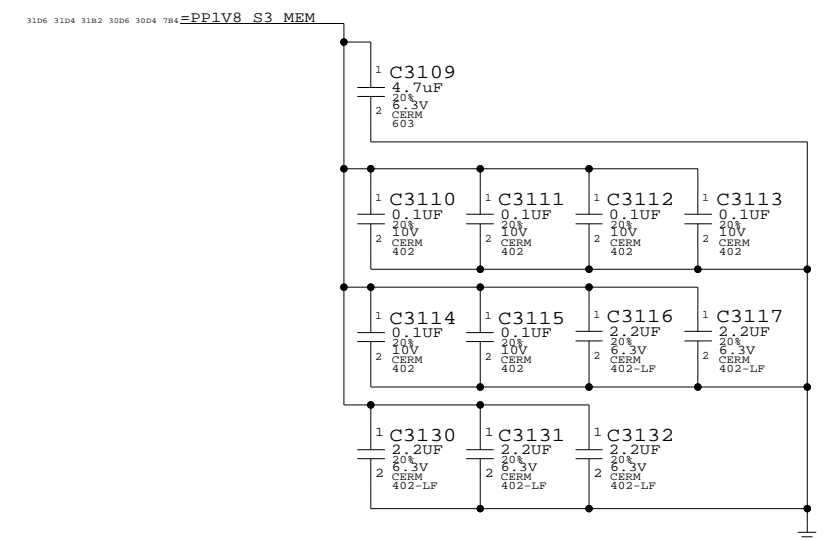


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

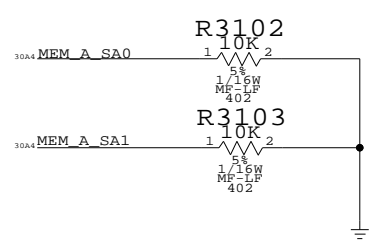
Page Notes

- Power aliases required by this page:
  - =PP1V8\_S3\_MEM
  - =PPSPD\_S0\_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
  - =I2C\_MEM\_SCL
  - =I2C\_MEM\_SDA
- BOM options provided by this page: (NONE)

DDR2 Bypass Caps  
(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



**DDR2 SO-DIMM Connector A**  
 SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005  
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 SCALE: NONE SHT: 30 OF 76

8

7

6

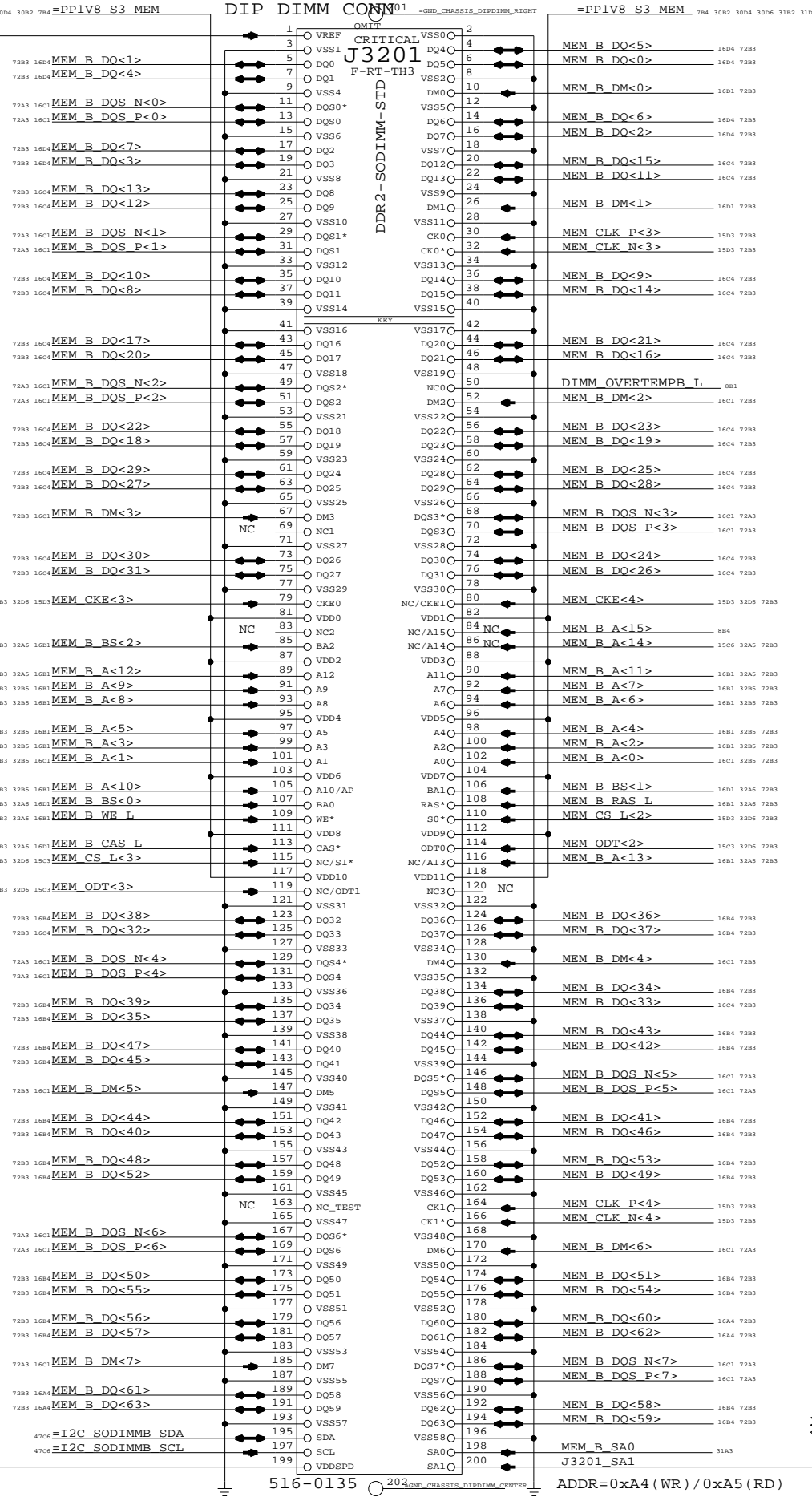
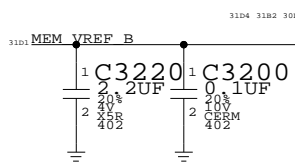
5

4

3

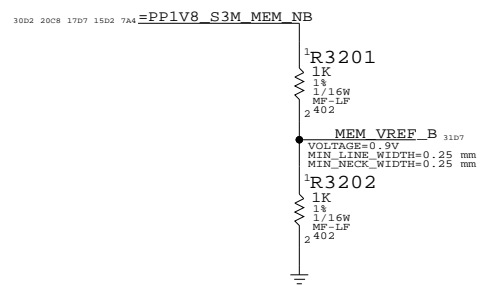
2

1



# DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector

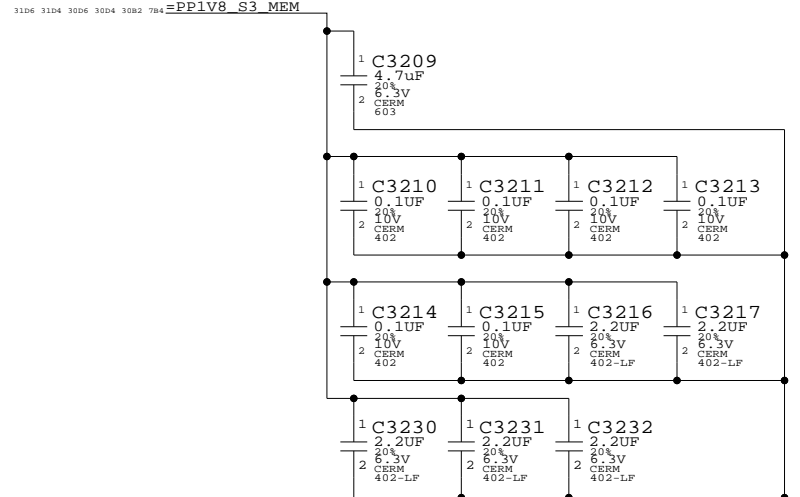


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

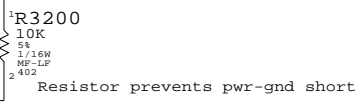
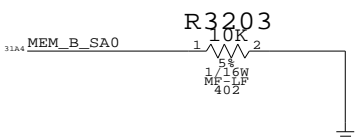
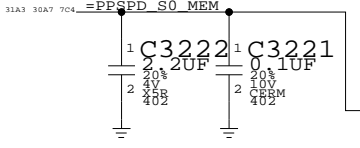
## Page Notes

- Power aliases required by this page:
  - =PPIV8\_S3\_MEM
  - =PPSPD\_S0\_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
  - =I2C\_MEM\_SCL
  - =I2C\_MEM\_SDA
- BOM options provided by this page: (NONE)
- NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

## DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.



## DDR2 SO-DIMM Connector B

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

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APPLE INC.	SIZE: D DRAWING NUMBER: 051-7455 REV.: 01
	SCALE: NONE SHT: 31 OF 76

8

7

6

5

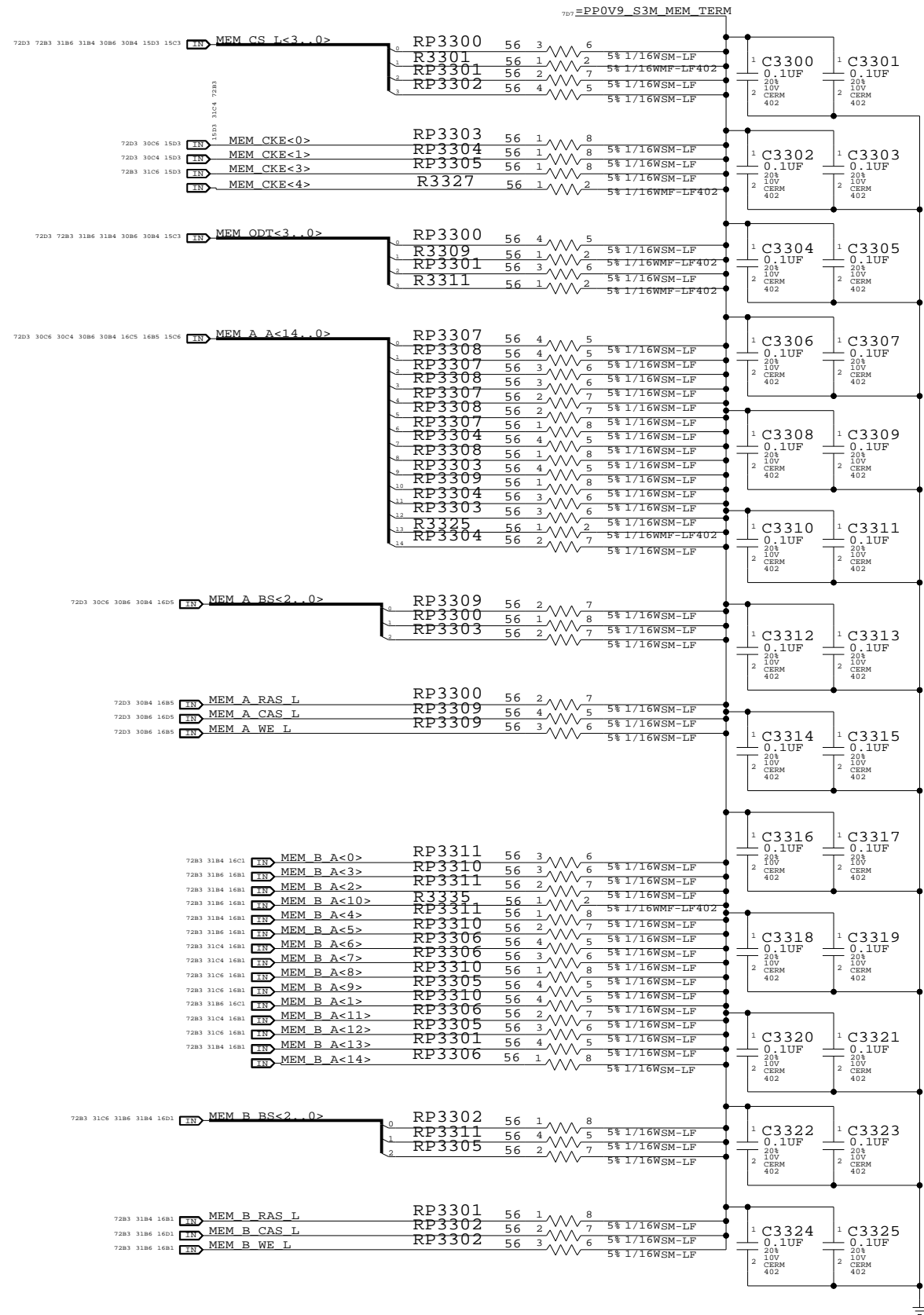
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
 BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9\_S0\_MEM\_TERM

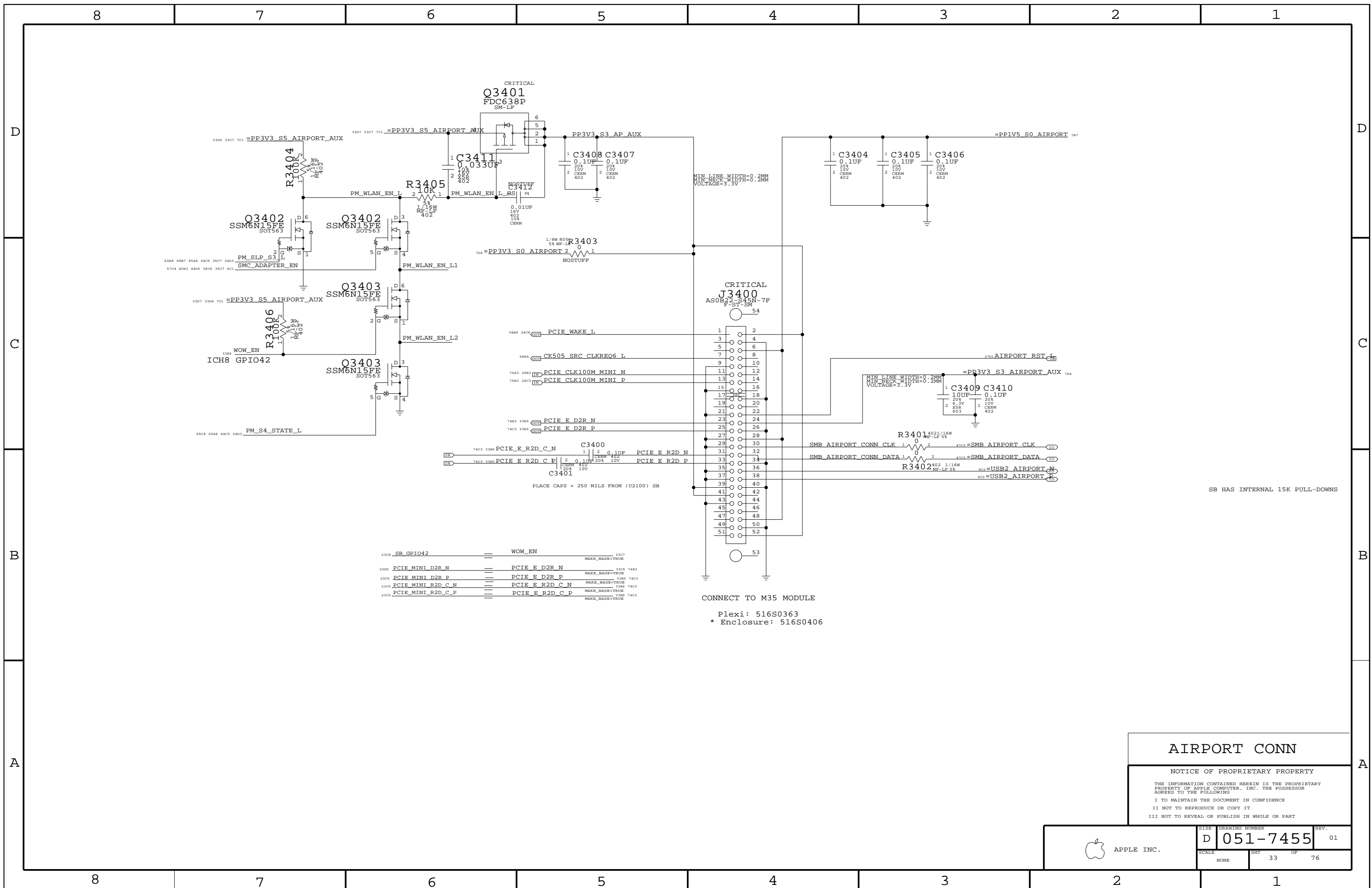
Memory Active Termination

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7455	REV. 01
	SCALE NONE	SHT 32	OF 76





# AIRPORT CONN

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SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	33	76

# Page Notes

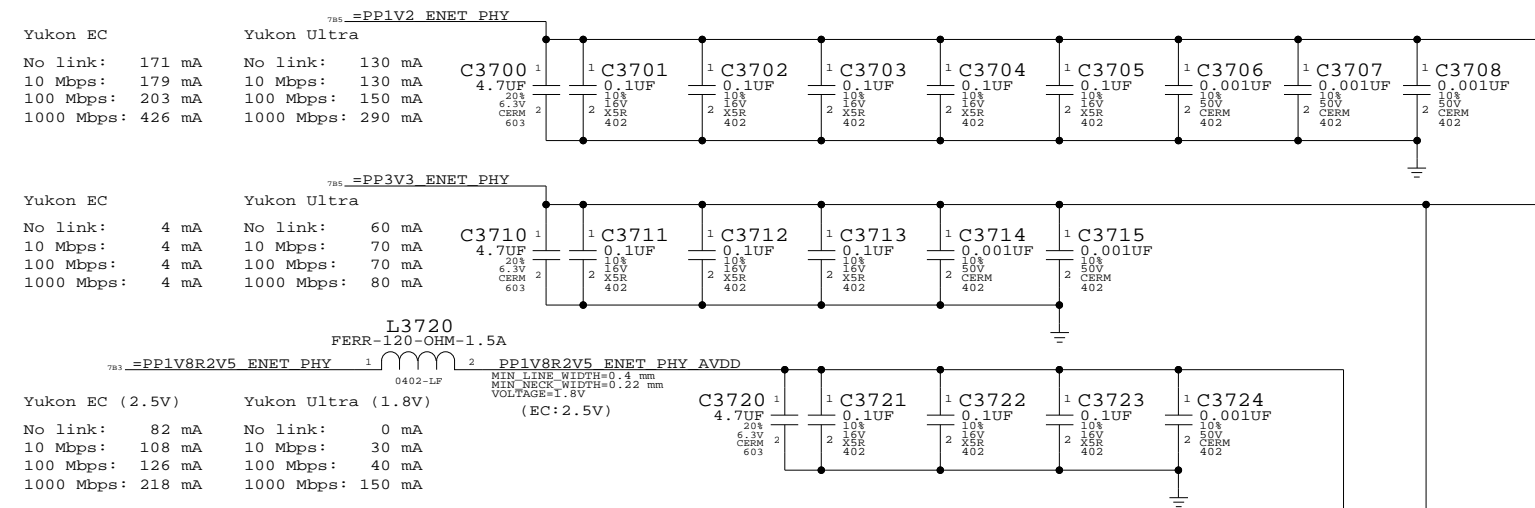
Power aliases required by this page:  
 - =PP3V3\_ENET\_PHY (EC / Ultra)  
 - =PP1V8R2V5\_ENET\_PHY (2.5V / 1.8V)  
 - =YUKON\_EC\_PP2V5\_ENET (2.5V / GND)  
 - =PP1V2\_ENET\_PHY

Signal aliases required by this page:  
 - =ENET\_CLKREQ\_L (NC/TP for Yukon EC)  
 - =ENET\_VMAIN\_AVLBL

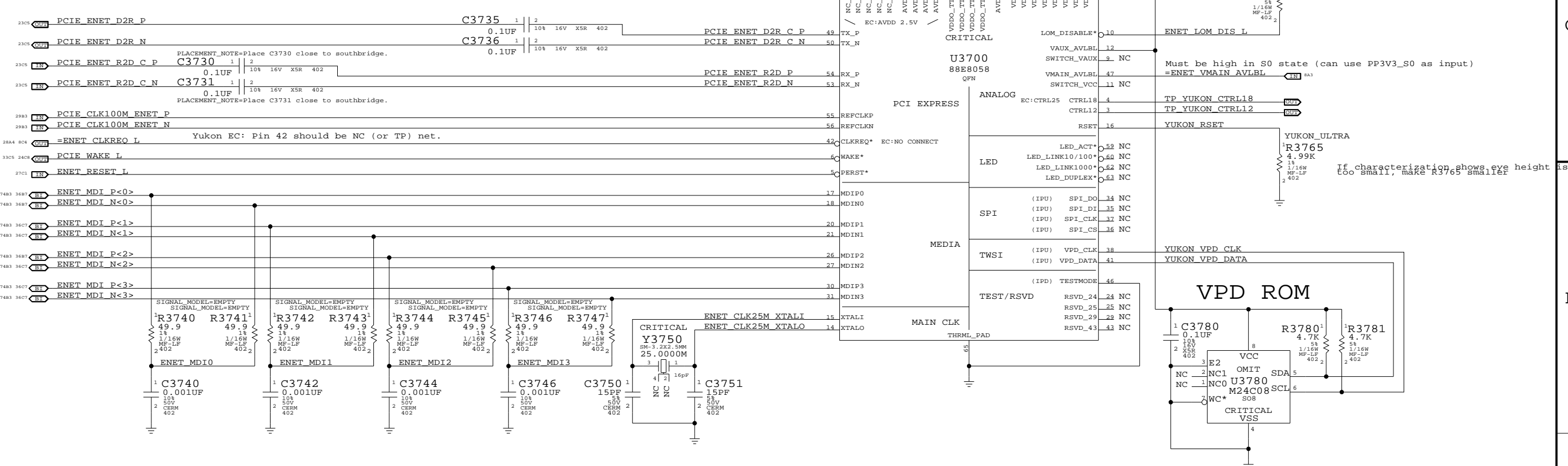
BOM options provided by this page:  
 YUKON\_EC - Selects Yukon EC RSET value.  
 YUKON\_ULTRA - Selects Yukon Ultra RSET.

NOTE: Yukon IC and EEPROM are OMITTED on this page. Proper part numbers must be called out elsewhere.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



**784 =YUKON\_EC\_PP2V5\_ENET**  
 Yukon EC: Alias to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF & 1x 0.001uF caps  
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:  
 - Alias =YUKON\_EC\_PP2V5\_ENET to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF and 1x 0.001uF caps  
 - Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5\_ENET\_PHY  
 - Connect =ENET\_CLKREQ\_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON\_ULTRA)  
 - Use YUKON\_EC and YUKON\_ULTRA BOMOPTIONS to select stuffed part

**Ethernet (Yukon)**  
 SYNC\_MASTER=USB SYNC\_DATE=10/07/2006

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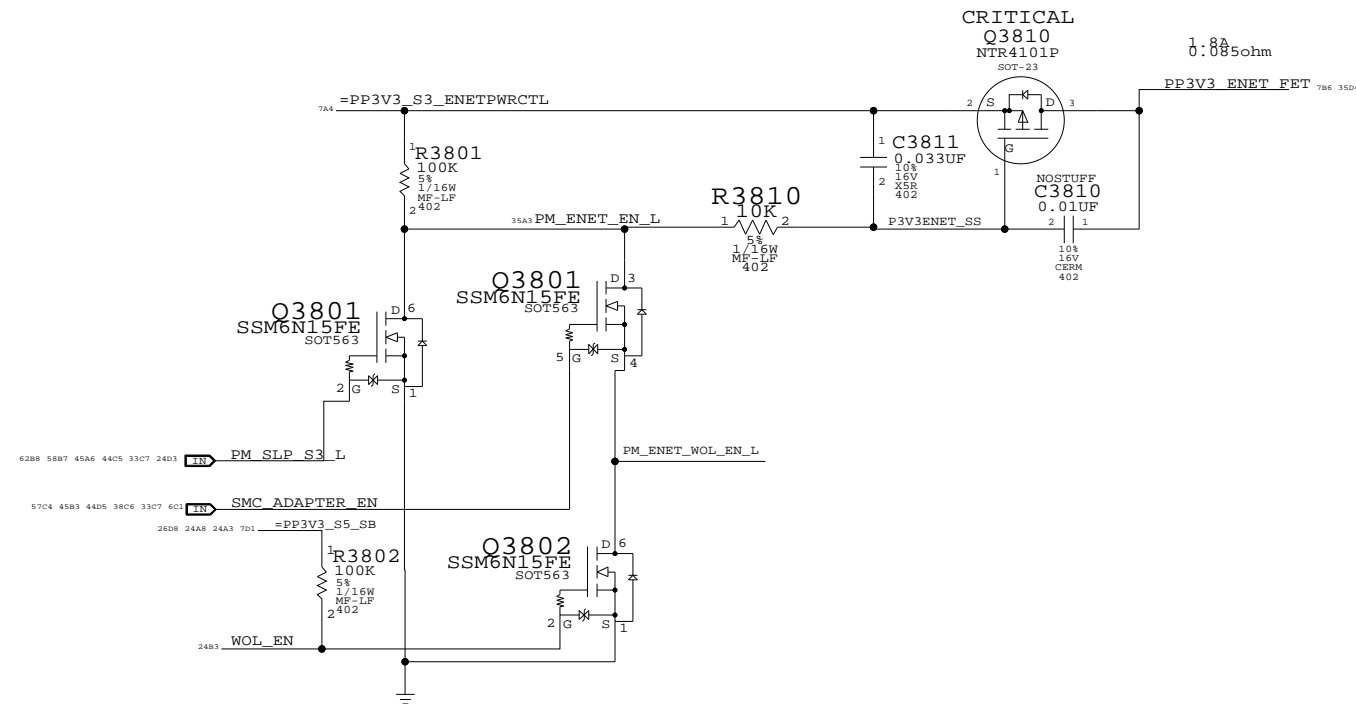
SIZE DRAWING NUMBER REV. 01  
**D 051-7455**

SCALE NONE SHEET 34 OF 76

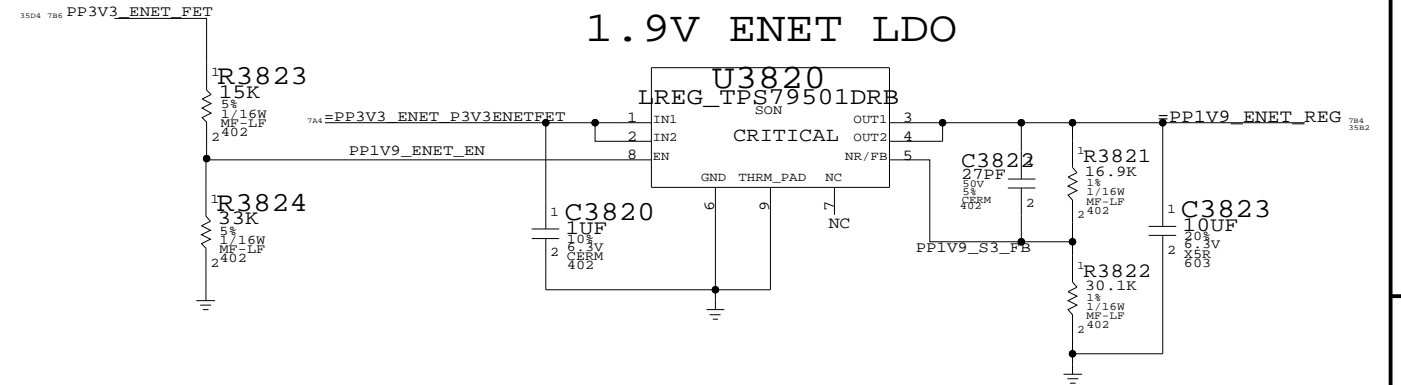
# ENET Enable Generation

"ENET" = "S0" || AC

## 3.3V ENET FET

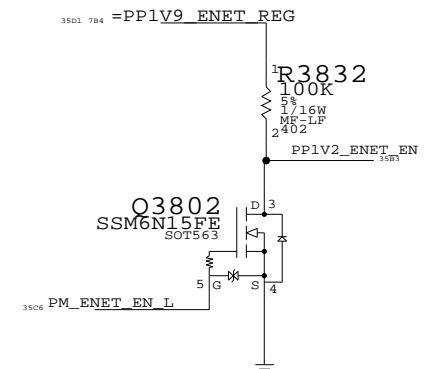
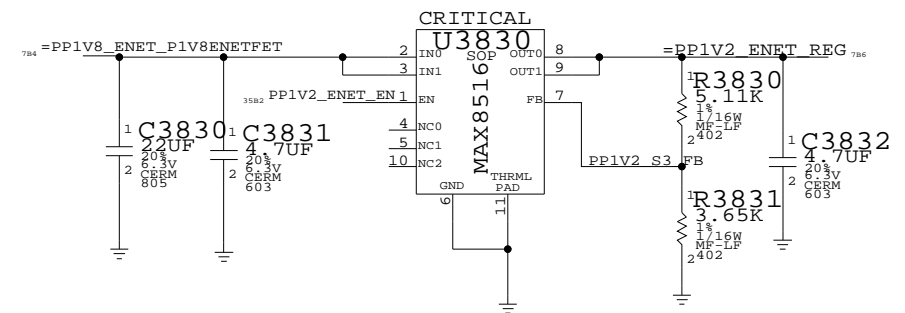


Name	PM_SLP_S3_L	SMC_ADAPTER_EN	PM_ENET_EN_L	PM_ENET_EN	Yukon Power
Logic	S0	AC			Powered by S3
S0 on Battery	High (3.3V)	Low (0V)	Low (0V)	High (3.3V)	Power
S3 on Battery	Low (0V)	Low (0V)	High (3.3V)	Low (0V)	Power
S0 on AC	High (3.3V)	High (3.3V)	Low (0V)	High (3.3V)	Power
S3 on AC	Low (0V)	High (3.3V)	Low (0V)	High (3.3V)	Power
S5 on anything	N/A	N/A	N/A	N/A	No Power



$$V_{out} = 1.2246V * (1 + R3821 / R3822)$$

## 1.2V ENET LDO

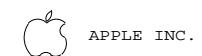


### Yukon Power Control

SYNC\_MASTER=USB SYNC\_DATE=10/07/2006

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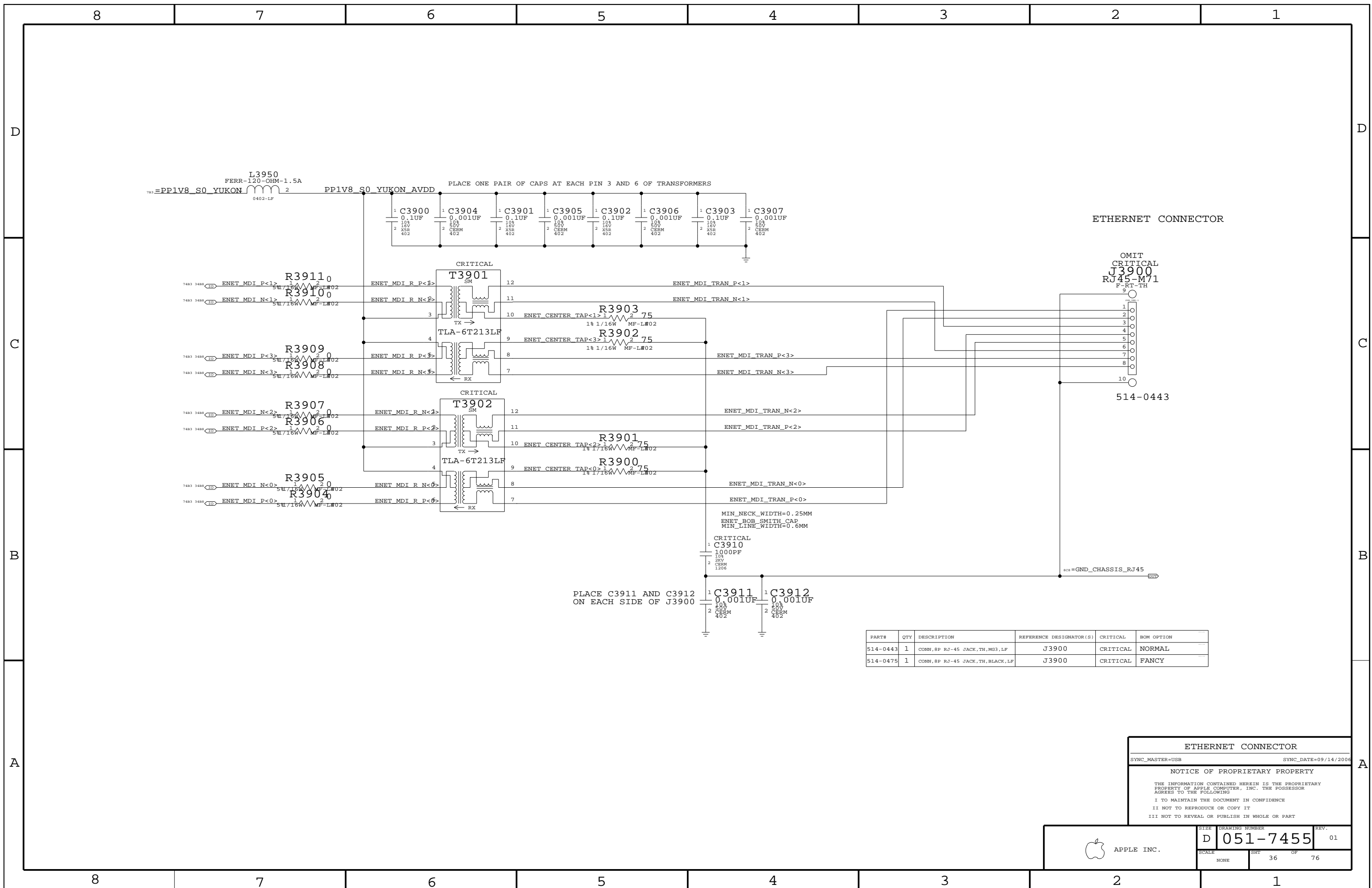


APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE SHEET OF 35 OF 76



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0443	1	CONN, 8P RJ-45 JACK, TH, MG3, LF	J3900	CRITICAL	NORMAL
514-0475	1	CONN, 8P RJ-45 JACK, TH, BLACK, LF	J3900	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC\_MASTER=USB SYNC\_DATE=09/14/2006

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APPLE INC.

SCALE NONE

SHEET 36 OF 76

SIZE D

DRAWING NUMBER 051-7455

REV. 01

PAGE NOTES

INPUT
=PP3V3\_S0\_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3\_S0\_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI\_GNT3\_L - PCI GRANT FROM SB
PCI\_CLK\_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI\_RST\_L - PCI RESET FROM SB
FW\_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT
PCI\_AD<0..31>, PCI\_C\_BE\_L<0..3>, PCI\_FRAME\_L, PCI\_IRDY\_L, PCI\_TRDY\_L,
PCI\_DEVSEL\_L, PCI\_STOP\_L, PCI\_PAR, PCI\_PERR\_L, PCI\_SERR\_L
FW\_A\_TPA\_P/N, FW\_A\_TPB\_P/N, FW\_A\_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW\_B\_TPA\_P/N, FW\_B\_TPB\_P/N, FW\_B\_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW\_C\_TPA\_P/N, FW\_C\_TPB\_P/N, FW\_C\_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

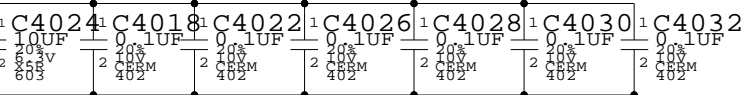
PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/21/2005 - CHANGED PIN # OF FW23-06 ADDED
6/21/2005 - CHANGED PIN # OF FW23-06 ADDED
6/21/2005 - CHANGED PIN # OF FW23-06 ADDED

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

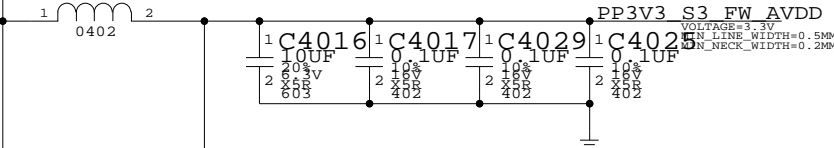
PP3V3\_S3\_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4024 ON VDD0



I4000

600-OHM-300MA PLACE ONE CAP PER TWO PINS STARTING WITH C4016 ON VDDA0

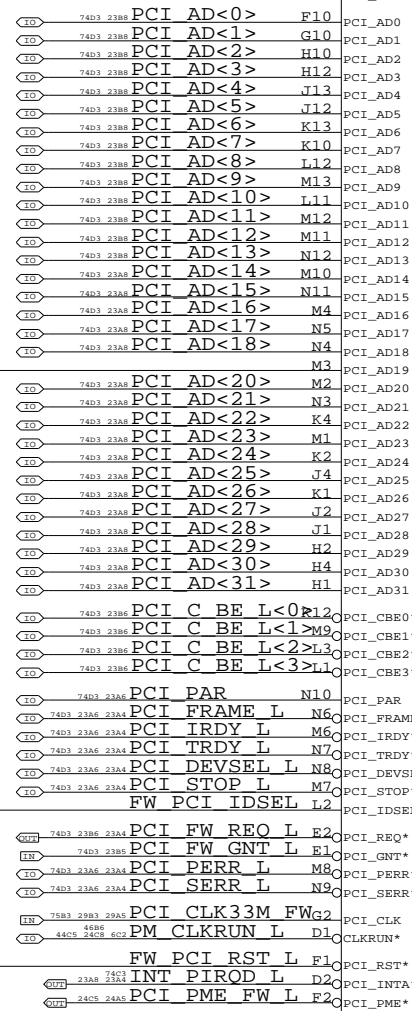


PP3V3\_S3\_FW\_AVDD

VOLTAGE=3.3V
LINE\_WIDTH=0.5MM
NECK\_WIDTH=0.2MM

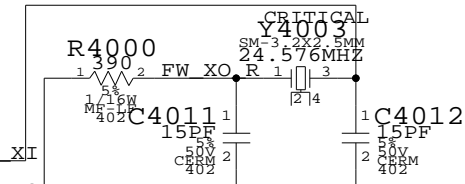
PP3V3\_S3\_PCI

CONNECT TO VDD FOR 3.3V OPERATION

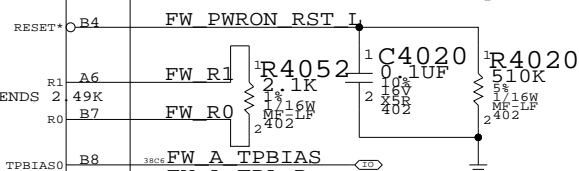


CRITICAL
U4000
FW32306
BGA

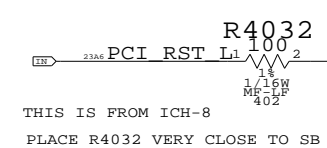
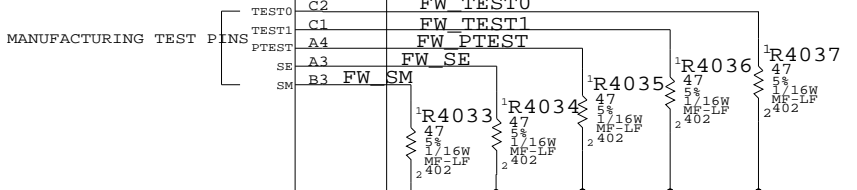
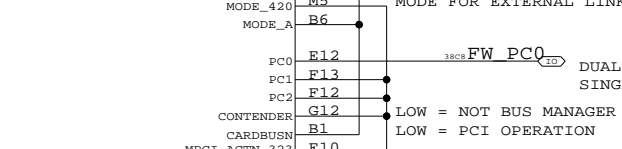
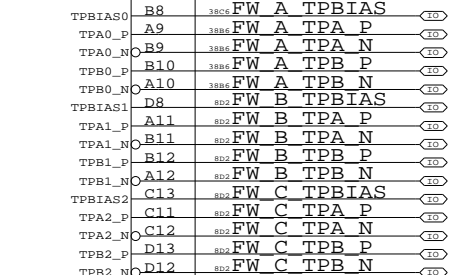
197S0030 3.2MMX2.5MM



NEED TO CHECK CRYSTAL LOAD CAPACITANCE



SPEC RECOMMENDS



FIREWIRE CONTROLLER
SYNC\_MASTER=ENESYNC\_DATE=08/30/2005

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Table with columns: SCALE (NONE), SHEET (37 OF 76), DRAWING NUMBER (D 051-7455), REV. (01)

Page Notes

INPUT:  
 =PPBUS\_FW - PORT POWER  
 =PP3V3\_S5\_FW - DIGITAL POWER  
 =GND\_CHASSIS\_FW\_PORT0 - CHASSIS GROUND  
 =FWPWR\_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:  
 FW\_TPA0\_P/N,FW\_TPBO\_P/N,FW\_TPBIAS0 - FIREWIRE DIFF PAIRS

OUTPUT:  
 FW\_PCO - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

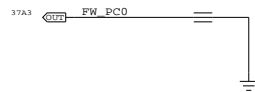
PAGE HISTORY

5/19/05 - INITIAL REVISION  
 6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE  
 6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER  
 6/26/05 - CONNECTED FW\_PCO FOR SINGLE PORT  
 6/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1  
 7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0  
 7/26/05 - SWITCHED TO 514-014 FOR PRE-PROD CONNECTOR  
 7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS  
 7/26/05 - CHANGED FL4590 TO 1.1A VERSION  
 7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT  
 7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

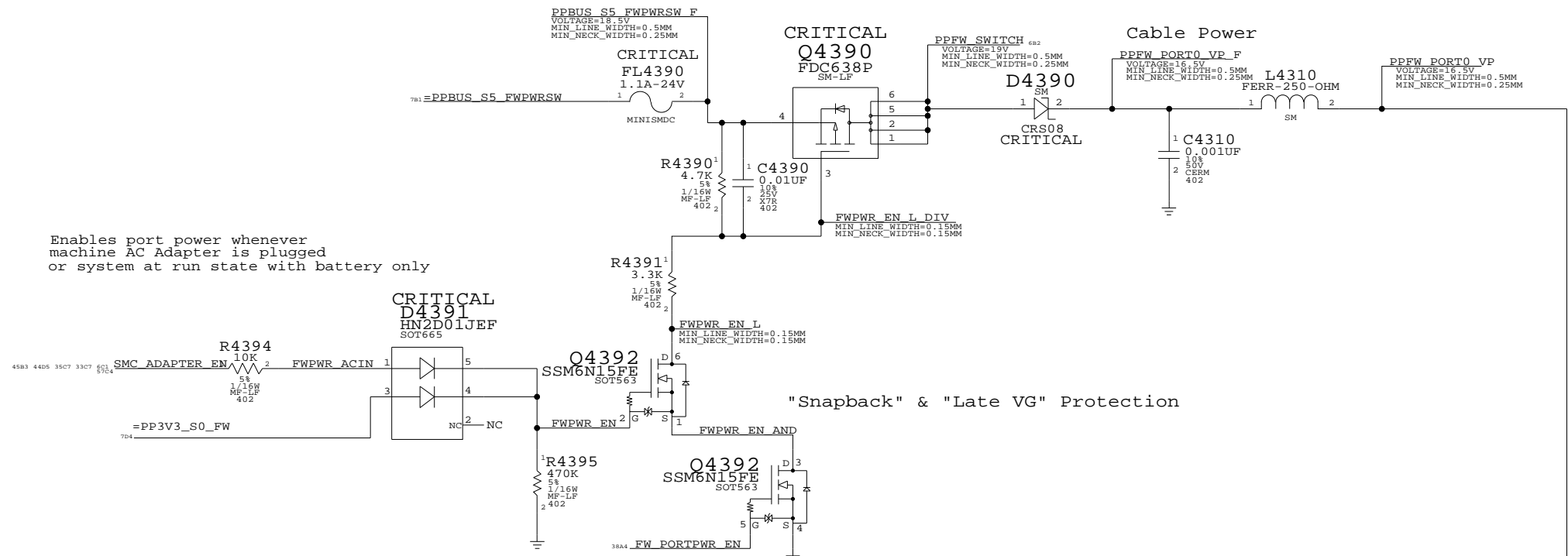
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

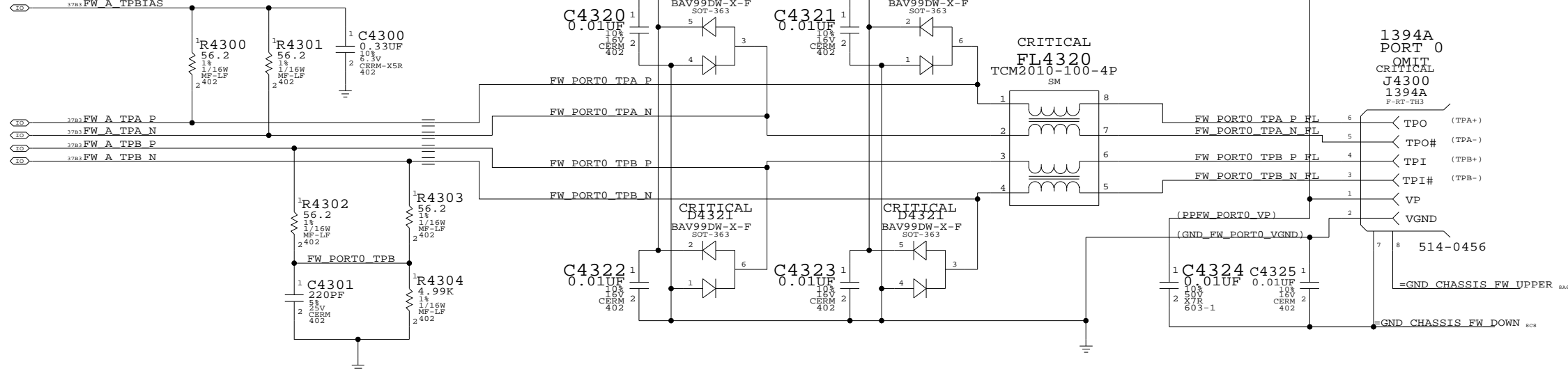
0 FOR SINGLE PORT  
 1 FOR DUAL PORT



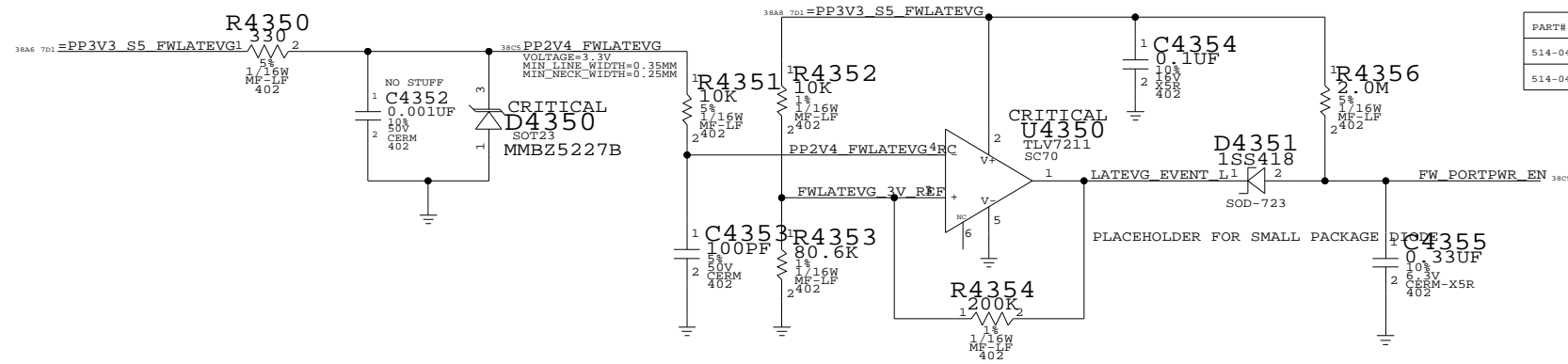
Enables port power whenever machine AC Adapter is plugged or system at run state with battery only



[LATE VG NOTES]  
 CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP



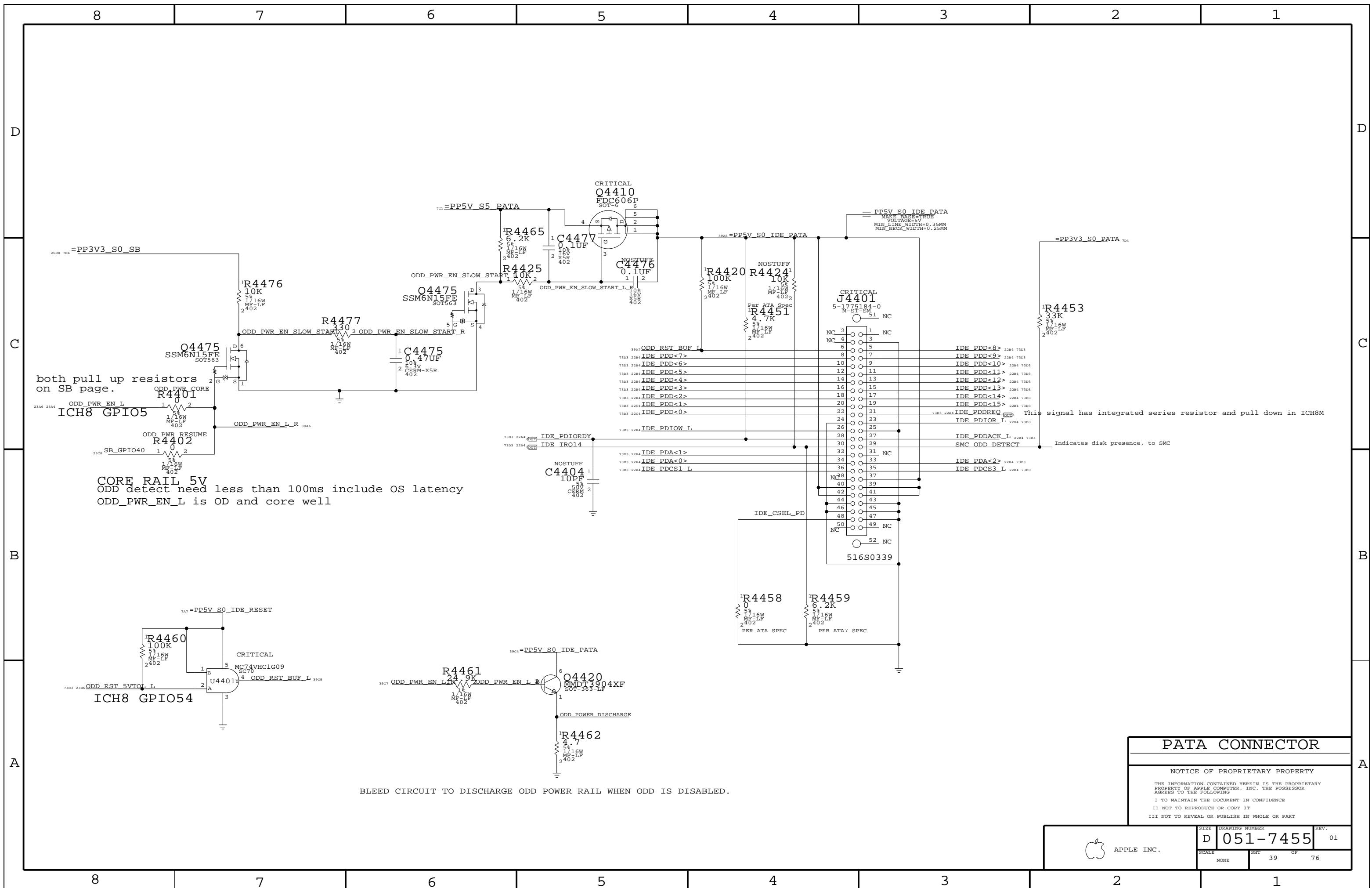
LATE-VG DETECTION CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0456	1	CONN, 6P 1394A RCPT, MIDPLANE, IN3, LP	J4300	CRITICAL	NORMAL
514-0476	1	CONN, 6P 1394A RCPT, MIDPLANE, BLACK, LP	J4300	CRITICAL	FANCY

**FIREWIRE PORT**  
 SYNC\_MASTER=GPU SYNC\_DATE=07/17/2006  
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APPLE INC. DRAWING NUMBER: D 051-7455 REV. 01  
 SCALE: NONE SHEET: 38 OF 76



both pull up resistors on SB page.

CORE RAIL 5V  
 ODD detect need less than 100ms include OS latency  
 ODD\_PWR\_EN\_L is OD and core well

This signal has integrated series resistor and pull down in ICH8M

Indicates disk presence, to SMC

BLEED CIRCUIT TO DISCHARGE ODD POWER RAIL WHEN ODD IS DISABLED.

**PATA CONNECTOR**

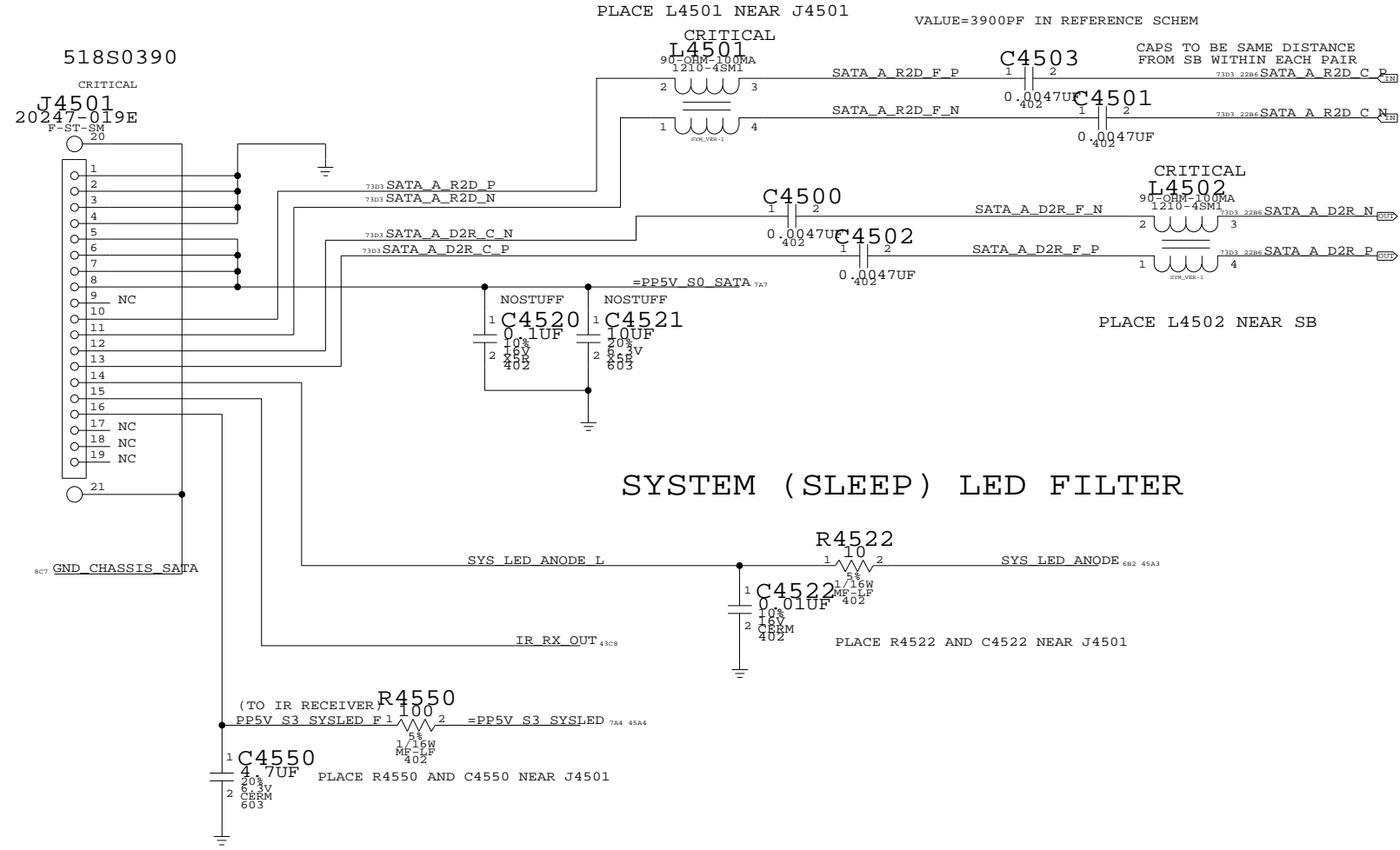
NOTICE OF PROPRIETARY PROPERTY

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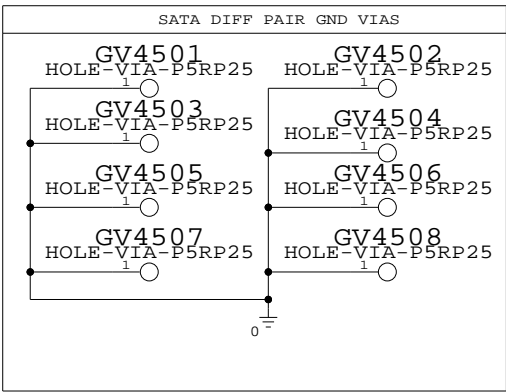
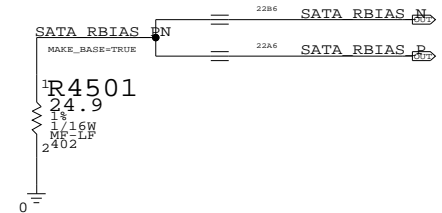
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7455	REV.: 01
	SCALE: NONE	SHEET: 39	OF: 76

# SATA CONNECTOR



PLACE NEAR ICH8 PIN



**SATA CONNECTOR**

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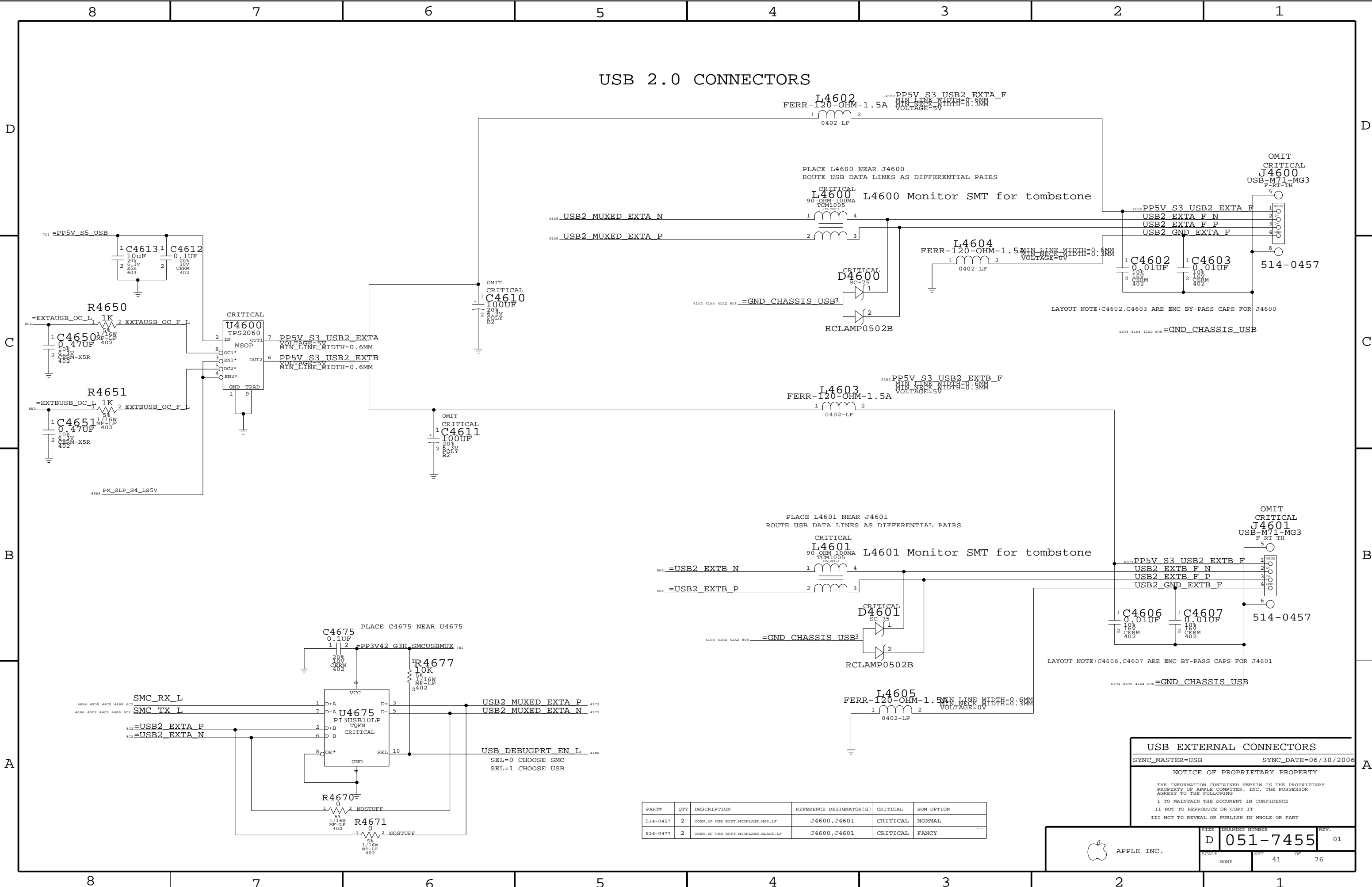
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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7455	REV.: 01
	SCALE: NONE	SHEET: 40	OF: 76



# USB 2.0 CONNECTORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0457	2	CONN, 4P USB RCPT, MIDPLANE, MG3, LF	J4600, J4601	CRITICAL	NORMAL
514-0477	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J4600, J4601	CRITICAL	FANCY

**USB EXTERNAL CONNECTORS**  
 SYNC\_MASTER=USB SYNC\_DATE=06/30/2006

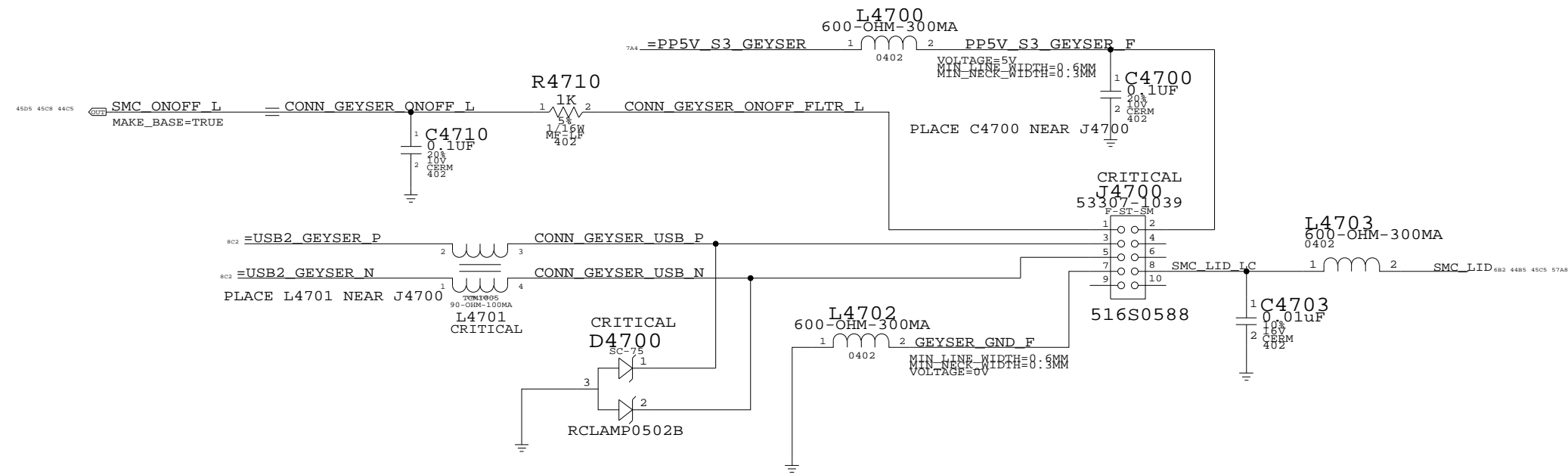
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SCALE: NONE SHEET: 41 OF 76

DRAWING NUMBER: **D 051-7455** REV. 01

# GEYSER AND DIMMO REMOTE TEMP SENSORS

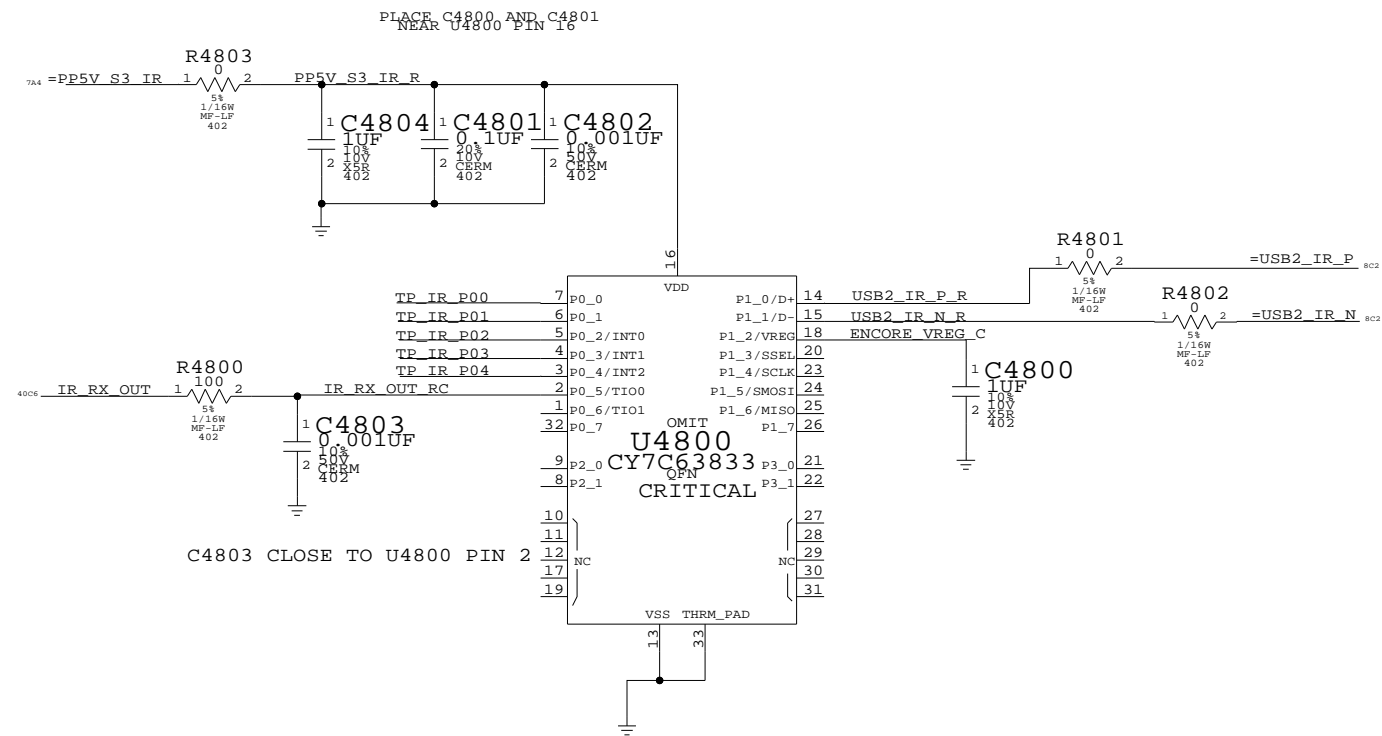


**CONNECTOR MISC**  
 SYNC\_MASTER=USB SYNC\_DATE=06/29/2006

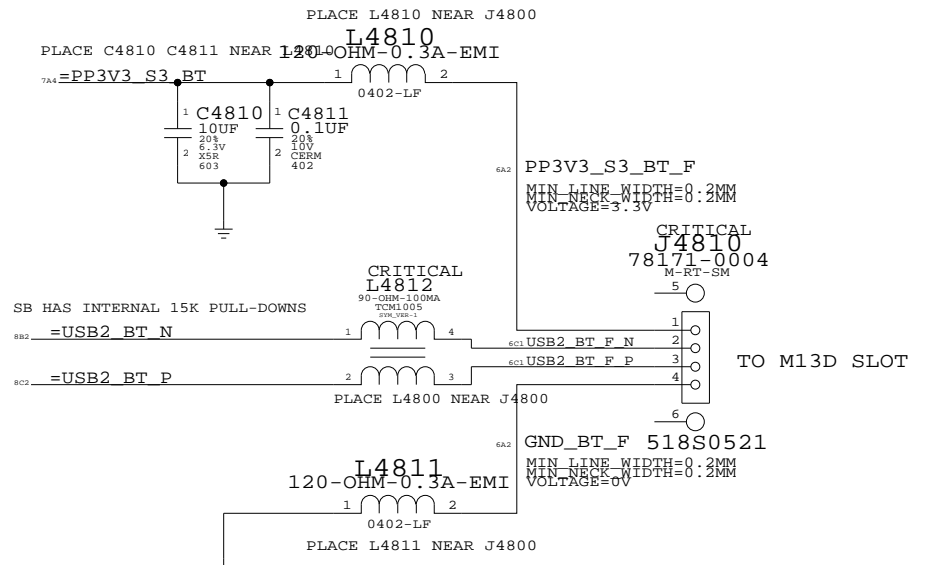
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APPLE INC.	SIZE DRAWING NUMBER REV. <b>D 051-7455</b> 01
	SCALE SHEET OF NONE 42 OF 76

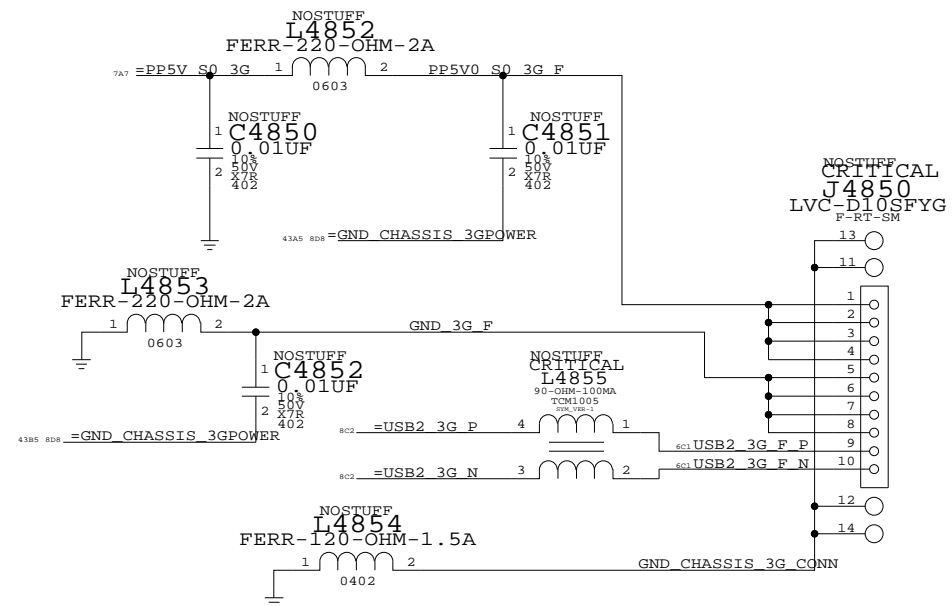
# IR CYPRESS ENCORE II USB CONTROLLER



# BLUETOOTH



# 3G CONNECTOR



# IR CONTROLLER & BT INTERFACE

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APPLE INC.	DRAWING NUMBER <b>D 051-7455</b>	REV. 01
	SCALE NONE	SHEET 43

8

7

6

5

4

3

2

1

NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designated as outputs can be left floating, those designated as inputs require pull-ups.

D

D

C

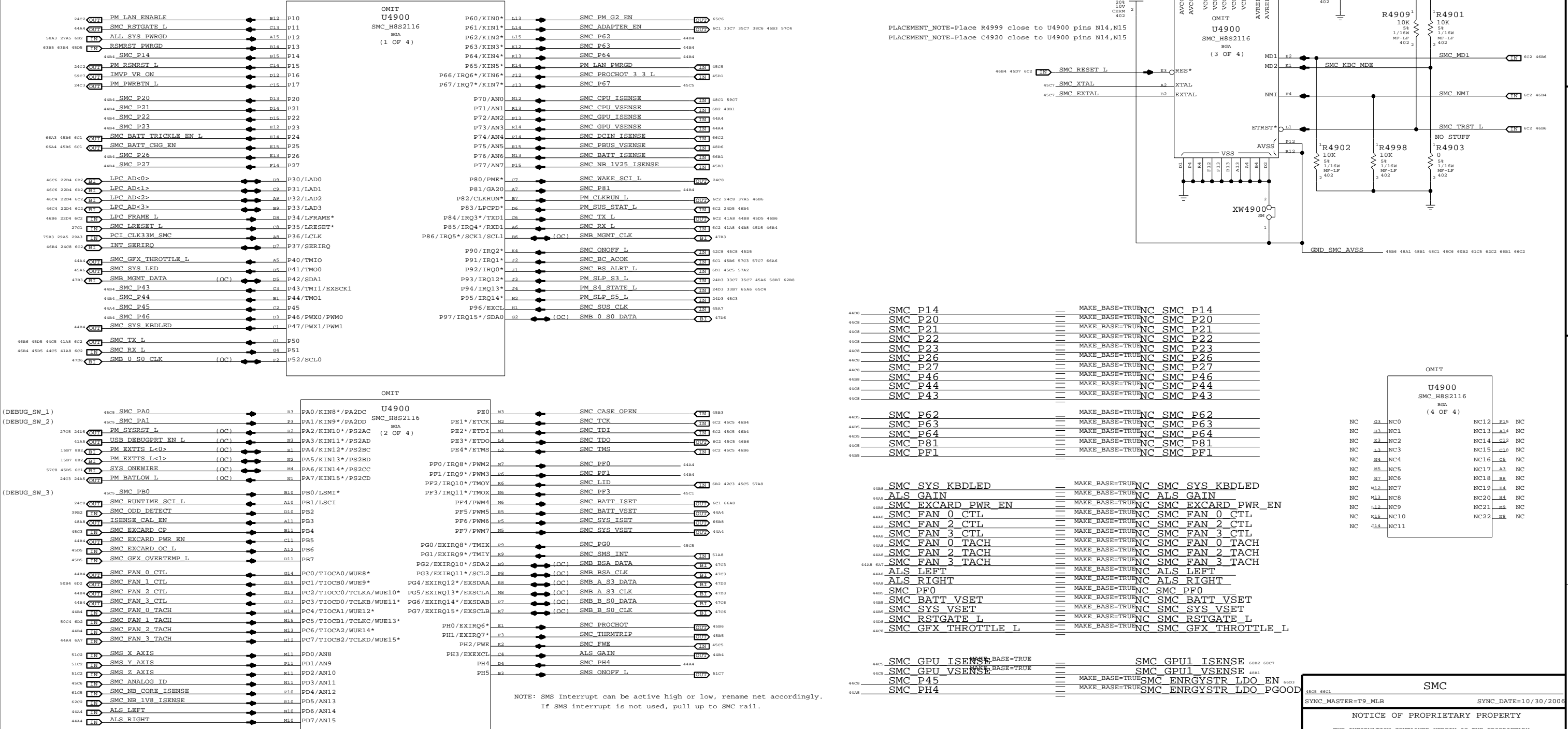
C

B

B

A

A



4408	SMC P14	==	MAKE_BASE=TRUE	NC	SMC P14
4408	SMC P20	==	MAKE_BASE=TRUE	NC	SMC P20
4408	SMC P21	==	MAKE_BASE=TRUE	NC	SMC P21
4408	SMC P22	==	MAKE_BASE=TRUE	NC	SMC P22
4408	SMC P23	==	MAKE_BASE=TRUE	NC	SMC P23
4408	SMC P26	==	MAKE_BASE=TRUE	NC	SMC P26
4408	SMC P27	==	MAKE_BASE=TRUE	NC	SMC P27
4408	SMC P46	==	MAKE_BASE=TRUE	NC	SMC P46
4408	SMC P44	==	MAKE_BASE=TRUE	NC	SMC P44
4408	SMC P43	==	MAKE_BASE=TRUE	NC	SMC P43
4405	SMC P62	==	MAKE_BASE=TRUE	NC	SMC P62
4405	SMC P63	==	MAKE_BASE=TRUE	NC	SMC P63
4405	SMC P64	==	MAKE_BASE=TRUE	NC	SMC P64
4405	SMC P81	==	MAKE_BASE=TRUE	NC	SMC P81
4405	SMC PF1	==	MAKE_BASE=TRUE	NC	SMC PF1

4408	SMC SYS KBDLED	==	MAKE_BASE=TRUE	NC	SMC SYS KBDLED
4408	ALS GAIN	==	MAKE_BASE=TRUE	NC	ALS GAIN
4408	SMC_EXCARD_PWR_EN	==	MAKE_BASE=TRUE	NC	SMC_EXCARD_PWR_EN
4408	SMC_FAN_0_CTL	==	MAKE_BASE=TRUE	NC	SMC_FAN_0_CTL
4408	SMC_FAN_2_CTL	==	MAKE_BASE=TRUE	NC	SMC_FAN_2_CTL
4408	SMC_FAN_3_CTL	==	MAKE_BASE=TRUE	NC	SMC_FAN_3_CTL
4408	SMC_FAN_0_TACH	==	MAKE_BASE=TRUE	NC	SMC_FAN_0_TACH
4408	SMC_FAN_2_TACH	==	MAKE_BASE=TRUE	NC	SMC_FAN_2_TACH
4408	SMC_FAN_3_TACH	==	MAKE_BASE=TRUE	NC	SMC_FAN_3_TACH
4408	ALS_LEFT	==	MAKE_BASE=TRUE	NC	ALS_LEFT
4408	ALS_RIGHT	==	MAKE_BASE=TRUE	NC	ALS_RIGHT
4408	SMC_PFO	==	MAKE_BASE=TRUE	NC	SMC_PFO
4408	SMC_BATT_VSET	==	MAKE_BASE=TRUE	NC	SMC_BATT_VSET
4408	SMC_SYS_VSET	==	MAKE_BASE=TRUE	NC	SMC_SYS_VSET
4408	SMC_RSTGATE_L	==	MAKE_BASE=TRUE	NC	SMC_RSTGATE_L
4408	SMC_GFX_THROTTLE_L	==	MAKE_BASE=TRUE	NC	SMC_GFX_THROTTLE_L

4405	SMC_GPU_ISENSE	==	MAKE_BASE=TRUE	SMC_GPU1_ISENSE	6082 60C7
4405	SMC_GPU_VSENSE	==	MAKE_BASE=TRUE	SMC_GPU1_VSENSE	4881
4408	SMC_P45	==	MAKE_BASE=TRUE	SMC_ENRGYSTR_LDO_EN	66D3
4405	SMC_PH4	==	MAKE_BASE=TRUE	SMC_ENRGYSTR_LDO_PGOOD	45C5 66C1

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

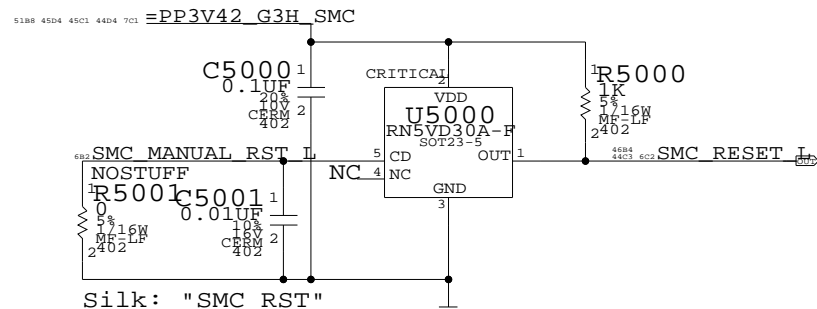
**SMC**  
 SYNC\_MASTER=T9\_MLB SYNC\_DATE=10/30/2006

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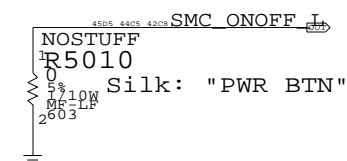
SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	44	76

### SMC Reset Button / Brownout Detect



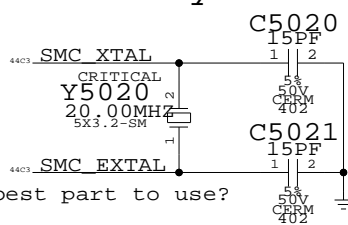
Silk: "SMC\_RST"

### Debug Power Button



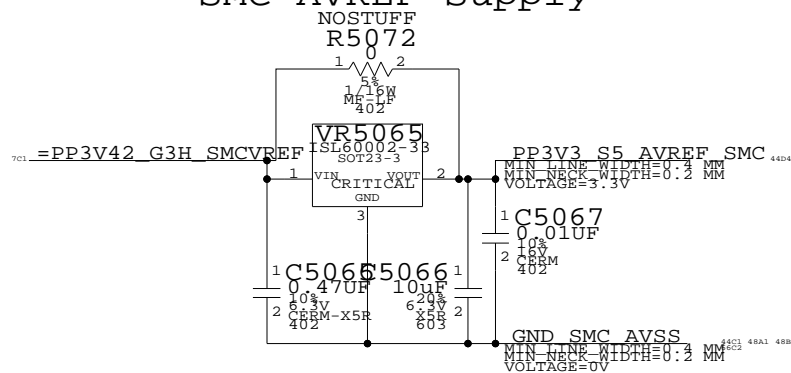
Silk: "PWR\_BTN"

### SMC Crystal Circuit



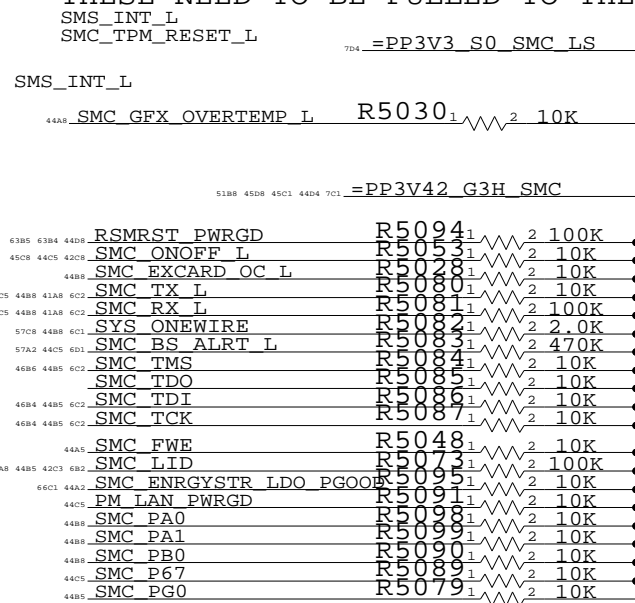
Is this the best part to use?

### SMC AVREF Supply

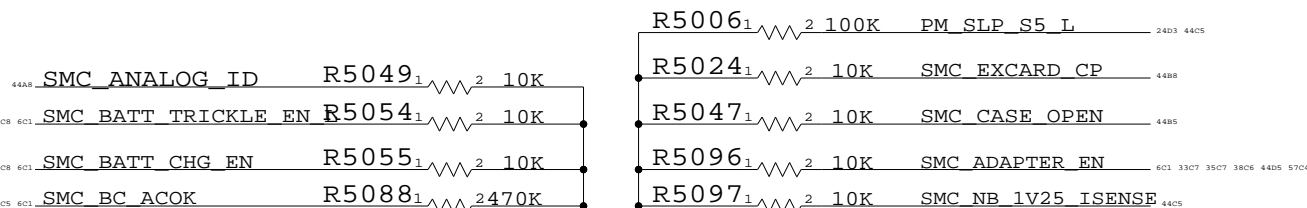
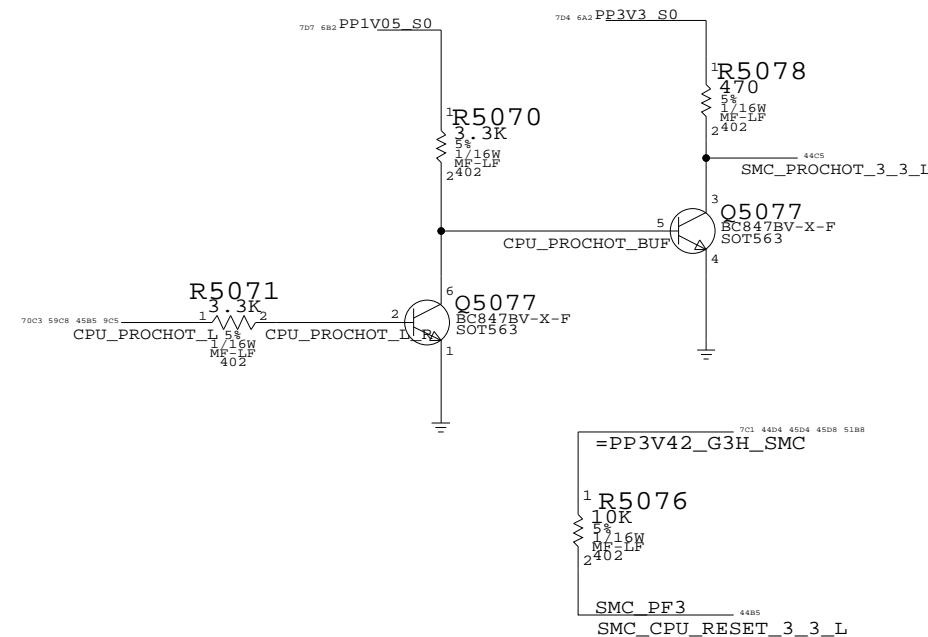


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5065	TI REF3133

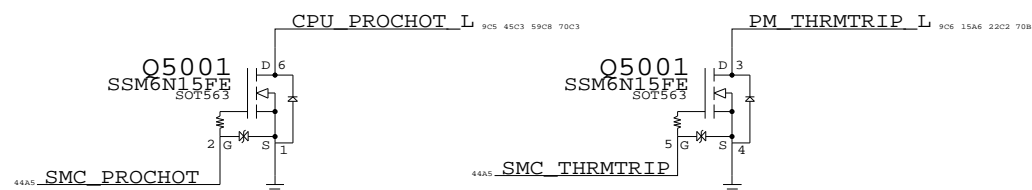
THESE NEED TO BE PULLED TO THE PROPER RAIL:



### SMC 1.05V to 3.3V Level Shifting

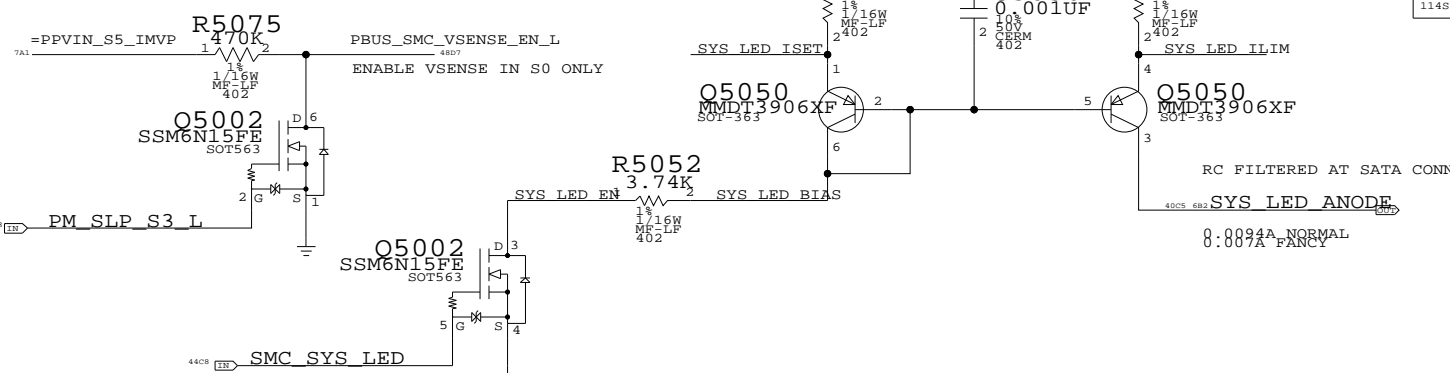
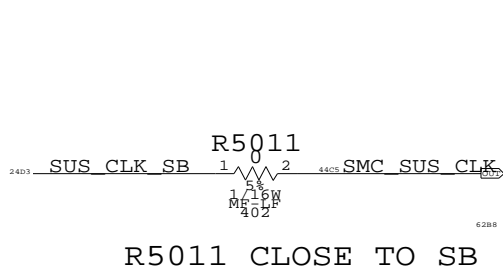


### SMC 3.3V to 1.05V Level Shifting



### SYSTEM (SLEEP) LED CURRENT DRIVER

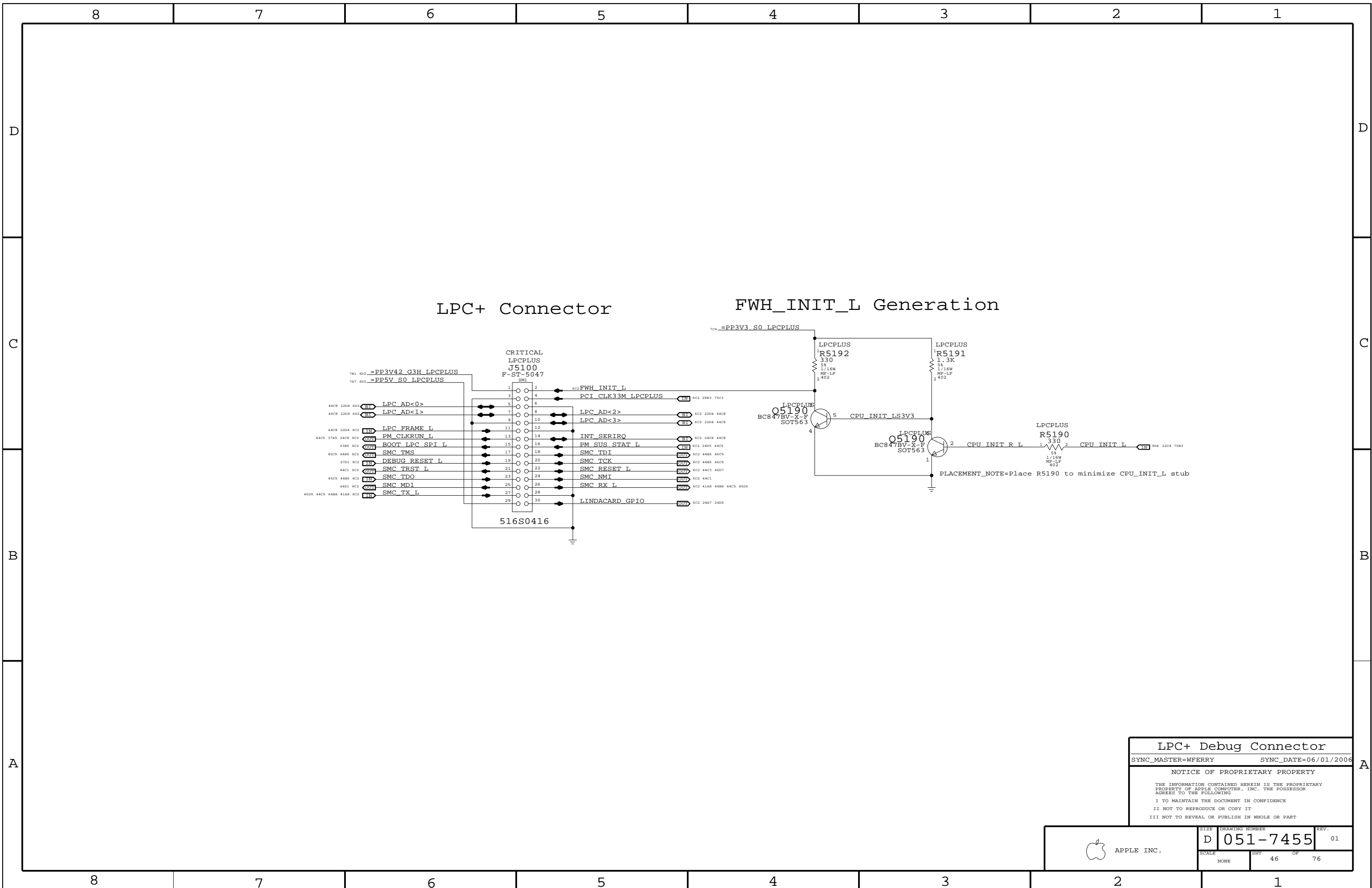
### 3.3V TO PBUS LEVEL SHIFTING



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0071	1	31.6, 1%, 1/16W, MF-LF, 402	R5050	NORMAL
114S0086	1	44.2, 1%, 1/16W, MF-LF, 402	R5050	FANCY

**SMC SUPPORT**  
 SYNC\_MASTER=GPU SYNC\_DATE=07/17/2006  
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APPLE INC.	SCALE	SHEET		OF	REV.
	NONE	45		76	01



LPC+ Connector

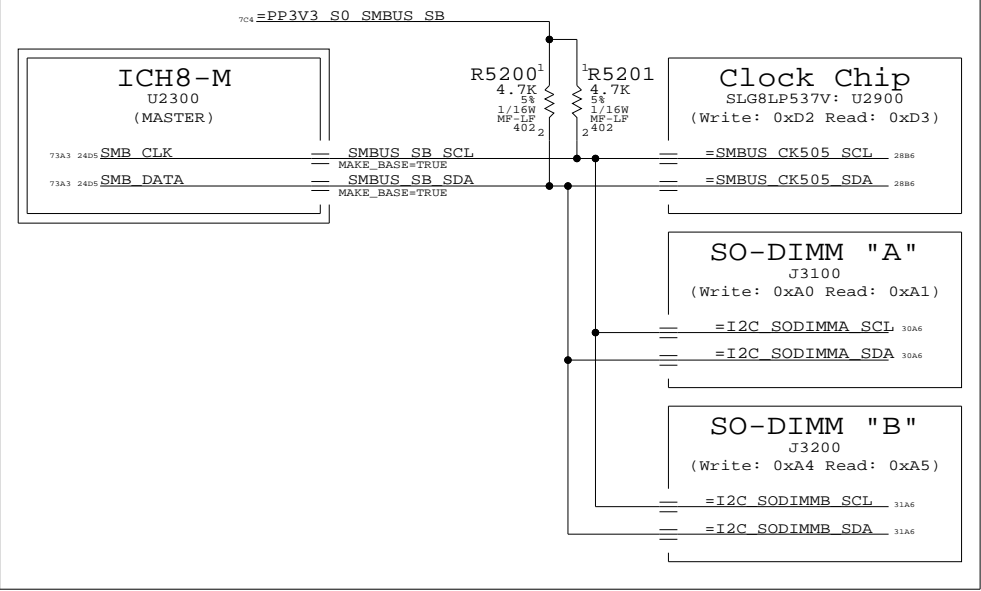
FWH\_INIT\_L Generation

LPC+ Debug Connector  
 SYNC\_MASTER=WFERRY SYNC\_DATE=06/01/2006  
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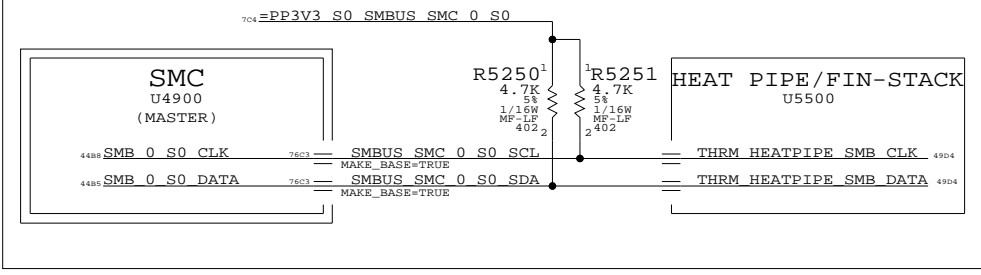
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		46	76

8 7 6 5 4 3 2 1

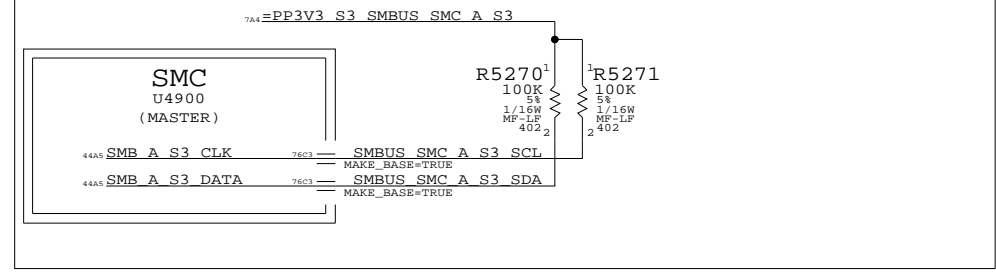
### ICH8-M SMBus Connections



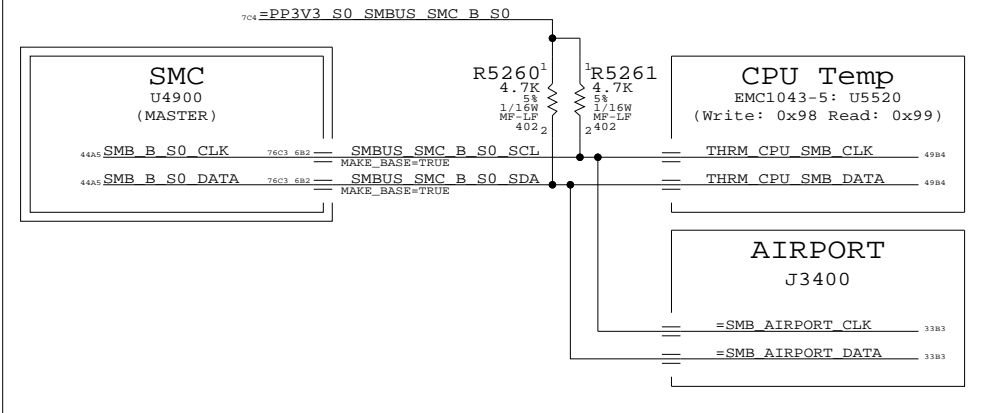
### SMC "0" SMBus Connections



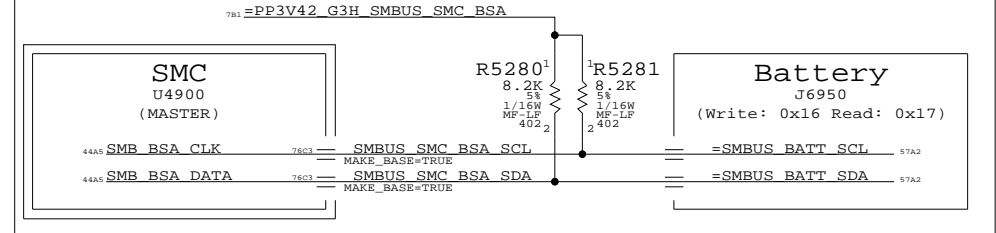
### SMC "A" SMBus Connections



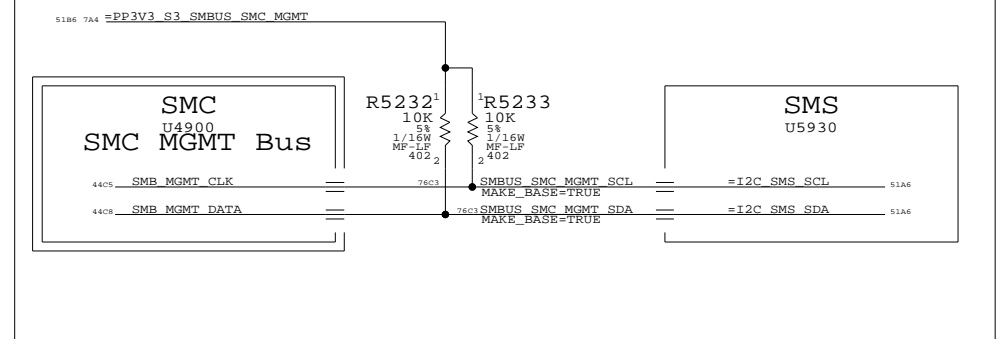
### SMC "B" SMBus Connections



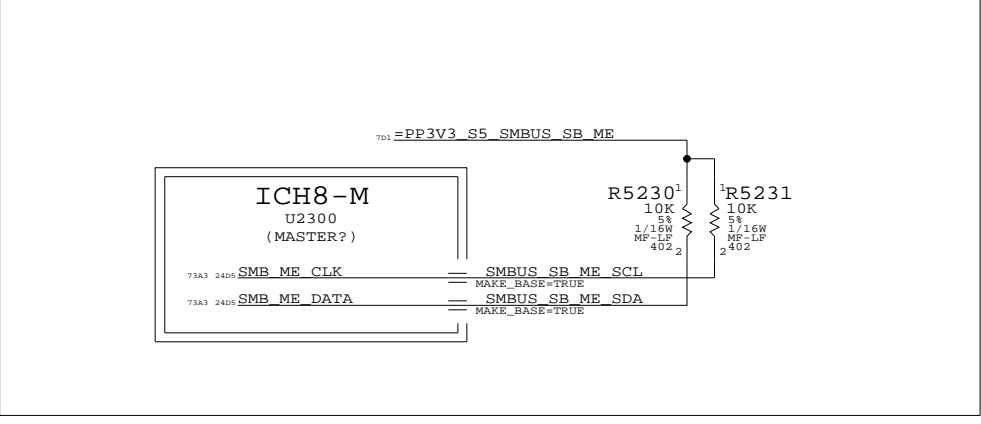
### SMC "Battery A" SMBus Connections



### SMC "MANAGEMENT" SMBUS CONNECTIONS



### ICH8-M ME SMBus Connections



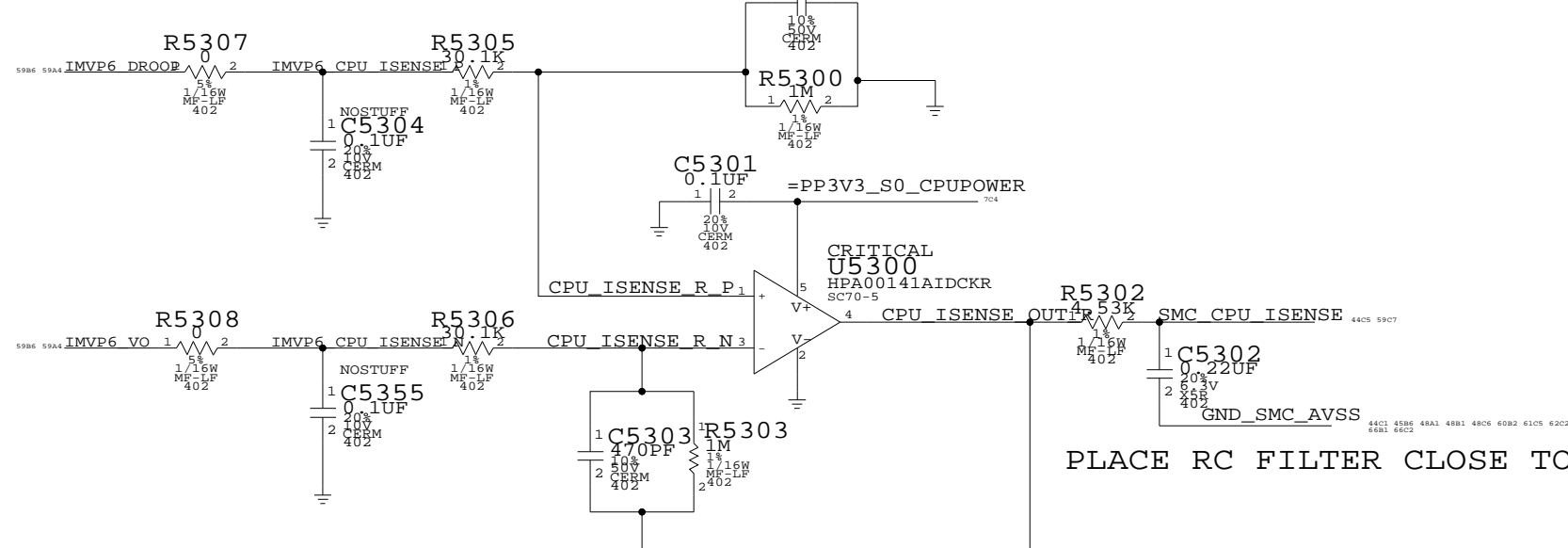
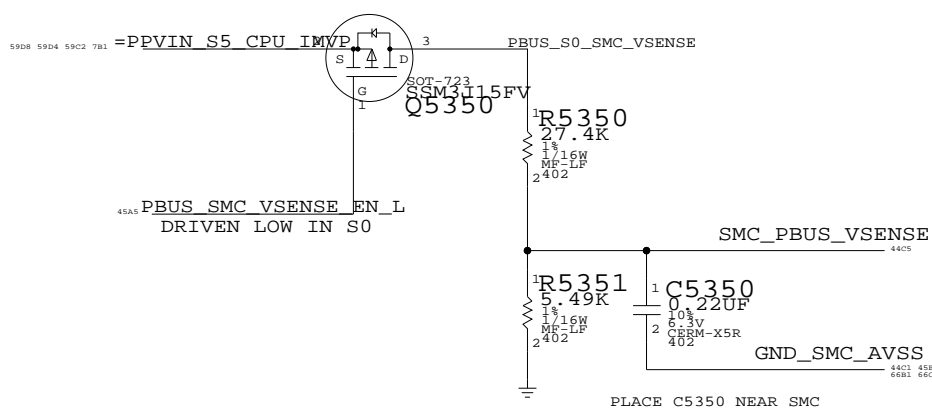
**SMBUS CONNECTIONS**  
 SYNC\_MASTER=WFERRY SYNC\_DATE=06/01/2006  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		47	76

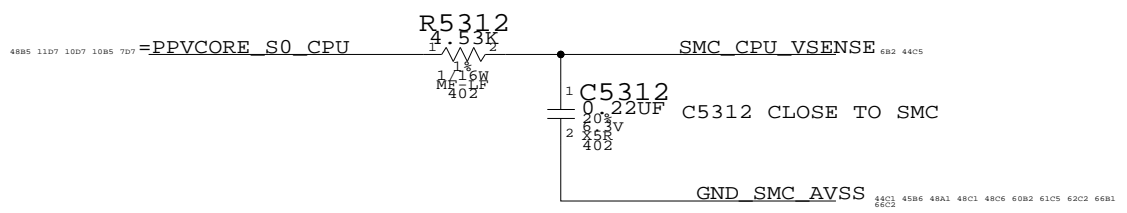
8 7 6 5 4 3 2 1

PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

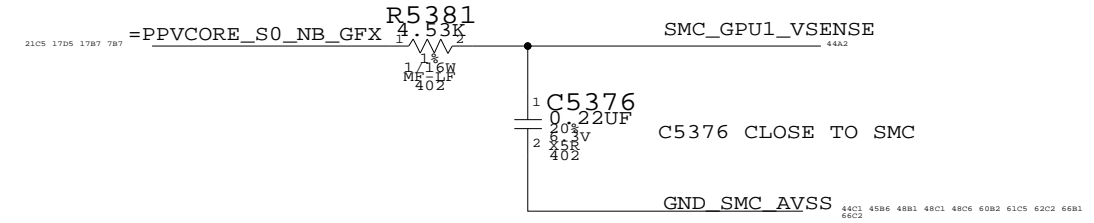
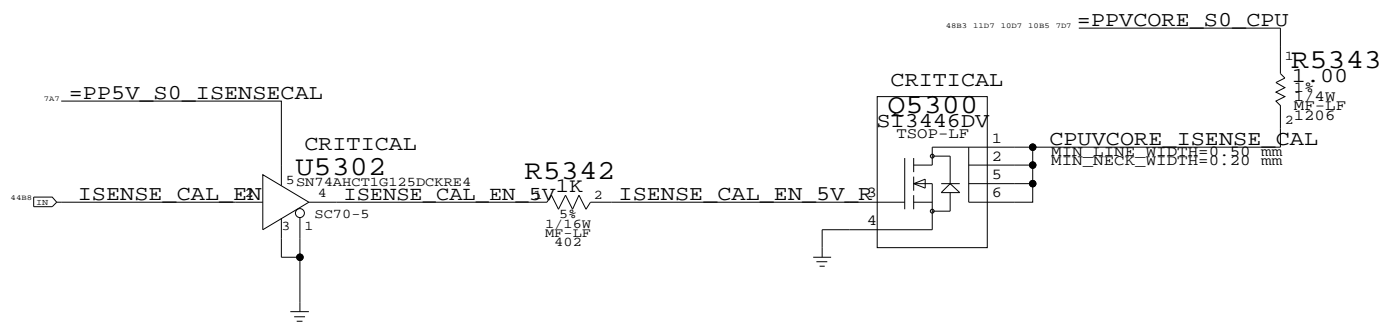


CPU VOLTAGE SENSE



Current Sense Calibration Circuit  
Switches in fixed load on power supplies to calibrate current sense circuits

GPU VOLTAGE SENSE

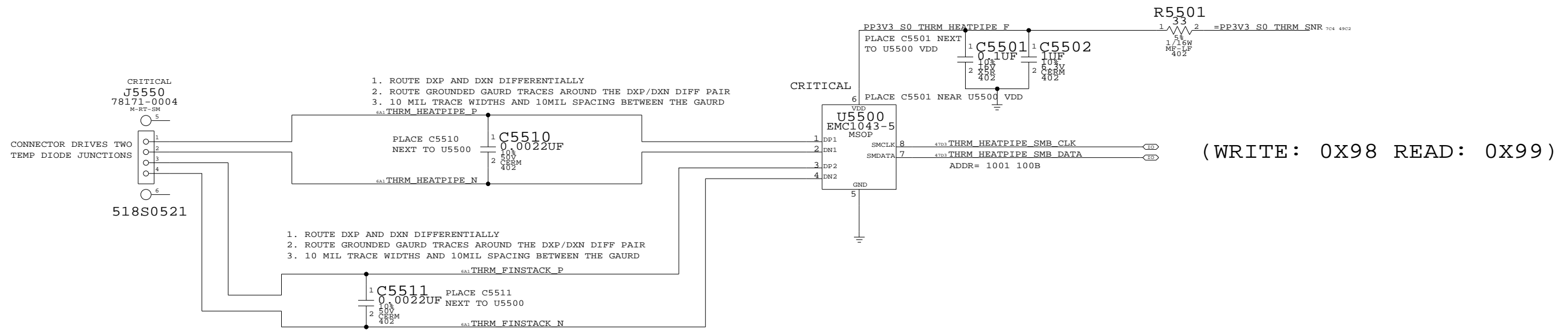


CPU Current & Voltage Sense  
 SYNC\_MASTER=GPU SYNC\_DATE=07/17/2006  
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	NONE	SHT	48 OF 76



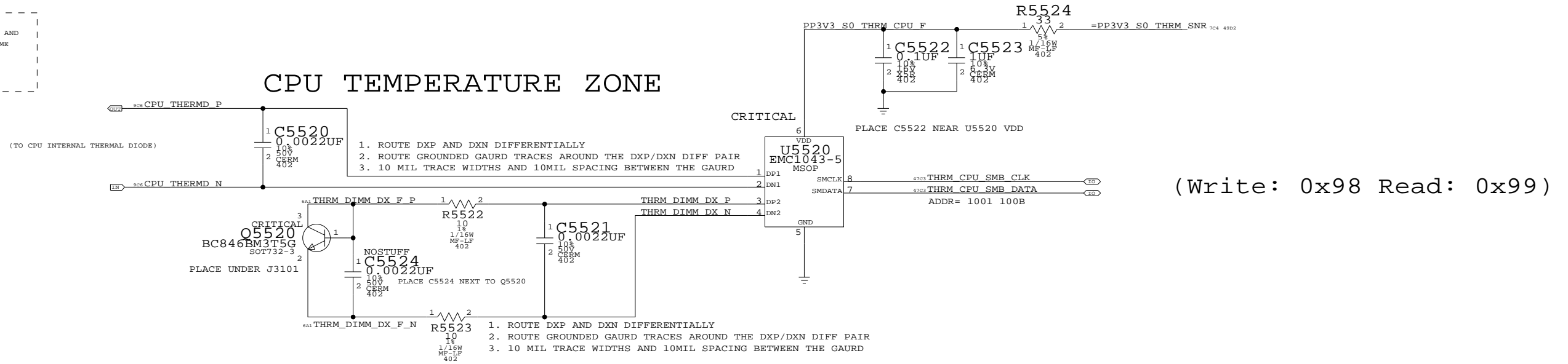
# HEAT-PIPE/FIN-STACK TEMPERATURE ZONE



LAYOUT NOTE:  
ADD GND GUARD TRACE FOR CPU\_THERMD\_P AND CPU\_THERMD\_N

LAYOUT NOTE:  
ROUTE CPU\_THERMD\_P AND CPU\_THERMD\_N ON SAME LAYER.  
10 MIL TRACE  
10 MIL SPACING

# CPU TEMPERATURE ZONE



**TEMPERATURE SENSE**

SYNC\_MASTER=GPU SYNC\_DATE=06/21/2006

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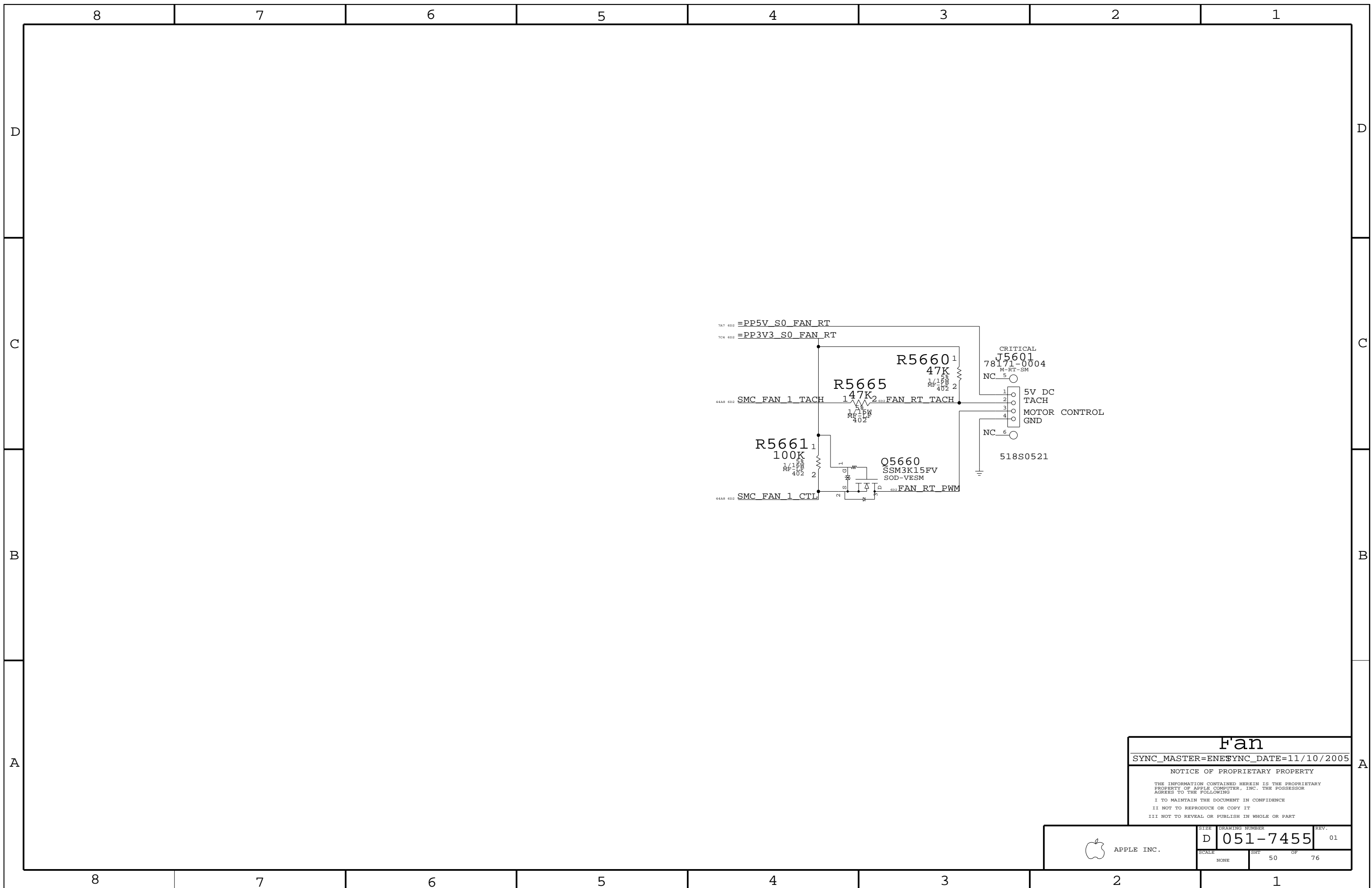
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-7455	01
SCALE		SHT	OF
NONE		49	76



**F'an**  
 SYNC\_MASTER=ENESYNC\_DATE=11/10/2005  
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7455	REV. 01
	SCALE NONE	SHEET 50	OF 76

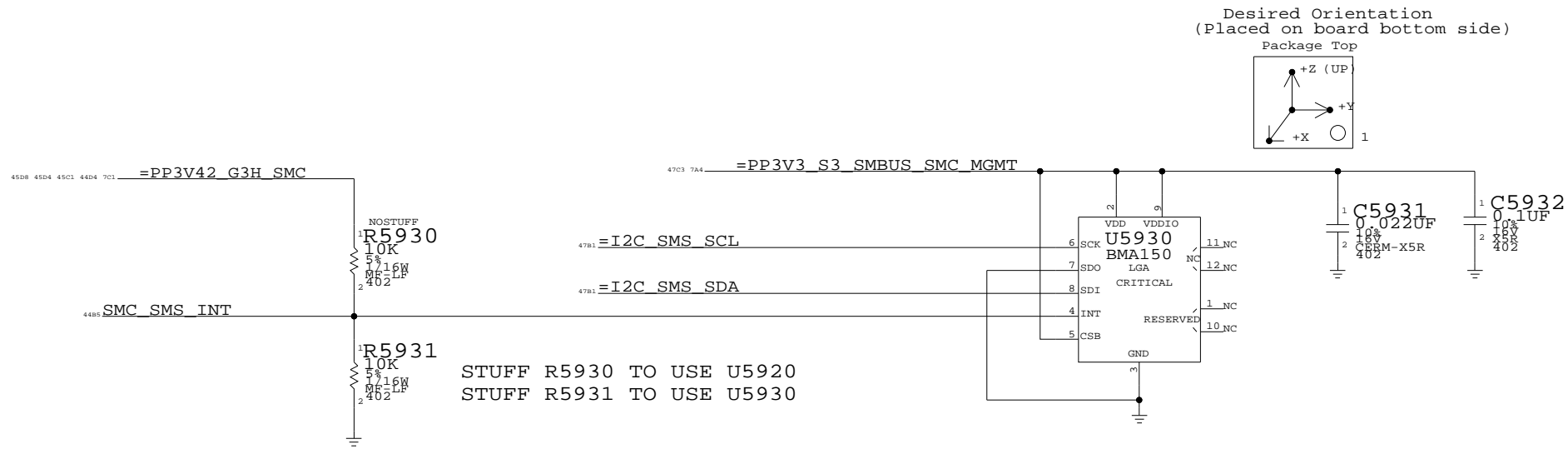
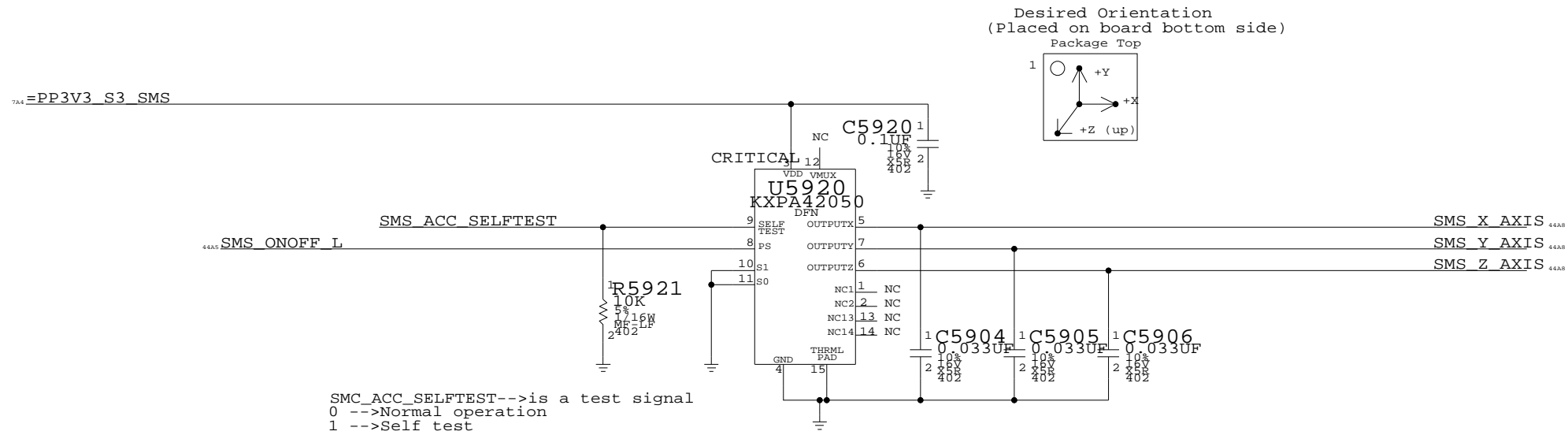
PAGE NOTES

INPUT  
 =PP3V3\_S3\_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)  
 SMS\_ONOFF\_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT  
 SMS\_ACC\_\*\_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE  
 7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050  
 7/28/2005 - CONNECTED PD PIN TO SMC'S SMS\_ONOFF\_L



**SMS**

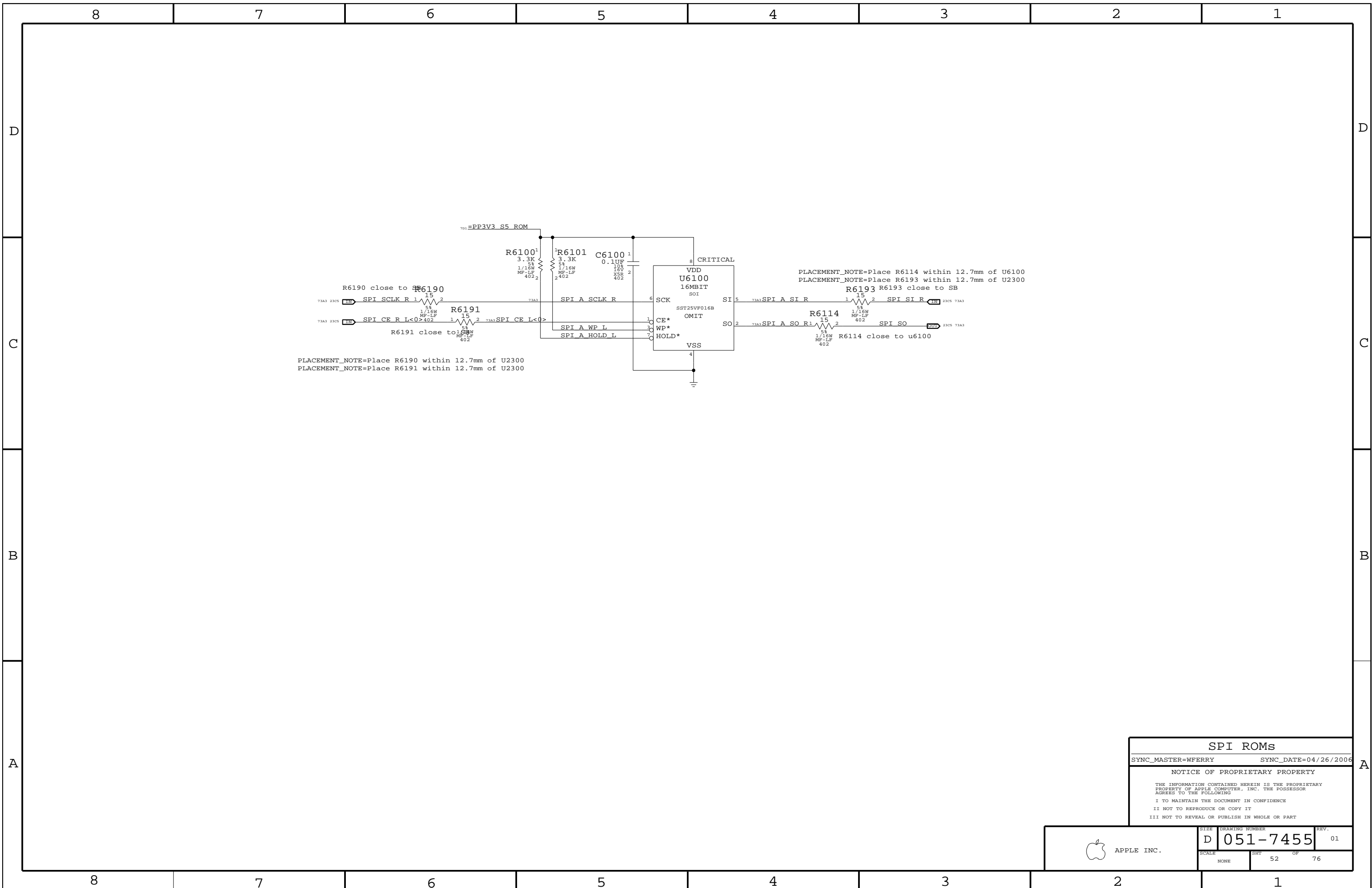
SYNC\_MASTER=SMC SYNC\_DATE=08/23/2005

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SCALE		SHT	OF
NONE		51	76



**SPI ROMs**

SYNC\_MASTER=WFERRY SYNC\_DATE=04/26/2006

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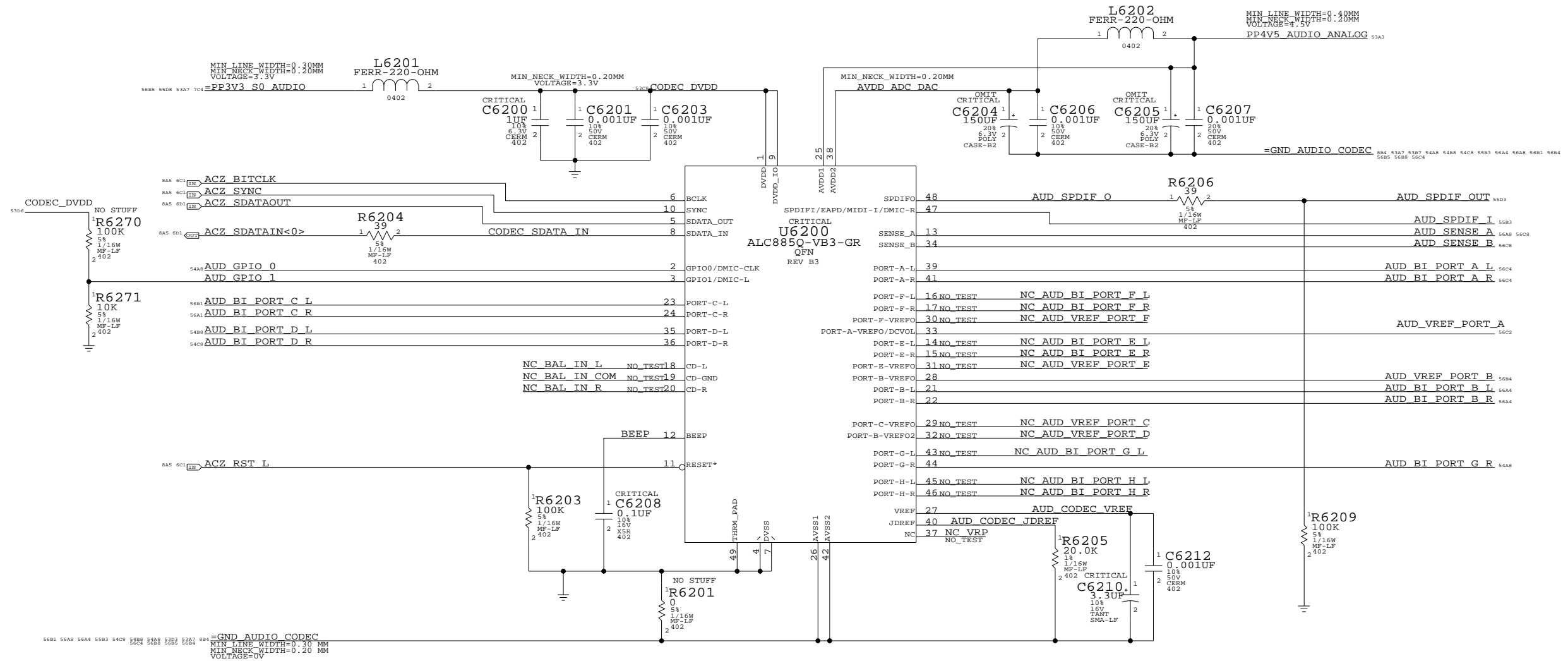
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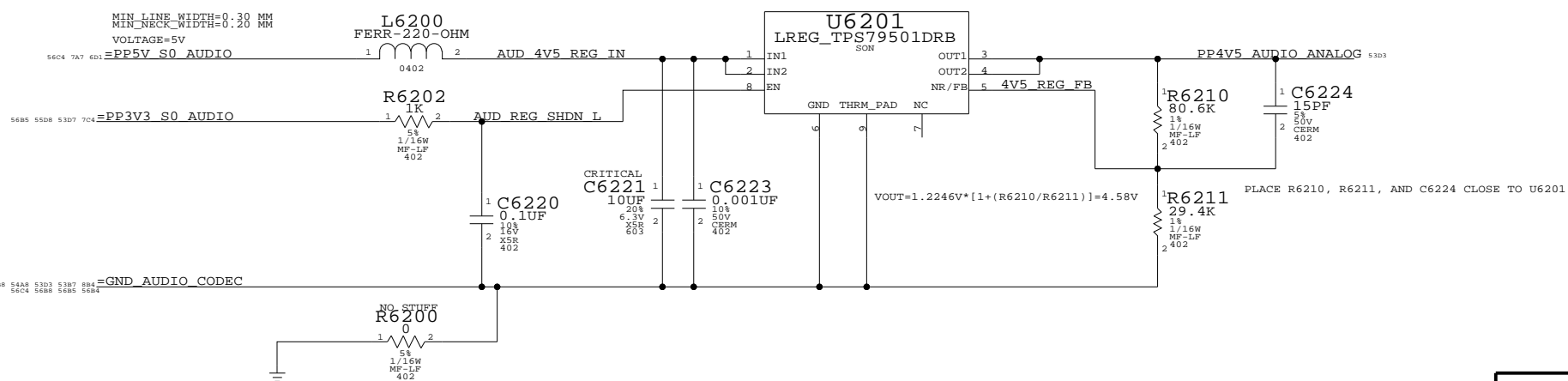
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7455	01
SCALE		SHT	OF
NONE		52	76

AUDIO CODEC  
APPLE P/N 353S1538



AUDIO 4.5V REGULATOR  
APPLE P/N 353S1576



AUDIO: CODEC

SYNC\_MASTER=M70AUDIO

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SCALE		SHT	OF
		53	76

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 169 HZ < FC < 282 HZ  
 SUB 80 HZ < FC < 132 HZ  
 GAIN 12DB

VOLTAGE=5V  
 MIN\_LINE\_WIDTH=0.60 MM  
 MIN\_NECK\_WIDTH=0.20 MM  
 5408 5488 7A7 6D1 =PP5V\_S0\_AUDIO\_AMP

VOLTAGE=5V  
 MIN\_LINE\_WIDTH=0.30 MM  
 MIN\_NECK\_WIDTH=0.20 MM

MIN\_LINE\_WIDTH=0.30 mm MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 mm MIN\_NECK\_WIDTH=0.20 mm  
 5404 SPKRAMP\_R\_P\_OUT 2 R6660 0 SPKRCONN\_R\_P\_OUT 681 5502

MIN\_LINE\_WIDTH=0.30 mm MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 mm MIN\_NECK\_WIDTH=0.20 mm  
 5404 SPKRAMP\_R\_N\_OUT 2 R6661 0 SPKRCONN\_R\_N\_OUT 681 5502

RIGHT SATELLITE

MIN\_LINE\_WIDTH=0.30 mm MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 mm MIN\_NECK\_WIDTH=0.20 mm  
 5404 SPKRAMP\_L\_P\_OUT 2 R6670 0 SPKRCONN\_L\_P\_OUT 681 5502

MIN\_LINE\_WIDTH=0.30 mm MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 mm MIN\_NECK\_WIDTH=0.20 mm  
 5404 SPKRAMP\_L\_N\_OUT 2 R6671 0 SPKRCONN\_L\_N\_OUT 681 5502

LEFT SATELLITE

MIN\_LINE\_WIDTH=0.30 mm MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 mm MIN\_NECK\_WIDTH=0.20 mm  
 5404 SPKRAMP\_SUB\_P\_OUT 2 R6680 0 SPKRCONN\_SUB\_P\_OUT 681 5502

MIN\_LINE\_WIDTH=0.30 mm MIN\_LINE\_WIDTH=0.30 mm  
 MIN\_NECK\_WIDTH=0.20 mm MIN\_NECK\_WIDTH=0.20 mm  
 5404 SPKRAMP\_SUB\_N\_OUT 2 R6681 0 SPKRCONN\_SUB\_N\_OUT 681 5502

SUB-TWEETER

MIN\_LINE\_WIDTH=0.60 MM XW6600  
 MIN\_NECK\_WIDTH=0.20 MM SM  
 5408 5488 54A5 8A4 =GND\_AUDIO\_AMP 1 0 2 SPKRAMP\_THERMPLANE 54A4 54B4 54C4

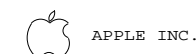
AUDIO: SPEAKER AMP

SYNC\_MASTER=M70AUDIO SYNC\_DATE=03/12/2007

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SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE SHEET OF 76

D  
C  
B  
A

D  
C  
B  
A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR

APN:518S0392

CRITICAL  
J6701  
48227-0301  
M-RT-SM

SPEAKER CONNECTOR

APN:518S0519

CRITICAL  
J6702  
78171-0002  
M-RT-SM

CRITICAL  
J6703  
78171-0004  
M-RT-SM

APN:518S0521

XW6705

MIC EMI FILTER

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

AUDIO: JACK

SYNC\_MASTER=M70AUDIO SYNC\_DATE=03/12/2007

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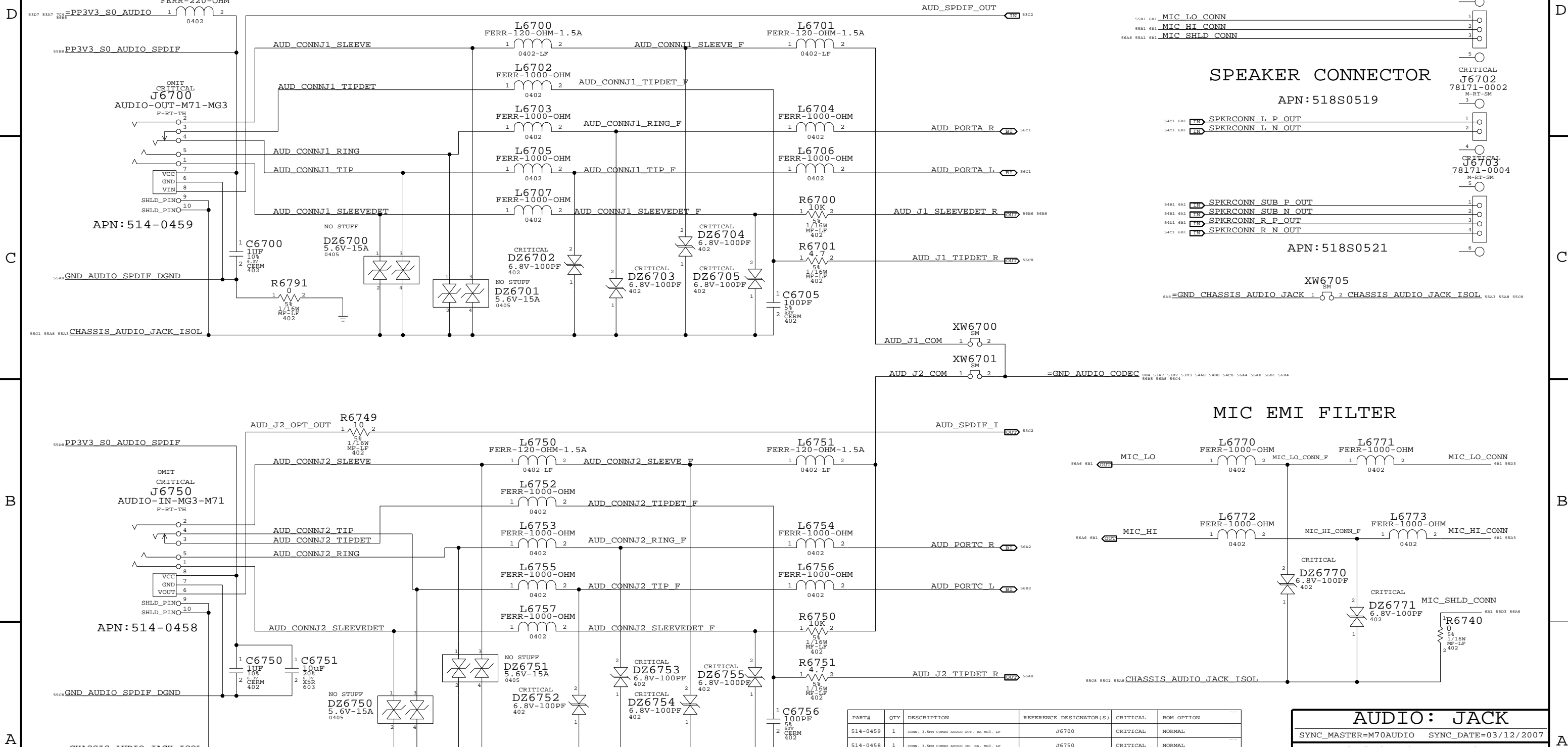
SIZE DRAWING NUMBER REV.

D 051-7455 01

SCALE SHEET OF

NONE 55 OF 76

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0459	1	CONN, 3.5MM COMBO AUDIO OUT, RA, NEG, LF	J6700	CRITICAL	NORMAL
514-0458	1	CONN, 3.5MM COMBO AUDIO IN, RA, NEG, LF	J6750	CRITICAL	NORMAL
514-0479	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J6700	CRITICAL	FANCY
514-0478	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J6750	CRITICAL	FANCY



CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

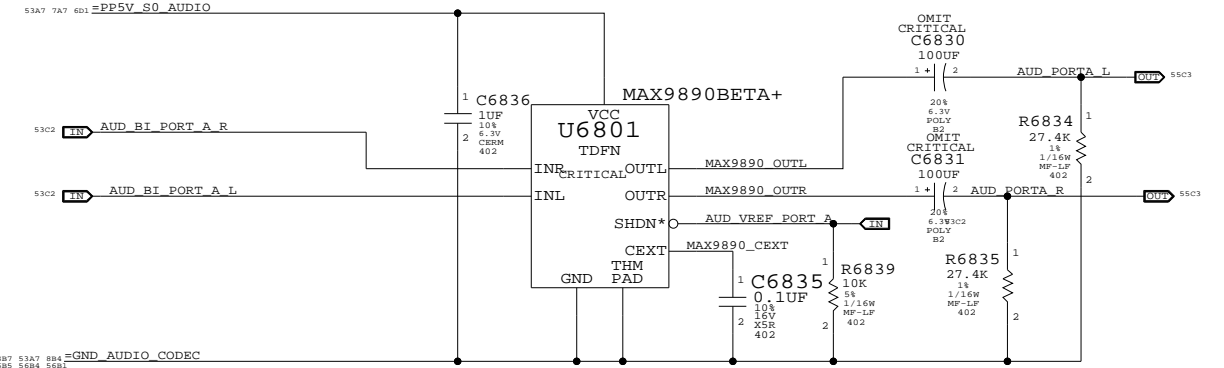
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

HP/LO DE-POP SWITCH  
APN:353S1459

PORT A HP/LO

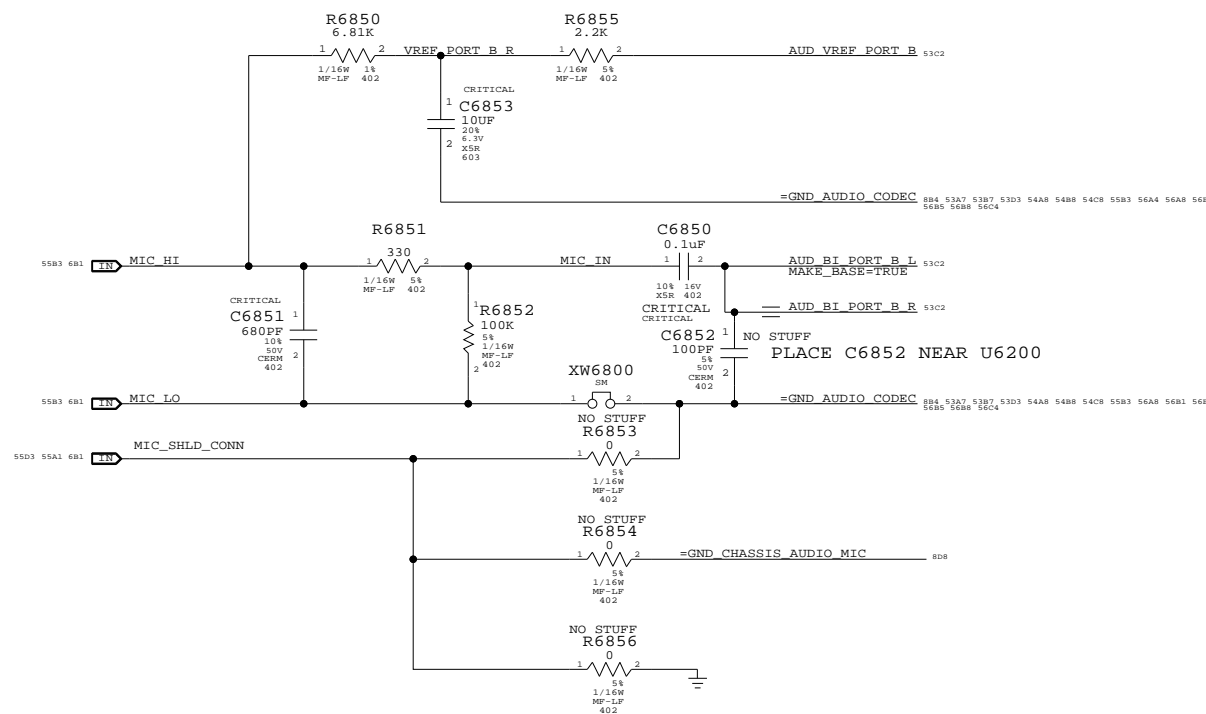
PORT A DETECT PORT E DETECT (SPDIF DELEGATE)



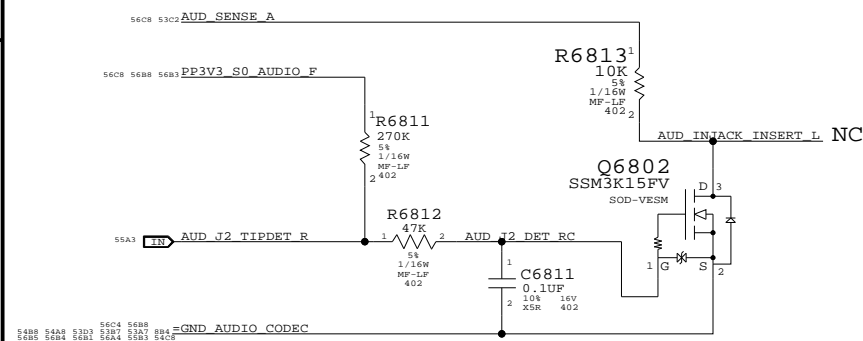
PLACE L6800/C6800 CLOSE TO Q6800  
L6800  
FERR-1000-OHM

MIC INPUT CIRCUITRY

PORT C LI



Line-in (PORT C) DETECT



AUDIO: JACK TRANSLATORS

SYNC\_MASTER=M7AUDIO SYNC\_DATE=03/12/2007

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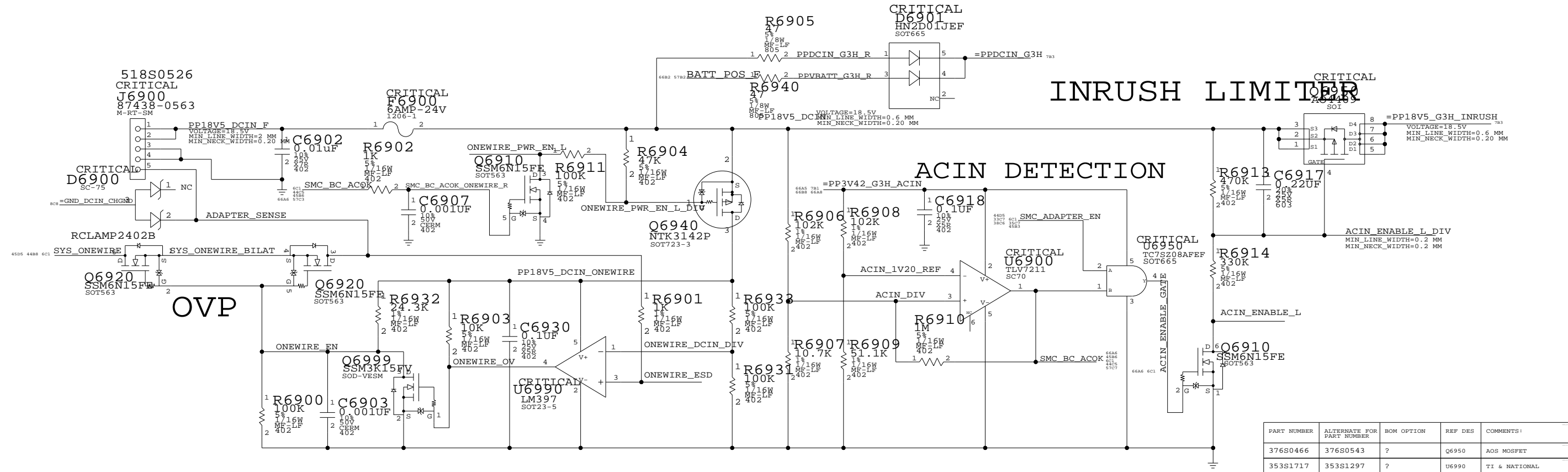
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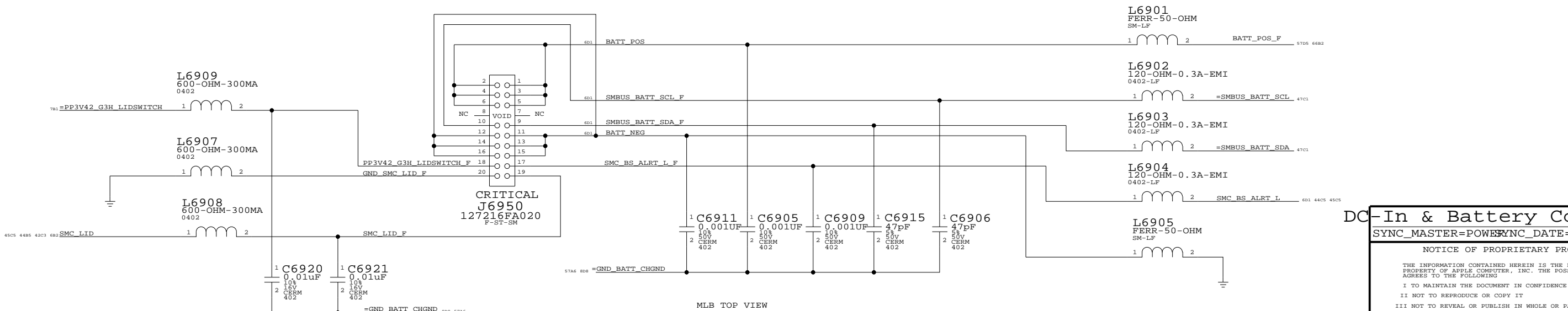
SIZE	DRAWING NUMBER	REV.
NONE	D 051-7455	01
SCALE	SHT	OF
NONE	56	76



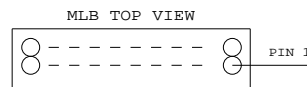
# DC-JACK INTERFACE



# BATTERY INTERFACE



LID HALL EFFECT SENSOR



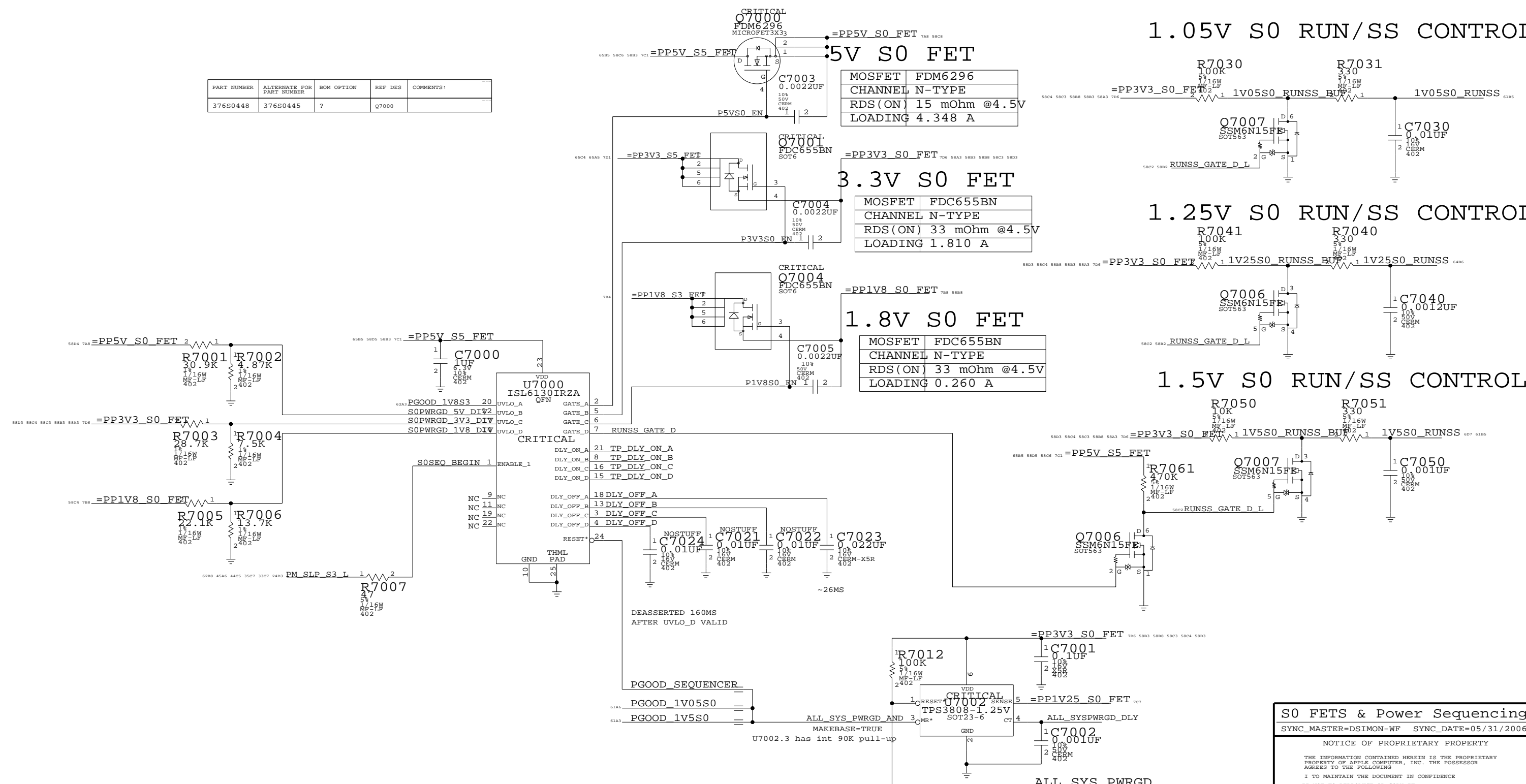
DC-In & Battery Connectors  
 SYNC\_MASTER=POWER\_NG\_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7455	01
SCALE	SHT	OF
NONE	57	76

# S0 FETS & POWER SEQUENCING & PGOOD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q7000	



1.05V S0 RUN/SS CONTROL

1.25V S0 RUN/SS CONTROL

1.5V S0 RUN/SS CONTROL

## S0 FETS & Power Sequencing

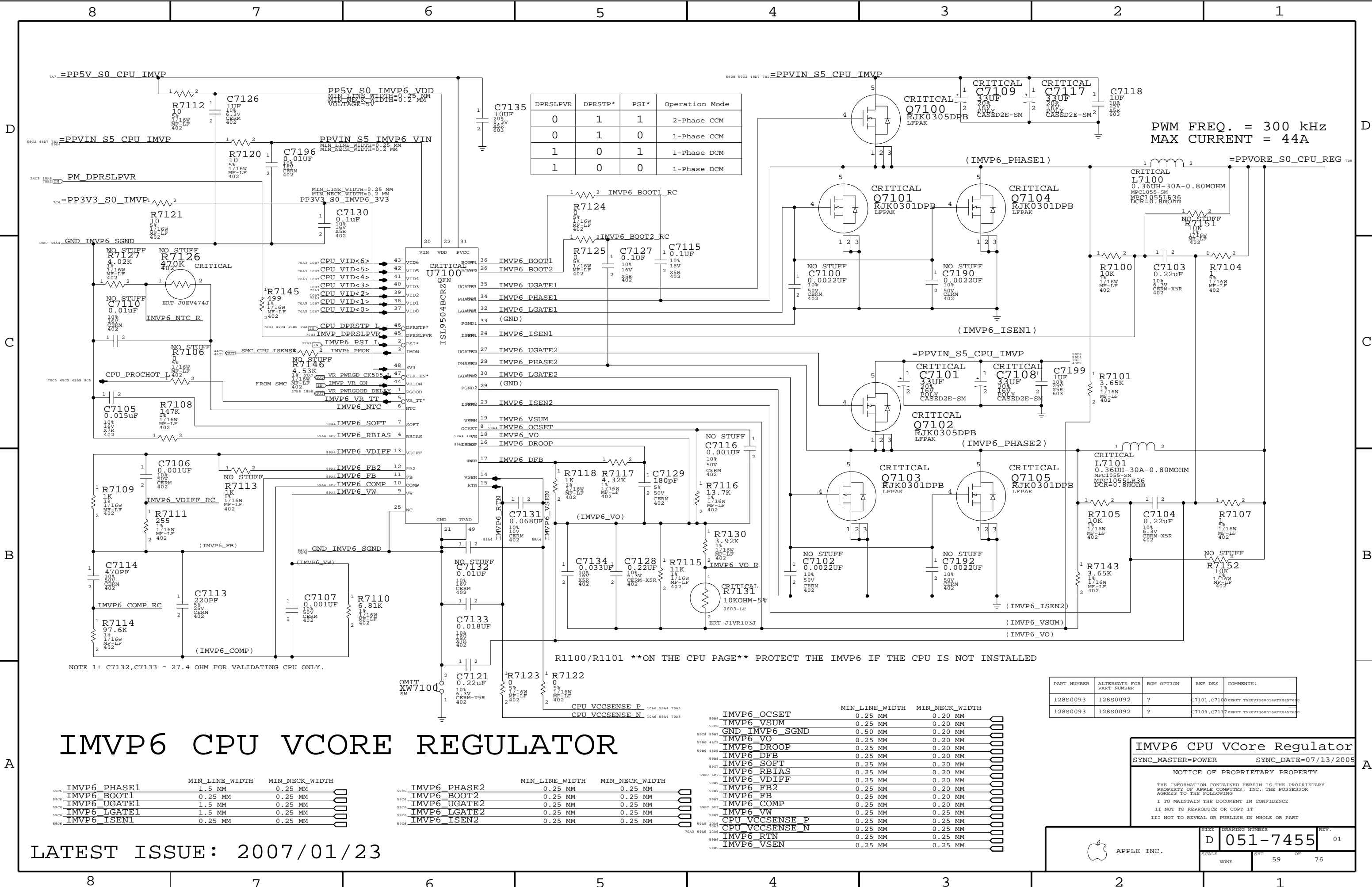
SYNC\_MASTER=DSIMON-WF SYNC\_DATE=05/31/2006

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LATEST ISSUE: 2007/01/02

APPLE INC.	SCALE	SHT	OF	REV.
	NONE	58	76	01



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

PWM FREQ. = 300 kHz  
MAX CURRENT = 44A

NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 \*\*ON THE CPU PAGE\*\* PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

# IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5986 IMVP6 PHASE1	1.5 MM	0.25 MM
5987 IMVP6 BOOT1	0.25 MM	0.25 MM
5988 IMVP6 UGATE1	1.5 MM	0.25 MM
5989 IMVP6 LGATE1	1.5 MM	0.25 MM
5990 IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5991 IMVP6 PHASE2	0.25 MM	0.25 MM
5992 IMVP6 BOOT2	0.25 MM	0.25 MM
5993 IMVP6 UGATE2	0.25 MM	0.25 MM
5994 IMVP6 LGATE2	0.25 MM	0.25 MM
5995 IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
5996 IMVP6_OCSET	0.25 MM	0.20 MM
5997 IMVP6_VSUM	0.25 MM	0.20 MM
5998 GND_IMVP6_SGND	0.50 MM	0.20 MM
5999 IMVP6_VO	0.25 MM	0.20 MM
5986 48C5 IMVP6_DROOP	0.25 MM	0.20 MM
5986 48C5 IMVP6_DFB	0.25 MM	0.20 MM
5986 IMVP6_SOFT	0.25 MM	0.20 MM
5987 IMVP6_RBIAS	0.25 MM	0.20 MM
5987 6D7 IMVP6_VDIFF	0.25 MM	0.20 MM
5987 IMVP6_FB2	0.25 MM	0.20 MM
5987 IMVP6_FB	0.25 MM	0.20 MM
5987 IMVP6_COMP	0.25 MM	0.20 MM
5987 6D7 IMVP6_VW	0.25 MM	0.25 MM
5987 CPU_VCCSENSE_P	0.25 MM	0.25 MM
5987 CPU_VCCSENSE_N	0.25 MM	0.25 MM
5987 10A5 IMVP6_RTN	0.25 MM	0.25 MM
5987 10A5 IMVP6_VSEN	0.25 MM	0.25 MM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7101,C7108	KEMET T520V336M016ATE0457690
128S0093	128S0092	?	C7109,C7117	KEMET T520V336M016ATE0457690

## IMVP6 CPU VCore Regulator

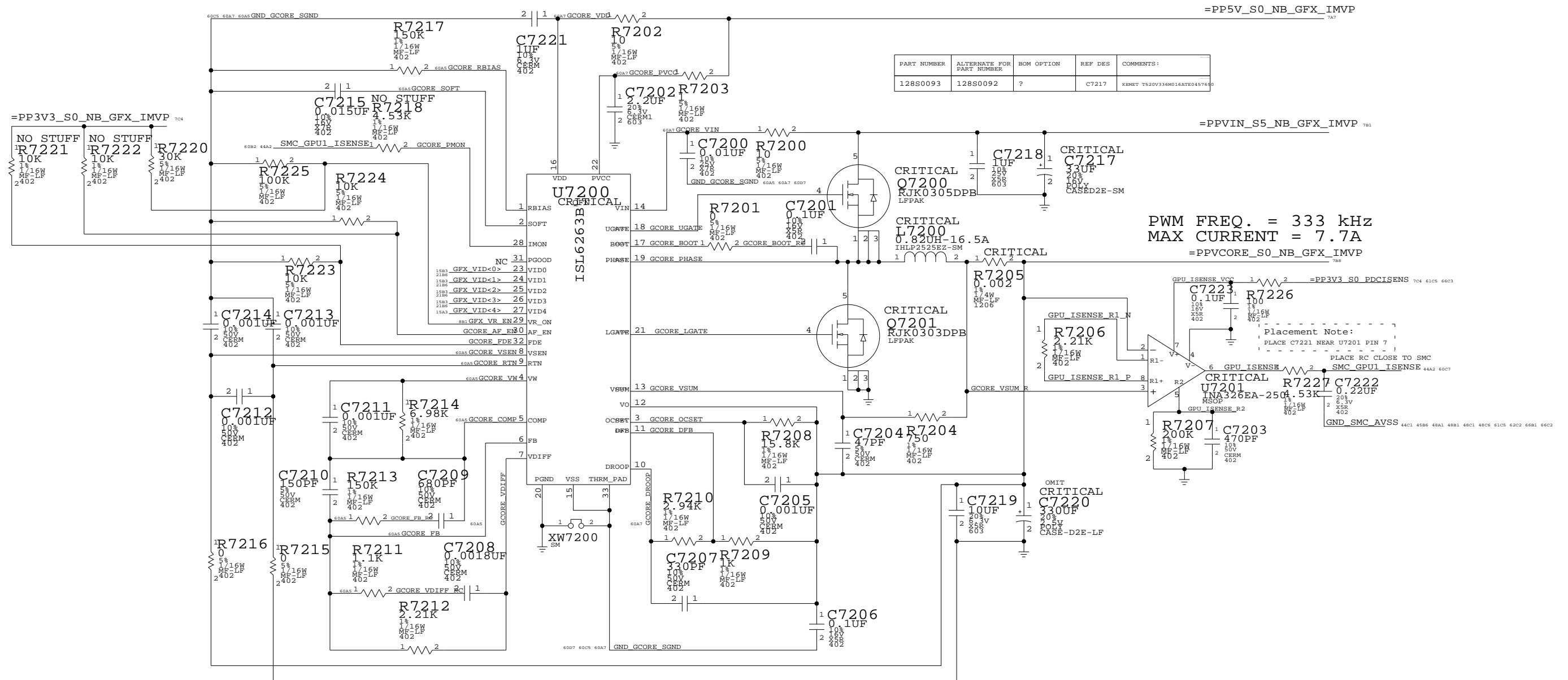
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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LATEST ISSUE: 2007/01/23

APPLE INC.	SCALE	SHEET	OF	REV.
	NONE	59	76	01

# RENDER VCORE POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7217	KEMET T520V3360C16ATK045760

PWM FREQ. = 333 kHz  
MAX CURRENT = 7.7A

Placement Note:  
PLACE C7221 NEAR U7201 PIN 7  
PLACE RC CLOSE TO SMC  
SMC GPU1 ISENSE 44A2 6007

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
60C5 GCORE_PHASE	1 MM	0.25 MM	489
60C5 GCORE_BOOT	0.3 MM	0.25 MM	494
60C5 GCORE_UGATE	1 MM	0.25 MM	495
60C5 GCORE_LGATE	1 MM	0.25 MM	496
60C5 GCORE_BOOT_RC	0.3 MM	0.25 MM	497
60C5 GND_GCORE_SGND	0.6 MM	0.25 MM	498
60C5 GCORE_VDD	0.3 MM	0.25 MM	499
60C5 GCORE_PVCC	0.3 MM	0.25 MM	500
60C5 GCORE_VIN	0.3 MM	0.25 MM	501
60C5 GCORE_DROOP	0.3 MM	0.25 MM	502
60C5 GCORE_VSUM	0.3 MM	0.25 MM	503
60C5 GCORE_DFB	0.3 MM	0.25 MM	504

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
60B5 GCORE_OCSET	0.3 MM	0.25 MM	485
60B5 GCORE_VW	0.3 MM	0.25 MM	486
60B5 GCORE_RTN	0.3 MM	0.25 MM	487
60B5 GCORE_VSEN	0.3 MM	0.25 MM	488
60B5 GCORE_RBIAS	0.3 MM	0.25 MM	489
60B5 GCORE_SOFT	0.3 MM	0.25 MM	490
60B5 GCORE_COMP	0.3 MM	0.25 MM	491
60B5 GCORE_FB	0.3 MM	0.25 MM	492
60B5 GCORE_VDIFF	0.3 MM	0.25 MM	493
60B5 GCORE_FB_RC	0.3 MM	0.25 MM	494
60B5 GCORE_VDIFF_RC	0.3 MM	0.25 MM	495

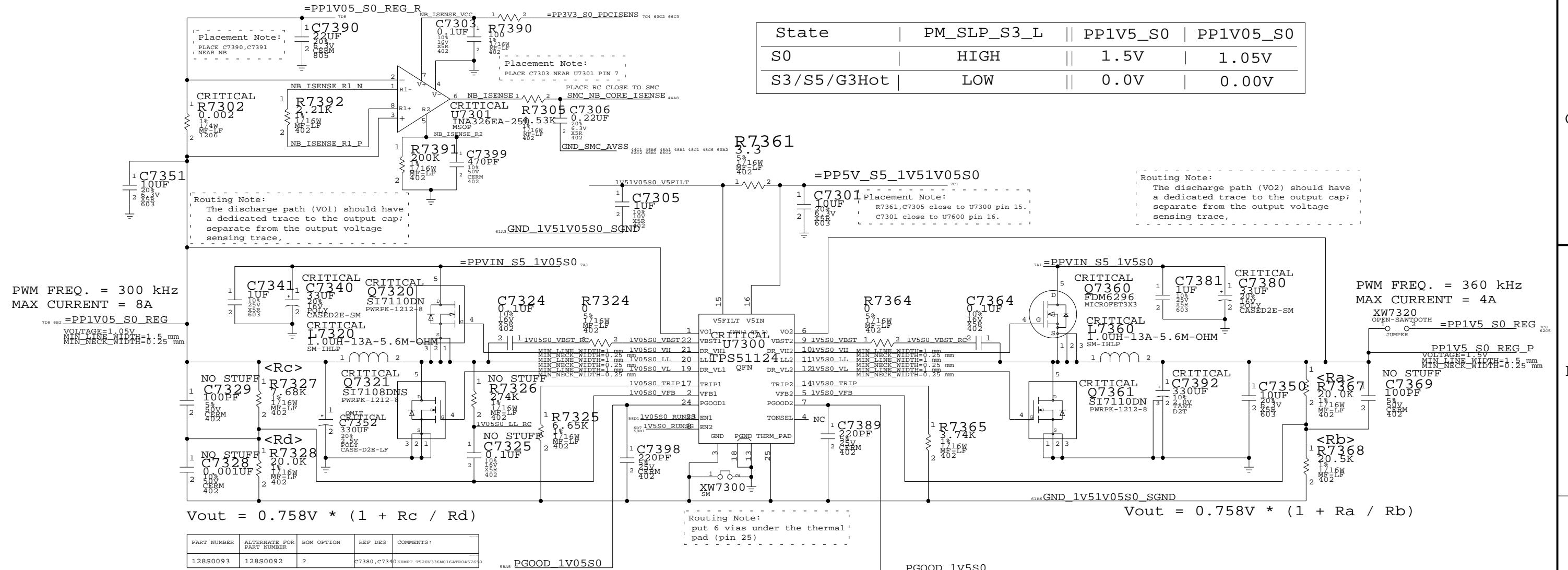
Render VCore Supplies  
SYNC\_MASTER=GPU SYNC\_DATE=06/29/2006  
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LATEST ISSUE: 2006/12/22

APPLE INC.	SCALE	SHT	OF	REV.
	NONE	60	76	01

# 1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



PWM FREQ. = 300 kHz  
MAX CURRENT = 8A

PWM FREQ. = 360 kHz  
MAX CURRENT = 4A

$$V_{out} = 0.758V * (1 + R_c / R_d)$$

$$V_{out} = 0.758V * (1 + R_a / R_b)$$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7380, C7340	KEMET T820V336M016AT8045740

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0448	376S0445	?	Q7360	

1.5V / 1.05V Supplies  
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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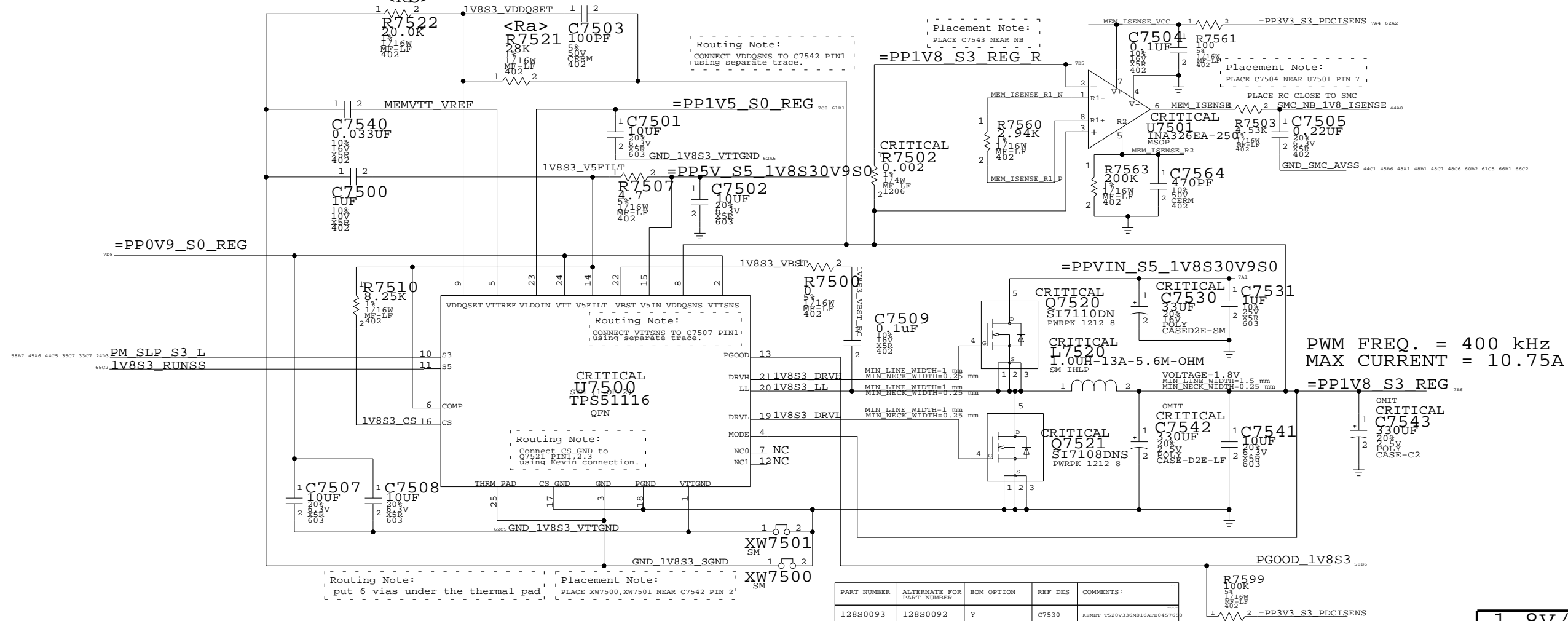
LATEST ISSUE: 2006/12/22

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-7455	01
SCALE		SHT	OF
		61	76

# 1.8V/0.9V POWER SUPPLY

State	PM_SLP_S4	IPM_SLP_S3	IPP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V

$$V_{out} = 0.75V * (1 + \frac{R_a}{R_b})$$



PWM FREQ. = 400 kHz  
MAX CURRENT = 10.75A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7530	KEYMET T520V336M016ATK0457650

1.8V/0.9V Supplies  
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7455	01
SCALE	NONE	SHT	62 OF 76

# 5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

$$V_{out} = 1V * (1 + R_a / R_b)$$

$$V_{out} = 1V * (1 + R_c / R_d)$$

Routing Note:  
The discharge path (VO1) should have a dedicated trace to the output cap; separate from the output voltage sensing trace,

Routing Note:  
The discharge path (VO2) should have a dedicated trace to the output cap; separate from the output voltage sensing trace,

Routing Note:  
put 6 vias under the thermal pad (pin 33)

PWM FREQ. = 280 kHz  
MAX CURRENT = 7.5A

PWM FREQ. = 430 kHz  
MAX CURRENT = 5A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682, C7680	KEMET T520V336M016AT0457610
128S0093	128S0092	?	C7640	KEMET T520V336M016AT0457610
376S0448	376S0445	?	Q7620	KEMET T520V336M016AT0457610

Placement Note:  
R7601, C7605 close to U7600 pin 20.  
C7602 close to U7600 pin 22.  
C7604 close to U7600 pin 21.  
C7603 close to U7600 pin 19.  
R7605, R7603 close to U7600.

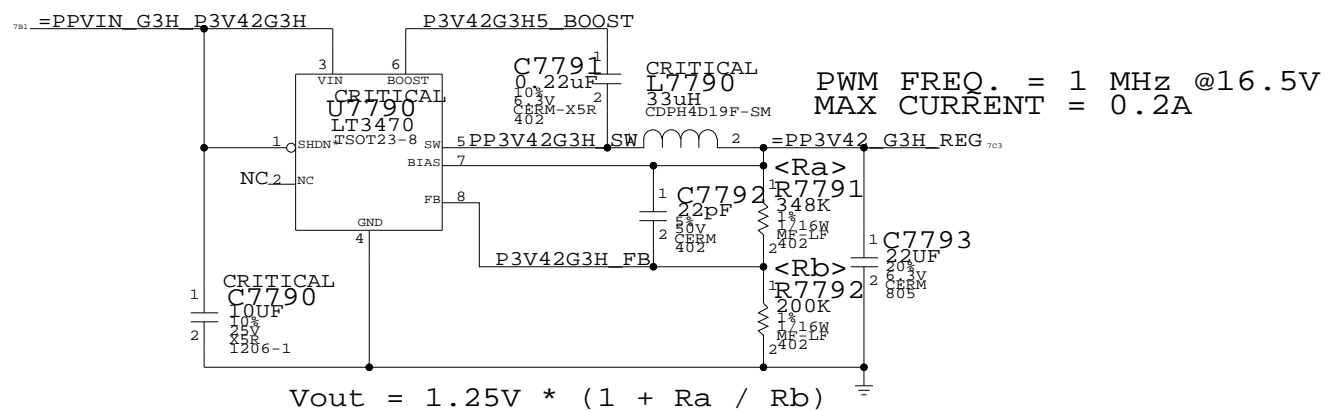
**5V/3.3V Supplies**  
 SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005  
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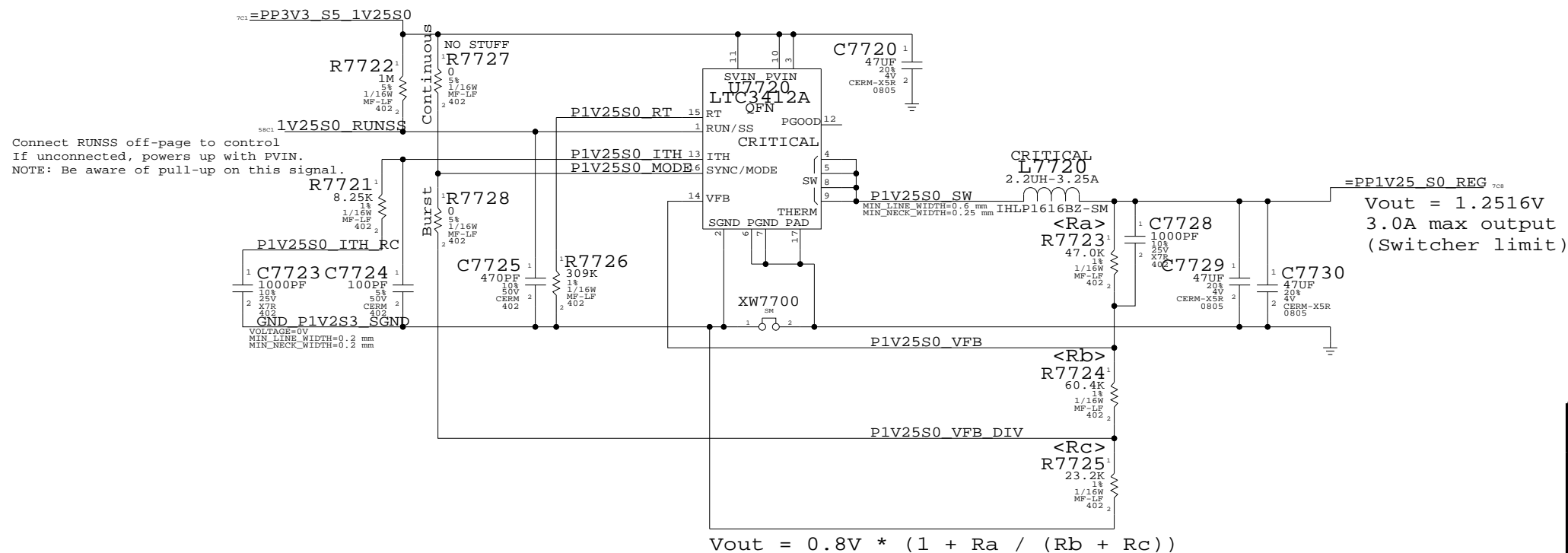
APPLE INC.  
 DRAWING NUMBER: D 051-7455 01  
 SCALE: NONE SHEET: 63 OF 76

# 3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



# 1.25V S0 REGULATOR



3.42V/1.25V Switcher

SYNC\_MASTER=ENESYNC\_DATE=12/06/2005

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SIZE DRAWING NUMBER REV.

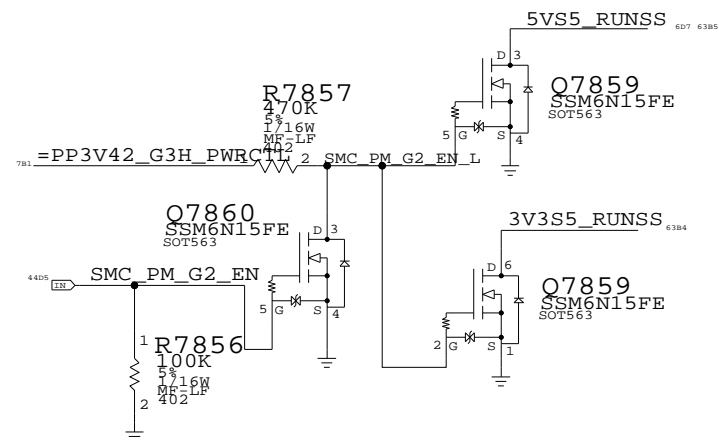
D 051-7455 01

SCALE NONE SHT 64 OF 76

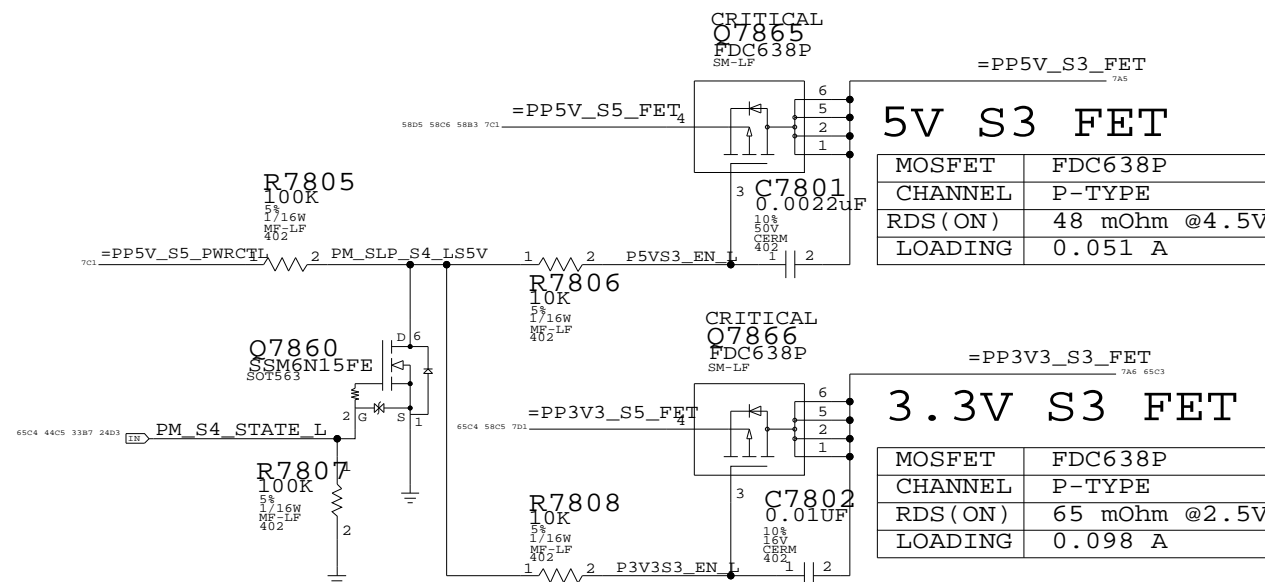
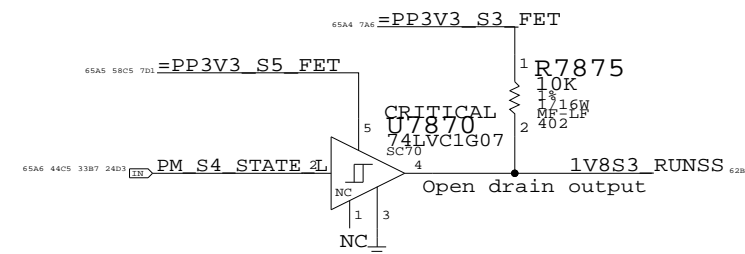


# S3 FETS & S3/S5 CONTROL

## 5V/3.3V S5 RUN/SS CONTROL



## 1.8V S3 RUN/SS CONTROL



5V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

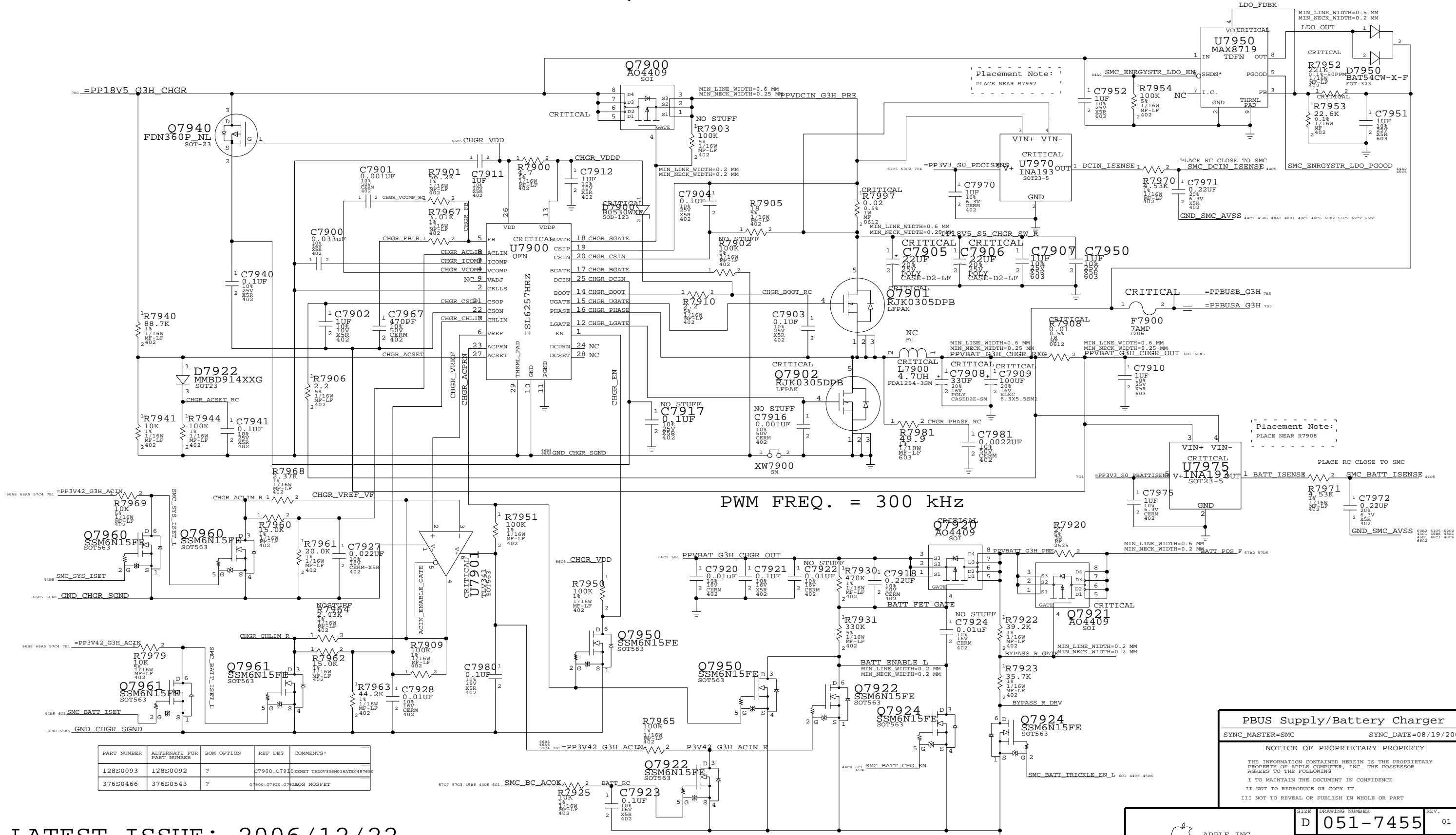
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

**S3 FET & S3/S5 Control**  
 SYNC\_MASTER=DSIMON DATE=06/12/2006  
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LATEST ISSUE: 2006/12/22

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	NONE	051-7455	01
SCALE		SHT	OF
NONE		65	76

# PBUS SUPPLY / BATTERY CHARGER



PWM FREQ. = 300 kHz

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7908, C7910	KEMET T520V336016ATE045760
376S0466	376S0543	?	Q7900, Q7920, Q7920S	MOSFET

## PBUS Supply/Battery Charger

SYNC\_MASTER=SMC SYNC\_DATE=08/19/2005

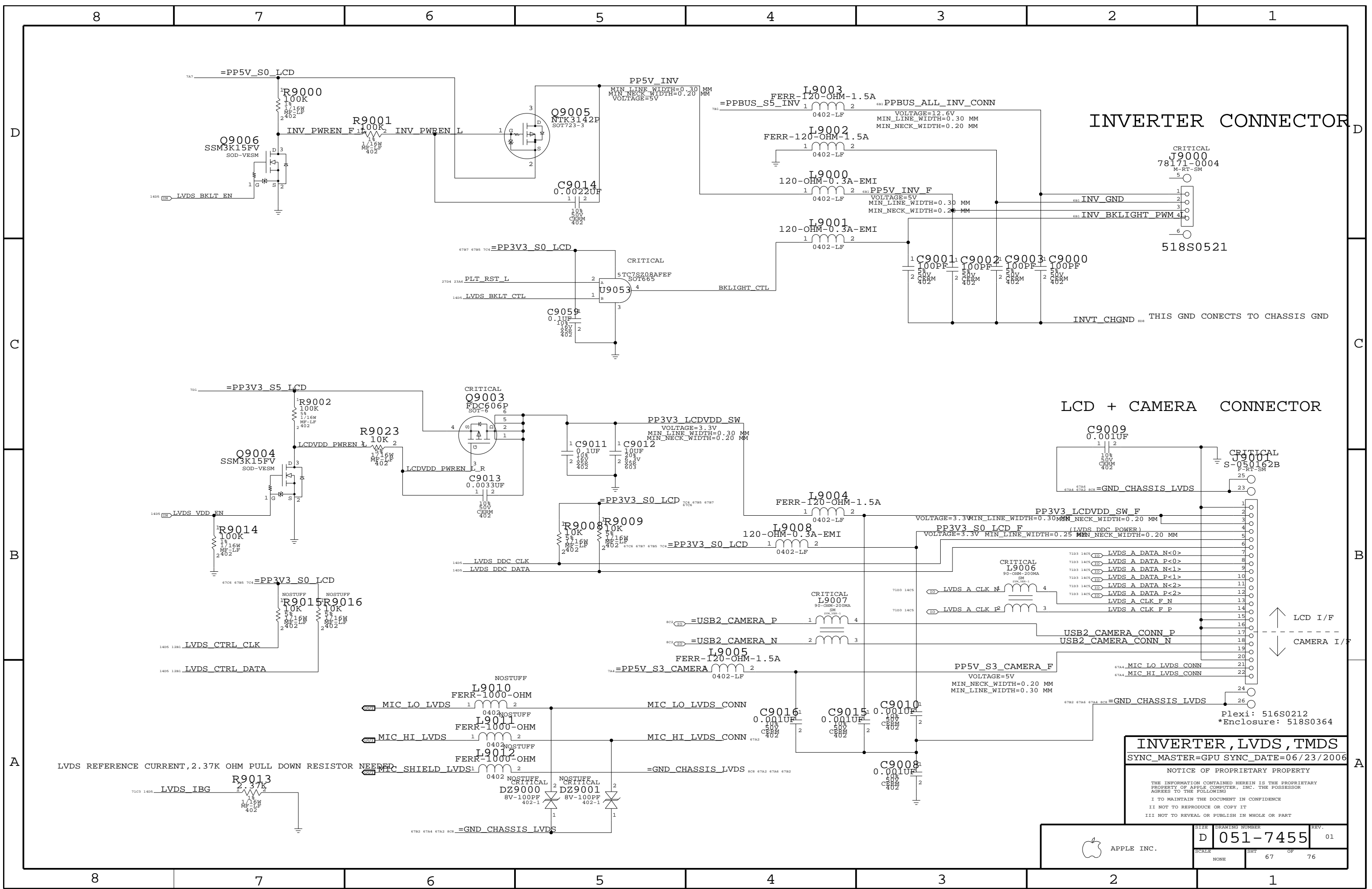
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LATEST ISSUE: 2006/12/22



SIZE	DRAWING NUMBER	REV.
	D 051-7455	01
SCALE	SHEET	OF
NONE	66	76



**INVERTER CONNECTOR**

**LCD + CAMERA CONNECTOR**

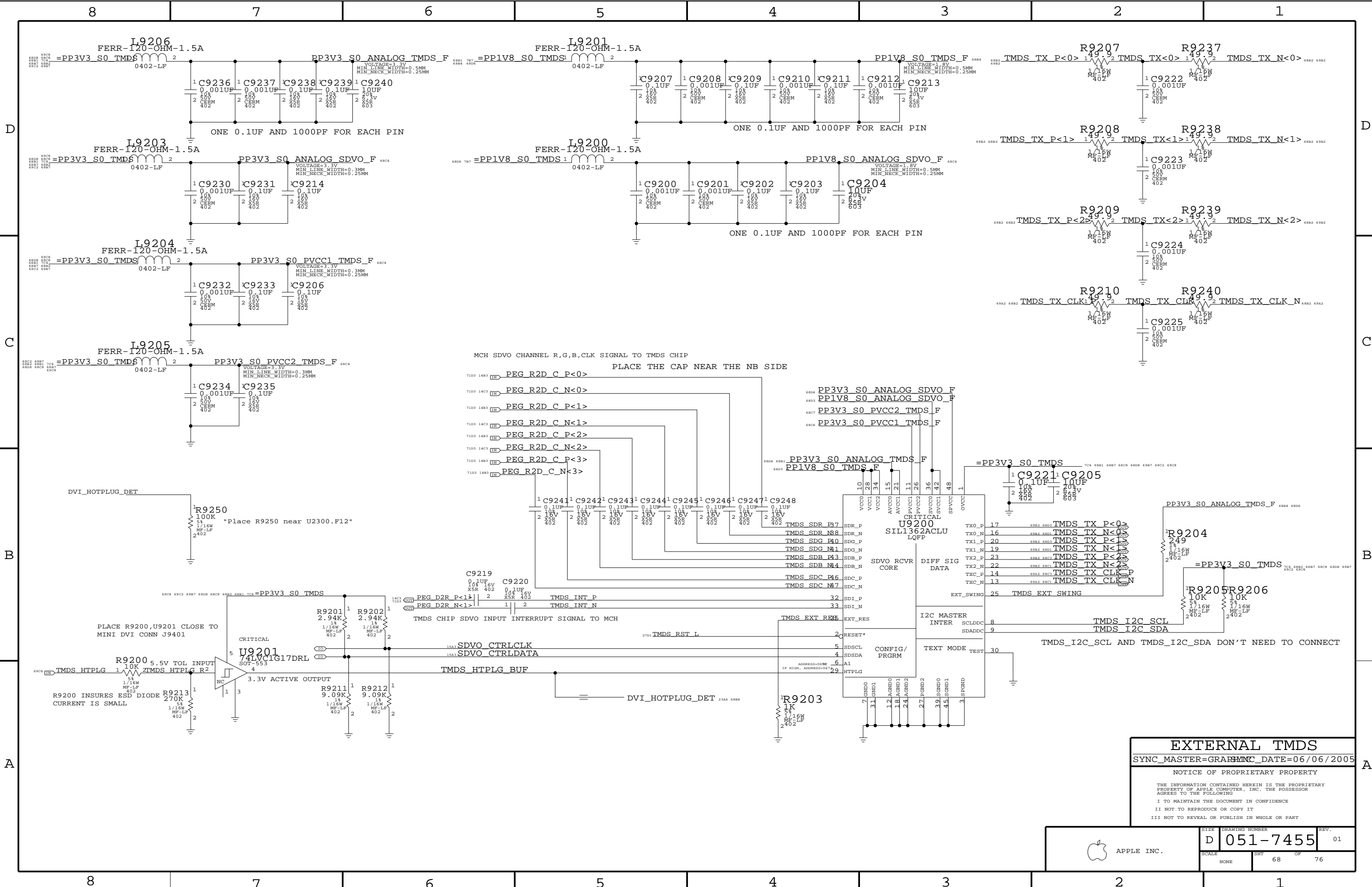
**INVERTER, LVDS, TMDS**

SYNC\_MASTER=GPU SYNC\_DATE=06/23/2006  
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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7455	REV.: 01
	SCALE: NONE	SHEET: 67	OF: 76

LVDS REFERENCE CURRENT, 2.37K OHM PULL DOWN RESISTOR NEEDED

Plexi: 516S0212  
 \*Enclosure: 518S0364



**EXTERNAL TMDS**  
 SYNC\_MASTER=GRABMNC\_DATE=06/06/2005

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APPLE INC.	SCALE	SHEET	OF	REV.
	NONE	68	76	01

NB VIDEO ALIASES

1445	=CRT_TVO_IREF	CRT_TVO_IREF	1489 71C3	=CRT_BLUE	CRT_BLUE	6988 71C3
1445	=TV_A_DAC	TV_A_DAC	MAKE_BASE=TRUE 6988 71C3			
1485	=TV_B_DAC	TV_B_DAC	MAKE_BASE=TRUE 6988 71C3	=CRT_GREEN	CRT_GREEN	6988 71C3
1485	=TV_C_DAC	TV_C_DAC	MAKE_BASE=TRUE 6988 71C3			
1485	=CRT_RED	CRT_RED	MAKE_BASE=TRUE 6988 71C3			
1485	=CRT_HSYNC_R	CRT_HSYNC_R	69C3 71C3			
1445	=CRT_VSYNC_R	CRT_VSYNC_R	69C3 71C3			

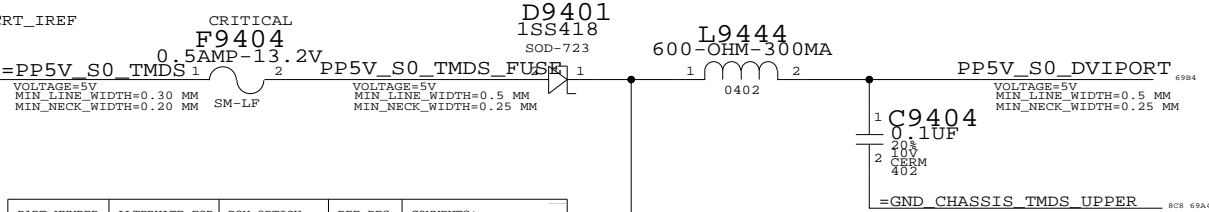
Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

TMDS (MINI DVI) INTERFACE

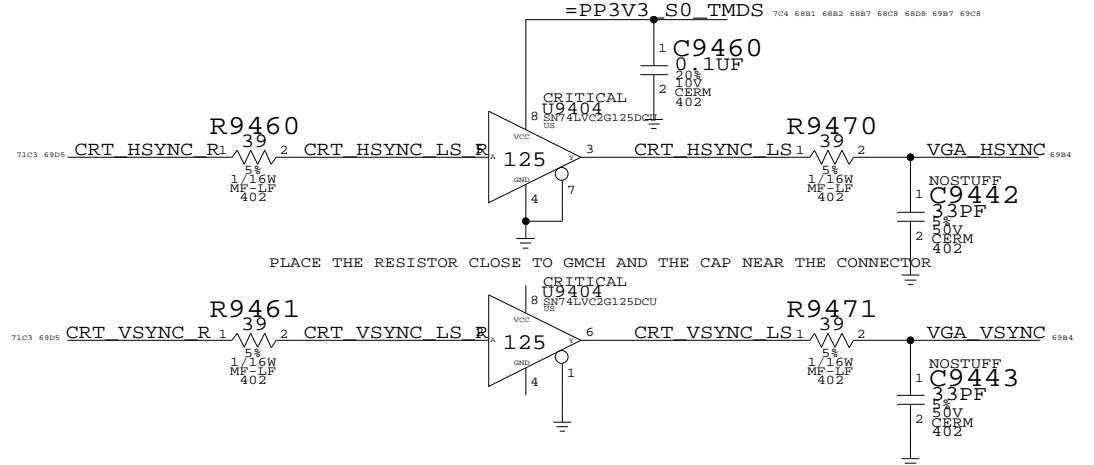
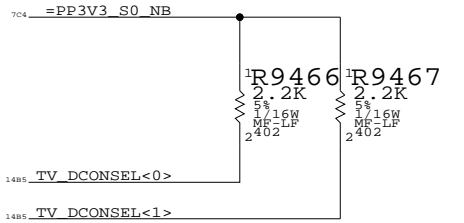
Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT\_IREF AND GROUND



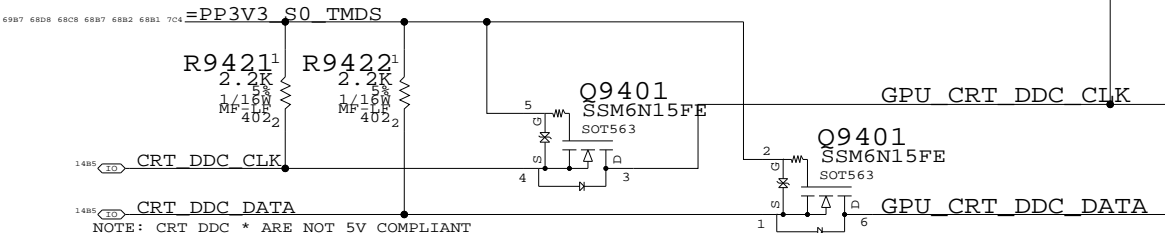
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
740S0044	740S0028	?	F9404	

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR



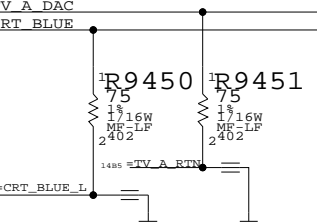
DVI power DIODE on page 95 (D9500)

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

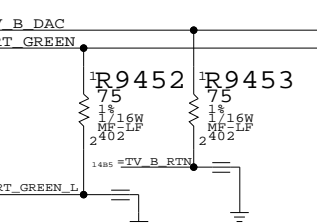


NOTE: CRT\_DDC\_\* ARE NOT 5V COMPLIANT

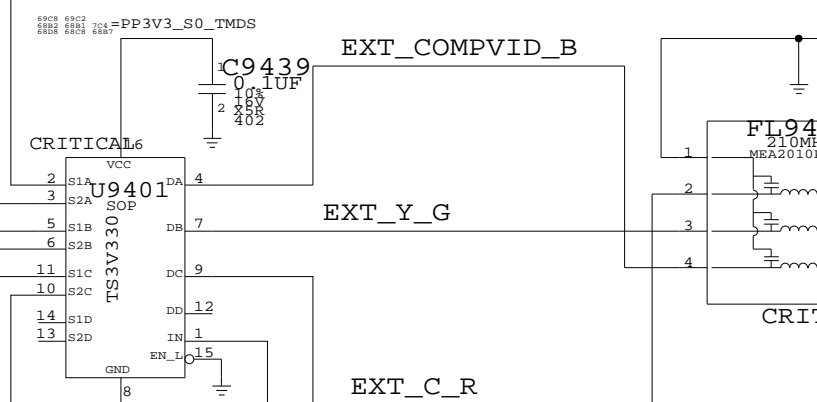
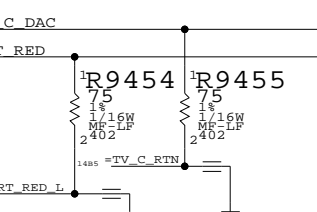
PLACE R9450 R9451 CLOSE TO GMCH



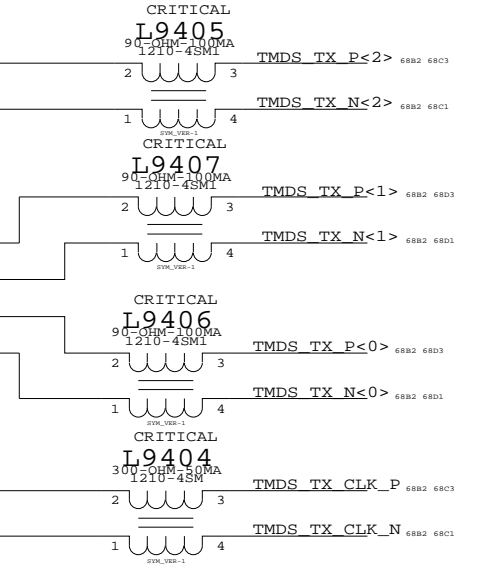
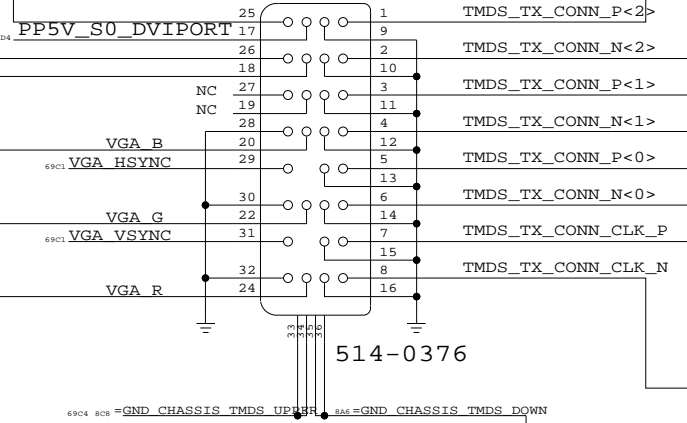
PLACE R9452 R9453 CLOSE TO GMCH



PLACE R9454 R9455 CLOSE TO GMCH



OMIT CRITICAL J9401 MINI-DVI-M42-BLK F-RT-TH



MINI-DVI CONNECTOR

SYNC\_MASTER=EUGENESYNC\_DATE=05/21/05

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0480	1	CONN_REC_MINI-DVI_32P_RA,TABS_MG3	J9401	CRITICAL	NORMAL
514-0481	1	CONN_REC_MINI-DVI_32P_RA,TABS_BLK	J9401	CRITICAL	FANCY

APPLE INC.

SCALE NONE SHEET 69 OF 76

D 051-7455 01



### PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

### Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.  
 CRT & TVDAC signal single-ended impedance varies by location:  
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.  
 - 50-ohm +/- 15% from first to second termination resistor.  
 - 55-ohm +/- 15% from second termination resistor to connector.  
 CRT\_HSYNC/CRT\_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG D2R N<1>	1403 6886
	PCIE_100D	PCIE	PEG D2R P<1>	1403 6886
	PCIE_100D	PCIE	PEG R2D_C P<3..0>	1403 6886 680C
	PCIE_100D	PCIE	PEG R2D_C N<3..0>	1403 1403 6886 680C
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>	1503 2302
	DMI_100D	DMI	DMI N2S N<3..0>	1503 2302
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>	1503 2302
	DMI_100D	DMI	DMI S2N N<3..0>	1503 1503 2302
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P	1405 6783
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N	1405 6783
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>	1405 6782
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>	1405 6782
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>	
LVDS_IBG		LVDS	LVDS_IBG	1405 6748
CRT_TVO_IREF		CRT	CRT TVO_IREF	6907 6908
CRT_RED	CRT_50S	CRT	CRT RED	6908 6905
CRT_GREEN	CRT_50S	CRT	CRT GREEN	6908 6905
CRT_BLUE	CRT_50S	CRT	CRT BLUE	6908 6905
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R	6903 6905
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R	6903 6905
TV_A_DAC	CRT_50S	TVDAC	TV A DAC	6908 6907
TV_B_DAC	CRT_50S	TVDAC	TV B DAC	6908 6907
TV_C_DAC	CRT_50S	TVDAC	TV C DAC	6908 6907

### NB Constraints

SYNC\_MASTER=WFERRY SYNC\_DATE=06/12/2006

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D	051-7455	01
SCALE	SHT	OF
NONE	71	76

DDR2 Memory Bus Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW\_ROUTE\_ON\_LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include MEM\_45S, MEM\_55S, MEM\_70D, MEM\_85D.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include MEM\_CLK2MEM, MEM\_CTRL2CTRL, MEM\_CTRL2MEM, MEM\_CMD2CMD, MEM\_CMD2MEM, MEM\_DATA2DATA, MEM\_DATA2MEM, MEM\_DQS2MEM, MEM\_2OTHER.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CLK, MEM\_CTRL, MEM\_CMD, MEM\_DATA, MEM\_DQS.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CMD, MEM\_CTRL, MEM\_DATA, MEM\_DQS.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CTRL, MEM\_CMD, MEM\_DATA, MEM\_DQS.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_DATA, MEM\_CTRL, MEM\_CMD, MEM\_DATA.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CLK, MEM\_CTRL, MEM\_CMD, MEM\_DATA, MEM\_DQS.

Table with 4 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_DQS, MEM\_CTRL, MEM\_CMD, MEM\_DATA.

Need to support MEM\*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

Large table with columns: ELECTRICAL\_CONSTRAINT\_SET, NET\_TYPE, PHYSICAL, SPACING. Rows list various memory constraints like MEM\_CLK, MEM\_CTRL, MEM\_CMD, MEM\_DATA, MEM\_DQS, MEM\_DM, MEM\_DQS, MEM\_B, MEM\_C, MEM\_D.

Memory Constraints

SYNC\_MASTER=WFERRY SYNC\_DATE=06/08/2006

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### Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

### HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

### USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

### Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SYMBOL	REFERENCE
	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	2284 2204 3903 3905
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	2284 3983 3985
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L	2284 3983
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3 L	2284 3983
IDE_PDIOW	IDE_55S	IDE	IDE_PDIOW L	2284 3985
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR L	2284 3983
IDE_PDDACK	IDE_55S	IDE	IDE_PDDACK L	2284 3983
IDE_PDDRQ	IDE_55S	IDE	IDE_PDDRQ	2284 3983
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	2284 3985
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	2284 3985
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L	2286 3988
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D C P	2286 4004
SATA_100D	SATA_100D	SATA	SATA_A_R2D C N	2286 4004
SATA_100D	SATA_100D	SATA	SATA_A_R2D P	4007
SATA_100D	SATA_100D	SATA	SATA_A_R2D N	4007
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R P	2286 4004
SATA_100D	SATA_100D	SATA	SATA_A_D2R N	2286 4004
SATA_100D	SATA_100D	SATA	SATA_A_D2R C P	4007
SATA_100D	SATA_100D	SATA	SATA_A_D2R C N	4007
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	8A6 2208
HDA_55S	HDA_55S	HDA	HDA_BIT_CLK R	2208
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	8A6 2208
HDA_55S	HDA_55S	HDA	HDA_SYNC R	2208
HDA_RST_L	HDA_55S	HDA	HDA_RST L	8A6 2208
HDA_55S	HDA_55S	HDA	HDA_RST L R	2208
HDA_SDINO	HDA_55S	HDA	HDA_SDINO	8A6 2208
HDA_SDOU_T	HDA_55S	HDA	HDA_SDOU_T	8A6 2288
HDA_55S	HDA_55S	HDA	HDA_SDOU_T R	2288
USB_EXT_A	USB_90D	USB	USB_EXT_A P	8C1 2302
USB_90D	USB_90D	USB	USB_EXT_A N	8C1 2302
USB_90D	USB_90D	USB	USB_EXT_A MUXED P	
USB_90D	USB_90D	USB	USB_EXT_A MUXED N	
USB_MINI	USB_90D	USB	USB_MINI P	8C1 2302
USB_90D	USB_90D	USB	USB_MINI N	8C1 2302
USB_3G	USB_90D	USB	USB_3G P	
USB_90D	USB_90D	USB	USB_3G N	
USB_CAMERA	USB_90D	USB	USB_CAMERA P	8C1 2302
USB_90D	USB_90D	USB	USB_CAMERA N	8C1 2302
USB_BT	USB_90D	USB	USB_BT P	8C1 8C2 2302
USB_90D	USB_90D	USB	USB_BT N	883 882 2302
USB_TPAD	USB_90D	USB	USB_TPAD P	8C1 2302
USB_90D	USB_90D	USB	USB_TPAD N	8C1 2302
USB_IR	USB_90D	USB	USB_IR P	8C1 8C2 2302
USB_90D	USB_90D	USB	USB_IR N	8C1 8C2 2302
USB_EXT_B	USB_90D	USB	USB_EXT_B P	881 2302
USB_90D	USB_90D	USB	USB_EXT_B N	881 2302
USB_EXCARD	USB_90D	USB	USB_EXCARD P	881 2302
USB_90D	USB_90D	USB	USB_EXCARD N	881 2302
USB_EXTC	USB_90D	USB	USB_EXTC P	881 2302
USB_90D	USB_90D	USB	USB_EXTC N	881 2302
USB_RBIA_S	USB_60S	USB	USB_RBIA_S	2383
SMB_SB_SCT	SMB_55S	SMB	SMB_CLK	2405 4708
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	2405 4708
SMB_SB_ME_SCT	SMB_55S	SMB	SMB_ME_CLK	2405 4748
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	2405 4748
SPI_SCLK	SPI_55S	SPI	SPI_SCLK R	2305 5207
SPI_55S	SPI_55S	SPI	SPI_A_SCLK R	5205
SPI_ST	SPI_55S	SPI	SPI_ST R	2305 5203
SPI_55S	SPI_55S	SPI	SPI_A_ST R	5204
SPI_SO	SPI_55S	SPI	SPI_SO	2305 5203
SPI_55S	SPI_55S	SPI	SPI_A_SO R	5204
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R L<0>	2305 5207
SPI_55S	SPI_55S	SPI	SPI_CE_L<0>	5205
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R L<1>	

### SB Constraints (1 of 2)

SYNC\_MASTER=WFERRY SYNC\_DATE=06/12/2006

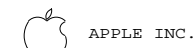
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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	Y	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

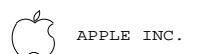
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	23A8 23B8 37B5 37C5
PCI_AD19	PCI_55S	PCI	PCI AD<19>	23A8 37B6
PCI_AD20	PCI_55S	PCI	PCI AD<20>	23A8 37B5
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	23A8 37B5
PCI_AD	PCI_55S	PCI	PCI PAR	23A6 37B5
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	23B6 37B5
PCI_CNTL	PCI_55S	PCI	PCI IRDY_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI DEVSEL_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI PERR_L	23A4 23A6 37A5
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	23A4 23A6
PCI_CNTL	PCI_55S	PCI	PCI SERR_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI STOP_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI TRDY_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI FRAME_L	23A4 23A6 37A5
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	23A4 23B6 37A5
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	23B5 37A5
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	23A4 23B6
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	23A4 23B6
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	
INT_PIROA_L	PCI_55S	PCI	INT PIROA_L	23A4 23A8
INT_PIROB_L	PCI_55S	PCI	INT PIROB_L	23A4 23A8
INT_PIROC_L	PCI_55S	PCI	INT PIROC_L	23A4 23A8
INT_PIROD_L	PCI_55S	PCI	INT PIROD_L	23A4 23A8 37A5
INT_PIROE_L	PCI_55S	PCI	INT PIROE_L	23A4 23A6
INT_PIROF_L	PCI_55S	PCI	INT PIROF_L	23A4 23A6
PCI_E_R2D	PCI_E_100D	PCI_E	PCI_E R2D C P	33B5 33B6
PCI_E_100D	PCI_E_100D	PCI_E	PCI_E R2D C N	33B5 33B6
PCI_E_D2R	PCI_E_100D	PCI_E	PCI_E D2R P	33B5
PCI_E_100D	PCI_E_100D	PCI_E	PCI_E D2R N	33B5 33C5
GLAN_COMP			GLAN_COMP	22C5
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC	
ENET_LAN	LAN_55S	ENET_LAN	LAN R2D<2..0>	
ENET_LAN	LAN_55S	ENET_LAN	LAN D2R<2..0>	
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK R	
LAN_55S	ENET_CLK		ENET_GLAN_CLK	
ENET_MDI0	ENET_100D	ENET_MDI	ENET MDI P<0>	34B8 36B7
ENET_100D	ENET_MDI		ENET MDI N<0>	34B8 36B7
ENET_MDI1	ENET_100D	ENET_MDI	ENET MDI P<1>	34B8 36C7
ENET_100D	ENET_MDI		ENET MDI N<1>	34B8 36C7
ENET_MDI2	ENET_100D	ENET_MDI	ENET MDI P<2>	34B8 36B7
ENET_100D	ENET_MDI		ENET MDI N<2>	34B8 36C7
ENET_MDI3	ENET_100D	ENET_MDI	ENET MDI P<3>	34B8 36C7
ENET_100D	ENET_MDI		ENET MDI N<3>	34B8 36C7
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	15A3 24C3
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	15A3 24C3
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET L	15A3 24C3
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	24C3
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	24C3
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET L	24C3
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	15A4
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	24C3
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	24C3

SB Constraints (2 of 2)

SYNC\_MASTER=WFERRY SYNC\_DATE=06/12/2006

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SHEET	74	OF 76

### Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

### Clock Net Properties

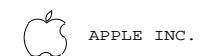
ELECTRICAL_CONSTRAINT_SET	NET TYPE		PROPERTY	VALUE
	PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	6C7 28C4 29D6
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	6C7 28C4 29D6
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	6C7 28C4 29D6
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	6C7 28C4 29D6
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	6C7 28C4 29D6
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	6C7 28C4 29D6
CK505_PCIE0	CLK_MED_55S	CLK_MED	CK505_PCIE0_CLK	2886 2986
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	6C7 2886 2986
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1_CLK	2886 2986
CK505_PCIE2	CLK_MED_55S	CLK_MED	CK505_PCIE2_CLK	8C4 2886
CK505_PCIE3	CLK_MED_55S	CLK_MED	CK505_PCIE3_CLK	2886 2986
CK505_PCIE4	CLK_MED_55S	CLK_MED	CK505_PCIE4_CLK	8C4 2886
CK505_PCIE5	CLK_MED_55S	CLK_MED	CK505_PCIE5_FCTSEL1	2886 2982
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_USB48_FSA	28A4 29D8
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_CLK14P3M_TIMER	28A4 29D8
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	6C7 28A4 2986
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	6C7 28A4 2986
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	6C7 2884 29C6
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	6C7 2884 29C6
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	6C7 2884 29C6
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	6C7 2884 29C6
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	6C7 2884 29C6
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	6C7 2884 29C6
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	6C7 2884 29C6
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	6C7 2884 29C6
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	6C7 2884 29C6
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	6C7 2884 2986
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	6B7 28A4 2986
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	6B7 28A4 2986
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	986 29D3
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	986 29D3
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	1383 29D3
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	1383 29D3
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	70A3
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	70A3
(CK505_PCIE0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6C2 29B3 46C4
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	21A6 29A5 29B3
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	29A5 29B3 37A5
(CK505_PCIE2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCIE3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	29A3 29A5 44C8
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_PCI4 is project-specific	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	24D3 29A5 29D6
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	24D3 29A5 29D6
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	29C8 29D6
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	29A8 29D6
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	8B1 29B3
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	8B1 29B3
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	8B1 29C3
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	8A1 29C3
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	23C2 29C3
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	23D2 29C3
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	2286 29C3
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	2286 29C3
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	15C3 29C3
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	15C3 29C3
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29C3 33C5
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29A3 33C5
			CK505_SRC7 is project-specific	
			CK505_SRC8 is project-specific	

### Clock Constraints

SYNC\_MASTER=WFERRY SYNC\_DATE=06/12/2006

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NONE	051-7455	01
SCALE	SHT	OF
	75	76

### FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

### FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
FW_D_CTL	FW_55S	FW	FW LINK<7..0>
FW_D_CTL	FW_55S	FW	FW CTL<1..0>
FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK
FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK
FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK
FW_LKON	FW_55S	FW	FW LKON
FW_LKON	FW_55S	FW	FW LKON R
FW_LPS	FW_55S	FW	FW LPS
FW_LREQ	FW_55S	FW	FW LREQ
FW_PINT	FW_55S	FW	FW PINT
FWPHY_CLK98P304M_XT	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
FWPHY_CLK98P304M_XT	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
FW_0_TPA	FW_110D	FW_TP	FW 0 TPA P
FW_0_TPA	FW_110D	FW_TP	FW 0 TPA N
FW_0_TPB	FW_110D	FW_TP	FW 0 TPB P
FW_0_TPB	FW_110D	FW_TP	FW 0 TPB N
FW_1_TPA	FW_110D	FW_TP	FW 1 TPA P
FW_1_TPA	FW_110D	FW_TP	FW 1 TPA N
FW_1_TPB	FW_110D	FW_TP	FW 1 TPB P
FW_1_TPB	FW_110D	FW_TP	FW 1 TPB N
Port 2 Not Used			

### SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL 4702
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA 4702
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL 682 4705
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA 682 4705
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL 4705
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA 4705
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL 4702
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA 4702
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL 4782
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA 4782

### FireWire & SMC Constraints

SYNC\_MASTER=WFERRY SYNC\_DATE=06/12/2006

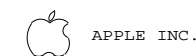
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