1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
		546198			

SCHEM,MLB,M82
PVT
11/14/2007

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7230	1	SCHEM,MLB,M82	SCH	CRITICAL	
820-2179	1	PCBF,MLB,M82	PCB	CRITICAL	

DRAWING
TITLE=M82_MLB
ABBREV=DRAWING
LAST_MODIFIED=Wed Nov 14 17:25:50 2007

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH
NOTED AS
APPLICABLE

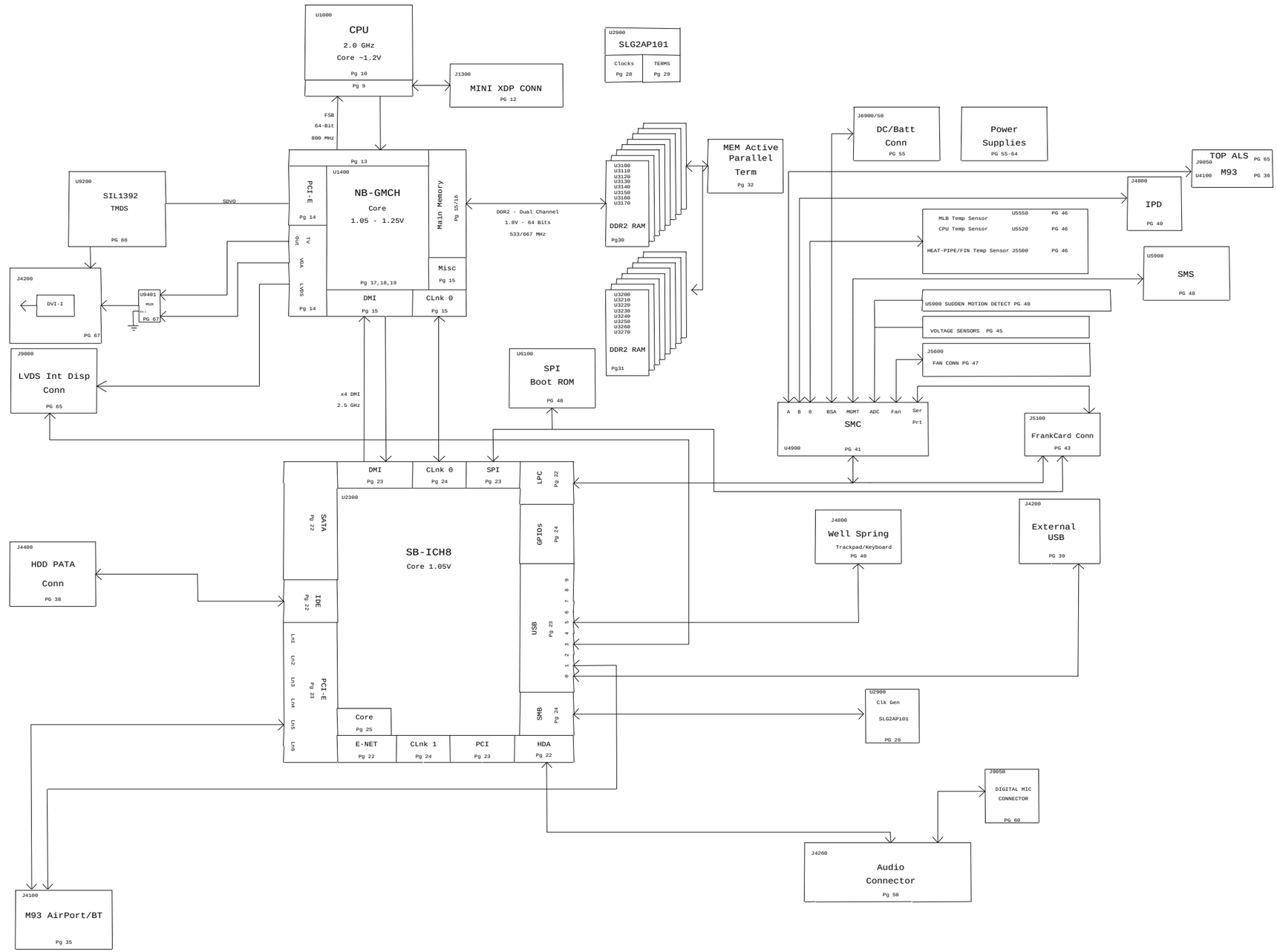
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M82

DRAWING NUMBER 051-7230
REV. B.0.0

SHT 1 OF 73



System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	2	73

M82 POWER SYSTEM ARCHITECTURE

AC ADAPTER IN — J6980 — PP18V5_DCIN — 6A FUSE F6900 — =PP18V5_G3H_CHGR

=PPDCIN_G3H, PPVBAT_G3H_R, PPBUSB_G3H — D6901 ×3 — =PPDCIN_G3H

ENABLE — 3.425V G3HOT LT1934 U7790 (PAGE 62) — PP3V42_G3H_REG (? A MAX CURRENT) — PP3V42_G3H_SMC

SMC PWRGD RN5VD30A-F U5000 (PAGE 41) — SMC_RESET_L

SMC_BATT_CHG_EN

ENABLES — PBUS CONVERTER/ BATTERY CHARGER ISL6258 U7900 (PAGE 63) — VOUT — CHGR_SMBUS

PPVBAT_G3H_CHGR_REG — 7A FUSE — PPBUSB_G3H — R7980 — =PBUSA_G3H

BATTERY 2S2P

Q7950 — R7930 — CHGR_BGATE — BATT_POS_F

1V05S0_RUNSS (S0) — 1.05V — PP1V05_S0_REG (9.9 A MAX CURRENT)

1V5S0_RUNSS (S0) — 1.5V — PP1V5_S0_REG (3.3 A MAX CURRENT)

TPS51124 U7300 (PAGE 58) — PGOOD_1V5S0, PGOOD_1V05S0

U2803 — VR_PWRGD_CK505 — VR_PWRGD_CLKEN

CLOCK — SLG2AP101 U2900 (PAGE 28) — CLK_PWRGD

ICH8M — CK_PWRGD, VRMPWRGD, PWROK — PWRBTN*, PLTRST*, RSMRST* — CPU_PWRGD(GPIO49) — U2300 (PAGE 22)

NB_RESET_L, TMDS_RST_L, AIRPORT_RST_L, LCDBKLT_PLT_RST_L, PLT_RST_L, CPU_PWRGD

U2880

PM_SB_PWROK — U2801

Q7860 — DELAY R-10K C-0.002uF P5VS3_EN_L (S3) — DELAY R-10K C-0.01uF P3V3S3_EN_L (S3)

CPUVCORE — ISL6261CRZ U7100 (PAGE 56) — VIN, VR_ON, IMVP_VR_ON, CLKEN#, PGOOD, VOUT

PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU (30 A MAX CURRENT)

VR_PWRGD_CK505_L

VR_PWRGOOD_DELAY

CPU — U1000 (PAGE 9) — PWRGOOD, RESET*

ICH — PM_S4_STATE_L, PM_SLP_S3_L

PPBUS_G3H

SMC — U4900 (PAGE 40) — PG2, PG3, P60 — SMC_PM_G2_EN (S5)

Q7000 — P5VS0_EN — PP5V_S0 — TPS79933 U2280 (PAGE 21) — P3V3_S0_NB_TVDAC (205mA MAX CURRENT)

Q7865 — P5VS3_EN_L — PP5V_S3

=PPBUSB_G3H — VIN 5V EN1 VO1 — 5VS5_RUNSS (S5) — PP5V_S5_REG (? A MAX CURRENT) — PP5V_S5

VIN 3.3V EN2 VO2 — 3V3S5_RUNSS (S5) — PP3V3_S5_REG (? A MAX CURRENT) — PP3V3_S5

TPS51120 U7600 (PAGE 60) — PGOOD1,2 — RSMRST_PWRGD

Q7866 — P3V3S3_EN_L — PP3V3_S3

1.25V S0 LTC3412A U7750 (PAGE 61) — 1V25S0_RUNSS — PP1V25_S0_REG (3 A MAX CURRENT)

CRESTLINE — U1400 (PAGE 13) — PWROK, H_CPURST* — FSB_CPURST_L

Q7001 — P3V3S0_EN — PP3V3_S0

U7002 — PP1V25_S0_FET, ALL_SYS_PWRGD_AND — ALL_SYS_PWRGD

SMC_ADAPTER_PRESENT — WOW_EN — PM_WLAN_EN_L

GPU_VCORE VCC — ADP3209 U7200 (PAGE 57) — VIN, EN, VOUT — PP5V_S0_NB_GFX_IMVP — GFX_VR_EN, GCORE_EN — =PPVCORE_S0_NB_GFX_IMVP (13 A MAX CURRENT)

SMC — U4900 (PAGE 40) — RSMRST_OUT(P15), PWRGD(P12) 99ms DLY, IMVP_VR_ON(P16), RSMRST_IN(P13), PLT_RST*, PWR_BUTTON(P90), P17(BTN_OUT), RST* — SLP_S5_L(P95), SLP_S4_L(P94), SLP_S3_L(P93)

PM_RSMRST_L, IMVP_VR_ON, SMC_LRESET_L, PM_PWRBTN_L, SMC_RESET_L

PGOOD_1V5S0, PGOOD_1V05S0, PGOOD_SEQUENCER

SMC_ONOFF_L — BATTERY ONLY: 05 — ADAPTER IN : 10-1

PM_SLP_S5_L, PM_S4_STATE_L, PM_SLP_S3_L

Q7004 — P1V8S0_EN — =PP1V8_S0_FET — =PP1V8_S0_NB_DPLL — MCH DPLL TPS731125 U2265 (PAGE 21) — VIN, ENA, VOUT — P1V25_S0_NB_DPLL

PP1V8_S3_FET — PP1V8_S3_REG (11 A MAX CURRENT)

R7870 — 1V8S3_RUNSS — PM_SLP_S3_L — VIN 1.8V VLDOIN S5 VOUT1 — S3 0.9V VOUT2 — TPS51116 U7500 (PAGE 59) — PP0V9_S0_REG — PGOOD_1V8S3

RUNSS_GATE_D — Q7006 Q7007 DELAY R-330 C-0.022uF 1V5S0_RUNSS (S0) — C-0.01uF 1V05S0_RUNSS (S0) — C-1000PF 1V25S0_RUNSS (S0)

U7000 — ISL6130IRZA — RST*, UVLO_A, UVLO_B, UVLO_C, UVLO)D, ENABLE_1 — GATE A, GATE B, GATE C, GATE D — (PAGE 56)

PGOOD_1V8S3, PP5V_S0_FET, PP3V3_S0_FET, PP1V8_S0_FET, PM_SLP_S3_L

P5VS0_EN, P3V3S0_EN, P1V8S0_EN, RUNSS_GATE_D

Power Block Diagram

SYNC_MASTER=POWER — SYNC_DATE=06/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 3 OF 73	

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7886	PCBA,MLB,1.6GHZ,MI 2GB,SS CAP,M82	EEE_XSC,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9024	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M82	EEE_YMS,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_SS_CAP
630-9133	PCBA,MLB,1.8GHZ,MI 2GB,SS CAP,M82	EEE_Z80,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9134	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M82	EEE_Z81,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_SS_CAP
630-9204	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M82	EEE_ZU5,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9205	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M82	EEE_ZU6,M82_COMMON,M82_HYNIX,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9206	PCBA,MLB,1.6GHZ,MI 2GB,MU CAP,M82	EEE_ZU7,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_MU_CAP
630-9207	PCBA,MLB,1.6GHZ,MI 2GB,TY CAP,M82	EEE_ZU8,M82_COMMON,M82_MICRON,CPU_PRQ_1_6GHZ,M82_TY_CAP
630-9208	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M82	EEE_ZU9,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9209	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M82	EEE_ZUA,M82_COMMON,M82_HYNIX,CPU_PRQ_1_8GHZ,M82_TY_CAP
630-9210	PCBA,MLB,1.8GHZ,MI 2GB,MU CAP,M82	EEE_ZUB,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_MU_CAP
630-9211	PCBA,MLB,1.8GHZ,MI 2GB,TY CAP,M82	EEE_ZUC,M82_COMMON,M82_MICRON,CPU_PRQ_1_8GHZ,M82_TY_CAP

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XSC]	CRITICAL	EEE_XSC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:YMS]	CRITICAL	EEE_YMS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z80]	CRITICAL	EEE_Z80
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:Z81]	CRITICAL	EEE_Z81
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU5]	CRITICAL	EEE_ZU5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU6]	CRITICAL	EEE_ZU6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU7]	CRITICAL	EEE_ZU7
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU8]	CRITICAL	EEE_ZU8
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZU9]	CRITICAL	EEE_ZU9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUA]	CRITICAL	EEE_ZUA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUB]	CRITICAL	EEE_ZUB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:ZUC]	CRITICAL	EEE_ZUC

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M82_COMMON	ALTERNATE,COMMON,M82_COMMON1,M82_COMMON2,M82_COMMON3
M82_COMMON1	ISL6258,BOOTROM_DEVEL,SMC_PRGRM
M82_COMMON2	SMS_MOT_DIS,LPCPLUS,XDP,DRAM_2GB
M82_COMMON3	
M82_MICRON	DRAM_MICRON,DRAM_SPD_1
M82_HYNIX	DRAM_HYNIX,DRAM_SPD_2
M82_HYNIX_LP	DRAM_HYNIX_LP,DRAM_SPD_2
M82_SS_CAP	SS_CAP_1UF,SS_CAP_2_2UF,SS_CAP_10UF
M82_MU_CAP	MU_CAP_1UF,MU_CAP_2_2UF,MU_CAP_10UF
M82_TY_CAP	TY_CAP_1UF,TY_CAP_2_2UF,TY_CAP_10UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3522	1	IC,SANTAYNEZ,MEROM,1.6GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_6GHZ
337S3523	1	IC,SANTAYNEZ,MEROM,1.8GHZ,ES,20W,956BGA	U1000	CRITICAL	CPU_1_8GHZ
338S0420	1	IC,965GM,CRESTLINE,USFF BGA	U1400	CRITICAL	
338S0421	1	IC,ICH8M,USFF BGA	U2300	CRITICAL	
359S0130	1	LOW POWER CLOCK SYNTHESIZER,SLG2AP101,68PIN	U2900	CRITICAL	
335S0510	1	IC, 16MBIT 8-PIN SERIAL FLASH,VWQPN	U6100	CRITICAL	BOOTROM_BLANK_2MB
335S0509	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2111	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M82	U6100	CRITICAL	BOOTROM_DEVEL
341S2112	1	IC,EFI,BOOTROM FINAL (LOCKED),M82	U6100	CRITICAL	BOOTROM_FINAL
337S3477	1	SST89V54RD MICROCONTROLLER	U9300	CRITICAL	SST8051_BLANK
341S2173	1	IC,PRGM,SST SST89V54RD,UCNTRLR,M82	U9300	CRITICAL	SST8051_PRGRM
338S0422	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2115	1	IC,PRGRM,SMC (NEW),M82	U4900	CRITICAL	SMC_PRGRM
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3140,U3150,U3160,U3170	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0406	4	MICRON,DRAM,64M16,8x12.5	U3240,U3250,U3260,U3270	CRITICAL	DRAM_MICRON
333S0411	4	HYNIX,DRAM,64M16,8x13	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0411	4	HYNIX,DRAM,64M16,8x13	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3140,U3150,U3160,U3170	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX_LP
333S0415	4	HYNIX,DRAM,64M16,8x13,LP	U3240,U3250,U3260,U3270	CRITICAL	DRAM_HYNIX_LP
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	ISL6258
197S0213	1	14.318MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_14MHZ
197S0231	1	20MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_20MHZ
197S0257	1	33MHZ XTAL, 2.5x2.0	Y9390	CRITICAL	SST8051_33MHZ
337S3563	1	IC,SANTAYNEZ,MEROM,1.6GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_6GHZ
337S3564	1	IC,SANTAYNEZ,MEROM,1.8GHZ,PRQ,REV3,20W,956BGA	U1000	CRITICAL	CPU_PRQ_1_8GHZ
338S0514	1	IC,965GM,CRESTLINE,PRQ,USFF BGA	U1400	CRITICAL	NB_PRQ
338S0515	1	IC,ICH8M,PRQ,USFF BGA	U2300	CRITICAL	SB_PRQ

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0044	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. B.0.0

SCALE NONE | SHT 4 OF 73

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	5	CAP, 1UF, 6.3V, 10%, 0402	C1001,C1002,C2102,C2151,C2170	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C2200,C2230,C2400,C2701,C2800,C2900,C7000,C7100,C7101	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	5	CAP, 1UF, 6.3V, 10%, 0402	C1001,C1002,C2151,C2151,C2170	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C2200,C2230,C2400,C2701,C2800,C2900,C7000,C7100,C7101	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	5	CAP, 1UF, 6.3V, 10%, 0402	C1001,C1002,C2102,C2151,C2170	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C2200,C2230,C2400,C2701,C2800,C2900,C7000,C7100,C7101	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	SS_CAP_2_2UF
138S0632	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8600,C8601,C8602,C8603,C8604,C8605,C8606,C8607,C8608,C8609	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8610,C8611,C8612,C8613,C8614,C8615,C8616,C8617,C8618,C8619	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620,C8621,C8622,C8623,C8624,C8625,C8626,C8627,C8628,C8629	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8630,C8631,C8632,C8633,C8634,C8635,C8636,C8637,C8638,C8639	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8600,C8601,C8602,C8603,C8604,C8605,C8606,C8607,C8608,C8609	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8998,C8901,C8902,C8903,C8904,C8905,C8906,C8907	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1301,C1302,C1305,C1306,C1307,C1308,C1201,C1202,C1203,C1204,C1205,C1206	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1022,C1023,C1099	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5255,C5259,C5140,C5141	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5148,C5150,C5151,C5254,C5255	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5255,C5259,C5140,C5141	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5148,C5150,C5151,C5254,C5255	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	MU_CAP_2_2UF
138S0633	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8600,C8601,C8602,C8603,C8604,C8605,C8606,C8607,C8608,C8609	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8610,C8611,C8612,C8613,C8614,C8615,C8616,C8617,C8618,C8619	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620,C8621,C8622,C8623,C8624,C8625,C8626,C8627,C8628,C8629	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8630,C8631,C8632,C8633,C8634,C8635,C8636,C8637,C8638,C8639	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8600,C8601,C8602,C8603,C8604,C8605,C8606,C8607,C8608,C8609	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8998,C8901,C8902,C8903,C8904,C8905,C8906,C8907	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1301,C1302,C1305,C1306,C1307,C1308,C1201,C1202,C1203,C1204,C1205,C1206	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1022,C1023,C1099	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5255,C5259,C5140,C5141	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5148,C5150,C5151,C5254,C5255	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5255,C5259,C5140,C5141	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5148,C5150,C5151,C5254,C5255	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1140,C1141,C1142,C1143,C1144,C1145,C1146,C1147,C1148,C1149	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	TY_CAP_2_2UF
138S0634	6	CAP, 2.2UF, 6.3V, 20%, 0402	C2214,C2215,C2240,C2241,C2242,C2243	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8600,C8601,C8602,C8603,C8604,C8605,C8606,C8607,C8608,C8609	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8610,C8611,C8612,C8613,C8614,C8615,C8616,C8617,C8618,C8619	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8620,C8621,C8622,C8623,C8624,C8625,C8626,C8627,C8628,C8629	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8630,C8631,C8632,C8633,C8634,C8635,C8636,C8637,C8638,C8639	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C8600,C8601,C8602,C8603,C8604,C8605,C8606,C8607,C8608,C8609	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C8998,C8901,C8902,C8903,C8904,C8905,C8906,C8907	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1301,C1302,C1305,C1306,C1307,C1308,C1201,C1202,C1203,C1204,C1205,C1206	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C1022,C1023,C1099	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5255,C5259,C5140,C5141	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5148,C5150,C5151,C5254,C5255	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5400,C5401,C5402,C5405,C5410,C5411,C5412,C5413,C5415,C5416	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C5220,C5221,C5222,C5225,C5230,C5231,C5255,C5259,C5140,C5141	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C5142,C5143,C5145,C5148,C5150,C5151,C5254,C5255	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1300	CRITICAL	SS_CAP_10UF
138S0626	9	CAP, 10UF, 6.3V, 20%, 0603	C2100,C2101,C2212,C2216,C2231,C2232,C2300,C2304,C2305	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C2701,C2706,C2708,C2720,C2901	CRITICAL	SS_CAP_10UF
138S0626	6	CAP, 10UF, 6.3V, 20%, 0603	C5400,C5401,C5402,C5600,C5601,C5602	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4100,C4400,C4613,C5000,C7201,C7301,C7350,C7351	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7600,C7641,C7803,C7804,C7900,C7909	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9204,C9205,C9213,C9240	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1300	CRITICAL	MU_CAP_10UF
138S0625	9	CAP, 10UF, 6.3V, 20%, 0603	C2100,C2101,C2212,C2216,C2231,C2232,C2300,C2304,C2305	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C2701,C2706,C2708,C2720,C2901	CRITICAL	MU_CAP_10UF
138S0625	6	CAP, 10UF, 6.3V, 20%, 0603	C5400,C5401,C5402,C5600,C5601,C5602	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4100,C4400,C4613,C5000,C7201,C7301,C7350,C7351	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7600,C7641,C7803,C7804,C7900,C7909	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9204,C9205,C9213,C9240	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307,C1308,C1309	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1300	CRITICAL	TY_CAP_10UF
138S0627	9	CAP, 10UF, 6.3V, 20%, 0603	C2100,C2101,C2212,C2216,C2231,C2232,C2300,C2304,C2305	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C2701,C2706,C2708,C2720,C2901	CRITICAL	TY_CAP_10UF
138S0627	6	CAP, 10UF, 6.3V, 20%, 0603	C5400,C5401,C5402,C5600,C5601,C5602	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4100,C4400,C4613,C5000,C7201,C7301,C7350,C7351	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C7502,C7507,C7600,C7641,C7803,C7804,C7900,C7909	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9204,C9205,C9213,C9240	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 5 OF 73	

ICT Test Points

These nets have a ICT_TEST property   This indicates a MUSTHAVE requirement for ICT

ICT_TEST

ICT_TEST	Net
TRUE	PP18V5_DCIN
TRUE	BATT_POS
TRUE	PP3V3_S5
TRUE	PP3V42_G3H
TRUE	GND
TRUE	PM_SLP_S3_L
TRUE	PM_S4_STATE_L
TRUE	PM_SLP_S5_L
TRUE	SMC_PM_G2_EN
TRUE	IMVP_VR_ON
TRUE	GFX_VR_EN
TRUE	SMC_BATT_CHG_EN
TRUE	SMC_ONOFF_L
TRUE	ALL_SYS_PWRGD_AND
TRUE	PPVBAT_G3H_CHGR_REG
TRUE	CPU_PWRGD
TRUE	PM_RSMRST_L
TRUE	PM_PWRBTN_L
TRUE	TP_PCI_RST_L
TRUE	PLT_RST_L
TRUE	SMC_RESET_L
TRUE	PM_SYSRST_L
TRUE	PP1V5_S0
TRUE	PP1V05_S0
TRUE	PP1V8_S0
TRUE	PP1V8_S3
TRUE	PP0V9_S0
TRUE	PP0V9_S3
TRUE	PP1V25_S0
TRUE	PP5V_S5
TRUE	PP5V_S3
TRUE	PP5V_S0
TRUE	PP3V3_S3
TRUE	PP3V3_A_S0
TRUE	PP3V3_B_S0
TRUE	PPVCORE_S0_CPU
TRUE	PPVCORE_S0_NB_GFX
TRUE	XDP_TCK
TRUE	XDP_TDI
TRUE	XDP_TDO
TRUE	XDP_TMS
TRUE	XDP_TRST_L
TRUE	XDP_CPURST_L
TRUE	XDP_BPM_L<4>
TRUE	XDP_BPM_L<5>
TRUE	XDP_DBRESET_L
TRUE	XDP_PWRGD
TRUE	SPI_A_SCLK_R
TRUE	SMC_MANUAL_RST_L
TRUE	SMC_TCK
TRUE	SMC_TDI
TRUE	SMC_TDO
TRUE	SMC_TMS
TRUE	SMC_TRST_L
TRUE	CPU_A20M_L
TRUE	CPU_DPRSTP_L
TRUE	CPU_DPSLP_L
TRUE	CPU_FERR_L
TRUE	NB_BSEL<0>
TRUE	NB_BSEL<1>
TRUE	NB_BSEL<2>
TRUE	NB_CFG<16>
TRUE	NB_CFG<19>
TRUE	NB_CFG<20>

ICT_TEST	Net
TRUE	NB_CFG<3>
TRUE	NB_CFG<4>
TRUE	NB_CFG<5>
TRUE	NB_CFG<6>
TRUE	NB_CFG<7>
TRUE	NB_CFG<8>
TRUE	NB_CFG<9>
TRUE	NB_RESET_L
TRUE	NB_SB_SYNC_L
TRUE	NB_TEST1
TRUE	NB_TEST2
TRUE	1V05S0_RUNSS
TRUE	1V05S0_TRIP
TRUE	1V25S0_RUNSS
TRUE	1V51V05S0_V5FILT
TRUE	1V5S0_RUNSS
TRUE	1V5S0_TRIP
TRUE	1V8S3_CS
TRUE	1V8S3_V5FILT
TRUE	1V8S3_VDDQSET
TRUE	3V3S5_CS
TRUE	5V3V3S5_TONSEL
TRUE	5V3V3S5_V5FILT
TRUE	5V3V3S5_VREF
TRUE	5V3V3S5_VREG3
TRUE	5VS5_CS
TRUE	5VS5_VREG
TRUE	ADAPTER_SENSE
TRUE	AIRPORT_RST_L
TRUE	ALL_SYSPWRGD_DLY
TRUE	ALL_SYS_PWRGD
TRUE	ALL_SYS_PWRGD_AND
TRUE	ARB_DETECT_L
TRUE	AUD_MIC_CLK
TRUE	AUD_MIC_CLK_F
TRUE	AUD_MIC_DATA
TRUE	AUD_MIC_DATA_F
TRUE	BATT_POS
TRUE	BATT_POS_F
TRUE	BOOTROM_OVR_EN_L
TRUE	CHGR_AGATE
TRUE	CHGR_AMON
TRUE	CHGR_BGATE
TRUE	CHGR_BMON
TRUE	CHGR_BOOT
TRUE	CHGR_CSIN
TRUE	CHGR_CSIP
TRUE	CHGR_CSON
TRUE	CHGR_CSOP
TRUE	CHGR_DCIN
TRUE	CHGR_LOWCURRENT_GATE
TRUE	CHGR_LOWCURRENT_REF
TRUE	CHGR_SGATE
TRUE	CHGR_SGATE_DIV
TRUE	CHGR_VCOMP_R
TRUE	CHGR_VDD
TRUE	CHGR_VDDP
TRUE	CHGR_VNEG
TRUE	CHGR_VNEG_R
TRUE	CK505_CLK14P3M_TIMER
TRUE	CK505_FSA
TRUE	CK505_FSB_TEST_MODE
TRUE	CK505_FSC
TRUE	CK505_PCI3_CLK

ICT_TEST	Net
TRUE	CK505_PCI5_FCTSEL1
TRUE	CK505_PCIF0_CLK
TRUE	CK505_PCIF1_CLK
TRUE	CK505_SRC_CLKREQ6_L
TRUE	CK505_USB48_FSA
TRUE	CK505_XTAL_OUT
TRUE	CLINK_NB_CLK
TRUE	CLINK_NB_DATA
TRUE	CLINK_NB_RESET_L
TRUE	CLK_PWRGD
TRUE	CPU_A20M_L
TRUE	CPU_BSEL<0>
TRUE	CPU_BSEL<1>
TRUE	CPU_BSEL<2>
TRUE	CPU_COMP<0>
TRUE	CPU_COMP<1>
TRUE	CPU_COMP<2>
TRUE	CPU_COMP<3>
TRUE	CPU_DPRSTP_L
TRUE	CPU_DPSLP_L
TRUE	CPU_FERR_L
TRUE	CPU_GTLREF
TRUE	CPU_IERR_L
TRUE	CPU_IGNNE_L
TRUE	CPU_INIT_L
TRUE	CPU_INTR
TRUE	CPU_NMI
TRUE	CPU_PROCHOT_BUF
TRUE	CPU_PROCHOT_L
TRUE	CPU_PROCHOT_L_R
TRUE	CPU_PWRGD
TRUE	CPU_SMI_L
TRUE	CPU_STPCLK_L
TRUE	CPU_THERMD_N
TRUE	CPU_THERMD_P
TRUE	CPU_THERMTRIP_R
TRUE	CPU_VCCSENSE_N
TRUE	CPU_VCCSENSE_P
TRUE	CPU_VID<6..0>
TRUE	CRT_BLUE
TRUE	CRT_GREEN
TRUE	CRT_HSYNC_LS
TRUE	CRT_HSYNC_LS_R
TRUE	CRT_HSYNC_R
TRUE	CRT_RED
TRUE	CRT_TVO_IREF
TRUE	CRT_VSYNC_LS
TRUE	CRT_VSYNC_LS_R
TRUE	CRT_VSYNC_R
TRUE	DEBUG_RESET_L
TRUE	DLY_OFF_A
TRUE	DLY_OFF_B
TRUE	DLY_OFF_C
TRUE	DLY_OFF_D
TRUE	DMI_IRCOMP_R
TRUE	DMI_N2S_N<3..0>
TRUE	DMI_N2S_P<3..0>
TRUE	DMI_S2N_N<3..0>
TRUE	DMI_S2N_P<3..0>
TRUE	DVI_HOST
TRUE	DVI_HOTPLUG_DET
TRUE	DVI_HOTPLUG_DET_BUF
TRUE	DVI_HOTPLUG_DET_DEL_L
TRUE	DVI_HOTPLUG_DET_INT_L

ICT_TEST	Net
TRUE	DVI_HPDET_RC
TRUE	EXCARD_OC_L
TRUE	EXTAUSB_OC_F_L
TRUE	EXTAUSB_OC_L
TRUE	EXTBUSB_OC_L
TRUE	EXTGPU_LVDS_EN
TRUE	EXT_COMPVID_B
TRUE	EXT_C_R
TRUE	EXT_Y_G
TRUE	FAN_RT_PWM
TRUE	FAN_RT_TACH
TRUE	FRANKCARD_GPIO
TRUE	FSB_CLK_CPU_N
TRUE	FSB_CLK_CPU_P
TRUE	FSB_CLK_NB_N
TRUE	FSB_CLK_NB_P
TRUE	FSB_CPURST_L
TRUE	FWH_MFG_MODE
TRUE	GCORE_BST_D
TRUE	GCORE_COMP_R
TRUE	GCORE_CSFB
TRUE	GCORE_FBRTN
TRUE	GCORE_LLINE
TRUE	GCORE_PMON
TRUE	GCORE_PMONFS
TRUE	GCORE_PWRGD
TRUE	GCORE_RAMP
TRUE	GCORE_RPM
TRUE	GCORE_RT
TRUE	GCORE_ST
TRUE	GCORE_SW
TRUE	GCORE_SW_R
TRUE	GCORE_VARFREQ
TRUE	GCORE_VCC
TRUE	GCORE_VDC_DIV
TRUE	GCORE_VRPM
TRUE	GFX_VID<3..0>
TRUE	GFX_VR_EN
TRUE	GLAN_COMP
TRUE	GND_1V51V05S0_SGND
TRUE	GND_1V8S3_CSGND
TRUE	GND_1V8S3_SGND
TRUE	GND_5V3V3S5_SGND
TRUE	GND_ALS_F
TRUE	GND_CHGR_SGND
TRUE	GND_GCORE_PGND
TRUE	GND_IMVP6_SGND
TRUE	GND_LCDBKLT_GNDA
TRUE	GND_P1V2S3_SGND
TRUE	GND_SMC_AVSS
TRUE	HDA_BIT_CLK
TRUE	HDA_BIT_CLK_R
TRUE	HDA_DOCK_EN_L
TRUE	HDA_RST_L
TRUE	HDA_RST_L_R
TRUE	HDA_SDIN0
TRUE	HDA_SDIN1
TRUE	HDA_SDOUT
TRUE	HDA_SDOUT_R
TRUE	HDA_SYNC
TRUE	HDA_SYNC_R
TRUE	HDMI_HOST
TRUE	I2C_TOP_ALS_SCL_F
TRUE	I2C_TOP_ALS_SDA_F

ICT_TEST	Net
TRUE	IDE_IRQ14
TRUE	IDE_PDA<2..0>
TRUE	IDE_PDCS1_L
TRUE	IDE_PDCS3_L
TRUE	IDE_PDD<15..0>
TRUE	IDE_PDDACK_L
TRUE	IDE_PDDREQ
TRUE	IDE_PDIORDY
TRUE	IDE_PDIOR_L
TRUE	IDE_PDIOW_L
TRUE	IDE_RESET_BUF_L
TRUE	IDE_RESET_L
TRUE	IMVP6_BOOT
TRUE	IMVP6_BOOT_RC
TRUE	IMVP6_COMP_R
TRUE	IMVP6_DROOP
TRUE	IMVP6_PHASE
TRUE	IMVP6_PVCC
TRUE	IMVP6_RBIAS
TRUE	IMVP6_SOFT
TRUE	IMVP6_VDIFF
TRUE	IMVP6_VDIFF_RC
TRUE	IMVP6_VO_R
TRUE	IMVP6_VR_TT
TRUE	IMVP6_VSEN_N
TRUE	IMVP6_VSEN_P
TRUE	IMVP6_VSUM
TRUE	IMVP6_VW
TRUE	IMVP_DPRSLPVR
TRUE	IMVP_VR_ON
TRUE	INT_PIRQA_L
TRUE	INT_PIRQB_L
TRUE	INT_PIRQC_L
TRUE	INT_PIRQD_L
TRUE	INT_PIRQE_L
TRUE	INT_PIRQF_L
TRUE	INT_SERIRQ
TRUE	LAN_ENERGY_DET
TRUE	LAN_PHYPC
TRUE	LCDBKLT_ENA
TRUE	LCDBKLT_ISET
TRUE	LCDBKLT_OVP
TRUE	LCDBKLT_PWM_UNBUF
TRUE	LCDBKLT_PWREN
TRUE	LCDBKLT_RT
TRUE	LCDBKLT_RTN<6..1>
TRUE	LCDBKLT_RTN_RC<6..1>
TRUE	LCDBKLT_SSTCMP
TRUE	LCDBKLT_SSTCMP_RC
TRUE	LCDBKLT_VREF
TRUE	LCDVDD_PWREN_L
TRUE	LCDVDD_PWREN_L_R
TRUE	LOCAL_CTRL_CLK
TRUE	LOCAL_CTRL_DATA
TRUE	LPC_AD<3..0>
TRUE	LPC_FRAME_L
TRUE	LSOC_H
TRUE	LSOC_H_R
TRUE	LVDS_A_CLK_F_N
TRUE	LVDS_A_CLK_F_P
TRUE	LVDS_A_CLK_N
TRUE	LVDS_A_CLK_P
TRUE	LVDS_A_DATA_F_N<2..0>
TRUE	LVDS_A_DATA_F_P<2..0>

ICT_TEST	Net
TRUE	LVDS_A_DATA_N<2>
TRUE	LVDS_A_DATA_P<2>
TRUE	LVDS_DDC_CLK
TRUE	LVDS_DDC_DATA
TRUE	LVDS_IBG
TRUE	LVDS_VDD_EN
TRUE	MEM_ODT<3..0>
TRUE	MEM_RCOMP
TRUE	MEM_RCOMP_L
TRUE	MEM_RCOMP_VOH
TRUE	MEM_RCOMP_VOL
TRUE	NB_BSEL<0>
TRUE	NB_BSEL<1>
TRUE	NB_BSEL<2>
TRUE	NB_CFG<16>
TRUE	NB_CFG<19>
TRUE	NB_CFG<20>
TRUE	NB_CFG<3>
TRUE	NB_CFG<4>
TRUE	NB_CFG<5>
TRUE	NB_CFG<6>
TRUE	NB_CFG<7>
TRUE	NB_CFG<8>
TRUE	NB_CFG<9>
TRUE	NB_CLINK_VREF
TRUE	NB_CLK100M_DPLLSS_N
TRUE	NB_CLK100M_DPLLSS_P
TRUE	NB_CLK100M_PCIE_N
TRUE	NB_CLK100M_PCIE_P
TRUE	NB_CLK96M_DOT_N
TRUE	NB_CLK96M_DOT_P
TRUE	NB_CLKREQ_L
TRUE	NB_FSB_RCOMP
TRUE	NB_FSB_SCOMP
TRUE	NB_FSB_SCOMP_L
TRUE	NB_FSB_SWING
TRUE	NB_FSB_VREF
TRUE	NB_RESET_L
TRUE	NB_SB_SYNC_L
TRUE	NB_TEST1
TRUE	NB_TEST2
TRUE	NB_VCCSM_LF1
TRUE	NB_VCCSM_LF2
TRUE	NB_VCCSM_LF3
TRUE	NB_VCCSM_LF4
TRUE	NB_VCCSM_LF5
TRUE	NB_VCCSM_LF6
TRUE	NB_VCCSM_LF7
TRUE	NB_VTTLF_CAP1
TRUE	NB_VTTLF_CAP2
TRUE	NB_VTTLF_CAP3
TRUE	ODD_PWR_EN_L
TRUE	ONEWIRE_DCIN_DIV
TRUE	ONEWIRE_EN
TRUE	ONEWIRE_ESD
TRUE	ONEWIRE_OV
TRUE	ONEWIRE_PWR_EN_L
TRUE	ONEWIRE_PWR_EN_L_DIV
TRUE	P1V25S0NBDPLL_FB
TRUE	P1V25S0NBDPLL_RF
TRUE	P1V25S0_ITH
TRUE	P1V25S0_ITH_RC
TRUE	P1V25S0_MODE
TRUE	P1V25S0_RT

ICT_TEST	Net
TRUE	P1V8S0_EN
TRUE	P3V3S0_EN
TRUE	P3V3S3_EN_L
TRUE	P3V3TVDAC_EN_RC
TRUE	P3V3TVDAC_NOISE
TRUE	P3V42G3H5_BOOST
TRUE	P3V42G3H_SHDN_L
TRUE	P3V42G3H_SHDN_L1
TRUE	P5VS0_EN
TRUE	P5VS3_EN_L
TRUE	PBUS_ISENSE_IN_NEG
TRUE	PBUS_ISENSE_VREG
TRUE	PBUS_S0_SMC_VSENSE
TRUE	PBUS_SMC_VSENSE_EN_L
TRUE	PCIE_CLK100M_MINI_N
TRUE	PCIE_CLK100M_MINI_P
TRUE	PCIE_CLK100M_MINI_N_F
TRUE	PCIE_CLK100M_MINI_P_F
TRUE	PCIE_E_D2R_N
TRUE	PCIE_E_D2R_N_F
TRUE	PCIE_E_D2R_P
TRUE	PCIE_E_D2R_P_F
TRUE	PCIE_E_R2D_C_N
TRUE	PCIE_E_R2D_C_N_F
TRUE	PCIE_E_R2D_C_P
TRUE	PCIE_E_R2D_C_P_F
TRUE	PCIE_E_R2D_N
TRUE	PCIE_E_R2D_P
TRUE	PCIE_WAKE_L
TRUE	PCI_CLK33M_LPCPLUS
TRUE	PCI_CLK33M_SB
TRUE	PCI_CLK33M_SMC
TRUE	PCI_DEVSEL_L
TRUE	PCI_FRAME_L
TRUE	PCI_FW_GNT_L
TRUE	PCI_FW_REQ_L
TRUE	PCI_IRDY_L
TRUE	PCI_LOCK_L
TRUE	PCI_PERR_L
TRUE	PCI_PME_FW_L
TRUE	PCI_REQ1_L
TRUE	PCI_REQ2_L
TRUE	PCI_SERR_L
TRUE	PCI_STOP_L
TRUE	PCI_TRDY_L
TRUE	PEG_COMP
TRUE	PEG_D2R_N<1>
TRUE	PEG_D2R_P<1>
TRUE	PEG_R2D_C_N<3..0>
TRUE	PEG_R2D_C_P<3..0>
TRUE	PGOOD_1V25S0
TRUE	PGOOD_1V8S3
TRUE	PLT_RST_BUF_L
TRUE	PLT_RST_L
TRUE	PM_BATLOW_L
TRUE	PM_BMBUSY_L
TRUE	PM_CLKRUN_L
TRUE	PM_DPRSLPVR
TRUE	PM_EXTTS_L<0>
TRUE	PM_EXTTS_L<1>
TRUE	PM_LAN_ENABLE
TRUE	PM_LAN_PWRGD
TRUE	PM_LATRIGGER_L
TRUE	PM_PWRBTN_L
TRUE	PM_RI_L
TRUE	PM_RSMRST_L
TRUE	PM_S4_STATE_L
TRUE	PM_SB_PWROK
TRUE	PM_SLP_S3_L
TRUE	PM_SLP_S4_LS5V
TRUE	PM_SLP_S5_L
TRUE	PM_STPCPU_L
TRUE	PM_STPPCI_L
TRUE	PM_SUS_STAT_L
TRUE	PM_SYSRST_L
TRUE	PM_THRMTRIP_L
TRUE	PM_THRM_L
TRUE	PM_WLAN_EN_L
TRUE	PM_WLAN_EN_L1
TRUE	PM_WLAN_EN_L2
TRUE	PM_WLAN_EN_L_SS
TRUE	PP0V9_S0
TRUE	PP0V9_S3
TRUE	PP18V5_DCIN

ICT_TEST	Net
TRUE	PP18V5_DCIN_ONEWIRE
TRUE	PP18V5_G3H
TRUE	PP18V5_S5_CHGR_SW_R
TRUE	PP1V05_S0
TRUE	PP1V05_S0_NB_VCCPEG
TRUE	PP1V25_S0
TRUE	PP1V25_S0M_NB_VCCA_HPLL
TRUE	PP1V25_S0_NB_DPLL
TRUE	PP1V25_S0_NB_PEGPLL
TRUE	PP1V25_S0_NB_PEGPLL_RC
TRUE	PP1V25_S0_NB_VCCA_DPLLA
TRUE	PP1V25_S0_NB_VCCA_DPLLB
TRUE	PP1V5_S0
TRUE	PP1V5_S0_NB_QDAC
TRUE	PP1V5_S0_NB_VCCD_CRT
TRUE	PP1V5_S0_NB_VCCD_QDAC
TRUE	PP1V5_S0_SB_VCC1_5_B
TRUE	PP1V5_S0_SB_VCCDMIPLL
TRUE	PP1V5_S0_SB_VCCDMIPLL_F
TRUE	PP1V5_S0_SB_VCCSATAPLL
TRUE	PP1V8_S0
TRUE	PP1V8_S0_ANALOG_SDVO_F
TRUE	PP1V8_S0_ANALOG_TMDS_F
TRUE	PP1V8_S0_NB_VCCTXLVDS
TRUE	PP1V8_S0_PVCC1_TMDS_F
TRUE	PP1V8_S0_PVCC2_TMDS_F
TRUE	PP1V8_S0_TMDS_F
TRUE	PP1V8_S3
TRUE	PP1V8_S3M_NB_VCCSMCK
TRUE	PP1V8_S3_NB_VCCSMCK_RC
TRUE	PP3V3_A_S0
TRUE	PP3V3_B_S0
TRUE	PP3V3_LCDVDD_SW
TRUE	PP3V3_LCDVDD_SW_F
TRUE	PP3V3_S0_ANALOG_SDVO_F
TRUE	PP3V3_S0_CK505_VDD48
TRUE	PP3V3_S0_CK505_VDDA
TRUE	PP3V3_S0_CK505_VDDA_R
TRUE	PP3V3_S0_CK505_VDD_CPU_SRC
TRUE	PP3V3_S0_CK505_VDD_PCI
TRUE	PP3V3_S0_CK505_VDD_REF
TRUE	PP3V3_S0_HDCP_F
TRUE	PP3V3_S0_IMVP6_3V3
TRUE	PP3V3_S0_LCD_F
TRUE	PP3V3_S0_NBCORE_FOLLOW_R
TRUE	PP3V3_S0_NB_CRTDAC_F
TRUE	PP3V3_S0_NB_TVDAC
TRUE	PP3V3_S0_NB_TVDAC_F
TRUE	PP3V3_S0_NB_TVDAC_FOLLOW
TRUE	PP3V3_S0_NB_VCCA_CRTDAC
TRUE	PP3V3_S0_NB_VCCA_DAC_BG
TRUE	PP3V3_S0_NB_VCCA_TVDACA
TRUE	PP3V3_S0_NB_VCCA_TVDACB
TRUE	PP3V3_S0_NB_VCCA_TVDACC
TRUE	PP3V3_S0_SPVCC_TMDS_F
TRUE	PP3V3_S3
TRUE	PP3V3_S3_ALS_F
TRUE	PP3V3_S3_AP_AUX
TRUE	PP3V3_S5_AVREF_SMC
TRUE	PP3V3_S5_SMC_AVCC
TRUE	PP3V42G3H_SW
TRUE	PP3V42_G3H
TRUE	PP3V42_G3H_IPD_F
TRUE	PP3V42_G3H_SMCUSBMUX_R
TRUE	PP5V_S0
TRUE	PP5V_S0_DVIPORT
TRUE	PP5V_S0_DVIPORT_D
TRUE	PP5V_S0_IMVP6_VDD
TRUE	PP5V_S0_KBDLED_F
TRUE	PP5V_S0_SB_V5REF
TRUE	PP5V_S0_TMDS_FUSE
TRUE	PP5V_S3
TRUE	PP5V_S3_CAMERA_F
TRUE	PP5V_S3_TOPCASE_F
TRUE	PP5V_S3_USB2_EXTA
TRUE	PP5V_S3_USB2_EXTA_F
TRUE	PP5V_S5
TRUE	PP5V_S5_SB_V5REF_SUS
TRUE	PPBUS_G3H
TRUE	PPBUS_R_G3H
TRUE	PPDCIN_G3H
TRUE	PPDCIN_G3H_R
TRUE	PPVBATT_G3H_R

ICT_TEST	Net
TRUE	PPVBAT_G3H_CHGR_OUT
TRUE	PPVBAT_G3H_CHGR_REG
TRUE	PPVBAT_G3H_CHRGR_REG_0
TRUE	PPVBAT_G3H_CHRGR_REG_R
TRUE	PPVCORE_S0_CPU
TRUE	PPVCORE_S0_NB_GFX
TRUE	PPVDCIN_G3H_PRE
TRUE	PPVDCIN_G3H_PRE2
TRUE	PPVDCIN_G3H_PRE_0
TRUE	PPVDCIN_G3H_PRE_R
TRUE	PPVIN_S5_IMVP6_VIN
TRUE	PPVOUT_S0_LCDBKLT
TRUE	PPVOUT_S0_LCDBKLT_SW
TRUE	RSMRST_PWRGD
TRUE	RSVD_EXTGPU_LVDS_EN
TRUE	RUNSS_GATE_D
TRUE	RUNSS_GATE_D_L
TRUE	S0PWRGD_1V8_DIV
TRUE	S0PWRGD_3V3_DIV
TRUE	S0PWRGD_5V_DIV
TRUE	S0SEQ_BEGIN
TRUE	SATA_B_DET_L
TRUE	SB_A20GATE
TRUE	SB_CLINK_VREF0
TRUE	SB_CLINK_VREF1
TRUE	SB_CLK100M_DMI_N
TRUE	SB_CLK100M_DMI_P
TRUE	SB_CLK14P3M_TIMER
TRUE	SB_CLK48M_USBCTLR
TRUE	SB_CRT_TVOUT_MUX_L
TRUE	SB_GPIO10_CL1
TRUE	SB_GPIO18
TRUE	SB_GPIO30
TRUE	SB_GPIO36
TRUE	SB_GPIO40

ICT_TEST	Net
TRUE	SB_INTVRMEN
TRUE	SB_LAN100_SLP
TRUE	SB_RCIN_L
TRUE	SB_RTC_RST_L
TRUE	SB_RTC_X1
TRUE	SB_RTC_X1_R
TRUE	SB_RTC_X2
TRUE	SB_SLOAD
TRUE	SB_SM_INTRUDER_L
TRUE	SB_SPKR
TRUE	SDVO_CTRLCLK
TRUE	SDVO_CTRLDATA
TRUE	SMBUS_SB_ME_SCL
TRUE	SMBUS_SB_ME_SDA
TRUE	SMBUS_SB_SCL
TRUE	SMBUS_SB_SDA
TRUE	SMBUS_SMC_0_S0_SCL
TRUE	SMBUS_SMC_0_S0_SDA
TRUE	SMBUS_SMC_A_S3_SCL
TRUE	SMBUS_SMC_A_S3_SDA
TRUE	SMBUS_SMC_BSA_SCL
TRUE	SMBUS_SMC_BSA_SDA
TRUE	SMBUS_SMC_B_S3_SCL
TRUE	SMBUS_SMC_B_S3_SDA
TRUE	SMBUS_SMC_MGMT_SCL
TRUE	SMBUS_SMC_MGMT_SDA
TRUE	SMB_AIRPORT_CONN_CLK
TRUE	SMB_AIRPORT_CONN_DATA
TRUE	SMC_ACIN_VSENSE
TRUE	SMC_ADAPTER_EN
TRUE	SMC_BATTPACK_STAT
TRUE	SMC_BATT_CHG_EN
TRUE	SMC_BATT_ISENSE
TRUE	SMC_BC_ACOK
TRUE	SMC_BC_ACOK_ONEWIRE_R

ICT_TEST	Net
TRUE	SMC_BS_ALRT_L
TRUE	SMC_CASE_OPEN
TRUE	SMC_DCIN_ISENSE
TRUE	SMC_EXTAL
TRUE	SMC_FAN_0_CTL
TRUE	SMC_FAN_0_TACH
TRUE	SMC_GPU_ISENSE
TRUE	SMC_GPU_VSENSE
TRUE	SMC_KBC_MDE
TRUE	SMC_LID
TRUE	SMC_LRESET_L
TRUE	SMC_MANUAL_RST_L
TRUE	SMC_MANUAL_RST_L1
TRUE	SMC_MD1
TRUE	SMC_NMI
TRUE	SMC_ODD_DETECT
TRUE	SMC_ONOFF_H
TRUE	SMC_ONOFF_L
TRUE	SMC_PBUS_ISENSE
TRUE	SMC_PBUS_VSENSE
TRUE	SMC_PF3
TRUE	SMC_PM_G2_EN
TRUE	SMC_PROCHOT
TRUE	SMC_PROCHOT_3_3_L
TRUE	SMC_RESET_L
TRUE	SMC_RUNTIME_SCI_L
TRUE	SMC_RX_L
TRUE	SMC_SMS_INT
TRUE	SMC_SUS_CLK
TRUE	SMC_SYS_KBDLED
TRUE	SMC_SYS_LED
TRUE	SMC_TCK
TRUE	SMC_TDI
TRUE	SMC_TDO
TRUE	SMC_THRMTRIP

ICT_TEST	Net
TRUE	SMC_TMS
TRUE	SMC_TRST_L
TRUE	SMC_TX_L
TRUE	SMC_VCL
TRUE	SMC_WAKE_SCI_L
TRUE	SMC_XTAL
TRUE	SMS_MOT_EN
TRUE	SMS_ONOFF_L
TRUE	SMS_X_AXIS
TRUE	SMS_Y_AXIS
TRUE	SMS_Z_AXIS
TRUE	SPI_A_INT_CLK
TRUE	SPI_A_INT_HOLD_L
TRUE	SPI_A_INT_SI
TRUE	SPI_A_INT_WP_L
TRUE	SPI_A_SCLK_R
TRUE	SPI_A_SI_R
TRUE	SPI_A_SO_R
TRUE	SPI_CE_L<0>
TRUE	SPI_CE_R_L<0>
TRUE	SPI_CE_R_L<1>
TRUE	SPI_EXT_A_SCLK_R
TRUE	SPI_EXT_A_SI_R
TRUE	SPI_EXT_CE_L<0>
TRUE	SPI_INT_CE_L<0>
TRUE	SPI_SCLK_R
TRUE	SPI_SI_R
TRUE	SPI_SO
TRUE	SST8051_DDC_CLK
TRUE	SST8051_DDC_DATA
TRUE	SST8051_DDC_EN
TRUE	SST8051_DVI_HOTPLUG_DET
TRUE	SST8051_EA_L
TRUE	SST8051_P25_AUDIO_CONFIG
TRUE	SST8051_P34_AUDIO_CONFIG

ICT_TEST	Net
TRUE	SST8051_RST
TRUE	SST8051_SW_RESET_L
TRUE	SST8051_UPDATE_L
TRUE	SST8051_XTAL1
TRUE	SST8051_XTAL2
TRUE	SUS_CLK_SB
TRUE	SYS_ONEWIRE
TRUE	SYS_ONEWIRE_BILAT
TRUE	THRM_CPU_ALERT_L
TRUE	THRM_CPU_DXN
TRUE	THRM_CPU_DXP
TRUE	THRM_CPU_THM_L
TRUE	TMDS_DDC_SCL
TRUE	TMDS_DDC_SDA
TRUE	TMDS_EXT_RES
TRUE	TMDS_EXT_SWING
TRUE	TMDS_HTPLG
TRUE	TMDS_HTPLG_R
TRUE	TMDS_HW_RESET_L
TRUE	TMDS_INT_N
TRUE	TMDS_INT_P
TRUE	TMDS_LINT_L
TRUE	TMDS_LSCL
TRUE	TMDS_LSDA
TRUE	TMDS_SDB_N
TRUE	TMDS_SDB_P
TRUE	TMDS_SDC_N
TRUE	TMDS_SDC_P
TRUE	TMDS_SDG_N
TRUE	TMDS_SDG_P
TRUE	TMDS_SDR_N
TRUE	TMDS_SDR_P
TRUE	TMDS_SW_RESET_L
TRUE	TMDS_TX<2..0>
TRUE	TMDS_TX_CLK

ICT_TEST	Net
TRUE	TMDS_TX_CLK_N
TRUE	TMDS_TX_CLK_P
TRUE	TMDS_TX_CONN_CLK_N
TRUE	TMDS_TX_CONN_CLK_P
TRUE	TMDS_TX_CONN_N<2..0>
TRUE	TMDS_TX_CONN_P<2..0>
TRUE	TMDS_TX_N<2..0>
TRUE	TMDS_TX_P<2..0>
TRUE	TV_A_DAC
TRUE	TV_B_DAC
TRUE	TV_C_DAC
TRUE	TV_DCONSEL<1>
TRUE	USB2_AIRPORT_N
TRUE	USB2_AIRPORT_N_F
TRUE	USB2_AIRPORT_P
TRUE	USB2_AIRPORT_P_F
TRUE	USB2_CAMERA_F_N
TRUE	USB2_CAMERA_F_P
TRUE	USB2_CAMERA_N
TRUE	USB2_CAMERA_P
TRUE	USB2_EXTA_F_N
TRUE	USB2_EXTA_F_P
TRUE	USB2_EXTA_N
TRUE	USB2_EXTA_P
TRUE	USB2_MUXED_EXTA_N
TRUE	USB2_MUXED_EXTA_P
TRUE	USB2_WSPRING_N
TRUE	USB2_WSPRING_P
TRUE	USB_DEBUGPRT_EN_L
TRUE	USB_EXTC_OC_L
TRUE	USB_EXTD_OC_L
TRUE	USB_IR_N
TRUE	USB_IR_P
TRUE	USB_RBIAS
TRUE	VCCCL1_5V

ICT_TEST	Net
TRUE	VGA_B
TRUE	VGA_G
TRUE	VGA_HSYNC
TRUE	VGA_R
TRUE	VGA_VSYNC
TRUE	VR_PWRGD_CK505
TRUE	VR_PWRGD_CK505_L
TRUE	VR_PWRGOOD_DELAY
TRUE	WOL_EN
TRUE	WOW_EN
TRUE	XDP_BPM_L<0>
TRUE	XDP_BPM_L<1>
TRUE	XDP_BPM_L<2>
TRUE	XDP_BPM_L<3>
TRUE	XDP_BPM_L<4>
TRUE	XDP_BPM_L<5>
TRUE	XDP_CLK_N
TRUE	XDP_CLK_P
TRUE	XDP_CPURST_L
TRUE	XDP_DBRESET_L
TRUE	XDP_OBS20
TRUE	XDP_PWRGD
TRUE	XDP_TCK
TRUE	XDP_TDI
TRUE	XDP_TDO
TRUE	XDP_TMS
TRUE	XDP_TRST_L

ICT Test Points

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	8.0.0
SCALE NONE	SHT 6	OF 73

Functional Test Points

NB NO_TESTS

These are normally testpoints but become NC

NO_TEST

TP30	TRUE	NC_LVDS_VBG	NC_LVDS_VBG	MAKE_BASE=TRUE	7 15
TP26	TRUE	NC_NB_RSVD_31	NC_NB_RSVD_31	MAKE_BASE=TRUE	7 16
TP25	TRUE	NC_NB_RSVD_32	NC_NB_RSVD_32	MAKE_BASE=TRUE	7
TP27	TRUE	NC_NB_RSVD_33	NC_NB_RSVD_33	MAKE_BASE=TRUE	7
TP29	TRUE	NC_MEM_A_RCVEN_L	NC_MEM_A_RCVEN_L	MAKE_BASE=TRUE	7 17
TP28	TRUE	NC_MEM_B_RCVEN_L	NC_MEM_B_RCVEN_L	MAKE_BASE=TRUE	7 17
TP23	TRUE	NC_NB_RSVD_1	NC_NB_RSVD_1	MAKE_BASE=TRUE	7 16
TP38	TRUE	NC_NB_RSVD_2	NC_NB_RSVD_2	MAKE_BASE=TRUE	7 16
TP37	TRUE	NC_NB_RSVD_3	NC_NB_RSVD_3	MAKE_BASE=TRUE	7 16
TP32	TRUE	NC_NB_RSVD_4	NC_NB_RSVD_4	MAKE_BASE=TRUE	7 16
TP47	TRUE	NC_NB_RSVD_5	NC_NB_RSVD_5	MAKE_BASE=TRUE	7 16
TP40	TRUE	NC_NB_RSVD_6	NC_NB_RSVD_6	MAKE_BASE=TRUE	7 16
TP42	TRUE	NC_NB_RSVD_7	NC_NB_RSVD_7	MAKE_BASE=TRUE	7 16
TP36	TRUE	NC_NB_RSVD_8	NC_NB_RSVD_8	MAKE_BASE=TRUE	7 16
TP24	TRUE	NC_NB_RSVD_14	NC_NB_RSVD_14	MAKE_BASE=TRUE	7 16
TP46	TRUE	NC_NB_RSVD_21	NC_NB_RSVD_21	MAKE_BASE=TRUE	7 16
TP35	TRUE	NC_NB_RSVD_22	NC_NB_RSVD_22	MAKE_BASE=TRUE	7 16
TP39	TRUE	NC_NB_RSVD_23	NC_NB_RSVD_23	MAKE_BASE=TRUE	7 16
TP45	TRUE	NC_NB_RSVD_24	NC_NB_RSVD_24	MAKE_BASE=TRUE	7 16
TP44	TRUE	NC_NB_RSVD_25	NC_NB_RSVD_25	MAKE_BASE=TRUE	7 16
TP34	TRUE	NC_NB_RSVD_26	NC_NB_RSVD_26	MAKE_BASE=TRUE	7 16
TP43	TRUE	NC_NB_RSVD_27	NC_NB_RSVD_27	MAKE_BASE=TRUE	7 16
TP33	TRUE	NC_NB_RSVD_35	NC_NB_RSVD_35	MAKE_BASE=TRUE	7 16
TP31	TRUE	NC_NB_RSVD_36	NC_NB_RSVD_36	MAKE_BASE=TRUE	7 16
TP41	TRUE	NC_NB_CFG_10	NC_NB_CFG_10	MAKE_BASE=TRUE	7 16
TP22	TRUE	NC_NB_CFG_11	NC_NB_CFG_11	MAKE_BASE=TRUE	7 16
TP21	TRUE	NC_NB_CFG_14	NC_NB_CFG_14	MAKE_BASE=TRUE	7 16
TP20	TRUE	NC_NB_CFG_15	NC_NB_CFG_15	MAKE_BASE=TRUE	7 16
TP19	TRUE	NC_NB_CFG_17	NC_NB_CFG_17	MAKE_BASE=TRUE	7 16
TP48	TRUE	NC_NB_NC_1	NC_NB_NC_1	MAKE_BASE=TRUE	7 16
TP18	TRUE	NC_NB_NC_2	NC_NB_NC_2	MAKE_BASE=TRUE	7 16
TP17	TRUE	NC_NB_NC_3	NC_NB_NC_3	MAKE_BASE=TRUE	7 16
TP16	TRUE	NC_NB_NC_4	NC_NB_NC_4	MAKE_BASE=TRUE	7 16
TP15	TRUE	NC_NB_NC_5	NC_NB_NC_5	MAKE_BASE=TRUE	7 16
TP14	TRUE	NC_NB_NC_6	NC_NB_NC_6	MAKE_BASE=TRUE	7 16
TP13	TRUE	NC_NB_NC_7	NC_NB_NC_7	MAKE_BASE=TRUE	7 16
TP12	TRUE	NC_NB_NC_8	NC_NB_NC_8	MAKE_BASE=TRUE	7 16
TP11	TRUE	NC_NB_NC_9	NC_NB_NC_9	MAKE_BASE=TRUE	7 16
TP10	TRUE	NC_NB_NC_10	NC_NB_NC_10	MAKE_BASE=TRUE	7 16
TP9	TRUE	NC_NB_NC_11	NC_NB_NC_11	MAKE_BASE=TRUE	7 16
TP8	TRUE	NC_NB_NC_12	NC_NB_NC_12	MAKE_BASE=TRUE	7 16
TP7	TRUE	NC_NB_NC_13	NC_NB_NC_13	MAKE_BASE=TRUE	7 16
TP6	TRUE	NC_NB_NC_14	NC_NB_NC_14	MAKE_BASE=TRUE	7 16
TP5	TRUE	NC_NB_RSVD_29	NC_NB_RSVD_29	MAKE_BASE=TRUE	7 16
TP4	TRUE	NC_NB_RSVD_28	NC_NB_RSVD_28	MAKE_BASE=TRUE	7 16
TP3	TRUE	NC_NB_RSVD_30	NC_NB_RSVD_30	MAKE_BASE=TRUE	7 16

TP49	TRUE	NC_CRT_DDC_CLK	NC_CRT_DDC_CLK	MAKE_BASE=TRUE	7 15
TP50	TRUE	NC_CRT_DDC_DATA	NC_CRT_DDC_DATA	MAKE_BASE=TRUE	7 15

Power Supply NO_TESTs

NO_TEST

CLOCK NO_TESTS

NO_TEST

LVDS NO_TESTS

NO_TEST

REQUIRED NETS

FUNC TEST - BATTERY CONNECTOR

x3	TP47	TRUE	BATT_POS	6 50
x3	TP49	TRUE	GND	
	TP31	TRUE	SMC_BS_ALRT_L	6 41 42 50
	TP44	TRUE	SMBUS_SMC_BSA_SCL	6 41 44 50 59 71
	TP33	TRUE	SMBUS_SMC_BSA_SDA	6 41 44 50 59 71

FUNC TEST - DC-IN CONNECTOR

x2	TP48	TRUE	PP18V5_DCIN	6 50 72
	TP55	TRUE	SYS_ONEWIRE	6 41 42 50
x2	TP80	TRUE	GND	

FUNC TEST - TEMP SENSOR CONNECTOR

	TP75	TRUE	SMBUS_SMC_0_S0_SCL	6 41 44 46 71
	TP72	TRUE	SMBUS_SMC_0_S0_SDA	6 41 44 46 71
	TP67	TRUE	PP3V3_A_S0	6 44 46 51 52 24 25 26 27 8 7 8 13 16 19 21 22 23 59 28 29 30 44 59 60 61 64

FUNC TEST - FAN CONNECTOR

	TP66	TRUE	PP5V_S0	32 53 63 72 7 7 8 27 40 43 47 51
	TP68	TRUE	FAN_RT_PWM	6 47
	TP69	TRUE	FAN_RT_TACH	6 47
	TP73	TRUE	GND	

FUNC TEST - CAMERA USB, LVDS, ALS

x2	TP54	TRUE	PP5V_S3_CAMERA_F	6 60 72
	TP58	TRUE	USB2_CAMERA_F_P	6 60 69
	TP56	TRUE	USB2_CAMERA_F_N	6 60 69
	TP57	TRUE	LCDBKLT_RTN<1..6>	6 60 64
	TP55	TRUE	LVDS_A_DATA_N<0..2>	6 15 60 67
	TP59	TRUE	LVDS_A_DATA_P<0..2>	6 15 60 67
	TP60	TRUE	PPVOUT_S0_LCDBKLT	6 60 64 72
	TP63	TRUE	LVDS_A_CLK_F_N	6 60
	TP65	TRUE	LVDS_A_CLK_F_P	6 60
	TP64	TRUE	LVDS_DDC_CLK	6 15 60
	TP62	TRUE	LVDS_DDC_DATA	6 15 60
	TP65	TRUE	PP3V3_S0_LCD_F	6 60 72
x2	TP66	TRUE	PP3V3_LCDVDD_SW_F	6 60 72
	TP71	TRUE	SMBUS_SMC_B_S3_SDA	6 41 44 60
	TP72	TRUE	SMBUS_SMC_B_S3_SCL	6 41 44 60
x10	TP73	TRUE	GND	

FUNC TEST - AUDIO CONNECTOR

	TP45	TRUE	HDA_SYNC	6 9 23 37 69
	TP46	TRUE	HDA_BIT_CLK	6 9 23 37 69
	TP38	TRUE	AUD_MIC_DATA	6 37 60
	TP36	TRUE	HDA_SDOUT	6 9 23 37 69
	TP37	TRUE	PPBUS_G3H	7 8 37 45 50 56 59 64 72
	TP35	TRUE	HDA_SDIN0	6 9 23 37 69
	TP40	TRUE	AUD_MIC_CLK	6 37 60
	TP39	TRUE	PM_SLP_S3_L	6 25 36 37 41 42 51 55

FUNC TEST - IPD CONNECTOR

	TP97	TRUE	SMC_LID	6 40 41 42
	TP96	TRUE	PP3V42_G3H_IPD_F	6 40
	TP98	TRUE	SMC_SYS_KBDLED	6 40 41
	TP99	TRUE	SMC_SYS_LED	6 40 41
	TP10	TRUE	USB2_WSPRING_N	6 9 24 40 69
	TP12	TRUE	USB2_WSPRING_P	6 9 24 40 69
	TP11	TRUE	SMC_ONOFF_L	6 7 40 41 42
	TP15	TRUE	USB_IR_N	6 7 9 24 40 59
	TP14	TRUE	USB_IR_P	6 7 9 24 40 59
	TP15	TRUE	PP5V_S0_KBDLED_F	6 7 40 72
	TP13	TRUE	PP5V_S3_TOPCASE_F	6 40
	TP18	TRUE	SMBUS_SMC_A_S3_SCL	6 7 36 40 41 44 71
	TP19	TRUE	SMBUS_SMC_A_S3_SDA	6 7 36 40 41 44 71
	TP20	TRUE	SMC_ONOFF_L	6 7 40 41 42
	TP15	TRUE	USB_IR_N	6 7 9 24 40 69
	TP22	TRUE	USB_IR_P	6 7 9 24 40 69
	TP67	TRUE	PP5V_S0_KBDLED_F	6 7 40 72
	TP35	TRUE	LSOC_H_R	6

FUNC TEST - XDP/ITP CONNECTOR

	TP55	TRUE	XDP_BPM_L<0..5>	6 10 13 66
	TP55	TRUE	NB_BSEL<0..2>	6 13 16 30 66
	TP80	TRUE	NB_CFG<3..8>	6 13 16
	TP81	TRUE	XDP_PWRGD	6 13
	TP83	TRUE	XDP_OBS20	6 13
	TP82	TRUE	TP_XDP_HOOK2	13
	TP84	TRUE	TP_XDP_HOOK3	13
	TP86	TRUE	LOCAL_CTRL_DATA	6 13 15
	TP87	TRUE	LOCAL_CTRL_CLK	6 13 15
	TP88	TRUE	XDP_TCK	6 10 13 66
	TP89	TRUE	SMC_WAKE_SCI_L	6 13 26 41
	TP90	TRUE	EXTAUSB_OC_L	6 9 13 24 39
	TP91	TRUE	SB_GPIO40	6 13 24
	TP92	TRUE	USB_EXTD_OC_L	6 13 24
	TP93	TRUE	WOW_EN	6 13 24 36
	TP94	TRUE	PM_LATRIGGER_L	6 13 24
	TP95	TRUE	EXTGPU_LVDS_EN	6 13 24
	TP96	TRUE	SB_GPIO30	6 13 24
	TP97	TRUE	EXTBUSB_OC_L	6 9 13 24
	TP98	TRUE	XDP_CLK_P	6 13 29 30 66 71
	TP99	TRUE	XDP_CLK_N	6 13 29 30 66 71
	TP91	TRUE	XDP_CPURST_L	6 13 66
	TP90	TRUE	XDP_DBRESET_L	6 10 13 66
	TP92	TRUE	XDP_TDO	6 10 13 66
	TP93	TRUE	XDP_TRST_L	6 10 13 66
	TP95	TRUE	XDP_TDI	6 10 13 66 63 64 66 71
	TP96	TRUE	XDP_TMS	6 10 13 66 63 64 66 71
	TP97	TRUE	PP3V3_A_S0	7 8 13 16 19 21 23 24 25 27 30 42 54 59
	TP98	TRUE	PP1V05_S0	6 7 8 13 16 19 21 23 24 25 27 30 42 54 59
x16	TP99	TRUE	GND	

FUNC TEST - RIO HATCH CONNECTOR

	TP16	TRUE	HDMI_HOST	6 37 63
	TP17	TRUE	DVI_HOST	6 37 63
	TP18	TRUE	TMDS_HTPLG	6 37 61 63
	TP19	TRUE	TMDS_DDC_SDA	6 37 61 62 63 67
	TP20	TRUE	TMDS_DDC_SCL	6 37 61 62 63 67
	TP21	TRUE	VGA_VSYNC	6 37 63
	TP22	TRUE	VGA_HSYNC	6 37 63
	TP23	TRUE	TMDS_TX_CONN_CLK_P	6 37 63 67
	TP24	TRUE	TMDS_TX_CONN_CLK_N	6 37 63 67
	TP25	TRUE	TMDS_TX_CONN_P<0..2>	6 37 63
	TP26	TRUE	TMDS_TX_CONN_N<0..2>	6 37 63
	TP27	TRUE	USB2_EXTA_F_P	6 37 39 69
	TP28	TRUE	USB2_EXTA_F_N	6 37 39 69
x14	TP29	TRUE	PP5V_S3_USB2_EXTA_F	6 37 39 72
	TP30	TRUE	PP5V_S0_DVIPORT	6 37 63 72
	TP31	TRUE	VGA_B	6 37 63 67
	TP32	TRUE	VGA_G	6 37 63 67
	TP33	TRUE	VGA_R	6 37 63 67
x14	TP10	TRUE	GND	

FUNC TEST - AIRPORT

	TP41	TRUE	CK505_SRC_CLKREQ6_L	6 7 29 36
	TP42	TRUE	PCIE_WAKE_L	6 7 25 36
	TP43	TRUE	AIRPORT_RST_L	6 7 28 36
	TP44	TRUE	SMBUS_SMC_A_S3_SCL	6 7 36 40 41 44 71
	TP45	TRUE	SMBUS_SMC_A_S3_SDA	6 7 36 40 41 44 71
	TP46	TRUE	GND	

NICE2HAVE NETS

FUNC TEST - Power Supplies

	TP2	TRUE	PPVCORE_S0_CPU	6 8 11 12 52 65 72
	TP54	TRUE	PP0V9_S0	6 8 33 55 72
	TP55	TRUE	PP1V05_S0	6 7 8 10 11 12 13 14 18 19 21 23 25 27 30 42 54 72
	TP57	TRUE	PP1V25_S0	6 8 16 18 19 21 26 27 51 57 72
	TP60	TRUE	PP1V5_S0	6 8 11 12 22 26 27 54 72
	TP59	TRUE	PP1V8_S0	6 8 19 22 51 61 72
	TP58	TRUE	PPVCORE_S0_NB_GFX	6 8 18 22 45 53 65 72
	TP61	TRUE	PP5V_S0	6 7 8 22 27 40 43 47 51 52 53 63 72
	TP60	TRUE	PP3V3_S0	72
	TP65	TRUE	PP1V8_S3	6 8 16 18 21 31 32 34 35 51 55 58 72
	TP63	TRUE	PP3V3_S3	6 8 36 42 44 48 51 58 60 72
	TP62	TRUE	PP5V_S3	6 8 40 58 60 72
	TP67	TRUE	PP3V3_S5	6 8 24 25 26 27 28 36 43 44 49 51 56 57 58 60 72
	TP68	TRUE	PP5V_S5	6 8 27 39 51 54 55 56 58 72
	TP69	TRUE	PP3V42_G3H	6 8 23 26 27 28 39 40 41 42 43 44 57 59 72
	TP72	TRUE	PP18V5_G3H	6 8 50 59 72
	TP73	TRUE	PPDCIN_G3H	6 8 50 57 72
	TP72	TRUE	PPBUS_G3H	6 7 8 37 45 50 56 59 64 72
	TP71	TRUE	PPBUS_R_G3H	6 8 42 52 53 54 55 59 72

FUNC TEST - M93 WIRELESS CONNECTOR

	TP78	TRUE	PLT_RST_L	6 24 28 60 64
	TP75	TRUE	PCIE_WAKE_L	6 7 25 36
	TP79	TRUE	CK505_SRC_CLKREQ6_L	6 7 29 36
	TP78	TRUE	PCIE_CLK100M_MINI_N_F	6 36
	TP76	TRUE	PCIE_CLK100M_MINI_P_F	6 36
	TP77	TRUE	PCIE_E_D2R_N_F	6 36
	TP80	TRUE	PCIE_E_D2R_P_F	6 36
	TP83	TRUE	PCIE_E_R2D_C_N_F	6 7 36
	TP84	TRUE	PCIE_E_R2D_C_P_F	6 7 36
	TP82	TRUE	AIRPORT_RST_L	6 7 28 36
	TP99	TRUE	SMB_AIRPORT_CONN_CLK	6 36
	TP98	TRUE	SMB_AIRPORT_CONN_DATA	6 36
	TP61	TRUE	PCIE_E_R2D_C_N_F	6 7 36
	TP62	TRUE	PCIE_E_R2D_C_P_F	6 7 36
	TP63	TRUE	PP3V3_S3_AP_AUX	6 36 72

x13	TP22	GND		

Functional Test and No-Tests

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	7	73

"S0,S0M" RAILS

(REGULATOR OUTPUT CPU VCORE PWR)

PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE

(CPU VCOR PWRE)

PPVCORE_S0_CPU

PP0V9_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(DDR2 TERMINATION 0.9V PWR)

PP0V9_S0

(REGULATOR OUTPUT CPU 0.90V PWR)

PP0V9_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(NB MEM VREF 0.9V PWR)

R0800
0
5%
1/20W
MF
201

PP0V9_S3_MEM_NBVREFA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

R0801
0
5%
1/20W
MF
201

PP0V9_S3_MEM_NBVREFB
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V

PP1V05_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V25_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP1V8_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PPVCORE_S0_NB_GFX
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.45V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP3V3_A_S0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3_S0 split into 2
for layout optimization
of plane splits

PP3V3_B_S0
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

3V3_B_S0 plane on right side
(peninsula)

"S3" RAILS

PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

"S5" RAILS

PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

"G3H" RAILS

PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

PP18V5_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPBUS_R_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

Power Aliases

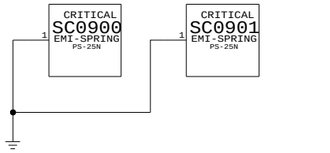
SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

APPLE INC.

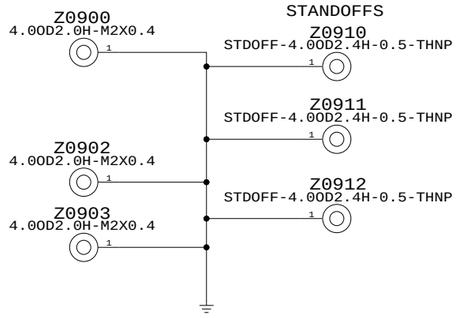
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 8 OF 73	

EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900



BOSSES TO CONNECT TO HEATSINK



SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

			NO_TEST
NC_SMC_PA0	NC_SMC_PA0	TRUE	
NC_SMC_PA1	NC_SMC_PA1	TRUE	
NC_SMC_PB0	NC_SMC_PB0	TRUE	
NC_SMC_PG0	NC_SMC_PG0	TRUE	
NC_SMC_P14	NC_SMC_P14	TRUE	
NC_SMC_P20	NC_SMC_P20	TRUE	
NC_SMC_P21	NC_SMC_P21	TRUE	
NC_SMC_P22	NC_SMC_P22	TRUE	
NC_SMC_P23	NC_SMC_P23	TRUE	
NC_SMC_P26	NC_SMC_P26	TRUE	
NC_SMC_P27	NC_SMC_P27	TRUE	
NC_SMC_P41	NC_SMC_P41	TRUE	
NC_SMC_P43	NC_SMC_P43	TRUE	
NC_SMC_P44	NC_SMC_P44	TRUE	
NC_SMC_P46	NC_SMC_P46	TRUE	
NC_SMC_P62	NC_SMC_P62	TRUE	
NC_SMC_P63	NC_SMC_P63	TRUE	
NC_SMC_P64	NC_SMC_P64	TRUE	
NC_SMC_P67	NC_SMC_P67	TRUE	
NC_SMC_P81	NC_SMC_P81	TRUE	
NC_SMC_GFX_OVERTEMP_L	NC_SMC_GFX_OVERTEMP_L	TRUE	
NC_EXCARD_OC_L	NC_EXCARD_OC_L	TRUE	
NC_SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	TRUE	
NC_SMC_EXCARD_CP	NC_SMC_EXCARD_CP	TRUE	
NC_SMC_ENRGYSTR_LDO_EN	NC_SMC_ENRGYSTR_LDO_EN	TRUE	
NC_SMC_ENRGYSTR_LDO_PGOOD	NC_SMC_ENRGYSTR_LDO_PGOOD	TRUE	
NC_ALS_RIGHT	NC_ALS_RIGHT	TRUE	
NC_ALS_GAIN	NC_ALS_GAIN	TRUE	
NC_SMC_EXCARD_PWR_EN	NC_SMC_EXCARD_PWR_EN	TRUE	
NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	TRUE	
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	TRUE	
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	TRUE	
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	TRUE	
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	TRUE	
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	TRUE	
NC_SMC_PF0	NC_SMC_PF0	TRUE	
NC_SMC_BATT_VSET	NC_SMC_BATT_VSET	TRUE	
NC_SMC_SYS_VSET	NC_SMC_SYS_VSET	TRUE	
NC_SMC_RSTGATE_L	NC_SMC_RSTGATE_L	TRUE	
NC_SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	TRUE	
NC_SYS_ISET	NC_SYS_ISET	TRUE	
NC_BATT_ISET	NC_BATT_ISET	TRUE	
NC_ISENSE_CAL_EN	NC_ISENSE_CAL_EN	TRUE	
NC_SMC_FWE	NC_SMC_FWE	TRUE	
NC_SMC_ANALOG_ID	NC_SMC_ANALOG_ID	TRUE	
NC_SMC_TEST_DAC1	NC_SMC_TEST_DAC1	TRUE	
NC_SMC_TEST_DAC2	NC_SMC_TEST_DAC2	TRUE	
NC_SMC_TEST_DAC3	NC_SMC_TEST_DAC3	TRUE	

SMC_SMS_INT	SMC_SMS_INT	
SMC_ADAPTER_EN	SMC_ADAPTER_EN	

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

		NO_TEST
NC_LVDS_B_CLK_N	NC_LVDS_B_CLK_N	TRUE
NC_LVDS_B_CLK_P	NC_LVDS_B_CLK_P	TRUE
NC_LVDS_B_DATA_N0	NC_LVDS_B_DATA_N0	TRUE
NC_LVDS_B_DATA_N1	NC_LVDS_B_DATA_N1	TRUE
NC_LVDS_B_DATA_N2	NC_LVDS_B_DATA_N2	TRUE
NC_LVDS_B_DATA_N3	NC_LVDS_B_DATA_N3	TRUE
NC_LVDS_B_DATA_P0	NC_LVDS_B_DATA_P0	TRUE
NC_LVDS_B_DATA_P1	NC_LVDS_B_DATA_P1	TRUE
NC_LVDS_B_DATA_P2	NC_LVDS_B_DATA_P2	TRUE
NC_LVDS_B_DATA_P3	NC_LVDS_B_DATA_P3	TRUE
NC_LVDS_A_DATA_P3	NC_LVDS_A_DATA_P3	TRUE
NC_LVDS_A_DATA_N3	NC_LVDS_A_DATA_N3	TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

NC_PEG_D2R_N0	NC_PEG_D2R_N0	TRUE
NC_PEG_D2R_N2	NC_PEG_D2R_N2	TRUE
NC_PEG_D2R_N3	NC_PEG_D2R_N3	TRUE
NC_PEG_D2R_N4	NC_PEG_D2R_N4	TRUE
NC_PEG_D2R_N5	NC_PEG_D2R_N5	TRUE
NC_PEG_D2R_N6	NC_PEG_D2R_N6	TRUE
NC_PEG_D2R_N7	NC_PEG_D2R_N7	TRUE
NC_PEG_D2R_N8	NC_PEG_D2R_N8	TRUE
NC_PEG_D2R_N9	NC_PEG_D2R_N9	TRUE
NC_PEG_D2R_N10	NC_PEG_D2R_N10	TRUE
NC_PEG_D2R_N11	NC_PEG_D2R_N11	TRUE
NC_PEG_D2R_N12	NC_PEG_D2R_N12	TRUE
NC_PEG_D2R_N13	NC_PEG_D2R_N13	TRUE
NC_PEG_D2R_N14	NC_PEG_D2R_N14	TRUE
NC_PEG_D2R_N15	NC_PEG_D2R_N15	TRUE
NC_PEG_D2R_P0	NC_PEG_D2R_P0	TRUE
NC_PEG_D2R_P2	NC_PEG_D2R_P2	TRUE
NC_PEG_D2R_P3	NC_PEG_D2R_P3	TRUE
NC_PEG_D2R_P4	NC_PEG_D2R_P4	TRUE
NC_PEG_D2R_P5	NC_PEG_D2R_P5	TRUE
NC_PEG_D2R_P6	NC_PEG_D2R_P6	TRUE
NC_PEG_D2R_P7	NC_PEG_D2R_P7	TRUE
NC_PEG_D2R_P8	NC_PEG_D2R_P8	TRUE
NC_PEG_D2R_P9	NC_PEG_D2R_P9	TRUE
NC_PEG_D2R_P10	NC_PEG_D2R_P10	TRUE
NC_PEG_D2R_P11	NC_PEG_D2R_P11	TRUE
NC_PEG_D2R_P12	NC_PEG_D2R_P12	TRUE
NC_PEG_D2R_P13	NC_PEG_D2R_P13	TRUE
NC_PEG_D2R_P14	NC_PEG_D2R_P14	TRUE
NC_PEG_D2R_P15	NC_PEG_D2R_P15	TRUE
NC_PEG_R2D_C_N4	NC_PEG_R2D_C_N4	TRUE
NC_PEG_R2D_C_N5	NC_PEG_R2D_C_N5	TRUE
NC_PEG_R2D_C_N6	NC_PEG_R2D_C_N6	TRUE
NC_PEG_R2D_C_N7	NC_PEG_R2D_C_N7	TRUE
NC_PEG_R2D_C_N8	NC_PEG_R2D_C_N8	TRUE
NC_PEG_R2D_C_N9	NC_PEG_R2D_C_N9	TRUE
NC_PEG_R2D_C_N10	NC_PEG_R2D_C_N10	TRUE
NC_PEG_R2D_C_N11	NC_PEG_R2D_C_N11	TRUE
NC_PEG_R2D_C_N12	NC_PEG_R2D_C_N12	TRUE
NC_PEG_R2D_C_N13	NC_PEG_R2D_C_N13	TRUE
NC_PEG_R2D_C_N14	NC_PEG_R2D_C_N14	TRUE
NC_PEG_R2D_C_N15	NC_PEG_R2D_C_N15	TRUE
NC_PEG_R2D_C_P4	NC_PEG_R2D_C_P4	TRUE
NC_PEG_R2D_C_P5	NC_PEG_R2D_C_P5	TRUE
NC_PEG_R2D_C_P6	NC_PEG_R2D_C_P6	TRUE
NC_PEG_R2D_C_P7	NC_PEG_R2D_C_P7	TRUE
NC_PEG_R2D_C_P8	NC_PEG_R2D_C_P8	TRUE
NC_PEG_R2D_C_P9	NC_PEG_R2D_C_P9	TRUE
NC_PEG_R2D_C_P10	NC_PEG_R2D_C_P10	TRUE
NC_PEG_R2D_C_P11	NC_PEG_R2D_C_P11	TRUE
NC_PEG_R2D_C_P12	NC_PEG_R2D_C_P12	TRUE
NC_PEG_R2D_C_P13	NC_PEG_R2D_C_P13	TRUE
NC_PEG_R2D_C_P14	NC_PEG_R2D_C_P14	TRUE
NC_PEG_R2D_C_P15	NC_PEG_R2D_C_P15	TRUE

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.38 MM

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

NC_SATA_A_D2R_N	NC_SATA_A_D2R_N	TRUE
NC_SATA_A_D2R_P	NC_SATA_A_D2R_P	TRUE
NC_SATA_A_R2D_C_N	NC_SATA_A_R2D_C_N	TRUE
NC_SATA_A_R2D_C_P	NC_SATA_A_R2D_C_P	TRUE
NC_SATA_B_D2R_N	NC_SATA_B_D2R_N	TRUE
NC_SATA_B_D2R_P	NC_SATA_B_D2R_P	TRUE
NC_SATA_B_R2D_C_N	NC_SATA_B_R2D_C_N	TRUE
NC_SATA_B_R2D_C_P	NC_SATA_B_R2D_C_P	TRUE
NC_SATA_C_D2R_N	NC_SATA_C_D2R_N	TRUE
NC_SATA_C_D2R_P	NC_SATA_C_D2R_P	TRUE
NC_SATA_C_R2D_C_N	NC_SATA_C_R2D_C_N	TRUE
NC_SATA_C_R2D_C_P	NC_SATA_C_R2D_C_P	TRUE

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

NC_CK505_SRC1_N	NC_CK505_SRC1_N	TRUE
NC_CK505_SRC1_P	NC_CK505_SRC1_P	TRUE
NC_CK505_SRC_CLKREQ1_L	NC_CK505_SRC_CLKREQ1_L	TRUE
NC_CK505_SRC3_N	NC_CK505_SRC3_N	TRUE
NC_CK505_SRC3_P	NC_CK505_SRC3_P	TRUE
NC_CK505_SRC_CLKREQ3_L	NC_CK505_SRC_CLKREQ3_L	TRUE
NC_CK505_SRC4_N	NC_CK505_SRC4_N	TRUE
NC_CK505_SRC4_P	NC_CK505_SRC4_P	TRUE
NC_CK505_SRC_CLKREQ4_L	NC_CK505_SRC_CLKREQ4_L	TRUE
NC_CK505_SRC7_N	NC_CK505_SRC7_N	TRUE
NC_CK505_SRC7_P	NC_CK505_SRC7_P	TRUE
NC_CK505_PGMODE	NC_CK505_PGMODE	TRUE
NC_CK505_SRC8_N	NC_CK505_SRC8_N	TRUE
NC_CK505_SRC8_P	NC_CK505_SRC8_P	TRUE
NC_CK505_SRC_CLKREQ8_L	NC_CK505_SRC_CLKREQ8_L	TRUE
NC_GPU_STOP_L	NC_GPU_STOP_L	TRUE
NC_CK505_PCI1_CLK	NC_CK505_PCI1_CLK	TRUE
NC_CK505_PCI2_CLK	NC_CK505_PCI2_CLK	TRUE
NC_CK505_PCI4_CLK	NC_CK505_PCI4_CLK	TRUE

SB ALIASES

NO-CONNECT UNUSED INTERFACE PORTS

VR_PWRGD_CK505	VR_PWRGD_CK505	
PM_SB_PWROK	PM_SB_PWROK	
PCI_AD<0..31>	NC_PCI_AD<0..31>	TRUE
PCI_C_BE_L<0..3>	NC_PCI_C_BE_L<0..3>	TRUE
NC_PCI_PAR	NC_PCI_PAR	TRUE
TP_PCI_RST_L	TP_PCI_RST_L	

NB ALIASES

GFX_VR_EN	GFX_VR_EN	
VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY	
NB_CLK96M_DOT_P	NB_CLK96M_DOT_P	
NB_CLK96M_DOT_N	NB_CLK96M_DOT_N	
NB_CLK100M_DPLLSS_P	NB_CLK100M_DPLLSS_P	
NB_CLK100M_DPLLSS_N	NB_CLK100M_DPLLSS_N	
LCDBKLT_PWM_UNBUF	LCDBKLT_PWM_UNBUF	
LCDBKLT_PWREN	LCDBKLT_PWREN	

AUDIO ALIASES

HDA_BIT_CLK	HDA_BIT_CLK	
HDA_SYNC	HDA_SYNC	
HDA_RST_L	HDA_RST_L	
HDA_SDIN0	HDA_SDIN0	
HDA_SDOUT	HDA_SDOUT	

USB ALIASES

USB PORT [0] = External USB2.0 Port A

USB2_EXTA_P	USB2_EXTA_P	
USB2_EXTA_N	USB2_EXTA_N	
EXTAUSB_OC_L	EXTAUSB_OC_L	
USB2_MUXED_EXTA_N	USB2_MUXED_EXTA_N	
USB2_MUXED_EXTA_P	USB2_MUXED_EXTA_P	

USB PORT [1] = PCI-E Mini Card

USB2_AIRPORT_P	USB2_AIRPORT_P	
USB2_AIRPORT_N	USB2_AIRPORT_N	

USB PORT [2] = Unused

TP_USB2_3G_P	TP_USB2_3G_P	
TP_USB2_3G_N	TP_USB2_3G_N	

USB PORT [3] = CAMERA

USB2_CAMERA_P	USB2_CAMERA_P	
USB2_CAMERA_N	USB2_CAMERA_N	

USB PORT [4] = IR CONTROLLER

USB_IR_P	USB_IR_P	
USB_IR_N	USB_IR_N	

USB PORT [5] = Trackpad(Wellspring)

USB2_WSPRING_P	USB2_WSPRING_P	
USB2_WSPRING_N	USB2_WSPRING_N	

USB PORT [6] = BLUETOOTH

NC_USB_BT_P	NC_USB_BT_P	
NC_USB_BT_N	NC_USB_BT_N	

USB PORT [7] = Unused

NC_USB2_EXTB_P	NC_USB2_EXTB_P	
NC_USB2_EXTB_N	NC_USB2_EXTB_N	
EXTBUSB_OC_L	EXTBUSB_OC_L	

USB PORT [8] = Unused

TP_USB_EXCARD_P	TP_USB_EXCARD_P
TP_USB_EXCARD_N	TP_USB_EXCARD_N

USB PORT [9] = Unused

TP_USB_EXTC_P	TP_USB_EXTC_P
TP_USB_EXTC_N	TP_USB_EXTC_N

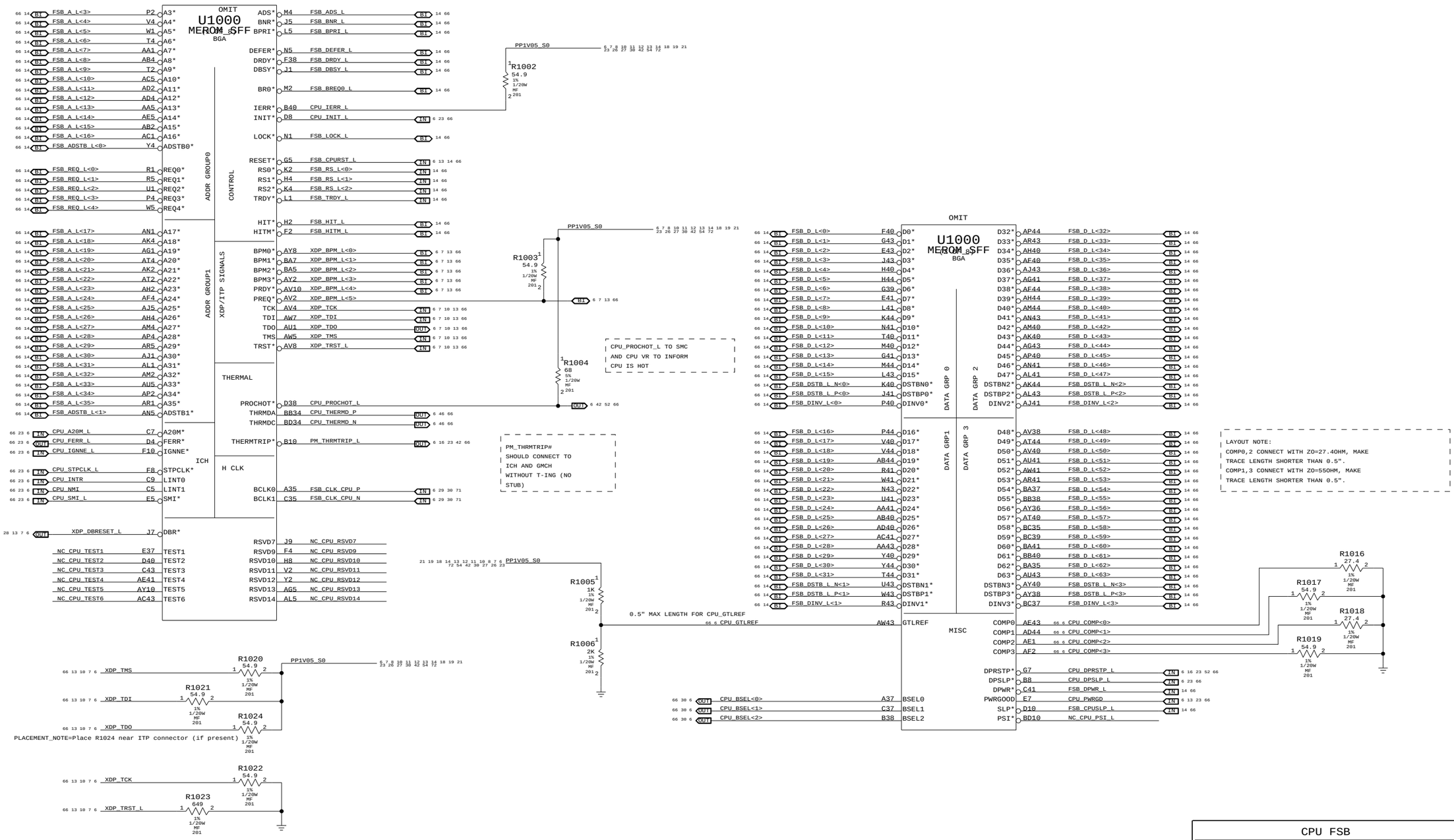
SIGNAL ALIAS /RESET

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE D | DRAWING NUMBER 051-7230 | REV. B.0.0

SCALE NONE | SHT 9 OF 73



CPU FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

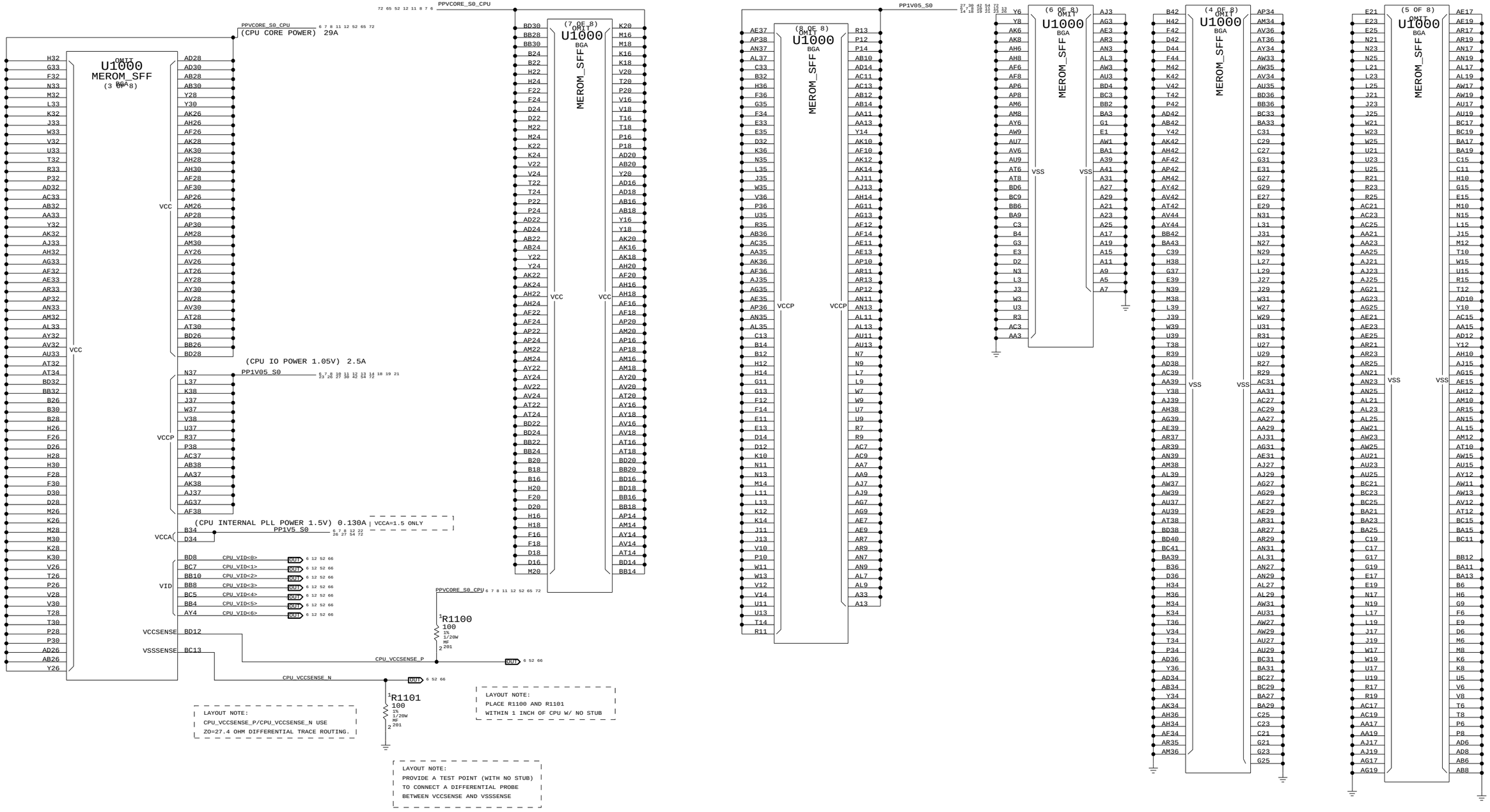
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 10 OF 73	


PPVCORE_S0_CPU
72 65 52 12 11 8 7 6
PPVCORE_S0_CPU
6 7 8 11 12 52 65 72
(CPU CORE POWER) 29A
U1000
MEROM_SFF
(3 OF 8)
OMIT
BGA
VCC
VCCP
(CPU IO POWER 1.05V) 2.5A
PP1V05_S0
6 7 8 10 11 12 13 14 18 19 21 23 26 27 30 42 64 72
(CPU INTERNAL PLL POWER 1.5V) 0.130A
VCCA=1.5 ONLY
PP1V5_S0
6 7 8 12 22 26 27 54 72
VCCA
VID
CPU_VID<0>
CPU_VID<1>
CPU_VID<2>
CPU_VID<3>
CPU_VID<4>
CPU_VID<5>
CPU_VID<6>
OUT
6 12 52 66
VCCSENSE
VSSSENSE
CPU_VCCSENSE_P
CPU_VCCSENSE_N
R1100
100
1%
1/20W
MF
201
R1101
LAYOUT NOTE:
CPU_VCCSENSE_P/CPU_VCCSENSE_N USE
ZO=27.4 OHM DIFFERENTIAL TRACE ROUTING.
LAYOUT NOTE:
PLACE R1100 AND R1101
WITHIN 1 INCH OF CPU W/ NO STUB
LAYOUT NOTE:
PROVIDE A TEST POINT (WITH NO STUB)
TO CONNECT A DIFFERENTIAL PROBE
BETWEEN VCCSENSE AND VSSSENSE
(7 OF 8)
(8 OF 8)
(6 OF 8)
(4 OF 8)
(5 OF 8)
PP1V05_S0
VSS
CPU Power & Ground
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE
D
DRAWING NUMBER
051-7230
REV.
B.0.0
SCALE
NONE
SHT
11
OF
73

CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 1uF 0402
Intel recommends 32+28 but is evaluating 24+24

72 65 52 11 8 7 6 PPVCORE_S0_CPU

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1200 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1201 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1202 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1203 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1204 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1205 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1206 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1207 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1208 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1210 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1211 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1212 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1213 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1214 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1215 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1216 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1217 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1218 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITIICAL C1220 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1221 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1222 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1223 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1224 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1225 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1226 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1227 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1228 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1230 10UF 20% 6.3V X5R 603
OMIT CRITICAL C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1240 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1241 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1242 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1243 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1244 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1245 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1246 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1247 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1248 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1250 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1251 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1252 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1253 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1254 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1255 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1256 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1257 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1258 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C1260 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1261 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1262 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1263 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1264 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1265 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1266 2.2UF 20% 6.3V CERM 402-LF
OMIT CRITICAL C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 330UF 20% 2.0V TANT D2T
CRITICAL C1271 330UF 20% 2.0V TANT D2T

CRITICAL C1272 330UF 20% 2.0V TANT D2T

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

Intel recommends 3x220UF @ 9mOHM

CPU VCORE VID CONNECTIONS

66 52 11 6 CPU_VID<0..6> — IMVP6_VID<0..6> 66
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

72 54 27 26 22 11 8 7 6 PP1V5_S0

1x 10uF, 1x 0.01uF

OMIT C1280 10UF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

23 21 19 18 14 13 11 10 8 7 6 72 64 42 30 27 26 PP1V05_S0

1X 330UF, 12X 2.2UF

OMIT C1283 2.2UF 20% 6.3V CERM 402-LF
OMIT C1284 2.2UF 20% 6.3V CERM 402-LF
OMIT C1285 2.2UF 20% 6.3V CERM 402-LF
OMIT C1286 2.2UF 20% 6.3V CERM 402-LF
OMIT C1287 2.2UF 20% 6.3V CERM 402-LF
OMIT C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 330UF 20% 2.5V POLY CASE-C2-SM-1

OMIT C1291 2.2UF 20% 6.3V CERM 402-LF
OMIT C1292 2.2UF 20% 6.3V CERM 402-LF
OMIT C1293 2.2UF 20% 6.3V CERM 402-LF
OMIT C1294 2.2UF 20% 6.3V CERM 402-LF
OMIT C1295 2.2UF 20% 6.3V CERM 402-LF
OMIT C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

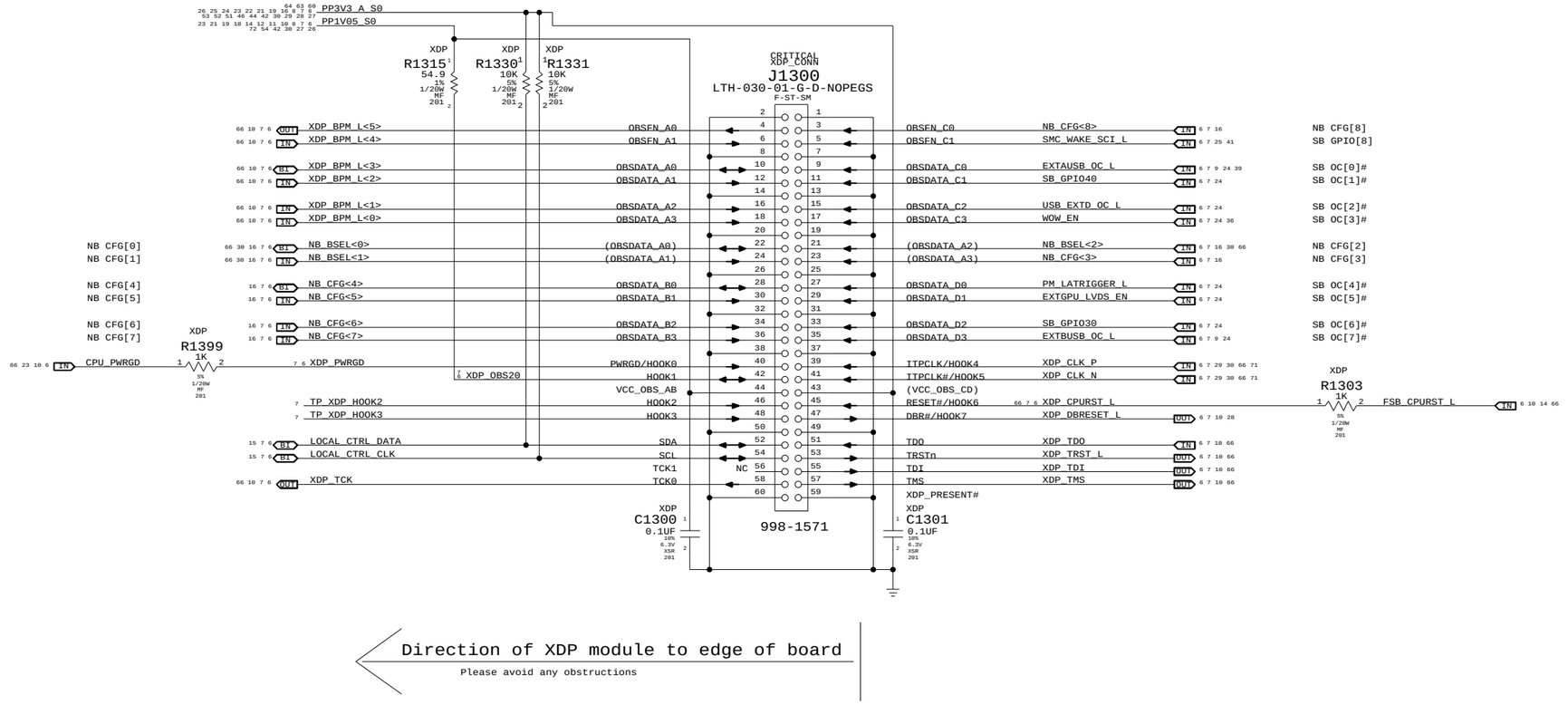
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 12 OF 73	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module to edge of board

Please avoid any obstructions

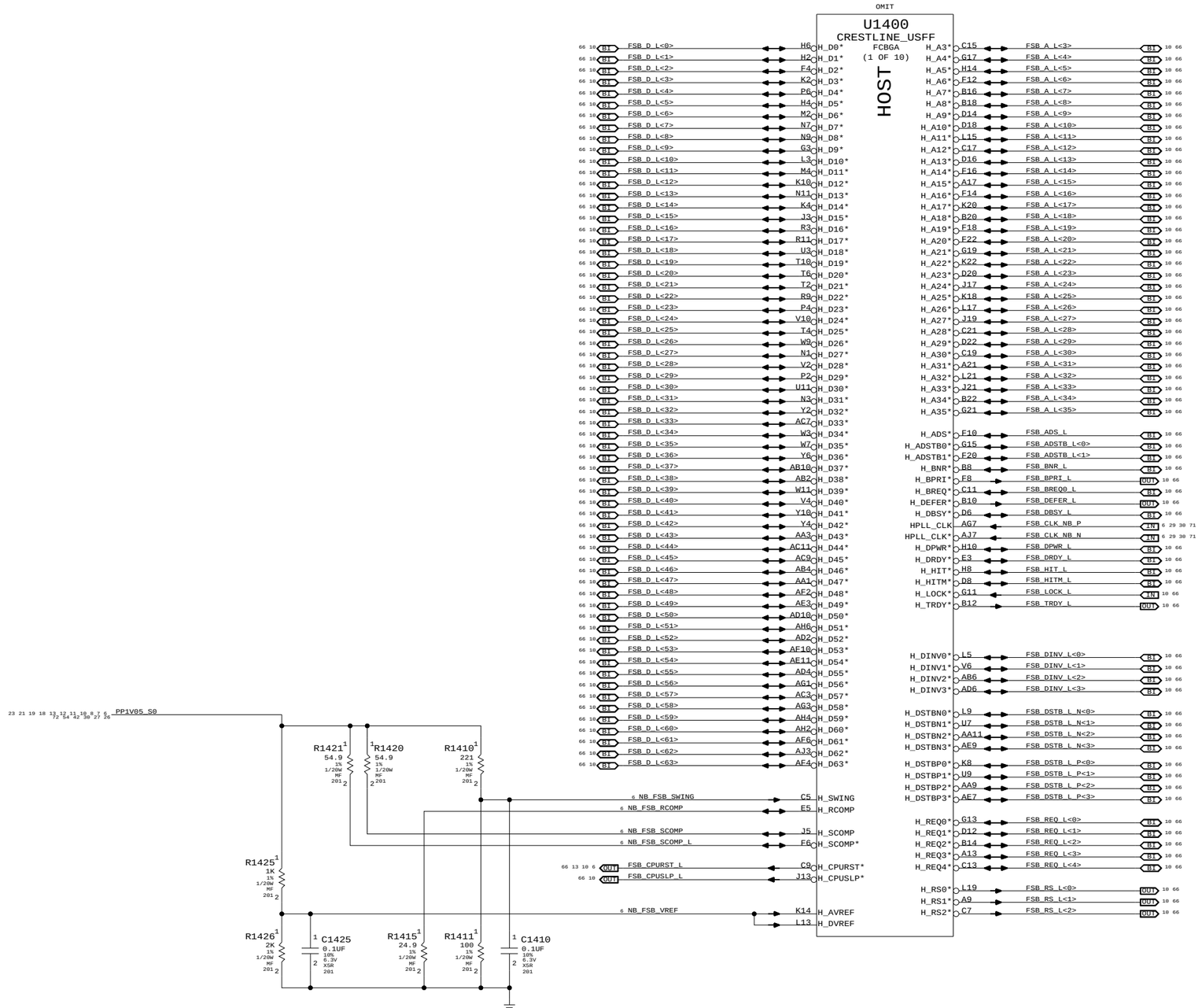
eXtended Debug Port (XDP)

SYNC_MASTER=M75 SYNC_DATE=01/24/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 13 OF 73	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 14 OF 73	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

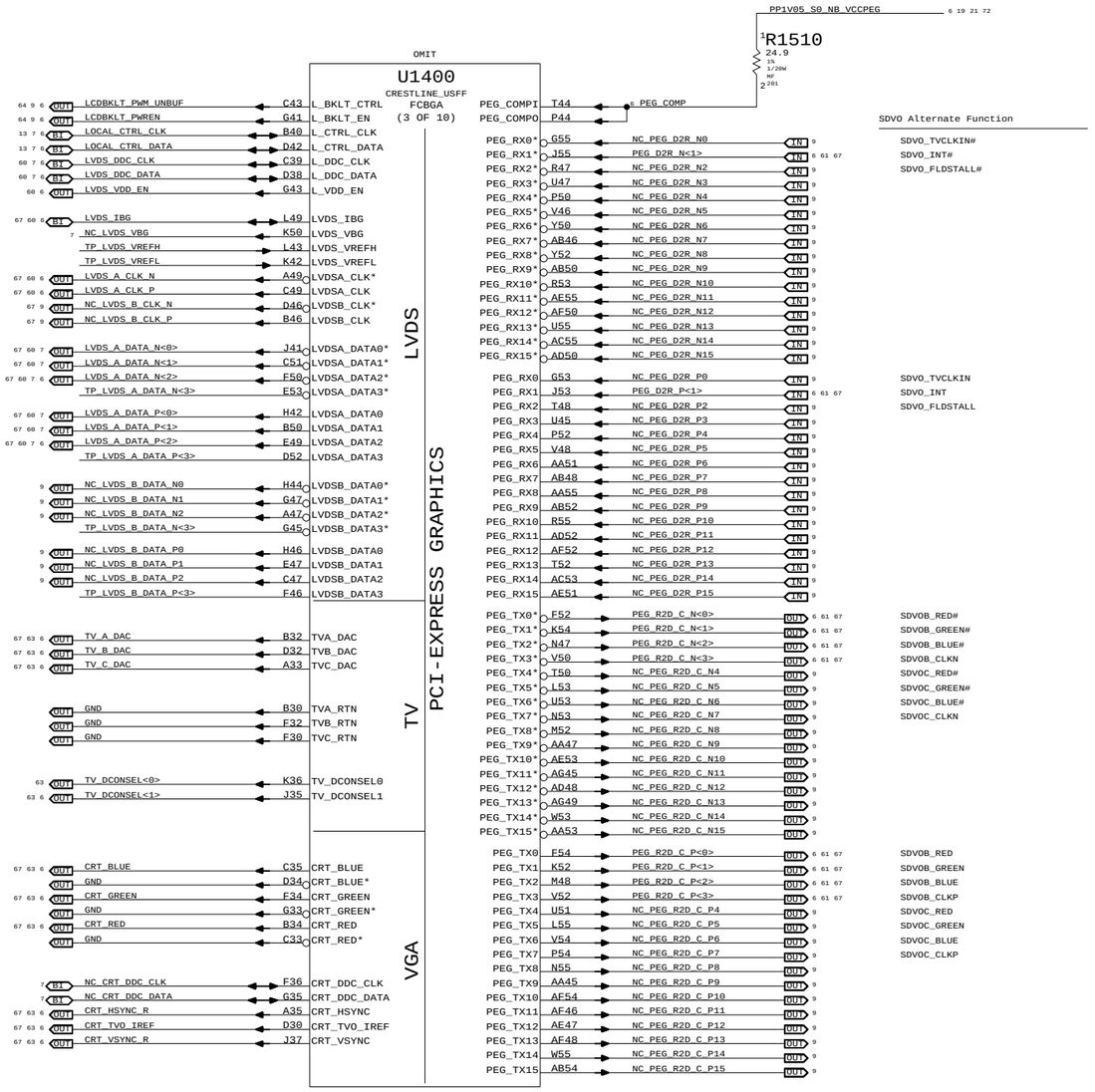
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 15 OF 73	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB CFG<5> chooses DMI x4 w/ TP

NB_CFG<9> — NBCFG_PEG_REVERSE — R1659 4.02K 1% 1/20W MF 201

NB_CFG<16> — NBCFG_DYN_ODT_DISABLE — R1666 4.02K 1% 1/20W MF 201

PP3V3_A_S0 — NBCFG_SDVO_MODE_REVERSE — R1669 4.02K 1% 1/20W MF 201 — NB_CFG<19>

PP3V3_A_S0 — NBCFG_SDVO_AND_PCIE — R1670 4.02K 1% 1/20W MF 201 — NB_CFG<20>

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

PP3V3_A_S0 — R1630 10K 5% 1/20W MF 201 — R1631 10K 5% 1/20W MF 201

PM_EXTTS_L<0>
PM_EXTTS_L<1>

OMIT

U1400
CRESTLINE_USFF
FCBGA
(2 OF 10)

RSVD bit ordering based on CRB numbering

TP_NB_RSVD<42>	A39	
NC_NB_RSVD_8	AG11	
NC_NB_RSVD_7	AG9	
NC_NB_RSVD_5	AH10	
NC_NB_RSVD_6	AJ11	
TP_NB_RSVD<12>	AJ43	
TP_NB_RSVD<11>	AL43	
TP_NB_RSVD<13>	AN43	
TP_NB_RSVD<10>	AR43	
TP_NB_RSVD<45>	B36	
TP_NB_RSVD<41>	B38	
NC_NB_RSVD_21	B55	
NC_NB_RSVD_28	BA33	
NC_NB_RSVD_35	BB22	
NC_NB_RSVD_29	BC33	
NC_NB_RSVD_30	BF22	
NC_NB_RSVD_31	BE23	
NC_NB_RSVD_24	BH18	
NC_NB_RSVD_36	BE27	
NC_NB_RSVD_22	BJ17	
NC_NB_RSVD_25	BK16	
NC_NB_RSVD_27	BK18	
TP_NB_RSVD<34>	BK32	
NC_NB_RSVD_26	BL17	
NC_NB_RSVD_23	BL19	
TP_NB_RSVD<43>	C37	
TP_NB_RSVD<9>	D10	
TP_NB_RSVD<44>	D36	
NC_NB_RSVD_4	G51	
TP_NB_RSVD<20>	G9	
NC_NB_RSVD_3	H52	
NC_NB_RSVD_14	J25	
NC_NB_RSVD_1	M46	
NC_NB_RSVD_2	N45	

RSVD

DDR MUXING

SM_CK0	BC37	MEM_CLK_P<0>
SM_CK1	BC25	MEM_CLK_P<1>
SM_CK3	BB36	MEM_CLK_P<3>
SM_CK4	BB24	MEM_CLK_P<4>
SM_CK0*	BA37	MEM_CLK_N<0>
SM_CK1*	BC23	MEM_CLK_N<1>
SM_CK3*	BB34	MEM_CLK_N<3>
SM_CK4*	BB26	MEM_CLK_N<4>
SM_CKE0	BE33	MEM_CKE<0>
SM_CKE1	BE35	MEM_CKE<1>
SM_CKE3	BF40	MEM_CKE<3>
SM_CKE4	BE39	MEM_CKE<4>
SM_CS0*	BA23	MEM_CS_L<0>
SM_CS1*	BH16	MEM_CS_L<1>
SM_CS2*	BE15	MEM_CS_L<2>
SM_CS3*	BH14	MEM_CS_L<3>
SM_ODT0	BJ15	MEM_ODT<0>
SM_ODT1	BF20	MEM_ODT<1>
SM_ODT2	BE13	MEM_ODT<2>
SM_ODT3	BH12	MEM_ODT<3>
SM_RCOMP	BL13	MEM_RCOMP
SM_RCOMP*	BK14	MEM_RCOMP_L
SM_RCOMP_VOH	BK36	MEM_RCOMP_VOH
SM_RCOMP_VOL	BL37	MEM_RCOMP_VOL
SM_VREF0	AM54	PP0V9_S3M_MEM_NBVREFA
SM_VREF1	AT12	PP0V9_S3M_MEM_NBVREFB

PP1V8_S3

R1610 20 1% 1/20W MF 201
R1620 1K 1% 1/20W MF 201
C1623 0.01UF 10% 10V X5R 201
C1622 OMIT 2.2UF 20% 6.3V CERM 402-LF
R1622 3.01K 1% 1/20W MF 201
C1615 0.1UF 10% 6.3V X5R 201
C1616 0.1UF 10% 6.3V X5R 201
R1611 20 1% 1/20W MF 201
C1625 0.01UF 10% 10V X5R 201
C1624 OMIT 2.2UF 20% 6.3V CERM 402-LF
R1624 1K 1% 1/20W MF 201

CLK

DPLL_REF_CLK	C45	NB_CLK96M_DOT_P
DPLL_REF_CLK*	B44	NB_CLK96M_DOT_N
DPLL_REF_SSCLK	H50	NB_CLK100M_DPLLSS_P
DPLL_REF_SSCLK*	G49	NB_CLK100M_DPLLSS_N
PEG_CLK	N51	NB_CLK100M_PCIE_P
PEG_CLK*	M50	NB_CLK100M_PCIE_N

Clk used for PEG and DMI

CFG

NB_BSEL<0>	H28	CFG0	
NB_BSEL<1>	G25	CFG1	
NB_BSEL<2>	C25	CFG2	
NB_CFG<3>	K24	CFG3	IPU
NB_CFG<4>	B28	CFG4	IPU
NB_CFG<5>	G27	CFG5	IPU
NB_CFG<6>	B26	CFG6	IPU
NB_CFG<7>	D26	CFG7	IPU
NB_CFG<8>	D24	CFG8	IPU
NB_CFG<9>	F26	CFG9	IPU
NC_NB_CFG_10	A25	CFG10	IPU
NC_NB_CFG_11	L23	CFG11	IPU
TP_NB_CFG<12>	D28	CFG12	IPU
TP_NB_CFG<13>	F24	CFG13	IPU
NC_NB_CFG_14	C29	CFG14	IPU
NC_NB_CFG_15	C27	CFG15	IPU
NB_CFG<16>	A29	CFG16	IPU
NC_NB_CFG_17	J27	CFG17	IPU
TP_NB_CFG<18>	G31	CFG18	IPD
NB_CFG<19>	K30	CFG19	IPD
NB_CFG<20>	L37	CFG20	IPD

DMI

DMI_RXN0	AL45	DMI_S2N_N<0>
DMI_RXN1	AK54	DMI_S2N_N<1>
DMI_RXN2	AJ55	DMI_S2N_N<2>
DMI_RXN3	AH52	DMI_S2N_N<3>
DMI_RXP0	AM46	DMI_S2N_P<0>
DMI_RXP1	AK52	DMI_S2N_P<1>
DMI_RXP2	AJ53	DMI_S2N_P<2>
DMI_RXP3	AH50	DMI_S2N_P<3>
DMI_TXN0	AH48	DMI_N2S_N<0>
DMI_TXN1	AK48	DMI_N2S_N<1>
DMI_TXN2	AG55	DMI_N2S_N<2>
DMI_TXN3	AL53	DMI_N2S_N<3>
DMI_TXP0	AJ47	DMI_N2S_P<0>
DMI_TXP1	AK50	DMI_N2S_P<1>
DMI_TXP2	AG53	DMI_N2S_P<2>
DMI_TXP3	AL55	DMI_N2S_P<3>

PM

PM_BMBUSY_L	F44	PM_BM_BUSY*
CPU_DPRSTP_L	C41	PM_DPRSTP*
	L39	PM_EXT_TS0*
	J39	PM_EXT_TS1*
VR_PWRGOOD_DELAY	AT50	PWROK
NB_RESET_L	BB20	RSTIN*
PM_THRMTRIP_L	F28	THERMTRIP*
PM_DPRSLPVR	F40	DPRSLPVR

GRAPHICS VID

		GND
GFX_VID0	G37	GFX_VID<0>
GFX_VID1	A45	GFX_VID<1>
GFX_VID2	B42	GFX_VID<2>
GFX_VID3	D44	GFX_VID<3>
GFX_VR_EN	F42	GFX_VR_EN

ME

CL_CLK	BE52	CLINK_NB_CLK
CL_DATA	BE53	CLINK_NB_DATA
CL_PWROK	AP50	VR_PWRGOOD_DELAY
CL_RST*	BH52	CLINK_NB_RESET_L
CL_VREF	BE54	NB_CLINK_VREF

NC

NC_NB_NC_14	A52	
NC_NB_NC_13	A54	
NC_NB_NC_12	B54	
NC_NB_NC_10	BH1	
NC_NB_NC_2	BH55	
NC_NB_NC_9	BK1	
NC_NB_NC_8	BK2	NC
NC_NB_NC_4	BK54	
NC_NB_NC_1	BK55	
NC_NB_NC_7	BL2	
NC_NB_NC_6	BL4	
NC_NB_NC_5	BL52	
NC_NB_NC_3	BL54	
NC_NB_NC_11	D55	

MISC

SDVO_CTRL_CLK	K38	SDVO_CTRLCLK
SDVO_CTRL_DATA	K40	SDVO_CTRLDATA
CLKREQ*	G39	NB_CLKREQ_L
ICH_SYNC*	D40	NB_SB_SYNC_L
TEST1	F38	NB_TEST1
TEST2	K34	NB_TEST2

R1691 20K 5% 1/20W MF 201
R1690 0 5% 1/20W MF 201

PP1V25_S0

R1640 1K 1% 1/20W MF 201
C1640 0.1UF 10% 6.3V X5R 201
R1641 392 1% 1/20W MF 201

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

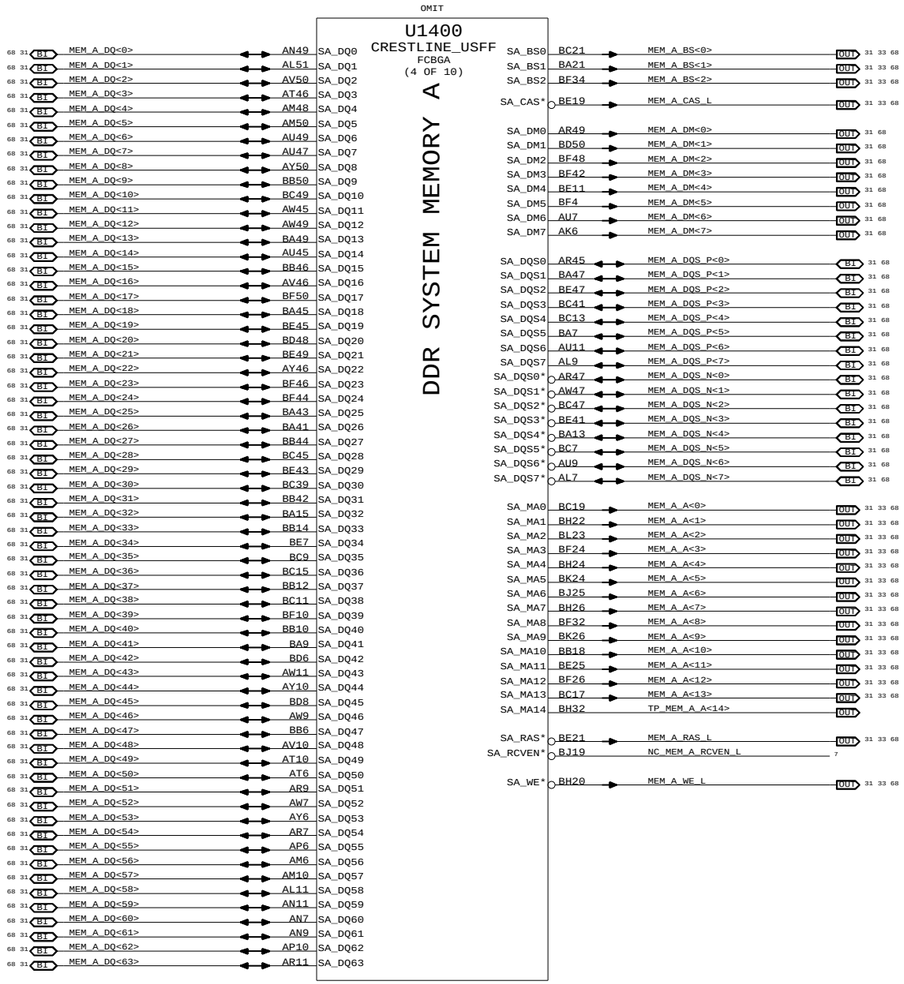
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

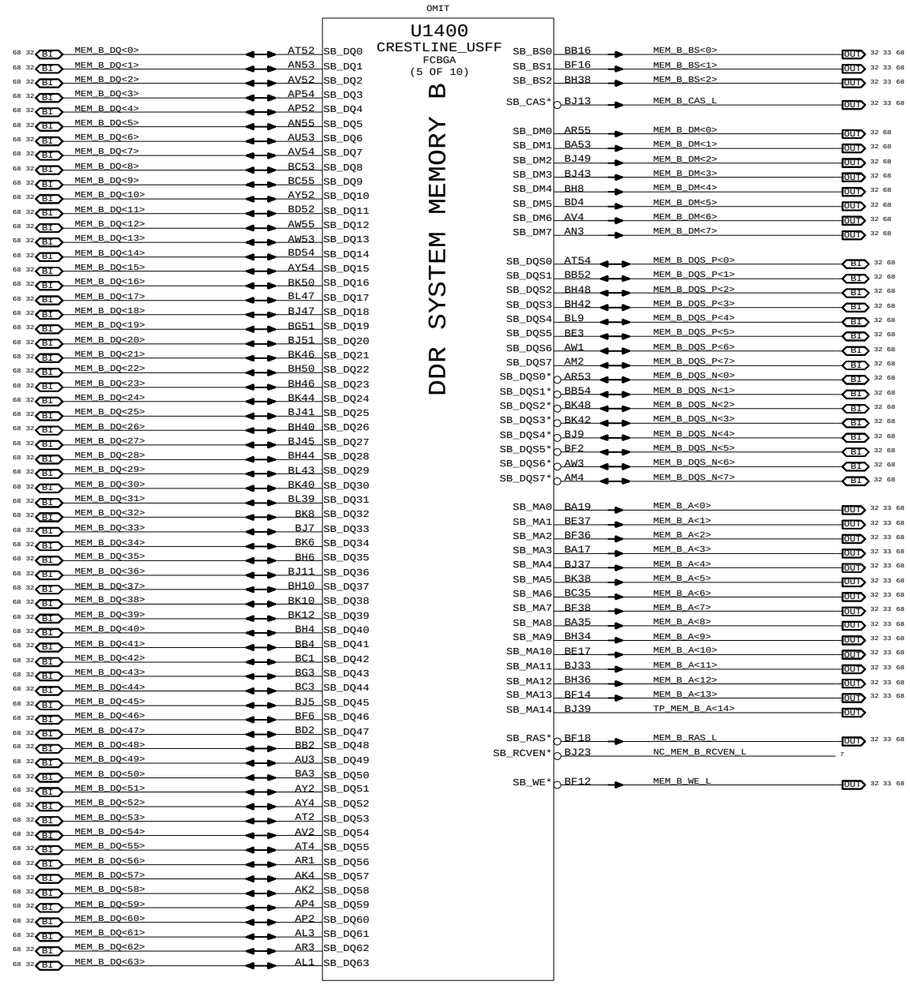
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 16 OF 73	





NB DDR2 Interfaces

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 17 OF 73	

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

PPVCORE_S0_NB_GFX

PP1V05_S0

1310 mA (Ext Graphics)
1600 mA (Int Graphics)

PP1V8_S3

3300 mA (2 ch, 667MHz)
2700 mA (2 ch, 533MHz)
1700 mA (1 ch, 667MHz)
1395 mA (1 ch, 533MHz)
5 mA (standby)

PPVCORE_S0_NB_GFX

7700 mA (Int Graphics)

PP1V05_S0

540mA

PP1V05_S0

PP1V25_S0

640mA

NB_VCCSM_LF1
NB_VCCSM_LF2
NB_VCCSM_LF3
NB_VCCSM_LF4
NB_VCCSM_LF5
NB_VCCSM_LF6
NB_VCCSM_LF7

C1807 0.1UF 10% 6.3V X5R 201
C1806 0.1UF 10% 6.3V X5R 201
C1805 0.22UF 20% 6.3V X5R 402
C1804 0.22UF 20% 6.3V X5R 402
C1803 0.47UF 10% 6.3V CERM-X5R 402
C1802 1uF OMIT 10% 6.3V CERM 402
C1801 1uF OMIT 10% 6.3V CERM 402

Current numbers from Crestline EDS, doc #21749.

NB Power 1

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

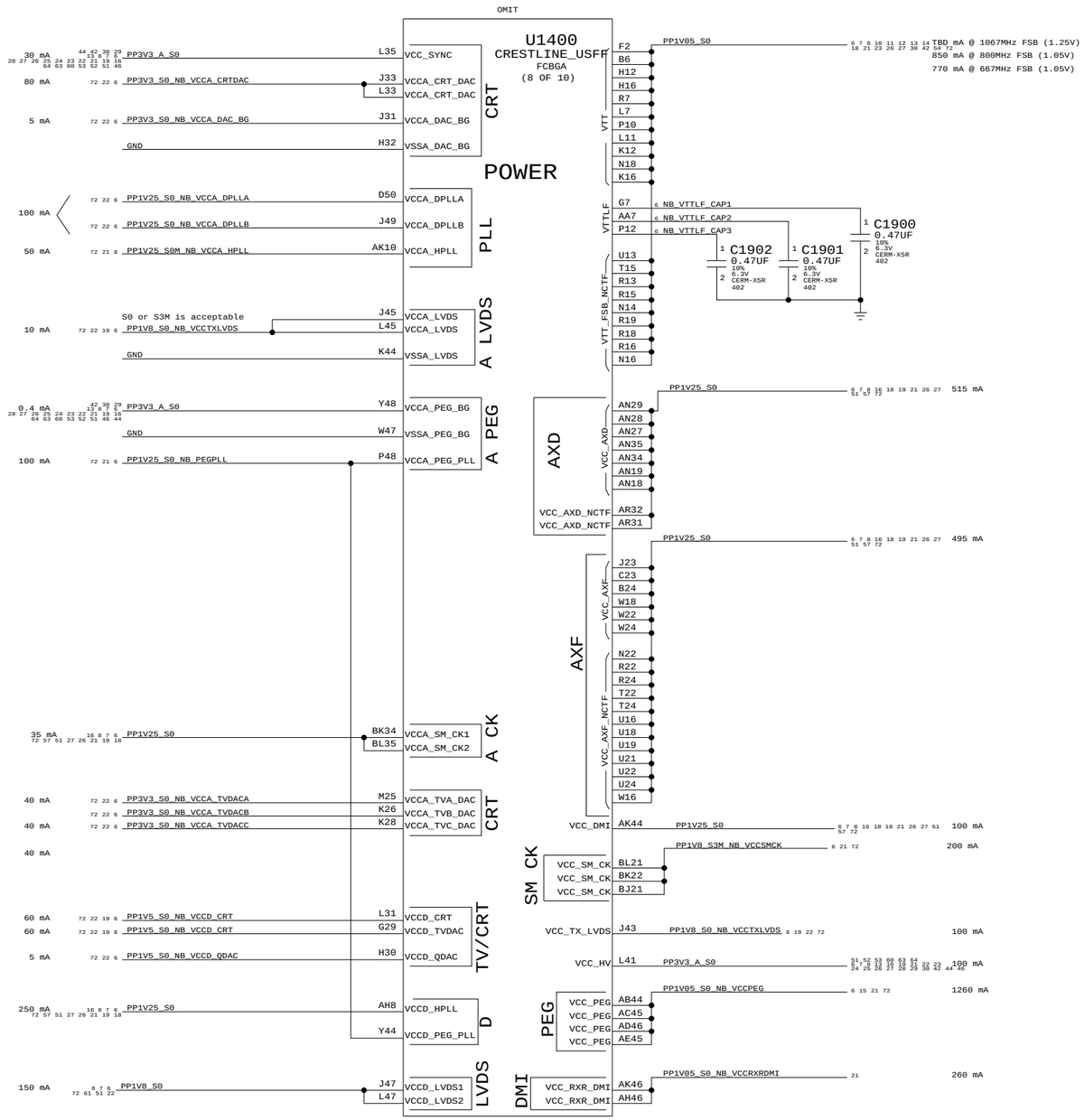
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 18 OF 73	



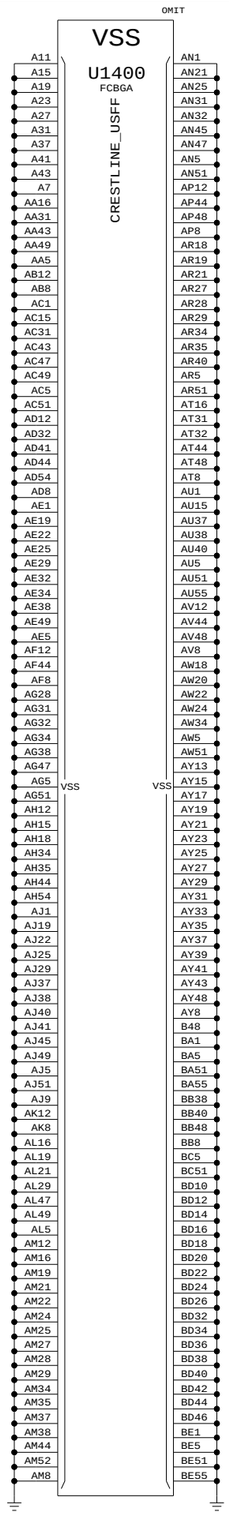
Current numbers from Crestline EDS, doc #21749.

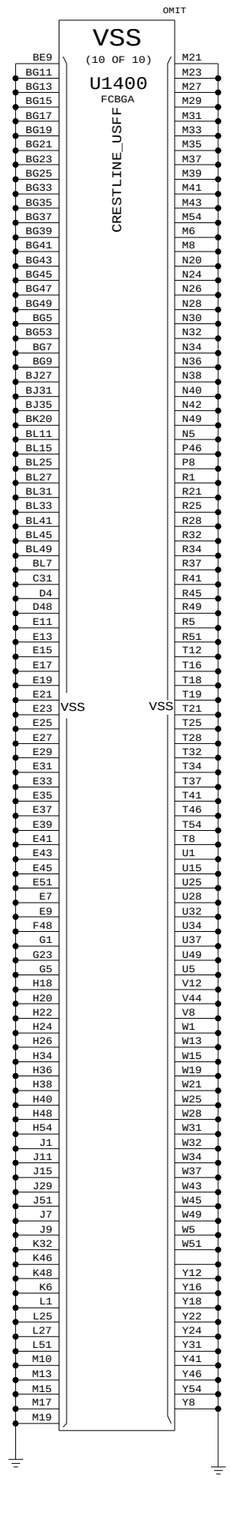
NB Power 2

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 19 OF 73	





NB Grounds

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	20	73

GMCH Core Power

PP1V05_S0

1600 mA

CRITICAL
C2100 330UF 20% 2.5V POLY CASE-C2-SM-1

C2101 22UF 20% 6.3V CERM 805

C2102 0.22uF 20% 6.3V XSR 402

C2103 0.22uF 20% 6.3V XSR 402

C2104 0.1UF 10% 6.3V XSR 201

PLACEMENT_NOTE=Place in GMCH cavity

GMCH ME Core Power

PP1V05_S0

540 mA

C2110 22UF 20% 6.3V CERM 805

C2111 0.22uF 20% 6.3V XSR 402

C2112 0.22uF 20% 6.3V XSR 402

C2113 0.1UF 10% 6.3V XSR 201

C2114 0.1UF 10% 6.3V XSR 201

C2115 0.1UF 10% 6.3V XSR 201

Place C2110-12 on edge near AH31..AM32

Place C2113-2115 close as possible to AH31..AM32

PP1V05_S0

1520 mA

Layout Note:
Place L and C
close to MCH

CRITICAL
L2173 91NH 1210

CRITICAL
C2173 220UF 20% 2.5V POLY CASE-B2-HF

Analog,I/O logic,and Term Voltage for PCI-E Graphics

PP1V05_S0_NB_VCCPEG

MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

1260 mA

C2174 22UF 20% 6.3V CERM 805

Layout Note:
22uF caps should
be close to MCH
on opposite side.
Place C2174 Near Pins AB44..AE45

GMCH FSB I/O Rail

PP1V05_S0

850 mA

C2121 4.7uF 20% 6.3V CERM 603

C2122 4.7uF 20% 6.3V CERM 603

C2123 2.2uF 20% 6.3V CERM1 603

C2124 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place C2121-24 close to U1400.F2..K16

RX and I/O Logic for DMI

PP1V05_S0_NB_VCCRXRDMI

260 mA

C2177 22UF 20% 6.3V CERM 805

Layout Note:
22uF caps should
be close to MCH
on opposite side.
Place C2177 Near Pins AH46,AK46

GMCH Memory I/O Rail

PP1V8_S3

3300 mA

CRITICAL
C2130 330UF 20% 2.0V POLY CASE-B2-HF

this is "1 of 2" 1.8V bulk decoupling caps.

C2135 0.1UF 10% 6.3V XSR 201

Place C2135 where LVDS taps from DDR2 plane.

C2132 22UF 20% 6.3V CERM 805

C2133 22UF 20% 6.3V CERM 805

PLACEMENT_NOTE=Place C2132,C2133 close to U1400.BA27..BL29

Memory I/O logic and DLL voltage.

PP1V25_S0

675 mA

CRITICAL
C2140 100UF 20% 6.3V POLY B2-HF

C2142 22UF 20% 6.3V CERM 805

C2143 4.7UF 10% 6.3V X5R-CERM 603

PP1V25_S0

640 mA

OMIT
C2144 1UF 10% 6.3V CERM 402

Layout Note:
PLACE C2143,C2144 NEAR AL18..AN38

Memory clock logic voltage.

PP1V25_S0

35 mA

C2145 22UF 20% 6.3V CERM 805

C2148 0.1UF 10% 6.3V X5R 201

Layout Note:
PLACE C2145,C2148 NEAR BL35,BK34

Memory voltage supply.

PP1V25_S0

515 mA

OMIT
C2151 1UF 10% 6.3V CERM 402

Layout Note:
PLACE C2151 NEAR AN29..AN18

I/O voltage Supply

PP1V25_S0

495 mA

PP1V25_S0

OMIT
C2170 1UF 10% 6.3V CERM 402

Layout Note:
PLACE C2170 NEAR J23..W24

PP1V25_S0

450 mA

Host PLL Digital Supply

PP1V25_S0

250 mA

C2180 0.1UF 10% 6.3V XSR 201

Layout Note:
Place C2180 Near Pin AH8

250mA,0.5ohm
L2181 120-OHM-0.3A-EMI 0402-LF

Host PLL Analog Supply

PP1V25_S0_NB_VCCA_HPLL

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

50 mA

C2181 22UF 20% 6.3V CERM 805

C2182 0.1UF 10% 6.3V XSR 201

Layout Note:
Place C2182 Near Pin AK10

250mA,0.5ohm

These supplies are still needed even using external GPU

D2186 1SS418 SOD-723

PP1V05_S0

PP3V3_S0_NBCORE_FOLLOW_R

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2186 10 1% 1/16W MF-LF 402

PP3V3_A_S0

NOTE: This follower is redundant if VCORE is always 1.05V.

Analog PLL Voltage for PCI-E GPU

PP1V25_S0

100 mA

L2190 FERR-220-OHM-2.5A 0603

PP1V25_S0_NB_PEGPLL

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

100 mA

R2190 1.1 1% 1/10W MF-LF 402

C2191 0.1UF 10% 6.3V X5R 201

C2192 0.1UF 10% 6.3V X5R 201

Layout Note:
PLACE C2191 NEAR U1400.P48
PLACE C2192 NEAR U1400.Y44

PP1V25_S0_NB_PEGPLL_RC

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

OMIT
C2190 10UF 20% 6.3V X5R 603

need to find "1uH,220mA,150mohm max"

PP1V8_S3

200 mA

L2195 1.0UH-0.23A 0603

PP1V8_S3_NB_VCCSMCK

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

200 mA

R2195 1.1 1% 1/16W MF-LF 402

C2196 22UF 20% 6.3V CERM 805

C2197 0.1UF 10% 6.3V X5R 201

Layout Note:
PLACE C2197 AND FILTER CLOSE TO BL21..BJ21

PP1V8_S3_NB_VCCSMCK_RC

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

OMIT
C2195 10UF 20% 6.3V X5R 603

PP3V3_A_S0

100 mA

PP1V25_S0

100 mA

Layout Note:
PLACE C2160 NEAR PIN AK44

C2160 0.1UF 10% 6.3V XSR 201

Layout Note:
PLACE C2161 NEAR PIN L41

C2161 0.1UF 10% 6.3V XSR 201

PP3V3_A_S0

5 mA

C2165 0.1UF 10% 6.3V XSR 201

Layout Note:
PLACE C2165 BETWEEN Y48,W47

GND

Layout Note: Route to caps, then GND

PP1V8_S3

NB_VTTREF_DIV
R2112 1K 1% 1/20W MF 201

PP0V9_S3M_MEM_NBVREFA

NB_VTTREF_DIV
R2113 1K 1% 1/20W MF 201

Layout Note:
PLACE NEAR NB

PP1V8_S3

NB_VTTREF_DIV
R2110 1K 1% 1/20W MF 201

PP0V9_S3M_MEM_NBVREFB

NB_VTTREF_DIV
R2111 1K 1% 1/20W MF 201

Current numbers from Crestline EDS Addendum, doc .....

NB Standard Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 21 OF 73	

NOTE: This filter is required even if using only external graphics.

VCCD_TVDAC also powers internal thermal sensors.

PP1V5_S0 — 125 mA

CRITICAL C2201 22000pF-1000mA 16V NFM18

C2202 0.01UF 10% 10V X5R 201

C2200 0.1UF 10% 6.3V X5R 201

PP1V5_S0_NB_VCCD_CRT — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V — 60 mA

PP1V5_S0_NB_VCCD_CRT — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V — 60 mA

PP1V5_S0_NB_VCCD_CRT — MAKE_BASE=TRUE

R2205 100 1% 1/10W MF-LF 402

PP1V5_S0_NB_QDAC — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V

CRITICAL C2206 22000pF-1000mA 16V NFM18

PP1V5_S0_NB_VCCD_QDAC — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V — 500 uA

C2205 0.01UF 10% 10V X5R 201

C2207 0.1UF 10% 6.3V X5R 201

C2208 1UF 10% 10V X5R 402-1

Filtering changed per SR MOW # 541194

Layout Note: These 4 caps should be within 6.35 mm of NB edge

PP5V_S0 — 205 mA

R2281 0 5% 1/20W MF 201

OMIT C2280 1UF 10% 6.3V CERM 402

NO STUFF C2281 1UF 10% 6.3V CERM 402

P3V3TVDAC_EN_RC

U2280 TPS79933 SON — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=3.3V

IN, OUT, EN, NR, NC, GND, THRML PAD

PP3V3_S0_NB_TVDAC — 205 mA

P3V3TVDAC_NOISE

C2282 0.01UF 10% 10V X5R 201

OMIT C2285 10UF 20% 6.3V X5R 603

CRITICAL L2288 180-OHM-1.5A 0603

PP3V3_S0_NB_CRTDAC_F — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 80 mA

CRITICAL C2289 22000pF-1000mA 16V NFM18

C2295 0.01UF 10% 10V X5R 201

C2288 0.1UF 10% 6.3V X5R 201

PP3V3_S0_NB_VCCA_CRTDAC — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 80 mA

Layout Note: These 2 caps should be within 6.35 mm of NB edge

NO STUFF D2285 1SS418 SOD-723

PP1V5_S0

PP3V3_S0_NB_TVDAC_FOLLOW — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V

NO STUFF R2285 10 1% 1/10W MF-LF 402

CRITICAL L2290 180-OHM-1.5A 0603

PP3V3_S0_NB_TVDAC_F — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 125 mA

CRITICAL C2292 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_TVDACA — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 40 mA

C2293 0.01UF 10% 10V X5R 201

C2291 0.1UF 10% 6.3V X5R 201

CRITICAL C2294 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_TVDACB — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 40 mA

Layout Note: These 11 caps should be within 6.35 mm of NB edge

CRITICAL C2296 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_TVDACC — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 40 mA

GMCH Graphics Core Power

PPVCORE_S0_NB_GFX — 7700 mA

CRITICAL C2210 330UF 20% 2.5V POLY CASE-C2-SM-1

OMIT C2219 10uF 20% 6.3V X5R 603

OMIT C2231 10uF 20% 6.3V X5R 603

OMIT C2232 10uF 20% 6.3V X5R 603

OMIT C2240 2.2UF 20% 6.3V CERM 402-LF

OMIT C2241 2.2UF 20% 6.3V CERM 402-LF

OMIT C2242 2.2UF 20% 6.3V CERM 402-LF

OMIT C2243 2.2UF 20% 6.3V CERM 402-LF

OMIT C2213 10uF 20% 6.3V X5R 603

OMIT C2214 2.2UF 20% 6.3V CERM 402-LF

OMIT C2215 2.2UF 20% 6.3V CERM 402-LF

C2216 0.47UF 10% 6.3V CERM-X5R 402

C2217 0.1UF 10% 6.3V X5R 201

C2218 0.1UF 10% 6.3V X5R 201

PLACEMENT_NOTE=Place in GMCH cavity Place smaller caps as close as possible to NB pins.

NEED TO FIND A "1#GH, 500MA, 78MOHM" INDUCTOR

L2220 1.0UH-0.5A-0.675A 1007

PP1V8_S0 — 260 mA

CRITICAL C2220 220UF 20% 2.5V POLY CASE-B2-SM-HF

C2221 1000PF 10% 16V X7R 201

PP1V8_S0_NB_VCCTXLVDS — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.8V — 110 mA

C2223 1000PF 10% 16V X7R 201 — Place C2221,C2223 close between J45,L45,J43 and K44

GND — Layout Note: Route to cap, then GND

PP1V8_S0 — 150 mA

C2226 22UF 20% 6.3V CERM 805 — Place C2226 close to Pins J47, L47

CRITICAL C2298 22000pF-1000mA 16V NFM18

PP3V3_S0_NB_VCCA_DAC_BG — MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V — 5 mA

C2299 0.01UF 10% 10V X5R 201

C2297 0.1UF 10% 6.3V X5R 201

GND — Layout Note: Route to caps, then GND

PP3V3_A_S0

R2242 22K 5% 1/20W MF 201 — NO STUFF

R2243 22K 5% 1/20W MF 201 — NO STUFF

R2244 22K 5% 1/20W MF 201 — NO STUFF

R2245 22K 5% 1/20W MF 201

GFX_VID<0> OUT

GFX_VID<1> OUT

GFX_VID<2> OUT

GFX_VID<3> OUT

R2247 22K 5% 1/20W MF 201

R2248 22K 5% 1/20W MF 201

R2249 22K 5% 1/20W MF 201

R2250 22K 5% 1/20W MF 201 — NO STUFF

PP3V3_A_S0 — 10 mA

C2230 0.1UF 10% 6.3V X5R 201 — Place C2230 close to Pin L35

WARNING VOLTAGE DROP

PP1V8_S0 — (1.7V - 5.5V) 80 mA

CRITICAL U2265 TPS731125 SOT23-5

Vout = 1.204V * (Ra + Rb)/Rb

Ra || Rb should be 19Kohms

IN, EN, GND, OUT, NR/FB

OMIT C2265 1UF 10% 6.3V CERM 402

PP1V25_S0_NB_DPLL — MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V

P1V25S0NBDPLL_FB

OMIT C2266 10UF 20% 6.3V X5R 603

P1V25S0NBDPLL_RF

C2267 0.01UF 10% 10V X5R 201

R2266 0.300 5% 1/10W FF 603

80 mA

R2261 0 5% 1/16W MF-LF 402

PP1V25_S0_NB_VCCA_DPLLA — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V

C2261 0.1UF 10% 6.3V X5R 201 — Place C2261 close to Pin D50

R2262 0 5% 1/16W MF-LF 402

PP1V25_S0_NB_VCCA_DPLLB — MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.25V

OMIT C2260 10uF 20% 6.3V X5R 603

C2262 0.1UF 10% 6.3V X5R 201 — Place C2262 close to Pin J49

80 mA

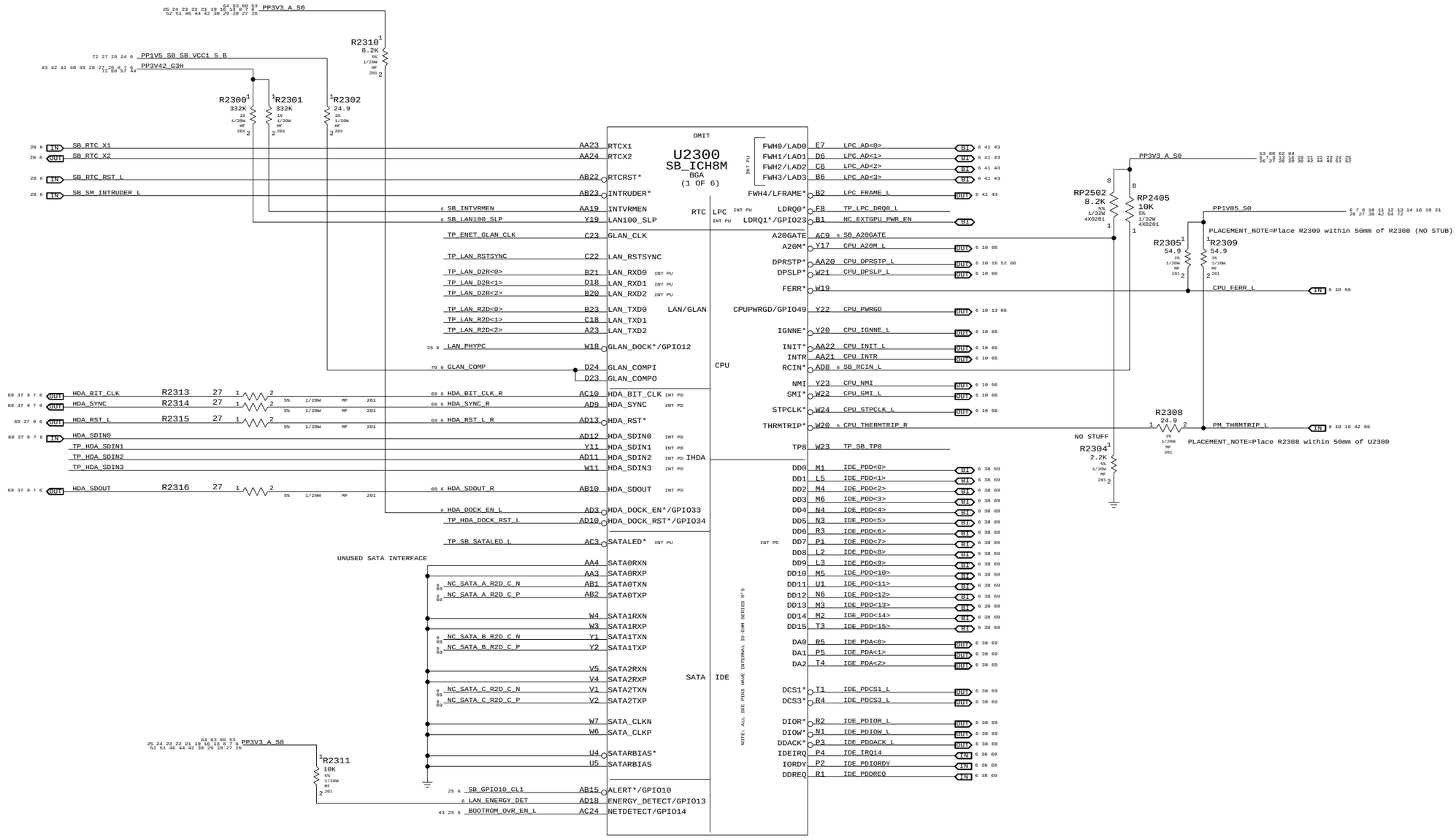
Current numbers from Crestline EDS Addendum, doc #20127.

NB Graphics Decoupling

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 22 OF 73	



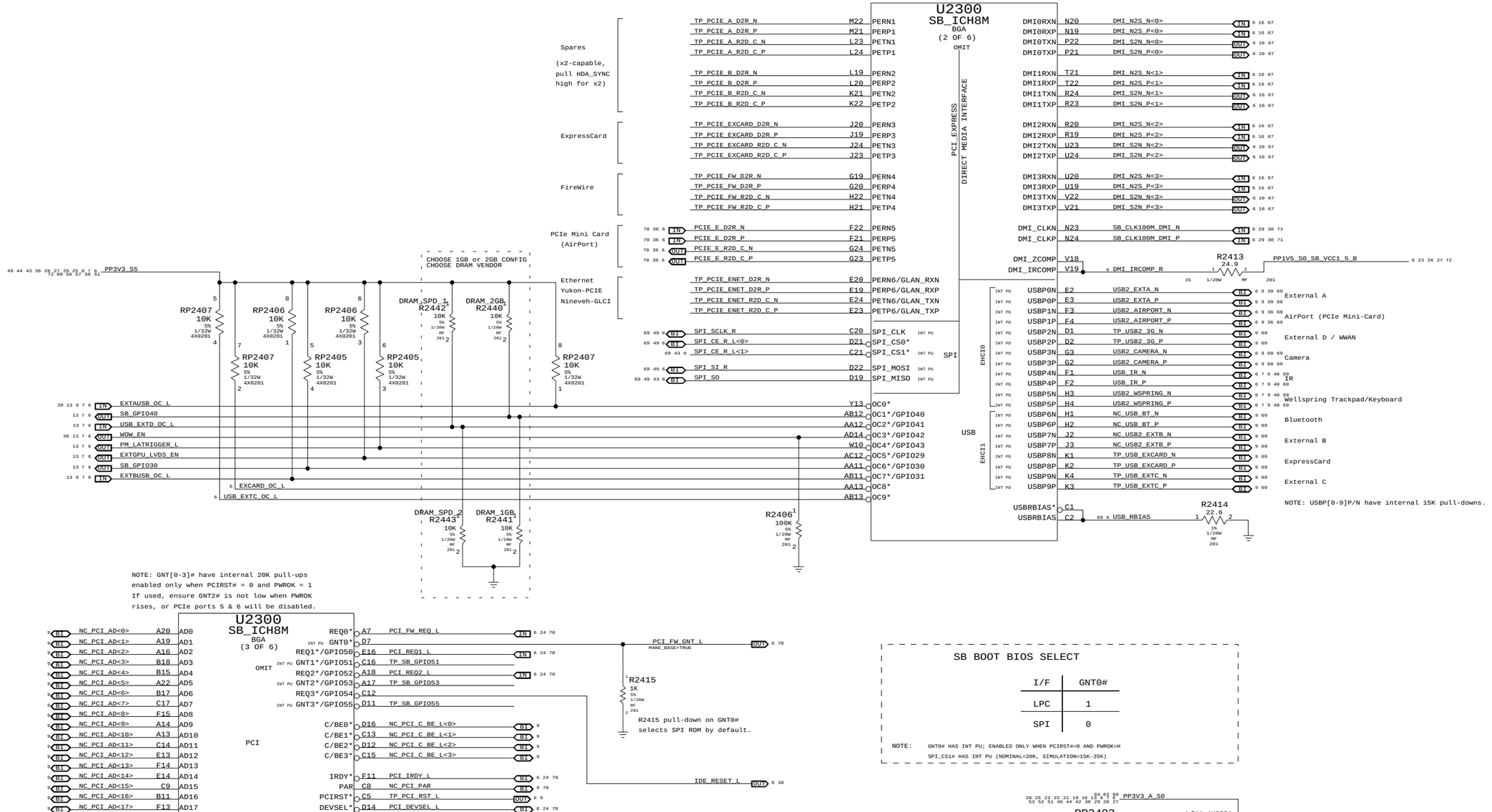
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

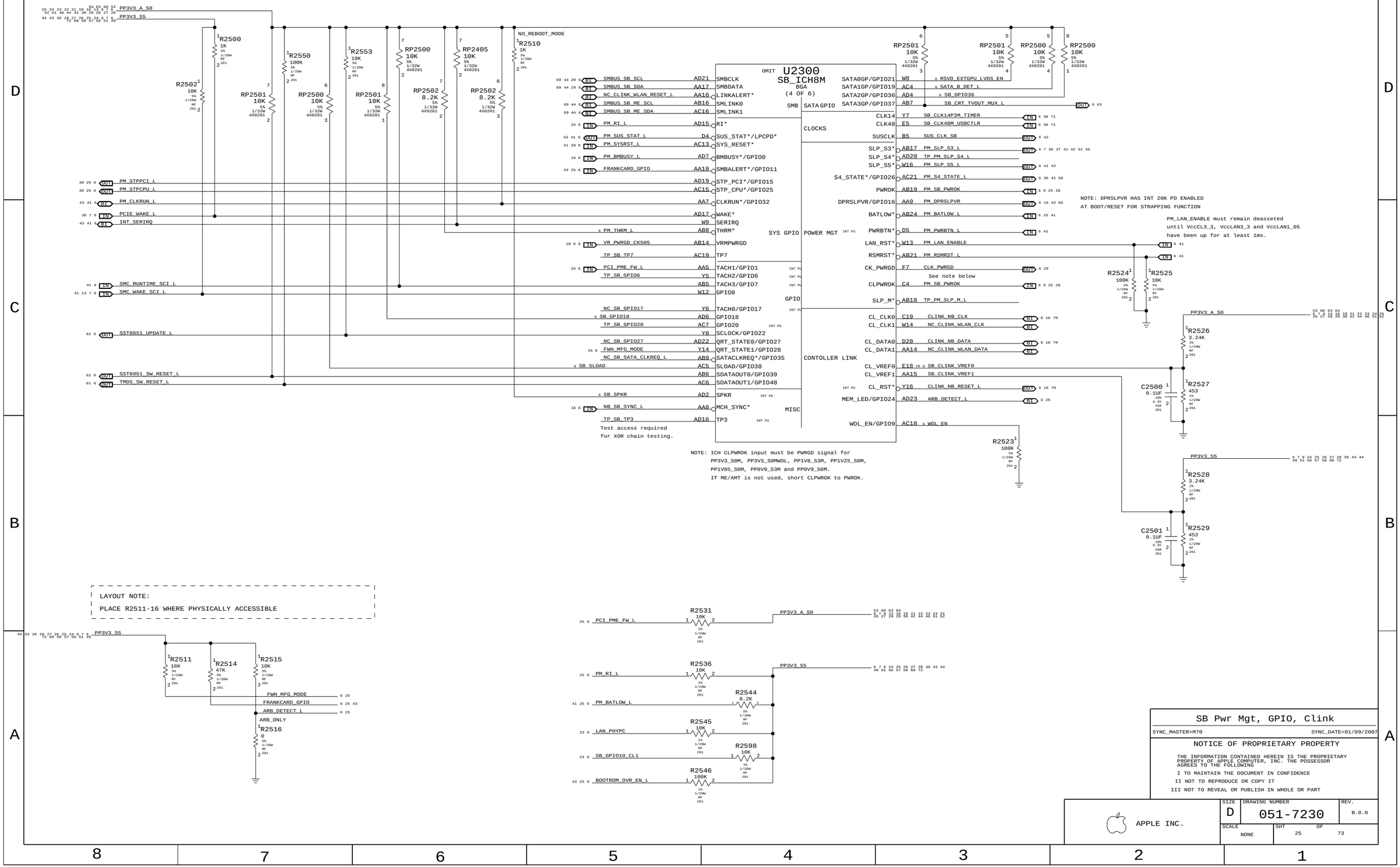
SB Enet, Disk, FSB, LPC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 23 OF 73	


U2300
SB_ICH8M
BGA
(2 OF 6)
OMIT
PCI_EXPRESS
DIRECT MEDIA INTERFACE
SPI
USB
EHCI0
EHCI1
Spares
(x2-capable, pull HDA_SYNC high for x2)
ExpressCard
FireWire
PCIe Mini Card (AirPort)
Ethernet Yukon-PCIE Nineveh-GLCI
CHOOSE 1GB or 2GB CONFIG
CHOOSE DRAM VENDOR
PP3V3_S5
RP2407 10K
RP2406 10K
RP2405 10K
DRAM_SPD_1 R2442 10K
DRAM_2GB R2440 10K
DRAM_SPD_2 R2443 10K
DRAM_1GB R2441 10K
R2406 100K
EXTAUSB_OC_L
SB_GPIO40
USB_EXTD_OC_L
WOW_EN
PM_LATRIGGER_L
EXTGPU_LVDS_EN
SB_GPIO30
EXTBUSB_OC_L
EXCARD_OC_L
USB_EXTC_OC_L
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1
If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.
INTERRUPT I/F
PCI
PCI_FW_GNT_L
R2415 1K
R2415 pull-down on GNT0# selects SPI ROM by default.
IDE_RESET_L
Provide a pull-down on this GPIO if not used.
R2413 24.9
R2414 22.6
PP1V5_S0_SB_VCC1_5_B
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
USBRBIAS
USBRBIAS*
USB_RBIAS
External A
AirPort (PCIe Mini-Card)
External D / WWAN
Camera
IR
Wellspring Trackpad/Keyboard
Bluetooth
External B
ExpressCard
External C
NOTE: USBP[0-9]P/N have internal 15K pull-downs.
SB BOOT BIOS SELECT
I/F | GNT0#
LPC | 1
SPI | 0
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
PP3V3_A_S0
RP2403 10K
RP2402 10K
RP2400 10K
RP2401 10K
R2431 10K
R2433 10K
Changed pullups from 8.2K to 10K, since not critical.
SB PCI, PCIe, DMI, USB
SYNC_MASTER=M70
SYNC_DATE=01/09/2007
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7230
REV. B.0.0
SCALE NONE
SHT 24 OF 73

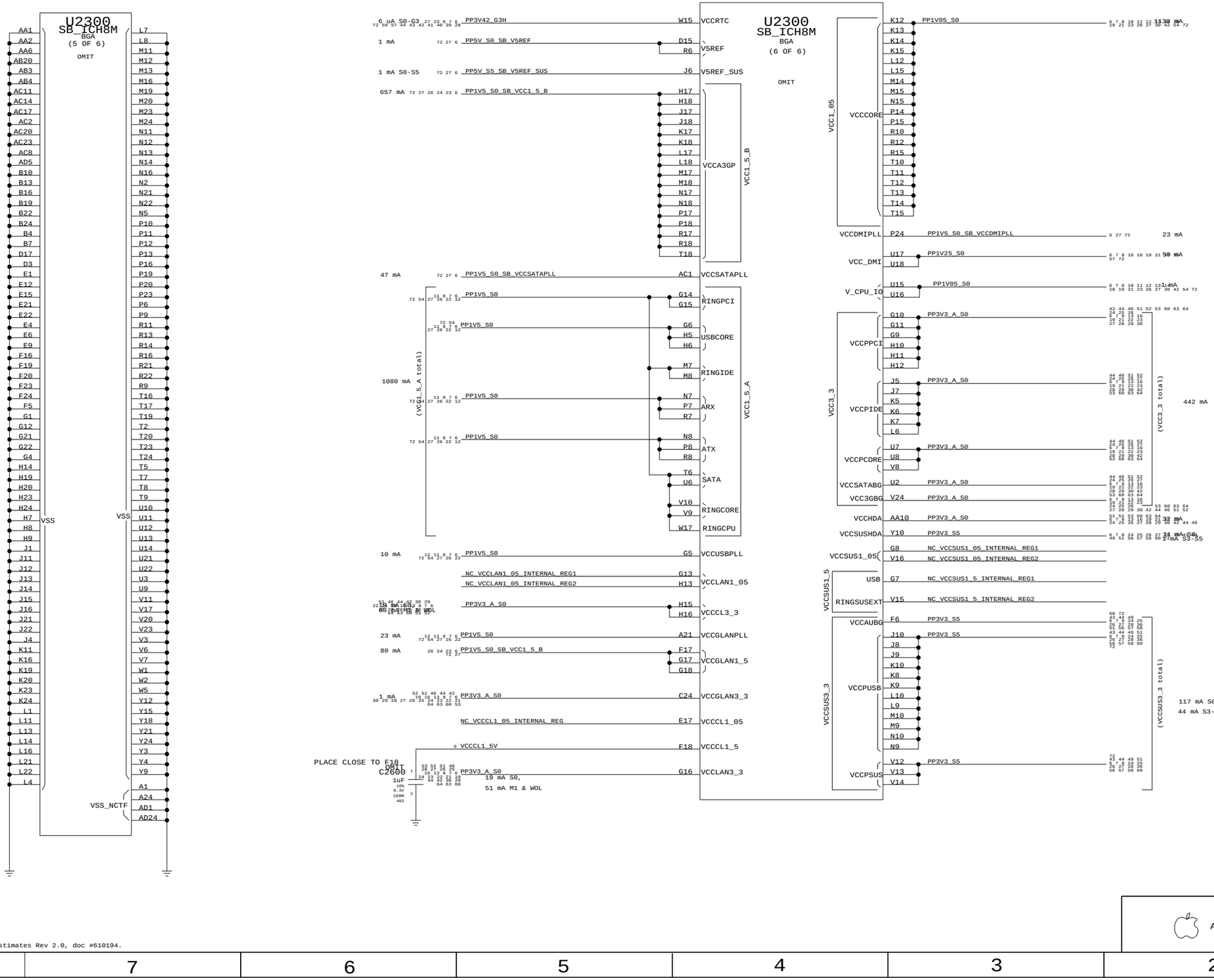


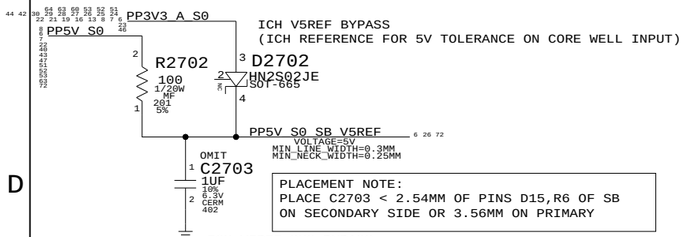
SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

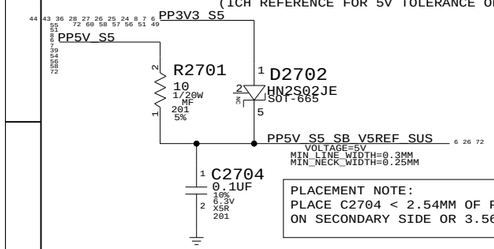
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 25 OF 73	


U2300
SB_ICH8M
BGA
(5 OF 6)
OMIT
VSS
VSS_NCTF
U2300
SB_ICH8M
BGA
(6 OF 6)
OMIT
6 uA S0-G3
PP3V42_G3H
W15 VCCRTC
1 mA
PP5V_S0_SB_V5REF
D15 V5REF
R6
1 mA S0-S5
PP5V_S5_SB_V5REF_SUS
J6 V5REF_SUS
657 mA
PP1V5_S0_SB_VCC1_5_B
H17
H18
J17
J18
K17
K18
L17
L18
M17
M18
N17
N18
P17
P18
R17
R18
T18
VCCA3GP
VCC1_5_B
47 mA
PP1V5_S0_SB_VCCSATAPLL
AC1 VCCSATAPLL
PP1V5_S0
G14 RINGPCI
G15
PP1V5_S0
G6
H5 USBCORE
H6
M7
M8 RINGIDE
1080 mA
(VCC1_5_A total)
PP1V5_S0
N7
P7 ARX
R7
PP1V5_S0
N8
P8 ATX
R8
T6
U6 SATA
V10
V9 RINGCORE
W17 RINGCPU
VCC1_5_A
10 mA
PP1V5_S0
G5 VCCUSBPLL
NC_VCCLAN1_05_INTERNAL_REG1
G13
NC_VCCLAN1_05_INTERNAL_REG2
H13 VCCLAN1_05
PP3V3_A_S0
H15
H16 VCCCL3_3
23 mA
PP1V5_S0
A21 VCCGLANPLL
80 mA
PP1V5_S0_SB_VCC1_5_B
F17
G17
G18 VCCGLAN1_5
1 mA
PP3V3_A_S0
C24 VCCGLAN3_3
NC_VCCCL1_05_INTERNAL_REG
E17 VCCCL1_05
VCCCL1_5V
F18 VCCCL1_5
PLACE CLOSE TO E18
PP3V3_A_S0
G16 VCCLAN3_3
19 mA S0,
51 mA M1 & WOL
C2600
1uF
10%
6.3V
CERM
402
VCC1_05
VCCCORE
K12
K13
K14
K15
L12
L15
M14
M15
N15
P14
P15
R10
R12
R15
T10
T11
T12
T13
T14
T15
PP1V05_S0
1130 mA
VCCDMIPLL
P24
PP1V5_S0_SB_VCCDMIPLL
23 mA
VCC_DMI
U17
U18
PP1V25_S0
50 mA
V_CPU_IO
U15
U16
PP1V05_S0
1 mA
VCC3_3
VCCPPCI
G10
G11
G9
H10
H11
H12
PP3V3_A_S0
VCCPIDE
J5
J7
K5
K6
K7
L6
PP3V3_A_S0
VCCPCORE
U7
U8
V8
PP3V3_A_S0
VCCSATABG
U2
PP3V3_A_S0
VCC3GBG
V24
PP3V3_A_S0
VCCHDA
AA10
PP3V3_A_S0
VCCSUSHDA
Y10
PP3V3_S5
14 mA S0,
7 mA S3-S5
VCCSUS1_05
G8
NC_VCCSUS1_05_INTERNAL_REG1
V16
NC_VCCSUS1_05_INTERNAL_REG2
VCCSUS1_5
USB
G7
NC_VCCSUS1_5_INTERNAL_REG1
RINGSUSEXT
V15
NC_VCCSUS1_5_INTERNAL_REG2
VCCAUBG
F6
PP3V3_S5
VCCSUS3_3
VCCPUSB
J10
J8
J9
K10
K8
K9
L10
L9
M10
M9
N10
N9
PP3V3_S5
VCCPSUS
V12
V13
V14
PP3V3_S5
(VCCSUS3_3 total)
117 mA S0,
44 mA S3-S5
(VCC3_3 total)
442 mA
NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V
depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.
Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.
SB Power & Ground
SYNC_MASTER=M70
SYNC_DATE=01/09/2007
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE
D
DRAWING NUMBER
051-7230
REV.
B.0.0
SCALE
NONE
SHT
26
OF
73



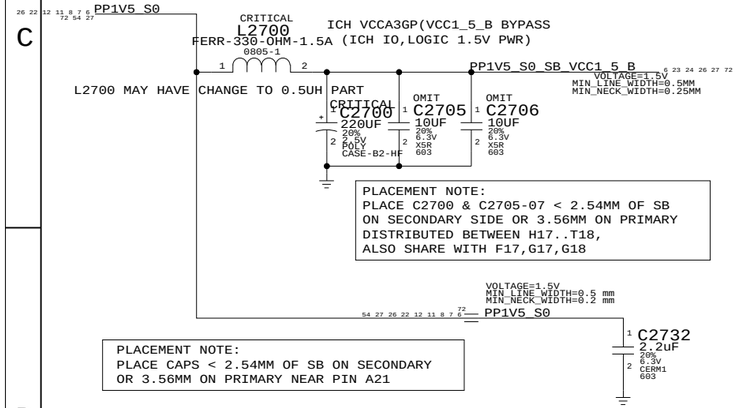
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)

PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PINS D15,R6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY



ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)

PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN J6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

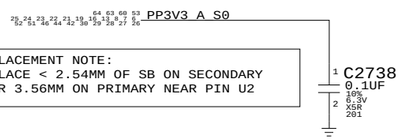


ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)

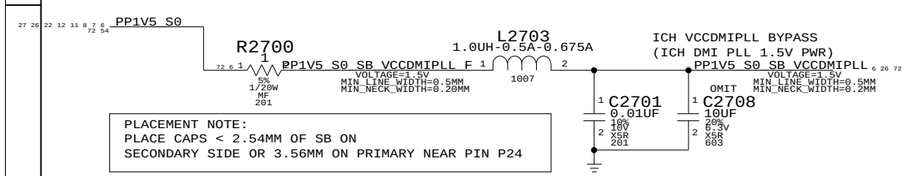
L2700 MAY HAVE CHANGE TO 0.5UH PART

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN H17..T18,
ALSO SHARE WITH F17,G17,G18

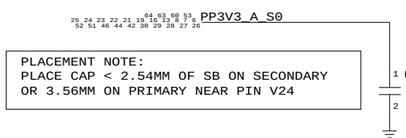
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A21



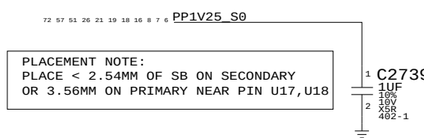
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN U2



PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY NEAR PIN P24

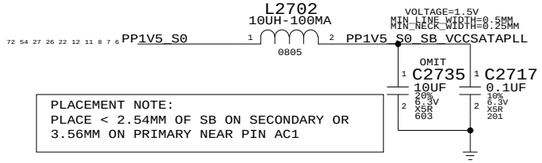


PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN V24



PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN U17,U18

L2702 MAY HAVE CHANGE TO 1.0UH PART

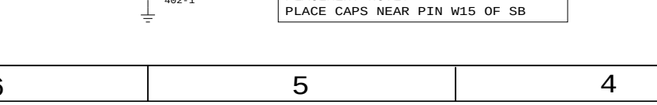


PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
VCCPCORE DOES NOT REQUIRE DECOUPLING PER INTEL RECOMMENDATIONS

COMBINED VCC1_5_A, ARX AND ATX DECOUPLING PER INTEL RECOMMENDATIONS
ICH VCC1_5A/ARX/ATX BYPASS
(ICH LOGIC&IO/[ARX]/[ATX] 1.5V PWR)

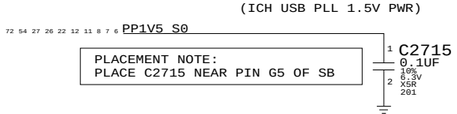
PLACEMENT NOTE:
PLACE CAP NEAR PINS
T6..U6, N7..R7, N8..R8 OF SB



ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)

PLACEMENT NOTE:
PLACE CAPS NEAR PIN W15 OF SB

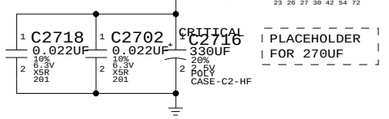
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)



PLACEMENT NOTE:
PLACE C2715 NEAR PIN G5 OF SB

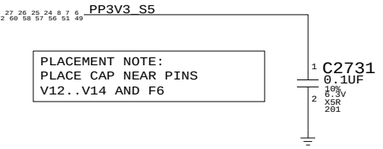
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
PLACE C2718,C2702 NEAR SB K12..T15

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)



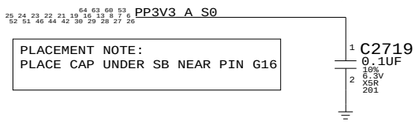
PLACEHOLDER
FOR 270UF

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)



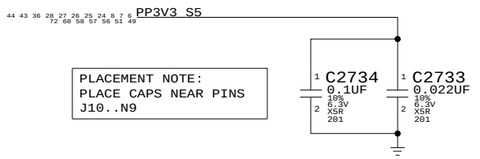
PLACEMENT NOTE:
PLACE CAP NEAR PINS
V12..V14 AND F6

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)



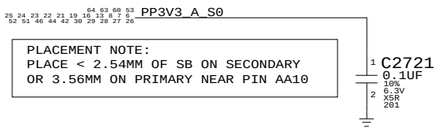
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PIN G16

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)



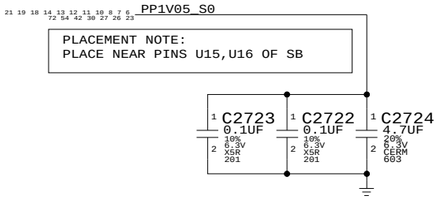
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
J10..N9

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)



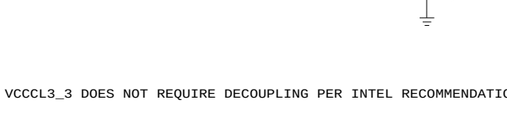
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AA10

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)



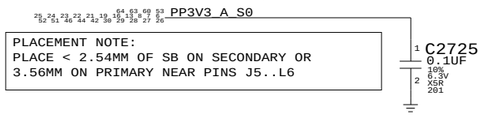
PLACEMENT NOTE:
PLACE NEAR PINS U15,U16 OF SB

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)



PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS G6..H6

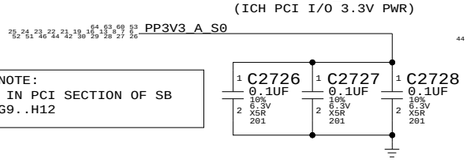
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)



PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS J5..L6

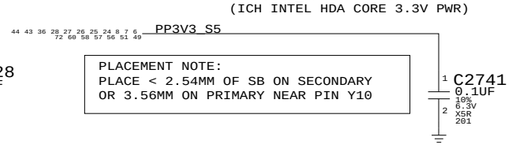
VCCCL3_3 DOES NOT REQUIRE DECOUPLING PER INTEL RECOMMENDATIONS

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)



PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS G9..H12

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)



PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN Y10

PP1V5_S0_SB_VCC1_5_B — PP1V5_S0_SB_VCC1_5_B
MAKE_BASE=TRUE

SB Decoupling

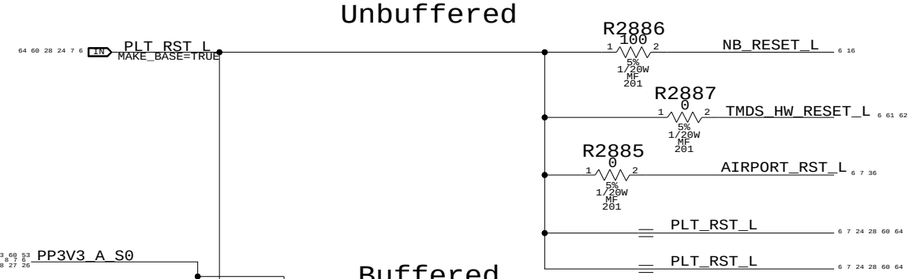
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

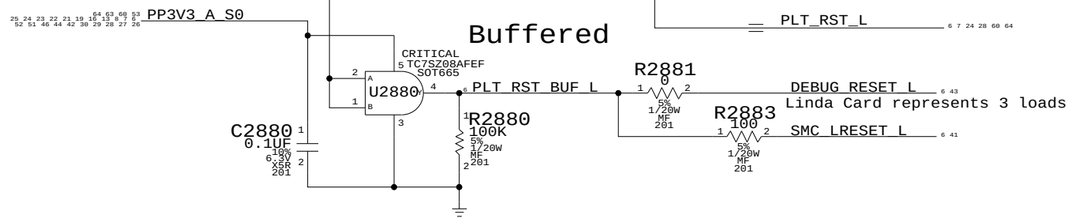
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 27 OF 73	

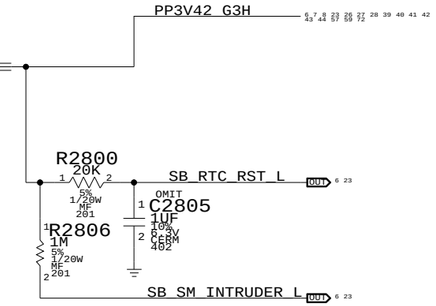
Platform Reset Connections

Unbuffered

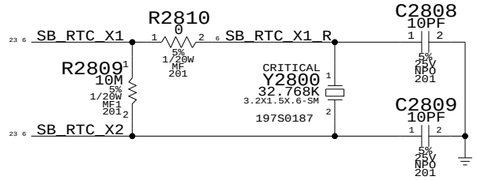


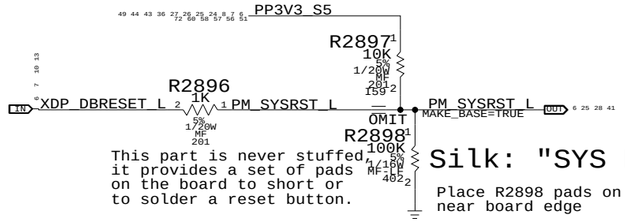
Buffered





SB RTC Crystal Circuit

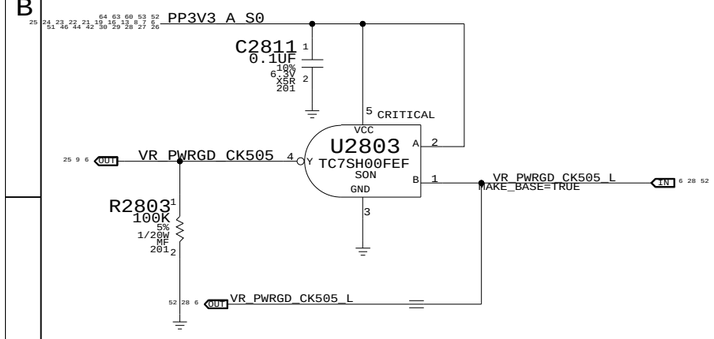


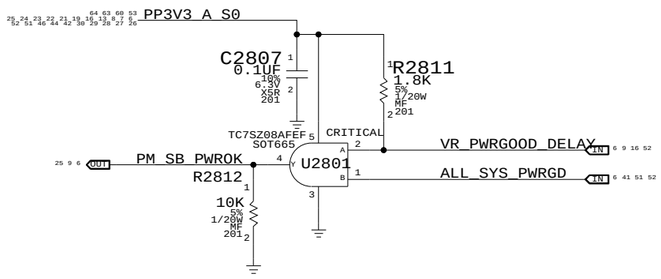


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

Place R2898 pads on bottom side near board edge





SB Misc

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 28 OF 73	

Silego recommend to remove L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

PP3V3_A_S0

CRITICAL
L2901
FERR-120-OHM-1.5A
0402-LF
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

PP3V3_S0_CK505_VDD_CPU_SRC

OMIT C2900 1UF 10% 6.3V CERM 402
OMIT C2901 10UF 20% 6.3V X5R 603
C2902 0.1UF 10% 6.3V X5R 201
C2903 0.1UF 10% 6.3V X5R 201
C2904 0.1UF 10% 6.3V X5R 201
C2905 0.1UF 10% 6.3V X5R 201
C2906 0.1UF 10% 6.3V X5R 201
C2908 0.1UF 10% 6.3V X5R 201
C2909 0.1UF 10% 6.3V X5R 201
C2912 0.1UF 10% 6.3V X5R 201
C2913 0.1UF 10% 6.3V X5R 201
C2915 0.1UF 10% 6.3V X5R 201

CRITICAL
Y2901
SM-2.5X2.0MM
14.318MHZ-35PPF-20PF
C2989 20PF 5% 25V NP0-C0G 201
C2990 20PF 5% 25V NP0-C0G 201

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

U2900
SLG2AP101
QFN

3	VDD_48			
43	VDD_CPU			
61	VDD_PCI			
67	VDD_REF			
49				
12				
17				
28				
35	VDD_SRC			
38	VDD_A			
39	VSS_A			
51	XTAL_IN	CK505_XTAL_IN		
50	XTAL_OUT	CK505_XTAL_OUT		
8	FS_B/TEST_MODE	CK505_FSB_TEST_MODE	IN	
57	PCI_1	NC_CK505_PCI1_CLK	OUT	(FW PCI 33MHZ)
58	PCI_2	NC_CK505_PCI2_CLK	OUT	(TPM LPC 33MHZ)
63	PCI_3	CK505_PCI3_CLK	OUT	(SMC LPC 33MHZ)
64	PCI_4	NC_CK505_PCI4_CLK	OUT	(PCI SLOT)
65	PCI_5/FCI_SEL	CK505_PCI5_FCTSEL1	BI	(PORT80 LPC 33MHZ)
68	PCIF_0/ITP_EN	CK505_PCIF0_CLK	OUT	(NO INT PD) (INT PU)
1	PCIF_1	CK505_PCIF1_CLK	OUT	(ICH8M PCI 33MHZ) (NO INT PU)
47	SCL	SMBUS_SB_SCL	IN	(ICH SM BUS)
48	SDA	SMBUS_SB_SDA	BI	
5	VSS_48			
46	VSS_CPU			
62				
66	VSS_PCI			
52	VSS_REF			
31	VSS_SRC			
69	THRM_PAD			

PCI_STOP*	56	PM_STPPCI_L	IN		(FROM ICH8M GPIO15 STPPCI*)
CPU_STOP*	55	PM_STPCPU_L	IN		(FROM ICH8M GPIO25 STPCPU*)
CPU_0*	44	FSB_CLK_CPU_N	OUT		(CPU HOST 133/167MHZ)
CPU_0	45	FSB_CLK_CPU_P	OUT		
CPU_1_MCH*	41	FSB_CLK_NB_N	OUT		(GMCH HOST 133/167MHZ)
CPU_1_MCH	42	FSB_CLK_NB_P	OUT		
CPU_ITP*/SRC_10*	36	XDP_CLK_N	OUT		(ITP HOST 133/167MHZ)
CPU_ITP/SRC_10	37	XDP_CLK_P	OUT		
SRC_0*/LCD_CLK*	11	NB_CLK100M_DPLLSS_N	OUT		(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
SRC_0/LCD_CLK	10	NB_CLK100M_DPLLSS_P	OUT		
SRC_1*	14	NC_CK505_SRC1_N	OUT		(SLOT F - GPU PCI-E 100 MHZ)
SRC_1	13	NC_CK505_SRC1_P	OUT		
CLKREQ_1*	9	NC_CK505_SRC_CLKREQ1_L	IN		
SRC_2*	16	SB_CLK100M_DMI_N	OUT		(ICH8M DMI 100 MHZ)
SRC_2	15	SB_CLK100M_DMI_P	OUT		
SRC_3*	19	NC_CK505_SRC3_N	OUT		(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
SRC_3	18	NC_CK505_SRC3_P	OUT		
CLKREQ_3*	59	NC_CK505_SRC_CLKREQ3_L	IN		
SRC_4*	22	NC_CK505_SRC4_N	OUT		(ICH SATA 100 MHZ) (FROM ICH8M GPIO35)
SRC_4	21	NC_CK505_SRC4_P	OUT		
CLKREQ_4*	20	NC_CK505_SRC_CLKREQ4_L	IN		
SRC_5*	24	NB_CLK100M_PCIE_N	OUT		(GMCH G_CLKIN 100 MHZ) (FROM GMCH CLK_REQ*)
SRC_5	23	NB_CLK100M_PCIE_P	OUT		
CLKREQ_5*	60	NB_CLKREQ_L	IN		
SRC_6*	27	PCIE_CLK100M_MINI_N	OUT		(WIRELESS PCI-E 100 MHZ)
SRC_6	26	PCIE_CLK100M_MINI_P	OUT		
CLKREQ_6*	25	CK505_SRC_CLKREQ6_L	IN		
SRC_7*	30	NC_CK505_SRC7_N	OUT		(DB400 SRC)
SRC_7	29	NC_CK505_SRC7_P	OUT		
CLKREQ_7*	40	NC_CK505_PGMODE			
SRC_8*	32	NC_CK505_SRC8_N	OUT		(SLOT E)
SRC_8	33	NC_CK505_SRC8_P	OUT		
CLKREQ_8*	34	NC_CK505_SRC_CLKREQ8_L	IN		
DOT_96*/27M_SS	7	NB_CLK96M_DOT_N	OUT		(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
DOT_96/27M	6	NB_CLK96M_DOT_P	OUT		
CKPWRGD/PD*	2	CLK_PWRGD	IN		(INT PD)
48M/FS_A	4	CK505_USB48_FSA	OUT		(FROM ICH8M)
REF_0/FS_C/TEST_SEL	54	CK505_CLK14P3M_TIMER	OUT		(ICH8M USB 48MHZ)
GPU_STOP*	53	NC_GPU_STOP_L	BI		(ICH8M,SIO,LPC REF. 14.318MHZ)

R2903 10K 5% 1/20W MF 201

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)

FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM

Clock (CK505)

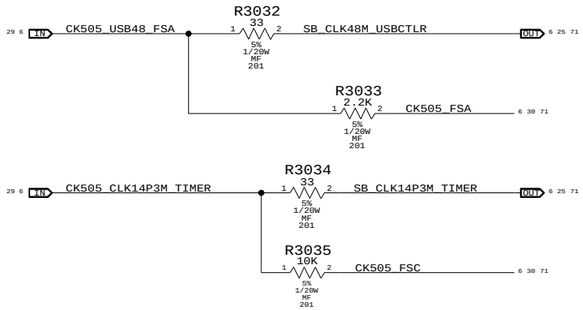
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

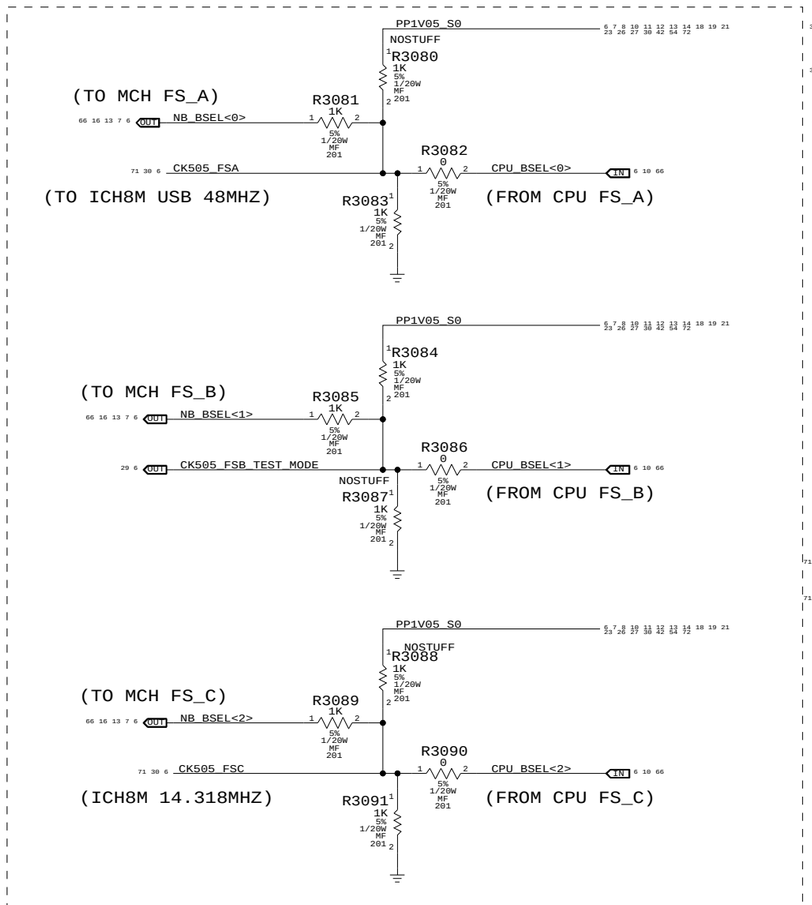
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE NONE SHT 29 OF 73

CLK Termination

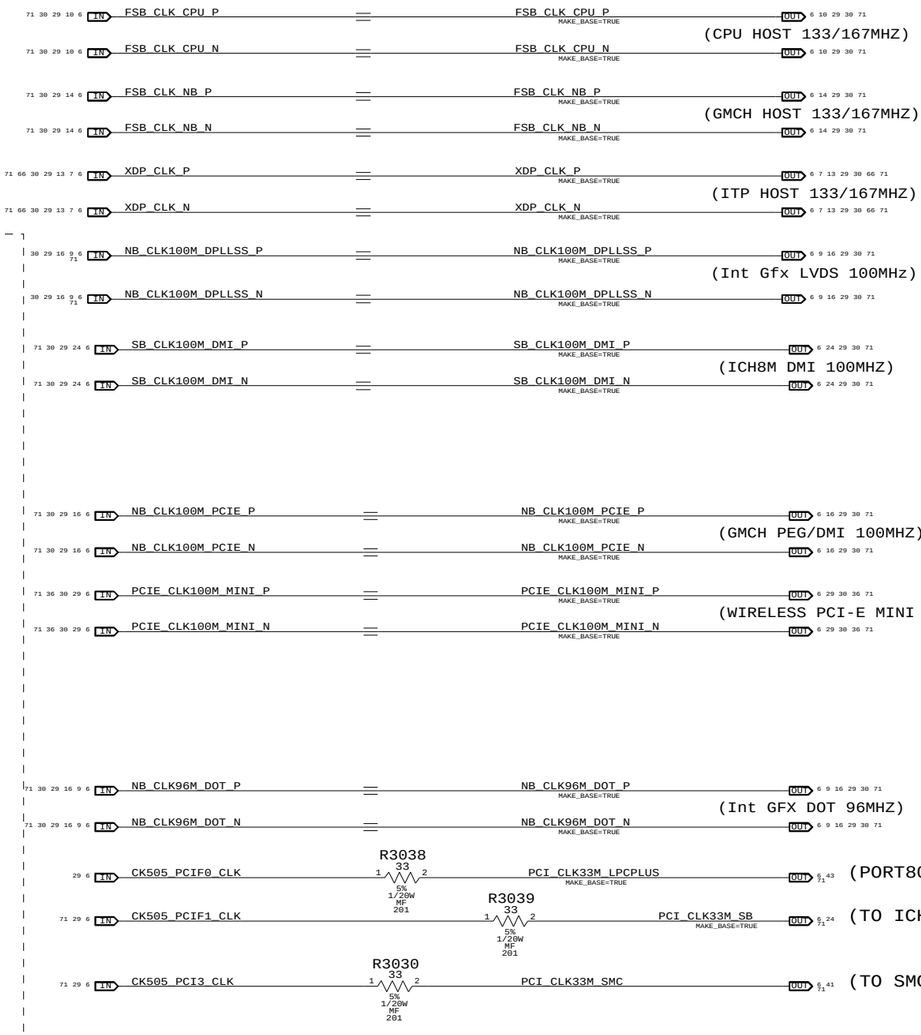




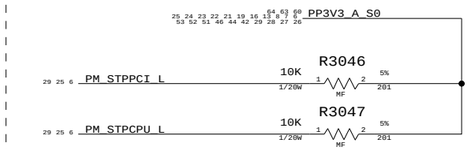
FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	1	166M
* 0	1	0	200M
1	1	0	400M
1	1	1	Resrvd
1	0	1	100M
1	0	0	333M

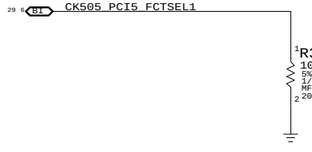
NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY

CPU speed is currently set to 200MHz

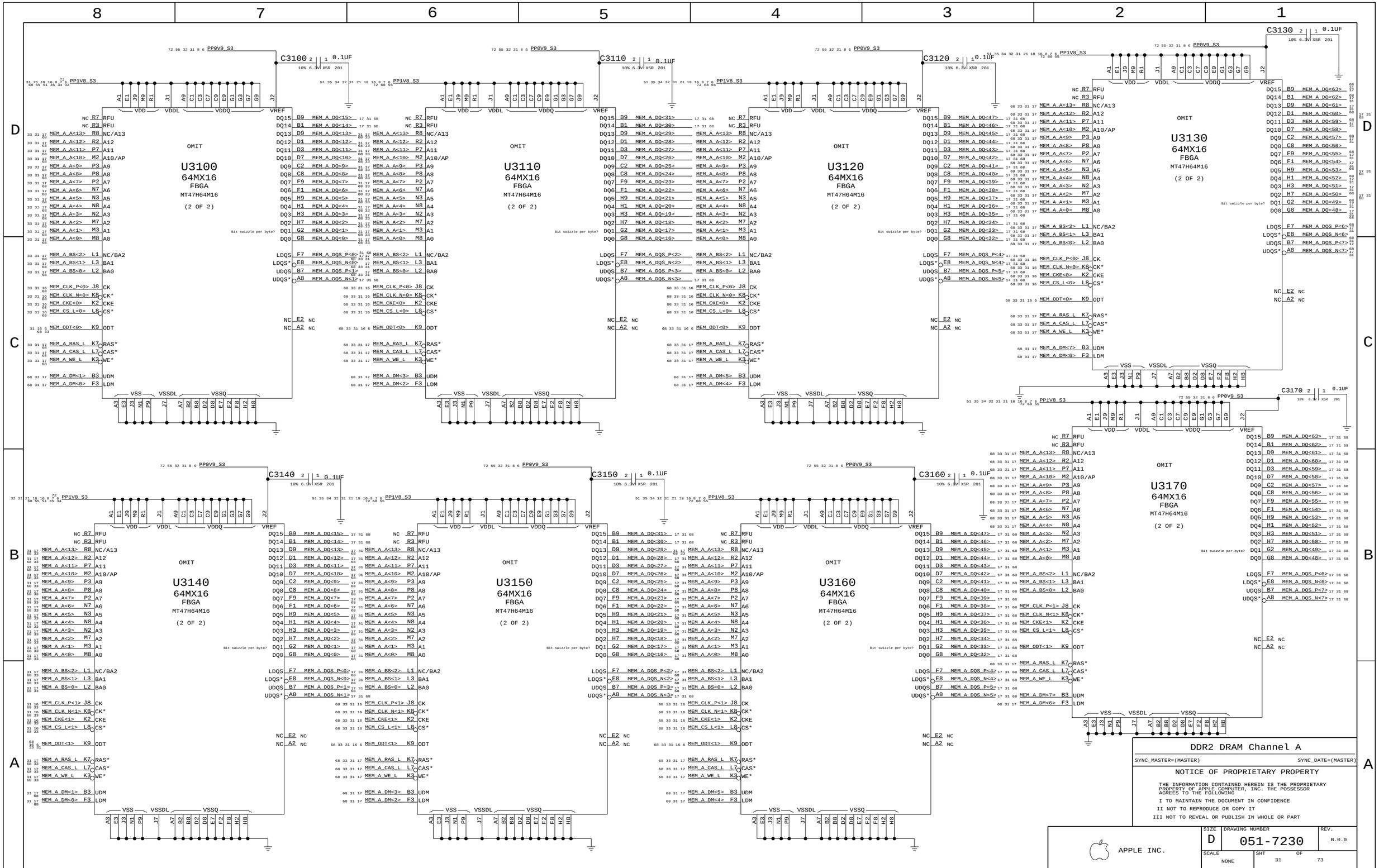


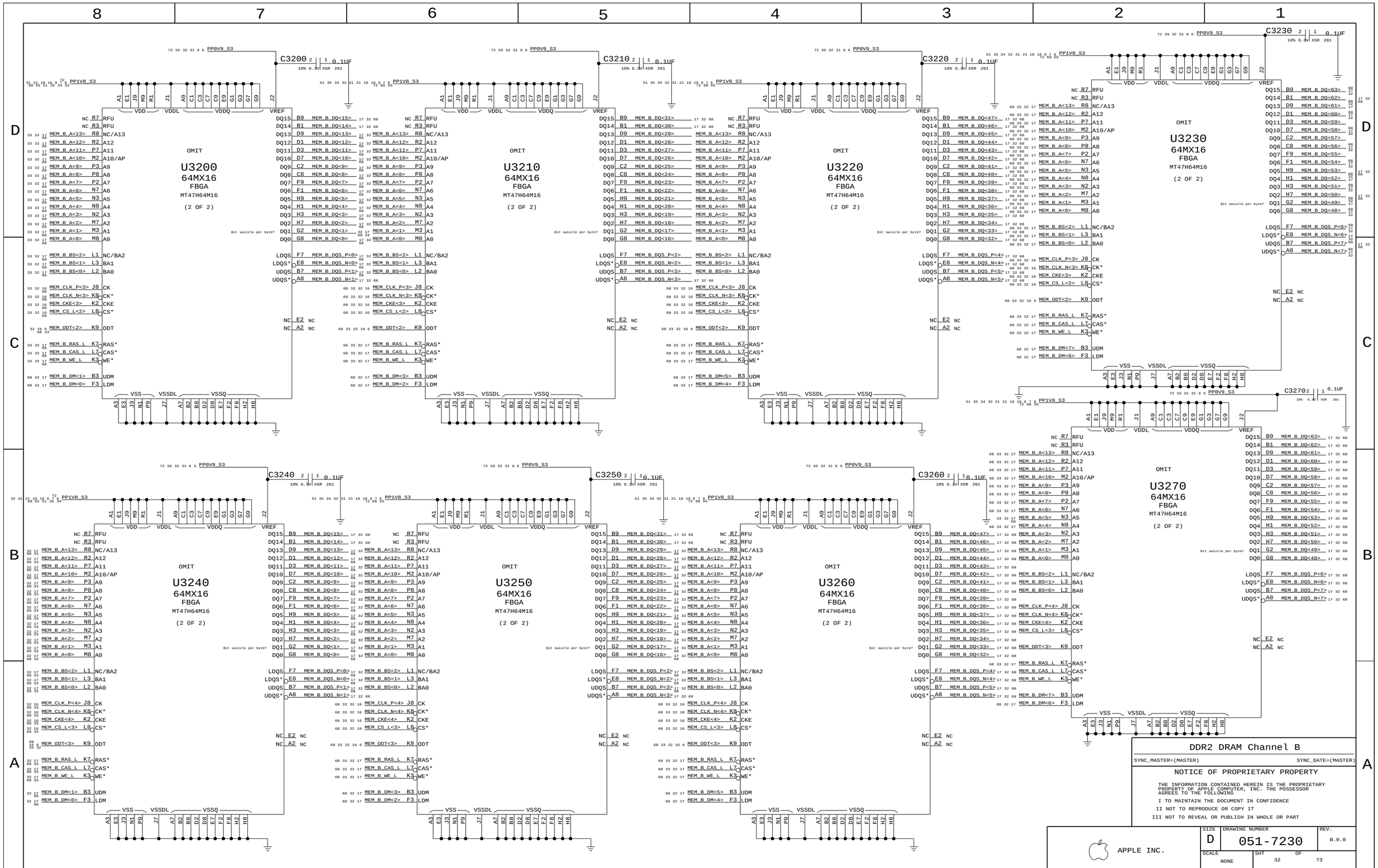
CLKREQ Controls





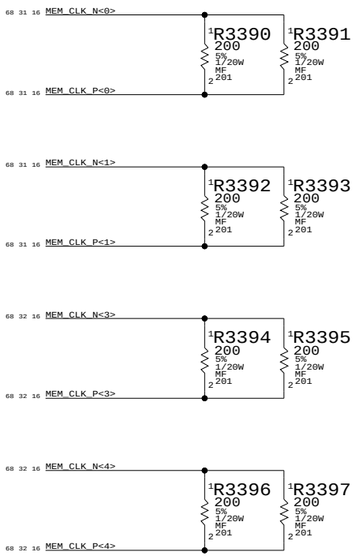
Clock Termination		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE INC.	SIZE D / DRAWING NUMBER 051-7230 / REV. B.0.0	
	SCALE NONE / SHT 30 OF 73	


C3100
C3110
C3120
C3130
C3140
C3150
C3160
C3170
0.1UF
10% 6.3V X5R 201
PP0V9_S3
PP1V8_S3
U3100
U3110
U3120
U3130
U3140
U3150
U3160
U3170
64MX16
FBGA
MT47H64M16
(2 OF 2)
OMIT
VDD
VDDL
VDDQ
VREF
VSS
VSSDL
VSSQ
DDR2 DRAM Channel A
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE
D
DRAWING NUMBER
051-7230
REV.
B.0.0
SCALE
NONE
SHT
31
OF
73

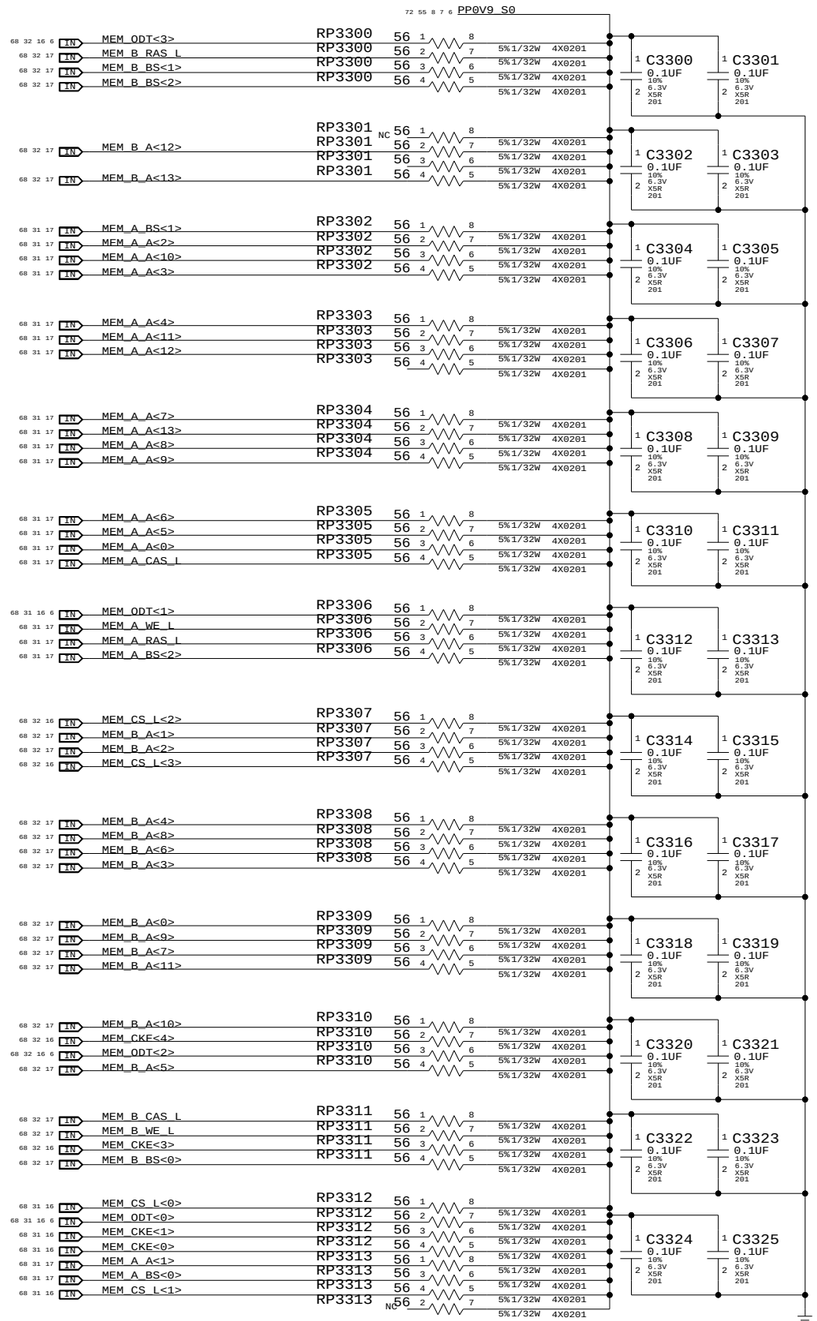

C3200 0.1UF
C3210 0.1UF
C3220 0.1UF
C3230 0.1UF
C3240 0.1UF
C3250 0.1UF
C3260 0.1UF
C3270 0.1UF
10% 6.3V X5R 201
PP0V9_S3
PP1V8_S3
U3200
U3210
U3220
U3230
U3240
U3250
U3260
U3270
64MX16
FBGA
MT47H64M16
(2 OF 2)
OMIT
VDD
VDDL
VDDQ
VREF
VSS
VSSDL
VSSQ
DDR2 DRAM Channel B
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7230
REV. B.0.0
SCALE NONE
SHT 32 OF 73

MEM CLOCK TERMINATION

Place one resistor at each end of Y split



One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it

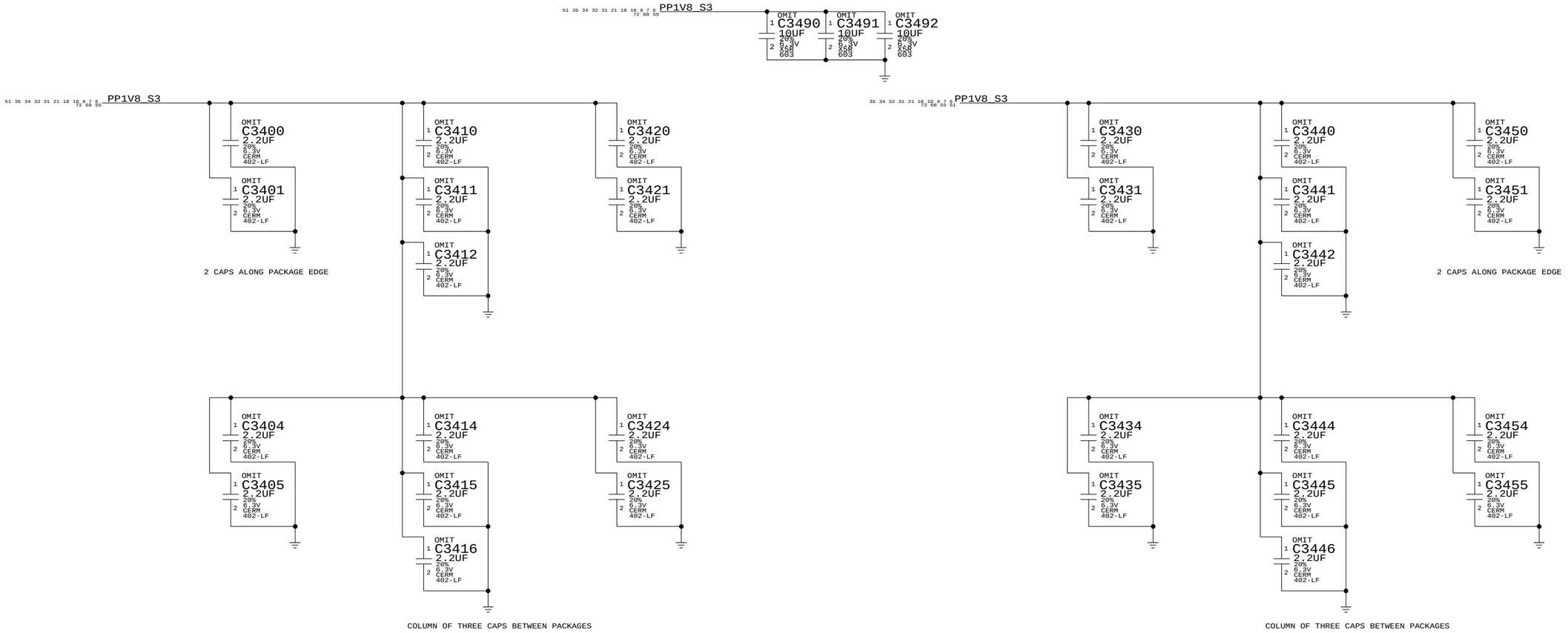


LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

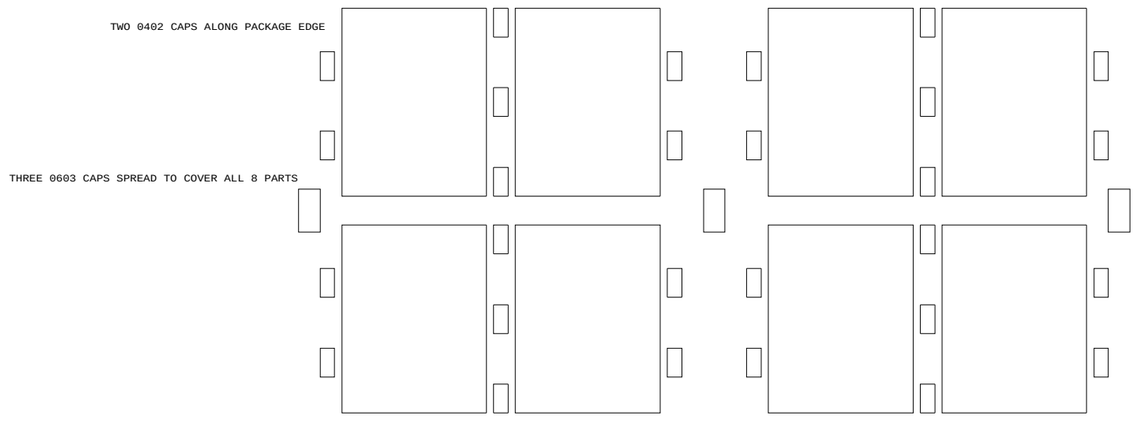
Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 33 OF 73	



APPROXIMATE CAP ARRANGEMENT



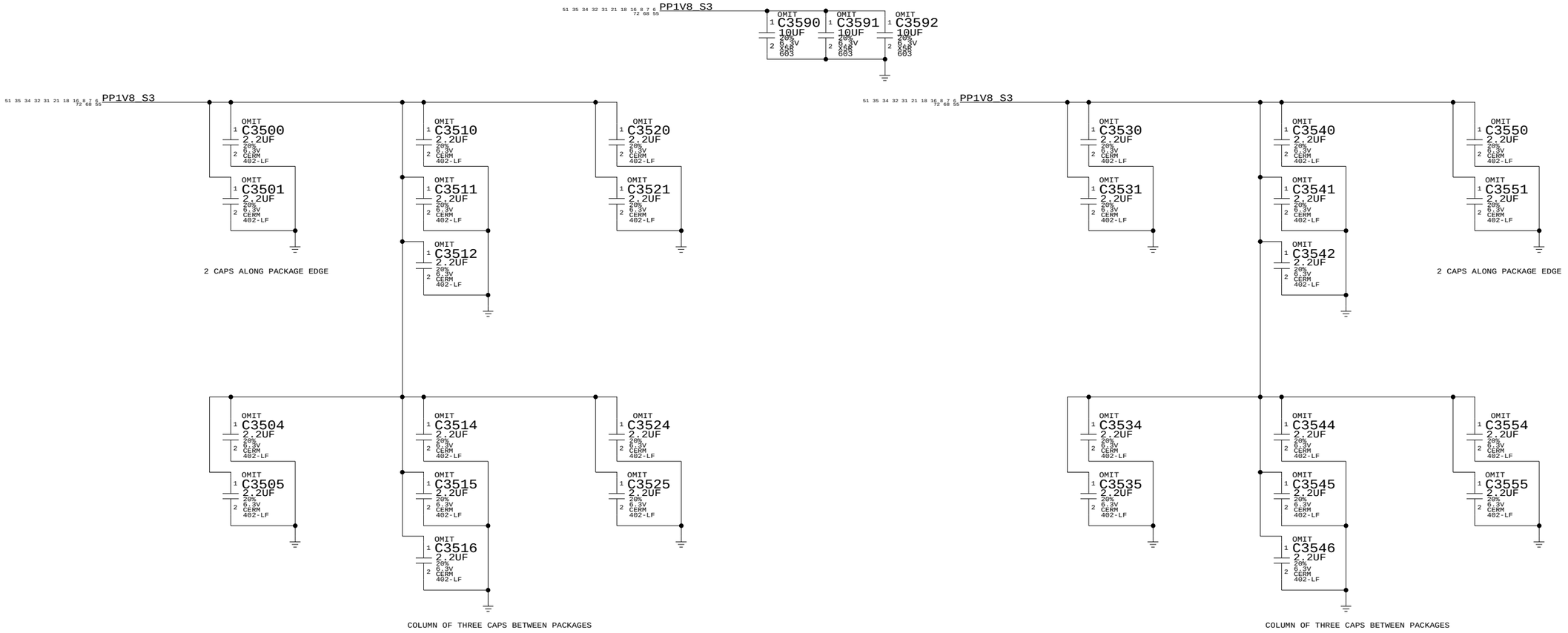
COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

DDR2 BYPASSING 1

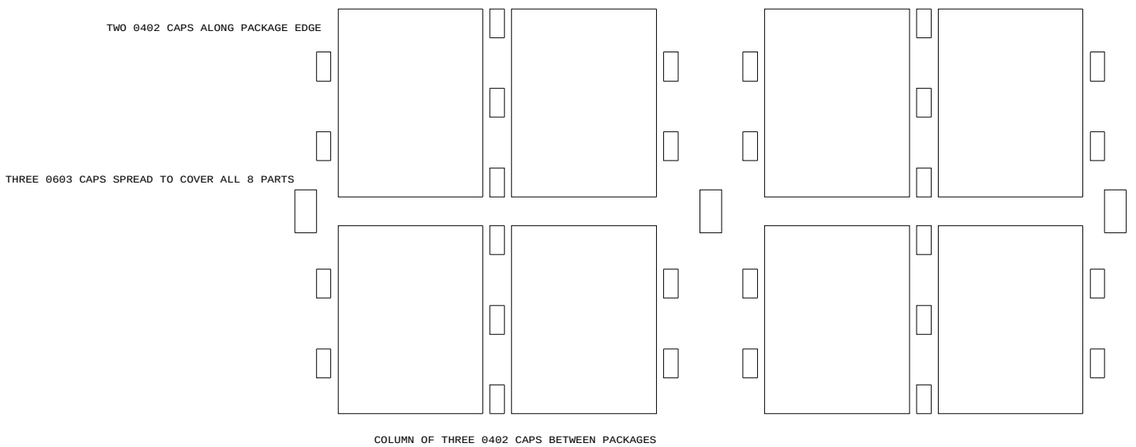
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 34 OF 73	



APPROXIMATE CAP ARRANGEMENT



COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

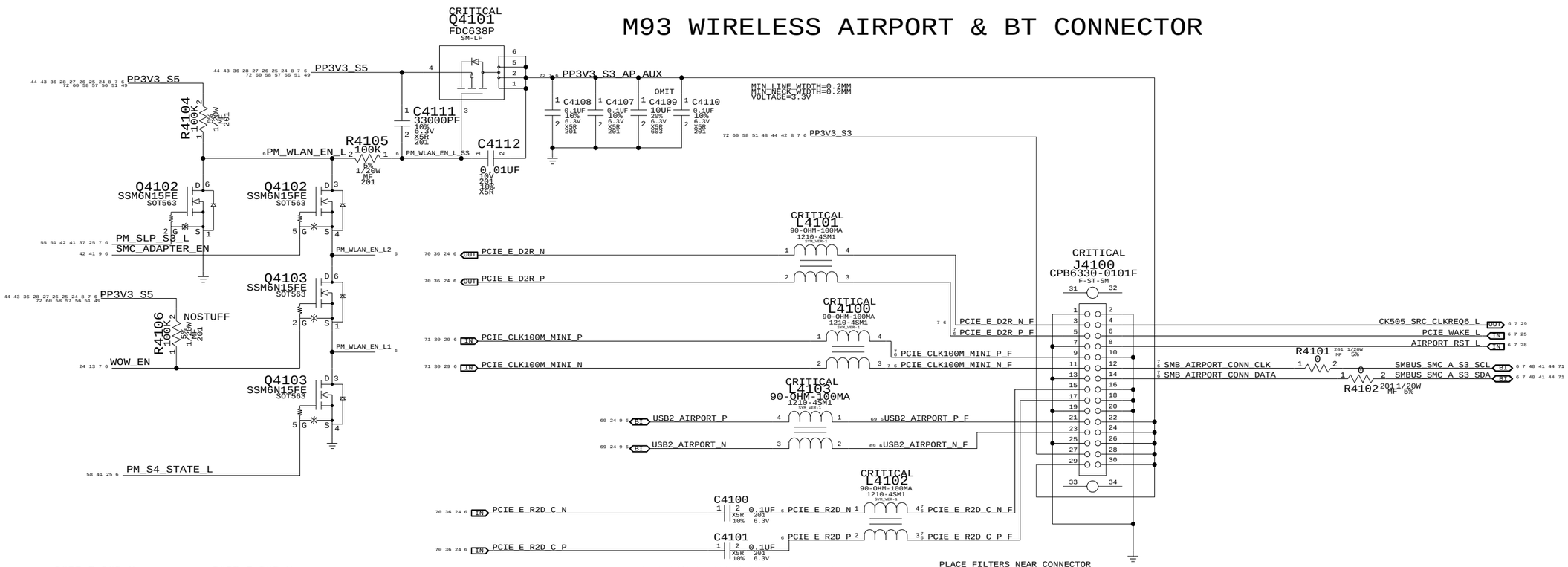
DDR2 BYPASSING 2

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 35 OF 73	

M93 WIRELESS AIRPORT & BT CONNECTOR



PCIE_E_D2R_N — PCIE_E_D2R_N — MAKE_BASE=TRUE

PCIE_E_D2R_P — PCIE_E_D2R_P — MAKE_BASE=TRUE

PCIE_E_R2D_C_N — PCIE_E_R2D_C_N — MAKE_BASE=TRUE

PCIE_E_R2D_C_P — PCIE_E_R2D_C_P — MAKE_BASE=TRUE

PLACE C4100,C4101 < 250 MILS FROM SB

PLACE FILTERS NEAR CONNECTOR

APN:516S0580

Wireless M93 Connector

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

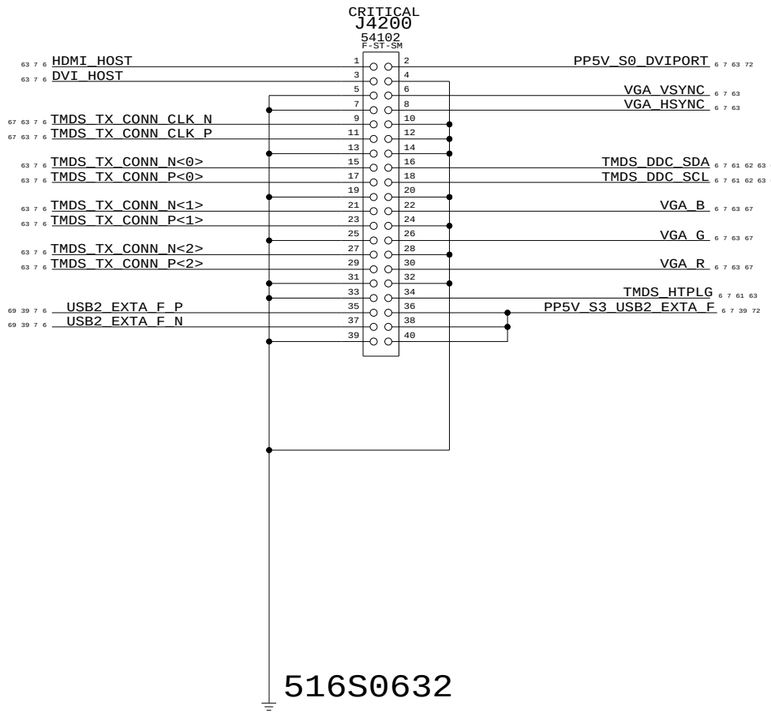
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

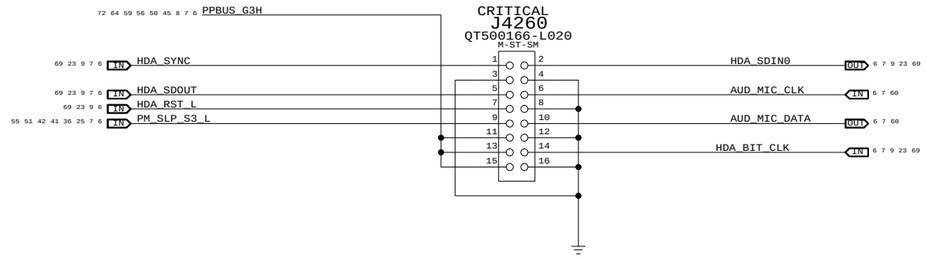
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 36 OF 73	

Micro DVI, USB, to RIO Hatch Assembly



516S0632

Audio Connector



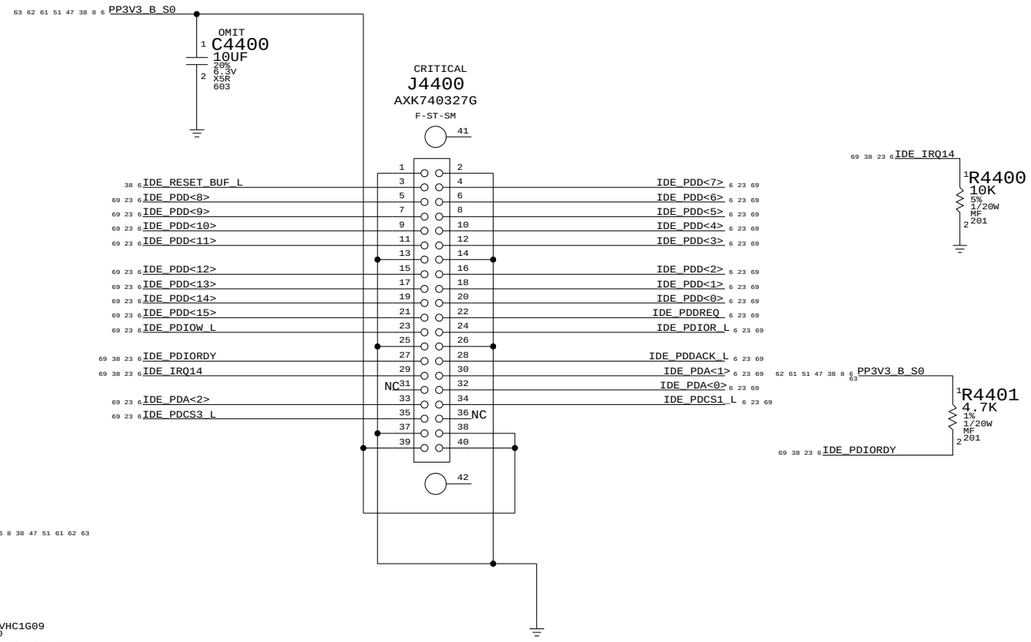
516S0350

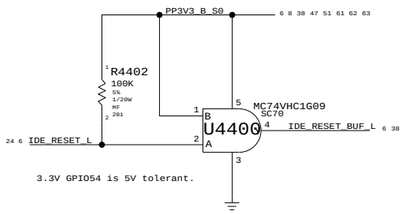
Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 37 OF 73	





516S0594

PATA HDD CONNECTOR

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 38 OF 73	

USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT

PP5V_S5

OMIT C4613 10uF 20% 6.3V X5R 603

C4612 0.1UF 10% 6.3V X5R 201

CRITICAL C4610 100UF 20% 6.3V POLY B2-HF

CRITICAL L4602 FERR-120-OHM-3A 0603

PP5V_S3_USB2_EXTA_F
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

ROUTE USB DATA LINES AS DIFFERENTIAL PAIRS

CRITICAL L4600 90-OHM-100MA 1210-4SM1

USB2_MUXED_EXTA_N
USB2_MUXED_EXTA_P

PP5V_S3_USB2_EXTA_F
USB2_EXTA_F_N
USB2_EXTA_F_P
CONNECT TO RIO CONNECTOR J4200

CRITICAL D4600 SC-75 RCLAMP0502B

C4602 0.01UF 10% 10V X5R 201

LAYOUT NOTE:C4602 IS AN EMC BY-PASS CAP FOR J4200

U4600 TPS2023DG4 SOI

CRITICAL
IN_0 OUT_0 → PP5V_S3_USB2_EXTA
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
IN_1 OUT_1
OUT_2
EN* OC*
GND

PM_SLP_S4_LS5V

EXTAUSB_OC_F_L

R4650 1K 5% 1/20W MF 201

EXTAUSB_OC_L

C4650 0.47UF 10% 6.3V CERM-X5R 402

CURRENT LIMIT TO 1.5A CONTINUOUS

USB/SMC MUX

PP3V42_G3H

R4675 100 5% 1/20W MF 201

PP3V42_G3H_SMCUSBMUX_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V

C4675 0.1UF 10% 6.3V X5R 201

PLACE C4675 NEAR U4675

R4677 10K 5% 1/20W MF 201

USB2_MUXED_EXTA_P
USB2_MUXED_EXTA_N

SMC_RX_L
SMC_TX_L
USB2_EXTA_P
USB2_EXTA_N

U4675 PI3USB10LP TQFN

CRITICAL
D+A D+
D-A D-
D+B
D-B
OE*
SEL
VCC
GND

USB_DEBUGPRT_EN_L

SEL=0 CHOOSE SMC
SEL=1 CHOOSE USB

USB EXTERNAL CONNECTORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

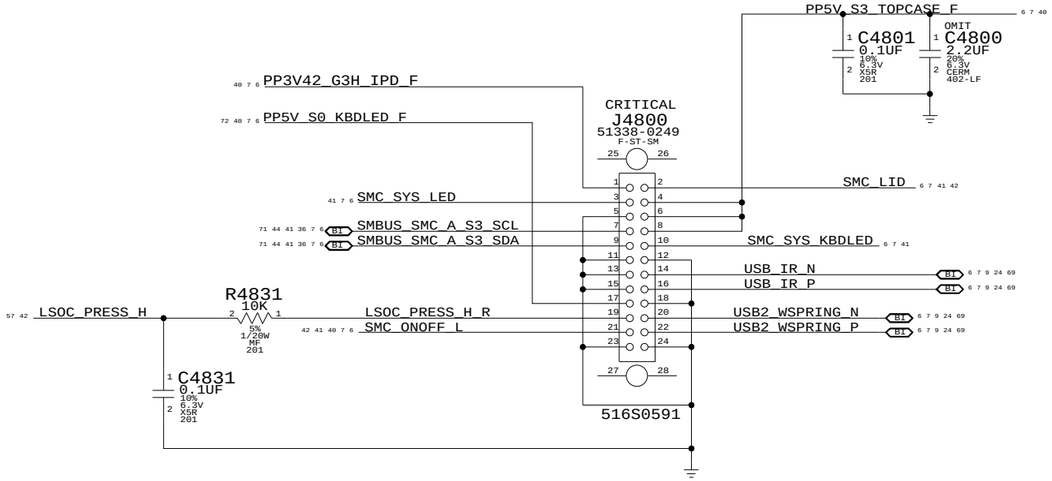
APPLE INC.

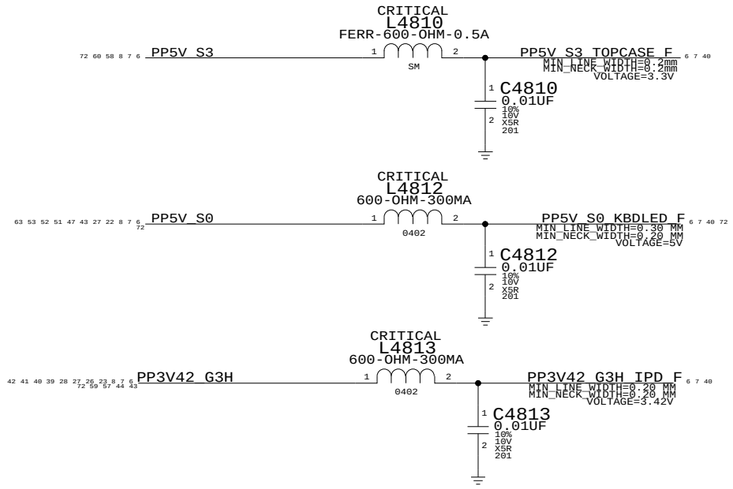
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE: NONE

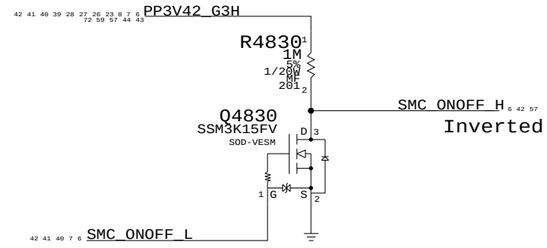
SHT 39 OF 73

IPD Connector





Power Button Inverter



Inverted to drive SMC_RESET logic

IPD Connector

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

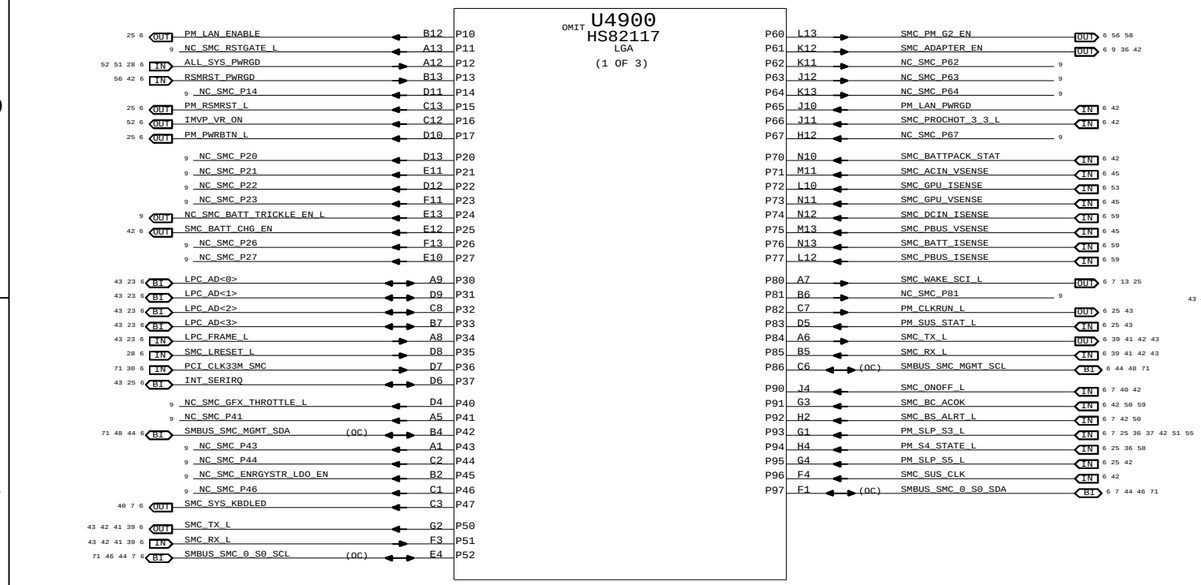
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

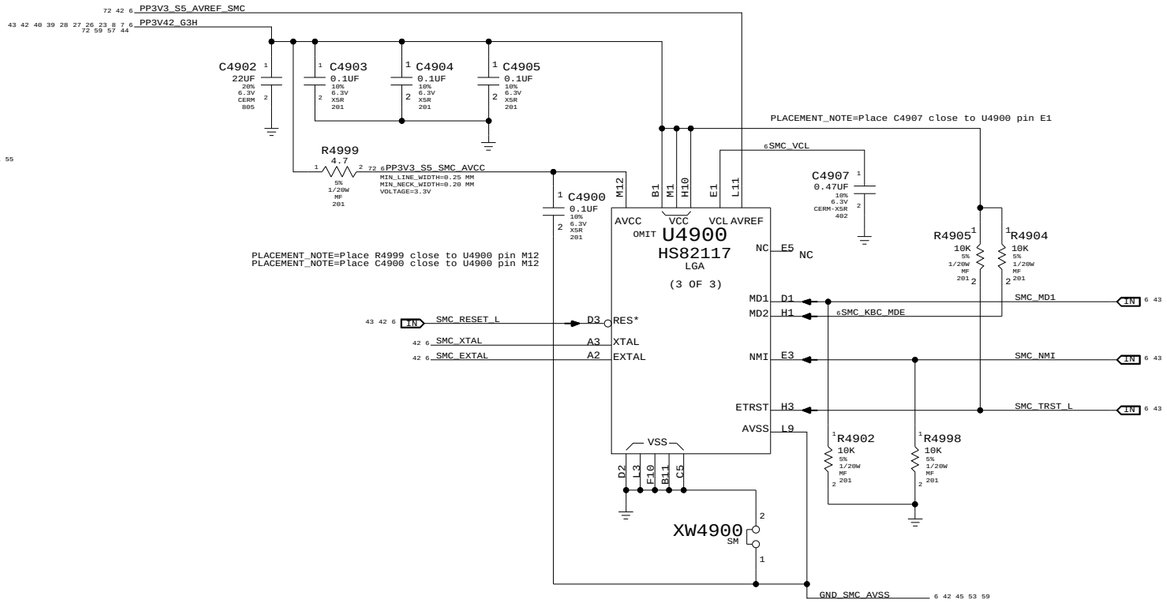
APPLE INC.

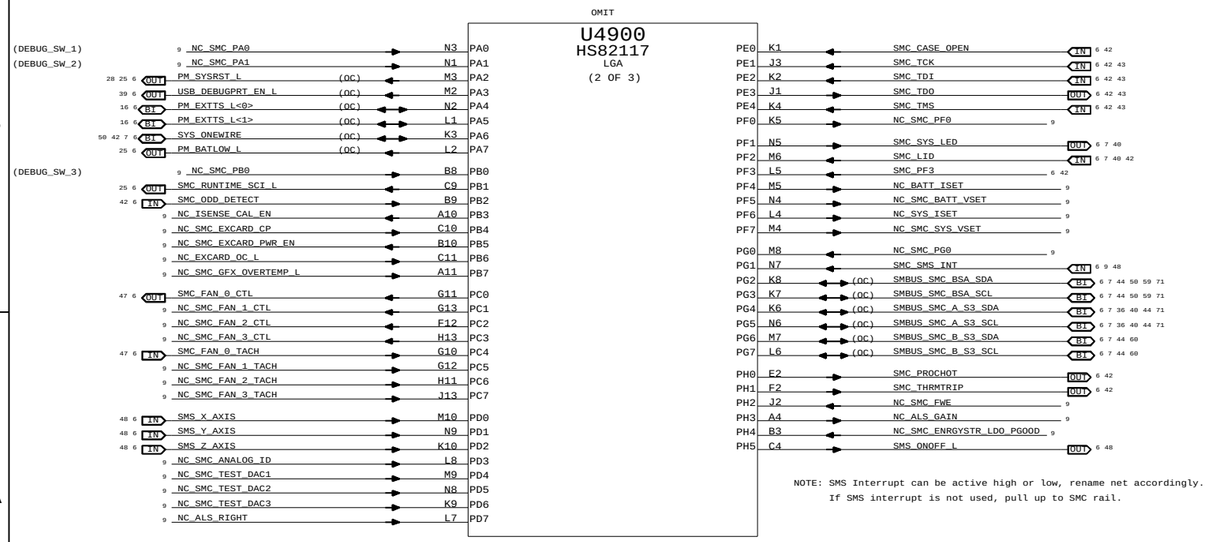
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 40 OF 73	

SMC

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

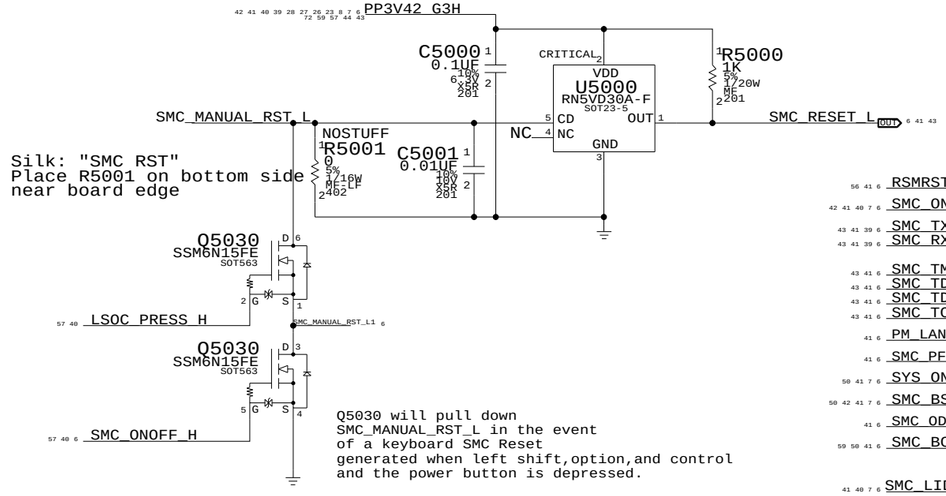
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

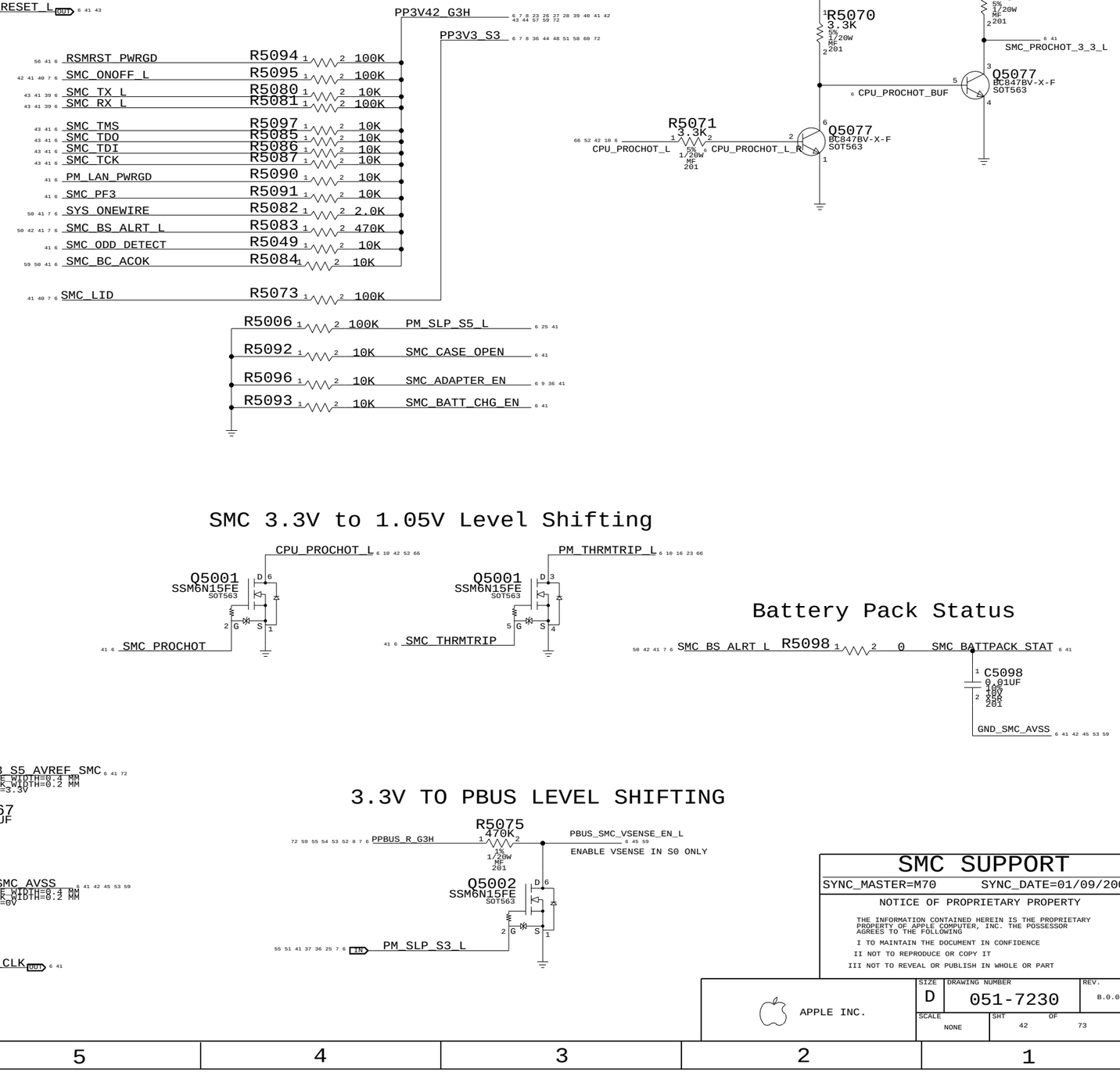
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 41 OF 73	

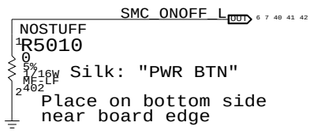
SMC Reset Button / Brownout Detect



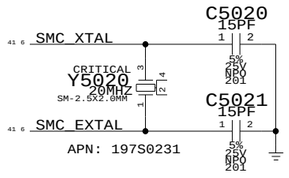
SMC 1.05V to 3.3V Level Shifting



Debug Power Button



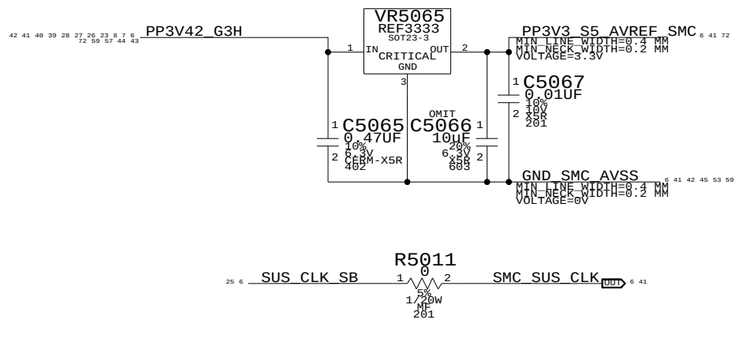
SMC Crystal Circuit



SMC 3.3V to 1.05V Level Shifting

Battery Pack Status

SMC AVREF Supply



3.3V TO PBUS LEVEL SHIFTING

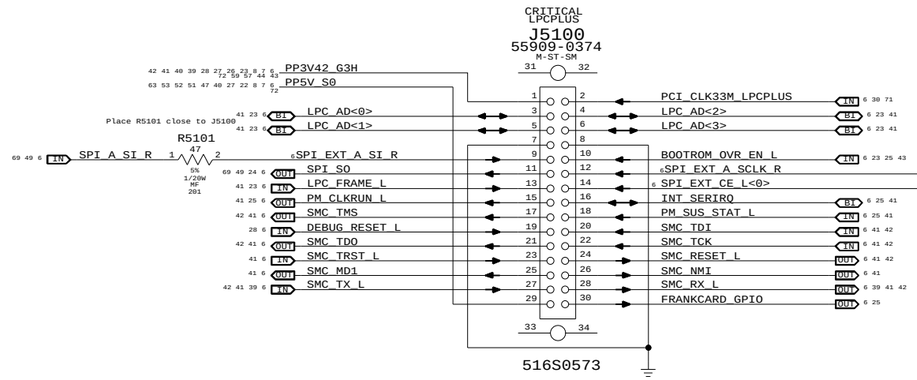
SMC SUPPORT

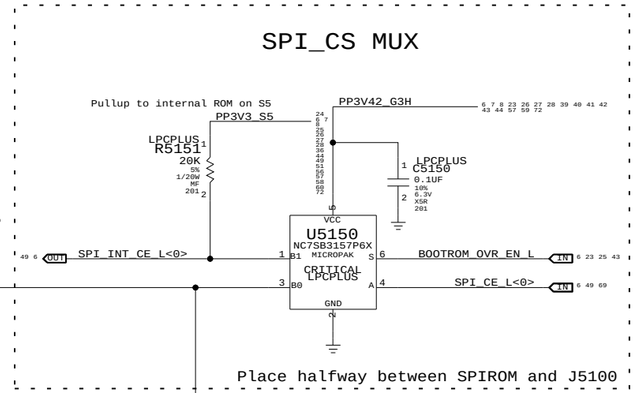
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 42 OF 73	

LPC+SPI Connector





LPC+SPI Debug Connector

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

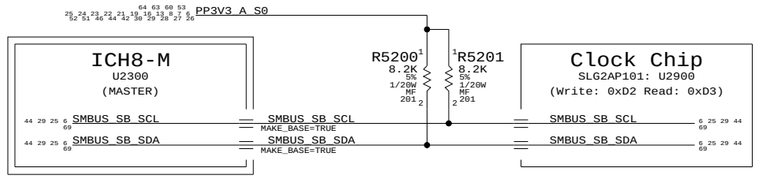
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

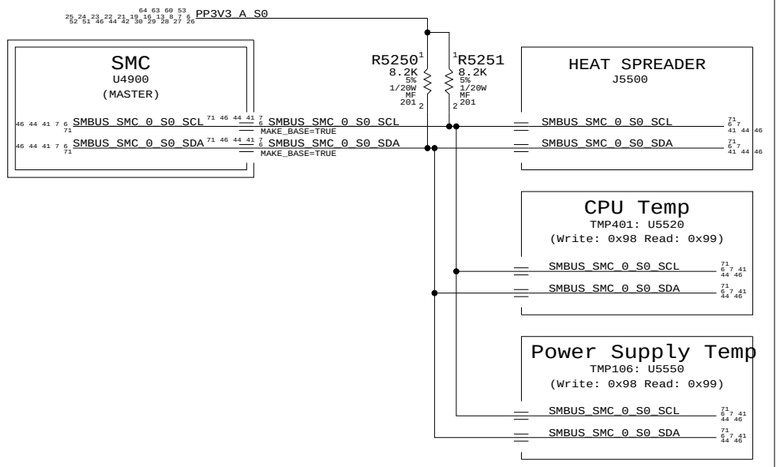
SCALE: NONE

SHT 43 OF 73

ICH8-M SMBus Connections

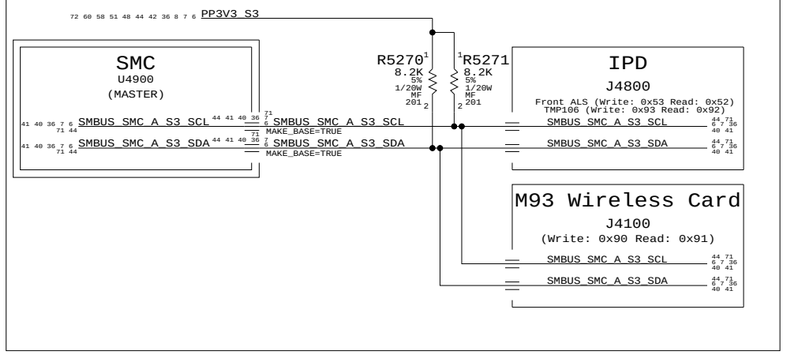


SMC "0" SMBus Connections

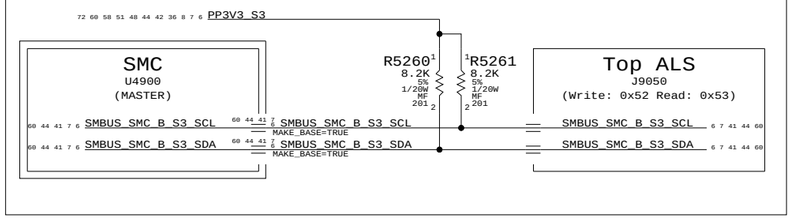


SMC "A" SMBus Connections

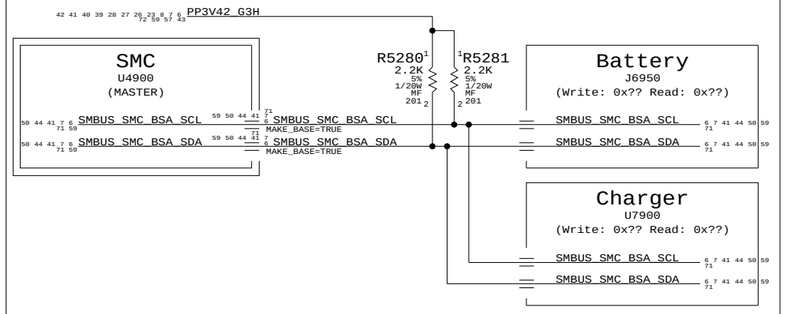
NOTE: SMC RMT bus remains powered and may be active in S3 state



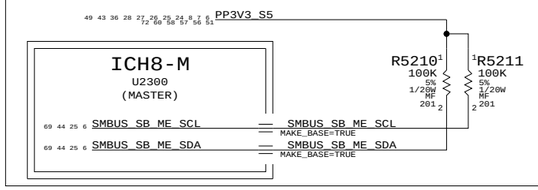
SMC "B" SMBus Connections



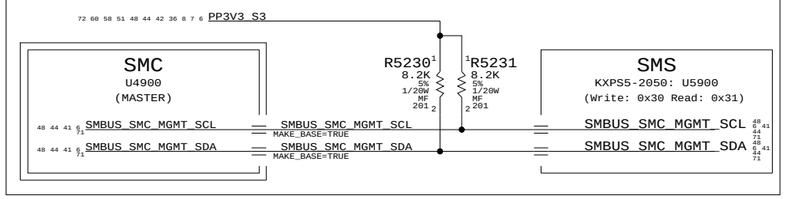
SMC "Battery A" SMBus Connections



ICH8-M ME SMBus Connections



SMC "Management" SMBus Connections



SMBUS CONNECTIONS

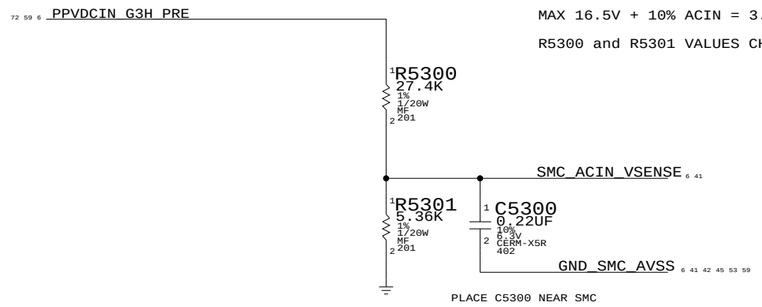
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 44 OF 73	

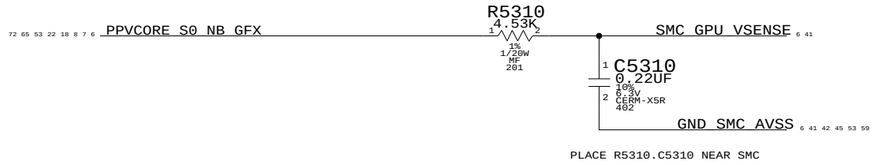
ACIN VOLTAGE SENSE



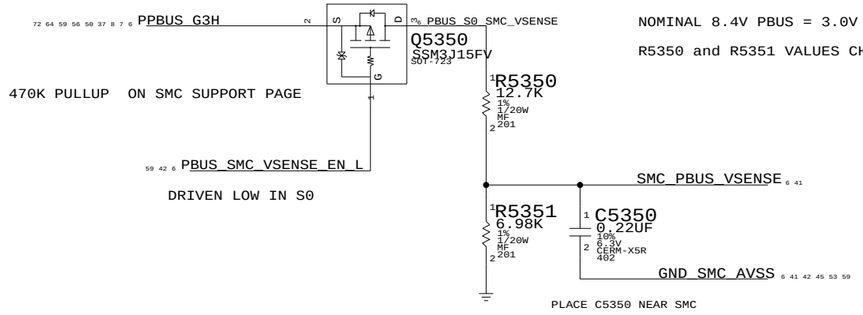
MAX 16.5V + 10% ACIN = 3.0V SMC_PBUS_VSENSE

R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

GPU VOLTAGE SENSE



PBUS VOLTAGE SENSE



NOMINAL 8.4V PBUS = 3.0V SMC_PBUS_VSENSE

R5350 and R5351 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

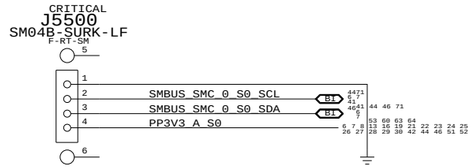
Voltage Sensors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

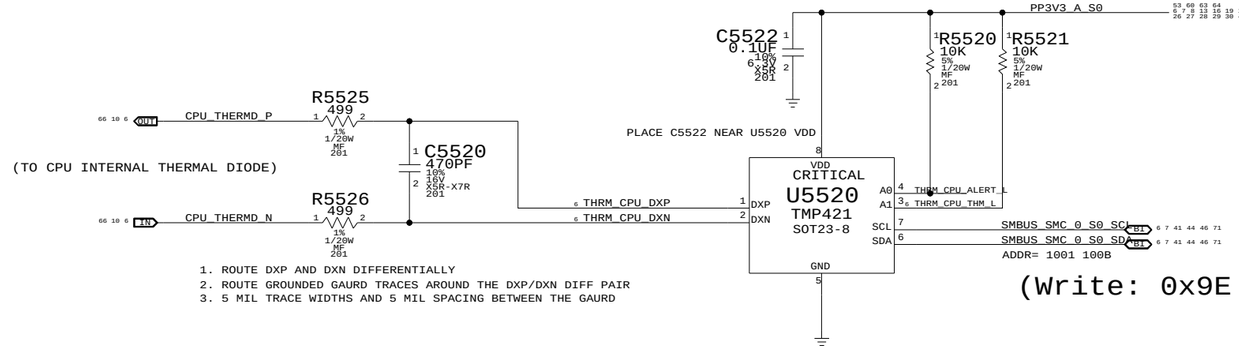
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 45 OF 73	

REMOTE TEMP AT HEAT SPREADER

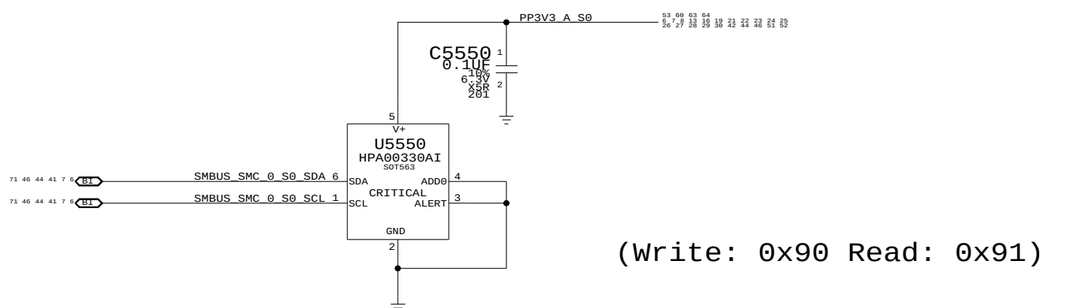


APN:518S0354

CPU THERMAL DIODE



LOCAL TEMP NEAR POWER SUPPLIES



TEMPERATURE SENSORS

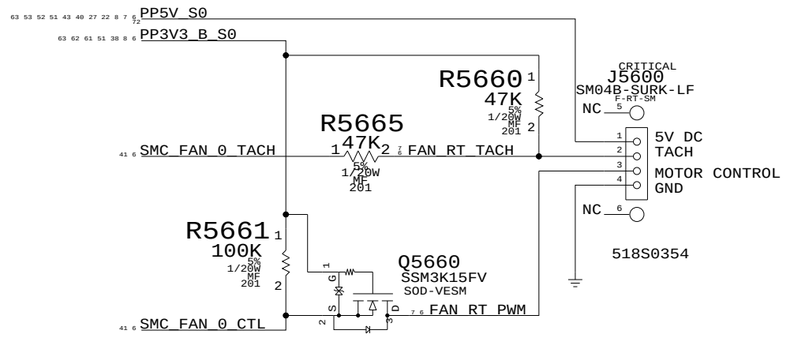
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	46	73

FAN CONNECTOR



Fan

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

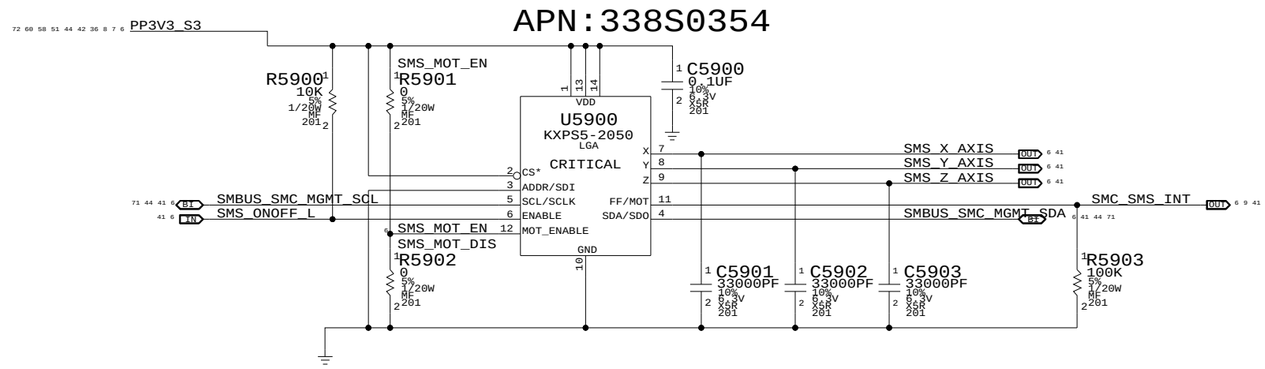
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	47	73

SUDDEN MOTION SENSOR

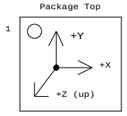
APN:338S0354



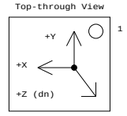
I2C addresses:

ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



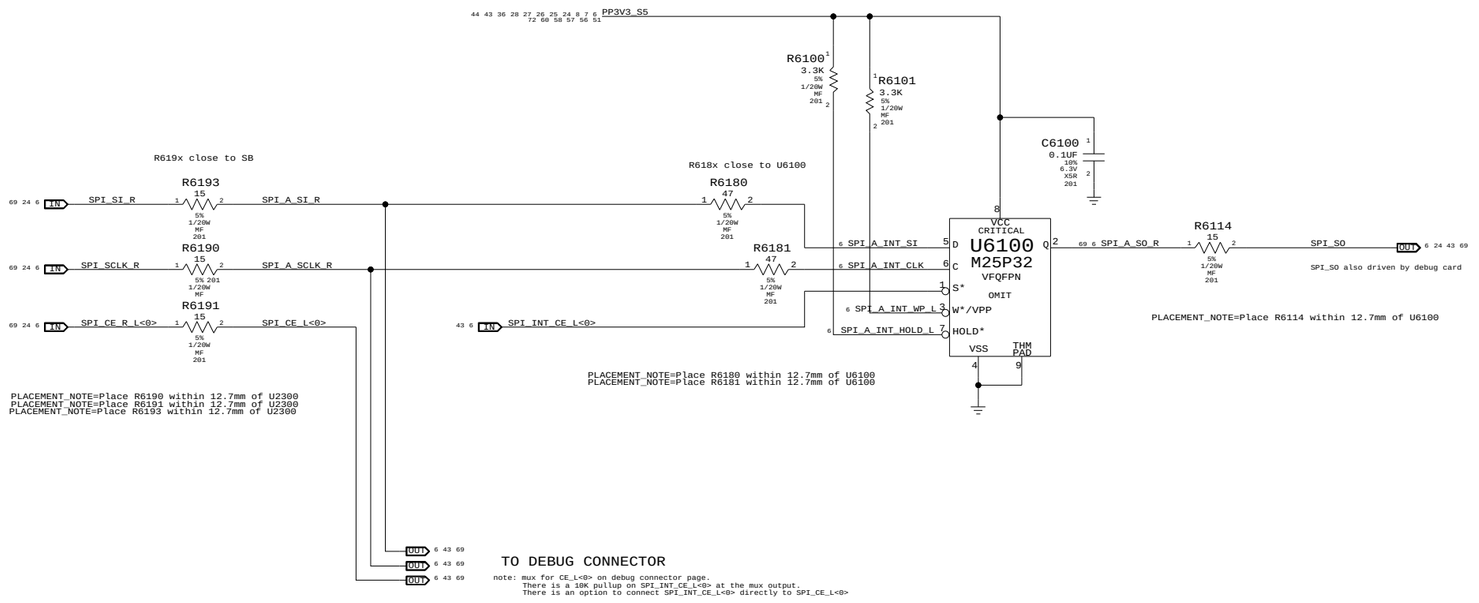
Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 48 OF 73	

SPI ROM



SPI ROMs

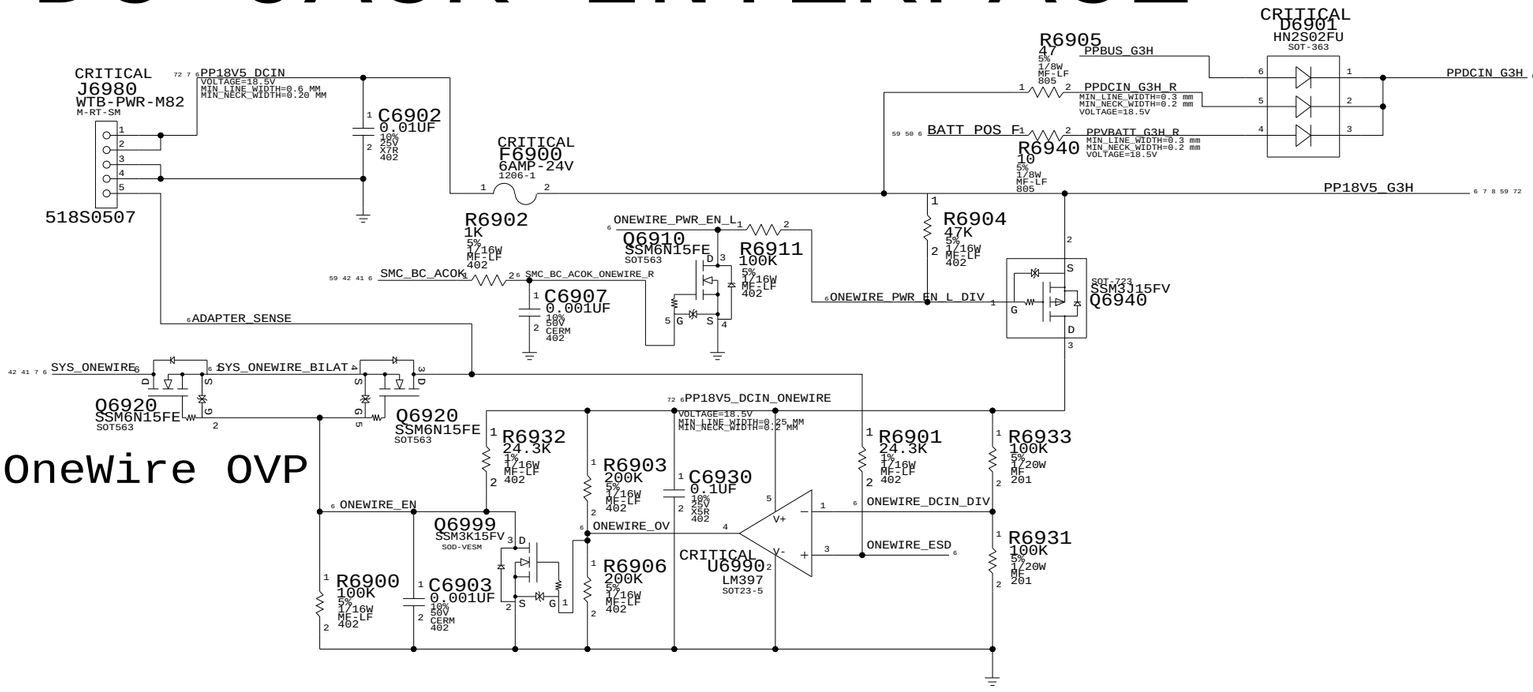
SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

APPLE INC.

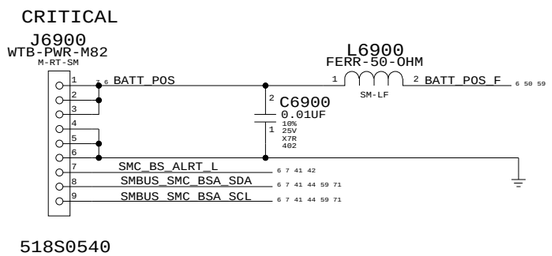
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	49	73

DC-JACK INTERFACE



BATTERY INTERFACE



DC-In & Battery Connectors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 50 OF 73	

S0 FETS & POWER SEQUENCING & PGOOD

5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.061 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.063 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	.776 A

1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.120 A

1.05V S0 RUN/SS CONTROL

1.25V S0 RUN/SS CONTROL

1.5V S0 RUN/SS CONTROL

DEASSERTED 160MS
AFTER UVLO_D VALID

~26MS

STUFF R7013,R7014 and UNSTUFF U7002,C7001,C7002
TO USE WIRE-AND OF ALL PGOODs INSTEAD OF TPS3808

U7002.3 has int 90K pull-up

S0 FETS & Power Sequencing	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

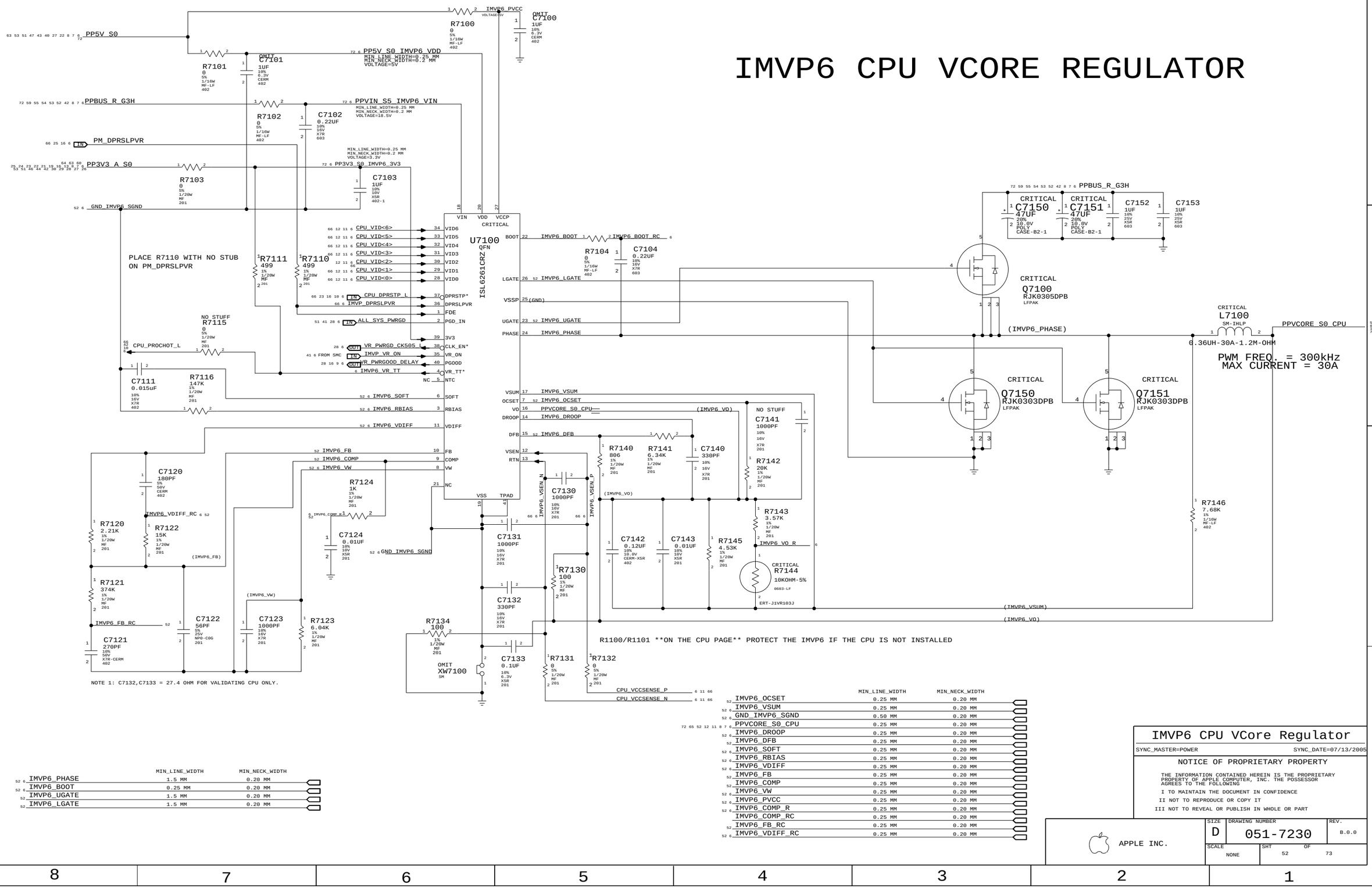
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT: 51	OF: 73

IMVP6 CPU VCORE REGULATOR



R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
PPVCORE_S0_CPU	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_COMP_RC	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

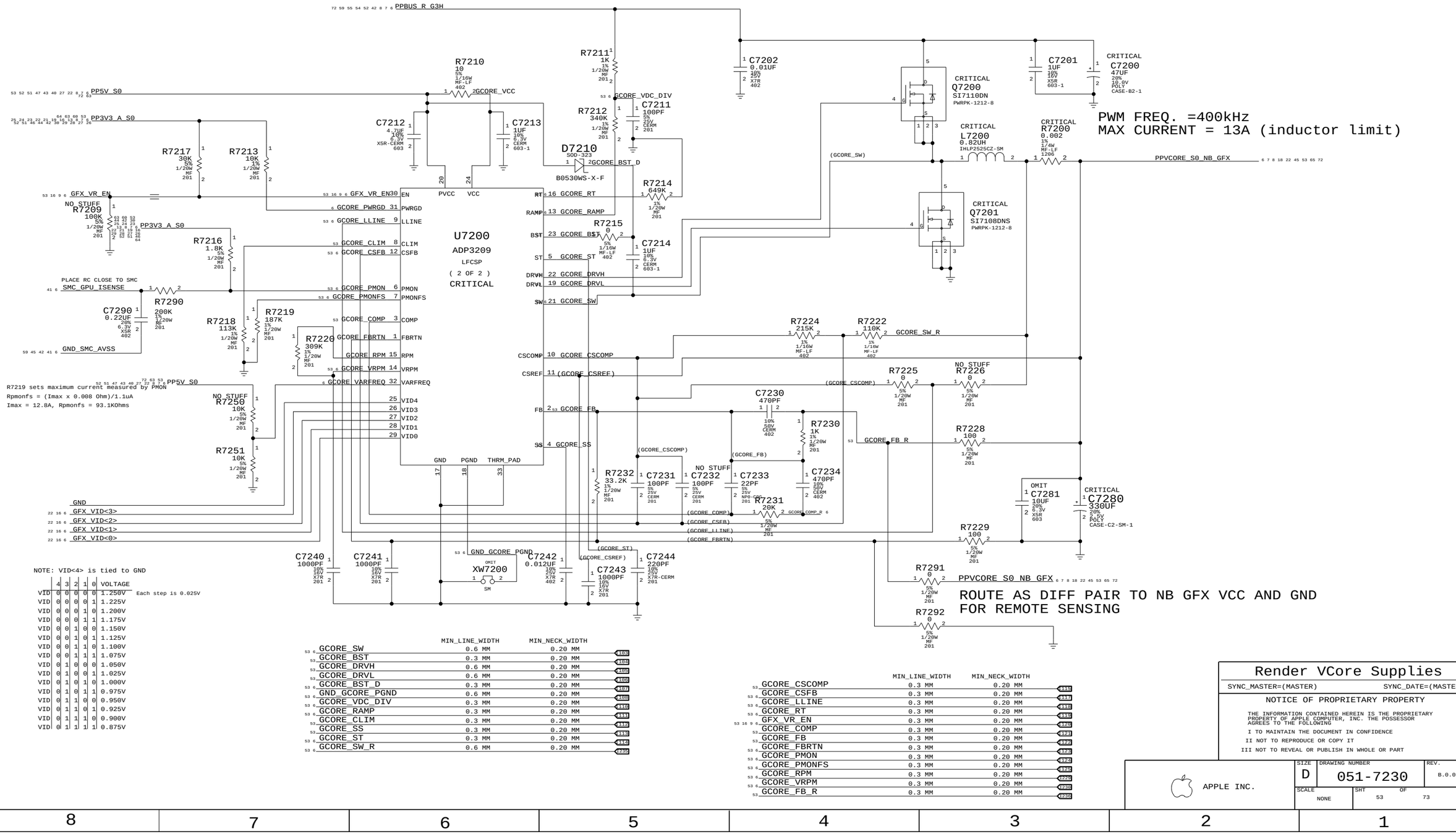
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 52 OF 73	

RENDER VCORE POWER SUPPLY



NOTE: VID<4> is tied to GND

	4	3	2	1	0	VOLTAGE
VID	0	0	0	0	0	1.250V
VID	0	0	0	0	1	1.225V
VID	0	0	0	1	0	1.200V
VID	0	0	0	1	1	1.175V
VID	0	0	1	0	0	1.150V
VID	0	0	1	0	1	1.125V
VID	0	0	1	1	0	1.100V
VID	0	0	1	1	1	1.075V
VID	0	1	0	0	0	1.050V
VID	0	1	0	0	1	1.025V
VID	0	1	0	1	0	1.000V
VID	0	1	0	1	1	0.975V
VID	0	1	1	0	0	0.950V
VID	0	1	1	0	1	0.925V
VID	0	1	1	1	0	0.900V
VID	0	1	1	1	1	0.875V

Each step is 0.025V

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GCORE_SW	0.6 MM	0.20 MM	103
GCORE_BST	0.3 MM	0.20 MM	104
GCORE_DRVH	0.6 MM	0.20 MM	105
GCORE_DRVL	0.6 MM	0.20 MM	106
GCORE_BST_D	0.3 MM	0.20 MM	107
GND_GCORE_PGND	0.6 MM	0.20 MM	108
GCORE_VDC_DIV	0.3 MM	0.20 MM	110
GCORE_RAMP	0.3 MM	0.20 MM	111
GCORE_CLIM	0.3 MM	0.20 MM	112
GCORE_SS	0.3 MM	0.20 MM	113
GCORE_ST	0.3 MM	0.20 MM	114
GCORE_SW_R	0.6 MM	0.20 MM	2225

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GCORE_CSCOMP	0.3 MM	0.20 MM	1135
GCORE_CSFB	0.3 MM	0.20 MM	1137
GCORE_LLINE	0.3 MM	0.20 MM	1138
GCORE_RT	0.3 MM	0.20 MM	1139
GFX_VR_EN	0.3 MM	0.20 MM	1140
GCORE_COMP	0.3 MM	0.20 MM	1141
GCORE_FB	0.3 MM	0.20 MM	1142
GCORE_FBRTN	0.3 MM	0.20 MM	1143
GCORE_PMON	0.3 MM	0.20 MM	1144
GCORE_PMONFS	0.3 MM	0.20 MM	1145
GCORE_RPM	0.3 MM	0.20 MM	1146
GCORE_VRPM	0.3 MM	0.20 MM	1147
GCORE_FB_R	0.3 MM	0.20 MM	1148

Render VCore Supplies

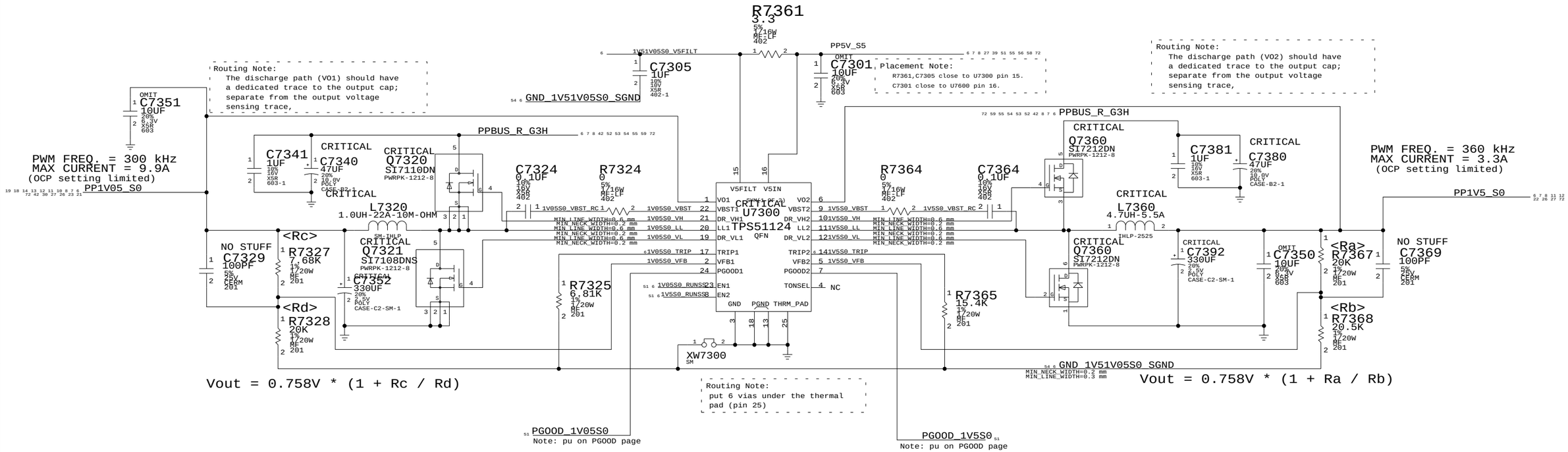
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 53 OF 73	

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



1.5V/1.05V Supplies

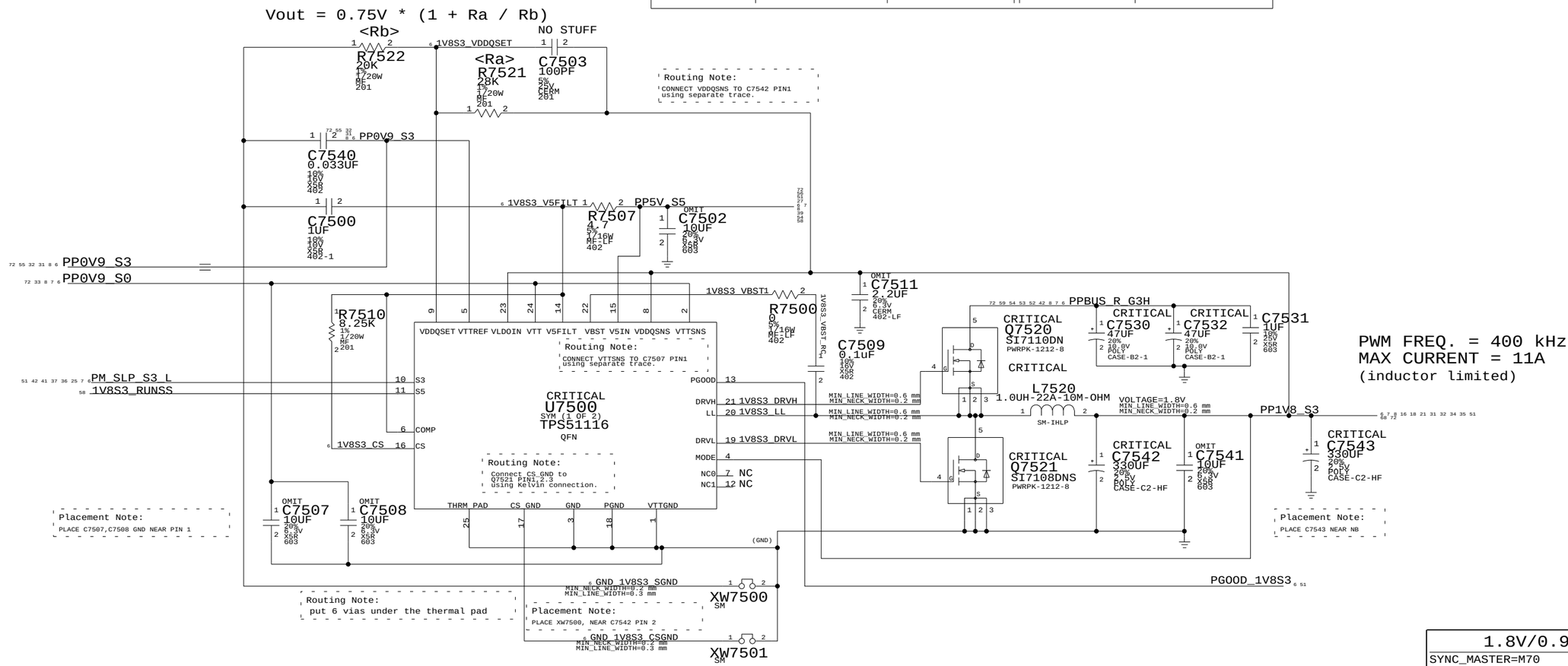
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 54 OF 73	

1.8V/0.9V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



1.8V/0.9V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	55	73

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V

Vout = 1V * (1 + Ra / Rb)
5.106V = 1V * (1 + 20K / 4.87K)

<Ra> R7667 20K 1% 1/20W MF 201
<Rb> R7668 4.87K 1% 1/20W MF 201
NO STUFF C7667 100PF 5% 25V CERM 201
GND_5V3V3S5_SGND
5VS5_FB
R7610 0 5% 1/16W MF 402
C7600 0.001UF 10% 50V CERM 402
25V3V3S5_VREF
5V3V3S5_V5FILT
GND_5V3V3S5_SGND

Routing Note:
The discharge path (VO1) should have a dedicated trace to the output cap;

Routing Note:
The discharge path (VO2) should have a dedicated trace to the output cap; separate from the output voltage sensing trace,

PPBUS_G3H

Routing Note:
put 6 vias under the thermal pad (pin 33)

CRITICAL U7600 TPS51120 LLP SYM (2 OF 3)
33 PWPD
32 SKIPSEL
31 TONSEL
30 PGOOD1
29 EN1
28 VBST1
27 DRVH1
26 LL1
25 DRVL1
24 PGND1
23 CS1
22 VIN
21 VREG5
20 V5FILT
19 VREG3
18 CS2
17 PGND2
1 VO1
2 COMP1
3 VFB1
4 VREF2
5 GND
6 VFB2
7 COMP2
8 VO2
9 EN5 NC
10 EN3 NC
11 PGOOD2
12 EN2 SMC_PM_G2_EN
13 VBST2 3V3S5_VBST
14 DRVH2 3V3S5_DRVH
15 LL2 3V3S5_LL
16 DRVL2 3V3S5_DRVL

C7680 47UF 20% 10.0V POLY CASE-B2-1
C7681 1UF 10% 16V X5R 603-1
C7660 0.1UF 10% 16V X5R 402
R7660 0 5% 1/16W MF-LF 402
RSMRST_PWRGD
SMC_PM_G2_EN
5VS5_VBST_RC
5VS5_VBST
5VS5_DRVH
5VS5_LL
5VS5_DRVL
CRITICAL Q7660 SI7110DN PWRPK-1212-8
CRITICAL L7660 3.3UH-6.5A IHLP
VOLTAGE=5V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm
CRITICAL Q7661 SI7110DN PWRPK-1212-8
OMIT C7690 10UF 20% 6.3V X5R 603
CRITICAL C7691 150UF 20% 6.3V POLY CASE-B2-HF
CRITICAL C7692 150UF 20% 6.3V POLY CASE-B2-HF
R7605 5.90K 1% 1/20W MF 201
R7603 7.15K 1% 1/20W MF 201
5V3V3S5_V5FILT
5V3V3S5_VREG3
PPBUS_G3H
R7601 4.7 5% 1/16W MF-LF 402
C7602 1UF 10% 16V X5R 603-1
OMIT C7604 10UF 20% 6.3V X5R 603
C7605 1UF 10% 16V X5R 402-1
OMIT C7603 10UF 20% 6.3V X5R 603
GND_5V3V3S5_SGND
XW7601 SM

Placement Note:
R7601,C7605 close to U7600 pin 20.
C7602 close to U7600 pin 22.
C7604 close to U7600 pin 21.
C7603 CLOSE TO U7600 PIN 19.
R7605,R7603 close to U7600.

PPBUS_G3H
C7641 1UF 10% 16V X5R 603-1
CRITICAL C7640 47UF 20% 10.0V POLY CASE-B2-1
R7620 0 5% 1/16W MF-LF 402
C7620 0.1UF 10% 16V X5R 402
CRITICAL Q7620 SI7110DN PWRPK-1212-8
CRITICAL L7620 2.2UH-14A IHLP2525CZ-SM1
VOLTAGE=3.3V MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm
CRITICAL Q7621 SI7110DN PWRPK-1212-8
CRITICAL C7652 150UF 20% 6.3V POLY CASE-B2-HF
CRITICAL C7651 150UF 20% 6.3V POLY CASE-B2-HF
OMIT C7650 10UF 20% 6.3V X5R 603
PP3V3_S5

PWM FREQ. = 280 kHz
MAX CURRENT = 6.0A
(inductor limited)

PWM FREQ. = 430 kHz
MAX CURRENT = 7.8A
(OCP setting limited)

PP5V_S5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7683	KEMET T520V336M016ATE045760
128S0093	128S0092	?	C7640	KEMET T520V336M016ATE045760

5V/3.3V Supplies

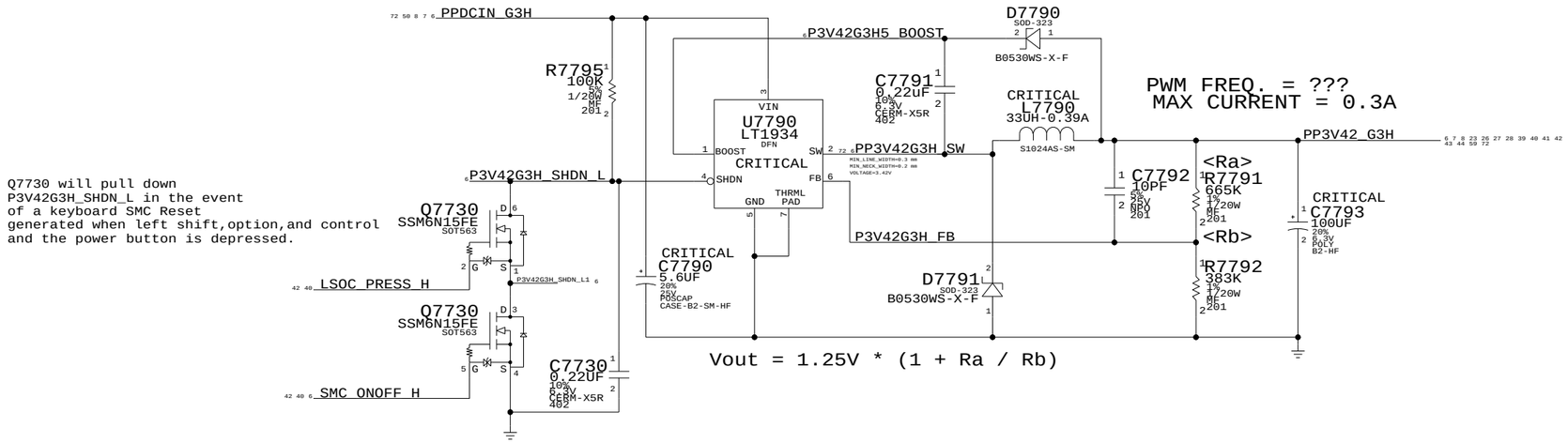
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

APPLE INC.

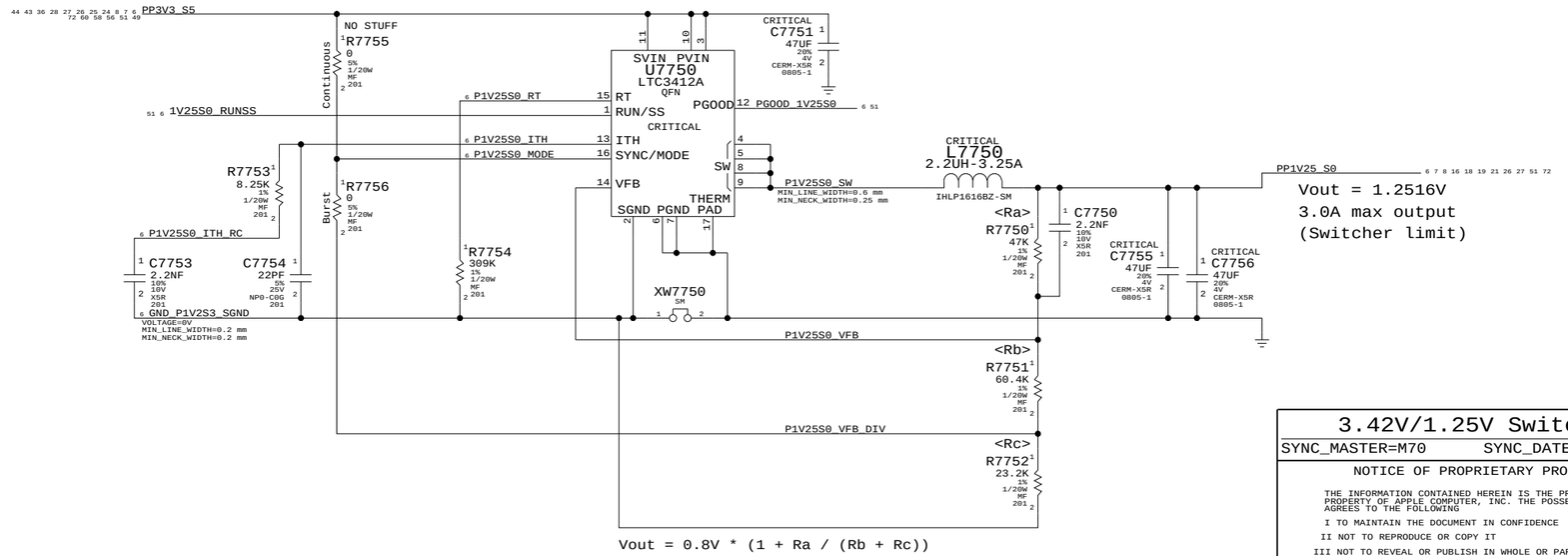
SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 56 OF 73	

3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.25V S0 REGULATOR

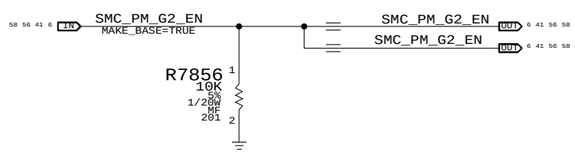


3.42V/1.25V Switcher		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	

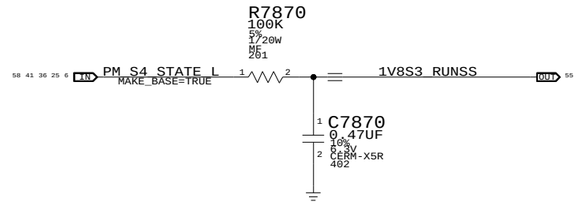
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7230	B.0.0
	SCALE: NONE	SHT 57 OF 73	

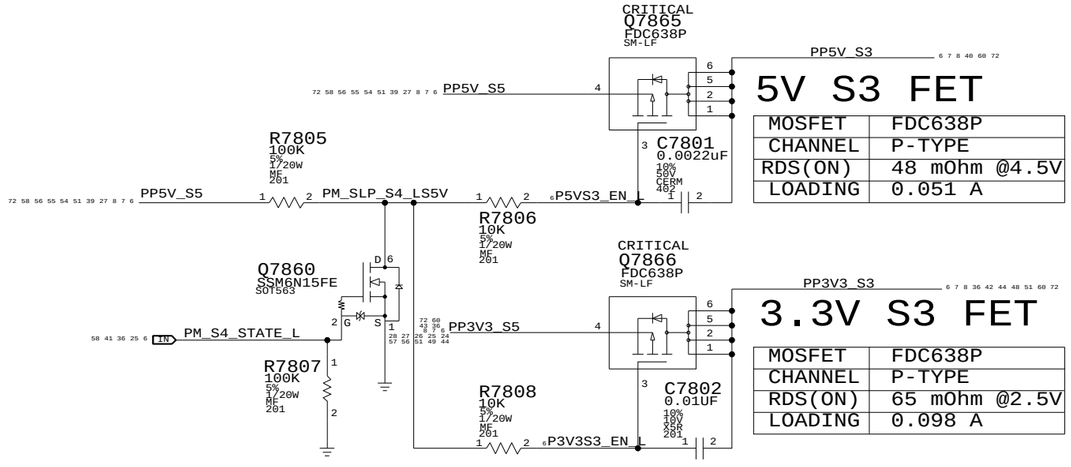
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL



1.8V S3 RUN/SS CONTROL





5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

S3 FET & S3/S5 Control

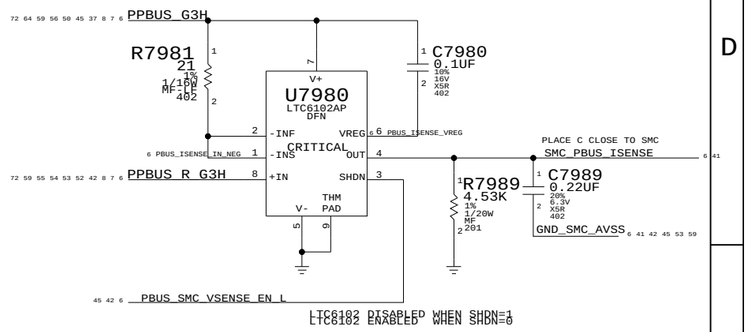
SYNC_MASTER=M70 SYNC_DATE=02/01/2007

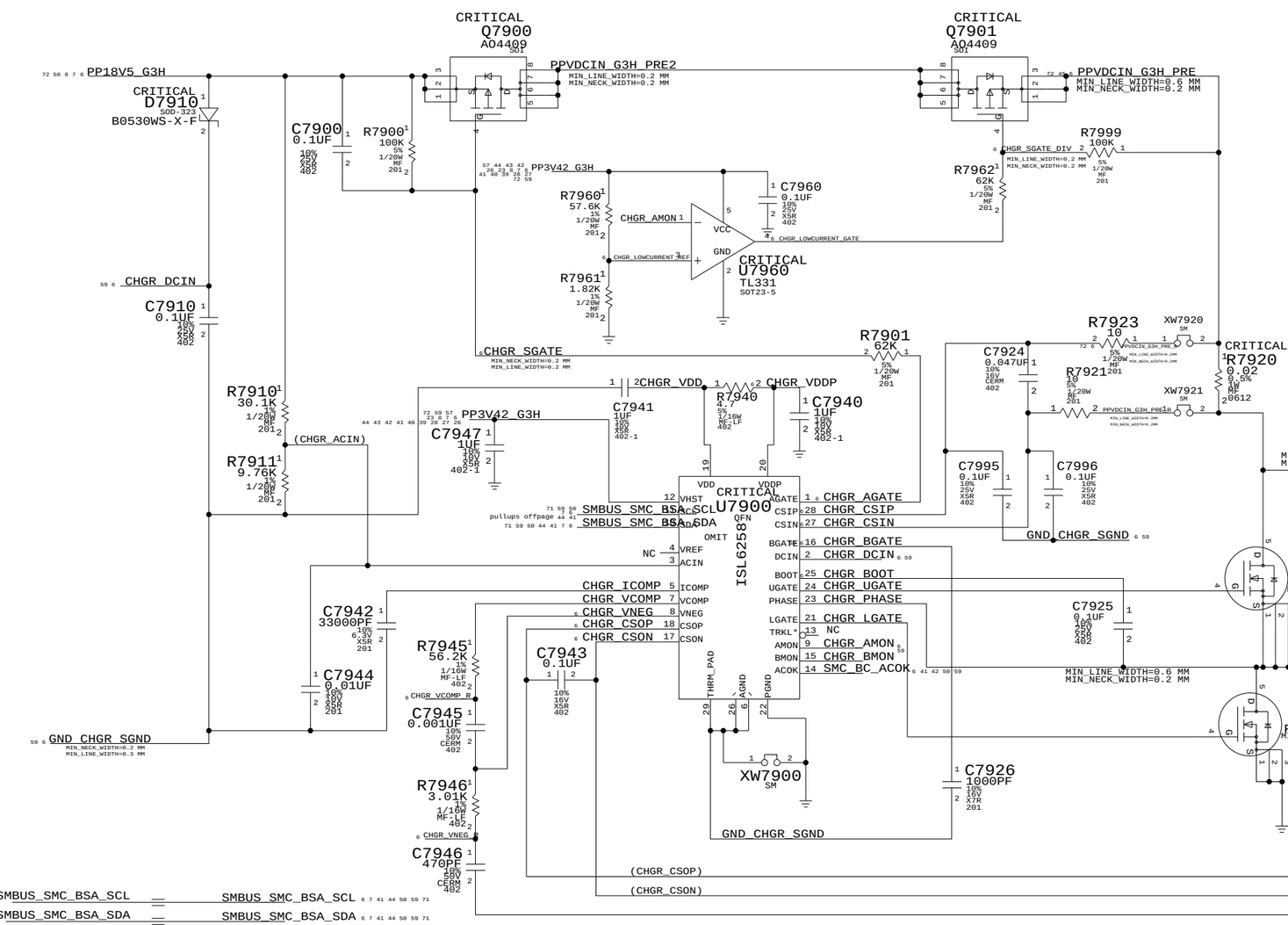
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 58 OF 73	

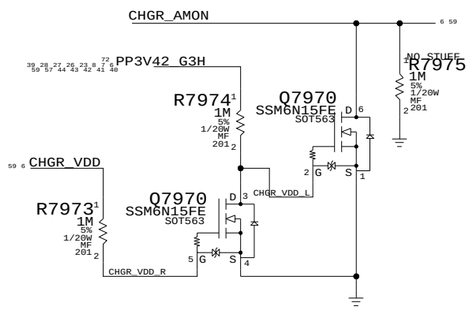
PBUS SUPPLY / BATTERY CHARGER

PBUS CURRENT SENSOR

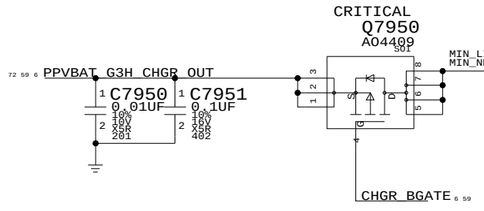




AMON PULLDOWN LOGIC



BATTERY CHARGING



PWM FREQ. = 400 kHz
MAX CURRENT = ??A
(??? limited)

PBUS Supply/Battery Charger

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 59 OF 73	

LCD + CAMERA CONNECTOR

PP3V3_S5
R9002 100K 5% 1/20W MF 201
C9040 0.1UF 10% 6.3V X5R 201
Q9004 SSM3K15FV SOD-VESM
R9023 10K 5% 1/20W MF 201
CRITICAL Q9003 FDC638P SM-LF
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603
OMIT
PP3V3_LCDVDD_SW
LCDVDD_PWREN_L
LCDVDD_PWREN_L_R
C9013 0.0033UF 10% 50V CERM 402
PLT_RST_L
LVDS_VDD_EN
U9040 TC7SZ08AFEF SOT665
LVDS_VDD_GATED_EN
R9014 100K 1% 1/20W MF 201

USB2_CAMERA_N
USB2_CAMERA_P
CRITICAL L9007 90-OHM-100MA 1210-4SM1
PP5V_S3
CRITICAL L9005 FERR-120-OHM-1.5A 0402-LF
C9016 1000PF 10% 16V X7R 201
CRITICAL L9004 FERR-120-OHM-1.5A 0402-LF
C9015 1000PF 10% 16V X7R 201

PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR

L9052 240-OHM-0.2A-0.8-OHM 0201
SMBUS_SMC_B_S3_SDA
I2C_TOP_ALS_SDA_F
L9051 240-OHM-0.2A-0.8-OHM 0201
SMBUS_SMC_B_S3_SCL
I2C_TOP_ALS_SCL_F
C9052 10PF 5% 25V NPO 201
C9051 10PF 5% 25V NPO 201

CRITICAL J9000 20347-130E-11 F-RT-SM
518S0433

PP5V_S3_CAMERA_F
USB2_CAMERA_F_P
USB2_CAMERA_F_N
PP3V3_LCDVDD_SW_F
PP3V3_S0_LCD_F
CAMERA I/F
LCD I/F

L9008 120-OHM-0.3A-EMI 0402-LF
PP3V3_A_S0
(LVDS_DDC_POWER)
C9010 1000PF 10% 16V X7R 201
R9008 10K 5% 1/20W MF 201
R9009 10K 5% 1/20W MF 201
LVDS_DDC_CLK
LVDS_DDC_DATA

LVDS_A_DATA_F_N<0>
LVDS_A_DATA_F_P<0>
LVDS_A_DATA_F_N<1>
LVDS_A_DATA_F_P<1>
LVDS_A_DATA_F_N<2>
LVDS_A_DATA_F_P<2>
LVDS_A_CLK_F_N
LVDS_A_CLK_F_P
LCDBKLT_RTN<1>
LCDBKLT_RTN<2>
LCDBKLT_RTN<3>
LCDBKLT_RTN<4>
LCDBKLT_RTN<5>
LCDBKLT_RTN<6>
PPVOUT_S0_LCDBKLT

LVDS REFERENCE CURRENT,2.37K OHM PULL DOWN RESISTOR NEEDED
R9013 2.37K 1% 1/20W MF 201
LVDS_IBG
PLACE NEAR NB

CRITICAL L9010 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
CRITICAL L9011 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
CRITICAL L9012 90-OHM-100MA 1210-4SM1
LVDS_A_DATA_N<2>
LVDS_A_DATA_P<2>
CRITICAL L9006 90-OHM-100MA 1210-4SM1
LVDS_A_CLK_N
LVDS_A_CLK_P

MIC CONNECTOR

CRITICAL J9050 GS03067-11131-7F F-RT-SM
PP3V3_S3_MIC_F
NC
NC
GND_MIC_F
L9050 240-OHM-0.2A-0.8-OHM 0201 PP3V3_S3
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
L9030 240-OHM-0.2A-0.8-OHM 0201 AUD_MIC_DATA
L9031 240-OHM-0.2A-0.8-OHM 0201 AUD_MIC_CLK
AUD_MIC_DATA_F
AUD_MIC_CLK_F
L9053 240-OHM-0.2A-0.8-OHM 0201
C9050 0.01UF 10% 10V X5R 201
C9053 0.01UF 10% 10V X5R 201
C9030 10PF 5% 25V NPO 201 NO STUFF
C9031 10PF 5% 25V NPO 201 NO STUFF

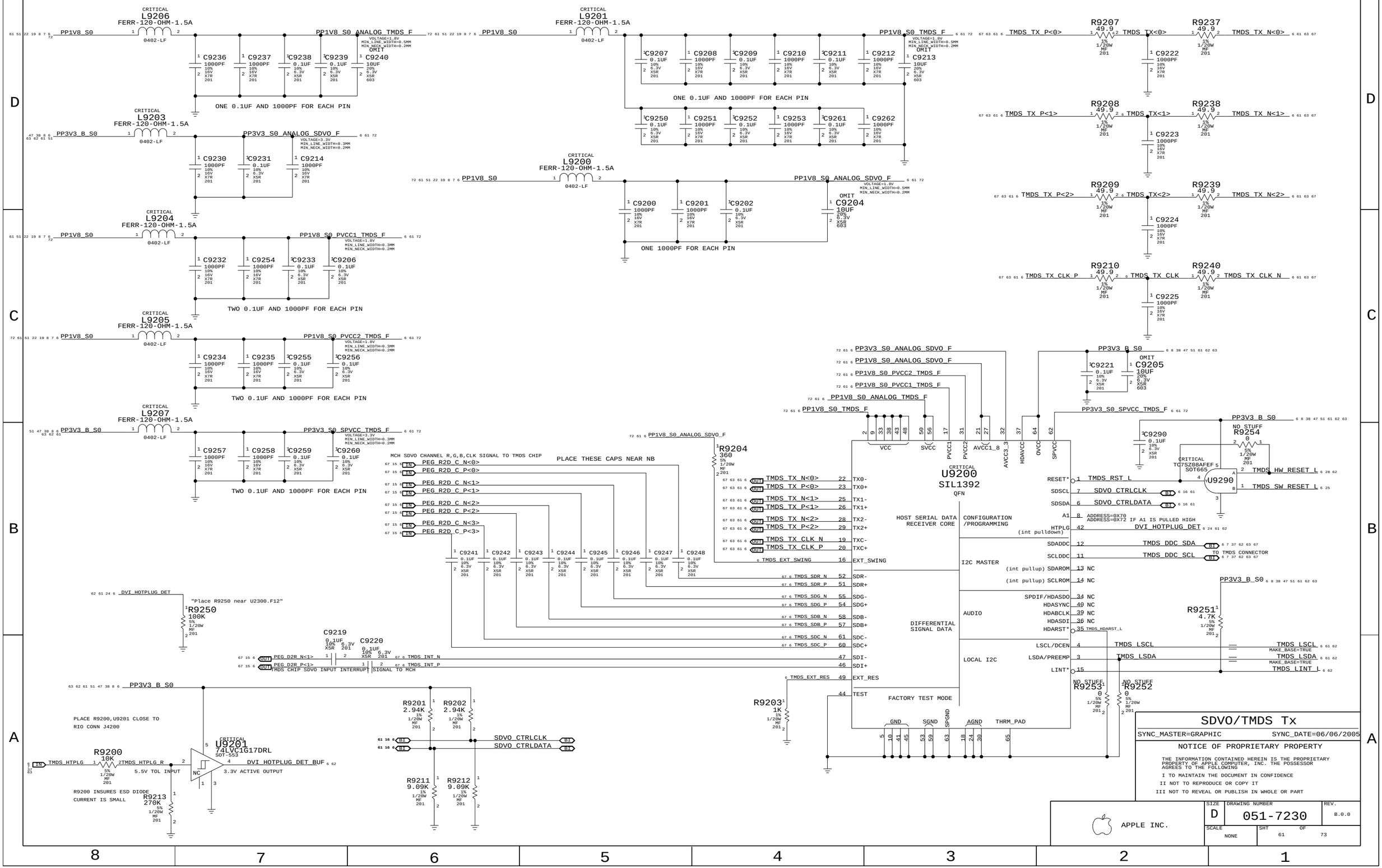
APN:518S0356

LVDS,Camera Conn. and ALS Conn.

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 60 OF 73	


CRITICAL
L9206
FERR-120-OHM-1.5A
0402-LF
PP1V8_S0
PP1V8_S0_ANALOG_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
C9236 1000PF 10% 16V X7R 201
C9237 1000PF 10% 16V X7R 201
C9238 0.1UF 10% 6.3V XSR 201
C9239 0.1UF 10% 6.3V XSR 201
C9240 OMIT 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 1000PF FOR EACH PIN
L9203
FERR-120-OHM-1.5A
PP3V3_B_S0
PP3V3_S0_ANALOG_SDVO_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
C9230 1000PF 10% 16V X7R 201
C9231 0.1UF 10% 6.3V XSR 201
C9214 1000PF 10% 16V X7R 201
L9204
FERR-120-OHM-1.5A
PP1V8_S0
PP1V8_S0_PVCC1_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
C9232 1000PF 10% 16V X7R 201
C9254 1000PF 10% 16V X7R 201
C9233 0.1UF 10% 6.3V XSR 201
C9206 0.1UF 10% 6.3V XSR 201
TWO 0.1UF AND 1000PF FOR EACH PIN
L9205
FERR-120-OHM-1.5A
PP1V8_S0
PP1V8_S0_PVCC2_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
C9234 1000PF 10% 16V X7R 201
C9235 1000PF 10% 16V X7R 201
C9255 0.1UF 10% 6.3V XSR 201
C9256 0.1UF 10% 6.3V XSR 201
TWO 0.1UF AND 1000PF FOR EACH PIN
L9207
FERR-120-OHM-1.5A
PP3V3_B_S0
PP3V3_S0_SPVCC_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
C9257 1000PF 10% 16V X7R 201
C9258 1000PF 10% 16V X7R 201
C9259 0.1UF 10% 6.3V XSR 201
C9260 0.1UF 10% 6.3V XSR 201
TWO 0.1UF AND 1000PF FOR EACH PIN
L9201
FERR-120-OHM-1.5A
PP1V8_S0
PP1V8_S0_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
C9207 0.1UF 10% 6.3V X5R 201
C9208 1000PF 10% 16V X7R 201
C9209 0.1UF 10% 6.3V X5R 201
C9210 1000PF 10% 16V X7R 201
C9211 0.1UF 10% 6.3V X5R 201
C9212 1000PF 10% 16V X7R 201
C9213 OMIT 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 1000PF FOR EACH PIN
C9250 0.1UF 10% 6.3V X5R 201
C9251 1000PF 10% 16V X7R 201
C9252 0.1UF 10% 6.3V X5R 201
C9253 1000PF 10% 16V X7R 201
C9261 0.1UF 10% 6.3V X5R 201
C9262 1000PF 10% 16V X7R 201
L9200
FERR-120-OHM-1.5A
PP1V8_S0
PP1V8_S0_ANALOG_SDVO_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
C9200 1000PF 10% 16V X7R 201
C9201 1000PF 10% 16V X7R 201
C9202 0.1UF 10% 6.3V X5R 201
C9204 OMIT 10UF 20% 6.3V X5R 603
ONE 1000PF FOR EACH PIN
R9207 49.9 1% 1/20W MF 201
R9237 49.9 1% 1/20W MF 201
TMDS_TX_P<0>
TMDS_TX<0>
TMDS_TX_N<0>
C9222 1000PF 10% 16V X7R 201
R9208 49.9 1% 1/20W MF 201
R9238 49.9 1% 1/20W MF 201
TMDS_TX_P<1>
TMDS_TX<1>
TMDS_TX_N<1>
C9223 1000PF 10% 16V X7R 201
R9209 49.9 1% 1/20W MF 201
R9239 49.9 1% 1/20W MF 201
TMDS_TX_P<2>
TMDS_TX<2>
TMDS_TX_N<2>
C9224 1000PF 10% 16V X7R 201
R9210 49.9 1% 1/20W MF 201
R9240 49.9 1% 1/20W MF 201
TMDS_TX_CLK_P
TMDS_TX_CLK
TMDS_TX_CLK_N
C9225 1000PF 10% 16V X7R 201
PP3V3_B_S0
C9221 0.1UF 10% 6.3V X5R 201
C9205 OMIT 10UF 20% 6.3V X5R 603
PP3V3_S0_SPVCC_TMDS_F
C9290 0.1UF 10% 6.3V X5R 201
PP3V3_B_S0
NO STUFF
R9254 0 5% 1/20W MF 201
CRITICAL
TC7SZ08AFEAPE SOT665
U9290
TMDS_HW_RESET_L
TMDS_SW_RESET_L
PP3V3_S0_SDVCC_TMDS_F
PP1V8_S0_ANALOG_SDVO_F
PP1V8_S0_PVCC2_TMDS_F
PP1V8_S0_PVCC1_TMDS_F
PP1V8_S0_ANALOG_TMDS_F
PP1V8_S0_TMDS_F
VCC
SVCC
PVCC1
PVCC2
AVCC1_8
AVCC3_3
HDAVCC
OVCC
SPVCC
CRITICAL
U9200
SIL1392
QFN
HOST SERIAL DATA RECEIVER CORE
CONFIGURATION /PROGRAMMING
I2C MASTER
AUDIO
LOCAL I2C
DIFFERENTIAL SIGNAL DATA
FACTORY TEST MODE
RESET*
SDSCL
SDSDA
A1
HTPLG
SDADDC
SCLDDC
SDAROM
SCLROM
SPDIF/HDASDO
HDASYNC
HDABCLK
HDASDI
HDARST*
LSCL/DCEN
LSDA/PREEMP
LINT*
TMDS_RST_L
SDVO_CTRLCLK
SDVO_CTRLDATA
ADDRESS=0X70
ADDRESS=0X72 IF A1 IS PULLED HIGH
DVI_HOTPLUG_DET
TMDS_DDC_SDA
TMDS_DDC_SCL
TO TMDS CONNECTOR
NC
TMDS_LSCL
TMDS_LSDA
TMDS_LINT_L
MAKE_BASE=TRUE
GND
SGND
SPGND
AGND
THRM_PAD
MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PLACE THESE CAPS NEAR NB
PEG_R2D_C_N<0>
PEG_R2D_C_P<0>
PEG_R2D_C_N<1>
PEG_R2D_C_P<1>
PEG_R2D_C_N<2>
PEG_R2D_C_P<2>
PEG_R2D_C_N<3>
PEG_R2D_C_P<3>
C9241 0.1UF 10% 6.3V XSR 201
C9242 0.1UF 10% 6.3V XSR 201
C9243 0.1UF 10% 6.3V XSR 201
C9244 0.1UF 10% 6.3V XSR 201
C9245 0.1UF 10% 6.3V XSR 201
C9246 0.1UF 10% 6.3V XSR 201
C9247 0.1UF 10% 6.3V XSR 201
C9248 0.1UF 10% 6.3V XSR 201
R9204 360 5% 1/20W MF 201
TMDS_TX_N<0>
TMDS_TX_P<0>
TMDS_TX_N<1>
TMDS_TX_P<1>
TMDS_TX_N<2>
TMDS_TX_P<2>
TMDS_TX_CLK_N
TMDS_TX_CLK_P
TMDS_EXT_SWING
TMDS_SDR_N
TMDS_SDR_P
TMDS_SDG_N
TMDS_SDG_P
TMDS_SDB_N
TMDS_SDB_P
TMDS_SDC_N
TMDS_SDC_P
TMDS_INT_N
TMDS_INT_P
TMDS_EXT_RES
R9203 1K 1% 1/20W MF 201
DVI_HOTPLUG_DET
"Place R9250 near U2300.F12"
R9250 100K 5% 1/20W MF 201
C9219 0.1UF 10% 6.3V XSR 201
C9220 0.1UF 10% 6.3V XSR 201
PEG_D2R_N<1>
PEG_D2R_P<1>
TMDS CHIP SDVO INPUT INTERRUPT SIGNAL TO MCH
R9251 4.7K 5% 1/20W MF 201
PP3V3_B_S0
PLACE R9200,U9201 CLOSE TO RIO CONN J4200
R9200 10K 5% 1/20W MF 201
TMDS_HTPLG
TMDS_HTPLG_R
5.5V TOL INPUT
R9200 INSURES ESD DIODE CURRENT IS SMALL
R9213 270K 5% 1/20W MF 201
CRITICAL
U9201
74LVC1G17DRL
SOT-553
NC
3.3V ACTIVE OUTPUT
DVI_HOTPLUG_DET_BUF
R9201 2.94K 1% 1/20W MF 201
R9202 2.94K 1% 1/20W MF 201
R9211 9.09K 1% 1/20W MF 201
R9212 9.09K 1% 1/20W MF 201
SDVO_CTRLCLK
SDVO_CTRLDATA
R9253 0 5% 1/20W MF 201
R9252 0 5% 1/20W MF 201
NO STUFF
NO STUFF
SDVO/TMDS Tx
SYNC_MASTER=GRAPHIC
SYNC_DATE=06/06/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7230
REV. B.0.0
SCALE NONE
SHT 61 OF 73

SST8051 microcontroller for HDCP support

PP3V3_B_S0
C9341 0.1UF 10% 6.3V XSR 201
DVI_HOTPLUG_DET_BUF
R9340 10K 5% 1/20W MF 201
U9340 74LVC2G132 US8
C9340 1UF 10% 6.3V CERM 603-1
10MS RC GENERATES ONE-SHOT LOW PULSE ON INT0# TO ALLOW PART TO WAKE UP AND XTAL TO START
L9300 FERR-120-OHM-1.5A 0402-LF
PP3V3_S0_HDCP_F
C9302 0.01UF 10% 10V XSR 201
C9301 0.1UF 10% 6.3V XSR 201
C9300 10UF 20% 6.3V XSR 603
U9300 SST89V54RD WQFN
DVI_HOTPLUG_DET_INT_L
TMDS_LINT_L
TP_SST8051_RXD
SST8051_P34_AUDIO_CONFIG
TP_SST8051_TXD
C9390 22PF 5% 25V NP0-C0G 201
C9391 22PF 5% 25V NP0-C0G 201
Y9390 14.318MHZ-35PPF-20PF SM-2.5X2.0MM
SST8051_XTAL1
SST8051_XTAL2
SST8051_RST
SST8051_EA_L
SST8051_UPDATE_L
SST8051_UPDATE_L
MAKE_BASE=TRUE
SST8051_UPDATE_L pulled up to 10K at SB
SST8051_UPDATE_L
SST8051_DVI_HOTPLUG_DET
SST8051_DDC_CLK
SST8051_DDC_DATA
SST8051_P25_AUDIO_CONFIG
R9302 2.2K 5% 1/20W MF 201
R9303 2.2K 5% 1/20W MF 201
R9304 2.2K 5% 1/20W MF 201
R9305 2.2K 5% 1/20W MF 201
R9306 4.7K 5% 1/20W MF 201
SST8051_DDC_EN
Q9300 SSM6N15FE SOT563
TMDS_DDC_SCL
TMDS_DDC_SDA
TMDS_LSCL
TMDS_LSDA
R9350 0 5% 1/20W MF 201
R9351 0 5% 1/20W MF 201
NO STUFF
SST8051_DVI_HOTPLUG_DET
DVI_HOTPLUG_DET
STUFFING OPTION CHOOSES RAW OR CONTROLLER OUTPUT OF DVI_HOTPLUG_DET
C9326 0.1UF 10% 6.3V XSR 201
U9325 TC7SH00FEF SON
TMDS_HW_RESET_L
SST8051_SW_RESET_L
R9325 10K 1% 1/20W MF 201
R9330 4.7K 1% 1/20W MF 201
R9333 4.7K 1% 1/20W MF 201
R9301 10K 1% 1/20W MF 201
SST8051_EA_L

AUDIO CONFIG OPTIONS

P25	P34	OPTION
0	0	HD AUDIO
0	1	SPDIF
1	0	NO AUDIO
1	1	RESERVED

HDCP uController

SYNC_MASTER= SYNC_DATE=

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE: NONE SHT 62 OF 73

Video Connectors

TMDS(MICRO DVI) INTERFACE
EXTERNAL VIDEO (VGA) INTERFACE

NB VIDEO ALIASES

CRT_TVO_IREF = CRT_TVO_IREF
TV_A_DAC = TV_A_DAC (MAKE_BASE=TRUE)
TV_B_DAC = TV_B_DAC (MAKE_BASE=TRUE)
TV_C_DAC = TV_C_DAC (MAKE_BASE=TRUE)
CRT_BLUE = CRT_BLUE (MAKE_BASE=TRUE)
CRT_GREEN = CRT_GREEN (MAKE_BASE=TRUE)
CRT_RED = CRT_RED (MAKE_BASE=TRUE)
CRT_HSYNC_R = CRT_HSYNC_R (MAKE_BASE=TRUE)
CRT_VSYNC_R = CRT_VSYNC_R (MAKE_BASE=TRUE)

Isolation required for DVI power switch

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

R9469 1.3K 1% 1/20W MF 201 — CRT_TVO_IREF — GND

CRITICAL
F9404 0.5AMP-13.2V SM-LF
PP5V_S0 (VOLTAGE=5V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM) → PP5V_S0_TMDS_FUSE (VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM)

L9444 600-OHM-300MA 0402
PP5V_S0_TMDS_FUSE → PP5V_S0_DVIPORT (VOLTAGE=5V, MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM)

C9404 0.1UF 10% 10V X5R 402 — PP5V_S0_DVIPORT — GND

PP3V3_A_S0

R9466 2.2K 5% 1/20W MF 201 — TV_DCONSEL<0>
R9467 2.2K 5% 1/20W MF 201 — TV_DCONSEL<1>

D9401 1SS418 SOD-723
PP5V_S0_DVIPORT → PP5V_S0_DVIPORT_D (VOLTAGE=5V, MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM)

R9462 1K 5% 1/20W MF 201 — PP5V_S0_DVIPORT_D
R9463 1K 5% 1/20W MF 201 — PP5V_S0_DVIPORT_D

PP3V3_B_S0

R9480 10K 5% 1/20W MF 201 — PP3V3_B_S0 — DVI_HOST
R9481 100K 5% 1/20W MF 201 — HDMI_HOST — DVI_HOST

TMDS_HTPLG (B1)
C9410 1000PF 10% 16V X7R 201 — TMDS_HTPLG — GND

TMDS_DDC_SDA (B1)
NOSTUFF C9411 100PF 5% 25V CERM 201 — TMDS_DDC_SDA — GND

TMDS_DDC_SCL (B1)
NOSTUFF C9412 100PF 5% 25V CERM 201 — TMDS_DDC_SCL — GND

SB_CRT_TVOUT_MUX_L

PLACE R9450 R9451 CLOSE TO NB
R9450 150 1% 1/20W MF 201 — TV_A_DAC
R9451 150 1% 1/20W MF 201 — CRT_BLUE
GND (VOLTAGE=0V)

PLACE U9401 NEAR NB
PP3V3_A_S0
C9439 0.1UF 10% 10V X5R 201 — PP3V3_A_S0 — GND

U9401 FSAV430 DQFN (CRITICAL)
VCC (16)
S (1)
1B1 (2), 1B2 (3), 1A (4)
2B1 (5), 2B2 (6), 2A (7)
OE* (15)
4B1 (14) NC, 4B2 (13) NC, 4A (12) NC
3B1 (11), 3B2 (10), 3A (9)
GND, THMPAD (8, 17) — GND (VOLTAGE=0V)

PLACE R9452 R9453 CLOSE TO NB
R9452 150 1% 1/20W MF 201 — TV_B_DAC
R9453 150 1% 1/20W MF 201 — CRT_GREEN
GND (VOLTAGE=0V)

PLACE R9454 R9455 CLOSE TO NB
R9454 150 1% 1/20W MF 201 — TV_C_DAC
R9455 150 1% 1/20W MF 201 — CRT_RED
GND (VOLTAGE=0V)

EXT_C_R
EXT_Y_G
EXT_COMPVID_B

FL9400 210MHZ MEA2010P-SM (CRITICAL)
EXT_C_R → VGA_B
EXT_Y_G → VGA_G
EXT_COMPVID_B → VGA_R

VGA_B
VGA_G
VGA_R

These nets connect to RIO connector J4200:
TMDS_TX_CONN_P<2>
TMDS_TX_CONN_N<2>
TMDS_TX_CONN_P<1>
TMDS_TX_CONN_N<1>
TMDS_TX_CONN_P<0>
TMDS_TX_CONN_N<0>
TMDS_TX_CONN_CLK_P
TMDS_TX_CONN_CLK_N

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PP3V3_B_S0
C9460 0.1UF 10% 6.3V X5R 201 — PP3V3_B_S0 — GND

CRITICAL U9404 SN74LVC2G125DCU (VCC, GND, OE)

R9460 39 5% 1/20W MF 201 — CRT_HSYNC_R — CRT_HSYNC_LS_R
R9470 39 5% 1/20W MF 201 — CRT_HSYNC_LS — VGA_HSYNC
NOSTUFF C9442 33PF 5% 50V NP0-C0G 201 — VGA_HSYNC — GND

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

CRITICAL U9404 SN74LVC2G125DCU (VCC, GND, OE)

R9461 39 5% 1/20W MF 201 — CRT_VSYNC_R — CRT_VSYNC_LS_R
R9471 39 5% 1/20W MF 201 — CRT_VSYNC_LS — VGA_VSYNC
NOSTUFF C9443 33PF 5% 50V NP0-C0G 201 — VGA_VSYNC — GND

CRITICAL L9405 90-OHM-100MA 1210-4SM1
TMDS_TX_P<2> → TMDS_TX_CONN_P<2>
TMDS_TX_N<2> → TMDS_TX_CONN_N<2>

CRITICAL L9407 90-OHM-100MA 1210-4SM1
TMDS_TX_P<1> → TMDS_TX_CONN_P<1>
TMDS_TX_N<1> → TMDS_TX_CONN_N<1>

CRITICAL L9406 90-OHM-100MA 1210-4SM1
TMDS_TX_P<0> → TMDS_TX_CONN_P<0>
TMDS_TX_N<0> → TMDS_TX_CONN_N<0>

CRITICAL L9404 300-OHM-100MA 1210-4SM
TMDS_TX_CLK_P → TMDS_TX_CONN_CLK_P
TMDS_TX_CLK_N → TMDS_TX_CONN_CLK_N

Place components near J4200 unless otherwise noted

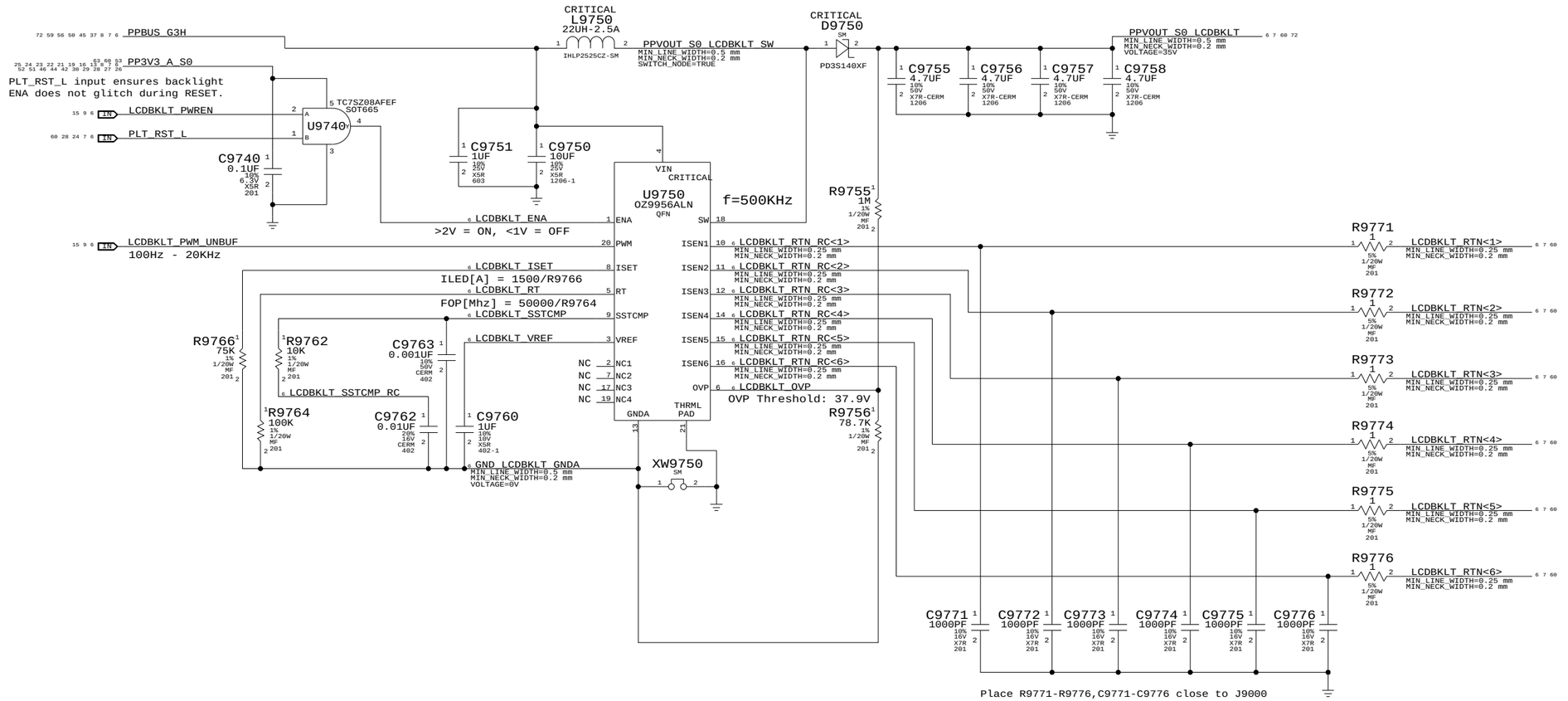
DVI CONNECTIONS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 63 OF 73	

LED Backlight Driver



LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT: 64	OF: 73

ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402

72 52 12 11 8 7 6 PPVCORE_S0_CPU

LAYOUT NOTE:

PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9900 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9901 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9902 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9903 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9904 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9905 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9906 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9907 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9908 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9909 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:

PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9910 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9911 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9912 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9913 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9914 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9915 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9916 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9917 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9918 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9919 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:

PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9920 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9921 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9922 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9923 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9924 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9925 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9926 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9927 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9928 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9929 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:

PLACE ON OPPOSITE SIDE OF CPU

OMIT CRITICAL C9930 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9931 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9932 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9933 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9934 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9935 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9936 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9937 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9938 2.2UF 20% 6.3V CERM 402-LF	OMIT CRITICAL C9939 2.2UF 20% 6.3V CERM 402-LF

ADDITIONAL GPU VCORE HF DECOUPLING

18x 1uF 0402

72 53 45 22 18 8 7 6 PPVCORE_S0_NB_GFX

OMIT 1 C9980 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9981 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9982 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9983 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9984 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9985 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9986 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9987 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9988 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9989 2.2UF 20% 6.3V CERM 402-LF 2

OMIT 1 C9990 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9991 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9992 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9993 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9994 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9995 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9996 2.2UF 20% 6.3V CERM 402-LF 2	OMIT 1 C9997 2.2UF 20% 6.3V CERM 402-LF 2

Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	65	73

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	ISL3,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_4MIL	*	0.100 MM	?
FSB_9MIL	*	0.228 MM	?
FSB_DATA	*	=FSB_4MIL	?
FSB_DATA2DATA	*	=FSB_4MIL	?
FSB_DSTB	*	=FSB_9MIL	?
FSB_DATA2DSTB	*	=FSB_9MIL	?
FSB_ADDR	*	=FSB_4MIL	?
FSB_ADDR2ADDR	*	=FSB_4MIL	?
FSB_ADSTB	*	=FSB_9MIL	?
FSB_ADDR2ADSTB	*	=FSB_9MIL	?
FSB_COMMON	*	=FSB_4MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?
CPU_THERMD	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	6 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	6 10
CPU_FERR_L	CPU_55S		CPU_FERR_L	6 10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	6 10 42 52
CPU_PWRGD	CPU_55S		CPU_PWRGD	6 10 13 23
CPU_FROM_SB	CPU_55S		CPU_INTR	6 10 23
CPU_FROM_SB	CPU_55S		CPU_NMI	6 10 23
CPU_FROM_SB	CPU_55S		CPU_A20M_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	6 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_SMI_L	6 10 23
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	6 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	6 10 16 23 42
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	6 16 25 52
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	6 52
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	6 7 13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	6 7 13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	6 10 30
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	6 7 13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	6 10 16 23 52
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	6 10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	6 10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	6 10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	6 7 10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	6 7 10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	6 7 10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	6 7 10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	6 7 10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	6 7 10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	6 7 10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 71
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 71
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	6 7 13
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	6 11 12 52
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	6 11 52
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	6 11 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	6 52
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	6 52
	CPU_70D	CPU_THERMD	CPU_THERMD_P	6 10 46
	CPU_70D	CPU_THERMD	CPU_THERMD_N	6 10 46

CPU/FSB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 66 OF 73	

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
PCIE_R2D_2_PCIE_R2D	*	0.228 MM	?
PCIE_D2R_2_PCIE_D2R	*	0.228 MM	?
PCIE_R2D_2_PCIE_D2R	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_N2S_2_DMI_N2S	*	0.228 MM	?
DMI_S2N_2_DMI_S2N	*	0.228 MM	?
DMI_N2S_2_DMI_S2N	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_R2D_2_PCIE_R2D
PCIE_D2R	PCIE_D2R	*	PCIE_D2R_2_PCIE_D2R
PCIE_R2D	PCIE_D2R	*	PCIE_R2D_2_PCIE_D2R

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_N2S_2_DMI_N2S
DMI_S2N	DMI_S2N	*	DMI_S2N_2_DMI_S2N
DMI_N2S	DMI_S2N	*	DMI_N2S_2_DMI_S2N

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PWR	*	BUS2PWR_GND
PCIE_R2D	GND	*	BUS2PWR_GND
PCIE_D2R	PWR	*	BUS2PWR_GND
PCIE_D2R	GND	*	BUS2PWR_GND
DMI_N2S	PWR	*	BUS2PWR_GND
DMI_N2S	GND	*	BUS2PWR_GND
DMI_S2N	PWR	*	BUS2PWR_GND
DMI_S2N	GND	*	BUS2PWR_GND
LVDS	PWR	*	BUS2PWR_GND
LVDS	GND	*	BUS2PWR_GND
TMDS	PWR	*	BUS2PWR_GND
TMDS	GND	*	BUS2PWR_GND

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?
LVDS2LVDS	*	0.300 MM	?
TMDS	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC
LVDS	LVDS	*	LVDS2LVDS

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PEG_R2D	PCIE_100D	PCIE_R2D	PEG_R2D_P<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_N<15..0>	
	PCIE_100D	PCIE_R2D	PEG_R2D_C_P<15..0>	6 15 61
	PCIE_100D	PCIE_R2D	PEG_R2D_C_N<15..0>	6 15 61
PEG_D2R	PCIE_100D	PCIE_D2R	PEG_D2R_P<15..0>	6 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_N<15..0>	6 15 61
	PCIE_100D	PCIE_D2R	PEG_D2R_C_P<15..0>	
	PCIE_100D	PCIE_D2R	PEG_D2R_C_N<15..0>	
DMI_N2S	DMI_100D	DMI_N2S	DMI_N2S_P<3..0>	6 16 24
	DMI_100D	DMI_N2S	DMI_N2S_N<3..0>	6 16 24
DMI_S2N	DMI_100D	DMI_S2N	DMI_S2N_P<3..0>	6 16 24
	DMI_100D	DMI_S2N	DMI_S2N_N<3..0>	6 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	6 15 60
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	6 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	6 7 15 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_P<2..0>	6 60
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_F_N<2..0>	6 60
LVDS_A_DATA3	LVDS_100D	LVDS	NC_LVDS_A_DATA_P3	9
LVDS_A_DATA3	LVDS_100D	LVDS	NC_LVDS_A_DATA_N3	9
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_P	9 15
LVDS_B_CLK	LVDS_100D	LVDS	NC_LVDS_B_CLK_N	9 15
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	
LVDS_B_DATA3	LVDS_100D	LVDS	NC_LVDS_B_DATA_P3	9
LVDS_B_DATA3	LVDS_100D	LVDS	NC_LVDS_B_DATA_N3	9
LVDS_IBG		LVDS	LVDS_IBG	6 15 60
CRT_TVO_IREF		CRT	CRT_TVO_IREF	6 15 63
CRT_RED	CRT_50S	CRT	CRT_RED	6 15 63
CRT_GREEN	CRT_50S	CRT	CRT_GREEN	6 15 63
CRT_BLUE	CRT_50S	CRT	CRT_BLUE	6 15 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R	6 15 63
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R	6 15 63
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC	6 15 63
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC	6 15 63
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC	6 15 63
EXT_COMPVID_B	CRT_50S	CRT	EXT_COMPVID_B	6 63
EXT_Y_G	CRT_50S	CRT	EXT_Y_G	6 63
EXT_C_R	CRT_50S	CRT	EXT_C_R	6 63
VGA_R	CRT_50S	CRT	VGA_R	6 7 37 63
VGA_G	CRT_50S	CRT	VGA_G	6 7 37 63
VGA_B	CRT_50S	CRT	VGA_B	6 7 37 63
	PCIE_100D	PCIE_R2D	TMDS_SDB_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDB_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDC_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDG_N	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_P	6 61
	PCIE_100D	PCIE_R2D	TMDS_SDR_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CLK_P	6 61 63
	TMDS_100D	TMDS	TMDS_TX_CLK_N	6 61 63
	PCIE_100D	PCIE_D2R	TMDS_INT_P	6 61
	PCIE_100D	PCIE_D2R	TMDS_INT_N	6 61
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_P	6 7 37 63
	TMDS_100D	TMDS	TMDS_TX_CONN_CLK_N	6 7 37 63
	TMDS_100D	TMDS	TMDS_CONN_P<3..0>	
	TMDS_100D	TMDS	TMDS_CONN_N<3..0>	
	TMDS_100D	TMDS	TMDS_TX_P<3..0>	6 61 63
	TMDS_100D	TMDS	TMDS_TX_N<3..0>	6 61 63
	SMB_55S	SMB	TMDS_DDC_SCL	6 7 37 61 62 63
	SMB_55S	SMB	TMDS_DDC_SDA	6 7 37 61 62 63

NB Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 67 OF 73	

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	ISL3,ISL10	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_87D	*	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF	=87_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	NB_STATIC	*	PWR_P2MM
MEM_CTRL	NB_STATIC	*	PWR_P2MM
MEM_DATA	NB_STATIC	*	PWR_P2MM
MEM_DQS	NB_STATIC	*	PWR_P2MM
MEM_CMD	NB_STATIC	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	MEM_87D	MEM_CLK	MEM_CLK_P<2..0> 16 31 33
	MEM_87D	MEM_CLK	MEM_CLK_N<2..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_CKE<1..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_CS_L<1..0> 16 31 33
	MEM_45S	MEM_CTRL	MEM_ODT<1..0> 6 16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<13..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0> 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L 17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0> 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8> 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16> 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24> 17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32> 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40> 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48> 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56> 17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0> 17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1> 17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2> 17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3> 17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4> 17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5> 17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6> 17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7> 17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0> 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1> 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2> 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3> 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4> 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5> 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6> 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7> 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7> 17 31
	MEM_87D	MEM_CLK	MEM_CLK_P<5..3> 16 32 33
	MEM_87D	MEM_CLK	MEM_CLK_N<5..3> 16 32 33
	MEM_45S	MEM_CTRL	MEM_CKE<4..3> 16 32 33
	MEM_45S	MEM_CTRL	MEM_CS_L<3..2> 16 32 33
	MEM_45S	MEM_CTRL	MEM_ODT<3..2> 6 16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<13..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0> 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L 17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0> 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8> 17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16> 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24> 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32> 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40> 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48> 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56> 17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0> 17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1> 17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2> 17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3> 17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4> 17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5> 17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6> 17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7> 17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0> 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1> 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2> 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3> 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4> 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5> 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6> 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7> 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7> 17 32

R93	PP0V9_S3M_MEM_NBVREFB	NET_SPACING_TYPE=NB_STATIC 8 16 21
R95	PP0V9_S3M_MEM_NBVREFA	NET_SPACING_TYPE=NB_STATIC 8 16 21
R94	NB_VCCSM_LF1	NET_SPACING_TYPE=NB_STATIC 6 18
R96	NB_VCCSM_LF2	NET_SPACING_TYPE=NB_STATIC 6 18
R97	NB_VCCSM_LF3	NET_SPACING_TYPE=NB_STATIC 6 18
R98	NB_VCCSM_LF4	NET_SPACING_TYPE=NB_STATIC 6 18
R99	NB_VCCSM_LF5	NET_SPACING_TYPE=NB_STATIC 6 18
R101	NB_VCCSM_LF6	NET_SPACING_TYPE=NB_STATIC 6 18
R100	NB_VCCSM_LF7	NET_SPACING_TYPE=NB_STATIC 6 18
R102	PP1V8_S3	NET_SPACING_TYPE=PP1V8_MEM 6 7 8 16 18 21 31 32 34 35 51 55 72
	GND	NET_SPACING_TYPE=GND

Memory Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 68 OF 73	

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	PWR	*	BUS2PWR_GND
USB	GND	*	BUS2PWR_GND

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 6 23 38
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 6 23 38
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L 6 23 38
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L 6 23 38
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ 6 23 38
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 6 23 38
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 6 23 38
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L
SATA_A_R2D	SATA_100D	SATA	NC_SATA_A_R2D_C_P 9 23
	SATA_100D	SATA	NC_SATA_A_R2D_C_N 9 23
	SATA_100D	SATA	SATA_A_R2D_P
	SATA_100D	SATA	SATA_A_R2D_N
SATA_A_D2R	SATA_100D	GND	NC_SATA_A_D2R_P 9
	SATA_100D	GND	NC_SATA_A_D2R_N 9
	SATA_100D	SATA	SATA_A_D2R_C_P
	SATA_100D	SATA	SATA_A_D2R_C_N
SATA_B_R2D	SATA_100D	SATA	NC_SATA_B_R2D_C_P 9 23
	SATA_100D	SATA	NC_SATA_B_R2D_C_N 9 23
	SATA_100D	SATA	SATA_B_R2D_P
	SATA_100D	SATA	SATA_B_R2D_N
SATA_A_D2R	SATA_100D	GND	NC_SATA_B_D2R_P 9
	SATA_100D	GND	NC_SATA_B_D2R_N 9
	SATA_100D	SATA	SATA_B_D2R_C_P
	SATA_100D	SATA	SATA_B_D2R_C_N
SATA_C_R2D	SATA_100D	SATA	NC_SATA_C_R2D_C_P 9 23
	SATA_100D	SATA	NC_SATA_C_R2D_C_N 9 23
	SATA_100D	SATA	SATA_C_R2D_P
	SATA_100D	SATA	SATA_C_R2D_N
SATA_A_D2R	SATA_100D	GND	NC_SATA_C_D2R_P 9
	SATA_100D	GND	NC_SATA_C_D2R_N 9
	SATA_100D	SATA	SATA_C_D2R_C_P
	SATA_100D	SATA	SATA_C_D2R_C_N
SATA_RBIAS	SATA_55S		SATA_RBIAS
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 6 7 9 23 37
	HDA_55S	HDA	HDA_BIT_CLK_R 6 23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 6 7 9 23 37
	HDA_55S	HDA	HDA_SYNC_R 6 23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 6 9 23 37
	HDA_55S	HDA	HDA_RST_L_R 6 23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 6 7 9 23 37
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 6 7 9 23 37
	HDA_55S	HDA	HDA_SDOUT_R 6 23
USB_EXTA	USB_90D	USB	USB2_EXTA_P 6 9 24 39
	USB_90D	USB	USB2_EXTA_N 6 9 24 39
	USB_90D	USB	USB2_MUXED_EXTA_N 6 9 39
	USB_90D	USB	USB2_MUXED_EXTA_P 6 9 39
USB_MINI	USB_90D	USB	USB2_AIRPORT_P 6 9 24 36
	USB_90D	USB	USB2_AIRPORT_N 6 9 24 36
USB_EXTD	USB_90D	USB	TP_USB2_3G_P 9 24
	USB_90D	USB	TP_USB2_3G_N 9 24
USB_CAMERA	USB_90D	USB	USB2_CAMERA_P 6 9 24 60
	USB_90D	USB	USB2_CAMERA_N 6 9 24 60
USB_BT	USB_90D	USB	NC_USB_BT_P 9 24
	USB_90D	USB	NC_USB_BT_N 9 24
USB_TPAD	USB_90D	USB	USB2_WSPRING_P 6 7 9 24 40
	USB_90D	USB	USB2_WSPRING_N 6 7 9 24 40
USB_IR	USB_90D	USB	USB_IR_P 6 7 9 24 40
	USB_90D	USB	USB_IR_N 6 7 9 24 40
USB_EXTB	USB_90D	USB	NC_USB2_EXTB_P 9 24
	USB_90D	USB	NC_USB2_EXTB_N 9 24
USB_EXCARD	USB_90D	USB	TP_USB_EXCARD_P 9 24
	USB_90D	USB	TP_USB_EXCARD_N 9 24
USB_EXTC	USB_90D	USB	TP_USB_EXTC_P 9 24
	USB_90D	USB	TP_USB_EXTC_N 9 24
	USB_90D	USB	USB2_AIRPORT_P_F 6 36
	USB_90D	USB	USB2_AIRPORT_N_F 6 36
	USB_90D	USB	USB2_CAMERA_F_P 6 7 60
	USB_90D	USB	USB2_CAMERA_F_N 6 7 60
	USB_90D	USB	USB2_EXTA_F_P 6 7 37 39
	USB_90D	USB	USB2_EXTA_F_N 6 7 37 39
			USB2_3G_F_P
			USB2_3G_F_N
USB_RBIAS	USB_60S		USB_RBIAS 6 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL 6 25 29 44
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA 6 25 29 44
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL 6 25 44
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA 6 25 44
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 6 24 49
	SPI_55S	SPI	SPI_SCLK
	SPI_55S	SPI	SPI_A_SCLK_R 6 43 49
	SPI_55S	SPI	SPI_B_SCLK_R
SPI_SI	SPI_55S	SPI	SPI_SI_R 6 24 49
	SPI_55S	SPI	SPI_SI
	SPI_55S	SPI	SPI_A_SI_R 6 43 49
	SPI_55S	SPI	SPI_B_SI_R
SPI_SO	SPI_55S	SPI	SPI_SO 6 24 43 49
	SPI_55S	SPI	SPI_A_SO_R 6 49
	SPI_55S	SPI	SPI_B_SO
	SPI_55S	SPI	SPI_B_SO_R
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 6 24 49
	SPI_55S	SPI	SPI_CE_L<0> 6 43 49
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1> 6 24 43
	SPI_55S	SPI	SPI_CE_L<1>

SB Constraints (1 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 69 OF 73	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?
PCIE_R2D	*	=PCIE	?
PCIE_D2R	*	=PCIE	?
PCIE_9MIL	*	0.228 MM	?
PCIE_12MIL	*	0.300 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_R2D	PCIE_R2D	*	PCIE_9MIL
PCIE_D2R	PCIE_D2R	*	PCIE_9MIL
PCIE_D2R	PCIE_R2D	*	PCIE_12MIL

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PCI_AD	PCI_5SS	PCI	PCI_AD<18..0> 9
PCI_AD19	PCI_5SS	PCI	NC_PCI_AD<19> 9 24
PCI_AD20	PCI_5SS	PCI	NC_PCI_AD<20> 9 24
PCI_AD	PCI_5SS	PCI	PCI_AD<31..21> 9
PCI_AD	PCI_5SS	PCI	NC_PCI_PAR 9 24
PCI_C_BE_L	PCI_5SS	PCI	PCI_C_BE_L<3..0> 9
PCI_CNTL	PCI_5SS	PCI	PCI_IRDY_L 6 24
PCI_CNTL	PCI_5SS	PCI	PCI_DEVSEL_L 6 24
PCI_CNTL	PCI_5SS	PCI	PCI_PERR_L 6 24
PCI_LOCK_L	PCI_5SS	PCI	PCI_LOCK_L 6 24
PCI_CNTL	PCI_5SS	PCI	PCI_SERR_L 6 24
PCI_CNTL	PCI_5SS	PCI	PCI_STOP_L 6 24
PCI_CNTL	PCI_5SS	PCI	PCI_TRDY_L 6 24
PCI_CNTL	PCI_5SS	PCI	PCI_FRAME_L 6 24
PCI_FW_REQ_L	PCI_5SS	PCI	PCI_FW_REQ_L 6 24
PCI_FW_GNT_L	PCI_5SS	PCI	PCI_FW_GNT_L 6 24
PCI_REQ1_L	PCI_5SS	PCI	PCI_REQ1_L 6 24
PCI_GNT1_L	PCI_5SS	PCI	PCI_GNT1_L
PCI_REQ2_L	PCI_5SS	PCI	PCI_REQ2_L 6 24
PCI_GNT2_L	PCI_5SS	PCI	PCI_GNT2_L
INT_PIRQA_L	PCI_5SS	PCI	INT_PIRQA_L 6 24
INT_PIRQB_L	PCI_5SS	PCI	INT_PIRQB_L 6 24
INT_PIRQC_L	PCI_5SS	PCI	INT_PIRQC_L 6 24
INT_PIRQD_L	PCI_5SS	PCI	INT_PIRQD_L 6 24
INT_PIRQE_L	PCI_5SS	PCI	INT_PIRQE_L 6 24
INT_PIRQF_L	PCI_5SS	PCI	INT_PIRQF_L 6 24
PCIE_A_R2D	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_A_R2D_C_N
PCIE_A_D2R	PCIE_100D	PCIE_D2R	PCIE_A_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_A_D2R_N
PCIE_B_R2D	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_P
	PCIE_100D	PCIE_R2D	PCIE_B_R2D_C_N
PCIE_B_D2R	PCIE_100D	PCIE_D2R	PCIE_B_D2R_P
	PCIE_100D	PCIE_D2R	PCIE_B_D2R_N
			PCIE_EXCARD_R2D_C_P
			PCIE_EXCARD_R2D_C_N
			PCIE_EXCARD_D2R_P
			PCIE_EXCARD_D2R_N
			PCIE_FW_R2D_C_P
			PCIE_FW_R2D_C_N
			PCIE_FW_D2R_P
			PCIE_FW_D2R_N
PCIE_MINI_R2D	PCIE_100D	PCIE_R2D	PCIE_E_R2D_C_P 6 24 36
	PCIE_100D	PCIE_R2D	PCIE_E_R2D_C_N 6 24 36
PCIE_MINI_D2R	PCIE_100D	PCIE_D2R	PCIE_E_D2R_P 6 24 36
	PCIE_100D	PCIE_D2R	PCIE_E_D2R_N 6 24 36
			PCIE_ENET_R2D_C_P
			PCIE_ENET_R2D_C_N
			PCIE_ENET_D2R_P
			PCIE_ENET_D2R_N
GLAN_COMP			GLAN_COMP 6 23
ENET_KBIAS			NINEVEH_KBIAS_P
ENET_RBIAS			NINEVEH_RBIAS
(PCIE_ENET_R2D)	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_R2D_N
(PCIE_ENET_D2R)	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_P
	GLAN_100D	ENET_GLAN	ENET_GLAN_D2R_C_N
ENET_LAN	LAN_5SS	ENET_LAN	LAN_RSTSYNC
ENET_LAN	LAN_5SS	ENET_LAN	LAN_R2D<2..0>
ENET_LAN	LAN_5SS	ENET_LAN	LAN_D2R<2..0>
ENET_GLAN_CLK	LAN_5SS	ENET_CLK	ENET_GLAN_CLK_R
	LAN_5SS	ENET_CLK	ENET_GLAN_CLK
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>
	ENET_100D	ENET_MDI	ENET_MDI_N<0>
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>
	ENET_100D	ENET_MDI	ENET_MDI_N<1>
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>
	ENET_100D	ENET_MDI	ENET_MDI_N<2>
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>
	ENET_100D	ENET_MDI	ENET_MDI_N<3>
CLINK_NB	CLINK_5SS	CLINK	CLINK_NB_CLK 6 16 25
CLINK_NB	CLINK_5SS	CLINK	CLINK_NB_DATA 6 16 25
CLINK_NB_RESET_L	CLINK_5SS	CLINK	CLINK_NB_RESET_L 6 16 25
CLINK_WLAN	CLINK_5SS	CLINK	CLINK_WLAN_CLK
CLINK_WLAN	CLINK_5SS	CLINK	CLINK_WLAN_DATA
CLINK_WLAN_RESET_L	CLINK_5SS	CLINK	CLINK_WLAN_RESET_L
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF 6 16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0 6 25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1 6 25

SB Constraints (2 of 2)

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 70 OF 73	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	PWR	*	BUS2PWR_GND
CLK_FSB	GND	*	BUS2PWR_GND
CLK_PCIE	PWR	*	BUS2PWR_GND
CLK_PCIE	GND	*	BUS2PWR_GND
CLK_MED	PWR	*	BUS2PWR_GND
CLK_MED	GND	*	BUS2PWR_GND

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
CK505_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
CK505_NB	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	6 29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	6 29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	6 10 29 30 71
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	6 10 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	6 14 29 30 71
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	6 14 29 30 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	6 7 13 29 30 66 71
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	6 7 13 29 30 66 71
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6 30 43
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	6 24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	6 30 41
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	6 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	6 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	6 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	6 30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	6 9 16 29 30 71
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	6 9 16 29 30 71
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	6 9 16 29 30 71
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	6 9 16 29 30 71
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	6 24 29 30 71
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	6 24 29 30 71
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_P	
(CK505_SRC4)	SATA_100D	GND	SB_CLK100M_SATA_N	
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	6 16 29 30 71
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	6 16 29 30 71
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	6 29 30 36 71
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	6 29 30 36 71
			CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	6 7 36 40 41 44
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	6 7 36 40 41 44
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	6 7 41 44 46
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	6 7 41 44 46
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	6 7 41 44 50 59
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	6 7 41 44 50 59
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	6 41 44 48
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	6 41 44 48

Clock & SMC Constraints

SYNC_MASTER=T9 SYNC_DATE=01/30/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE NONE SHT 71 OF 73

1	PPBUS_G3H	NET_SPACING_TYPE=PWR	6 7 8 37 45 50 56 59 64
2	PPBUS_R_G3H	NET_SPACING_TYPE=PWR	6 7 8 42 52 53 54 55 59
3	PPDCIN_G3H	NET_SPACING_TYPE=PWR	6 7 8 50 57
4	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR	6 50
5	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR	6 50
6	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR	6 59
7	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR	6 59
8	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR	6 59
10	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR	6 59
9	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR	6 7 8 11 12 52 65
12	PPVCORE_S0_NB_GFX	NET_SPACING_TYPE=PWR	6 7 8 18 22 45 53 65
11	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR	6 45 59
13	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR	6 59
14	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR	6 59
16	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR	6 59
15	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR	6 52
18	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR	6 7 60 64
17	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR	6 64
19	PP0V9_S0	NET_SPACING_TYPE=PWR	6 7 8 33 55
21	PP0V9_S3	NET_SPACING_TYPE=PWR	6 8 31 32 55
20	PP1V5_S0	NET_SPACING_TYPE=PWR	6 7 8 11 12 22 26 27 54
23	PP1V5_S0_NB_QDAC	NET_SPACING_TYPE=PWR	6 22
160	PP1V5_S0_NB_VCCD_CRT	NET_SPACING_TYPE=PWR	6 19 22
161	PP1V5_S0_NB_VCCD_QDAC	NET_SPACING_TYPE=PWR	6 19 22
22	PP1V5_S0_NB_VCCDMIPLL	NET_SPACING_TYPE=PWR	
24	PP1V5_S0_NB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR	
25	PP1V5_S0_SB_VCCDMIPLL	NET_SPACING_TYPE=PWR	6 26 27
26	PP1V5_S0_SB_VCCDMIPLL_F	NET_SPACING_TYPE=PWR	6 27
28	PP1V5_S0_SB_VCCSATAPLL	NET_SPACING_TYPE=PWR	6 26 27
27	PP1V5_S0_SB_VCC1_5_B	NET_SPACING_TYPE=PWR	6 23 24 26 27
30	PP1V8_S0	NET_SPACING_TYPE=PWR	6 7 8 19 22 51 61
29	PP1V8_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR	6 61
31	PP1V8_S0_ANALOG_TMDS_F	NET_SPACING_TYPE=PWR	6 61
33	PP1V8_S0_NB_VCCTXLVDS	NET_SPACING_TYPE=PWR	6 19 22
32	PP1V8_S0_PVCC1_TMDS_F	NET_SPACING_TYPE=PWR	6 61
35	PP1V8_S0_PVCC2_TMDS_F	NET_SPACING_TYPE=PWR	6 61
34	PP1V8_S0_TMDS_F	NET_SPACING_TYPE=PWR	6 61
36	PP1V8_S3	NET_SPACING_TYPE=PWR	6 7 8 16 18 21 31 32 34 35 51 55 68
38	PP1V8_S3M_NB_VCCSMCK	NET_SPACING_TYPE=PWR	6 19 21
37	PP1V8_S3_NB_VCCSMCK_RC	NET_SPACING_TYPE=PWR	6 21
39	PP1V05_S0	NET_SPACING_TYPE=PWR	6 7 8 10 11 12 13 14 18 19 21 23 26 27 38 42 54
41	PP1V05_S0_NB_VCCPEG	NET_SPACING_TYPE=PWR	6 15 19 21
140	PP1V25_S0	NET_SPACING_TYPE=PWR	6 7 8 16 18 19 21 26 27 51 57
143	PP1V25_S0M_NB_VCCA_HPLL	NET_SPACING_TYPE=PWR	6 19 21
142	PP1V25_S0_NB_DPLL	NET_SPACING_TYPE=PWR	6 22
144	PP1V25_S0_NB_PEGPLL	NET_SPACING_TYPE=PWR	6 19 21
146	PP1V25_S0_NB_PEGPLL_RC	NET_SPACING_TYPE=PWR	6 21
145	PP1V25_S0_NB_VCCA_DPLLA	NET_SPACING_TYPE=PWR	6 19 22
148	PP1V25_S0_NB_VCCA_DPLLB	NET_SPACING_TYPE=PWR	6 19 22
147	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR	6 60
149	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR	6 7 60
150	PP3V3_S0	NET_SPACING_TYPE=PWR	7
152	PP3V3_S0_ANALOG_SDVO_F	NET_SPACING_TYPE=PWR	6 61
151	PP3V3_S0_CK505_VDDA	NET_SPACING_TYPE=PWR	6
154	PP3V3_S0_CK505_VDDA_R	NET_SPACING_TYPE=PWR	6
153	PP3V3_S0_CK505_VDD_CPU_SRC	NET_SPACING_TYPE=PWR	6 29
155	PP3V3_S0_CK505_VDD_PCI	NET_SPACING_TYPE=PWR	6
157	PP3V3_S0_CK505_VDD_REF	NET_SPACING_TYPE=PWR	6
156	PP3V3_S0_CK505_VDD48	NET_SPACING_TYPE=PWR	6
159	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR	6 52
158	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR	6 7 60
160	PP3V3_S0_NBCORE_FOLLOW_R	NET_SPACING_TYPE=PWR	6 21
162	PP3V3_S0_NB_CRTDAC_F	NET_SPACING_TYPE=PWR	6 22
161	PP3V3_S0_NB_TVDAC	NET_SPACING_TYPE=PWR	6 22
163	PP3V3_S0_NB_TVDAC_F	NET_SPACING_TYPE=PWR	6 22
165	PP3V3_S0_NB_TVDAC_FOLLOW	NET_SPACING_TYPE=PWR	6 22
164	PP3V3_S0_NB_VCCA_CRTDAC	NET_SPACING_TYPE=PWR	6 19 22
167	PP3V3_S0_NB_VCCA_DAC_BG	NET_SPACING_TYPE=PWR	6 19 22
166	PP3V3_S0_NB_VCCA_TVDACA	NET_SPACING_TYPE=PWR	6 19 22
168	PP3V3_S0_NB_VCCA_TVDACB	NET_SPACING_TYPE=PWR	6 19 22
170	PP3V3_S0_NB_VCCA_TVDACC	NET_SPACING_TYPE=PWR	6 19 22
169	PP3V3_S0_SPVCC_TMDS_F	NET_SPACING_TYPE=PWR	6 61
172	PP3V3_S3	NET_SPACING_TYPE=PWR	6 7 8 36 42 44 48 51 58 60
171	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR	6 7 36
173	PP3V3_S3_TOPCASE_F	NET_SPACING_TYPE=PWR	
174	PP3V3_S5	NET_SPACING_TYPE=PWR	6 7 16 24 25 26 27 28 36 43 44 49 51 52 57 58 60
176	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR	6 41 42
175	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR	6 41
178	PP3V42G3H_SW	NET_SPACING_TYPE=PWR	6 57
177	PP3V42_G3H	NET_SPACING_TYPE=PWR	6 7 8 23 26 27 28 39 40 41 42 43 44 57 59
179	PP3V42_G3H_SMC_F	NET_SPACING_TYPE=PWR	
181	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR	6 39
180	PP4V5_AUDIO_ANALOG	NET_SPACING_TYPE=PWR	
183	PP5V_S0	NET_SPACING_TYPE=PWR	6 7 8 22 27 40 43 47 51 52 53 63
182	PP5V_S0_AUDIO	NET_SPACING_TYPE=PWR	
184	PP5V_S0_AUDIO_AMP	NET_SPACING_TYPE=PWR	
186	PP5V_S0_DVIPORT	NET_SPACING_TYPE=PWR	6 7 37 63
185	PP5V_S0_DVIPORT_D	NET_SPACING_TYPE=PWR	6 63
187	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR	6 52
189	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR	6 7 40
188	PP5V_S0_SB_V5REF	NET_SPACING_TYPE=PWR	6 26 27
191	PP5V_S0_TMDS_FUSE	NET_SPACING_TYPE=PWR	6 63
190	PP5V_S0_3G_F	NET_SPACING_TYPE=PWR	
192	PP5V_S3	NET_SPACING_TYPE=PWR	6 7 8 40 58 60
194	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR	6 7 60
193	PP5V_S3_IR_F	NET_SPACING_TYPE=PWR	
196	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR	6 39
195	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR	6 7 37 39
197	PP5V_S5	NET_SPACING_TYPE=PWR	6 7 8 27 39 51 54 55 56 58
198	PP5V_S5_SB_V5REF_SUS	NET_SPACING_TYPE=PWR	6 26 27
199	PP18V5_DCIN	NET_SPACING_TYPE=PWR	6 7 50
1102	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR	6 50
1103	PP18V5_G3H	NET_SPACING_TYPE=PWR	6 7 8 50 59
1104	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR	6 59

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M82 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0
SCALE: NONE	SHT 72 OF 73	

M82 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL2,ISL4,ISL5	Y	0.215 MM	0.215 MM			
27P4_OHM_SE	ISL10,ISL11,ISL13	Y	0.215 MM	0.215 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.290 MM	0.290 MM			
45_OHM_SE	ISL2,ISL4,ISL5	Y	0.091 MM	0.091 MM			
45_OHM_SE	ISL10,ISL11,ISL13	Y	0.091 MM	0.091 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.235 MM	0.235 MM			
50_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM			
50_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.190 MM			
55_OHM_SE	ISL2,ISL4,ISL5	Y	0.070 MM	0.070 MM	55OHM SE ON INTERNAL LAYERS NOT ACHIEVABLE IN M82 STACKUP USING 50OHM SE		
55_OHM_SE	ISL10,ISL11,ISL13	Y	0.070 MM	0.070 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.310 MM	0.310 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.230 MM	0.230 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM
85_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.090 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
87_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
87_OHM_DIFF	TOP,BOTTOM	Y	0.220 MM	0.220 MM		0.180 MM	0.180 MM
87_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM
87_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.082 MM	0.082 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.190 MM	0.190 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.170 MM		0.205 MM	0.205 MM
100_OHM_DIFF	ISL2,ISL4,ISL5	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

M82 Rule Definitions

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7230	B.0.0

SCALE	SHT	OF
NONE	73	73