1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT

REV. A

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001052699	PRODUCTION RELEASED	2011-01-10

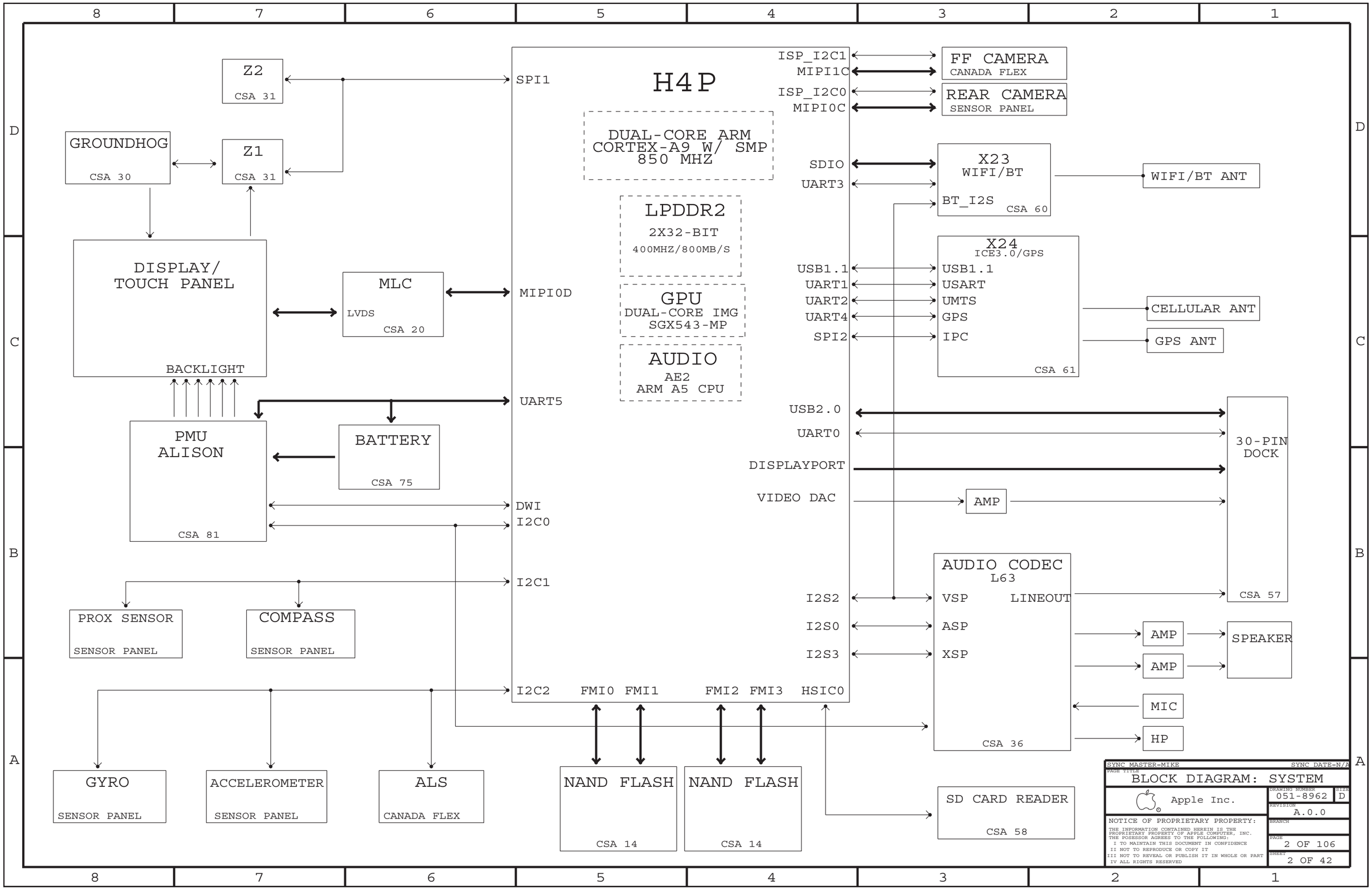
PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	MIKE	N/A
2	2	BLOCK DIAGRAM: SYSTEM	MIKE	N/A
3	5	BOM TABLE	MIKE	N/A
4	6	AP: MAIN	JAMES	N/A
5	7	AP: I/Os	JAMES	N/A
6	8	AP: NAND	JAMES	N/A
7	9	AP: TV,DP,MIPI	JAMES	N/A
8	10	AP: PWR	JAMES	N/A
9	11	AP: PWR	JAMES	N/A
10	12	AP: MISC & ALIASES	JAMES	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES	JAMES	N/A
12	14	NAND	JONATHAN	N/A
13	17	VIDEO: DISPLAY PORT	JAMES	N/A
14	20	VIDEO: MLC	MIKE	N/A
15	21	VIDEO: MLC ALIASES	MIKE	N/A
16	22	VIDEO: LVDS CONNECTOR	ALEX	N/A
17	30	GRAPE: GROUNDHOG,CONN,BOOST	RAMSIN	N/A
18	31	GRAPE: Z1, Z2	RAMSIN	N/A
19	36	AUDIO: L63 CODEC	LENG	N/A
20	37	AUDIO: SPEAKER AMP	LENG	N/A
21	38	AUDIO: HEADPHONE OUT	LENG	N/A
22	39	AUDIO: BLANK	LENG	N/A
23	42	AUDIO: DETECT/MIC BIAS	LENG	N/A
24	43	AUDIO: HP/MIC FILTERS	LENG	N/A
25	54	CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES	MARK B.	N/A
26	55	CONNECTOR: CANADA FLEX FILTERS	MARK B.	N/A
27	56	CONNECTOR: SENSOR PANEL CONNECTOR	MARK B.	N/A
28	57	IO FLEX: DOCK COMPONENTS	JAMES	N/A
29	59	IO FELX: B2B Connector	JAMES	N/A
30	60	CONNECTOR: X23 WIFI/BT	MIKE	N/A
31	61	CONNECTOR: X24 CELLULAR/GPS	MIKE	N/A
32	73	POWER: ALIASES	YOSH	N/A
33	75	POWER: BATTERY CONNECTOR	YOSH	N/A
34	81	POWER: PMU	YOSH	N/A
35	82	POWER: PMU	YOSH	N/A
36	83	POWER: 3.3V VR	YOSH	N/A
37	90	DEBUG AND MISC	MIKE	N/A
38	93	FCT/ICT TEST/BRACKETS	MIKE	N/A
39	100	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A
40	101	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A
41	102	CONSTRAINTS: MLB RULES	MIKE	N/A
42	106	CONSTRAINTS: RF RULES	MIKE	N/A

_DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE: CHOPIN MLB

Apple Inc.

DRAWING NUMBER: 051-8962 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 106
SHEET: 1 OF 42



SYNC MASTER=MIKE
SYNC DATE=N/A
PAGE TITLE
BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-8962
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD

BKLT_PLL

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP
JTAG_TAP_NOT

SPEAKER
INTERNAL_MIC

PORTRAIT_DOCK

MLC_DEV
MLC_PROD

K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH,CHOPIN_AUDIO,MLB,K94	SCH1	
820-3069	1	PCBF,CHOPIN_AUDIO,MLB,K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE,GRAPE,MLB,K93/K94	FENCE1	
806-1397	1	CAN,GRAPE,MLB,K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE,CPU,MLB,K93/K94	FENCE2	
806-1399	1	CAN,CPU,MLB,K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE,NAND,MLB,K93/K94	FENCE3	
806-1401	1	CAN,NAND,MLB,K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DFC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DFC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DFC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
BOM TABLE

Apple Inc.

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION

U0652
H4P-512MB
BGA
SYM 11 OF 12
SC58940X01-A030

AU14 AU15 AU16 AU17 AV1 AV2 AV3 AV4 AV5 AV6 AV7 AV8 AV9 AV10 AV11 AV12 AV13 AV14 AV15 AV16 AV17 AV29 AV33 AV34 AW1 AW2 AW4 AW23 AW33 AW34 AY1 AY2 AY3 AY4 AY20 AY22 AY24 AY30 AY31 AY32 AY33 AY34 B1 B2 B7 B9 B10 B12 B13 B15 B17 B18 B20 B22 B23 B28 B29 B30 B32 B33 B34 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C23 C27 C29 C32 C33 D1 D3 D5 D7 D9 D11 D13 D15 D16 D23 — VSS

D27 D32 E1 E2 E3 E4 E6 E8 E10 E12 E14 E16 E17 E18 E19 E20 E21 E22 E23 E25 E26 E27 E28 E30 E31 E32 E34 F1 F2 F3 F5 F19 F20 F21 F22 F23 F25 F26 F29 F30 F31 F32 G1 G3 G4 G7 G8 G9 G10 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G25 G28 G29 G30 H1 H2 H3 H5 H7 H8 H10 H12 H14 H16 H18 H20 H22 H24 H25 H29 H30 J1 J2 J3 J4 J7 J9 J11 J13 J15 J17 J19 — VSS

=PP1V1_PLL_H4 — R0620 0.00 — C0651 0.01UF — PP1V1_PLL4_F
R0621 0.00 — C0648 0.01UF — PP1V1_PLL3_F
R0622 0.00 — C0646 0.01UF — PP1V1_PLL2_F
R0623 0.00 — C0644 0.01UF — PP1V1_PLL1_F
R0624 0.00 — C0608 0.01UF + C0660 56PF — PP1V1_PLL0_F

VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V1_USB_H4 — C0643 0.22UF
=PP1V2_HSIC_H4 — C0642 0.01UF + C0641 0.01UF

JTAGSEL
0 - PARALLEL
1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)
PER RADAR #6755237

HSIC_VDD121 HSIC_VDD122 HSIC_DVDD PLL0_AVDD11 PLL1_AVDD11 PLL2_AVDD11 PLL3_AVDD11 PLL4_AVDD11 PLL_USB_AVDD11 MIPI0D_VDD11_PLL MIPI1D_VDD11_PLL USB_DVDD USB_VDD330

TP_HSIC1_AP_DATA — HSIC1_DATA
TP_HSIC1_AP_STB — HSIC1_STB
NC_HSIC2_AP_DATA — HSIC2_DATA
NC_HSIC2_AP_STB — HSIC2_STB

SYM 1 OF 12
U0652
H4P-512MB
BGA

JTAG_SEL
NC_JTAG_AP_RTCK
JTAG_TRST* — JTAG_AP_TRST_L
JTAG_TDO — JTAG_AP_TDO
JTAG_TDI — JTAG_AP_TDI
JTAG_TMS — JTAG_AP_TMS
JTAG_TCK — JTAG_AP_TCK
TESTMODE — AP_TESTMODE
FUSE1_FSRC
TST_STPCLK — AP_TST_STPCLK
TST_CLKOUT — TP_AP_TST_CLKOUT
FAST_SCAN_CLK (FOR IC TESTER) — AP_FAST_SCAN_CLK
HOLD_RESET (0=NORMAL) — AP_HOLD_RESET
RESET* — RST_AP_1V8_L
CFSB — AP_CFSB
DDR0_CKEIN
DDR1_CKEIN

R0645 100K — JTAG_AP_TCK
R0646 100K — JTAG_AP_TMS
R0647 100K — JTAG_AP_TDI
DEVELOPMENT_JTAG_TAP
R0662 100K — AP_JTAG_SEL

=PP3V3_USB_H4 — R0617 10K — R0632 100K — RST_AP_L
NOSTUFF XW0604 SHORT-01005
R0688 42.2K + C0618 1000PF
NOSTUFF XW0605 SHORT-01005 — AP_DDR1_CKEIN_1V2 — AP_DDR1_CKEIN
R0689 82.5K

HSIC_VSS121 HSIC_VSS122 HSIC_DVSS PLL0_AVSS11 PLL1_AVSS11 PLL2_AVSS11 PLL3_AVSS11 PLL4_AVSS11 PLL_USB_AVSS11 MIPI_VSS_0 MIPI_VSS_1 USB_DVSS USB_VSSA0 USB_VSSAC

PP1V1_PLL_USB_F — R0625 0.00 — =PP1V1_USB_H4
C0652 0.01UF
FL0610 80-OHM-0.2A-0.4-OHM
PP1V1_MIPID_PLL_F — =PP1V1_MIPI_PLL_H4
C0661 56PF + C0654 0.1UF + C0655 1UF
=PP1V1_USB_H4 — C0627 0.01UF
=PP3V3_USB_H4 — C0640 1UF + C0630 0.01UF

WDOG — RST_PMU_IN
XI0 — XTAL_24M_I
XO0 — XTAL_24M_O
R0655 1.00M
R0640 22
CRITICAL Y0602 24.000MHZ-16PF-60PPM
C0613 22PF + C0607 22PF
USB11_DP — USB_FS_D_P
USB11_DM — USB_FS_D_N
USB_DP — USB_D_P
USB_DM — USB_D_N
USB_ANALOGTEST — NC_USB_ANALOGTEST
USB_VBUS — USB_AP_VBUS — R0651 100K — PPVBUS_USB
USB_ID — NC_USB_ID
USB_BRICKID — DZ0600 GDZT2R5.1B — USB_BRICKID
USB_REXT — R0642 44.2
NOTE: PAGE 4608 H4P UM V0.83

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PAGE TITLE: AP: MAIN		
Apple Inc.	DRAWING NUMBER: 051-8962	SIZE: D
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	BRANCH:	
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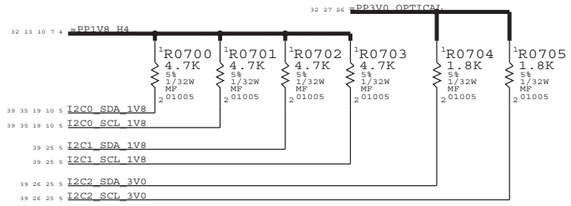

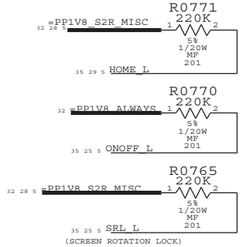

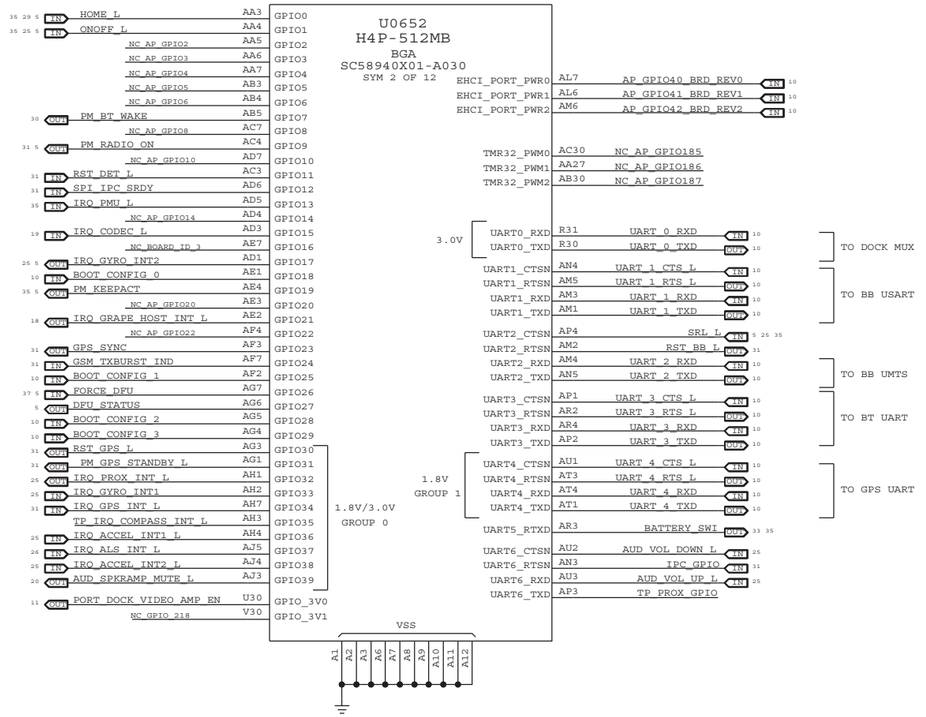

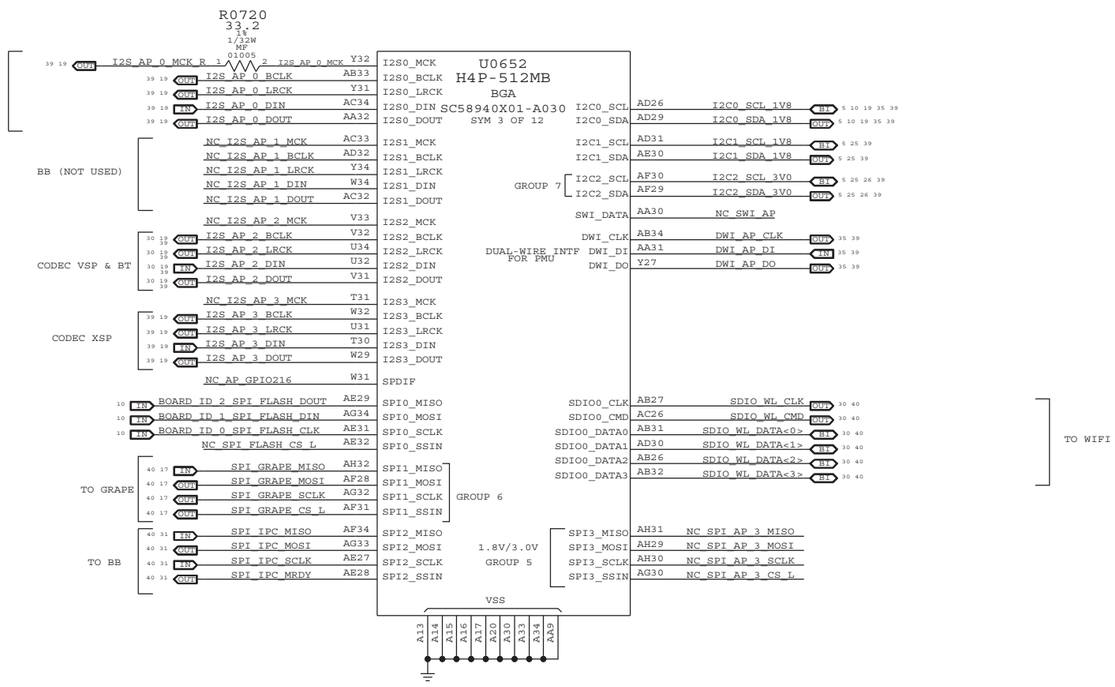

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	REVISION: A.0.0
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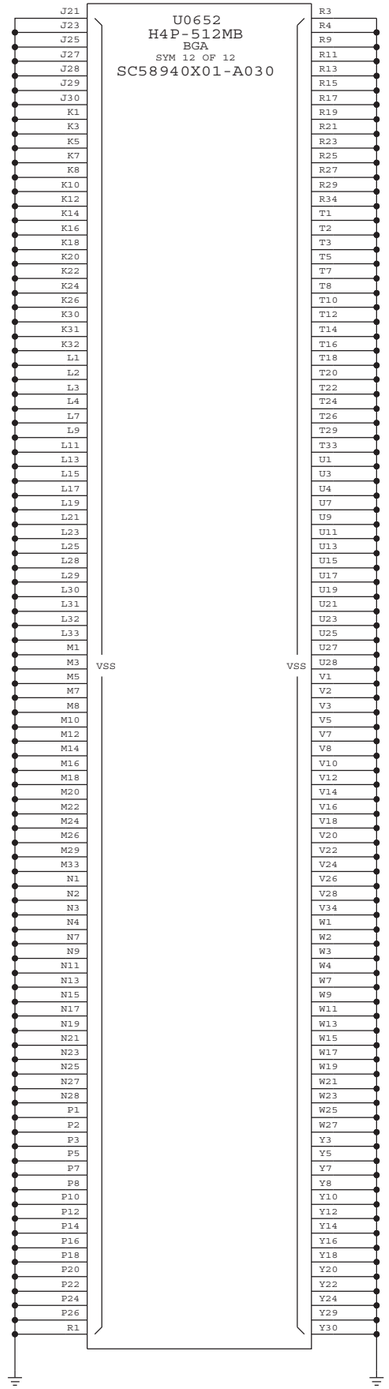

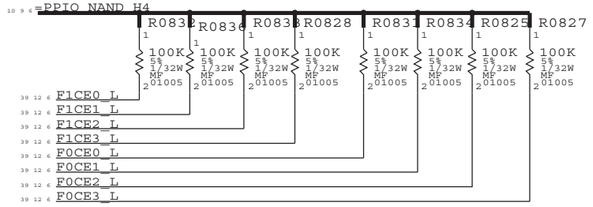

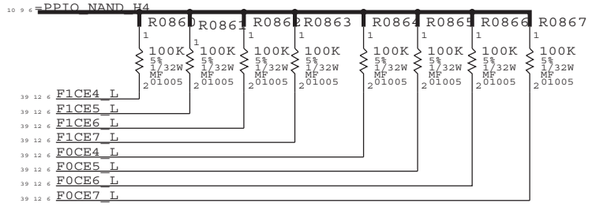

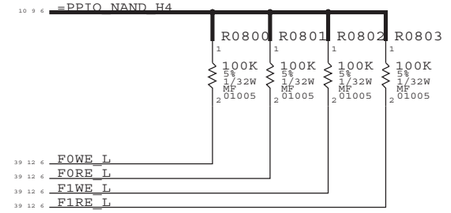

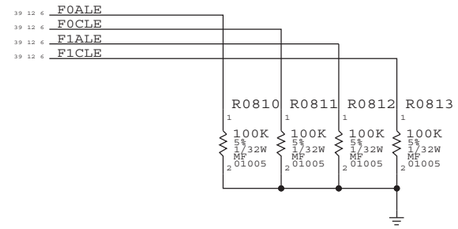

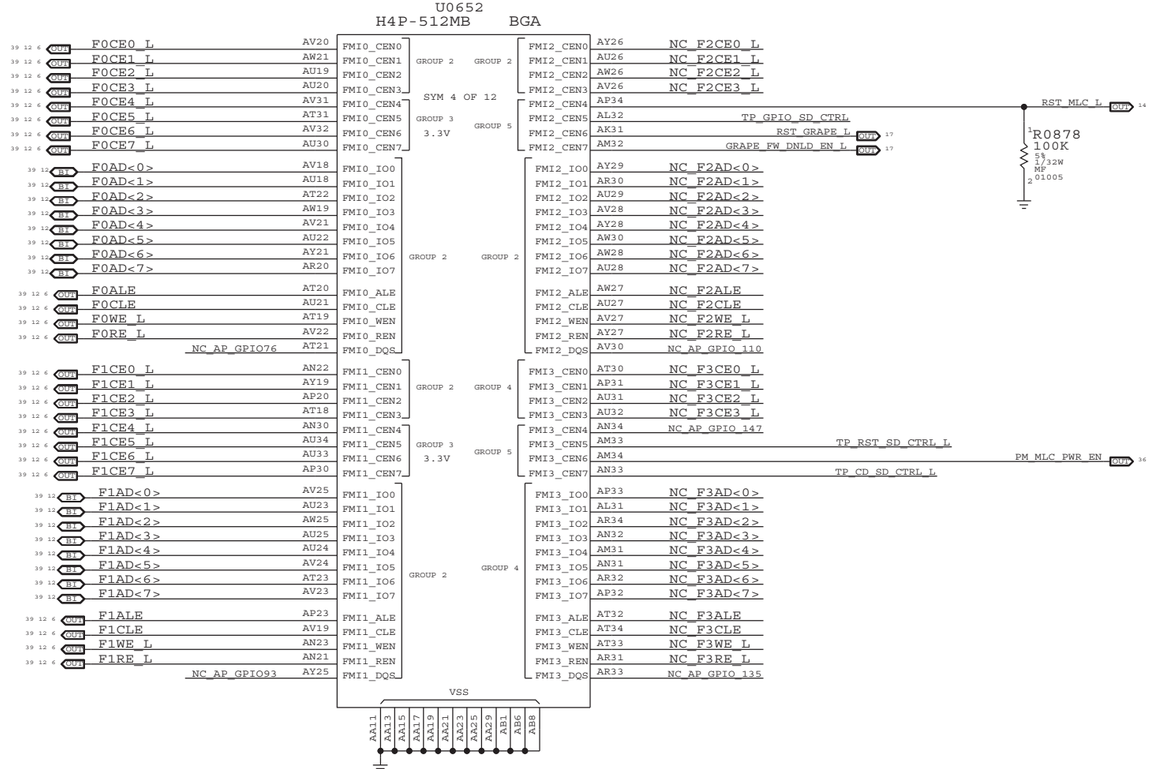

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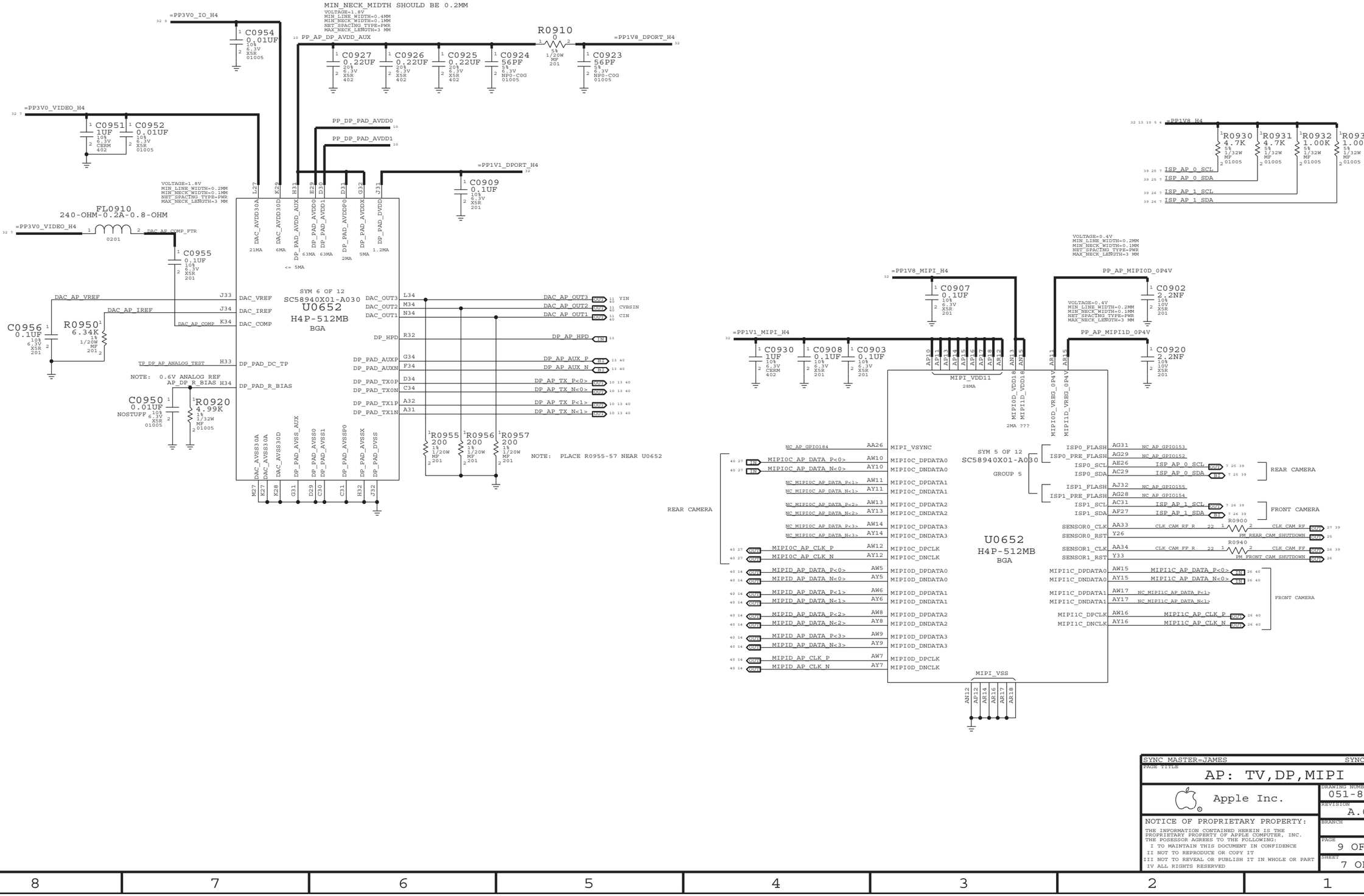
Apple Inc.	DRAWING NUMBER 051-8962 · SIZE D · REVISION A.0.0 · BRANCH · PAGE 8 OF 106 · SHEET 6 OF 42


MIN_NECK_MIDTH SHOULD BE 0.2MM
=PP3V0_IO_H4
C0954 0.01UF
PP_AP_DP_AVDD_AUX
R0910 0
=PP1V8_DPORT_H4
C0927 0.22UF
C0926 0.22UF
C0925 0.22UF
C0924 56PF
C0923 56PF
=PP3V0_VIDEO_H4
C0951 1UF
C0952 0.01UF
PP_DP_PAD_AVDD0
PP_DP_PAD_AVDD1
=PP1V1_DPORT_H4
C0909 0.1UF
FL0910
240-OHM-0.2A-0.8-OHM
DAC_AP_COMP_FTR
C0955 0.1UF
DAC_AP_VREF
DAC_AP_IREF
C0956 0.1UF
R0950 6.34K
TP_DP_AP_ANALOG_TEST
NOTE: 0.6V ANALOG REF
AP_DP_R_BIAS
C0950 0.01UF NOSTUFF
R0920 4.99K
SYM 6 OF 12
SC58940X01-A030
U0652
H4P-512MB
BGA
DAC_OUT3
DAC_OUT2
DAC_OUT1
DP_HPD
DP_PAD_AUXP
DP_PAD_AUXN
DP_PAD_TX0P
DP_PAD_TX0N
DP_PAD_TX1P
DP_PAD_TX1N
DP_PAD_R_BIAS
DP_PAD_DC_TP
DAC_AP_OUT3
DAC_AP_OUT2
DAC_AP_OUT1
DP_AP_HPD
DP_AP_AUX_P
DP_AP_AUX_N
DP_AP_TX_P<0>
DP_AP_TX_N<0>
DP_AP_TX_P<1>
DP_AP_TX_N<1>
YIN
CVBSIN
CIN
R0955 200
R0956 200
R0957 200
NOTE: PLACE R0955-57 NEAR U0652
REAR CAMERA
=PP1V8_H4
R0930 4.7K
R0931 4.7K
R0932 1.00K
R0933 1.00K
ISP_AP_0_SCL
ISP_AP_0_SDA
ISP_AP_1_SCL
ISP_AP_1_SDA
=PP1V8_MIPI_H4
C0907 0.1UF
PP_AP_MIPI0D_0P4V
C0902 2.2NF
=PP1V1_MIPI_H4
C0930 1UF
C0908 0.1UF
C0903 0.1UF
MIPI_VDD11
28MA
PP_AP_MIPI1D_0P4V
C0920 2.2NF
2MA ???
MIPI_VSYNC
MIPI0C_DPDATA0
MIPI0C_DNDATA0
MIPI0C_DPDATA1
MIPI0C_DNDATA1
MIPI0C_DPDATA2
MIPI0C_DNDATA2
MIPI0C_DPDATA3
MIPI0C_DNDATA3
MIPI0C_DPCLK
MIPI0C_DNCLK
MIPI0D_DPDATA0
MIPI0D_DNDATA0
MIPI0D_DPDATA1
MIPI0D_DNDATA1
MIPI0D_DPDATA2
MIPI0D_DNDATA2
MIPI0D_DPDATA3
MIPI0D_DNDATA3
MIPI0D_DPCLK
MIPI0D_DNCLK
SYM 5 OF 12
SC58940X01-A030
GROUP 5
U0652
H4P-512MB
BGA
ISP0_FLASH
ISP0_PRE_FLASH
ISP0_SCL
ISP0_SDA
ISP1_FLASH
ISP1_PRE_FLASH
ISP1_SCL
ISP1_SDA
SENSOR0_CLK
SENSOR0_RST
SENSOR1_CLK
SENSOR1_RST
CLK_CAM_RF_R
CLK_CAM_FF_R
PM_REAR_CAM_SHUTDOWN
PM_FRONT_CAM_SHUTDOWN
REAR CAMERA
FRONT CAMERA
MIPI1C_DPDATA0
MIPI1C_DNDATA0
MIPI1C_DPDATA1
MIPI1C_DNDATA1
MIPI1C_DPCLK
MIPI1C_DNCLK
MIPI_VSS
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SYNC_DATE=N/A
PAGE TITLE
AP: TV,DP,MIPI
Apple Inc.
DRAWING NUMBER 051-8962
SIZE D
REVISION A.0.0
BRANCH
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SHEET 7 OF 42
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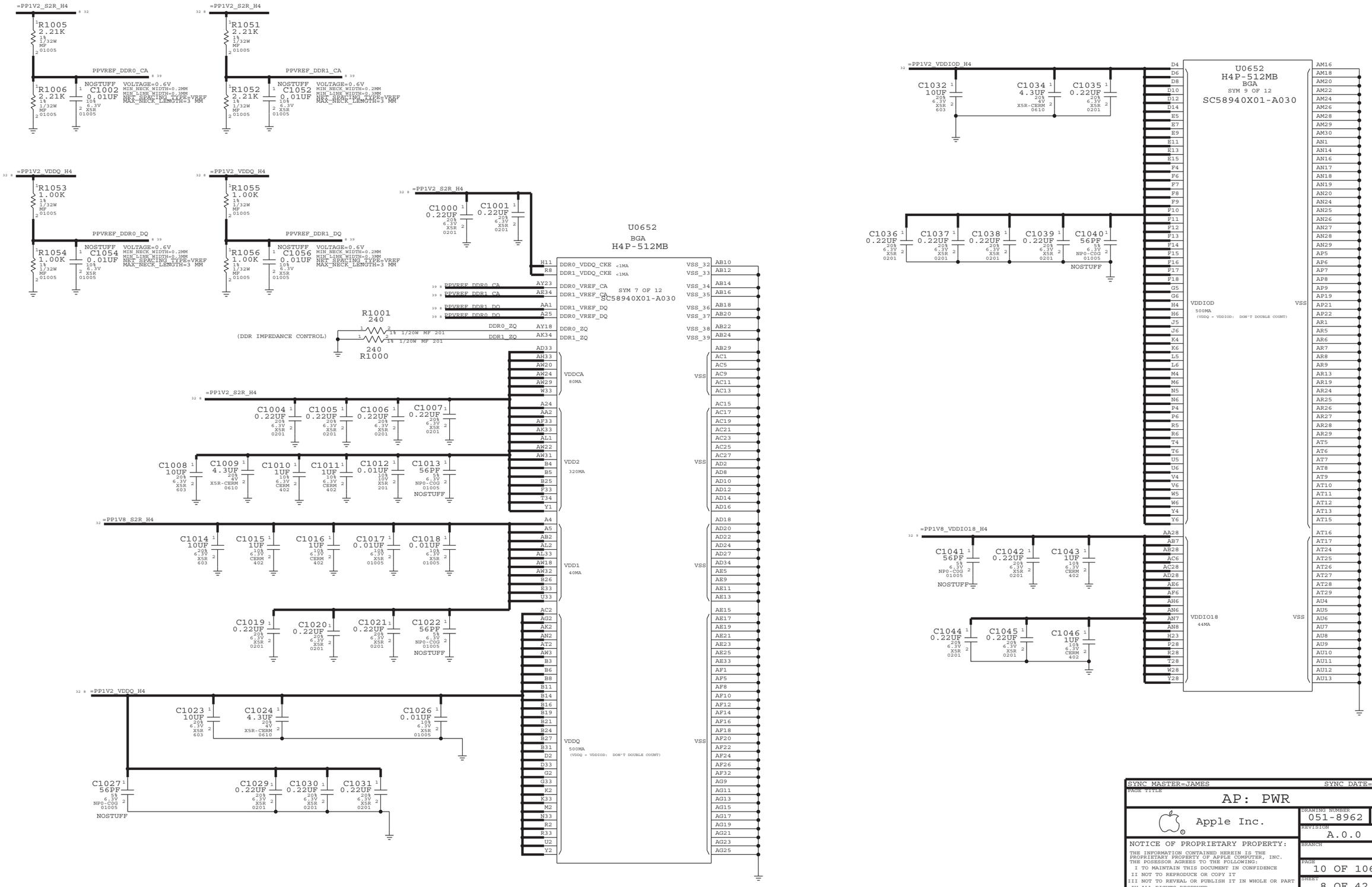
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R1005 2.21K 1% 1/32W MF 01005
PPVREF_DDR0_CA
R1006 2.21K 1% 1/32W MF 01005
NOSTUFF C1002 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.1MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM
=PP1V2_S2R_H4
R1051 2.21K 1% 1/32W MF 01005
PPVREF_DDR1_CA
R1052 2.21K 1% 1/32W MF 01005
NOSTUFF C1052 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.1MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_H4
R1053 1.00K 1% 1/32W MF 01005
PPVREF_DDR0_DQ
R1054 1.00K 1% 1/32W MF 01005
NOSTUFF C1054 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
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MIN_LINE_WIDTH=0.1MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM
=PP1V2_VDDQ_H4
R1055 1.00K 1% 1/32W MF 01005
PPVREF_DDR1_DQ
R1056 1.00K 1% 1/32W MF 01005
NOSTUFF C1056 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.1MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM
=PP1V2_S2R_H4
C1000 0.22UF 20% 6.3V X5R 0201
C1001 0.22UF 20% 6.3V X5R 0201
U0652
BGA
H4P-512MB
SYM 7 OF 12
SC58940X01-A030
DDR0_VDDQ_CKE <1MA
DDR1_VDDQ_CKE <1MA
DDR0_VREF_CA
DDR1_VREF_CA
DDR1_VREF_DQ
DDR0_VREF_DQ
DDR0_ZQ
DDR1_ZQ
PPVREF_DDR0_CA
PPVREF_DDR1_CA
PPVREF_DDR1_DQ
PPVREF_DDR0_DQ
R1001 240 1% 1/20W MF 201
(DDR IMPEDANCE CONTROL)
240 R1000
VDDCA 80MA
VDD2 320MA
VDD1 40MA
VDDQ 500MA
(VDDQ - VDDIOD: DON'T DOUBLE COUNT)
VSS
=PP1V2_S2R_H4
C1004 0.22UF 20% 6.3V X5R 0201
C1005 0.22UF 20% 6.3V X5R 0201
C1006 0.22UF 20% 6.3V X5R 0201
C1007 0.22UF 20% 6.3V X5R 0201
C1008 10UF 20% 6.3V X5R 603
C1009 4.3UF 20% 4V X5R-CERM 0610
C1010 1UF 10% 6.3V CERM 402
C1011 1UF 10% 6.3V CERM 402
C1012 0.01UF 10% 10V X5R 201
C1013 56PF 5% 6.3V NP0-C0G 01005
NOSTUFF
=PP1V8_S2R_H4
C1014 10UF 20% 6.3V X5R 603
C1015 1UF 10% 6.3V CERM 402
C1016 1UF 10% 6.3V CERM 402
C1017 0.01UF 10% 6.3V X5R 01005
C1018 0.01UF 10% 6.3V X5R 01005
C1019 0.22UF 20% 6.3V X5R 0201
C1020 0.22UF 20% 6.3V X5R 0201
C1021 0.22UF 20% 6.3V X5R 0201
C1022 56PF 5% 6.3V NP0-C0G 01005
NOSTUFF
=PP1V2_VDDQ_H4
C1023 10UF 20% 6.3V X5R 603
C1024 4.3UF 20% 4V X5R-CERM 0610
C1026 0.01UF 10% 6.3V X5R 01005
C1027 56PF 5% 6.3V NP0-C0G 01005
NOSTUFF
C1029 0.22UF 20% 6.3V X5R 0201
C1030 0.22UF 20% 6.3V X5R 0201
C1031 0.22UF 20% 6.3V X5R 0201
=PP1V2_VDDIOD_H4
C1032 10UF 20% 6.3V X5R 603
C1034 4.3UF 20% 4V X5R-CERM 0610
C1035 0.22UF 20% 6.3V X5R 0201
C1036 0.22UF 20% 6.3V X5R 0201
C1037 0.22UF 20% 6.3V X5R 0201
C1038 0.22UF 20% 6.3V X5R 0201
C1039 0.22UF 20% 6.3V X5R 0201
C1040 56PF 5% 6.3V NP0-C0G 01005
NOSTUFF
U0652
H4P-512MB
BGA
SYM 9 OF 12
SC58940X01-A030
VDDIOD 500MA
(VDDQ + VDDIOD: DON'T DOUBLE COUNT)
VSS
=PP1V8_VDDIO18_H4
C1041 56PF 5% 6.3V NP0-C0G 01005
NOSTUFF
C1042 0.22UF 20% 6.3V X5R 0201
C1043 1UF 10% 6.3V CERM 402
C1044 0.22UF 20% 6.3V X5R 0201
C1045 0.22UF 20% 6.3V X5R 0201
C1046 1UF 10% 6.3V CERM 402
VDDIO18 44MA
VSS
SYNC MASTER=JAMES
SYNC DATE=N/A
PAGE TITLE
AP: PWR
Apple Inc.
DRAWING NUMBER 051-8962
SIZE D
REVISION A.0.0
BRANCH
PAGE 10 OF 106
SHEET 8 OF 42
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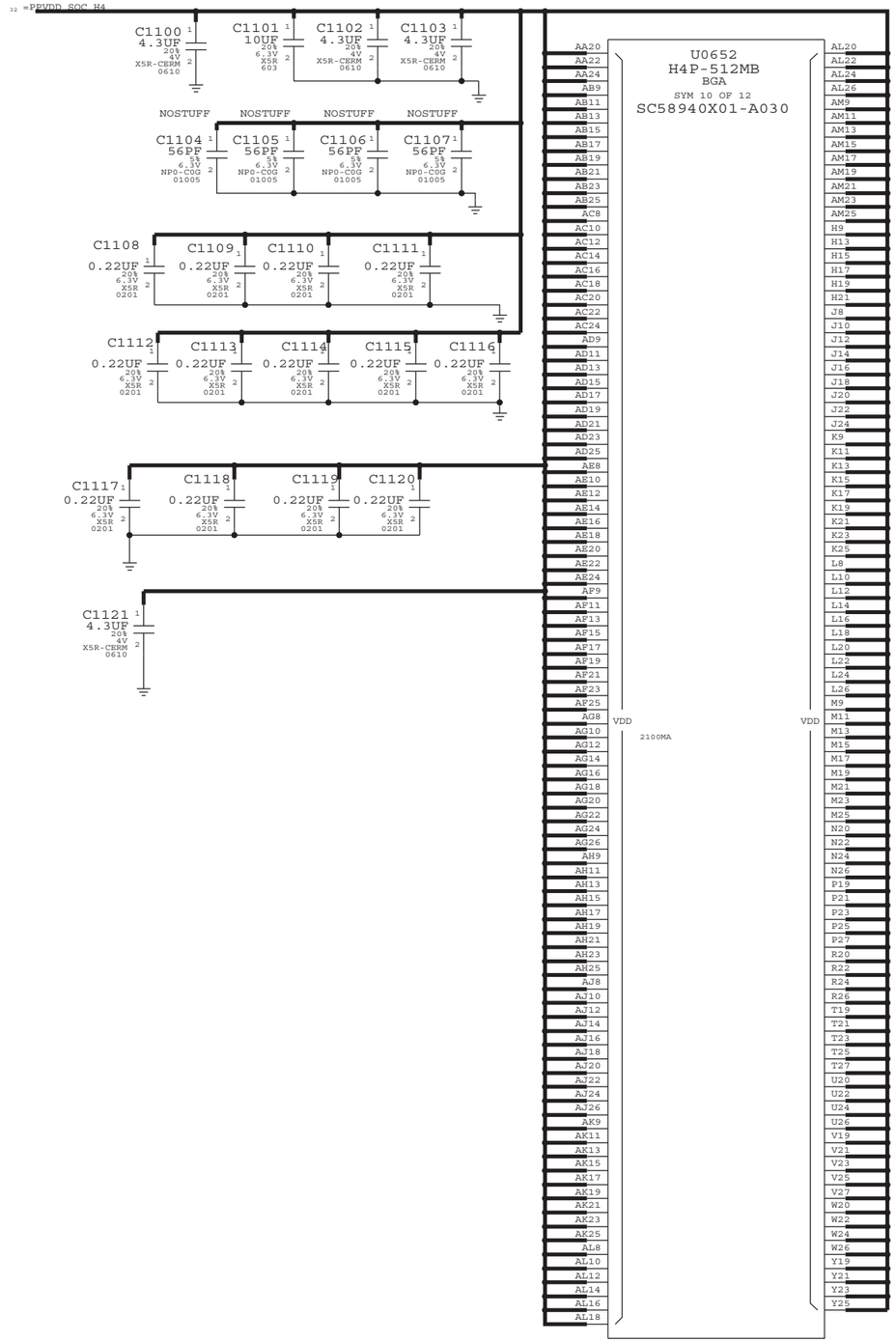

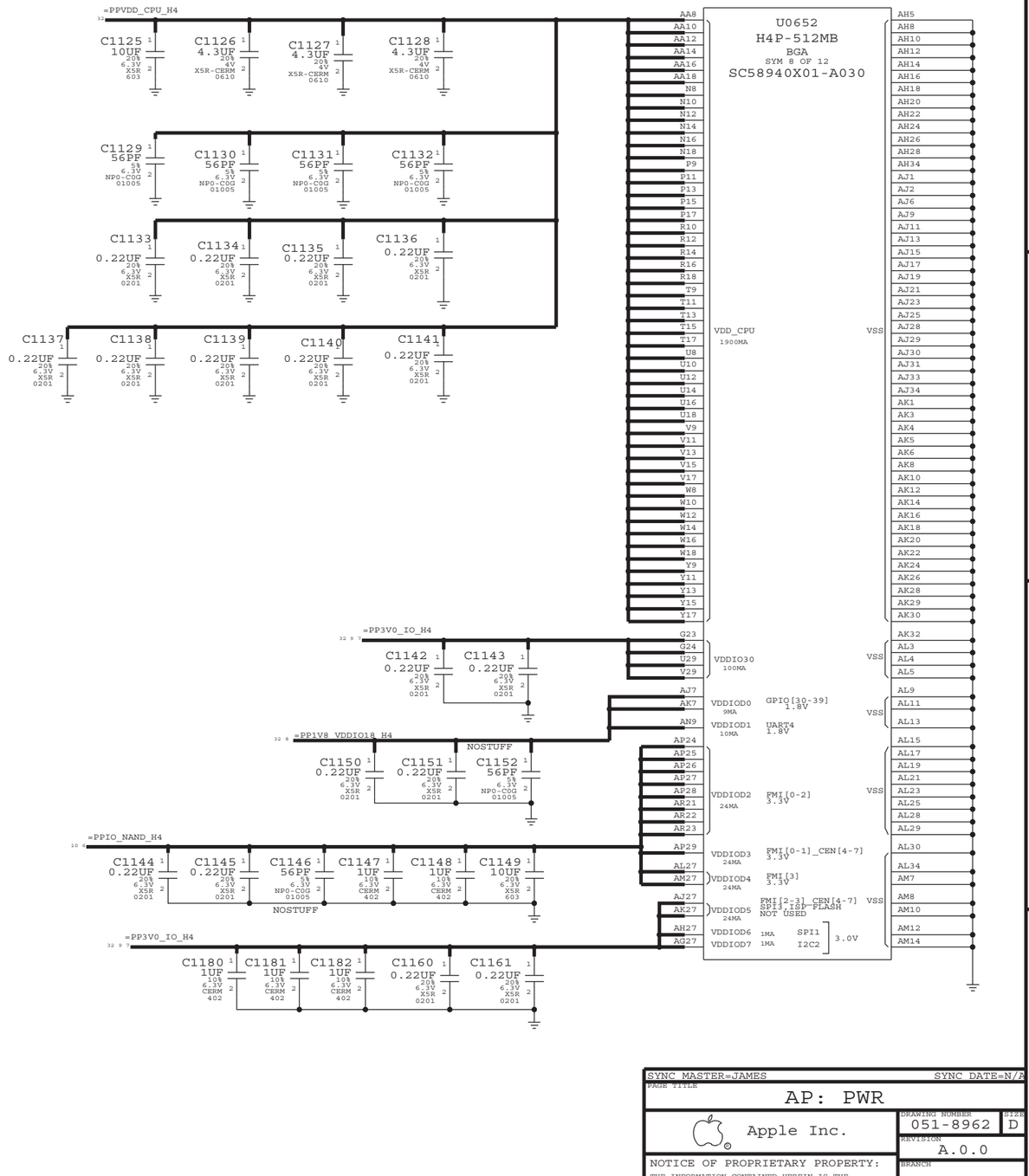

SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE

AP: PWR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

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BOOT CONFIG ID

=PP1V8_H4

R1200	R1201	R1202 (FMI_TEST)	R1203 (FMI_NOTEST)
10K 5% 1/20W MF 201	10K 5% 1/20W MF 201	10K 5% 1/20W MF 201	10K 5% 1/32W MF 01005

BOOT_CONFIG[3] (GPIO29)	BOOT_CONFIG_3
BOOT_CONFIG[2] (GPIO28)	BOOT_CONFIG_2
BOOT_CONFIG[1] (GPIO25)	BOOT_CONFIG_1
BOOT_CONFIG[0] (GPIO18)	BOOT_CONFIG_0

BOOT_CONFIG[3-0]	
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

JTAG

JTAG_DAP	R1210 100 1 2 AP_JTAG_SEL (OUT)
JTAG_DAP	R1211 100 1 2 JTAG_AP_TRST_L (OUT)

DEVELOPMENT_JTAG_TAP	R1212 0.00 5% 1/32W MF 01005	JTAG_AP_TDO (IN)	VIDEO_EMI_C_Y (OUT)
DEVELOPMENT_JTAG_TAP	R1213 0.00 5% 1/32W MF 01005	JTAG_AP_TDI (OUT)	VIDEO_EMI_Y_PR (IN)
DEVELOPMENT_JTAG_TAP	R1214 0.00 5% 1/32W MF 01005	JTAG_AP_TRST_L (OUT)	VIDEO_EMI_CVBS_PB (IN)

2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	

BOARD ID

=PP1V8_H4

	K93-K94	K94-K95	K9X_DEV
	R1204 10K 5% 1/32W MF 01005	R1205 10K 5% 1/32W MF 01005	R1206 10K 5% 1/32W MF 01005

BOARD_ID[3]	BOARD_ID_3
BOARD_ID[2]	BOARD_ID_2_SPI_FLASH_DOUT
BOARD_ID[1]	BOARD_ID_1_SPI_FLASH_DIN
BOARD_ID[0]	BOARD_ID_0_SPI_FLASH_CLK

BOARD_ID[3-0]	
0100	K93 AP
0101	K93 DEV
0110	K94 AP
0111	K94 DEV
0010	K95 AP
0011	K95 DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

AP_GPIO42_BRD_REV2	R1207 10K 5% 1/20W MF 201	R1208 10K 5% 1/20W MF 201	R1209 (NOSTUFF) 10K 5% 1/20W MF 201
AP_GPIO41_BRD_REV1			
AP_GPIO40_BRD_REV0			

BRD_REV[2-0]	
000	PROTO 1
001	PROTO 2
010	EVT
011	EVT2
100	DVT

S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

PLACEMENT NOTE: NEAR U0652

DP_AP_TX_P<0> (OUT)	DP_AP_TX_N<0> (OUT)	DP_AP_TX_P<1> (OUT)	DP_AP_TX_N<1> (OUT)
SIGNAL_MODEL=EMPTY NOSTUFF R1250 150 5% 1/20W MF 201	SIGNAL_MODEL=EMPTY NOSTUFF R1251 150 5% 1/20W MF 201	SIGNAL_MODEL=EMPTY NOSTUFF R1252 150 5% 1/20W MF 201	SIGNAL_MODEL=EMPTY NOSTUFF R1253 150 5% 1/20W MF 201
DP_TERM_C1250		DP_TERM_C1251	
SIGNAL_MODEL=EMPTY NOSTUFF C1250 100PF 5% 25V CERM 201		SIGNAL_MODEL=EMPTY NOSTUFF C1251 100PF 5% 25V CERM 201	

PP_AP_DP_AVDD_AUX (MAKE_BASE=TRUE)	PP_DP_PAD_AVDD0 / PP_DP_PAD_AVDD1
=PPIO_NAND_H4	=PP3V3_NAND_H4

R1260 100 5% 1/32W MF 01005 — AP_TESTMODE

NOSTUFF SHORT-01005 XW0601	AP_TST_STPCLK
NOSTUFF SHORT-01005 XW0602	AP_FAST_SCAN_CLK
NOSTUFF SHORT-01005 XW0603	AP_HOLD_RESET

UART_0_RXD	UART_0_TXD	UART_1_CTS_L	UART_1_RTS_L / UART_1_RXD / UART_1_TXD
UART_AP_0_RXD (IN)	UART_AP_0_TXD (OUT)	UART_AP_1_CTS_L (IN)	UART_AP_1_RTS_L (OUT) / UART_AP_1_RXD (IN) / UART_AP_1_TXD (OUT)
TO DOCK MUX		TO BB USART	

UART_2_RXD	UART_2_TXD	UART_3_CTS_L	UART_3_RTS_L / UART_3_RXD / UART_3_TXD
UART_AP_2_RXD (IN)	UART_AP_2_TXD (OUT)	UART_AP_3_CTS_L (IN)	UART_AP_3_RTS_L (OUT) / UART_AP_3_RXD (IN) / UART_AP_3_TXD (OUT)
TO BB UMTS		TO BT UART	

UART_4_CTS_L	UART_4_RTS_L / UART_4_RXD / UART_4_TXD	
UART_AP_4_CTS_L (IN)	UART_AP_4_RTS_L (OUT) / UART_AP_4_RXD (IN) / UART_AP_4_TXD (OUT)	
TO GPS UART		

CHS_SCL	I2C0_SCL_1V8
CHS_SDA	I2C0_SDA_1V8

FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1011	RESERVED
1100	FMI0/1 2/2 CS
CURRENT SETTING -> 1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

SYNC_MASTER=JAMES — SYNC_DATE=N/A

PAGE TITLE: AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER: 051-8962 — SIZE: D

REVISION: A.0.0

BRANCH:

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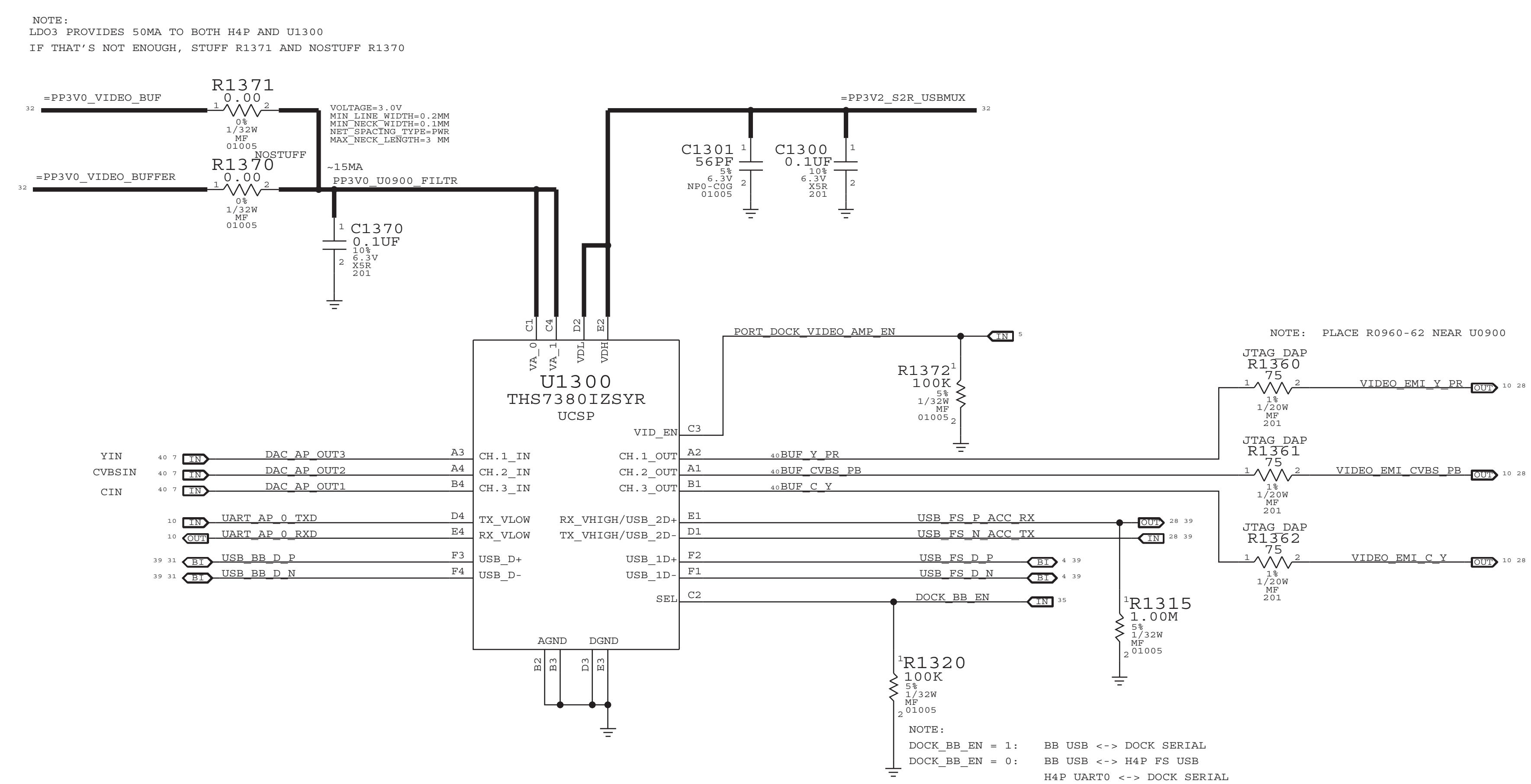
SHEET: 10 OF 42



SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE

AP: VIDEO BUFFER,BB USB MUXES

Apple Inc.

DRAWING NUMBER	SIZE
051-8962	D

REVISION A.0.0

BRANCH

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

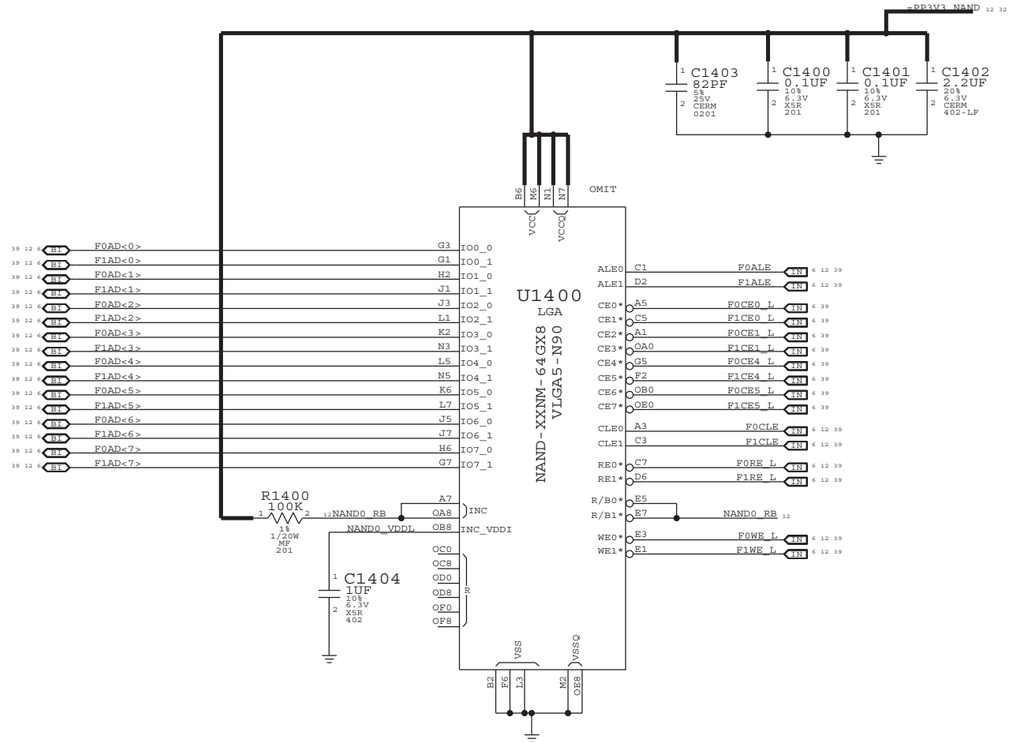
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

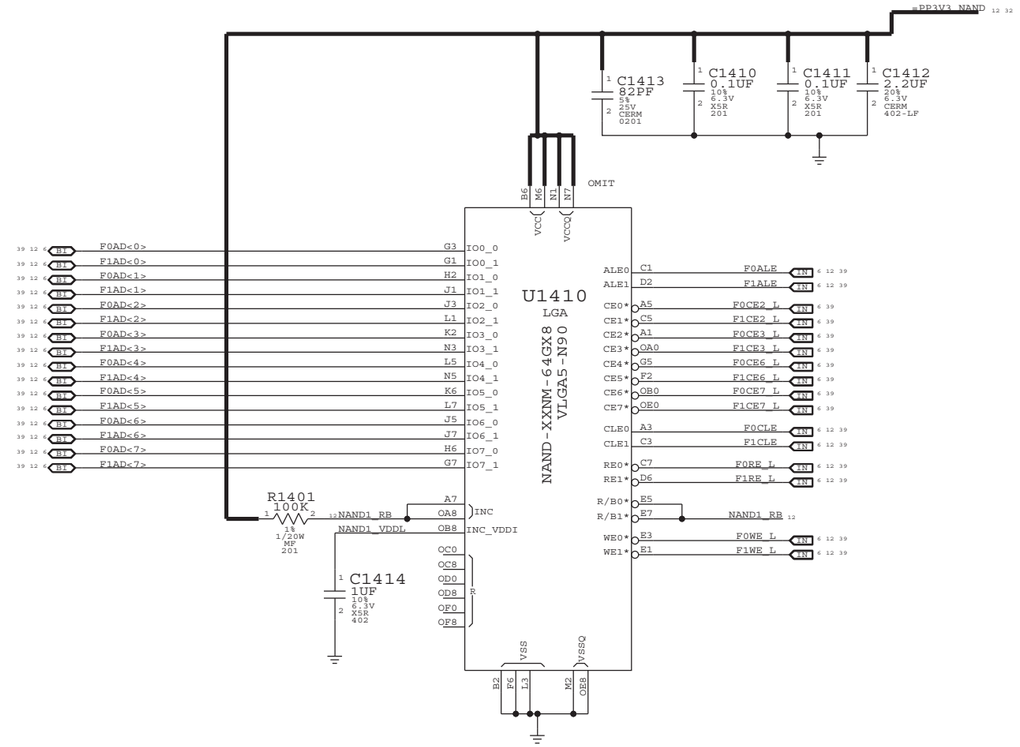
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN





SYNC MASTER=JONATHAN SYNC DATE=N/A

PAGE TITLE

NAND

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DRAWING NUMBER 051-8962 SIZE D

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BRANCH

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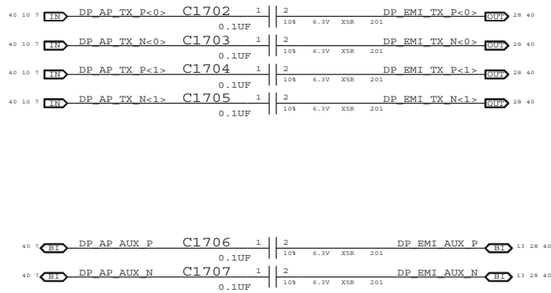
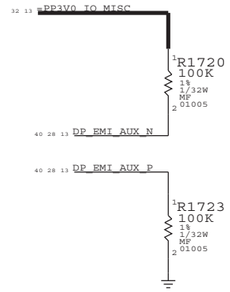
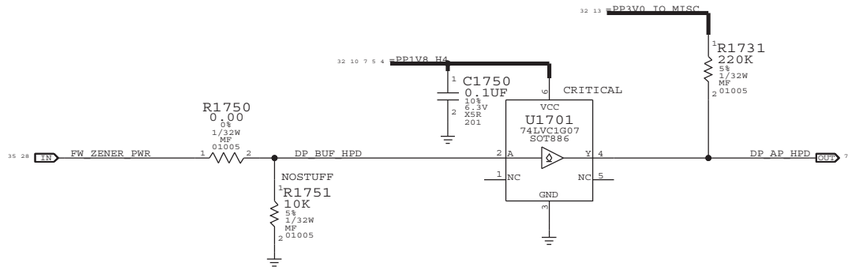
DISPLAYPORT AC COUPLING





DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
VIDEO: DISPLAY PORT

Apple Inc.

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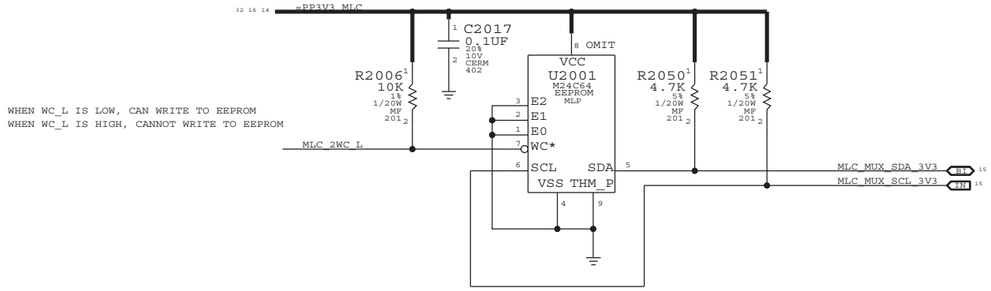
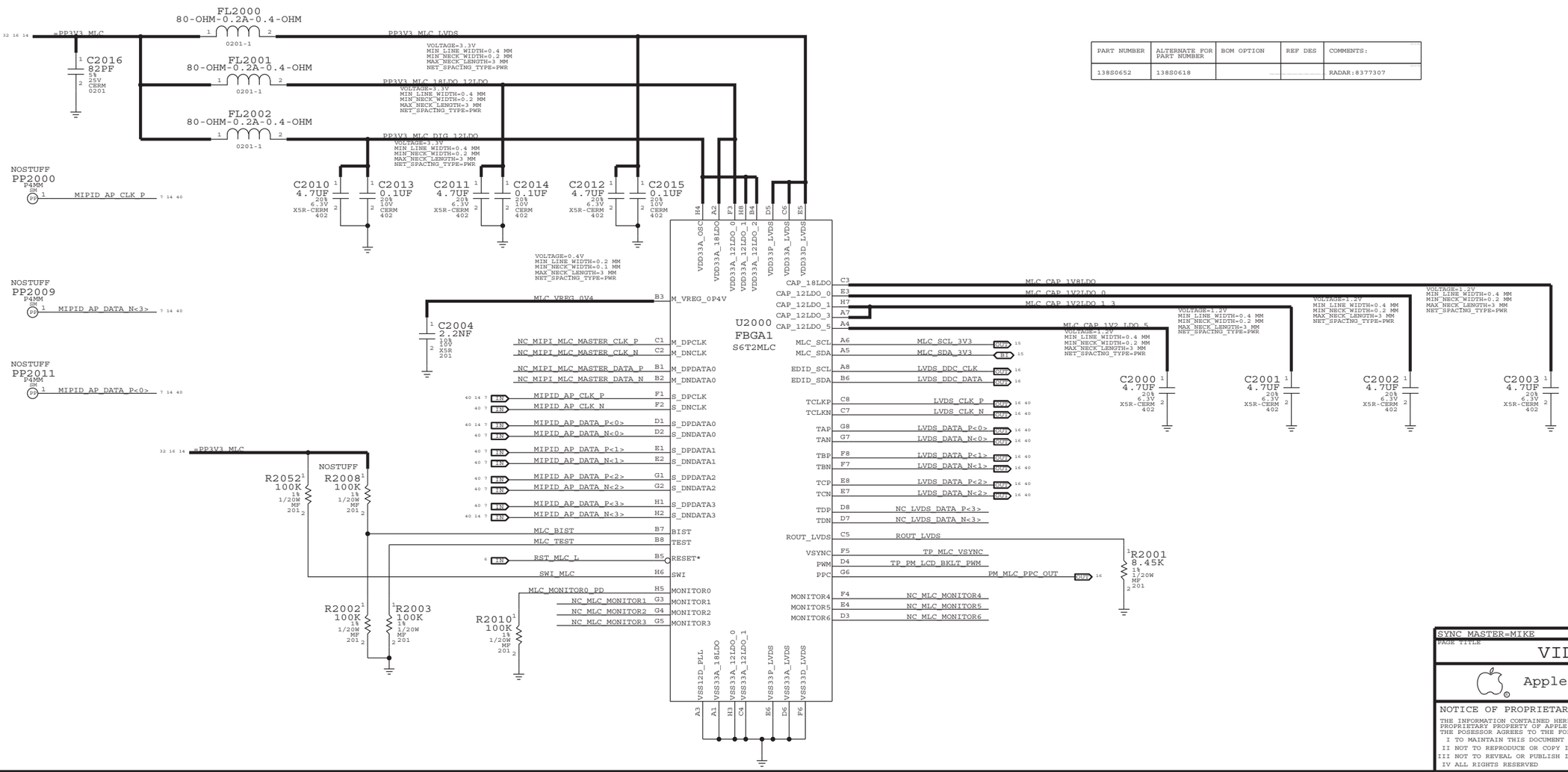
MLC EEPROM:RAW APN 335S0661

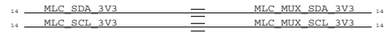
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307



SYNC MASTER=MIKE	SYNC DATE=N/A
PAGE TITLE	VIDEO: MLC
Apple Inc.	DRAWING NUMBER 051-8962 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 20 OF 106
	SHEET 14 OF 42



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

VIDEO: MLC ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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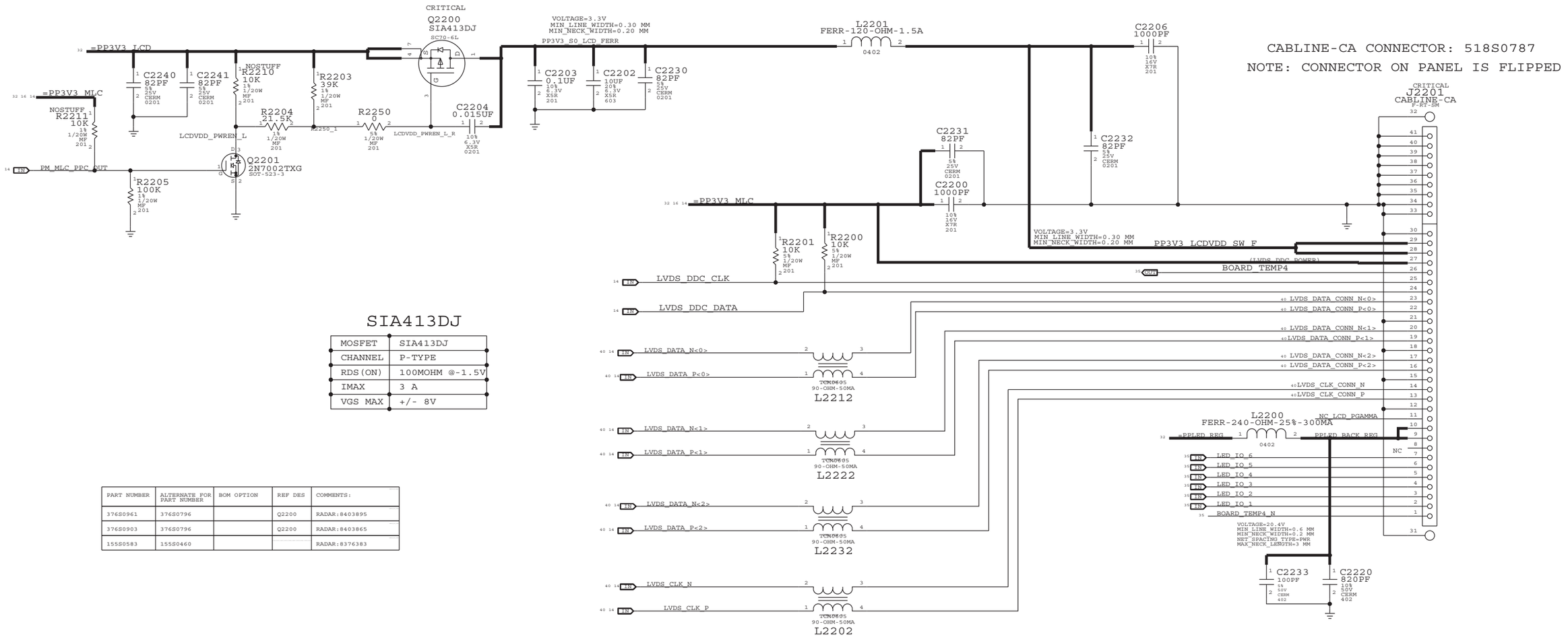
LVDS CONNECTOR



CABLINE-CA CONNECTOR: 518S0787

NOTE: CONNECTOR ON PANEL IS FLIPPED

SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO
INVESTIGATE POSSIBILITY OF REMOVING
THE CHOKE

SYNC_MASTER=ALEX SYNC_DATE=N/A

PAGE TITLE

VIDEO: LVDS CONNECTOR

Apple Inc.

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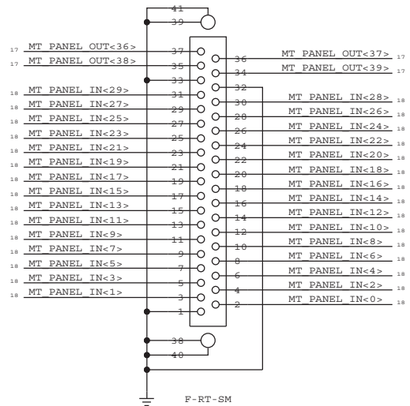
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

CONNECTORS TO GRAPE FLEX

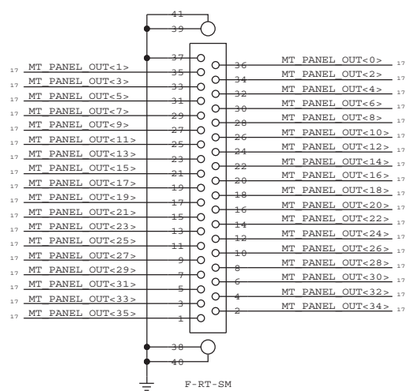
P/N 518S0817



502250-8237

J3010

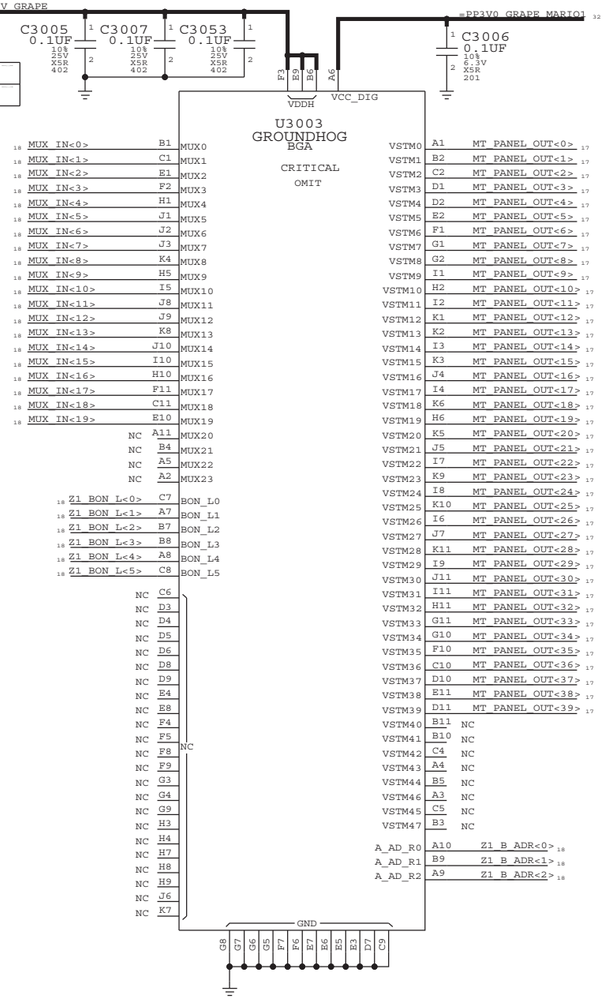
MATES WITH LEFTMOST GRAPE FLEX TAIL

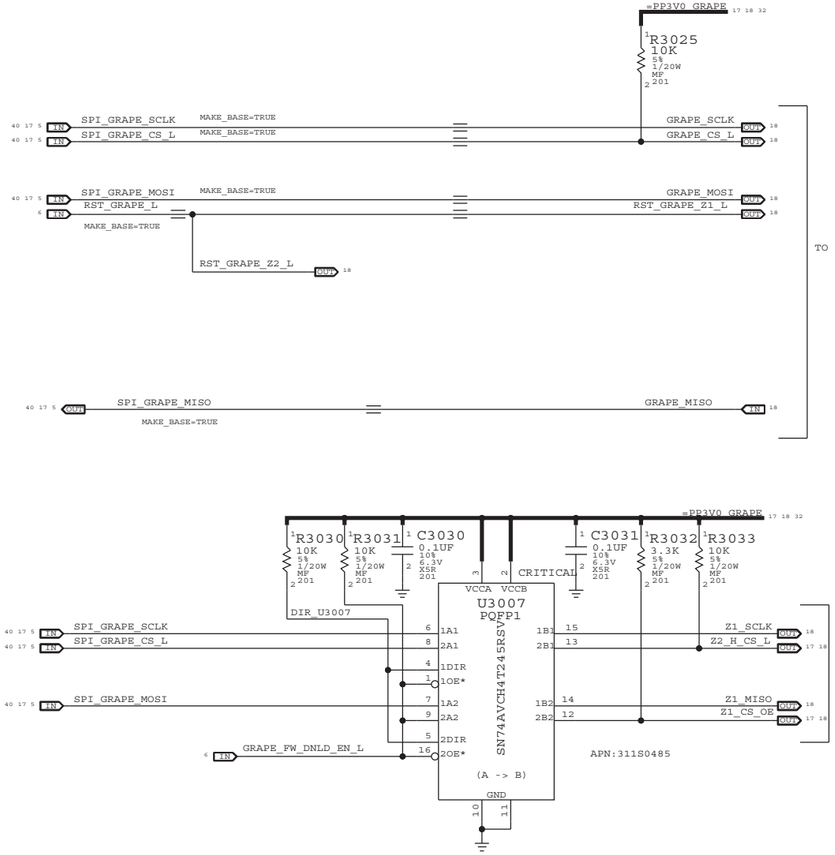


502250-8237

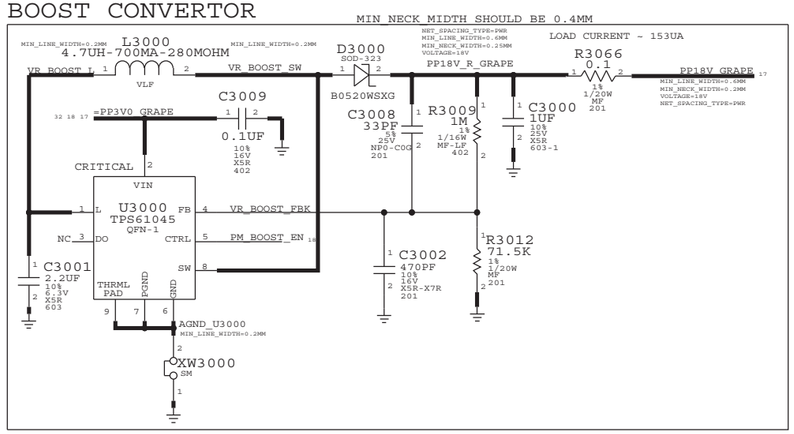
J3011

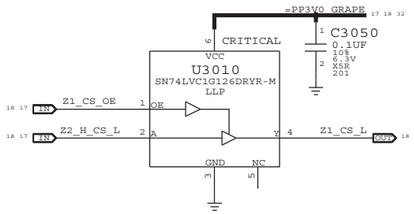
MATES WITH RIGHTMOST GRAPE FLEX TAIL

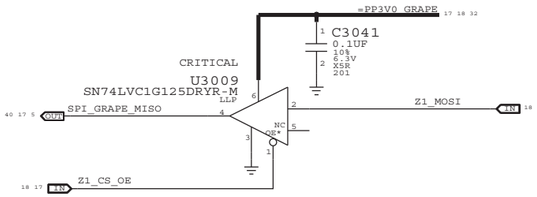




BOOST CONVERTOR







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=RAMSIN SYNC DATE=N/A

PAGE TITLE

GRAPE: GROUNDHOG,CONN,BOOST

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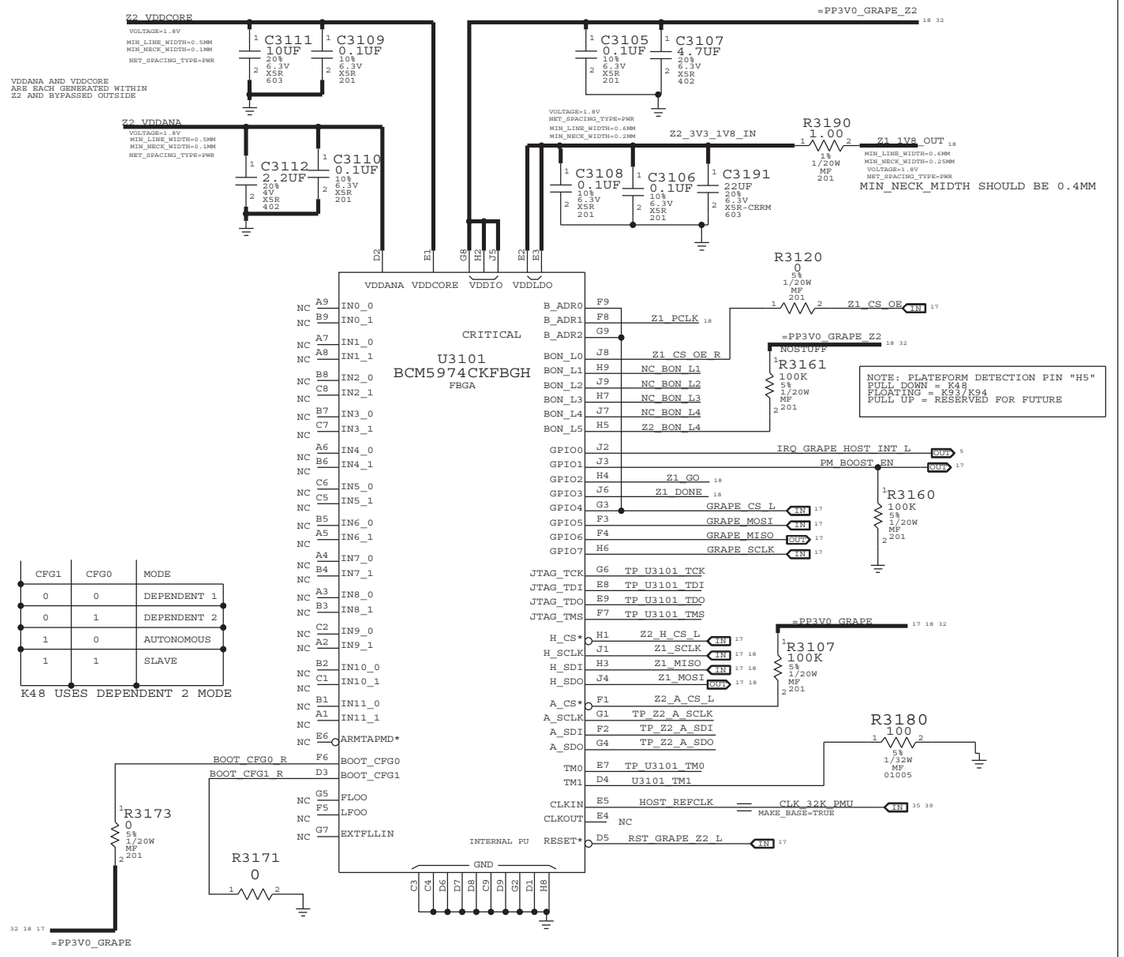
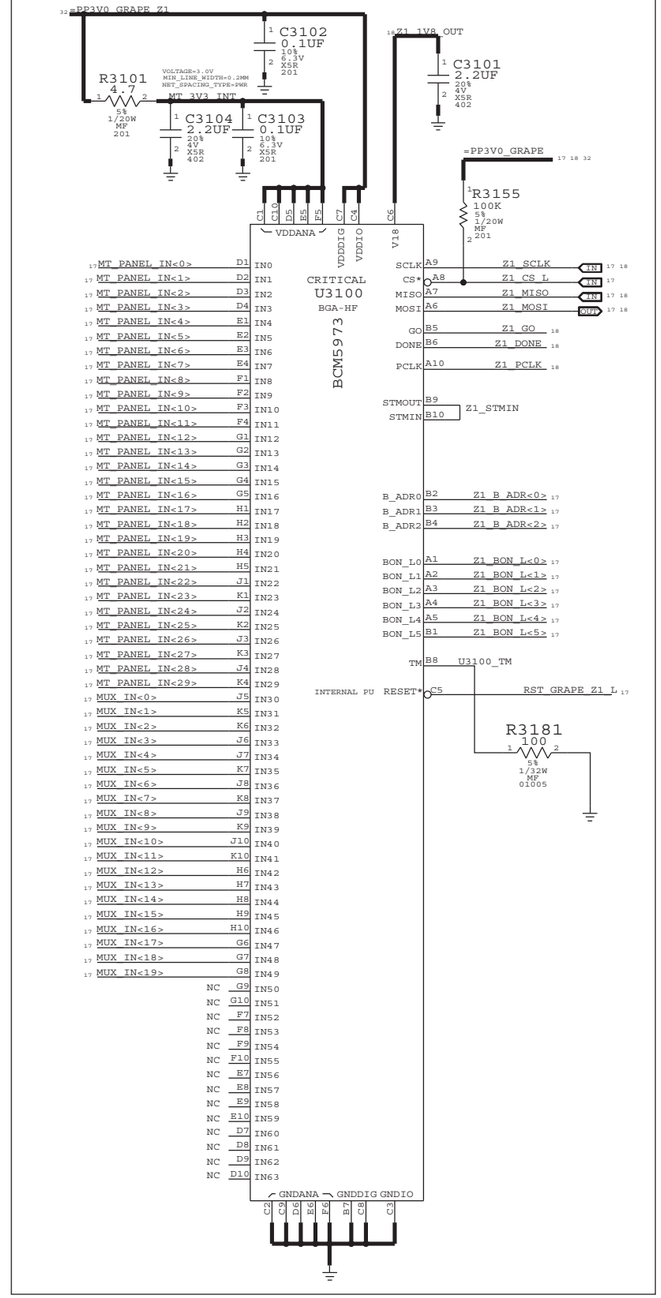
ARM9 MCU (Z2 BASED)



CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

ZEPHYR 1+ ASIC



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR:8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

SYNC MASTER=RAMSIN SYNC DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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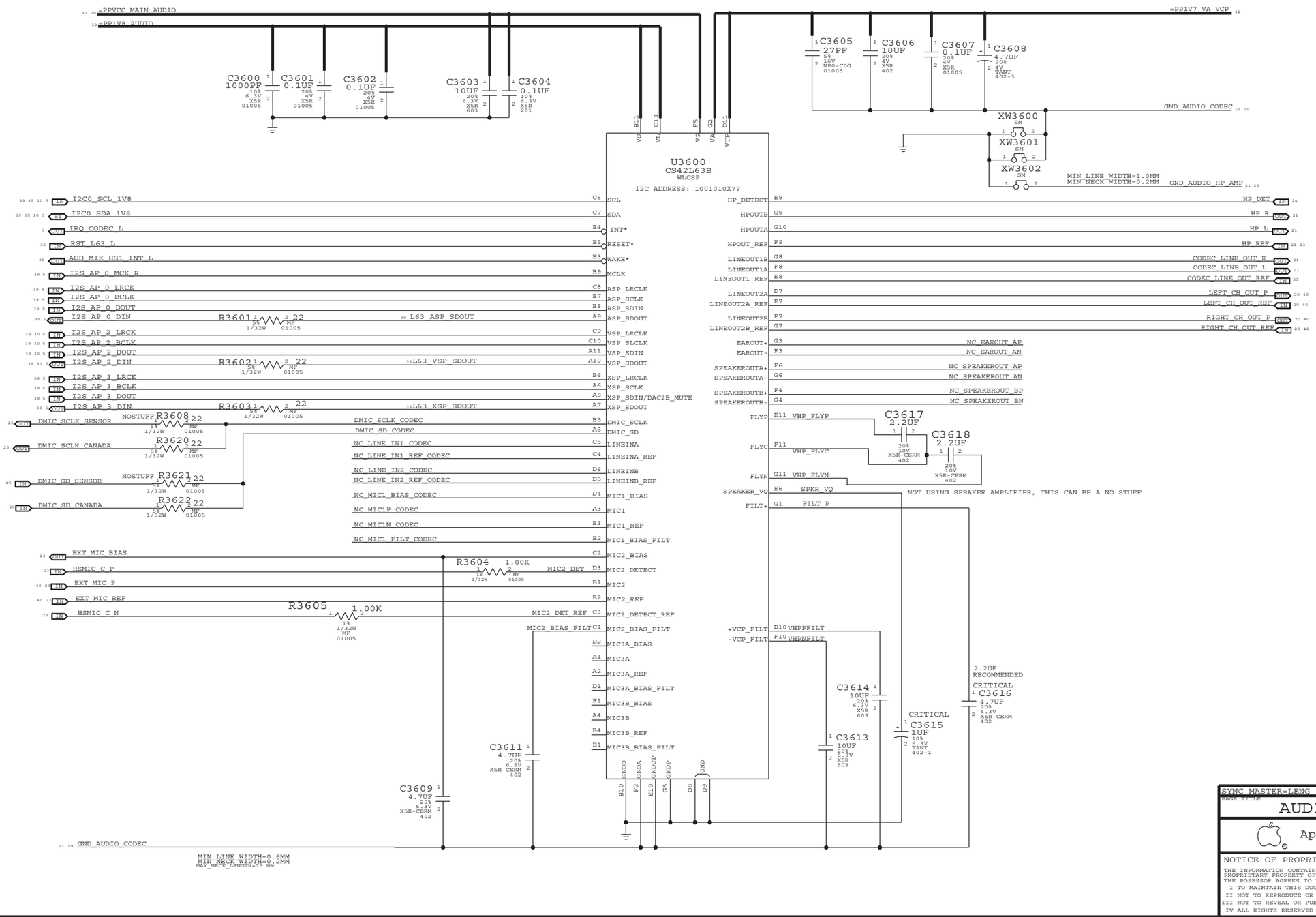
L63 AUDIO CODEC

APN:338S0940



SPEAKER AMPLIFIER

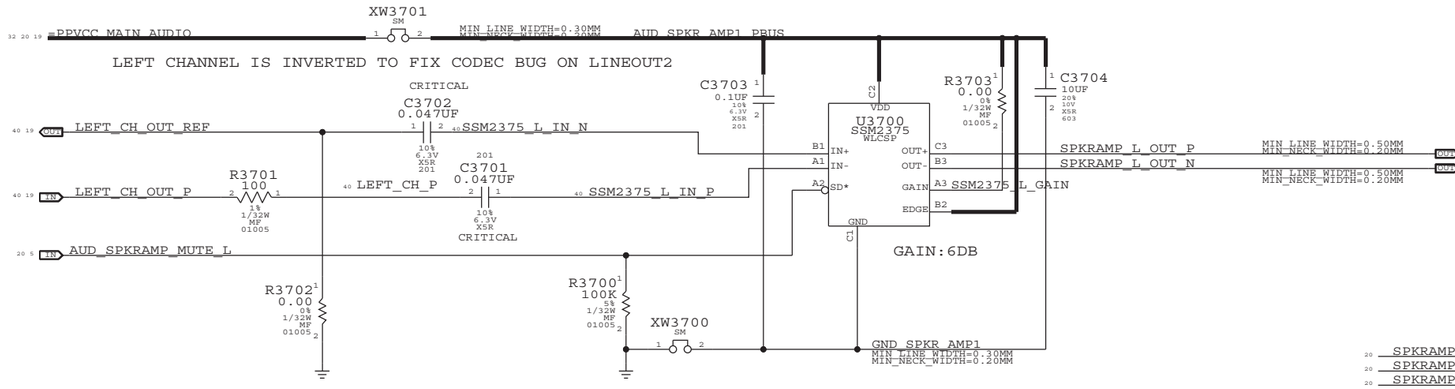
APN:353S2958

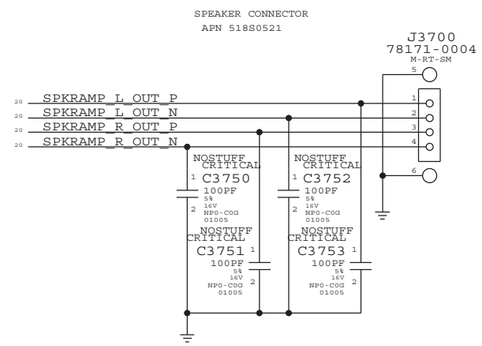
80HZ +/- XXX%

TURN ON TIME: 7.5MS

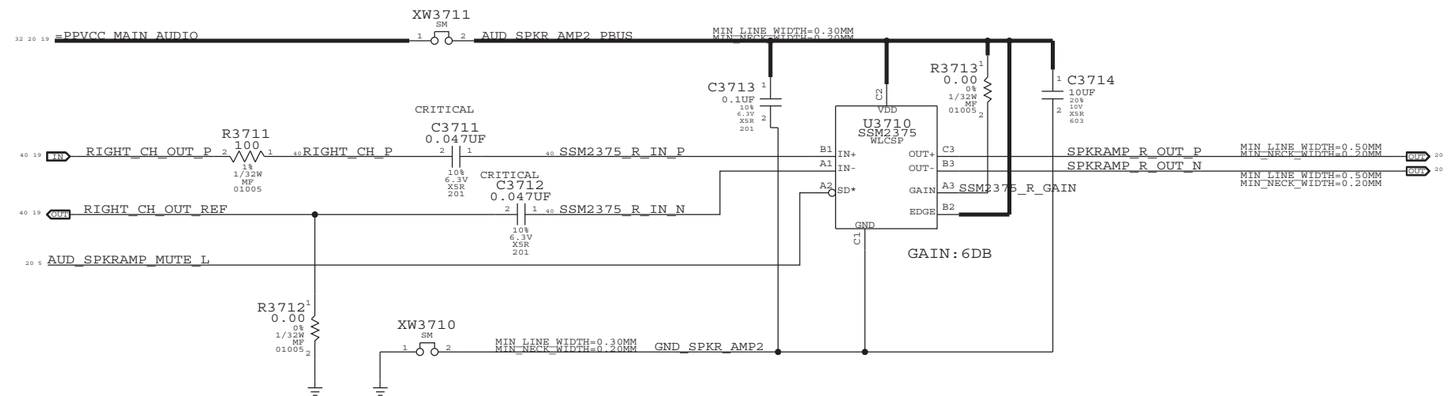
TURN ON DELAY: 20MS

GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT



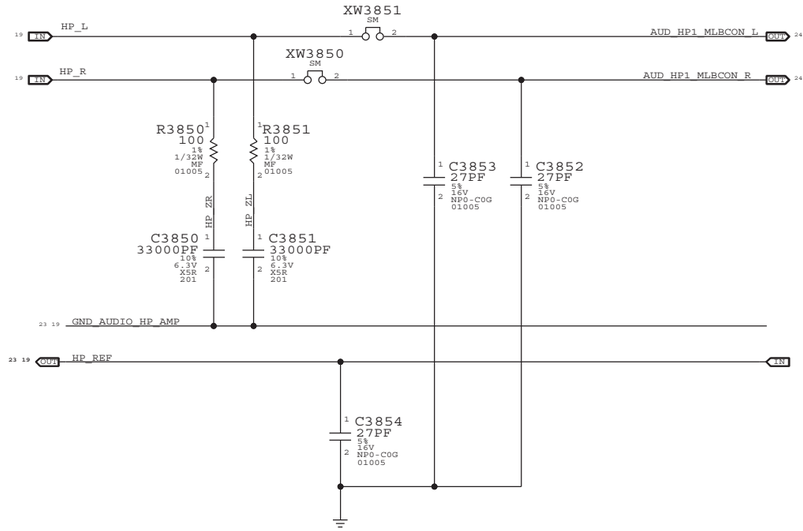


L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710

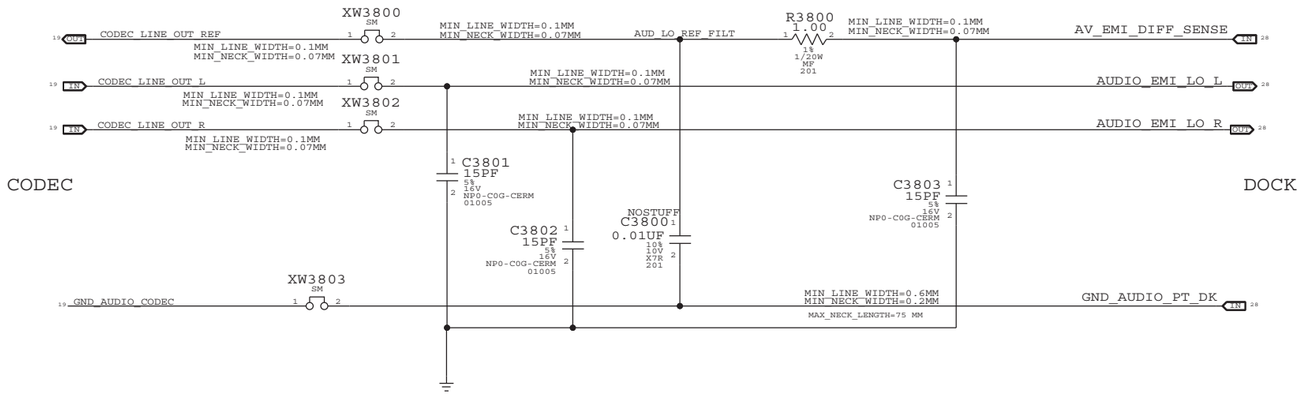


SYNC MASTER=LENG	SYNC DATE=N/A
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH: PAGE: 37 OF 106 SHEET: 20 OF 42

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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8 7 6 5 4 3 2 1

D C B A

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE

AUDIO: BLANK

Apple Inc.

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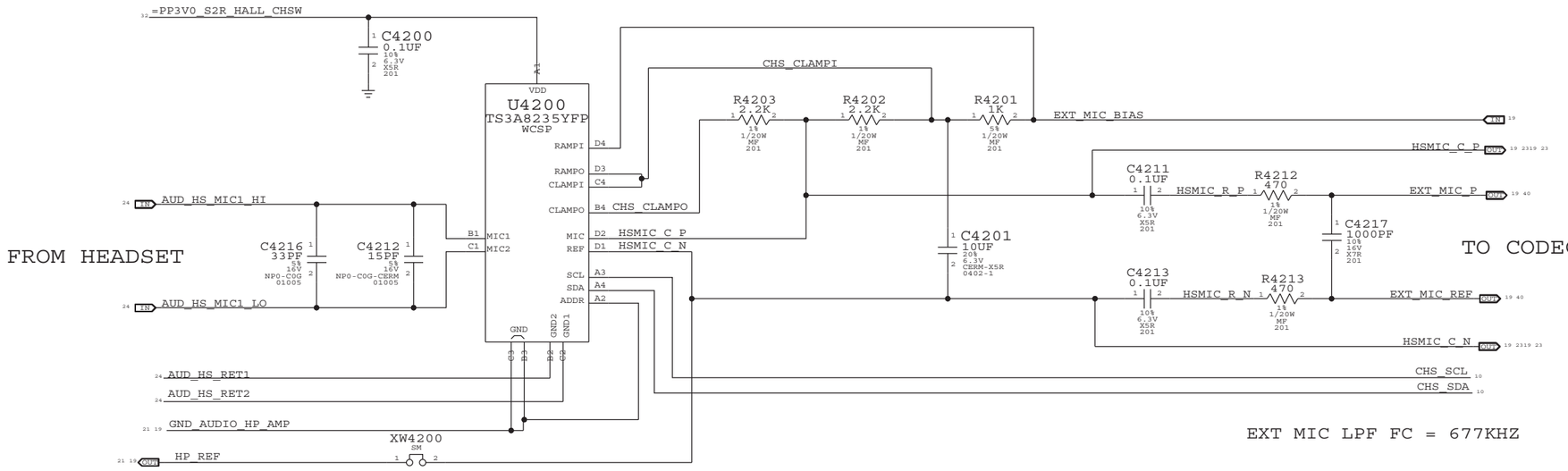
8 7 6 5 4 3 2 1

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



EXT MIC LPF FC = 677KHZ

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: DETECT/MIC BIAS

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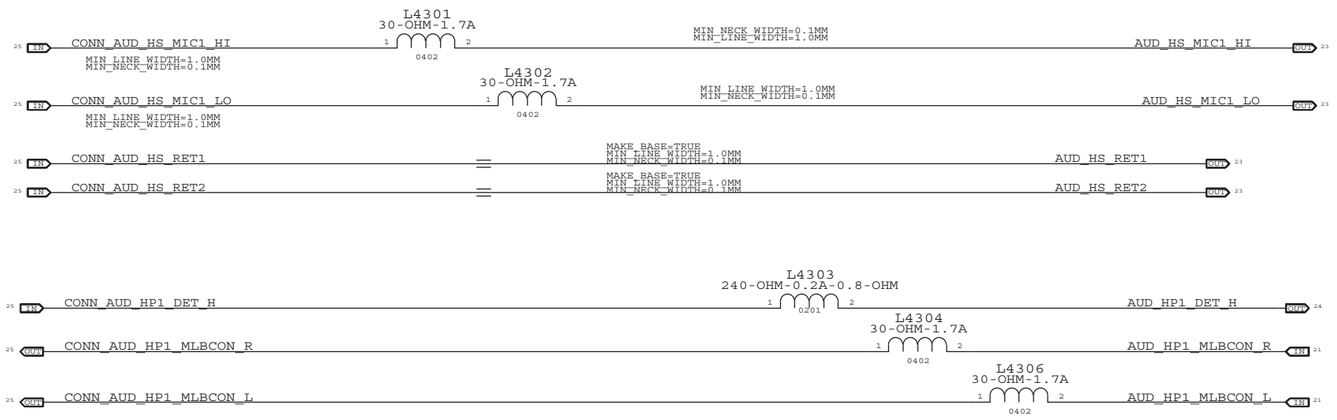
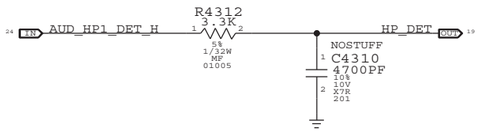
HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
PLACE ALL COMPONENTS NEAR J5501



HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG
SYNC DATE=N/A

PAGE TITLE
AUDIO: HP/MIC FILTERS

Apple Inc.

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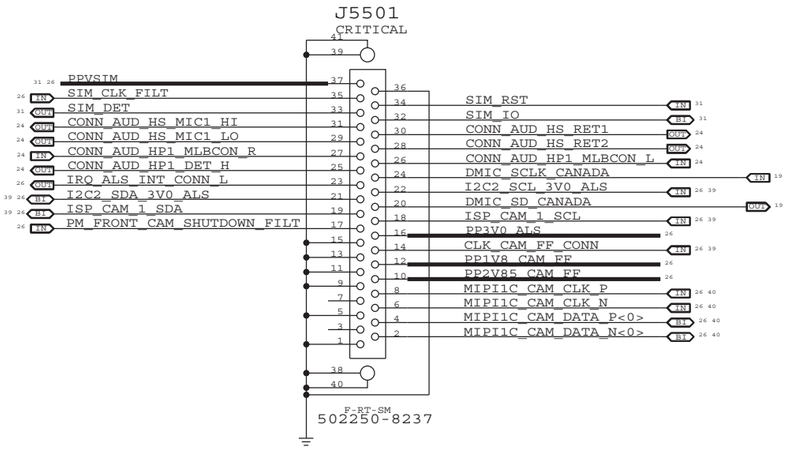
CANADA FLEXES CONN.

APN: 518S0817



SENSOR BOARD CONN ALIASES

39 27	CLK_CAM_RF_FILT	MAKE_BASE=TRUE	CONN_CLK_CAM_RF_FILT	27
40 27	MIPI0C_CAM_DATA_N<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_N<0>	27
40 27	MIPI0C_CAM_DATA_P<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_P<0>	27
		MAKE_BASE=TRUE		
40 27	MIPI0C_CAM_CLK_N	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_N	27
40 27	MIPI0C_CAM_CLK_P	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_P	27
7	PM_REAR_CAM_SHUTDOWN	MAKE_BASE=TRUE	CONN_PM_REAR_CAM_SHUTDOWN	27
27	PP1V8_SENSOR_FILT	MAKE_BASE=TRUE	CONN_PP1V8_SENSOR_FILT	27
27	PP2V85_CAM_REAR	MAKE_BASE=TRUE	CONN_PP2V85_CAM_REAR	27
19	DMIC_SD_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SD_SENSOR	27
19	DMIC_SCLK_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SCLK_SENSOR	27
39 7	ISP_AP_0_SCL	MAKE_BASE=TRUE	CONN_ISP_AP_0_SCL	27
39 7	ISP_AP_0_SDA	MAKE_BASE=TRUE	CONN_ISP_AP_0_SDA	27
39 26 5	I2C2_SCL_3V0	MAKE_BASE=TRUE	CONN_I2C2_SCL_3V0	27
39 26 5	I2C2_SDA_3V0	MAKE_BASE=TRUE	CONN_I2C2_SDA_3V0	27
5	IRQ_ACCEL_INT1_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT1_L	27
5	IRQ_ACCEL_INT2_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT2_L	27
5	IRQ_GYRO_INT1	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT1	27
5	IRQ_GYRO_INT2	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT2	27
39 5	I2C1_SCL_1V8	MAKE_BASE=TRUE	CONN_I2C1_SCL_1V8	27
39 5	I2C1_SDA_1V8	MAKE_BASE=TRUE	CONN_I2C1_SDA_1V8	27
35	IRQ_HALL	MAKE_BASE=TRUE	CONN_IRQ_HALL	27
5	IRQ_PROX_INT_L	MAKE_BASE=TRUE	CONN_IRQ_PROX_INT_L	27
27	PP3V0_S2R_HALL_FILT	MAKE_BASE=TRUE	CONN_PP3V0_S2R_HALL	27
35 5	ONOFF_L	MAKE_BASE=TRUE	CONN_ONOFF_FTR_L	27
35 5	SRL_L	MAKE_BASE=TRUE	CONN_SRL_FTR_L	27
5	AUD_VOL_UP_L	MAKE_BASE=TRUE	CONN_AUD_VOL_UP_FTR_L	27
5	AUD_VOL_DOWN_L	MAKE_BASE=TRUE	CONN_AUD_VOL_DOWN_FTR_L	27
		MAKE_BASE=TRUE		
27	PP3V0_OPTICAL_SENS	MAKE_BASE=TRUE	CONN_PP3V0_OPTICAL_SENS	27

SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES

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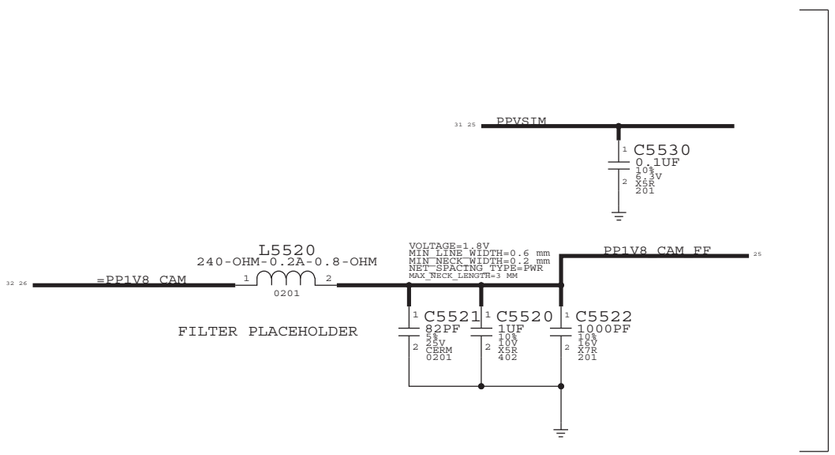
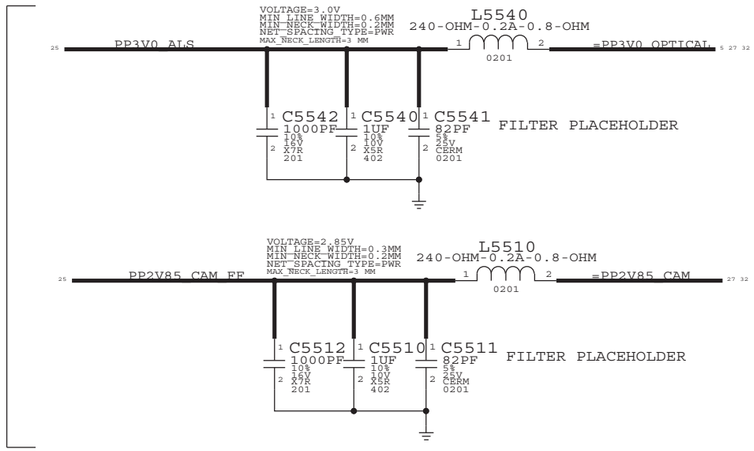
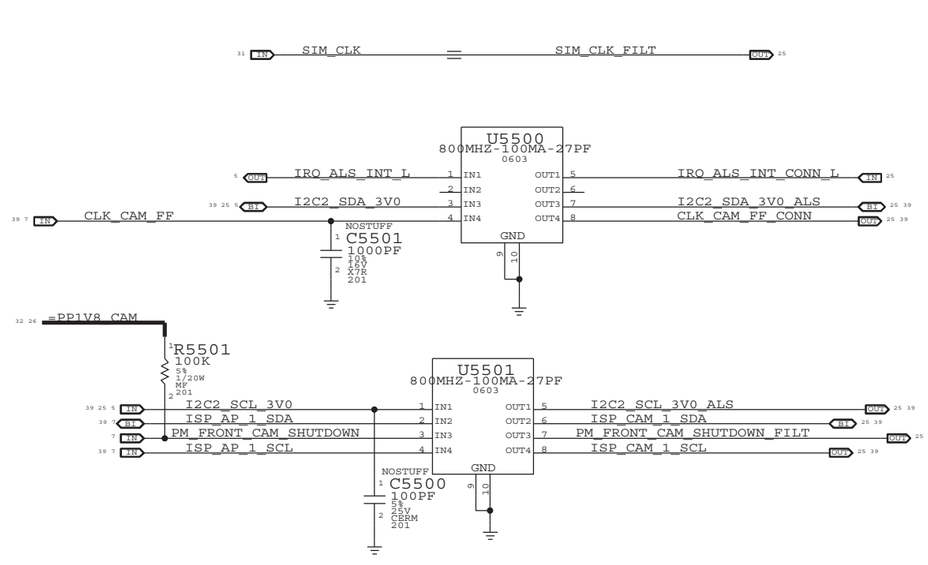
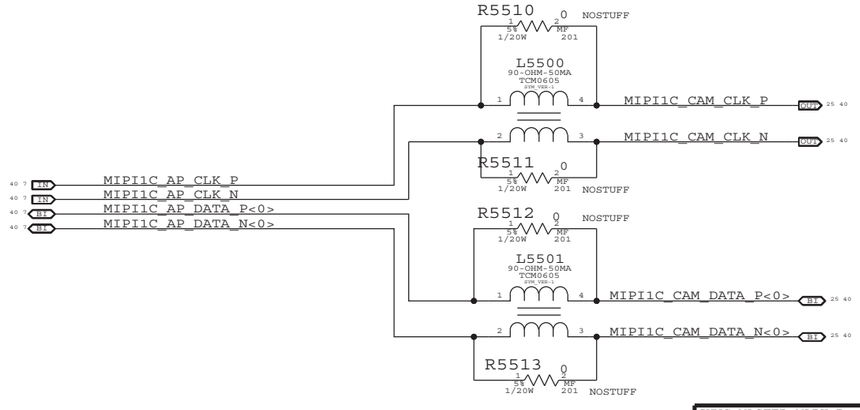


CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS





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PAGE TITLE
CONNECTOR: CANADA FLEX FILTERS

Apple Inc.

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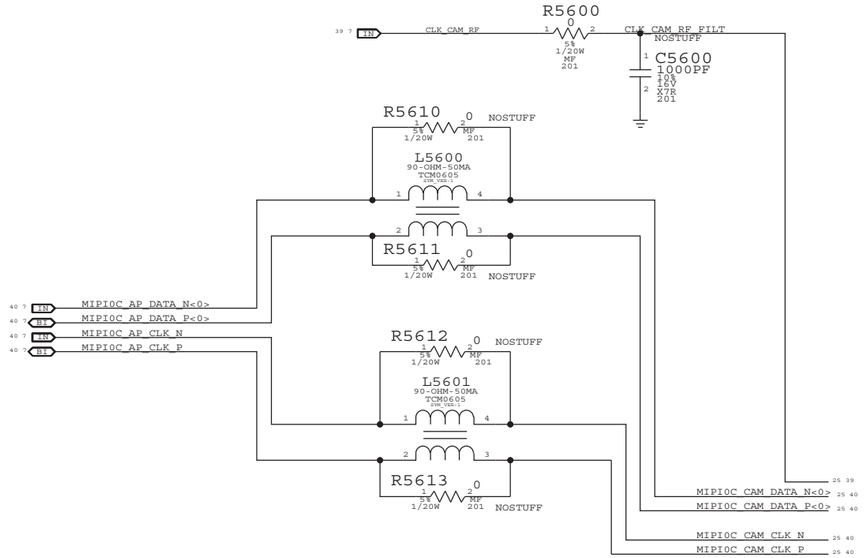
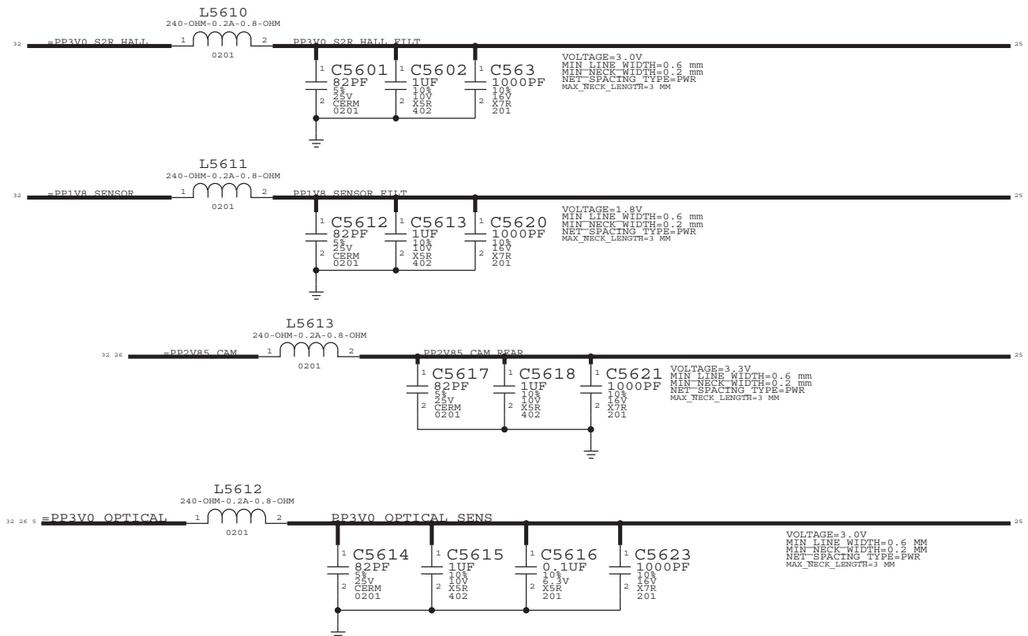
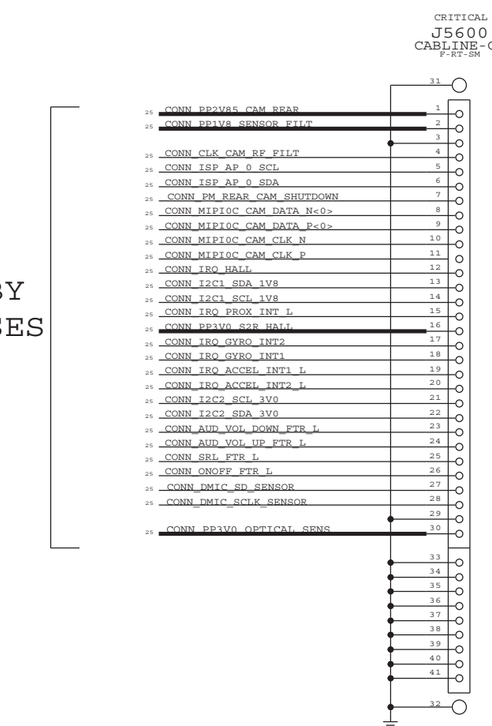




CONNECTED BY
PG 54 ALIASES

SENSOR PANEL CONNECTOR
CABLINE-CA CONNECTOR: 518S0787



SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: SENSOR PANEL CONNECTOR

Apple Inc.

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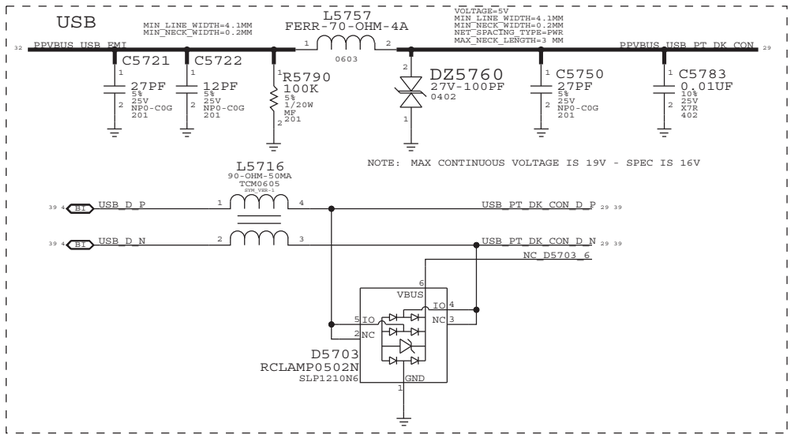

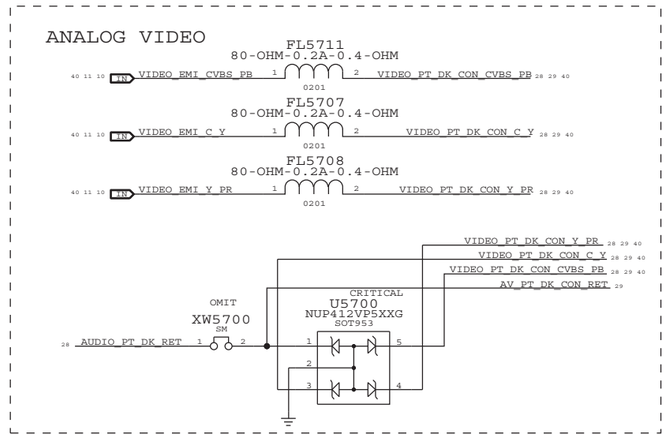

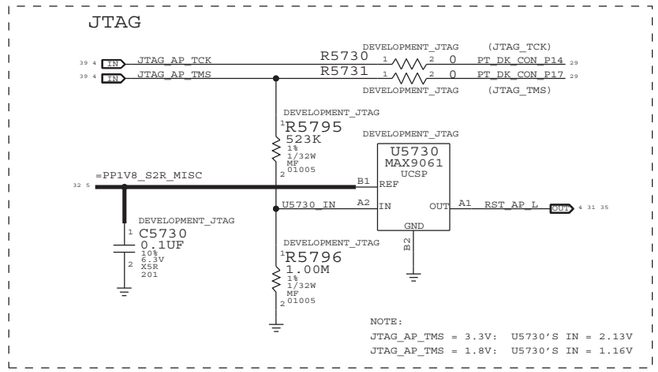

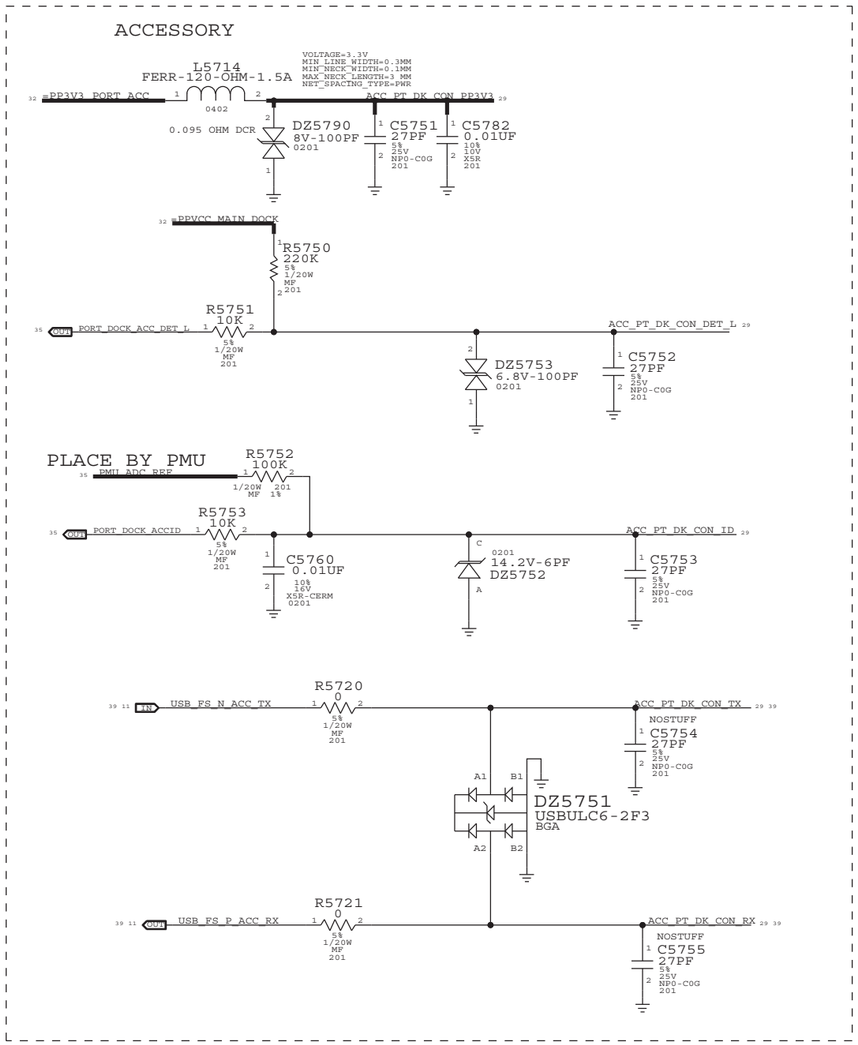

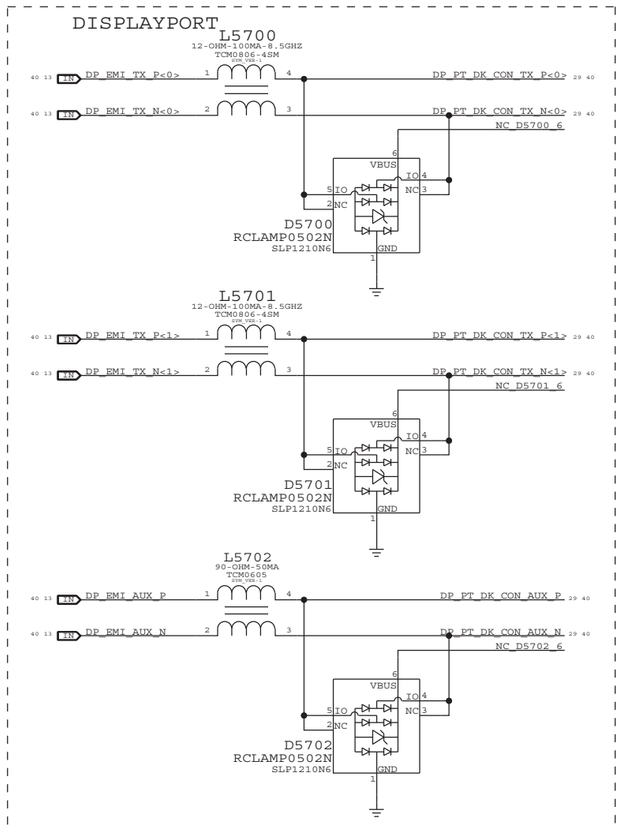

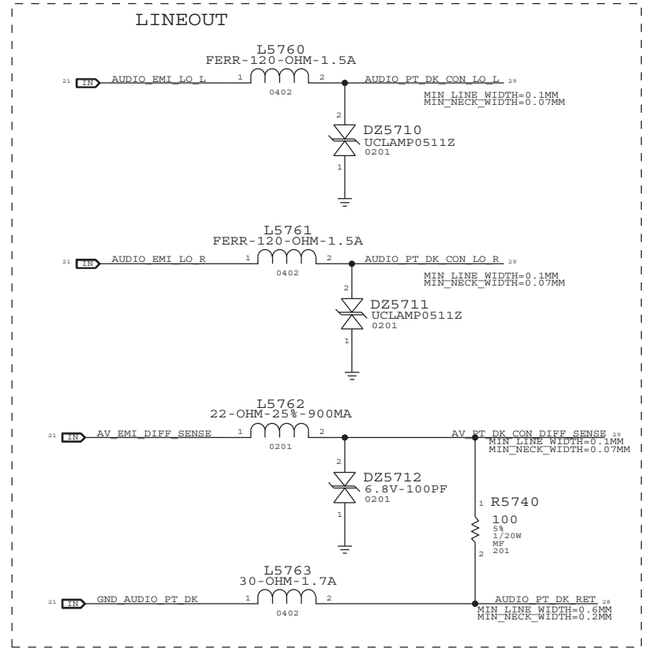

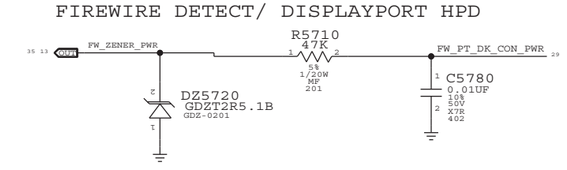

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DZ5710,DZ5711	RADAR:8379541
377S0107	377S0066		DZ5700,DZ5701,DZ5702,DZ5712	RADAR:8289785
155S0625	155S0559		L5700,L5701	RADAR:8423156

SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE
IO FLEX: DOCK COMPONENTS

Apple Inc.

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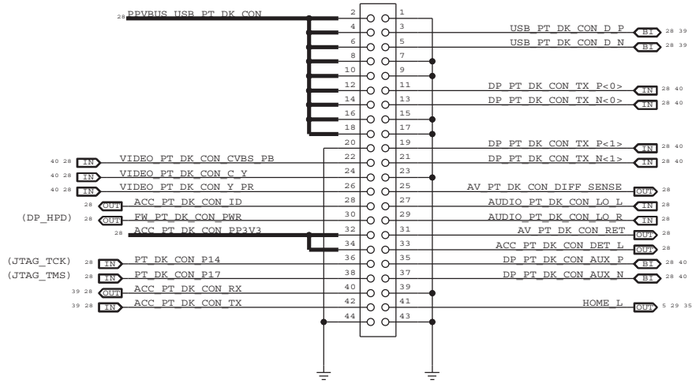
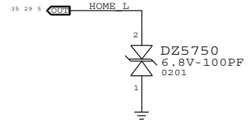
PN 516S0817 (PLUG - MALE)

CRITICAL

J5900
AXK844135WG
M-ST-SM





SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
IO FELX: B2B Connector

Apple Inc.

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SIZE D
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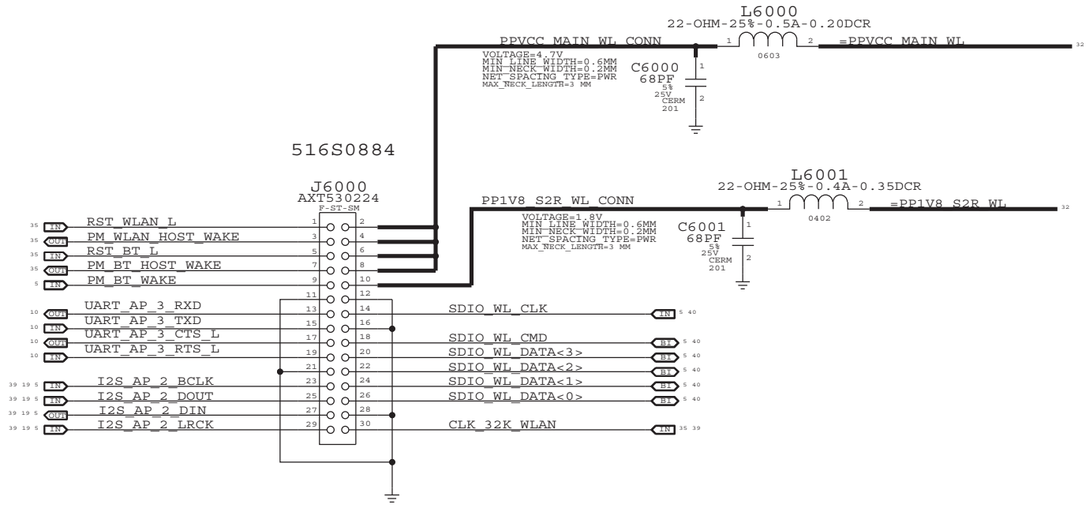
X23 WIFI/BT CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X23 WIFI/BT

Apple Inc.

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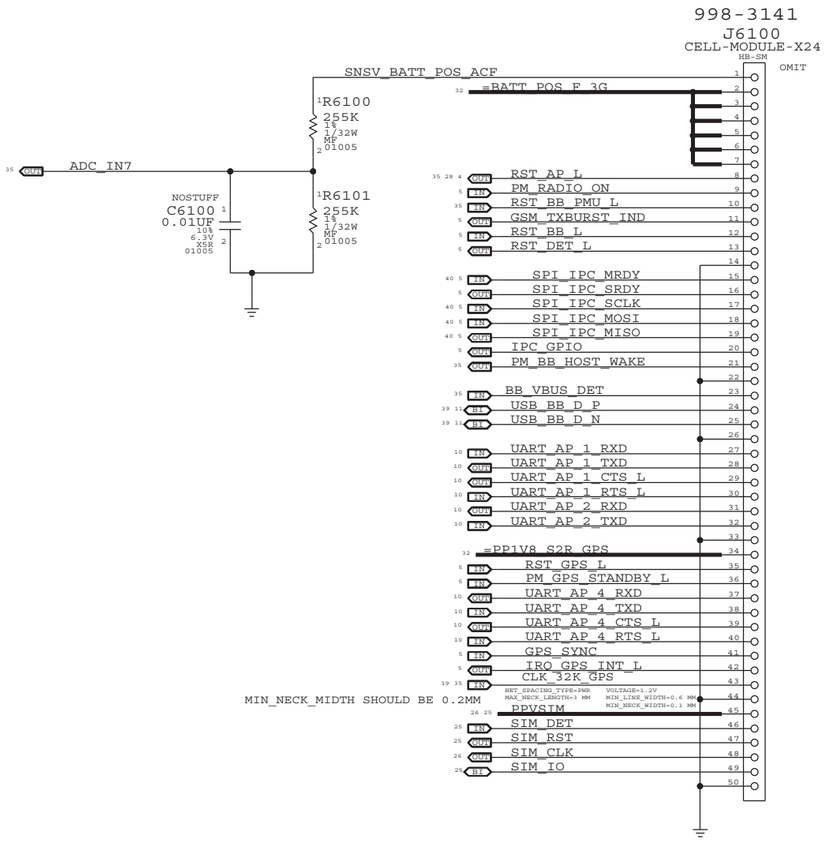
X24 CELLULAR/GPS CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X24 CELLULAR/GPS

Apple Inc.

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POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

34 PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_S2R_HALL 27
= =PP3V0_S2R_HALL_CHSW 23

34 PP1V7_VA_VCP = =PP1V7_VA_VCP 19
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V0_VIDEO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_VIDEO_BUFFER 11
= =PP3V0_VIDEO_H4 7

34 PP3V0_OPTICAL = =PP3V0_OPTICAL 5 26 27
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V2_SD
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V3_ACC = =PP3V3_PORT_ACC 28
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V0_VIDEO_BUF = =PP3V0_VIDEO_BUF 11
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V2_S2R_USBMUX = =PP3V2_S2R_USBMUX 11
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V0_IO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_IO_H4 7 9
= =PP3V0_IO_MISC 13

34 PP2V85_CAM = =PP2V85_CAM 26 27
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V0_GRAPE = =PP3V0_GRAPE 17 18
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_GRAPE_Z1 18
= =PP3V0_GRAPE_Z2 18
= =PP3V0_GRAPE_MARIO1 17

34 PP1V1
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
= =PP1V1_PLL_H4 4
= =PP1V1_MIPI_H4 7
= =PP1V1_DPORT_H4 7
= =PP1V1_USB_H4 4
MIN_NECK_MIDTH SHOULD BE 0.2MM = =PP1V1_MIPI_PLL_H4 4

34 PP1V8_ALWAYS = =PP1V8_ALWAYS 5
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

BUCK RAILS

34 PP1V2_SOC = =PPVDD_SOC_H4 9
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM MIN_NECK_MIDTH SHOULD BE 0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM

34 PP1V2_CPU = =PPVDD_CPU_H4 9
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM MIN_NECK_MIDTH SHOULD BE 0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM

34 PP1V2_S2R = =PP1V2_S2R_H4 8
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM MIN_NECK_MIDTH SHOULD BE 0.2MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM

34 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V8_S2R_H4 8
= =PP1V8_S2R_WL 30
= =PP1V8_S2R_GPS 31
= =PP1V8_S2R_MISC 5 28

34 PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
= =PP1V8_CAM 26
= =PP1V8_SENSOR 27
= =PP1V8_AUDIO 19
= =PP1V8_H4 4 5 7 10 13
MIN_NECK_MIDTH SHOULD BE 0.2MM = =PP1V8_VDDIO18_H4 8 9
= =PP1V8_MIPI_H4 7
= =PP1V8_DPORT_H4 7

34 PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
= =PP3V3_NAND 12
= =PP3V3_USB_H4 4
= =PP3V3_MLC_HI 36
= =PP3V3_LCD 16
MIN_NECK_MIDTH SHOULD BE 0.2MM = =PP3V3_NAND_H4 10

35 PPLED_OUT = =PPLED_REG 16
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM NET_SPACING_TYPE=PWR
MIN_NECK_WIDTH=0.2 MM MAX_NECK_LENGTH=3 MM

36 PP3V3_MLC_OUT = =PP3V3_MLC 14 16
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
= =PP1V2_VDDQ_H4 8
= =PP1V2_VDDIOD_H4 8
= =PP1V2_HSIC_H4 4
MIN_NECK_MIDTH SHOULD BE 0.2MM

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.10MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

CHARGER MAIN

35 34 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PPVCC_MAIN_AUDIO 19 20
= =PPVCC_MAIN_WL 30
= =PPVCC_MAIN_DOCK 28
= =PPVCC_MAIN_LED 35

BATTERY

37 34 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=1.7 MM
= =BATT_POS_F_3G 31
= =BATT_POS_CONN 33

USB POWER INPUT

28 PPVBUS_USB_EMI = PPVBUS_USB_DCIN 34
MAKE_BASE=TRUE

SYNC_MASTER=YOSH SYNC_DATE=N/A
PAGE TITLE
POWER: ALIASES

Apple Inc.

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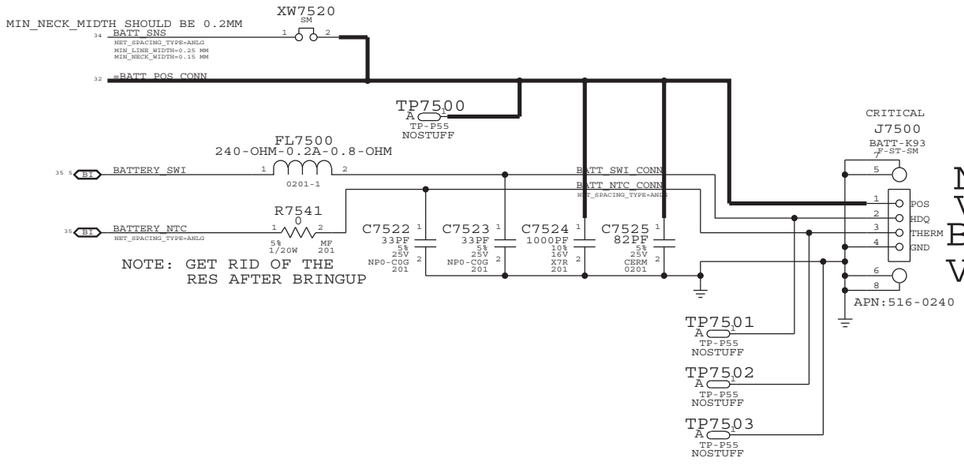

NOTE:
VERIFY PINOUT OF
BATTERY CONNECTOR
VERIFY MOUNTING CONN TO GND

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: BATTERY CONNECTOR

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0542	1	IC,PMU,ALISON,D1946A2,OTPXX,UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299		Y8138	ALT FOUNDRY

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

NOTE: FOR NO BATTERY SITUATION

VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 1UF CAP AT EACH VDD INPUT)

NOTE: CONCERNED ABOUT ESR > 20MOHM

LDO BYPASS

ADDITIONAL DISTRIBUTED:
PP1V2: 30UF (NO DE-RATING)
PP1V8: 6UF (NO DE-RATING)

SYNC_MASTER=YOSH	SYNC_DATE=N/A
PAGE TITLE	POWER: PMU
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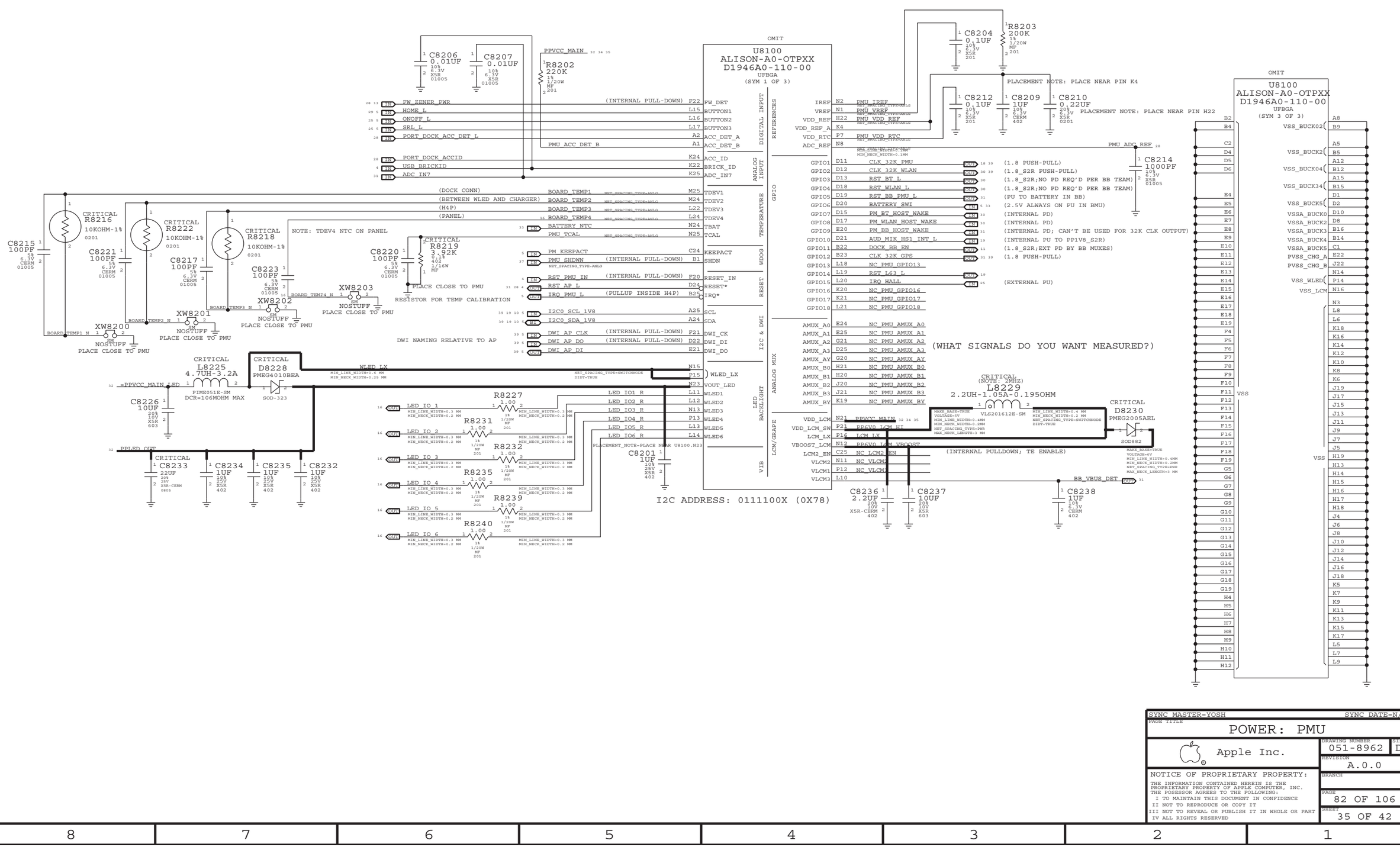

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE

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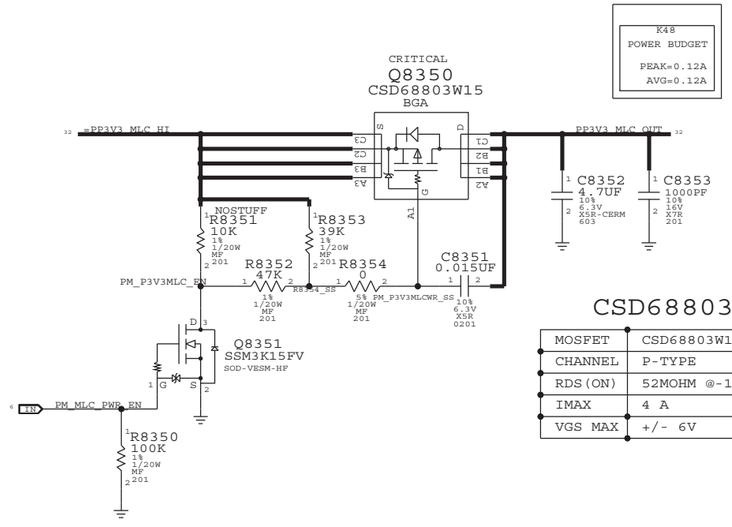

K48
POWER BUDGET
PEAK=0.12A
AVG=0.12A

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS(ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0972	376S0612		Q8351	RADAR:8537160

SYNC MASTER=YOSH SYNC DATE=N/A

PAGE TITLE
POWER: 3.3V MLC & 1.2V VR

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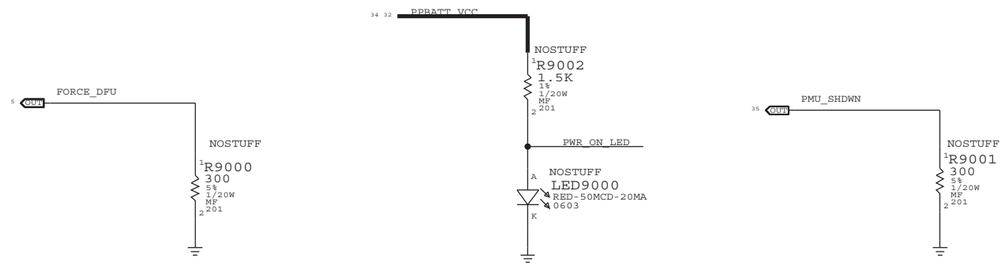
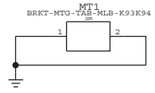
DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: DEBUG AND MISC

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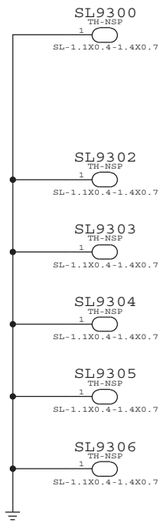
PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
FCT/ICT TEST/BRACKETS

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H63	CLK_50S	CLK	CLK_32K_PMU	18 35
H62	CLK_50S	CLK	CLK_32K_WLAN	30 35
H61	CLK_50S	CLK	CLK_32K_GPS	31 35
H88	CLK_50S	CLK	CLK_CAM_FF	7 26
H80	CLK_50S	CLK	CLK_CAM_FF_FILT	
H95	CLK_50S	CLK	CLK_CAM_FF_CONN	25 26
H96	CLK_50S	CLK	CLK_CAM_RF	7 27
H94	CLK_50S	CLK	CLK_CAM_RF_FILT	25 27
H130	CLK_50S	CLK	I2S_AP_0_MCK	5
H132	CLK_50S	CLK	I2S_AP_0_MCK_R	5 19
H157	CLK_50S	CLK	CLK_CAM_FF_R	7
H158	CLK_50S	CLK	CLK_CAM_RF_R	7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H50	NAND_50S	NAND	F0AD<7..0>	6 12
H49	NAND_50S	NAND	F0CE0_L	6 12
H48	NAND_50S	NAND	F0CE1_L	6 12
H47	NAND_50S	NAND	F0CE2_L	6 12
H46	NAND_50S	NAND	F0CE3_L	6 12
H167	NAND_50S	NAND	F0CE4_L	6 12
H164	NAND_50S	NAND	F0CE5_L	6 12
H166	NAND_50S	NAND	F0CE6_L	6 12
H165	NAND_50S	NAND	F0CE7_L	6 12
H41	NAND_50S	NAND	F0CLE	6 12
H42	NAND_50S	NAND	F0ALE	6 12
H43	NAND_50S	NAND	F0RE_L	6 12
H44	NAND_50S	NAND	F0WE_L	6 12
H37	NAND_50S	NAND	F0WP_L	
H49	NAND_50S	NAND	F1AD<7..0>	6 12
H51	NAND_50S	NAND	F1CE0_L	6 12
H52	NAND_50S	NAND	F1CE1_L	6 12
H53	NAND_50S	NAND	F1CE2_L	6 12
H54	NAND_50S	NAND	F1CE3_L	6 12
H167	NAND_50S	NAND	F1CE4_L	6 12
H164	NAND_50S	NAND	F1CE5_L	6 12
H166	NAND_50S	NAND	F1CE6_L	6 12
H165	NAND_50S	NAND	F1CE7_L	6 12
H171	NAND_50S	NAND	F1CLE	6 12
H55	NAND_50S	NAND	F1ALE	6 12
H56	NAND_50S	NAND	F1RE_L	6 12
H57	NAND_50S	NAND	F1WE_L	6 12
H58	NAND_50S	NAND	F1WP_L	
H59				
H100	NAND_50S	NAND	F2AD<7..0>	
H102	NAND_50S	NAND	F2CE0_L	
H103	NAND_50S	NAND	F2CE1_L	
H104	NAND_50S	NAND	F2CE2_L	
H105	NAND_50S	NAND	F2CE3_L	
H107	NAND_50S	NAND	F2CLE	
H109	NAND_50S	NAND	F2ALE	
H110	NAND_50S	NAND	F2RE_L	
H111	NAND_50S	NAND	F2WE_L	
H112	NAND_50S	NAND	F2WP_L	
H113	NAND_50S	NAND	F3AD<7..0>	
H114	NAND_50S	NAND	F3CE0_L	
H115	NAND_50S	NAND	F3CE1_L	
H116	NAND_50S	NAND	F3CE2_L	
H117	NAND_50S	NAND	F3CE3_L	
H119	NAND_50S	NAND	F3CLE	
H120	NAND_50S	NAND	F3ALE	
H121	NAND_50S	NAND	F3RE_L	
H122	NAND_50S	NAND	F3WE_L	
H123	NAND_50S	NAND	F3WP_L	

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H16		JTAG	JTAG_AP_TCK	4 28
H15		JTAG	JTAG_AP_TMS	4 28
H14		JTAG	JTAG_AP_TDI	4 10
H13		JTAG	JTAG_AP_TDO	4 10
H20		JTAG	JTAG_AP_TRST_L	4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H1	I2C_50S	I2C	I2C1_SDA_1V8	5 25
H2	I2C_50S	I2C	I2C1_SCL_1V8	5 25
H3	I2C_50S	I2C	I2C0_SDA_1V8	5 10 19 35
H4	I2C_50S	I2C	I2C0_SCL_1V8	5 10 19 35
H91	I2C_50S	I2C	I2C2_SDA_3V0	5 25 26
H92	I2C_50S	I2C	I2C2_SCL_3V0	5 25 26
H98	I2C_50S	I2C	ISP_AP_0_SCL	7 25
H99	I2C_50S	I2C	ISP_AP_0_SDA	7 25
H100	I2C_50S	I2C	ISP_AP_1_SCL	7 26
H101	I2C_50S	I2C	ISP_AP_1_SDA	7 26
H106	I2C_50S	I2C	I2C2_SCL_3V0_ALS	25 26
H105	I2C_50S	I2C	I2C2_SDA_3V0_ALS	25 26
H124	I2C_50S	I2C	ISP_CAM_1_SCL	25 26
H125	I2C_50S	I2C	ISP_CAM_1_SDA	25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H92		CRYSTAL	XTAL_24M_I	4
H90		CRYSTAL	XTAL_24M_O	4
H91		CRYSTAL	24M_O	4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H133		VREF	PPVREF_DDR0_CA	8
H131		VREF	PPVREF_DDR0_DQ	8
H135		VREF	PPVREF_DDR1_CA	8
H137		VREF	PPVREF_DDR1_DQ	8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H5	USB_90D	USB	USB_D_P	4 28
H6	USB_90D	USB	USB_D_N	4 28
H7	USB_90D	USB	USB_PT_DK_CON_D_P	28 29
H8	USB_90D	USB	USB_PT_DK_CON_D_N	28 29
H82	USB_90D	USB	USB_BB_D_P	11 31
H83	USB_90D	USB	USB_BB_D_N	11 31
H84	USB_90D	USB	USB_FS_D_P	4 11
H85	USB_90D	USB	USB_FS_D_N	4 11
H128	USB_90D	USB	USB_FS_N_ACC_TX	11 28
H129	USB_90D	USB	USB_FS_P_ACC_RX	11 28
H127	USB_90D	USB	ACC_PT_DK_CON_TX	28 29
H126	USB_90D	USB	ACC_PT_DK_CON_RX	28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H40	I2S_50S	I2S	I2S_AP_0_BCLK	5 19
H38	I2S_50S	I2S	I2S_AP_0_LRCK	5 19
H39	I2S_50S	I2S	I2S_AP_0_DIN	5 19
H45	I2S_50S	I2S	I2S_AP_0_DOUT	5 19
H60	I2S_50S	I2S	L63_ASP_SDOUT	19
H40	I2S_50S	I2S	I2S_AP_2_BCLK	5 19 30
H38	I2S_50S	I2S	I2S_AP_2_LRCK	5 19 30
H39	I2S_50S	I2S	I2S_AP_2_DIN	5 19 30
H45	I2S_50S	I2S	I2S_AP_2_DOUT	5 19 30
H60	I2S_50S	I2S	L63_VSP_SDOUT	19
H40	I2S_50S	I2S	I2S_AP_3_BCLK	5 19
H38	I2S_50S	I2S	I2S_AP_3_LRCK	5 19
H39	I2S_50S	I2S	I2S_AP_3_DIN	5 19
H45	I2S_50S	I2S	I2S_AP_3_DOUT	5 19
H60	I2S_50S	I2S	L63_XSP_SDOUT	19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
H40		DWI	DWI_AP_CLK	5 35
H38		DWI	DWI_AP_DI	5 35
H39		DWI	DWI_AP_DO	5 35

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: CONSTRAINTS: ASSIGNMENTS

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ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
P214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
P215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
P216	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
P217	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
P218	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
P219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 28
P220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 28
P222	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 28
P223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 28 29
P224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 28 29
P227	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P236	LVDS_100D	LVDS	LVDS_DATA_P<2..0> 14 16
P238	LVDS_100D	LVDS	LVDS_DATA_N<2..0> 14 16
P240	LVDS_100D	LVDS	LVDS_DATA_CONN_P<2..0> 16
P242	LVDS_100D	LVDS	LVDS_DATA_CONN_N<2..0> 16
P244	LVDS_100D	LVDS	LVDS_CLK_P 14 16
P246	LVDS_100D	LVDS	LVDS_CLK_N 14 16
P248	LVDS_100D	LVDS	LVDS_CLK_CONN_P 16
P250	LVDS_100D	LVDS	LVDS_CLK_CONN_N 16

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P191	MIPI_100D	MIPI	MIPID_AP_DATA_P<0> 7 14
P192	MIPI_100D	MIPI	MIPID_AP_DATA_N<0> 7 14
P193	MIPI_100D	MIPI	MIPID_AP_DATA_P<1> 7 14
P194	MIPI_100D	MIPI	MIPID_AP_DATA_N<1> 7 14
P195	MIPI_100D	MIPI	MIPID_AP_DATA_P<2> 7 14
P196	MIPI_100D	MIPI	MIPID_AP_DATA_N<2> 7 14
P227	MIPI_100D	MIPI	MIPID_AP_DATA_P<3> 7 14
P270	MIPI_100D	MIPI	MIPID_AP_DATA_N<3> 7 14
P197	MIPI_100D	MIPI	MIPID_AP_CLK_P 7 14
P198	MIPI_100D	MIPI	MIPID_AP_CLK_N 7 14
P331	MIPI_100D	MIPI	MIPI0C_AP_DATA_P<0> 7 27
P332	MIPI_100D	MIPI	MIPI0C_AP_DATA_N<0> 7 27
P333	MIPI_100D	MIPI	MIPI0C_AP_CLK_P 7 27
P334	MIPI_100D	MIPI	MIPI0C_AP_CLK_N 7 27
P343	MIPI_100D	MIPI	MIPI0C_CAM_DATA_P<0> 25 27
P344	MIPI_100D	MIPI	MIPI0C_CAM_DATA_N<0> 25 27
P341	MIPI_100D	MIPI	MIPI0C_CAM_CLK_P 25 27
P342	MIPI_100D	MIPI	MIPI0C_CAM_CLK_N 25 27
P345	MIPI_100D	MIPI	MIPI1C_AP_DATA_P<0> 7 26
P346	MIPI_100D	MIPI	MIPI1C_AP_DATA_N<0> 7 26
P347	MIPI_100D	MIPI	MIPI1C_AP_CLK_P 7 26
P348	MIPI_100D	MIPI	MIPI1C_AP_CLK_N 7 26
P339	MIPI_100D	MIPI	MIPI1C_CAM_DATA_P<0> 25 26
P340	MIPI_100D	MIPI	MIPI1C_CAM_DATA_N<0> 25 26
P335	MIPI_100D	MIPI	MIPI1C_CAM_CLK_P 25 26
P336	MIPI_100D	MIPI	MIPI1C_CAM_CLK_N 25 26

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P249	DP_100D	DP	DP_AP_TX_P<0> 7 10 13
P245	DP_100D	DP	DP_AP_TX_N<0> 7 10 13
P246	DP_100D	DP	DP_AP_TX_P<1> 7 10 13
P250	DP_100D	DP	DP_AP_TX_N<1> 7 10 13
P251	DP_100D	DP	DP_AP_AUX_P 7 13
P252	DP_100D	DP	DP_AP_AUX_N 7 13
P273	DP_100D	DP	DP_EMI_TX_P<0> 13 28
P274	DP_100D	DP	DP_EMI_TX_N<0> 13 28
P275	DP_100D	DP	DP_EMI_TX_P<1> 13 28
P276	DP_100D	DP	DP_EMI_TX_N<1> 13 28
P277	DP_100D	DP	DP_EMI_AUX_P 13 28
P272	DP_100D	DP	DP_EMI_AUX_N 13 28
P327	DP_100D	DP	DP_PT_DK_CON_TX_P<0> 28 29
P324	DP_100D	DP	DP_PT_DK_CON_TX_N<0> 28 29
P328	DP_100D	DP	DP_PT_DK_CON_TX_P<1> 28 29
P331	DP_100D	DP	DP_PT_DK_CON_TX_N<1> 28 29
P330	DP_100D	DP	DP_PT_DK_CON_AUX_P 28 29
P332	DP_100D	DP	DP_PT_DK_CON_AUX_N 28 29

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P189	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
P188	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
P186	AUDIO	AUDIO	LEFT_CH_P 20
P187	AUDIO	AUDIO	SSM2375_L_IN_P 20
P185	AUDIO	AUDIO	SSM2375_L_IN_N 20
P224	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
P192	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
P193	AUDIO	AUDIO	RIGHT_CH_P 20
P194	AUDIO	AUDIO	SSM2375_R_IN_P 20
P195	AUDIO	AUDIO	SSM2375_R_IN_N 20
P172	AUDIO	AUDIO	EXT_MIC_P 19 23
P173	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P600	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
P598	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R
P599	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
P596	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
P166	SPI_50S	SPI	SPI_GRAPE_MISO 5 17
P164	SPI_50S	SPI	SPI_GRAPE_MOSI 5 17
P163	SPI_50S	SPI	SPI_GRAPE_SCLK 5 17
P162	SPI_50S	SPI	SPI_GRAPE_CS_L 5 17
P160	SPI_50S	SPI	SPI_IPC_MISO 5 31
P158	SPI_50S	SPI	SPI_IPC_MOSI 5 31
P159	SPI_50S	SPI	SPI_IPC_SCLK 5 31
P157	SPI_50S	SPI	SPI_IPC_MRDY 5 31

SYNC_MASTER=MIKE SYNC_DATE=N/A

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2,ISL3,ISL8,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2,ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES
100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL3,ISL8,ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC MASTER=MIKE SYNC DATE=N/A

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CONSTRAINTS: MLB RULES

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