

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# SCHEM, MLB, M96

## EVT

08/01/2008

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE

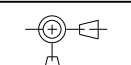

Page	Contents	Sync
1	Table of Contents	N/A
2	System Block Diagram	WFERRY-WF
3	Power Block Diagram	POWER
4	CONFIGURATION OPTIONS	(N/A)
5	Acoustic Cap BOM Config Tables	N/A
6	Functional Test and No-Tests	(MASTER)
7	Power Aliases	WFERRY
8	SIGNAL ALIAS /RESET	(MASTER)
9	CPU FSB	M97
10	CPU Power & Ground	(MASTER)
11	CPU Decoupling & VID	MSARWAR
12	eXtended Debug Port (XDP)	M97
13	MCP CPU Interface	M97
14	MCP Memory Interface	M97
15	MCP Memory Misc	M97
16	MCP PCIe Interfaces	M97
17	MCP Ethernet & Graphics	M97
18	MCP PCI & LPC	M97
19	MCP SATA & USB	M97
20	MCP HDA & MISC	M97
21	MCP Power & Ground	M97
22	MCP Standard Decoupling	M97
23	MCP Graphics Support	M97
24	SB Misc	M97
25	FSB/DDR3 Vref Margining	BEN
26	DDR3 Support	T18_MLB
27	DDR3 DRAM Channel A (0-31)	(MASTER)
28	DDR3 DRAM Channel A (32-63)	(MASTER)
29	DDR3 DRAM Channel B (0-31)	(MASTER)
30	DDR3 DRAM Channel B (32-63)	(MASTER)
31	DDR BYPASSING 1	MEMORY
32	DDR BYPASSING 2	MEMORY
33	Memory Active Termination	M70
34	Wireless M93 Connector	M70
35	Hatch and Audio Connectors	(MASTER)
36	SATA Connectors	CHANGZHANG
37	USB EXTERNAL CONNECTORS	M70
38	IPD Connector	M70
39	SMC	M97
40	SMC SUPPORT	M70
41	LPC+SPI Debug Connector	CHANGZHANG

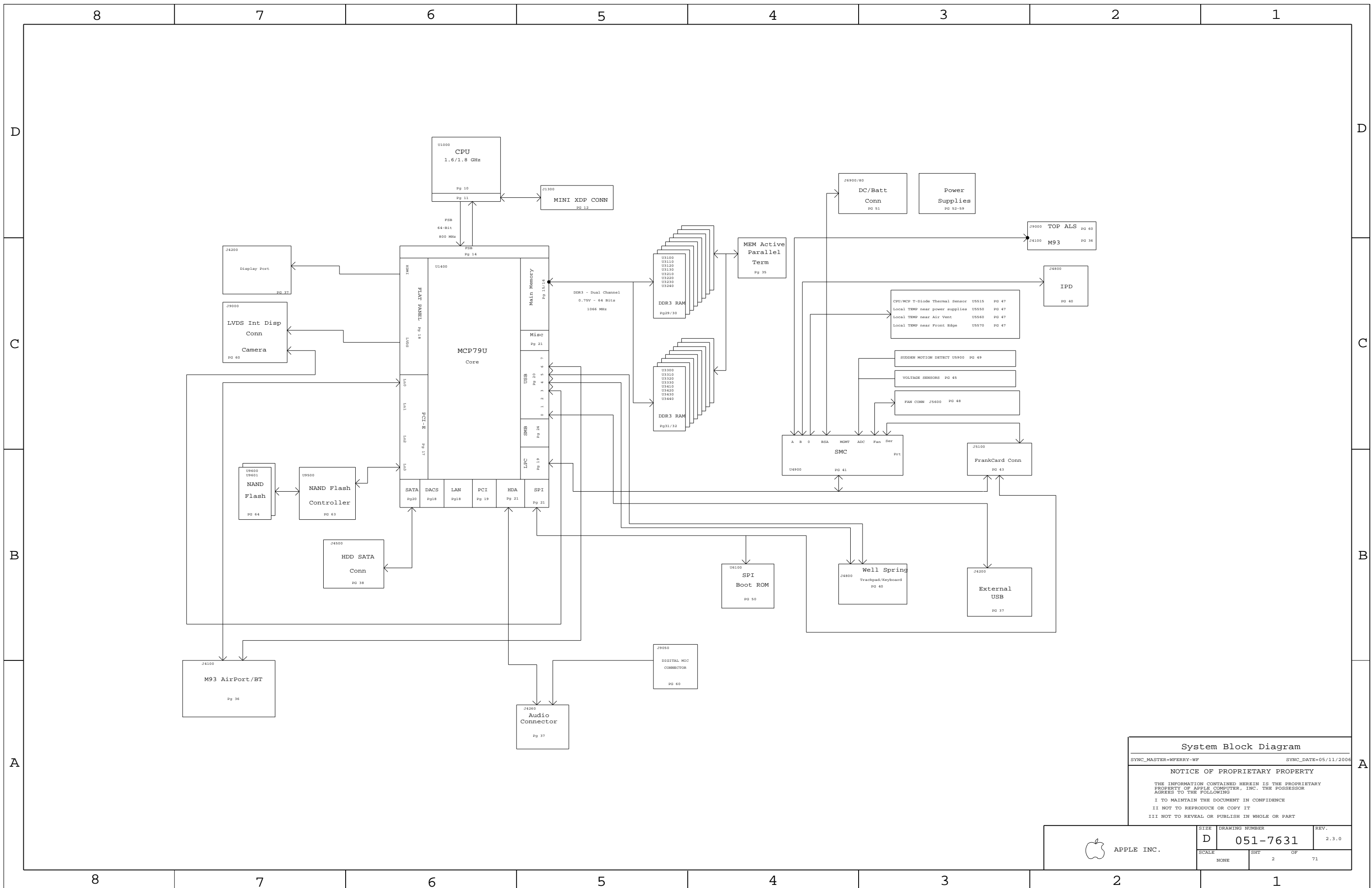
Page	Contents	Sync
42	M97 SMBUS CONNECTIONS	BEN
43	Voltage Sensors	M70
44	Current Sensing	YUNNU
45	TEMPERATURE SENSORS	M70
46	Fan	M70
47	Sudden Motion Sensor (SMS)	M76_MLB
48	SPI ROM	CHANGZHANG
49	DC-In & Battery Connectors	M70
50	IMVP6 CPU VCore Regulator	POWER
51	MCP CORE REGULATOR	MINGJING
52	1.8V LDO Supply	
53	1V05 S5 Power Supply	RXU_K20
54	1.5V/0.75V Supplies	M70
55	5V / 3.3V Power Supply	RXU_K20
56	POWER SEQUENCING	YUAN.MA
57	POWER FETS	YUAN.MA
58	PBUS Supply/Battery Charger	M70
59	LVDS,Camera Conn. and ALS Conn.	GPU
60	DISPLAYPORT SUPPORT	NMARTIN
61	DisplayPort Connector	M98_MLB
62	LED Backlight Driver	(MASTER)
63	LCD Backlight Support	M97
64	Additional CPU/GPU Decoupling	
65	CPU/FSB Constraints	M97
66	Memory Constraints	M97
67	MCP Constraints 1	M97
68	MCP Constraints 2	M97
69	SMC Constraints	M97
70	M96 Power and Ground Nets	(MASTER)
71	M96 RULE DEFINITIONS	M97

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7631	1	SCHEM, MLB, M96	SCH	CRITICAL	
820-2375	1	PCBF, MLB, M96	PCB	CRITICAL	

DRAWING  
TITLE=M96\_MLB  
ABBREV=DRAWING  
LAST\_MODIFIED=04 Aug 1 09:54:13 2008

<p style="text-align: center;">DIMENSIONS ARE IN MILLIMETERS</p> <p>XX : _____</p> <p>X.XX : _____</p> <p>X.XXX : _____</p> <p>ANGLES : _____</p> <p style="text-align: center;">DO NOT SCALE DRAWING</p> <p style="text-align: center;">           THIRD ANGLE PROJECTION       </p>	<b>METRIC</b>	 <b>APPLE INC.</b>												
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">DRAFTER</td> <td style="width: 50%;">DESIGN CK</td> </tr> <tr> <td>ENG APPD</td> <td>MFG APPD</td> </tr> <tr> <td>QA APPD</td> <td>DESIGNER</td> </tr> <tr> <td>RELEASE</td> <td>SCALE</td> </tr> <tr> <td colspan="2" style="text-align: center;">NONE</td> </tr> <tr> <td>MATERIAL/FINISH NOTED AS APPLICABLE</td> <td>SIZE D</td> </tr> </table>		DRAFTER	DESIGN CK	ENG APPD	MFG APPD	QA APPD	DESIGNER	RELEASE	SCALE	NONE		MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D	<p style="text-align: center;">NOTICE OF PROPRIETARY PROPERTY</p> <p style="font-size: 8px;">THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</p> <p style="font-size: 8px;">I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</p> <p style="text-align: center; font-weight: bold;">SCHEM, MLB, M96</p> <p style="font-size: 8px;">DRAWING NUMBER 051-7631 REV. 2.3.0</p> <p style="text-align: right; font-size: 8px;">SHT 1 OF 71</p>
DRAFTER	DESIGN CK													
ENG APPD	MFG APPD													
QA APPD	DESIGNER													
RELEASE	SCALE													
NONE														
MATERIAL/FINISH NOTED AS APPLICABLE	SIZE D													



**System Block Diagram**

SYNC\_MASTER=WFERRY-WF SYNC\_DATE=05/11/2006

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	2		



BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9734	PCBA,MLB,1.6GHZ,HY 2GB,SS CAP,M96	EEE_4DA,M96_COMMON,M96_HYNIX,M96_SS_CAP,CPU_1_6GHZ
630-9735	PCBA,MLB,1.6GHZ,HY 2GB,MU CAP,M96	EEE_4DB,M96_COMMON,M96_HYNIX,M96_MU_CAP,CPU_1_6GHZ
630-9514	PCBA,MLB,1.6GHZ,HY 2GB,TY CAP,M96	EEE_2AL,M96_COMMON,M96_HYNIX,M96_TY_CAP,CPU_1_6GHZ
630-9738	PCBA,MLB,1.8GHZ,HY 2GB,SS CAP,M96	EEE_4DC,M96_COMMON,M96_HYNIX,M96_SS_CAP,CPU_1_8GHZ
630-9516	PCBA,MLB,1.8GHZ,HY 2GB,MU CAP,M96	EEE_2AN,M96_COMMON,M96_HYNIX,M96_MU_CAP,CPU_1_8GHZ
630-9517	PCBA,MLB,1.8GHZ,HY 2GB,TY CAP,M96	EEE_2AP,M96_COMMON,M96_HYNIX,M96_TY_CAP,CPU_1_8GHZ

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M96_COMMON	ALTERNATE,COMMON,M96_COMMON1,M96_COMMON2,M96_COMMON3
M96_COMMON1	MCP_B02,BOOTROM_DEVEL,SMC_PRGRM,BOOT_MODE_USER,UTAG_ALLDEV,MEMRESET_HW,MEMRESET_MCP,VREFMRGN
M96_COMMON2	LPCPLUS,XDP,XDP_CONN
M96_COMMON3	MCP_CS1_NO
M96_HYNIX	DRAM_HYNIX
M96_MICRON	DRAM_MICRON,DRAM_SPD_2
M96_SS_CAP	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF
M96_MU_CAP	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF
M96_TY_CAP	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4DA]	CRITICAL	EEE_4DA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4DB]	CRITICAL	EEE_4DB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AL]	CRITICAL	EEE_2AL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:4DC]	CRITICAL	EEE_4DC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AN]	CRITICAL	EEE_2AN
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2AP]	CRITICAL	EEE_2AP

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3658	1	IC,PDC,QS,1.60GHZ,17M,1066,6M	U1000	CRITICAL	CPU_1_6GHZ
337S3659	1	IC,PDC,QS,1.80GHZ,17M,1066,6M	U1000	CRITICAL	CPU_1_8GHZ
338S0604	1	IC,GMCP,MCP79U-A01Q,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_A01Q
338S0601	1	IC,GMCP,MCP79U-B01,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_B01
338S0637	1	IC,GMCP,MCP79U-B02,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_B02
335S0615	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2382	1	IC,EPI,BOOTROM DEVELOPMENT (UNLOCKED),M96	U6100	CRITICAL	BOOTROM_DEVEL
341S2326	1	IC,EPI,BOOTROM FINAL (LOCKED),M96	U6100	CRITICAL	BOOTROM_FINAL
338S0563	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2327	1	IC,PRGRM,SMC (NEW),M96	U4900	CRITICAL	SMC_PRGRM
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_HYNIX
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_MICRON
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	

Alternate Parts


PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0067	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	
152S0684	152S0421	ALL	1.0UH,22A,10MOHM	
376S0627	376S0723	ALL	POWER NFET, 30V, 18A	
152S0905	152S0861	ALL	IND,1HLP4040CZ,0.68uH,18A	

CONFIGURATION OPTIONS

SYNC\_MASTER=(N/A) SYNC\_DATE=(N/A)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	4		



# Functional Test Points

**NB NO\_TESTS**  
 These are normally testpoints but become NC  
 NO\_TEST

**FUNC TEST - BATTERY CONNECTOR**

x2	E640	TRUE	BATT_POS	49
x2	E640	TRUE	GND	
E640	TRUE	SMC_BS_ALRT_L	39 40 49	
E640	TRUE	SMBUS_SMC_BSA_SCL	42 69	
E640	TRUE	SMBUS_SMC_BSA_SDA	42 69	

**FUNC TEST - DC-IN CONNECTOR**

x6	E640	TRUE	PP18V5_DCIN	49 70
E640	TRUE	ADAPTER_SENSE	49	
x6	E700	TRUE	GND	

**FUNC TEST - FAN CONNECTOR**

E640	TRUE	=PP5V_S0_FAN	7 46
E640	TRUE	FAN_RT_PWM	46
E640	TRUE	FAN_RT_TACH	46
E700	TRUE	GND	

**FUNC TEST - AIRPORT**

E640	TRUE	CK505_SRC_CLKREQ6_L	6
E640	TRUE	PCIE_WAKE_L	6 16 34
E640	TRUE	AIRPORT_RST_L	6 24 34
E640	TRUE	=SMB_AIRPORT_CLK	6 34 42
E640	TRUE	=SMB_AIRPORT_DATA	6 34 42
E700	TRUE	GND	

**FUNC TEST - MIC**

E640	TRUE	PP3V3_S0_MIC_F	59 70
E640	TRUE	AUD_MIC_DATA_F	59
E640	TRUE	AUD_MIC_CLK_F	59
E700	TRUE	GND_MIC_F	59

**FUNC TEST - AUDIO CONNECTOR**

E640	TRUE	HDA_SYNC	20 35 68
E640	TRUE	HDA_BIT_CLK	20 35 68
E640	TRUE	AUD_MIC_DATA	35 59
E640	TRUE	HDA_SDOUT	20 35 68
E640	TRUE	=PPVIN_S0_AUDIO	7 35
E640	TRUE	HDA_SDIN0	20 35 68
E640	TRUE	AUD_MIC_CLK	35 59
E640	TRUE	PM_SLP_S3_L	20 34 35 39 56

**FUNC TEST - IPD CONNECTOR**

E640	TRUE	SMC_LID	38 39 40
E640	TRUE	PP3V42_G3H_IPD_F	38 70
E640	TRUE	SMC_SYS_KBDLED	38 39
E640	TRUE	SMC_SYS_LED	38 39
E640	TRUE	=USB2_TPAD_N	8 38
E640	TRUE	=USB2_TPAD_P	8 38
E640	TRUE	SMC_ONOFF_L	6 38 39 40
E640	TRUE	=USB2_IR_N	6 8 38
E640	TRUE	=USB2_IR_P	6 8 38
E640	TRUE	PP5V_S0_KBDLED_F	6 38 70
E640	TRUE	PP5V_S3_TOPCASE_F	38 70
E640	TRUE	=I2C_TPAD_SCL	38 42
E640	TRUE	=I2C_TPAD_SDA	38 42
E640	TRUE	SMC_ONOFF_L	6 38 39 40
E640	TRUE	=USB2_IR_N	6 8 38
E640	TRUE	=USB2_IR_P	6 8 38
E640	TRUE	PP5V_S0_KBDLED_F	6 38 70
E640	TRUE	LSOC_PRESS_H_R	38

**FUNC TEST - M93 WIRELESS CONNECTOR**

E640	TRUE	AIRPORT_RST_L	6 24 34
E640	TRUE	PCIE_WAKE_L	6 16 34
E640	TRUE	CK505_SRC_CLKREQ6_L	6
E640	TRUE	PCIE_CLK100M_MINI_N_F	6 34
E640	TRUE	PCIE_CLK100M_MINI_P_F	34
E640	TRUE	PCIE_E_D2R_N_F	34
E640	TRUE	PCIE_E_D2R_P_F	34
E640	TRUE	PP5V_S0	6 34
E640	TRUE	PCIE_E_R2D_C_N_F	6 34
E640	TRUE	PCIE_E_R2D_C_P_F	6 34
E640	TRUE	AIRPORT_RST_L	6 24 34
E640	TRUE	=SMB_AIRPORT_DATA	6 34 42
E640	TRUE	=SMB_AIRPORT_CLK	6 34 42
E640	TRUE	PCIE_E_R2D_C_N_F	6 34
E640	TRUE	PCIE_E_R2D_C_P_F	6 34
E640	TRUE	PP3V3_S3_AP_AUX	34 70

**FUNC TEST - Power Supplies**

E640	TRUE	PPVCORE_S0_CPU	7 70
E640	TRUE	PP0V75_S0	7 70
E640	TRUE	PP1V05_S0	7 70
E640	TRUE	PP1V5_S0	7 70
E640	TRUE	PP1V5_S3	7 70
E640	TRUE	PP1V05_S5	7 70
E640	TRUE	PPMPCORE_S0	7 70
E640	TRUE	PP5V_S0	7 70
E640	TRUE	PP3V3_S0	7 70
E640	TRUE	PP3V3_S3	7 70
E640	TRUE	PP5V_S3	7 70
E640	TRUE	PP3V3_S5	7 70
E640	TRUE	PP3V42_G3H	7 70
E640	TRUE	PP18V5_G3H	7 70
E640	TRUE	PPDCIN_G3H	7 70
E640	TRUE	PPBUS_G3H	7 70
E640	TRUE	PPBUS_R_G3H	7 70
E640	TRUE	PP1V8_S0	7 70

**FUNC TEST - SATA HDD**

E640	TRUE	PP3V3_S0_HDD_F	36 70
E640	TRUE	SATA_HDD_R2D_N	36 67
E640	TRUE	SATA_HDD_R2D_P	36 67
E640	TRUE	SATA_HDD_D2R_C_N	36 67
E640	TRUE	SATA_HDD_D2R_C_P	36 67
E700	TRUE	GND	

**FUNC TEST - RIO HATCH CONNECTOR**

E640	TRUE	DP_ML_C_N<3..0>	61 67
E640	TRUE	DP_ML_C_P<3..0>	61 67
E640	TRUE	DP_AUX_CH_C_N	35 60 61 67
E640	TRUE	DP_AUX_CH_C_P	35 60 61 67
E640	TRUE	DP_CA_DET_Q	35 61
E640	TRUE	HDMI_CEC	35 61
E640	TRUE	DP_HPD_Q	35 61
E640	TRUE	PP3V3_S0_DPPWR	35 61 70
E640	TRUE	USB2_EXTA_F_P	35 37
E640	TRUE	USB2_EXTA_F_N	35 37
E640	TRUE	PP5V_S3_USB2_EXTA_F	35 37 70
E640	TRUE	GND	

x1 E700 TRUE GND

**Power Supply NO\_TESTS**  
 NO\_TEST

**CLOCK NO\_TESTS**  
 NO\_TEST

**LVDS NO\_TESTS**  
 NO\_TEST

**REQUIRED NETS**

**NICE2HAVE NETS**

**FUNC TEST - XDP/ITP CONNECTOR**

E640	TRUE	XDP_BPM_L<0..5>	85 12
E640	TRUE	TP_XDP_OBSFN_B0	12
E640	TRUE	TP_XDP_OBSFN_B1	12
E640	TRUE	TP_XDP_OBSFN_B0	12
E640	TRUE	TP_XDP_OBSFN_B1	12
E640	TRUE	TP_XDP_OBSFN_B2	12
E640	TRUE	TP_XDP_OBSFN_B3	12
E640	TRUE	XDP_PWRGD	12
E640	TRUE	XDP_OBS20	12
E640	TRUE	SMBUS_MCP_0_DATA	12 20 42 68
E640	TRUE	SMBUS_MCP_0_CLK	12 20 42 68
E640	TRUE	XDP_TCK	85 12
E640	TRUE	JTAG_MCP_TDO_CONN	85 12
E640	TRUE	JTAG_MCP_TRST_L	12 20
E640	TRUE	MCP_DEBUG<7..0>	12 18 68
E640	TRUE	JTAG_MCP_TDI	12 20
E640	TRUE	JTAG_MCP_TMS	12 20
E640	TRUE	FSB_CLK_ITP_P	12 13 65
E640	TRUE	FSB_CLK_ITP_N	12 13 65
E640	TRUE	XDP_CPURST_L	85 12
E640	TRUE	XDP_DBRESET_L	85 12
E640	TRUE	XDP_TDO_CONN	12
E640	TRUE	XDP_TRST_L	85 12
E640	TRUE	XDP_TDI	85 12
E640	TRUE	XDP_TMS	85 12
E640	TRUE	=PP3V3_S0_XDP	7 12
E640	TRUE	=PP1V05_S0_CPU	7 11 12

**FUNC TEST - CAMERA USB, LVDS, ALS**

x2 E640	TRUE	PP5V_S3_CAMERA_F	59 70
E640	TRUE	USB2_CAMERA_F_P	59
E640	TRUE	USB2_CAMERA_F_N	59
E640	TRUE	LCDBKLT_RTIN<1..6>	59 62
E640	TRUE	LVDS_IG_A_DATA_N<0..2>	17 59 67
E640	TRUE	LVDS_IG_A_DATA_P<0..2>	17 59 67
E640	TRUE	PPVOUT_S0_LCDBKLT	59 62 70
E640	TRUE	LVDS_IG_A_CLK_F_N	59 67
E640	TRUE	LVDS_IG_A_CLK_F_P	59 67
E640	TRUE	LVDS_IG_DDC_CLK	17 59
E640	TRUE	LVDS_IG_DDC_DATA	17 59
E640	TRUE	PP3V3_S0_LCD_F	59 70
x2 E640	TRUE	PP3V3_LCDVDD_SW_F	59 70
E640	TRUE	=I2C_ALS_SDA	42 59
E640	TRUE	=I2C_ALS_SCL	42 59
x1 E640	TRUE	GND	

**Functional Test and No-Tests**

**NOTICE OF PROPRIETARY PROPERTY**

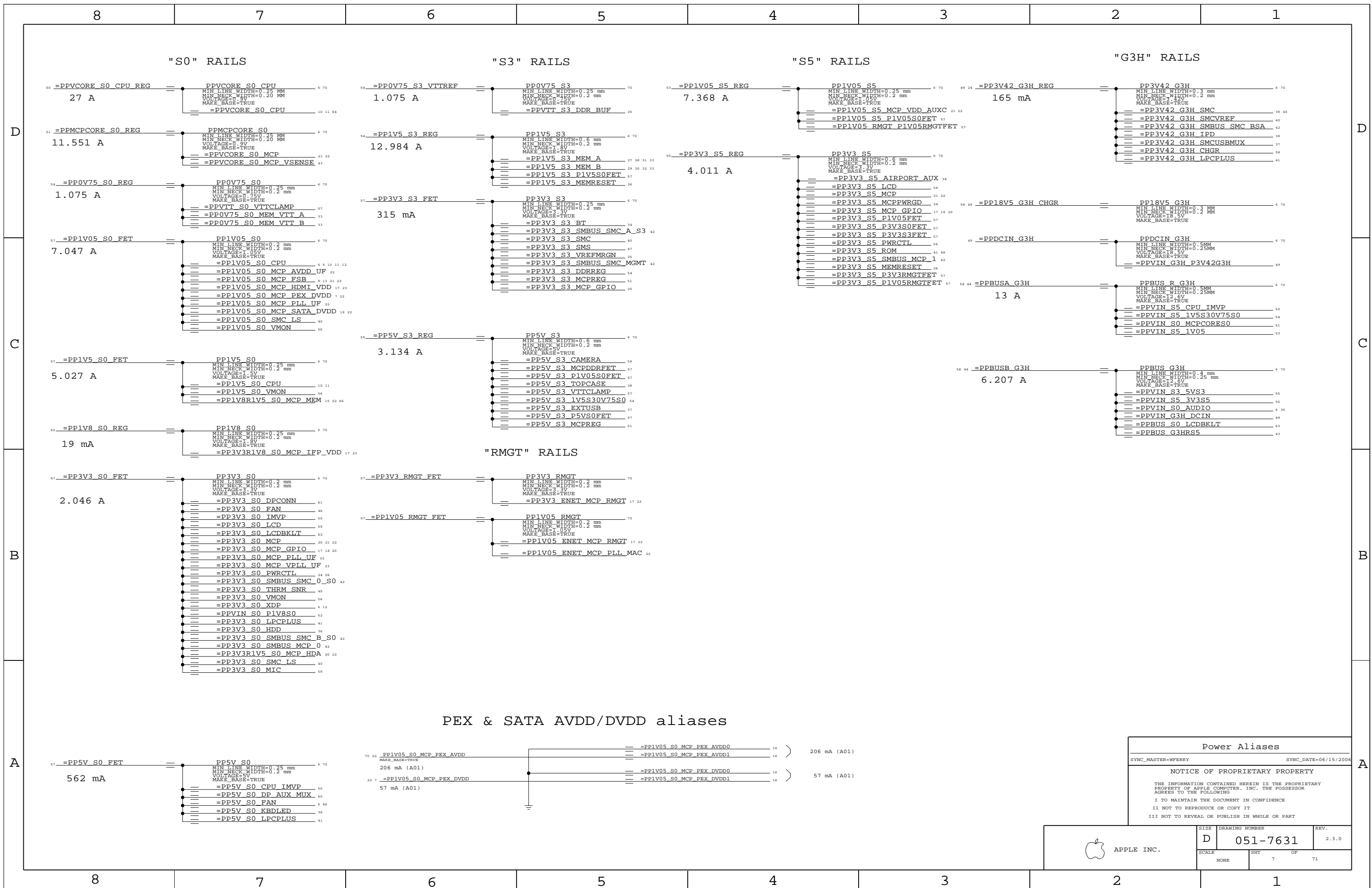
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

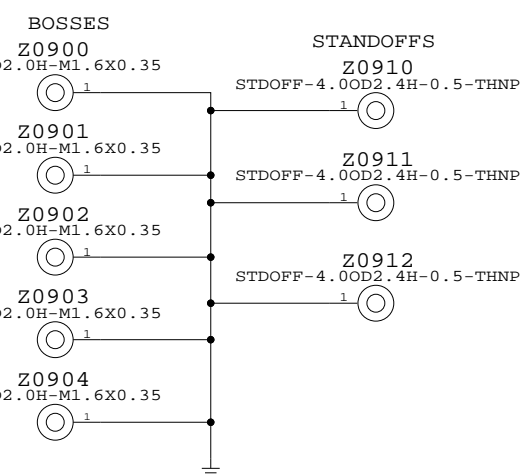
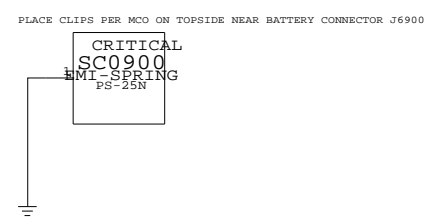
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	6		



Power Aliases			
SYNC_MASTER=WFERRY	SYNC_DATE=06/15/2006		
<b>NOTICE OF PROPRIETARY PROPERTY</b>			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING			
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	7		

### EMI SPRING CLIPS



### SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

SMC	NC SMC	NO_TEST
SMC PA0	NC SMC PA0	TRUE
SMC PA1	NC SMC PA1	MAKE_BASE=TRUE
ESTARLDO EN	NC ESTARLDO EN	TRUE
SMC P26	NC SMC P26	MAKE_BASE=TRUE
SMC P41	NC SMC P41	TRUE
SMC BIL BUTTON L	NC SMC P67	MAKE_BASE=TRUE
SMC GFX OVERTEMP L	NC SMC GFX OVERTEMP L	TRUE
SMC EXCARD OC L	NC EXCARD OC L	TRUE
SMC P24	NC SMC P24	TRUE
SMC EXCARD CP	NC SMC EXCARD CP	MAKE_BASE=TRUE
ALS RIGHT	NC ALS RIGHT	TRUE
ALS GAIN	NC ALS GAIN	MAKE_BASE=TRUE
SMC FAN 1 CTL	NC SMC FAN 1 CTL	MAKE_BASE=TRUE
SMC FAN 2 CTL	NC SMC FAN 2 CTL	TRUE
SMC FAN 3 CTL	NC SMC FAN 3 CTL	MAKE_BASE=TRUE
SMC FAN 1 TACH	NC SMC FAN 1 TACH	TRUE
SMC FAN 2 TACH	NC SMC FAN 2 TACH	MAKE_BASE=TRUE
SMC FAN 3 TACH	NC SMC FAN 3 TACH	TRUE
SMC EXCARD PWR EN	NC SMC RSTGATE L	MAKE_BASE=TRUE
ISENSE_CAL_EN	NC ISENSE_CAL_EN	TRUE
SMC FWE	NC SMC FWE	MAKE_BASE=TRUE
SMC ANALOG ID	NC SMC ANALOG ID	TRUE
ALS LEFT	NC ALS LEFT	MAKE_BASE=TRUE
SMC NB DDR ISENSE	NC SMC NB DDR ISENSE	TRUE
SMC P10	NC SMC P10	MAKE_BASE=TRUE
SMC PA5	NC SMC PA5	MAKE_BASE=TRUE
SMC GPU ISENSE	NC SMC GPU ISENSE	MAKE_BASE=TRUE

### PCI-E ALIASES

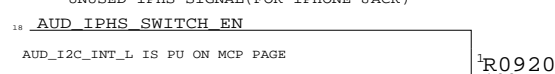
UNUSED GPU LANES

=PEG D2R N<15:0>	NC PEG D2R N<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
=PEG D2R P<15:0>	NC PEG D2R P<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
=PEG R2D C N<15:0>	NC PEG R2D C N<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
=PEG R2D C P<15:0>	NC PEG R2D C P<15:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
PEG PRSNT L	TP PEG PRSNT L	MAKE_BASE=TRUE	
PEG CLKR0 L	TP PEG CLKR0 L	MAKE_BASE=TRUE	
PEG CLK100M P	TP PEG CLK100M P	MAKE_BASE=TRUE	
PEG CLK100M N	TP PEG CLK100M N	MAKE_BASE=TRUE	
EXTGPU PWR EN	TP EXTGPU PWR EN	MAKE_BASE=TRUE	
EXTGPU RESET L	TP EXTGPU RESET L	MAKE_BASE=TRUE	

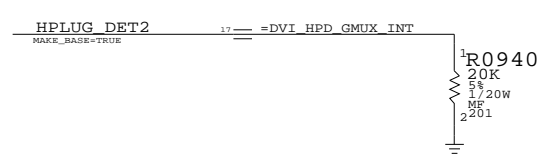
### AIRPORT CARD AND TURBOMEM PRESENT SIGNAL



### HDA PULL-DOWN

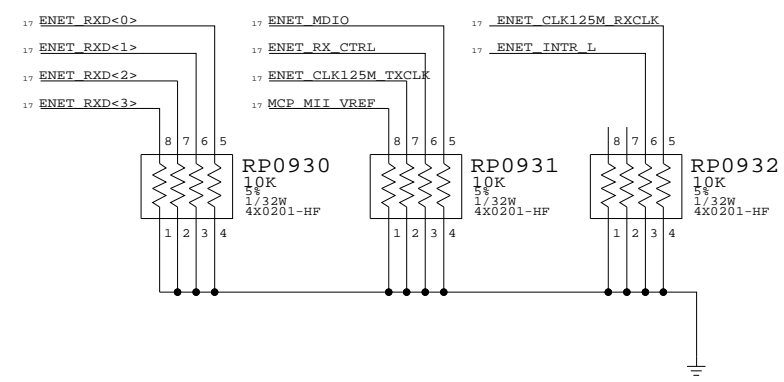


### DP HOTPLUG PULL-DOWN



### LAN ALIASES

UNUSED ETHERNET RG/MII INTERFACE



ENET RESET L	NC ENET RESET L	MAKE_BASE=TRUE
MCP_CLK25M_BUF0 R	NC MCP_CLK25M_BUF0 R	MAKE_BASE=TRUE
ENET_PWRDWN L	NC ENET_PWRDWN L	MAKE_BASE=TRUE
ENET_MDC	NC ENET_MDC	MAKE_BASE=TRUE
ENET_TX_CTRL	NC ENEX_TX_CTRL	MAKE_BASE=TRUE
ENET_TXD<3..0>	NC ENET_TXD<3..0>	MAKE_BASE=TRUE

### DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

MCP_TV_DAC_RSET	NC MCP_TV_DAC_RSET	NO_TEST=TRUE	MAKE_BASE=TRUE
MCP_TV_DAC_VREF	NC MCP_TV_DAC_VREF	NO_TEST=TRUE	MAKE_BASE=TRUE
MCP_CLK27M_XTALIN	NC MCP_CLK27M_XTALIN	NO_TEST=TRUE	MAKE_BASE=TRUE
MCP_CLK27M_XTALOUT	NC MCP_CLK27M_XTALOUT	NO_TEST=TRUE	MAKE_BASE=TRUE
CRT_IG_R_C_PR	NC CRT_IG_R_C_PR	NO_TEST=TRUE	MAKE_BASE=TRUE
CRT_IG_G_Y_Y	NC CRT_IG_G_Y_Y	NO_TEST=TRUE	MAKE_BASE=TRUE
CRT_IG_B_COMP_PB	NC CRT_IG_B_COMP_PB	NO_TEST=TRUE	MAKE_BASE=TRUE
CRT_IG_HSYNC	NC CRT_IG_HSYNC	NO_TEST=TRUE	MAKE_BASE=TRUE
CRT_IG_VSYNC	NC CRT_IG_VSYNC	NO_TEST=TRUE	MAKE_BASE=TRUE

### LVDS ALIASES

UNUSED LVDS SIGNALS

LVDS_IG_A_DATA_P<3>	NC LVDS_IG_A_DATA_P3	NO_TEST=TRUE	MAKE_BASE=TRUE
LVDS_IG_A_DATA_N<3>	NC LVDS_IG_A_DATA_N3	NO_TEST=TRUE	MAKE_BASE=TRUE
LVDS_IG_B_CLK_P	NC LVDS_IG_B_CLK_P	NO_TEST=TRUE	MAKE_BASE=TRUE
LVDS_IG_B_CLK_N	NC LVDS_IG_B_CLK_N	NO_TEST=TRUE	MAKE_BASE=TRUE
LVDS_IG_B_DATA_P<3:0>	NC LVDS_IG_B_DATA_P<3:0>	NO_TEST=TRUE	MAKE_BASE=TRUE
LVDS_IG_B_DATA_N<3:0>	NC LVDS_IG_B_DATA_N<3:0>	NO_TEST=TRUE	MAKE_BASE=TRUE

### MISC NC MCP79 ALIASES

CPU_PECI_MCP	TP CPU_PECI_MCP	MAKE_BASE=TRUE
FW_PME_L	TP FW_PME_L	MAKE_BASE=TRUE
ODD_PWR_EN_L	TP ODD_PWR_EN_L	MAKE_BASE=TRUE

### SATA ALIASES

UNUSED SATA ODD SIGNALS

SATA_ODD_R2D_C_P	TP SATA_ODD_R2D_C_P	MAKE_BASE=TRUE
SATA_ODD_R2D_C_N	TP SATA_ODD_R2D_C_N	MAKE_BASE=TRUE
SATA_ODD_D2R_P	TP SATA_ODD_D2R_P	MAKE_BASE=TRUE
SATA_ODD_D2R_N	TP SATA_ODD_D2R_N	MAKE_BASE=TRUE

### USB ALIASES

UNUSED USB PORTS

USB_EXTB_P	TP USB_EXTB_P	MAKE_BASE=TRUE
USB_EXTB_N	TP USB_EXTB_N	MAKE_BASE=TRUE
USB_EXTC_P	TP USB_EXTC_P	MAKE_BASE=TRUE
USB_EXTC_N	TP USB_EXTC_N	MAKE_BASE=TRUE
USB_EXTD_P	TP USB_EXTD_P	MAKE_BASE=TRUE
USB_EXTD_N	TP USB_EXTD_N	MAKE_BASE=TRUE
USB_EXCARD_P	TP USB_EXCARD_P	MAKE_BASE=TRUE
USB_EXCARD_N	TP USB_EXCARD_N	MAKE_BASE=TRUE
USB_MINI_P	TP USB_MINI_P	MAKE_BASE=TRUE
USB_MINI_N	TP USB_MINI_N	MAKE_BASE=TRUE

### EXTERNAL PORT A

=USB2_EXTA_P	USB_EXTA_P	19 68
=USB2_EXTA_N	USB_EXTA_N	19 68
=EXTAUSB_OC_L	USB_EXTA_OC_L	19

### CAMERA

=USB2_CAMERA_P	USB_CAMERA_P	19 68
=USB2_CAMERA_N	USB_CAMERA_N	19 68

### TRACKPAD (WELLSRING)

=USB2_TPAD_P	USB_TPAD_P	19 68
=USB2_TPAD_N	USB_TPAD_N	19 68

### IR

=USB2_IR_P	USB_IR_P	19 68
=USB2_IR_N	USB_IR_N	19 68

### BT (M93)

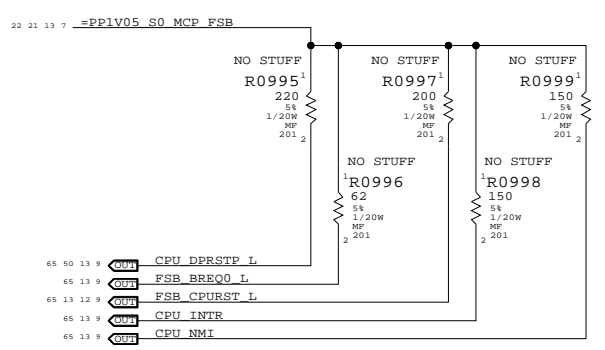
=USB2_BT_P	USB_BT_P	19 68
=USB2_BT_N	USB_BT_N	19 68

### CPU FSB FREQUENCY STRAPS

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	333
0 1 0	(156)
0 1 1	333
1 0 0	400
1 0 1	(400)
1 1 0	(400)
1 1 1	(RSVD)

### Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA. If found to be necessary, will move to page14.csa



### MEM ALIASES

TP_MEM_A_CLK4P	NC MEM_A_CLK4P	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CLK4N	NC MEM_A_CLK4N	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CLK3P	NC MEM_A_CLK3P	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CLK3N	NC MEM_A_CLK3N	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CS_L<2>	NC MEM_A_CS_L<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CS_L<3>	NC MEM_A_CS_L<3>	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CKE<2>	NC MEM_A_CKE<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_A_CKE<3>	NC MEM_A_CKE<3>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CLK4P	NC MEM_B_CLK4P	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CLK4N	NC MEM_B_CLK4N	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CLK3P	NC MEM_B_CLK3P	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CLK3N	NC MEM_B_CLK3N	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CS_L<2>	NC MEM_B_CS_L<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CS_L<3>	NC MEM_B_CS_L<3>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_ODT<2>	NC MEM_B_ODT<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_ODT<3>	NC MEM_B_ODT<3>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CKE<2>	NC MEM_B_CKE<2>	TRUE	MAKE_BASE=TRUE
TP_MEM_B_CKE<3>	NC MEM_B_CKE<3>	TRUE	MAKE_BASE=TRUE

### SIGNAL ALIAS /RESET

SYNC\_MASTER=(MASTER) SYNC\_DATA=(MASTER)

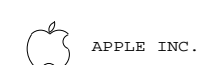
### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



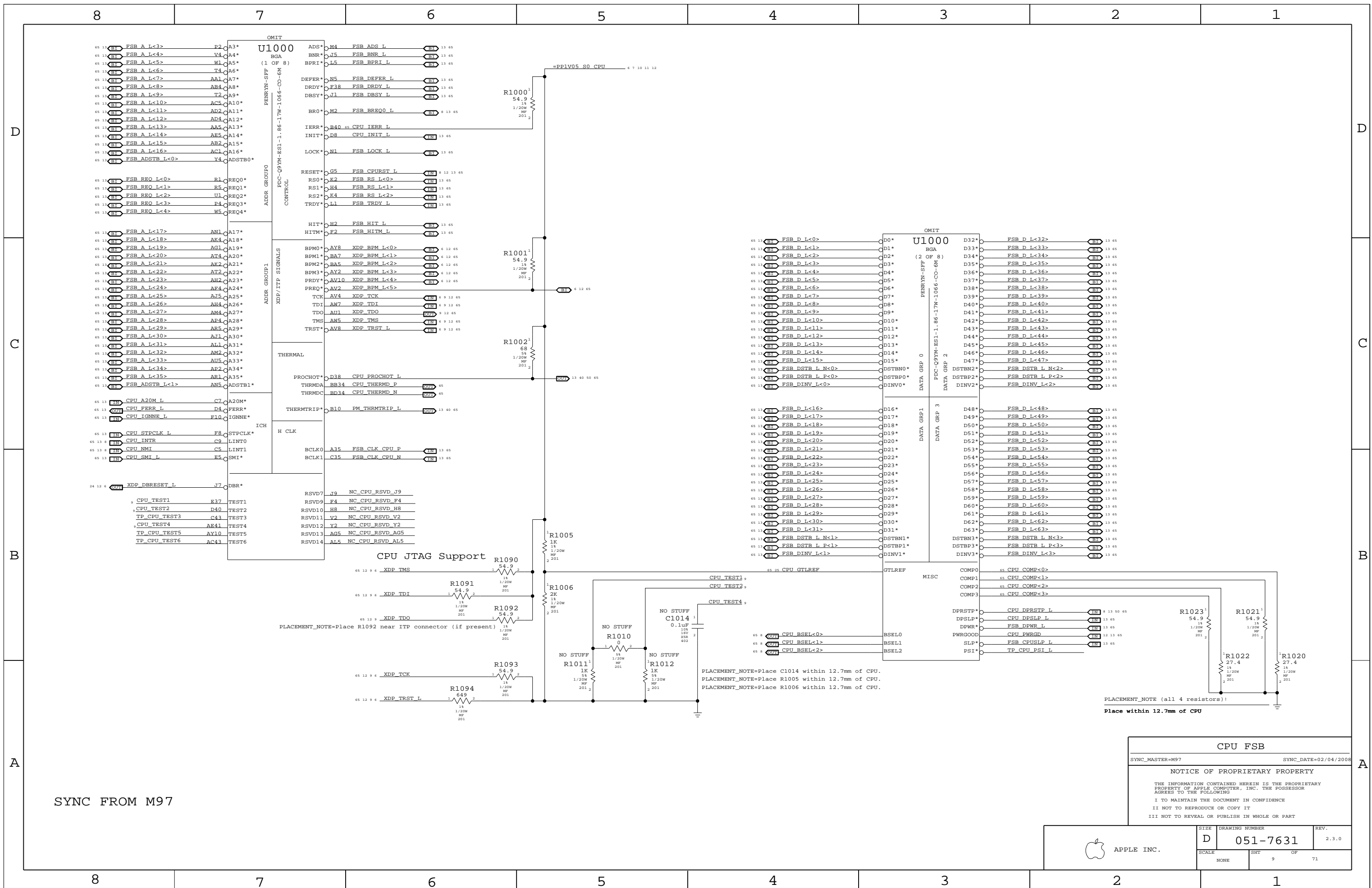
SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	8	71

SMC_IG_THROTTLE_L	SMC_GFX_THROTTLE_L	39
_SMC_SMS_INT_L	_SMC_SMS_INT	39
_SMC_ADAPTER_EN	_SMC_ADAPTER_PRESENT	34

GND

VOLTAGE=0V  
MIN\_NECK\_WIDTH=0.20 MM  
MIN\_LINE\_WIDTH=0.30 MM

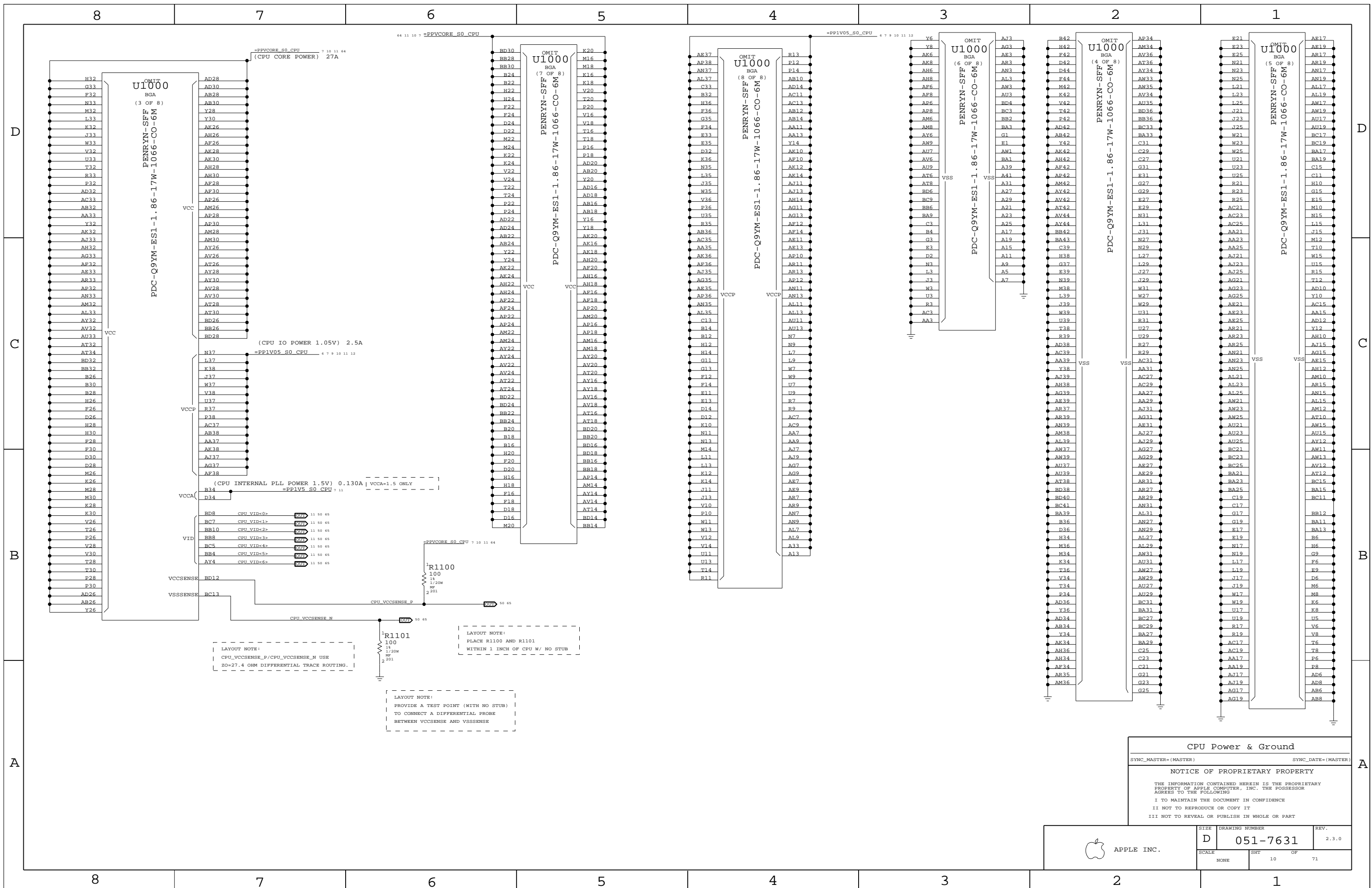




SYNC FROM M97

**CPU FSB**  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		9	71



**CPU Power & Ground**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	10		

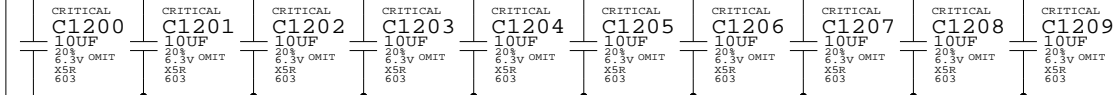
# CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

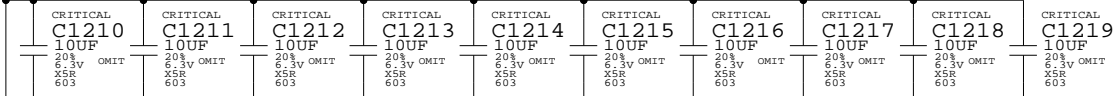
64 10 7 =PPVCORE\_S0\_CPU

10UF 0603 = APN:138S0568 = MURATA, TAIYO, TDK, SAMSUNG

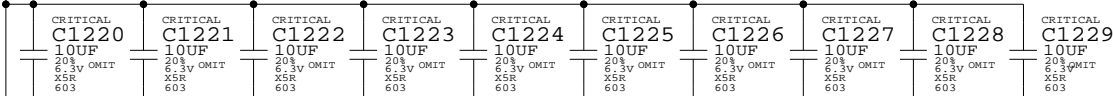
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



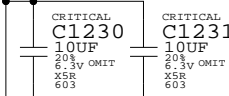
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



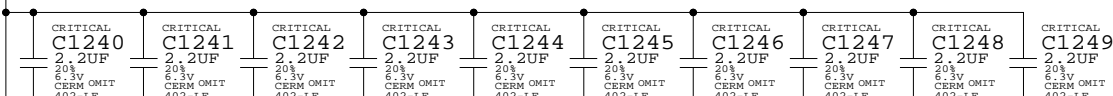
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



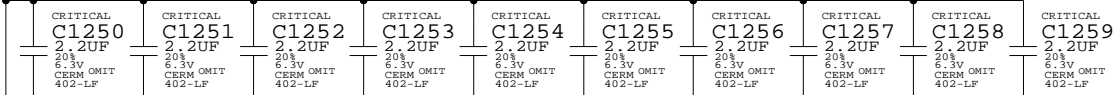
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



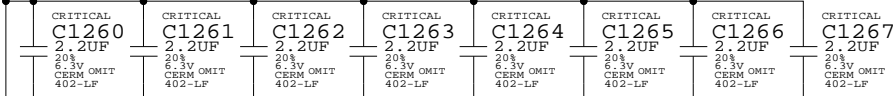
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



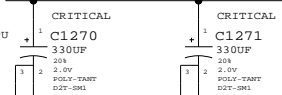
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



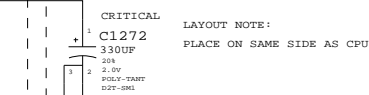
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:  
PLACE ON SAME SIDE AS CPU



LAYOUT NOTE:  
PLACE ON SAME SIDE AS CPU



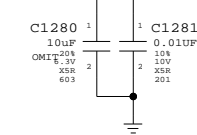
Intel recommends 3x220UF @ 9mOHM

## CPU VCORE VID CONNECTIONS

65 50 10 CPU VID<0..6> MAKE\_BASE=TRUE IMVP6 VID<0..6>

## VCCA (CPU AVdd) DECOUPLING

10 7 =PP1V5\_S0\_CPU 1x 10uF, 1x 0.01uF

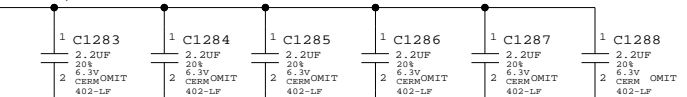


LAYOUT NOTE:  
PLACE C1281 NEAR PIN B34 OF U1000

## VCCP (CPU I/O) DECOUPLING

12 10 9 7 6 =PP1V05\_S0\_CPU

1x 330UF, 12x 2.2UF



LAYOUT NOTE:  
PLACE C1290 CLOSE TO CPU  
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS  
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

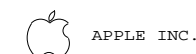
## CPU Decoupling & VID

SYNC\_MASTER=MSASBAR SYNC\_DATE=04/26/2006

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

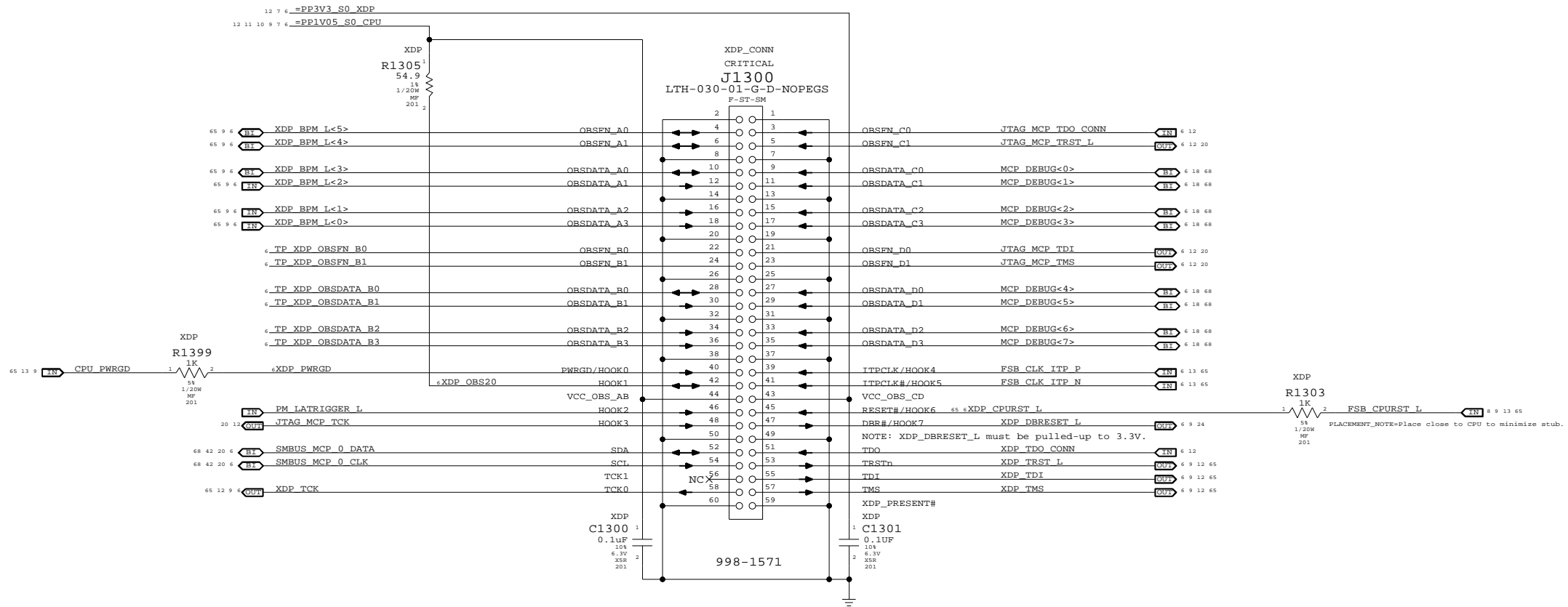
- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

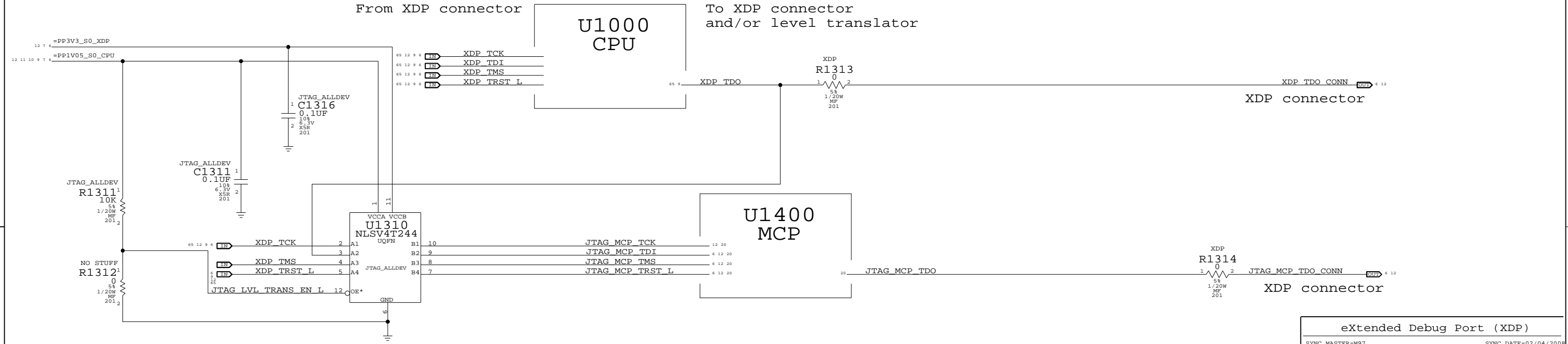
SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	11	71

MCP79-specific pinout



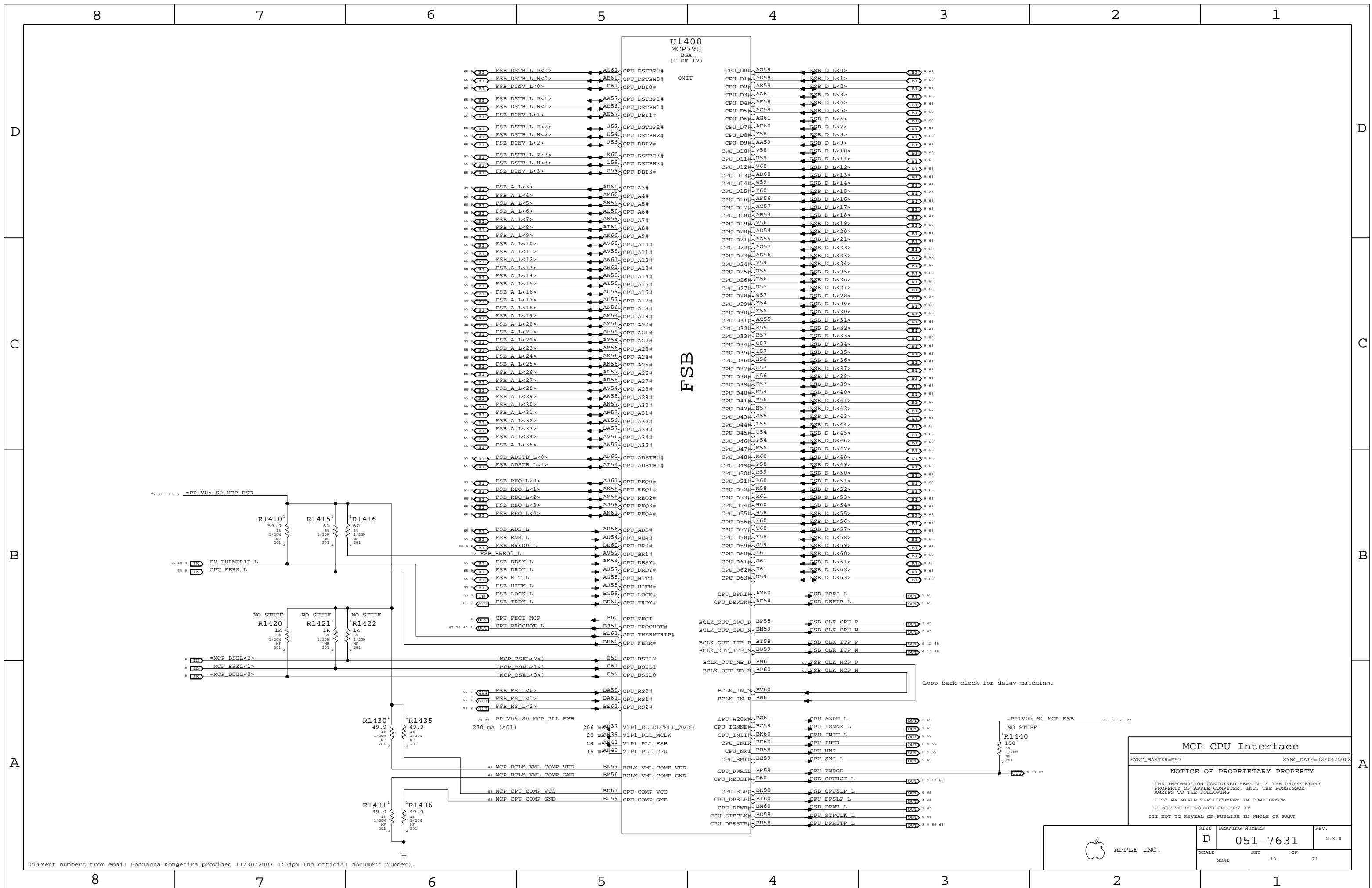
From XDP connector

To XDP connector and/or level translator



eXtended Debug Port (XDP)  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

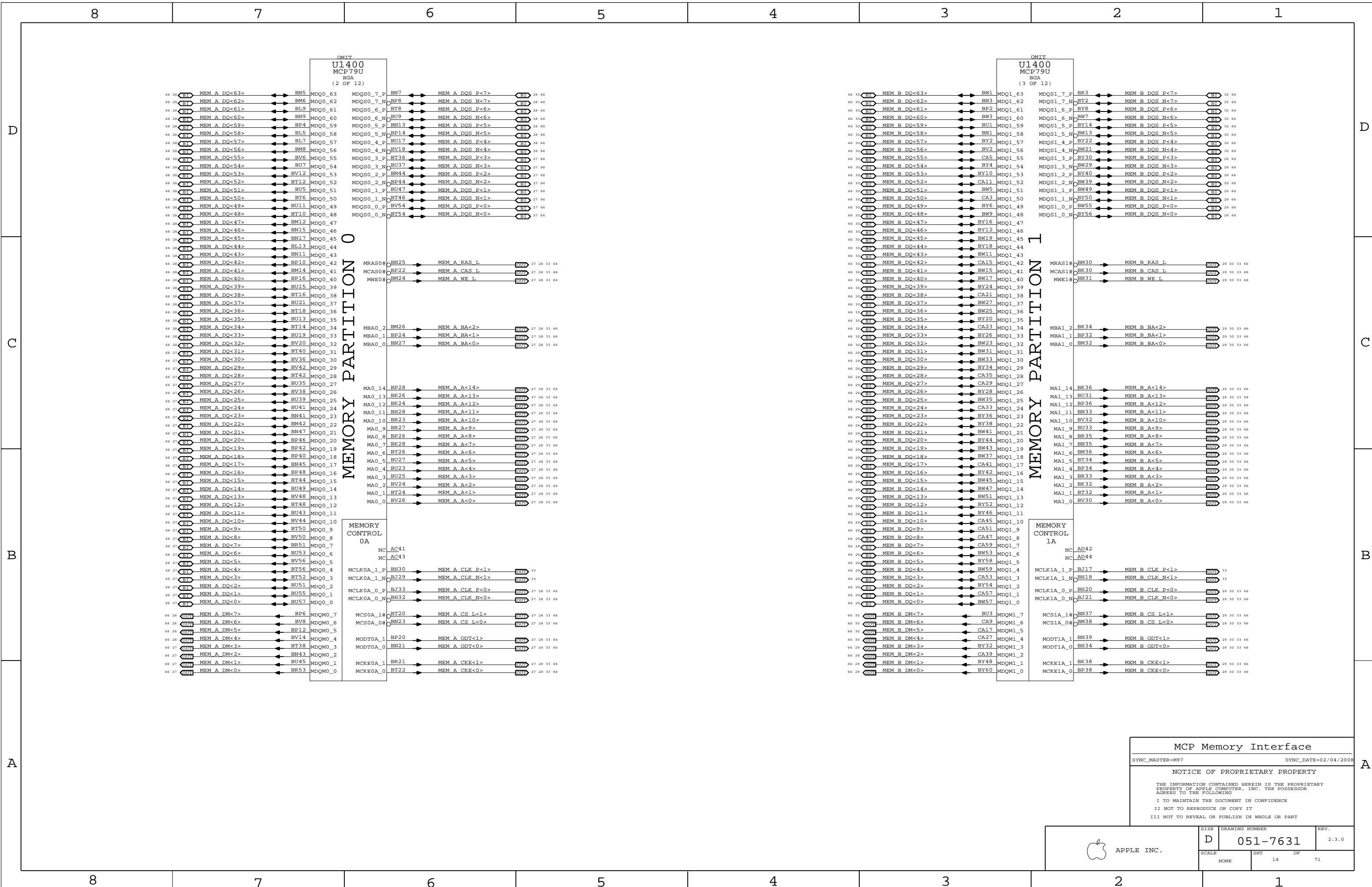
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT 12 OF 71		



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

**MCP CPU Interface**  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	13		



**MCP Memory Interface**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

---

**NOTICE OF PROPRIETARY PROPERTY**

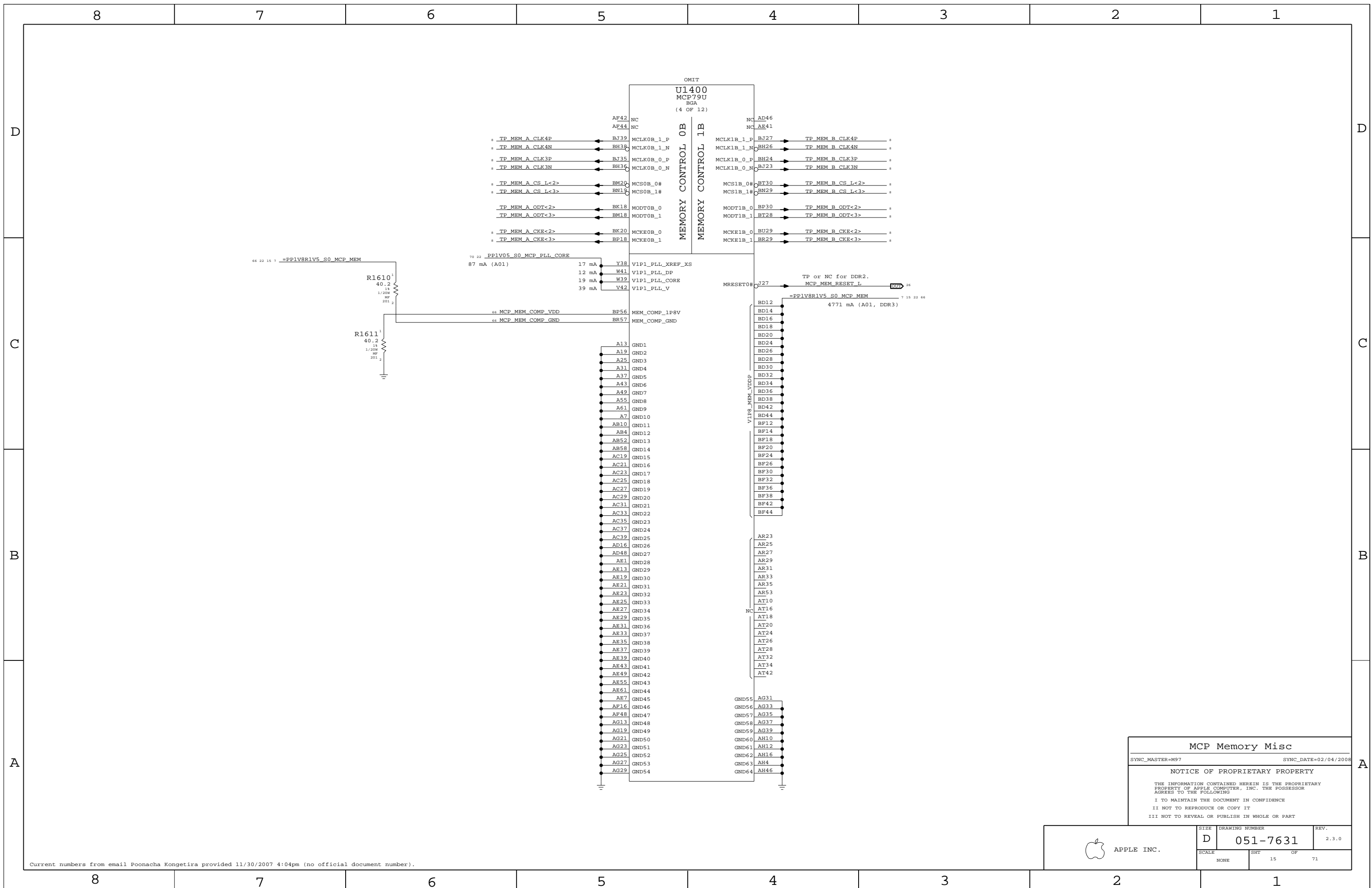
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7631</b>	REV. 2.3.0
	SCALE NONE	SHEET 14	OF 71



**MCP Memory Misc**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

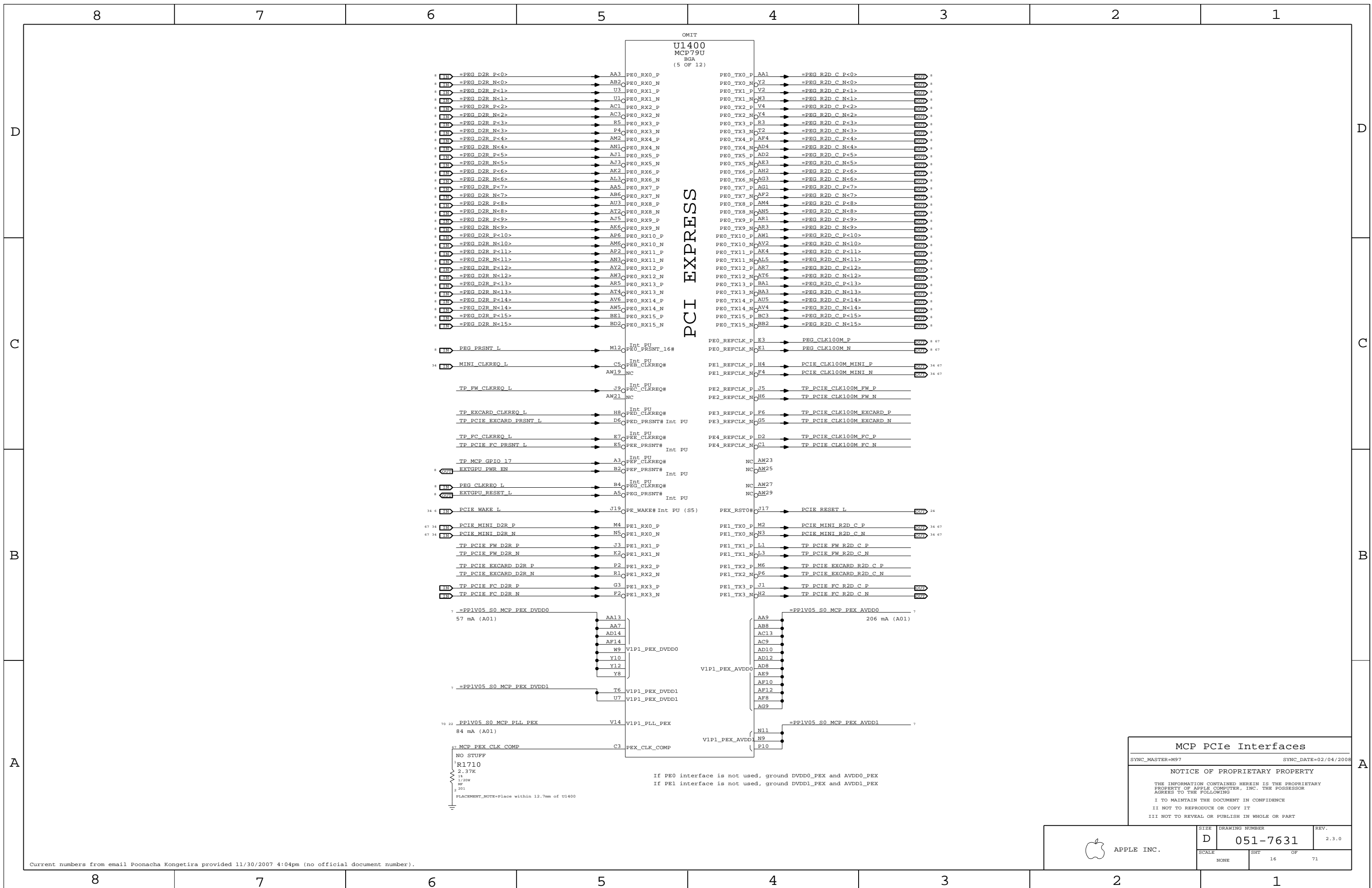
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7631</b>	REV. 2.3.0
	SCALE NONE	SHEET 15	OF 71

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



**MCP PCIe Interfaces**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

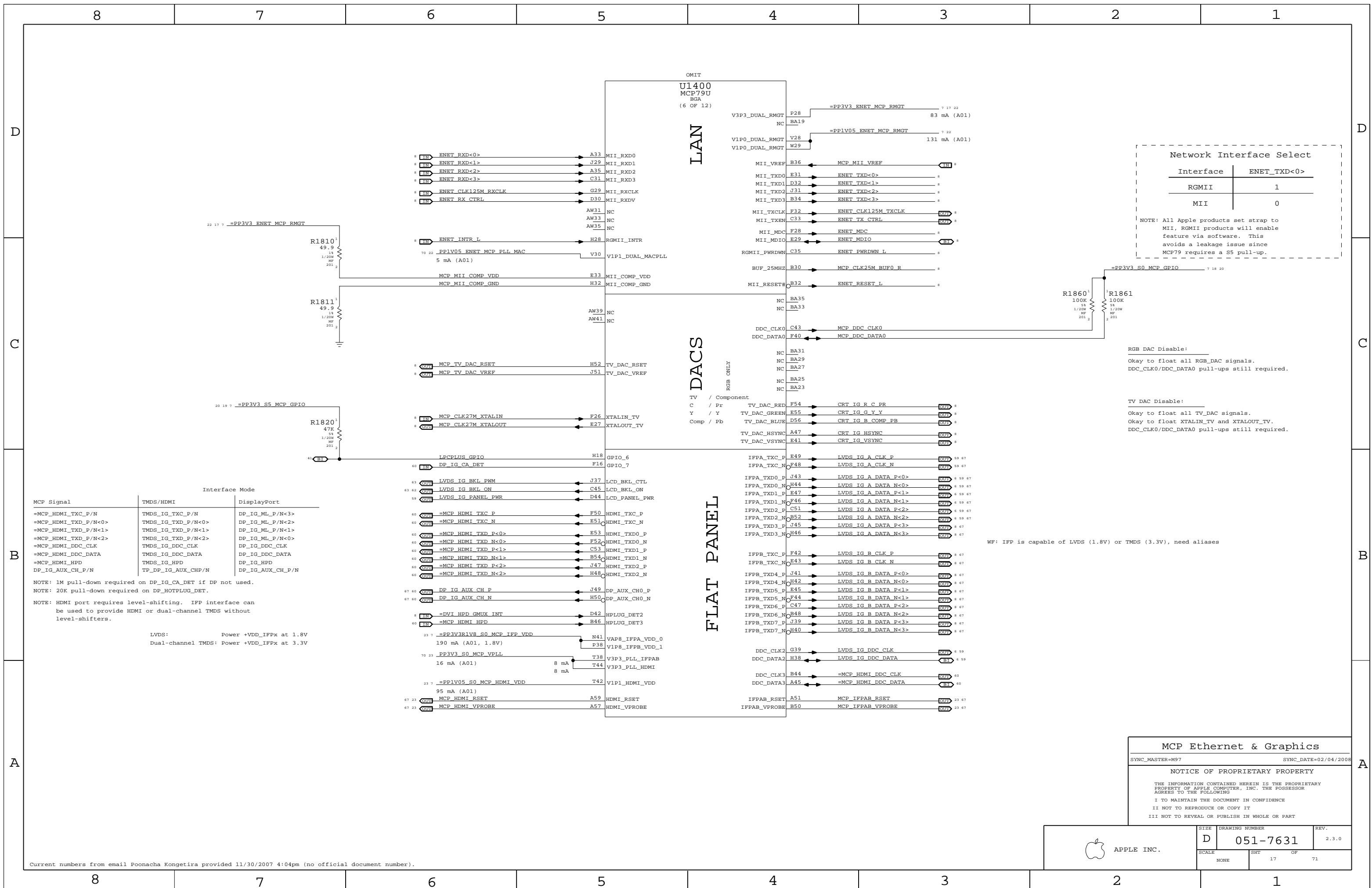
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7631</b>	REV. 2.3.0
	SCALE NONE	SHEET 16	OF 71

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).





Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:  
 Okay to float all RGB\_DAC signals.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

TV DAC Disable:  
 Okay to float all TV\_DAC signals.  
 DDC\_CLK0/DDC\_DATA0 pull-ups still required.

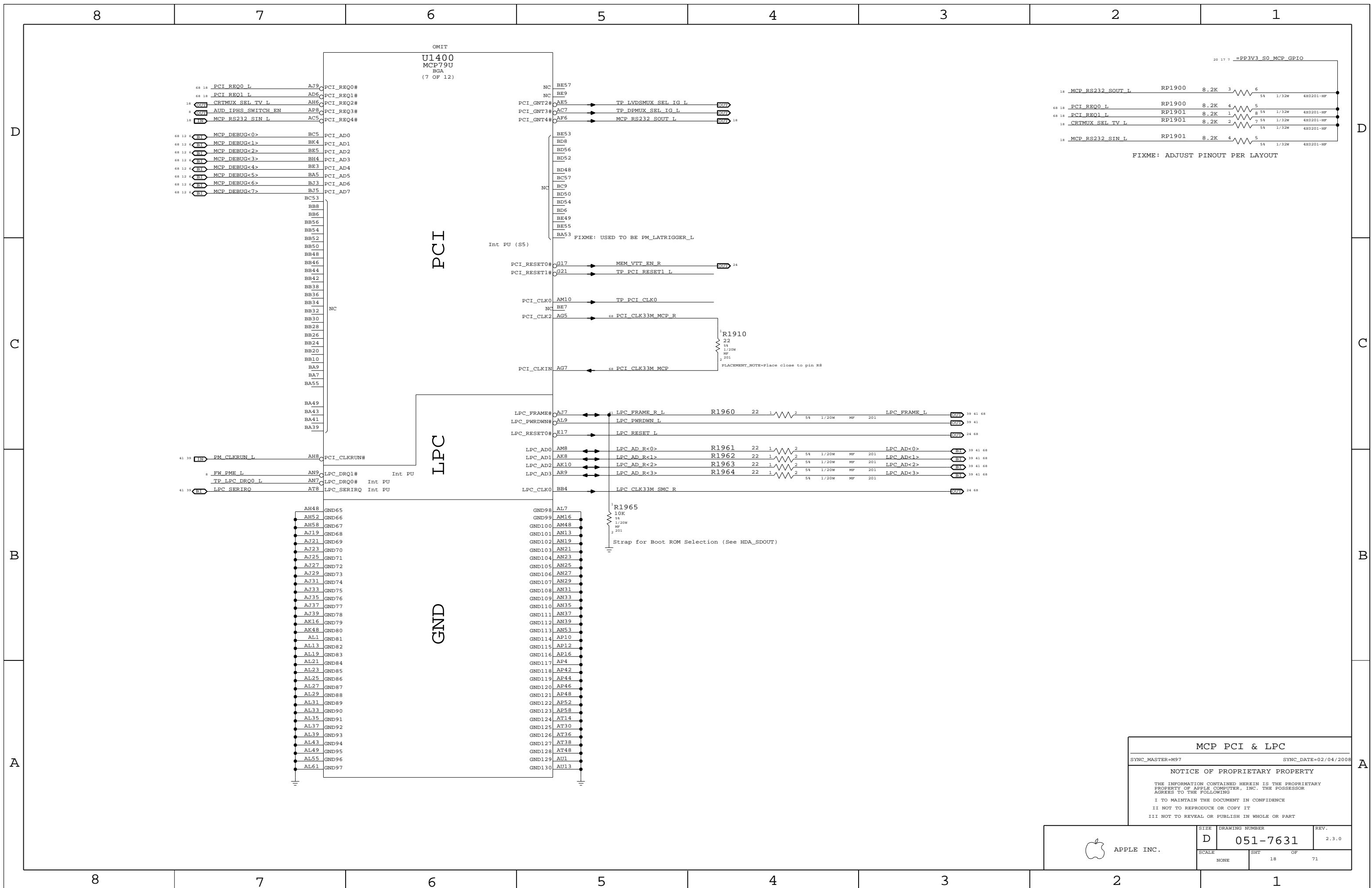
MCP Signal	Interface Mode	
	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP\_IG\_CA\_DET if DP not used.  
 NOTE: 20K pull-down required on DP\_HOTPLUG\_DET.  
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD\_IPFx at 1.8V  
 Dual-channel TMDS: Power +VDD\_IPFx at 3.3V

MCP Ethernet & Graphics  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		17	71



**MCP PCI & LPC**

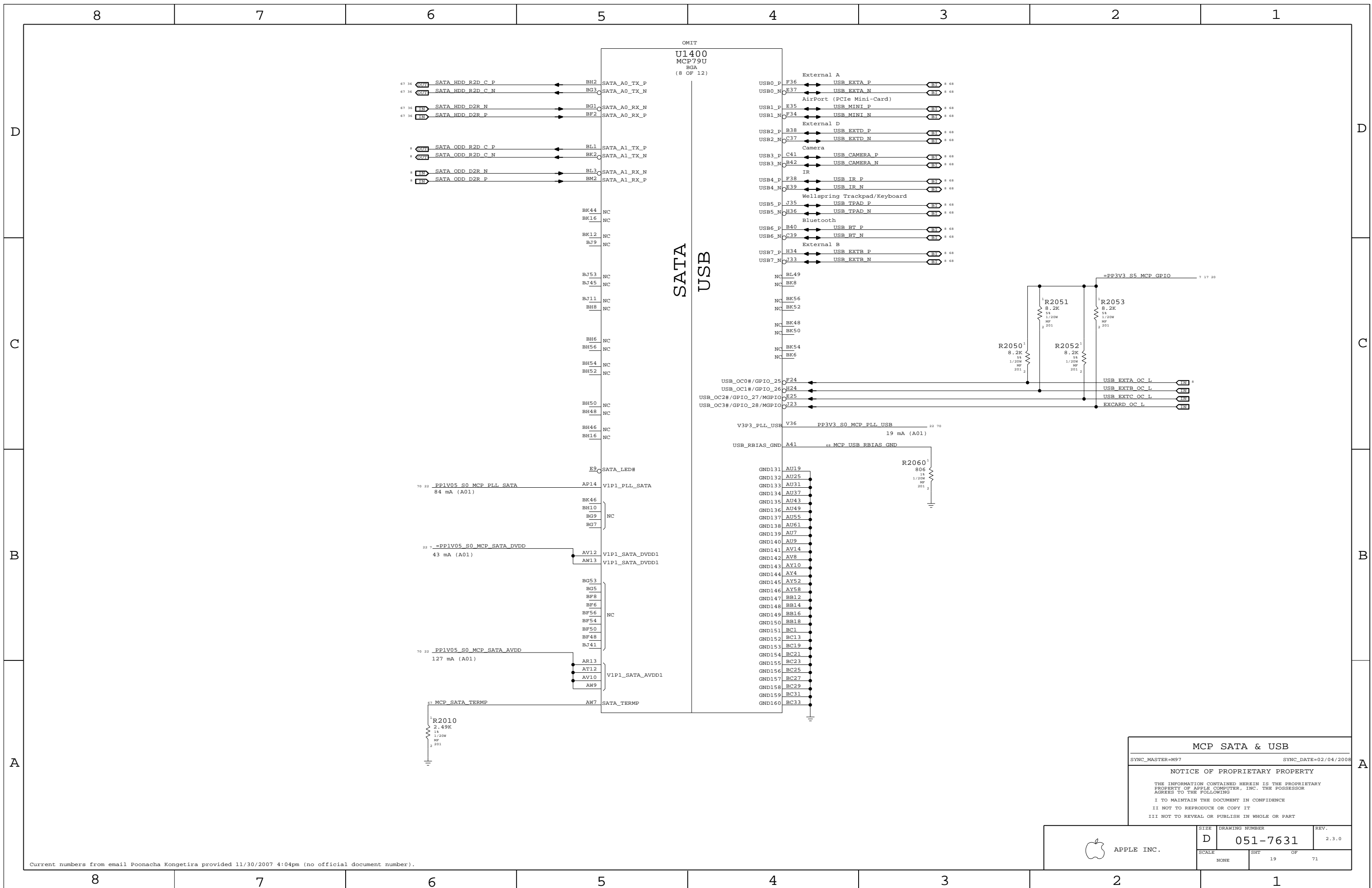
SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	18		



**MCP SATA & USB**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

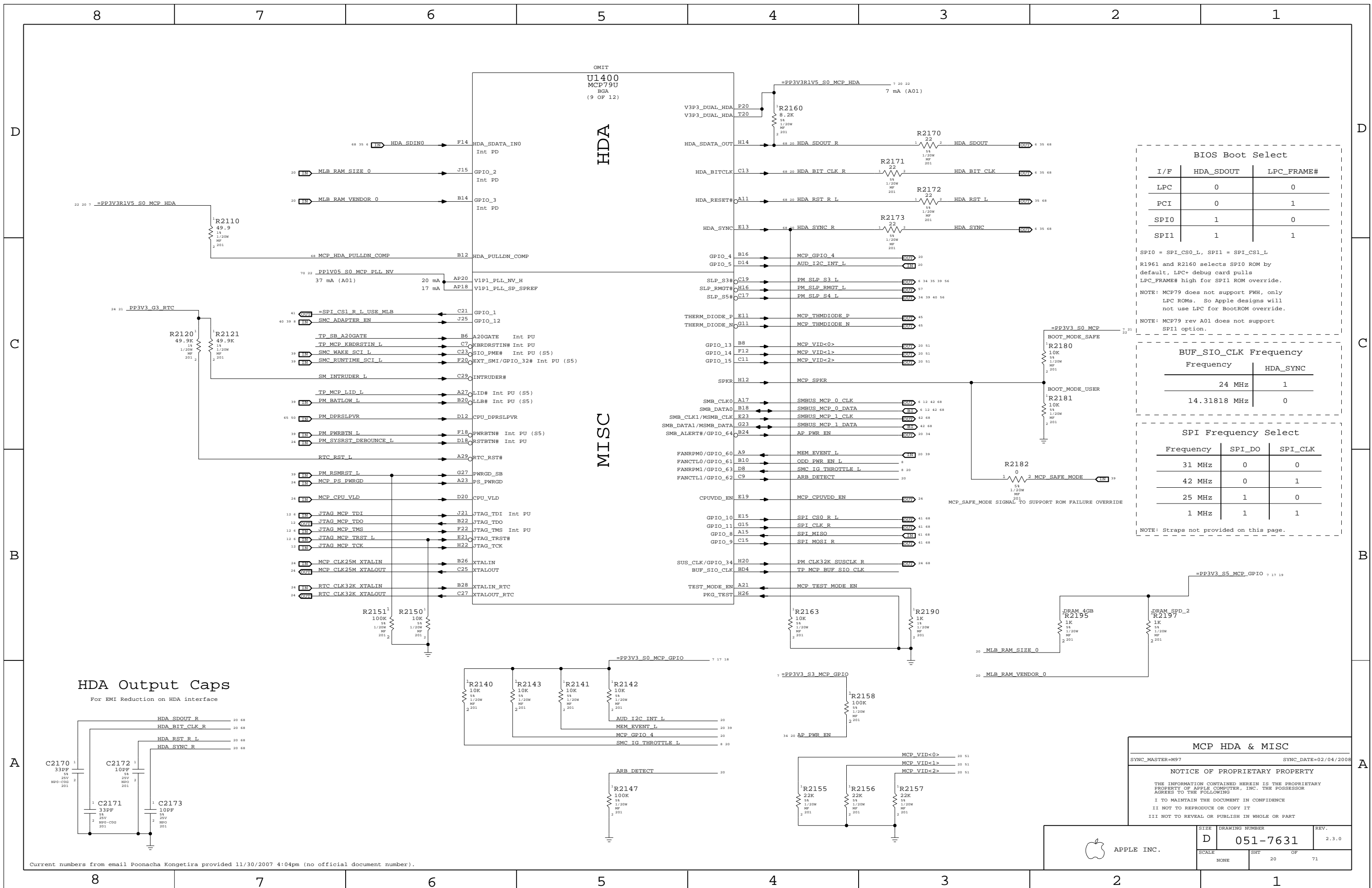
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		
NONE	19 OF 71		

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



**BIOS Boot Select**

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI\_CS0\_L, SPI1 = SPI\_CS1\_L  
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC\_FRAME# high for SPI1 ROM override.  
 NOTE: MCP79 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.  
 NOTE: MCP79 rev A01 does not support SPI1 option.

**BUF\_SIO\_CLK Frequency**

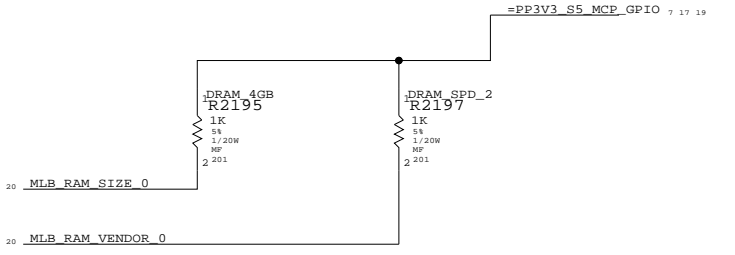
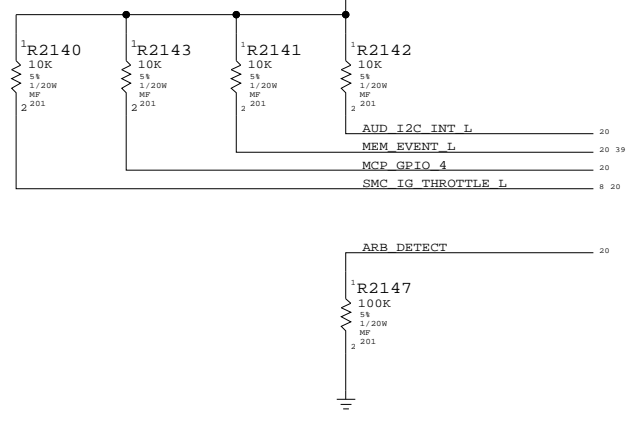
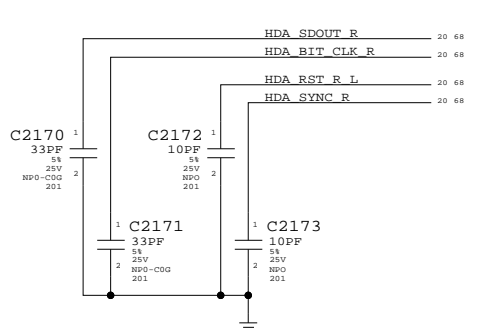
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

**SPI Frequency Select**

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

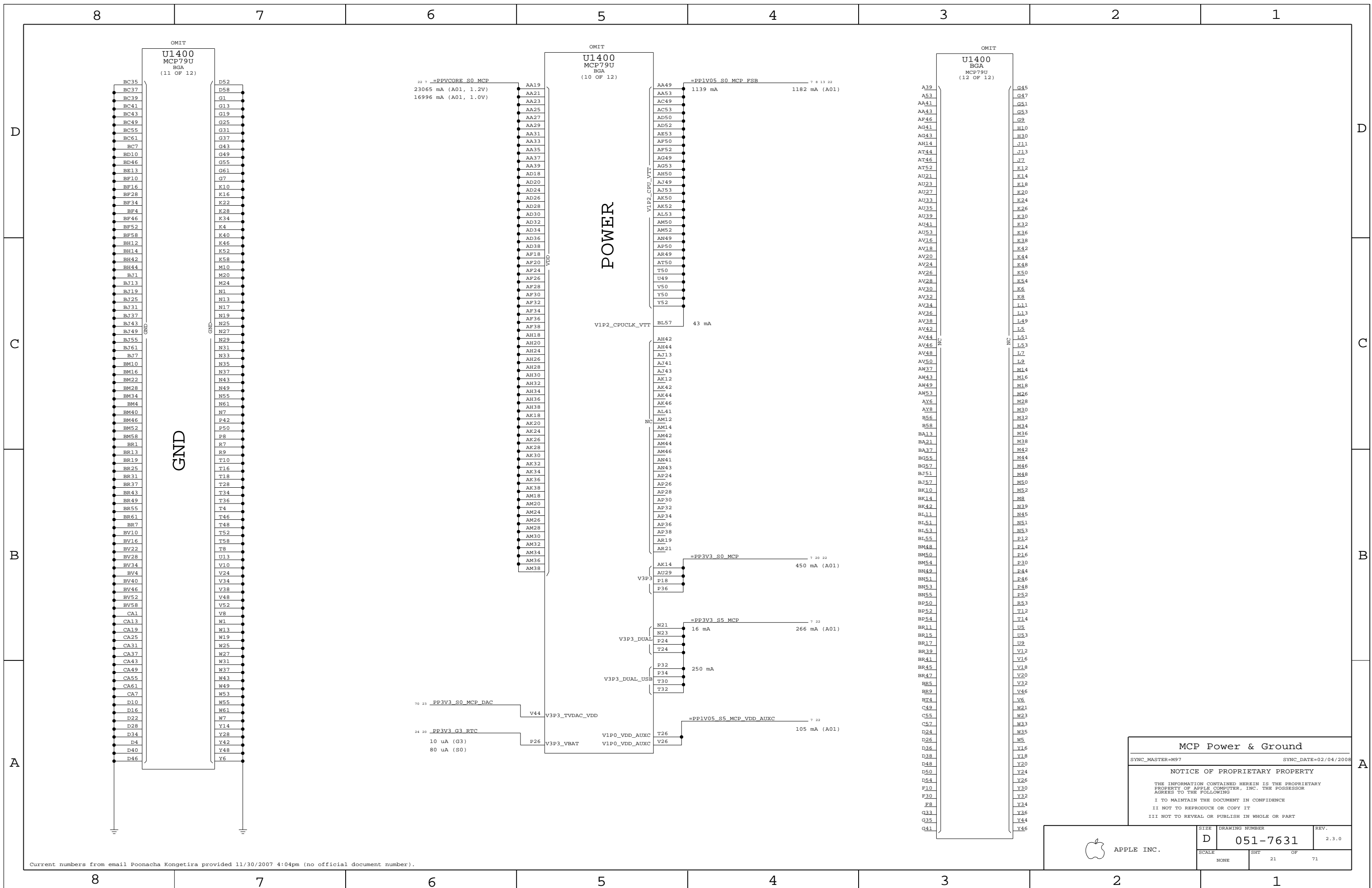
**HDA Output Caps**  
For EMI Reduction on HDA interface



**MCP HDA & MISC**  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		20	71

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



22 7 =PPVCORE\_S0\_MCP  
23065 mA (A01, 1.2V)  
16996 mA (A01, 1.0V)

70 23 PP3V3\_S0\_MCP\_DAC  
24 20 PP3V3\_G3\_RTC  
10 uA (G3)  
80 uA (S0)

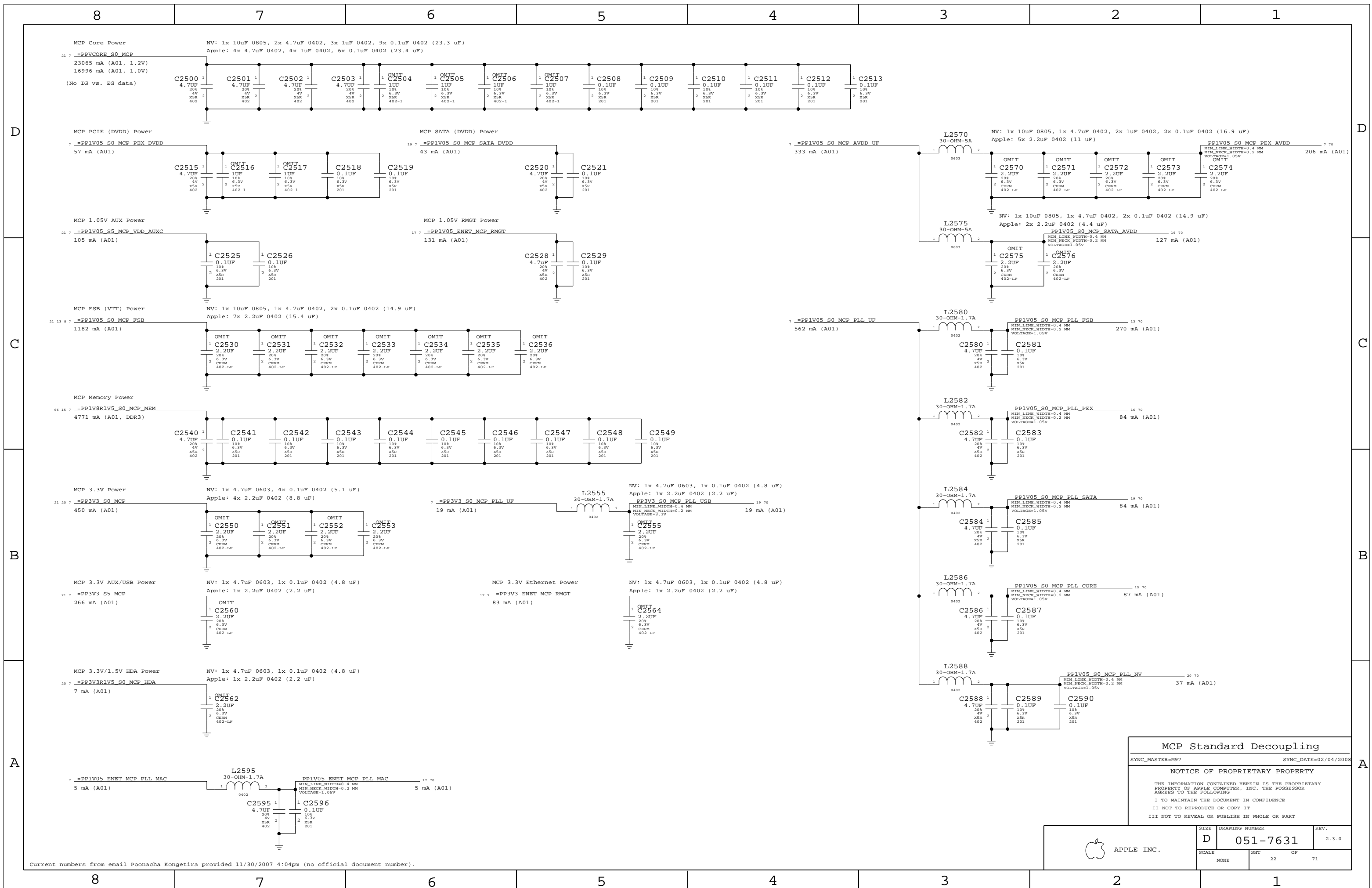
POWER

GND

MCP Power & Ground  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	
NONE	21	71	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



**MCP Standard Decoupling**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
APPLE INC.	D	051-7631	2.3.0
SCALE	SHEET	OF	71
NONE	22	22	71

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

8

7

6

5

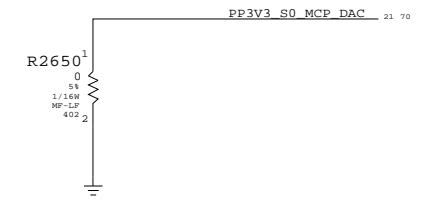
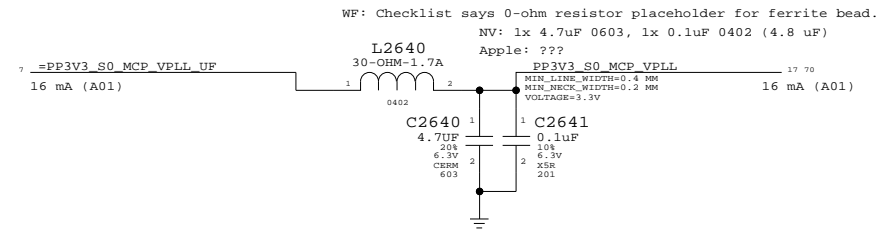
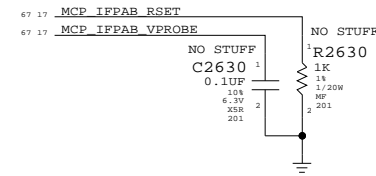
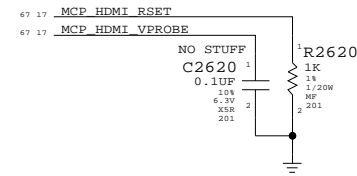
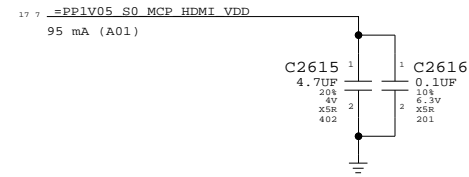
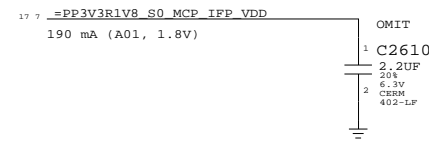
4

3

2

1

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.  
 NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)  
 Apple: 1x 2.2uF 0402 (2.2 uF)



SYNC FROM M97

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Graphics Support  
 SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	
NONE	23	71	

8

7

6

5

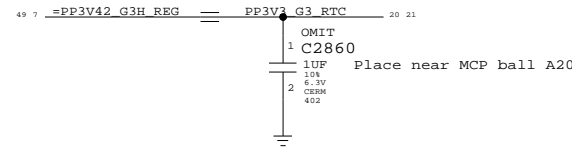
4

3

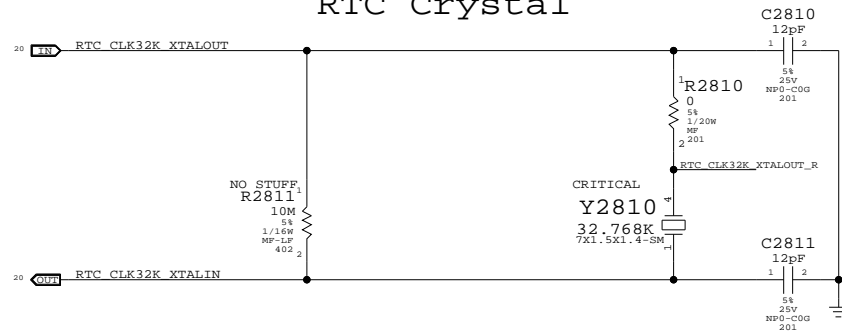
2

1

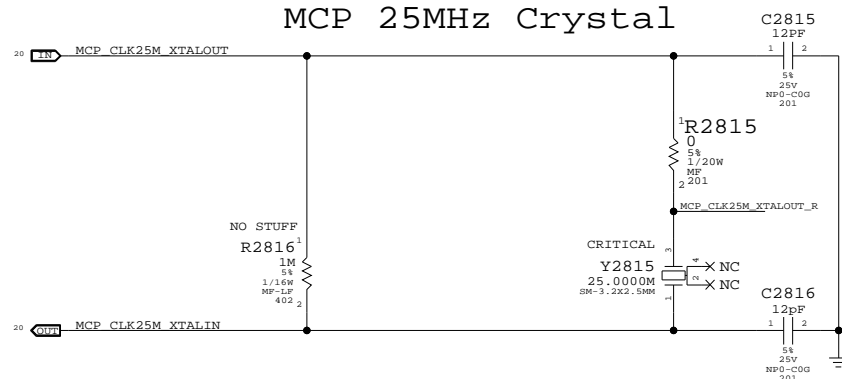
### RTC Power Sources



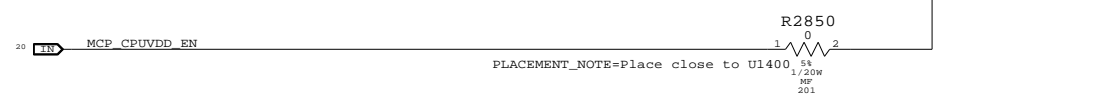
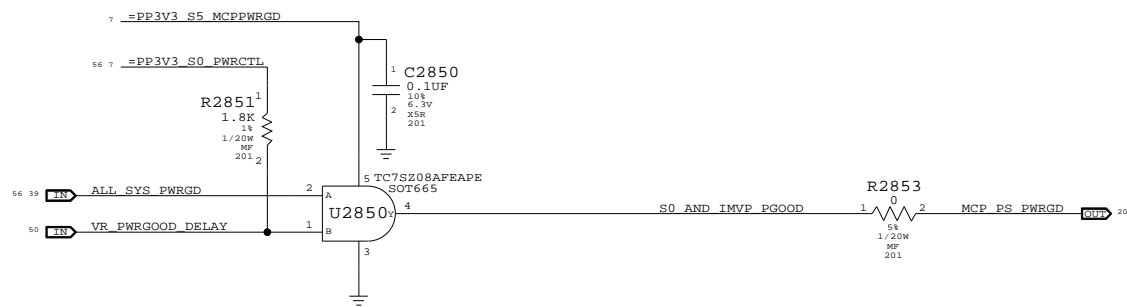
### RTC Crystal



### MCP 25MHz Crystal

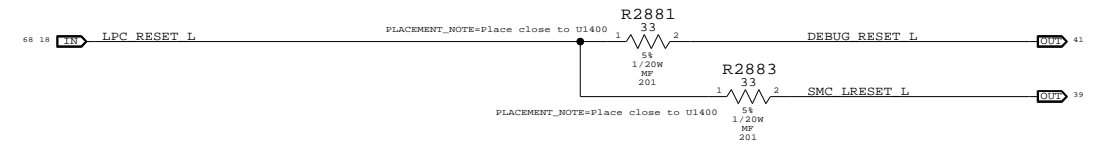


### MCP S0 PWRGD & CPU\_VLD

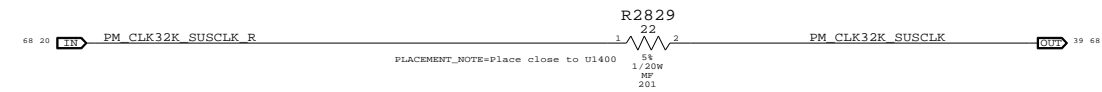
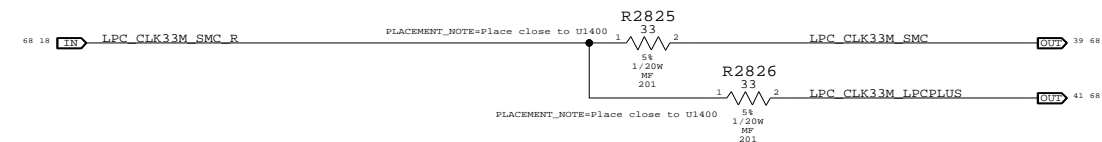
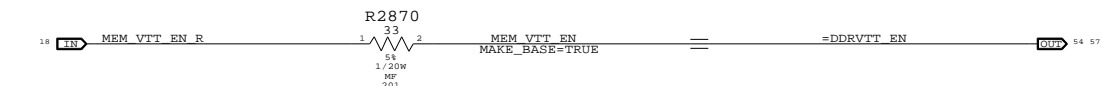
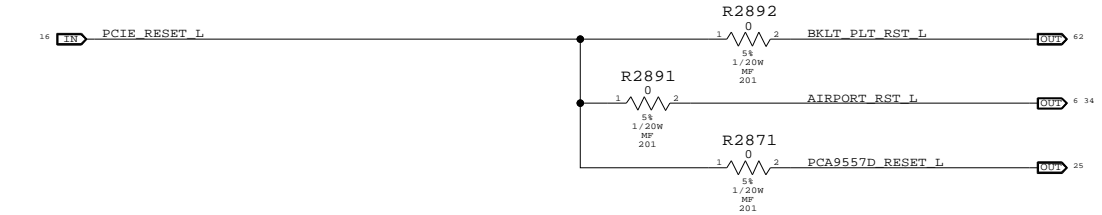


### Platform Reset Connections

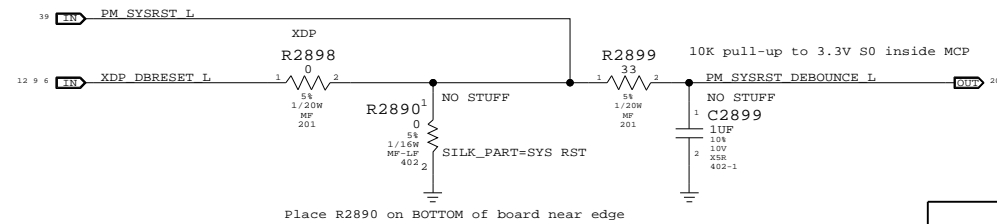
#### LPC Reset (Unbuffered)



#### PCIE Reset (Unbuffered)



### Reset Button



SYNC FROM M97  
 CHANGED RTC POWER SOURCE TO DIRECT CONNECTION  
 ADDED MCPSEQ\_SMC LOGIC

SB Misc			
SYNC_MASTER=M97	DRAWING NUMBER		REV.
	D	051-7631	2.3.0
	SCALE	SHT	OF
	NONE	24	71



APPLE INC.



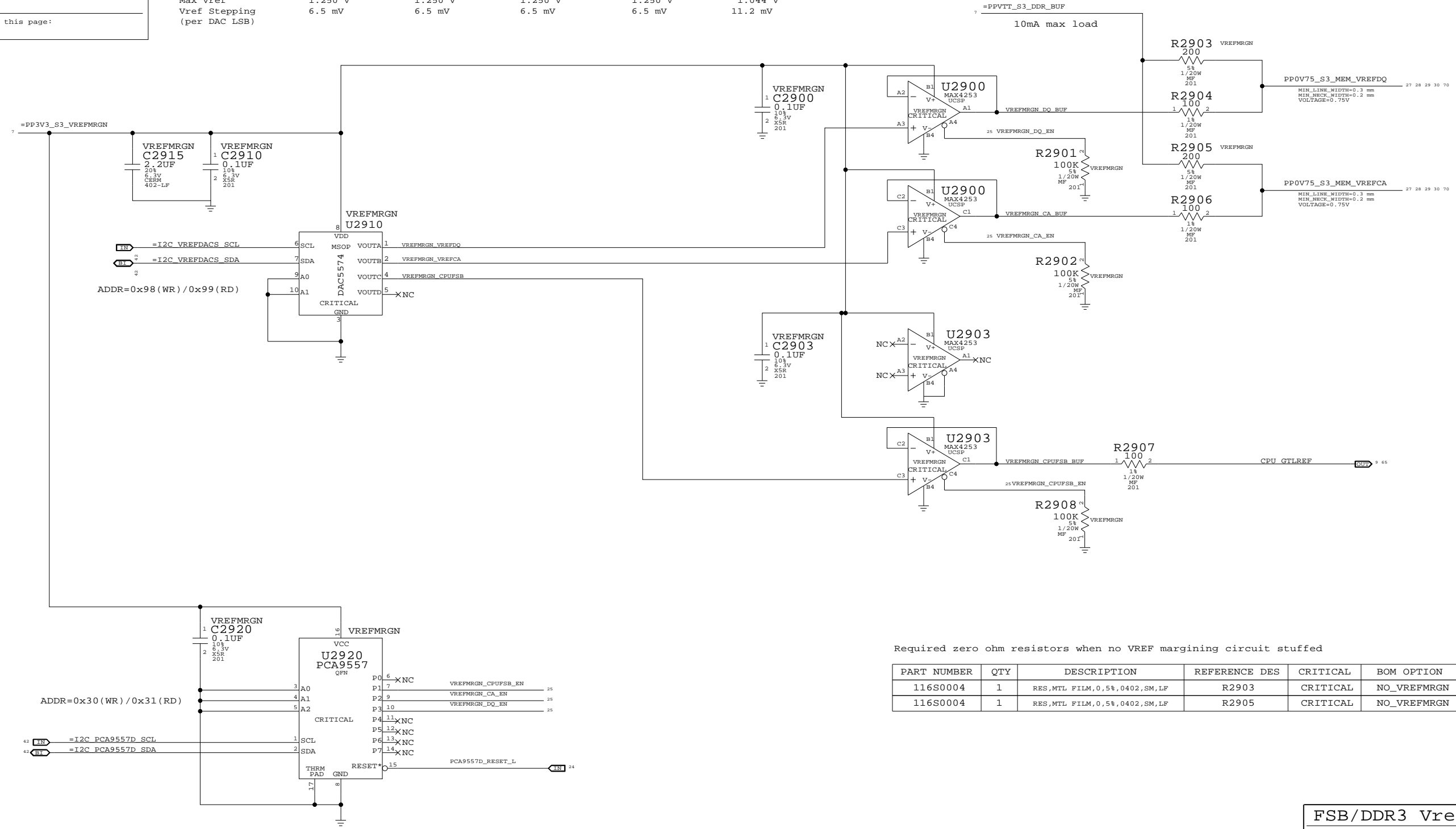
# Page Notes

Power aliases required by this page:  
 - =PP3V3\_S3\_VREFMRGN  
 - =PP3V3\_S5\_VREFMRGN  
 - =PPVTT\_S3\_DDR\_BUF

Signal aliases required by this page:  
 - =I2C\_VREFDACS\_SCL  
 - =I2C\_VREFDACS\_SDA  
 - =I2C\_PCA9557D\_SCL  
 - =I2C\_PCA9557D\_SDA

BOM options provided by this page:  
 VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN

## FSB/DDR3 Vref Margining

SYNC\_MASTER=BEN SYNC\_DATE=01/15/2008

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	25		

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

4

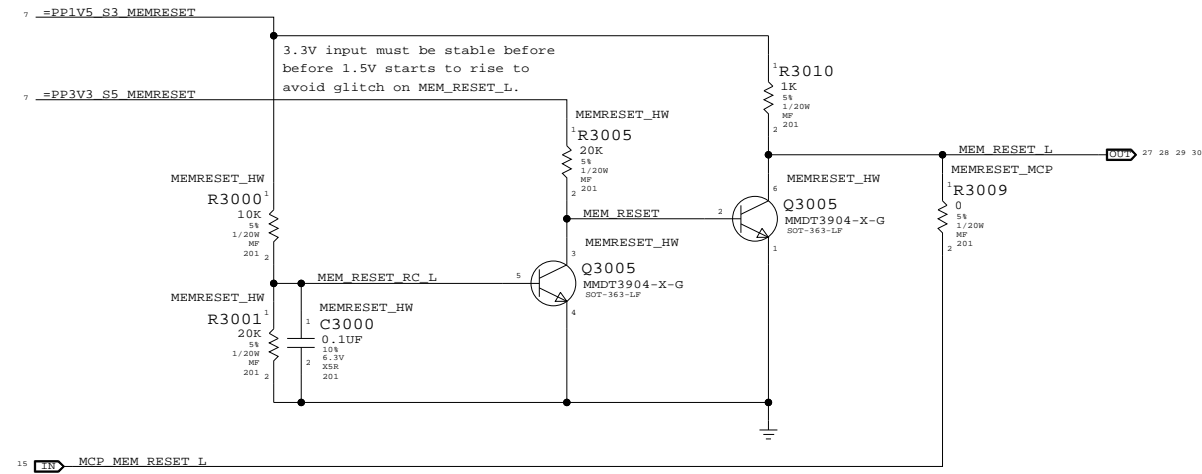
3

2

1

### DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



#### DDR3 Support

SYNC\_MASTER=T18\_MLB SYNC\_DATE=01/30/2008

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

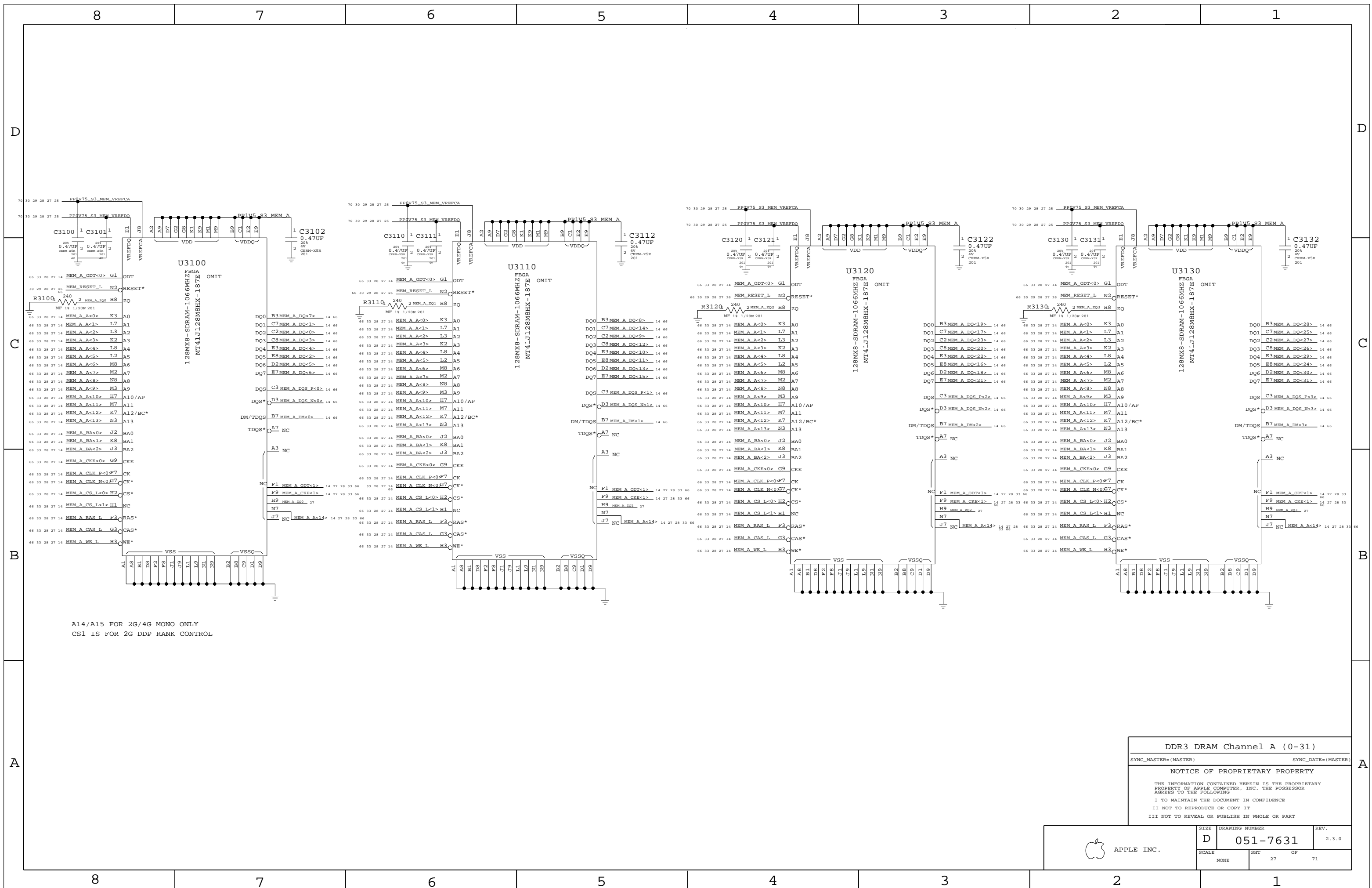
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

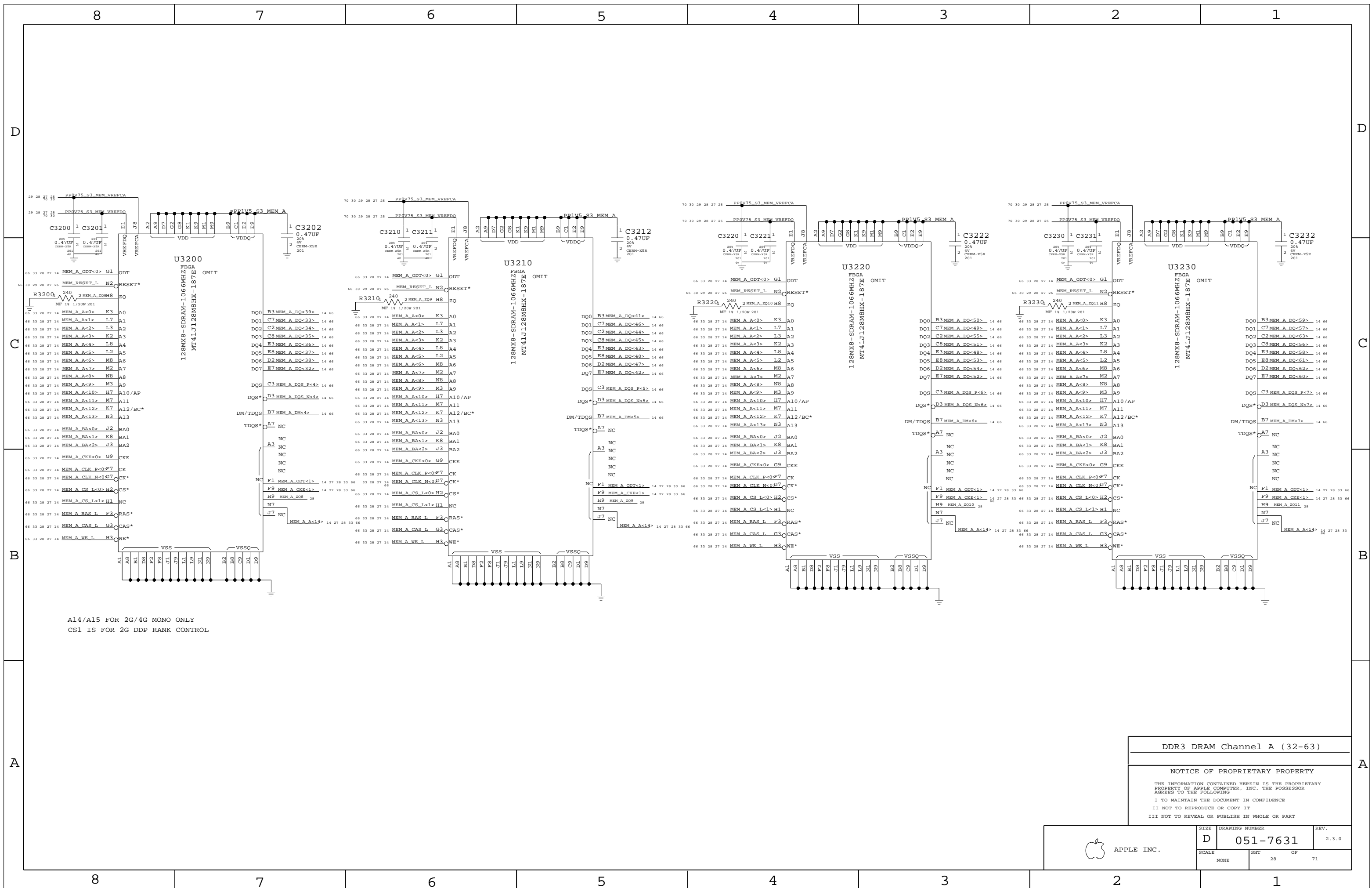
SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	26	71



A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel A (0-31)  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		27	71



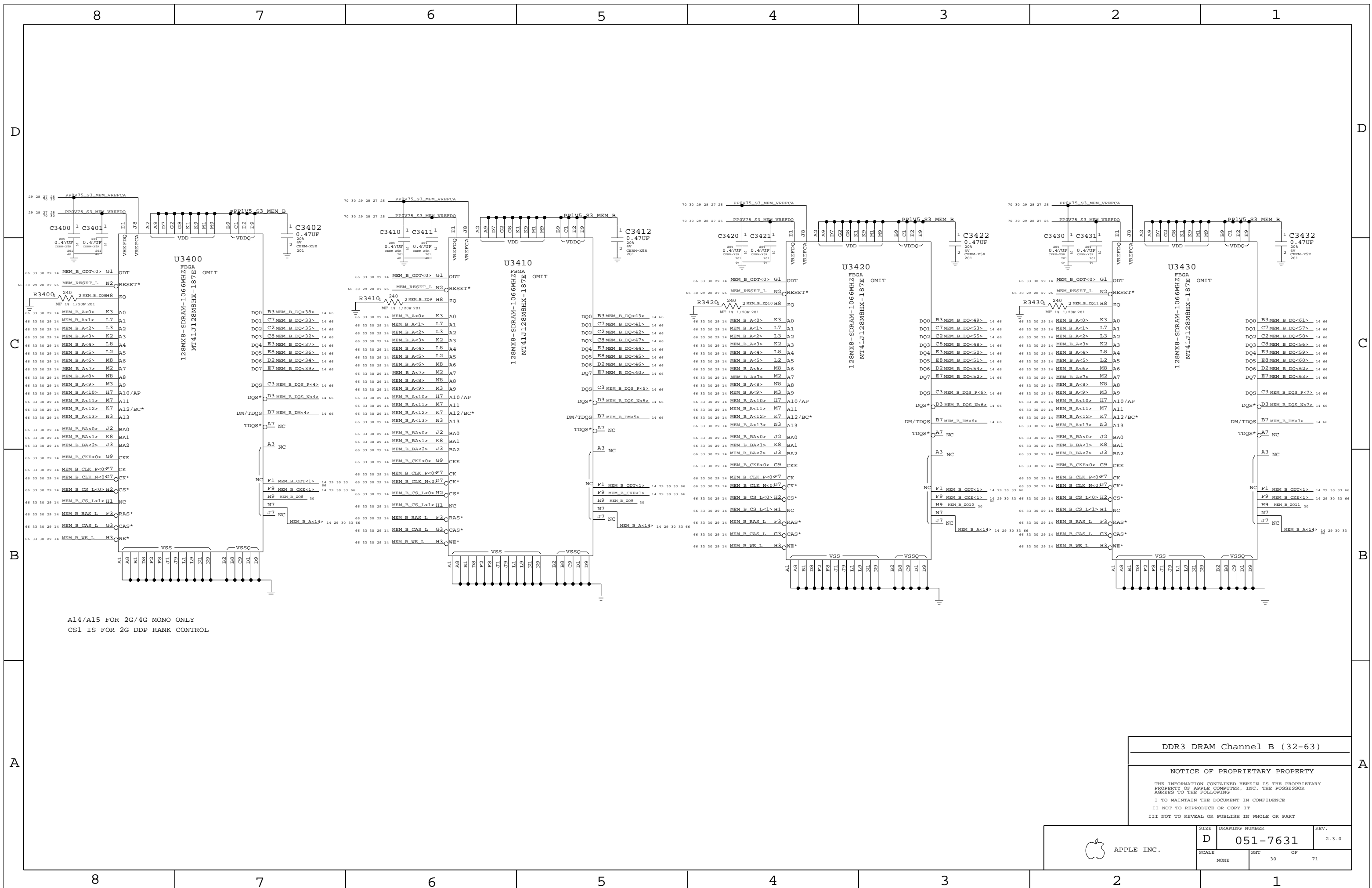
A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel A (32-63)

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	28		





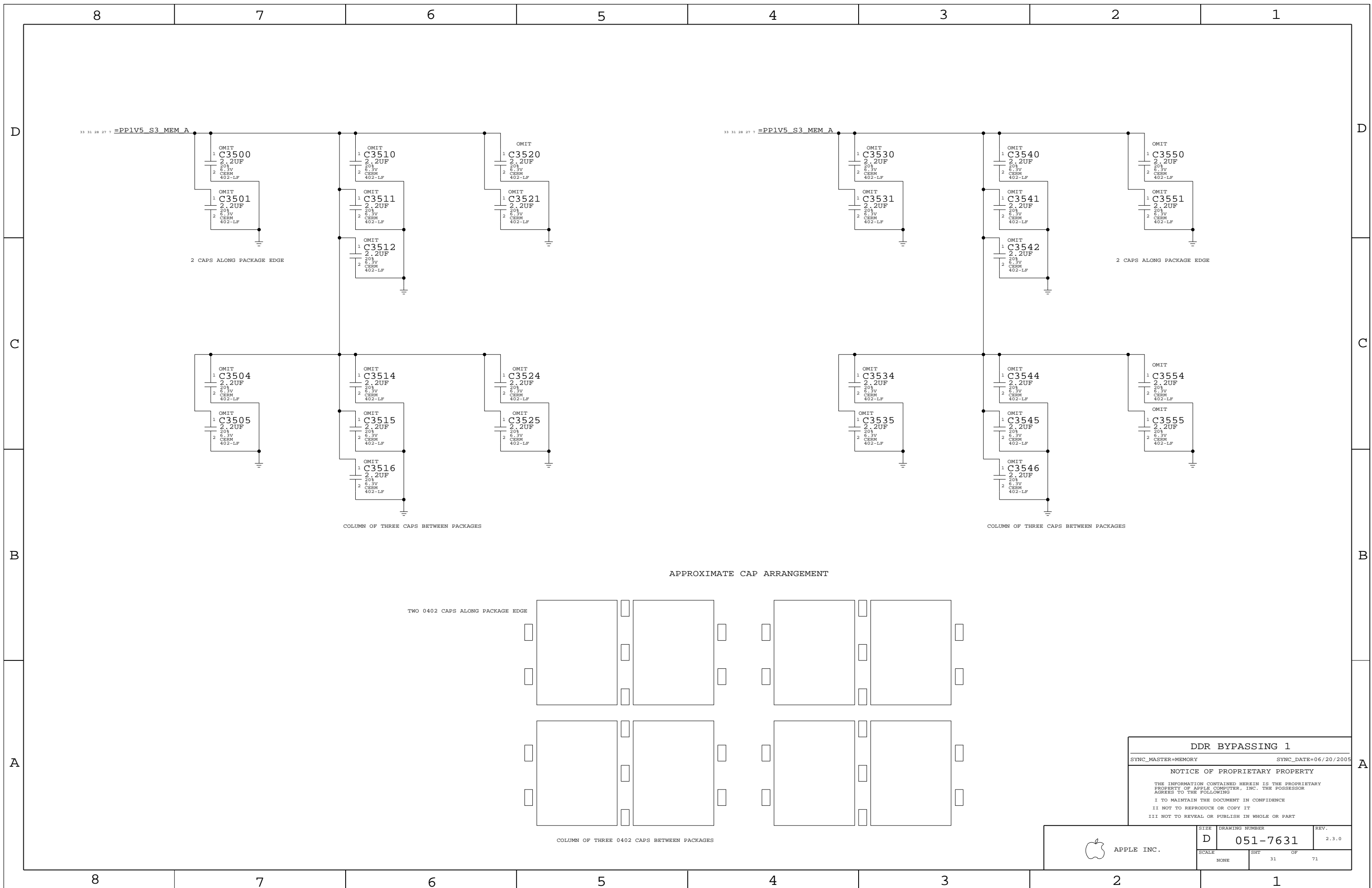
A14/A15 FOR 2G/4G MONO ONLY  
 CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel B (32-63)

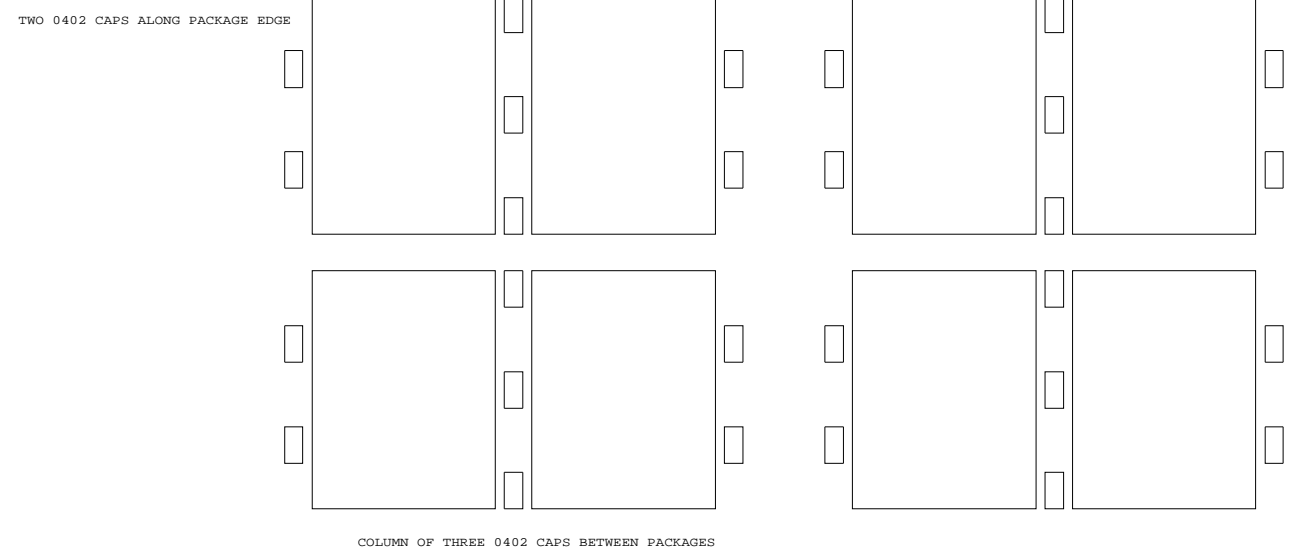
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7631	2.3.0
SHEET 30 OF 71			

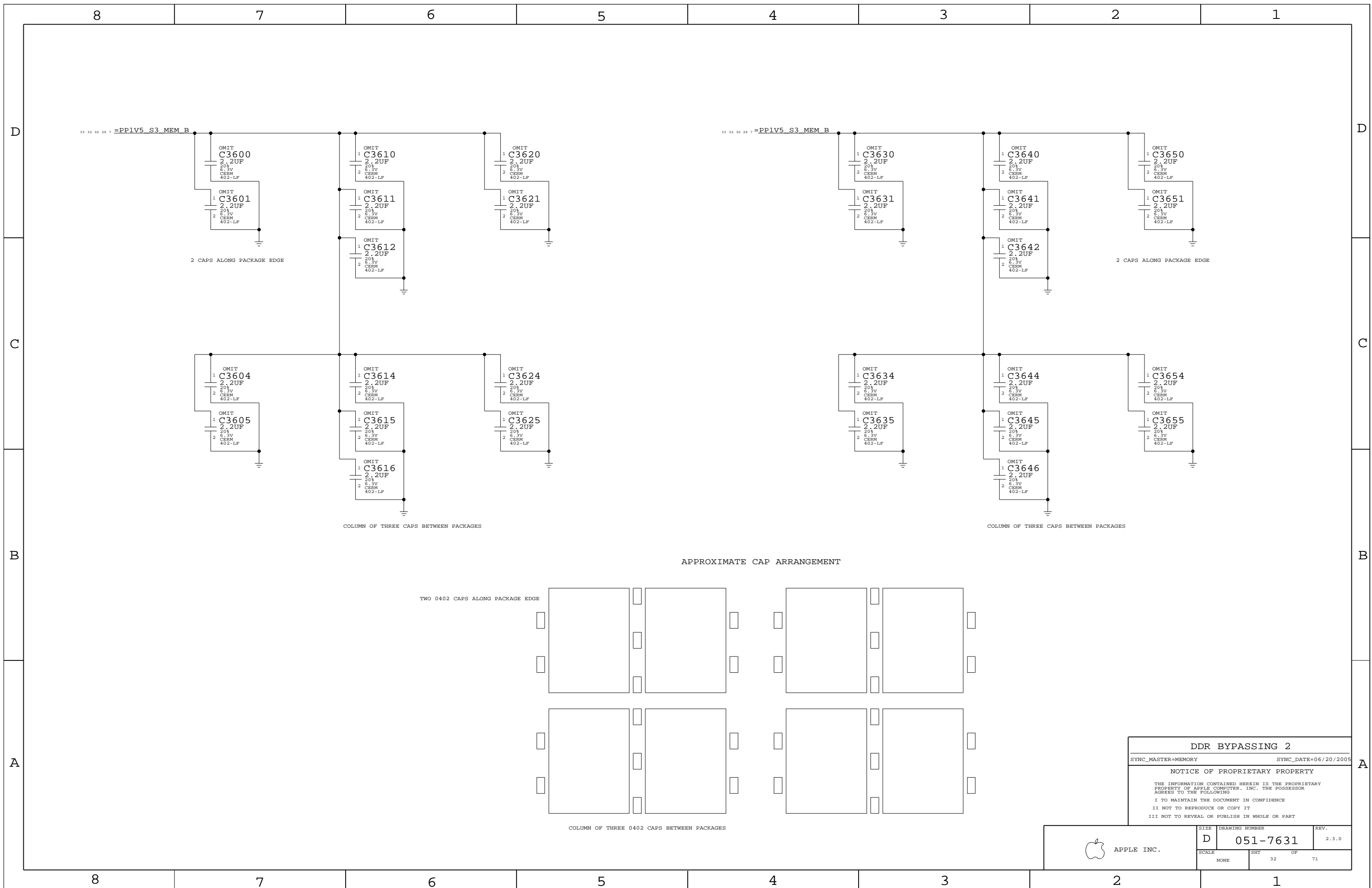


APPROXIMATE CAP ARRANGEMENT



DDR BYPASSING 1  
 SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	31		



APPROXIMATE CAP ARRANGEMENT

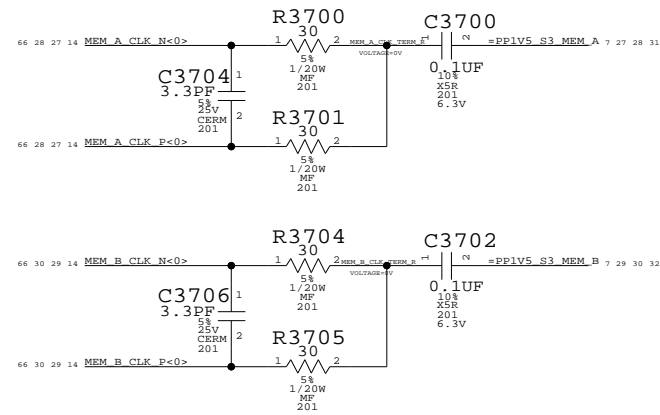
DDR BYPASSING 2  
 SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHEET		OF
NONE	32		71

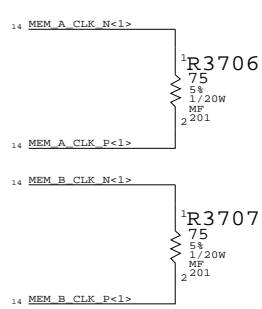


MEM CLOCK TERMINATION

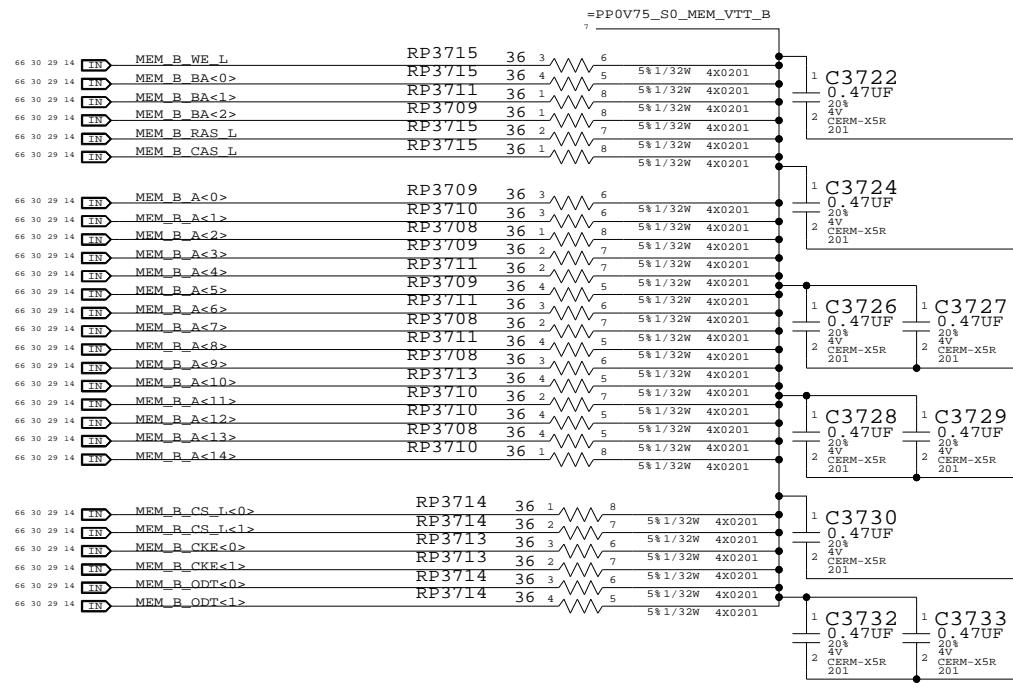
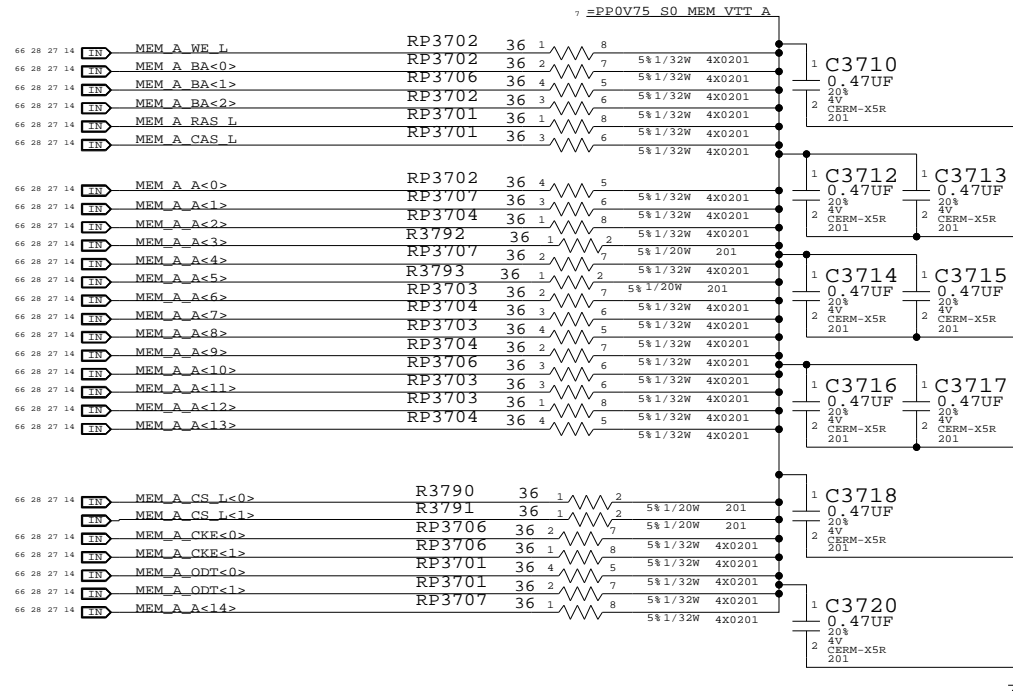
Place RC end termination after last DRAM  
Place Source Cterm at neckdown at first DRAM



Unused Clock Termination



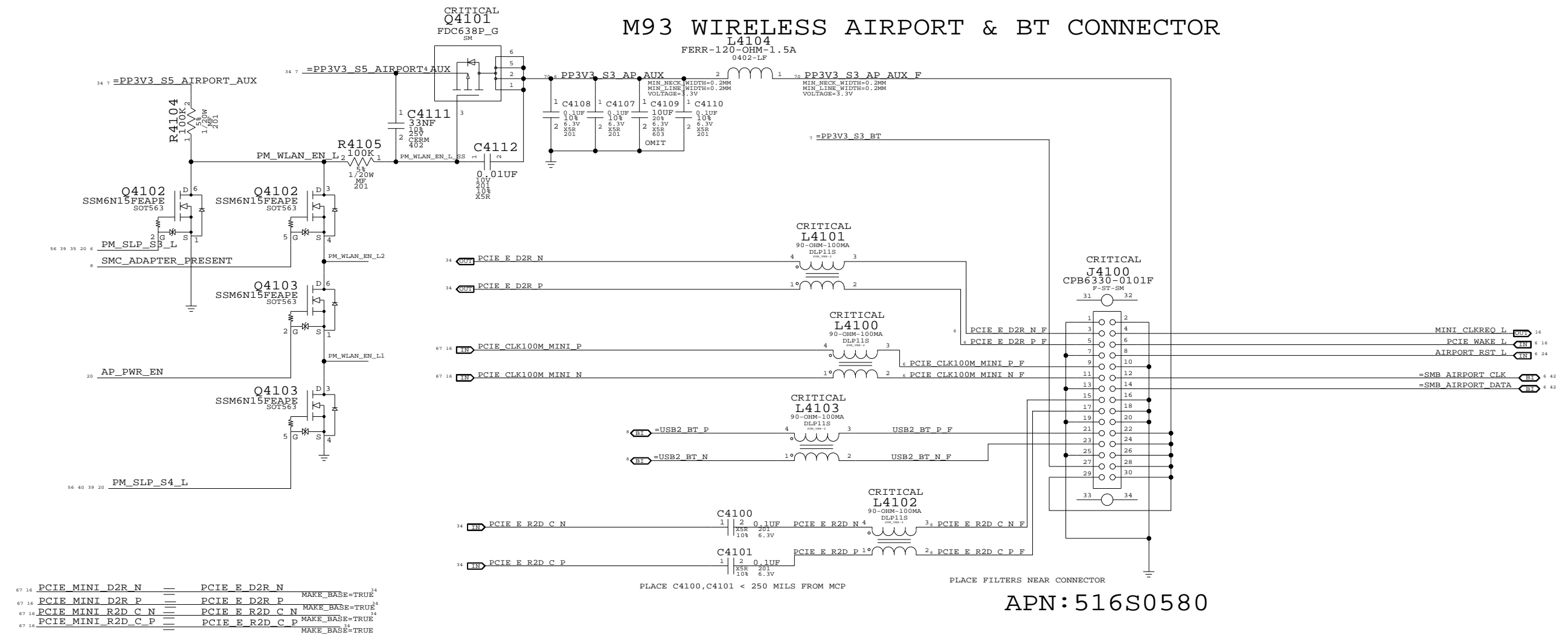
JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE



Memory Active Termination

NOTICE OF PROPRIETARY PROPERTY  
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

# M93 WIRELESS AIRPORT & BT CONNECTOR



APN: 516S0580

Wireless M93 Connector

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

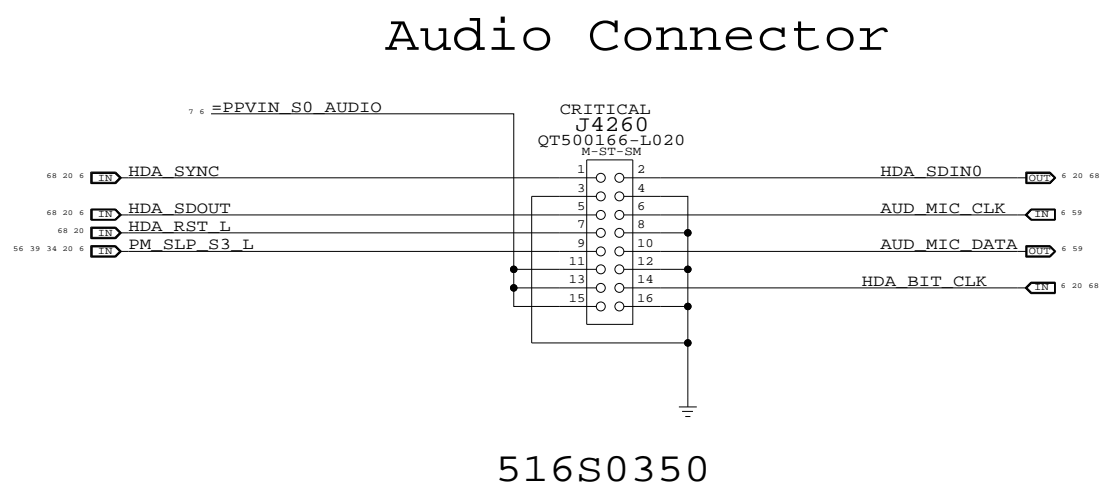
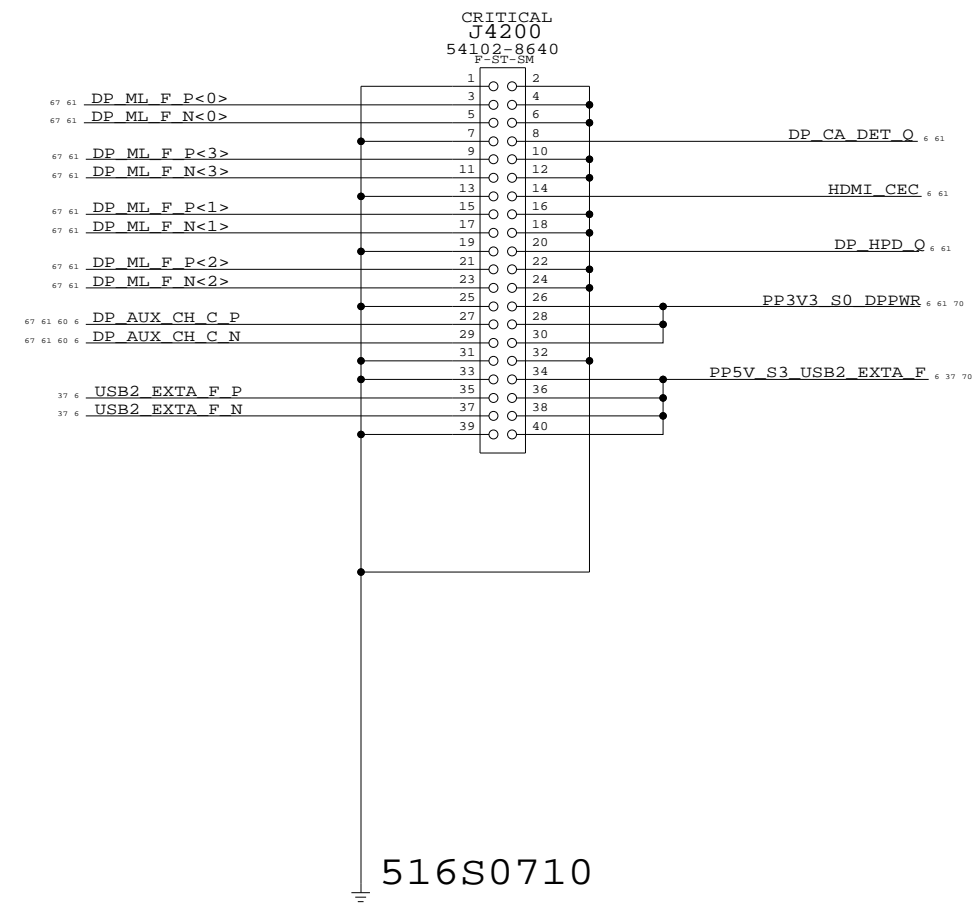
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	34		

# Micro-DisplayPort / USB to RIO Hatch Assembly



Hatch and Audio Connectors  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT		OF
NONE	35		71

8

7

6

5

4

3

2

1

D

D

C

C

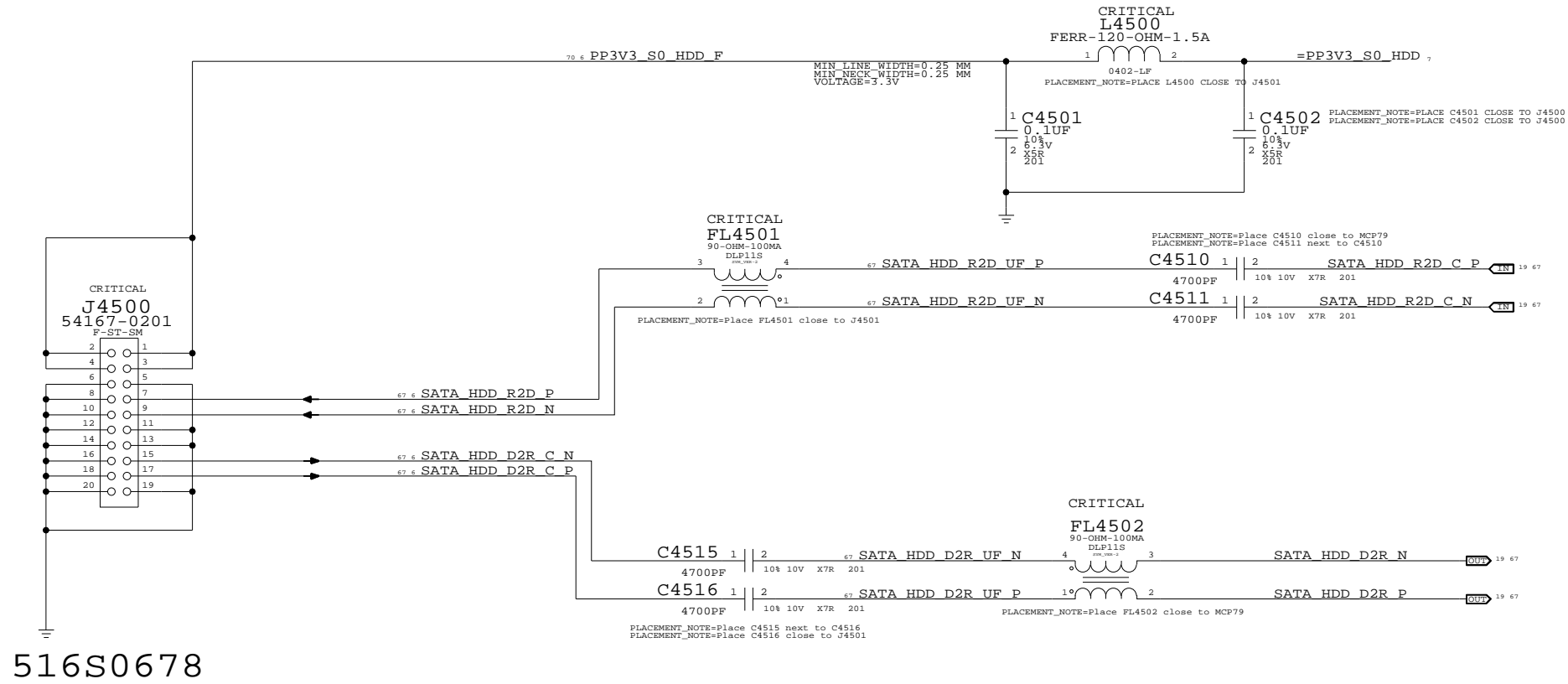
B

B

A

A

### SATA HDD PORT



**SATA Connectors**

SYNC\_MASTER=CHANGZHANG SYNC\_DATE=02/05/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
II NOT TO REPRODUCE OR COPY IT  
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		
NONE	36 OF		71

8

7

6

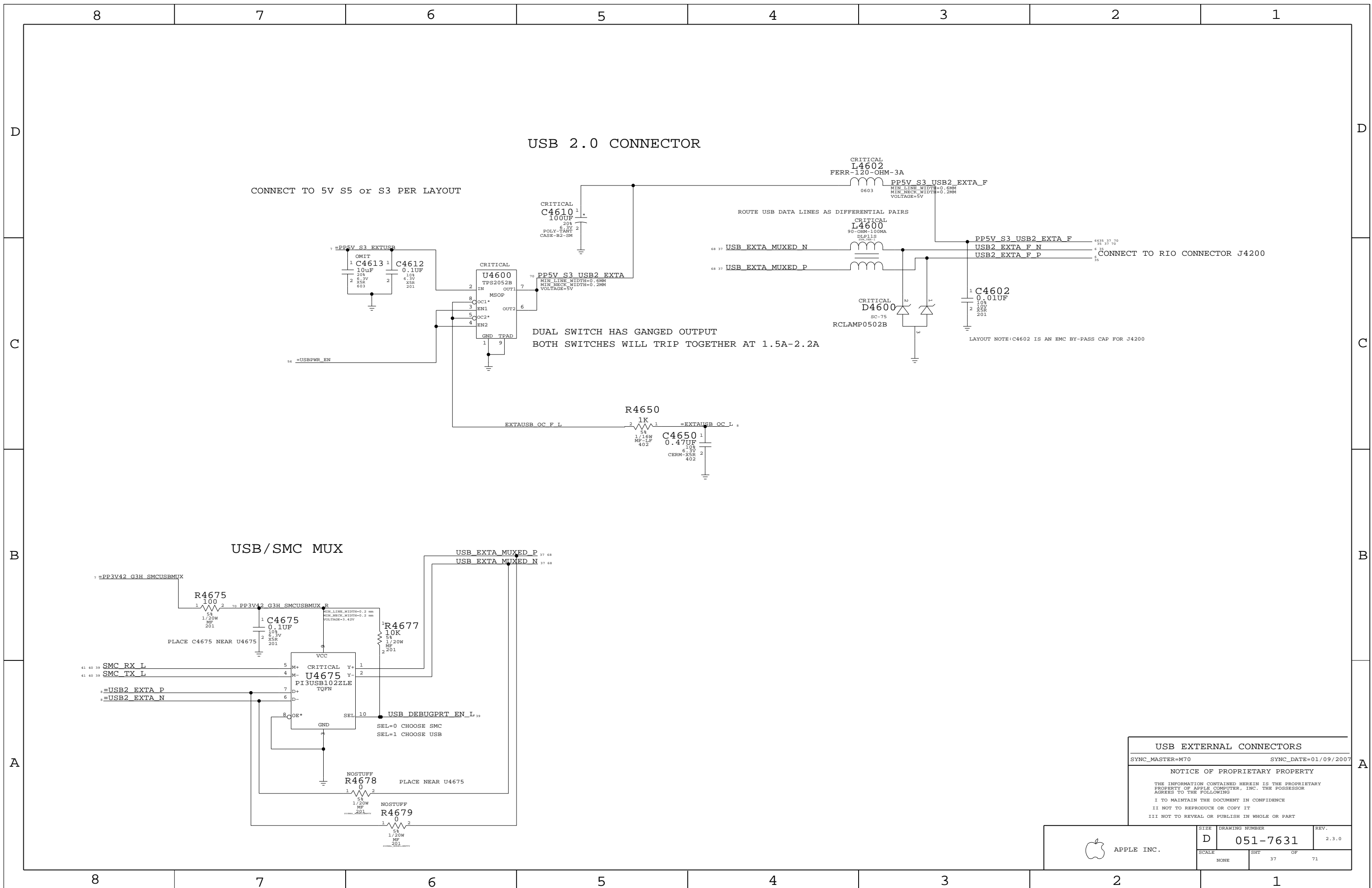
5

4

3

2

1



**USB EXTERNAL CONNECTORS**

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

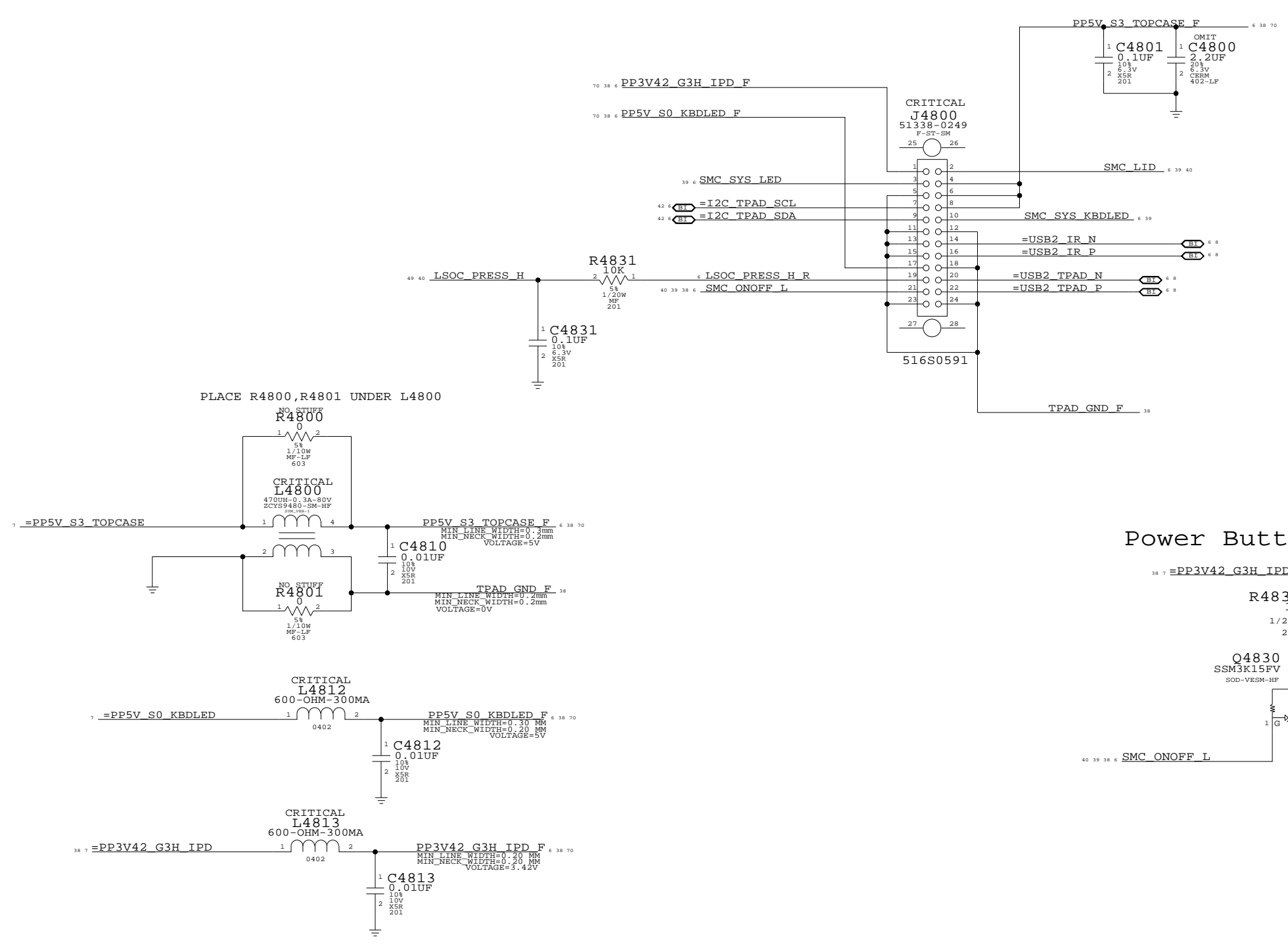
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

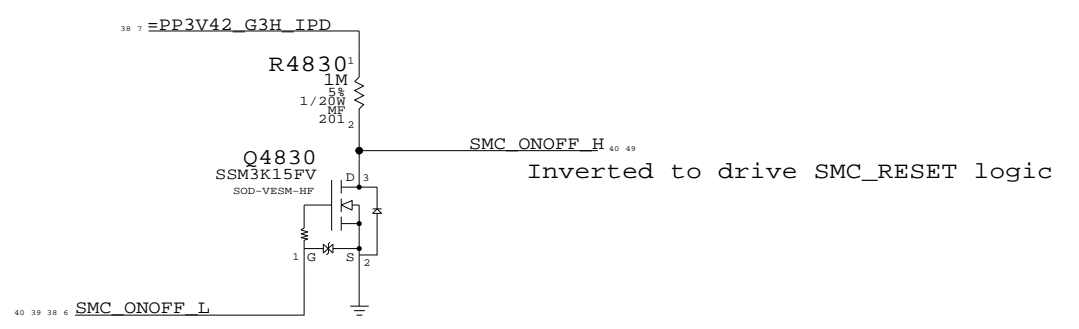
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	37		

# IPD Connector



## Power Button Inverter



**IPD Connector**

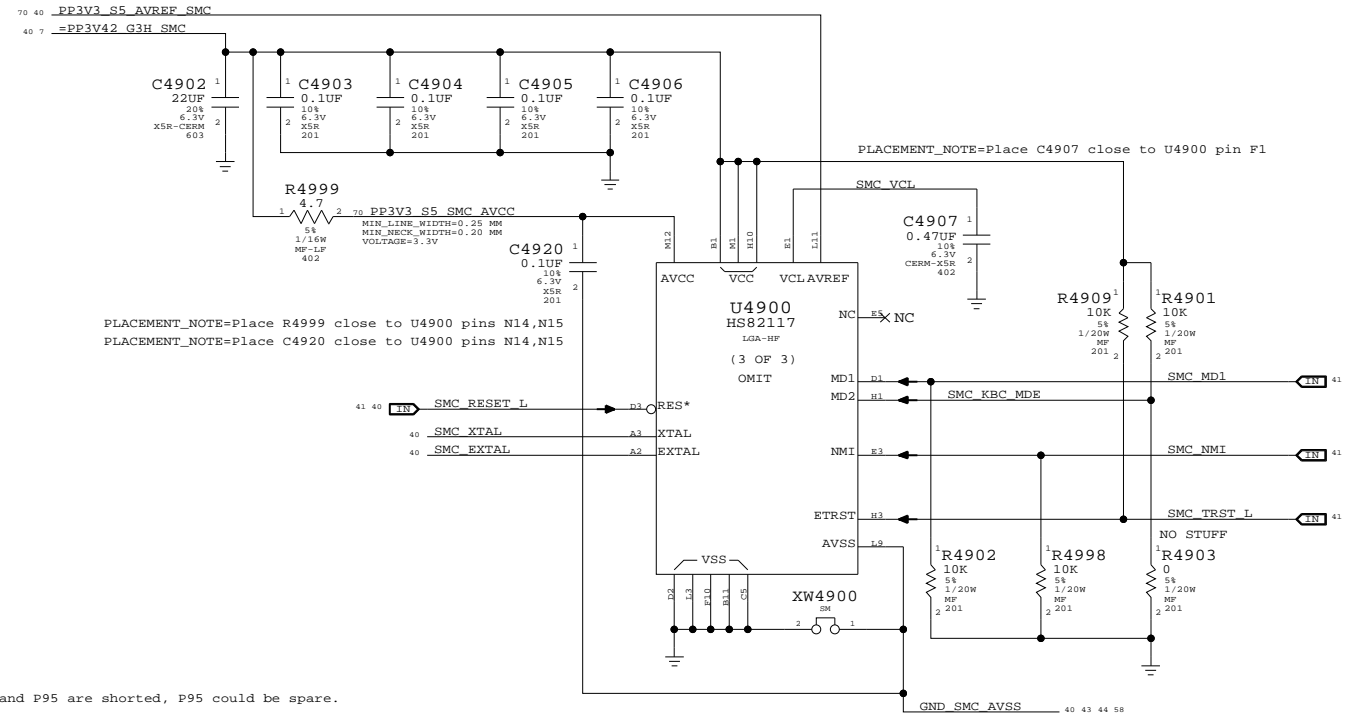
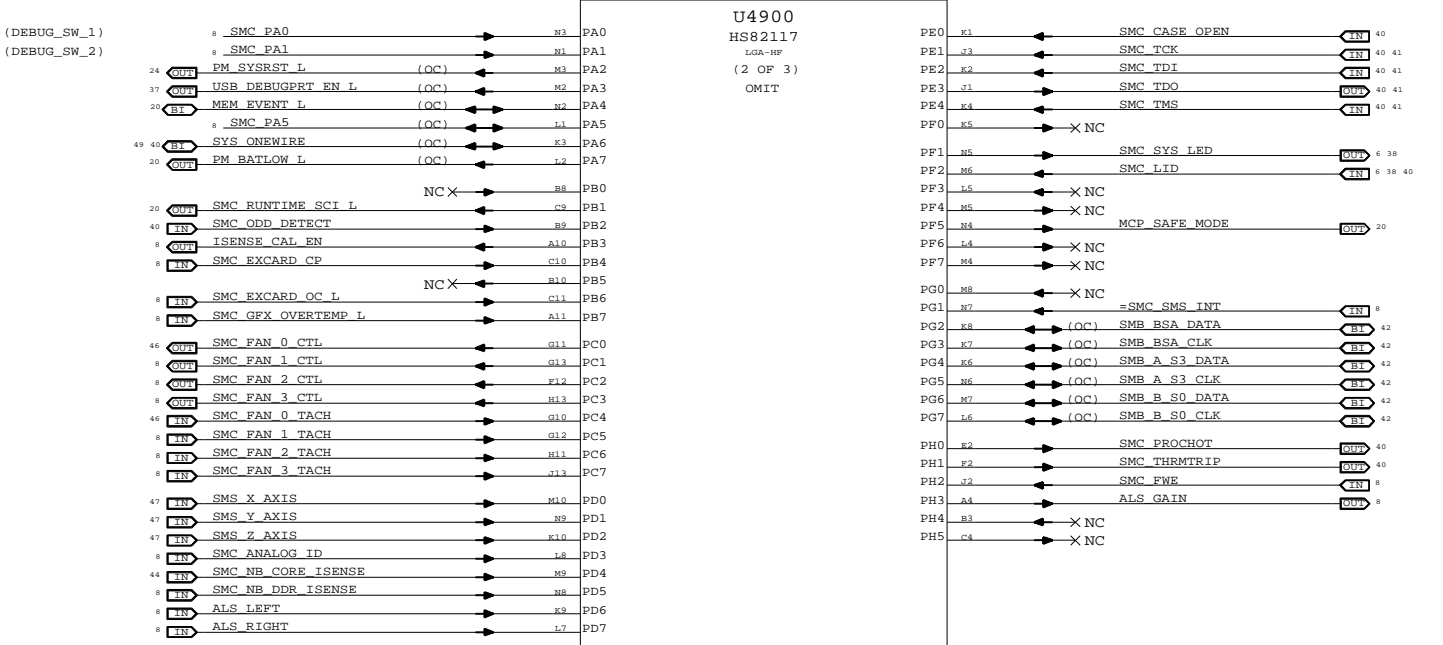
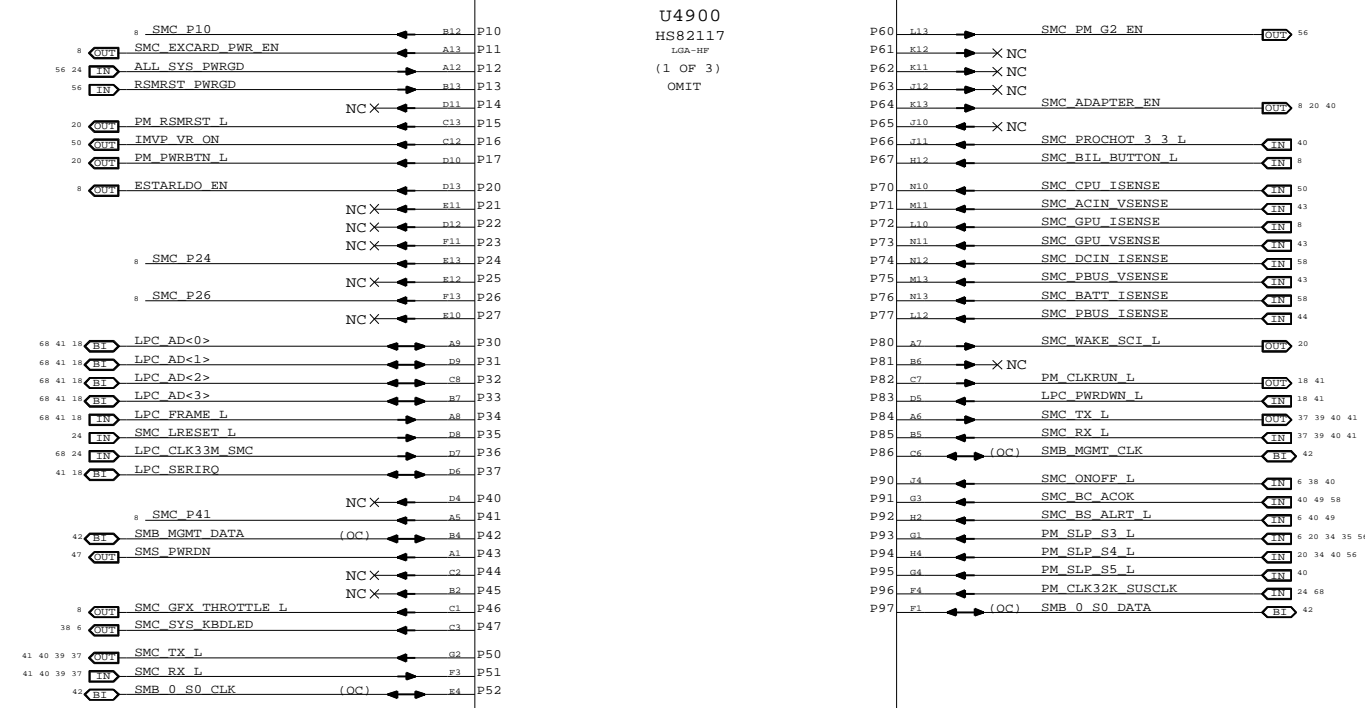
**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	38		

NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



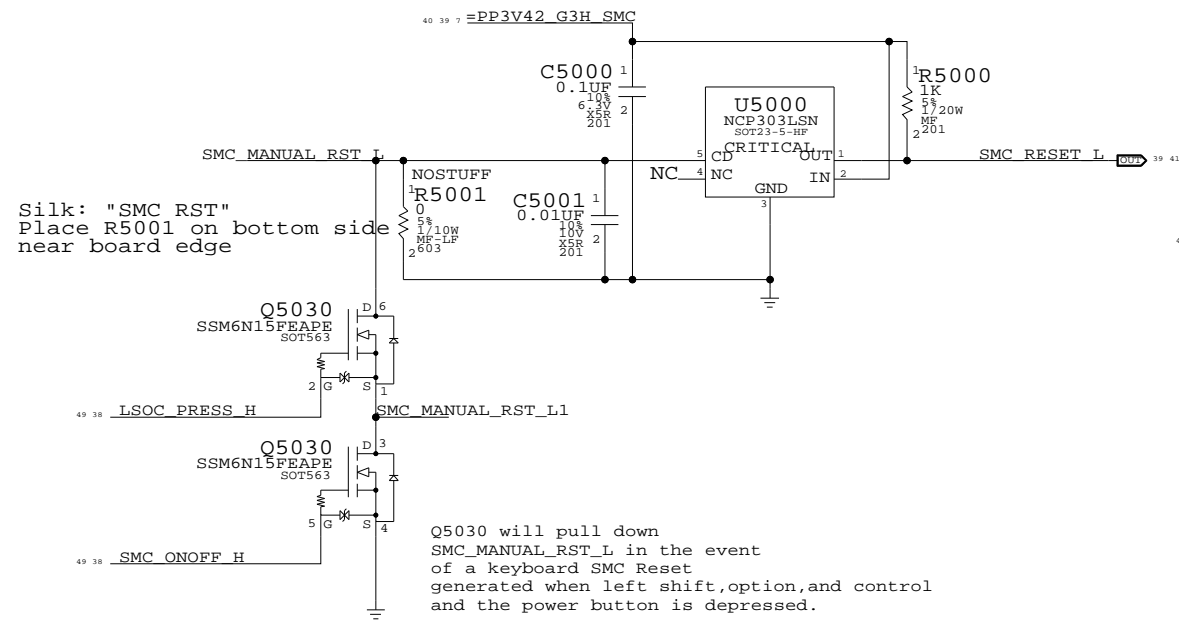
NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC  
 SYNC\_MASTER=M97 SYNC\_DATE=02/21/2008  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		39	71

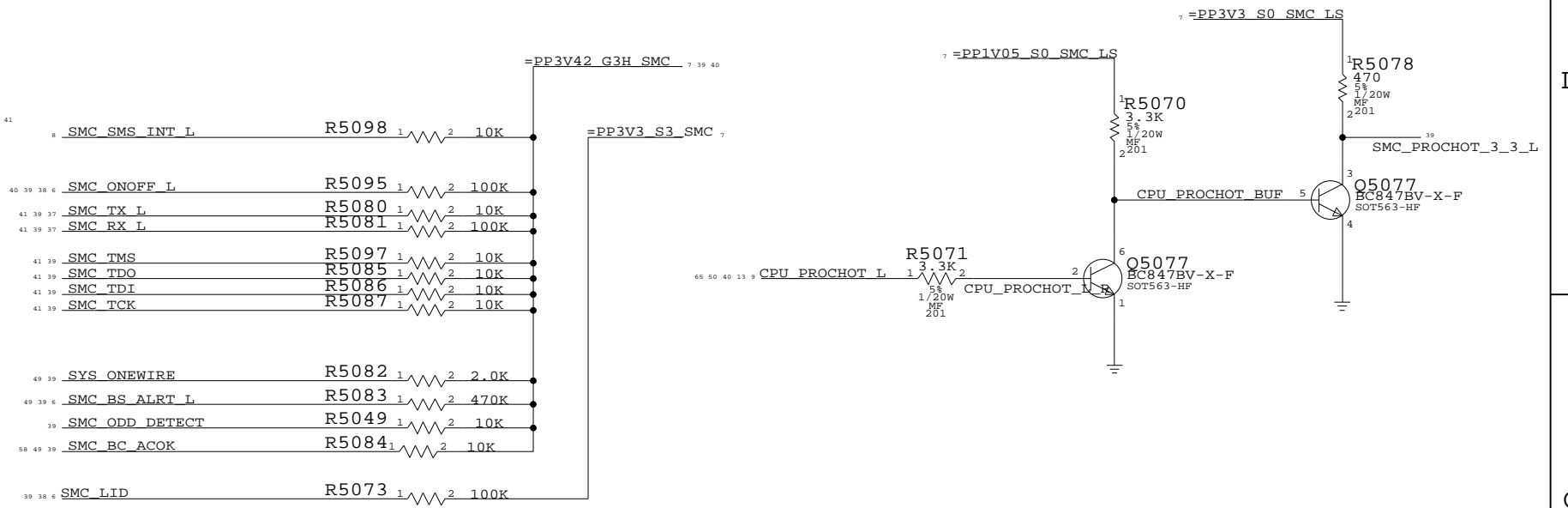
### SMC Reset Button / Brownout Detect



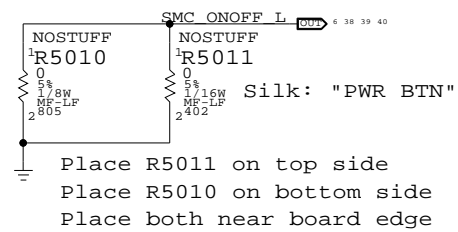
Silk: "SMC RST"  
Place R5001 on bottom side  
near board edge

Q5030 will pull down  
SMC\_MANUAL\_RST\_L in the event  
of a keyboard SMC Reset  
generated when left shift, option, and control  
and the power button is depressed.

### SMC 1.05V to 3.3V Level Shifting

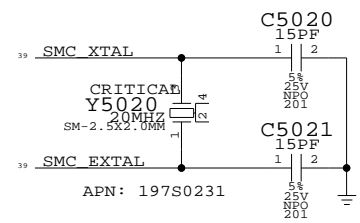


### Debug Power Button

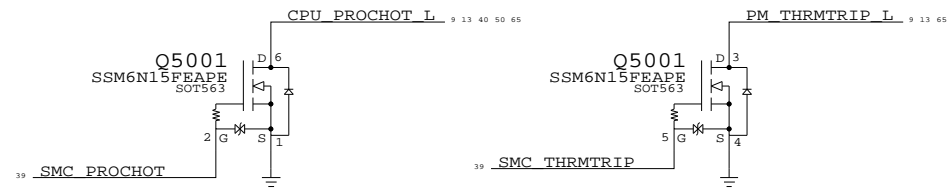


Silk: "PWR BTN"

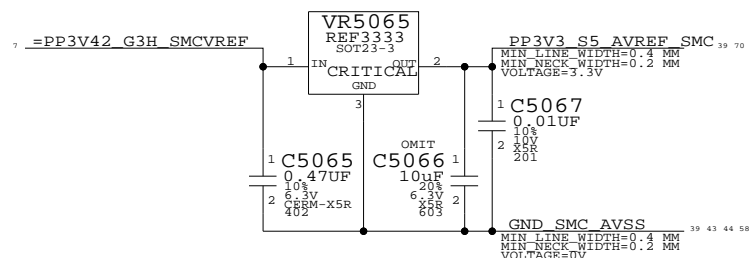
### SMC Crystal Circuit



### SMC 3.3V to 1.05V Level Shifting



### SMC AVREF Supply



**SMC SUPPORT**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		71
NONE	40		

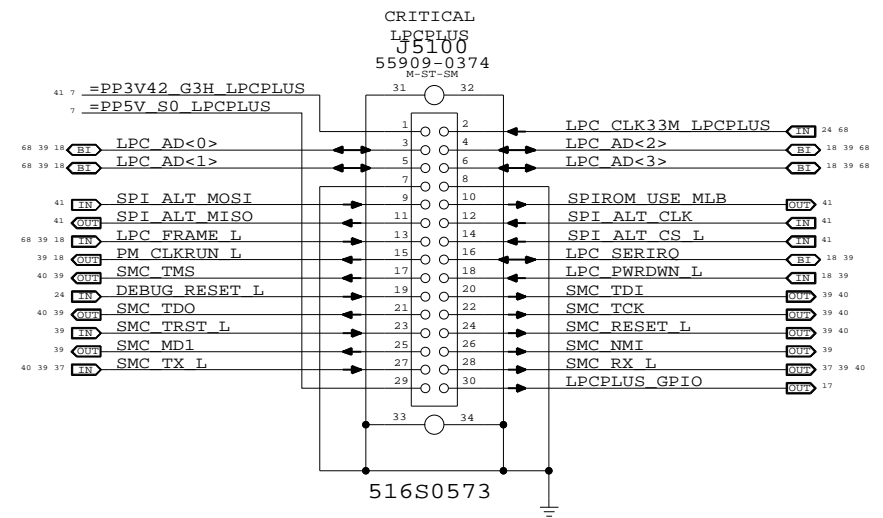


# LPC+SPI Connector

MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191  
 Any of the 4 frequencies can be selected w/ R5190,R5191,R5192,R5193

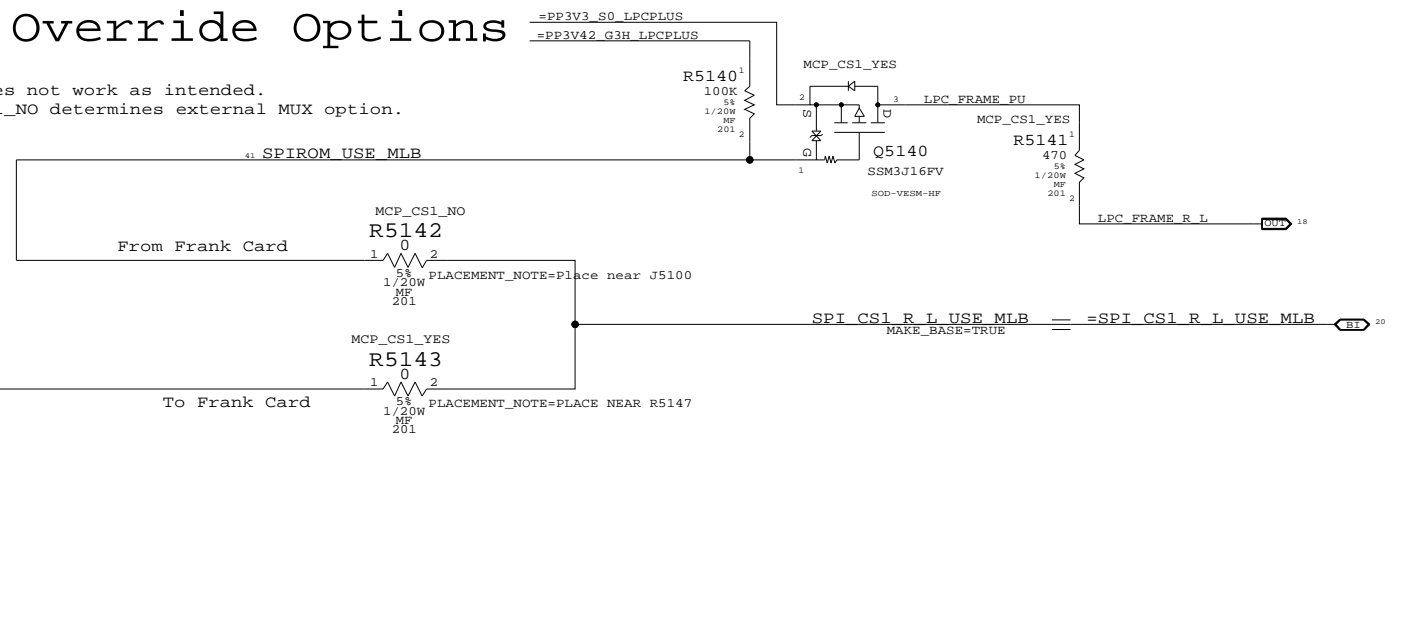
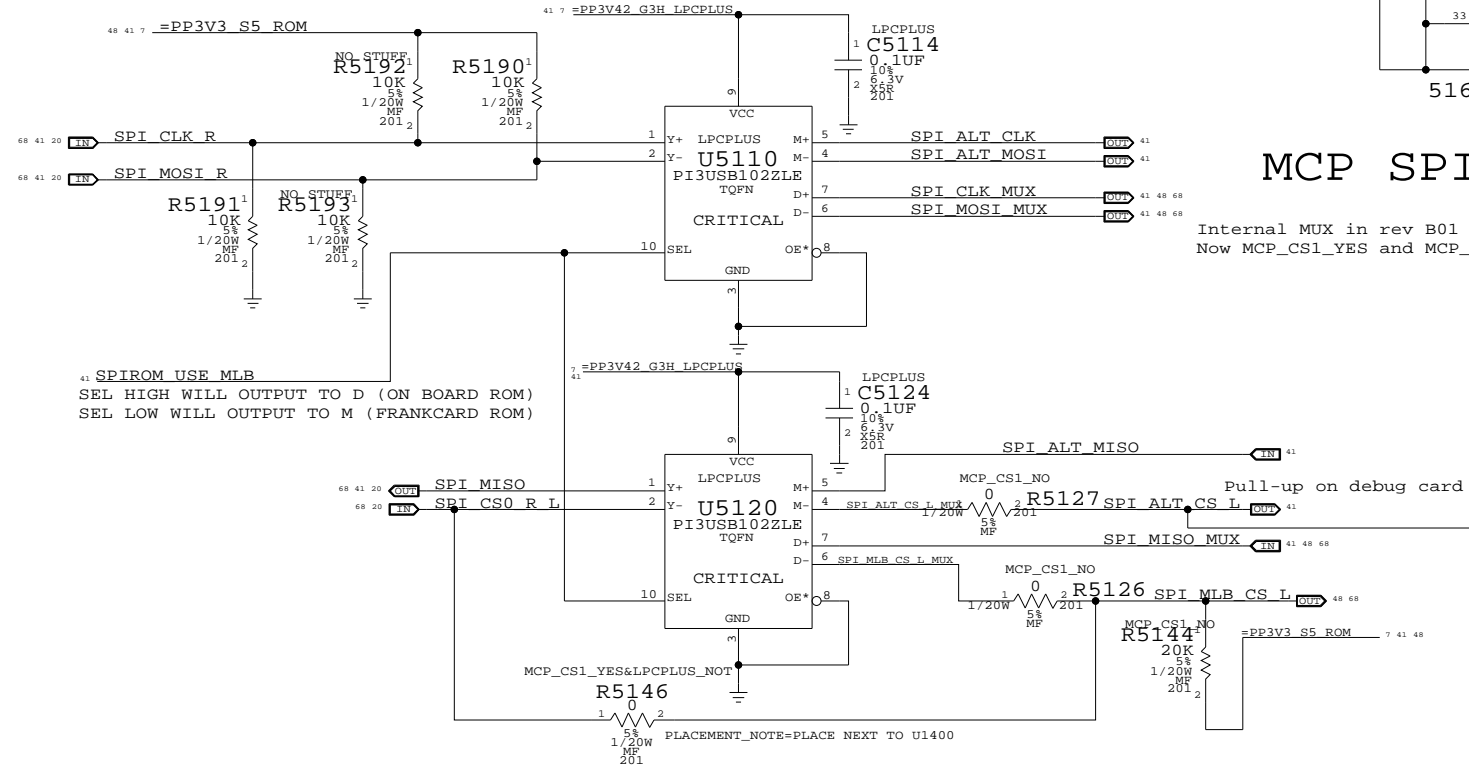


## MCP79 Internal SPI MUX Support

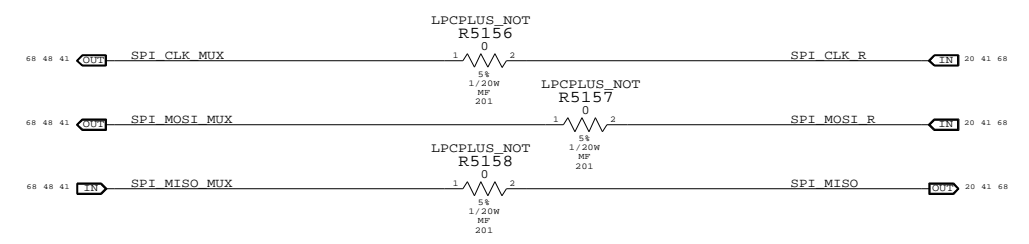
Not supported in Rev A01 MCP79 silicon

## MCP SPI Override Options

Internal MUX in rev B01 does not work as intended.  
 Now MCP\_CS1\_YES and MCP\_CS1\_NO determines external MUX option.



## SPI MUX BYPASS



**LPC+SPI Debug Connector**

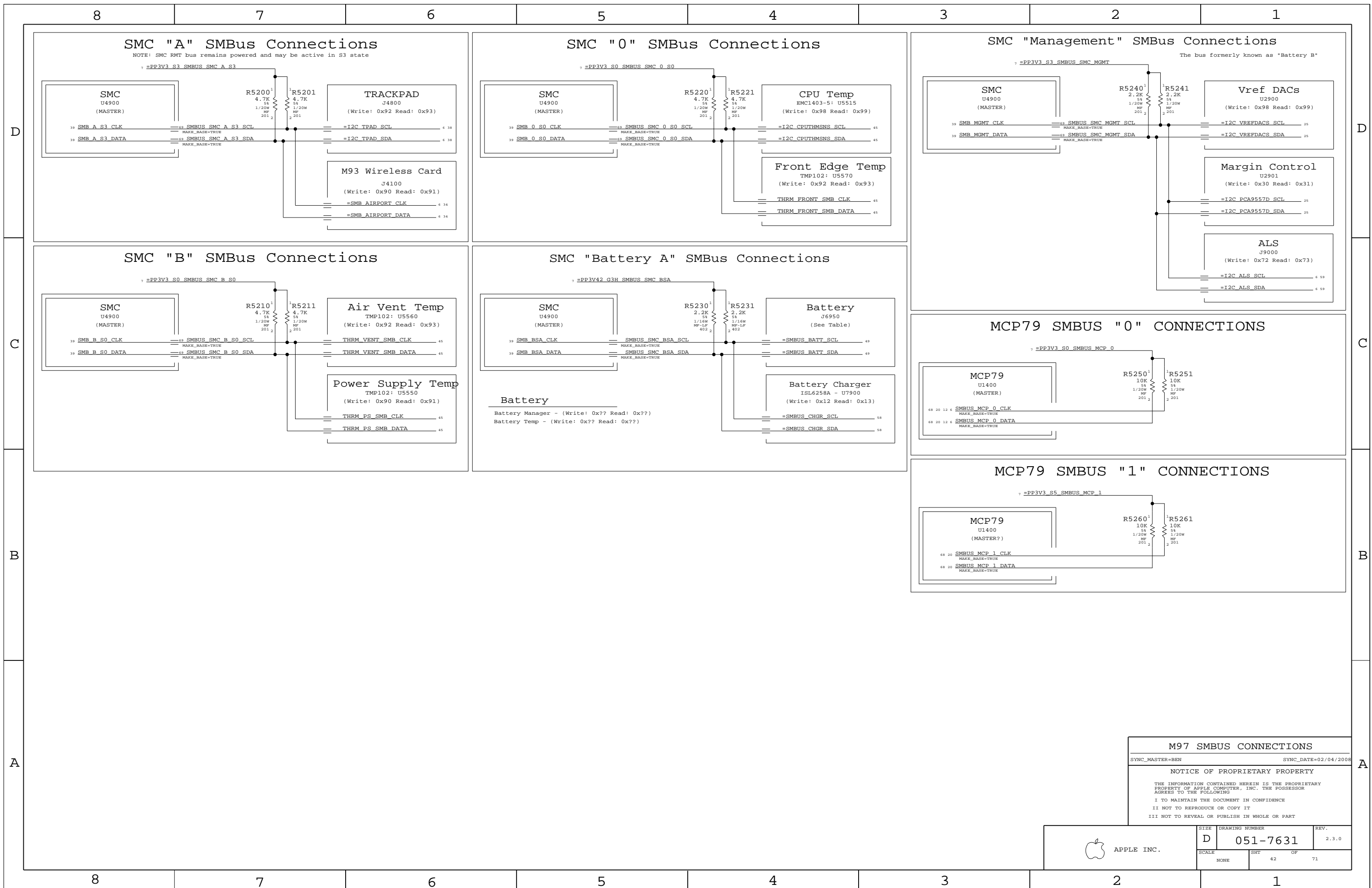
SYNC\_MASTER=CHANGZHANG SYNC\_DATE=01/24/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

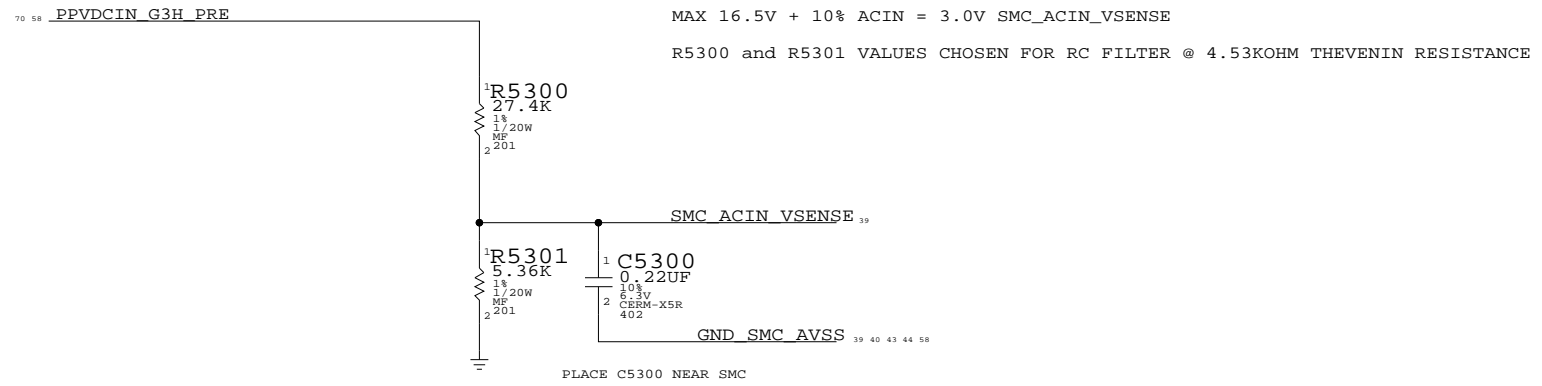
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		41	71



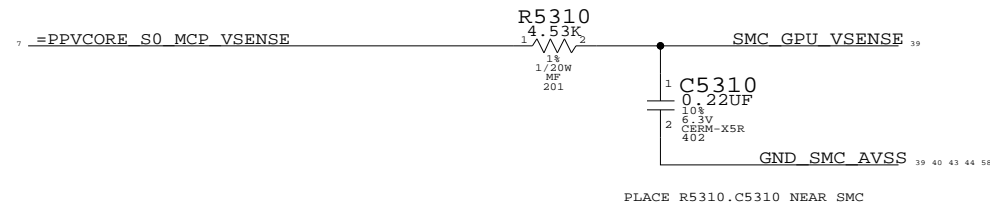
**M97 SMBUS CONNECTIONS**  
 SYNC\_MASTER=BEN SYNC\_DATE=02/04/2008  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7631</b>	REV. 2.3.0
	SCALE NONE	SHEETS 42	OF 71

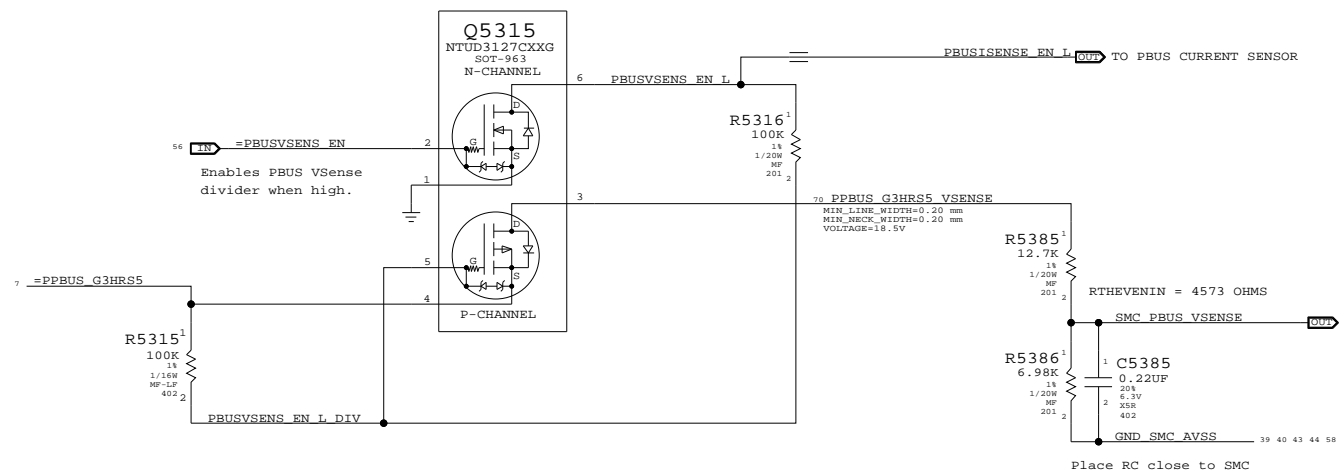
### ACIN VOLTAGE SENSE



### MCP VOLTAGE SENSE



### PBUS VOLTAGE SENSE



#### Voltage Sensors

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE DRAWING NUMBER REV.

D 051-7631 2.3.0

SCALE NONE SHEET 43 OF 71

8

7

6

5

4

3

2

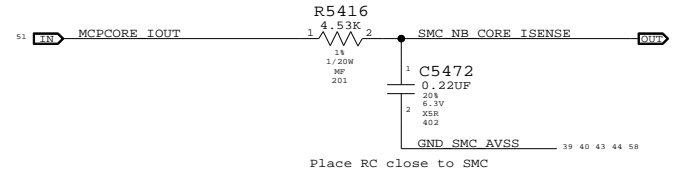
1

D

D

### MCP VCore Current Sense

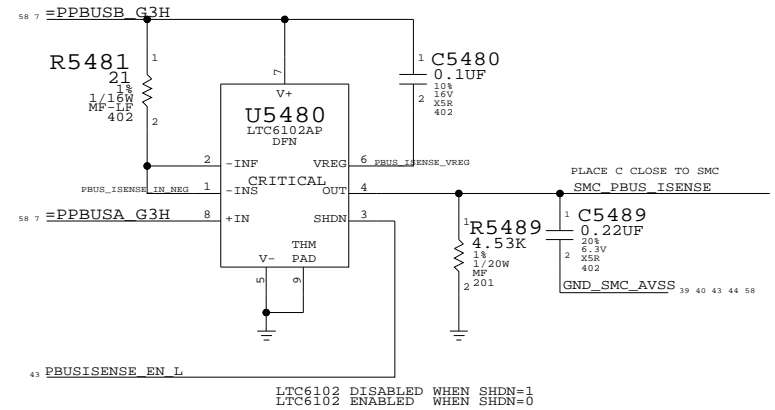
#### MCP VCore Current Sense Filter



C

C

### PBUS Current Sense



B

B

A

A

8

7

6

5

4

3

2

1

**Current Sensing**

SYNC\_MASTER=YUNWU SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

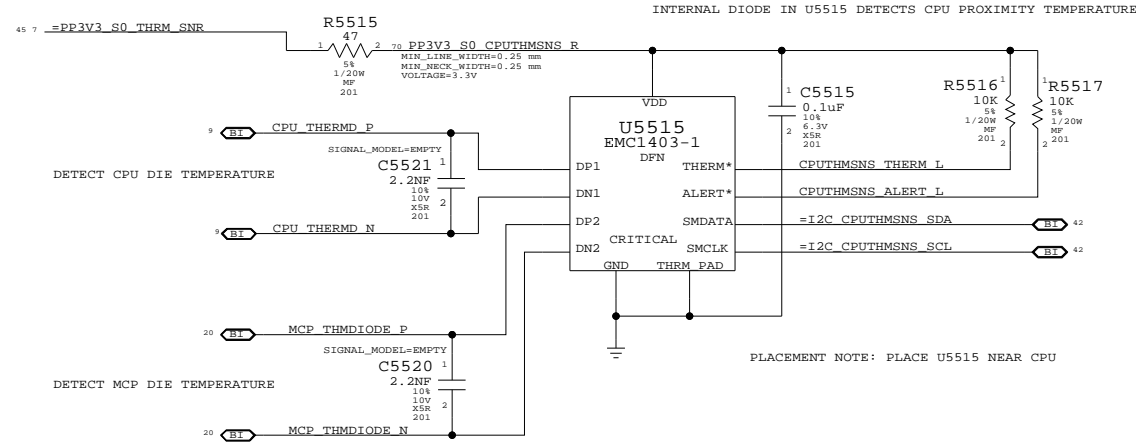
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

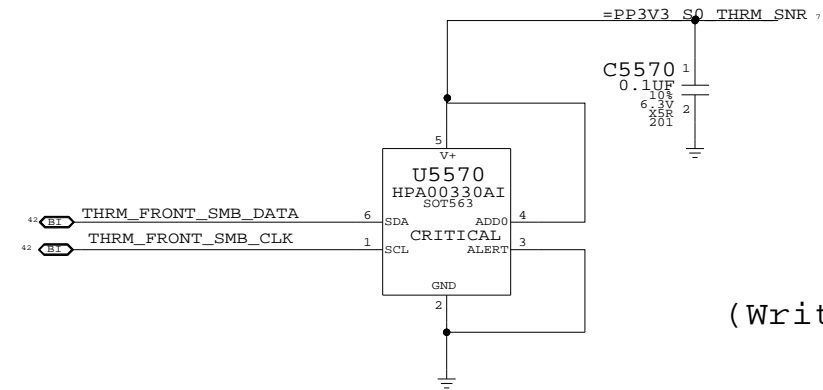
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	REV.
NONE	44	71	

# CPU/MCP T-Diode Thermal Sensor

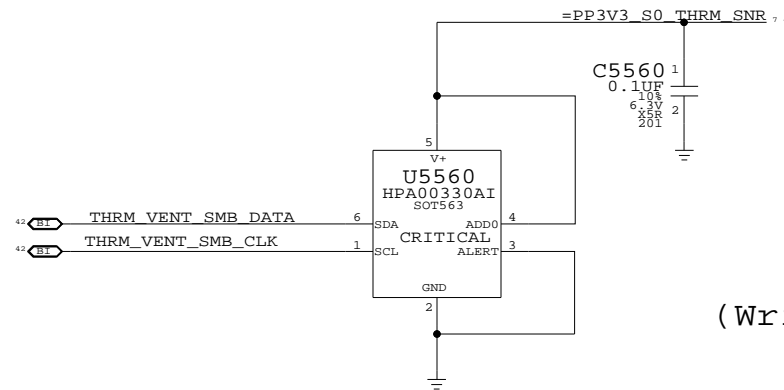


# LOCAL TEMP NEAR FRONT EDGE



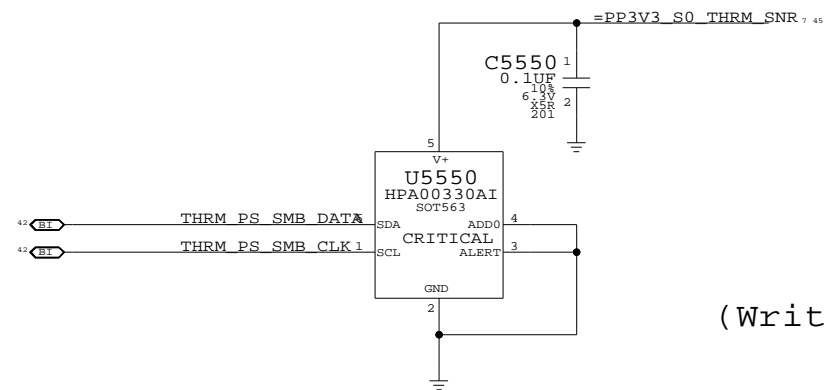
(Write: 0x92 Read: 0x93)

# LOCAL TEMP NEAR AIR VENT



(Write: 0x92 Read: 0x93)

# LOCAL TEMP NEAR POWER SUPPLIES



(Write: 0x90 Read: 0x91)

## TEMPERATURE SENSORS

SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



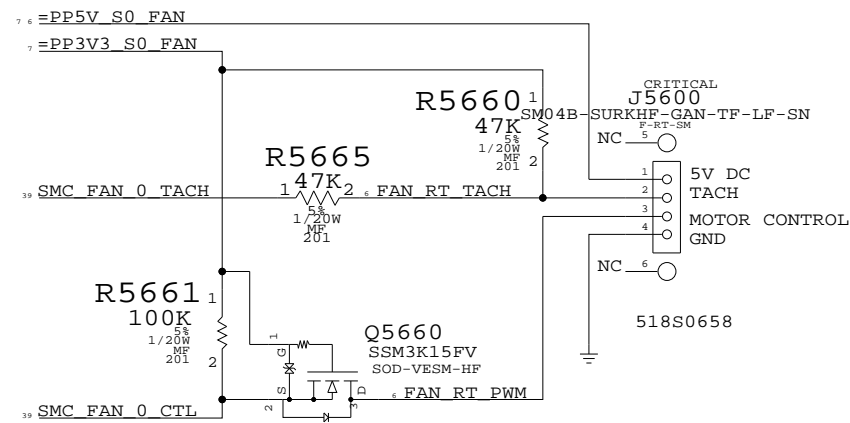
APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7631 2.3.0

SCALE NONE SHEET 45 OF 71

# FAN CONNECTOR



**Fan**  
 SYNC\_MASTER=M70      SYNC\_DATE=01/09/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		
NONE	46	71	

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

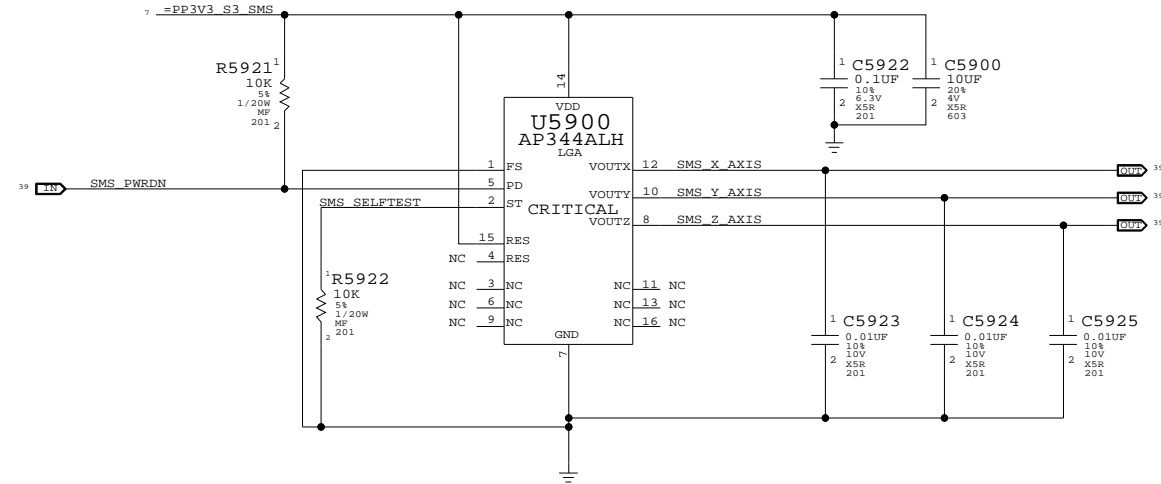
4

3

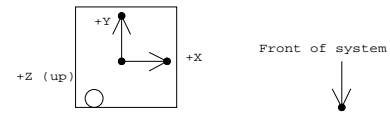
2

1

# SUDDEN MOTION SENSOR



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

## Sudden Motion Sensor (SMS)

SYNC\_MASTER=076\_MLB SYNC\_DATE=01/12/2007

### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

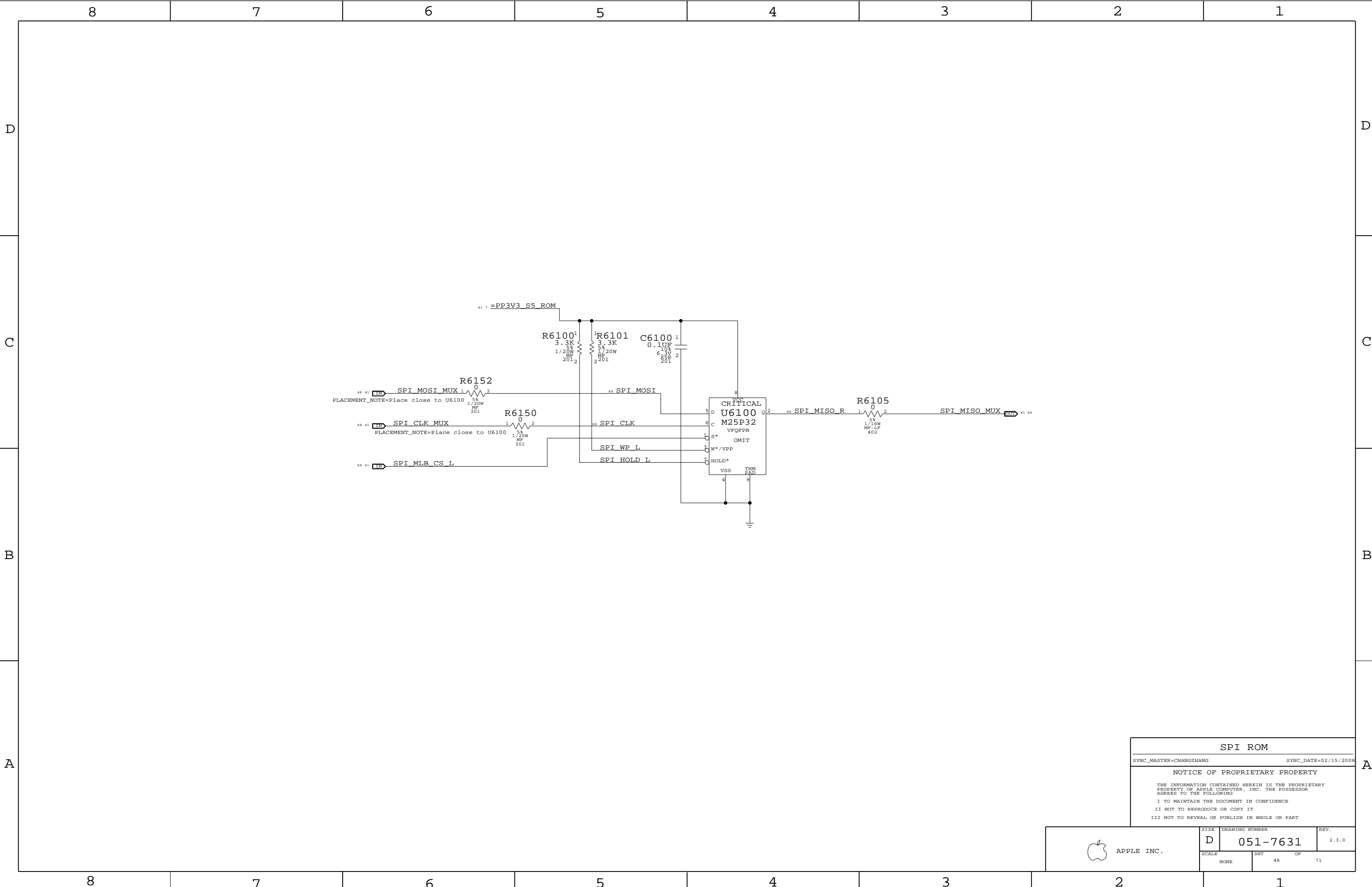
- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE DRAWING NUMBER REV.

D 051-7631 2.3.0

SCALE NONE SH1 OF 71



**SPI ROM**

SYNC\_MASTER=CHANGZHANG      SYNC\_DATE=02/15/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

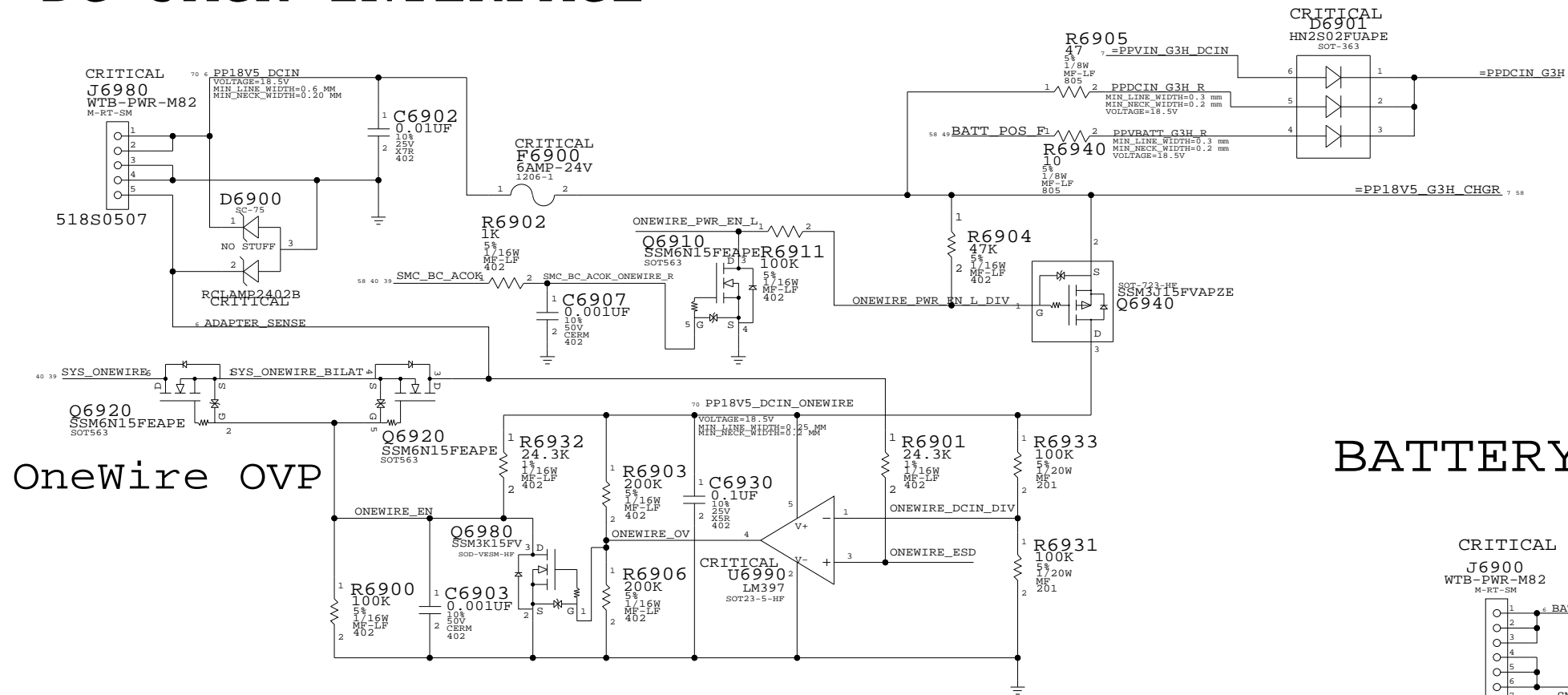
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	
NONE	48	71	

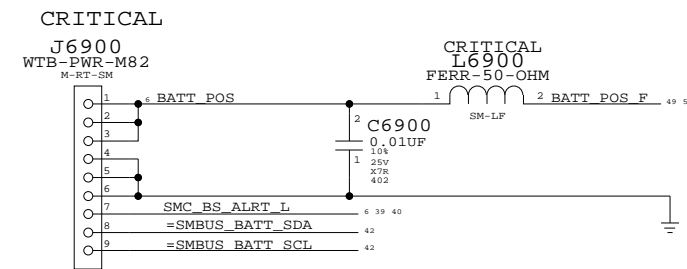


# DC-JACK INTERFACE



## OneWire OVP

# BATTERY INTERFACE

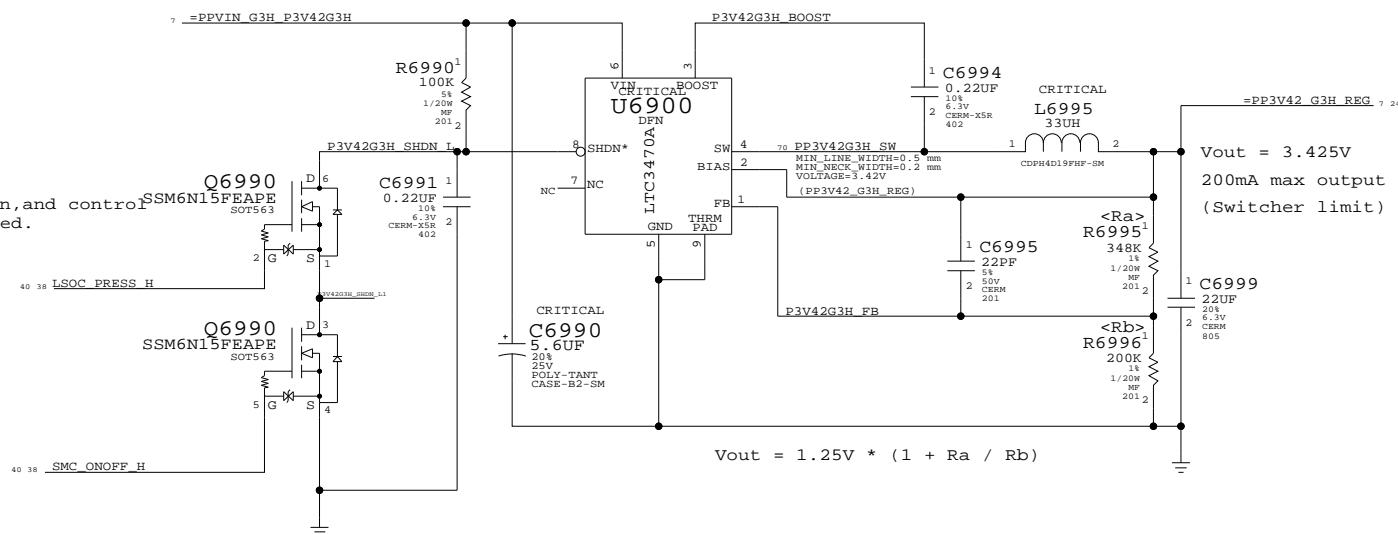


518S0540

## 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

Q6990 will pull down P3V42G3H\_SHDN\_L in the event of a keyboard SMC Reset generated when left shift, option, and control and the power button is depressed.



DC-In & Battery Connectors  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007

NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	49	71

# IMVP6 CPU VCore REGULATOR

8 7 6 5 4 3 2 1

D

D

C

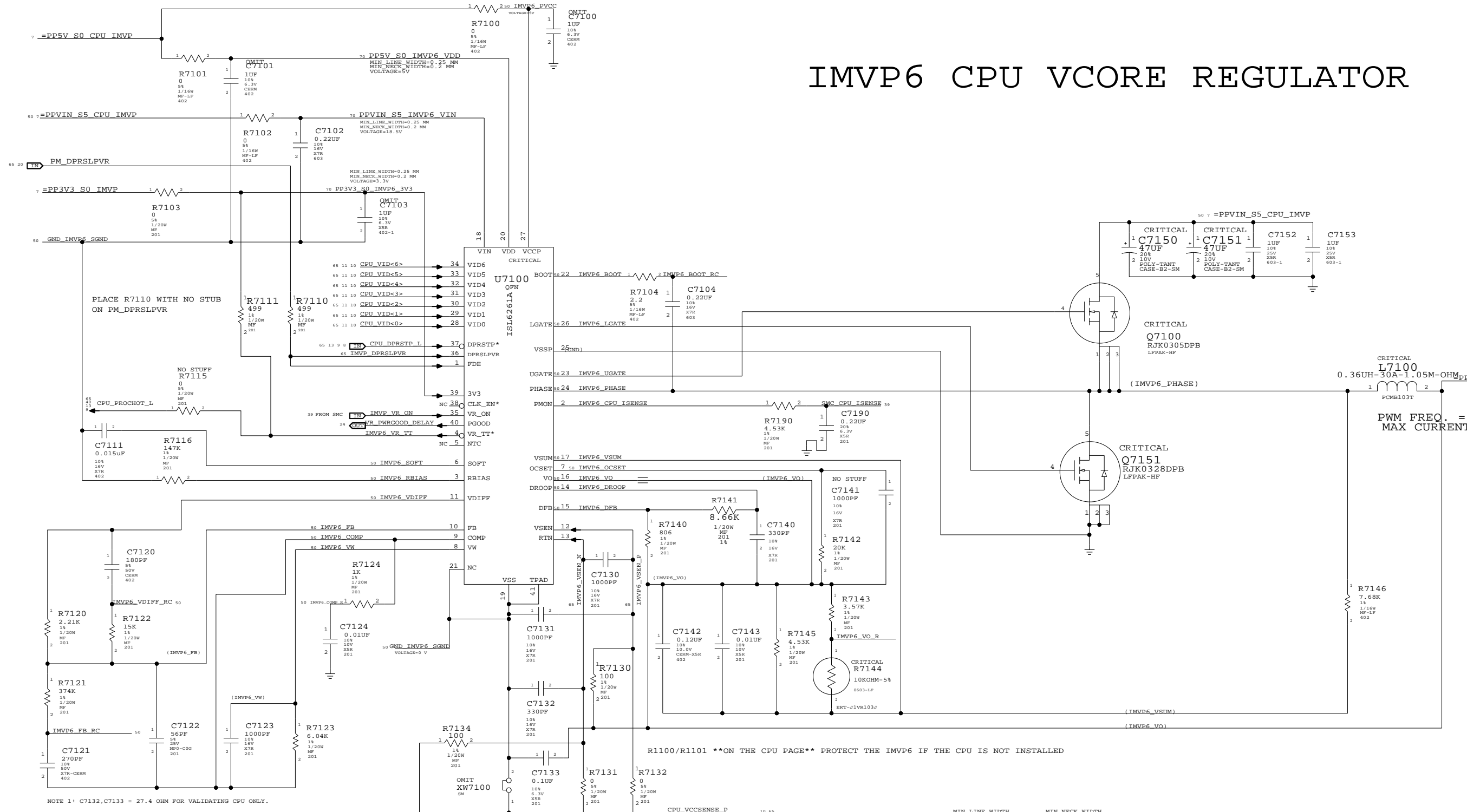
C

B

B

A

A



NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
50 IMVP6_PHASE	1.5 MM	0.20 MM
50 IMVP6_BOOT	0.25 MM	0.20 MM
50 IMVP6_UGATE	1.5 MM	0.20 MM
50 IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
50 IMVP6_OCSET	0.25 MM	0.20 MM
50 IMVP6_VSUM	0.25 MM	0.20 MM
50 GND_IMVP6_SGND	0.50 MM	0.20 MM
50 IMVP6_VO	0.25 MM	0.20 MM
50 IMVP6_DROOP	0.25 MM	0.20 MM
50 IMVP6_DFBS	0.25 MM	0.20 MM
50 IMVP6_SOFT	0.25 MM	0.20 MM
50 IMVP6_RBIAS	0.25 MM	0.20 MM
50 IMVP6_VDIFF	0.25 MM	0.20 MM
50 IMVP6_FB	0.25 MM	0.20 MM
50 IMVP6_COMP	0.25 MM	0.20 MM
50 IMVP6_VW	0.25 MM	0.20 MM
50 IMVP6_PVCC	0.25 MM	0.20 MM
50 IMVP6_COMP_R	0.25 MM	0.20 MM
50 IMVP6_FB_RC	0.25 MM	0.20 MM
50 IMVP6_VDIFF_RC	0.25 MM	0.20 MM

## IMVP6 CPU VCore Regulator

SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

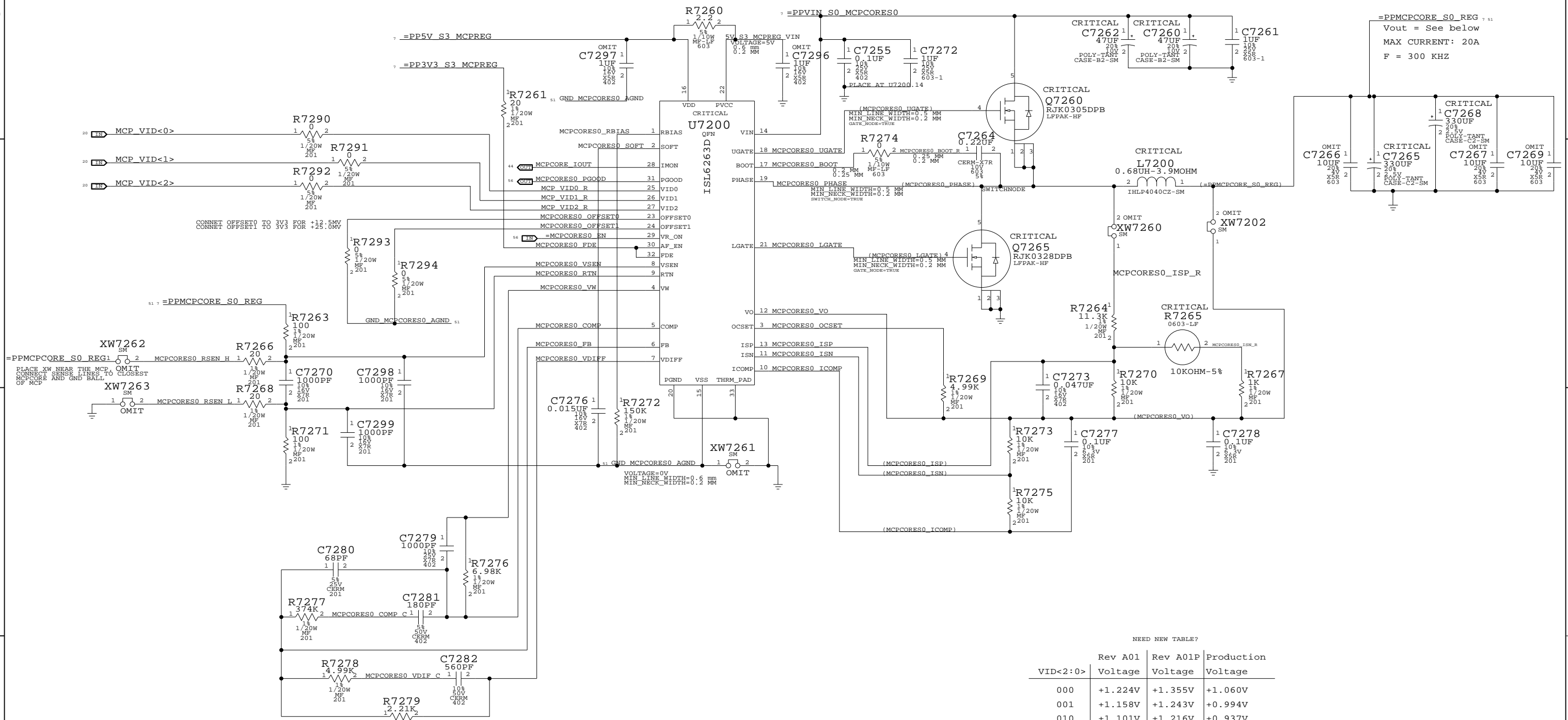
### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		50	71

8 7 6 5 4 3 2 1

# MCP CORE POWER SUPPLY



NEED NEW TABLE?

VID<2:0>	Rev A01 Voltage	Rev A01P Voltage	Production Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

**MCP CORE REGULATOR**

SYNC\_MASTER=MINGJING      SYNC\_DATE=06/24/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

8 7 6 5 4 3 2 1

D

D

C

C

B

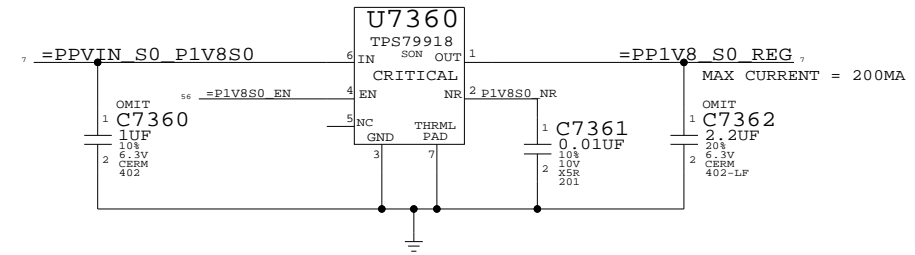
B

A

A

8 7 6 5 4 3 2 1

# 1.8V S0 LDO

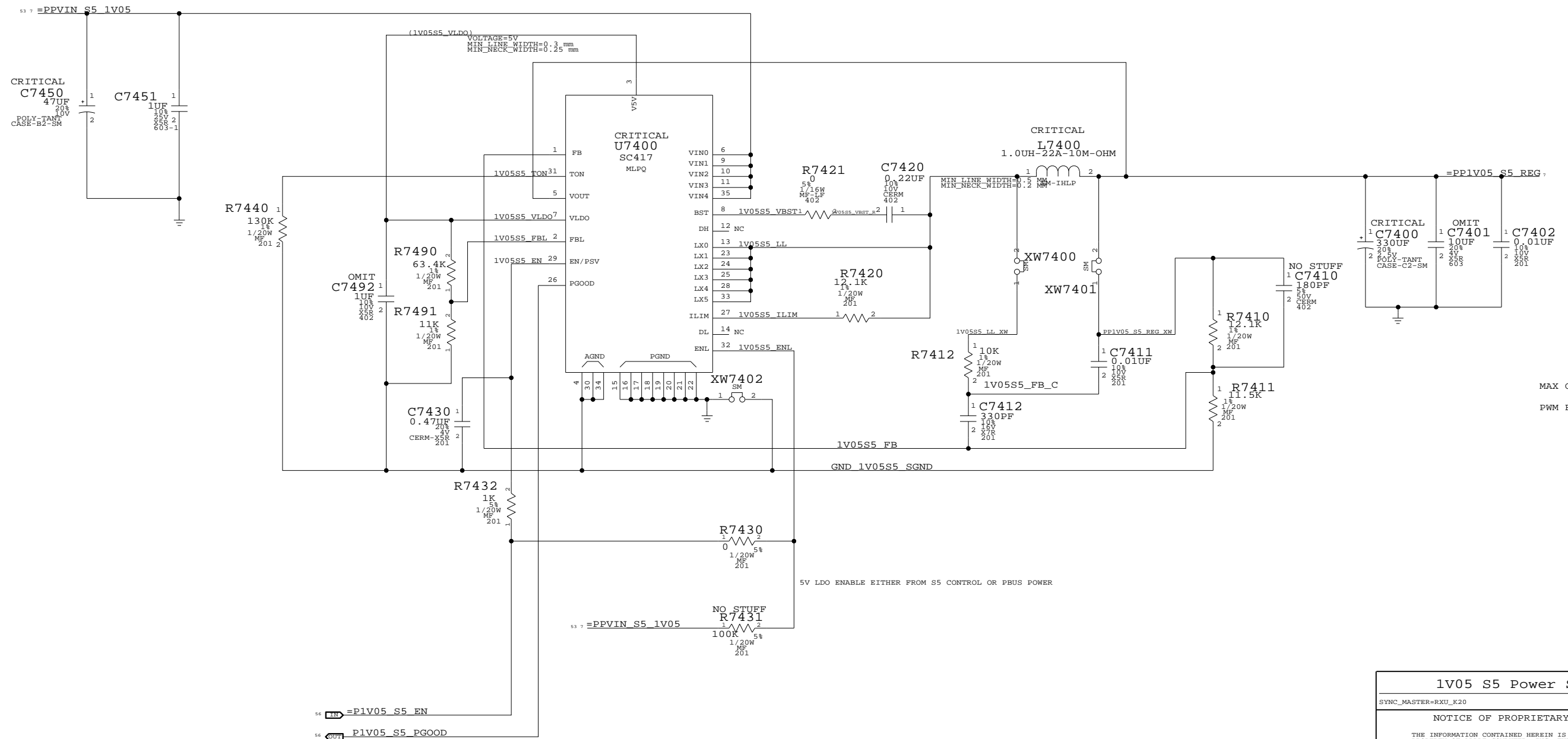


1.8V LDO Supply  
 SYNC\_MASTER= SYNC\_DATE=  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		
NONE	52 OF 71		

# 1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0



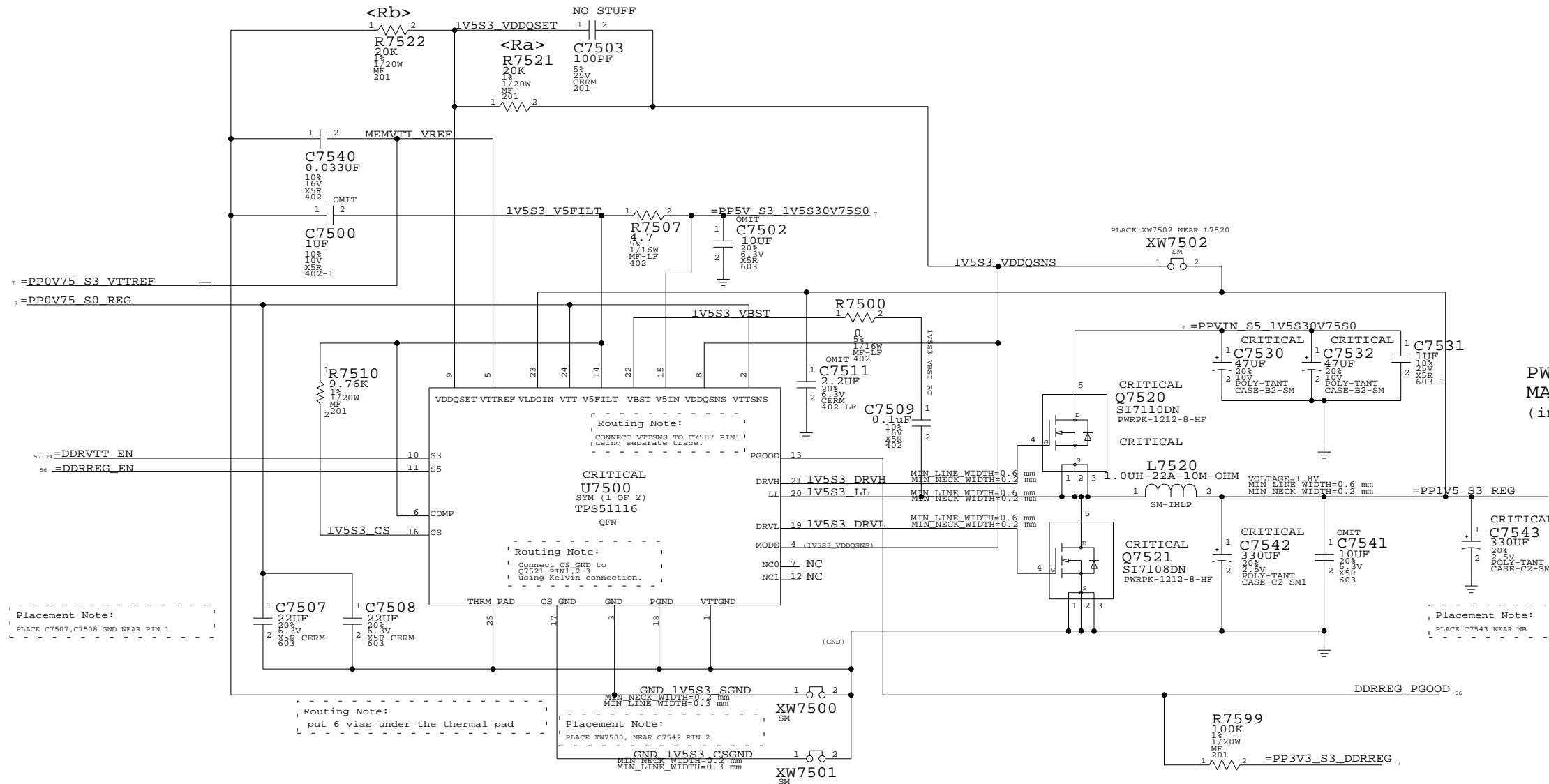
1V05 S5 Power Supply  
 SYNC\_MASTER=RXU\_K20 SYNC\_DATE=05/21/2008  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		53	71

# 1.5V/0.75V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_I	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V

$$V_{out} = 0.75V * (1 + R_a / R_b)$$

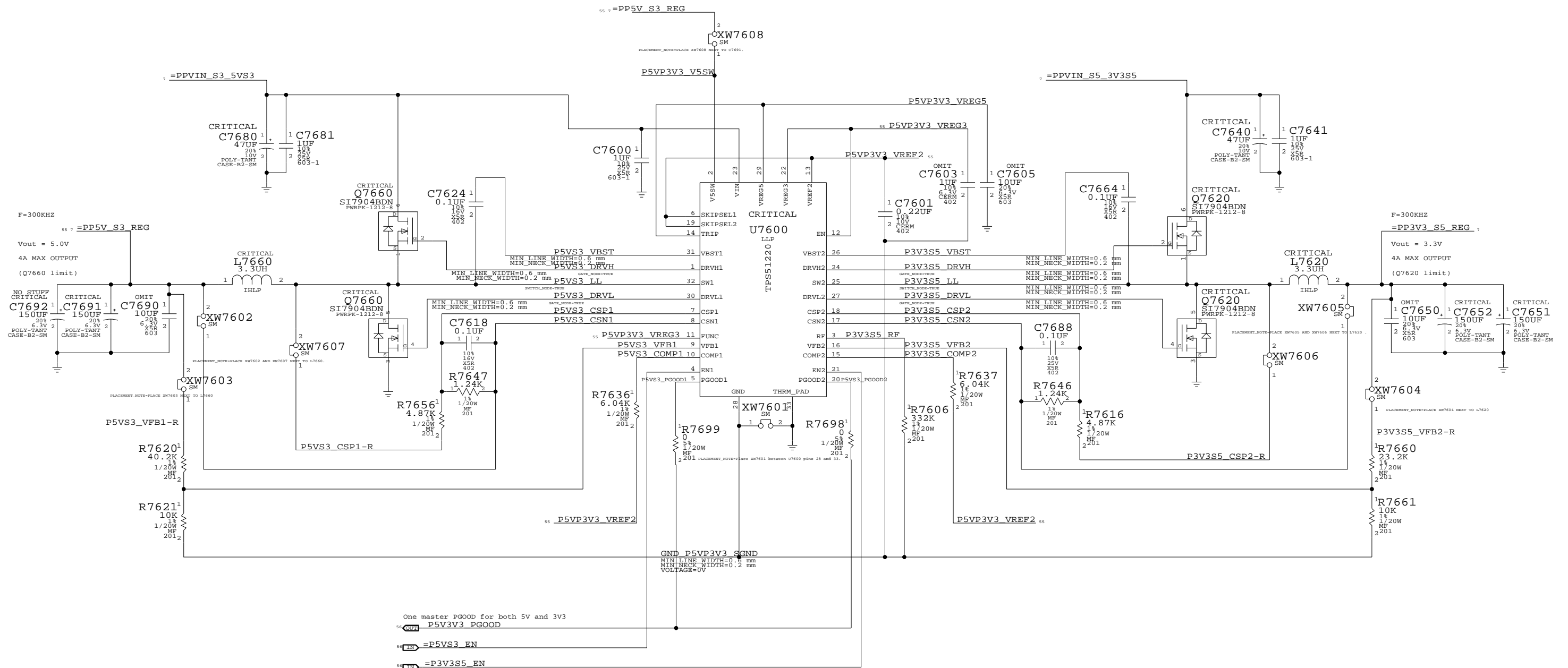


PWM FREQ. = 400 kHz  
MAX CURRENT = 11A  
(inductor limited)

**1.5V/0.75V Supplies**  
 SYNC\_MASTER=M70      SYNC\_DATE=01/09/2007  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	54		

# 5V\_S3 / 3V3\_S5 POWER SUPPLY



5V / 3.3V Power Supply

SYNC\_MASTER=RXU\_K20 SYNC\_DATE=05/21/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

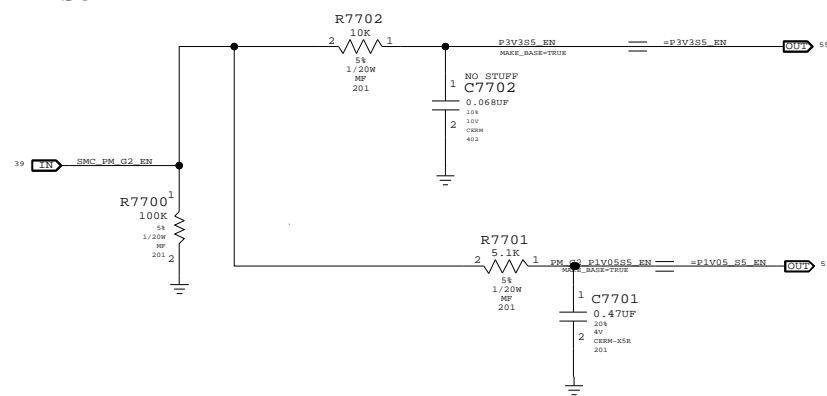
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

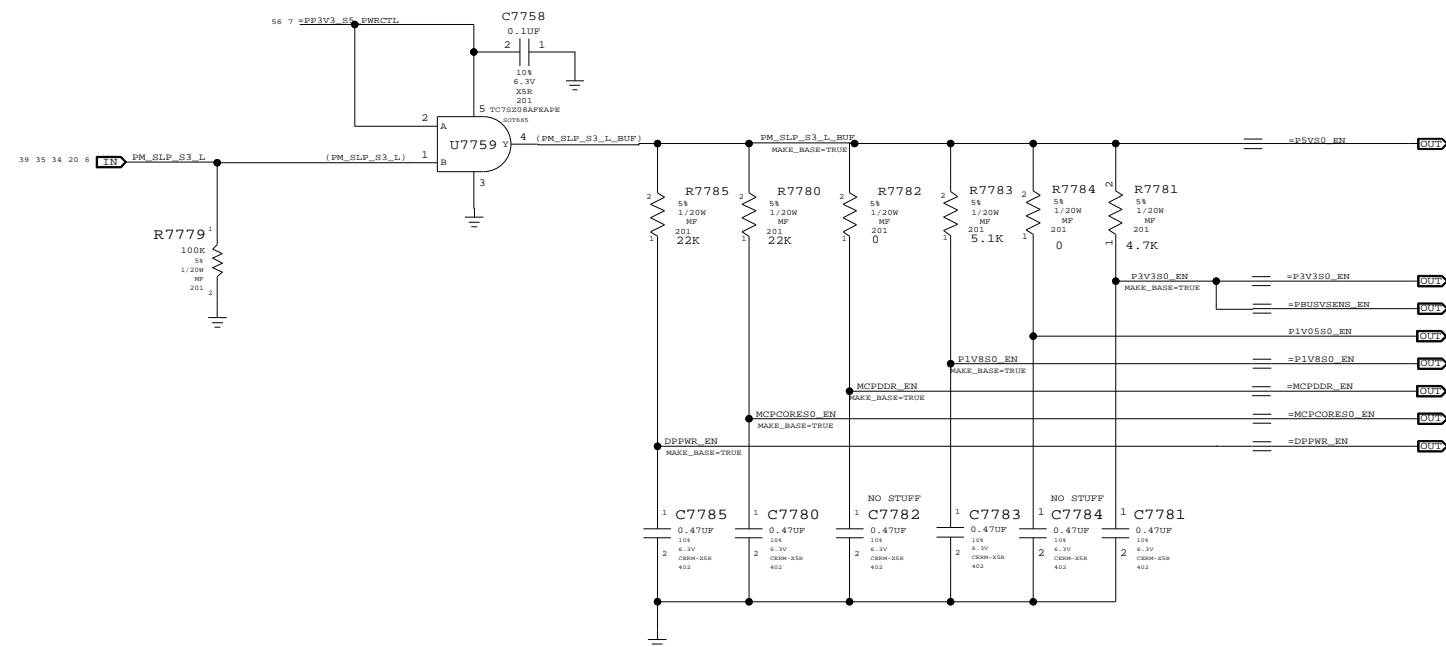
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		55	71

# Power Control Signals

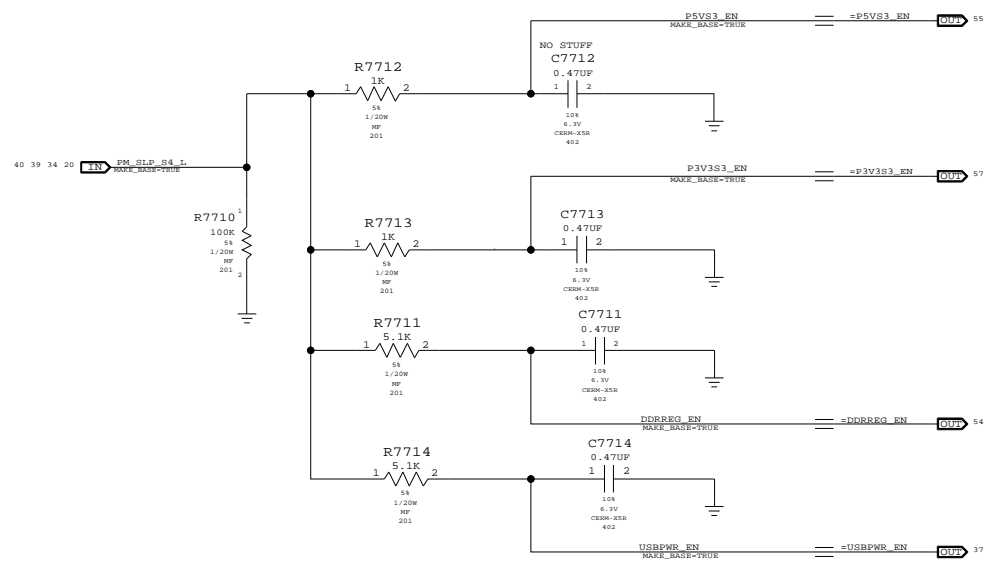
## S5 ENABLE



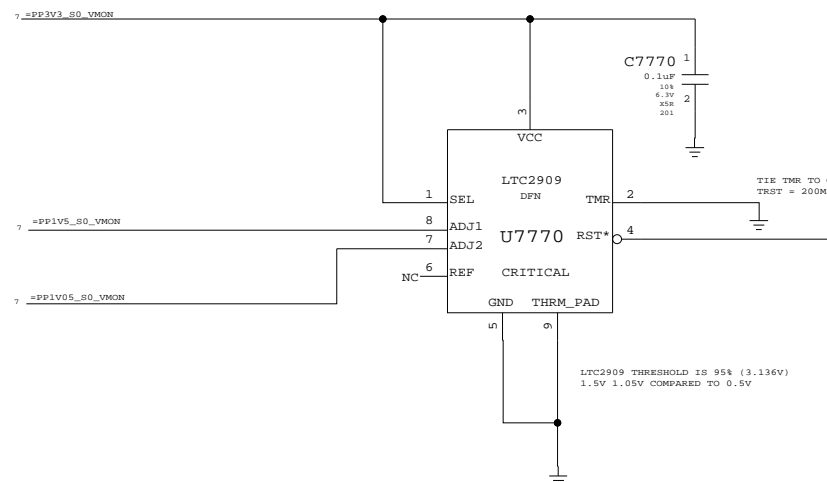
## S0 ENABLE



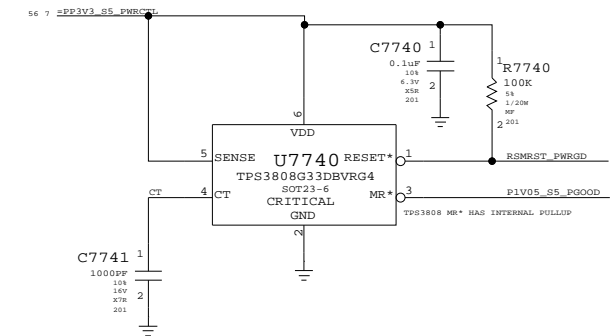
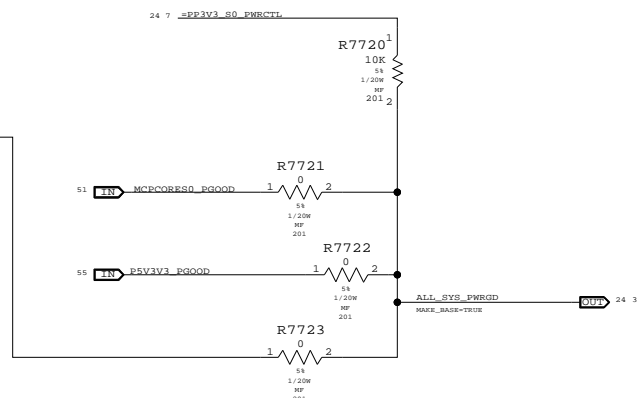
## S3 ENABLE



## 3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



## OTHER S0 RAILS PGOOD



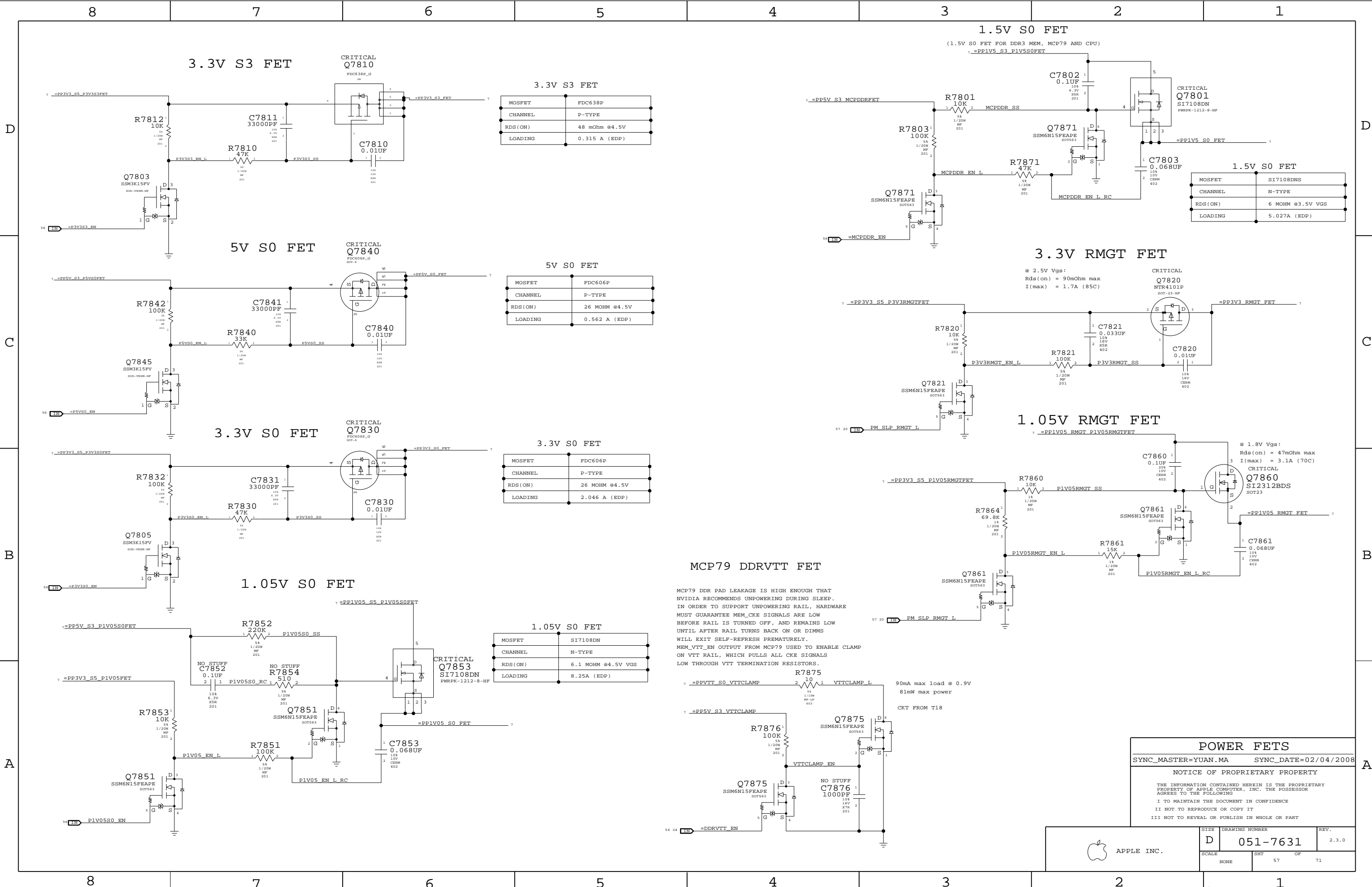
Unused PGOOD signal

TP\_DDRREG\_PGOOD  
MAKE\_BASE-TRUE

POWER SEQUENCING		
SYNC_MASTER=YUAN.MA	SYNC_DATE=02/04/2008	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING		
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE		
II NOT TO REPRODUCE OR COPY IT		
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		56	71





**3.3V S3 FET**

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.315 A (EDP)

**5V S0 FET**

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	0.562 A (EDP)

**3.3V S0 FET**

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	2.046 A (EDP)

**1.05V S0 FET**

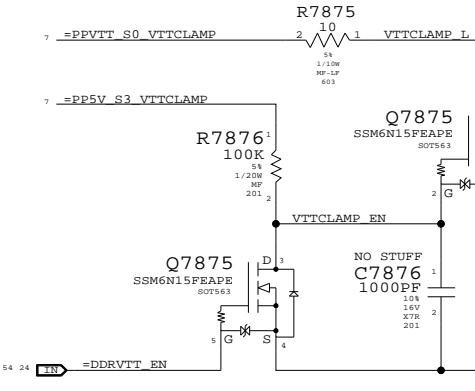
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6.1 MOHM @4.5V VGS
LOADING	8.25A (EDP)

**1.5V S0 FET**

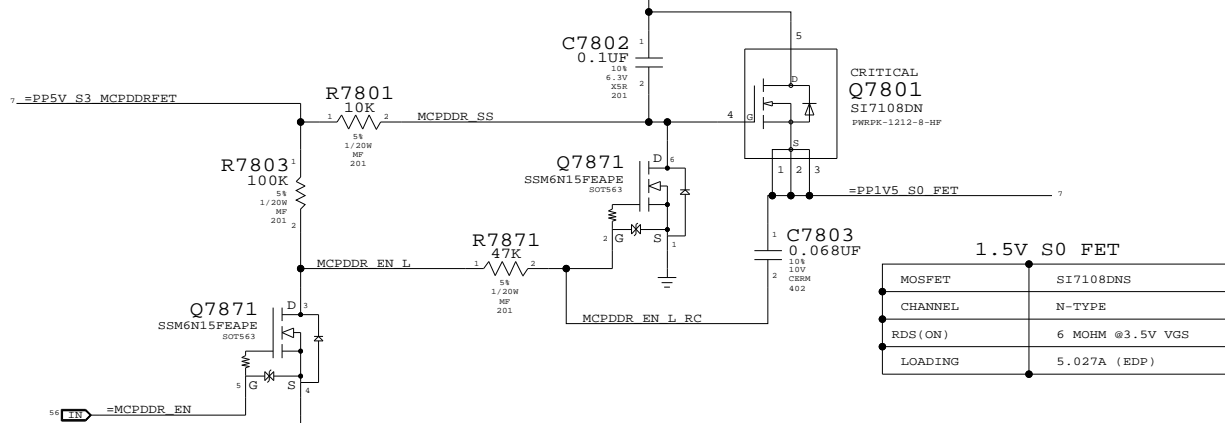
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5.027A (EDP)

**MCP79 DDRVTT FET**

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM\_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM\_VTT\_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



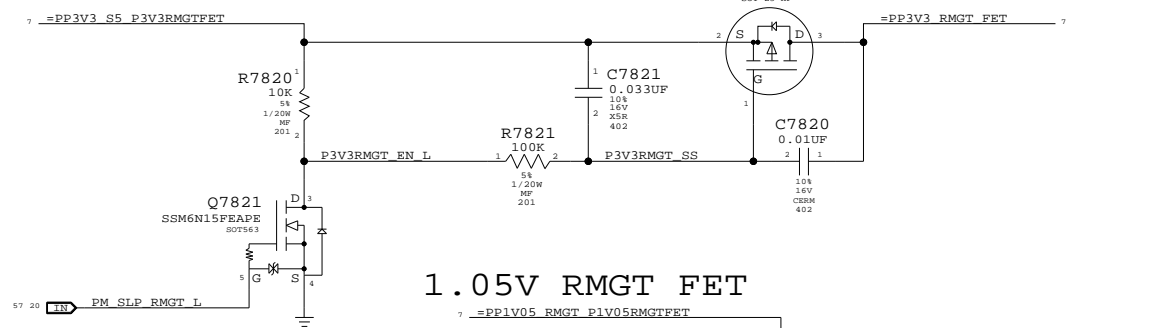
**1.5V S0 FET**  
(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)  
=PP1V5\_S3\_P1V5S0FET



**3.3V RMGT FET**

@ 2.5V Vgs:  
Rds(on) = 90mOhm max  
I(max) = 1.7A (85C)

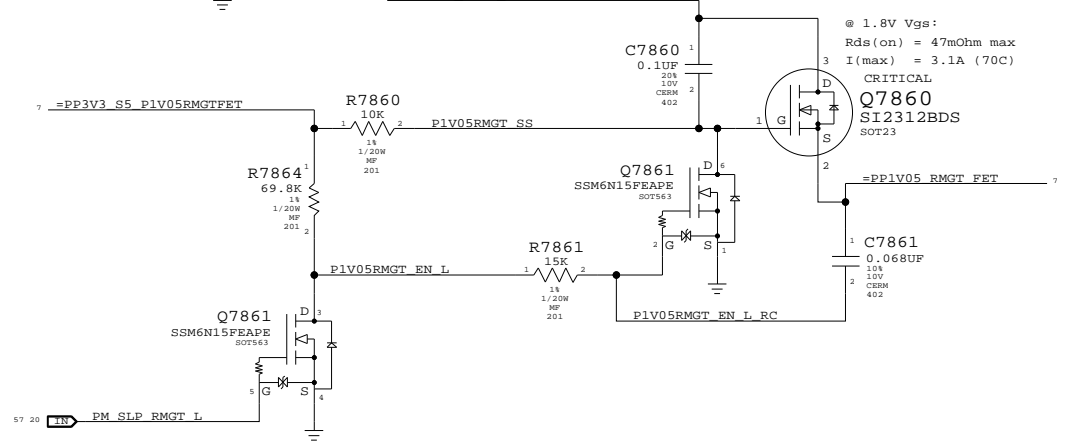
**CRITICAL Q7820**  
NTR4101P  
SOT-23-8F



**1.05V RMGT FET**

@ 1.8V Vgs:  
Rds(on) = 47mOhm max  
I(max) = 3.1A (70C)

**CRITICAL Q7860**  
SI2312BDS  
SOT23



**POWER FETS**

SYNC\_MASTER=YUAN.MA SYNC\_DATE=02/04/2008

NOTICE OF PROPRIETARY PROPERTY

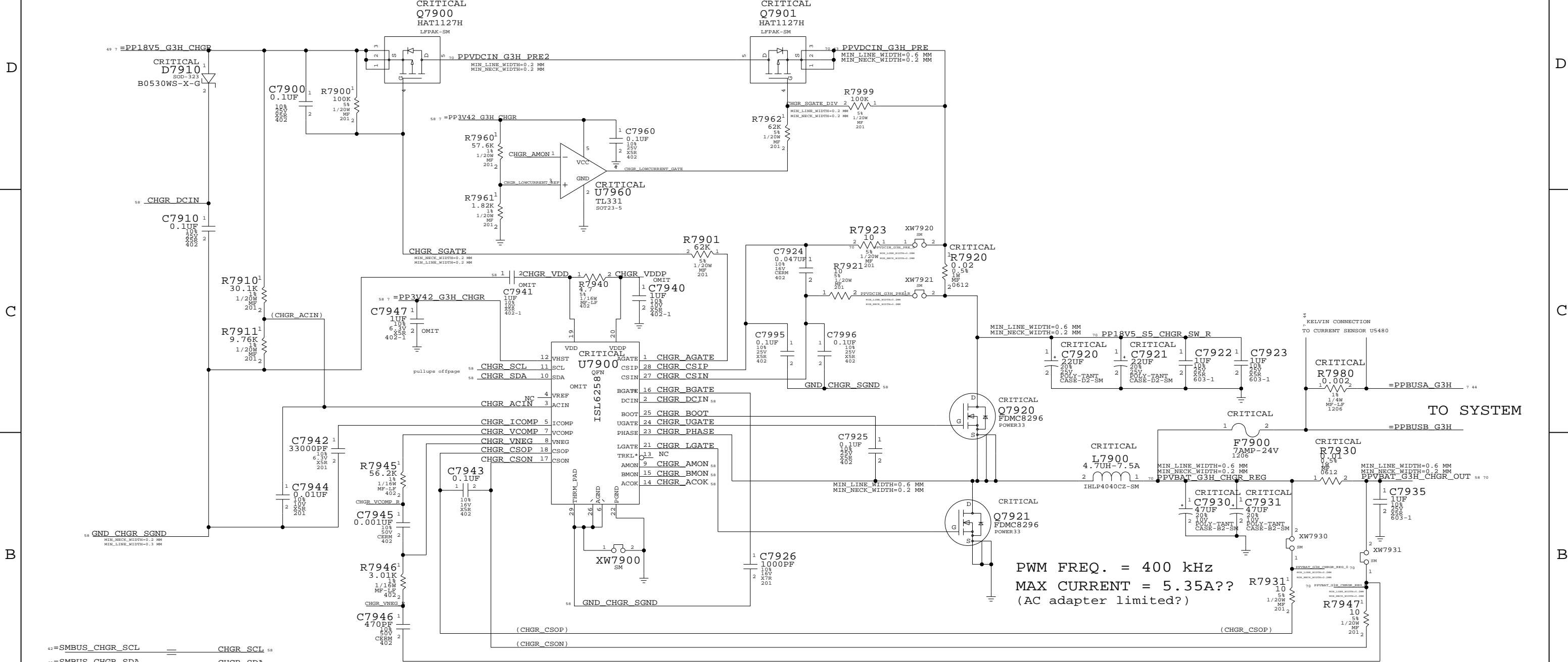
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

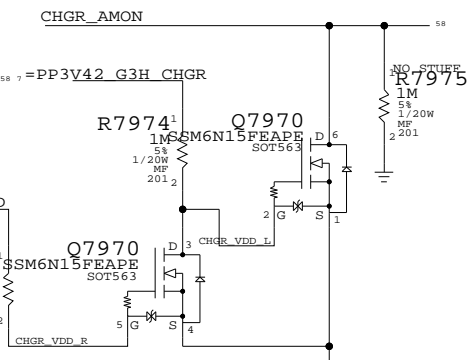
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

# PBUS SUPPLY / BATTERY CHARGER

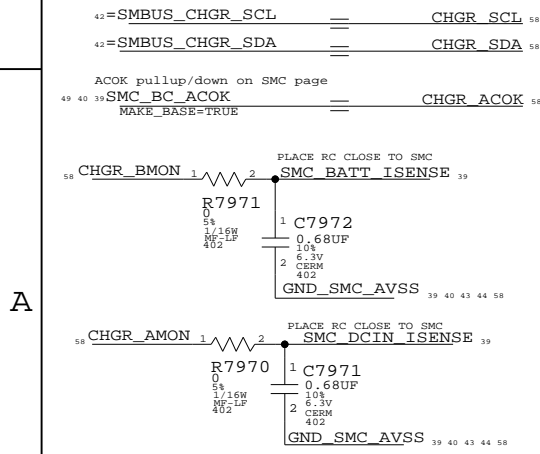
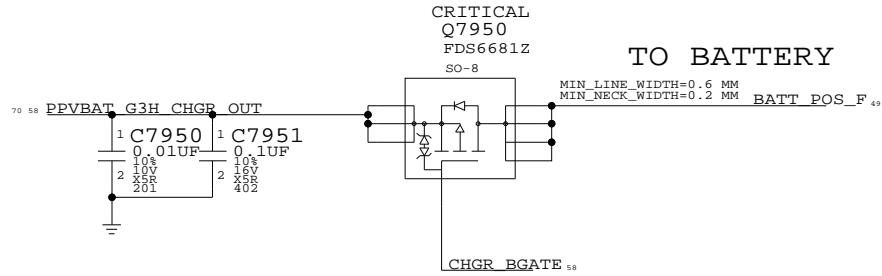


PWM FREQ. = 400 kHz  
 MAX CURRENT = 5.35A??  
 (AC adapter limited?)

## AMON PULLDOWN LOGIC

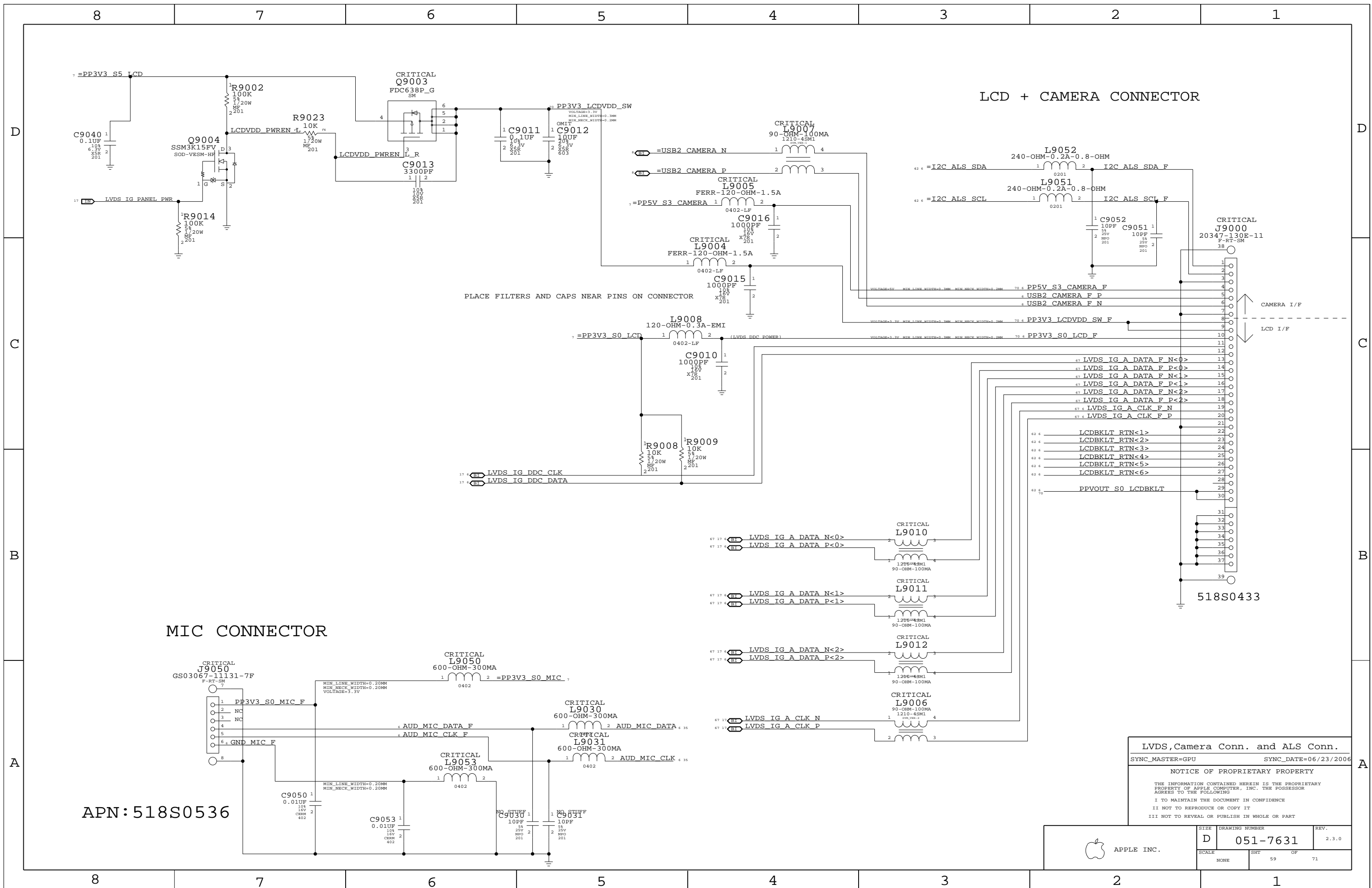


## BATTERY CHARGING



**PBUS Supply/Battery Charger**  
 SYNC\_MASTER=M70 SYNC\_DATE=01/09/2007  
**NOTICE OF PROPRIETARY PROPERTY**  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHEET	OF	71
NONE	58		



LVDS, Camera Conn. and ALS Conn.

SYNC\_MASTER=GPU SYNC\_DATE=06/23/2006

NOTICE OF PROPRIETARY PROPERTY

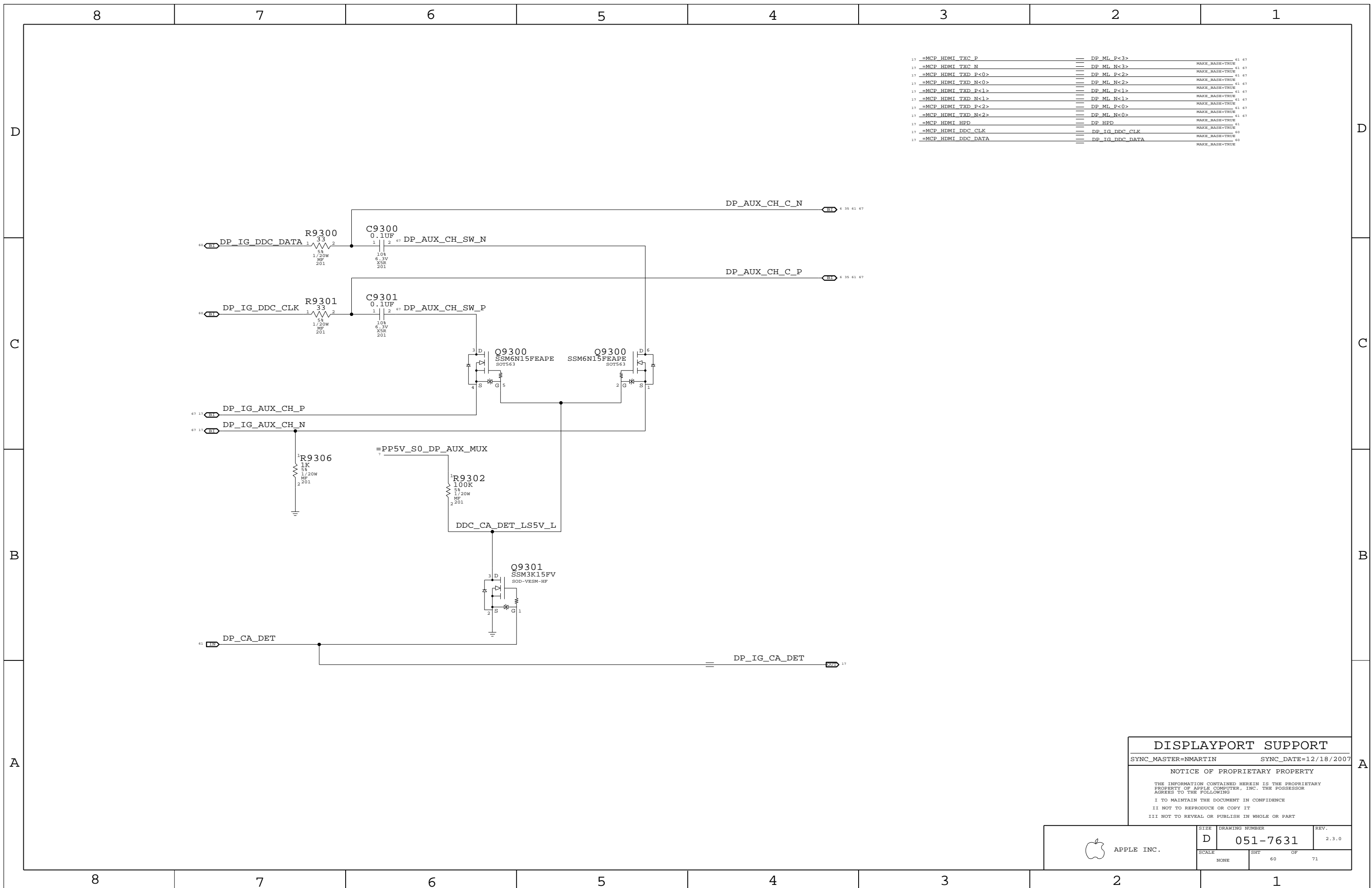
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

- I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	59	71




**DISPLAYPORT SUPPORT**

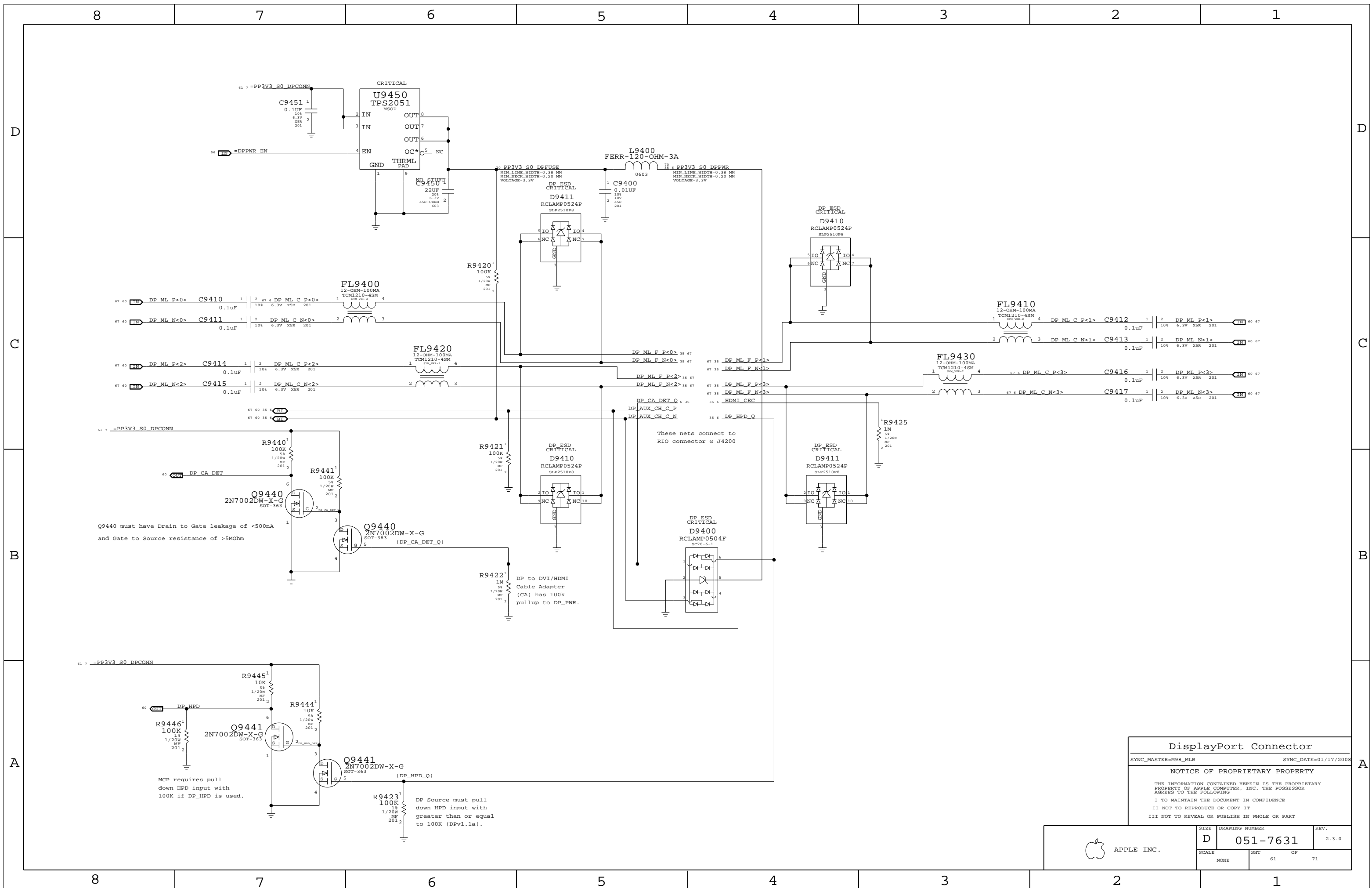
SYNC\_MASTER=NMARTIN      SYNC\_DATE=12/18/2007

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		
NONE	60 71		



**DisplayPort Connector**

SYNC\_MASTER=M98\_MLB SYNC\_DATE=01/17/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

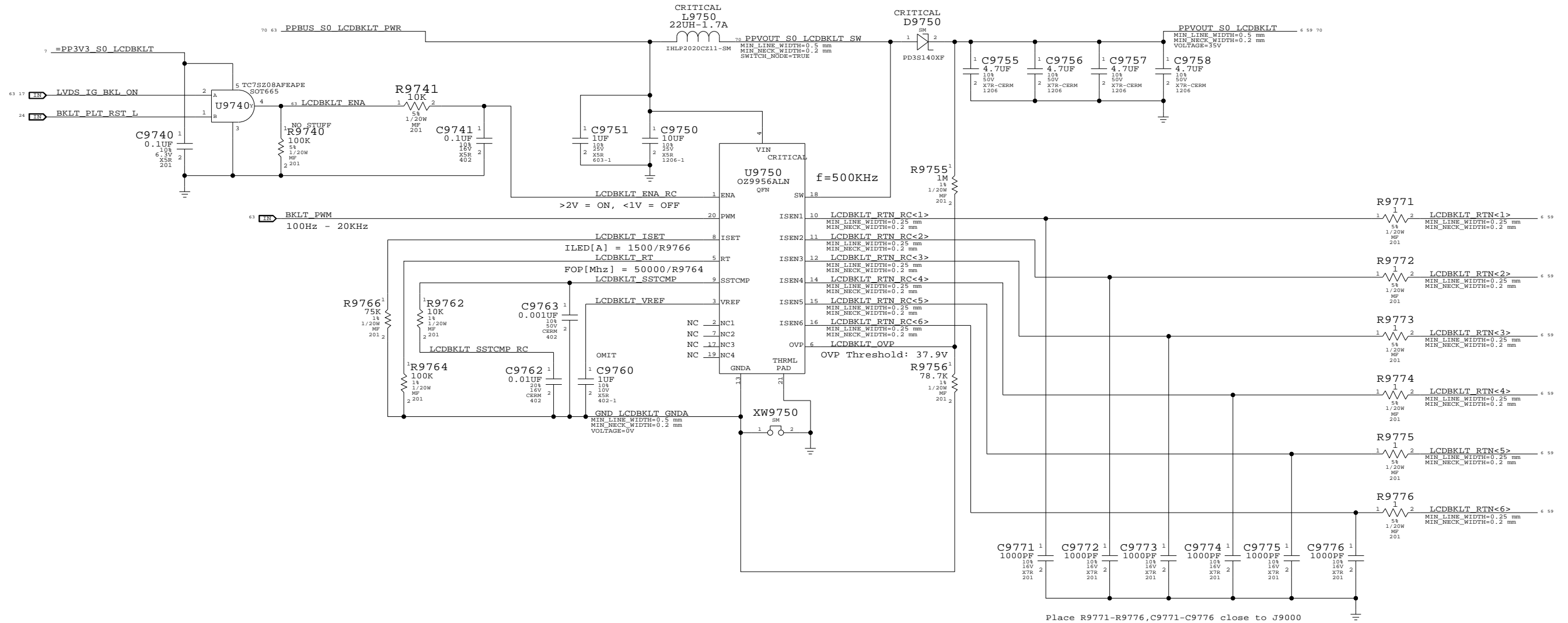
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE <b>D</b>	DRAWING NUMBER <b>051-7631</b>	REV. 2.3.0
	SCALE NONE	SHIT 61	OF 71

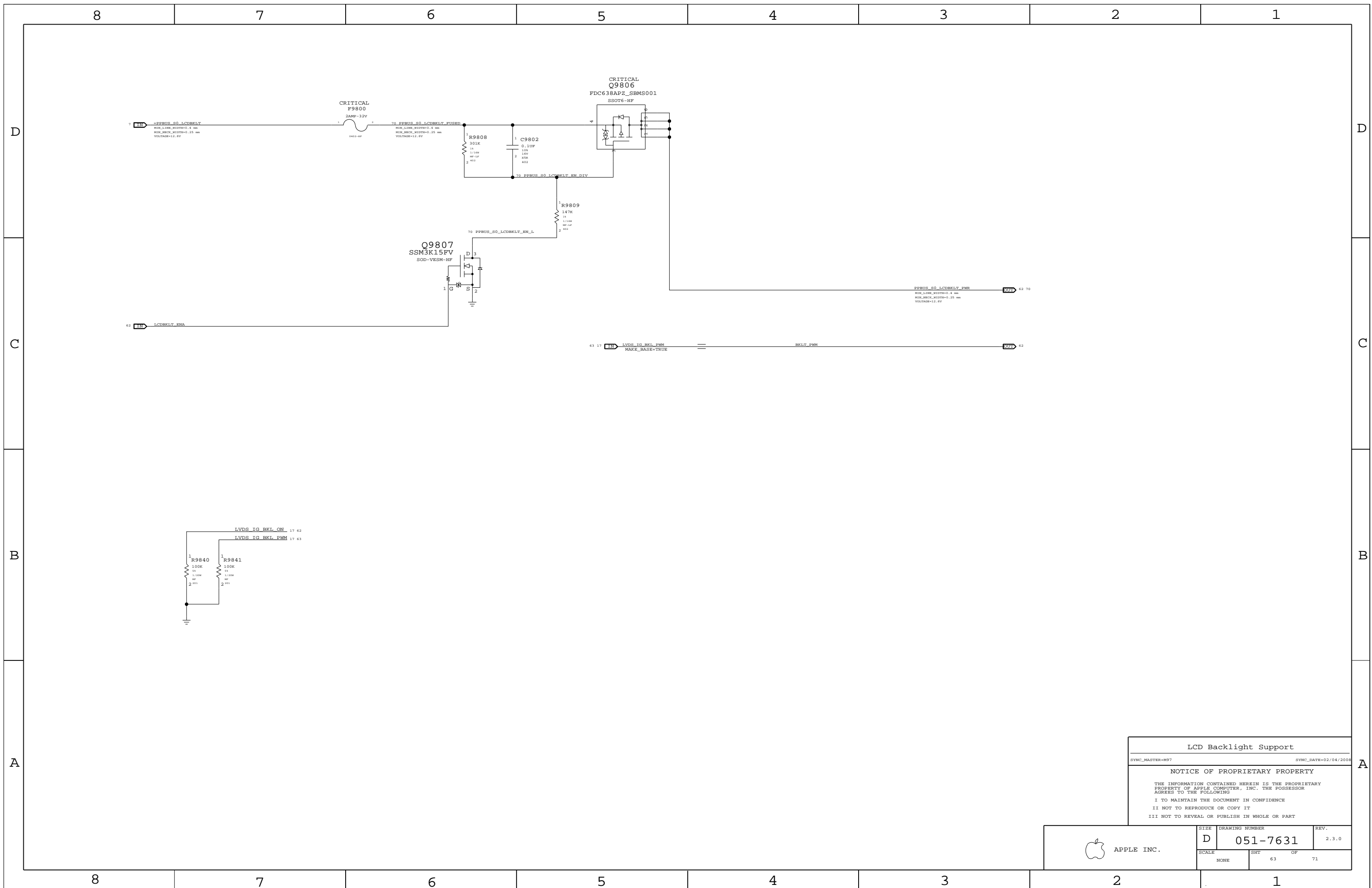
# LED Backlight Driver



Place R9771-R9776, C9771-C9776 close to J9000

**LED Backlight Driver**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)  
 NOTICE OF PROPRIETARY PROPERTY  
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	NONE	SHT	OF
		62	71



**LCD Backlight Support**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE		SHT	OF
NONE		63	71

8

7

6

5

4

3

2

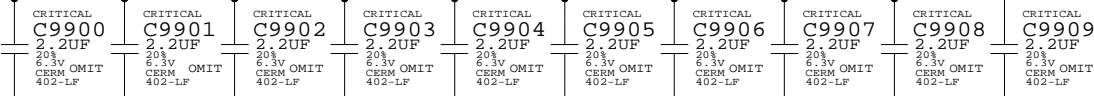
1

# ADDITIONAL CPU VCORE HF DECOUPLING

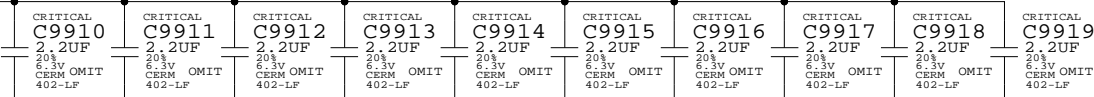
40x 2.2uF 0402

11 10 7 =FPVCORE\_S0\_CPU

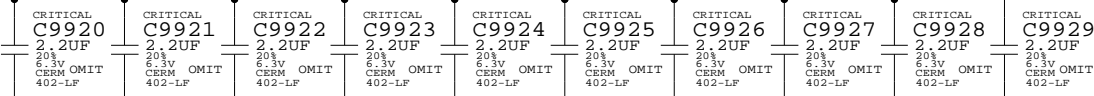
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



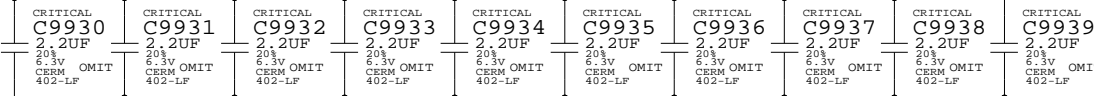
LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



LAYOUT NOTE:  
PLACE ON OPPOSITE SIDE OF CPU



## Additional CPU/GPU Decoupling

SYNC\_MASTER- SYNC\_DATE-

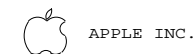
### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	64	71

8

7

6

5

4

3

2

1



FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB ADSTB L<1>
FSB_1X	FSB_50S	FSB_1X	FSB ADS L
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0 L
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB BREQ1 L
FSB_1X	FSB_50S	FSB_1X	FSB BNR L
FSB_1X	FSB_50S	FSB_1X	FSB BPR L
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L
FSB_1X	FSB_50S	FSB_1X	FSB HIT L
FSB_1X	FSB_50S	FSB_1X	FSB HITM L
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGARNE L
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM THRMTRIP L
FSB_CPURST_L	CPU_50S	CPU_AGTL	FSB CPURST L
CPU_PERR_SR	CPU_50S	CPU_AGTL	CPU DPSSL P
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N
CPU_IERR_L	CPU_50S		CPU IERR L
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L
	CPU_50S	CPU_8MIL	CPU VID<6..0>
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN P
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN N

CPU/FSB Constraints

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT	OF	71
NONE	65		

Memory Bus Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include MEM\_50S, MEM\_50S\_VDD, MEM\_90D, MEM\_90D\_VDD.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include MEM\_CLK2MEM, MEM\_CTRL2CTRL, MEM\_CTRL2MEM, MEM\_CMD2CMD, MEM\_CMD2MEM, MEM\_DATA2DATA, MEM\_DATA2MEM, MEM\_DQS2MEM, MEM\_2OTHER.

Memory Bus Spacing Group Assignments

Table with 8 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CLK, MEM\_CTRL, MEM\_CMD, MEM\_DATA, MEM\_DQS.

Table with 8 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CTRL, MEM\_DATA, MEM\_CMD, MEM\_DQS.

Table with 8 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_DQS, MEM\_CTRL, MEM\_CMD, MEM\_DATA.

Table with 8 columns: NET\_SPACING\_TYPE1, NET\_SPACING\_TYPE2, AREA\_TYPE, SPACING\_RULE\_SET. Rows include MEM\_CLK, MEM\_CMD, MEM\_CTRL, MEM\_DATA, MEM\_DQS, MEM\_CTRL, MEM\_DATA, MEM\_DQS, MEM\_CMD.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair. DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps. No DQS to clock matching requirement. CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps. A/BA/cmd signals should be matched within 5 ps of CLK pairs. All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate). DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

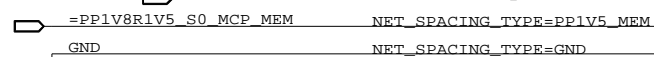
Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row: MCP\_MEM\_COMP.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row: MCP\_MEM\_COMP.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, SPACING, NET\_TYPE. Rows include MEM\_A\_CLK, MEM\_A\_CTRL, MEM\_A\_CMD, MEM\_A\_DATA, MEM\_A\_DQS, MEM\_B\_CLK, MEM\_B\_CTRL, MEM\_B\_CMD, MEM\_B\_DATA, MEM\_B\_DQS, MCP\_MEM\_COMP.



Memory Constraints

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



Table with 3 columns: DRAWING NUMBER, SCALE, REV. Row: D, 051-7631, 2.3.0.

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedance varies by location:  
 - 37.5-ohm from MCP to first termination resistor.  
 - 50-ohm from first to second termination resistor.  
 - 75-ohm from output of three-pole filter to connector (if possible).  
 R/G/B signals should be matched as close as possible and < 10 inches.  
 SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.  
 SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D_P<15..0>	PCIE_90D	PCIE	PEG_R2D_P<15..0>
PEG_R2D_N<15..0>	PCIE_90D	PCIE	PEG_R2D_N<15..0>
PEG_R2D_C_P<15..0>	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>
PEG_R2D_C_N<15..0>	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>
PEG_D2R_P<15..0>	PCIE_90D	PCIE	PEG_D2R_P<15..0>
PEG_D2R_N<15..0>	PCIE_90D	PCIE	PEG_D2R_N<15..0>
PEG_D2R_C_P<15..0>	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>
PEG_D2R_C_N<15..0>	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>
PCIE_MINI_R2D_P	PCIE_90D	PCIE	PCIE_MINI_R2D_P
PCIE_MINI_R2D_N	PCIE_90D	PCIE	PCIE_MINI_R2D_N
PCIE_MINI_R2D_C_P	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N
PCIE_MINI_D2R_P	PCIE_90D	PCIE	PCIE_MINI_D2R_P
PCIE_MINI_D2R_N	PCIE_90D	PCIE	PCIE_MINI_D2R_N
PCIE_MINI_D2R_C_P	PCIE_90D	PCIE	PCIE_MINI_D2R_C_P
PCIE_MINI_D2R_C_N	PCIE_90D	PCIE	PCIE_MINI_D2R_C_N
PCIE_FW_R2D_P	PCIE_90D	PCIE	PCIE_FW_R2D_P
PCIE_FW_R2D_N	PCIE_90D	PCIE	PCIE_FW_R2D_N
PCIE_FW_R2D_C_P	PCIE_90D	PCIE	PCIE_FW_R2D_C_P
PCIE_FW_R2D_C_N	PCIE_90D	PCIE	PCIE_FW_R2D_C_N
PCIE_FW_D2R_P	PCIE_90D	PCIE	PCIE_FW_D2R_P
PCIE_FW_D2R_N	PCIE_90D	PCIE	PCIE_FW_D2R_N
PCIE_FW_D2R_C_P	PCIE_90D	PCIE	PCIE_FW_D2R_C_P
PCIE_FW_D2R_C_N	PCIE_90D	PCIE	PCIE_FW_D2R_C_N
PCIE_EXCARD_R2D_P	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P
PCIE_EXCARD_R2D_N	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N
PCIE_EXCARD_R2D_C_P	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P
PCIE_EXCARD_R2D_C_N	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_D2R_P	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P
PCIE_EXCARD_D2R_N	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N
PCIE_FC_R2D_P	PCIE_90D	PCIE	PCIE_FC_R2D_P
PCIE_FC_R2D_N	PCIE_90D	PCIE	PCIE_FC_R2D_N
PCIE_FC_R2D_C_P	PCIE_90D	PCIE	PCIE_FC_R2D_C_P
PCIE_FC_R2D_C_N	PCIE_90D	PCIE	PCIE_FC_R2D_C_N
PCIE_FC_D2R_P	PCIE_90D	PCIE	PCIE_FC_D2R_P
PCIE_FC_D2R_N	PCIE_90D	PCIE	PCIE_FC_D2R_N
PEG_CLK100M_P	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P
PEG_CLK100M_N	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N
PCIE_CLK100M_MINI_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N
PCIE_CLK100M_FC_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P
PCIE_CLK100M_FC_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N
PCIE_CLK100M_FW_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N
PCIE_CLK100M_EXCARD_P	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P
PCIE_CLK100M_EXCARD_N	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N
MCP_PEX_CLK_COMP	MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_CLK_COMP
TMDS_IG_TXC_P	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P
TMDS_IG_TXC_N	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N
TMDS_IG_TXD_P<2..0>	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>
TMDS_IG_TXD_N<2..0>	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>
DP_ML_C_P<3..0>	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>
DP_ML_C_N<3..0>	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>
DP_ML_F_P<3..0>	DP_100D	DISPLAYPORT	DP_ML_F_P<3..0>
DP_ML_F_N<3..0>	DP_100D	DISPLAYPORT	DP_ML_F_N<3..0>
DP_ML_P<3..0>	DP_100D	DISPLAYPORT	DP_ML_P<3..0>
DP_ML_N<3..0>	DP_100D	DISPLAYPORT	DP_ML_N<3..0>
DP_IG_AUX_CH_P	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P
DP_IG_AUX_CH_N	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N
DP_AUX_CH_C_P	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P
DP_AUX_CH_C_N	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N
DP_AUX_CH_SW_P	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P
DP_AUX_CH_SW_N	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N
MCP_HDMI_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP_HDMI_RSET
MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP_HDMI_VPROBE
LVDS_IG_A_CLK_F_P	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P
LVDS_IG_A_CLK_F_N	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N
LVDS_IG_A_CLK_P	LVDS_100D	LVDS	LVDS_IG_A_CLK_P
LVDS_IG_A_CLK_N	LVDS_100D	LVDS	LVDS_IG_A_CLK_N
LVDS_IG_A_DATA_F_P<2..0>	LVDS_100D	LVDS	LVDS_IG_A_DATA_F_P<2..0>
LVDS_IG_A_DATA_F_N<2..0>	LVDS_100D	LVDS	LVDS_IG_A_DATA_F_N<2..0>
LVDS_IG_A_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>
LVDS_IG_A_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA3
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA3
LVDS_IG_B_CLK_P	LVDS_100D	LVDS	LVDS_IG_B_CLK_P
LVDS_IG_B_CLK_N	LVDS_100D	LVDS	LVDS_IG_B_CLK_N
LVDS_IG_B_DATA_P<2..0>	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>
LVDS_IG_B_DATA_N<2..0>	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA3
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA3
MCP_IFPAB_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP_IFPAB_RSET
MCP_IFPAB_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP_IFPAB_VPROBE
SATA_HDD_R2D_C_P	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P
SATA_HDD_R2D_C_N	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N
SATA_HDD_R2D_P	SATA_100D_HDD	SATA	SATA_HDD_R2D_P
SATA_HDD_R2D_N	SATA_100D_HDD	SATA	SATA_HDD_R2D_N
SATA_HDD_R2D_UF_P	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P
SATA_HDD_R2D_UF_N	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N
SATA_HDD_D2R_P	SATA_100D_HDD	SATA	SATA_HDD_D2R_P
SATA_HDD_D2R_N	SATA_100D_HDD	SATA	SATA_HDD_D2R_N
SATA_HDD_D2R_C_P	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P
SATA_HDD_D2R_C_N	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N
SATA_HDD_D2R_UF_P	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_P
SATA_HDD_D2R_UF_N	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_N
MCP_SATA_TERM	SATA_TERM	SATA_TERM	MCP_SATA_TERM

**MCP Constraints 1**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_BIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MCP_DEBUG	SPT_55S	SPT	MCP_DEBUG<7..0>
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REG0_I	PCI_55S	PCI	PCI_REG0_I
PCI_REG0_I	PCI_55S	PCI	PCI_GNT0_L
PCI_REG0_I	PCI_55S	PCI	PCI_REG0_L
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTX_I	PCI_55S	PCI	PCI_INTX_L
PCI_INTX_I	PCI_55S	PCI	PCI_INTX_L
PCI_INTX_I	PCI_55S	PCI	PCI_INTX_L
PCI_INTZ_I	PCI_55S	PCI	PCI_INTZ_L
PCI_CLK33M_MCP_R	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R
PCI_CLK33M_MCP	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L
LPC_RESET_I	LPC_55S	LPC	LPC_RESET_L
LPC_CLK33M_SMC_R	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R
LPC_CLK33M_SMC	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC
LPC_CLK33M_LPCPLUS	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS
USB_EXTN_P	USB_90D	USB	USB_EXTN_P
USB_EXTN_N	USB_90D	USB	USB_EXTN_N
USB_EXTN_MUXED_P	USB_90D	USB	USB_EXTN_MUXED_P
USB_EXTN_MUXED_N	USB_90D	USB	USB_EXTN_MUXED_N
CONN_USB_EXTN_P	USB_90D	USB	CONN_USB_EXTN_P
CONN_USB_EXTN_N	USB_90D	USB	CONN_USB_EXTN_N
USB_MINI_P	USB_90D	USB	USB_MINI_P
USB_MINI_N	USB_90D	USB	USB_MINI_N
USB_EXTD_P	USB_90D	USB	USB_EXTD_P
USB_EXTD_N	USB_90D	USB	USB_EXTD_N
USB_CAMERA_P	USB_90D	USB	USB_CAMERA_P
USB_CAMERA_N	USB_90D	USB	USB_CAMERA_N
USB_CAMERA_CONN_P	USB_90D	USB	USB_CAMERA_CONN_P
USB_CAMERA_CONN_N	USB_90D	USB	USB_CAMERA_CONN_N
USB_BT_P	USB_90D	USB	USB_BT_P
USB_BT_N	USB_90D	USB	USB_BT_N
CONN_USB2_BT_P	USB_90D	USB	CONN_USB2_BT_P
CONN_USB2_BT_N	USB_90D	USB	CONN_USB2_BT_N
USB_TPAD_P	USB_90D	USB	USB_TPAD_P
USB_TPAD_N	USB_90D	USB	USB_TPAD_N
CONN_TPAD_USB_P	USB_90D	USB	CONN_TPAD_USB_P
CONN_TPAD_USB_N	USB_90D	USB	CONN_TPAD_USB_N
USB_IR_P	USB_90D	USB	USB_IR_P
USB_IR_N	USB_90D	USB	USB_IR_N
USB_EXTB_P	USB_90D	USB	USB_EXTB_P
USB_EXTB_N	USB_90D	USB	USB_EXTB_N
CONN_USB_EXTB_P	USB_90D	USB	CONN_USB_EXTB_P
CONN_USB_EXTB_N	USB_90D	USB	CONN_USB_EXTB_N
USB_EXCARD_P	USB_90D	USB	USB_EXCARD_P
USB_EXCARD_N	USB_90D	USB	USB_EXCARD_N
USB_EXTC_P	USB_90D	USB	USB_EXTC_P
USB_EXTC_N	USB_90D	USB	USB_EXTC_N
MCP_USB_BIAS	MCP_USB_BIAS	MCP_USB_BIAS	MCP_USB_BIAS_GND
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK
HDA_BIT_CLK_R	HDA_55S	HDA	HDA_BIT_CLK_R
HDA_SYNC	HDA_55S	HDA	HDA_SYNC
HDA_SYNC_R	HDA_55S	HDA	HDA_SYNC_R
HDA_RST_I	HDA_55S	HDA	HDA_RST_I
HDA_RST_L	HDA_55S	HDA	HDA_RST_L
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0
HDA_SDIN_CODEC	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT
HDA_SDOUT_R	HDA_55S	HDA	HDA_SDOUT_R
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP	MCP_HDA_COMP	MCP_HDA_PULLDN_COMP
PM_CLK32K_SUSCLK_R	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R
PM_CLK32K_SUSCLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK
SPI_CLK_R	SPT_55S	SPT	SPI_CLK_R
SPI_CLK	SPT_55S	SPT	SPI_CLK
SPI_MOSI_R	SPT_55S	SPT	SPI_MOSI_R
SPI_MOSI	SPT_55S	SPT	SPI_MOSI
SPI_MISO	SPT_55S	SPT	SPI_MISO
SPI_MISO_R	SPT_55S	SPT	SPI_MISO_R
SPI_CS0_R_L	SPT_55S	SPT	SPI_CS0_R_L
SPI_CS0_L	SPT_55S	SPT	SPI_CS0_L
SPI_CLK_MUX	SPT_55S	SPT	SPI_CLK_MUX
SPI_MOSI_MUX	SPT_55S	SPT	SPI_MOSI_MUX
SPI_MISO_MUX	SPT_55S	SPT	SPI_MISO_MUX
SPI_MLB_CS_L	SPT_55S	SPT	SPI_MLB_CS_L

**MCP Constraints 2**

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

**NOTICE OF PROPRIETARY PROPERTY**

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

8

7

6

5

4

3

2

1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

### SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB 55G	2MM	SMBUS_SMC_A_S3_SCL	42
SMBUS_SMC_A_S3_SDA	SMB 55G	2MM	SMBUS_SMC_A_S3_SDA	42
SMBUS_SMC_B_S0_SCL	SMB 55G	2MM	SMBUS_SMC_B_S0_SCL	42
SMBUS_SMC_B_S0_SDA	SMB 55G	2MM	SMBUS_SMC_B_S0_SDA	42
SMBUS_SMC_0_S0_SCL	SMB 55G	2MM	SMBUS_SMC_0_S0_SCL	42
SMBUS_SMC_0_S0_SDA	SMB 55G	2MM	SMBUS_SMC_0_S0_SDA	42
SMBUS_SMC_BSA_SCL	SMB 55G	2MM	SMBUS_SMC_BSA_SCL	6 42
SMBUS_SMC_BSA_SDA	SMB 55G	2MM	SMBUS_SMC_BSA_SDA	6 42
SMBUS_SMC_MGMT_SCL	SMB 55G	2MM	SMBUS_SMC_MGMT_SCL	42
SMBUS_SMC_MGMT_SDA	SMB 55G	2MM	SMBUS_SMC_MGMT_SDA	42

### SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	
	1TO1_DIFFPAIR		CHGR_CSI_N	
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	
	1TO1_DIFFPAIR		CHGR_CSO_N	

D

D

C

C

B

B

A

A

### SMC Constraints

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

#### NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE	DRAWING NUMBER	REV.
D	051-7631	2.3.0
SCALE	SHT	OF
NONE	69	71

8

7

6

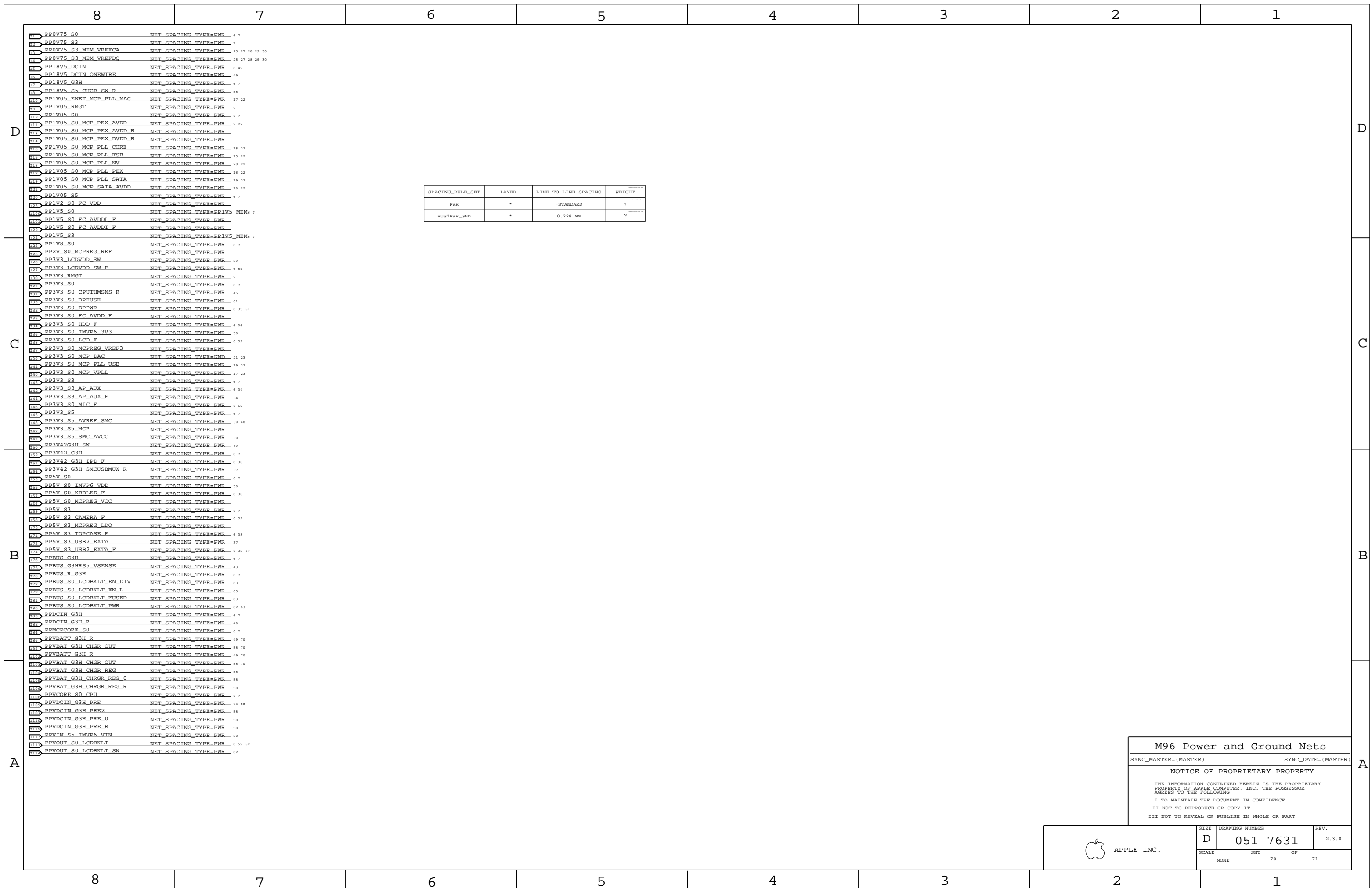
5

4

3

2

1



SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M96 Power and Ground Nets

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING  
 I TO MAINTAIN THE DOCUMENT IN CONFIDENCE  
 II NOT TO REPRODUCE OR COPY IT  
 III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7631	2.3.0
SCALE	SHT OF		
NONE	70 OF 71		

M96 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, ISL12, ISL13, BOTTOM				NO_TYPE, BGA_P1MM				MM	15.2
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
DEFAULT	*	Y	=50_OHM_SE	0.200 MM	30 MM	0 MM	0 MM		
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
55_OHM_SE	TOP, BOTTOM	Y	0.210 MM	0.200 MM					
55_OHM_SE	ISL2, ISL13	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD		
55_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
50_OHM_SE	TOP, BOTTOM	Y	0.250 MM	0.200 MM					
50_OHM_SE	ISL2, ISL13	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD		
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
40_OHM_SE	TOP, BOTTOM	Y	0.350 MM	0.200 MM					
40_OHM_SE	ISL2, ISL13	Y	0.122 MM	0.122 MM	=STANDARD	=STANDARD	=STANDARD		
40_OHM_SE	*	Y	0.110 MM	0.110 MM	=STANDARD	=STANDARD	=STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
27P4_OHM_SE	TOP, BOTTOM	Y	0.215 MM	0.200 MM					
27P4_OHM_SE	*	Y	0.215 MM	0.215 MM	=STANDARD	=STANDARD	=STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		
70_OHM_DIFF	ISL2, ISL4, ISL5, ISL6, ISL11, ISL12	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM		
70_OHM_DIFF	TOP, BOTTOM	Y	0.180 MM	0.180 MM		0.150 MM	0.150 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		
90_OHM_DIFF	ISL2, ISL4, ISL5, ISL6, ISL11, ISL12	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM		
90_OHM_DIFF	TOP, BOTTOM	Y	0.205 MM	0.200 MM		0.160 MM	0.160 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		
100_OHM_DIFF	ISL2, ISL4, ISL5, ISL6, ISL11, ISL12	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM		
100_OHM_DIFF	TOP, BOTTOM	Y	0.179 MM	0.179 MM		0.200 MM	0.200 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD		
100_OHM_DIFF_HDD	ISL2, ISL4, ISL5, ISL6, ISL11, ISL12	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM		
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.179 MM	0.179 MM		0.200 MM	0.200 MM		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
40_OHM_SE_MEM	TOP, BOTTOM	Y	0.170 MM	0.110 MM	10 MM				
40_OHM_SE_MEM	ISL2, ISL13	Y	0.122 MM	0.066 MM	170 MM	=STANDARD	=STANDARD		
40_OHM_SE_MEM	*	Y	0.110 MM	0.066 MM	170 MM	=STANDARD	=STANDARD		
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP		
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
4:1_SPACING	*	0.4 MM	?
2.28:1_SPACING	*	0.228 MM	?
1.1:1_SPACING	*	0.110 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP, BOTTOM	0.230 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.345 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.460 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.575 MM	?
2X_DIELECTRIC	ISL2, ISL13	0.110 MM	?
3X_DIELECTRIC	ISL2, ISL13	0.165 MM	?
4X_DIELECTRIC	ISL2, ISL13	0.220 MM	?
5X_DIELECTRIC	ISL2, ISL13	0.275 MM	?
2X_DIELECTRIC	*	0.120 MM	?
3X_DIELECTRIC	*	0.180 MM	?
4X_DIELECTRIC	*	0.240 MM	?
5X_DIELECTRIC	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_STATIC		=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_50s	BGA_P1MM	STANDARD

M96 RULE DEFINITIONS

SYNC\_MASTER=M97 SYNC\_DATE=02/04/2008

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



SIZE DRAWING NUMBER REV.

D 051-7631 2.3.0

SCALE NONE SHIT OF 71 71

D

D

C

C

B

B

A

A

8

7

6

5

4

3

2

1

8

7

6

5

4

3

2

1