1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2012-02-23

SCHEM,MLB,J13

2/23/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9277	1	SCHEM,MLB,J13	SCH	CRITICAL	
820-3209	1	PCBF,MLB,J13	PCB	CRITICAL	

DRAWING
TITLE=MLB
ASSEMY=DRAWING
LAST_MODIFIED=Thu Feb 23 17:52:06 2012

DRAWING TITLE: SCHEM,MLB,J13

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D
REVISION: 2.8.0
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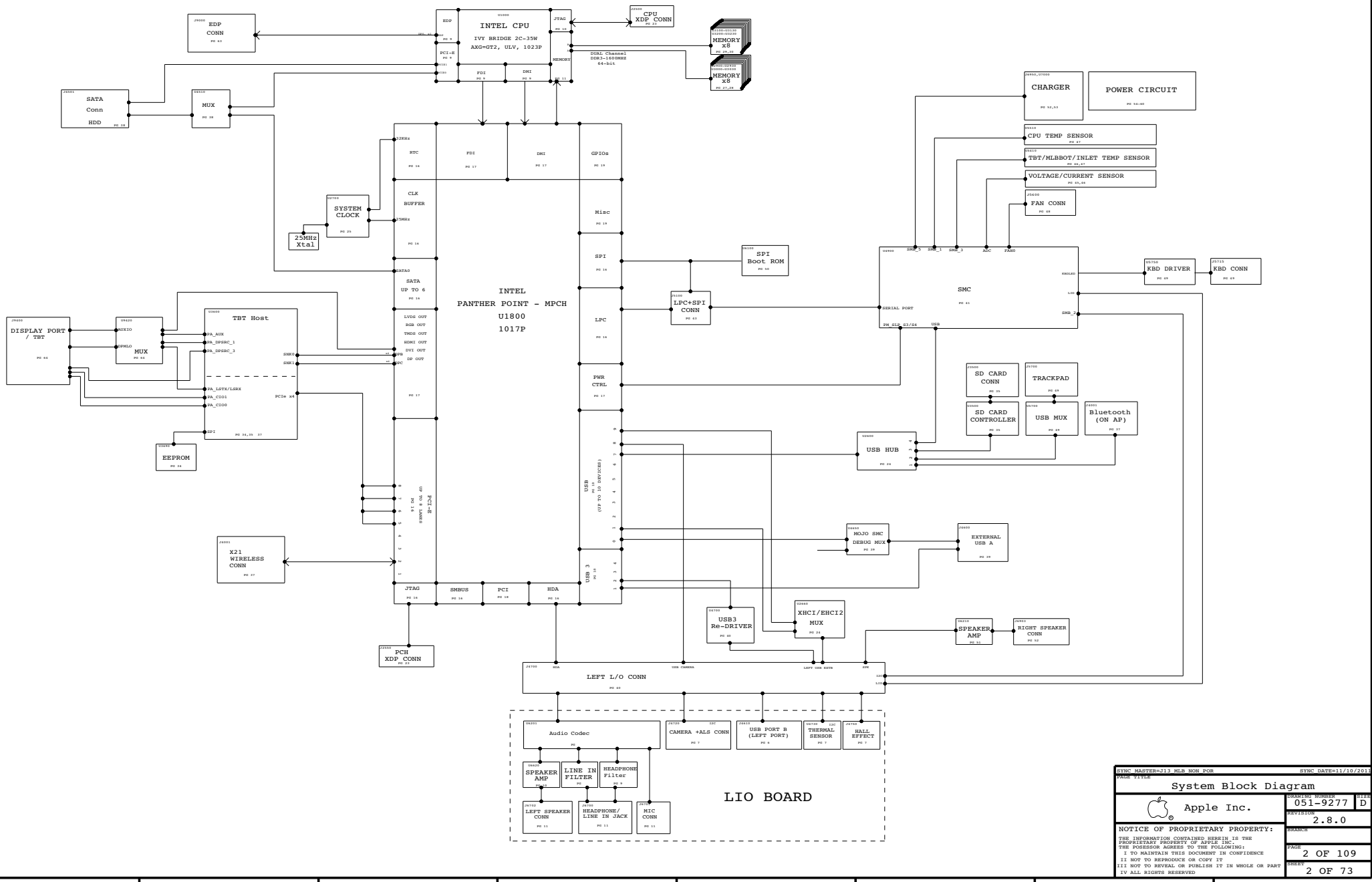

SYNC MASTER=J13_MLB_NON_POR SYNC DATE=11/10/2011

PAGE TITLE

System Block Diagram

Apple Inc.

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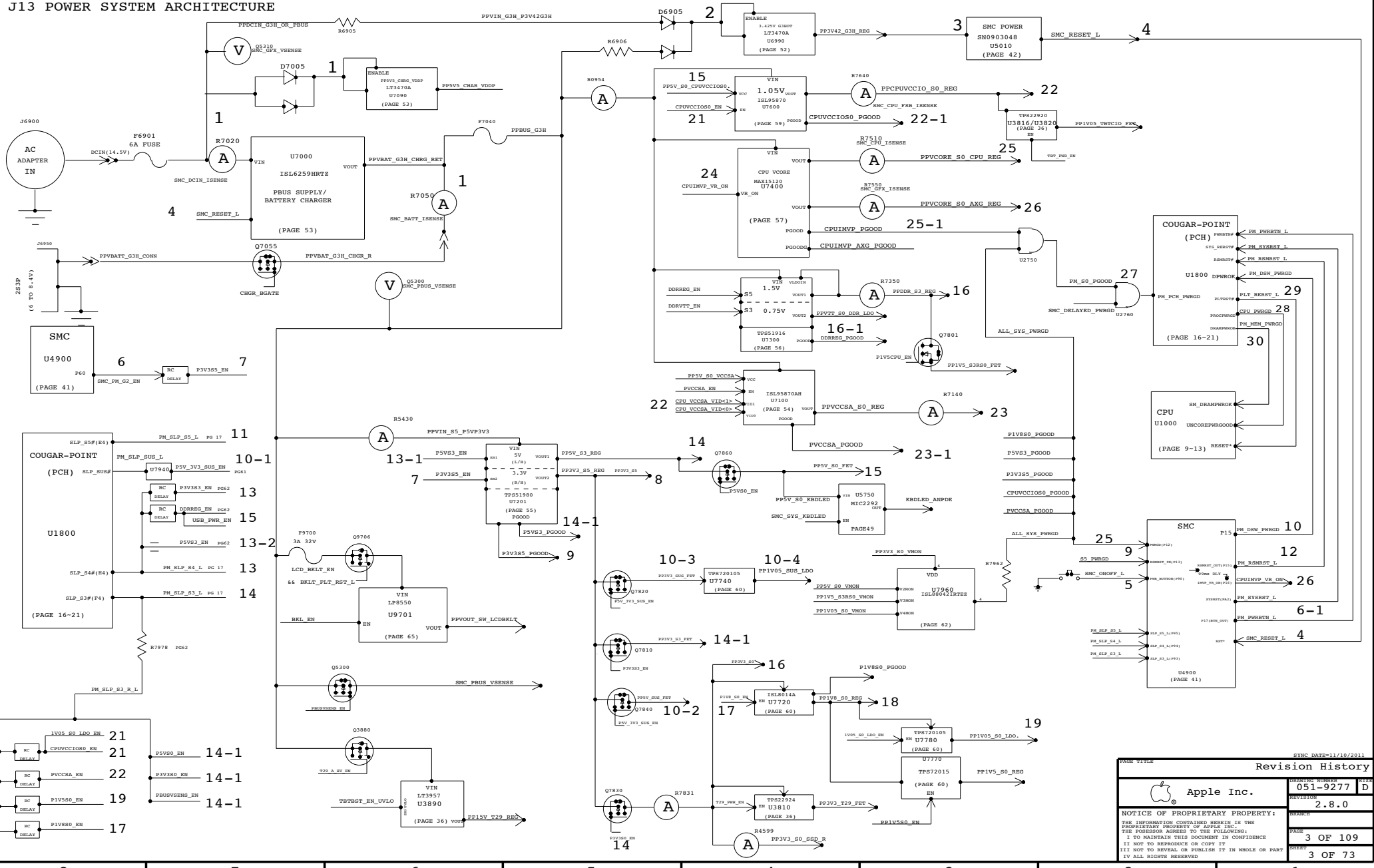
J13 POWER SYSTEM ARCHITECTURE



SYNC_DATE=11/10/2011

PAGE TITLE: Revision History

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3939	J13 MLB DEVELOPMENT BOM	J13_DEVEL:ENG
607-9090	CMN PTS,PCBA,MLB,J13	J13_COMMON
639-3552	PCBA,MLB,1.7GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRQ,CPU:1.7GHZ,DDR3:SAMSUNG_4GB
639-3553	PCBA,MLB,1.5GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRM,CPU:1.5GHZ,DDR3:SAMSUNG_4GB
639-3554	PCBA,MLB,1.5GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.5GHZ,DDR3:HYNIX_4GB
639-3555	PCBA,MLB,1.5GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRL,CPU:1.5GHZ,DDR3:HYNIX_8GB
639-3556	PCBA,MLB,1.7GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRK,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-3557	PCBA,MLB,1.7GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRP,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-3645	PCBA,MLB,1.5GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TC,CPU:1.5GHZ,DDR3:ELPIDA_8GB
639-3644	PCBA,MLB,1.7GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TD,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-3760	PCBA,MLB,1.8GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25Q,CPU:1.8GHZ,DDR3:SAMSUNG_4GB
639-3761	PCBA,MLB,1.8GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25T,CPU:1.8GHZ,DDR3:HYNIX_8GB
639-3762	PCBA,MLB,1.8GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25Y,CPU:1.8GHZ,DDR3:HYNIX_4GB
639-3763	PCBA,MLB,1.8GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25P,CPU:1.8GHZ,DDR3:ELPIDA_8GB
639-3764	PCBA,MLB,2.0GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25N,CPU:2.0GHZ,DDR3:SAMSUNG_4GB
639-3765	PCBA,MLB,2.0GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25W,CPU:2.0GHZ,DDR3:HYNIX_8GB
639-3766	PCBA,MLB,2.0GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25R,CPU:2.0GHZ,DDR3:HYNIX_4GB
639-3767	PCBA,MLB,2.0GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25V,CPU:2.0GHZ,DDR3:ELPIDA_8GB
639-3790	PCBA,MLB,1.7GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:1.7GHZ,DDR3:SAMSUNG_8GB
639-3791	PCBA,MLB,1.8GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27Q,CPU:1.8GHZ,DDR3:SAMSUNG_8GB
639-3792	PCBA,MLB,2.0GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27R,CPU:2.0GHZ,DDR3:SAMSUNG_8GB
639-3793	PCBA,MLB,1.7GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27W,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-3794	PCBA,MLB,1.8GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:1.8GHZ,DDR3:ELPIDA_4GB
639-3795	PCBA,MLB,2.0GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27T,CPU:2.0GHZ,DDR3:ELPIDA_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_DYRK]	CRITICAL	EEEE:DYRK
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_DYRL]	CRITICAL	EEEE:DYRL
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_DYRM]	CRITICAL	EEEE:DYRM
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_DYRN]	CRITICAL	EEEE:DYRN
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_DYRP]	CRITICAL	EEEE:DYRP
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_DYRQ]	CRITICAL	EEEE:DYRQ
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F0TC]	CRITICAL	EEEE:F0TC
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F0TD]	CRITICAL	EEEE:F0TD
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25N]	CRITICAL	EEEE:F25N
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25P]	CRITICAL	EEEE:F25P
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25Q]	CRITICAL	EEEE:F25Q
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25R]	CRITICAL	EEEE:F25R
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25T]	CRITICAL	EEEE:F25T
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25V]	CRITICAL	EEEE:F25V
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25W]	CRITICAL	EEEE:F25W
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F25Y]	CRITICAL	EEEE:F25Y
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F27Q]	CRITICAL	EEEE:F27Q
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F27R]	CRITICAL	EEEE:F27R
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F27T]	CRITICAL	EEEE:F27T
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F27V]	CRITICAL	EEEE:F27V
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F27W]	CRITICAL	EEEE:F27W
825-7670	1	LBL,P/N LABEL,PCB,28MM x 6 MM	[EEEE_F27Y]	CRITICAL	EEEE:F27Y

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3939	1	J13 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-9090	1	CMN PTS,PCBA,MLB,J13	CMNPTS	CRITICAL	J13_CMNPTS

SYNC MASTER=J30_MLB SYNC DATE=07/27/2013

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Revision History

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J13 BOM GROUPS

BOM GROUP	BOM OPTIONS
J13_COMMON	ALTERNATE,COMMON,J13_MISC,J13_DEBUG:ENG,J13_PROGPARTS,USBHUB2514B,EDP:YES,PCH_C1
J13_MISC	CPUMEM_SLG:NO,HUB_INGNSEN,TBT,NPM5:YES,PSYS_DCIN:NO,TPAD_PCH:NO,SKIP_3V3V3:INAUDIBLE,NTPWR:84,TBTHV:P15V,LVDDR3_HW:YES,AXG_ACOUSTIC:NO
J13_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J13_DEVEL:ENG	ALTERNATE,RELT:ENG,EDP_CONN,EDP_CPU:EPN,EDP_PCH,LPCPLUS,IGNVREF_DAC,VREFDQ:M1_M2,VREFCA:LDO_DAC,SSPSOCH_ISL,S3_S0_LED,VCCIOSENSE_ENG,AIRPORTSENSE_ENG,HDDISENS_ENG,LCDBKLTSENS_ENG
J13_DEVEL:PVT	LPCPLUS,EDP_CONN
J13_DEBUG:ENG	DEVEL_ROM,MOJO:YES,EDP
J13_DEBUG:PVT	DEVEL_ROM,RELT:PROD,MOJO:YES,EDP,EDP_CPU:EPN,VREFDQ:LDO,VREFCA:LDO,VCCIOSENS_PROD,AIRPORTSENS_PROD,HDDISENS_PROD,LCDBKLTSNS_PROD
J13_DEBUG:PROD	RELT:PROD,MOJO:YES,EDP,EDP_CPU:EPN,VREFDQ:LDO,VREFCA:LDO,LPCPLUS,VCCIOSENS_PROD,AIRPORTSNS_PROD,HDDISNS_PROD,LCDBKLTSNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	IC,SERIAL SPI EEPROM,256KBIT,20MHZ,WLP8	U3690	CRITICAL	TBTROM:BLANK
341S3475	1	IC,EEPROM,CN,V24.1,J11/J13	U3690	CRITICAL	TBTROM:PROG
338S1098	1	IC,SMC12-A2,40MHZ/50MIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
338S1065	1	IC,SMC12,40MHZ/50MIPS MCU, 9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3433	1	IC,SMC,V2.1A43,Proto1B,J13	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Samsung	U6100	CRITICAL	BOOTROM_BLANK
341S3482	1	IC,SPI ROM,PROTO1B,J13 J11	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0413		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
13S80676	13S80691		ALL	Murata alt to Samsung
371S0709	371S0652		ALL	NXP alt to NXP
13S80671	13S80673		ALL	Taiyo alt to Murata
376S0790	376S0928		ALL	TI alt to Fairchild
152S1462	152S1295		ALL	Toko alt for NEC inductor
152S1085	152S1307		ALL	Toko alt for Cyntec
13S80703	13S80648		ALL	Murata alt to Taiyo Yuden
13S80684	13S80660		ALL	Murata alt to Taiyo Yuden
152S1493	152S1300		ALL	Coilcraft alt to Murata

353S3238	353S1428		ALL	Intersil alt to OPA2333
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S0855	376S0413		ALL	Diodes alt to Toshiba
376S0903	376S0796		ALL	Fairchild alt to Siliconix
197S0431	197S0432		ALL	Epson alt to NDK
337S4198	337S4197		ALL	TDP 1.5GHZ alt to Nominal
337S4236	337S4196		ALL	TDP 1.7GHZ alt to Nominal
371S0713	371S0558		ALL	Diodes alt to ST Micro
129S0333	999-4435		ALL	Sanyo alt to Kemet
129S0357	998-4435		ALL	Sanyo alt to POS caps
998-4715	998-4435		ALL	Kemet_Rect alt to POS caps
998-4716	998-4435		ALL	Kemet_.0045 Flute alt to POS caps

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	SVB,QM49,ES2,K0,1.5,17W,2+2,0.95,4M,ULVH	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	SVB,QC55,QM,L0,1.7,17W,2+2,1.0,3M,ULVHGA	U1000	CRITICAL	CPU:1.7GHZ
337S4298	1	SVB,QC54,QM,L0,1.8,17W,2+2,1.1,3M,ULVHGA	U1000	CRITICAL	CPU:1.8GHZ
337S4296	1	SVB,QC52,QM,L0,2.0,17W,2+2,1.1,4M,ULVHGA	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	SVB,QM49,ES2,K0,1.5,17W,2+2,0.95,4M,ULVH	U1000	CRITICAL	CPU:1.5GHZTDP
337S4236	1	SVB,QMQF,ES2,K0,1.7,17W,2+2,1.0,4M,ULV,TDP	U1000	CRITICAL	CPU:1.7GHZTDP
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,K0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	TBT

333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FPGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FWGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FWGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MX8,DDR3-1600,82 FWGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FWGA,D-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FGBA,D-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FWGA,D-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FWGA,C-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FGBA,C-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FWGA,C-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FWGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FWGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FWGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FWGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB

353S2929	1	IC,ISL6259,BATCHARGER,3%,4X4MM,QFN20	U7000	CRITICAL	
946-3115	1	MLB,DYMAX UV ES 0.22GRAM,K21	GLUE	CRITICAL	

PD Module Parts

806-3142	1	CAM,T29,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAM,COVER,T29,J11/J13	TBTCOVER	CRITICAL	
806-3214	1	CAM,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3706	1	CAM,TOPSIDE_2Piece_Cover,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAM,TOPSIDE_2Piece_Fence,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3216	1	CAM,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF

SYNC MASTER=J30_MLB SYNC DATE=07/27/2013

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BOM Configuration

Apple Inc.

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN_F	37 42	(Need 5 TPs)
TRUE	WIFI_EVENT_L	37 41 42	
TRUE	PCIE_AP_R2D_N	37 69	
TRUE	PCIE_AP_R2D_P	37 69	
TRUE	PCIE_CLK100M_AP_N	16 37 69	
TRUE	PCIE_CLK100M_AP_P	16 37 69	
TRUE	USB_BT_CONN_P	37 68	
TRUE	USB_BT_CONN_N	37 68	
TRUE	PCIE_AP_D2R_P	16 37 69	
TRUE	PCIE_AP_D2R_N	16 37 69	
TRUE	PCIE_WAKE_L	17 37	
TRUE	AP_RESET_CONN_L	37	
TRUE	AP_CLKREQ_Q_L	37	
TRUE	PP3V3_S3RS4_BT_F	37	

(Need to add 8 GND TPs)

J5715: KB BKLT CONNECTOR

FUNC_TEST

TRUE	KBDLED_FB	49	
TRUE	KBDLED_ANODE	49	

(Need to add 2 GND TP)

J4700: LIO Connector

FUNC_TEST

TRUE	=PP3V42_G3H_ONEWIRE	? 40	
TRUE	=PP3V3_S0_AUDIO	? 40	(Need 2 TPs)
TRUE	=PP3V3R1V5_S0_AUDIO	? 40	
TRUE	SYS_ONEWIRE	40 61	
TRUE	SMC_BC_ACOK	40 61 42	
TRUE	=USB_PWR_EN	39 40 62	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	=I2C_LIO_SDA	40 64	
TRUE	=I2C_LIO_SCL	40 64	
TRUE	=I2C_MIKEY_SCL	40 64	
TRUE	=I2C_MIKEY_SDA	40 64	
TRUE	AUD_IPHS_SWITCH_EN	25 40	
TRUE	AUD_IP_PERIPHERAL_DET	19 40	
TRUE	AUD_I2C_INT_L	18 40	
TRUE	AUD_GPIO_3	40 51	
TRUE	SPKRAMP_INR_N	40 51 72	
TRUE	SPKRAMP_INR_P	40 51 72	
TRUE	USB_EXTB_N	24 40 68	
TRUE	USB_EXTB_P	24 40 68	
TRUE	USB3_EXTB_TX_C_N	40 68	
TRUE	USB3_EXTB_TX_C_P	40 68	
TRUE	USB3_EXTB_RX_RC_N	40 68	
TRUE	USB3_EXTB_RX_RC_P	40 68	
TRUE	USB_CAMERA_N	18 40 68	
TRUE	USB_CAMERA_P	18 40 68	
TRUE	HDA_SDOUT	16 40 69	
TRUE	HDA_BIT_CLK	16 40 69	
TRUE	HDA_SDIN0	16 40 69	
TRUE	USB_EXTB_OC_L		
TRUE	HDA_RST_L	16 40 69	
TRUE	HDA_SYNC	16 40 69	

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST

TRUE	PP3V3_SW_SD_PWR	33
TRUE	SD_CLK	33
TRUE	SD_CMD	33
TRUE	SD_D<7..0>	33
TRUE	SD_CD_L	33
TRUE	SD_WP	33

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	? 63
TRUE	=PP5V_S0_LPCPLUS	? 63
TRUE	LPC_AD<3..0>	16 41 63 69
TRUE	SPI_ALT_MOSI	63
TRUE	SPI_ALT_MISO	63
TRUE	LPC_FRAME_L	16 41 63 69
TRUE	PM_CLKRUN_L	17 41 63
TRUE	SMC_TMS	41 42 63
TRUE	LPCPLUS_RESET_L	25 63 69
TRUE	SMC_TDO	41 42 63
TRUE	TP_SMC_TEST_L	63
TRUE	TP_SMC_MD1	63
TRUE	SMC_TX_L	41 42 63
TRUE	LPC_CLK33M_LPCPLUS	25 63 69
TRUE	SPIROM_USE_MLB	19 63
TRUE	SPI_ALT_CLK	63
TRUE	SPI_ALT_CS_L	63
TRUE	LPC_SERIRQ	16 41 63
TRUE	LPC_PWRDWN_L	17 25 41 63
TRUE	SMC_TDI	41 42 63
TRUE	SMC_TCK	41 42 63
TRUE	SMC_RESET_L	41 42 63 53
TRUE	SMC_ROMBOOT	42 63
TRUE	SMC_RX_L	41 42 63
TRUE	LPCPLUS_GPIO	19 63

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

TRUE	=PP5V_S0_FAN	? 48	
TRUE	FAN_RT_TACH	48	
TRUE	FAN_RT_PWM	48	

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_TPAD_CONN	49	
TRUE	PP5V_TPAD_FILT	49	
TRUE	=PP3V42_G3H_TPAD	? 49	
TRUE	USB_TPAD_CONN_P	48	
TRUE	USB_TPAD_CONN_N	48	
TRUE	=I2C_TPAD_SDA	44 49	
TRUE	=I2C_TPAD_SCL	44 49	
TRUE	SMC_ONOFF_L	41 42 49	
TRUE	SMC_LID	6 40 41 42 49	
TRUE	SMC_TPAD_RST_L	42 49	
TRUE	SMC_PME_S4_WAKE_L	41 42 49	

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P	51 52 72	
TRUE	SPKRAMP_ROUT_N	51 52 72	

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	52 53	(Need 4 TPs)
TRUE	=SMBUS_BATT_SCL	44 52	
TRUE	=SMBUS_BATT_SDA	44 52	
TRUE	SYS_DETECT_L	52	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

TRUE	PPVOUT_SW_LCDBKLT	43 65	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	63	(Need 2 TPs)
TRUE	I2C_TCON_SDA_R	63	
TRUE	I2C_TCON_SCL_R	63	
TRUE	LED_RETURN_6	63 65	
TRUE	LED_RETURN_5	63 65	
TRUE	LED_RETURN_4	63 65	
TRUE	LED_RETURN_3	63 65	
TRUE	LED_RETURN_2	63 65	
TRUE	LED_RETURN_1	63 65	
TRUE	DP_INT_HPD_CONN	63	
TRUE	DP_INT_AUX_CH_C_N	63 66	
TRUE	DP_INT_AUX_CH_C_P	63 66	
TRUE	DP_INT_ML_F_P<0>	63 66	
TRUE	DP_INT_ML_F_N<0>	63 66	
TRUE	DP_INT_ML_F_P<1>	66	
TRUE	DP_INT_ML_F_N<1>	66	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H	? 52	
TRUE	PPVIN_SW_TBTBST	? 36	
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	?	
TRUE	PPDCIN_G3H	?	
TRUE	PP3V42_G3H	?	
TRUE	PPVRTC_G3H	?	
TRUE	PP5V_S5	?	
TRUE	PP5V_SUS	?	
TRUE	PP3V3_S5	? 72	
TRUE	PP3V3_SUS	?	
TRUE	PP3V3_S3	?	
TRUE	PP1V8_S0	?	
TRUE	PP3V3_S0	? 72	
TRUE	PP1V5_S3	? 67	
TRUE	PP1V5_S3RS0	? 67	
TRUE	PP1V5_S0	?	
TRUE	PP1V05_S0	?	
TRUE	PPVTTDDR_S3	?	
TRUE	PP0V75_S0_DDRVTT	?	
TRUE	PPVCCSA_S0_CPU	?	
TRUE	PP1V05_SUS	?	
TRUE	PP15V_TBT	?	
TRUE	PP3V3_TBTLC	?	
TRUE	PP1V05_TBTLC	? 26	
TRUE	PP1V05_S0_PCH_VCCADPLL	?	
TRUE	PPVCORE_S0_CPU	?	
TRUE	PPVCORE_S0_AXG	?	
TRUE	PP1V5_S3_CPU_VCCDQ	?	
TRUE	PP1V05_S0_CPU_VCCPQE	?	
TRUE	PP1V8_S0_CPU_VCCPLL_R	?	
TRUE	PP1V05_TBTCIO	?	
TRUE	PPBUS_S5_HS_OTHER_ISNS	?	
TRUE	PPDCIN_G3H_ISOL	?	
TRUE	PP5V_S3	?	
TRUE	PP5V_S0	?	
TRUE	PP3V3_S4	?	

(Need to add 27 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

TRUE	PP3V3_S0_SSD_FLT	28	(Need 5 TPs)
TRUE	SATA_SSD_D2R_P	28 68	
TRUE	SATA_SSD_D2R_N	28 68	
TRUE	SMC_OOB1_RX_L	28 41	
TRUE	SMC_OOB1_TX_L	28 41 42	
TRUE	PCIE_CLK100M_SSD_P	16 28 66	
TRUE	PCIE_CLK100M_SSD_N	16 28 66	
TRUE	PCIE_SSD_R2D_P<1>	28 66	
TRUE	PCIE_SSD_R2D_N<1>	28 66	
TRUE	PCIE_SSD_D2R_P<1>	8 28 66	
TRUE	PCIE_SSD_D2R_N<1>	8 28 66	
TRUE	SATA_SSD_R2D_N	28 68	
TRUE	SATA_SSD_R2D_P	28 68	
TRUE	SSD_CLKREQ_L	16 28	
TRUE	SATA_PCIE_SEL	28	
TRUE	SSD_P3V3S0_EN	28	
TRUE	SSD_RESET_L	25 28	

(Need to add 6 GND TPs)

J6900: DC-In Connector

FUNC_TEST

TRUE	=PP18V5_DCIN_CONN	? 52	(Need 6 TPs)
TRUE	=PP5V_S3_LIO_CONN	? 52	

(Need to add 5 GND TPs)

NO_TEST Nets

POWER SIGNALS

TRUE	VCCSAS0_SREF	54	
TRUE	VCCSAS0_SET1_R	54	
TRUE	VCCSAS0_SET0	54	
TRUE	VCCSAS0_SET1	54	

NO_TEST

TRUE	TP_CRT_IG_BLUE	MAKE_BASE=TRUE	NC_CRT_IG_BLUE
TRUE	TP_CRT_IG_GREEN	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
TRUE	TP_CRT_IG_RED	MAKE_BASE=TRUE	NC_CRT_IG_RED
TRUE	TP_CRT_IG_DDC_CLK	MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
TRUE	TP_CRT_IG_DDC_DATA	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
TRUE	TP_CRT_IG_HSYNC	MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
TRUE	TP_CRT_IG_VSYNC	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
TRUE	TP_LVDS_IG_CTRL_CLK	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
TRUE	TP_LVDS_IG_CTRL_DATA	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
TRUE	TP_PCH_LVDS_VBG	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
TRUE	TP_HDA_SDIN1	MAKE_BASE=TRUE	NC_HDA_SDIN1
TRUE	TP_HDA_SDIN2	MAKE_BASE=TRUE	NC_HDA_SDIN2
TRUE	TP_HDA_SDIN3	MAKE_BASE=TRUE	NC_HDA_SDIN3
TRUE	TP_PCI_PME_L	MAKE_BASE=TRUE	NC_PCI_PME_L
TRUE	TP_PCI_CLK33M_OUT3	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
TRUE	TP_CLINK_CLK	MAKE_BASE=TRUE	NC_CLINK_CLK
TRUE	TP_CLINK_DATA	MAKE_BASE=TRUE	NC_CLINK_DATA
TRUE	TP_CLINK_RESET_L	MAKE_BASE=TRUE	NC_CLINK_RESET_L
TRUE	TP_PCIE_CLK100M_PERN	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PERN
TRUE	TP_PCIE_CLK100M_PERP	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PERP
TRUE	XDP_PCH_AP_PWR_EN		
TRUE	XDP_PCH_USB_HUB_SOFT_RST_L		
TRUE	XDP_PCH_SDCONN_STATE_RST_L		
TRUE	XDP_PCH_ENET_PWR_EN		
TRUE	XDP_PCH_SDCONN_DET_L		
TRUE	XDP_PCH_S5_PWRGD	23	
TRUE	XDP_PCH_PWRBTN_L	23	
TRUE	XDP_PCH_ISOLATE_CPU_MEM_L		
TRUE	XDP_PM_CLKREQ_L		
TRUE	XDP_AP_CLKREQ_L		
TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN		
TRUE	TP_SDVO_TVCLKINN	MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
TRUE	TP_SDVO_TVCLKINP	MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
TRUE	TP_SDVO_STALLN	MAKE_BASE=TRUE	NC_SDVO_STALLN
TRUE	TP_SDVO_STALLP	MAKE_BASE=TRUE	NC_SDVO_STALLP
TRUE	TP_SDVO_INTN	MAKE_BASE=TRUE	NC_SDVO_INTN
TRUE	TP_SDVO_INTP	MAKE_BASE=TRUE	NC_SDVO_INTP
TRUE	TP_XDP_PCH_OBSFN_A<0..1>	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
TRUE	TP_XDP_PCH_OBSFN_B<0..1>	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
TRUE	TP_XDPPCH_HOOK2	MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
TRUE	TP_XDPPCH_HOOK3	MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
TRUE	TP_XDP_PCH_OBSFN_C<0..1>	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_C<0..1>
TRUE	TP_XDP_PCH_HOOK4	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
TRUE	TP_XDP_PCH_HOOK5	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
TRUE	TP_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
TRUE	TP_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
TRUE	TP_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
TRUE	TP_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC_EDP_TXP<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_P<0..3>	9
NC_EDP_TXN<0..3> MAKE_BASE=TRUE	TRUE	TP_EDP_TX_N<0..3>	9
NC_EDP_AUXP MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_P	
NC_EDP_AUXN MAKE_BASE=TRUE	TRUE	TP_EDP_AUX_N	
NC_CPU_THERMDA MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDA	
NC_CPU_THERMDC MAKE_BASE=TRUE	TRUE	TP_CPU_THERMDC	
NC_CPU_RSVD<30..45> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<30..45>	
NC_CPU_RSVD<8..27> MAKE_BASE=TRUE	TRUE	TP_CPU_RSVD<8..27>	
NC_PEG_R2D_CP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_P<15..2>	9
NC_PEG_R2D_CN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_R2D_C_N<15..2>	9
NC_PEG_D2RP<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_P<15..2>	9
NC_PEG_D2RN<15..2> MAKE_BASE=TRUE	TRUE	=PEG_D2R_N<15..2>	9

16 TP_PCIE_CLK100M_PE4N	TRUE	NC_PCIE_CLK100M_PE4N	
16 TP_PCIE_CLK100M_PE4P	TRUE	NC_PCIE_CLK100M_PE4P	
TP_PCIE_CLK100M_PE5N	TRUE	NC_PCIE_CLK100M_PE5N	
TP_PCIE_CLK100M_PE5P	TRUE	NC_PCIE_CLK100M_PE5P	
TP_PCIE_CLK100M_PE6N	TRUE	NC_PCIE_CLK100M_PE6N	
TP_PCIE_CLK100M_PE6P	TRUE	NC_PCIE_CLK100M_PE6P	
TP_PCIE_CLK100M_PE7N	TRUE	NC_PCIE_CLK100M_PE7N	
TP_PCIE_CLK100M_PE7P	TRUE	NC_PCIE_CLK100M_PE7P	
TP_PSOC_P1_3	TRUE	NC_PSOC_P1_3	
TP_SATA_B_D2RN	TRUE	NC_SATA_B_D2RN	
TP_SATA_B_D2RP	TRUE	NC_SATA_B_D2RP	
TP_SATA_B_R2D_CN	TRUE	NC_SATA_B_R2D_CN	
TP_SATA_B_R2D_CP	TRUE	NC_SATA_B_R2D_CP	
16 TP_SATA_D_D2RN	TRUE	NC_SATA_D_D2RN	
16 TP_SATA_D_D2RP	TRUE	NC_SATA_D_D2RP	
16 TP_SATA_D_R2D_CN	TRUE	NC_SATA_D_R2D_CN	
16 TP_SATA_D_R2D_CP	TRUE	NC_SATA_D_R2D_CP	
16 TP_SATA_E_D2RN	TRUE	NC_SATA_E_D2RN	
16 TP_SATA_E_D2RP	TRUE	NC_SATA_E_D2RP	
16 TP_SATA_E_R2D_CN	TRUE	NC_SATA_E_R2D_CN	
16 TP_SATA_E_R2D_CP	TRUE	NC_SATA_E_R2D_CP	
16 TP_SATA_F_D2RN	TRUE	NC_SATA_F_D2RN	
16 TP_SATA_F_D2RP	TRUE	NC_SATA_F_D2RP	
16 TP_SATA_F_R2D_CN	TRUE	NC_SATA_F_R2D_CN	
16 TP_SATA_F_R2D_CP	TRUE	NC_SATA_F_R2D_CP	

TP_PCH_TP18	TRUE	NC_PCH_TP18	
TP_PCH_TP17	TRUE	NC_PCH_TP17	
TP_PCH_TP16	TRUE	NC_PCH_TP16	
TP_PCH_TP15	TRUE	NC_PCH_TP15	
TP_PCH_TP14	TRUE	NC_PCH_TP14	
TP_PCH_TP13	TRUE	NC_PCH_TP13	
TP_PCH_TP12	TRUE	NC_PCH_TP12	
TP_PCH_TP10	TRUE	NC_PCH_TP10	
TP_PCH_TP9	TRUE	NC_PCH_TP9	
TP_PCH_TP8	TRUE	NC_PCH_TP8	
TP_PCH_TP7	TRUE	NC_PCH_TP7	
TP_PCH_TP6	TRUE	NC_PCH_TP6	
TP_PCH_TP5	TRUE	NC_PCH_TP5	
TP_PCH_TP4	TRUE	NC_PCH_TP4	
TP_PCH_TP3	TRUE	NC_PCH_TP3	
TP_PCH_TP2	TRUE	NC_PCH_TP2	
TP_PCH_TP1	TRUE	NC_PCH_TP1	
PCH_VSS_NCTF<1>	TRUE	PCH_VSS_NCTF<15>	
PCH_VSS_NCTF<2>	TRUE	PCH_VSS_NCTF<17>	
PCH_VSS_NCTF<5>	TRUE	PCH_VSS_NCTF<19>	6
	TRUE	PCH_VSS_NCTF<19>	6
PCH_VSS_NCTF<9>	TRUE	PCH_VSS_NCTF<21>	
PCH_VSS_NCTF<11>	TRUE	PCH_VSS_NCTF<25>	
PCH_VSS_NCTF<12>	TRUE	PCH_VSS_NCTF<27>	
	TRUE	PCH_VSS_NCTF<29>	
TP_LVDS_IG_B_CLKN	TRUE	NC_LVDS_IG_B_CLKN	
TP_LVDS_IG_B_CLKP	TRUE	NC_LVDS_IG_B_CLKP	
TP_LVDS_IG_BKL_PWM	TRUE	NC_LVDS_IG_BKL_PWM	
SMC_BS_ALRT_L	TRUE	NC_SMC_BS_ALRT_L	

SYNC_MASTER=K21_MLB SYNC_DATE=07/29/2013

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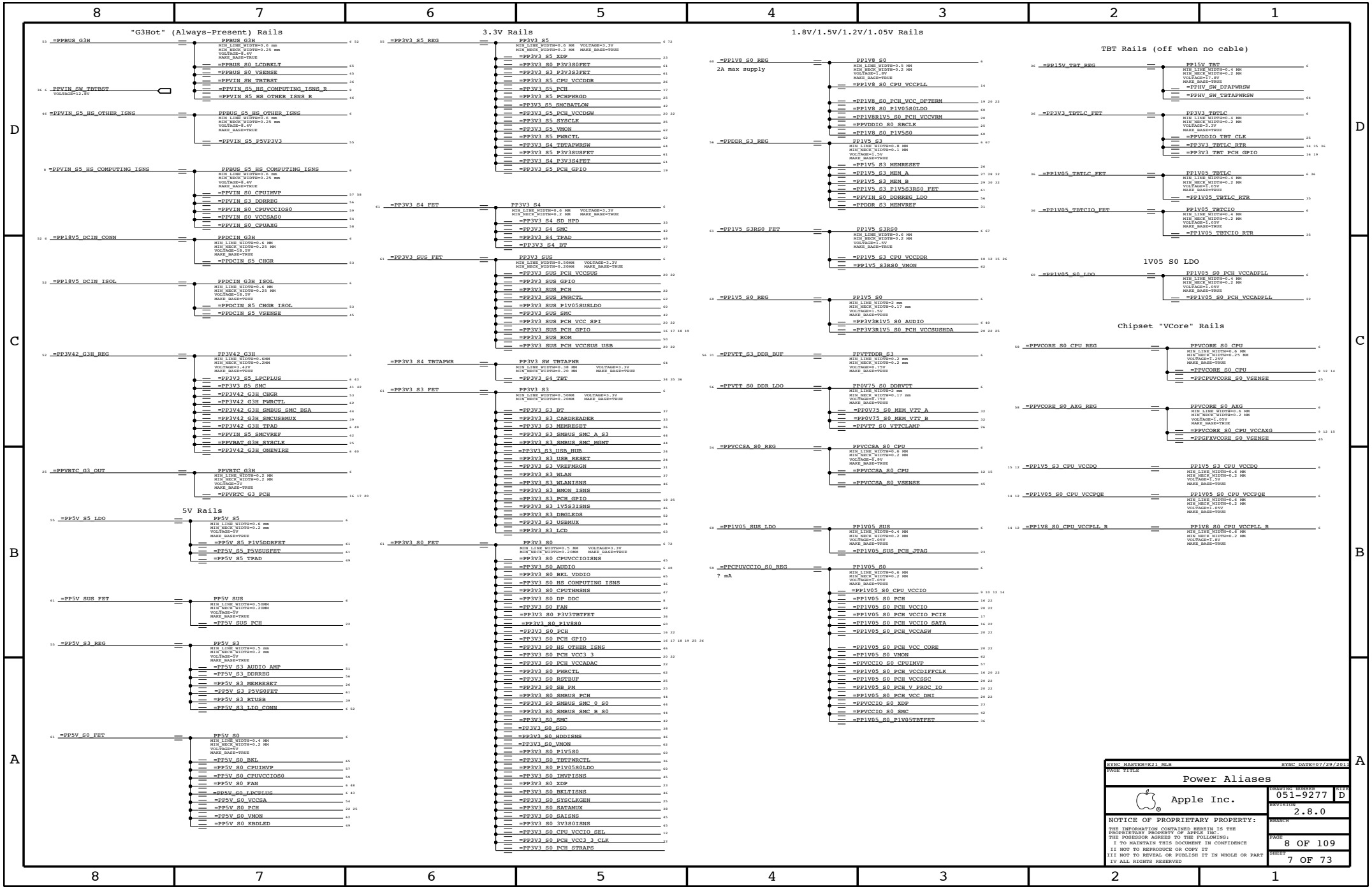
"G3Hot" (Always-Present) Rails
=PPBUS_G3H
PPBUS_G3H
=PPBUS_S0_LCDBKLT
=PPBUS_S0_VSENSE
=PPVIN_SW_TBTBST
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_OTHER_ISNS_R
=PPVIN_S5_HS_OTHER_ISNS
PPBUS_S5_HS_OTHER_ISNS
=PPVIN_S5_P5VP3V3
=PPVIN_S5_HS_COMPUTING_ISNS
PPBUS_S5_HS_COMPUTING_ISNS
=PPVIN_S0_CPUIMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_CPUVCCIOS0
=PPVIN_S0_VCCSAS0
=PPVIN_S0_CPUAXG
=PP18V5_DCIN_CONN
PPDCIN_G3H
=PPDCIN_S5_CHGR
=PP18V5_DCIN_ISOL
PPDCIN_G3H_ISOL
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE
=PP3V42_G3H_REG
PP3V42_G3H
=PP3V3_S5_LPCPLUS
=PP3V3_S5_SMC
=PP3V42_G3H_CHGR
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_TPAD
=PPVIN_S5_SMCVREF
=PPVBAT_G3H_SYSCLK
=PP3V42_G3H_ONEWIRE
=PPVRTC_G3_OUT
PPVRTC_G3H
=PPVRTC_G3_PCH
5V Rails
=PP5V_S5_LDO
PP5V_S5
=PP5V_S5_P1V5DDRFET
=PP5V_S5_P5VSUSFET
=PP5V_S5_TPAD
=PP5V_SUS_FET
PP5V_SUS
=PP5V_SUS_PCH
=PP5V_S3_REG
PP5V_S3
=PP5V_S3_AUDIO_AMP
=PP5V_S3_DDRREG
=PP5V_S3_MEMRESET
=PP5V_S3_P5VS0FET
=PP5V_S3_RTUSB
=PP5V_S3_LIO_CONN
=PP5V_S0_FET
PP5V_S0
=PP5V_S0_BKL
=PP5V_S0_CPUIMVP
=PP5V_S0_CPUVCCIOS0
=PP5V_S0_FAN
=PP5V_S0_LPCPLUS
=PP5V_S0_VCCSA
=PP5V_S0_PCH
=PP5V_S0_VMON
=PP5V_S0_KBDLED
3.3V Rails
=PP3V3_S5_REG
PP3V3_S5
=PP3V3_S5_XDP
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_PCH
=PP3V3_S5_PCHPWRGD
=PP3V3_S5_SMCBATLOW
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_PWRCTL
=PP3V3_S4_TBTAPWRSW
=PP3V3_S5_P3V3SUSFET
=PP3V3_S4_P3V3S4FET
=PP3V3_S5_PCH_GPIO
=PP3V3_S4_FET
PP3V3_S4
=PP3V3_S4_SD_HPD
=PP3V3_S4_SMC
=PP3V3_S4_TPAD
=PP3V3_S4_BT
=PP3V3_SUS_FET
PP3V3_SUS
=PP3V3_SUS_PCH_VCCSUS
=PP3V3_SUS_GPIO
=PP3V3_SUS_PCH
=PP3V3_SUS_PWRCTL
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_SMC
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_S4_TBTAPWR
PP3V3_SW_TBTAPWR
=PP3V3_S4_TBT
=PP3V3_S3_FET
PP3V3_S3
=PP3V3_S3_BT
=PP3V3_S3_CARDREADER
=PP3V3_S3_MEMRESET
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_SMBUS_SMC_MGMT
=PP1V3_S3_USB_HUB
=PP3V3_S3_USB_RESET
=PP3V3_S3_VREFMRGN
=PP3V3_S3_WLAN
=PP3V3_S3_WLANISNS
=PP3V3_S3_BMON_ISNS
=PP3V3_S3_PCH_GPIO
=PP3V3_S3_1VS3ISNS
=PP3V3_S3_DBGLEDS
=PP3V3_S3_USBMUX
=PP3V3_S3_LCD
=PP3V3_S0_FET
PP3V3_S0
=PP3V3_S0_CPUVCCIOISNS
=PP3V3_S0_AUDIO
=PP3V3_S0_BKL_VDDIO
=PP3V3_S0_HS_COMPUTING_ISNS
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_DP_DDC
=PP3V3_S0_FAN
=PP3V3_S0_P3V3TBTFET
=PP3V3_S0_P1V8S0
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_HS_OTHER_ISNS
=PP3V3_S0_PCH_VCC3_3
=PP3V3_S0_PCH_VCCADAC
=PP3V3_S0_PWRCTL
=PP3V3_S0_RSTBUF
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMC
=PP3V3_S0_SSD
=PP1V3_S0_HDDISNS
=PP3V3_S0_VMON
=PP3V3_S0_P1V5S0
=PP3V3_S0_TBTPWRCTL
=PP3V3_S0_P1V05S0LDO
=PP3V3_S0_IMVPISNS
=PP3V3_S0_XDP
=PP1V3_S0_BKLTISNS
=PP3V3_S0_SYSCLKGEN
=PP3V3_S0_SATAMUX
=PP3V3_S0_SAISNS
=PP3V3_S0_3V3S0ISNS
=PP3V3_S0_CPU_VCCIO_SEL
=PP3V3_S0_PCH_VCC3_3_CLK
=PP3V3_S0_PCH_STRAPS
1.8V/1.5V/1.2V/1.05V Rails
=PP1V8_S0_REG
2A max supply
PP1V8_S0
=PP1V8_S0_CPU_VCCPLL
=PP1V8_S0_PCH_VCC_DFTERM
=PP1V8_S0_P1V05S0LDO
=PP1V8R1V5_S0_PCH_VCCVRM
=PPVDDIO_S0_SBCLK
=PP1V8_S0_P1V5S0
=PPDDR_S3_REG
PP1V5_S3
=PP1V5_S3_MEMRESET
=PP1V5_S3_MEM_A
=PP1V5_S3_MEM_B
=PP1V5_S3_P1V5S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPDDR_S3_MEMVREF
=PP1V5_S3RS0_FET
PP1V5_S3RS0
=PP1V5_S3_CPU_VCCDDR
=PP1V5_S3RS0_VMON
=PP1V5_S0_REG
PP1V5_S0
=PP3V3R1V5_S0_AUDIO
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
=PPVTT_S0_DDR_LDO
PP0V75_S0_DDRVTT
=PP0V75_S0_MEM_VTT_A
=PP0V75_S0_MEM_VTT_B
=PPVFRT_S0_VTTCLAMP
=PPVCCSA_S0_REG
PPVCCSA_S0_CPU
=PPVCCSA_S0_CPU
=PPVCCSA_S0_VSENSE
=PP1V05_SUS_LDO
PP1V05_SUS
=PP1V05_SUS_PCH_JTAG
=PPCPUVCCIO_S0_REG
7 mA
PP1V05_S0
=PP1V05_S0_CPU_VCCIO
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_PCIE
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH_VCCASW
=PP1V05_S0_PCH_VCC_CORE
=PP1V05_S0_VMON
=PPVCCIO_S0_CPUIMVP
=PP1V05_S0_PCH_VCCDIFFCLK
=PP1V05_S0_PCH_VCCSSC
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0_PCH_VCC_DMI
=PPVCCIO_S0_XDP
=PPVCCIO_S0_SMC
=PP1V05_S0_P1V05TBTFET
TBT Rails (off when no cable)
=PP15V_TBT_REG
PP15V_TBT
=PP3V_SW_DPAPWRSW
=PPHV_SW_TBTAPWRSW
=PP3V3_TBTLC_FET
PP3V3_TBTLC
=PPVDDIO_TBT_CLK
=PP3V3_TBTLC_RTR
=PP3V3_TBT_PCH_GPIO
=PP1V05_TBTLC_FET
PP1V05_TBTLC
=PP1V05_TBTLC_RTR
=PP1V05_TBTCIO_FET
PP1V05_TBTCIO
=PP1V05_TBTCIO_RTR
1V05 S0 LDO
=PP1V05_S0_LDO
PP1V05_S0_PCH_VCCADPLL
=PP1V05_S0_PCH_VCCADPLL
Chipset "VCore" Rails
=PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
=PPVCORE_S0_CPU
=PPCPUVCORE_S0_VSENSE
=PPVCORE_S0_AXG_REG
PPVCORE_S0_AXG
=PPVCORE_S0_CPU_VCCAXG
=PPGFXVCORE_S0_VSENSE
=PP1V5_S3_CPU_VCCDQ
PP1V5_S3_CPU_VCCDQ
=PP1V05_S0_CPU_VCCPQE
PP1V05_S0_CPU_VCCPQE
=PP1V8_S0_CPU_VCCPLL_R
PP1V8_S0_CPU_VCCPLL_R
SYNC MASTER=K21_MLB
SYNC DATE=07/29/2013
PAGE TITLE
Power Aliases
Apple Inc.
DRAWING NUMBER
051-9277
SIZE
D
REVISION
2.8.0
BRANCH
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Plated Board Slot

SL0900 TH-NSP

SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM

Z0910 STDOFF-4.5OD1.8H-SM

Z0911 STDOFF-4.5OD1.8H-SM

Z0912 STDOFF-4.5OD1.8H-SM

4x 860-1327

Fan Boss

Z0905 STDOFF-4.5OD1.8H-SM

860-1327

X21 Boss

Z0914 STDOFF-4.5OD1.9H-SM

860-1327

SSD Boss

Z0915 STDOFF-4.5OD1.9H-SM

860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL

ZS0905 POGO-2.0OD-3.6H-K86-K87 SM

870-1938

USB/SD Card Pogo

CRITICAL

ZS0906 POGO-2.0OD-3.6H-K86-K87 SM

870-1938

Digital Ground

GND

VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

Can Slots

SL0901 TH-NSP — SL-1.1X0.4-1.4X0.7

SL0902 TH-NSP — SL-1.1X0.4-1.4X0.7

2x TBT pin diodes

SL0903 TH-NSP — SL-1.1X0.4-1.4X0.7

SL0906 TH-NSP — SL-1.1X0.4-1.4X0.7

2x MDP Connector

SL0905 TH-NSP — SL-1.1X0.45-1.4X0.75

SL0907 TH-NSP — SL-1.1X0.45-1.4X0.75

2x TBT chip

SL0904 TH-NSP — SL-1.1X0.4-1.4X0.7

SL0908 TH-NSP — SL-1.1X0.4-1.4X0.7

2x USB Connector

Unused PPT

PCIE_CLK100M_ENET_N	NC_PCIE_CLK100M_ENET_N	NO_TEST=TRUE
PCIE_CLK100M_ENET_P	NC_PCIE_CLK100M_ENET_P	NO_TEST=TRUE
PCIE_CLK100M_FW_N	NC_PCIE_CLK100M_FW_N	NO_TEST=TRUE
PCIE_CLK100M_FW_P	NC_PCIE_CLK100M_FW_P	NO_TEST=TRUE
PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	NO_TEST=TRUE
PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	NO_TEST=TRUE
PEG_CLK100M_N	NC_PEG_CLK100M_N	NO_TEST=TRUE
PEG_CLK100M_P	NC_PEG_CLK100M_P	NO_TEST=TRUE
PCIE_ENET_D2R_N	NC_PCIE_ENET_D2R_N	NO_TEST=TRUE
PCIE_ENET_D2R_P	NC_PCIE_ENET_D2R_P	NO_TEST=TRUE
PCIE_ENET_R2D_C_N	NC_PCIE_ENET_R2D_C_N	NO_TEST=TRUE
PCIE_ENET_R2D_C_P	NC_PCIE_ENET_R2D_C_P	NO_TEST=TRUE
PCIE_FW_D2R_N	NC_PCIE_FW_D2R_N	NO_TEST=TRUE
PCIE_FW_D2R_P	NC_PCIE_FW_D2R_P	NO_TEST=TRUE
PCIE_FW_R2D_C_N	NC_PCIE_FW_R2D_C_N	NO_TEST=TRUE
PCIE_FW_R2D_C_P	NC_PCIE_FW_R2D_C_P	NO_TEST=TRUE
PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	NO_TEST=TRUE
PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	NO_TEST=TRUE
PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	NO_TEST=TRUE
PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	NO_TEST=TRUE

MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1>	
MEM_A_CLK_N<1>	TP_MEM_A_CLKN<1>	
MEM_B_CLK_P<1>	TP_MEM_B_CLKP<1>	
MEM_B_CLK_N<1>	TP_MEM_B_CLKN<1>	

ENET_LOW_PWR_PCH	XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH	
SATARDRVR_EN	XDP_DC3_PCH_GPIO19_SATARDRVR_EN	
TP_PCH_CLKOUT_DPN	DPLL_REF_CLK_N — DPLL_REF_CLKN	
TP_PCH_CLKOUT_DPP	DPLL_REF_CLK_P — DPLL_REF_CLKP	

Unused USB

USB_EXTC_P	NC_USB_EXTC_P	NO_TEST=TRUE
USB_EXTC_N	NC_USB_EXTC_N	NO_TEST=TRUE
USB3_EXTC_RX_P	NC_USB3_EXTC_RX_P	NO_TEST=TRUE
USB3_EXTC_RX_N	NC_USB3_EXTC_RX_N	NO_TEST=TRUE
USB3_EXTC_TX_P	NC_USB3_EXTC_TX_P	NO_TEST=TRUE
USB3_EXTC_TX_N	NC_USB3_EXTC_TX_N	NO_TEST=TRUE
USB3_EXTD_RX_P	NC_USB3_EXTD_RX_P	NO_TEST=TRUE
USB3_EXTD_RX_N	NC_USB3_EXTD_RX_N	NO_TEST=TRUE
USB3_EXTD_TX_P	NC_USB3_EXTD_TX_P	NO_TEST=TRUE
USB3_EXTD_TX_N	NC_USB3_EXTD_TX_N	NO_TEST=TRUE
USB_EXTD_EHCI_N	NC_USB_EXTD_EHCI_N	NO_TEST=TRUE
USB_EXTD_EHCI_P	NC_USB_EXTD_EHCI_P	NO_TEST=TRUE

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE	P1V5S3RS0_RAMP_DONE	PM 61
TP_DDRREG_PGOOD	DDRREG_PGOOD	PM 56

SATA Aliases

Unused SATA ODD Signals

SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP	NO_TEST=TRUE
SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN	NO_TEST=TRUE
SATA_ODD_D2R_P	NC_SATA_ODD_D2RP	NO_TEST=TRUE
SATA_ODD_D2R_N	NC_SATA_ODD_D2RN	NO_TEST=TRUE

SSD PCIE Signals

-PEG_D2R_P<1..0>	PCIE_SSD_D2R_P<1..0>	SSD0 4 38 66
-PEG_D2R_N<1..0>	PCIE_SSD_D2R_N<1..0>	SSD0 4 38 66
-PEG_R2D_C_P<1..0>	PCIE_SSD_R2D_C_P<1..0>	SSD0 38 66
-PEG_R2D_C_N<1..0>	PCIE_SSD_R2D_C_N<1..0>	SSD0 38 66

CPU signals

MEMVTT_EN — =DDRVTT_EN

=PP3V3_S0_DP_DDC

R0920[1] 2.2K 5% 1/20W MF 201-2
R0921[1] 2.2K 5% 1/20W MF 201-2
R0922[1] 2.2K 5% 1/20W MF 201-2
R0923[1] 2.2K 5% 1/20W MF 201-2

NO STUFF NO STUFF

TP_DP_IG_C_CTRL_CLK	DPB_IG_DDC_CLK	
TP_DP_IG_C_CTRL_DATA	DPB_IG_DDC_DATA	
TP_DP_IG_D_CTRL_CLK	DP_IG_D_CTRL_CLK	
TP_DP_IG_D_CTRL_DATA	DP_IG_D_CTRL_DATA	

=PP3V3_S0_DP_DDC

R0924[1] 470K 1% 1/20W MF 201-2
R0925[1] 470K 1% 1/20W MF 201-2

DP_TBTSNK0_DDC_CLK	DPA_IG_DDC_CLK	
DP_TBTSNK0_DDC_DATA	DPA_IG_DDC_DATA	

CRITICAL
R0910 0.01 0.5% 1W MF 0612-1

PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL

MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V

ISNS_LCDBKLT_P
ISNS_LCDBKLT_N

=PPBUS_SW_BKL

CRITICAL
R0954 0.002 1% 1W MF 0612

=PPVIN_S5_HS_COMPUTING_ISNS — =PPVIN_S5_HS_COMPUTING_ISNS_R

ISNS_HS_COMPUTING_N
ISNS_HS_COMPUTING_P

MLB_RAMCFG3
MLB_RAMCFG2
MLB_RAMCFG1
MLB_RAMCFG0

RAMCFG3:L R0950[1] 10K 5% 1/20W MF 201-2
RAMCFG2:L R0951 10K 5% 1/20W MF 201-2
RAMCFG1:L R0952 10K 5% 1/20W MF 201-2
RAMCFG0:L R0953 10K 5% 1/20W MF 201-2

LVDS Aliases

TP_LVDS_IG_B_CLKP	LVDS_IG_B_CLK_P	
TP_LVDS_IG_B_CLKN	LVDS_IG_B_CLK_N	
NC_LVDS_IG_B_DATAP<0..3>	LVDS_IG_B_DATA_P<0..3>	NO_TEST=TRUE
NC_LVDS_IG_B_DATAN<0..3>	LVDS_IG_B_DATA_N<0..3>	NO_TEST=TRUE
NC_LVDS_IG_A_DATAP<3>	LVDS_IG_A_DATA_P<3>	NO_TEST=TRUE
NC_LVDS_IG_A_DATAN<3>	LVDS_IG_A_DATA_N<3>	NO_TEST=TRUE
LCD_BKLT_PWM	LVDS_IG_BKL_PWM	
LCD_IG_PWR_EN	LVDS_IG_PANEL_PWR	
LCD_BKLT_EN	LVDS_IG_BKL_ON	

SMC Aliases

Unused SMC Signals

SMC_SYS_LED	NC_SMC_SYS_LED	NO_TEST=TRUE
IR_RX_OUT_RC	NC_IR_RX_OUT_RC	NO_TEST=TRUE

TP_DP_IG_D_HPD — DP_IG_D_HPD

R0909[1] 100K 5% 1/20W MF 201-2

NC_PCIE_5_R2D_CP	PCIE_TBT_R2D_C_P<0>	
NC_PCIE_6_R2D_CP	PCIE_TBT_R2D_C_P<1>	
NC_PCIE_7_R2D_CP	PCIE_TBT_R2D_C_P<2>	
NC_PCIE_8_R2D_CP	PCIE_TBT_R2D_C_P<3>	
NC_PCIE_5_R2D_CN	PCIE_TBT_R2D_C_N<0>	
NC_PCIE_6_R2D_CN	PCIE_TBT_R2D_C_N<1>	
NC_PCIE_7_R2D_CN	PCIE_TBT_R2D_C_N<2>	
NC_PCIE_8_R2D_CN	PCIE_TBT_R2D_C_N<3>	
NC_PCIE_5_D2RP	PCIE_TBT_D2R_P<0>	
NC_PCIE_6_D2RP	PCIE_TBT_D2R_P<1>	
NC_PCIE_7_D2RP	PCIE_TBT_D2R_P<2>	
NC_PCIE_8_D2RP	PCIE_TBT_D2R_P<3>	
NC_PCIE_5_D2RN	PCIE_TBT_D2R_N<0>	
NC_PCIE_6_D2RN	PCIE_TBT_D2R_N<1>	
NC_PCIE_7_D2RN	PCIE_TBT_D2R_N<2>	
NC_PCIE_8_D2RN	PCIE_TBT_D2R_N<3>	

TBT DP Ports

DPB_IG_HPD	DP_TBTSNK1_HPD	
DPA_IG_HPD	DP_TBTSNK0_HPD	
DP_TBTSNK0_AUXCH_C_P	DPA_IG_AUX_CH_P	
DP_TBTSNK0_AUXCH_C_N	DPA_IG_AUX_CH_N	
DP_TBTSNK1_AUXCH_C_P	DPB_IG_AUX_CH_P	
DP_TBTSNK1_AUXCH_C_N	DPB_IG_AUX_CH_N	
DP_TBTSNK1_ML_C_P<3..0>	TP_DP_IG_C_MLP<3..0>	
DP_TBTSNK1_ML_C_N<3..0>	TP_DP_IG_C_MLN<3..0>	
DP_TBTSNK0_ML_C_P<3..0>	TP_DP_IG_B_MLP<3..0>	
DP_TBTSNK0_ML_C_N<3..0>	TP_DP_IG_B_MLN<3..0>	
DP_TBTPB_ML_C_P<1>	NC_DP_TBTPB_ML_C_P<1>	
DP_TBTPB_ML_C_N<1>	NC_DP_TBTPB_ML_C_N<1>	
DP_TBTPB_ML_C_P<3>	NC_DP_TBTPB_ML_C_P<3>	
DP_TBTPB_ML_C_N<3>	NC_DP_TBTPB_ML_C_N<3>	
DP_TBTPB_AUXCH_C_P	NC_DP_TBTPB_AUXCH_C_P	
DP_TBTPB_AUXCH_C_N	NC_DP_TBTPB_AUXCH_C_N	

TBT_B_R2D_C_N<0>	NC_TBT_B_R2D_C_N<0>	NO_TEST=TRUE
TBT_B_R2D_C_P<0>	NC_TBT_B_R2D_C_P<0>	NO_TEST=TRUE
TBT_B_R2D_C_N<1>	NC_TBT_B_R2D_C_N<1>	NO_TEST=TRUE
TBT_B_R2D_C_P<1>	NC_TBT_B_R2D_C_P<1>	NO_TEST=TRUE
TBT_B_D2R_P<0>	NC_TBT_B_D2R_P<0>	NO_TEST=TRUE
TBT_B_D2R_N<0>	NC_TBT_B_D2R_N<0>	NO_TEST=TRUE
TBT_B_D2R_P<1>	NC_TBT_B_D2R_P<1>	NO_TEST=TRUE
TBT_B_D2R_N<1>	NC_TBT_B_D2R_N<1>	NO_TEST=TRUE

TBT_B_CIO_SEL
DP_TBTPB_HPD
TBT_B_CONFIG2_RC
TBT_B_CONFIG1_BUF
TBT_B_LSRX

R0916 10K 5% 1/20W MF 201-2
R0917 10K 5% 1/20W MF 201-2
R0918 10K 5% 1/20W MF 201-2
R0919 10K 5% 1/20W MF 201-2
R0914 10K 5% 1/20W MF 201-2

TBT_B_LSTX — NC_TBT_B_LSTX

SYNC_MASTER=J13_MLB_NON_POR — SYNC_DATE=11/10/2011

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-9277 — SIZE: D
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NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

OMIT_TABLE
CRITICAL

U1000
IVY-BRIDGE
2C-35W
BGA
(1 OF 9)

DMI
INTEL FLEXIBLE DISPLAY INTERFACE SIGNALS
PCI EXPRESS BASED INTERFACE SIGNALS
EMBEDDED DISPLAY PORT

DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>

FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
FDI_DATA_N<3>
FDI_DATA_N<4>
FDI_DATA_N<5>
FDI_DATA_N<6>
FDI_DATA_N<7>
FDI_DATA_P<0>
FDI_DATA_P<1>
FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_INT
FDI_LSYNC<0>
FDI_LSYNC<1>
EDP_COMP

EDP_HPD_L
DP_INT_AUX_CH_N
DP_INT_AUX_CH_P
DP_INT_ML_N<0>
TP_EDP_TX_N<1>
TP_EDP_TX_N<2>
TP_EDP_TX_N<3>
DP_INT_ML_P<0>
TP_EDP_TX_P<1>
TP_EDP_TX_P<2>
TP_EDP_TX_P<3>

=PP1V05_S0_CPU_VCCIO
R1030 24.9 1% 1/20W MF 201
PLACE_NEAR=U1000.AF3:12.7MM

R1010 24.9 1% 1/20W MF 201
CPU_PEG_COMP
=PP1V05_S0_CPU_VCCIO
PLACE_NEAR=U1000.G3:12.7MM

PEG_ICOMPI
PEG_ICOMPO
PEG_RCOMPO

PEG_RX_0*
PEG_RX_1*
PEG_RX_2*
PEG_RX_3*
PEG_RX_4*
PEG_RX_5*
PEG_RX_6*
PEG_RX_7*
PEG_RX_8*
PEG_RX_9*
PEG_RX_10*
PEG_RX_11*
PEG_RX_12*
PEG_RX_13*
PEG_RX_14*
PEG_RX_15*

PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15

=PEG_D2R_N<0>
=PEG_D2R_N<1>
=PEG_D2R_N<2>
=PEG_D2R_N<3>
=PEG_D2R_N<4>
=PEG_D2R_N<5>
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=PEG_D2R_P<0>
=PEG_D2R_P<1>
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=PEG_D2R_P<3>
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=PEG_D2R_P<11>
=PEG_D2R_P<12>
=PEG_D2R_P<13>
=PEG_D2R_P<14>
=PEG_D2R_P<15>

PEG_TX_0*
PEG_TX_1*
PEG_TX_2*
PEG_TX_3*
PEG_TX_4*
PEG_TX_5*
PEG_TX_6*
PEG_TX_7*
PEG_TX_8*
PEG_TX_9*
PEG_TX_10*
PEG_TX_11*
PEG_TX_12*
PEG_TX_13*
PEG_TX_14*
PEG_TX_15*

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

=PEG_R2D_C_N<0>
=PEG_R2D_C_N<1>
=PEG_R2D_C_N<2>
=PEG_R2D_C_N<3>
=PEG_R2D_C_N<4>
=PEG_R2D_C_N<5>
=PEG_R2D_C_N<6>
=PEG_R2D_C_N<7>
=PEG_R2D_C_N<8>
=PEG_R2D_C_N<9>
=PEG_R2D_C_N<10>
=PEG_R2D_C_N<11>
=PEG_R2D_C_N<12>
=PEG_R2D_C_N<13>
=PEG_R2D_C_N<14>
=PEG_R2D_C_N<15>
=PEG_R2D_C_P<0>
=PEG_R2D_C_P<1>
=PEG_R2D_C_P<2>
=PEG_R2D_C_P<3>
=PEG_R2D_C_P<4>
=PEG_R2D_C_P<5>
=PEG_R2D_C_P<6>
=PEG_R2D_C_P<7>
=PEG_R2D_C_P<8>
=PEG_R2D_C_P<9>
=PEG_R2D_C_P<10>
=PEG_R2D_C_P<11>
=PEG_R2D_C_P<12>
=PEG_R2D_C_P<13>
=PEG_R2D_C_P<14>
=PEG_R2D_C_P<15>

Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active High signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kohm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

PLACE_NEAR=U1000.H43:50.8MM
PLACE_SIDE=BOTTOM
=PPVCORE_S0_CPU
=PPVCORE_S0_CPU_VCCAXG
R1064 49.9 1% 1/16W MF-LF 402
R1070 49.9 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.H45:50.8MM
PLACE_SIDE=BOTTOM

CPU_VCC_VALSENSE_P
CPU_VCC_VALSENSE_N
Note. VOLTAGE=1.25V
Note. VOLTAGE=0V
CPU_AXG_VALSENSE_P
CPU_AXG_VALSENSE_N
Note. VOLTAGE=1.05V
Note. VOLTAGE=0V
TP_CPU_VCC_DIF_SENSE

R1065 49.9 1% 1/16W MF-LF 402
R1071 49.9 1% 1/16W MF-LF 402
PLACE_NEAR=U1000.K45:50.8MM
PLACE_SIDE=BOTTOM
PLACE_NEAR=U1000.K43:50.8MM
PLACE_SIDE=BOTTOM

CPU_THERMD_P
CPU_THERMD_N

NOTE: Intel does not recommend to use this analog sense due to accuracy concern.

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

OMIT_TABLE
CRITICAL

U1000
BGA
(5 OF 9)
RESERVED
IVY-BRIDGE
2C-35W

CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
CPU_CFG<16>
CPU_CFG<17>

CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
PPCPU_MEM_VREFDQ_A
PPCPU_MEM_VREFDQ_B

RSVD_30
RSVD_31
RSVD_32
RSVD_33
RSVD_34
RSVD_35
RSVD_36
RSVD_37
RSVD_38
RSVD_39
RSVD_40
RSVD_41
RSVD_42
RSVD_43
RSVD_44
RSVD_45

VCC_VAL_SENSE
VSS_VAL_SENSE
VAXG_VAL_SENSE
VSSAXG_VAL_SENSE
VCC_DIF_SENSE
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
RSVD_16
RSVD_17
RSVD_18
RSVD_19
RSVD_20
RSVD_21
RSVD_22
RSVD_23
RSVD_24
RSVD_25
RSVD_26
RSVD_27

DC_TEST_A4 — TP_CPU_DC_TEST_A4
DC_TEST_C4 — CPU_DC_TEST_C4_D3
DC_TEST_D3
DC_TEST_D1 — TP_CPU_DC_TEST_D1
DC_TEST_A58 — TP_CPU_DC_TEST_A58
DC_TEST_A59 — CPU_DC_TEST_C59_A59
DC_TEST_C59
DC_TEST_A61 — CPU_DC_TEST_C61_A61
DC_TEST_C61
DC_TEST_D61 — TP_CPU_DC_TEST_D61
DC_TEST_BD61 — TP_CPU_DC_TEST_BD61
DC_TEST_BE61 — CPU_DC_TEST_BE59_BE61
DC_TEST_BE59
DC_TEST_BG61 — CPU_DC_TEST_BG59_BG61
DC_TEST_BG59
DC_TEST_BG58 — TP_CPU_DC_TEST_BG58
DC_TEST_BG4 — TP_CPU_DC_TEST_BG4
DC_TEST_BG3 — CPU_DC_TEST_C4_BE3_BG3
DC_TEST_BE3
DC_TEST_BG1 — CPU_DC_TEST_C4_BE1_BG1
DC_TEST_BE1
DC_TEST_BD1 — TP_CPU_DC_TEST_BD1

CPU_CFG<7>
CPU_CFG<6>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<2>
R1042 R1044 R1045 R1046 R1047 1K 5% 1/20W MF 201

CPU_CFG<16>
CPU_CFG<3>
CPU_CFG<1>
CPU_CFG<0>
R1040 R1041 R1043 R1049 1K 5% 1/20W MF 201

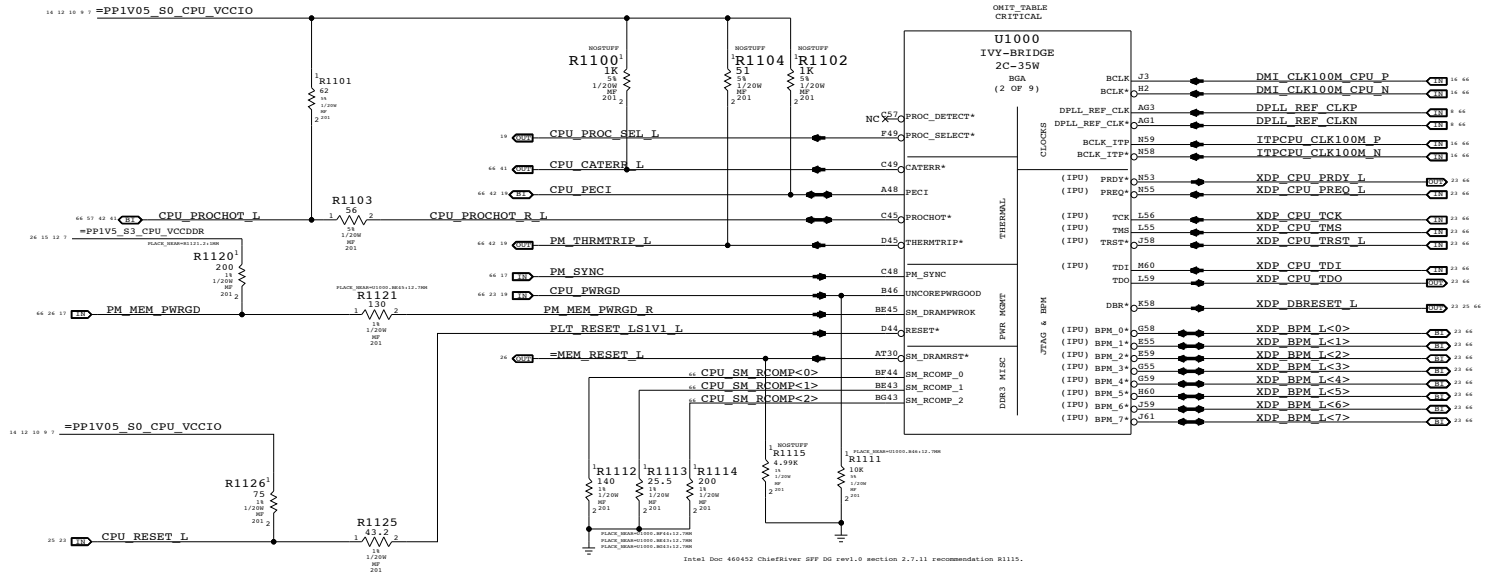
These can be Placed close to J2500 and Only for debug access

=PP1V05_S0_CPU_VCCIO
R1031 1K 5% 1/20W MF 201
EDP_HPD_L
DP_INT_HPD
Q1031 2N7002PXG
CR_SFF Intel doc #460452
Rise/Fall time <6ns

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC_MASTER=J13_MLB_NON_POR
SYNC_DATE=10/17/2011
PAGE TITLE: CPU DMI/PEG/FDI/RSVD
Apple Inc.
DRAWING NUMBER: 051-9277
SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 10 OF 109
SHEET: 9 OF 73



SYNC MASTER=J30_MLB SYNC DATE=07/27/2011

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

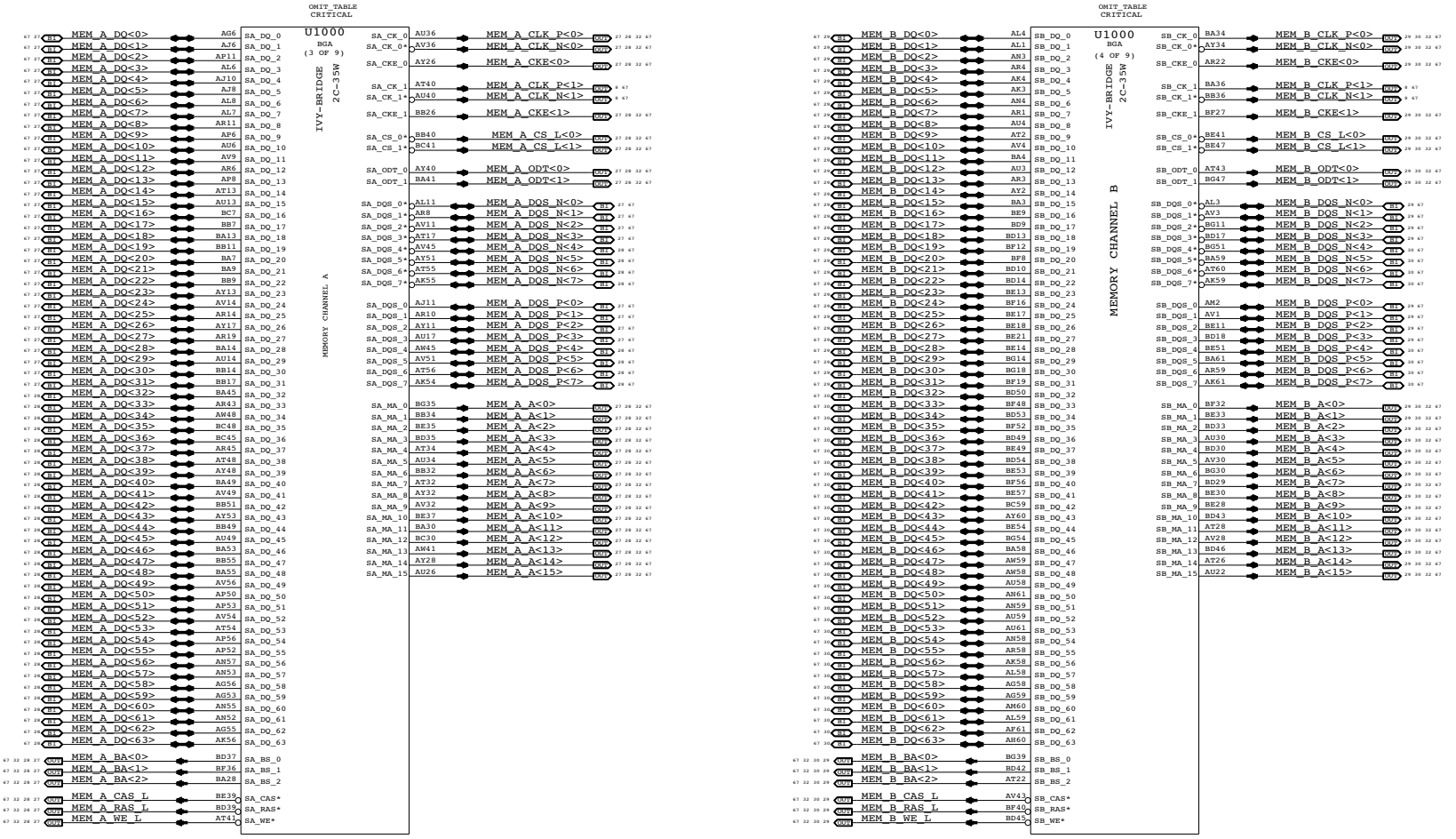
DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

PAGE 11 OF 109

SHEET 10 OF 73



SYNC MASTER=J30_MLB SYNC DATE=07/27/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

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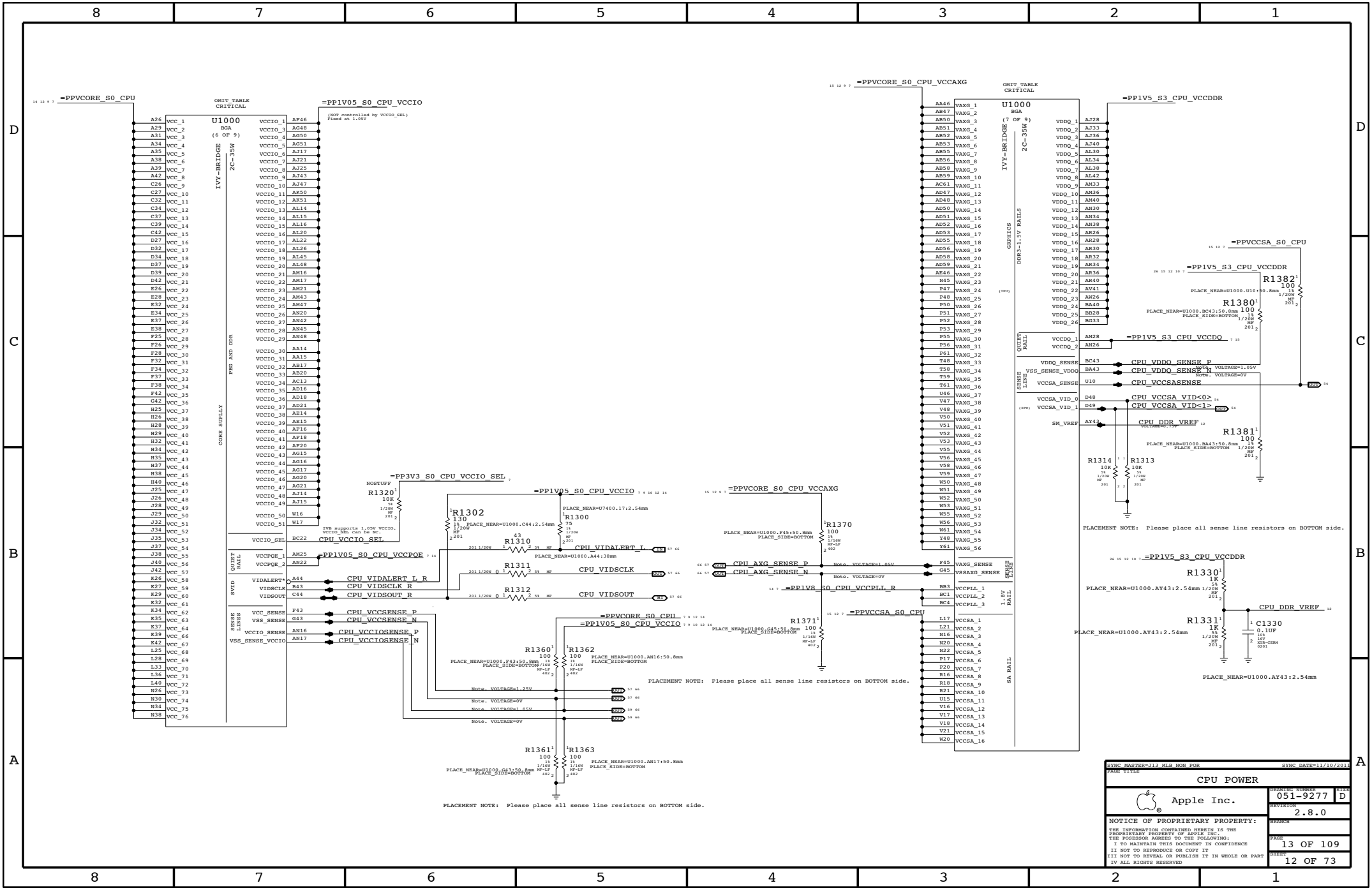
SHEET 11 OF 73


=PPVCORE_S0_CPU
U1000
BGA
(6 OF 9)
IVY-BRIDGE
2C-35W
CORE SUPPLY
PEG AND DDR
OMIT_TABLE
CRITICAL
=PP1V05_S0_CPU_VCCIO
(NOT controlled by VCCIO_SEL)
Fixed at 1.05V
=PP3V3_S0_CPU_VCCIO_SEL
NOSTUFF
R1320 10K
IVB supports 1.05V VCCIO.
VCCIO_SEL can be NC.
CPU_VCCIO_SEL
=PP1V05_S0_CPU_VCCPQE
CPU_VIDALERT_L_R
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
CPU_VCCSENSE_P
CPU_VCCSENSE_N
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N
R1302 130
R1300 75
R1310 43
R1311
R1312
R1360 100
R1362 100
R1361 100
R1363 100
PLACE_NEAR=U7400.17:2.54mm
PLACE_NEAR=U1000.C44:2.54mm
PLACE_NEAR=U1000.A44:38mm
PLACE_NEAR=U1000.F43:50.8mm
PLACE_NEAR=U1000.AN16:50.8mm
PLACE_NEAR=U1000.G43:50.8mm
PLACE_NEAR=U1000.AN17:50.8mm
PLACE_SIDE=BOTTOM
Note. VOLTAGE=1.25V
Note. VOLTAGE=0V
Note. VOLTAGE=1.05V
PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
=PPVCORE_S0_CPU_VCCAXG
R1370 100
R1371 100
CPU_AXG_SENSE_P
CPU_AXG_SENSE_N
=PP1V8_S0_CPU_VCCPLL_R
=PPVCCSA_S0_CPU
PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
=PP1V5_S3_CPU_VCCDDR
=PPVCCSA_S0_CPU
R1382 100
R1380 100
R1381 100
R1314 10K
R1313 10K
CPU_VDDQ_SENSE_P
CPU_VDDQ_SENSE_N
CPU_VCCSASENSE
CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>
CPU_DDR_VREF
PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
R1330 1K
R1331 1K
C1330 0.1UF
PLACE_NEAR=U1000.AY43:2.54mm
SYNC_MASTER=J13_MLB_NON_POR
SYNC_DATE=11/10/2011
PAGE TITLE
CPU POWER
Apple Inc.
DRAWING NUMBER
051-9277
SIZE
D
REVISION
2.8.0
BRANCH
PAGE
13 OF 109
SHEET
12 OF 73
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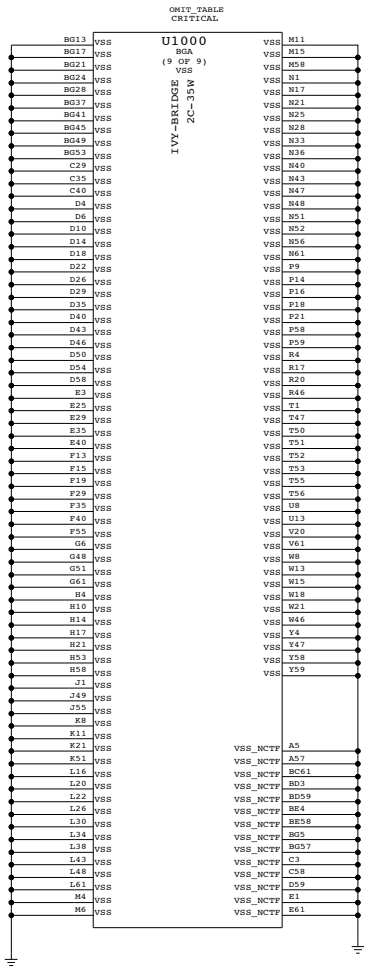

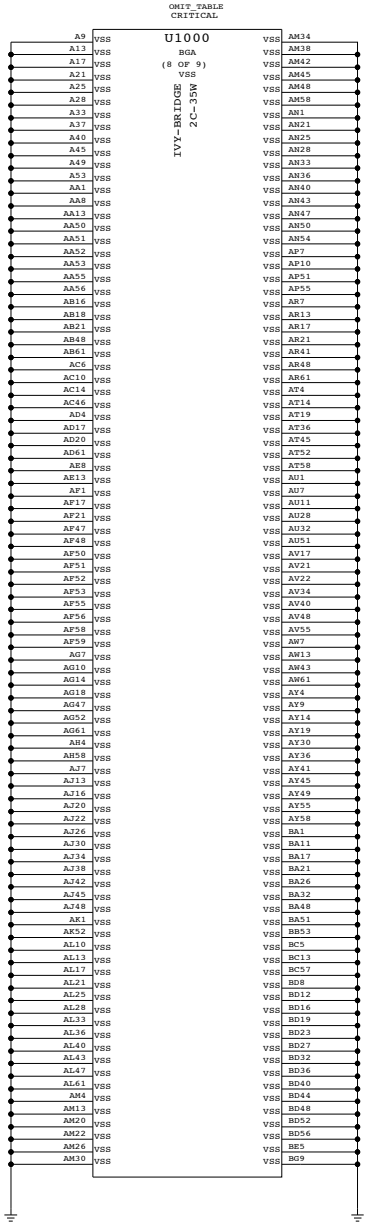

SYNC MASTER=J30_MLB SYNC DATE=07/27/2013

PAGE TITLE

CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

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SHEET 13 OF 73

All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Processor Load Line : -2.9 mOhms

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

=PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1640 C1641 C1642

C1616 C1617 C1618 C1619 C1620 C1621 C1622 C1623 C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 C1656 C1657 C1658 C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 C1681 C1682 C1683 C1679

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

=PP1V05_S0_CPU_VCCIO

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696

C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C

C167D C167E C167G C167H

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W 0603

=PP1V05_S0_CPU_VCCPQE

C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

=PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/16W MF-LF 402

=PP1V8_S0_CPU_VCCPLL_R

C160X 1UF 10% 10V X5R 402

C160Y 1UF 10% 10V X5R 402

C160Z 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC MASTER=211 MLB SYNC DATE=10/03/2011

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

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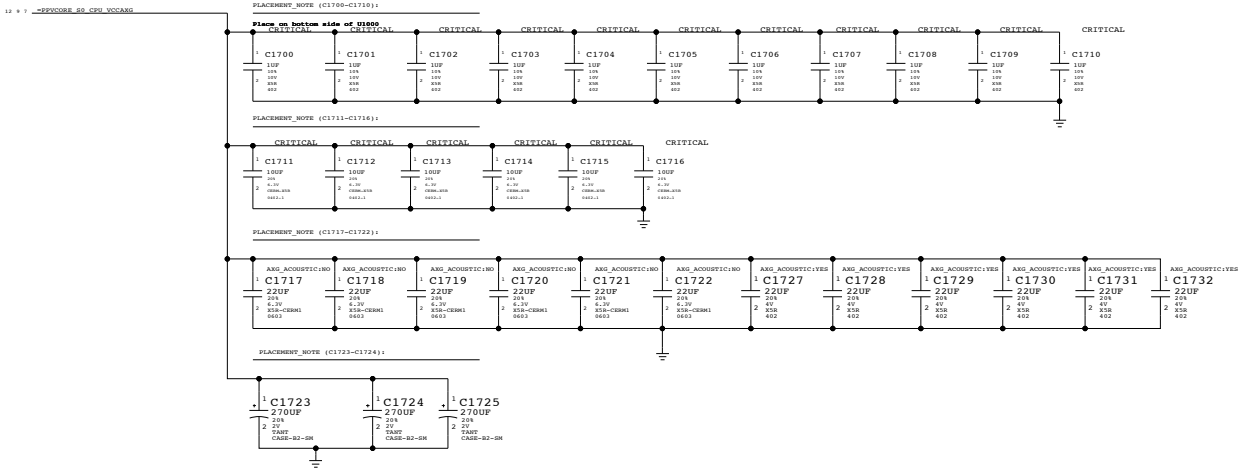
VAXG DECOUPLING

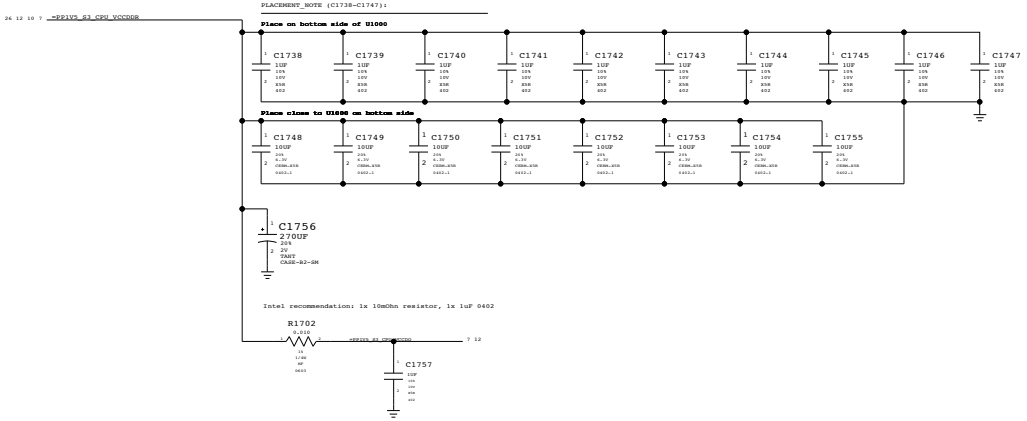
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)



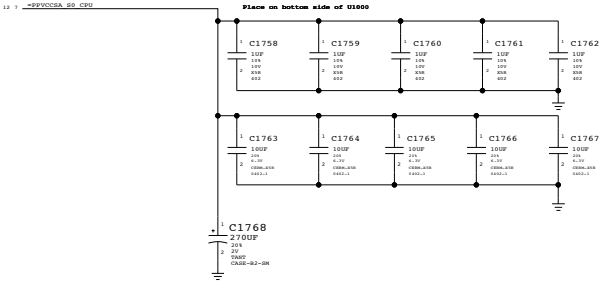
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF



CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf



SYNC MASTER=E21 MLB SYNC DATE=07/29/2013

PAGE TITLE

CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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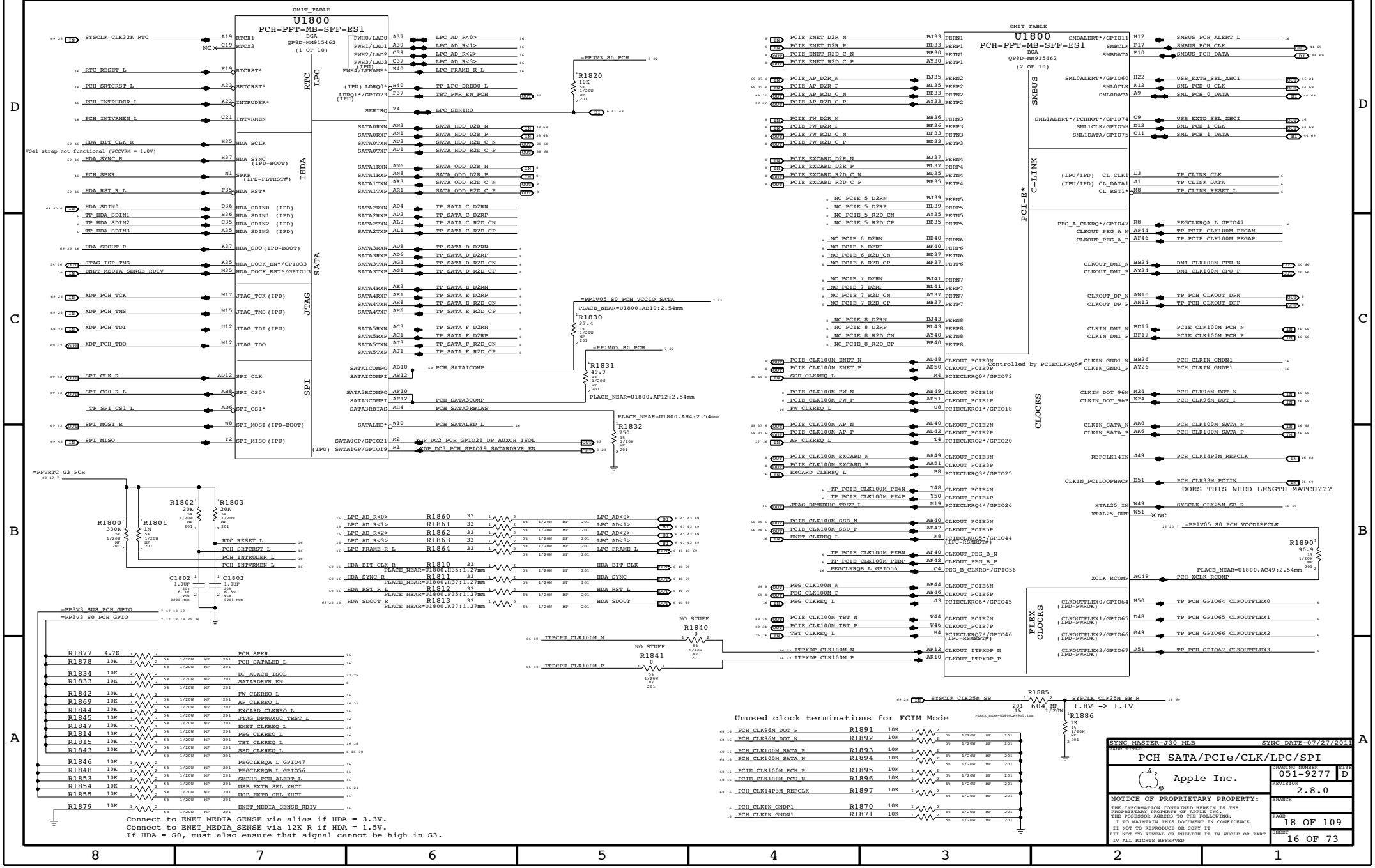
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK_CLK32K_RTC
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_ISP_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO_R
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
PCH_SATA3COMP
PCH_SATA3RBIAS
PCH_SATALED_L
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN
=PP3V3_S0_PCH
=PP1V05_S0_PCH_VCCIO_SATA
=PP1V05_S0_PCH
=PPVRTC_G3_PCH
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1820 10K
R1830 37.4
R1831 49.9
R1832 750
R1800 330K
R1801 1M
R1802 20K
R1803 20K
C1802 1.0UF
C1803 1.0UF
R1860 33
R1861 33
R1862 33
R1863 33
R1864 33
R1810 33
R1811 33
R1812 33
R1813 33
R1840 0
R1841 0
PLACE_NEAR=U1800.H35:1.27mm
PLACE_NEAR=U1800.H37:1.27mm
PLACE_NEAR=U1800.F35:1.27mm
PLACE_NEAR=U1800.K37:1.27mm
PLACE_NEAR=U1800.AB10:2.54mm
PLACE_NEAR=U1800.AF12:2.54mm
PLACE_NEAR=U1800.AH4:2.54mm
NO STUFF
R1877 4.7K
R1878 10K
R1834 10K
R1833 10K
R1842 10K
R1869 10K
R1844 10K
R1845 10K
R1847 10K
R1814 10K
R1815 10K
R1843 10K
R1846 10K
R1848 10K
R1853 10K
R1854 10K
R1855 10K
R1879 10K
PCH_SPKR
PCH_SATALED_L
DP_AUXCH_ISOL
SATARDRVR_EN
FW_CLKREQ_L
AP_CLKREQ_L
EXCARD_CLKREQ_L
JTAG_DPMUXUC_TRST_L
ENET_CLKREQ_L
PEG_CLKREQ_L
TBT_CLKREQ_L
SSD_CLKREQ_L
PEGCLKRQA_L GPIO47
PEGCLKRQB_L GPIO56
SMBUS_PCH_ALERT_L
USB_EXTB_SEL_XHCI
USB_EXTD_SEL_XHCI
ENET_MEDIA_SENSE_RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(2 OF 10)
SMBUS
PCI-E*
C-LINK
CLOCKS
FLEX CLOCKS
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_FW_D2R_N
PCIE_FW_D2R_P
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_D2R_P
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
SSD_CLKREQ_L
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
FW_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_EXCARD_N
PCIE_CLK100M_EXCARD_P
EXCARD_CLKREQ_L
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
JTAG_DPMUXUC_TRST_L
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP
PEGCLKRQB_L GPIO56
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
TBT_CLKREQ_L
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
(IPU/IPD) CL_CLK1
(IPU/IPD) CL_DATA1
CL_RST1
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
CLKOUTFLEX0/GPIO64 (IPD-PWROK)
CLKOUTFLEX1/GPIO65 (IPD-PWROK)
CLKOUTFLEX2/GPIO66 (IPD-PWROK)
CLKOUTFLEX3/GPIO67 (IPD-PWROK)
SMB_PCH_ALERT_L
SMB_PCH_CLK
SMB_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PEGCLKRQA_L GPIO47
TP_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
PCH_XCLK_RCOMP
SYSCLK_CLK25M_SB
CLKOUT_PCIE0N
CLKOUT_PCIE0P
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE1N
CLKOUT_PCIE1P
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE4N
CLKOUT_PCIE4P
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_PCIE6N
CLKOUT_PCIE6P
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE7N
CLKOUT_PCIE7P
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
Controlled by PCIECLKRQ5#
DOES THIS NEED LENGTH MATCH???
=PP1V05_S0_PCH_VCCDIFFCLK
R1885 604
R1886 1K
1.8V -> 1.1V
Unused clock terminations for FCIM Mode
R1891 10K
R1892 10K
R1893 10K
R1894 10K
R1895 10K
R1896 10K
R1897 10K
R1870 10K
R1871 10K
PCH_CLK96M_DOT_P
PCH_CLK96M_DOT_N
PCH_CLK100M_SATA_P
PCH_CLK100M_SATA_N
PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH_N
PCH_CLK14P3M_REFCLK
PCH_CLKIN_GNDP1
PCH_CLKIN_GNDN1
SYNC MASTER=J30_MLB
SYNC DATE=07/27/2011
PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
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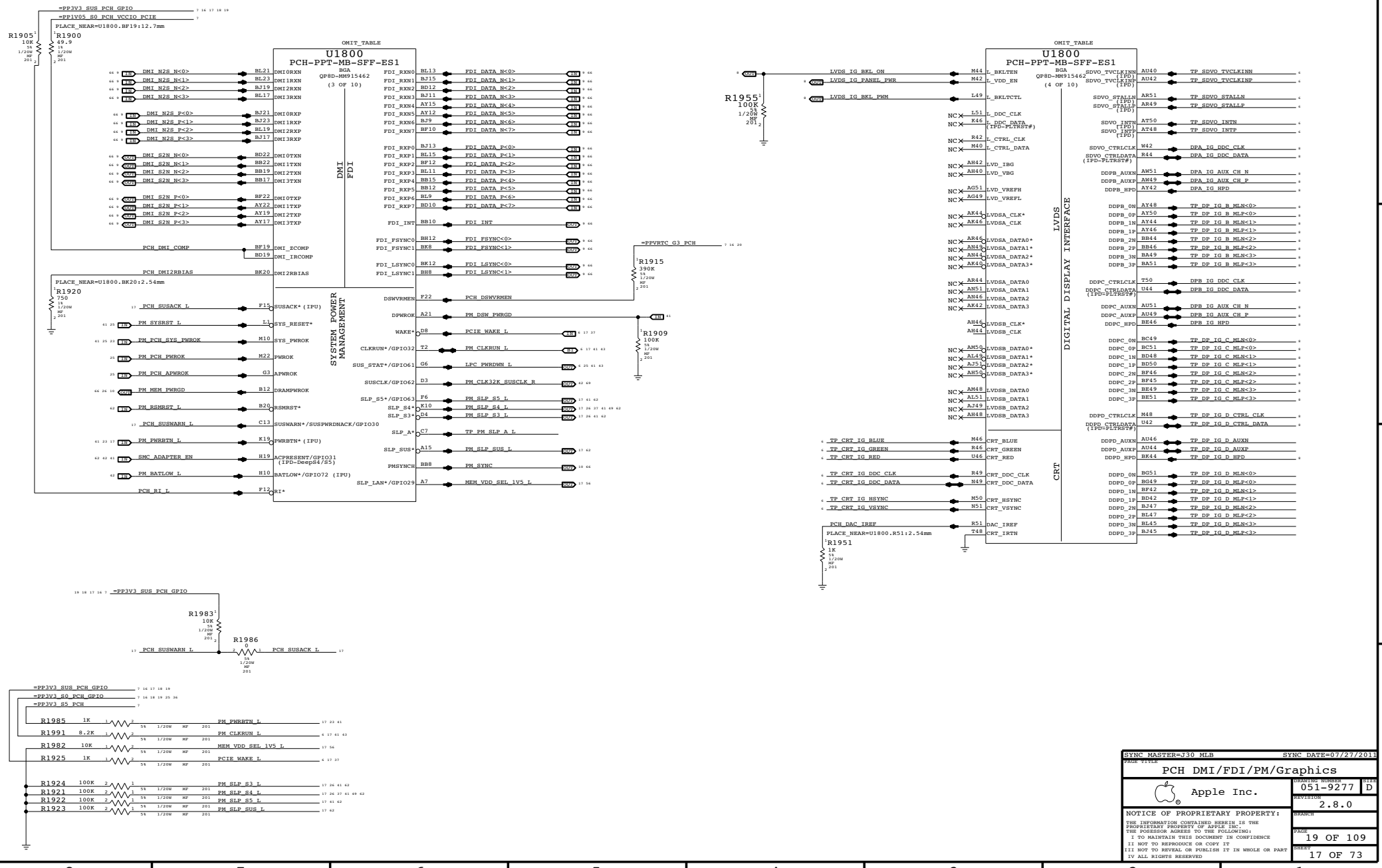
U1800
PCH-PPT-MB-SFF-ES1
OMIT_TABLE
DMI
FDI
SYSTEM POWER MANAGEMENT
LVDS
DIGITAL DISPLAY INTERFACE
CRT
R1905
R1900
R1920
R1915
R1909
R1955
R1951
R1983
R1986
R1985
R1991
R1982
R1925
R1924
R1921
R1922
R1923
SYNC MASTER=J30 MLB
SYNC DATE=07/27/2011
PCH DMI/FDI/PM/Graphics
Apple Inc.
051-9277
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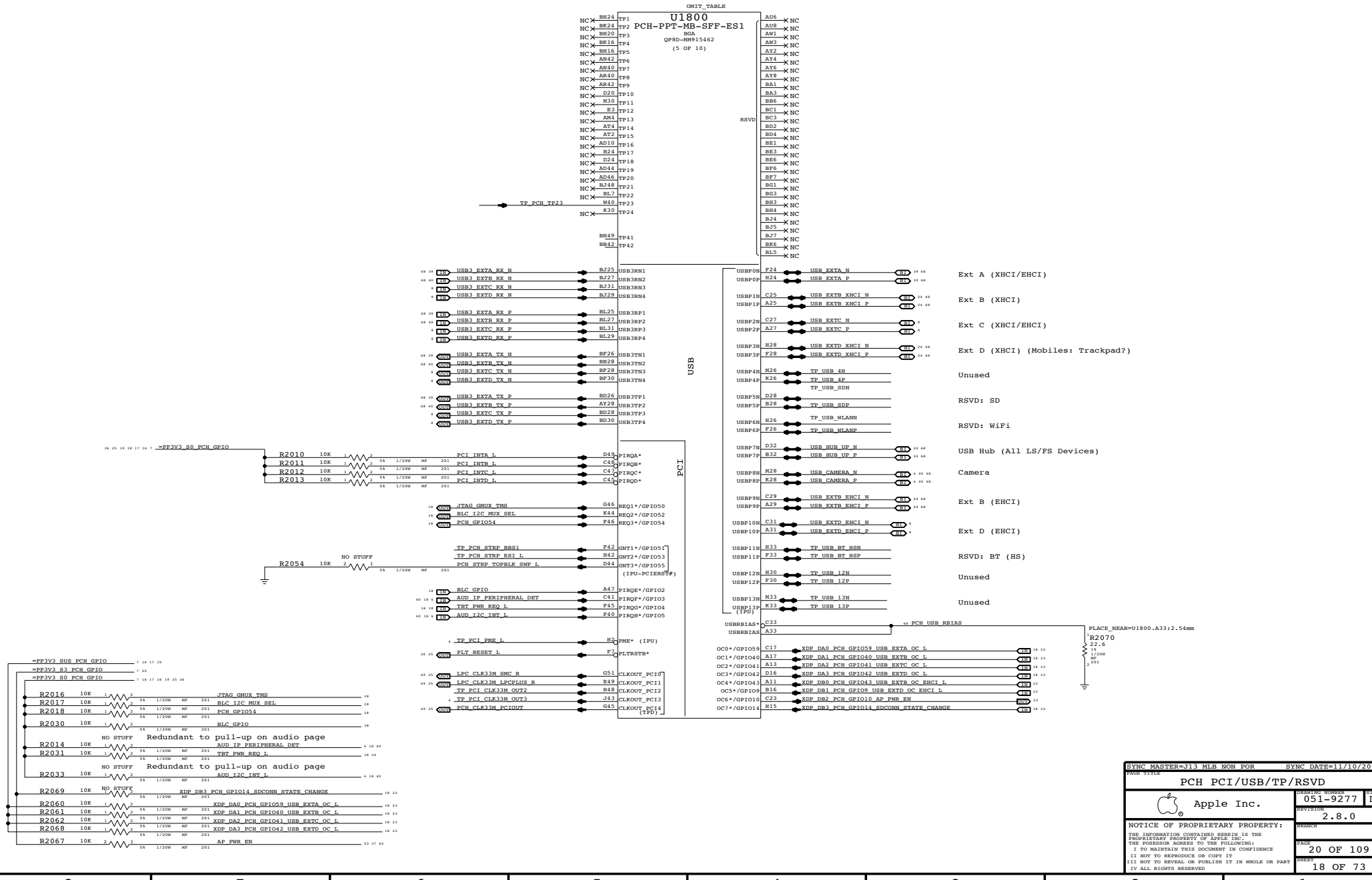
OMIT_TABLE
U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(5 OF 10)
USB
PCI
Ext A (XHCI/EHCI)
Ext B (XHCI)
Ext C (XHCI/EHCI)
Ext D (XHCI) (Mobiles: Trackpad?)
Unused
RSVD: SD
RSVD: WiFi
USB Hub (All LS/FS Devices)
Camera
Ext B (EHCI)
Ext D (EHCI)
RSVD: BT (HS)
Unused
Unused
Redundant to pull-up on audio page
Redundant to pull-up on audio page
SYNC MASTER=J13 MLB NON POR
SYNC DATE=11/10/2011
PCH PCI/USB/TP/RSVD
Apple Inc.
051-9277
2.8.0
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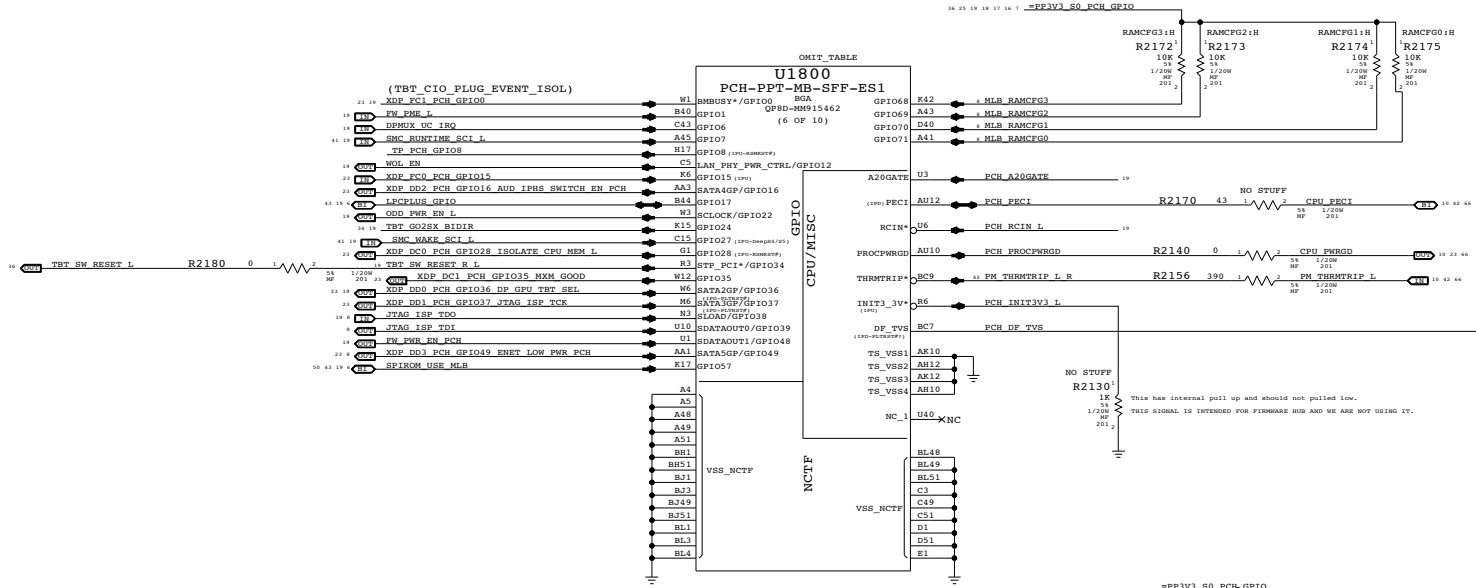
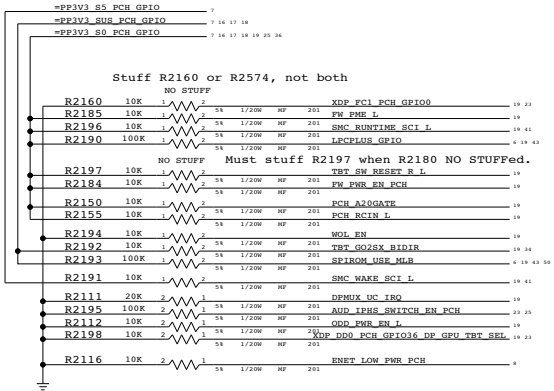
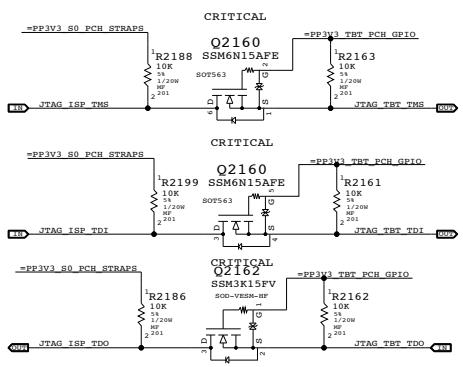
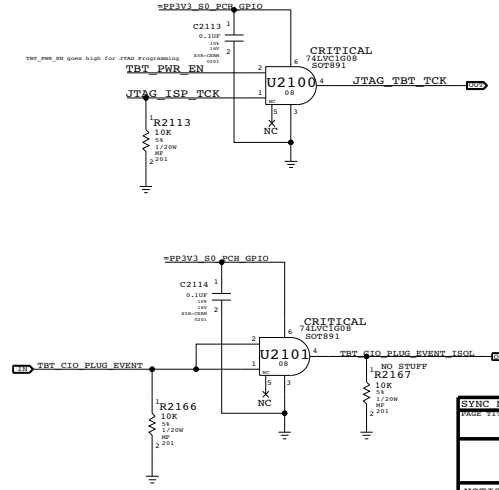
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.









SYNC MASTER=J11_MLB SYNC DATE=09/16/2011

PAGE TITLE
PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
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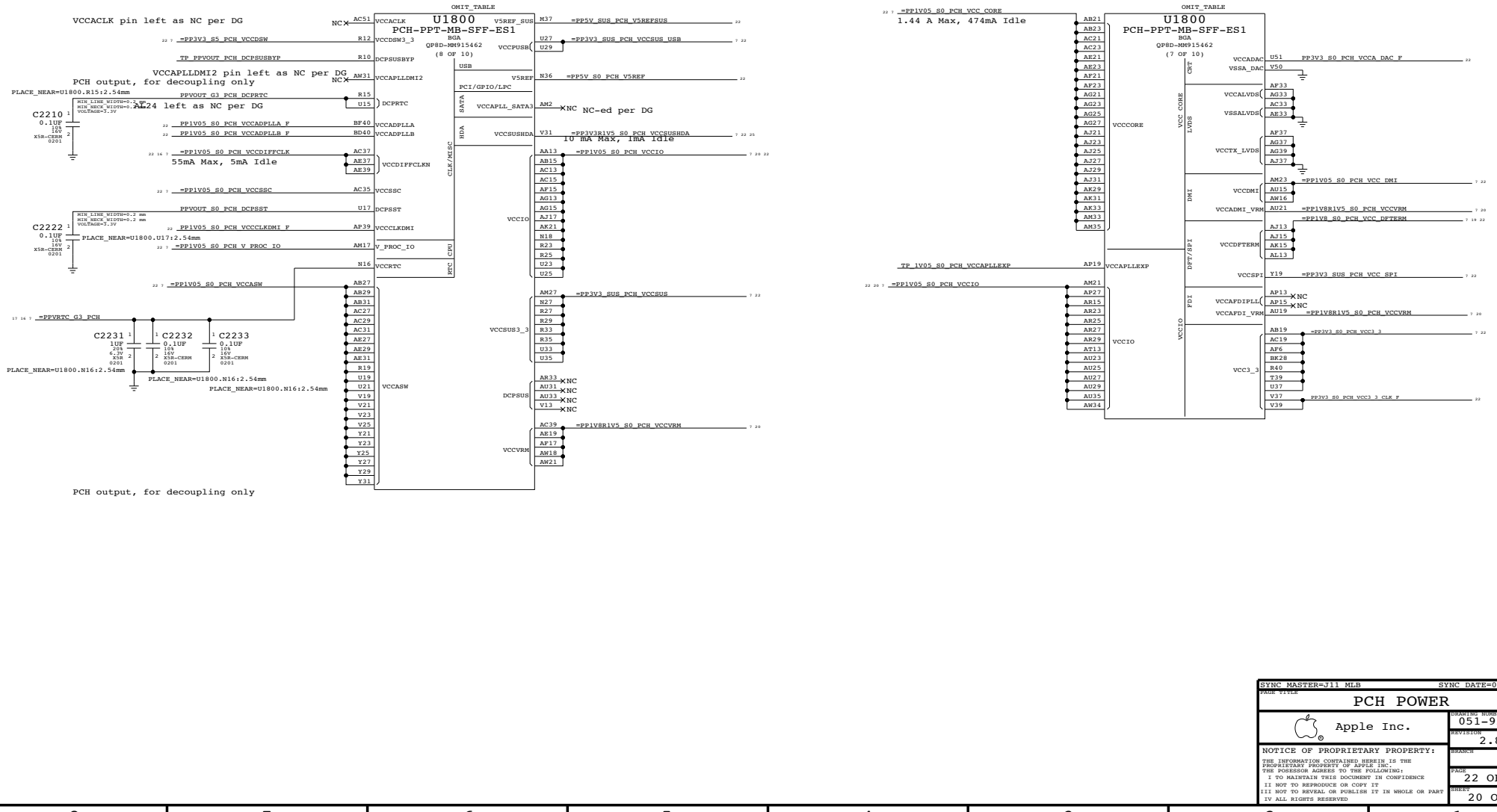

SYNC MASTER=J11_MLB SYNC DATE=09/30/2011

PAGE TITLE

PCH POWER

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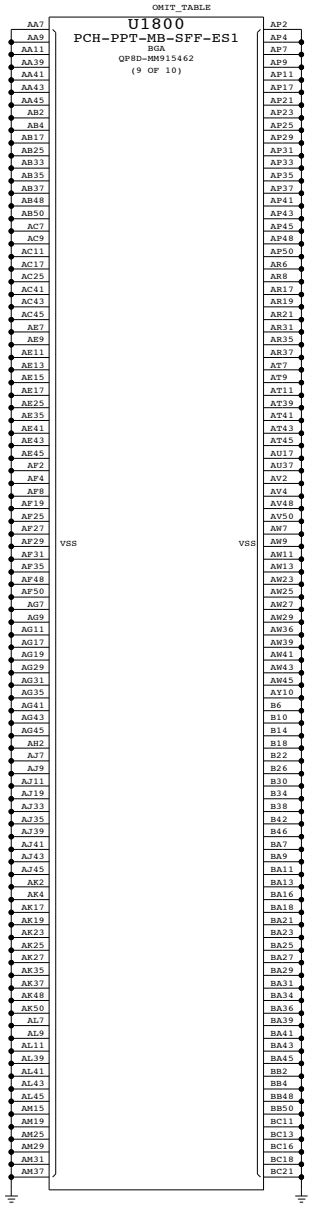

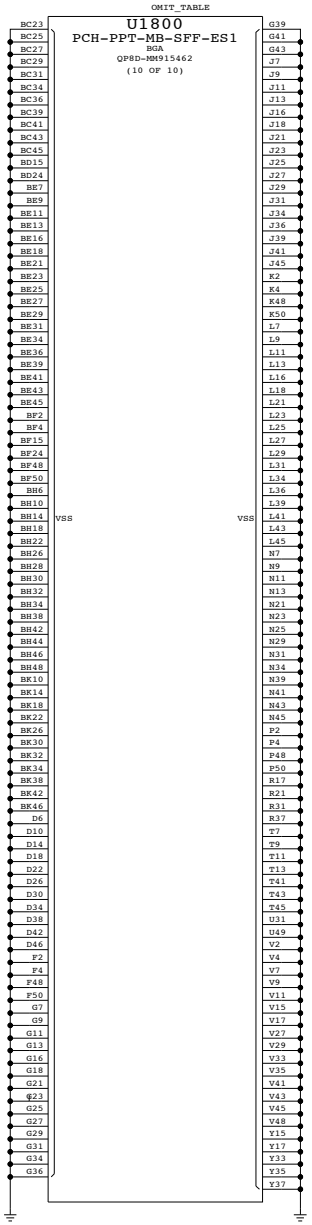

SYNC MASTER=J30_MLB SYNC DATE=07/27/2011

PAGE TITLE

PCH GROUNDS

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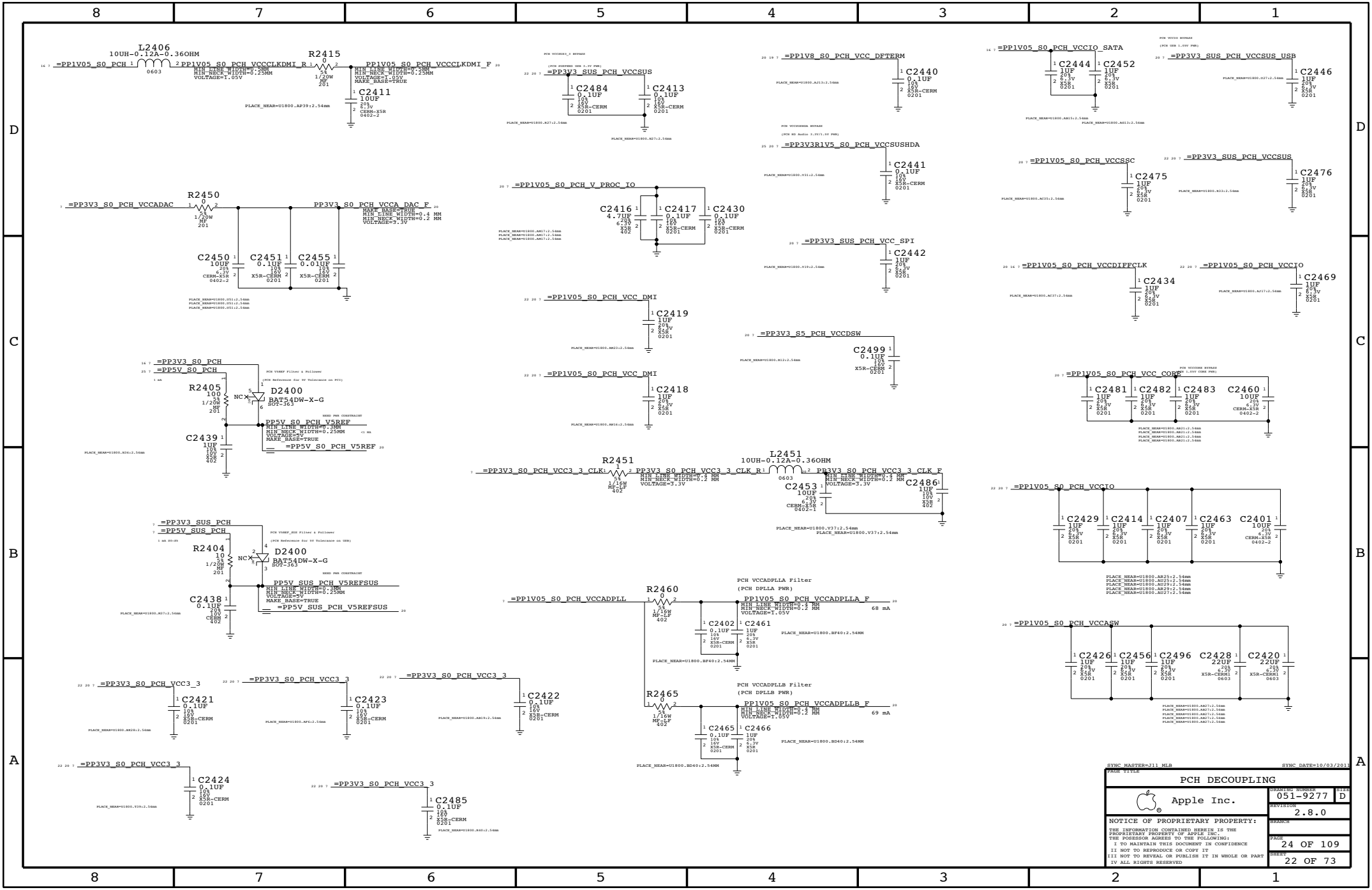
L2406
10UH-0.12A-0.36OHM
=PP1V05_S0_PCH
=PP1V05_S0_PCH_VCCCLKDMI_R
=PP1V05_S0_PCH_VCCCLKDMI_F
R2415
C2411
10UF
=PP3V3_SUS_PCH_VCCSUS
C2484
C2413
=PP1V8_S0_PCH_VCC_DFTERM
C2440
=PP1V05_S0_PCH_VCCIO_SATA
C2444
C2452
=PP3V3_SUS_PCH_VCCSUS_USB
C2446
=PP3V3R1V5_S0_PCH_VCCSUSHDA
C2441
=PP1V05_S0_PCH_VCCSSC
C2475
=PP3V3_SUS_PCH_VCCSUS
C2476
=PP1V05_S0_PCH_V_PROC_IO
C2416
4.7UF
C2417
C2430
R2450
=PP3V3_S0_PCH_VCCADAC
PP3V3_S0_PCH_VCCA_DAC_F
C2450
C2451
C2455
=PP3V3_SUS_PCH_VCC_SPI
C2442
=PP1V05_S0_PCH_VCCDIFFCLK
C2434
=PP1V05_S0_PCH_VCCIO
C2469
=PP1V05_S0_PCH_VCC_DMI
C2419
=PP3V3_S5_PCH_VCCDSW
C2499
=PP3V3_S0_PCH
=PP5V_S0_PCH
R2405
D2400
BAT54DW-X-G
SOT-363
PP5V_S0_PCH_V5REF
C2439
=PP1V05_S0_PCH_VCC_CORE
C2481
C2482
C2483
C2460
=PP3V3_S0_PCH_VCCADAC
R2451
L2451
10UH-0.12A-0.36OHM
=PP3V3_S0_PCH_VCC3_3_CLK
PP3V3_S0_PCH_VCC3_3_CLK_R
PP3V3_S0_PCH_VCC3_3_CLK_F
C2453
C2486
=PP1V05_S0_PCH_VCCIO
C2429
C2414
C2407
C2463
C2401
=PP3V3_SUS_PCH
=PP5V_SUS_PCH
R2404
D2400
BAT54DW-X-G
SOT-363
PP5V_SUS_PCH_V5REFSUS
C2438
=PP5V_SUS_PCH_V5REFSUS
=PP1V05_S0_PCH_VCCADPLL
R2460
PP1V05_S0_PCH_VCCADPLLA_F
68 mA
C2402
C2461
PCH VCCADPLLA Filter
(PCH DPLLA PWR)
R2465
PP1V05_S0_PCH_VCCADPLLB_F
69 mA
C2465
C2466
PCH VCCADPLLB Filter
(PCH DPLLB PWR)
=PP1V05_S0_PCH_VCCASW
C2426
C2456
C2496
C2428
C2420
=PP3V3_S0_PCH_VCC3_3
C2421
C2423
C2422
C2424
C2485
SYNC MASTER=J11 MLB
SYNC DATE=10/03/2011
PAGE TITLE
PCH DECOUPLING
Apple Inc.
DRAWING NUMBER
051-9277
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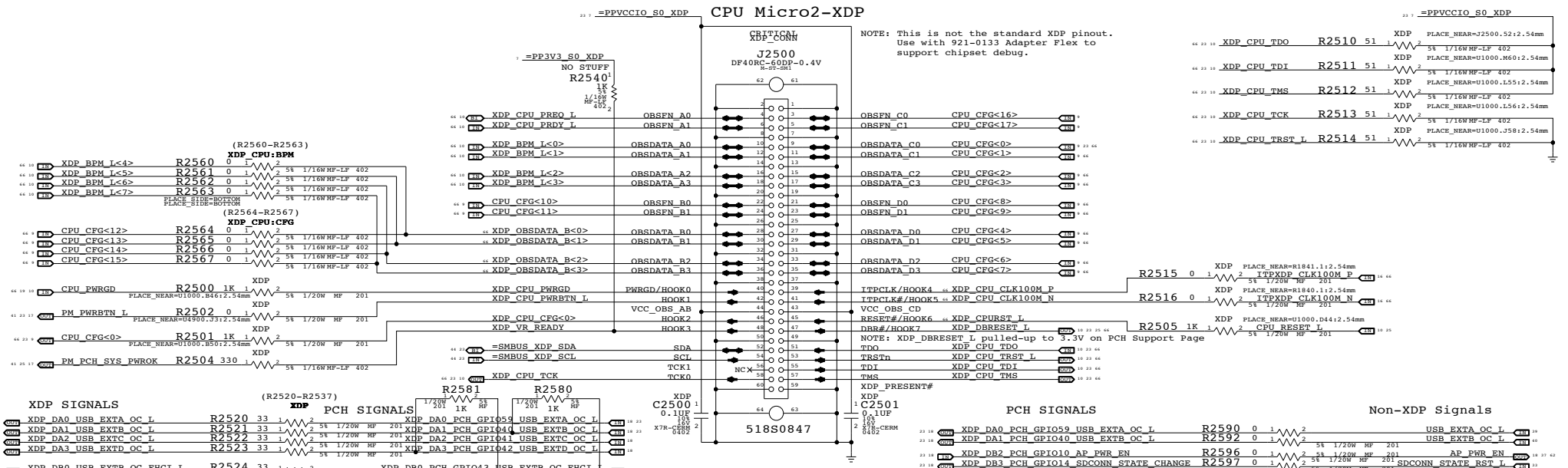
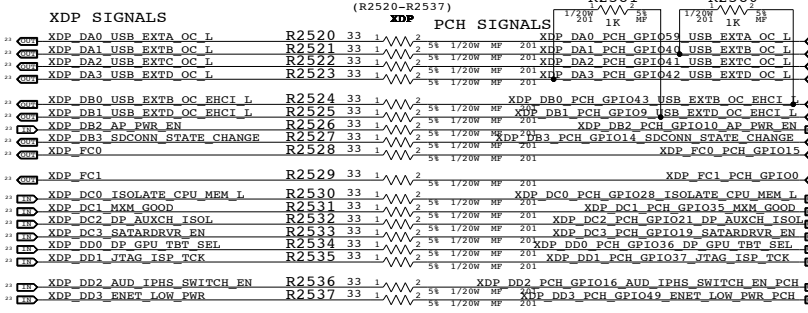
CPU Micro2-XDP



XDP SIGNALS

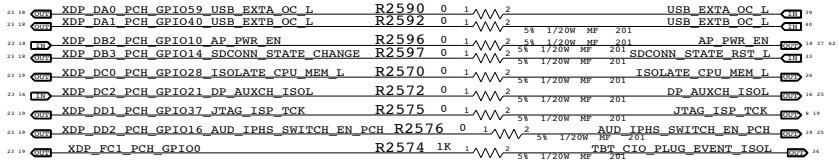
(R2520-R2537)



PCH SIGNALS

R2581 1K 1/20W MF 201
R2580 1K 1/20W MF 201

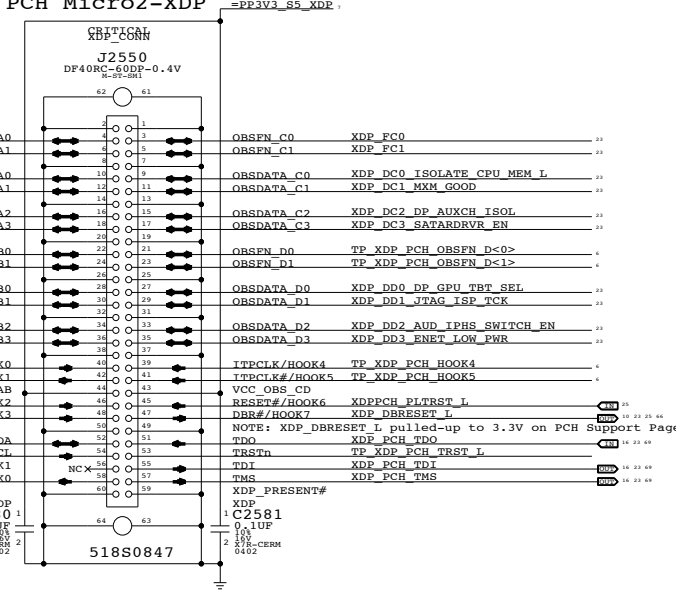
PCH SIGNALS



Non-XDP Signals

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
  Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

ALL_SYS_PWRGD R2584 1K
PM_PWRBTN_L R2585 0
PLACE_NEAR=J2550.50:2.54mm
PLACE_NEAR=U4900.J3:2.54mm

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO R2550 51
XDP_PCH_TDI R2551 51
XDP_PCH_TMS R2552 51
XDP_PCH_TCK R2556 51
PLACE_NEAR=J2550.51:2.54mm
PLACE_NEAR=U1800.U12:2.54mm
PLACE_NEAR=U1800.M15:2.54mm
PLACE_NEAR=U1800.M17:2.54mm

1K series R on PCH Support Page

SYNC MASTER=J13 MLB NON POR SYNC DATE=10/17/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D
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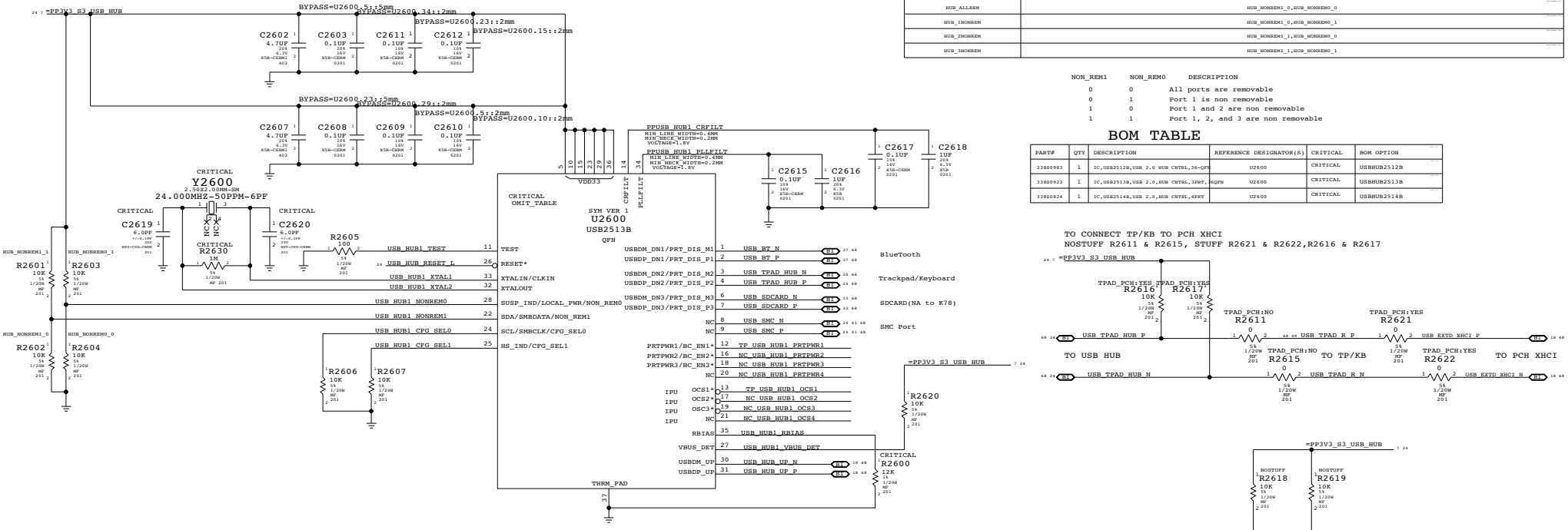


BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

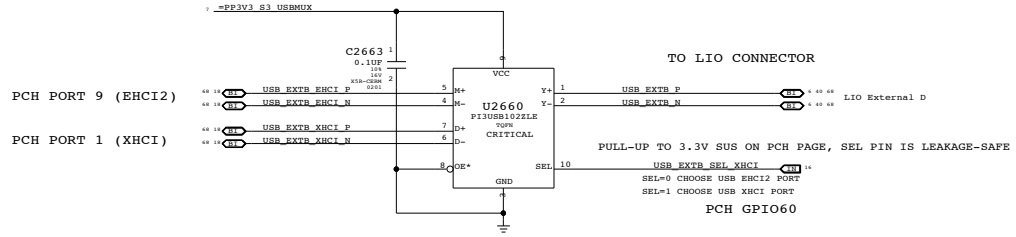
NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

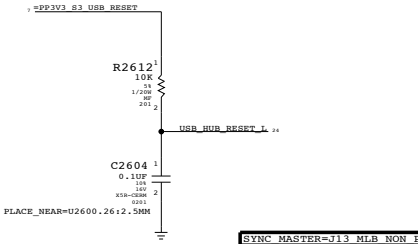
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,39PRT,56QFN	U2600	CRITICAL	USBHUB2513B
338S0824	1	IC,USB2514B,USB 2.0,HUB CNTRL,49PRT	U2600	CRITICAL	USBHUB2514B

TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R2611 & R2615, STUFF R2621 & R2622,R2616 & R2617

USB XHCI/EHCI2 PORT MUX FOR EXT B





SYNC MASTER=J13_MLB_NON_POR SYNC DATE=11/10/2011

PAGE TITLE: USB HUB & MUX

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D
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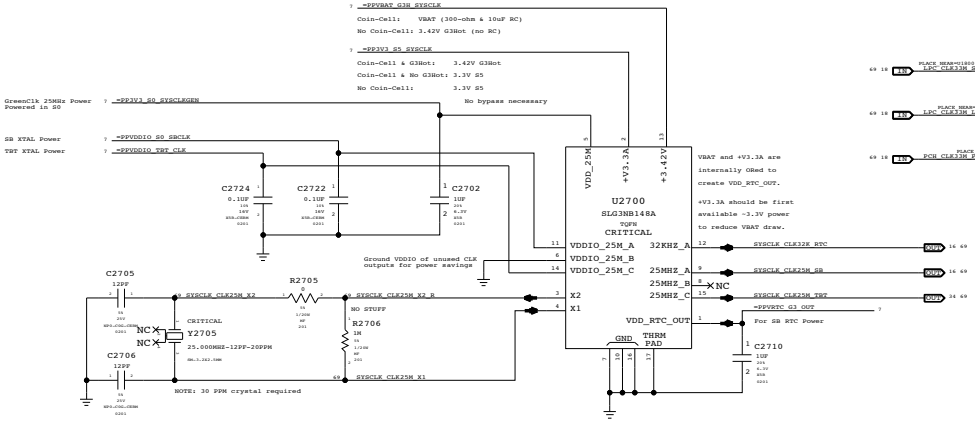
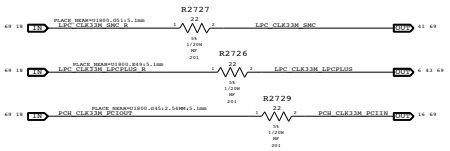
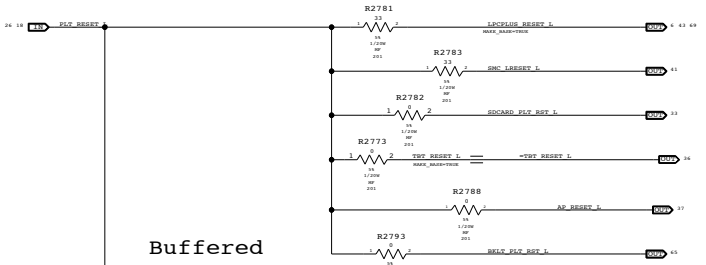
System RTC Power Source & 32kHz / 25MHz Clock Generator





Platform Reset Connections



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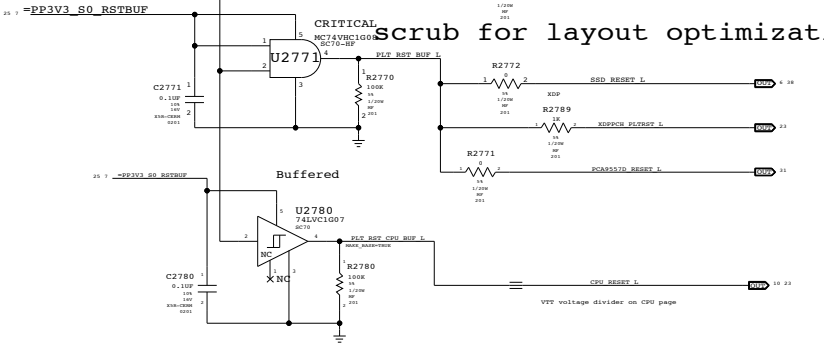
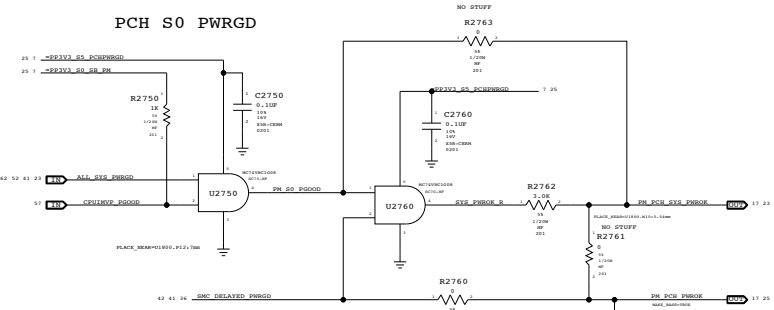
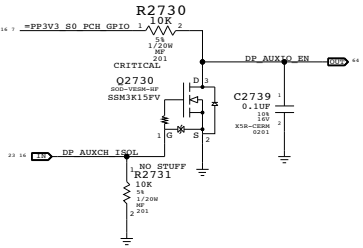


Scrub for layout optimization

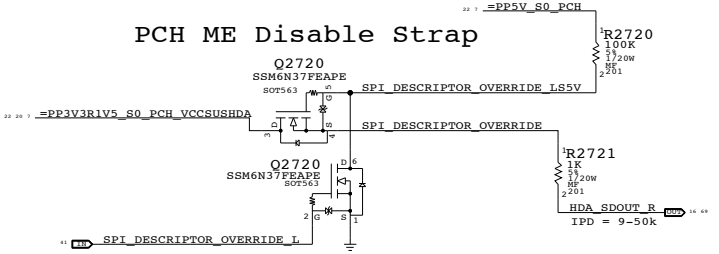
PCH S0 PWRGD



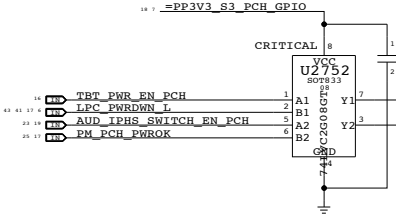
DP_AUXIO_EN Inversion



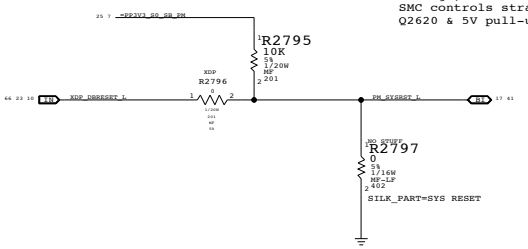
PCH ME Disable Strap



GPIO Glitch Prevention



PCH Reset Button



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

PAGE TITLE
Clock (CK505) and Chipset Support

Apple Inc.

DRAWING NUMBER	051-9277
SIZE	D
REVISION	2.8.0
BRANCH	
PAGE	27 OF 109
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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

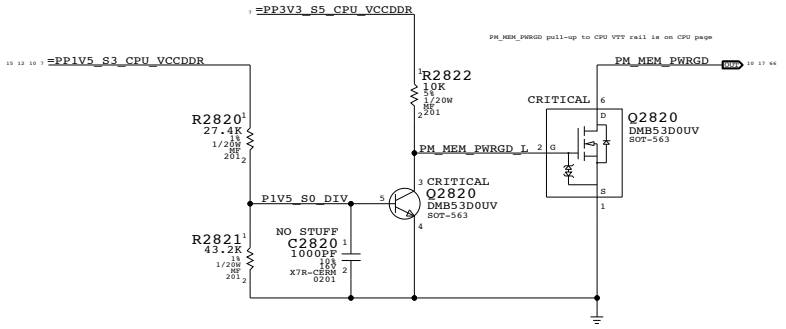
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

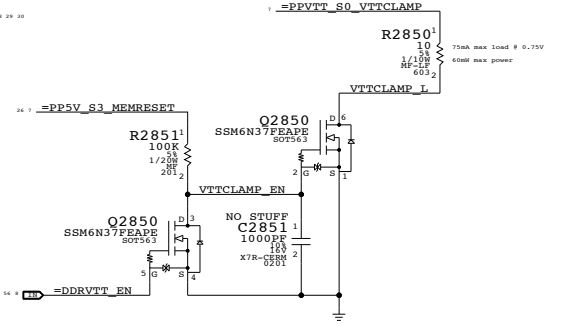
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

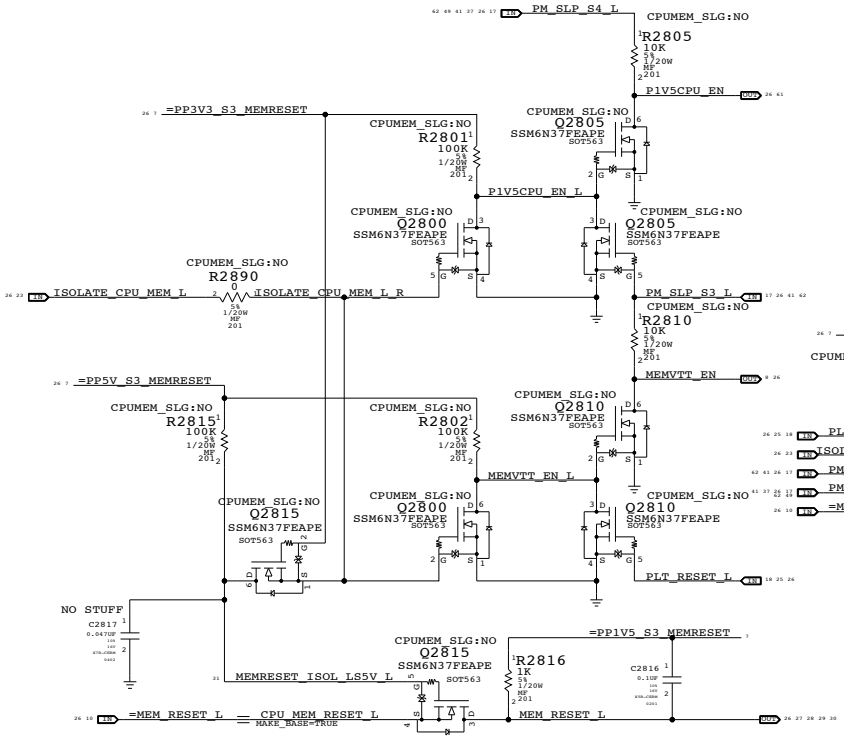
1V5 S0 "PGOOD" for CPU

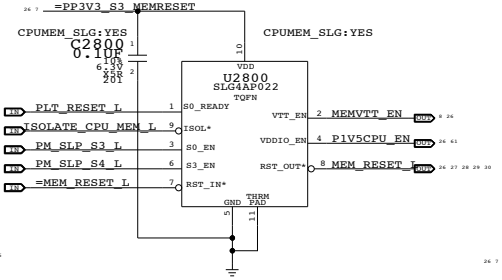


MEMVTT Clamp

Ensures CKE signals are held low in S3







Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
S3	2	0	0	1	1	1	0	1
	3	0	0	0	1	X	0	0
to	4	0	0	1	1	X	0	1
S0	5	0	1	1	1	0 (*)	1	1
	6	0	1	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=J13 MLB NON POR — SYNC DATE=11/10/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9277 — SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 28 OF 109

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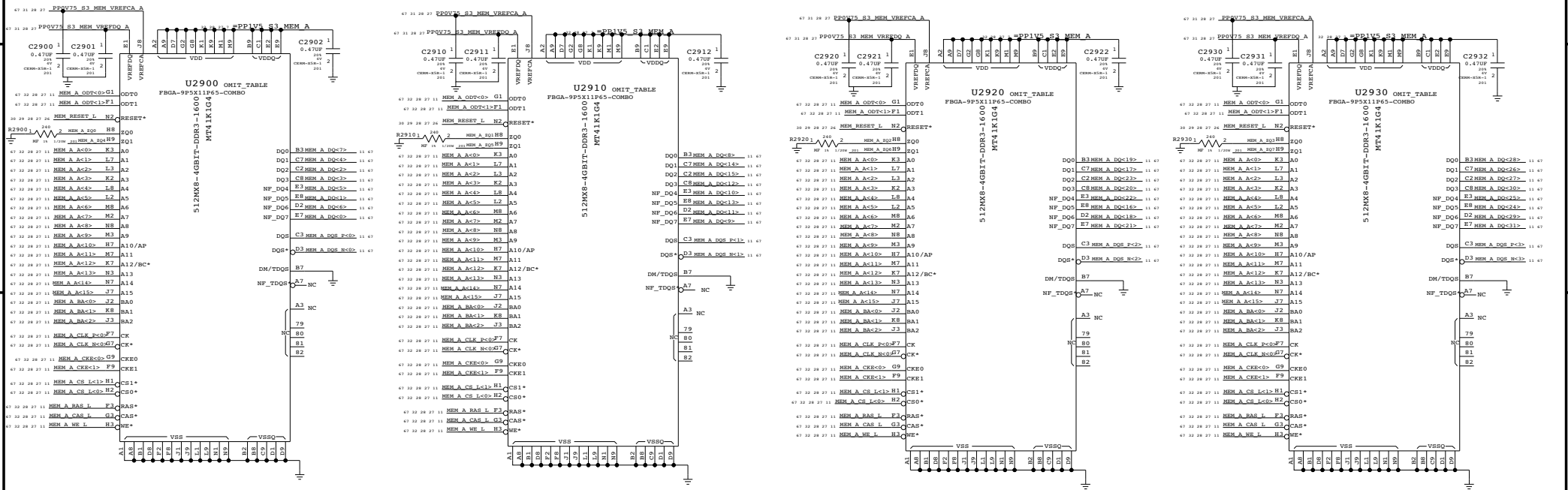


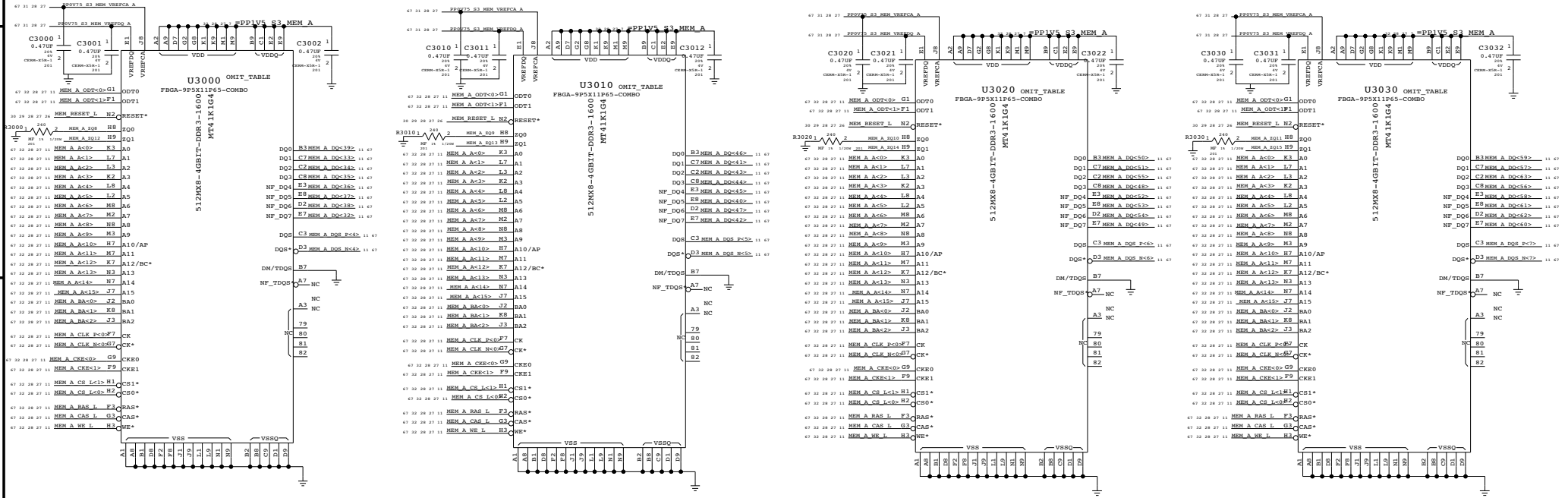
SYNC MASTER=K21_MLB
SYNC DATE=07/28/2011

PAGE TITLE

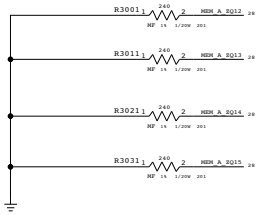
DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

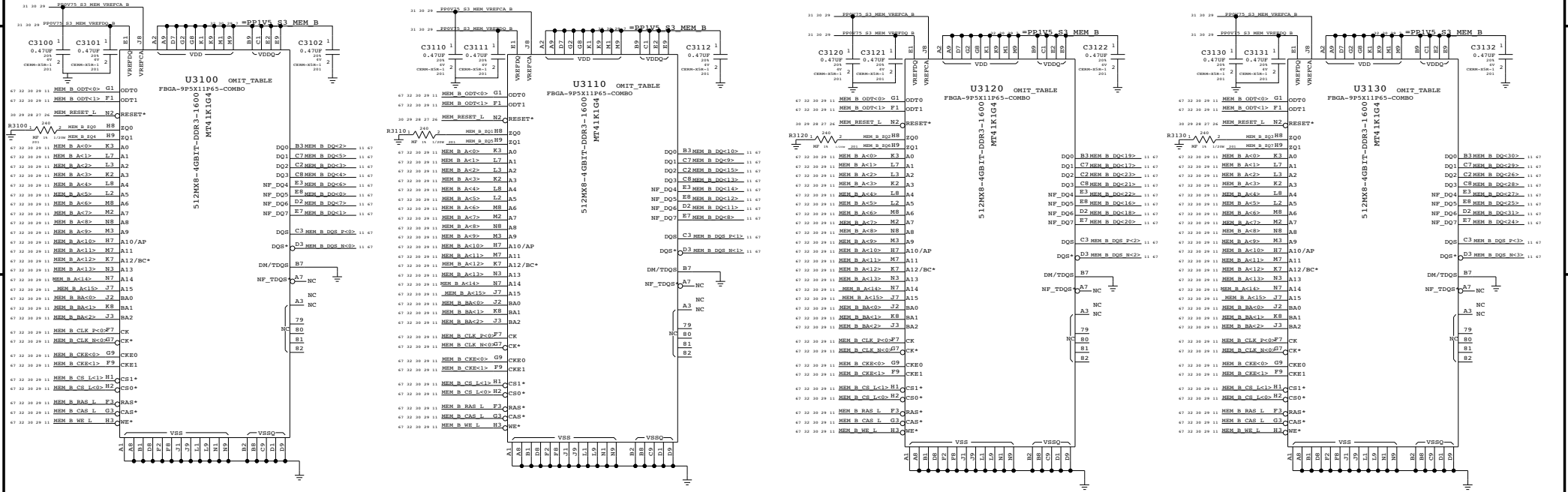
DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 29 OF 109
SHEET 27 OF 73



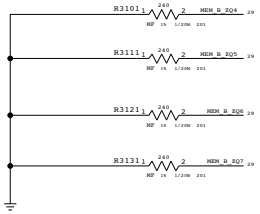
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



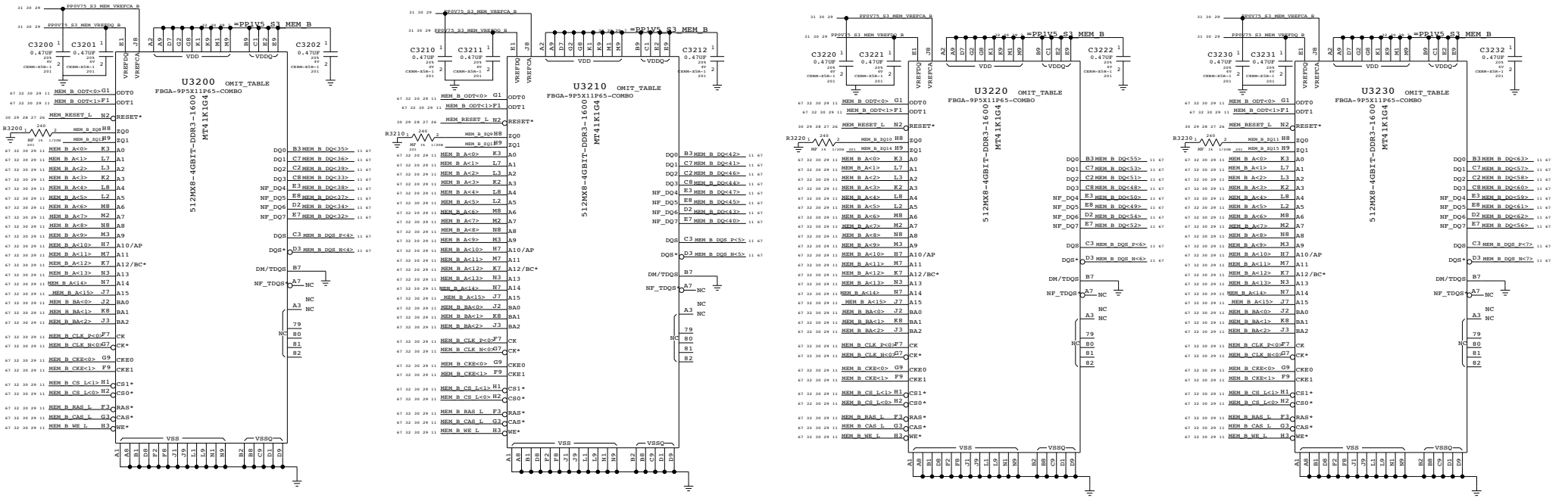
SYNC MASTER=K21_MLB	SYNC DATE=07/28/2011
PAGE TITLE: DDR3 DRAM CHANNEL A (32-63)	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 30 OF 109
	SHEET: 28 OF 73



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC MASTER=K21_MLB	SYNC DATE=07/28/2011
PAGE TITLE: DDR3 DRAM CHANNEL B (0-31)	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 31 OF 109
	SHEET: 29 OF 73



SYNC MASTER=821 MLB	SYNC DATE=07/28/2011
PAGE TITLE	DDR3 DRAM CHANNEL B (32-63)
Apple Inc.	DRAWING NUMBER 051-9277 SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 32 OF 109
	SHEET 30 OF 73

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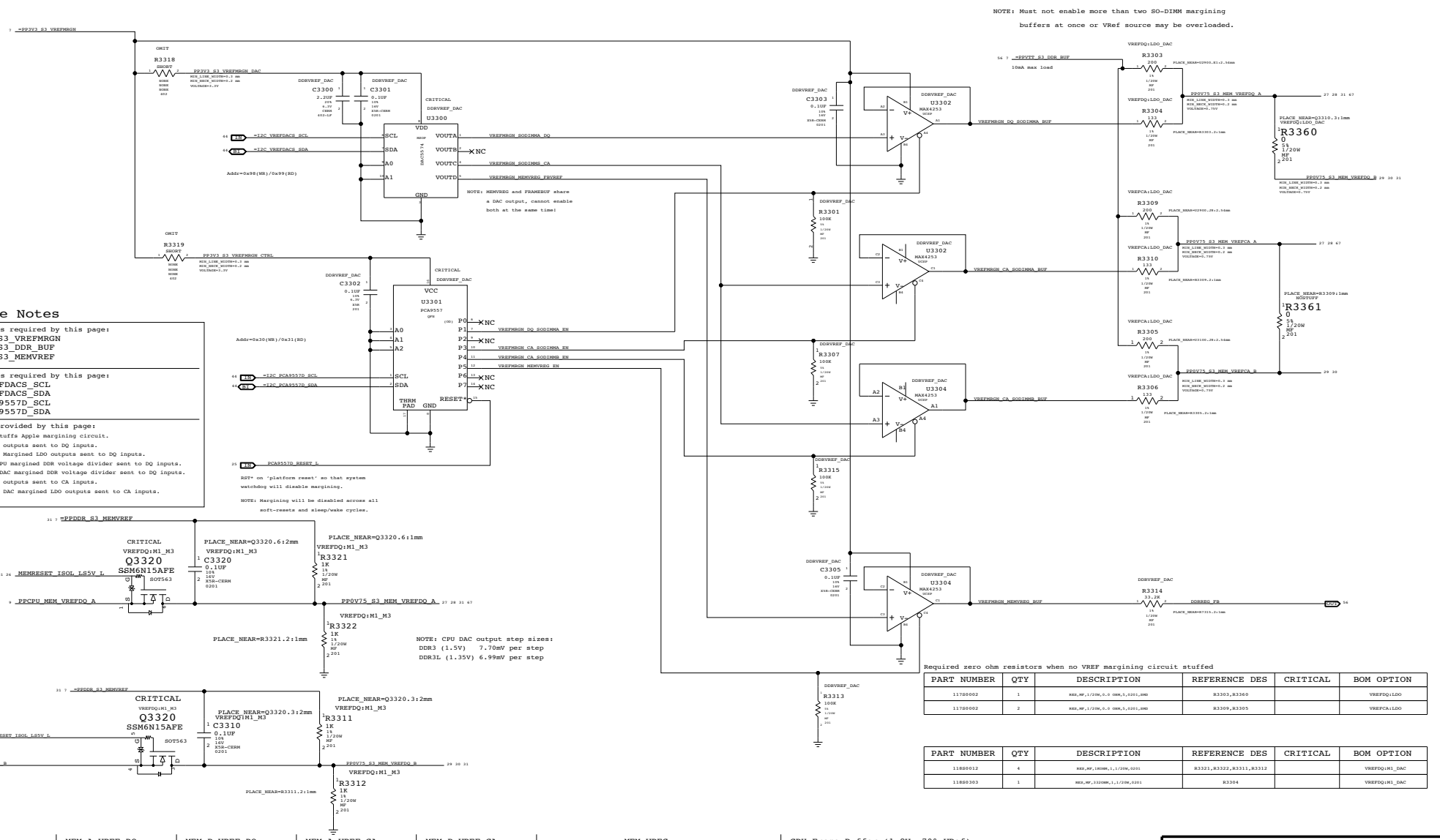

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0012	4	RES,MF,180OHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
118S0303	1	RES,MF,332OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J11 MLB — SYNC DATE=08/04/2011

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER: 051-9277 — SIZE: D

REVISION: 2.8.0

BRANCH:

PAGE: 33 OF 109

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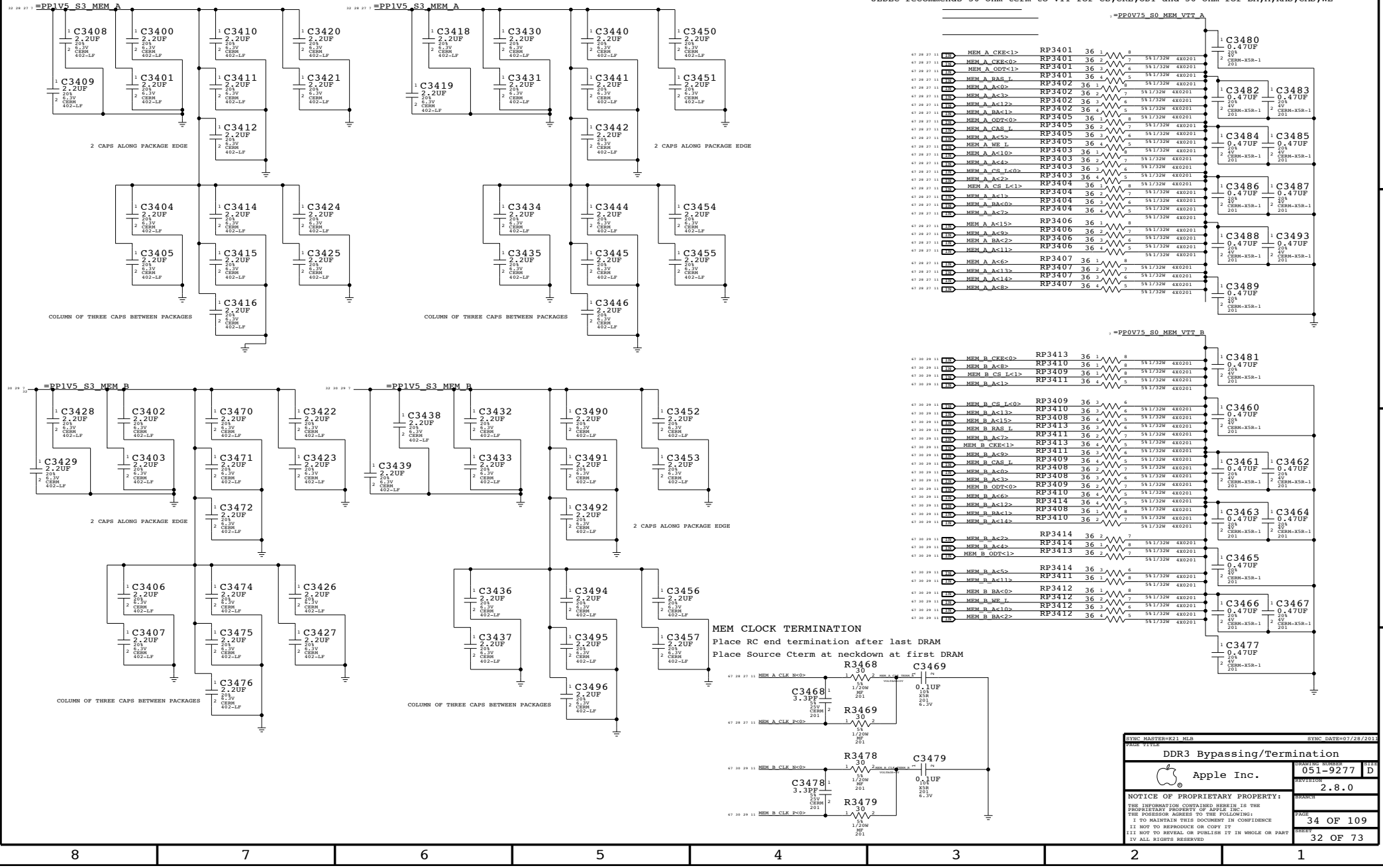
=PP1V5_S3_MEM_A
C3408 2.2UF
C3400 2.2UF
C3410 2.2UF
C3420 2.2UF
C3409 2.2UF
C3401 2.2UF
C3411 2.2UF
C3421 2.2UF
C3412 2.2UF
2 CAPS ALONG PACKAGE EDGE
C3404 2.2UF
C3414 2.2UF
C3424 2.2UF
C3405 2.2UF
C3415 2.2UF
C3425 2.2UF
C3416 2.2UF
COLUMN OF THREE CAPS BETWEEN PACKAGES
=PP1V5_S3_MEM_A
C3418 2.2UF
C3430 2.2UF
C3440 2.2UF
C3450 2.2UF
C3419 2.2UF
C3431 2.2UF
C3441 2.2UF
C3451 2.2UF
C3442 2.2UF
2 CAPS ALONG PACKAGE EDGE
C3434 2.2UF
C3444 2.2UF
C3454 2.2UF
C3435 2.2UF
C3445 2.2UF
C3455 2.2UF
C3446 2.2UF
COLUMN OF THREE CAPS BETWEEN PACKAGES
JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE
=PP0V75_S0_MEM_VTT_A
MEM_A_CKE<1>
MEM_A_CKE<0>
MEM_A_ODT<1>
MEM_A_RAS_L
MEM_A_A<0>
MEM_A_A<3>
MEM_A_A<12>
MEM_A_BA<1>
MEM_A_ODT<0>
MEM_A_CAS_L
MEM_A_A<5>
MEM_A_WE_L
MEM_A_A<10>
MEM_A_A<4>
MEM_A_CS_L<0>
MEM_A_A<2>
MEM_A_CS_L<1>
MEM_A_A<1>
MEM_A_BA<0>
MEM_A_A<7>
MEM_A_A<15>
MEM_A_A<9>
MEM_A_BA<2>
MEM_A_A<11>
MEM_A_A<6>
MEM_A_A<13>
MEM_A_A<14>
MEM_A_A<8>
RP3401 36
RP3402 36
RP3403 36
RP3404 36
RP3405 36
RP3406 36
RP3407 36
5%1/32W 4X0201
C3480 0.47UF
C3482 0.47UF
C3483 0.47UF
C3484 0.47UF
C3485 0.47UF
C3486 0.47UF
C3487 0.47UF
C3488 0.47UF
C3493 0.47UF
C3489 0.47UF
20% 4V CERM-X5R-1 201
=PP1V5_S3_MEM_B
C3428 2.2UF
C3402 2.2UF
C3470 2.2UF
C3422 2.2UF
C3429 2.2UF
C3403 2.2UF
C3471 2.2UF
C3423 2.2UF
C3472 2.2UF
2 CAPS ALONG PACKAGE EDGE
C3406 2.2UF
C3474 2.2UF
C3426 2.2UF
C3407 2.2UF
C3475 2.2UF
C3427 2.2UF
C3476 2.2UF
COLUMN OF THREE CAPS BETWEEN PACKAGES
=PP1V5_S3_MEM_B
C3438 2.2UF
C3432 2.2UF
C3490 2.2UF
C3452 2.2UF
C3439 2.2UF
C3433 2.2UF
C3491 2.2UF
C3453 2.2UF
C3492 2.2UF
2 CAPS ALONG PACKAGE EDGE
C3436 2.2UF
C3494 2.2UF
C3456 2.2UF
C3437 2.2UF
C3495 2.2UF
C3457 2.2UF
C3496 2.2UF
COLUMN OF THREE CAPS BETWEEN PACKAGES
=PP0V75_S0_MEM_VTT_B
MEM_B_CKE<0>
MEM_B_A<8>
MEM_B_CS_L<1>
MEM_B_A<1>
MEM_B_CS_L<0>
MEM_B_A<13>
MEM_B_A<15>
MEM_B_RAS_L
MEM_B_A<7>
MEM_B_CKE<1>
MEM_B_A<9>
MEM_B_CAS_L
MEM_B_A<0>
MEM_B_A<3>
MEM_B_ODT<0>
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MEM_B_A<12>
MEM_B_BA<1>
MEM_B_A<14>
MEM_B_A<2>
MEM_B_A<4>
MEM_B_ODT<1>
MEM_B_A<5>
MEM_B_A<11>
MEM_B_BA<0>
MEM_B_WE_L
MEM_B_A<10>
MEM_B_BA<2>
RP3413 36
RP3410 36
RP3409 36
RP3411 36
RP3408 36
RP3413 36
RP3411 36
RP3409 36
RP3410 36
RP3408 36
RP3414 36
RP3408 36
RP3410 36
RP3414 36
RP3413 36
RP3414 36
RP3411 36
RP3412 36
RP3412 36
RP3412 36
C3481 0.47UF
C3460 0.47UF
C3461 0.47UF
C3462 0.47UF
C3463 0.47UF
C3464 0.47UF
C3465 0.47UF
C3466 0.47UF
C3467 0.47UF
C3477 0.47UF
MEM CLOCK TERMINATION
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM
MEM_A_CLK_N<0>
MEM_A_CLK_P<0>
MEM_B_CLK_N<0>
MEM_B_CLK_P<0>
R3468 30
R3469 30
R3478 30
R3479 30
C3468 3.3PF
C3478 3.3PF
C3469 0.1UF
C3479 0.1UF
5% 1/20W MF 201
5% 25V CERM 201
10% X5R 201 6.3V
SYNC MASTER=K21_MLB
SYNC DATE=07/28/2011
PAGE TITLE
DDR3 Bypassing/Termination
Apple Inc.
DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
PAGE 34 OF 109
SHEET 32 OF 73
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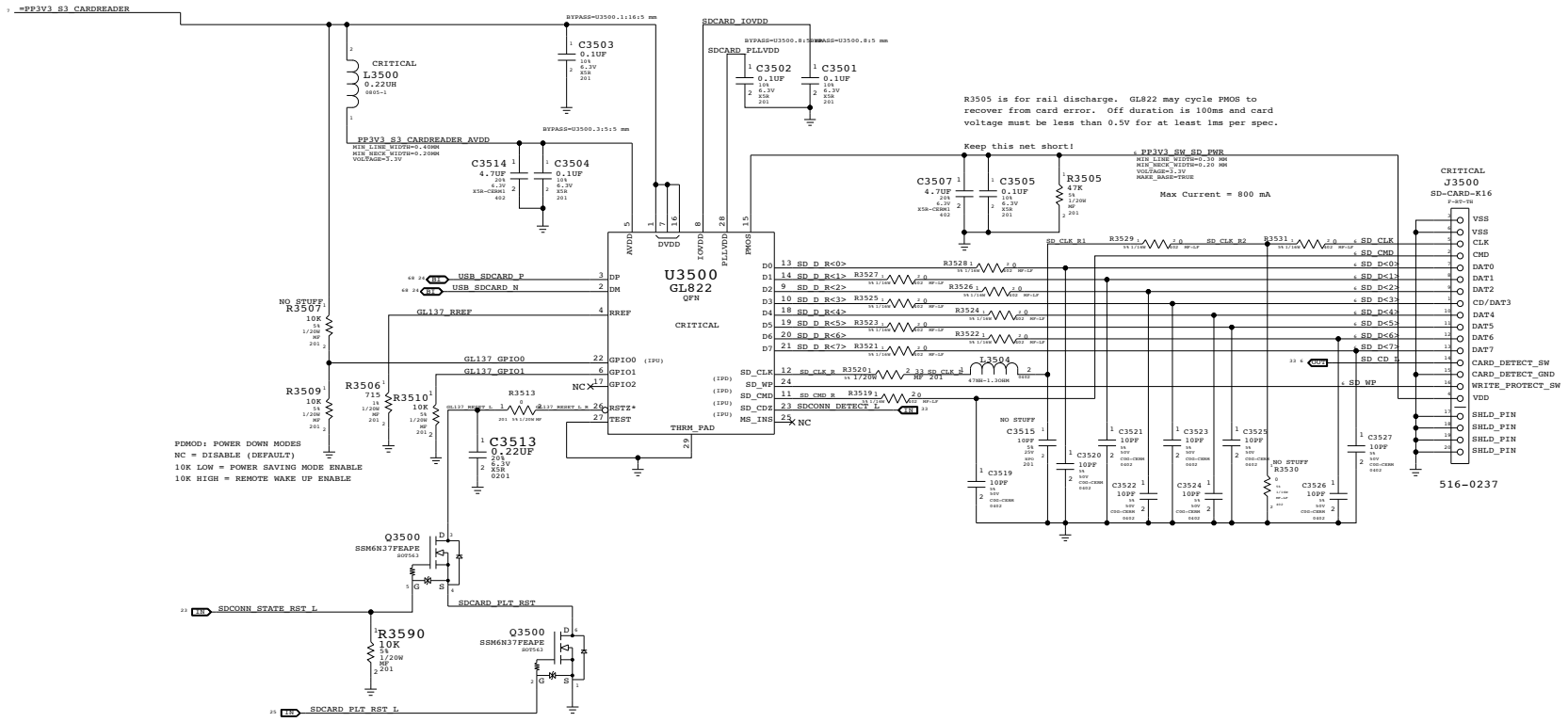
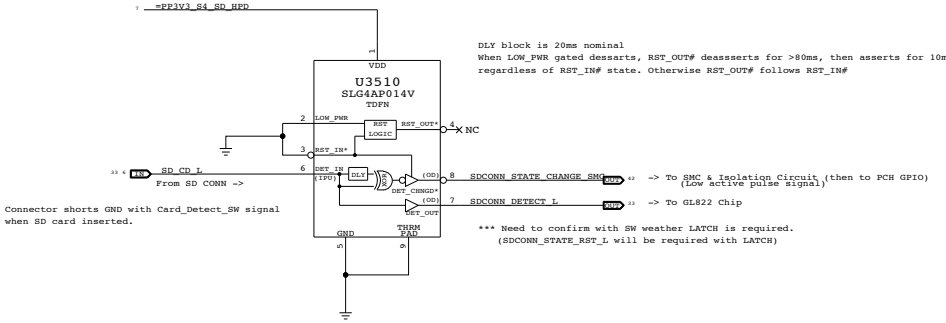


SD Detect & Reset Logic

SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses
RESET_IN* must be pulled to GND if not used. SD detect logic will only function if Reset logic is low.

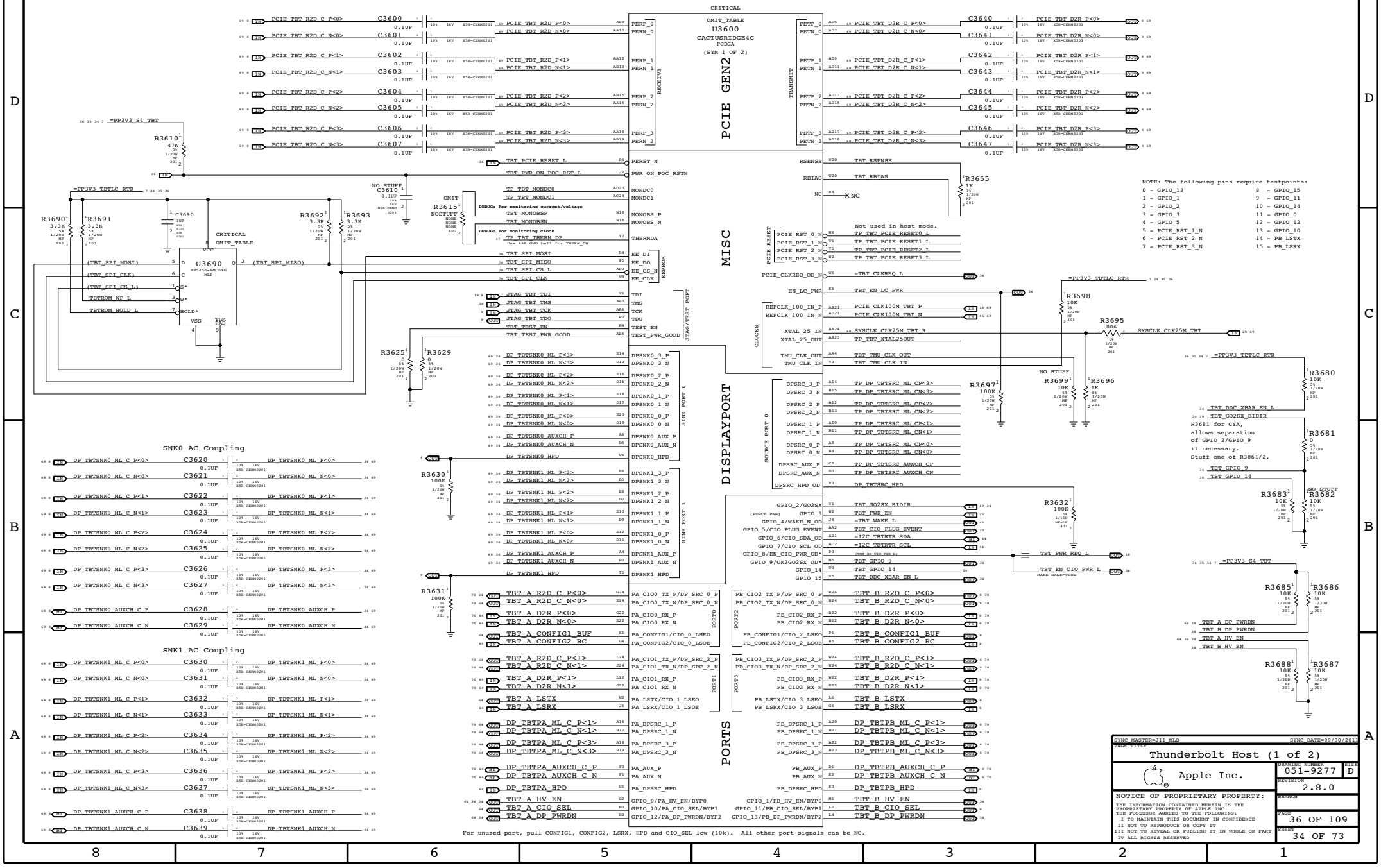


SYNC MASTER=J13_MLB_NON_POR SYNC DATE=11/10/2013

PAGE TITLE
SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
BRANCH
PAGE 35 OF 109
SHEET 33 OF 73


PCIE GEN2
MISC
DISPLAYPORT
PORTS
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
U3690
M95256-RMC6XG
MLP
SNK0 AC Coupling
SNK1 AC Coupling
Thunderbolt Host (1 of 2)
Apple Inc.
051-9277
2.8.0
36 OF 109
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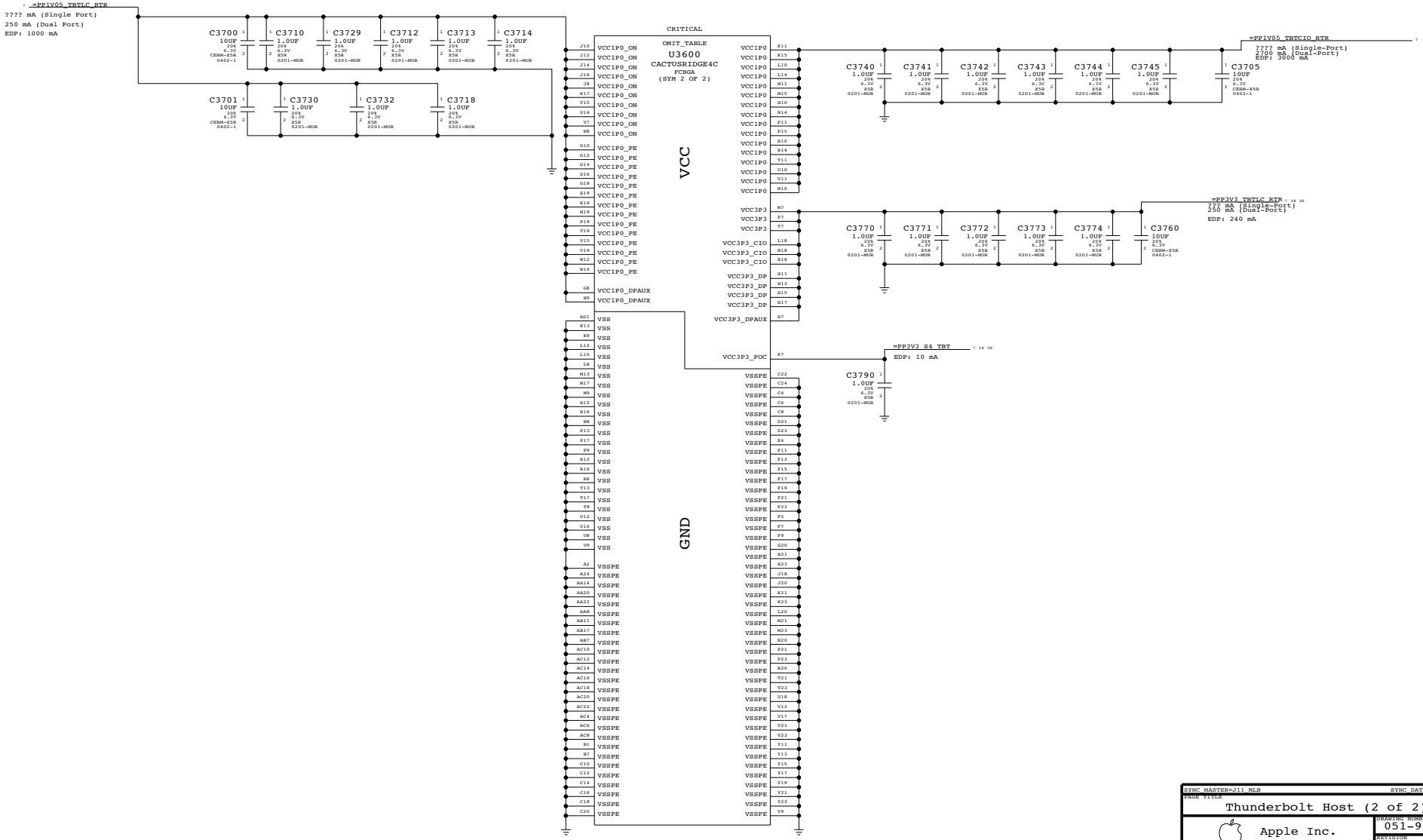

SYNC MASTER=J11_MLB SYNC DATE=10/04/2013

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

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SHEET 35 OF 73

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP18V_TBT_REG (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.

TBT 15V Boost Regulator

Q3880 SI8409DB — CRITICAL
SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

=PPVIN_SW_TBTBST
8-13V Input
Changes required for 2S.

R3880 470K, C3880 0.1UF, TBTBST_PWREN_DIV_L
R3881 150K, TBTBST_PWREN_L
Q3805 SSM3K15FV
TBT_A_HV_EN

L3895 6.8UH-4.0A PIMB062D-SW — CRITICAL
D3895 DFLS230L — CRITICAL
XW3895

U3890 LT3957 QFN — CRITICAL
VIN, SW, SNS1, SNS2, EN/UVLO, INTVCC, VC, RT, SS, SYNC, FBX, NC, SGND, GND

TBTBST_BOOST
TBTBST_SNS1
TBTBST_SNS2
TBTBST_VSNS
TBTBST_FBX
TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND

C3890 10UF, C3891 10UF
R3889 0, R3890 19.9K, R3895 133K <Ra>, R3896 15.8K <Rb>
C3888 22PF, C3889 100PF NO STUFF
C3887 47PF, R3893 10K, C3892 4.7UF, C3893 3300PF, R3894 41.2K, C3894 0.33UF
R3891 200K <R1>, R3892 73.2K <R2>

C3895 10UF, C3897 10UF, C3884 10UF, C3882 10UF, C3881 10UF, C3899 0.001UF
C3896 10UF, C3898 10UF, C3883 10UF

Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz
=PP15V_TBT_REG

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
Q3840 SSM3K15AMFVAPE
R3840 10K, C3800 0.1UF
U3800 SLG4AP016V TDFN — CRITICAL
SENSE 0.7V, DLY, MR*, RESET*, EN, OUT (OD), IN, GND, THRM PAD

=PP3V3_TBTLC_RTR
R3807 100K
PP1V05_TBTLC
TBT_EN_LC_PWR
=TBT_RESET_L
Platform (PCIe) Reset
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
TBT_CLKREQ_L
Pull-up provided by SB page.
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
U3810 TPS22924 CSP — CRITICAL
VIN, VOUT, ON, GND
R3811 0, TBT_EN_LC_3V3
C3810 1.0UF, C3811 1.0UF NO STUFF
=PP3V3_TBTLC_FET
Max Current = 2A (85C)

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ / 25.8 mOhm Max

TBT_EN_LC_ISOL
R3816 36.5K

1.05V TBT "LC" Switch

TBT_EN_LC_1V05
=PP1V05_S0_P1V05TBTFET
U3815 TPS22924 CSP — CRITICAL
VIN, VOUT, ON, GND
=PP1V05_TBTLC_FET
Max Current = 2A (85C)
C3815 1.0UF, C3816 1.0UF
C3816 must be 10%
RC guarantees minimum 5ms to reach 0.5V

U3815

Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ / 28.6 mOhm Max

Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
R3888 330K, R3887 330K
TBTBST_SHDN_DIV
SMC_DELAYED_PWRGD

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
U3830 TPS3808 QFN — CRITICAL
SENSE, CT, MR*, RESET*, GND, THRM PAD
Pull-up: R3610
TBT_PWR_ON_POC_RST_L
TBTPOCRST_MR_L
TBTPOCRST_CT
C3831 0.0047UF, C3830 0.1UF
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
Q3825 SSM6N37FEAPE SOT563
=PP3V3_S0_PCH_GPIO
R3830 100K
TBT_SW_RESET_L
C3825 330PF
WF: C value may need tuning.

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTFET
=PP3V3_TBTLC_RTR
U3820 TPS22920 CSP — CRITICAL
VIN, VOUT, ON, GND
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)
R3820 100K
TBT_EN_CIO_PWR
Q3825 SSM6N37FEAPE SOT563
C3820 1.0UF
TBT_EN_CIO_PWR_L

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ / 11.5 mOhm Max

SYNC MASTER=J13_MLB_NON_POR
SYNC DATE=11/10/2011
PAGE TITLE: TBT Power Support
Apple Inc.
DRAWING NUMBER: 051-9277
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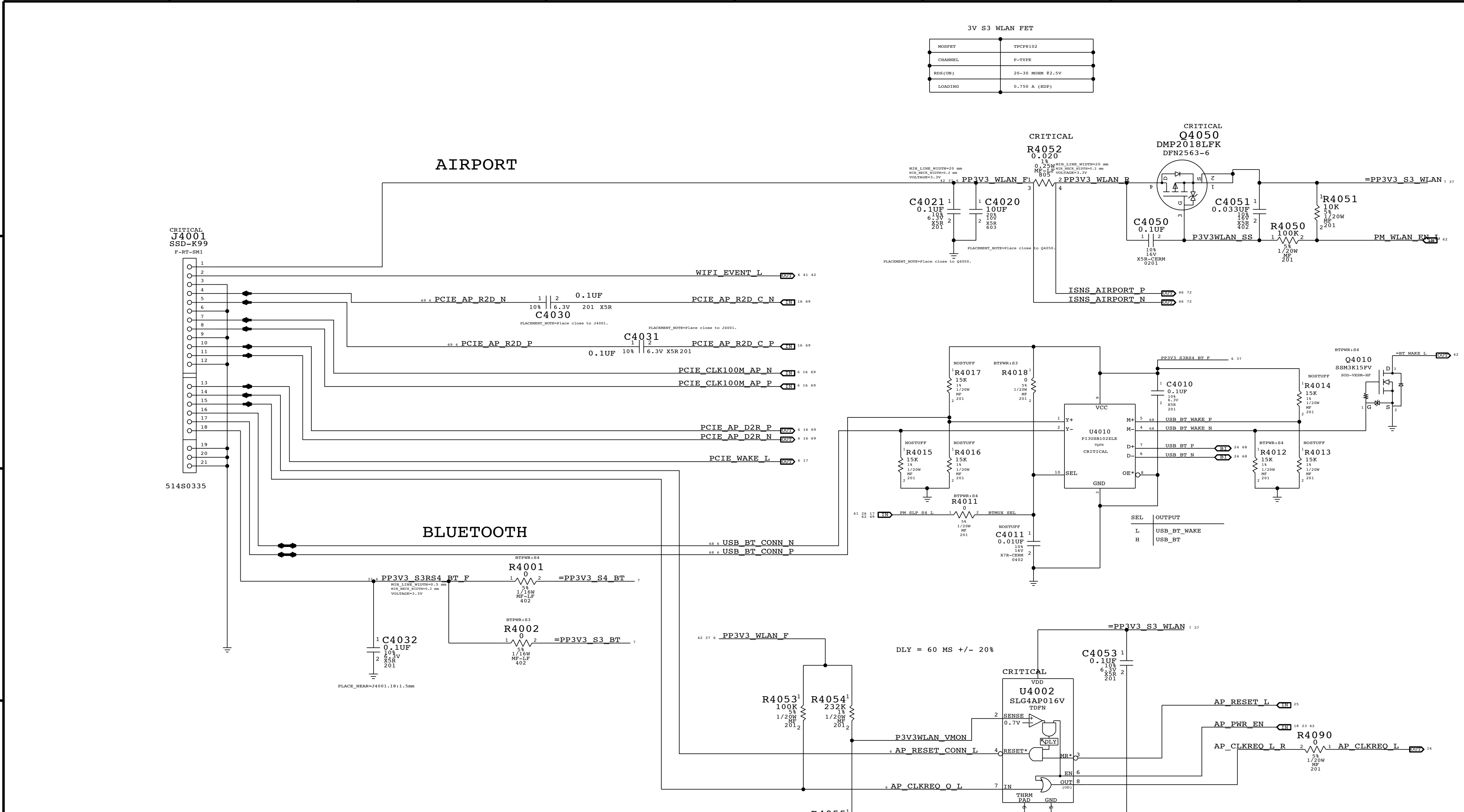

SYNC_MASTER=J11_MLB SYNC_DATE=10/11/2011

PAGE TITLE

X21 WIRELESS CONNECTOR

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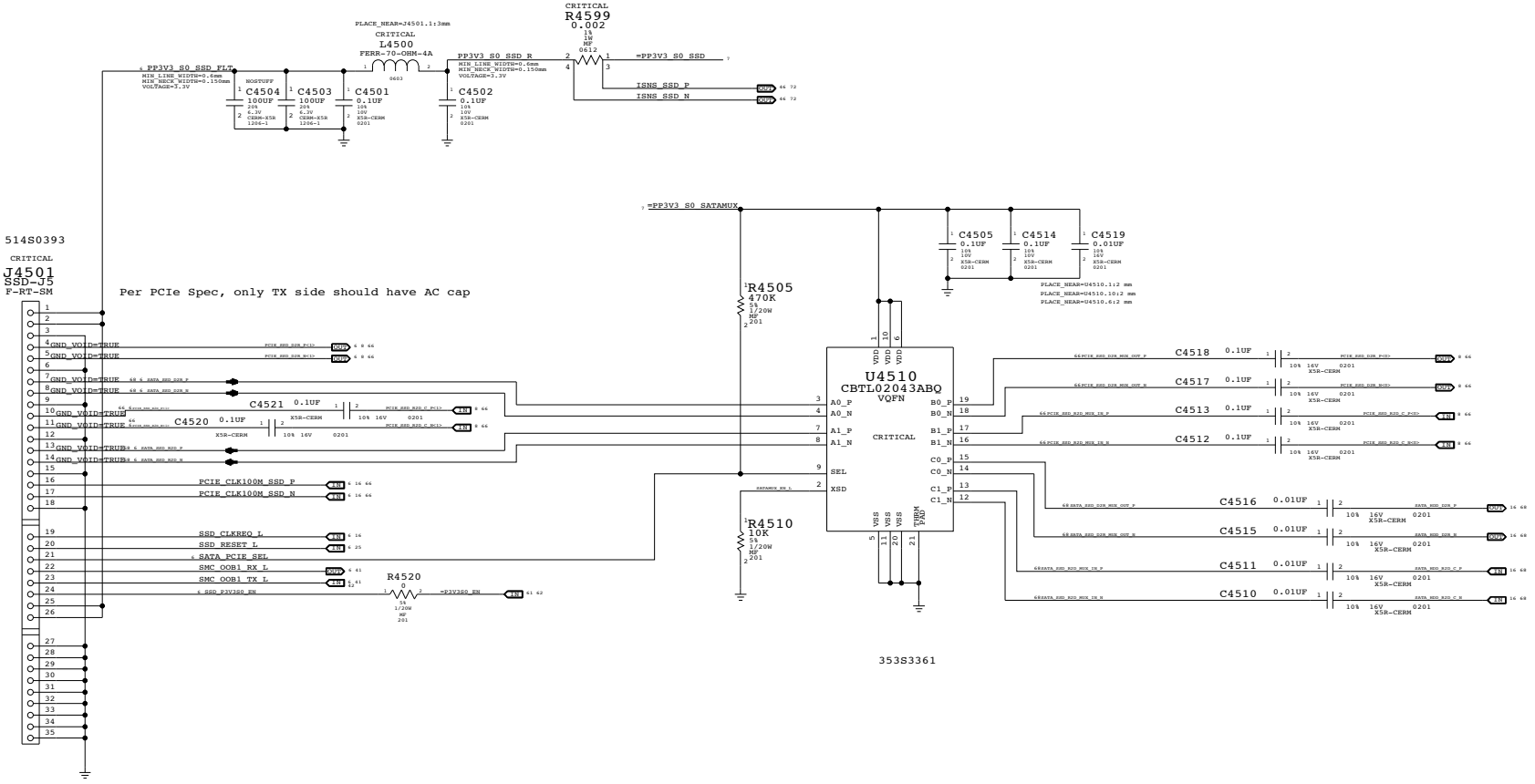

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC MASTER=J13_MLB_NON_POR	SYNC DATE=10/17/2013
PAGE TITLE: SSD CONNECTOR	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
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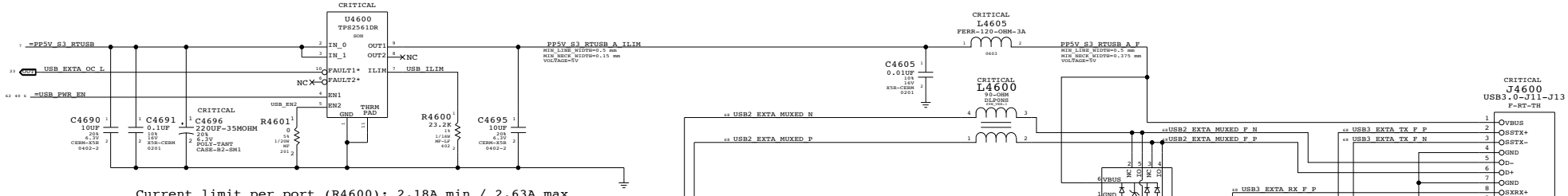
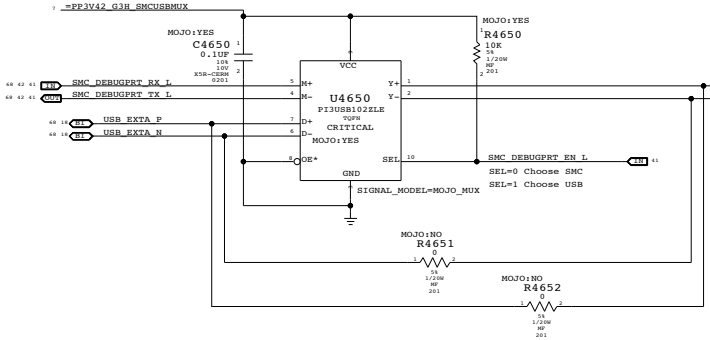
Right USB Port A

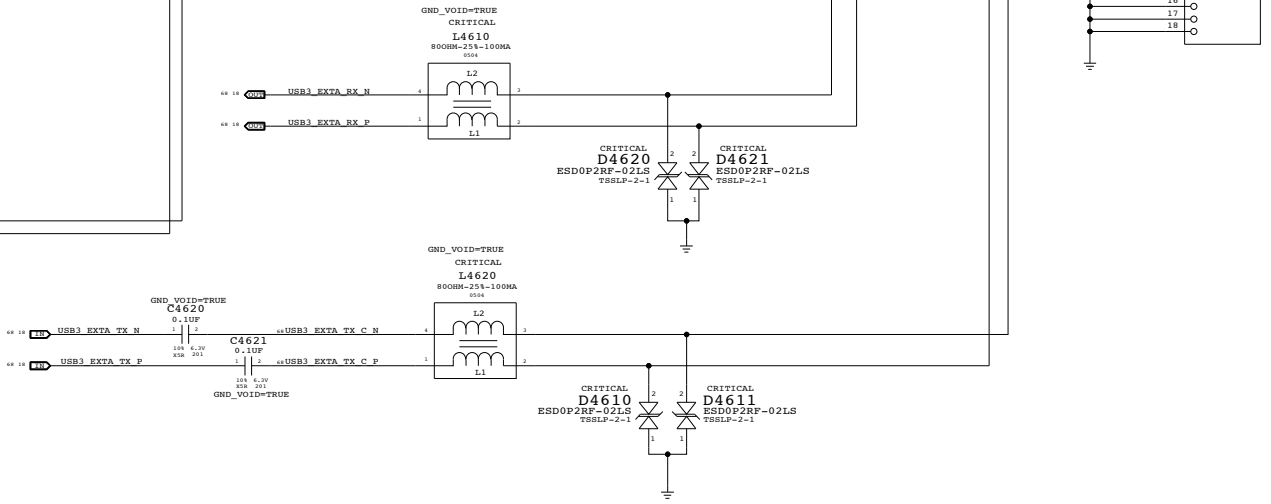
USB Port Power Switch



Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux





SYNC MASTER=J11_MLB	SYNC DATE=09/30/2013
PAGE TITLE: External A USB3 Connector	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
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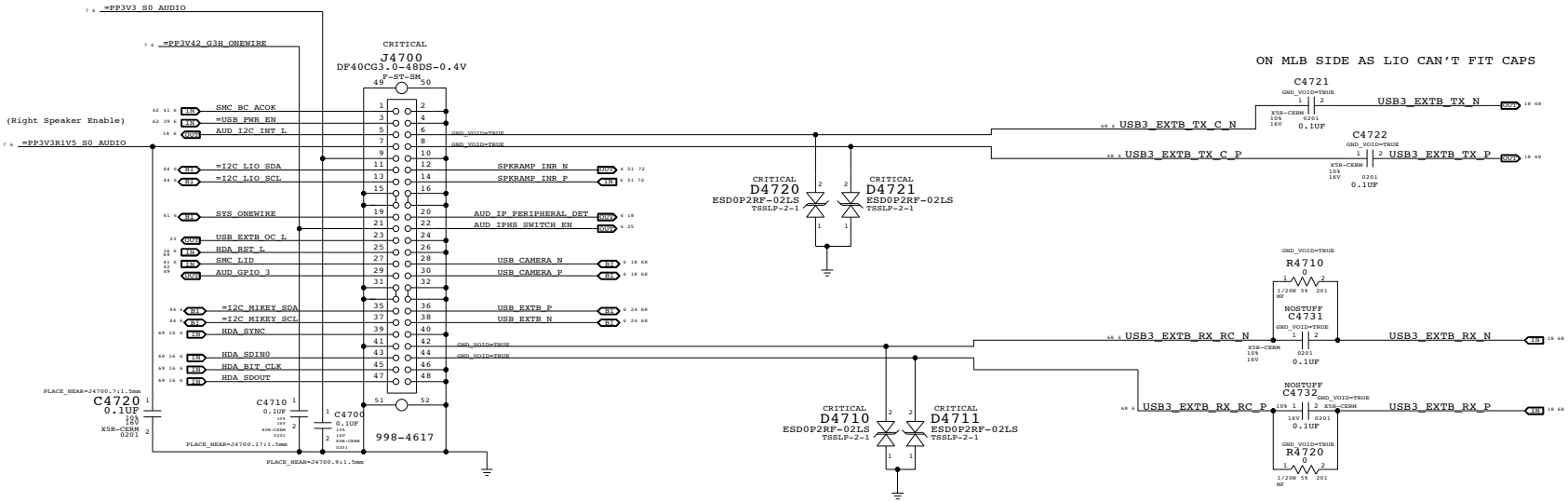

SYNC MASTER=J13_MLB_NON_POR SYNC DATE=11/10/2011

PAGE TITLE

Left I/O (LIO) Connector

Apple Inc.

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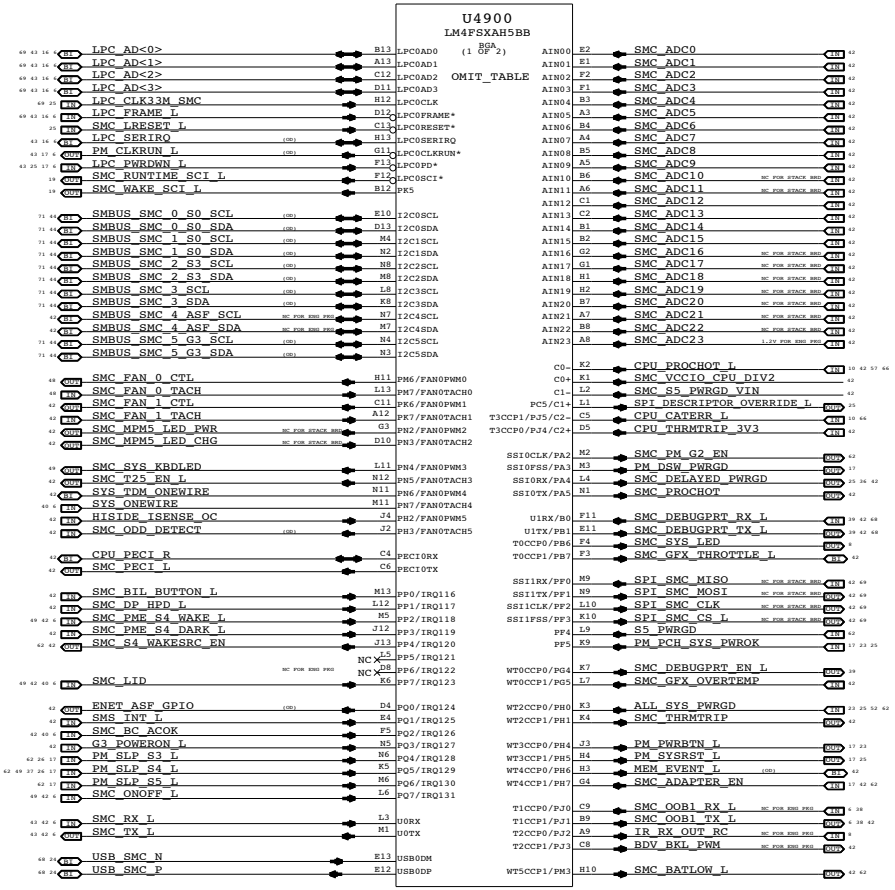
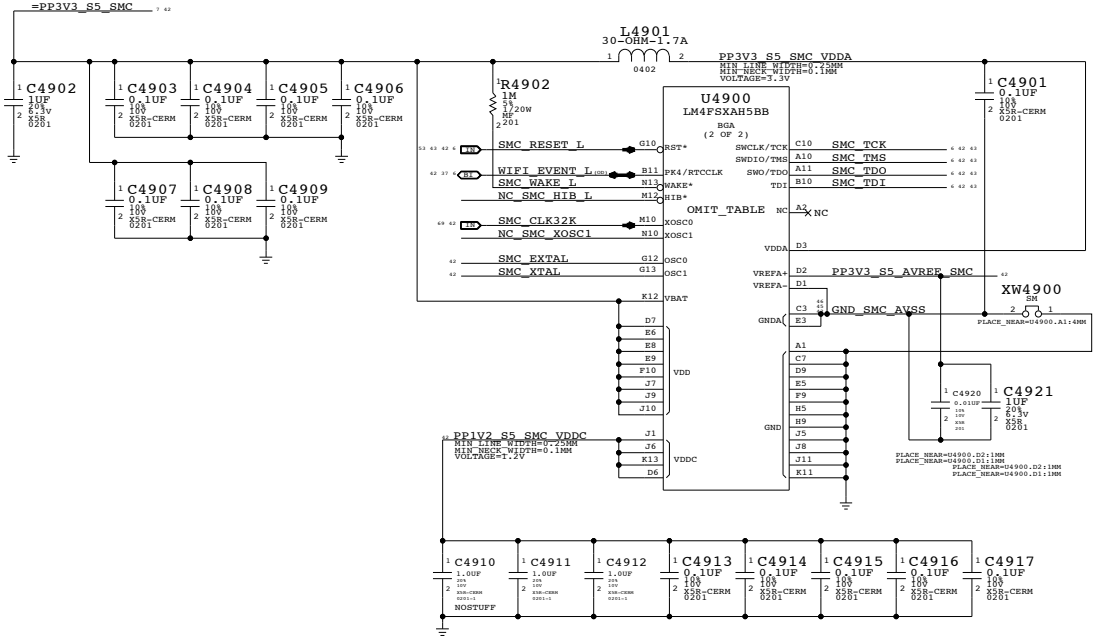


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2013

PAGE TITLE
SMC

Apple Inc.

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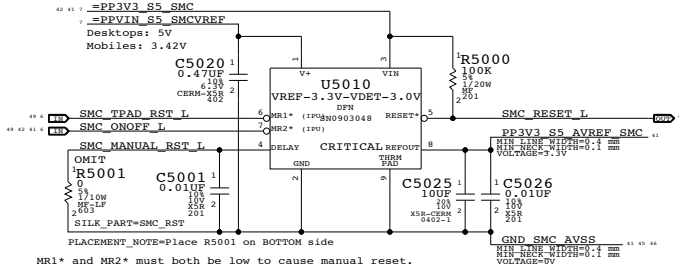
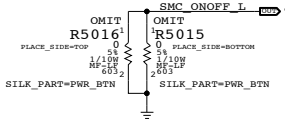
SMC Reset "Button", Supervisor & AVREF Supply



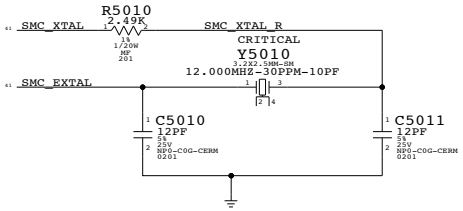
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



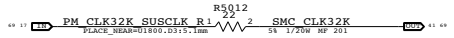
SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz



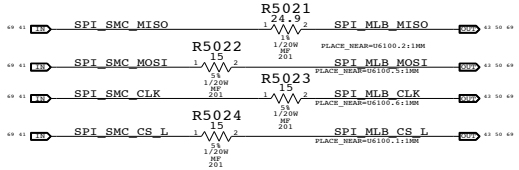
Note:
ADC10 and ADC11 are shared with comparators on Stack Board.

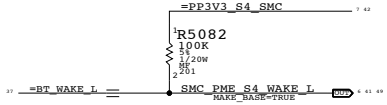
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_VCCSA_VSENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_HS_COMPUTING_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_ADC13	SMC_CPU_SA_ISENSE	MAKE_BASE=TRUE
SMC_ADC14	SMC_3V3S0_ISENSE	MAKE_BASE=TRUE
SMC_ADC15	SMC_WLAN_ISENSE	MAKE_BASE=TRUE
SMC_ADC16	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC17	NC_SCM_ADC17	MAKE_BASE=TRUE
SMC_ADC18	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE
SMC_ADC23	SMC_ADC23	MAKE_BASE=TRUE
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
ENET_ASF_GPIO	NC_ENET_ASF_GPIO	MAKE_BASE=TRUE
SMC_MPM5_LED_PWR	NC_SMC_MPM5_LED_PWR	MAKE_BASE=TRUE
SMC_MPM5_LED_CHG	NC_SMC_MPM5_LED_CHG	MAKE_BASE=TRUE
SYS_TDM_ONEWIRE	NC_SYS_TDM_ONEWIRE	MAKE_BASE=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
HISIDE_ISENSE_OC	NC_HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE
BDV_BKL_PWM	SMC_BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	SDCONN_STATE_CHANGE_SMC	MAKE_BASE=TRUE
	=TBT_WAKE_L	
SMC_T25_EN_L	NC_SMC_T25_EN_L	MAKE_BASE=TRUE

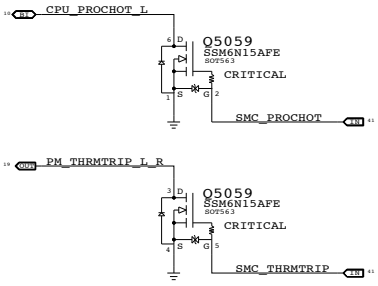


SMC12 SPI Support

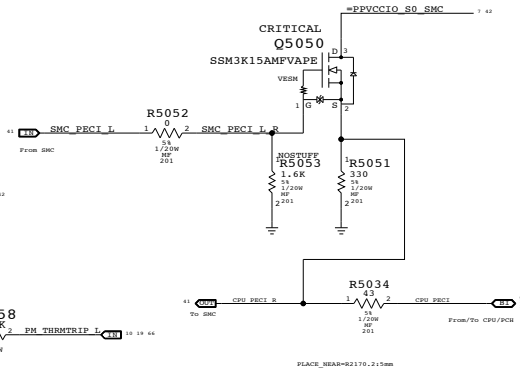
Series resistors are no stuffed until the topology of 2 SPI Masters are verified.





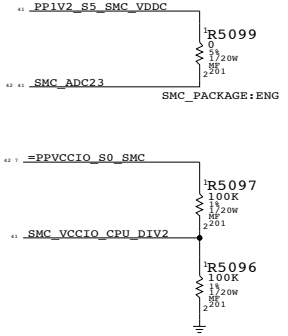


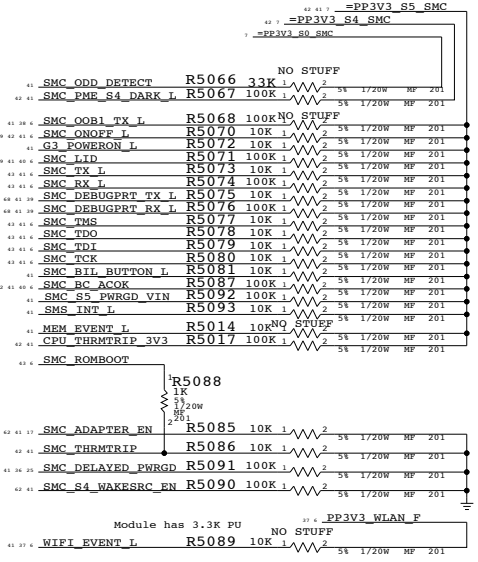
SMC12 PECI Support



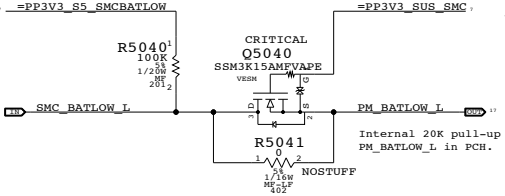
SMC12 Eng Pkg Support

Eng Package requires 1.2V ON SMC_ADC23 pin.





BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SYNC MASTER=J13 MLB NON POR
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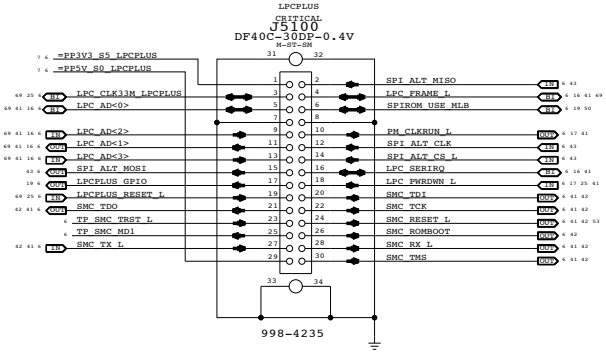
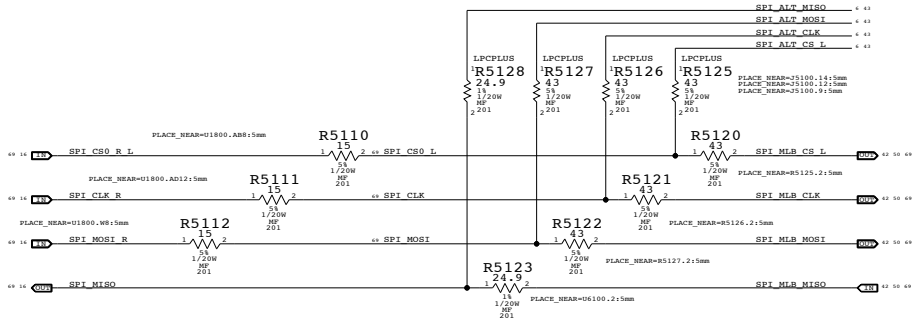
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=J11_MLB SYNC DATE=09/08/2011

PAGE TITLE

LPC+SPI Debug Connector

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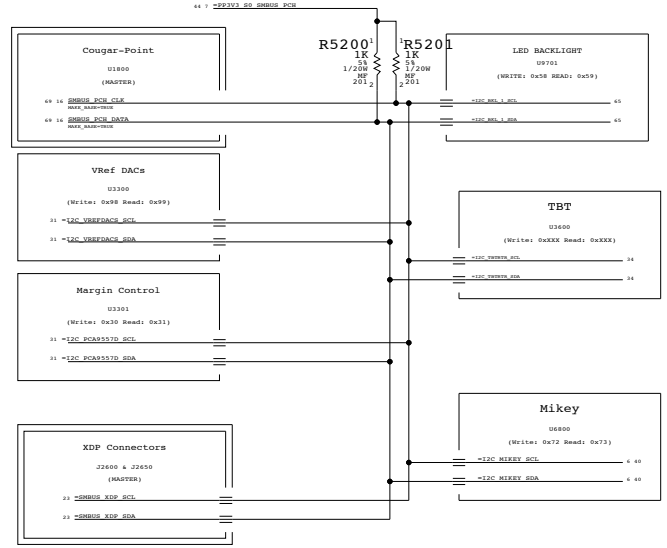
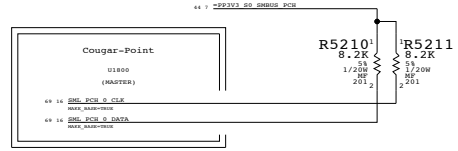
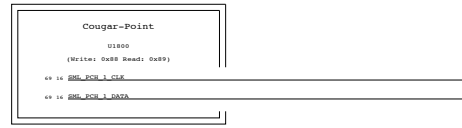
PCH S0 SMBus "0" Connections



PCH S0 "SMLink 0" Connections

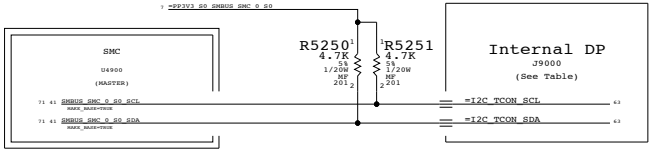


PCH S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH

SMC "0" SMBus S0 Connections

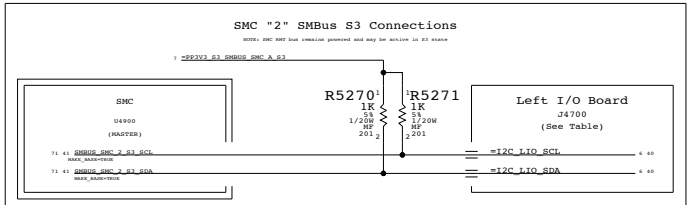


(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con – (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con – (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR – (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

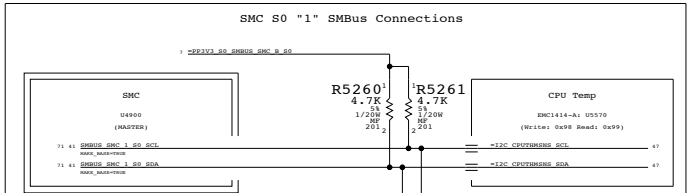
SMC "2" SMBus S3 Connections



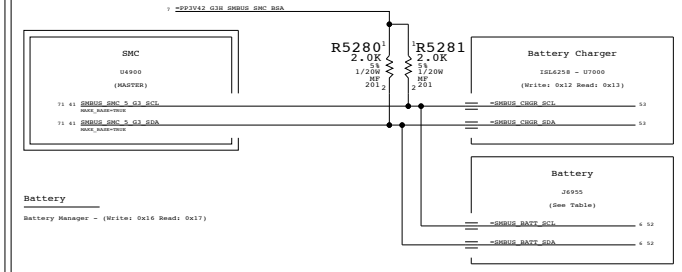
Left I/O Board

ALS – (write: 0x72 Read: 0x73)
Finstack Temp – (Write: 0x92 Read: 0x93)

SMC S0 "1" SMBus Connections



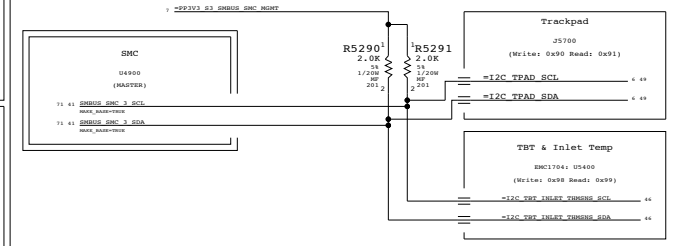
SMC "5" SMBus G3H Connections



Battery

Battery Manager – (Write: 0x16 Read: 0x17)

SMC "3" SMBus S3 Connections



SYNC MASTER=J11 MLB — SYNC DATE=10/04/2011

PAGE TITLE

SMBus Connections

Apple Inc.

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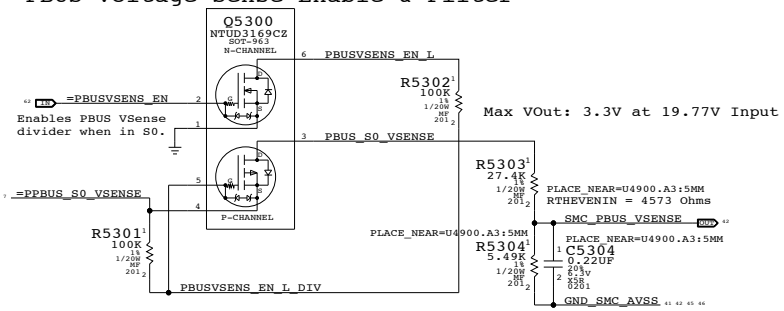
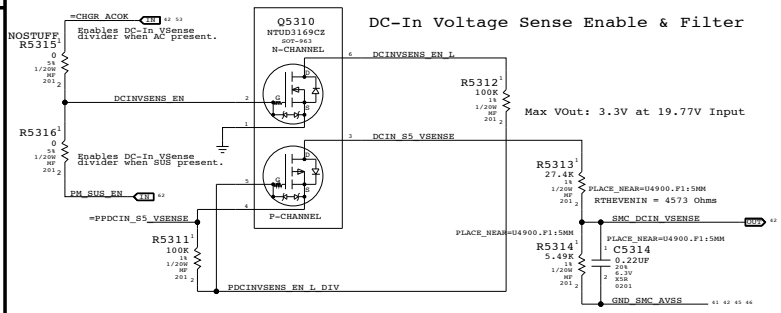
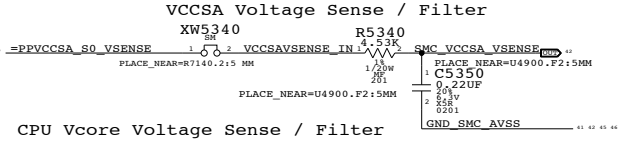
PBUS Voltage Sense Enable & Filter



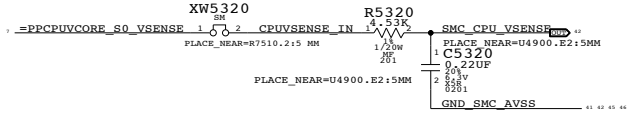
DC-In Voltage Sense Enable & Filter



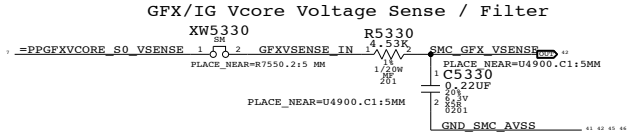
VCCSA Voltage Sense / Filter



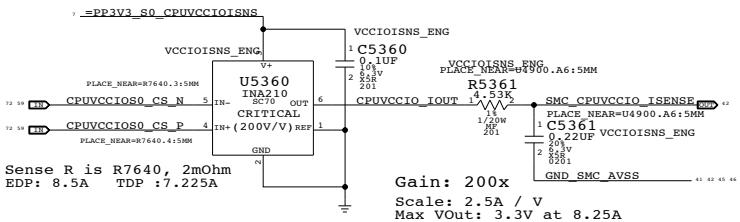
CPU Vcore Voltage Sense / Filter



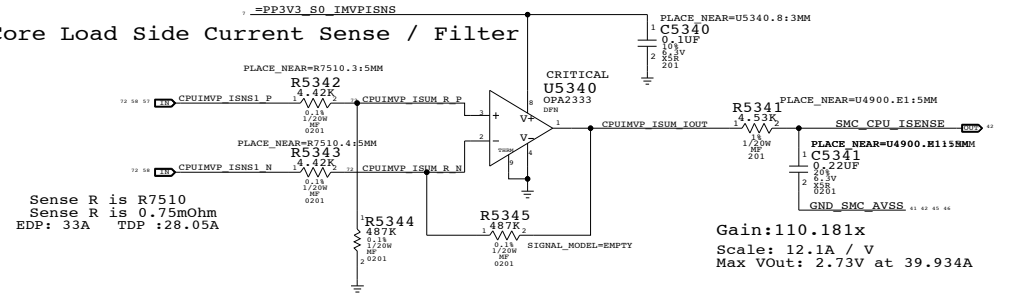
GFX/IG Vcore Voltage Sense / Filter



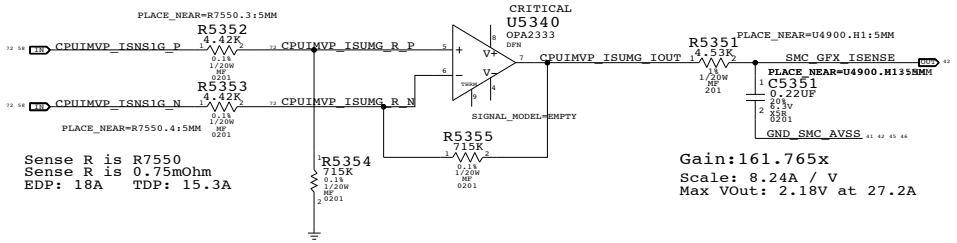
CPU 1.05V VCCIO Current Sense / Filter



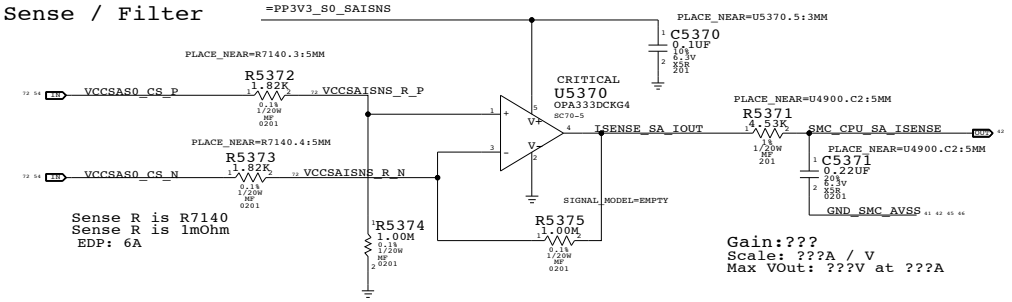
CPU VCore Load Side Current Sense / Filter



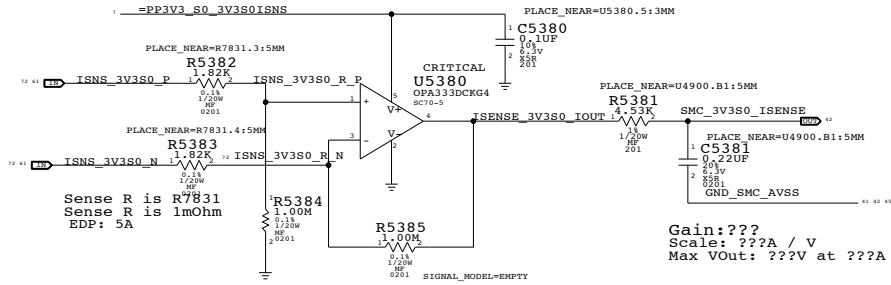
GFX/IG VCore Load Side Current Sense / Filter



CPU SA Current Sense / Filter



3.3V S0 FET Current Sense / Filter



SYNC MASTER=J11_MLB SYNC DATE=12/02/2011

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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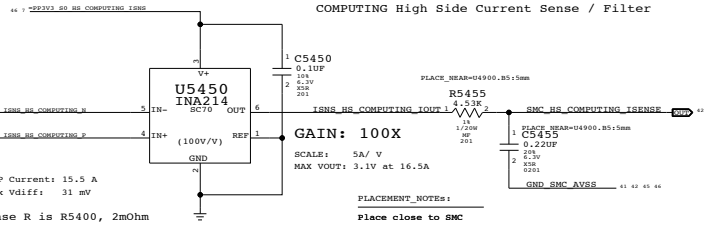
COMPUTING High Side Current Sense / Filter



GAIN: 100X

SCALE: 5A/ V

MAX VOUT: 3.1V at 16.5A

EDP Current: 15.5 A

Max Vdiff: 31 mV

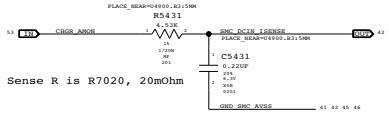
Sense R is R5400, 2mOhm

PLACEMENT_NOTEs:

Place close to SMC

(For R and C)

DC-IN (AMON) Current Sense Filter



Sense R is R7020, 20mOhm

DC-In AMON

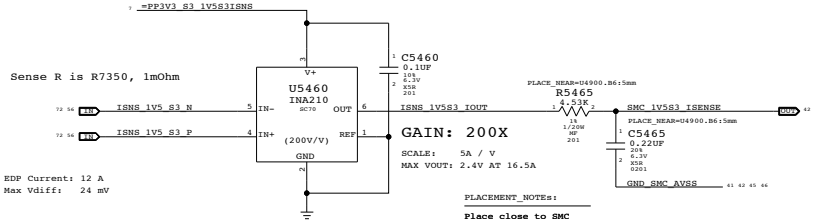
ISL6259 Gain: 20x

Scale: 2.5A / V

Max VOut: 1.4V at 8.25A

EDP Current: 3.5A

DDR3 1V5R1V35 Current Sense / Filter



Sense R is R7350, 1mOhm

GAIN: 200X

SCALE: 5A / V

MAX VOUT: 2.4V AT 16.5A

EDP Current: 12 A

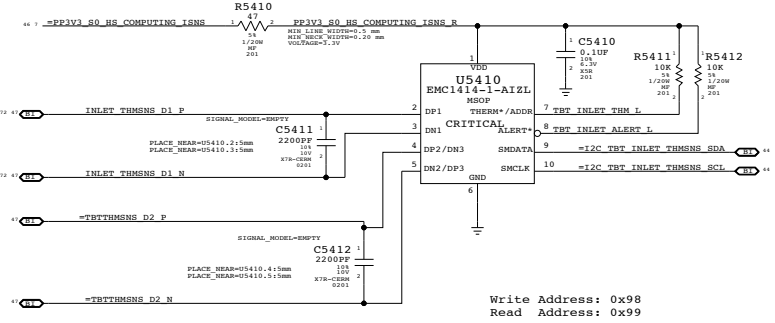
Max Vdiff: 24 mV

PLACEMENT_NOTEs:

Place close to SMC

(For R and C)

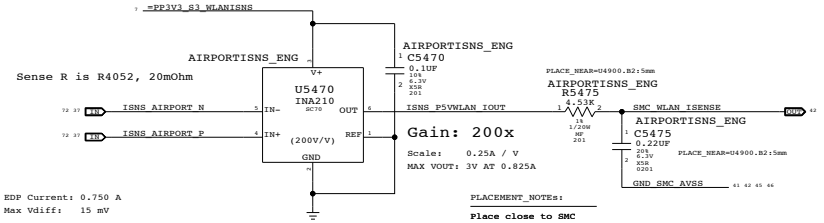
TBT/Inlet Temp Sensor



Write Address: 0x98

Read Address: 0x99

AirPort Current Sense / Filter



Sense R is R4052, 20mOhm

Gain: 200x

Scale: 0.25A / V

MAX VOUT: 3V AT 0.825A

EDP Current: 0.750 A

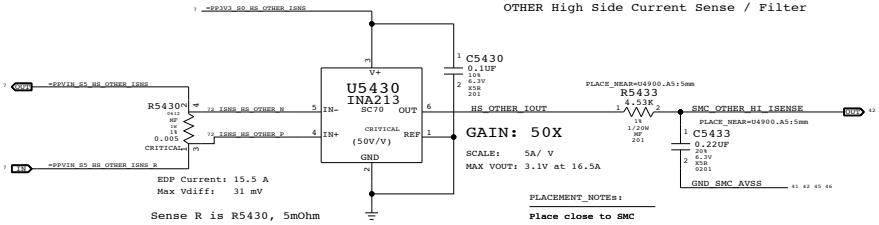
Max Vdiff: 15 mV

PLACEMENT_NOTEs:

Place close to SMC

(For R and C)

OTHER High Side Current Sense / Filter



EDP Current: 15.5 A

Max Vdiff: 31 mV

Sense R is R5430, 5mOhm

GAIN: 50X

SCALE: 5A/ V

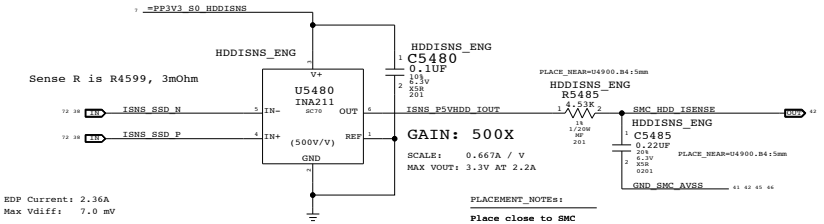
MAX VOUT: 3.1V at 16.5A

PLACEMENT_NOTEs:

Place close to SMC

(For R and C)

HDD Current Sense / Filter



Sense R is R4599, 3mOhm

GAIN: 500X

SCALE: 0.667A / V

MAX VOUT: 3.3V AT 2.2A

EDP Current: 2.36A

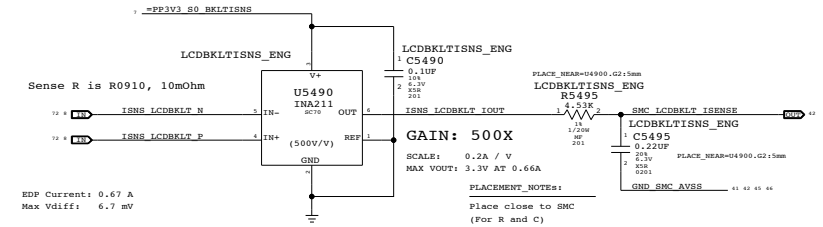
Max Vdiff: 7.0 mV

PLACEMENT_NOTEs:

Place close to SMC

(For R and C)

LCD Backlight Driver Input Current Sense / Filter



Sense R is R0910, 10mOhm

GAIN: 500X

SCALE: 0.2A / V

MAX VOUT: 3.3V AT 0.66A

EDP Current: 0.67 A

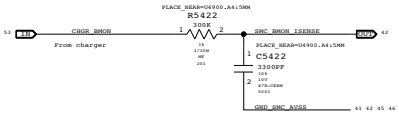
Max Vdiff: 6.7 mV

PLACEMENT_NOTEs:

Place close to SMC

(For R and C)

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



Charger BMON (Production) Solution

ISL6259 Gain: 36x

Scale: 2.78A / V

Max VOut: 3.3V at 9.167A

EDP Current: 310A

SYNC MASTER=J13 MLB NON POR	SYNC DATE=10/17/2011
PAGE TITLE: High Side Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
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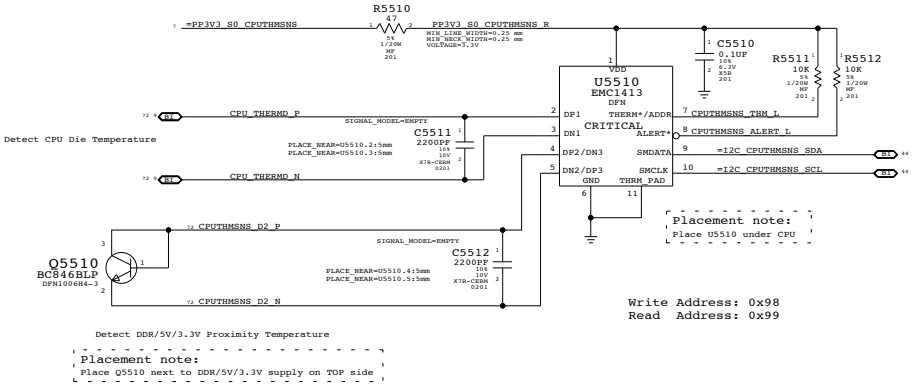
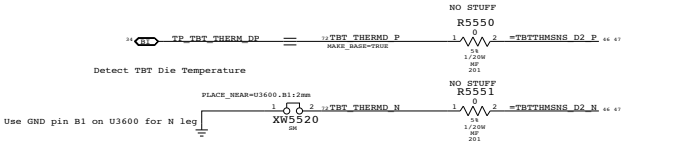
	SHEET: 46 OF 73

CPU Proximity Sensor



TBT Die

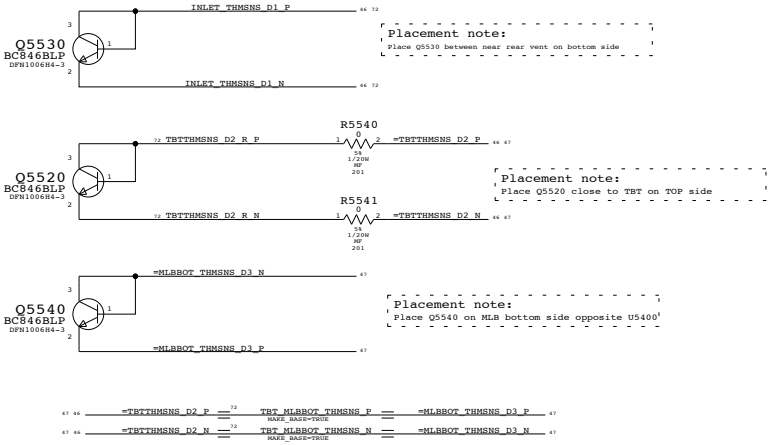


To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors



SYNC MASTER=J11_MLB SYNC DATE=08/03/2011

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 55 OF 109
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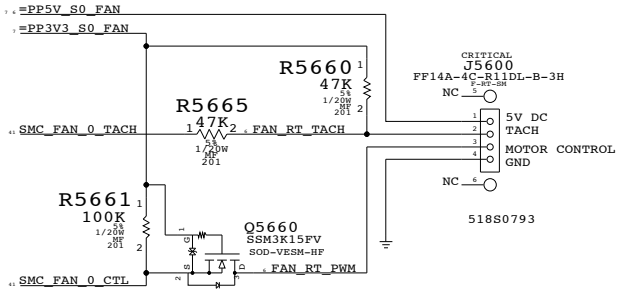
FAN CONNECTOR



SYNC MASTER=K21_MLB SYNC DATE=07/28/2011

PAGE TITLE: Fan

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

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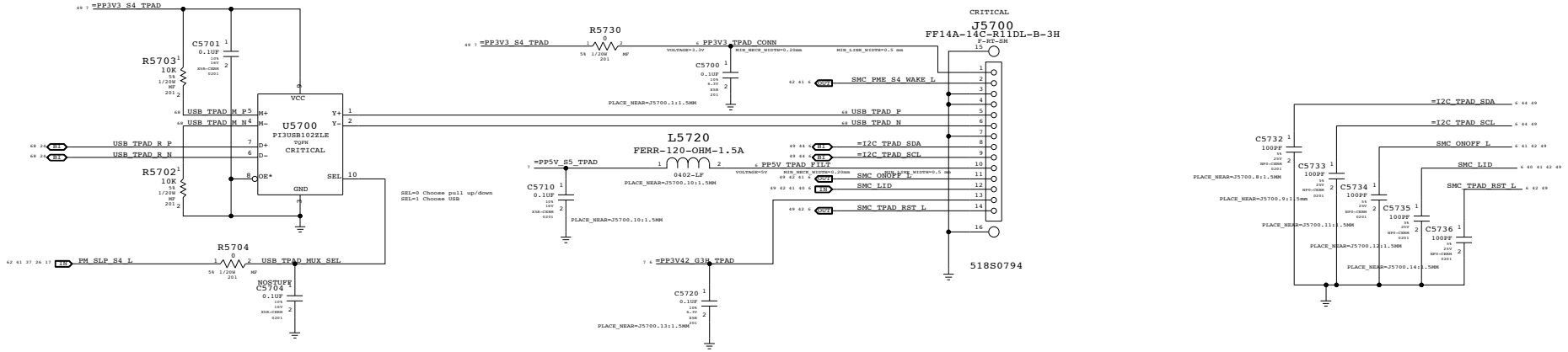
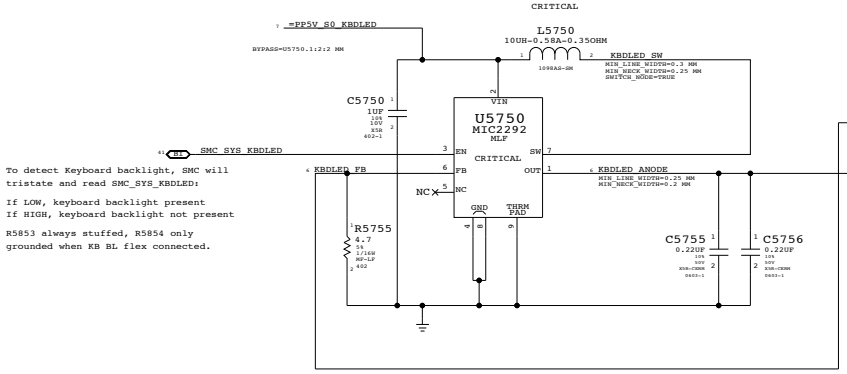
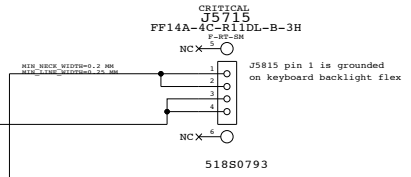
IPD Flex Connector



Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE: IPD / KBD Backlight

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

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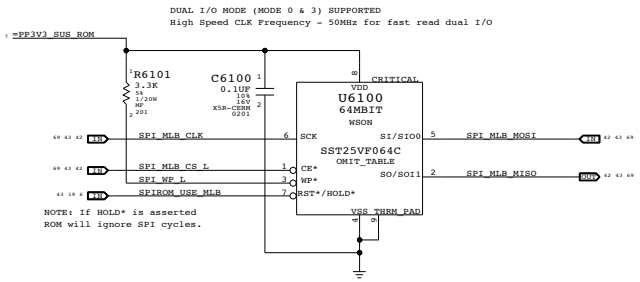

SYNC MASTER=K21_MLB SYNC DATE=07/28/2011

PAGE TITLE

SPI ROM

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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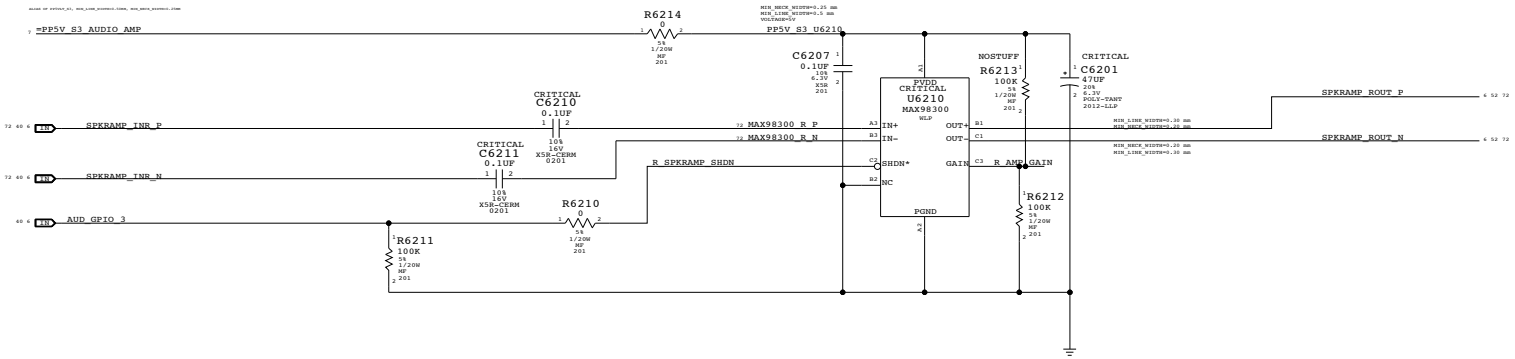
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC MASTER=J11_MLB SYNC DATE=09/30/2013

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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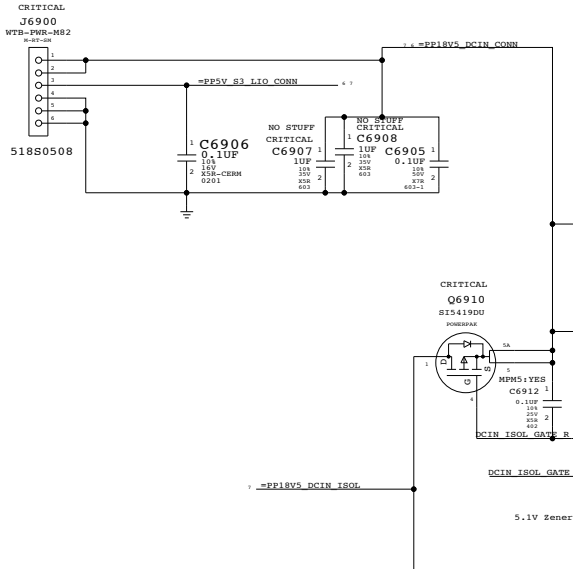
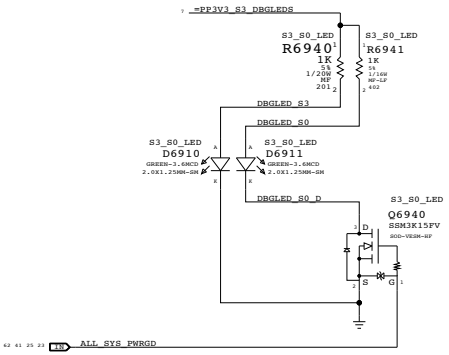
MLB to LIO Power Cable Connector

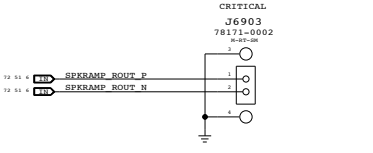


Debug LEDs

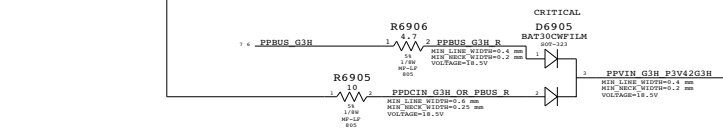
(For development only)



Right Speaker Connector

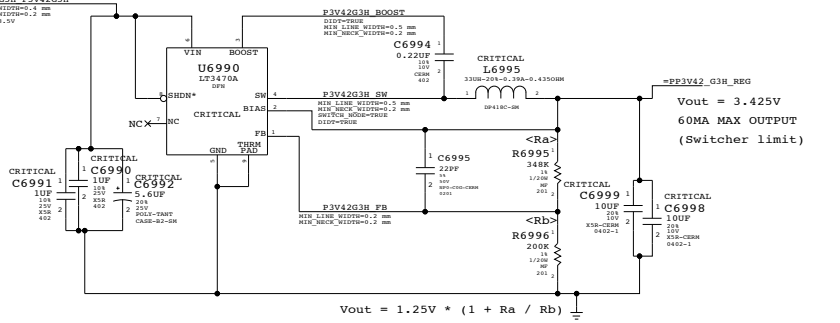


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,1/20W,90.9KOHM,1,0201,SMD	R6912		MPM5:YES
117S0008	1	RES,MF,1/20W,100KOHM,1,0201,SMD	R6911		MPM5:YES



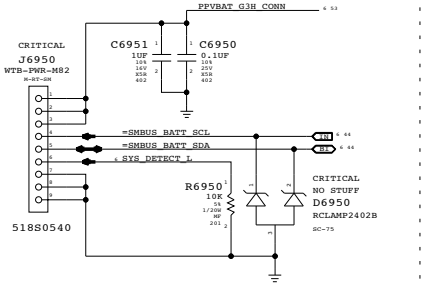
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



K16-Specific

Battery Connector



SYNC MASTER=J13 MLB NON POP — SYNC DATE=11/10/2011

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-9277 — SIZE D

REVISION 2.8.0

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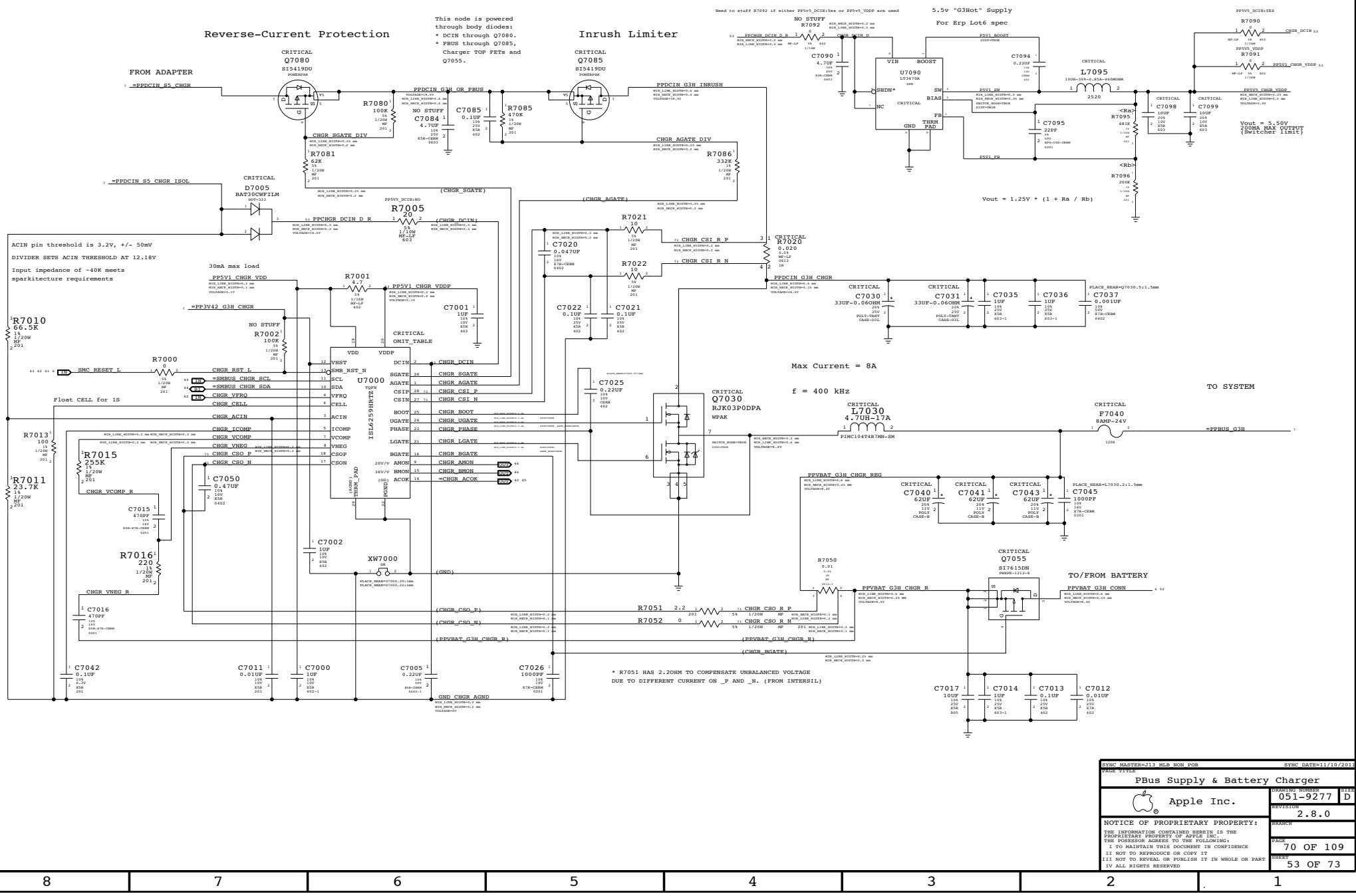

SYNC MASTER=J13_MLB_NON_POR	SYNC DATE=11/10/2011
PAGE TITLE: PBus Supply & Battery Charger	
Apple Inc.	DRAWING NUMBER: 051-9277 SIZE: D
	REVISION: 2.8.0
	BRANCH:
	PAGE: 70 OF 109
	SHEET: 53 OF 73

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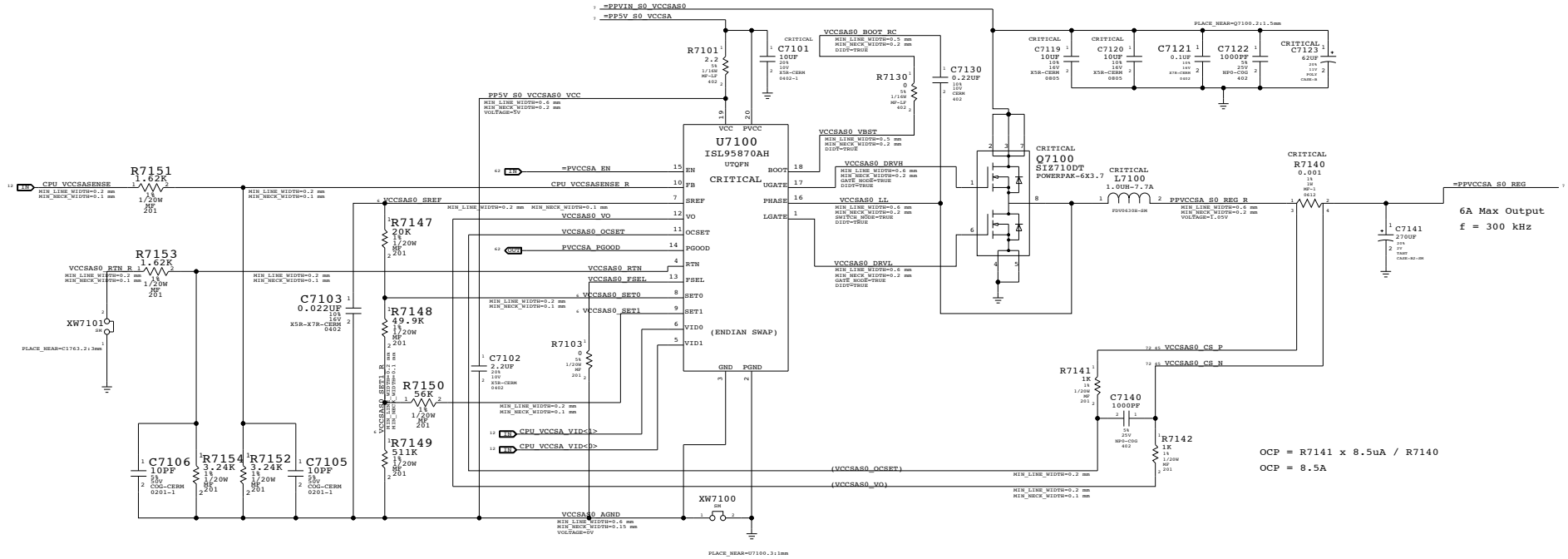

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC MASTER=J13_MLB_NON_POR SYNC DATE=10/17/2013

PAGE TITLE

System Agent Supply

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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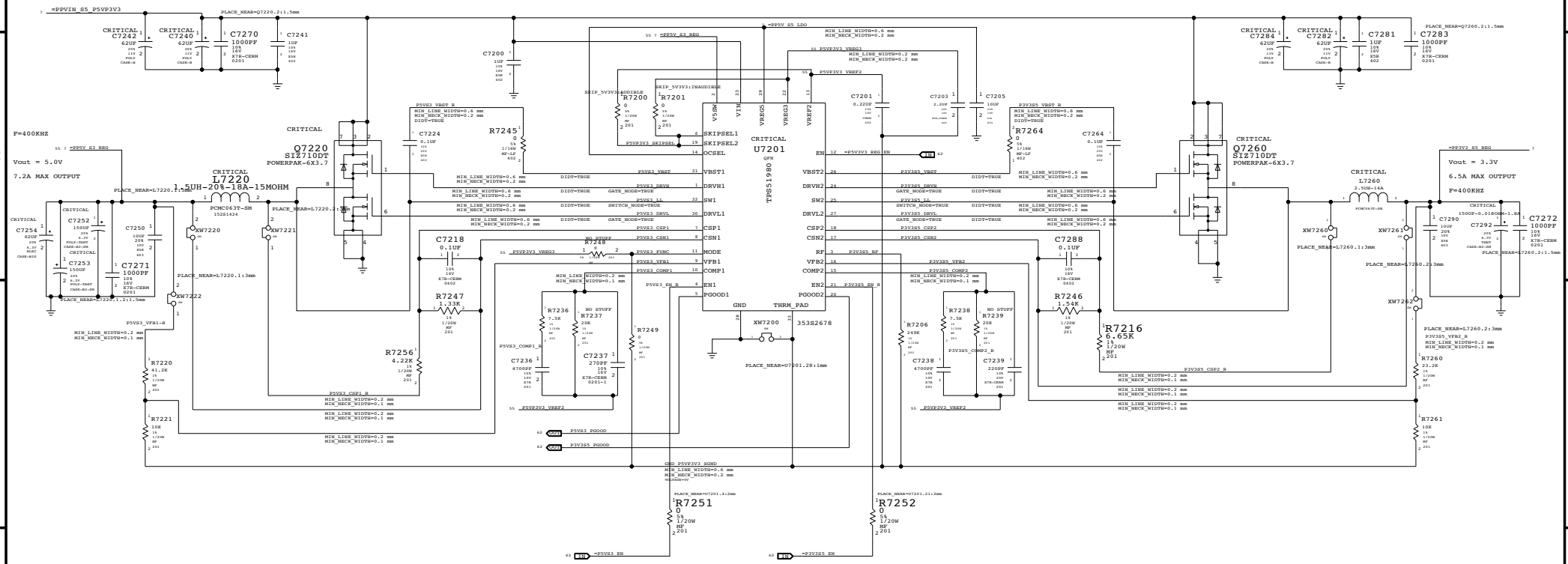

SYNC MASTER=J13_MLB_NON_POR	SYNC DATE=10/17/2013
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER 051-9277
	SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 72 OF 109
	SHEET 55 OF 73

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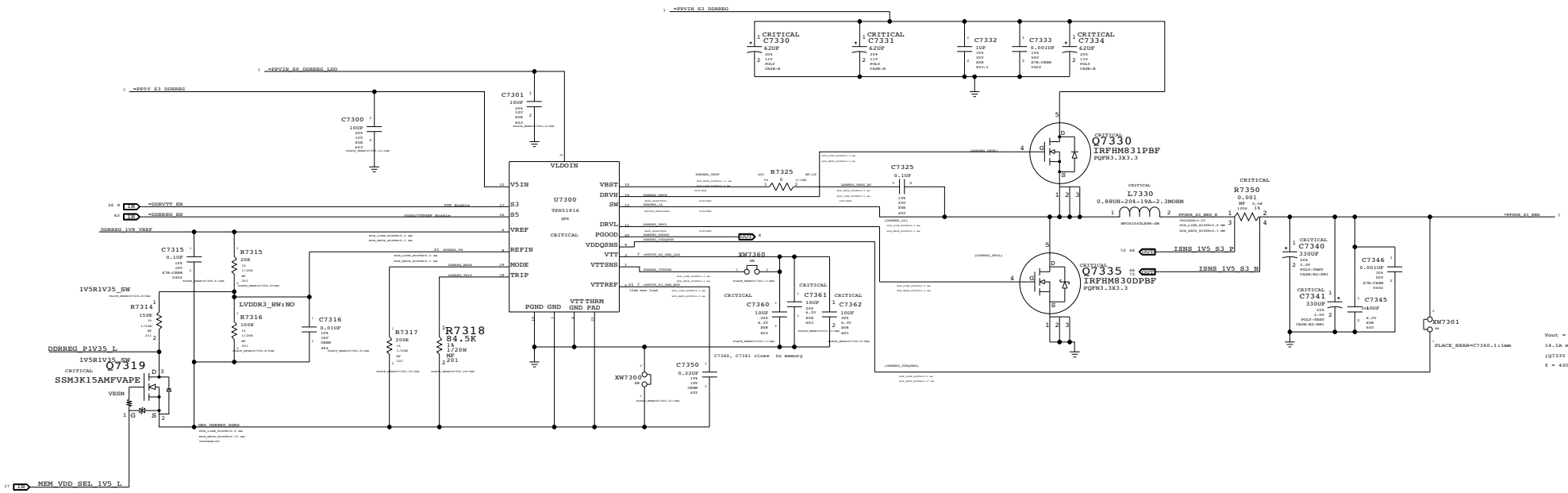

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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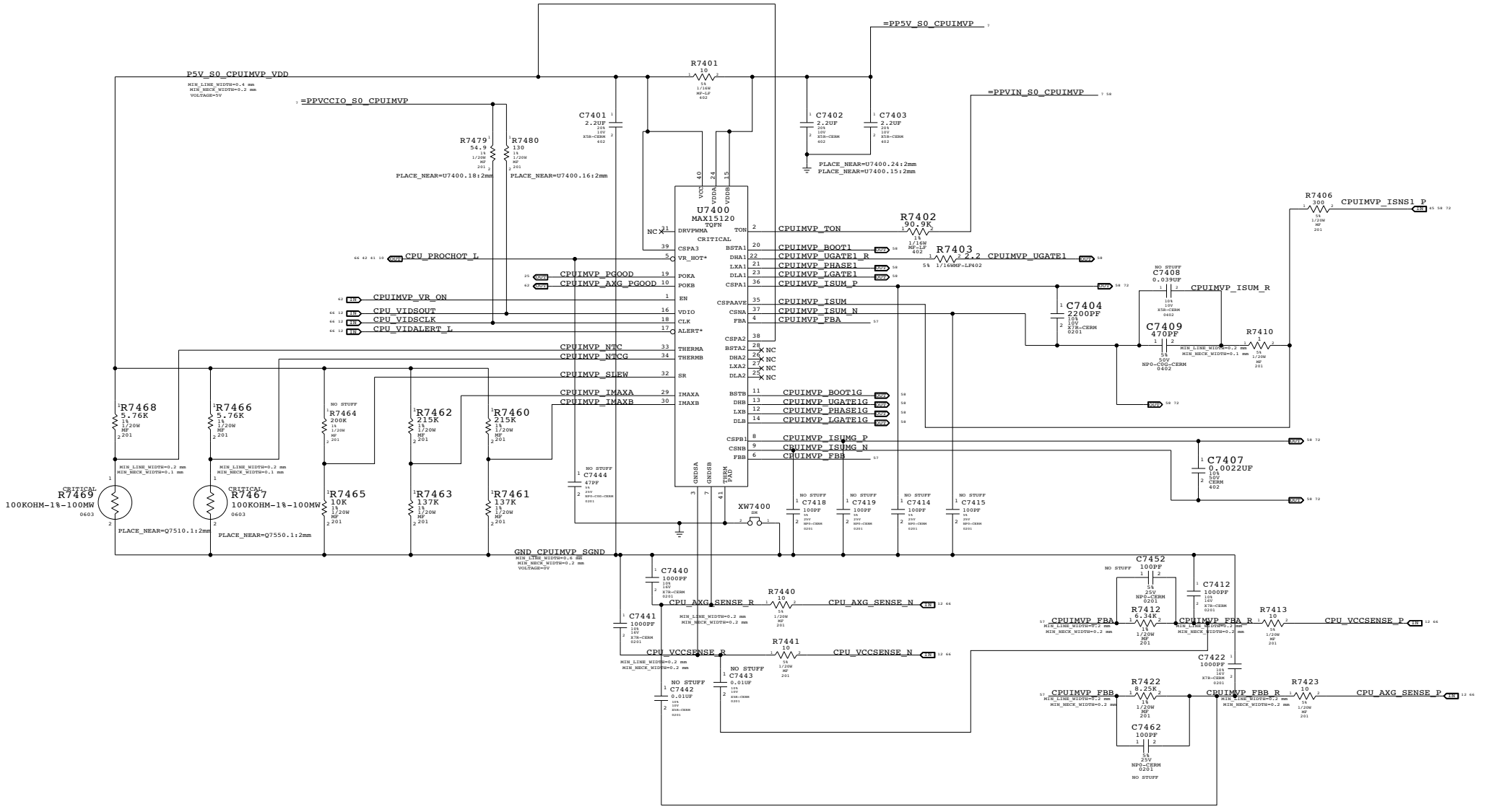

PAGE TITLE	CPU IMVP7 & AXG VCore Regulator
	Apple Inc.
DRAWING NUMBER	051-9277
SIZE	D
REVISION	2.8.0
BRANCH	
PAGE	74 OF 109
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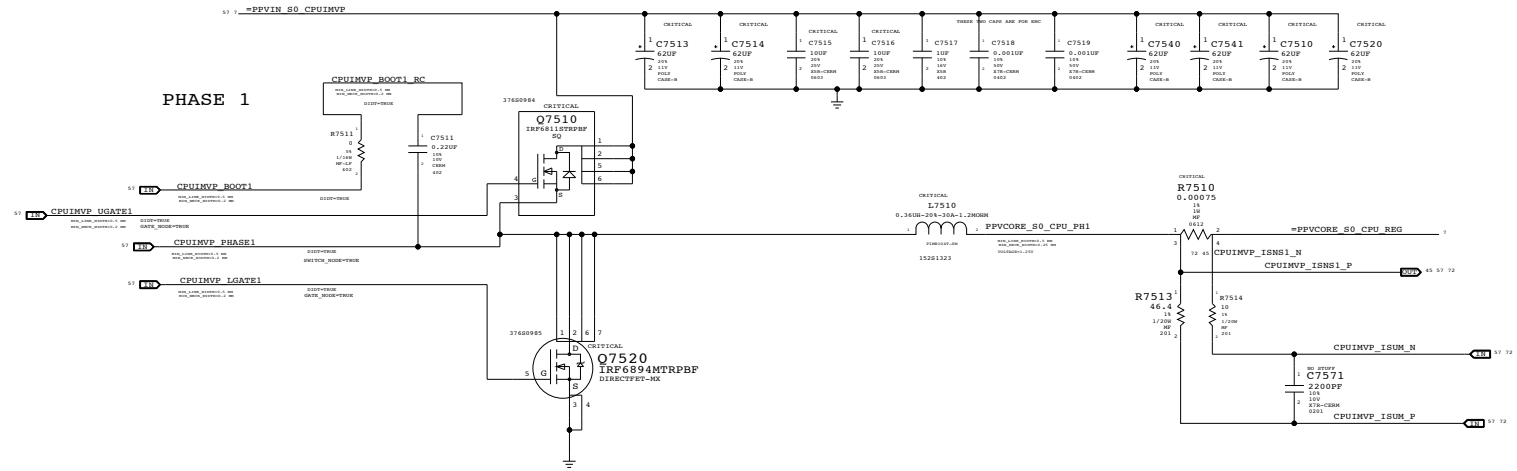
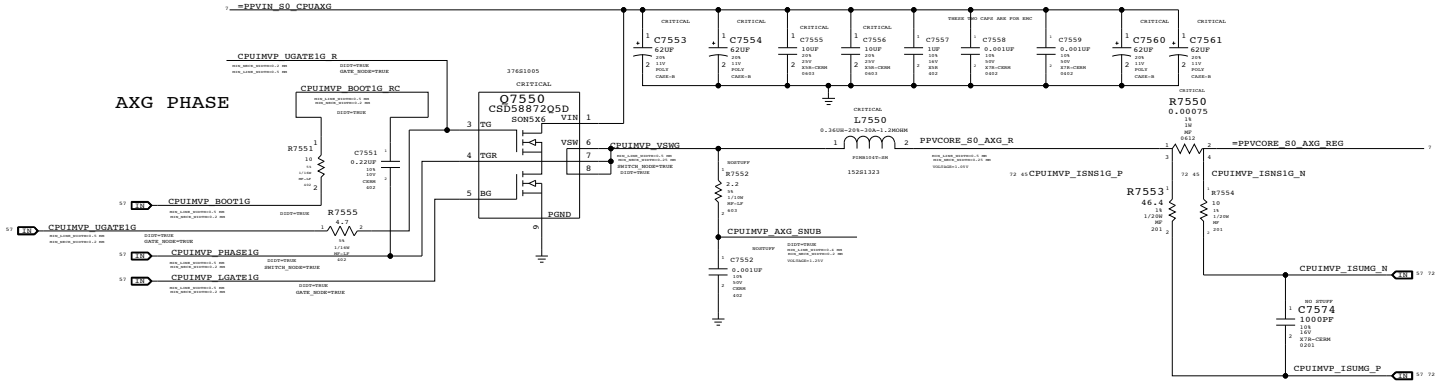
CPU=IV Bridge ULV, AXG=GT2





CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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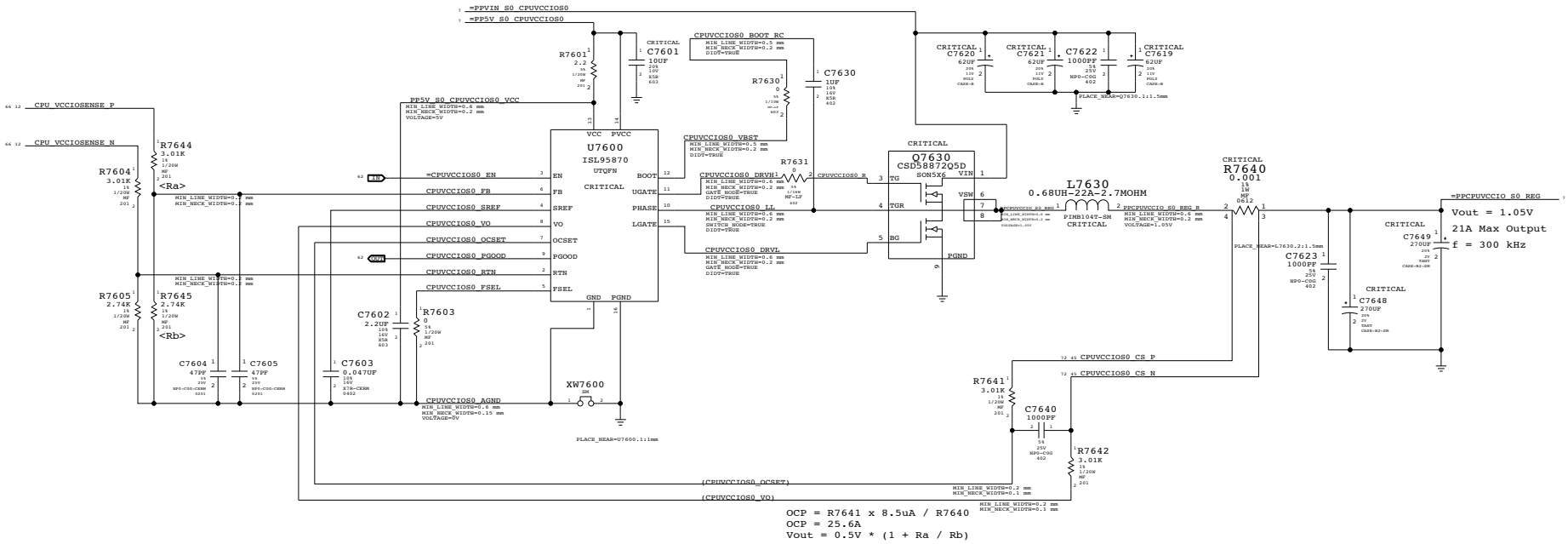
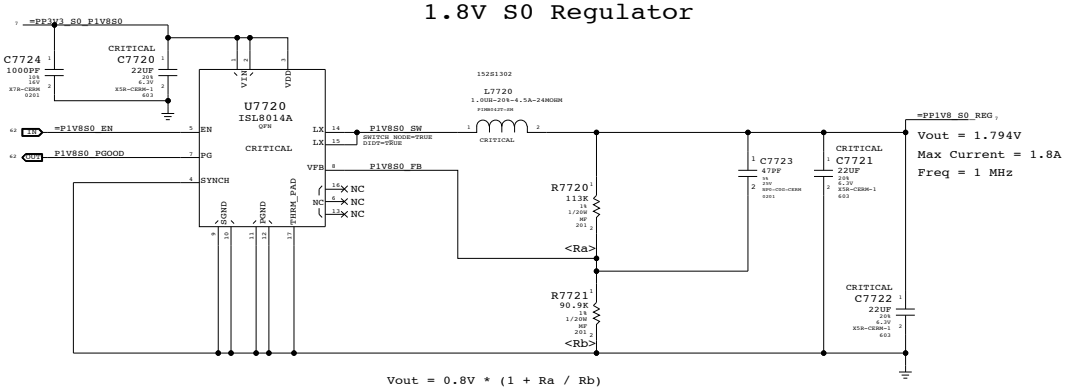
CPU VCCIO (1.05V S0) Regulator



PAGE TITLE	CPU VCCIO (1.05V) Power Supply
Apple Inc.	DRAWING NUMBER 051-9277 · SIZE D
	REVISION 2.8.0
	BRANCH
	PAGE 76 OF 109
	SHEET 59 OF 73

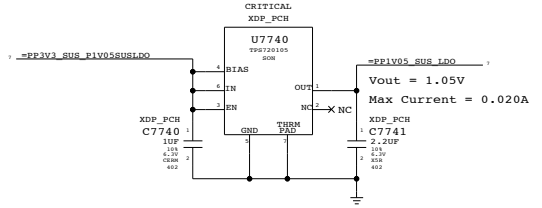
1.8V S0 Regulator



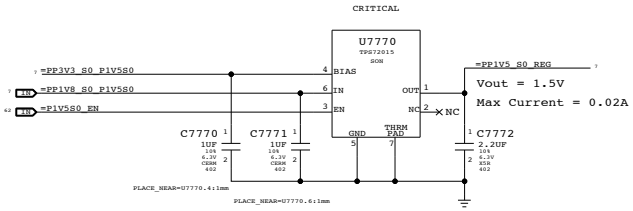
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

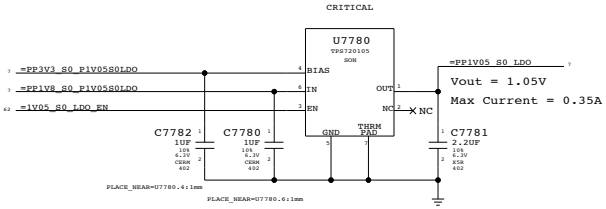
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



SYNC MASTER=K21_MLB SYNC DATE=07/28/2011

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

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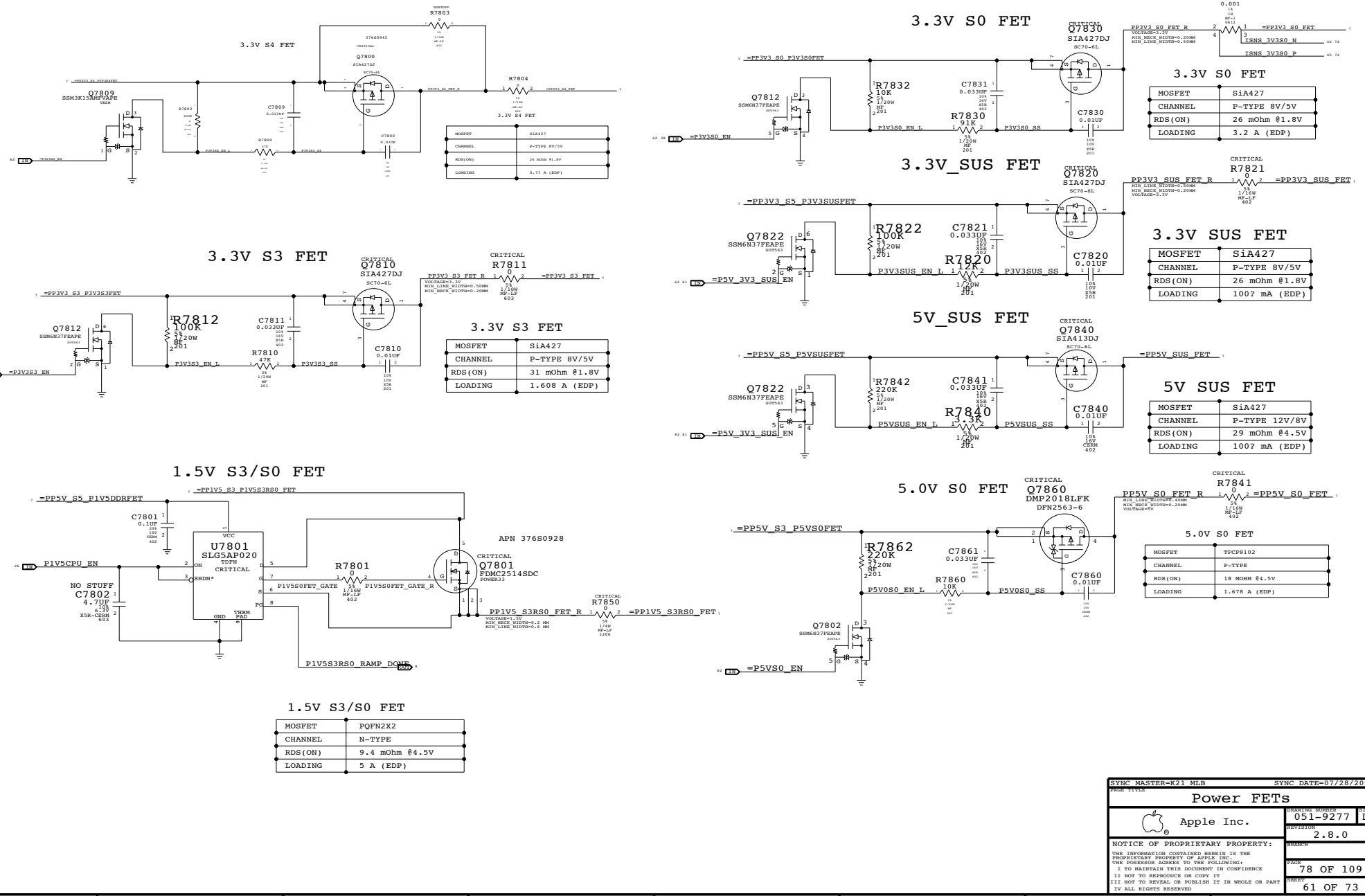
SHEET: 60 OF 73



SYNC MASTER=K21 MLB SYNC DATE=07/28/2011

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

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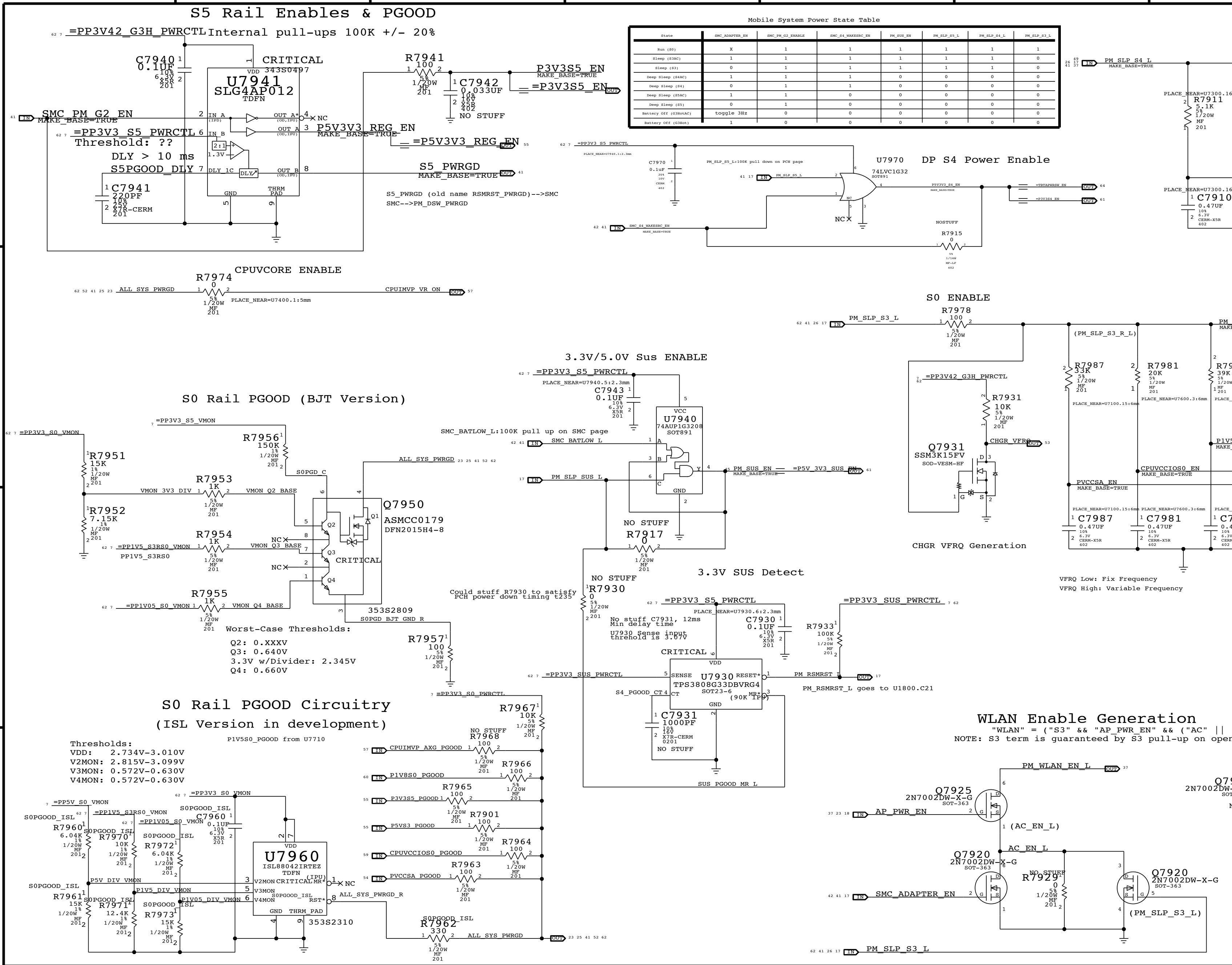
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0



SYNC MASTER=J13 MLB NON POR SYNC DATE=11/10/2011

PAGE TITLE
Power Control 1/ENABLE

DRAWING NUMBER 051-9277 SIZE D

Apple Inc.

REVISION 2.8.0

BRANCH

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0829	1	CONNTYN18-AX,P=0.4,30P,W-BOSS,HF	J9000		

LCD Connector

Internal DP Connector: 518S0787

OMIT_TABLE
CRITICAL

J9000
CABLINE-CA
P-PT-SM

CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP

=PP3V3_S3_LCD
LCD_IG_PWR_EN

CRITICAL
U9000
FPF1009
MPET-2X2-8IN
ON
VIN_1
VIN_2
VOUT_1
VOUT_2
GND
THRM PAD

R9014 1K 5% 1/20W MF 201
C9009 0.1UF 10% 6.3V X5R 201
C9011 0.1UF 10% 6.3V X5R 201
C9012 10UF 20% 6.3V X5R 603

PP3V3_SW_LCD_UP
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

Pull-ups on panel side,
4.7 kOhm to 3.3V

=I2C_TCON_SDA
R9061 0 5% 1/20W MF 201
I2C_TCON_SDA_R

=I2C_TCON_SCL
R9062 0 5% 1/20W MF 201
I2C_TCON_SCL_R

DP_INT_HPD
R9060 0 5% 1/20W MF 201
DP_INT_HPD_CONN

L9004
FERR-120-OHM-1.5A
0402-LF

C9015 1000PF 10% 16V X7R-CERN 0201

R9070 100K 5% 1/20W MF 201

PP3V3_SW_LCD
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

DP_INT_AUX_CH_N
C9024 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_N)

DP_INT_AUX_CH_P
C9025 0.1UF 10% 16V X5R-CERM 0201
(DP_INT_AUX_CH_C_P)

DP_INT_ML_P<0>
C9020 0.1UF 10% 16V X5R-CERM 0201

DP_INT_ML_N<0>
C9021 0.1UF 10% 16V X5R-CERM 0201

DP_INT_AUX_CH_C_N
DP_INT_AUX_CH_C_P
DP_INT_ML_F_P<0>
DP_INT_ML_F_N<0>

PPVOUT_SW_LCDBKLT

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1

NCX

LED Backlight I/F
DisplayPort I/F

PLACE_NEAR=J9000.25:13mm
R9017 1M 5% 1/20W MF 201
R9018 1M 5% 1/20W MF 201
PLACE_NEAR=J9000.24:13mm

PLACE_NEAR=J9000.14:2mm
R9050 100K 5% 1/20W MF 201
R9080 100K 5% 1/20W MF 201

PLACE_NEAR=J9000.3:2mm
C9017 1000PF 5% 50V C0G-CERM 603

SYNC_MASTER=K21_MLB
SYNC_DATE=07/28/2011

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-9277
SIZE D
REVISION 2.8.0
BRANCH
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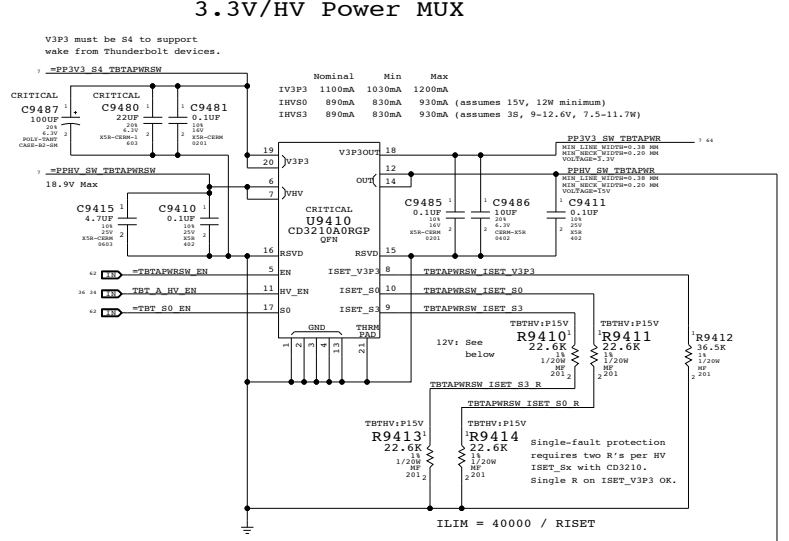
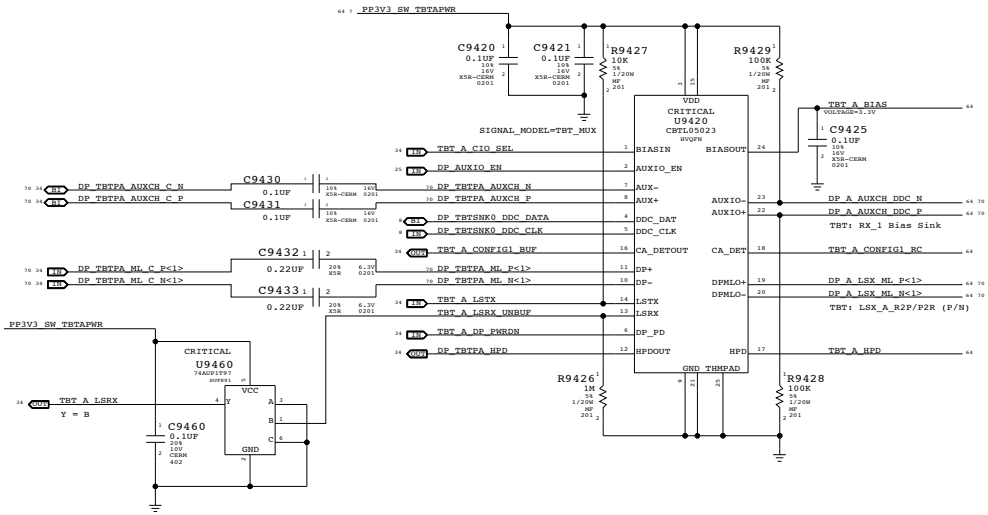
SHEET 63 OF 73

3.3V/HV Power MUX



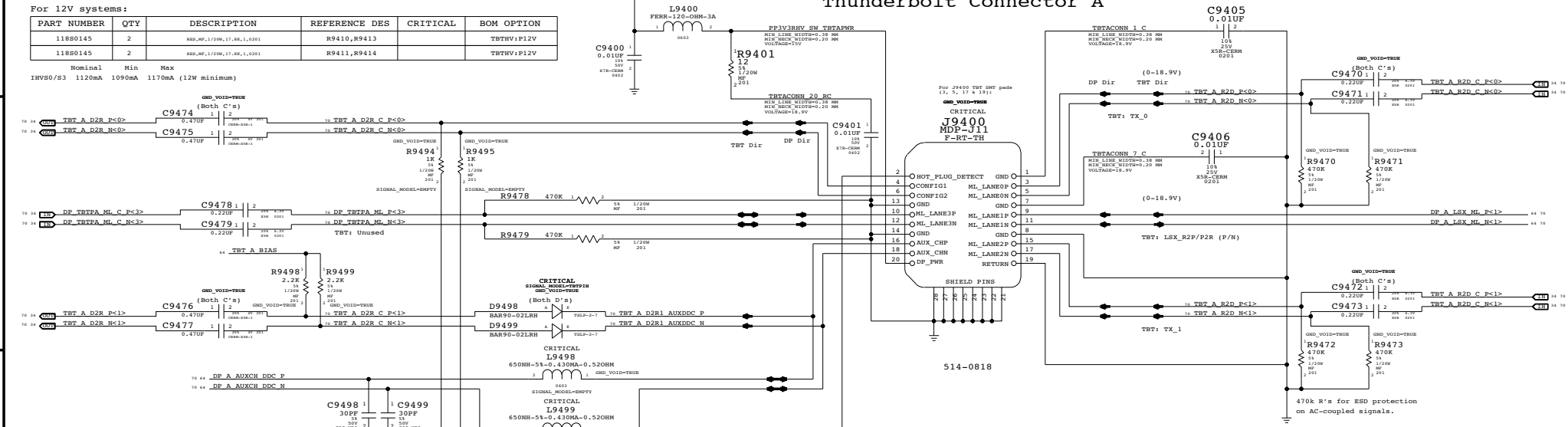


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector A



SYNC MASTER=J11_MLB SYNC DATE=10/03/2013
PAGE TITLE: Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER: 051-9277 SIZE: D
REVISION: 2.8.0
BRANCH:
PAGE: 94 OF 109
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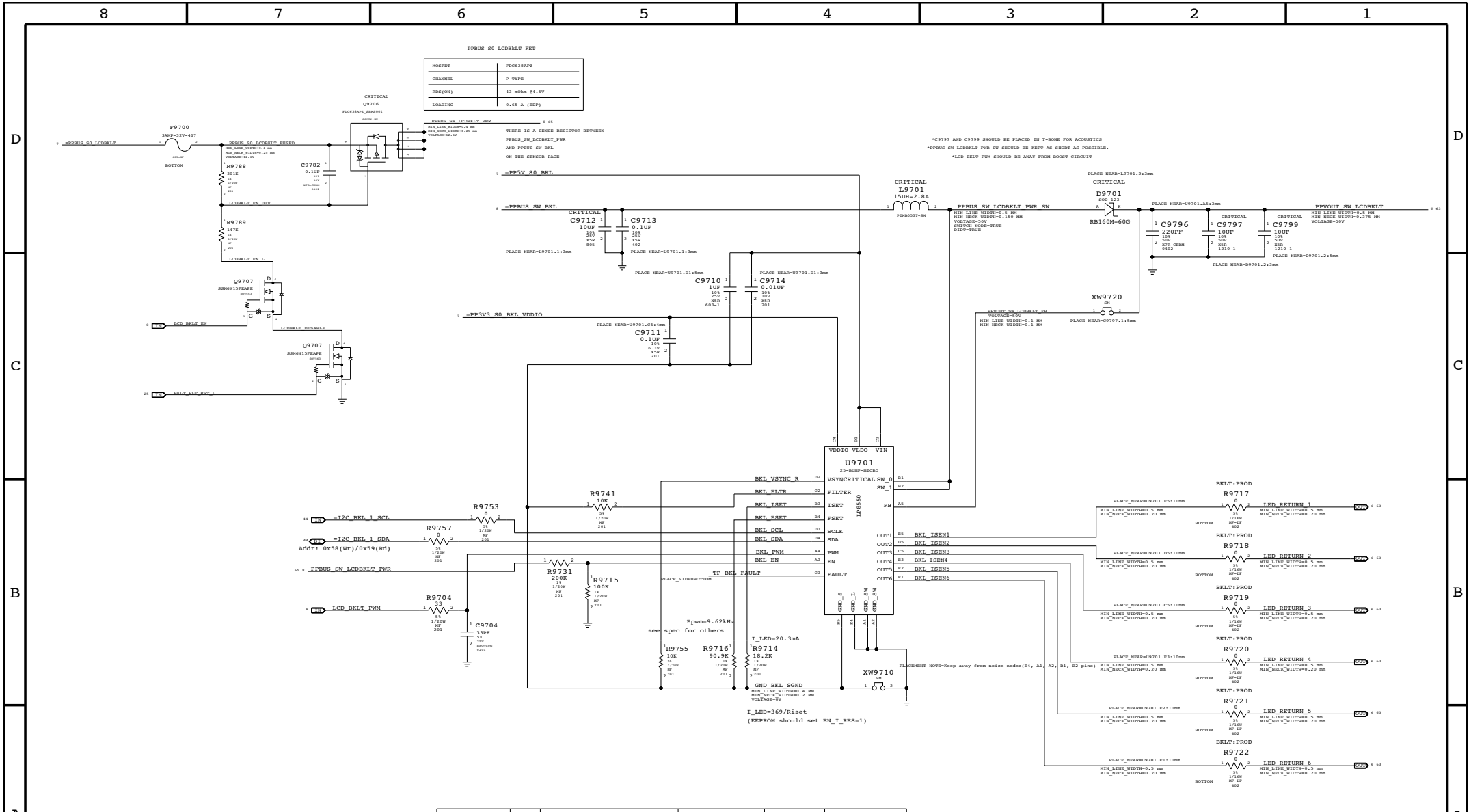

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FILM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=K21_MLB SYNC DATE=07/28/2011

PAGE TITLE: LCD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH:

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SHEET: 65 OF 73

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 103

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_45S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	10 19 42
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_45S	CPU_ITP	XDP_DBRESET_L	10 23 25
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_45S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	10 41
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	10 41 42 57
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	10 19 42
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	9 10
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	9 10
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	23
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L_R_CFG	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	23
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	12 57
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	12 57
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 59
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 59
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 57
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 57
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	12 57
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	12 57
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	12 57
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>	8 38
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>	8 38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P	38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N	38
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>	8 38
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>	8 38
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P	38
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N	38
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>	6 38
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>	6 38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>	6 38
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>	6 38
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>	6 8 38
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>	6 8 38
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>	
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	6 16 38
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	6 16 38
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	9 63
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	9 63
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>	6 63
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>	6 63
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	6 63
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	6 63
	DP_80D	DP_AUX	DP_INT_AUX_CH_P	9 63
	DP_80D	DP_AUX	DP_INT_AUX_CH_N	9 63

DMI/FDI

PCIe SSD

DP

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PAGE TITLE: CPU Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

PalPilot Spacing	"Real" Spacing
=2x_DIELECTRIC	=2x_DIELECTRIC
=5.7x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=4x_DIELECTRIC	=3x_DIELECTRIC
=8.6x_DIELECTRIC	=6x_DIELECTRIC
=5.7x_DIELECTRIC	=4x_DIELECTRIC
=PWR_P2MM	=PWR_P2MM
=GND_P2MM	=GND_P2MM
=8.6x_DIELECTRIC	=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	27 28 31

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Memory Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 38
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 38
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	38
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	38
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 38
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 38
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 38
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	38
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	38
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 38
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 38
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24
USB_BT	USB_80D	USB	USB_BT_P	24 37
USB_BT	USB_80D	USB	USB_BT_N	24 37
	USB_80D	USB	USB_BT_CONN_P	6 37
	USB_80D	USB	USB_BT_CONN_N	6 37
	USB_80D	USB	USB_BT_WAKE_P	37
	USB_80D	USB	USB_BT_WAKE_N	37
USB_TPAD	USB_80D	USB	USB_TPAD_P	49
USB_TPAD	USB_80D	USB	USB_TPAD_N	49
	USB_80D	USB	USB_TPAD_CONN_P	6
	USB_80D	USB	USB_TPAD_CONN_N	6
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	24
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	24
	USB_80D	USB	USB_TPAD_R_P	24 49
	USB_80D	USB	USB_TPAD_R_N	24 49
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	49
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	49
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	24 33
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	24 33
USB_SMC	USB_80D	USB	USB_SMC_P	24 41
USB_SMC	USB_80D	USB	USB_SMC_N	24 41
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 40
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 40
USB_EXTA	USB_80D	USB	USB_EXTA_P	18 39
USB_EXTA	USB_80D	USB	USB_EXTA_N	18 39
	UART_45S	UART	SMC_DEBUGPRT_TX_L	39 41 42
	UART_45S	UART	SMC_DEBUGPRT_RX_L	39 41 42
	USB_80D	USB	USB2_EXTA_MUXED_P	39
	USB_80D	USB	USB2_EXTA_MUXED_N	39
	USB_80D	USB	USB2_EXTA_MUXED_F_P	39
	USB_80D	USB	USB2_EXTA_MUXED_F_N	39
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_P	18 39
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_N	18 39
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_P	18 39
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_N	18 39
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_P	39
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_N	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_P	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_N	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_P	39
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_N	39
USB_EXTB	USB_80D	USB	USB_EXTB_P	6 24 40
USB_EXTB	USB_80D	USB	USB_EXTB_N	6 24 40
	USB_80D	USB	USB_EXTB_EHCI_P	18 24
	USB_80D	USB	USB_EXTB_EHCI_N	18 24
	USB_80D	USB	USB_EXTB_XHCI_P	18 24
	USB_80D	USB	USB_EXTB_XHCI_N	18 24
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	18 40
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	18 40
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	6 40
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	6 40
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	18 40
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	18 40
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	6 40
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	6 40
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	16
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	16
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16

SATA SSD

USB Hub nets

USB Camera nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

Unused USB nets

SYNC MASTER=J13_CONSTRAINTS SYNC DATE=01/11/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L
	LPC_45S	LPC	LPCPLUS_RESET_L
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN
	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK
	HDA_45S	HDA	HDA_BIT_CLK_R
HDA_SYNC	HDA_45S	HDA	HDA_SYNC
	HDA_45S	HDA	HDA_SYNC_R
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L
	HDA_45S	HDA	HDA_RST_L
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT
	HDA_45S	HDA	HDA_SDOUT_R
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K
SPI_CLK	SPI_45S	SPI	SPI_CLK_R
	SPI_45S	SPI	SPI_CLK
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R
	SPI_45S	SPI	SPI_MOSI
SPI_MISO	SPI_45S	SPI	SPI_MISO
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L
	SPI_45S	SPI	SPI_CS0_L
	SPI_45S	SPI	SPI_SMC_CLK
	SPI_45S	SPI	SPI_SMC_MOSI
	SPI_45S	SPI	SPI_SMC_MISO
	SPI_45S	SPI	SPI_SMC_CS_L
	SPI_45S	SPI	SPI_MLB_CLK
	SPI_45S	SPI	SPI_MLB_MOSI
	SPI_45S	SPI	SPI_MLB_MISO
	SPI_45S	SPI	SPI_MLB_CS_L
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R

SYNC MASTER=J13 CONSTRAINTS SYNC DATE=01/11/2012

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Apple Inc.

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0> 34 44
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0> 34 44
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0> 44
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0> 44
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1> 34 44
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1> 34 44
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3> 34 44
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3> 34 44
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2> 44
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2> 44
	DP_80D	DP_TX	DP_A_LSX_ML_P<1> 44
	DP_80D	DP_TX	DP_A_LSX_ML_N<1> 44
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0> 44
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0> 44
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1> 34 44
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1> 34 44
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0> 34 44
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0> 34 44
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P 34 44
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N 34 44
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P 44
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N 44
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P 44
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N 44
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P 44
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N 44
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0> 8 34
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0> 8 34
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2> 8 34
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2> 8 34
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0> 8 34
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0> 8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P 8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N 8 34
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 34
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 34
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 34
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 34

Only used on hosts supporting Thunderbolt video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	41 44
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	41 44
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	41 44
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	41 44
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	53
	1:1_DIFFPAIR		CHGR_CSI_R_P	53
	1:1_DIFFPAIR		CHGR_CSI_R_N	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	53
	1:1_DIFFPAIR		CHGR_CSO_R_P	53
	1:1_DIFFPAIR		CHGR_CSO_R_N	53

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_N
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_N
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_P
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_N
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_P
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_N
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_P
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_N
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_P
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_N
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_P
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N
		SB_POWER	PP3V3_S5
		SB_POWER	PP3V3_S0
		GND	GND

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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