

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

OROYA

03/20/2007 - DVT

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
?		?	?		
				DATE	DATE
				?	?

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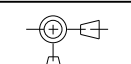
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ALIASES RESOLVED

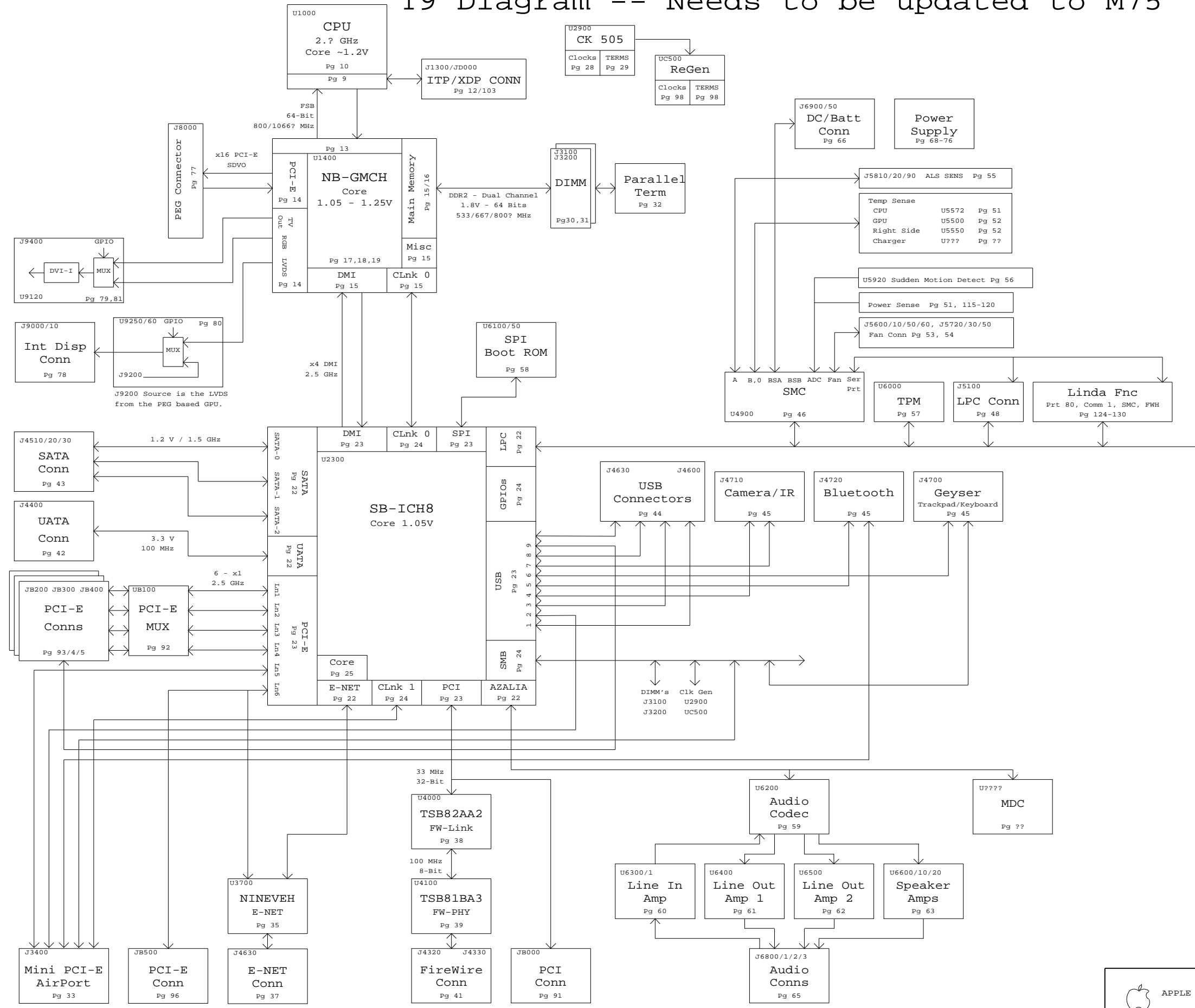
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7225	1	SCHEM, MLB, M75	SCH	CRITICAL	
820-2101	1	PCBF, MLB, M75	PCB	CRITICAL	

DRAWING TITLE=MLB ABBREV=DRAWING LAST_MODIFIED=Tue Mar 20 20:28:27 2007

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X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
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 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	
				DRAWING NUMBER 051-7225 REV. 14.0.0	
				SHT 1 OF 88	

T9 Diagram -- Needs to be updated to M75



System Block Diagram
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Power Block Diagram		
SYNC_MASTER=(T9_MLB)		SYNC_DATE=08/23/2006
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	<small>SCALE</small> NONE	<small>SHT</small> 3
		<small>OF</small> 88

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Power Block Diagram		
SYNC_MASTER=N/A		SYNC_DATE=N/A
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	D	14.0.0
SCALE	SHT	OF
NONE	4	88

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7931	PCBA,OROYA1,M75	M75_COMMON,EEE_X5D,CPU_2_2GHZ,FB_128_SAMSUNG
630-7932	PCBA,OROYA2,M75	M75_COMMON,EEE_X5E,CPU_2_4GHZ,FB_256_SAMSUNG
630-8659	PCBA,OROYA1,VRAM-HY,M75	M75_COMMON,EEE_XXS,CPU_2_2GHZ,FB_128_HYNIX
630-8662	PCBA,OROYA2,VRAM-HY,M75	M75_COMMON,EEE_XXT,CPU_2_4GHZ,FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE,COMMON,M75_COMMON1,M75_COMMON2,M75_DEBUG,M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_HW,GPU_TMP401,ISL9504B,LVDS_SEL_RESUME,ONEWIRE_PU
M75_COMMON2	P1V8S3_1V825,SLG2AP101,SMS_MOT_DIS,YUKON_ULTRA,VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS
M75_PROGPARTS	BOOTROM_PROG,SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128,VRAM_SAMSUNG,VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128,VRAM_HYNIX,VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256,VRAM_SAMSUNG,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256,VRAM_HYNIX,VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5D]	CRITICAL	EEE_X5D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:X5E]	CRITICAL	EEE_X5E
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXS]	CRITICAL	EEE_XXS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3457	1	IC,MEC,SR,E1,QS,2.2G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3458	1	IC,MEC,SR,E1,QS,2.4G,35W,800FSB,4M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0388	1	IC,GPU,NV G84M,BGA	U8000	CRITICAL	
338S0426	1	IC,NB,CRESTLINE,GM,C0,QS,965PM	U1400	CRITICAL	
338S0427	1	IC,SB,ICH8M,B1,QS,BGA	U2300	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,2PHAS,QFN48,LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC,ISL9504B,2PH IMVP6 REG,PMON,QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC,68 PIN,CK505,LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC,SLG2AP101,LM PWR CLCK GEN,CK505,QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC,88E8058,GIGABIT ENET XCVR,64P QFN	U3700	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2004	1	IC,SMC,DEVELOPMENT,M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC,EFI ROM,DEVELOPMENT,M75	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	IC,SGRAM,GDDR3,8Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC,SGRAM,GDDR3,16Mx32,700MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	See alt to TOK/BI-Tech magnetica
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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	SCALE NONE	SHIT 5 OF 88	

PROTO

See Perforce change notes for updates before Proto Release
12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0:
01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0:
01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0:
01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0:
01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0:
01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMPTIONS and values for ISL9504B
01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0:
01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path
9.4.0:
01/19/07 -- GPU GPIOs: Added 2 TPs on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787)
9.5.0:
01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMPTIONS for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3_1V825 BOMPTION to lift voltage at FB memories
10.0.0:
01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMPTIONS to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

EVT_SE

10.1.0:
01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0
01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings
01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes
10.2.0:
01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST
01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes
11.0.0:
01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K)
01/25/07 -- BOM: Updated all Intel APNs to use QS parts
01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03)
12.0.0:
02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup
02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup
02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain
02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain
02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

DVT

12.1.0:
02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)
02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)
02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)
02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates
02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)
12.2.0:
02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)
02/28/07 -- Power Aliases: Moving P1V8_GPU FET source to P1V8_S3 rather than P1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462)
12.3.0:
02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines
12.4.0:
03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)
03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
12.5.0:
03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements
12.6.0:
03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)
03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height
12.7.0:
03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request
03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)
03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)

D

D

C

C

B

B

A

A

Revision History table with columns for SYNC_MASTER, SYNC_DATE, and NOTICE OF PROPRIETARY PROPERTY.

Apple Computer Inc. table with columns for SCALE, DRAWING NUMBER, and REV.

Functional Test Points

ICT Test Points

Fan Connectors

FUNC_TEST	Pin
TRUE PP5V_S0	7 8 27 42 47 52 57
TRUE FAN_LT_PWM	52
TRUE FAN_LT_TACH	52
TRUE FAN_RT_PWM	52
TRUE FAN_RT_TACH	52

Battery Digital Connector

FUNC_TEST	Pin
TRUE SMC_BS_ALERT_L	45 46 56
TRUE SMBUS_SMC_BSA_SCL	45 48 56 84
TRUE SMBUS_SMC_BSA_SDA	45 48 56 84
TRUE GND_BATT	56

CPU FSB NO_TESTS

NO_TEST	Pin
TRUE FSB_A_L<31..3>	10 14 79
TRUE FSB_ADS_L	10 14 79
TRUE FSB_ADSTB_L<1..0>	10 14 79
TRUE FSB_BNR_L	10 14 79
TRUE FSB_BREQ0_L	10 14 79
TRUE FSB_D_L<63..0>	10 14 79
TRUE FSB_DBSY_L	10 14 79
TRUE FSB_DINV_L<3..0>	10 14 79
TRUE FSB_DRDY_L	10 14 79
TRUE FSB_DSTB_L_N<3..0>	10 14 79
TRUE FSB_DSTB_L_P<3..0>	10 14 79
TRUE FSB_HIT_L	10 14 79
TRUE FSB_HITM_L	10 14 79
TRUE FSB_LOCK_L	10 14 79
TRUE FSB_REQ_L<4..0>	10 14 79

NB NO_TESTS

NO_TEST	Pin
TRUE NC_NB_NC<1..16>	== TP_NB_NC<1..16> 16

LPC+ Debug Connector

FUNC_TEST	Pin
TRUE PP3V42_G3H	8 28 35 43 45 46 47
TRUE PP5V_S0	7 8 27 42 47 52 57 58
TRUE LPC_AD<0>	23 45 47
TRUE LPC_AD<1>	23 45 47
TRUE LPC_FRAME_L	23 45 47
TRUE PM_CLKRUN_L	25 45 47
TRUE PCI_FW_GNT_L	24 38 47 83
TRUE SMC_TMS	45 46 47
TRUE DEBUG_RESET_L	28 47
TRUE SMC_TRST_L	45 47
TRUE SMC_TDO	45 46 47
TRUE SMC_MD1	45 47
TRUE SMC_TX_L	43 45 46 47
TRUE FWH_INIT_L	47
TRUE PCI_CLK33M_LPCPLUS	30 47 84
TRUE LPC_AD<2>	23 45 47
TRUE LPC_AD<3>	23 45 47
TRUE INT_SERRIO	25 45 47
TRUE PM_SUS_STAT_L	25 45 46 47
TRUE SMC_TDI	45 46 47
TRUE SMC_TCK	45 46 47
TRUE SMC_RESET_L	45 46 47
TRUE SMC_NMI	45 47
TRUE SMC_RX_L	43 45 46 47
TRUE LINDACARD_GPIO	25 47

Left I/O Power Connector

FUNC_TEST	Pin
TRUE PPBUS_G3H	8 40 49 56 57 58 59 60 61 62 63
TRUE GND	

Request for at least 10 GND test points
NOTE: 10 additional GND test points are called out separately in these notes.

RTC Battery Connector

FUNC_TEST	Pin
TRUE PPVBATT_G3_RTC	28
TRUE GND	

Current Sense Calibration

FUNC_TEST	Pin
TRUE ISENSE_CAL_EN	45 49
TRUE PP5V_S3	7 8 44 46 49 53 57 78
TRUE PPVCORE_S0_NB_GFX	8 18 32 49
TRUE PPVCORE_S0_CPU	8 11 12 49
TRUE PPVCORE_GPU	8 49 67 74
TRUE GND	

6 TPs, 2 with each of above TP pairs

Left Clutch Barrel Connector

FUNC_TEST	Pin
TRUE PP5V_S3	7 8 44 46 49 53 57 78
TRUE USB_CAMERA_N	24 44 82
TRUE USB_CAMERA_P	24 44 82
TRUE PP5V_S3	7 8 44 46 49 53 57 78
TRUE USB_WWAN_N	24 44 82
TRUE USB_WWAN_P	24 44 82

Other Func Test Points

FUNC_TEST	Pin
TRUE PM_SYSRST_L	25 28 45
TRUE SMC_ONOFF_L	45 46 78

Left ALS Connector

FUNC_TEST	Pin
TRUE PP3V3_S3	8 36 38 48 50 51 53
TRUE ALS_GAIN	45 53 78
TRUE LTALS_OUT	53 78
TRUE GND	

Thermal Diode Connectors

FUNC_TEST	Pin
TRUE HSTHMSNS_D_P	51 87
TRUE HSTHMSNS_D_N	51
TRUE RSFTHMSNS_D_P	51 87
TRUE RSFTHMSNS_D_N	51
TRUE CPUTHMSNS_D2_P	51 87
TRUE CPUTHMSNS_D2_N	51

CPUTHMSNS can not be supported due to layout constraints

System Validation TPs

FUNC_TEST	Pin
TRUE CPU_PWRGD	10 13 23 79
TRUE CPU_DPSLP_L	7 10 23 79
TRUE PM DPRSLPVR	16 25 58 79
TRUE CPU_DPSLP_L	7 10 23 79
TRUE PM_LAN_ENABLE	25 45
TRUE PCI_RST_L	24 28
TRUE PM_RSMRST_L	25 45
TRUE PM_SB_PWR0K	9 25 28
TRUE SB_RTC_RST_L	23 28
TRUE PM_STPCPU_L	25 29 30
TRUE PM_STPPCI_L	25 29 30
TRUE VR_PWRGD_CLKEN	25 28
TRUE VR_PWRGD_DELAY	9 16 28 58
TRUE FSB_CPURST_L	10 13 14 79
TRUE FSB_CPUSLP_L	10 14 79
TRUE FSB_DPWR_L	10 14 79
TRUE NB_SB_SYNC_L	16 25

FUNC_TEST	Pin
TRUE IMVP_VR_ON	45 58
TRUE IMVP DPRSLPVR	58 79
TRUE PM_SLP_S3_L	25 35 36 40 45 49 57 62 65
TRUE PM_S4_STATE_L	25 34 43 45 57 65
TRUE PM_SLP_S5_L	25 45 46
TRUE PM_ENET_EN	36 61 65
TRUE P1V5P1V05S0_PGOOD	61 63 65
TRUE CPU DPRSTP_L	10 16 23 58 79
TRUE IMVP6_VID<6..0>	12 58 79
TRUE PLT_RST_L	24 28 77
TRUE NB_RESET_L	16 28
TRUE GPU_RESET_L	28 66
TRUE SMC_LRESET_L	28 45
TRUE CPU_STPCLK_L	10 23 79
TRUE FSB_CLK_NB_P	14 29 30 84
TRUE FSB_CLK_NB_N	14 29 30 84
TRUE NB_CLKREQ0_L	16 29
TRUE NB_CLK100M_PCIE_P	16 29 30 84
TRUE NB_CLK100M_PCIE_N	16 29 30 84
TRUE NB_CLK96M_DOT_P	84
TRUE NB_CLK96M_DOT_N	84
TRUE NB_CLK100M_DPLLSS_P	16 22 29 30 84
TRUE NB_CLK100M_DPLLSS_N	16 22 29 30 84
TRUE CPU_THERMTRIP_R	33

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

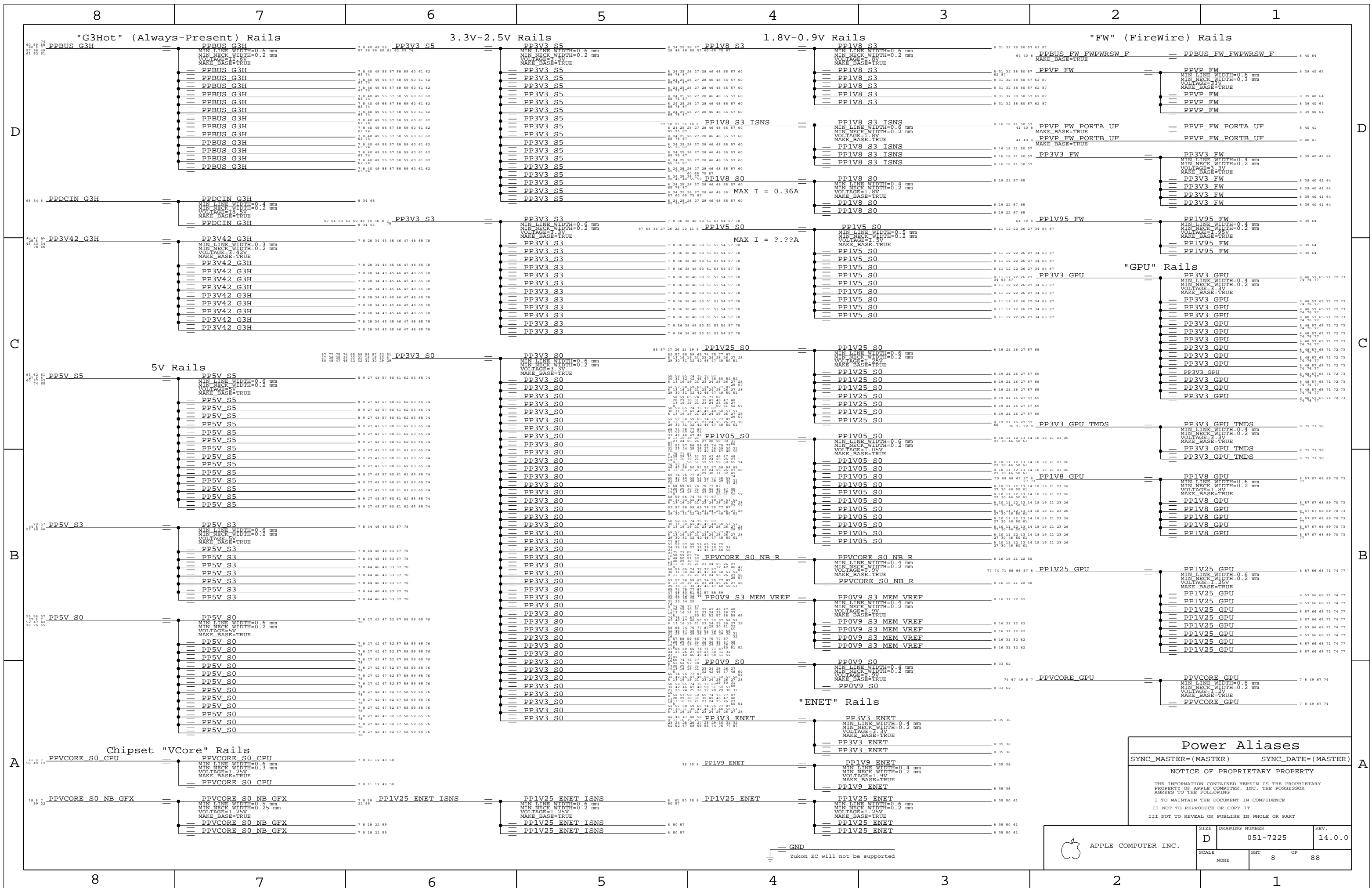
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NONE	7	88



Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

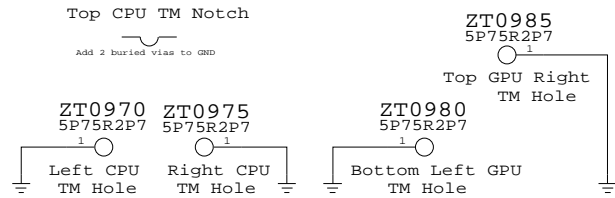
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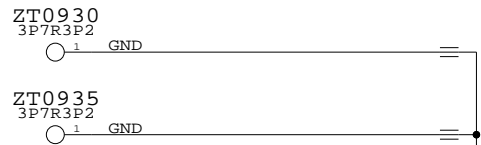
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NONE	8	88	

GND
 Yukon EC will not be supported

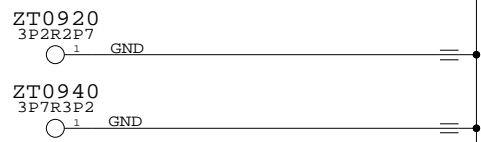
Thermal Module Holes



RAM Door (Torx) Holes

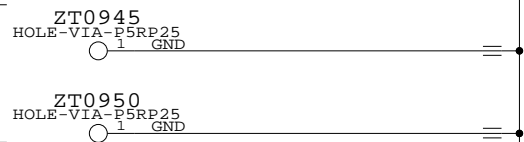


Frame Holes



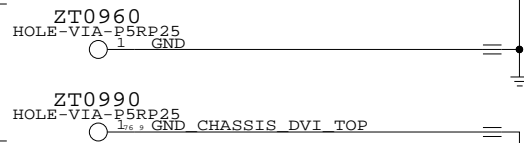
Board Edge Notches

(Can't be PTH)

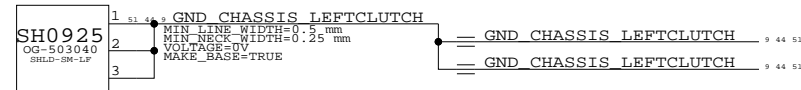
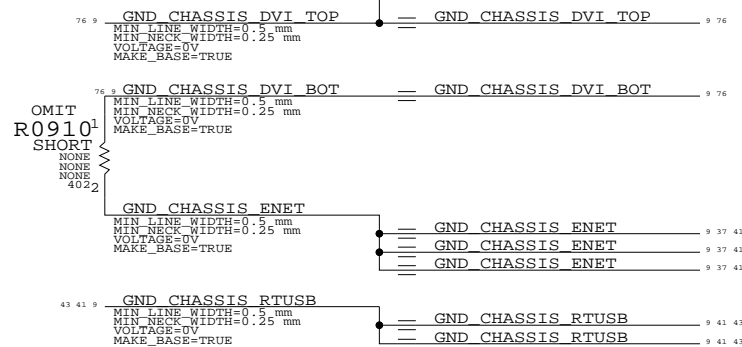


Tooling Holes

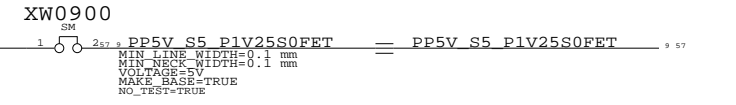
(Can't be PTH)



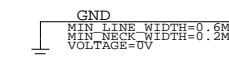
Chassis GNDs



28 25 9 7	PM_SB_PWROK MAKE_BASE=TRUE	==	PM_SB_PWROK	7 9 25 28
58 28 16 9 7	VR_PWRGOOD_DELAY MAKE_BASE=TRUE	==	VR_PWRGOOD_DELAY	7 9 16 28 58
54 45 9	SMC_SMS_INT MAKE_BASE=TRUE	==	SMC_SMS_INT	9 45 54
84 66 30 29 9	PEG_CLK100M_GPU_P MAKE_BASE=TRUE	==	PEG_CLK100M_GPU_P	9 29 30 66 84
84 66 30 29 9	PEG_CLK100M_GPU_N MAKE_BASE=TRUE	==	PEG_CLK100M_GPU_N	9 29 30 66 84
77 59 9	PM_ALL_NBGFX_PGOOD MAKE_BASE=TRUE	==	PM_ALL_NBGFX_PGOOD	9 59 77
59 16 9	GFX_VR_EN MAKE_BASE=TRUE	==	GFX_VR_EN	9 16 59
59	GFXIMVP6_VID<4..0> MAKE_BASE=TRUE	==	GFX_VID<4..0>	16
31 9	TP_MEM_A_A<15> MAKE_BASE=TRUE	==	TP_MEM_A_A<15>	9 31
32 9	TP_MEM_B_A<15> MAKE_BASE=TRUE	==	TP_MEM_B_A<15>	9 32
82 24 9	TP_USB_EXTCP MAKE_BASE=TRUE	==	TP_USB_EXTCP	9 24 82
82 24 9	TP_USB_EXTCN MAKE_BASE=TRUE	==	TP_USB_EXTCN	9 24 82



Digital Ground



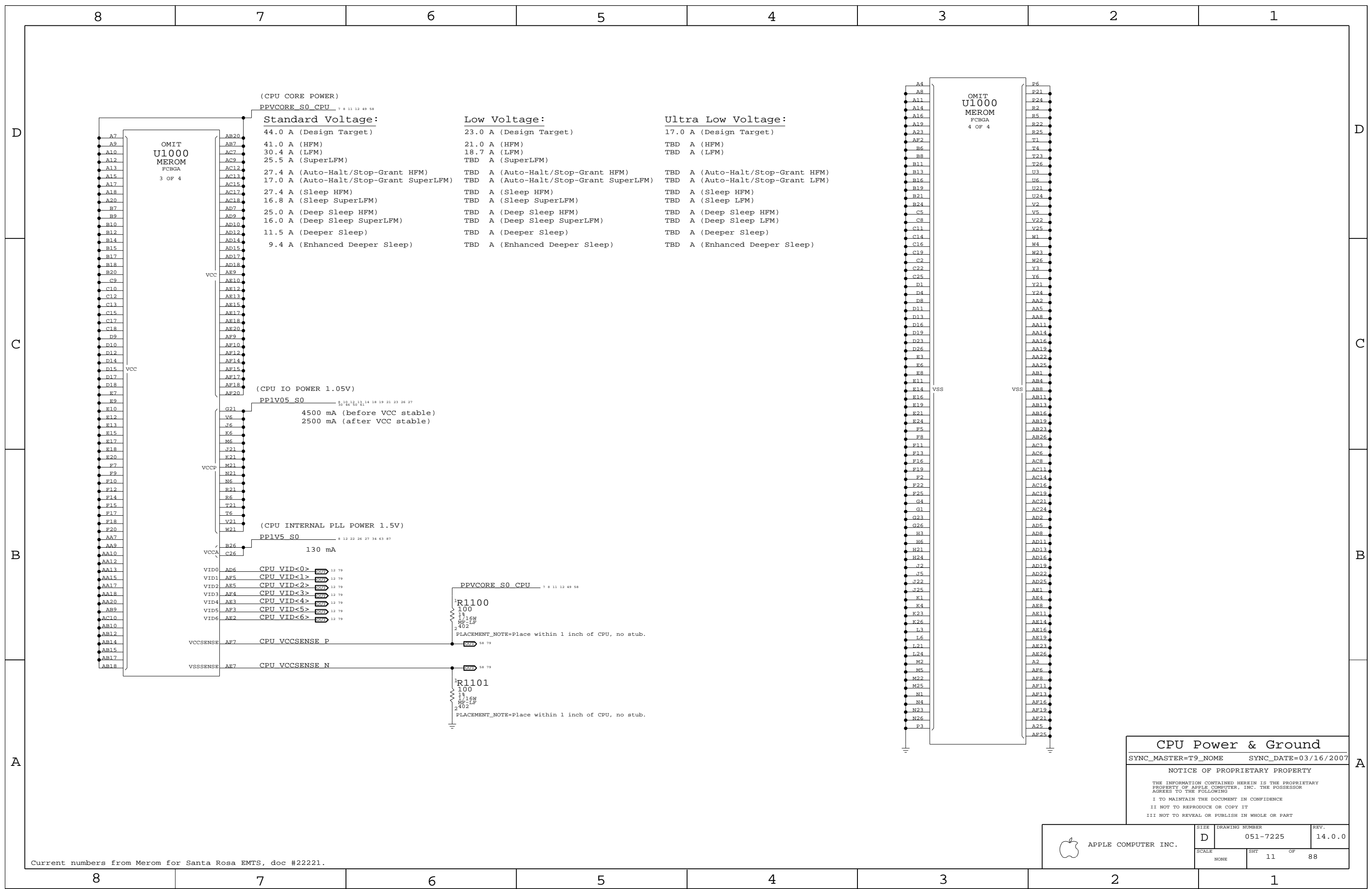
Signal Aliases

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/23/2006

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NONE	9	88	



(CPU CORE POWER)
PPV CORE S0 CPU 7 8 11 12 49 58

Standard Voltage:
44.0 A (Design Target)
41.0 A (HFM)
30.4 A (LFM)
25.5 A (SuperLFM)
27.4 A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)
27.4 A (Sleep HFM)
16.8 A (Sleep SuperLFM)
25.0 A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)
11.5 A (Deeper Sleep)
9.4 A (Enhanced Deeper Sleep)

Low Voltage:
23.0 A (Design Target)
21.0 A (HFM)
18.7 A (LFM)
TBD A (SuperLFM)
TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)
TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)
TBD A (Deep Sleep HFM)
TBD A (Deep Sleep SuperLFM)
TBD A (Deeper Sleep)
TBD A (Enhanced Deeper Sleep)

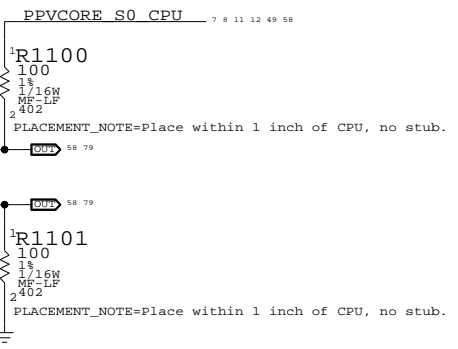
Ultra Low Voltage:
17.0 A (Design Target)
TBD A (HFM)
TBD A (LFM)
TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant LFM)
TBD A (Sleep HFM)
TBD A (Sleep LFM)
TBD A (Deep Sleep HFM)
TBD A (Deep Sleep LFM)
TBD A (Deeper Sleep)
TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)
PPV I05 S0 50 106 150 151 14 18 19 21 23 26 27
4500 mA (before VCC stable)
2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)
PPV I5 S0 8 12 22 26 27 34 63 87
130 mA

VID0 AD6 CPU VID<0>
VID1 AE5 CPU VID<1>
VID2 AE5 CPU VID<2>
VID3 AF4 CPU VID<3>
VID4 AE3 CPU VID<4>
VID5 AF3 CPU VID<5>
VID6 AE2 CPU VID<6>

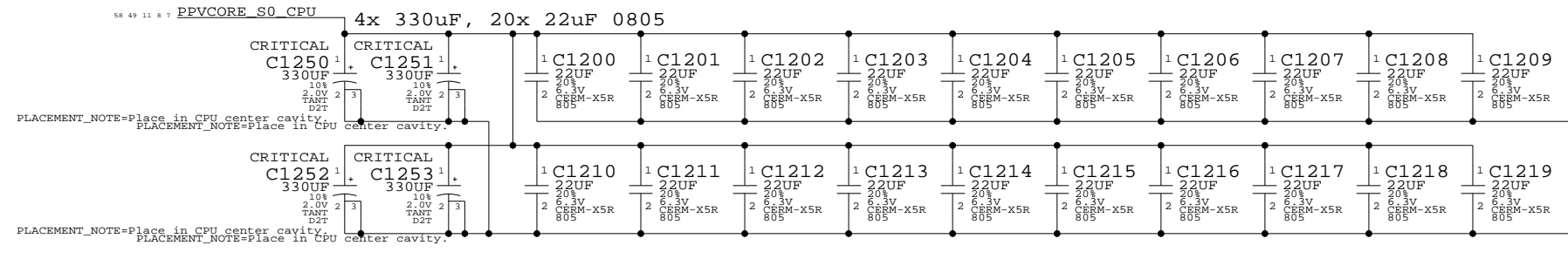
VCCSENSE AF7 CPU VCCSENSE P
VSSSENSE AE7 CPU VCCSENSE N



CPU Power & Ground
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007
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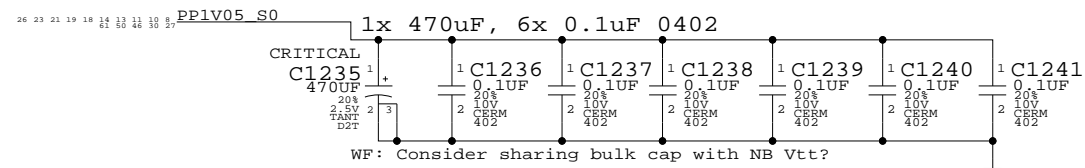
CPU VCORE HF AND BULK DECOUPLING



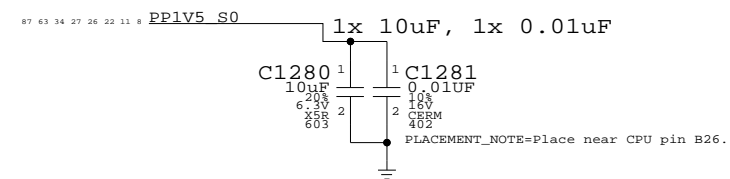
CPU VCORE VID CONNECTIONS

79 11 CPU VID<0..6> == IMVP6 VID<0..6> 7 58 79
MAKE_BASE=TRUE

VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

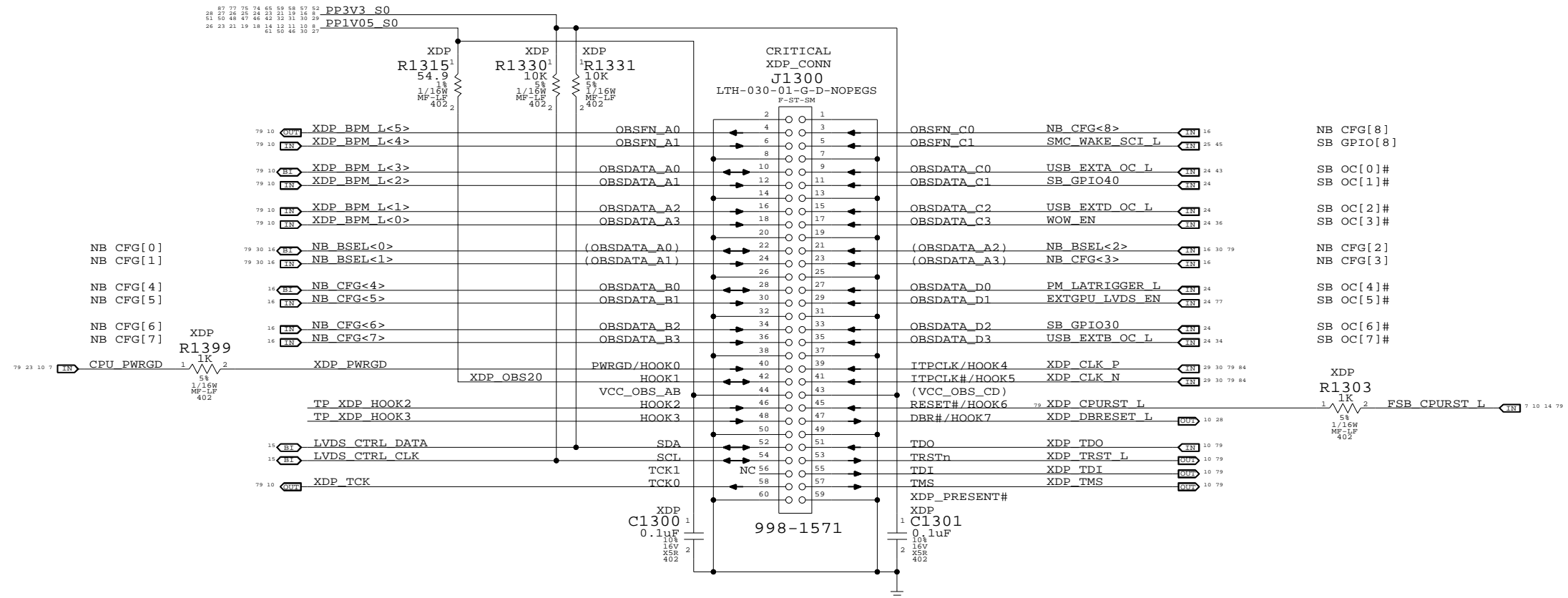
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NONE	12	18	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0451 adapter board to support CPU, NB & SB debugging.

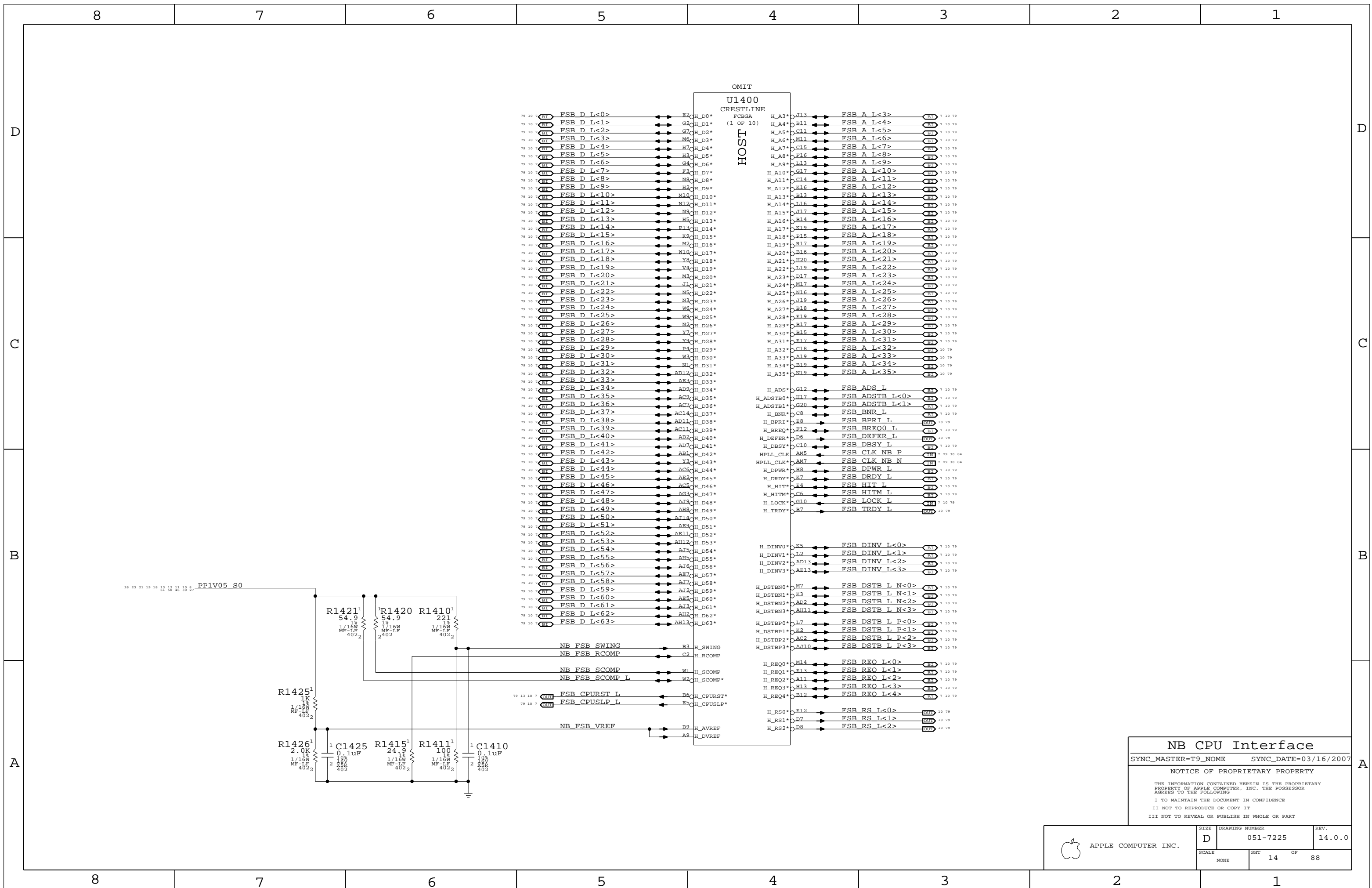


← Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300

eXtended Debug Port (XDP)
SYNC_MASTER=T9_NOME SYNC_DATE=12/12/2006

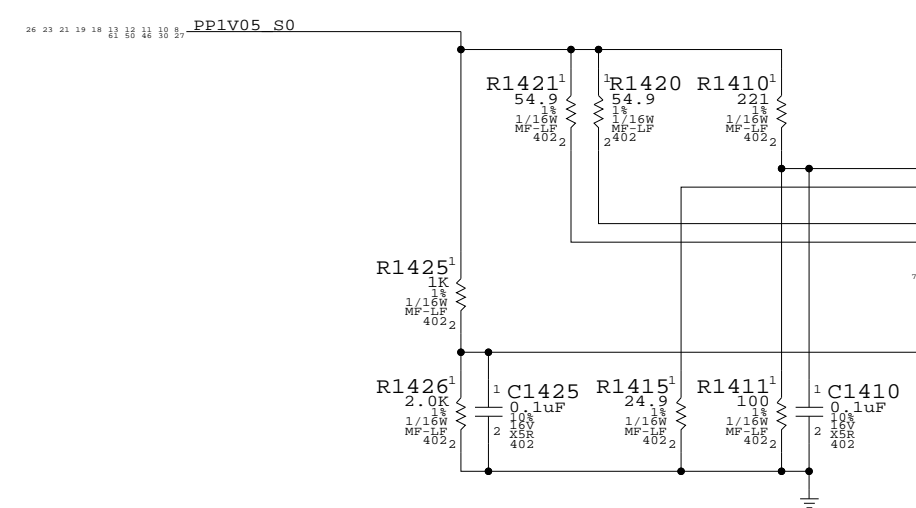
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NONE	13	88	



OMIT
U1400
CRESTLINE
FCBGA
(1 OF 10)

Host Pin	Host Label	Processor Pin	Processor Label
H_A3*	J13	E2	FSB D L<0>
H_A4*	B11	G2	FSB D L<1>
H_A5*	C11	G7	FSB D L<2>
H_A6*	M11	M6	FSB D L<3>
H_A7*	C15	H7	FSB D L<4>
H_A8*	F16	H3	FSB D L<5>
H_A9*	L13	G4	FSB D L<6>
H_A10*	G17	F3	FSB D L<7>
H_A11*	C14	N8	FSB D L<8>
H_A12*	K16	H8	FSB D L<9>
H_A13*	B13	M10	FSB D L<10>
H_A14*	L16	N12	FSB D L<11>
H_A15*	J17	N9	FSB D L<12>
H_A16*	B14	H5	FSB D L<13>
H_A17*	K19	P13	FSB D L<14>
H_A18*	P15	K9	FSB D L<15>
H_A19*	R17	M2	FSB D L<16>
H_A20*	B16	W10	FSB D L<17>
H_A21*	H20	Y8	FSB D L<18>
H_A22*	L19	V4	FSB D L<19>
H_A23*	D17	M3	FSB D L<20>
H_A24*	M17	J1	FSB D L<21>
H_A25*	N16	N5	FSB D L<22>
H_A26*	J19	N3	FSB D L<23>
H_A27*	B18	M6	FSB D L<24>
H_A28*	E19	W9	FSB D L<25>
H_A29*	B17	N2	FSB D L<26>
H_A30*	B15	Y7	FSB D L<27>
H_A31*	E17	Y9	FSB D L<28>
H_A32*	C18	F4	FSB D L<29>
H_A33*	A19	W3	FSB D L<30>
H_A34*	B19	N1	FSB D L<31>
H_A35*	N19	AD12	FSB D L<32>
		AE3	FSB D L<33>
		AD9	FSB D L<34>
		AC9	FSB D L<35>
		AC7	FSB D L<36>
		AC14	FSB D L<37>
		AD11	FSB D L<38>
		AC11	FSB D L<39>
		AE8	FSB D L<40>
		AD7	FSB D L<41>
		AB1	FSB D L<42>
		Y3	FSB D L<43>
		AC6	FSB D L<44>
		AE2	FSB D L<45>
		AC5	FSB D L<46>
		AG3	FSB D L<47>
		AJ9	FSB D L<48>
		AH8	FSB D L<49>
		M14	FSB D L<50>
		AE8	FSB D L<51>
		AE11	FSB D L<52>
		AH12	FSB D L<53>
		AJ5	FSB D L<54>
		AH5	FSB D L<55>
		AJ6	FSB D L<56>
		AE7	FSB D L<57>
		AJ7	FSB D L<58>
		AJ2	FSB D L<59>
		AE5	FSB D L<60>
		AJ3	FSB D L<61>
		AH2	FSB D L<62>
		AH13	FSB D L<63>
		B3	NB FSB SWING
		C2	NB FSB RCOMP
		W1	NB FSB SCOMP
		W2	NB FSB SCOMP L
		B6	FSB CPURST L
		E5	FSB CPUSLP L
		B9	NB FSB VREF
		A9	H_AVREF
			H_DVREF
		H_A3*	FSB A L<3>
		H_A4*	FSB A L<4>
		H_A5*	FSB A L<5>
		H_A6*	FSB A L<6>
		H_A7*	FSB A L<7>
		H_A8*	FSB A L<8>
		H_A9*	FSB A L<9>
		H_A10*	FSB A L<10>
		H_A11*	FSB A L<11>
		H_A12*	FSB A L<12>
		H_A13*	FSB A L<13>
		H_A14*	FSB A L<14>
		H_A15*	FSB A L<15>
		H_A16*	FSB A L<16>
		H_A17*	FSB A L<17>
		H_A18*	FSB A L<18>
		H_A19*	FSB A L<19>
		H_A20*	FSB A L<20>
		H_A21*	FSB A L<21>
		H_A22*	FSB A L<22>
		H_A23*	FSB A L<23>
		H_A24*	FSB A L<24>
		H_A25*	FSB A L<25>
		H_A26*	FSB A L<26>
		H_A27*	FSB A L<27>
		H_A28*	FSB A L<28>
		H_A29*	FSB A L<29>
		H_A30*	FSB A L<30>
		H_A31*	FSB A L<31>
		H_A32*	FSB A L<32>
		H_A33*	FSB A L<33>
		H_A34*	FSB A L<34>
		H_A35*	FSB A L<35>
		H_ADS*	FSB ADS L
		H_ADSTB0*	FSB ADSTB L<0>
		H_ADSTB1*	FSB ADSTB L<1>
		H_BNR*	FSB BNR L
		H_BPRI*	FSB BPRI L
		H_BREQ*	FSB BREQ L
		H_DEFER*	FSB DEFER L
		H_DBSY*	FSB DBSY L
		HPLL_CLK*	FSB CLK NB P
		HPLL_CLK*	FSB CLK NB N
		H_DPWR*	FSB DPWR L
		H_DRDY*	FSB DRDY L
		H_HIT*	FSB HIT L
		H_HITM*	FSB HITM L
		H_LOCK*	FSB LOCK L
		H_TRDY*	FSB TRDY L
		H_DINV0*	FSB DINV L<0>
		H_DINV1*	FSB DINV L<1>
		H_DINV2*	FSB DINV L<2>
		H_DINV3*	FSB DINV L<3>
		H_DSTBN0*	FSB DSTB L N<0>
		H_DSTBN1*	FSB DSTB L N<1>
		H_DSTBN2*	FSB DSTB L N<2>
		H_DSTBN3*	FSB DSTB L N<3>
		H_DSTBP0*	FSB DSTB L P<0>
		H_DSTBP1*	FSB DSTB L P<1>
		H_DSTBP2*	FSB DSTB L P<2>
		H_DSTBP3*	FSB DSTB L P<3>
		H_REQ0*	FSB REQ L<0>
		H_REQ1*	FSB REQ L<1>
		H_REQ2*	FSB REQ L<2>
		H_REQ3*	FSB REQ L<3>
		H_REQ4*	FSB REQ L<4>
		H_RS0*	FSB RS L<0>
		H_RS1*	FSB RS L<1>
		H_RS2*	FSB RS L<2>



NB CPU Interface
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SCALE	SHT	OF	
NONE	14	88	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

Note: SR DG says to tie LVDS_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

CRT & TV-Out Disable

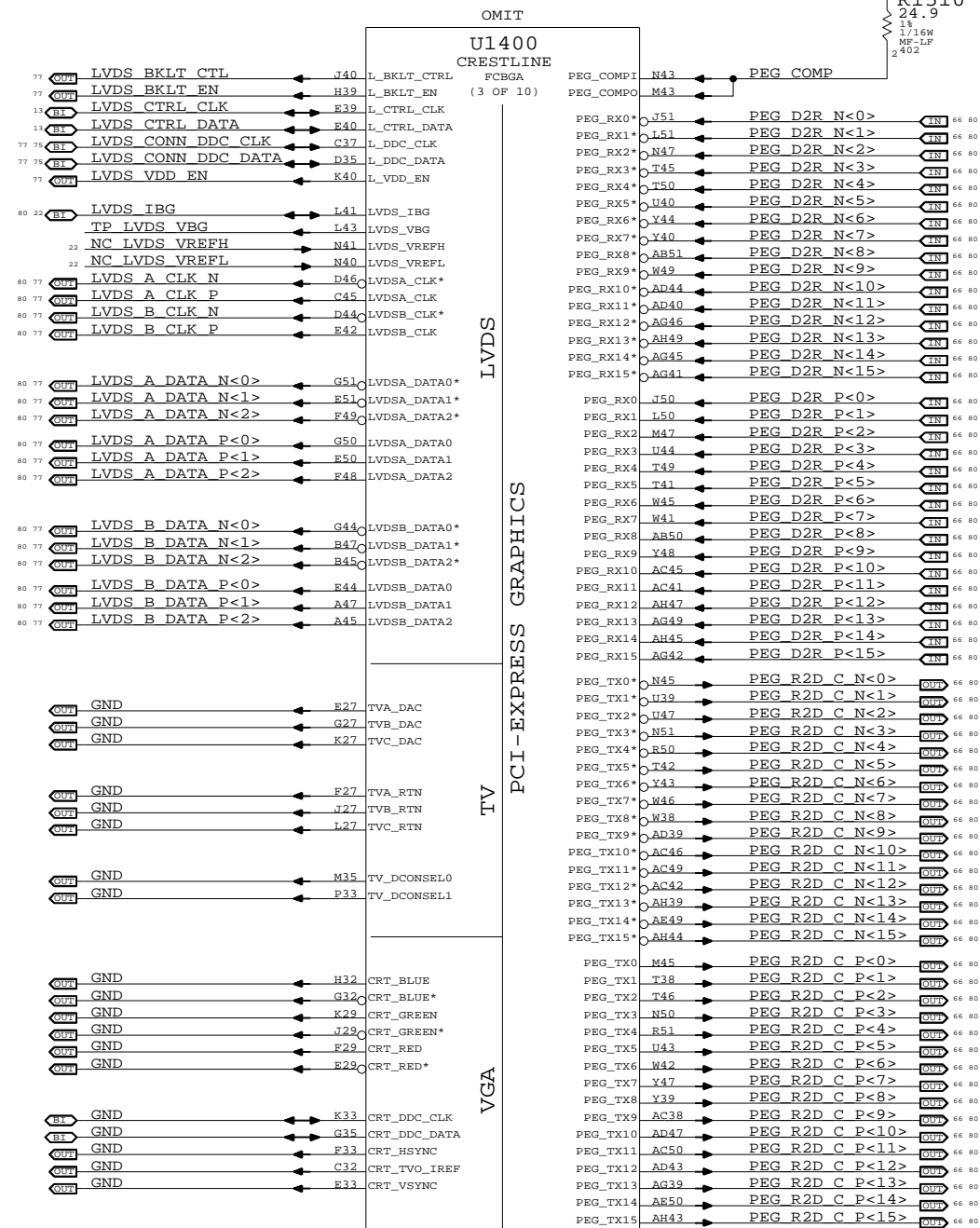
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DDC*, L_CTRL*, L_DDC*, SDVO_CTRL* and TV_DCONSELx to GND.

Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



SDVO Alternate Function

SDVO_TVCLKIN#
SDVO_INT#
SDVO_FLDSTALL#

SDVO_TVCLKIN
SDVO_INT
SDVO_FLDSTALL

SDVOB_RED#
SDVOB_GREEN#
SDVOB_BLUE#
SDVOB_CLKN
SDVOC_RED#
SDVOC_GREEN#
SDVOC_BLUE#
SDVOC_CLKN

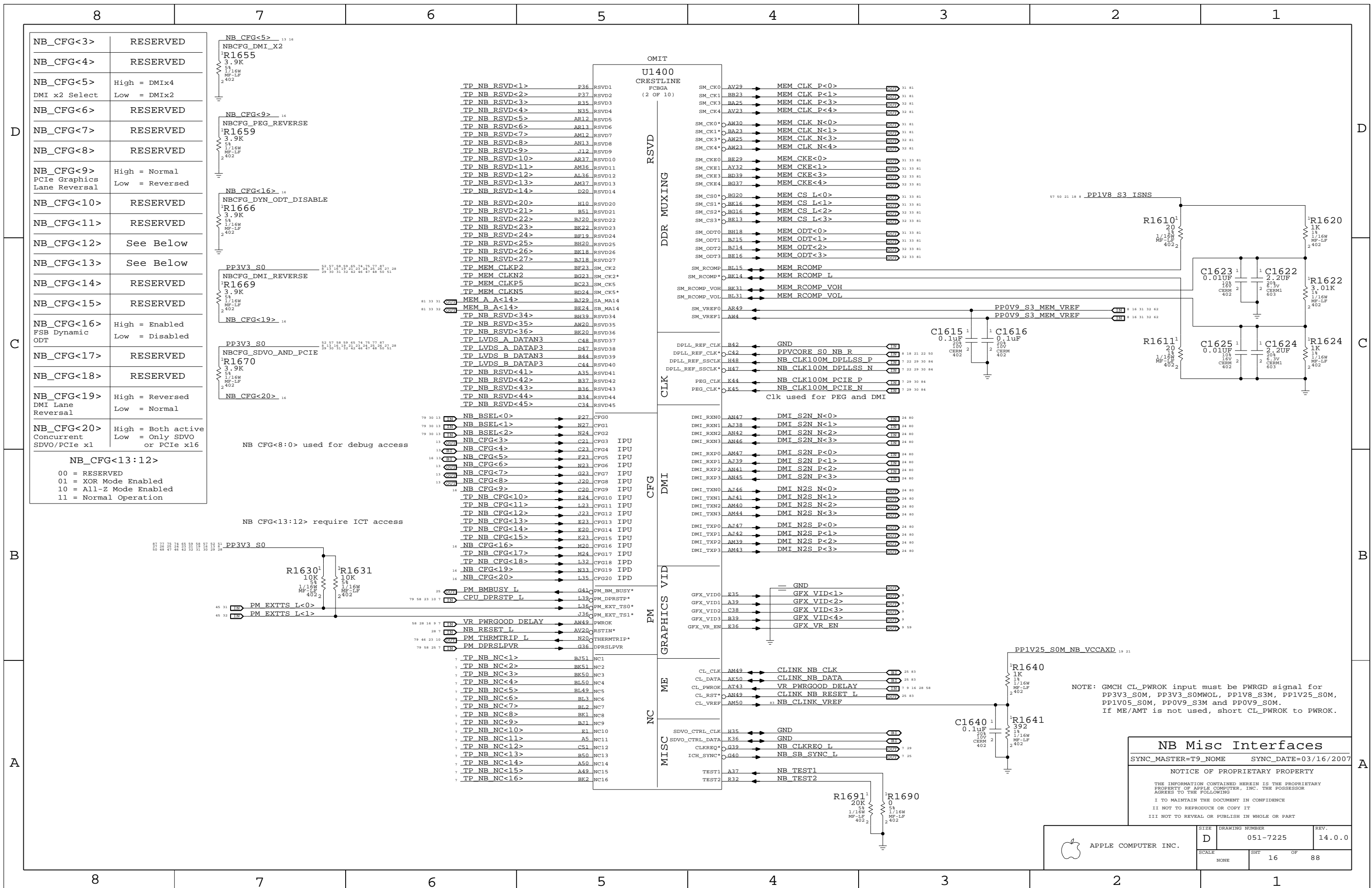
SDVOB_RED
SDVOB_GREEN
SDVOB_BLUE
SDVOB_CLKP
SDVOC_RED
SDVOC_GREEN
SDVOC_BLUE
SDVOC_CLKP

NB PEG / Video Interfaces
SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

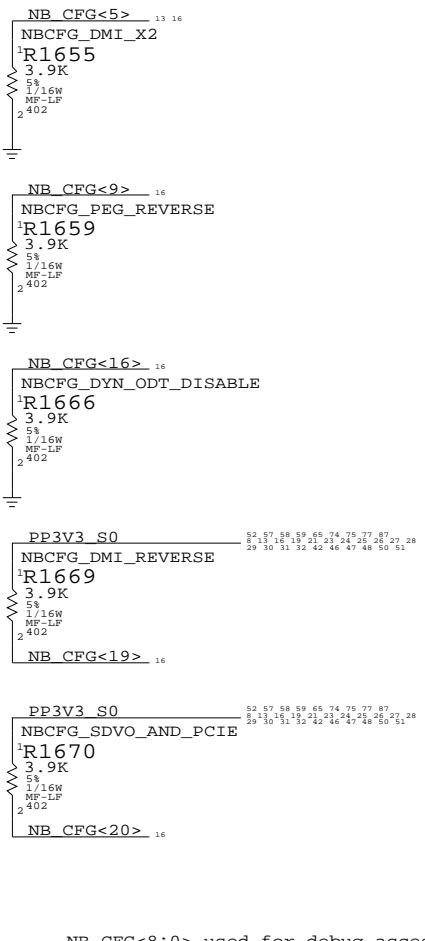
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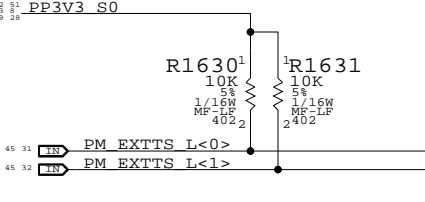


NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent Low = Only SDVO SDVO/PCIe x1 or PCIe x16



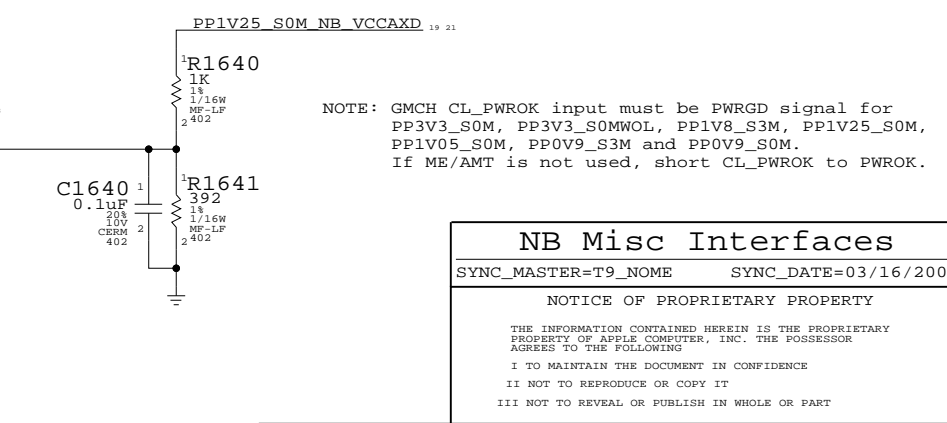
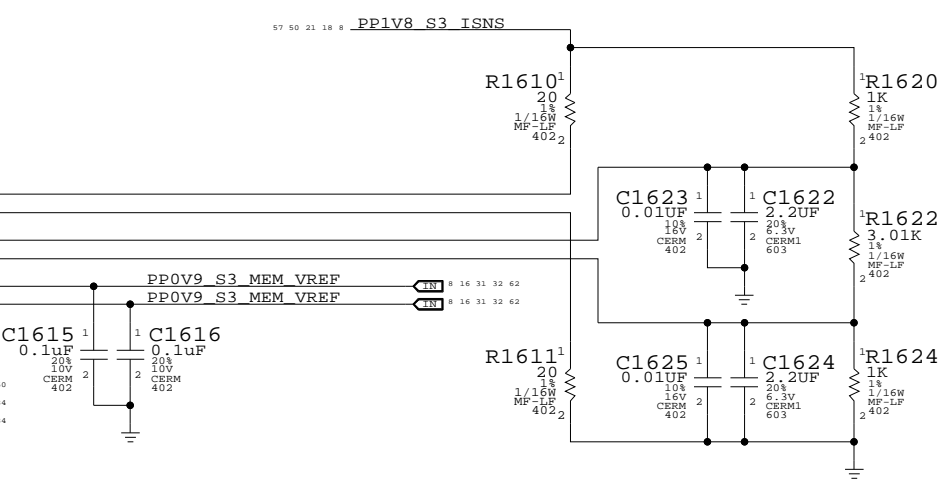
NB_CFG<8:0> used for debug access

NB_CFG<13:12> require ICT access



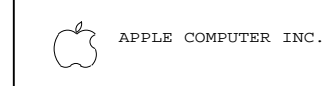
TP NB_RSVD<1>	P36	RSVD1
TP NB_RSVD<2>	P37	RSVD2
TP NB_RSVD<3>	R35	RSVD3
TP NB_RSVD<4>	N35	RSVD4
TP NB_RSVD<5>	AR12	RSVD5
TP NB_RSVD<6>	AR13	RSVD6
TP NB_RSVD<7>	AM12	RSVD7
TP NB_RSVD<8>	AM13	RSVD8
TP NB_RSVD<9>	J12	RSVD9
TP NB_RSVD<10>	AR37	RSVD10
TP NB_RSVD<11>	AM36	RSVD11
TP NB_RSVD<12>	AL36	RSVD12
TP NB_RSVD<13>	AM37	RSVD13
TP NB_RSVD<14>	D20	RSVD14
TP NB_RSVD<20>	H10	RSVD20
TP NB_RSVD<21>	B51	RSVD21
TP NB_RSVD<22>	BJ20	RSVD22
TP NB_RSVD<23>	BK22	RSVD23
TP NB_RSVD<24>	BF19	RSVD24
TP NB_RSVD<25>	BH20	RSVD25
TP NB_RSVD<26>	BK18	RSVD26
TP NB_RSVD<27>	BJ18	RSVD27
TP MEM_CLKP2	BE23	SM_CK2
TP MEM_CLKN2	EG23	SM_CK2*
TP MEM_CLKP5	BC23	SM_CK5
TP MEM_CLKN5	BD24	SM_CK5*
MEM A A<14>	BJ29	SM_MA14
MEM B A<14>	BE24	SB_MA14
TP NB_RSVD<34>	BH39	RSVD34
TP NB_RSVD<35>	AW20	RSVD35
TP NB_RSVD<36>	BK20	RSVD36
TP LVDS A DATAP3	C48	RSVD37
TP LVDS A DATAP3	D47	RSVD38
TP LVDS B DATAP3	B44	RSVD39
TP LVDS B DATAP3	C44	RSVD40
TP NB_RSVD<41>	A35	RSVD41
TP NB_RSVD<42>	B37	RSVD42
TP NB_RSVD<43>	B36	RSVD43
TP NB_RSVD<44>	B34	RSVD44
TP NB_RSVD<45>	C34	RSVD45
NB_BSEL<0>	P27	CFG0
NB_BSEL<1>	N27	CFG1
NB_BSEL<2>	N24	CFG2
NB_CFG<3>	C21	CFG3 IPU
NB_CFG<4>	C23	CFG4 IPU
NB_CFG<5>	F23	CFG5 IPU
NB_CFG<6>	N23	CFG6 IPU
NB_CFG<7>	G23	CFG7 IPU
NB_CFG<8>	J20	CFG8 IPU
NB_CFG<9>	C20	CFG9 IPU
TP NB_CFG<10>	R24	CFG10 IPU
TP NB_CFG<11>	L23	CFG11 IPU
TP NB_CFG<12>	J23	CFG12 IPU
TP NB_CFG<13>	E23	CFG13 IPU
TP NB_CFG<14>	E20	CFG14 IPU
TP NB_CFG<15>	K23	CFG15 IPU
NB_CFG<16>	M20	CFG16 IPU
TP NB_CFG<17>	M24	CFG17 IPU
TP NB_CFG<18>	L32	CFG18 IPD
NB_CFG<19>	N33	CFG19 IPD
NB_CFG<20>	L35	CFG20 IPD
PM_BMBUSY L	G41	PM_BMBUSY*
CPU DPRSTP L	L39	PM_DPRSTP*
	L36	PM_EXT_TSO*
	J36	PM_EXT_TS1*
VR_PWRGOOD DELAY	AW49	PWROK
NB_RESET L	AV20	RSTIN*
PM_THRMTRIP L	N20	THERMTRIP*
PM DPRSLPVR	G36	DPRSLPVR
TP NB_NC<1>	BJ51	NC1
TP NB_NC<2>	BK51	NC2
TP NB_NC<3>	BK50	NC3
TP NB_NC<4>	BL50	NC4
TP NB_NC<5>	BL49	NC5
TP NB_NC<6>	BL3	NC6
TP NB_NC<7>	BL2	NC7
TP NB_NC<8>	BK1	NC8
TP NB_NC<9>	BJ1	NC9
TP NB_NC<10>	E1	NC10
TP NB_NC<11>	A5	NC11
TP NB_NC<12>	B50	NC12
TP NB_NC<13>	C51	NC13
TP NB_NC<14>	A50	NC14
TP NB_NC<15>	A49	NC15
TP NB_NC<16>	BK2	NC16

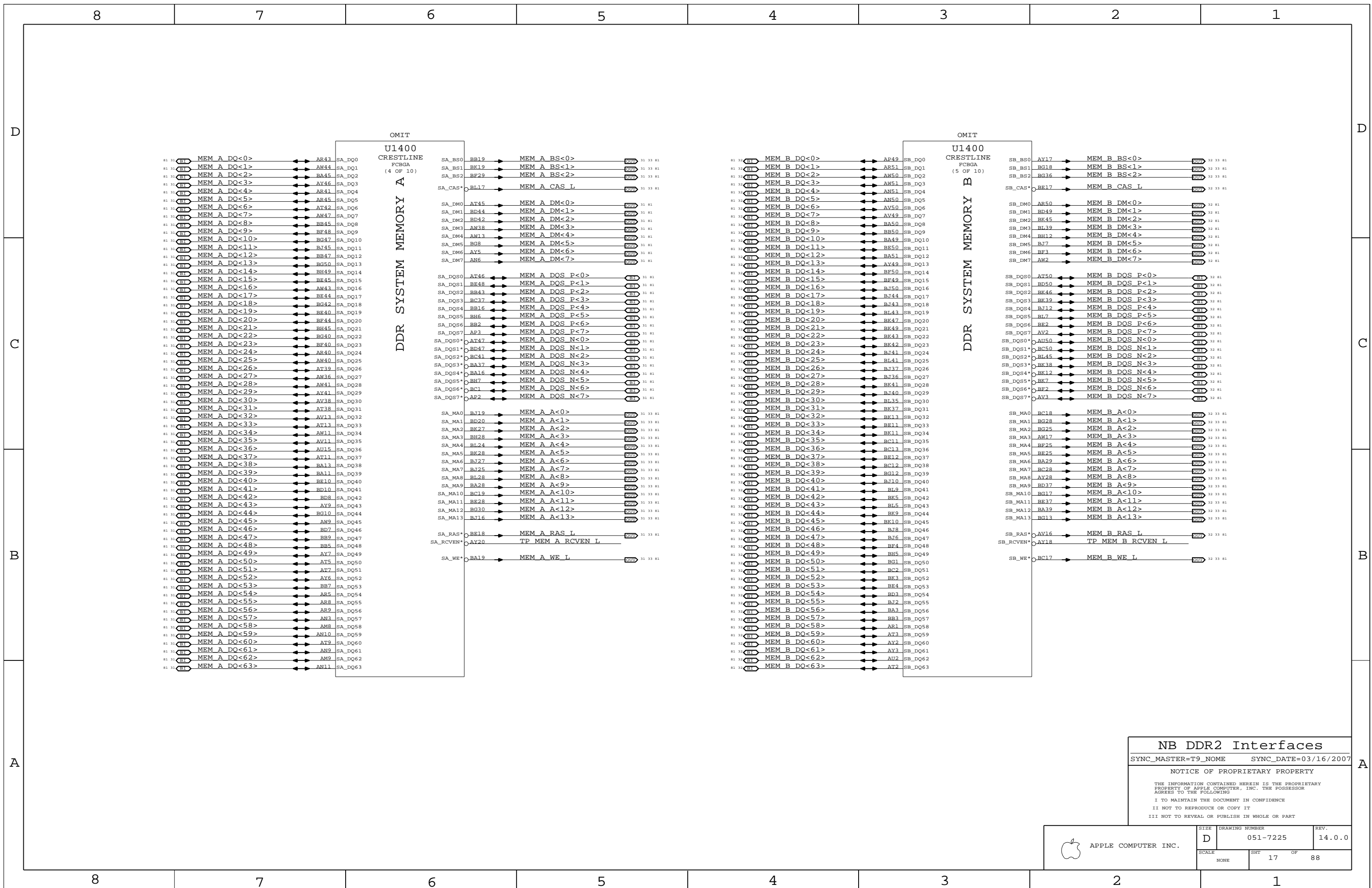
SM_CK0	AV29	MEM_CLK P<0>	9090	31 81
SM_CK1	BB23	MEM_CLK P<1>	9090	31 81
SM_CK3	BA25	MEM_CLK P<3>	9090	32 81
SM_CK4	AV23	MEM_CLK P<4>	9090	32 81
SM_CK0*	AW30	MEM_CLK N<0>	9090	31 81
SM_CK1*	BA23	MEM_CLK N<1>	9090	31 81
SM_CK3*	AW25	MEM_CLK N<3>	9090	32 81
SM_CK4*	AW23	MEM_CLK N<4>	9090	32 81
SM_CKE0	BE29	MEM_CKE<0>	9090	31 33 81
SM_CKE1	AY32	MEM_CKE<1>	9090	31 33 81
SM_CKE3	BD39	MEM_CKE<3>	9090	32 33 81
SM_CKE4	BG37	MEM_CKE<4>	9090	32 33 81
SM_CS0*	BG20	MEM_CS L<0>	9090	31 33 81
SM_CS1*	BK16	MEM_CS L<1>	9090	31 33 81
SM_CS2*	BG16	MEM_CS L<2>	9090	32 33 81
SM_CS3*	BE13	MEM_CS L<3>	9090	32 33 81
SM_ODT0	BH18	MEM_ODT<0>	9090	31 33 81
SM_ODT1	BJ15	MEM_ODT<1>	9090	31 33 81
SM_ODT2	BJ14	MEM_ODT<2>	9090	32 33 81
SM_ODT3	BE16	MEM_ODT<3>	9090	32 33 81
SM_RCOMP	BL15	MEM_RCOMP		
SM_RCOMP*	BK14	MEM_RCOMP L		
SM_RCOMP_VOH	BK11	MEM_RCOMP_VOH		
SM_RCOMP_VOL	BL31	MEM_RCOMP_VOL		
SM_VREF0	AR49			
SM_VREF1	AW4			
DPLL_REF_CLK	B42	GND		
DPLL_REF_CLK*	C42	PPVCORE S0 NB R	8 18 21 22 50	
DPLL_REF_SSCLK	H48	NB_CLK100M DPLLSS P	7 22 29 30 84	
DPLL_REF_SSCLK*	H47	NB_CLK100M DPLLSS N	7 22 29 30 84	
PEG_CLK	K44	NB_CLK100M PCIE P	7 29 30 84	
PEG_CLK*	K45	NB_CLK100M PCIE N	7 29 30 84	
		Clk used for PEG and DMI		
DMI_RXN0	AN47	DMI S2N N<0>	24 80	
DMI_RXN1	AJ38	DMI S2N N<1>	24 80	
DMI_RXN2	AN42	DMI S2N N<2>	24 80	
DMI_RXN3	AN46	DMI S2N N<3>	24 80	
DMI_RXP0	AM47	DMI S2N P<0>	24 80	
DMI_RXP1	AJ39	DMI S2N P<1>	24 80	
DMI_RXP2	AN41	DMI S2N P<2>	24 80	
DMI_RXP3	AN45	DMI S2N P<3>	24 80	
DMI_TXN0	AJ46	DMI N2S N<0>	24 80	
DMI_TXN1	AJ41	DMI N2S N<1>	24 80	
DMI_TXN2	AM40	DMI N2S N<2>	24 80	
DMI_TXN3	AM44	DMI N2S N<3>	24 80	
DMI_TXP0	AJ47	DMI N2S P<0>	24 80	
DMI_TXP1	AJ42	DMI N2S P<1>	24 80	
DMI_TXP2	AM39	DMI N2S P<2>	24 80	
DMI_TXP3	AM43	DMI N2S P<3>	24 80	
GFX_VID0	E35	GFX VID<1>	9 9	
GFX_VID1	A39	GFX VID<2>	9 9	
GFX_VID2	C38	GFX VID<3>	9 9	
GFX_VID3	B39	GFX VID<4>	9 9	
GFX_VR_EN	E36	GFX VR_EN	9 9	
CL_CLK	AM49	CLINK NB CLK	25 83	
CL_DATA	AK50	CLINK NB DATA	25 83	
CL_PWROK	AT43	VR_PWRGOOD DELAY	9 14 28 58	
CL_RST*	AN49	CLINK NB RESET L	25 83	
CL_VREF	AM50	NB CLINK VREF	25 83	
SDVO_CTRL_CLK	H35	GND		
SDVO_CTRL_DATA	K36	GND		
CLKREQ*	G39	NB_CLKREQ L	7 29	
ICH_SYNC*	G40	NB_SB_SYNC L	7 25	
TEST1	A37	NB TEST1		
TEST2	R32	NB TEST2		



NB Misc Interfaces		
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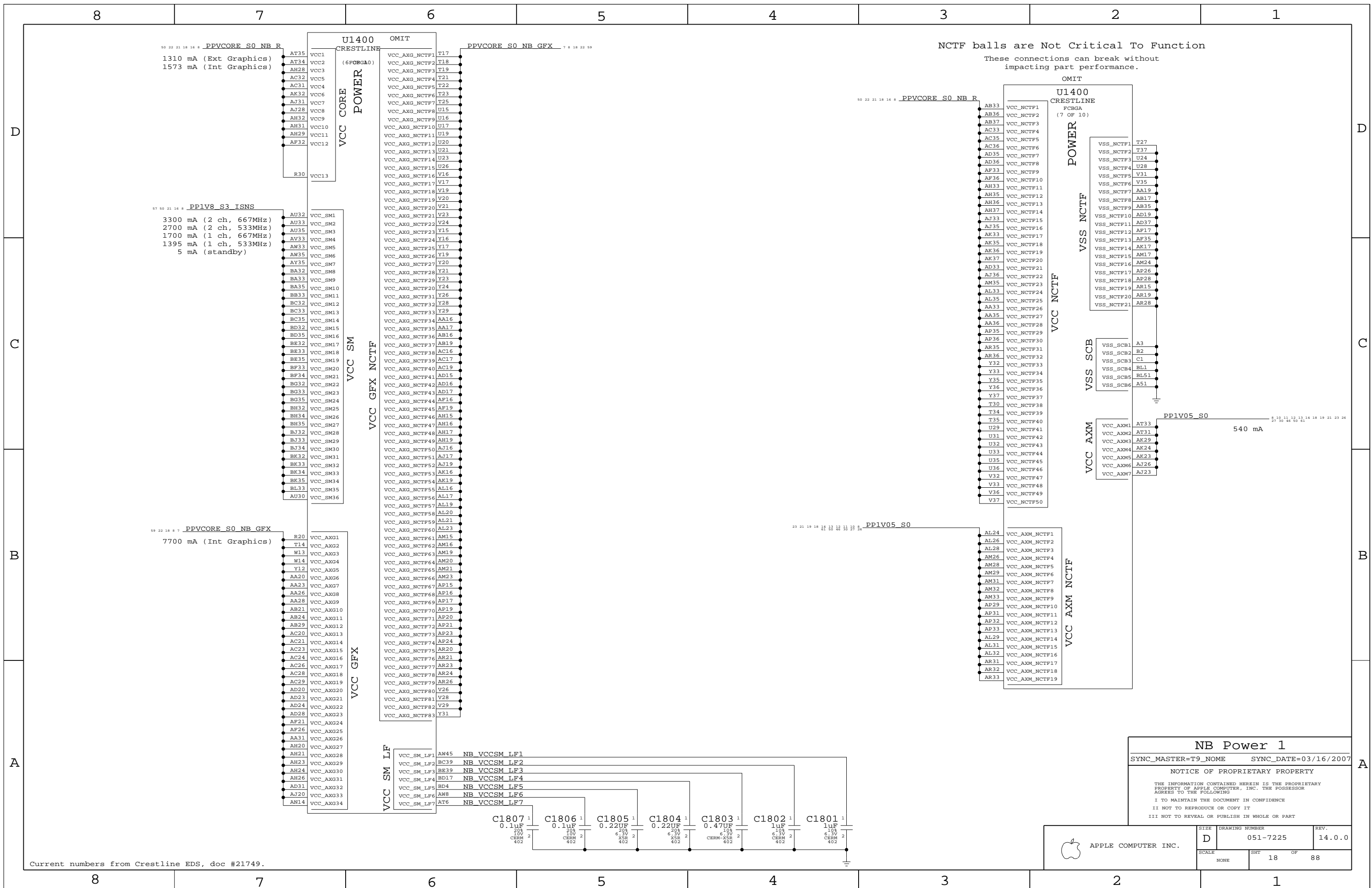
NB DDR2 Interfaces

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	SCALE NONE	SHEET 17	OF 88



50 22 21 18 16 8 PPVCORE_S0_NB_R
 1310 mA (Ext Graphics)
 1573 mA (Int Graphics)

57 50 21 16 8 PP1V8_S3_ISNS
 3300 mA (2 ch, 667MHz)
 2700 mA (2 ch, 533MHz)
 1700 mA (1 ch, 667MHz)
 1395 mA (1 ch, 533MHz)
 5 mA (standby)

59 22 18 8 7 PPVCORE_S0_NB_GFX
 7700 mA (Int Graphics)

NCTF balls are Not Critical To Function
 These connections can break without
 impacting part performance.

D
C
B
A

D
C
B
A

Pin	Power Plane	Pin	Power Plane
T17	VCC_AXG_NCTF1	AA16	VCC_AXG_NCTF33
T18	VCC_AXG_NCTF2	AA17	VCC_AXG_NCTF34
T19	VCC_AXG_NCTF3	AA17	VCC_AXG_NCTF35
T21	VCC_AXG_NCTF4	AA16	VCC_AXG_NCTF36
T22	VCC_AXG_NCTF5	AB19	VCC_AXG_NCTF37
T23	VCC_AXG_NCTF6	AC16	VCC_AXG_NCTF38
T25	VCC_AXG_NCTF7	AC17	VCC_AXG_NCTF39
U15	VCC_AXG_NCTF8	AC19	VCC_AXG_NCTF40
U16	VCC_AXG_NCTF9	AD15	VCC_AXG_NCTF41
U17	VCC_AXG_NCTF10	AD16	VCC_AXG_NCTF42
U19	VCC_AXG_NCTF11	AD17	VCC_AXG_NCTF43
U20	VCC_AXG_NCTF12	AF16	VCC_AXG_NCTF44
U21	VCC_AXG_NCTF13	AF19	VCC_AXG_NCTF45
U23	VCC_AXG_NCTF14	AH15	VCC_AXG_NCTF46
U26	VCC_AXG_NCTF15	AH16	VCC_AXG_NCTF47
V16	VCC_AXG_NCTF16	AH17	VCC_AXG_NCTF48
V17	VCC_AXG_NCTF17	AH19	VCC_AXG_NCTF49
V19	VCC_AXG_NCTF18	AJ16	VCC_AXG_NCTF50
V20	VCC_AXG_NCTF19	AJ17	VCC_AXG_NCTF51
V21	VCC_AXG_NCTF20	AJ19	VCC_AXG_NCTF52
V23	VCC_AXG_NCTF21	AK16	VCC_AXG_NCTF53
V24	VCC_AXG_NCTF22	AK19	VCC_AXG_NCTF54
Y15	VCC_AXG_NCTF23	AL16	VCC_AXG_NCTF55
Y16	VCC_AXG_NCTF24	AL17	VCC_AXG_NCTF56
Y17	VCC_AXG_NCTF25	AL19	VCC_AXG_NCTF57
Y19	VCC_AXG_NCTF26	AL20	VCC_AXG_NCTF58
Y20	VCC_AXG_NCTF27	AL21	VCC_AXG_NCTF59
Y21	VCC_AXG_NCTF28	AL23	VCC_AXG_NCTF60
Y22	VCC_AXG_NCTF29	AM15	VCC_AXG_NCTF61
Y24	VCC_AXG_NCTF30	AM16	VCC_AXG_NCTF62
Y26	VCC_AXG_NCTF31	AM19	VCC_AXG_NCTF63
Y28	VCC_AXG_NCTF32	AM20	VCC_AXG_NCTF64
Y29	VCC_AXG_NCTF33	AM21	VCC_AXG_NCTF65
AA16	VCC_AXG_NCTF34	AM23	VCC_AXG_NCTF66
AA17	VCC_AXG_NCTF35	AP15	VCC_AXG_NCTF67
AA16	VCC_AXG_NCTF36	AP16	VCC_AXG_NCTF68
AB19	VCC_AXG_NCTF37	AP17	VCC_AXG_NCTF69
AC16	VCC_AXG_NCTF38	AP19	VCC_AXG_NCTF70
AC17	VCC_AXG_NCTF39	AP20	VCC_AXG_NCTF71
AC19	VCC_AXG_NCTF40	AP21	VCC_AXG_NCTF72
AD15	VCC_AXG_NCTF41	AP23	VCC_AXG_NCTF73
AD16	VCC_AXG_NCTF42	AP24	VCC_AXG_NCTF74
AD17	VCC_AXG_NCTF43	AR20	VCC_AXG_NCTF75
AF16	VCC_AXG_NCTF44	AR21	VCC_AXG_NCTF76
AF19	VCC_AXG_NCTF45	AR23	VCC_AXG_NCTF77
AH15	VCC_AXG_NCTF46	AR24	VCC_AXG_NCTF78
AH16	VCC_AXG_NCTF47	AR26	VCC_AXG_NCTF79
AH17	VCC_AXG_NCTF48	V26	VCC_AXG_NCTF80
AH19	VCC_AXG_NCTF49	V28	VCC_AXG_NCTF81
AJ16	VCC_AXG_NCTF50	V29	VCC_AXG_NCTF82
AJ17	VCC_AXG_NCTF51	Y31	VCC_AXG_NCTF83
AJ19	VCC_AXG_NCTF52		
AK16	VCC_AXG_NCTF53		
AK19	VCC_AXG_NCTF54		
AL16	VCC_AXG_NCTF55		
AL17	VCC_AXG_NCTF56		
AL19	VCC_AXG_NCTF57		
AL20	VCC_AXG_NCTF58		
AL21	VCC_AXG_NCTF59		
AL23	VCC_AXG_NCTF60		
AM15	VCC_AXG_NCTF61		
AM16	VCC_AXG_NCTF62		
AM19	VCC_AXG_NCTF63		
AM20	VCC_AXG_NCTF64		
AM21	VCC_AXG_NCTF65		
AM23	VCC_AXG_NCTF66		
AP15	VCC_AXG_NCTF67		
AP16	VCC_AXG_NCTF68		
AP17	VCC_AXG_NCTF69		
AP19	VCC_AXG_NCTF70		
AP20	VCC_AXG_NCTF71		
AP21	VCC_AXG_NCTF72		
AP23	VCC_AXG_NCTF73		
AP24	VCC_AXG_NCTF74		
AR20	VCC_AXG_NCTF75		
AR21	VCC_AXG_NCTF76		
AR23	VCC_AXG_NCTF77		
AR24	VCC_AXG_NCTF78		
AR26	VCC_AXG_NCTF79		
V26	VCC_AXG_NCTF80		
V28	VCC_AXG_NCTF81		
V29	VCC_AXG_NCTF82		
Y31	VCC_AXG_NCTF83		

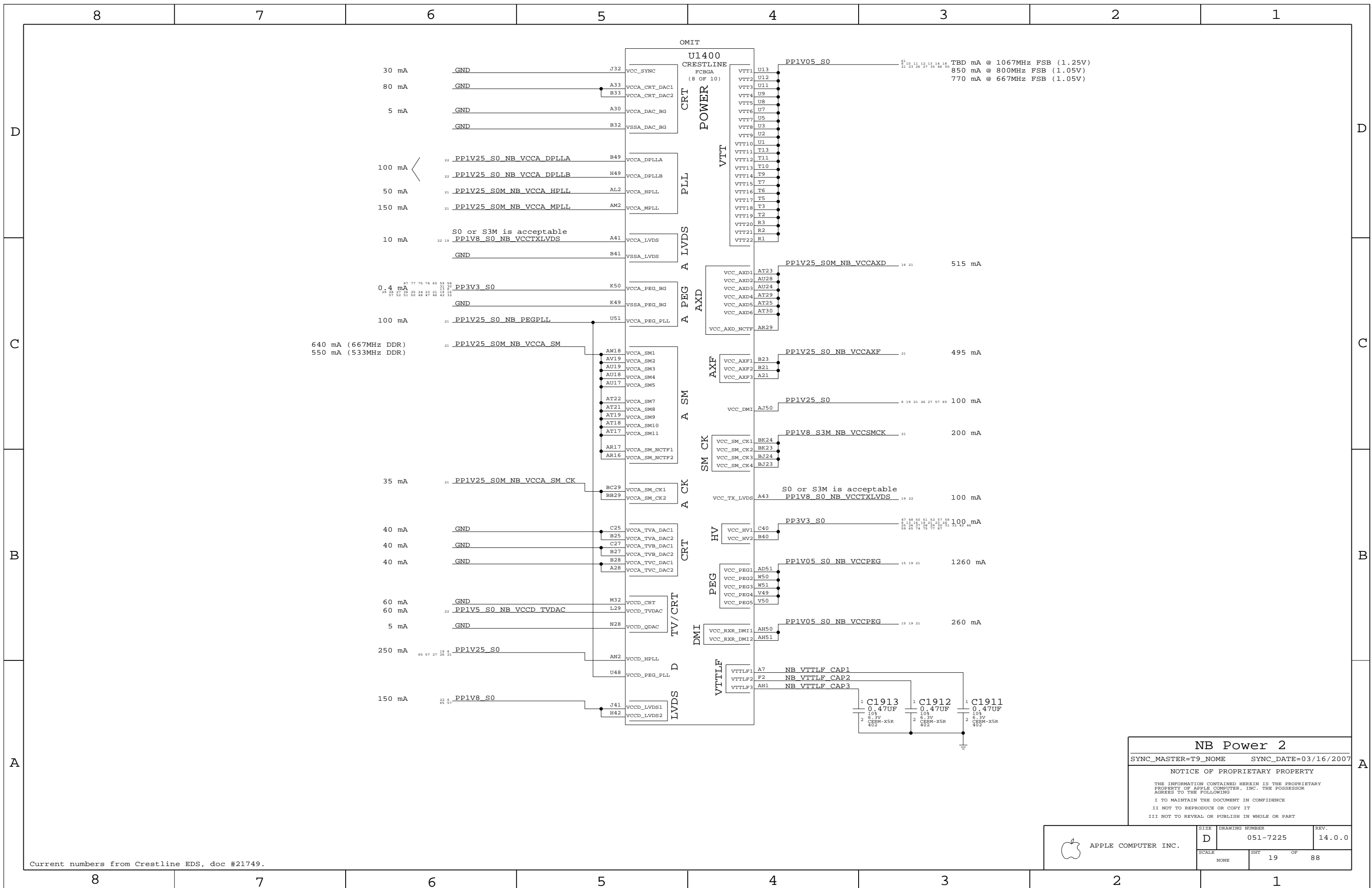
Pin	Power Plane	Pin	Power Plane
AM45	NB_VCCSM_LF1	BC39	NB_VCCSM_LF2
BC39	NB_VCCSM_LF2	BE39	NB_VCCSM_LF3
BE39	NB_VCCSM_LF3	BD17	NB_VCCSM_LF4
BD17	NB_VCCSM_LF4	BD4	NB_VCCSM_LF5
BD4	NB_VCCSM_LF5	AW8	NB_VCCSM_LF6
AW8	NB_VCCSM_LF6	AT6	NB_VCCSM_LF7
AT6	NB_VCCSM_LF7		

- C1807 1 0.1uF 20% 10V CERM 402
- C1806 1 0.1uF 20% 10V CERM 402
- C1805 1 0.22uF 20% 6.3V X5R 402
- C1804 1 0.22uF 20% 6.3V X5R 402
- C1803 1 0.47uF 10% 6.3V CERM-X5R 402
- C1802 1 1uF 10% 6.3V CERM 402
- C1801 1 1uF 10% 6.3V CERM 402

NB Power 1
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	18	88	14.0.0

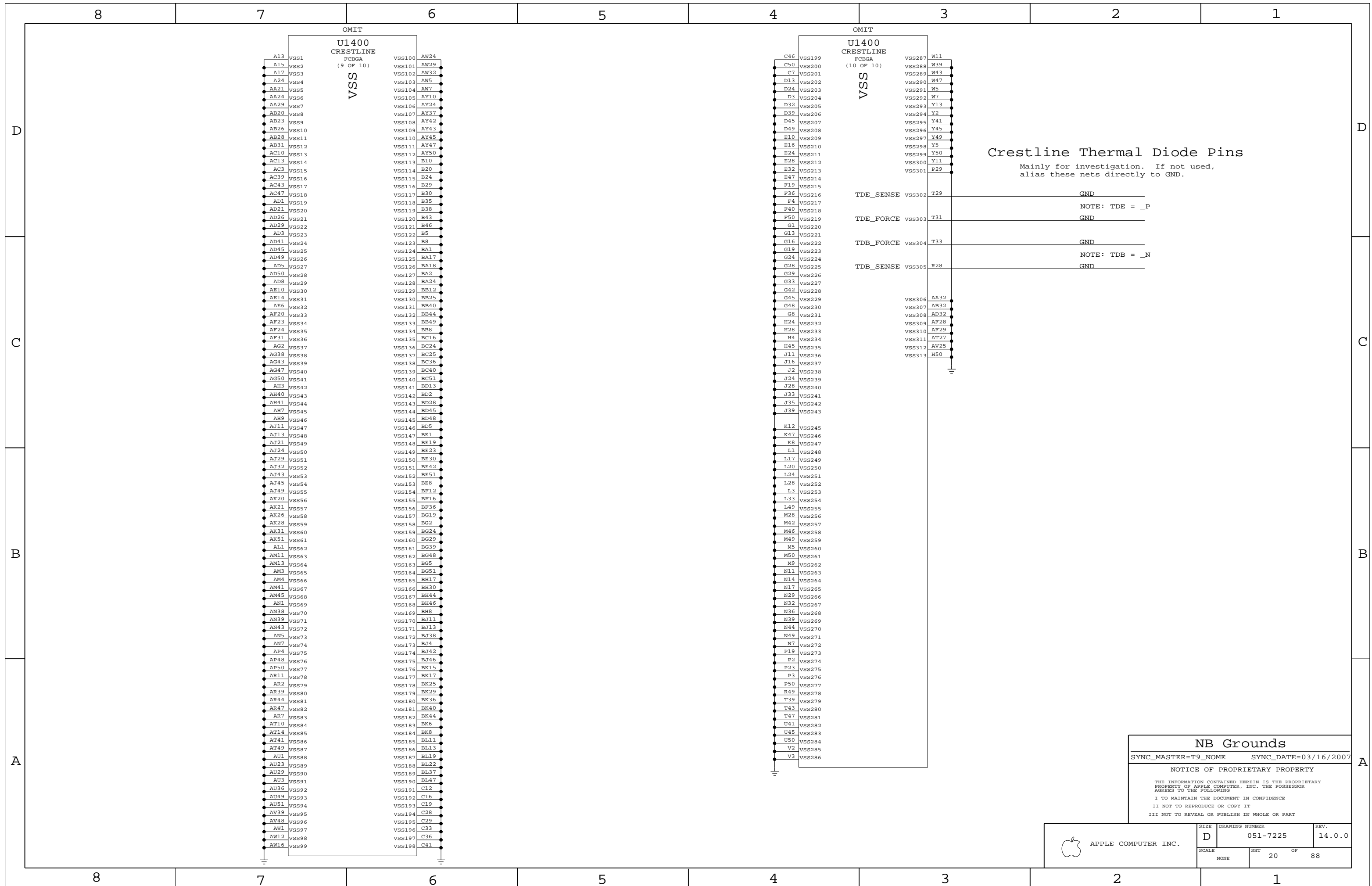
Current numbers from Crestline EDS, doc #21749.



Current numbers from Crestline EDS, doc #21749.

NB Power 2
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	19	88	



Crestline Thermal Diode Pins
 Mainly for investigation. If not used,
 alias these nets directly to GND.

NB Grounds

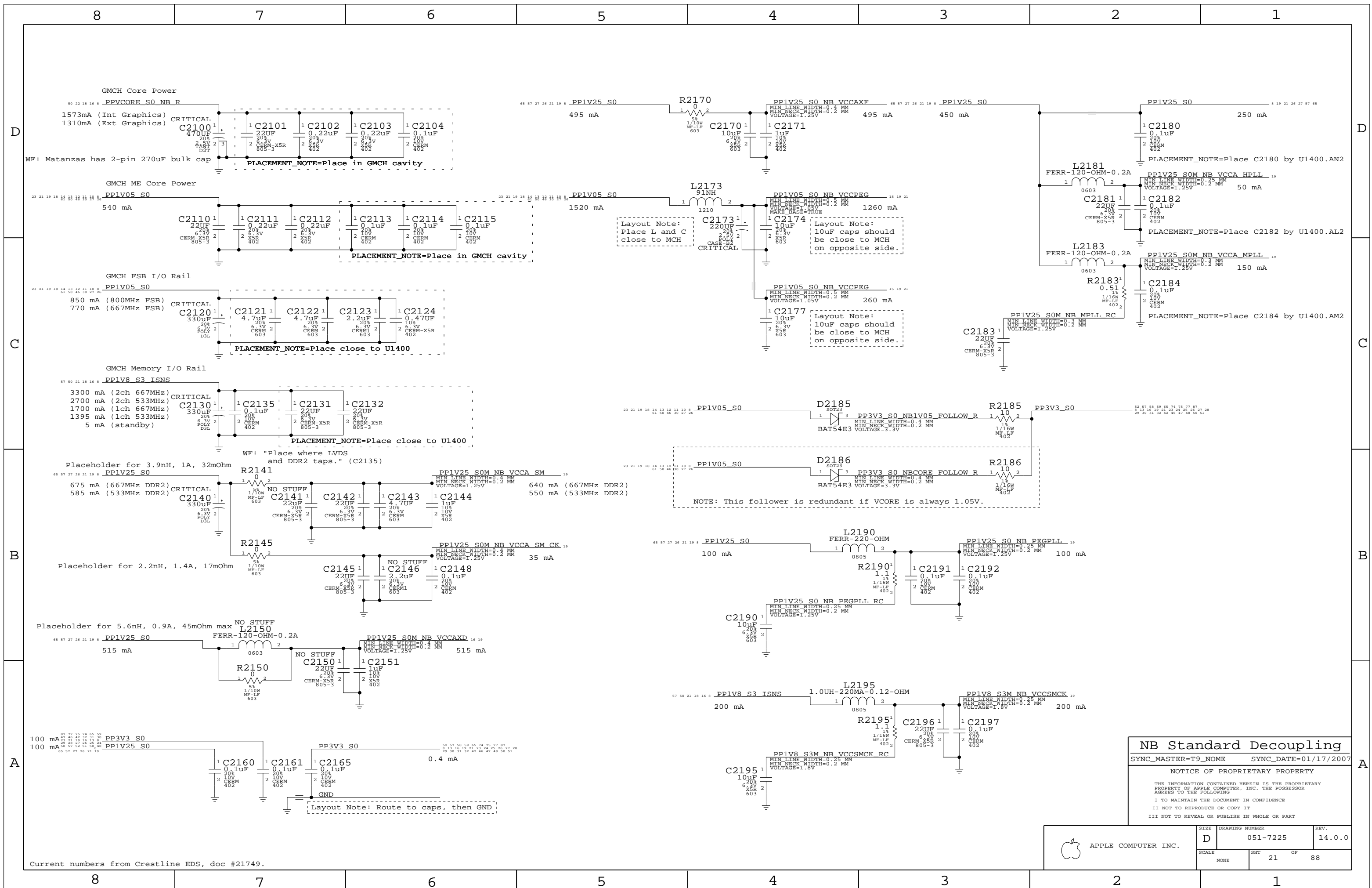
SYNC_MASTER=T9_NAME SYNC_DATE=03/16/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	20	88	



NB Standard Decoupling

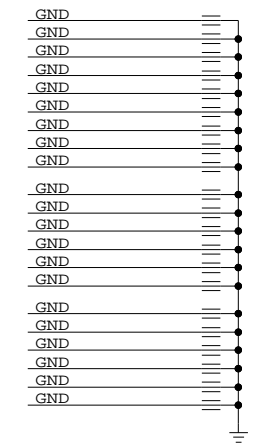
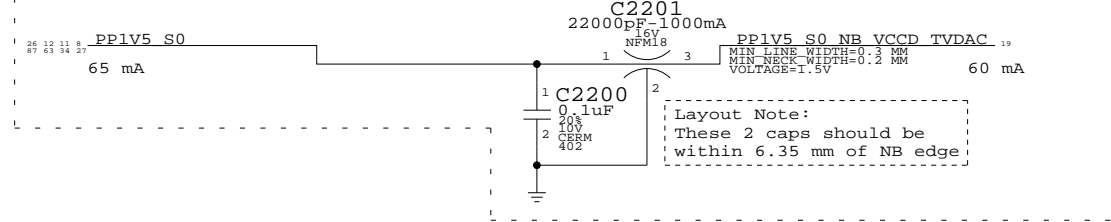
SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

NOTICE OF PROPRIETARY PROPERTY

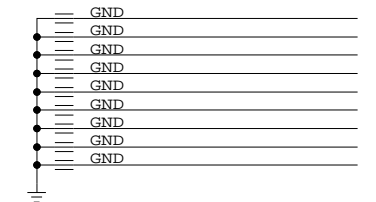
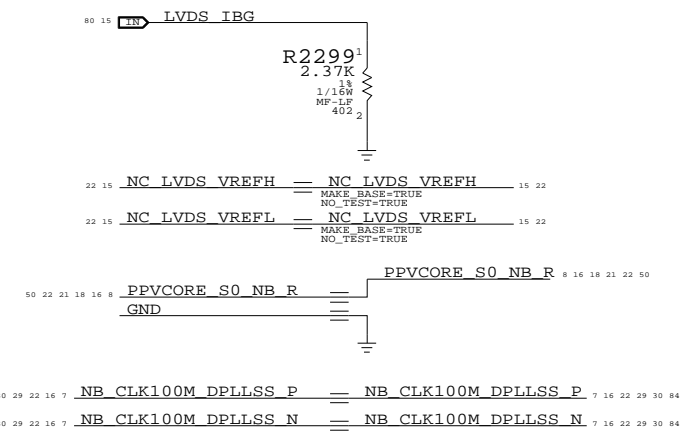
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHEET 21	OF 88

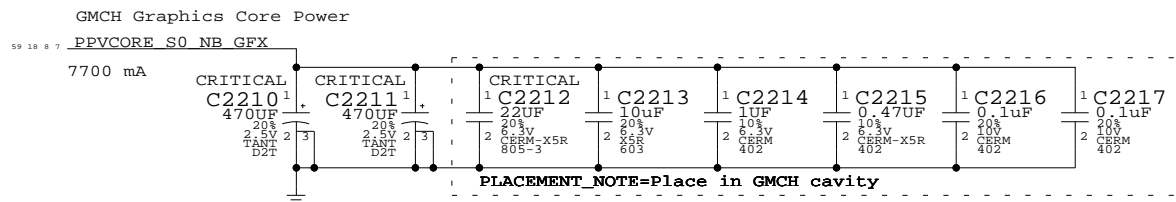
NOTE: This filter is required even if using only external graphics.
 VCCD_TVDAC also powers internal thermal sensors.



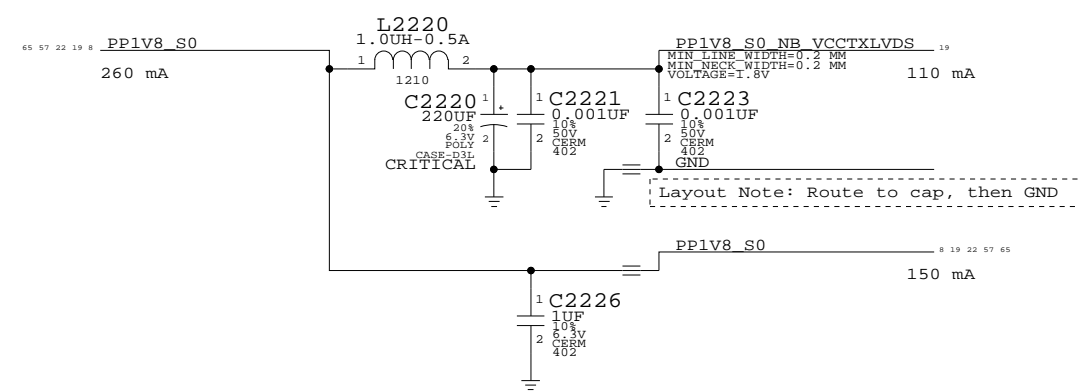
Crestline LVDS Support



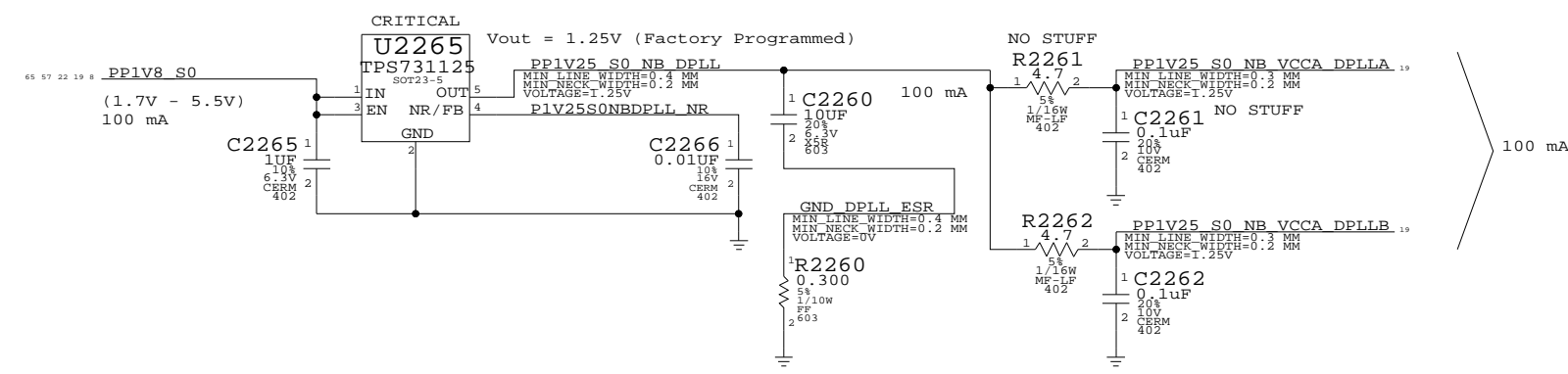
C



B



A



NB Graphics Decoupling

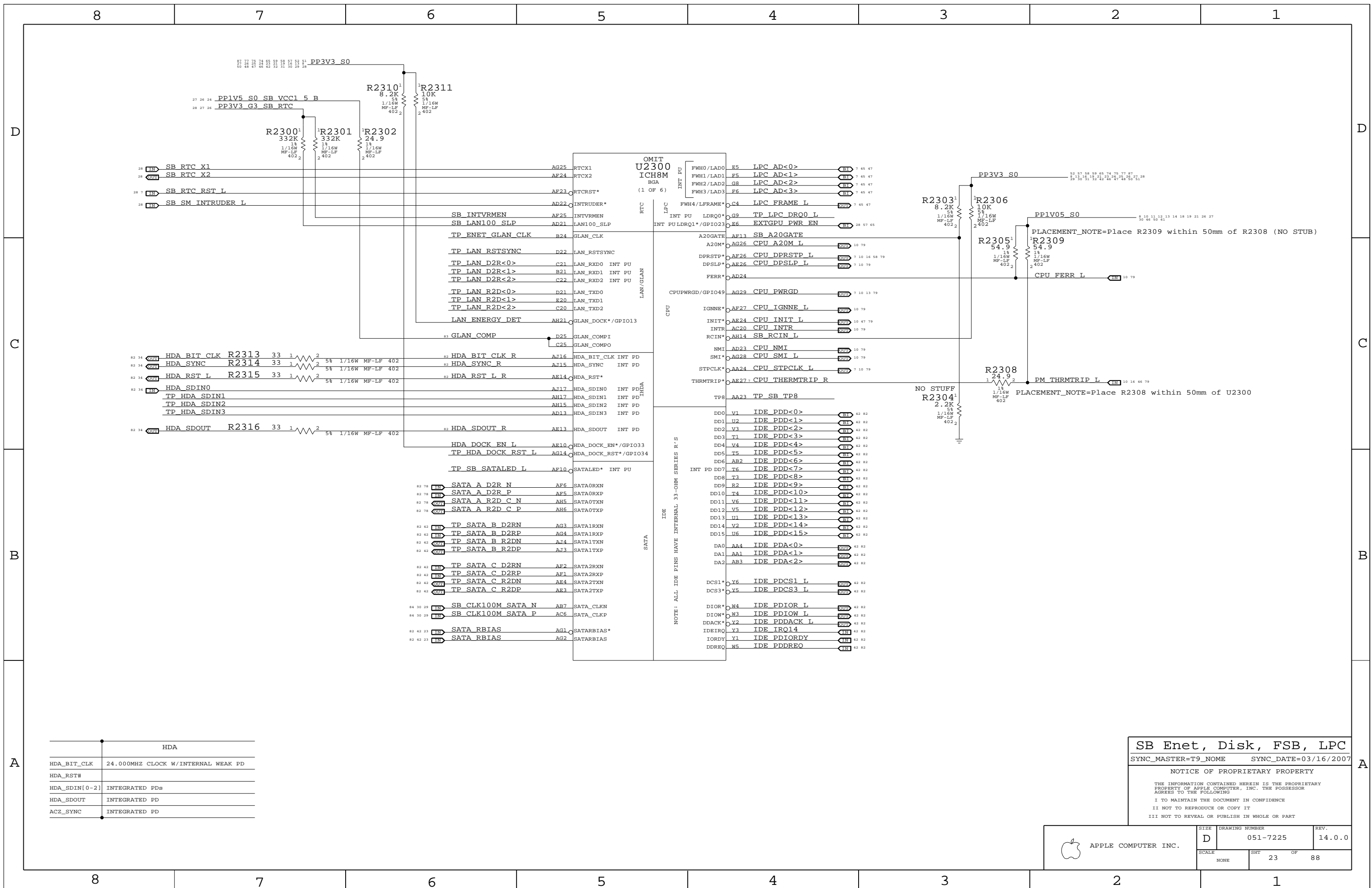
SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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	D	051-7225	14.0.0
SCALE	SHT	OF	REV.
NONE	22	88	

Current numbers from Crestline EDS Addendum, doc #20127.



HDA	
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

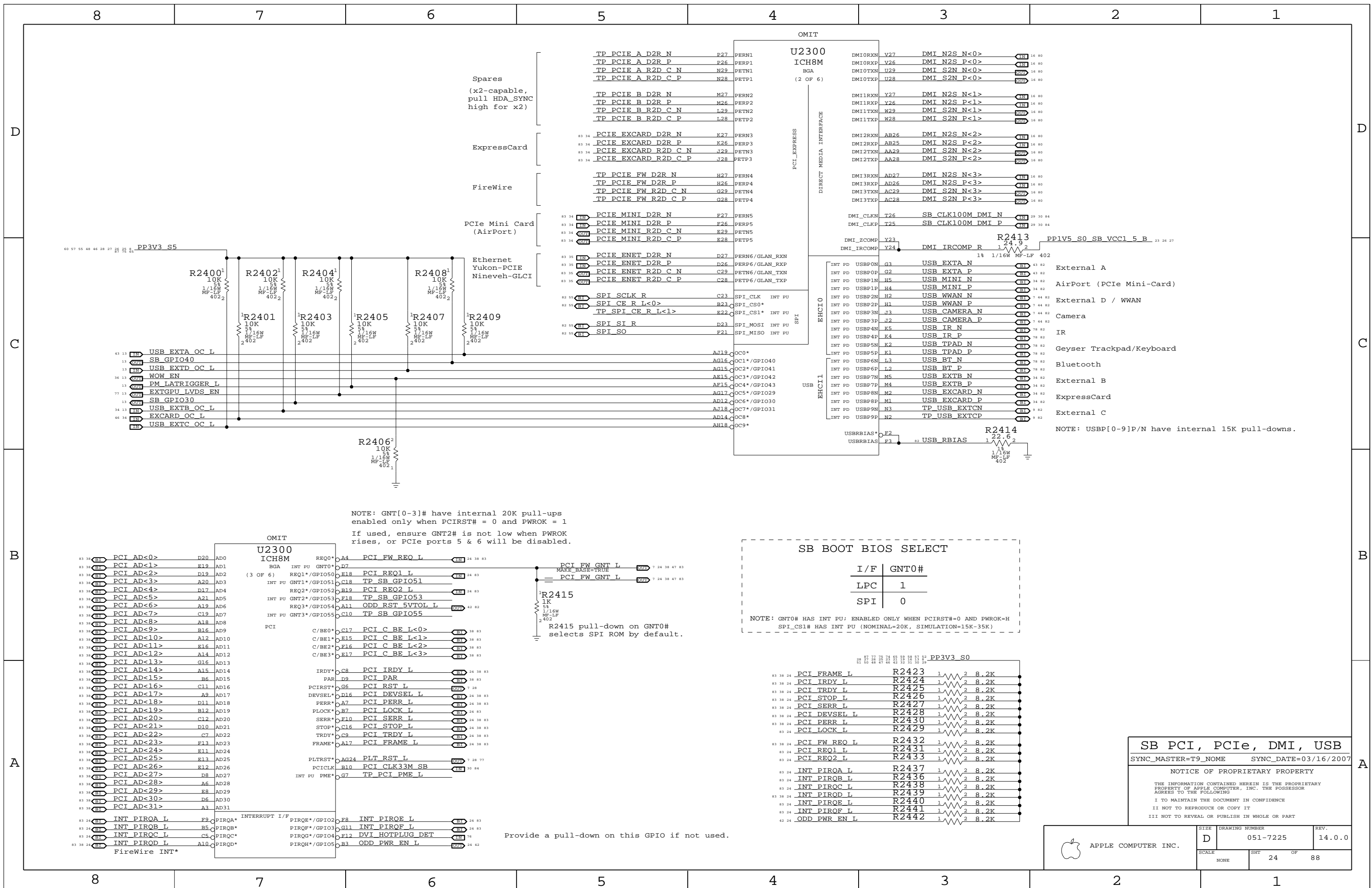
SB Enet, Disk, FSB, LPC
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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	D	051-7225	14.0.0
SCALE	SHT	OF	REV.
NONE	23	88	



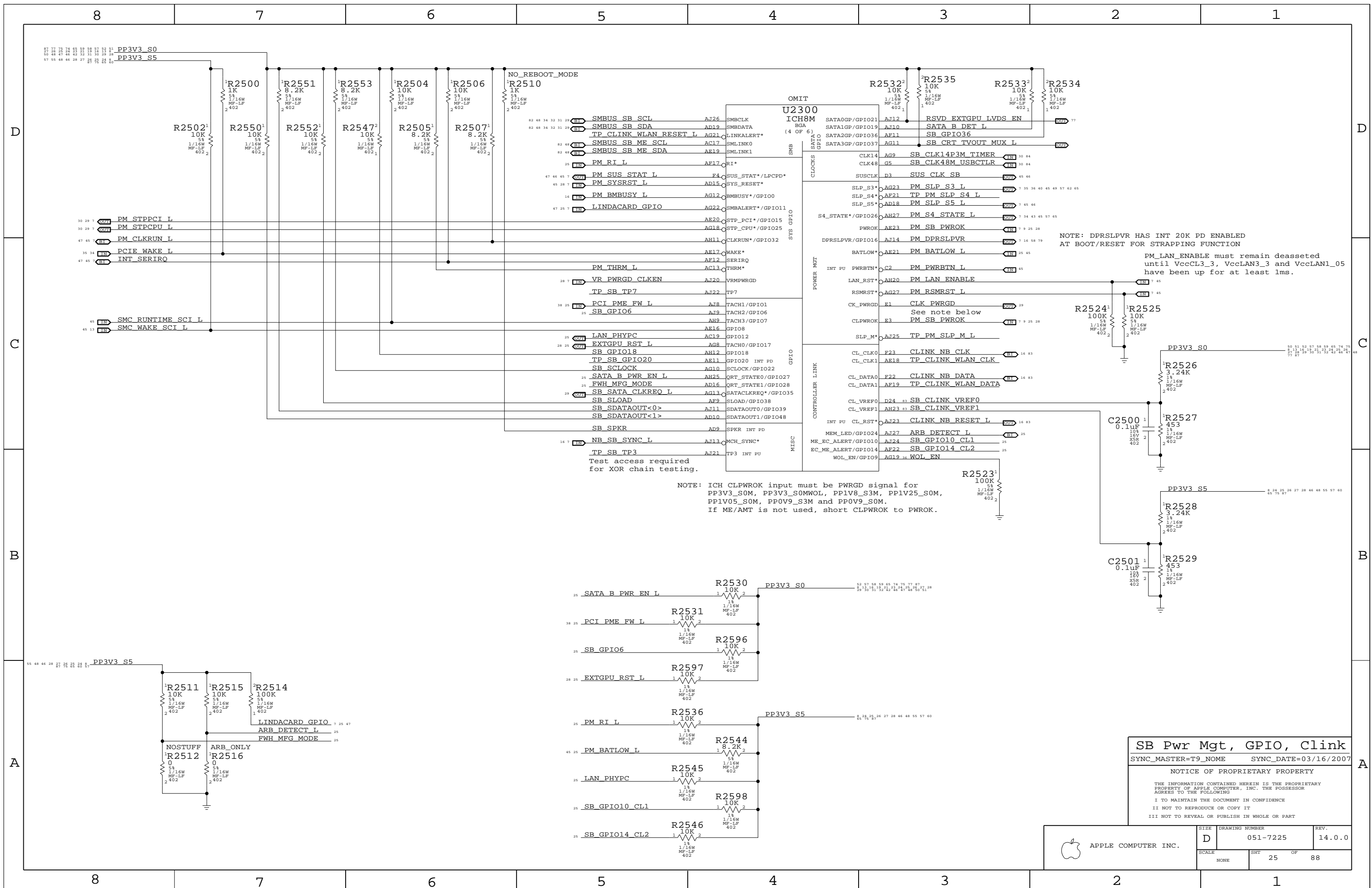
NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H. SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K).

Provide a pull-down on this GPIO if not used.

SB PCI, PCIe, DMI, USB
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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U2300 ICH8M BGA (4 OF 6)

Signal	Pin	Function
SMBUS_SB_SCL	AJ26	SMBCLK
SMBUS_SB_SDA	AD19	SMBDATA
TP_CLINK_WLAN_RESET L	AG21	LINKALERT*
SMBUS_SB_ME_SCL	AC17	SMLINK0
SMBUS_SB_ME_SDA	AE19	SMLINK1
PM_RI L	AF17	RI*
PM_SUS_STAT L	F4	SUS_STAT*/LPCPD*
PM_SYSRST L	AD15	SYS_RESET*
PM_BMBUSY L	AG12	BMBUSY*/GPIO0
LINDACARD_GPIO	AG22	SMBALERT*/GPIO11
	AE20	STP_PCI*/GPIO15
	AG18	STP_CPU*/GPIO25
	AH11	CLKRUN*/GPIO32
	AE17	WAKE*
	AF12	SERIRQ
	AC13	THRM*
VR_PWRGD_CLKEN	AJ20	VRMPWRGD
TP_SB_TP7	AJ22	TP7
PCI_PME_FW L	AJ8	TACH1/GPIO1
SB_GPIO6	AD9	TACH2/GPIO6
	AH9	TACH3/GPIO7
	AE16	GPIO8
LAN_PHYPC	AC19	GPIO12
EXTGPU_RST L	AG8	TACH0/GPIO17
SB_GPIO18	AH12	GPIO18
TP_SB_GPIO20	AE11	GPIO20 INT PD
SB_SCLK	AG10	SCLK/GPIO22
SATA_B_PWR_EN L	AH25	QRT_STATE0/GPIO27
FWH_MFG_MODE	AD16	QRT_STATE1/GPIO28
SB_SATA_CLKREQ L	AG13	SATACLKREQ*/GPIO35
SB_SLOAD	AE9	SLOAD/GPIO38
SB_SDATAOUT<0>	AJ11	SDATAOUT0/GPIO39
SB_SDATAOUT<1>	AD10	SDATAOUT1/GPIO48
SB_SPKR	AD9	SPKR INT PD
NB_SB_SYNC L	AJ13	MCH_SYNC*
TP_SB_TP3	AJ21	TP3 INT PU

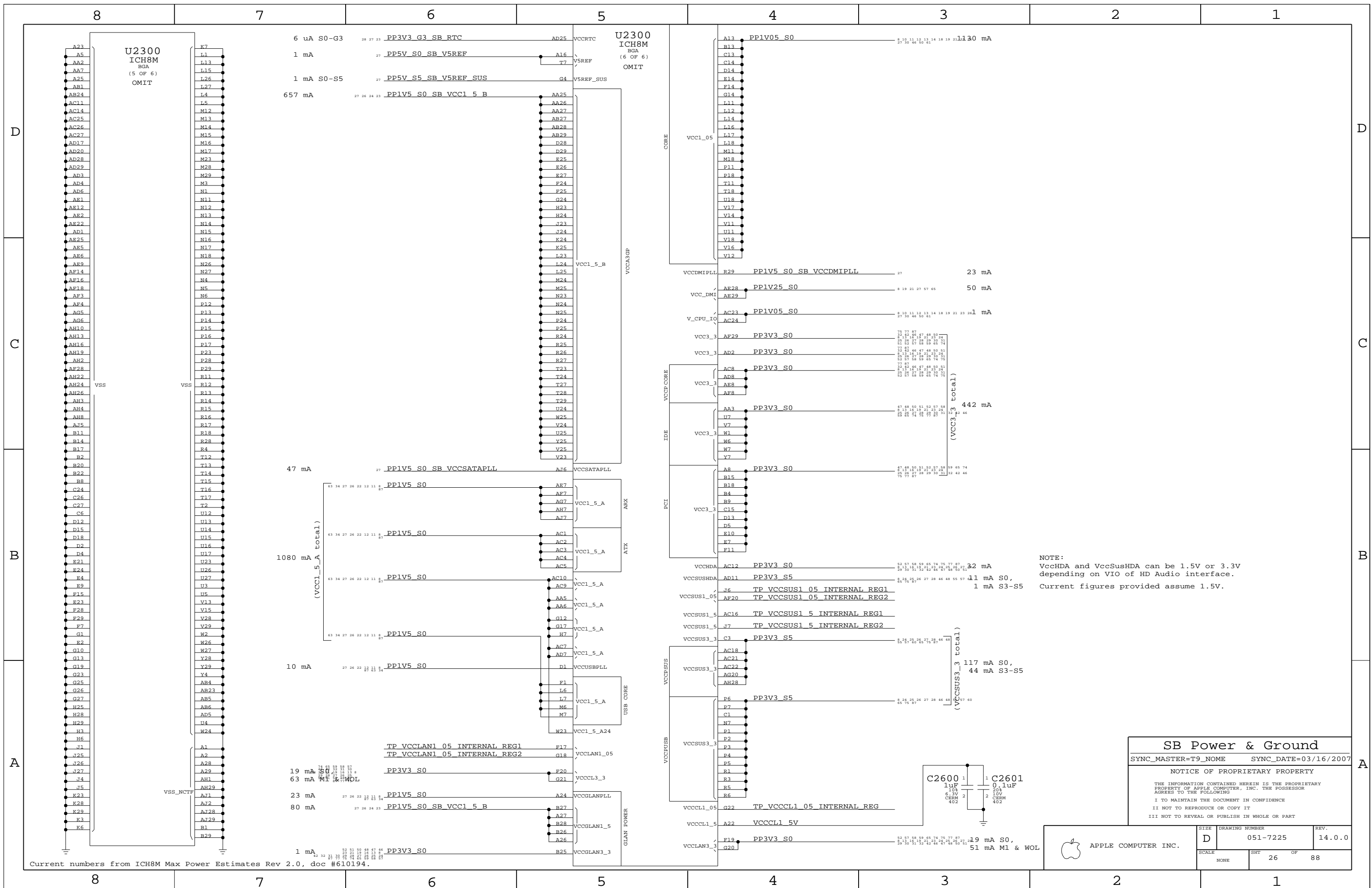
NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION
 PM_LAN_ENABLE must remain deasserted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

SB Pwr Mgt, GPIO, Clink
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

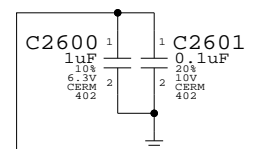
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	25	88	



Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
Current figures provided assume 1.5V.



SB Power & Ground

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

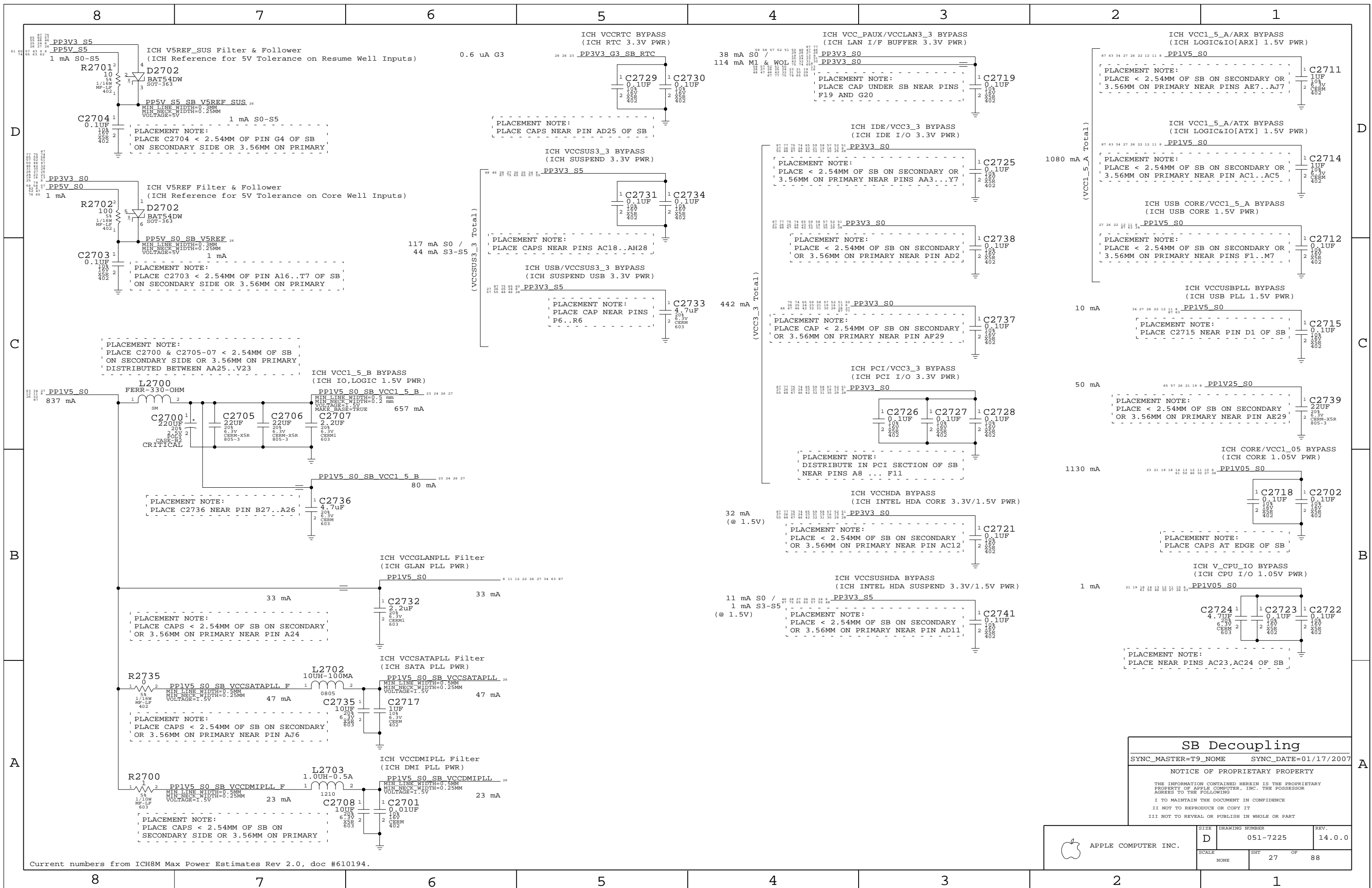
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SCALE NONE	SHT 26	OF 88	SIZE	DRAWING NUMBER	REV.
			D	051-7225	14.0.0



APPLE COMPUTER INC.



SB Decoupling

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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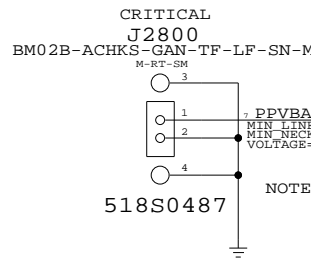
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

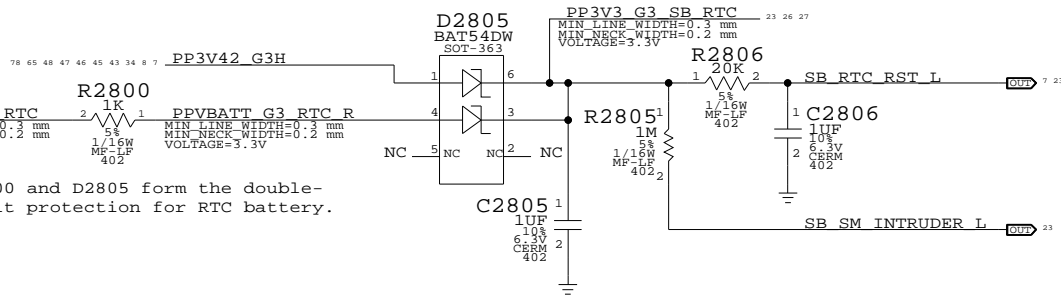
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHEET 27	OF 88

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

Coin-Cell Connector

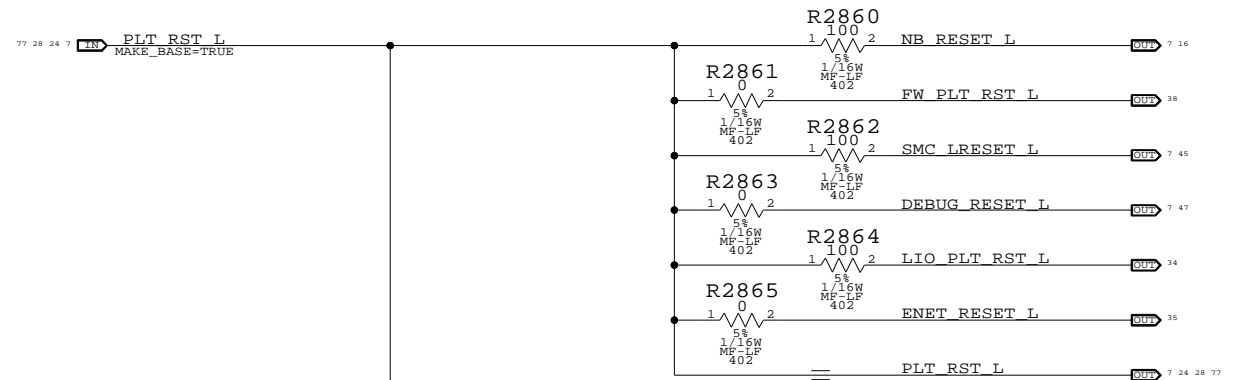


RTC Power Sources

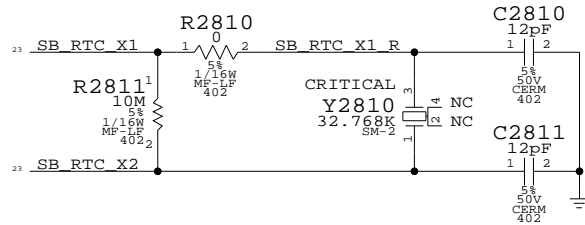


Platform Reset Connections

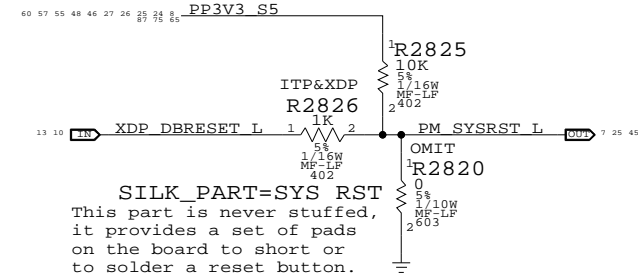
Unbuffered



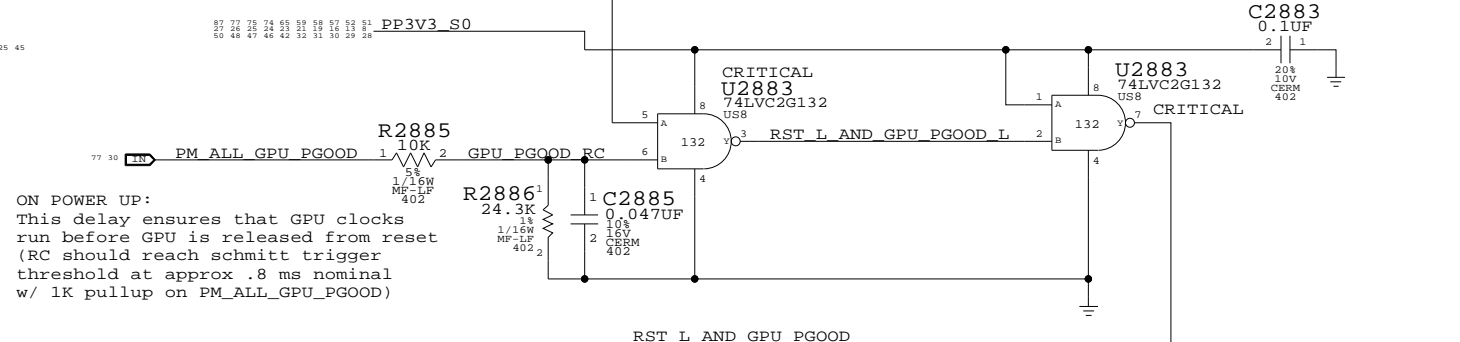
SB RTC Crystal



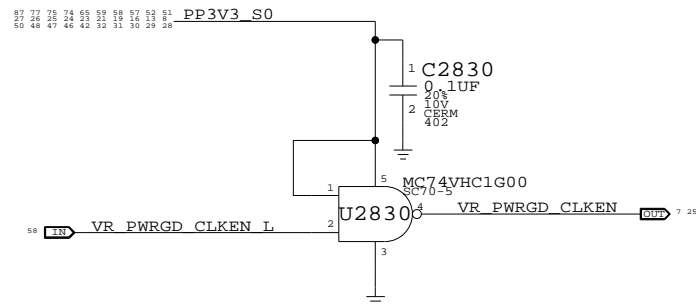
System Reset "Button"



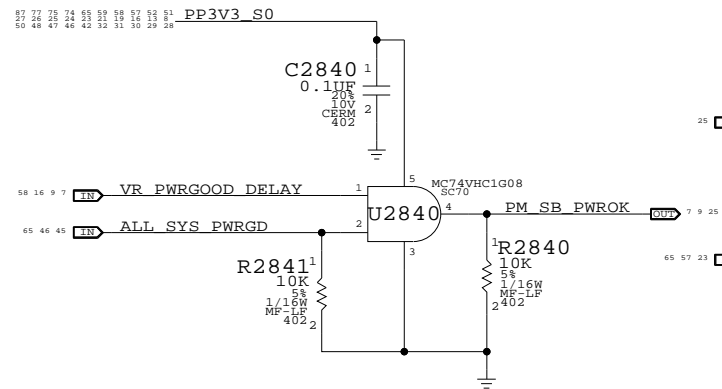
Muxed GFX GPU Reset Support



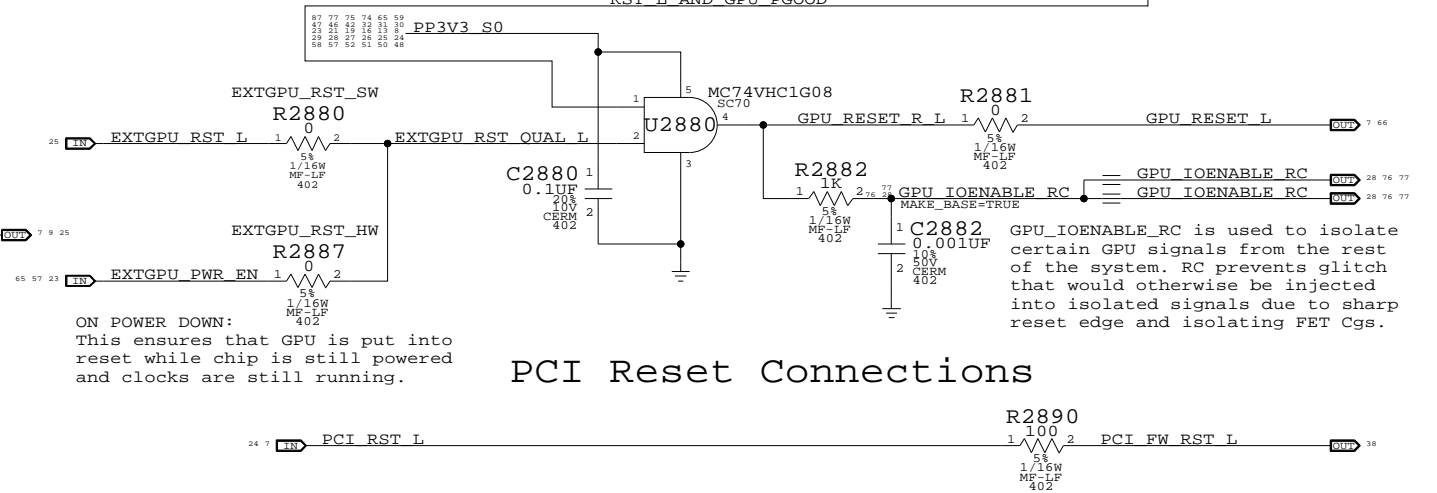
VRMPWRGD Inverter



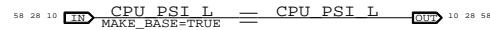
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI



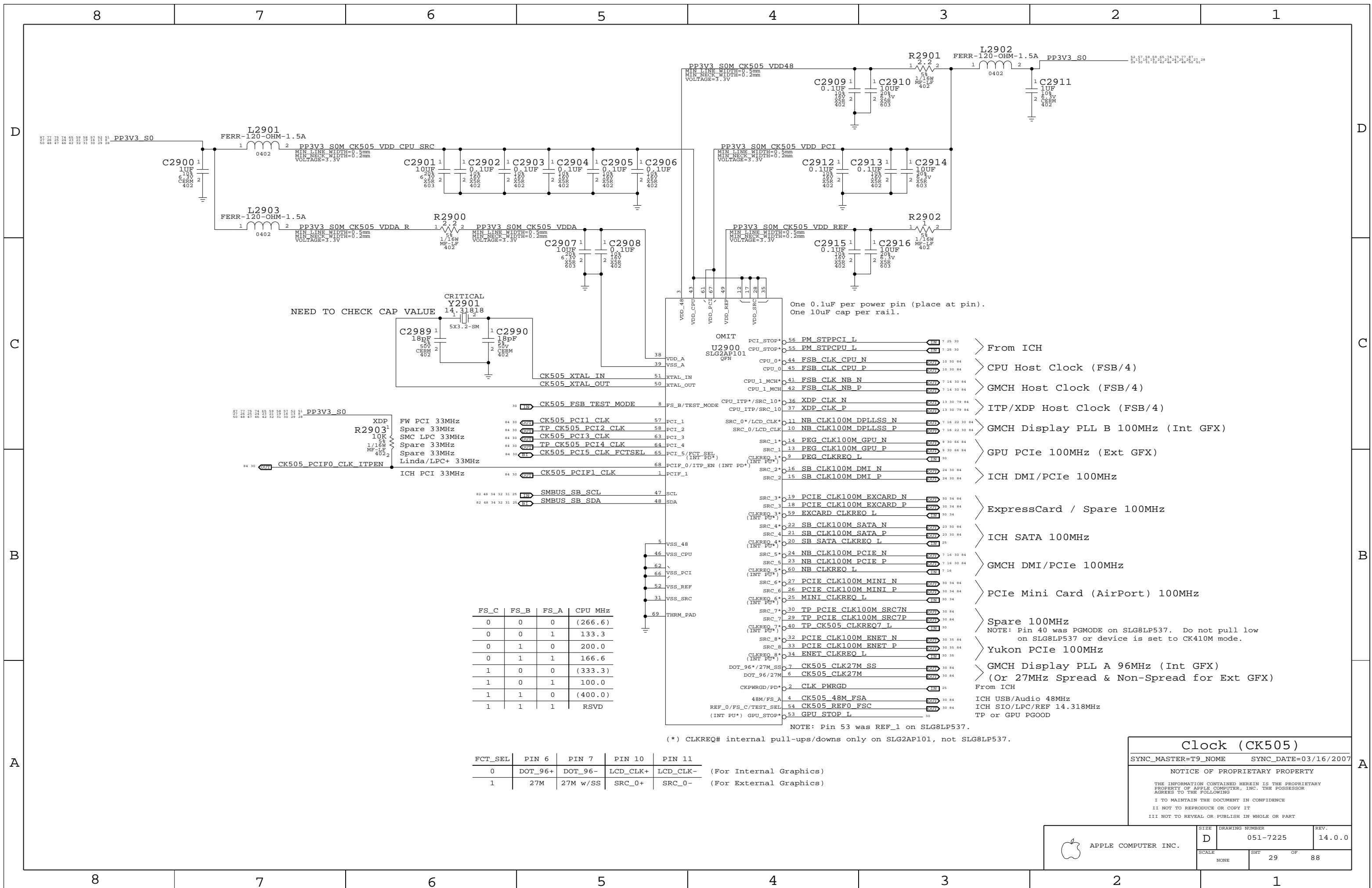
SB Misc

SYNC_MASTER=(T9_MLB) SYNC_DATE=08/24/2006

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SCALE	SHT	OF	
NONE	28	88	



One 0.1uF per power pin (place at pin).
One 10uF cap per rail.

NEED TO CHECK CAP VALUE

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

- > From ICH
- > CPU Host Clock (FSB/4)
- > GMCH Host Clock (FSB/4)
- > ITP/XDP Host Clock (FSB/4)
- > GMCH Display PLL B 100MHz (Int GFX)
- > GPU PCIe 100MHz (Ext GFX)
- > ICH DMI/PCIe 100MHz
- > ExpressCard / Spare 100MHz
- > ICH SATA 100MHz
- > GMCH DMI/PCIe 100MHz
- > PCIe Mini Card (AirPort) 100MHz
- > Spare 100MHz
- NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
- > Yukon PCIe 100MHz
- > GMCH Display PLL A 96MHz (Int GFX)
- > (Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
- ICH SIO/LPC/REF 14.318MHz
- TP or GPU PGOOD

NOTE: Pin 53 was REF_1 on SLG8LP537.

(*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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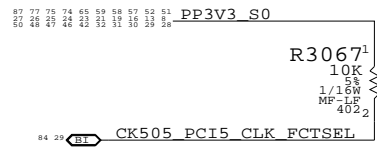
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	29	88	

CLK Termination

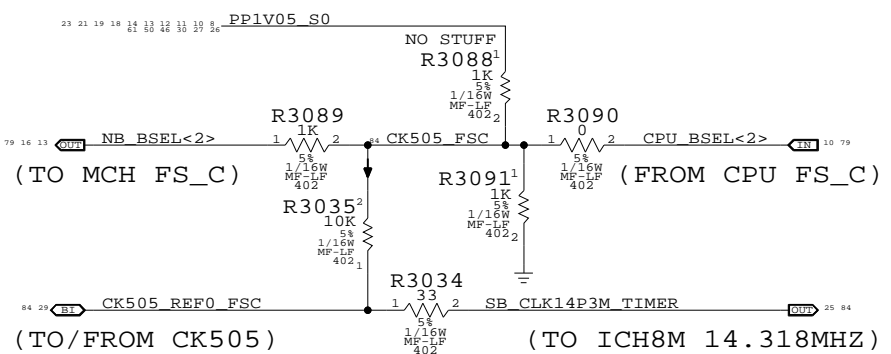
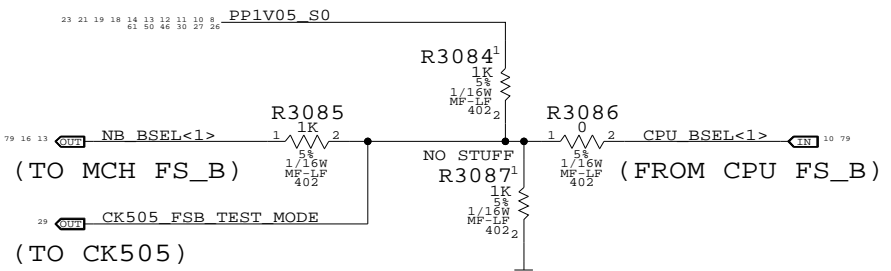
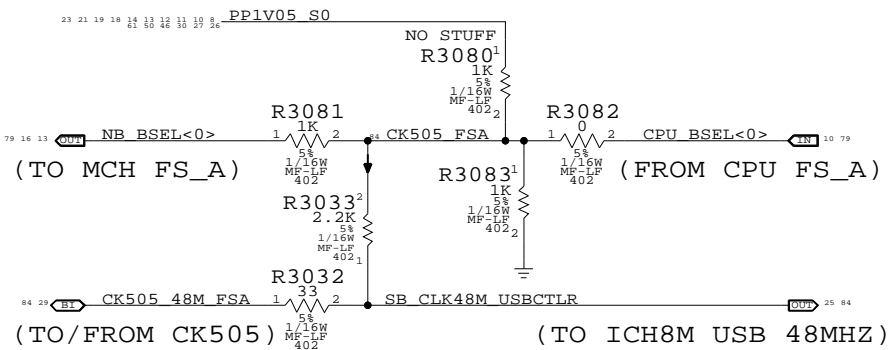
(Note: HOST/SRC/GFX clock termination removed. Silego SL8GLP536 or equiv. support only)

CK505 Configuration Straps

FCT_SEL (GFX clock select)



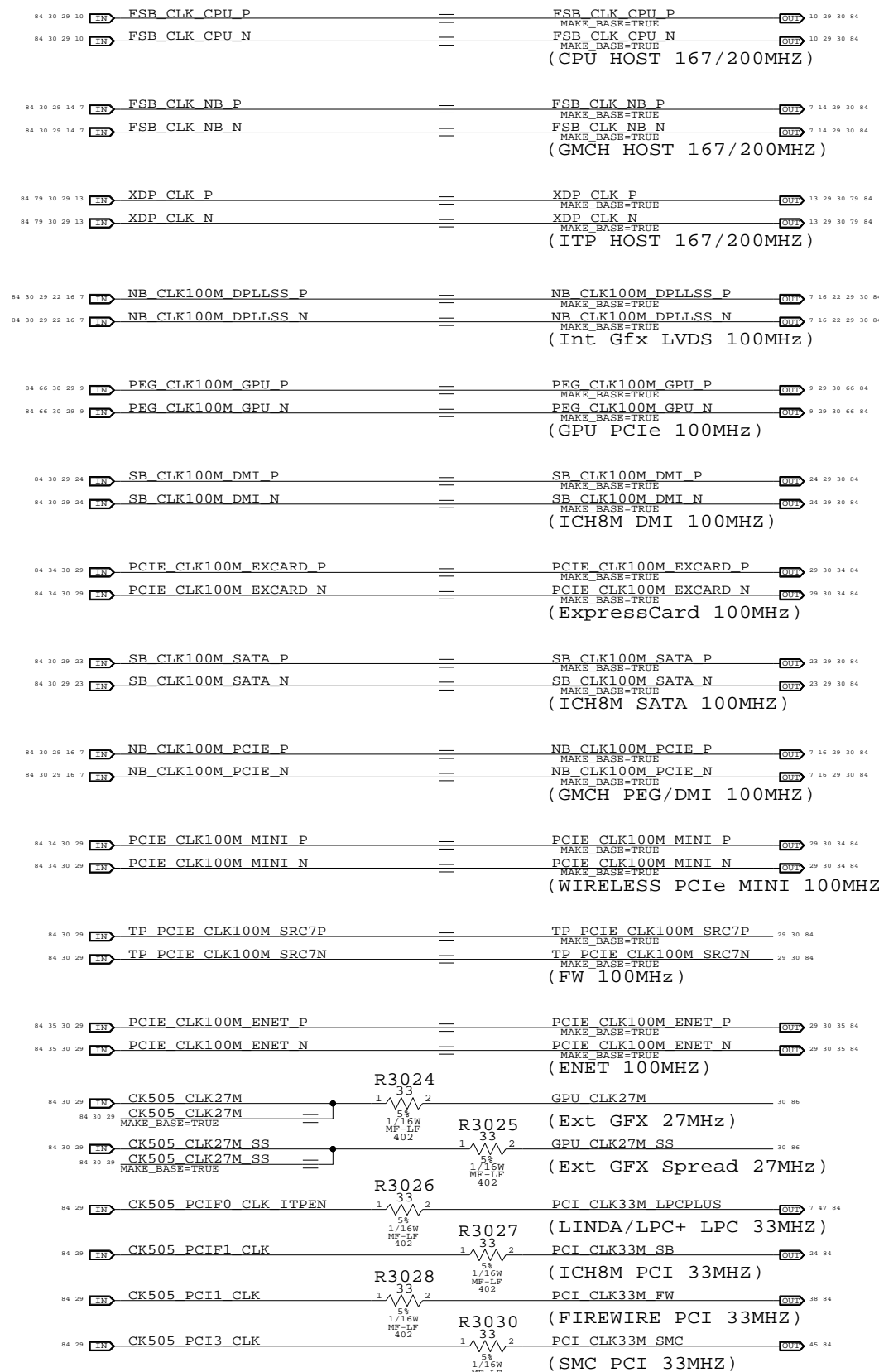
FS_A, FS_B, FS_C (Host clock freq select)



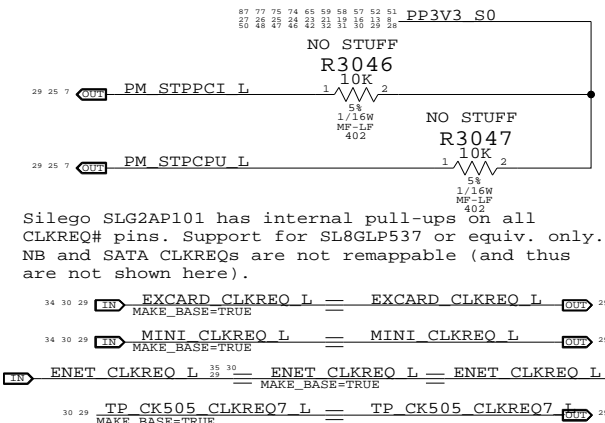
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

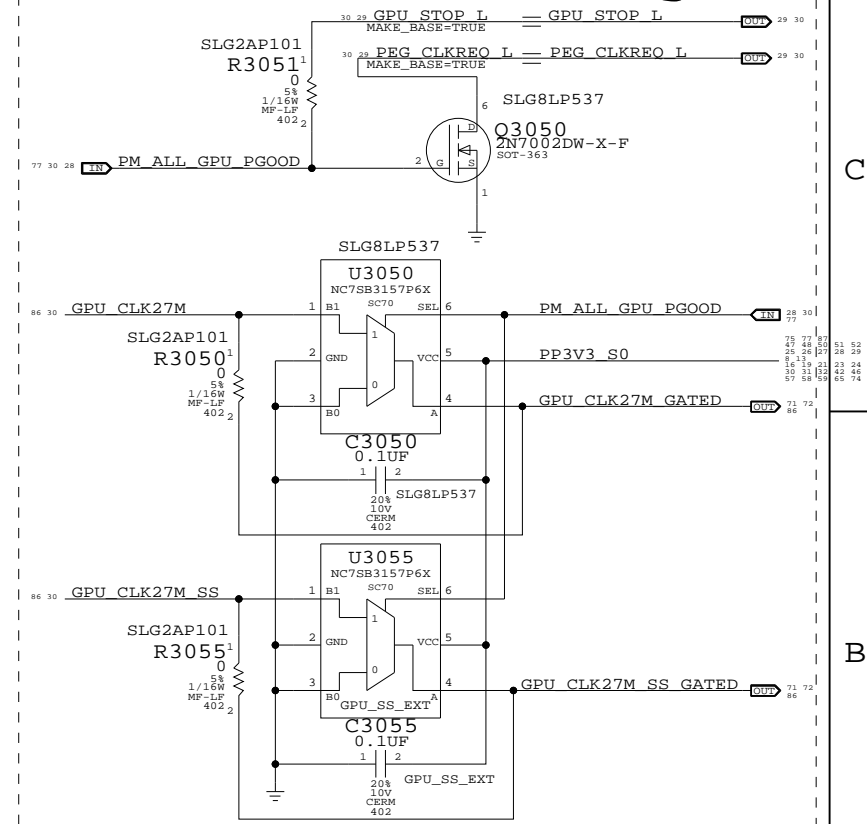


CLKREQ Controls

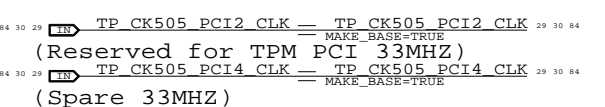


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

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	SCALE NONE	SHEET 30	OF 88

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

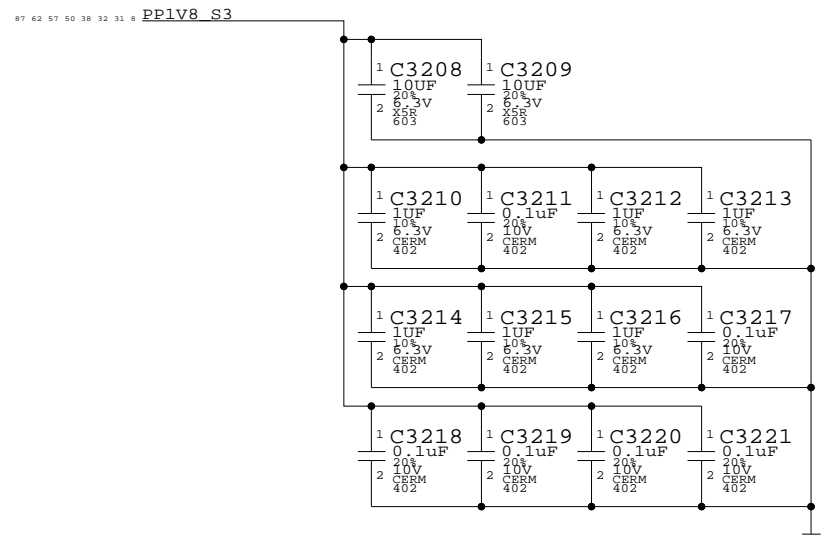
Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps (For return current)

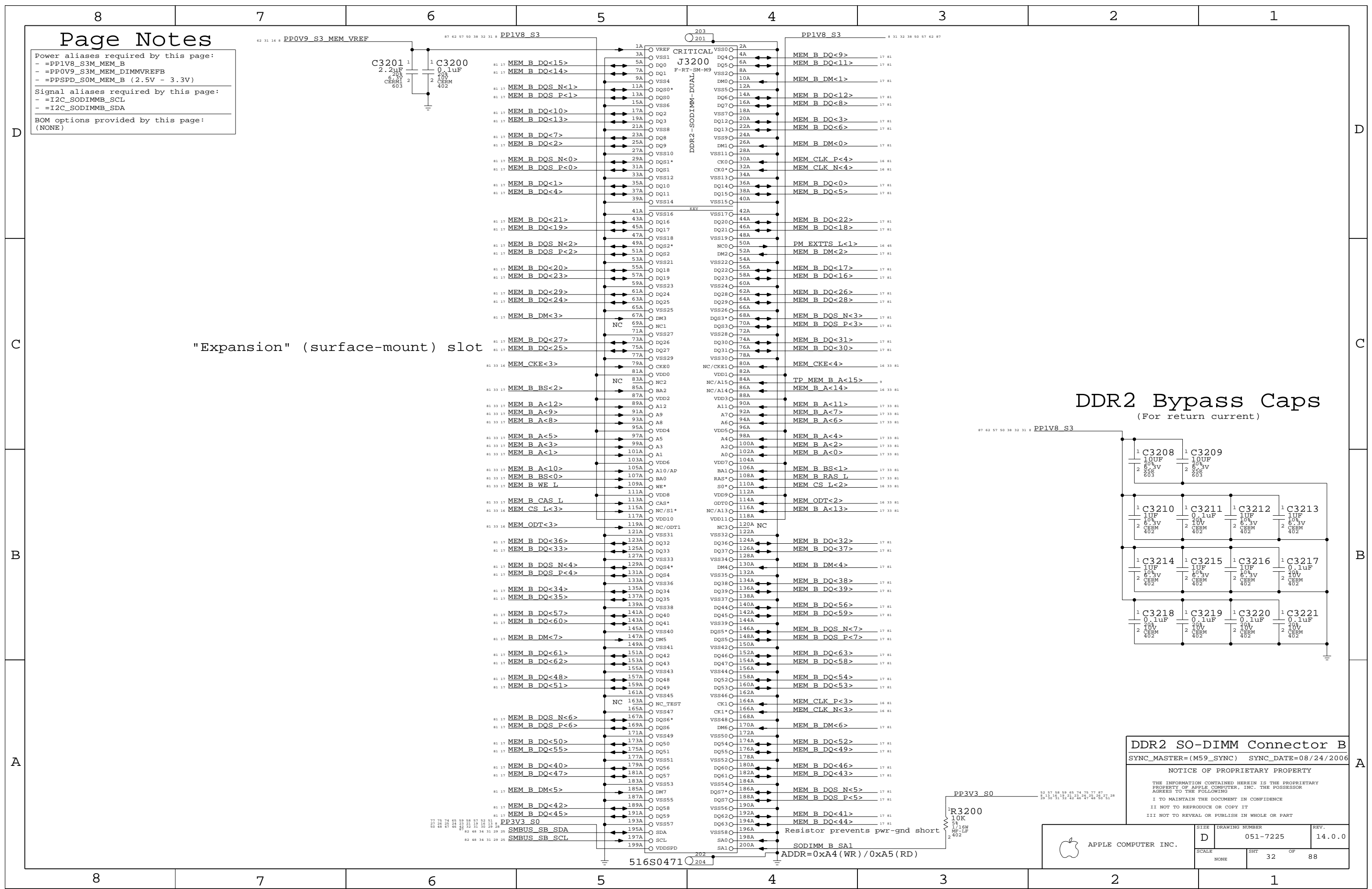


DDR2 SO-DIMM Connector B
SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	32	88	



One cap for each side of every RPAK, one cap for every two discrete resistors
 Ensure CS_L and ODT resistors are close to SO-DIMM connector

D

D

C

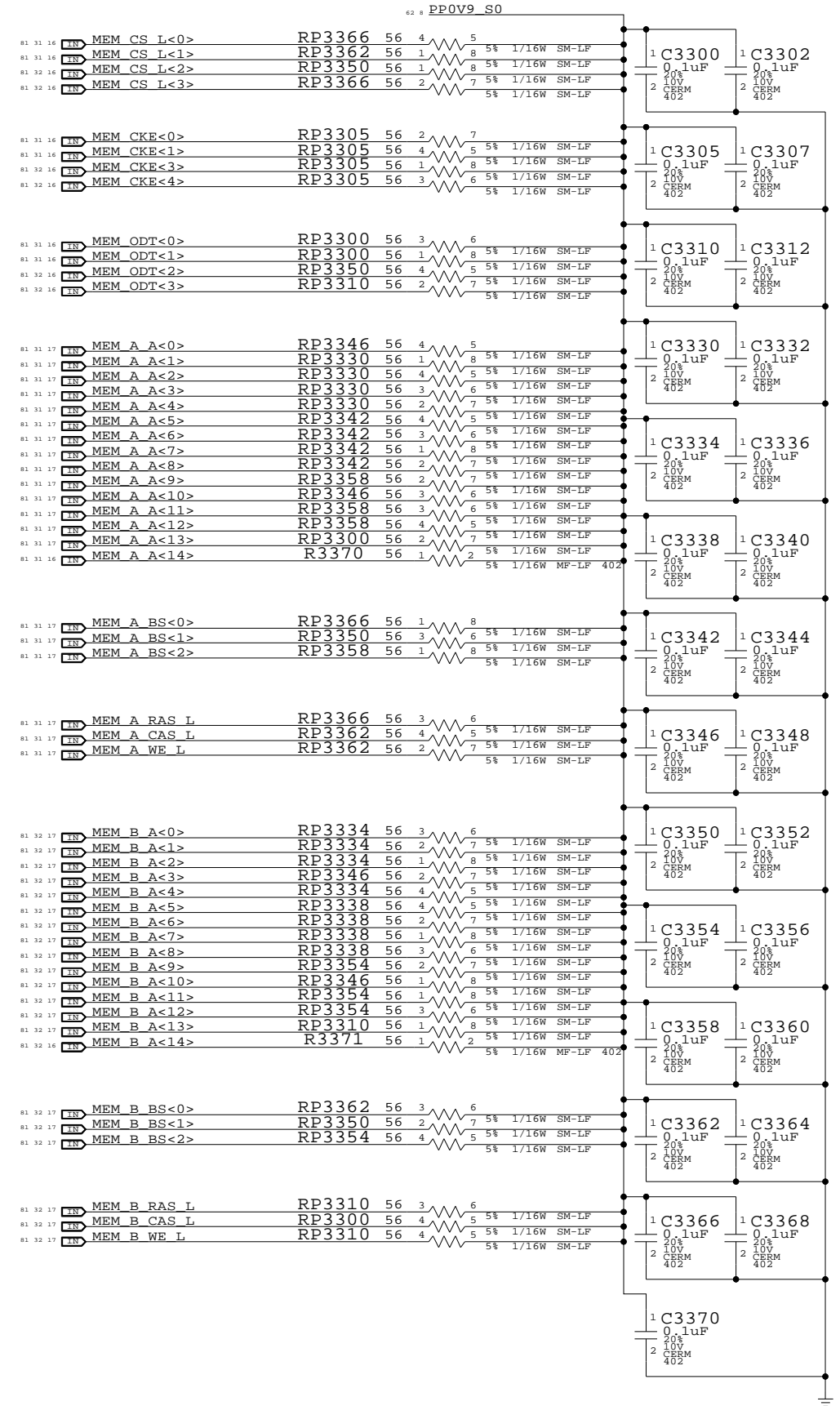
C

B

B

A

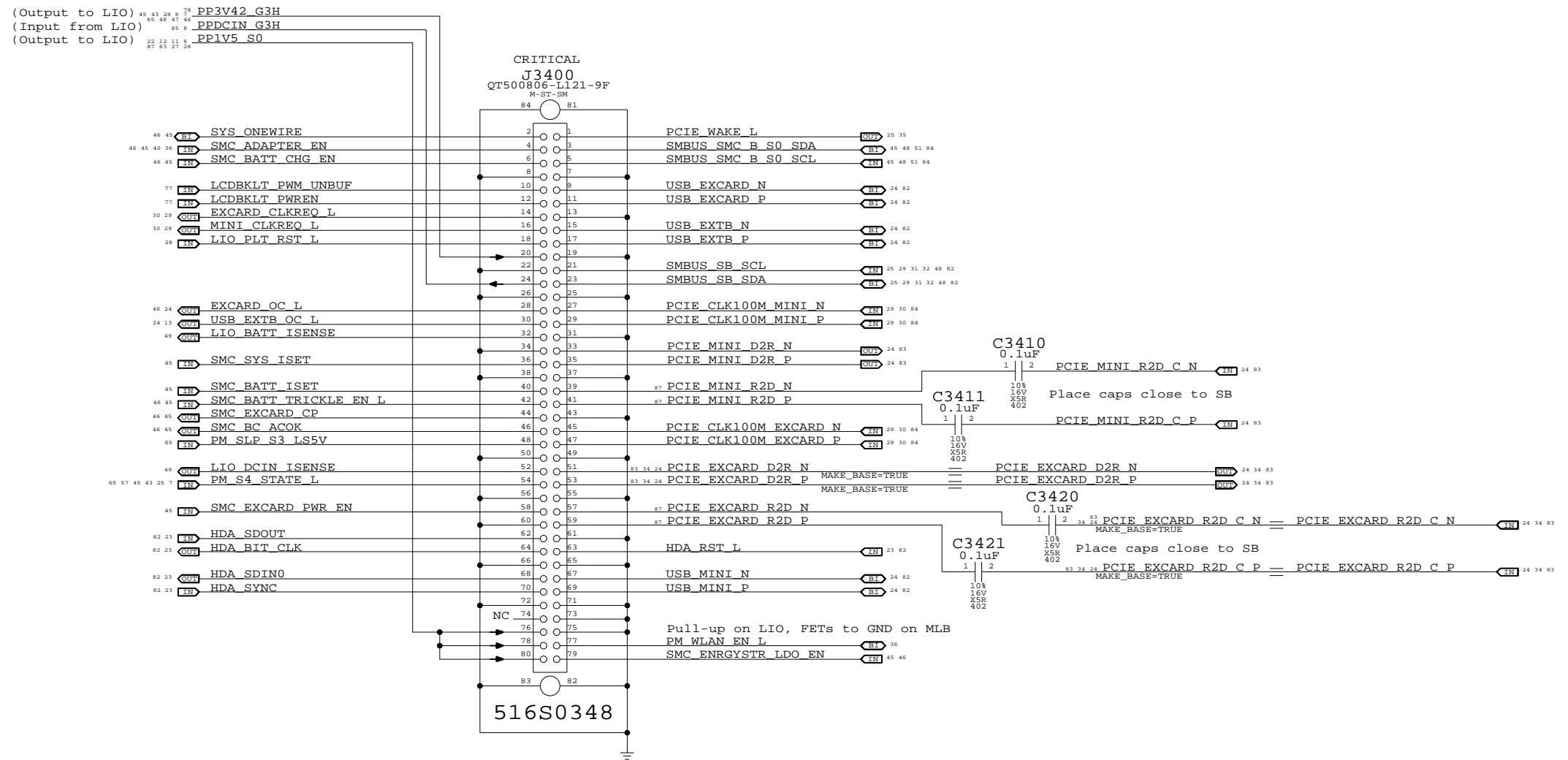
A



Memory Active Termination
 SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	33	88	

Left I/O Board Connector



Left I/O Board Connector
 SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	NONE	SHT	34 OF 88

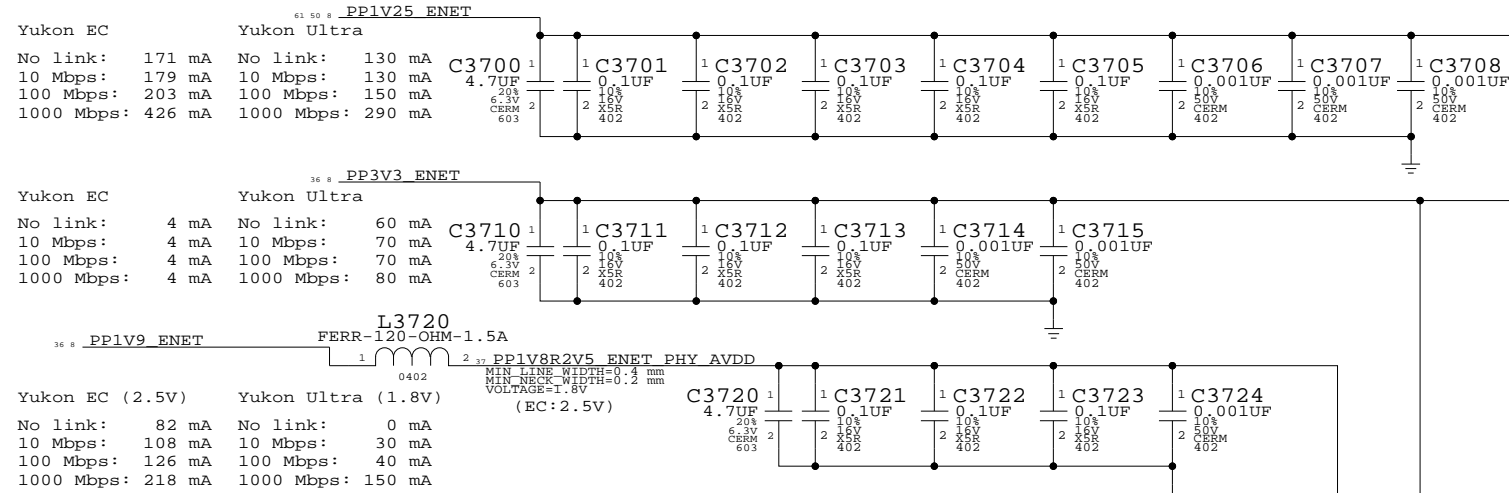
Page Notes

Power aliases required by this page:
 - =PP3V3_ENET_PHY (EC / Ultra)
 - =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
 - =YUKON_EC_PP2V5_ENET (2.5V / GND)
 - =PP1V2_ENET_PHY

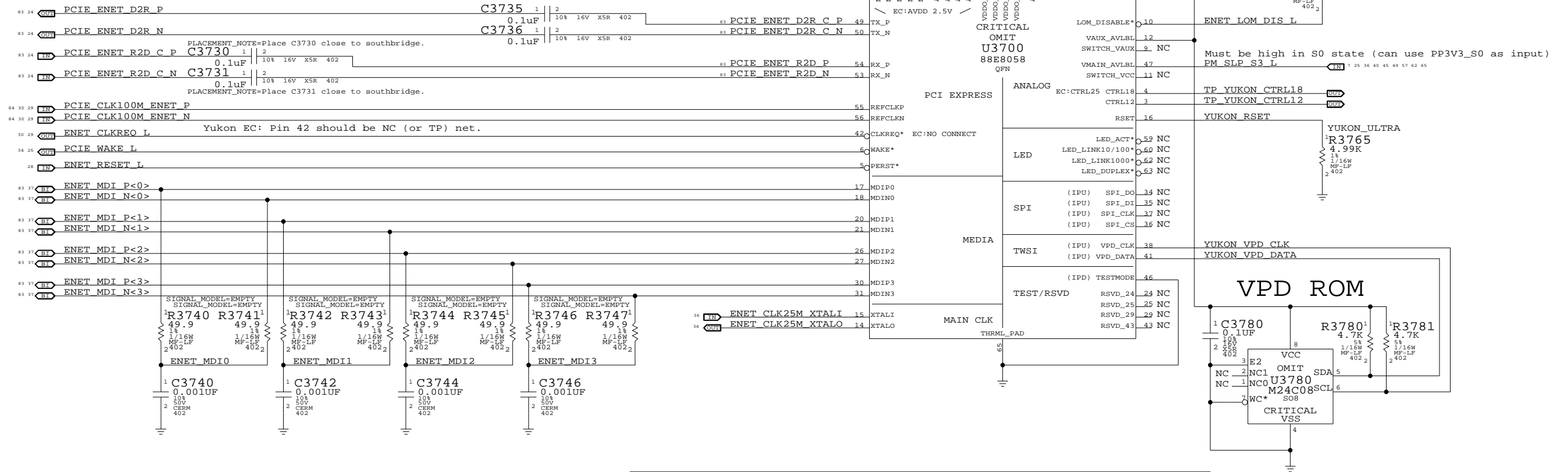
Signal aliases required by this page:
 - =ENET_CLKREQ_L (NC/TP for Yukon EC)
 - =ENET_VMAIN_AVLBLE (See note by pin)

BOM options provided by this page:
 YUKON_EC - Selects Yukon EC RSET value.
 YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



GND
 Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, S08	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, S08	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

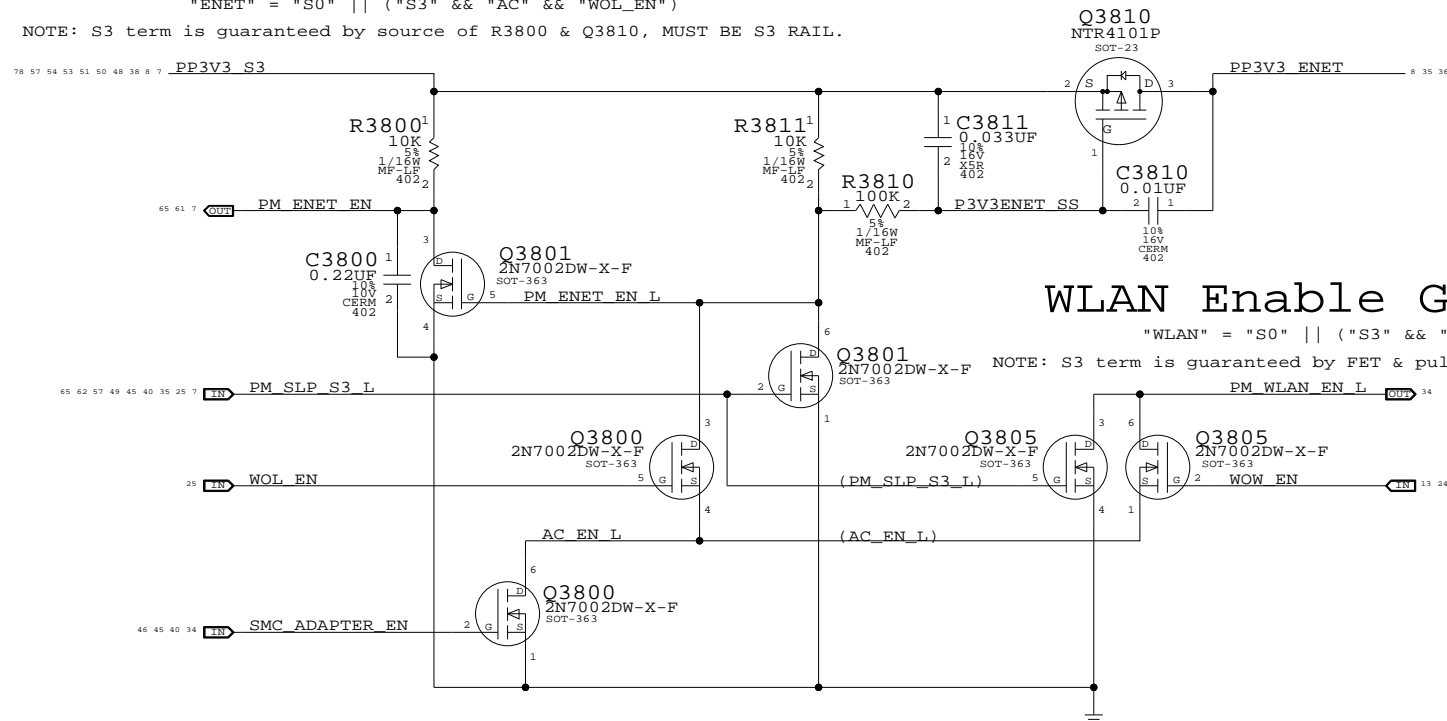
- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)
 SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	35	88	

ENET Enable Generation

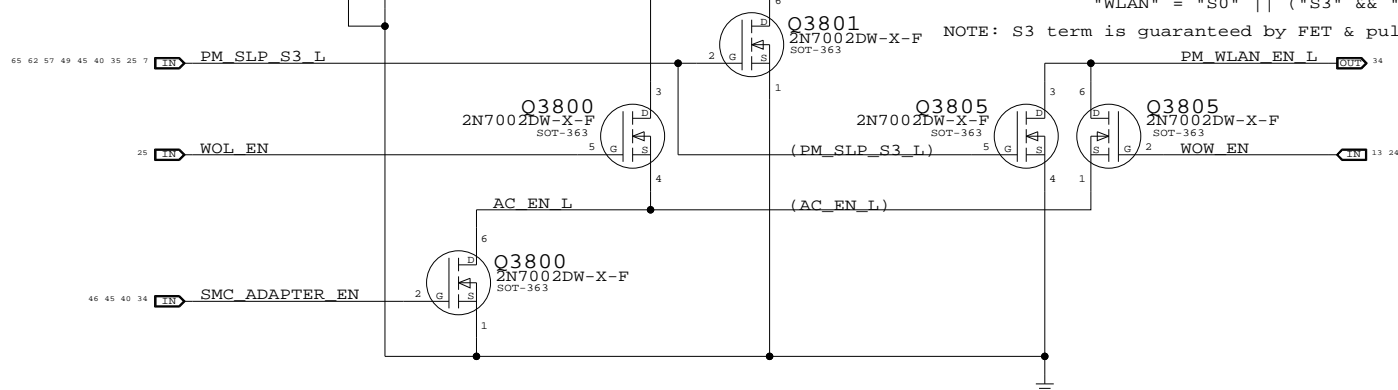
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

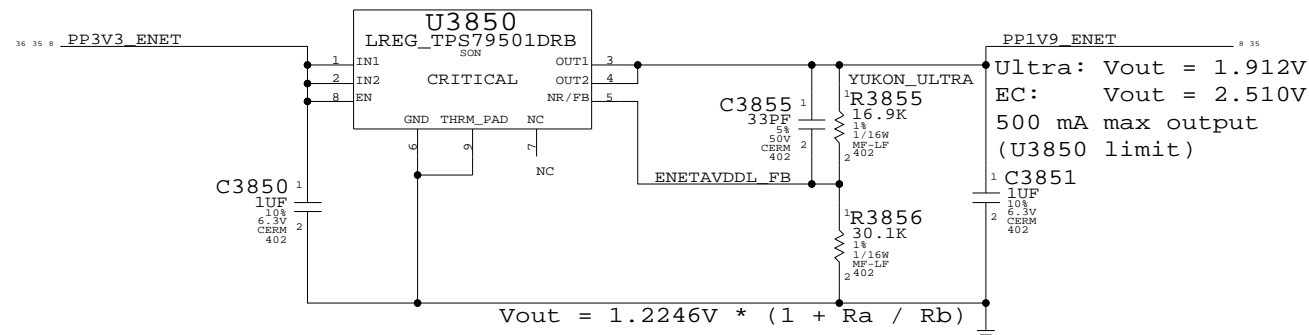
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



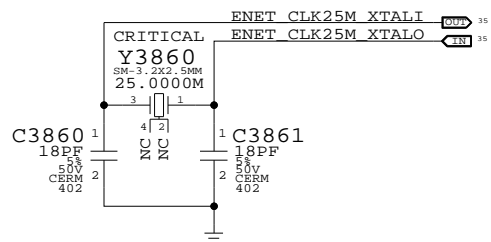
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	36	88	

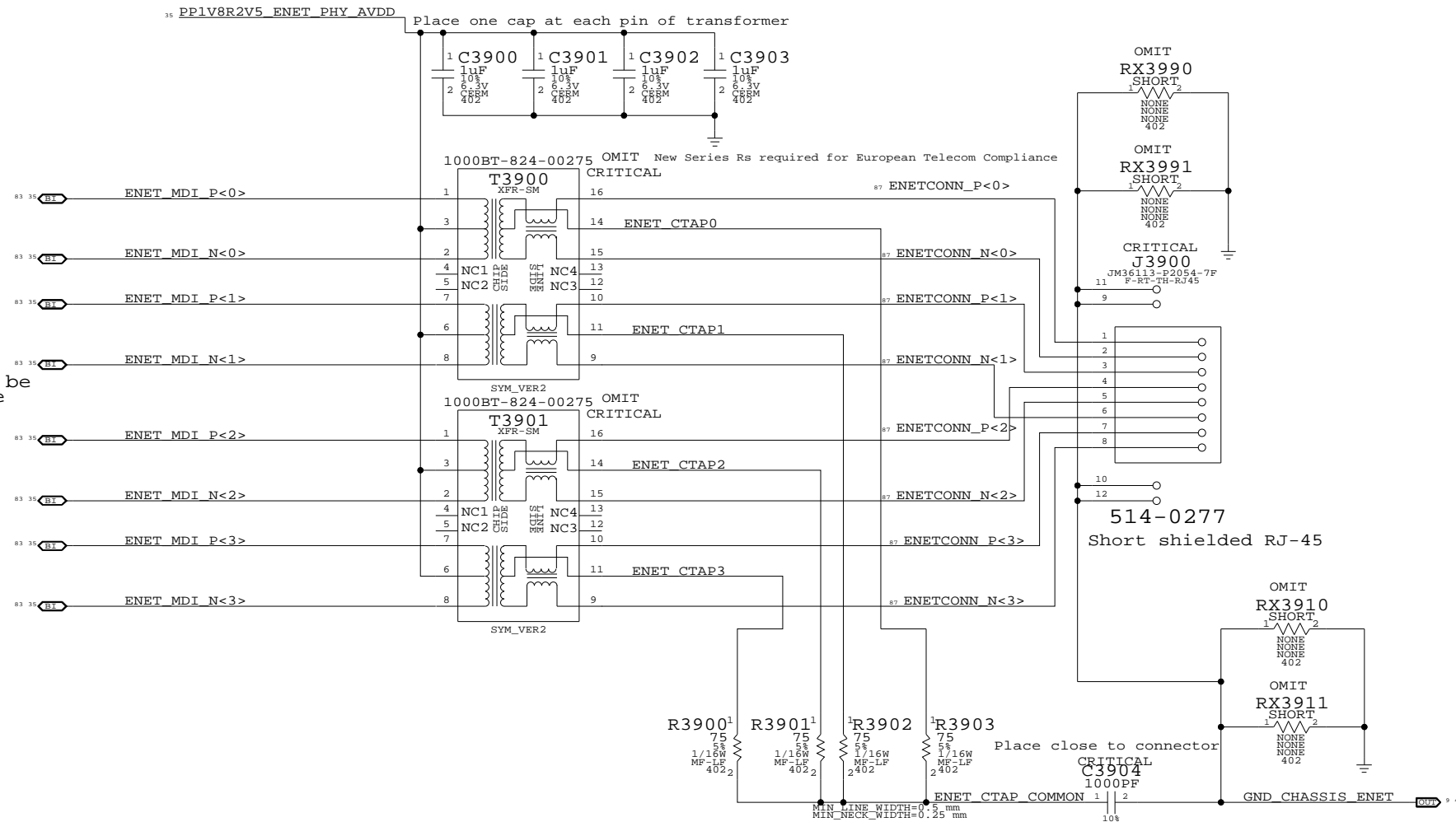
Page Notes

Power aliases required by this page:
 - =GND_CHASSIS_ENET

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

Transformers should be mirrored on opposite sides of the board



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15780030	2	XPR-SMD,HALF-PORT,1000T,16P,SMD,2MM	T3900,T3901	CRITICAL	

Ethernet Connector

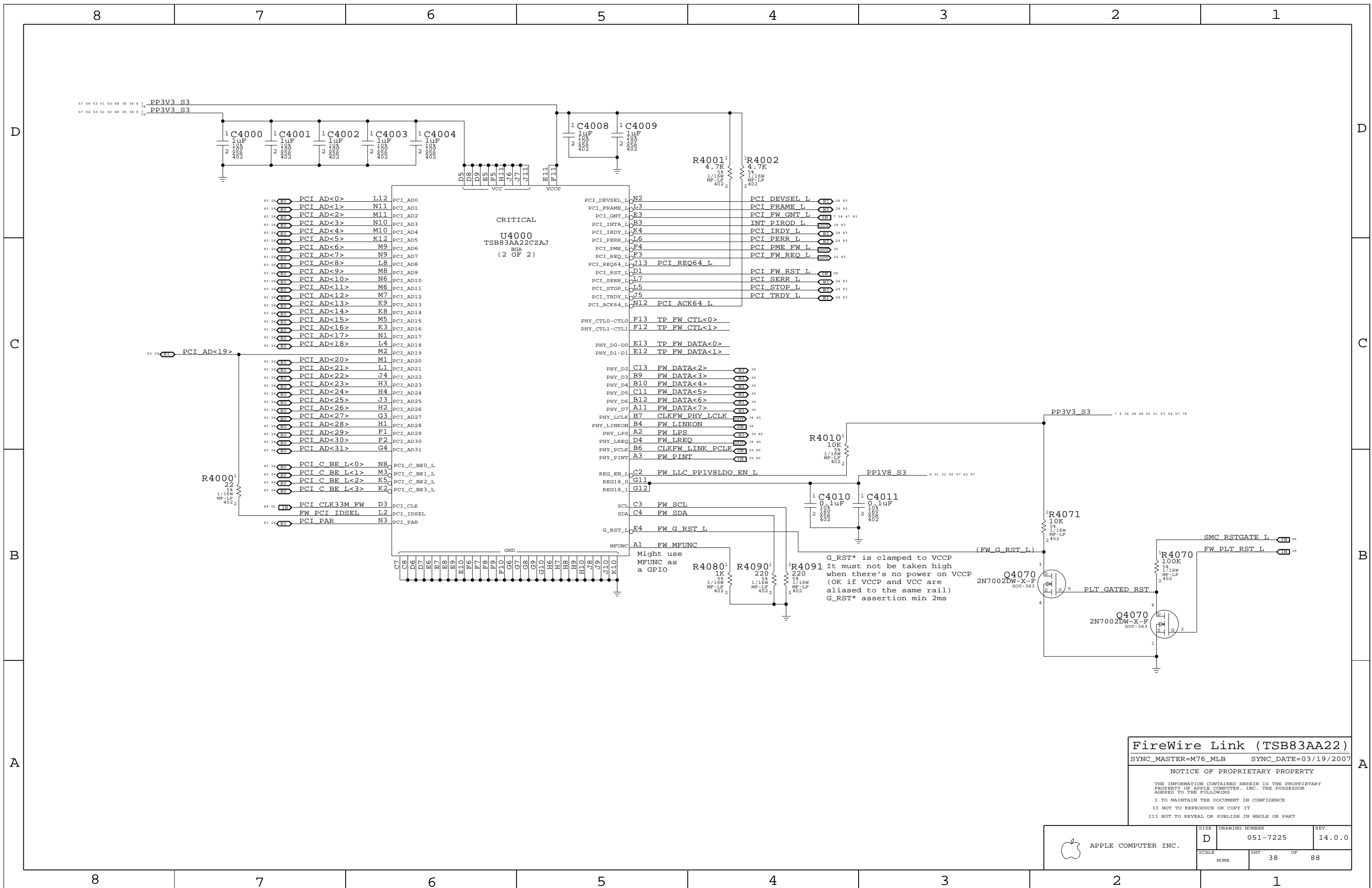
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	37	88	

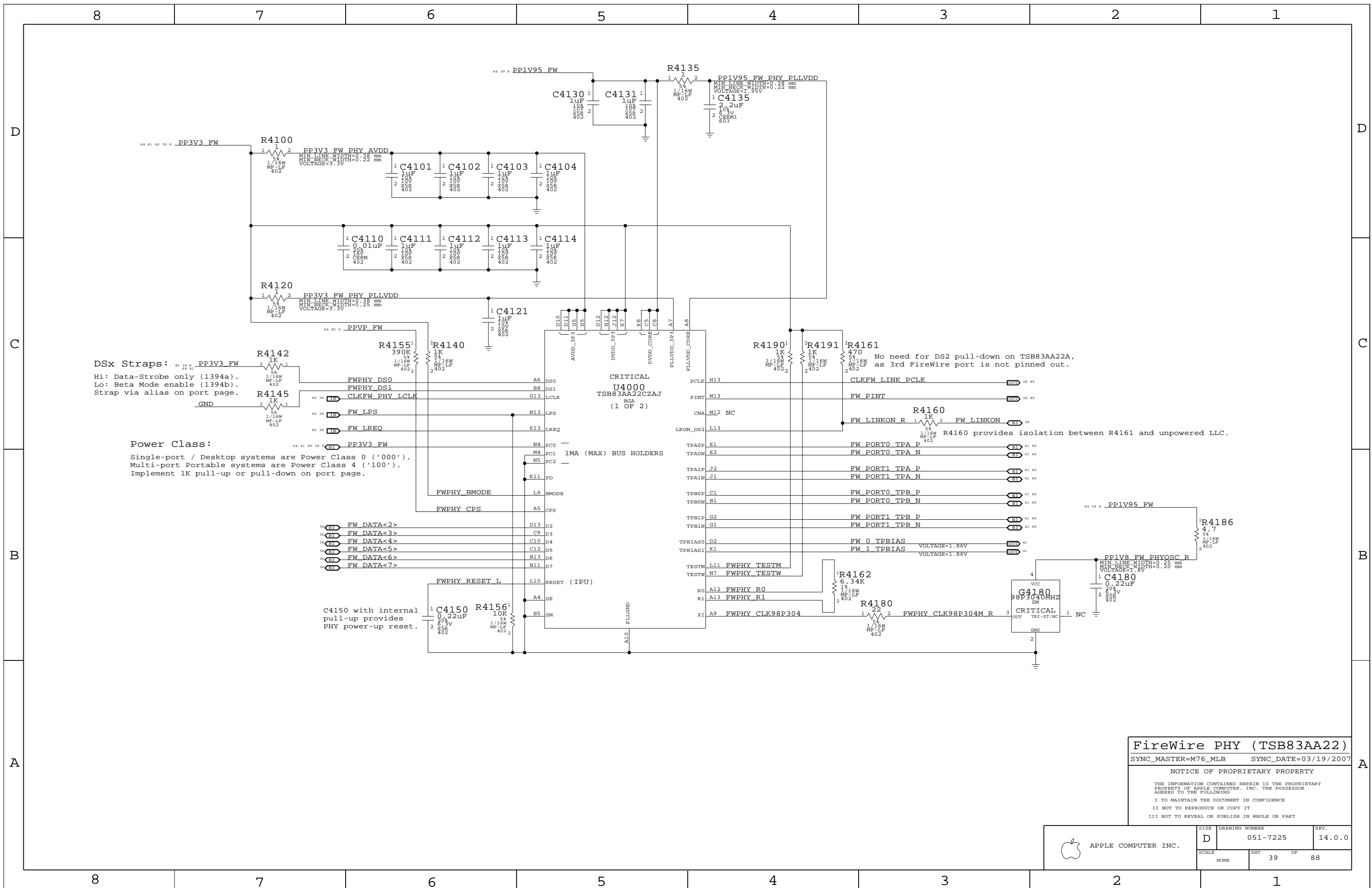


FireWire Link (TSB83AA22)
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHEET 38	OF 88

G_RST* is clamped to VCCP
 It must not be taken high when there's no power on VCCP (OK if VCCP and VCC are aliased to the same rail)
 G_RST* assertion min 2ms



FireWire PHY (TSB83AA22)
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	39	88	

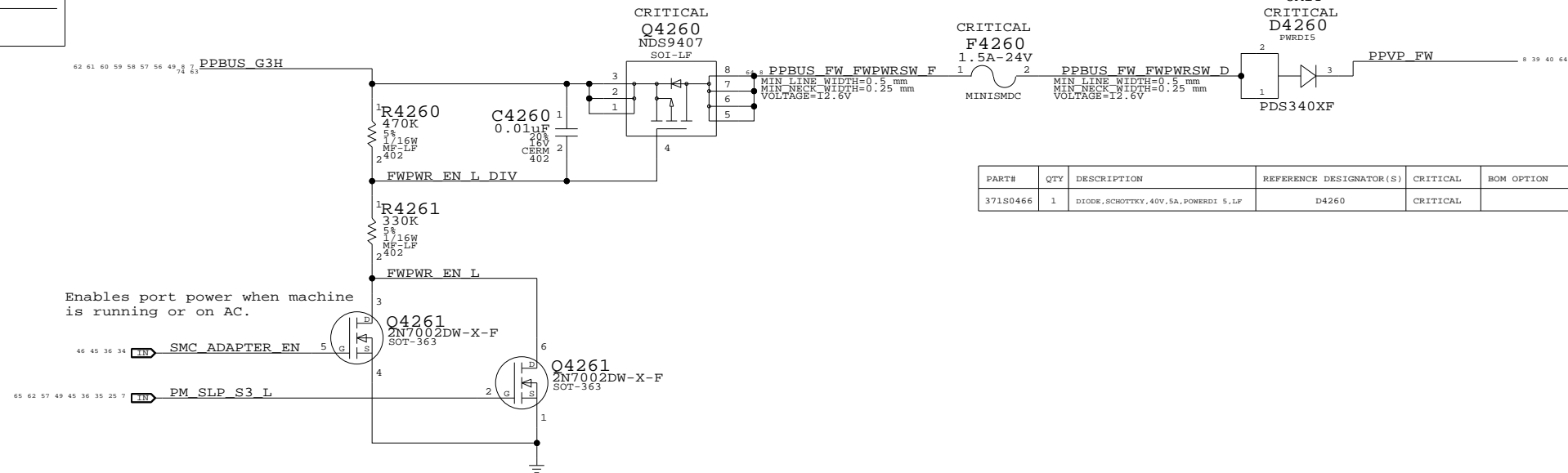
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
 (NONE)

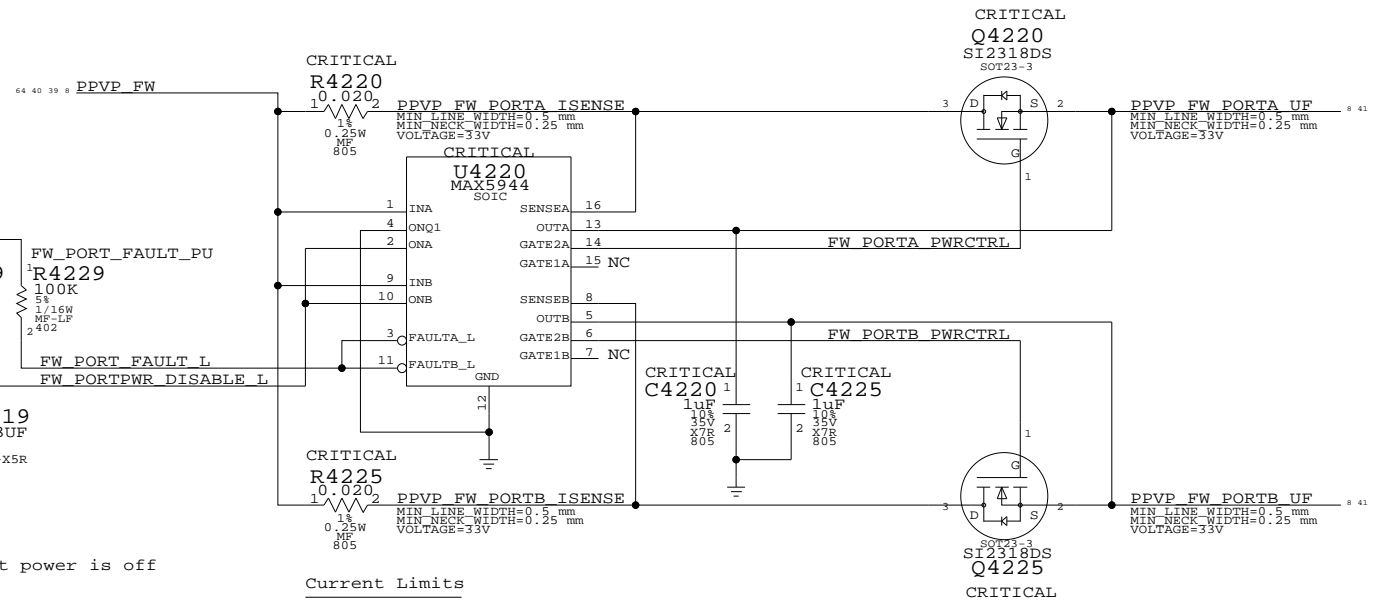
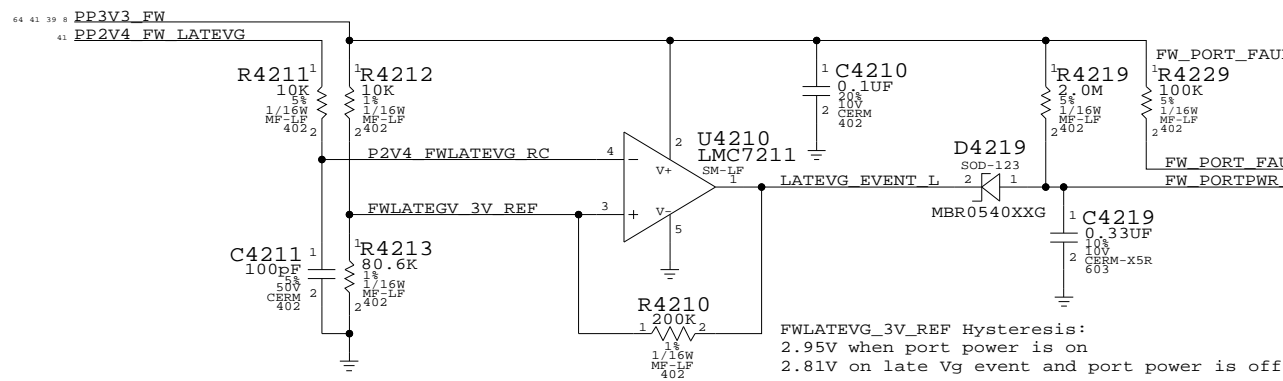
BOM options provided by this page:
 - FW_PORT_FAULT_PU

FireWire Port Power Switch



Current Limit/Active Late-VG Protection

Late-VG Event Detection



Current Limits
 0.020 ohm => 2.4A
 0.025 ohm => 2A
 0.030 ohm => 1.66A (Ideal)
 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	40	88	

Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT0
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG
 - =GND_CHASSIS_FW_PORT0L
 - =GND_CHASSIS_FW_PORT0U
 - =GND_CHASSIS_FW_PORT1
 - =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

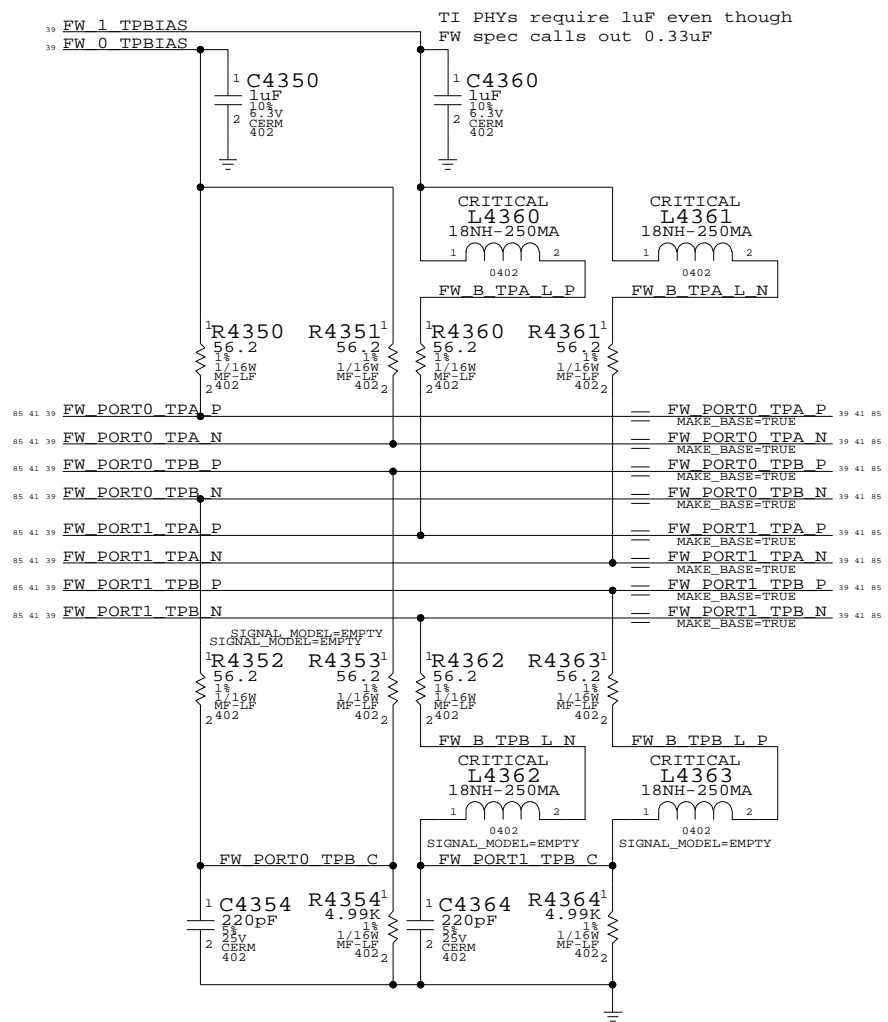
FireWire PHY Config Straps

Configures PHY for:

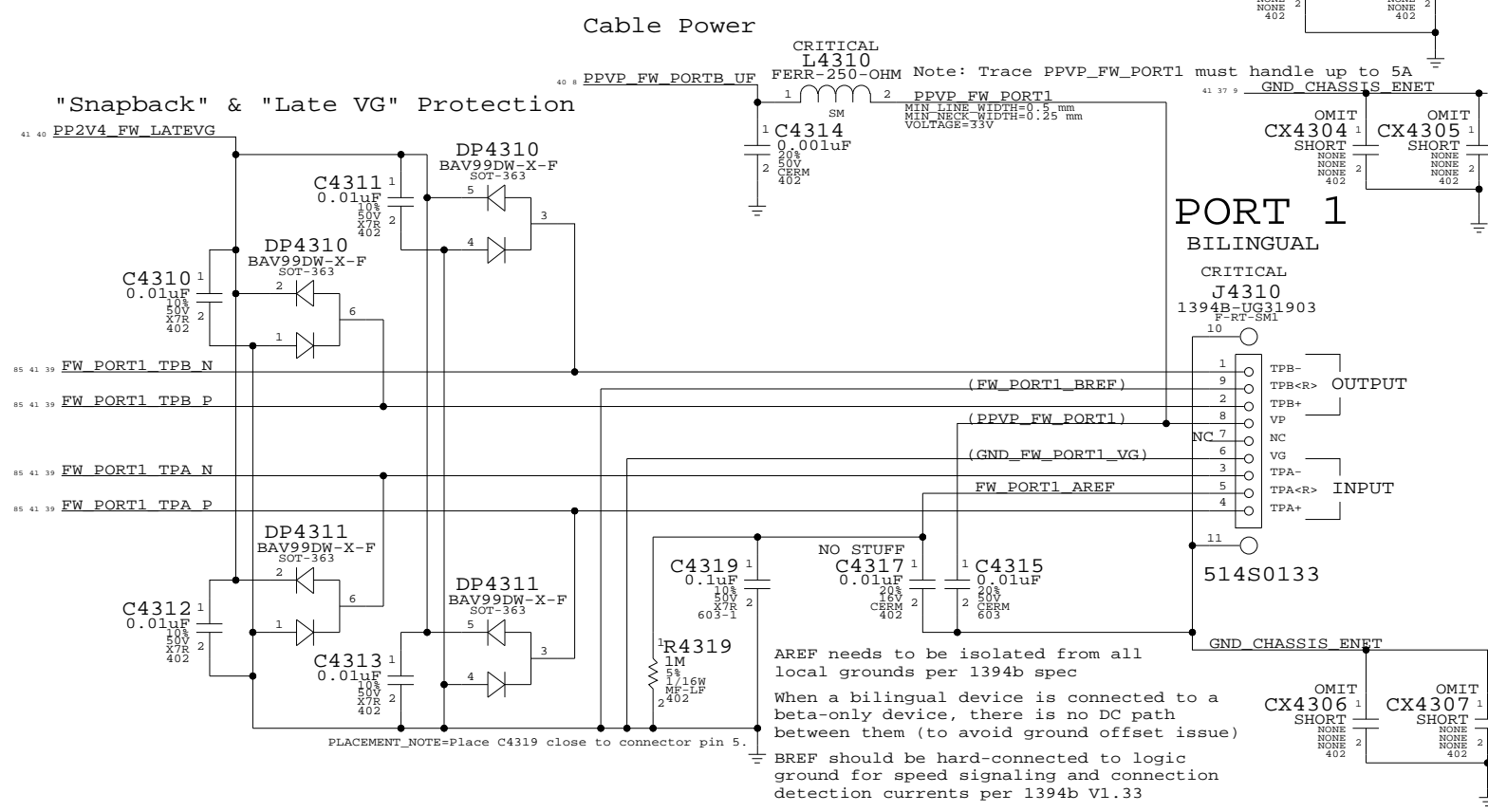
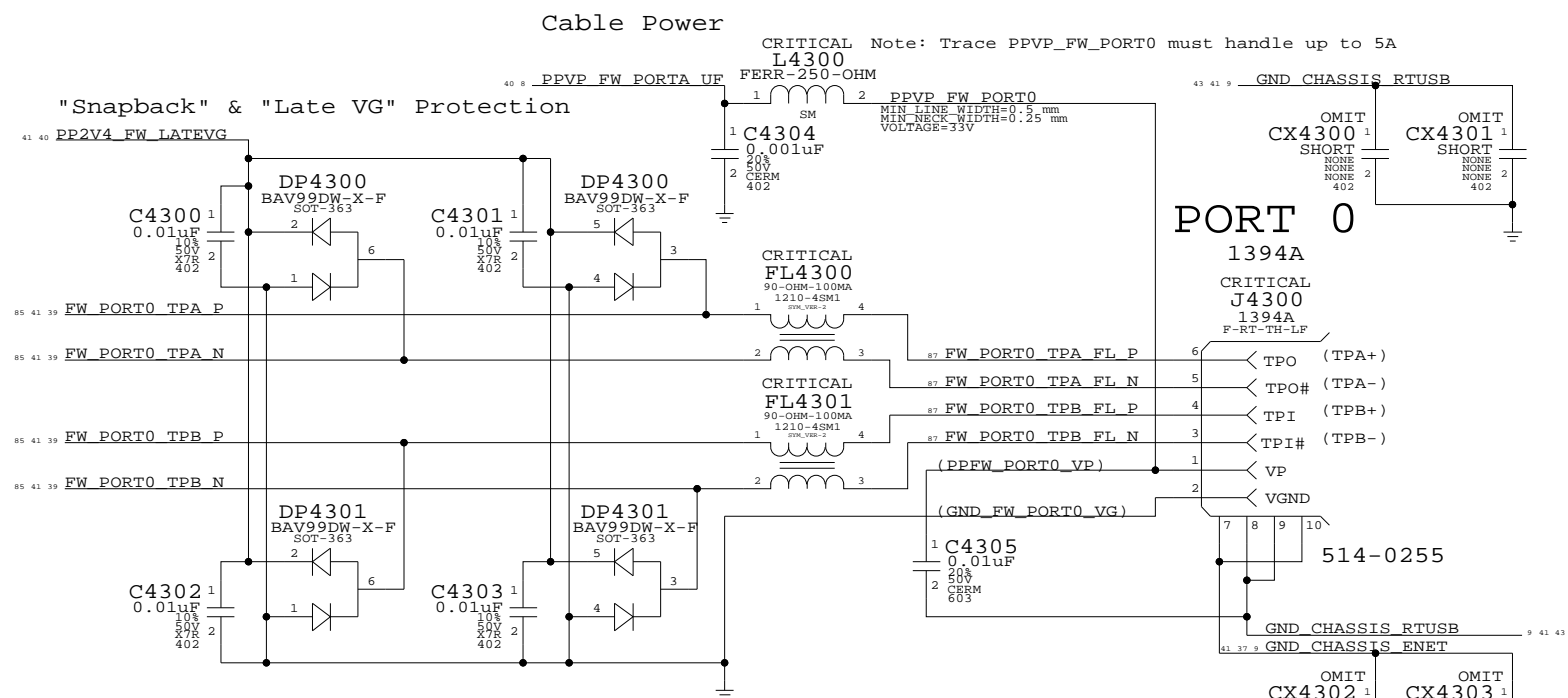
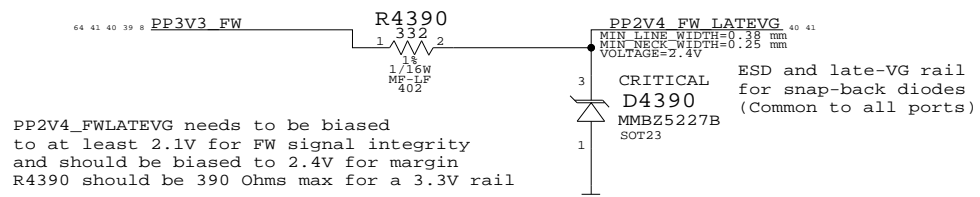
- 2-port Portable Power Class (4)
- Port "0" Data-Strobe only (1394A)
- Port "1" Bilingual (1394B)

Termination

Place close to FireWire PHY



Late-VG Protection Power



FireWire Ports

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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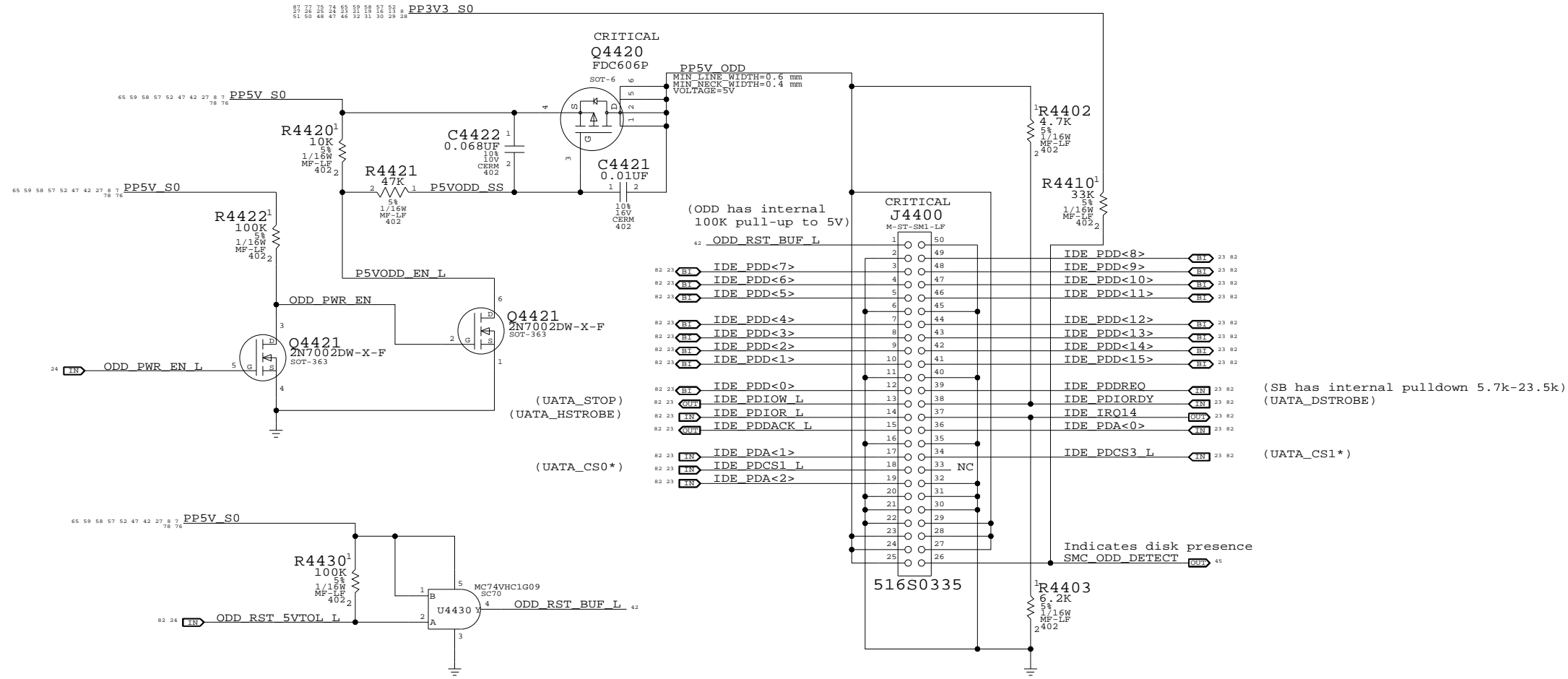
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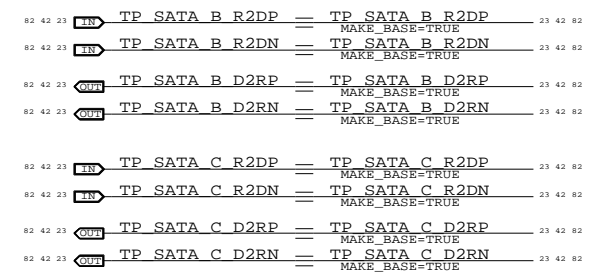
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	REV.
NONE	41	88	

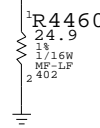
IDE (ODD) Connector



Unused SATA Ports

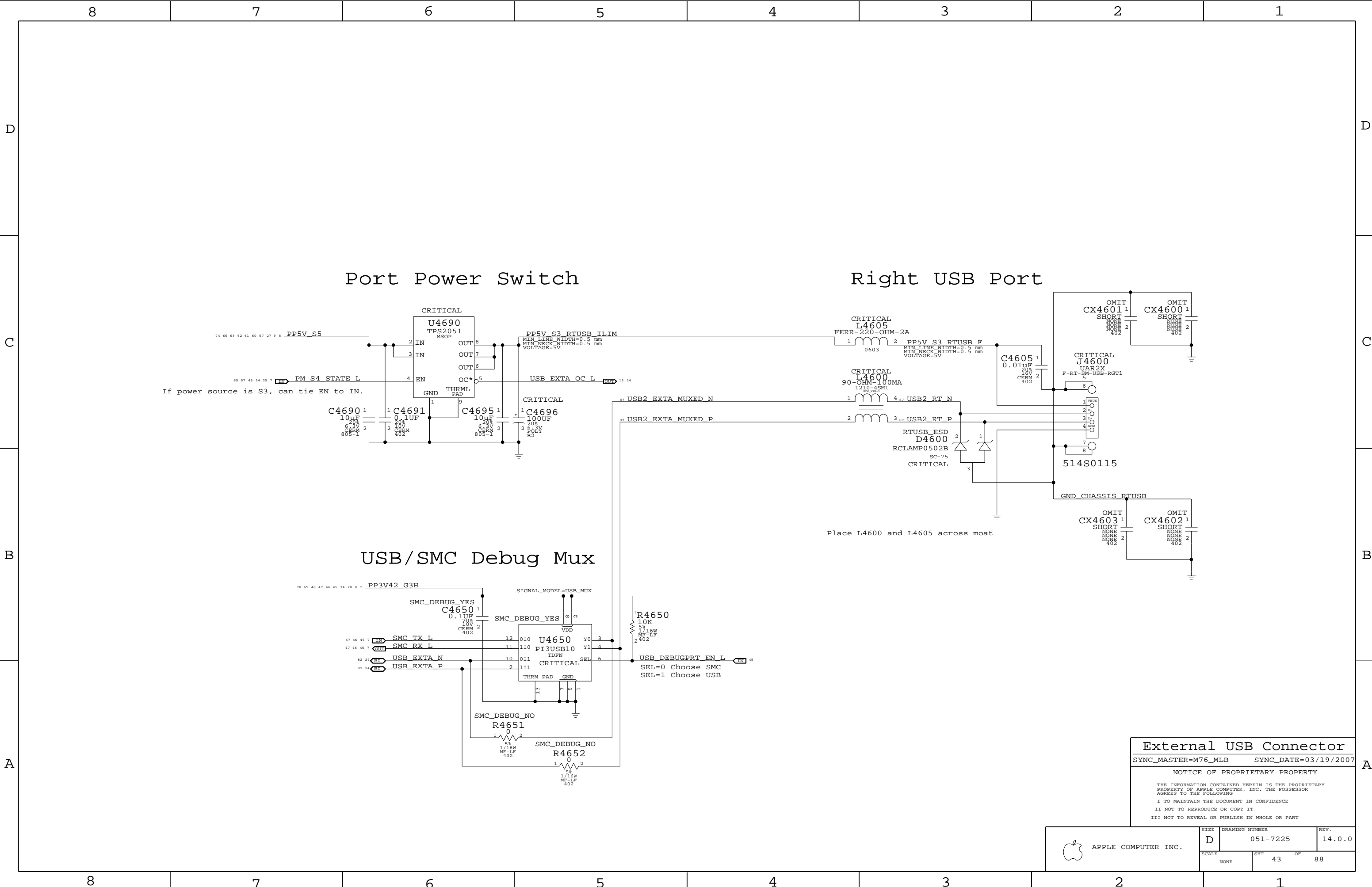


Placement note
Place within 12.7mm
from ball of SB



PATA Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	42	88	



Port Power Switch

Right USB Port

USB/SMC Debug Mux

Place L4600 and L4605 across moat

External USB Connector

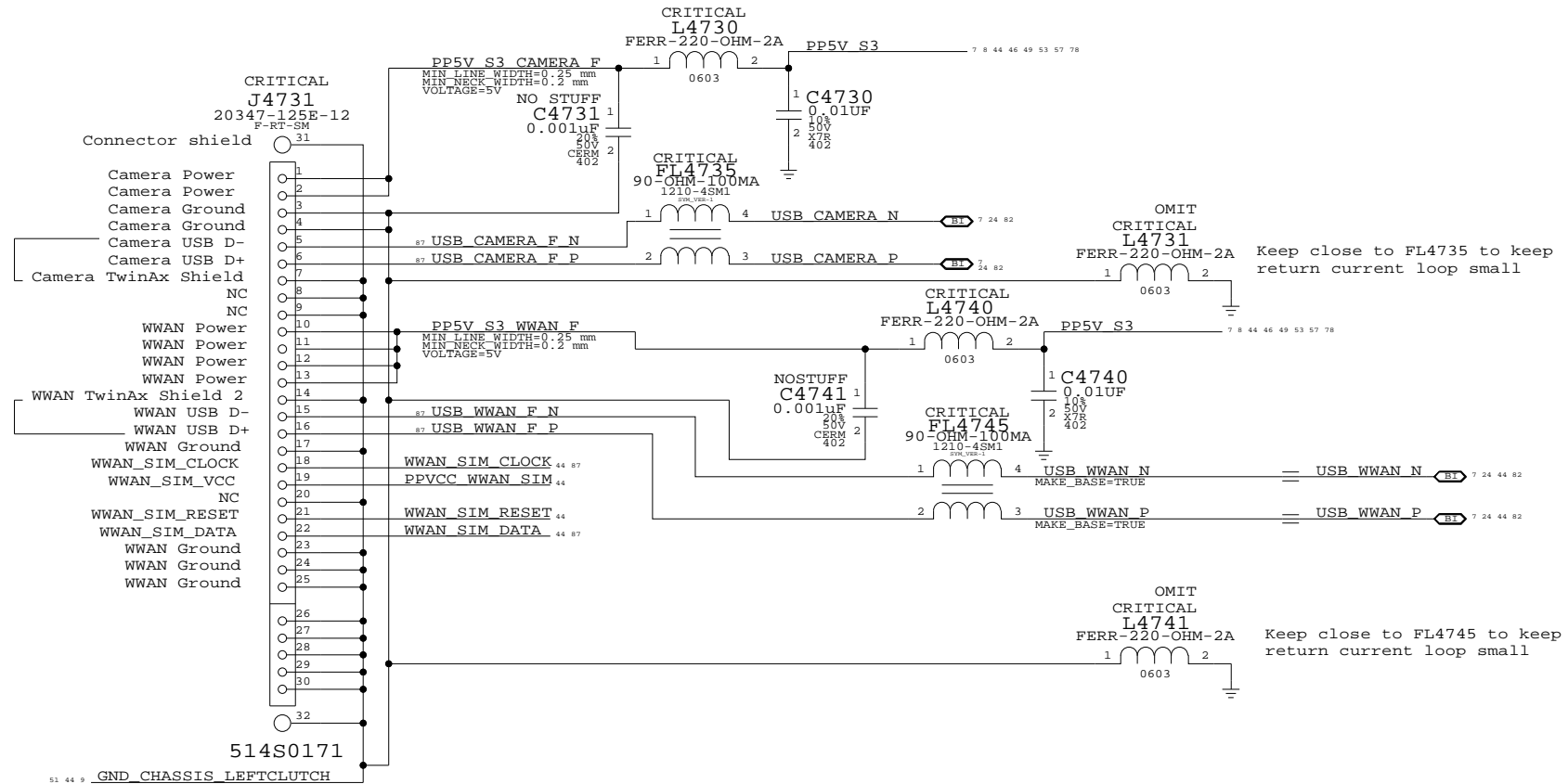
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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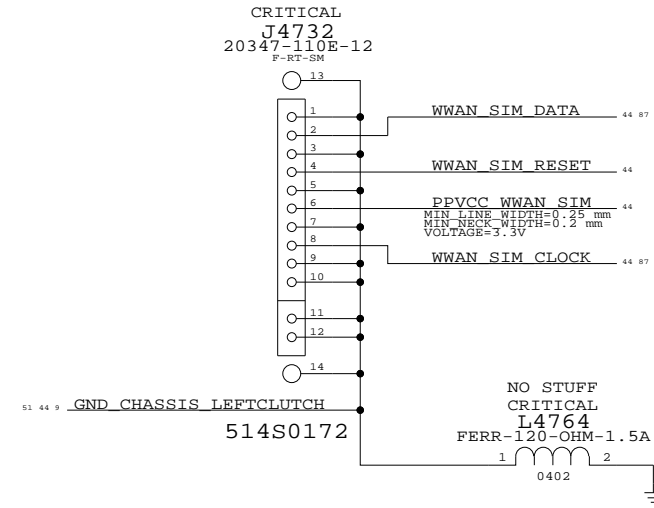
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	43	88	

Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES, MF, 1/10W, 00HM, 5, 0603, SM, LF	L4731, L4741	CRITICAL	

SIM Interconnect

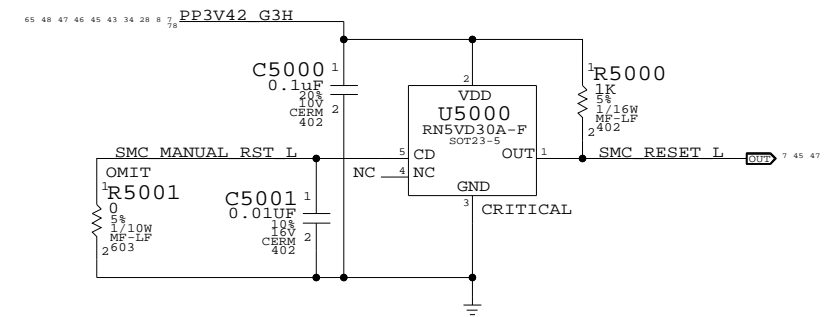


Left Clutch Barrel Interconnect
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

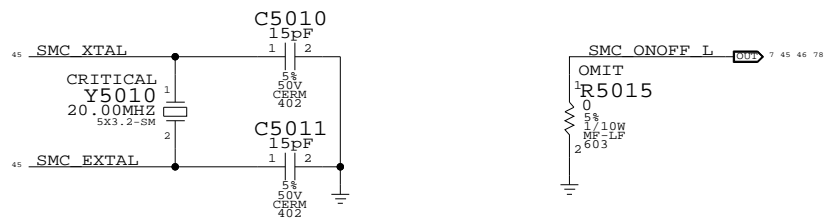
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	44	88	

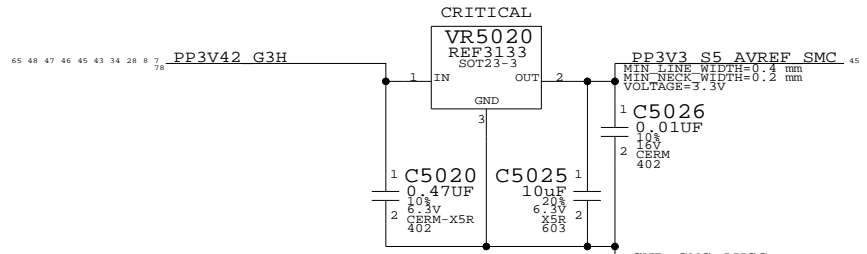
SMC Reset "Button" / Brownout Detect



SMC Crystal Circuit Debug Power "Button"

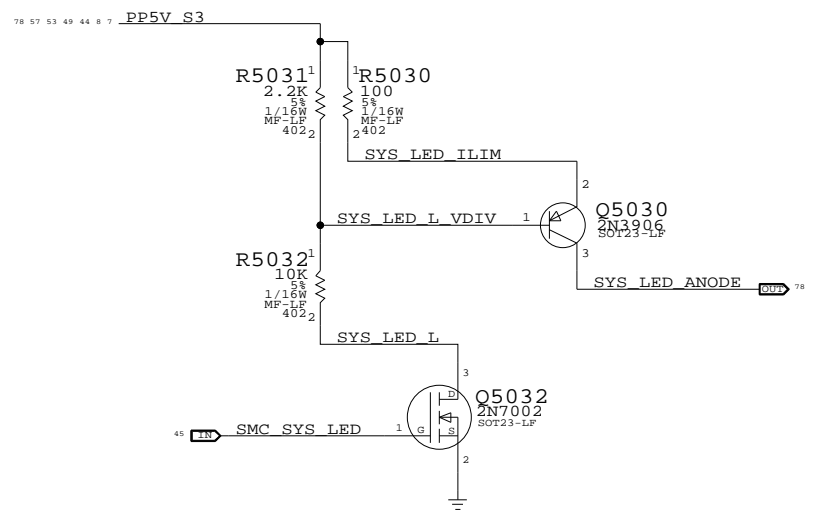


SMC AVREF Supply



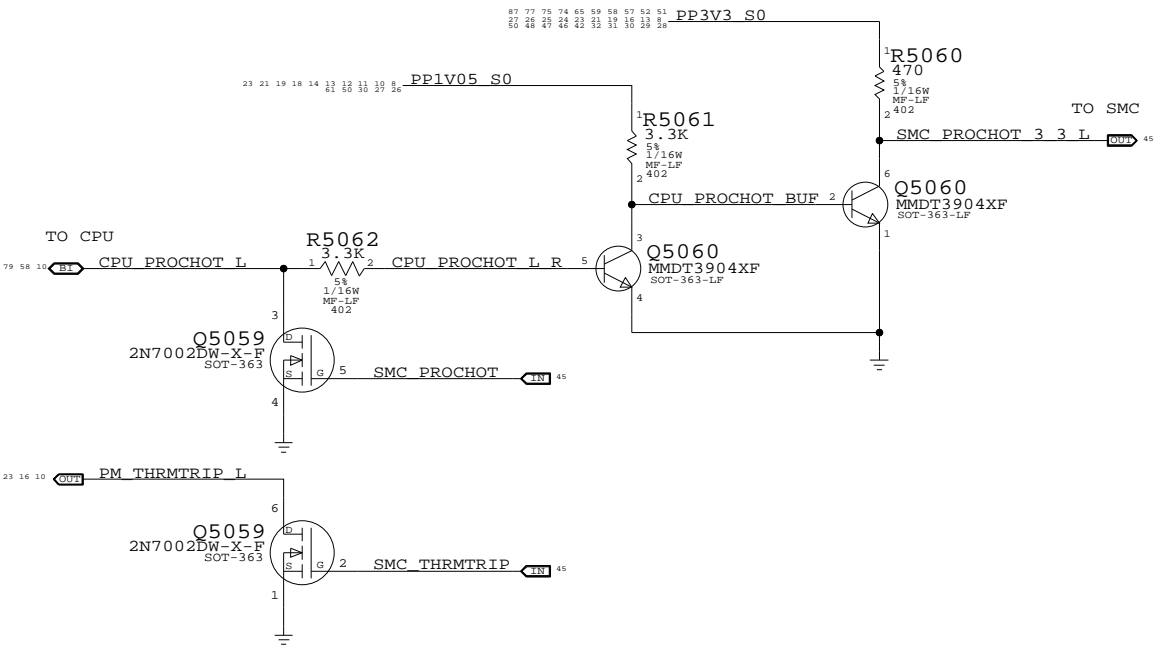
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interail ISL60002-33

System (Sleep) LED Circuit



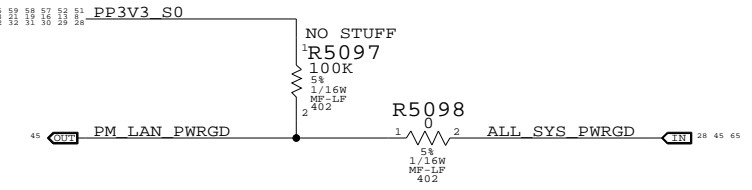
- TP_SMC_FAN_2_CTL == TP_SMC_FAN_2_CTL
- TP_SMC_FAN_2_TACH == TP_SMC_FAN_2_TACH
- TP_SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL
- TP_SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH
- TP_SMC_GFX_OVERTEMP_L == TP_SMC_GFX_OVERTEMP_L
- TP_SMC_GFX_THROTTLE_L == TP_SMC_GFX_THROTTLE_L
- TP_SMC_BATT_VSET == TP_SMC_BATT_VSET
- TP_SMC_SYS_VSET == TP_SMC_SYS_VSET
- TP_SMC_P14 == TP_SMC_P14
- TP_SMC_P20 == TP_SMC_P20
- TP_SMC_P21 == TP_SMC_P21
- TP_SMC_P22 == TP_SMC_P22
- TP_SMC_P23 == TP_SMC_P23
- TP_SMC_P26 == TP_SMC_P26
- TP_SMC_P27 == TP_SMC_P27
- TP_SMC_P43 == TP_SMC_P43
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- TP_SMC_P46 == TP_SMC_P46
- TP_SMC_P62 == TP_SMC_P62
- TP_SMC_P63 == TP_SMC_P63
- TP_SMC_P64 == TP_SMC_P64
- TP_SMC_P81 == TP_SMC_P81
- TP_SMC_PFO == TP_SMC_PFO
- TP_SMC_PF1 == TP_SMC_PF1

SMC FSB to 3.3V Level Shifting

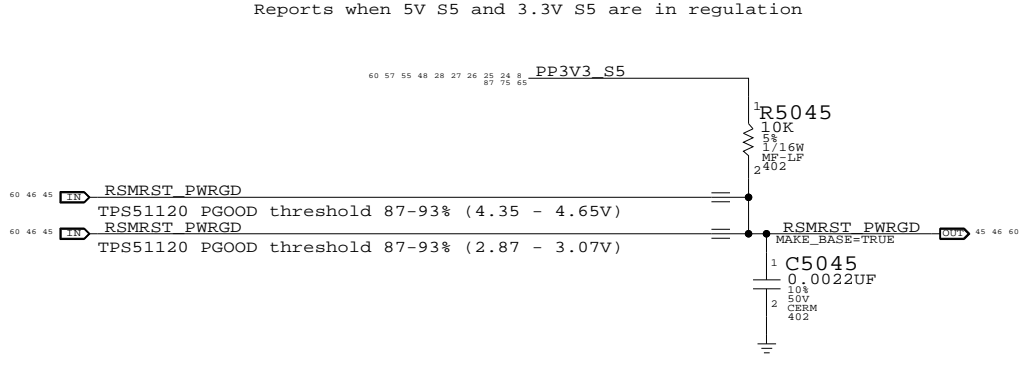


- SMC_EXCARD_OC_L == EXCARD_OC_L
- SUS_CLK_SB == SUS_CLK_SB
- SMC_ENRGYSTR_LDO_EN == SMC_ENRGYSTR_LDO_EN

LAN PWRGD Circuit



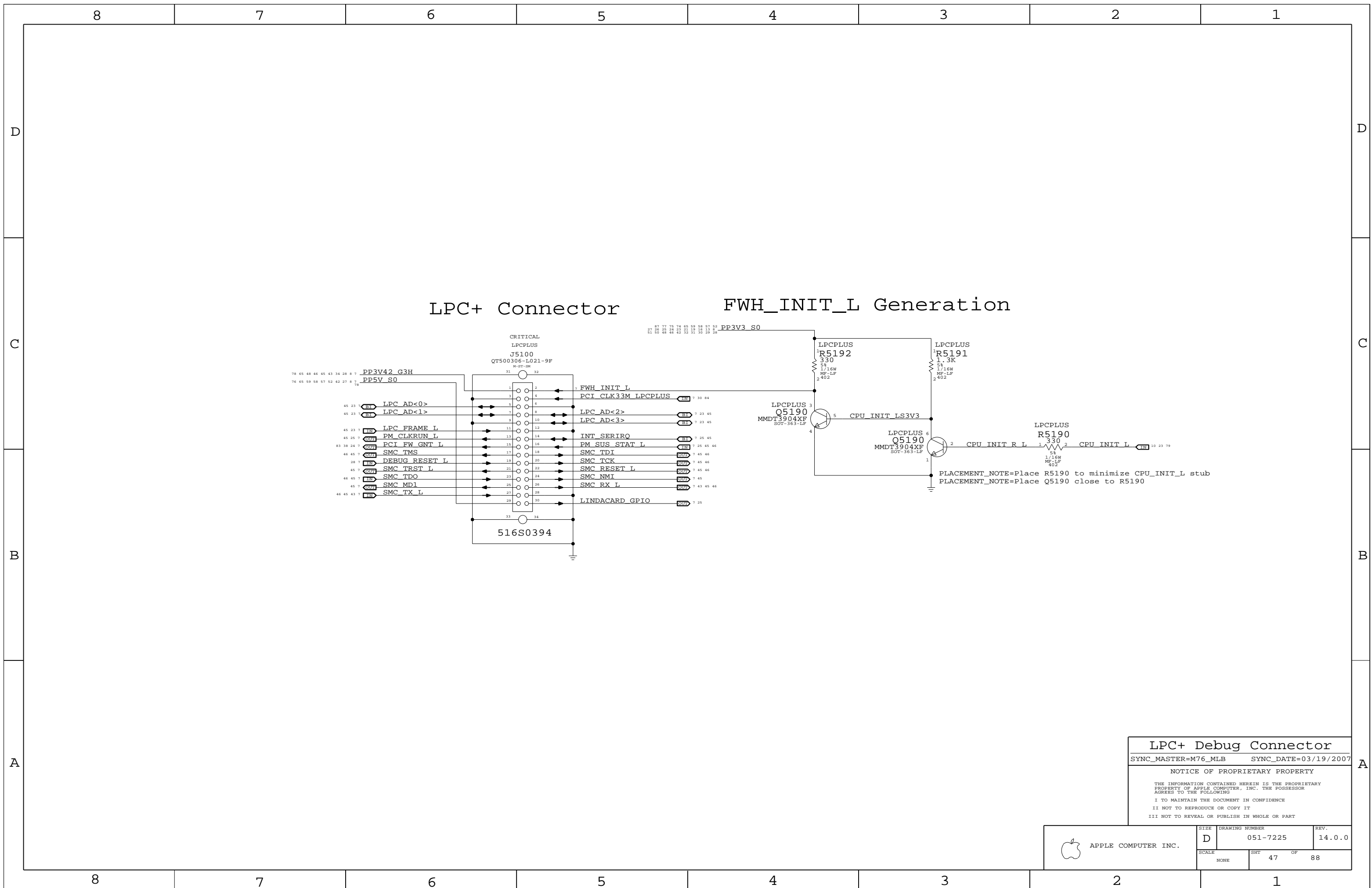
S5 Rail PWRGD Circuit



- SMC_PA0 == R5091 100K
- SMC_PA1 == R5092 100K
- SMC_PB0 == R5093 100K
- SMC_ONOFF_L == R5070 10K
- SMC_LID == R5071 100K
- SMC_FWE == R5072 10K
- SMC_TX_L == R5073 10K
- SMC_RX_L == R5074 100K
- SMC_BS_ALRT_L == R5076 100K
- SMC_TMS == R5077 10K
- SMC_TDO == R5078 10K
- SMC_TDI == R5079 10K
- SMC_TCK == R5080 10K
- SMC_P67 == R5094 10K
- SMC_P63 == R5081 10K
- SMC_P60 == R5096 10K
- SMC_PH4 == R5082 10K
- SMC_BATT_TRICKLE_EN_L == R5083 10K
- SMC_BATT_CHG_EN == R5084 10K
- SMC_ADAPTER_EN == R5085 10K
- SMC_CASE_OPEN == R5086 10K
- SMC_BC_ACOK == R5087 470K
- SMC_EXCARD_CP == R5088 10K
- PM_SUS_STAT_L == R5089 100K
- PM_SLP_S5_L == R5090 100K

SMC Support
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	46	88	



LPC+ Connector

FWH_INIT_L Generation

LPC+ Debug Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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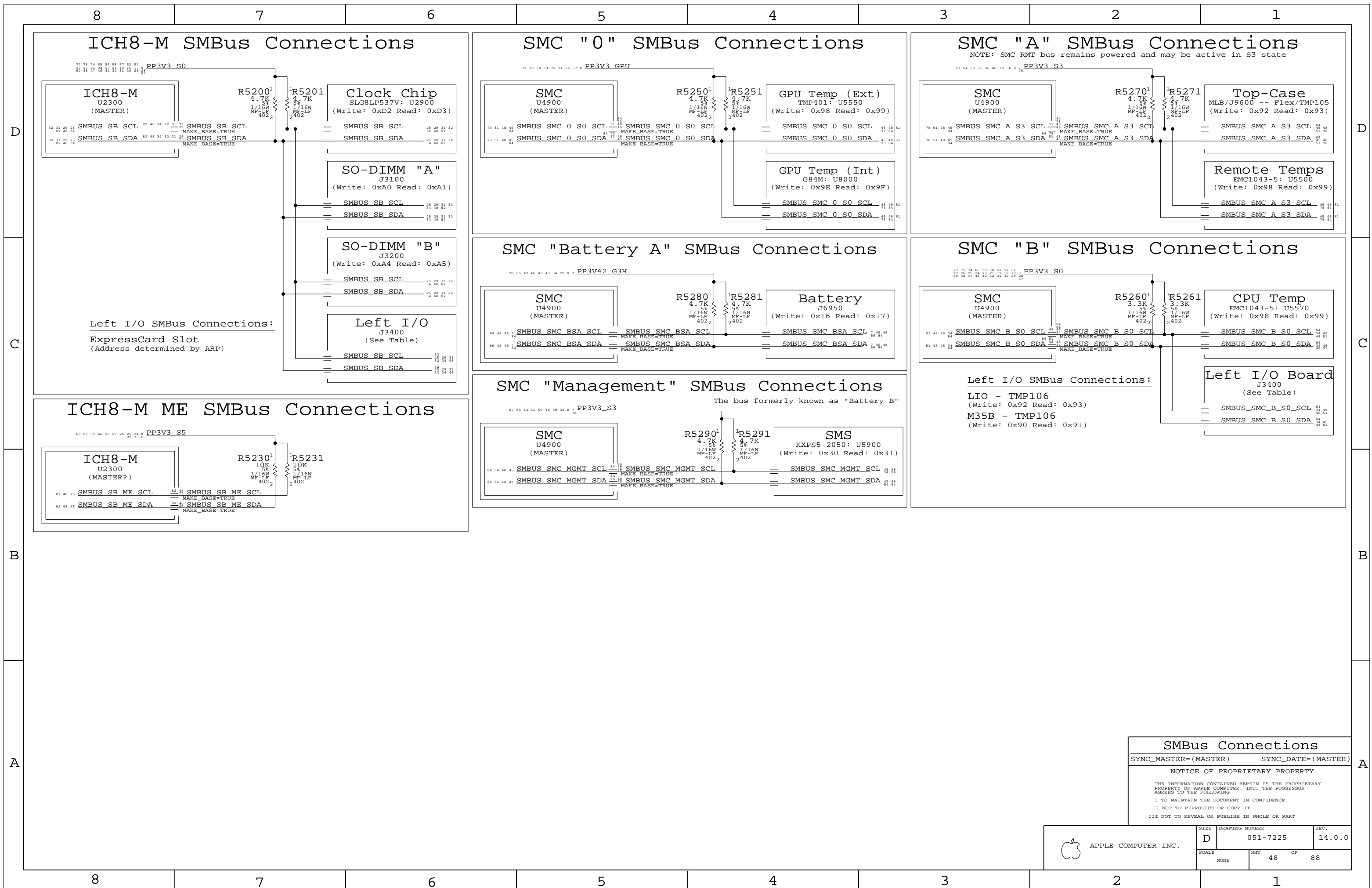
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	SCALE NONE	SHEET 47	OF 88



SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

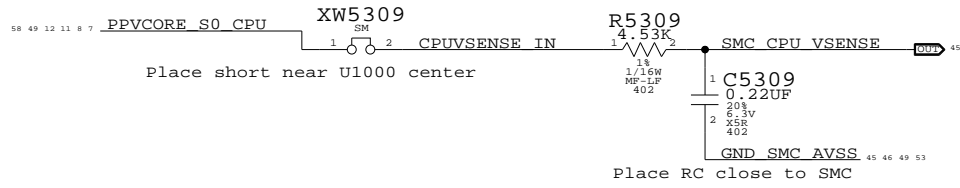
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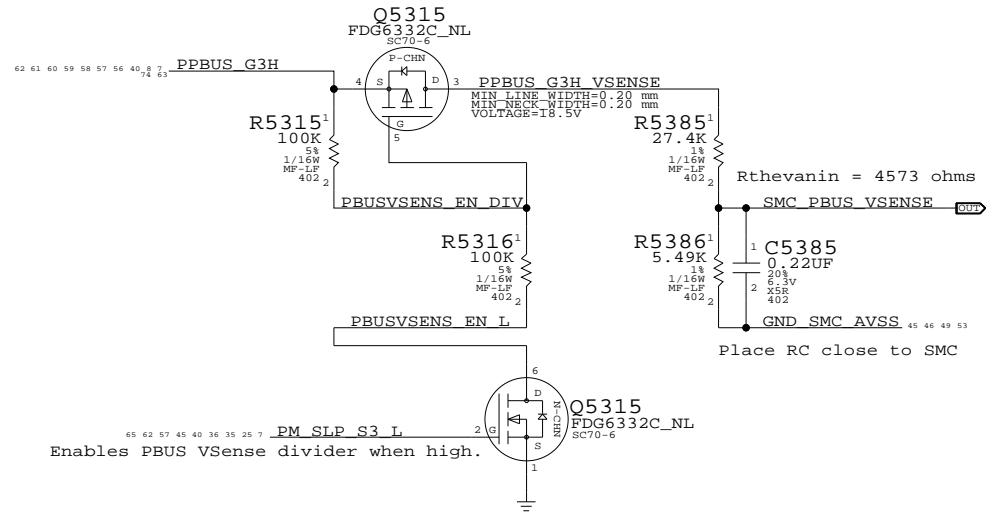
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	48	88	

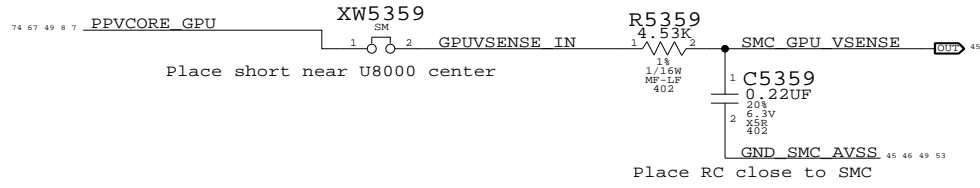
CPU Voltage Sense / Filter



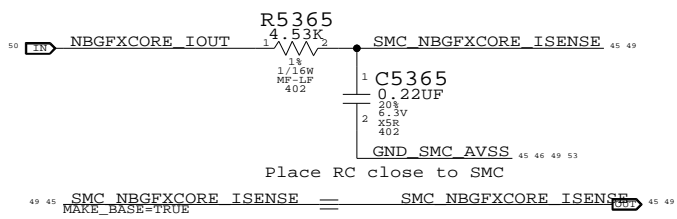
PBUS Voltage Sense & Filter



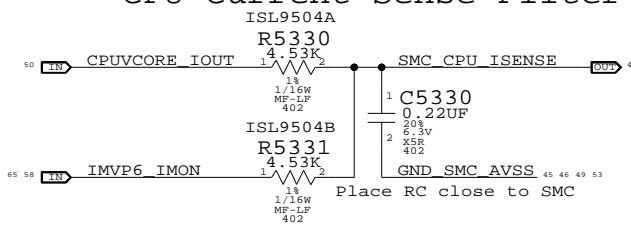
GPU Voltage Sense / Filter



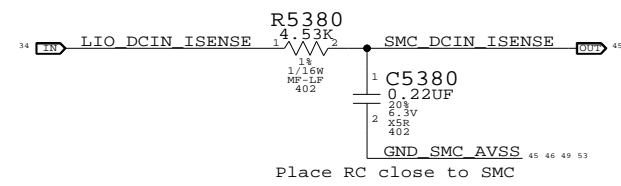
NB GFX Current Sense Filter



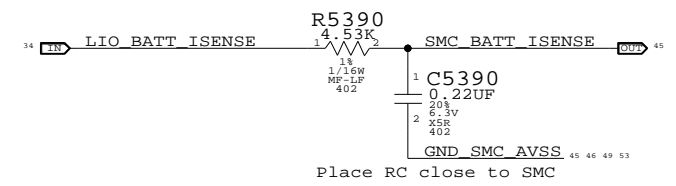
CPU Current Sense Filter



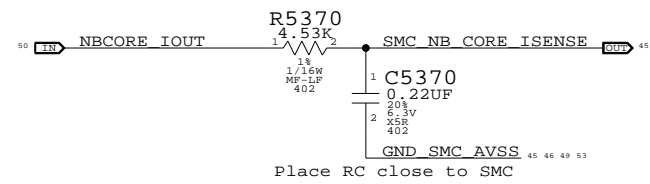
DCIN Current Sense Filter



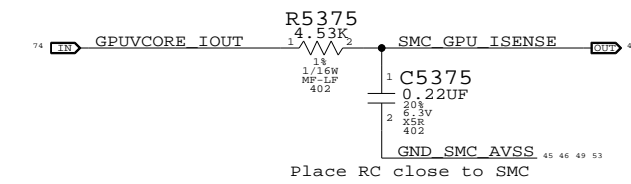
Battery (PBUS) Current Sense Filter



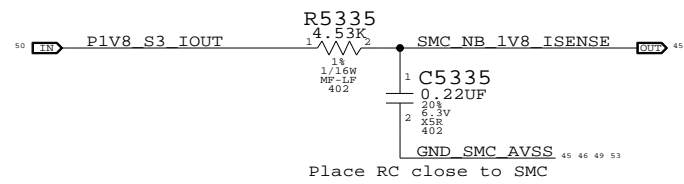
NB Core Current Sense Filter



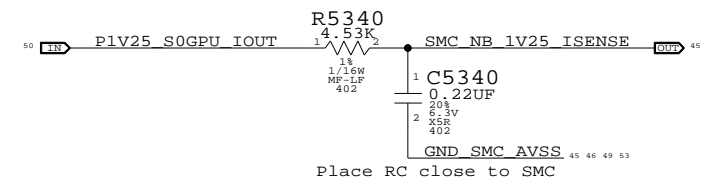
GPU Current Sense Filter



NB 1.8V Current Sense Filter

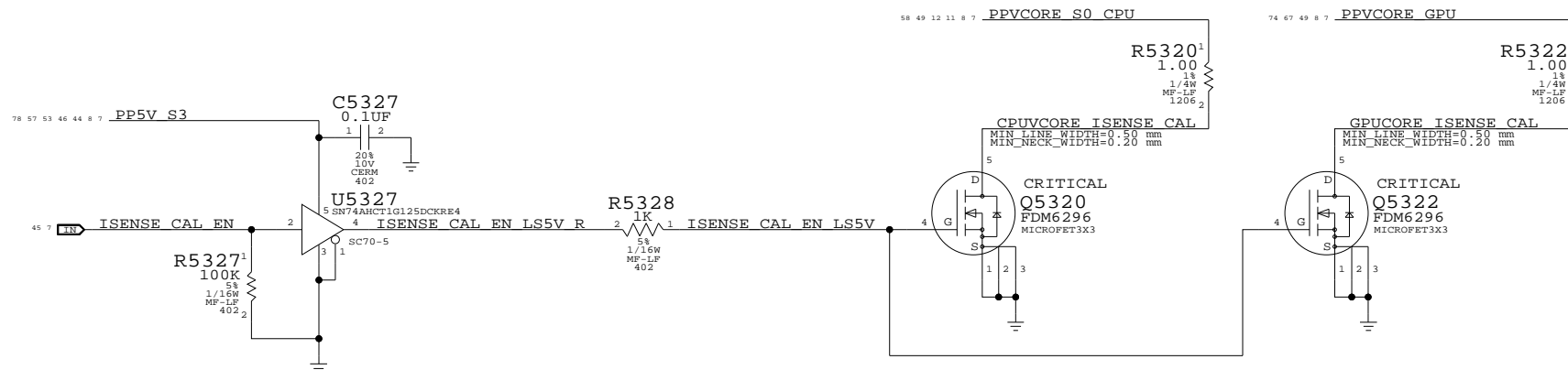


S0/GPU 1.25V Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



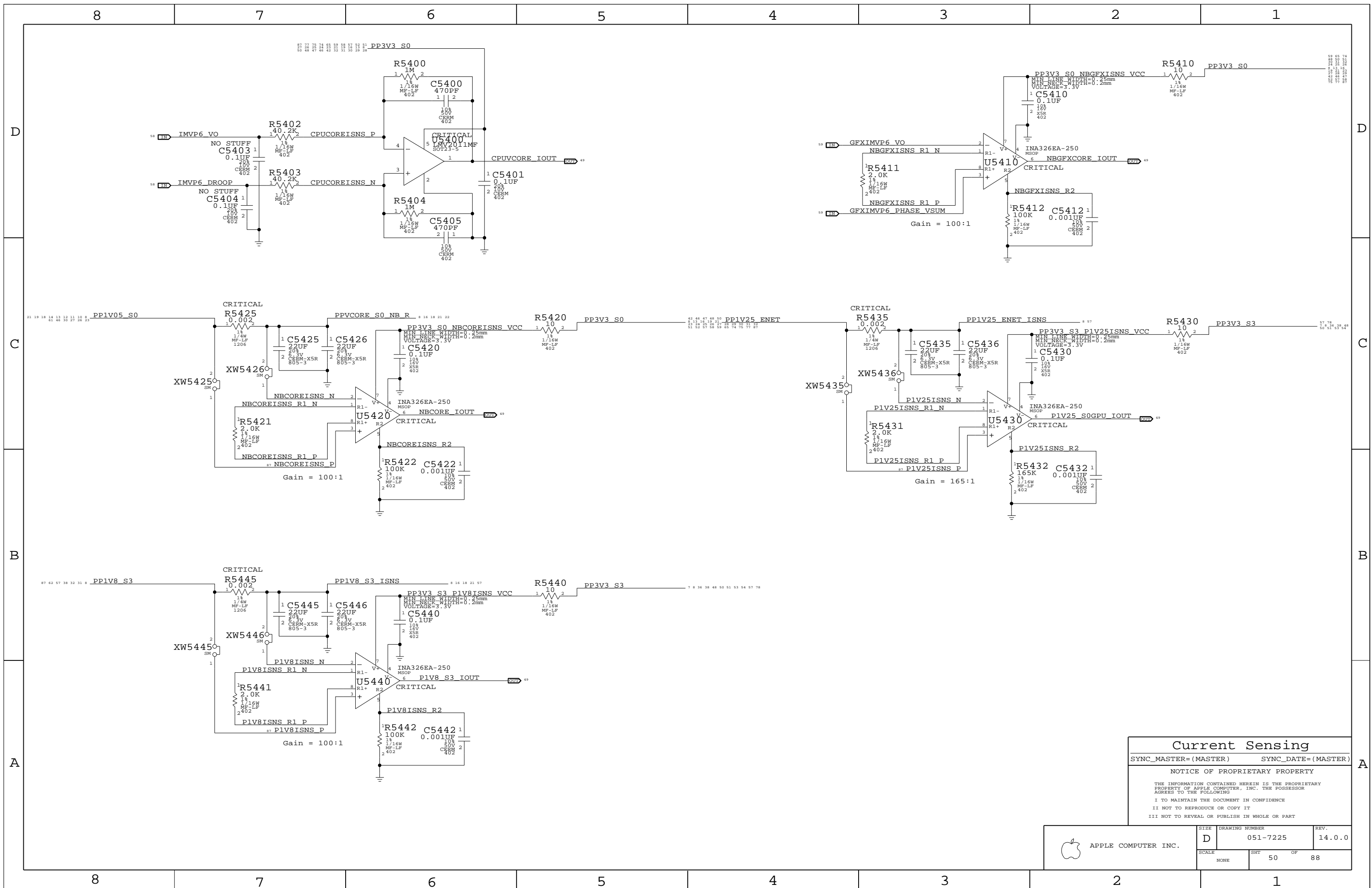
Current & Voltage Sensing

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	D	051-7225	14.0.0
SCALE	SHT	OF	REV.
NONE	49	88	



Current Sensing

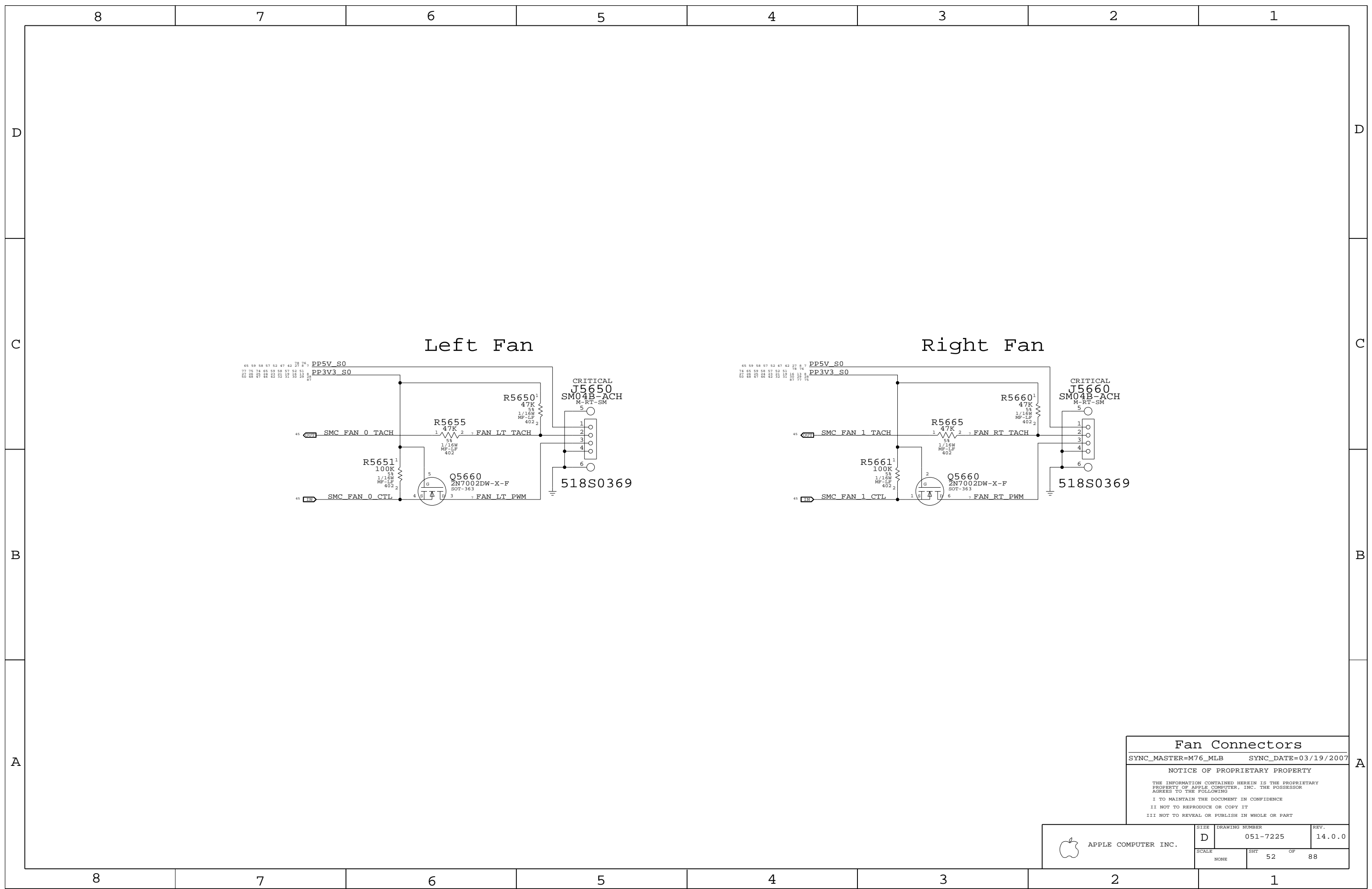
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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	SCALE NONE	SHEET 50	OF 88



Fan Connectors

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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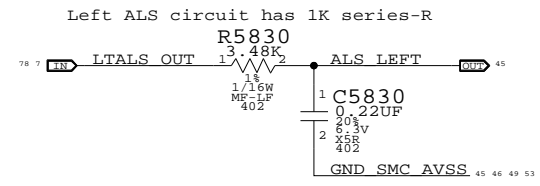
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II NOT TO REPRODUCE OR COPY IT

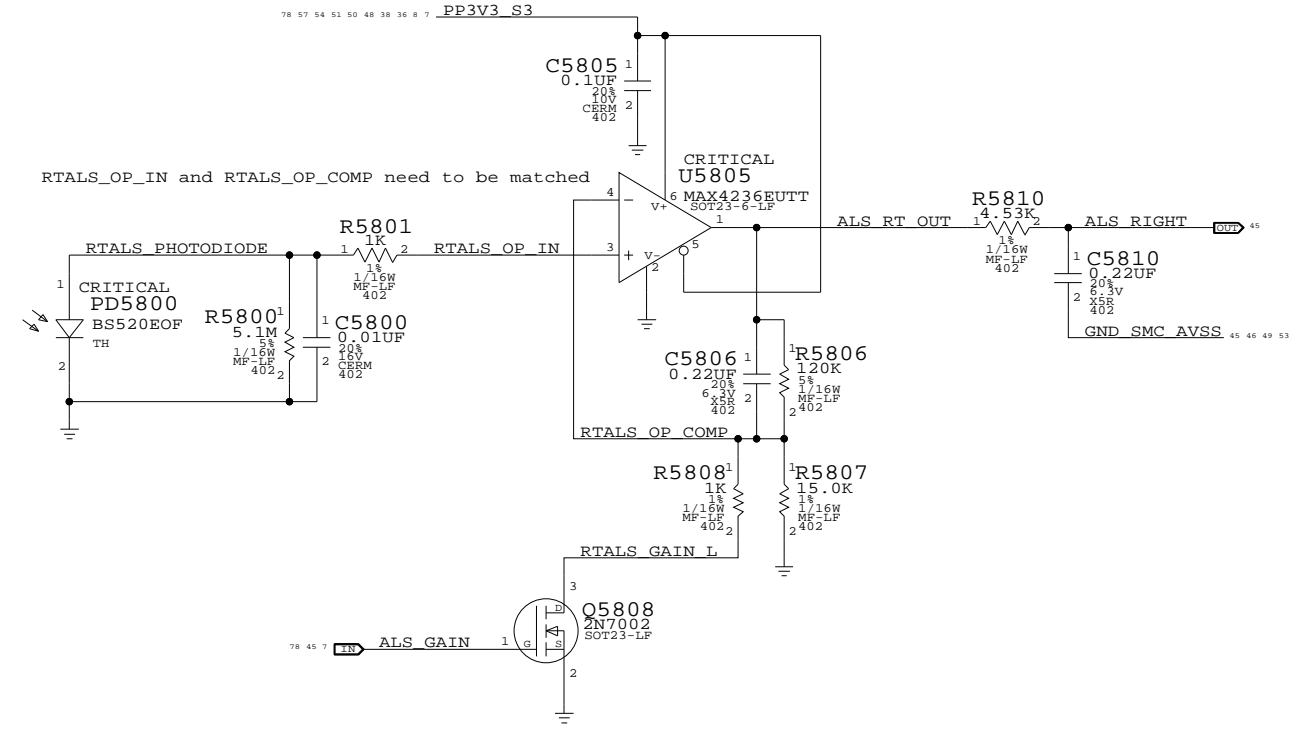
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. 14.0.0
	SCALE NONE	SHT 52	OF 88

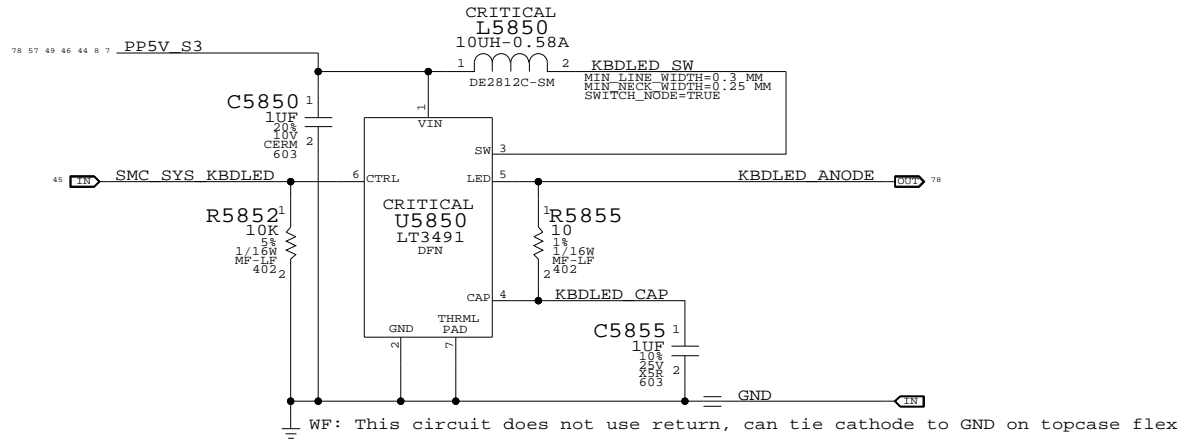
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

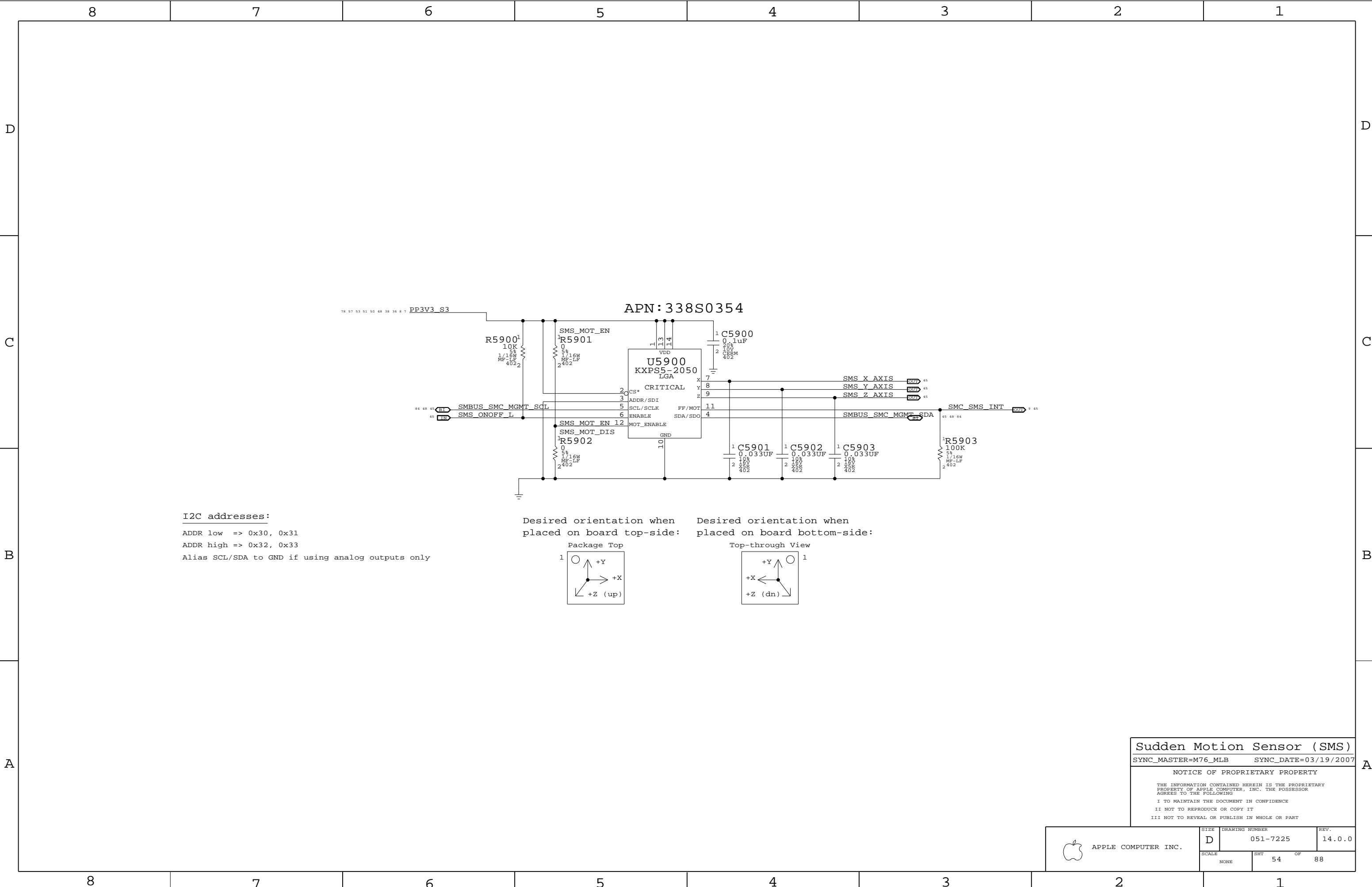
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SCALE	SHT	OF	
NONE	53	88	

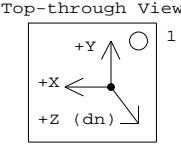
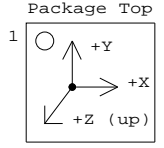


APN: 338S0354

I2C addresses:

ADDR low => 0x30, 0x31
 ADDR high => 0x32, 0x33
 Alias SCL/SDA to GND if using analog outputs only

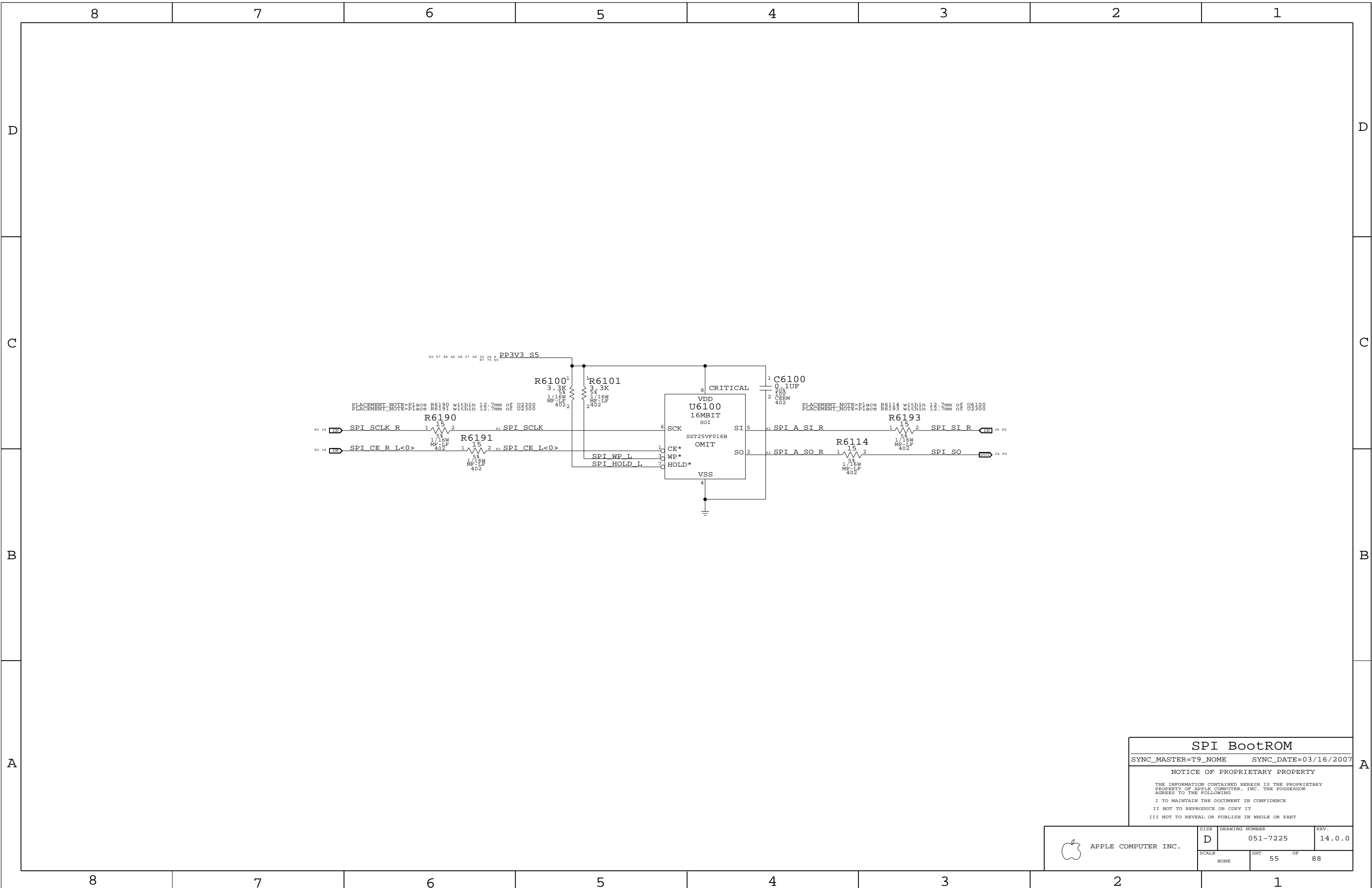
Desired orientation when placed on board top-side: Desired orientation when placed on board bottom-side:



Sudden Motion Sensor (SMS)
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SCALE	SHT	OF	
NONE	54	88	



SPI BootROM

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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	SCALE NONE	SHEET 55	OF 88

8

7

6

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1

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D

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C

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B

A

A

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5

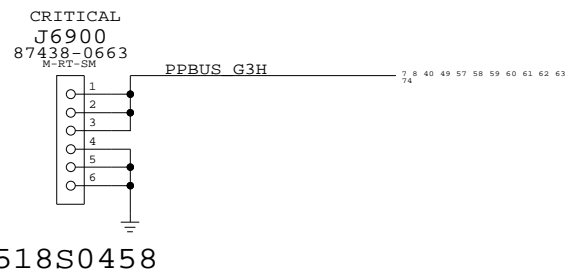
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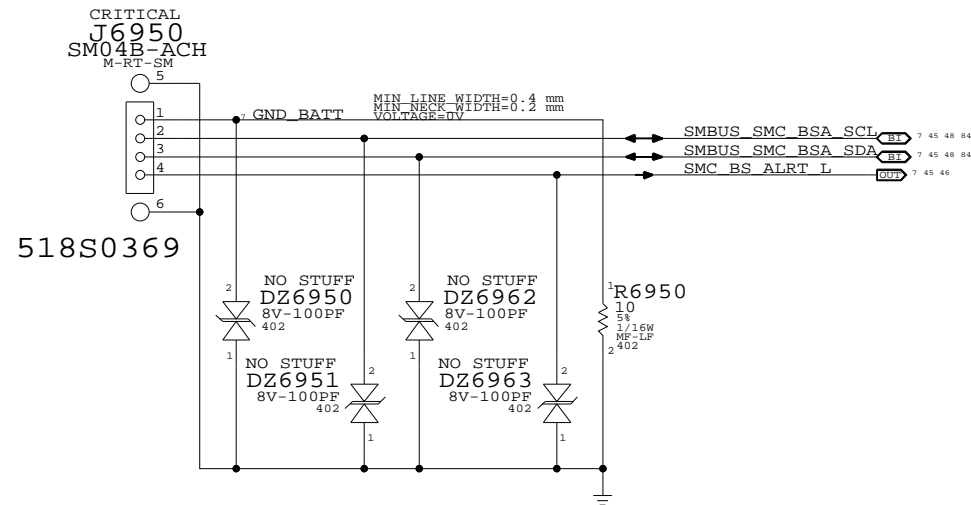
2

1

Left I/O Power Connector



Battery Connector (Digital Signals)

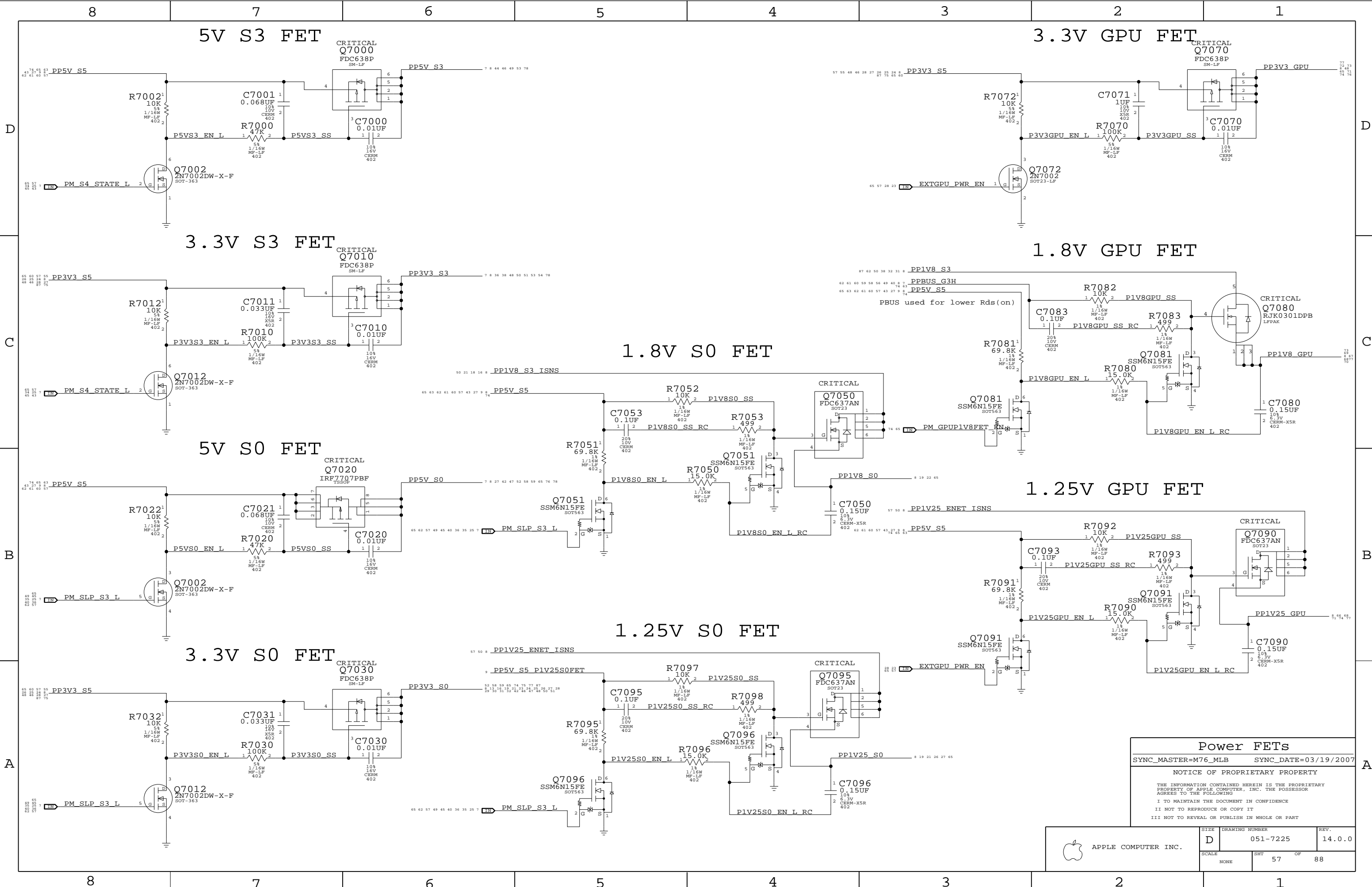


PBus-In & Battery Connectors
 SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

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SCALE	SHT	OF	
NONE	56	88	



Power FETs

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

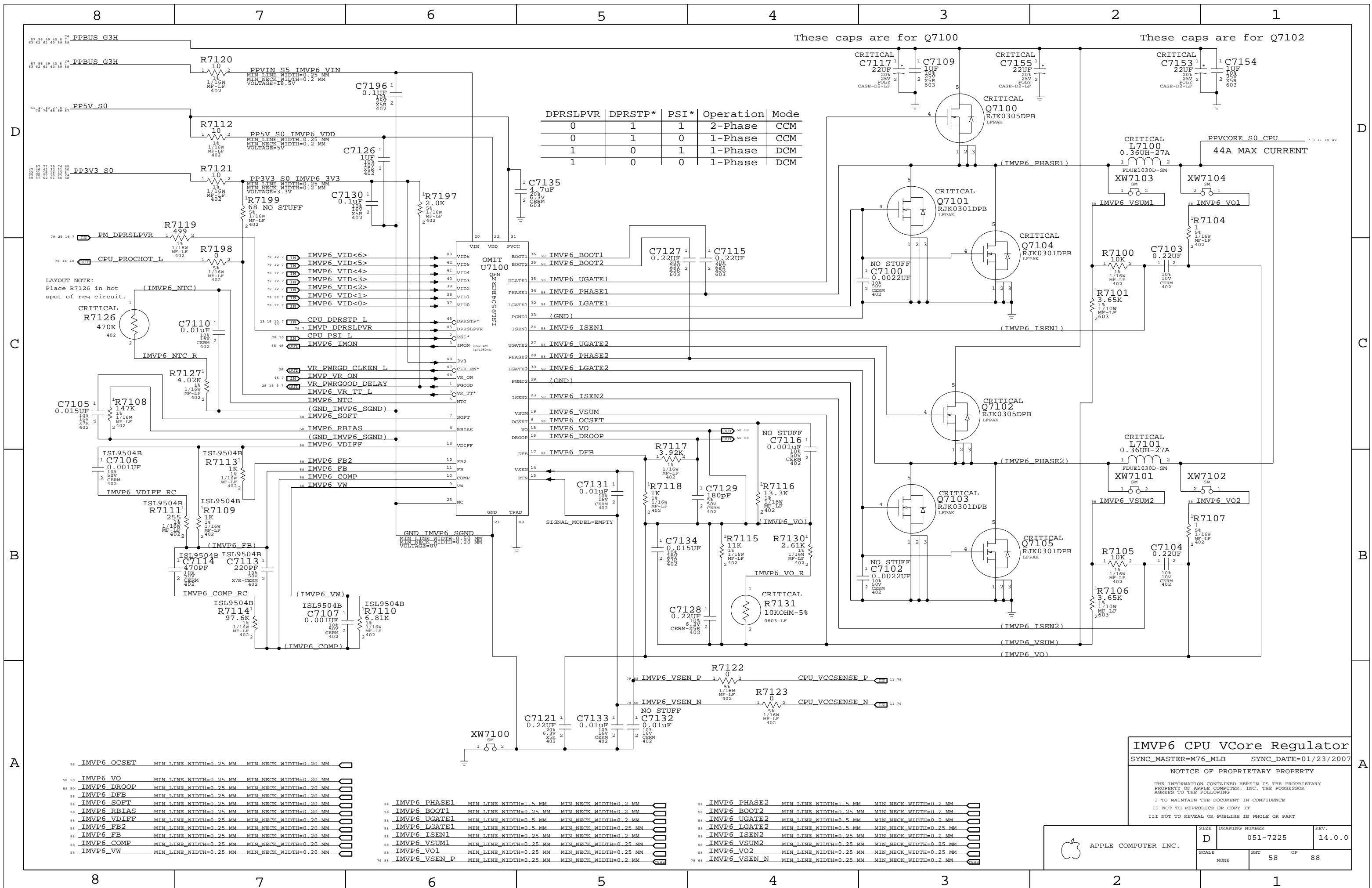
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	SCALE NONE	SHEET 57	OF 88



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

Pin	Signal	Value
36	IMVP6_BOOT1	0.22uF
26	IMVP6_BOOT2	0.22uF
35	IMVP6_UGATE1	0.0022uF
34	IMVP6_PHASE1	0.0022uF
32	IMVP6_LGATE1	0.0022uF
27	IMVP6_UGATE2	0.0022uF
28	IMVP6_PHASE2	0.0022uF
30	IMVP6_LGATE2	0.0022uF
23	IMVP6_ISEN2	0.0022uF
19	IMVP6_VSUM	0.0022uF
18	IMVP6_VO	0.0022uF

IMVP6 CPU VCore Regulator

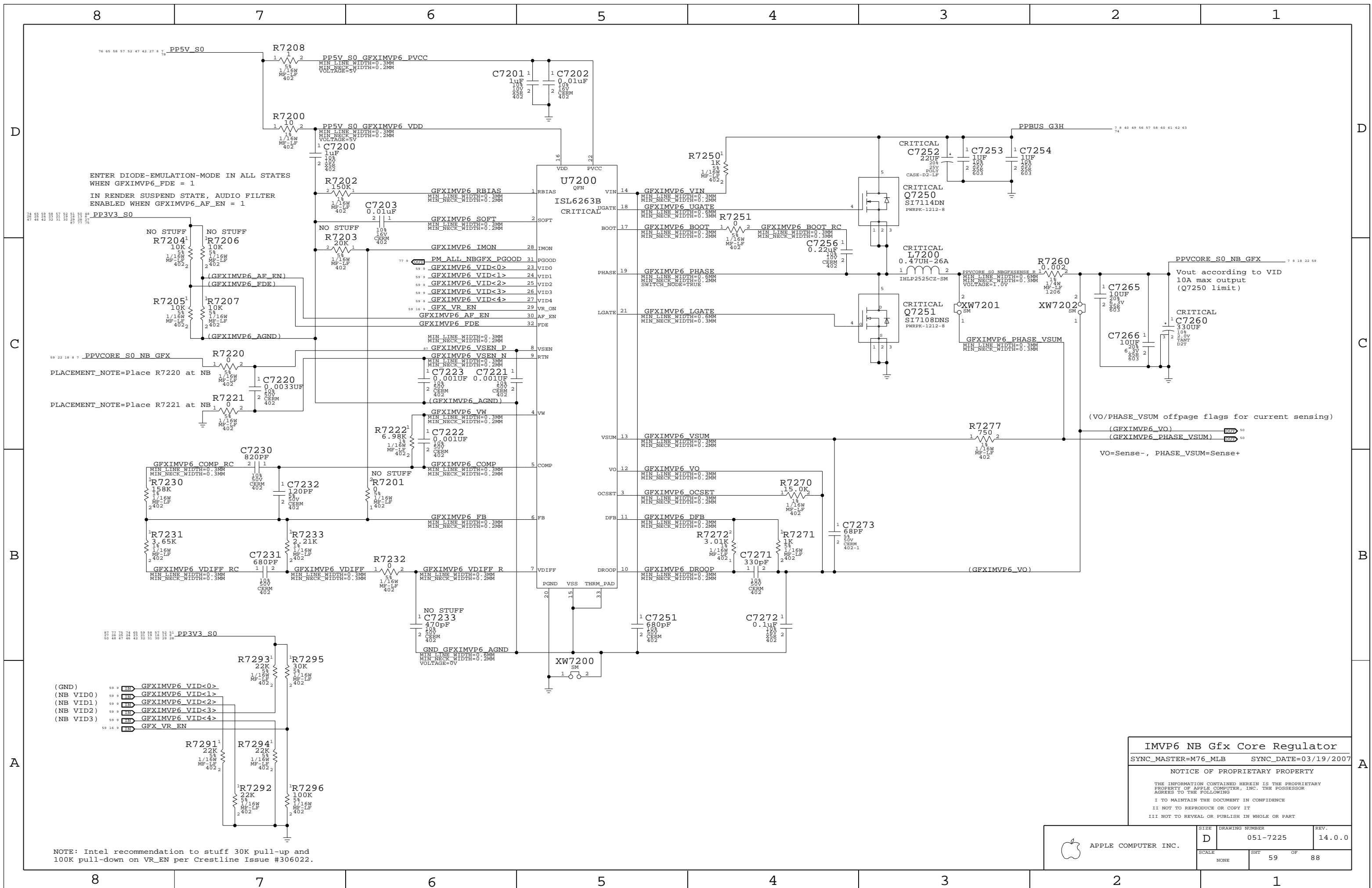
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	SCALE: NONE	SHEET: 58	OF: 88



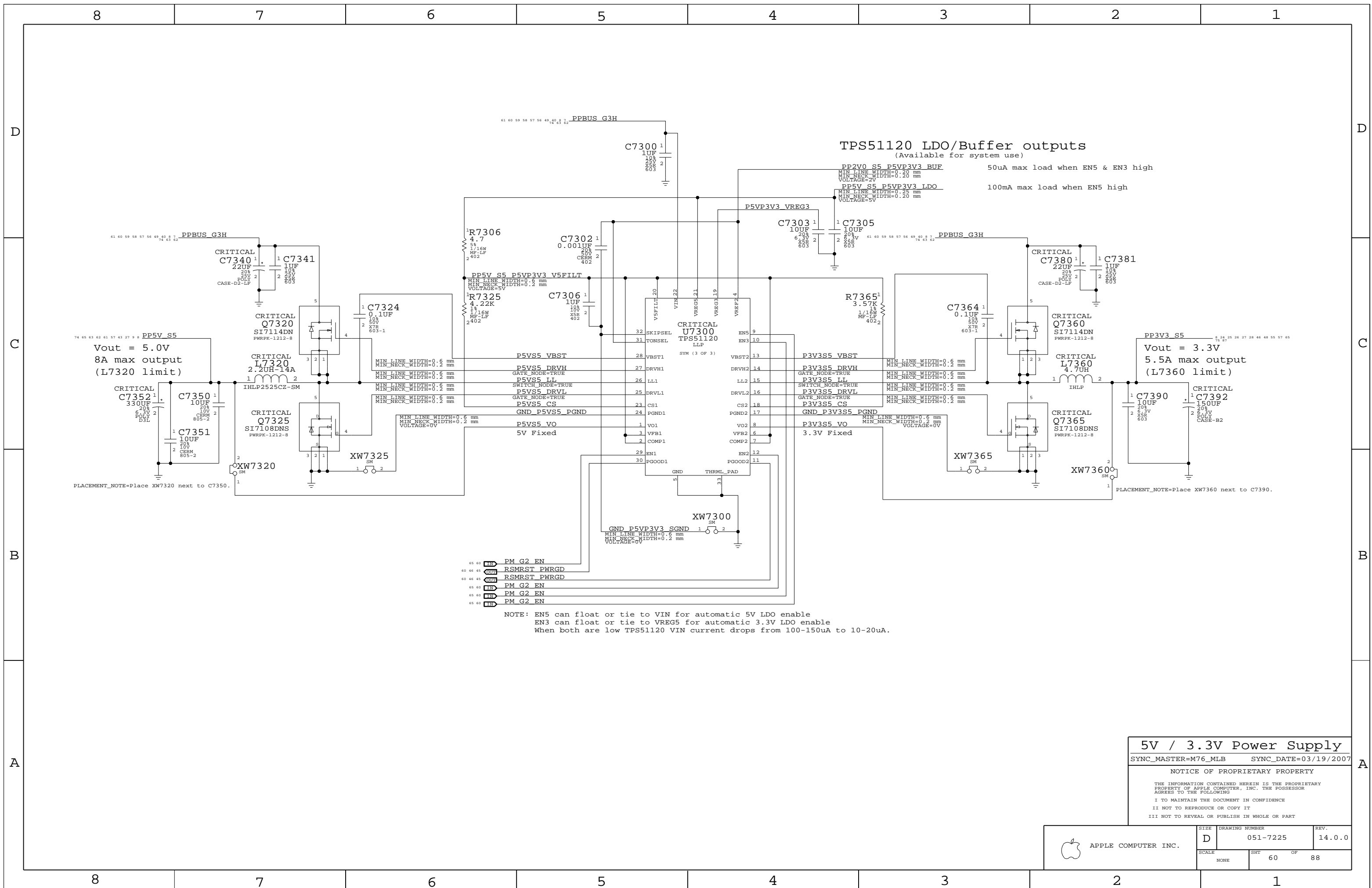
IMVP6 NB Gfx Core Regulator

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SCALE	SHT	OF	
NONE	59	88	



TPS51120 LDO/Buffer outputs
(Available for system use)

50uA max load when EN5 & EN3 high

100mA max load when EN5 high

Vout = 5.0V
8A max output
(L7320 limit)

Vout = 3.3V
5.5A max output
(L7360 limit)

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

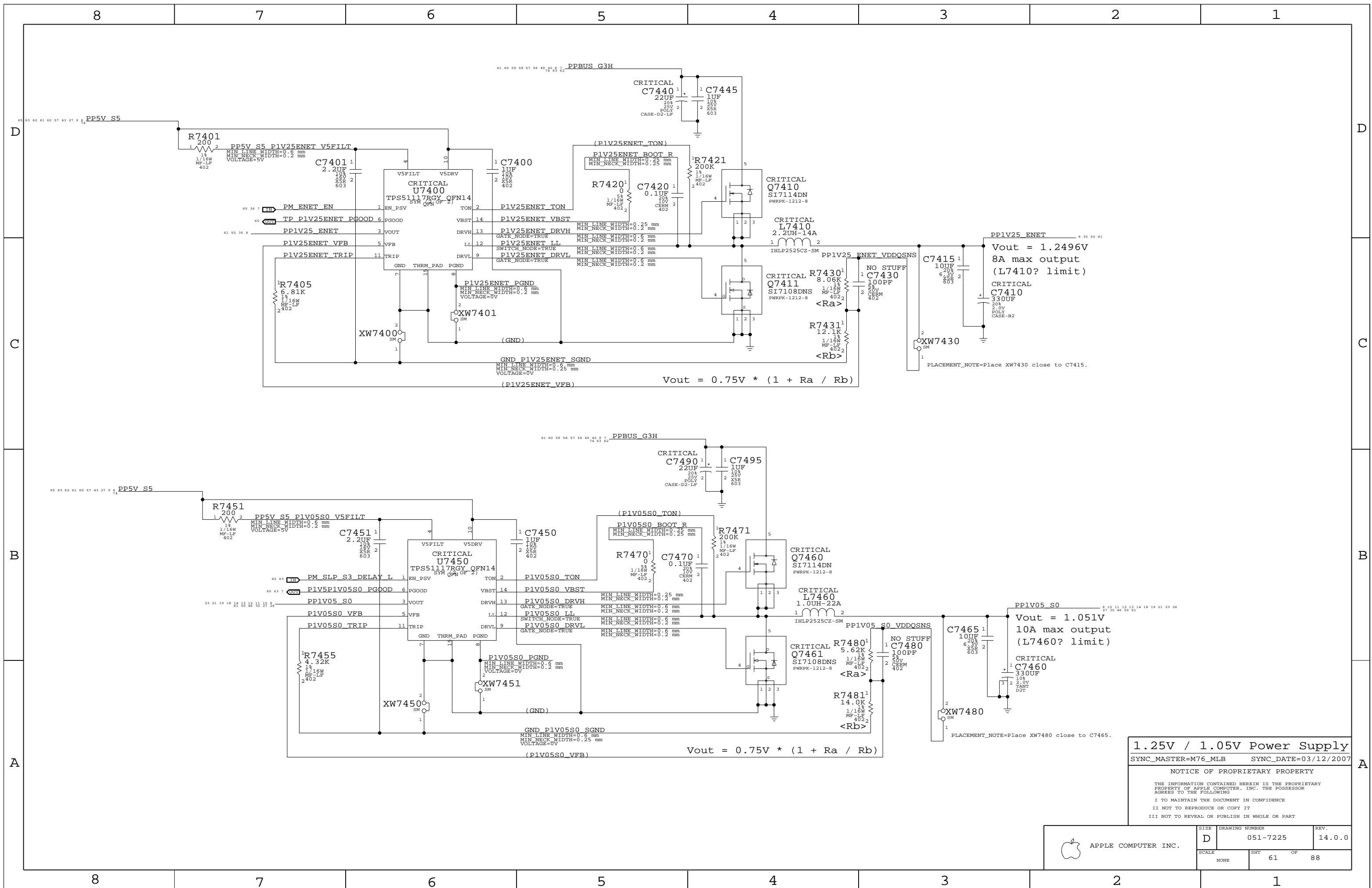
5V / 3.3V Power Supply

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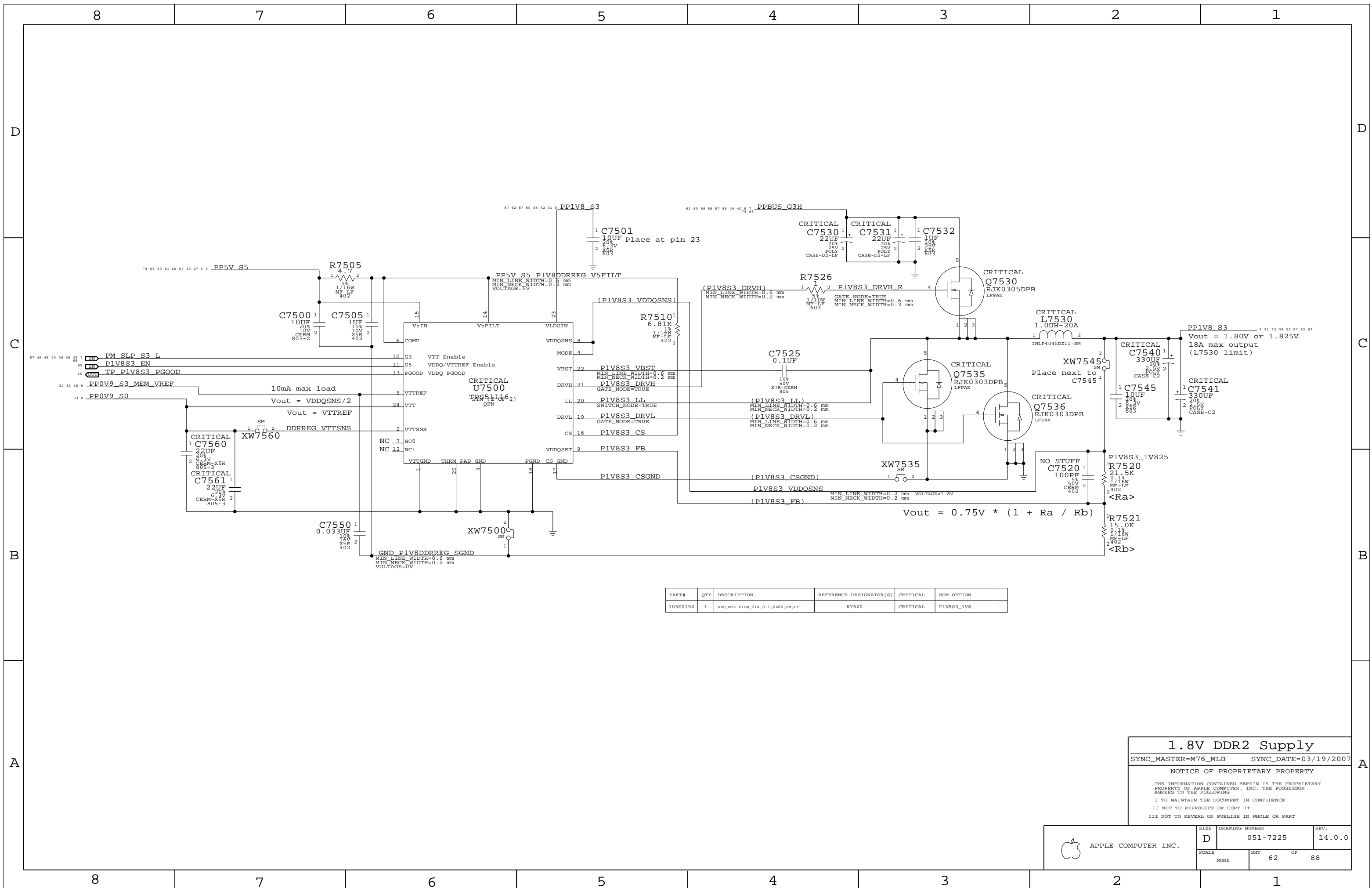
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	REV.
NONE	60	88	



1.25V / 1.05V Power Supply
 SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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SCALE	SHT	OF	
NONE	61	88	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S0192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_1V8

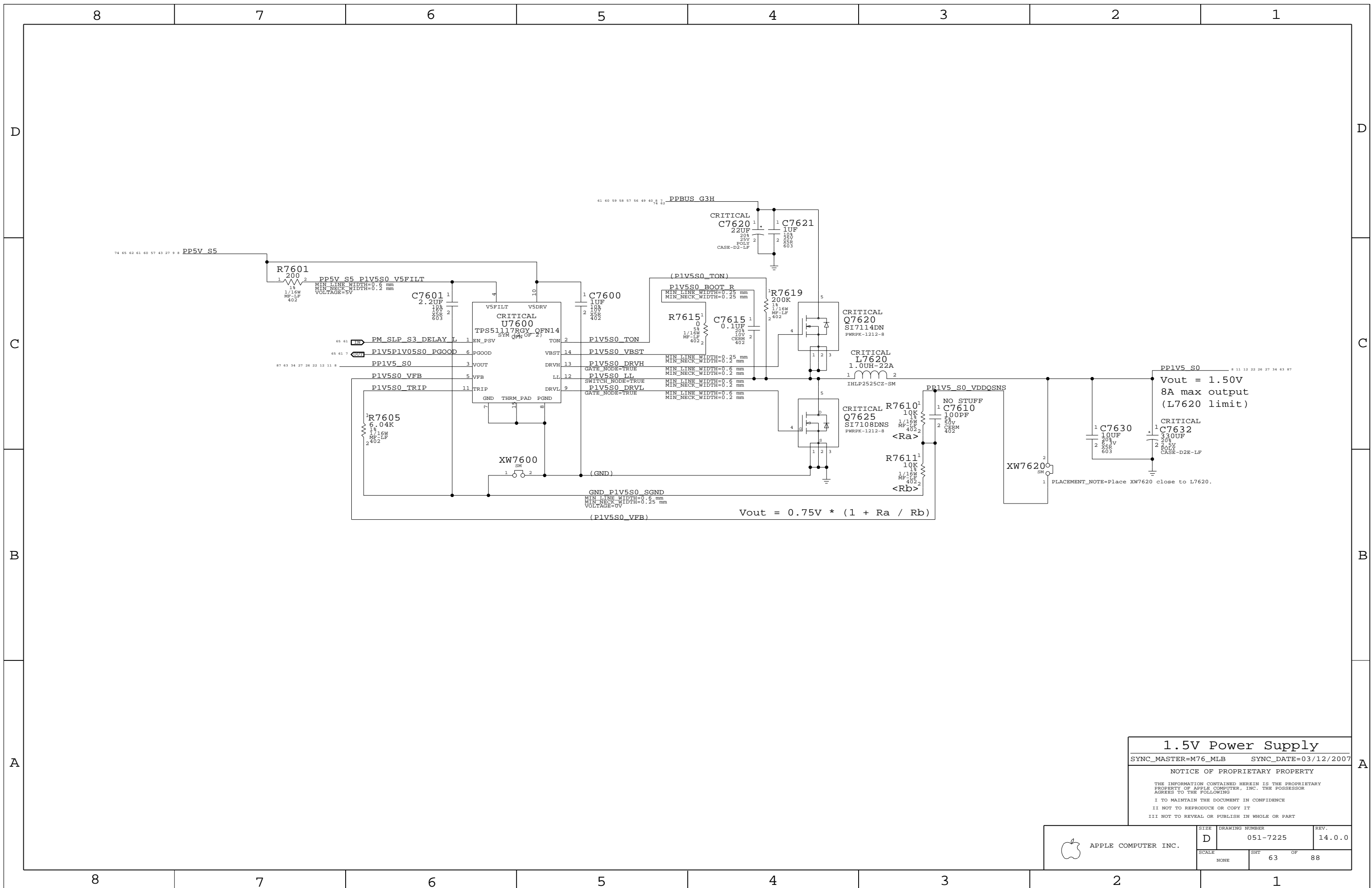
1.8V DDR2 Supply
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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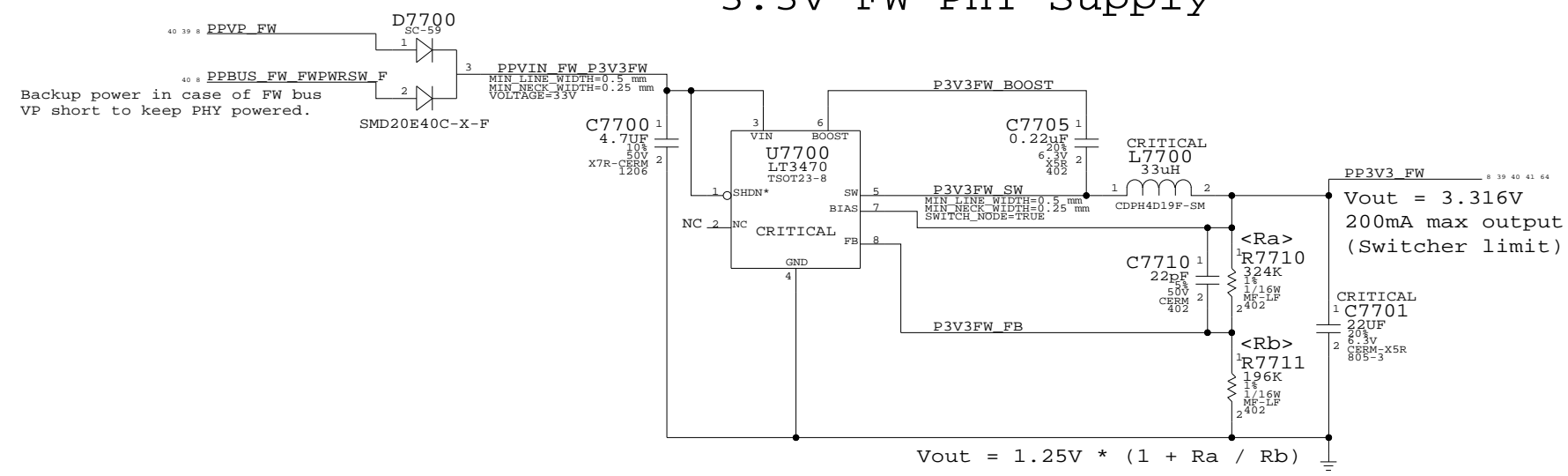
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SCALE	SHT	OF	REV.
NONE	62	88	



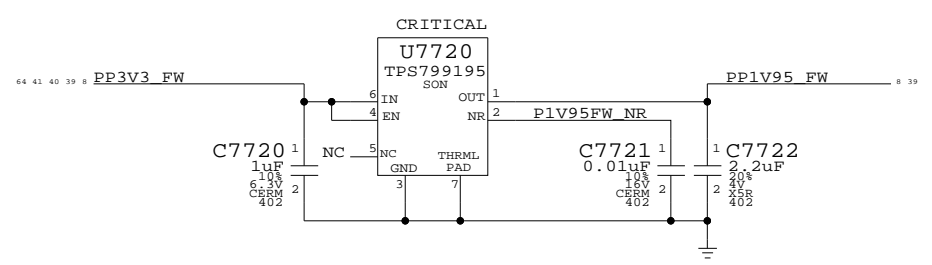
1.5V Power Supply
 SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	63	88	

3.3V FW PHY Supply



1.95V FW PHY Supply

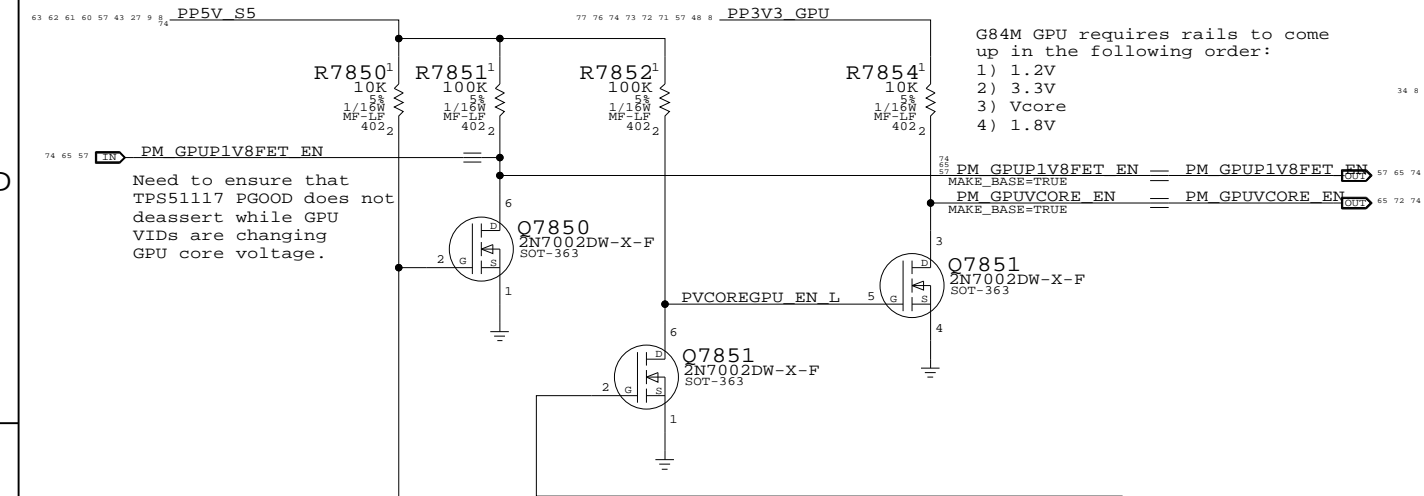


FW PHY Power Supplies
 SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SCALE	SHT	OF	REV.
NONE	64	88	

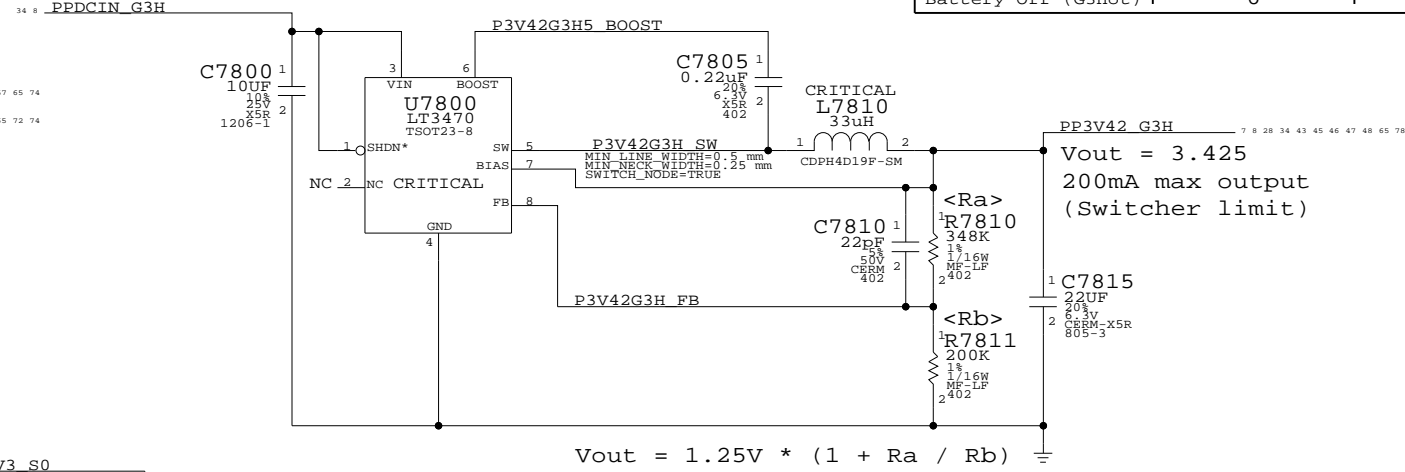
Power Control Signals



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



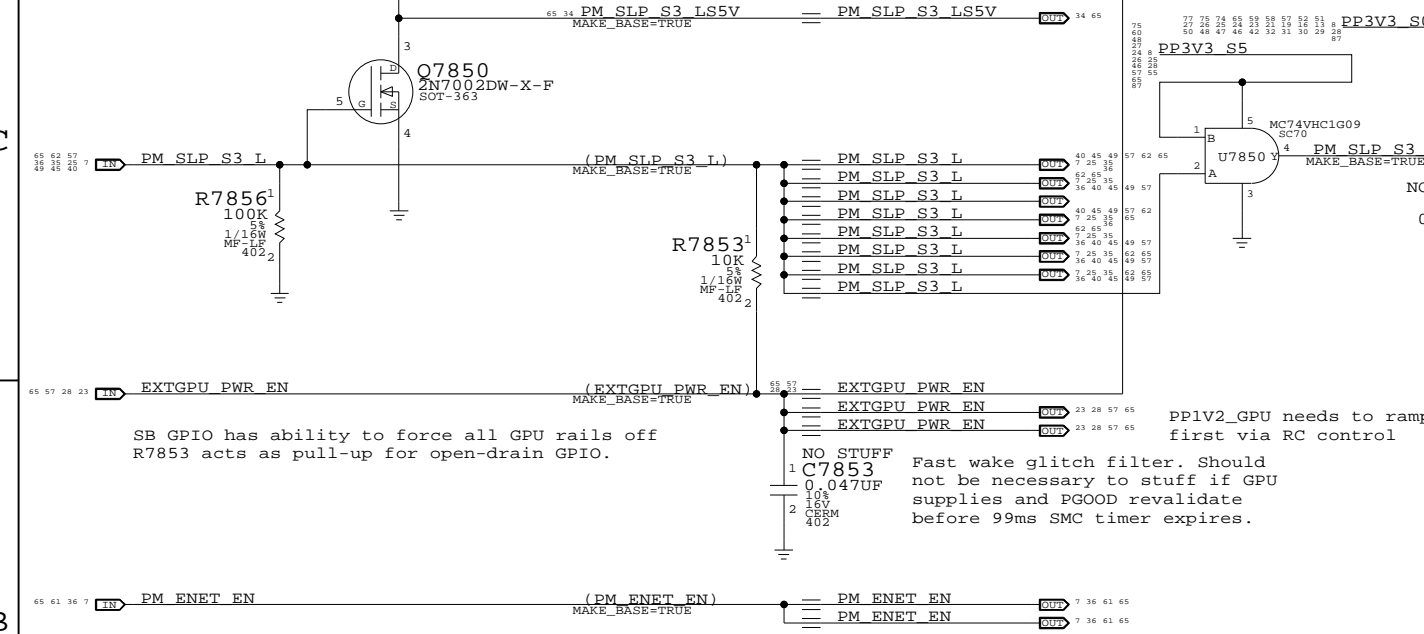
Vout = 3.425
200mA max output
(Switcher limit)

Unused PGOOD Signals

TP_P1V25ENET_PGOOD	=	TP_P1V25ENET_PGOOD
TP_P1V8S3_PGOOD	=	TP_P1V8S3_PGOOD

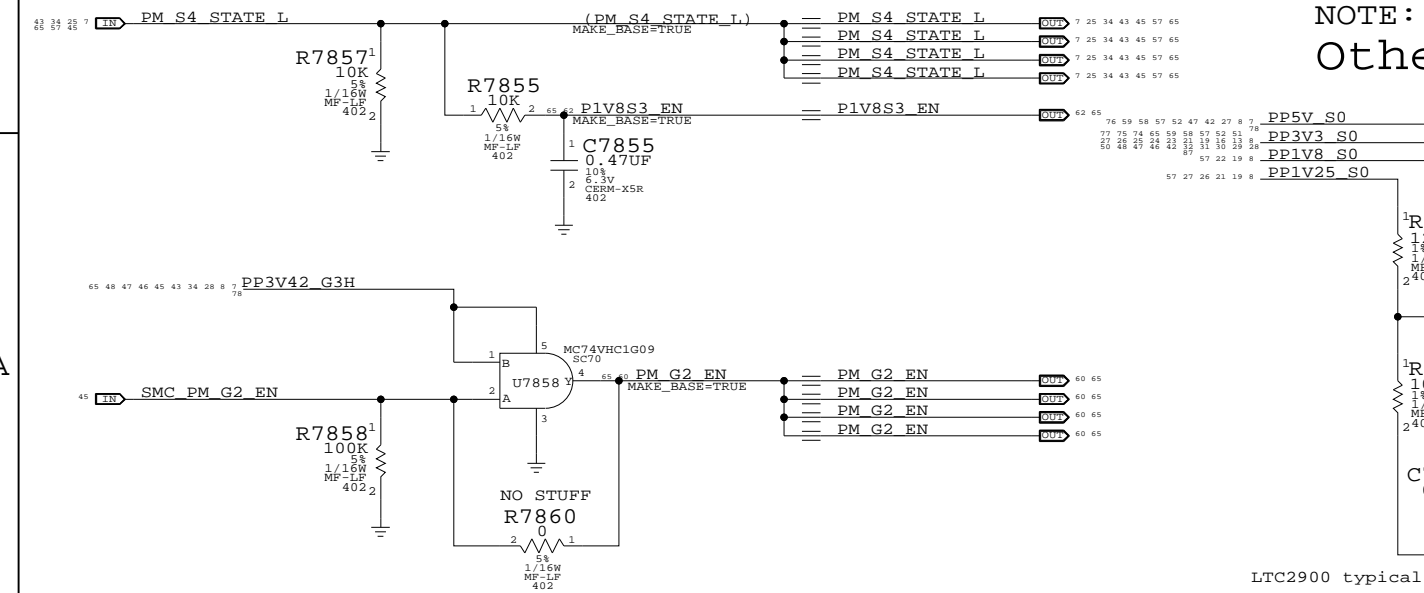
1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



NOTE: 0.9V/2.5V is not checked! Other S0 Rails PWRGD Circuit

Does not include GFX rails



3.425V G3Hot Supply & Power Control

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SCALE	SHT	OF
NONE	65	88



APPLE COMPUTER INC.

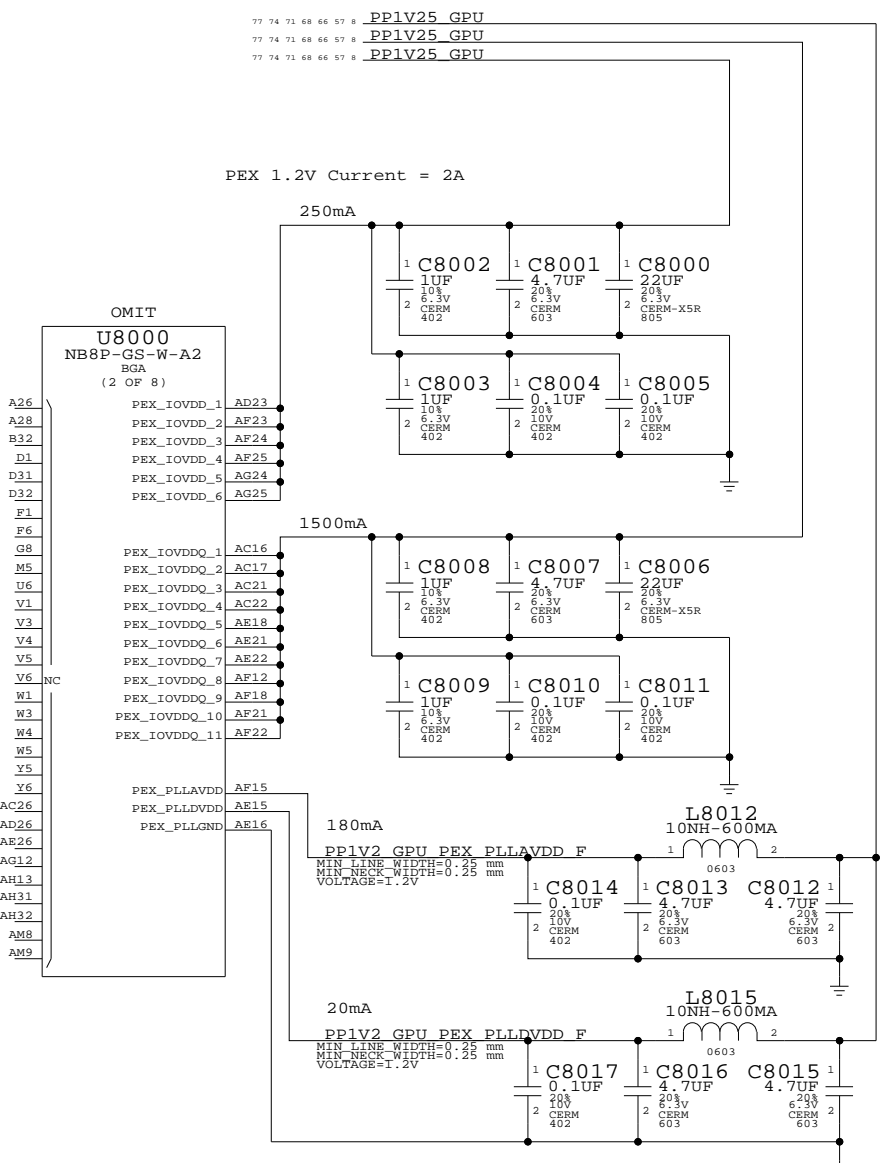
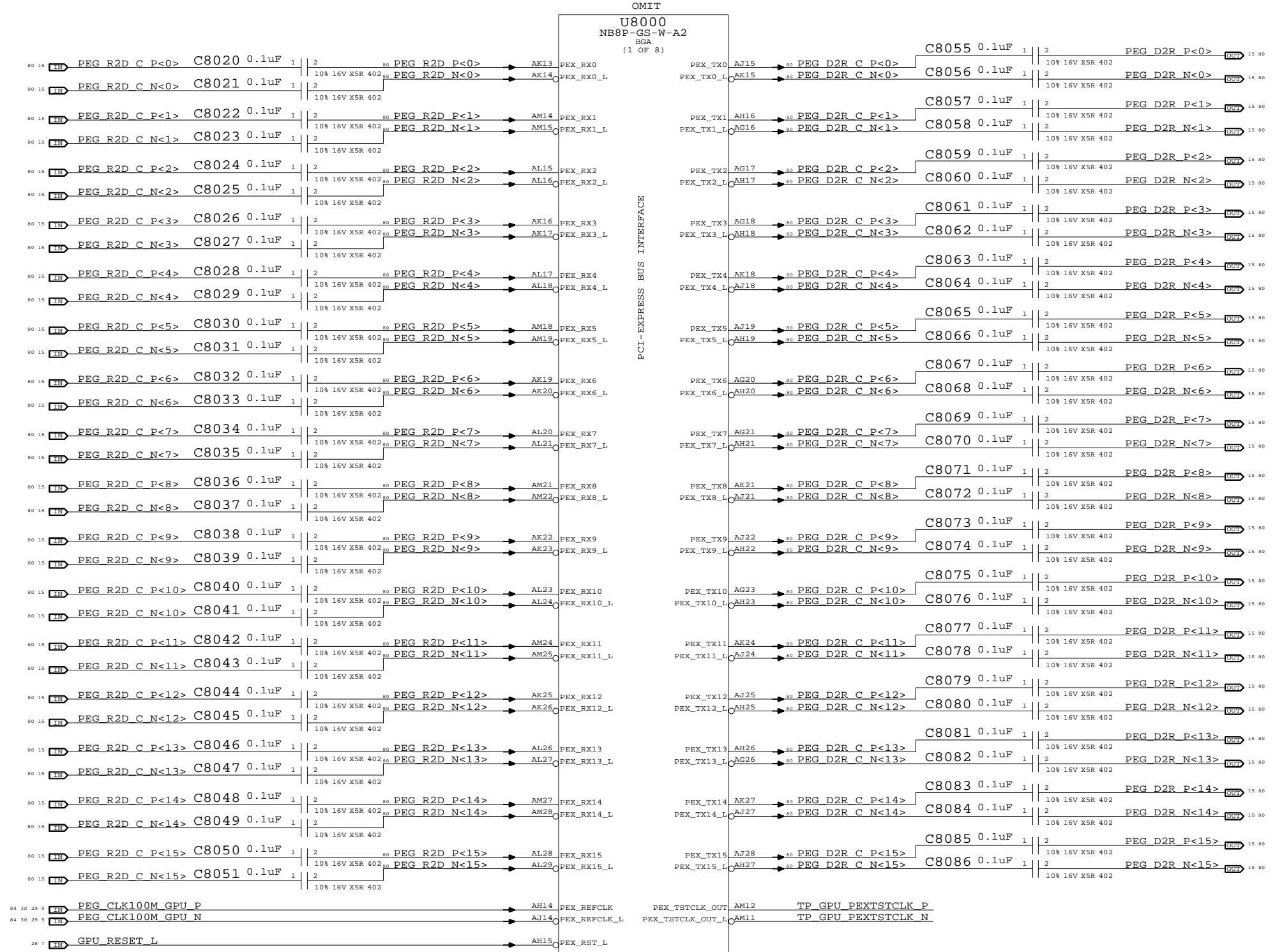
Page Notes

Power aliases required by this page:

- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M PCI-E
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	66	88	

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Power aliases required by this page:

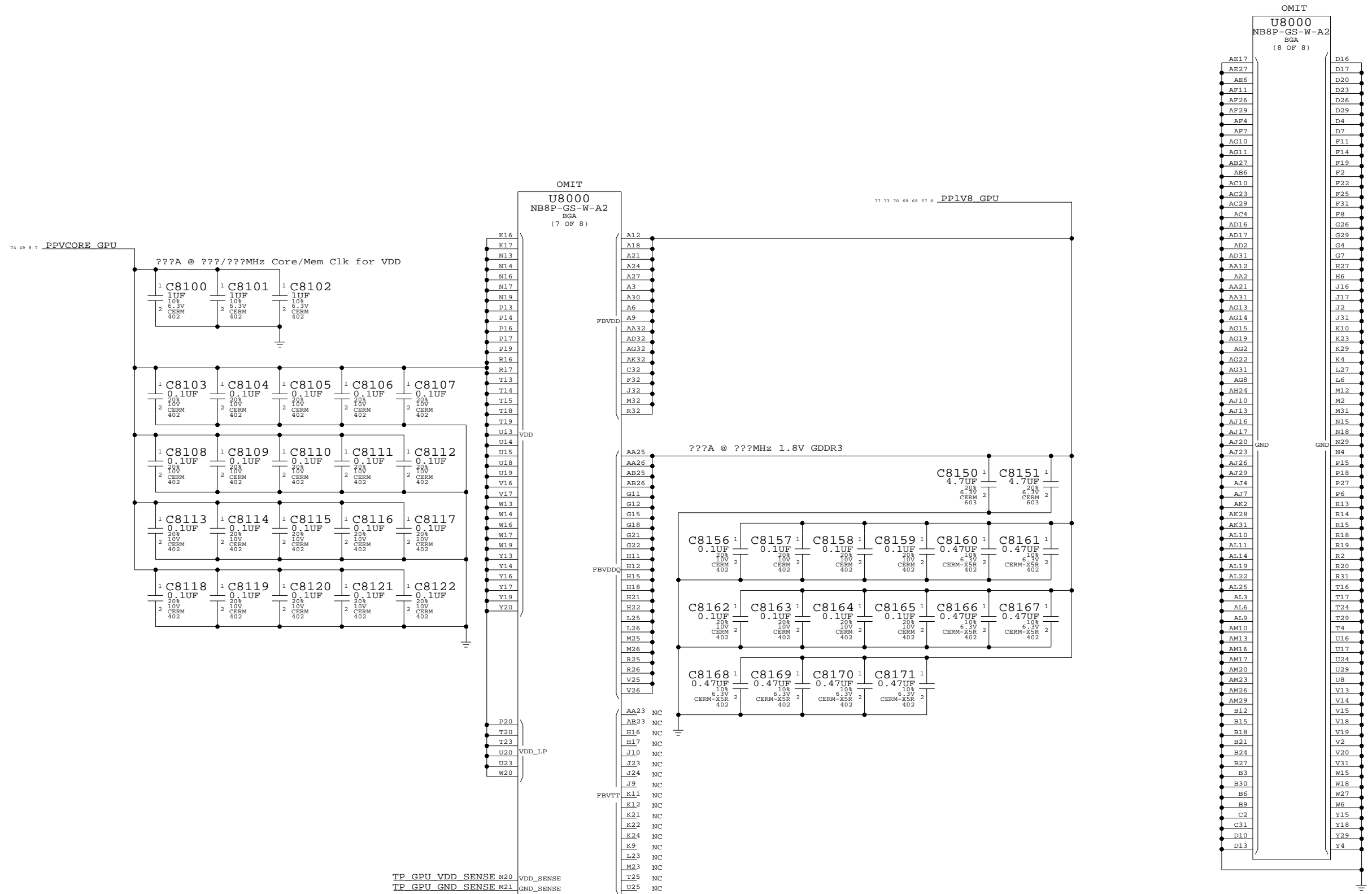
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



NV G84M Core/FB Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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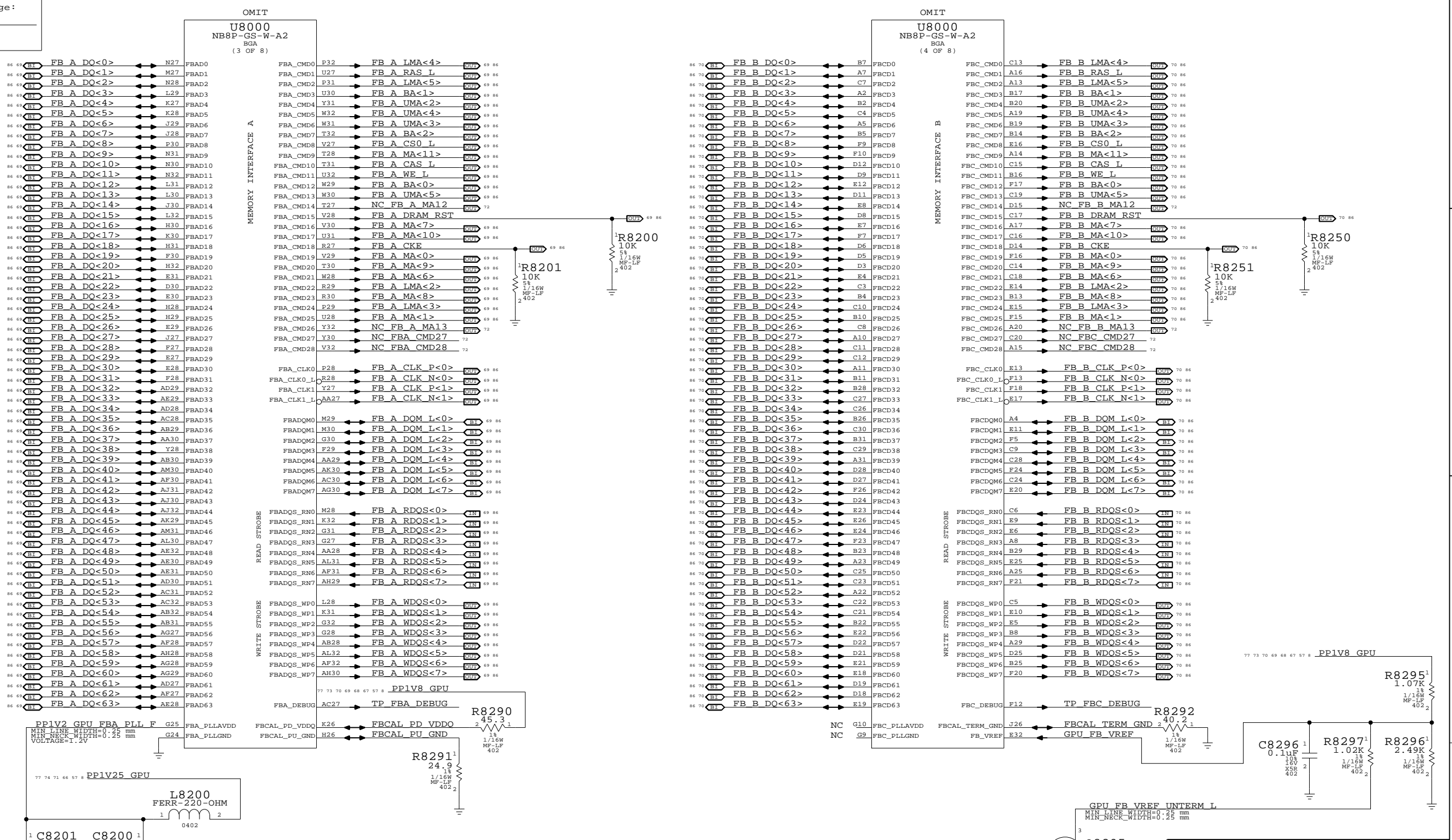
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	67	88	

Page Notes

Power aliases required by this page:
 - =PPIV2_GPU_FBPLLAVDD
 - =PPIV8_GPU_FBIO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

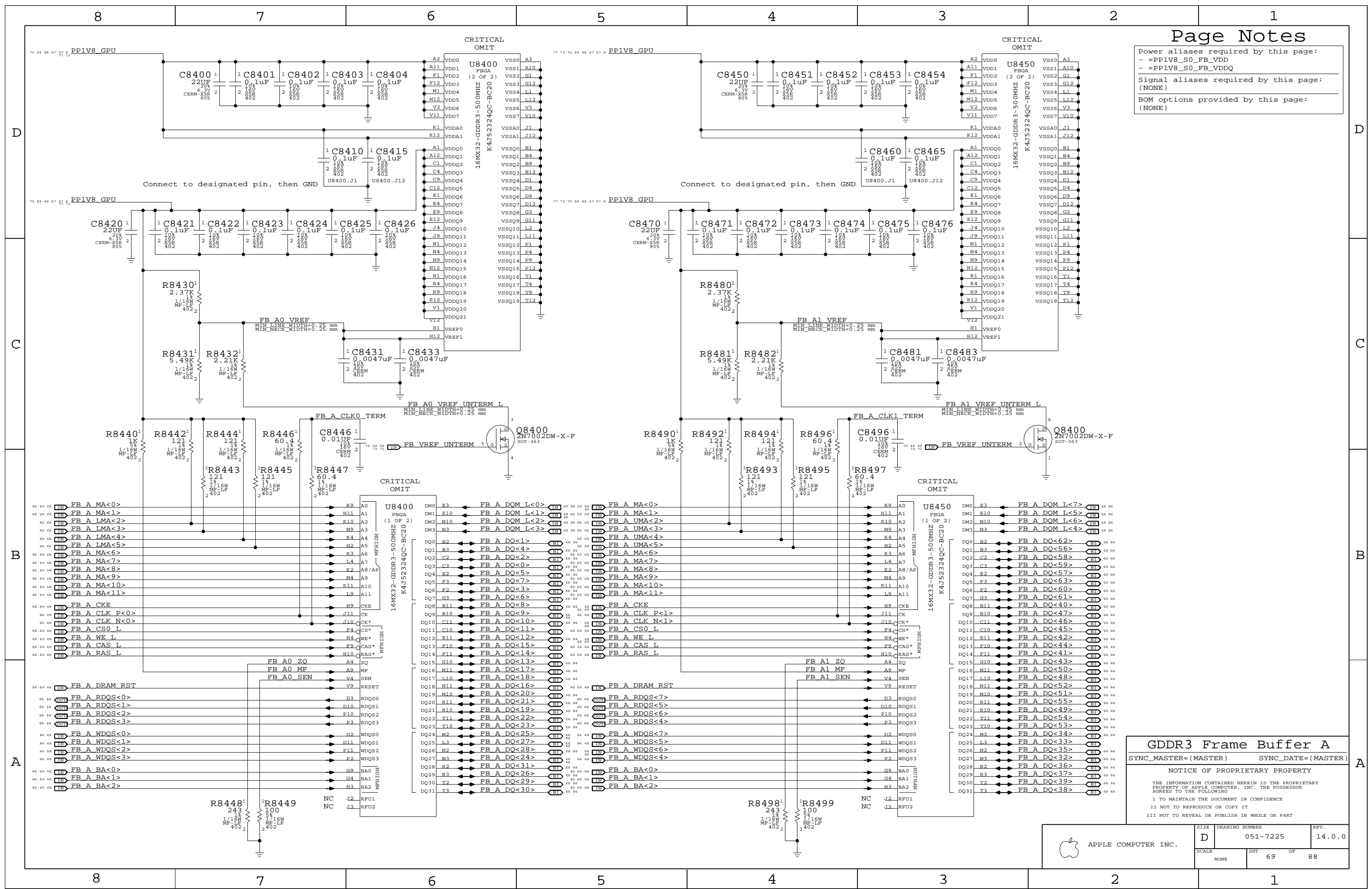


NV G84M Frame Buffer I/F
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF	
NONE	68	88	

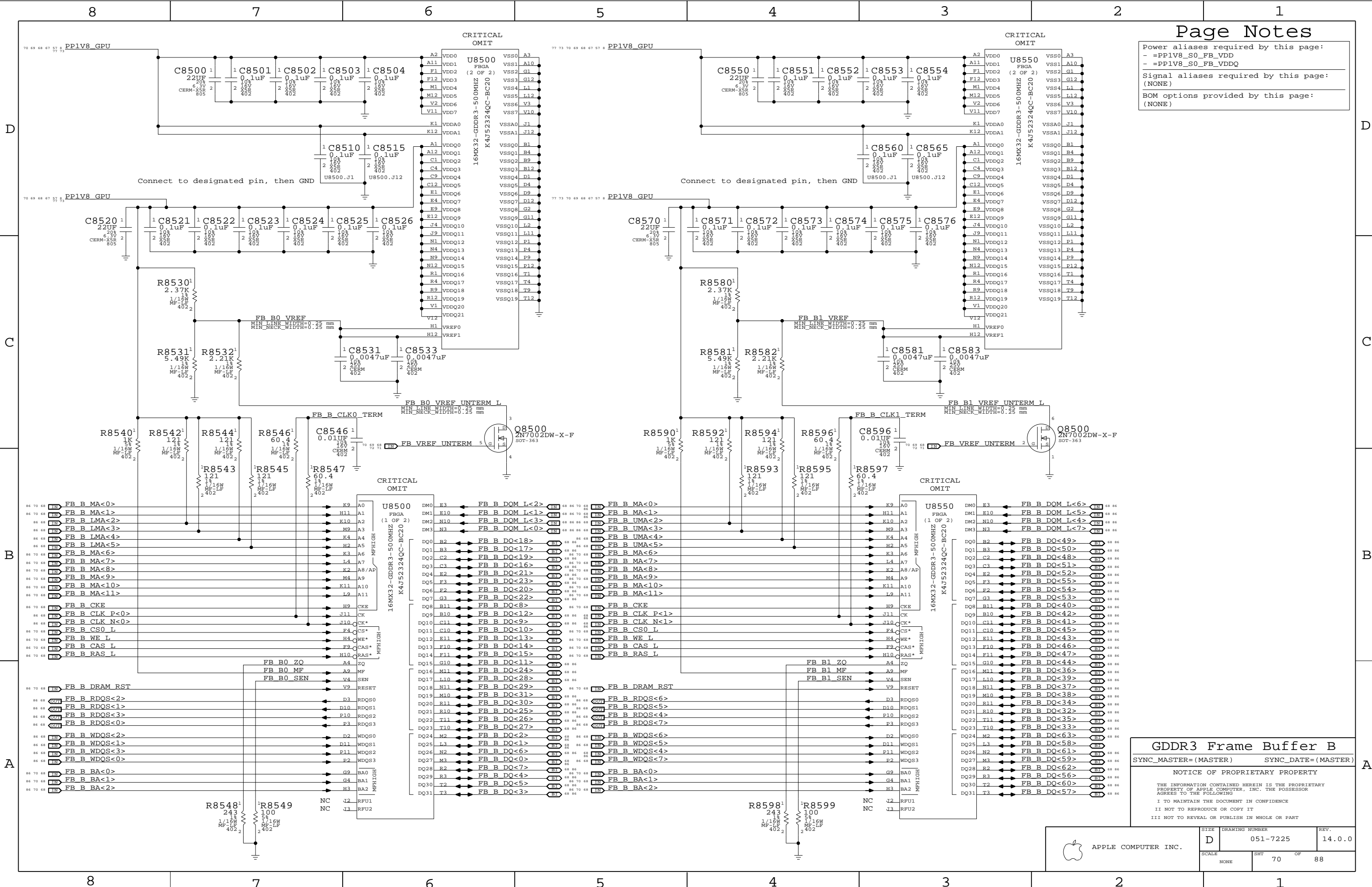
Power aliases required by this page:
- =PPIV8_S0_FB_VDD
- =PPIV8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)



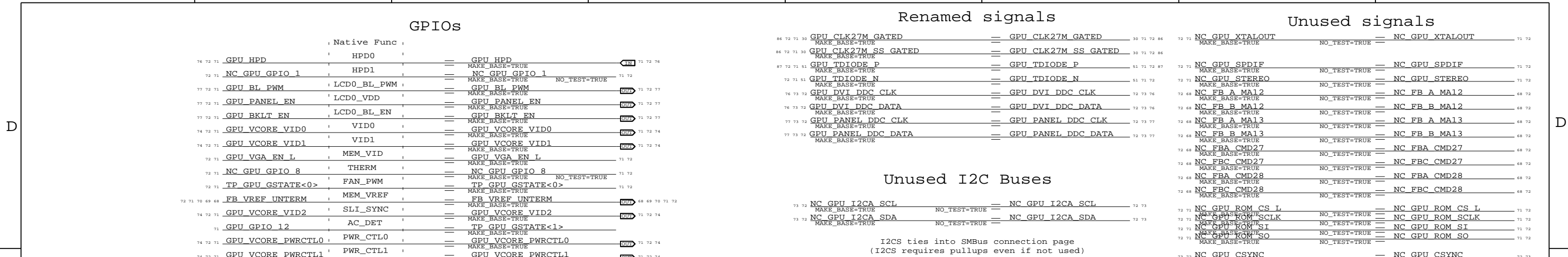
GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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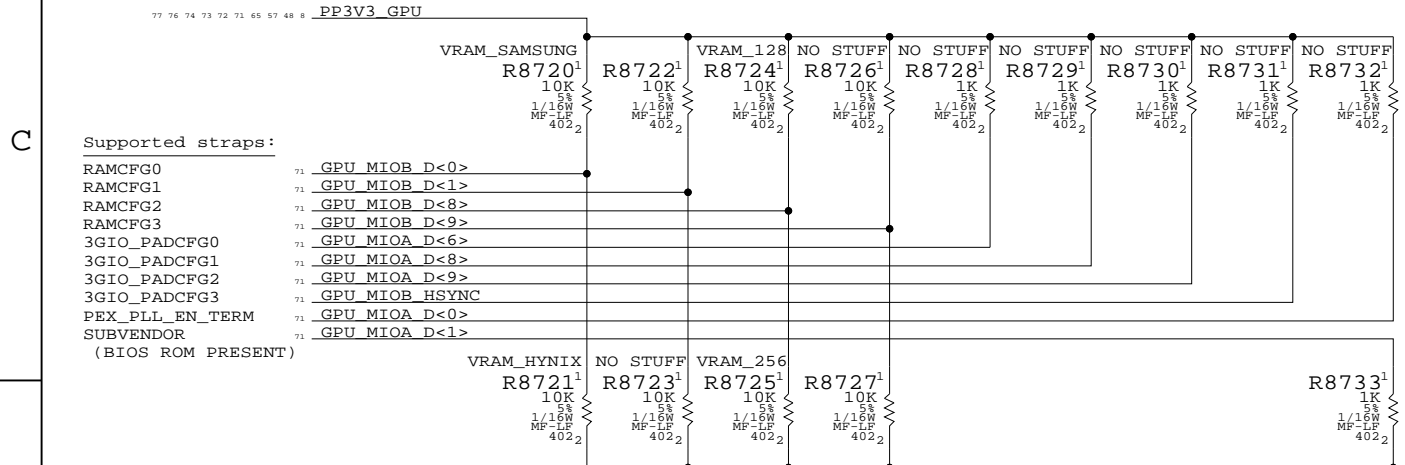
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	70	88	



Unused I2C Buses

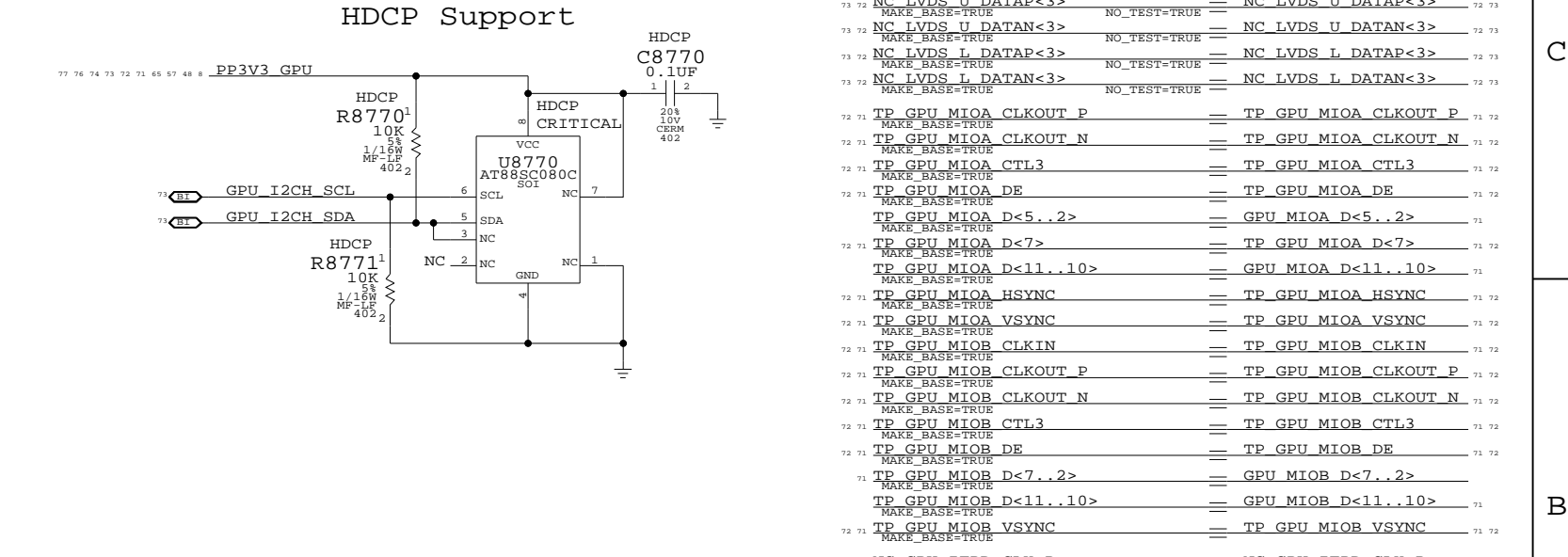
I2CS ties into SMBus connection page (I2CS requires pullups even if not used)

Config Straps

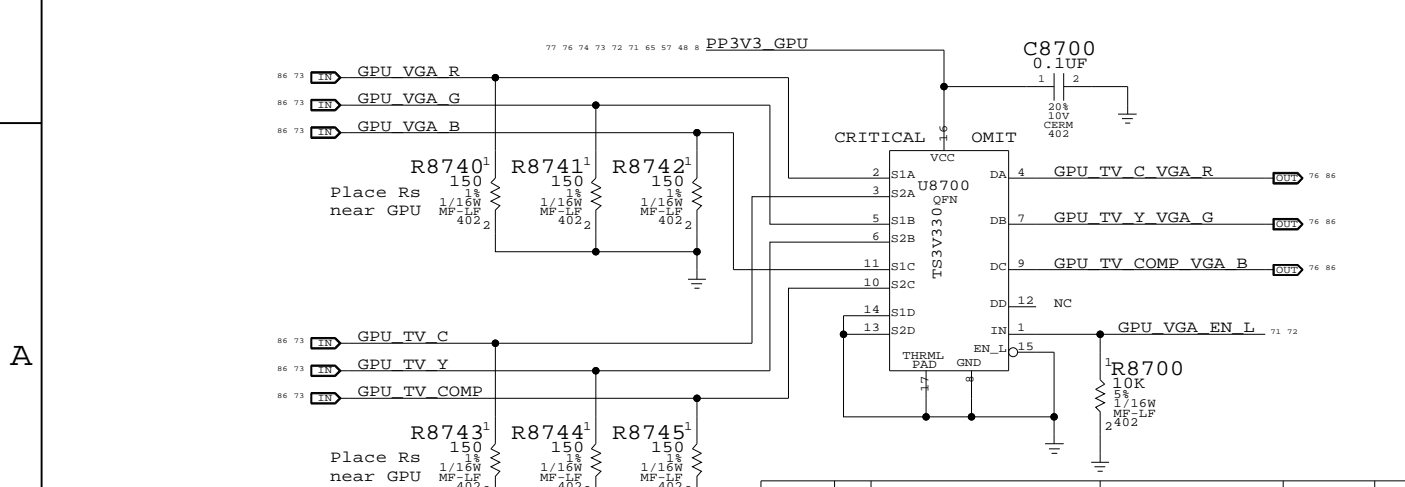


- Supported straps:**
- RAMCFG0 GPU MIOB D<0>
 - RAMCFG1 GPU MIOB D<1>
 - RAMCFG2 GPU MIOB D<8>
 - RAMCFG3 GPU MIOB D<9>
 - 3GIO_PADCFG0 GPU MIOA D<6>
 - 3GIO_PADCFG1 GPU MIOA D<8>
 - 3GIO_PADCFG2 GPU MIOA D<9>
 - 3GIO_PADCFG3 GPU MIOB HSYNC
 - PEX_PLL_EN_TERM GPU MIOA D<0>
 - SUBVENDOR GPU MIOA D<1>

- Straps not supported:**
- CRYSTAL MIOB D<2>
 - TVMODE<2..0> MIOB D<6,10,7>
 - PCI_DEVID<4..0> MIOB_CTL3, MIOB D<11,3,5,4>
 - USER<3..0> MIOA D<5..2>
 - ROMTYPE<1..0> MIOB_VSYNC, MIOB D<10>
 - SLOT_CLOCK_CFG MIOA_HSYNC
 - PCI_IOBAR MIOB D<7>
 - BAR2_SIZE MIOB_DE



Analog Video Mux



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35381718	1	IC,TS3V340,QUAD VIDEO SW,QFN16	U8700	CRITICAL	
PART NUMBER	18	ALTERNATE FOR PART NUMBER	REF DES	COMMENTS:	
35381579		35381718	ALL (U8700)	TS3V340 alt to TS3V340	

TMDS Backdrive Protection



Unused Clocks

GPU_CLK27M_SS_GATED	GPU_SS_INT
GPU_XTALOUTBUFF	R8780
	R8781

GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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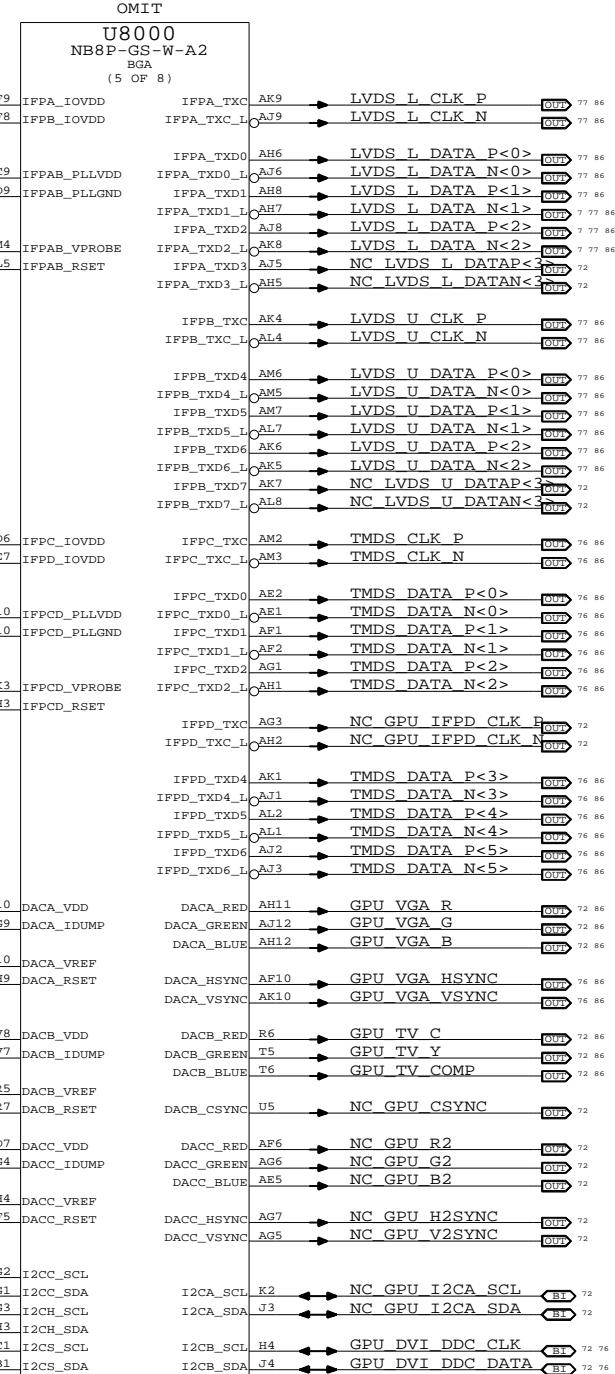
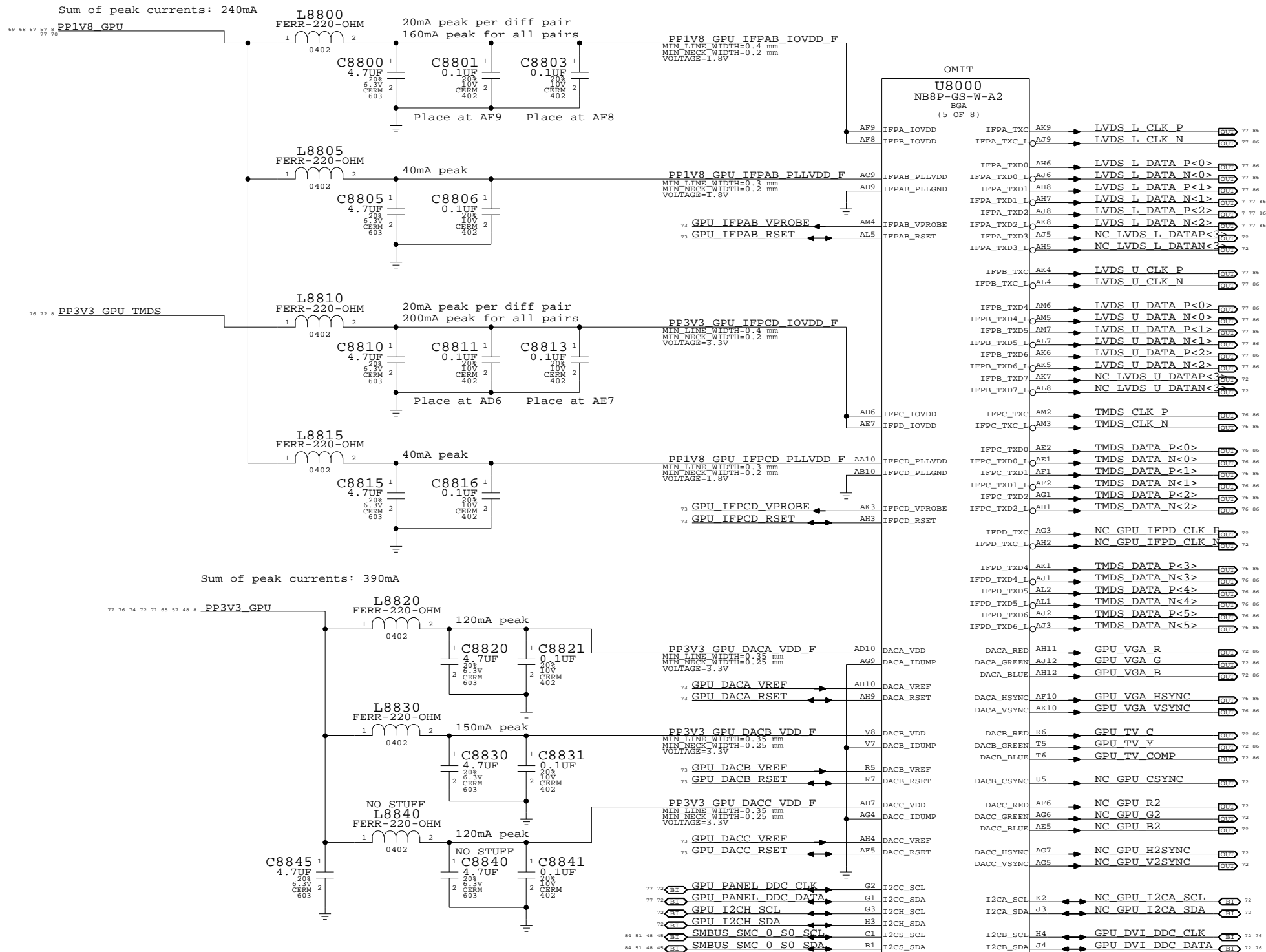
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	88
NONE	72		

Page Notes

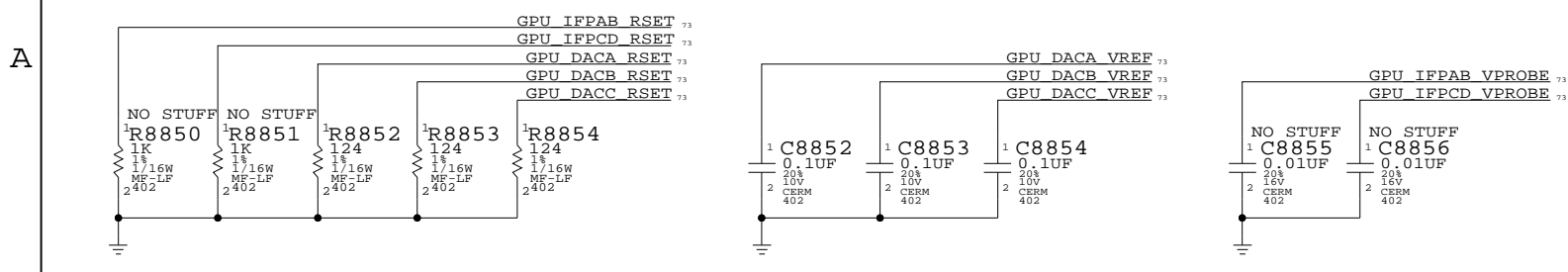
Power aliases required by this page:
 - =PP1V8_GPU_IFPX
 - =PP3V3_GPU_IFPCD_IOVDD
 - =PP3V3_GPU_DAC

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb



NV G84M Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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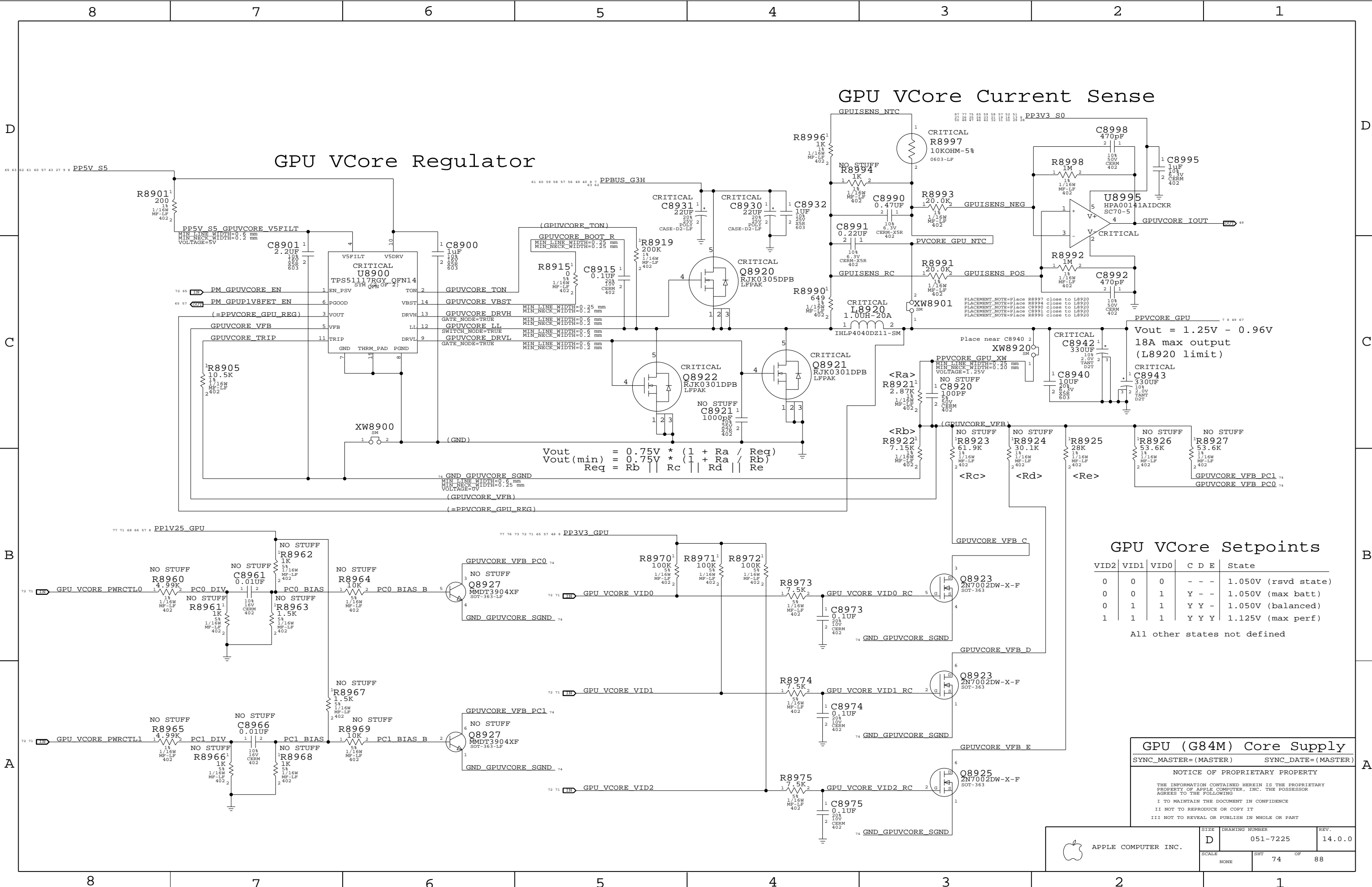
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	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	73	88	

GPU VCore Regulator

GPU VCore Current Sense



$$V_{out} = 0.75V * (1 + R_a / R_{eq})$$

$$V_{out}(\min) = 0.75V * (1 + R_a / R_b)$$

$$R_{eq} = R_b || R_c || R_d || R_e$$

GPU VCore Setpoints

VID2	VID1	VID0	C	D	E	State
0	0	0	-	-	-	1.050V (rsvd state)
0	0	1	Y	-	-	1.050V (max batt)
0	1	1	Y	Y	-	1.050V (balanced)
1	1	1	Y	Y	Y	1.125V (max perf)

All other states not defined

GPU (G84M) Core Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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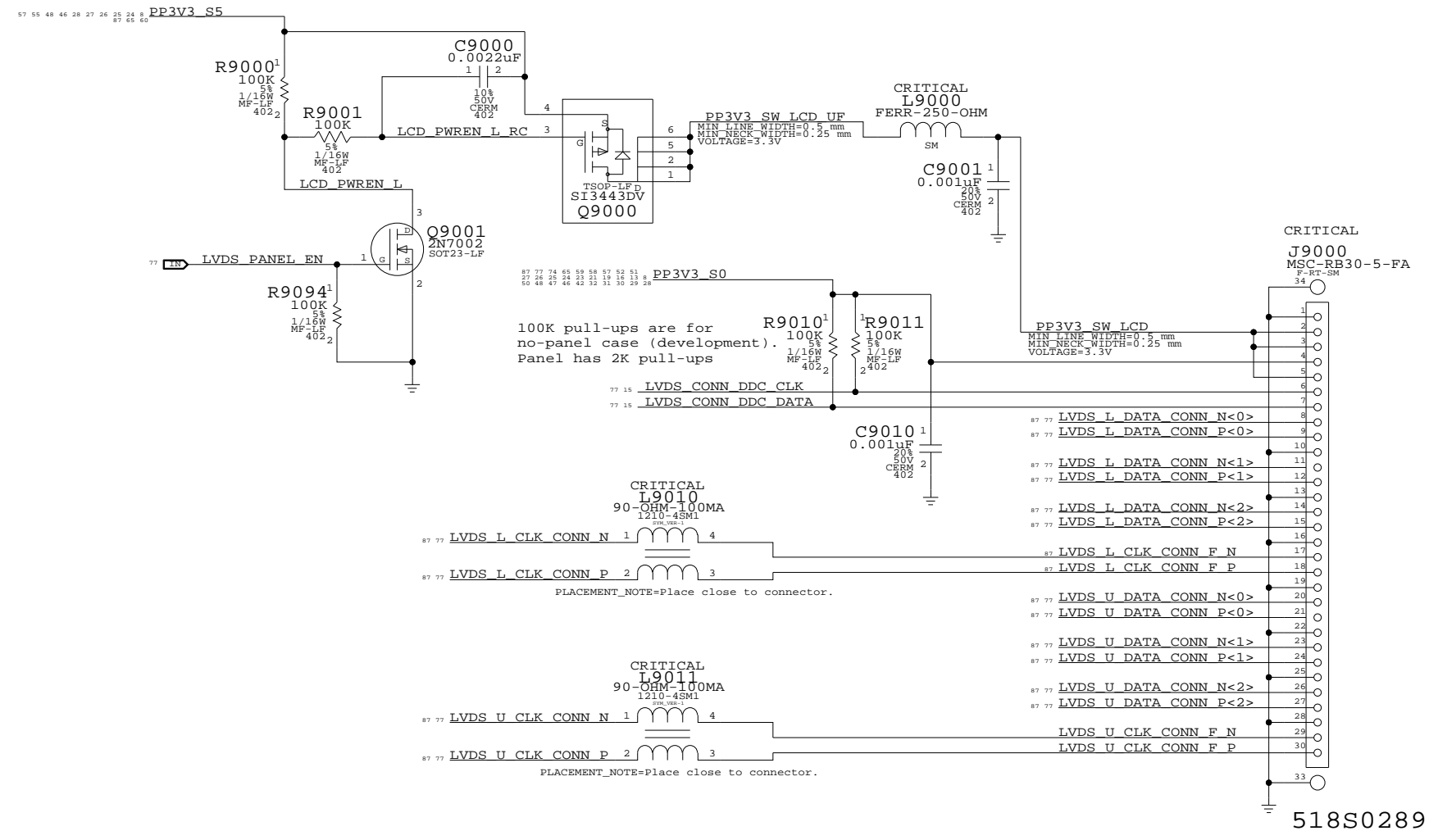
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SCALE	SHT	OF	
NONE	74	88	

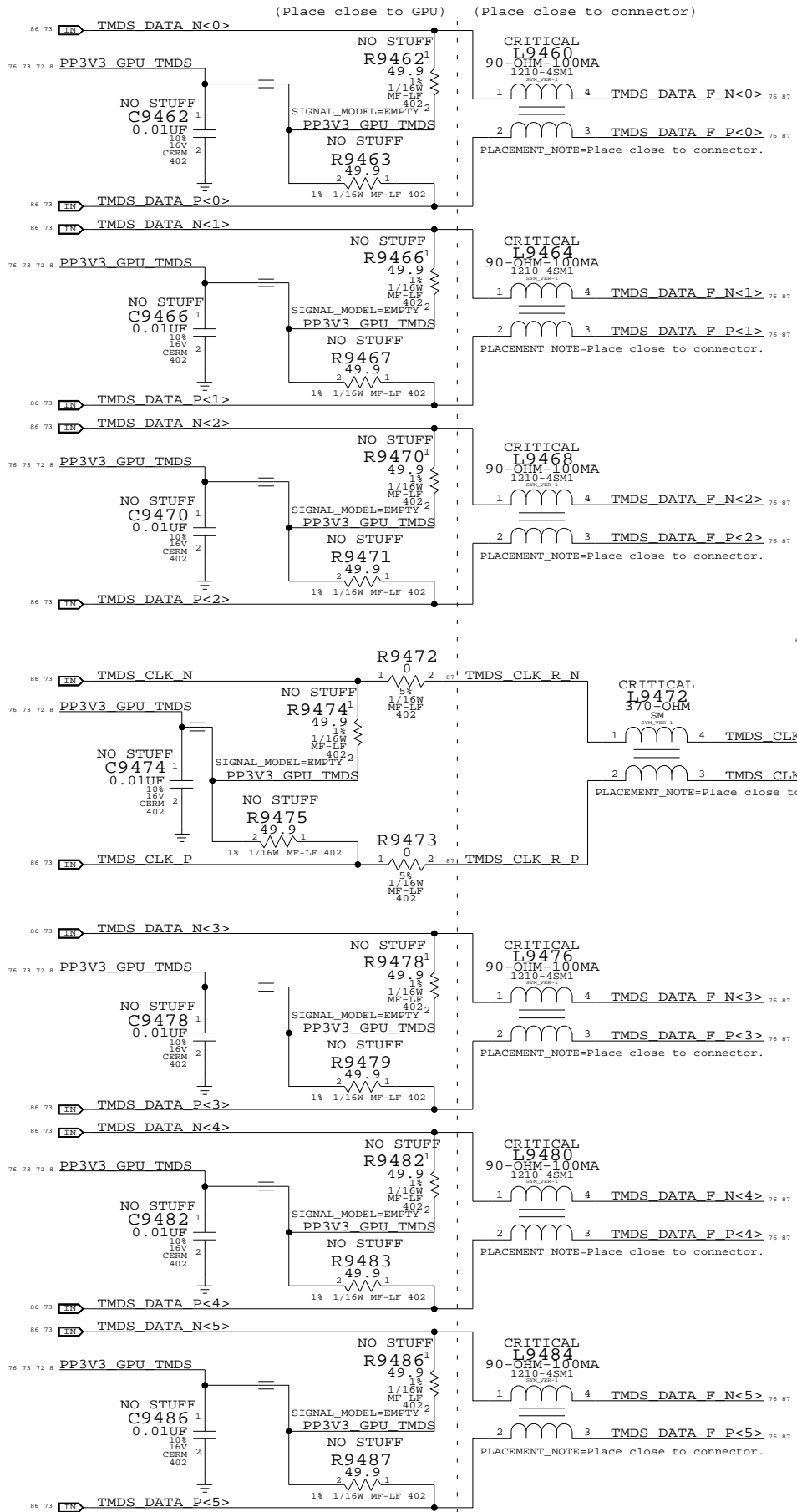
LCD (LVDS) INTERFACE



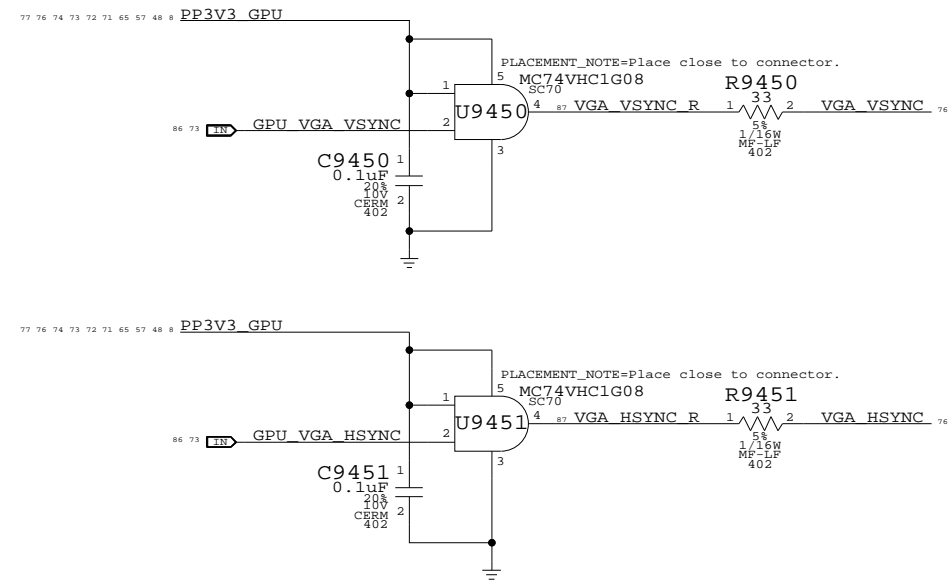
LVDS Display Connector
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7225	14.0.0
SCALE	SHT 75 OF 88		
NONE			

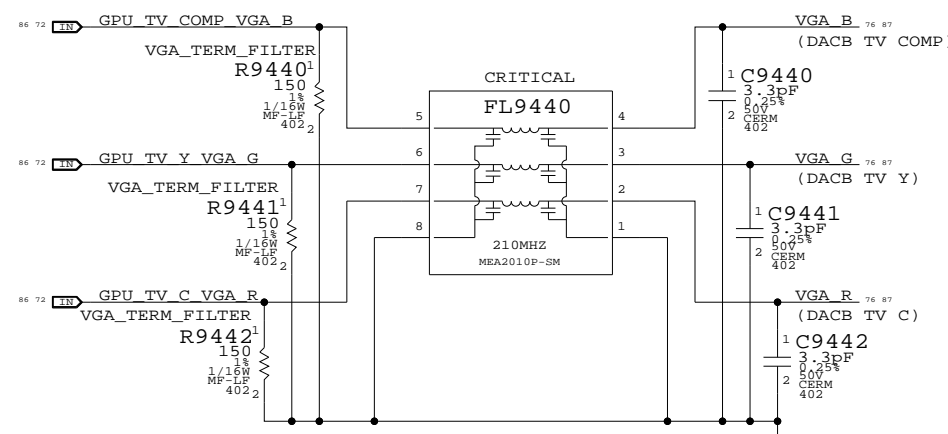
TMDS Filtering



VGA SYNC Buffers

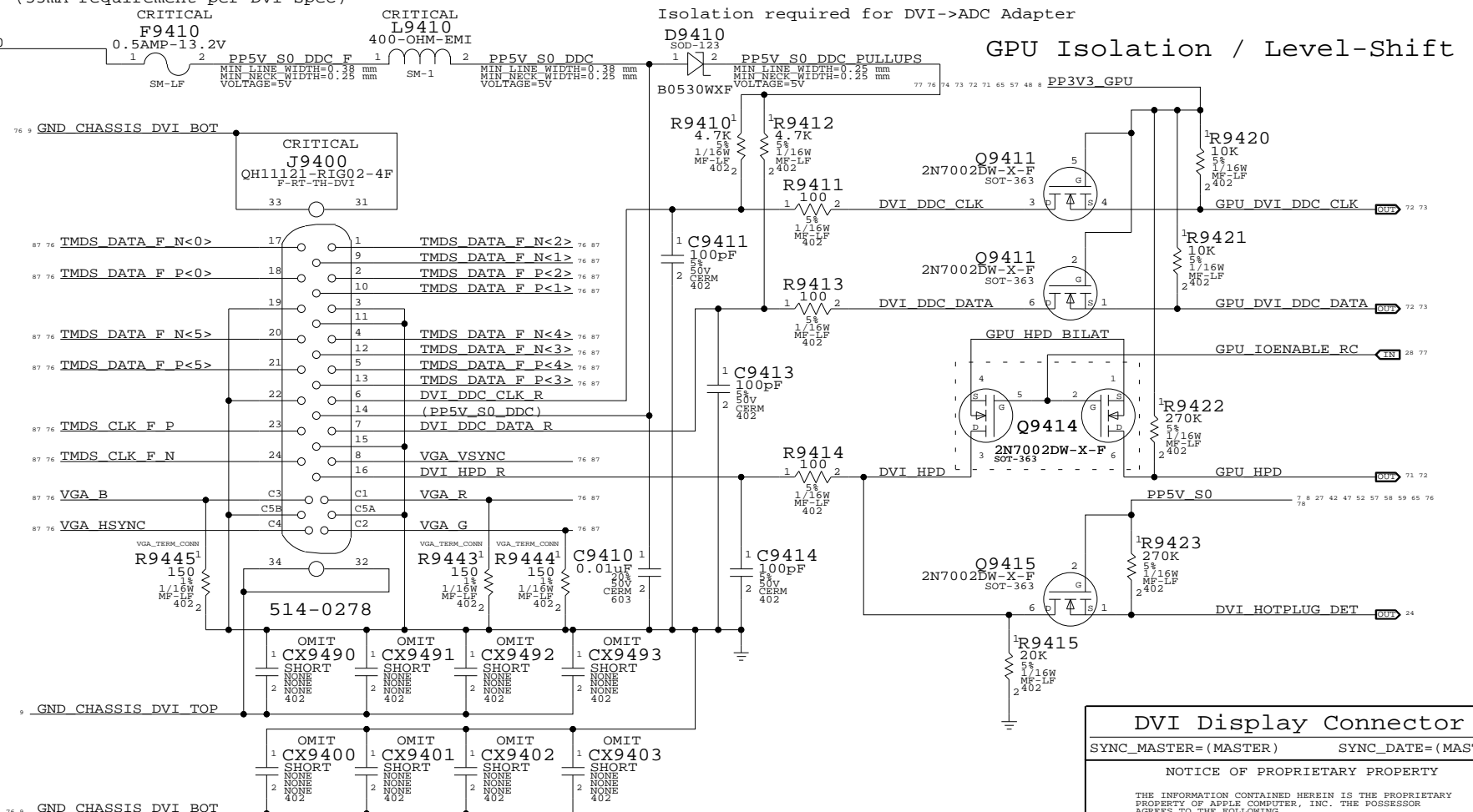


ANALOG FILTERING PLACE CLOSE TO CONNECTOR



DVI INTERFACE

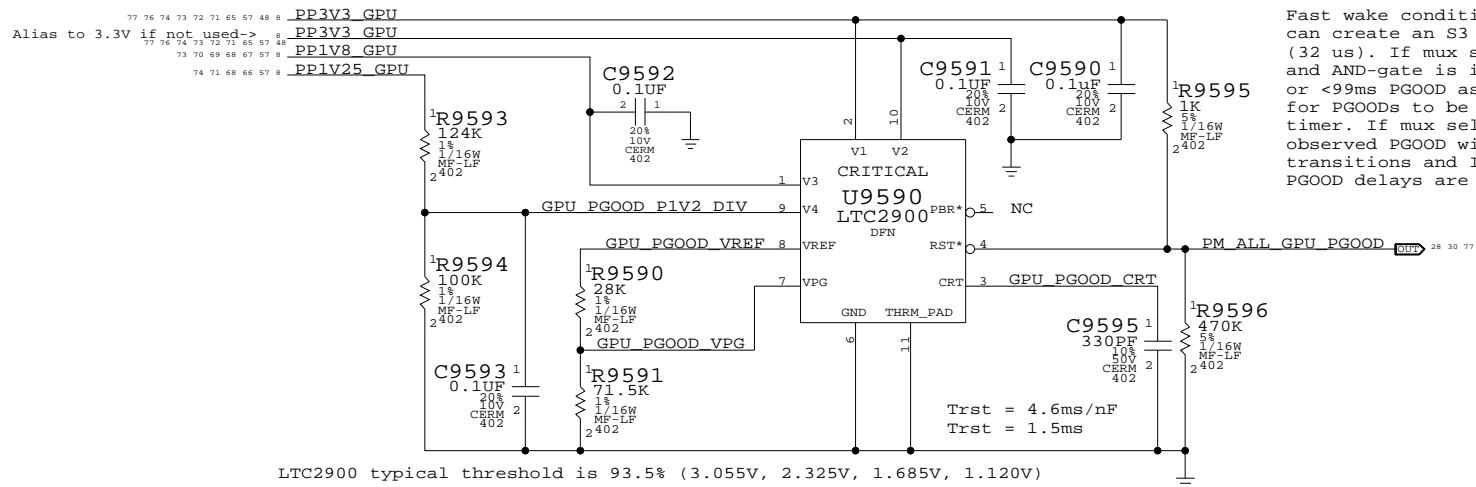
DVI DDC Current Limit (55mA requirement per DVI spec)



DVI Display Connector
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PGOOD Monitor for GPU Rails

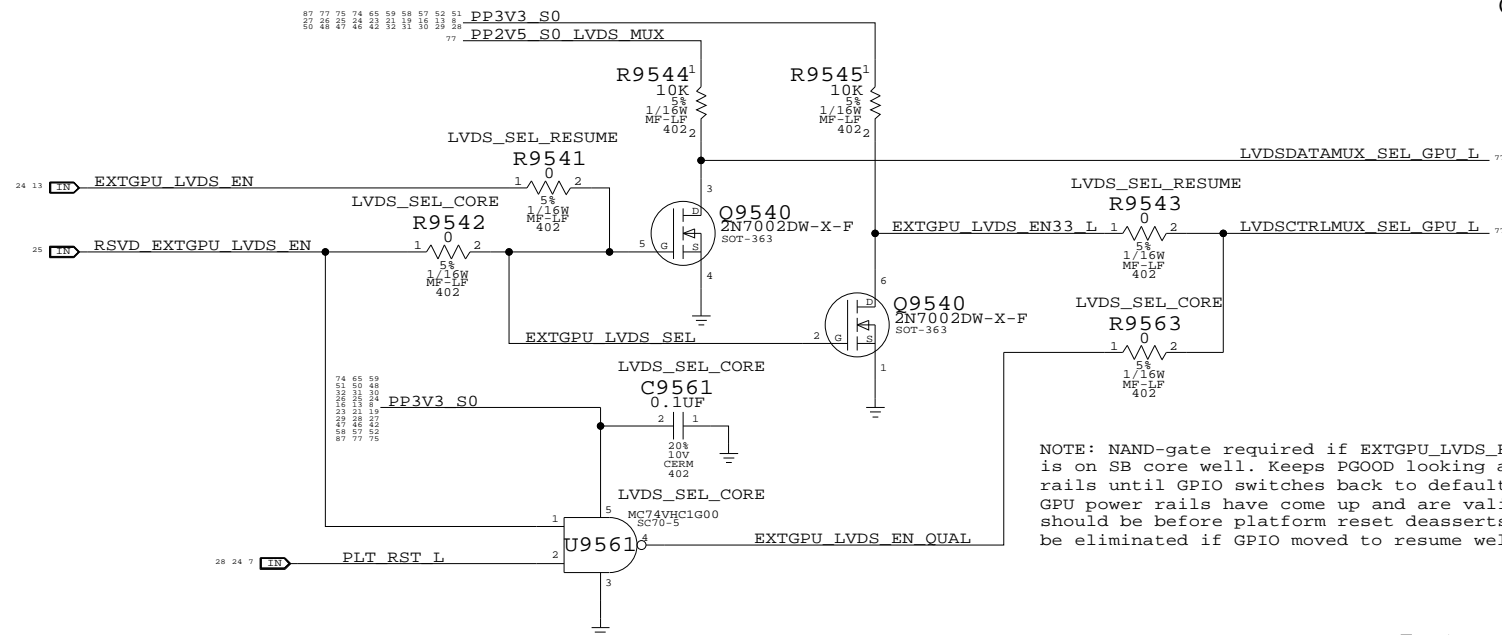
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Past wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

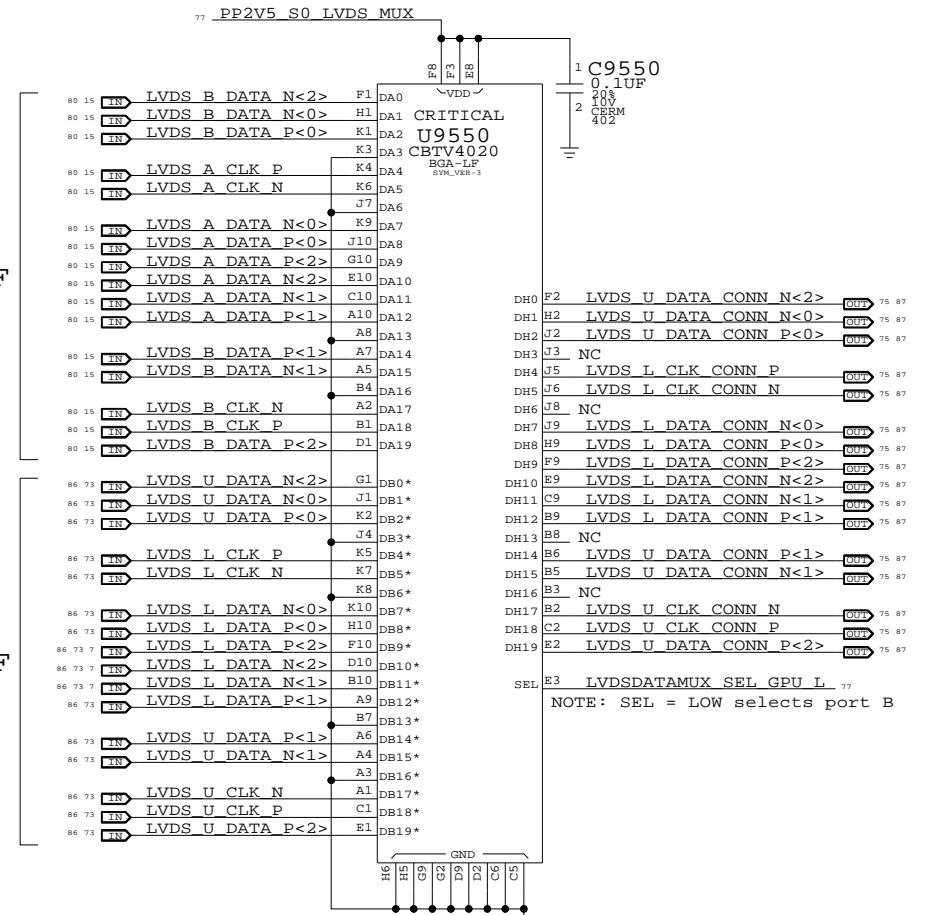
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

Mux Select Conditioning



NOTE: NAND-gate required if EXTGPU LVDS_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

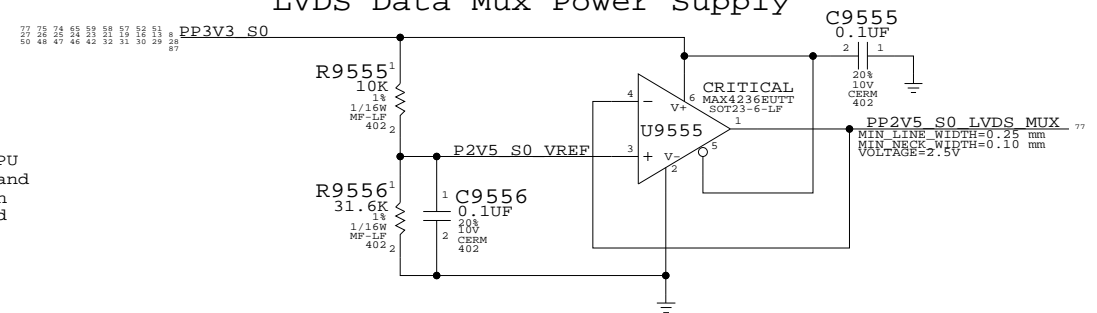
LVDS I/F Mux



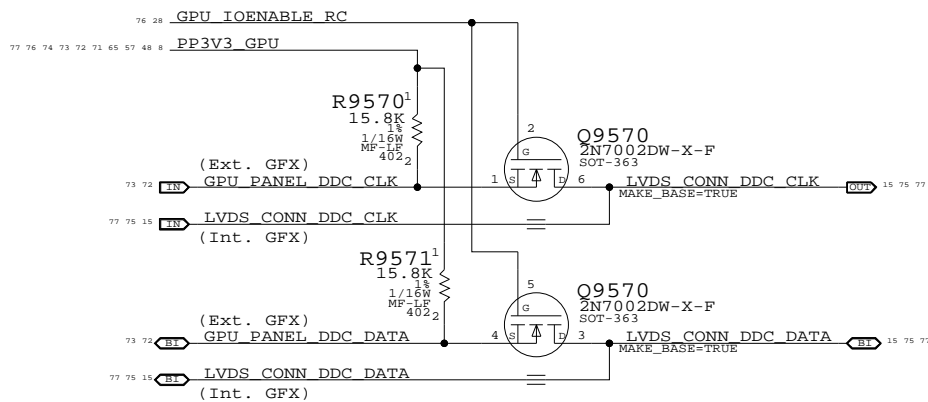
NB LVDS I/F

GPU LVDS I/F

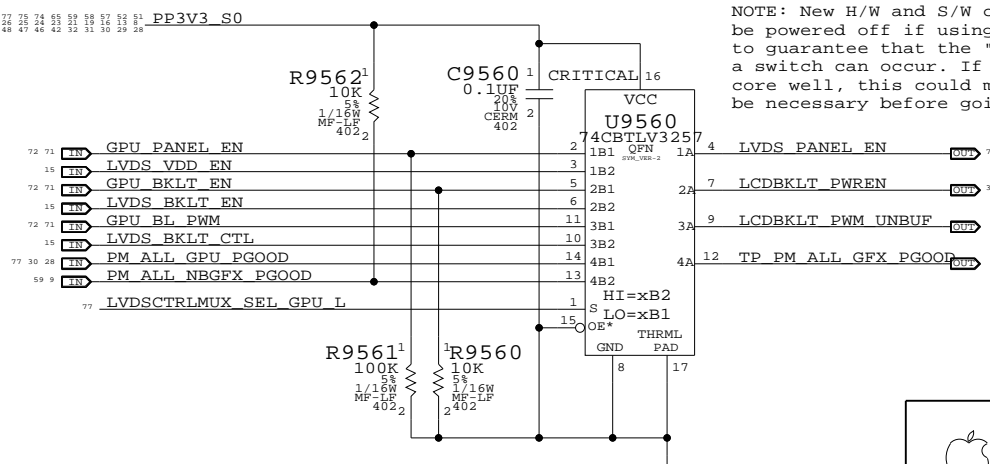
LVDS Data Mux Power Supply



GPU DDC Pass FETs



Panel/Backlight Control Mux

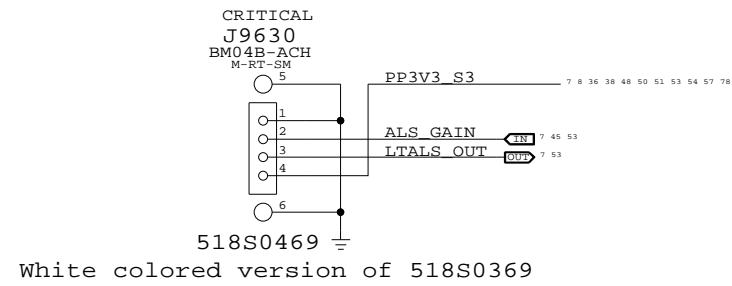


NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

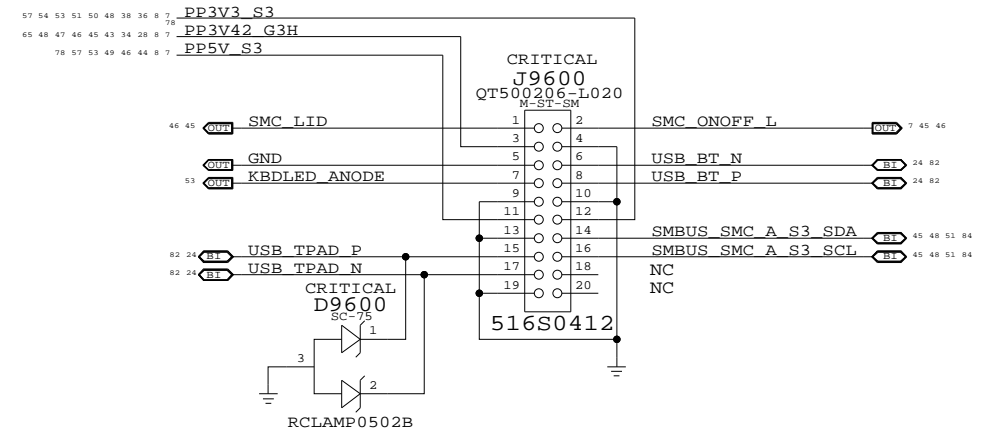
LVDS Interface Mux
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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SCALE	SHT	OF	
NONE	77	OF	88

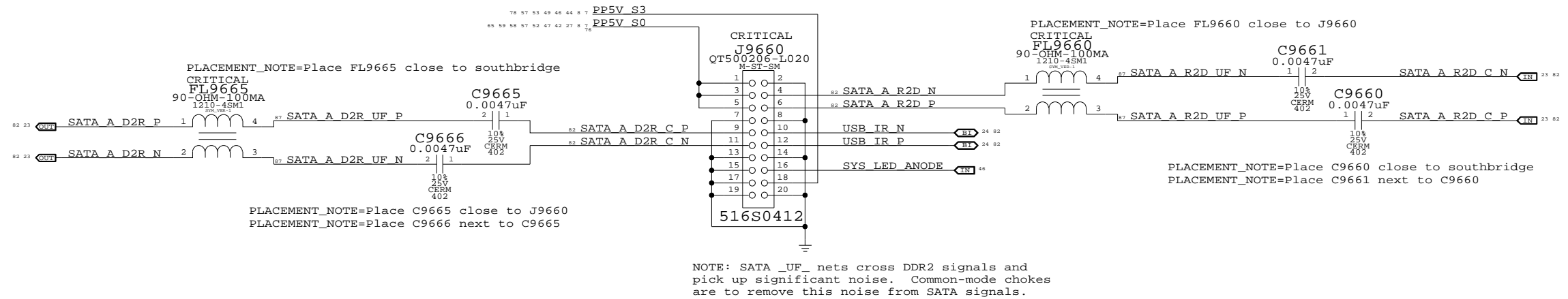
Left ALS Connector



Top-Case Connector



SATA HDD & IR & SIL Flex Connector



M75 Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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SCALE	NONE	SHT	78 OF 88

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BRQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 58
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FRGM_SB	CPU_55S		CPU INTR	10 23
CPU_FRGM_SB	CPU_55S		CPU NMI	10 23
CPU_FRGM_SB	CPU_55S		CPU A20M L	10 23
CPU_FRGM_SB	CPU_55S		CPU DPSTP L	7 10 23
CPU_FRGM_SB	CPU_55S		CPU IGNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FRGM_SB	CPU_55S		CPU SMI L	10 23
CPU_FRGM_SB	CPU_55S		CPU STPCLK L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	7 8
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TEST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_100D	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 84
CLK_FSB_100D	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 84
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
CPU_VID<6..0>	CPU_55S	CPU_2T01	CPU VID<6..0>	11 12
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 58
CPU_27P4S	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	58
CPU_27P4S	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	58

CPU/FSB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	79	88	

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
 CRT & TVDAC signal single-ended impedance varies by location:
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.
 - 50-ohm +/- 15% from first to second termination resistor.
 - 55-ohm +/- 15% from second termination resistor to connector.
 CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0> 66
	PCIE_100D	PCIE	PEG R2D N<15..0> 66
	PCIE_100D	PCIE	PEG R2D C P<15..0> 15 66
	PCIE_100D	PCIE	PEG R2D C N<15..0> 15 66
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0> 15 66
	PCIE_100D	PCIE	PEG D2R N<15..0> 15 66
	PCIE_100D	PCIE	PEG D2R C P<15..0> 66
	PCIE_100D	PCIE	PEG D2R C N<15..0> 66
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0> 16 24
	DMI_100D	DMI	DMI N2S N<3..0> 16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0> 16 24
	DMI_100D	DMI	DMI S2N N<3..0> 16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P 15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N 15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0> 15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0> 15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3> 15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3> 15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P 15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N 15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0> 15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0> 15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3> 15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3> 15 77
LVDS_IBG		LVDS	LVDS IBG 15 22
CRT_TVO_IREF		CRT	CRT TVO IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R
TV_A_DAC	CRT_50S	TVDAC	TV A DAC
TV_B_DAC	CRT_50S	TVDAC	TV B DAC
TV_C_DAC	CRT_50S	TVDAC	TV C DAC

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	80	88

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM CLK N<2..0>	16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	17 31
	MEM_85D	MEM_DQS	MEM A DQS N<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM CLK N<5..3>	16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CKE<4..3>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM CS L<3..2>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	17 32
	MEM_85D	MEM_DQS	MEM B DQS N<7>	17 32

Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1 L 23 42
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3 L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDIOW L 23 42
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDACK L 23 42
IDE_CNVL	IDE_55S	IDE	IDE_PDDREO 23 42
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D C P 23 78
SATA_100D	SATA	SATA	SATA_A_R2D C N 23 78
SATA_100D	SATA	SATA	SATA_A_R2D P 78
SATA_100D	SATA	SATA	SATA_A_R2D N 78
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R P 23 78
SATA_100D	SATA	SATA	SATA_A_D2R N 23 78
SATA_100D	SATA	SATA	SATA_A_D2R C P 78
SATA_100D	SATA	SATA	SATA_A_D2R C N 78
SATA_B_R2D	SATA_100D	SATA	TP_SATA_B_R2DP 23 42
SATA_100D	SATA	SATA	TP_SATA_B_R2DN 23 42
SATA_100D	SATA	SATA	SATA_B_R2D P 23 42
SATA_100D	SATA	SATA	SATA_B_R2D N 23 42
SATA_B_D2R	SATA_100D	SATA	TP_SATA_B_D2RP 23 42
SATA_100D	SATA	SATA	TP_SATA_B_D2RN 23 42
SATA_100D	SATA	SATA	SATA_B_D2R C P 23 42
SATA_100D	SATA	SATA	SATA_B_D2R C N 23 42
SATA_C_R2D	SATA_100D	SATA	TP_SATA_C_R2DP 23 42
SATA_100D	SATA	SATA	TP_SATA_C_R2DN 23 42
SATA_100D	SATA	SATA	SATA_C_R2D P 23 42
SATA_100D	SATA	SATA	SATA_C_R2D N 23 42
SATA_C_D2R	SATA_100D	SATA	TP_SATA_C_D2RP 23 42
SATA_100D	SATA	SATA	TP_SATA_C_D2RN 23 42
SATA_100D	SATA	SATA	SATA_C_D2R C P 23 42
SATA_100D	SATA	SATA	SATA_C_D2R C N 23 42
SATA_RBIAS	SATA_55S		SATA_RBIAS 23 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 23 34
HDA_55S	HDA	HDA	HDA_BIT_CLK R 23 34
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 23 34
HDA_55S	HDA	HDA	HDA_SYNC R 23 34
HDA_RST_L	HDA_55S	HDA	HDA_RST L 23 34
HDA_55S	HDA	HDA	HDA_RST L R 23 34
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 23 34
HDA_55S	HDA	HDA	HDA_SDIN CODEC 23 34
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 23 34
HDA_55S	HDA	HDA	HDA_SDOUT R 23 34
USB_EXTN	USB_90D	USB	USB_EXTN P 24 43
USB_90D	USB	USB	USB_EXTN N 24 43
USB_90D	USB	USB	USB_EXTN MUXED P 24 43
USB_90D	USB	USB	USB_EXTN MUXED N 24 43
USB_MINI	USB_90D	USB	USB_MINI P 24 34
USB_90D	USB	USB	USB_MINI N 24 34
USB_EXTD	USB_90D	USB	USB_WWAN P 7 24 44
USB_90D	USB	USB	USB_WWAN N 7 24 44
USB_CAMERA	USB_90D	USB	USB_CAMERA P 7 24 44
USB_90D	USB	USB	USB_CAMERA N 7 24 44
USB_BT	USB_90D	USB	USB_BT P 24 78
USB_90D	USB	USB	USB_BT N 24 78
USB_TPAD	USB_90D	USB	USB_TPAD P 24 78
USB_90D	USB	USB	USB_TPAD N 24 78
USB_IR	USB_90D	USB	USB_IR P 24 78
USB_90D	USB	USB	USB_IR N 24 78
USB_EXTB	USB_90D	USB	USB_EXTB P 24 34
USB_90D	USB	USB	USB_EXTB N 24 34
USB_EXCARD	USB_90D	USB	USB_EXCARD P 24 34
USB_90D	USB	USB	USB_EXCARD N 24 34
USB_EXTC	USB_90D	USB	TP_USB_EXTCP 9 24
USB_90D	USB	USB	TP_USB_EXTCN 9 24
USB_RBIAS	USB_60S		USB_RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMBUS_SB_SCL 25 29 31 32 34 48
SMB_SB_SDA	SMB_55S	SMB	SMBUS_SB_SDA 25 29 31 32 34 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMBUS_SB_ME_SCL 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMBUS_SB_ME_SDA 25 48
SPI_SCLK	SPI_55S	SPI	SPI_SCLK R 24 55
SPI_55S	SPI	SPI	SPI_SCLK 55
SPI_55S	SPI	SPI	SPI_A_SCLK R 55
SPI_55S	SPI	SPI	SPI_B_SCLK R 55
SPI_SI	SPI_55S	SPI	SPI_SI R 24 55
SPI_55S	SPI	SPI	SPI_SI 55
SPI_55S	SPI	SPI	SPI_A_SI R 55
SPI_55S	SPI	SPI	SPI_B_SI R 55
SPI_SO	SPI_55S	SPI	SPI_SO 24 55
SPI_55S	SPI	SPI	SPI_A_SO R 55
SPI_55S	SPI	SPI	SPI_B_SO R 55
SPI_55S	SPI	SPI	SPI_B_SO R 55
SPI_CE_L0	SPI_55S	SPI	SPI_CE R L<0> 24 55
SPI_55S	SPI	SPI	SPI_CE L<0> 55
SPI_CE_L1	SPI_55S	SPI	SPI_CE R L<1> 55
SPI_55S	SPI	SPI	SPI_CE L<1> 55

SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7225	14.0.0
	SHT	OF	
	82	88	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	24
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	7 24 38 47
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	24
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT PIROC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT PIROD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT PIROF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	24 34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C N	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	24 34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R N	24 34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D P	35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C P	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

SB Constraints (2 of 2)

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	14.0.0
SCALE	SHT	OF	
NONE	83	88	

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CK505_CPUH	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 29 30 84
CK505_CPUN	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 29 30 84
CK505_NBP	CLK_FSB_100D	CLK_FSB	FSB CLK NB P	7 14 29 30 84
CK505_NBN	CLK_FSB_100D	CLK_FSB	FSB CLK NB N	7 14 29 30 84
CK505_ITP	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 79 84
CK505_ITN	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 79 84
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505 PCIF0 CLK ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505 PCIF1 CLK	29 30
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505 PCI1 CLK	29 30
CK505_PCI2	CLK_MED_55S	CLK_MED	TP CK505 PCI2 CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505 PCI3 CLK	29 30
CK505_PCI4	CLK_MED_55S	CLK_MED	TP CK505 PCI4 CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505 PCI5 CLK FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505 48M FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505 REF0 FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505 CLK27M	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505 CLK27M SS	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPLLSS P	7 16 22 29 30 84
	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPLLSS N	7 16 22 29 30 84
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU P	9 29 30 66 84
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU N	9 29 30 66 84
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI P	24 29 30 84
	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI N	24 29 30 84
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	29 30 34 84
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	29 30 34 84
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA P	23 29 30 84
	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA N	23 29 30 84
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE P	7 16 29 30 84
	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE N	7 16 29 30 84
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	29 30 34 84
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	29 30 34 84
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M SRC7P	29 30
	CLK_PCIE_100D	CLK_PCIE	TP PCIE CLK100M SRC7N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P	29 30 35 84
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N	29 30 35 84
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10 29 30 84
(CK505_CPUN)	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10 29 30 84
(CK505_NBP)	CLK_FSB_100D	CLK_FSB	FSB CLK NB P	7 14 29 30 84
(CK505_NBN)	CLK_FSB_100D	CLK_FSB	FSB CLK NB N	7 14 29 30 84
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP CLK P	13 29 30 79 84
(CK505_ITN)	CLK_FSB_100D	CLK_FSB	XDP CLK N	13 29 30 79 84
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI CLK33M LPCPLUS	7 30 47
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI CLK33M SB	24 30
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI CLK33M FW	30 38
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI CLK33M TPM	30 45
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI CLK33M SMC	30 45
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB CLK48M USBCTLR	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB CLK14P3M TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505 FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505 FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB CLK96M DOT P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB CLK96M DOT N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPLLSS P	7 16 22 29 30 84
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M DPLLSS N	7 16 22 29 30 84
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU P	9 29 30 66 84
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M GPU N	9 29 30 66 84
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI P	24 29 30 84
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M DMI N	24 29 30 84
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	29 30 34 84
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	29 30 34 84
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA P	23 29 30 84
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB CLK100M SATA N	23 29 30 84
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE P	7 16 29 30 84
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB CLK100M PCIE N	7 16 29 30 84
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	29 30 34 84
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	29 30 34 84
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	CK505 SRC7 is project-specific	
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P	29 30 35 84
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N	29 30 35 84

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC A S3_SCL	45 48 51 78
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC A S3_SDA	45 48 51 78
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC B S0_SCL	34 45
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC B S0_SDA	34 45
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC 0 S0_SCL	45 48 51 73
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC 0 S0_SDA	45 48 51 73
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC BSA_SCL	7 45 48 56
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC BSA_SDA	7 45 48 56
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC MGMT_SCL	45 48 54
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC MGMT_SDA	45 48 54

Clock & SMC Constraints

SYNC_MASTER=T9_NAME SYNC_DATE=01/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	14.0.0
SCALE	SHT	OF
NONE	84	88

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
EW_D_CTL	EW_55S	FW	FW LINK<7..0>
EW_D_CTL	EW_55S	FW	FW CTL<1..0>
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW LINK LCLK
EW_LCLK	CLK_MED_55S	CLK_MED	CLKFW PHY LCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW LINK PCLK 38 39
EW_PCLK	CLK_MED_55S	CLK_MED	CLKFW PHY PCLK 38 39
EW_LKON	EW_55S	FW	FW LKON
EW_LKON	EW_55S	FW	FW LKON R
EW_LPS	EW_55S	FW	FW LPS 38 39
EW_LREQ	EW_55S	FW	FW LREQ 38 39
EW_PINT	EW_55S	FW	FW PINT 38 39
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI R
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW XI
EW_0_TPA	EW_110D	EW_TP	FW PORT0 TPA P 39 41
EW_0_TPA	EW_110D	EW_TP	FW PORT0 TPA N 39 41
EW_0_TPB	EW_110D	EW_TP	FW PORT0 TPB P 39 41
EW_0_TPB	EW_110D	EW_TP	FW PORT0 TPB N 39 41
EW_1_TPA	EW_110D	EW_TP	FW PORT1 TPA P 39 41
EW_1_TPA	EW_110D	EW_TP	FW PORT1 TPA N 39 41
EW_1_TPB	EW_110D	EW_TP	FW PORT1 TPB P 39 41
EW_1_TPB	EW_110D	EW_TP	FW PORT1 TPB N 39 41
Port 2 Not Used			

FireWire Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007


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NONE	85	88	

GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	68 69
FB_A_CLK_N	GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	68 69
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>	68 69
FB_B_CLK_N	GDDR3_80D	GDDR3_CLK	FB A CLK N<1>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<1..0>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<11..6>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A BA<2..0>	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A RAS L	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CAS L	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A WE L	68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A CKE	68 69
FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CS0 L	68 69
FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A DRAM_RST	68 69
FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB A LMA<5..2>	68 69
FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB A UMA<5..2>	68 69
FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<0>	68 69
FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<1>	68 69
FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<2>	68 69
FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<3>	68 69
FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<0>	68 69
FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<1>	68 69
FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<2>	68 69
FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<3>	68 69
FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<7..0>	68 69
FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<15..8>	68 69
FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<23..16>	68 69
FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<31..24>	68 69
FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM L<0>	68 69
FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM L<1>	68 69
FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM L<2>	68 69
FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM L<3>	68 69
FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<4>	68 69
FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<5>	68 69
FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<6>	68 69
FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<7>	68 69
FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<4>	68 69
FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<5>	68 69
FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<6>	68 69
FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<7>	68 69
FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<39..32>	68 69
FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<47..40>	68 69
FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<55..48>	68 69
FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<63..56>	68 69
FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM L<4>	68 69
FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM L<5>	68 69
FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM L<6>	68 69
FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM L<7>	68 69

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>	68 70
FB_C_CLK_N	GDDR3_80D	GDDR3_CLK	FB B CLK N<0>	68 70
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>	68 70
FB_D_CLK_N	GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<1..0>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<11..6>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B BA<2..0>	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B RAS L	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CAS L	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B WE L	68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B CKE	68 70
FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CS0 L	68 70
FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B DRAM_RST	68 70
FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB B LMA<5..2>	68 70
FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB B UMA<5..2>	68 70
FB_C_WDQS0	GDDR3_50SE	GDDR3_DQS	FB B WDQS<0>	68 70
FB_C_WDQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<1>	68 70
FB_C_WDQS2	GDDR3_50SE	GDDR3_DQS	FB B WDQS<2>	68 70
FB_C_WDQS3	GDDR3_50SE	GDDR3_DQS	FB B WDQS<3>	68 70
FB_C_RDQS0	GDDR3_50SE	GDDR3_DQS	FB B RDQS<0>	68 70
FB_C_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<1>	68 70
FB_C_RDQS2	GDDR3_50SE	GDDR3_DQS	FB B RDQS<2>	68 70
FB_C_RDQS3	GDDR3_50SE	GDDR3_DQS	FB B RDQS<3>	68 70
FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<7..0>	68 70
FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<15..8>	68 70
FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<23..16>	68 70
FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<31..24>	68 70
FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM L<0>	68 70
FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM L<1>	68 70
FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM L<2>	68 70
FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM L<3>	68 70
FB_D_WDQS0	GDDR3_50SE	GDDR3_DQS	FB B WDQS<4>	68 70
FB_D_WDQS1	GDDR3_50SE	GDDR3_DQS	FB B WDQS<5>	68 70
FB_D_WDQS2	GDDR3_50SE	GDDR3_DQS	FB B WDQS<6>	68 70
FB_D_WDQS3	GDDR3_50SE	GDDR3_DQS	FB B WDQS<7>	68 70
FB_D_RDQS0	GDDR3_50SE	GDDR3_DQS	FB B RDQS<4>	68 70
FB_D_RDQS1	GDDR3_50SE	GDDR3_DQS	FB B RDQS<5>	68 70
FB_D_RDQS2	GDDR3_50SE	GDDR3_DQS	FB B RDQS<6>	68 70
FB_D_RDQS3	GDDR3_50SE	GDDR3_DQS	FB B RDQS<7>	68 70
FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<39..32>	68 70
FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<47..40>	68 70
FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<55..48>	68 70
FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<63..56>	68 70
FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM L<4>	68 70
FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM L<5>	68 70
FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM L<6>	68 70
FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM L<7>	68 70

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED	30 71 72
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED	30 71 72
	LVDS_100D	LVDS	LVDS L CLK P	73 77
	LVDS_100D	LVDS	LVDS L CLK N	73 77
	LVDS_100D	LVDS	LVDS L DATA P<3..0>	73 77
	LVDS_100D	LVDS	LVDS L DATA N<3..0>	73 77
	LVDS_100D	LVDS	LVDS U CLK P	73 77
	LVDS_100D	LVDS	LVDS U CLK N	73 77
	LVDS_100D	LVDS	LVDS U DATA P<3..0>	73 77
	LVDS_100D	LVDS	LVDS U DATA N<3..0>	73 77
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK P	73 76
TMDS_CLK	TMDS_100D	TMDS	TMDS CLK N	73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA P<5..0>	73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS DATA N<5..0>	73 76
VGA_B_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R	72 76
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G	72 76
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B	72 76
	VGA_50S	VGA	GPU_VGA_R	72 73
	VGA_50S	VGA	GPU_VGA_G	72 73
	VGA_50S	VGA	GPU_VGA_B	72 73
	VGA_50S	VGA	GPU_TV_C	72 73
	VGA_50S	VGA	GPU_TV_Y	72 73
	VGA_50S	VGA	GPU_TV_COMP	72 73
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC	73 76
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC	73 76

GPU (G84M) Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	86	88	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	ENET_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	FW_POWER	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM	2.54 MM	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4, ISL10			0.100 MM	2.54 MM		

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
TMDS_100D	BGA	100_DIFF_BGA

SIM Card Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WWAN_SIM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
WWAN_SIM	*	=2:1_SPACING	?

M75 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P 34
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P 34
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N 34
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>
	ENET_100D	ENETCONN	ENETCONN_P<3..0> 37
	ENET_100D	ENETCONN	ENETCONN_N<3..0> 37
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P 41
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N 41
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P 78
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N 78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P 78
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N 78
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_P 43
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	NONE	D 051-7225	14.0.0
	SHT	OF	
	87	88	

M75 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2, ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

M75 Rule Definitions

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NONE	88	88	