

Myna II

<http://hobi-elektronika.net>

Project code: 91.4C201.001

PCB REVISION: 05216-SB

CLK GEN.
IDT CV125
3

Mobile CPU
Dothan
CLE-1.5G / Dothan2.13G
(CPU on board,no socket)
4, 5

G792
19

HOST BUS 533MHz

DDR II
400/533 MHz
11,12

DDR II
400/533 MHz
11,12

Alviso-GM

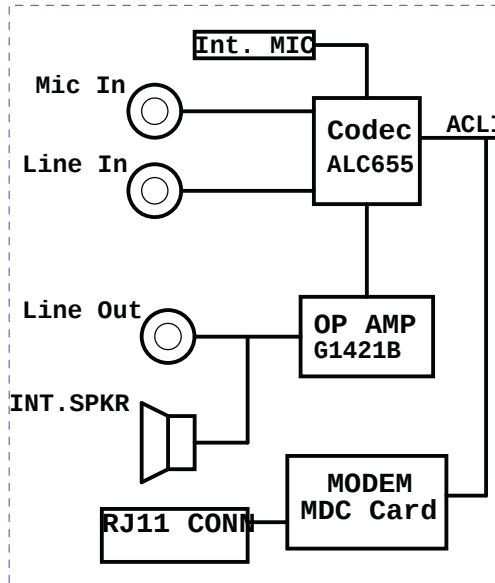
KI.91501.017

6,7,8,9,10

DMI I/F 100MHz

ICH6-M

Ver.: B2, KI.80101.011



IO Board

(co-lay with PCMCIA)

New card
29

PWR SW
TPS2231
29

PCI-E

PATA

two USB port
on IO Board

USB
3 PORT
21

MINI USB
Blue-tooth
21

HDD
20

NS
SIO
87392
31

FIR

KBC
Renesas RE144B
30

Touch
Pad
32

INT.
KB
32

BIOS ROM
4M BITS
PM49F004T-33VC
33

LPC
DEBUG
CONN.
33

TI
PCI 7411
1* Slot Cardbus
1* 1394
CardReader
24,25

PCMCIA I/F

PWR SW
TSP2220A
26

MS/MS Pro/
xD/ MMC/SD
5 in 1
26

Mini-PCI
802.11A/B/G
(only smaller)
30

LAN
Giga
BCM5788-M
22, 23

TXFM
23

RJ45 CONN
23

PCI BUS

LPC BUS

15,16,17,18

LVDS

TV
(EZ4 only)

LCD
13

RGB CRT

CRT
14

CH7307C

53-TMDS

DVI-D
(EZ4 only)
35

SYSTEM DC/DC TPS5130 41,42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO)
SYSTEM DC/DC ISL6227 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
TPS51100DGQ 43	
1D8V_S3	VTT_S0(0.9V)

MAXIM CHARGER MAX8725ETI 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 3.2A UP+5V 5V 100mA

CPU DC/DC ISL6218CV-T 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

Easy Port 4 (124 PIN)

AC IN RJ45-11 SEARIAL PORT CRT PRINTER PS2 MIC LINE IN LINE OUT TV OUT DVI PCIEx2 SMBUS
34, 35

<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Rev
BLOCK DIAGRAM	SB
Size	Document Number
Custom	Myna II
Date	Sheet
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Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott 1 = Dothan (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test Straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	CPU VTT Select	0 = 1.05V (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCTRL_DATA	SDVO Present	0 = No SDVO device present (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

- 1.CHECK P5[105V & 105V-AVDD]
- 2.CHECK P8[PM & GM]

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

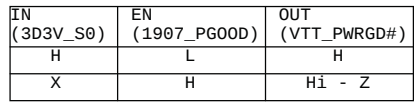
ICH6-M Integrated Pull-up and Pull-down Resistors

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCLK_PCM & PCLK_SIO
need equal length



3D3V_CLKGEN_S0

R155 1K R2

R152 DUMMY-R2 2

R371 DUMMY-R2 2

R154 DUMMY-R2 2

R153 DUMMY-R2 2

R372 DUMMY-R2 2

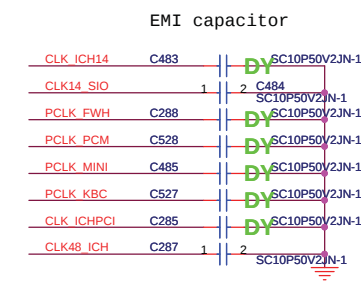
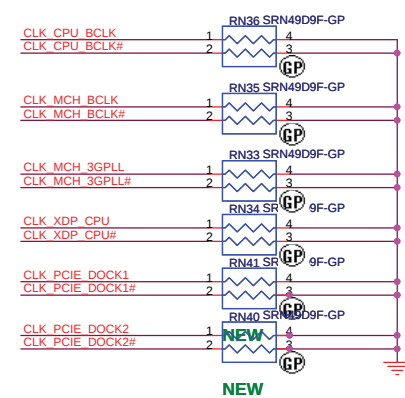
R373 DUMMY-R2 2

FS_A

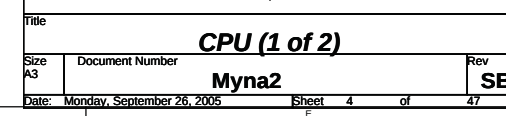
CPU_SEL1 7

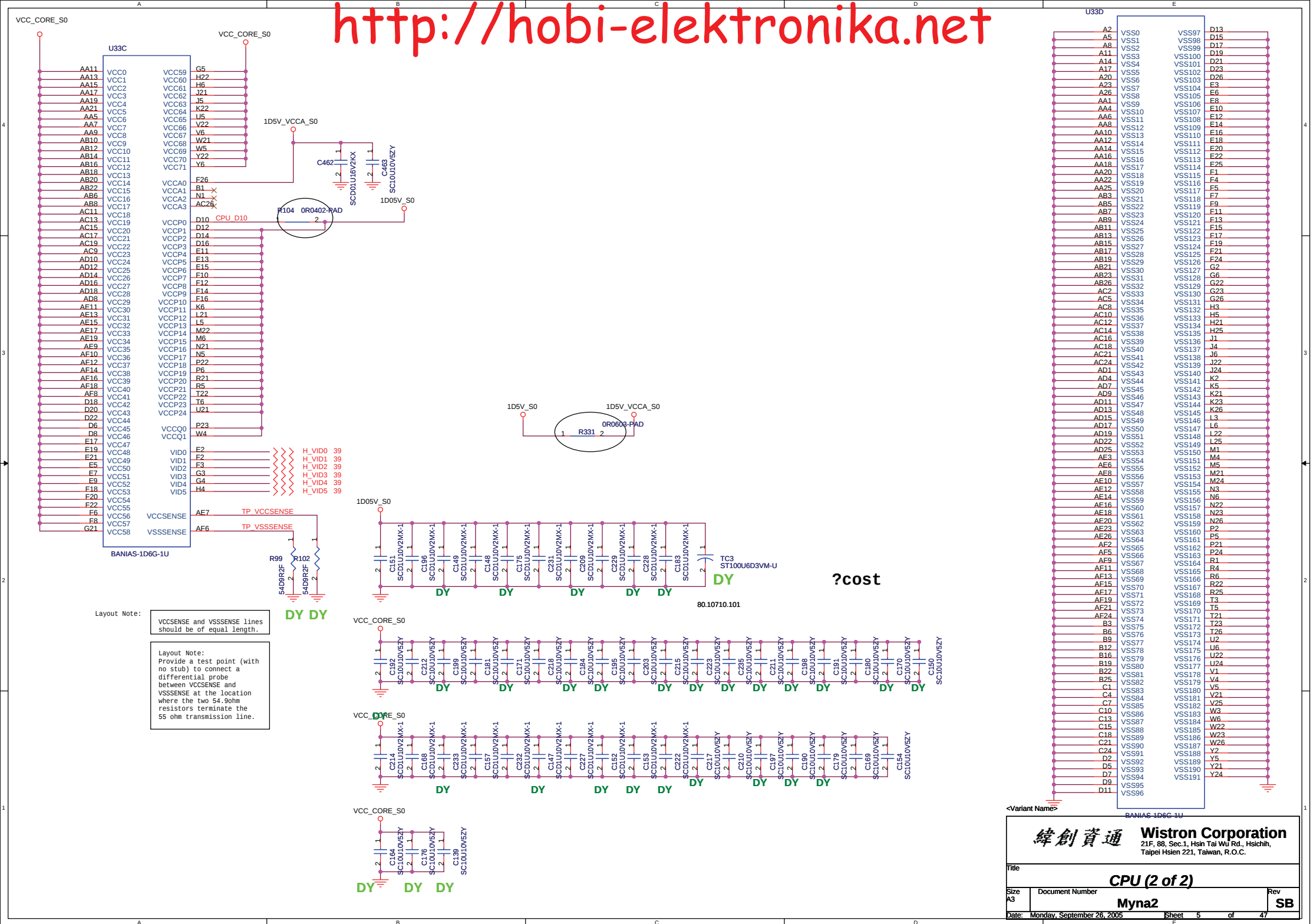
CPU_SEL0 4,7

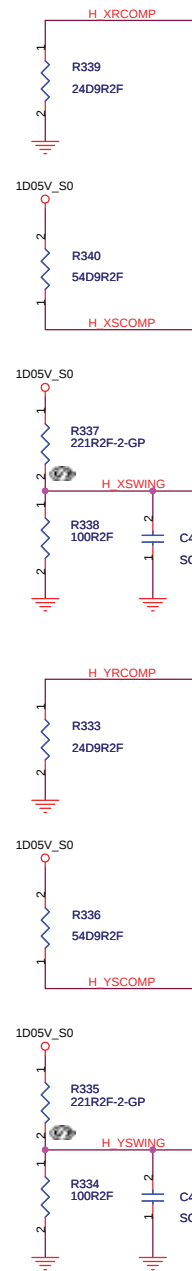
CF62	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	266M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved



		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Clock Generator - IDT125			
Size A3	Document Number		Rev
Myna2		SB	
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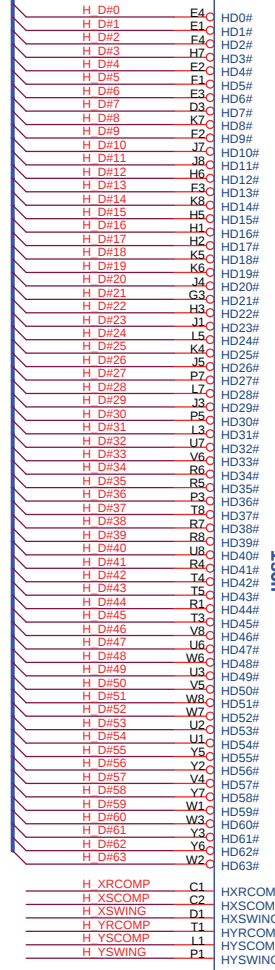




Place them near to the chip

4 H_D#[63..0]

<<>>

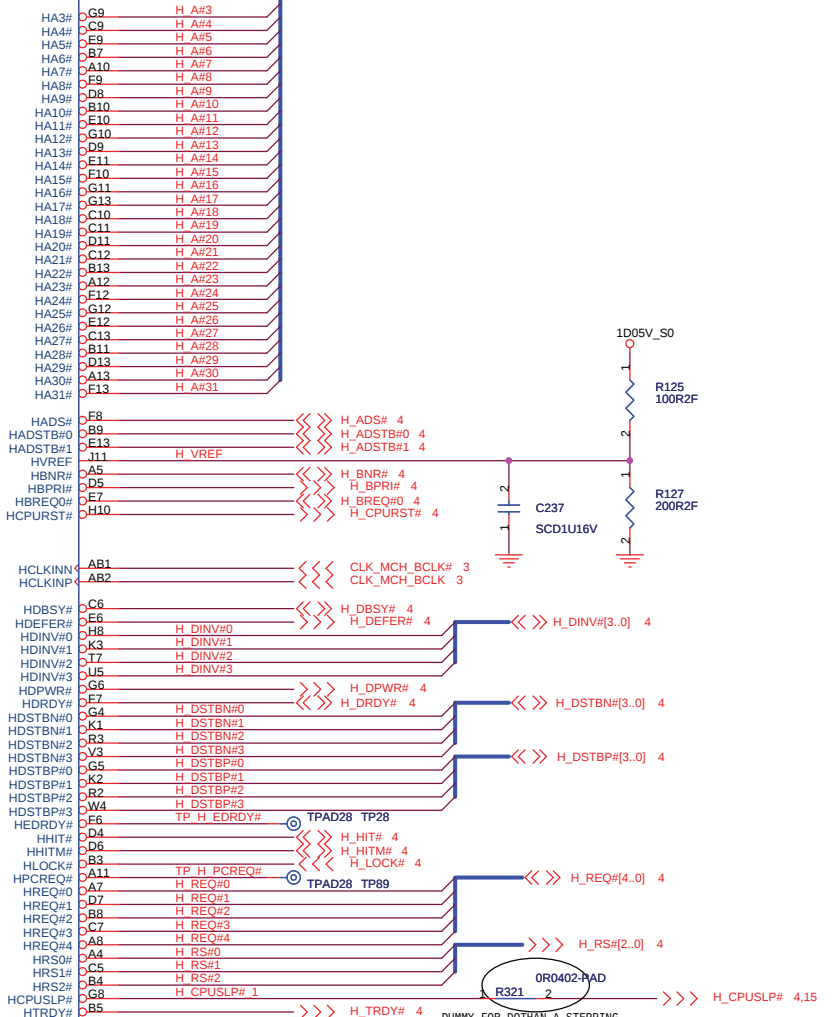


U34A

HOST

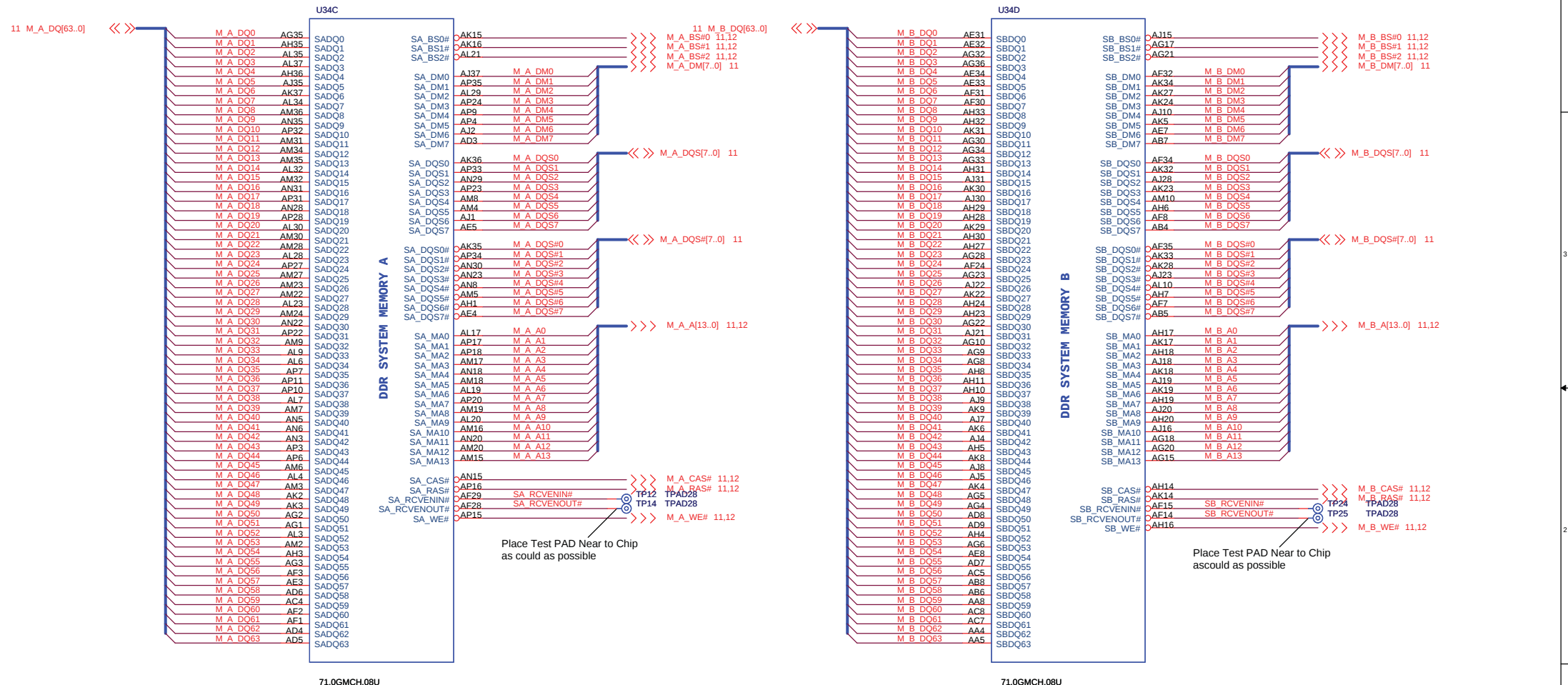
71.0GMCH.08U

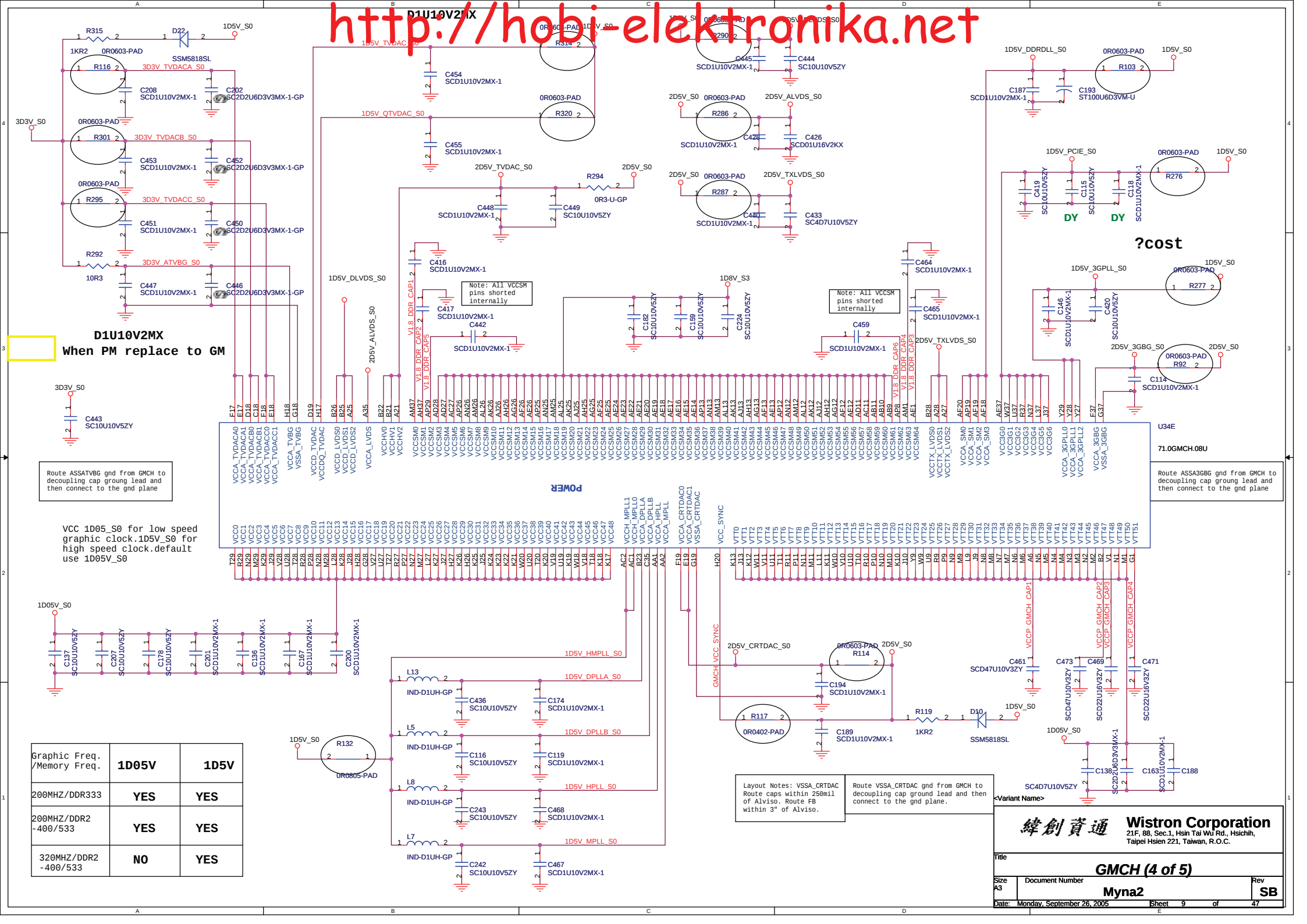
<<>> H_A#[31..3] 4



<Variant Name>





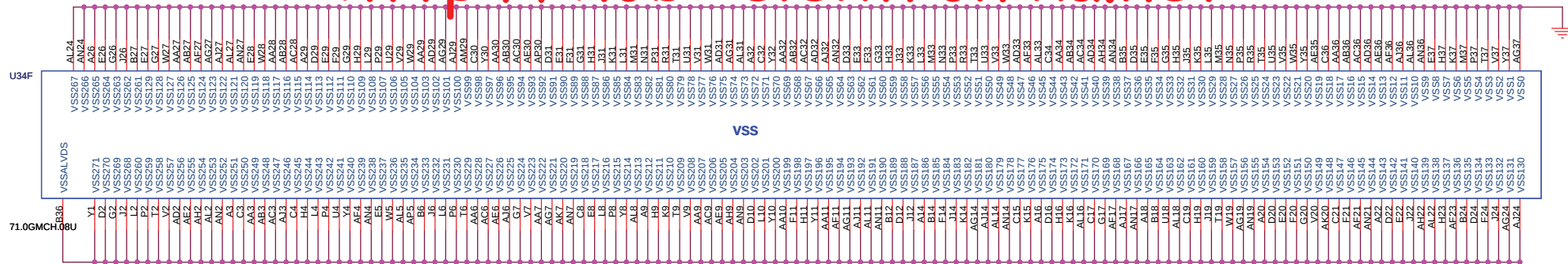


D1U10V2MX
When PM replace to GM

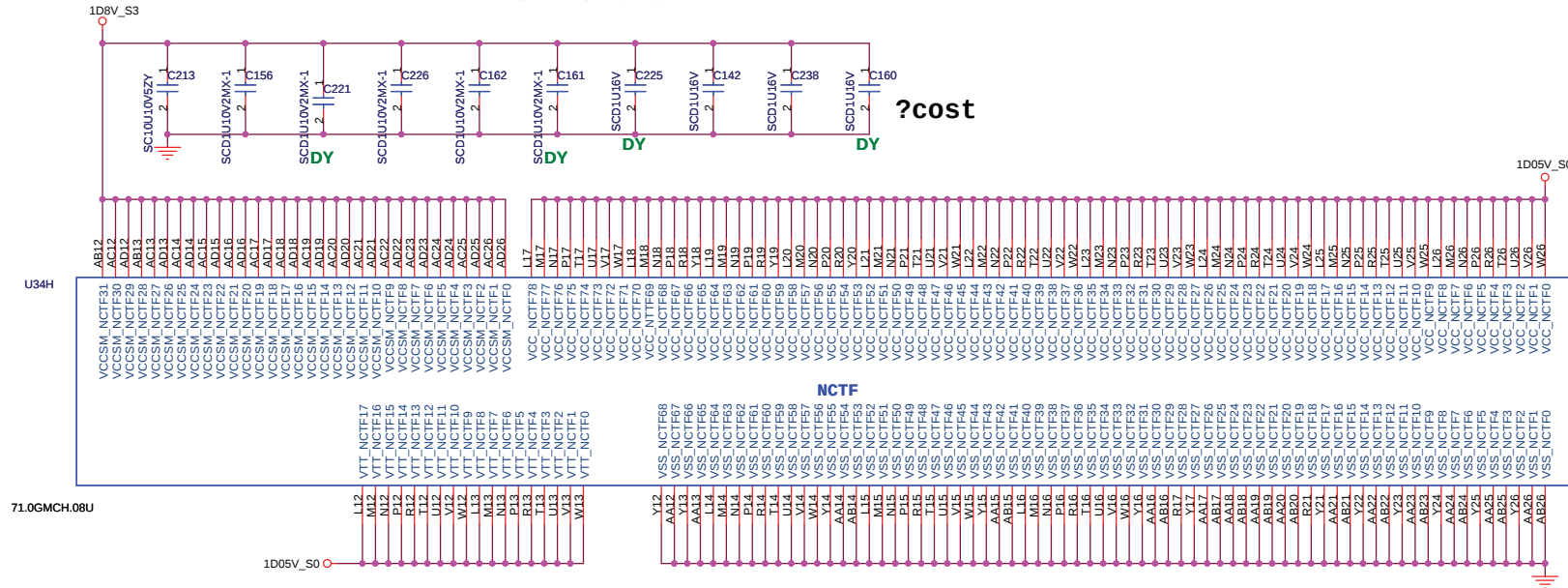
Route ASSATV86 gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane

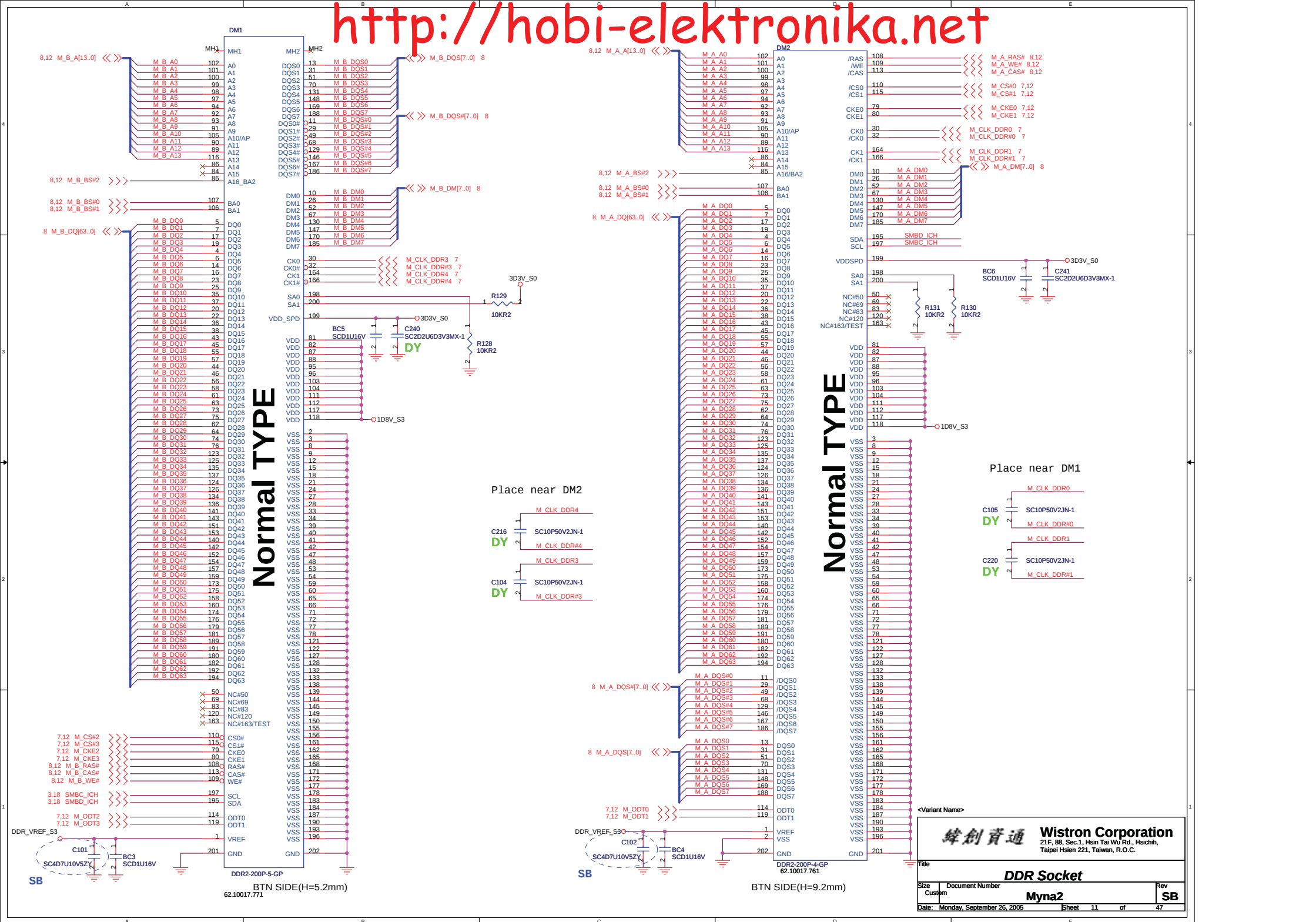
VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0

Graphic Freq. /Memory Freq.	1D05V	1D5V
200MHZ/DDR333	YES	YES
200MHZ/DDR2 -400/533	YES	YES
320MHZ/DDR2 -400/533	NO	YES



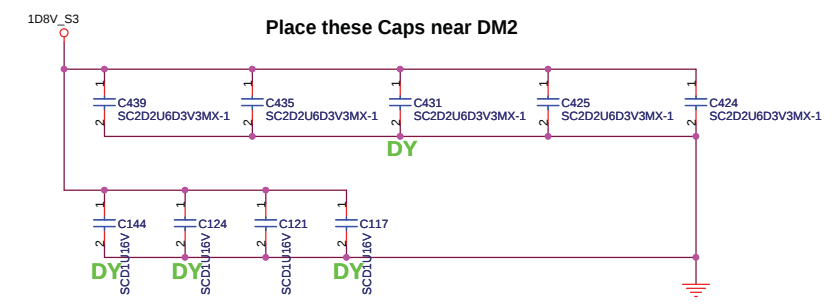
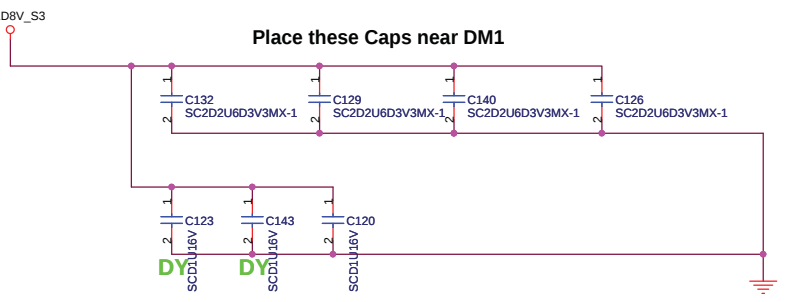
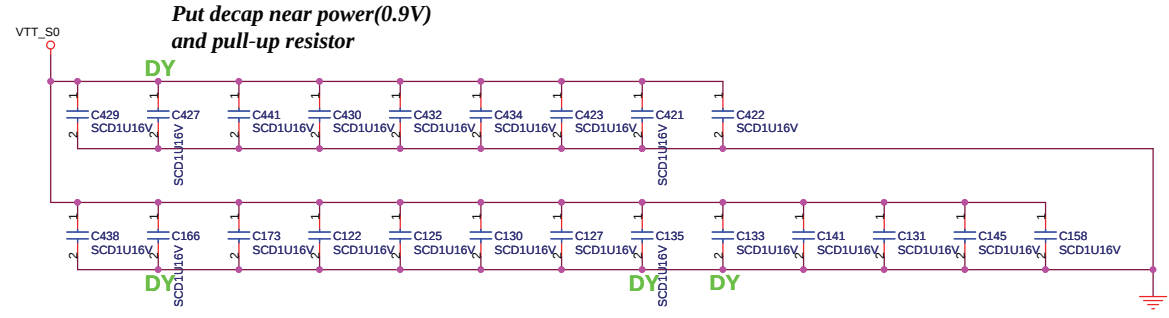
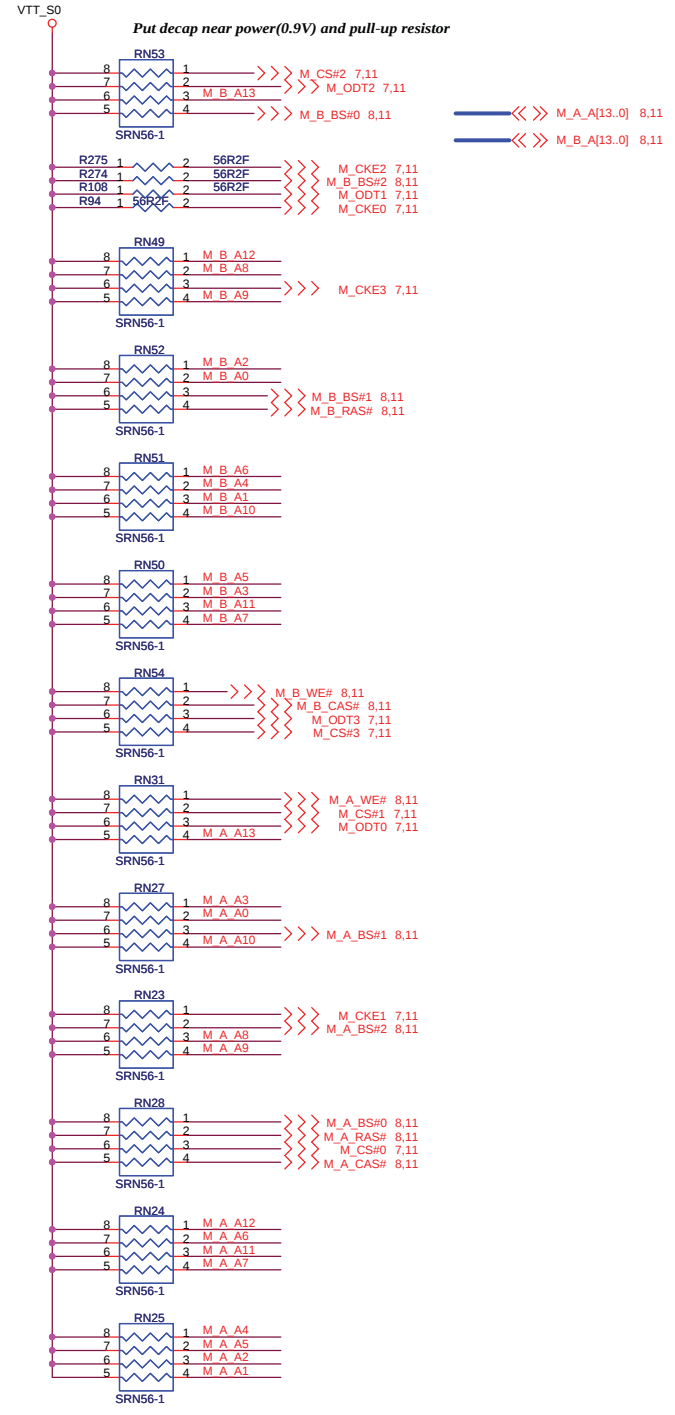
Place these Hi-Freq decoupling caps near GMCH

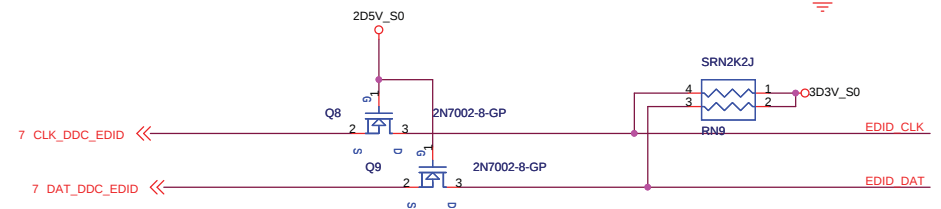
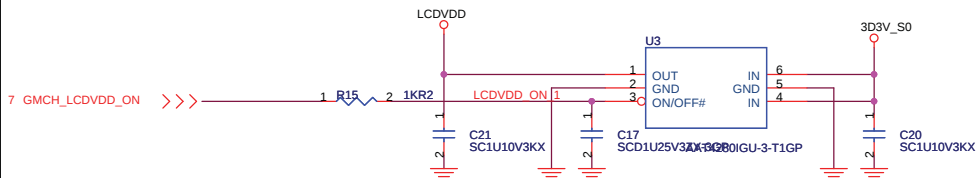


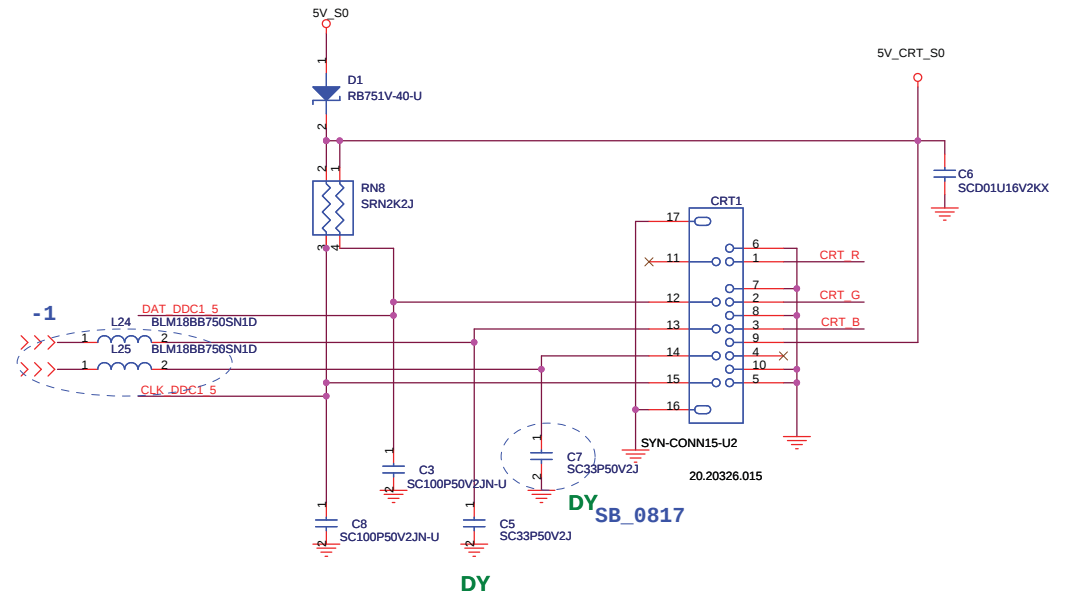
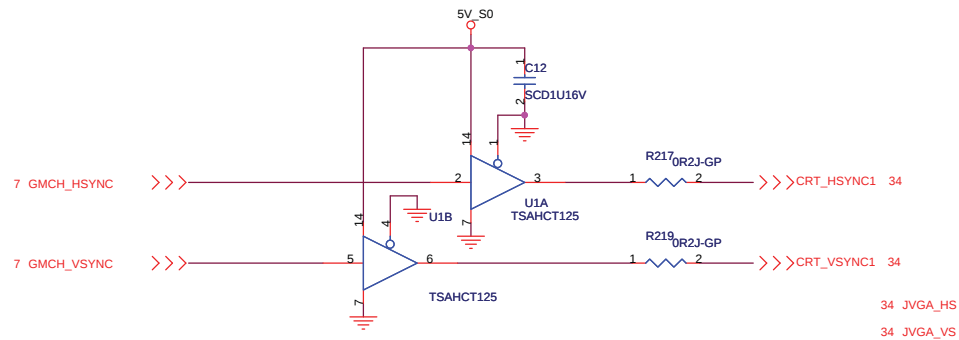
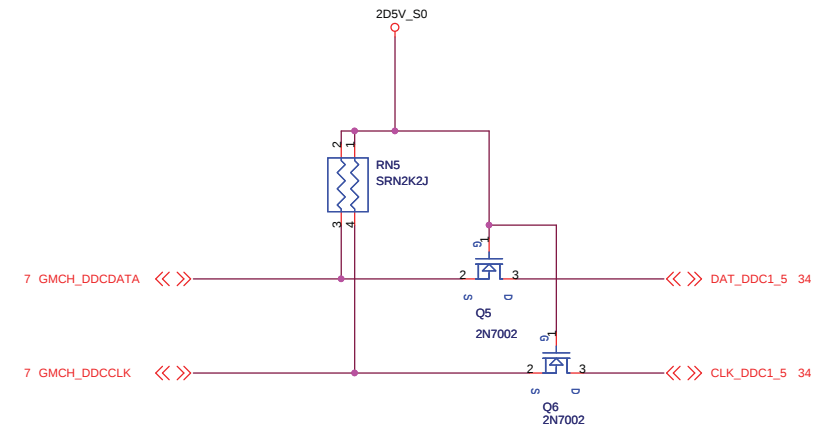
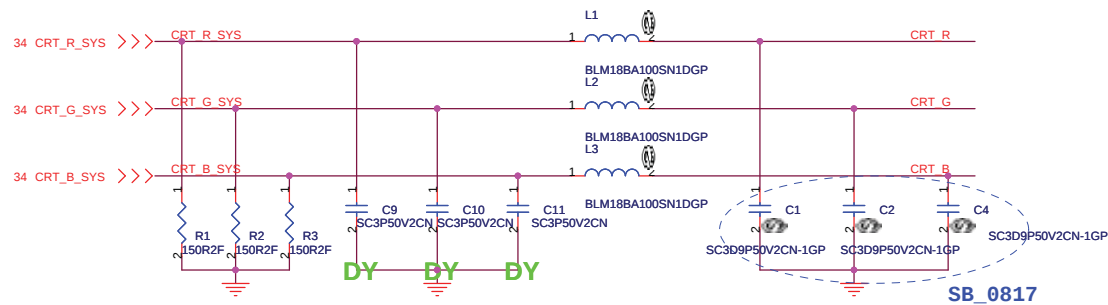


PARALLEL TERMINATION

Decoupling Capacitor



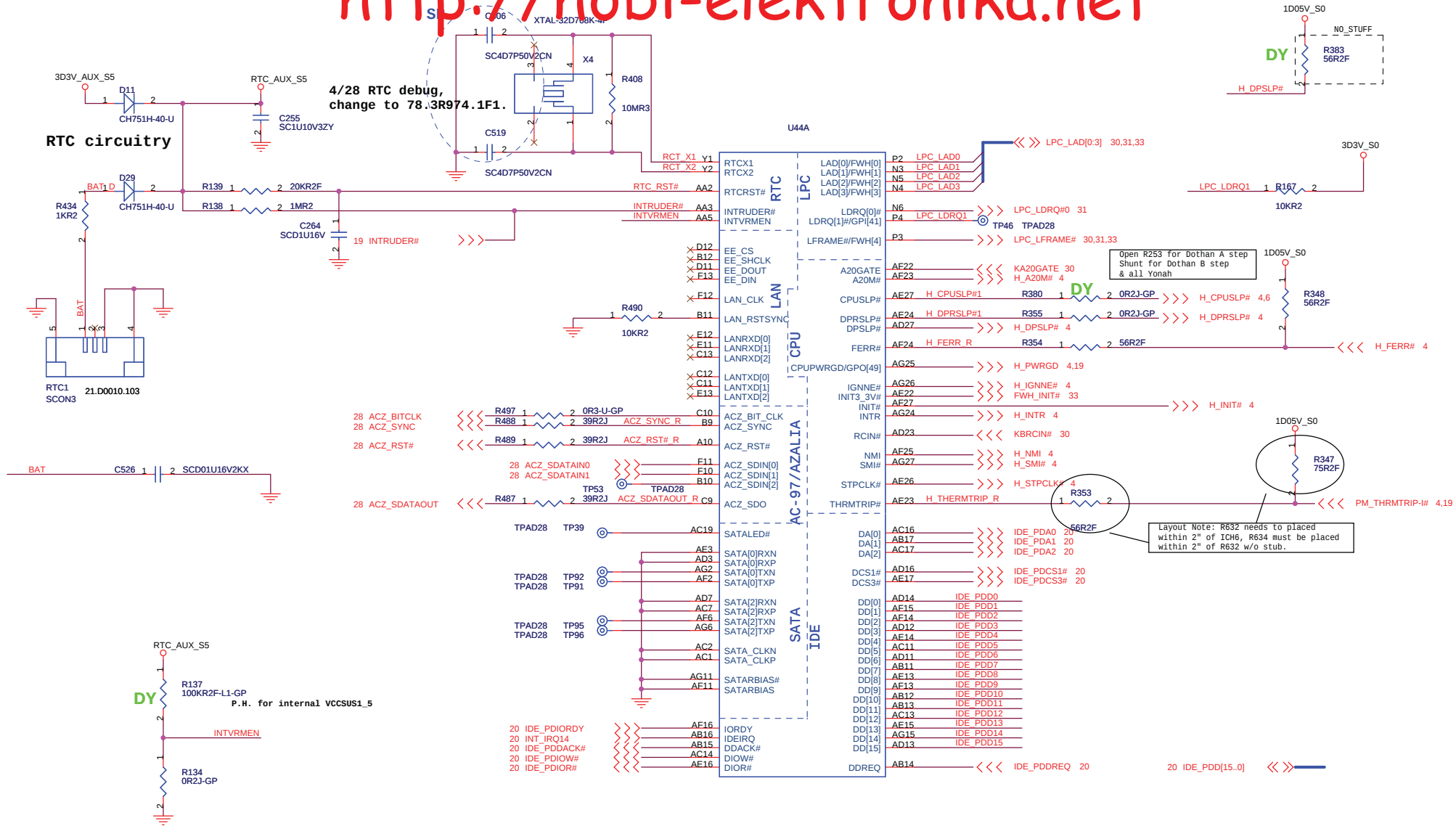




<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size A3	Document Number Myna2	Rev SB
Date: Monday, September 26, 2005	Sheet 14 of 47	



<Variant Name>

Layout Note:
Place above caps within
100 mils of ICH near F27, P27, AB27

Layout Note:
Place near pin AA19

?cost

Layout Note:
IDE decoupling

Layout Note:
PCI decoupling

Place within 100
mils of ICH
near pin AG5

Place within 100
mils of ICH
near pin AG9

?cost

Place within 100
mils of ICH
near E26, E27

Place within 100
mils of ICH
pin AE1

Place within 100
mils of ICH
pin AG10

?cost

Place within 100
mils of ICH
pin A13

Place within 100
mils of ICH
pin V7

ALL NO_STUFF Caps do
not have layout
requirements but if
layout allows then place
next to ICH6

*Within a given well, 5VREF needs to be up before the
corresponding 3.3V rail

Layout Note:
Place near ICH6

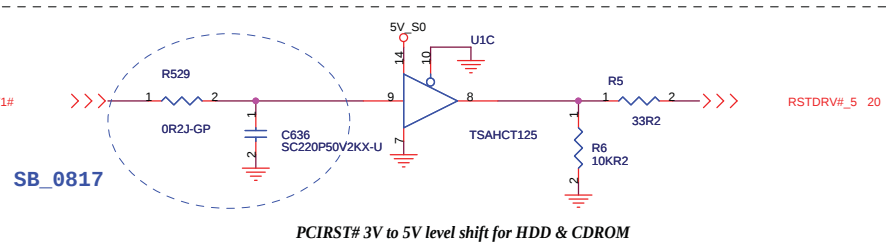
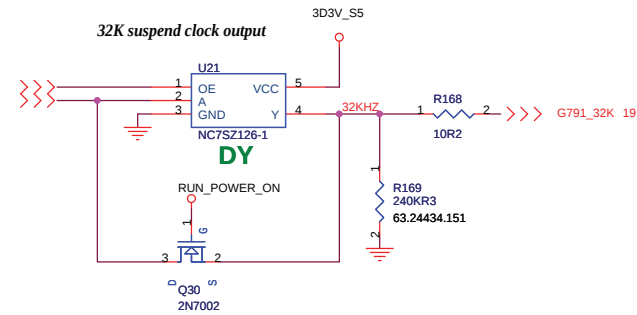
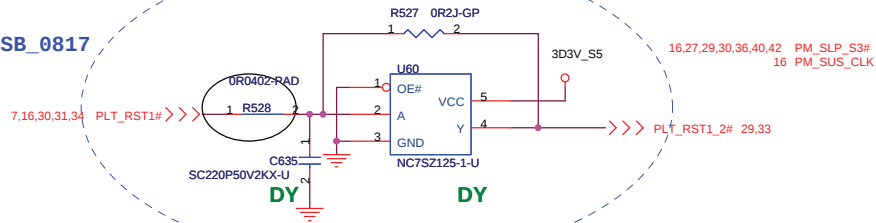
Place within 100
mils of ICH

Place within 100
mils of ICH

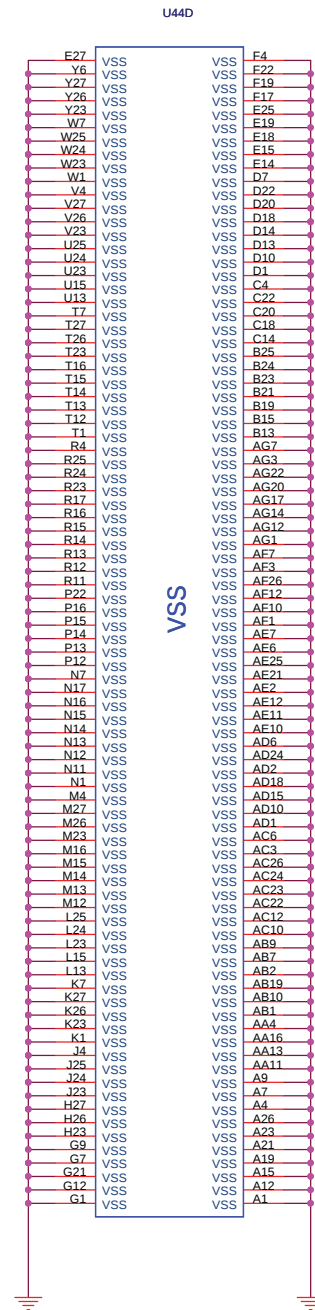
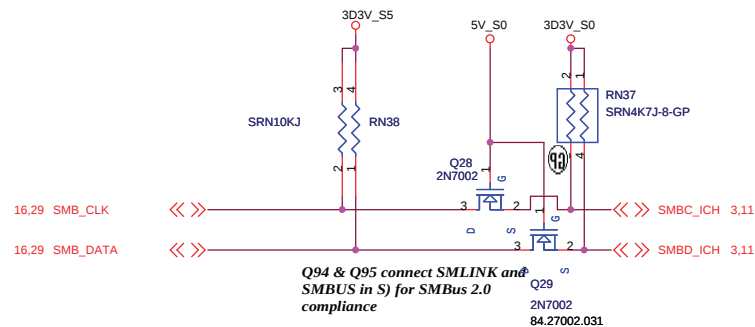
Layout Note:
Place near AB3

Layout Note:
Place near AG23

Place within 100
mils of ICH
pin A17



SMBUS



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ICH6-M (4 of 4)

Size
A3

Document Number

Myna2

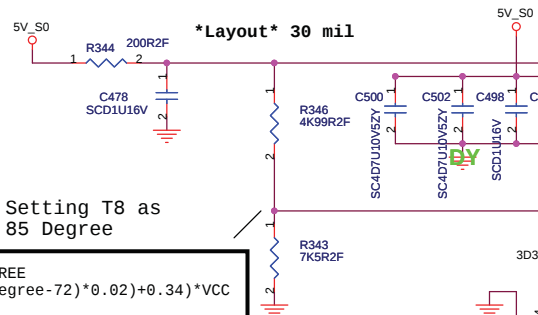
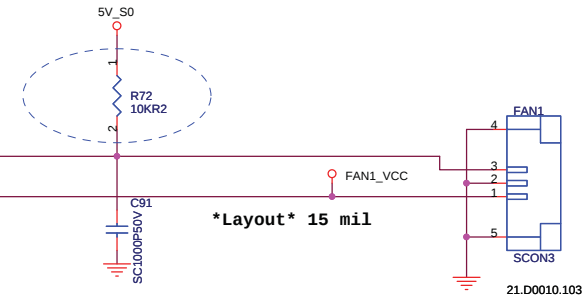
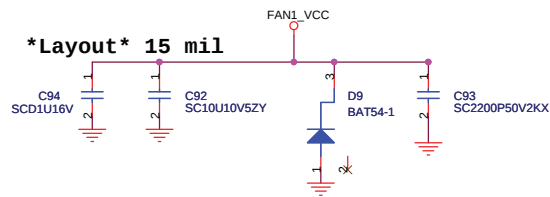
Rev

SB

Date: Monday, September 26, 2005

Sheet 18

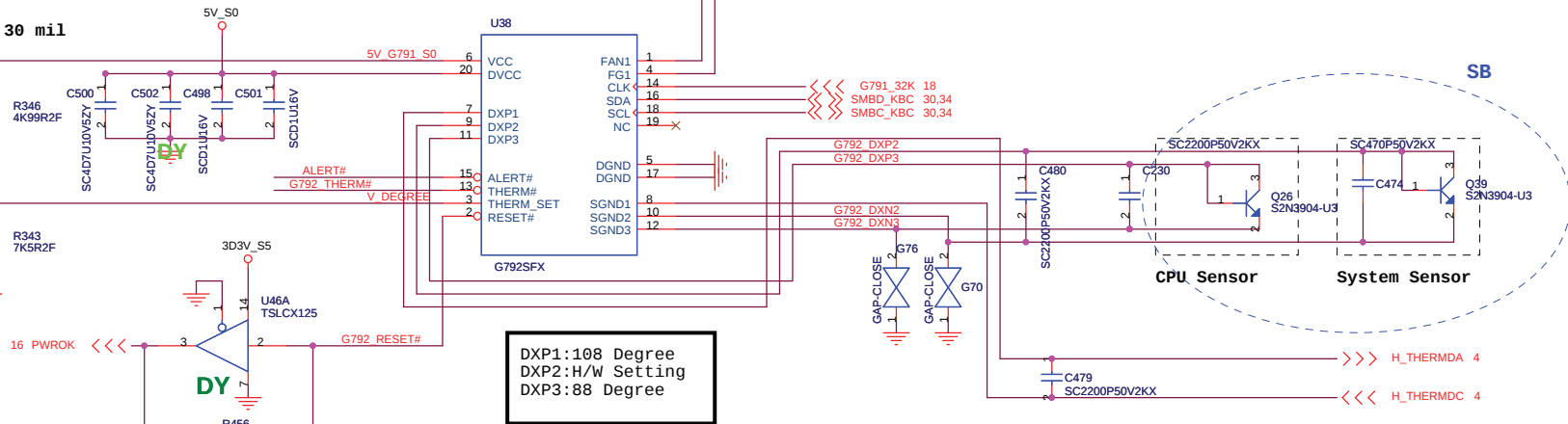
47



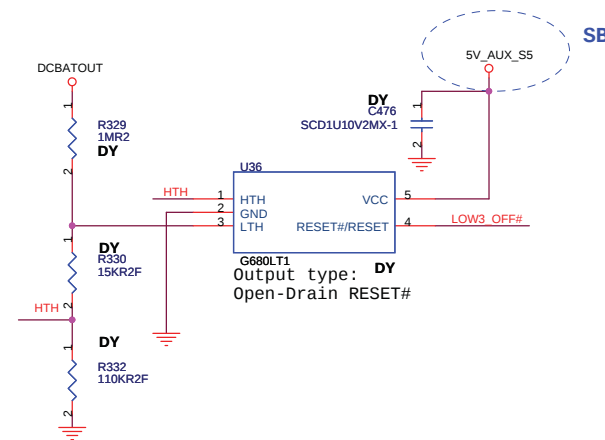
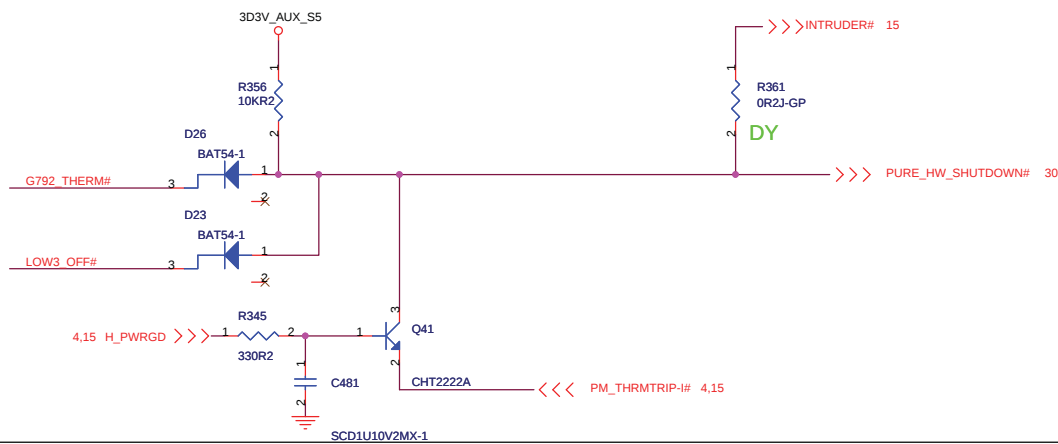
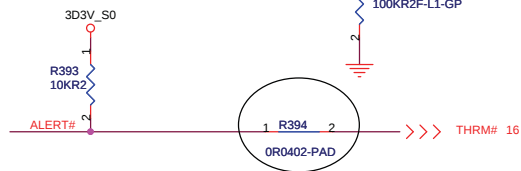
Setting T8 as
85 Degree

$$V_DEGREE = ((Degree - 72) * 0.02) + 0.34 * VCC$$

setting 85 degree dor DXP2/DXN2...



HW Thermal Throttling

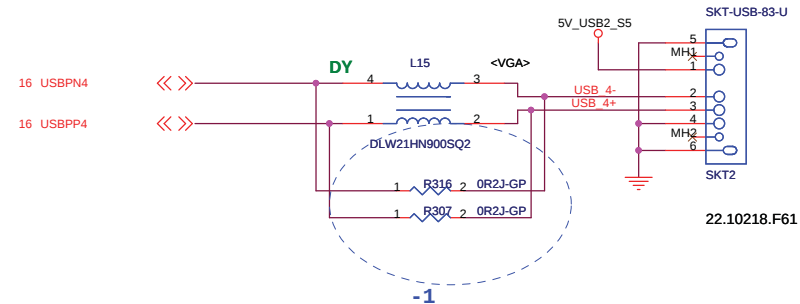


L3# at 11.25V

Low3 Circuit :

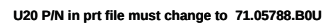
<Variant Name>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Thermal/Fan Controller</i>			
Size Custom	Document Number		Rev
	Myna2		SB
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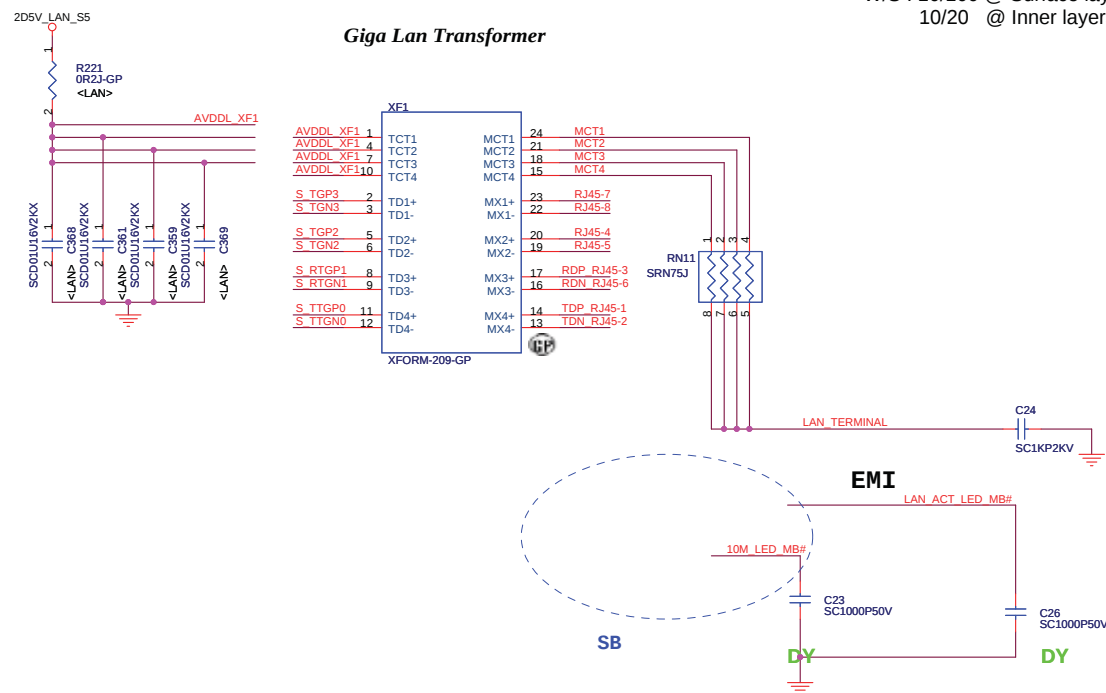




12/29
Place near BT1







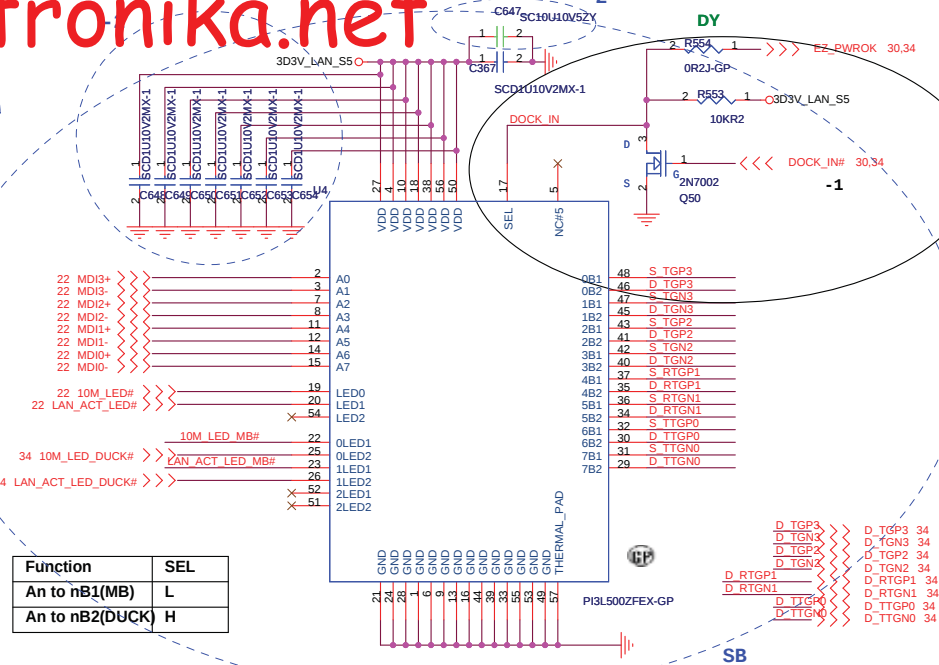
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other traces.
7. Must not cross ground moat, except RJ-45 moat.

```

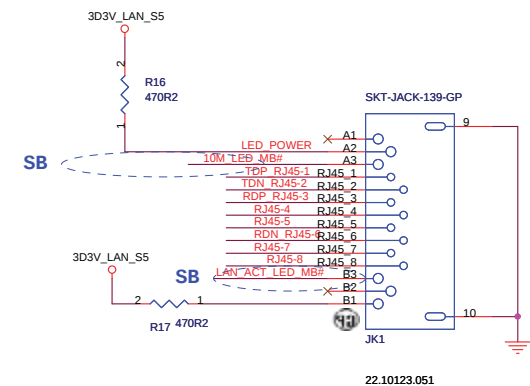
Green LED: Speed 100: ON / Speed 10:OFF
Yellow LED: Link: ON, TX/RX:
Flash(10Hz) -----

```

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



RJ45 Connector



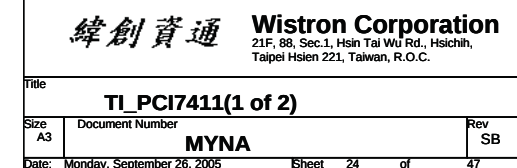
Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

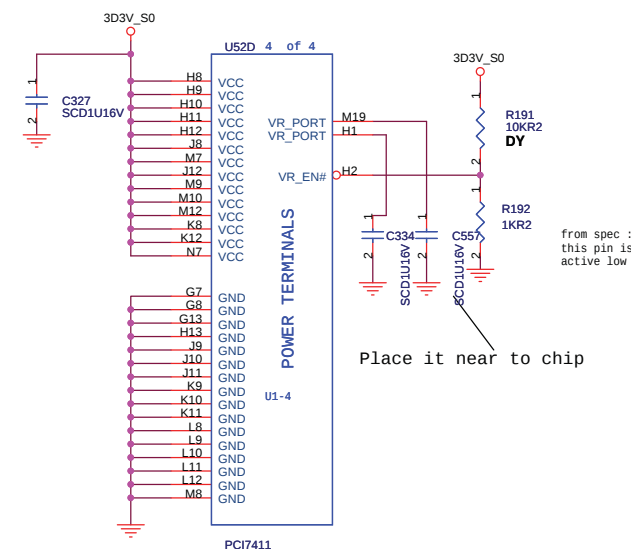
Activity: Yellow

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LAN Connector			
Size Custom	Document Number		Rev
	Myna2		SB
Date:	Monday, September 26, 2005	Sheet 23 of	47

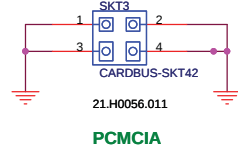
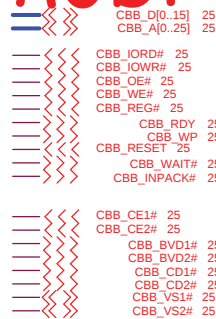




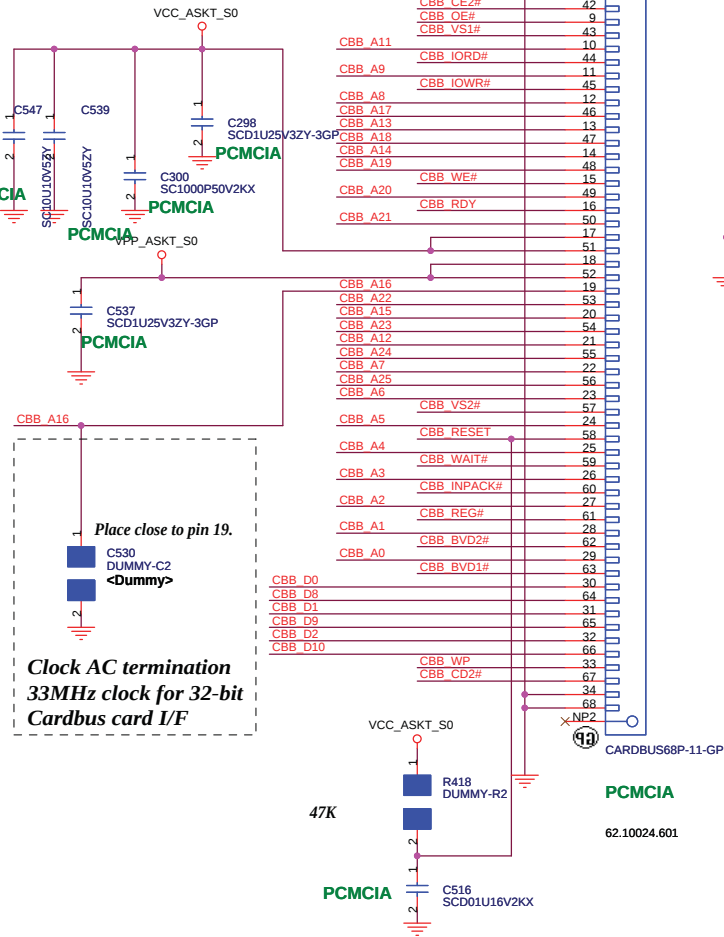
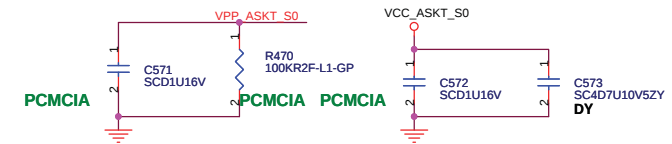
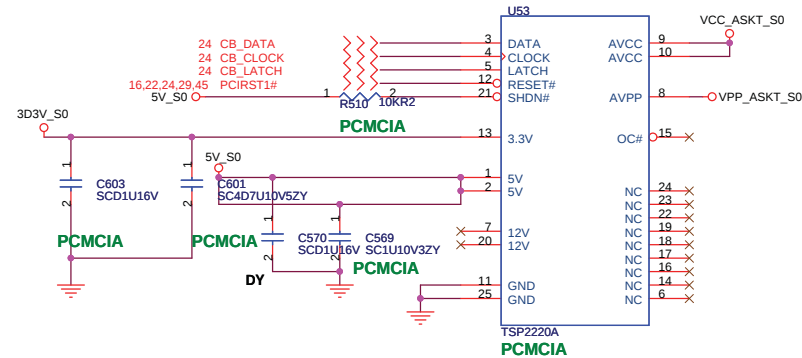
PCMCIA Socket

<http://hobi-elektronika.net>

Cardbus I/F

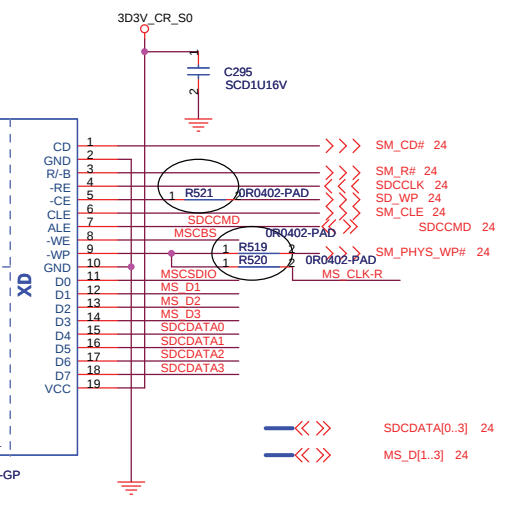
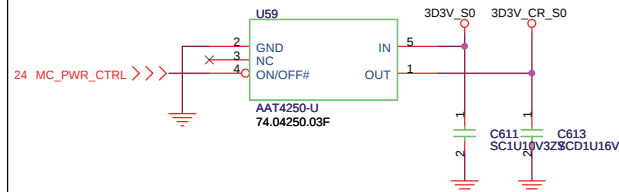


Power switch



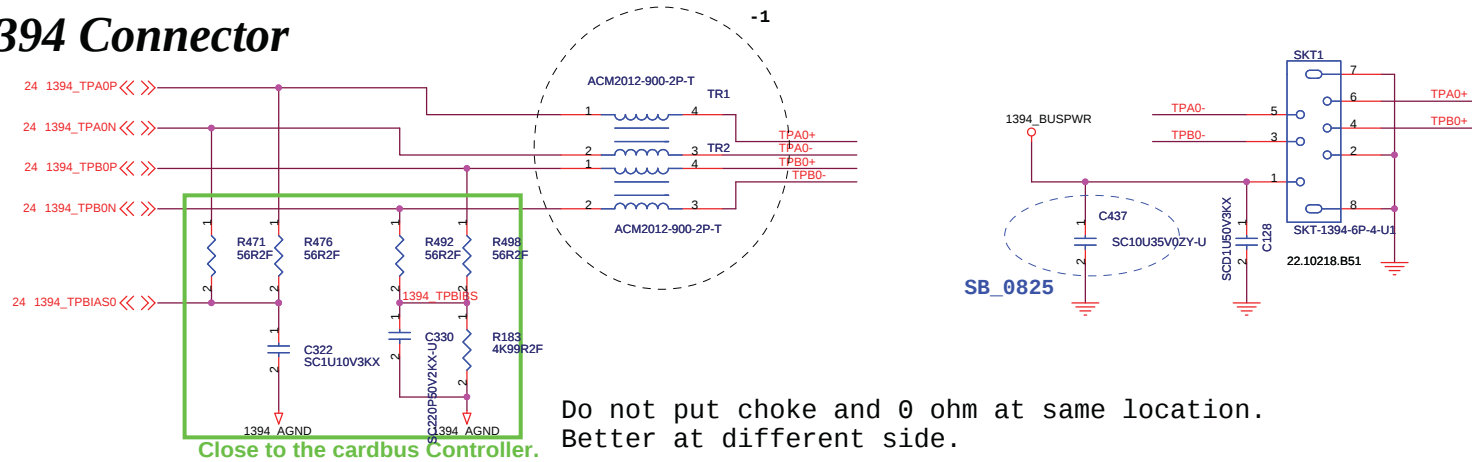
Place close to pin 19.
C530 DUMMY-C2 <Dummy>
Clock AC termination
33MHz clock for 32-bit
Cardbus card I/F

POWER SWITCH

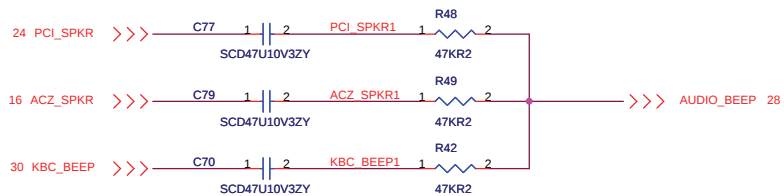
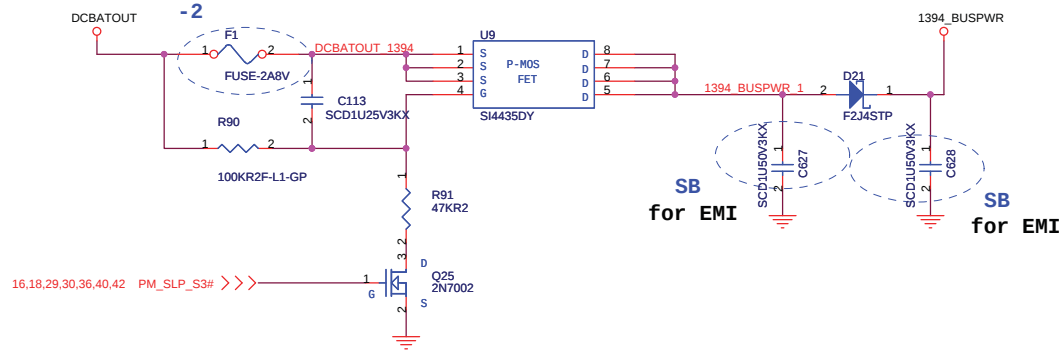


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
PCMCA / 1394 / CARD READER		
Size	Document Number	Rev
A3	Myna2	SB
Date: Monday, September 26, 2005	Sheet 26 of 47	

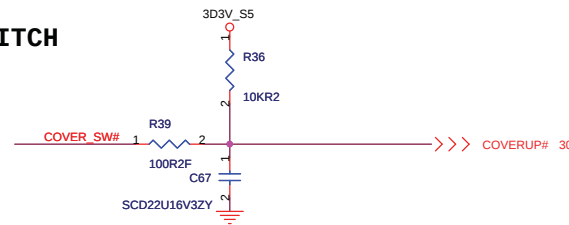
1394 Connector



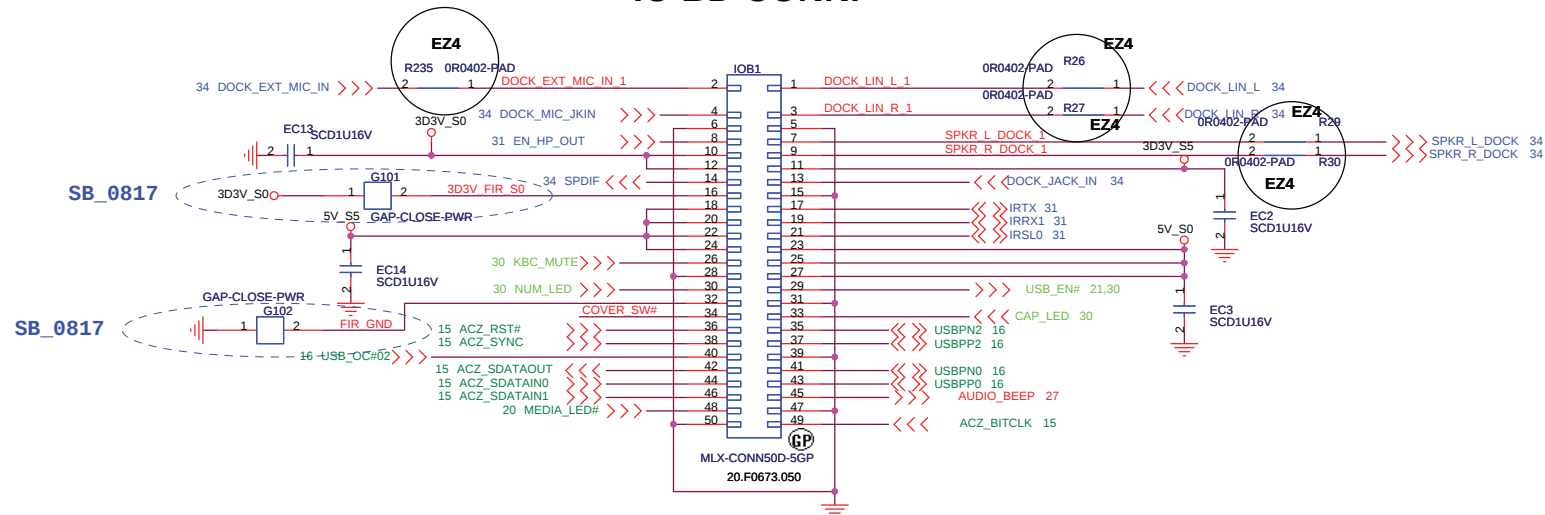
4/21 External ODD will suck more than 1.5A when battery mode



COVER SWITCH



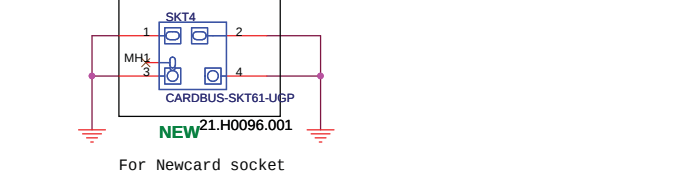
IO BD CONN.



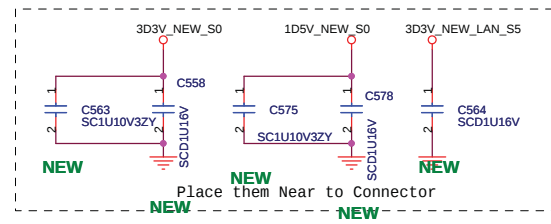
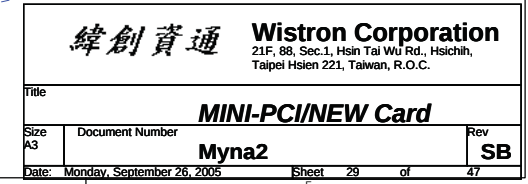
Blue -> Dock or SuperIO
Light Green -> KBC
Green -> SouthBridge

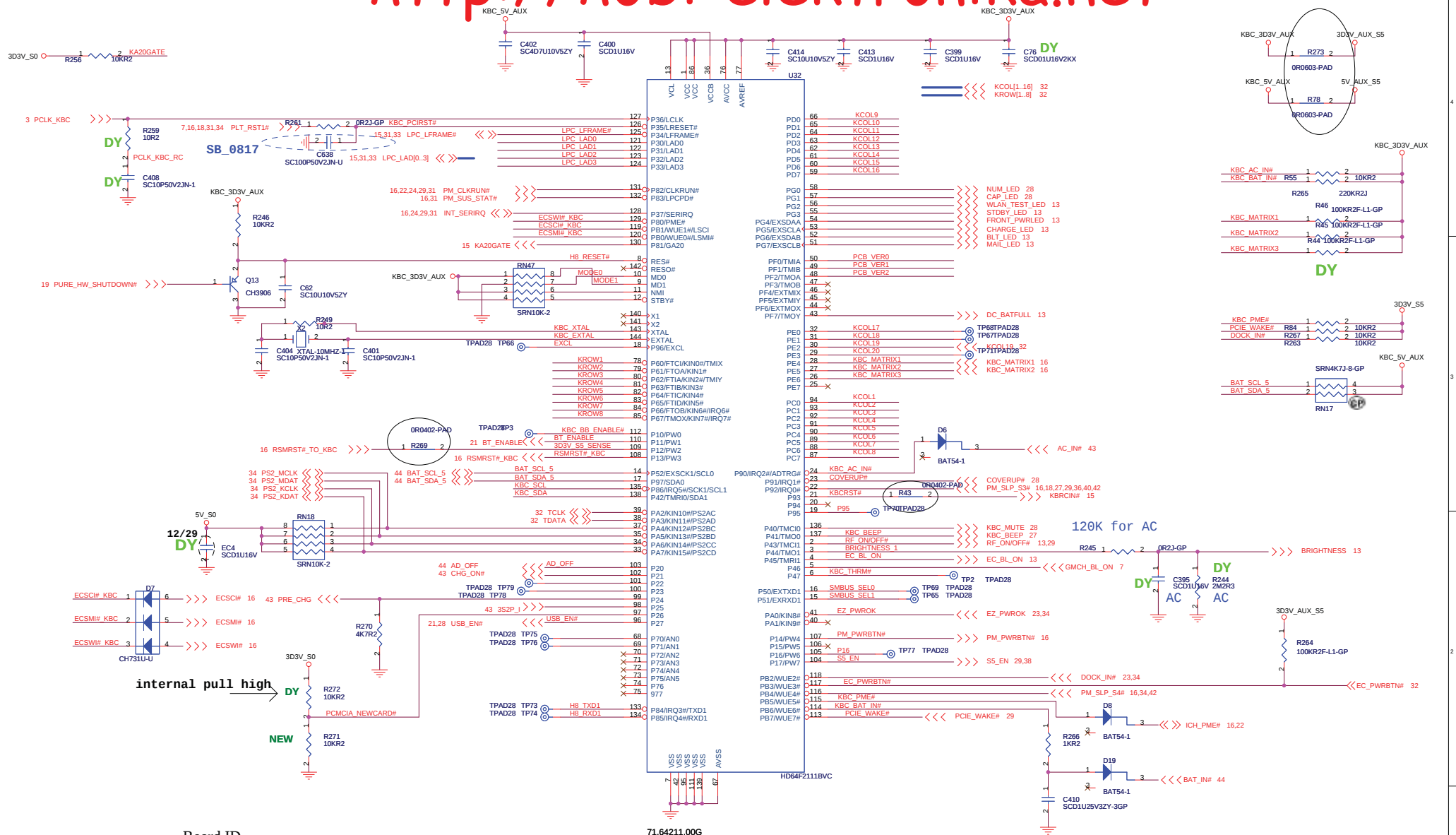
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AC'97 CODEC - ALC655			
Size A3	Document Number	Rev	
	Myna2		
Date: Monday, September 26, 2005		Sheet 28 of 47	SB

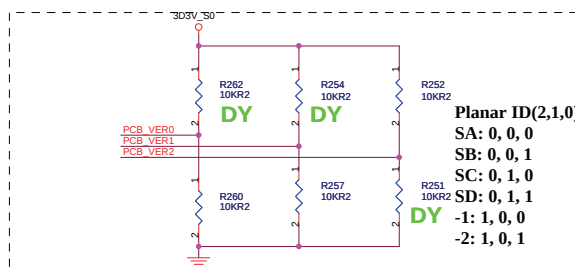


Reserve the symbol
for bottom side
connector

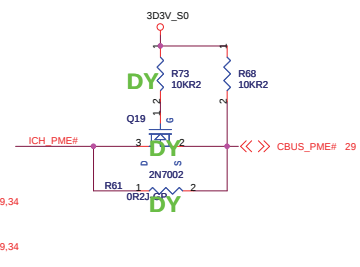
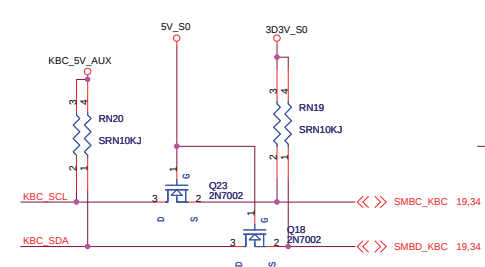




Board ID



Planar ID(2,1,0)
SA: 0, 0, 0
SB: 0, 0, 1
SC: 0, 1, 0
SD: 0, 1, 1
-1: 1, 0, 0
-2: 1, 0, 1



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

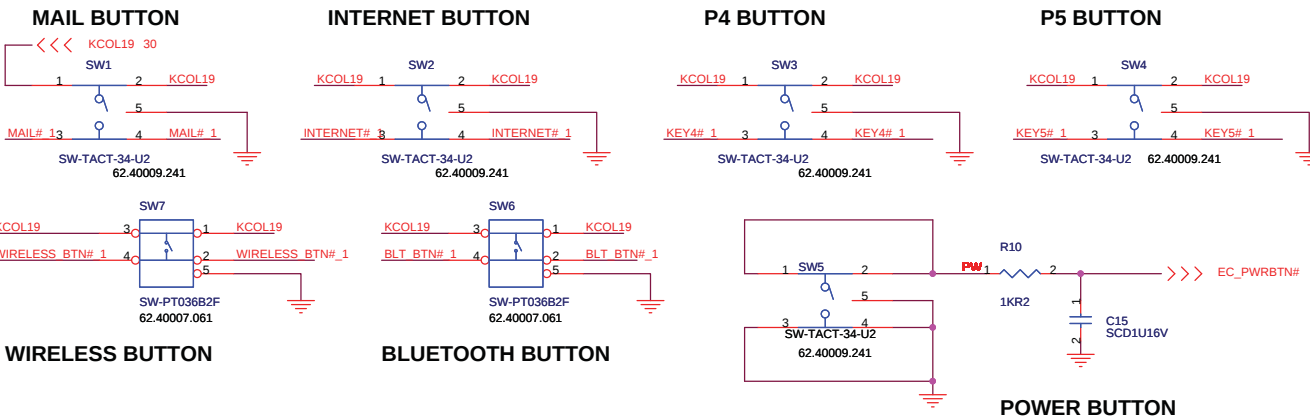
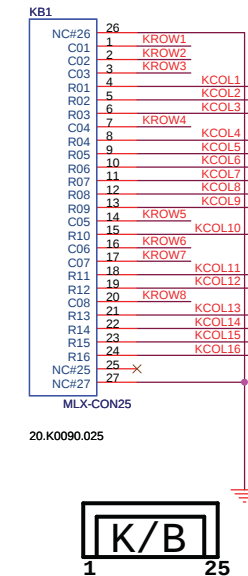
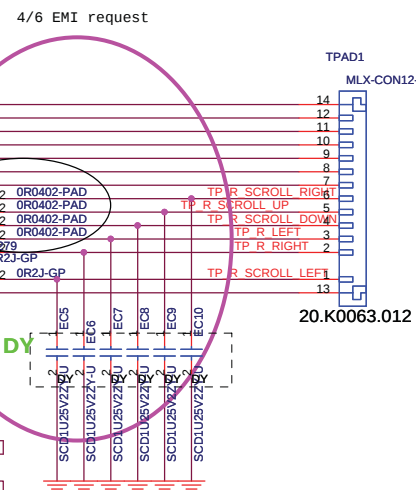
Title			
KBC H8			
Size	Document Number	Rev	
Custom	Myna2	SB	
Date: Monday, September 26, 2005		Sheet 30	of 47

<http://hobi-elektronika.net>



The diagrams show the following connections:

- RC4:** KCOL2 (red) to pin 1, KCOL3 (red) to pin 2, KROW4 (green) to pin 3, KCOL4 (red) to pin 4, pin 8 to pin 7, pin 6 to pin 5, and pin 5 to ground.
- RC5:** KCOL5 (red) to pin 1, KCOL6 (red) to pin 2, KCOL7 (red) to pin 3, KCOL8 (red) to pin 4, pin 8 to pin 7, pin 6 to pin 5, and pin 5 to ground.
- RC6:** KROW9 (green) to pin 1, KROW5 (green) to pin 2, KCOL10 (red) to pin 3, KROW6 (green) to pin 4, pin 8 to pin 7, pin 6 to pin 5, and pin 5 to ground.
- RC8:** KCOL13 (red) to pin 1, KCOL14 (red) to pin 2, KCOL15 (red) to pin 3, KCOL16 (red) to pin 4, pin 8 to pin 7, pin 6 to pin 5, and pin 5 to ground.
- RC3:** KROW1 (green) to pin 1, KROW2 (green) to pin 2, KROW3 (green) to pin 3, KCOL1 (red) to pin 4, pin 8 to pin 7, pin 6 to pin 5, and pin 5 to ground.
- RC7:** KROW7 (green) to pin 1, KCOL11 (red) to pin 2, KCOL12 (red) to pin 3, KROW8 (green) to pin 4, pin 8 to pin 7, pin 6 to pin 5, and pin 5 to ground.

[illegible]

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

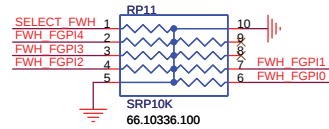
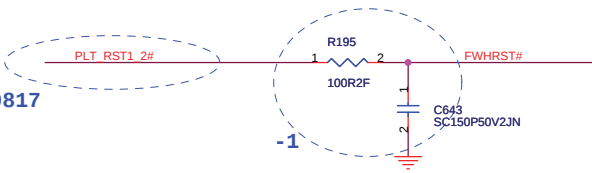
Title			
KBC&TPAD CONN			
Size A3	Document Number		Rev
	Myna2		SB
Date:	Monday, September 26, 2005	Sheet 32 of 47	

? if use Debug Board, remove this

<http://hobi-elektronika.net>

Unused FGPI pins must not be float

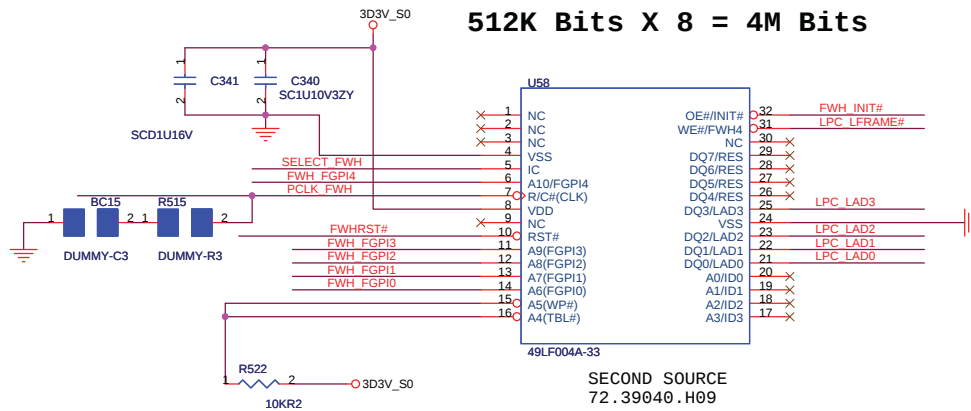
SB_0817



15,30,31 LPC_LAD[0:3] << >>

FLASH ROM

512K Bits X 8 = 4M Bits



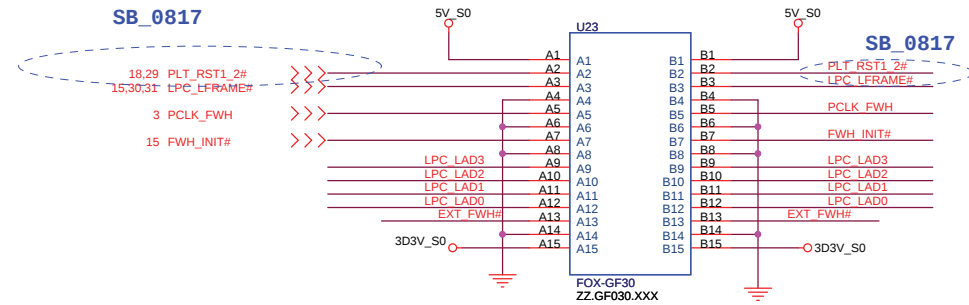
SECOND SOURCE
72.39040.H09

TOP VIEW

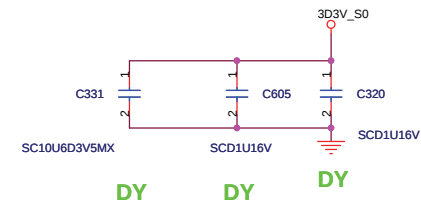
A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

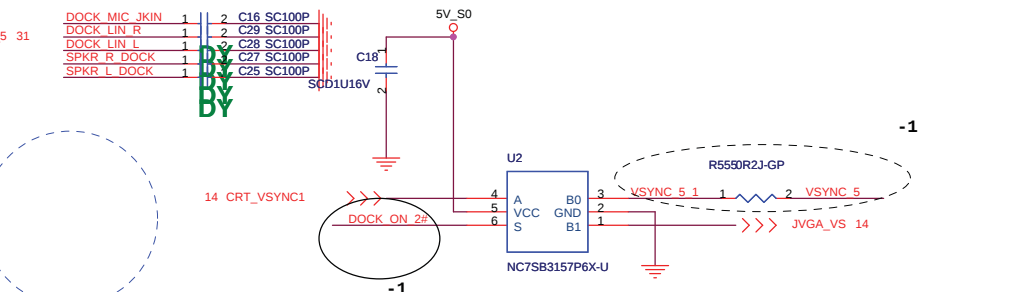
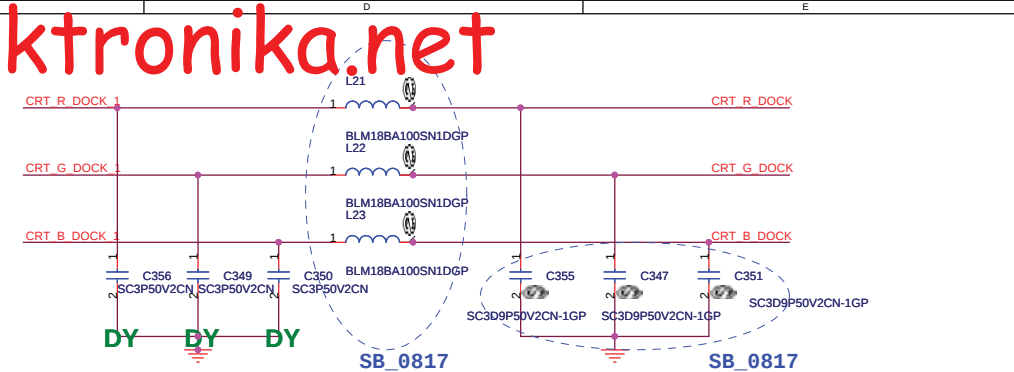
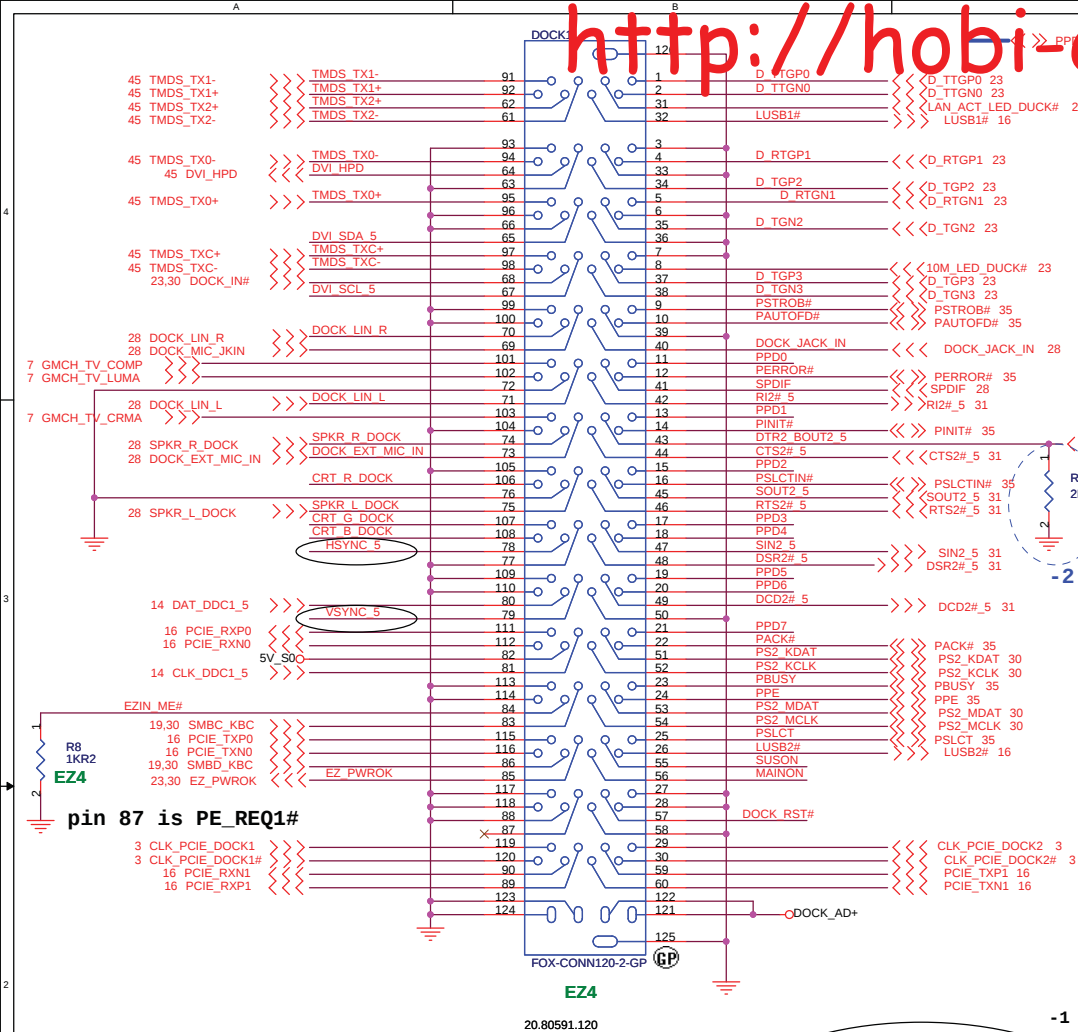


Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



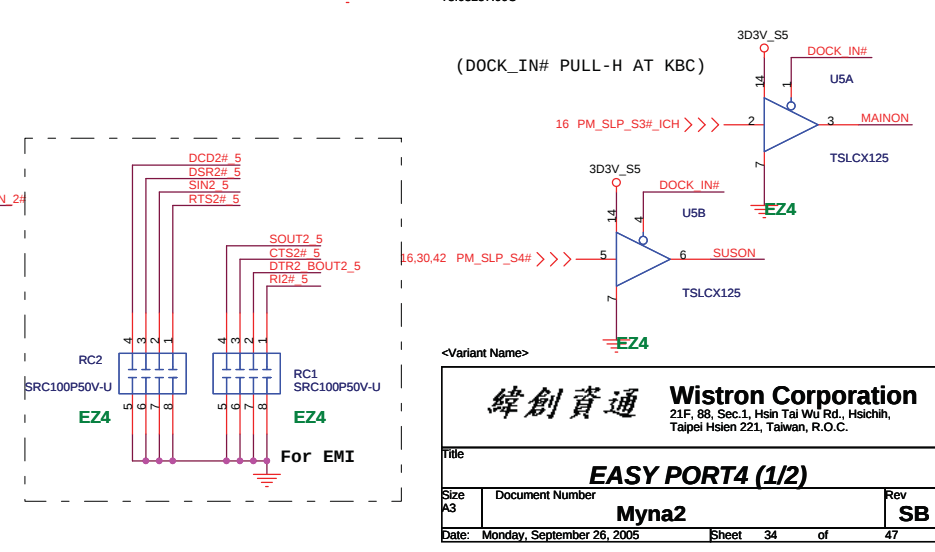
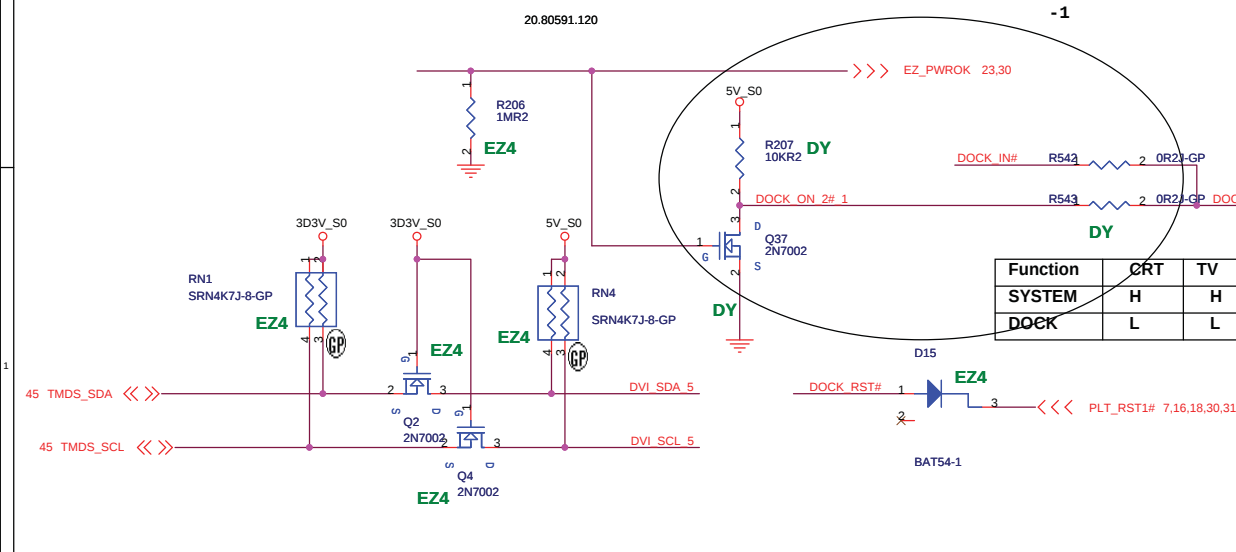
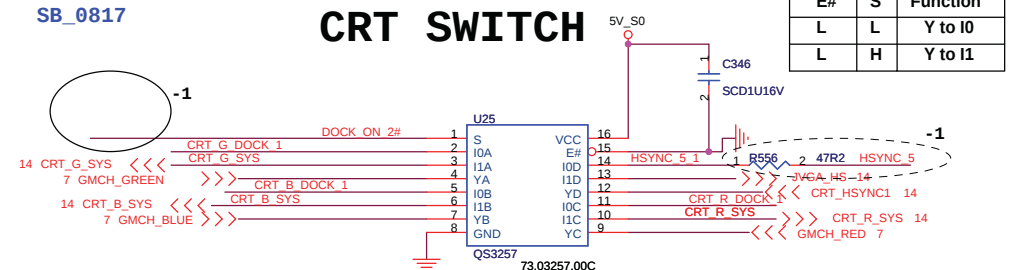
<Variant Name>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
FWH and Debug			
Size	Document Number	Rev	
A3	Myna2	SB	
Date:	Monday, September 26, 2005	Sheet	33 of 47

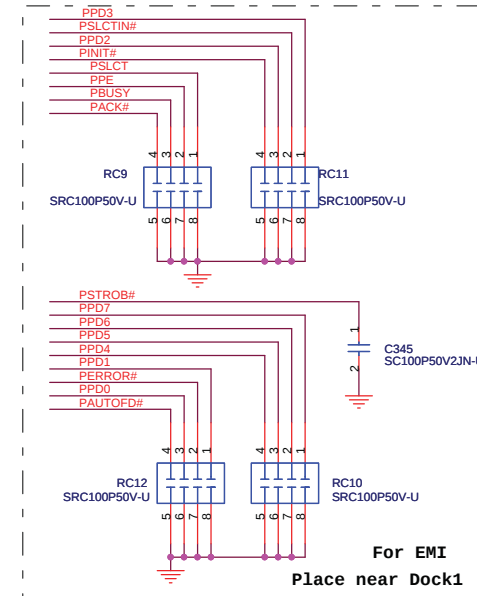
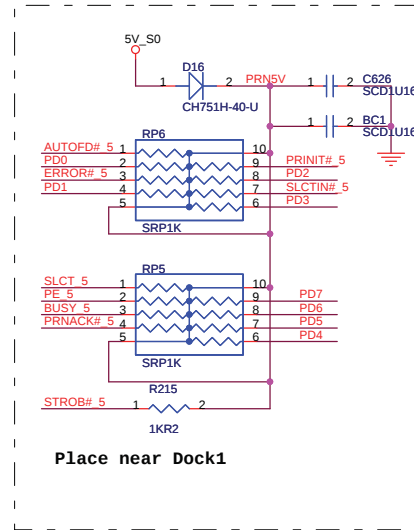
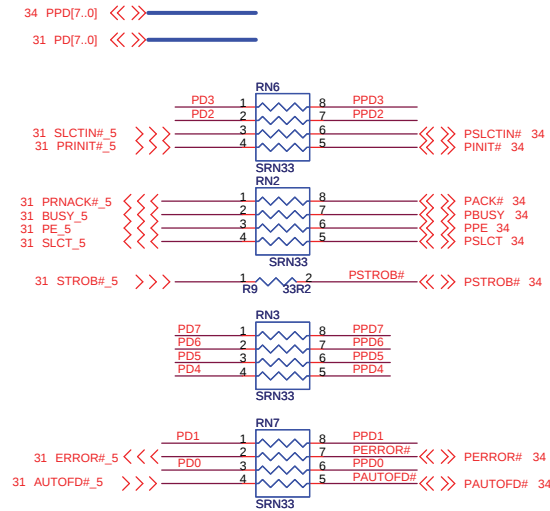


CRT SWITCH

E#	S	Function
L	L	Y to I0
L	H	Y to I1



PRINT PORT



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

EASY PORT4 (2/2)

Size
A3

Document Number

Myna2

Rev

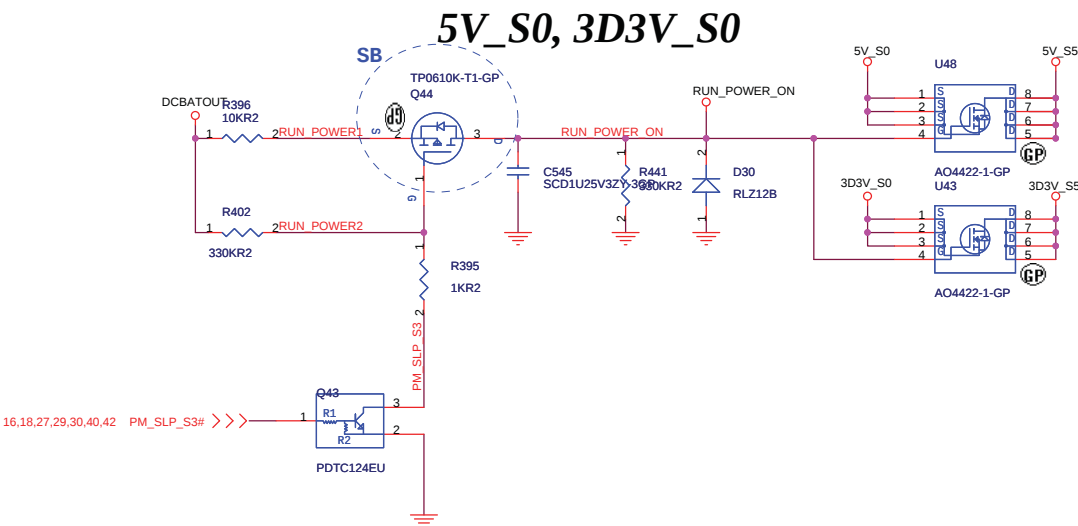
SB

Date: Monday, September 26, 2005

Sheet 35

of

47

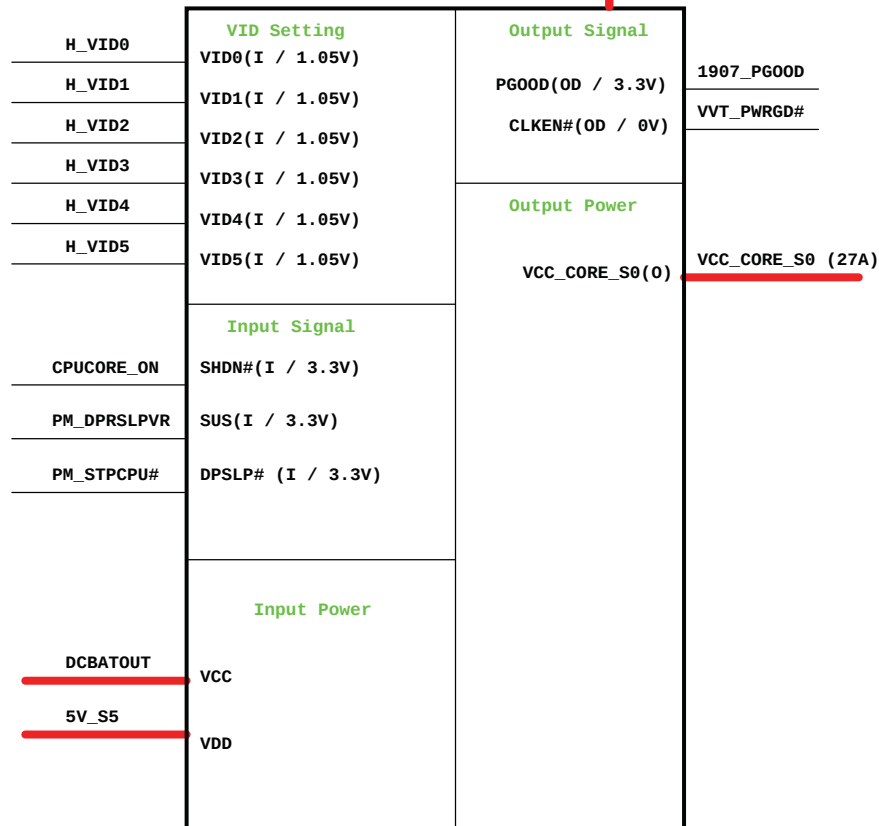


<Variant Name>

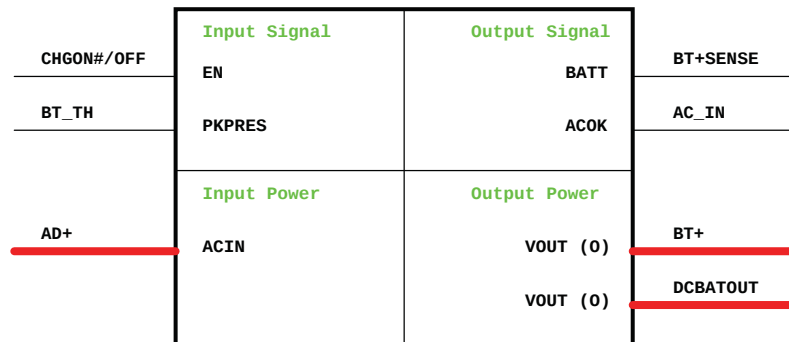
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title RUN Power		
Size A3	Document Number Myna2	Rev SB
Date: Monday, September 26, 2005	Sheet 36 of 47	

CPU_CORE

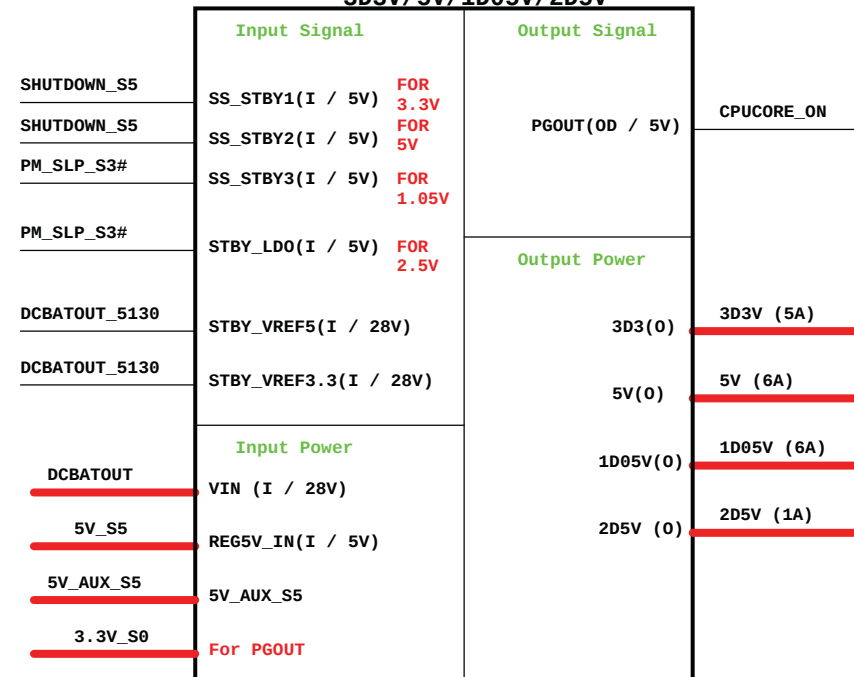
MAX1907AEFL-U



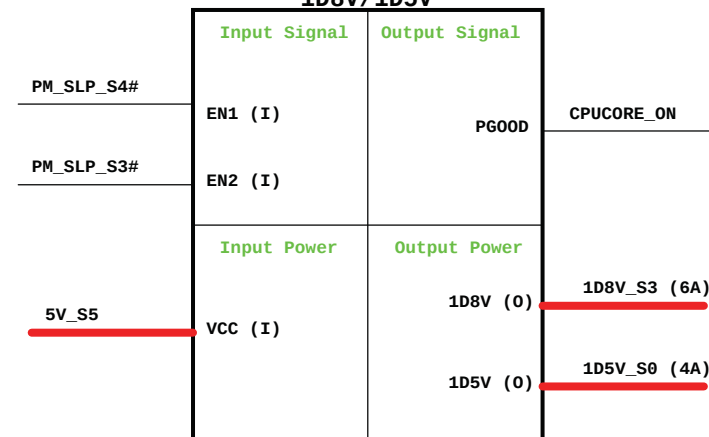
Charger ISL6225



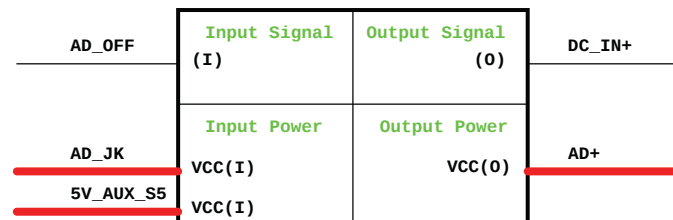
PS5_30 3D3V/5V/1D05V/2D5V

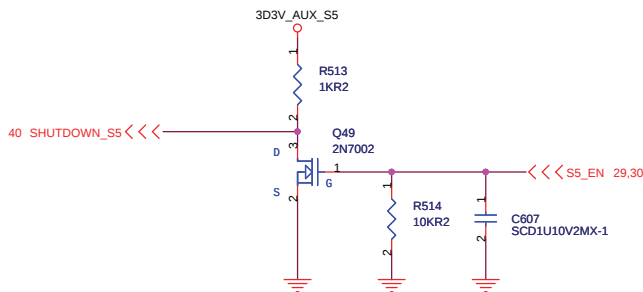


MAX8743 1D8V/1D5V

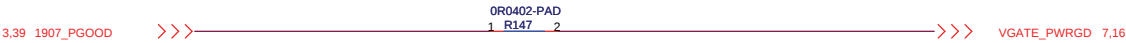


Adapter





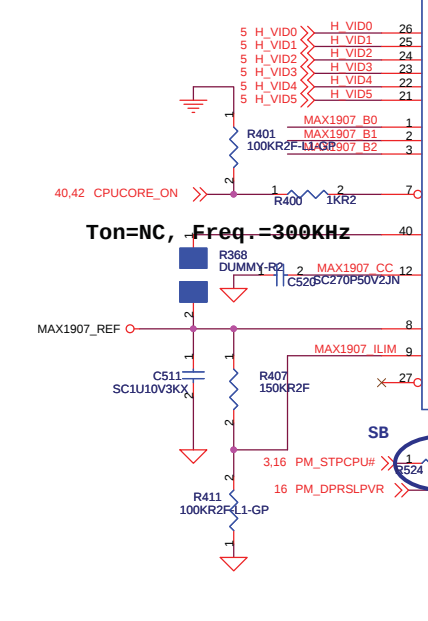
PWRGD for NB and SB



CPU_CORE - MAX1907

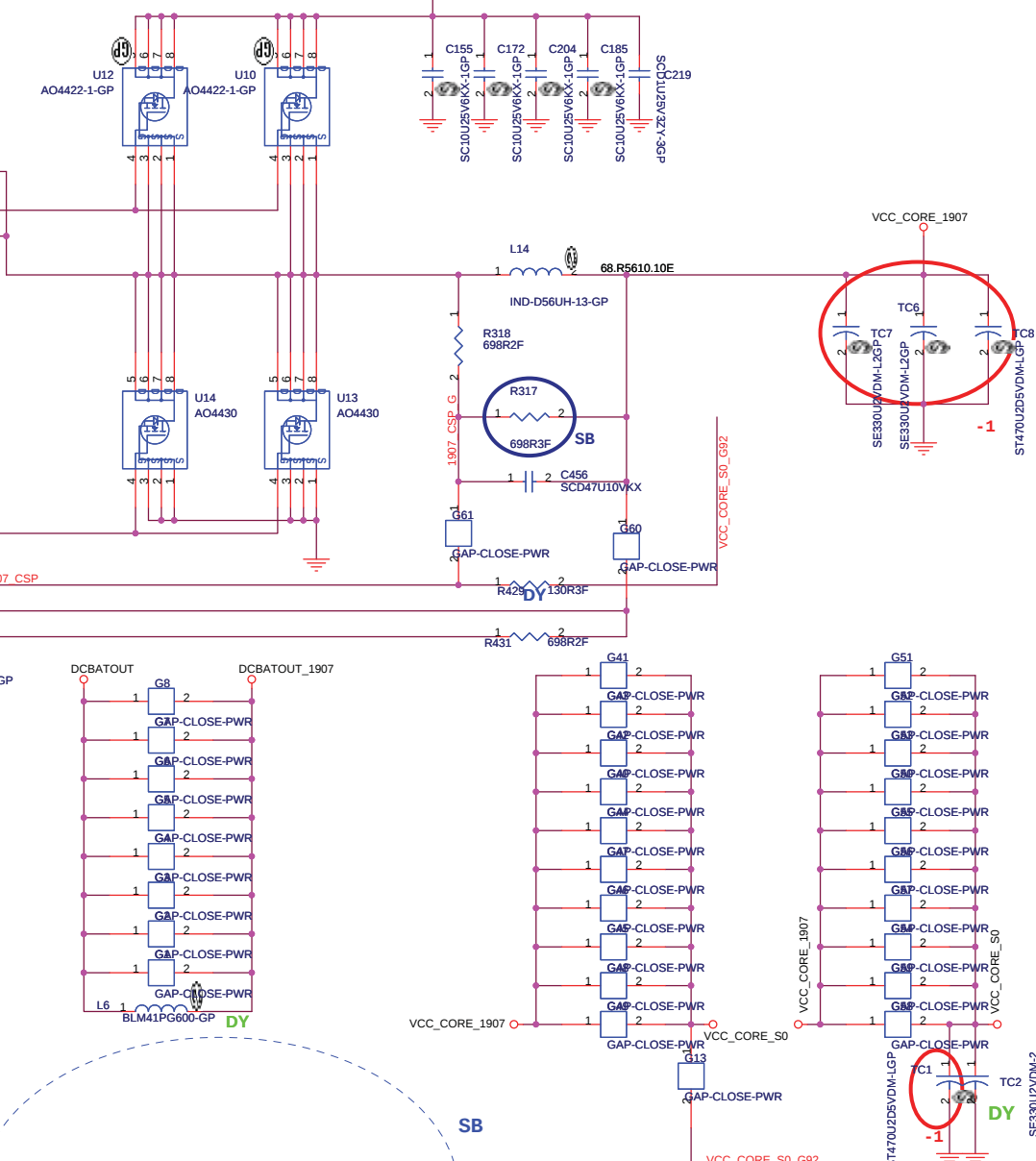
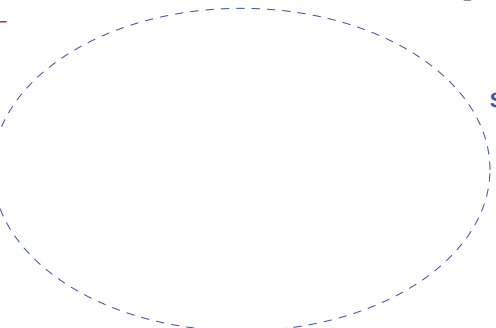
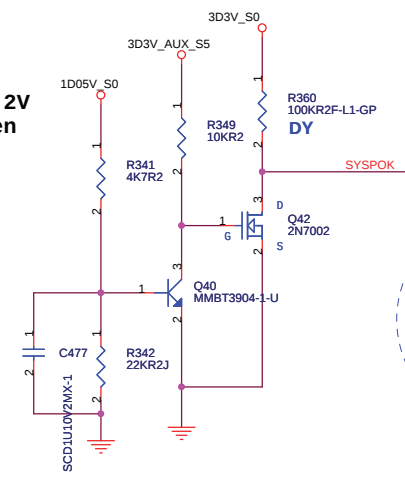
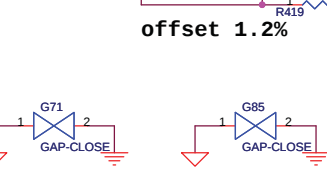
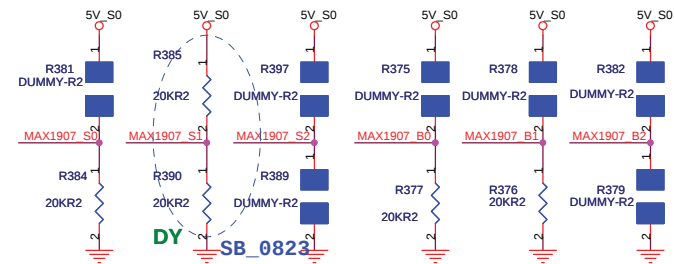
<http://hobi-elektronika.net>

3 VTT_PWRGD#
3,38 1907_PGOOD

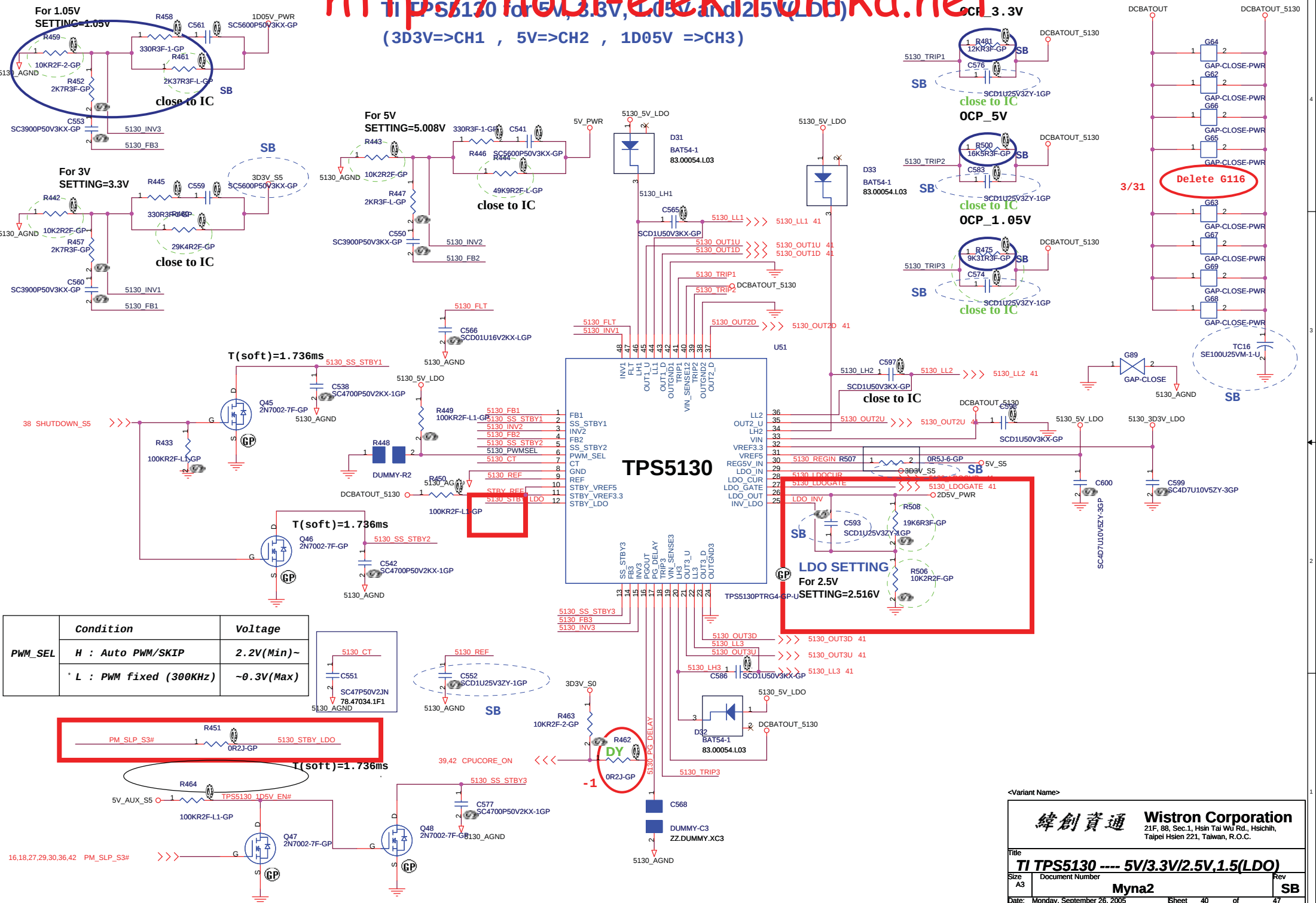


OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V Boot-up Voltage : 1.2V
, S0=L, S1=L, S2=Open, , B0=L, B1=L, B2=Open



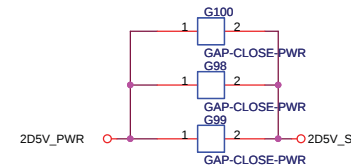
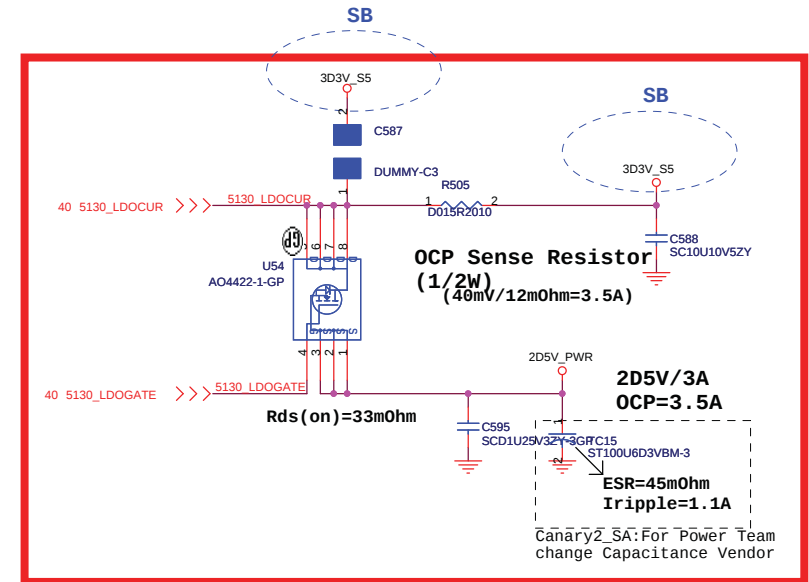
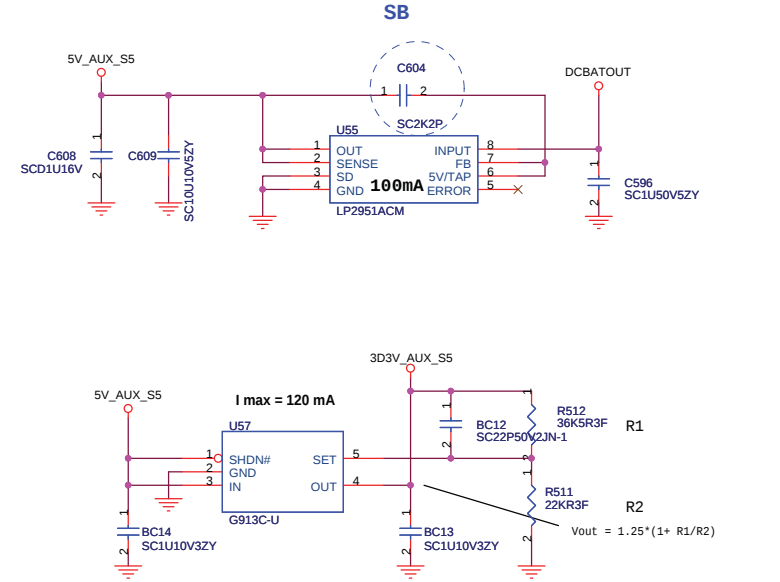
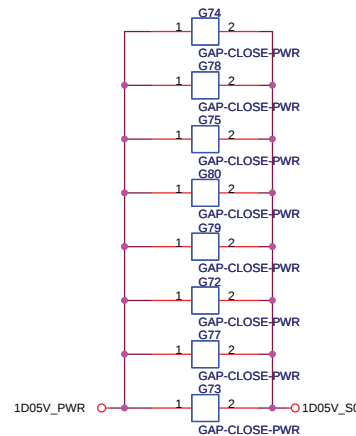
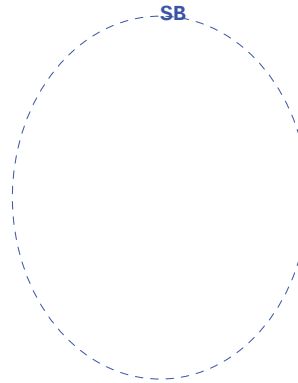
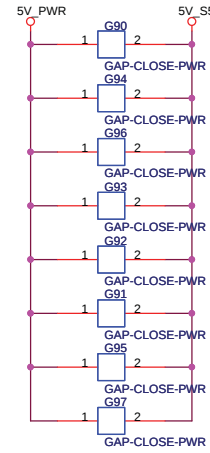
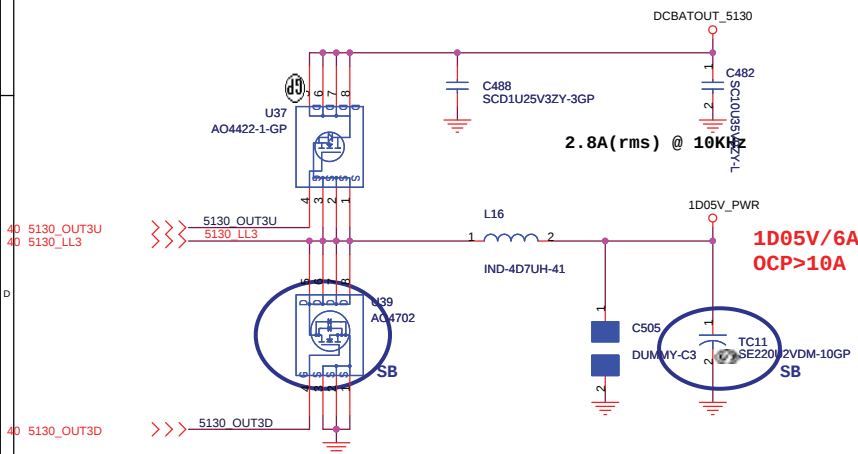
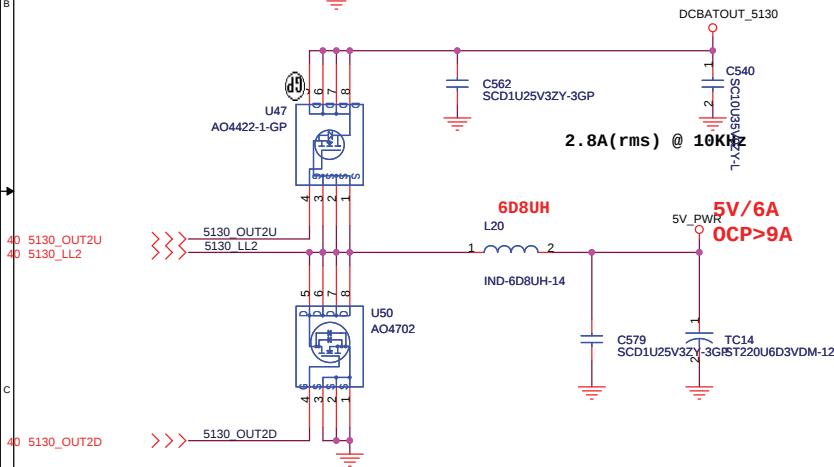
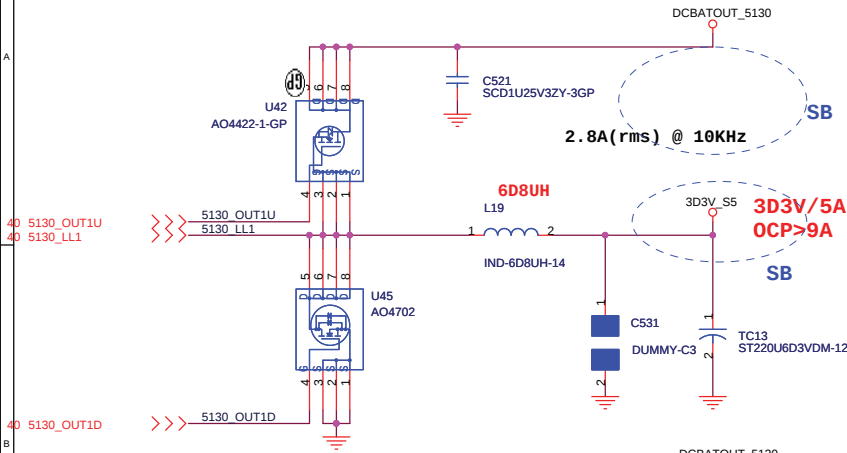
TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)
(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)

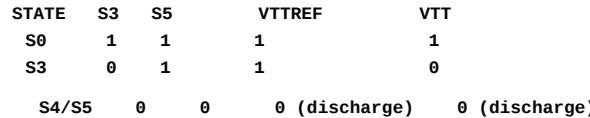


	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

Aux Power

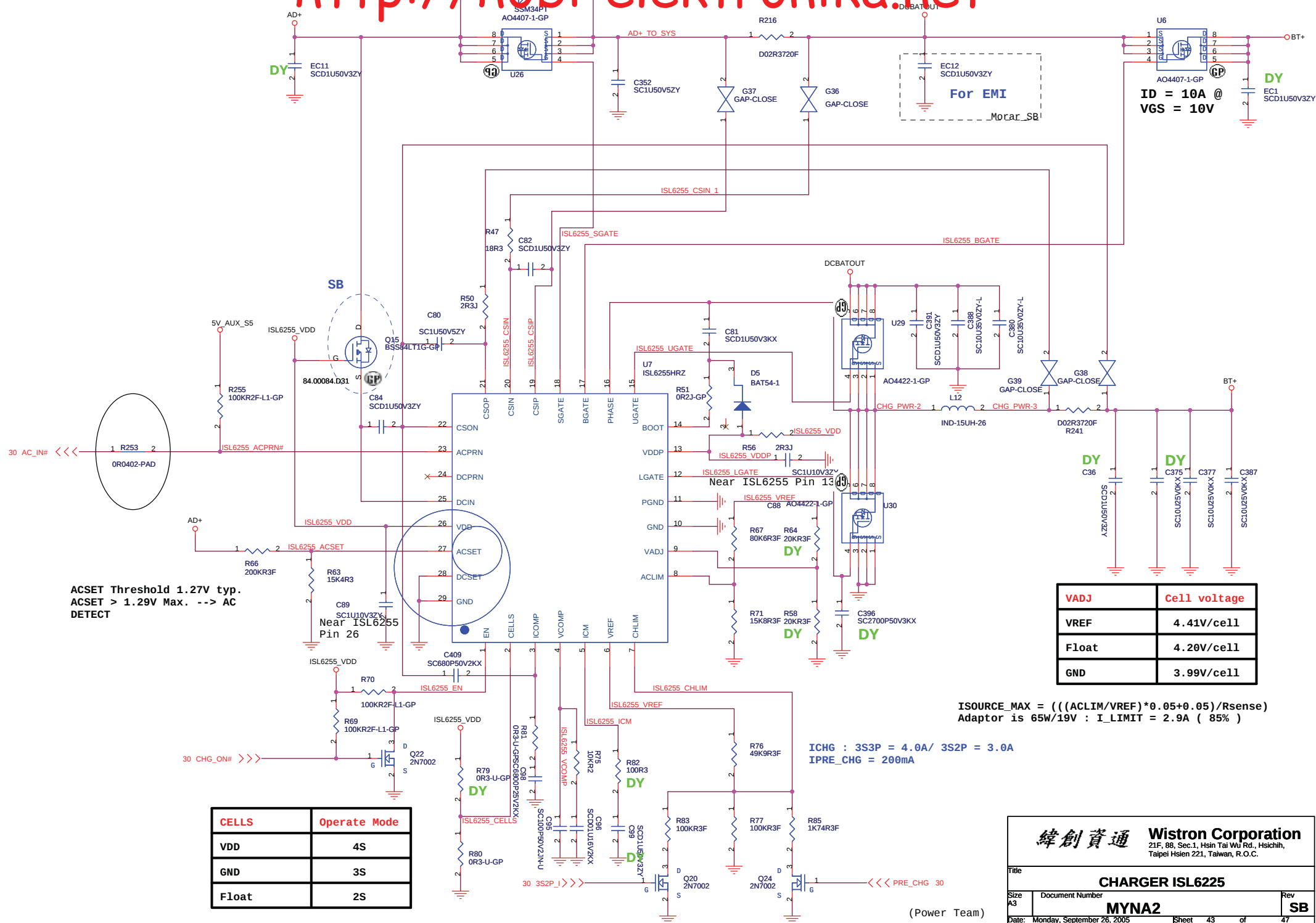
TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V (LDO)
(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

 緯創資通		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1D8V_S3/1.05V_S0			
Size A3	Document Number	Rev	
	MYNA2	SB	
Date:	Monday, September 26, 2005	Sheet	42 of 47



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

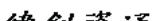
ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

```

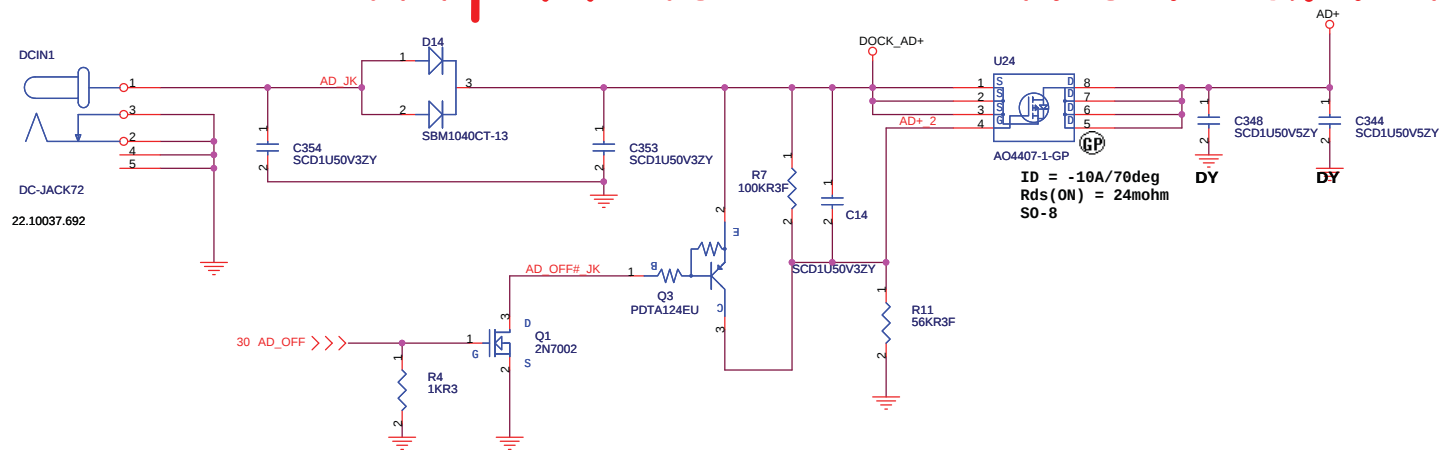
ICHG : 3S3P = 4.0A/ 3S2P = 3.0A
IPRE_CHG = 200mA

```

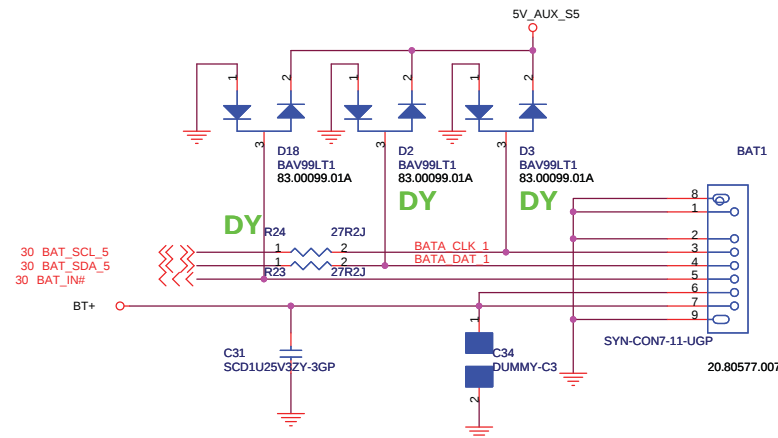
CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CHARGER ISL6225			
Size A3	Document Number	Rev	
MYNA2		SE	
Date:	Monday, September 26, 2005	Sheet 43	of 47

Adaptor in to generate DCBATOUT

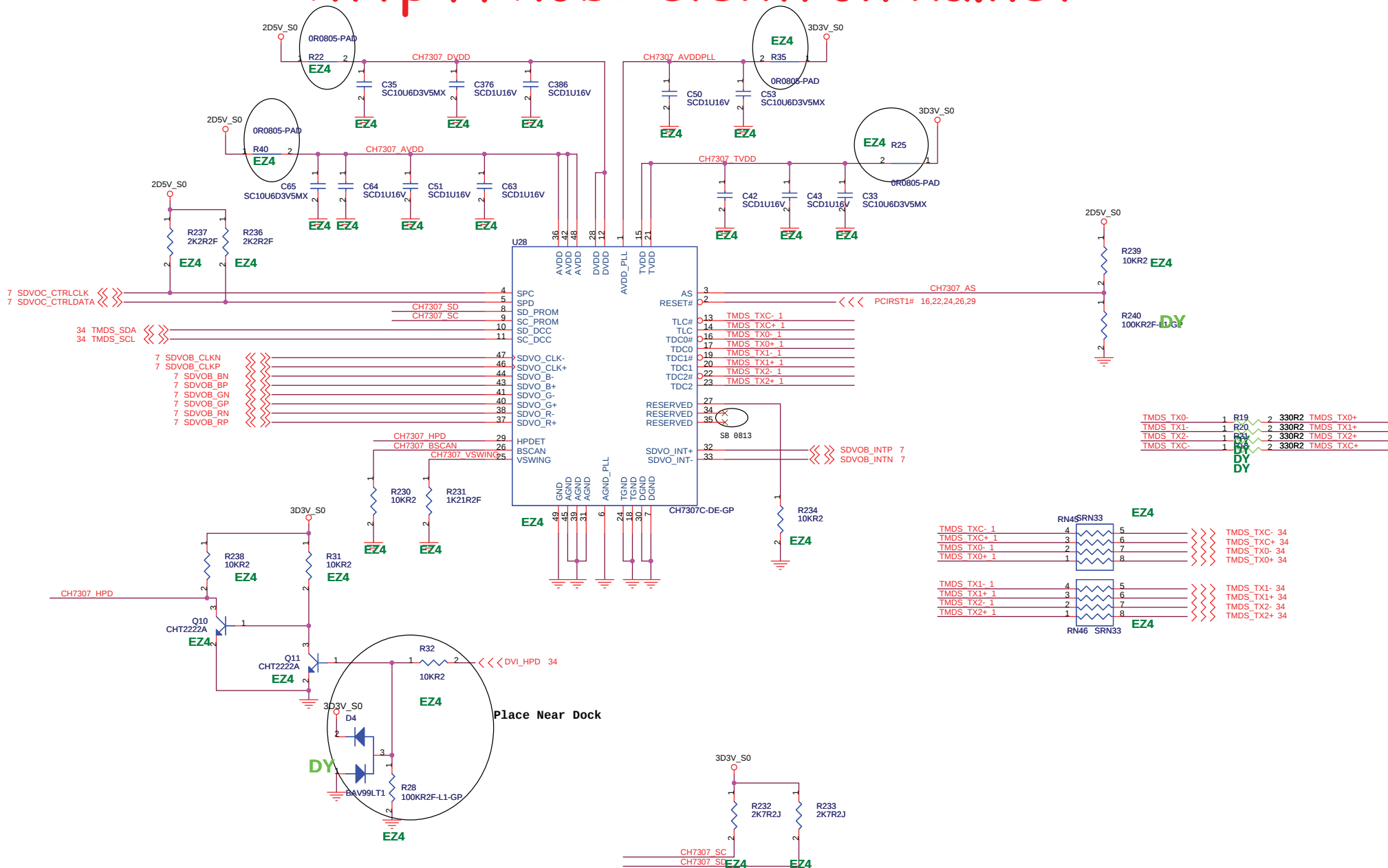


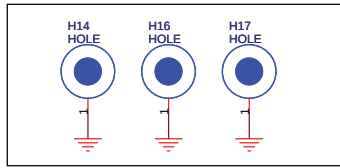
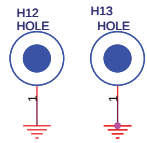
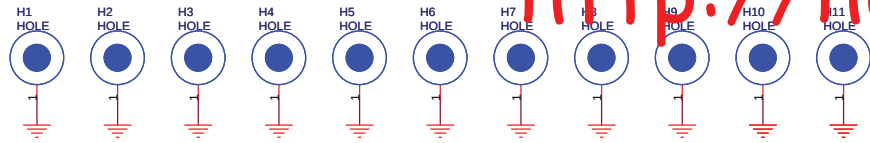
BATTERY CONNECTOR



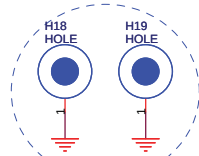
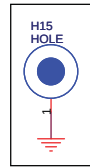
<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AD/BAT CONN			
Size A3	Document Number Myna2		Rev SB
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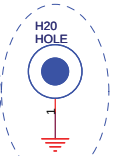




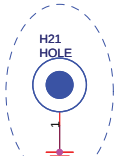
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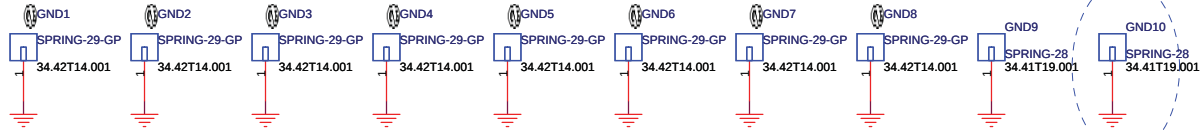
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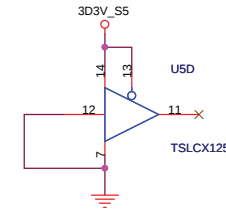
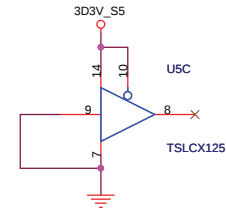
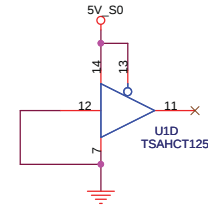
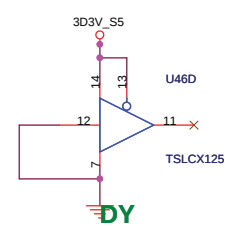
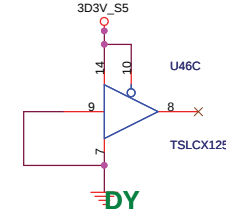
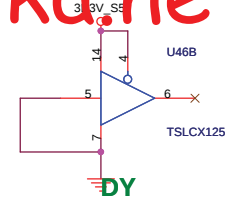
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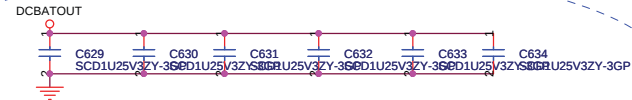
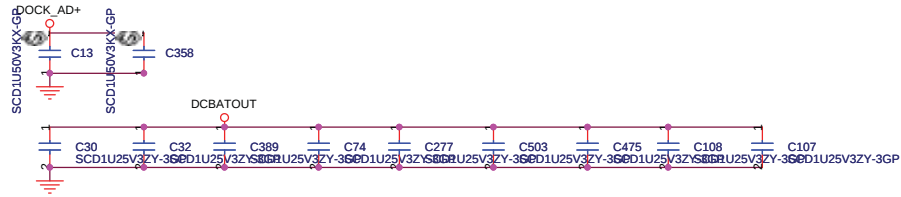
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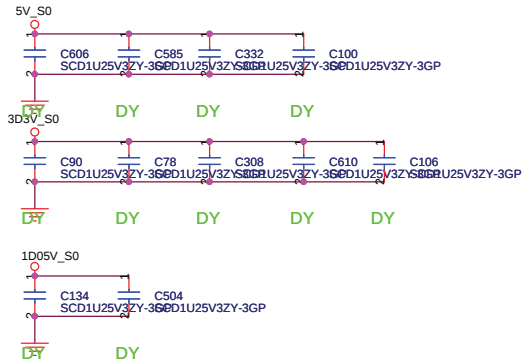
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SB



<Core Design>

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