ZY2 SYSTEM BLOCK DIAGRAM

BOM MARK

E@ EXT VGA 要打
268@ AUDIO 268 要打
D@ DOCK
D2@ DDR2 要打
SP@ 特殊(EXT VGA OR DDR2)
LC@ LOW COST 要打
ED2@ EXT VGA & DDR2 要打
CB@ CARDBUS 要打
NSF@ Non ASF 要打

I@ INT VGA 要打
888@ AUDIO 888要打
D3@ DDR3 要打
ND@ NON DOCK 要打
NLC@ NON LOW COST 要打
TPM@ INT TPM
ID2@ INT VGA & DDR2 要打
ED3@ EXT VGA & DDR3 要打
ID3@ INT VGA & DDR3 要打
ASF@ ASF 要打
NCB@ NON CARDBUS 要打

LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI

X'TAL 14.318MHZ
CLOCK GENERATOR
ICS: ICS9LPRS365BGLFT
SELGO: SLG8SP512K05
P2

Penryn 479 uFCPGA P3,P4
CPU Thermal Sensor P3

FSB 667/800/1067 Mhz

DDRII SO-DIMM 0 SO-DIMM 1 P16
Dual Channel DDR2 667/800 MHz

DDRIII SO-DIMM 0 SO-DIMM 1 P17
Dual Channel DDR3 667/800 MHz

NB Cantiga PM965 P5,P6,P7,P8,P9,P10,P11

PCIE
MXM-NB8P-GS (nVidia) VRAM 256M VRAM 512M P18

EXT_LVDS
EXT_CRT
EXT_DVI
INT_LVDS
INT_CRT
INT_DVI

LVDS
RGB

SWITCH CIRCUIT

CRT Page:19
LVDS Page:19
HDMI Page:20
DOCKING/DVI Page: 31

DVI Level Shift IC PI3VDP411LSZDE Page:20

X4 DMI interface

HDD (SATA)*2 P25
ODD (SATA) P25

SATA0
SATA1
SATA4

SB ICH9M P12,P13,P14,P15

PCI-Express
PCIE-1
New Card P23
USB5

PCIE-4
Mini Card / WLAN / TV P23
USB6

PCIE-6
X'TAL 25M
BROADCOM 10/100/1G LAN 5764M P21
SWITCH CIRCUIT Page:22
DOCK/LAN Page: 33
Transformer P22
RJ45 P22

USB 2.0
Bluetooth USB4 P22
USB Port x 4 USB0~3 P25
CCD USB7 P19

Azalia
Int MIC P27
Azalia Audio Controller ALC268 & 888 27
Audio Amplifier P27 & 28
MDC 1.5 P27

PCI Bus
X'TAL 32.768KHZ
Cardreader Controller OZ601T P29
Media Card Reader P29

LPC
TPM P23
EC (WPC8769LDG) P32
X'TAL 32.768K
SPI ROM P32
Touch Pad P32
K/B CONN. P32
VR P27
CIR P32

Connector
Speaker P28
Phone Jack P28
SPDIF P28
Line in P28
MIC Jack P28
SUBWOOFER P28

Fan Header P31

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	Block Diagram	1A

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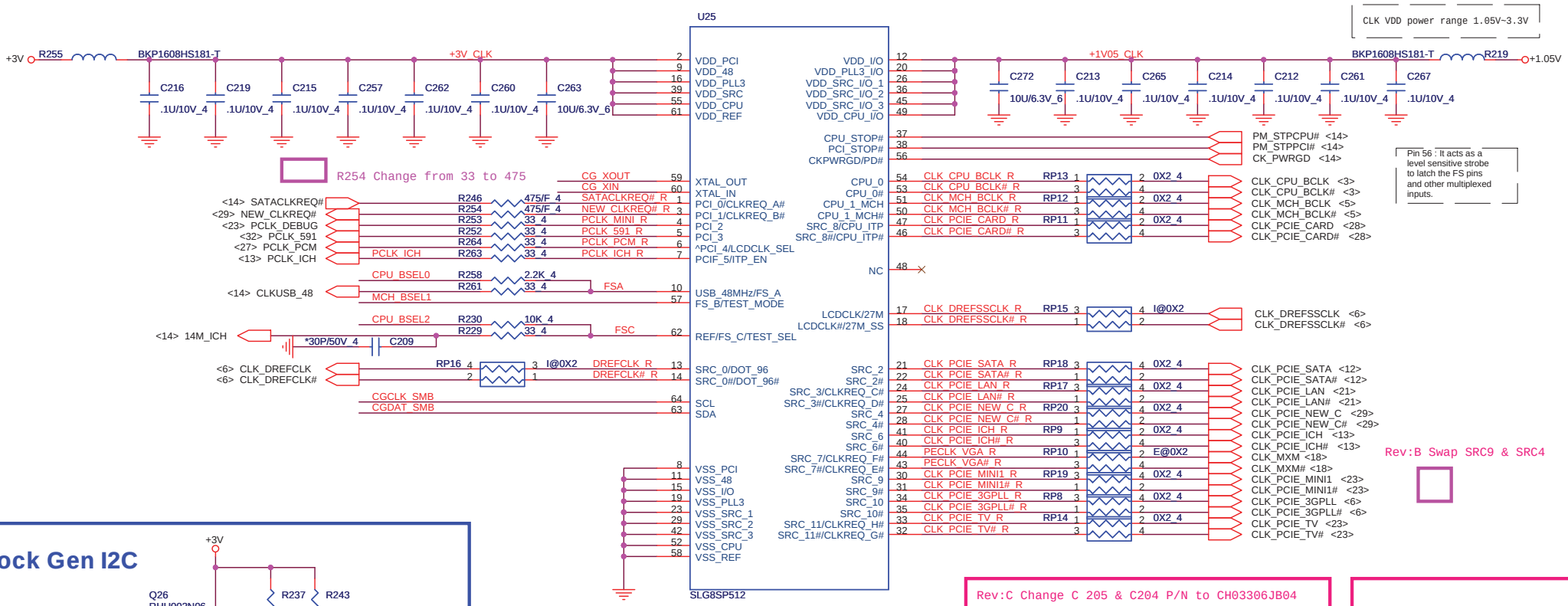
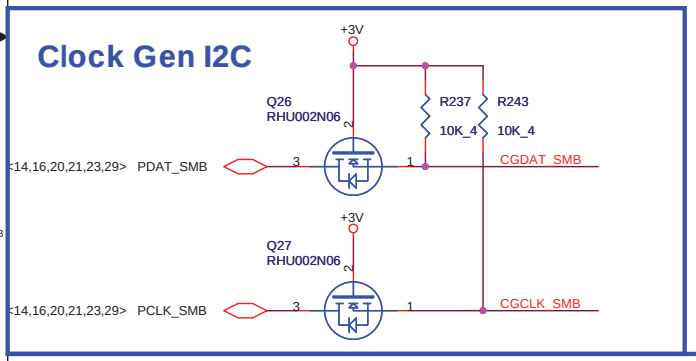
Clock Generator

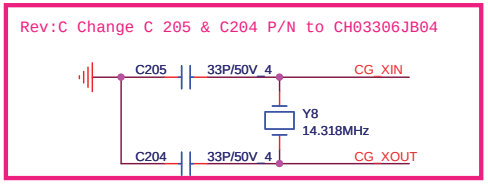


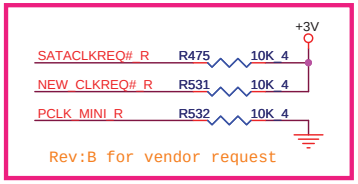
Clock Gen I2C



	QCI P/N
SLG8SP512	AL8SP512K05
ICS9LPRS365BGLFT	ALPRS365K13

Rev:C Change C 205 & C204 P/N to CH03306JB04





CPU Clock select

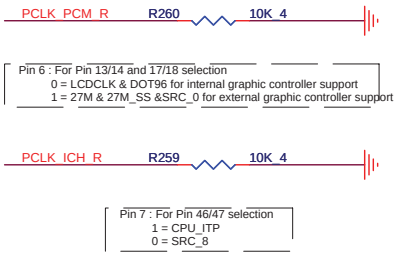
Pin 10/57/62 : For Pin CPU frequency selection

CRB Rev0.7 : 110(CBA)

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



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PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	1A
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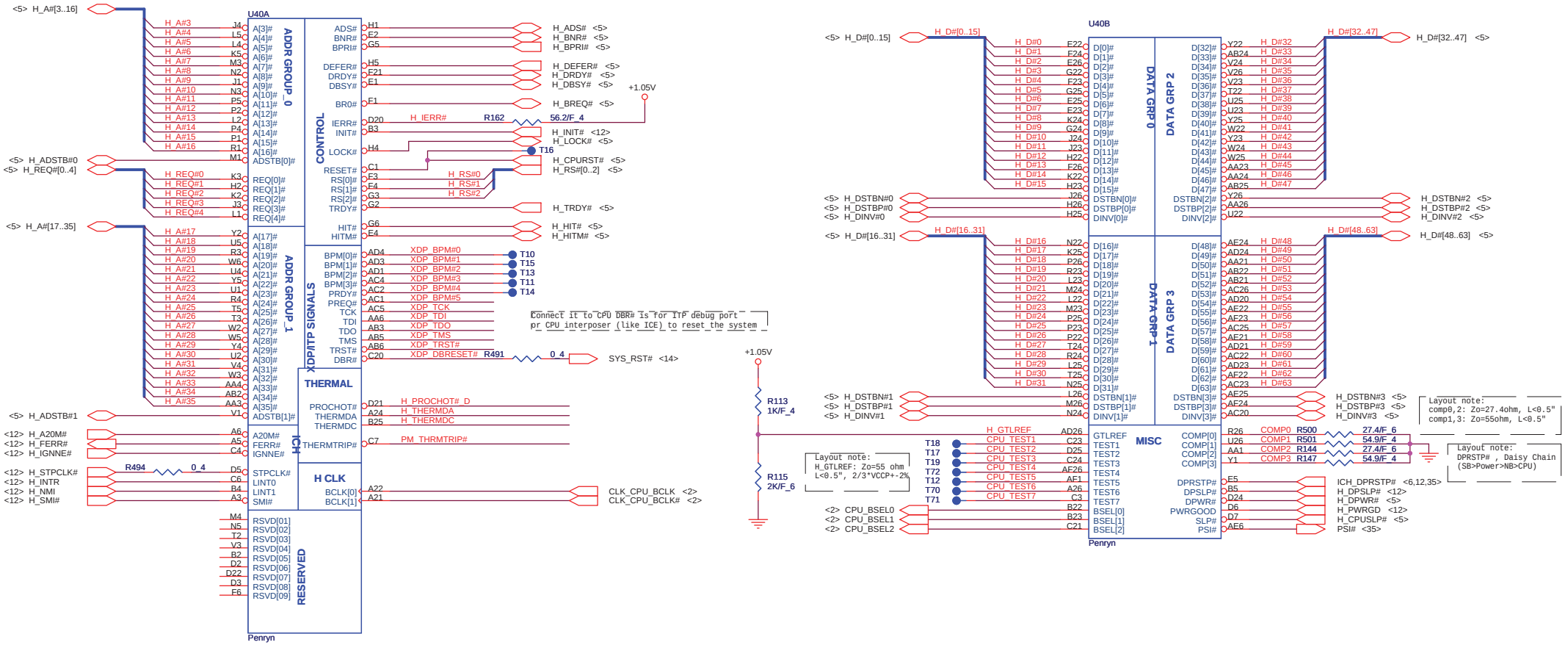
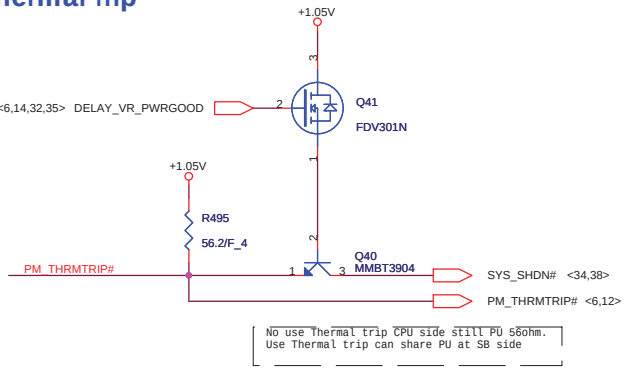
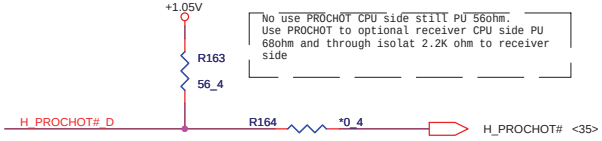


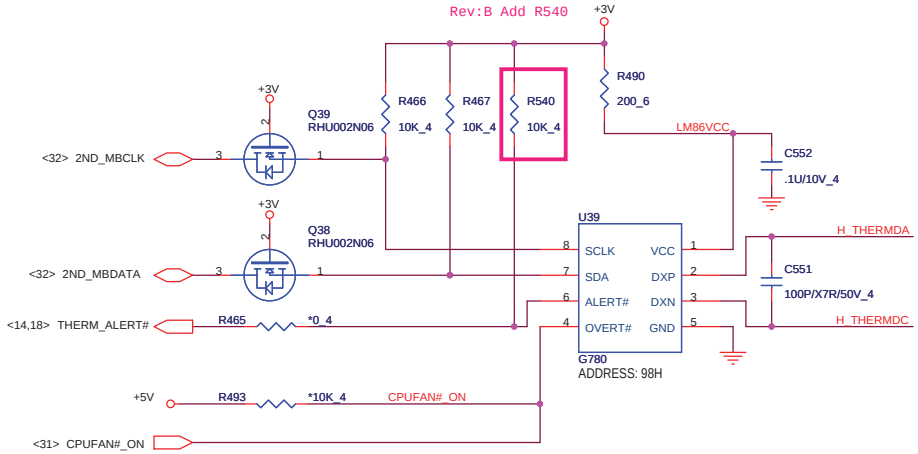
Thermal Trip



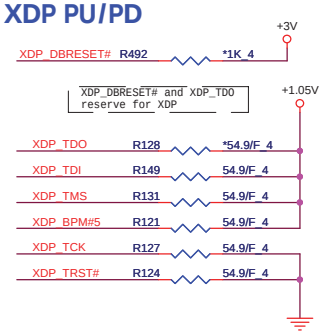
Processor hot



CPU Thermal monitor



XDP PU/PD



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CPU Host Bus	1A
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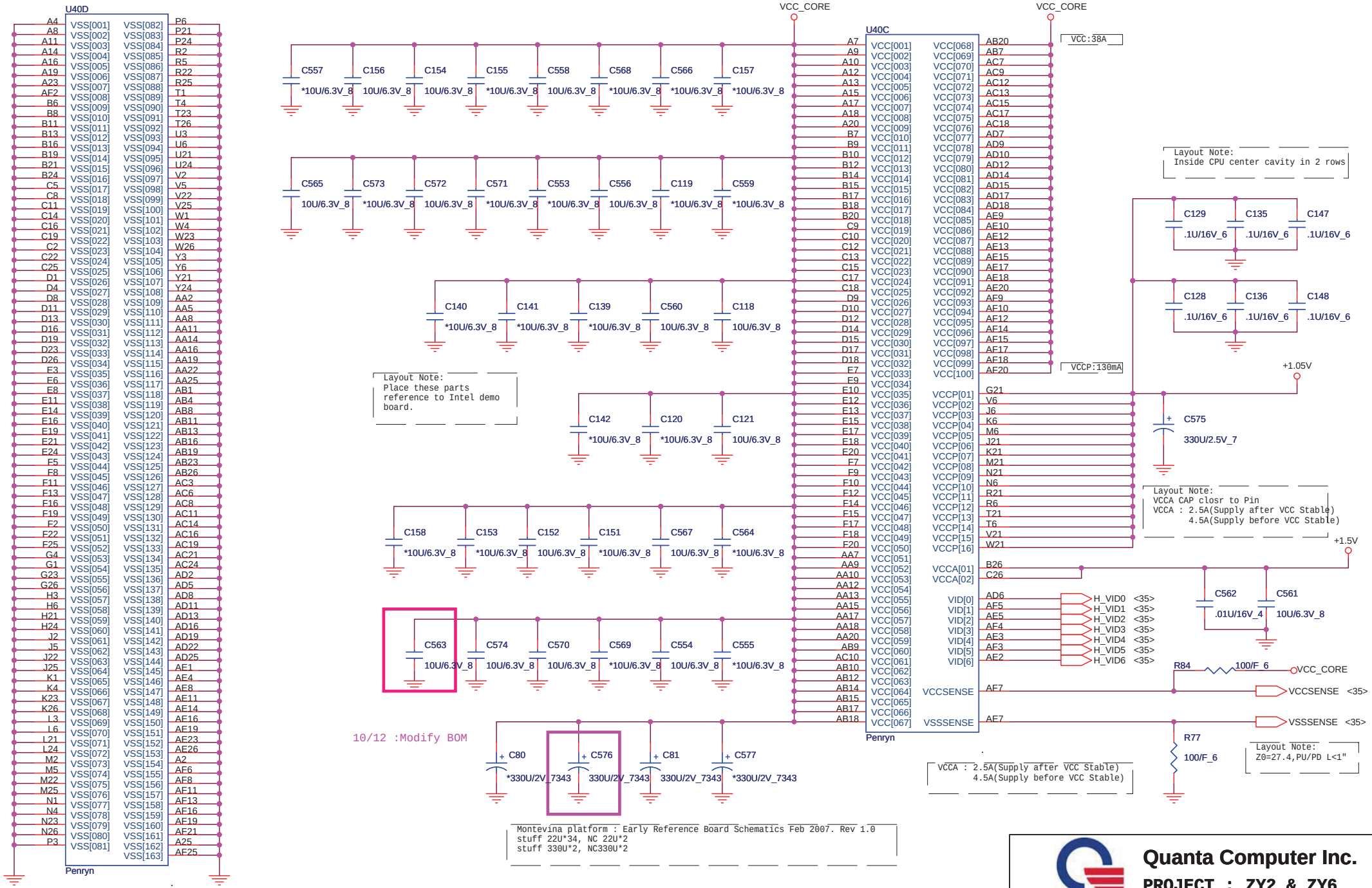
U40D
Penryn
U40C
Penryn
VCC_CORE
VCC_CORE
VCC:38A
VCCP:130mA
+1.05V
+1.5V
Layout Note:
Inside CPU center cavity in 2 rows
Layout Note:
Place these parts
reference to Intel demo
board.
Layout Note:
VCCA CAP closr to Pin
VCCA : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
VCCA : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)
Layout Note:
Z0=27.4,PU/PD L<1"
10/12 :Modify BOM
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
CPU Power
Rev
1A
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	QCI P/N
Intel Cantiga (G)M	AJ0QT620T01
Intel Cantiga (P)M	AJ0QT780T03

+1.05V
R177 221/F_4
0.3125*VCCP
WIDE(10):SPACING(20) ,
L<0.5"
H_SWING
R175 100/F_4
C178 0.1U/10V_4
Capacitor close to the pin

H_RCOMP
R464 24.9/F_4
WIDE(10):SPACING(20) ,
L<0.5"

+1.05V
R484 1K/F_4
R482 2K/F_4
2/3*VCCP
WIDE(10):SPACING(20),
L<0.5"

U38A
HOST
SP@CANTIGA_1p2

<3> H_D#[0..63]
H_D#0 F2 H_D#_0
H_D#1 G8 H_D#_1
H_D#2 F8 H_D#_2
H_D#3 E6 H_D#_3
H_D#4 G2 H_D#_4
H_D#5 H6 H_D#_5
H_D#6 H2 H_D#_6
H_D#7 E6 H_D#_7
H_D#8 D4 H_D#_8
H_D#9 H3 H_D#_9
H_D#10 M9 H_D#_10
H_D#11 M11 H_D#_11
H_D#12 J1 H_D#_12
H_D#13 J2 H_D#_13
H_D#14 N12 H_D#_14
H_D#15 J6 H_D#_15
H_D#16 P2 H_D#_16
H_D#17 L2 H_D#_17
H_D#18 R2 H_D#_18
H_D#19 N9 H_D#_19
H_D#20 L6 H_D#_20
H_D#21 M5 H_D#_21
H_D#22 J3 H_D#_22
H_D#23 N2 H_D#_23
H_D#24 R1 H_D#_24
H_D#25 N5 H_D#_25
H_D#26 N6 H_D#_26
H_D#27 P13 H_D#_27
H_D#28 N8 H_D#_28
H_D#29 L7 H_D#_29
H_D#30 N10 H_D#_30
H_D#31 M3 H_D#_31
H_D#32 Y3 H_D#_32
H_D#33 AD14 H_D#_33
H_D#34 Y6 H_D#_34
H_D#35 Y10 H_D#_35
H_D#36 Y12 H_D#_36
H_D#37 Y14 H_D#_37
H_D#38 Y7 H_D#_38
H_D#39 W2 H_D#_39
H_D#40 AA8 H_D#_40
H_D#41 Y9 H_D#_41
H_D#42 AA13 H_D#_42
H_D#43 AA9 H_D#_43
H_D#44 AA11 H_D#_44
H_D#45 AD11 H_D#_45
H_D#46 AD10 H_D#_46
H_D#47 AD13 H_D#_47
H_D#48 AE12 H_D#_48
H_D#49 AE9 H_D#_49
H_D#50 AA2 H_D#_50
H_D#51 AD8 H_D#_51
H_D#52 AA3 H_D#_52
H_D#53 AD3 H_D#_53
H_D#54 AD7 H_D#_54
H_D#55 AE14 H_D#_55
H_D#56 AE3 H_D#_56
H_D#57 AC1 H_D#_57
H_D#58 AE3 H_D#_58
H_D#59 AC3 H_D#_59
H_D#60 AE11 H_D#_60
H_D#61 AE8 H_D#_61
H_D#62 AG2 H_D#_62
H_D#63 AD6 H_D#_63

H_SWING C5 H_SWING
H_RCOMP E3 H_RCOMP

<3> H_CPURST# C12 H_CPURST#
<3> H_CPUSLP# E11 H_CPUSLP#

H_AVREF A11 H_AVREF
H_DVREF B11 H_DVREF

H_A#_3 A14 H_A#3
H_A#_4 C15 H_A#4
H_A#_5 F16 H_A#5
H_A#_6 H13 H_A#6
H_A#_7 C18 H_A#7
H_A#_8 M16 H_A#8
H_A#_9 J13 H_A#9
H_A#_10 P16 H_A#10
H_A#_11 R16 H_A#11
H_A#_12 N17 H_A#12
H_A#_13 M13 H_A#13
H_A#_14 E17 H_A#14
H_A#_15 P17 H_A#15
H_A#_16 F17 H_A#16
H_A#_17 G20 H_A#17
H_A#_18 B19 H_A#18
H_A#_19 J16 H_A#19
H_A#_20 E20 H_A#20
H_A#_21 H16 H_A#21
H_A#_22 J20 H_A#22
H_A#_23 L17 H_A#23
H_A#_24 A17 H_A#24
H_A#_25 B17 H_A#25
H_A#_26 L16 H_A#26
H_A#_27 C21 H_A#27
H_A#_28 J17 H_A#28
H_A#_29 H20 H_A#29
H_A#_30 B18 H_A#30
H_A#_31 K17 H_A#31
H_A#_32 B20 H_A#32
H_A#_33 F21 H_A#33
H_A#_34 K21 H_A#34
H_A#_35 L20 H_A#35
H_A#[3..35] <3>

H_ADS# H12 H_ADS# <3>
H_ADSTB#_0 B16 H_ADSTB#0 <3>
H_ADSTB#_1 G17 H_ADSTB#1 <3>
H_BNR# A9 H_BNR# <3>
H_BPRI# F11 H_BPRI# <3>
H_BREQ# G12 H_BREQ# <3>
H_DEFER# E9 H_DEFER# <3>
H_DBSY# B10 H_DBSY# <3>
HPLL_CLK AH7 CLK_MCH_BCLK <2>
HPLL_CLK# AH6 CLK_MCH_BCLK# <2>
H_DPWR# J11 H_DPWR# <3>
H_DRDY# F9 H_DRDY# <3>
H_HIT# H9 H_HIT# <3>
H_HITM# E12 H_HITM# <3>
H_LOCK# H11 H_LOCK# <3>
H_TRDY# C9 H_TRDY# <3>

H_DINV#_0 J8 H_DINV#0
H_DINV#_1 L3 H_DINV#1
H_DINV#_2 Y13 H_DINV#2
H_DINV#_3 Y1 H_DINV#3
H_DINV#[3..0] <3>

H_DSTBN#_0 L10 H_DSTBN#0
H_DSTBN#_1 M7 H_DSTBN#1
H_DSTBN#_2 AA5 H_DSTBN#2
H_DSTBN#_3 AE6 H_DSTBN#3
H_DSTBN#[3..0] <3>

H_DSTBP#_0 L9 H_DSTBP#0
H_DSTBP#_1 M8 H_DSTBP#1
H_DSTBP#_2 AA6 H_DSTBP#2
H_DSTBP#_3 AE5 H_DSTBP#3
H_DSTBP#[3..0] <3>

H_REQ#_0 B15 H_REQ#0
H_REQ#_1 K13 H_REQ#1
H_REQ#_2 F13 H_REQ#2
H_REQ#_3 B13 H_REQ#3
H_REQ#_4 B14 H_REQ#4
H_REQ#[0..4] <3>

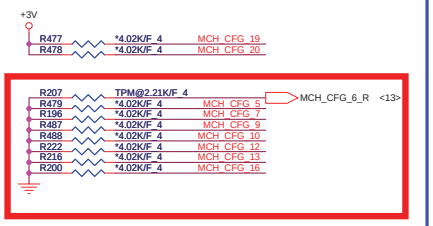
H_RS#_0 B6 H_RS#0
H_RS#_1 F12 H_RS#1
H_RS#_2 C8 H_RS#2
H_RS#[0..2] <3>

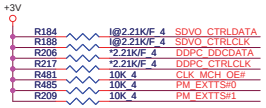
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size | Document Number: GMCH HOST | Rev: 1A
Date: Tuesday, April 08, 2008 | Sheet 5 of 40

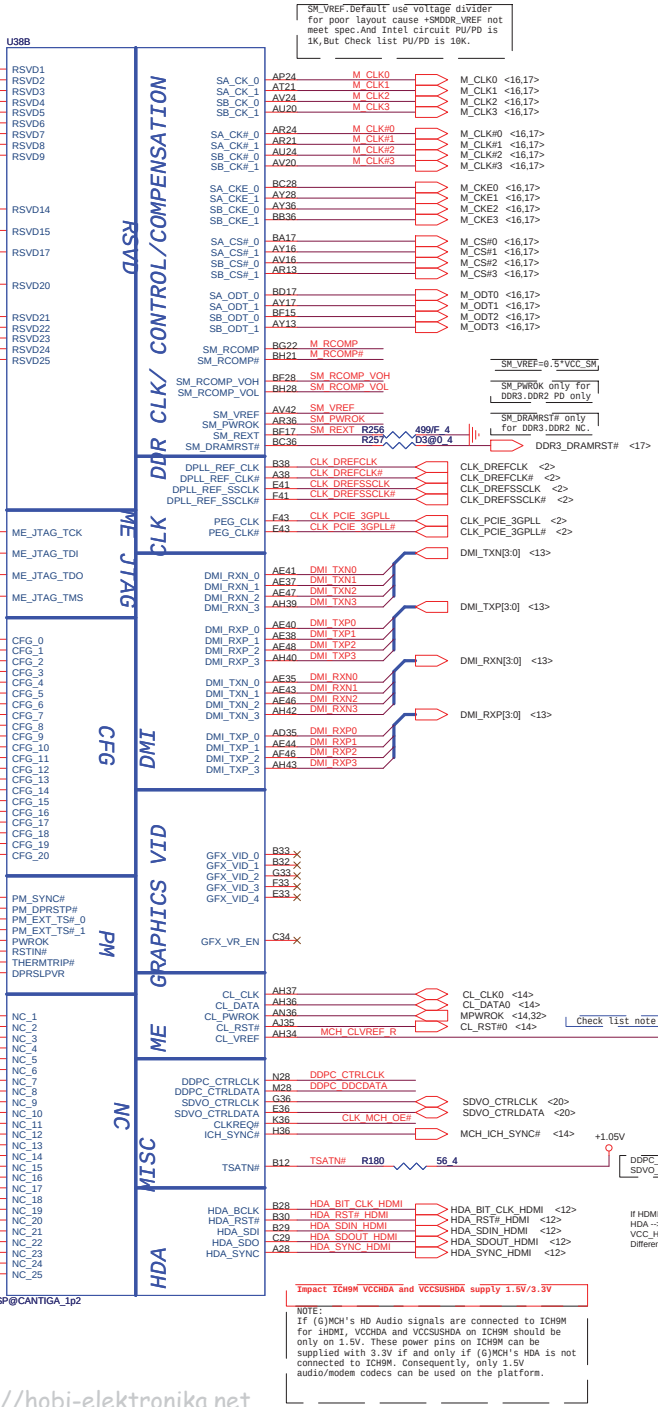
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin







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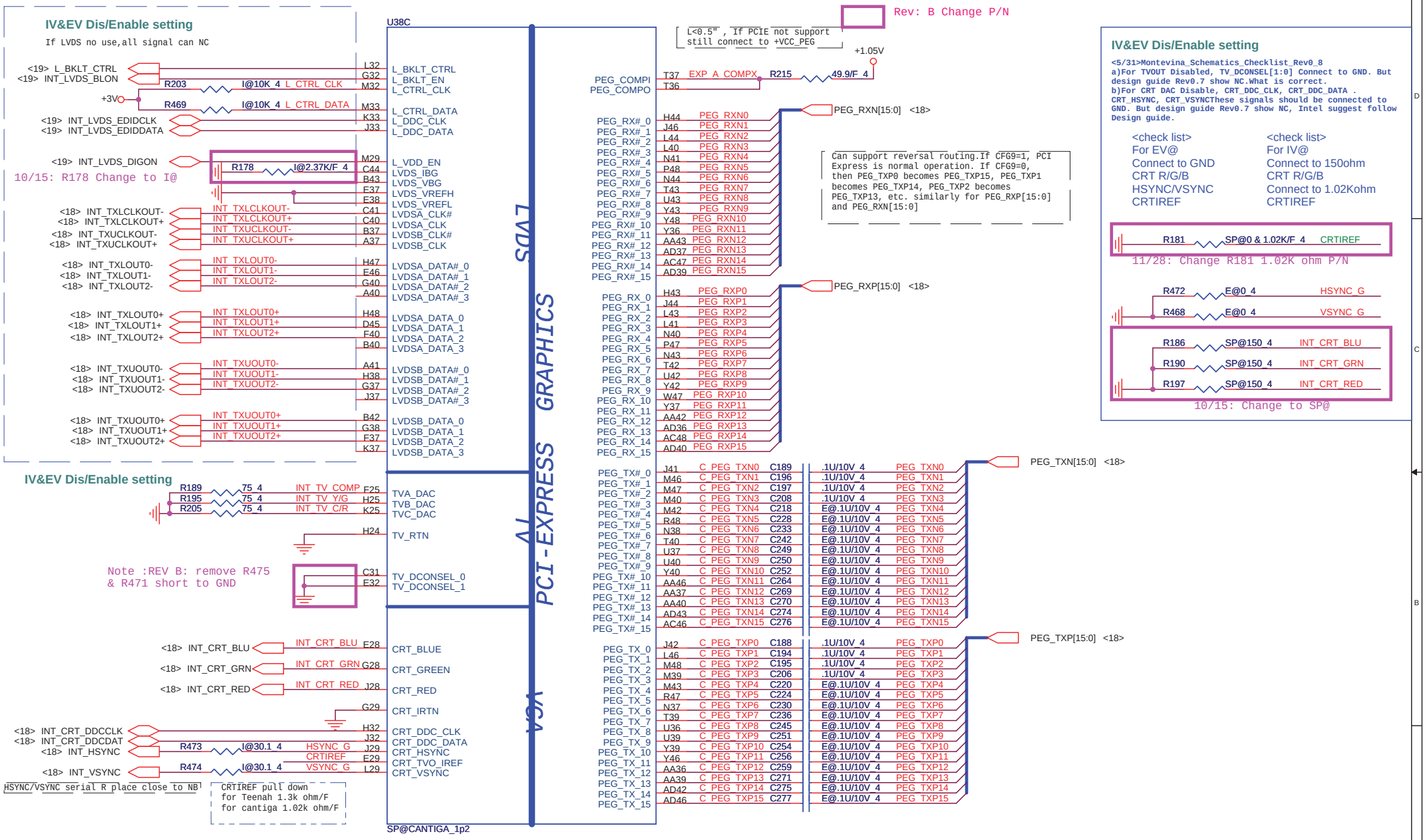
PROJECT : ZY2 & ZY6			
Size	Document Number: GMCH DMI		Rev: 1A
Date: Tuesday, April 08, 2008	Sheet 6 of 40		



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PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VGA	1A

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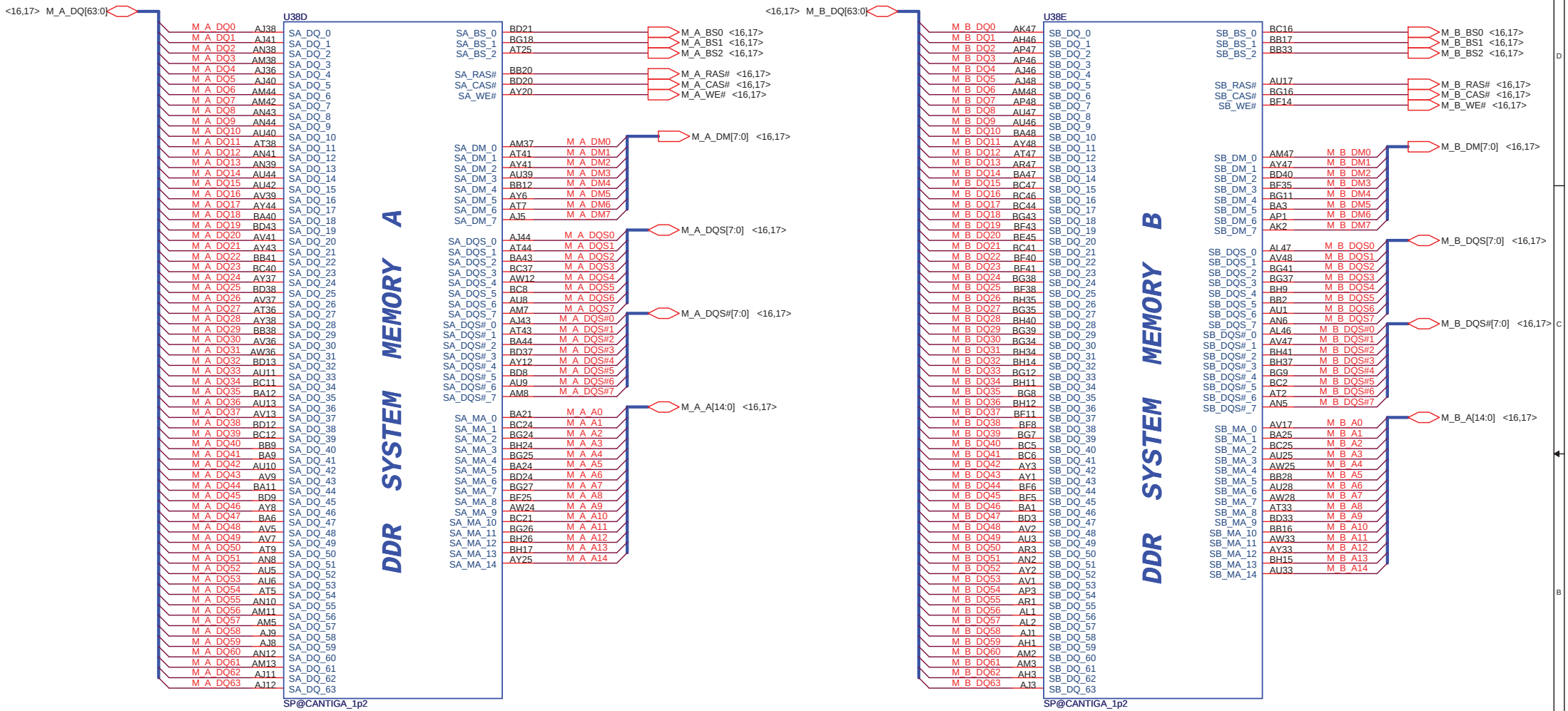

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PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH DDRII	1A

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Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL, VCCA_MPLL, VCCA_PEG_PLLVCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

1.8V
Internal connect to power

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND
SP@:INT 上 1 U
EXT 上 0 ohm

Place close to the GMCH
Cavity Capacitors
Place on the edga
Place close to the GMCH

U38G
U38F
VCC SM POWER
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC CORE POWER
VCC NCTF
SP@CANTIGA_1p2

+VDR_SUS
+1.05V_AXG
+1.05V

C519 22U/6V_8
C521 22U/6V_8
C244 0.1U/10V_4
C518 330U/2.5V_7
C231 .1U/10V_4
C225 .22U/6V_4
C226 .22U/6V_4
C210 22U/6V_8
C524 330U/2.5V_7
C191 I@330U/2.5V_7343
C192 I@330U/2.5V_7343
C200 I@.47U/6V_4
C237 SP@0_6
C217 I@10U/10V_8
C201 I@22U/6V_8
C247 I@.1U/10V_4
C203 I@.1U/10V_4
C268 .1U/10V_4
C239 .1U/10V_4
C255 .22U/6V_4
C253 .22U/6V_4
C238 .47U/6V_4
C266 1U/6V_4
C258 1U/6V_4
R227 I@0_8
R228 I@0_8
R242 I@10/F_4
R238 I@10/F_4

VCC_SM_1 … VCC_SM_42 / VCC_SM_36/NC … VCC_SM_42/NC
VCC_AXG_1 … VCC_AXG_42
VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60
VCC_SM_LF1 … VCC_SM_LF7
VCC_AXG_SENSE
VSS_AXG_SENSE
VCC_1 … VCC_35
VCC_NCTF_1 … VCC_NCTF_44

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

Date: Tuesday, April 08, 2008 Sheet 9 of 40

Power consumption reference to Intel 644135 Cantiga chipset EDS Volume1. Section 10

IV&EV Dis/Enable setting Design guide Table 72

External Graphics (GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

1.05V 64.8mA for A/B

3.3V 73mA

3.3V 2.68mA

1.05V FSB-1067 852mA

1.05V 24mA

1.05V 139.2mA

1.8V 13.2mA

1.5V 414uA

1.05V 50mA

1.05V 321.35mA

1.8V DDR2-800 124mA

1.05V DDR2-800 720mA

1.05V DDR2-800 26mA

1.8V 118.8mA

3.3V 105.3mA

1.5V 50mA

3.3V 24.15mA for VCCA_TVA_DAC 39.48mA for VCCA_TVB_DAC 24.15mA for VCCA_TVC_DAC Total 87.78mA

1.05V 1782mA

1.5V 58.67mA

1.05V 157.2mA

1.5V 48.363mA for CRT 5mA for TV

1.05V 456mA

1.05V Internal connect to power

1.05V 50mA

1.8V 60.31mA

VCCD_QDAC share to TV and CRT

Power Rail Differences between the Teenah and Cantiga Chipset Family

Power Net Name	Cantiga(V)	Tennah(V)	Tennah Current
VCC_AXG_# VCC_AXG_NCTF_#	1.05V	1.25V	6326.84mA Cantiga use
VCCA_PEG_BG	1.5V	3.3V	400uA
VCCA_DPLLA	1.05V	1.25V	100mA
VCCA_DPLLB	1.05V	1.25V	100mA
VCCA_SM_#	1.05V	1.25V	1065mA
VCCA_HPLL	1.05V	1.25V	50mA
VCCA_MPLL	1.05V	1.25V	150mA
VCCA_SM_CK_#	1.05V	1.25V	35mA
VCCA_PEG_PLL	1.05V	1.25V	100mA
VCC_AXF_#	1.05V	1.25V	495mA
VCCD_HPLL	1.05V	1.25V	250mA
VCCD_PEG_PLL	1.05V	1.25V	100mA

Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size | Document Number: GMCH POWER | Rev: 1A
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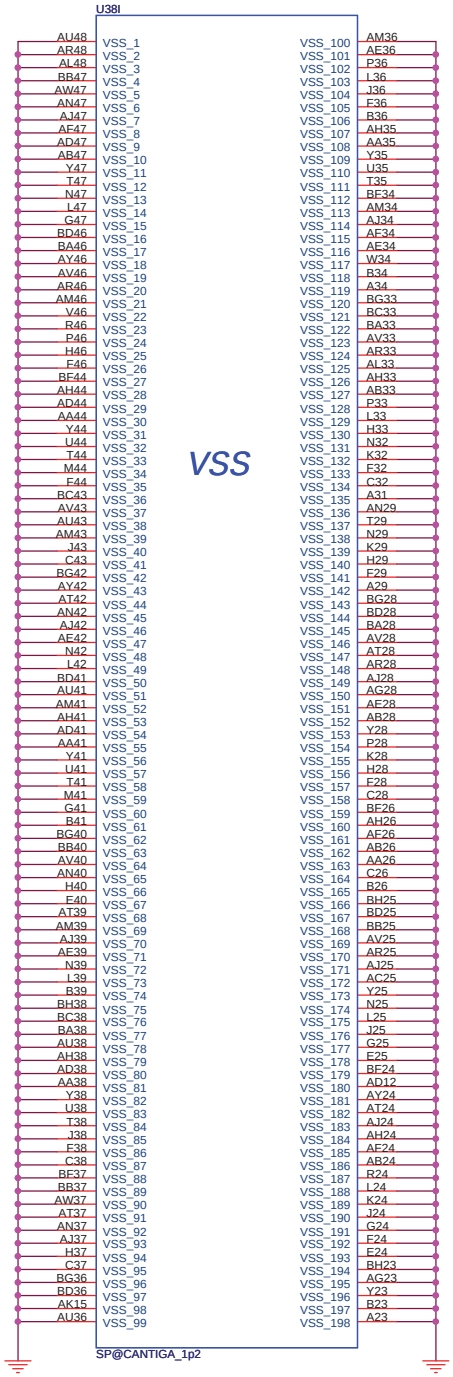
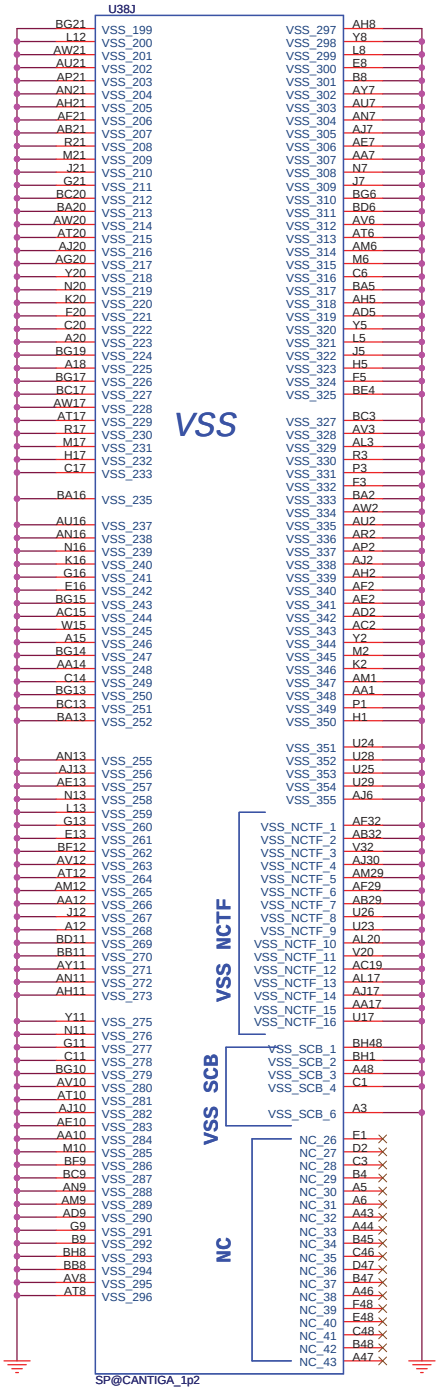
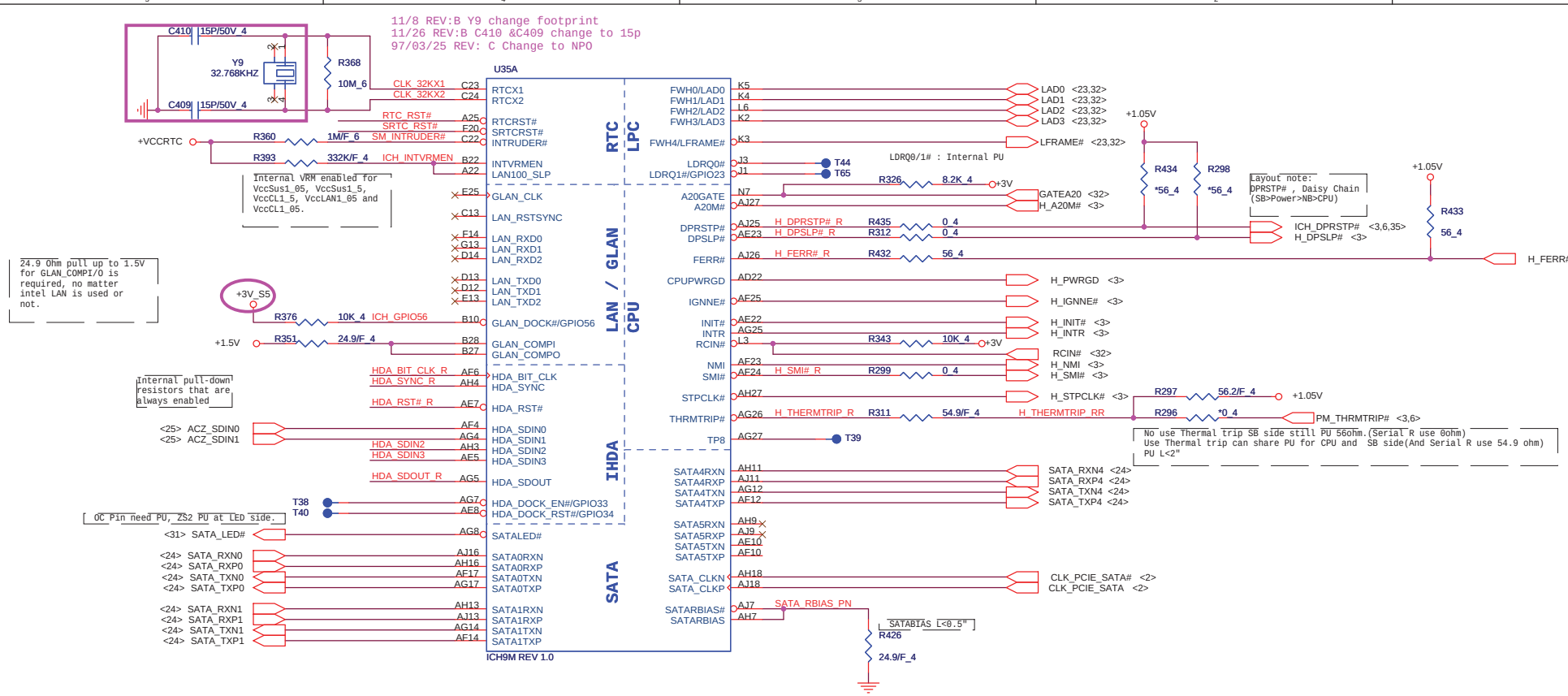
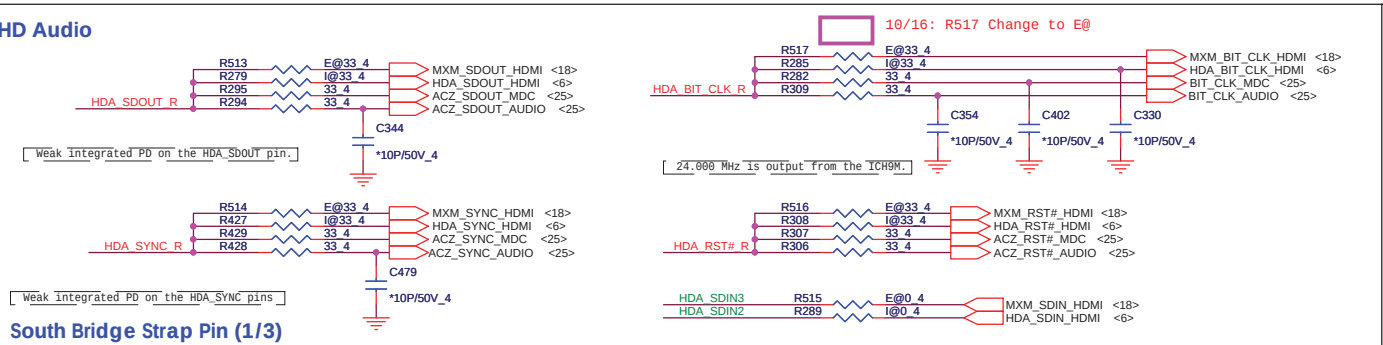




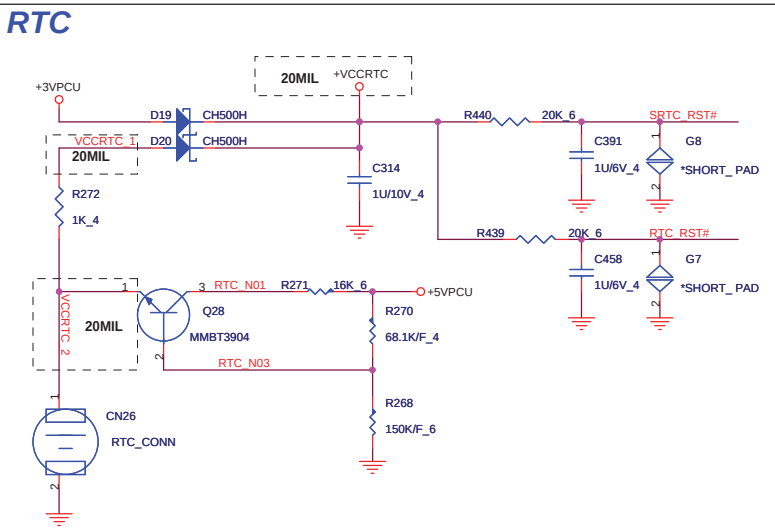
Quanta Computer Inc.		
PROJECT : ZY2 & ZY6		
Size	Document Number: GMCH VSS	Rev: 1A
Date: Tuesday, April 08, 2008	Sheet 11 of 40	





South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	<14> ICH_TP3 — ICH_TP3 — R406 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R310 *1K_2 — +3V



Quanta Computer Inc.	PROJECT : ZY2 & ZY6		
Size	Document Number: ICH9M HOST		Rev: 1A
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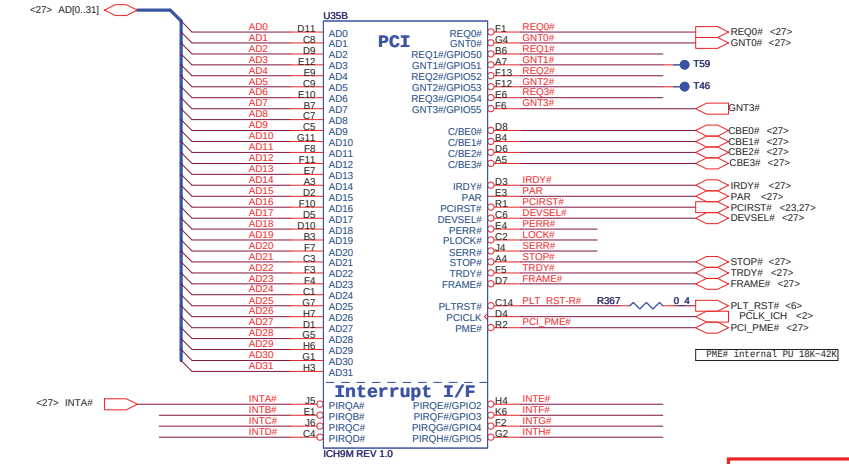
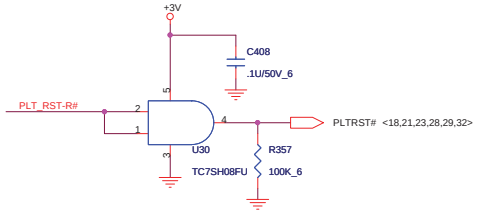
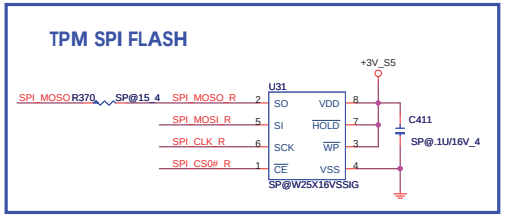
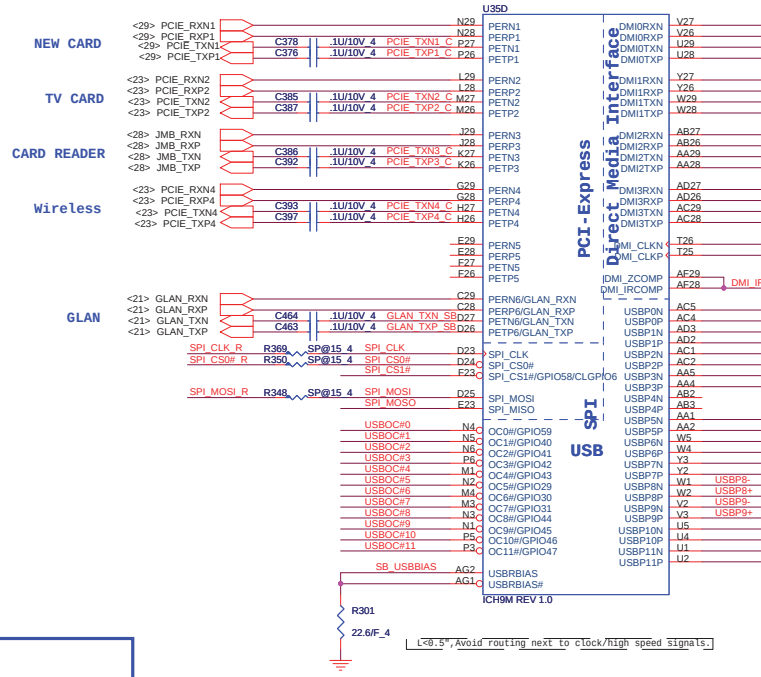


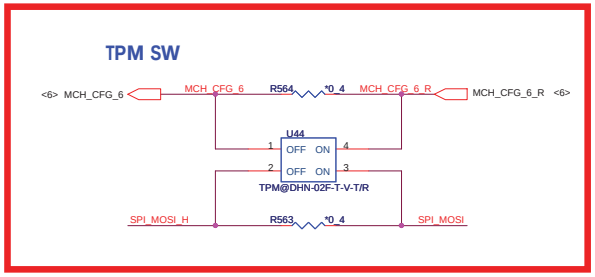
TM & AS	Y
LOW COST	N





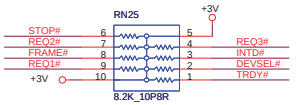


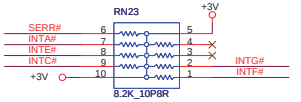
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTA#	OZ601T

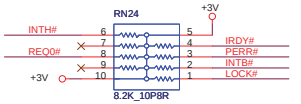


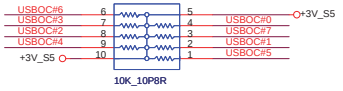
South Bridge Strap Pin (2/3)

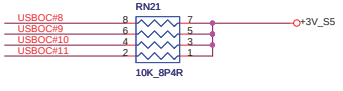
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R347 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_H R329 TPM@10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI 1 / 1 / LPC	GNT0# R344 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R340 *1K_4







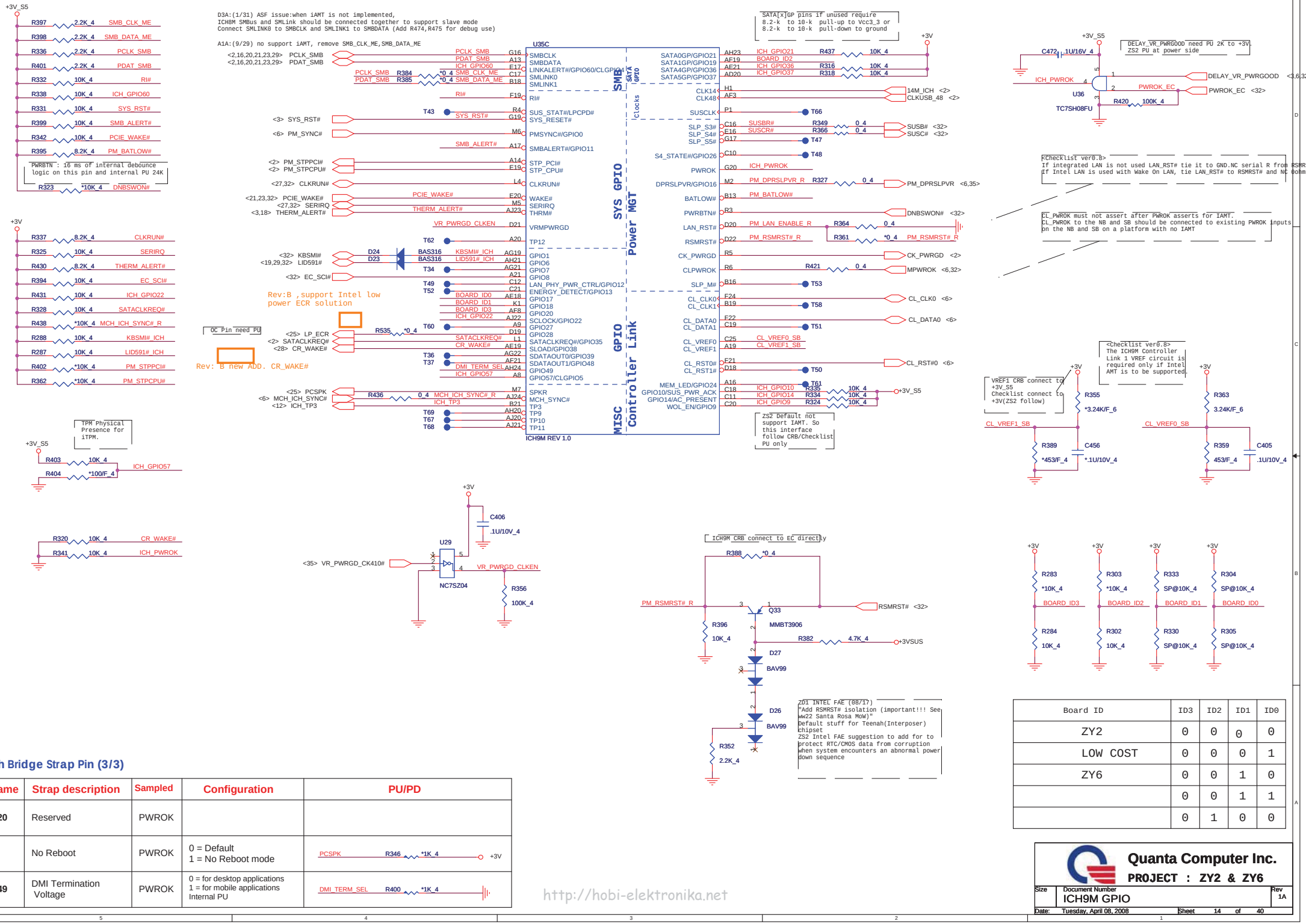




Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A

Date: Wednesday, April 09, 2008 Sheet 13 of 40



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R346 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R400 *1K_4

Board ID	ID3	ID2	ID1	ID0
ZY2	0	0	0	0
LOW COST	0	0	0	1
ZY6	0	0	1	0
	0	0	1	1
	0	1	0	0

Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size | Document Number: ICH9M GPIO | Rev: 1A
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Power consumption reference to Intel
642879 ICH9 Family EDS Rev 1.5

2~3.456v
3.6uA_G3

5V
2mA

5V
2mA_S0
1mA_S3/S4/S5

1.5V
646mA

1.5V
47mA

VCC1_5_A
1.5V
1342mA

1.5V
11mA

1.05V , Powered by VCC1_05 in S0

3.3V
19mA_S0 ,
78mA_S3/S4/S5

1.5V
23mA

1.5V
80mA

3.3V
1mA

1.05V
1634mA

1.5V
23mA

1.05V
50mA

VCCP
2mA

VCC3_3
3.3V
308mA

1.5V / 3.3V
11mA

1.5V / 3.3V
11mA_S0 , 1mA_S3/S4/S5

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

3.3V
212mA_S0 , 53mA_S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

3.3V
19mA_S0 , 73mA_S3/S4/S5

If use SB MAC for LAN function. And support wake up need connect to relation power.

ZS2 Default not support INT HDMI interface

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

U35F
ICH9M REV 1.0

U35E
ICH9M REV 1.0

http://hobi-elektronika.net

Quanta Computer Inc.	PROJECT : ZY2 & ZY6		
Size	Document Number: ICH9 POWER		Rev: 1A
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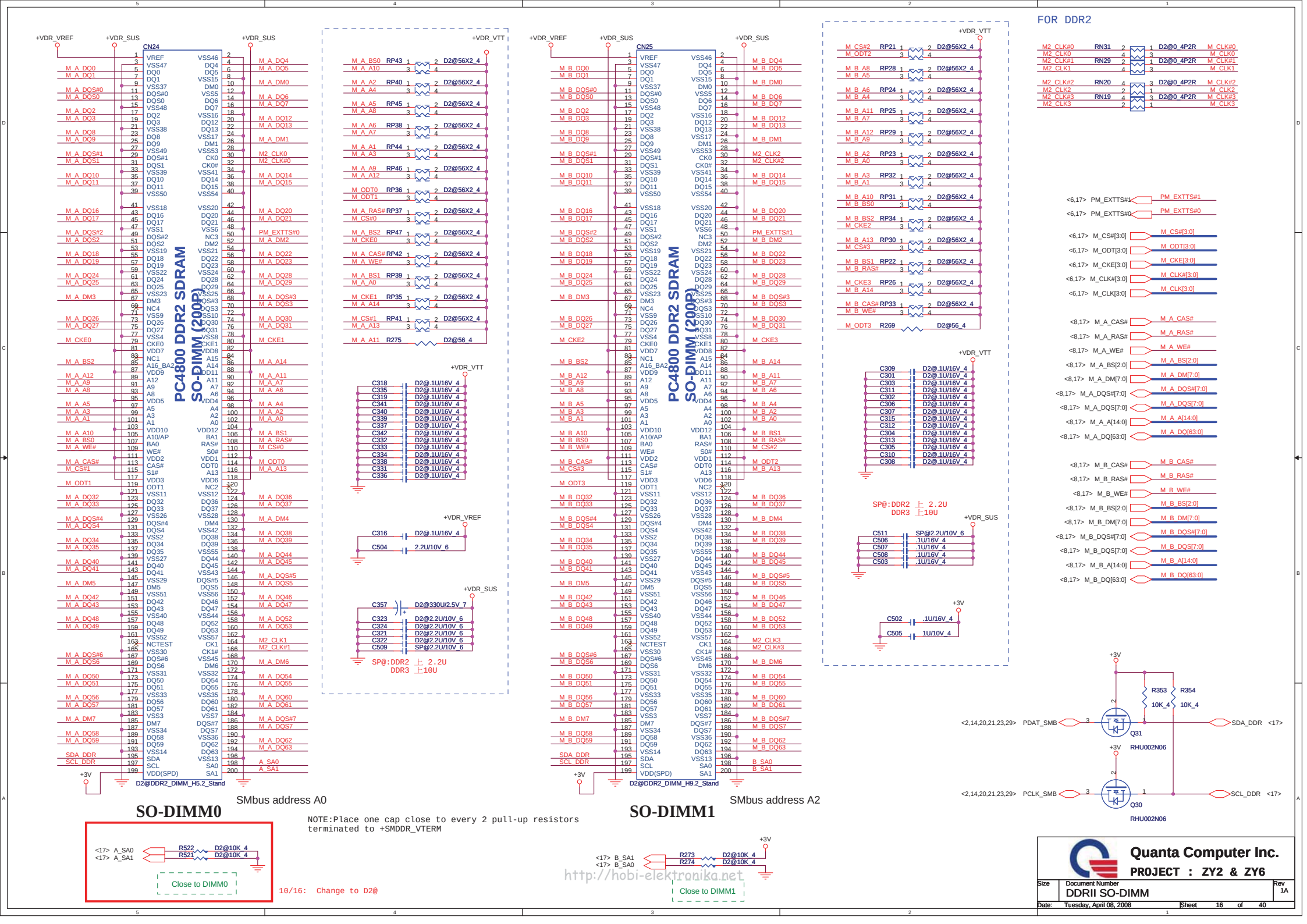
FOR DDR2
CN24
PC4800 DDR2 SDRAM SO-DIMM (200P)
D2@DDR2_DIMM_H5.2_Stand
SMbus address A0
SO-DIMM0
CN25
PC4800 DDR2 SDRAM SO-DIMM (200P)
D2@DDR2_DIMM_H9.2_Stand
SMbus address A2
SO-DIMM1
SP@:DDR2 2.2U
DDR3 10U
NOTE:Place one cap close to every 2 pull-up resistors terminated to +SMDDR_VTERM
Close to DIMM0
Close to DIMM1
10/16: Change to D2@
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
DDRII SO-DIMM
Size
Document Number
Rev 1A
Date: Tuesday, April 08, 2008
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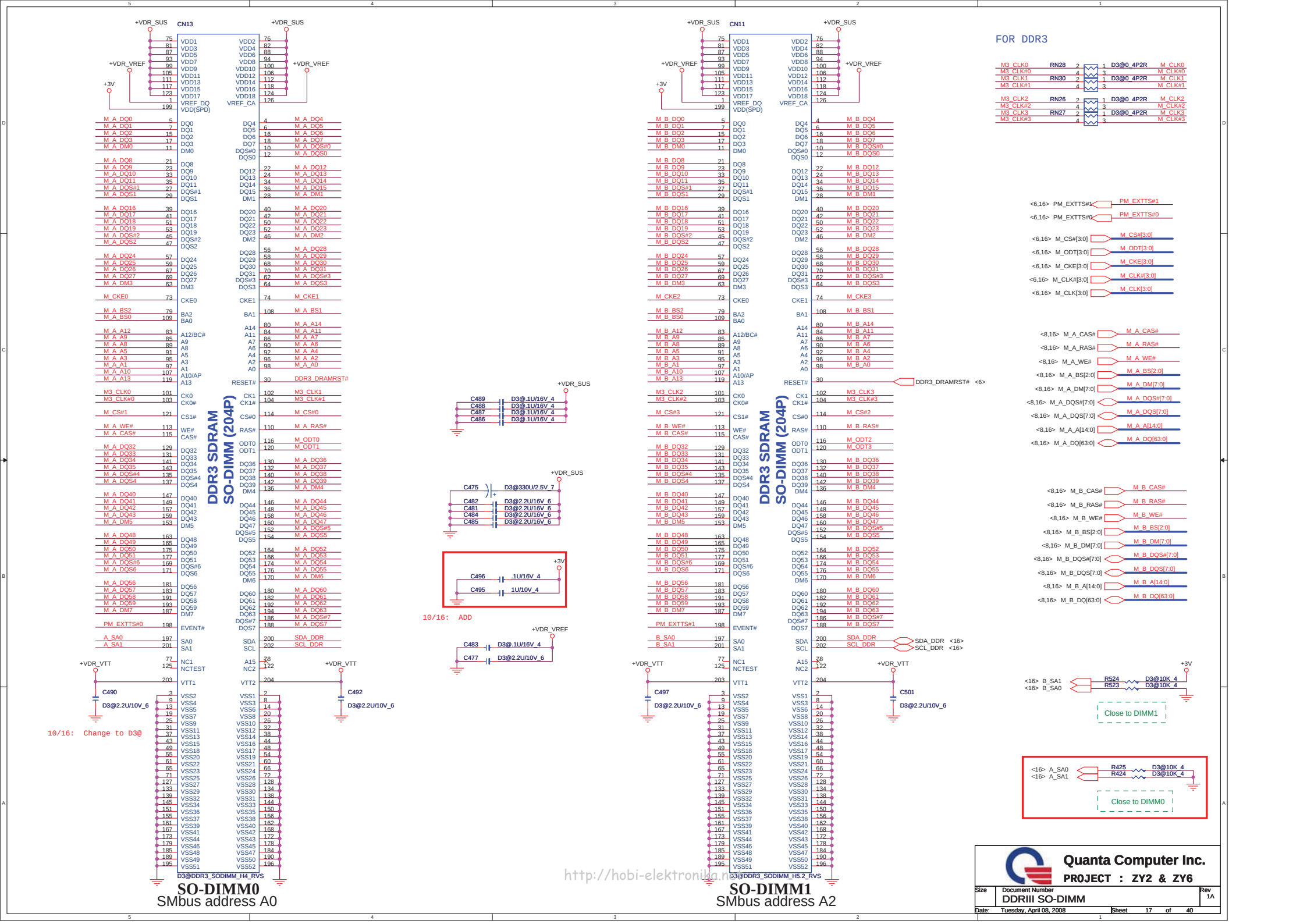
CN13
DDR3 SDRAM SO-DIMM (204P)
D3@DDR3_SODIMM_H4_RVS
SO-DIMM0
SMbus address A0
10/16: Change to D3@
10/16: ADD
CN11
DDR3 SDRAM SO-DIMM (204P)
D3@DDR3_SODIMM_H5.2_RVS
SO-DIMM1
SMbus address A2
FOR DDR3
Close to DIMM1
Close to DIMM0
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
DDRIII SO-DIMM
Tuesday, April 08, 2008
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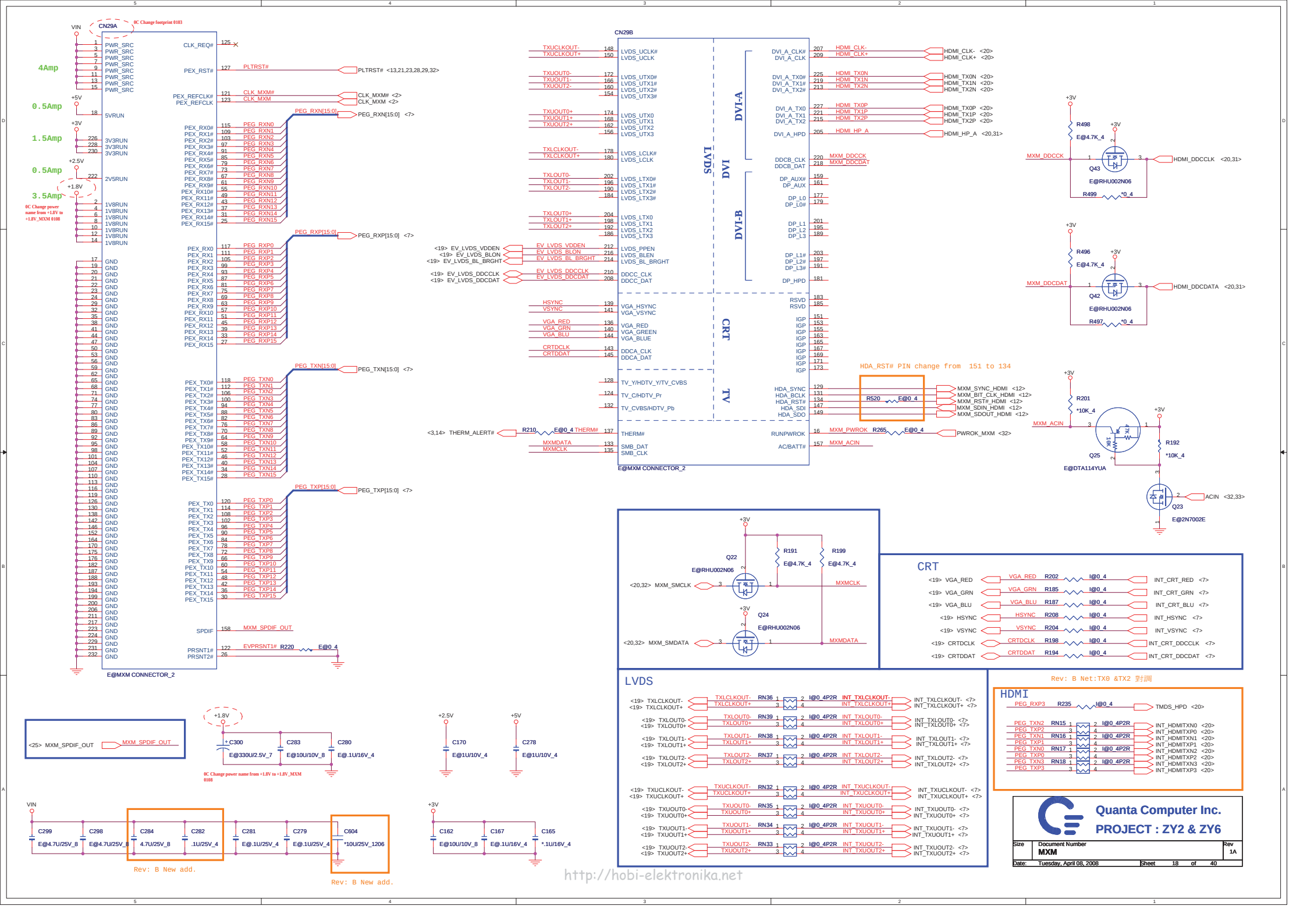
CN29A
0C Change footprint 0103
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
0C Change power name from +1.8V to +1.8V_MXM 0108
E@MXM CONNECTOR_2
CN29B
LVDS
DVI-A
DVI
DVI-B
CRT
TV
E@MXM CONNECTOR_2
HDA_RST# PIN change from 151 to 134
E@DTA114YUA
E@2N7002E
CRT
LVDS
HDMI
Rev: B Net:TX0 &TX2 對調
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Document Number
MXM
Rev
1A
Tuesday, April 08, 2008
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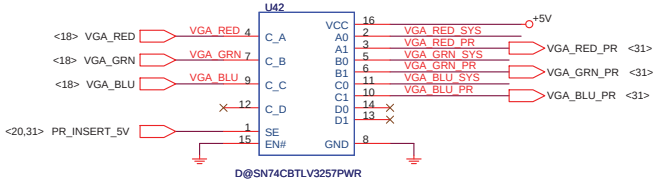
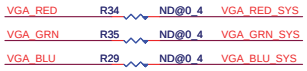
Rev: B New add.
Rev: B New add.
http://hobi-elektronika.net

CRT Select

CRT SWITCH

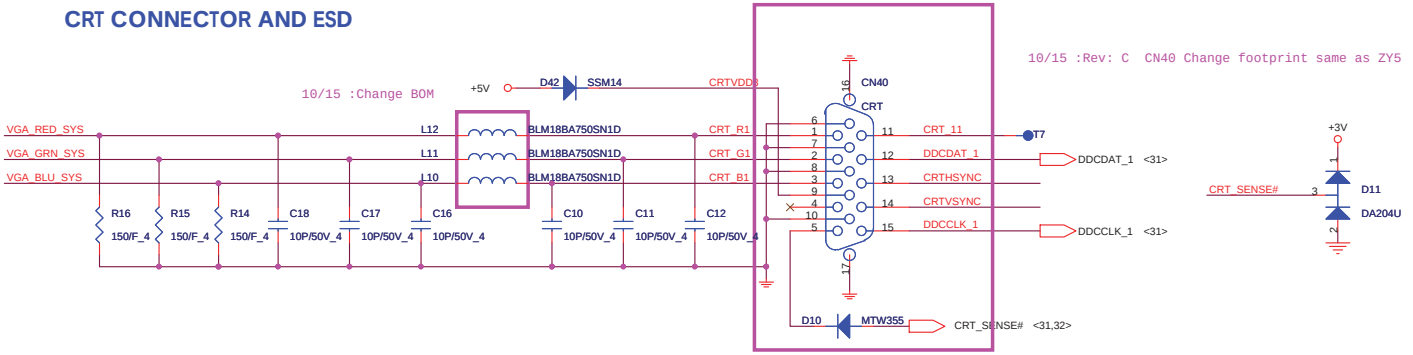


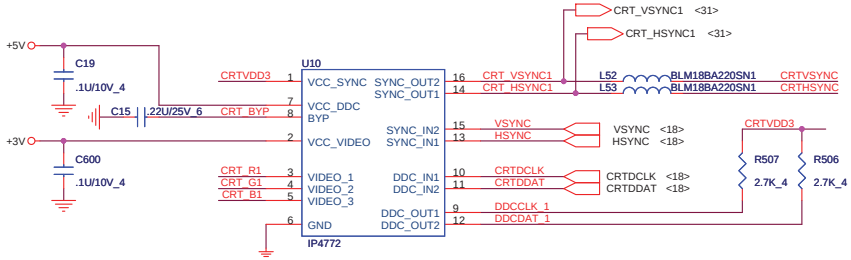


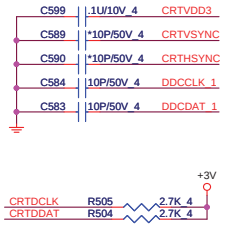
CRT CONNECTOR AND ESD

10/15 :Change BOM

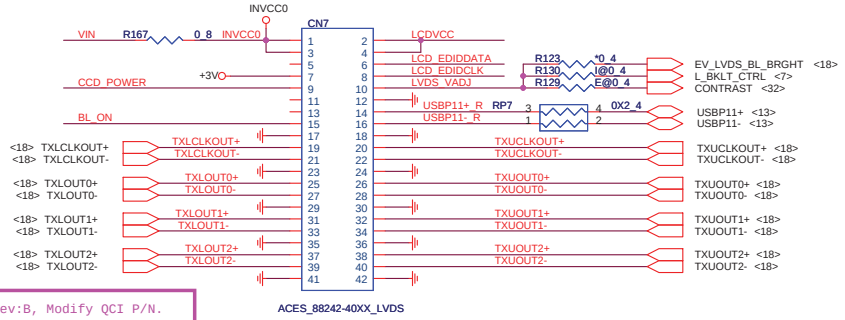
10/15 :Rev: C CN40 Change footprint same as ZY5

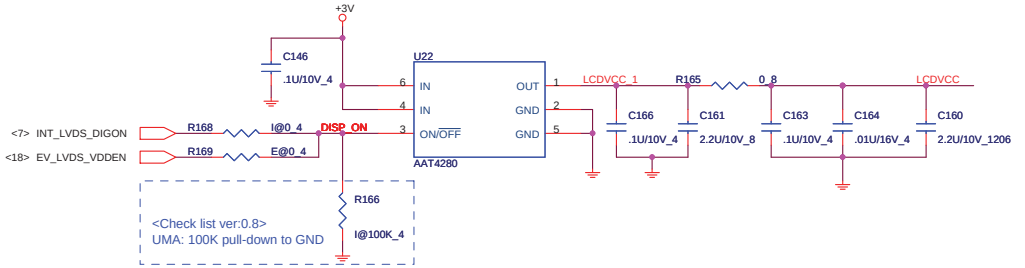




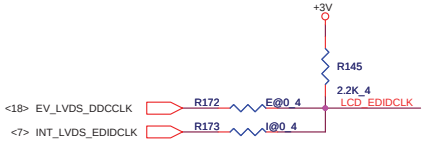


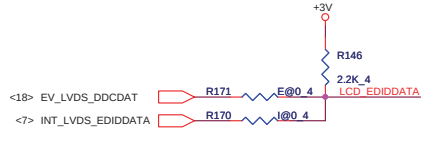
LVDS

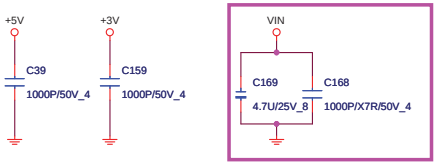




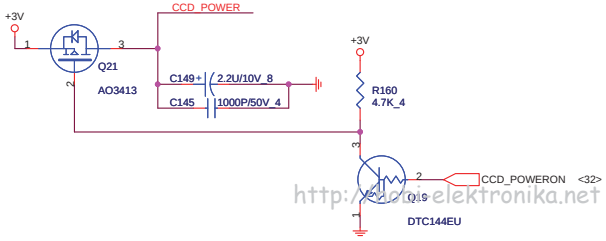
Rev:C, Change to 4.7U 0805



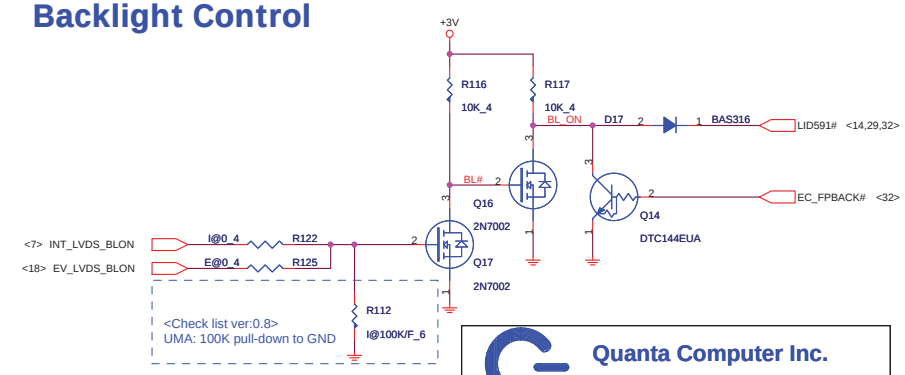




CAMERA MODULE CONNECTOR



Backlight Control



Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CRT	1A
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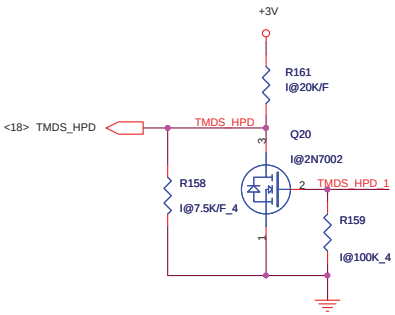
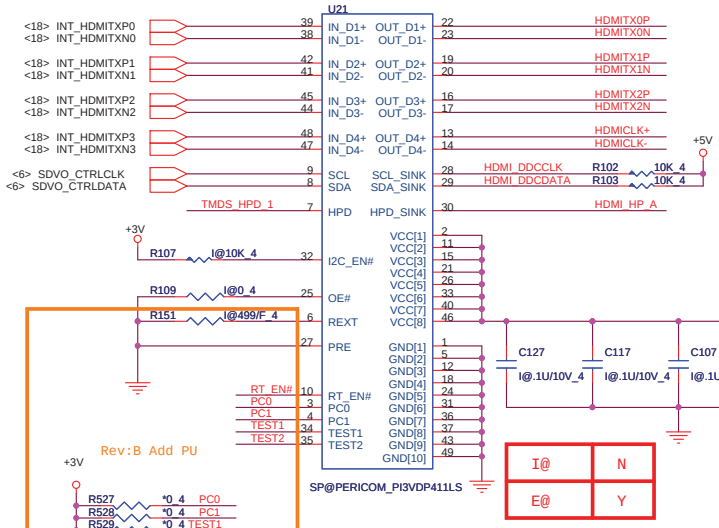
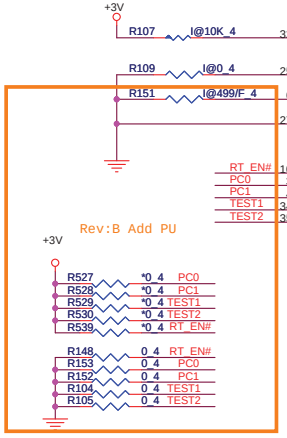
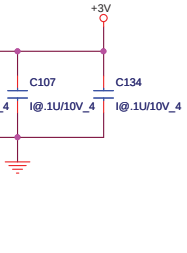
DVI-I CONNECTOR (DVI-D)

	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



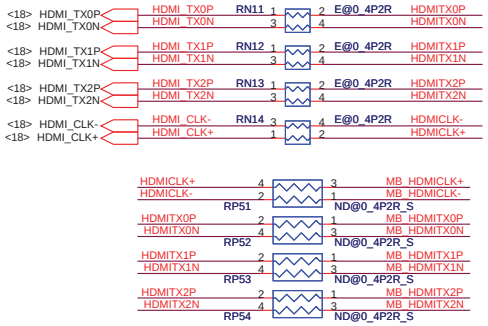




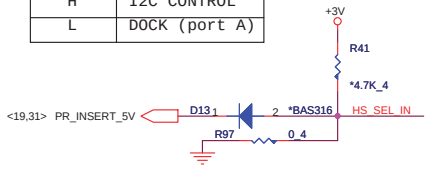


I@	N
E@	Y

LOW COST	N
TM & AS	Y

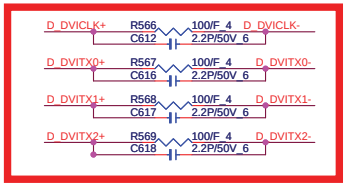


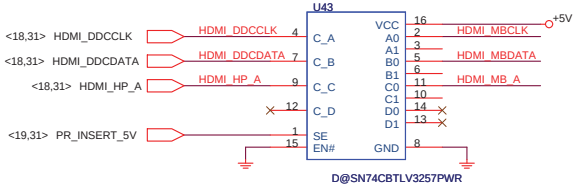
MS	FUN
H	I2C CONTROL
L	DOCK (port A)

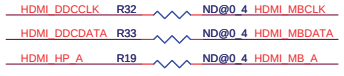


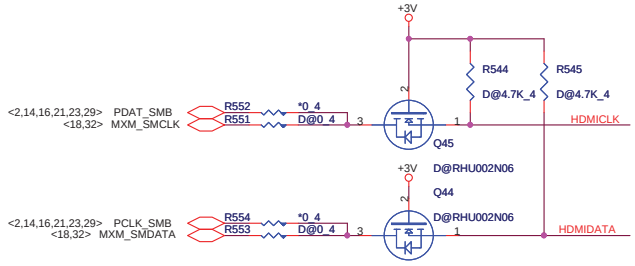
SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)

Rev:B ,change IC

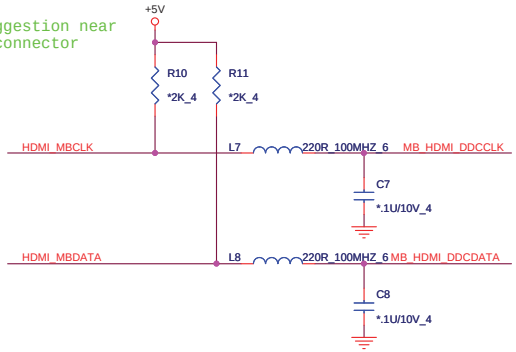


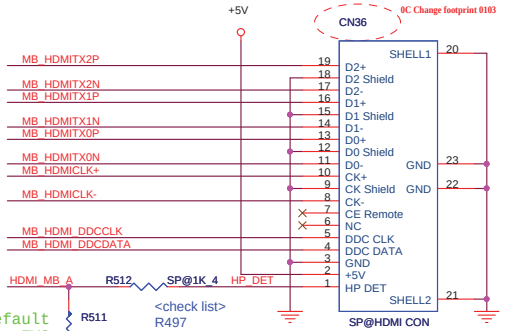






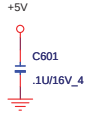
NV suggestion near
HDMI connector





HDMI monitor default
have PU to 5V.So ZY3
PD for level
change.And serial R
for current limited

<check list>
R497
For EV@
Connect to 1K
For IV@
Connect to 0ohm

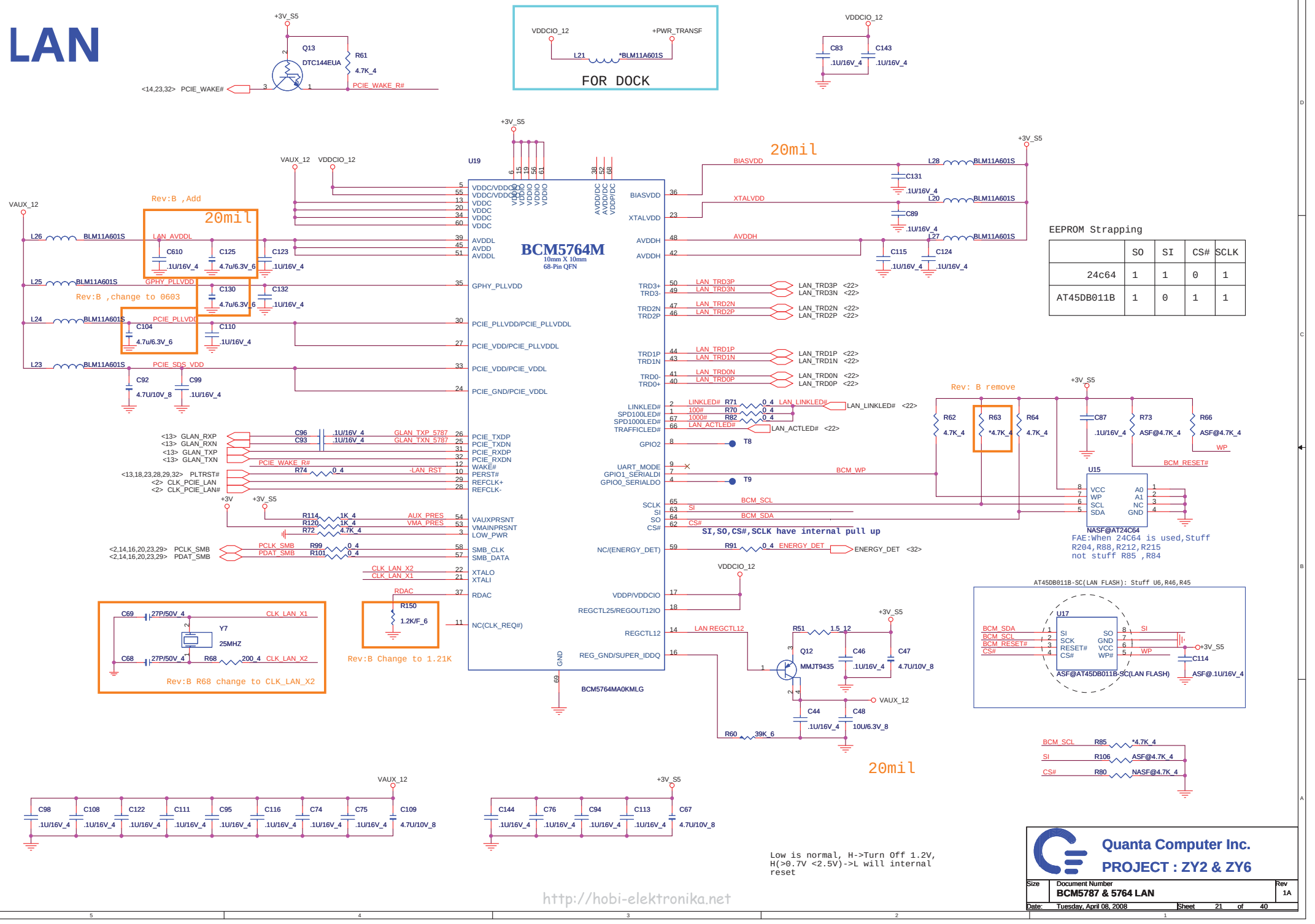


LOW COST	N
TM & AS	Y

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	LVDS/HDMI/CAMERA/LID	1A
Date: Wednesday, April 09, 2008	Sheet 20 of 40	

LAN


+3V_S5
Q13
DTC144EUA
R61
4.7K_4
<14,23,32> PCIE_WAKE#
PCIE_WAKE_R#
VDDCIO_12
+PWR_TRANSF
L21
*BLM11A601S
FOR DOCK
C83
C143
.1U/16V_4
U19
BCM5764M
10mm X 10mm
68-Pin QFN
BCM5764MA0KMLG
20mil
Rev:B ,Add
Rev:B ,change to 0603
VAUX_12
VDDCIO_12
L26 BLM11A601S
L25 BLM11A601S
L24 BLM11A601S
L23 BLM11A601S
LAN_AVDDL
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_SDS_VDD
C610
C125
C123
C130
C132
C104
C110
C92
C99
4.7u/6.3V_6
4.7U/10V_8
BIASVDD
XTALVDD
AVDDH
L28 BLM11A601S
L20 BLM11A601S
L27 BLM11A601S
C131
C89
C115
C124
LAN_TRD3P
LAN_TRD3N
LAN_TRD2N
LAN_TRD2P
LAN_TRD1P
LAN_TRD1N
LAN_TRD0N
LAN_TRD0P
LINKLED#
LAN_ACTLED#
GPIO2
T8
UART_MODE
GPIO1_SERIALDI
GPIO0_SERIALDO
T9
SCLK
SI
SO
CS#
BCM_SCL
BCM_SDA
BCM_WP
SI,SO,CS#,SCLK have internal pull up
NC/(ENERGY_DET)
R91
ENERGY_DET
Rev: B remove
R62
R63
*4.7K_4
R64
4.7K_4
C87
R73
ASF@4.7K_4
R66
ASF@4.7K_4
WP
BCM_RESET#
U15
NASF@AT24C64
FAE:When 24C64 is used,Stuff
R204,R88,R212,R215
not stuff R85 ,R84
EEPROM Strapping
SO SI CS# SCLK
24c64 1 1 0 1
AT45DB011B 1 0 1 1
AT45DB011B-SC(LAN FLASH): Stuff U6,R46,R45
U17
ASF@AT45DB011B-SC(LAN FLASH)
C114
ASF@.1U/16V_4
BCM_SDA R85 *4.7K_4
SI R106 ASF@4.7K_4
CS# R80 NASF@4.7K_4
<13> GLAN_RXP
<13> GLAN_RXN
<13> GLAN_TXP
<13> GLAN_TXN
GLAN_TXP_5787
GLAN_TXN_5787
PCIE_WAKE_R#
<13,18,23,28,29,32> PLTRST#
<2> CLK_PCIE_LAN
<2> CLK_PCIE_LAN#
-LAN_RST
R74
<2,14,16,20,23,29> PCLK_SMB
<2,14,16,20,23,29> PDAT_SMB
R99
R101
R114
R120
R72
AUX_PRES
VMA_PRES
CLK_LAN_X1
CLK_LAN_X2
RDAC
R150
1.2K/F_6
Rev:B Change to 1.21K
C69
C68
27P/50V_4
Y7
25MHZ
R68
200_4
Rev:B R68 change to CLK_LAN_X2
LAN REGCTL12
R51
1.5_12
Q12
MMJT9435
C46
C47
4.7U/10V_8
C44
C48
10U/6.3V_8
R60
39K_6
20mil
C98
C108
C122
C111
C95
C116
C74
C75
C109
C144
C76
C94
C113
C67
Low is normal, H->Turn Off 1.2V,
H(>0.7V <2.5V)->L will internal
reset
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
Size
Document Number
BCM5787 & 5764 LAN
Rev
1A
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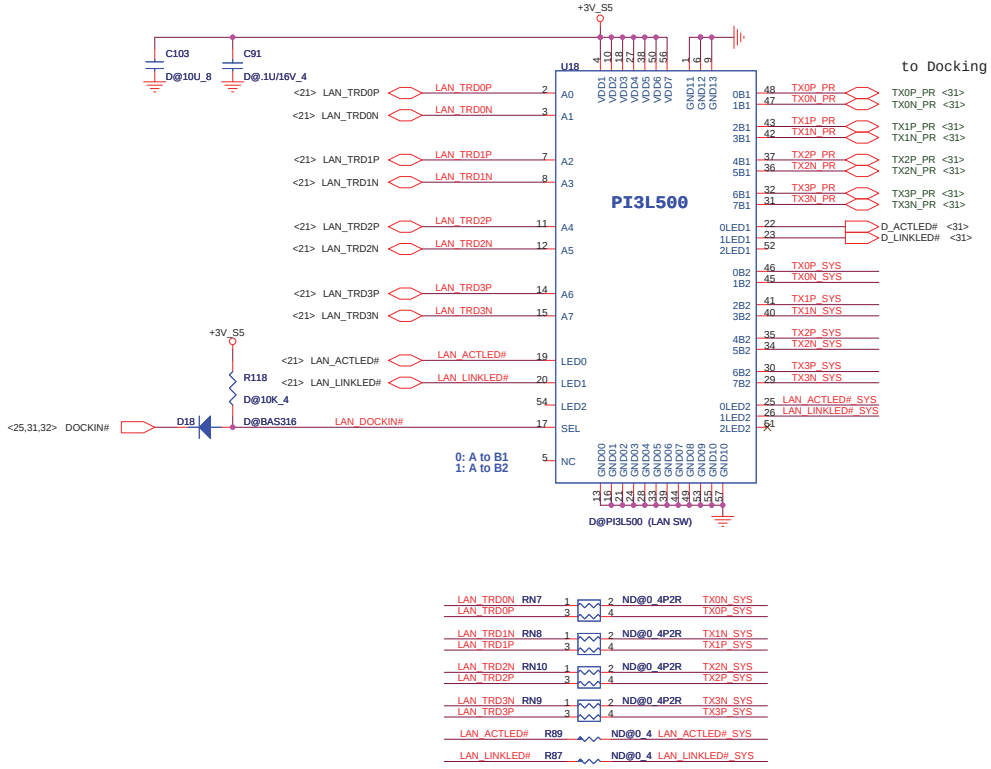
Sheet 21 of 40

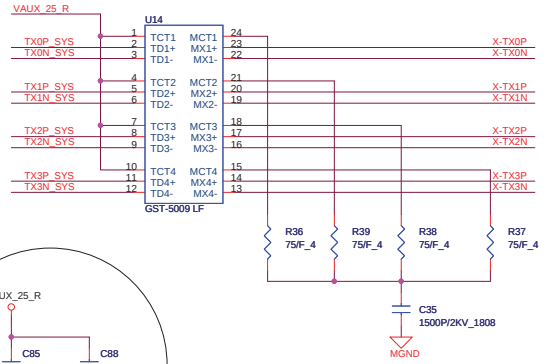
LAN SWITCH

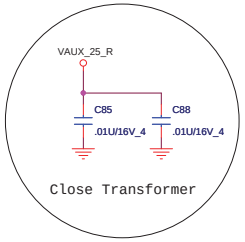


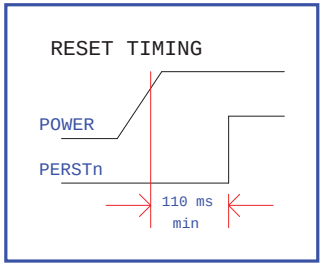
Transfomer

Source 1: DELTA LFE9249 DB0ZR1LAN11

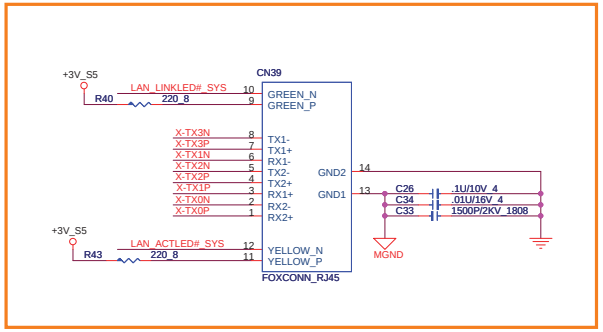
Source 2: Bothand GST5009 DBKN1NLAN03





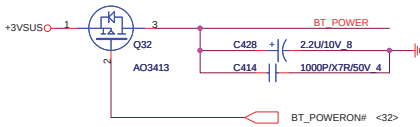


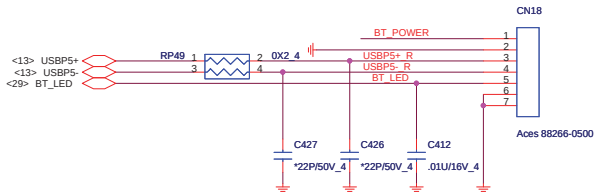
RJ45-11



9/29: change footprint
11/27 :change footprint
11/28 : R43 & R40 Change to 0805
1/31 :Rev: C change PIN define about 9,10,11 & 12

BLUETOOTH MODULE CONNECTOR





Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	1A
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MINI-CARD

MODULE 'A' TV card

MODULE 'B' Wireless card

Double Stack MINI CARD

Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538

MODULE 'A' MODULE 'B'

CN27

+3V R542 0_8 +3V_MINI_A

+3V_MINI_B R543 0_8 +3V

RF_LED# R536 *0_4 RF_LED# A

RF_LED# A_LED_WPAN# A_LED_WLAN# A_LED_WWAN#

B_LED_WPAN# B_LED_WLAN# B_LED_WWAN#

RF_LED# B R447 0_4 RF_LED# RF_LED# <29>

<13> USBP2+ <13> USBP2- USBP2+ RP27 USBP2- 0X2_4 USBP2+_C USBP2-_C

USBP3+_C RP57 USBP3-_C 0X2_4 USBP3+ USBP3- USBP3+ <13> USBP3- <13>

MINI_SMDATA MINI_SMCLK A_SMB_DATA A_SMB_CLK

B_SMB_DATA B_SMB_CLK MINI_SMDATA MINI_SMCLK

<13> PCIE_TXP2 <13> PCIE_TXN2 <13> PCIE_RXP2 <13> PCIE_RXN2

PCIE_TXP2 PCIE_TXN2 PCIE_RXP2 PCIE_RXN2 PLTRST# A_PERST#

B_PETp0 B_PETn0 B_PERp0 B_PERn0 B_PERST#

PCIE_TXP4 <13> PCIE_TXN4 <13> PCIE_RXP4 <13> PCIE_RXN4 <13> PLTRST# <13,18,21,28,29,32>

<2> CLK_PCIE_TV <2> CLK_PCIE_TV#

CLK_PCIE_TV CLK_PCIE_TV# A_REFCLK+ A_REFCLK- A_CLKREQ#

B_REFCLK+ B_REFCLK- B_CLKREQ#

CLK_PCIE_MINI1 <2> CLK_PCIE_MINI1# <2>

PCIE_WAKE# R R538 *0_4 PCIE_WAKE# R_A A_WAKE#

B_WAKE# PCIE_WAKE# R_B R537 *0_4 PCIE_WAKE# R

+1.5V A_+1.5V A_+1.5V A_+1.5V

+1.5V B_+1.5V B_+1.5V B_+1.5V

<12,32> LFRAME# R445 0_4 A_LFRAME# R

<12,32> LAD3 R444 0_4 A_LAD3_R

<12,32> LAD2 R443 0_4 A_LAD2_R

<12,32> LAD1 R442 0_4 A_LAD1_R

<12,32> LAD0 R441 0_4 A_LAD0_R

B_LFRAME# R R561 0_4 LFRAME#

B_LAD3_R R559 0_4 LAD3

B_LAD2_R R558 0_4 LAD2

B_LAD1_R R560 0_4 LAD1

B_LAD0_R R562 0_4 LAD0

Debug

<13,27> PCIRST# R450 *0_4

<2> PCLK_DEBUG R448 *0_4

C-Link_RST C-Link_DAT C-Link_CLK

+3V R446 SP@0_6 +3V_MINI_R

TV use +3V C510 .1U/16V_4

RF_EN R557 *0_4 A_RF_EN A_W_DISABLE#

B_W_DISABLE# B_RF_EN R556 0_4 RF_EN <32>

+5V L41 SP@FBJ3216HS800_12 +5V_TV-CARD A_BT_CHCLK A_BT_DATA

B_BT_CHCLK B_BT_DATA

C494 4.7U/6.3V_6 C493 .1U/16V_4

500mA, 25mil

GND

A/B MODULE Share pin

SP@QUASAR-CA0404-071N21_92P

FOR R446 & L41	
LOW COST	N
TM & AS	Y

LC@ LOW COST 要打

+3V_S5 for WWAN card is 2.75A

+3V C513 4.7U/6.3V_6 C499 4.7U/6.3V_6 C491 .1U/16V_4 C498 .1U/16V_4

+1.5V C512 .1U/16V_4 C317 .1U/16V_4 C500 10U/6.3V_6

<2,14,16,20,21,29> PCLK_SMB +3V R449 10K_4 Q35 2N7002 MINI_SMCLK

<2,14,16,20,21,29> PDAT_SMB +3V R451 10K_4 Q36 2N7002 MINI_SMDATA

<14,21,32> PIE_WAKE# +3VSUS Q34 *DTC144EUA PCIE_WAKE# R

FOR EMI

+5V C605 1U/10V_4

VCC_CORE C70 1U/10V_4

VIN C150 1U/25V_6 +3V_S5

+3V C613 .1U/16V_4

+1.05V C614 .1U/16V_4

INVCC0 C607 1U/25V_6

+VDR_SUS C273 1U/10V_4

+VDR_SUS C394 1U/10V_4

+1.8V C615 .1U/16V_4

Quanta Computer Inc.

PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	MINI PCI-E card/TV/TPM	1A
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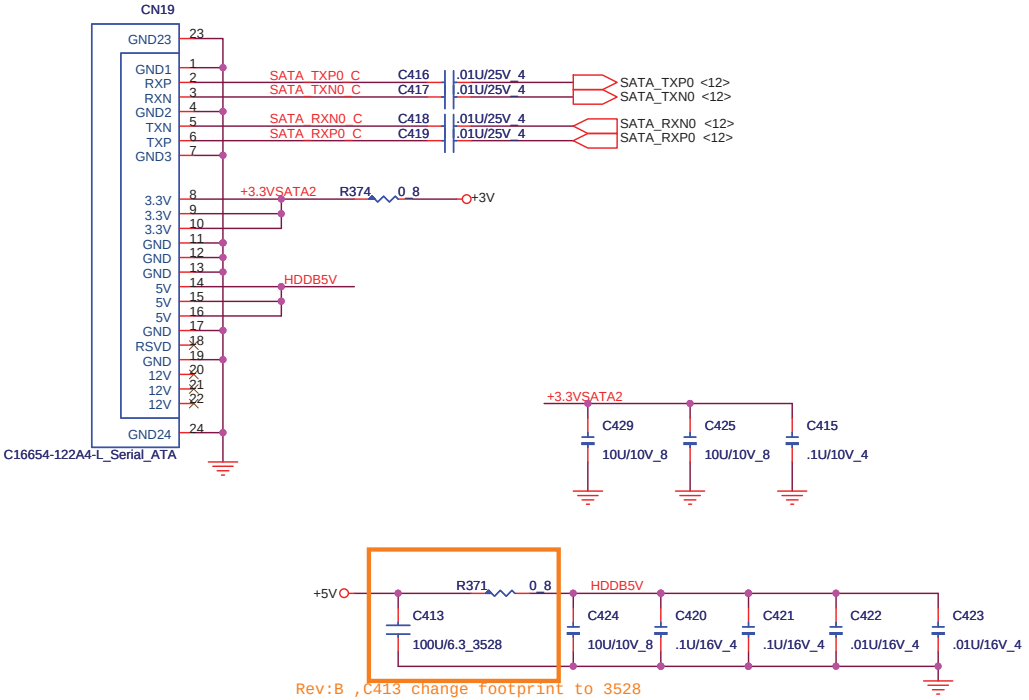
SATA HDD

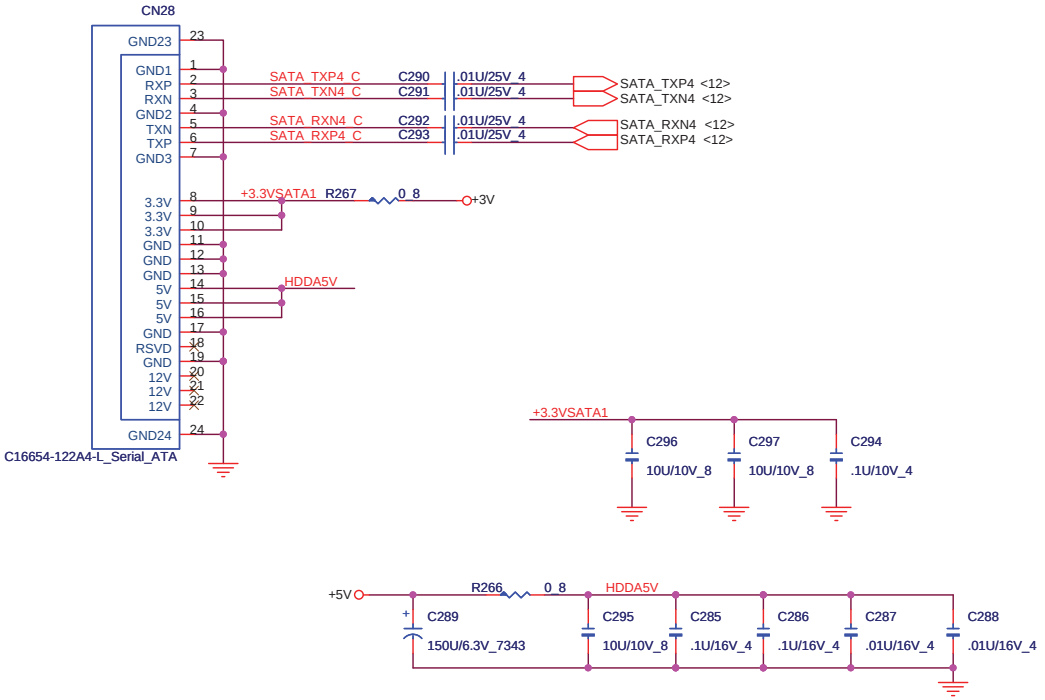
11/8 REV:B Conn. 掉對調 CN28 & CN19

Main

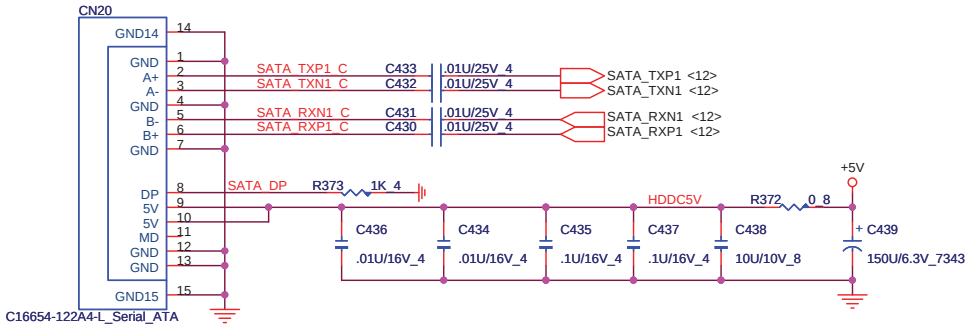


Rev:B ,C413 change footprint to 3528

2ND SATA HDD



ODD (SATA)

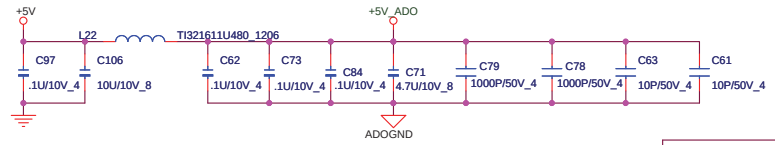


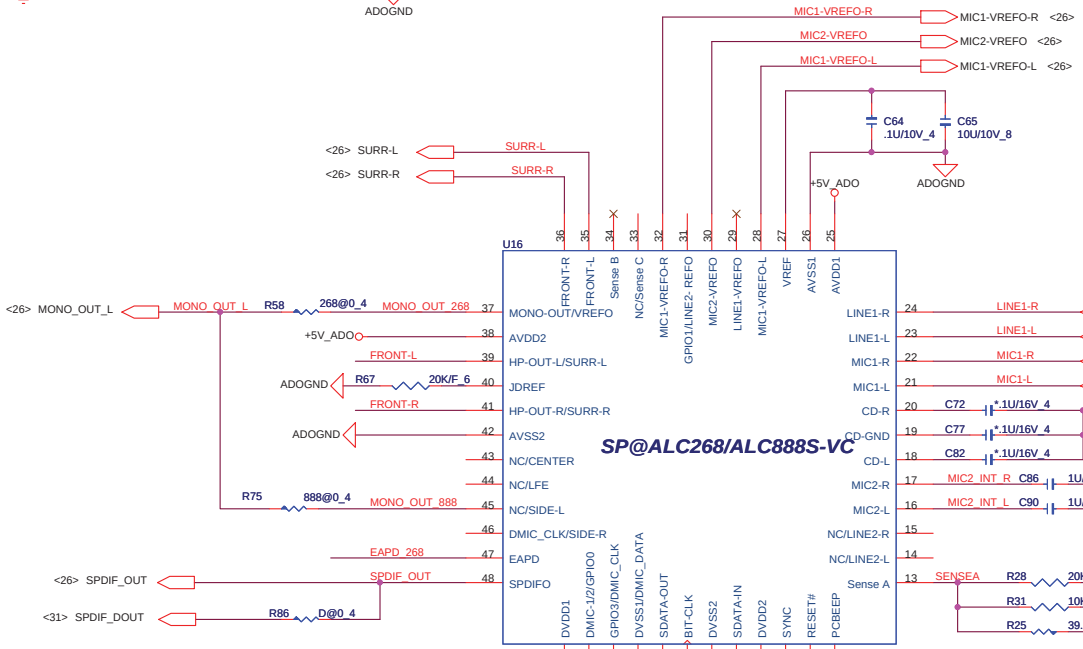
Quanta Computer Inc.

PROJECT : ZY2 & ZY6

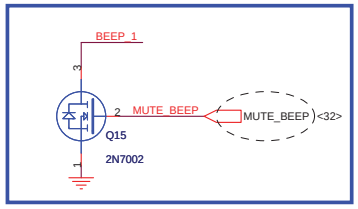
Size	Document Number	Rev
	SATA-HDD & ODD	1A
Date: Tuesday, April 08, 2008	Sheet 24 of 40	

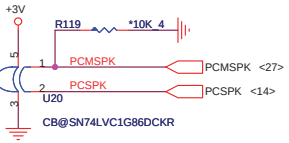
CODEC(ALC268)

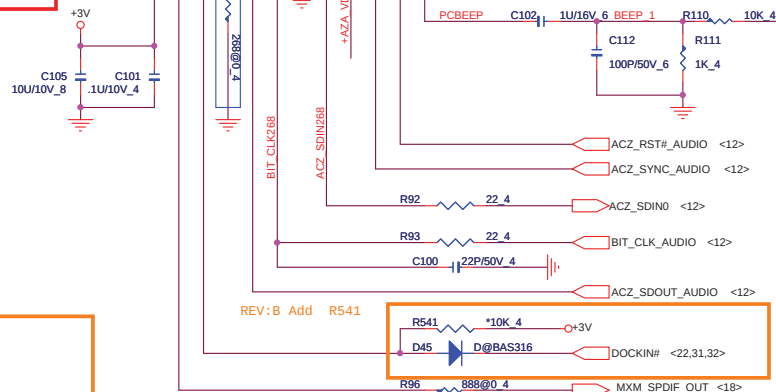




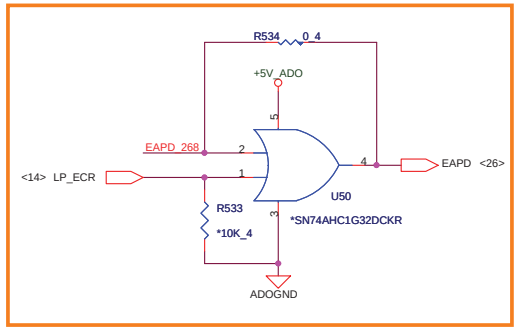
11/8 REV:B Remove R97, R98



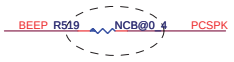




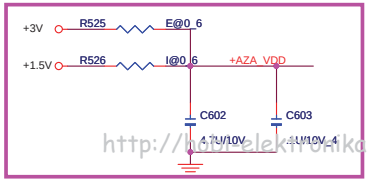
REV:B Add R541



10/10 : ADD. FOR NO CARDBUS

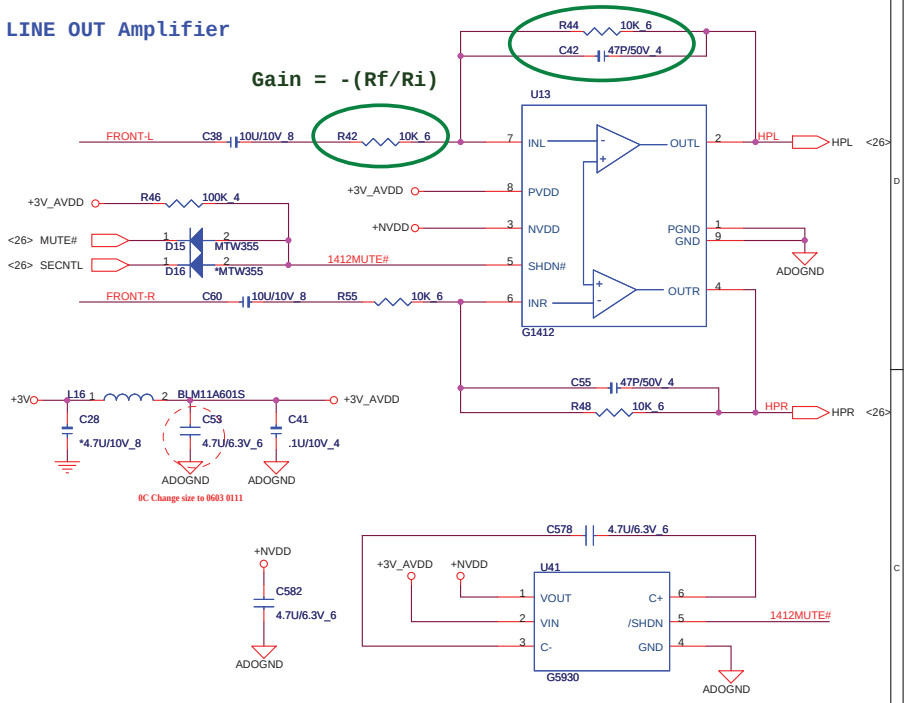


REV:B, Please modify U16.PIN9.same as ZD1



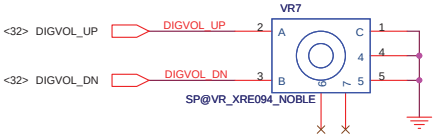
LINE OUT Amplifier

Gain = -(Rf/Ri)

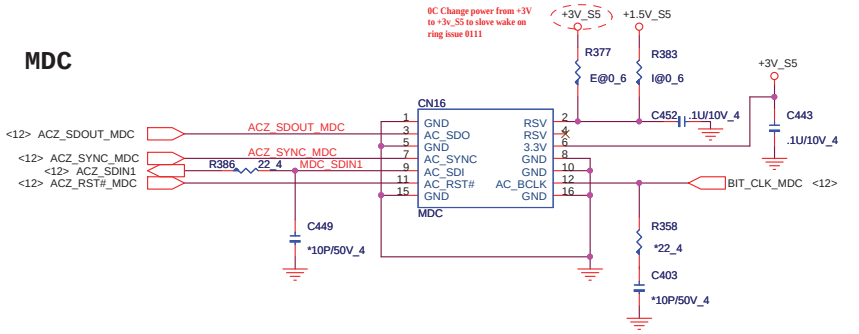


VR

TM	N
AS & LOW COST	Y



MDC



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	REALTEK ALC268&888/MDC/VR	1A
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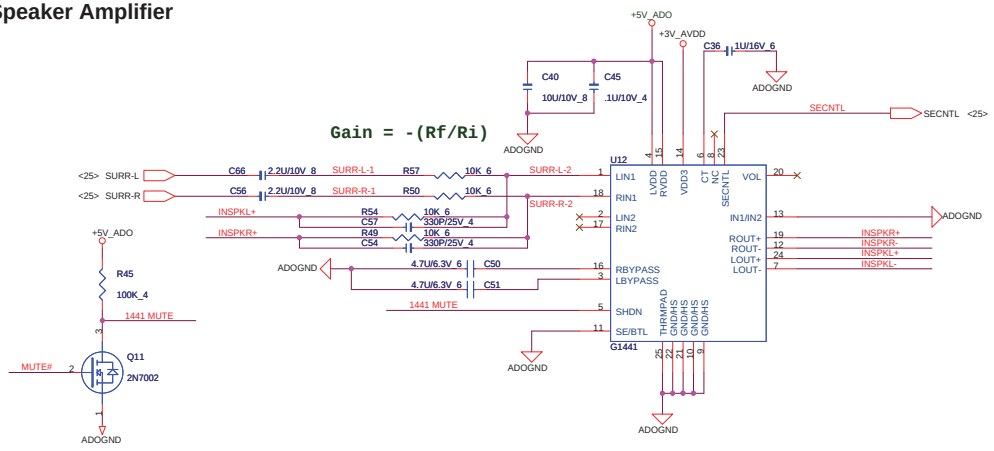
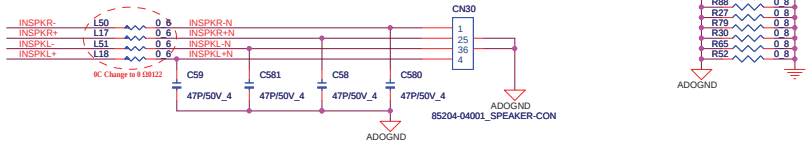
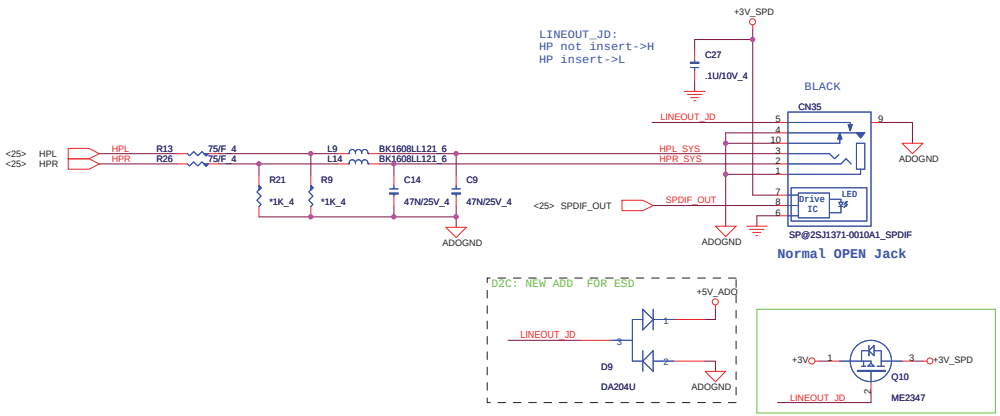
Speaker Amplifier

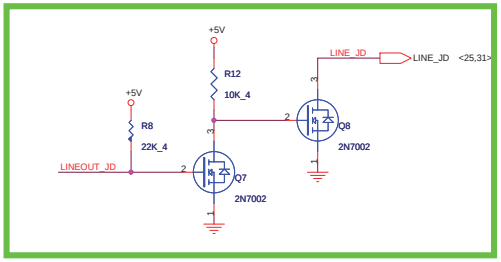


SPEAKER



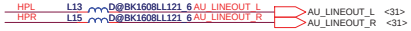
SYSTEM LINE OUT/SPDIF



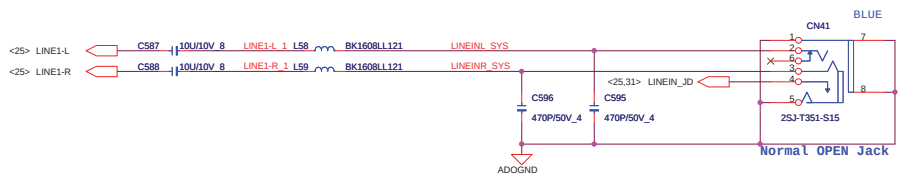


Foxconn DFTJ10FR470 2FB5441-BKMC-7F
Singatron DFTJ10FR437 2SJ1371-0010A1

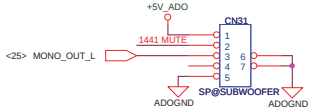
Docking LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER

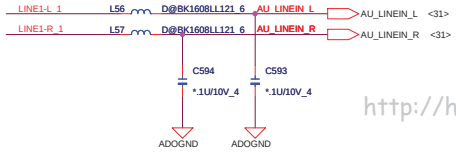


Singatron DFTJ06FR732 2SJ-T351-S15
Foxconn DFTJ06FRA21 JA6233L-U3T4-7F
Alltop DFTJ06FR902 C12107-906A9-L

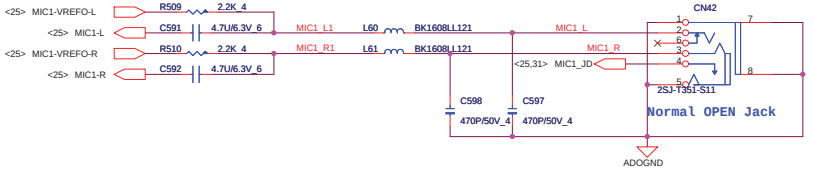


TM & LOW COST	N
AS	Y

Docking LINE IN

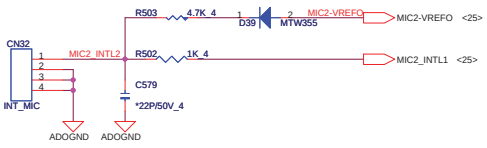


MIC



Singatron DFTJ06FR741 2SJ-T351-S11
Foxconn DFTJ06FRA39 JA6233L-P3T4-7F
Alltop DFTJ06FR899 C12107-D06A9-L

INT MIC array



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

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	AMP /AUDIO JACK CONN	1A
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IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS
FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY
CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST
BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R239 CB@100/F_4 PCM_IDSEL

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

O2MICRO OZ2210 8PIN
SINGLE SLOT PARALLEL
POWER SWITCH

PCMCIA SOCKET

CN9

CB@PCMCIA_SOCKET

PCMCIA SOCKET

CN44

*CB@PCMCIA_SOCKET

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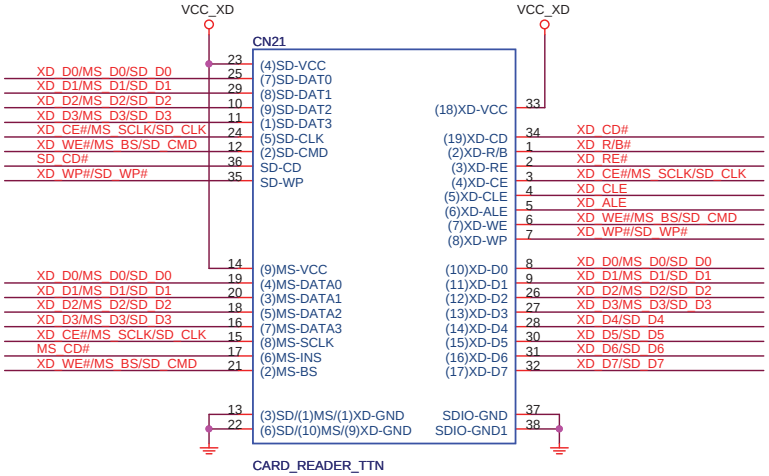
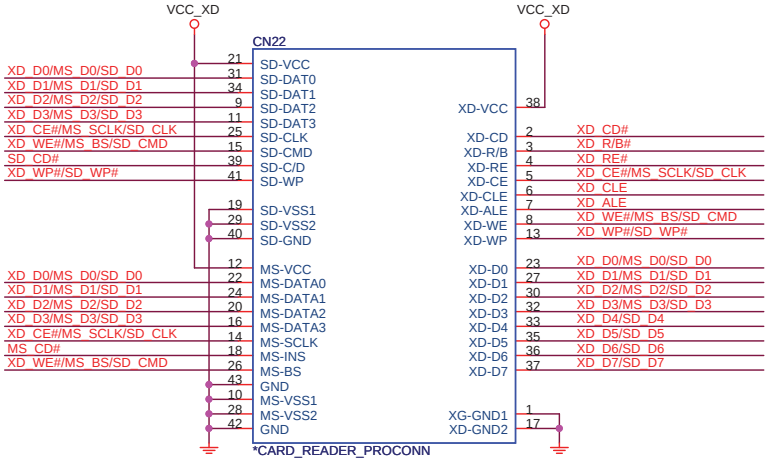
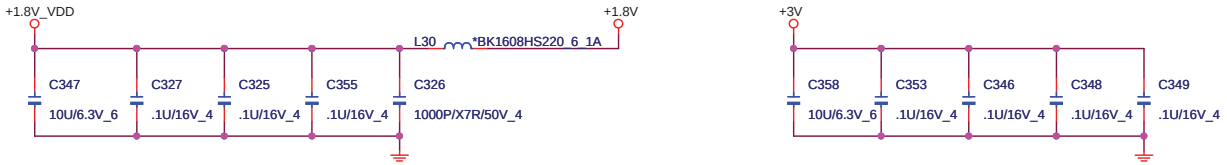
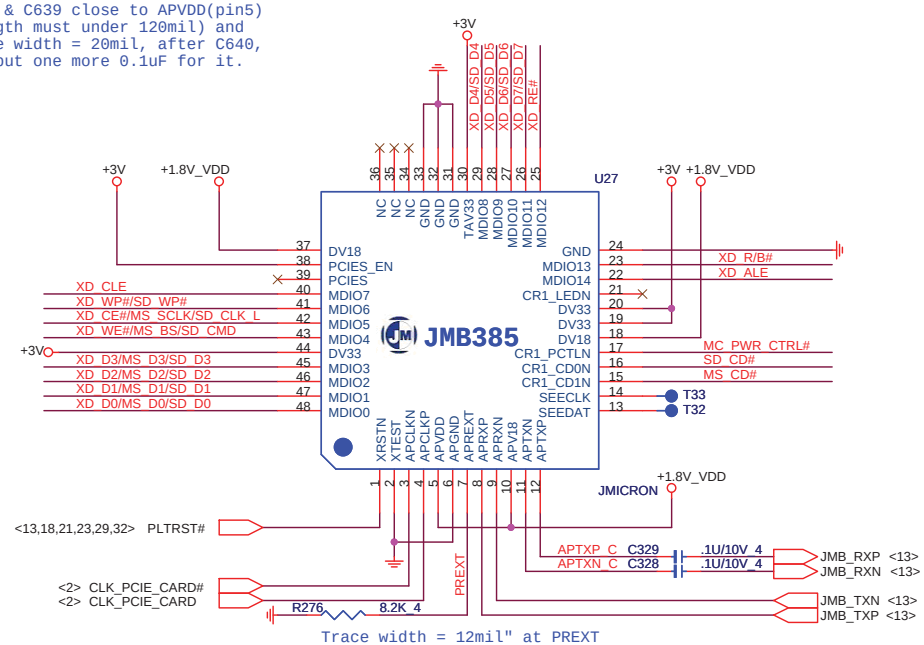
7 IN 1 CARD READER





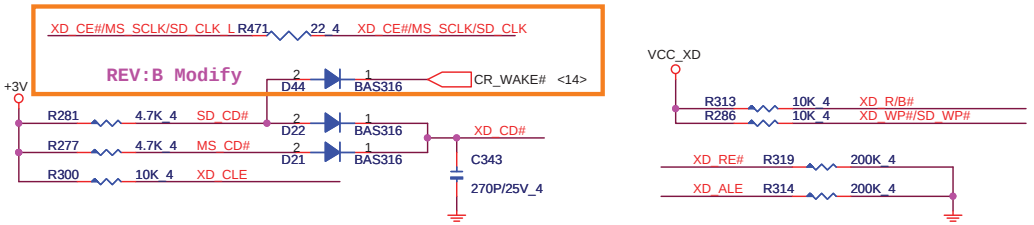


C640 & C639 close to APVDD(pin5)
(length must under 120mil) and
trace width = 20mil, after C640,
pls put one more 0.1uF for it.



Trace width = 12mil" at PREXT

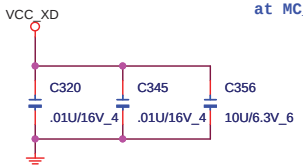
Rev: B Add. for Vendor request

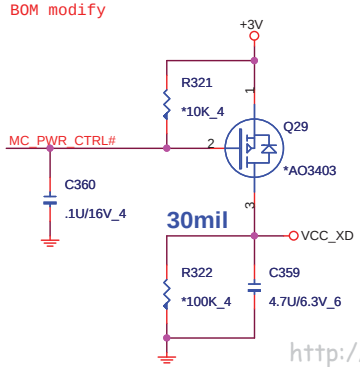


Memory Card Power Supply

10/12 : BOM modify

Use 0805 type and
Trace width = 30 mil"
at MC_PWR_CTRL#,





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	CARD READER JMB385	1A
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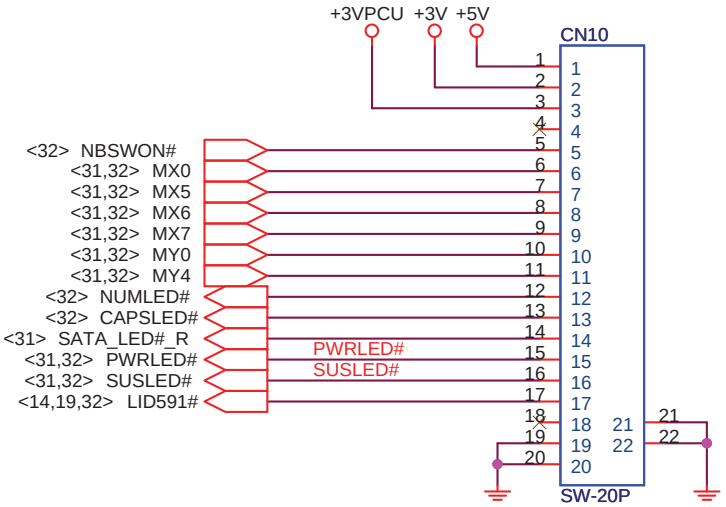
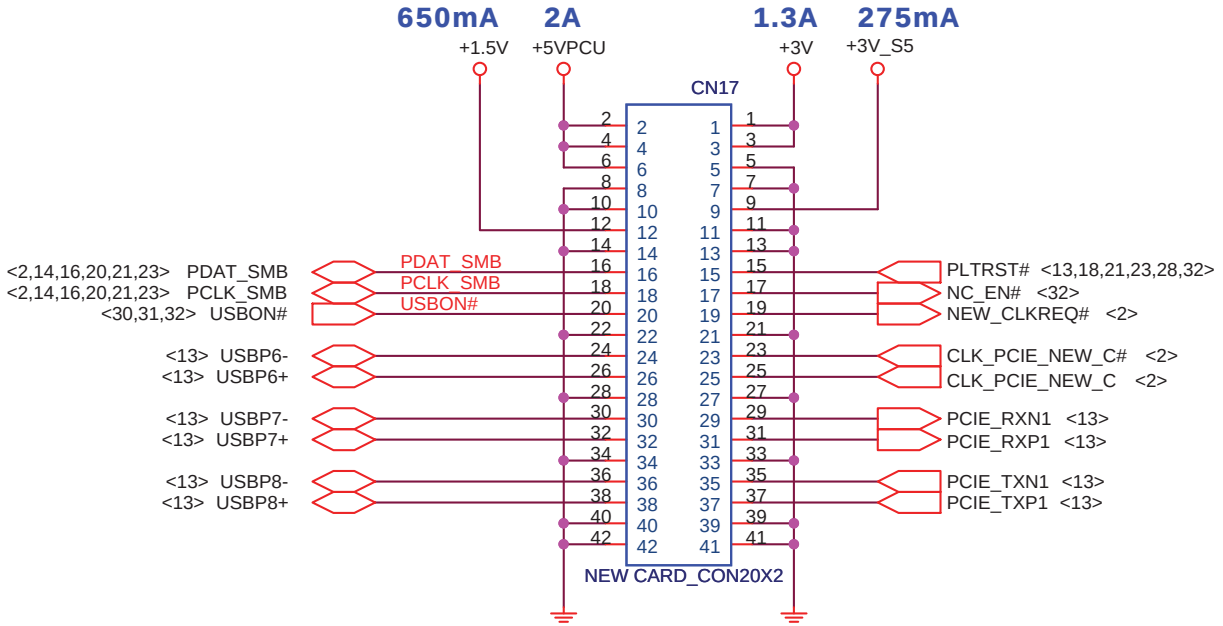
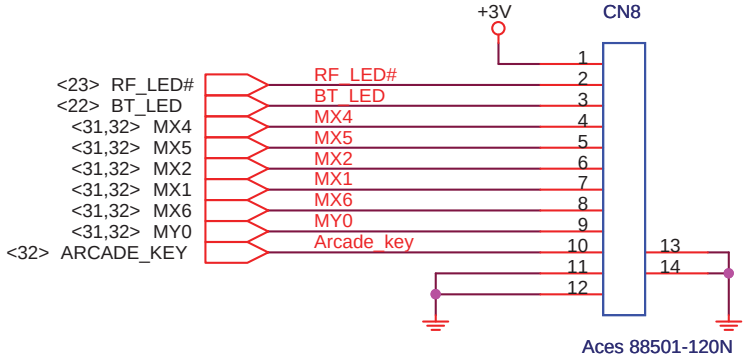
To NEW-CARD & EXT. USB

REV:B, CN10 change footprint

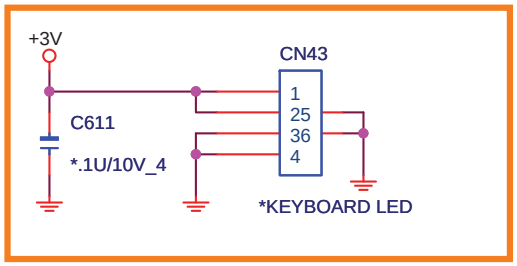




REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Fnction	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4



Rev:B Add CN43 For backlight KB

Rev:B Change to 圓 to 方PAD
C255,C234,C221,C199,R217,C198,R183,
R182,R174,R257,R324,R335,R334,R349,C395

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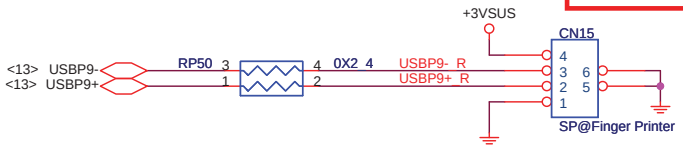
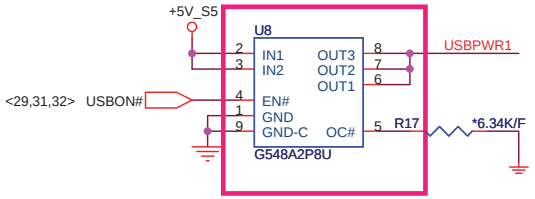
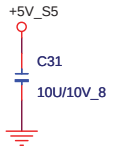
Finger Printer

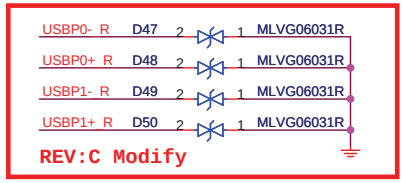
TM & AS	Y
LOW COST	N



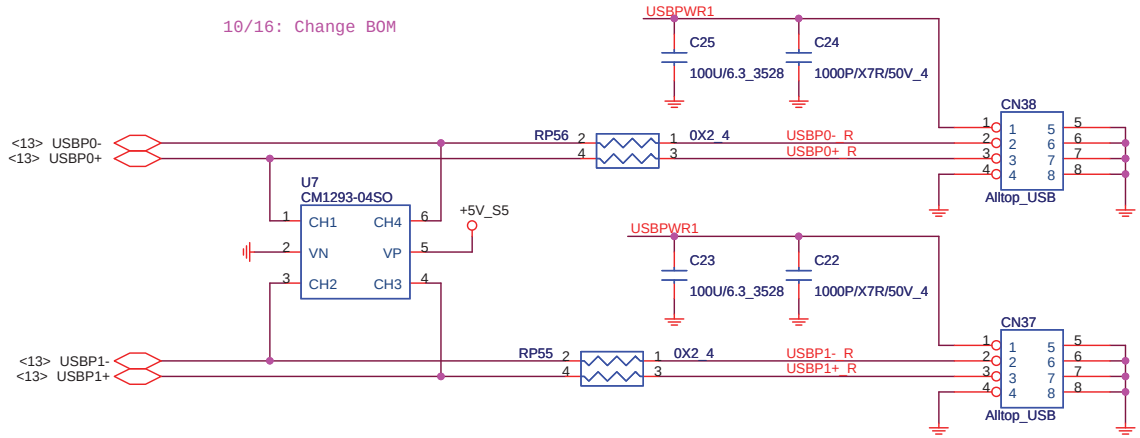
USB





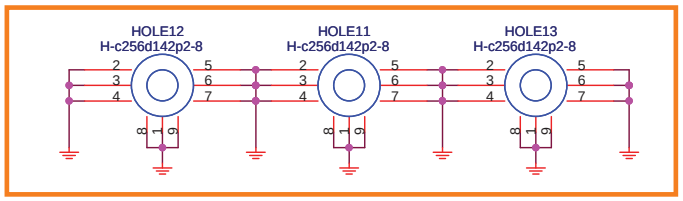


10/16: Change BOM

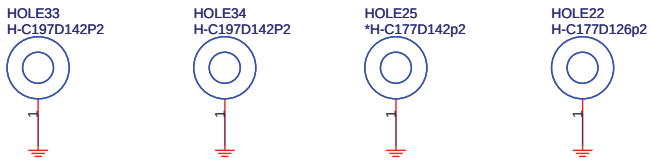


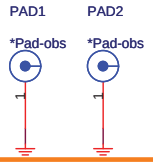
HOLES

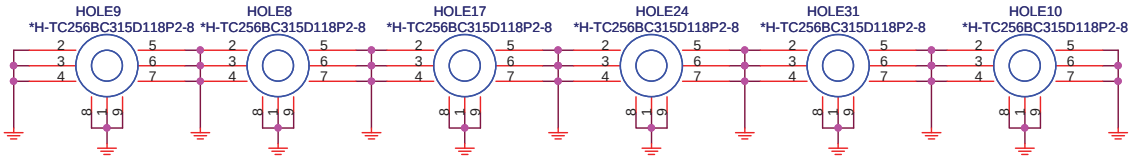
CPU NUT (BOT)



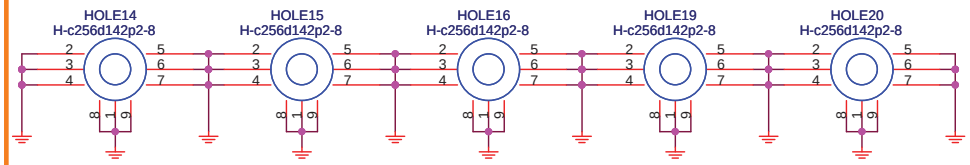
Rev : B Add MINI NUT

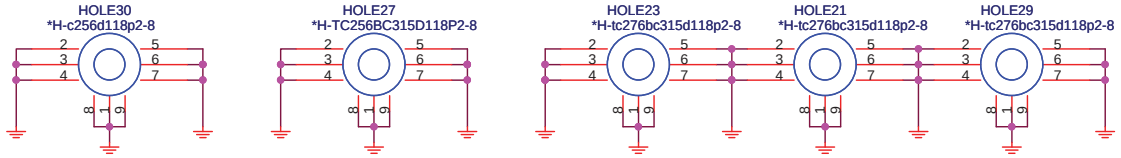




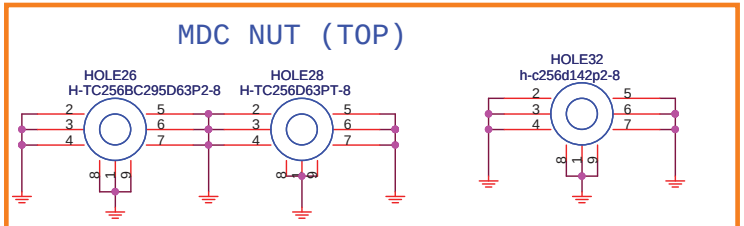


MXM NUT (BOT)

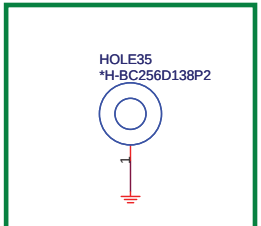




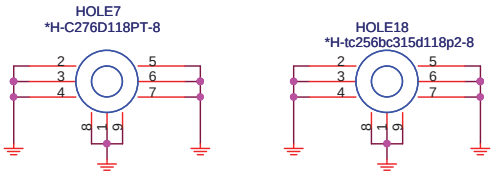
MDC NUT (TOP)



Rev:B New add HOLE32
HOLE26 & 28 Change footprint



HOLE35 要搬到BOT去



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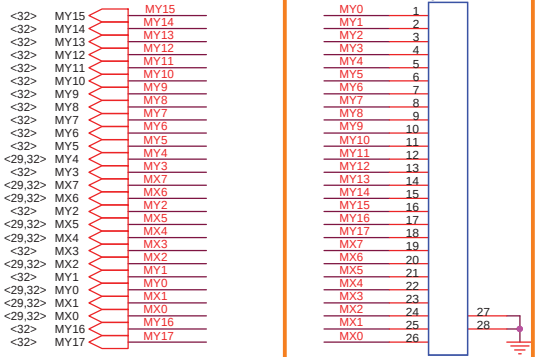
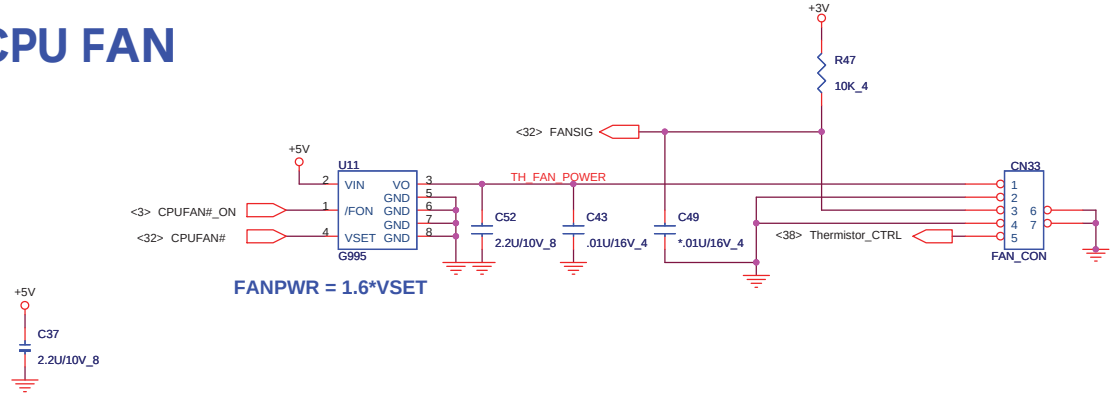
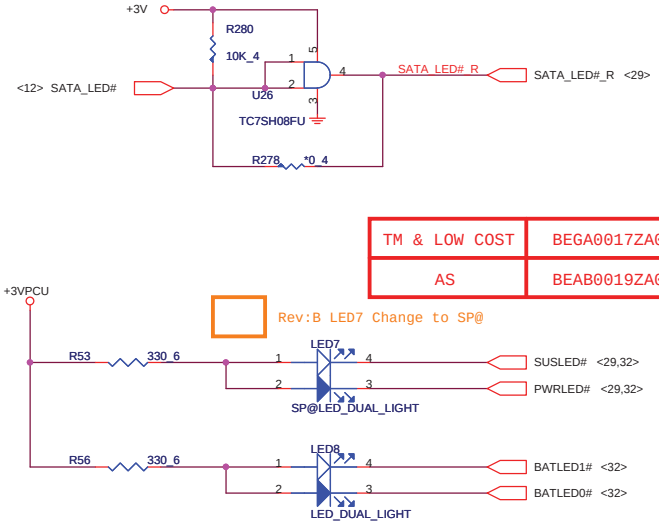
INT K/B



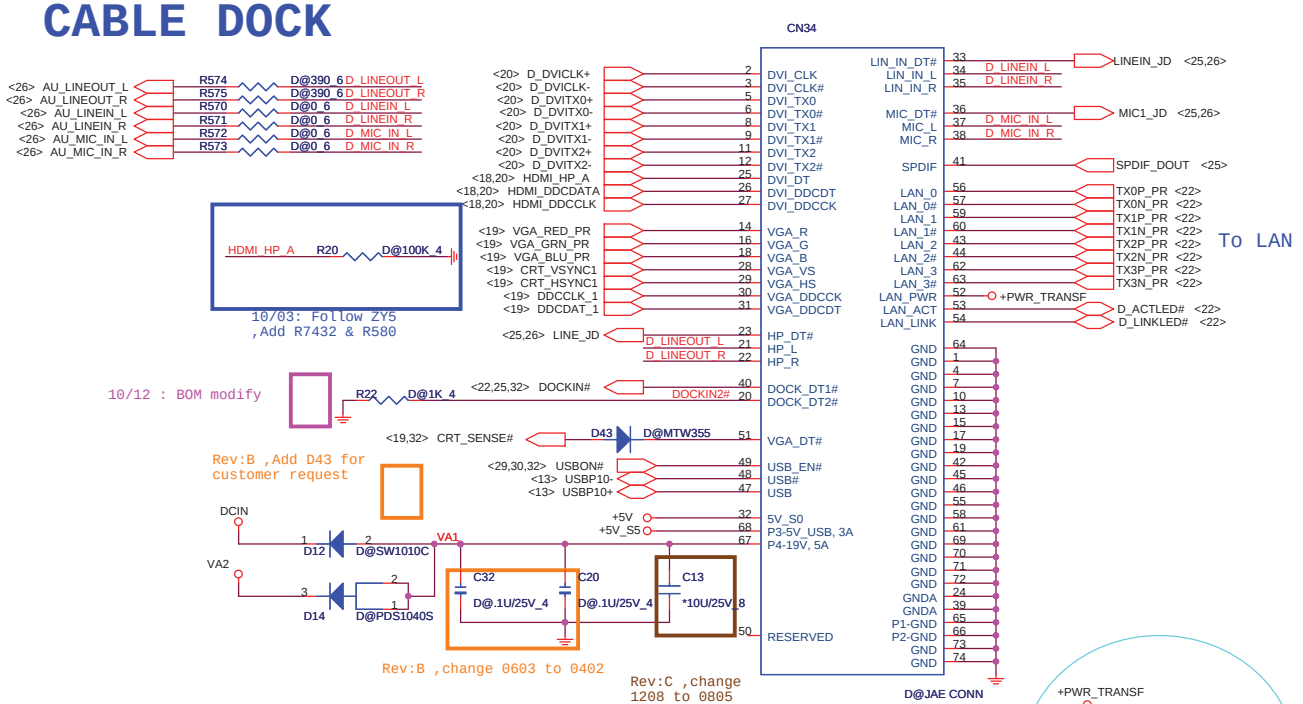
CPU FAN



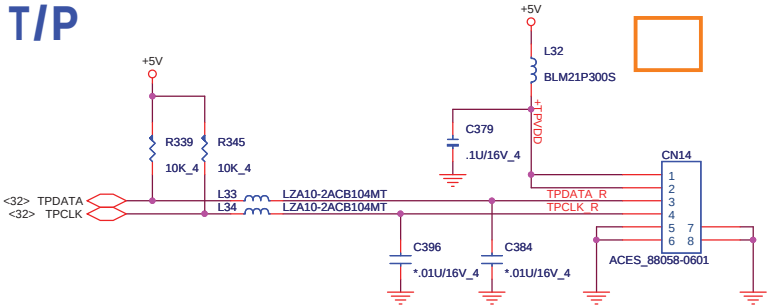
LED

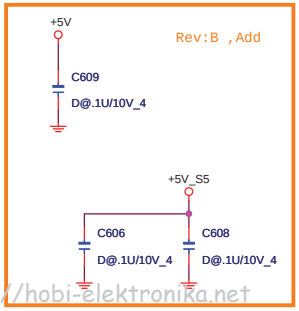


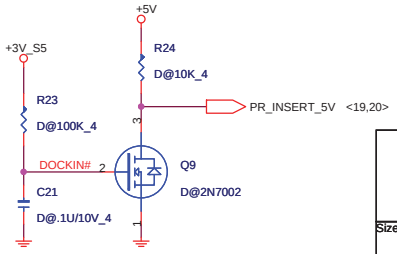
CABLE DOCK

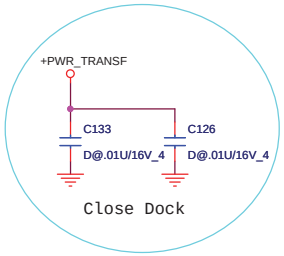


T/P









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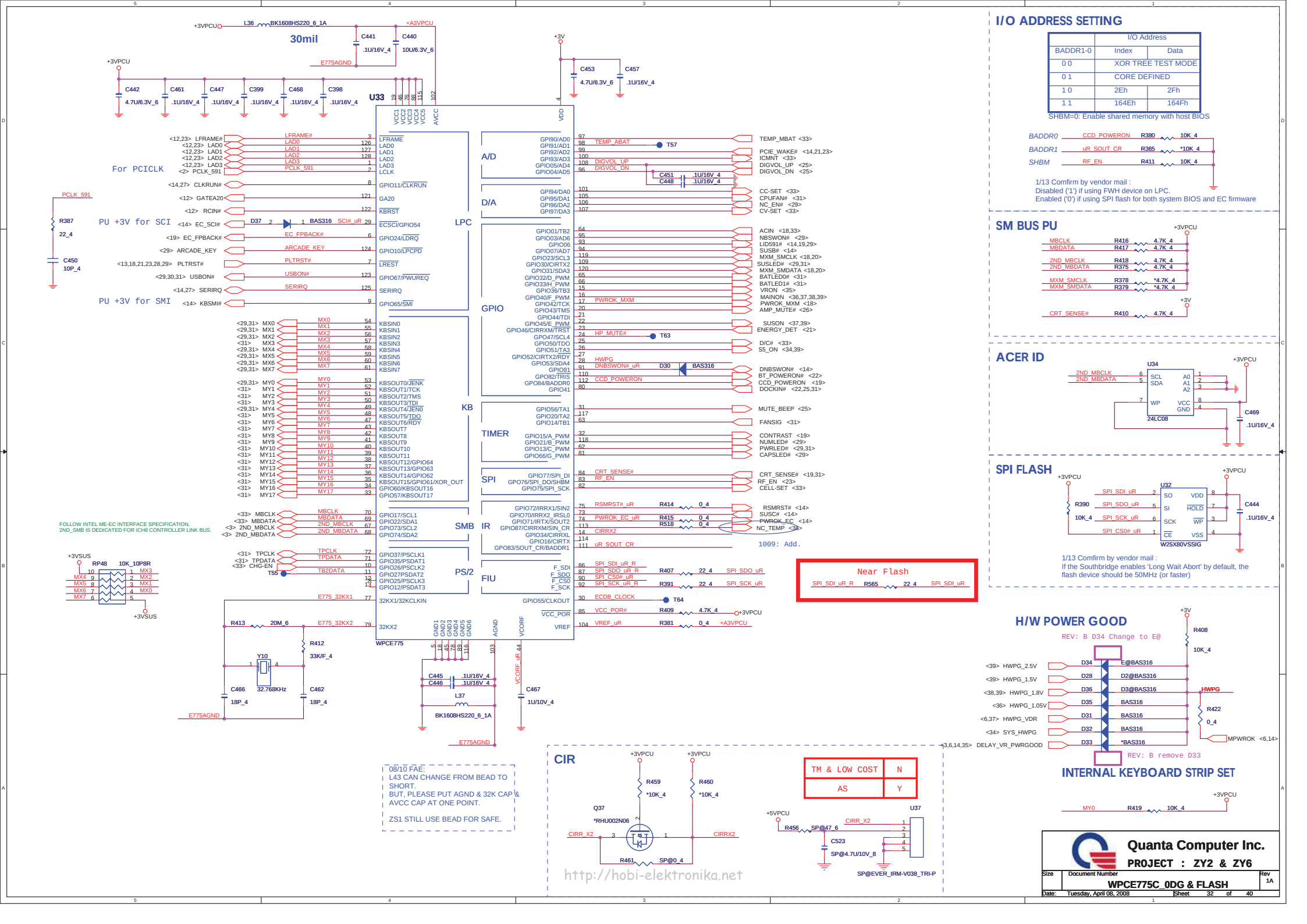
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0
BADDR1
SHBM
CCD_POWERON
uR_SOUT_CR
RF_EN
R380
R365
R411
10K_4
*10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
SM BUS PU
MBCLK
MBDATA
2ND_MBCLK
2ND_MBDATA
MXM_SMCLK
MXM_SMDATA
CRT_SENSE#
R416
R417
R418
R375
R378
R379
R410
4.7K_4
*4.7K_4
ACER ID
U34
24LC08
C469
.1U/16V_4
SPI FLASH
U32
W25X80VSSIG
C444
R390
10K_4
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
H/W POWER GOOD
REV: B D34 Change to E@
R408
D34
D28
D36
D35
D31
D32
D33
E@BAS316
D2@BAS316
D3@BAS316
BAS316
*BAS316
HWPG
R422
0_4
MPWROK
REV: B remove D33
INTERNAL KEYBOARD STRIP SET
U33
WPCE775
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
SMB
IR
PS/2
FIU
Near Flash
SPI_SDI_uR_R
R565
22_4
SPI_SDI_uR
1009: Add.
FOLLOW INTEL ME-EC INTERFACE SPECIFICATION,
2ND_SMB IS DEDICATED FOR ICH8 CONTROLLER LINK BUS.
RP48
10K_10P8R
For PCICLK
PU +3V for SCI
PU +3V for SMI
BAS316
R387
22_4
C450
10P_4
Y10
32.768KHz
R413
20M_6
R412
33K/F_4
C466
C462
18P_4
L37
BK1608HS220_6_1A
C467
1U/10V_4
08/10 FAE:
L43 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
CIR
Q37
*RHU002N06
R459
R460
R461
SP@0_4
CIRR_X2
CIRRX2
TM & LOW COST
N
AS
Y
U37
SP@EVER_IRM-V038_TRI-P
C523
SP@4.7U/10V_8
R456
SP@47_6
http://hobi-elektronika.net
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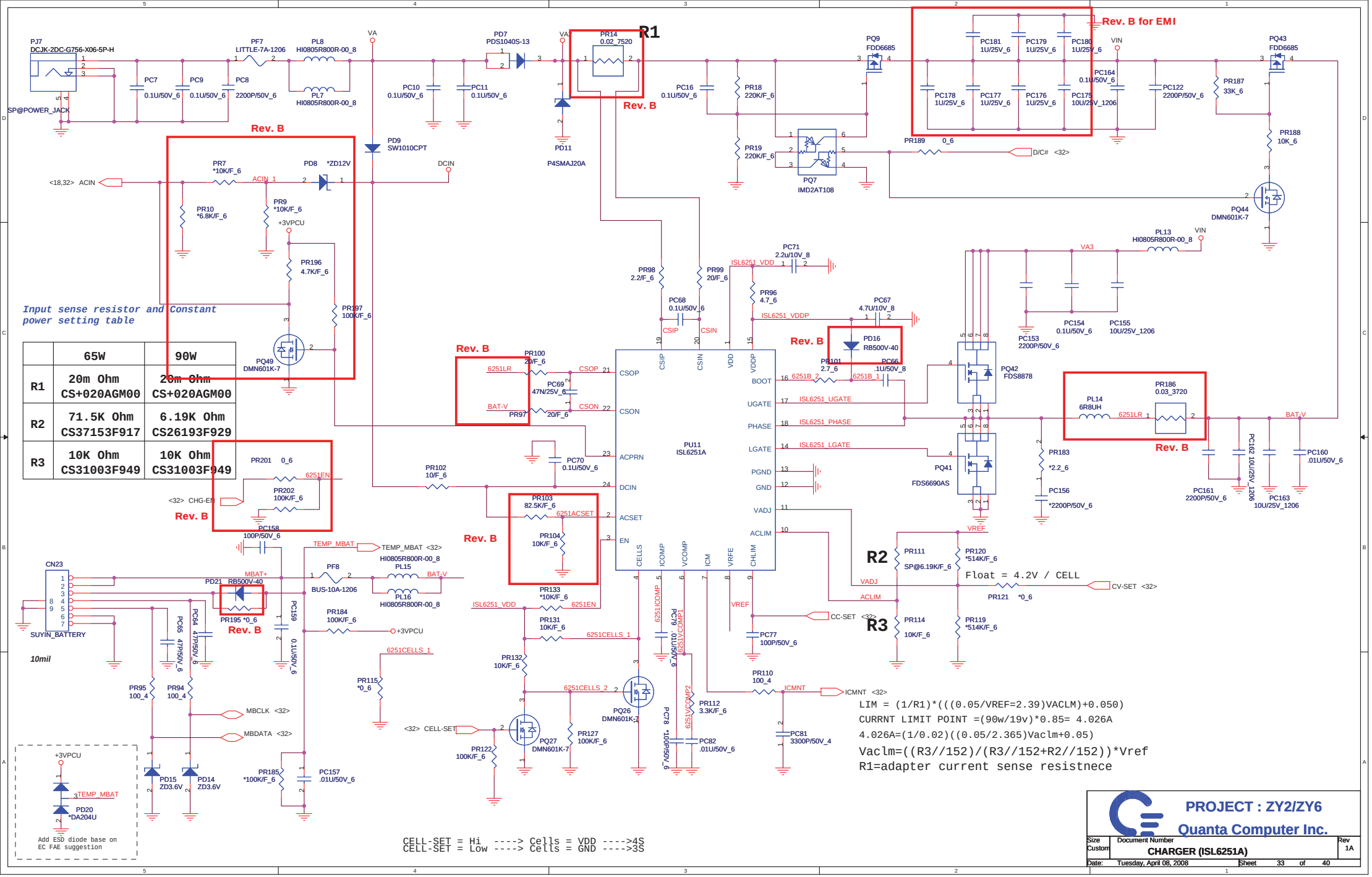
R1
R2
R3
Rev. B
Rev. B for EMI
Input sense resistor and Constant power setting table
65W
90W
R1
20m Ohm CS+020AGM00
20m Ohm CS+020AGM00
R2
71.5K Ohm CS37153F917
6.19K Ohm CS26193F929
R3
10K Ohm CS31003F949
10K Ohm CS31003F949
PU11 ISL6251A
Float = 4.2V / CELL
LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S
Add ESD diode base on EC FAE suggestion
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CHARGER (ISL6251A)
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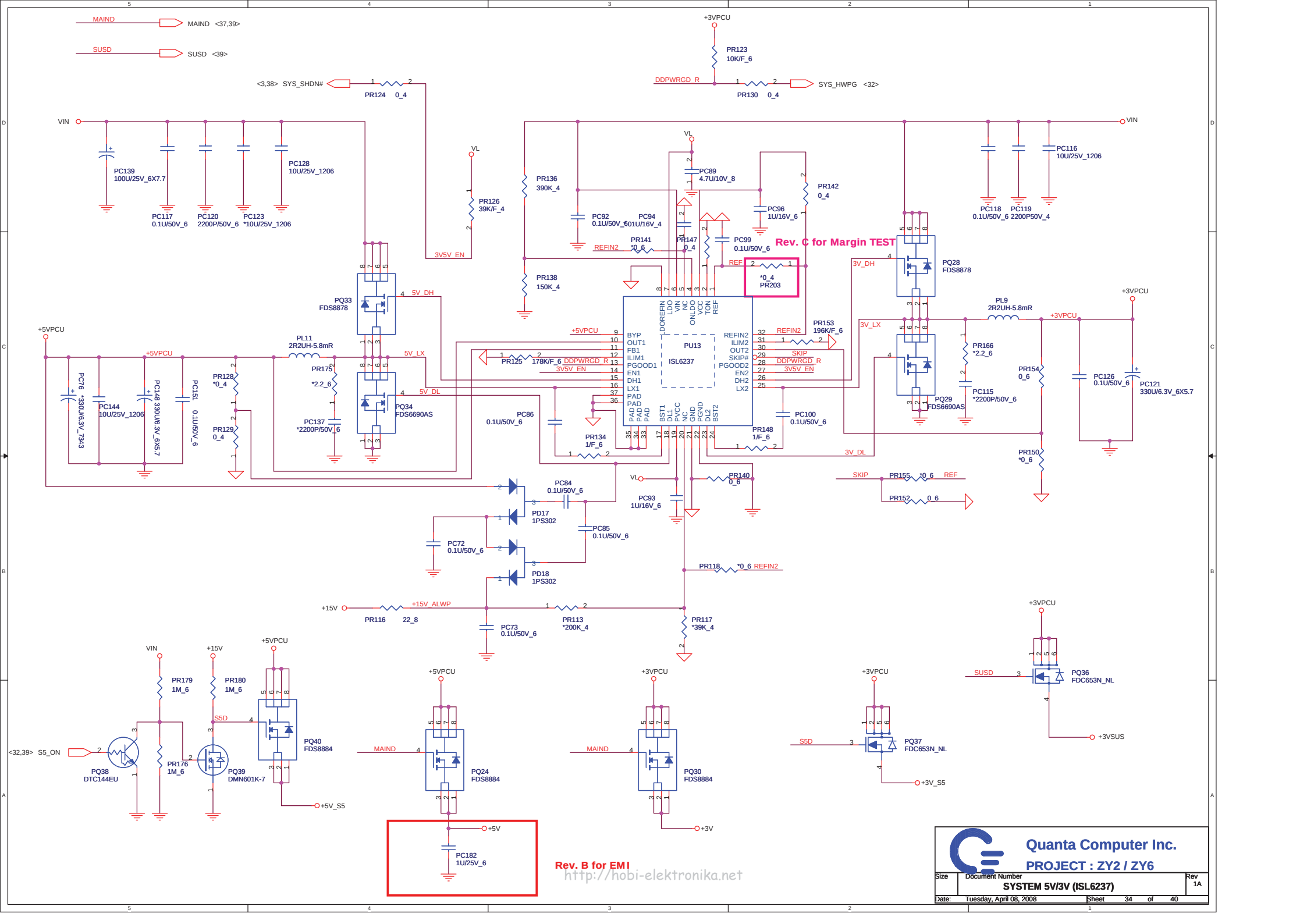
http://hobi-elektronika.net


MAIND
MAIND <37,39>
SUSD
SUSD <39>
<3,38> SYS_SHDN#
PR124 0_4
+3VPCU
PR123 10K/F_6
DDPWRGD_R
PR130 0_4
SYS_HWPG <32>
VIN
PC139 100U/25V_6X7.7
PC117 0.1U/50V_6
PC120 2200P/50V_6
PC123 *10U/25V_1206
PC128 10U/25V_1206
VL
PR126 39K/F_4
3V5V_EN
PR136 390K_4
PR138 150K_4
PC92 0.1U/50V_6
PC94 01U/16V_4
REFIN2
PR141 *0_6
PC89 4.7U/10V_8
PR147 0_4
PC99 0.1U/50V_6
PC96 1U/16V_6
PR142 0_4
REF
*0_4 PR203
Rev. C for Margin TEST
PC118 0.1U/50V_6
PC119 2200P50V_4
PC116 10U/25V_1206
PQ28 FDS8878
3V_DH
PQ33 FDS8878
5V_DH
+5VPCU
PL11 2R2UH-5.8mR
5V_LX
5V_DL
PR128 *0_4
PR129 0_4
PR175 *2.2_6
PC137 *2200P/50V_6
PQ34 FDS6690AS
PC76 *330U/6.3V_7343
PC144 10U/25V_1206
PC148 330U/6.3V_6X5.7
PC151 0.1U/50V_6
PC86 0.1U/50V_6
PU13
ISL6237
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND GND DL2 BST2
PR125 178K/F_6 DDPWRGD_R
PR153 196K/F_6
PR134 1/F_6
PR148 1/F_6
PC100 0.1U/50V_6
3V_LX
PQ29 FDS6690AS
PL9 2R2UH-5.8mR
PR166 *2.2_6
PC115 *2200P/50V_6
PR154 0_6
PR150 *0_6
PC126 0.1U/50V_6
PC121 330U/6.3V_6X5.7
SKIP
PR155 *0_6
PR152 0_6
PC84 0.1U/50V_6
PD17 1PS302
PD18 1PS302
PC72 0.1U/50V_6
PC85 0.1U/50V_6
PC93 1U/16V_6
PR140 0_6
PR118 *0_6
+15V
+15V_ALWP
PR116 22_8
PR113 *200K_4
PR117 *39K_4
PC73 0.1U/50V_6
PR179 1M_6
PR180 1M_6
PR176 1M_6
<32,39> S5_ON
PQ38 DTC144EU
PQ39 DMN601K-7
S5D
PQ40 FDS8884
+5V_S5
PQ24 FDS8884
PQ30 FDS8884
+3V_S5
PQ36 FDC653N_NL
PQ37 FDC653N_NL
+3VSUS
PC182 1U/25V_6
+5V
+3V
Rev. B for EMI
http://hobi-elektronika.net
Quanta Computer Inc.
PROJECT : ZY2 / ZY6
Size
Document Number
SYSTEM 5V/3V (ISL6237)
Rev 1A
Date: Tuesday, April 08, 2008
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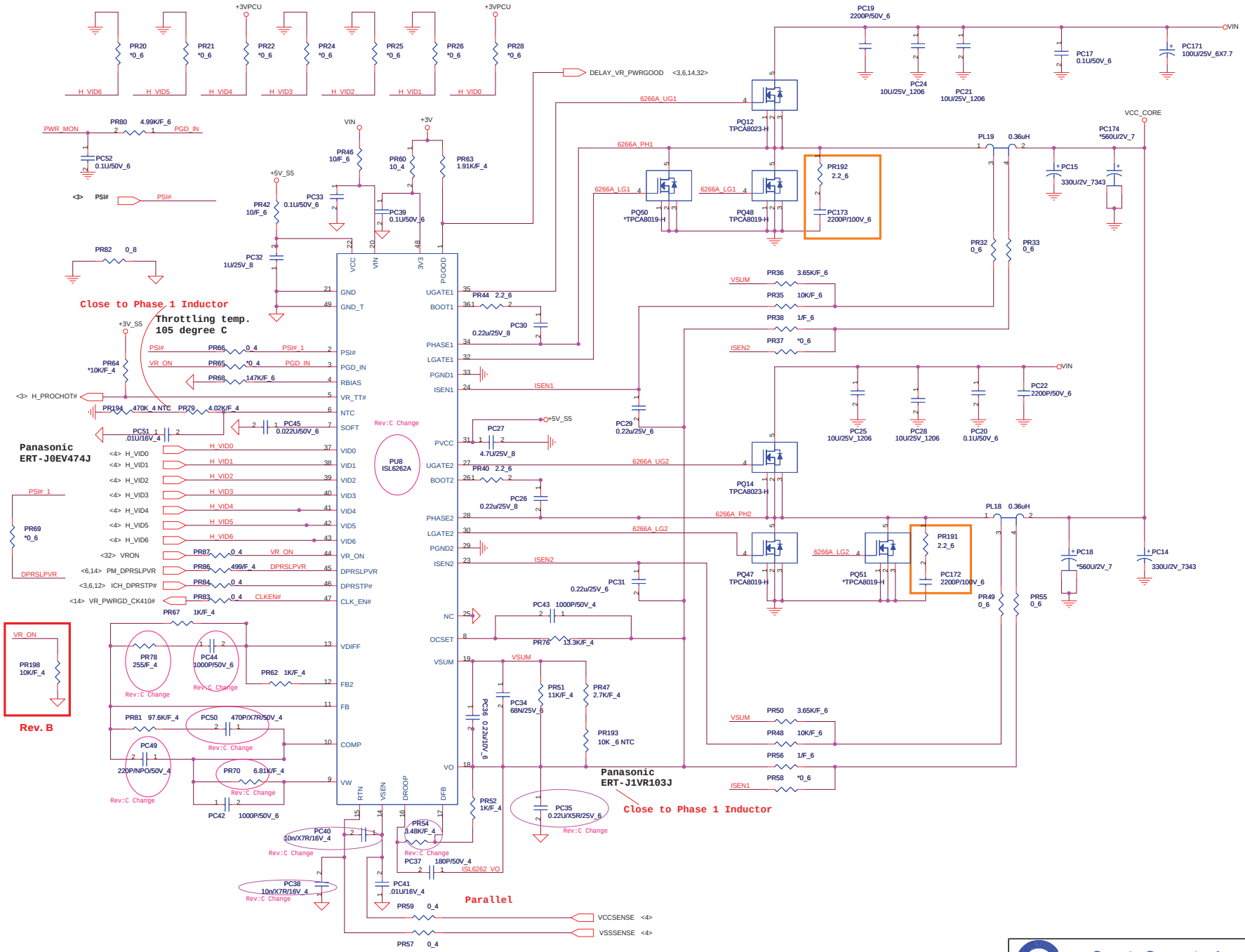
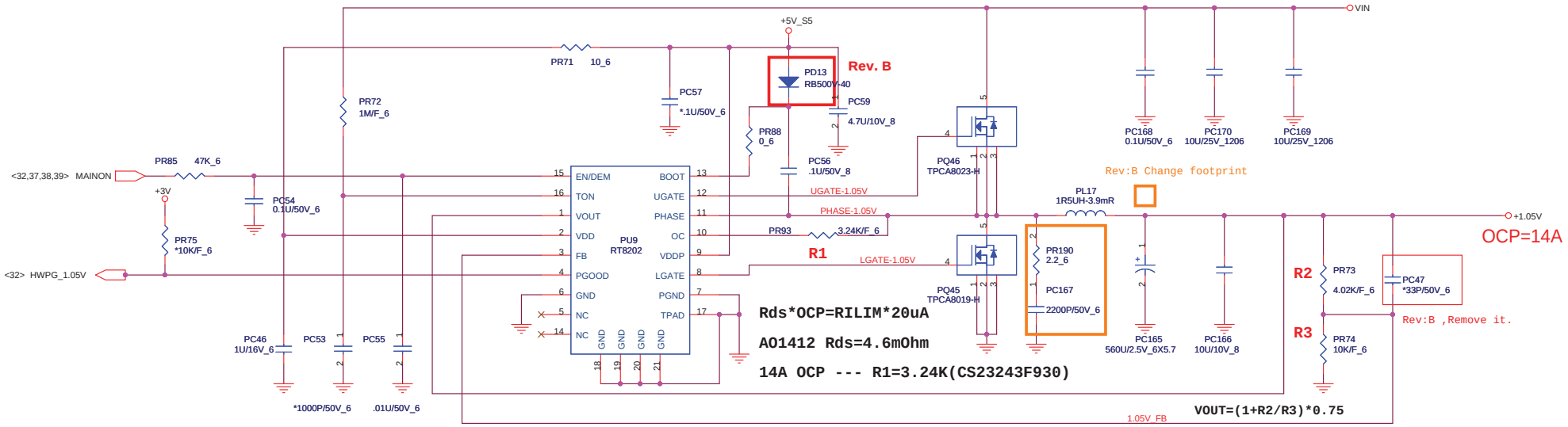


Quanta Computer Inc.
PROJECT : ZY2 / ZY6

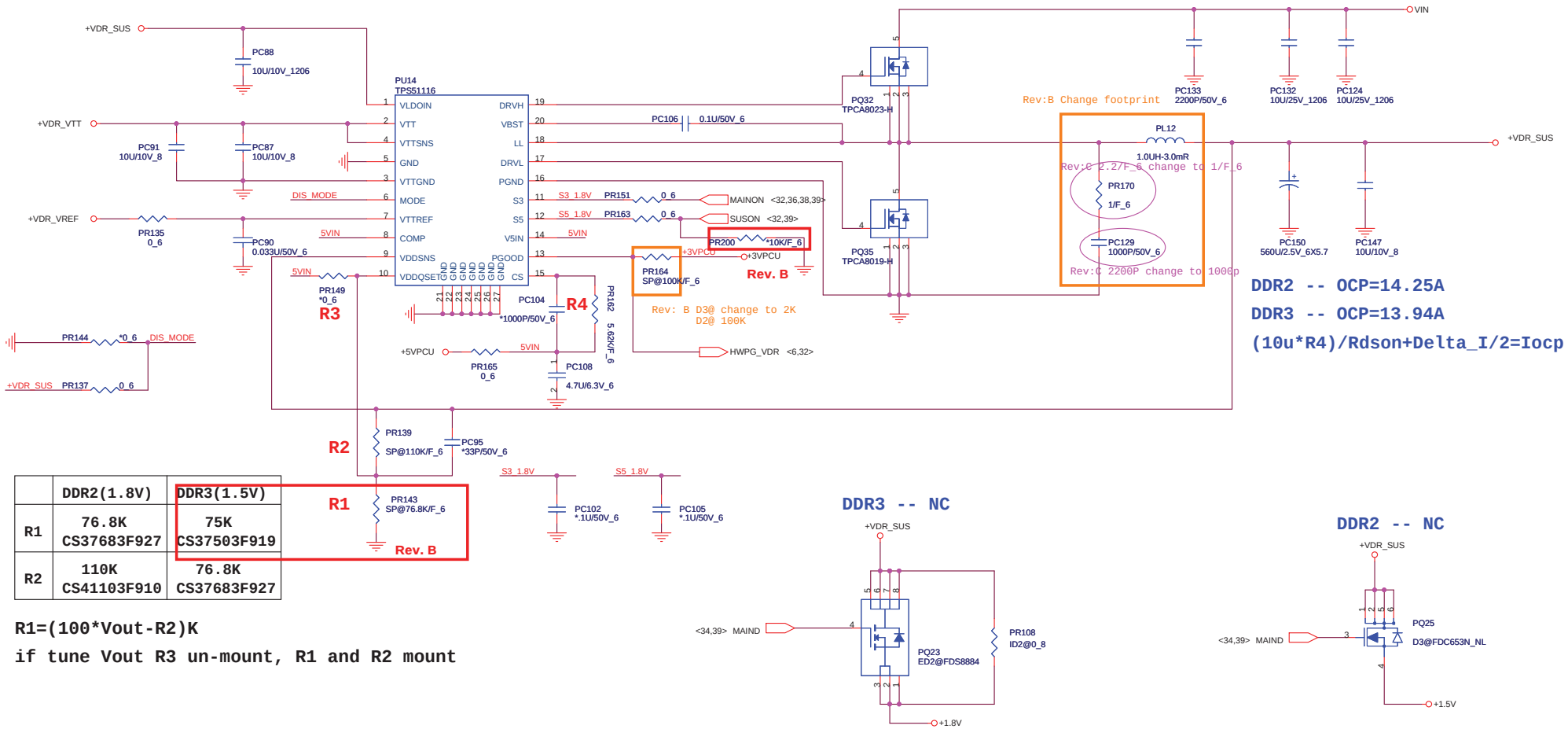
Size	Document Number	Rev
Custom	CPU CORE(ISL6266)	1A
Date: Tuesday, April 08, 2008	Sheet 35 of 40	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.		
PROJECT : ZY2 / ZY6		
Size	Document Number: VTT 1.05V (RT8202)	Rev: 1A
Date: Tuesday, April 08, 2008	Sheet 36 of 40	



	DDR2(1.8V)	DDR3(1.5V)
R1	76.8K CS37683F927	75K CS37503F919
R2	110K CS41103F910	76.8K CS37683F927

R1=(100*Vout-R2)K

if tune Vout R3 un-mount, R1 and R2 mount

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PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	VDR (TPS51116)	1A

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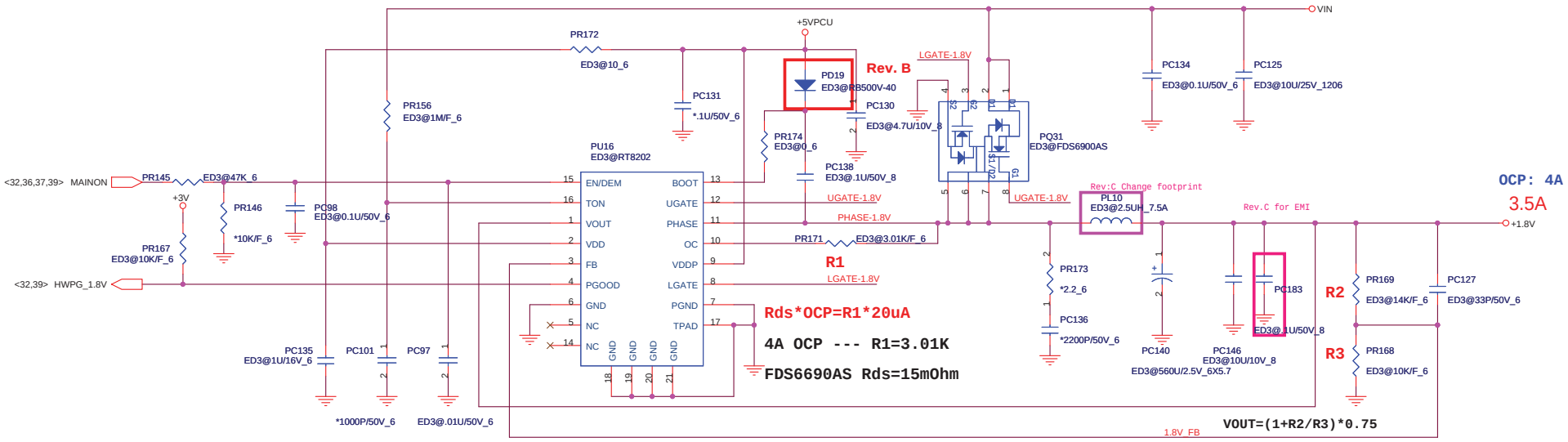
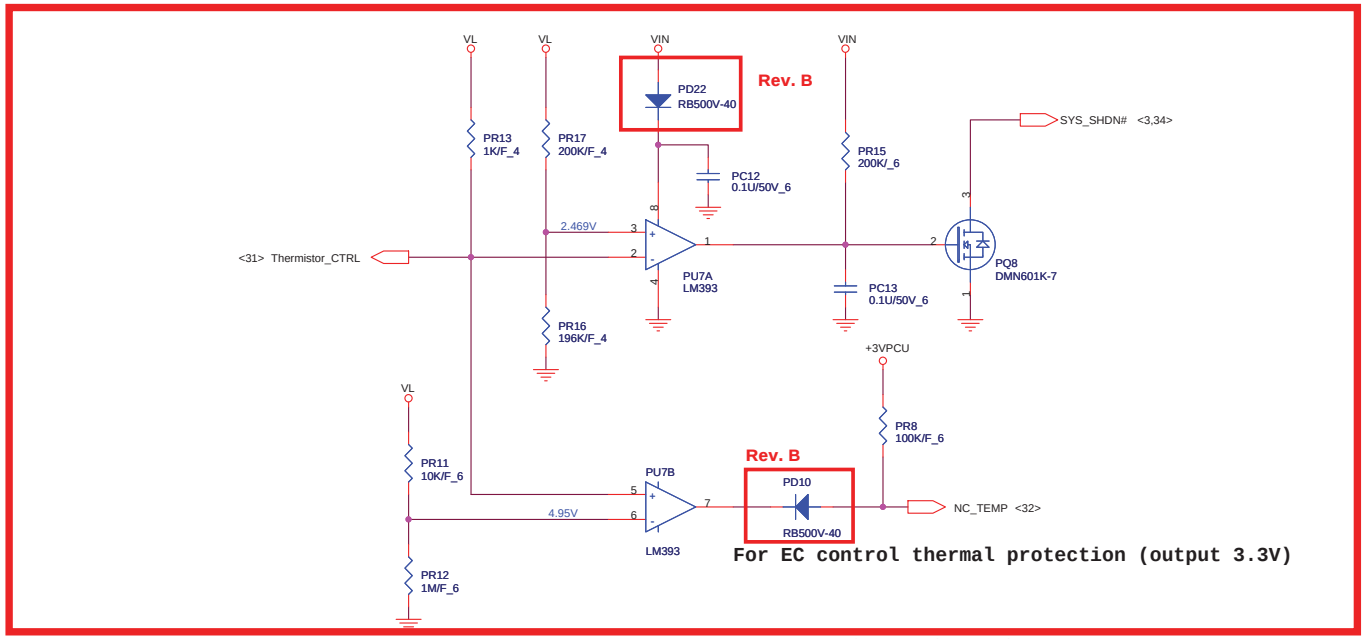


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

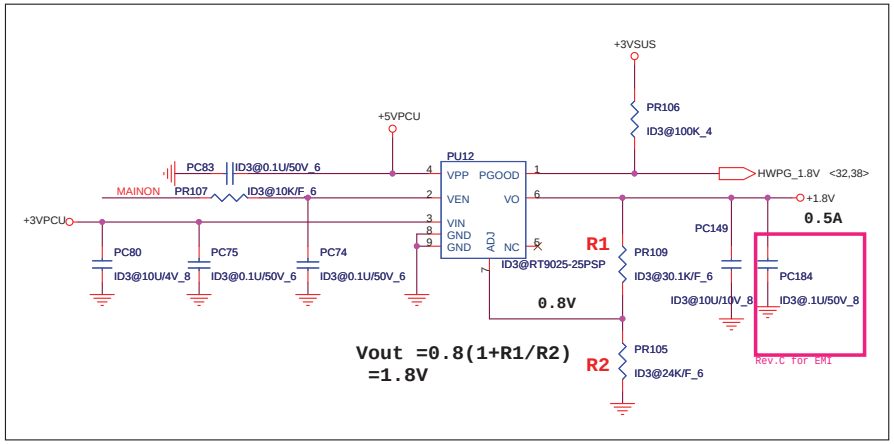
thermal protection --0928



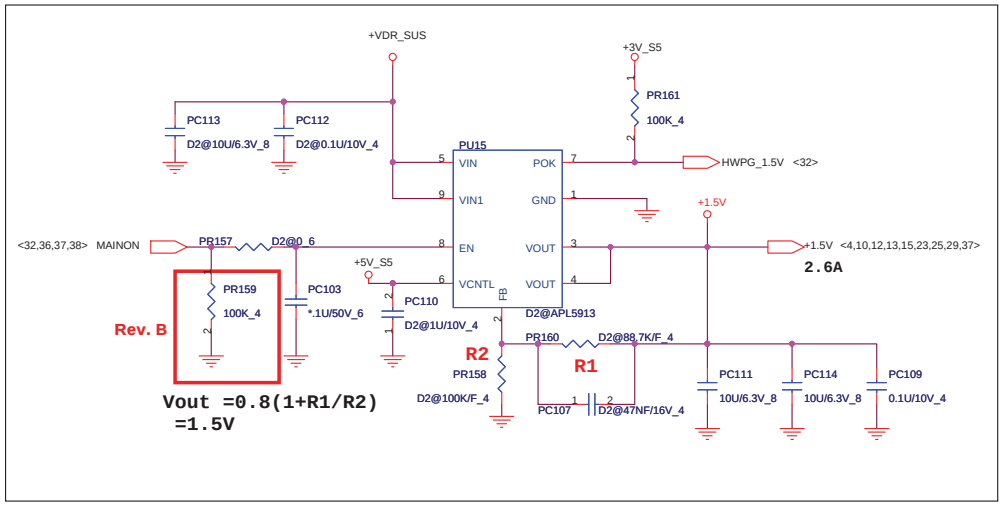
Quanta Computer Inc.
PROJECT : ZY2 / ZY6

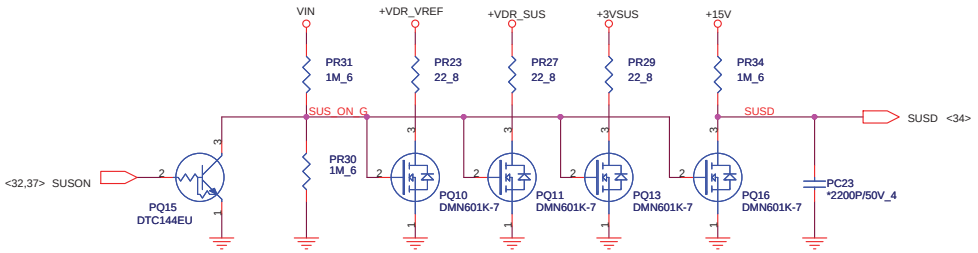
Size	Document Number	Rev
	1.8V (RT8202)	1A
Date: Tuesday, April 08, 2008	Sheet 38 of 40	

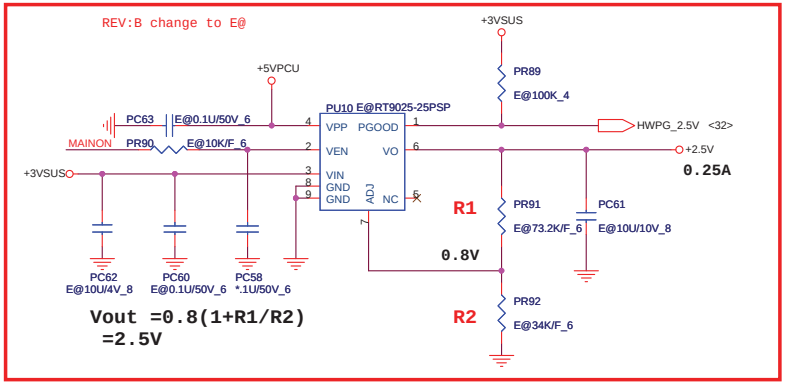
for DDR3 and UMA

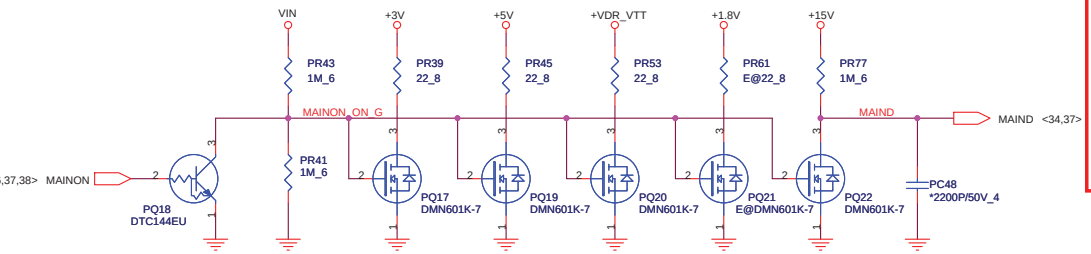


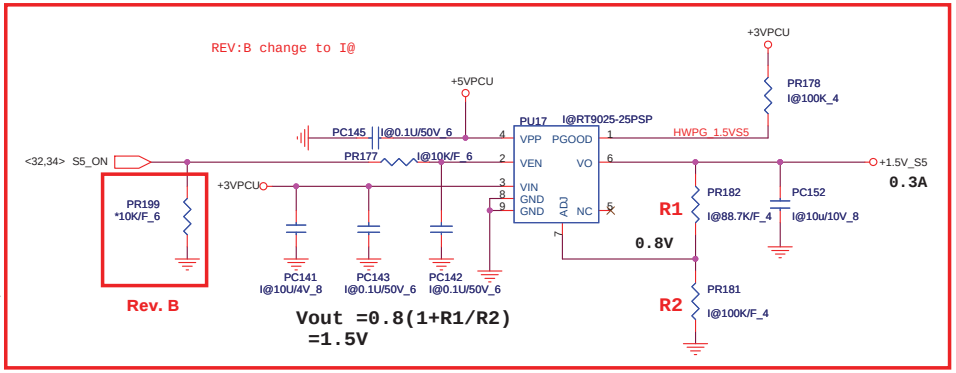
DDR3 -- NC











REV:B change to E@

Quanta Computer Inc.
PROJECT : ZY2 / ZY6

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A
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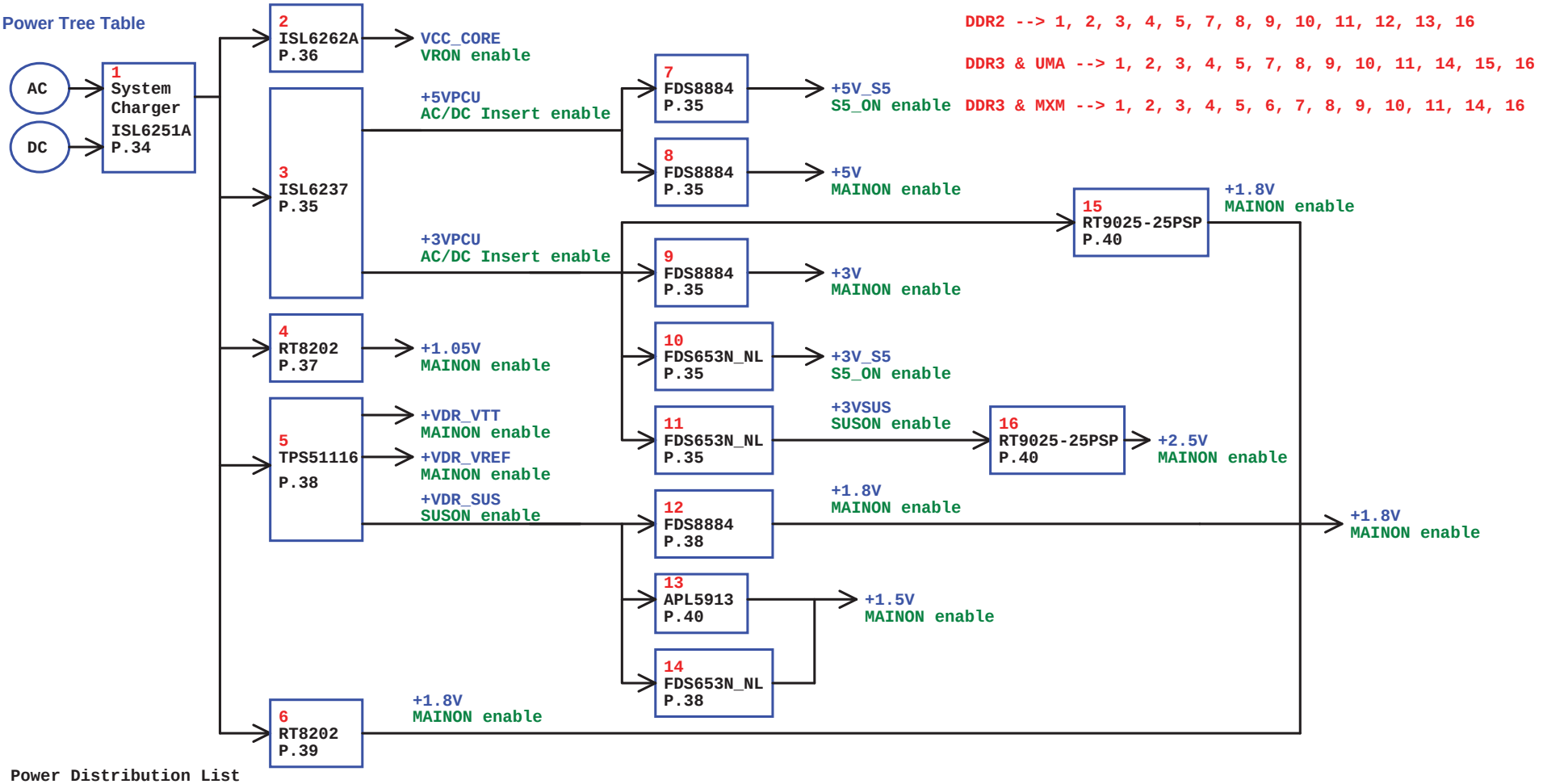
Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (OZ129T) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	Power Tree Table	1A

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CHANGE LIST

Model	REV	
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)
	2A	Page19 : change U22 LVDS PWR SW IC to TI for display isuue Page21 : remove 5787 schematic Page23 : Add C605 ,C70 ,C150 ,C613 &C614 for EMI request Page23 : Change CN27 CONN. & schematic for intel WL burnout issue Page25 :change U13 packing from TQFN to TDFN for vendor request
	2B	Page20 : Add

MODEL	ZY2 FROM	ZY2 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

PROJECT : ZY2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A

Date: Wednesday, April 09, 2008 Sheet 41 of 41

DOC NO.					
PROJECT MODEL :	ZY2	APPROVED BY:		DATE:	2007/ 2/15
PART NUMBER:		DRAWING BY:		REVISON:	3A