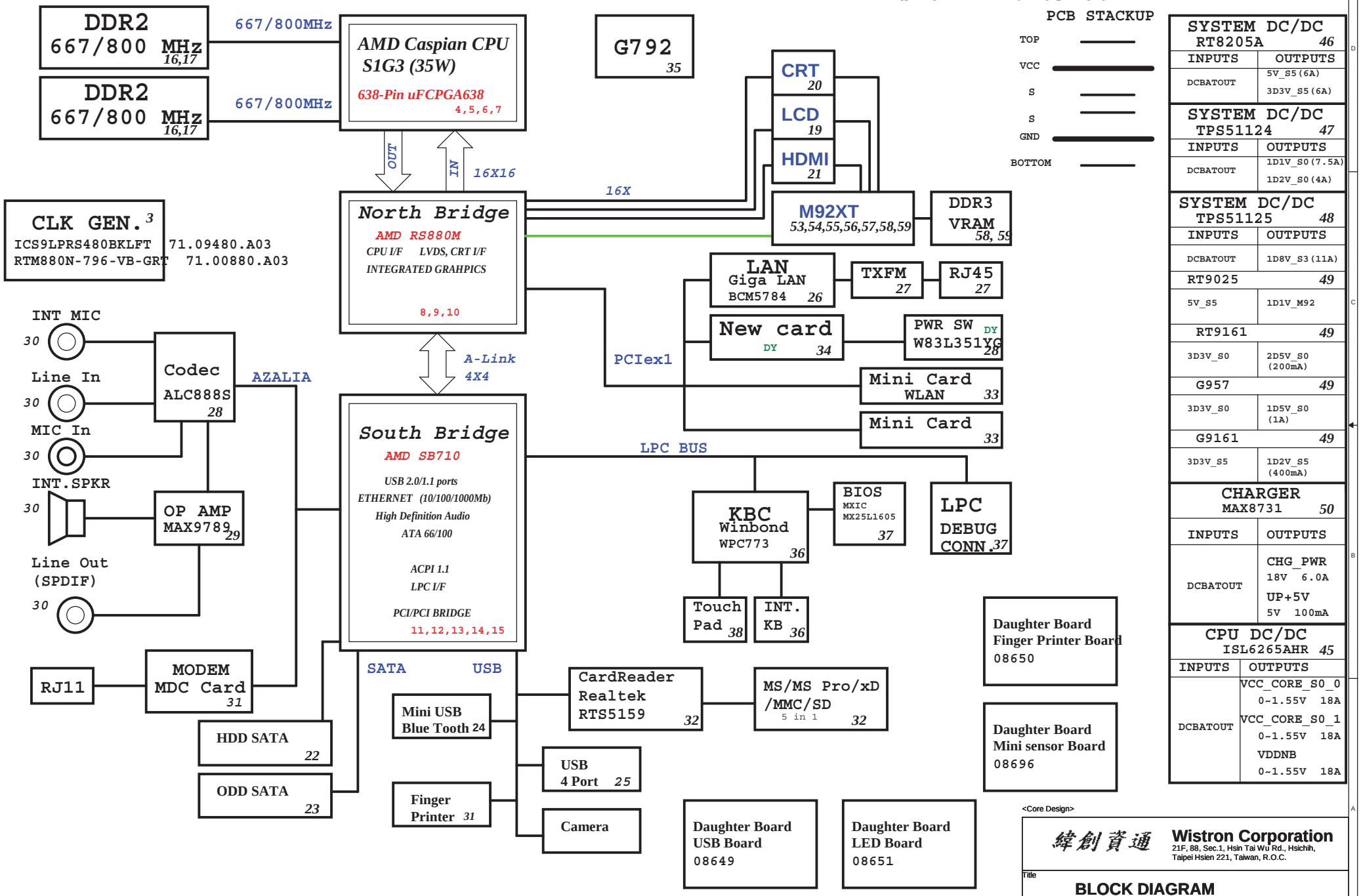
JV50-TR Block Diagram

Project code: 91.4FN01.001
PCB P/N : 48.4FN01.001
REVISION : 09230- -1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC TPS51125 48	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49	
5V_S5	1D1V_M92

RT9161 49	
3D3V_S0	2D5V_S0 (200mA)

G957 49	
3D3V_S0	1D5V_S0 (1A)

G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265AHR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JV50-TR | Rev: SB
Date: Tuesday, June 16, 2009 | Sheet 1 of 61

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV50-TR	A

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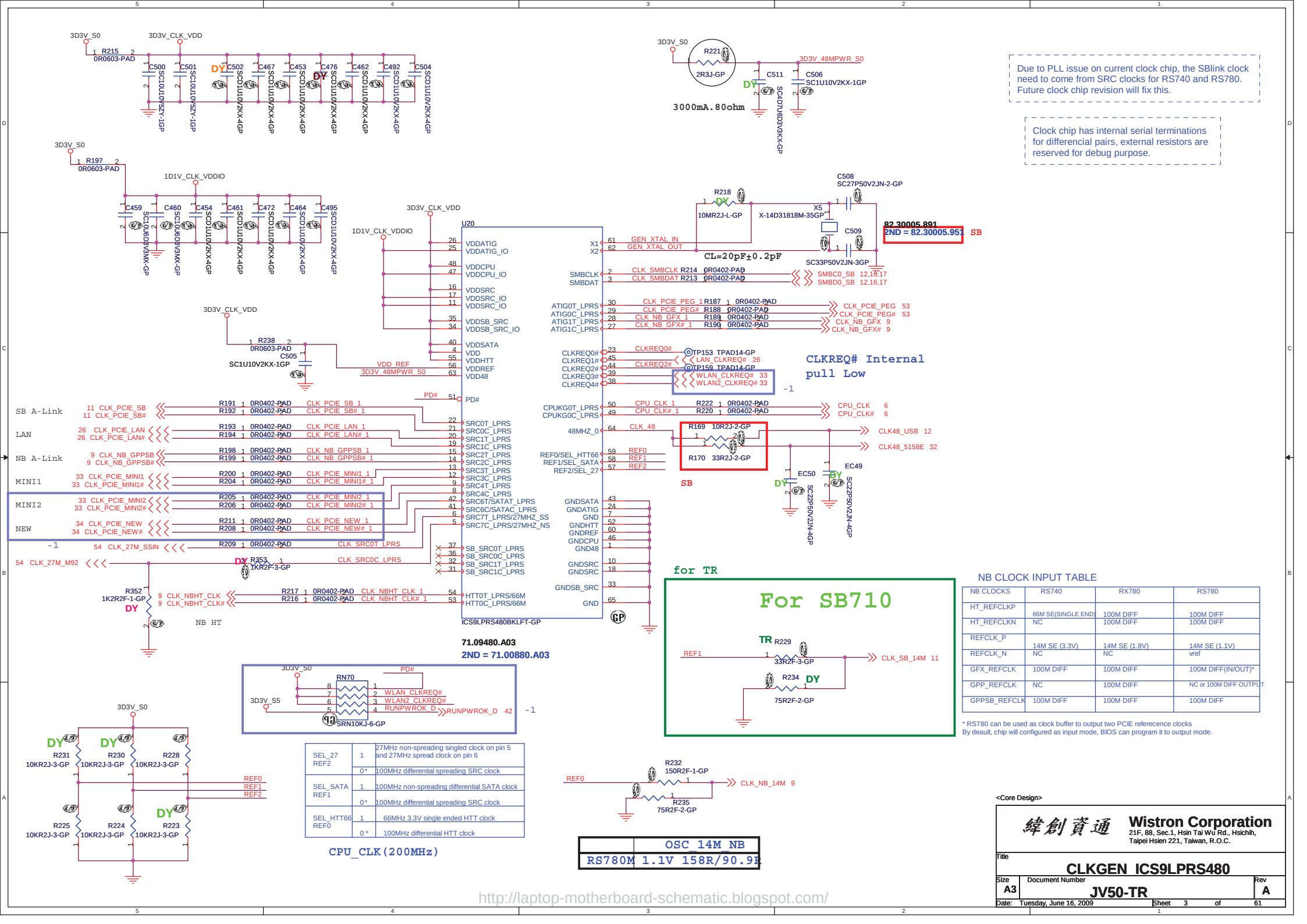
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.
CLKREQ# Internal pull Low
for TR
For SB710
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
CPU_CLK(200MHz)
OSC_14M_NB
RS780M 1.1V 158R/90.9R
82.30005.891
2ND = 82.30005.951 SB
71.09480.A03
2ND = 71.00880.A03
ICS9LPRS480BKLFT-GP
CL=20pF±0.2pF
3000mA.80ohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CLKGEN_ICS9LPRS480
JV50-TR
Size A3
Rev A
Date: Tuesday, June 16, 2009
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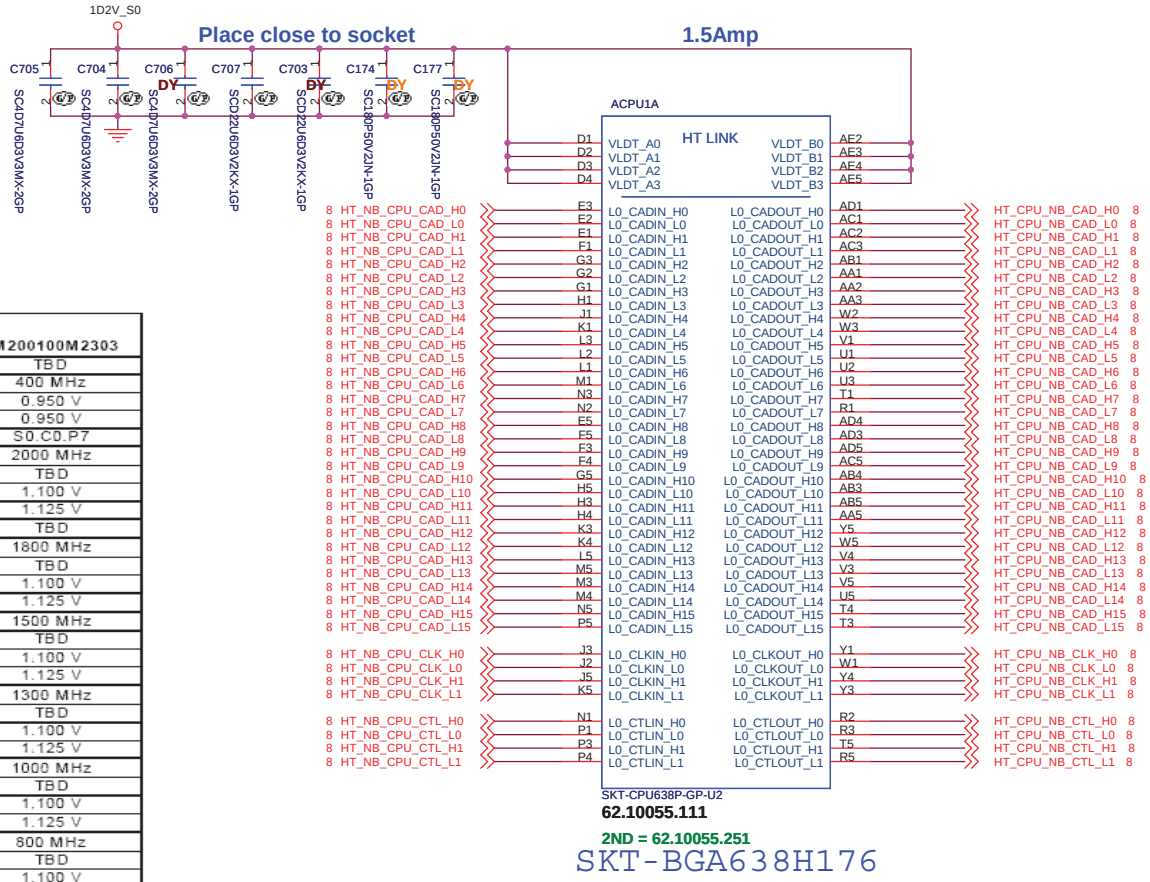
http://laptop-motherboard-schematic.blogspot.com/



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

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Title: CPU HT LINK I/F (1/4)

Size: A3 | Document Number: JV50-TR | Rev: SB

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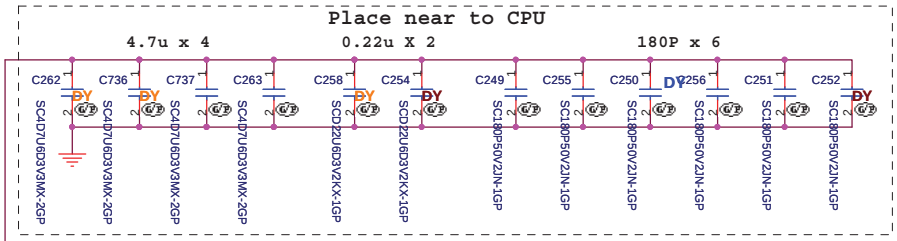
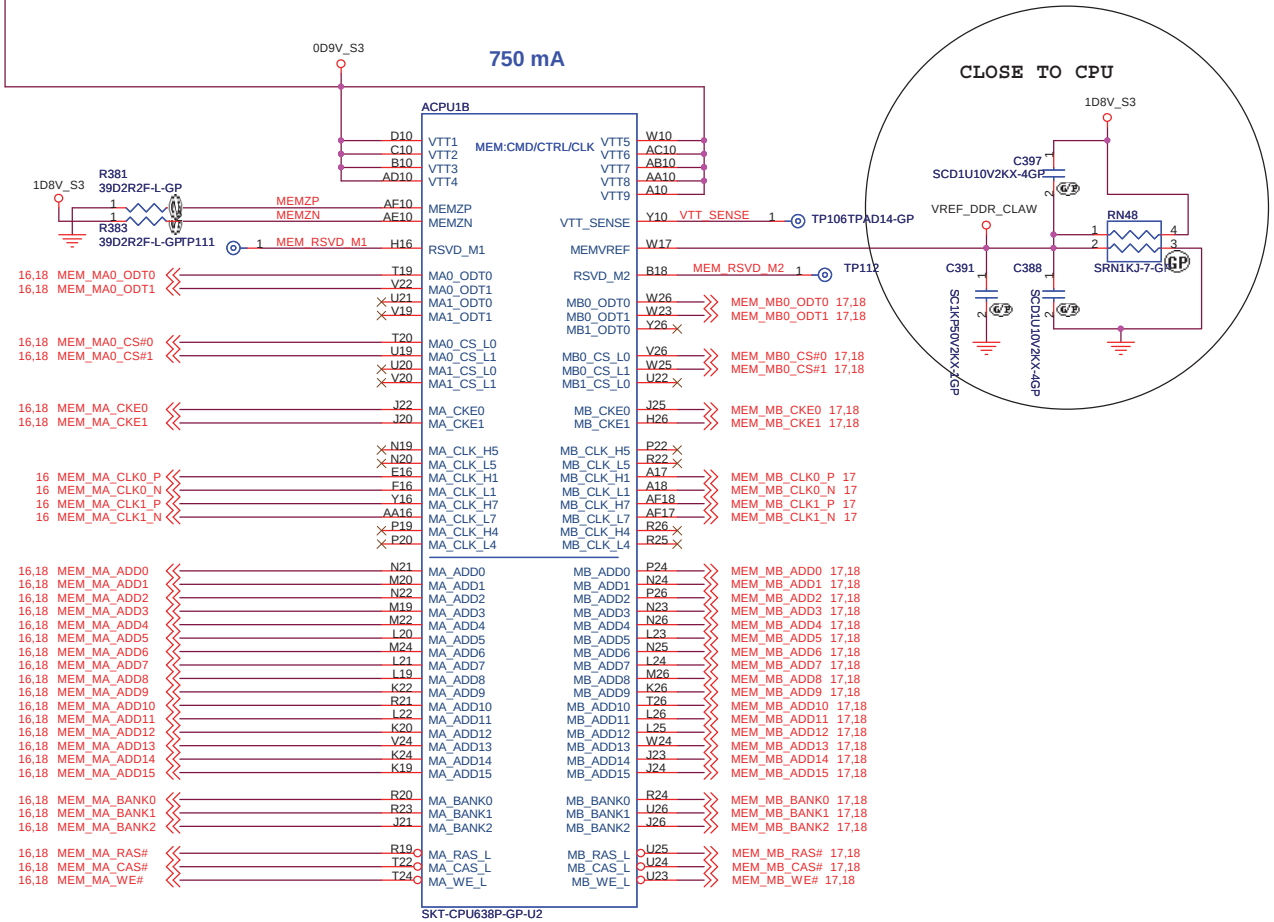
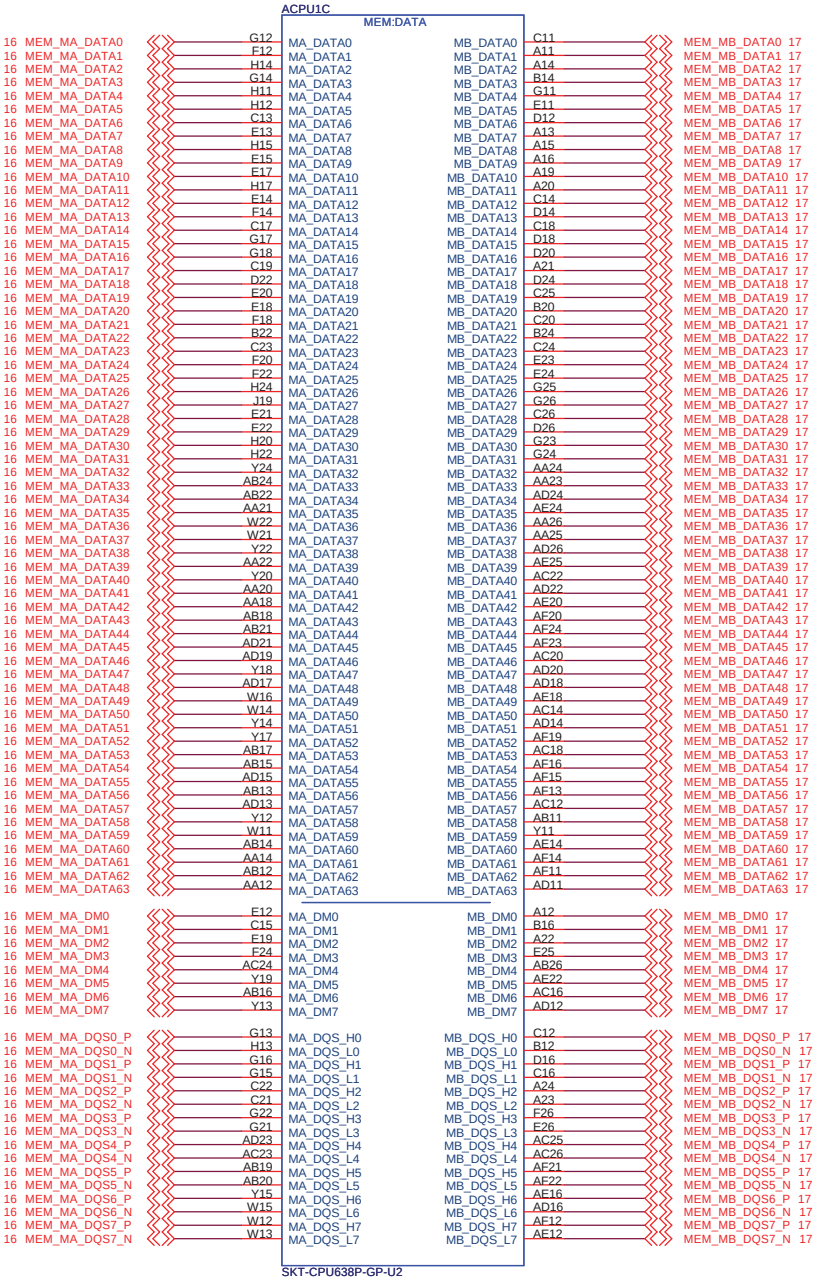




62.10055.111



<Core Design>

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Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	JV50-TR	SB

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The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

SB

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

for TR

PU-->300R
TR-->510R

Near CPU PIN

CPU exceeds to 125℃

84.T3904.C11
2ND = 84.03904.L06

SKT-CPU638P-GP-U2

HDT Connectors

<Core Design>

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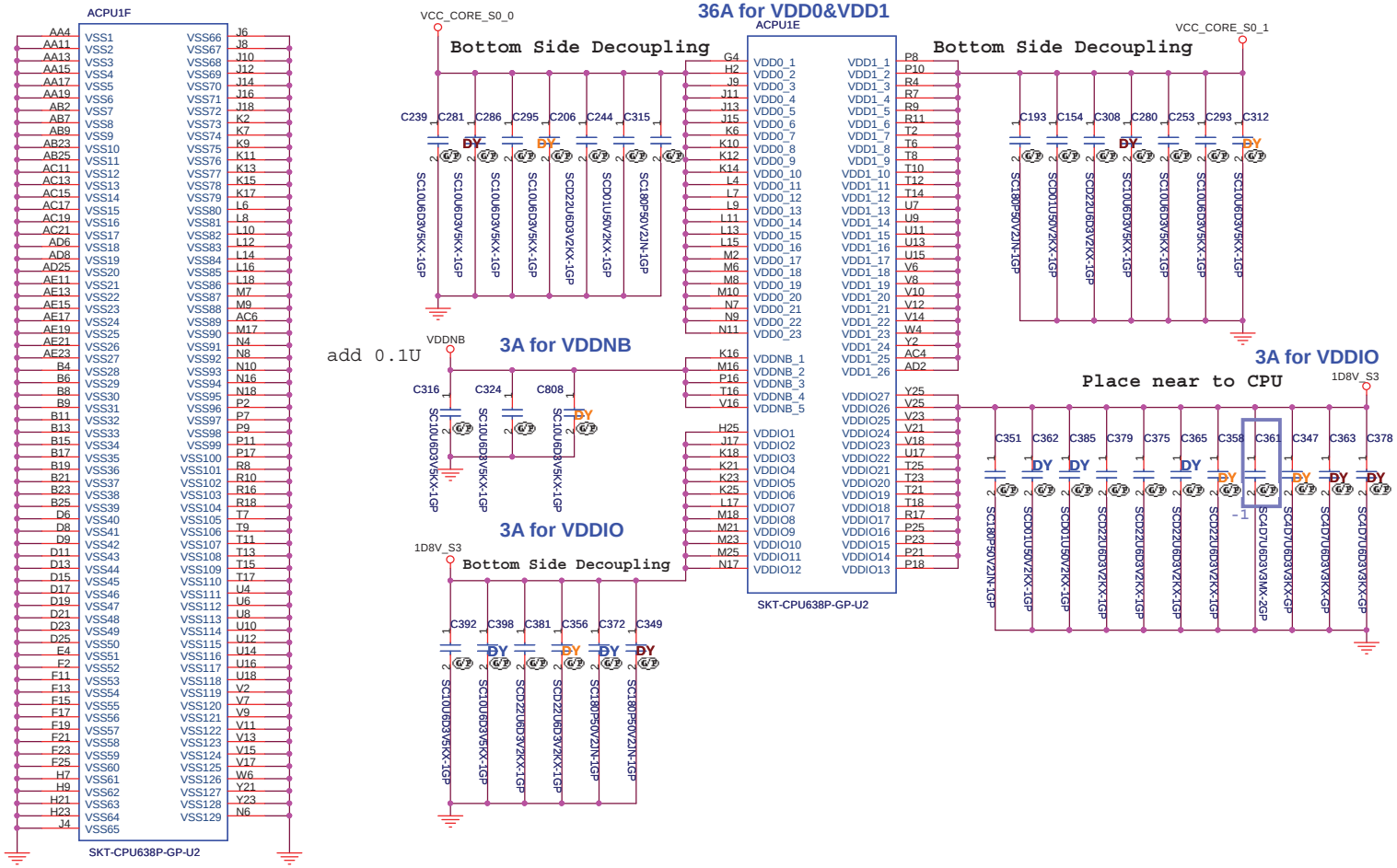
Title: CPU_Control&Debug_(3/4)		
Size: A3	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 6 of 61	



<Core Design>

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Title: CPU_Power_(4/4)

Size: A3 | Document Number: JV50-TR | Rev: SB

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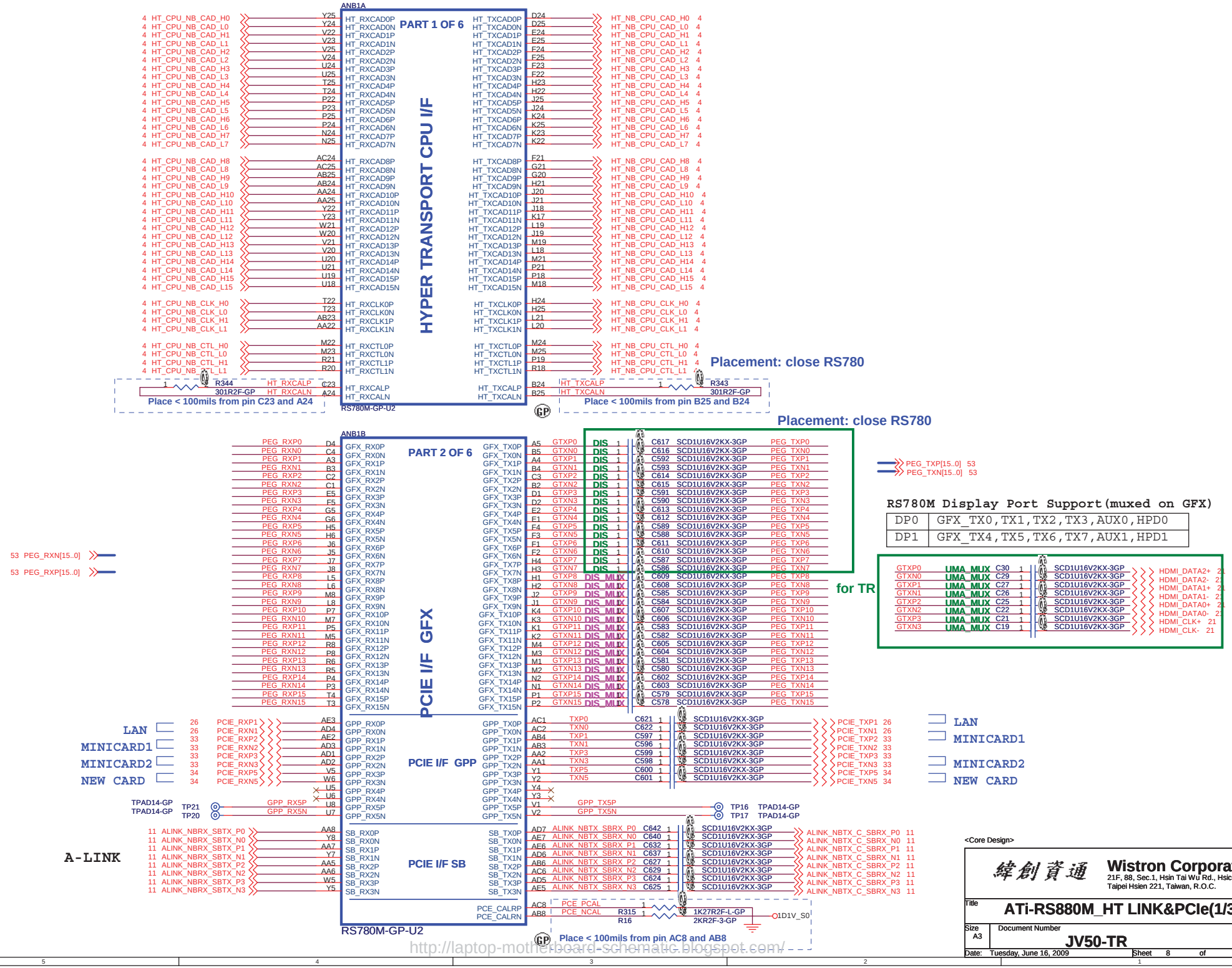

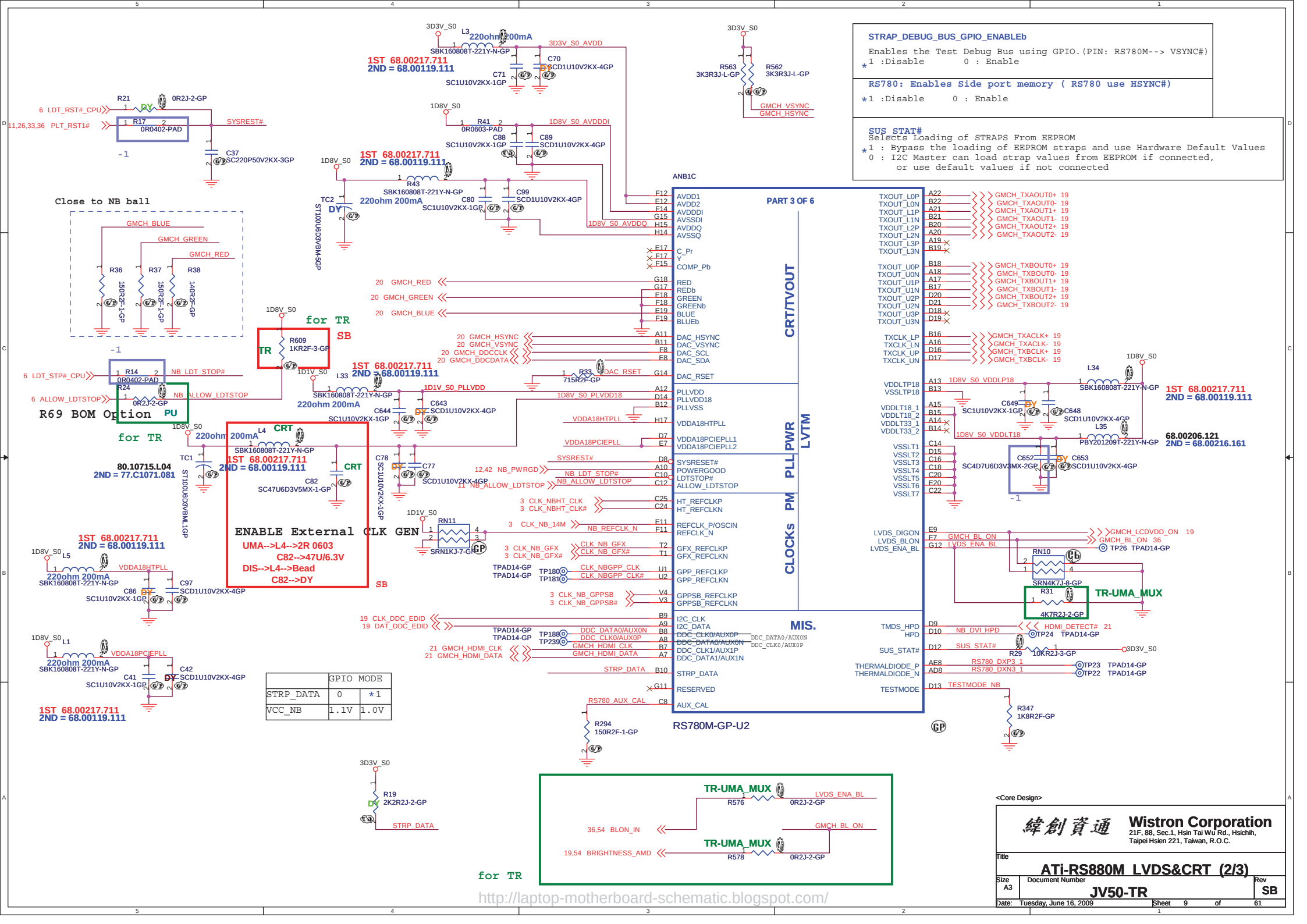
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
ANB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
PWR
LVTM
PLL
CLOCKs
PM
MIS.
Close to NB ball
R69 BOM Option PU
for TR
SB
ENABLE External CLK GEN
UMA-->L4-->2R 0603
C82-->47U/6.3V
DIS-->L4-->Bead
C82-->DY
TR-UMA_MUX
80.10715.L04
2ND = 77.C1071.081
68.00206.121
2ND = 68.00216.161
1ST 68.00217.711
2ND = 68.00119.111
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.1V 1.0V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS880M LVDS&CRT (2/3)
JV50-TR
Rev SB
Tuesday, June 16, 2009
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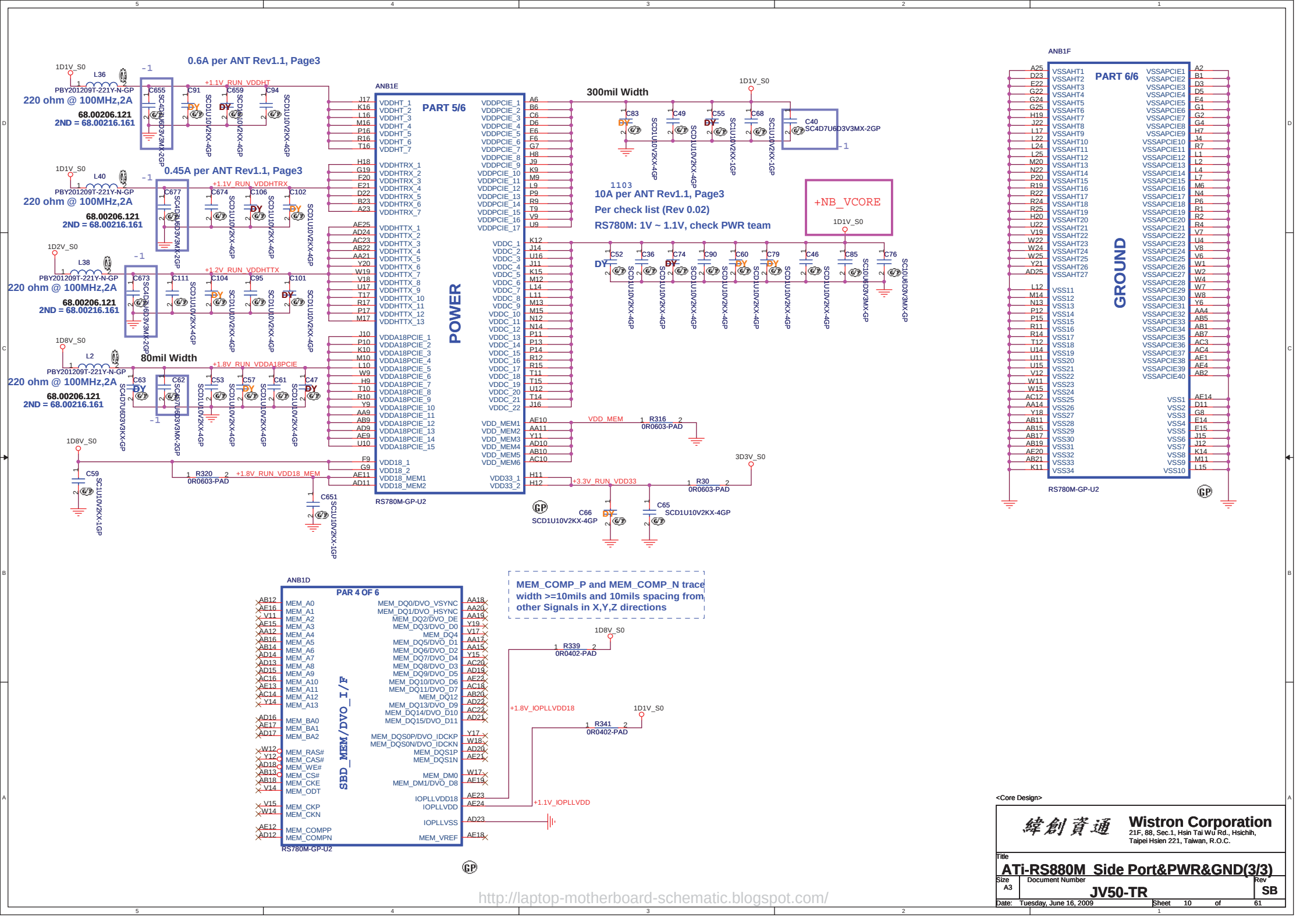
http://laptop-motherboard-schematic.blogspot.com/



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Title: ATi-RS880M Side Port&PWR&GND(3/3)

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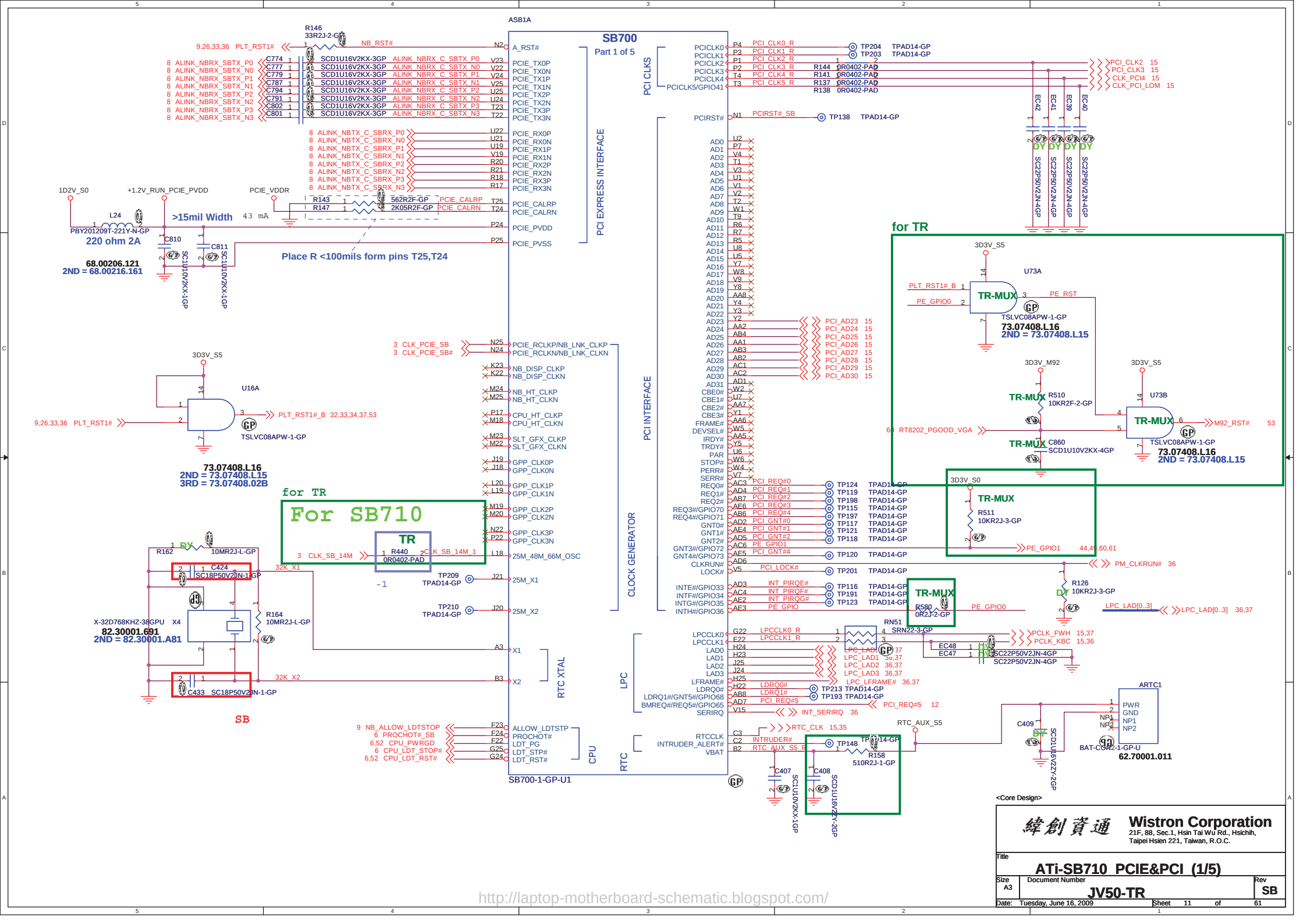
ASB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
for TR
For SB710
TR
SB
PCIRST# SB
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
TP204 TPAD14-GP
TP203 TPAD14-GP
TP138 TPAD14-GP
R146 33R2J-2-GP
NB_RST#
PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U16V2KX-3GP
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L24
PBY201209T-221Y-N-GP
220 ohm 2A
>15mil Width
43 mA
68.00206.121
2ND = 68.00216.161
R143 562R2F-GP
R147 2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
C810
C811
SC1U10V2KX-1GP
3D3V_S5
U16A
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
CLK_PCIE_SB
CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
CLK_SB_14M
R440 0R0402-PAD
25M_48M_66M_OSC
25M_X1
25M_X2
TP209 TPAD14-GP
TP210 TPAD14-GP
R162 10MR2J-L-GP
C424 SC18P50V2JN-1GP
C433 SC18P50V2JN-1-GP
R164 10MR2J-L-GP
X-32D768KHZ-38GPU X4
82.30001.691
2ND = 82.30001.A81
32K_X1
32K_X2
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_PVDD
PCIE_PVSS
PCI_AD23 15
PCI_AD24 15
PCI_AD25 15
PCI_AD26 15
PCI_AD27 15
PCI_AD28 15
PCI_AD29 15
PCI_AD30 15
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#4
PE_GPIO1
PCI_LOCK#
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
PE_GPIO
INT_SERIRQ 36
LPCCLK0_R
LPCCLK1_R
LPC_LAD0 36,37
LPC_LAD1 36,37
LPC_LAD2 36,37
LPC_LAD3 36,37
LPC_LFRAME# 36,37
LDRQ0#
LDRQ1#
TP213 TPAD14-GP
TP193 TPAD14-GP
PCI_REQ#5 12
RTC_CLK 15,35
INTRUDER#
RTC_AUX_S5
TP148 TPAD14-GP
R158 510R2J-1-GP
C407 SC1U10V2KX-1GP
C408 SCD1U16V2ZY-2GP
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
9 NB_ALLOW_LDTSTOP
6 PROCHOT#_SB
6,52 CPU_PWRGD
6 CPU_LDT_STOP#
6,52 CPU_LDT_RST#
PCI_CLK2 15
PCI_CLK3 15
CLK_PCI4 15
CLK_PCI_LOM 15
EC42
EC41
EC39
EC40
SC22P50V2JN-4GP
U73A
TR-MUX
PLT_RST1#_B
PE_GPIO0
PE_RST
73.07408.L16
2ND = 73.07408.L15
3D3V_M92
U73B
R510 10KR2F-2-GP
RT8202_PGOOD_VGA
M92_RST# 53
C860 SCD1U10V2KX-4GP
3D3V_S0
R511 10KR2J-3-GP
PE_GPIO1 44,47,60,61
PM_CLKRUN# 36
R126 10KR2J-3-GP
LPC_LAD[0..3]
LPC_LAD[0..3] 36,37
R580 0R2J-2-GP
RN51 SRN22-3-GP
PCLK_FWH 15,37
PCLK_KBC 15,36
EC48
EC47
SC22P50V2JN-4GP
ARTC1
PWR
GND
NP1
NP2
C409
SCD1U16V2ZY-2GP
BAT-CON2-1-GP-U
62.70001.011
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 PCIE&PCI (1/5)
Size A3
Document Number
JV50-TR
Rev SB
Date: Tuesday, June 16, 2009
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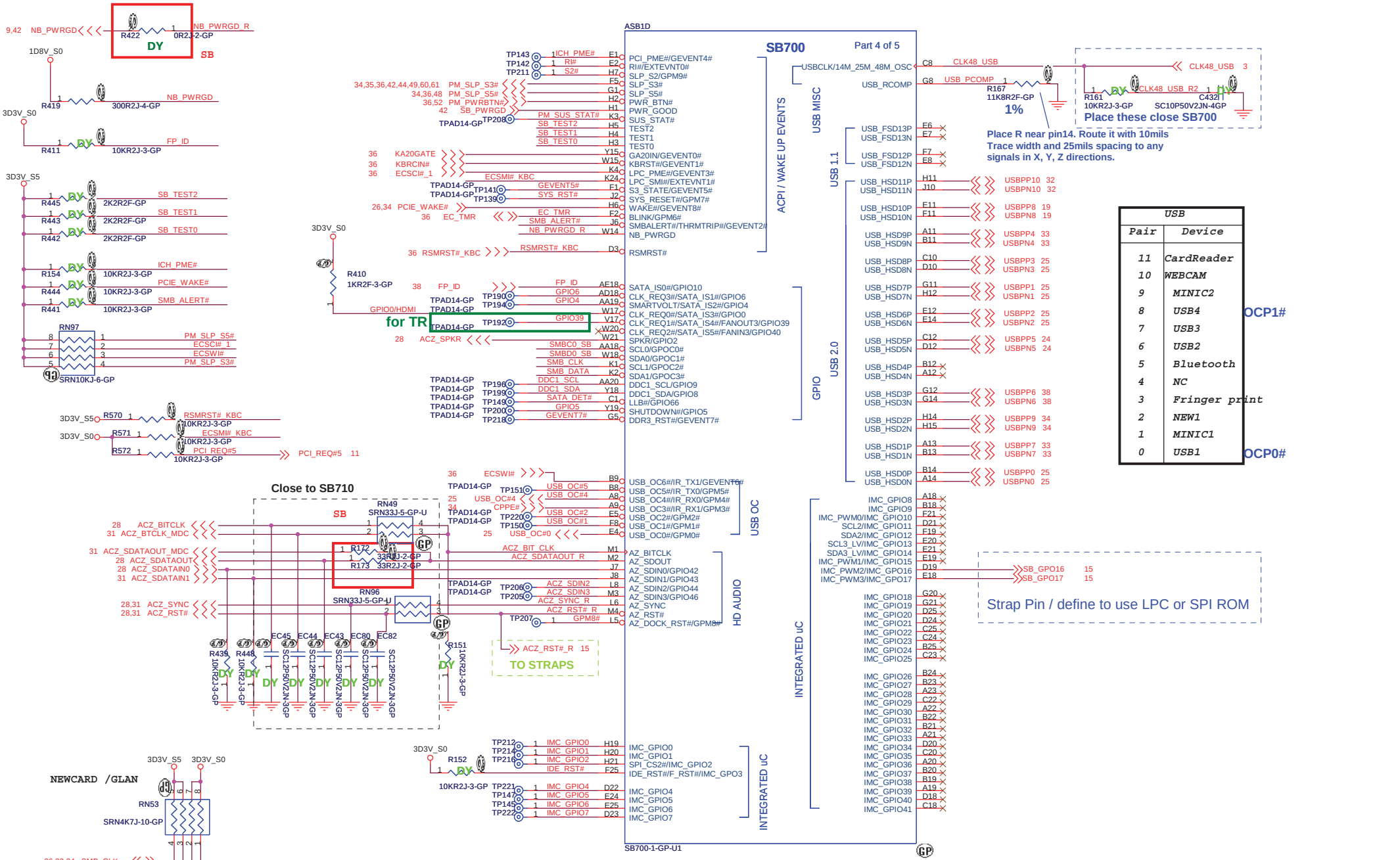

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB710

SATA HDD
SATA ODD

SB700
Part 2 of 5

SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR

SB700-1-GP-U1

Very Close to SB710

1ST 82.30020.851
2ND = 82.30020.791
SB

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

<Core Design>

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Title: ATi-SB710 SATA-IDE (3/5)
Size: A3
Document Number: JV50-TR
Rev: SB
Date: Tuesday, June 16, 2009
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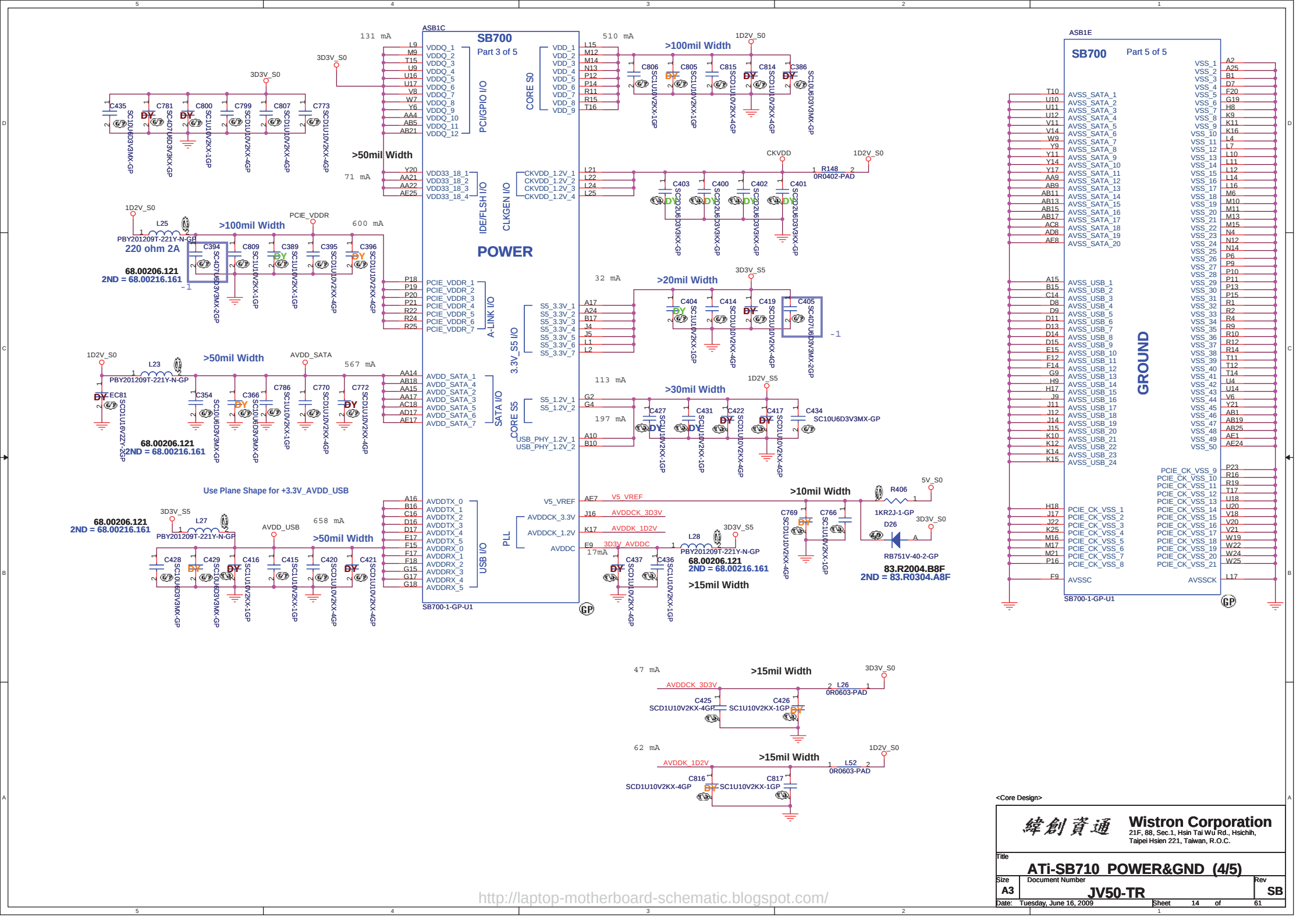

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 POWER&GND (4/5)

Size: A3 | Document Number: JV50-TR | Rev: SB

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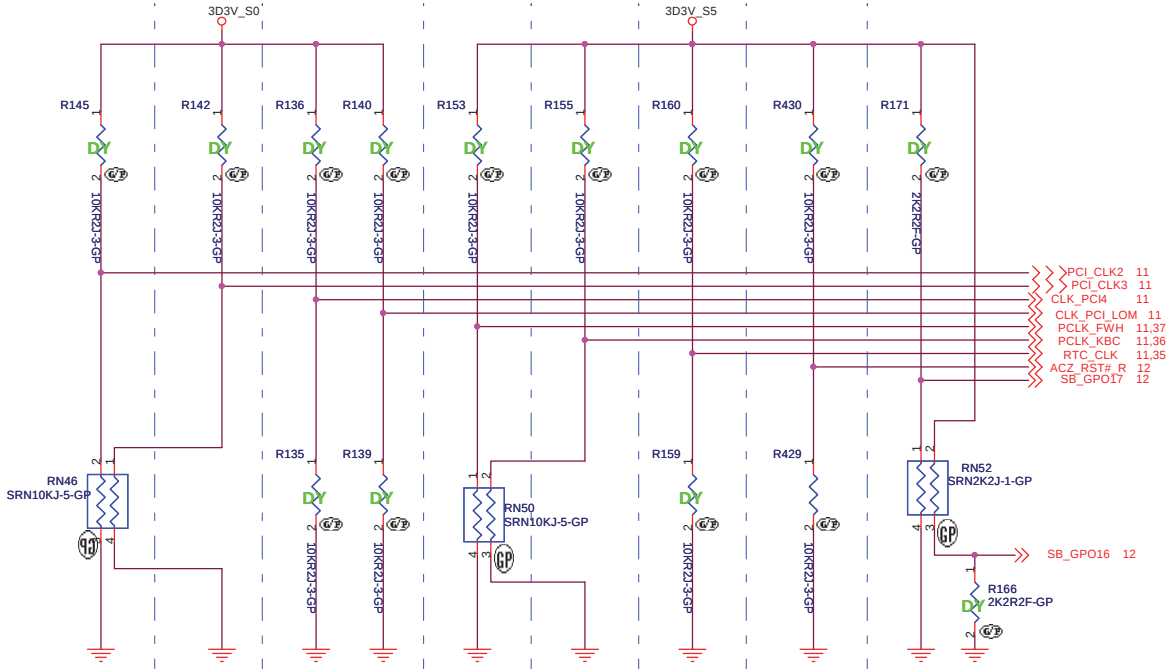
REQUIRED STRAPS

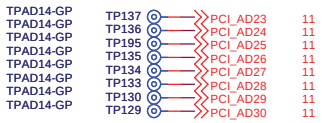
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB710 STRAPPING (5/5)

Size: A3 | Document Number: JV50-TR | Rev: SB

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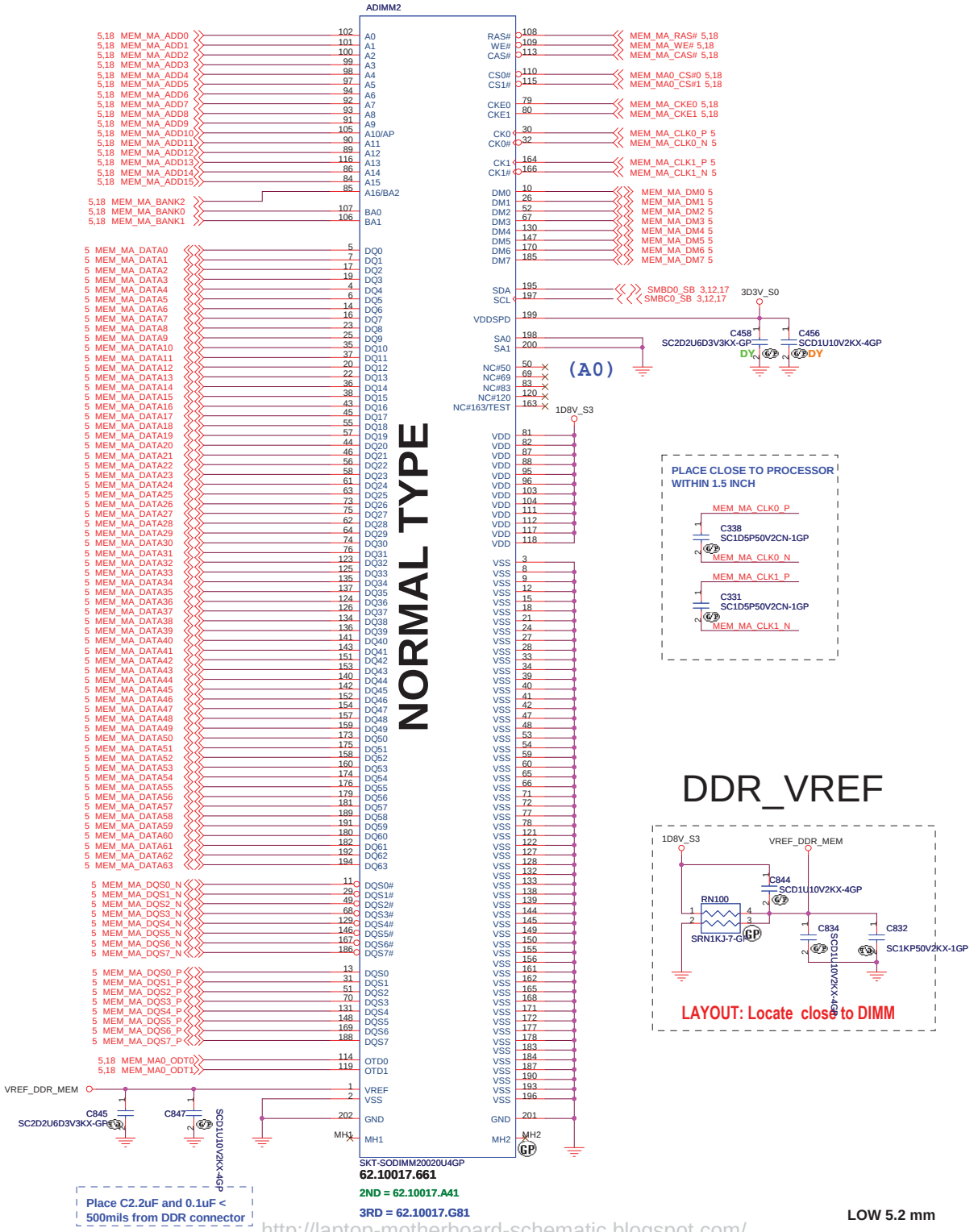

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: JV50-TR | Rev: SB

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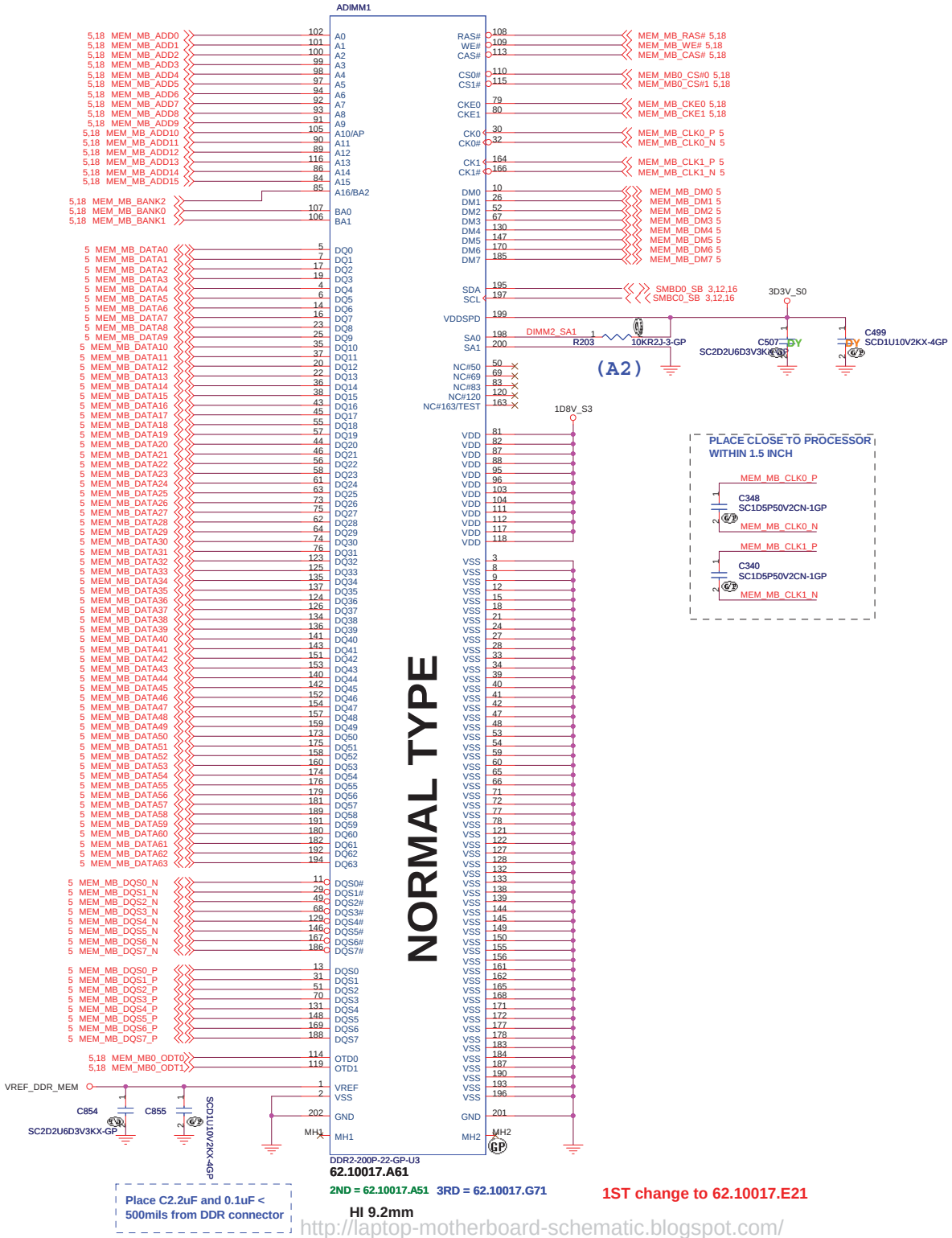

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: JV50-TR | Rev: SB

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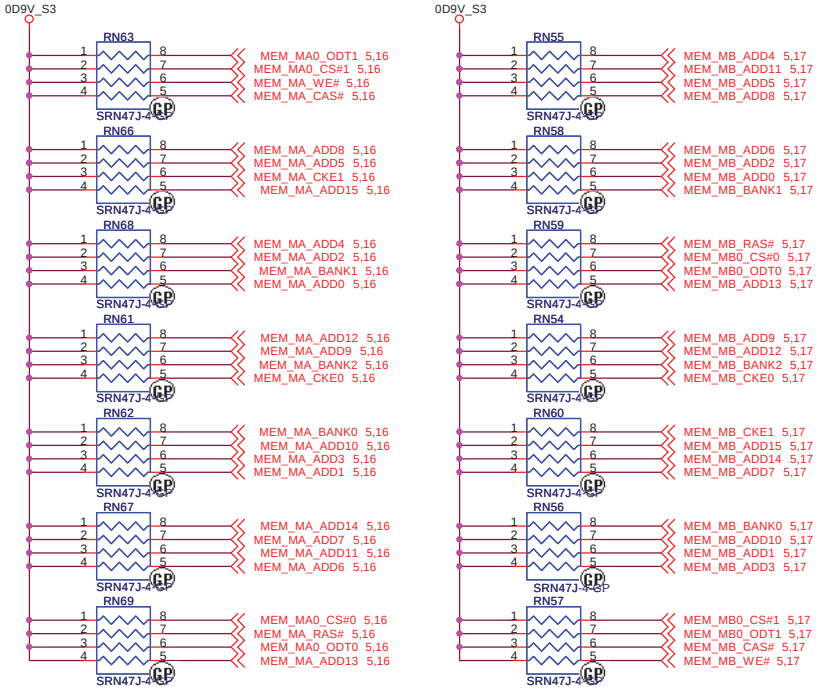
PARALLEL TERMINATION

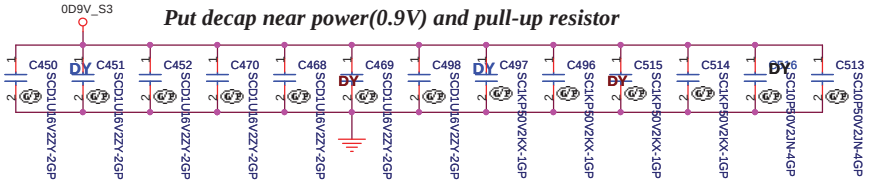
Put decap near power(0.9V) and pull-up resistor



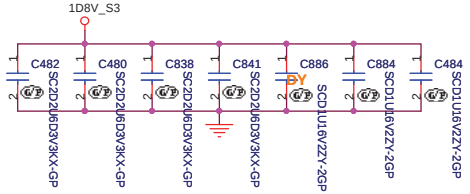
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

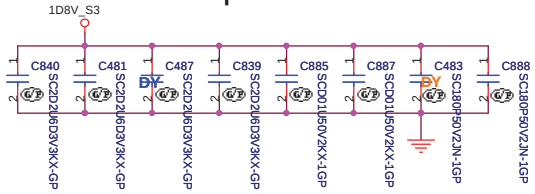


Place these Caps near DM1



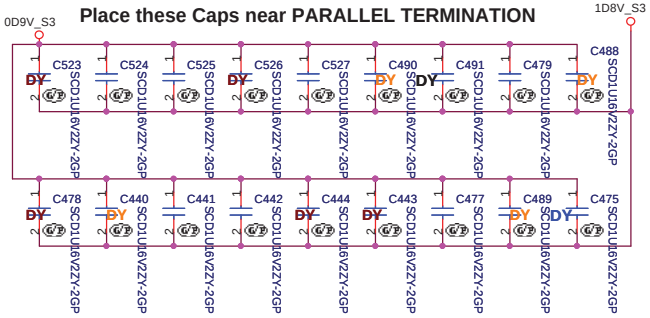
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

緯創資通 **Wistron Corporation**
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Title: **DDR_DAMPING & TERMINATION**

Size	Document Number	Rev
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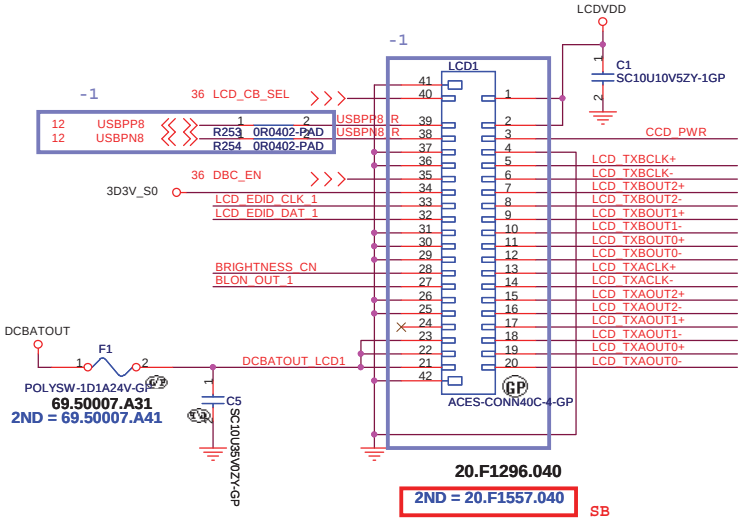
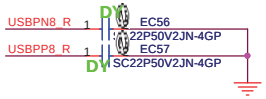
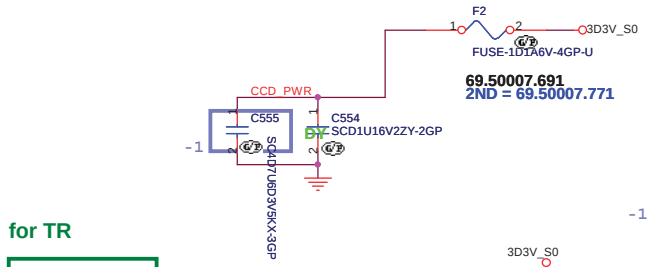
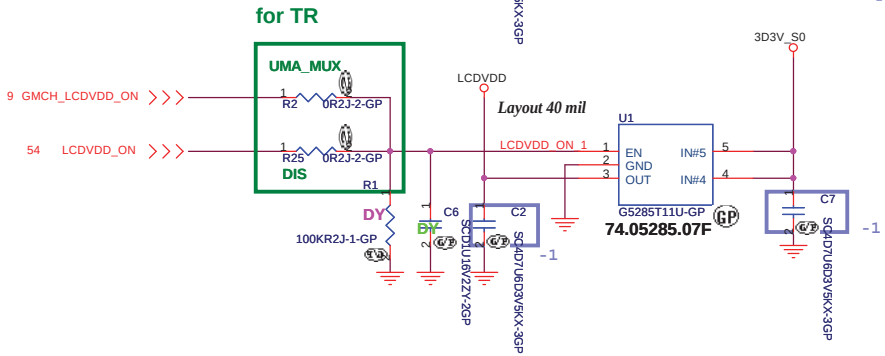
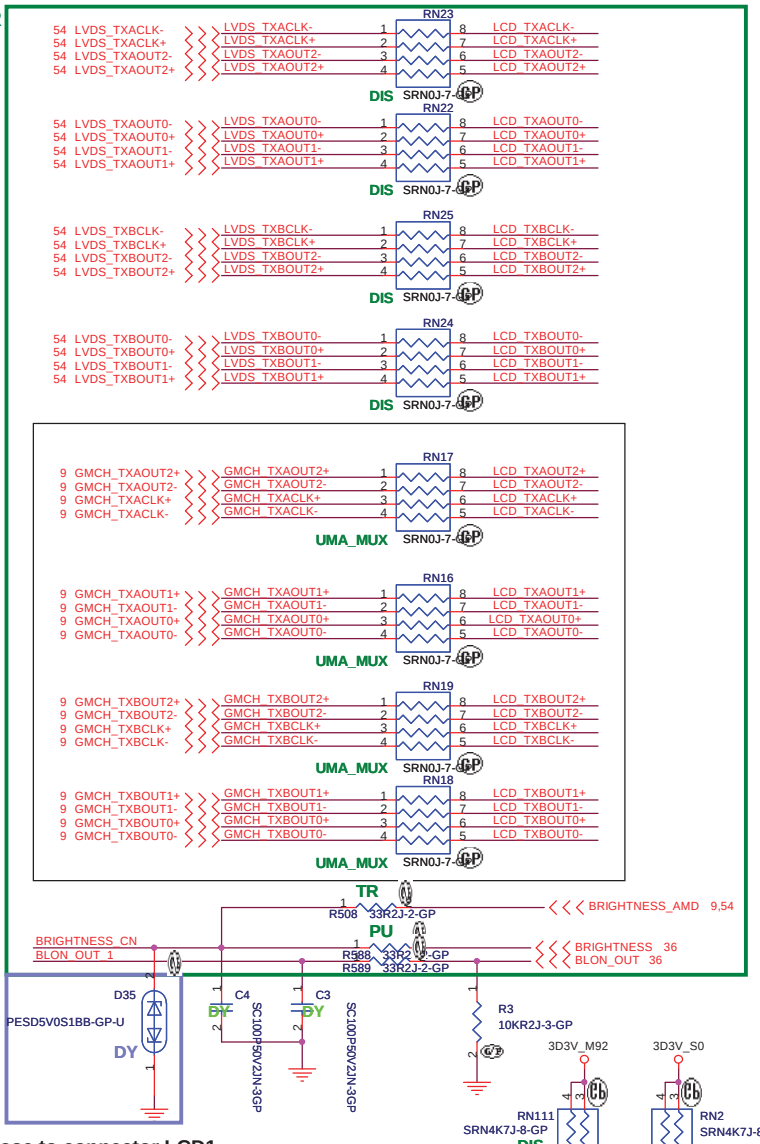
LCD/INVERTER/CCD CONN











Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

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Title: LCD CONN
Size: A3 | Document Number: JV50-TR | Rev: SB
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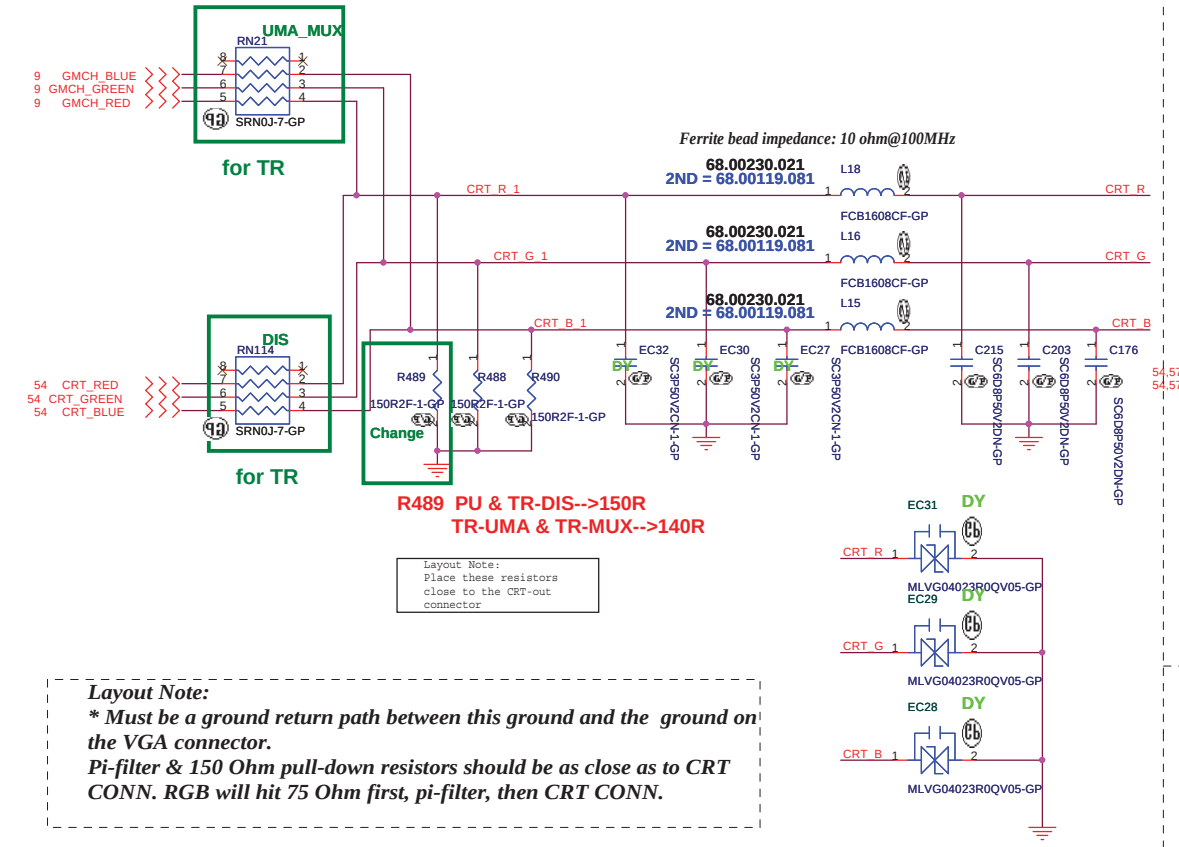

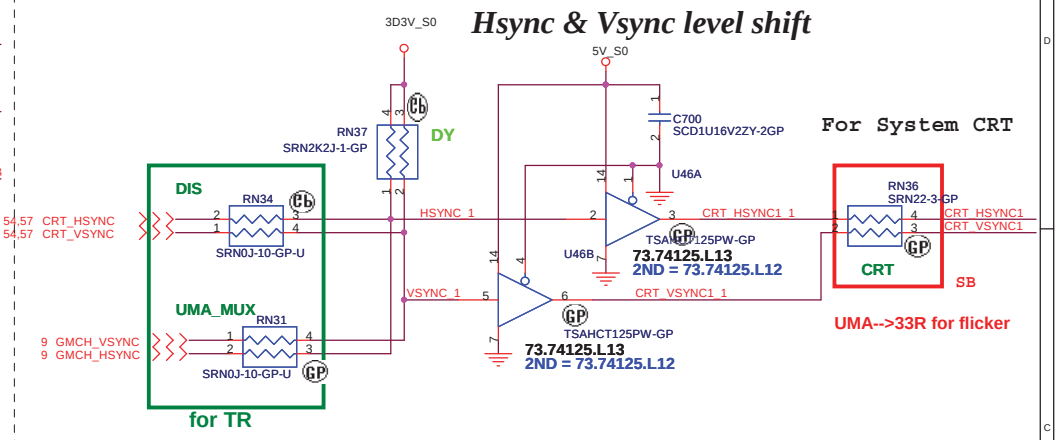

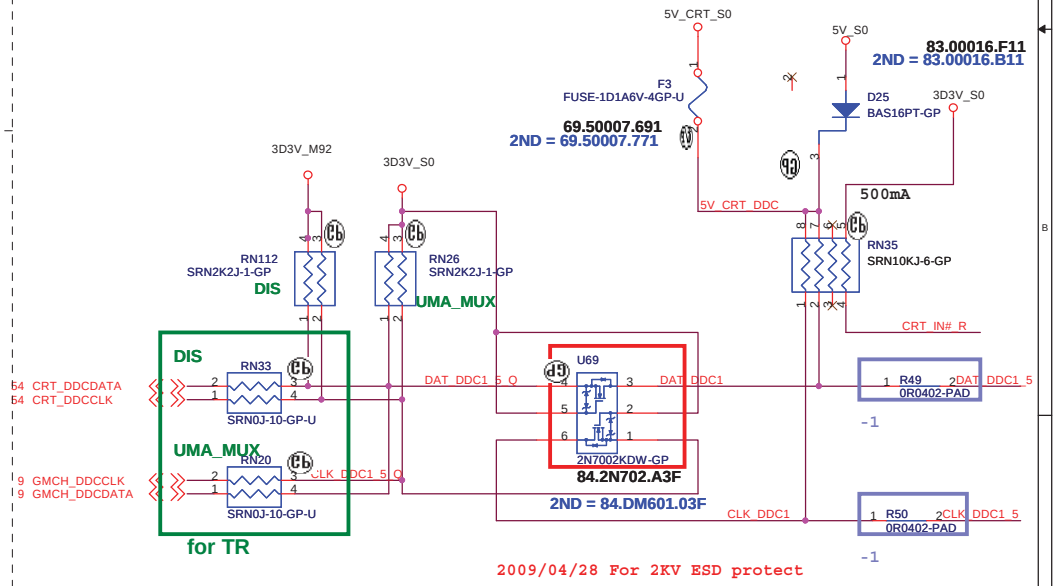

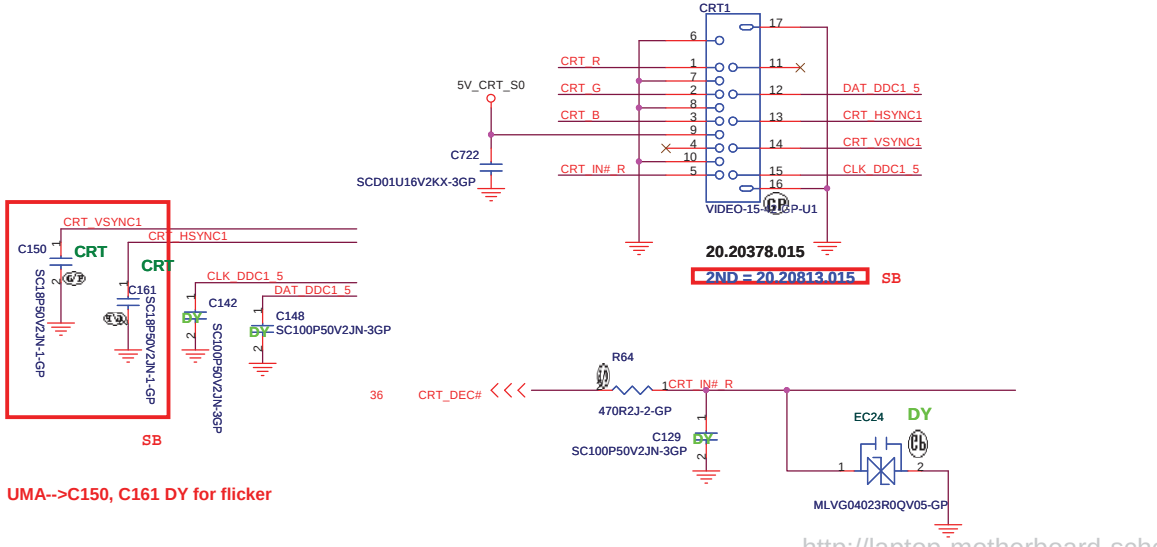

<Core Design>

緯創資通 Wistron Corporation
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Title: CRT Connector

Size	Document Number	Rev
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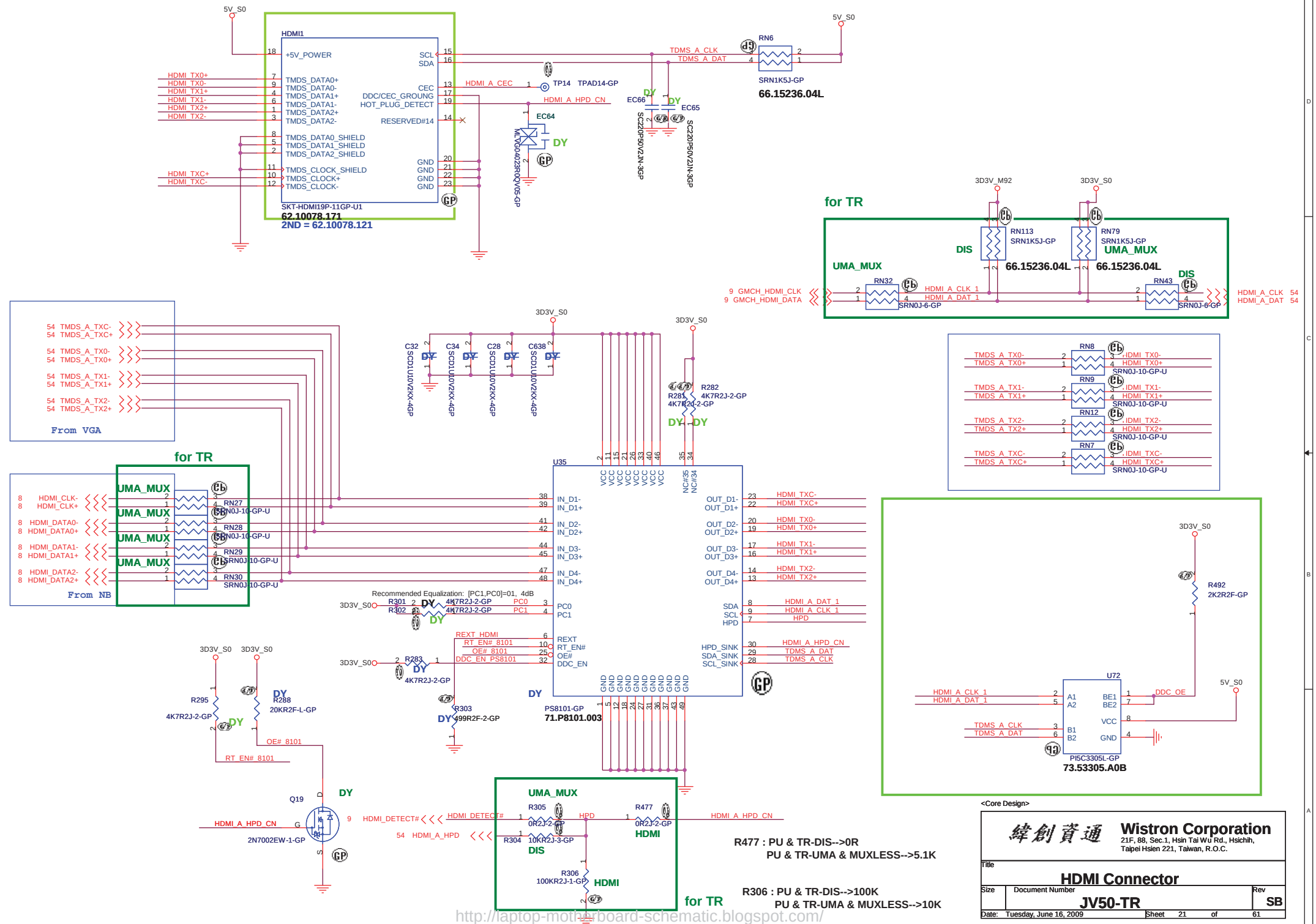
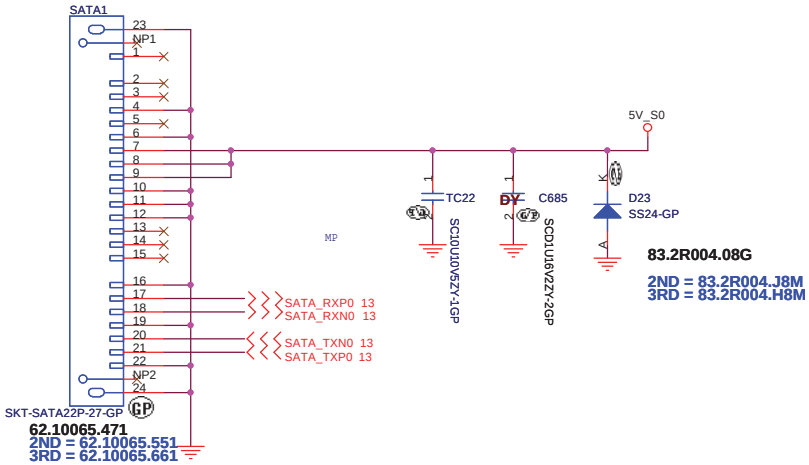
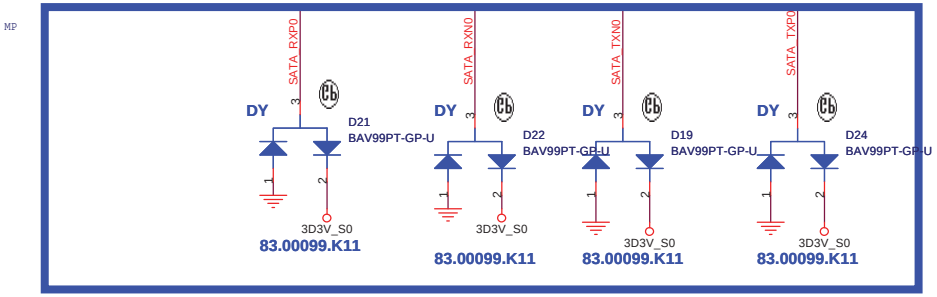


SATA Connector





<Core Design>

緯創資通 Wistron Corporation
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Title: HDD		
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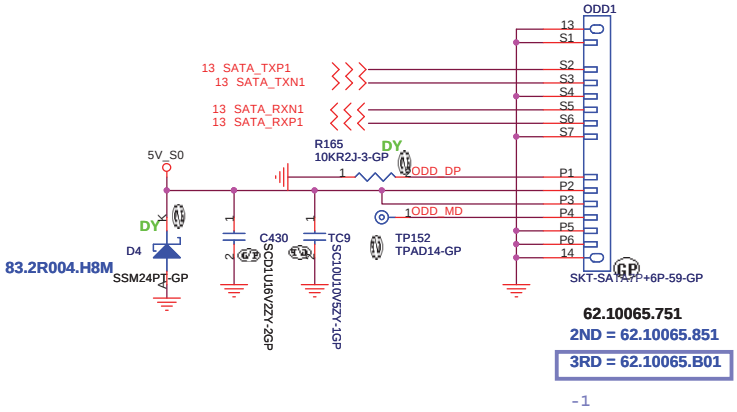
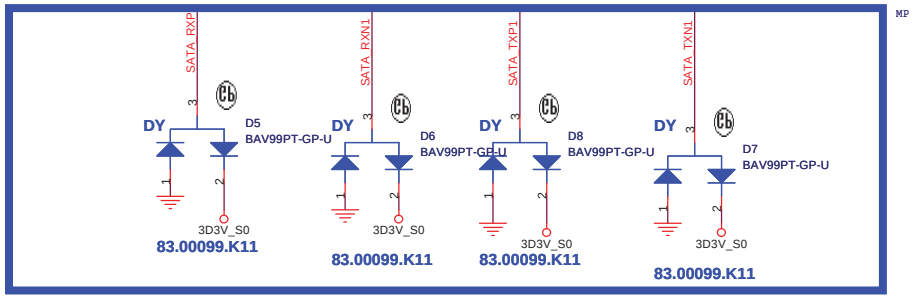
SATA ODD Connector





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ODD

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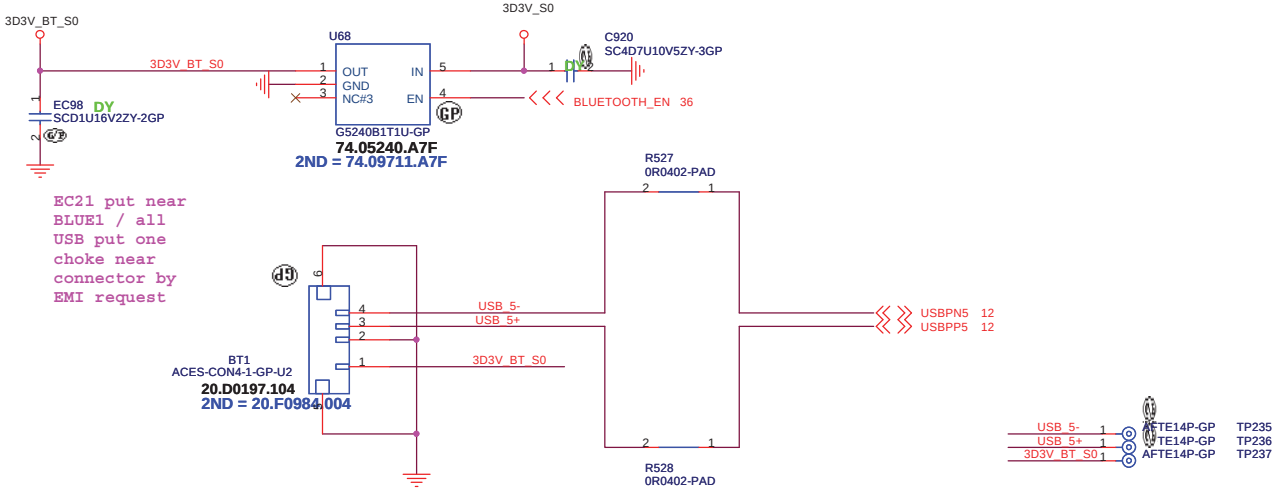
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



緯創資通 Wistron Corporation		
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Title: BLUETOOTH		
Size	Document Number: JV50-TR	Rev: SB
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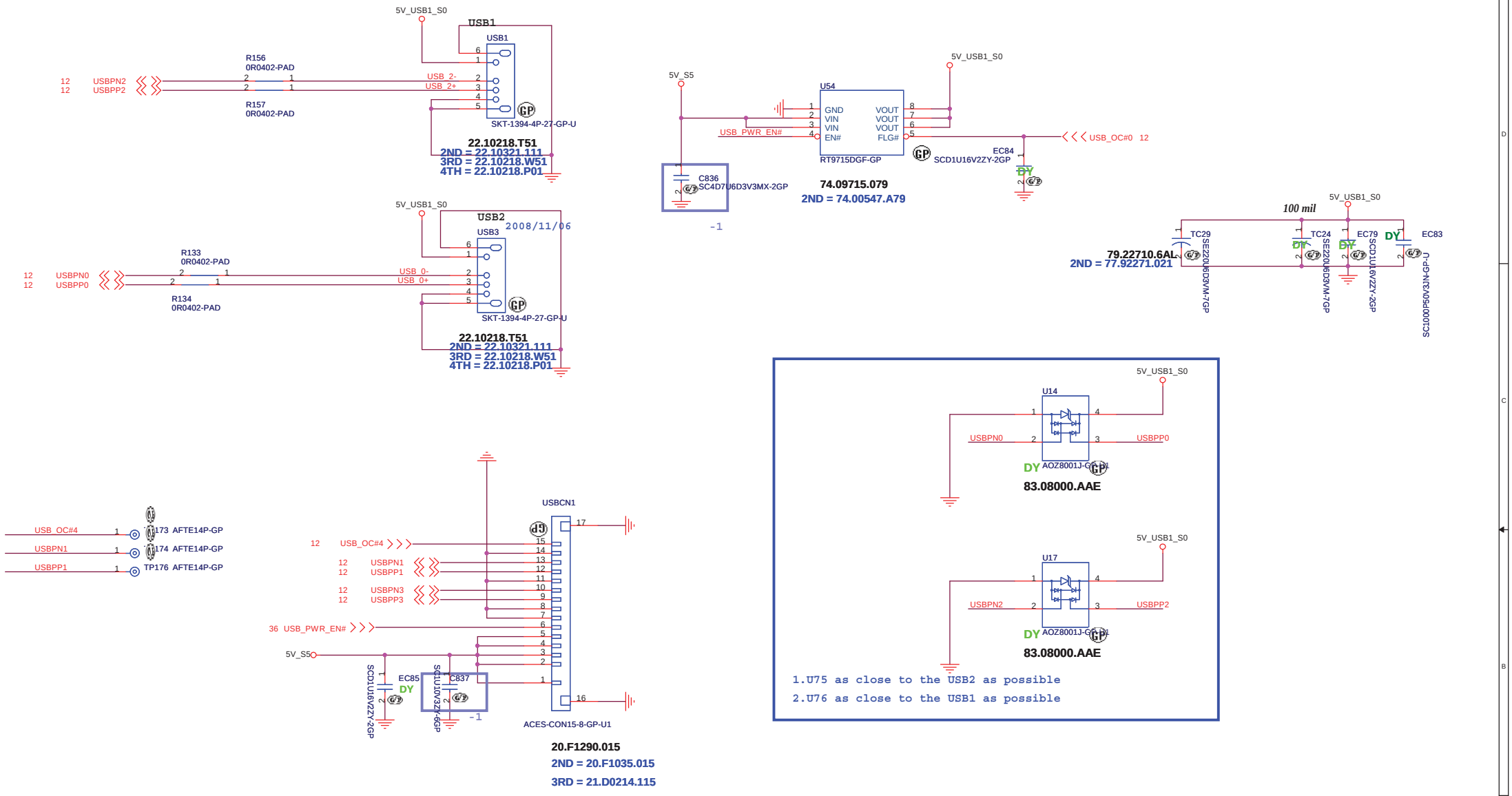

緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**USB**
Size	Document Number: **JV50-TR**
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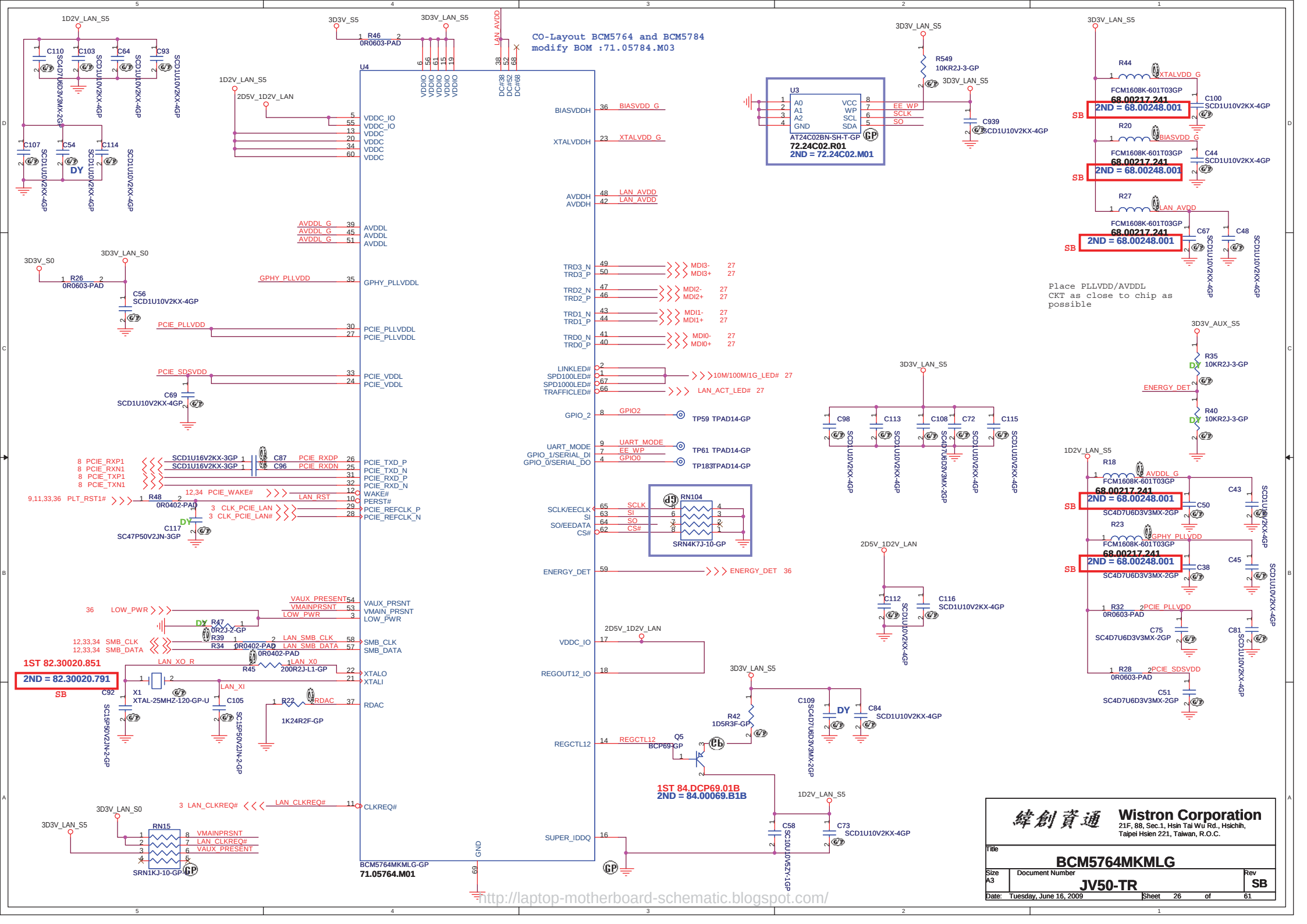
CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.M03
U4
BCM5764MKMLG-GP
71.05764.M01
U3
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
1ST 82.30020.851
2ND = 82.30020.791
SB
1ST 84.DCP69.01B
2ND = 84.00069.B1B
Place PLLVDD/AVDDL
CKT as close to chip as
possible
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size
A3
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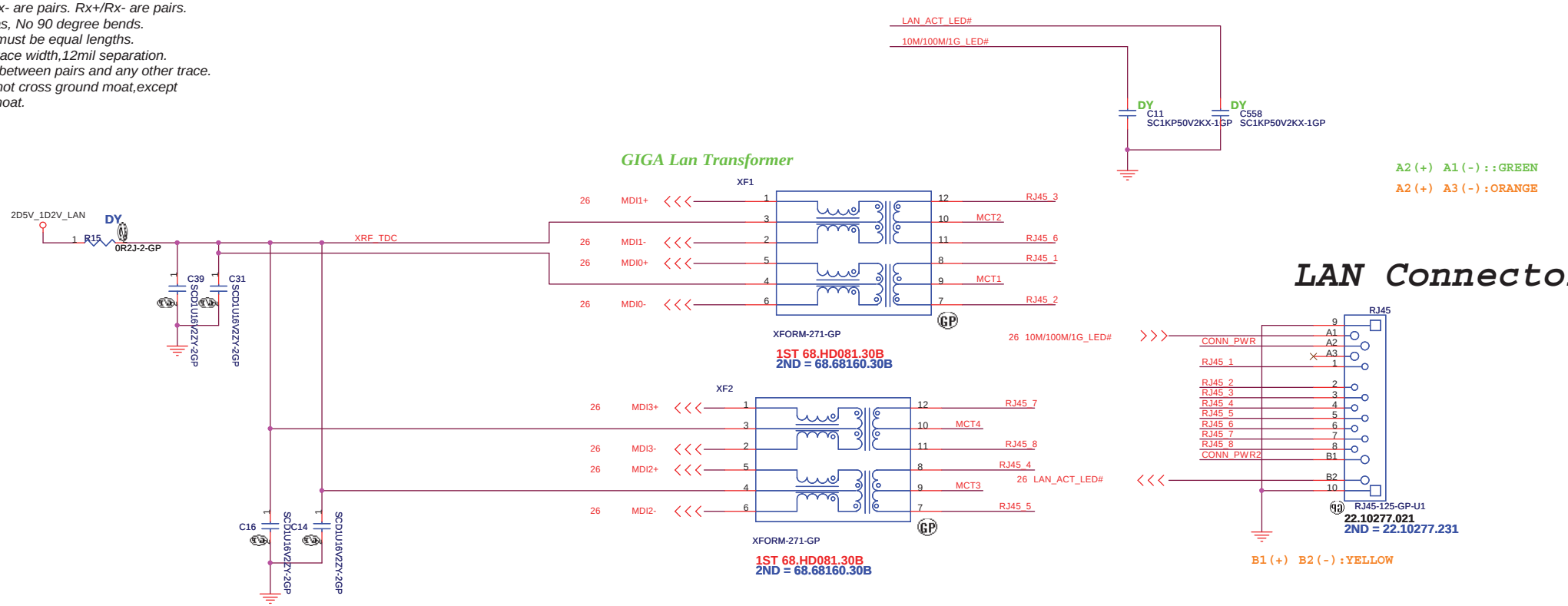
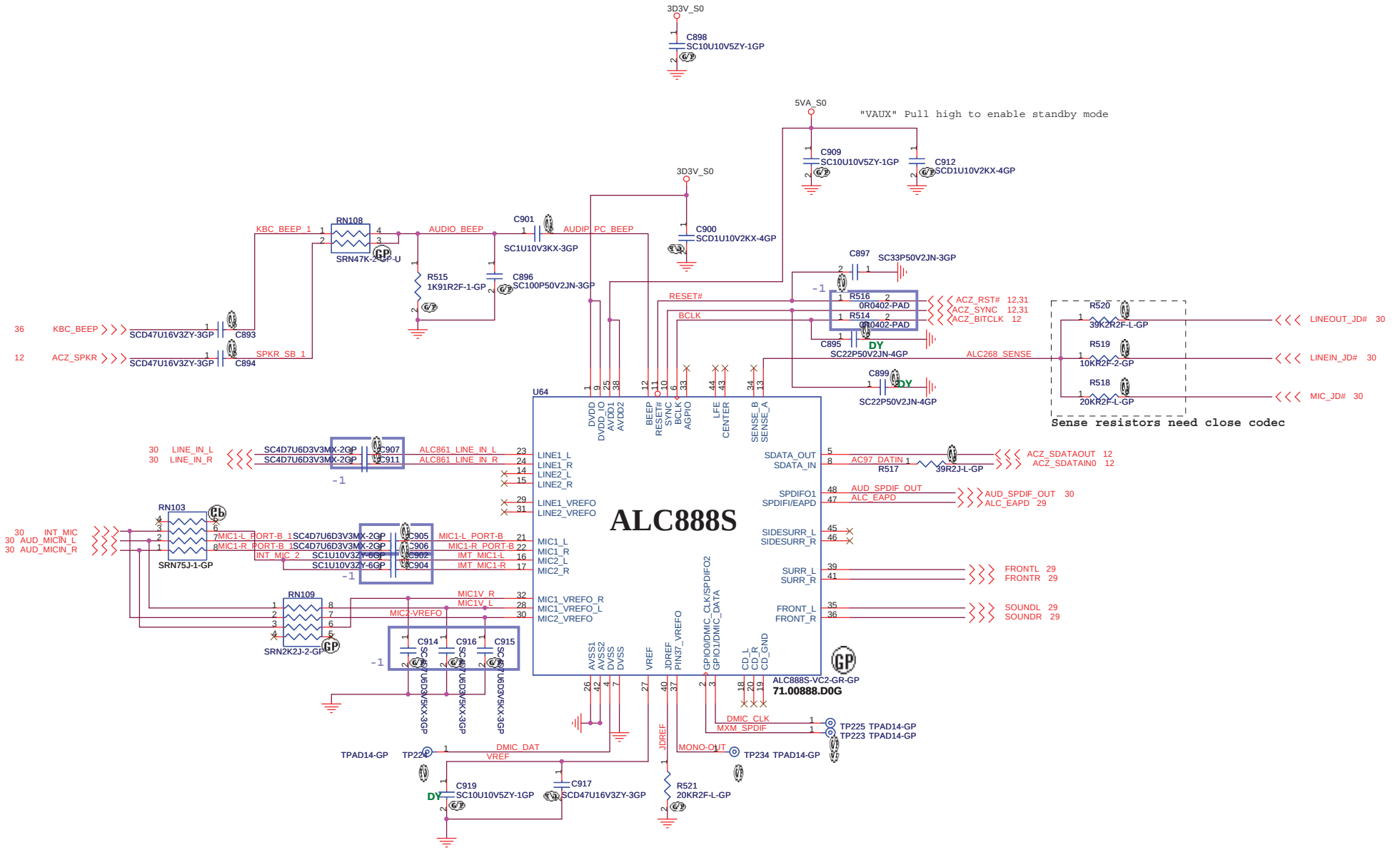
http://laptop-motherboard-schematic.blogspot.com/

LAN Connector

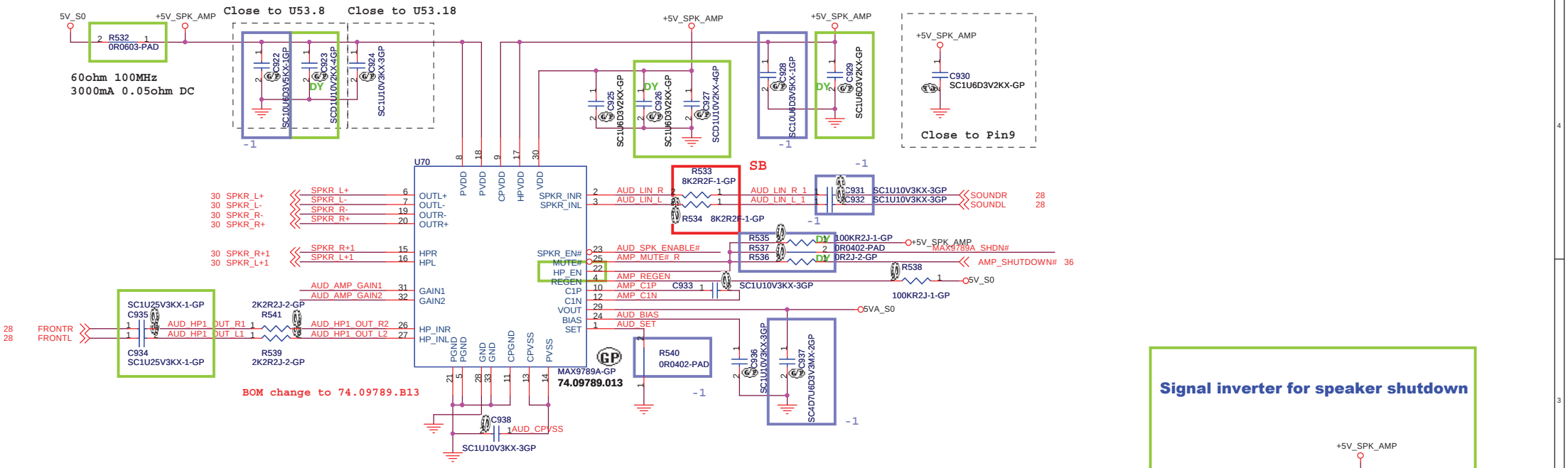
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

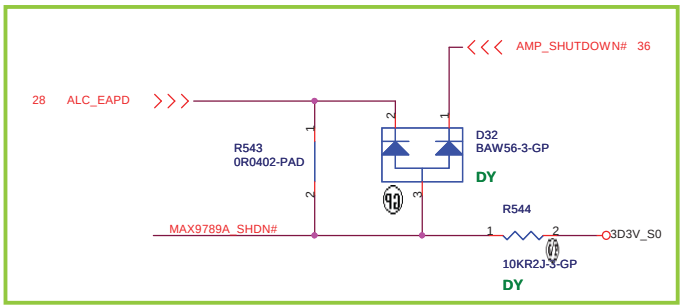


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **LAN CONN**		
Size: A3	Document Number: **JV50-TR**	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 27 of 61	

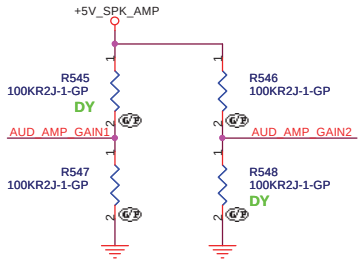


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Azalia codec ALC888**
Size A3	Document Number **JV50-TR** Rev **SB**
Date: Tuesday, June 16, 2009	Sheet 28 of 61



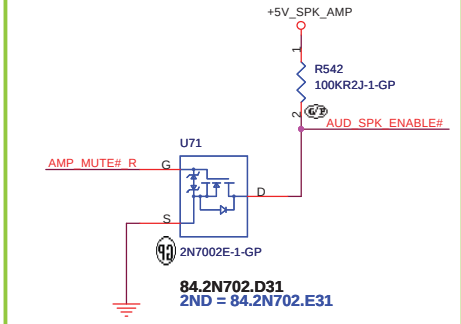


GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP	
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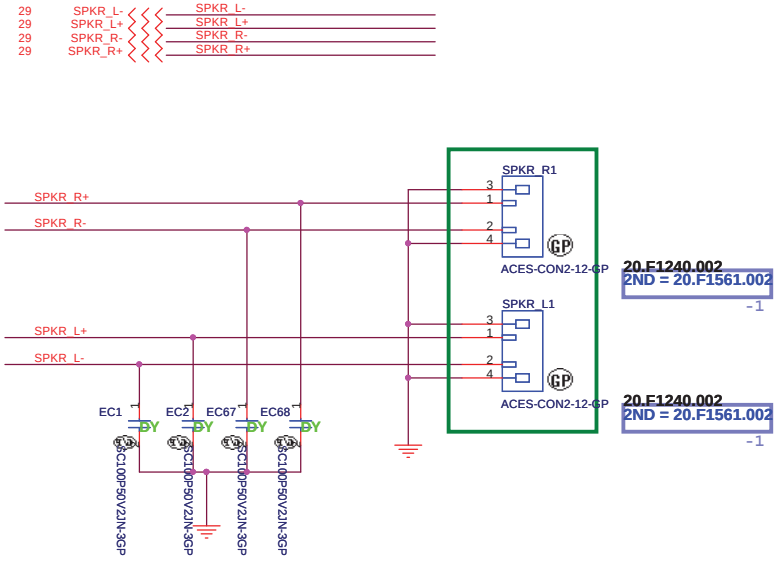
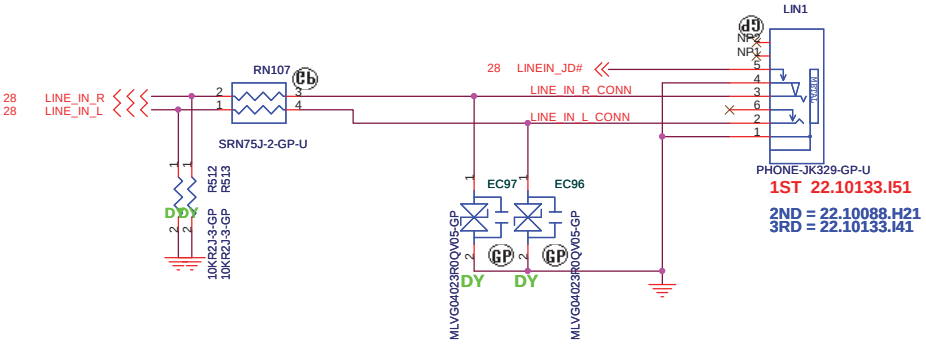
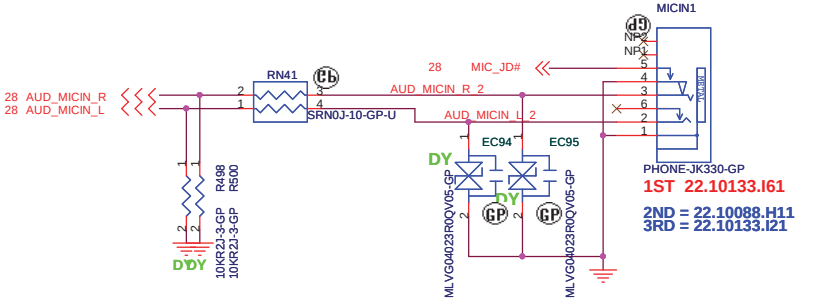
Internal Speaker

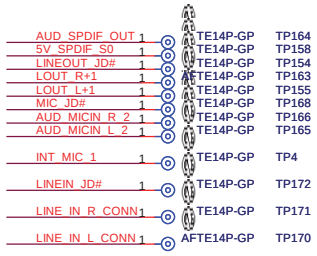


LINE IN

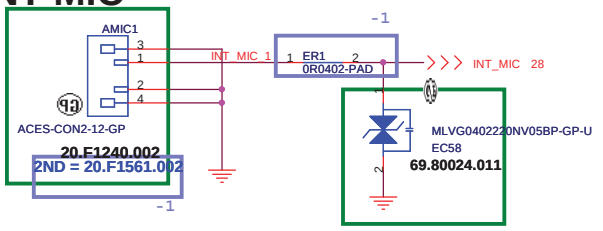


MIC IN

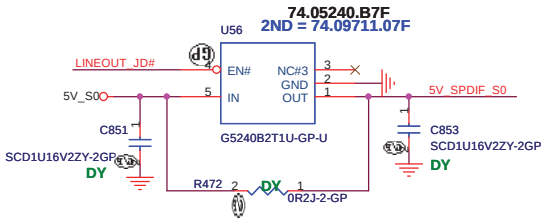


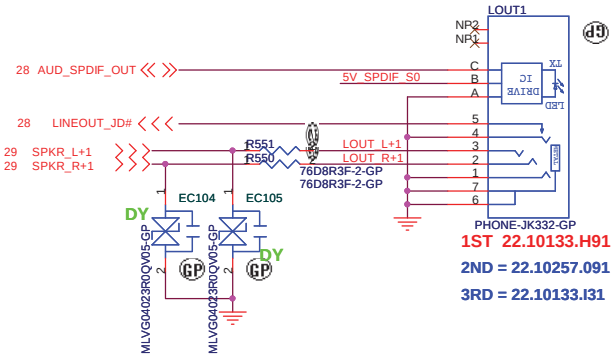


INT MIC



LINE OUT





緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO JACK		
Size	Document Number: JV50-TR	Rev: SB
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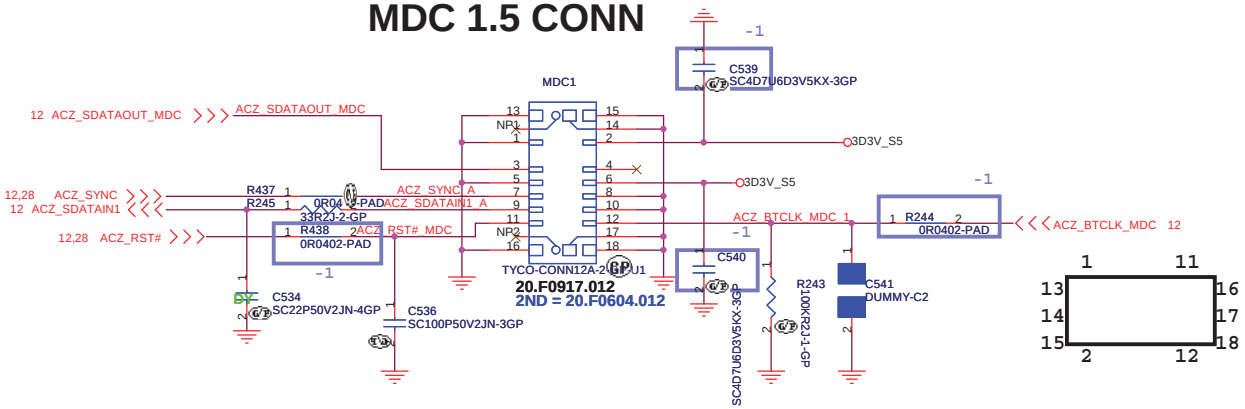
MDC 1.5 CONN



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JV50-TR	Rev: SB
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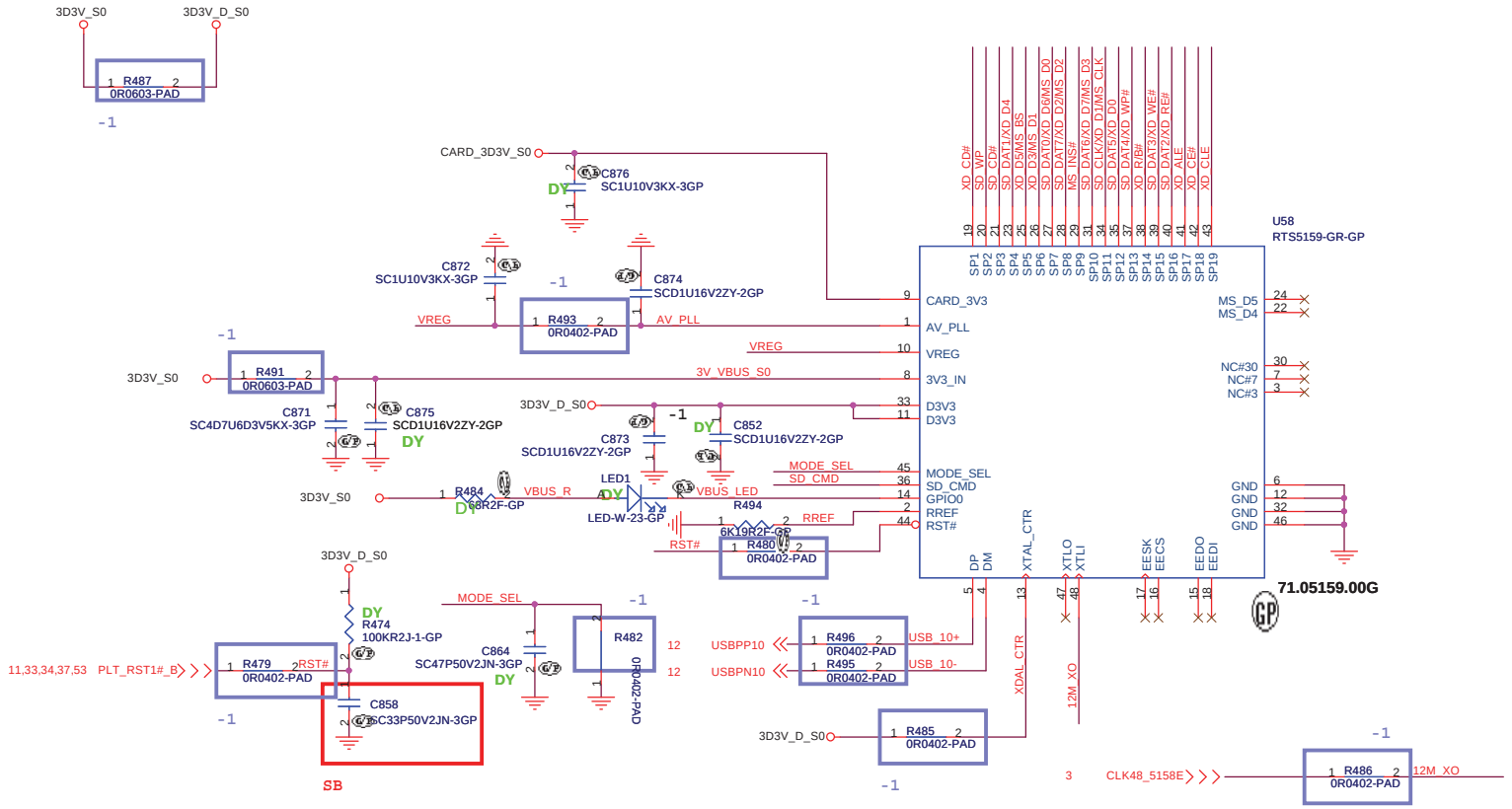
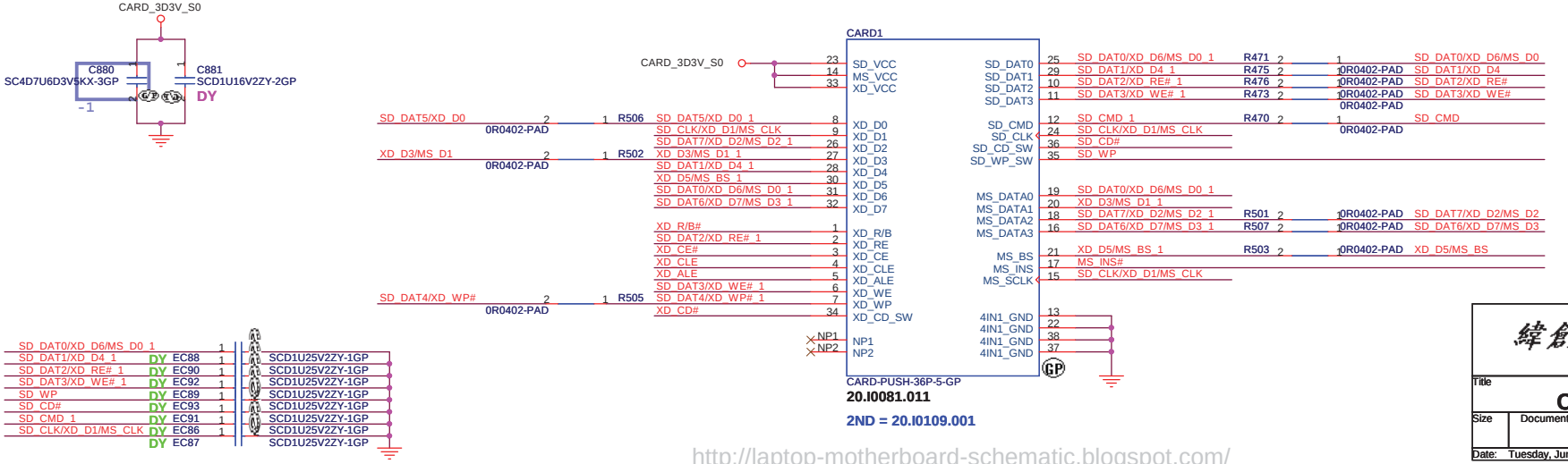


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Company	Wistron Corporation, 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CARDREADER- RTS5159
Size	
Document Number	JV50-TR
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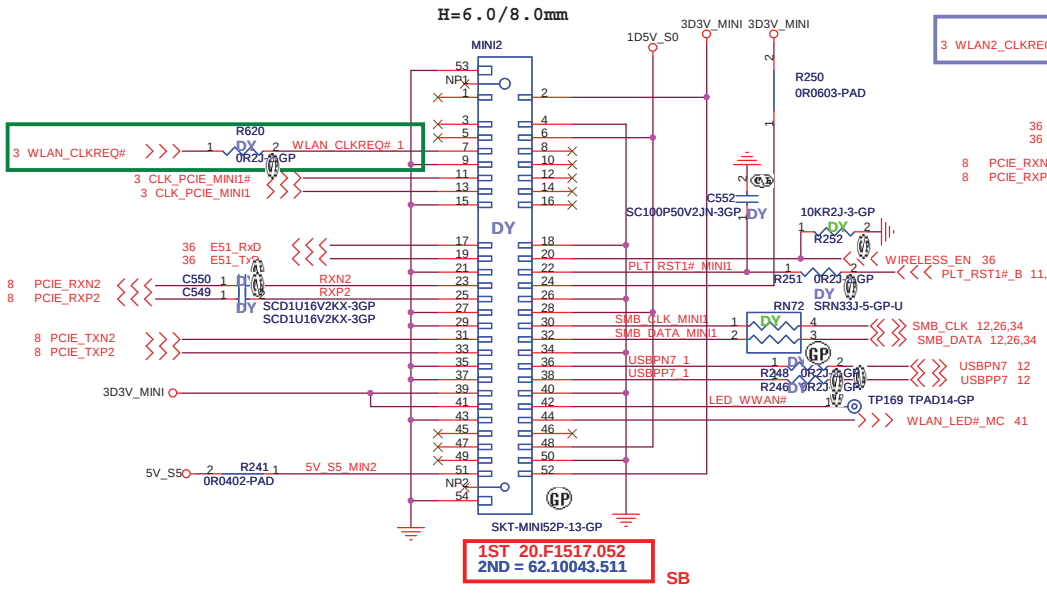
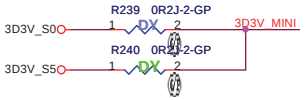
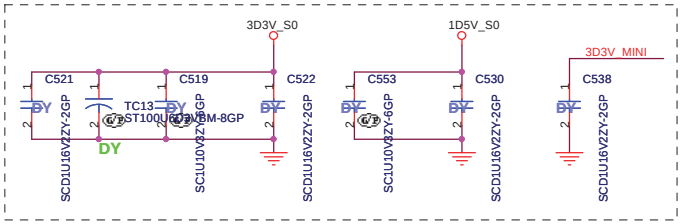
Mini Card Connector(WLAN)

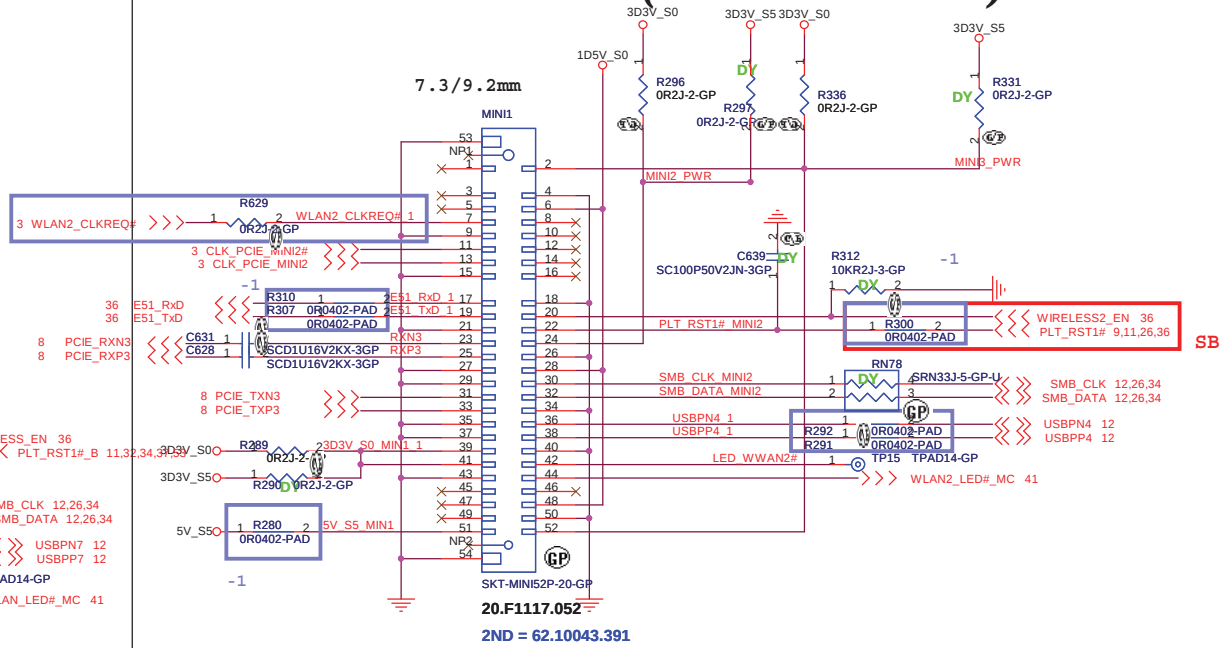




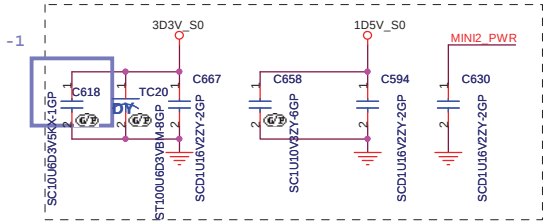
Place near MINI2



Mini Card Connector(Robson2 and 3G)



Place near MINI1



緯創資通 **Wistron Corporation**
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Title	MINI CARD	
Size	Document Number: JV50-TR	Rev: SB
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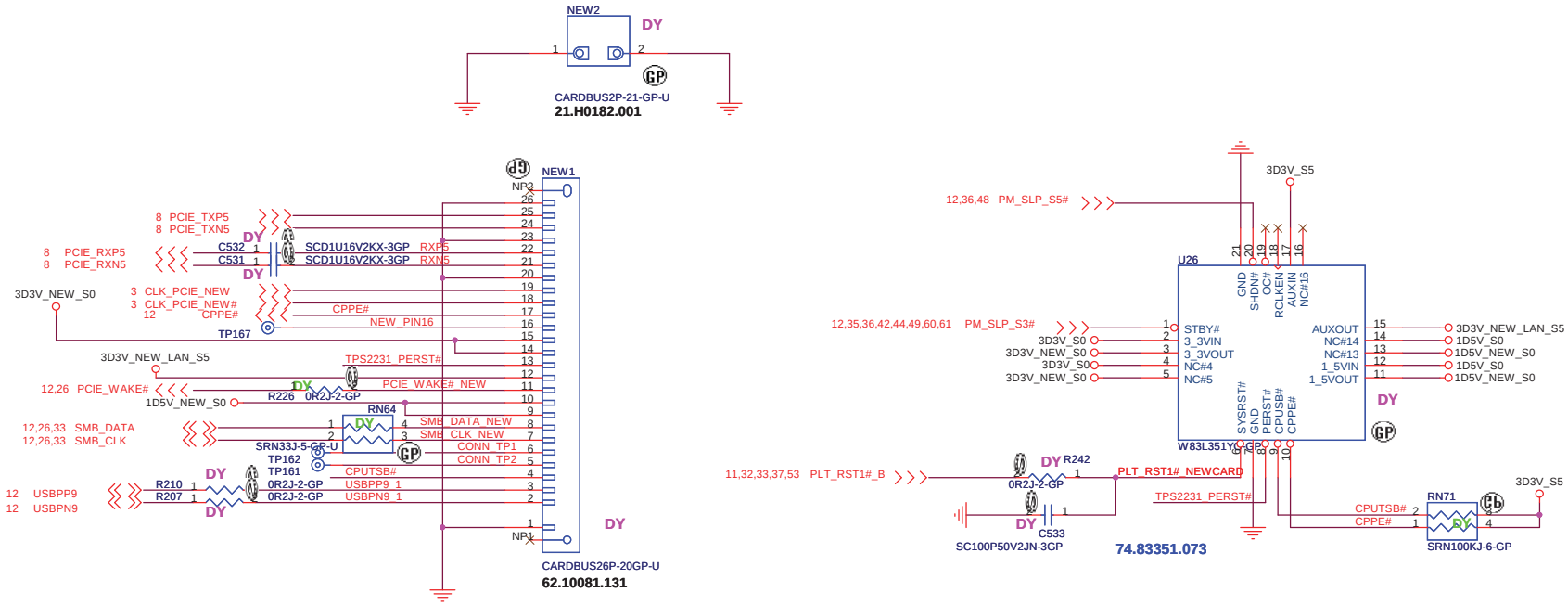
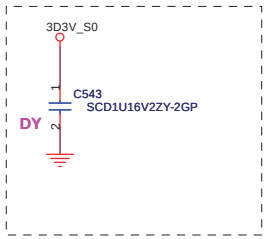
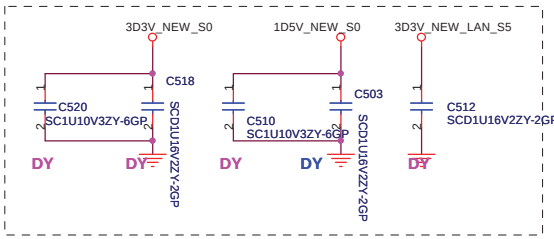
NEWCARD Connector



Place them Near to Chip



Place them Near to Connector



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**NEW CARD**	
Size	Document Number **JV50-TR**	Rev **SB**
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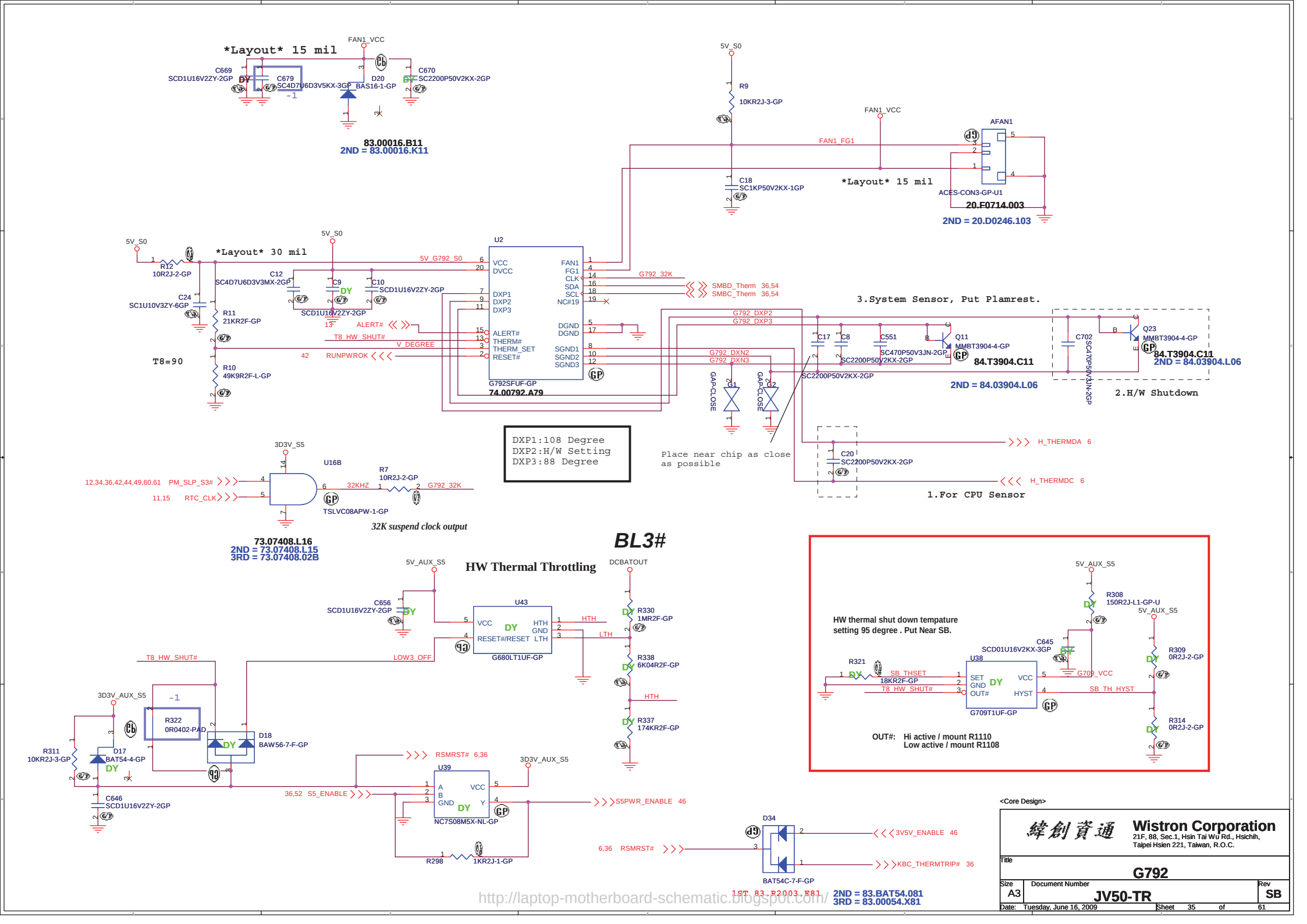

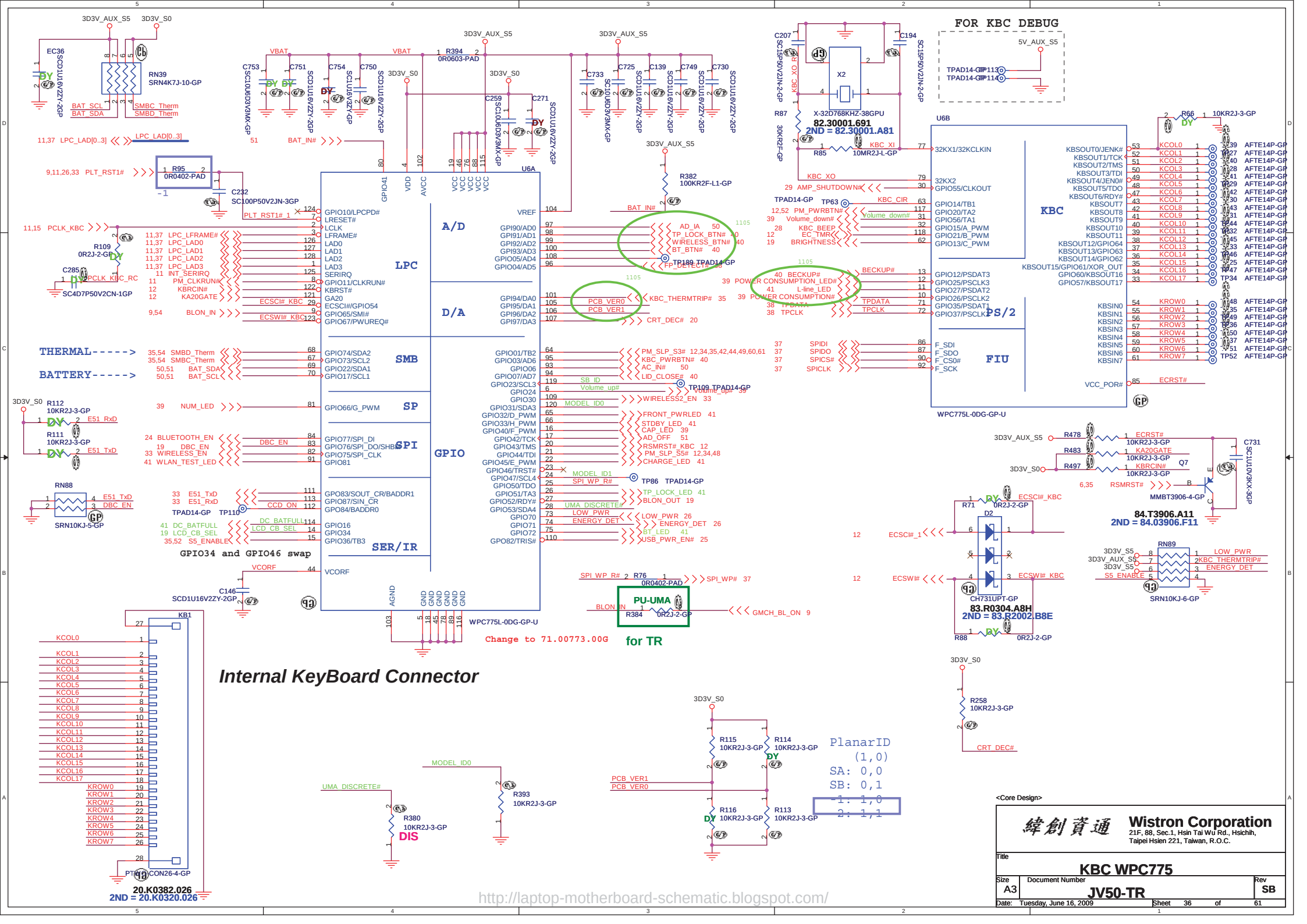
FOR KBC DEBUG
U6A
U6B
WPC775L-0DG-GP-U
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
GPIO34 and GPIO46 swap
PU-UMA
for TR
Change to 71.00773.00G
Internal KeyBoard Connector
84.T3906.A11
2ND = 84.03906.F11
83.R0304.A8H
2ND = 83.R2002.B8E
20.K0382.026
2ND = 20.K0320.026
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
2: 1,1
DIS
Wistron Corporation
KBC WPC775
JV50-TR
Size A3
Rev SB
Date: Tuesday, June 16, 2009
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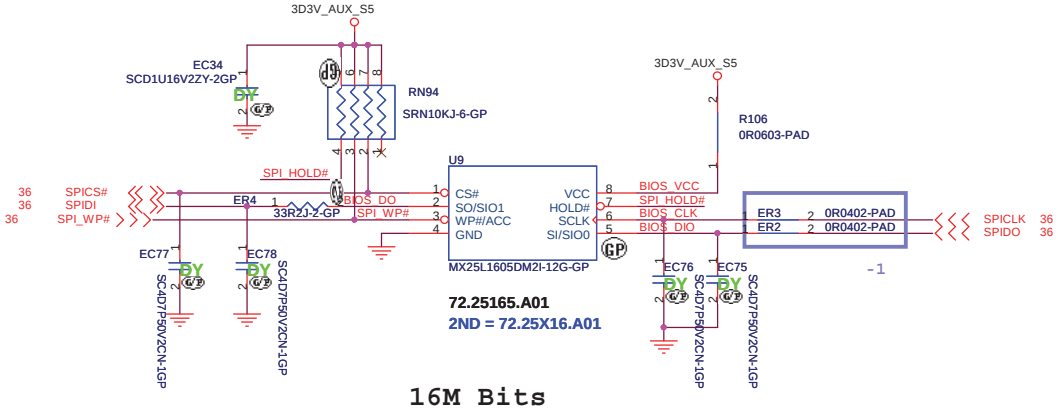
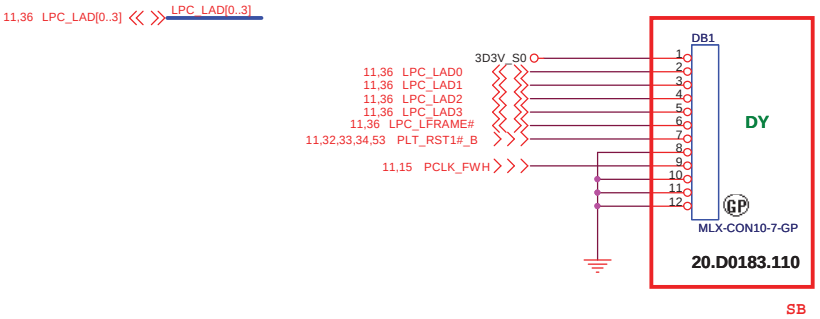
http://laptop-motherboard-schematic.blogspot.com/



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS

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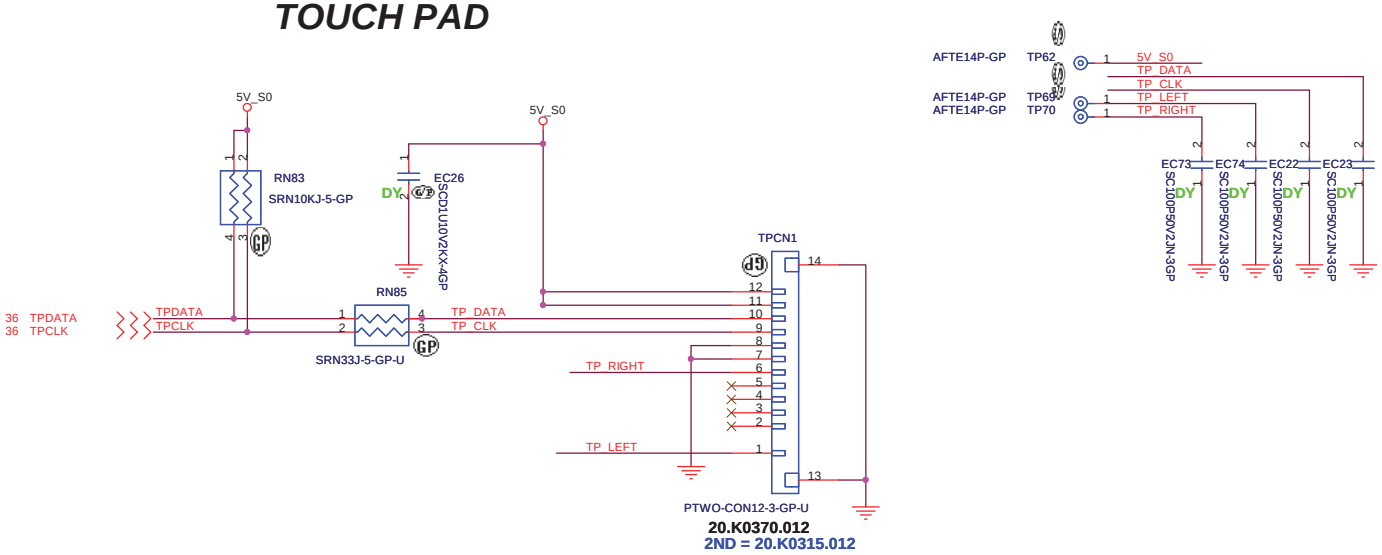
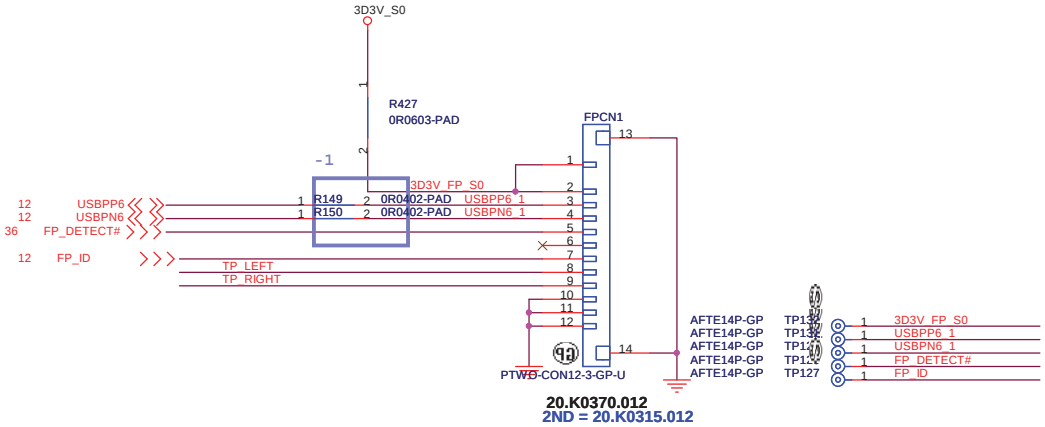
TOUCH PAD



Finger printer



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD/Finger printer

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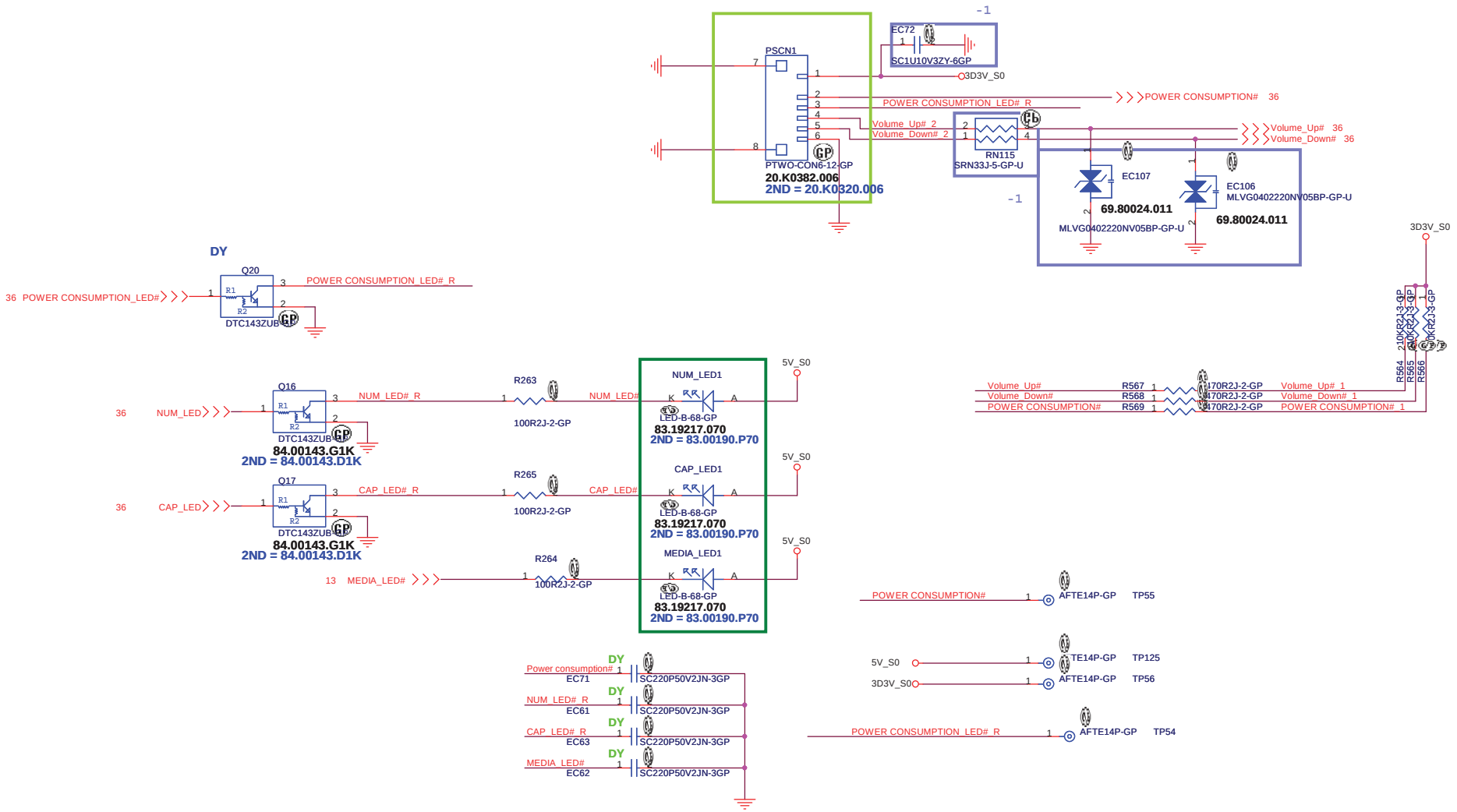

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAUNCH BOARD	
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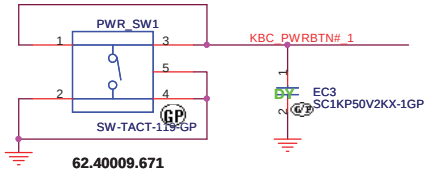
Cover Up Switch

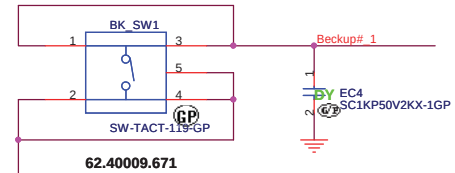
Power Button



62.40009.671

2ND = 62.40012.101

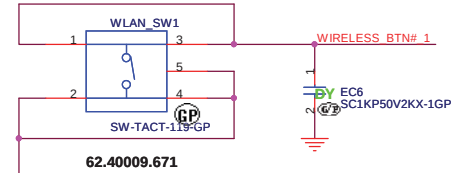
Beckup Button



62.40009.671

2ND = 62.40012.101

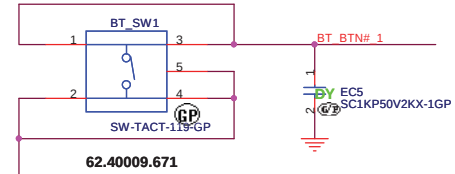
WIRELESS Button



62.40009.671

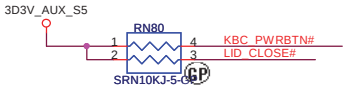
2ND = 62.40012.101

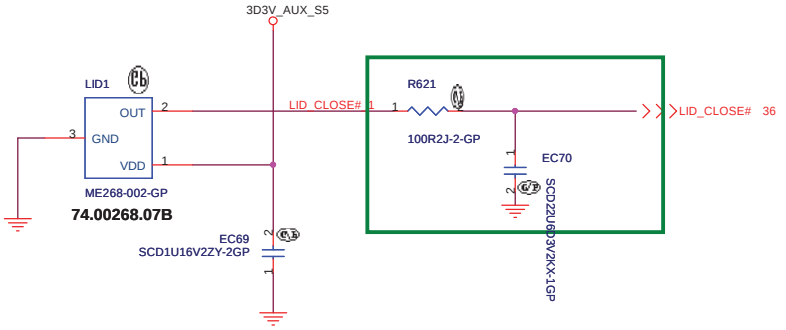
BT/3G Button

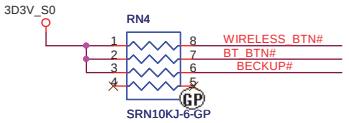


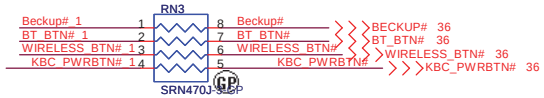
62.40009.671

2ND = 62.40012.101

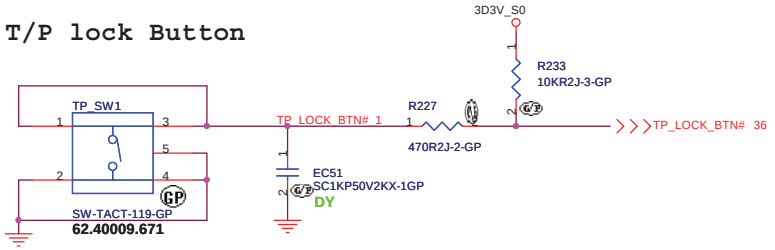








T/P lock Button



62.40009.671

2ND = 62.40012.101

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
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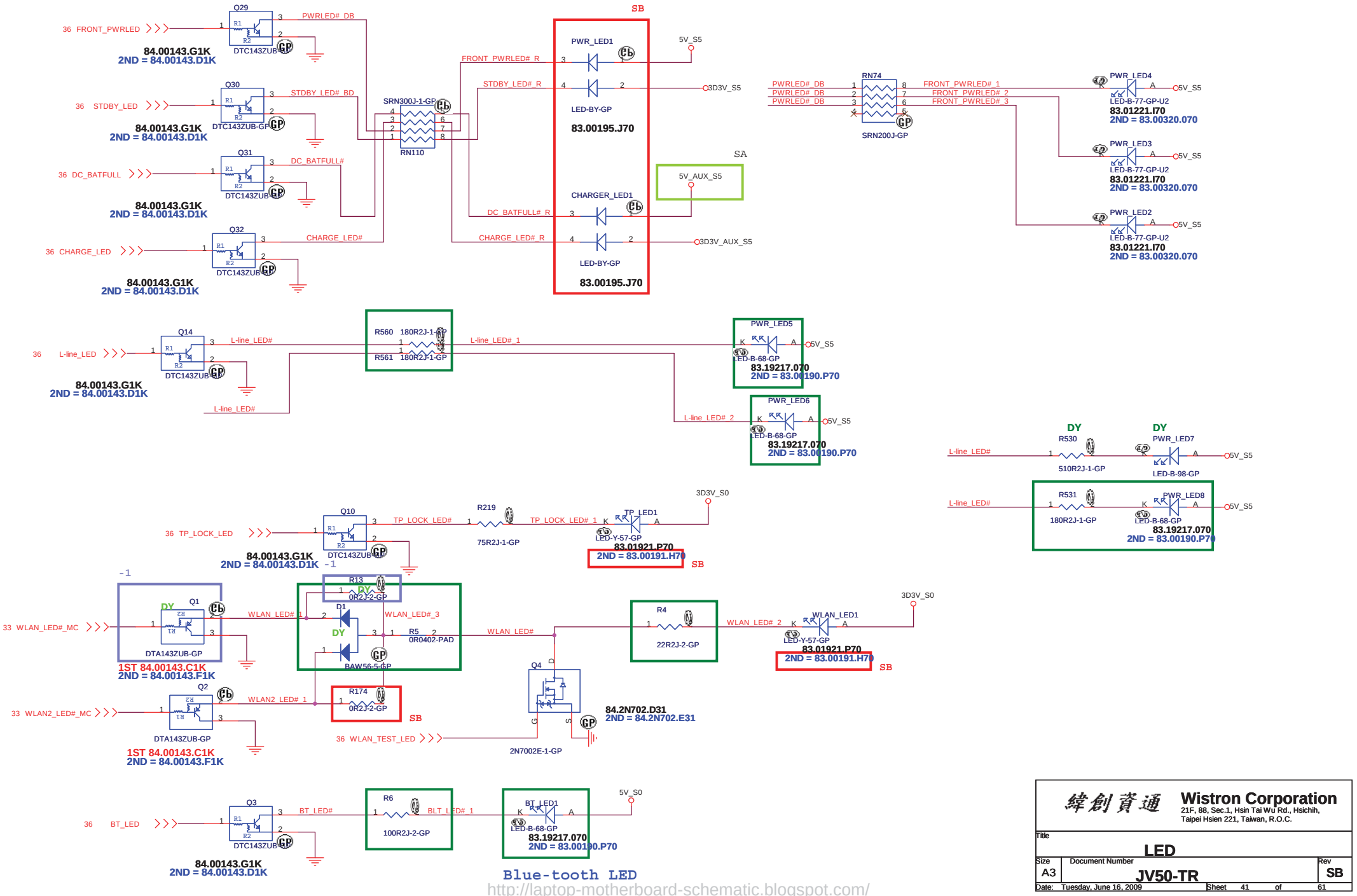

緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED	
Size: A3	Document Number: JV50-TR	Rev: SB
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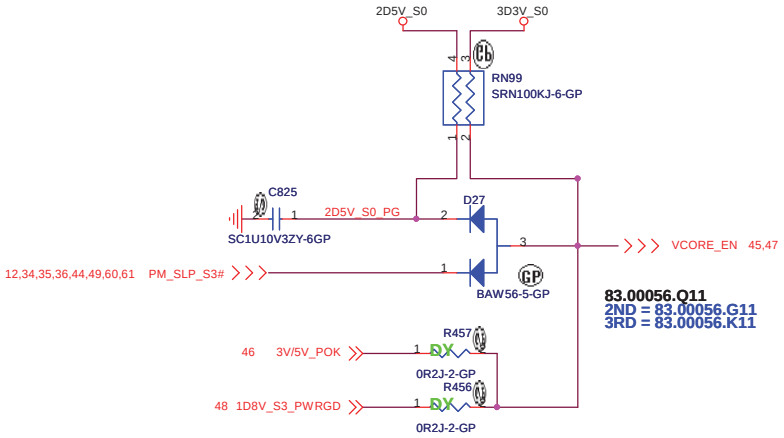
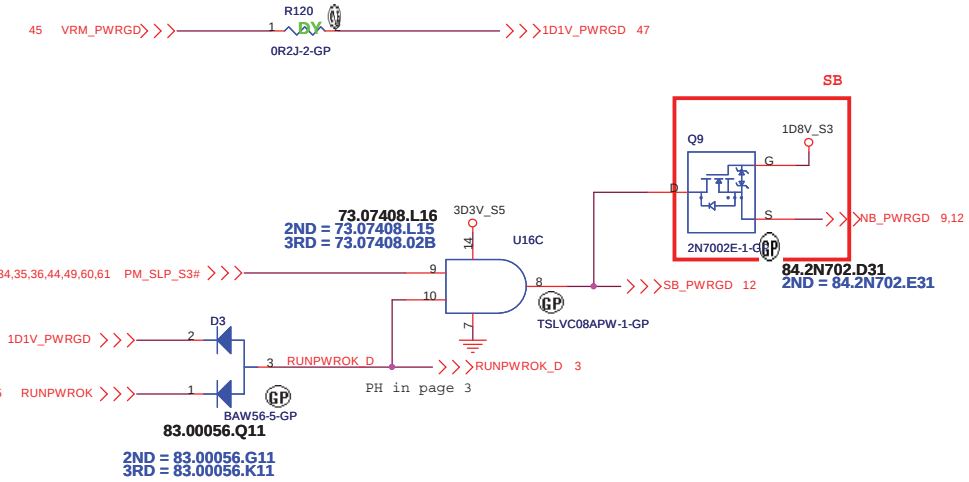


P/H @ 1D8V_S3 PAGE



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

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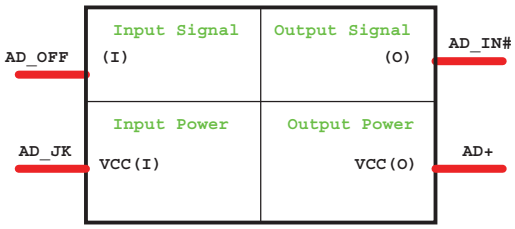
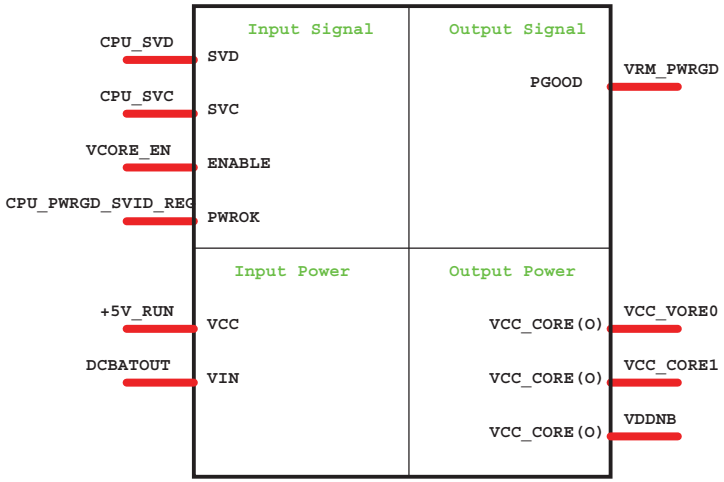
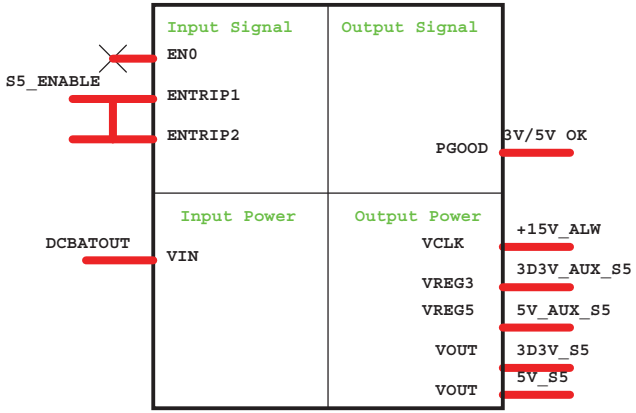
Adapter



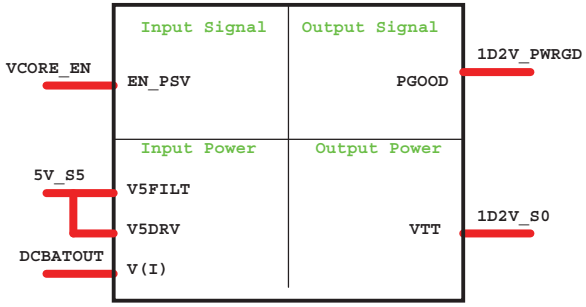
CPU_CORE
ISL6265HRTZ



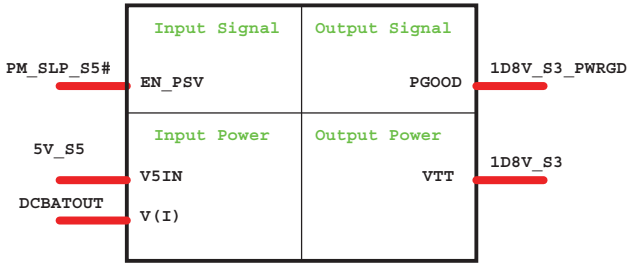
DCDC 5V/3D3V(RT8205A)



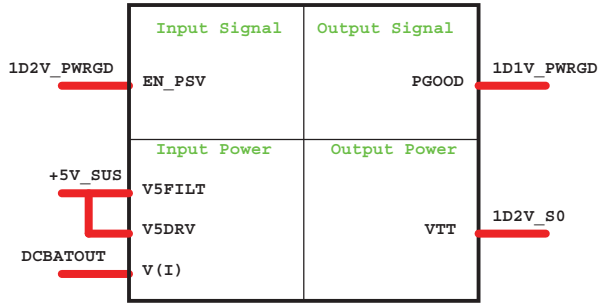
DCDC 1D2V(TPS51124)



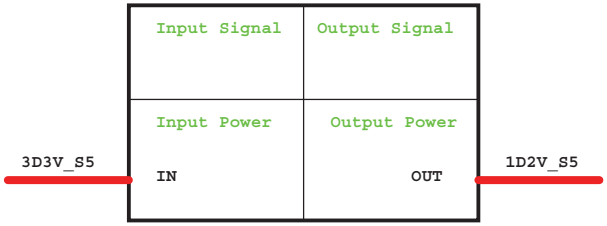
DCDC 1D8V(RT8209B)



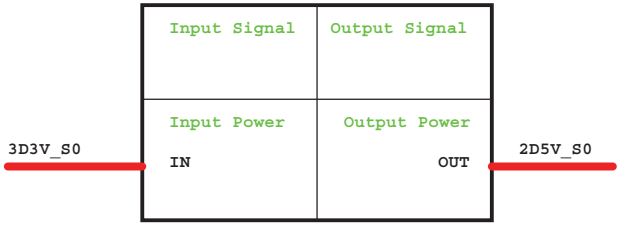
DCDC 1D1V(TPS51124)



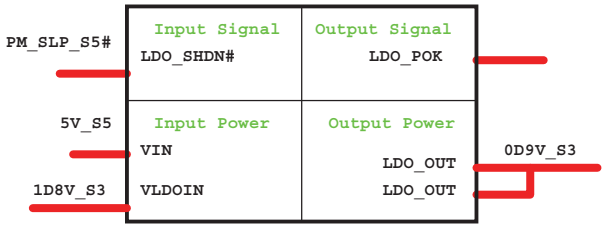
1D2V LDO G9161



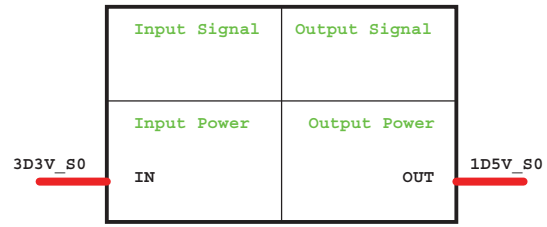
2D5V LDO R9161



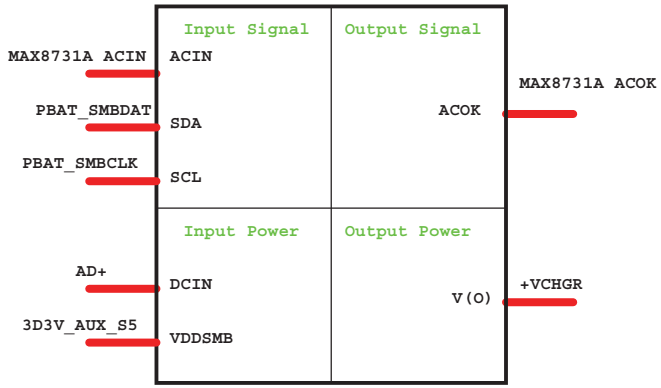
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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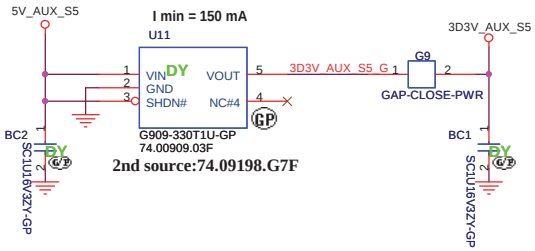
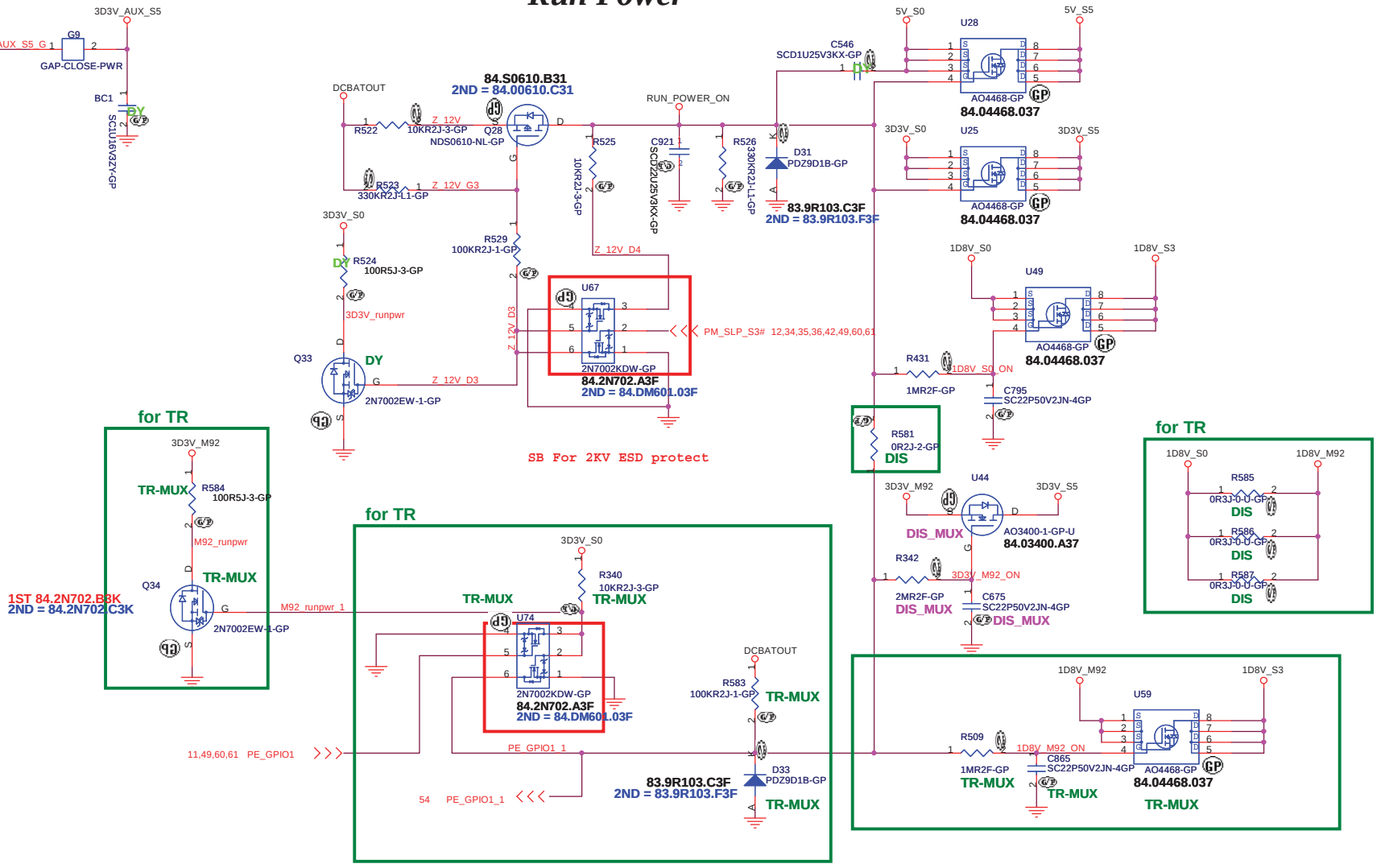
Aux Power 3D3V_AUX_S5



Run Power



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN AND AUX POWER

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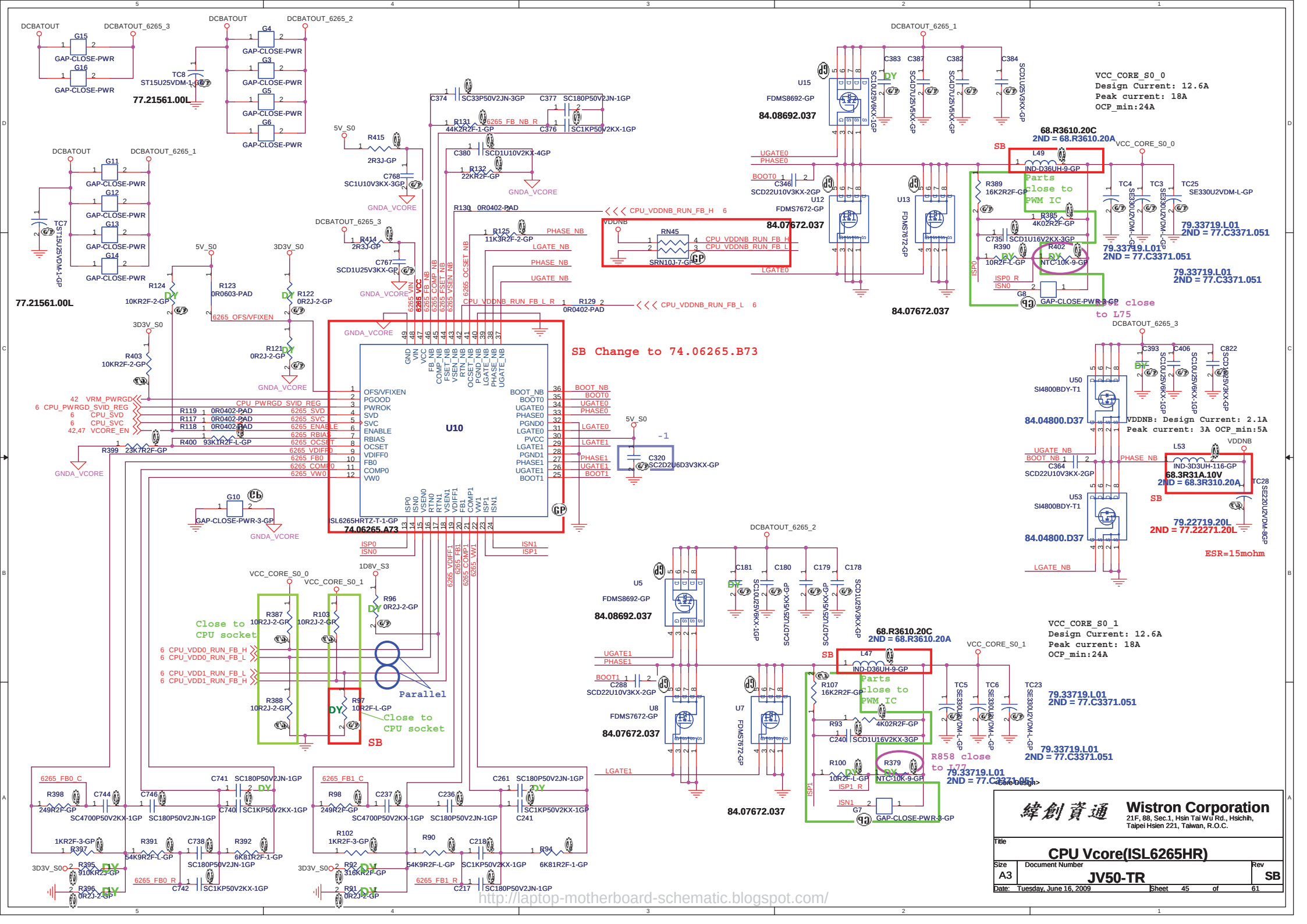
U10
SL6265HRTZ-T-1-GP
74.06265.A73
SB Change to 74.06265.B73
U15
FDMS8692-GP
84.08692.037
U12
FDMS7672-GP
U13
84.07672.037
U5
U8
U7
U50
SI4800BDY-T1
84.04800.D37
U53
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
68.R3610.20C
2ND = 68.R3610.20A
L49
IND-D36UH-9-GP
Parts close to PWM IC
79.33719.L01
2ND = 77.C3371.051
R389 16K2R2F-GP
R385 4K02R2F-GP
R390 10R2F-L-GP
R402 NTC-10K-9-GP
R3 close to L75
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
L47
R107 16K2R2F-GP
R93 4K02R2F-GP
C240 SCD1U16V2KX-3GP
R100 10R2F-L-GP
R379 NTC-10K-9-GP
R858 close to r77
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
L53
IND-3D3UH-116-GP
68.3R31A.10V
2ND = 68.3R310.20A
79.22719.20L
2ND = 77.22271.20L
ESR=15mohm
77.21561.00L
Close to CPU socket
Parallel
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
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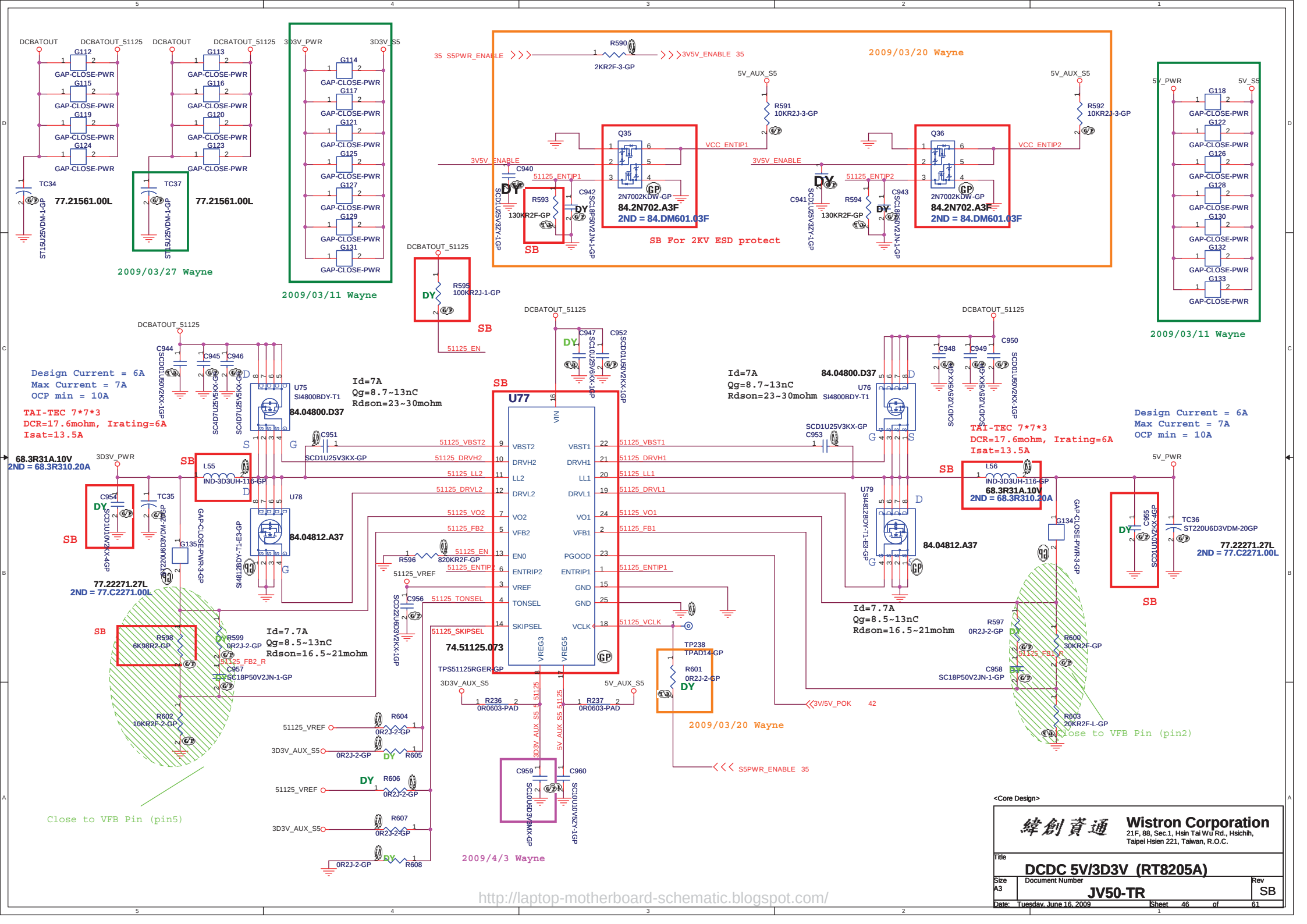
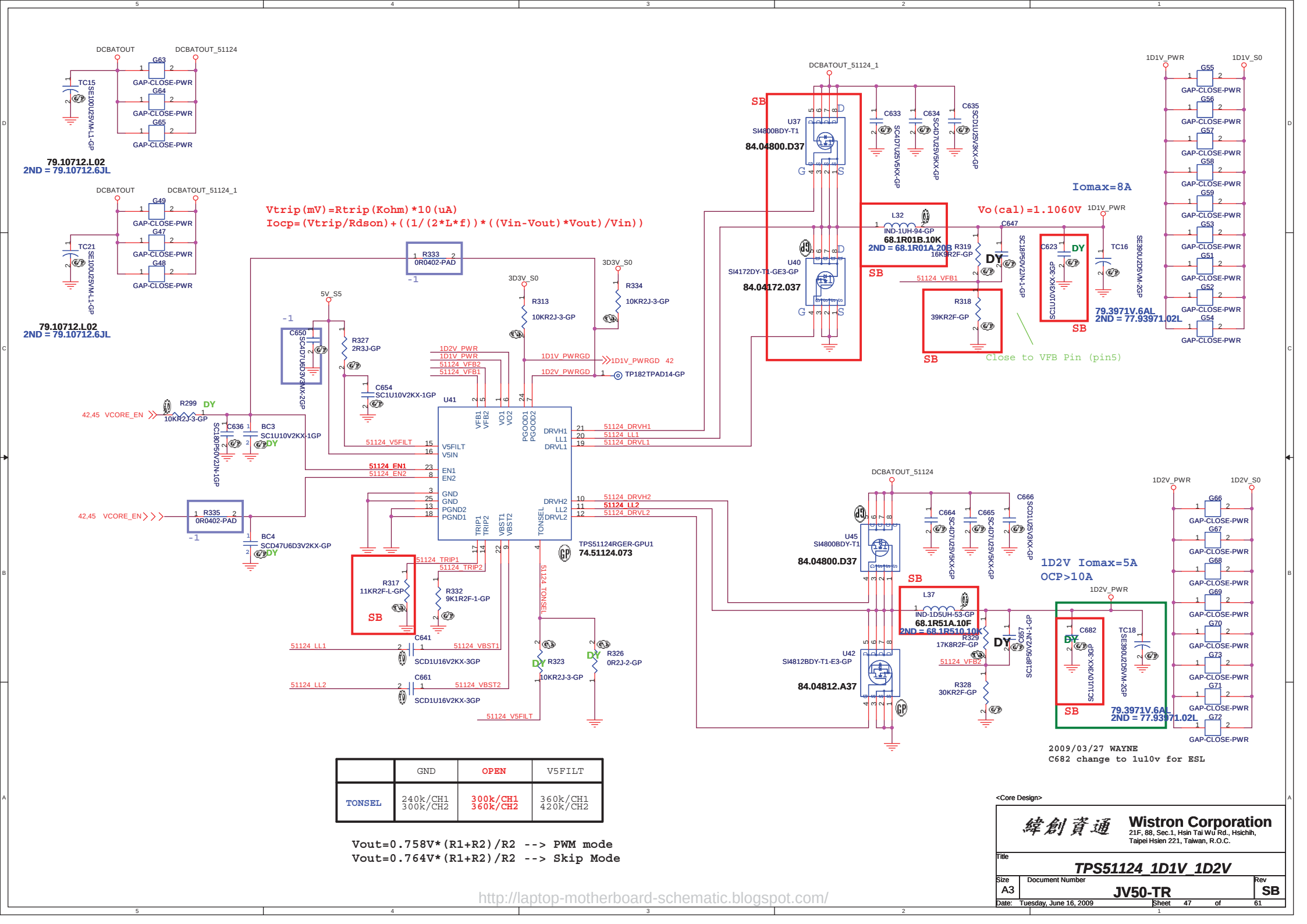

DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
35 S5PWR_ENABLE
3V5V_ENABLE 35
R590
2KR2F-3-GP
R591
10KR2J-3-GP
R592
10KR2J-3-GP
Q35
Q36
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
VCC_ENTIP1
VCC_ENTIP2
3V5V_ENABLE
51125_ENTIP1
51125_ENTIP2
C940
C941
C942
C943
R593
130KR2F-GP
R594
130KR2F-GP
SCD1U25V2ZY-1GP
SC18P50V2JN-1-GP
DY
SB
SB For 2KV ESD protect
2009/03/20 Wayne
2009/03/27 Wayne
2009/03/11 Wayne
TC34
TC37
77.21561.00L
ST15U25VDM-1-GP
G112
G113
G114
G115
G116
G117
G118
G119
G120
G121
G122
G123
G124
G125
G126
G127
G128
G129
G130
G131
G132
G133
GAP-CLOSE-PWR
R595
100KR2J-1-GP
51125_EN
Design Current = 6A
Max Current = 7A
OCP min = 10A
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
84.04800.D37
U75
U76
SI4800BDY-T1
U77
VIN
VBST2
VBST1
DRVH2
DRVH1
LL2
LL1
DRVL2
DRVL1
VO2
VO1
VFB2
VFB1
EN0
PGOOD
ENTRIP2
ENTRIP1
VREF
GND
TONSEL
SKIPSEL
VCLK
VREG3
VREG5
TPS51125RGER-GP
74.51125.073
51125_SKIPSEL
51125_TONSEL
51125_VCLK
51125_VBST2
51125_VBST1
51125_DRVH2
51125_DRVH1
51125_LL2
51125_LL1
51125_DRVL2
51125_DRVL1
51125_VO2
51125_VO1
51125_FB2
51125_FB1
51125_EN
51125_ENTIP2
51125_ENTIP1
51125_VREF
3V/5V_POK 42
S5PWR_ENABLE 35
3D3V_AUX_S5
5V_AUX_S5
68.3R31A.10V
2ND = 68.3R310.20A
L55
L56
IND-3D3UH-116-GP
84.04812.A37
U78
U79
SI4812BDY-T1-E3-GP
77.22271.27L
2ND = 77.C2271.00L
TC35
TC36
ST220U6D3VDM-20GP
R596
820KR2F-GP
R597
0R2J-2-GP
R598
6K98R2-GP
R599
0R2J-2-GP
R600
30KR2F-GP
R601
0R2J-2-GP
R602
10KR2F-2-GP
R603
20KR2F-L-GP
R604
0R2J-2-GP
R605
0R2J-2-GP
R606
0R2J-2-GP
R607
0R2J-2-GP
R608
0R2J-2-GP
R236
0R0603-PAD
R237
0R0603-PAD
TP238
TPAD14-GP
C947
C948
C949
C950
C951
C952
C953
C954
C955
C956
C957
C958
C959
C960
SCD1U25V3KX-GP
SCD1U50V2KX-1GP
SC4D7U25V5KX-GP
SCD1U10V2KX-4GP
SCD22U6D3VMX-GP
SC18P50V2JN-1-GP
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
2009/4/3 Wayne
2009/03/20 Wayne
2009/03/11 Wayne
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
Size
A3
Document Number
JV50-TR
Rev
SB
Date: Tuesday, June 16, 2009
Sheet 46 of 61
http://laptop-motherboard-schematic.blogspot.com/



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

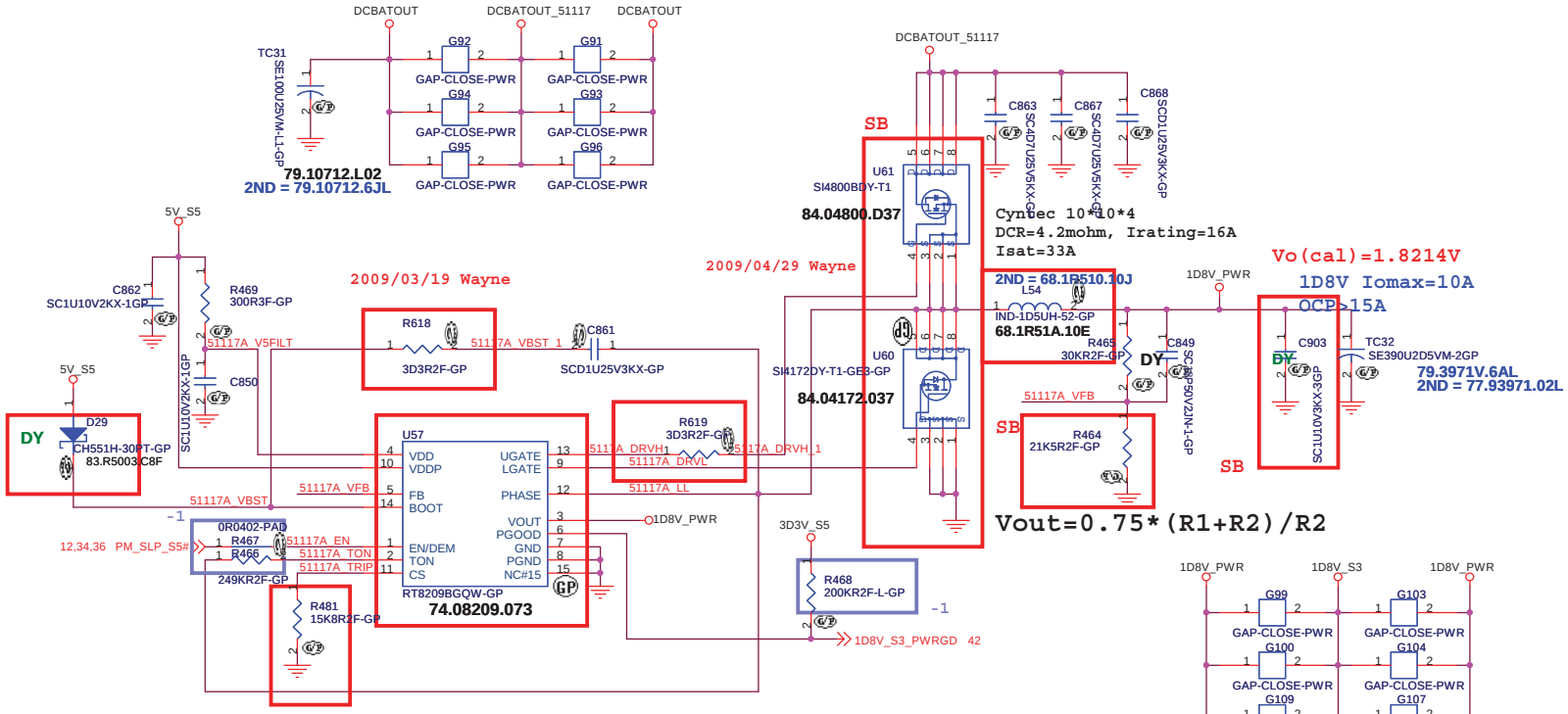
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

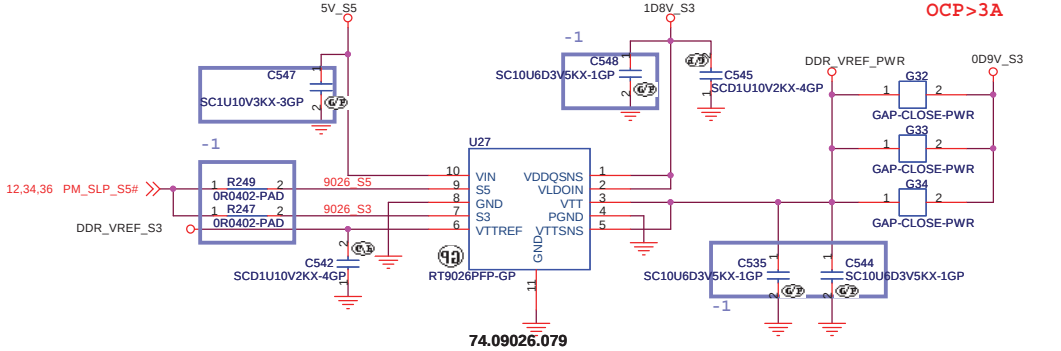
Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 47 of 61



DDR_0.9V

Iomax=1.5A
OCP>3A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

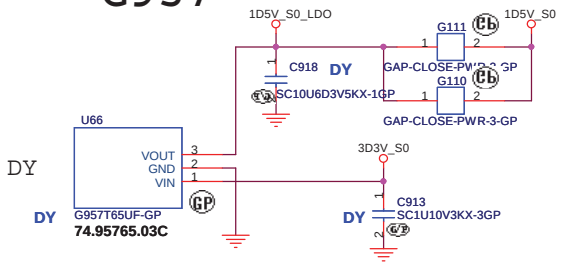
Title: DCDC_1D8V_RT8209B/LDO 0D9V

Size	Document Number	Rev
A3	JV50-TR	SB

Date: Tuesday, June 16, 2009 Sheet 48 of 61

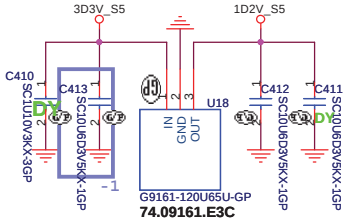
1D5V_S0
Iomax=1A

G957



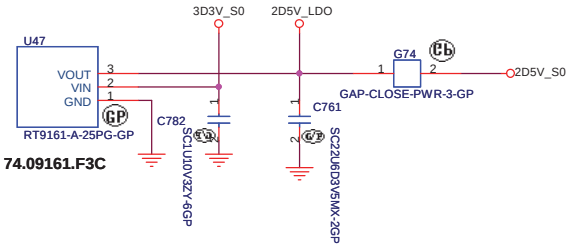
For MINI Card.NEW Card power SW

1D2V_S5
Iomax=400mA



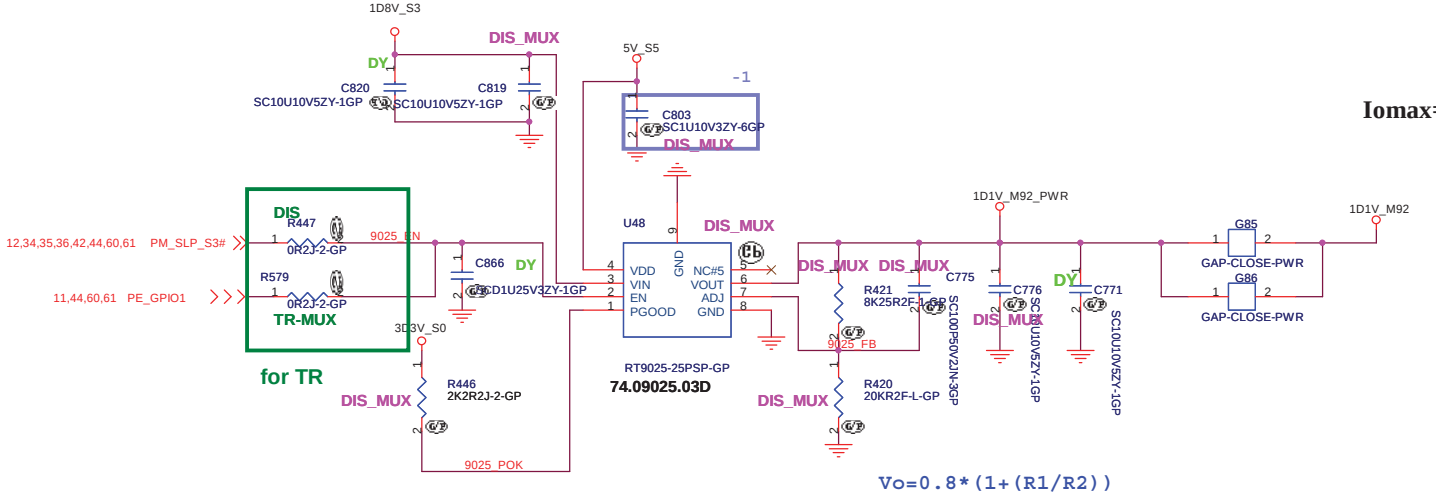
Place near to SB700

2D5V
Iomax=0.2A



Place near to CPU

Iomax=0.8A



Vo=0.8*(1+(R1/R2))

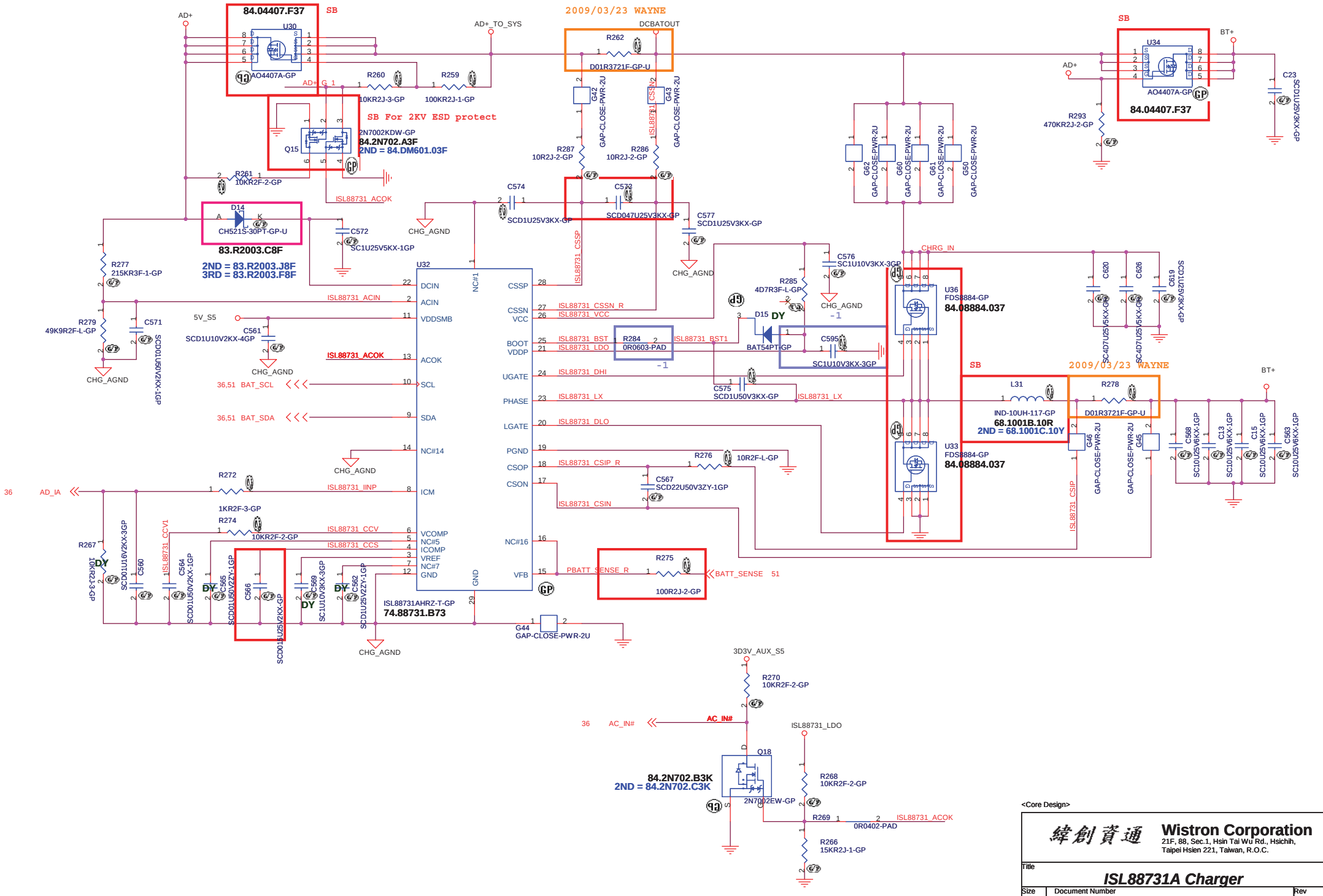
<Core Design>

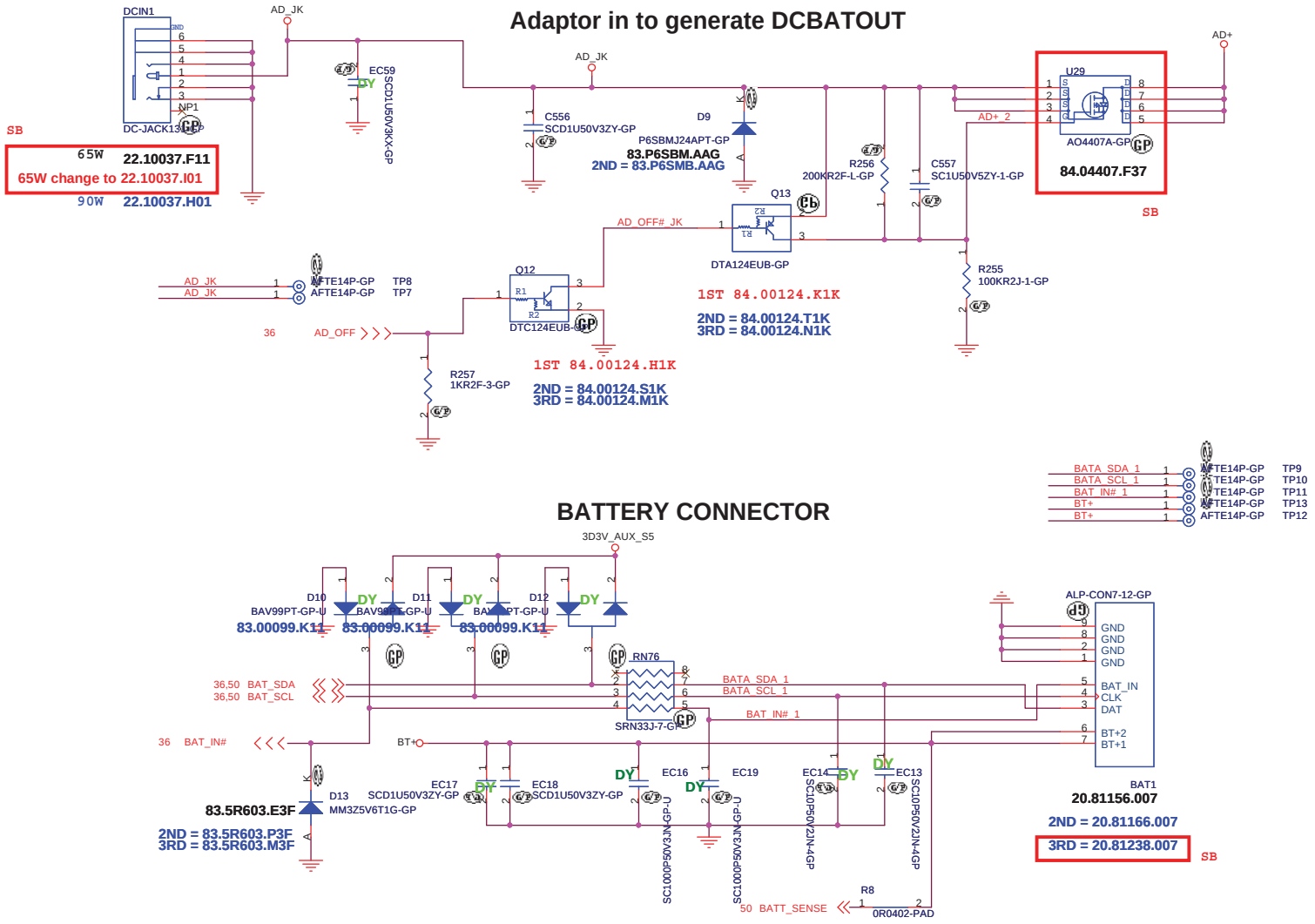
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 2D5V/1D5V/1D2V_S5

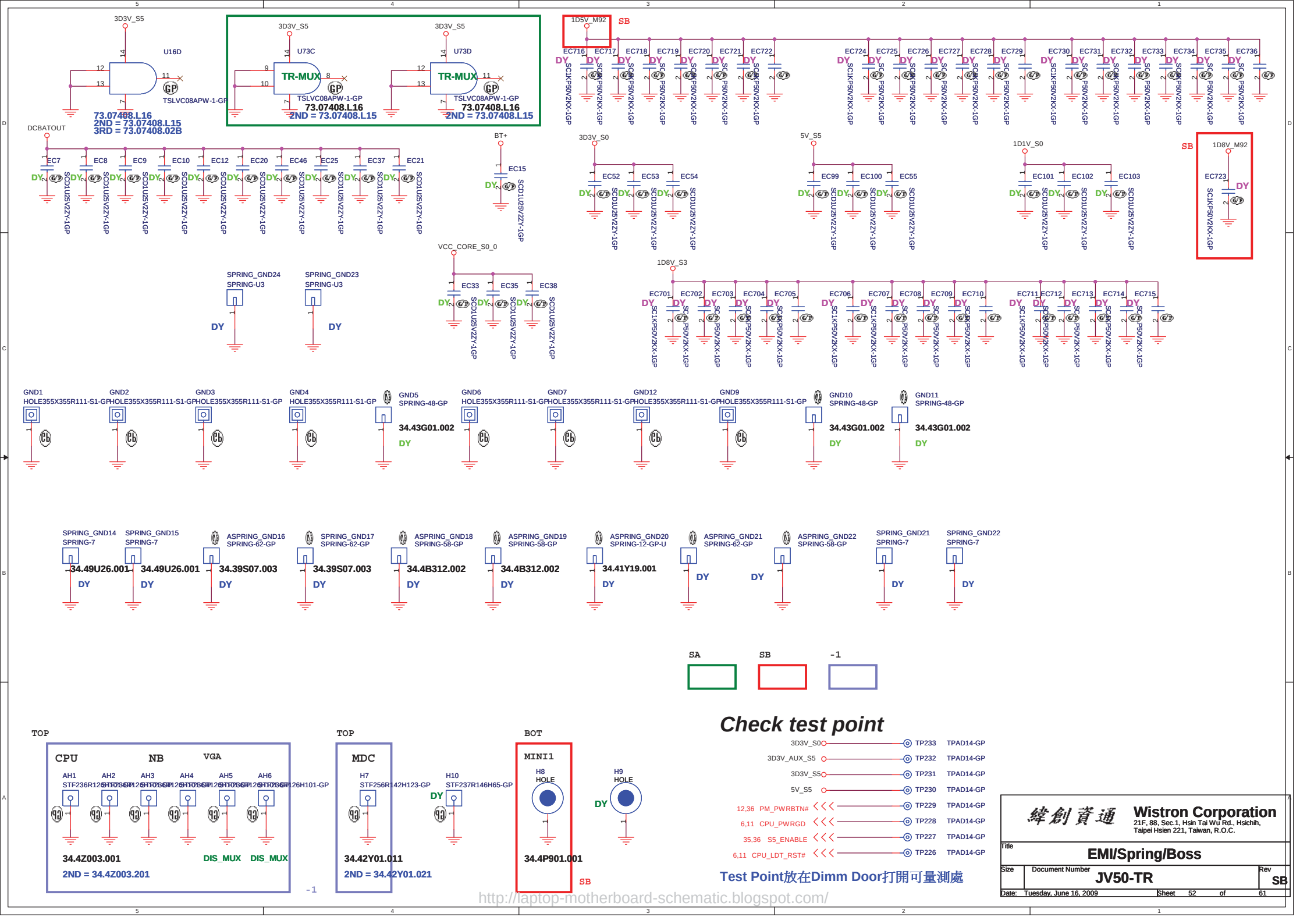
Size: A3 | Document Number: JV50-TR | Rev: SB

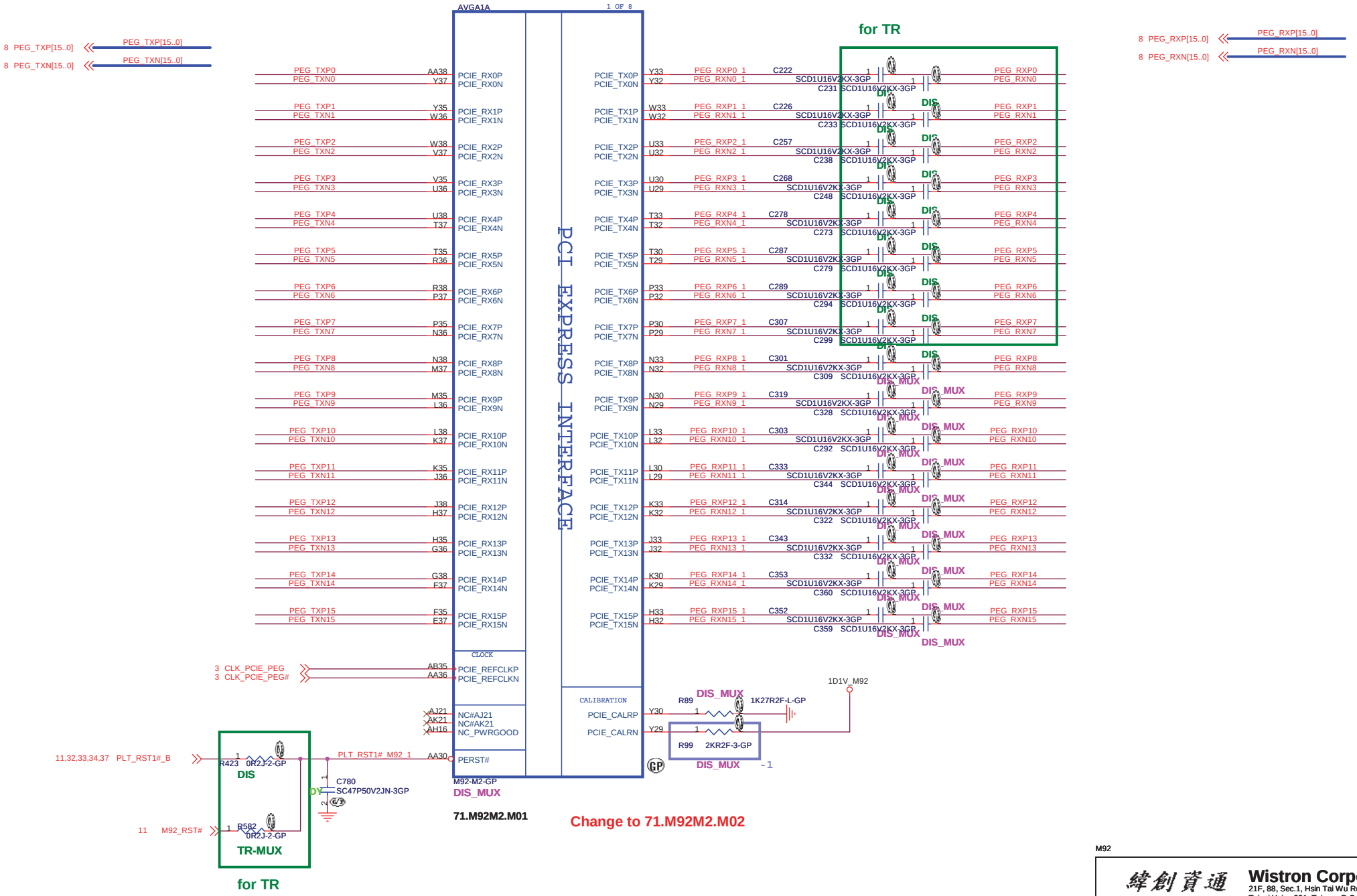
Date: Tuesday, June 16, 2009 | Sheet 49 of 61

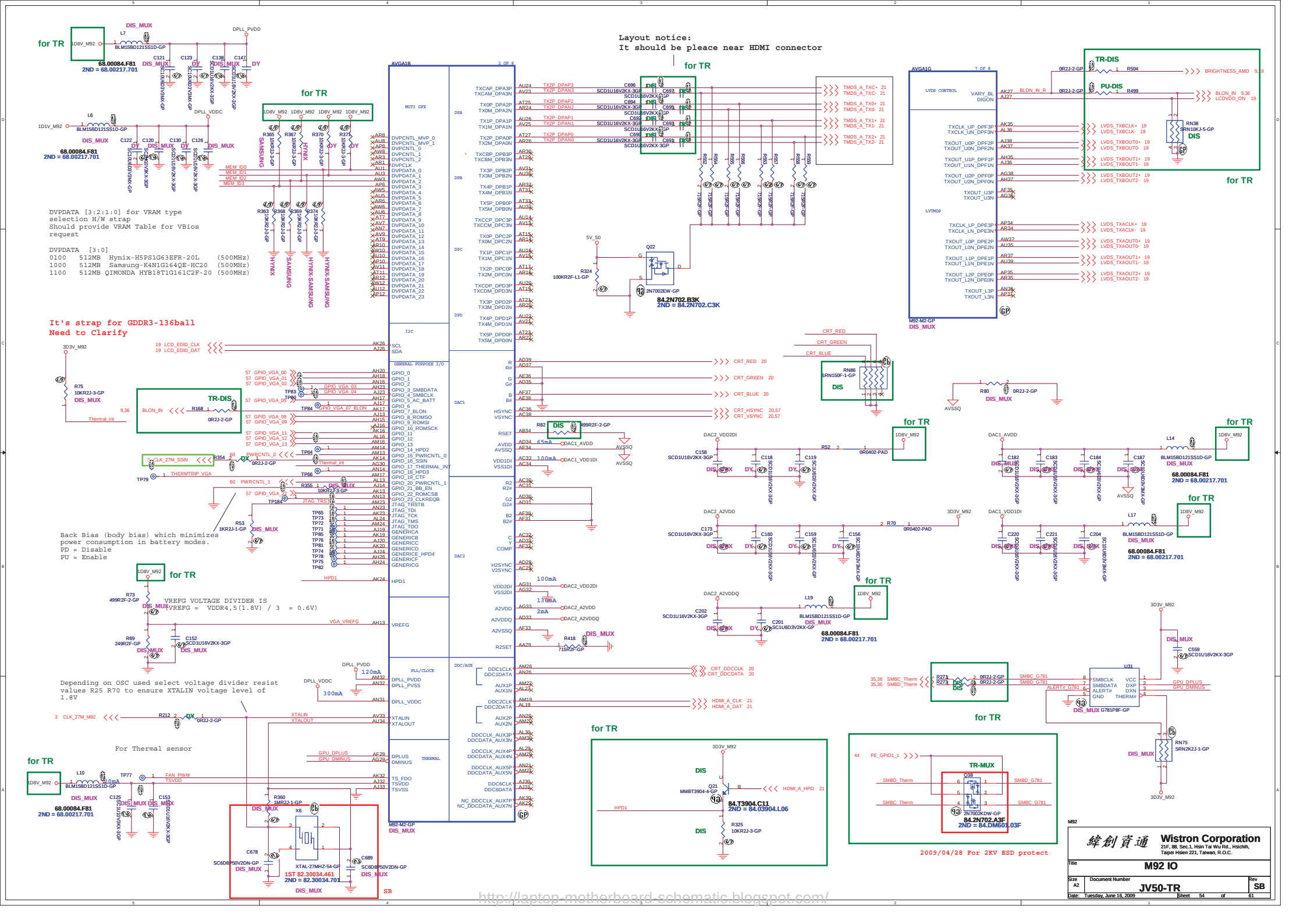


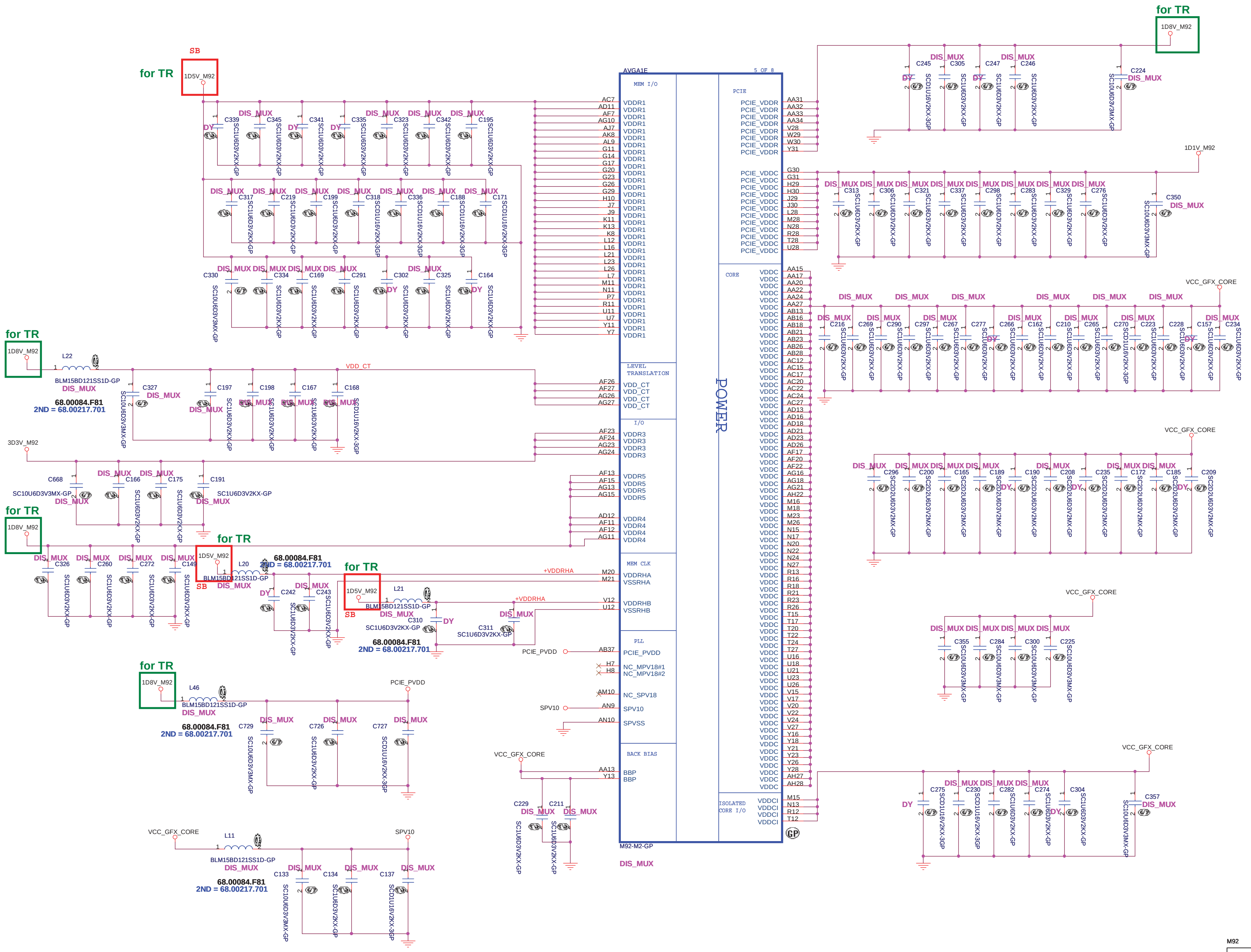


緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: AD/BATT CONN		
Size	Document Number: JV50-TR	Rev: SB
Date: Tuesday, June 16, 2009	Sheet 51 of 61	





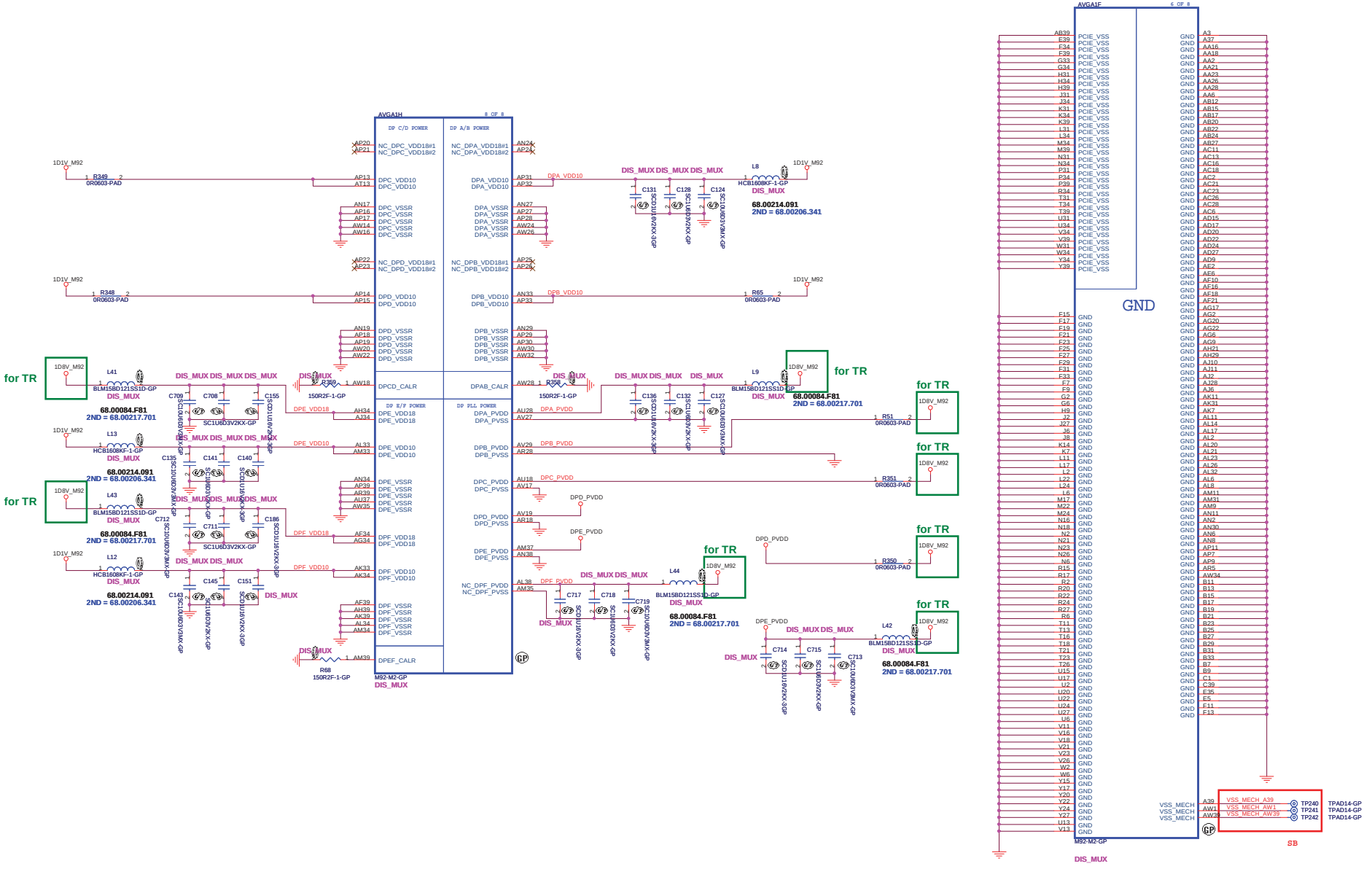

Layout notice:
It should be pleace near HDMI connector
for TR
DIS_MUX
DPLL_PVDD
DPLL_VDDC
68.00084.F81
2ND = 68.00217.701
68.00084.F81
2ND = 68.00217.701
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
SAMSUNG
HYNIX
HYNIX-SAMSUNG
It's strap for GDDR3-136ball
Need to Clarify
TR-DIS
Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V
For Thermal sensor
XTAL-27MHZ-54-GP
1ST 82.30034.461
2ND = 82.30034.701
SB
AVGA1B
MUTI GFX
GENERAL PURPOSE I/O
M92-M2-GP
DIS_MUX
AVGA1G
LVDS CONTROL
LVTMDP
PU-DIS
BRIGHTNESS_AMD
BLON_IN
LCDVDD_ON
LVDS_TXBCLK+
LVDS_TXBCLK-
LVDS_TXBOUT0+
LVDS_TXBOUT0-
LVDS_TXBOUT1+
LVDS_TXBOUT1-
LVDS_TXBOUT2+
LVDS_TXBOUT2-
LVDS_TXACLK+
LVDS_TXACLK-
LVDS_TXAOUT0+
LVDS_TXAOUT0-
LVDS_TXAOUT1+
LVDS_TXAOUT1-
LVDS_TXAOUT2+
LVDS_TXAOUT2-
TMDS_A_TXC+
TMDS_A_TXC-
TMDS_A_TX0+
TMDS_A_TX0-
TMDS_A_TX1+
TMDS_A_TX1-
TMDS_A_TX2+
TMDS_A_TX2-
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_HSYNC
CRT_VSYNC
CRT_DDCCLK
CRT_DDCDATA
HDMI_A_CLK
HDMI_A_DAT
HDMI_A_HPD
SMBC_Therm
SMBC_G781
ALERT# G781
GPU_DPLUS
GPU_DMINUS
TR-MUX
PE_GPIO1_1
2009/04/28 For 2KV ESD protect
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
M92 IO
JV50-TR
SB
Tuesday, June 16, 2009
http://laptop-motherboard-schematic.blogspot.com/



M92

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

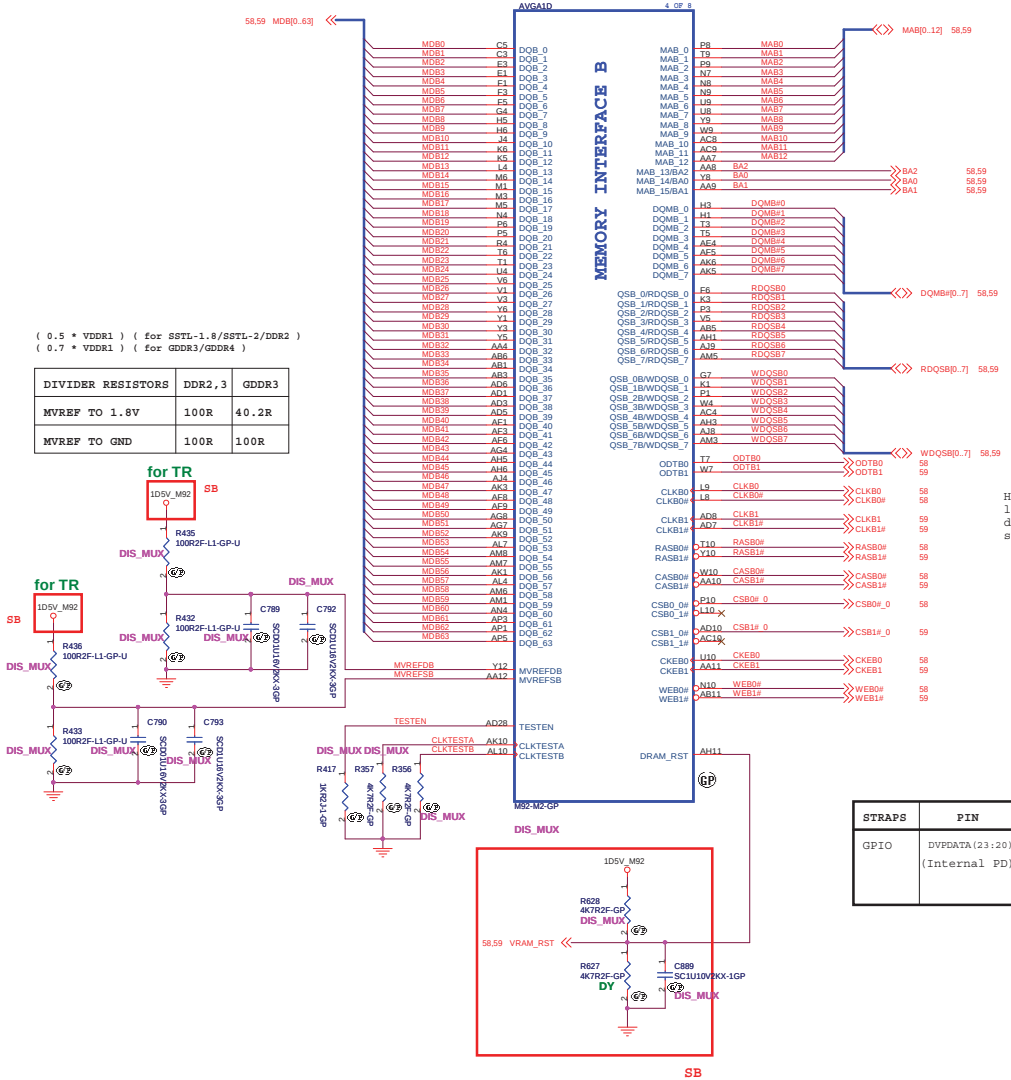
Title	M92 POWER	
Size A2	Document Number JV50-TR	Rev SB
Date: Tuesday, June 16, 2009	Sheet 55 of 61	



M92

緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DP POWER_GND	
Size A2	Document Number JV50-TR	Rev SB
Date: Tuesday, June 16, 2009	Sheet 56 of 61	

M92-M2 uses memory group B only



DIVIDER RESISTORS	DDR2,3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
V 64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x			
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

M92

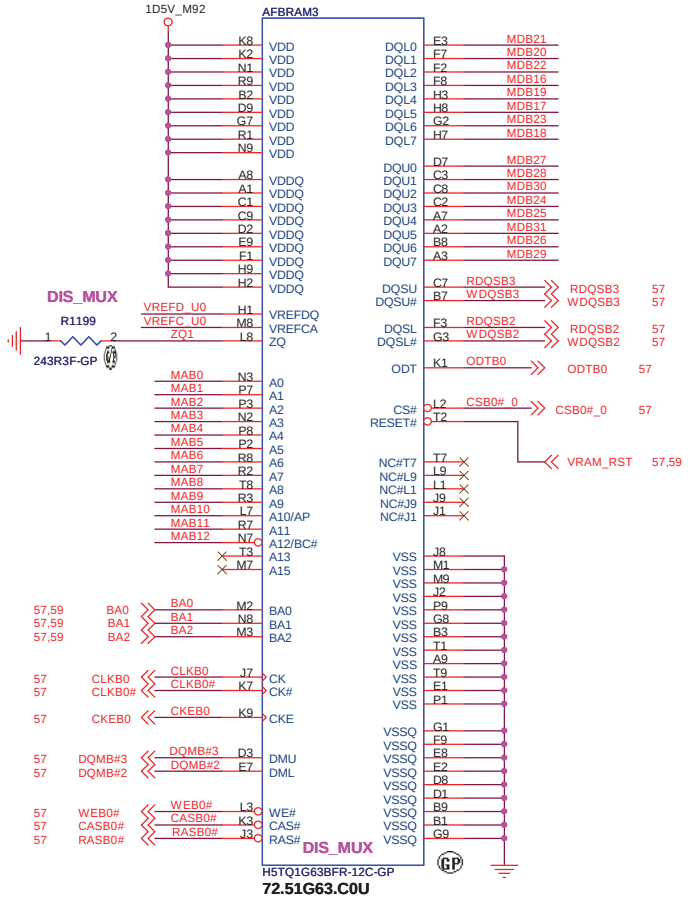
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

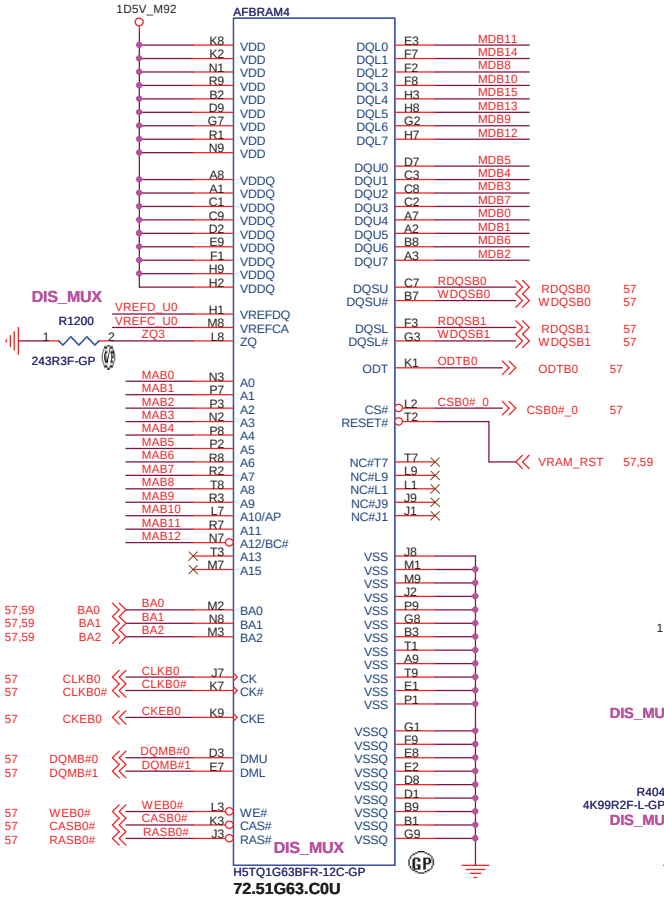
Title: Memory / Straps

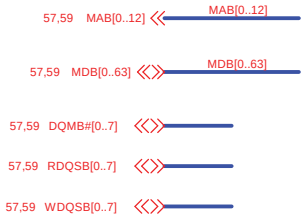
Size: A2 | Document Number: JV50-TR | Rev: SB

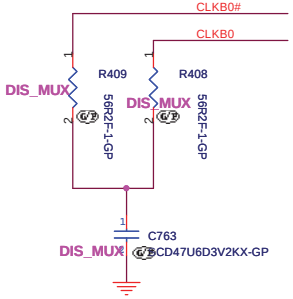
Date: Tuesday, June 16, 2009 | Sheet 57 of 61

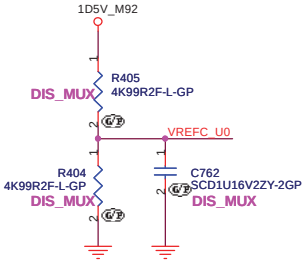
DDR3

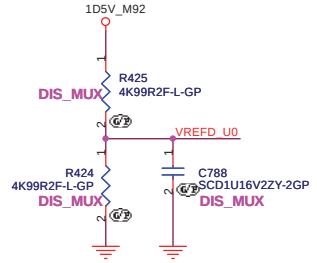












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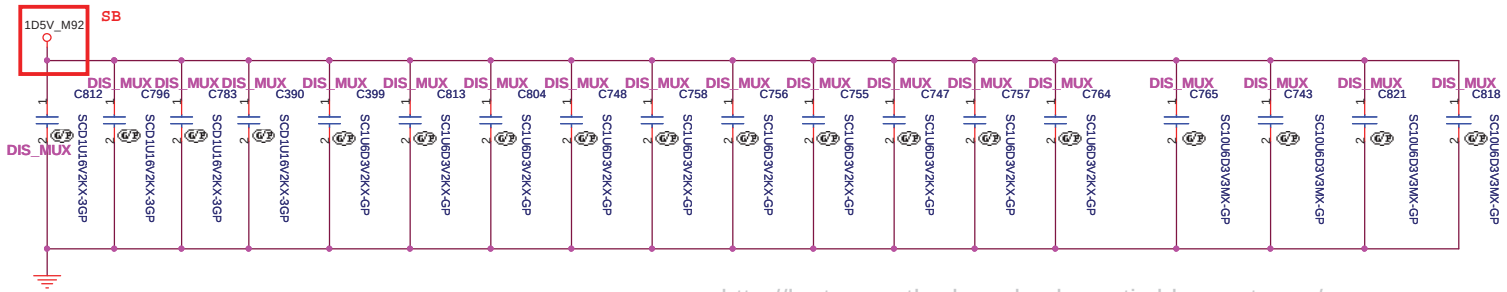
HYUNIX 2ND=72.51G63.C0U

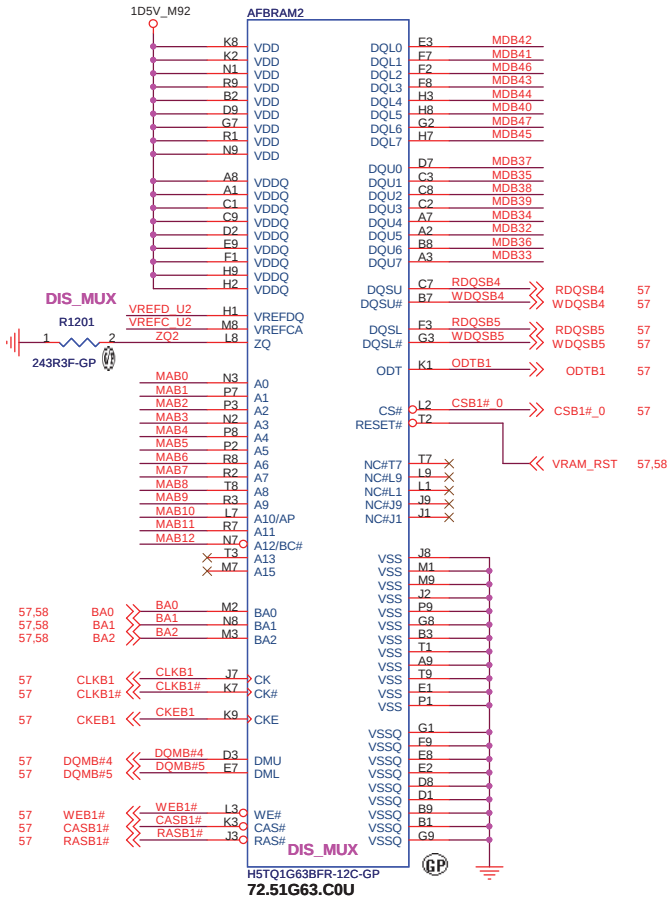


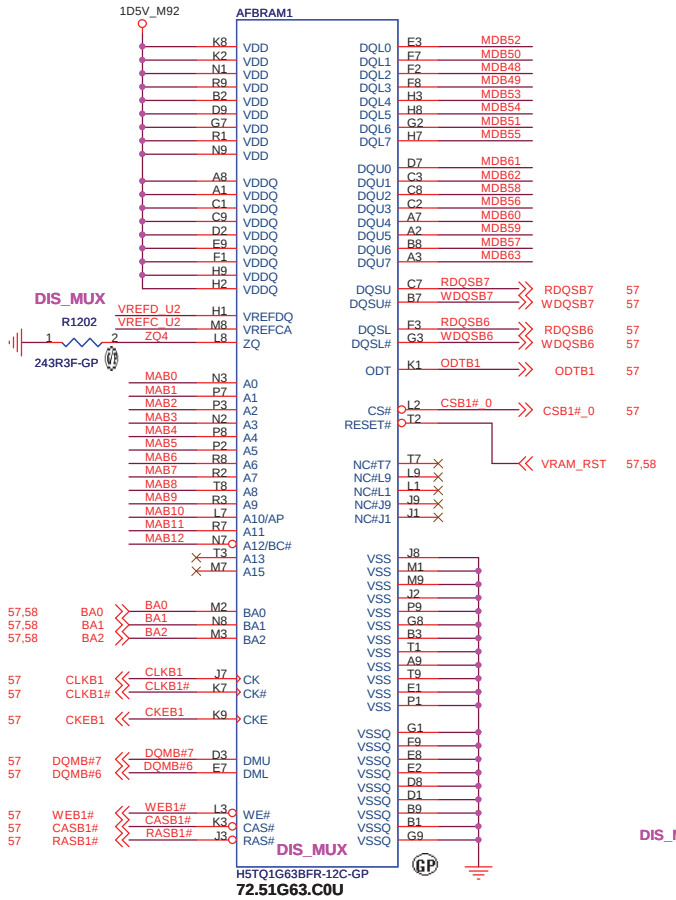
M92

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

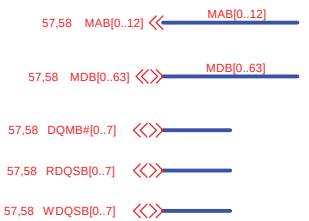
Title	M92 DDR3 B0	
Size A3	Document Number JV50-TR	Rev A
Date: Tuesday, June 16, 2009	Sheet 58 of 61	

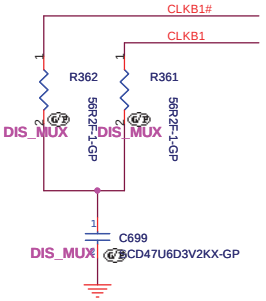
DDR3

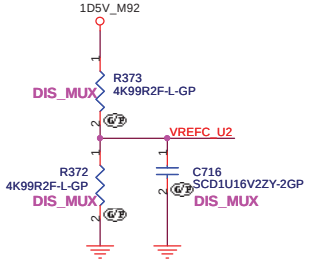


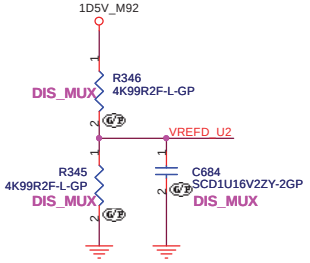


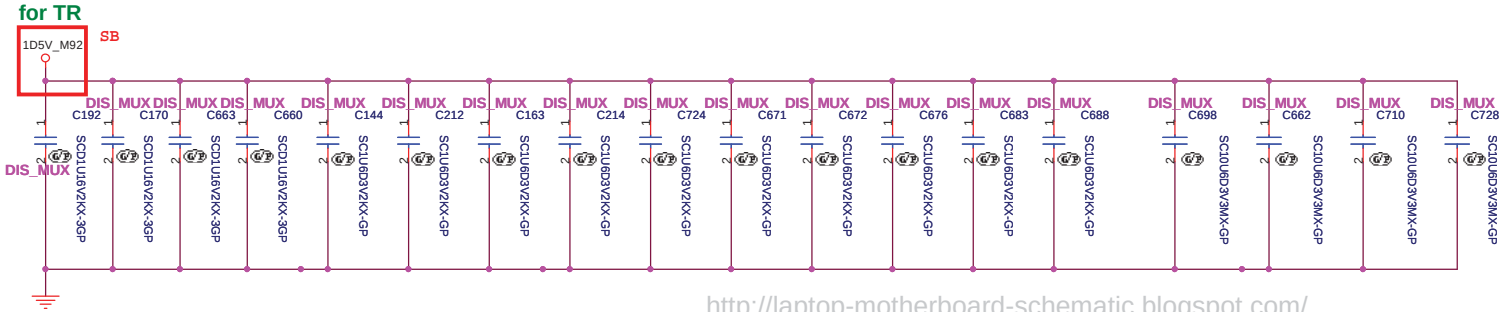
SAMSUNG 1ST=72.41164.H0U
HYUNIX 2ND=72.51G63.C0U







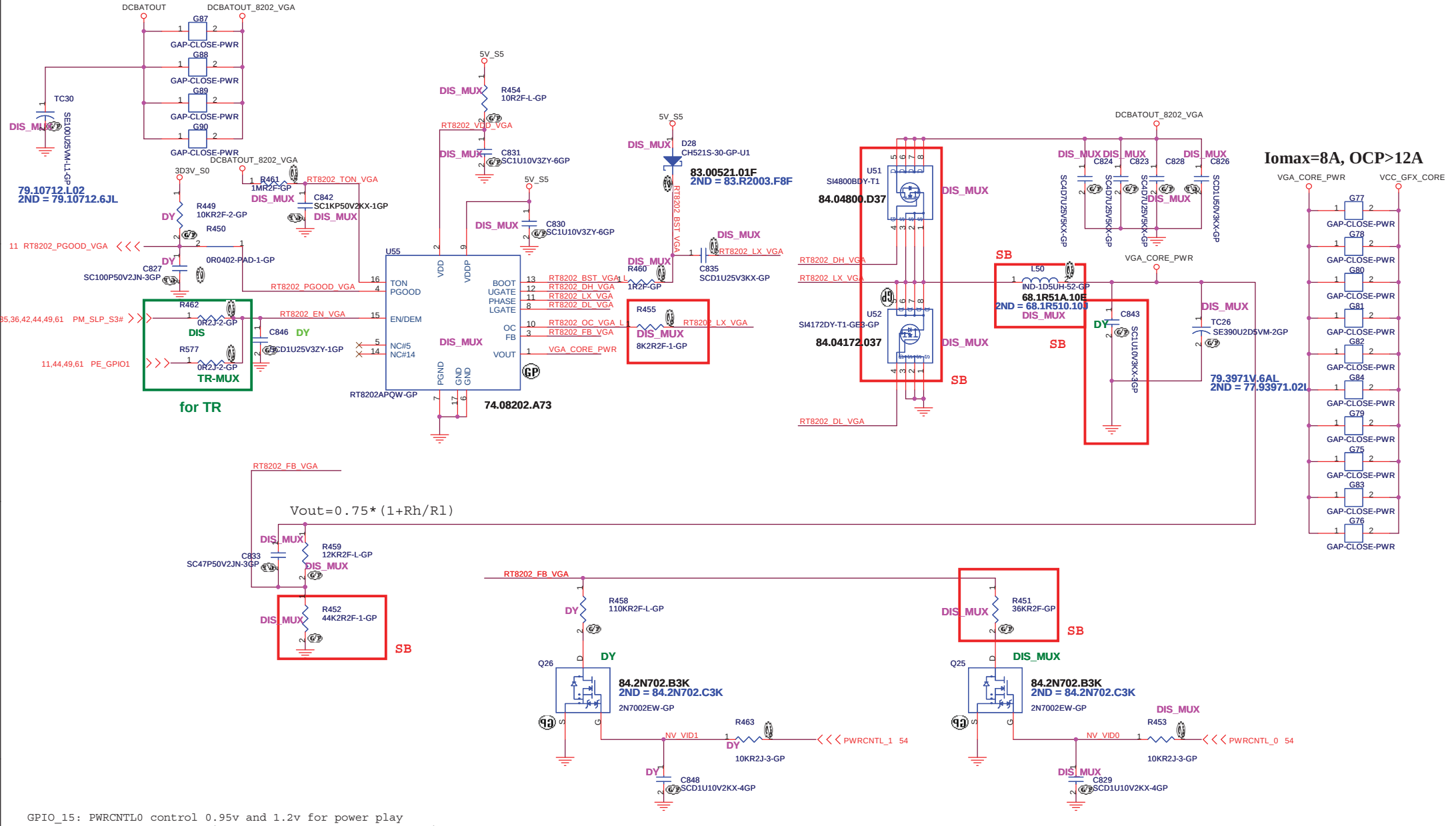




M92

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	M92 DDR3 B1	
Size A3	Document Number JV50-TR	Rev SB
Date: Tuesday, June 16, 2009	Sheet 59 of 61	

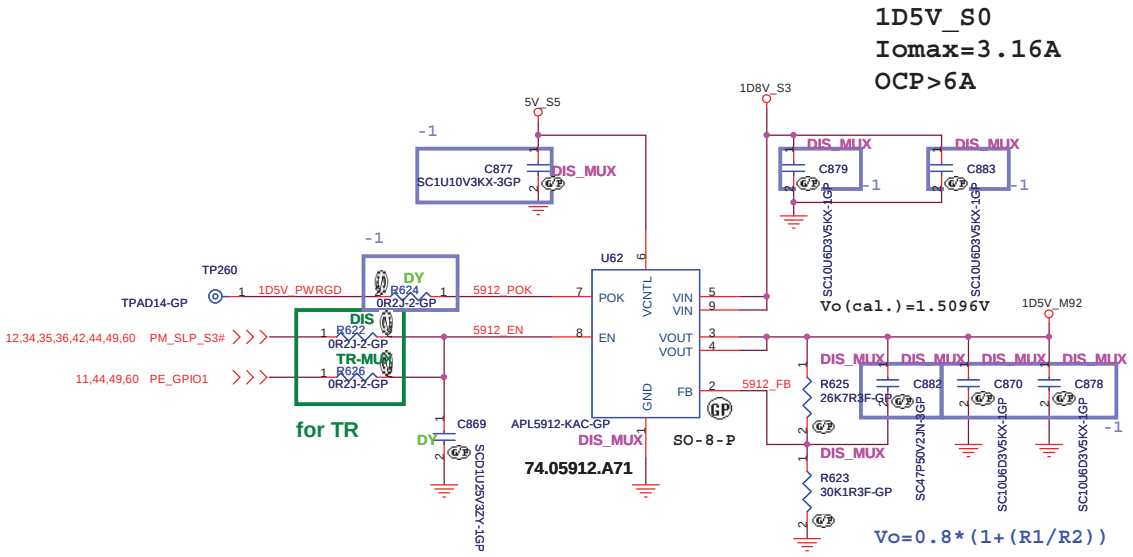


GPIO_15: PWRCNTL0 control 0.95v and 1.2v for power play
M92 XT - PowerPlay States will base your power control setting change as below,
High state: 1.2V, e680/m500MHz
Medium state: 0.95V, e300/m500 MHz
Low state: 0.95V, e220/m250 MHz
UVD state: 1.2V, e600/m500 MHz

	I/O	Inter pull low	GPIO TABLE
PWRCNTL_0	O	Yes	GPU Voltage H:=1.210V GPU Voltage L:=0.954V

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202A VGA CORE
Size: A3
Document Number: JV50-TR
Rev: SB
Date: Tuesday, June 16, 2009
Sheet 60 of 61



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: APL5912 1D5V VRAM POWER

Size: A3 | Document Number: JV50-TR | Rev: SB

Date: Tuesday, June 16, 2009 | Sheet 61 of 61